SEALing Neural Network Models in Secure Deep Learning Accelerators

Pengfei Zuo†, Yu Hua†, Ling Liang†, Xinfeng Xie†, Xing Hu†, Yuan Xie†
Huazhong University of Science and Technology
† Scalable Energy-efficient Architecture Lab (SEAL), University of California, Santa Barbara

ABSTRACT

Deep learning (DL) accelerators are increasingly deployed on edge devices to support fast local inferences. However, they suffer from a new security problem, i.e., being vulnerable to physical access based attacks. An adversary can easily obtain the entire neural network (NN) model by physically snooping the GDDR (graphics double data rate) memory bus that connects the accelerator chip with DRAM memory. Therefore, memory encryption becomes important for DL accelerators on edge devices to improve the security of NN models. Nevertheless, we observe that traditional memory encryption solutions that have been efficiently used in CPU systems cause significant performance degradation when directly used in DL accelerators. The main reason comes from the big bandwidth gap between the GDDR memory bus and the encryption engine. To address this problem, our paper proposes SEAL, a Secure and Efficient Accelerator scheme for deep Learning. SEAL enhances the performance of the encrypted DL accelerator from two aspects, i.e., improving the data access bandwidth and the efficiency of memory encryption. Specifically, to improve the data access bandwidth, SEAL leverages a criticality-aware smart encryption scheme which identifies partial data that have no impact on the security of NN models and allows them to bypass the encryption engine, thus reducing the amount of data to be encrypted. To improve the efficiency of memory encryption, SEAL leverages a co-location mode encryption scheme to eliminate memory accesses from counters used for encryption by co-locating data and their counters. Our experimental results demonstrate that, compared with traditional memory encryption solutions, SEAL achieves $1.4 \times -1.6 \times$ IPC improvement and reduces the inference latency by $39\% - 60\%$. Compared with a baseline accelerator without memory encryption, SEAL compromises only $5\% - 7\%$ IPC for significant security improvement.

1. INTRODUCTION

Machine learning techniques, especially deep learning (DL), have made significant progress in the past few years, whose performances have surpassed those of humans in some application domains, such as image classification [25, 36, 67], speech recognition [12, 20, 76], and games [66]. With the increase of computing performance and storage capacity of edge devices, DL systems are increasingly expanded and used from cloud to edge devices [19, 75], such as self-driving cars [31] and Internet-of-things devices [40]. By employing DL accelerators, e.g., GPU and NPU, edge devices are able to carry out real-time local inferences based on current environments without a connection with a remote control center with high latency. For example, over 99% smartphones are equipped with a GPU by 2019 [63, 70]. The self-driving computer within Tesla cars [7] and Google edge TPU [64] also include a GPU.

In DL accelerators, neural network (NN) models are confidential information that needs to be protected. Because NN models represent the Intellectual Property (IP) of model owners, which should be confidentially protected to preserve their competitive advantages. More importantly, the knowledge of NN models can facilitate an adversary to carry out more powerful adversarial attacks [18, 69]. In adversarial attacks, an adversary is able to intentionally affect the outcome of the DL inference by modifying the input data with a slight perturbation that is imperceptible to humans. For example, by performing adversarial attacks, an adversary is able to manipulate self-driving cars [16] and trick the speaker recognition system in smartphones [6]. In general, if the adversary does not know the NN model, the success rate of the adversarial attack is low. With the knowledge of the NN model, the success rate is significantly improved [44, 53].

However, DL accelerators deployed on edge devices suffer from a new security issue compared with those deployed on the cloud. The reason is that DL accelerators on edge devices are easier to be physically accessed, thus being vulnerable to physical access based attacks. The accelerator chip and DRAM themselves are usually well packaged and hence secure to physical access, but the memory bus collecting accelerator and DRAM is not secure, due to being vulnerable to bus snooping attacks [27, 29, 30, 77]. Since the DL accelerator has to access the NN model stored in the DRAM memory through the GDDR memory bus during the inference, an adversary can easily obtain the entire NN model by inserting a bus snooper on the GDDR bus to intercept the data communicated between the DL accelerator chip and the DRAM memory. Therefore, memory encryption for encrypting the data transmitted between the DL accelerator chip and the DRAM memory is important.

There are two existing memory encryption models in secure CPU systems including direct encryption and counter mode encryption. Direct encryption encrypts all memory lines by using the same global key. It has a low security level since the same data are always encrypted to the same ciphertext, leaving the direct encryption vulnerable to dictionary and retry attacks [3]. Counter mode encryption [41] encrypts a memory line by using a globe key in conjunction with its line address and a per-line counter. Thus the same plaintexts are encrypted to different ciphertexts, achieving a high security level. Counter mode encryption needs to
maintain a counter cache on the CPU chip. When accessing a memory line, if its corresponding counter is found in the counter cache, its decryption latency is hidden in the memory read latency to improve the system performance. The reason is that counter mode encryption generates a one-time pad (OTP) using the counter in parallel with the memory read and decrypts the memory line by XORing the OTP with the data. Due to the benefit of hiding decryption latency, counter mode encryption only incurs about 5% performance overhead in CPU systems [77].

However, we observe that employing these memory encryption techniques in DL accelerators significantly decreases their performance. The IPC (instruction per cycle) of the DL accelerator is reduced by over 50% after using memory encryption, as evaluated in Section 2.4. Such a significant performance decrease is unacceptable for the latency-sensitive DL accelerators on edge devices that must carry out real-time inferences based on current environments, e.g., self-driving cars. The main reason comes from the big bandwidth gap between the GDDR memory bus and the encryption engine. For DL accelerators, e.g., GPUs, their performance is highly bandwidth-bounded and hence the GDDR memory is designed for GPUs to achieve high memory access bandwidth. The bandwidth of the GDDR memory bus is generally higher than 160GB/s [49, 50, 51, 52]. However, the state-of-the-art encryption engine with hardware implementation achieves only about 8GB/s of bandwidth on average [15, 42, 45, 46, 62]. Even though we deploy one encryption engine in every memory controller, the big bandwidth gap remains. As a result, the high bandwidth of the GDDR memory bus is under-utilized and the encryption engine becomes the bandwidth bottleneck in secure DL accelerators. Moreover, since the data access bandwidth is the performance bottleneck, counter mode encryption causing extra memory accesses from counters exacerbates the performance on DL accelerators, which even delivers worse performance than direct encryption.

To address these problems, our paper proposes SEAL, a Secure and Efficient Accelerator scheme for deep Learning to enhance the security of DL accelerators on edge devices while delivering a high performance. SEAL reduces the performance overhead of encryption by using a criticality-aware smart encryption (SE) scheme and a colocation mode encryption (ColoE) scheme. Specifically, to improve the data access bandwidth of DL accelerators, SEAL leverages the SE scheme to identify partial data having no impact on the security of NN models and allow them to bypass the encryption engine, lowering the amount of data to be encrypted without affecting security. To improve the efficiency of memory encryption, SEAL leverages the ColoE scheme that co-locates the storage of each data and its counter. ColoE has the same security level as the traditional counter mode encryption while achieving higher performance in DL accelerators due to removing extra memory accesses from counters. In summary, this paper makes the following contributions:

- **Observations and Insights on Securing DL Accelerators.** We present the new security problem of DL accelerators on edge devices, i.e., being vulnerable to physical access based attacks. We observe that memory encryption that has been efficiently used in CPU systems causes significant (up to 50%) performance degradation when being directly used in DL accelerators. By analyzing experimental results, we present the insights that the big bandwidth gap between the GDDR bus and the encryption engine is the main reason of causing performance degradation.

- **Criticality-aware Smart Encryption for NN Models.** We propose a criticality-aware smart encryption (SE) scheme to allow partial data to bypass the encryption engine for improving the data access bandwidth in DL accelerators without any loss of security. The idea of the SE scheme is to measure the relative importance of weight parameters in the NN model. Based on the relative importance, the SE scheme does not encrypt these weight parameters with the lowest importance, and thus it is unnecessary to encrypt their corresponding channels in the input or output feature maps. Based on the quantitative security evaluation in terms of both IP protection and adversarial attacks [17, 18, 37, 55], we determine the percentage of encrypted data with which the SE scheme achieves the same security level as the full encryption scheme.

- **Colocation Mode Encryption for DL Accelerators.** In order to improve the efficiency of memory encryption, we propose a colocation mode encryption (ColoE) scheme to store the data and its counter in the same memory line, unlike the traditional counter mode encryption storing them separately. Thus the ColoE scheme removes extra memory accesses from counters to improve the system performance and does not need a large on-chip counter cache compared with the traditional counter mode encryption. Due to the usage of counters for encryption, the ColoE scheme also has higher security level than traditional direct encryption.

- **Implementation and Evaluation.** We have implemented SEAL in GPGPU-Sim [5] and evaluated it using three classical CNN models including VGG-16 [67], ResNet-18 [25], and ResNet-34 [25]. Experimental results show that, compared with traditional direct and counter mode encryption, SEAL achieves $1.4 \times -1.6 \times$ IPC improvement and 39% – 60% of latency reduction. Compared with a baseline accelerator without memory encryption, SEAL is able to improve the security with a slight overhead (5% – 7% IPC).

2. BACKGROUND AND MOTIVATION

2.1 Deep Learning Accelerators

Deep learning (DL) [38] is widely used in current artificial intelligence applications, such as natural language processing, speech recognition, and computer vision. Achieving high accuracy and low processing latency in these applications requires complicated deep learning computation [25, 67]. Therefore, various DL hardware accelerators [9, 10, 11, 33, 51] are used to deliver high performance.

GPU is the most widely used DL accelerator due to compatibility with different algorithms and high parallelism. The powerful parallel processing ability of GPU is efficient and suitable for DL with a large amount of parallel floating-point and matrix/vector multiplication computation. FPGA is an alternative for implementing DL accelerators with energy efficiency. Furthermore, various ASIC DL accelerators are proposed to speed up special machine learning algorithms, such as TPU [33], DianNao family [9, 11], and Eyeriss [10].
A generic hardware architecture for these GPU, FPGA, and ASIC DL accelerators is shown in Figure 1. The accelerator architecture consists of an array of processing elements (PEs, or called cores in GPUs) and a data cache (or called global buffer) on chip. Each PE has its own control logic and scratchpad, and communicates with the data cache through network-on-chips (NoCs). As the size of the on-chip data cache is limited, the entire NN model and the intermediate data produced during DL inference are stored in the off-chip DRAM memory with large capacity. The accelerator accesses the DRAM through the high-bandwidth GDDR bus.

### 2.2 Threat Model and Purposes

For DL applications, neural network (NN) models are critical data maintained in DL accelerators [29, 30]. However, DL accelerators deployed on edge devices have the risk of leaking their NN models due to being vulnerable to physical access based attacks. Compared with devices deployed in the cloud, edge devices are easier to be physically accessed. For example, a user can dismantle his/her own self-driving car to look into the internal computer system. Therefore, DL accelerators on edge devices have the security vulnerability to physical access based attacks, i.e., bus snooping [65, 77].

**Threat Model:** Like existing threat models for hardware attacks on CPUs [65, 77] and accelerators [29, 30], we consider on-chip components of accelerators and DRAM are secure. However, an adversary can insert a bus snooper or a memory scanner on the GDDR memory bus\(^2\) to obtain the data communicated between the accelerator chip and off-chip DRAM [29, 30], and further steals the entire NN model.

**Threat Purposes:** We consider two threat purposes that an adversary obtains NN models via bus snooping.

1) **IP Stealing.** NN models are considered as the Intellectual Property (IP) of model owners [30, 60, 72]. Model owners may consume a large amount of financial and material resources to train a sophisticated NN model. The adversary may be a business competitor of model owners. The leakage of NN models incurs the property loss of model owners and reduces their competitive advantages.

2) **Adversarial Attacks.** The exposition of an NN model can significantly increase the risk that the NN model is attacked by adversarial attacks. In adversarial attacks, an adversary aims to apply an imperceptible non-random perturbation on the input data to change the prediction results of NN models [18, 69]. The perturbed input data are termed as adversarial examples. If the adversary does not know the NN model, the adversarial attack is called black-box attack. If the adversary knows the entire NN model, the adversarial attack is called white-box attack. In the black-box attacks, the attack success rate is low. In the white-box attacks, the attack success rate significantly increases since the adversary can generate high-quality adversarial examples by using the known model information [44, 53].

In order to protect the NN models in DL accelerators from bus snooping attacks, encrypting the data transmitted through the GDDR bus is important. Existing memory encryption techniques [65, 77] are widely used in secure CPU systems to enable secure data transmission through the DDR bus of CPU memory. However, data security on the GDDR memory bus for DL accelerators are rarely touched by existing work. In this following, we first present memory encryption techniques for secure CPUs (§2.3) and then investigate whether the straightforward solutions that perform CPU memory encryption directly on DL accelerators are efficient (§2.4).

### 2.3 Memory Encryption

In secure CPUs, the encryption engine of a block cipher algorithm (e.g., AES [13]) is added in the memory controller for encrypting and decrypting data. In general, there are two memory encryption models used for secure CPUs, including direct encryption and counter mode encryption.

As shown in Figure 2a, in the direct encryption, each cache line is encrypted by the AES encryption engine before being written back to the DRAM memory. After being read from the DRAM memory, each line is decrypted and then put into the last level cache. However, direct encryption causes high decryption latency in the critical path of memory accesses in CPUs. Additionally, direct encryption encrypts all memory lines by using the same global key, which has a low security level. Since the same data are always encrypted to the same ciphertext, it leaves direct encryption vulnerable to dictionary and retry based attacks [3, 79].

As shown in Figure 2b, in counter mode encryption [41], a global key, the line address and the per-line counter pass through the AES encryption engine to generate a one-time pad (OTP). The plaintext or ciphertext is then encrypted or decrypted by simply XORing its OTP. Each memory line in the off-chip DRAM has a counter. All counters are stored in the DRAM. Recently used counters are buffered in an on-chip counter cache managed by the memory controller. If the counter of a memory line to be read is in the counter cache, its decryption latency is hidden in the memory read latency, since the OTP is generated in parallel with the memory read. Only the XOR latency is added to the critical path, thus reducing their competitive advantages.

\(^2\)As we aim to protect the confidentiality of NN models, bus tampering attacks are not considered in our threat model that can be defended via Merkle Trees based authentication techniques [68], which are orthogonal to our work.

---

**Figure 1:** The generic DL accelerator architecture.

**Figure 2:** Encryption and decryption operations in the direct encryption and counter mode encryption.
Without loss of generality, in the rest of this paper, we analyze memory encryption solutions. (“Baseline” means a baseline GPU without using memory encryption. “Direct” means the direct encryption. “Cir-96” means the counter mode encryption with the 96KB counter cache and each memory controller has a 16KB (=96KB/6) counter cache.)

Moreover, counter mode encryption provides a higher security level than direct encryption, since OTPs are never reused for data encryption which keep counter mode encryption secure from dictionary and retry based attacks. First, since the line address is used to generate the OTP, the data stored at different addresses are encrypted by different OTPs. Second, a per-line counter is used to generate the OTP and the counter increases one on each write. Data rewritten in the same address are encrypted by different OTPs. In general, counters are stored in the plaintext since data cannot be decrypted if an adversary has the knowledge of the counter value but does not know the key [41,79].

### 2.4 Straightforward Solutions for Securing DL Accelerators

We consider two straightforward solutions, i.e., simply employing the direct encryption and counter mode encryption in DL accelerators, to improve the security of NN models. Without loss of generality, in the rest of this paper, we analyze GPU as a representative example of DL accelerators. However, the problems, insights, and solutions that we develop are also applicable to other DL accelerators.

We implement the two straightforward solutions in GPGPU-Sim [5]. Since the encryption engine increases the chip area and energy overhead that also affects the chip cooling [4, 45, 54], each memory controller generally includes one encryption engine [3, 43, 77, 79]. Thus the six memory controllers in the modeled GPU include six encryption engines. For the counter mode encryption, we add an on-chip counter cache to buffer recently used counters. The detailed GPU configurations are shown in Section 4.1. We use the modeled GPU to execute matrix multiplication computation that is the most common operation in DL algorithms. We evaluate the IPC (instruction per cycle) of the GPU with different encryption schemes and compare them with a baseline GPU without using memory encryption, as shown in Figure 3a.

First, we observe the GPU with memory encryption is significantly less efficient than the GPU without memory encryption. Memory encryption decreases the GPU IPC by 45% – 54% for the matrix multiplication computation. Second, using the counter mode encryption scheme does not deliver higher performance compared to using the direct encryption scheme on GPU. With the small counter cache sizes, i.e., 24KB, 96KB, and 384KB, the performance of the counter mode encryption scheme is even lower than the direct encryption scheme. By using a large counter cache, i.e., 1536KB, the IPC of the GPU is improved by 15%. However, the counter cache size is double of the L2 cache size in the modeled GPU as shown in the configurations (Section 4.1), which is too large to be deployed on the GPU die.

The reason that memory encryption significantly reduces the GPU performance is the big bandwidth gap between the GDDR memory bus and the encryption engine, as shown in Table 1. In CPU systems, memory encryption works well [65, 77] since the AES encryption engine has a similar bandwidth to the DDR memory bus and the PCIe bus of CPU. However, in GPU systems, the GPU performance is highly bandwidth-bounded and hence the GDDR memory is designed for GPUs to achieve high memory access bandwidth. The bandwidth of the GDDR memory bus is generally more than 160GB/s [49, 50, 51, 52]. However, the state-of-the-art pipelined AES encryption engine with hardware implementation achieves only about 8GB/s of bandwidth on average [45].

Even though we deploy one encryption engine in every memory controller, the total encryption bandwidth is 48 GB/s. As a result, the high bandwidth of the GDDR memory bus is under-utilized and the AES encryption engine becomes the bandwidth bottleneck in secure GPUs. A single AES engine usually occupies over 1 mm² on-die area and has hundreds or thousands of mW power, as shown in Table 2. As resources on the microprocessor die are very scarce, it is ruinously costly to integrate more encryption engines into memory controllers on the GPU die [21]. Even though a GPU/CPU die usually has an area of 90 – 600 mm², most area is occupied by cores and on-die memory and only less than 10% area is left to memory controllers [34, 59]. This is also the reason why Intel carefully designs the AES hardware implementation to reduce area and energy overheads for Software Guard Extensions (SGX) [21]. Like the design principle of Intel’s SGX [21] and many previous works [3, 43, 77, 79], the goal of this paper is also to improve the hardware security while having low on-die overheads. Moreover, since the data access bandwidth is the performance bottleneck, the counter mode encryption incurs extra memory access requests for reading and writing counters compared with the direct encryption, thus delivering low performance with small cache sizes.

### 3. THE SEAL DESIGN

We propose SEAL, a secure and efficient DL accelerator scheme to enhance the security of NN models. SEAL improves the performance of secure DL accelerators by exploring and exploiting software and hardware co-design. In the software layer, to improve the data access bandwidth of DL accelerators, a criticality-aware smart encryption (SE)
scheme (§3.1) is used to measure the relative importance of weight parameters in the NN model. Only the relatively important weight parameters are processed by the AES encryption engine and the remaining parameters bypass the AES encryption engine, which reduces the amount of data to be encrypted without compromising the security. We quantitatively analyze and evaluate the security of the SE scheme in terms of both IP protection and adversarial attacks, and leverage the evaluation results to guide the parameter configuration of the SE scheme to obtain the maximum performance benefit and the highest security level (§3.4).

In the hardware layer, to improve the efficiency of memory encryption, SEAL leverages a colocation mode encryption (ColoE) scheme (§3.2) to achieve the same security level as the counter mode encryption while eliminating extra memory accesses from counters. Moreover, we present the overall hardware architecture design to support SE and ColoE (§3.3).

3.1 Criticality-aware Smart Encryption

In this subsection, we first use the convolutional neural network (CNN) that is a widely used neural network for DL as an example to present the challenges of performing partial encryption on DL accelerators. We then present the proposed criticality-aware smart encryption scheme.

3.1.1 Challenges for Partial Encryption

During the process of the CNN inference, there are four kinds of data, i.e., data in the input layer, data in the output layer, weight parameters in hidden layers (i.e., the NN model data), and intermediate data (i.e., feature maps) produced by hidden layers, as shown in Figure 4. If we encrypt all the data during the CNN inference, the inference performance significantly decreases, as presented in Section 2.4. This is mainly because the bandwidth of the AES encryption engine is far lower than that of the GDDR memory bus, limiting the total data access bandwidth. If we can only encrypt partial data to reduce the amount of data to be encrypted, the total data access bandwidth improves. Nevertheless, performing partial encryption is not easy due to the following fundamental challenges.

Challenge 1: How to select appropriate data to be encrypted? Among the four kinds of data, the data in the input and output layers are usually known by the adversary. For example, for the DL accelerator in a self-driving car, the input data are the pictures of the current visual field taken by cameras, which can be obtained by the adversary. The output data are the current actions of the car, e.g., stop, turning left, or turning right, also known by the adversary. A simple way of the partial encryption is that we do not encrypt the data in the input and output layers and encrypt the remaining data including weight parameters in the NN model and intermediate data produced by hidden layers. However, the sizes of the data in the input and output layers are far smaller than that of the intermediate data, as shown in Figure 4. For example, the data in the input layer with the size of 224 × 224 × 3 are 11 times smaller than the output feature maps of the first CONV layer with the size of 224 × 224 × 64. Therefore, this simple way is inefficient to improve inference performance.

Moreover, among these data in the CNN inference, weight parameters of the NN model have to be protected. Intuitively, we can encrypt only the weight parameters of the NN model and do not encrypt the remainder of the data to reduce the encryption overhead. However, an adversary can calculate or speculate the weight parameters of the NN model via unencrypted feature maps. For example, a CONV layer computes the input feature maps $X$ with a kernel matrix $\omega$ to produce the output feature maps $Y$, i.e., $Y = X\omega$. If $X$ and $Y$ are not encrypted, an adversary can easily compute the kernel matrix $\omega$ via the equation $\omega = X^{-1}Y$ in which $X^{-1}$ is the inverse matrix of $X$. Therefore, it is important to protect the NN model data from being calculated or speculated from the unencrypted data.

Challenge 2: How to evaluate the impact of partial encryption on security? Intuitively, encrypting all data inputted and produced during the NN inference has a high security level but causes significant performance degradation. Selectively un-encrypting partial data can improve the performance which however may exacerbate security. An adversary can directly compute encrypted weights via unencrypted feature maps as discussed above. Moreover, existing fine-tuning techniques [39, 58] for NN models can also be used to speculate a complete NN model based on known partial weight parameters and the data in the input and output layers. Specifically, the adversary can fill the known partial weight parameters in the NN model and then use the data in the input and output layers to retain a complete NN model. Hence, how to evaluate and quantify the impact of partial encryption on security...
is non-trivial for designing an efficient encryption scheme.

3.1.2 Smart Encryption in SEAL

To address these challenges, we propose a criticality-aware smart encryption (SE) scheme in SEAL, which aims to reduce the amount of encrypted data while improving the NN model security. The SE scheme quantitatively measures the relative importance of weight parameters in each layer by calculating the sum of their absolute weights, i.e., $\ell_1$-norm. The weight parameters with the smallest absolute values in each layer are considered to be least important and hence are not encrypted. Thus it is unnecessary to encrypt the corresponding channels in the input or output feature maps of unencrypted weight parameters. As a result, the amount of data to be encrypted is significantly reduced. The percentage of un-encrypted weight parameters is determined based on the quantitative security evaluation in Section 3.4 to obtain maximum performance benefit and highest security level.

In deep neural networks, we consider use the SE scheme in the CONV layers since most layers in a CNN model are CONV layers, e.g., 13/16 for VGG-16, 17/18 for ResNet-18, and 33/34 for ResNet-34. The computation process of a CONV layer is shown in Figure 5. Weight parameters in a CONV layer are organized as a convolutional kernel matrix, and each convolutional kernel is a weight matrix, e.g., $3 \times 3$. The computation of a CONV layer transforms the input feature maps with the convolutional kernel matrix to the output feature maps. The convolutional kernel matrix has $n_x$ kernel rows and $n_y$ kernel columns. $n_x$ is equal to the number of channels in the input feature maps. Each kernel row in the kernel matrix corresponds to a single input channel in the input feature maps and this input channel does not involve the convolution computation with other kernel rows, as shown in Figure 5. Similarly, $n_y$ is equal to the number of channels in the output feature maps. Each kernel column in the kernel matrix corresponds to a single output channel in the output feature maps, as shown in Figure 5.

Relative Importance Measurement. We first present our approach for relative importance measurement as shown in Figure 5. We measure the relative importance of a kernel row in each layer by calculating the sum of its absolute weights, i.e., $\ell_1$-norm. The sum of absolute weights in a row also represents the average magnitude of the kernel weights which gives an expectation of the magnitude of the output feature map. Thus kernel rows with smaller sums of absolute weights tend to produce feature maps with weak activations, compared with the other kernel rows in the same layer [39]. Hence, these rows with small absolute-value sums have a lower impact on the output of the entire NN model compared with the rows with large absolute-value sums. Existing work [23, 39] on pruning NN models demonstrate that, even after completely eliminating the convolution computation that uses these weight parameters with small absolute values, the original accuracy of the NN model can be regained by retraining the networks. This observation indicates that these weight parameters with small absolute values are less important to the NN model and thus rarely affect the security of the NN model.

We have confirmed this conjecture by performing IP protection and adversarial attack tests as presented in Section 3.4, whose results motivate us to propose the smart encryption (SE) scheme to reduce the encryption overhead in DL accelerators by only encrypting the weight parameters with large absolute values.

Smart Encryption (SE). After computing the sum of absolute weights in each row, the SE scheme sorts the kernel rows based on their sums. The SE scheme then encrypts partial kernel rows with the largest sums. The percentage of the encrypted kernel rows is determined by our quantitative security analysis as shown in Section 3.4. However, the encrypted weight parameters in the SE scheme can be figured out if the input and output feature maps of this CONV layer are unencrypted as discussed in Section 3.1.1. Therefore, for each encrypted row, the SE scheme also encrypts one input channel in the input feature maps corresponding to the encrypted row, since each kernel row corresponds to a single input channel and does not involve the convolution computation with other input channels, as shown in Figure 5. In this way, the encrypted weight parameters cannot be figured out. For example, for the matrix multiplication $Y = X\omega$, the input channel $X$ and the weights $\omega$ are encrypted. $\omega$ cannot be figured out even though the adversary knows $Y$. The data in the input channel $X$ is encrypted once being produced by the previous CONV layer. Hence, the plaintext in the encrypted channel $X$ is never exposed to the memory bus.

Moreover, when considering unencrypted data among multiple layers, the encrypted channels and weights cannot be figured out and hence also secure. To prove this, we use a simple example with two sequential CONV layers, i.e., $Y = X\omega$ and $Z = Y\omega'$, as follows,

$$X = \begin{bmatrix} X_0 & X_1 \end{bmatrix}, \omega = \begin{bmatrix} \omega_{00} & \omega_{01} \\ \omega_{00} & \omega_{01} \end{bmatrix}, Y = \begin{bmatrix} Y_0 & Y_1 \end{bmatrix},$$

$$\omega' = \begin{bmatrix} \omega'_{00} \omega'_{01} \\ \omega'_{00} \omega'_{01} \end{bmatrix}, Z = \begin{bmatrix} Z_0 & Z_1 \end{bmatrix}. \tag{1}$$

The feature maps $X$, $Y$, and $Z$ have 2 channels. Since there are 2 input and output channels, the kernel matrices $\omega$ and $\omega'$ have 2 rows and 2 columns. With a 50% encryption ratio, we assume the first row $\omega_{00}$ in $\omega$ is encrypted, and the second row $\omega'_{01}$ in $\omega'$ is encrypted. Based on the SE scheme, we should encrypt the first channel $X_0$ in $X$ and the second channel $Y_1$ in $Y$. Moreover, we assume $Z_0$ is encrypted in $Z$. In Equation 1, the bold fonts mean encrypted data. Thus for the two sequential CONV layers, we can have the following equations (the encrypted data are in bold):

$$\begin{cases} X_0 \ast \omega_{00} + X_1 \ast \omega_{01} = Y_0 \\ \frac{X_0}{X_1} \ast \omega_{01} = Y_1 \end{cases} \tag{2}$$

$$\begin{cases} Y_0 \ast \omega'_{00} + Y_1 \ast \omega'_{01} = Z_0 \\ \frac{Y_0}{Y_1} \ast \omega'_{01} = Z_1 \end{cases} \tag{3}$$

As shown in Equations 2 and 3, encrypted input channels are never multiplied with unencrypted weight rows, and unencrypted input channels are never multiplied with encrypted.
weight rows. Thus we can only obtain the product of two encrypted matrices, e.g., \( X_0 \times W_0 \), but cannot figure out any single encrypted matrix from Equations 2 and 3. Therefore, the data in encrypted channels and weights are secure even considering data among multiple layers.

In fact, the SE scheme can also be applied to FC layers since each FC layer includes a kernel matrix like the CONV layer. Therefore, the proposed SE scheme can be applied to other deep neural networks, e.g., recurrent neural networks [12, 28], that are composed of many FC layers.

### 3.2 Colocation Mode Encryption

There are two existing memory encryption models, i.e., direct encryption and counter mode encryption, as discussed in Section 2.3. Direct encryption has a lower security level due to being vulnerable to the directory and retry based attacks. Counter mode encryption enhances security by using counters for encryption but requires a large counter cache on chip to achieve a high cache hit rate. Based on previous works [3, 43, 77] on counter mode encryption, the size of the used counter cache is usually up to 1MB−4MB. It is reasonable to add a large counter cache on CPU chips, since a large part of the area on CPU chips is occupied by memories, e.g., last level cache, and thus it is easy to partition some memories for the counter cache. However, for DL accelerators, especially GPUs, a large part of the on-chip area is used for computing units. The L2 cache for current commercial GPUs [2, 50, 51] is usually no more than several MB. Therefore, adding a large counter cache on GPU chips is impractical.

Our paper proposes a colocation mode encryption (ColoE) scheme for DL accelerators without using an on-chip counter cache. The ColoE scheme achieves the same security level while having higher performance on DL accelerators, compared with the traditional counter mode encryption. Unlike the traditional counter mode encryption that stores the data and their counters separately as shown in Figure 6a, the ColoE scheme stores the data and its counter together, i.e., colocation. Like Intel’s SGX [21, 22], we use the monolithic counter scheme rather than the split counter scheme [77] to avoid the overheads of intricate page re-encryption. The counter area is 8B for each memory line. Thus a memory line for storing the encrypted data is 136B including 128B data and 8B counter area as shown in Figure 6b. When the data is evicted from the L2 cache, the ColoE scheme encrypts the data using its co-located counter, its memory address, and a key and then writes it into the DRAM memory. When the data is read from the DRAM memory, the ColoE scheme decrypts the data and then sends it to the L2 cache. Unlike the traditional counter mode encryption that needs extra memory accesses to read/write counters, the ColoE scheme avoids these memory requests from counters by co-locating the data and their counters, thus improving the encryption performance in GPUs.

### 3.3 Implementation and Overall Architecture

To support the proposed SE and ColoE schemes, SEAL is implemented via exploring and exploiting software and hardware co-design. The implementation and overall architecture of SEAL are shown in Figure 7.

To support the SE scheme, in the software layer, we expose a new programming primitive, emalloc(), to the high-level program in order to allow programmers to leverage the benefits of the smart encryption. The memory space allocated by emalloc() needs to be encrypted. The memory space allocated by existing malloc() in current programming languages does not need to be encrypted. In the hardware layer, the counter area is 64 bits while the counter used in the counter mode encryption only needs 56 bits, like the implementation in Intel’s SGX [21, 22]. Thus 8 bits in the counter area are not used. We use one bit in the counter area of each memory line as a flag to indicate whether the memory line is allocated by emalloc() or malloc(). Hence, memory controllers can distinguish the memory lines allocated by emalloc() or malloc() based on the flags. Memory lines allocated by malloc() bypass the AES engine.

To support the ColoE scheme, referring to the design of error-correcting code (ECC) DRAM [8, 14], we design the DRAM DIMM to include an extra chip without changing the DRAM burst mechanism. As shown in Figure 7, in a DRAM rank, there are 16 data chips and 1 counter chip (in the ECC DRAM, the chip is used for storing ECC bits). For a memory line, 128B data is stored in the 16 data chips (8B per chip) and 8B counter area is stored in the counter chip.

### 3.4 Security Analysis

For the security analysis, we first discuss the case where an adversary does not know what NN architecture is used in the target DL accelerator. In this case, even though some NN model data are obtained by the bus snooping attack, the adversary is difficult to distinguish which data are used for a particular layer. In our proposed SE scheme, some data are encrypted and hence it is more difficult for the adversary to recover the NN model. Therefore, we consider a strong
attack model in which an adversary is able to figure out the NN architecture in the DL accelerator via side channel information [29,30,78], e.g., memory access patterns obtained from the memory bus, or device specifications [32]. In this case, the adversary can distinguish the data from different layers and know the locations in the NN model where the encrypted and unencrypted data correspond to. Under the strong attack model, we present the security analysis. The security of NN models involves two aspects including IP stealing and adversarial attacks, as presented in Section 2.2.

### 3.4.1 Substitute Model Generation

In the security evaluation tests, we use three classical CNN models including VGG-16 [67], ResNet-18 [25], and ResNet-34 [25] and train them on the widely used CIFAR-10 dataset [35]. The NN model stored in the target DL accelerator is called victim model, and the NN model that the adversary extracts from the accelerator by using bus-snooping attacks is called substitute model. Based on the fact that the adversary does not know the training dataset of the victim model, we isolate 90% of training samples (45,000 images) in CIFAR10 as the training dataset of the victim model [56]. The remaining 10% of training samples (5,000 images) are used by the adversary. Based on the 5,000 images, the adversary uses Jacobian-based dataset augmentation [56] to generate additional 40,000 images and then query them in the target accelerator to obtain their corresponding labels. The generated image-label pairs are used as the training dataset of the adversary’s substitute models. There are three kinds of substitute models that the adversary may obtain as follows.

- **White-box model.** If a DL accelerator does not equip memory encryption, the adversary can know the entire victim model including all weight parameters and the NN architecture. Thus we consider an NN model that is the same as the victim model as the white-box substitute model.

- **Black-box model.** If we encrypt all the victim model data and intermediate data, the adversary knows the NN architecture but does not know any weight parameters. However, the adversary can feed his/her own images into the target DL accelerator and obtain the output label. By using the image-label pairs, the adversary is able to retrain an NN model with the same architecture as the victim model. We consider the retrained NN model as the black-box substitute model.

- **Smart encryption (SE) model.** In the SEAL, we selectively encrypt partial data that are critical and thus the adversary knows the NN architecture and partial weight parameters that are unencrypted. We perform full encryption on the first two CONV layers, the last one CONV layer, and the last FC layers of a CNN model to prevent the adversary from calculating the weight parameters via input and output layers, and perform the SE scheme on the remaining weight layers.

### 3.4.2 Security on IP Stealing

One of the attack purposes is to steal the IP of NN models. The adversary that may be a business competitor aims to reduce the competitive advantages of model owners. The efficiency of the stolen attacks depends on the inference accuracy of the extracted substitute models. In the stolen attack tests, we first generate the three kinds of substitute models including white-box, black-box, and SE models that the adversary may obtain as mentioned above. For the SE models, we vary the encryption ratio from 90% to 10%. The encryption ratio is defined as the ratio of encrypted weight parameters to all weight parameters in each layer. The encrypted weights have the largest absolute weight values in each layer as presented in Section 3.1.2. We evaluate the inference accuracy of these substitute models using test samples of the victim model.

Figure 8 shows their inference accuracy. We observe that the white-box model has a very high accuracy, i.e., about 94%, due to being the same as the victim model. The black-box model significantly reduces the accuracy from 94% to 75%. This is because the adversary does not know any weights and training samples in the victim model, and the black-box model can only be trained from a blank model by retraining the NN using inputs and outputs of the target DL accelerator. However, by using inputs and outputs of the target DL accelerator, the adversary is able to supplement the unknown part of weight parameters via retraining the NN. Specifically, the adversary initializes an NN model with known weight parameters and fills random numbers following a standard normal distribution for unknown weight parameters [24]. The adversary then keeps the known weight parameters unchanged and fine-tunes unknown weight parameters by retraining the NN using inputs and outputs of the target DL accelerator. Note that the attacker can know the information that the sums of unknown weight rows must be larger than those of known weight rows and then leverage this information during fine-tuning. However, in our experiments, we observe the generated substitute models leveraging the information do not perform better, since limiting the sums of unknown weight rows may destroy efficient parameter fine-tuning.
3.4.3 Security on Adversarial Attacks

If the purpose is to attack the victim model, the adversary can use the extracted NN models to generate adversarial examples and then use the adversarial examples to perform adversarial attacks. In the adversarial attack tests, we use the three kinds of substitute models including white-box, black-box, and SE models to respectively generate 1,000 adversarial examples via the I-FGSM method [37]. Each batch of 1,000 adversarial examples have a 100% attack success rate to attack their corresponding substitute models. We then use these adversarial examples to attack the victim model and evaluate the transferability of adversarial examples. The transferability is defined as the ratio of the adversarial examples that successfully attack the victim model to all adversarial examples, which is a widely used metric to evaluate the efficiency of substitute models for adversarial attacks [17, 44, 71, 80]. Figure 9 shows the transferability of the adversarial examples generated by different substitute models.

We observe that black-box models have much lower transferability (about 20%) for the three CNN models compared with white-box models, since the adversary with black-box models does not have any weight parameters and training samples of the victim model. For the SE models, when the encryption ratios $\geq 50\%$ for the three CNN models, the transferability is close to, and even smaller than those of black-box models. The reason is that the unencrypted weight parameters in the SE scheme are relatively unimportant because they have the smallest absolute weights in each layer. If the adversary keeps the unencrypted weight parameters unchanged and fine-tunes the remaining weight parameters, the unchanged, unimportant weight parameters may disturb the retrained model, thus producing smaller attack success rates than the black-box model. When the encryption ratios $< 40\%$, the transferability rapidly increases since some important weight parameters with large absolutes are exposed to the adversary. Based on the above results, we set the encryption ratio of the SE scheme to 50%, which obtains the maximum performance benefit when achieving the same security level as the black-box models.

## 4. PERFORMANCE EVALUATION

### 4.1 Methodology

We evaluate the performance of SEAL using the GPGPU-Sim v3.2.2 [5], a cycle-level simulator for contemporary GPUs. We model the microarchitecture for NVIDIA GeForce GTX480 GPU [49] with 15 streaming multiprocessors (SMs), one of the default GPUs in GPGPU-Sim. The details of our used GPU configuration are shown in Table 3. Although we perform our simulations on an Nvidia Fermi GPU, our solution focusing on the accelerator memory system is also applicable and generalizable to newer GPU architectures including Maxwell, Pascal, and Volta, as well as other kinds of DL accelerators as presented in Section 2.4. To implement SEAL, we add an AES encryption engine in every memory controller of the simulated GPU. We model a pipeline AES encryption engine with 128-bit block [4, 45, 54], in which the overall AES encryption latency for a cache line is 20 cycles and the bandwidth of an AES engine is 8GB/s. According to bandwidth values summarized in Tables 1 and 2, we set a mean bandwidth value for AES and GPU.

### 4.2 Performance of Different Layers

#### 4.2.1 IPC of Different-layer Computation

We perform the SE scheme on CONV layers whose input and output feature maps are also the input and output of POOL layers. Different encryption schemes have different impacts on the performance of CONV and POOL layers. The default encryption ratio is 50% for the SE scheme as presented in Section 3.4. To investigate the impact of different encryption schemes on the performance of different layers, we evaluate four typical CONV layers in VGG, in which the number of input and output channels is 64, 128, 256, and 512, respectively. We also evaluate the five different POOL layers.

Figure 10 shows the relative IPCs of different encryption schemes when computing these CONV layers. We
observe that the Direct scheme and the Counter scheme reduce the GPU IPC by up to 40% compared with the baseline GPU without memory encryption. The reason is that memory encryption significantly reduces the data access bandwidth in GPUs as discussed in Section 2.4. By comparing the performance between the Direct/Counter and the Direct+SE/Counter+SE schemes, our proposed SE scheme significantly improves the memory encryption performance on GPUs by reducing the amount of the encrypted data to improve the data access bandwidth without compromising security. The Direct+SE scheme has higher IPC performance than the Counter+SE scheme, since the counter mode encryption causes extra memory accesses from counters. However, the direct encryption has a lower security level than the counter mode encryption. SEAL leverages a ColoE scheme to achieve the same security level as counter mode encryption while delivering higher performance. Compared with the Counter+SE scheme, we observe that SEAL improves the IPC by up to 12% by using the ColoE scheme.

Figure 11 shows the relative IPCs of different encryption schemes when computing POOL layers. We observe the Direct and Counter schemes reduce the IPC by up to 50%, and perform worse in comparison to computing CONV layers even though the computation of POOL layers is more bandwidth-bound than that of CONV layers. Due to the same reason, the Direct+SE, Counter+SE, and SEAL perform worse when compared to computing CONV layers. Nevertheless, for the entire neural network, the amount of computation overhead in CONV layers is much larger than that in POOL layers.

4.2.2 Performance under Different Encr. Ratios

We investigate the impact of different encryption ratios on the performance of SEAL when computing a CONV/POOL layer. We vary the encryption ratio from 100% to 0% with the 10% interval. A 100% encryption ratio means a full-encryption GPU. When the encryption ratio is 0%, the performance is the same as that of a baseline GPU without memory encryption. The experimental results are shown in Figure 12. When slightly reducing the encryption ratio by 20% – 30% from a 100% encryption ratio, the IPC is significantly improved. The reason is that allowing partial data to bypass

4.3 Overall Performance

4.3.1 IPC

We evaluate the IPC of the GPU with different encryption schemes when executing the NN inference using VGG-16, ResNet-18, and ResNet-34, as shown in Figure 13. Traditional memory encryption solutions including the Direct and Counter schemes reduce the GPU IPC for executing NN inference by 30% – 38%, compared with a baseline GPU. Moreover, the Direct and Counter schemes deliver higher performance in ResNets than those in VGG. The reason is that the amounts of computation and data accesses to memory in VGG are much larger than those in ResNets [25] and thus VGG requires higher data access bandwidth. Memory encryption limits the data access bandwidth and hence has more significant impact on the performance of VGG. By using our proposed SE scheme to allow some data to bypass the AES encryption engine, the Direct+SE and Counter+SE schemes improve the IPC by about 31% and 20% respectively, compared with the Direct and Counter schemes. By using our proposed ColoE scheme to eliminate memory accesses of counters, SEAL further improves the IPC by about 7% compared with the Counter+SE scheme. As a result, compared with the traditional memory encryption solutions, i.e., the Direct and Counter schemes, SEAL achieves $1.4 \times -1.6 \times$ IPC improvement. Moreover, SEAL achieves the 93% – 95% IPC of a baseline GPU without memory encryption, i.e., compromising only 5% – 7% performance for security improvement.

4.3.2 The Number of Memory Accesses

We evaluate the number of different kinds of memory accesses when using different encryption schemes, as shown in Figure 14. For the baseline GPU, all memory accesses including reads and writes come from unencrypted data. For
the Direct scheme, all memory accesses are from encrypted data and thus need to pass through the low-bandwidth AES encryption engine. Therefore, the Direct scheme significantly reduces the GPU performance compared with the Baseline as shown in Figure 13. For the Counter scheme, all memory accesses from data are also from encrypted data. Moreover, the Counter scheme incurs 31% – 35% more memory accesses from counters and thus has lower performance than the Direct scheme. Nevertheless, in the Direct and Counter schemes, the main performance bottleneck is the AES encryption engine rather than the DRAM. Hence, extra memory accesses from counters in Counter scheme do not incur much performance decrease, compared with the Direct scheme.

By using the SE scheme, the number of memory accesses from encrypted data is reduced by 39% – 45%. Therefore, the IPCs of Direct+SE and Counter+SE schemes are significantly improved compared with the Direct and Counter schemes, as shown in Figure 13. Moreover, the Counter+SE scheme incurs about 20% more memory accesses from counters and thus has lower performance than the Direct+SE scheme. Nevertheless, in the Direct+SE and Counter+SE schemes, the AES encryption engine may not be the main performance bottleneck due to using the SE scheme. Therefore, extra 20% memory accesses from counters in Counter scheme incur much performance decrease, compared with the Direct scheme. SEAL leverages the ColoE scheme to achieve the same security level as counter mode encryption while eliminating the extra memory accesses from counters. Therefore, compared with the Direct+SE scheme, SEAL achieves higher security level and the approximate performance. Compared with the Counter+SE scheme, SEAL achieves higher performance and the same security level.

4.3.3 Inference Latency

We investigate the impact of different encryption schemes on the inference latency, as shown in Figure 15. Traditional memory encryption solutions including the Direct and Counter schemes increase the inference latency by 39% – 60%, compared to a baseline GPU. By using the proposed SE scheme, the Direct+SE and Counter+SE schemes reduce the extra inference latency to 5% – 18%. By using both the SE and ColoE schemes, SEAL incurs only 5% – 7% higher inference latency than the baseline GPU.

5. RELATED WORK

Model Extraction Attacks. 1) Algorithm layer. There exist algorithm-layer approaches to extract the NN model related information by exploiting the inputs and outputs of the NN model architecture. Wang et al. [74] propose an approach to extract the hyperparameters of the NN model. The hyperparameters are usually used to balance between the regularization terms in the objective function and the loss function. 2) System and architecture layers. Existing works exploit the information of the operating system and architecture layers to speculate the NN model related information. Naghibjouybari et al. [47] exploit the side channel information in the operating system, such as memory allocation APIs, GPU performance counters, and timing measurement, to speculate the NN model related information, e.g., the number of neurons. Hua et al. [30] exploit the side channel information in the DL accelerator architecture, e.g., the memory access pattern, to speculate the NN architecture related information.

The model extraction attacks mentioned above can obtain only a small part of the NN model related information. Compared with these model extraction attacks, the bus snooping attacks for DL accelerators that our paper focuses on are much more dangerous. This is because an adversary can obtain all data of the entire NN model including weight parameters in each layer by the bus snooping attacks. Our paper proposes a secure and efficient solution, called SEAL, to defend against the bus snooping attacks for DL accelerators.

Memory Encryption. Obviously, software memory encryption, such as Graviton [73], cannot adequately defend against physical access based attacks [77], since the programs of encryption software themselves can be stored in the memory. Hardware memory encryption has been widely used in secure CPU systems [3, 27, 41, 61, 77, 79] to defend against physical access based attacks by adding the hardware encryption engine on the CPU chip. Memory encryption does not cause significant performance degradation in CPU systems, since the DDR memory bus for CPUs has a similar bandwidth to the encryption engine. However, memory encryption significantly decreases the performance of DL accelerators, e.g., GPUs, due to the big bandwidth gap between the GDDR memory bus and encryption engine. Our proposed SEAL is able to efficiently address this problem via criticality-aware smart encryption and colocation mode encryption.

6. CONCLUSION

Our paper proposes SEAL to enhance the security of NN models in DL accelerators on edge devices. To reduce performance overheads from memory encryption, SEAL leverages...
a criticism-aware smart encryption (SE) scheme and a colocation mode encryption (ColoE) scheme. The SE scheme is used to improve the data access bandwidth of DL accelerators by identifying partial data that have no impact on the security of NN models and allowing them to bypass the encryption engine without affecting the security of the NN model. The ColoE scheme is used to improve the efficiency of memory encryption by co-locating data and their counters to reduce the memory accesses from counters. Our experimental results show that, compared with traditional memory encryption solutions, SEAL achieves $1.4 \times -1.6 \times$ IPC improvement. Compared with a baseline accelerator without using memory encryption, SEAL improves the security with a slight overhead ($5\% - 7\%$ IPC).

REFERENCES

[1] S. Affeld, X. Zhu, and P. Burford, “Data poisoning attacks against autoregressive models,” in Proceedings of the Thirteenth AAAI Conference on Artificial Intelligence (AAAI), 2016.

[2] AMD Corporation, “White Paper: AMD Graphics Cores Next (GCN) Architecture,” https://www.amd.com/Documents/GCN_Architecture_whitepaper.pdf, 2012.

[3] A. Awad, P. Manadatha, S. Haber, Y. Solihin, and W. Horne, “Silent shredder: Zero-cost shredding for secure non-volatile main memory controllers,” in Proceedings of the 21st International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2016.

[4] A. Awad, Y. Wang, D. Shands, and Y. Solihin, “Obfuscemem: A low-overhead obfuscation for trusted memories,” in Proceedings of the 44th Annual International Symposium on Computer Architecture (ISCA), 2017.

[5] A. Bakhoda, G. L. Yuan, W. W. Fung, H. Wong, and T. M. Aamodt, “Analyzing CUDA workloads using a detailed GPU simulator,” in Proceedings of the 2009 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2009.

[6] N. Carlini, P. Mishra, T. Vaidya, Y. Zhang, M. Sherr, C. Shields, D. Wagner, and W. Zhou, “Hidden voice commands,” in Proceedings of the 25th USENIX Security Symposium (USENIX Security), 2016.

[7] Chanan Bos, “Teslaâ€”s new hw3 self-driving computer – itâ€”s a beast,” June 2019, https://cleantechnica.com/2019/06/15/tesla-new-hw3-self-driving-computer-its-a-beast-cleantechnica-deep-dives/.

[8] C.-L. Chen and M. Hsiang, “Error-correcting codes for semiconductor memory applications: A state-of-the-art review,” IBM Journal of Research and development, vol. 28, no. 2, pp. 124–134, 1984.

[9] T. Chen, Z. Du, N. Sun, J. Wang, C. Wu, Y. Chen, and O. Temam, “Dinanno: A small-footprint high-throughput accelerator for ubiquitous machine-learning,” in Proceedings of the 19th international conference on Architectural support for programming languages and operating systems (ASPLOS), 2014.

[10] Y.-H. Chen, T. Krishna, J. S. Emer, and V. Sze, “Eyeriss: An energy-efficient reconfigurable accelerator for deep convolutional neural networks,” IEEE Journal of Solid-State Circuits, vol. 52, no. 1, pp. 127–138, 2017.

[11] Y. Chen, T. Luo, S. Liu, S. Zhang, L. He, J. Wang, L. Li, T. Chen, Z. Xu, N. Sun et al., “Dadamno: A machine-learning supercomputer,” in Proceedings of the 47th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), 2014.

[12] K. Cho, B. Van Merriënboer, C. Gulcehre, D. Bahdanau, F. Bougares, H. Schwenk, and Y. Bengio, “Learning phrase representations using rnn encoder-decoder for statistical machine translation,” arXiv preprint arXiv:1406.1078, 2014.

[13] J. Daemen and V. Rijmen, The design of Rijndael: AES-the advanced encryption standard. Springer Science & Business Media, 2013.

[14] T. J. Dell, “A white paper on the benefits of chipkill-correct eec for pc server main memory,” IBM Microelectronics Division, vol. 11, pp. 1–23, 1997.

[15] Ensilica, “Advanced encryption standard cryptographic ip,” 2020, https://www.ensilica.com/ip/esi-crypto/aes/.

[16] K. Eykholt, I. Evtimov, E. Fernandes, B. Li, A. Rahmati, C. Xiao, A. Prakash, T. Kohno, and D. Song, “Robust physical-world attacks on deep learning visual classification,” in Proceedings of the Conference on Computer Vision and Pattern Recognition (CVPR), 2018.

[17] J. Goodfellow, P. McDaniel, and N. Papernot, “Making machine learning robust against adversarial inputs,” Communications of the ACM, vol. 61, no. 7, pp. 56–66, 2018.

[18] J. Goodfellow, J. Pouget-Abadie, M. Mirza, B. Xu, D. Warde-Farley, S. Ozair, A. Courville, and Y. Bengio, “Generative adversarial nets,” in Advances in neural information processing systems (NeurIPS), 2014.

[19] Google Corporation, “Edge TPU: Google’s purpose-built ASIC designed to run inference at the edge,” https://cloud.google.com/edge-tpu/, 2018.

[20] A. Graves, A. R. Mohamed, and G. Hinton, “Speech recognition with deep recurrent neural networks,” in Proceedings of the 2013 IEEE international conference on acoustics, speech and signal processing (ICASSP), 2013.

[21] S. Gueron, “A memory encryption engine suitable for general purpose processors,” Cryptology ePrint Archive, Report 2016/204, 2016, https://eprint.iacr.org/2016/204.

[22] S. Gueron, “Memory encryption for general-purpose processors,” IEEE Security & Privacy, vol. 14, no. 6, pp. 54–62, 2016.

[23] S. Han, H. Mao, and W. J. Dally, “Deep compression: Compressing deep neural networks with pruning, trained quantization and huffman coding,” in Proceedings of the International Conference on Learning Representations (ICLR), 2015.

[24] K. He, X. Zhang, S. Ren, and J. Sun, “Delving deep into rectifiers: Surpassing human-level performance on imagenet classification,” in Proceedings of the IEEE international conference on computer vision (ICCV), 2015.

[25] K. He, X. Zhang, S. Ren, and J. Sun, “Deep residual learning for image recognition,” in Proceedings of the IEEE conference on computer vision and pattern recognition (CVPR), 2016.

[26] J. L. Hennessy and D. A. Patterson, Computer architecture: A quantitative approach. Elsevier, 2011.

[27] M. Henson and S. Taylor, “Memory encryption: A survey of existing techniques,” ACM Computing Surveys (CSUR), vol. 46, no. 4, pp. 53–79, 2014.

[28] S. Hochreiter and J. Schmidhuber, “Long short-term memory,” Neural computation, vol. 9, no. 8, pp. 1735–1780, 1997.

[29] X. Hu, L. Liang, S. Li, L. Deng, P. Zuo, Y. Ji, X. Xie, Y. Ding, C. Liu, T. Sherwood, and Y. Xie, “Deepsniffer: a dnn model extraction framework based on learning architectural hints,” in Proceedings of the 25th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2020.

[30] W. Hua, Z. Zhang, and G. E. Suh, “Reverse engineering convolutional neural networks through side-channel information leaks,” in Proceedings of the 2018 55th ACM/IEEE Design Automation Conference (DAC), 2018.

[31] B. Hual, T. Wang, S. Tandon, J. Kiske, W. Song, J. Puzhayampallil, M. Andriluka, P. Rajpurkar, T. Mignutus, R. Cheng-Yue et al., “An empirical evaluation of deep learning on highway driving,” arXiv preprint arXiv:1504.01716, 2015.

[32] Intel Corporation, “Intel® Deep Learning Inference Accelerator-Product Specification and User Guide,” https://www.intel.com/content/dam/support/us/en/documents/server-products/server-accessories/Intel_DLIA_UserGuide_1.0.pdf, 2017.

[33] N. P. Jouppi, C. Young, N. Patil, D. Patterson, G. Agrawal, R. Bajwa, A. Bommireddy, S. Bryant, S. Buxman, B. Chen et al., “In-datacenter performance analysis of a tensor processing unit,” in Proceedings of the 2013 IEEE/ACM 44th Annual International Symposium on Computer Architecture (ISCA), 2017.

[34] Khald Moammer, “Nvidia gtx 1070 undressed, gp104 gpu gets first ever die shots Î§ disconnecting the heart of geforce,” 2016, https://wccftech.com/nvidia-gtx-1080-gp104-die-shot/.

[35] A. Krizhevsky and G. Hinton, “Learning multiple layers of features from tiny images,” Citeseer, Tech. Rep., 2009.
[77] C. Yan, D. Englender, M. Prvulovic, B. Rogers, and Y. Solihin, “Improving cost, performance, and security of memory encryption and authentication,” in Proceedings of the 33rd Annual International Symposium on Computer Architecture (ISCA), 2006.

[78] M. Yan, C. Fletcher, and J. Torrellas, “Cache telepathy: Leveraging shared resource attacks to learn dnn architectures,” arXiv preprint arXiv:1808.04761, 2018.

[79] V. Young, P. J. Nair, and M. K. Qureshi, “DEUCE: write-efficient encryption for non-volatile memories,” in Proceedings of the Twentieth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2015.

[80] Y. Zhao, I. Shumailov, R. Mullins, and R. Anderson, “To compress or not to compress: Understanding the interactions between adversarial attacks and neural network compression,” in Proceedings of the Conference on Systems and Machine Learning (SysML), 2019.