A SOT-MRAM-based Processing-In-Memory Engine for Highly Compressed DNN Implementation

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Abstract—The computing wall and data movement challenges of deep neural networks (DNNs) have exposed the limitations of conventional CMOS-based DNN accelerators. Furthermore, the deep structure and large model size will make DNNs prohibitive to embedded systems and IoT devices, where low power consumption are required. To address these challenges, spin orbit torque magnetic random-access memory (SOT-MRAM) and SOT-MRAM based Processing-In-Memory (PIM) engines have been used to reduce the power consumption of DNNs since SOT-MRAM has the characteristic of near-zero standby power, high density, none-volatile. However, the drawbacks of SOT-MRAM based PIM engines such as high writing latency and requiring low bit-width data decrease its popularity as a favorable energy efficient DNN accelerator. To mitigate these drawbacks, we propose an ultra energy efficient framework by using model compression techniques including weight pruning and quantization from the software level considering the architecture of SOT-MRAM PIM. And we incorporate the alternating direction method of multipliers (ADMM) into the training phase to further guarantee the solution feasibility and satisfy SOT-MRAM hardware constraints. Thus, the footprint and power consumption of SOT-MRAM PIM can be reduced, while increasing the overall system throughput at the meantime, making our proposed ADMM-based SOT-MRAM PIM more energy efficiency and suitable for embedded systems or IoT devices. Our experimental results show the accuracy and compression rate of our proposed framework is consistently outperforming the reference works, while the efficiency (area & power) and throughput of SOT-MRAM PIM engine is significantly improved.

In the following paper, we first illustrate how to connect ADMM to our model compression techniques in order to achieve deeply compressed models that are tailored to SOT-MRAM PIM designs. Then we introduce the architecture and mechanism of SOT-MRAM PIM and how to map our compressed model onto it. Finally, we evaluate our proposed framework on different networks. The experimental results show the accuracy and compression rate of our framework is consistently outperforming the baseline works. And the efficiency (area & power) and throughput of SOT-MRAM PIM engine can be significantly improved.

I. INTRODUCTION

Large-scale DNNs achieve significant improvement in many challenging problems, such as image classification [1], speech recognition [2] and natural language processing [3]. However, as the number of layers and the layer size are both expanding, the introduced intensive computation and storage have brought challenges to the traditional Von-Neumann architecture [4], such as computing wall, massive data movement and high power consumption [5], [6]. Furthermore, the deep structure and large model size will make DNNs prohibitive to embedded systems and IoT devices, where low power consumption are required.

To address these challenges, spin orbit torque magnetic random-access memory (SOT-MRAM) has been used to reduce the power consumption of DNNs since it has the characteristic of near-zero standby power, high density, and none-volatile [7]. Combined with the in-memory computing technique [8], [9], the SOT-MRAM based Processing-in-memory (PIM) engine could perform arithmetical and logic computations in parallel. Therefore, the most intensive operation, matrix multiplication and accumulation (MAC) in both convolutional layers (CONV) and fully-connected layers (FC), can be implemented using bit-wise parallel AND, bit-count, bit-shift, etc.

Compared to SRAM and DRAM, SOT-MRAM has higher write latency and energy [7], [10], [11], which decrease its popularity as a favorable energy efficient DNN accelerator. To mitigate these drawbacks, from the software level, weight quantization has been introduced to SOT-MRAM PIM. By using binarized weight representation, [10] efficiently processed data within SOT-MRAM to greatly reduce power-hungry and omit long distance data communication. However, weight binarization will cause accuracy degradation, especially for large-scale DNNs. In reality, many scenarios require as high accuracy as possible, e.g., self-driving cars. Thus, binarized weight representation is not favorable.

In this work, we propose an ultra energy efficient framework by using model compression techniques [12]–[16] including weight pruning and quantization from the software level considering the architecture of SOT-MRAM PIM. To further guarantee the solution feasibility and satisfy SOT-MRAM hardware constraints while providing high solution quality (no obvious accuracy degradation after model compression and after hardware mapping), we incorporate the alternating direction method of multipliers (ADMM) into the training phase. As a result, we can reduce the footprint and power consumption of SOT-MRAM PIM, and improve the overall system throughput, making our proposed ADMM-based SOT-MRAM PIM more energy efficiency and suitable for embedded systems or IoT devices.

In the following paper, we first illustrate how to connect ADMM to our model compression techniques in order to achieve deeply compressed models that are tailored to SOT-MRAM PIM designs. Then we introduce the architecture and mechanism of SOT-MRAM PIM and how to map our compressed model onto it. Finally, we evaluate our proposed framework on different networks. The experimental results show the accuracy and compression rate of our framework is consistently outperforming the baseline works. And the efficiency (area & power) and throughput of SOT-MRAM PIM engine can be significantly improved.
II. A UNIFIED AND SYSTEMATIC MODEL COMPRESSION FRAMEWORK FOR EFFICIENT SOT-MRAM BASED PIM ENGINE DESIGN

In this section, we propose a unified and systematic framework for DNN model compression, which simultaneously and efficiently achieves DNN weight pruning and quantization. By re-forming the pruning and quantization problems into optimization problems, the proposed framework can solve the structured pruning and low-bit quantization problems iteratively and analytically by extending the powerful ADMM [17] algorithm.

In the meantime, our structured pruning model has a unique (i.e., tiny and regular) spatial property which naturally fits into the SOT-MRAM based processing-in-memory engine utilization, thereby successfully bridges the gap between the large-scale DNN inference and the computing ability limited platforms. After mapping the compressed DNN model on SOT-MRAM based processing-in-memory engine, bit-wise convolution can be executed with very high efficiency consistently.

A. DNN Weight Pruning using ADMM

For an $N$-layer DNN of interest. The first $M$ layers are CONV layers and the rest are FC layers. The weights and biases of the $i$-th layer are respectively denoted by $W_i$ and $b_i$, and the loss function associated with the DNN is denoted by $f(\{W_i\}_{i=1}^N, \{b_i\}_{i=1}^N)$; see [18]. In this paper, $\{W_i\}_{i=1}^N$ and $\{b_i\}_{i=1}^N$ respectively characterize the collection of weights and biases from layer 1 to layer $N$.

In this paper, our objective is to implement structured pruning on the DNN. In the following discussion we focus on the CONV layers because they have the highest computation requirements. More specifically, we minimize the loss function subject to specific structured sparsity constraints on the weights in the CONV layers, i.e.,

$$\min_{\{W_i\},\{b_i\}} \ f(\{W_i\}_{i=1}^N, \{b_i\}_{i=1}^N),$$

subject to $W_i \in S_i, \ i = 1, \ldots, M$,\hspace{1cm}(1)

where $S_i$ is the set of $W_i$ with desired “structure”. Next we introduce constraint sets corresponding to different types of structured sparsity to facilitate SOT-MRAM PIM engine implementation.

The collection of weights in the $i$-th CONV layer is a four-dimensional tensor, i.e., $W_i \in \mathbb{R}^{F_i \times C_i \times H_i \times W_i}$, where $F_i, C_i, H_i$, and $W_i$ are respectively the number of filters, the number of channels in a filter, the height of the filter, and the width of the filter, in layer $i$.

Filter-wise structured sparsity: When we train a DNN with sparsity at the filter level, the constraint on the weights in the $i$-th CONV layer is given by $W_i \in S_i := \{X | \text{the number of nonzero filters in } X \text{ is less than or equal to } \alpha_i\}$. Here, nonzero filter means that the filter contains some nonzero weight.

Channel-wise structured sparsity: When we train a DNN with sparsity at the channel level, the constraint on the weights in the $i$-th CONV layer is given by $W_i \in S_i := \{X | \text{the number of nonzero channels in } X \text{ is less than or equal to } \beta_i\}$. Here, we call the $c$-th channel nonzero if $\{X_{i,c,:,:}\}$ contains some nonzero element.

Kernel-wise structured sparsity: When we train a DNN with sparsity at the Kernel level, the constraint on the weights in the $i$-th CONV layer is given by $W_i \in S_i := \{X | \text{the number of nonzero vectors in } \{X_{i,c,:,:}\}_{f,c=1}^F \text{ is less than or equal to } \theta_i\}$. To solve the problem, we propose a systematic framework of dynamic ADMM regularization and masked mapping and retraining steps. We can guarantee solution feasibility (satisfying all constraints) and provide high solution quality through this integration.

B. Solution to the DNN Pruning Problem

Corresponding to every set $S_i, \ i = 1, \ldots, M$ we define the indicator function $g_i(W_i) = \begin{cases} 0 & \text{if } W_i \in S_i; \\ -\infty & \text{otherwise}. \end{cases}$

Furthermore, we incorporate auxiliary variables $Z_i, \ i = 1, \ldots, M$. The original problem (1) is then equivalent to

$$\min_{\{W_i\},\{b_i\}} \ f(\{W_i\}_{i=1}^N, \{b_i\}_{i=1}^N) + \sum_{i=1}^M g_i(Z_i),$$

subject to $W_i = Z_i, \ i = 1, \ldots, M$.\hspace{1cm}(2)

By adopting augmented Lagrangian [19] on (2), the ADMM regularizar decomposes problem (2) into two subproblems, and solves them iteratively until convergence.

The first subproblem is

$$\min_{\{W_i\},\{b_i\}} \ f(\{W_i\}_{i=1}^N, \{b_i\}_{i=1}^N) + \sum_{i=1}^M \rho_i \left\|W_i - Z_i + U_i^k\right\|^2_F,$$

where $U_i^k := U_i^{k-1} + W_i^k - Z_i^k$. The first term in the objective function of [3] is the differentiable loss function of the DNN, and the second term is a quadratic regularization term of the $W_i$’s, which is differentiable and convex. As a result [3] can be solved by standard SGD. Although we cannot guarantee the global optimality, it is due to the non-convexity of the DNN loss function rather than the quadratic term enrolled by our method. Please note that this subproblem and solution are the same for all types of structured sparsities.

The Second subproblem is

$$\min_{\{Z_i\}} \ \sum_{i=1}^M g_i(Z_i) + \sum_{i=1}^M \rho_i \left\|W_i^{k+1} - Z_i + U_i^k\right\|^2_F.$$\hspace{1cm}(4)

Note that $g_i(\cdot)$ is the indicator function of $S_i$, thus this subproblem can be solved analytically and optimally [19]. For $i = 1, \ldots, M$, the optimal solution is the Euclidean projection of $W_i^{k+1} + U_i^k$ onto $S_i$. The set $S_i$ is different when we apply different types of structured sparsity, and the Euclidean projections will be described next.

Solving the second subproblem for different structured sparsities: For filter-wise structured sparsity constraints, we first calculate

$$R_{\text{f}} = \left\|(W_i^{k+1} + U_i^k)_{f,:,:}\right\|^2_F.$$

Note that $g_i(\cdot)$ is the indicator function of $S_i$, thus this subproblem can be solved analytically and optimally [19]. For $i = 1, \ldots, M$, the optimal solution is the Euclidean projection of $W_i^{k+1} + U_i^k$ onto $S_i$. The set $S_i$ is different when we apply different types of structured sparsity, and the Euclidean projections will be described next.
for $f = 1, \ldots, F_i$, where $\| \cdot \|_F$ denotes the Frobenius norm. We then keep $\alpha_i$ elements in $(W_i^{k+1} + U_i^k)_{f,c,:}$ corresponding to the $\alpha_i$ largest values in $\{ R_{f,c} \}_{f=1}^F$ and set the rest to zero.

For **channel-wise structured sparsity**, we first calculate

$$R_{c} = \| (W_i^{k+1} + U_i^k)_{:,c,:} \|^2_F$$

for $c = 1, \ldots, C_i$. We then keep $\beta_i$ elements in $(W_i^{k+1} + U_i^k)_{:,c,:}$ corresponding to the $\beta_i$ largest values in $\{ R_{c} \}_{c=1}^{C_i}$ and set the rest to zero.

For **kernel-wise structured sparsity**, we first calculate

$$R_{f,c} = \| (W_i^{k+1} + U_i^k)_{f,:c,:} \|^2_F$$

for $f = 1, \ldots, F_i$, $c = 1, \ldots, C_i$. We then keep $\theta_i$ elements in $(W_i^{k+1} + U_i^k)_{f,:c,:}$ corresponding to the $\theta_i$ largest values in $\{ R_{f,c} \}_{f=1}^F$ and set the rest to zero.

**C. SOT-MRAM Processing-In-Memory Engine for DNN**

The main purpose of SOT-MRAM PIM engine is to convert and perform the MACs operations in convolutional layers using bit-wise convolution format. There are four main steps included in bit-wise convolutions: parallel AND operation, bitcount, bitshift and accumulation. They can be formulated as Eqn. (5). And $M$ and $N$ stands for the bit-length of inputs and weights respectively. The $c_m(I)$ represents the $n_{th}$-bit of all inputs in $I$, where the $c_n(W)$ contains the $n_{th}$-bit of all weights in $W$.

Consider a CONV layer with $2 \times 2$ kernel size, where $W$ contains 4 weights on a kernel and $I$ contains 4 current inputs covered by this kernel. We assume both weights and inputs are using 3-bit representation. From Figure 1 we can see that inputs and weights are mapped to two different sub-arrays. During the computation, two rows are selected from two sub-arrays each time, and the parallel AND results can be obtained from sense amplifiers [20]. Each row in one sub-array will conduct parallel AND operation with all the rows from the other sub-array. And every AND results will go through bitcount and shifter unit, then accumulated with other results to get a bit-wise convolution result [11].

$$I \ast W = \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} 2^{m+n} \text{bitcount}(\text{and}(c_m(I), c_n(W)))$$

**D. Framework Mapping**

In our proposed framework, based on the architecture of SOT-MRAM-based PIM engine, we incorporate structured pruning and quantization using ADMM to effectively reduce the PIM engine’s area and power. Quantization can be integrated in the same ADMM-based framework with different constraints. We omit the details of ADMM quantization due to space limit. Please note that our ADMM-based framework can achieve weight pruning and quantization simultaneously or separately. Moreover, the overall throughput of SOT-MRAM based DNN computing system can be improved as well. The SOT-MRAM-based PIM engine contains several processing elements (PEs). And each PE consists a column decoder, a row decoder, one computing set and multiple SOT-MRAM sub-arrays as shown in Figure 2(a). It also shows how we map the inputs and weights to the PIM engine. In each PE, the inputs will be mapped on one sub-array, and every other sub-array will accommodate the different filters’ weights from the same input channel. For example, the PE1 will compute the convolution of the inputs in channel1 and all the weights in channel1 from filter1 to filterm. And the number of columns and rows in each sub-array depends on the kernel size of the network and the bit-length of the inputs and weights respectively. All PEs are able to work parallely and individually.

In Figure 2(b), examples are given to show the corresponding structured pruning types that are used in our proposed framework and how it facilitates the reduction of PIM engine size. For the filter pruning, all the sub-arrays on the same row (i.e., storing the weights from the same filter) can be removed.
by quantizing the weights to fewer bits. The number of rows in each sub-array can be evenly reduced equals to the bit-length that is used to represent the weights. This allows for a reduction in complexity and power consumption, as well as easier maintenance and system throughput.

Table I: Structured pruning results on MNIST, CIFAR-10 and ImageNet using VGG-16 and ResNet-18/50 (RNT-18/50 in table). Accuracy results for ImageNet format as Top-1/Top5 accuracy.

| Method                  | Base Accuracy | Prune Accuracy | CONV Comp. Rate |
|-------------------------|---------------|----------------|------------------|
| RNT-50 (LeNet-5)        |               |                |                  |
| Group Scissor [21]      | 99.15%        | 99.14%         | 4.2×             |
| Our's                   | 99.16%        | 99.12%         | 81.3×            |
| CIFAR-10                |               |                |                  |
| DCP [22]                | 88.9%         | 87.6%          | 2.0×             |
| AMC [23]                | 90.5%         | 90.2%          | 2.0×             |
| Our's                   | 94.1%         | 93.2%          | 59.8×            |
| Iterative Pruning [24]  | 92.5%         | 92.2%          | 2.0×             |
| 2PPFCE [26]             | 92.9%         | 92.8%          | 4.0×             |
| Our's                   | 93.7%         | 93.3%          | 44.8×            |
| ImageNet                |               |                |                  |
| Deep compression [27]   | 57.2/82.2%    | 57.2/80.3%     | 2.7×             |
| NeST [28]               | 57.2/82.2%    | 57.2/80.3%     | 4.2×             |
| Our's                   | 57.4/82.4%    | 57.3/82.2%     | 5.2×             |
| Network Slimming [29]   | 68.9/88.7%    | 67.2/87.4%     | 1.4×             |
| DCP [22]                | 69.6/88.9%    | 69.2/88.8%     | 3.3×             |
| Our's                   | 69.9/89.1%    | 69.1/89.4%     | 3.0×             |
| Soft Filter Prune [30]  | 76.1/92.8%    | 74.6/92.1%     | 1.7×             |
| ThiNet [31]             | 72.9/91.1%    | 68.4/88.3%     | 3.3×             |
| Our's                   | 76.8/92.8%    | 75.5/92.3%     | 2.7×             |

Thus, the number of sub-arrays that are contained by each PE will be reduced. For the channel prune, since the pruned channels are no longer needed, the number of required PEs can be reduced without decreasing the throughput. Since each sub-array stores the weights from one channel of one filter, which is also considered as the weights from one convolution kernel, the kernel pruning will remove all the weights on a sub-array. By applying filter pruning and channel pruning, all the pruned sub-arrays or PEs can be physically removed directly. However, removing the sub-arrays by kernel pruning may cause an uneven size between different PEs. But since all the sub-arrays have same size and a sub-array is considered as a basic computing unit in bit-wise convolutions, the control overheads for addressing uneven sub-array numbers in PEs is ignorable. An alternative way is to use a look-up-table (LUT) to mark those pruned sub-arrays and skip them during computation instead of removing them physically.

Each pruning type has its own advantages. The filter pruning and channel pruning has propagation property. Because filter pruning (channel pruning) can not only remove the pruned weights but also removes the corresponding output channels (input channels) as well. By taking the advantage of that, the corresponding channels (filters) in next (previous) layer become redundant and can also be removed. The kernel pruning is especially tailored to the SOT-MRAM-based DNN computing system. Compared to filter and channel pruning, kernel pruning provides higher pruning flexibility, which means it is easier to maintain network accuracy under the same pruning rate. And none of them will incur complicated control logic.

The ADMM based quantization is also used in our proposed framework. In each weight sub-array, the number of rows equals to the bit-length that is used to represent the weights. The number of rows in each sub-array can be evenly reduced by quantizing the weights to fewer bits.

Fig. 3: Power/area reduction and throughput improvement over uncompressed models using MNIST and CIFAR-10 dataset.

III. EXPERIMENTAL RESULTS

In our experiment, our generated compressed models are based on four widely used network structures, LeNet-5 [32], AlexNet [1], VGG-16 [33] and ResNet-18/50 [34], and are trained on an eight NVIDIA RTX-2080Ti GPUs server using PyTorch [35]. For hardware results, we choose 32nm CMOS technology for the peripheral circuits. Cacti 7 [36] is utilized to compute the energy and area of buffers and on-chip interconnects. NVSim platform [37] with modified SOT-MRAM configuration is used to model the SOT-MRAM sub-arrays. The power and area results of ADC are taken from [38].

Several groups of experiments are performed, and we only show one result under each dataset and network, which achieves highest compression rate with minor accuracy degradation. Our results are based on 8-bit quantization, and we use combined pruning scheme (which means all three pruning types are used simultaneously). Table I shows our result on MNIST dataset using LeNet-5 can achieve 81.3× compression without accuracy degradation, which is 19.4× higher than Group Scissor [21]. Our CIFAR-10 dataset, our compression rates achieve 59.8× and 44.8× on ResNet-18 and VGG-16 networks with minor accuracy degradation. And on ImageNet, our compression rates for AlexNet, ResNet-18 and VGG-16 is 5.2×, 3.0× and 2.7×, respectively.

By applying our framework, the power and area of SOT-MRAM PIM engine can be significantly reduced and the overall system throughput can also be improved comparing to uncompressed design, as shown in Figure 3. From our observation, channel pruning usually contributes more power and area saving than filter and kernel pruning, since it can remove entire PE with its peripheral circuits. On the other hand, the filter and kernel pruning can reduce the computing iterations between sub-arrays, which can improve the overall throughput.

IV. CONCLUSION

In this paper, we propose an ultra energy efficient framework by using model compression techniques including weight pruning and quantization at the algorithm level considering the architecture of SOT-MRAM PIM. And we incorporate ADMM into the training phase to further guarantee the solution feasibility and satisfy SOT-MRAM hardware constraints. The experimental results show the accuracy and pruning rate of our framework is consistently outperforming the baseline works. Consequently, the area and power consumption of SOT-MRAM PIM can be significantly reduced, while the overall system throughput is also improved dramatically.
