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Research Update: Reactively sputtered nanometer-thin ZrN film as a diffusion barrier between Al and boron layers for radiation detector applications

Negin Golshani, V. Mohammadi, H. Schellevis, C. I. M. Beenakker, and R. Ishihara
ECTM, DIMES, Faculty of Electrical Engineering (EWI), Delft University of Technology (TU Delft), Feldmannweg 17, P.O. Box 5053, 2628 CT Delft, The Netherlands

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In this paper, optimization of the process flow for PureB detectors is investigated. Diffusion barrier layers between a boron layer and the aluminum interconnect can be used to enhance the performance and visual appearance of radiation detectors. Few nanometers-thin Zirconium Nitride (ZrN) layer deposited by reactive sputtering in a mixture of Ar/N₂, is identified as a reliable diffusion barrier with better fabrication process compatibility than others. The barrier properties of this layer have been tested for different boron layers deposited at low and high temperatures with extensive optical microscopy analyses, electron beam induced current, SEM, and electrical measurements. This study demonstrated that spiking behavior of pure Al on Si can be prevented by the thin ZrN layer thus improving the performance of the radiation detectors fabricated using boron layer. © 2014 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution 3.0 Unported License. [http://dx.doi.org/10.1063/1.4897959]

Recently, the ability of a pure boron (PureB) layer for a variety of applications where a shallow p-n junction is required, such as low energy electron detectors, vacuum ultraviolet (VUV) and extreme ultraviolet (EUV) detectors, has been successfully demonstrated and commercialized. Chemical vapor deposition of PureB has been applied to fabricate successfully ultra-shallow, 2 nm deep, silicon p⁺n junction diodes. Pure Al is being used as metallization layer due to the chemical resistance of the PureB-layer to the conventional Al etchant (i.e., diluted HF) and also it provides low-resistance ohmic-contact with P⁺ boron layer. However, when the PureB layer is thin or non-uniform, Al will have direct contact with silicon causing spiking problem. This will short the shallow junction contacts to the substrate. To avoid the spiking, Al/Si(1%) is commonly used for metallization which solves the spiking phenomena but it will introduce Si precipitations that will grow on the Si surface underneath the Al, resulting in a high contact resistance especially for n-doped Si and small contacts. Moreover, in case of using AlSi for metallization in PureB detectors silicon residuals will be left on top of the active region of the detector after wet-etching of Al. Dry etching cannot be used for Al since it damages the boron layer.

In this paper, we will focus on the properties and performance of different barrier layers such as ZrN, Ti, and TiN on top of the PureB layers deposited at 500 °C and 700 °C for low energy electron detector applications. Among different layers, ZrN shows promising and better performance for the low energy electron detectors. Zirconium nitride exhibits attractive properties for IC technology and industrial applications such as high melting point, low electrical resistivity, good phase stability, and chemical inertness. These properties make ZrN an attractive material as diffusion barrier in Al interconnects.

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Author to whom correspondence should be addressed. Electronic mail: negingolshani@gmail.com; Tel: +31-(0)15-2788837; Fax: +31152787369.
ZrN thin films have been deposited typically by inductively coupled plasma (ICP) deposition techniques, remote plasma-enhanced atomic layer deposition, and physical vapor deposition techniques such as vacuum arc deposition, reactive magnetron sputtering, ion beam assisted deposition, metal organic chemical vapor deposition, and pulsed laser deposition. However, reactive sputtering offers advantages in terms of large area growth, good composition control, and conformal coverage of the substrate. Therefore, we used this method in this study.

Boron layer was deposited in an ASM Epsilon one reactor by chemical vapor deposition (CVD) at atmospheric pressure and processing temperatures of 500 °C and 700 °C. The dopant gas, diborane (B₂H₆) was injected with a flow rate of 490 sccm. Hydrogen was used as a carrier gas and for dilution of the doping source. Continuous rotation of the sample provides homogeneous exposure preventing gas depletion phenomena during the deposition. For a given temperature and mentioned conditions, the boron thickness and the doping of the crystalline silicon substrate can be controlled by varying the deposition time. Boron atoms will not be absorbed as a distinct layer on SiO₂. A patterned SiO₂ layer could therefore be used as hard mask for selective boron deposition and it is important to provide, at the same time, an oxide-free Si substrate for the boron layer deposition. This is achieved by HF (0.55%) dip-etching, Marangoni drying, and an in-situ thermal baking step in H₂ ambient prior to deposition.

Figure 1(a) shows a high resolution TEM image of PureB layer deposited at 700 °C for 10 min deposition time. It can be observed that PureB consists of stacked amorphous boron (α-B) and boron-silicon compound (BₓSiᵧ) uniformly deposited over the silicon surface. However, when the deposition time is reduced to 2 min and 40 s as can be seen in Figure 1(b) the uniformity of the boron layer becomes worse. Furthermore, with decreasing deposition temperature to 500 °C, the deposited boron layer after 10 min has a porous structure as shown in Figure 1(c). This should be avoided as depositing a pure Al layer on top of the non-uniform or porous boron layer may lead to Si-Al reaction and spiking.

The starting material is n-type 100 mm (diameter) silicon wafer with (100) orientation and 2-5 Ω cm resistivity. Fabrication starts with 200 nm thick thermal oxidation followed by boron and phosphorous implantations through the oxide layer with proper masks. Boron and phosphorous implantations create the lightly doped p− guard rings surrounding the diodes (180 keV energy and 10¹³/cm² dose) and n-type guard rings between the diodes for separation (180 keV energy and 5 x 10¹⁵/cm² dose), respectively. After implantation steps, 400 nm thick LPCVD SiO₂ layer using TEOS as precursor at 750 °C was deposited followed by an annealing step at 1000 °C for 35 min to activate the dopants. Figure 2 displays a schematic diagram of the fabrication process. Using a

![Figure 1](image_url)
mask, the oxide layer was wet etched in order to prepare the region for the boron deposition. After cleaning steps, HF dipping was performed followed by Marangoni drying. Before boron layer deposition, we performed a prebaking step at 800 °C in H₂ atmosphere to ensure removing native oxide from the surface of target area. The boron layer was deposited at 500 °C and 700 °C on different wafers and different deposition times, using diborane B₂H₆ and H₂ as gas source and carrier gas, respectively.

After the boron layer deposition process, we measured the boron layer thickness using a Wool-lam Ellipsometer system. Depending on the window opening size, boron thickness varies from 2.3 nm to 3.5 nm for 6 min deposition time. Smaller openings have thicker boron layer. Immediately after measurement, we put the wafers in the sputtering metallization system to deposit few nanometers (10 nm) of a barrier layer. Different barrier layers such as ZrN, Ti, and TiN were studied. Then we deposited 1000 nm pure Al followed by a photolithography step to define the contact pads in two steps of dry and wet (0.55% HF dip for 3 min) etching to land on PureB layer. Other wafers had a PECVD SiO₂ layer directly on top of the PureB layer, then opening the contact holes was followed by 1000 nm pure Al deposition. The last step was alloying at 400 °C for 30 min in H₂ and N₂ atmosphere (forming gas) to improve the metal junctions.

All barrier layers were deposited by sputtering. Specifically, the zirconium nitride film was deposited using reactive DC sputtering with a base pressure of 1 × 10⁻⁷ Torr. A target of 99.8% pure zirconium was sputtered in a mixture of argon and nitrogen without breaking the vacuum. The substrate temperature was 350 °C. In 37 s deposition time, a 10 nm thick ZrN film was deposited on the substrate.

In the following paragraphs about the physical and electrical characterization, we will explore different barrier layers in between the PureB and the Al layer. In some applications to improve the performance and reliability of the detectors, at the end of the process, an oxide layer is deposited on top of the detector.
FIG. 3. Thick boron layer can act as barrier between Si and pure Al (a) a sample with 10 min boron deposition at 700 °C shows good barrier layer in the regions with boron layer and (b) 2 min 40 s boron layer is not enough to act as barrier as voids and spikes can be seen. Inset image shows AFM analysis of the surface.15,17

As mentioned in the introductory paragraph, pure Al can create spikes. There are at least two reasons for the spiking formation in the active area of the PureB photodiodes used in low energy electron detectors.16 The first one is related to the cleanliness of the fabrication process. Any possible particles or defects existing already in epi-Si or bulk- silicon layer in the active area of the diodes may prevent boron deposition on those regions resulting in Al reaction with silicon and consequently spiking. Another reason is related to the thickness and uniformity of the boron layer. A thicker layer of PureB (10 min deposition at 700 °C) can act as a diffusion barrier between Al and the silicon substrate and results in a defect free entrance window.17 However, for detection of low energy radiation, the boron layer should be as thin as possible. It has been shown that a very thin layer of PureB can act as reliable p-type dopant for p+n junctions,3 however, it is not thick enough to act as good diffusion barrier.15

Figure 3(a) shows a SEM image of the silicon surface for a sample which had contact holes with and without thicker boron layer deposition followed by pure Al deposition, 20 min alloying at 400 °C and selective removal of the aluminum. It can be observed (from Figure 3(a)) that the thicker boron layer can act as diffusion barrier and prevents spiking. Thicker layer of PureB (~5 nm), which is deposited for 10 min at 700 °C, forms a barrier between Si and Al.17 Figure 3(b) shows a sample with 2 min 40 s deposition time (~1.8 nm average thickness) which after Al wet etching shows in some points of the silicon surface spiking and also precipitates can be seen in inset image of AFM analysis.15

PureB deposition at low temperatures such as 500 °C results in a non-uniform layer3 with some pinholes in PureB. After pure Al deposition, it reacts with silicon in the areas where there is no boron layer and difficulties arise in removing Al from voids inside of the nanometers thin PureB surface, while at the same time the above-deposited pure Al layer has to be preserved (Figure 4). In this SEM image, some Al dots or residuals are observed after wet Al etching. These Al dots might create dark spots on the final image of the detector.

On the other hand, if we use an AlSi (1%) metal layer directly on the boron layer and try to etch it with HF 0.55% solution to expose the boron layer, silicon dots will stay on top of the active region of the detector as shown in Figure 5(a). Silicon dots will create dark spots on the image too. To remove the silicon residuals, 30 s poly-silicon etchant (HF, HNO₃, CH₃COOH, and H₂O) can be used. However, this solution will remove the boron layer too, hence AlSi is not a good option to deposit on top of the PureB for metallization. We tried to use a 40 nm thick Ti layer between AlSi and boron layer however, as it can be seen in Figure 5(b) after Al etching, Si dots are still remaining on top of the Ti layer. By using a thin layer of Ti/TiN as diffusion barrier layer between Si and pure Al, the spiking problem can be solved. However, if Ti/TiN is used as a barrier layer in PureB photodiodes, removing this layer on top of a few nanometers thin boron layer in the entrance window is challenging because at the same time the above-deposited pure Al layer has to be preserved. Figures 5(c) and 5(d) show removal of the Ti/TiN layer on top of a few nanometers thick PureB layer. As it can be seen, the Al metal grid layers are over-etched while still there is a Ti layer left on the active
FIG. 4. Top view SEM image after Al wet-etching from boron layer deposited at 500 °C.

FIG. 5. Optical image of a wafer with Boron layer deposited at 700 °C followed by (a) 100 nm AlSi and 875 nm pure Al layers, (b) 40 nm Ti and 875 nm AlSi, (c) and (d) Ti and pure Al deposition, Al grid is over etched while Ti is not etched completely.

area of the detector. Al grid layer is used on top of the boron layer to lower the series resistance of diodes. Therefore, Ti on boron layer is not a good option for a diffusion barrier layer.

Using a thin barrier layer on top of the boron layer before pure Al deposition might passivate the silicon surface. In Figures 6(a) and 6(b), SEM inspection in combination with EBIC (Electron Beam Induced Current) imaging displays an unexpected high number of pits in the surface of the active area of the detector in case of existing Al residuals on the surface when there is no barrier layer between pure Al and Si. Those dark spots lead to dead regions for the detector. Energy dispersive x ray (EDX) analysis verified aluminium existing in the locations of the dots.
FIG. 6. On top SEM (a) and EBIC (b) images of the detector surface, (with Boron layer deposited at 700 °C) for sample without ZrN layer. Si surface was defective before Boron deposition hence, high number of unwanted Al dots is seen. On bottom 2 kV ETD (Everhart-Thornley Detector) (c) and 2 kV EBIC (d) images of sample with few nanometers thin ZrN layer as diffusion barrier between Al and PureB show no Al dots and no dark spots as dead layer.

To remove Al residuals from the detector surface, different barrier layers such as TiN, AlN, and ZrN were examined. Using AlN as barrier layer increases the series resistance of the diodes and may impact on the performance of the fabricated detectors. This effect is more pronounced in devices with very small areas. It is mentioned that it is very difficult to remove TiN from a thin boron layer selectively.

Depositing nanometers thin ZrN on top of the PureB is more promising to prevent diffusing of Al to the Si substrate. To study this we deposited, after boron layer deposition, a very thin layer of ZrN, 10 nm, as diffusion barrier followed by 1075 nm pure Al layer. Figures 6(c) and 6(d) illustrate the entrance window of the detector fabricated using PureB layer followed by few nanometers thin ZrN layer as barrier layer. The surface of the detectors was observed in SEM and EBIC. Images show no dark spots when using ZrN layer on top of the PureB resulting in significantly reduced dead regions. Figure 7 shows two SEM images of the detector surface with boron layers deposited at 700 °C and 500 °C followed by 10 nm ZrN and 875 nm pure Al. As it can be seen, there are no Al dots or any defects on the boron layer in both cases.

We performed electrical measurement for the fabricated devices to see the influence of adding ZrN on the IV and constant voltage (CV) curves. As shown in Figure 8, IV and CV curves are exactly the same when using a barrier layer of ZrN between the boron layer and pure Al on the surface of the detectors and there is no significant increase in the series resistance of diodes. The dark current of the fabricated detectors is in the order of 1 nA/cm² measured at room temperature which shows this few nanometers thick layer does not have any influence in the performance of detector. Another advantage of using ZrN is the fact that the etch rate of ZrN is lower in comparison
with Al layer in 0.55% HF solution. Thus, any possible Al residuals on the surface can be removed by longer wet etching in HF solution while PureB layer is protected by the barrier layer.

In some applications, an oxide layer is used to obtain higher quantum efficiency or responsivity for photodiodes. PECVD oxide and PECVD TEOS are two candidates which can be deposited at low temperature on boron layer while keeping shallow junction properties intact.

The most critical processing step is to deposit and pattern the PECVD oxide or TEOS on top of the boron layer which was deposited at lower temperatures. Some applications require low temperature boron deposition for thermal budget reasons or to obtain higher sheet resistance layer. As mentioned before, boron layer deposited at 500 °C has a non-uniform and porous surface, therefore the subsequent deposited oxide layer might have low adhesion. For these purposes, PECVD oxide and TEOS layers were examined. In general, all wafers with deposited PureB at 700 °C showed good adhesion without any delamination of oxide layer particularly during oxide patterning and Al deposition. However, the wafers with PureB layer deposited at 500 °C had weak adhesion to PECVD oxide hence, pealing-off of boron and oxide layers when doing HF dip step prior to Al deposition (Fig. 9(a)). The possible explanation can be growing oxide under porous boron layer during PECVD oxide deposition which will lead to under etching of oxide during etching as displayed in Figures 9(a) and 9(b). However, PECVD TEOS oxide deposited wafers generally had much better adhesion than PECVD oxide as shown in Figure 9(c).

In order to have a clean surface without Al residuals for the entrance window of the detector, one can use lift-off process to eliminate any Al contact to the radiation entering area. After PureB
layer deposition at 700 °C or 500 °C, a negative photoresist was applied and patterned followed by 400 nm thick Al layer deposition by evaporation. Then, resist was stripped in acetone or an n-methylpryolidone (NMP) solution in an ultrasonic bath. For both PureB layers deposited at 700 °C or 500 °C, the lift-off process was successfully performed as shown in Figure 10. There was no adhesion problem or any Al dots observed on the surface of the detectors. However, in this process, Al thickness is limited to 400 nm otherwise stripping resist will be very difficult.

In this paper, it was shown that reactively sputtered 10 nm ZrN as a diffusion barrier between a thin boron layer and pure Al can enhance the quality of the detectors without any influence on the electrical parameters of the devices and is compatible with detectors fabrication flowcharts. Furthermore, for the low temperature deposited PureB layer, it was shown that PECVD TEOS has better adhesion than PECVD oxide to the porous boron layer to enhance the responsivity of the detectors. Alternatively, lift-off process was introduced and was used successfully in the detectors process flow to avoid any contact between Al and silicon layers. Best results based on visual inspection and electrical measurements were obtained for boron deposition at 700 °C and a thin layer of 10 nm ZrN. On this layer, PECVD oxide shows good adhesion and can be used to improve the performance of the detector.

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