A Soft Error Study on Tri-gate Based FinFET and Junctionless-FinFET 6T SRAM Cell - A Comparison

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Abstract

When junction based semiconductor devices are scaled down to extreme lower dimensions, the formation of ultra-sharp junctions between source/drain and channel becomes complex since the doping concentration has to vary by several orders of magnitudes over a distance of a few nanometers. In addition, as CMOS device is scaling down significantly, the sensitivity of Integrated Circuits (ICs) to Single Event Upset (SEU) radiation increases. As soft errors emerge as reliability threat there is a significant interest lies both at device and circuit level for SEU hardness in memories. The critical dose observed in FinFET and Junctionless-FinFET (JLT) based 6T-SRAM is given by LET=1.4 and 0.1 pC/µm. The simulation result analyzes electrical and SEU radiation parameters of FinFET and JLT based 6T-SRAM memory circuit.

Keywords: FinFET 6T-SRAM, Junctionless 6T-SRAM, SEU Radiation, LET, HeavyIon, TCAD Simulation

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1. Introduction

The conventional single gate planar devices like bulk and SOI and multi-gate structures like FinFETs, tri-gate, and Gate-All-Around (GAA) devices control the current flow through junctions and hence they are called as junction-based devices. When these devices are scaled down to extreme dimensions, the formation of ultra-sharp junctions between source/drain and channel becomes complex since the doping concentration has to vary by several orders of magnitudes over a distance of a few nanometers. Therefore highly accurate doping techniques and ultrafast dopant activation processes are required to avoid the lateral diffusion of source and drain impurities into the channel region. Based on Lilienfeld’s first transistor architecture a solution to this problem [1] very recently, a transistor has been proposed, successfully fabricated and named as Junctionless Field Effect Transistor [2, 3] which exhibits an unconventional architecture that presents neither source/drain junctions nor doping concentration gradients. As the name suggests these devices do not have p-n junctions i.e. the junctions do not play any role in the current flow [4-7]. The device is basically a resistor in which the mobile carrier density can be modulated by the gate. The work function difference between the gate electrode and the fin/silicon film is exploited to make the threshold voltage to positive values (assuming an n-channel device). The JLT and JLT MuGFET is a promising device for future technology as it reduces the fabrication complexity as well as cost of fabrication. To optimize the performance of JLT, new design approaches, such as, SOI JLFET, bulk planar JLFET, nanowire Junctionless transistors [8,9] Gate All Around FET etc. [10] have been proposed. The radiation analysis of a Junctionless device is studied by [11]. In this work, FinFET and Junctionless-FinFET based 6T-SRAM is subjected to heavy ion type SEU radiation. Minimum radiation dose required to flip the cell is found out by doing the transient simulations with radiation models turned-on in TCAD device simulator.

2. Device Construction and Calibration

The 2-D schematic view of FinFET and JLT device is as shown in Figure 1 which consists of various device level geometrical parameters and regions [12-15]. Figure 2 and 3 shows NMOS and PMOS structure of FinFET and JLT (Gate oxide is removed). Table 1 gives the various device dimensions and doping values.
Table 1. Device Dimensions

| Parameter                             | FINFET         | JLT            |
|---------------------------------------|----------------|----------------|
| Gate Length ($L_g$)                   | 30 nm          | 30 nm          |
| Gate-oxide thickness ($T_{ox}$)       | 2 nm           | 2 nm           |
| Fin width ($W$)                       | 5 nm           | 5 nm           |
| Fin height ($H$)                      | 5 nm           | 5 nm           |
| Channel doping                        | $1 \times 10^{15}/cm^2$ (N transistor) | $8 \times 10^{19}/cm^2$ (N transistor) |
| Source-drain doping                   | $1 \times 10^{20}/cm^2$ (N transistor) | $8 \times 10^{19}/cm^2$ (P transistor) |

Figure 1. 2-D Schematic view of FinFET and Junctionless-FinFET device

Figure 2. Common Tri-gate NMOS Device Structure of FinFET and JLT (Gate Oxide is removed)

Figure 3. Common Tri-gate PMOS Device Structure of FinFET and JLT (Gate Oxide is removed)
An $I_d-V_g$ characteristic of NMOS (FinFET and JLT) device is shown in Figure 4. Supply Voltage ($V_{dd}$) used in this study is 1 V. Following $I_d-V_g$ simulations, both the devices are biased in off state i.e. $V_g=0$ V and $V_d=V_{dd}$, and irradiated with heavy ions. The radiation is supposed to impact the leakage current and is shown in Figure 5. The radiation peak time=0.2 µs. It can be observed from Figure 5 that Junctionless device shows more disturbances compared to FinFET device. The three different fin doping concentration and the radiation induced drain current transient peaks are shown in Figure 6a and 6b.

![Figure 4: Common Tri-gate NMOS Device $I_d-V_g$ simulation of FinFET and JLT](image1)

![Figure 5: FinFET and Jnless Device SEU simulation](image2)

![Figure 6: Drain current transients of Junctionless device for different dopingsion ion strikes at 275e-12s with LET=0.1 pC/µm and FinFET device for different dopings ion strikes at 275e-12s with LET=1.4 pC/µm](image3)
The drain current peaks during the radiation strike. After radiation strike at \( t=275 \text{ ps} \) the floating body effects related to junctionless device are the cause for this difference at the tail portion and the doping concentration affects the behavior substantially as shown in Figure 6.

Figure 6 shows no variation for different fin doping concentration from the radiation-hardness point of view, the lower doping level in a silicon film of a FinFET could have less impact on its immunity to radiation strike; also floating-body effects are lower. The peak disturbances are independent of the doping values in Figure 6.

3. FinFET and Junctionless 6T-SRAM Structure

A FinFET and JLT based 6T-SRAM cell is designed by replacing the conventional MOSFETs with FinFET and Junctionless transistors. The generated 6T-SRAM structure from SDE is shown in Figure 7. Meshing is shown on one-side of the device namely (N2, ACC2, P2 transistors) in Figure 7.

Figure 8 Shows 6T-SRAM operation simulation curve before SEU radiation. Mixed mode simulation approach is used in SRAM simulation. In mixed mode simulation some portion of the circuit can be simulated at the device level and some part of the circuit can use compact models. In this study, interconnects are assumed to be perfect interconnects.

Figure 9 shows the collected charge at strike node with an LET=0.09 pC/\( \mu \text{m} \) (which does not flip both the 6T-SRAM cell) of the FinFET and Junctionless 6T-SRAM when an heavy-ion strikes the OFF-state NMOS transistor. We can see junctionless transistor collected charges are higher compared to FinFET based device.
The SRAM cells consist of FinFET and Junctionless based 6T-SRAM tri-gate topologies as mentioned. To study radiation performance of these two 6T-SRAM circuits independently the dose value or LET is varied from the flipped LET value. The ion strikes at 275e-12s with LET=1.4 pC/µm.

Figure 10 shows the drain current variation of FinFET and Junctionless 6T-SRAM with three different LET values. FinFET and Junctionless 6T-SRAM current peaks can be clearly seen which ranges in the orders of pA and µA.

**4. SEU Radiation Effects and Results**

FinFET and JLT 6T-SRAM have been studied to extract the critical charge ($Q_{crit}$). Length of the ion track is 0.035µm, characteristic radius $w_t=0.01\,\mu m$. Figure 11 shows peak time radiation simulation of both FinFET and JLT based 6T-SRAM structure.

Figure 12 shows node voltages of FinFET and JLT 6T-SRAM after heavy ion strike at 275 ps for LET=1.3 pC/ µm and LET=0.09 pC/ µm (which does not flip both the cell). Whereas Figure 13 shows node voltages after heavy ion strike at 275 ps for LET =1.4 pC/µm and LET=0.1 pC/µm.

There are various parameters like electron and hole densities, electron and hole current densities, electro-static potential, SRH recombination rate etc. can be analyzed to study the SEU radiation effects. Tri-gate Jnless 6T-SRAM based structure switches its state at LET value of 0.1 pC/µm and the FinFET structure flips at 1.4 pC/µm.
Figure 12. Node Voltages after Heavy ion strike at 275 ps for LET=1.3 pC/µm (FINFET) and LET= 0.09 pC/µm (JLT).

Figure 13. Node Voltages after Heavy ion strike at 275 ps for LET= 1.4 pC/µm (FINFET) and 0.1 pC/µm (JLT).

Figure 14 and 15 depict the SRH recombination across the both the structures, at three different time instants, i.e. @250 pS, @275 pS, and @330 pS. These time instants correspond to pre, peak and post radiations. It can be observed that SRH recombination rate is very low for pre and post radiations.

Figure 14. JLT 6T-SRAM SRH Recombination pre-peak-post radiation simulation.
Figure 15. FINFET 6T-SRAM SRH Recombination pre-peak-post radiation simulation

It may also be noted that SRH recombination is lower in Junctionless SRAM structure compared to the FinFET structure, for peak radiation. Since the Junctionless device’s drain uses a doping of $8 \times 10^{19}$ cm$^{-3}$ (for N device) and $2.5 \times 10^{19}$ cm$^{-3}$ (for P device) and the FinFET device’s drain uses a doping value of $1 \times 10^{20}$ cm$^{-3}$ (for both N and P devices) the reduction in SRH recombination is expected in Junctionless structure. This can be attributed to the lower critical dose value of the Junctionless SRAM compared to the FinFET SRAM.

5. Conclusion

Tri-gate FinFET and Jnless 6T-SRAM is simulated and studied for their SEU/soft error performance (the minimum LET value required to flip the cell) in TCAD. As the doping concentration is higher, SRH recombination rate accordingly lowers which can be observed from peak radiation curves of Figure 15 and 16. The LET required to flip the FinFET and Jnless 6T-SRAM is found to be $\text{LET}=1.4$ and $0.1 \text{ pC/µm}$.

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