CNFET Based Voltage Differencing Transconductance Amplifier

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Abstract: In CMOS Technology basic Problem mainly includes dopant fluctuation, tunnelling effect and line edge roughness below 45nm technology. Carbon Nanotube based structures is better option for widen the Moore’s law due to its scalability channel electrostatics and higher mobility. In this manuscript we demonstrate an optimum design for linear property of CNTFET based VDTA at 32nm technology node. The proposed circuit consist of VDTA with CNTFET having two voltage input and two current outputs so that it works as voltage and transconductance operation to obtain the high performance. The minimum supply voltages of ±0.9V with 32nm technology mode are used. The CNTFET-VDTA performance is simulated on HSPICE. In this paper CNFET-based VDTA provides better results of DC transfer characteristics as compared with CMOS. All the simulation results are performed on HSPICE. Keywords: Carbon Nanotube Field Effect Transistor (CNTFET) Carbon Nanotube (CNT), Low voltage operation, Low power, VDTA

Keywords: About four key words or phrases in alphabetical order, separated by commas.

1. INTRODUCTION
In the field of mobile communication system with the beginning of portable electronic the design of low voltage circuit has achieved a lot of importance. In last few years there has been lot of focus on reduction of supply voltage in order to diminish the power consumed by the circuit. For the purpose of low voltage operation in analog signal processing, Voltage Mode (VM) and Current Mode (CM) circuits have found great importance in the field of analog signal processing. In addition to low voltage operations these circuits contribute large dynamic range high speed and low impedance level with low power consumption. We have many active elements which contribute as current mode circuits such as current operational amplifier, current conveyor, current differencing buffered amplifier voltage differencing transconductance amplifier, operational trans-resistance amplifier and have suitably met the requirements. Brief
introduction of this work can be found in [1].

The Voltage differencing transconductance amplifier (VDTA) was originally given by yesil, kacar and kuntman.[2] Better flexibility can be provided because it is operational in both voltage as well as current mode, work at high frequency operation and it is free from parasitic capacitances.

![Fig. 1 Symbolic Notation of VDTA](image)

In analog signal processing many active elements is purposed and these elements have different features but in VDTA there are two voltage input and two current outputs. The symbolic notation of VDTA is shown in Figure 1. The terminals relationship of a VDTA can be characterized by:

$$
\begin{bmatrix}
  i_z \\
  i_{x+} \\
  i_{x-}
\end{bmatrix} =
\begin{bmatrix}
  g_{m_1} & -g_{m_2} & 0 \\
  0 & 0 & g_{m_2} \\
  0 & 0 & -g_{m_2}
\end{bmatrix}
\begin{bmatrix}
  v_p \\
  v_n \\
  v_z
\end{bmatrix}
$$

In VDTA, two input voltage ($V_p$ and $V_N$) which are differential, at terminal $Z$ which is transmit to current by first transconductance gain and the output terminals are represented by $X+, X-, Z$.  

2. CARBON NANOTUBE FIELD EFFECT TRANSISTOR

Ijima of NEC Japan had discovered Carbon nanotube in 1993 which is the allotrope of carbon. Carbon nanotube is taken as a promising material which can be replacing the use of silicon due to its property. Carbon nanotube have unique feature like higher electrical conductivity than silver, Large tensile strength more than steel and large thermal conductivity than diamond. The most important property of of carbon nanotube is 1D ballistic transport capability. Due to these exceptional properties CNT have wide number of applications in the field of nano-electronics and nano-science. Carbon nanotube is available in three types : Single wall carbon nanotube (SWCNT) and (ii) Double wall carbon nanotube (iii) Multiwall carbon nanotube (MWCNT) as demonstrate in Figure 2(a). SWCNT are normally placed at the ends [9-11]. The diameter of SWCNT varies from 1 nm to few micro meter based on the value of (m,n) or type of SWCNT. MWCNT are better than SWCNT but they are costly and they are like co-axial cable. Whereas the diameter of MWCNT varies from 5nm to 50nm with the inter layer spacing of is 3.4Å.. The pair of indices (m,n) is represented by wrapping of sheet which are called Charality vector as demonstrate in figure 2(b). Depending upon the pair of indices the :-z SWCNT is categories in three types:[12-13]

(i) Armchair if (n=0 ,m = 0 and θ = 30°)
(ii) Zig-Zag if \((n=0, m = 0 \text{ and } \theta = 0^\circ)\)  
(iii) Chiral if \((n=0, m = 0 \text{ and } \theta \text{ lies between } 0^\circ \text{ to } 30^\circ)\)

Figure 3 demonstrates the layout diagram of CNTFET, i.e. carbon nanotube field effect transistor (CNTFET). In a CNTFET, the parallel combination of SWCNTs are used to manage channels. Whereas drain and source terminal of CNTFET are highly doped and channel is undoped. The most important advantage of carbon nanotube is 1D ballistic transport capability and large current driving capacity with low power consumption and high mobility. For improvement in the performance of the device below the 45nm technology we use some alternative technique apart from use of CMOS technology because it reaches its scaling limit. So Nanotechnology based devices or fabrication exhibits large density and performance of electronic circuits, electronic characteristic of CNTFET has made it appear brighter [14]. The usual and the basic problems such as leakage currents, lithographic limits, high field effects, extreme short channel effects, and quantum confinement effect related with CMOS are solved to a great extent in CNFET [15]. To enhancing the efficiency of the circuit the width can be channel reduced to 4nm and channel length can be reduce up to 10nm. A large number of issues in fabrication of CNTFET can be resolved now and it look good [16-19].

| Parameters of CNTFET | Value |
|----------------------|-------|
| Oxide thickness\(T_{OX}\) | 4mm |
| Mean free path: Intrinsic CNT | 200NM |
| Gate oxide | HFO₂ |
| Dielectric constant | 16 |
| Power supply | ±0.9v |
| Mean free path: doped CNT | 12.5NM |
| Work function(CNT) | 4.5eV |
| Physical channel Length\(L_{ch}\) | 32nm |
| Pitch | 20nm |
| Chirality of tube \((m,n)\) | 19,0 |

Fig. 2. Structural of Carbon NanoTubes  
Fig. 3 Layout diagram CNTFET
3. Proposed CNTFET Based VDTA

In the conventional MOSFET the channel is replaced by CNTFET as demonstrate in Fig. 3 (layout of CNTFET). Ijima had discovered that CNT’s are long and allotropes of carbon. When they are made up of single shell they are called single wall Carbon nanotube(SWCNT) [20]. They are formed by folding of graphite layer and having quasi 1-D molecular structure. Due to this 1-D structure CNTFET give better control over 2-D and 3-d devices [21]. Moreover, differing in CMOS, in which the aspect ratio of the transistor are regulate to adjust the PMOS/NMOS ratio, a CNTFET-based CDBA is proposed in terms of the following finest structural parameters.

(a) Number of CNTs (N): Since single nanotube based transistor is unable to provide sufficiently good performance over CMOS so in order to give proper current supply for the purpose of driving the fixed capacitive load, it is very much necessary to determine the number of CNTs used in the array.

(b) Inter-CNT Pitch (S): When the two CNTs are lying beside each other in the channel then the distance between their centre is said to be inter CNT pitch. It is denoted by “S” and one of the factor that cannot be ignored when deciding the performance of CNTFET.

(c) Diameter of CNT (Dcnt): The device threshold voltage is directly affected by the diameter of carbon nanotube \( D_{CNT} \), hence requiring careful selection mechanism [24].

\[
D_{cnt} = \frac{A \sqrt{(n^2 + m^2 + mn)}}{\Pi} \quad \text{-------------------1}
\]

\[
V_{th} = \frac{aV_{f1}}{\sqrt{3qD_{cnt}}} \quad \text{-----------------------------2}
\]

\[
W = ((n-1) \times S + D_{cnt}) \quad \text{------------------------3}
\]
The low power low voltage cnfet based vdtas use (M1-M8) mosfet with cntfet having equal channel length and current with 32nm technology node ,where the oxide thickness is taken as 4nm and power supply of ±0.9v material for the gate oxide is chosen as HFO₂, dielectric component 16 ,mean feepat of intrinsic CNTand doped CNT is 200nm and 12.5 nm respectively. Where the most important parameter for the channel length ratio will depend upon the number of carbon tube take in n and p type of CNFET-MOSFET. Figure 4 (b) demonstrate the proposed diagram of the CNFET based VDTA as compared to conventional VDTA shown in figure 4(a).

4. SIMULATION RESULTS AND DISCUSSION

We perform the simulations by using HSPICE at 32 nm technology node And verified the DC transfer characteristics as compared to CMOS-VDTA. Supply voltages are taken as VDD = −VSS = 0.9 V and the biasing currents are taken as IB1 = IB2 = IB3 = IB4 = 150 µA. Simulation results show that this give transconductance values of VDTA as gm1 = gm2 = 636.3 µA/V.

The DC transfer characteristics of CNFET based VDTA realization is shown in figure 5. In the simulation result DC transfer characteristics range is -1V to +1V between voltage and current which is more liner with respect to basic circuit.

5. CONCLUSION

In this paper VDTA based on CNTFET is proposed which is appropriate for low power and low voltage operation at 32nm technology node. The paper has successfully shown the design of CNTFET-CDBA for low power and low voltage along with better DC transfer characteristics.

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