Distributed Training of Deep Neural Networks: Theoretical and Practical Limits of Parallel Scalability.

Janis Keuper
Fraunhofer ITWM
Competence Center High Performance Computing
Kaiserslautern, Germany
Email: janis.keuper@itwm.fhg.de

Franz-Josef Pfreundt
Fraunhofer ITWM
Competence Center High Performance Computing
Kaiserslautern, Germany
Email: franz-josef.pfreundt@itwm.fhg.de

Abstract—This paper presents a theoretical analysis and practical evaluation of the main bottlenecks towards a scalable distributed solution for the training of Deep Neural Networks (DNNs). The presented results show, that the current state of the art approach, using data-parallelized Stochastic Gradient Descent (SGD), is quickly turning into a vastly communication bound problem. In addition, we present simple but fixed theoretic constraints, preventing effective scaling of DNN training beyond only a few dozen nodes. This leads to poor scalability of DNN training in most practical scenarios.

I. INTRODUCTION

The tremendous success of Deep Neural Networks (DNNs) [18], [14] in a wide range of practically relevant applications has triggered a race to build larger and larger DNNs [20], which need to be trained with more and more data, to solve learning problems in fast extending fields of applications. However, training DNNs is a compute and data intensive task: current models take several ExaFLOP to compute, while processing hundreds of petabyte of data [20]. Table I gives an impression of the compute complexity and shows, that even the latest compute hardware will take days to train the medium sized benchmark networks used in our experiments. While a parallelization of the training problem over up to 8 GPUs hosted in a single compute node can be considered to be the current state of the art, available distributed approaches [4], [15], [1], [2], [7] yield disappointing results [19] in terms of scalability and efficiency. Figure 1 shows representative experimental evaluations, where strong scaling is stalling after only a few dozen nodes. In this paper, we investigate the theoretical and practical constraints preventing better scalability, namely model distribution overheads (in section II), data-parallelized matrix multiplication (section III) and training data distribution (section IV).

A. Stochastic Gradient Descent

Deep Neural Networks are trained using the Backpropagation Algorithm [16]. Numerically, this is formulated as a highly non-convex optimization problem in a very high dimensional space, which is typically solved via Stochastic Gradient Descent (SGD) [3]. SGD, using moderate mini-batch sizes $B$, provides stable convergence at fair computational costs on a

Table I

| DNN     | CPU | K80 | TitanX | KNL |
|---------|-----|-----|--------|-----|
| AlexNet |     |     |        |     |
| time per iteration | 2s  | 0.9s | 0.2s [10] | 0.6s |
| time till convergence | 250h | 112h | 25h [10] | 75h |
| GoogLeNet: |     |     |        |     |
| time per iteration | 1.3s | 0.36s | - | 0.32s |
| time till convergence | 361h | 100h | - | 89h |

APPROMATE COMPUTATION TIMES FOR ALEXNET WITH BATCH SIZE $B = 256$ AND 450K ITERATIONS AND GOOGLENET WITH $B = 32$ AND 1000K ITERATIONS. KNL (XENON PHI “KNIGHTS LANDING”) RESULTS WITH MKL17. TITAN X WITH PASCAL GPU. SEE SECTION II.

Fig. 1. Experimental evaluation of DNN training scalability (strong scaling) for different DNNs with varying global batch sizes $B$. Results from an "out of the box" installation of IntelCaffe on a common HPC system (Details are given in section I-B).
single node. However, it is very hard to parallelize. This is due to the inherently sequential nature of the algorithm, shown in equation and algorithm.

\[
w_{t+1} \leftarrow w_t - \epsilon \partial_{w} x_j(w_t),
\]

where \(w_t\) represents the current state (e.g. the weights at the neurons), \(\epsilon\) defines the step-size and \(\partial_{w} x_j(w_t)\) is computed from a given loss-function over the forward results of a small set of training samples (called \textit{mini-batch} and the given training labels). In fact, there are only two ways to speedup SGD: (I) computing updates \(\Delta w\) faster and (II) making larger update steps \(\epsilon\). While (I) is hard to achieve in a distributed setting given already low compute times (<1s) per iteration, (II) is bound by the difficult topologies of the non-convex problems, causing SGD to diverge easily.

1) Parallelizing SGD: Figure 2 shows the data-parallel version of SGD [4], which is commonly used for single node multi-GPU and distributed implementations: The global batch of \(B\) training samples for the current iteration is split into \(n\) equal sized sets of size \(b\) (with \(b = B/n\)) of training samples which are then fed to \(n\) workers holding synchronous local copies of the model state. The results (gradients) off all workers are then accumulated and used to update the model. Hence, the entire approach is implementing a simple \textit{map-reduce} scheme.

Notably, this scheme implies two different levels parallelization: the data- and task-parallel [12] \textit{Inner Parallelization}, located at the compute units of the nodes using parallel algorithms to compute the forward and backward operations within the layers of the DNN (see section [11] for details on the local parallelization of layer operations), and the \textit{Outer Parallelization} over the distributed batches.

B. Experimental Setup

1) Benchmarks: We apply two widely used convolutional networks (CNNs), AlexNet [13] and GoogLeNet [22], for the benchmarking of our experimental evaluations. Both neural networks follow different strategies to learn predictive models for the \textit{ImageNet} [17] visual recognition challenge. While AlexNet implements a rather shallow network with 3 dominant fully-connected (FC) layers, is GoogLeNet using a very deep network with many convolutional layers. Table II shows the technical details of both networks.

| Property                        | AlexNet | GoogLeNet |
|---------------------------------|---------|-----------|
| ExaFLOP to convergence          | \(~0.3\) | \(~1.1\)  |
| # Iterations till convergence   | \(~450k\) | \(~1000k\) |
| Model size @32 bit FP           | \(~250\ MB) | \(~50\ MB) |
| Default batch size              | 256     | 32        |
| Default step-size               | 0.01    | 0.01      |
| # Layers                        | 25      | 159       |
| # Convolutional layers          | 5       | 59        |
| # Fully-connected (FC) layers   | 3       | 1         |
| # Weights in FC layers          | \(~55M\) | \(~1M\)   |

TABLE II PROPERTIES OF THE DEEP NEURAL NETWORKS USED FOR THE FOLLOWING BENCHMARKS.

2) Software Framework: We use the MPI based distributed Version (\textit{IntelCaffe}) [1] of the popular open source framework \textit{Caffe} [9] for our evaluation. \textit{IntelCaffe} was built with CUDA

Fig. 2. Schematic overview of a distributed SGD implementation of the Backpropagation Algorithm.

Algorithm 1 Mini-Batch SGD with samples \(X = \{x_0, \ldots, x_m\}\), iterations \(T\), step-size \(\epsilon\), batch size \(B\)

Require: \(\epsilon > 0\)

1: for all \(t = 0 \ldots T\) do

2: randomly draw batch \(M \leftarrow B\) samples from \(X\)

3: \(\text{Init} \Delta w_t = 0\)

4: for all \(x \in M\) do

5: aggregate update \(\Delta w \leftarrow \partial_{w} x_j(w_t)\)

6: update \(w_{t+1} \leftarrow w_t - \epsilon \Delta w_t\)

7: return \(w_T\)
7.5 and cuDNN 5 using the latest Intel compiler, MKL\(^2\) and IntelMPI.

3) Hardware: All distributed experiments were conducted on a HPC cluster with nodes holding a dual Xeon ES-2680 v3 CPU (12 cores @ 2.50GHz), a NVIDIA Tesla K80 GPU and FDR-Infiniband interconnects.

II. DISTRIBUTION OVERHEAD

The parallelization of DNN training via SGD (as shown in algorithm 1 and figure 2) requires the communication of the model \(w_t\) and the computed gradients \(\Delta w_t\) between all nodes in every iteration \(t\). Since \(w\) has to be synchronous in all nodes and \(\Delta w_{t+1}\) cannot be computed before \(w_t\) is available, the entire communication has to be completed before the next iteration \(t + 1\). Naturally, one would try to overlap this communication (which can be done layer by layer) with the compute times. However, there are several pitfalls to this strategy: (I) \(w\) and \(\Delta w\) have the size of all weights in the neural network, which can be hundreds of megabytes\(^3\). (II) the compute times per iteration are rather low and are decreasing further when scaling to more nodes (see section III). (III) communication can not start before the forward pass of the network has succeeded (practically cutting the overlap times by half). Ironically, faster compute units (e.g. newer GPUs) in the compute nodes increase the fundamental problem, that the communication time exceeds the compute time, after scaling to only a few nodes. Leaving valuable compute units idle. Figure 3 shows the strong divergence of communication- and compute times. Depending on the model size, the training problem becomes communication bound after scaling to only 4 to 8 nodes. This directly correlates to the general scaling results shown in figure 1. Figure 3 also shows, that the network layout has a large impact on the crucial communication/compute ratio: shallow networks with many neurons per layer (like AlexNet) scale worse than deep networks with less neurons (like GoogLeNet) where longer compute times meet smaller model sizes.

A. Limited Network Bandwidth

Limited network bandwidth is one of the key bottlenecks towards the scalability of distributed DNN training. Recently, there have been several approaches proposed to overcome this problem: e.g. \([7]\) introduced a binary communication tree, which reduces the network load to a maximum of \(\log_2(n)\) peer to peer model/gradient sends at a time. However, expecting linear speedups at the compute side, figure 3 shows that this approach will only move the intersection of the communication/compute ratio by a small factor, as the additional overhead is increasing with the depth of the communication tree. Other methods try to reduce the model size before the communication. This can be done by (I) a redesign of the network \([8]\) - eliminating unused weights, (II) limiting the numerical precision of the model weights \([6]\) has shown that one byte per weight is enough), (III) compression (which is available in \([1]\) or (IV) transmitting only sparse gradient and model information \([21]\). All these methods have practical impact, moving the scalability by the factor of the model reduction rate. But non of these approaches is able to solve the problem in principle. As model sizes are increasing much faster than the available network bandwidth, the communication overhead remains an unsolved problem.

III. COMPUTATIONAL COSTS AND SCALING OF MATRIX MULTIPLICATIONS

The previously discussed communication overhead is actually a well known problem that has recently been drawing more and more attention in the deep learning community \([7], [8], [6], [21]\). But communication overhead is not the only problem preventing DNN scalability: there is an even more severe limitation, which turns out to be a hard theoretical constraint. We illustrate this problem by means of a simple experiment: assuming that the communication in the distributed DNN training was free, one would expect close to linear strong scaling properties. However, figure 4 shows, that this is not the case. Again, scalability stalls after only a few nodes. While it is obvious that it is not possible to split the global batch into local batches \(b < 1\), thus imposing a strict scalability limit at \(n = B\), the limitation induced by the batch size are taking effect even for \(b >> 1\). To allow further investigation of these results, we provide a layer by layer analysis on the computational complexity and scalability of out benchmark networks.

\(^2\)Some CPU experiments used the latest DNN extensions of the MKL17 library which provides special purpose functions for the fast implementation of several layer types like cuDNN for CUDA.

\(^3\)See table II for details.

\(^4\)See table II.
A. Layer by Layer Analysis

Figure 5 shows the analysis for DNN training on CPUs. The dominance of the Local Response Normalization layer (LRN) is caused by a rather poor multi-threaded implementation in Caffe and is neglectable in terms of scalability (as shown in figure 5). More interesting is the growing portion of compute time spend in the InnerProduct (= Fully-Connected) layer. Figure 6 shows the same tendencies for layer computations on GPUs, where the LRN layer has no significant impact. Yet another interesting observation can be made in figure 5 which shows the impact of the convolution optimization of the cuDNN library used in figure 6. Even more evident than the relative compute portions of the different layer types shown in figures 5, 6, 15 and 14 are the scaling properties by the different layer types. Figure 5 depicts these for DNN training on CPUs (see figure 14 for results on the new Xeon-Phi): all but one layer types show almost perfect linear scaling. Only the significantly compute intensive InnerProduct layer scales poorly for batch sizes \( b < 64 \), which is equivalent to scaling to only \( n > 4 \) nodes for the original batch size \( B = 256 \). On the GPU, the crucial InnerProduct layer scales much better than on the CPU, but still fails linear speedup as we can see accelerations factors around 32x at 256 nodes. Again, the speedup stalls for batch sizes \( b \leq 32 \).
Fig. 7. Speedup achieved by reducing the batch size - computed from the results in Fig. 5. Top: results for AlexNet. Bottom: results for GoogLeNet.

Layer | # operations | matrix sizes  
--- | --- | ---  
Fully Connected | 1 | $b \times I \times I \times O$  
Convolutional | $b$ | $C \times I \times I \times Z$  
Softmax | $b$ | $I \times 1 \times 1 \times 1$  

Definitions:

I: Input size from top layer  
O: Output size of this layer  
b: local Batch size (train or validation)  
c: Number of filters  
P: Patch size (i.e. pixel)  
k: kernel size  
Z: Effective size after kernel application.

For convolution $Z := \left(\sqrt{P} - \lfloor k/2 \rfloor\right)^2$

### TABLE III

| Layer          | # operations | matrix sizes  
|----------------|--------------|---------------  
| Convolutional  | $b$          | $C \times I \times I \times Z$  
| Softmax        | $b$          | $I \times 1 \times 1 \times 1$  

FC layers perform a single\(^7\) matrix multiplication per pass. Table [III] shows the impact of the batch size $b$ on the size, shape and number of matrix multiplications. While $b$ only affects the number of matrix operations for Convolutional layers (which can implemented task-parallel \(^1\)), it directly reshapes the left-hand matrix in the FC sgemm operation in a very unfavorable way. For typically large $I$ and $O$ (e.g. for a layer in AlexNet we find $I = 4096, O = 9192$), $b = B/n$ decreases from $B = 256$ - producing “degenerated” (maximal non-square) matrices. This “degeneration” hurts the Inner Parallelization of the matrix multiplication (see section I-A1), where the sgemm is either multi-threaded by the MKL Blas Library or parallelized via cudaBlas. Both implementations have an optimal performance for square matrices and suffer from the “degeneration” \(^5\). Hence, speedups gained by the Outer Parallelization (the data-parallel SGD) start to harm the performance of Inner Parallelizations and cause a “scalability deadlock”. Figure [9] shows the impact of $b$ on the MKL sgemm speedup performance. It is not surprising, that this evaluation shows exactly the same speedup characteristic as the overall communication free scaling experiment in fig. [4].

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\(^7\)The changing name convention is due to the naming used in Caffe.  
\(^8\)The optimization strategy is also available in MKL17, as shown in figure [11].
Fig. 9. MKL SGEMM: impact of the batch size \( b \) on the MKL sgemm speedup performance for matrix multiplications with the shape \( b \times 4096 \times 4096 \times 9192 \). These matrix shapes correspond to the sgemms computed in the largest Fully-Connected layer of AlexNet.

C. Increasing the global Batch Size

A simple way to overcome the stalling scalability beyond 8 nodes (or \( b < 32 \)), has recently been suggested in \cite{7} and is also utilized in \cite{1}: increasing the global batch size \( B \) to the extend, that the worker batch size keeps an effective size \( b \geq 32 \) for the Inner Parallelization.

Figure \ref{fig:11} shows, that this strategy is actually providing almost perfect linear speedup up to 128 nodes for a global batch size of 4096. However, these results have to be taken with strong caution: Increasing the global batch size also increases the computational complexity of the problem linearly. Beyond a certain batch size, SGD will not converge significantly faster in terms of the number of iterations. Hence, large batch sizes will increase the computation time per iteration while the number of iterations stays constant. In order to reduce the number of iterations till convergence, one would have to increase the step size as well. The authors of \cite{7} argue, that larger batch sizes will provide more stable gradient information which should allow larger step sizes. If it was possible to increase the step size in the same way this is done with the batch size, one would yield perfect linear scaling.

Sadly, this is hardly the case. Figure \ref{fig:10} shows the accuracy plots for AlexNet, computed till full convergence with differently large global batch sizes. The experiments were performed on a single KNL node to avoid possible interferences in a distributed setting\footnote{The KNL provides enough memory for such large batch sizes. On common GPUs with 12GB memory, the batch size limit is \( b = 256 \) for AlexNet and \( b = 128 \) for GoogLeNet.}. The step sizes \( \epsilon \) were increased according to the batch size as suggested by \cite{7}, while the number of iterations has been decreased by the same factor. The results are quite disappointing: while we reach linear speedup as expected, the validation accuracy is suffering significantly: These experimental results confirm the theoretic analysis by \cite{11}, who showed that large batch sizes lead to sharp minima with poorer generalization properties. Considering, that an early stopping of the original problem when reaching the according error rates yields almost the same speedup as the parallelized large batch variants, shows that this approach might not be suitable to solve the scaling problem of the matrix multiplications.

\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|c|}
\hline
batch size & speedup & step-size & accuracy \\
\hline
256 & 1 & \( \epsilon = 0.01 \) & 57.2\% \\
512 & 2 & \( \epsilon = 0.02 \) & 56.4\% \\
1024 & 4 & \( \epsilon = 0.04 \) & 54.7\% \\
2048 & 8 & \( \epsilon = 0.08 \) & 52.2\% \\
\hline
\end{tabular}
\caption{Effect of choosing larger step-sizes \( \epsilon \) on the resulting test/validation accuracy. Our experiments show, that larger batch sizes can not compensate for the loss in accuracy.}
\end{table}
D. Non-Scaling Layers

Figure 8 also shows very poor scalability for some layers like Dropout, Pooling or LRN. This is mostly due to the fact that these layers are computed so fast, that the latency of loading the data to the GPU becomes the dominant constant factor. Overall, these particular layers consume only a marginal portion of the total compute time (0.1% for AlexNet and 0.3% for GoogLeNet, assuming that all other layers are parallelizable). Applying Amdahl’s Law shows in figure 12 that this still affects the scalability in the long run. Again, scalability begins to stall at \( n > 32 \).
namely the communication overhead, parallelization of matrix operations and training data distribution which need to be solved in order to achieve a sustainably scalable solution which should allow strong scaling to thousands of nodes. Currently, effective scaling is not possible beyond 16 nodes.

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APPENDIX

Fig. 14. Additional layer by layer results for the KNL (see section III-A for details). Top: Proportional compute times by layer type and batch size for AlexNet. Bottom: Speedups by layer type and batch size for AlexNet.

Fig. 15. Layer by layer analysis for GoogLeNet without cuDNN.