ABSTRACT

High Level Synthesis (HLS) tools, like the Intel FPGA SDK for OpenCL, improve design productivity and enable efficient design space exploration guided by simple program directives (pragmas), but may sometimes miss important optimizations necessary for high performance. In this paper, we present a study of the tradeoffs in HLS optimizations, and the potential of a modern HLS tool in automatically optimizing an application. We perform the study on a 5-stage camera ISP pipeline using the Intel FPGA SDK for OpenCL and an Arria 10 FPGA Dev Kit. We show that automatic optimizations in the HLS tool are valuable, achieving a up to 2.7× speedup over equivalent CPU execution. With further hand tuning, however, we can achieve up to 36.5× speedup over CPU. We draw several specific lessons about the effectiveness of automatic optimizations guided by simple directives, and the nature of manual rewriting required for high performance.

1 INTRODUCTION

In recent years, High-Level Synthesis (HLS) has gained a lot of traction in the accelerator design community as a faster means of designing high-performance accelerators on Field Programmable Gate Arrays (FPGAs) and Application Specific Integrated Circuits (ASICs) [1–4, 8–10, 12, 15, 19, 27, 30]. With the right optimizations and tuning, HLS allows designers to reach the same end goal as Hardware Descriptive Languages (HDLs) like Verilog and VHDL, in a fraction of the design time with minimal loss of performance. In fact, recent literature has been showing a wide adoption of HLS in designing accelerators for new applications in a multitude of domains [5, 17, 28].

A successful example of an HLS system is AOC, the Intel FPGA SDK for OpenCL [2]. AOC allows designers to use OpenCL for designing their accelerator while targeting Intel’s family of FPGAs. However, getting good performance with AOC is non-trivial, requiring extensive tuning. Intel has released two supporting documents, a Programming Guide [14] and a Best Practices Guide [13] to provide designers with optimization techniques for achieving the best possible performance with AOC. In addition, AOC provides two reporting mechanisms: 1) a pre-synthesis Optimization Report that gives the designer a quick estimate of performance, allowing for rapid code modification without having to go through synthesis, and 2) a Profile Report that gives profiling information of the kernel physically running on the FPGA (post synthesis and place-and-route).

However, even with the guidance that Intel provides in its manuals, getting the best performance possible still presents at least three challenges. First, the programmer must often use compiler directives (in the form of pragmas) to provide information that may not be tractable for the compiler to prove automatically, such as for interprocedural pointer aliasing or loop-carried dependences. Second, it is often the case that different optimizations come with different tradeoffs. Navigating the design space of these optimizations requires the programmer to go through many iterations of their designs, many of which need to go through the complete synthesis flow, because the Optimization Report is not always indicative of the actual performance in hardware. Third, and most problematic, some important optimizations may be lacking in the compiler entirely (for a variety of reasons), and programmers may need to make significant manual changes to the code in order to accomplish those optimizations.

In this work, we study the tradeoffs of different optimization techniques, and the potential of automatic directive-driven optimizations in AOC, on a 5-stage Image Signal Processing (ISP) pipeline that takes a raw image produced by camera sensors, and converts it into a viewable image format. Our target device is an Intel Arria 10 GX FPGA Development Kit which carries a GX 1150 FPGA. We show through our study that while some optimizations have clear-cut benefits and always yield improvements, others behave differently depending on the kernel being optimized. We also show that the amount of performance improvement that can be achieved automatically by the compiler, with only simple directives and minimal code modifications, is useful but limited, and that, in most cases, achieving the best performance requires significant modifications to the code.

In order to perform our study, we implemented the stages of the ISP pipeline as separate kernels in OpenCL using the Intel-recommended single work item model. Next, we used the pre-synthesis Optimization Report to choose different optimizations from Intel’s Best Practices Guide that would help us achieve perfect pipelining of the outer loops in the kernels. We profiled the resulting design and found that significant performance improvements were possible but not achievable using automated optimizations implemented in the compiler (even with programmer directives), and therefore required further hand-tuned optimization of the kernels. While some of these optimizations are described in the Best Practices Guide (like buffering of inputs), a very important transformation (similar to unroll-and-jam [6]) is not. We performed both kinds of optimizations through manual hand-tuning of the code.
Our final results show that for the full pipeline, automatic optimizations give a 3.3× slowdown, while hand tuning the kernels gives us up to 4.6× speedup compared to CPU execution. Looking at individual kernel performance, we find that automatic optimizations can achieve up to 2.72× speedup, while hand tuning the kernels allows us to achieve close to 36.5× speedup compared to CPU.

In our study, we treated the 5 stages of the ISP pipeline as distinct kernels, each exhibiting its own characteristics, to try and identify patterns in the effect of the optimization techniques that we apply. Through comparing the behaviors of the 5 kernels, we were able to learn the following lessons:

1. Our most important finding is that automatic optimizations that are performed by AOC, even those guided by directives, are not sufficient to achieve the best performance possible without extensive manual modifications by the designer.
2. In spite of the above limitation, using ‘restrict’ and ‘ivdep’ keywords almost always provide a decent boost in performance by allowing AOC to avoid memory dependence assumptions.
3. Rewriting the kernels to increase the amount of independent operations within the body of a pipelined outerloop provides significant performance benefits by increasing spatial parallelism.
4. If read-only data fits on the FPGA, manually buffering the data gives better performance than depending on AOC’s constant memory, in all but one case, since it removes the overhead of the cache structure.
5. Finally, if inner loops are present in the body of the pipelined loop, even partially unrolling them gives a boost in performance since it increases the amount of parallel operations.

By performing this study, we identified the limitations of automatic optimization in a modern commercial HLS tool like AOC, which motivates the need for more extensive compiler optimizations in these tools. This is an area of research that we are interested in and are pursuing as future work.

The rest of the paper is organized as follows: Section 2 provides a background about the ISP pipeline and the Intel FPGA SDK for OpenCL, followed by the details of how the optimizations we used, and how we applied them to each kernel in Section 3. Next, Section 4 provides our experimental evaluation, followed by some of the related work in Section 5, after which we conclude in Section 6.

2 BACKGROUND

2.1 The 5-Stage Camera ISP Pipeline

To perform our case study, we use the 5-stage Camera ISP pipeline that is shown in Figure 1 [26]. It takes in a raw image that is produced by camera sensors, and generates a useful image that can be displayed. The main stages of the pipeline are described below:

Demosaic: This stage applies a Bayer Filter color filter array on each raw pixel to interpolate it’s true R-G-B values. It produces a mosaic of RGB pixel intensities. [21]

Denoise: This stage applies a local nonlinear interpolation denoising algorithm to reduce the level of noise in the image. [24]

Color Space Transform / White Balancing: This stage performs color balancing by multiplying the RGB color value at each point with a 3x3 diagonal matrix whose values are configurable. It preserves the neutrality of neutral colors. [22]

Gamut Mapping: This stage maps the colors of the original image to a set of restricted available colors of an output device without compromising the original image. To do so, it first computes the L2-norm from each pixel to the set of control points that represent the target gamut. Then, the L2 distances are weighted and summed. Finally, a bias is added to implement a radial basis function. This is the most computationally-intensive kernel and serves as the bottleneck for the pipeline. [23]

Tone Mapping: This stage approximates images with a higher dynamic range than the output device. This is done by using a Tone Map Operator to squeeze the original dynamic range of the image into the lower range of the output device. [25]

Profile of the pipeline: The execution time breakdown of the pipeline is as follows: 99% in Gamut Map, 0.8% in Denoise, 0.04% in Transform, 0.03% in Demosaic, and 0.02% in Tone Map. Therefore, we can see that Gamut Map significantly outweighs all the other kernels, and we focus our efforts on achieving the best speedup for this kernel, while still studying the tradeoffs in applying different optimizations on the other kernels.

2.2 Intel FPGA SDK for OpenCL

The Intel FPGA SDK for OpenCL is an HLS tool that allows hardware designers to use OpenCL, instead of HDLs, for programming Intel FPGAs. The main tool in the SDK is the Altera OpenCL Compiler (AOC), an HLS compiler that compiles the OpenCL kernels into RTL, then runs them through Intel Quartus to synthesize them and generate an FPGA bitstream. AOC’s strong suit is in automatically pipelining loops in a kernel and trying to achieve perfect pipelining with an initiation interval (II) equal to 1. As such, it is recommended that designers implement their kernels as Single Work Item Kernels (SWIK), as opposed to the traditional multithreaded kernels that OpenCL is known for, in order to maximize AOC’s ability to pipeline the kernel’s execution, and extract as much parallelism as possible. To facilitate the process of optimizing kernels using Intel’s OpenCL SDK, AOC provides three key resources: 1) An Optimization Report, which can be generated through a quick intermediate compilation step, that contains information about estimated resource utilization and the status of all the loops (unrolled, pipelined – along with the estimated II). 2) A Profile Report, which requires a full synthesis and place-and-route to be completed, and provides profiling information related to the kernel performance (operating frequency, execution time, memory bandwidth, etc...). 3) A Best Practices Guide, which is a document that provides different optimization techniques to assist the designer in selecting optimization decisions based on the results of the optimization and profiling reports. Next, we will describe the main information that is reported by the Optimization Report and Profiling Report.

Understanding the Optimization Report: The Optimization Report provides an analysis of the loops in the kernel, identifying which loops were unrolled, and which were pipelined along with their corresponding II. If the II > 1, the report provides an explanation of what might be the bottlenecks that prevented perfect pipelining of the loops, along with pointers to the corresponding sections in the Intel guides that might provide techniques to improve the
II. In addition to loop information, the report provides a "System Viewer". This viewer shows the basic blocks of the kernel and provides information about the start cycle, end cycle, and latency of each basic block, along with the structure of local memories.

*Understanding the Profile Report:* The Profile Report is an essential tool for understanding the performance of the generated kernel. It provides the total execution time of the kernel, the operating frequency, and the global bandwidth to DRAM. It also provides details about each load and store in the kernel.

3 OPTIMIZING THE ISP PIPELINE

In this section, we will first describe our baseline implementation of the pipeline, followed by a description of the different optimizations that we applied along with our optimization strategy.

3.1 Baseline

For our baseline, we use a simple 'single work item' OpenCL implementation that is a direct mapping of the original C implementation of the pipeline into OpenCL. In this implementation, all arrays are stored in OpenCL global memory (FPGA on-board memory), and kernels communicate through global memory as well – each kernel writes its output to global memory, which is then read by the next kernel. Our pipeline implementation operates on images with three channels (‘R’, ‘G’, and ‘B’). Images are stored in memory in row-major order such that all the rows of the ‘R’ channel come first, followed by the rows of the ‘G’ channel, which are then followed by the rows of the ‘B’ channel. In the baseline implementation, all the kernels, except Demosaic, operate on the 3 channels sequentially, and produce all the pixels of ‘R’ followed by ‘G’, then ‘B’.

3.2 Automatic Optimizations

Some of the optimization techniques that are provided by Intel’s guides, and that we use in this study, require minimal code modifications in the form of directives, and rely on the compiler to automatically optimize the kernel based on the information that these directives provide. We will now describe the three optimizations that we use:

- The "restrict" keyword: Is an attribute that can be used to mark the different pointer operands of a kernel as non-aliasing. This allows AOC to avoid making conservative assumptions about whether or not the operands may alias.
- The "inline" pragma: Is a directive that can be used to instruct AOC to ignore any assumed loop-carried dependecies that enforce serialization of loop iterations, thus limiting the ability of AOC to pipeline the loops.
- The “constant” attribute: This attribute can be added to pointer operands of the kernel that are read-only. It instructs AOC to cache accesses to these operands in a global Constant Memory Cache that it creates using the FPGA Block RAM. A single constant cache of configurable size – the default of which is 16KB – is shared among all the ‘constant’ operands of all the kernels that would be running on the FPGA at the same time.
- The "unroll" pragma: Is a directive that can be used to instruct AOC to attempt unrolling a loop. A specific unroll factor can be specified, otherwise AOC attempts to fully unroll the loop. If done on an inner loop of a pipelined outerloop, it gives AOC the potential to increase spatial parallelism by having more parallel computations to perform per iteration.

3.3 Manual Optimizations

In addition to the automatic optimization techniques, Intel’s guides recommend other optimizations that require significant code modifications, thus relying more heavily on the designer. We also combine this category other hand-tuned optimizations that are not specifically recommended by Intel, but rather stem from the natural design considerations of spatial parallelism on the FPGA. The following describe the manual optimizations that we use in our study:

- Using local memory when possible: This represents a set of optimizations recommended by Intel that involve moving computation to local memory when possible. These techniques include copying read-only kernel inputs that possess temporal locality from global to local memory, and privatizing any kernel operands that are only generated and accessed in the kernel.
- Manual loop modifications: There are scenarios where loop nests could be rewritten with a combination of unrolling, interchange, and fusion in order to maximize the amount of spatial parallelism by exposing more independent computations per iteration of a pipelined loop. We perform a variety of these optimizations as described Section 3.4 below.
- Using Intel Channels: Intel Channels are FIFO buffers that can be used to transfer data between kernels. This can be useful when multiple kernels are running on the FPGA at the same time, and they exhibit a producer-consumer behavior. By using channels, all the data can be transferred between the kernels locally on the FPGA without having to write to/read from global memory. In many cases, using channels require modifications to the kernel code to make sure that the memory access pattern of the producer and consumer match.
3.4 Optimization Strategy

Starting with the baseline from Section 3.1, we performed different combinations of the optimizations that we discussed in Sections 3.2 and 3.3 on each kernel. We carefully chose optimizations to apply based on the results of the AOC Optimization Report and the Profile Report. We break down our study of the optimizations into four steps:

1. First, we apply the ‘restrict’ and ‘ivdep’ keywords, to achieve perfect pipelining of the outer loop, and study the extent of which AOC can automatically optimize the kernels with these keywords in place.

2. Next, we apply manual rewrites to the code, such that each kernel generates the corresponding pixel of the ‘R’, ‘G’, and ‘B’ channels in the same iteration as opposed to generating them sequentially. This step involves a combination of loop unrolling, loop interchange, and loop fusion. By performing this step, we are increasing the amount of parallel computations in a single iteration of the outerloop, which in turn should allow AOC to exploit the spatial parallelism that is available.

3. After that, we try to further optimize the kernels by optimizing the memory accesses. In this step, we study the effects of using ‘constant’ memory versus manually buffering for all the read-only inputs of each kernel that demonstrate temporal locality.

4. Finally, we use the ‘unroll’ pragma on any inner loops to increase the spatial parallelism that can be exploited in each iteration, and as such further improve the performance.

Once we have the fully optimized version of each kernel, we make an additional modification for the full pipeline, where we use Intel Channels to pass data between the kernels on-chip rather than using global memory. We use this to study the effect of channels on our pipeline. We also study two other versions of the full pipeline, one having the best performing version of each kernel, and one having the best performing version of each kernel using only the automatic optimizations that we described in Section 3.2 above.

We will now describe how each kernel in the pipeline was optimized.

3.4.1 Demosaic: This kernel has a doubly-nested loop that goes over the rows and columns of the image and calculates the ‘R’, ‘G’, and ‘B’ values of each pixel, while reading the input from global memory, and writing the output to global memory. As such, we only apply step 1 from our optimization strategy to it, since it does not have read-only operands, and it cannot benefit from rewrites.

3.4.2 Denoise: This kernel has a triply-nested loop that iterates over the image channels, rows, and columns. For each input pixel (which is coming from the output of the previous kernel), it reads a 3x3 tile centered around that pixel, sorts the values, and sets the corresponding output pixel to the median of the sorted values. Optimizing the sorting algorithm is beyond the scope of this paper; as such, we can only apply steps 1 and 2 from our strategy to this kernel.

3.4.3 Color Space Transform: This kernel loops over the channels, rows, and columns of the image, and for each output pixel it reads the ‘R’, ‘G’, and ‘B’ values of input pixel, multiplies them by a column from a 3x3 matrix (one column for each channel), and sums up the products. The 3x3 matrix is a read-only input, as such we apply steps 1, 2, and 3 from our strategy to this kernel. We will refer to this kernel as Transform in the rest of the paper.

3.4.4 Gamut Map: For each input pixel, the Gamut Map kernel calculates the L2 distance between the ‘R’, ‘G’, and ‘B’ values of that pixel and each control point. Then, the L2 distances are weighted and summed. Finally, a bias is added to that sum by multiplying each ‘R’, ‘G’, and ‘B’ value with a coefficient and adding them up. The final result is the corresponding output pixel. As such, the Gamut Map kernel is the most computationally intensive kernel in the pipeline. Given that the L2 distance calculation is performed in an innermost loop, we apply all 4 steps of our strategy to this kernel.

3.4.5 Tone Map: The Tone Map kernel reads each input pixel, uses its value to access a tone_map matrix, and sets the corresponding value from the matrix as the output pixel value. Given that this kernel has a read-only input and potential for rewrite, we apply steps 1, 2, and 3 from our strategy to it.

4 EXPERIMENTAL EVALUATION

In this section, we start by presenting our evaluation methodology. Next we present the results of the full pipeline, which as an overview of the optimizations. Finally, we show the results of optimizing each kernel separately, to highlight the effect of each optimization.

4.1 Methodology

Our software infrastructure consists of the Intel FPGA SDK for OpenCL version 18.1 (along with Quartus Pro 18.1) running on Ubuntu 16.04 LTS. Our target device is an Intel Arria 10 GX FPGA Development Kit which houses an Arria 10 GX1150 FPGA. Our CPU implementation is single-threaded running on an Intel Xeon E3-1240 V2 @ 3.40GHz. The operating frequency of the kernels on the FPGA ranges between 210MHz and 360MHz.
We synthesized different versions of each kernel, and of the entire pipeline, according to our optimization strategy described in Section 3. We tested the execution with multiple different input images of the same size, and confirmed that the results are similar. As such, we present the results for a single image, averaged over 10 runs.

4.2 Full Pipeline Result
In this section, we provide an overview of the performance of the full pipeline, before diving into the different steps of our optimization strategy and analyzing each kernel separately. Figure 2 (a) presents the execution time for the different versions of the full pipeline, normalized to CPU. Two versions were tested: Best: has the best performing version of each kernel constituting the pipeline; Auto: has the best performing version of each kernel, with automatic optimizations only (as described in Section 3.2), constituting the pipeline. Note that since the Baseline described in Section 3 is very unoptimal, we do not use it as a comparison point in the overall performance study of the pipeline. The results in the graph clearly show that there is a big gap in the overall performance benefits of automatic optimizations that can be performed by a tool like AOC (3.3x slowdown over CPU), and the best performance possible using manual modifications of the code (21x speedup over CPU).

We also study the effects of channels on the pipeline (Figure 2 (b)). We compare two versions against the best case from Figure 2 (a), one that uses constant memory with channels (C.CH) and another that uses manual buffering with channels (B.CH). We see that in our application Intel channels do not provide us with much more speedup compared to the best version of each kernel that uses global memory. The reason behind that is the imbalance between the kernels of the pipeline, which in this case causes increased stalling where the consumers are waiting on the producers to generate the data. We also show that manual buffering of the data gives better performance than using constant memory. This is due to the overhead in accessing the cache structure that is generated for constant memory compared to accessing the local memory that would be used for buffering.

4.3 Single Kernel Results
As discussed in Section 3, our optimization strategy involves four steps, applied incrementally to the baseline. We discuss the analysis of our strategy, one step at a time, in this section.

4.3.1 Step 1: This step studies the effect of the ‘restrict’ (R) and ‘ivdep’ (I) keywords on each kernel. Figure 3 shows the three versions (R, I, and RI) compared to baseline and CPU. Although we also applied this step to Gamut Map, we do not show any results because these three versions of Gamut Map did not fit on our FPGA, and therefore we were not able to gather results for them. Our results show that there is always benefit in adding the two keywords, which is expected since this allows AOC to avoid making any assumptions related to memory aliasing and inter-loop memory dependence, thus allowing it to parallelize memory accesses to the fullest. Although RI isn’t always the best-performing version, we chose it as the version to build on in our next steps in order to maintain uniformity across all kernels. We also believe that R and I together will be beneficial for AOC to exploit more memory parallelism when we apply further optimizations.

4.3.2 Step 2: This step studies the effect of performing manual code modifications on top of RI, these include a combination of loop unrolling, interchange, and fusion, in order to increase the amount of parallel operations that can be scheduled in one iteration of the pipelined outerloop (as described in Section 3.3 above). Our results are presented in Figure 4, where W corresponds to manual rewrites. The results show that manual code modifications are crucial, as they can provide huge performance benefits (2.16x-3.34x speedup vs RI) because of their ability to extract more independent operations per outerloop iteration, which can be spatially parallelized. Note that this optimization cannot be applied to Demosaic due to the nature of the kernel. Also, Gamut Map’s version of RIW does not fit on our FPGA.

4.3.3 Step 3: This step studies the effect of further optimizing accesses to read-only memory after performing manual code modifications. This can either be done using constant memory (C) or manual buffering of the data in local memory (B). Figure 5 and Figure 6 present the results for applying C and B on top of RIW. For Tone Map, our read only-data is larger and less frequently accessed, thus we believe that the overhead of the constant memory cache accesses slightly hurt performance. We also see that RIW performs slightly better than using either C or B, which we found is due to the fact that AOC was able to schedule it at a faster frequency compared to the other two. Another interesting observation is that with C and B added, the Gamut Map kernel now fits in our FPGA. We added an extra configuration to Gamut Map (.128), which corresponds to manually configuring the size of the constant cache to 128KB, instead of the default 16KB, since the amount of read-only data accessed by this kernel is closer to 128KB (cache size can only be set to a power of 2). We see that by moving from a cache size that is smaller than the data set, to one that allows the data set to fit, greatly improves performance (~6x speedup vs ~2x slowdown, when compared to CPU). We also see that, although they are close, using buffering is slightly better than using constant memory. Finally, for Transform, the amount of read-only memory is small enough (9 floats), and the variation in the execution time is small enough, making the effect of C vs B negligible to the bigger picture. Therefore, the results show that it is almost always better to use buffering instead of constant memory when the data can fit on the FPGA, especially when the amount of data being accessed is significant.

4.3.4 Step 4: In addition to all the above optimizations, we perform an extra step for Gamut Map, which is unrolling its inner loop by a factor of 6. This optimization is not possible for the other kernels since they do not possess such an inner loop. We see in Figure 6 that by unrolling, we further improve the performance compared to buffering and using constant memory (~36x vs CPU with unrolling, ~6x without). This is expected, since by unrolling the inner loop we are increasing the amount of independent operations that can benefit from the spatial parallelism on the FPGA.
5 RELATED WORK

One recent work that also analyzes AOC is presented in [20]. In this work the authors build an analysis framework for modeling the effects of different AOC optimization techniques. Their goal is to provide a tool for designers to be able to analyze the performance effects of difference AOC optimizations on their code. However, their work does not focus on determining the potential of AOC’s automatic optimizations. Their work is that they focus on the multi-threaded execution model of AOC, rather than the Single Work Item model that we focus our study on because it is recommended by Intel to allow AOC to perform more automatic optimizations. Given that the multi-threaded model of AOC depends on the programmer to manually express the parallelism, most of the optimizations there require manual hand-tuning.

There are recent surveys that focus on comparing HLS tools [7, 18]. These surveys provide a description of the abilities of different HLS tools, and compare ability of these tools in generating high-performing FPGA designs. However, they do not highlight what is possible with automatic optimizations in the different tools, versus what requires extensive hand-tuning.

Multiple academic papers present new HLS tool flows that can perform better automatic optimizations than AOC [8, 9, 11, 16, 29, 30]. However, these papers do not specifically study the potential of automatic optimizations in AOC (or other commercial tools) compared to non-automatic optimizations. Instead, they show an overall improvement in generated code quality, and design efficiency. In addition, some of them are domain-specific targeting specific [12, 15, 19]. We focus on evaluating automating optimizations, and use AOC as a leading example of a commercial HLS tool that provides such optimizations.

6 CONCLUSION

In this paper, we presented a study of the automatic optimization potential of the AOC compiler, and the tradeoffs in using different optimization techniques. We show that there is limited potential in
automatic optimizations that AOC can perform, even driven with programmer directives (2.8× speedup vs. CPU in the best case), and that great performance benefits can be achieved by combining them with other optimizations that require manual hand-tuning of code (36.5× speedup vs. CPU). This motivates the need for more extensive compiler optimizations in commercial HLS tools, an area of research that we are interested in. We also show that different optimizations have different effects on different kernels, and that while some have clear-cut effects, others depend on the behavior of the kernel.

REFERENCES

[1] 2018. SDAccel Development Environment. https://www.xilinx.com/products/design-tools/software-zone/acceldev.html. (2018). Accessed: Sept 16, 2019.
[2] 2019. Intel FPGA SDK for OpenCL. https://www.altera.com/products/design-software/embedded-software-developers/opencv-overview.html. (2019). Accessed: Sept 16, 2019.
[3] 2019. MaxCompiler. https://www.maxeler.com/products/software/maxcompiler/. (2019). Accessed: Sept 16, 2019.
[4] 2019. Vivado High-Level Synthesis. https://www.xilinx.com/products/design-tools/vivado/integration/ml-design.html. (2019). Accessed: Sept 16, 2019.
[5] Jakub Cabal, Pavel Benaček, Lukáš Keckely, Michal Keckely, Viktor Půl, and Jan Kotenek. 2018. Configurable FPGA Packet Parser for Terabit Networks with Guaranteed Wire-Speed Throughput. In Proceedings of the 2018 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA ’18). ACM, New York, NY, USA, 249–258. https://doi.org/10.1145/3174243.3174250
[6] David Callahan, John Cocke, and Ken Kennedy. 1988. Estimating interlock and improving balance for pipelined architectures. J. Parallel Distrib. Comput. 5, 4 (1988), 334–358.
[7] Keith Campbell, Wei Zuo, and Deming Chen. 2017. New advances of high-level synthesis for efficient and reliable hardware design. Integration, the VLSI Journal 58 (2017), 189–214.
[8] Andrew Canis, Jongsoo Choi, Mark Aldham, Victor Zhang, Ahmed Kammoona, Jason H Anderson, Stephen Brown, and Tomasz Czajkowski. 2011. LegUp: high-level synthesis for FPGA-based processor/accelerator systems. In Proceedings of the 19th ACM/SIGDA international symposium on Field programmable gate arrays. ACM, 33–36.
[9] Andrew Canis, Jongsoo Choi, Mark Aldham, Victor Zhang, Ahmed Kammoona, Tomasz Czajkowski, Stephen D Brown, and Jason H Anderson. 2013. LegUp: An open-source high-level synthesis tool for FPGA-based processor/accelerator systems. ACM Transactions on Embedded Computing Systems (TECS) 13, 2 (2013), 24.
[10] Tomasz S Czajkowski, Utku Aydonat, Dmitry Denisenko, John Freeman, Michael Kistner, David Neto, Jason Wong, Peter Tiemanncouas, and Deshanand P Singh. 2012. From OpenCL to high-performance hardware on FPGAs. In Field Programmable Logic and Applications (FPL), 2012 22nd International Conference on. IEEE, 531–534.
[11] Sumit Gupta, Rajesh Kumar Gupta, Nikil D Dutt, and Alexandru Nicolau. 2004. Coordinated parallelizing compiler optimizations and high-level synthesis. ACM Transactions on Design Automation of Electronic Systems (TODAES) 9, 4 (2004), 441–470.
[12] James Hegarty, John Brunhaver, Zachary DeVito, Jonathan Ragan-Kelley, Noy Cohen, Steven Bell, Artem Vasilyev, Mark Horowitz, and Pat Hanrahan. 2014. Darkroom: compiling high-level image processing code into hardware pipelines. ACM Trans. Graph. 33, 4 (2014), 144–1.
[13] Intel 2018. Intel FPGA SDK for OpenCL. Pro Edition Best Practices Guide. Intel.
[14] Intel 2018. Intel FPGA SDK for OpenCL. Pro Edition Programming Guide. Intel.
[15] David Koeplinger, Matthew Feldman, Raghu Prabhakar, Yaqi Zhang, Stefan Hadiis, Ruben Fizel, Tian Zhao, Luigi Nardi, Ardavan Pedram, Christos Kozarakis, et al. 2018. Spatial: a language and compiler for application accelerators. In Proceedings of the 39th ACM SIGPLAN Conference on Programming Language Design and Implementation. ACM, 296–311.
[16] Seyoung Lee, Jungwon Kim, and Jeffrey S Vetter. 2016. Openacc to fpga: A framework for directive-based high-performance reconfigurable computing. In Parallel and Distributed Processing Symposium, 2016 IEEE International. IEEE, 544–554.
[17] Hiroki Nakahara, Haruyoshi Yonekawa, Tomyo Fujii, and Shimpei Sato. 2018. A lightweight yolov2: A binarized cnn with a parallel support vector regression for an fpga. In Proceedings of the 2018 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays. ACM, 31–40.
[18] Razvan Nane, Vlad-Mihai Sima, Christian Piatel, Jongsoo Choi, Blair Fort, Andrew Canis, Yu Ting Chen, Hsuan Hsiao, Stephen Brown, Fabrizio Ferrandi, et al. 2016. A survey and evaluation of FPGA high-level synthesis tools. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 35, 10 (2016), 1591–1604.
[19] Jing Pu, Steven Bell, Xuan Yang, Jeff Setter, Stephen Richardson, Jonathan Ragan-Kelley, and Mark Horowitz. 2017. Programming heterogeneous systems from an image processing DSL. ACM Transactions on Architecture and Code Optimization (TACO) 14, 3 (2017), 26.
[20] Zeke Wang, Bingheng He, Wei Zhang, and Shuming Jiang. 2016. A performance analysis framework for optimizing OpenCL applications on FPGAs. In 2016 IEEE International Symposium on High Performance Computer Architecture (HPCA). IEEE, 114–125.
[21] Wikipedia contributors. 2019. Bayer filter — Wikipedia, The Free Encyclopedia. (2019). https://en.wikipedia.org/w/index.php?title=Bayer_filter&oldid=915626373 [Online; accessed 17-September-2019].
[22] Wikipedia contributors. 2019. Color balance — Wikipedia, The Free Encyclopedia. https://en.wikipedia.org/w/index.php?title=Color_balance&oldid=91682036. (2019). [Online; accessed 17-September-2019].
[23] Wikipedia contributors. 2019. Color management — Wikipedia, The Free Encyclopedia. https://en.wikipedia.org/w/index.php?title=Color_management&oldid=914472420. (2019). [Online; accessed 17-September-2019].
[24] Wikipedia contributors. 2019. Noise reduction — Wikipedia, The Free Encyclopedia. (2019). https://en.wikipedia.org/w/index.php?title=Noise_reduction&oldid=913799999 [Online; accessed 17-September-2019].
[25] Wikipedia contributors. 2019. Tone mapping — Wikipedia, The Free Encyclopedia. https://en.wikipedia.org/w/index.php?title=Tone_mapping&oldid=914229318. (2019). [Online; accessed 17-September-2019].
[26] Yuan Yao and Saketh Rama. [n. d.]. yaoyuannnnn/cava. ([n. d.]). https://github.com/yaoyuannnnn/cava.
[27] Zhuru Zhang, Yiping Fan, Wei Jiang, Guoling Han, Changyi Yang, and Jason Cong. 2008. AutoPilot: A platform-based ESL synthesis system. In High-Level Synthesis. Springer, 99–112.
[28] Hamid Reza Zohouri, Artur Podobas, and Satoshi Matsuoka. 2018. Combined spatial and temporal blocking for high-performance stencil computation on FPGAs using OpenCL. In Proceedings of the 2018 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays. ACM, 153–162.
[29] Wei Zuo, Peng Li, Deming Chen, Louis-Noël Pouchet, Shuman Zhong, and Jason Cong. 2013. Improving Polyhedral Code Generation for High-level Synthesis. In Proceedings of the Ninth IEEE/ACM/FIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS ’13). IEEE Press, Piscataway, NJ, USA, Article 15, 10 pages. http://dl.acm.org/citation.cfm?id=2555692.2555707
[30] Wei Zuo, Yun Liang, Peng Li, Kyle Rupnow, Deming Chen, and Jason Cong. 2013. Improving high level synthesis optimization opportunity through polyhedral transformations. ACM/SIGDA International Symposium on Field Programmable Gate Arrays - FPGA, 9–18. https://doi.org/10.1145/2435264.2435271