Active feedback supported CMOS LNA blended with coplanar waveguide-fed antenna for Wi-Fi networks

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Abstract
This study presents integration of complementary CMOS active feedback low noise amplifier with coplanar waveguide fed patch antenna for Wi-Fi networks. The LNA design-I, involves a cascode amplifier followed by active feedback common source amplifier offering wideband impedance matching with lowered parasitic losses. The inductor-less feedback mechanism is used to nullify noise effect with extended bandwidth in the range of 2.2 to 5.8 GHz and a peak forward gain of 22.5 dB. It is implemented on agilent’s advance design system using 45 nm CMOS process. The noise figure (NF) is approximately 2 dB while the stability factors \( \mu \) and \( \mu' \) prime are well above 1 dB with IIP3 of about 15 dBm. The chip area is 0.57 x 0.57 mm\(^2\) under dc power supply of 1V while power consumption of 0.8 mW. A CPW fed antenna design-II, achieves a wide band response similar to the bandwidth of LNA. The size of the fabricated antenna is calculated as 40 x 40 mm\(^2\). The peak gain is approximately 4.1 dBi at 3.9 GHz. The codesign-III, proposes a receiver achieving a much wider band of 1.6 to 6 GHz with a gain of 16.5 dB and NF of 2.59 dB at 2.06 GHz. The codesign improves the system integration by reducing overall chip area and offers saving in the effective cost.

1 | INTRODUCTION

The demand and supply rule is applicable in the field of research and technology too. The demands of consumers of technology are fulfilled by the scientists and researchers by supplying the upgrading in technology. In the field of radio frequency (RF) integrated circuit, the researchers have adopted new methods and technology to satisfy the escalating technical hunger of human beings. In wireless communication, the complementary metal oxide semiconductor (CMOS) low noise amplifier (LNA) with integrated antenna has gained ubiquitous reputation to serve as a receiver system. The basic criteria of designing a receiver system are wide bandwidth, high gain, good impedance matching, high reverse isolation, minimal noise with good linearity and stability at the cost of lower power consumption and smallest chip size. Till now, thousands of researchers have tried to achieve the best results, with lots of scope for improvement. Various technologies are adopted to get the optimum results. An LNA must primarily adopt the noise cancellation technique. It has been done by catering a two stage differential LNA offering noise figure (NF) of only 1.7 to 2.7 dB with higher power consumption of 13 mW and low voltage gain of only 16 to 18 dB [1]. For gain consideration, distributed stages have been a trend in the designing of an LNA. In [2], it is also taken into account by having current reuse configuration with double transformer coupling technique. The three common source (CS) stages turn out to be successful in achieving a peak gain of 31.4 dB. But the setback observed is RF inductor coupling that gives unreliable frequency stability. However, the other issues like noise and bulkiness are worth considering. The use of inductor is to be avoided to eliminate its evident drawbacks. Other techniques of noise control incorporates dual cross coupling that brings out NF less than 4.5 dB [3]. Linearity is the other serious issue that needs a proper attention while synthesizing an LNA. Thus, a wide band inductor-less LNA is designed that offers...
high linearity of 10 dBm in terms of third order intercept point (IIP3) attained to be 1 dB with compression point of 0 dBm. The hinder in this approach is the maximum power dissipation of 30.2 mW [4]. In [5], a special technique of parallel push-pull design using CMOS circuit is devised to adhere high noise cancellation and high linearity at the cost of high power consumption of 20.8 mW and low voltage gain of 13 dB in the frequency spectrum of 0.1 to 1.6 GHz. The inductive gain peaking technique popularly adopted choice for noise cancelling and gain flattening, offers the limitation of narrow bandwidth and use of inductor [6]. The other scheme that enhances gain performance with wide band, used a negative capacitance that mitigates the effect of parasitic capacitances [7]. When designing LNA, the use of active inductor omits obvious problems encountered by the conventional inductors [8]. In [9], a multistage LNA is designed using active tunable inductor to offer a reasonably high gain. Although, the active inductor has the potential to be a solution to multiple problems encountered by the conventional one, it needs to be altered. Thus, the much simpler inductor-less technique is used to make the circuit-less complex. In [10], inductor-less LNA with multiple feedback technique is used to achieve the desired parameters along with least power consumption of only 2.8 mW. Another low power inductor-less LNA design used common gate active \( g_m \) boost method, where the power consumed by LNA is even less that is only 1.32 mW [11]. In [12], the inductor-less LNA is designed using active shunt feedback technology. It offers the same band as that of [4] with a maximum gain of 12.3 dB and IIP3 of -10 dBm. In another low power active shunt feedback approach of an LNA, a much wider band of interest of 2 to 8 GHz has been attained with the little compromise in power gain [13]. Another approach of current reuse feed forward noise cancellation offers the minimum power consumption [14]. In one more design of current reuse, the concept of inductor-less LNA is incorporated with an active feedback network (AFB), where the maximum voltage gain of 21.1 dB and IIP3 of 4.7 dBm are attained [15]. Not only this but the inductor-less technology is being adapted to a huge extent such that even the transconductance \( g_m \) boost and noise cancelling techniques exploit it [16]. An LNA design uses a cascode amplifier followed by active feedback inductor-less CS amplifier to lower the parasitic losses and achieve wide impedance matching. The tunable AFB is exploited to yield the well-defined outcomes while being active it offers significant amount of gain. The bandwidth achieved is 3.6 GHz ranging from 2.2 GHz to 5.8 GHz. The coplanar waveguide (CPW) fed antenna is designed to achieve wide band response similar to that of LNA. The peak gain is approximately 4.1 dBi at 3.9 GHz. The codesign receiver system gives a much wider band of 1.6 to 6 GHz, whereas the gain of 16.5 dB is achieved at minimum NF of 2.59 dB at 2.06 GHz. The study is organised as follows: Section 2 describes design and performance of LNA. Section 3 presents antenna design and performance. Section 4 discusses the blending approach of LNA with antenna and finally, Section 5 briefs the conclusion.

2 | LNA DESIGN-I, CONSIDERATION AND PERFORMANCE EVALUATION

A lot of research study has been done in the field of CMOS LNA. The researchers have the constraints to get the optimised performance out of minimal resources used with less complexity. The basic designing idea is to keep the desired results intact with simplified architecture. In the proposed design of LNA, the complete design involves cascading of a cascode amplifier and a single stage CS amplifier along with AFB network. The cascode network shown in Figure 1(a) is widely used to design distributed amplifiers because of its capability to satisfy the gain and resistance properties with good reverse isolation features as compared to a conventional CS amplifier while it does not offer significantly higher \( g_m \). However, the bandwidth is restricted due to the internal capacitive effect of the metal oxide semiconductor (MOS) devices. The frequency response of the cascode network offers a low frequency dominant pole at \( \frac{1}{2 \pi R C} \) where \( R \) is the gate resistance of the transistor and high frequency nondominant pole. The size of CS transistor is used to control the value of the dominant pole [17]. To compensate the parasitic effect, a 100 fF capacitor is connected between the drain of \( M \) and the output of the feedback network. Figure 1(b) depicts the feedback network used to serve multiple purposes including the gain flatness. Here, negative feedback has been exercised to excel the LNA performance. A negative feedback topology caters various benefits to an amplifier behaviour inclusive of bandwidth enhancement, noise reduction, gain stability improvement and impedance matching. It can be practiced by using the traditional passive elements or recently used active devices. Passive networks can be used comprising only of resistive or only reactive elements such as LC networks.

The resistive feedback technique provides a wideband input impedance matching without utilising the extra power in the feedback path and is preferred due to the small die area consumption, whereas the LC tuning feedback networks have their evident limitations but can be used for higher frequency ranges. The inductor-less configurations are preferred as it reduces the chip size, cost and noise factor. Thus considering these issues, the AFBs prove themselves to be better performers at the cost of additional power [12]. The integration of the devices using CMOS technology is a cumbersome process.

![FIGURE 1](image-url) Adopted designs for LNA: (a) cascode cell and (b) CS with feedback network.
since linearity, dynamic range and signal-to-noise ratio are limited by the short channel effect [14]. Thus, the feedback used here not only enhances the expected features but also it significantly contributes to the linearity parameter (IIP3). The feedback is obtained through the combination of complementary derivative superposition and active shunt feedback. The shunt feedback reduces input impedance by a factor of \((1 + A)\), so lower \(g_m\) is used which in turn enables a lower power consumption. Figure 2 shows the complete proposed schematic of LNA. Here \(M_1\) and \(M_2\) form an input stage that is a cascode amplifier which gives high impedance matching due to reverse isolation and good noise factor with a bandwidth about three times the conventional amplifier. The output of this stage is coupled to a CS amplifier \(M_3\) to provide a cascade approach enabling much higher gain. The CS stage is the most widely used LNA, being simple and traditional. It offers high gain and other complementary factors of LNA inclusive of decent bandwidth. Its small channel size yields into downscaling of the chip size. The output of CS stage is fed back into a negative feedback loop where the feedback network is active in nature using MOS devices. This offers all the anticipated benefits of negative feedback in amplifiers along with the gain factor. Transistors \(M_4\) and \(M_5\) form an active network to offer gain and wide band in conjunction with \(M_6\) forming a folded network to behave like a feedback network. Figure 3 shows the impedance bandwidth response of LNA. It is mainly influenced by the capacitive effect of the device. For a cascode amplifier, it is considered to be three times to that of conventional amplifier as it mitigates the Miller effect to limit the bandwidth while for a negative shunt feedback amplifier, it elevates by the factor \((1 + |A_v|)\). The proposed LNA achieved a band that ranges from 2.2 GHz to 5.8 GHz. The bandwidth of a cascode amplifier can be given by Equation (1).

\[
f_1 = \frac{1}{2\pi R_s' \left(C_{gs2} + 2C_{gs2}\right)}
\]

where \(R_s' = R_s \parallel r_m2\) (2)

Also \(C_{gs2}\) is about 20 pF and \(C_{gs1}\) is approximately 1 pF. For a feedback system, it is defined as:

\[
f_2 = f_o (1 + |A_v|)
\]

where \(f_o\) is the bandwidth of the open loop system. More conventionally, it can be put as Equation (4).

\[
f_2 = \frac{1}{2\pi R \left(C_{gs3} + C_1(1 + |A_v|)\right)}
\]

where \(R\) is the output resistance of cascode stage.

The frequency response representation of return loss is approximated by exploiting a two port S-parameter model shown in Figure 4. The incoming and outgoing waves at input and output ports are described by the following equations [18].

\[
a = \frac{1}{2\sqrt{Z_{01}}} (V_1 + I_1 Z_{01})
\]

\[
b = \frac{1}{2\sqrt{Z_{01}}} (V_1 - I_1 Z_{01})
\]

F I G U R E 2  Proposed schematic of LNA

F I G U R E 3  Return loss versus frequency

F I G U R E 4  General two-port representation of S-parameters
where \( Z_{in} \) and \( Z_{out} \) are characteristic impedances of input and output ports. These equations have interlinks to block specific S-parameters in the following manner:

\[
b = S_{11}a + S_{12}c
\]

\[
d = S_{11}a + S_{12}c
\]

The generalised equation of return loss of LNA in terms of input and source impedance is considered from [19].

\[
S_{11} = \frac{Z_{in} - R_s}{Z_{in} + R_s}
\]

The return loss in terms of frequency response is given as:

\[
S_{11} = \frac{S^2 + \omega_i^2}{S^2 + \frac{\omega_i^2}{\omega_0^2} + \omega_i^2}
\]

where \( \omega_i \) and \( Q_i \) are resonance frequency and quality factor, respectively, defined as:

\[
\omega_i = \frac{1}{\sqrt{(R_s + R_f)[C_{gs1} + C_{gd1}(1 + g_m R_f)]}}
\]

\[
Q_i = \frac{1}{2R_s \sqrt{C_{gs1} + C_{gd1}(1 + g_m R_f)}}
\]

Figure 5 depicts the input impedance of LNA with respect to frequency. Total input impedance is affected by all three active stages of the device which include a cascode stage, gain cell, and the feedback network. The parameters are so chosen that the input impedance of the LNA is matched with 50 Ω requirements. The input impedance is determined by the cascode stage only given in Equation (15) [20].

\[
Z_1 = \frac{1}{g_m(1 + S_{cgs1})}
\]

where \( g_m \) is the material transconductance of \( M_1 \) while \( c_{gs1} \) is the gate-to-source junction capacitance. The impedance of feedback network is given below [16].

\[
Z_F = R_B \left\| \frac{1}{S(c_{gds1-2} + c_{gds4} + c_{gds5})} \right\|
\]

where \( c_{gds1-2} \) is the gate to drain capacitance of \( M_1 \) and \( M_2 \). The effective transconductance of feedback structure and the output impedance can be calculated as:

\[
G_{m4} = \frac{g_{m4}}{1 + g_{m4}}
\]

\[
Z_2 = \frac{1}{g_{ds1-2} \left\| \frac{1}{S g_{ds3}} \right\|}
\]

where \( g_{ds1-2} \) is drain-to-source conductance of \( M_1 \) and \( M_2 \).

The overall gain of the LNA is determined by the product of the gains of the cascode amplifier and the CS amplifier with feedback network. It is observed that with the increase of transconductance of the transistors, the gain is improved. Due to the combined feedback system, the \( g_m \) factor elevates resulting into higher gain and reduced power consumption [15]. Figure 6 shows equivalent small signal model of LNA.

**Figure 5** Input impedance variation versus frequency

**Figure 6** Small signal equivalent model of LNA
used to analyse the gain factor while in Figure 7 the gain performance of LNA is depicted in terms of simulated, mathematically calculated and measurement done from the fabricated chip of LNA. It is observed that theoretically, that the gain is 21.2 dB while the measurement turns out to be 22.5 dB when the other performance factors are taken into consideration such as parasitic components and noise factors, these are remarkably good figures. The gain of cascode amplifier is given by the following equation [20].

\[ A_{v1} = - \frac{g_{m2}r_{o2}(1 + g_{m1}r_{o1})Z_2}{2[r_{o1} + r_{o2} + r_{o1}r_{o2}(sC_{g1} + g_{m1})]} \] (19)

The gain of CS amplifier with feedback network is acquired from the following equation [15].

\[ A_{v2} = - \left( G_{m3} - \frac{1}{Z_F} \right) (Z_2 || Z_F) \] (20)

Taking \( Z_F \gg Z_2 \), the above equation can be simplified as:

\[ A_{v2} = -G_{m3}Z_2 \] (21)

By multiplying Equations (19) and (21), the total gain of LNA is achieved.

From the LNA circuit, it is evident that the main noise contributors are MOS devices along with the passive resistors. In order to calculate noise factor, it is more important to assume some parameters. For example, the output impedance of the transistors is assumed to be infinite, while the bias current source is assumed to be an ideal one. Only the thermal noise from transistors \( (i_n^2/\Delta f = 4kTg_m) \) and resistors \( (i^2/\Delta f = 4kT/R) \) is taken into consideration. Here \( \gamma \) is noise parameter of the MOS devices that varies from 2/3 to 2 for short channel devices. The gate resistance can be ignored [12]. The NF can be determined from the below mentioned equations [15].

\[ F = F_{\text{Cascode}} + F_{\text{CS-amplifier}} + F_{R_s} + F_{\text{FB}} \] (22)

\[ F_{\text{Cascode}} = \gamma_{m} \frac{m_3R_s}{\alpha_{\text{m1}}G_m} \left[ \frac{1}{R_s} + \frac{g_{m2}}{1 + g_{m2}R_f} \right]^2 \] (23)

where \( \alpha = \frac{g_{m1}}{g_{ds}} \), while \( g_{ds} \) is the zero bias transconductance of the transistor.

\[ F_{CS} = \frac{\gamma g_m c_s \left( 1 + g_m c_G R_s \right)}{(n + 1)^2R_sG_m^2} t^2 \] (24)

\[ g_m c_s = \frac{(n + 1)}{R_s} \] (25)

\[ g_m c_G = (n + 1)g_m c_G \] (26)

\[ G_m = 2g_m c_G \] (27)

\[ F_{CS} = \frac{\gamma}{n + 1} \] where \( n = 4 \) (28)

\[ F_{\text{feedback}} = \frac{\gamma M_5 g_m M_5}{\alpha_{M_5}} \frac{R_s}{(1 + g_m M_5 R_s)^2} \] (29)

\[ F_{\text{feedback}} = 1 \] (30)

\[ F = R_s R_f \left[ \frac{g_{m4}}{1 + g_m M_4 R_f} \right] \] (31)

The above expressions explain the combined effect of NF. Further studies of these expressions show that it can be minimised by choosing some factors carefully.

In case of cascode amplifier section of LNA, by increasing \( \alpha \) factor which in turn can be controlled by \( g_{m1} \) and \( g_{ds} \), the NF can be reduced. The effect of \( R_s \) and \( R_f \)
contributes in the noise performance of the device. By keeping these values low, the NF can be improved. Figure 8 shows the performance of LNA in terms of NF with respect to frequency. It is noted that NF remains almost constant in the operating band of 2.2 to 5.8 GHz at approximately 2 dB.

Figure 9 shows stability factor and third-order intercept point (IIP3) performances with respect to frequency. When the feedback method is adopted, it is worth considering stability of the amplifier, as it is evident that the incorporation of negative feedback improves the stability factor. For RF frequency range, the stability is determined by using $K$ factor that depends on $S$-parameters. To achieve stability, it is required to have $K > 1$ and $\Delta < 1$. Both $K$ and $\Delta$ are given by the equations given below [12].

\[
K = 1 - \left| \frac{S_{11}}{S_{22}} \right|^2 - \left| \frac{S_{12}}{S_{22}} \cdot \frac{S_{12}}{S_{21}} \right|^2 \]

\[
\Delta = \left| S_{11}S_{22} - S_{12}S_{21} \right| \]

The stability factor is dependent on gain and reflection coefficients which in turn are derived from the transistor parameters like $g_m$ and $r_o$. By varying these factors along with the body bias voltage ranges within 1 V, the unconditionally good stability is achieved for the complete frequency range of operation as depicted in the simulated performance graph. The stability factor is only 2.5 dB. The linearity of a circuit is affected by nonlinear $g_m$ of MOS devices. It occurs at the time of conversion of input voltage into output voltage. Most commonly, the linearity of LNA is determined by third-order intercept point. The indulgence of feedback in the LNA circuit yields all the frequency responses which include fundamental response ($H_1$ and $F_1$), second-order response ($H_2$ and $F_2$) and third-order response ($H_3$ and $F_3$). The complete effect can be

\[
IIP3 = \left( \sqrt{\frac{4}{3}} \right) \left| \frac{H_1}{R^3(H_3 - 2H_2F_1R + H_1^2(2H_2F_2R - F_3) - 4H_2^2F_2R)} \right| \]  

(34)

The Figure 10 shows the effect of $\mu$ and $\mu$ prime versus frequency.
shown in equation given below \[15\], where \( R = (1 + H1F1) - 1 \) is the feedback gain reduction factor. The \((W/L)\) aspect ratio of all the MOS devices is maintained in a manner so as to keep the linearity factor in desired range. As depicted graphically the simulated IIP3 is about 15 dBm. The stability is elaborated by considering the factors \( \mu \) and \( \mu \)-prime plotted in Figure 10 where both have acquired the values greater than 1 for unconditionally stable system. Figure 11 shows die microchip photograph of CMOS active feedback proposed LNA. It is fabricated using mixed signal TSMC process 45 nm CMOS technology with all testing pads. The calculated dimensions of the chip are 0.57 x 0.57 mm², while dc power consumption is 0.9 mW. Here, BSIM (Barkley short channel IGFET) RF MOSFET is used with an \( n \)-channel substrate for designing and fabricating the LNA chip. The behavioural performance of the chip is governed by measuring \( S \)-parameters and NF as depicted in Figures 3, 7 and 8 where the results are found to be quite correlated. The figure-of-merit (FoM) of LNA is calculated to be 111.8. The FoM can be calculated by using relation given below:

\[
FOM = \frac{S_{21}[dB] \times BW \ [GHz]}{P_{dc}(mW) \times [NF_{min} - 1]} \quad (35)
\]

Table 1 summarises about component values while Table 2 gives a comparison of the proposed research work with other reported works.

### TABLE 1 Component values of LNA design

| Components | Values | Components | Values |
|------------|--------|------------|--------|
| \( C_1 \) | 225 pF | RL | 200 \( \Omega \) |
| \( C_2 \) | 1 pF | 1 | 5 mA |
| \( C_3 \) | 1 pF | \( M_1 \) (W/L, \( g_{on} \)) (0.001/0.045 \( \mu \)m, 0.0091S) |
| \( R_1 \) | 175 K\( \Omega \) | \( M_2 \) (W/L, \( g_{on} \)) (225/0.045 \( \mu \)m, 0.0425S) |
| \( R_2 \) | 175 \( \Omega \) | \( M_3 \) (W/L, \( g_{on} \)) (325/0.045 \( \mu \)m, 0.0165S) |
| \( R_3 \) | 175 K\( \Omega \) | \( M_4 \) (W/L, \( g_{on} \)) (525/0.045 \( \mu \)m, 0.0125S) |
| \( R_4 \) | 175 \( \Omega \) | \( M_5 \) (W/L, \( g_{on} \)) (0.001/0.045 \( \mu \)m, 0.0091S) |
| \( R_5 \) | 1K \( \Omega \) | \( M_6 \) (W/L, \( g_{on} \)) (225/0.045 \( \mu \)m, 0.0425S) |

### TABLE 2 Performance comparison of LNA with other

| Design parameters | Present work \( [6] \) | \( [8] \) | \( [11] \) | \( [13] \) | \( [14] \) |
|-------------------|--------------------------|--------|--------|--------|--------|
| Technology (nm)   | 65                       | 65     | 65     | 180    | 180    | 45     |
| Frequency (GHz)   | 1–11                     | 0.3–4.4| 0.1–4.3| 2–8    | 2–5    | 2.2–5.8|
| NF (dB)           | 2.5–3                    | 3–4.4  | 2.8–4  | 2.9–3.3| 6–8    | 2      |
| \( |S_{21}| \) (dB)  | 14–17                    | 26.7   | 21.2   | 11     | 13     | 22.5   |
| IIP3 (dBm)        | >8                       | 14.2   | –7.7   | +14    | -      | +15    |
| \( P_{dc} \) (mW) | 11.3                     | 13.9   | 0.96   | 7      | 1.8    | 0.8    |
| FoM               | 138.6                    | 5.69   | 27.08  | 76     | 129    | 111.8  |

### FIGURE 12 Proposed active antenna (a) structure and (b) measurement set-up

3 | ANTENNA DESIGN-II AND ANALYSIS

The structural design of antenna with its results has been discussed in this section. A rectangular slotted CPW fed antenna is crafted for its obvious enormous benefits. The FR-4 substrate with relative permittivity (\( \varepsilon_r \)) of 4.4 and thickness \( h = 1.6 \) mm is used with the dimensions of 40 mm x 40 mm. The antenna design with its dimensions is illustrated in Figure 12(a) while measurement set up is depicted in Figure 12(b). The simulation is done on EM-Ansoft high frequency structure simulator (HFSS) v-11. The total substrate comprises of a rectangular radiator with two rectangular slots inside it. The CPW feeding is used whose dimensions are calculated from [21] with two partial symmetrical rectangular ground planes. These ground planes produce capacitive effect in order to nullify the inductive effect created by the rectangular radiator. Thus the antenna becomes completely resistive. The outcomes of CPW feeding are desirable in many ways that is why it is popularly used in antenna designing. The obvious benefits are its wideband response, minimal losses and ease of fabrication [22]. The antenna is designed for Wi-Fi network applications in the band range of 2.2 to 5.8 GHz. The worthy point considered in this design is that the LNA crafted in the above section...
has the same operating band so that both can be integrated together to form a complete receiver unit. Figure 13 shows the frequency band of antenna. It exactly matches with LNA while $S_{11}$ is closely $-16$ dB. Figure 14 gives the variation of the peak gain of the antenna with respect to frequency which remains almost of the highest value in the range of 3 to 5 GHz, while Figure 15 depicts its radiation pattern that turns out to be desirable one. The dimensions of antenna are illustrated in Table 3.

4 | DESIGN III, INTEGRATED RECEIVER

This section includes the antenna incorporation with LNA to get the receiver system designed for Wi-Fi application. The designing and performance results of antenna and LNA are discussed in the above sections. This structure can be attributed to an active antenna. The performance of receiver is based on the two vital parts which are antenna and LNA. In order to simulate the overall receiver performance, we call for integration of both LNA and antenna. For this purpose, the process includes export of HFSS file and imports it on advanced design system (ADS) platform. It is done by using the procedure given in the mentioned flow diagram of Figure 16. The first step includes creation of s2p file from HFSS software tool. In second step, it is imported in ADS and finally the simulation is done for the integrated device. As mentioned above, both these elements are designed to work in the same band so that they can be built together for other various functions in RF communication systems. The similar combination has been used in [23] for millimetre wave application. The concept of configuring LNA with antenna is being used time to time to elevate the features of wireless receiver systems.

The impedance matching and NF of an antenna are improved by directly coupling the antenna with an LNA [24].

**FIGURE 13** Return loss variation with respect to frequency

**FIGURE 14** Antenna gain variation with frequency

**FIGURE 15** Antenna radiation pattern

**TABLE 3** Dimensions of proposed antenna

| Dimensions | Values (mm) | Dimensions | Values (mm) |
|------------|-------------|------------|-------------|
| $W_{sub}$  | 40          | $L_2$      | 15          |
| $L_{sub}$  | 40          | $L_g$      | 17          |
| $A$        | 36          | $W_y$      | 18          |
| $B$        | 20          | $W_x$      | 3           |
| $W_1$      | 15          | $T$        | 0.5         |
| $W_2$      | 5           | $G$        | 2           |
| $L_1$      | 10          |            |             |
In another research effort [25], a low frequency radio astronomy antenna is connected to measure noise of a differential LNA. Thus this research study proposes a blend of LNA with active antenna. The codesign structure is shown in Figure 17. In this design, it is important to maintain impedance matching between the elements so that the gain factor and other desired parameters are not affected poorly. Here the impedance of the structure is attained in the preferred range. As it is evident that antenna catches noise, therefore, the combination of LNA with antenna sacrifices noise factor which comes out to be 2.6 dB of its minimum value at 2.06 GHz with variation of ±1.5 dB as shown in Figure 18. The combinational performance of the receiver in terms of S-parameters shown in Figure 19 reveals that much wider band ranging from 1.6 GHz to 6 GHz is attained. The individual gain of antenna is not good enough as the signal can be fed to the load directly. Thus addition of LNA with antenna offers a reasonably good gain factor in the same band with a peak value of 16.5 dB.

5 | CONCLUSION

The study presented a CMOS LNA with AFB for Wi-Fi networks. The LNA design architecture has the input stage as a cascode network to offer wideband impedance matching followed by the CS amplifier along with NMOS AFB. The feedback mechanism with inductor-less approach is used to nullify the noise effect with improved bandwidth, gain stability and impedance performances while being active and helps to obtain the enhanced gain. The LNA achieved wide bandwidth in the range of 2.2 GHz to 5.8 GHz with the peak forward gain of 22.5 dB. The NF value of approximately 2 dB, the stability factor of nearly 2.5 dB and IIP3 of about 15 dBm have been achieved with µ and µ prime well above 1. A CPW fed antenna is designed to achieve wide band response similar to that of LNA. The peak gain of approximately 4.1 dBi at 3.9 GHz is achieved. Finally, the codesign receiver system gave a much wider band of 1.6–6 GHz, whereas gains of 16.5 dB and minimum NF of 2.59 dB at 2.06 GHz in the same band were achieved.
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