Electrically function-switchable magnetic domain-wall memory

Yu Sheng1, Weiyang Wang1,2, Yongcheng Deng1, Yang Ji1,2, Houzhi Zheng1,2 and Kaiyou Wang1,2,*

ABSTRACT

Versatile memory is strongly desired for end users, to protect their information in the information era. In particular, bit-level switchable memory that can be switched from rewritable to read-only function would allow end users to prevent important data being tampered with. However, no such switchable memory has been reported. We demonstrate that the rewritable function can be converted into read-only function by applying a sufficiently large current pulse in a U-shaped domain-wall memory, which comprises an asymmetric Pt/Co/Ru/AlOx heterostructure with strong Dzyaloshinskii-Moriya interaction. Wafer-scale switchable magnetic domain-wall memory arrays on 4-inch Si/SiO2 substrate are demonstrated. Furthermore, we confirm that the information can be stored in rewritable or read-only states at bit level according to the security needs of end users. Our work not only provides a solution for personal confidential data, but also paves the way for developing multifunctional spintronic devices.

Keywords: spintronics, spin orbit torques, magnetic domain-wall, SOT-MRAM, information security

INTRODUCTION

With the unprecedented expansion of information technology, the large amount of data produced by an abundance of terminals calls for memory with increased versatility, advantageous performance and high security, which is in particular demand by end users. Complementary-metal-oxide-semiconductor (CMOS) based memory, as the current mainstream memory, is the main bottleneck of computer systems [1,2]. Researchers have made great efforts with regards to creating versatile memory with high-performance and low-power operation, producing, for example, resistance change memory [3–6], phase change memory [7–10], ferroelectric memory [11–14] and spintronic memory [15–19]. All these reported memories so far only have a rewritable function, and thus the stored information is at risk of being tampered with by hackers through the internet, and this cannot be fully resolved by encryption. Read-only memory can effectively protect data integrity, but existing memory solutions do not allow end users to selectively set the important data to read-only at bit level.

Domain-walls driven by spin orbit torques (SOTs) have a reciprocating motion, meaning they have great potential in the area of rewritable memory due to their non-volatility, high speed and low power consumption [17,18]. If the domain-wall can be electrically annihilated, the device can be turned into read-only. However, the high potential step caused by exchange bias makes the domain-wall hard to cross and annihilate with a current without damaging the device [20]. To realize function-switchable memory, the height of the potential step in different regions of the U-shaped device should be carefully designed to guarantee the device works in both the rewritable and read-only functions.

Here we report on the experimental realization of wafer-scale domain-wall memory arrays for high performance and high security. This U-shaped domain-wall memory, composed of a Pt/Co/Ru/AlOx heterostructure, can be electrically switched from rewritable to read-only function at bit level. With the strong Dzyaloshinskii-Moriya interaction (DMI) of the asymmetric multilayer and reduction of critical current by controlling the deposition of the AlOx layer [21], the rewritable function can be...
Figure 1. Device structure, magnetization switching by magnetic field, and purely current-driven domain-wall motion. (a) Optical image of the U-shaped device and anomalous Hall effect measurement configuration with the definition of x–y–z coordinates. The gray stripe at both ends of the U-shaped region are trenches where the Co/Ru bilayer is etched away by the argon ion beam. (b) Out-of-plane magnetic hysteresis loops, obtained by a polar magneto-optical Kerr effect (pMOKE) microscope, of the U-shaped device in the Pt(4 nm)/Co(0.85 nm)/Ru(1.2 nm) region (red), Pt/Co/Ru/AlOx (0.5 nm) region (gray) and the boundary (blue), as shown in the insets. (c,d) pMOKE images of the magnetic domain states with initialization of \( H_x = 3600 \) Oe and \( I_{pulse} = +22 \) mA \((c_a)\), and images after \( I_{pulse} = -9 \) mA \((c_b)/+9 \) mA \((c_c)\) in the absence of \( H_x \). \((c_d)\) pMOKE images with initialization of \( H_x = 3600 \) Oe and \( I_{pulse} = -22 \) mA \((c_d)\) and after \( I_{pulse} = -9 \) mA \((c_e)/+9 \) mA \((c_f)\) in the absence of \( H_x \). Light- and dark-gray regions indicate magnetization-down and -up domains, respectively. (d–g) Field-free current-induced deterministic switching loops of perpendicular magnetization in the curved section \((\text{AlO}_x\text{ capped})\) for four types of initializations: \( H_x = \pm 3600 \) Oe and \( I_{pulse} = \pm 22 \) mA. (h) Out-of-plane magnetic-field-induced magnetization switching loop in the curved section.

realized by field-free current-induced domain-wall reciprocating motion by SOTs. The stored information can be converted to a read-only state bit by bit through domain-wall annihilation at the edge of the ferromagnetic layer after applying a sufficiently large current. Thus, the read-only bits become immune to electric current pulses, ensuring information integrity when under threat from hackers or impostors.

RESULTS

Electrical operation of a U-shaped SOT-driven domain-wall memory device

To effectively create and control the magnetic domain-wall by SOTs, a U-shaped device was designed consisting of asymmetric Pt(4 nm)/Co(0.85 nm)/Ru(1.2 nm) multilayers. An AlOx(0.5 nm) capped layer was deposited on the curved region to locally weaken the perpendicular magnetic anisotropy (PMA) through tuning the density of defects by ion irradiation [21] (Fig. 1a). Magnetic hysteresis loops were measured using a polar magneto-optical Kerr effect (pMOKE) microscope, with a focused laser spot positioned at the straight section, curved section and the boundary between them (Fig. 1b). The switching fields of the curved and straight sections are 25 Oe and 125 Oe, respectively, confirming the role of the AlOx capped layer. Double-step switching of the hysteresis loop reveals that the domain-wall can be pinned at the boundary of the straight and curved sections (Fig. 1b). The design of the PMA difference is to constrain the domain-wall motion in the low PMA region under a small current in the rewritable function, and also allow the domain-wall to cross over the boundary under a relatively large current intensity without damaging the device during function switching.
Theoretically, the z-component of SOTs effective field is given by [22],

$$H_{z}^{\text{SOT}} = \frac{\hbar}{2eM_{s}t} \theta_{SH} J_{x} m_{x},$$

(1)

where $\hbar$ is the reduced Planck constant, $e$ is the electron charge, $M_{s}$ is the saturation magnetization, $t$ is the thickness of the ferromagnetic layer, $\theta_{SH}$ is the spin Hall angle of heavy metal, $m_{x}$ is the x-component of magnetization orientation and $J_{x}$ is the x-component of charge current density. The $H_{z}^{\text{SOT}}$ direction is defined by both directions of $J_{x}$ and $m_{x}$. In the U-shaped device, the $J_{x}$ changes its direction as it passes the centerline of the curved section. Therefore, the $H_{z}^{\text{SOT}}$ for the up- and down-regions of the device will be opposite with the same direction of $m_{x}$ consistently determined by an in-plane magnetic field, leading to opposite domains formed at both sides of the centerline of the curved section, which is confirmed by the pMOKE images in Fig. 1c$_{x}$ and c$_{d}$. The up-region prefers downward magnetization and the down-region prefers upward magnetization after initialization with $H_{x} = 3600 \text{ Oe}$ and $I_{x} = 22 \text{ mA}$, where the duration of current pulses is set to be 10 ms for this paper except where stated (Fig. 1c$_{x}$). But opposite magnetic domain configurations are formed after $H_{x} = 3600 \text{ Oe}$ and $I_{x} = -22 \text{ mA}$ (Fig. 1c$_{d}$). If both the magnetic field and current directions are reversed for initializations, the same magnetic domain configurations are formed. By constructing asymmetric stacks of Pt/Co/Ru with large DMI, the left-hand Néel domain-wall (⊙| ⃝×| ⊙) can be stabilized [23,24]. Thus, the electric current can move the domain-wall along the current direction without the assistance of an external magnetic field.

We then investigated field-free current-induced magnetization switching with the domain-wall motion using both the anomalous Hall effect and pMOKE for different initialized magnetic domain configurations. As shown in Fig. 1d, after the initialization with $H_{x} = 3600 \text{ Oe}$ and $I_{x} = 22 \text{ mA}$, a clockwise current-induced switching loop at zero field was observed, where the current pulses scanned from +9 to -9 mA, and then back to +9 mA with each point representing a single pulse. The positive current favors the domain-wall motion from up-region to down-region, while the negative current favors the opposite domain-wall motion, resulting in the magnetization downward and upward, respectively. However, after the initialization with $H_{x} = 3600 \text{ Oe}$ and $I_{x} = -22 \text{ mA}$, anticlockwise current-induced magnetization switching was observed (Fig. 1e). As expected, for the same initialization of the magnetic domain configurations, the device showed the same deterministic current-induced magnetization switching (Fig. 1d and f, and Fig. 1e and g). The switching magnitudes of $R_{\text{Hall}}$ after initializations of $H_{x} = 3600 \text{ Oe}$ and $I_{x} = 22 \text{ mA}$, $H_{x} = 3600 \text{ Oe}$ and $I_{x} = -22 \text{ mA}, H_{x} = -3600 \text{ Oe}$ and $I_{x} = 22 \text{ mA},$ and $H_{x} = -3600 \text{ Oe}$ and $I_{x} = -22 \text{ mA}$ are $1.31 \Omega, 1.31 \Omega, 1.31 \Omega$ and $1.30 \Omega$, respectively, which are very close to the switching amplitude of 1.34 $\Omega$ (~97%) by the magnetic field (Fig. 1h). The critical switching current densities for these four initialized configurations are (2.5 ± 0.2) x 10$^{6}$ A/cm$^{2}$, indicating low power consumption in application. By driving the domain-wall with microsecond short pulses, we found that the motion speed of the domain-wall is at least 14.5 m/s, so that the function speed can be improved to ns-regime by shrinking the device to nm-scale. In contrast, the referenced symmetrically stacked Pt/Co/Pt U-shaped devices (Fig. S1) have much smaller switching amplitude (12%–35%) and the current-induced switching direction is uncorrelated with the initialization [25,26], indicating the importance of the large DMI for SOT-based domain-wall devices.

**Narrow resistance distribution and high reproducibility**

To achieve error-free rewritable domain-wall memory and robust read-out, the average change in resistance ($\Delta R$) from the low to high state should be at least $12\sigma$ to have working memories with bit counts of Mb or more [27], where the standard deviation $\sigma = \sqrt{\sum_{i=1}^{n}(R_{i} - R_{\text{ave}})^{2}/n}$, $R_{\text{ave}}$ is the averaged anomalous Hall resistance $R_{H}$ of each state, and $n = 2000$ is the total number of pulse cycles. For all four types of initializations, we realized the rewritable function with high reproducibility using alternating current pulses (Fig. 2a–d). The ratios of $\Delta R/\sigma$ for each type of initialization, $H_{x} = 3600 \text{ Oe}$ and $I_{x} = 22 \text{ mA}, H_{x} = 3600 \text{ Oe}$ and $I_{x} = -22 \text{ mA},$ $H_{x} = -3600 \text{ Oe}$ and $I_{x} = 22 \text{ mA},$ and $H_{x} = -3600 \text{ Oe}$ and $I_{x} = -22 \text{ mA}$ are 177, 240, 223 and 146 respectively, proving that the device shows excellent error-free switching and read-out ability. A wide current-induced switching window up to 10 mA with $\Delta R/\sigma$ higher than 12 is obtained for initialization of $H_{x} = 3600 \text{ Oe}$ and $I_{x} = 22 \text{ mA}$ (Fig. S2), ensuring stable switching for applications.

**Function switching in a domain-wall memory device**

To convert the device from rewritable to read-only function, a large current pulse is needed to annihilate the domain-wall. After initialization of
Figure 2. Narrow resistance distribution under alternately positive and negative current pulses. (a–d) Histograms of resistance distribution with a bin size of 0.0015 $\Omega$ under alternating current pulses for all types of initializations: $H_x = \pm 3600$ Oe and $I_{\text{pulse}} = \pm 22$ mA. The applied pulse sequences are alternately positive and negative current pulses with an amplitude of 9 mA and duration of 10 ms for 2000 cycles. $H_x = 3600$ Oe and $I_x = -22$ mA (Fig. 3), the $+/−9$ mA current pulses can drive the domain-wall back and forth to realize the rewritable function at zero magnetic field. Then, a large current pulse of $+21$ mA is injected into the device, and $R_{\text{Hall}}$ switched from a low-resistance state to a high-resistance state. After that, the $R_{\text{Hall}}$ remains in the high-resistance state and cannot be changed even with very large current pulses of $+/−21$ mA (Fig. 3).

Similarly, a $−21$ mA current pulse led to a low-resistance state in the device. Therefore, after a large current pulse was applied, the device entered the read-only function associated with the annihilation of the domain-wall, as confirmed by the pMOKE images in Fig. 3a, and ad. We further studied the dependence of switching probability from rewriteable to read-only function on the current pulse magnitude. The switching probability was <0.01% with a current smaller than 15.5 mA, increasing to 100% with a current of 19.5 mA and above (Fig. 3d and Fig. S4).

Interestingly, with the assistance of an in-plane magnetic field, the device in read-only function was electrically reconverted to rewriteable function along with the regeneration of the domain-wall (Fig. 3c).

Figure 3. Function switching of the domain-wall device. (a–c) The measured magnetic domain-wall configurations ($a_2−a_4$) and $R_{\text{Hall}}$ (b) after each current pulse (c). Red (blue)-line segments indicate the positive (negative) current pulses and the corresponding $R_{\text{Hall}}$ after the current pulse, and the black-line segments indicate the current pulse for function switching from rewriteable to read-only and the corresponding $R_{\text{Hall}}$. The orange area represents initialization with $H_x = 3600$ Oe and $I_x = −22$ mA. Insets show pMOKE images of the corresponding magnetic states indicated by the dashed arrows ($a_2−a_4$). The pulse durations are all 10 ms. (d) The switching probability from rewriteable to read-only function as a function of the current pulse amplitude.

Demonstration of wafer-scale function-switchable domain-wall memory arrays

We fabricated function-switchable domain-wall memories on a 4-inch Si/SiO$_2$ substrate (Fig. 4a) using a standard CMOS-compatible process. The optical image of the zoomed-in $6 \times 6$ array of the wafer-scale devices is shown in Fig. 4b. Each device in the array can be electrically controlled by selecting the corresponding row and column electrodes. The information in our function-switchable domain-wall memory can be stored in rewriteable state or read-only state at bit level according to the demands of end users. A set of data in rewriteable function was written by current pulses of $+/−9$ mA. As shown
Figure 4. Wafer-scale function-switchable domain-wall memory arrays. (a) Optical image of the function-switchable magnetic domain-wall memory arrays fabricated on a 4-inch silicon wafer. (b) Optical image of the zoomed-in 6 × 6 array of the wafer-scale devices, where the red line with arrows indicates the path to inject a current pulse to a single device. (c–e) pMOKE images of the zoomed-in 6 × 6 array. The right column defines the pMOKE images for ‘0’ and ‘1’ in rewritable and read-only state, and also recovery state. (c) Under the rewritable function, a selected set of data ‘0’ and ‘1’ was written. (d) Four bits in the center of the array were converted to read-only function of ‘1’ (‘0’) by a current pulse of +(-)21 mA, as shown in the brown frame. (e) One read-only bit was reversed back to rewritable function by a combination of an in-plane magnetic field of 3600 Oe and a current pulse of -22 mA (brown frame changing to blue frame).

in Fig. 4c, the bits in the outermost circle are ‘1’, written using +9 mA (magnetization downward), the bits in the middle circle are ‘0’, written using -9 mA (magnetization upward), and the 2 × 2 bits in the center are ‘1’, written using +9 mA as well. The 2 × 2 bits in the center were converted into read-only function of ‘1’ using a current pulse of +21 mA and ‘0’ using a current pulse of -21 mA (Fig. 4d, brown frames). The read-only state cannot be changed solely by electrical current since it has no domain-wall (Fig. 4d), thus eliminating the possibility of data tampering by hackers through the internet. With the aid of an in-plane magnetic field, the read-only bit cell can be electrically converted back to a rewritable cell without affecting other bits (Fig. 4e, blue frame). To our knowledge, such recoverability is not available with conventional read-only memory. The wafer-scale switchable domain-wall memory not only allows end users to store their information in rewritable or read-only mode at bit level according to their own wishes, but can also work together with existing encryption techniques, which can further meet customized security requirements.

Except for spin-torque[1] driven race-track memory [28,29], magnetic domain-wall memories with non-volatility and high design flexibility have attracted more interest, with remarkable achievements in magnetic field-driven logic [30], SOT-driven magnetic logic [17,28] and neuromorphic computing [31,32]. The reciprocal motion of the current-driven domain-wall in this work could also be utilized for spin logic and neuromorphic computing, for example, through series and parallel connecting devices with materials of opposite spin Hall angle.

CONCLUSION

In conclusion, we experimentally demonstrate wafer-scale electrically function-switchable domain-wall memory arrays by designing U-shaped domain-wall memory composed of Pt/Co/Ru/AlOx. The capped AlOx layer can effectively reduce the critical current of SOT-driven domain-wall motion in the curved section of the U-shaped device by its thickness. With a strong DMI, the rewritable function can be realized by field-free SOT-induced domain-wall reciprocating motion with a small driving current density of (2.5 ± 0.2) × 10^6 A/cm^2. When the injected current is increased over a critical value, the domain-wall is annihilated at the edge of the ferromagnetic layer, inducing the stored information conversion from a rewritable to read-only state at bit level. The electrically function-switchable memory not only provides more versatile memory, but also paves the way for developing spin logic and neuromorphic computing.

MATERIALS AND METHODS

Thin film preparation

The films were deposited on Si/SiO2 substrate by magnetron sputtering at room temperature. DC magnetron sputtering was used to deposit the Ta, Pt, Co and Ru layers. AC magnetron sputtering was used to deposit the AlOx layer. The base pressure of the chamber was less than 2.0 × 10^-6 Pa. The pressure of the chamber was 1.06 × 10^-1 Pa for Ta, Pt, Co and Ru, and 2.67 × 10^-1 Pa for AlOx during deposition, respectively. The deposition rates for Ta, Pt, Co, Ru and AlOx layers were controlled at 0.022, 0.0240, 0.0124, 0.017 and 0.002 nm/s, respectively.

Device fabrication

For a single device, UV lithography and magnetron sputtering deposition were used twice. First, the Ta (1 nm)/Pt (4 nm)/Co (0.85 nm)/Ru (1.2 nm) film was patterned into U-shaped devices with a channel width of 16 μm and inner diameter of 30 μm. Then, using photolithography engraving and magnetron sputtering deposition, an AlOx layer with a thickness of 0.5 nm was grown in
the curved section. Finally, argon ion beam etching was used to make trenches with a width of 5 μm in both straight sections, where Co/Ru bilayers were precisely etched away.

For the wafer-scale domain-wall memory arrays, every U-shaped device has a channel width of 10 μm and an inner diameter of 20 μm. The additional process of lift-off is needed to make the row electrodes (Ta (10 nm)/Au (50 nm)) and column electrodes (Ta (10 nm)/Au (150 nm)). To prevent electrical contact between the two layers of electrodes, a layer of SiOx with a thickness of 100 nm is deposited by plasma-enhanced chemical vapor deposition (PECVD) to separate them.

Measurement and characterization

The current-induced magnetization switching and anomalous Hall effect measurements were carried out at room temperature with a Keithley 2602B as the current source and Keithley 2182 as the nanovoltmeter. The Kerr imaging measurements were carried out using a NanoMOKE3 microscope.

SUPPLEMENTARY DATA

Supplementary data are available at NSR online.

FUNDING

This work was supported by the National Key Research and Development Program of China (2022YFA1405100), the Beijing Natural Science Foundation Key Program (Z190007), the National Natural Science Foundation of China (12241405 and 12104449) and the Chinese Academy of Sciences (QYZDY-SSW-JSC020, XDPB44000000 and XDB28000000).

AUTHOR CONTRIBUTIONS

K.W. conceived the work. Y.S. and W.W. deposited the thin films. Y.S. fabricated the devices and performed the SOT-driven domain-wall measurements. Y.S. and K.W. analyzed the data and wrote the manuscript. All authors discussed the results and commented on the manuscript.

Conflict of interest statement. None declared.

REFERENCES

1. Banerjee W. Challenges and applications of emerging non-volatile memory devices. *Electronics* 2020; 9: 1029.
2. Ding K, Wang J and Zhou Y et al. Phase-change heterostructure enables ultralow noise and drift for memory operation. *Science* 2019; 215: 210–5.
3. Borghetti J, Snider GS and Kuekes PJ et al. “Memristive” switches enable “stateful” logic operations via material implication. *Nature* 2010; 464: 873–6.
4. Ohno T, Hasegawa T and Tsuruoka T et al. Short-term plasticity and long-term potentiation mimicked in single inorganic synapses. *Nat Mater* 2011; 10: 591–5.
5. Zhou F, Zhou Z and Chen J et al. Optoelectronic resistive random access memory for neuromorphic vision sensors. *Nat Nanotechnol* 2019; 14: 776–82.
6. Strukov DB, Snider GS and Stewart DR et al. The missing memristor found. *Nature* 2008; 453: 80–3.
7. Jo SH, Chang T and Ebbing J et al. Nanoscale memristor device as synapse in neuromorphic systems. *Nano Lett* 2010; 10: 1297–301.
8. Van De Burgt Y, Lubberman E and Fuller EJ et al. A non-volatile organic electrochemical device as a low-voltage artificial synapse for neuromorphic computing. *Nat Mater* 2017; 16: 414–8.
9. Hamann HF, Boyle MO and Martin YC et al. Ultra-high-density phase-change storage and memory. *Nat Mater* 2006; 5: 383–7.
10. Loke D, Skelton JM and Wang W et al. Ultrafast phase-change logic device driven by melting processes. *Proc Natl Acad Sci USA* 2014; 11: 13272–7.
11. Kim WW, Kim H and Kim T et al. Graphene–ferroelectric metadevices for nonvolatile memory and reconfigurable logic-gate operations. *Nat Commun* 2016; 7: 10429.
12. Khan AI, Keshavari A and Datta S. The future of ferroelectric field-effect transistor technology. *Nat Electron* 2020; 3: 588–97.
13. Ghittorelli M, Lenz T and Sharifi Dehsari H et al. Quantum tunnelling and charge accumulation in organic ferroelectric memory diodes. *Nat Commun* 2017; 8: 15741.
14. Tomas J, Bellaiche L and Bies M. Learning through ferroelectric domain dynamics in solid-state synapses. *Nat Commun* 2017; 8: 14736.
15. Cao Y, Sheng Y and Edmonds KW et al. Deterministic magnetization switching using lateral spin–orbit torque. *Adv Mater* 2020; 32: 1907929.
16. Cai K, Yang M and Ju H et al. Electric field control of deterministic current-induced magnetization switching in a hybrid ferromagnetic/ferroelectric structure. *Nat Mater* 2017; 16: 712–6.
17. Luo Z, Hrabec A and Yao TP et al. Current-driven magnetic domain-wall logic. *Nature* 2020; 579: 214–8.
18. Raymenants E, Bulynck O and Wann D et al. Nanoscale domain wall devices with magnetic tunnel junction read and write. *Nat Electron* 2021; 4: 392–6.
19. Allwood DA. Magnetic domain-wall logic. *Science* 2005; 309: 1688–92.
20. Fukami S, Suzuki, T and Nagahara K et al. Low-current perpendicular domain wall motion cell for scalable high-speed MRAM. *2009 Symposium On Vlsi Technology, Digest of Technical Papers* 2009; 230–1. https://ieeexplore.ieee.org/document/5200610?arnumber=5200610
21. Li R, Li Y and Sheng Y et al. RF magnetron sputtering induced the perpendicular magnetic anisotropy modification in Pt/Co based multilayers. *Chinese Phys B* 2021; 30: 028506.
22. Li R, Zhang S and Luo S et al. A spin–orbit torque device for sensing three-dimensional magnetic fields. *Nat Electron* 2021; 4: 179–84.
23. Khadka D, Karayev S and Huang SH. Dzyaloshinskii – Moriya interaction in Pt/Co/Ir and Pt/Co/Ru multilayer films. *J Appl Phys* 2018; 123: 123905.
24. Emori S, Bauer U and Ahn S-M et al. Current-driven dynamics of chiral ferromagnetic domain walls. *Nat Mater* 2013; 12: 611–6.
25. Hrabec A, Porter NA and Wells A et al. Measuring and tailoring the Dzyaloshinskii-Moriya interaction in perpendicularly magnetized thin films. *Phys Rev B* 2014; 90: 020402.
26. Haazen PPJ, Mureau E and Franken JH et al. Domain wall depinning governed by the spin Hall effect. *Nat Mater* 2013; 12: 299–303.
27. Akerman J, De Herrera M and Durlam M et al. Magnetic tunnel junction based magnetoresistive random access memory. In: Johnson and M (ed.). Magneto-electronics. Cambridge: Academic Press, 2004, 231–72.
28. Parkin SSP, Hayashi M and Thomas L. Magnetic domain-wall racetrack memory. *Science* 2008; 320: 190–4.
29. Parkin S and Yang S. Memory on the racetrack. *Nat Nanotechnol* 2015; 10: 195–8.
30. Luo Z, Dao TP and Hrabec A et al. Chirally coupled nanomagnets. *Science* 2019; 363: 1435–9.
31. Yue K, Liu Y and Lake RK et al. A brain-plausible neuromorphic on-the-fly learning system implemented with magnetic domain wall analog memristors. *Sci Adv* 2019; 5: aau8170.
32. Siddiqui SA, Dutta S and Tang A et al. Magnetic domain wall based synaptic and activation function generator for neuromorphic accelerators. *Nano Lett* 2020; 20: 1033–40.