This manuscript is the accepted version of the following IEEE Xplore Conference Proceedings:
M. Maezawa, K. Imafuku, M. Hidaka, H. Koike and S. Kawabata, “Design of Quantum Annealing Machine for Prime Factoring,” in the special number of IEEE Xplore Conference Proceedings of the 16th International Superconductive Electronics Conference (ISEC 2017), Sorrento, Italy, June 12 - 16, 2017.

©2017 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.
Design of Quantum Annealing Machine for Prime Factoring

M. Maezawa, K. Imafuku, M. Hidaka, H. Koike, S. Kawabata
National Institute of Advanced Industrial Science and Technology
Tsukuba, Ibaraki 305-8565, Japan
masaaki.maezawa@aist.go.jp

Abstract—We propose a prime factoring machine operated in a framework of quantum annealing (QA). The idea is inverse operation of a quantum-mechanically reversible multiplier implemented with QA-based Boolean logic circuits. We designed the QA machine on an application-specific-annealing-computing architecture which efficiently increases available hardware budgets at the cost of restricted functionality. The circuits are to be implemented and fabricated by using superconducting integrated circuit technology. We propose a three-dimensional packaging scheme of a qubit-chip / interposer / package-substrate structure for realizing practically-large scale QA systems.

Keywords—quantum annealing; factoring; superconducting integrate circuit; adiabatic quantum computing; three-dimensional packaging

I. INTRODUCTION

Since Shor’s discovery of quantum algorithms [1], prime factoring of large numbers has been the biggest game in the field of quantum computing [2]-[4] because its difficulty guarantees the security of RSA cryptosystem [5]. On the other hand, a new type of quantum computing, i.e., quantum annealing (QA) was proposed by Kadowaki and Nishimori [6], and has been pursued and developed mainly by D-Wave Systems in the past decade [7]-[11]. While D-Wave-type QA machines are considered promising for solving optimization and sampling problems, they can also solve various problems expressed in forms of combinational logic on the basis of Ising-model implementation of Boolean logic [12]. In this paper we present design of a superconducting QA-based factoring machine which is basically the same as a Boolean multiplier operated in the inverse direction. Our plan toward a practical-scale factoring machine is discussed from concept to technology.

II. QUANTUM ANNEALING FOR FACTORING

The QA process is reversible because its time evolution is unitary. Fig. 1 shows an operation principle of a factoring machine which is a QA multiplier operated inversely [12]. The QA machine, multiplier and/or factorizer, is designed to have the minimum energy when the boundary states satisfy \( P = M \times N \). By setting \( M \) and \( N \), the product \( P = M \times N \) is obtained at the energy minimum after the annealing process. In a similar way, by setting \( P \), one of the possible combinations of the factors \( M \) and \( N \) is probabilistically obtained.

The QA factoring machine is simply designed as a multiplier composed of Boolean logic gates in the same way as classical digital circuits. But different from the classical circuits, the logic gates consist of qubits and inter-qubit couplers to be operated quantum mechanically. The QA implementation of the Boolean logic gates is expressed by Hamiltonian of Ising model,

\[
H = \sum_i h_i \sigma_i + \sum_{ij} J_{ij} \sigma_i \sigma_j ,
\]

where \( \sigma_i \) is an \( i \)-th qubit spin, \( h_i \) is a qubit bias energy, and \( J_{ij} \) is a coupling energy between qubits [12]. For instance, a QA NOR gate has \( h_1 = h_2 = 0.5, h_3 = 1, J_{12} = 0.5 \) and \( J_{13} = J_{23} = 1 \) (Fig. 2(a)). An arbitrary Boolean logic circuit is constructed by accordingly connecting the QA logic gates with \( J_{ij} = -1 \). As shown in Fig. 2(b), a QA half adder is composed of three QA NOR gates, \( Q_1-Q_2-Q_3, Q_4-Q_5-Q_6 \) and \( Q_7-Q_8-Q_9 \). Here, the \( Q_3-Q_8 \) and \( Q_6-Q_7 \) couplings with \( J_{38} = J_{67} = -1 \) plainly interconnect the qubits whereas the \( Q_1-Q_4 \) and \( Q_2-Q_5 \) couplings with \( J_{14} = J_{25} = 1 \) provide not only interconnection but also NOT operation. Assuming the straightforward implementation like a...

This paper is partly based on results obtained from a project commissioned by the New Energy and Industrial Technology Development Organization (NEDO).
half adder in Fig. 2(b), we roughly estimate that $25p^2$ qubits carry out factoring of a $p$-bit number.

**III. ARCHITECTURE AND IMPLEMENTATION**

The QA machine for factoring is to be realized using superconducting integrated circuit technology that is the most advanced one among solid-state quantum circuit technologies [13][14]. However, a strong constraint in the architecture layer is the limited hardware budget associated with the immaturity of the superconducting circuit manufacturing. Even state-of-the-art Nb-based technologies allow the integration of $10^6$ to $10^7$ Josephson junctions per chip [15][16], which is four to five orders of magnitude lower than those in today’s semiconductor circuits. Our strategy is restriction of the functionality: we intend to develop a QA machine only for factoring applications. The target QA machine has a fixed structure of the qubit network with built-in parameters, $h_i$ and $J_{ij}$, specialized for the factoring operation. The special-purpose approach, which we name an Application Specific Annealing Computing (ASAC) architecture, efficiently reduces the hardware overhead as well as the cost and time for development. Although the limited faculty limits the applications, we expect a complementary role with general purpose QA machines like D-Wave machine.

The circuits are implemented with Josephson junctions and superconducting inductors. Following D-Wave [8]-[10], we employ a superconducting flux qubit whose potential is tunable with transvers fields. In contrast with D-Wave machine, the inter-qubit coupler is a passive transformer with fixed mutual inductance. Fig. 3 shows a simplified schematic of the qubit which is equipped with eight connection ports, C1 to C8, for connecting other qubits, control circuits and a readout circuit. The qubit bias $h_i$ is set with a current $I_x$. The coupling strength $J_{ij}$ is fixed but discretely changed by selecting the built-in number of the connection ports for coupling. The polarity of $J_{ij}$, positive or negative, is also selectable by changing the connection polarity of the ports. The transvers field is induced by an external input current $I_t$ for annealing. The circuit parameters such as the junction critical currents and inductances are under optimization.

Fig. 4 shows a block diagram of a QA NOR gate consisting of three superconducting qubits, $Q_1$, $Q_2$ and $Q_3$. Blank ports are used for the inter-gate connections, fine bias control and readout.

**IV. TECHNOLOGY INTEGRATION**

As discussed at the beginning of Section III, the number of available Josephson junctions or superconducting qubits per chip is strictly limited. At present, for instance, the existing largest-scale QA machine, D-Wave 2000Q, has at most 2000 qubits, which consists of a single QA processor chip [7]. Multi-chip module (MCM) packaging is therefore an essential technology for realizing a practically-large-scale QA machine for solving practical problems. Another big challenge in the technology layer is how to meet the different technology requirements for different types, quantum and classical, of circuits. On one hand, low-$J_c$ Josephson junctions in submicron sizes are necessary for the quantum circuits, qubits and couplers, to reduce both subgap leakage currents and parasitic capacitance for achieving long decoherence times. On the other hand, higher-$J_c$ junctions in moderate sizes are suitable for fabricating the classical circuits for control and readout of the qubits. Our decision is separation of the fabrication processes: the qubits and couplers are integrated on reasonably small-size chips for maintaining sufficient yields of working chips; the auxiliary control and readout circuits are built in large-size interposers for facilitating the MCM packaging.

Fig. 5 shows a schematic cross-section of a three-dimensional packaging, a Qubit-chip / Interposer / Package-substrate (QUIP) structure, which we propose for realizing practical-scale QA factoring machines on ASAC architecture. A qubit chip, on which the qubits and couplers are densely integrated, is fabricated by using a modified version of our standard technology developed chiefly for superconducting digital circuits [15]. The modification includes the deposition of Nb/AlO$_x$/Nb Josephson-junction trilayers directly on hydrogen-terminated silicon substrates and the elimination of noisy disordered oxide such as anodized NbO$_x$, which are expected to improve the qubit performance. An active interposer, on which the qubit chips are mounted by using a
flip-chip technology with superconducting solder bumps, includes the control and readout circuits consisting of moderate-size Josephson junctions. Superconducting through silicon vias are also fabricated in the active interposers for package interconnection. A package substrate, on which the active interposers with the qubit chips are packaged, is used for arranging a large number of wirings to connect the QA machine and room temperature electronics. In addition, bridge interposers are introduced for connecting the adjacent active interposers on the package substrate.

We estimate an occupation area per qubit to be 6400 μm² including the peripheral solder-bump bonding pads, suggesting a possible integration of 62 thousand qubits on a 20-mm-square chip. With these numbers, we simply expect factoring of a 512-bit number by a QA machine consisting of 100 qubit chips on a 250-mm-square package substrate (Fig. 6). Perhaps the number of bits to be factored, 512, is not very impressive but nevertheless the integration scale, 6 million qubits, is very challenging. Reduction of the number of the qubits is critical for constructing practical-scale QA machines for practical problems. Efficient designs of the QA Boolean logic circuits with the smaller number of qubits are discussed in detail elsewhere [17]. There also remain a lot of issues to be considered, e.g., a method of calibrating the individual qubits, arrangements of the fine tuning mechanisms such as the CCJ SQUID and Iqp compensator [8]-[10], and reduction of the number of cables between low and room temperatures.

V. SUMMARY

We have designed a superconducting QA machine to perform prime factoring for analyzing RSA cryptosystem. The operation principle is the unitary reversibility of a multiplier composed of QA Boolean logic circuits. A new concept of an ASAC architecture efficiently utilizes the limited hardware budget in superconducting integrated circuit technology in exchange for the restriction of the functionality. A practical-scale ASAC QA factoring machine is to be realized in a three-dimensional QUIP packaging structure.

ACKNOWLEDGMENT

We are grateful to T. Endo, G. Fujii, M. Hioki, K. Inomata, T. Katashita, K. Kikuchi, S. Kohjiro, S. Nagasawa, T. Nakagawa, M. Ukibe, T. Yamada, and H. Yamamori for valuable discussions.

REFERENCES

[1] P. W. Shor, “Algorithm for quantum computation: discrete logarithms and factoring,” in Proceedings of 35th Annual Symposium on Foundations of Computer Science, IEEE press, Los Alamitos, CA, 1994.
[2] M. A. Nielsen and I. L. Chuang, Quantum Computation and Quantum Information: 10th Anniversary Edition, Cambridge University Press, 2010.
[3] A. Ekert and R. Jozsa, “Quantum computation and Shor's factoring algorithm,” Rev. Mod. Phys., vol. 68, pp. 733-753, July 1996.
[4] P. Kaye, R. Laflamme, and M. Mosca, An Introduction to Quantum Computing, Oxford University Press, 2007.
[5] R. L. Rivest, A. Shamir, and L. Adleman, “A method for obtaining digital signatures and public-key cryptosystems,” Commun. ACM, vol. 21, pp. 120-126, February 1978.
[6] T. Kadowaki and H. Nishimori, “Quantum annealing in the transverse Ising model,” Phys. Rev. E, vol. 58, pp. 5355-5363, November 1998.
[7] D-Wave Systems, Inc., https://www.dwavesys.com/
[8] R. Harris et al., “Experimental investigation of an eight-qubit unit cell in a superconducting optimization processor,” Phys. Rev. B, vol. 82, 024511, July 2010.
[9] M. W. Johnson et al., “Quantum annealing with manufactured spins,” Nature, vol. 473, pp. 194-198, May 2011.
[10] P. I. Bunyk et al., “Architectural considerations in the design of a superconducting quantum annealing processor,” IEEE Trans. Appl. Supercond., vol. 24, 1700110, August 2014.
[11] C. C. McGeoch, Adiabatic Quantum Computation and Quantum Annealing: Theory and Practice, Morgan & Claypool, 2014.
[12] K. Imafuku, T. Katashita, S. Kawabata, H. Koike, and M. Maezawa, “Inverting Boolean function with annealing computation -- its potential application to cryptanalysis,” presented to Adiabatic Quantum Computing Conference 2016 (AQC2016), Venice, USA, June 27, 2016.
[13] Y. Nakamura, Yu. A. Pashkin, and J. S. Tsai, “Coherent control of macroscopic quantum states in a single-Cooper-pair box,” Nature, vol. 398, 786-788, April 1999.
[14] J. Kelly et al., “State preservation by repetitive error detection in a superconducting quantum circuit,” Nature, vol. 519, pp. 66-69, March 2015.
[15] S. Nagasawa and M. Hidaka “Run-to-run yield evaluation of improved Nb 9-layer advanced process using single flux quantum shift register chip with 68,990 Josephson junctions,” unpublished.
[16] V. K. Semenov, Y. A. Polyanov, and S. K. Tolpygo, “AC-biased shift registers as fabrication process benchmark circuits and flux trapping diagnostic tool,” IEEE Trans. Appl. Supercond., vol. 27, 1301409, June 2017.
[17] K. Imafuku, unpublished.