Automatic Generation of Equivalent Electrothermal SPICE Netlists from 3D Electrothermal Field Models

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Abstract—Starting from a 3D electrothermal field problem discretized by the Finite Integration Technique, the equivalence to a circuit description is shown by exploiting the analogy to the Modified Nodal Analysis approach. Using this analogy, an algorithm for the automatic generation of a monolithic SPICE netlist is presented. Joule losses from the electrical circuit are included as heat sources in the thermal circuit. The thermal simulation yields nodal temperatures that influence the electrical conductivity. Apart from the used field discretization, this approach applies no further simplifications. An example 3D chip package is used to validate the algorithm.

I. INTRODUCTION

For many electrothermal applications, complex problems need to be solved to calculate the desired quantities of interest. While analytical methods only serve for very simple problems, real world problems require numerical field simulations. Nowadays, Finite Difference (FD), Finite Element (FE) or Finite Volume (FV) methods are well known and frequently applied. On the other hand, when a fast computation is required, it is often recommended to derive a model that only consists of a few lumped elements which allows to use circuit simulators. However, network models are not always sufficiently accurate or they are too complex to be generated by hand compared to models based on partial differential equations. This paper attempts to fill this gap by deriving a circuit netlist from a field model, thereby avoiding any further approximation.

When the first circuit simulators were introduced, the Simulation Program with Integrated Circuit Emphasis (SPICE) soon became the standard tool for describing and solving circuits using netlists. At that time, the operating temperature of the simulated devices was set globally and did not change according to the operational load of the circuit. However, especially in power electronic applications that involve strongly temperature dependent materials [1], [2], self-heating and thermal coupling between devices become important and therefore the device’s temperature changes dynamically. Thus, the concurrent simulation of electrical and thermal circuits was soon developed as a SPICE extension [3]. To account for the coupling, an extra temperature node was added to the electrical device models [4], [5].

Traditionally, the circuit topology and the netlist parameters are determined by hand calculations which necessarily neglect nonlinear effects and field inhomogeneities. Nowadays, the thermal behavior is more accurately analyzed by 3D field solvers which allow to couple the resulting temperature distribution iteratively to the electric circuit simulator, known as the relaxation method [6], [7], [8]. On the other hand, the definition of mesh-based equivalent thermal circuits [9] motivates the direct method that couples the electrical and thermal circuits without any 3D field solver required. Following the direct approach, this work aims at exploiting the accurate electrothermal field model by automatic and loss-free extraction of an equivalent electrothermal circuit model (as visualized in Fig. 1). The netlists generated by this approach are therefore an exact representation of the nonlinear FD, FE or FV field discretizations. Moreover, a straightforward coupling with an additional (external) SPICE circuitry is possible and standard techniques of model order reduction for networks [10] can be applied afterwards.

If a 3D electrothermal field model is investigated, occasionally surrounding circuitry is treated by a field-circuit coupled approach [11], [12]. In some cases, a two-step procedure is executed, i.e., from the field model part, a reduced model is extracted and then included in a circuit model [13]. In this paper, a further alternative is proposed, i.e., the full field model is translated into a circuit model. This approach is promising for small device parts with severe electrothermal issues, to be embedded in an overall circuit model.

Figure 1: Visualization of the approach to extract lumped elements from a 3D field model.
The paper is organized as follows: The electrothermal field problem is introduced in section II. Then, section III presents the discretization by the Finite Integration Technique (FIT). This technique is based on integral-type degrees of freedom and therefore allows a straightforward circuit interpretation as demonstrated in section IV. The details of the automatic SPICE netlist generation are given in section V. Finally, numeric validation examples are discussed in section VI before section VII concludes the paper.

II. ELECTROTHERMAL FIELD PROBLEM

We consider an electrothermal problem that couples the electroquasistatic approximation of Maxwell’s equations [14] with the transient nonlinear heat equation

\[-\nabla \cdot (\sigma \nabla \tilde{\varphi}(t)) - \nabla \cdot (\lambda(T) \nabla T(t)) = Q_{el}(\varphi), \tag{1} \]

subject to adequate initial and boundary conditions. The given quantities are the Joule heating term \(Q_{el}(\varphi) = \sigma(T) \nabla \varphi \cdot \nabla \varphi\), the time \(t\), the temperature \(T\) and the electric scalar potential \(\varphi\). The material parameters \(\varepsilon, \sigma, \lambda, \rho\) and \(c\) are the electrical permittivity and conductivity, the thermal conductivity, the volumetric mass density and the specific heat capacity, respectively. All involved materials may be nonlinear, inhomogeneous or anisotropic. Note that the spatial dependencies have been suppressed here and that the temperature dependency of \(\rho\) and \(c\) is neglected.

III. DISCRETIZATION BY THE FINITE INTEGRATION TECHNIQUE

The coupled electrothermal problem given by (1) and (2) is discretized in space by the Finite Integration Technique (FIT) on a staggered 3D hexahedral grid with \(n\) canonically indexed nodes [15, 16, 17]. The discretization turns the material relations and the differential operators into material matrices and topological matrices, respectively. The discrete unknowns, i.e., the electric potentials \(\tilde{\Phi} \in \mathbb{R}^n\) and the temperatures \(\tilde{T} \in \mathbb{R}^n\) are associated with the nodes of the primary grid (see Fig. 2). The voltage and temperature drops are allocated at the primary edges and resemble differences, i.e., \(\tilde{e} = -G\tilde{\Phi}\) and \(\tilde{t} = -GT\tilde{T}\), where \(G \in \{-1, 0, 1\}^{3n \times n}\) is the discrete gradient matrix according to the topology of the primary grid. The electrical currents \(\tilde{j}\) and heat fluxes \(\tilde{q}\) are assigned to the faces of the dual grid. They are accumulated on the dual cells by \(S \tilde{j}\) and \(S \tilde{q}\) where \(S \in \{-1, 0, 1\}^{n \times 3n}\) is the discrete divergence matrix determined by the topology of the dual grid. The duality of the staggered grid gives raise to the property \(G = -S^T\).

Note that the signs of the different entries of \(G = [P_{x}, P_{y}, P_{z}]^T\) (and thus also \(S\)) define the orientation of the grid’s edges. Here, their direction is chosen to be the same as the direction of the coordinate axes. The \(n \times n\) sub-matrices \(P_{\xi}\) with \(\xi \in \{x, y, z\}\) are therefore the discrete representation of the spatial derivatives \(\frac{d}{dx}, \frac{d}{dy}\) and \(\frac{d}{dz}\). This results in \(-1\) entries on the main diagonals of \(P_{\xi}\) and in \(+1\) entries on one of the super-diagonals. The discrete gradient matrix \(G\) resembles an incidence matrix as used in circuit theory that is more structured than a typical circuit incidence matrix. Both matrices share the property that their column sums are zero.

The discrete unknowns at the primary grid are related to the ones at the dual grid by material matrices, i.e., the electrical conductance matrix \(M_{e} \in \mathbb{R}^{3n \times 3n}\), the electrical capacitance matrix \(M_{\varepsilon} \in \mathbb{R}^{3n \times 3n}\), the thermal conductance matrix \(M_{\lambda} \in \mathbb{R}^{3n \times 3n}\) and the thermal capacitance matrix \(M_{\rho c} \in \mathbb{R}^{3n \times 3n}\). The electrical currents, displacement currents, heat fluxes and stored heats are then given by

\[\tilde{j} = M_{e} \tilde{e}, \quad \tilde{d} = M_{\varepsilon} \tilde{e}, \quad \tilde{q} = M_{\lambda} \tilde{t} \quad \text{and} \quad Q = M_{\rho c} \tilde{T},\]

respectively. In case of a mutually orthogonal grid pair, the material matrices are diagonal. Then, each primary edge crosses the corresponding dual facet perpendicularly. The primary edge and facet as well as the primary nodes and dual cells are indexed pairwise identically. This gives the entries of \(M_{e}, M_{\varepsilon}, M_{\lambda}\) and \(M_{\rho c}\) as

\[M_{e,j,j} = \frac{\sigma_j |A_j|}{|L_j|}, \quad M_{\lambda,j,j} = \frac{\lambda_j |A_j|}{|L_j|}, \quad \text{and} \quad M_{\rho c;i,i} = \frac{\rho c_i |V_i|}{|L_j|},\]

where \(|L_j|\) is the length of the primary edge \(L_j\), \(|A_j|\) is the area of the dual facet \(A_j\) and \(|V_i|\) is the volume of dual cell \(V_i\). The material parameters \(\sigma_j, \lambda_j, A_j\) and \(\rho c_i\) are found by averaging the corresponding parameters, cf. [18, 19]. Note that the counter \(i\) addresses all primary nodes (or dual volumes) while \(j\) addresses all primary edges (or dual facets).

The applied averaging scheme depends on the allocation of the materials on the grid. In this paper, the material properties are allocated at the primary grid cells, i.e., each primary cell contains a homogeneous material. This gives rise to the so-called staircase approximation. Although this paper adopts this approximation for reasons of conciseness, partially filled cells [20] and conforming techniques [21] are preferred. According to the chosen allocation scheme (see Fig. 2), the averaging of a conductance for a primary-edge, dual-facet pair involves

![Figure 2: Allocation of electrical and thermal quantities at the primary and dual grid.](image)
four surrounding primary volumes resulting in the average of the four involved conductivities. For an equidistant grid, this gives

$$\sigma_j = \frac{1}{4} \sum_{p=1}^{4} \sigma_p,$$  \hspace{1cm} (3)$$

with \( p \) being a local counter over the four primary volumes \( V_p \) that share the edge \( L_j \). Note that this averaging scheme can easily be generalized for non-equidistant grids by taking the different cell sizes into account.

The heat powers generated by the thermal losses from the electroquasistatic problem are calculated by

$$\hat{Q}_{el} = \hat{\mathbf{e}} \odot \hat{\mathbf{J}},$$

with the component-wise Hadamard product \( \odot \) and the vector \( \hat{\mathbf{Q}}_{el} \in \mathbb{R}^{4n \times 1} \) that allocates the thermal losses at the shifted cells \( \hat{V}_j \) with the volume \(|\hat{V}_j| = |A_j||L_j|\) as shown in Fig. 3. The shifted cells consist of two half dual cells sharing a common dual facet and are indexed according to the dual facets.

To include all calculated heat contributions as sources in the heat equation, they need to be integrated from the shifted volumes \( \hat{V}_j \) to the neighboring dual cells \( \tilde{V}_i \). This relation is given by

$$Q_{el,i} = \sum_{p=1}^{6} \frac{|\tilde{V}_i|}{2|V_p|} \hat{Q}_{el,p},$$

where \( p \) is a local counter that loops over all shifted cells that intersect the dual cell \( i \). To sum up all contributions of the shifted volumes to the dual cell \( \tilde{V}_i \), the incidence matrix \( \mathbf{P}_{Q} \in \{0,1\}^{n \times 3n} \) is defined. Then, the Joule losses \( Q_{el} \in \mathbb{R}^n \) on the dual cells become

$$Q_{el} = \frac{1}{2} \tilde{D}_{\mathbf{V}} \mathbf{P}_{Q} \tilde{D}_{\mathbf{V}}^{-1} \hat{\mathbf{Q}}_{el}.$$  \hspace{1cm} (4)$$

Here, \( \tilde{D}_{\mathbf{V}} \in \mathbb{R}^{n \times n} \) and \( \tilde{D}_{\mathbf{V}} \in \mathbb{R}^{3n \times 3n} \) are diagonal matrices containing the dual volumes \(|\tilde{V}_i|\) and the shifted volumes \(|\hat{V}_j|\), respectively.

Finally, the topological operators \( \tilde{\mathbf{S}} \) where \( \tilde{\mathbf{S}}^\top = -\mathbf{G} \), the material matrices \( \mathbf{M}_{\sigma}, \mathbf{M}_{\epsilon}, \mathbf{M}_{\lambda} \) and \( \mathbf{M}_{pc} \) and the heat powers \( \mathbf{Q}_{el} \) are utilized to express the discrete counterpart of (1) and (2), i.e.,

$$\tilde{\mathbf{S}} \mathbf{M}_{\sigma} \tilde{\mathbf{S}}^\top \Phi + \tilde{\mathbf{S}} \mathbf{M}_{\epsilon}(\mathbf{T}) \tilde{\mathbf{S}}^\top \Phi = 0,$$  \hspace{1cm} (5)$$

$$\mathbf{M}_{pc} \tilde{\mathbf{T}} + \tilde{\mathbf{S}} \mathbf{M}_{\lambda}(\mathbf{T}) \tilde{\mathbf{S}}^\top \mathbf{T} = \mathbf{Q}_{el}(\Phi).$$  \hspace{1cm} (6)$$

The equivalence between the discretized FIT formulations (5) and (6) and the Modified Nodal Analysis (MNA) \cite{22,23} becomes obvious when the latter is derived from the Maxwell equations along a similar reasoning as in section III. First, Kirchhoff’s Voltage Law (KVL) and Kirchhoff’s Current Law (KCL) are derived directly from Faraday’s law and the current continuity equation, respectively. Then, they are assembled together with the branch relations to give a circuit formulation. From this, the electric and thermal equivalences to the FIT formulation are obtained.

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{fig3.png}
\caption{Visualization of the shifted volume \( \tilde{V}_j \).}
\end{figure}

\textbf{A. Kirchhoff’s Voltage Law (KVL)}

In the electroquasistatic case, Faraday’s law reads

$$\oint_{\partial A_{loopt}} \vec{E} \cdot d\vec{s} = 0,$$

where \( A_{loopt} \) is the surface enclosed by the loop such that \( \partial A_{loopt} = \bigcup_{j=1}^{b} L_j \), with \( b \) branches \( L_j \). Loops in a circuit closely resemble loops in the primary grids, i.e., a loop is a collection of edges and nodes forming a closed path. The integral form of Faraday’s law directly breaks down in an addition of voltage drops \( V_j \) along the branches \( L_j \) giving

$$\oint_{\partial A_{loopt}} \vec{E} \cdot d\vec{s} = \sum_{j=1}^{b} \int_{L_j} \vec{E} \cdot d\vec{s} = \sum_{j=1}^{b} V_j = 0.$$  \hspace{1cm} (7)$$

In MNA, (7) is implicitly fulfilled by defining the \( n \) nodal voltages \( v_i \) and expressing the branch voltages \( V_j \) by

$$\mathbf{V} = \mathbf{A}^\top \mathbf{v},$$

where \( \mathbf{A} \in \{-1,0,1\}^{n \times b} \) is the circuit incidence matrix. In analogy to the FIT matrix \( \mathbf{G} \) (cf. section III), the entries \( a_{ij} \) of \( \mathbf{A} \) have to be subject to a convention. Let us define \( a_{ij} = +1 \) if branch \( L_j \) is directed away from node \( i \) and \( a_{ij} = -1 \) if branch \( L_j \) is directed towards node \( i \). If branch \( L_j \) is not directly connected to node \( i \), the corresponding entry \( a_{ij} \) is zero. The nodal voltages \( \mathbf{v} \) are the circuit counterpart of the electric potentials \( \Phi \) in the FIT formulation. Note that in the electrical case, at least one of the \( n \) potentials needs to be chosen as the reference potential (ground) to ensure uniqueness of the solution.
B. Kirchhoff’s Current Law (KCL)

The KCL is derived from the current continuity equation

$$\int_{\partial V} \mathbf{J} \cdot d\mathbf{A} = \int_V \dot{\mathbf{J}} \, dV,$$

(8)

where $\rho(\vec{r}, t)$ is the charge density and $V$ an arbitrary cell. In analogy to FIT, we consider a cell $\bar{V}$ around a node $i$ of the circuit. Furthermore, we assume that the total charge in $\bar{V}$ is zero. This means that capacitive charges are located on branches that are either fully outside or fully inside $\bar{V}$. Then, (3) becomes

$$\int_{\partial \bar{V}_i} \mathbf{J} \cdot d\mathbf{A} = 0,$$

with the boundary $\partial \bar{V}_i$ of $\bar{V}_i$. Assuming that a finite number $s$ of conductors with cross-sectional areas $A_j$ and currents $I_j$ are leaving this cell, KCL is obtained as

$$\sum_{j=1}^s I_j = \sum_{j=1}^s \int_{A_j} \mathbf{J} \cdot d\mathbf{A} = 0.$$

Using the definition of the circuit incidence matrix,

$$\mathbf{A} \mathbf{I} = 0$$

states KCL for every node in the network. Note that $\mathbf{0}$ denotes a vector of zeros of suitable dimension.

C. Branch Relations

Due to the nature of the considered problem, we limit ourselves to resistances, capacitances and current sources as branch elements. With $b_R$ resistive branches, $b_C$ capacitive branches and $b_I$ current sources, $\mathbf{A}$ can be divided into two blocks representing these elements. We therefore obtain

$$\mathbf{A} = [\mathbf{A}_R \quad \mathbf{A}_C \quad \mathbf{A}_I],$$

where $\mathbf{A}_R \in \{-1,0,1\}^{n \times b_R}$, $\mathbf{A}_C \in \{-1,0,1\}^{n \times b_C}$ and $\mathbf{A}_I \in \{-1,0,1\}^{n \times b_I}$. The vector of currents is partitioned accordingly, i.e.,

$$\mathbf{I}^T = [\mathbf{I}_R^T \quad \mathbf{I}_C^T \quad \mathbf{I}_I^T],$$

with the blocks $\mathbf{I}_R \in \mathbb{R}^{b_R}$, $\mathbf{I}_C \in \mathbb{R}^{b_C}$ and $\mathbf{I}_I \in \mathbb{R}^{b_I}$. Similarly, with $\mathbf{V}_R \in \mathbb{R}^{b_R}$, $\mathbf{V}_C \in \mathbb{R}^{b_C}$ and $\mathbf{V}_I \in \mathbb{R}^{b_I}$, the branch voltage vector is partitioned as

$$\mathbf{V}^T = [\mathbf{V}_R^T \quad \mathbf{V}_C^T \quad \mathbf{V}_I^T].$$

With these definitions, KVL and KCL are expressed by

$$\mathbf{V}_R = \mathbf{A}_R^T \mathbf{V}, \quad \mathbf{V}_C = \mathbf{A}_C^T \mathbf{V}, \quad \mathbf{V}_I = \mathbf{A}_I^T \mathbf{V}$$

and

$$\mathbf{A}_R \mathbf{I}_R + \mathbf{A}_C \mathbf{I}_C + \mathbf{A}_I \mathbf{I}_I = \mathbf{0}.$$  

(9)

(10)

The introduction of the diagonal conductance matrix $\mathbf{G} \in \mathbb{R}^{b_R \times b_R}$ and the diagonal capacitance matrix $\mathbf{C} \in \mathbb{R}^{b_C \times b_C}$ with the corresponding values on the diagonal leads to the branch relations

$$\mathbf{I}_R = \mathbf{G} \mathbf{V}_R, \quad \mathbf{I}_C = \mathbf{C} \dot{\mathbf{V}}_C \quad \text{and} \quad \mathbf{I}_I = \mathbf{I}_s(t),$$

where $\mathbf{I}_I = \mathbf{I}_s(t)$ is an arbitrary source current.

The combination of KVL, KCL and the branch relations gives the MNA formulation

$$\mathbf{A}_C \mathbf{G} \mathbf{A}_C^T \dot{\mathbf{V}} + \mathbf{A}_R \mathbf{G} \mathbf{A}_R^T \mathbf{V} = -\mathbf{A}_I \mathbf{I}_s(t).$$

(11)

D. Circuit Formulation and Electrical Equivalences

For the EQS case, when comparing the structure of (5) and (6) with (11), many equivalences are found. Thanks to the equally chosen orientation of the edges in the FIT grid in comparison to the edges in the MNA, the discrete field formulation can be interpreted as a circuit formulation by setting

$$\mathbf{A}_C^{\text{el}} = \mathbf{A}_R^{\text{el}} = \mathbf{S}, \quad \mathbf{C}_v^{\text{el}} = \mathbf{M}_v, \quad \mathbf{G}_v^{\text{el}} = \mathbf{M}_R, \quad \mathbf{I}_s^{\text{el}} = \mathbf{0} \quad \text{and} \quad \mathbf{v}^{\text{el}} = \mathbf{\Phi},$$

with the superscript $\text{el}$ denoting the quantities for the electro-quasistatic case.

E. Thermal Circuit and Equivalences

In a thermal circuit, heat capacitances connect the circuit nodes to a common node (thermal ground) with zero temperature. This reflects the different nature of the term $\mathbf{M}_{th}$ in (3) compared to the term $\mathbf{S} \mathbf{M}_{th} \mathbf{S}^T \mathbf{\Phi}$ in (5).

With node $n + 1$ as the thermal ground node, (11) becomes

$$\mathbf{A}_C^{\text{th}} \mathbf{A}_C^{\text{th}} T \dot{\mathbf{v}} + \mathbf{A}_R^{\text{th}} \mathbf{G} \mathbf{A}_R^{\text{th}} T \mathbf{v} = -\mathbf{A}_I \mathbf{I}_s(t)$$

(13)

with $\mathbf{A}_C^{\text{th}} \in \{-1,0,1\}^{(n+1) \times b_R}$, $\mathbf{A}_R^{\text{th}} \in \{-1,0,1\}^{(n+1) \times b_C}$, $\mathbf{A}_I^{\text{th}} \in \{-1,0,1\}^{(n+1) \times b_I}$ and $\mathbf{v} \in \mathbb{R}^{n+1}$ being the expansion of the corresponding quantities by this additional node. To mirror the structure of the discretized heat equation (3), we set the potential $v$ of the thermal ground node to zero and choose

$$\mathbf{A}_C^{\text{th}} = [\mathbf{I} - \mathbf{1}], \quad \mathbf{A}_R^{\text{th}} = [\mathbf{A}_R \quad 0],$$

$$\mathbf{A}_I^{\text{th}} = [\mathbf{I} - \mathbf{1}] \quad \text{and} \quad \mathbf{v} = [\mathbf{v}_{\text{gnd}}].$$

Here, $\mathbf{I}$ is the $n \times n$ identity matrix and $\mathbf{1}$ is a vector of ones with dimension $n$. If we then omit line $n + 1$ in (13) (as we would do with a ground node in an electric circuit), we end up with (11) again and obtain

$$\mathbf{A}_C^{\text{th}} = \mathbf{A}_I^{\text{th}} = \mathbf{I}, \quad \mathbf{A}_R^{\text{th}} = \mathbf{S}, \quad \mathbf{G}_v^{\text{th}} = \mathbf{M}_R, \quad \mathbf{G}_v^{\text{th}} = \mathbf{M}_R, \quad \mathbf{I}_s^{\text{th}} = -\mathbf{Q}_{el} \quad \text{and} \quad \mathbf{v}^{\text{th}} = \mathbf{T},$$

with the superscript $\text{th}$ denoting the quantities for the thermal problem.

The equivalences between the FIT formulation (5) and (6) and the circuit formulation (11) as shown above are the main motivation for this paper. The relations (12) and (14) allow to derive an equivalent SPICE netlist from any given 3D problem discretized by the FIT. The detailed methodology and numerical examples are discussed in the remaining sections of the paper.
V. SPICE NETLIST GENERATION

This section deals with the implementation details for the automated netlist generation. First, the topology of the generated network is described for the EQS problem including the extraction of the Joule loss term. Then, the topology of the thermal network with inclusion of the Joule loss term is discussed. In the second part of the section, the approach for nonlinear material relations is shown.

A. Circuit Topology

For the EQS problem, the degrees of freedom in the FIT are the potentials \( \Phi \) allocated at the primary nodes. In the MNA, these potentials are placed on the nodes of the network and thus remain nodal values. From the previous section, we know that the branch voltages of capacitive and resistive branches are equal, cf. [9] and [17]. Therefore, these elements are placed in parallel. With the definition of the voltages \( V^e_R = V^e_C = S^T \Phi \) as the difference of two nodal potentials, the resistive and capacitive elements are located on the branches between the nodes. From the pair-wise equality of \( M_{\sigma} \) and \( G \) as well as \( M_L \) and \( C \), the entries \( M_{\sigma,i,j} \) and \( M_{el,i,j} \) from the material matrices are the values for the lumped conductances and capacitances on circuit branch \( L_j \), respectively. To impose inhomogeneous Dirichlet boundaries, voltage sources between a Dirichlet node and ground have to be defined. Fig. 4a shows the structure of the described electrical circuit for one example branch between nodes \( i \) and \( i+1 \).

Since each branch contains resistive elements, the thermal losses need to be calculated on every branch. For branch \( L_j \), this is achieved by the evaluation of the branch voltage \( U_j \) and the current \( I_j \) giving

\[
\hat{Q}_{el,j} = U_j I_j.
\]

Note that this thermal power \( \hat{Q}_{el,j} \) coincides with the one calculated in the field model discussed in section [II]. Writing the different \( \hat{Q}_{el,j} \) in a vector, it becomes \( \hat{Q}_{el} \) and leads to the thermal power \( Q_{el} \) on the dual volumes as given by [3].

For the thermal problem, the structure of the conductive part \( (S^T M_{\rho} S) \) is equal to the structure of the electrical problem. Therefore, as done for the electrical problem, conductive elements are placed on the branches between two circuit nodes. On the other hand, the structure of the capacitive part \( (M_{\rho c} \hat{T}) \) differs slightly from the EQS structure. Since the identity matrix is chosen for the incidence matrix of the capacitive branches \( (A^{|th}_i = I) \), the voltage \( V_C = I \) is not defined by temperature differences but by the absolute values of the temperatures (with respect to a reference temperature). If the temperature values are now allocated at the nodes of the thermal network, a capacitive connection from every thermal network node to the thermal ground as introduced in section [IV] is obtained. The values for these capacitances correspond to the values on the diagonal of \( M_{\rho c} \), cf. [14]. To include inhomogeneous Dirichlet conditions, temperature sources are modeled by voltage sources between the Dirichlet nodes and ground as done for the electrical circuit. Furthermore, the mapping of the heat powers \( Q_{el} \) to a circuit definition is given by its incidence matrix \( A^{|th}_i = I \). Therefore, the corresponding current sources are placed between each circuit node and thermal ground. In Fig. 4b these observations are summarized for a thermal example edge.

B. Nonlinear Materials

In practice, all material properties may depend on the temperature. In this section, the dominating nonlinearity is assumed to be the electric conductivity \( \sigma \). However, other dependencies can be incorporated analogously. If an inhomogeneous material distribution is given in the domain of interest, the average conductivity has to be found as presented in section [II] to correctly consider the nonlinearity in SPICE. For the EQS problem, the degrees of freedom in the FIT are evaluated according to its nonlinear definition. In the simplest case, the temperature dependence of an isotropic conductivity is expressed via the resistivity, i.e.,

\[
\rho_p(T_j) = \frac{1}{\sigma_p(T_j)} = \rho_{0,p} \left( 1 + \alpha_p \left( T_j - T_0 \right) \right).
\]

In this equation, \( \rho_{0,p} \) is the resistivity at the reference temperature \( T_0 \) and \( \alpha_p \in \mathbb{R} \) the temperature coefficient depending on the material of cell \( V_p \). Once the nonlinear functions have been evaluated, the average conductivity \( \sigma_j \) of edge \( L_j \) can be found as given by [5]. Then, the nonlinear conductance \( R_j(T_j) \) is established by the length \( |L_j| \) of primary edge \( L_j \) and the area \( |A_j| \) of dual facet \( A_j \), giving

\[
R_j(T_j) = \frac{1}{\sigma_j(T_j)} |A_j|/|L_j|.
\]

Note that more complex material laws, non-equidistant grids and a more sophisticated averaging can be implemented analogously.

A pseudocode for the generation of electrothermal netlists with nonlinearities is shown in Algorithm [I].
Algorithm 1 SPICE netlist generation algorithm

1: for edge \( E_j \) between primary nodes \( i \) and \( k \) do
2: write \( R_{el}(j) \) node(i) node(k) \( R_j(T_j) \)
3: write \( C_{el}(j) \) node(i) node(k) \( M_{el}(j, j) \)
4: write \( R_{th}(j) \) node(i) node(k) \( M_{th}^{-1}(j, j) \)
5: write \( C_{th}(i) \) gnd node(i) \( M_{th}(i, i) \)
6: write \( I_{Loss} \) gnd node(i) \( Q_{el,i} \)
7: if \( i \) is electric Dirichlet node then
8: write \( V_{dir,el}(i) \) node(i) gnd \( V_{Dir,i} \)
9: end if
10: if \( i \) is thermal Dirichlet node then
11: write \( V_{dir,th}(i) \) node(i) gnd \( T_{Dir,i} \)
12: end if
13: end for

Table 1: Material properties of the benchmark example.

| Property | \( 0 < x < \ell \) | \( \ell < x < \ell + d \) |
|----------|-----------------|-----------------|
| \( \sigma \) (S/m) | 3 | 0 |
| \( \varepsilon_i \) | 1 | 1.13 \times 10^5 |
| \( \lambda \) (W/K/m) | 400 | 400 |
| \( \rho_c \) (I/K/m^3) | 8000 | 8000 |

VI. NUMERICAL VALIDATION

A. Benchmark Example

For validation of the presented methodology, a benchmark cuboid of dimensions 4 mm \( \times \) 1 mm \( \times \) 1 mm is selected. It is composed of two different regions as shown in Fig. 5. The left part of length \( \ell = 3 \) mm is chosen to be mainly resistive while the right part of length \( d = 1 \) mm is mainly capacitive. The material properties of the two regions are summarized in Table 1. On the boundaries in \( x \)-direction, Perfect Electric Conducting (PEC) facets are assumed. At the left boundary, a sinusoidal electric Dirichlet condition with 1 kV amplitude and a frequency of 76.9 kHz is imposed. At the right boundary, a potential of 0 V is applied. Homogeneous Neumann conditions are chosen for the remaining boundaries. Thermally, all boundaries are set to homogeneous Neumann (thus adiabatic) conditions. For the initial conditions, all electric and thermal non-Dirichlet nodes are set to zero.

From a circuit point of view, the electric Dirichlet condition is modeled by a voltage source \( V_{Dir} \) as the potential difference between the facets. Furthermore, the resistive material is modeled by a single resistance and the capacitive material by a single capacitor. However, the thermal properties of the two materials are assumed to be equal.

After setting up the model with its material properties and boundary conditions, Algorithm 1 generates an equivalent electrothermal netlist. Then, using this netlist, a SPICE simulation is carried out and compared with the electrothermal FIT simulation. The electrical simulation result is shown in Fig. 6. From the obtained potentials \( \Phi \), the thermal loss term \( Q_{el} \) is calculated. These losses are then coupled into the heat equation yielding the resulting temperatures as shown in Fig. 7.

From all three figures, it is clearly seen that a very good agreement of the SPICE and FIT simulation is achieved. The relative error norm for the obtained temperature is calculated as

\[
\text{error} = \frac{\max_i ||T_{SPICE}(t_i) - T_{FIT}(t_i)||_2}{\max_i ||T_{FIT}(t_i)||_2} \approx 0.52 \%,
\]

where \( T_{SPICE} \) and \( T_{FIT} \) are \( n_t \) vectors of dimension \( n \) with \( n_t \) being the number of time steps. Since the spatial discretization is chosen identically and the generated netlist is a representation of the 3D field model without any further simplifications, the only error is resulting from the different time integrators.

B. Chip Package

To apply the method to a more complex example, a microelectronic chip package as shown in Fig. 8 is considered. Here, the same setting as in [19] is chosen. However, only one bonding wire connects one of the contacts to the chip. The bonding wire’s electrical conductance is \( G_{bw}^d = 1 \) S and its thermal conductance \( G_{bw}^t = 1 \) kW/K. Furthermore, the relative permittivity for all materials are set to one while the thermal boundary conditions are adiabatic. To excite the system, an
exponential voltage \( V_0(t) = 10 \text{V} [1 - \exp(-t)] \) is applied over the bonding wire. Algorithm [1] is executed to generate the equivalent netlist. This is simulated using SPICE and the temperature of the hottest node of the domain is compared to the result obtained by FIT as shown in Fig. 9. The error as calculated by (15) is 0.07 %. Due to the mainly resistive character of this example, the resulting constant current leads to a constant heating of the considered node.

VII. CONCLUSIONS

The automatic generation of netlists directly from an electrothermal 3D field model has been presented. Starting from a Finite Integration Technique (FIT) discretization, an equivalent circuit description in terms of the Modified Nodal Analysis (MNA) was shown for the electrical as well as for the thermal case. As it is a direct representation of the field model, no further simplifications apply when generating the netlist. For validation, the field solution of an electrothermal benchmark example and a complex 3D chip package problem have been compared to the SPICE solution based on the generated netlist.

Next steps are the treatment of non-hexahedral meshes, arbitrary nonlinear materials and model order reduction of the resulting network to reduce the complexity of the obtained circuit and thus enable a more efficient circuit simulation.

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