Design of E-mode GaN HEMTs by the Polarization Super Junction (PSJ) technology

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A B S T R A C T

In this paper, a normally-OFF high voltage GaN HFETs based on the Polarization Super Junction (PSJ) concept has been presented. In this new device, threshold voltage (V_TH) can be controlled by adjusting the etching depth of the recessed region without modifying on-resistance (R_{ON}) characteristics. The threshold voltage of E-mode device increased to 2 V while the threshold voltage for experimental D-mode structure was about −4 V. The challenge of achieving high breakdown voltage (BV) with minimum on-resistance has been addressed by the lateral scaling of recessed region to achieve an improved figure of merit (FOM). The specific on-resistance of the proposed E-mode PSJ HFET is maintained low while the BV of the device increases from 560 V to 800 V of the D-mode PSJ HFET with the same dimensional parameters.

1. Introduction

GaN high electron mobility transistors (HEMTs) are good candidates for high power, high frequency, and low loss applications because of their high critical breakdown field [1]. Due to high electron density two-dimensional (2D) and high electron mobility, GaN transistors are emerging as commercial products. The development roadmap of GaN power semiconductor devices is currently geared towards power conversion systems with voltage rating between 600 V and 1.2 kV [2]. Several termination techniques have been proposed to improve the BV, such as field plate [3], fluorine ion implantation [4], and recessed gate-edge termination [5,6].

An alternative solution for manufacturing low cost high voltage GaN power switching devices that can overcome reliability and cost challenge is the Polarization Super Junction (PSJ) technology that is promising candidate for fully GaN based power ICs. Polarization Super Junction (PSJ) is unique technique to achieve charge balance not through impurity based doping control, but by engineering of positive and negative polarization charges inherent in the GaN materials. PSJ technology is based on a GaN/AlGaN/GaN double heterostructure there both 2DEG and 2DHG are well-confined to quantum wells and possess enhanced mobility with negligible impurity scattering [7].

PSJ technology offers no current collapse due to effective lateral charge balance and field distribution by compensation of positive and negative polarization charge [8]. PSJ offers lower saturation currents than conventional HEMTs [9], while maintaining ultra-low on-state resistance. Another attribute of the PSJ technology is that CMOS inverter operation of monolithic P and N channel MOSFETs has been demonstrated [10].

GaN PSJ HFET devices have been demonstrated for the first time by the cooperation of university of Sheffield, U.K. and POWDEC KK, Japan [8,11]. PSJ technology has been offered a depletion mode device with normally-ON characteristics. For automotive electronics, power transformation, motor drives, industrial control and wireless communication applications, a high-performance enhancement-mode (E-mode) channel devices with normally-OFF characteristic are of desirable interest from the perspective of safety and energy saving. So, E-mode HFETs are the main issue in PSJ technology. Normally-OFF devices without a gate voltage during the off state, can decrease the static power loss causes by the leakage current.

Achieving normally-OFF GaN PSJ HEMTs with the high breakdown voltage (BV) and low on resistance (R_{ON}) is one of the most important design targets in this paper. It is of great importance to improve the BV, especially neither at the cost of increasing the device size or increasing R_{ON}. In this work, a comparison of the fabricated conventional GaN PSJ HFETs (D-mode) and the E-mode proposed structure will be presented.

2. Device structure and fabrication process

Fig. 1 shows the schematic of a GaN PSJ HFET with recessed i-GaN top layer. Our unique design with locally recessed i-GaN top layer, delivers a normally-OFF GaN PSJ HFET that is suitable for power electronics applications. For conventional GaN HFET devices, it has been experimentally verified that the recessed structure is useful to shift the threshold voltage without degradation of R_{ON}-BV trade-off characteristics.
The positive threshold voltage in this technology is attributed to the recessed top i-GaN layer at GaN/AlGaN/GaN super heterojunction, which eliminates the 2DEG under the base region which enhances the threshold voltage of the HFET. Furthermore, the 2DEG remaining in the channel except for the recessed i-GaN region enabled device to maintain a low on-state resistance.

Providing of a prototype of E-mode GaN device is more complicated and expensive than its D-mode counterparts due to some additional steps. Here, an experimental procedure to develop the new E-mode super HFET is proposed. This latter is based on methods used to process D-mode super HFET [8], except that one etching step and one a mask preparation added.

In this prototype, a super junction GaN/AlGaN/GaN structure is grown by metal organic chemical vapor deposition on a sapphire substrate (Fig. 1). The epitaxial growth initiates with a high-resistance undoped-GaN buffer layer (1.5 μm). Subsequently, in a 47-nm-thick undoped AlGaN layer with an Al composition of 23%, the grown AlGaN layer of 47 nm is thicker than those used in conventional HFETs in order to obtain high-density 2DHG.

A part of AlGaN layer is etched, the dimension of the etched region is determined by the optimization done through simulations. Then an undoped GaN layer is deposited in the etched region and another 10-nm-thick undoped GaN layer is grown on top of it to create edge 2 in the structure. 2DHG and 2DEG are formed at the upper GaN/AlGaN and bottom AlGaN/GaN interfaces, respectively (Fig. 1). A 30-nm-thick Mg-doped (3 × 10^{19} cm^{-3}) p-GaN layer is grown on the undoped GaN layer to form an ohmic contact to 2DHG. A small difference between the densities of 2DHG and 2DEG can be explained by p-type doping in the top p-GaN layer. The conventional HFETs have no base electrode or 2DHG. The source and drain ohmic electrodes (Ti/Al/Ti/Au) have been deposited on the AlGaN surface and annealed under N₂ ambient at 800°C. The gate and base electrodes have been formed using Ni/Au on the AlGaN and p-GaN layers, respectively, and are annealed in air at 600°C to decrease the contact resistance of the base electrode. Finally, a 300-nm-thick SiO₂ deposited by a Plasma Enhanced Chemical Vapor Deposition (PECVD) system is used as the passivation layer. The gate–source distance and the gate lengths of super HFETs are 3 and 3 μm, respectively. The gate–drain length L_{GD} is 10 μm. The base contact length and the distance between the p-GaN/i-GaN layers and the drain of the super HFET are 4 and 3 μm, respectively.

3. Results and discussion

3.1. Electrical characteristics and optimization

The accuracy of physical models is verified by matching DC simulations with experimental data for conventional super GaN HFET for different gate voltages with I_Dmax of around 290 mA/mm at V_{GS} = +2 V, shown in Fig. 2. This figure shows the I–V curves for the device with L_{GD} = 10 μm. The fabricated device realized the specific on-resistance of 11.26 Ω·mm and the breakdown voltage of 560 V [8].

At the off-state, for the breakdown voltage measurement, the gate–source voltage of −15 V was selected, which is sufficiently lower than V_{TH} of −4 V so that the 2DEG channel beneath the gate was completely removed to achieve the off-state. The maximum drain current for the designed normally-OFF device is smaller than that for the normally-ON device. The maximum drain current for new device was decreased due to the low 2DEG density in the channel. These 2DEG densities can be the same as those for the normally-ON device using the optimized design. Therefore, the maximum drain current for the normally-OFF device can be on the same level as for the normally-ON device.

Fig. 3 compares the transfer characteristics of D-mode and E-mode super GaN HFETs at V_{DS} = 10 V. This figure shows that the super GaN HFET structure can obtain a positive threshold voltage by recessing the...
The i-GaN top layer. Fig. 4 confirms that the $V_{TH}$ of the device can be modulated by modifying the depth of the recessed i-GaN layer that has been specified as “H” in Fig. 1. The increase of the recessed height requires to decrease the AlGaN barrier layer, so that the threshold voltage of the device shifts positively, and the current density decreases due to the significant reduction of charge carriers. A $V_{TH}$ versus recess height law can be extrapolated from simulations data and gives $V_{TH} = 0.2h - 4.8$, where $h$ is the height of the recessed i-GaN layer. From the extrapolation, the normally-OFF operation can be realized by the recessed i-GaN layer height of more than 24 nm. By increasing the recessed height, the thickness of AlGaN barrier layer between gate and drain decreases and the electron channel can be formed by the reverse electron, leading to a more positive $V_{TH}$. This technology realizes an efficient approach for engineering the interface charges, that leads to an effective $V_{TH}$ control.

As can be seen in Fig. 5, by the recessing of the i-GaN layer in the AlGaN barrier layer, an additional peak indicated with “2” in the electric field distribution is introduced. Theoretically, the electric field distribution can be flattened in the drift region compared to a conventional GaN PSJ-HFET.

This device structure with recessed i-GaN layer presents the enhanced breakdown voltage. In this paper a simulation of the off-state breakdown performance of the super GaN HFET with a recessed i-GaN top layer is performed and it is investigated how the height and length of this recessed region affect the breakdown voltage of super GaN HFET. By increasing the drain voltage in the off state, $I_D$ increases and reaches a critical current level of 10 $\mu$A/mm. It can be concluded that the breakdown voltage is limited by the current flow through the buffer layer. The increase of $I_D$ correlates well with the increase of $I_G$ and the breakdown voltage is determined by the impact ionization of carriers. Fig. 6 shows the breakdown voltage versus the recessed i-GaN layer height. The breakdown voltage is calculated when the $I_D$ reaches a value of 10 $\mu$A/mm. The breakdown voltage is higher for a smaller recessed height due to the lower current flow through the buffer layer that is arising from the steeper barrier for electrons at the buffer channel interface. The obtained highest breakdown voltage is about 805 V at the recessed height of 1 nm while the measured breakdown voltage of conventional GaN HFET is about 560 V. Both structures have no field plate and breakdown occurs at the peak named 1 in Fig. 5 because the electric field is crowding. In addition to the recessed i-GaN height, the recessed region length is also critical to obtain maximum breakdown voltage.

As Fig. 7 represents, the recessed region length should be optimized to achieve the higher breakdown voltage. The recessed edge neither can be close to drain edge or P-GaN cap edge. To achieve maximum $V_{BR}$ (around 800 V), the optimal location for the recessed edge is 1 $\mu$m from the drain edge.

The recessed length also effects $R_{on}$ of the E-mode device. By laterally extending the recessed region, more 2DEG in the drift region would be formed, leading to a lower $R_{on}$ and higher breakdown voltage.
would be depleted and thus increase the channel resistance. However, owing to the 2DEG remaining in the channel except for the recessed region, lower $R_{on}$ can be attained compared to the conventional GaN HFETs. In order to design an E-mode device with improved Figure of Merit (FOM, $V_{Th}/R_{on}$), the length of recessed i-GaN region should be optimized.

3.2. Reliability of device

Current collapse is the most debated reliability issue for GaN HFETs. It's obvious that the large gate-drain electric field plays a key role in current collapse and degradation data. So, the surface electric field distribution at the drain-side gate edge in the GaN HFETs, is one of the most important factors related to reliability issues [12]. Consequently, surface engineering efforts, aimed at smoothing the field profile such as overlapping gates [13] and field plates [14,15] effectively relax the electric field profile in the gate drain region. This has beneficial effects on reliability [16,17]. So, in this paper, regarding to reliability, the relation between the collapse phenomena and the electric field distribution in high-voltage GaN-HEMTs discussed physically. References [18,19] provided the experimental results for different GaN device structures to discuss relation between the current collapse phenomena and the electric field peak.

Current collapse is caused by the electron trapping at defects in the AlGaN and GaN layers as well as the passivation interface. Under high applied voltage, the channel electrons are accelerated by the electric field, and a part of the accelerated electrons is trapped in the device. As the trapped electrons partially deplete the 2DEG channel even after turn-on state, the on-resistance is increased with applied voltage. Therefore, the electric field affects the collapse phenomena. So, the proposed structure for the GaN device becomes a solution for suppressing the collapse phenomena due to the relaxation of the electric field concentration. In super GaN HFETs, the presence of a polarization 2DHG above the 2DEG across the AlGaN barrier layer forms a super junction which helps to prevent current collapse by suppressing the non-linear distribution of the electric field around the drain-side p-GaN edge, thus improving the reliability [8]. In the prior super HFETs [8,11,20], the electric field distribution has two spikes (see Fig. 5) at the drain side p-GaN edge and at the drain edge, have been marked up in Fig. 1 by “1” and “3” respectively. In the new device with PSJ technology, by recessing the i-GaN top layer, an extra spike has been introduced at the drain side recessed edge numbered as “2”. Using the recessing i-GaN technique, the electric field distribution between gate and drain achieved more uniformity that reduces current collapse and improves the device reliability.

4. Conclusion

A normally-OFF GaN HFET in Polarization Super Junction (PSJ) technology was proposed. Silvaco simulation carried out to analyse the electrical characteristics of device. The GaN PSJ HEMT with a recessed i-GaN top layer has been applied to realize a $V_{Th}$ of $+2 \text{ V}$, a breakdown voltage of 800 V, an on-resistances of 11.26 $\Omega \text{mm}$ and a drain and gate leakage current of less than 1 $\mu \text{A/mm}$. In this structure, $V_{Th}$ can be controlled by the etching depth of the recess without significant increase in the on-resistance characteristics. A better trade-off between the threshold voltage control and drain current drive capability can be obtained by optimization of the recessed depth. Moreover, the length of recessed i-GaN region is also critical parameter for $R_{on-VBR}$ trade-off characteristics. The breakdown voltage of normally-OFF GaN PSJ HFET with $L_{GD} = 10 \mu \text{m}$ can achieve 800 V by selecting a recessed length from the gate edge of 9 $\mu \text{m}$, while $V_{BR}$ for the normally-ON counterparts is 560 V. For the power electronics application, a higher FOM ($V_{Th}^2/R_{on}$) has been provided by increasing breakdown voltage and maintaining low on-resistance. Moreover, the reliability issue associated with currents collapse in the new device will be improved through the uniformed electric filed distribution introduced by the recessed edge.

CRediT authorship contribution statement

Samaneh Sharbati:Conceptualization, Methodology, Software, Formal analysis, Writing - original draft. Thomas Ebel:Validation. Investigation, Resources, Funding acquisition. Wulf-Toke Franke:Supervision, Data curation, Visualization, Writing - review & editing, Project administration.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supplementary data

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