LEAPER: Modeling Cloud FPGA-based Systems via Transfer Learning

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Abstract—Machine-learning-based models have recently gained traction as a way to overcome the slow downstream implementation process of FPGAs by building models that provide fast and accurate performance predictions. However, these models suffer from two main limitations: (1) training requires large amounts of data (features extracted from FPGA synthesis and implementation reports), which is cost-inefficient because of the time-consuming FPGA design cycle; (2) a model trained for a specific environment cannot predict for an unknown environment. In a cloud system, where getting access to platforms is typically costly, data collection for ML models can significantly increase the total-cost-ownership (TCO) of a system. To overcome these limitations, we propose LEAPER, a transfer learning-based approach for FPGA-based systems that adapts an existing ML-based model to a new, unknown environment to provide fast and accurate performance and resource utilization predictions. Experimental results show that our approach delivers, on average, 85% accuracy when we use our transferred model to a new, unknown environment to provide fast and accurate performance in a cloud environment with $5$-shot learning and reduces design-space exploration time by $10^3$, from days to only a few hours.

I. INTRODUCTION

The need for energy efficiency from edge to cloud computing has boosted the widespread adoption of FPGAs. In addition to the reconfigurability of an FPGA to implement diverse workloads, FPGAs’ flexibility in a cloud system is attributed to its cloud deployment model [1]–[12]. These deployment models span from on-premises clusters to compute, storage, and networking capacity in public clouds.

An FPGA is highly configurable as its circuitry can be tailored to perform any task. The large configuration space of FPGA and the complex interactions among configuration options lead many developers to explore individual optimization options in an ad-hoc manner [13], [14]. Moreover, FPGAs have infamous low productivity due to the time-consuming FPGA implementation process [15]. A common challenge that past works have faced is how to evaluate the performance of an FPGA implementation in a reasonable amount of time [16]. To overcome this problem, researchers have recently employed machine learning (ML)-based models [16]–[25] to estimate the performance of an FPGA-based system quickly. These models are based, in turn, on traditional ML approaches. Traditional ML models have three fundamental issues that can reduce the usability for assessing FPGA performance, especially in a cloud system.

First, they are trained for specific workloads, fixed hardware, and/or a set of inputs. Therefore, when presented with a different feature-space distribution because of a new workload or hardware, an ML model must be retrained from scratch. Otherwise, the model will perform poorly because the trained model does not have a notion of the new, unknown environment [1] Therefore, traditional ML-based models have limited use-ability.

Second, learning-based approaches, such as neural networks, require a considerable number of samples to construct a useful prediction model. Collecting such a large number of samples is often slow and time-consuming due to the very long FPGA implementation cycle. Similarly, in cloud computing or other settings, where getting access to platforms is typically costly and error-prone, which makes collecting enough samples almost infeasible.

Third, traditional machine learning with limited samples is prone to serious overfitting problems (i.e., when a model matches too closely to the training data) [26], limiting model generalization.

Figure 1 demonstrates the traditional approach to building ML-based models. Using the traditional approach, we would need to create two separate prediction models, one for the low-end cloud environment and another one for the high-end cloud environment, each one requiring a large number of samples.

![Fig. 1: Comparison of traditional learning approach and LEAPER.](image)

Our goal is to leverage an ML-based performance model trained on a low-end local system to: (1) predict the performance in a new, unknown, high-end FPGA-based system, (2) predict the performance of a new, unknown application to overcome the limitations of current ML-based performance models in a cloud environment.

To this end, we present LEAPER\textsuperscript{\textdualcolor{red}{1}}\textdualcolor{red}{1}, a transfer learning-based model that predicts performance of a new, unknown high-end FPGA-based system. First, we train LEAPER on a low-end local system see Figure 2. Second, LEAPER uses transfer learning\textsuperscript{\textdualcolor{red}{1}}\textdualcolor{red}{2} to efficiently adapt the trained base model to an unknown, target environment (i.e., a high-end system) with a few samples from the target environment as possible. LEAPER also transfers models across unknown, new applications.

This paradigm is also referred to as few-shot learning [28]. The idea behind few-shot learning is that, similar to humans, algorithms can learn from past experiences and transfer the knowledge to accomplish previously-unknown tasks more efficiently. The transferred models usually have high generality [28].

In this paper, we make the following contributions:

1) We present the first use of few-shot learning to transfer FPGA-based computing models across different hardware platforms and applications (Section II). This approach dramatically reduces (up to $10^3$) the training overhead by adapting a base model trained on a low-end edge FPGA platform to a new, unknown high-end environment (a cloud environment in our

\textsuperscript{1}We call our mechanism LEAPER because it allows us to hop or “leap” between machine learning models.
LEAPER is a performance and resource estimation approach to transfer ML models based on classic machine learning algorithms [29], [30] across different FPGA-based platforms and across different applications on the same platform. First, we give an overview of LEAPER (Section II-A). Second, we describe FPGA-based accelerator configuration options and application features used for training our base model (Section II-B). Third, we briefly describe the base model training (Section II-C). Fourth, we explain the key component of LEAPER: the transfer learning technique (Section II-D).

A. Overview

Figure 2 depicts the key components of LEAPER. The upper part of the figure describes the base model building, while the lower part shows the target model building.

**Base Model Building.** LEAPER’s base model building consists of three phases. In the first phase (1) in Figure 2, we employ the design of experiment (DoE) technique [31] to select a small set of input configurations that we represent the entire space of input configurations \(C_{base}^{loc}\) to build a highly accurate base learner. By using DoE, we minimize the number of experiments needed to gather training data for LEAPER while ensuring good quality training data. In the second phase (2), FPGA implementations are made with a software-hardware co-design process. Once the FPGA design has been implemented, the resulting FPGA-based accelerator is deployed in a system with a host CPU. Then, we run the \(C_{base}^{loc}\) configurations on the deployed FPGA-based system to gather samples for training our base model. The generated responses, along with the applied configuration options (ref. Table I), form the input to our base ML algorithm. In the third phase (3), we train our ML algorithm (Section II-C) using ensemble learning [32]. During this phase, we perform 10-fold cross-validation to validate the performance of our model. During cross-validation, we divide our dataset into 10 equal subsamples of which 1 set is used for validation and the others for training. Once trained, the framework can predict the performance and resource usage on the base system (a low-end FPGA) of previously-unseen configurations, which are not part of the \(C_{base}^{loc}\) configurations used during the training.

**Target Model Building.** We use transfer learning to reuse an ML model (trained on a low-end FPGA) in a high-end cloud environment. The first phase (4) in Figure 2 of the target model building, we repeat the accelerator generation step to get a few sample configurations. We perform this step to create our few-shot learning dataset \(C_{target}\), which is used to adapt the base model to the target cloud environment. In the final phase (5), we train our transfer learners (see Section II-D) to leverage the base model to perform predictions for a new, unknown target environment (new application or hardware).

### B. FPGA Configuration Options and Application Features

The ML feature vector used for training an ML model is composed of FPGA configuration options (Table I) and application features (Table II). Table I describes commonly used high-level synthesis (HLS) [33] pragmas that belong to our FPGA configuration options, for both the base and the target environment, and constitute part of our ML feature vector. We select these HLS pragmas because they are used to optimize and tune the performance of FPGA implementations [34].

We include these configuration options among the features because of their large potential impact on performance. Both loop pipelining (PL) and loop unrolling (U) can improve application performance significantly. To enable simultaneous memory accesses, array partitioning (PR) divides arrays into smaller memory units of arbitrary dimensions to map them to different memory banks. This optimization produces considerable speedups but consumes more resources. Inlining (I) ensures that a function is instantiated as dedicated hardware. Dataflow (D) allows parallel execution of tasks. In addition, burst read (R) and burst write (W) access to/from the host guarantee that the accelerator is not stalled for data. Moreover, FPGA frequency (F) affects not only performance but also resource consumption. For instance, to meet the FPGA timing requirements, the FPGA tool tries to insert registers between the flip-flops, which increases resource consumption. The actual configuration space of an application depends on the specific application characteristics (see Table I). For example, we include loop unrolling in the configuration space when an application contains loops that can be unrolled. In total, our configuration options for a particular application consist of up to 4,608 configurations.

**Application Features.** We also include inherent application features in our training dataset. For each application kernel \(k\) processing a dataset \(d\), we obtain an application profile \(p(k, d)\), where each parameter is a statistic about an application feature. Table III lists the main application features we extract by using the LLVM-based PISA analysis tool [35]. Ultimately, the application profile has 395 features, which includes all the sub-features of each metric we consider. We perform feature selection to select the 100 most important features to analyze the behavior of an application with the FPGA configuration options (see Table I).

### C. Base Model Building

The third phase of the base model building is the base learner training phase. Formally, in a learning task, \(X\) represents feature space with label \(Y\), where a machine learning model is responsible for estimating a
TABLE II: Main application features extracted from LLVM.

| Feature          | Description                                                                 |
|------------------|------------------------------------------------------------------------------|
| Instruction Mix  | Fraction of instruction types (integer, floating point, memory read, memory write, etc.) |
| ILP              | Instruction-level parallelism on an ideal machine.                           |
| Data/Instruction  | For a given distance $\delta$, probability of reusing one data element/instruction (in a certain memory location) before accessing $\delta$ other unique data elements/instructions (in different memory locations). |
| Reuse Distance   |                                                                             |
| Register Traffic | Average number of registers per instruction.                                 |
| Memory Footprint | Total memory size used by the application.                                   |

function $f : \mathcal{X} \rightarrow \mathcal{Y}$. LEAPER predicts the execution time (resource consumption) $\mathcal{Y}$ for a tuple $(p, k, c)$ that belongs to the ML feature space $\mathcal{X}$, where $p$ is an FPGA-based configuration options (ref. Section II-B) that runs an application characteristics $k$, with an optimization configuration vector $c$.

We use an ensemble of two base learners. Our base learners are nonlinear algorithms that can capture the intricacies of FPGA architectures by predicting the execution time or resource consumption. Our first algorithm is the random forest (RF) [30], which is based on bagging [36]. We use RF to avoid a complex feature-selection scheme since RF embeds automatic procedures that are able to screen many input features [37], like the ones we selected in the previous section. Starting from a root node, RF constructs a tree and iteratively grows the tree by associating a node with a splitting value for an input feature to generate two child nodes. Each node is associated with a prediction of the target metric equal to the observed mean value in the training dataset for the input subspace that the node represents. Our second learner is gradient boosting [33]. Bagging [35] reduces model variance, and boosting decreases errors [40]. Therefore, we use RF and gradient boosting together to increase the predictive power of our final trained base model.

The training dataset for our base model has two parts: (1) an optimization configuration vector $c$, whose representation remains invariant across different environments, and (2) the responses corresponding to each tuple $(p, k, c)$. To gather the architectural responses, we run each application $k$ belonging to the training set $\mathcal{T}$ with an input dataset $d$ on an FPGA-based platform $p$, deploying a configuration $c$. This way, we obtain the execution time for the tuple $(p, k, d)$, which we can use as a label (Y) for training our base learner for performance prediction. We build a similar model to predict resource consumption, where we use the resource consumption (i.e., DRAM, FF, LUT, DSP) of the tuple $(p, k, d)$ as a label when we train our base learner for resource consumption. After training our base learners, we can predict the execution time (resource usage) $(f_s : \mathcal{X_s} \rightarrow \mathcal{Y_s})$ of tuples $(p, k, d)$ that are not in the training set. We use 10-fold cross-validation to validate our base learner’s performance, whereby the data is divided into ten validation sets.

D. Cloud Model Building via Transfer Learner

LEAPER provides the ability to transfer trained FPGA models across different environments. LEAPER defines a target environment $\tau_3$ as an environment for which we wish to build a prediction model $f_3$ where, however, data collection is expensive, and a source environment $\tau_2$ as an environment for which we can cheaply collect many samples to build an ML model. $\tau_1$ is a low-cost edge FPGA, while $\tau_2$ is a high-cost cloud FPGA. LEAPER then transfers the ML model for $\tau_2$ to $\tau_3$.

Algorithm 1 presents LEAPER’s transfer learning approach. We use a few sample observations $c_{tl}$ (line 5) from both the source and the target environments to make our transfer learners (TLs) learn how to make source environment distribution to target environment distribution. $c_{tl}$ is a subset of $c_{doe}$. This helps us to avoid measuring all $c_{doe}$ from a cost-prohibitive target cloud environment. LEAPER trains TLs (line 4) that transform the source performance and utilization model $f_s$ to the target model $f_t$.

Algorithm 1: LEAPER’s transfer learning

Input: (1) Base learner ($f_s$) i.e., trained low-end edge FPGA prediction model, (2) Sub-sampled few-shot learning dataset $C_{tl} \subseteq c_{doe}$ from the base and the target model

Output: Target cloud FPGA model $\hat{f}_t : \mathcal{X}_t \rightarrow \mathcal{Y}_t$

- **Initialization:** Maximum number of iterations $M$
- **While** $M \neq 0$ **do**
  - Normalize the feature vector
  - Train ensemble transfer learners (TL) with $c_{tl}$
  - Find the candidate TL ($\hat{h}_t$): $\mathcal{X}_t \rightarrow \mathcal{Y}_t$ that minimizes the error over the $c_{doe} - C_{tl}$
  - Compute the mean relative error:
    - $\epsilon_{mre} = \frac{1}{c_{doe} - C_{tl}} \sum_{i=1}^{c_{doe} - C_{tl}} | \eta_{acc} - \eta_{pred}^{acc} |$
  - Use identified $h_t$ to transform predictions of $f_s$:
    - $\hat{f}_t = h_t(f_s)$
  - $M = M - 1$
- **Return** $\hat{f}_t$

In transfer learning, a weak relationship between the base and the target environment can decrease the predictive power of the target environment model. This degradation is referred to as a negative transfer [41]. To avoid this, we use an ensemble model trained on the transfer set (i.e., the few-shot learning dataset in Figure 2) as our transfer learners (TLs). We chose these specific TL methods based on our extensive empirical analysis. Our first TL is based on TrAdaBoost [26], a boosting algorithm, which is a learning framework that fuses many weak learners into one strong predictor by adjusting the weights of training instances. The motivation behind such an approach is that by fusing many weak learners boosting can improve the overall predictions in areas where the previously grown learners did not perform well. We use Gaussian process regression [42] as our second TL. It is a Bayesian non-parametric algorithm that calculates the probability distribution over all the appropriate functions that fit the data. To transfer a trained model, we train TrAdaBoost and Gaussian process regression, which are our candidate TLs. We choose the one that has minimum transfer error (ref. Line 6).

Finally, to build $f_3$ from $f_s$, we use $h_t$, which performs a non-linear transformation of the predictions of $f_s$. We use a non-linear transfer learner because, based on our analysis (Section III-F), non-linear models are able to capture the nonlinearities present in the FPGA performance and configuration options.

III. EVALUATION

We evaluate LEAPER using six benchmarks (see Table III), which are hand-tuned for FPGA execution covering several application domains, i.e., (1) image processing (histogram calculation (hist)) [43], and canny...
edge detection (cddf [43]); (2) machine learning: binary long short term memory (blstm [44]), digit recognition (digit) [45]; (3) databases: relational operation (select) [46]; and (4) data reorganization: stream compaction (sc) [43]. These kernels are specified in C/C++ code using high-level synthesis ( HLS) that is compiled to the FPGA target.

A. Hardware Platform and Tools

Table IV summarizes the system details of the source and our on-prem research cloud environment. We select a low-end edge PYNQ-Z1 [48] as the source platform to build base learners. We use the Accelerator Coherency Port (ACP) port [49] for attaching accelerators to the ARM Cortex A9 CPU of PYNQ-Z1. Figure 3a shows the target system space. As we increase the number of labeled samples, the target model accuracy increases. However, the accuracy saturates and, with 5-10 shots, we cannot achieve an accuracy as high as 80 to 90%. Second, compared to applications with multiple complex kernels (blstm, cedd, digit), simpler kernels (hist, sc, select) can be more easily transferred using fewer samples. Applications with multiple kernels have a larger optimization space. The large optimization space leads to more complex interactions that have compounding effects with other optimization options because we are modeling for multiple kernels rather than just a single kernel. Additionally, simple kernels such as sc and select have been implemented using hls stream interfaces. Here rather than storing intermediate data in local FPGA memories, we read streams of data, and hence certain complex optimizations (like array partitioning) cannot be applied. This leads to a change in the feature space of different environments. Third, less severe changes are more amenable to transfer as the source, and target models are more closely related, e.g., transferring to CAP11 (PCle Gen 3 with 3.3 GB/s bandwidth) from low-end PYNQ with PCIe Gen 2 (1.2 GB/s bandwidth) entails a smaller increment in bandwidth than moving to CAP12, which offers R/W bandwidth of ~12.3 GB/s. Fourth, change in the technology node from one FPGA to another (e.g., changing from ADMKU3 board to AD9V3 board) has a larger effect. The large optimization space leads to more complex interactions that have compounding effects with other optimization options because we are modeling for multiple kernels rather than just a single kernel. Additionally, simple kernels such as sc and select have been implemented using hls stream interfaces. Here rather than storing intermediate data in local FPGA memories, we read streams of data, and hence certain complex optimizations (like array partitioning) cannot be applied.

Figure 5 shows LEAPER’s accuracy for transferring across different cloud platforms. We make the following four observations. First, as we increase the number of labeled samples, the target model accuracy increases. However, the accuracy saturates and, with 5-10 shots, we cannot achieve an accuracy as high as 80 to 90%. Second, compared to applications with multiple complex kernels (blstm, cedd, digit), simpler kernels (hist, sc, select) can be more easily transferred using fewer samples. Applications with multiple kernels have a larger optimization space. The large optimization space leads to more complex interactions that have compounding effects with other optimization options because we are modeling for multiple kernels rather than just a single kernel. Additionally, simple kernels such as sc and select have been implemented using hls stream interfaces. Here rather than storing intermediate data in local FPGA memories, we read streams of data, and hence certain complex optimizations (like array partitioning) cannot be applied.

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target environment. Figure [6] shows the accuracy of a target model trained by 5-shot transfer learning for predicting a resource utilization vector \( \eta(BRAM,FFLUT,DSP) \). The reported accuracy is for the transferred model, i.e., using a base model (low-end FPGA) to predict a target model (high-end cloud FPGA) after few-shot learning. In Figure [6a], the horizontal axis depicts the target platform, while the base learner is trained on a PYNQ-Z1 board. In the case of an application model transfer (Figure [6b]), the platform remains unchanged (PYNQ-Z1), while the base learner application changes (horizontal axis). We make three observations. First, the resource model shows low error rates for predicting BRAM and DSP. This is attributed to the fact that the technological configuration of these resources remains relatively unchanged across platforms (e.g., BRAM is implemented as 18 kbits in both the source and target platforms). Second, flip-flops and look-up-tables have comparably higher error rates because the configuration of CLB\(^8\) slices varies with the transistor technology and FPGA family. Third, Figure [6b] shows the mean accuracy for transferring different application-based models on a fixed FPGA board.

We observe relatively low accuracy for DSP consumption while transferring a base model trained on \( \text{hist} \). This low accuracy is because the \( \text{hist} \) FPGA implementation does not make use of DSP units. However, all other applications utilize DSPs. Therefore, the ML model trained on \( \text{hist} \) is not able to perform well in other transferred environments. Table [V] compares the average accuracy across different boards and applications using two different TLs: (1) decision tree (DT)\(^8\) and (2) adaBoost (ADA)\(^8\). We observe that our ensemble of TLs are able to outperform both DT and ADA.

C. Target Cloud FPGA Model Building Cost

Table [VI] shows the time for collecting (see “DoE run (hours)”) the 50 sampled DoE configurations \( \{c_{ih}\} \) that we use to gather training data. Please note that while the process of synthesis and P&R of the high-end system’s FPGA, which is needed to obtain the maximum operating clock frequency and the resources’ utilization, can be carried out offline, most of the cloud providers are offering VMs with all the appropriate software, IPs and licenses needed to generate an FPGA image ready to be deployed at their cloud infrastructure (e.g., the Vivado AMI of AWS\(^8\)). This justifies the argument of the cost of the

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\(^8\) A configurable logic block (CLB) is the fundamental component of an FPGA, made up of look-up-tables (LUTs) and flip-flops (FF).
cloud environment for DoE runs. We use a Linux image with FPGA and SoC development tools, IPs, and licences to generate bitstreams for the selected Xilinx devices in Table IV on the Nimbix cloud. Table VII also includes the execution time on the ADM-PCIE-KU3 cloud platform (“Exec (msec)”) and the transfer time (“Transfer (msec)”) for each model. By using transfer learning, the DoE runtime is amortized and, by using a few labeled samples \(c_{\text{TL}}\) (“5-shot (hours)”) from the target platform, we can transfer a previously trained model and make predictions for all the other configurations for the target platform. As a result, quick exploration and significant time savings (at least 10×2×) are possible when transferring a model (i.e., “5-shot (hours)” + “Transfer (msec)”) as compared to building a new model from scratch (i.e., “DoE run (hours)” + “Exec (msec)”). Note, DoE reduces training samples from 500+ to 50, while 5-shot transfer learning further reduces this space to 5, so we achieve 100× speedup over building a new model from scratch using just the DoE data (still more cost-efficient than traditional “brute-force” training).

In Table VII we mention the performance and resource utilization for our considered applications both on a low-end system and a high-end cloud system. We use LEAPER, to obtain the performance and resource utilization for the high-end cloud configuration.

**D. Base Model Accuracy Analysis**

We also evaluate the accuracy of our base model. The base model (Section II-C) is trained on a low-end PYNQ-Z1 to different high-end target FPGA boards (horizontal axis), and (b) different applications as base learners (horizontal axis) to all the target applications, on low-end PYNQ-Z1 board.

**TABLE VI:** DoE time for gathering sampled data points for a single CPU-FPGA platform (“DoE run (hours”)”), DoE execution time on the deployed platform (“Exec (msec)”), Estimated Cost on a cloud platform (“Est. Cost ($)”), time for gathering 5 labeled samples (“5-shot (hours)”), LEAPER time including the transfer time (“Transfer (msec)”), “Speedup” over building a new model from scratch using just the DoE data (still more cost-efficient than traditional “brute-force” training).

| Application | DoE run (hours) | Exec (msec) | Est. Cost ($) | 5-shot (hours) | Transfer (msec) | Est. Cost ($) | Speedup |
|-------------|----------------|-------------|--------------|---------------|----------------|--------------|---------|
| blstm       | 135            | 455         | 166.7        | 13            | 55.6           | 16.2         | 10.4    |
| cedd        | 122            | 295         | 155.0        | 12            | 26.5           | 13.0         | 10.3    |
| digit       | 97             | 45          | 121.2        | 9             | 17.1           | 11.3         | 10.8    |
| sc          | 104            | 145         | 130.0        | 10            | 27.9           | 12.4         | 10.6    |
| select      | 106            | 145         | 132.5        | 10            | 27.6           | 12.5         | 10.6    |

The cost is estimated based on an enterprise online cost estimator [62] using a public-cloud system with configuration akin to our on-prem system. Specifically, we have selected an m2.8xlarge, 64GB RAM VM - 125(h) for bistream generation (x86) and an m5.large instance (360-thread POWER8, 1TB RAM, ADM-PCIE-KU3 with CAPS-1 - 500h) for deployment.
TABLE VII: Execution time and resource utilization for low-end base configuration (PYNQ-Z1) and high-end cloud configuration, a Nimbin mp3fi instance.

| Application | Config. | Exec. Time (ms) | BRAM | DSP | FF | LUT |
|-------------|---------|----------------|------|-----|----|-----|
| blstm       | low-end | 4200           | 80%  | 15% | 24%| 47% |
|             | high-end| 1245           | 62%  | 8%  | 12%| 21% |
| cedd        | low-end | 10254          | 83%  | 37% | 95%| 97% |
|             | high-end| 2217           | 56%  | 3%  | 75%| 94% |
| digit       | low-end | 2458           | 94%  | 33% | 79%| 85% |
|             | high-end| 873            | 84%  | 12% | 24%| 75% |
| hist        | low-end | 6173           | 94%  | 0%  | 11%| 37% |
|             | high-end| 1104           | 67%  | 0%  | 5% | 30% |
| sc          | low-end | 19306          | 82%  | 0.4%| 12%| 25% |
| select      | low-end | 4018           | 91%  | 0.1%| 12%| 23% |
|             | high-end| 18306          | 82%  | 0.4%| 12%| 25% |
|             | high-end| 3918           | 91%  | 0.1%| 12%| 23% |

![Image](image.png)

Fig. 7: Mean accuracy for performance and resource utilization predictions using LEAPER’s base model and other popular machine learning techniques.

E. Why does LEAPER work?

To explain our results for transfer learning, we analyze the degree of relatedness between the source and target environments. We perform Pearson correlation analysis [66] followed by a divergence analysis [67] of the performance distributions of the environments.

Using the correlation analysis, we make the following three observations. First, for different target hardware platforms, we see a high correlation of 0.76 to 0.97 between the source and target execution time, which indicates that the target model’s performance behavior can easily be learned using the source environment. As the linear correlation is not 1 for all platforms, the use of a nonlinear transfer model is substantiated. Second, as we switch to a higher external bandwidth for the target platform (i.e., CAPI1 to CAPI2), the correlation becomes lower because the hardware change is much more severe coming from a low-end FPGA with limited external bandwidth. Third, the correlation between applications on a single platform is lower (0.45 to 0.9) because of the varying application characteristics and optimization space.

We measure the relatedness of the performance distributions of the source ($P(\tau_s)$) and the target applications ($P(\tau_t)$). This analysis measures the degree of non-linearity because application-based environments exhibit a low linear correlation. We employ the Jensen-Shannon Divergence (JSD) [68] (ref. Table VIII) to quantify the statistical distance between $P(\tau_s)$ and $P(\tau_t)$. The lower the values of JSD, the more similar the target environment is to the source (i.e., if $D_{JSD}(P(\tau_s)||P(\tau_t)) = 0$ implies the distributions are identical and 1 indicates unrelated distributions). This analysis confirms the trend observed from transferring application models (Figure 5), i.e., the more closely related the source and target applications, the fewer samples are required to train our non-linear transfer learners. The measured distance between the tasks is proportional to the error of the target task. As can be seen from Table VIII for many applications, transfer learning to build accurate models is feasible since their JSD is limited. Similar trends are observed for the resource utilization model.

F. Discussion and Limitations

Transfer to a new platform and application simultaneously. In supervised learning, transferring both to a new platform and application at the same time would lead to sub-optimal results (as observed in [69]) this is because we would perform two-levels of transfer. Moreover, for transfer learning, an ML model needs to have some notion of the target environment. Therefore, we explicitly exclude this option in the paper.

FPGA resource constrained environments. During partial reconfiguration [70] or in a multi-tenant environment [5], we are often constrained by limited resources [71]. In such scenarios, the resource management is more efficient to be controlled by a middleware layer [72]. We do not assume such as a middleware. Therefore, our analysis targets bare-metal systems. In future, we aim to extend our work to such scenarios as well.

LEAPER generality to other platforms. LEAPER, in essence, is a framework for building and then transferring models from a small edge platform to any new, unknown FPGA-based environment. We demonstrate our approach using the cloud as our target environment because cloud systems often use expensive, high-end FPGAs, e.g., Amazon AWS F1 cloud [3], Alibaba Elastic cloud with FPGAs [4], etc. We can, thus, achieve tangible gains in terms of cost, efficiency, and performance.

Effect of FPGA resource saturation. An FPGA gives us the flexibility to map operation to different resources. For example, we can map a multiplication operation either to a CLB or a DSP slice. The deciding factor is the operand width. If the operand width is smaller than DSP slice width, the operation is mapped to a CLB else to a DSP unit. An ML-model can be trained to learn such relations. However, we avoid it in our current work.

IV. RELATED WORK

To our knowledge, this is the first paper to propose the transfer of FPGA-based performance (resource) models. FPGAs are infamous for low productivity due to the time-consuming downstream implementation process. We have extensively evaluated our approach using five FPGA-based platforms with three different interconnect technologies on six real-world applications. In this section, we describe other related works in FPGA ML-based modeling, analytical modeling, and transfer learning.

FPGA ML-Based Modeling. Recent works propose ML-based methods [10]–[16] to overcome the issue of low productivity with FPGAs. O’Neal et al. [16] uses CPU
performance counters to train several ML-based models to predict FPGA performance and power consumption. Makrani et al. [20] trained a neural network-based model to predict application speedup across different FPGAs. Makrani et al. [17] and Dai et al. [21] use ML to predict resource utilization for an FPGA implementation. However, these solutions become largely impractical once the platform, the application, or even the size of the workload changes. LEAPER proposes to reuse previously built models on a low-end source environment to accelerate the learning of ML models on a high-end target environment through transfer learning. Unlike LEAPER, past works apply traditional, time-consuming brute-force techniques to collect training data. These techniques quickly become intractable when the number of optimization parameters increases due to the curse of dimensionality [73].

Transfer Learning. Recently, transfer learning [27], [74], [75] has gained traction to decrease the cost of learning by transferring knowledge. Valov et al. [76] investigated the transfer of application models across different CPU-based environments using linear transformations. Jamshidi et al. [41] demonstrated the applicability of using nonlinear models to transfer CPU-based performance models. The works above influenced the design of LEAPER. In contrast, we focus on FPGA-based systems that, unlike a CPU-based system, has a different hardware architecture for every application and optimization strategy, and (2) use an ensemble of transfer learners that transfers accurate models to a target environment.

V. CONCLUSION

We introduce LEAPER, the first transfer learning-based approach to transfer FPGA-based prediction models. LEAPER combines statistical techniques and transfer learning methodologies for training data ML overhead. It overcomes the inefficiency of traditional ML-based methods by accurately transferring an existing ML model built on an inexpensive, low-end FPGA platform to a new, unknown, high-end environment.

Our experiments show that we can develop cheaper (with S-shots), faster (up to 10×), and highly accurate (on average 85%) models to predict performance and resource usage. LEAPER combines statistical techniques and transfer learning. Unlike a CPU-based system, has a different hardware architecture for every application and optimization strategy, and (2) use an ensemble of transfer learners that transfers accurate models to a target environment.

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