Design of CMOS Reconfigurable Passive Down-conversion Mixer for LTE MTC Receiver

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Abstract. A reconfigurable passive down-conversion mixer is fabricated in standard 65nm TSMC RF CMOS technology and presented in this paper. Different from traditional mixers, transconductor stage in this design is variable, and the transconductance stage uses a second-order low-pass transimpedance amplifier composed of Tow-Thomas structure to form a current-limited filter with adjustable bandwidth. From 900MHz to 1920MHz, the mixer circuit achieves flexible gains(5/11/19/26dB) and variable IF bandwidth(5/7.5/10MHz) with 4-bit control words, while linearity, noise figure and other indicators will also be adapted to suit the requirements of different communication standards. Under the maximum gain, its noise figure NF is 7.8dB; and under the minimum gain, its IIP3 is about 14.6dBm. It drains a current of 3.4/6.3mA from a 1.2V voltage supply at different gain mode.

1 Introduction

With the rapid development of Internet and mobile Internet, the Internet of things is coming to an outbreak. Internet of things based on LTE is the new technology of Internet of things, which brings many advantages to the application of the Internet of things, including deepening wide network coverage, predictable service quality, high reliability and stable end-to-end security and seamless interoperability supported by global standards, which will bring more opportunities to the Internet of things. The application scenarios of the Internet of Things can be roughly divided into three categories. One is the monitoring service represented by the Internet of Vehicles. The transmission rate is about 10 Mbit/s, and the representative technology is LTE-V[1]. The second is the interactive collaborative service represented by the wearable class. The transmission rate is less than 1Mbit/s, and the representative technology has eMTC and LTE Cat1; the third is the data collection service represented by remote meter reading, the transmission rate is less than 100Kbit/s, and the representative technologies are NB-IoT, Lora and SigFox.

As the key module of RF receiver, the design technology of mixer is always the research focus of RF integrated circuits. The downconverting mixer moves the output RF signal of the low noise amplifier to the intermediate frequency band after the low noise amplifier in the receiver. The direct conversion architecture has obvious advantages in terms of power consumption, hardware cost, and flexibility of reconstruction when implementing eMTC receivers [2], so a direct conversion (zero intermediate frequency) architecture is adopted for eMTC receivers. However, direct conversion mixers in CMOS technology have problems such as flicker noise, dc offset, and intermodulation distortion. So how to design a low noise, high linearity, and reconfigurable mixer in a low-cost CMOS process is a major challenge in implementing eMTC receivers. Based on TSMC65LP CMOS technology, this paper designs a broadband reconfigurable mixer for eMTC zero intermediate frequency receiver.
2 Circuit Design

2.1 Architecture of Reconfigurable Mixer

This paper uses the current-mixing based on passive switching mixing as shown in Fig. 1, which is a mixer structure consisting of a transconductance stage, a switching stage, and a transimpedance amplifier (TIA) stage. As shown in Figure 1, the transconductance stage converts the input RF signal into an RF current output, which is used to achieve the mixing of the current signal at the switching stage and finally the current signal is converted to voltage through the transimpedance stage, which achieves a positive voltage conversion gain.

The transconductance stage uses two stages of programmable transconductance to provide two different transconductances, where the transconductance is controlled by VC1, and the transimpedance stage uses a two-stage flexible filtered transimpedance amplifier with a Tow-Thomas structure, where the cross-resistance value is also variable, controlled by VC2. The voltage conversion gain of the current type passive mixer is

\[ VCG = \frac{2}{\pi} \frac{g_{m1}}{g_{m2}} R_{IA} \]

Where, the coefficient \( \frac{2}{\pi} \) is caused by the commutation behavior of the switches\(^3\).

At the same time, TIA has a certain filtering effect due to its own structure. The cutoff frequency can be changed by the adjustment of the feedback component parameters, which provides a direction for the intermediate frequency reconfigurable. In this design, a second-order low-pass transimpedance amplifier with a Tow-Thomas structure is used. It has better design flexibility, and also implements -3 dB IF bandwidths of 5/7.5/10MHz through two control words (VCT1, VCT2) to reach some requirements for baseband bandwidth in eMTC systems.

2.2 Transconductor Stage

The design of the transconductance stage is shown in Fig. 2, where a two-stage self-biasing inverter array is used, and the first stage is fixed on to improve the lower fixed transconductance. On the basis of self-biasing inverter, the second stage adds switch control transistor to the source of PMOS and NMOS transistors respectively, and controls turn-on or not by controlling word VC1 to provide higher transconductance. In this way, the two different transconductance achieves two kinds of gain of the whole mixer circuit, and the reconfiguration of power consumption is realized because of the difference of the effective working circuit.
2.3 Switches Stage
The switching stage of the current-type passive mixer is shown in Fig. 3. The circuit consists of two switch pairs, forming a double-balanced frequency conversion characteristic. The capacitor Cc in the figure is the AC coupling capacitor between the transconductance stage and the switching stage. Its blocking effect attenuates the low frequency interference signal, and the switching transistor has no DC component, thus having better flicker noise characteristics. At the same time, it can be seen that the switching stage only transmits RF signals and does not consume additional current. The size setting of the switch is a key issue. In general, the larger W/L makes the switch have a small on-resistance, and the ideal switching performance is beneficial for better linearity performance. The parasitic capacitance between the transconductance stage and the switching stage becomes large, which is detrimental to noise characteristics. In addition, considering the high frequency characteristics of the mixer, the switching transistor uses a deep N-well process RF transistors[4].

2.4 TIA Stage
The Tow-Thomas structure implements a second-order low-pass transimpedance amplifier as shown in Figure 4. Its input impedance[6] can be expressed as:

\[ Z_{in,TIA} = \frac{R_2}{(1 + SC_1R_1)(1 + A_1(s))(1 + LG(s))} \]  

(2)

Where LG(s) represents the loop gain. It can be given by:

\[ LG(s) = \frac{R_2}{SR_1R_3C_2(1 + SC_1R_1)} \]  

(3)

To ensure that the transimpedance amplifier input impedance is small enough, it depends mainly on the ideality of the op amp, that is, there is a large enough bandwidth gain product GBW. A large enough GBW ensures that A1(s) has a large value in a wide low frequency range, so that the input impedance remains small enough in a wide low frequency range. According to the input frequency of
the out-of-band third-order intercept point in the 10MHz bandwidth of the LTE protocol, the bandwidth gain product of the operational amplifier here is designed to be about 400MHz.

![Figure 4. Circuit of TIA stage based on Tow-Thomas biquad topology](image)

This structure maintains two conjugate poles in the original filter structure with a 40 dB/decade attenuation. Take \( R_1R_2 = R^2 \), \( C_1 = C_2 = C \), where the cutoff frequency and quality factor can be reduced to:

\[
\omega_0 = \frac{1}{\sqrt{R_1R_2C_1C_2}} = \frac{1}{RC} \tag{4}
\]

\[
Q = R_2 \sqrt{\frac{C_1}{R_1R_3C_2}} = \frac{R_2}{R} \tag{5}
\]

It should be noted that extra transistors are introduced here as switching transistors, and the size of the transistors should be noted to prevent the introduction of additional resistance and capacitance.

### 3 Post-simulated Results

The reconfigurable mixer is fabricated in TSMC 65nm RF CMOS process and the layout of the reconfigurable mixer is shown in Figure 5. It consists of three parts: transcondutor stage, switches stage and TIA stage. The area of the whole circuit is 0.840 mm×0.685 mm including pad.

![Fig. 5. Layout of the reconfigurable mixer.](image)
The post simulation is performed in Cadence. Fig.6(a) depicts the simulated VCG of the proposed downconverter with LO frequency of 1.9GHz, and 4 gain steps (5/11/19/25dB) are clearly shown in Fig.6(a).

Figure.6(b) and Figure.6(c) show the voltage conversion gain diagram for the IF bandwidth of 7.5MHz and 5Mhz, respectively. It can be seen from the Figure.6 that under different IF bandwidth modes, the gain does not change much, and the IF bandwidth can be reconstructed.

Taking into account the GSM and LTE frequency bands, LO signals with frequencies of 940 MHz, 1.9GHz are applied respectively. Along with the change of the LO frequency, VCG of the mixer only has a slight change.
Figure 6. FLO=1.9GHz, Simulated VCG curve of the proposed mixer.

The simulated NF is illustrated in Fig.7. The mixer has smallest NF when it has the highest gain. Under the highest gain, the double sideband NF of the mixer is 7.8dB. Under other kinds of gain, the NF is about 8.7dB, 16.8 dB, 18.9dB, respectively.

Figure 7. Simulated NF in different gain modes with FLO=940MHz, VCG=25/19/11/6dB.

At the lowest gain, the mixer has the best linearity and when fLO=1.9GHz, the simulated IIP3 of the mixer is 14.6dBm, as shown in Fig.8.
4 Conclusion
A reconfigurable mixer in standard 65nm TSMC RF CMOS technology is presented. The simulated results show that the mixer operates correctly, which provides 4 gain steps (5/11/19/25dB). Moreover, it has three kinds of variable IF bandwidth (5/7.5/10MHz), a current of 3.4/6.3 mA is drawn from the 1.2V supply. As the voltage gain changes, the mixer's noise and linearity will also follow. At the highest gain, the mixer has the best noise figure, and at the lowest gain, the mixer has the best linearity. Therefore, we can adjust the mixer to meet the receiver sensitivity and dynamic range according to different communication modes and this design is very suitable for eMTC receiver system.

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