REVIEW ON FIR FILTER ARCHITECTURE DESIGN AND ITS COMPUTATIONAL BLOCKS

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Abstract - Low power VLSI circuit employed applications power consumption and high performance, the area is crucial in DSP. A filter is used in almost all electronic devices that function on signals. They are used to extract the useful part from the input signal and the required part of signal reaches the receiver. This paper is mainly focussed on the survey of different architecture design for FIR filter. The different performances such as speed, complexity, PDP, ADP, are reviewed.

Keywords: Re-configurable FIR filter, speed, area, power.

1. INTRODUCTION

In the past, Area, Performance, Cost, and Reliability were only the major concerns of a VLSI designer. whereas the power consumption of the circuit was merely considered. In recent years this has begun to change dramatically. Power consumption is considered and given the importance that has been given to other factors, in some cases or demand of applications, a bit more. Digital signal processing is an important part of electronic devices as signal is an integral part of DSP. A signal is pulse coded with information that needs to be transferred from source to the destination, and a medium is needed to do so, called channel. During the transmission, some of the data is lost due to the noise present in the channel. This information must be retained in the signal in its
original form till the transfer is complete to have complete data transfer with minimal loss. A signal has high-frequency range, low-frequency angle, and mid-frequency range. Sometimes the information is contained in only one frequency range to make the extraction and transfer easy. So that the loss induced could also be compromised effectively. To pull-up, the information from the signal filters is used. The filters employed are different based on the signal whether it’s digital or analog. We use digital filters in Digital Signal Processing (DSP).

FIR filter is a type of digital filter that is used for linear characteristics applications. It is usually preferred because of its linear phase response and non-recursive property, which makes FIR filter possess stronger resilience to phase shift and higher stability in long-term processing tasks than its FIR counterparts. As a result, to date FIR filters are widely adopted in numerous commercial produces, especially in the base-band processing market. Based on this various apps are implemented to design an efficient FIR filter to reduce power, delay, and area. Minimising area and delay have always been considered important. But, reducing power consumption has been gaining prominence recently as high power operation in small area circuits could rise thermal problems. The customers will take some products which they want to buy and go to the billing counter. The shopkeeper will take the products which are attached with Li-Fi hardware which communicates to the billing server through Li-fi Receiver connected to it. After that, all the product and its details will be shown to the android application and the total billing amount will also show. As the shopkeeper is a visually challenged person, the total billing amount will convert into speech. After that Shopkeeper has to say “BILL” on his mobile application by pressing the power button, then the bill will automatically generate. Then billing will be done successfully.

2. LITERATURE REVIEW

FIR Filter Architecture The FIR filter basically consists of three components, the D flip-flop, multiplier and an adder. The D flip-flop to implement a delay, a multiplier to implement the coefficient, and an adder to sum the nodes at the end of each tap [5]. Figure: A shows the basic block diagram of FIR filter.

![Figure 1a. – FIR Filter](image)

![Figure 1b. –MAC unit in FIR Filter](image)

Deepika etal (2016) described implementation of MAC unit in the design of FIR filter. It is easy when compared to window techniques. MAC unit is multiple accumulation unit. It comprises of multiplier and adder.
A reconfigurable booth multiplier was selected as it is a high speed multiplier[2,8]. Carry look ahead adder is used for the purpose of final addition and these combinations together make the circuit execute algorithms faster and efficient [10].

Figure 1b, shows architecture of MAC unit. It is a combination of reconfigurable booth multiplier and carry look ahead adder. Due to regular structure and speed by reducing partial product booth multiplier and it can work for n number of bits. A configuration register has been added in booth multiplier to avoid move clock cycle. Register introduced is set for 4-bit,8-bit,16-bit [8]. First of all 2 input's that are given to the MAC unit gets multiplied by using reconfigurable booth multiplier and the multiplication result is added to the previously stored result in the MAC unit. When an input a₁ has been taken which is constant throughout the computation and another input b₁ which is FIR filter co-efficient was taken, if these two inputs get multiplied by using reconfigurable booth multiplier then result is fixed to carry look ahead adder and another variable a₀ which is set to zero initially works as a second input to the adder later in next cycle, a₀ is previous output of MAC unit [13].

Evangelos kyritsis et al (2016) explained about the implementation of karatsuba algorithm in the design of efficient and faster FIR filter[16]. The KMA (Karatsuba Multiplication Algorithm) reduces a 2N x 2N bit multiplication to a set of (N+1) x (N+1) and N x N bit multiplication and additions by splitting the 2N bit input operands and generating same auxiliary variable. When karatsuba algorithm is applied to FIR filter equation, a parallel architecture is obtained resulting in increased speed and reduced area especially in case of high dynamic range filter, and also uses carry-save(CS) in order to decrease the critical path and to speed up calculations[13,5].
Multiplication Unit contains a Partial Product Generator Unit (PPG) and a Wallace tree for adding the partial products. For the Wallace tree, the Synopsis Design Ware IP (DW02_tree) has been used [4]. CS architecture is used in order to enhance delay savings. Figure 3 shows the proposed Karatsuba FIR filter. The karatsuba design which proposed shows better performance with less circuit area, and lower power consumption.

*hamizharan. V et al (2012)* described the implementation of computation sharing multiplier in the design of FIR filter. Computation Sharing Multiplier (CHSM) is efficiently used for the low complexity design of FIR filter. Both add and shift operations were represented by multiplications in FIR filtering operations over common computation results using CHSM. CHSM multiplier was implemented by using Carry Select Adder (CSA) [7-9] which is a high-speed adder. In the design by using single ripple carry adder and add one circuit using fast all-one finding circuit and low-delay multiplexers a Carry ahead adder was implemented which will further decrease area and accelerate the speed of CSA. No additional memory is required to share when the common computations are found. A high performance and low power in FIR implementation was approached by computation sharing multiplier [14].

![Figure 3](image)

Figure 4 shows FIR filter in transposed circuit form (TDF) fir filter.

![Figure 4](image)

Figure 5 points that FIR filter based on CHSM. In transposed direct form (TDF), FIR filter multipliers were replaced by S&A’s as a pre-computer is connected to input. Therefore, the FIR filter using CHSM consists of one pre-computer and ten S&A’s. Then, figure 5, the pre-computer outputs are shared by all the S&M’s. The CHSM scheme and circuit-level techniques help to achieve high performance FIR filtering operations.

*Bo Yuan et al (2016)* introduced the implementation of stochastic multiplier [10-11] in designing of a high accuracy FIR filter. In the proposed edition, it achieved significant reduction in the hardware complexity as compared to the conventional design using the simplicity of stochastic arithmetic unit and the high accuracy non-scaled stochastic adder that has significant increase in the computation accuracy. It avoids the original down scaling effect for large T cases. Based on this method the high accuracy stochastic FIR filter was developed. Here SA refers to stochastic adder and SM to stochastic multiplier. Figure 6 points the hardware architecture of the proposed stochastic adder. Figure 7 shows direct form stochastic FIR filter.
First of all, it is a non-scaled adder. Although OR gate can be used as an approximated non-scaled adder, in some applications the OR-gate based adder suffers from huge approximation errors as well as the limitation for positive only addition. Thereby, causing the OR-gate based adder has very severe accuracy loss if we consider the negative inputs. Secondly, the proposed stochastic adder has very high accuracy in terms of signal to noise ratio (SNR). Especially, for the adder chain case. Figure 8 shows two-line stochastic multiplier. By using two-line based non-scaled stochastic adder and multiplier, the hardware architecture of the high accuracy stochastic FIR filter was developed. The overall architecture was chosen as either direct-form or lattice format. Due to this proposed stochastic FIR achieves both low hardware cost and high computation accuracy and is suitable for practical systems.

M. Ganasekaran et al (2014) elaborated the design of low delay high compact FIR filter using reduced Wallace multiplier [12]. In this proposed system, the adder was modified by reduced carry save adder in the last stage of multiplier. So that, the performance of the over-all FIR filter structure is improved in terms of area and delay. The operation of carry save adder is, it computes the sum in parallel without waiting for its carry. The carry is computed in the next stage of adder structure. So, no adder performs the addition of ‘m’ numbers faster than normal or regular addition. And it has a full adder like ripple carry adder. But, the carry output from each bit is taken out to form second result vector rather than being directed to the next most significant bit.
3. CONCLUSION

The elaborated design of high compact FIR filter, and its different structures are described. The computational blocks are described. Such as Adders and Multipliers. The performance of the FIR filter structure are analysed in terms of area and delay.

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