1. Introduction

Moore’s law has remained relatively consistent for transistor manufacturing over the last 30 years. However, improvements in the degree of integration and minimization of design rules are facing physical and economic limitations. Recently, three-dimensional (3D) integration, a new method used to increase the degree of integration (such as in the cases of a wafer on wafer, system in package, package on package and through-silicon via [TSV]), was attempted and commercialized.

3D integration technology using a TSV of copper interconnects enables vertical connection between layers without wire bonding. The depth of a TSV, which corresponds to the thickness of a chip or interposer of a TSV, is the same as the length of a bonding wire. Therefore, advantages, including high-speed signal transmission, excellent conductivity and volume reduction, can be expected in the near future. However, the manufacturing processes of TSVs for 3D integration are complex, and a high yield for each process is required. A TSV is generally manufactured via formation by reactive ion etching, followed by the formation of an insulating layer. The barrier/seed layer is then formed by physical vapor deposition, metal filling of the via is performed by electroplating, and planarization by chemical mechanical polishing (CMP), wafer thinning, and the formation of bumps. These complex manufacturing processes can result in a number of issues, including leakage current because of poor step coverage, the formation of a deep barrier/seed layer with an increasing aspect ratio, incomplete copper filling, and stress generated by the structure and differences in thermal expansion coefficients. Therefore, each process in manufacturing a TSV requires careful checking and management. To analyze the issues, destructive methods such as the cross-sectional inspection method using an optical microscope (OM), scanning electron microscopy (SEM), transmission electron microscopy, and the use of a focused ion beam (FIB) have been previously used. Other, non-destructive methods employ X-ray computer tomography and scanning acoustic tomography. However, the electrical characteristics cannot be evaluated by these methods and the methods have limited resolution.

As a non-destructive analytical technique, the optical beam induced current (OBIC) technique is based on detecting photocurrents using the irradiation of light with a photon energy greater than the band gap energy of the semiconductors. This technique has been used widely in analyzing defects in the junction and metal–oxide–semiconductor (MOS). The OBIC technique for power semiconductor devices was introduced in 1979.[1] The OBIC
and electron-beam-induced current (EBIC) techniques have been used by many researchers to observe the formation of the depletion region in silicon devices.[2–4] Furthermore, the OBIC technique has been applied to the accurate detection of failure locations in semiconductors.[5, 6] The optical-beam-induced resistance change (OBIRCH) method has been used to detect high-resistance areas at the bottom of vias and in metal lines using a laser with wavelength longer than the OBIC.[7] Mizushima et al.[8] used the OBIRCH method to evaluate leakage currents around TSVs with an intentionally formed undercut. We have reported[9] the defect analysis of high-electron-mobility transistors (HENTs) using a scanning electron and laser-beam-induced current (SELBIC) system. In the SELBIC system, the cold cathode emission gun and laser sources with two wavelengths of 1,064 nm (YAG laser) and 1,400 nm (laser diode) are installed coaxially across a vacuum chamber. The system can be used in air or in a vacuum. Meanwhile, the scanning-laser-beam-induced current (SLBIC) system is fundamentally based on OBIC techniques. It uses only a laser beam sources (YAG laser and laser diode) in air, except for the cold cathode gun of the SELBIC system. An infrared laser beam can penetrate most semiconductor substrates. Recently, most of the top surface of a substrate of a semiconductor device is formed as multi-layer metal wiring. Thus, the irradiation of a laser beam from the sample’s back surface will be useful for defect analysis of the back surface of wiring or analysis of internal defects in the substrate. In particular, it is expected to be useful in the defect inspection of the bottom area of a via.

So far, the OBIC technique has been used mainly in the failure analysis of completely manufactured TSVs. Before completing production, the depth of the barrier/seed layers and copper filling must also be checked occasionally by cross-sectional observation employing SEM and an FIB. Because the quality of a copper via filled by electroplating is determined by the sputtered barrier/seed layer, various issues might arise in the manufacturing of vias. If these issues are not precisely detected, the reliability of the product will be reduced. The TSV process involves a number of metals, such as those in the bump and redistribution layers. Accordingly, many difficulties arise in analyzing failures. In the manufacturing process of TSVs, it is necessary to accurately detect defects in vias as soon as possible.

In this work, to confirm the filling state of the electroplating copper after the barrier/seed layers have been deposited by sputtering, TSVs manufactured in a via-first process are investigated using the SLBIC method. The current image corresponding to insufficient deposition of barrier/seed layers is examined.

2. Experimental Procedure

2.1 Sample preparation

Figure 1 shows the manufacturing process of the via-first TSV. Via holes with diameters ranging from 50 μm to 150 μm were formed on a p-type silicon wafer of 200 mm using a deep reactive ion etching system. The 500-nm-thick insulating layer on the top surface of the silicon and the walls of vias was formed by thermal oxidation. The barrier/seed (Ti/Cu) layers (240 nm/2,000 nm thick) were deposited by a sputtering system. Copper filling in the vias was achieved by electroplating. A chemical mechanical process (CMP) followed for Cu planarization. The silicon wafer of 200 mm was diced after the copper CMP into pieces having dimensions of 2 cm × 2 cm, and a piece was taken as a sample for the SLBIC measurement. A face-up sample was mounted on an aluminum sheet holder that was 130 μm thick. A tungsten probe for electrical connections on the back surface was applied to the top surface of an aluminum sheet holder. The barrier layer of titanium covering the top surface was used as an electrode for electrical probing. An ohmic contact was formed on one end of the side of the back surface by the evaporation

![Fig. 1 Schematic diagram of the manufacturing process of the first-via TSV.](image-url)
of Au. It was used as another probing electrode. The aspect ratio of the vias ranged from 2.23 to 4.88. The depth of the via hole with a diameter of 80 μm was approximately 320 μm. The sample was 710 μm thick. It had a typical MOS structure.

2.2 SLBIC system and measurement

Figure 2 is a schematic diagram of the SLBIC system with its confocal infrared laser scanning microscope. A YAG laser beam was scanned over the sample’s back surface using a Galvano mirror. An infrared laser beam can penetrate most semiconductor substrates. Consequently, the focal point was moved from the back surface into the silicon in the z direction. Physical movement resolution in the z direction was 0.1 μm. The wavelength and power were 1,064 nm and 3 mW, respectively. The glass sample stage was kept in a dark chamber with an atmospheric environment. Optical and current images were obtained at the same time as changing the remote control mode. The maximum resolution of both images was 1,024 × 1,024 pixels in a frame (400 nm/pixel for an objective lens of 50 times and 100% zoom). The laser scan speed was 3 s per frame. The minimum current and maximum gain of the DC amplifier were 40 pA and 10,000, respectively. The feedback resistance of the amplifier was 500 kΩ. The sample was biased by up to ±5 V.

To detect the induced currents, tungsten probes were connected to the sample as shown in Fig. 2. Two types of probe connection were used. An amplifier input probe was connected to the back surface in what is referred to as a Type A connection. A Type B connection is a connection to the top surface. The current image was measured as the position changed between the voltage bias and amplifier input probes.

3. Results and Discussion

An SLBIC measurement was carried out to assess the filling state of the electroplating conformal copper after the barrier/seed layers were deposited by sputtering in the vias.

Figure 3 shows an optical image of the top surface and
corresponding current image measured by the SLBIC system. A current image of $1,024 \times 1,024$ pixels was obtained under the conditions of zero applied voltage, feedback resistance of 500 k$\Omega$ and unity gain. To observe the SLBIC of the via holes with diameter of 80 $\mu$m, the laser beam was focused upwards from the back surface. The dotted circles and ellipses in the optical and current images show the same positions of the vias that were analyzed in detail.

Figures 3(b) and (c) show the measured current image for probe connection Types A and B, respectively. In the case of Type A, a bright tail similar to a comet was observed at one end of the via (Fig. 3(b)). The electrical potential of the silicon substrate will be the same throughout the region. However, the same side of one end of the vias is constantly brighter. The laser beam will be scanned across silicon–insulator–silicon or silicon–insulator–copper–insulator–silicon material. We believe that a bright tail will appear to extend in the silicon substrate in the scanning direction of the laser when a laser beam scans the SiO$_2$/Si interface. It is thus thought that the tail is closely related to the scanning condition of the laser beam. But the scanning speed of the laser beam of the used SLBIC system is fixed to be constant. In the case of Type B, there were two types of current image patterns (Fig. 3(c)), namely an O-ring pattern and a bright circle pattern. The difference between the two patterns in terms of the brightness of the tails is presented in Fig. 3(b). The brightness of the tail in the bright circle pattern appeared stronger than that in the O-ring pattern.

To investigate both types of current image, a YAG laser was used to irradiate via holes with diameters ranging from 50 $\mu$m to 150 $\mu$m. Results of the SLBIC measurements obtained while changing via diameters and the probing are shown in Fig. 4. As the via diameter increased, the O-ring pattern appeared. The bright circle pattern was observed for small via diameters, such as diameters of 50 $\mu$m and 70 $\mu$m. For the via diameter of 80 $\mu$m, the two patterns coexisted but the O-ring pattern was dominant. This was also confirmed in the current image of high magnification. The optical image was observed using the SLBIC system at the same depth as for the current image. The O-ring pattern in the optical image appeared to be brighter in the wide area of the via than the bright circle pattern. It is thought that because the focal point of the laser beam had moved from the back to the top that the bottom of the via was completely filled with copper. Consequently, if the bottoms of vias are filled uniformly with copper, when the laser beam meets a uniform metal surface, it will be reflected in the form of brightness over a wide area. Luhan et al.[10] reported on the aspect ratio (1.25–2.5), showing the applicability and limits of sputtering for barrier/seed deposition in a via. It is thought that the occurrence of a brightness difference in the optical images was due to the difference in the depth of metal in the via.

Generally, in an MOS structure under forward biased conditions, there is typically a brightness contrast in OBIC when there is a defect, such as poor insulating characteristics at the interfaces.[11]
To determine whether the brightness contrast changed because of the defect, the position of the sample on a glass stage relative to the scan direction of the YAG laser was rotated from 0° to 360°, as shown in Fig. 5. The YAG laser always scanned under the same conditions for each rotation and was irradiated to the same depth in the sample. The arrows indicate the same via. As shown in Fig. 3, in the case of Type A, the brightness contrast appeared at the same location on the side of one end of the via hole, regardless of the rotation of the sample. In the case of Type B, the brightness contrast was the reverse of that for Type A. If the current image was the result of a defect in any one of the vias, the location of the brightness should change with the rotation of the sample according to the location of the defects. The measured image was thus thought to be unrelated to defects and believed to be caused by the charging of the carriers.

Figure 6 shows (a) the current image measured by the SLBIC system, (b) the magnified current image of the dotted rectangle in (a), and (c) a cross-sectional image observed by a conventional OM, for a via diameter of 80 μm.
observed using a conventional OM, for a via diameter of 80 μm. To confirm the difference between the two patterns in the measured current image, the back surface of the sample was polished carefully and mechanically. In the case of via d, with a diameter of 80 μm as shown in Fig. 6(c), the existence of a space 18 μm from the bottom of the via was confirmed. It is seen as a bright circle pattern in the current image (Fig. 6(a) and (b)). As shown in Fig. 4, a bright circle pattern were also measured in vias with diameters of 50 μm and 70 μm, and a space in the bright circle pattern of the current image was observed in all vias as a result of incomplete copper filling at the bottom of the via. It was found that this related to the bright circle pattern from the measured current image. We believe the pattern was due to the presence of a discontinuity in the film of the sputtered barrier/seed layer. In addition, the bottoms of vias a, b, c and e were filled with electroplated copper. In this case, the O-ring pattern appeared in the image. Discontinuous seed layers in the side walls of vias b, c, and e were also observed, but these were not related to the current image. The current image of the O-ring pattern was measured in the presence of the electroplated copper layer on the bottom surface of a via. The difference between the patterns in the measured current image was positively confirmed in a cross-sectional observation using an OM.

Figure 7 shows the variation in maximum brightness as a function of the bias voltage. In the case of Type B, an amplifier probe was connected to the metal on the SiO2/Si to detect the induced currents. A biased voltage of up to ±5 V was applied to the back surface with ohmic contact. The maximum brightness in both patterns remained constant up to −5 V, when a negative voltage was applied to the Ohmic contact. However, when a positive voltage was applied, the maximum brightness decreased dramatically at 2 V. In the case of Type A, the maximum brightness was the reverse of that for Type B. The maximum brightness of the circle pattern was greater than that of the O-ring pattern.

When the bias voltage was applied to the sample of an MOS structure, there was a change in the distribution of charges in the semiconductor. For a p-type semiconductor, a positive voltage from the gate to the bulk of the silicon created a depletion layer by forcing the positively charged holes away from the gate-insulator/semiconductor interface, exposing a carrier-free region of immobile, negatively charged acceptor ions. When the voltage between the gate and bulk silicon was high enough, a high concentration of negative charge carriers formed in an inversion layer located in a thin layer next to the interface of the semiconductor and insulator.

In the case of Type B, when a negative bias voltage was applied to the back surface with ohmic contact and at the same time a laser beam with a wavelength of 1,064 nm was irradiated from the back surface, positive charges including holes generated by the laser drifted in the silicon. In addition, negative charges accumulated at the SiO2/Si interface. As the negative bias voltage was increased, the insulation resistance and the thickness of the depletion layer at the SiO2/Si interface further increased, and the maximum brightness of the bright circle pattern became greater than that of the O-ring pattern. The generated space around the bottom surface of a via, as identified in Fig. 6(c), indicated the elevated effects of the insulation thickness. As a result, the insulation resistance increased further. Accordingly, with reference to the high maximum brightness for the negative bias voltage as shown in Fig. 7, it is thought that the induced current detected was related to the increased negative charges in the SiO2/Si interface. In the case of positive bias voltage, it is believed that almost all the negative charges at a positive voltage exceeding 2 V had drifted in the silicon. As such, when the bias voltage is changed from negative to positive, it is thought that the rapid change in maximum brightness was related to a change in the band structure to a flat band at the SiO2/Si interface.

Figure 8 is a schematic diagram of the relationship between the sputtered barrier/seed layer (a) and the current image (b) obtained from the results of Fig. 6. Additionally, Fig. 8(c) shows the current image measured with Type A and Type B connections respectively. The state of...
the copper grown by electroplating according to the formation of the discontinuous and/or continuous barrier/seed layer is presented in Fig. 8(a). If the barrier/seed layer deposited by sputtering on the side walls and bottom surface of the via hole was incompletely formed, the electroplated copper could not be deposited without the copper seed layer. Eventually, the front end of the electroplated copper was deposited in a rough and non-uniform manner. Spaces of different lengths were generated between the front end of the copper and the bottom of the vias. As described by previous results (Fig. 7), the difference in insulation thickness affects the dielectric properties, which are thought to affect the distribution of charges. It was found that a current image with a bright circle pattern formed. Furthermore, vias with complete copper filling would form a uniform distribution of charges. As a result, the O-ring pattern was obtained.

4. Conclusions

The evaluation of the electroplating copper filling of TSVs manufactured in a first-via process was investigated using the SLBIC method. The current images for a Type B connection had two patterns: an O-ring pattern and a bright circle pattern. In the case of complete copper filling by electroplating, corresponding to a good deposition of the barrier/seed layer, the current image had an O-ring pattern. Conversely, in the case of poor deposition, such as when there is a lack of a barrier/seed layer on the bottom surface of a via, there was an abnormal growth of copper electroplating. A space around the bottom of a via was also generated. This was confirmed by cross-sectional observation using an OM. A current image with a bright circle pattern was obtained. The generated space was caused by the variation in thickness of the dielectric and the increase in insulation resistance. This also affected the distribution of charges. The difference in brightness contrast in the measured current image obtained by irradiation from a YAG laser was considered to be the result of a greater number of negative charges such as those of electrons on the SiO$_2$/Si interface.

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Woon Choi received B. E. Degree, M. E. Degree, and Doctor of Engineering Degree in metallurgical engineering from Hongik University, Seoul, Korea, in 1989, 1991, and 1996, respectively. He joined the Hajime Tomokage research group at Fukuoka University and at the Fukuoka Industry, Science and Technology Foundation, Fukuoka, Japan in 1998. He has been an Assistant Professor in Department of Electronics Engineering and Computer Science, Fukuoka University since 2007. His research includes thin-film processes involving carbon materials, high-frequency system-in-a-package simulation and evaluation and defect analysis of the through silicon via.

Takahiro Ishimoto was born in Fukuoka, Japan in 1992. He received a B. S. Degree in electronics engineering and computer science from Fukuoka University and is now pursuing an M. S. degree in the same field.

Hajime Tomokage was born in Yamaguchi, Japan in 1953. He received B. E. Degree, M. E. Degree, and Doctor of Engineering Degree in electrical engineering from Kyushu University, Fukuoka, Japan in 1977, 1979, and 1982, respectively. He joined Fukuoka University as a Lecturer in 1982. Since 1992, he has been a Professor in the Department of Electronics Engineering and Computer Science, Fukuoka University. His research area covers nanotechnology with carbon materials and high-frequency system-in-a-package design and evaluation. Dr. Tomokage was the President of the Japan Institute of Electronics Packaging from 2009 to 2011. He has been the Chairman of the International Workshop on Microelectronics Assembling and Packaging since 2001.