BP-Im2col: Implicit Im2col Supporting AI Backpropagation on Systolic Arrays

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Abstract—State-of-the-art systolic array-based accelerators adopt the traditional im2col algorithm to accelerate the inference of convolutional layers. However, traditional im2col cannot efficiently support AI backpropagation. Backpropagation in convolutional layers involves performing transposed convolution and dilated convolution, which usually introduces plenty of zero-spaces into the feature map or kernel. The zero-space data reorganization interferes with the continuity of training and incurs additional and non-negligible overhead in terms of off- and on-chip storage, access and performance. Since countermeasures for backpropagation are rarely proposed, we propose BP-im2col, a novel im2col algorithm for AI backpropagation, and implement it in RTL on a TPU-like accelerator. Experiments on TPU-like accelerator indicate that BP-im2col reduces the backpropagation runtime by 34.9% on average, and reduces the bandwidth of off-chip memory and on-chip buffers by at least 22.7% and 70.6% respectively, over a baseline accelerometer adopting the traditional im2col. It further reduces the additional storage overhead in the backpropagation process by at least 74.78%.

Index Terms—im2col, AI backpropagation, systolic array

I. INTRODUCTION

State-of-the-art neural network accelerators adopt systolic arrays [1] to accelerate the inference and training of convolutional neural networks (CNNs) [2]–[5]. The existing systolic array-based accelerators largely adopt the traditional im2col algorithm [6] to lower the inference of convolutional layers to general matrix multiplication (GEMM). Backpropagation in convolutional layers involves performing more complicated transposed convolution and dilated convolution, which is necessary to perform zero-insertions and zero-paddings (collectively referred to as zero-spaces) for the feature map or kernel. According to our analysis, for convolutional layers with stride ≥ 2, the zero-spaces cause the sparsity of the lowered matrix to be as high as about 75%.

Existing accelerators [2]–[5] use the same systolic array-based platforms to speed up the inference and training of convolutional layers. The core idea of solving zero-space of the input or kernel on systolic array-based platforms is to pre-process them to be zero-inserted and zero-padded in advance [7]. However, the data reorganization requires large amounts of memory access and interferes with the continuity of training. Even though part of the latency of data reorganization can be hidden in the training process as a whole, it nevertheless increases the complexity of hardware control. The transmission of zero-spaces also leads to very high bandwidth requirements, which is more obvious for processors with mismatched bandwidth and computing power. Therefore, it is essential for the im2col algorithm to integrate zero-skipping mechanism. Besides, explicit im2col generates and stores a matrix-like copy of the input and kernel to facilitate further matrix multiplication by PEs, which also incurs significant performance and memory overhead for the convolution itself. This disadvantage can be avoided through the use of the implicit im2col.

While numerous publicly available methods [8]–[10] describing the im2col algorithm only support the inference of convolutional layers, countermeasures for the backpropagation are rarely proposed. Our contributions are summarized as follows:

• We propose a novel implicit im2col algorithm, named BP-im2col, which completely eliminates the zero-space data reorganization during backpropagation;
• We design and implement a TPU-like accelerator, integrated with the hardware implementation of BP-im2col. The address generation modules achieve low-overhead Non-Zero detection and avoid data reorganization during training;
• The proposed TPU-like accelerator reduces the backpropagation runtime by 34.9% on average, and reduces the bandwidth of off-chip memory and on-chip buffers by at least 22.7% and 70.6% respectively, over a baseline accelerator adopting the traditional im2col. It also reduces the additional storage overhead in the backpropagation process.

For clarity, TABLE I shows the meaning of the symbols used in this article.

II. BACKPROPAGATION OF CNN

The backpropagation involves calculating the loss of the input and the gradient of the kernel. Equation (1) outlines the training process [2], [3]. After expressing the convolution as a matrix multiplication (Y = A × B) via im2col [6], the huge benefit of the very regular memory access pattern produces a high ratio of floating-point operations per byte of data transferred.

\[
\text{inference} : \quad I^{l+1} = I^l \ast W^l \\
\text{loss} : \quad \delta I^l = \delta H^{l+1} \ast Tr(rot(180 \ast W^l)) \\
\text{gradient} : \quad Tr(\delta W^l) = Tr(I^l) \ast Tr(\delta I^{l+1}) 
\]

1) Loss calculation: The difference between loss calculation and inference is that loss calculation is realized by performing transposed convolution on the loss of the output by the convolving kernel (see Equation (1)). Another important difference is that the stride of the transposed convolution is a fixed value of 1. The transposed convolution and the im2col process of loss calculation are illustrated in Fig. 1 and Fig. 2. It can be observed that zero-insertions and zero-paddings of the
loss of the output result in more zero pixels in the convoluted feature map. The combination of zero-paddings and zero-insertions introduces a huge amount of zero pixels to matrix $B$ after im2col, and the ratio of zero pixels is as high as 75% to 93.91% for popular convolutional neural networks.

2) Gradient Calculation: The gradient calculation is realized by performing dilated convolution on the reorganized input by the reorganized loss of the output (see Equation (1)). As with the loss calculation, the stride of the dilated convolution is a fixed value of 1. We detail the reorganized steps of the input and the loss of the output in Fig. 3, while Fig. 4 illustrates the im2col process for gradient calculation. The number of zeros introduced by the zero-paddings of the input is roughly the same as that introduced by the inference. What causes the overall plenty of zeros is the zero-insertions for the loss of the output. The zero pixels caused by zero-insertions for the loss of the output is extremely large, and the ratio of zero pixels is as high as 74.8% to 93.6% for popular convolutional neural networks.

III. ALGORITHM AND HARDWARE DESIGN

A. Address Generation of BP-Im2col

When performing BP-im2col for loss calculation, we maintain a virtual matrix $B$ along with a virtual four-dimensional convoluted feature map with zero-spaces. We map the addresses of virtual matrix $B$ to the virtual four-dimensional convoluted feature map with zero-spaces, and then map it to the four-dimensional convoluted feature map without zero-spaces, which is actually stored in the on-chip buffer. For gradient calculation, the mapping of matrix $A$ with zero-spaces is similar to matrix $B$, except that it does not need to perform im2col and has only zero-insertions. Fig. 5 describes the address mapping of matrix $A$ and matrix $B$.

B. NZ Detection

1) Transposed convolution mode: For loss calculation, we divide the zero pixels in a single channel into two areas: namely, one is composed of upper and left zero-paddings (area 0), while the other is composed of other zero-spaces (area 1), which is shown in Fig. 2. The condition that a pixel $(h, w)$ is in area 0 is:

$$ h < K_h - 1 - P_h \text{ or } w < K_w - 1 - P_w. \quad (2) $$

Moreover, the condition that the pixel is in area 1 is:

$$ [h - (K_h - 1 - P_h)]\%S > 0 \text{ or } [w - (K_w - 1 - P_w)]\%S > 0. \quad (3) $$

We present the address mapping algorithm of matrix $B$ lowered during loss calculation in Algorithm 1.

2) Dilated convolution mode: Assuming that a certain pixel to be calculated is mapped to the position of the virtual convolving kernel with zero-insertions as $(h, w)$, the position of the pixel in the channel is shown in Fig. 2. The condition that this pixel to be located in the zero pixel area (area 1) is:

$$ h\%S > 0 \text{ or } w\%S > 0. \quad (4) $$

Moreover, its target position in the actually stored convolving kernel is $(h/S, w/S)$. We present the address mapping algorithm of matrix $A$ lowered during gradient calculation in Algorithm 2.

C. Hardware Design

We implement a systolic array, named as TPU-like accelerator. It uses a $16 \times 16$ systolic array as the accelerator core and adopts the input-stationary data flow. Fig. 5 illustrates the architectural details. Both buffer $A$ and buffer $B$ are double-buffered. Buffer $A$ supplies the data of the dynamic lowered matrix $A$ for PEs, while buffer $B$ supplies that of the stationary lowered matrix $B$. We design 16 FIFOs with different depths between buffer $A$ and the systolic array to skew the data layout. To implement BP-im2col, we use address generation and compression logic to generate appropriate addresses for each block of matrix $A$ and matrix $B$, and recover the data format for the compressed data that is transmitted back.
Transposed convolution mode. In Fig. 5, we describe how a block of matrix B is loaded onto the systolic array. The address generation module first generates pixel addresses under the virtual stationary matrix B view and we take 16 channels to generate addresses in parallel during the address generation of matrix B to supply data for 16 PEs in each row of the systolic array. We detect each address according to Section III-B to filter the zero pixels, and perform address mapping to generate the compressed address of the actually stored feature map. After the data is transmitted back, we send it directly to the PEs, according to its compressed mask. When the data enters the systolic array, the zero pixel position identified by the compressed mask is temporarily filled with zeros.

Dilated convolution mode. Fig. 5 also describes how a block of lowered matrix A is loaded into the systolic array. The dynamic matrix address generation module generates addresses under the virtual dynamic matrix A view. The addresses of the dynamic matrix A are continuous; thus, we only generate the first address of the data in each row of blocks of matrix A (addr), and the addresses of the 16 elements in this row are: \( addr, addr + 1, \ldots, addr + 15 \). However, 16 elements of a row block of matrix A are not strictly continuously stored for dilated convolution, for the reason that there may be zeros that are not actually stored. We therefore need all addresses of the 16 channels to perform address mapping and NZ detection to determine the non-zero position of the row elements. Although the mapped addresses of the 16 elements in a row of matrix A are not strictly consecutive, the non-zero elements are stored consecutively in buffer A. We compress the non-consecutive

**Algorithm 1**: BP-im2col of transposed mode.

**Input**: Address of a pixel in virtual matrix \( B, addr_{in} \);

**Output**: Address in the original feature map without zero-spaces, \( addr_{out} \);

1. \( row, col = \lfloor addr_{in}/(B \cdot H_o \cdot W_i) \rfloor, addr_{in} \% (B \cdot H_o \cdot W_i) \);  
2. \( b, temp1, w_k = \lfloor col/(H_o \cdot W_i) \rfloor, \lfloor row/K_u \rfloor, \lfloor row \cdot K_u \rfloor \);  
3. \( h, k, temp2 = \lfloor temp1/K_u \rfloor, \lfloor temp1\%K_u \rfloor, \lfloor col/(H_o \cdot W_i) \rfloor \);  
4. \( h, w = \lfloor temp2/W_i \rfloor + h_k, \lfloor temp2 \% W_i \rfloor + w_k \);  
5. if \( (h, w) \) satisfy Equation (2) or Equation (3) then  
   \( addr_{out} = NULL; \) if-zero-spaces.
6. else  
   \( h', w' = (h - (K_h - 1) - P_h), w - (K_w - 1) - P_w) / S \);  
7. \( addr_{out} = b \cdot N \cdot H_o \cdot W_o + n \cdot H_o \cdot W_o + h' \cdot W_o + w' \);  
end

TPU-like Experiment Setup. We implement the traditional im2col [6] and BP-im2col on TPU-like accelerator. Our evaluation uses the FP32 data type and a batch size of 2. The synthesis uses ASAP7, a 7 nm predictive PDK library [11].

**Workload.** We evaluate all convolutional layers with stride \( \geq 2 \) from several CNNs. The ”Original” legend in figures is referred to the adoption of traditional im2col integrated with zero-space reorganization, while the ”Ours” legend refers to the adoption of implicit BP-im2col.

IV. EVALUATION

A. Overall Calculation Time

We recorded the performing time of loss calculation and gradient calculation during backpropagation. Figure 6a demonstrates that BP-im2col significantly reduces the loss calculation time by 14.5%, 41.2%, 16.0%, 38.3%, 22.8% and 79.0% respectively, and that most of this gap stems from the data reorganization of zero-spaces. Figure 6b demonstrates that the gradient calculation time of BP-im2col is reduced by 31.3%, 76.3%, 17.7%, 45.3%, 20.9% and 92.4% respectively. BP-im2col greatly reduces the performance overhead of loss calculation and gradient calculation caused by data reorganization. Table II also shows the runtime of loss calculation and gradient calculation of several convolutional layers.
TABLE II: Runtime of loss calculation and gradient calculation of several convolutional layers.

| Convolution layers | Loss Calculation (cycles) | Grad Calculation (cycles) |
|--------------------|---------------------------|---------------------------|
|                    | BP-im2col | Traditional im2col | Speedup | BP-im2col | Traditional im2col | Speedup |
|                    | Computation | Reorganization | | Computation | Reorganization | |
| H1(W1)/C/N/K1(Kw)/S1/2(Sp) | 8962/102 | 8929/989 | 1.3 | 3108/36 | 3798/997 | 1.3 |
| 11/64/64/51/2/1 | 1031/04 | 1032/985 | 1.3 | 943/974 | 895/216 | 1.3 |
| 36/25/25/12/2/0 | 933/068 | 912/588 | 1.3 | 116/331 | 116/363 | 1.3 |
| 22/24/22/43/2/1 | 8081/314 | 822/224 | 1.3 | 83/57/59 | 80/899 | 1.3 |
| 14/102/2048/1/2/0 | 1198/4898 | 11059/200 | 1.3 | 115/27/80 | 150/7648 | 1.3 |

Fig. 6: Performance comparison.

B. Off-chip Memory & Buffer Bandwidth Occupation

Figure 7a demonstrates that BP-im2col significantly reduces the bandwidth occupation of data transmission to buffer B during loss calculation: specifically, it has a minimum reduction of 2.34% (for SqueezeNet) and a maximum reduction of 54.63% (for AlexNet). Figure 7b further demonstrates that BP-im2col significantly reduces the bandwidth occupation of data transmission to buffer A during gradient calculation: specifically, it has a minimum reduction of 18.98% (for ResNet) and a maximum reduction of 31.66% (for AlexNet).

Figure 8a demonstrates that BP-im2col reduces the bandwidth occupation of buffer B during loss calculation by 93.90%, 75.36%, 75.45%, 75.04%, 70.56%, and 76.15%, respectively. The ratio of the bandwidth occupation reduction of buffer B is close to the sparsity of the output in loss calculation. Figure 8b demonstrates that BP-im2col reduces the bandwidth occupation of buffer A by 94.23%, 76.67%, 74.70%, 74.15%, 74.53%, and 76.30%, respectively, which is also close to the sparsity of the output in gradient calculation.

C. Prologue Latency Overhead & Area Overhead

TABLE III: Prologue latency for two matrix address generation modules with sufficient network bandwidth.

| Module | Loss calculation (μm) | Gradient calculation (μm) |
|--------|-----------------------|--------------------------|
| Traditional im2col | Dynamic | Stationary | Dynamic | Stationary |
| BP-im2col | Dynamic | Stationary | Dynamic | Stationary |
| 0 cycle | 31 cycles | 0 cycle | 31 cycles |
| 0 cycle | 68 cycles | 68 cycles | 51 cycles |

The prologue latency introduced by fixed-point dividers from address mapping to completion of on-chip buffer address calculation, as shown in Table III. And the area overhead of the address generation modules after adopting the traditional im2col and BP-im2col in hardware is shown in Table IV.

TABLE IV: Area overhead of address generation modules.

| Module | Traditional im2col | Area (μm²) | Ratio (%) | BP-im2col | Area (μm²) | Ratio (%) |
|--------|-------------------|-----------|-----------|-----------|-----------|-----------|
| Dynamic | 5103 | 0.43 | 56028 | 2.44 |
| Stationary | 5326 | 2.42 | 12109 | 5.22 |

V. CONCLUSION

We propose an implicit im2col algorithm for AI backpropagation, named BP-im2col with the goal of better adapting the training of convolutional layers mapping on systolic arrays. We design and implement the hardware address generation modules based on the TPU-like accelerator, and further develop special optimizations for the hardware based on the accelerator’s architectural characteristics. However, our design does not support sparse computation at this stage, and the crossbar still occupy a very large on-chip area after being pruned. In the future, we will further optimize sparse computation and data flow for the computing modes of the TPU-like accelerator.

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