Research Article

New OTRA-Based Generalized Impedance Simulator

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Operational transresistance amplifier (OTRA) has attracted considerable attention in the recent literature in several applications
such as impedance simulation, universal biquad filter realization, realization of sinusoidal oscillators and multivibrators. However,
to the best knowledge of the authors, any OTRA-based generalized impedance simulator circuits have not been reported so far. The
purpose of this paper is to present such a circuit.

1. Introduction

Although a large number of building blocks have been considered as an alternative to the classical voltage-mode
operational amplifier (VOA) which suffers from the well-known disadvantage of gain-bandwidth conflict, the OTRA
introduced in [1, 2] has been found to be particularly attractive in analog signal processing/signal generation due
to the following advantageous features: transmission properties similar to the current feedback op-amp, lack of slew
rate limitations as encountered in VOAs, and having two low-impedance inputs and one low-impedance output. The
OTRA is a three-terminal analog building block defined by the following matrix equation:

\[
\begin{bmatrix}
V_1 \\
V_2 \\
V_o
\end{bmatrix}
\begin{bmatrix}
0 & 0 & 0 \\
0 & 0 & 0 \\
R_m & -R_m & 0
\end{bmatrix}
\begin{bmatrix}
I_1 \\
I_2 \\
I_o
\end{bmatrix}. \quad (1)
\]

The circuit symbol of the OTRA is shown in Figure 1. In an OTRA, both input terminals are virtually grounded, and
the output voltage is the difference between the two input currents multiplied by the transresistance gain \( R_m \), such that

\[
V_o = R_m (I_1 - I_2). \quad (2)
\]

Thus, both input and output terminals are characterized by low impedance, thereby eliminating response limitations
incurred by capacitive time constants leading to circuits that are insensitive to the stray capacitances at the input terminals.
For ideal operation, the transresistance gain \( R_m \) approaches infinity forcing the input currents to be equal. Thus, the
OTRA is employed in a negative feedback configuration in a way similar to the operational amplifiers.

For discrete designs, the OTRA can be implemented using two current feedback operational amplifiers (CFOA)
(see [3–5], and references cited therein) as shown in Figure 2. On the other hand, from the viewpoint of analog VLSI
implementation, several high-performance CMOS OTRA realizations have also been introduced in the current litera-
ture for instance, see [1, 6, 7] and the references cited therein. An exemplary CMOS implementation from [6] is shown in
Figure 3. The use of OTRAs has been widely investigated in a number of applications such as immitance simulators
[3, 5, 8, 9], integrators [10], filters [11–22], square-wave generators [23], current-mode monostable multivibrators
[24] and oscillators [4, 25, 26], to name a few.

There have been few earlier attempts on simulating various kinds of impedances using OTRAs for instance,
2. The Proposed Generalized Positive Impedance Simulator

The proposed configuration is shown in Figure 4. Assuming the OTRAs to be characterized by the equation \( V_p = V_n = 0 \) and \( V_o = R_m(I_p - I_n) \) where \( R_m \) is the transresistance gain and considering the OTRAs to be ideal (i.e., \( R_m \to \infty \)), a routine analysis of the circuit gives the following expression for input impedance:

\[
Z_{in} = Z_1 Z_2 Z_3 Z_4.
\]  

(3)

From (3) it is clear that by appropriate (resistive/capacitive) choice of impedances, the circuit can be easily used to realize an ideal inductor, frequency-dependent-negative resistance (FDNR) having \( Z_{in} = 1/Ds^2 \) where \( D \) is known as super-capacitance, resistively-variable capacitance and frequency-dependent negative-capacitance (FDNC) having \( Z_{in} = Ms^2 \) where \( M \) is known as super-inductance.

2.1. Grounded Inductor. With the choice of impedance \( Z_3 \) or \( Z_4 \) as a capacitor and the other impedances as resistors, the circuit of Figure 4 can realize a grounded inductor in two ways. (i) with \( Z_1 = R_1, Z_2 = 1/sC_2, Z_3 = R_3, Z_4 = R_4 \) and \( Z_5 = R_5 \), the input impedance is given by \( Z_{in} = sC_2R_1R_3R_4/R_2 \) resulting in a simulated grounded inductor having \( L = C_2R_1R_3R_4/R_2 \). (ii) with \( Z_1 = R_1, Z_2 = R_3, Z_3 = R_4, Z_4 = 1/sC_4 \) and \( Z_5 = R_5 \), the input impedance is given by \( Z_{in} = sC_4R_1R_3R_4/R_2 \) and the simulated grounded inductance has a value \( L = C_4R_1R_3R_4/R_2 \).

2.2. Grounded FDNR. With any two of the three impedances \( Z_1, Z_3 \) and \( Z_5 \) as capacitors, the circuit shown in Figure 4 can realize an FDNR in three ways. (i) with \( Z_1 = 1/sC_1, Z_2 = R_2, Z_3 = R_3, Z_4 = R_4 \) and \( Z_5 = 1/sC_5 \), the input impedance is found to be \( Z_{in} = R_1/sC_1C_2R_3R_4 \) and thus, the circuit realizes an ideal grounded FDNR \( (Z(s)) = 1/s^2D \) where, \( D = C_1C_2R_3R_4R_5 \). (ii) with \( Z_1 = R_1, Z_2 = R_2, Z_3 = 1/sC_3, Z_4 = R_4 \) and \( Z_5 = 1/sC_5 \), the input impedance is found to be

\[
Z_{in} = \frac{Z_1Z_2Z_3Z_4}{Z_5}.
\]
3. Nonideal Analysis

Practically, the trans-resistance gain of an OTRA is infinite and therefore the frequency limitations associated with the OTRA should be considered. Considering a single-pole model, the trans-resistance gain, \( R_m \), can be expressed as

\[
R_m(s) = \frac{R_{o1}}{1 + (s/\omega_o)} = \frac{R_{o1}}{s + \omega_o} = \frac{1}{(s/R_{o1})\omega_o + (1/R_{o1})}
\]

where \( \omega_o = \frac{1}{C_p R_{o1}} \).

For

\[
R_{o1} \rightarrow \infty, \quad R_m(s) = \frac{1}{s C_p},
\]

where \( R_{o1} \) is the DC transresistance gain and \( C_p \) is the parasitic capacitance. By straightforward analysis, the general expression for the input impedance of the positive generalized impedance simulator shown in Figure 4 (when the parasitic capacitance of the OTRA is taken into consideration as per (3)) is found to be

\[
Z_{in} = \frac{Z_1 Z_2 Z_5}{Z_2 Z_4} \left[ s^2 C_p^2 Z_2 Z_4 + s C_p (Z_2 + Z_4) + 1 \right].
\]

Similarly, a still more generalized expression for the input impedance of the positive generalized impedance simulator shown in Figure 4, when the finite output resistance (\( R_o \), typically 15\( \Omega \)) and the parasitic capacitance (\( C_p \), typically 5 pF) of the OTRA both were taken into consideration, has been found to be

\[
Z_{in} = \frac{Z_1 Z_2 Z_5}{Z_2 Z_4} \left[ s^2 C_p^2 Z_2 Z_4 + s C_p (Z_2 + Z_4) + 1 \right].
\]

It is now useful to consider the various special cases. However, to conserve space, we have dealt with only that realization in each case which has been found to be better than the other alternatives.

\[
Z_{in} = \frac{s^2 C_p^2 R_1 R_3 Z_2 Z_5}{R_4}
\]

It is obviously not very fruitful to try to make an equivalent nonideal circuit from the above mentioned because it not likely to give any insight about the effect of various parasitic impedances. However, if \( Z_{in}(j \omega) \) is represented as \( Z_{in}(j \omega) = \text{Re}[Z_{in}(j \omega)] + j \text{Im}[Z_{in}(j \omega)] = R_{eq}(\omega) + j \omega L_{eq}(\omega) \), then it would be useful to know the frequency domain behavior.

2.3. Resistively Variable Capacitor. Resistively variable capacitors have several applications in analog circuit design, for instance see [27, 28]. With any one of the three impedances \( Z_1, Z_3, \) and \( Z_5 \) taken as a capacitor, the circuit of Figure 4 realizes a grounded resistively-variable-capacitor in three different ways: (i) with \( Z_1 = 1/s C_1, Z_2 = R_2, Z_3 = 1/s C_2, Z_4 = R_4 \) and \( Z_5 = R_5 \), the value of input impedance is found to be \( Z_{in} = R_5 R_3/s C_3 R_2 R_4 \), realizing a resistively variable capacitor having \( C_{eq} = C_1 R_2 / R_3 R_5 \) (i) with \( Z_1 = R_1, Z_2 = R_2, Z_3 = 1/s C_3, Z_4 = R_4 \), and \( Z_5 = R_5 \), the input impedance is found to be \( Z_{in} = R_1 R_3 s C_3 R_2 R_4 \) with \( C_{eq} = C_3 R_2 R_4 / R_1 R_5 \), (iii) with \( Z_1 = R_1, Z_2 = R_2, Z_3 = R_3, Z_4 = R_4 \), and \( Z_5 = 1/s C_5 \) input impedance is \( Z_{in} = R_1 R_3 s C_3 R_2 R_4 \) with \( C_{eq} = C_3 R_2 R_4 / R_1 R_5 \). It is easy to see that in all cases, \( C_{eq} \) can be varied by a single variable resistance.

2.4. Grounded FDNC. With the values of the impedances taken as \( Z_1 = R_1, Z_2 = 1/s C_2, Z_3 = 1/s C_3, Z_4 = 1/s C_4 \) and \( Z_5 = R_5 \), the value of input impedance is found to be \( Z_{in} = s^2 C_2 C_4 R_1 R_3 R_5 \). Thus, the circuit of Figure 4 realizes an FDNC whose \( M \) value is given by \( M = C_2 C_4 R_1 R_3 R_5 \).
of the real and imaginary parts from where we can infer to what extent (in magnitude) and up to what frequency, the non-ideal resistive part, \( \text{Re}\{Z_{\text{in}}(j\omega)\} \) and the inductive part \( \text{Im}\{Z_{\text{in}}(j\omega)\}/\omega \) remain close to their intended design values. These plots obtained from SPICE simulations are shown in Figures 5 and 6, respectively, for the circuit designed by taking component values as \( C_2 = 0.05 \) nF, \( R_1 = R_3 = R_4 = R_5 = 7.07 \) k\( \Omega \), yielding the value of lossless grounded inductor to be \( L = 2.5 \) mH.

In order to simplify the expression of (8), we consider the following assumptions:

(i) \( \omega^3 C_2 C_p R_4 R_1 R_5 \left( 1 + \frac{R_2}{R_1} + \frac{R_2}{R_4} \right) \ll 1 \),

(ii) \( \omega^3 C_p R_4 R_5 \left( 1 + \frac{R_2}{R_1} + \frac{R_2}{R_4} \right) \ll 1 \).

\( \omega^3 C_2 C_p R_4 R_1 R_5 \left[ \frac{R_2}{R_4} + C_p \right] \left( 1 + \frac{R_2}{R_1} + \frac{R_2}{R_3} + \frac{R_2}{R_4} + \frac{R_2}{R_5} \right) \ll 1. \) (9)

The simplified expression for the input resistance \( Z_{\text{in}} \) from (8), after making the previous assumptions, is found to be

\[
Z_{\text{in}} = R_4 \left[ \frac{1 + \frac{R_2}{R_1}}{1 + \frac{R_2}{R_4}} \right],
\]

where

\[
R(\omega) = \frac{C_2 R_1 R_3 R_5}{R_4} \frac{\omega^2 (\alpha \tau_2 - \tau_1)}{1 + \omega^2 \tau_2^2},
\]

\[
L(\omega) = \frac{C_2 R_1 R_3 R_5}{R_4} \frac{\alpha + \omega^2 \tau_1 \tau_2}{1 + \omega^2 \tau_2^2},
\]

\[
Z_{\text{in}} = R(\omega) + j\omega L(\omega),
\]
From (13), the appropriate non-ideal value of the inductor simulated by the circuit (at \( \omega = 0 \)) is found to be

\[
\tau_2 = \frac{C_p R_5}{R_4},
\]

\[
\alpha = 1 + \frac{C_p}{C_2} \left( 1 + \frac{R_0}{R_5} \right).
\]

From (16) it can be shown that \( Z_{in}(j\omega) \) can be expressed as

\[
Z_{in}(j\omega) = \frac{1}{j\omega C_{eq}} - \frac{1}{\omega^2 D_{eq}^2}.
\]

From SPICE simulations we have extracted plots showing variation of \( D_{eq}(\omega) \) and \( C_{eq}(\omega) \) as functions of frequency, \( \omega \) which are shown respectively in Figures 7 and 8, for component values taken as \( C_1 = C_5 = 0.22 \, \text{nF} \) and \( R_2 = R_3 = R_4 = 1 \, \text{k}\Omega \), resulting in an ideal value of \( D = 4.84 \times 10^{-17} \, \Omega \).

From the plots shown in Figures 7 and 8 it is found that the resistive part remains nearly constant showing a value of \( D_{eq} = 4.952 \times 10^{-17} \, \Omega \) (as required) up to a frequency of about 10 MHz whereas the equivalent capacitive value is \( C_{eq} = 4.895 \, \text{nF} \) (as also verified by the theoretical formula) which remains almost invariant till a frequency of 10 MHz. Hence, the usable frequency range of the circuit is till about 10 MHz.

3.3. Resistively-Variable Capacitor. With \( Z_1 = R_1, Z_2 = R_2, Z_3 = R_3, Z_4 = R_4 \) and \( Z_5 = 1/sC_5 \) the expression for the input impedance considering the non-idealities of OTRA was found to be

\[
L(\omega) = \frac{C_3 R_1 R_2 R_5}{R_4} \left[ 1 + \frac{C_p}{C_2} \left( 1 + \frac{R_0}{R_5} \right) \right].
\]

Thus, it is seen that due to the non-ideal effects, the actual value of the simulated inductor would be slightly more than the intended value. Furthermore, (15) can also be used to obtain a predistorted design of the circuit utilizing known values of \( C_3 \) and \( R_4 \).

From the plots shown in Figures 5 and 6 it is found that the resistive part remains nearly zero ohms as required, showing a value of 14.5\( \Omega \) at a frequency of 0.795 MHz and remains very small up to a frequency of about 10 MHz whereas the inductive part shows \( L = 2.759 \, \text{mH} \) as also predicted by the theoretical formula of (15) which remains almost invariant till a frequency of about 10 MHz. Hence, the usable frequency range of the circuit is till about 10 MHz.

3.2. Grounded FDNR. With \( Z_1 = R_1, Z_2 = R_2, Z_3 = 1/sC_3, Z_4 = R_4 \) and \( Z_5 = 1/sC_5 \) the expression for the input impedance considering the non-idealities of OTRA is found to be

\[
Z_{in}(\omega) = \frac{R_1}{s^2 C_3 C_5 R_2 R_4} \left[ \frac{s^2 C_3^2 C_4 R_2 R_4 (1 + (R_1/R_2) + (R_1/R_3) + (R_1/R_4)) + 1}{s (C_3^2/C_4) R_0 (1 + (R_0/R_5)) (1 + (R_1/R_5) + (R_1/R_4) + (R_1/R_2)) + 1} \right].
\]
From (17) it can be shown that $Z_{\text{in}}(j\omega)$ can be expressed as

$$Z_{\text{in}}(j\omega) = (1/j\omega C_{\text{eq}}) + (R_{\text{eq}}).$$

From SPICE simulations we have extracted plots showing variation of $R_{\text{eq}}(\omega)$ and $C_{\text{eq}}(\omega)$ as function of frequency ($\omega$) which are shown respectively in Figures 9 and 10, with component values taken as $R_1 = R_2 = R_3 = R_4 = 1 \text{ K} \Omega$ and $C_3 = 1 \text{nF}$ with ideal value of $C_{\text{eq}} = 1 \text{nF}$.

From the plots shown in Figures 9 and 10 it is found that the resistive part remains nearly constant showing a value of $R_{\text{eq}} = 5.2475 \Omega$ (which is quite small) up to a frequency of about 10 MHz whereas the equivalent capacitive value is $C_{\text{eq}} = 1.01 \text{nF}$ (as also verified by the theoretical formula) which remains almost invariant till a frequency of 10 MHz. Hence, the usable frequency range of the circuit is till about 10 MHz.

3.4. Grounded FDNC. With $Z_1 = R_1, Z_2 = 1/sC_2, Z_3 = R_3, Z_4 = 1/sC_4$ and $Z_5 = R_5$ the expression for the input impedance considering the non-idealties of OTRA was found to be

$$Z_{\text{in}} = s^2 C_2 C_4 R_3 R_5 \left[ \frac{s^4 C_2^2 R_3^2 + s C_2 R_3 [C_2/R_3] + [C_2 C_3/R_3] (1 + (R_3/R_1)) + [C_2 C_3/R_3] (1 + (R_3/R_1)) + [1 + (C_2 C_3/R_3)] (1 + (R_3/R_1))]}{s^4 C_2^2 C_4 R_3 R_5 + s^2 C_2 C_4 R_3 R_5 [C_2/R_3] + [C_2 C_3/R_3] (1 + (R_3/R_1)) + [1 + (C_2 C_3/R_3)] (1 + (R_3/R_1)) + [1 + (C_2 C_3/R_3)] (1 + (R_3/R_1))} \right].$$

From (18) it can be shown that $Z_{\text{in}}(j\omega)$ can be expressed as

$$Z_{\text{in}}(j\omega) = (-\omega^2 M_{\text{eq}}) + j\omega(L_{\text{eq}}).$$

From SPICE simulations we have extracted plots showing variation of $M_{\text{eq}}(\omega)$ and $L_{\text{eq}}(\omega)$ as function of frequency ($\omega$) which is shown respectively in Figures II and 12, with component values taken as $C_2 = C_4 = 0.001 \mu\text{F}, R_1 = R_2 = R_3 = 10 \text{ K} \Omega$ yielding an ideal value of $M = 1 \times 10^{-6} \Omega$.

From the plots shown in Figures II and 12 it is found that the resistive part remains nearly constant showing a value of $M_{\text{eq}} = 1.024 \times 10^{-6} \Omega$ (which is almost negligible) up to a frequency of about 10 MHz. Hence, the usable frequency range of the circuit is till about 10 MHz.

4. Application Examples

To verify the workability of the proposed structure we now show some sample application circuits and their verification using SPICE simulations.

4.1. Grounded Inductor. With the values of components chosen as $C_2 = 0.05 \text{nF}, R_1 = R_2 = R_4 = R_3 = 7.07 \text{ K} \Omega$, the simulated lossless grounded inductor has a value of 2.5 mH. The simulated ideal grounded inductor realized using positive generalized impedance simulator circuit shown in Figure 4 is used to design a Second-order band pass filter shown in
A CMOS implementation of the OTRA (taken from Figure 6 of [6] with 0.5 μm CMOS process parameters and aspect ratios the filter parameters are given by: (i) center frequency
The circuit realizes a Second-order band pass filter for which the transfer function is given by
\[ \frac{V_o}{V_{in}} = \frac{s(1/CR)}{s^2 + s(1/CR) + (1/LC)}. \] (19)

The circuit realizes a Second-order band pass filter for which the filter parameters are given by: (i) center frequency \( f_o = 1/2\pi \sqrt{LC} \) and (ii) bandwidth \( \omega_c/Q = 1/CR \). With the choice of impedances as \( Z_1 = R_1, Z_2 = R_2, Z_4 = R_4, Z_5 = R_5 \) and \( Z_2 = 1/sC_2 \), the input impedance of grounded inductor was found to be \( L = C_2R_1R_2R_3/R_4 \) resulting in the value of filter parameters as: (i) \( f_o = (1/2\pi) \sqrt{R_1C_2R_2R_3R_5} \) and (ii) \( \omega_c/Q = 1/CR \).

A Second-order band pass filter having a center frequency of \( f_o = 897.443 \) KHz, BW = 1.02584 MHz and \( Q = 0.89 \) was realized using this inductor by using the component values as \( C_2 = 0.05 \) nF, \( R_1 = R_3 = R_4 = R_5 = 7.07 \) KΩ. The OTRA was implemented using AD844 type CFOAs as per the schematic of Figure 2 of [4]. The experimentally observed frequency response is shown in Figure 14 which confirms the workability of the circuit as a band pass filter.

4.2. Grounded FDNR. This was used to realize a Second-order low pass filter consisting of a series RC branch (having \( R_s = 0.09 \) KΩ and \( C_s = 1 \) nF) and FDNR (having \( D = 4.84 \times 10^{-17} \) Ω with the choice of components taken as \( C_1 = 0.22 \) nF, \( R_2 = 1 \) KΩ, \( R_3 = 1 \) KΩ and \( R_4 = 1 \) KΩ). The simulated lossless grounded FDNR was used to design a Second-order low pass filter shown in Figure 15 for which the transfer function is given by
\[ \frac{V_o}{V_{in}} = \frac{(1/DR)}{s^2 + s(1/CR) + (1/DR)}. \] (20)

The transfer function thus obtained realizes a Second-order low pass filter for which the filter parameters are found to be: (i) cut-off frequency \( f_o = 1/2\pi \sqrt{DR} \) and (ii) quality factor \( Q = C\sqrt{R/D} \). With the choice of impedances as \( Z_1 = 1/sC_1, Z_2 = R_2, Z_4 = R_4, Z_5 = 1/sC_5 \) and \( Z_3 = R_3 \) the input impedance of an ideal grounded FDNR is given by \( D = C_1C_2R_2R_3/R_4 \) resulting in the value of filter parameters as: (i) \( f_o = (1/2\pi) \sqrt{R_4C_2R_2R_3} \) and (ii) \( Q = C_1\sqrt{R_4}C_2R_3R_5 \).

The SPICE generated frequency response using a CMOS implementation of the OTRA (taken from Figure 6 of [6] with 0.5 μm CMOS process parameters and aspect ratios
of MOSFETs as given in Table 2 therein of [6]) is shown in Figure 16, which confirms the validity of the FDNR realization.

4.3. Resistively-Variable Capacitor. This simulated capacitor was used to realize a variable cut-off frequency first order RC low pass (LP) filter circuit whose cut-off frequency was linearly controlled by varying the resistance $R_5$. The simulated capacitor realized using positive generalized impedance simulator circuit shown in Figure 4 was used to design a first order low pass filter circuit shown in Figure 17 for which the transfer function is given by

$$\frac{V_o}{V_{in}} = \frac{1}{1 + sCR}.$$  \hspace{1cm} (21)

The transfer function thus obtained realizes a first order low pass filter for which the cut-off frequency is $f_0 = 1/2\pi CR$. With component values $C_2 = C_4 = 0.001 \mu F$ and $R = R_1 = R_3 = R_5 = 10 \Omega$, the SPICE simulation results showed a resonant frequency of 15.625 KHz which is in good agreement with the theoretical value of $f_0 = 15.9$ KHz as shown in Figure 20.

The applications and the simulation results described earlier, thus, confirm the practical validity of the various modes of operation of the proposed configuration.

5. Conclusions

A new generalized positive (it is interesting to point out that a generalized negative impedance simulator using OTRAs can be devised by interchanging the input terminals of OTRA_1 and leaving the p-terminal of the same OTRA open with impedance $Z_4$ used in the feedback path with impedance $Z_5$ connected to the negative terminal. The performance, evaluation, and application of this circuit are, however, a matter of continuing investigations) impedance simulator using OTRAs was presented and its various applications were confirmed by hardware implementation of OTRAs using commercially available AD844-type CFOAs as well as a CMOS implementation of OTRA known earlier.

It is worth pointing out that with CMOS OTRAs and MOS capacitors, the special cases of the proposed configuration can be made completely compatible with CMOS technology by replacing CMOS voltage-controlled resistances (VCRs) in which case, the floating nature of the resistors employed would not create any difficulty since it is well known that grounded and floating VCRs both can be realized with exactly the same number of MOSFETs; for instance, see [29–31].
It is expected that the proposed configuration may find useful applications in the design of analog filters and oscillator design as well as in higher order filter design using methods based upon impedance simulation.

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