Design Rules for High Performance Tunnel Transistors from 2D Materials

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I. ABSTRACT

Tunneling field-effect transistors (TFETs) based on 2D materials are promising steep sub-threshold swing (SS) devices due to their tight gate control. There are two major methods to create the tunnel junction in these 2D TFETs: electrical and chemical doping. In this work, design guidelines for both electrically and chemically doped 2D TFETs are provided using full band atomicistic quantum transport simulations in conjunction with analytic modeling. Moreover, several 2D TFETs’ performance boosters such as strain, source doping, and equivalent oxide thickness (EOT) are studied. Later on, these performance boosters are analyzed within a novel figure-of-merit plot (i.e. constant ON-current plot).

II. INTRODUCTION

Transistor scaling has driven device designs toward thinner channels for better gate control over the channel. 2D materials can provide a shortcut to the ultimate channel thickness scaling: an atomically thin channel. A tight gate control is important in FETs to obtain a 1-to-1 band movement in the channel potential with respect to the gate voltage. The tight gate control is even more crucial for the performance of tunnel FETs (TFETs) [1], [2] since the scaling length and accordingly tunneling distance decreases with a better gate control [3]–[10]. The exponential dependence of the tunneling current on the tunneling distance emphasizes the role of a thin channel and tight gate control in TFETs.

Some 2D materials, such as graphene or silicene suffer from the lack of a bandgap \( (E_g) \) and are not suitable for transistor applications. On the other hand, 2D materials such as transition metal dichalcogenides (TMD: MoS\(_2\), WSe\(_2\), MoTe\(_2\), etc.) exhibit a sizable direct bandgap in their monolayer configuration. Among those, monolayer WTe\(_2\) shows particular promise for high performance TFET applications [4] due to its rather small effective mass and an expected bandgap of about 0.75eV [13]. Note that a bandgap of about \( (1.1 \sim 1.5)qV_{DD} \) provides the best performance in TFETs, where \( V_{DD} \) is the supply voltage [11], which means that for a \( V_{DD} \) of about 0.5V an \( E_g \) range of 0.55-0.75eV is expected to provide best performance. Unfortunately, however, experiments indicate that the WTe\(_2\) 2H phase may not be stable [14].

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III. SIMULATION METHOD

According to our previous analysis [4] WSe\(_2\) is the next best choice in terms of existing TMD materials for TFET applications after WTe\(_2\). Hence, monolayer WSe\(_2\) is chosen.
for our atomistic simulations and the detailed analysis of various performance boosters. The WSe$_2$ Hamiltonian employs an sp$^3$d$^5$ 2nd nearest neighbor tight-binding (TB) model. The semi-empirical TB parameters are optimized based on first principles bandstructures (E-K) calculated from density functional theory (DFT) with the generalized gradient approximation (GGA) \cite{4}. A similar TB parameter fitting procedure based on DFT E-K has been used in the presence of strain. DFT-GGA has been chosen since it provides band gaps and effective masses in TMDs comparable to experimental measurements \cite{13}.

In this work, self-consistent Poisson-NEGF (non-equilibrium Green’s function) methodology has been employed within the tight-binding description. Because in-plane and out-of-plane dielectric constants ($\epsilon_{in}$ and $\epsilon_{out}$) of WSe$_2$ are different, the Poisson equation reads as follows \cite{4} if the z direction is considered to be along the c-axis of the TMDs:

$$\frac{d}{dx}(\epsilon_{in} \frac{dV}{dx}) + \frac{d}{dy}(\epsilon_{in} \frac{dV}{dy}) + \frac{d}{dz}(\epsilon_{out} \frac{dV}{dz}) = -\rho \quad (1)$$

where $V$ and $\rho$ are the electrostatic potential and total charge, respectively. The dielectric constant values ($\epsilon_{in}$ and $\epsilon_{out}$) of WSe$_2$ are taken from ab-initio studies \cite{24}. In this work, quantum transport simulations have been performed with our simulation tool NEMO5 \cite{33}–\cite{35}.

IV. Results

In spite of the similarities between CD-TFETs and ED-TFETs, they obey rather different scaling rules and design guidelines \cite{26}, \cite{29}. We will discuss the impact of the various performance boosters in CD-TFETs and ED-TFETs in the following sections.

A. Chemically doped TMD TFETs

First, the design aspects of chemically doped (CD) TFETs are studied with the structure shown in Fig. 1. A 15nm long monolayer WSe$_2$ channel with $V_{DD}$ of 0.5V is considered in all CD-TFET simulations. We have identified a number of critical factors enhancing the performance of 2D CD-TFETs: strain, high doping levels of the source ($N_D$), and small EOT values. Fig. 2 shows transfer characteristics of a WSe$_2$ CD-TFET. The black current-voltage (I-V) curve shows the results for the reference transistor with an EOT=2nm, $N_D$=1e20 cm$^{-3}$, and no strain. At the first step, EOT is decreased to 0.45nm (blue curve). In the second step, the doping level is increased to 2e20 cm$^{-3}$ (pink curve), and finally a biaxial strain of 3% is applied (red curve). Notice that these performance boosters not only improve the ON-current, but also they enhance the OFF-state performance by decreasing SS and increasing $I_{on}$ \cite{36}.

Fig. 3: SS as a function of drain-current $I_D$ for performance boosted WSe$_2$ CD-TFETs. Starting with EOT=2nm (black curve), EOT is then decreased to 0.45nm (blue curve). Subsequently, the doping level is increased to 2e20 cm$^{-3}$ (pink curve), and finally a biaxial strain of 3% is applied (red curve). Notice that these performance boosters not only improve the ON-current, but also they enhance the OFF-state performance by decreasing SS and increasing $I_{on}$ \cite{36}.

Fig. 4: Constant ON-current figure-of-merit. The blue lines show a constant current for a set of device design parameters. The ON-current of TFETs mainly depends on the band bending distance ($\Lambda$) and material properties of the channel $m^*_r$ and $E_g$. The device design determines $\Lambda$ which has two main components: a) the depletion width of the source ($W_D$) and b) the scaling length of the gated region ($\lambda$). Increasing doping reduces $W_D$, while decreasing the EOT, reduces $\lambda$. Both of these boosters result in a reduction in $\Lambda$. On the other hand, strain changes the material properties without affecting $\Lambda$. 

Fig. 2: Transfer characteristics of a chemically doped monolayer WSe$_2$ TFET with EOT=2nm (black curve), EOT=0.45nm (blue curve), doping level of 2e20 cm$^{-3}$ (pink curve), and biaxial strain of 3% (red curve). At each level, the previous boosting factor is included. Increasing the biaxial strain, and source doping level and decreasing EOT boosts the ON-current of 2D TFETs significantly.
Effective mass of monolayer WSe$_2$ decreases by application of biaxial strain; e.g. 3% biaxial strain reduces the reduced effective mass $m^*_r$ and the band gap $E_g$ by about 10% and 22%, respectively. Application of all performance boosters increases $I_{ON}$ by more than 2 orders of magnitude.

Fig. 3 shows the impact of the performance boosters (i.e. strain, source doping, and EOT) on the OFF-state performance. SS is plotted versus the drain current at which SS is calculated [28]. It is shown that the performance boosters not only increase $I_{ON}$, but also increase $I_{60}$ (the current level where SS=60 mV/dec [36]) and decrease SS. About 3 orders of magnitude increase in $I_{60}$ and a factor of 3 reduction in SS are obtained combining the performance boosters.

The ON-state performance of TFETs mainly depends on 1) the band bending distance $\Lambda$ (shown in Fig. 4) which is determined by the device design and 2) the channel material properties: $m^*_r$ and $E_g$ [26]. Fig. 4 shows a constant ON-current plot. Notice that $I_{ON}$ depends exponentially on the product of $\Lambda$ and $\sqrt{m^*_rE_g}$ and since both axes are plotted on a logarithmic scale, constant current contours appear as parallel lines [27]. To achieve a higher $I_{ON}$, one can reduce $\Lambda$ or $\sqrt{m^*_rE_g}$. In CD-TFETs, $\Lambda$ is composed of two terms: 1) the scaling length ($\lambda$) under the gated region and 2) the source depletion width ($W_D$). Increasing the source doping level, reduces $W_D$, and reducing the EOT, reduces $\Lambda$. Consequently $\Lambda$ is also reduced. On the other hand, strain changes the material properties without affecting $\Lambda$. Fig. 4 therefore portrays the interplay between design and material parameters and the impact of the various performance boosters.

**B. Electrically doped TMD TFETs**

In this part, the performance analysis of 2D electrically doped (ED) TFETs is discussed. Notice that the design guidelines for ED-TFETs are rather different due to the presence of fringing fields. Fig. 1b shows the schematic of a double gated ED-TFET [29]. In ED-TFETs, the tunnel junction is created through two adjacent gates with opposite polarities. One of these 2 gates is a conventional gate and the other one is connected to the source contact which tunes the electrically induced doping level of that side. Each gate has a length of 12nm and $V_{DS}$ is set to 0.5V in all ED-TFET simulations. The major players affecting the performance of ED-TFETs are: 1) the spacing between the gates: $\epsilon$ (Fig. 1b), 2) the thickness of the oxide (not the EOT), 3) the dielectric constant of the spacing region ($\epsilon_S$) [32], and 4) strain. Fig. 5 shows that $t_{ox}$ and $\epsilon_S$ have much higher impact on the performance of ED-TFETs compared to $S$ and strain.

Fig. 4 shows how the OFF-state performance of the 2D ED-TFETs gets affected by different design parameters. It is
and ED-TFETs: 1) the expression for the scaling length and enhance fabrication feasibility. One can use a low-k back oxide to avoid performance degradation if the arrows would shift to the left and a higher ON-current could be achieved. This shows the importance of the choice of materials for 2D TFETs.

apparent that both SS and $I_{SS}$ significantly improve using a thinner oxide, smaller spacing, and a smaller spacer dielectric constant. The most effective improvement comes from a smaller spacer dielectric constant and thinner oxide which increases $I_{SS}$ by more than 4 orders of magnitude.

One of the main differences between 2D CD-TFETs and ED-TFETs is that the concept of EOT is not applicable to ED-TFETs. In the case of ED-TFETs, the electric field at the tunnel junction ($E_T$) is inversely proportional to the total thickness of the device (including top and bottom oxides) [29]–[31]:

$$E_T \propto \frac{1}{t_{top} + t_{bot}}$$  \hspace{1cm} (2)

This point is usually ignored in the design of electrically doped devices; a common layout uses a thick back oxide which leads to a small $E_T$. This problem can be overcome by using a back oxide with low dielectric constant compared to the top oxide ($\epsilon_{bot} \ll \epsilon_{top}$). Fig. 7b shows the potential profile of an electrically doped TFETs with thin and thick back oxides with high-k dielectric on the top and bottom. It is apparent that a thick back oxide increases the potential spread and reduces $E_T$. Fig. 7b shows that a low-k dielectric back gate can reduce the impact of thick back gate oxide significantly.

$$E_T \propto \frac{1}{t_{top}}$$  \hspace{1cm} (3)

These results suggests that if a thin back oxide with gates aligned with the top gates is experimentally challenging, one can use a low-k back oxide to avoid performance degradation and enhance fabrication feasibility.

There are two main differences between $\Lambda$ of CD-TFETs and ED-TFETs: 1) the expression for the scaling length $\lambda$ [29] and 2) $\lambda$ replaces $W_D$ (Fig. 8). The constant $I_{ON}$ plot of the WSe$_2$ ED-TFET is shown in Fig. 8.

**CONCLUSION**

In conclusion, important design parameters of 2D CD- and ED-TFETs are discussed here. It is shown that the EOT and source doping ($N_D$) are the main players in the case of CD-TFETs, whereas the performance of ED-TFETs mainly depends on $t_{ox}$ and $\epsilon_S$. Considering performance boosters can in principle increase the ON-current of both CD- and ED-TFETs by orders of magnitude.

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![Fig. 8: Constant ON-current figure-of-merit for WSe$_2$ ED-TFETs. The y-axis shows the impact of the bending distance $\Lambda$ which has one main component: the scaling length of the gated region ($\lambda$). Notice that the expression for $\lambda$ is different in ED-TFETs if compared with CD-TFETs. Decreasing $t_{ox}$, $\epsilon_S$, and $S$ reduces $\lambda$ and $\Lambda$ and increases $I_{ON}$. If another material with smaller $E_g$ and $m_r$ (e.g. WTe$_2$) is used instead of WSe$_2$, the arrows would shift to the left and a higher ON-current could be achieved. This shows the importance of the choice of materials for 2D TFETs.](image-url)
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