Structural characterization of GaN/AIN layers on 3C-SiC/Si(111) by TEM

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Abstract. In the present work 20-µm-thick GaN epilayers have been grown by hydride–chloride vapor-phase epitaxy on 1.5-inch Si(111) substrates with AlN and SiC interlayers. Silicon carbide has been obtained by an original method of solid phase epitaxy. The transmission electron microscopy analysis revealed the effect of AlN layer structure on the quality of the gallium nitride epilayer. It is established that pores with dimensions of several nanometres formed on an AlN/GaN interface favour the growth of an epitaxial weakly strained single crystalline GaN layer. A good quality of the obtained GaN epilayers (local dislocation density is about $4 \times 10^7 \text{ cm}^{-2}$, average density $\sim 10^9 \text{ cm}^{-2}$) is demonstrated. The silicon substrate structure features near to a SiC interlayer will be discussed.

1. Introduction

Gallium nitride (GaN)-based heterostructures are extensively used in light emitting devices, high frequency, high power devices, and high-electron-mobility transistor substrates. The absence of low-cost GaN substrates stimulates a search for materials appropriate for heteroepitaxy. The use of sapphire as a substrate results in a high density of dislocations because of a significant (~13%) lattice mismatch in the (0001) interface plane [1]. At the same time, silicon carbide (SiC) substrates that are more suitable from the standpoint of lattice matching, are too expensive and have small areas. In recent years, much attention has been given to the growth of GaN on silicon (Si) substrates [2]. This interest is related, first, to the prospects for integration of the gallium-nitride and silicon electronics technologies and, second, to the possibility of using inexpensive single crystal silicon substrates, available in large diameters (up to 150 mm) and with reasonable thermal and electrical conductivity. However, GaN layers grown on Si suffer from crack generation, possibly due to the strain induced by a large lattice mismatch (17%) and difference in thermal expansion coefficients (33%) between GaN and Si. On the other hand, the lattice mismatch between (0001) GaN and (111) 3C-SiC is only 3% [3]. Thus, high quality GaN is expected by employing 3C-SiC as intermediate layers (ILs) in the GaN/Si system. The aim of this work is to study the influence of ILs morphology on the structural quality of GaN layers.
2. Experimental details
A thin SiC layer (110 nm) was initially formed on a Si(111) substrate by means of solid phase epitaxy [4,5], and then AlN (260 nm) and GaN (15 µm) layers were sequentially grown over the silicon carbide interlayer by the method of hydride–chloride vapour-phase epitaxy (HVPE) (sample 1) using a procedure described in [6]. Sample 2 differed from sample 1 in thickness of SiC (350 nm), AlN (100 nm) and GaN (20 µm) layers. The microstructure of GaN/AlN/3C-SiC/Si(111) heterostructure was examined by cross-sectional transmission electron microscopy (XTEM). Samples for XTEM were prepared by mechanical thinning with the use of tripod and ion milling in Gatan Precision Ion Polishing system at 4 kV. Conventional TEM study was carried out with a Philips EM420 transmission electron microscope operating at 100 kV.

3. Results and discussion
Figure 1 shows the microstructure of sample 1. The analysis of the selected area electron diffraction pattern (SAED) recorded from area of interfaces has confirmed that layers are epitaxial (figure 1b). The TEM analysis revealed the epitaxial relationships:

\[ (0001)\text{GaN}|| (111)\text{3C-SiC} || (111)\text{Si} \]
\[ [0002]\text{GaN}|| [11\bar{2}0]\text{GaN} || [1\bar{1}0]3\text{C-SiC} || [1\bar{1}0]\text{Si}. \]

Figure 1. a: Cross-sectional TEM image of GaN/AlN/3C-SiC/Si(111) heterostructure (sample 1); b: SAED recorded from round area (figure 1). Diffraction spots of 0 0 0 2 (GaN and AlN) and 1 1 1 3 SiC are superimposed; c: a void in Si substrate; d: SAED recorded from the void.

The SiC interlayer was a product of chemical reaction between crystalline silicon and carbon monoxide [5].

\[ 2\text{Si(cr)} + \text{CO(v)} = \text{SiC(cr)} + \text{SiO(v)} \uparrow \]

Fort the formation of one molecule of SiC two atoms Si are necessary, and one of them volatilizes, which leads to the formation of voids in silicon near to interface Si/SiC [5,7]. The thickness of the defective layer in the substrate reaches 3 µm (figure 1). According to [5], the volume of pores must be approximately equal to the that of grown silicon carbide. In the electron micrograph, the total volume of voids seems to be somewhat greater, but it should be taken into account that the voids could be additionally increased in size as a result of etching with argon ions in the course of sample preparation. These voids improve the quality of a growing epilayer, since a decrease in the contact area leads to a reduction of elastic stresses at the interface that are caused by lattice mismatch and a difference in the coefficients of thermal expansion of the substrate and deposit layer.
TEM investigation has revealed that besides the SiC epilayer formed on the surface of a silicon substrate, inside of voids silicon carbide is also formed as a result of a chemical reaction between CO and the gaseous silicon (see streaky structure in figure 1c). Streaking of diffraction spots arises due to a large number of basal stacking faults (figure 1d).

In the SiC layer there are a lot of defects like stacking faults and dislocations, but there are no cracks. In [8], the presence or absence of cracks is connected to the thickness of the SiC layer: if its thickness is larger than \( x \), the formation of cracks is suppressed. The value of \( x \), according to [8], lies in the range of 0.05–1 µm. Though the thickness of the silicon carbide layer in our case (figure 2) also gets to this range, we consider that here the method of SiC growth has played a main part in the prevention of crack formation.

**Figure 2.** a — a pore in AlN layer at SiC/AlN interface; b — pores at AlN/GaN interface.

Generally, ILs have a smooth surface except for rare protrusions (figures 2, 3). In the AlN layer, besides planar defects and dislocations, a small amount of pores in the size range of 10–20 nm is revealed. These pores are located on SiC/AlN and AlN/GaN interfaces.

**Figure 3.** Two-beam images of the same area taken with different \( g \) vectors showing absence of \( c \)-screw dislocations. a: \( g=(0002) \); b: \( g=(1120) \).

In the GaN layer presented in figure 3, it is possible to identify three areas. A very defective area (in figure not shown) of width 50 nm begins at the Si/SiC interface. The area A with a low density of dislocations follows further. In area B, the density is even lower. The reduction of the dislocation density is possible particularly because of a small number of threading dispositions with lines parallel to the \( c \) axis. Burgers vectors have been determined by two beam analysis. The dislocation density...
near the AlN layer is too high for the identification of these dislocations. The results of TEM analyses of distribution of different types of dislocations in sample 1 are summarized in Table 1.

Table 1. Distribution of different types of dislocations in different areas of sample 1 obtained by TEM analysis.

| Type of dislocation | Burgers vector | Density (cm$^{-2}$) | Area under investigation (figure 3a) |
|---------------------|----------------|--------------------|-------------------------------------|
| Screw               | $a=1/3<11\overline{2}0>$ | $4\times10^7$     | A+B                                 |
| Mixed               | $a=1/3<11\overline{2}0>$ | $1.4\times10^8$   | A+B                                 |
| Mixed               | $a+c=1/3<11\overline{2}3>$ | $1\times10^9$     | A+B                                 |
| All types           | $c=0001>$              | 0                  | A+B                                 |
| All types           | $a$, $c$ and $a+c$    | $3\times10^9$     | A                                   |
| All types           | $a$, $c$ and $a+c$    | $6\times10^9$     | B                                   |

Figure 4 shows the structure of sample 2. The main difference of this structure from the structure of sample 1 is a presence of a system of pores on the AlN/GaN interface. The subsequent nucleation and growth of GaN grains starts on the tops of pyramids while pores are left between pyramids. The pores can be produced by the impurities collected on the growth fronts of the GaN layer [9]. These pores lower the stresses generated by mismatch between the lattice parameters, which leads to improvement of quality of the GaN layer. Results of measurements have shown that local dislocation density is about $4\times10^7$ cm$^{-2}$, average density $\sim10^9$ cm$^{-2}$.

4. Conclusions

GaN epilayers grown by HVPE on 1.5-inch Si(111) substrates with AlN and SiC interlayers have been studied by TEM. A comparison of structures of samples with different morphology of interlayers has shown that a system of pores on the AlN/GaN interface lowered the dislocation density in the GaN layer. In the GaN layer the fraction of dislocation lines parallel to the $c$ axis is small and $c=0001>$ dislocations have not been revealed. Good quality GaN epilayers (with local dislocation density about $4\times10^7$ cm$^{-2}$, average density $\sim10^9$ cm$^{-2}$, compare [2]) have been grown.

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