AccSS3D: Accelerator for Spatially Sparse 3D DNNs

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Abstract—Semantic understanding and completion of real-world scenes is a foundational primitive of 3D Visual perception widely used in high-level applications such as robotics, medical imaging, autonomous driving and navigation. Due to the curse of dimensionality, compute and memory requirements for 3D scene understanding grow in cubic complexity with voxel resolution, posing a huge impediment to realizing real-time energy-efficient deployments. The inherent spatial sparsity present in the 3D world due to free space is fundamentally different from the channel-wise sparsity that has been extensively studied. We present ACCELERATOR FOR SPATIALLY SPARSE 3D DNNs (AccSS3D), the first end-to-end solution for accelerating 3D scene understanding by exploiting the ample spatial sparsity. As an algorithm-dataflow-architecture co-designed system specialized for spatially-sparse 3D scene understanding, AccSS3D includes novel spatial locality-aware metadata structures, a near-zero latency and spatial sparsity-aware dataflow optimizer, a surface orientation aware pointcloud reordering algorithm and a co-designed hardware accelerator for spatial sparsity that exploits data reuse through systolic and multicast interconnects. The SSNN accelerator core together with the 64 KB of L1 memory requires 0.92 mm2 of area in 16nm process at 1 GHz. Overall, AccSS3D achieves 16.8x speedup and a 2232x energy efficiency improvement for 3D sparse convolution compared to an Intel-i7-8700K 4-core CPU, which translates to a 11.8x end-to-end 3D semantic segmentation speedup and a 24.8x energy efficiency improvement (iso technology node).

I. INTRODUCTION

Understanding 3D geometry and semantics of a scene is essential to many real-world systems including but not limited to autonomous driving, robotics, remote sensing, AR/VR and medical treatment [6], [16], [31], [34], [62]. With rapid growth in 3D acquisition technologies, 3D sensors are becoming increasingly available and affordable for rich data generation through various types of 3D scanners, LiDARs and RGB-D cameras. 3D data is usually represented in various formats like pointclouds, meshes, depth maps and volumetric grids. Deep Learning techniques have disrupted traditional methods in domains such as computer vision, speech processing and machine translation that operate over images, videos, audio, text and other forms of data. However, DL methods face severe challenges in processing 3D visual data due to the high dimensionality and the unstructured nature of 3D data.

Several methods (Figure 1) have been proposed for various 3D visual AI applications such as shape classification, object detection, tracking, and scene segmentation. 3D scene segmentation requires extraction of global geometric structure and intricate details of each point in the 3D pointcloud. Semantic segmentation (Figure 2) aims to divide a pointcloud into several subsets based on real world semantics. Instance segmentation identifies instances of each semantic object, while part segmentation further breaks each instance into different parts. Scene completion predicts and labels missing regions arising from sensing inaccuracies or occlusions.

Point based networks (Table I) directly operate over irregular, orderless and unstructured pointclouds, making it infeasible to directly apply standard CNNs. Performance of multi-view 2D projection based methods is highly sensitive to viewpoint selection and these methods also do not fully exploit underlying 3D geometry. Since volumetric representation preserves neighbourhood structure of pointcloud and regular data formats allow direct application of standard 3D convolutions, volumetric projection based methods provide higher accuracy. However, voxelization introduces discretization artifacts and causes information loss. A low resolution voxel representation can degrade accuracy, whereas high resolution pointclouds cubically grow compute and memory requirements (Figure 5). This poses a huge impediment in achieving real-time real-world deployments of visual AI that fundamentally require low-latency and low-energy 3D scene understanding capability. Thankfully, the ample free space in 3D scenes provides significant opportunity to exploit the inherent spatial sparsity.

For dense DNNs, multiple accelerator designs [17], [22],
TABLE I

| Category | Method                        | mIoU  |
|-----------|-------------------------------|-------|
| Projection| PointNet [34]                 | 71.7  |
| Volumetric| Voxel-Net [36]                | 72.5  |
| Volumetric| PointCNN [32]                 | 73.6  |
| Multiview | Convolution [64]             | 65.6  |
| Multiview | PointCNN [32]                 | 64.0  |
| Multiview | PointSIFT [28]                | 40.9  |
| Multiview | PointWiseMLP [51]            | 33.9  |
|           | VoxelNet [36]                 | 72.5  |

A. Our Contribution

Driven by a detailed end-to-end performance characterization of the Sparse Convolution Network (SCN), we present ACCELERATOR FOR SPATIALLY SPARSE 3D DNNs, the first end-to-end solution for accelerating 3D scene segmentation by exploiting spatial sparsity. In brief, our key contributions are as follows:

1. We introduce a novel locality-aware metadata structure, COIR, for voxel data that stores spatial locality information by encoding active receptive fields at each location. We also present a novel pointcloud reordering technique, SOAR, that maximizes spatial data locality and reuse across all DNN layers for multi-level memory architectures.

2. We present (to the best of our knowledge) the first-ever sparsity aware dataflow optimizer, SPADE, that analyzes the local geometry structure of a pointcloud and uses the sparsity attributes to maximize data reuse across all DNN layers. To meet real-time requirements, we enable latency-critical dataflow optimizer routines to be run in offline mode while retaining the benefits of the sparsity-aware dataflow.

3. We present a novel sparse-accelerator for spatially-sparse DNNs, SSpNNA, whose scheduler maximizes weight reuse. Systolic and multicast interconnects in the PE arrays maximize input feature-map reuse. We also propose, AdMAC, an accelerator for fast 3D neighbourhood search and COIR metadata creation and CAROM, a joint dataflow optimization technique for multi-level memory hierarchies. We show how a scaled-up architecture based on AccSS3D accelerates 3D sparse convolution by 16.8x compared to a 4-core CPU baseline with a 2232x improvement in energy efficiency.

II. BACKGROUND

Recent algorithmic advances [13], [56], [55] extended 2D-CNNs to 3D to recognize 3D objects and enabled semantic segmentation of real-world 3D scenes. However, due to the curse of dimensionality, compute and memory requirements grow in cubic complexity with voxel resolution.

Free space in 3D scenes is a source of inherent spatial sparsity, offering high opportunity for efficient processing. Recent algorithms [18], [42], [43] exploit this spatial sparsity by processing only those voxels (active voxels) that are in the vicinity of a surface boundary. They transform 3D sparse data into a list of active voxels for compressed storage and use a map [26], [50] to retrieve lists of indices based on 3D coordinates. Graham et al. [19] introduced Sparse Convolution Network (SCN) using the novel Valid Sparse Convolution (VSC) that provides significant reduction in compute and memory costs by considering output voxels as active only if the corresponding input voxel is active. This retains the sparsity structure of feature maps across the network and paves the way for achieving real-time complex 3D scene understanding. Zhang et al. [61] extended SCN to use Spatial Group Convolution, dividing the pointcloud into groups, further reducing compute without accuracy loss. Several systems employ encoder-decoder U-net topologies [12], [14], [33], [45], [46], [53], [54], [57], [59], [60], with layers that reduce spatial resolution (strided convolutions) followed by upsampling layers (deconvolutions), interspersed with VSC layers.

III. MOTIVATION

A. Increasing complexity of 3D Visual processing

Over the years, compute/memory requirements for 3D visual processing have increased multi-fold. (Table I). While 3D volumetric representations enable higher accuracy (Table I), low-resolution representation can hurt accuracy (Figure 5).
Though compute and memory requirements grow in cubic order with resolution size, the free space in 3D scenes, a source of exploitable ‘spatial sparsity’, motivates a hardware-software co-designed approach to acceleration of 3D visual processing.

B. Sparse Convolution Network (SCN) workload profile

Figure 4 shows the runtime CPU profile of SCN as a representative workload. The middle layers take much lower execution time than initial and last few layers as in the U-net, the middle layers operate on lowest resolution needing lower compute. As the order of voxel processing can be different from the memory layout, a gather operation for inputs and scattered write for outputs is required. Overall, Input Gather and Output Write dominates across the layers, due to the weight stationary dataflow, where input-output index pairs are created and processed for each weight plane independently. These components are majorly dominant for the initial and last few layers, where the voxel resolution sizes are higher. Lack of tiled execution and inability of CPU caches to hold the entire large pointcloud significantly hurts data reuse.

We observe that the performance of the workload scales poorly with number of cores and flattens beyond 4 cores (Figure 4). Further analysis shows that thread synchronization (spin locks) and thread creation events (both of which scale with #cores), increased load/store traffic for shared data, and increased DRAM bandwidth bottlenecks are responsible for this lack of scaling. On an Nvidia GPU, SCN performance improves by 2.34X over single-core CPU (Figure 5), but effective GPU utilization is low due to high register usage per thread, thereby limiting the number of threads that simultaneously execute. By recompiling GPU kernels to enforce fewer registers per thread, running thread count can be increased, but performance saturates due to memory load-store bottlenecks.

### D. Accelerator Options for 3D Spatial Sparsity

As discussed in Section III-C, storing 3D spatially-sparse data in 1D compressed format leads to inefficient execution due to irregular data accesses as convolution operations need to be performed on spatially proximate points in 3D space while the data is stored in 1D compressed format. We discuss two potential ways to accelerate spatially sparse 3D processing:

1) **Generic GEMM-based Acceleration:** Implement 3D sparse convolution as a dense-GEMM using efficient gather/scatter operations and performing GEMM over the regularized data structure similar to reference CPU implementation (Figure 4). **Challenges:** a) Since a 3D convolution is mapped onto a GEMM engine, input/output features need to be re-fetched as many times as the local receptive field, requiring prohibitively large data transfers and bandwidth. b) Due to input-dependent sparsity, data-specific source/destination rulebook tables need to be created by the host to enable a gather/scatter engine to perform explicit data copies. When local sparsity is medium-to-high and the point-cloud is large, the rulebook can significantly increase size and bandwidth requirement.

2) **Specialized Acceleration for 3D Sparsity:** Build specialized implementation to locate input/output data on-the-fly while performing 3D sparse convolution on a pool of MACs. **Challenges:** a) While custom acceleration for 3D sparsity can entirely eliminate the need for explicit metadata/rulebook generation, re-computation of input/output data addresses would be required for each DNN layer with the same resolution and at every accelerator core in the system. b) The number of lookups into the sparse hash-map required per unit compute is input sparsity-dependent. So, either the convolution engine will suffer significant utilization loss due to the high variability in the local receptive field OR to cover the variable latency
Fig. 4. Performance characterization of SCN [13] inference for a typical ScanNet [11] dataset on Intel-i7-8700K CPU with single core execution @ 3.7GHz. 
(a) Layer-wise runtime and break-up into constituent functions (b) Runtime break-up across all layers (c) Performance scaling with multi-core execution.

Fig. 5. Correlation between compute needs and accuracy (mIoU) as a function of resolution obtained by downsampling input pointclouds in ScanNet [11].

Fig. 6. SCN performance characterization on Nvidia GeForce-GTX-1080 @1.6GHz. Though GPU is processing for most of the time, average GPU core utilization is significantly low at 21% due to high register usage and bandwidth requirement, the local buffering would need to be prohibitively large. We propose in section IV-D a semi-specialized accelerator for 3D sparsity which can process a compressed metadata structure while adopting a tile-based sparsity-aware dataflow for efficient data-movement.

E. Custom Accelerator Requirements for 3D Spatial Sparsity

State-of-the-art sparse accelerators [22], [29], [41], [63] have been proposed for sparse matrix multiply or sparse DNN models. In general, these sparse accelerators are composed of two major blocks: 1) a Front-end which processes metadata of input operands (feature-maps and weights) locating pairs of non-zero input operands and 2) a Back-end for performing valid operations (MAC, activation, pooling etc.) through PEs. Proposals such as Sparten [17] also schedule work efficiently such that the imbalance between compute engines can be mitigated. We discuss challenges in adopting prior sparse- accelerators for 3D spatially sparse data processing:

A) Front-end: for 3D spatially sparse convolution, valid input pair selection depends solely on whether the voxel is active in the receptive field in the input pointcloud and not on the weights. Further, the selection logic (Figure 7) significantly decreases the imbalance between compute engines.

| TABLE III | MICRO-OPS AND DATA ACCESSES SAVINGS WITH COARSE LEVEL OF WORK-SCHEDULING |
|-----------|-------------------------------------------------|
| Layers    | Type | Total Ops | uOps | Data-Accesses Savings |
|-----------|------|-----------|------|-----------------------|
| L2        | SCN  | 1.3e+9    | 2.5e+6 | 1.93x |
| L12       | Conv | 4.4e+8    | 8.6e+5 | 1.94x |
| L24       | Dconv| 1.7e+8    | 2.7e+6 | 1.75x |
| L35       | SCN  | 5.4e+9    | 4.2e+7 | 1.88x |

IV. HARDWARE-SOFTWARE CO-DESIGNED ACCELERATION FOR 3D SPATIAL SPARSITY

A. Locality aware Data-structure (COIR)

Workload analysis in Section III-E provided the following insights: 1) performing convolution for all the voxels together in the receptive field (i.e. neighbourhood points) can reduce data accesses for input/output feature maps 2) storing all input point indices per output point (or vice a versa) can achieve metadata compression compared to weight wise listing of input pairs [18]. Metadata size savings could be significantly higher for denser pointclouds. Inspired by these insights, we propose a novel metadata structure (COIR) with two flavors 1) Compressed Output Response Field (CORF), 2) Compressed Input Receptive Field (CIRF) (Figure 7). In CORF, each metadata entry corresponds to a unique output point and consists of 1) the index of the input point, 2) indices of all the points in the output space in the response field of the input point. In addition, relative location of each neighbour is also required to select the appropriate weight index for convolution operation. For this, a weight bit-mask is stored for each entry with ‘1’s indicating valid neighbours and bit-locations indicating corresponding weight indices. Similarly, each CIRF entry contains the index of a unique output point, the indices of all the input points in the receptive field required to compute feature map for the output point and bit-masks...
for weight index selection. Two flavours of metadata are motivated by the observation that for the layers with resolution change (input and output space having different resolution), input to output mapping is not one-to-one. Hence, based on the sparsity in the pointcloud and the type of convolution (upsampling or downsampling) picking the right flavor could provide higher compression and data-savings over the other.

B. Point-cloud Reordering (SOAR)

COIR improves data reuse of input points with CORF (or output points with CIRF) by performing convolution across multiple neighbours per element access, but it doesn’t ensure data reuse of neighbours across multiple input or output points. To maximize data reuse for neighbours as well, entries in the metadata needs to be ordered such that the entries with shared neighbours are co-located in the metadata structure and processed in close temporal vicinity. To achieve this, we propose Surface Orientation Aware Reordering (SOAR) of the pointcloud. We first create an Adjacency Map with the voxel index as key and a list of indices to all its neighbours as value. When provided as input the maximum number of voxels for which data can fit in the on-chip memory, SOAR pushes all its neighbours to a Neighbour Queue and pops out voxels one-by-one. If a voxel is already selected in previous chunks, it gets dropped otherwise it is inserted into the m-ary tree as a child node to the first neighbour in breadth-first order. The inserted voxel is then tagged as selected and all its neighbours are added to the Neighbour Queue. This process continues till the number of voxels in the m-ary tree matches with the provided threshold, upon which the m-ary tree is selected as the desired chunk with voxels in the breadth-first order. The root node for the next chunk is selected among voxels in the Neighbour Queue with minimal number of neighbours and then this queue is flushed. This process gets completed when all the voxels in the pointcloud are divided into chunks.

C. Sparsity Aware Dataflow (SPADE)

Section II-C highlighted two key challenges of tiling 3D spatially sparse data: 1) memory requirement varies highly due to input dependent spatial sparsity 2) data accesses can not be estimated through mathematical expressions due to irregular data-structures. In this section, we propose a framework for dataflow exploration for spatially sparse data processing.

For a layer $\mathcal{L}$, let the total number of input voxels, output voxels, filter size, input channels, output channels and metadata size be represented as $I$, $O$, $K$, $C$, $N$ and $M$ respectively. And if $\Delta$’s correspond to respective values in a given tile $T$ (Figure 9), then the tile size $\Delta T$ can be expressed as:

$$\Delta T = (\Delta I, \Delta C) + (\Delta O, \Delta N) + (\Delta K, \Delta C, \Delta N) + \Delta M$$

(1)

For a number of output voxels ($\Delta O$) in the tile, required number of input voxels and metadata size could be obtained per region ($R_{i}^{\Delta O}$) as:

$$\Delta I = f_{I}(R_{i}^{\Delta O}, \Delta O), \Delta M = f_{MO}(R_{i}^{\Delta O}, \Delta O)$$

(2)

Tile size $\Delta T$, therefore, could be formulated as a complex function of $\Delta O$, $\Delta N$ and $\Delta C$. There are two possible ways of tiling: 1) dynamic tiling and 2) static tiling. In dynamic tiling, the data fetch module can keep fetching additional input feature maps as required for computing every new
output feature map till the on-chip memory is full, thus each tile can have different value of ∆O. Note that to enable this, ∆N and ∆C need to be known prior to the execution and, therefore, a joint optimization of all tiling parameters could not be performed. A solution to this would be to process the metadata before the DNN execution extracting out region information \((f_1, f_{MO})\) for every region and empirically choose the optimal tiling candidates by iterating over all possible values of ∆C and ∆N pairs. This would explore the dataflow exploration space and require multiple passes of metadata processing significantly degrading latency in real-time scenarios. Thus, we propose to decouple extraction of region information in the form of sparsity attributes and then perform dataflow exploration using these attributes via an analytical framework. We compute sparsity attributes, \(SA_I\) and \(SA_{MO}\), as function of ∆O over all regions (Eqn. 4). Note that \(SA_{MO}\) represents Average number of voxels in Receptive Field (ARF) for a given region, while \(SA_I\) takes the form of \((1 + β)\) where β reflects the fraction of voxels at region boundary.

\[
\begin{align*}
SA_I(I^\Delta_O, ∆O) &= \left(f_I(I^\Delta_O, ∆O) \right) / ∆O \\
SA_{MO}(I^\Delta_O, ∆O) &= \left(f_{MO}(I^\Delta_O, ∆O) \right) / ∆O \\
\end{align*}
\]

(3)

We adopt static tiling with two methods: 1) Strict Static Tiling (SST) and 2) Relaxed Static Tiling(RST). In SST, \(SA_I\) and \(SA_{MO}\) with the highest value across all regions are picked for each ∆O to ensure worst-case tile size allocation while under-utilizing the on-chip memory for quite a few tiles. In RST, to improve memory utilization, we use \(n\)th quantile of \(SA_I\) and \(SA_{MO}\) such that majority of the tiles fits within on-chip memory. The tiles overshooting the on-chip memory are split into two (or a next power of two) such that each sub-tile fits well into the on-chip memory. To calculate data transfers and operations, we use \(SA_{Avg}^I\) and \(SA_{Avg}^{MO}\) (Eqn. 4) averaging the sparsity attributes over all the regions \((I^\Delta_O)\) for each ∆O.

\[
\begin{align*}
SA_{Avg}^I(∆O) &= \left(∑_{R^\Delta_O}SA_I(R^\Delta_O, ∆O) \right) / |I^\Delta_O|, \\
SA_{Avg}^{MO}(∆O) &= \left(∑_{R^\Delta_O}SA_{MO}(R^\Delta_O, ∆O) \right) / |I^\Delta_O| \\
\end{align*}
\]

(4)

Similar to dense DNN, we choose between three types of walk-patterns (\(WP\)) 1) Input Stationary (\(IS\) 2) Output Stationary (\(OS\)) and 3) Weight Stationary (\(WS\)). Note that Eqns. 2, 3, and 4 could also be expressed as functions of \(I\) computing for ∆O and ∆M with CORF metadata structure and ARF representing as Average Response Field. Using the analytical framework (as shown in Figure 10), SPade explores the entire dataflow design space to arrive upon the best tile size, walk pattern and metadata structure (\(MD\)) for each layer in the network given an input pointcloud. SPade’s Analytical framework minimizes data accesses \(DA\) (Eqn. 5) between the on-chip memory and the off-chip memory over the entire dataflow design space \(D = \{(T, WP, MD)\}

\[
\begin{align*}
DA(D) &= F_{WS}(WP, [O/∆O]).(C.N.K) \\
&+ F_{IS}(WP, [N/∆N]).(SA_{Avg}^I(∆O).O.C) \\
&+ F_{OS}(WP, [C/∆C]).(O.N + SA_{Avg}^{MO}(∆O).O) \\
\end{align*}
\]

(5)

where, \(F_X(Y, Z) = 1 \iff (Y = X), \text{else } Z\)

D. 3D-Sparse-NN-Core Micro-architecture: SSpNNA

Section III-E described the distinctive requisites of a custom accelerator for 3D spatial sparsity, especially contrasted with prior sparse accelerators. We describe in this section, the microarchitecture of the SSpNNA (Spatially SParse Neural Network Accelerator) core which lies at the heart of our AccSS3D solution. The primary requisite for the hardware accelerator (HWA) is to process a tile (Figure 9), convert from sparse to dense representation by restructuring the tile data in the Front-end and perform dense compute in the Back-end.

Top-level Overview: The SSpNNA HWA is comprised of two major blocks (a) WAVES Front-end- Weight plane based Active Voxel Execution Scheduler (b) SyMAC Back-end- Systolic and Multicast based MAC Computation in Figure 11 Metadata (MT) is partitioned into header and feature data, where header stores COIR bit-masks and feature data stores the feature indices and its data. HWA also has a memory arbiter, a configuration and a control block. The Global event controller initiates execution after loading the L1 and configuring the HWA. Upon start, the WAVES scheduler formats the metadata and then triggers SyMAC for channel-wise computation and output element accumulation, during which, WAVES starts working on formatting the next set of data.

The WAVES Front-end rearranges the spatially distributed voxels along weight plane (Figure 11-a). Its subblock MT HDR Processor fetches weight mask and corresponding IFM and OFM indices. By using smart-lookups, it finds weight index for 4 active neighbor voxels per cycle. The HDR Format block forms tuples by grouping 4 features per weight plane, using 27 blocks to manage all weight planes together. Link-List based buffer is used to provide dynamic memory space allocation for weight planes, enabling more storage for weights with more active voxels. This design choice was motivated by the observation that fixed allocation of resources per weight plane leads to significant under-utilization, since it depends on ARF. By allocating 1 FIFO per weight plane for tuple storage, higher occupancy for all the FIFOs cannot be achieved. This under-utilization can be visualized as a wavy line touching the top element in each FIFO. The Link-List design helps increase the utilization by dynamic allocation of more resources to planes with higher number of active neighboring voxels, allowing us to accommodate 1.5X-2X more metadata lines in the same size of memory internal to the SSpNNA.

The SyMAC Back-end increases the data reuse within the HWA by connecting multiple compute blocks systolically, multicasting the input features to a set of PEs and accumulating data within the PEs as per channel length. Figure 11(b) shows three options for systolic groups as \(A, B, C\), which can be dynamically selected for weight plane grouping in the WAVES. Figure 11(b) ACC OFM block has local buffering with cache lookup capability which helps in reducing memory transactions for elements with cache hit. Figure 11(c) shows a DeNN block where input features are buffered and reused for all output channels, by convolving with different weights. PEs are implemented using tree structure where they can
perform dot-product on IEEE754 Full Floating-Point numbers and accumulate locally along the input channels.

4-DeNN configuration with 4 PEs per DeNN computes 4 elements per PE per cycle allowing SSpNNA to support 64-MUL operations per cycle. Changing SSpNNA configuration to 8 DeNNs, working in two systolic groups of 4-DeNN each, doubles performance to 128 MUL operations per cycle, but does not require any more memory ports for weights. **Through conscious design choices we reduce bandwidth requirement by 68%**: a) Local input buffer sharing and Systolic weight connection reduce bandwidth requirement by 37% and 25% respectively, b) local accumulation within PEs for connection reduce bandwidth requirement by 68%.

E. Adjacency Map accelerator Micro-Architecture - AdMAC

Section [V-B] described the requirements for reordering pointcloud and Section [IV-C] Figure [9] described metadata structure for tiling. We describe in this section, the Micro-Architecture of AdMAC-Adjacency map and Metadata Accelerator core in Figure [12] Input voxels (x,y,z) are fetched serially by block A in Figure [12]. Block B creates lookup table for all the active voxels. For faster lookup, AdMAC maintains hierarchical lookup table, at level one it encodes active voxels at higher granularity (called voxel 3D groups) and at second level it stores active information and corresponding memory address per voxel. Voxel information is stored in an 8-banked memory where bankID is encoded using \( y[z2], z[1:0] \). Within the bank, voxels are hashed so that each memory read of 64 Bytes can provide information for 16 voxels as per \( y[1:0], x[1:0] \) addressing. **This specific hashing helps in reading 26 neighboring voxels in a single cycle**, with the exception of boundary voxels. Block C creates Adjacency List for the voxels in the memory using the Sparse hash from B. Blocks C\( ①, ②, ③ \) compute address of neighbors, reads voxel information and write to memory after packing data as per metadata structure.

V. Scale-up Architecture for 3D Spatial Sparsity

In this section, we present Accelerator for Spatially Sparse 3D DNNs, an architecture (Figure [13]) targeting 3D spatially sparse DNN applications.

A. Overall Architecture

1) On-die memory architecture: Multi-level memory hierarchies have been widely adopted as they allow high bandwidth short-distance reuse at smaller inner level memories with lower latencies, while longer-distance reuse are captured at higher capacity by outer memory levels. The two levels of memories in the AccSS3D architecture are managed as scratchpads by the software to orchestrate the 3D sparse-CNN execution following the optimal directives of the SPADE. A scratchpad-based architecture with multiple levels of memory, requires compute and data-transfer needs to be effectively synchronized to maximize compute and bandwidth utilization. As a result of the locality-aware tile-based execution as described in section [V-C] there is significantly higher space sensitivity at L1 compared to L2. This is because when processing similar number of voxels, the unique-OFM to unique-IFM ratio is typically highly skewed (away from 1) for L1 when compared to L2. This results in higher sensitivity for reuse opportunity to memory size at L1 as compared to L2. This precludes double-buffering at L1. Hence, we choose distinct compute and data-exchange phases as in [22]. All data transfers from between the shared-L2 and a SSpNNA core’s L1 are blocked when the core is active, and the SSpNNA core is idled when data is being exchanged between its L1 and the shared L2.

2) Scaled-up multi-sparse-NN Core architecture: To compensate for the increased latency due to sequential phases, we adopt an overlapped tile execution model across the multiple SSpNNA cores in our scaled-up architecture (Figure [14] a). Using a shared bus at the L1-L2 interface, tile data is transferred between the shared-L2 and a SSpNNA core’s L1 memory while other cores are in their compute phases and this continues in round-robin mode as each core enters its data exchange phase.
3) Data transfers between L1, L2 and DRAM: We employ a DMA-based architecture to accomplish data transfers in the data-exchange phases. DMAs are triggered through a global hardware-based event controller, with the software specifying data-movement details such as source/destination addresses and number of bytes through the DMA engines tables. We provision two DMA engines: one each for the L1-L2 and L2-DRAM interfaces respectively. Based on the selected metadata structure (CORF or CIRF) - either one of the datatypes between IFM and OFM is accessed in order, while the other can be un-ordered (see Figure 9). We use block transfers programmed as a single DMA table entry for the entire tile for the datatype with ordered accesses. For the other datatype, we use DMA table entries per voxel level. Since weights are programmed as a single DMA table entry for the entire tile can be un-ordered (see Figure 9). We use block transfers interface lower than a maximum threshold value \( (DA_{th}) \) without being bandwidth constrained. For this, CAROM first identifies a set of dataflow candidates \( D^{L_q} \), such that: 

\[
D^{L_q} = \{ D_i : DA^{L_q}_{D_i} \leq DA_{th} \} \cup \{ \text{argmax}_{D_i} (DA^{L_q}_{D_i}) \}
\]

where, \( DA_{th} \) is computed based on number of operations to be performed on the working set at \( L_q+1 \), total compute \( (Ops/sec) \) available to an instance of memory level \( L_q \) and bandwidth at \( L_q \leftrightarrow L_{q+1} \) interface: 

\[
DA^{L_q}_{D_i} = \frac{\text{Ops}^{L_q} \times BW^{L_q}}{\text{Total Comp}^{L_q}}
\]

where, \( \text{Ops}^{L_q} = \text{SA}^{L_q}_{MO}(C^{L_q}), O^{L_q}, N^{L_q}, C^{L_q} \)

CAROM then selects the optimal dataflow over the set \( D^{L_q} \), maximizing reuse opportunity \( (RO^{L_q-1}) \) for \( L_q \) memory level: 

\[
D^{L_q}_{opt} = \text{argmax}_{D_i \in D^{L_q}} (RO^{L_q-1})
\]

Since for a given working set, reuse opportunity is proportional to the total number of operations to be performed on the working set, \( \text{Ops}^{L_q-1} \) is used for reuse opportunity maximization. The optimal tile candidate at a memory level \( L_q \) acts as the working set for level \( L_q-1 \). And, therefore, CAROM continues to pick optimal dataflow(s) from outer levels to inner levels except the innermost level as per the above criterion. For the innermost memory level, it selects the optimal dataflow by minimizing data accesses \( \text{argmin}_{D_i \in D^{L_q}} (DA_{D_i}) \).

To improve data locality across all the memory levels through pointcloud reordering, SOAR (Section IV-B) is extended to perform hierarchical pointcloud ordering starting from innermost to outermost levels. Given optimal tiling from SPADE, SOAR groups the entire pointcloud in chunks and finds optimal ordering of points in each chunk based on tiling parameters for the innermost memory. Reinterpreting each chunk as a point, SOAR is reapplied to recursively group these chunks into super-chunks with optimal ordering based on tile parameters of the outer memory level, till the outermost level.

C. Minimizing SPADE latency overhead

As described in sections IV-C and V-B, SPADE requires pre-processing of input pointcloud data to extract sparsity attributes \( (SA's) \) to perform dataflow exploration. Extraction of \( SA's \) could add significant overhead to end-to-end latency. To minimize this, we explore: 1) if the sparsity attributes could be categorized into two sets: a) common attributes which are consistent across pointclouds - referred to as Meta Sparsity Attributes (MSA), b) Input Specific Attributes (ISA) which
varies highly across pointclouds; and, 2) whether by using $M_{SA}$, optimal dataflow candidates can be pre-computed for selected binned values of $I_{SA}$. Thus, we correlate $SA_{Avg}$ over randomly picked pointclouds (Figure 15) and observe that:

1. $SA_{Avg}(\Delta O)$ exhibits high variance across various values of $\Delta O$, but follows similar pattern across pointclouds. Also, $SA_{Avg}(v)$ shows a high correlation with $m$-dimensional cube with volume $v$ and faces $\alpha_m$.

2. $SA_{Avg}(\Delta O)$ which represents the ARF, remains constant with $\Delta O$ for a pointcloud, but varies across pointclouds.

Based on above observations, we propose an offline version of SPADE to use $SA_{Avg}$ as the meta sparsity attribute and ARF as $I_{SA}$. The $M_{SA}$ is computed over a representative set of pointclouds $P$ using Eq. 10. We generate tables of optimal dataflow candidates with ARF as table index, for all network layers. For tile allocation, we use 90-quantile of $SA_{Avg}(\Delta O)$ along with RST as described in [V-C]. Note that the proposed semi-offline mode of dataflow exploration strikes a conscious balance between DNN execution performance and runtime latency overhead of sparse dataflow selection.

$$M_{SA_{Avg}}(\Delta O) = \left(\sum_{P \in P} SA_{Avg}(\Delta O)\right) / |P| \quad (10)$$

To minimize latency overhead, SPADE is deployed as two components (Figure 16): 1) offline-Spade - to generate a table of optimal dataflows for multiple selected ARF values, and 2) on-the-fly SPADE (OTF-Spade) - to reorder a given input pointcloud and select optimal dataflow for the input. Though $Adjacency Map$ and COIR metadata contain a similar data structure, due to tiling and reordering, entries in $Adjacency Map$ are re-grouped to create tiled metadata ($\Delta M$) based on tiling parameters of innermost memory level. To transfer data between memory levels, required DMA tables (as mentioned in section V-A3) are generated prior to DNN execution. To further hide the latency for OTF-Spade, DNN execution is kicked-off just after the OTF-Spade completes processing for the first layer. Since OTF-Spade processing for the rest of the layers does not depend on DNN execution of previous layers, both the threads, OTF-Spade and DNN execution, proceed independently without further need for synchronization.

VI. EVALUATION

A. Setup, Methodology and Workloads

We evaluate AccSS3D using a whole chip performance and energy model. We design, synthesize Sspnna core with

64KB L1 memory using Synopsys DC [1] at 1GHz clock, perform Place and route using Synopsys IC Compiler II [2]. L2 memory of 2×1MB is constructed hierarchically, using sub-arrays of size 16KB each, with 4 banks per instance, 4 sub-banks per bank and 4 sub-arrays per sub-bank. Power consumption for compute and on-chip buffers is estimated using Synopsys PrimeTimePX from SystemVerilog (SV) simulation. Interconnect energy is computed using estimated wire lengths and added to L1 and L2 access energy estimates. Area and energy cost for AdMAC is estimated using micro-architecture accurate model and counting data access events. DRAM power is taken from Micron power calculator [37] for DDR4-2660.

**Performance:** To measure AccSS3D performance, we obtain execution cycles for Sspnna core for each tile processing in every network layer through SystemVerilog simulation. For end-to-end latency estimation, we simulate multi-core asynchronous execution model through a detailed analytical framework feeding per tile execution time from the SV simulation and including processing time for OTF-Spade (Section V-C). CPU (Intel-i7-8700K @3.7 GHz) performance is measured through VTune [3] and power is estimated using PSST tool [38]. GPU (Nvidia GeForce-GTX-1080 @ 1.6GHz) performance is obtained form visual profiler [40] and power is reported from nvidia-smi. We denote single core CPU, 4-core CPU and GPU software baseline performance as 1-CPU, 4-CPU and GPU.

**Workloads and Datasets:** We evaluate AccSS3D on three applications of 3D visual analytics: 1) 3D semantic segmentation 2) 3D object detection 3) 3D scene completion picking three state-of-the-art workloads 1) SCN [18], 2) PV-RCNN [46] and 3) SGN [12] one from each application. We choose 3D pointclouds from ScanNet [11] and Waymo Open Dataset [48] (Table 2 rows 5 and 6) for indoor and outdoor scenarios.

B. Scaled-up Configuration for AccSS3D

We describe a 1024 MACs based AccSS3D architecture that achieves a 50x execution-time speed-up at an operating frequency of 1 GHz compared to 1-CPU. Given the prohibitively large architecture configuration space, we adopt a hierarchical framework to arrive at the most optimal configuration. Firstly, the optimal L2 memory size is selected such that
total DRAM accesses do not exceed $1.5 \times$ of the total data footprint accumulated across layers while avoiding bandwidth bottlenecks at DRAM interface for a given DRAM bandwidth. A joint optimization is then performed to optimize L1 memory size, L1+L2 bandwidth and number of the SSpNNA cores. Figure 17 shows performance sensitivity to these parameters for a chosen pair of L2 memory size and DRAM bandwidth. Performance scales with cores up to a certain number owing to a reduction in idle time during data-transfer phase. With further increase in cores, data replication for shared datatype dominates, degrading the performance. At higher L1+L2 bandwidth and larger L1 size, data-transfer time reduces significantly favoring lower core count configuration. Similarly, we obtain the optimal architecture configuration for each DRAM bandwidth point (Figure 15) and select the optimal bandwidth that maximizes performance. Since the L2 is dual-buffered, we provision for 2x the required size. Figure 20 Right lists the optimized architecture parameters.

### C. Power, Performance and Area Analysis

As described in Section IV-D, the SSpNNA core can be scaled with the number of internal DeNN instances. The design parameters, area breakup for the major blocks on a typical 16nm process and the local buffering details in the SSpNNA core for both configurations are shown in Figure 20. With dual 8KB of local buffer we were able to hide the execution latency of WAVES MT formatting. Figure 20 also shows the physical placement for the SSpNNA core where we achieved a high utilization 72.6% by placing the logic blocks as dictated by the internal dataflow. The energy consumption of the SSpNNA compute core and other local storage contributes to $\sim 50\%$ of total energy and remaining 50% is attributed to SRAM accesses. 70% of the logic power is consumed by the clock network whereas sequential and combinational cells consume 5% and 25% respectively. For AdMAC, energy is dominated by DRAM reads. Local buffer access and logic energy contributes to only 2% of total energy.

Figure 19 shows layer-wise speed-up and power reduction for the 3D sparse convolution operation in the SCN network with ScanNet. Speedup for initial and last few layers reaches up to $80x$ over 1-CPU. As SPADE adopts spatial sparsity aware tiled execution, data accesses are reduced significantly. With tiled metadata, ordered data transfers through DMAs and asynchronous execution model, data transfer latencies are overlapped with the accelerator’s compute, as compared to CPU execution where Input Gather and Output Write incur high sequential latency. In the middle layers, reuse opportunity is significantly higher, therefore the impact of dataflow optimization is low, yet speedups close to 20x are achieved over 1-CPU. AccSS3D achieves a power reduction by $56.8x$ and $132.9x$ on average across all layers compared to 1-CPU and 4-CPU respectively. Since middle layers are convolution heavy, CPU achieves higher instructions-per-cycle resulting in higher power consumption. Therefore, power reduction with AccSS3D is relatively higher for the middle layers.

Table IV summarises speed-up and energy reduction for both 3D sparse convolution operation and end-to-end scene segmentation over CPU baselines for SCN on ScanNet. Figure 21 shows power and performance for two additional workloads (PV-RCNN, SGNN) and including Waymo’s outdoor dataset, where AccSS3D is compared with 1-CPU, 4-CPU and GPU. For PV-RCNN and SGNN networks, acceleration for Adjacency Map creation provides significant speed-up and energy savings as size of pointcloud is relatively higher than number of channels ($N,C$) in these network topologies.

### D. AccSS3D Feature Analysis

We evaluate the goodness of AccSS3D features as described in Sections IV and V (Figure 22). We collect performance metrics for each feature by disabling it from the fully-featured AccSS3D. As reference software implements a weight-stationary dataflow with no spatial tiling, it was infeasible to implement for few layers due to large weight size and also likely to be unoptimized for a system with limited memory such as the proposed AccSS3D. Hence, we picked input-stationary dataflow as a reasonable baseline which performs tiling on available on-chip memory, equally distributing tiles along output channels ($N$) onto many-cores and supporting on-chip partial accumulation minimizing DRAM accesses. **Optimal tiling and walk-pattern selected by SPADE** provides significant reduction in both on-chip and DRAM data accesses compared to baseline dataflow. A data-accseses minimization at L2 results in lower DRAM accesses, but it increases on-chip data transfers and hence performance drops significantly due to on-chip bandwidth bottlenecks. **CAROM** helps alleviating this issue by striking a balance between the DRAM and the on-chip data-transfers without being bandwidth limited at DRAM interface. Comparing with input pointcloud dependent

### TABLE IV

**SPEED-UP & ENERGY SAVINGS WITH ACCSS3D ON SCN/SCANNET**

| DNN Only | End-to-end |
|----------|------------|
|          | 1-CPU  | 4-CPU  | 1-CPU  | 4-CPU  |
| Speed-up | 36.6x  | 16.8x  | 23.7x  | 11.8x  |
| Energy Savings | 2079.0x | 2232.0x | 23.2x  | 24.8x  |
Fig. 19. Layer-wise Power Reduction and Performance for SCN/ScanNet with AccSS3D for 3D sparse convolution over 1-CPU and 4-CPU [18] (setting OpenMP threads to 1 and 4). Hyper-threading was disabled during measurement. Idle power was subtracted from total power to get workload power.

Fig. 20. Left: Physical placement and area utilization of SSpNNA, Right-Top: 16nm SSpNNA Design parameters, Right-Bottom: Architecture Parameters.

Fig. 21. Power, Performance and Energy Savings (including DRAM) across workloads and datasets with AccSS3D over CPU and GPU baselines.

SA based dataflow (3SA), AccSS3D with MSA marginally loses performance for a few pointclouds while it provides significant reduction in end-to-end latency through offline-dataflow. Gains with SOAR based pointcloud reordering varies across pointclouds as scope for the reordering depends on input geometry and scan order performed during the data acquisition. Figure 23 shows relative data-access savings with SOAR comparing with three different scan-orders along x, y and z direction.

E. CPU Performance with SPADE

To evaluate the performance impact of SPADE on a CPU only system, we implement tiling and loop order in the reference SCN-CPU baseline [18]. Performing the 3D sparse convolution as per COIR metadata structure requires irregular data accesses interleaved with compute. Without explicitly ensuring data residency in inner level caches, processing performance will be limited by latency. For efficient processing, irregular data accesses need to be separated from the convolution. To achieve this, similar to the reference CPU baseline, we gather input and weights into local buffers and after convolution we perform scattered write for output features. Since footprint for most of layers exceeds the capacity of the CPU’s last-level-cache (LLC) and given the high latency to DRAM memory, we optimize for DRAM accesses. The dataflow optimizer assumes 10% of LLC’s capacity to be used for code and miscellaneous data and remaining 90% would be be available for the SCN’s working set. Figure 24 shows the CPU performance with the optimized tiling and loop order as recommended by SPADE. For brevity, we show one layer from each spatial resolution. With SPADE, overall performance improves by 18%. For some layers gain performance upto 74%, while for a few layers it drops by 21%. These layers have smaller metadata (due to lower resolution) and more channels (C, N), hence SPADE prefers tiling across channels requiring metadata to be accessed and processed repeatedly. We observe that high CPU overheads of metadata processing and explicit scatter-gather operation are reasons for lower performance.

VII. RELATED WORK

Taichi [23] offers a high level interface to efficient data structures for spatially sparse data by using index analysis. Eyeriss [7] proposed row-stationary dataflow with diagonal data-feedingover 2D systolic array demonstrating substantial energy savings, while Eyeriss-V2 [8] extended it to a scale-up architecture through mesh connections. [55] utilizes a tiling structure through unrolling nested loops of convolution to maximize reuse at different levels of caches. FlexFlow [55] aims to maximize compute utilization by minimizing wastage due to spatial split of work among PEs. Morph [21]
optimizes dataflows for a 3-level memory scale-up architecture maximizing reuse at each level in the hierarchy. ExTensor [22] proposes technique to find non-zero element intersection for effective computation. Spartan [17] defines SparseMap, which is two tuple of bitmask and performs efficient inner join logic to feed MAC. SMAASH [29] compresses sparse matrix in software and performs efficient index finding by hardware accelerator on compressed data. [24] proposes fine grained channel gating technique and an accelerator to exploit the dynamic sparsity. [63] proposes an accelerator with Indexing Module to efficiently select and transfer needed neurons to PEs.

VIII. CONCLUSION

Understanding of 3D objects and environment is critical for many real world applications. To our best of knowledge, this is the first end-to-end solution for accelerating 3D scene analysis by exploiting spatial sparsity through sparsity-aware dataflow optimizer, novel micro-architecture and design for a spatially-sparse compute engine and, employing custom software-hardware co-designed methodologies.

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