Reduce Wafer Remnants Through Pre-Assembly Process Optimization

P. Vijayakumaran1, M. H. M. Ramli1, M. Selvam1, K. Hamid1, A. Atiqah2, A. Jalar2, 3, M. A. Bakar2

1Nexperia Malaysia Sdn. Bhd, PT No. 12687, Tuanku Jaafar Industrial Park, 71450 Seremban, Negeri Sembilan, Malaysia
2Institute of Microengineering and Nanoelectronics, Universiti Kebangsaan Malaysia, 43600 UKM Bangi, Selangor, Malaysia
3Department of Applied Physics, Faculty of Science and Technology, Universiti Kebangsaan Malaysia, 43600 UKM Bangi, Selangor, Malaysia

Abstract. Wafer fabrication technology has been seeing exponential growth in recent years. This development is driven by the demand for better reliability, superior performance, and lower cost of electronic consumer products. Generally, the standard soft-soldering wafer backside metallization multilayer stack is AuAs/Ag/Ni/Ag. The present backside metallization being developed is Ti/NiV/Ag as the cost of Ti is almost negligible compared to Au. However, this new wafer backside metallization leads to increased remnants remaining on the dicing tape after die pickup. The reduced effective area of the die backside surface may cause adhesion issues in the subsequent die attach process. In realizing this essential phase, in pre-assembly process optimization has been carried out using some assessment on the process flow and data analysis through statistical analyses image and measurement of wafer skeleton remnants was taken showing a reduction from 70μm to 40μm in width. This method shows that skipping the baking process in the pre-assembly process will undoubtedly lessen the adhesion with the back metal with mounting tape. Without compromising the saw quality will indeed give a reduced wafer remnant. Henceforth, skipping baking in the pre-assembly process will significantly reduce wafer remnants and further improve die attach process.

1 Introduction

The wafer technology process is more economical for the manufacturer thus, it is cost saving and with this wafer technology, a wide range of customer requests can be met. The standard metal backside deposition is included of Au (gold), As (Arsenic), Ag (Silver), Ni (Nickel), Ag (Silver) [1]. The new back metallization consists of Ti (titanium), Ni (Nickel), V (Vanadium) Ag (Silver), the wafer is developed as the cost of Ti is almost negligible compared to Au. In order to reduce the wafer cost of the AuAs/Ag/Ni/Ag, the wafer backside metallization can be changed to Ti/NiV/Ag [2–4].

Currently, the wafers containing Au are receiving a cost uplift of 7 € for the Au. An estimated production load of approximately 13000 wafers per year would lead to savings of 91k€ per year only by considering the Au uplift [5]. There are further reasons to select Ti/NiV/Ag instead of AuAs/Ag/Ni/Ag metallization. The Cu interconnects with no risks as Cu from leadframe/solder diffuses into Au interface layer and becomes high ohmic. The present backside metallization being developed is Ti/NiV/Ag as the cost of Ti is almost negligible compared to Au. However, this new wafer backside metallization leads to increased amounts of remnants remaining on the dicing tape after die pickup. The wafer remnants are the rough surface or residual damage left on the wafer that comes from backside metallization process. This wafer remnants may reduce effective area of the die backside surface may cause adhesion issues in the subsequent die attach process [6,7].

Previous works on characterization of wafer remnants by using real time X-ray diffraction found that the method enable to detect element existed on the wafer [8]. In this method, the location and the size of wafer remnants cannot be detected precisely. In this study, the wafer remnants can be easily obtained by using optical microscopy. Moreover, in order to avoid the wafer remnants on the backside, there is another method by skip Ag placement on leadframe in assembly. This method could possibly reduce the manufacturing cost is in term of processing time which

1Corresponding author: a.atiqah@ukm.edu.my
reduce the manufacturing process mainly in pre-assembly process. Though, the implementation of this new wafer backside metallization TiNiVAg having increased amounts of wafer remnants remaining on the dicing tape after die pickup has been observed which wasn’t observed in AuAs/Ag/Ni/Ag wafer backside metallization. This could be investigated by optimization processing of variable parameter such as single cut no bake, single cut bake, step cut no bake and step cut bake process. The characterization through optical microscopy to determine the wafer remnants.

2 Methodology

When new wafer products arrive at the backend operation process pre-assembly optimization. Some necessary actions should be taken into consideration to ensure manufacturability and quality is within the expectation level. Initially, some trial took place to see the output response by validating existing process flow and sawing parameter. In Fig. 1 of the wafer skeleton shows comparison of wafer skeleton AuAs/Ag/Ni/Ag and TiNiVAg wafer back metallization. It was noticed that all output response is within the requirement. Only wafer remnants were visible in wafer backside metallization TiNiVAg compared to the AuAs/Ag/Ni/Ag wafer backside metallization had zero.

The wire bonded and molded sample was used for nitrogen-free chemical deflash to ensure the chemical was fulfilled the zero delamination requirements. Table 1 shows the detailed inspection items required to ensure the new chemical fulfilled the assembly requirement. The indication criteria used is the mold bleed occurrence on leadframe surface after the chemical deflashing process.

![Fig. 1. Comparison of (a) wafer skeleton AuAs/Ag/Ni/Ag and (b) TiNiVAg wafer back metallization.](image)

To further validate on this remnant and to have an assembly process optimization design of experiment consists of 4 runs as shown in the Table 1. There were only two (2) methods were involved for clip bond wafer was sawn to ensure before and the output from others process were within the standard specification. Table 1 shows the design of experiment trail run for wafer remnants were consisted of four (4) variables process such as single cut no bake, single cut bake, step cut no bake and step cut bake process.

| Trial’s Variables | Wafer location | Response |
|-------------------|---------------|----------|
| Saw cutting method | Bake process  |          |
| A1                | Single        | No       | #3, #4   |
| A2                | Single        | Yes      | #7, #8   | Wafer remnant skeleton |
| A3                | Step          | No       | #10, #11 |
| A4                | Step          | Yes      | #15, #16 |
3. Characterization

Each of the wafer data was collected as shown in Fig. 2 showed that point each trial had a total reading of 30. The characterization was carried out by using Olympus Industrial Microscopes STM7As to determine the remnants existence on the wafer.

![Image of wafer data collection points](image)

**Fig. 2.** Data collection point on the wafer skeleton for remnants.

4 Results and Discussion

The comparison of the variable process such as A1-single cut no bake, A2-single cut bake, A3-step cut no bake and A4-step cut bake in boxplot form as shown in Fig. 3.

![Boxplot of wafer remnants](image)

**Fig. 3.** Boxplot of wafer remnants.

The larger size of wafer remnant’s is A4-step cut no bake, followed by A3-step cut no bake, A2-single cut bake and A1-single cut no bake with the approximately size of 40 - 50 μm, 30 – 40 μm, 25 - 35 μm and 16-28 μm. The wafer baking is required to increase the adhesion of the wafer and tape so that during sawing and cleaning process, all these diced units will remain intact, and no flying die will be observed. However, this TiNiVAg wafer back metallization wafer shows that the dull back finishing without baking showed no flying die was observed for all the skipped baking process. The remnant’s result shows that all these wafers are lessening to a level as the boxplot of the wafer remnants below shows the comparison of the variables as shown in Fig. 3.

Fig. 4 (a) – (b) show the wafer remnants for each process consisted of A1-single cut no bake, A2-single cut bake, A3-step cut no bake and A4-step cut bake The actual image of the remnants for each trail as depicted in Fig. 4 is the quantity and size should be less than 40 μm is acceptable. In this study A1-single cut no bake and A3-step cut no bake with skipping bake process showed less than 40 μm, while the process includes baking process A2-single cut no bake similar have the wafer remnant’s size less than 40 μm. When the larger size of wafer remnants existed on the wafer in Fig. 4, this will give difficulty in die picking process. In order to overcome this phenomenon, the optimization of the process should be carried out as in Fig. 3. Even though those trials exhibited the wafer remnants, the important is each process give different additional cost and time saving.
Fig. 4. Process flow of backside metallization TiNiVAg (a) A1-single cut no bake, (b) single cut bake, (c) step cut no bake and (d) A4-step cut bake.

Fig. 5. Process flow of backside metallization TiNiVAg.

As shown in Fig. 5 the process flow of backside metallization TiNiVAg the step for baking were removed. Furthermore, the A1-single cut parameter with no baking showing an overall good outcome on remnants and all other output responses well within the specification. The sawing time for a single cut and no-bake is approximately 20 minutes compare to a step cut with a bake which takes approximately 90 minutes. On the other hand, skip baking process will provide additional cost and time saving to operation compared to the existing AuAs/Ag/Ni/Ag backside metallization that required baking.

5. Conclusion

Based on the outcome of the process optimization, it is observed that skipping the baking process in the pre-assembly process flow lead a reduction the wafer remnants. This method may give a significant improvement for pre-assembly process. However, future works to further reduce or eliminate the wafer remnants is currently undergoing by attempting in a new blade and UV tape, at the same time some wafer-level research to further strengthen the adhesion of TiNiVAg to the substrate in wafer fabrication level.
The author would like to acknowledge and convey his deepest gratitude to Dr. Henry Greve & Dr. Ruediger Weber from Wafer Fabrication Nexperia Germany GmbH, Nexperia team member, for their support and encouragement like to extend appreciation to Universiti Kebangsaan Malaysia under GGPM-2020-036 for publishing this paper.

References

1. J. J. Licari, D. W. Swanson, "Adhesives technology for electronic applications: materials, processing, reliability (William Andrew)." (2011)
2. A. Hooper, J. Ehorn, M. Brand, C. Bassett, "Review of wafer dicing techniques for via-middle process 3D/TSV ultrathin silicon device wafers 2015 IEEE 65th Electronic Components and Technology Conference (ECTC)," (IEEE), 1436–46 (2015)
3. B. Kim, C. Sharbono, T. Ritzdorf, D. Schmauch, Trans., 2, 269 (2007)
4. M. Calabretta, A. Sitta, S. M. Oliveri, G. Sequenzia, Int. J. Interact. Des. Manuf., 15, 117–9 (2021)
5. Anon News | Waferworld.com
6. R. P. Donovan, "National technology roadmap for semiconductors: basis and alignment Contamination-Free Manufacturing for Semiconductors and Other Precision Products," (CRC Press), 19–38 (2018)
7. W. M. M. B. W. Suleiman, N. Krishnan, "High voltage isolation silicon node wafer saw 2015 IEEE 37th International Electronics Manufacturing Technology (IEMT) & 18th Electronics Materials and Packaging (EMAP)" Conference (IEEE), 1–6 (2016)
8. A. N. Danilewský, J. Wittge, A. Hess, A. Cröll, A. Rack, D. Allen, P. McNally, T. dos Santos Rolo, P. Vagovič, T. Baumbach, Phys. status solidi, 288, 2499–504 (2011)