Circuit Analysis and Optimization of GAA Nanowire FET Towards Low Power and High Switching

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Abstract

The main aim of this work is to study the effect of symmetric and asymmetric spacer length variations towards source and drain on n-channel SOI JL vertically stacked (VS) nanowire (NW) FET at 10 nm gate length ($L_G$). Spacer length is proved to be one of the stringent metrics in deciding device performance along with width, height and aspect ratio (AR). The physical variants in this work are symmetric spacer length ($L_{SD}$), source side spacer length ($L_S$) and drain side spacer length ($L_D$). The simulation results give the highest $I_{ON}/I_{OFF}$ ratio with $L_D$ variation compared to $L_S$ and $L_{SD}$, whereas latter two variations have similar effect on $I_{ON}/I_{OFF}$ ratio. At 25 nm ($2.5 \times L_G$) of $L_D$, the device gives appreciable ON current with the highest $I_{ON}/I_{OFF}$ ratio ($2.19 \times 10^8$) with optimum subthreshold slope (SS) and ensures low power and high switching drivability. Moreover, it is noticed that among optimal values of $L_S$ and $L_D$, the device $I_{ON}/I_{OFF}$ ratio has an improvement of 22.69% as compared to other variations. Moreover, the effect of various spacer dielectrics on optimized device is also investigated. Finally, the CMOS inverter circuit analysis is performed on the optimized symmetric and asymmetric spacer lengths.

Keywords Junctionless · GAA nanowire FET · Spacer length · $I_{ON}/I_{OFF}$ · SS

1 Introduction

Increased growth in semiconductor market improved the transistor performance but with the various adverse SCEs. Various attempts to overcome the SCE problem have resulted in radical changes in transistor structural design. Many researchers predict that the vertically stacked nanowire (VS-NW) structure, is future option to drive electronic industry, which has good gate controllability and great packing density, will be the eventual destination of the shrinking transistor. The VS superior NW performance is due to its gate-all-around (GAA) based architecture. Recent research [1] has shown that VS-NWs are capable of balancing outstanding low OFF state and high ON-state properties. However, a very few of these studies have taken into account the VS-NW structure’s spacer optimization, which is an unavoidable for sub-10 nm nodes for better gate controllability [2–4]. Moreover, to increase device efficiency at sub-10 nm regime JL devices are formed. Simple manufacturing method, junction free nature, low thermal budgets, doping concentration gradient, improved scalability, and immunity to short channel effects (SCEs) are all advantages of JL based devices. [5–8].

Moreover, the JL devices exhibits better $I_{OFF}$ characteristics due to volume depletion nature. For volume depletion in JL FETs the need of channel thickness less than 10 nm is fundamental and advanced architectures like trigate, vertical super thin body (VSTB), double gate, Gate all Around (GAA) structure is essential [9, 10]. Moreover, higher gate work function is also required for full depletion [11, 12]. In a VSTB FET, carrier mobility improves for decreased body thickness since carrier transport is predominantly controlled by a single gate [13]. As a result, $I_{ON}$ improves. Furthermore, this novel device is significantly easier to make than SOI FETs [14]. Since JL device use volume conduction phenomena hence improves carrier transit speed and minimize surface roughness through scattering [15].

The NW FETs were proposed as a successor to FinFETs, with a GAA design and improved gate electrostatics. However, because to their limited cross-section area and width.
constraint, the NWFETs have weak driving. While a large number of nanowires may be employed to increase $I_D$, this also leads to higher parasitic capacitances.

To minimize SCEs for sub-20 nm device’s, the introduction of spacers is fundamental [4]. The addition of spacers, on the other hand, enhances series resistance and so minimizes drive current ($I_{ON}$) current performance. The flow of gate-source/drain carriers is restricted as the spacer length increases, even at high $V_{DS}$. High-$k$ spacers increase switching ratios ($I_{ON}/I_{OFF}$) by inducing field coupling via the fringing effect [16]. However, in order to achieve superior performance metrics, spacer length should be carefully chosen. Aside from thickness and width, spacer length is also carefully adjusted to improve transistor performance. According to research [14], the effect of drain asymmetry variation reduces leakages by 57%. The inclusion of spacer reduces leakages mostly due to edge tunneling of carriers. This paper explores symmetric and asymmetric spacer length variation on GAA NW FET at nano regime. Various performance metrics like $I_{ON}$, $I_{OFF}$, $I_{ON}/I_{OFF}$, and SS are analyzed.

The paper is organized as follows. The section 2 describes device physics and device geometrical parameters. In section 3.1 symmetrical dielectric variation of spacer length optimization is performed on SS and $I_{ON}/I_{OFF}$. In section 3.2 source spacer length is varied ($L_S$) by keeping drain spacer length ($L_D$) constant. In section 3.3 drain spacer length is varied ($L_D$) by keeping $L_S$ as constant. Section 4 illustrates the CMOS inverter performance of symmetric and asymmetric spacers.

### 2 Device Structure and Simulation Methodology

Figure 1 depicts the 3-D JL SOI nanowire FET and 2-D view of symmetric spacer. In this paper we have considered 3-D JL SOI VS NW FET to understand the effect of spacer length on device DC performance. The high-$k$ dielectric HfO$_2$ is used as a spacer material to increase switching performance. Although the use of spacer length improves subthreshold performance, but reduces $I_{ON}$. As a result, a spacer length with a high-$k$ dielectric is provided to compensate for this impact, increasing $I_{ON}$ by increasing electron flow from source to drain. Furthermore, introducing high-$k$ gate dielectric along with interfacial oxide (SiO$_2$) achieves a lower EOT and better gate electrostatics, the suppression of leakages, and the suppression of random threshold voltage changes [17, 18]. The $I_{OFF}$ is maintained $<100$ pA for all variations with a fixed work function of 4.8 eV. With Titanium (Ti) as the gate metal, continuous and uniform doping is maintained. The device parameters used for the simulation are listed in Table 1.

Due to higher channel doping concentrations Fermi Dirac statistics are activated. Since carrier degradation phenomena are produced by surface roughness, acoustic phonon scattering, and doping dependency mobility reduction, the Lombardi mobility model is taken into account. A band-to-band tunneling model is included to handle the band gap narrowing effect that can occur as a result of increased channel doping. To account for carrier production and recombination events, the Shockley-Read-Hall (SRH) model is used. To account for quantum correction effects, quantum models are used. The threshold voltage is extracted at $(W/L) \times 10^{-7}$ A at $V_{DS} = 0.9$ V and $V_{GS} = 1.2$ V. The simulation models have been thoroughly calibrated using experimental data [19]. The simulations are carried out through 3D Cogenda Visual TCAD simulator [20].

### 3 Result Analysis and Discussion

#### 3.1 Symmetric Variation of Spacer Length

Figure 2 depicts the ON and OFF parameters of the VS NW FET from the TCAD simulator. The VS NW FET demonstrates behavioral change with modification in spacer length, as shown in Fig. 2a and b, with both $I_{ON}$ and $I_{OFF}$ decreasing as spacer length increases. Longer spacers produce good subthreshold behavior but result in a decrease in $I_{ON}$ due to the increased series resistance. Due to downfall in edge tunneling from source to drain and gate overlap results in lowering of $I_{OFF}$ with more spacer distance i.e., higher $L_{SD}/L_G$ ratio.

From Fig. 3 it is observed that the symmetric spacer exhibits highest $I_{ON}/I_{OFF}$ of $2.65 \times 10^8$ and lower SS of 63 mV/dec at $L_{SD} = 1.5 \times L_G$. Moreover, the device exhibits diminished $I_{ON}/I_{OFF}$ at $L_{SD} = 2 \times L_G$ and thus removed from design of symmetric spacer perspective.

| Table 1 | Various device parameters used for simulation |
|---------|---------------------------------------------|
| Parameters | JL VS NW FET |
| Gate length ($L_G$) | 10 nm |
| Gate oxide thickness (SiO$_2$) | 0.5 nm |
| Gate oxide thickness (HfO$_2$) | 1.5 nm |
| Metal gate thickness | 5 nm |
| EOT (Equivalent oxide thickness) | 0.75 nm |
| Each channel thickness and height | 10 nm |
| Source/drain length | 20 nm |
| Length of source or drain extensions ($L_S/L_D/L_S$) | Varied |
| Work function | 4.8 eV |
| Source/channel/drain doping | $10^{19}$ cm$^{-3}$ |

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3.2 $L_S$ Variation with Fixed $L_D$

The length of the spacer dielectric is asymmetrically altered in this section. The source side spacer length is adjusted while the drain spacer length is kept constant at $1.5 \times L_G$, because the device achieves the maximum $I_{ON}/I_{OFF}$ ratio and mild SS at this symmetric spacer length. From the Fig. 4a and b increase in $L_S$ length the $I_{ON}$ decreases at fixed $L_D$ length of 15 nm. From the Fig. 5 the $I_{ON}/I_{OFF}$ ratio increases with raise in $L_S/L_G$ value and reaches to highest value at $1.5 \times L_G$.

Figure 5 depicts the asymmetric spacer variation of $L_S$ in ON state. The device exhibits highest $I_{ON}/I_{OFF}$ ratio at $S_G = 1.5 \times L_G$. The $I_{ON}/I_{OFF}$ of $2.6 \times 10^8$ is obtained at source
spacer length optimization which is permissible for driving logic applications. However, the device exhibits downfall after $L_S = 1.5 \times L_G$ due to increase of OFF state electron tunneling with more $L_S$.

3.3 $L_D$ Variation with Fixed $L_S$

In this section, the same analysis as in section 3.2 is carried out, but the drain side spacer length is altered while the source side spacer length is fixed at $1.5 \times L_G$. The greater the $L_D/L_G$ ratio, lower the $I_{OFF}$ and $I_{ON}$, as shown in Fig. 6a and b. The $I_{ON}$ increases with lower $L_D$ length. Since higher $L_D$ of device leads to higher resistance to electron flow. Moreover, the $I_{OFF}$ which is significant for low stand by power applications is reduced with higher $L_D/L_G$ value. Since in the OFF state the spacer dielectric fringing fields increase the potential barrier height and restrict tunneling of electrons.

From Fig. 7, increase in spacer length the $I_{ON}/I_{OFF}$ ratio increases up to $2.5 \times L_G$ and then degrades. The device achieves the highest $I_{ON}/I_{OFF}$ ratio at $L_S = 15$ nm and $L_D = 25$ nm at $L_G = 10$ nm with acceptable SS. Moreover, the device $I_{ON}/I_{OFF}$ ratio falls after $2.5 \times L_G$ due to reduced fringing effect with larger $L_D$. Thus, spacer optimization is vital for enhanced performance at nano regime.
3.4 Comparison of Source/Drain Side Spacer Length Variation

The performance metrics of \( L_S \) and \( L_D \) variation on \( I_{ON} \), \( I_{OFF} \), \( I_{ON}/I_{OFF} \), and SS are compared in this section and displayed in Figs. 8 and 9. Both \( L_S \) and \( L_D \) variation on VS NW FET shows contrasting effect on performance metrics. From Fig. 8a and b, both ON current and OFF current decreases with increase in \( L_S \) and \( L_D \). The ON current of \( L_S \) is higher compared to \( L_D \) up to \( 1 \times L_G \), whereas opposite behavior results from \( 1.5 \times L_G \) to \( 2.5 \times L_G \).

The \( I_{OFF} \) of \( L_S \) is more compared to \( L_D \) with spacer distance variation. The lowest \( I_{OFF} \) for \( L_S \) and \( L_D \) takes place at the highest spacer length i.e., at \( 2.5 \times L_G \) whereas, the highest \( I_{OFF} \) occurs at lowest spacer distance i.e., \( 0.2 \times L_G \). Since the highest \( I_{OFF} \) occurs at \( 0.2 \times L_G \), \( 0.5 \times L_G \) and hence they are discarded for device design perspective. The permissible \( L_S \) and \( L_D \) values for the device design are \( 1 \times L_G \), \( 1.5 \times L_G \), \( 2 \times L_G \), and \( 2.5 \times L_G \) respectively. However, the best optimized device set is at \( L_S = 1.5 \times L_G \) and \( L_D = 2.5 \times L_G \) with acceptable SS.

Figure 9a and b shows SS and the \( I_{ON}/I_{OFF} \) performance of the VS NW FET with both \( L_S \) and \( L_D \) versions. The \( I_{ON}/I_{OFF} \) ratio diminishes after \( 2 \times L_G \) for \( L_S \), whereas it increases up to \( 1.5 \times L_G \) for both \( L_S \) and \( L_D \) spacer length variations. So, the maximum allowable range of \( L_S \) variation is limited to \( L_S = 1.5 \times L_G \) to drive device for better switching and low power applications.

Figure 9a shows the SS performance of the VS NW FET for both \( L_S \) and \( L_D \) variations, with the highest SS value at \( 0.2 \times L_G \) and the lowest value at \( 2.5 \times L_G \). Except at \( 0.2 \times L_G \), the device achieves the lowest SS among \( L_S \), and \( L_D \) variations.

4 Spacer Dielectric Optimization

The Fig. 10a and b show the \( I_{DS}-V_{GS} \) characteristics with symmetric (\( L_S = 15 \) nm and \( L_D = 15 \) nm) and asymmetric (\( L_S = 15 \) nm and \( L_D = 25 \) nm) combinations.

The simulated transfer characteristics (\( I_{DS}-V_{GS} \)) with different spacer dielectrics of JL NW FET with symmetric spacer are shown in Fig. 10a. With all spacer dielectrics, the device has an \( I_{OFF} \) of less than nA. With spacer dielectrics, however, the \( I_{ON} \) varies from 60 A to 75 A. The \( I_{DS}-V_{GS} \) of asymmetric spacer variation follow the same pattern as symmetric variation, as shown in Fig. 10b. For all spacer combinations, the \( I_{OFF} \) of the device with asymmetric spacer is less than nA. With the HfO\(_2\) spacer, the \( I_{ON} \) reaches a maximum of 68 A, while with no spacer, it reaches 54 A. According to the results, a rise in the ‘\( k \)’ value causes a decrease in the \( I_{OFF} \). Stronger
the fringing fields result in lower \( I_{OFF} \) when the ‘\( k \)’ value is higher. Due to the spacer fringing electric fields, the depletion region improves. The p-n junctions form the depletion zone in inversion mode FETs, whereas energy barrier generation owing to depletion in the OFF state occurs in JL devices. The subthreshold current decreases as the spacer dielectric value increases because of high vertical electric field at \( V_{DS} = 0.9 \) V and \( V_{GS} = 0 \) V i.e., in the OFF state. Furthermore, the \( I_D \) is marginally affected in the ON state due to the zero electric field induced by the flat band situation. In comparison to Air and SiO\(_2\) spacers, the HfO\(_2\) followed by Si\(_3\)N\(_4\) spacer has good switching behavior and a lower \( I_{OFF} \) at nano-regime. As a consequence of the analysis, high-\( k \) spacer dielectrics such as Si\(_3\)N\(_4\) and HfO\(_2\) excel with better subthreshold and switching behavior at nano-regime, ensuring potential candidate for low-power applications [21]

The \( I_{ON} \) for a device is calculated at \( V_{DS} = 0.9 \) V and \( V_{GS} = 1.2 \) V whereas, \( I_{OFF} \) is calculated at \( V_{DS} = 0.9 \) V and \( V_{GS} = 0 \) V. As seen in Fig. 11a, the \( I_{ON} \) is much lower with the asymmetric spacer than with the symmetric spacer. HfO\(_2\) has the smallest \( I_{ON} \) decrease of all the spacer combinations, at 11.24%. The Si\(_3\)N\(_4\) spacer and no spacer materials had a 13.26 percent and 15.8 percent drop, respectively. Because higher fringing fields with a high-\( k \) spacer diminish the \( I_{ON} \) decrement with asymmetric spacer compared to a low-\( k \) spacer, the \( I_{ON} \) decrement with asymmetric spacer is minimized. The \( I_{OFF} \) for various spacer dielectrics is shown in Fig. 11b. Although symmetric spacers improve \( I_{ON} \), asymmetric spacers diminish direct tunneling of electrons in the OFF state due to the greater distance between the channel and drain. The \( I_{ON} / I_{OFF} \) ratio of a device with varied spacer dielectrics is shown in Fig. 11c. With only SiO\(_2\), Si\(_3\)N\(_4\), and HfO\(_2\) spacers, the asymmetric spacer has a greater \( I_{ON} / I_{OFF} \) ratio than the symmetric spacer. In comparison to Air and no spacer, the symmetric spacer exhibits a modest increase in the \( I_{ON} / I_{OFF} \) ratio due to increased \( I_{ON} \) and marginal \( I_{OFF} \) fluctuation. The negligible difference in \( I_{OFF} \) between symmetric and asymmetric spacers for Air and no spacer is attributed to ineffective leakage control due to decreased dielectric fringing fields. Furthermore, the asymmetric spacer aims to improve the \( I_{ON} / I_{OFF} \) ratio while lowering coupling and parasitic capacitances [22, 23]. With HfO\(_2\) spacer, the asymmetric spacer improves the \( I_{ON} / I_{OFF} \) ratio by 19.6% and reduces \( I_{OFF} \) by 34.13% when compared to the symmetric spacer. Furthermore, as seen in Fig. 11d, the performance of SS is poorer with an asymmetric spacer. Although the \( I_{ON} \) is
lowered by 11.24% with the asymmetric spacer, the sub-threshold behavior and switching performance are improved thanks to a spectacular reduction in $I_{OFF}$.

The electric field on the channel region of the symmetric spacer is higher than that of the asymmetric spacer, as shown in Fig. 12a and b. Due to larger distance between the channel and drain in the asymmetric spacer the electric field lines are minimized into the silicon and thus enhanced tunneling width. Figure 12c and d demonstrate the potential distribution of JL nanowire FETs with symmetric and asymmetric spacers. Because of the long distance between channel and drain, an asymmetric spacer ensures lower SCEs.

5 CMOS Inverter Performance Analysis

Figure 13 depicts the $I_D-V_{GS}$ characteristics of both NMOS and PMOS with optimized symmetric and asymmetric spacers. The gate length $L_G = 10$ nm, EOT (high-$k$ + SiO$_2$) = 0.75 nm, Si channel thickness = 10 nm, and HfO$_2$ as spacer material have all been maintained same as in NMOS. The design for PMOS symmetric spacer is $L_S = L_D = 15$ nm and $L_S = 15$ nm and $L_D = 25$ nm for asymmetric spacer, which is maintained same as NMOS. The $V_{th}$ is matched for both NMOS and PMOS by work function engineering. The SS and DIBL of symmetric and asymmetric spacers NMOS are depicted inside Fig. 13. Furthermore, the delay performance is calculated by CMOS inverter as shown in Fig. 14.

The CMOS inverter delay ($T_D$) is calculated using the effective drive current model, such as in equation 1 [24], where $I_{EFF}$ is the effective drive current, $C_L$ is the load capacitance, and $V_{DD}$ is the supply voltage of the first stage inverter at the output node.

$$T_D = 0.5 \times C_L \times \frac{V_{DD}}{I_{EFF}} \quad (1)$$

The evaluation of $C_L$ is carried through parasitic first stage output and input capacitance of second stage as (2) and a value of 1.5 is considered for miller coefficient (M) [24]. The $C_{IN2}$ is calculated by using the weighted distribution of NMOS and PMOS during input transitions of the OFF and ON-state capacitances. During the output-fall transition to 0.5$V_{DD}$, the transistor P2 remains ON while N2 switches from OFF to ON. As a result, the OFF to ON ratio of 0.25: 0.75 [24, 25] is utilized to calculate $C_{IN2}$ (3).

$$C_L = M \times C_M + C_{IN2} \quad (2)$$

$$C_{IN2} = 0.25 \times C_{G,OFF} + 0.75 \times C_{G,ON} \quad (3)$$

Where, $I_{EFF} = (I_L + I_H + I_M)/3$, $I_M = I_{DS}(V_{DS} = 0.75V_{DD})$, $I_H = I_{DS}(V_{GS} = V_{DD}, V_{DS} = 0.5V_{DD})$, $V_{GS} = 0.75V_{DD}$ and...
$I_L = I_{DS} (V_{GS} = 0.5V_{DD}, V_{DS} = V_{DD})$ as defined in [25], and are taken from the individual $I_D-V_{GS}$ characteristics.

Figure 15 depicts the CMOS inverter delay of symmetric and asymmetric spacer dielectrics. The terms $t_{PHL}$ and $t_{PLH}$ defines the speed of the logic and detrimental in calculating propagation delay ($t_p$). The symmetric spacer exhibits lower delay compared to asymmetric spacers. Since in asymmetric spacer the $L_D$ is 25 nm which is higher compared to symmetric spacer which is 15 nm. Thus, symmetric spacer is better for circuit applications at nano regime [27] and [28]. However, asymmetric spacer outperforms symmetric spacer in terms of OFF current, subthreshold performance, and good switching behavior.

Fig. 12 Electric field and potential distribution contour plots a, c $L_S = L_D = 15$ nm, b, d $L_S = 15$ nm $L_D = 25$ nm in ON state with HfO$_2$ spacer

Fig. 13 PMOS and NMOS $I_D-V_{GS}$ characteristics of symmetric and asymmetric spacer
The proposed VS nanowire FET is compared with FinFET, nanowire, and nanosheet FET and their electrical characteristics are presented in Table 2.

### 6 Conclusion

In this work detailed study of spacer length has been presented on n-channel SOI JL VS NW FET. According to the performance optimization metrics, spacer length modification has a serious effect on SCE reduction. By result analysis the $I_{ON}/I_{OFF}$ ratio with $L_S = 1.5$ nm and $L_D = 2.5$ nm exhibits best performance. Among optimized $L_S$ and $L_D$ values an improvement of 22.69% in $I_{ON}/I_{OFF}$ ratio is noticed with $L_D = 2.5 \times L_G$, whereas the SS is reduced i.e., 63 mV/dec to 62 mV/dec. The highest OFF current with $0.2 \times L_G$ and $0.5 \times L_G$ for both $L_S$ and $L_D$ variations are not considered for device design considerations. For $L_S$ variations $2 \times L_G$ and $2.5 \times L_G$ are neglected, whereas for $L_D$ the spacer length $3 \times L_G$ is not considered since the device $I_{ON}/I_{OFF}$ ratio tends to down fall. From the result analysis with $L_S = 15$ nm $L_D = 25$ nm and high-ε spacer for 10 nm n-channel JL VS NW FET shows best optimized results. Hence optimized asymmetric VS NW FET exhibit low OFF current, higher $I_{ON}/I_{OFF}$ ratio and hence assures low standby power requirements and low power applications. Moreover, symmetric spacer exhibits higher $I_{ON}$ and lower delay and assures high performance applications.

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### Author Contribution

V. Bharath Sreenivasulu: Writing- Original draft preparation, Formal Analysis, Investigation, Simulation, Data Curation.
V. Narendar: Supervision, Resources.

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