Automated Design Space Exploration for optimised Deployment of DNN on Arm Cortex-A CPUs

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Abstract—The spread of deep learning on embedded devices has prompted the development of numerous methods to optimise the deployment of deep neural networks (DNN). Works have mainly focused on: i) efficient DNN architectures, ii) network optimisation techniques such as pruning and quantisation, iii) optimised algorithms to speed up the execution of the most computational intensive layers and, iv) dedicated hardware to accelerate the data flow and computation. However, there is a lack of research on the combination of these methods as the space of approaches becomes too large to test and obtain a globally optimised solution, which leads to suboptimal deployment in terms of latency, accuracy, and memory.

In this work, we first detail and analyse the methods to improve the deployment of DNNs across the different levels of software optimisation. Building on this knowledge, we present an automated exploration framework to ease the deployment of DNNs for industrial applications by automatically exploring the design space and learning an optimised solution that speeds up the performance and reduces the memory on embedded CPU platforms. The framework relies on a Reinforcement Learning-based search that, combined with a deep learning inference framework, enables the deployment of DNN implementations to obtain empirical measurements on embedded AI applications. Thus, we present a set of results for state-of-the-art DNNs on a range of Arm Cortex-A CPU platforms achieving up to 4x improvement in performance and over 2x reduction in memory with negligible loss in accuracy with respect to the BLAS floating-point implementation.

I. INTRODUCTION

Artificial intelligence (AI) is rapidly growing and will soon become ubiquitous in our daily life. In particular, deep learning has grown quickly in the last years, achieving remarkable results in computer vision [1] and speech recognition [2]. Adoption of deep learning by major industrial players, e.g., Google [3], Tesla [4], is already a reality, and its numerous applications are to bring on a new technological revolution.

Deep Neural Networks (DNN) are capable of learning abstract features by stacking many layers in parallel and in depth, which turns them into complex architectures. Training of CNNs has drawn significant attention in the last years towards building more and more competitive and accurate architectures [5] and surpassing human capabilities, e.g., ImageNet competition [6]. More recently, the focus has shifted towards the deployment of such DNNs on resource-constrained devices. In contrast to cloud environments, edge devices are often severely constrained in terms of computing power, memory, and energy consumption, which is available to a given application. These constraints hamper deployment of deep learning solutions to edge devices and require innovation in the design of deep learning systems (or neural network architectures), and in the software which executes them.

Numerous research works have focused on optimizing the deployment of DNN through the development of i) efficient DNN architectures such as MobileNets [7], SqueezeNet [8], including hardware-aware neural architecture search (NAS) [9], [10], ii) optimisation techniques such as pruning and quantisation [11], [12], [13], [14], iii) optimised algorithms to speedup the execution of the most computational layers, e.g., general matrix multiplication (GEMM) [15] or Winograd [16] and, iv) dedicated hardware to accelerate the data flow and parallelise the computation [17], [18], [19].

There is, however, a lack of research on cross-level optimisation and design space exploration (DSE) for a complete end-to-end solution [20]. The space of approaches for DNN deployment becomes too large to fully explore and obtain an optimal implementation as each layer of the neural network may be executed following a different optimisation technique, optimised algorithm, or even in a different processor, resulting in a different performance, memory footprint or power consumption. The complexity of exploring and combining the wide variety of design options usually results in a sub-optimal solution [21].

The objective of this work is to ease the deployment of pre-trained DNNs for industrial applications by automatically exploring the design space and finding an optimised solution to speed up the performance and reduce the memory on embedded CPU platforms. To that end, we employ LPDNN [22], a deep learning framework that enables the deployment and inference of DNN implementations. We focus on software optimisation for the deployment on Arm CPU cores as these represent the majority of processors on mobile and IoT devices and have extensive support for DNN inference [23]. Our work is complementary to DNN architecture design to optimise the deployment further and could also be applied to dedicated hardware. Our contributions are the following:
• We analyse methods to improve the deployment of DNNs across different levels of software optimisation and introduce the range of techniques provided by LPDNN to optimise DNN inference.
• We present QS-DNN, an automatic exploration framework based on Reinforcement Learning (RL), that, combined with LPDNN, finds an optimised combination of design options that speeds up DNN inference and reduces memory for a target platform.
• We present a set of results for state-of-the-art DNNs on a wide range of Arm Cortex-A CPU platforms that cover the current spectrum of deployment on mobile devices.

The paper is organized as follows: In Section II, we present the background of the optimization for the deployment of DNNs. Section III describes the deep learning inference framework. In Section IV, we address the design space problem and introduce the Reinforcement-Learning-based approach. In Section V, we introduce the RL-based search engine and the methodology of the experiments. Section VI presents the results and discussion.

II. BACKGROUND: DEPLOYMENT OPTIMISATION OF DEEP NEURAL NETWORKS

Given the constraints imposed on edge devices, namely, relatively limited compute performance, small memory capacities, and thermal and power consumption restrictions, there are several goals for which one may choose to optimise. For example, one might decide to sacrifice neural network inference latency to reduce overall power consumption, or to stay within a more limited memory capacity. Depending on the goal of the optimisation, neural networks present a range of software optimisation opportunities. We divide these opportunities into several broad categories as shown in Fig. 1:

A. Network Design

We define network design optimisation to be the set of techniques that tailor the structure of a network before, or during training, to improve the latency or cost of network inference. Examples of this are MobileNet-V1/V2 [7], [24], SqueezeNet [8] and, ShuffleNet [25] which were manually shaped thanks to the expertise of the authors. A set of newer works introduced the neural architecture search (NAS) as a technique to reduce the high-level human knowledge needed for the conception of such architectures. Examples of this are MNASnet [26], FbNet [10], and Lemonade [27] which used hardware-aware NAS via reinforcement learning, evolutionary algorithms or gradient-based methods to discover neural network structures with both good accuracy and high performance.

Distillation is another technique where a neural network teacher can transfer its learned knowledge to student networks. Students are constructed to present lower computational complexity and memory cost than their teachers. The student imitates the teacher over a training dataset and obtains high accuracy while reducing the complexity of the neural network. Works implementing this technique are [28], [29], [30].
bitwidth down to binary networks \cite{38,39} and, ii) techniques to find a suitable trade-off between compression and accuracy where autoML methods represent the SoA for mixed-precision inference \cite{40,41,42}. We refer the reader to extensive analyses for efficient quantisation deployment, which are provided by \cite{43,44}.

All the mentioned works provide quantisation methods or tools that involve training or fine-tuning the DNNs to push the limits of quantisation as well as a large training dataset. There are, however, several works that provide tools for post-training (direct) quantisation achieving 8-bit \cite{44,45,46} or even 4-bit \cite{47,48} inference with minimal loss in accuracy, making them very attractive for any user to deploy DNNs efficiently on embedded devices.

3) Layer fusion: Layer fusion can improve the memory traffic of a DNN as several linear operations in a neural network graph can be fused into a single one – avoiding repeatedly writing and rereading the same area of a tensor. In general terms, the fusion of two consecutive layers approximately halves the memory traffic associated with the combination. Examples of this are merging the batch normalisation and scale layer or the activation and concatenation layer into the previous convolution or fully connected layer. Further memory optimisations can be achieved by different layers sharing the same memory space if there is no dependency between them, e.g., in-place computation or network-memory pool.

C. Algorithm Optimisation

Once a network has been designed (and possibly optimised through application of quantisation, sparsity, or fusion), execution of the network can be optimised through modification of the way in which layers of the network are implemented. We mainly focus on the performance optimization of convolutions since these comprise the lions share of the computation work contained in a neural network. There are several ways in which convolution can be performed: direct convolution; a number of the several approaches that exploit a General Matrix-matrix Multiplication (GEMM) call; or by one of many fast-convolution methods like Winograd convolution. Each of these methods has its own trade-offs.

1) Direct: A naive approach to implementing convolution on CPU is to directly implement the six-nested for loop which describes convolution. Although direct convolutions incur no memory overhead, its usage is rare since it is difficult to express the algorithm in a way that extracts much performance from CPU architectures \cite{49}. Implementations can be improved by keeping some of the weights, inputs, or outputs resident in registers – especially for a small number of parameters \cite{50} – and reordering the layout and loops to optimise data reuse \cite{51}.

2) GEMM-based: Use of GEMM is attractive to accelerate convolutions since there exist a wide range of fast implementations provided by highly optimised BLAS libraries such as OpenBLAS \cite{52} or BLIS \cite{53} capable of exploiting the SIMD instructions of the Armv8-A architecture. The prototypical approach to constructing a GEMM-backed convolution is to use the im2col or im2row algorithms to construct a “patch” matrix, which can be multiplied by a matrix representing the convolution weights to form the final output matrix. It should be noted, however, that while the amount of work performed by the GEMM is equivalent to direct convolution, the memory footprint is \(k^2\) larger (where \(k\) is the size of the kernel). This significant memory overhead has led to research into more memory efficient GEMM-backed convolutions. Examples of which are the \texttt{kn2row} technique \cite{15}, and indirect GEMM \cite{49} approach – neither of these techniques reduce the arithmetic cost of performing a convolution, although they do avoid the cost of rearranging the data into \texttt{im2col} or \texttt{im2row} form.

3) Winograd: Winograd Convolution \cite{54} can help to address the problem of the high arithmetic cost of convolution. These algorithms help to reduce the overall compute complexity of convolution by transforming the convolution into another domain where the number of required strong operations (such as multiplication) is reduced at the expense of an increase in the number of weak operations (such as addition). Implementations of these algorithms are well suited to low power embedded systems, as the resources and power budget are very limited. By contrast, they have a higher cost in memory consumption and accuracy \cite{16}.

D. Primitive design

Finally, the lowest level of software instantiating a neural network can be optimised to make better use of the hardware upon which it is executed. All of the algorithms described in the previous sections feature at least one loop, which will be executed many thousands of times during neural network inference. Ensuring that this innermost loop is implemented as well as possible is vital to achieving good overall performance. Optimisations at this level of abstraction can vary from changing the layout of data in memory, through changing how vectorised instructions are used to process the layer, to writing assembly implementations of the kernels to extract maximum performance from specific processors.

1) Data layout: Ensuring that operands are laid out to achieve proper use of the processor cache hierarchy, and easy exploitation of vectorized execution may produce significant improvements in performance \cite{16}. Indeed, several works, including \cite{21,55}, apply several algorithms to find an optimised selection of data layout for each layer of a DNNs.

2) Vectorisation: It is crucial that the vector (Single Instruction Multiple Data – SIMD) instructions provided by the Instruction Set Architecture (ISA) are used to make the most of processor throughput. Examples of works leveraging vectorisation for the optimisation of convolutions on GPU or CPU are \cite{56,53,16}.

3) Assembly code: Modern compilers, while good at ensuring general-purpose code can be compiled into fairly efficient assembly, have some drawbacks. Writing assembly code by hand can allow the programmer to perform optimisations missed by the compiler and allows for a much greater degree of control of the final binary.
E. Discussion

The vast majority of the works presented above focused on specific optimisations for DNNs without taking into account the trade-offs at different levels of the software stack. We draw inspiration from Anderson et al. [21] who use PBQP to optimize inference time by selecting suitable backends. However, they only profile the latency for convolutional layers without addressing other layer types or optimisations at network level, e.g., quantisation.

In this work, we provide a broader picture and show the various steps of the optimisation for the deployment of DNNs on CPU. Furthermore, we present an automatic exploration framework, based on Reinforcement Learning, that searches through different design option and analyses several DNNs on a range of embedded platforms while trading off metrics like latency, memory, or accuracy. Thereby, we can find a solution that, for instance, can answer the following questions: What DNN shall I use? What are the best optimisation techniques that I can follow? How can I obtain a fast implementation under a certain memory or accuracy constraints?

III. DEEP LEARNING INFERENCE FRAMEWORK

We form part of a European collaboration to bring deep learning methods to any party who would like to take up deep learning solutions in an industrial environment [57]. In this context, a deep learning framework (LPDNN) has been developed [22] to produce efficient and tunable code that enables and maximizes the portability among platforms. In this work, we introduce the range of techniques provided by LPDNN to optimise the deployment of DNNs. Besides, we address the integration of the LPDNN into our search environment to tightly couple empirical measurements of a heterogeneous platform to a learning-based search.

A. Architecture

One of the main goals of LPDNN is the portability and flexibility of AI applications across platforms. LPDNN’s core comprises a set of CPU dependency-free functions which can be complemented by specific-platform acceleration libraries, such as Arm Compute Library [58] and cuDNN [59], to generate an optimised implementation for the system. LPDNN contains a modular and hierarchical architecture that supports multiple libraries and optimisations at the same time. This flexibility allows us to experiment with optimised algorithms for a particular layer or blocks to execute each layer with the most suitable implementation according to the network architecture, target platform, and desired accuracy and performance specification.

B. Optimisations

We follow the structure given in Section [11] and show the software optimisations that LPDNN contains at various levels:

1) Network optimisation: LPDNN provides efficient inference with integer arithmetic as it supports post-training quantisation for both weights and activations. Weights can be directly quantised to 8-bit integer while the activations require a validation set to determine their dynamic range. The range is then used to calculate the scale and offset for both symmetric and asymmetric quantisation methods. The scale value can be further tuned to reduce the loss of information by minimising the KL divergence between the quantised and original distribution [46]. LPDNN supports both per layer and per channel quantisation. However, due to the lack of support by the acceleration libraries for channel quantisation, we only focus and show results for the former.

Several other optimisations are performed in LPDNN:

- **Static layer fusion**: Fusion of linear operations to reduce the neural network graph at build time. LPDNN supports the fusion of the Bnorm and scale layers into the previous convolution or fully connected layer.
- **Runtime layer fusion**: The execution of two or more layers is performed in a single pass with a significant reduction in memory traffic. LPDNN supports the fusion of the activation and concatenation layers into the previous convolution.
- **In-place computation**: Layers such as activation, reshape or, flatten may store the output result directly on the memory allocated for the input, which halves the memory allocations for a layer.
- **Memory pool**: Layers whose execution does not overlap and who do not have data dependencies, share the same memory, which – due to the sequential nature of most DNNs – notably reduces overall memory footprint.

2) Algorithm optimisation: LPDNN integrates a set of acceleration libraries including, OpenBLAS, BLIS, NNPACK and, ArmCL, that provide optimised algorithms for the execution of DNNs on CPUs. LPDNN leverages the algorithms provided by the libraries and may execute each layer of the network with a different algorithm. Further, LPDNN also uses a lower-level interface of the Arm Compute Library that we refer to as LPDNN-Arm library. It supports both floating-point 32-bit (FP32) and integer 8-bit (INT8) operations and provides special optimisations for the following layers:

- **Standard convolution**: LPDNN integrates a FP32 fast convolution implementations that relies on Winograd for 3x3, 5x5 and linear kernels (originally from [16]), and a vectorised GEMM implementation for all kernels, including the common 1x1, for both FP32 and INT8.
- **Depthswise Convolution**: Despite containing relatively little computational work, is challenging to implement efficiently due to its memory-bound nature. LPDNN’s exploits all the reuse presented by the algorithm by carefully mapping to both the SIMD instructions and the cache for both F32 and INT8.
- **Others**: LPDNN also optimises pooling, element-wise and, activation layers by providing vectorisation for both F32 and INT8 implementations.

- **Fusion of linear operations**
- **In-place computation**
- **Memory pool**

- **Standard convolution**
- **Depthswise Convolution**
- **Others**
3) Primitive design: In Section II we noted three different elements of primitive design which can be combined to build optimised kernels to implement neural network algorithms. These were data layout, vectorisation, and assembly code.

The first two of these are neatly tied together: the order in which data is stored suggests the vectorisation approach taken and vice versa. For example, when implementing a vectorised convolution one may decide to operate on several channels of data simultaneously, in which case storing channels contiguously facilitates easier use of the data. We have determined empirically that, on CPUs, it is often better (both easier and more performant) to write kernels which operate on multiple channels simultaneously [16, § 2.1]. Consequently, the majority of optimised kernels in LPDNN operate of NHWC-ordered data (where N stands for the number of batches, H for the height of the tensor, W for the width and C for the number of channels). However, it can still be beneficial to support data in other formats (as shown in Section VI) – for example, when the channel count is low it is better to make use of data-reuse across the plane of a convolution.

We noted above that it can often be worth hand-writing assembly code implementations for key kernels, rather than relying on the compiler. There are a few reasons for this, largely stemming from wanting finer-grain control over register allocation, instruction selection and scheduling than is possible from use of compiler intrinsics. LPDNN integrates several hand-optimised vendor kernels covering algorithms such as GEMM and depthwise convolution.

IV. LEARNING-BASED SEARCH ENGINE

In this section, we address the design space problem for the deployment’s optimisation of DNN and we propose Reinforcement Learning as a solution.

A. Problem formulation

Given a DNN, each layer of the neural network may follow a different optimisation technique, or be executed by different acceleration libraries which, in turn, might provide several algorithms, data types or layouts. The space of approaches for DNN deployment becomes too large to test exhaustively and obtain an optimal implementation. The problem is not as trivial as to benchmark all possible implementations individually and select the most suitable for each layer to make up the optimal network implementation. Each implementation may follow a different optimisation strategy, have a different layout, data type, or even be executed in a different processor which might not correspond to those from the previous and following layers. Therefore, incompatibilities arise and a conversion or data copy layers are needed which incur in extra penalties, see Fig. 2.

The number of combinations within a network, which is the design space to explore, grows exponentially with the number of layers, $N_L$, having as base the number of different implementations for such layer, $N_I$. Hence, the design space size for a network would be $N_I^{N_L}$ as the worst case. This is a non-trivial problem and therefore, a careful search must be carried out to select the right set of deployment options that, combined and assuming the conversion penalties, yields the most suitable implementation for a given goal, e.g., latency, accuracy or memory.

B. Reinforcement Learning Approach

Reinforcement Learning (RL) lends itself perfectly to exploring large design spaces due to its sample-based approach and far-sighted accumulative reward [60], [61]. Consider the network space exploration as a Markov Decision Process (MDP) containing an agent. We are interested in learning a function that optimises the agent’s behavior or policy $\pi(a_t|s_t)$, i.e., mapping from state $s_t$ to actions $a_t$, without modeling the environment and only relying on the reward function. Q-learning [62] fits well this description as it is a model-free and value-based implementation, having the policy implicit in the value function. The action-value function $q_\pi$ is the expected return $G_t$ in a state $s_t$ taking an action $a_t$:

$$q_\pi(s, a) = E_\pi [G_t | s_t = s, a_t = a]$$

The objective of Q-learning is to maximize the total reward: $R_T = \sum_{t=0}^{\infty} \gamma^t r_t$ where $r_t$ is an individual reward and $\gamma$ is the discounted factor for successive states. Besides, Q-learning is an off-policy implementation, that is, it may follow a behavior policy $\mathcal{B}$ while targeting a greedy policy $\mathcal{E}$. Following Bellman’s equation, we can iteratively update the action-value function ($Q = q_\pi$) as follows:

$$Q(s_t, a_t) = Q(s_t, a_t)(1 - \alpha) + \alpha [r_t + \gamma \max_a Q(s_{t+1}, a)]$$

C. Search Engine

We consider an agent whose aim is to learn the optimal path among a large but finite set of states $S$ i.e., layer representations, employing a set of actions $\mathcal{A}$ i.e., layer implementations. RL suits well the specifications of the problem that we address in this work. Latency, accuracy or memory represent clear reward function given by the environment that we aim to explore: a Deep Neural Network.
phases:

a) DNN is to automatically optimise the inference of any DNN framework for the deployment of DNNs. The aim of QS-DNN is to leverage the optimisations at network, algorithm and primitive level. The objective is to measure the costs of all possible graph nodes, i.e., layer implementations, and all possible edges, i.e., the compatibility conversions inserted between each node, to build a look-up inference table for the search engine.

Thus, the inference controller goes over each acceleration library and benchmarks each implementation\(^1\) one at a time, in all those layers where the library is able to implement such implementation. Therefore, we only need to infer the whole network on the embedded platform as many times as different global implementations exist. In each inference, the execution time and memory consumption for each layer are measured. Once all the implementations have been benchmarked, we profile the compatibility conversions for data type and layout transformation as well as for data transfers between different processor if needed.

B. Search Engine (2/3)

The search space and the conditions of the search can be defined for each network. They specify the behavior of the agent: number of episodes for each \(\epsilon\), learning rate, discounted factor and replay buffer’s size. We have set the learning rate to 0.05 and discounted factor to 0.9 to give slightly more importance to short-term rewards. Once the metrics collection phase has finished, the Q-learning-based search begins and proceeds as shown in Algorithm\(^1\).

First, \(\epsilon\) is retrieved from the specifications as well as the number of episodes for each \(\epsilon\). In all experiments, 50% of

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| State Parameters       | Definition                                                  |
|------------------------|-------------------------------------------------------------|
| Layer type             | Any layer, e.g., convolution, pooling                       |
| Layer depth            | Position of the layer in the network                       |
| Acceleration library   | Name of the library                                         |
| Algorithm              | Routine type                                                |
| Algorithm config       | Sub-routine or lowering method                              |
| Data type              | Any type, e.g., FP32, FP16, INT8                           |
| Data layout            | Any layout, e.g., NCHW, NHWC                               |
| Target hardware core   | CPU, GPU, FPGA                                              |

Table I: State Space. Parameters define the execution implementation of a layer on a target platform.

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1Each implementation is inferred for 20 images and the mean is calculated.
Inference of Learnt Solutions (3/3)

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the total episodes correspond to full exploration and 5% to any other $\epsilon$ from 0.9 to 0.1. By these means, the agent obtains enough knowledge from the environment before starting exploitation, see Fig. 4.

For each episode, the agent samples sequentially a new set of implementations based on the $\epsilon$-strategy. Once the network’s configuration is set, the engine automatically looks for incompatibilities between layers. At last, the total network inference time is computed by looking up each implementation in the inference table and summing up the values of all layers. If any incompatibility has been found between two layers, the extra penalty in time is added to the inference time of the latter layer. Finally, the action-value function is updated with the current reward and stored for experience replay. When the number of episodes for a given $\epsilon$ has been met, $\epsilon$ is decreased towards exploitation phase. By the end of the search, the engine gives out the most performing configuration and the learning curve that the agent has followed, see Fig. 4.

C. Inference of Learnt Solutions (3/3)

A drop in accuracy may be caused by quantized or fast-convolution methods. Thus, we perform the accuracy measurements after the RL-based search have been performed and benchmark the learnt solutions against a validation dataset. We are only interested in the most performing networks and hence, only benchmark those solutions that are up to 25% slower than the fastest learnt solution. Thus, we can speed up the process and obtain Pareto optimal solutions with a strong focus on latency optimisation having accuracy and memory as thresholds, e.g., accuracy drop <1% or memory reduction >2x.

VI. EXPERIMENTAL RESULTS AND DISCUSSION

In this section, we show the optimisation results for the deployment of state-of-the-art DNNs on a range of Arm Cortex-A CPUs. First, we introduce the set of networks and platforms that we have used to validate our experiments. Next, we show the importance of the different individual software optimisations currently available in LPDNN (see Section III-B). Finally, we present the results from applying the automated design space exploration, introduced in Section V, to optimise deployment of DNNs on Arm Cortex-A CPUs.

A. Experimental setup and platforms

The set of pre-trained networks that we have selected form part of the Imagenet contest (image classification task) as it represents a challenging dataset where optimisations can have a significant effect on metrics such as latency, accuracy, and memory. We evaluate several representative network topologies for resource-constrained devices that allows us to show the range of optimisation and trade-offs on the target platforms: small networks such as Squeezenet and MobilenetV3-small, slightly more complex networks like MobilenetV2, and reasonably large networks such as MobilenetV3-large and Resnet50. Although we have focused on an image classification task to demonstrate our design, the experiments could also be applied to any other deep learning task.

The range of Arm Cortex-A (Armv8 64-bit) CPU platforms that we have chosen cover the current spectrum of deployment on mobile devices. We divide the experiment into two parts: i) For each of the techniques discussed in Section III-B we present benchmark results on the RaspberryPi 4 (Cortex-A72 at 1.5GHz) as a reference platform to show each optimisation. ii) For the automated DSE discussed in Section V we show experiments on the Raspberry4, Nvidia Jetson Nano, CPU only (Cortex-A57 at 1.43GHz) and, RaspberryPi 3b+ (Cortex-A53 at 1.4GHz) to validate the design and optimisations on LITTLE and big cores:

- **Cortex-A53** is a low-power, highly efficient, core [67]. Power efficiency is achieved through running inorder [68], hence this core is highly sensitive to instruction order and operand data availability.
- **Cortex-A57** is a higher-performance, and consequently higher-power, out-of-order core [69].
- **Cortex-A72** is an update to the Cortex-A57 with improved floating-point and memory performance [70].

All inferences are performed identically: using a single-thread, calculating the average of twenty inferences after an initial (discarded) warm-up run. The boards were fitted with a heatsink, and the CPU frequency governors were overridden to achieve the maximum possible performance. To ensure that the platform does not overheat, triggering thermal throttling.
we have monitored the platforms and sampled the OS registers each second.

### B. Optimisation results

In this section, we demonstrate the improvement in performance due to the software optimisations explained in Section III-B.

#### 1) Network Optimisation

- **Quantisation:** We compare the performance of DNN layers when they are deployed employing INT8 arithmetic instead of the baseline FP32 operations. Although INT8 variables can be packed into 32-bit operations and, therefore, achieve a theoretical x4 arithmetic-intensity improvement, the real uplift in performance may not be as much. For instance, Fig. 5 shows INT8 performance uplift for Squeezenet’s convolutions, where the highest layer improvement goes no higher than 1.7x and the overall network speedup (including all layers) is 1.24x. These results are roughly in line with [71], where speedups of 1.13x and 1.2x are obtained by using INT8 on a small and big core of the Snapdragon835, respectively.

#### 2) Algorithm Optimisation

We compare the performance of DNN layers with respect to FP32 is due to several factors:

- **Layer fusion:** Fig. 6 shows the performance improvement obtained by static and runtime layer fusions. Fig. 6a depicts the static fusion of Bnorm and scale layers into previous convolutions for Mobilenet-V2, obtaining a 25% improvement in latency. Such significant improvement is mostly due to the lack of optimisation on both fused layers as this graph reduction is a common approach in many inference frameworks.

- **Memory optimisation:** Table II displays the total dynamic memory allocated over the execution of various DNNs in terms of weights, activations, and other (structures, buffers, or code). We can observe that, while the activations account for a small portion in Resnet50, they consume most of the memory allocated in Squeezenet and Mobilenet-V2. This, we show the reduction in memory achieved in the allocation of the activations by in-place and memory pool techniques. The use of in-place technique achieves a noticeable reduction, especially on the ReLu layers, which varies from 16.1% (Resnet50) to 37.2% (Mobilenet-V2). Further, memory pool technique accomplishes a remarkable memory reduction that goes from 80% (Squeezenet) to 88.1% (Mobilenet-V2) thanks to the reuse of memory across layers. Further memory optimisations can be achieved by applying quantisation which would provoke a 4x reduction in the memory allocated for the weights and the remaining activations.

- **Quantisation:** We further show the speedup achieved by Winograd-FP32 over GEMM-FP32 for Squeezenet’s 3x3 convolutions (Winograd not available for k=1x1 in LPDNN). We can observe that Winograd clearly outperforms GEMM-FP32 in all convolutions, accomplishing an uplift of up to 2.5x. Likewise, Winograd achieves a speedup of up to 3.9x for Resnet50, especially in the first convolutions, which are the most computing-intensive (Fig. 4 in Appendix). Further, we have included GEMM-INT8 performance in...
both figures to demonstrate that early design decisions may lead to sub-optimal solutions, e.g., selecting the use of quantisation at network level without considering the underneath algorithm level. In this case, selecting uniform quantisation, e.g., INT8 data type for the whole network, discards Winograd algorithm as, to date, it is only available in FP32. Thus, a homogeneous INT8 network would underperform against a mixed-precision network, including Winograd.

3) Primitive Optimisation: We show the influence of data layout for vectorised methods employing the GEMM algorithm. Fig. 8 present the most computational-intensive convolutions of Squeezenet (kernel=3x3). We can observe that NCHW performs slightly better in the first layers, which might be due to a lower number of channels in this stage of the network and, therefore, lower reuse of data under the NWHC layout. Nonetheless, NHWC broadly outperforms NCHW on 3x3 kernels, and also on 1x1 kernels, which, having a lower degree of data reuse across the plane of the convolution, are notably more performing under the NHWC layout. Overall, NHWC achieves a reduction in the latency of 8% throughout the network.

Another substantial improvement is the optimisation of the first convolution, which typically accounts for one of the most time-consuming layers. Input data is generally organised in NCHW-order while, by contrast, many performant convolution primitives prefer an NHWC layout (as we saw previously). However, converting from NCHW to NHWC (particularly where only three channels of data are concerned) to match the preferred input layout of the first convolution is relatively costly and hence undesirable. We can avoid this by taking input data in NCHW and producing NHWC directly – avoiding additional rearrangement. This is achieved simply by providing an im2row routine specialised for NCHW-order data and a low channel count.

C. Automated Design Space Exploration (DSE)

We aim to show the trade-offs between latency, accuracy, and memory footprint when all the different levels of software optimisations shown in Section VI-B are available and may be applied, e.g., employing either quantised, or fast-convolution methods may have a substantial impact in all three metrics. We illustrate the DSE and the optimisations achieved by QS-DNN by providing two Pareto fronts: latency-accuracy and latency-memory, where we present the achievable performance based on different degrees of accuracy and memory.

To show the optimization improvements, we display the following interesting points on the graphs:

- **Ref-FP32**: We take LPDNN coupled with Openblas library as reference implementation since it is a well-known and standard library for industrial deployment. Ref-FP32 employs GEMM-based methods under NCWH layout for convolutions and fully connected layers and direct methods for any other layer.
- **Opt-FP32**: Solution found by QS-DNN when only FP32 implementations are allowed, i.e., no quantised methods.
- **INT8**: Fully INT8 deployment implementation.
- **Pareto front**: Set of points that are not dominated by any other implementation based on the two given objectives.

For the sake of fairness, static layer fusion (graph reduction) and memory pool optimisations are always ON for all implementations.

1) Latency-Accuracy: Fig. 10 illustrates the most interesting points found by QS-DNN while performing a DSE for the range of networks on the Jetson Nano. Dotted lines represent the loss in accuracy (1%, 2.25%, 5% and 10%) with respect to the Ref-FP32 implementation while braces expose the performance gains.

Generally, we can observe that the DSE provided by QS-DNN for Opt-FP32 clearly outperforms Ref-FP32 from 1.7x
(Resnet50) to 3.87x (MobilenetV3-small) with no loss in accuracy. We can explain this significant improvement mainly due to the selection of Winograd convolutions for SqueezeNet and Resnet50 and, optimised depthwise convolutions for Mobilenets. Besides, techniques such as runtime layer fusion and the optimisation of layouts through the network make a meaningful impact in performance.

By allowing QS-DNN to select quantised methods, further improvement can be achieved with only a small drop in accuracy: up to 1.05x and 1.2x increase in performance with under 1% and 3% drop in accuracy for SqueezeNet and Resnet50, respectively. Mobilenets, on the other hand, are significantly more sensitive to quantisation and their accuracy drops drastically when quantised methods are employed. This sensitivity to quantisation is largely due to depthwise convolutions, as each channel represent an independent kernel and may have very different ranges. As our acceleration libraries only support layer quantisation, i.e., one range or scale per layer, the use of quantised depthwise layers clearly hurts the accuracy (see the fully INT8 solution on Fig. 10). Thanks to the DSE given by QS-DNN, we can find mixed-precision solutions that bring up to 1.10x and 1.13x increase in performance with a modest drop in accuracy of around 3% and 8% for MobilenetV3-small and -large respectively.

If we compare the Pareto fronts of the networks on the different platforms, we can see in Fig. 12 that there is not a significant difference in latency or accuracy between the RPI4 and the Jetson Nano while the RPI3, containing a “LITTLE” Arm core, performs around 2x slower. Interestingly, no fully INT8 solution forms part of the Pareto front on the RPI4 and Jetson Nano platforms. This indicates that fully quantised networks may not always be optimal in terms of latency due to a lack of support for certain primitives and the need for requantisation after each layer.

2) Latency-Memory: As we described earlier, the memory pool optimisation for the activations is always ON and achieves over 80% reduction in memory allocation. Hence, we can only achieve further reductions of memory by reducing the size of the weights, e.g., through quantisation. Fig. 11 shows the most interesting points found by QS-DNN while performing a DSE for the range of networks on the Jetson Nano. Dotted lines represent the memory consumption for the weights (75%, 50%, and 25%) with respect to the Ref-FP32 implementation while braces expose the performance gains.

Building from the Latency-Accuracy graph, we see that the Latency-Memory Pareto fronts are convex rather than linear. While FP32 layers are preferred in the Latency-Accuracy DSE...
due to their higher precision, in this case, quantised methods are favoured due to their lower memory footprint, being the fully \textit{INT8} solution the lowest point of the Pareto front (25\%) for all networks. From the lowest point, the Pareto rises and turns towards less latency as some more performing FP32 algorithms are picked, e.g., Winograd, which increases the memory up to 0.58\% and 0.65\% for Squeezenet and Resnet50, respectively.

Distinctly, Mobilenets’ Pareto fronts rise less and tend to remain close to 25\% as they do not contain any Winograd implementation and quantized methods are more efficient. Overall, if we combined the optimisations in memory from both the weights and activation, the total memory reduction can go up to 1.9x and 2.3x for small networks like Squeezenet and MobilenetV3-small and, up to 1.6x and 2.5x for larger networks such as Resnet50 and MobilenetV3-large.

From the comparison between the Pareto fronts on the different platforms (Fig. [13]), we can draw that the RPI4 performs slightly better than the Jetson Nano. This may indicate, given the similar FP32 performance, that quantised methods are more performing on the A72 core than the A57 counterpart. Interestingly, the Pareto front of Mobilenets on the RPI3 consists of one point, the \textit{INT8} solution. This can be explained by looking at the Latency-Accuracy Pareto front of Mobilenets where \textit{INT8} solutions are the fastest ones (despite the poor accuracy), which denotes the efficiency of quantized methods for this network topology on the A53 core.

3) Discussion: Thanks to the automatic DSE provided by QS-DNN, we can quickly analyse several DNNs on a range of embedded platforms and find a suitable solution for a given problem. Thus, analysing the previous experiments, we can observe that the recent MobilenetV3s are far more efficient than Squeezenet and Resnet50, e.g., MobilenetV3-small performs 3x faster than Squeezenet (on the Arm Cortex-A57) and is and over 8\% more accurate while having the same memory footprint. Likewise, we could select the most suitable platform for a given problem based on latency, memory or energy constraint.

VII. CONCLUSION AND FUTURE WORK

We have analysed the methods to improve the deployment of DNNs across the different levels of software optimisation and introduced the range of techniques provided by LPDNN to optimise DNN inference. Building on this knowledge, we have shown that single optimisation methods may lead to sub-optimal deployment for end-to-end solutions in terms of latency, accuracy, and memory footprint.

Therefore, we have introduced an automated exploration framework that relies on a Reinforcement-Learning-based search which, combined with LPDNN, enables the deployment of DNN implementations to obtain empirical measurements. Thus, we are able to learn an optimised solution for a given task by automatically exploring the deployment design options on the target embedded device. To validate the design, we have presented a set of results for state-of-the-art DNNs on a range of Arm Cortex-A CPU platforms achieving up to 4x improvement in performance and over to 2x reduction in memory with negligible loss in accuracy with respect to the BLAS floating-point implementation.

We aim to extend this work to micro-controllers where the resources are very limited, and careful design needs to be performed. Further, we envision extending this work for runtime adaptation of the AI solution by having an online search to improve continuously the latency and memory consumption based on the environment state.

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REFERENCES

[1] H. A. Rowley, S. Baluja, and T. Kanade, “Neural network-based face detection,” IEEE Transactions on pattern analysis and machine intelligence, vol. 20, no. 1, pp. 23–38, 1998.
[2] A. Graves, A. r. Mohamed, and G. Hinton, “Speech recognition with deep recurrent neural networks,” in 2013 IEEE international conference on acoustics, speech and signal processing. IEEE, 2013, pp. 6645–6649.
[3] “Google ai,” 2020. [Online]. Available: URL:https://ai.google/
[4] “Tesla.” [Online]. Available: https://www.forbes.com/sites/bernardmarr/2018/01/08/
[5] Y. LeCun, Y. Bengio, and G. Hinton, “Deep learning,” nature, vol. 521, no. 7553, pp. 436–444, 2015.
[6] “Imagenet.” [Online]. Available: http://www.image-net.org.
[7] A. G. Howard, M. Zhu, B. Chen, D. Kalenichenko, W. Wang, T. Weyand, M. Andreetto, and H. Adam, “Mobilenets: Efficient convolutional neural networks for mobile vision applications,” arXiv preprint arXiv:1704.04861, 2017.
[8] F. N. Iandola, S. Han, M. W. Moskewicz, K. Ashraf, W. J. Dally, and K. Keutzer, “Squeezenet: Alexnet-level accuracy with 50x fewer parameters and ¡ 0.5 mb model size,” arXiv preprint arXiv:1602.07360, 2016.
[9] T.-J. Yang, A. Howard, B. Chen, X. Zhang, A. Go, M. Sandler, V. Sze, and H. Adam, “Netadapt: Platform-aware neural network adaptation for mobile applications,” in Proceedings of the European Conference on Computer Vision (ECCV), 2018, pp. 285–300.
[10] B. Wu, X. Dai, P. Zhang, Y. Wang, F. Sun, Y. Wu, Y. Tian, P. Vajda, Y. Jia, and K. Keutzer, “Fnet: Hardware-aware efficient convnet design via differentiable neural architecture search,” in Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition, 2019, pp. 10734–10742.
[11] E. Wang, J. J. Davis, R. Zhao, H.-C. Ng, X. Niu, W. Luk, P. Y. Cheung, and G. A. Constantinides, “Deep neural network approximation for custom hardware: Where we’ve been, where we’re going,” ACM Computing Surveys (CSUR), vol. 52, no. 2, pp. 1–39, 2019.
[12] Y. He, J. Lin, Z. Liu, H. Wang, L.-J. Li, and S. Han, “Amp: Automl for model compression and acceleration on mobile devices,” in Proceedings of the European Conference on Computer Vision (ECCV), 2018, pp. 784–800.
[13] S. Han, H. Mao, and W. J. Dally, “Deep compression: Compressing deep neural networks with pruning, trained quantization and huffman coding,” arXiv preprint arXiv:1510.00149, 2015.
[14] P. Stock, A. Joulion, R. Gribonval, B. Graham, and H. Jégou, “And the bit goes down: Revisiting the quantization of neural networks,” arXiv preprint arXiv:1907.05686, 2019.
[15] A. Anderson, A. Vasudevan, C. Keane, and D. Gregg, “Low-memory gemm-based convolution algorithms for deep neural networks,” arXiv preprint arXiv:1709.03395, 2017.
Convolutions

Direct Convolution vs. Fast Convolution

- Efficient Winograd or Cook-Toom convolution

- Fast implementations on embedded systems:
  - Fft vs direct convolution
  - Openblas

- Effectiveness of fast convolution:
  - pruning
  - quantization
  - mixed-precision

Model Quantization

- Quantized Neural Networks
  - Xnor-Net
  - SqueezeNet
  - MobileNet
  - MobileNetV2

- Mixed-precision
  - TensorRT
  - TFLite

- Parameterized Activation
  - PACT

- Hardware-Aware Quantization
  - Hardware-Aware Accelerator Design

- Learning to Quantize
  - Reinforcement Learning
  - Bayesian Optimization

- Searching for Primitives
  - Neural Architecture Search
  - Evolutionary Algorithms

- Accelerators for AI
  - FPGA-based Accelerators
  - GPP-based Accelerators

- Optimization
  - FPGA-based Accelerator Design

- Performance Evaluation
  - Benchmarking
  - Testing

- Challenges
  - Latency
  - Throughput
  - Energy Efficiency

- Future Directions
  - Hybrid Architectures
  - Neuromorphic Systems

- Conclusion
  - Contributions
  - Limitations
  - Future Work

References

- P. Maji, A. Mundy, G.Dasika, J. Beu, M. Mattina, and R. Mullins, "Efficient Winograd or Cook-Toom Convolution Implementation for Mobile EIPs," arXiv preprint arXiv:1903.01521, 2019.

- K.-S. Oh and K. Jung, "Gpu Implementation of Neural Networks," Pattern Recognition, vol. 37, no. 6, pp. 1311–1314, 2004.

- C. Zhang, P. Li, G. Sun, Y. Guan, B. Xiao, and J. Cong, "Optimizing Fpga-Based Accelerator Design for Deep Convolutional Neural Networks," in Proceedings of the 2015 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, 2015, pp. 161–170.

- R. Andri, L. Cavigelli, D. Rossi, and L. Benini, "Yodann: An Ultra-Low Power Convolutional Neural Network Accelerator Based on Binary Weights," in 2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI). IEEE, 2016, pp. 236–241.

- M. de Prado, J. Su, R. Dahyot, R. Saeed, L. Keller, and N. Vallez, "Ai Pipeline-Bringing Ai to you, End-to-End Integration of Data, Algorithms and Deployment Tools," arXiv preprint arXiv:1901.05049, 2019.

- A. Anderson and D. Gregg, "Optimal Dnn Primitive Selection with Partitioned Boolean Programming," in Proceedings of the 2018 International Symposium on Code Generation and Optimization, 2018, pp. 340–351.

- M. de Prado, M. Denna, L. Benini, and N. Pazos, "Quenn: Quantization Engine for Low-Power Neural Networks," in Proceedings of the 15th ACM International Conference on Computing Frontiers, 2018, pp. 36–44.

- C.-J. Wu, D. Brooks, K. Chen, D. Chen, S. Choudhury, M. Dukhan, K. Hazelowood, E. Isaac, Y. Jia, B. Jia et al., "Machine Learning at Facebook: Understanding Inference at the Edge," in 2019 IEEE International Symposium on High Performance Computer Architecture (HPCA). IEEE, 2019, pp. 331–344.

- M. Sandler, A. Howard, M. Zhu, A. Zhmoginov, and L.-C. Chen, "Mobilenetv2: Inverted residuals and linear bottlenecks," in Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition, 2018, pp. 4510–4520.

- X. Zhang, X. Zhou, M. Lin, and J. Sun, "Shufflenet: An Extremely Efficient Convolutional Neural Network for Mobile Devices," in Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition, 2018, pp. 6848–6856.

- B. Wu, Y. Wang, P. Zhang, Y. Tian, P. Vajda, and K. Keutzer, "Mixed Precision Quantization of Convnets via Differentiable Neural Architecture Search," arXiv preprint arXiv:1812.00900, 2019.

- R. Krishnamoorthi, "Quantizing Deep Convolutional Networks for Efficient Inference: A Whitepaper," arXiv preprint arXiv:1806.08342, 2018.

- R. Zhao, Y. Hu, J. Dotzel, C. De Sa, and Z. Zhang, "Improving Neural Network Quantization Without Retraining Using Outlier Channel Splitting," in International Conference on Machine Learning, 2019, pp. 7543–7552.

- M. Nagel, M. van Baalen, T. Blankoveoott, and M. Wellinger, "Data-Free Quantization Through Weight Equalization and Bias Correction," in Proceedings of the IEEE International Conference on Computer Vision, 2019, pp. 1325–1334.

- "Caffe-Int8-Convert-Tools," 2020. [Online]. Available: https://github.com/BUG1989/caffe-int8-convert-tools

- R. Banner, Y. Nahshan, and D. Soudry, "Post Training 4-Bit Quantization of Convolutional Networks for Rapid Deployment," in Advances in Neural Information Processing Systems, 2019, pp. 7948–7956.

- M. Dukhan, "The indirect convolution algorithm," 2019.

- "Openblas," 2020. [Online]. Available: https://www.openblas.net/

- J. Zhang, F. Franchetti, and T. M. Low, "High performance zero-memory overhead direct convolutions," arXiv preprint arXiv:1809.10170, 2018.

- "Openblas," 2020. [Online]. Available: https://www.openblas.net/
[64] V. Mnih, K. Kavukcuoglu, D. Silver, A. A. Rusu, J. Veness, M. G. Bellemare, A. Graves, M. Riedmiller, A. K. Fidjeland, G. Ostrovski et al., “Human-level control through deep reinforcement learning,” *Nature*, vol. 518, no. 7540, pp. 529–533, 2015.

[65] L.-J. Lin, “Self-improving reactive agents based on reinforcement learning, planning and teaching,” *Machine learning*, vol. 8, no. 3-4, pp. 293–321, 1992.

[66] E. Wiewiora, *Reward Shaping*. Boston, MA: Springer US, 2010, pp. 863–865. [Online]. Available: https://doi.org/10.1007/978-0-387-30164-8_731

[67] Arm Ltd. Cortex-A53. [Online]. Available: https://www.arm.com/products/silicon-ip-cpu/cortex-a/cortex-a53

[68] A. Lal Shimpi. (2012, Oct.) ARM’s Cortex A57 and A53. [Online]. Available: https://www.anandtech.com/show/6420/arms-cortex-a57-and-cortex-a53-the-first-64bit-armv8-cpu-cores

[69] Arm Ltd. Cortex-A57. [Online]. Available: https://www.arm.com/products/silicon-ip-cpu/cortex-a/cortex-a57

[70] A. Frumusanu. (2015, Apr.) ARM Reveals Cortex-A72 Architecture Details. [Online]. Available: https://www.anandtech.com/show/9184/arm-reveals-cortex-a72-architecture-details

[71] B. Jacob, S. Kligys, B. Chen, M. Zhu, M. Tang, A. Howard, H. Adam, and D. Kalenichenko, “Quantization and training of neural networks for efficient integer-arithmetic-only inference,” in *Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition*, 2018, pp. 2704–2713.

[72] J. Andrews. (2017, Dec.) Exploring the Arm dot product instructions. [Online]. Available: https://community.arm.com/developer/tools-software/tools/b/tools-software-ides-blog/posts/exploring-the-arm-dot-product-instructions

[73] N. Stephens. (2019, Sep.) Developments in the Arm A-Profile Architecture: Armv8.6-A. [Online]. Available: https://community.arm.com/developer/ip-products/processors/b/processors-ip-blog/posts/arm-architecture-developments-armv8-6-a

**APPENDIX**

Fig. 14: **Algorithm optimisation.** Speedup of Winograd over GEMM-FP32 for Resnet50’ (the higher, the better).