Accelerating Multigrid-based Hierarchical Scientific Data Refactoring on GPUs

Jieyang Chen, Lipeng Wan, Xin Liang, Ben Whitney, Qing Liu∗, Dave Pugmire, Nicholas Thompson, Matthew Wolf, Todd Munson†, Ian Foster†, Scott Klasky
Oak Ridge National Laboratory, Oak Ridge, TN, USA
∗ New Jersey Institute of Technology, Newark, NJ, USA
† Argonne National Laboratory, Lemont, IL, USA
{chenj3, wanl, liangx, whitneybe, pugmire, thompsonna, wolfmd, klasky}@ornl.gov
qliu@njit.edu {tmunson, foster}@mcs.anl.gov

Abstract—Rapid growth in scientific data and a widening gap between computational speed and I/O bandwidth makes it increasingly infeasible to store and share all data produced by scientific simulations. Multigrid-based hierarchical data refactoring is a class of promising approaches to this problem. These approaches decompose data hierarchically; the decomposed components can then be selectively and intelligently stored or shared, based on their relative importance in the original data. Efficient data refactoring design is one key to making these methods truly useful. In this paper, we describe highly optimized data refactoring kernels on GPU accelerators that are specialized for refactoring scientific data. We demonstrate that our optimized design can achieve 45.42 TB/s aggregated data refactoring throughput when using 4,096 GPUs of the Summit supercomputer. Finally, we showcase our optimized design by applying it to a large-scale scientific visualization workflow and the MGARD lossy compression software.

Index Terms—Multigrid, Data refactoring, GPU

I. INTRODUCTION

With the dawn of the big data era, managing the massive volume of data generated by data-intensive applications becomes extremely challenging, particularly for scientific simulations running on leadership-class high-performance computing (HPC) systems and experiments running on federated instruments and sensor platforms. For instance, the XGC dynamic fusion simulation code [1, 2] from the Department of Energy (DoE)’s Princeton Plasma Physics Laboratory can generate 1 PB of data every 24 hours when running on the DoE’s fastest supercomputers. In the future, these physicists expect that their simulation codes will generate 10 PB of data per day. A more extreme example is the Square Kilometer Array (SKA) radio astronomy project [3], which plans to be generating data at a velocity of 1 PB/s in the next 10 to 20 years. Few storage systems can keep up with data generated at that velocity, including those built for the DoEs leadership-class supercomputers. Moreover, even if full-accuracy data could be stored at these sizes and rates, processing the data with standard multi-pass data analysis routines may consume more computational resources and be more expensive to run than the original generation, leading to significant degradation in overall scientific productivity.

Current solutions for managing this overwhelming amount of complex and heterogeneous scientific data are usually passive and based on “rules of thumb.” For instance, to mitigate the pressure on I/O bandwidth, domain scientists often decide to decimate in time by reducing the frequency of outputting data based on some arbitrary factor (e.g., writing data every 1,000 simulation steps). Although this approach can effectively reduce the amount of data written to the storage system, it increases the potential risk of missing novel scientific discovery, as the data thrown away might contain some important features. Moreover, due to limited capacity, the data cannot reside in fast storage tiers such as parallel file systems forever. Eventually the data must be moved to much slower storage tiers, such as archival storage systems, and purged from fast storage. For example, on the DoE’s Summit supercomputer, data can only be kept on the parallel file system for 90 days before it is either moved to archival storage systems such as HPSS [4] or permanently deleted. Once data is moved to archival storage, it can take weeks or even months for scientists to retrieve the data before they could run their analysis procedures.

There are no universal solutions for addressing all of the technical and domain-specific requirements at such large data sizes. In fact, from the domain scientist’s perspective, having the capability to store a huge amount of data does not necessarily lead to more scientific discoveries. It is common that the most valuable scientific insights come from a small portion of the original data, while the remaining data is less useful. What domain scientists expect is the capability to reduce and reorganize the data intelligently based on their intentions so that: 1) they will not lose any valuable data that contains important features; and 2) they can quickly fetch the needed data when they run their analysis routines. We call such capability intelligent scientific data refactoring. To enable this capability, new algorithms such as multigrid-based hierarchical data refactoring [5-8] have recently been developed by the applied mathematics community.

In this work, we explore how one can apply the capability to refactor datasets into more reasonable sizes while maintaining the fidelity of domain-driven analytics. In particular, multigrid-based hierarchical data refactoring is a class of data refactoring that decomposes the original data into series of prioritization classes, where each class contains a number of coefficients,
called a coefficient class. Approximations to the original data can be reconstructed by selecting a number of coefficient classes based on accuracy requirements. Thus, hierarchical data refactoring gives both the data producers (e.g., scientific simulations) and consumers (e.g., data analysis routines) the flexibility to store, transport, and access data to satisfy space and/or accuracy requirements.

For example, data sharing can be optimized by intelligently moving coefficient classes through multi-tiered-storage systems (e.g., storage systems containing non-volatile memory, magnetic disks, and tapes) and/or networks based on available capacity and bandwidth. Figure 1 shows original simulation data being refactored into five coefficient classes and then shared with data analysis routines via multi-tiered-storage systems and networks. When the accuracy can be estimated based on the number of selected coefficient classes, users can control the accuracy of the reconstructed data while storing and reading the data. For example, based on user-defined accuracy requirements, information encoded in the first four coefficient classes are enough for data analyses later on, so the fifth coefficient class is ignored. Then, the four coefficient classes can be intelligently shared over the storage systems and network based on their size, available bandwidth/capacities, and accuracy requirements from data analysis routines. In the figure, data analysis routine 1 only needs two coefficient classes to achieve the desired accuracy, while routine 2 needs four. The flexibility of choosing a reduced number of coefficient classes gives users the potential to greatly reduce data movement costs.

As great as the benefits of reduction in data movement and management costs may be, if the decomposition and recomposition routines used by data refactoring are expensive then the total process will not show an advantage. However, Graphics Processing Units (GPUs) have shown great potential to speed up scientific computations that fit their streaming execution model, as they offer high parallel computational power with high memory throughput. As the algorithms involved in multigrid-based hierarchical data refactoring are both parallelizable and memory bound, accelerating the routines in data refactoring processes using GPUs is attractive. Furthermore, we have found that GPU-based refactoring also have other benefits for both CPU- and GPU-based scientific applications.

For CPU-based scientific applications, even though the data are originally generated or processed on CPUs, we find that it can be cost-effective to offload the data refactoring workloads to GPUs when they are available, especially given that fast CPU-GPU interconnections such as PCIe and NVLinks are available in modern computing systems. For GPU-based scientific applications, GPU-based refactoring enables those operations to be performed in place on the GPUs, reducing the data movement cost between GPUs and CPUs. Together with emerging technologies such as GPUDirect Storage or GPUDirect RDMA, refactored data can be shared directly among remote GPUs or to/from the storage systems without the added costs of transferring data back to the host memory.

In this work, we focus on accelerating the two major routines, decomposition and recomposition, in multigrid-based data refactoring on GPUs and evaluating the benefit for producer and consumer applications. Although the multigrid-based algorithms are naturally parallelizable, achieving good performance faces the usual dual challenges on GPUs of minimizing the memory footprint and simultaneously improving the memory access efficiency. Specifically, our contributions are as follows:

- We document in §III the first multigrid-based data refactoring routines for modern GPU architectures that can potentially help build systems to reduce I/O pressure for a variety of scientific applications and workflows;
- We design a series of systematic optimizations for multigrid-based data refactoring in three levels: instruction level, kernel level, and program-structure level. Our optimization can balance both minimizing the memory footprint and improving the memory access efficiency, as seen in §III;
- We demonstrate our design by implementing the state-of-the-art non-uniform multi-dimensional multigrid-based data refactoring algorithms of Ainsworth et al. [5–8];
- In §IV we evaluate our designs on both a consumer-class desktop and the Summit supercomputer at Oak Ridge National Laboratory (ORNL) and achieve 110× and 330× speedups compared with the state-of-the-art CPU designs. We achieve 45.42 TB/s throughput using 4096 NVIDIA Tesla V100 GPUs on Summit;
- Finally, in §V we showcase our work using two common scenarios in scientific computing: 1) reducing data movement costs between scientific simulations and in situ visualization applications; and 2) speeding up lossy compression for scientific data.
The Coefficients at grid level
Nodes at grid level

formulated with notations in Table I

missing grid nodes in each iteration. If we use functions to fashion, with a global correction to account for the impact of scientific computations. These algorithms support nonuniformly-spaced structured multidimensional data, which are commonly found in GPUs. These algorithms support nonuniformly-spaced structured multidimensional data, which are commonly found in GPUs.

II. BACKGROUND: MULTIGRID-BASED HIERARCHICAL DATA REFACTO RING

We use the algorithms of Ainsworth et al. [5] to demonstrate our optimizations for multigrid-based data refactoring on GPUs. These algorithms support nonuniformly-spaced structured multidimensional data, which are commonly found in scientific computations.

These multigrid methods use hierarchical representations to approximate data. Specifically, they decompose data from fine grid representation to coarse grid representation in an iterative fashion, with a global correction to account for the impact of missing grid nodes in each iteration. If we use functions to represent the discrete values continuously, the decomposition from a fine grid level \( l \) to a coarser grid level \( l - 1 \) can be formulated with notations in Table I as follows,

\[
Q_{l-1}u = Q_lu - (I - \Pi_{l-1})Q_lu + (Q_{l-1}u - \Pi_{l-1}Q_lu)
\]

where \( u \) is the piecewise linear function that takes the same values as original data for each node, \( Q_{l-1}u \) and \( Q_lu \) are the function approximations of \( u \) at levels \( l - 1 \) and \( l \), respectively, \( (I - \Pi_{l-1})Q_lu \) is the difference between the values of the fine grid nodes at level \( l \) and their corresponding piecewise linear approximation, and \( (Q_{l-1}u - \Pi_{l-1}Q_lu) \) is the global correction. According to Eq. (1), two major steps are involved at each level of the multigrid decomposition: 1) compute coefficients for the current multigrid level \( l \); and 2) compute global correction and add it to the nodes in the next coarse grid (level \( l - 1 \)). In what follows, we introduce how to compute coefficients and corrections in details.

1) Compute coefficients: Mathematically, the coefficients store the difference between the data approximated by the nodes at level \( l \) (i.e., \( N_l \)) and \( l - 1 \) (i.e., \( N_{l-1} \)) before corrections are added. Since \( N_{l-1} \) is also contained in \( N_l \) and they have the same value for nodes in \( N_{l-1} \) for both levels, the nonzero differences only occur on nodes in \( N_l \setminus N_{l-1}. \) Figure 2 shows how coefficients are calculated along one dimension through linear interpolation. It can be generalized to multi-dimensional cases easily by using multi-linear interpolations for approximation.

2) Compute correction: As proven in [5], the correction is the orthogonal projection of the calculated coefficients at grid level \( l \) onto \( V_{l-1} \), so adding correction to the next coarse grid can better approximate data in current grid. To explain, we first define \( z_{l-1} \) as the correction for grid at level \( l - 1 \). According to Eq. (1) we have the observation that:

\[
z_{l-1} - (I - \Pi_{l-1})Q_lu = -(Q_l - Q_{l-1})u \in V_{l-1}^\perp
\]

Overall process of decomposition and recomposition: We demonstrate this process of decomposing and recomposing using a 5x5 2D data in Figure 3. The left-hand-side represents the full, original data set, while the right-hand-side is the refactored representation. The decomposition process moves from left to right along the top in the figure (i.e., finest grid to coarsest grid). There are four steps to be carried out, the coefficient and correction operations (II.1 and II.2) for each of the two levels. For multi-dimensional data, the computation of correction is done by working on each dimension in a prescribed order. For the 2D data in our example, the calculation proceeds along the rows first and then the columns. We will future explain this in Algorithm 3. The recomposition

### Table I: Notation in Algorithms and Formulations

| Symbol | Description |
|--------|-------------|
| \( u \) | Function represented by the original data. |
| \( N_l \) | Nodes at grid level \( l \). |
| \( C_l \) | Coefficients at grid level \( l \). |
| \( V_l \) | Function space with respect to \( N_l \). |
| \( Q_l \) | The \( L^2 \) projection onto \( V_l \). |
| \( \Pi_l \) | The piecewise linear interpolant in space \( V_l \). |
process moves from the right to the left along the bottom in the figure (i.e., coarsest grid to finest grid). Similar to decomposition, there are four total stages, but they occur in the reverse order. First, the corrections are calculated using coefficients and used to undo the corrections (i.e., subtract values) on the next coarser grid to restore their nodal values. Then, the coefficients are restored back to their original values by adding the interpolated values from the next coarser grid.

III. DESIGNING GPU-ACCELERATED DATA REFACTORIZING

We now discuss the design details of our GPU-accelerated multigrid-based hierarchical data refactoring. We first focus on the optimizations for each computing kernels involved in both the decomposition and recomposition processes. We classify the computing kernels into two categories and propose two optimized frameworks that can help optimize the two kinds of kernels on GPUs. Following the kernel-level optimization, we discuss optimizations to help each of the kernels efficiently work together so that their performance can be maximized. Finally, we discuss design details about how to efficiently use these kernels to build data refactoring tools for multidimensional data.

A. Designing optimized GPU multigrid kernels

There are five major computing kernels involved in the decomposition and recomposition process: 1) computing coefficients; 2) restore from coefficients; 3) mass matrix multiplication; 4) transfer matrix multiplication; and 5) correction solver. Based on their computation pattern, we can classify them into two categories: grid processing kernels and linear processing kernels. So, instead of designing optimizations for each kernel individually, we choose to optimize them by their type. The goal is to define optimizations for each processing type that generally work for each kernel belonging to that type. To accomplish our goal, we design optimized frameworks for the two processing types. A framework in our context is a design template of the computing kernel for a specific type. To actually design a computing kernel, we can follow the template to outline the general structure of the kernel and incorporate computing logics (e.g., call device functions) that are specific to the operations that kernel focuses on. One major benefit to designing each kernel this way is that optimizations for the common overall structure of the kernel can be separated from the specific computing logic of each kernel. We first focus on designing kernel frameworks. The major challenge when designing optimized multigrid kernels is balancing efficient parallelism and memory footprint, as sometimes optimal designs for each metric are not compatible. For example, out-of-place processing usually bring better parallelism, but can cause a larger memory footprint. We develop balanced designs that can help achieve high performance with low memory footprint.

1) Grid processing framework: Two operations directly related to coefficients are computing coefficients and restoring the original nodal values using coefficients. The former is used in decomposition and the latter is used in recompositions. Although they have opposite effects, they share similar computational patterns. We focus on the design of a grid processing kernel framework that can be applied to both kernels. Grid processing has the following characteristics:

- The computation is usually applied to the whole grid at a time;
- A subset of nodes are used to update the nodal value of a disjoint subset of nodes in the grid;
- Each update operation (e.g., interpolation) can be performed independently without dependencies, and operations can be different from each other;
- The results need to be stored in-place.

The main calculation is to compute the interpolation at nodes in \( N_i \setminus N_{i-1} \) using nodal values in \( N_i \). The parallelization can favor either interpolation operations (i.e., parallelism \( \propto O(N_{i-1}) \)) or accessing nodal values (i.e., parallelism \( \propto O(N_i) \)). The former can lead to less thread divergence, while the latter can achieve higher memory access efficiency. The computation of coefficients is a memory bound operation as it needs to access \( N_i \) nodes with a total of \( N_{i-1} \) calculations (the total number of operations involving each node in \( N_{i-1} \) is \( O(1) \)). Therefore, it is essential to optimize in favor of memory access efficiency instead of computation. Thus, we choose to parallelize against the total number of memory accesses instead of the number of operations. Figure 4 shows the grid processing framework. As nodes in \( N_i \) need to be shared...
among several neighbors during interpolation operations, we let each thread block coordinate work on a 3D block of data (or 2D block for 2D data) and use shared memory as a scratch space. We organize threads such that threads in the same warp load values that are consecutive in memory to achieve efficient coalesced memory access patterns. For computing, it is easy to have thread divergence if we assign threads to work on interpolation the way we load nodal values, since interpolation operations that are close to each other are likely to be different. Although choosing large block sizes can reduce thread divergence, it may cause the total number of threads to exceed the maximum allowed on a streaming multiprocessor (SM) or make the SM underutilized. Therefore, we apply a thread re-assignment strategy that assigns threads in the same warp to compute the same interpolation type in the same direction to achieve divergence-free execution. Algorithm 1 shows how we calculate the thread-interpolation operation assignments that can eliminate thread divergence.

Algorithm 1: Calculate assignments between threads and interpolation operations

1 Function InterpolationThreadAssignment (b):
2     x, y, z ← Thread local indexes within thread block;
3     lane_id, wrap_id ← x, y, z;
4     \( P \leftarrow \frac{WARP\_SIZE}{(2^b-1)^3} \) /* Number of warp(s) per interpolation type */
5     \( P_{id} \leftarrow (\text{wrap}_id \% P) \times WARP\_SIZE + \text{lane}_id; \)
6     \( wx \leftarrow P_{id} \% 2^{b-1}; \)
7     \( wy \leftarrow P_{id}/(2^{b-1}) \% 2^{b-1}; \)
8     \( wz \leftarrow P_{id}/(2^{b-1})^{2}\% 2^{b-1}; \)
9     return
10 Function SelectInterpolation(wrap_id, wx, wy, wz, Type_id):
11     if \( \text{wrap}_id/P = \text{Type}_id \) then
12         InterpolationOperation(wx, wy, wz);
13     return

2) Linear processing kernel framework: Three steps directly related to the calculation of corrections require linear processing: mass matrix multiplication, transfer matrix multiplication, and correction solver. Linear processing has the following characteristics:

- When applied to multi-dimensional data, this kind of operation can be sequentially applied one dimension at a time until all dimensions have been applied;
- When applying to each dimension, the operation needs to be individually applied to each vector along that dimension that consists of nodes in the current grid level;
- When applying to a vector, the calculation on each node depends on neighboring nodes so that they have to be processed in a certain order;
- The results need to be stored in-place.

Similar to the calculation of coefficients, we consider optimizing both the parallelism and the memory footprint in a balanced way. There are two straightforward ways to parallelize the task at two different granularities: vector-wise and element-wise. Vector-wise parallelism is achieved by assigning the workload related to different vectors to different threads. Element-wise parallelism is achieved by assigning calculations related to different vector elements to different threads. However, neither of them satisfies our need for a balanced design. Vector-wise parallelism brings no extra memory footprint but it would suffer from low parallelism for small grids. Element-wise parallelism can exploit maximum parallelism but it brings a 100% extra memory footprint due to data dependencies.

Hence, we develop a novel linear processing algorithm that balances both minimizing extra memory footprint and maximizing parallel efficiency. We first parallelize the vectors by assigning a batch to a thread block. Since the update of each node depends on its neighboring elements, we use shared memory as scratch space to avoid polluting the un-processed nodes. Specifically, we let each thread block iteratively work on a segment of coefficient vectors at a time until the whole coefficient vector is updated. Thus, as shown in Figure 6 during the computation we divide the coefficients in the vectors into six regions: 1) the processed region stores updated coefficients (gray dots); 2) the main region consists of coefficients that the current iteration is working on (green dots); 3) and 4) due to dependence on the neighboring coefficients, the original value of coefficients in the two ghost regions (red and cyan dots) are needed to update the coefficients in the main region; 5) for better streaming processor utilization, we prefetch coefficients needed for the next iteration (purple dots); and 6) we mark the unprocessed region as block dots. The regions move forward as the computation proceeds. One challenge to design the algorithm is to simultaneously consider maximizing coalesced global memory access patterns, minimize bank conflict in accessing shared memory, and minimize thread divergence. We use a dynamic coefficient-thread assignment strategy \([9,10]\) so that both the accessing and computation of coefficients are optimized. Figure 5 shows the structure of the algorithms we use to implement our linear processing framework kernels based on the above requirements.
Fig. 5: Skeleton linear processing framework for design three correction calculation related kernels in decomposition and recomposition.

Fig. 6: Mass matrix multiplication designed following linear processing framework. The node vectors are partitioned into six regions during processing.

Algorithm 2: Mass matrix multiplication

```
Function MassMult(Ni, SMain, Rghost1, Sghost2):
    h1 ← spacing(Ni[y−1], Ni[y]);
    h2 ← spacing(Ni[y], Ni[y+1]);
    h3 ← h1 + h2;
    t: holding temporary thread local result;
    if y == 0 then
        t ← h1 * rghost1 + 2 * h3 * SMain[x, y] + h2 * SMain[x+1, y];
    else if y == 2^l−1 then
        t ← h1 * SMain[x−1, y] + 2 * h3 * SMain[x, y] + h2 * Sghost2[x+1, y];
    else
        t ← h1 * SMain[x−1, y] + 2 * h3 * SMain[x, y] + h2 * SMain[x+1, y];
    end
    SMain[x, y] ← t;
End
```

B. Designing kernels based on frameworks

To show how to design optimized kernels using grid and linear processing framework, we use mass matrix multiplication kernel as an example (other kernels have similar structure so they are omitted due to page space limit). Algorithms 2 shows the mass matrix multiplication plug-in device function for the linear processing framework. We can see by using our optimized processing frameworks, we can decouple the design of logic of specific operations from handling memory accesses, while at the same time maintaining high parallelism and memory access efficiency. Also, by using the framework, we minimize the extra memory footprint needed for each kernel. First of all, there is no extra memory footprint for computing coefficients and restoring kernel that uses grid processing framework. Also, there is no extra memory footprint for two of the three kernels that use linear processing framework: mass matrix multiplication and transfer matrix multiplication. This is because our linear processing framework naturally avoids adding extra memory and for the mass and transfer matrices we store the matrix elements implicitly by computing in demand. The solve correction kernel needs an extra \( O(2^l+1) \) memory space per dimension, as the elements in updated main diagonal cannot be efficiently computed during the backward substitution process. This kernel still requires minimum extra memory. For example, with a 100×100×100 grid, the extra memory footprint is only about 0.3%.

C. Handling strided memory accesses in grids

For GPU memory, strided memory accesses decrease the memory access efficiency by a factor of the stride length. Since multigrid-based data refactoring routines are memory bound, maintaining high memory access efficiency is especially important for overall performance. There are two kinds of strided memory accesses in the decomposition and recomposition routines. The first is caused by the nature of the linear storage pattern in memory. Only consecutive nodes in the leading dimension are stored in consecutive memory addresses. When working on consecutive nodes in other dimension, it would lead to strided memory accesses. The second is caused by the nature of the multigrid structure. As mentioned before there are \((2^l+1) \times (2^l+1) \times (2^l+1)\) nodes in the grid at level \( l \) during decomposition or recomposition. Therefore, each node is \( 2^{L−l} \) steps away for its neighboring nodes in each dimension. When working on the grid with a level smaller than \( L \) (finest grid), accessing consecutive nodes in the grid would lead to strided memory accesses. The stride length increases exponentially as it equals to \( 2^{L−l} \).

To minimize strided memory accesses, we apply two optimization techniques. The first kind of strided memory access can impact both grid and linear processing kernels. We pack the nodes specific to a level of the grid in the working memory space to make the stride always equal to one. For the correction calculation, since there is working memory space for storing intermediate results (will be explained in detail in the next section), we can pack nodes in the working memory space. For coefficient related calculations, we can reuse the working memory space for the correction calculation for node packing.
The memory space needed for packing nodes will be no larger than memory used for storing intermediate results for the correction calculation; it brings no extra memory footprint. The second kind of strided memory access can mainly impact linear processing kernels, as we can easily adjust the thread block size of the grid processing kernels to minimize the impact. In the case of 3D grids, strided memory accesses occur only when processing vectors along the second or third dimension. Due to our compute-access decoupled design, our linear processing framework can be easily adapted to avoid strided memory accesses when processing on the second or third dimension. The key idea is to always batch vector processing on the x-y plane for the second dimension and the x-z plane for the third dimension. Due to space limitation, the detailed design of this framework is omitted.

D. Overall algorithms

Algorithm 3 shows how we use our optimized kernels to build data refactoring routines for multi-dimensional data on GPUs. For each level, the computed coefficients are also used for calculate corrections. This process involves altering the values of coefficients. So, to preserve the value of previously computed coefficients, the correction is computed in a working memory space. Specifically, during decomposition the computed coefficients is copied from working memory space to input/output memory space (line 5) before they are used for computing global corrections (line 6-10). Similarly, during recomposition the coefficients are first loaded to working memory space (line 16) for correction calculation (line 17-21), so that they will not be corrupted when used to restore current level nodal values (line 25). The size of working memory space is equal to the original input size, which is the same for original CPU design [11] and our GPU design. In this work, we propose three kinds of optimization specifically for our GPU design: 1) As mentioned in Section III.B, we use the working memory space to pack nodes in a more condensed way to achieve better memory access efficiency for correction calculation without bringing extra memory footprint compared with the CPU design. The operation of packing and unpacking nodes are fused with node copy, applying corrections, undo corrections operations as marked in Algorithm 3. 2) When the working memory space is not used by correction calculation, we use the space to improve the memory access efficiency of coefficient calculation. Since coefficient calculation and correction calculation have to be done in order, they will not cause conflicts when sharing the same working memory space. 3) For linear processing kernels in correction calculations, we use the 2D design to build both 2D and 3D data refactoring routines since correction calculations can be done by calculating along each dimension at a time as mentioned in Section III. When working on 3D input, limited by the GPU memory space, each 2D slice of the data is usually much smaller compared with 2D input, so it is anticipated those 2D linear processing kernel would cause GPU under-utilization. As processing different 2D slices for 3D input can be performed independently, we use CUDA streams to improve GPU utilization. This allows multiple 2D slices to be processed at the same time when there are enough GPU resources.

IV. EXPERIMENTAL EVALUATION

We evaluate our work on two GPU-enabled platforms. One is a GPU-accelerated desktop with an NVIDIA RTX 2080 Ti GPU with 11 GB of memory and one 8-core Intel i7-9700K CPU with 32 GB of memory. The other is the Summit supercomputer at ORNL. Each node on Summit is equipped with 6 NVIDIA Tesla V100 GPUs with 16 GB memory on each GPU and two 22-core IBM POWER9 CPUs with 512 GB memory.

In our evaluation, we use datasets generated from the Gray-Scott Reaction-Diffusion simulation [12][13]. Each node in the input grid data is represented as double precision floating

2 Only 21 cores/socket are accessible for computation.
point numbers. Note that our data refactoring algorithms have deterministic computation time complexity regardless of the values in the chosen dataset, so it will yield the same performance for any datasets at have the same dimensions and size. We configure the simulation codes to generate 3D data so that each dimension is in the form of $2^L + 1$, where $L$ is an positive integer and is not necessary the same for all dimensions. If at least of one dimension is not in this form, one extra pre-processing step and the corresponding post-processing step are necessary, which consist of one iteration of special decomposition and recomposition. Since the extra one iteration for pre-processing and post-processing contributes a small portion of the total execution time, in order to better show the results of our optimizations on the main decomposition/recomposition loop we avoid those step in our tests by generating data with dimensions that follows the form of $2^L + 1$. To simplify, we let each dimension to have the same length. The 2D datasets are obtained from taking 2D slices of the 3D datasets.

In our experiments, we use the CPU-based multigrid-based data refactoring implementations integrated in the MGARD lossy compression software [11] as our baseline.

A. Evaluation at kernel level

We first show the performance improvement we achieve from accelerating several major kernels in multigrid-based data refactoring on GPUs. Table III and IV show the maximum, minimum, and average performance improvement on the Summit supercomputer and the GPU-accelerated desktop. Note that since computing coefficients and restoring from coefficients are almost exactly the same computation pattern except minor operations, we only show the performance of computing coefficients in our evaluation. We can see that since the computing coefficients, mass matrix multiplication, and transfer matrix multiplication tend to be easily parallelizable, they achieve considerable performance improvement compared with serial CPU implementations. Solving corrections is naturally less parallelizable, so it is expected to have less improvements. Comparing 2D and 3D, since the three kernels used for calculating the correction in 2D data are reused for 3D, the only kernel unique to 3D is the computation of coefficients. It is anticipated to see the speedup for the 3D case to be lower than for the 2D case because each thread block for calculating the 3D coefficients has much longer latency due to the interpolation on one extra dimension and fewer concurrent thread blocks due to the high thread block resource usage. Another factor limiting the maximum speedup for the 3D case is that available GPU memory prohibits us from testing on larger data sizes that can leads to similar parallelism compared with 2D.

As our linear processing framework involves complicated designs, we study the mass matrix multiplication kernel designed following the framework to show how our optimization impacts performance. Figure 7 shows the memory throughput of mass matrix multiplication as different optimizations are applied. Specifically, we show the performance of mass matrix multiplication kernel when decomposing a $4097 \times 4097$ grid of input data, which needs 12 levels of decomposition. We can see the original serial CPU version suffers from degraded performance due to inefficient memory access when grid spacing is large (level is small). This is also the case for the naive GPU design. The naive GPU design parallelizes the workload vector-wise [14] without applying memory access efficiency optimizations proposed in this work. When mass multiplication kernel are designed following our linear processing framework we can see it can achieve much better performance and can sustain similar performance when grid spacing is large (i.e., $l$ is small) and only degrades on small grids, which bring minor impacts to the overall performance.

Fig. 7: Using mass matrix multiplication to show how much performance can be improved by designing kernels following our linear processing framework (evaluated on a single NVIDIA Tesla V100 GPU on Summit)

TABLE III: Performance improvement of four major kernels on different grids sizes (GPU vs. serial CPU on Summit@ORNL)

| Grid Size | Kernel          | Max       | Min       | Avg       |
|-----------|-----------------|-----------|-----------|-----------|
| $5^2$     | Comp. Coefficients | 158.88x   | 7.66x     | 64.00x    |
| $5^2-513$ | Comp. Coefficients | 774.97x   | 47.07x    | 316.76x   |
| $5^2-8193$| Mass Matrix Mult.| 2405.83x  | 219.42x   | 1154.65x  |
| $5^2-8193$| Trans. Matrix Mult.| 791.32x  | 51.13x    | 406.82x   |
| $5^2-8193$| Solve Correction | 506.46x   | 77.52x    | 317.01x   |

TABLE IV: Speedups of four major kernels on different grids sizes (GPU vs. serial CPU on GPU-accelerated desktop)

| Grid Size | Kernel          | Max       | Min       | Avg       |
|-----------|-----------------|-----------|-----------|-----------|
| $5^2$     | Comp. Coefficients | 440.04x   | 9.95x     | 189.04x   |
| $5^2$     | Comp. Coefficients | 2919.47x  | 61.08x    | 1045.16x  |
| $5^2$     | Mass Matrix Mult.| 2141.62x  | 203.89x   | 1139.05x  |
| $5^2$     | Trans. Matrix Mult.| 1949.72x | 166.81x   | 950.46x   |
| $5^2$     | Solve Correction | 729.72x   | 154.20x   | 250.04x   |

B. Evaluation on overall data refactoring routines

1) Overall time breakdown: To show the absolute time taken by each kernel and how much each of them contributes to the overall time, we profiled the end-to-end time breakdown for both decomposition and recomposition on both 2D and 3D data on CPU and GPU as shown in Table IV. We can see that besides the major kernels we have focused on, other operations such as memory copies also take considerable time. For example, memory copies take about 23.2%-40.1% of the total time on CPU. The memory copy is part of the
algorithm used to copy computed coefficients and the derived correction in and out from the scratch memory space and they cannot be avoided. This is also true for GPU implementation, but we are able to take advantage of the scratch memory to optimize memory access efficiency for each kernel. For example, by packing nodes in a more condensed way onto the scratch memory, it enables much greater performance gain for computing kernels.

2) Optimizing resource utilization for 3D data: Next, we evaluate the optimizations specialized for 3D data. We parallelize the 2D kernels against the third dimension through the use of CUDA streams that range from one stream (baseline) to 64 CUDA streams. We show the speedups of using different numbers of streams compared with using one stream with the largest possible data size $513 \times 513 \times 513$ on one NVIDIA Tesla V100 GPU on a Summit computing node. As shown in Figure 8 up to $2.6 \times$ and $3.2 \times$ speedups are achieved by using eight CUDA streams for data decomposition and recomposition.

3) Single node performance: Table VI also shows the overall performance improvement achieved using one GPU compared with one CPU core on our GPU-accelerated desktop and the Summit supercomputer. On the GPU-accelerated desktop, our designs achieve up to $102.31 \times$ and $116.52 \times$ performance improvement for decomposition and recomposition on 2D data. For 3D data, our designs achieve up to $64.03 \times$ and $91.13 \times$ performance improvement for decomposition and recomposition. On Summit, our designs achieve up to $311.18 \times$ and $330.76 \times$ speedup for decomposition and recomposition on 2D data, respectively. For 3D data, our designs achieve up to $103.41 \times$ and $135.92 \times$ performance improvement for decomposition and recomposition. We also show the extra memory footprint used by our GPU optimization compared with the original CPU designs. We can see our designs only bring equal or less than $6\%$ extra memory footprint for small-sized inputs and less than $1\%$ extra memory footprint for large inputs.

4) Multi-node performance: To show the potential of using GPU-accelerated data refactoring in large-scale scientific applications, we conduct weak scaling test on Summit. For large-scale parallelization, we choose to parallelize the workload by assigning each GPU an equal sized data partition and do decomposition and recomposition independently. Due to the nature of multigrid-based data refactoring, parallelizing the workload this way brings great large-scale performance with negligible impact on decomposition and recomposition results. We assign each GPU to one MPI process and do GPU-based data refactoring on 1 GB of simulation data. We scale the number of processes (GPUs) up to 4096 in our tests with 4 GPUs per computing node on Summit. As shown in Figure 9 with 4096 GPUs we achieve $45.42 \text{ TB/s}$ and $40.45 \text{ TB/s}$ aggregated throughput for decomposition and recomposition for 2D, respectively; for 3D data, the corresponding numbers are $17.78 \text{ TB/s}$ and $19.86 \text{ TB/s}$. These numbers show great potential in speeding up data refactoring-based I/O operations, especially when used in combination with emerging new technologies that help move data in or out of the GPU efficiently, such as GPU-CPU NVLink and GPUDirect Storage.

V. SHOWCASE

Data refactoring algorithms were designed to offer much greater flexibility when managing large scientific data than the traditional methods. With well-designed data management, data can be shared between scientific applications more intelligently with a large reduction in I/O costs. However, inefficient data refactoring routines can diminish the benefits brought by data refactoring itself. Here we use two examples to show the benefits of GPU-based data refactoring over the CPU designs.

A. Visualization workflow

First we show how our GPU optimizations can make data refactoring effective when used for I/O cost reduction in scientific workflows that rely on file-based data sharing. Figure 10 shows the cost of writing and reading a 4 TB simulation data file using 4096 and 512 processes using the state-of-the-art ADIOS I/O library [15] on Summit with GPU-accelerated data refactoring enabled. By writing or reading fewer coefficient classes, we can see immediate cost reduction in file write and read. When our efficient GPU-accelerated data refactoring is used, we can see this reduction in the cost of file write and read can be effectively translated into a reduction in the total I/O cost. Although multigrid-based data refactoring allows us to encode the most important information in the data with a few coefficient classes, it would not reduce the total I/O cost unless those coefficient classes can be efficiently computed or used for data recovery. For example, in our experiments we achieve $\sim 95\%$ accuracy for a chosen feature in the visualization result (i.e., the total area of the iso-surfaces) with only three out of ten coefficient classes. This can be effectively translated into $\sim 66\%$ I/O cost reduction.

B. Lossy compression

Multigrid-based hierarchical data refactoring can also be used as a preconditioner in scientific lossy compression software. As one of the key components in lossy compression workflows, it is important to have efficient data refactoring in order to make fast lossy compression possible. We showcase how our GPU-accelerated data refactoring can help improve the performance of lossy compression workflows in the MGARD lossy compression software. MGARD is a CPU-based lossy compressor with three components in its workflow: multigrid-based data refactoring, quantization, and entropy encoding. Figure 11 show the time breakdown of the each component in MGARD [11] when data refactoring remains on the CPU (left bars) or is off-loaded to the GPU (right bars). In our test, besides the data refactoring process, we also off-load the quantization and de-quantization processes to the GPUs, since it can help reduce the CPU-GPU data transfer cost. The entropy encoding stage (ZLib lossless compression) is kept on the CPU. We can see our GPU-accelerated data refactoring can greatly reduce the overall execution time of the lossy compression workflows.
TABLE IV: Time breakdown for data refactoring routines running on single CPU and GPU on Summit

| Dims. | Ops. | 2D: (513 x 513 x 513) | 3D: (513 x 32772) |
|-------|------|------------------------|------------------|
|       | Serial CPU | GPU | Serial CPU | GPU | Serial CPU | GPU | Serial CPU | GPU |
|       | Time(s) | % Total | Time(s) | % Total | Time(s) | % Total | Time(s) | % Total |
| CC    | 2.30 | 16.0% | 5.37 | 1.4% | 1.92 | 0.3% | 3.83 | 0.7% |
| MM    | 2.10 | 20.9% | 4.44 | 11.2% | 2.57 | 11.0% | 5.43 | 10.1% |
| TM    | 2.87 | 19.1% | 4.95 | 10.2% | 2.87 | 16.0% | 4.99 | 9.2% |
| SC    | 2.64 | 17.5% | 1.66 | 33.6% | 2.64 | 14.7% | 1.66 | 30.7% |
| MC    | 3.90 | 25.9% | 5.55 | 11.5% | 6.68 | 40.1% | 4.83 | 19.8% |

CC: Calculation of coefficients; MM: Mass matrix multiplication; TM: Transfer matrix multiplication; SC: Solve for corrections; MC: Memory copy; PN: Packing nodes

TABLE V: Performance improvement using one GPU vs. one CPU core

| Dims. | Input | GPU-accel. desktop | Summit@ORNL | Extra Mem. | Footprint* |
|-------|-------|---------------------|-------------|------------|------------|
| 2D    | 33^2  | 0.40x | 0.39x | 0.30x | 0.30x | 6.06% |
|       | 65^2  | 1.00x | 0.92x | 0.79x | 0.87x | 3.08% |
|       | 129^2 | 2.35x | 2.54x | 2.29x | 2.29x | 1.53% |
|       | 257^2 | 6.39x | 6.41x | 6.80x | 6.83x | 0.78% |
|       | 513^2 | 16.08x | 15.22x | 19.46x | 20.13x | 0.39% |
|       | 1025^2 | 31.26x | 33.21x | 50.19x | 51.05x | 0.20% |
|       | 2049^2 | 57.94x | 64.92x | 108.77x | 110.92x | 0.10% |
|       | 4097^2 | 85.40x | 97.29x | 217.97x | 219.77x | 0.05% |
|       | 8193^2 | 102.31x | 116.32x | 311.18x | 320.76x | 0.02% |

| 3D    | 33^3  | 2.08x | 2.61x | 1.14x | 1.33x | 0.28% |
|       | 65^3  | 7.59x | 9.57x | 4.03x | 4.83x | 0.07% |
|       | 129^3 | 20.11x | 24.41x | 16.20x | 19.13x | 0.02% |
|       | 257^3 | 36.95x | 54.07x | 52.96x | 65.22x | 0.05% |
|       | 513^3 | 84.03x | 97.13x | 103.41x | 135.92x | 0.01% |

*Extra memory footprint compared with the original CPU design.

TABLE VI: Performance improvement using all GPUs vs. all CPU cores on the desktop and one computing node on Summit

| Dims. | Ops. | 2D: (513 x 513 x 513) | 3D: (513 x 32772) |
|-------|------|------------------------|------------------|
|       | Serial CPU | GPU | Serial CPU | GPU | Serial CPU | GPU | Serial CPU | GPU |
|       | Time(s) | % Total | Time(s) | % Total | Time(s) | % Total | Time(s) | % Total |
| CC    | 4.36 | 17.0% | 2.99e-2 | 4.7% | 3.60 | 18.6% | 5.91e-2 | 8.4% |
| MM    | 5.63 | 21.9% | 5.99e-2 | 9.3% | 3.70 | 18.6% | 5.91e-2 | 8.4% |
| TM    | 5.18 | 20.1% | 7.02e-2 | 11.1% | 5.23 | 17.0% | 7.20e-2 | 10.1% |
| SC    | 4.55 | 17.3% | 3.18e-1 | 50.4% | 4.61 | 15.0% | 3.22e-1 | 45.0% |
| MC    | 5.98 | 23.8% | 6.75e-1 | 1.1% | 8.37 | 34.3% | 6.21e-1 | 1.9% |

Related Works

In this section, we present a brief survey of existing literature that focuses on optimizing multigrid methods for GPU architectures.

Multigrid methods are effective solvers commonly used for a wide range of problems in numerical analysis. In order to improve the computing efficiency of multigrid methods, many existing studies attempt to design new parallel algorithms for multigrid methods to take advantage of GPUs’ capability to do massively parallel operations. Particularly, these algorithms need to expose sufficient fine-grained parallelism that can be properly mapped to the GPU architectures. For example, a parallel algebraic multigrid method is developed in [16], which targets GPU devices and exposes substantial fine-grained parallelism in both the construction of the multigrid hierarchy and the cycling or solve stage. Similarly, [17] shows that it is possible to significantly accelerate algebraic multigrid methods on GPUs by carefully selecting algorithms with sufficient fine-grained parallelism. By combining graph coloring and greedy maximal independent set computations, [18] significantly improves the performance of a 3D unstructured geometric multigrid solver. In [19], a multi-GPU implementation of Krylov subspace methods with algebraic multi-grid preconditioners is proposed, which preserves the effects of fine-grained parallelism with shared memory on the GPU, while distributing data across multiple GPUs with minimal communication. To accelerate lattice QCD multigrid on GPUs, [20] leverages all sources of parallelism that the underlying stencil problem possesses to achieve high efficiency even for the coarsest of grids.

There are some studies that focus on evaluating and optimizing the implementation of parallel multigrid algorithms for...
GPU architectures from a software engineering perspective. For instance, [21] analyzes the performance of an optimized GPU-based implementation of the geometric multigrid method on different state-of-the-art NVIDIA GPUs. Similar work also includes [22–26]. [27] takes portability into account and provides a unified user interface so that optimized multigrid solvers can run on diverse platforms including multicore CPUs and GPUs. Similarly, [28] studies a variety of optimization techniques for geometric multigrid on different multi- and many-core processors. In [14], a compiler-based auto-tuning framework is studied which delivers performance portability across CPU- and GPU-accelerated platforms for the geometric multigrid linear solvers found in many scientific applications. A library called AmgX is designed and implemented in [29], which provides drop-in GPU acceleration of distributed algebraic multigrid and preconditioned iterative methods. In [30], a classical algebraic multigrid solver and a smoothed aggregation algebraic multigrid solver are implemented on NVIDIA GPUs. [31] presents a CUDA implementation of the parallel multigrid solver for linear complementary problems. Besides CUDA, multigrid solvers implemented using OpenCL are also proposed, such as the implementation for a multigrid gradient vector flow computation presented by [32].

Comparing with existing multigrid solvers, the data refactoring approach that we aim to optimize in this work share similar settings such as multiple interlocking grids structure. However, the multigrid-based data refactoring is designed and optimized targeting a different goal compared with multigrid solvers. Multigrid solvers aim to accelerate the processing of solving linear systems while multigrid-based data refactoring approach aims to reconstruct the scientific data progressively with hierarchical representations. This leads to two fundamental differences that make existing optimizations hard to be applied to our work: 1) although some operations in data refactoring are similar to the ones in multigrid solvers, the operations in data refactoring are composed in a unique way; 2) the correction in this work is designed specifically for the orthogonal projection in data refactoring, while the correction in multigrid solvers is used to generate the fine grid solution. In addition, our optimizations are proposed specifically for handling large-volume scientific data, which means we need to consider not only limited GPU memory but also cases where refactoring process can share resources with original scientific computations on GPUs. So, it is essential to optimize for low memory footprint. As performance is also important, we need optimizations that balance both parallelism and memory footprint. Although part of the kernels used in data refactoring share similar computation patterns as the ones used in multigrid solvers, it is challenging to directly leverage existing works to achieve good parallelism and memory footprint balance when used in data refactoring. For example, [14] only uses vector-wise parallelism without inplace update, which can cause lower performance with large memory footprint for our data refactoring. We observe this performance degradation in our test as shown in Figure 7.

VII. CONCLUSION

As I/O becomes one of the major performance bottleneck for scientific computing, data refactoring shows great potential to reduce I/O costs. In this work, we used GPUs to accelerate multigrid-based hierarchical data refactoring for scientific data using highly optimized data refactoring kernels.
specialized for scientific data refactoring. We evaluated our designs on two platforms including the world leadership-class supercomputer Summit at ORNL. Compared with the start-of-the-art CPU design, our GPU version can speed up the data refactoring process by up to 330.76× with 45.42 TB/s aggregated throughput on 4096 GPUs. Finally, we showcased our work using a large-scale scientific visualization workflow and the MGARD lossy compression technique. Together, these results demonstrate that scientists have another opportunity for dealing with their high data throughput requirements. Inline refactoring of scientific data can offer performance improvements and temporal fidelity that can benefit a number of science scenarios.

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