Design and Implementation of Hybrid Multiple Valued Logic Error Detector using Single Electron Transistor and CMOS at 120nm Technology

Vaishali P. Raut1, Dr. P. K. Dakhole2,
1Author’s affiliation and full address: Department of Electronics & Telecommunication Engineering GHRCEM, Pune, India
vaishraut02@gmail.com
2Author’s affiliation and full address: Department of Electronics Y.C.C.E, Nagpur, India

Abstract: Hybridization of single electron transistor with MOSFET using quaternary logic for the design of Down Literal circuits are introduced here due to which the number of components as well as interconnection complexity will get reduced just by designing the proper values of components of individual SET such as capacitor and resistors and by changing the values of W/L ratio of MOSFETS. This DLC’s are used for the design of hybrid quaternary logic error detector and verified by CADENCE Tool.

Keywords: MOSFET, SET, Hybrid, MV, SPICE, Quaternary

1. INTRODUCTION
An important aspect of multi-valued logic systems is of choosing the radix value and the choice of radix is available in actual or conceptual domains. Actual and conceptual domains may be different. The choice mainly depends on the ease of manipulations of variables in conceptual domain and manipulations of voltage, current, charge etc. in actual circuits. In this thesis, logic levels are represented as voltage levels and are 0, 1, 2, 3. The no of bits required for binary representation of an n-digit base-r value is n[log2 r] When the radix is not a power of 2, more no of bits are required than minimum and this leads to an inefficient representation. Hence when r = 2^k exact k bits are required. Among the radix values that are powers of 2, the system based on 4 shows considerable promise. The values 8 and 16 are potentially useful. Quaternary logic is quite feasible since the implementations can be designed using available circuitry, and no additional special components are required. Hence quaternary radix is selected to realize the logic circuits[1][2].

2. HYBRIDIZATION OF SINGLE ELECTRON TRANSISTOR MODEL [03] WITH MOSFET BSIM(4.1.0) MODEL
The basic schematic of a SET device where a conductive island is sandwiched between two tunnel junction is depicted in Fig. 1. A proper operation of a SET device requires: 1) the tunnel junction resistances (R_D, R_S) to be greater than the quantum resistance to confine the electron in
the island, and 2) The charging energy of the island capacitance to be larger than the available thermal energy to avoid electron tunneling due to the thermionic emission.

The SET is a four-terminal device. It has a source and drain along with two separate gates. One gate resembles the functionality similar to CMOS transistor gate and second gate is specifically used as back gate for controlling purpose. A single-electron transistor consists of a small conducting island coupled with source and drain, leads by tunnel junctions, and capacitively coupled to one or more gates [3]. Tunnel junction is combination of capacitor and resistor. Fig 1 shows symbol of single electron transistor and PMOS. Single electron transistor which is shown in fig 1 consists of two tunnel junction formed by $R_1C_1$ and $R_2C_2$ whose values are given in table I. For hybrid design SET [03] and BSIM4.1.0 PMOS model used. Fig.2 shows symbol of P-MOSFET of model BSIM(4.1.0).

| Sr. No. | SET[11] | PMOS[BSIM 4.1.0] |
|---------|---------|------------------|
| 1       | SET:    | PMOS:            |
|         | $C_1=1E^{-18}$ | $V_{th}=-0.42V$ |
|         | $C_2=1E^{-18}$ | $W/L=600nm/120nm$ |
|         | $R_1=R_2=1E^5$ |                  |
|         | $C_{g1}=1E^{-18}$ |                  |
|         | $C_{g2}=0$ |                  |

![Fig. 1. Symbol of Single Electron transistor [03]](image1)

![Fig. 2. Symbol of PMOS [BSIM 4.1.0]](image2)
3. QUATERNARY HYBRID ERROR DETECTOR

Detection of errors in any digital circuit plays very important role for the design of big applications consequently it increases the chip area due to addition of extra circuit. There is necessity of compact low power error detection circuit in near future. The single electron transistor is low power as well as very compact devices but one of the disadvantages of single electron transistor is its low current driving capability. To overcome this addition of MOSFET makes it suitable for any practical application having features like low power, less chip area and proper current driving capability.

For the design of quaternary hybrid error detector requires quaternary down literal circuits, multiplexer and quaternary decoder. Initially compact low power three types of down literal circuits are designed is shown in fig.3, 4 and 5 as DLC1,DLC2,DLC3. The down literal circuit performs decoding functions shown in table V. Table II shows combined truth table of three down literal circuits.

| IN | DLC1 | DLC2 | DLC3 |
|----|------|------|------|
| 0  | 3    | 3    | 3    |
| 1  | 0    | 3    | 3    |
| 2  | 0    | 0    | 3    |
| 3  | 0    | 0    | 0    |

3.1 QUATERNARY DOWN LITERAL CIRCUIT: DLC 1

Fig. 3 shows down literal circuit 1 which consists of one P-MOSFET and one N-MOSFET. The W/L ratio of P-MOSFET is (600/120)nm and W/L ratio of N-MOSFET is (4500/120)nm. For the quaternary input 0,1,2,3 which is shown in table II the output of DLC 1 is 3,0,0,0 is verified through simulation.
3.2 Quaternary Down Literal Circuit: DLC 2

![Image of Quaternary Down Literal Circuit 2]

Fig. 4. Quaternary Down Literal Circuit 2

Fig. 4 shows down literal circuit 2 which consists of one P-MOSFET and one N-SET. The W/L ratio of P-MOSFET is (600/120)nm. For the quaternary input 0,1,2,3 which is shown in table II the output of DLC 2 is 3,3,0,0 is verified through simulation.

3.3 Quaternary Down Literal Circuit: DLC 2

![Image of Quaternary Down Literal Circuit 3]

Fig. 5. Quaternary Down Literal Circuit 3
Fig. 5 shows down literal circuit 2 which consists of one P-MOSFET and one N-SET. The w/l ratio of P-MOSFET is (3000/120)nm. For the quaternary input 0,1,2,3 which is shown in table II the output of DLC 3 is 3,3,3,0 is verified through simulation.

As compared to conventional down literal circuits these down literal circuits are different because the proposed DLC circuits are designed by changing the values of W and L of corresponding MOSFET in combination with single electron transistor where as in normal CMOS DLC circuits selection of MOSFET is according to the value of threshold voltage is important. If the DLC circuits are designed with selection of threshold voltage increases the hardware as well as dependency of particular MOSET increases the cost of chip. for this reason the proposed DLC circuits are low power and compact which reduces the chip area.

Fig. 6 shows the block diagram of quaternary hybrid error detector. This is designed using quaternary decoder, quaternary multiplexer and DLC circuits. According to the table V input 0,1,2,3 is given to the quaternary decoder whose corresponding outputs are given to the quaternary multiplexer as input and same signal as input which was given to the decoder is given as a select line to the multiplexer that means select line and input of decoder is same signal which is tested by using this quaternary hybrid error detector. Output waveform verifies the error detection operation of this signal which is shown in fig. 7.

![Quaternary Hybrid Error Detector](image-url)
TABLE III. QUATERNARY HYBRID ERROR DETECTOR TRUTH TABLE

| INPUT | DECODER OUTPUT | MUX OUTPUT |
|-------|----------------|------------|
|       | QLD0 | QLD1 | QLD2 | ERRPR | DETECTION |
| 0     | 3    | 0    | 0    | 0     | QLD0 3    |
| 1     | 0    | 3    | 0    | 0     | QLD1 3    |
| 2     | 0    | 0    | 3    | 0     | QLD2 3    |
| 3     | 0    | 0    | 0    | 3     | QLD3 3    |

Fig. 7. Quaternary hybrid error detector output waveform
4. PERFORMANCE ANALYSIS OF DLC CIRCUITS

*Quaternary Down Literal Functions [11]*

| TABLE IV. QUATERNARY DOWN LITERAL CIRCUIT [11] |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| SR.NO. | T1 | T2 | T3 | T4 | T5 | T6 |
| Threshold Voltage | -0.1 | 1.0 | 0.6 | 0.2 | -0.2 | -0.6 |
| Voltage | PMOS | NMOS | PMOS | NMOS | PMOS | NMOS |

*Quaternary Decisive Literal Functions (Proposed)*

| TABLE V. QUATERNARY DOWN LITERAL CIRCUIT [PROPOSED] |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| SR.NO. | T1 | T2 | T1 | T2 | T1 | T2 |
| DLC1 | DLC2 | DLC3 |
| W | 600nm | 4500nm | 600nm | SET[03] | 3000nm | SET[03] |
| L | 120nm | 120nm | 120nm | 120nm |
| Type | PMOS | NMOS | PMOS | NSET[03] | PMOS | NSET[03] |

5. CONCLUSION

Quaternary hybrid error detector is proposed with unique DLC circuits and verified according to the truth table through simulation. By using this type of DLC circuit dependency of threshold based transistor selection is not needed. The proposed quaternary hybrid error detector is compact and easy to design. It consumes very less power. Hybridization of single electron transistor with MOSFET using quaternary logic for the design of Down Literal circuits are introduced here due to which the number of components as well as interconnection complexity will gets reduced just by designing the proper values of components of individual SET such as capacitor and resistors and by changing the values of W/L ratio of MOSFETS.

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