Rethinking Reinforcement Learning based Logic Synthesis

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Abstract

Recently, reinforcement learning has been used to address logic synthesis by formulating the operator sequence optimization problem as a Markov decision process. However, through extensive experiments, we find out that the learned policy makes decisions independent from the circuit features (i.e., states) and yields an operator sequence that is permutation invariant to some extent in terms of operators. Based on these findings, we develop a new RL-based method that can automatically recognize critical operators and generate common operator sequences generalizable to unseen circuits. Our algorithm is verified on both the EPFL benchmark, a private dataset and a circuit at industrial scale. Experimental results demonstrate that it achieves a good balance among delay, area and runtime, and is practical for industrial usage.

1 Introduction

Logic synthesis (LS) aims at finding an equivalent representation of large-scale integrated circuits [Mishchenko et al. 2007]. It mainly consists of three steps, namely pre-mapping optimizations, technology mapping and post-mapping optimizations. In the pre-mapping optimization phase, technology-independent transformations are performed on the And-Inverter-Graph (AIG) representation of a circuit to reduce the graph’s total number of nodes and levels [Ziegler et al. 2016, Rieger et al. 2019, Yu et al. 2018, Haaswijk et al. 2018, Hosny et al. 2020, Zhu et al. 2020]. In the technology mapping and post-mapping optimization phases, the AIG is mapped into standard ASIC or FPGA cells, followed by technology-dependent optimizations such as up-sizing and downsizing [Mishchenko et al. 2007, Liu and Zhang 2017].

Usually, a large portion of the optimization efforts is on pre-mapping optimizations, which are carried out by a sequence of operators such as rewrite, refactor, and resub [Mishchenko et al. 2007]. Some of these operators are good at reducing the number of nodes of an AIG, and others the number of levels. Pre-mapping optimization targets at finding an operator sequence that can reduce an AIG’s total number of nodes (a.k.a., area), levels (a.k.a., delay) or both of them while keeping its boolean function unchanged. Since there are a large number of operators and the sequence length could be extremely long, combination of different operators and their permutations result in an exponentially growing search space. Additionally, each operator is associated with a set of tunable hype-parameters, making the LS problem even more difficult. For ease of discussion, as most of existing works do [Hosny et al. 2020, Zhu et al. 2020, Li et al. 2022, Grosnit et al. 2022], we

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herein only consider the operator sequence optimization, setting each operator’s hype-parameters as default. There are a number of pre-mapping optimization sequences, among which Resyn2 is a well-known one.

As LS is a sequential decision making problem, some recent works formulate it as a Markov decision process (MDP) [Liu and Zhang 2017] and use reinforcement learning (RL) algorithms to attack it. RL learns a control policy that determines which operator to use at different states, where states are feature vectors of the current AIG. Hosny et al. [2020] extracts some statistical features as the feature vector. In contrast, Zhu et al. [2020] and Haaswijk et al. [2018] transform an AIG into a feature vector using graph neural networks (GNN). The policy is learned in a trial-and-error manner, maximizing s long-term accumulated reward, which is defined as a function of the AIG’s reduced number of nodes or levels. Experiment results demonstrate their efficiency in terms of area or delay reduction. However, runtime of these algorithms is completely ignored. All of these methods train a different policy for different circuit online and then choose the best-performed one among tens or hundreds of online evaluation trials. The training and evaluation procedures often take hundreds of or thousands of times the runtime cost of Resyn2, which is totally unacceptable for real applications.

Based on these works, we conduct extensive experiments and have two basic findings: (1) decisions made by the RL policy do not depend on circuit features; (2) permutation of these operators have little effect on the final performance. These findings reveal that: 1) it is unnecessary to extract circuit features 2) though LS has an exponentially growing search space, the loss surface is somewhat flat, since permutation of operators in the same sequence has little effect on the final performance.

Based on these findings, we develop a new method that can automatically recognize critical operators and generate a common sequence for different circuits. The method consists of two major steps, where the first step learns a shared policy for a number of circuits (served as a training dataset), and the second step searches for a best-performed common sequence based on the learned policy. Different from previous RL-based methods that recommend a different operator sequence for different circuit, the common sequence can be directly used to optimize unseen circuits without online learning or further adaptation, saving lots of time. Extensive experiment results demonstrate that our method is capable of finding a common sequence that achieves good performance in terms of area or delay reduction and significantly reduce the runtime. The common sequence can be directly integrated into ABC [Mishchenko et al. 2007], a well-known LS tool, as a substitute for Resyn2, without modifying the ABC architecture.

The remainder of this paper is organized as follows. Section 2 gives a brief introduction to LS and RL. Section 3 elaborates our basic findings on RL based LS. Section 4 introduces our proposed method. Section 5 presents experiment results and section 6 concludes this paper.

2 Background

2.1 Logic Synthesis

The whole process of LS can be divided into three stages, i.e., pre-mapping optimizations, technology mapping and post-mapping optimizations. The pre-mapping optimization stage is at the core of the LS process. There exist a rich set of optimization operators, such as rewrite, refactor, and resub. Some of these operators are good at reducing the number of nodes of an AIG, and others the number of levels.

An AIG often has thousands of or even millions of nodes, and the number of levels can also be large. Most of these operators optimize an AIG by iteratively replacing the subgraph rooted at a chosen node with a new subgraph that has less number of nodes or levels, where the root node is selected in a topological order. In this way, the whole AIG could be optimized [Mishchenko et al. 2007]. As some operators are good at reducing area and some delay, it is necessary to design an operator sequence that can make full use of different operators. As the length of an operator sequence could be large, the search space grows exponentially with the sequence length.

2.2 Reinforcement Learning

MDPs [Sutton and Barto 2018] are widely used to formulate discrete time stochastic control processes. Consider a MDP defined by a tuple \((\mathcal{M}, S, A, r, P, \gamma, H)\), where \(S\) is the state space, \(A\) is...
the finite action space, \( r : S \times A \to \mathbb{R} \) the bounded reward function, \( P : S \times A \times S \to \mathbb{R}_{\in[0,1]} \) is the transition probability distribution, \( \gamma \) is the discount factor that we assume \( \gamma \in [0, 1) \) and \( H \) is the episode horizon. The agent interacts with the MDP at discrete time steps by performing its policy \( \pi : S \times A \to \mathbb{R}_{\in[0,1]} \), generating a trajectory of states and actions, \( \tau = (s_0, a_0, s_1, a_1, \ldots s_H, a_H) \), where \( s_0 \sim \rho_0(s) \), \( a_t \sim \pi(\cdot | s_t) \) and \( s_{t+1} \sim P(\cdot | s_t, a_t) \).

The objective of a reinforcement learning agent is to find a policy that maximizes the expected cumulative discounted rewards given the initial state \( s_0 \):

\[
J(\pi) = \mathbb{E}_{a_t \sim \pi(\cdot|s_t), s_{t+1} \sim P(\cdot|s_t, a_t)} \left[ \sum_{t=0}^{H} \gamma^t r(s_t, a_t) \right].
\]

(1)

REINFORCE is a RL algorithm that parameterizes the policy \( \pi(a|s) \) as a continuous function \( \pi(a|s, \theta) \) with \( \theta \) as the function parameters. \( \theta \) is updated by the policy gradient method [Sutton et al. 2000]:

\[
\theta = \theta + \alpha \nabla_{\theta} \log \pi(\theta)(s_t, a_t) \sum_{i=t}^{H} r_i,
\]

(2)

where \( \alpha \) is the learning rate.

### 2.3 Problem Formulation

As done in [Liu and Zhang 2017, Hosny et al. 2020, Zhu et al. 2020], given a circuit, LS can be formulated as a MDP, where the state space \( S \) contains all equivalent AIGs and the action space \( A \) contains available operators. In this paper, we fix the action space as \( A = \{\text{resub}, \text{resub} \rightarrow z, \text{rewrite}, \text{rewrite} \rightarrow z, \text{refactor}, \text{refactor} \rightarrow z, \text{balance}\} \), which is the same as that used by Resyn2. The initial state \( s_0 \) is the original AIG to be optimized. Given any \( s \in S \) and \( a \in A \), \( s' \) is an AIG obtained by applying an operator \( a \) to AIG \( s \). The reward function \( r(s, a, s') \) can be designed as a function of the reduced amount of area or delay after applying the operator \( a \) (e.g., the weighted summation of the reduced area or delay). Then we can leverage RL algorithms to learn a policy that can transform a circuit into a simpler one.

Different reward functions are designed in [Liu and Zhang 2017, Hosny et al. 2020, Zhu et al. 2020], some encourage area reduction under a delay constraint, some encourage delay reduction, etc. For ease of discussion, in this paper, we employ two simple reward schemes, one encourages area reduction and the other delay reduction, denoted as area-first and delay-first reward schemes, respectively. Specifically, for the area-first reward scheme, \( r(s, a, s') \) denotes the ratio of the reduced area of the two AIGs \( s \) and \( s' \) over the initial area. Similarly, for the delay-first reward scheme, \( r(s, a, s') \) is the ratio reduced delay over the initial delay.

### 3 Revisiting RL-based Logic Synthesis

In this section, we dive deep into current RL-based LS methods. Specifically, we first evaluate the influence of different feature embeddings of an AIG on the LS performance, and then investigate the behavior of the learned policy during the decision-making phase. We select four circuits in the EPFL benchmark [Amarú et al. 2015] and four from [Mishchenko et al. 2007, Brglez et al. 1989] and [Yang 1991] as a circuit dataset, denoted as EPFL-Test. Besides, we use REINFORCE as the learning algorithm and follow similar hyper-parameter configurations as done in [Zhu et al. 2020].

### 3.1 Circuit Features

Since the state is an AIG with thousands of or even millions of nodes and edges, feature extraction is needed to transform the raw AIG into a compact representation. Existing representation methods can be roughly divided into two categories.

- **Statistics features** [Hosny et al. 2020] use the statistical information of an AIG, \([\#\text{primaryI/O}, \#\text{nodes}, \#\text{edges}, \#\text{levels}, \#\text{latches}, \%\text{ANDs}, \%\text{NOTs}]\), to represent the circuit. When an operator is applied, these statistics will change. Therefore, statistics embedding indeed includes some important information of the circuit.
We argue that both the statistics feature and the graph feature are incapable of extracting useful features. Firstly, it is obvious that the statistics feature loses too much structural information of an AIG, and it is quite possible that two thoroughly different AIGs have the same statistical features.

The reasons are two fold. One on hand, aggregating millions of node features into a single feature vector is still open to discussion, and computing the graph embedding requires huge computational overhead. On the other hand, most LS operators are in fact local optimization operators that iteratively choose one node each time in an AIG and replace the subgraph rooted at the chosen node (a.k.a., cut [Mishchenko et al. [2007]]) with a new subgraph that has the same boolean function but less nodes or levels. In principle, aggregating all the nodes information into a single vector can not guide operators to conduct subgraph replacements.

Our empirical studies also verify the above claims. We perform RL-based LS using different types of circuit features as circuit states, i.e., statistics features, graph features and non-informative features (random vectors having the same dimension as that of statistics features). For ease of denotation, we name non-informative features as random features. Experiment results are shown in Table 1. As we can see, the area and delay given by different RL algorithms are reduced by around 16%, which are similar to those of Resyn2. Furthermore, it seems that these RL policies can make decisions without accessing AIG states, since the policy performs well even using random features.

| Dataset | Results | Init. | Resyn2 | Area-first | Delay-first |
|---------|---------|-------|--------|------------|------------|
|         | Area    | Delay | Area Imp. | Delay Imp. | Area Imp. | Delay Imp. | Area Imp. | Delay Imp. |
| Log2    | 27062   | 274   | 0.09    | 0.04      | 24776     | 274       | 0.08      | 26888     | 266       | 0.03      |
|        | 24618   | 3088  | 0.07    | 0.21      | 3086      | 179       | 0.07      | 3267      | 205       | 0.097     |
| Log2    | 502     | 25    | 0.22    | 0.32      | 390       | 18        | 0.22      | 387       | 18        | 0.48      |
|        | 1776    | 37    | 0.29    | 0.27      | 1523      | 36        | 0.14      | 1388      | 27        | 0.27      |
| Log2    | 1469    | 26    | 0.03    | 0.01      | 1400      | 26        | 0.047     | 1466      | 26        | 0.0       |
| I1O     | 2673    | 50    | 0.31    | 0.36      | 1768      | 44        | 0.31      | 1055      | 33        | 0.34      |

**Graph features** [Haaswijk et al. [2018], Zhu et al. [2020]] propose to use not only the statistical features but also the graph embedding of an AIG. To obtain the graph embedding, each node in the AIG is firstly represented as a vector (node embedding) containing information about its node type, as well as the edge type of its two fanins. Node embeddings are then passed through two consecutive layers of graph convolution networks so that each node’s neighborhood information is aggregated. The graph features are then obtained by taking the average of all the node embeddings.

We argue that both the statistics feature and the graph feature are incapable of extracting useful features. Firstly, it is obvious that the statistics feature loses too much structural information of an AIG, and it is quite possible that two thoroughly different AIGs have the same statistical features. Secondly, the current graph feature extracting scheme is virtually ineffective and impractical. The reasons are two fold. One on hand, aggregating millions of node features into a single feature vector is still open to discussion, and computing the graph embedding requires huge computational overhead. On the other hand, most LS operators are in fact local optimization operators that iteratively choose one node each time in an AIG and replace the subgraph rooted at the chosen node (a.k.a., cut [Mishchenko et al. [2007]]) with a new subgraph that has the same boolean function but less nodes or levels. In principle, aggregating all the nodes information into a single vector can not guide operators to conduct subgraph replacements.

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### 3.2 Permutation Invariance

Since decisions are made without accessing circuit features (i.e., \( \pi(a \mid s) \) degenerates to \( \pi(a) \)), we guess the action distributions at different time steps are similar. To this end, we investigate the decisions made by them at different time steps. As expected, the learned policy samples an operator...
from an operator distribution that hardly evolves over time, where operator distributions for different circuits are illustrated in Fig 1 (due to space limitation, we only show the operator distributions of the policy using random feature features. Policies using statistic features and graph features have similar results. Besides, we also show the learned operator distributions of the RL algorithm with an extended operator space, which we would discuss later).

The above finding suggests that operators may be permutation invariant to some extent. To verify it, for each circuit, we first sample an operator sequence (consisting of ten operators) according to the operator distribution shown in Fig 1, and then generate ten sequences by randomly shuffling the sampled sequence. Evaluation results of these randomly permuted sequences are shown in Table 3. As expected, there is only a minor difference among the results of these sequences, demonstrating that the performance of an operator sequence is almost permutation invariant. Based on these findings, we can conclude that although LS has an exponentially growing search space, the loss surface seems relatively flat and the (local) optima is easy to reach.

### 3.3 Critical Operators

From Fig 1 we can see that the performance improvements are mainly determined by some frequently used operators, which we denote as critical operators, and RL-based algorithms could learn to discover these critical operators. Then we wonder if the performance would be further improved by involving new operators. In this regard, we re-implement the above RL algorithms with an extended operator space (newly added operators are sopb, fraig, dsdb, blut). As shown in Table 2, when more operators are used, the area remains similar but the delay is reduced from 0.82 to 0.52 (these numbers are the mean of the ratios of the area or delay of the optimized circuit over the those of the initial circuit, and the smaller, the better). The results make sense since most of the four newly added operators are good at delay optimization.

These results demonstrate that the newly incorporated operators do expand the optimization upper bound of LS and RL algorithms are still capable of discovering good operators suitable for different circuits.

Table 2: RL-based LS with more Operators. Each number in the table is the mean of ratios of the optimized area or delay over their initial values (the smaller, the better).

|          | Init. | Resyn2 |       |       |       |       |
|----------|-------|--------|-------|-------|-------|-------|
|          | Area  | Delay  | Area  | Delay | Area  | Delay |
|          | 1.0   | 1.0    | 0.83  | 0.82  | 0.83  | 0.84  |
|          | 1.009 | 0.52   |       |       |       |       |

In summary, we first find out that decisions made by RL policies do not depend on circuit features (states). The phenomenon in Subsection 3.2 that the operator distribution does not evolve over time also verifies the state-agnostic property. Furthermore, it also indicates that operators are permutation invariant to some extent, which is supported by our experiments. Besides, we also observe that the
Table 3: Permutation Invariance of Operator Sequences. Ten randomly permuted sequences are evaluated for each circuit. Each number in the "Mean", "Max" and "Min" column denotes the area or delay of an AIG normalized by its initial values (the smaller, the better).

| Name | Area-first |   |   |   | Delay-first |   |   |   |
|------|------------|---|---|---|-------------|---|---|---|
|      | Mean       | Max| Min| Std| Mean        | Max| Min| Std |
| log2 | 0.92       | 0.93| 0.91| 0.005| 0.93 | 0.94| 0.86| 0.012 |
| multi. | 0.90 | 0.91| 0.89| 0.003| 0.11 | 0.93| 0.96| 0.01 |
| sin | 0.93      | 0.94| 0.93| 0.003| 0.93 | 0.95| 0.79| 0.007 |
| sqrt | 0.79      | 0.80| 0.78| 0.006| 0.78 | 0.79| 0.99| 0.003 |
| c1355 | 0.77 | 0.78| 0.76| 0.004| 0.78 | 0.85| 0.77| 0.019 |
| c5315 | 0.73 | 0.76| 0.70| 0.019| 0.75 | 0.77| 0.72| 0.012 |
| c7552 | 0.94 | 0.95| 0.94| 0.004| 0.95 | 0.96| 0.93| 0.006 |
| 110  | 0.68      | 0.72| 0.64| 0.02 | 0.71 | 0.74| 0.67| 0.024 |

performance could be further improved by incorporating new operators and RL is still capable of discovering critical operators.

4 Method

Though existing RL methods can learn policies with good performance, runtime is thoroughly ignored, which is of critical importance for real applications. Existing works [Hosny et al. 2020; Zhu et al. 2020] propose to learn different policies for different circuits. For each circuit, time elapsed for the feature extraction process and RL training process is often hundreds of thousands of times that of Resyn2. Therefore, when there are a number of circuits to be optimized, the time required is totally unacceptable. In this section, we propose a method that learns a common policy for different circuits using RL, based on which a low-runtime common operator sequence is derived.

Algorithm 1 RL-driven Common Sequence Design

1: procedure RL TRAINING(D, T) \(\triangleright\) RL training phase takes a circuit dataset \(D\) and the maximum training \(T\) step as inputs
2: Randomly Initialize a policy function \(\pi(a|s_r)\), where \(s_r\) is sampled from a 4D uniform distribution each time \(\pi(a|s_r)\) is used
3: for \(i = 0, \ldots, T\) do
4: Randomly sample a circuit from the training set \(D\).
5: Rollout an operator sequence following policy \(\pi(a|s_r)\).
6: Update policy parameters using REINFORCE [Sutton and Barto 2018]
7: end for
8: Return \(\pi(a|s_r)\)
9: end procedure
10: procedure SEQUENCE DESIGN(D, \(\pi(a|s_r)\), \(L\)) \(\triangleright\) Sequence design phase takes the training set \(D\), the learned policy \(\pi(a|s_r)\) and the sequence length \(L\) as inputs
11: Initialize an empty sequence \(Seq\) and a performance metric \(m = 0\)
12: for \(i = 0, \ldots, 9\) do
13: Sample a common sequence \(S_i\) with length \(L\) by following the learned policy \(\pi(a|s_r)\).
14: Obtain the value of reduced area or delay \(m_i\) of the common sequence by evaluating it on the training set \(D\).
15: Let \(m = m_i\) and \(Seq = Seq_i\) if \(m_i > m\).
16: end for
17: Return \(Seq\)
18: end procedure

The reason of choosing RL is as follows. According to our analysis in Section 3, we can reach a conclusion that LS is a MDP with a really special structure: given a circuit, the optimal action distribution at different time steps hardly evolve over time. This is analogous to a barrier-free 2-
dimensional navigation task. It is obvious that a talented agent should move towards the target position at each time step, and superficially, navigation decisions are made without accessing any states. For LS, an agent aims to push an initial AIG to another point (in the AIG space) that has less number of nodes or levels. Then executing an operator sampled from a fixed operator distribution at different time steps is analogous to executing a fixed action in the 2D navigation task. Accordingly, we continue to leverage RL algorithms with random state representations to learn policies, as done in Subsection 3.1. Using random features saves plenty of time especially when compared with the approach using graph features.

Furthermore, we need to learn a policy that can generalize to unseen circuits. Only in this way, we can avoid online learning a new policy for a new circuit, making RL a feasible approach for real applications. Fortunately, the operator distributions are similar to each other, as shown in Fig 1. Consequently, we expect a common distribution would work for different circuits. To this end, we no longer train a separate policy for each circuit. Instead, we train a shared policy on a training dataset consisting of multiple circuits. During the training phase, the algorithm randomly samples a circuit from the training dataset, rollouts an operator sequence using the currently learned policy and then performs policy gradient update using the collected data.

Additionally, observing that operators are somewhat permutation invariant, we further derive a common sequence based on the learned common policy. Specifically, we randomly sample 10 sequences (each composed of 10 operators) according to the learned policy and select the best-performed one based on their evaluation results on the training dataset. The selected common sequence can serve as an alternative to Resyn2, without modifying the structure of the ABC LS tool.

Table 4: Results of different RL-based algorithms on the six unseen circuits from the EPFL benchmark. The 'Common' row is the results of our common sequence. Runtime is normalized by the elapsed time of the common sequence. Each number in the area and delay columns is the mean of ratios of the area or delay over their initial values (the smaller, the better).

| Methods               | Init. | Area-first | Delay-first |
|-----------------------|-------|------------|-------------|
|                       | Area  | Delay      | Area        | Delay     | Runtime | Area   | Delay | Runtime |
| Graph embeddings      | 1.0   | 1.0        | 0.89        | 0.93      | 1000+   | 10.921 | 0.943 | 1000+   |
| Stats. embeddings     | 1.0   | 1.0        | 0.91        | 0.992     | 200+    | 0.9355 | 0.999 | 200+    |
| Common sequence       | 1.0   | 1.0        | 0.876       | 0.94      | 1.0     | 0.845  | 0.95  | 1.0     |

In summary, our proposed method first learns a common policy on a training dataset consisting of multiple circuits through RL, and then derives a common operator sequence based on the learned policy. The common sequence can be directly used for new circuits without online learning or further adaptation. Our proposed method is demonstrated in algorithm 1.

5 Experiments

In this section we present the main results of our proposed method. We first evaluate its runtime efficiency and then its generalization ability to unseen circuits. The maximum training epochs \( T \) in algorithm 1 is set to 200. Besides, in Section 5.2 and 5.3 to meet with industrial demands, we extend the fixed operator set introduced in Section 2.3 by adding the four operators \( sopb, fraig, dsdb, blut \) used in Section 5.2.

5.1 Learning a Common Sequence

We feed the EPFL-Test dataset into algorithm 1 and it returns a common operator sequence, which is directly evaluated on the left six circuits from the EPFL benchmarks [Amaru et al. 2015]. Besides, the two RL algorithms using graph features and statistics features are re-implemented to learn a new policy online for each of the six circuits, as done in [Hosny et al. 2020] and [Zhu et al. 2020] (each policy is also trained for 200 epochs). Experiment results are shown in Table 4. As we can see, these RL-based online learning algorithms and our common sequence yield similar results, demonstrating that our RL-based common sequence design method is indeed capable of automatically generating common sequences that perform well on new circuits.
Most importantly, since our method does not require online learning a new policy or searching a new sequence for an unseen circuit, its runtime cost is comparable with that of Resyn2. On the contrary, the RL algorithm using statistics features needs to learn a new policy for each unseen circuit, which takes more than two hundred times the runtime of ours. Worse still, the RL algorithm using graph features needs to extract graph features and the runtime cost is even worse. The online learning paradigm of existing RL solutions prevents them from real applications.

5.2 Generalization to New Circuits

| Dataset | Results | Init. | Resyn2 | Area-first | Delay-first | Runtime |
|---------|---------|-------|--------|------------|-------------|---------|
|         |         | Area  | Delay  | Area       | Delay       |         |
|         |         |       |        |            |             |         |
| Training|         | 1.0   | 1.0    | 0.72       | 0.70        | 1.0     |
| Evaluation |     | 1.0   | 1.0    | 0.80       | 0.87        | 1.0     |

To evaluate the generalization ability of our method, we introduce a private dataset (denoted as INDU) that was originally for industrial uses and consists of 40 circuits. We select ten of them as the training set and evaluate the common sequence on the rest. Results are shown in Table 5.

As observed, the common sequence significantly reduces the area (area-first) and the delay (delay-first) on the training set to 0.68 and 0.47, respectively, and the two values are reduced to 0.77 and 0.59 on the evaluation set. Although the common sequence is trained on 10 circuits, it generalizes well to the left 30 circuits that do not appear in the training set. Besides, the common sequence only consists of 10 operators and is consequently runtime efficient.

Table 6: LS results on a large-scale circuit C347. Note that each number in the last row denotes the area and delay of the circuit after technology mapping.

| Circuit | Init. | Resyn2 | Common Sequence |
|---------|-------|--------|-----------------|
|         | Area  | Delay  | Area            | Delay | Runtime | Area | Delay | Runtime |
| C347    | 61586 | 223    | 365002          | 195   | 414s    | 344040 | 176   | 1635s   |

5.3 Evaluation on an Industrial Circuit

To meet with the industrial demand, we design a new common sequence by re-implementing our method on the entire INDU benchmark with slightly different configurations. Specifically, our previous experiments use the reduced number of nodes or levels before technology mapping as the reward function. Here we shift the reward function to the reduced amount of area or delay of an AIG after technology mapping. The learned common sequence (consisting of 10 operators) is then used to optimize a large-scale circuit named C347 with around 3,470,000 nodes and 700 levels. Results are shown in Table 6. Again, our method generates a common sequence that shows impressive performance on the circuit which is significantly different from the training set in terms of circuit scale (i.e., the number of nodes and levels).

6 Conclusion

In this paper, we propose a practical RL-based method that can automatically recognize critical operators and generate a common sequence for LS tasks. Specifically, we first investigate current RL-based methods and find out that the learned policy is state-agnostic and yields an operator sequence that is somewhat permutation invariant. In this regard, we propose to learn a common policy using RL and then derives a common sequence on the training set consisting of multiple circuits. Experiment results demonstrate that the common sequence can reduce the area or delay of different circuits and can be directly applied to new circuits without online learning or further adaptation. Furthermore, when more operators are used, our method is still capable of finding good operator distributions and generating common sequences that reduce the area and delay by a large margin.
Last but not least, our method is runtime-efficient when compared with existing RL-based methods that need to learn a new policy for a new circuit. Besides, the designed common sequence can serve as a substitute for Resyn2 baseline without modifying the architecture of ABC, the open-source LS tool. In future work, we will continue exploring novel sequence and parameter optimization methods alone the line that does not access circuit features to better solve the LS problem.

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