The role of the substrate in Graphene/Silicon photodiodes

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Abstract. The Graphene/Silicon (Gr/Si) junction can function as a Schottky diode with performances strictly related to the quality of the interface. Here, we focus on the substrate geometry and on its effects on Gr/Si junction physics. We fabricate and study the electrical and optical behaviour of two types of devices: one made of a Gr/Si planar junction, the second realized with graphene on an array of Si nanotips. We show that the Gr/Si flat device exhibits a reverse photocurrent higher than the forward current and achieves a photoresponsivity of 2.5 A/W. The high photoresponse is due to the charges photogenerated in Si below a parasitic graphene/SiO\textsubscript{2}/Si structure, which are injected into the Gr/Si junction region. The other device with graphene on Si-tips displays a reverse current that grows exponentially with the bias. We explain this behaviour by taking into account the tip geometry of the substrate, which magnifies the electric field and shifts the Fermi level of graphene, thus enabling fine-tuning of the Schottky barrier height. The Gr/Si-tip device achieves a higher photoresponsivity, up to 3 A/W, likely due to photocharge internal multiplication.

1. Introduction

Schottky diodes are formed by a metal/semiconductor junction. They possess a low forward voltage drop and fast switching, which make them suitable for fast digital logic circuit, high sensible photodetectors and easy-to-fabricate solar cells. Their performance and photosensitivity are strictly related to the metal electrode [1]. The metal can reflect part of the light or absorb a certain range of the spectrum, which become unavailable for sensing. Such problem can be overcome with the use of a transparent and conductive two-dimensional material such as graphene, in graphene/semiconductor junctions [2]. Graphene is formed by a single layer of carbon atoms arranged in a honeycomb lattice; it possesses maximum surface to volume ratio, high mobility [3, 4], high thermal [5] and electrical conductivity [6], constant optical absorption over a wide spectral range [2], low contact resistance [7, 8, 9], and easy down-scaling [10]. The conduction and valence bands of graphene touch in 6 points, where they form double-cone structures, which correspond to vanishing energy gap and density of states. Then, graphene/semiconductor junctions offer the opportunity to study the phenomena that occurs at the interface between a gapless 2D material and a semiconducting 3D material. In particular, the Gr/Si junction is one of the simplest device that one can realize. It behaves like a Schottky diode and its current-voltage characteristics can be described by thermionic emission theory. Some peculiarities, such as the growing reverse bias saturation current has been explained by the modulation of the Schottky barrier height caused by the low density of states of graphene [2]. In this work, we mainly study how the geometry of the Si substrate can affect the electrical transport and the photoresponse of Gr/Si junctions, a topic which is attracting growing attention [11].
2. Materials and method

We realized two different types of devices. The first device type, Fig. 1(a), was fabricated by depositing a layer of \( \sim 245 \) nm thickness of SiO\(_2\) on a low doped n-type Si wafer (\( \sim 4.5 \cdot 10^{14} \) cm\(^{-3}\)) by chemical vapor deposition (CVD). We patterned a trench of 10 \( \mu \)m wide by lithography, then we removed the SiO\(_2\) from the trench area by a hydrofluoric acid treatment. Graphene sheet of \( \sim 1 \times 0.4 \) cm\(^2\) was deposited on the wafer soon after to reduce the chance of oxide formation on the Si surface. Graphene acts as the anode of the Gr/Si junction and top electrode of the Gr/SiO\(_2\)/Si Metal-Oxide-Semiconductor (MOS) capacitor, formed at two sides of the junction [12, 13]. The second type of device, shown in Fig. 1(b), was made from a degenerately doped (\( \sim 10^{18} \) cm\(^{-3}\)) n-type Si wafer. We used lithography and Reactive-Ion Etching (RIE) to fabricate a matrix of nanotips with \( \sim 450 \) nm height, \( \sim 50 \) nm top-diameter and 1.4 \( \mu \)m distance from each other (from here on, we will refer to the nanotip array as the Si-tips). Subsequently, the Si-tips were coated with a layer of SiO\(_2\) deposited by CVD, then, the SiO\(_2\) thickness was reduced through a chemical-mechanical planarization step until the Si-tips were revealed. Before the graphene transfer, the Si-tips were dipped in a 0.5\% hydrofluoric acid solution for 10 s to remove the native SiO\(_2\) from their apices [14]. In both devices graphene was transferred from commercial Cu foils onto the Si substrate using the wet transfer process [15]. Ohmic metal contact to graphene was fabricated by evaporation of Ti/Au metal stack through a shadow mask. In the first device, the cathode was established by depositing Ag paste on the exposed Si area of the wafer after scratching it to ensure ohmic contact. In the second device, Ag paste was deposited on the bottom of the substrate after the SiO\(_2\) was removed by scratching. The I-V characterization was performed in vacuum (\( \sim 10 \) mbar) using a Janis ST-500 micromanipulated probe station connected to a Keithley Semiconductor Characterization System 4200 (SCS-4200). The forcing bias was applied to the Ti/Au contact while the Ag contact was grounded. The responsivity was investigated using the light from a white LED array with controllable intensity up to 5 mW/cm\(^2\) and spectral range 420 – 720 nm with two peaks at 454 nm and 536 nm, respectively.

3. Results and discussion

In Fig. 1(c) we show the current-voltage characteristics of the devices of Fig. 1(a) and (b), which we refer to as the flat Gr/Si and the Gr/Si-tip junction, respectively. Both devices were measured at 300 K and show a rectification behaviour with the forward current at positive bias typical of p-type graphene on n-type Si. At the bias of \( \pm 1 \) V, the flat Gr/Si device displays a rectification factor of \( 10^3 \) while the Gr/Si-tip junction has a rectification ratio of \( 10^2 \).
Figure 1. (a) Schematic view of the flat Gr/Si and (b) Gr/Si-tip devices. (c) I-V characteristics of the two devices, measured at 300 K and from $-1.5$ V to 1.5 V. The inset shows the Richardson plot of both devices where $I_0$ is the zero bias saturation current, obtained by extrapolating the forward current to 0 V. (d) Numerical simulation (by COMSOL Software) of the electric field around the tip at a reverse bias of $-1$ V. The intensity of the electric field is shown through a scale of colors in which blue indicates the minimum value while the red is the maximum. The Gr/Si junction in this simulation is considered like an ideal Schottky contact with a work function of 4.6 eV and a Schottky barrier height of 0.19 eV. The Gr/Si is at $-1$ V respect to the bottom n-Si substrate, which is grounded.

The I-V characteristic can be studied using the thermionic emission model:

$$I = I_0 \left[ e^{\frac{qV}{nkT}} - 1 \right]$$

(1)

where

$$I_0 = AA^* T^2 e^{-\frac{\Phi_B}{kT}}$$

(2)

is the reverse current, A is the contact surface, $A^* = 4\pi\tau m^* k^2/h^3$ is the effective Richardson constant which is specific of the semiconductor type (for n-Si, $A^* = 120 A/(K \cdot cm)^2$), $m^*$ is the effective electron mass, $q$ is the electronic charge, $\Phi_B$ (eV) is the Schottky barrier height, $k$ is the Boltzmann constant and $n$ is the ideality factor. The ideality factor is a phenomenological parameter that takes into account deviations from the thermionic regime, as carrier generation/recombination or effects due to the presence of oxide or other inhomogeneities at the Gr/Si interface. Rewriting equation (1) in the form:

$$\ln \left( \frac{I_0}{T^2} \right) = \ln(AA^*) - \frac{\Phi_B}{kT}$$

(3)

$\Phi_B$ and $A^*$ can be evaluated from the slope and the intercept of the plot of $\ln(I_0 / T^2)$ vs. $10^3/T$, respectively. In Tab. 1 we report the Schottky barrier height $\Phi_B$, the ideality factor $n$ and the Richardson constant $A^*$ of the two devices.

| Table 1. Schottky parameter of both devices |
|---------------------------------------------|
| Flat Gr/Si device | $\Phi_B$ (eV) | $n$ | $A^*$ ($A/cm^2K^2$) |
|------------------|-------------|----|-------------------|
| Gr/Si-tip device | 0.52        | 3.9| $4.78 \times 10^{-5}$ |
|                  | 0.36        | 1.5| 0.002             |

The difference in the barrier height can be ascribed to the stronger force image barrier lowering which depends on the forth root of the doping level, $\Delta \Phi_B \sim \sqrt[N_D]{N_D}$. The high value of the ideality factor $n$ and the resulting $A^*$, which is lower than the theoretical value in metal-semiconductor junctions [13, 14, 16,
17], suggest the presence of an insulating layer and of inhomogeneity at the Gr/Si interface, which are higher for the flat Gr/Si device, due to the larger junction area.

Fig. 1(c) shows also that the reverse current of the flat Gr/Si device is constant while the one of the Gr/Si-tip junction increases exponentially with the bias. The reason for this difference lies in the geometry of the substrate. The electric field of the flat Gr/Si junction is homogeneous throughout the contact surface and weakly dependent on the applied bias. In the Gr/Si-tip device, the tip geometry greatly enhances the electric field (Fig. 1(d)), and the effect of bias on graphene becomes more pronounced. A change of the applied bias causes a shift of the graphene Fermi level and therefore affects the Schottky barrier height [2, 14], as shown in Fig. 2(a). The growing reverse saturation current of the Gr/Si-Tip device can be explained by a decrease of the Schottky barrier height, as confirmed experimentally in Fig. 2(b), where the barrier height has been estimated from equation (3) at different biases.

![Figure 2.](image)

Figure 2. (a). Band diagram of the Gr/Si junction, in forward and in reverse bias. \(E_F\) is the graphene Fermi level, \(E_S\) is the Si Fermi energy, \(E_c\) and \(E_v\) are the bottom and the top of the conduction and valence bands. \(\phi_i\) is the build-in potential and \(V\) is the applied bias. In forward (reverse) bias, the potential shifts down (up) the graphene Fermi level increasing (decreasing) the Schottky barrier height. (b) Schottky barrier height versus bias, extracted using equation (3) on a series of I-V measurements at different temperatures (Ref. [12, 14] for details).

We also studied the responsivity of both devices by shining light from the top, on the graphene layer. Fig. 3(a) and (b) show the I-V characteristics of the two devices illuminated with white LED light at different illumination levels. The responsivity is defined as:

\[
\mathcal{R} = \frac{I_{light} - I_{dark}}{P_{in}}
\]

where \(I_{light}\) and \(I_{dark}\) are the reverse currents measured under illumination and in dark, \(P_{in}\) is the incident optical power. The flat Gr/Si device showed a responsivity linearly dependent on the incident power and reached 2.5 A/W at \(V = -2.4\) V under the light intensity of 5 mW/cm\(^2\) [12], while the Gr/Si-tip junction achieved a responsivity of 3 A/W at \(V = -0.5\) V under light intensity of 3mW/cm\(^2\) (this latter value is obtained considering the effective junction area, i.e. the total Gr/Si-tips contact area) [14]. Fig. 3(c) and (d) show the ON/OFF sequence of both devices at \(V = -2.4\) V and \(V = -0.5\) V, respectively. In both cases, the rising/falling times are limited by the measurement rate of our source measurement unit (2Hz). The higher responsivity of the Gr/Si-tip device points toward of a more efficient light collection as well as to an intrinsic photocharge avalanche multiplication by impact ionization caused by the enhanced electric field at the top of the tips.
Figure 3. (a)-(b) I-V characteristic of the flat Gr/Si and Gr/Si-tip device under different illumination levels from a white LED array, whose spectrum is shown as inset of figure (b). (c)-(d) Dynamic measurement of the photocurrent at reverse bias $V = -2.4$ V for the flat Gr/Si device and $V = -0.5$ V for the Gr/Si-tip device.

Remarkably, the flat Gr/Si device displays a reverse current greater than the forward at maximum illumination level. We explain this phenomenon as due to Gr/SiO$_2$/Si MOS capacitor in parallel with the Gr/Si Schottky diode. In negative bias, the MOS capacitor accumulates photogenerated minority carriers (holes), which diffuse to the Gr/Si junction region and contribute to reverse saturation current [12, 13, 18].

4. Conclusion

In conclusion, we have fabricated two types of devices with different geometries and measured their current-voltage characteristics and responsivity to white LED light. We have extracted the Schottky parameters and compared them to each other. These Schottky barrier heights of Gr/Si Flat device is in agreement with other Gr/Si heterojunction with flat geometry, while the Schottky barrier height of the Gr/Si-tip device is slightly lower due to the mentioned barrier lowering effect. Both device show a responsivity of one order of magnitude higher Ref. [11, 18], due to the embedded MOS capacitor and the nano-tip geometry, respectively. We have highlighted some advantages of the Gr/Si-tip approach, such as the higher photoresponse due to improved light collection and internal gain, as well as the possibility of tuning the Schottky barrier height. For the Gr/Si flat junction we have shown that high responsivity can be achieved by exploiting the parallel MOS capacitor, which is naturally built together with the junction. Our study clearly shows the importance of the substrate geometry, which can be used to enable specific functionalities of the Gr/Si junction.
5. References

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Acknowledgments

We acknowledge the economic support of Regione Campania through the projects POR FSE 2014-2020, Asse III Ob. Specifico 14, Avviso pubblico decreto dirigenziale n. 80 del 31/05/2016 and L.R. num. 5/2002 Finanziamento progetti annualità 2008, Prot. 2014, 0293185, 24/04/2014.