An Approach for Drain Current Modeling Including Quantum Mechanical Effects for a DMDG Junctionless Field Effect Nanowire Transistor

N. Bora

Received: 21 May 2021 / Accepted: 15 July 2021 / Published online: 27 July 2021
© Springer Nature B.V. 2021

Abstract
This paper presents the effects of quantum confinements on the surface potential, threshold voltage, drain current, transconductance, and drain conductance of a Dual Material Double Gate Junctionless Field Effect Nanowire Transistor (DMDG-JLFENT). The carrier energy quantization on the threshold voltage of a DMDG-JLFENT is modeled, and subsequently, other parameters like drain current were analytically presented. The QME considered here is obtained under the quantum confinement condition for an ultra-thin channel, i.e., below 10 nm of Si thickness. The threshold voltage shift due to QME can be used as a quantum correction term for compact modeling of junctionless transistors. The analytical model proposed for surface potential, threshold voltage, transconductance, and drain conductance were verified by TCAD 3-D quantum simulation results which makes it suitable for SPICE compact modeling.

Keywords Quantum confinement · Drain current · Transconductance · DMDG-JLFENT · TCAD

1 Introduction

As the IC industry moves toward very low dimensions of the order of 10 nm and below the need for alternate device structure are highly desirable. To overcome the fabrication difficulty to maintain very steep junctions at low dimensions, recently, an alternate MOS structure named Junctionless transistor was proposed [1]. Several analytical models were developed for double gate junctionless transistor with symmetric gate, assymetric gates [2–7]. The quantum confinements models are also available in literature for these structures [8–10]. Even though this structure has many advantages the leakage current in the sub-threshold regime of Double Gate Junctionless Field Effect Transistors (DG JLFET) is considerably high. It flows through the center of the channel i.e., volume conduction occurs due to the low concentration of the depletion charge carriers [11, 12]. The necessity for materials with high work function (~5.6 eV) arises from turning the device properly OFF and lowering the subthreshold leakage current [13], which is technologically challenging. To overcome this problem, the use of dual material (DM) in the gate [1, 4] was suggested, enhancing the electrostatic performance of the device by incorporating a step in the surface potential profile.

In 2014, Agarwal et al. [13] proposed a pseudo-2-D surface potential model for dual material double gate junctionless field-effect transistor (DMDG-JLFET). Baruah et al. [14] presented a study on analog circuit performance of a DMDG-JLFET with a high k-spacer. Recently, Kumari et al. [11] proposed a theoretical investigation of DMDG-JLFET for analog and digital performance. Gupta et al. [15], showed that a continuous increase in the threshold voltage was observed as we move down towards sub 10 nm regime of the silicon film thickness. The growth is less prominent above 10 nm silicon thickness which occurs due to QMEs [16]. Because of the high substrate doping and ultra-thin silicon thickness, severe band bending on the substrate occurs. The narrowing of potential well in the interface is sufficient for energy quantization of the carrier [17]. As a result, the inversion charge density will get reduced at the same gate bias compared to the classical mechanically computed results. The inclusion of quantum mechanical analysis becomes necessary when the device dimensions are scaled down to 10 nm as the QME governs the...
device performances at such a small dimension. This paper has included the QME on DMDG JLFENT by incorporating the shift in threshold voltage and charge quantization effects. The analytical model results were verified with that obtained from the 3-D GENIUS Visual TCAD quantum simulation, which shows the high accuracy of our model.

2 Analytical Model

The 3-D Poisson’s equation in the channel region for the DMDG JLFENT device shown in Fig. 1(a), can be written as

\[
\frac{d^2 \psi(x,y,z)}{dx^2} + \frac{d^2 \psi(x,y,z)}{dy^2} + \frac{d^2 \psi(x,y,z)}{dz^2} = \frac{qN_{si}}{\varepsilon_{si}} \left[ \varphi(x,y,z) - V - V_T - \frac{1}{\varphi_{si}} \right],
\]

where,

\[ \psi(x,y,z) = \text{Potential at any point in the channel}, \]
\[ N_{si} = \text{Channel doping concentration}, \]
\[ \varepsilon_{si} = \text{Dielectric constant of silicon}, \]
\[ V = \text{Quasi-Fermi potential}, \]
\[ V_T = \text{Thermal voltage}, \]

As the variation along the width (z) is very less so we consider a parabolic potential profile as

\[
\psi(x,y) = \psi_s(x) + \alpha(x)y + \beta(x)y^2,
\]

where \( \psi_s(x) \) is the surface potential, \( \alpha(x), \beta(x) \) are arbitrary coefficients that are functions of ‘x’. The total channel length is \( L = 20 \text{ nm} \) and \( L_{M1} = 10 \text{ nm}, L_{M2} = 10 \text{ nm} \) is the portion of the channel under the metal \( M_1 \) and \( M_2 \), respectively.

2.1 Surface Potential Model

In DMDG JLFENT we have two different gate materials with different work functions so the flat-band voltages can be given as

\[
V_{FB1} = \phi_{M1} - \phi_{si} \quad \text{and} \quad V_{FB2} = \phi_{M2} - \phi_{si};
\]

here \( \phi_{M1}, \phi_{M2} \) are work functions of metal \( M_1, M_2 \) and \( \phi_{si} \) is that of the silicon region, respectively.

Now, the potential under the gate (\( M_1 \)) can be written as,

\[
\psi_1(x,y) = \psi_s(x) + \alpha_{11}(x)y + \beta_{12}(x)y^2. \tag{4}
\]

Similarly, the potential under the gate (\( M_2 \)) can be written as,

\[
\psi_2(x,y) = \psi_s(x) + \alpha_{21}(x)y + \beta_{22}(x)y^2. \tag{5}
\]

The Poisson’s eq. (1) under two gates can be solved using the boundary conditions:

1. The electric flux at the front gate-oxide interface is continuous,

\[
\varepsilon_{si} \frac{\partial \psi_1(x,y) = 0}{\partial y} = (V_{GS1} - V_{FB1} - \psi_s(x)) \quad \text{for} \ M_1 \tag{6}
\]

\[
\varepsilon_{si} \frac{\partial \psi_2(x,y) = 0}{\partial y} = (V_{GS2} - V_{FB2} - \psi_s(x)) \quad \text{for} \ M_2 \tag{7}
\]

here, the gate oxide capacitance is \( C_{ox} = \frac{\varepsilon_{ox}}{l_{ox(f=bs)}} \), where \( \varepsilon_{ox} \) is the dielectric constant of the oxide layer and \( l_{ox(f=bs)} \) is symmetric oxide layer thickness i.e. both front and back oxide thickness are considered to be same. Moreover, we have used high-k material HfO\(_2\) as a gate oxide which gives better results compared to SiO\(_2\) in ultra scaled transistors [18].

2. The surface potential at the interface of two different materials is continuous,

![Fig. 1](image-url)
\psi_{s1}(L_1) = \psi_{s2}(L_1).  \hspace{1cm} (8)

3. The electric field at the interface of two different materials is continuous,

\[ \frac{d\psi_1}{dx} \big|_{L_1} = \frac{d\psi_2}{dx} \big|_{L_1}. \hspace{1cm} (9) \]

Considering the extra depletion \( 'd' \) into the source region, we have the potential at the source end to be,

\[ \psi_{\text{Source}} = V - \frac{qN_{sl}d^2}{2\varepsilon_{sl}}. \hspace{1cm} (10) \]

The potential at the drain end similarly can be given as,

\[ \psi_{\text{Drain}} = V + V_{DS} - \frac{qN_{sl}d^2}{2\varepsilon_{sl}}. \hspace{1cm} (11) \]

In junctionless transistor’s high current flows before the flat band condition, we would consider full and partial depletion modes of operations that are enough for most practical applications. Poisson’s equation neglecting mobile charge in depletion mode \((V_{GS} < V_{Th})\) can thus be written as,

\[ \frac{\partial^2 \psi(x,y)}{\partial x^2} + \frac{\partial^2 \psi(x,y)}{\partial y^2} = \frac{qN_{sl}}{\varepsilon_{si}}, \hspace{1cm} (12) \]

due to symmetry, the electric field at the center is zero thus

\[ \frac{\partial \psi(x,y) = -t_{si}/2}{\partial x} = 0. \hspace{1cm} (13) \]

The coefficients \(\alpha_j(x), \beta_j(x)\)can be obtained from the (6), (7), and (13) where \(j = 1, 2\). Using the values of coefficients in (4) and (5) and then substituting the potentials in (12) we have,

\[ \frac{\partial^2 \psi_j}{\partial x^2} - a_j \psi_j = b_j, \hspace{1cm} (14) \]

\[ a_j = \frac{C_{ox}}{t_{si}\varepsilon_{si}}, \hspace{1cm} \beta_j = -\frac{qN_{sl}}{\varepsilon_{si}} + A \left(V_{GS} - \psi_{M_j} + \psi_{S_j}\right), \hspace{1cm} (15) \]

When \(V_{Th} < V_{GS} < V_{FB}\), the transistor operates in partial depletion mode during which a neutral region starts to develop in the middle of the device. Taking the origin to be at the center of the device, the electric field and depletion thickness \(y_d\) can be calculated as [13],

\[ E_0 = \frac{\partial \psi(x,y = y_d)}{\partial y} = -\frac{8V_Ty_d}{r_{si}^2}, \hspace{1cm} (16) \]

\[ y_d = \frac{-m + \sqrt{m^2 - 4nl}}{2l}, \hspace{1cm} (17) \]

where,

\[ l = \frac{qN_{sl}}{2\varepsilon_{si}} + \frac{8V_T}{r_{si}^2}, \hspace{1cm} m = \frac{qN_{sl}}{\varepsilon_{ox}} + \frac{8\varepsilon_{si}V_T}{C_{ox}r_{si}^2}, \hspace{1cm} n = V_{GS} - V_{FB} - V + V_T \]

The potential in the neutral region follows a simple parabolic potential approximation [19], where the potential at the center \((V_C)\) of the device can be approximated as,

\[ \psi(x,y = -t_{si}/2) = V_C. \hspace{1cm} (18) \]

The coefficients \(\alpha_j(x), \beta_j(x)\) are deduced from the boundary conditions (8), (9), and (18). Substituting their corresponding values in (4) and (5) and then from (12), we obtain,

\[ \frac{\partial^2 \psi_j}{\partial x^2} - a_j \psi_j = b_j, \hspace{1cm} (19) \]

where,

\[ a = \frac{C_{ox}}{y_d\varepsilon_{si}} \hspace{1cm} \text{and} \hspace{1cm} b_j = -\left[\frac{qN_{sl}}{\varepsilon_{si}} + A \left(V_{GS} - \psi_{M_j} + \psi_{S_j}\right)\right], \hspace{1cm} (15) \]

For \(j = 1, 2\).

2.2 Combination of Operating Modes

As the gate work functions are different \((\psi_{M1} > \psi_{M1})\), thus the threshold and the flatband voltages for the gate under metal \(M_1\) \((G_{M1})\) are higher than that of the gate under metal \(M_2\) \((G_{M2})\). When we apply gate voltage, the corresponding channel region may be in different modes of operations. The first useful combination is the full depletion under \(G_{M1}\) and partial depletion under \(G_{M2}\). Under this condition, the surface potentials are,

\[ \psi_{s1}(x) = C_1e^{x/L_1} + D_1e^{-x/L_1} - \frac{b_1}{a}, \hspace{1cm} 0 \leq x \leq L_1, \hspace{1cm} (20) \]

\[ \psi_{s2}(x) = C_2e^{x/L_2} + D_2e^{-x/L_2} - \frac{b_2}{a}, \hspace{1cm} \text{for} \hspace{1cm} 0 \leq x \leq L_2 \hspace{1cm} (21) \]

where the coefficients are deduced using the boundary conditions eqs. (6–9).

Similarly, the surface potential for the second possible combination, i.e., channel region under both the gates \(G_{M1}\) and \(G_{M2}\), is in partial depletion. It happens when gate voltage crosses the threshold voltage of \(G_{M1}\).

 Springer
2.3 Threshold Voltage Model

Substituting \( y_d = -t_{si}/2 \) in eq. (17) and solving for the gate voltage, we get the threshold voltage as,

\[
V_{Th} = V_{FB} - \frac{qN_{si}t_{si}^{2}}{8\varepsilon_{si}} - \frac{qN_{si}t_{ox}}{2\varepsilon_{ox}}V_{T} + V_{c} - 3V_{T} - \frac{4C_{si}}{C_{ox}}V_{T}.
\]  

(22)

2.4 Inclusion of Quantum Mechanical Effect

In the subthreshold region of junctionless transistors, the channel is fully depleted, the channel potential is bent, and electrons are preferentially confined at the center of the channel. The Schrödinger’s equation can be decoupled from the Poisson’s equation by neglecting the mobile charge term in the Poisson’s equation, when \( t_{si} \) is large the discrete subband energy levels are mostly confined between the bent portion of the conduction band boundaries. In this case, the system is similar to a quantum harmonic oscillator (QHO) with an energy potential given as [17],

\[
V_{QM} = \frac{q^2N_{si}x^2}{2\varepsilon_{si}}.
\]  

(23)

Using the effective-mass approximation, the discrete subband energy levels can be expressed as

\[
E_{k,n} = \left(n + \frac{1}{2}\right)\frac{h}{2\pi} \sqrt{\frac{q^2N_{si}}{m^*c_k\varepsilon_{si}}}.
\]  

(24)

where \( n \) is a quantum number \((n = 0, 1, 2, 3,...)\), and \( h \) is the Planck’s constant. When the \( t_{si} \) is small, the discrete sub-band energy levels for this case are expressed by [17],

\[
E_{k,n} = \frac{\hbar^2n^2}{8m^*_{c,k}t_{si}^2} + \frac{q^2N_{si}t_{si}^{2}}{24\varepsilon_{si}} \left(1 - \frac{6}{\pi^2n^2}\right),
\]  

(25)

where, \( k = 1 \) and \( 2; n = 1, 2, 3, ... \).

The quantum shift in threshold voltage is incorporated by the energy quantization of the carriers in a channel. In a silicon crystal with \(<100>\) orientation, six valleys in the conduction band clustered into two separate groups with degeneracy factors \( g_1 = 2 \) and \( g_2 = 4 \), respectively [20].

Quantum Shift in threshold voltage can then be expressed as [20],

\[
\Delta V_{QM}^{Th} = kT\ln\left[\frac{\left(\frac{k^2N_{c}}{4\varepsilon_{si}^{3/2}}\right)}{2\sqrt{\pi}}\right],
\]  

where,

\[
\Delta V_{QM}^{Th} = \frac{kT}{q}\ln\left[\frac{\pi^{1/2}}{2\varepsilon_{si}^{3/2}}\frac{k^2N_{c}}{qN_{si}t_{si}}\right].
\]  

The quantum shift in threshold voltage can then be expressed as

\[
\psi_{s'i}(x) = C_{s'}e^{i(x-L_{j})} + D_{s'}e^{-i(x-L_{j})} + \frac{b'_{j}}{a}; \quad j = 1, 2
\]  

(28)

where,

\[
V_{Cl+QM}^{Th} = V_{Cl}^{Th} + \Delta V_{QM}^{Th}.
\]  

(27)

Thus surface potential becomes

\[
V_{QM}^{Th} = V_{QM}^{Th} + \psi_{s'i}(x).
\]  

The eq. (28) gives the surface potential with QME. However, it can be noted that while carrying out investigations, the QME is assumed to be uniform throughout the channel.

2.5 Drain Current and Transconductance Model

The drain current equation for DMDG JLFENT, including the quantum effect, can be obtained by using (27) for threshold voltage in linear and saturation regions of operations as

\[
I_{Dlin} = \kappa \left(\frac{V_{GS} - V_{Th}^{Cl+QM}}{V_{DS} - \frac{V_{DS}^2}{2}}\right),
\]  

(29)

\[
I_{Dsat} = \kappa \left(\frac{V_{GS} - V_{Th}^{Cl+QM}}{V_{DS} - \frac{V_{DS}^2}{2}}\right)^2,
\]  

(30)

where, \( \kappa = \mu_C C_{ox}(W/L) \).

The gate transconductance equation is obtained from (30) as

\[
g_{m} = \frac{dI_{D}}{dV_{GS}} = \kappa \left(\frac{V_{GS} - V_{Th}^{Cl+QM}}{V_{DS} - \frac{V_{DS}^2}{2}}\right).
\]  

(31)

The drain conductance equation is obtained from (29) as

\[
g_{ds} = \frac{dI_{D}}{dV_{DS}} = \kappa \left(\frac{V_{GS} - V_{Th}^{Cl+QM}}{V_{DS} - \frac{V_{DS}^2}{2}}\right)^2.
\]  

(32)
3 Results and Discussion

To validate the semi-analytical model for threshold voltage, drain current, and transconductance, the results were compared with that obtained from GENIUS 3-D TCAD software [21]. Figure 1(b) shows the 3D device structure with mesh distribution used for simulation. To include the dependence on the impurity concentrations and the transverse and longitudinal electric field values Lombardi mobility model is employed. Carrier trapping, the DIBL, the Shockley-Read-Hall recombination model, and Fermi-Dirac carrier statistics with impact ionization is utilized in the simulations. The quantum mechanical effect can be modeled using the density gradient technique [22]. The QME model is based on the Wigner Function Equations of motion moments, which consists of quantum correction to the carrier current equations. The corrected carrier current equations and their derivatives are pretty sensitive to low carrier concentrations. The doping concentration of the entire Silicon region is $5 \times 10^{19} \text{ cm}^{-3}$ and the work function of the gate metals $M_1$ and $M_2$ are considered as 5.4 eV and 4.7 eV, respectively. We have considered very high doping in the channel which is required for sufficient current to flow through the device, unlike traditional junction based transistor where current flows through the surface and

![Fig. 2 Surface Potential along the channel with thickness of 10 nm](image1)

![Fig. 3 Surface Potential along the channel with a thickness of 6 nm](image2)
hence subject to surface roughness and scattering which are absent in the junctionless transistor as volume current conduction occurs. Throughout the paper the oxide thickness is considered to be 2 nm unless mentioned. The GENIUS VTCAD 3D quantum simulation results are shown as symbols, and the thick lines represent the results obtained from our analytical model for all results illustrated in this paper.

Figure 2-3, shows the surface potential variations with $V_{GS}$ for two different values of silicon thickness of 10 nm and 6 nm, respectively. In both the figures, we can observe a step increase in the surface potential due to the use of two dissimilar metals having different work functions. As the work function increases, the surface potential decreases; thus the surface potential under the gate $G_{M1}$ is lower than that of the gate $G_{M2}$. Figure 2, where silicon thickness is 10 nm, shows the surface potential bent is more prominent under the gate $G_{M1}$ due to higher work function difference, thereby controlling the threshold voltage, therefore the name control gate. When $V_{GS}$ is 0 V, the bent is highest and the region under $G_{M1}$ is fully depleted and under $G_{M2}$ is partially depleted. As the $V_{GS}$ increases the bent decreases and at 0.6 V the region under $G_{M1}$ is partially depleted and under $G_{M2}$ is near flat band. In fig. 3, the silicon thickness is considered 6 nm; the bent is more prominent than that of 10 nm at any given $V_{GS}$, which can be explained based on higher QME or confinement effect with a decrease in silicon thickness. The quantum effect is more prominent since...
the electron concentration peaks below the silicon-oxide interface and goes nearly zero at the interface, which is entirely in contrast to the classical model. Classically, the electron concentration peaks at the surface. The bending that occurred in the curve at the end portion is due to the inclusion of \( d_S \) (depletion towards source region) and \( d_D \) (depletion towards drain region) in our analytical model. In both cases the model shows excellent agreement with that of the quantum simulation results of 3-D VTCAD software.

Figure 4, shows the surface potential variations along the channel for different values of silicon thickness from 4 nm to 10 nm, while \( V_{DS} \) kept at 0.5 V and \( V_{GS} \) kept at 0.4 V, respectively. Here we can observe that as the silicon thickness decreases from 10 nm down towards 4 nm, the bend in the surface potential contours also increases and this happens because of a higher control of gate over the channel, and the charge carriers become more and more confined due to higher QME.

The transfer characteristics of the DMDG JLFENT were plotted in Fig. 5-7. The variation of the drain current to the gate voltage is shown in Fig. 5. While \( V_{DS} \) was kept constant, the silicon thickness was varied from 10 nm down to 4 nm. Here we can observe that, as silicon thickness decreases, the drain current reduces for the same value of \( V_{GS} \). Moreover, we
can observe that at 4 nm, the curve is not smooth because of distortion that occurred due to the high confinement effect or QME. Figure 6, shows the same plot on a semi-logarithmic scale, reflecting the low leakage current in smaller silicon body thickness due to better control of the gate over the channel. Figure 7, shows the variation of the drain current regarding $V_{DS}$ where $V_{GS}$ was kept constant at 0.5 V and silicon thicknesses are being varied. Here we can note that as silicon thickness decreases, the drain current reduces, which is evident for reduced charged carriers and confinement effects. In all the cases Fig. 5-7, the model is in good agreement with quantum simulation results of 3-D VTCAD software.

The transconductance for varying silicon thickness model was plotted in Fig. 8; we can observe that the plot for $T_{Si}$ of 4 nm is low up to the threshold voltage and increases just after crossing it. This may be because of the very high confinement effect as compared to others. Figure 9, shows the drain conductance model for various silicon thicknesses where we can observe that the conductance was low for lower dimensions owing to lower corresponding drain currents. In both cases,
the model shows excellent agreement with that of the quantum 3D TCAD simulation results.

4 Summary

This paper investigated the effects of quantum confinements on the several key parameters of a DMDG-JLFENT. The carrier energy quantization on the threshold voltage of a DMDG-JLFENT is analytically modeled. The QME considered here is obtained under the quantum confinement condition for an ultra-thin channel, i.e., below 10 nm of Si thickness. Based on the shifts in threshold voltage, the change in drain current, transconductance, and drain conductance with quantum effects were modeled. The analytical model proposed for surface potential, threshold voltage, drain current, transconductance, and drain conductance were verified by GENIUS Cogenda VTCAD 3-D quantum simulation results. The model is thereby suitable for compact modellings.

Acknowledgments The author is highly thankful to the Dr. R. Subadar, HOD, Department of Electronics and Communication Engineering, NEHU Shillong for providing the software support in carrying out this work.

Author Contribution All work carried out by the author N. bora.

Funding The authors did not receive support from any organization for the submitted work.
• No funding was received to assist with the preparation of this manuscript.
• No funding was received for conducting this study.
• No funds, grants, or other support was received.

Data Availability There are no linked data or material to this submission.

References

1. Colinge JP, Kranti A, Yan R, Lee CW, Feraun I, Yu R, Dehdashti Akhavan N, Razavi P (2011) Junctionless nanowire transistor (JNT): properties and design guidelines. Solid State Electron 65–66:33–37. https://doi.org/10.1016/j.sse.2011.06.004
2. Raiabarua AK, Sama KC (2021) A potential model for parallel gated Junctionless field effect transistor. Silicon. https://doi.org/10.1007/s12633-020-00890-8
3. Jazaeri F, Makris N, Saeidi A, Bucher M, Sallese JM (2018) Charge-based model for junction FETs. IEEE Trans Electron Devices 65:2694–2698. https://doi.org/10.1109/TED.2018.2830972
4. Shin YH, Weon S, Hong D, Yun I (2017) Analytical model for Junctionless double-gate FET in subthreshold region. IEEE Trans Electron Devices 64:1433–1440. https://doi.org/10.1109/TED.2017.2664825
5. Bora N, Das P, Subadar R (2016) An analytical universal model for symmetric double gate junctionless transistors. J Nano- Electron Phys 8:02003–1–02003–4. https://doi.org/10.21272/jnep.8(2).02003
6. Chandra K, Sarma D, Sharma S et al (2015) An approach for complete 2-D analytical potential modelling of fully depleted symmetric double gate junction less transistor. J Comput Electron 14:717–725. https://doi.org/10.1007/s10825-015-0706-0
7. Bora N, Subadar R (2019) A complete analytical model of surface potential and drain current for an ultra Short Channel double gate asymmetric Junctionless transistor. J Nanoelectron Optoelectron 14:1283–1289. https://doi.org/10.1166/jno.2019.2643
8. Bora N, Deka N, Subadar R (2020) Quantum mechanical analysis on modeling of surface potential and drain current for nanowire jfet. J Nano Res 64:123–134. https://doi.org/10.4028/www.scientific.net/JNanoR.64.123
9. Shalchian M, Jazaeri F, Sallese JM (2018) Charge-based model for ultrathin Junctionless DG FETs, including quantum confinement. IEEE Trans Electron Devices 65:4009–4014. https://doi.org/10.1109/TED.2018.2854905
10. Bora N, Baruah RK (2011) Quantum mechanical treatment on modeling of drain current, capacitances and transconductances for thin film undoped symmetric DG MOSFETs. IEEE Int Conf Nanosci Technol Soc Implice NSTSI11 1–6, https://doi.org/10.1109/NSTSI.2011.6111994
11. Kumari V, Modi N, Saxena M, Gupta M (2015) Theoretical investigation of dual material junctionless double gate transistor for analog and digital performance. IEEE Trans Electron Devices 62:2098–2105. https://doi.org/10.1109/TED.2015.2433951
12. Wang Y, Shan C, Dou Z, Wang LG, Cao F (2015) Improved performance of nanoscale junctionless transistor based on gate engineering approach. Microelectron Reliab 55:318–325. https://doi.org/10.1016/j.microrel.2014.11.009
13. Agrawal AK, Koutilya PNVR, Jagadesh Kumar M (2015) A pseudo 2-D surface potential model of a dual material double gate junctionless field effect transistor. J Comput Electron 14:686–693. https://doi.org/10.1007/s10825-015-0710-4
14. Baruah RK, Paity RP (2014) A dual-material gate junctionless transistor with high-k spacer for enhanced analog performance. IEEE Trans Electron Devices 61:123–128. https://doi.org/10.1109/TED.2013.2292852
15. Gupta S, Ghosh B, Rahi SB (2015) Compact analytical model of double gate junction less field effect transistor comprising quantum-mechanical effect. J Semiconductor 36:1–6. https://doi.org/10.1088/1674-4926/36/2/024001
16. Yu B, Wang L, Yuan Y, Asbeck PM, Taur Y (2008) Scaling of nanowire transistors. IEEE Trans Electron Devices 55:2846–2858. https://doi.org/10.1109/TED.2008.2005163
17. Duarte JP, Kim MS, Choi SJ, Choi YK (2012) A compact model of quantum electron density at the subthreshold region for double-gate junctionless transistors. IEEE Trans Electron Devices 59:1008–1012. https://doi.org/10.1109/TED.2012.2185827

18. Boro UC, Bora N, Pegu PA, Subadar R (2017) Impact of temperature on the performance of sub-35nm symmetric double gate Junctionless transistor based inverter using high-K gate dielectric, a TCAD simulation study. In: 1st IEEE international conference on power electronics, intelligent control and energy systems, ICPEICES 2016

19. Duarte JP, Choi SJ, Choi YK (2011) A full-range drain current model for double-gate junctionless transistors. IEEE Trans Electron Devices 58:4219–4225. https://doi.org/10.1109/TED.2011.2169266

20. Y. Taur and T. H. Ning, Taur Y, Ning TH (2009) Fundamentals of modern VLSI devices, 2nd ed. Cambridge University Press

21. (2014) Cogenda Pte Ltd., Genius, 3-D Device Simulator, Reference Manual, 1.9.3. Singapore

22. Garcia-Loureiro AJ, Seoane N, Aldegunde M, Valin R, Asenov A, Martinez A, Kalna K (2011) Implementation of the density gradient quantum corrections for 3-d simulations of multigate nanoscaled transistors. IEEE Trans Comput Des Integr Circuits Syst 30:841–851. https://doi.org/10.1109/TCAD.2011.2107990

Publisher’s Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.