Abstract

We introduce a denotational semantic framework for shared-memory concurrent programs in a C11-style memory model. This denotational approach is an alternative to techniques based on “execution graphs” and axiomatizations, and it allows for compositional reasoning. Our semantics generalizes from traces (sequences of actions) to pomsets (partial orders of actions): instead of traces and interleaving, we embrace “true” concurrency. We build on techniques from our prior work that gives a denotational semantics to SPARC TSO. We add support for C11’s wider range of memory orderings, e.g., acquire-release and relaxed, and support for local variables and various synchronization primitives, while eliminating significant amounts of technical bookkeeping. Our approach features two main components. We first give programs a syntax-directed denotation in terms of sets of pomsets of memory actions. We then give a race-detecting executional interpretation of pomsets using footprints and a local view of state.

Keywords: C11, denotational semantics, pomsets, concurrency, weak memory models.

1 Introduction

A memory model specifies which values can be read by memory accesses. C11-style memory models allow the programmer to specify if a given memory location should be acted on atomically or non-atomically [10]. Atomic memory locations are intended to be used for inter-thread communication and synchronization. Every atomic memory action has a programmer-chosen memory ordering tag. The action’s memory ordering specifies the visibility of actions sequenced before or after it to other actions that synchronize with it. Intuitively, the memory ordering stipulates how the memory action can be reordered with other actions in the same thread. Following Lahav et al. [10], we differ from C11 and do not treat unsequenced races between atomic accesses to the same location as undefined behaviour. In contrast, multiple concurrent accesses to a non-atomic location, at least one of which is a write, constitutes a race and is regarded as undefined behaviour, because reading...
from a non-atomic location could retrieve a value from an intermediate state. Memory actions on non-atomic locations can be compiled to normal memory accesses, cheaper to perform than their atomic counterparts.

We provide a denotational framework for exploring C11-style memory models. We did not set out to exactly capture any particular account of the C11 memory model for two reasons. First, because the literature presents many different accounts of the C11 memory model (e.g., [2,10,13]), each addressing various shortcomings, we believe it is better to develop a generic framework in which we can study various formulations. Second, C11 has some features, such as consume accesses, that we deem are premature or introduce excessive complexity with little gain.

Our framework has two major components. In Section 3, we give a denotational (and hence compositional) account of a C11-style memory model. Each program is given a set of pomsets (a generalization of traces) as its denotation using various composition operators designed to capture exactly the per-thread memory reorderings permitted by the memory model. In Section 4, we give these pomsets an executional interpretation inductively defined on the structure of the pomset, using a local view of state. This interpretation is carefully constructed to respect synchronization constraints provided by the memory model and it is race-detecting.

2 An Informal Account

Each type of memory location has an associated set of actions. Non-atomic locations can be read from and written to. Atomic locations can additionally be acted on with atomic read-modify-write actions. There are memory operations that involve no locations. For example, a fence is a special atomic memory action that acts as a barrier against reordering. All atomic operations have an associated memory ordering tag chosen by the programmer.

The strongest ordering on atomic actions is sequential consistency, denoted by the tag sc. An sc action cannot be reordered with any other action, and every execution induces a total order on the sc actions. Though sc actions are expensive to implement, they allow the programmer to reason via an interleaving semantics. All atomic memory actions can use this ordering.

The release-acquire memory ordering paradigm gives lightweight synchronization between threads. No memory action sequenced before a release (rel) write can be reordered to after the write. Symmetrically, no action sequenced after an acquire (acq) read can be reordered to before the read. The intended semantics is that any action after an acquire read that “synchronizes with” a release write to the same atomic location sees the effects of all actions that occurred before the write. Fences and atomic read-modify-write actions, such as locking primitives, can use the acquire-release (ar) ordering. These actions behave both as an acquire read and a release write. A key difference from sc is that executions need not induce a total order on ar actions.

The weakest memory ordering we consider is relaxed (rlx). It imposes no additional constraints on reordering and only guarantees atomicity.

It is helpful to visualize the relative strength of these memory orderings using...
the following diagram by Lahav et al. [10]:

\[
\begin{array}{c}
na \xrightarrow{\text{rlx}} \xrightarrow{\text{acq}} \xrightarrow{\text{ar}} \xrightarrow{\text{sc}} \\
\xrightarrow{\text{rel}} \xrightarrow{\text{acq}} \xrightarrow{\text{rlx}} \xrightarrow{\text{ar}} \xrightarrow{\text{sc}}
\end{array}
\]

A key desideratum is that executing a single sequential thread under our memory model should produce the same result as execution without any reorderings. This implies that at no point may we reorder memory actions to the same location within a given thread. We also want coherence, i.e., the property that writes to the same location appear in the same order to all threads. Our model should further respect data dependencies: whenever we write the value of an expression to a location, any reads required to evaluate that expression must be ordered before the write.

We illustrate these principles and the interplay between the release and acquire orderings using a simple message-passing example. Consider executing the program

\[
x := \text{na} 42 ; y := \text{rel} 1 \parallel (\text{while } y_{\text{acq}} = 0 \text{ do skip}) ; z := \text{rlx } x_{\text{na}}
\]

from an initial state where all locations are initialized to 0. The fact that the write to \(y\) is a release and the reads from \(y\) are acquires guarantees that after the while loop terminates, the read from \(x\) will see the value 42. We make these dependencies explicit by means of diagrams, where an arrow \(a \rightarrow b\) indicates that memory action \(a\) is sequenced before \(b\), and \(a \rightarrow a\) abbreviates \(a \rightarrow a \rightarrow \cdots \rightarrow a\):

\[
x := \text{rlx} 42 \rightarrow y := \text{rel} 1 \quad y_{\text{acq}} = 0 \rightarrow y_{\text{acq}} = 0 \rightarrow x_{\text{rlx} 42} \rightarrow z := \text{rlx} 42
\]

Had all of the actions been tagged with the \(\text{rlx}\) ordering, the compiler could have reordered the writes to \(x\) and \(y\) because they do not depend on each other, and then the read from \(x\) could have returned 0 instead of 42, giving us

\[
x := \text{rlx} 42 \quad y := \text{rlx} 1 \quad y_{\text{rlx}} 0 \rightarrow y_{\text{rlx}} 0 \rightarrow x_{\text{rlx} 42} \rightarrow z := \text{rlx} 42
\]

We pause to remark that the reads from \(y\) are still ordered before the read from \(x\): this is because there is a control-flow dependency between the read \(y_{\text{rlx}}\) from the loop test and the write \(z := \text{rlx } x_{\text{rlx}}\) immediately following. Preserving control-flow dependencies will be important for eliminating various thin air behaviours.

3 Denotational Semantics

We make our informal account precise using a denotational semantics. Its chief advantage is compositionality: the meaning (or denotation) of a program in the memory model is determined by the denotations of its subphrases. This allows for modular reasoning and the validation of various program-level optimizations. The denotations of programs will be order structures on syntactic objects called “memory actions”. These order structures, called partially-ordered multisets (pomsets), generalize traces and are an abstract description of the program’s memory accesses.
We specify a simple imperative language with while loops, fences, local variables, and atomic read-modify-write actions. These features were chosen to illustrate the principles underlying our approach, but the details of the language are not important. We assume meta-variables for disjoint sets of identifiers \( a \in \text{Ide}_{at} \) (atomic assignable identifiers) and \( n \in \text{Ide}_{na} \) (non-atomic assignable identifiers) and we let \( x, y \) range over the set \( \text{Ide} = \text{Ide}_{at} \cup \text{Ide}_{na} \) of all identifiers. Finally, we let \( v \in V = \mathbb{Z} \) (integer values) and \( f \) range over partial functions of type \( V \to V \).

The abstract syntax of our language is given by the following grammar:

\[
\begin{align*}
\alpha & ::= \text{rlx} | \text{rel} | \text{acq} | \text{ar} | \text{sc} \\
\mu & ::= \text{na} | \alpha \\
e & ::= v | a_{\alpha \notin \{\text{rel, ar}\}} | n_{\text{na}} | \text{rmw}(a_\alpha; f) | e_1 + e_2 | \cdots \\
b & ::= \text{true} | \neg b | b_1 \lor b_2 | e_1 < e_2 | \cdots \\
c & ::= \text{skip} | a := a_{\alpha \notin \{\text{acq, ar}\}} | n := n_{\text{na}} | e | n_{\text{na}} e | \text{fence}_{\text{rlx}} | \text{rmw}_\alpha(a; f) \\
& \quad \mid \text{local } n_{\text{na}} = v \text{ in } c | c_1 ; c_2 | \text{if } b \text{ then } c_1 \text{ else } c_2 | \text{while } b \text{ do } c \\
p & ::= c | p ; p \\
\end{align*}
\]

The meta-variables are \( e \in \text{Exp}_{\text{int}} \) (integer expressions), \( b \in \text{Exp}_{\text{bool}} \) (boolean expressions), \( c \in \text{Cmd} \) (commands), and \( p \in \text{Prog} \) (programs). We abuse notation and use subscripts such as \( > \mu \) to mean all memory orderings \( \mu' \) such that \( \mu' > \mu \). Though the phrase \( \text{rmw}(a_\alpha; f) \) is used both as an expression and a command, context will make its syntactic class unambiguous. In examples, we let the associated memory order tag determine whether an identifier corresponds to an atomic or non-atomic assignable.

Our semantic clauses will transform our language’s syntactic phrases into sets of memory action pomsets. A (memory) action \( \lambda \) is a syntactic object representing an action on the store. Memory actions are given by the following:

\[
\begin{align*}
\lambda & ::= \delta \quad \text{(no-op)} \\
& \quad | n := n_{\text{na}} v \quad \text{(non-atomic write)} \\
& \quad | a := a v \quad \text{(atomic write, } a \in \{\text{rlx, rel, sc}\}) \\
& \quad | n = n_{\text{na}} v \quad \text{(non-atomic read)} \\
& \quad | a = a v \quad \text{(atomic read, } a \in \{\text{rlx, acq, sc}\}) \\
& \quad | \text{fence}_\alpha \quad \text{(atomic fence, } a > \text{rlx}) \\
& \quad | \text{rmw}_\alpha(a; v, v') \quad \text{(atomic read-modify-write: read } v \text{ and write } v') .
\end{align*}
\]

Let \( \mathcal{A} \) be the set of all actions and let \( \text{Mo} \) and \( \text{Ide} \) be the (partial) projections from \( \mathcal{A} \) to memory orderings and \( \text{Ide} \), respectively. Given a predicate \( \pi \) on \( \mathcal{A} \), let \( \mathcal{A}_\pi \) be the set of actions satisfying \( \pi \). For example, \( \mathcal{A}_{< \mu} \) is the set of all actions \( \lambda \) such that \( \text{Mo}(\lambda) < \mu \). Special cases are the set \( \mathcal{A}_\mu \) of all memory actions with memory ordering \( \mu \), the set \( \mathcal{A}_r \) of all reading actions \( (i = \mu v \text{ and rmw}_\alpha(a; v, v')) \), the set \( \mathcal{A}_w \) of all writing actions \( (i := \mu v \text{ and rmw}_\alpha(a; v, v')) \), the set \( \mathcal{A}_f \) of fence actions, and the set \( \mathcal{A}_x \) of all actions involving the identifier \( x \).

A pomset over a set of labels \( L \) is a triple \((P, <, \Phi)\) where \((P, <)\) is a strict partial order satisfying the finite-height property and \( \Phi : P \to L \) is a labelling function. A
partial order \((P, <)\) satisfies the **finite-height property** if for all \(p \in P\), the set \(\{q \in P \mid q < p\}\) is finite. Because our pomsets describe orderings between a program’s memory actions, the finite-height property implies that we have no unreachable actions in our pomset, i.e., that every action could in principle be executed. As is typical with mathematical structures, we call a pomset by its underlying set, and given a pomset \(P\), we let \(<_P\) and \(\Phi_P\) denote its obvious components. We denote by \(\text{Pom}(L)\) the set of pomsets over \(L\). We typically refer to pomset elements by their labels, relying on context to disambiguate which underlying element we mean. In fact, the underlying elements carry no meaning, and we identify pomsets \(P, Q \in \text{Pom}(L)\) whenever there exists an order-isomorphism \(\Psi : (P, <_P) \to (Q, <_Q)\) respecting labels, i.e., satisfying \(\Phi_Q \circ \Psi = \Phi_P\). We can identify pomsets and labelled directed acyclic graphs, as we did in Section 1, where we have an edge \(\Phi(a) \to \Phi(b)\) if and only if \(a < b\). We say a pomset \(P\) is **linear** if \(<_P\) is a total order.

We further identify non-empty pomsets \(P, Q \in \text{Pom}(A)\) whenever there exists a non-empty pomset \(R \in \text{Pom}(A)\) such that \(R\) can be obtained from \(P\) and from \(Q\) by deleting finitely many \(\delta\) actions.\(^3\) This is akin to closure under stuttering and mumbling in trace semantics (cf. [6]), and our semantics is well-defined relative to it.

Our semantic clauses assign sets of pomsets to syntactic phrases, and compositionality requires us to be able to compose the pomsets from subphrases to form the denotation of a phrase. The **sequential composition** \((P_1, <_1, \Phi_1) \circ (P_2, <_2, \Phi_2)\) of pomsets \(P_1\) and \(P_2\) is \((P_1 \sqcup P_2, <, \Phi_1 \sqcup \Phi_2)\) when \(P_1\) is finite, where \((i, p) < (j, q)\) if and only if \(i = j\) and \(p <_1 q\), or \(i < j\), and where \((\Phi_1 \sqcup \Phi_2)(i, p) = \Phi_i(p)\). Intuitively, this orders everything in \(P_1\) before everything \(P_2\) while preserving their internal orderings. When \(P_1\) is infinite, \(P_1 \circ P_2 = P_1\). The finiteness check on \(P_1\) ensures \(P_1 \circ P_2\) satisfies the finite-height property. The **parallel composition** \((P_1, <_1, \Phi_1) \parallel (P_2, <_2, \Phi_2)\) of pomsets \(P_1\) and \(P_2\) is given by \((P_1 \sqcup P_2, <, \Phi_1 \sqcup \Phi_2)\) where \((i, p) < (j, q)\) if and only if \(i = j\) and \(p <_1 q\). It is straightforward to check that these compositions are all associative with the empty pomset \(0 = (\emptyset, \emptyset, \emptyset)\) as their unit. They lift to sets of pomsets in the obvious manner.

The denotation of an integer expression is a subset of \(\text{Pom}(A) \times V\) inductively defined on the syntax of the expression:

\[
\begin{align*}
P(v) &= \{(\{\delta\}, v)\} \\
P(x_{\mu}) &= \{(\{x = \mu\ v\}, v) \mid v \in V\} \\
P(\text{rmw}_\alpha(a; f)) &= \{(\{\text{rmw}_\alpha(a; v; v')\}, v') \mid (v, v') \in \text{graph}(f)\} \\
P(e_1 + e_2) &= \{(P_1 \parallel P_2, v_1 + v_2) \mid (P_i, v_i) \in P(e_i)\}\end{align*}
\]

The \(x_{\mu}\) clause has a pomset \(\{x = \mu\ v\}\) for each possible value \(v\) that could be read from \(x\). We must allow for all possible values to get compositionality: we do not know a priori which writes an expression may be composed, and hence do not know what values might be read from \(x\). The \(\text{rmw}_\alpha(a; f)\) clause is analogous and captures the atomic nature of the read-modify-write by treating it as a single memory action, rather than a sequenced read-write pair. We indicate that we

\(^3\) Formally, the **deletion** of \(S \subseteq P\) from \(P\) is given by \((P \setminus S, <_P \cap ((P \setminus S) \times (P \setminus S))), \Phi \mid (P \setminus S))\). Deleting finitely many \(\delta\) actions from \(P\) means deleting a finite subset of \(\Phi_P^{-1}(\delta)\) from \(P\).
compute the $e_i$ in $e_1 + e_2$ in parallel by combining the memory actions $P_i$ with a parallel composition.

The denotation of a boolean expression is a subset of $\text{Pom}(A) \times \text{Bool}$ and is defined analogously. To simplify the clauses with conditionals, we introduce the helper definitions $\mathcal{P}(b)_{\text{true}} = \{ P \mid (P, \text{true}) \in \mathcal{P}(b) \}$ and the analogous $\mathcal{P}(b)_{\text{false}}$.

The denotation of a program $p$ is a subset of $\text{Pom}(A)$ inductively defined on its syntax: $\mathcal{P}(p \parallel c) = \mathcal{P}(p) \parallel \mathcal{P}(c)$. The denotation of a command $c$ is a subset of $\text{Pom}(A)$, also inductively defined on its syntax. The basic commands are given by:

$$
\mathcal{P}(\text{skip}) = \{ \delta \} \\
\mathcal{P}(x :=_\mu e) = \{ P ; \{ x :=_\mu v \} \mid (P, v) \in \mathcal{P}(e) \} \\
\mathcal{P}(\text{fence}_\alpha) = \{ \{ \text{fence}_\alpha \} \} \\
\mathcal{P}(\text{rmw}_\alpha(a; f)) = \{ \{ \text{rmw}_\alpha(a; v; v') \} \mid (v, v') \in \text{graph}(f) \}
$$

The only interesting clause here is for $x :=_\mu e$, where data dependency requires that the corresponding write be sequenced after all actions performed in computing $e$.

Before we can give semantic clauses for compound commands, we must introduce the relaxed sequential composition. The relaxed composition of two pomsets orders actions from the first before those of the second only when required by the memory model. To make this precise, we introduce the following predicates. $\text{IsAcq}(\lambda)$ holds if and only if $\lambda \in A_r \cup A_f$ and $\text{Mo}(\lambda) \geq \text{acq}$. $\text{IsRel}(\lambda)$ holds if and only if $\lambda \in A_r \cup A_f$ and $\text{Mo}(\lambda) \geq \text{rel}$. Actions $\lambda$ and $\lambda'$ are memory-ordered, $\text{Ord}(\lambda, \lambda')$, if and only if $\text{Id}(\lambda) = \text{Id}(\lambda')$, $\text{IsAcq}(\lambda)$, or $\text{IsRel}(\lambda')$. The relaxed sequential composition $(P_1, <_1, \Phi_1); (P_2, <_2, \Phi_2)$ of pomsets is $(P_1 \oplus P_2, <^+, \Phi_1 \uplus \Phi_2)$ when $P_1$ is finite, where $(i, p) < (j, q)$ if and only if $i = j$ and $p < q$, or $i = 1, j = 2$, and $\text{Ord}(\Phi_1(p), \Phi_2(q))$, and $<_+$ is the transitive closure of $<$. When $P_1$ is infinite, $P_1 : P_2 = P_1$. Relaxed sequential composition is also associative with $0$ as its unit.

The sequencing, looping, and conditional clauses are given by:

$$
\mathcal{P}(c_1 ; c_2) = \mathcal{P}(c_1) ; \mathcal{P}(c_2) \\
\mathcal{P}(\text{if } b \text{ then } c_1 \text{ else } c_2) = (\mathcal{P}(b)_{\text{true}} ; \mathcal{P}(c_1)) \cup (\mathcal{P}(b)_{\text{false}} ; \mathcal{P}(c_2)) \\
\mathcal{P}(\text{while } b \text{ do } c) = \left( \bigcup_{n=0}^{\infty} I^n(b, c) \right) \cup I^\omega(b, c) \\
I^0(b, c) = \mathcal{P}(b)_{\text{false}} \\
I^{n+1}(b, c) = \mathcal{P}(b)_{\text{true}} ; \left( \mathcal{P}(c) ; I^n(b, c) \right)
$$

where $I^\omega(b, c)$ is the taken to be the evident infinite unfolding. There are a few subtleties in these clauses. In the clause for $\text{if } b \text{ then } c_1 \text{ else } c_2$, we use sequential compositions because there is a control-flow dependency between the memory actions for $b$ and those for the $c_i$. Respecting this dependency is important to eliminating “thin-air” behaviours. Indeed, suppose we had used the relaxed composition instead, and consider the program $\text{if } y_{rlx} = 1 \text{ then } x :=_{rlx} 1 \parallel \text{ if } x_{rlx} = 1 \text{ then } y :=_{rlx} 1$. Then it would have a pomset of the form $\{ y =_{rlx} 1 \ x :=_{rlx} 1 \ x =_{rlx} 1 \ y :=_{rlx} 1 \}$ in its denotation, and none of the memory actions would be ordered because the
locations in the boolean expressions and the commands in the conditional branches involve different locations. One could then perform the write actions before the read actions and execute the whole program, even from a state where $y$ and $x$ are initialized to 0. By instead using sequential composition, the reads are sequenced before the branch’s writes, and the program is not executable from this state. In contrast, in the clause for $c_1; c_2$, we should be permitted to reorder memory accesses if the memory model allows it, and so we use the relaxed sequential composition.

The last clause is for local assignables, which can be thought of as registers. Given a command $\text{local } n_{na} = v \text{ in } c$, the intention is that the assignable $n$ should be initialized to $v$ and be visible only to $c$. Consequently, any other commands $c'$ should not be able to observe $c$’s effects on $n$, even if $n$ appears free in $c'$. We must, however, be able to observe that $c$ did an action whenever it does an $n$-action: the program $\text{local } n_{na} = 0 \text{ in } (\text{while } n_{na} = 0 \text{ do } n :=_{na} 0)$ should be non-terminating. To satisfy these desiderata we take all of the pomsets of $c$ whose uses of the location $n$ are internally consistent and then replace all $n$-actions with no-op $\delta$ actions. We formally accomplish this by introducing additional operations on pomsets. To ensure internal consistency on $n$, we need to restrict our attention to $n$-actions. The restriction of a pomset $(P, <, \Phi)$ to a subset $L' \subseteq L$ is the pomset $P | L' = (\Phi^{-1}(L'), < \cap L' \times L', \Phi | \Phi^{-1}(L'))$ obtained by discarding all elements whose label is not in $L'$. To make sure they are internally consistent, we check that they are sequentially executable. This is accomplished with a predicate $\text{SeqExec}_n(P)$ that holds if and only if $P$ is $n :=_{na} v$ followed by zero or more occurrences of $n =_{na} v$, or if $P = P_1 ; P_2$ with $\text{SeqExec}_n(P_1)$ and $\text{SeqExec}_n(P_2)$. This syntactic check is equivalent to the sequential executions of Section 4. Finally, to replace all $n$-actions by $\delta$ actions, we need a substitution operation. The substitution of $l$ for $L' \subseteq L$ in $P$, $[l/L']P$, is given by $(P, <, \Phi)$ where $\Phi(p) = l$ if $\Phi(p) \in L'$, and $\Phi(p) = \Phi(p)$ otherwise. Combining these ingredients, we get the clause

$$\mathcal{P}(\text{local } n_{na} = v \text{ in } c) = \{[\delta/A_n]P | P \in \mathcal{P}(c), \text{SeqExec}_n(\{i :=_{na} v\} ; P | A_n)\}.$$  

This definition satisfies various desirable equivalences, such as

$$\text{local } n_{na} = 0 \text{ in } n :=_{na} 42 \equiv_p \text{skip}$$

$$\text{local } n_{na} = 0 \text{ in } (\text{while } n_{na} = 0 \text{ do } n :=_{na} 0) \equiv_p \text{while true do skip},$$

where $p \equiv_p p'$ is program equivalence, defined to hold if and only if $\mathcal{P}(p) = \mathcal{P}(p')$.

To illustrate our semantic clauses, we observe that the command

$$\text{while } i < 2 \text{ do } (x :=_{na} x_{na} + 1 ; i :=_{na} i_{na} + 1)$$

includes pomsets of the following form, for each $v \in V$, in its denotation:

$$\begin{align*}
&i =_{na} 0 \rightarrow i =_{na} 1 \rightarrow i =_{na} 1 \rightarrow i =_{na} 2 \\
&i =_{na} 0 \rightarrow x =_{na} v \rightarrow x =_{na} v + 1 \rightarrow x =_{na} v + 1 \rightarrow x =_{na} v + 2.
\end{align*}$$
In contrast, the command

\[
\text{local } i_{\text{na}} = 0 \text{ in while } i < 2 \text{ do } (x := _{\text{na}} x_{\text{na}} + 1; i := _{\text{na}} i_{\text{na}} + 1)
\]

has executable pomsets of the form

\[
x = _{\text{na}} v \rightarrow x := _{\text{na}} v + 1 \rightarrow x = _{\text{na}} v + 1 \rightarrow x := _{\text{na}} v + 2.
\]

4 Executional Interpretation

We give a race-detecting input-output interpretation to the abstract denotations of Section 3. This interpretation serves three main purposes. First, it gives us a notion of “running” the executions a pomset describes, and it tells us the initial states from which we can do so, along with the corresponding effects on state. Second, it gives us a means of detecting which syntactic races are meaningful, and which can not occur. For example, the program (1) (page 3) has a syntactic race on the non-atomic location \(x\), but this race can never occur during an execution starting from a zero-initialized state because of the synchronization via the atomic location \(y\). Finally, it allows us to rule out various pomsets assigned to commands that are not executable alone, but that are included for the sake of compositionality and that are executable in a larger environment. Consider, for example, the pomset \(x := _{\text{sc}} 2 \rightarrow x := _{\text{sc}} 1 \rightarrow y := _{\text{sc}} 1\) belonging to the program \(x := _{\text{sc}} 2; \text{if } x_{\text{sc}} = 1 \text{ then } y := _{\text{sc}} 1\). It is not executable, but it would be if we were to compose it with \(x := _{\text{sc}} 1\).

We use two kinds of state: proper and overdefined. **Proper states** are finite partial function from identifiers to values, in particular, elements of \(\text{Ide} \rightarrow ^{\text{fin}} V_{\bot}\). We include a least element \(\bot\) in the codomain to denote an unconstrained value. Its purpose will be made clear when we define footprints of actions below. We use the notation \([x_1 : u_1, \ldots, x_n : u_n]\) to mean the proper state whose graph is \(\{(x_1, u_1), \ldots, (x_n, u_n)\}\). Given proper states \(\sigma\) and \(\sigma'\), let \(\sigma \sqsubseteq \sigma'\) if and only if for all \(x \in \text{dom}(\sigma)\), \(\sigma(x) \sqsubseteq \sigma'(x)\). The symbol \(\top\) is the **overdefined state**, which is the result of a race. Let \(\Sigma\) be the set of all states, ranged over by \(\sigma\).

We proceed in two stages. We first assign an executional meaning to individual memory actions. Then, we assign an executional meaning to action pomsets. Because we are in a weak memory setting in which a single location can be acted on concurrently, the concept of a “global state” is not well-defined. Indeed, hardware features such as write buffers could cause different threads to read different values from the same location at the same time. Instead, we use a local notion of state called a footstep. A **footstep** of an action \(\lambda\) is a pair \((\sigma, \tau)\) of states, where \(\sigma\) is a minimal piece of state enabling \(\lambda\) to be performed, and \(\tau\) describes the effect of performing \(\lambda\) from \(\sigma\). The **footprint** \([\lambda]\) of \(\lambda\) is the set of all of its footprints. We define the footprints of memory actions as follows:

\[
[x := \mu v] = \{(x : v), []\}, \quad [\delta] = \{([], [])\}
\]

\[
[x := \mu v] = \{(x : \bot), [x : v]\}, \quad \text{fence}_\alpha = \{([], [])\}
\]

\[
[\text{rmw}_\alpha(a; v; v')] = \{([a : v], [a : v'])\}
\]

Informally, it should be clear that none of the above actions cause any allocation.
whenever \((\sigma, \tau) \in \llbracket \lambda \rrbracket\) for some action \(\lambda\), \(\text{dom}(\tau) \subseteq \text{dom}(\sigma)\). We use the \(\perp\) value in the codomain of proper states to indicate that, though a write action \(x :=_w v\) requires that the location \(x\) appear in the initial state, it is ambivalent to its value. The footprint of an action is also agnostic of the action’s memory ordering tag.

We can give pomsets an analogous notion of footprint. We will do so by recursing on the structure of the pomset, considering three principle cases: when the pomset is a single action, when the pomset can be decomposed into a pair of parallel pomsets, and when the pomset has an executable prefix.

We first specify structural conditions for when two pomsets can be run concurrently and whether doing so constitutes a race. Because we want a total order on all \(sc\) actions, we cannot run two pomsets containing \(sc\) actions concurrently. So we say concurrently executing \(P_1\) and \(P_2\) respect \(sc\) actions, \(P_1 \text{ rsc } P_2\), if and only if only one of them performs \(sc\) actions, i.e., if and only if \(P_1 \upharpoonright A_{sc} = \emptyset\) or \(P_2 \upharpoonright A_{sc} = \emptyset\). We say that pomsets \(P_1\) and \(P_2\) have a data race\(^4\) on \(n\) if \(n \in \text{RaceLocs}(P_1, P_2) = \bigcup_{1 \leq i, j \leq 2} \text{Ide}(P_1 \upharpoonright (A_{sc} \cap A_{w})) \cap \text{Ide}(P_j \upharpoonright (A_{na}))\) and that they have a data race, \(P_1 \text{ dr } P_2\), if they have one on some \(n\). Intuitively, \(n \in \text{RaceLocs}(P_1, P_2)\) means that \(P_1\) and \(P_2\) both act on \(n\) with at least one of them writing to \(n\).

Pomsets \(P_1\) and \(P_2\) are consistent, \(P_1 \text{ co } P_2\), if (i) \((- (P_1 \text{ dr } P_2))\), (ii) \(P_1 \text{ rsc } P_2\), and (iii) \(\text{Ide}(P_1 \upharpoonright A_w) \cap \text{Ide}(P_2 \upharpoonright A_w) = \emptyset\). Consistency means that there is no syntactic constraint preventing us from considering concurrent execution of \(P_1\) and \(P_2\). The third condition means we do not have any write-write races between \(P_1\) and \(P_2\), and is required to totally order writes on a per-location basis. In contrast, pomsets \(P_1\) and \(P_2\) could race, \(P_1 \text{ rc } P_2\), if (i) \(P_1 \text{ dr } P_2\), (ii) \(P_1 \text{ rsc } P_2\), and (iii) \(\text{Ide}(P_1 \upharpoonright (A_w \setminus A_{na})) \cap \text{Ide}(P_2 \upharpoonright (A_w \setminus A_{na})) = \emptyset\). The third condition means that we do not have any atomic write-write races. The intention is whenever \(P_1 \text{ rc } P_2\), we should be able to regain consistency by deleting all of the data races.

Next, we need a notion of splitting a pomset into a prefix and a suffix that can sequentially be executed. We say that a subset \(Q\) of a pomset \(P\) is downward-closed if whenever \(p <_P q\) and \(q \in Q\), then \(p \in Q\). We write \(P_1 \prec_P P_2\) to mean that \(P_1\) is a finite downward-closed subset of \(P\) and that \(P_2\) is the remainder of \(P\). In this case, we call \(P_1\) a prefix of \(P\) and \(P_2\) a suffix of \(P\). Observe that if \(P = P_1 \upharpoonright P_2\) and \(P_1\) is finite, then \(P_1 \prec_P P_2\); finiteness is needed to guarantee fairness.

When executing two threads in parallel, we need only consider footsteps starting from consistent states. We say two proper states \(\sigma, \sigma' \in \Sigma\) are consistent, \(\sigma \upharpoonright \sigma'\), if \(\sigma \sqcup \sigma'\) exists. This means that for all \(x \in \text{dom}(\sigma) \cap \text{dom}(\sigma')\), if \(\sigma(x) \neq \perp\) and \(\sigma'(x) \neq \perp\), then \(\sigma(x) = \sigma'(x)\). The overdefined state \(\top\) is consistent with no state. Given a set \(S\) and a state \(\sigma\), we let \(\sigma \setminus S\) be \(\top\) when \(\sigma = \top\), and \(\{(x, v) \in \sigma \mid x \notin S\}\) otherwise. Given proper states \(\sigma\) and \(\sigma'\), updating \(\sigma\) by \(\sigma'\) gives us a new state \([\sigma \mid \sigma']\) = \(\sigma' \sqcup (\sigma \setminus \text{dom}(\sigma'))\). Explicitly, \([\sigma \mid \sigma'](x)\) is \(\sigma'(x)\) whenever \(x \in \text{dom}(\sigma')\), and \(\sigma(x)\) whenever \(x \notin \text{dom}(\sigma')\). If \(\sigma\) or \(\sigma'\) is \(\top\), then \([\sigma \mid \sigma']\) is defined to be \(\top\).

To combine the initial states of two pomsets data racing on \(R \subseteq \text{Ide}_{na}\), we define the racy product \(\sigma_1 \otimes_R \sigma_2 = [\sigma_1 \sqcup \sigma_2 \mid (\sigma_1 \cap \sigma_2) \upharpoonright R]\), explained below.

We let the footprint \(\llbracket P \rrbracket\) of a pomset \(P\) be inductively defined as the least set given by the following rules, which are explained below:

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4 One could replace \(A_{na}\) with \(A_{\pi}\) throughout to instead consider races between actions satisfying \(\pi\).
The set of executions of a pomset \( P \) is \( \mathcal{E}(P) = \{ (\sigma, [\sigma | \tau]) \mid \sigma \in \Sigma, (\sigma', \tau) \in [P], \sigma' \subseteq \sigma, \text{Im}(\sigma) \subseteq V \} \), and the set of executions of a program \( p \) is \( \mathcal{E}(p) = \bigcup_{P \in \Gamma(p)} \mathcal{E}(P) \). Executions capture running programs on “real” states, so we require initial states to have a specific value for each location. We say \( P \) is executable from \( \sigma \) if \((\sigma, \tau) \in \mathcal{E}(P) \) for some \( \tau \), and \( P \) is racy if \((\sigma, \top) \in [P] \) for some \( \sigma \).

We explain each of the rules in turn. The (SEQ) rule captures sequential execution of a prefix \( P_1 \) before a suffix \( P_2 \). The consistency condition \([\sigma_1 | \tau_1] \uparrow \sigma_2 \) tells us that, if we start from a state satisfying \( \sigma_1 \) and update it with the effects \( \tau_1 \) of performing \( P_1 \), the resulting state doesn’t disable the execution of \( P_2 \). The state \( \sigma_2 \setminus \text{dom} \tau_1 \) contributes the initial state required by \( P_2 \) that isn’t provided by \( P_1 \).

The (PAR) rule tells us that whenever \( P_1 \) and \( P_2 \) cannot race and agree on their initial states, then we can run them in parallel with resulting effect \( \tau_1 \sqcup \tau_2 \). The effect \( \tau_1 \sqcup \tau_2 \) is a well-defined proper state because the assumption \( P_1 \sqcup P_2 \) guarantees that \( P_1 \) and \( P_2 \) do not write to the same location, i.e., that \( \text{dom}(\tau_1) \cap \text{dom}(\tau_2) = \emptyset \).

The (RACEP) rule handles races a in pomset’s prefix. The rule tells us that if \( \sigma_1 \) is sufficient to reach a race in \( P_1 \) and \( P_1 \) is a prefix of \( P \), then \( \sigma_1 \) is sufficient to reach a race in \( P \). This captures the viewpoint that if we ever encounter a race, we do not need to execute the rest of the program. The (RACES) rule deals with a race in a suffix of a pomset, and is analogous to the (SEQ) rule.

The (RACE) rule resembles the (PAR) rule. The key difference is how we form the initial state. Before considering motivating examples, we first unpack the definition of the racy product \( \sigma = \sigma_1 \otimes_{\text{RaceLocs}(P_1, P_2)} \sigma_2 \), assuming \( \sigma_1 \uparrow \sigma_2 \). If \( x \notin \text{dom}(\sigma_2) \), then \( \sigma(x) = \sigma_1(x) \), and vice-versa. Now consider \( x \in \text{dom}(\sigma_1) \cap \text{dom}(\sigma_2) \). If \( x \in \text{RaceLocs}(P_1, P_2) \), i.e., if \( P \) has a race on the non-atomic location \( x \), then \( \sigma(x) = \sigma_1(x) \sqcup \sigma_2(x) \), i.e., \( \sigma(x) = \perp \) if any of the \( \sigma_i(x) \) is \( \perp \). As we will see in the example \( Q_\mu \) below, this captures a race where the action writing to \( x \) does not depend on a prior read from \( x \) in order to be executable. If \( x \notin \text{RaceLocs}(P_1, P_2) \), then \( \sigma(x) = \sigma_1(x) \sqcup \sigma_2(x) \). For example, \( [x:0, a:1, n:2, n':3, n'':4] \otimes_{\{a, n, n'\}} [a:1, n:2, n':3, n'':4] \) is \( [x:0, a:1, n:2, n':3, n'':4] \).
state caused by the writing of \( x \). Our semantics validates this desideratum: we can apply (RACE) to the unsequenced actions to get the footstep \( ([x : \bot], \top) \), and then using (RACES) we get that \( ([x : \bot], \top) \in \llbracket Q_{\mu} \rrbracket \). Now assume that \( \mu \neq na \), then \( Q_{\mu} \) is not \( na \)-racy: it has no \( na \) actions on which it can race. Moreover, \( Q_{\mu} \) has a non-empty footprint only if \( u \in \{0, v\} \), and \( \llbracket Q_{\mu} \rrbracket = \{ ([x : \bot], [x : v]) \} \).

Next consider the pomset \( R_{\mu} = \{ x := \mu \ (w \leftarrow x = \mu \ w \leftarrow x := \mu \ 0 \rightarrow x = \mu \ u \} \), and assume first that \( \mu = na \). We argue that this pomset should be executable only when \( w = 0 \); when \( w \neq 0 \), there is no write supplying the value \( w \) required by the read, and so the data-race on \( x \) should not be able to manifest itself. However, when \( w = 0 \), this pomset should be racy, because we have an unsequenced non-atomic write and read from \( x \). Our semantics captures these behaviours. For example, \( \llbracket x := \mu \ w \leftarrow x = \mu \ w \leftarrow x := \mu \ 0 \rightarrow x = \mu \ u \rrbracket = \{ ([x : w], [x : v]) \} \) and \( \llbracket x := \mu \ u \rrbracket = \{ ([x : u], [\bot]) \} \), and the states \( [x : w] \) and \( [x : u] \) are consistent only if \( w = u \). When this is the case, we get \( ([x : w], \top) \) as the sole footprint for the parallel composition. But we can apply the (RACES) rule only when \( [x : \bot | x : 0] \uparrow [x : w] \), which holds only when \( w = 0 \). Decomposing the pomset differently provides the same constraint. In contrast, when \( \mu \neq na \), \( R_{\mu} \) is not racy and it is executable only when \( w = 0 \) and \( u \in \{0, v\} \).

Finally, consider the pomset \( S = \{ x := na \ y := rel 1 \ = acq 1 \rightarrow x = na \ u \} \). We get the footsteps \( ([x : u, y : 1], [x : v, y : 1]) \) and \( ([x : \bot, y : 1], \top) \) for all \( u \) and \( v \). The first footprint corresponds to a sequential execution with all the reads before the writes. The second footprint corresponds to \( y \) reading 1 from the initial state, and then the program racing on \( x \). When \( u = v \), we also get the footprint \( ([x : \bot, y : 1], [x : v, y : 1]) \), which describes an execution where all reads are performed after all writes.

We show that our definition of execution validates various other litmus tests in the way we expect. The SB (store buffering) test is the simplest example of behaviour that is not sequentially consistent. When \( \alpha \neq sc \), we can execute the pomset \( \{ x := \alpha \ 1 \rightarrow y = \alpha \ 0 \quad y := \alpha \ 1 \rightarrow x = \alpha \ 0 \} \) starting from the state \( [x : 0, y : 0] \) by using the (PAR) rule.

We can also validate the IRIW (independent reads of independent writes) test. Indeed, we can execute the pomset
\[
x := rel 1 \quad y := acq 1 \rightarrow x := acq 0 \quad y := rel 1 \quad x := acq 1 \rightarrow y := acq 0
\]
starting from the initial state \( [x : 0, y : 0] \) by splitting the pomset down the middle and applying the (PAR) rule. This shows that we are weaker than the TSO memory model, because we do not impose a total order on all writes. Though we can read writes to different locations in different orders, the \textbf{co} restriction on the (PAR) rule ensures that we have a per-location total order on writes. Then all threads see the writes to the same location in the same order, i.e., we guarantee coherence.

5 Related Work

Most work on formalizing weak memory models so far uses “execution graphs” or “candidate executions”, in which nodes are labeled with actions and there are multiple kinds of edge, usually characterized as \textbf{po} (program order), \textbf{rf} (reads-from), \textbf{sc} (store  order), \textbf{acq} (acquire), and \textbf{rel} (release). However, these formalisms do not include a total order on all writes. The work of Edelkamp et al. [3••, 5••, 7••] and Kavanagh and Brookes [8••] provide semantics that include an order on all writes, and this enables a stronger notion of execution graph. We consider that our semantics is closer to the notion of execution graph in that it includes a total order on all writes, which is essential for validating the sequential consistency of weak memory models.
mo (modification order), and so on. There is a substantial body of well-established research in this vein, including [1,3,5,11,12]. In work aiming to formalize C/C++11 such as [4], axioms are imposed to rule out candidate executions involving undesirable cycles of composite edges, primarily to avoid issues with so-called thin-air reads, and to ensure that each read action is justified by a suitable write. It has proven to be difficult to strike the right balance between ruling out bad cases while still allowing intended behaviours.

Our memory model is heavily based on the RC11 (“Repaired C11”) model presented by Lahav et al. [10]. The RC11 model repairs compilation to Power by providing a better semantics for SC accesses. Like RC11, our model differs from C11 by not treating races between atomic accesses as undefined behaviour. Our approach to eliminating “thin-air” behaviour is similar to theirs: we prohibit violations of data and control-flow dependency, which amounts to prohibiting cycles in the execution (“hb”) order between reads and their corresponding writes.

In prior work [9], we give a semantics to the SPARC TSO weak memory model using pomset denotations and executions, and buffered state. The semantics developed in this paper is a significant step forward toward greater generality and wider applicability. Rather than attempt to model out-of-order execution by explicitly modelling buffers, both in pomset generation and in execution, we use the relaxed composition operator and leverage pomset structure. To enforce a total order on writes during execution, TSO executions were parametrized with linearizations of writes. In contrast, C11 executions totally order sc actions via the co relation, thereby reducing technical overhead.

Jeffrey and Riely [8] and Castellan [7] give a denotational semantics using event structures and exploit game-theoretic ideas in formulating a notion of execution. We prefer to work with a set of pomsets, obtained by taking account of possible relaxations and executions, rather than using a single structure combining these possibilities into one object; it seems less cumbersome to work with sets-of-pomsets.

6 Conclusion

Our extension to incorporate the wider range of C11-style memory orderings required significant technical development in order to produce a denotational account that is faithful to operational intuitions, and improves on the foundations laid by our prior denotational account of TSO. A key new idea presented here is the relaxed sequential composition for pomsets, a form of sequential composition that takes account of the memory model’s support for reordering of memory actions. We are careful to avoid reordering of actions for which there is a control-flow dependency, arguing that this eliminates a major class of thin-air behaviours. We discussed a selection of “litmus test” examples to show that our semantics and our notion of pomset execution yield results consistent with the literature. We plan a more comprehensive cataloguing of litmus tests to solidify this claim. Indeed, we expect to prove a pomset analogue of the DRF-SC property, which provides programmers a sufficient condition for ensuring their programs are not executionally racy.
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