Design of 2.4Ghz CMOS Floating Active Inductor LNA using 130nm Technology

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Abstract. This paper presents about design and optimization of CMOS active inductor integrated circuit. This active inductor implements using Silterra 0.13μm technology and simulated using Cadence Virtuoso and Spectre RF. The center frequency for this active inductor is at 2.4 GHz which follow IEEE 802.11 b/g/n standard. To reduce the chip size of silicon, active inductor is used instead of passive inductor at low noise amplifier LNA circuit. This inductor test and analyse by low noise amplifier circuit. Comparison between active with passive inductor based on LNA circuit has been performed. Result shown that the active inductor has significantly reduce the chip size with 73 % area without sacrificing the noise figure and gain of LNA which is the most important criteria in LNA. The best low noise amplifier provides a power gain (S21) of 20.7 dB with noise figure (NF) of 2.1dB.

1. Introduction
The LNA is widely used in wireless application such as phone. It is required LNA to operate in low voltage without compromising other factor such as high gain, low noise and linearity requirements at the operating frequency. In term of sizing of chip, it must design small as possible due to cost. The design of the LNA imposes a challenge in terms of meeting total functions. In order to reduce chip area or smaller size it is further challenging. The technology now days are racing towards nano-meter range. The conventional LNA is using passive inductor which are consume lot of area in chip [1,2]. For the reasons maintaining cost to market ratio is a bigger challenge. As the value of inductance climb it required lot space on a chip [3,4]. The consequences are that active inductor using CMOS is used. Several circuit topologies had been proposed in the past to implement active inductor based on gyrators design. Active inductor manages to constantly tune to protect temperature or process variation. The proses variation usually occur at fabrication foundry where naturally occurring variation in the attributes of transistors (length, widths, oxide thickness) when integrated circuits are fabricated. By implement the active inductor on LNA circuit it takes about 1% until 10% of passive active inductor which can reduce cost [5]. Other than that, active inductor has higher inductance value, wide frequency tuning range and higher quality factor which is important for circuit design. Indeed, active inductor may reduce the chip area, but it leads to high power dissipation [6,7].
Table 1 shows the design specification set for LNA following 802.11b/g/n IEEE Wireless Local Area
Network standard. The LNA should be designed to run with the center frequency at 2.4 GHz.

| Parameter                  | Specification |
|----------------------------|---------------|
| Process technology         | RFCMOS 130nm  |
| Center frequency (GHz)     | 2.4           |
| Power supply (V)           | ≤ 1.2         |
| $S_{21}$ (dB)              | > 15          |
| $S_{11}$ (dB)              | < -12         |
| $S_{22}$ (dB)              | < -12         |
| $S_{12}$ (dB)              | < -20         |
| Noise factor (dB)          | < 4           |
| Power dissipation (mW)     | < 8           |

2. Active Inductor

Many applications required the inductance of active inductor can be tuneable from a small range up
to larger range of inductance. The applications may include phase-locked loops, filters, voltage or
current controlled oscillators and others. Thus, there are verity of active inductor design or technique
to get the exact inductance value. A floating active inductor using resistive feedback and single ended
active inductor has been chosen.

2.1. Floating Active Inductor using Resistive Feedback

Figure 1 shown gyrator-C floating inductor differentially configured. Most of the transistor are in
biased in the saturation region except transistor at M5 and M6. Both transistors were biased in triode
region and behave as voltage-controlled resistors whose value are controlled by the gate voltage $V_g$.
[8]. M1, M2, M5, M6 are NMOS transistors and M3,M4 are PMOS transistors. Feedback resistor are
added between M1 and M2.

![Proposed schematic floating active inductor using resistive feedback](image_url)
In Figure 2, \( g_f \) is the conductance of feedback resistor \( R \). \( C_L \), \( g_C \), \( g_2 \) are the effective parasitic capacitance and conductance at node \( V_1 \) and \( V_2 \).

**Figure 2.** Small signal model for floating active inductor

Input impedance equation:

\[
Y_{\text{in}} = g_{m1} + \frac{g_{m2}^2 (g_{m2} - g_f)}{(g_{f} + g_{C2}) + (g_{f} + g_{C1}) + (g_{m1} - g_f)(g_f - g_{m2})} \tag{1}
\]

Quality Factor equation:

\[
Q = \frac{\text{Im}[Z]}{\text{Re}[Z]} \tag{2}
\]

Inductor equation:

\[
L = \frac{\text{Im}(Z_{\text{in}})}{\omega} \tag{3}
\]

Equation 1, 2, 3 indicate input impedance, quality factor and tuning inductor value respectively. These equations are required for tuning the value of inductor for floating active inductor using resistive feedback circuit.

### 2.2. Single Ended Active Inductor

Figure 3 indicate design of single ended active inductor. Transistor \( M_1 \) and \( M_2 \) represents positive transconductance \( g_{m1} \) between input and output. For transistor \( M_3 \) and \( M_4 \) it represents negative transconductance \( g_{m1} \). These two transconductance will form gyrator \(-C\) which transform intrinsic capacitance into inductive behaviour.
Figure 3. Schematic circuit of single ended active inductor

Input impedance equation:

\[ Y_{in} = g_1 + sC_1 + \frac{\beta m_4 + \beta m_3 + \beta m_2 + \beta m_1}{(G + sC2)(G + sC3)(G + sC4 + \beta s)} \]  \hspace{1cm} (4)

Quality Factor equation:

\[ Q = \frac{\text{Im}[Z]}{\text{Re}[Z]} \]  \hspace{1cm} (5)

Inductor equation:

\[ L = \frac{z_{in}}{j\omega} \]  \hspace{1cm} (6)

Equation 4, 5, 6 indicate input impedance, quality factor and tuning inductor value respectively. These equations are required for tuning the value of inductor for single ended circuit. These works basically take the LNA inductively degenerated design technique and by using the same design active inductor is replaced with passive inductor.

The schematic as shown in Figure 4 is the combination technique between floating active inductor using resistive feedback and single ended active inductor. Both techniques are used in one circuit to optimize the result of the gain bandwidth and noise figure. This circuit basically is an inductive degenerated design and spiral inductor has been replacing with active inductor where it can give exact function as spiral inductor.
3. Results and Discussion
S-parameter measurements stated which is the characteristic impedance or system impedance. Figure 5 below indicate the s-parameters for LNA active inductor and passive inductor respectively. It includes all four s-parameters which are $S_{11}$, $S_{12}$, $S_{21}$ and $S_{22}$. $S_{21}$ is a power gain. Power gain should be higher than 15 dB to compensate for noise contribution of the next stage of the circuit. So with these LNA active inductor it can get value of 20.7dB and for the LNA passive inductor the value is 17.9dB. This value should have very small value in order to get high reverse isolation and it can give better stability to the LNA. By using LNA active inductor circuit the value at -42.39dB while passive inductor is -38.3dB. $S_{22}$ representing output matching. The LNA will produce the low output impedance. With this design it can give output matching of -19.8dB and -19.9dB for LNA passive inductor. The last s-parameters are $S_{11}$ which is input matching. With the LNA active inductor it archives value of -1dB and for LNA passive inductor the value is -19.3dB.

![Figure 4. Inductively degenerated LNA circuit using active inductor](image)

![Figure 5. Comparison of S-Parameter LNA Performance using active and passive inductor](image)
The value NF for active inductor are 2.1dB while the passive 1.66dB. There are 0.44dB increasing noise figure at active inductor as shown in Figure 6.

![noise figure LNA passive and active inductor](image)

**Figure 6.** Noise Figure comparison between LNA active and passive inductor

The layout comparison between LNA active inductor and passive inductor respectively was shown in Figure 7. The sizing of layout can be reduced up to 73% when use active inductor to replace passive inductor. LNA active inductor also can reduce the cost of making chip since it consumed less area compare to LNA passive inductor.

![LNA layout](image)

**Figure 7.** LNA layout (a) using active inductor, (b) using passive inductor

| Parameter | Active Inductor [This work] | Passive Inductor | Other work [9] | Other work [10] | Other work [11] | Other work [12] |
|-----------|-----------------------------|------------------|----------------|----------------|----------------|----------------|
| \( s_{11} \) (dB) | -1 | -19.3 | 12.6 | -10 | -9 | -10 |
| \( s_{12} \) (dB) | -42.3 | -38.3 | - | - | - | - |
| \( s_{21} \) (dB) | 20.7 | 17.9 | 14.6 | 13 | 16.4 | 14.18 |
| \( s_{22} \) (dB) | -19.8 | -19.9 | -19.6 | -10 | -8 | -16.21 |
| NF (dB) | 2.1 | 1.66 | 2.5 | 3 | 4 | 2.78 |
| Power dissipation (mW) | 24.9 | 4.19 | 8.14 | 62.5 | 14.5 | 10.36 |
4. Conclusion
A floating active inductor and single ended active inductor has been used in this project to replace the passive inductor at LNA circuit. LNA active inductor was design and tuning using Siltechra 0.13μm CMOS technology. By designing active inductor, it can reduce the area of chip without compromising the two most important factors in LNA circuit which is noise figure, NF and power gain, $S_{21}$, which is 2.1 dB and 20.7 dB respectively. The consequences of reduction area lead to reduction of cost in a chip making. The total power consumption for LNA active inductor is 24.9 mW. The future recommendation is to be able to replace all the active inductor since this work able to replace two of out three inductors without compromising the power gain and noise figure.

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