Near-thermal limit gating in heavily-doped III-V semiconductor nanowires using polymer electrolytes

A.R. Ullah,1 D.J. Carrad,1,2 P. Krogstrup,2 J. Nygård,2 and A.P. Micolich1

1School of Physics, University of New South Wales, Sydney NSW 2052, Australia
2Center for Quantum Devices and Station Q Copenhagen, Niels Bohr Institute, University of Copenhagen, Universitetsparken 5, DK-2100 Copenhagen, Denmark

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Doping is a common route to reducing nanowire transistor on-resistance but has limits. High doping level gives significant loss in gate performance and ultimately complete gate failure. We show that electrolyte gating remains effective even when the Be doping in our GaAs nanowires is so high that traditional metal-oxide gates fail. In this regime we obtain a combination of sub-threshold swing and contact resistance that surpasses the best existing p-type nanowire MOSFETs. Our sub-threshold swing of 75 mV/dec is within 25% of the room-temperature thermal limit and comparable with n-InP and n-GaAs nanowire MOSFETs. Our results open a new path to extending the performance and application of nanowire transistors, and motivate further work on improved solid electrolytes for nanoscale device applications.

I. INTRODUCTION

Complementary metal-oxide-semiconductor (CMOS) technology is central to modern integrated circuits. The technology combines p-type and n-type Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), exploiting the opposing charge carrier polarity and channel current versus gate voltage characteristics to achieve low power logic. Miniaturisation drove development of nanowire CMOS featuring III-V nanowires integrated on Si towards high performance at low cost [1–3]. This is underpinned by broader research aimed at improved gating in III-V Nanowire Field-Effect Transistors (NWFETs) seeking steeper sub-threshold slope and lower parasitic resistance for reduced operating voltage and enhanced energy efficiency [2]. Progress has been strong for n-type III-V NWFETs with near-thermal limit sub-threshold slope obtained for InP [5], InGaAs [6] and AlGaAs/GaAs [7]. Integration of n-type III-V NWFETs on Si is well established [8] with GHz operation demonstrated [9]. Most of these devices achieve their excellent gate channel coupling by employing high-κ dielectrics such as HfO2.

The development of p-type III-V NWFETs has lagged behind [1]. This is caused by several key challenges for p-type devices including lower intrinsic carrier mobility and difficulties in growth, doping and fabrication of high quality ohmic contacts and gates. Hence III-V nanowire CMOS typically features p-type transistors far less ideal than their n-type counterparts [3, 10, 11]. Here we present polymer electrolyte gated Be-doped p+-GaAs NWFETs with near-thermal limit gating that point out a path to filling this significant performance gap. Our p+-doping ensures low contact resistance and high channel conductivity while the electrolyte gate provides sub-threshold slope ~ 75 mV/dec, on-off ratio of order 104 and low hysteresis. This is despite the doping level being so high that traditional metal-oxide gate structures fail completely, i.e., give no gate modulation or very poor on-off ratio (< 3) [12]. In particular, even top gates with HfO2 dielectric - similar to those that facilitate near thermal limit switching in, e.g., InP [5] - do not provide effective transistor action.

Our polymer electrolyte (PE) gate consists of an electron-beam patterned polymer gel, e.g., polyethylene oxide, spanning the gap between a metal electrode and the nanowire [13]. The gel absorbs water providing an environment for mobile ions, either H+/OH− from dissociated H2O, or added salt, e.g., LiClO4 [14]. Gating occurs by electric field driven ion migration with gate charge forming a concentric ion layer within ~ 1 nm of the nanowire surface [15]. The resulting strong gating has seen electrolyte gating become a well-known approach to improved performance in materials ranging from organic semiconductors to chalcogenides [16]. Electrolyte gating also provides a simpler route to achieving concentric gating action for nanowire devices [13, 17]. The key result of this work is a demonstration that electrolyte-gated nanowire transistors remain functional even in the limit where the doping density becomes sufficiently high that traditional gating approaches fail. This is useful because heavy doping provides a path to reduced contact and channel resistance. Additionally, PE gates are far simpler to produce than traditional metal-oxide wrap-gate structures [18] and utilise an intrinsically biocompatible material [22]. Nanopatterned PE gates have been used in applications from enacting external ionic doping of quantum devices [17] to ionic-to-electronic signal transduction [14]. Here we extend this to include improved p-type NWFETs for room temperature nanowire complementary circuits.
FIG. 1. Source-drain current $I_{sd}$ vs gate voltage $V_g$ for (a) metal-oxide top-gated and (b) PE-gated NW FETs. Both feature high Be acceptor concentration $N_A = 1.5 \times 10^{19} \text{cm}^{-3}$ p$^+$-GaAs. $V_{sd} = 100 \text{mV}$ for all traces with solid (dashed) lines showing sweeps towards more positive (negative) $V_g$. The blue and green traces in (a) are the metal top-gate and n$^+$-Si back-gates, respectively. The blue traces are offset downwards by 100 nA for clarity. The green and red traces in (b) are for the n$^+$-Si back-gate and PE-gate respectively. The dashed black line in (b) indicates the thermal limit sub-threshold swing 60 mV/dec. The inset to (a) shows the metal-oxide top-gated data from (a) on a linear scale to further demonstrate that weak gate modulation and no clear switching is observed. Corresponding device structures are inset to (a) and (b); S = source, D = drain, G = gate electrode, NW = nanowire, PEO = polyethylene oxide. The typical gate electrode G to nanowire gap is 2 $\mu$m for the device in (b). All data obtained at room temperature.

II. METHODS

Our self-catalysed GaAs nanowires were grown by molecular beam epitaxy on (111)Si. The undoped core was grown at 630°C using As$_4$ and a V/III flux ratio of 60 for 30–45 minutes. The Be-doped shell was grown at 465°C using As$_2$ and a V/III ratio of 150 for 30 minutes giving nanowires with typical diameter 150–200 nm and length 5–7 $\mu$m. The nanowires should be pure zincblende crystal phase throughout. There will possibly be some short wurtzite segments at the ends; these will be buried under the contacts. We focus here on nanowires with shell acceptor density $N_A = 1.5 \times 10^{19} \text{cm}^{-3}$; the highest doping density from our earlier work on all-inorganic p-GaAs NW FETs. Nanowires were transferred to a pre-patterned HfO$_2$/SiO$_2$-coated n$^+$-Si substrate for device fabrication with two architectures used: (a) a traditional metal-oxide $\Omega$-gate structure (Fig. 1(a) inset) and (b) a PE gate (Fig. 1(b) inset). Fabrication for both began with the contacts. These were defined by electron-beam lithography (EBL) and thermal evaporation of 200 nm of 1% Be in Au alloy (ACI Alloys). GaAs native oxide at the contact interfaces was removed by a 30 s etch in 10% HCl solution. The metal-oxide gate was produced in two steps. First a patterned 10 nm layer of the high-$\kappa$ insulator HfO$_2$ was defined by EBL and atomic layer deposition (ALD). An overlapping 20/180 nm Ti/Au gate electrode was then formed in a separate round of EBL and metal deposition.

For PE-gated devices, the Ti/Au gate electrode terminated 2 $\mu$m from the nanowire and was defined by EBL and thermal evaporation. Patterning of the PE was the final step. 200 mg polyethylene oxide (molecular weight 200k – Aldrich) was dissolved in 10 mL methanol by sonication for 30 min. Addition of LiClO$_4$ is optional and provides no significant performance enhancement in our NW FETs. For all of the PE gates used in this study, the polyethylene oxide is doped with LiClO$_4$ with a 1:10 LiClO$_4$:PEO ratio. The solution was left to stand overnight with the supernatant spin-coated onto the device at 3000 rpm for 60 s. The device was baked at 90°C for 30 mins to remove residual methanol. Polyethylene
oxide acts as a positive EBL resist[13] and was directly patterned by EBL with beam energy 7 keV and dose 300 µC/cm². Development in H$_2$O removed unexposed regions giving nanoscale PE strips between the gate electrode and nanowire[13]. Electrical measurements were performed at room temperature in ambient. Yokogawa GS200 voltage sources supplied the source-drain voltage $V_{sd}$ and gate voltage $V_g$ for both PE and metal-oxide gates. We measured the drain current $I_d$ using a Keithley 6517A electrometer.

### III. RESULTS

A key challenge for $p$-GaAs NWFTs is obtaining low contact resistance and strong gate performance simultaneously. Low resistance contacts to GaAs nanowires are difficult because surface-states pin the surface Fermi energy mid-gap, unlike for InAs, where the surface Fermi energy is pinned at the conduction band edge. This leads to a significant Schottky barrier for metal-GaAs interfaces. Ohmic contacts to GaAs typically use an annealed alloy of a noble metal and a diffusive dopant[27], e.g., AuGe for $n$-type[4] and AuBe for $p$-type[12]. The idea is that the diffusive dopant causes the semiconductor local to the metal contact to become very highly doped. This makes the Schottky barrier depletion region very narrow, raising the electron tunnelling probability and giving a linear $I$-$V$ characteristic for the contact. This can be assisted by doping the semiconductor local to the contact by other means, e.g., by ion-implantation[28], or during growth[23, 29].

Our GaAs nanowires are readily doped $p$-type with Be, which incorporates preferentially via the nanowire side facets enabling structures with an undoped core and Be-doped shell[25]. A Be-doped shell provides an ideal interface for AuBe contacts with narrow Schottky barrier and thereby $p$-type NWFTs with low resistance ohmic contacts. We recently showed that contact annealing is detrimental in this case likely because the Be diffusion rate within the nanowire exceeds the Be out-diffusion rate from the alloy, reducing the net doping level at the contact interface[12]. This provides a strong incentive to compensate by maximising shell doping density to ensure the Schottky barrier depletion width remains minimised. However, this approach brings a second problem: severe loss in gate performance. Figure 1(a) shows $I_{sd}$ versus $V_g$ for a $p$-GaAs nanowire MOSFET with high shell acceptor density $N_A = 1.5 \times 10^{19}$ cm$^{-3}$. The metal-oxide Ω-gate (blue trace) modulates the current by a factor of 2 at best despite the use of high-$κ$ dielectric. The data is presented on a focussed linear $I_{sd}$ scale in the inset to Fig. 1(a) to conclusively demonstrate this. To prove that this is not due to limited gate voltage range, we take a separate device to catastrophic gate dielectric breakdown without switching being observed. The data for this is shown in Supplementary Fig. 1. We obtain similar lack of gate efficacy from the $n^+$-Si back-gate (green
trace). Poor gating at the high free carrier density arising from degenerate doping is expected; it is exactly why FETs do not have metal channels. An obvious potential solution is to keep the shell doping density high near the contacts yet lower near the gate. Unfortunately, it is not clear how to achieve nanowire shell growth with controlled axial doping variation. Ion implantation is an alternative but one that causes significant damage to the nanowire [28]. Thus for our p-GaAs nanowire MOSFETs we are trapped in an unfortunate trade-off between contact resistance and gate performance governed by shell doping density. Our key finding in this paper is that electrolyte gating offers a path to obtaining low contact resistance and good gate performance simultaneously.

Figure 1(b) shows the performance of the PE gate (red trace) for a p-GaAs nanowire with \(N_A = 1.5 \times 10^{19} \text{cm}^{-3}\) from the same growth. The green trace shows the performance for the n"-Si back-gate to confirm that conventional gating still fails and there is no unanticipated difference between the nanowires in Figs. 1(a) and 1(b). The PE gate gives very strong gating with sub-threshold swing \(S = 75 \pm 15 \text{mV/dec}\) and on-off ratio near \(10^4\). The sub-threshold swing is comparable to the best obtained for n-InP (68 mV/dec) [5] and n-GaAs (70 mV/dec) [7] nanowire MOSFETs and within 25% of the room temperature thermal limit (60 mV/dec). We obtain on-current \(I_{on} \approx 0.25 \mu \text{A}\) at \(V_{sd} = 100 \text{mV}\) corresponding to 400 k\Omega channel resistance, with contact resistance \(R_{con} \approx 30 \text{k}\Omega\) previously measured for this doping level [12]. Similar performance is obtained from separate nominally identical devices as demonstrated by the data in Fig. 2. Figure 2(a) shows \(I_{sd}\) versus \(V_{sd}\) for a PE gated device at several \(V_g\) demonstrating good linear contact performance throughout the entire PE gate range. Saturating is not observed for \(V_{sd} < 2.5 \text{ V}\) in these high \(N_A\) nanowires, as expected given their high doping density. A significant aspect of Fig. 1(b) is the low hysteresis, particularly in the sub-threshold regime, which we attribute to three factors. First, growth on (111)Si gives (110) side-facets for which surface-states largely reside outside the band-gap [30]. Second, there is no added oxide beyond the thin GaAs native oxide that grows upon air exposure. Third, the high density of free carriers in the shell and mobile ions in the PE strongly screen the residual surface state/oxide trapping effects. As with the p-GaAs nanowire MOSFETs, the precise performance is tunable via \(N_A\), for example, at lower \(N_A = 1 \times 10^{18} \text{ cm}^{-3}\) we see slightly poorer sub-threshold swing (95 mV/dec) and higher \(R_{on} \approx 1.4 \text{ M}\Omega\) but improved on-off ratio \(\sim 10^4\), lower threshold voltage \(\sim +2\text{V}\) and no appreciable worsening in hysteresis. We also find that the threshold voltage is slightly influenced by \(V_{sd}\) as shown in Fig. 2(b). We do not expect significant short-channel effects in our devices, and accordingly, the threshold shift direction is opposite that expected for drain-induced barrier lowering (DIBL). The threshold shift direction is instead indicative of the increased \(I_{sd}\) that naturally follows increased \(V_{sd}\) at fixed \(V_g\), consistent with other nanowire transistors [5, 10]. Finally, we comment briefly on the field-effect mobility for our device. We can obtain the field-effect mobility \(\mu_{FE} = g_m L^2 / C V_{sd}\) with transconductance \(g_m = \partial I_{ds} / \partial V_g\) channel length \(L\) and gate capacitance \(C\). The latter is difficult to accurately estimate for an electrolyte gate and should be considered an order-of-magnitude estimate at best. Here we estimate the capacitance of the electrical double layer at the PE/NW interface using a concentric cylinder formula \(C = \frac{2 \pi \epsilon_0 \epsilon_r t}{\ln(1+r/r)}\) where \(\epsilon_0\) is the permittivity of free space, \(t\) is the electrical double layer thickness and \(r\) is the nanowire radius. We measured \(r = 72.5 \text{nm}\) by scanning electron microscopy, and \(L = 1.5 \mu\text{m}\), which is the length of nanowire covered by the PE gate, by optical microscopy. We take typical values of \(\epsilon_r = 20\) and \(t = 1 \text{ nm}\) for a polyethylene oxide formulation similar to ours from Takeya et al. [32] and thereby obtain \(C \approx 0.12 \text{ pF}\). This gives a capacitance per area of 17 \(\mu\text{F/cm}^2\), which is consistent with the 10 \(\mu\text{F/cm}^2\) typical of polyethylene oxide-based polymer electrolytes [13]. With a measured transconductance \(g_m = 175 \text{nS}\) at \(V_{sd} = 100 \text{mV}\) for the data in Fig. 1(b), we obtain \(\mu_{FE} \approx 0.3 \text{ cm}^2/\text{Vs}\). The field-effect mobility is low compared to, e.g., InAs nanowire transistors, but this is not unexpected given the much higher effective mass \(m^* \approx 0.35m_0\) for 1D-confined holes in GaAs [32] (c.f., \(m^* \approx 0.023m_0\) for electrons in InAs nanowires [34]), and the fact that conduction occurs largely via a thin, heavily-doped shell in our devices.

**IV. DISCUSSION**

We now put our results into context with other p-type III-V NWFETs. The most promising alternate III-V is GaSb, which is intrinsically p-type even when undoped due to native antisite defects [35, 36]. Dey et al. [10] recently reported on single InAs/GaSb nanowire CMOS inverters with a GaSb p-MOSFET sub-threshold swing \(S = 400 \text{mV/dec}\), on-off ratio \(\sim 10^{1.8}\) and on-resistance \(R_{on} > 1.2 \text{ M}\Omega\). Our device in Fig. 1(b) surpasses all three performance metrics. The on-resistance for GaSb NWFETs can be improved by Zn doping [37] but this compromises on sub-threshold swing, as for GaAs p-MOSFETs [12]. Babadi et al. [37] obtain \(R_{on} \approx 26 \text{k}\Omega\) with \(S \approx 820 \text{mV/dec}\) for moderate Zn doping and short channel length \(L = 200 \text{ nm}\) but lose pinch-off for longer channels and/or higher doping levels. The one aspect where our PE-gated GaAs NWFETs fall behind is ac response. The InAs/GaSb CMOS inverter of Dey et al. shows square-wave fidelity loss at \(\sim 10 \text{ kHz}\) [10]. We currently experience fidelity loss at \(\sim 10 \text{ Hz}\) due to the limited ionic conductivity of our PE, but our estimates suggest \(\sim 1 \text{ kHz}\) is possible with some engineering of the PE and device design [14], whilst MHz operation of other PE-gated devices is well established [15]. A key limitation of polyethylene oxide-based electrolyte gates is their strong affinity for water and hygroscopic nature, which makes their performance sensitive to ambient humidity.
and hydration accumulated during processing \[14\]. We expect improved performance to be obtained by a shift to other electrolyte-gate materials see, e.g., discussion in Kim et al. \[15\], as well as through further engineering of $N_d$ and the device architecture; this will be the subject of future work.

Briefly considering other $p$-type III-Vs, $p$-InAs gives ambipolar behaviour because conduction via the sub-surface electron layer from surface Fermi-level pinning competes with hole conduction in the core \[38\]. This competition leads to poor off-current and sub-threshold slope performance albeit with low contact resistance at room temperature \[38\]. $p$-InP is likewise ambipolar. The higher band-gap of InP aids with off-current suppression giving on-off ratio $> 10^2$ with $S \sim 220$ mV/dec but low $I_{on} < 10$ pA \[5\]. In contrast, InSb has the smallest bandgap and gives the poorest performance in the role of room temperature $p$-NFLFET \[39\].

V. CONCLUSION

We have shown that electrolyte gating remains effective in nanowire transistors where the doping level is sufficiently high that traditional metal-oxide gate formulations fail completely. We exploit this to obtain $p$-GaAs nanowire transistors that surpass other III-V $p$-type nanowire MOSFETs on a combination of three performance metrics: sub-threshold swing, on-off ratio and on-resistance. The latter is achieved via the high doping density which necessitates electrolyte gating for functional gating. We obtain a sub-threshold swing of $75 \pm 15$ mV/dec, within 25% of the room-temperature thermal limit, and comparable with the best $n$-type nanowire MOSFETs. Additionally, our gate structures show low hysteresis in the sub-threshold regime, are easier to fabricate than metal-oxide gate structures, and feature an inherently biocompatible material. Our results point an interesting path to extending the performance and application of nanowire transistors, and motivate further work on improved electrolyte materials for nanoscale device and bioelectronics applications.

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