Minimum leakage current optimization on 22 nm SOI NMOS device with HfO$_2$/WSi$_x$/Graphene gate structure using Taguchi method.

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Abstract. To acquire the optimal value of the performance parameter, a bilayer graphene with silicon on insulator (SOI) was enhanced and analyzed on 22 nm NMOS device. The device is made of Hafnium Dioxide (HfO$_2$) as a high-k material whereas Tungsten Silicide (WSi$_x$) as a metal gate. The Silvaco software ATHENA and ATLAS modules were applied to simulate the fabrication process of virtual devices and to verify the device's electrical properties accordingly. The Taguchi L9 orthogonal array method was then used to enhance the device process parameters minimum leakage current ($I_{LEAK}$) according to the International Technology Roadmap Semiconductor (ITRS) specification of 100nA/µm maximum range. The result from smaller-the-better (STB) for $I_{LEAK}$ is then reviewed by the percentage affecting the process parameter. The simulation result shows that the halo tilting angle is the most dominant factor for $I_{LEAK}$ optimization process. The optimized results indicate excellent device performance with $I_{LEAK} = 9.29746$ nA/µm which is far lower than the prediction.

1. Introduction
The endless method challenge of scaling down to pull extra transistors into a chip, invented by Gordon E. Moore, which has resulted in the creation of proposed new device design and materials [1]. The International Technology Roadmap for Semiconductor (ITRS) recommended this creation for a successful device scaling in the next 15 years [2]. Evaluation of technologies for complementary metal oxide semiconductor (CMOS) requires low power for fast-growing mobile applications that can deliver low standby power, improved performance and active power without high costs. Pursuant to the above requirements, one of the most promising technologies for low-power applications is a high-permittivity (high-k)/metal gate [3]. A high k/metal gate (HKMG) transistor is the ideal option to replace the SiO$_2$/poly-gate that is expected to resolve the current leakage extremity [4]. Recently, 2-dimensional carbon material known as graphene has become popular in the design of the planar metal-oxide-semiconductor field-effect transistor (MOSFET). Because of its excellent properties, single and bi-layer
graphene was used as a channel. However, it was then restricted due to energy gap defects [2]. Together with the application of high-k metal gate pairings, bilayer graphene was implemented as the top gate to produce the bandgap, control the drainage current and maximum the carrier's mobility through the channel.

At this stage, the top-gated bilayer graphene was simulated in the evaluation of the performance of the device and will now be optimized using the robust Taguchi method analysis [2]. Finally, the introduction of a method called buried oxide deposition has had a significant impact on MOSFET technology. This improved method, known as silicon on insulator (SOI) MOSFET, can further improve the electrical properties of MOSFET. This is due to the benefit of SOI expertise that can lessen the short-channel effect (SCE) problem [5].

The purpose was to investigate the manner in which different parameters affect the S/N ratio and mean factor of device performance. The results also outline how well the whole process is operating. This, at once, will help for the production of a high-quality device at a low cost to the manufacturer.

HKMG materials are used in this paper using hafnium dioxide (HfO$_2$) as a high-k material and tungsten silicide (WSi$_x$) as a metal gate. Based on the previous paper, high-k dielectric permittivity such as materials based on Hafnium has magnificent electrical characteristics and thermal stability. By achieving low current of leakage, it will be advantageous [6]. It is used as a metal gate for tungsten silicide (WSi$_x$) because it has a mid-gap metal that is found to deliver high drive current when using a proper retrograde channel [7]. However, due to scaling on the device and accurate concentrations of doping should also be considered as this will severely affect the performance of the device.

A comprehensive study was conducted to investigate the performance of the device before the optimization process in future research can be carried out. The results are as shown in this paper and are achieved by executing variations of process parameters in several implantation dosages. In the International Technology Roadmap for Semiconductors (ITRS) prediction, a 22 nm gate-length HfO$_2$/WSi$_x$ gate was virtually patterned successfully. From ITRS prediction, the I$_{OFF}$ is expected to be equal to or less than 100 nA/um for excellent SCE suppression [4].

2. **Experiment description**

2.1. **Virtual Fabrication of 22 nm Bilayer Graphene NMOS with SOI**

The fabrication recipe is summarized in Table 1. The completed device and its close-up views for 22 nm bilayer graphene NMOS with SOI are shown in Figure 1(a) and Figure 1(b) respectively. The doping profile of the device can be view in Figure 2. The device was then ready for the simulation of the electrical characteristic performance, which was measured through ATLAS module.
Table 1. Bilayer NMOS with SOI Fabrication Recipe.

| Process Step                      | n-type MOSFET Parameters                                                                 |
|-----------------------------------|------------------------------------------------------------------------------------------|
| Substrate                         | Silicon                                                                                  |
|                                   | <100> orientation                                                                        |
| Retrograde well                   | 200Å oxide screen by 999°C, 20 min of dry oxygen                                          |
| implantation                      | 3.75x10^{12} ions/cm² Boron                                                            |
|                                   | 30 min, 900°C diffused in nitrogen                                                      |
|                                   | 36 min, dry oxygen                                                                       |
| Box formation (SOI)               | 0.30 µm SiO₂                                                                              |
| STI isolation (X)                 | 130Å stress buffer by 900°C, 20 min of dry oxygen                                         |
|                                   | 1500 Si₃N₄, applying LPCVD                                                               |
|                                   | 1.0µm photoresist deposition                                                             |
|                                   | 5min annealing at 900°C                                                                  |
| Gate oxide                        | Diffused dry oxygen for 0.1 min, 805°C                                                  |
| Vth adjust implant                | 7.5x10^{10} ions/cm² Boron difluoride                                                   |
|                                   | 5KeV implant energy, 7° tilt                                                            |
|                                   | 20 min annealing at 800°C                                                               |
| Halo implantation (A, B)          | 1.05x10^{13} ions/cm² Indium                                                            |
|                                   | 33° tilt                                                                                 |
| Bilayer graphene deposition       | 0.005µm graphene                                                                         |
|                                   | Permittivity: 2.4                                                                        |
| High-k/metal gate deposition      | 0.002µm HfO₂                                                                             |
|                                   | 0.05µm WSiₓ                                                                              |
|                                   | 3.5 min, 850°C annealing                                                                 |
| Sidewall spacer deposition        | 0.010µm Si₃N₄                                                                            |
| S/D implantation (C)              | 4.80x10^{14} ions/cm² Arsenic                                                           |
|                                   | 12KeV implant energy                                                                     |
|                                   | 7° tilt                                                                                  |
| PMD deposition (D, Y)             | 0.015µm BPSG                                                                             |
|                                   | 20 min, 855°C annealing                                                                  |
|                                   | 1.00x10^{12} ions/cm² Phosphorous                                                       |
|                                   | 60KeV implant energy                                                                     |
|                                   | 7° tilt                                                                                  |
| Metal 1                           | 0.015µm Aluminum                                                                         |
| IMD deposition                    | 0.05µm BPSG                                                                              |
|                                   | 15 min, 950°C annealing                                                                  |
| Metal 2                           | 0.06µm Aluminum                                                                          |
Figure 1. (a) A complete device of 22 nm bilayer graphene with SOI NMOS virtual transistor, (b) zoom in of 22 nm gate length.

Figure 2. Doping profile of the device.
2.2. Semi-analytical approach for Bilayer Graphene

In the device simulation for this project, the physical effects of graphene material are considered. The entire operation was carried out at room temperature (T=300 K) with a bandgap of 0.55 eV, permittivity of 2.4, carrier mobility with top-gated material, a high value of 100 ns for radiative electron recombination rate and holes, and an effective field of $E_{\text{eff}} = 0.4 \text{MV/cm}^2$, while the electron and hole densities of the states were calculated and obtained from Equation (1) and Equation (2) [2].

$$N_c = \frac{8\pi m_e kT}{\hbar^2} \ln 1 + \left( e^{-((E_c-E_f)/kT)} \right)$$  \hspace{1cm} (1)

$$N_v = \frac{8\pi m_h kT}{\hbar^2} \ln 1 + \left( e^{-((E_f-E_v)/kT)} \right)$$  \hspace{1cm} (2)

Graphene electrons and holes have been set to $m_e \approx 0.06 \text{ mo}$, $m_h \approx 0.03 \text{ mo}$ where mo is the free electron mass [8].

2.3. Taguchi Method to Parameter Design

The Taguchi method is a measurement of robustness that classifies the control factors that reduce the effect of noise factors to lower process variability. The process parameters controlled are the control factors. Since noise factors cannot be controlled while the product is in use, experiments have been carried out to manipulate the noise factor for variability. The result identifies the optimal control factor setting which makes the process robust to vary from noise to noise. The control factor settings that reduce the influence of the noise factor determine the highest value of the signal to noise ratio (SNR).

There are two steps in the Taguchi method of optimization that use the SNR first to analyze the control factors that reduce the variability. Then, the control factor that moves the mean to the target that has no effect on the SNR is identified. There are various noise conditions which can be measured with the SNR. In this project, smaller-the-better (STB) analysis is used to minimizing $I_{\text{LEAK}}$ value.

Taguchi L9 is introduced to extract minimum significant data with the smallest number of tests. It uses orthogonal arrays (OA) with consist of four control factors (CF) and two noise factors (NF) in order to optimize the experimental design to create a matrix of experiments without overlooking any restrictions. The aim is to encourage researchers to effectively discover and analyze the effects of various manageable factors on the usual quality characteristics.

3. Result and analysis

3.1. Transistor electrical characteristic in Silvaco ATLAS

Using Silvaco ATLAS, the electrical properties curves of the designed device are achieved. Figure 3 illustrates the NMOS device's $I_{DS}$-$V_{DS}$ characteristics, while Figure 4 illustrates the NMOS device's $I_{DS}$-$V_{GS}$ characteristics. If the voltage of the gate ($V_{GS}$) is lower than the voltage of the threshold ($V_{TH}$), the current of drain leakage ($I_{OFF}$) or the current of sub-threshold leakage occurs. Ideally, when the transistor, $V_{GS} = 0 \text{ V}$ and $V_{DS} = V_{DD}$ (voltage supply) is turned off, there is no current in the channel ($I_{OFF}$). The excellent MOSFET design performance is when $I_{OFF} = 0 \text{ A}$. As the dimensions of the device decline, leakage currents develop one of the major limitations that need to be considered.
3.2. Analysis for 22 nm NMOS device

L9 Taguchi method was introduced to extract reliable significant data with the least number of experiments. By utilizes Orthogonal Arrays (OA) technique, the goals are to help analysis researcher to learn and analyze the impact of various process parameter factors in order to find the most quality characteristics efficiently. The parameters’ values for CF and NF at each level are as depicted in Table 2 and Table 3 respectively.

The I_{LEAK} data results of the L9 array for 36 simulations are following shown in Table 4. Based on the results, the significant control factors for the mean, variance, and SNR process parameters must be determined. A control factor is a factor that increases the efficiency of the device characteristics. The SNR function is to ensure that the design is fully comprehensive to the variations. To achieve a minimum I_{LEAK} value in accordance with ITRS prediction, STB SNR analysis is used in this experiment, and the process parameter for each level is calculated. The SNR value is consistently increasing and decreasing to performance regardless of the performance characteristics category [9]. The I_{LEAK} of the device is optimized using SNR of Smaller-the-Better, STB, \eta_{STB} where it can be expressed as [10]:

$$\eta_{STB} = -10\log_{10}\left[\frac{1}{n}\sum(Y_1^2 + Y_2^2 + ... Y_n^2)\right]$$

where \( n \) is number of tests, \( Y_i \) is the experimental value of the leakage current. By applying the formula given in Equation (1), the \( \eta_{STB} \) were calculated as given in Table 5.

| Table 2. Control Factor. |
|--------------------------|
| Factor | Process Parameter | Unit         | Level 1 | Level 2 | Level 3 |
| A      | HALO Implantation Dose (\(\times10^{13}\)) | Atom/cm\(^3\) | 1.00    | 1.05    | 1.10    |
| B      | Halo Tilting Angle | Degree      | 30      | 33      | 36      |
| C      | S/D Implantation Dose (\(\times10^{14}\)) | Atom/cm\(^3\) | 4.79    | 4.80    | 4.81    |
| D      | Compensation Implantation Dose (\(\times10^{12}\)) | Atom/cm\(^3\) | 0.99    | 1.00    | 1.01    |
### Table 3. Noise Factors.

| Factor | Noise Factor                      | Unit | Level 1 | Level 2 |
|--------|-----------------------------------|------|---------|---------|
| X      | PSG annealing temperature         | °C   | 900 (X0) | 902 (X1) |
| Y      | BPSG Oxide annealing temperature  | °C   | 855 (Y0) | 857 (Y1) |

### Table 4. Result of $I_{\text{LEAK}}$.

| Exp. No. | $I_{\text{LEAK}}$ (nA/µm) |
|----------|-----------------------------|
|          | X0Y0 | X0Y1 | X1Y0 | X1Y1 |
| 1        | 7.49417 | 7.85777 | 7.78937 | 7.85915 |
| 2        | 8.18484 | 8.26419 | 8.52913 | 8.61223 |
| 3        | 9.29750 | 9.38749 | 9.64959 | 9.73594 |
| 4        | 7.00835 | 7.05443 | 7.23833 | 7.29050 |
| 5        | 7.53250 | 7.59580 | 7.82930 | 7.89890 |
| 6        | 8.44053 | 8.52770 | 8.79380 | 8.88180 |
| 7        | 6.68103 | 6.71240 | 6.85210 | 6.88950 |
| 8        | 7.02785 | 7.07320 | 7.26040 | 7.31110 |
| 9        | 7.77477 | 7.84560 | 8.09290 | 8.16870 |

3.3. Analysis of variance (ANOVA)

ANOVA is a common statistical analysis designed to recognize the contribution percentage for each factor involved. In Table 5, the results of ANOVA for $I_{\text{LEAK}}$ for the NMOS device is given. The dominant factor for finding the best combination of process parameters can be determined from the table. The percentage of the SNR effect factor shows a process parameter's preference to scale down the variation [11].

### Table 5. S/N Response and ANOVA Result for $I_{\text{LEAK}}$.

| Factor | S/N Ratio (mean) | Total mean S/N ratio | Factor Effect (%) |
|--------|------------------|----------------------|-------------------|
|        | Level 1 | Level 2 | Level 3 |                    |                   |
| A      | 161.39   | 162.14   | 162.74   | 162.09              | 41                |
| B      | 162.83   | 162.22   | 161.21   | 162.09              | 58                |
| C      | 162.12   | 162.13   | 162.02   | 162.09              | 0.55              |
| D      | 162.14   | 162.04   | 162.08   | 162.09              | 0.45              |

The results of the factor effect on SNR of STB show that Factor B (Halo Tilting Angle) with the highest percentage of 58.0% is the most dominant factor in the influencing $I_{\text{LEAK}}$ resulting from the NMOS device.

3.4. Optimum factor combination

Based on Table 5, the highest value of SNR (mean) for each factor indicates the best level for designing the device. The combination of parameters that have finalized for an optimized for NMOS devices for $I_{\text{LEAK}}$ are level A, B, C and D. The best-predicted setting for the process parameter combination for $I_{\text{LEAK}}$ by Taguchi method is shown in Table 6. These final parameters were then simulated with the noise factor to obtain the optimum result for minimum $I_{\text{LEAK}}$ as shown in Table 7.

Following the final improvement of the noise factor parameter process, the results obtained for the $I_{\text{LEAK}}$ value are lower compared to the ITRS prediction value. After the final optimization, the lowest $I_{\text{LEAK}}$ at noise X0 and Y0 is 9.29746 nA/µm. Table 8 shows that $I_{\text{LEAK}}$ values are consistent with the ITRS and better scores after optimization.
Table 6. Best Combination of the Process parameters (I_{LEAK}).

| Factor | Process Parameter | Unit       | Level | Best Value |
|--------|-------------------|------------|-------|------------|
| A      | HALO Implantation Dose | (×10^{13}) | Atom/cm | 3 | 1.10 |
| B      | Halo Tilting Angle | Degree | 1 | 30 |
| C      | S/D Implantation Dose | (×10^{14}) | Atom/cm | 2 | 4.80 |
| D      | Compensation Implantation | (×10^{12}) | Atom/cm | 1 | 0.99 |

Table 7. Final Result of I_{LEAK} with added Noise.

| I_{LEAK} 1 (nA/µm) | I_{LEAK} 2 (nA/µm) | I_{LEAK} 3 (nA/µm) | I_{LEAK} 4 (nA/µm) |
|---------------------|---------------------|---------------------|---------------------|
| (X0, Y0)            | (X0, Y1)            | (X1, Y0)            | (X1, Y1)            |
| 9.29746             | 9.38641             | 9.64907             | 9.73526             |

Table 8. Simulation Results versus ITRS Prediction.

| Performance Parameter | ITRS Prediction | Non-Optimized Result | Optimized Result |
|-----------------------|-----------------|----------------------|------------------|
| I_{LEAK} (nA/µm)     | < 100           | 7.52102              | 9.29746         |

4. Conclusion
The 22 nm SOI NMOS device with virtual design of HfO_{2}/WSi_{2}/graphene gate structure and Taguchi method design analysis is presented briefly. The design of the NMOS transistor is suitable for the performance analysis design parameter studies. Halo implantations, halo tilting angle, S/D implantation and compensation implant are the four parameters used as control factors for the L9 Taguchi orthogonal method. Taguchi analysis improves researchers to analyze the parameter that most influenced the performance of the device and helped optimize the reliability of the design [12]. Halo tilting angle is finding as a dominant factor in this research. Every change in the dopant value of control factor completely affects the performance of the device. Finally, the device design using virtual simulation with aid in Taguchi method analysis found the reliable result as predicted from ITRS focuses [13].

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References
[1] A H Afifah Maheran, P S Menon, I Ahmad, and S Shaari Optimisation of Process Parameters for Lower Leakage Current in 22 nm n-type MOSFET Device using Taguchi Method 2014 J. Teknologi (Sciences Eng.) 4 45–49
[2] Z A Noor Faizah, I Ahmad, P J Ker, P S Menon and A H Afifah Maheran VTH and I_{LEAK} Optimization using Taguchi Method at 32nm Bilayer Graphene PMOS 2017 J. Telecommun. Electron. Comput. Eng. 9 105–109
[3] L Xiao, H Deng, F Li, J Qi, J Zhao and B Zhang PMA Effects on Al/HfO2 High-k PMOS Capacitors 2016 China Semicond. Technol. Int. Conf. 1–4
[4] A H Afifah Maheran, P S Menon, I Ahmad, F Salehuddin, A S M Zain and N F Z A Control Factors Optimization on Threshold Voltage and Leakage Current in 22 nm NMOS Transistor Using Taguchi Method 2017 J. Telecommun. Electron. Comput. Eng. 9 137–141
[5] M N I A Aziz, F Salehuddin, A S M Zain and K E Kaharudin Study of Electrical Characteristic for 50nm and 10nm SOI Body Thickness in MOSFET Device 2015 J. Teknologi 77 109–115
[6] A H Afifah Maheran, P S Menon, I Ahmad and S Shaari Effect of Halo structure variations on the threshold voltage of a 22nm gate length NMOS transistor 2014 *Mater. Sci. Semicond. Process.* **17** 155–161.

[7] H Sun, L Fang, Y Wang, Y Chi and R Liu A low contact resistance graphene field effect transistor with single-layer-channel and multi-layer-contact 2018 *IEEE Int. Symp. Nanoscale Archit.* 139–144

[8] A F Roslan, K E Kaharudin, F Salehuddin, A S M Zain, I Ahmad, Z A Noor Faizah, H Hazura, A R Hanim, S K Idris, A M Zaiton, N R Mohamad and A H Afifah Maheran Optimization of 10nm Bi-GFET Device for higher ION/IOFF ratio using Taguchi Method 2018 *J. Phys. Conf. Ser.* **1123** 012046

[9] A H Afifah Maheran, P S Menon, I Ahmad, S Shaari, H A Elgomati and F Salehuddin Design and Optimization of 22 nm Gate Length High-k/Metal gate NMOS Transistor 2013 *J. Phys. Conf. Ser.* **431** 1–9

[10] A H Afifah Maheran, P S Menon, I Ahmad, F Salehuddin and A S M Zain Process Parameter Optimisation for Minimum Leakage Current in a 22nm p-type MOSFET using Taguchi Method 2016 *J. Telecommun. Electron. Comput. Eng.* **8**, 19–23

[11] K E Kaharudin, A H Hamidon and F Salehuddin Implementation of taguchi Modeling for Higher Drive Current (ION) in Vertical DG-MOSFET Device 2014 *J. Telecommun. Electron. Comput. Eng.* **6** 11–17

[12] K E Kaharudin, F Salehuddin, A H Hamidon, M N I A Aziz and I. Ahmad Taguchi Modelling of Process Parameters in VDG-MOSFET Device for Higher Ion/Ioff Ratio 2015 *J. Teknologi* **21** 19–26

[13] ITRS, “ITRS Report,” 2012.