A 100-140 GHz SiGe-BiCMOS Sub-Harmonic Down-Converter Mixer

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\textbf{Abstract}— This paper presents an F-band bottom-LO down-converter transconductance sub-harmonic mixer in a commercial 130-nm SiGe-BiCMOS process for broadband applications. The mixer features a high conversion gain and good linearity using a frequency doubling LO-stage, a differential switched-transconductance RF-stage, and two emitter-follower IF-stages without any amplifier. It exhibits an input referred 1-dB compression point of -7.2 dBm and a maximum conversion gain up to 2.6 dB with a DC power of 46.3 mW, including 26.7 mW for the IF buffers. The measured results demonstrates a wide 3-dB IF bandwidth up to 12 GHz, which to the authors’ best knowledge, is the highest obtained among active sub-harmonic mixers operating above 100 GHz. The chip occupies 0.4 mm\textsuperscript{2}, including pads.

\textbf{Keywords}— SiGe MMICs, millimeter-wave, above 100 GHz, sub-harmonic mixer (SHM), down-converter, broadband circuits.

\section{I. INTRODUCTION}

The sub-harmonic mixer (SHM) is an attractive candidate for frequency conversion in micro-wave and millimeter-wave transceivers \cite{1}. It requires only a fraction of the local oscillator (LO) frequency compared to a fundamental mixer and increases the LO-to-RF isolation significantly. Unfortunately, most of the high frequency SHMs above 100 GHz have relatively conversion loss, which imposes severe noise figure (NF), gain and linearity requirements on the low noise amplifier and following building blocks of receiver chain \cite{2,3,4}. On the other hand, to realize a high gain amplifier at the RF or IF side, usually three to five stages are utilized, where it burdens the power budget of a low power system. Therefore, implementing a millimeter-wave down-converter SHM is challenging with respect to conversion gain, bandwidth, NF and linearity requirements.

Recently, several efforts have been done in literature to develop millimeter-wave SHMs with improved performance. In \cite{5}, a transformer-based gm-boosting SHM is presented operating at 79 GHz, where a conversion gain of 1.6 dB and NF of 13 dB is achieved with a LO power of -5 dBm. This technique boosts the RF transconductance without additional power consumption. However, it is not appropriate for operating frequencies above 100 GHz due to the additional loss of transformer network. In \cite{6}, a modified Gilbert-cell based on two stacked switching quads is reported for 122 GHz. This topology shows better conversion gain compared to a Gilbert-cell configuration with parallel transistor pairs, which is adopted in \cite{7} due to its higher operating frequency. However, as the frequency goes up, the maximum conversion gain and accordingly minimum NF occurs by non-quadrature LO signals due to the delay produced in RF path from the emitter to the collector of the switching stage \cite{8}. Hence, a novel hybrid with an arbitrary phase shift is needed in order to provide an optimum LO phase distribution. Furthermore, owing to the several stacked transistors, a larger supply voltage is required to avoid the compression of the output voltage amplitude, which inevitably influences the power consumption of whole circuit. In \cite{4,9} a two-stage sub-harmonically base-pumped transconducance mixer is introduced that reaches to a maximum -1 dB and 9 dB conversion gain at D-band and V-band using a -1 dBm and 2 dBm LO power, respectively. This type of mixer utilizes the internal mixing of RF signal with the second- or higher-order harmonics of the LO signal, generated by nonlinearities of transistor itself. It features a better gain performance compared to a passive SHM \cite{10}, and a decent NF, however it has rather high conversion loss in sub-harmonic operation and requires a lower base bias along with a typically large driving LO power to fulfill the optimum conduction duty cycle \cite{4}. Therefore, a power hungry IF buffer amplifier is usually exploited at the output, which correspondingly leads to a high power consumption, e.g. 120 nW \cite{4} and 262 mW \cite{9}.

This paper presents a high conversion gain and a broadband transconducance SHM based on a bottom-LO frequency doubler to operate at 100 to 140 GHz frequency range. The aim of this work is to benchmark the performance of this topology above 100 GHz in a 130-nm SiGe-BiCMOS technology for the first time. To improve the gain-bandwidth and linearity characteristics of mixer, several techniques and approaches have been employed and followed from different publications.

\section{II. CIRCUIT IMPLEMENTATION}

The idea of a transconductance SHM with a bottom-LO frequency doubler was first demonstrated at 930 MHz \cite{11} and is well described in \cite{12}. Unlike a standard Gilbert-cell topology which implements the mixer function by a trans-
Both mixer core and buffers are biased with current sources, regulated by a reference current. Subsequently, a high current or a low current can be injected into the circuit, which accordingly offers a high linearity or moderate linearity operation. Regarding low break-down voltage of transistors, two series resistors of $150 \, \Omega$ ($R_{E1}/R_{E2}$), are placed at the collector of output current sources to prevent any damage under high current levels.

In order to achieve a wideband RF operation, Marchand baluns with broadside coupled lines are applied at both RF and LO ports [13]. A further improvement is done on baluns by removing the ground layer (M4) under the signal lines resulting to more compact layout and lower insertion loss [14]. Fig. 2 exhibits the simulated performance of each balun in terms of phase and amplitude imbalance, while the minimum loss is $-1.3 \, \text{dB}$ and $-2 \, \text{dB}$, for RF and LO signals respectively.

As is seen in RF balun, the amplitude imbalance is better than $0.4 \, \text{dB}$ and the maximum phase difference is 3 degree. The LO balun also shows a maximum amplitude imbalance of $0.8 \, \text{dB}$ with a phase difference of 4 degree.

The high frequency RF signal is applied through a shunt spiral inductor ($L_{1}/L_{2}$) accompanied by a series line ($TL_{1}/TL_{2}$) to transform the low input impedance of transistor base to a higher value [3]. To do this, custom inductors are designed with one-turn symmetric structure on M6, where the simulated value of each inductor is about $20 \, \mu\text{H}$.

To increase the LO swing across the emitter terminal of the RF transistors, a tuning-out series line ($TL_{3}$) is adopted between RF and LO stages, implementing a $\pi$-network [15]. This network provides a higher conversion gain at lower LO powers and slightly enhances the RF-bandwidth of the mixer. Finally, the collector loads ($R_{C1}/R_{C2}$) incorporate $150 \, \Omega$ resistors to provide a broadband IF response under a low supply voltage.

All passive components are simulated with a 2.5D planar EM-simulator using Sonnet/Cadence interface. The high frequency signal pads are also shielded from the substrate by a grounded layer and its capacitance is included in the simulation results.

Fig. 1. Single-balanced broadband SHM (a) circuit view (b) chip photo, active area: 0.215 mm$^2$, total area: 0.4 mm$^2$.

Fig. 2. Simulated amplitude imbalance and phase difference of (a) RF (b) LO.
A SHM circuit is designed and fabricated in a 130-nm SiGe-BiCMOS process. This technology features high speed npn HBTs with maximum \( f_{\text{t}}/f_{\text{max}} \) of 250 GHz/370 GHz and \( B_{\text{CEO}} = 1.5 \) V. As shown in Fig. 1 (b), the chip occupies 600 \( \mu \)m \( \times \) 670 \( \mu \)m, while the active area including RF and LO baluns is only 500 \( \mu \)m \( \times \) 430 \( \mu \)m. To characterize the mixer performance, on-wafer measurements are carried out. The RF signal is generated and calibrated using a Keysight N5242A microwave network analyzer from 10 MHz to 26.5 GHz and a N5262BW08, WR 8.0 based frequency converter to extend the frequency range from 90 to 140 GHz. The LO signal is provided from an Agilent E8257D, 250 KHz to 67 GHz PSG signal generator. A Rohde and Schwarz spectrum analyzer is used to measure the IF signal.

Fig. 3 shows the measured conversion gain, input referred P1dB, and the total power consumption of circuit as a function of collector current in the mixer core (\( I_{\text{cc, mixer}} \)), while the LO-power is fixed at 5 dBm. As can be seen, the conversion gain enhances with increasing the collector current of mixer core, which is controlled by a reference voltage \( (V_{\text{ref}}) \) until it reaches to maximum value of 2.4 dB at \( I_{\text{cc, mixer}} = 6.2 \) mA. Consequently, the input P1dB also improves and the total power consumption rapidly grows due to the high current levels of buffer-stages, where a -2.2 dBm input power at a 1-

dB compression point is achieved with a power dissipation of 58.4 mW.

The variation of mixer conversion gain versus LO power is shown in Fig. 4 at a LO frequency of 57.5 GHz, RF frequency of 113 GHz and IF frequency of 2 GHz. A good agreement is obtained between simulation and measurement results. It demonstrates a positive gain from LO input power of +1 dBm. The LO frequency is swept from 46 to 68 GHz with an input power of 5 dBm, while the IF frequency is fixed at 2 GHz. As shown in Fig. 5, an RF frequency range from 98 to 140 GHz is achieved with a conversion gain of -0.4 to 2.6 dB, which represents more than 40 GHz 3-dB bandwidth. The 2LO-to-RF isolation is better than 45 dB over the entire bandwidth.

The measured IF response at LO frequency equal to 61 GHz is shown in Fig. 6. The results indicate a flat conversion gain, and 3-dB IF bandwidth is 12 GHz from 1 to 13 GHz. This is the widest IF bandwidth among silicon-based active sub-harmonic mixers operating above 100 GHz.

Finally, Fig. 7 describes the output power at 2 GHz versus input power at RF frequency of 113 GHz. It can be seen, the circuit has a 1-dB compression at \(-7.2\) dBm input power. The total power consumption is only 46.3 mW.

The simulated single-side band NF of the mixer is below 16 dB over the entire IF bandwidth, which is decent enough to be preceded by an LNA with a moderate NF.

In Table I, the performance of the presented SHM and other published results in the literature are listed. It can be seen that our SHM achieves competitive conversion gain, and record IF bandwidth with a good linearity.
Fig. 7. Measured IF output power and conversion gain as a function of the RF input power at a fixed RF and IF frequency of 113 GHz and 2 GHz, respectively.

IV. CONCLUSIONS

A wideband sub-harmonic bottom-LO down converting transconductance SHM is designed and presented in a 130-nm SiGe-BiCMOS process for F-band applications. This mixer features a high conversion gain up to 2.6 dB over the frequency range of 100 to 140 GHz with a LO power of 5 dBm. It demonstrates a good linearity and a wide IF bandwidth among the above 100 GHz active mixers. In addition, the SHM shows a port-to-port isolation better than 45 dB and a relatively small chip size.

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TABLE I PERFORMANCE SUMMARY OF 2X SHMs

| Ref. | Topology       | Process   | RF (GHz) | CGp (dB) | IF (GHz) | P1dB (dBm) | OP1dB (dBm) | 2LO-RF Iso. (dB) | PLO (dBm) | Psic (mW) | Area (mm²) |
|------|----------------|-----------|----------|----------|----------|------------|-------------|-----------------|------------|-----------|------------|
| [2]  | leveled Gilbert | 90nm CMOS | 30-100   | 0        | 0.1      | -8.6       | -9.6        | 47              | 10         | 58        | 0.35       |
| [3]  | resist.+ IF Amp. | 32 nm SOI CMOS | 158-182 | +8**     | 1-6      | -          | -            | -               | 4          | 74        | 0.75       |
| [4]  | trans.+ IF Amp. | 230 nm InP DHBT | 110-170 | -1       | 5        | -          | -            | 40              | -1         | 262       | 0.825      |
| [5]  | gm-boost Gilbert | 65 nm CMOS | 75-81    | 3.4      | 0.5      | -16.2      | -15.6       | 38              | -5         | 12        | 0.31       |
| [6]  | stacked Gilbert | 130 nm SiGe:C | 125-129 | 4        | -        | -          | -            | -               | 9          | 89.1      | -          |
| [9]  | trans.+ IF Amp. | 250 nm InP DHBT | 55-67   | 6        | 0.25-3   | -2         | 3           | 40              | 5          | 120       | 0.63       |
| [16] | Amp. + APDP    | 90 nm CMOS | 33-103  | -0.5     | 1        | -3         | 5**         | 60              | 10         | 24.5      | 0.49       |
| This Work | bottom-LO trans. | 130 nm SiGe | 98-140 | 2.6      | 1-13     | -7.2       | -6          | 45              | 5          | 46.3      | 0.4        |

CGp = peak conversion gain, **simulated stand-alone mixer gain is -23 dB, **by estimated mixer loss, resist=resitive, Amp=amplifier trans.=transconductance, APDP = anti-parallel diode pair