Some Like It Cold: Initial Testing Results for Cryogenic Computing Components

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Abstract. With the exponential growth of bandwidth demands on present data centers, we are researching the feasibility of deploying cryogenic DRAM based memory subsystems for the next generation of higher bandwidth, more efficient, lower cost and smaller footprint data centers of the future. As part of our early research, we are designing DRAM based subsystems that operate at 77K and are submerged in liquid nitrogen. To effectively test the memory subsystem at cryogenic temperatures, creative test methods must be employed. This paper illustrates the test setups, procedures and methodologies that were used to successfully test DRAM based subsystems at cryogenic temperatures.

1. Introduction
Rapidly evolving workloads and exploding data volumes place intense pressure on data-center performance. As one option, Quantum Computing promises to solve currently intractable problems, allowing us to keep up much better with this data deluge. Another type of emerging, superconducting coprocessor is built from Single Flux Quantum (SFQ) logic circuits that operate at the temperature of liquid helium. Such devices offer the potential to increase processor speeds and bandwidth by two orders of magnitude, reduce overall energy by two orders of magnitude, and cut memory access time by 75% [1]. Despite these impressive properties, system power remains a large concern, given that such coprocessors are intended for use in warehouse-scale data centers [2]. These 4K coprocessors must still interact with classical processors that operate at temperatures around 300K. Ware et al. [3] claim that since the system will require an intermediate temperature domain as a thermal shield [4] between the cryogenic and ambient components, it makes sense to place the memory to support such cryogenic coprocessors in the intermediate domain. This can save substantially on cooling energy and costs and can improve performance by reducing data transport distance. As a near-term solution, we explore the use of mature DRAM technology in cryogenic memory subsystems.

Here we describe the setup and operation of the cryogenic lab we use to test and troubleshoot commercially available DRAM components employed in the design of such memory subsystems. We present initial results for DDR2 and DDR3 DRAMs from multiple vendors. While we demonstrate that commercial DRAMs designed for ambient temperature operation can also function at 77K, we observe that there is little power savings when using these unmodified parts. Retention times lengthen at 77K and provide the best opportunities for power savings and performance. Optimizing a DRAM for lowest power at 77K will require larger modifications and most likely process changes. We describe our root-cause analysis, discuss challenges and lessons learned, and make recommendations for architectural changes to improve cryogenic DRAM operation.
Our investigation of memory subsystem architectures for cryogenic operation considers the constraints imposed by today’s DRAM architecture and technology. We choose FPGAs to control and test the memory subsystem due to their availability, flexibility, and performance.

2. Background
While some attempts to operate various kinds of unmodified electronics at colder temperatures have largely failed [5, 6, 7], many others have at least partially succeeded, often by modifying the devices for the colder environments. For instance, Zebulum et al. [8] consider evolutionary configuration changes in addition to process and design changes to harden electronics at deep-space temperatures. Conway Lamb et al. [9] develop an instrumentation platform to enable signal routing, multiplexing, and complex digital signal processing close to devices within a cryostat. Their platform includes FPGAs operating at temperatures approaching 4K.

Charbon et al. [10] study cryogenic CMOS for scalable control circuitry in fault-tolerant quantum systems. They test many components — both active and passive — with different aspect ratios in two standard processes (40nm and 160nm bulk CMOS) at temperatures down to 40mK. They confirm the increase of mobility and threshold voltage in silicon at cryogenic temperatures and observe a higher $V_d$ due to impact ionization at the drain, finding that the ensuing substrate current and increase in substrate resistivity lower $V_T$. Nonetheless, they find that CMOS transistors are suitable for implementing multiplexing functions and other, more complex circuitry at deep-cryogenic temperatures.

Like us, Tannu et al. [11] perform a feasibility study of a cryogenic DRAM-based memory system by characterizing the minimum operating temperatures for off-the-shelf commercial DIMMs from five vendors, finding that 18% of their DIMMs exhibit errors, but that most of these DIMMs contain just one faulty DRAM. Since their focus is on cryogenic DRAM, they operate the hardware driving the DIMMs at ambient temperatures, and they omit root cause analysis of DRAM failures in this initial study. They, too, observe mostly single-bit errors that are amenable to existing error detection and correction approaches, and they note that cell sparing can help tolerate permanent faults. Chang et al. [12] perform an experimental study of DDR3 low-voltage DRAM chips from three major vendors. They find that reducing the supply voltage too much can introduce bit errors. Their characterization of this behavior indicates that the errors can be avoided by increasing the latencies of some major DRAM operations, which is consistent with our conclusions and observations of cryogenic DRAM operation.

2.1. DRAM Technology and Architecture at Low Temperatures
DRAMs are commodity parts, and thus the market necessity of minimizing their manufacturing costs severely constrains their design. Any changes we propose for better cryogenic operation must therefore affect the organization of these high-volume components as little as possible [13].

Lowering the operating temperature decreases both junction and subthreshold leakage, and it steepens the subthreshold slope. In an unmodified process, the threshold voltage increases so that operating voltage cannot be reduced due to the need to maintain gate overdrive. Our results show that leakage at 77K is already so low that retention time will no longer be leakage-limited, but limited by temperature-independent mechanisms like coupling between neighboring lines in a dense storage array. Memory latency in a computer system improves with closer physical proximity between DRAM and CPU. DRAMs at 4K would be closest to the CPU at 4K, but cooling would incur a very high overhead, while DRAMs at room temperature would be physically far away from the CPU and have the potential of large thermal leakage via the link between DRAM and CPU. A compromise could be to place the DRAMs in the intermediate temperature domain.

2.2. DRAM Testing
To test the memories at cryogenic temperatures, we need to use a variety of other devices, like FPGAs, sensors, and power supplies. These devices need to work in the temperature domain in which they are placed, and low temperatures affect their behavior in different manners. Some require work-arounds, some work partially, and others simply become unusable.
To control the memories, we use commercial FPGAs for their flexibility and programmability. We place them close to the memories to reduce cabling and to ensure signal integrity. This proximity also means that the FPGA gets cold, and sensitive parts like phase-locked loops (PLLs), serializer/deserializers (SerDes), Serial Peripheral Interface (SPI) bus controllers, power distribution, terminations, and even the general logic fabric can be affected. We keep the FPGAs around 230-240K, the minimum specified industrial range, when testing the memory to make sure it is not a factor in the memory testing. Incidentally, we have also tested some FPGA devices at 77K, finding that all parts of the device are operative. For our testing, we evaluate both the programmable logic and a pre-designed SerDes hard macro block to see if the overall features of the FPGA are operational and capable of supporting the DRAM testing.

3. Evaluation Methodology

We created an experimental setup fully equipped for detailed mechanical, functional, and parametric testing of components, ASICs, and boards at temperatures down to 77K. To reach that temperature we employ liquid nitrogen dewars because of their relative simplicity of use and the low overall cost of the experiments. A drawback of the nitrogen dewar is that it is complex to control the temperature, and so we designed methods to overcome this problem. The system’s main components are the liquid nitrogen dewar, the cryotube that helps manage the system in the dewar, the “sled” that provides rigidity and helps with cable management, the system control board, the FPGA board implementing the memory controller and pattern generators, and memory daughter card boards that carry the devices under test (DUTs). We have the option to use extender boards of various lengths to connect the FPGA board and the memory daughter cards.

We designed a stainless steel and aluminum tube that is used for lowering the system into the dewar. It acts as a thermal shield, helping to reduce the thermal shock of the DUTs, and its thermal mass acts as a temperature stabilizer. The cryotube together with the sled inside the tube also help to manage cables, provide support for the boards, and reduce condensation and frost on components being tested. When the cryotube meets the liquid nitrogen as it is lowered, its temperature drops dramatically, creating a sharp increase in the rate of change. To mitigate this thermal shock, we add copper braids to the aluminum tube bottom. The copper contacts the liquid nitrogen before the tube body, slowing the rate of change by decreasing the cross section of thermally conductive material moving heat away from the cryotube assembly earlier in the experiment. Small holes in the tube allow liquid nitrogen to flood the chamber for experiments at 77K. Canisters without holes are useful for experiments at less cold temperatures.

The aluminum sled holds the boards being tested and provides stability and thermal conductivity into the ground plane on the boards. Figure 3 shows the temperature gradient as the cryotube is lowered into the dewar. The process of raising and lowering the cryotube is relatively long. We automated this process with a step motor and a small microprocessor to control the speed and step size of the movement. The system can also be connected to a temperature probe to make a control loop. Since the DUT gets lowered into the dewar, the control and power must be located outside and connected to the DUT via cables. The system is grounded through these cables, and sensors are taken down to the boards to

Figure 1. System architecture
monitor and measure the power. We use serial protocols at relatively low frequency (JTAG, SPI, I2C) and a handful of general-purpose I/Os for health-monitoring and alarms.

3.1. Methodology
We perform three different families of tests: mechanical tests, functional tests, and thermal characterization. Our tests are designed to identify potential problems due to exposure of the material and components to low temperatures. The coefficient of thermal expansion (CTE) ends up being the most important parameter to investigate and understand. A high CTE can result in permanent damage to many of the boards, packages, and components in the system.

We lower the assembly into the liquid nitrogen at a speed that depends on the test to be done. Examples of these speeds are 0.33 inch per minute (for “gradual dip tests”) or within five seconds (“fast dip tests” for mechanical shock tests). The cryotube passes through three environmental regions. It starts in ambient air, typically at about 300K with 35% or more relative humidity. Then it enters the mixed air and nitrogen vapor, which lowers the temperature to about 130K. Finally, it enters the liquid nitrogen. The DUT remains submerged for a given period (depending on the test) and then is raised from the liquid nitrogen at a similar rate.

Mechanical tests are designed to evaluate the behavior of the materials and components at and in the transition to low temperature and do not normally require power or control. We use this setup to perform thermal characterization of the tools to be used, and perform mechanical tests of the DDR2 and DDR3 memory DIMMS. Functional electrical tests are done at room temperature prior to and after mechanical tests at cold temperature.

Characterization tests are also run to determine whether components or devices are appropriate for use in more complex boards. We test basic functionality under specific conditions to ensure that the parts are still active at cryogenic temperatures, e.g., to determine the range of frequencies at which we can operate a device for a given voltage and temperature combination. Other experiments require submerging boards in the dewar. These need more complex control and power.

Functional tests ensure that the parts still behave correctly at cryogenic temperatures. To run characterization and functional tests with memory devices, the controller board contains a pattern generator that can be configured to send different access patterns to the DUTs. The patterns can be generic or designed to provoke errors in a section of the memory.
4. Results

We performed mechanical tests on commercially available die. We studied five different DDR2 and DDR3 DIMM devices (D1 to D5) with different storage capacities and array architectures. All die correctly executed MEMTEST86+ in our powered PC even after repeated immersions. We observed no performance changes or delamination signs in the components, printed circuit boards, and packages. We lost some of the DIMM labels due to humidity, and we encountered some problems due to excessive cycling in the host connectors of the testing computers.

4.1. DRAM Characterization

We used six standard DDR2, DDR3L, and DDR3 DRAM device samples (S1 to S6). We experimented with 4-15 die of each, depending on availability. We tested the system with several voltage and frequency combinations (600, 800 and 1,000 Mbps) with the FPGA at ~233K and the memories at 77K. Initial experiments with the memories showed that the devices are very resilient to the temperature tests. All but one of the devices were completely functional at 77K, running error-free or with a very low bit error rate for the duration of our tests, depending on the pattern. One device had more errors below 140K because it has difficulties with link training at lower temperatures. None of the devices are designed for cryogenic temperatures.

The errors we observe point to characteristics of the devices, and thus most of the die samples of a given device naturally show similar characteristics. For instance, one of our devices shows sporadic errors only during pattern changes below 180K, while another’s bit error rate begins rising below 150K. All devices are designed for operation at or above 233K, and thus failures below 180K do not indicate fundamental problems or an inferior design or process. We also perform cold-start tests: we leave the devices in the cold for 5-10 minutes and then power them on and begin the initialization or link-training sequence. Although others have reported transistor malfunctions under such conditions [14] [5] [7], in most cases we find no differences in behavior from when the devices are powered on throughout the dipping process. Section 5 describes specific failures and our root-cause analysis efforts.

4.2. DRAM Power Consumption in Temperature

Figure 4 shows the comparison in temperature of power consumption in one of the tested samples. We tested each device in the same way and under the same conditions, yet we observed substantial differences in the power dissipation of the different samples. We cannot directly compare samples with differences in size, organization, and internal architecture, but, within the same sample, all devices showed a strong consistency in their results.

There were no trends with respect to operation at ambient temperatures versus cryogenic temperatures — particularly in read versus write operations. The current used in each experiment changed depending on the type of sample and the pattern used. Some of the variation might be due to internal voltages that are not at the target value since the device power system was not designed for 77K.

In general, it is not surprising that power consumption at 77K, under the same conditions of voltage, frequency, and refresh rate, is roughly the same as at room temperature: supply voltages cannot be
lowered without process modifications due to the increasing threshold voltages of the transistors reducing gate overdrive. Capacitances change little with temperature, so the active power of the CMOS circuits changes little. These results indicate that there is much opportunity to architect DRAMs to function better and to use less power at cryogenic temperatures.

4.3. Effect of Temperature on Retention Time
As expected, the number of retention fails goes down with the temperature. We observed fails at shorter retention tests (milliseconds or less) only at temperatures close to the upper limit of the DRAM temperature range. The retention time grows quickly as the temperature begins to drop and increases more gradually below 270K.

Table 1. DRAM Errors/Capacity at Different Temperatures

| Time (s) | 360K  | 297K  | 77K   |
|---------|-------|-------|-------|
| 5497.62 | 1.41E-02 | 0.00E+00 |
| 2748.78 | 7.41E-03  | 0.00E+00 |
| 1374.42 | 3.07E-03  | 0.00E+00 |
| 687.18  | 9.37E-04  | 0.00E+00 |
| 343.62  | 2.17E-04  | 0.00E+00 |
| 171.78  | 4.63E-05  | 0.00E+00 |
| 85.92   | 7.91E-06  | 0.00E+00 |
| 42.96   | 1.09E-06  | 0.00E+00 |
| 19.98   | 1.09E-07  | 0.00E+00 |
| 10.02   | 6.52E-09  | 0.00E+00 |
| 4.98    | 1.08E-06  | 0.00E+00 |
| 1.98    | 7.09E-06  | 0.00E+00 |

Table 1 shows the evolution of the errors with the temperature for sample S6. This experiment is a simple pause retention test, where the memory is written with a fixed pattern, the refresh is disabled, and the memory is read after the specified time has passed. The device used had a 4 Gb capacity. This sample showed no retention fails at 77K even for 90 minutes pause time. This means that retention will be limited not by leakage, but by disturb effects like row hammer, and the contribution of retention to power consumption will be negligible. More of our retention tests are described in Wang et al. [15].

4.4. Effect of Temperature on DRAM Supply Voltage
To understand the behavior of DRAMs when reducing operating voltage, we devised an experiment where we vary a starting operating voltage, at which the device is trained, and gradually lower the voltage during the test. We select an “all-1s” pattern and use two different sequences (1WR-1RD and 1WR-3 RD) to determine if the errors are more prone in the writing or the reading direction. We repeat the experiment at different voltages.

Figure 6 shows the results for sample S6, a DDR3L device with nominal operating voltage 1.35V. The lower the voltage we used to train, the lower we could go without a significant number of...
errors. This is expected, as the memory trains closer to the area of work. The voltage can be lowered slightly more at colder temperatures — around 5% at 77K. As expected, unmodified DRAMs do not allow significant lowering of the operating voltage.

4.5. FPGAs at Low Temperatures
All tested FPGA devices function properly at 77K when reading and writing the registers in the programmable region of the FPGA, but some failed when accessing some of the registers within the SerDes. Devices that failed during the register access while at 77K became operational again when warmed to 90K. The SerDes contains a TX section, an RX section, and registers for control and status. We measure the rise, fall, and slew rates of the TX output with voltage swing settings of 253mV, 499mV, 1002mV, and 1074mV while operating at 2.5, 3.5, and 5Gbps. We also evaluate our ability to change the phase of the TX signal and equalization of the signal.

To test the SerDes receiver, a PRBS (7,15,23,31) pattern is generated externally and checked inside the receiver for errors. The SerDes RX contains logic which we use to facilitate bit error rate (BER) testing and 2-D statistical eye plotting so that we could quantify the quality of the receiver at 77K. We conclude that the programmable region of the FPGA performs well at 77K but that the SerDes receiver does not do as well. For instance, we obtained two 2-D statistical BER heat maps, at 300 and 89K, of the SerDes eye using a PRBS-15 pattern and a 499mV TX output swing which was looped back to the RX input. The change in the eye plots shown in Figure 7 illustrates that the SerDes behaves differently near 77K. Though the SerDes transmitter appeared to be less affected by lower temperatures, in fact the TX signal showed a decrement in amplitude that could influence the receiver when in loopback. Of course, the eye distortion shown in Figure 7 would be less important when the source of the signal is external to the system.

We test the fabric and I/O’s of the FPGA using low speed interfaces (JTAG, SPI) and a memory controller with external DDR2 memory. The memory device is located close to the FPGA I/O’s to minimize environmental and PCB factors. The results were satisfactory: some devices showed a few errors, but they do not differ significantly from when the FPGA is kept at warmer temperatures and the memory is kept at 77K. We exercised the parallel I/O’s of the devices on five different boards interfacing directly to DDR2 memories running at 600Mbps, 800Mbps, and 1,000Mbps. Experiments used the same pattern generator and memory controller as in the regular memory tests, and we again repeated these tests at 300K, 233K, and 77K. Two of the five boards failed the tests at the two higher bitrates on a repeating data pattern of 0xAA. This pattern also causes the most errors in the regular memory tests. Contrary to our expectations, the FPGAs exhibited no problems with cold start (when the system is powered up directly at 77K) where we obtained the same results as when they were kept on throughout the dipping process.

5. Discussion
Although the DRAMs we studied were designed to operate at much higher temperatures, many of the devices worked correctly at 77K. Of the ones that operated incorrectly in some of our tests, we mainly observed two types of failures: start-up fails and single-bit fails.

Random single cell fails can be caused by an incomplete write or by a fail during a read. Cold temperature affects both write and read operations due to the need for a higher threshold voltage. Basic circuit behavior of the cell and sense-amplifier make it much more difficult to write a ‘1’ and slightly
more difficult to read a ‘0’. Writing is the more critical operation. In the case of a write, the overdrive of the word line voltage at the cell transistor is lower at cryogenic temperatures, which hinders writing a ‘1’. In the case of a read, the higher threshold voltage of the sense-amplifier transistors delays the start of sensing. Since sensing a ‘0’ means sensing a lower voltage than sensing a ‘1’, ‘0’ is worse. Such random single-cell failures occur in different numbers in the tested devices, from fewer than 10 to about 100,000 per test. Since the devices have Gb capacities, the number were in all cases a small fraction of the total number of cells. Initial results showed that most pattern errors are due to single-bit writes. When we performed multiple writes to the same cell, the number of failures were reduced or eliminated. These failures only appear when the pattern generator operates in address-first mode, i.e., when it runs through the entire address range with one command and then updates the commands and data. By switching to a new address not on the same row, the memory controller on the FPGA causes the DRAM to write the contents of the sense-amps back to the array and to close the page. Using command-first mode, which performs write/read sequences on the same cell without closing the page, results in a very low or zero failure count, indicating that writing to and reading from the sense amps is not an issue. The number of errors depends slightly on the frequency and voltage but varies less than 5%, indicating that the issue does not seem to be an external tWR related issue, but it could be related to internal voltage levels or resistance.

Our setup gives us no control over internal device timing or voltage, and thus we cannot perform the two simplest tests to check whether a fail is caused by an incomplete write: changing the internal timing between doing the write and closing the word line or changing the word line voltage during the write. Instead, we either do only one write and then close the word line or we do multiple writes to the same cells before closing the word line. All our fails tested this way indicate that they were write fails – they show up when writing ‘1’, and their number can be reduced by doing multiple writes before closing the word line. One device had a spurious fail that showed up on a ‘0’, so we suspect this is due to a weak sense-amplifier.

One of our memory devices failed the cold-start tests. Given that others have observed problems with the bandgap reference in the device’s internal power system [5], we suspect this to be the cause. DRAM bandgap references include a bipolar device assembled using available well and junction structures. The doping level of the wells are low enough not to be ionized or to be only partially ionized at cryogenic temperatures [6, 7]. The bandgap reference may operate correctly when it is started at room temperature and current is flowing to supply the carriers while the temperature is lowered, but it likely does not start at low temperatures because not enough carriers are present in the powered-off state to kick off the current.

6. Conclusions and Future Work
Design choices can be made to make electronic components that work at both ambient and cryogenic temperatures. By serendipity, some currently available parts, like DRAM memories, PCBs, passive components, transistors, diodes, common logic, and FPGAs already work at both temperatures. When parts do fail, failure characteristics result from design decisions made for these devices.

We find that a DRAM device can be designed to work at both room temperature and 77K without additional cost if appropriate design-time decisions are made. Some single-cell fails are only visible at cryogenic temperatures, and these cells need to be replaced with redundancy. Post-package repair is an effective way to handle such fails with the least disruption to a normal manufacturing and test flow. Current commercial DRAMs consume similar power at both room and cryogenic temperatures, but refresh is needed much less often at 77K. Optimizing a DRAM for lowest power at 77K will require larger modifications and process changes to allow the operating voltage to be significantly lowered by using the steeper subthreshold slope at 77K. Lowering of threshold and operating voltage was not needed to show experimentally the feasibility of a DRAM-based memory system at 77K, but the power consumption of unmodified DRAM is too high for energy-efficient volume deployment.
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