Self-aligned graphene field-effect transistors with polyethyleneimine doped source/drain access regions

Hema C. P. Movva,1, Michael E. Ramón,1 Chris M. Corbet,1 Sushant Sonde,1 Sk. Fahad Chowdhury,1 Gary Carpenter,2 Emanuel Tutuc,1 and Sanjay K. Banerjee1
1) Microelectronics Research Center, The University of Texas at Austin, Austin, TX 78758
2) IBM Research, Austin, TX 78758

(Dated: 3 May 2014)

We report a method of fabricating self-aligned, top-gated graphene field-effect transistors (GFETs) employing polyethyleneimine spin-on-doped source/drain access regions, resulting in a 2X reduction of access resistance and a 2.5X improvement in device electrical characteristics, over undoped devices. The GFETs on Si/SiO2 substrates have high carrier mobilities of up to 6,300 cm2/Vs. Self-aligned spin-on-doping is applicable to GFETs on arbitrary substrates, as demonstrated by a 3X enhancement in performance for GFETs on insulating quartz substrates, which are better suited for radio frequency applications.

PACS numbers: 85.30.Tv, 72.80.Le

Graphene’s exceptional electronic properties, in particular its high carrier mobility,1 high saturation velocity,2 and large current density,2 make it an excellent channel material for future ultra-high-speed electronic devices. Graphene field-effect transistors (GFETs) have recently attracted significant attention for potential radio frequency (RF) applications,4 with reports of RF GFETs operating at intrinsic cut-off frequencies up to 300 GHz.5 However, theoretical calculations predict GFETs to be capable of running at THz operating frequencies.6 One of the major factors preventing optimal THz RF performance of GFETs is high series resistance of the access regions between the source/drain electrodes and the top-gated graphene channel. This parasitic access resistance reduces device drive currents (I_D) and transconductances (g_m), thereby directly affecting GFET performance. Electrostatic modulation of the access regions is one way of reducing this resistance for devices on heavily doped substrates.7 This approach requires a global, conducting back-gate and does not provide for independent control of multiple devices on the same substrate, and is unsuitable for GFETs on insulating substrates. This problem can be addressed by fabricating GFETs with self-aligned gates, where the access region dimensions and consequently their resistances are reduced. Previous methods of self-aligned GFET fabrication are not straightforward, and either use physically assembled nanowire gates,8 or require pristine quality graphene and ultra high vacuum metal-deposition,9 or restrict scaling of the top-gate dielectric.10 In this work, we present a simple and scalable approach of fabricating self-aligned GFETs, exploiting the unique property of charge-transfer doping of graphene using polyethyleneimine (PEI).

The problem of high access resistance in conventional Si complementary metal-oxide-semiconductor (CMOS) transistors is overcome by heavily doping the source/drain access regions through ion implantation.11 We employed a similar approach in this work, by using charge-transfer doping of graphene with PEI, to dope the access regions and reduce their resistance. We chose PEI due to its ease of application, but any other method of doping (substitutional, surface-transfer, etc.) can, in principle, be used for the same result. We fabricated top-gated GFETs with exposed source/drain access regions and doped them with PEI in a self-aligned manner using a controllable method of spin-on-doping. The fabrication process is universally applicable to GFETs on arbitrary substrates and is specifically demonstrated for GFETs on Si/SiO2 and quartz substrates.

PEI spin-on-doping of graphene was characterized on back-gated GFETs. Monolayer graphene was exfoliated onto highly-doped n-type Si substrates with a 285 nm thermally grown SiO2 layer acting as the back-gate dielectric. Graphene active regions were patterned by e-beam lithography (EBL) and oxygen plasma etching. A second EBL step was performed to define metal contacts for 4-point probe structures, followed by e-beam evaporation of a 50 nm Ni layer as contact metal and a final lift-off. The branched PEI (Sigma Aldrich, M_n ~ 60,000, M_w ~ 750,000) molecular dopants were applied by spin-coating a dilute solution of PEI in methanol onto the substrate. A solution of 0.02% (by wt.) PEI in methanol was

---

(a) Schematic of a PEI spin-on-doped back-gated GFET on Si/SiO2 and (b) optical micrograph of a representative spin-on-doped GFET (scale bar is 10 µm)

---

a) Electronic mail: hemacp@utexas.edu
prepared by magnetic stirring in a dark, air-tight container for a period of 48 hours. Methanol was used as a solvent due to its high volatility which minimizes solvent residue on the graphene surface. To dope the graphene, this dopant solution was spin-coated onto the GFETs at 1500 rpm for 60 s, followed by a quick bake at 90°C for 20 s to drive away any remaining methanol residue. PEI, being a heavy macromolecule does not evaporate, but forms a thin adsorbed layer on the graphene, thereby doping it. Figure 1(a) shows the schematic and Fig. 1(b) the optical micrograph of a back-gated GFET after spin-on-doping. PEI-doped graphene has a thin, uniform layer of dopants adsorbed on it and cannot be optically distinguished from clean, undoped graphene.

Figure 2 (a) compares the Raman spectra of graphene before and after doping with PEI. There is a reduction in $I_{2D}/I_G$ from 2.5 to 1.5 and an upshift of the G and 2D peaks after doping. PEI characteristic peaks appear at $\sim 1500$ cm$^{-1}$. (b) 4-point resistivity measurements of the GFET after repetitive spin-on-doping steps. There is a reduction in the extracted carrier mobility with successive spin-on-doping steps (inset).

Control of the doping dose was achieved by repetitive spin-on-doping steps. Figure 2(b) shows 4-point resistivity measurements of the back-gated GFET after successive PEI spin-on-doping steps. The undoped GFET shows a Dirac point ($V_{\text{DIRAC}}$) at $+3$ V, likely due to unintentional doping by water vapor during the fabrication process. $V_{\text{DIRAC}}$ shifts to $-5$ V after the first spin-on-doping step, signifying n-type doping due to PEI. Successive spin-on-doping steps increasingly dope the graphene n-type, as evident from shifts in $V_{\text{DIRAC}}$ to larger negative voltages after every spin. Carrier mobilities were extracted using a well-established field-effect mobility model and plotted along with $V_{\text{DIRAC}}$ after every spin-on-doping step in Fig. 2(b) (inset). There is a reduction in carrier mobility with each spin-on-doping step, in accordance with previous reports of dopant induced mobility degradation. However, the mobility after four spin-on-doping steps still remains high at $\sim 6,000$ cm$^2$/Vs. An important effect of doping is reduction in the graphene resistivity at $V_{BG} = 0$ V from 4.5 kΩ/□ to 1.5 kΩ/□, a factor of 3X. This reduction in resistivity when employed to the source/drain access regions of a top-gated GFET can result in improved GFET performance.

To test this hypothesis, dual-gated GFETs were fabricated on clean, back-gated GFETs by patterning a top-gate stack. A 20 nm ALD Al$_2$O$_3$ layer, seeded by a 15 Å evaporated Al layer, was deposited as the top-gate dielectric. This was followed by a final EBL step to pattern the top-gate electrode. A 50 nm Ni layer was subsequently deposited as the top-gate metal contact. The source/drain access regions of the GFET at this stage were covered by the ALD Al$_2$O$_3$ layer, which was etched away in order to dope them. This etch was performed in a self-aligned manner using a 1:50 dilute HF solution as the etchant. The top-gate metal acts as a self-aligned hard mask during the etch and protects the top-gate dielectric. It has to be noted that the HF solution etches the underlying SiO$_2$ layer too, albeit at a much slower rate ($5$ nm/min.) than the ALD Al$_2$O$_3$ top-gate dielectric ($60$ nm/min.). The etch could thus be conveniently timed to minimize etching of the SiO$_2$ layer. The access regions were then finally spin-on-doped using PEI. Figures 3(a)-(c) illustrate the fabrication of self-aligned spin-on-doped GFETs and Fig. 3(d) shows an optical micrograph of the finished top-gated GFET.
region. The n-type doping of the top-gated graphene is unintentional, and is probably due to impurities in the ALD Al₂O₃ layer. The position of the secondary V_{DIRAC} can be selectively modulated using the top-gate bias. A negative V_{TG} (= -0.5 V) depletes electrons from the top-gated graphene region and shifts the secondary V_{DIRAC} close to 0 V, which, in turn, overlaps with the primary V_{DIRAC} to result in one “apparent” V_{DIRAC} for the entire graphene. A positive V_{TG} (= +0.5 V), on the other hand, induces excess electrons in the top-gated graphene region and shifts its V_{DIRAC} to a more negative voltage, beyond -30 V in this case, as evident from the downturn of the resistance profile along the V_{TG} voltage. This is evident as an apparent downward shift contour plot of the device as a function of V_{TG} and V_{BG}, show selective modulation of the top-gated graphene region, independent of the access regions. (f) and (g) show the resistance contour plots for a GFET before self-aligned etching and after spin-on-doping respectively. The slope of the contours of charge neutrality (dashed lines) gives C_{TG}/C_{BG} = 21.

Selective spin-on-doping of the GFETs was done only in the exposed source/drain regions using 0.02% PEI, while the top-gated graphene region was protected by the top-gate stack. Figures 3(f) and (g) show the resistance contour plot of the device as a function of V_{TG} and V_{BG} before the self-aligned etch and after self-aligned doping. The only effect of self-aligned doping is to dope the access regions n-type and shift their V_{DIRAC} to a negative voltage. This is evident as an apparent downward shift of the resistance profile along the V_{BG} axis after doping. The resistance profile along the V_{TG} axis remains the same before and after doping, signifying that there is no effect of doping on the top-gated graphene region. The dashed lines represent contours of charge neutrality for the top-gated channel and their slope gives the ratio of the top-gate capacitance to the back-gate capacitance, C_{TG}/C_{BG} = 21. Using the back-gate capacitance value of C_{BG} = 11 nF/cm², the top-gate capacitance is estimated to be C_{TG} ~ 236 nF/cm². This corresponds to a relative dielectric constant of 5.7 for the Al₂O₃ film, which agrees with reports from literature for ALD Al₂O₃ films on graphene. The slope remains unchanged after the self-aligned etch and doping, thereby indicating no degradation of dielectric properties.

The properties of a GFET with a top-gated channel length, L_{G} = 1.0 µm, channel width, W_{G} = 7.0 µm and access region length, L_{A} = 1.5 µm, before and after two self-aligned doping steps with 0.02% PEI are shown in Fig. 3. The transfer characteristics show an improvement in the maximum drive current (I_{D,max}) from 7.4 µA to 16.6 µA and in the peak transconductance (g_{m,x}) from 4.2 µS to 10.3 µS after two spins, an approximately 2.5X improvement. The I_{ON}/I_{OFF} ratio also improves by 20% after two spins. To extract the reduction in access resistance, the resistance profiles of the GFET (R_{SD}) are fit to the expression,

\[ R_{SD} = R_S + \frac{L_G}{eW_GF_EV/n_0^2 + n^2} \]  

where e is the electron charge, n is the field-modulated carrier concentration, n_0 is the residual carrier concentration at the neutrality point, and \mu_{FE} is the field-effect mobility of the top-gated graphene region. \(R_S\) is the
total series resistance contribution from the source/drain contacts, \( R_C \) and access regions, \( R_A \): \( R_{S} = R_{C} + R_{A} \). The undoped device shows a \( \mu_{FE} \approx 6,800 \, \text{cm}^2/\text{Vs} \), which reduces to \( \approx 6,300 \, \text{cm}^2/\text{Vs} \) after doping. \( R_S \) reduces from 2.6 kΩ to 1.5 kΩ after one spin, and further down to 1.1 kΩ after two spins. This reduction in \( R_S \) is primarily from reduction of \( R_A \). It has to be noted that, in addition to improving the device characteristics, self-aligned spin-on-doping can be used as a knob to tune the \( I_D \) of a GFET post-fabrication, by varying the doping dose. This method of tuning \( I_D \) can be particularly useful to compensate for device-to-device variability in graphene integrated circuits.

The full advantage of self-aligned spin-on-doping is realized on GFETs on insulating substrates, where the absence of a back-gate makes it impossible to electrostatically modulate the access region resistance\(^{11}\). Insulating substrates are also better suited for RF applications due to their lower parasitic capacitances. We specifically chose single crystal quartz substrates, since they are ideal for low loss, temperature stable high-frequency electronics\(^{22}\). To fabricate GFETs on quartz, monolayer graphene was first exfoliated on Si/SiO\(_2\) substrates and transferred onto quartz using a poly(methyl methacrylate) based transfer method\(^{22}\). Subsequent processing was similar to the processing used for fabricating top-gated GFETs on Si/SiO\(_2\) substrates.

Transfer characteristics of a top-gated GFET on quartz, before and after self-aligned doping using 0.02\% PEI are shown in Fig. 4. The device dimensions are: \( L_{G} = 2.0 \, \mu\text{m}, \, W_{G} = 7.0 \, \mu\text{m} \) and \( L_A = 1.8 \, \mu\text{m} \). The gains in device performance are similar to the GFET on Si/SiO\(_2\). \( I_{D,\text{max}} \) improves from 6.8 \( \mu\text{A} \) to 15.3 \( \mu\text{A} \) and \( g_{m,\text{max}} \) from 4.3 \( \mu\text{S} \) to 13.1 \( \mu\text{S} \). A \( \sim 3 \times \) improvement.

A carrier mobility of 5,600 \( \text{cm}^2/\text{Vs} \) is extracted for the undoped device, which reduces slightly to 5,200 \( \text{cm}^2/\text{Vs} \) after doping. These values are comparable to the GFET on Si/SiO\(_2\) and indicate that quartz can be an attractive insulating substrate for graphene electronics.

In summary, we have demonstrated a simple and controllable method of spin-on-doping graphene using PEI as a chemical dopant. Control of the doping dose was achieved by repetitive spin-on-doping steps. We fabricated dual-gated GFETs on Si/SiO\(_2\) substrates and spin-on-doped their access regions in a self-aligned manner to reduce their resistance and improve device performance by up to 2.5X. Further, we fabricated GFETs on insulating quartz substrates and spin-on-doped their access regions, which enhanced their device characteristics by up to 3X. These results indicate that chemical doping of the source/drain access regions can be a viable method of improving GFET performance on arbitrary substrates.

This work was supported by NRI-SWAN and the NSF NASCENT center. We thank D. Ferrer for help with TEM imaging.

1. A. K. Geim and K. S. Novoselov, Nat. Mater. 6, 183 (2007).
2. A. H. C. Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, Rev. Mod. Phys. 81, 109 (2009).
3. A. Barreiro, M. Lazzeri, J. Moser, F. Mauri, and A. Bachtold, Phys. Rev. Lett. 103, 076601 (2009).
4. S. O. Koswatta, A. V. Garcia, M. B. Steiner, Y. M. Lin, and P. Avouris, IEEE Trans. Microwave Theory Tech. 59, 2739 (2011).
5. L. Liao, Y. C. Lin, M. Bao, R. Cheng, J. Bai, Y. Liu, Y. Qu, K. L. Wang, Y. Huang, and X. Duan, Nature 467, 305 (2010).
6L. Liao, J. Bai, R. Cheng, Y. C. Lin, S. Jiang, Y. Qu, Y. Huang, and X. Duan, Nano Lett. 10, 3952 (2010).
7Y. M. Lin, H. Y. Chi, K. A. Jenkins, D. B. Farmer, P. Avouris, and A. V. Garcia, IEEE Electron Dev. Lett. 31, 68 (2010).
8D. B. Farmer, Y. M. Lin, and P. Avouris, Appl. Phys. Lett. 97, 013103 (2010).
9A. Badmaev, Y. Che, Z. Li, C. Wang, and C. Zhou, ACS Nano 6, 3371 (2012).
10R. W. Bower and R. G. Dill, IEDM 12, 102 (1966).
11D. B. Farmer and R. G. Mojarad and V. Perebeinos and Y. M. Lin and G. S. Tulevski and J. C. Tsang and P. Avouris, Nano Lett. 9, 388 (2009).
12H. Liu, Y. Liu, and D. Zhu, J. Mater. Chem. 21, 3335 (2011).
13A. Gupta, G. Chen, P. Joshi, S. Tadigadapa, and P. C. Eklund, Nano Lett. 6, 2667 (2006).
14E. Muoz, D.-S. Sub, S. Collins, M. Selvidge, A. Dalton, B. Kim, J. Razal, G. Ussery, A. Rinzler, M. Martinez, and R. Baughman, Adv. Mater. 17, 1064 (2005).
15C. Casiraghi, S. Pisana, K. S. Novoselov, A. K. Geim, and A. C. Ferrari, Appl. Phys. Lett. 91, 233108 (2007).
16A. Das, S. Pisana, B. Chakraborty, S. Piscanec, S. K. Saha, U. V. Waghmare, K. S. Novoselov, H. R. Krishnamurthy, A. K. Geim, A. C. Ferrari, and A. K. Sood, Nat. Nano. 3, 210 (2008).
17D. B. Farner, Y. M. Lin, A. A. Ardakani, and P. Avouris, Appl. Phys. Lett. 94, 213106 (2009).
18K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, Science 306, 666 (2004).
19S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, and S. K. Banerjee, Appl. Phys. Lett., 062107 (2009).
20B. Fallahazad, K. Lee, G. Lian, S. Kim, C. M. Corbet, D. A. Ferrer, L. Colombo, and E. Tutuc, Appl. Phys. Lett. 100, 093112 (2012).
21D. Berdebes, T. Low, Y. Sui, J. Appenzeller, and M. S. Lundstrom, IEEE Trans. Electron Devices 58, 3925 (2011).
22M. E. Ramon, K. N. Parrish, S. F. Chowdhury, C. W. Magnuson, H. C. P. Movva, R. S. Ruoff, S. K. Banerjee, and D. Akinwande, IEEE Trans. Nanotech. 11, 877 (2012).
23S. Kim, I. Jo, J. Nah, Z. Yao, S. K. Banerjee, and E. Tutuc, Phys. Rev. B 83, 161401 (2011).