Electronic Design Automation tools for superconducting circuits

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Abstract. Superconducting integrated circuits have long been completely handcrafted or at best designed with a loose collection of tools that require manual manipulation of data and design transfer between tools. Electronic Design Automation (EDA) software development requires significant investment of resources to track the evolution of integrated circuit fabrication processes, which has only been possible commercially for highly successful semiconductor integrated circuit processes. The IARPA SuperTools project which started in 2017 is the largest known investment to date made in superconducting EDA tool development. SuperTools is divided into two main categories: high-level tools for the synthesis of digital logic circuits, clock networks and placed-and-routed layouts for systems such as processors with millions of logic gates; and physical-level tools for the design, simulation, optimisation, verification, layout and parameter extraction of devices and digital logic cells with the inclusion of fabrication process simulation. In this paper the modules developed for the ColdFlux project under SuperTools are discussed from device modelling to chip tape-out. Progress on parameter extraction tools is highlighted.

1. Introduction
Superconducting electronics design automation (S-EDA) tool development has received limited attention for decades, primarily because of lack of funding. Consequently, early S-EDA tools were all loose-standing freeware utilities developed at universities and research laboratories, with very little maintenance or continued development (for a detailed history, see [1, 2]).

Early tools focused on:

- electrical circuit simulation with simulators derived from SPICE engines [3], such as JSIM [4] and WRSpice [5] (the latter as part of XIC Tools) and phase-based circuit simulation engines such as COMPASS [6] and its successor PSCAN [7, 8];
- margin and yield analysis and optimisation tools [8, 9, 10, 11];
- inductance calculation with tools such as Lmeter [12] and FastHenry [13];
- hardware description language logic simulation with Verilog [14] and VHDL [15]; and
- logic synthesis, placement and routing (including clock synthesis [16]), with only one practical tool demonstrated [17].

There is a sizeable collection of S-EDA modules available today, but this paper will only address the ColdFlux [18] tool suite, which aims to provide complete S-EDA capability from
device characterization and circuit creation all the way to tape-out. Under the ColdFlux project of the IARPA SuperTools programme, our group develops:

- Katana for TCAD modelling interface and device characterisation [19];
- JoSIM for electrical circuit simulation both in voltage and phase mode [20];
- JJ model extraction software for converting measured Josephson junction data to models;
- JoSIM Tools for margin and yield analysis and optimisation [21];
- tools for thermal analysis of structures in layouts [22];
- InductEx (including the TetraHenry engine for numerical solution of field equations [23]) for parameter extraction of cell and chip layouts [24, 25];
- SPIRA for parameterised circuit layout synthesis and layout-vs-schematic verification;
- ViPeR for logic and clock synthesis, placement and routing;
- TimEx for timing extraction and JoSIM to Verilog model translation [26]; and
- GDS processing tools for passive transmission line synthesis and chip filling.

Other partners under ColdFlux develop tools that complete the suite:

- JOINUS user interface [27] to stitch all the ColdFlux tools together;
- FLOOXS TCAD tools [18] to model processes;
- qPALACE suite that includes RSFQ logic synthesis, technology mapping [28], placement [29], clock synthesis [30] and routing [31] tools; and
- logic [32] and clock synthesis [33], placement and routing tools for AQFP circuits [34].

2. The design process with ColdFlux S-EDA tools

2.1. Physical tools

A new design is started at the device level with the extraction of a compact SPICE model for the Josephson junction for electrical circuit simulation. The Technology Computer-Aided Design (TCAD) process flow and tools for this task are shown in Figure 1.

If no measured I-V data are available, we start at process modelling. FLOOXS [18] is used to calculate material growth or removal during fabrication steps with level-set methods. The fabrication steps can be defined manually, or automated from a slice through a layout file processed with Katana [19]. If measured I-V data for Josephson junctions are available, the junction model is extracted with a model parameter fitting tool.
The design flow for physical level cell design is shown in Figure 2. A cell is designed in the Xic schematic editor and simulated electrically with JoSIM [20] or WRSpice by using extracted Josephson junction models. JoSIM Tools [21] is used to analyse margins and yield and optimise the region of operation. Layout can be done with Xic, or scripted as a parameterised cell for SPIRA. Layout-versus-schematic verification is handled by SPIRA, which also generates a Design Rule Check (DRC) verified GDS2 layout. The layout can be converted to an InductEx IXI file with Gds2IXI to allow parameterisation and package modelling. InductEx does parameter extraction from the layout, after which the back-annotated simulation file can be resimulated at the electrical level. InductEx can also extract compact models of the layout in the presence of physical phenomena such as external magnetic field and trapped flux. From the netlist file, TimEx and AQFPTX extract the Verilog HDL models of RSFQ and AQFP cells respectively to include timing parameters. All cell files are then added to the cell library.

2.2. Front-end tools

At the front-end, a behavioural design is processed with tools that perform logic synthesis with the cells available in the cell library. A technology conversion tool adds pulse splitters (for RSFQ circuits) and path or level-balancing delay elements. A placement tool places cells in a row-based configuration. This is followed by clock synthesis and placement, after which all interconnects are routed. The post placed-and-routed result is verified by converting it back to electrical or HDL simulation decks and running simulations with test patterns in JoSIM and iVerilog. Separately, static timing analysis is performed. Afterwards, passive transmission line layouts are synthesized along the trajectories of the routed interconnects, DRC-required fill structures are populated, and the resulting chip layout is analysed with InductEx in a packaging and shielding environment before tape-out.
2.3. Limitations

Despite recent advances, there are still limitations to the designs that can be done with current tool suites. Clocking in DC-biased SFQ circuits remains difficult and research is ongoing [35]. Synthesis of sequential logic circuits is still very difficult for RSFQ.

3. InductEx: parameter extraction tool progress

Progress in S-EDA tool capabilities requires continuous development and maintenance. After Xic [5], the physical parameter extraction module InductEx is the S-EDA tool with the longest sustained development and maintenance period. This section discusses the growth in capabilities of InductEx over 15 years from inductance extraction for single inductors through full logic gate layouts to entire chip-on-carrier systems as a demonstration of how S-EDA matured.

3.1. Early superconductor inductance estimators

For early superconductor circuits and analogue devices, analytical [36] and empirical [37] methods were used. These methods quickly became ineffective for complex digital circuits, and numerical methods such as MFB [38] were introduced. The most successful numerical inductance calculator for almost two decades was the quasi-2D tool Lmeter [12] that supports gate-level multi-terminal inductance extraction, but does not handle holes.

3D-MLSI [39] was developed to handle 2D sheet currents in triangular segments, with 3D magnetic field calculation and mostly found application in SQUID design or analysis.

FastHenry [40], developed mostly for printed circuit board structures, was adapted for superconductivity. FastHenry cannot process a multi-terminal inductance structure such as a superconductor logic circuit, so that was initially used to generate inductance tables for different inductive structures that could be combined to find total inductance [13]. This method was not practical, because return current and mutual inductance were effectively not modelled.

3.2. InductEx

InductEx was initially developed in 2004 to find the self and mutual inductance of isolated inductors with complicated three-dimensional (3D) layouts [41]. It created 3D models from layout information, and used FastHenry as the numerical engine. Layouts were limited to flattened GDS files with Manhattan-type structures only, and the models had a practical limit
of about 10,000 segments. Solution time at that stage was 10 - 30 minutes on a personal computer (PC).

In 2007 _InductEx_ was expanded to handle multi-terminal networks. Circuit netlists were read in from a file, and inductance was calculated from port to port after which linear equation solving was employed to find individual branch inductance. This method did not support mutual inductance, and it was slow (around 10 - 30 hours to extract a typical RSFQ cell).

Improved meshing and a port current calculation method were added in 2010, which allowed mutual inductance to be solved too, and brought calculation time down to between 1 and 2 hours.

Improvements since 2011 were aimed at usability by design engineers: a full GDS hierarchy read-in of fabrication ready cells; verification of calculation results against experimental measurements for structures [24]; support for resistive-inductive branches and a 1,000 times improvement in calculation speed through re-engineering of the meshing strategy and the field solver’s preconditioners, LU decomposition methods and the use of parallel threads.

The TetraHenry engine was added in 2015, which allows better non-uniform meshing. Other developments include support for magnetoresistive materials, magnetic field calculation, capacitance calculation, characteristic impedance calculation, external magnetic field excitation (uniform and gradient fields), analysis of flux in superconducting holes and the extraction of compact simulation models for circuits in the presence of external fields and trapped flux. Recently, the interface to _InductEx_ was improved to allow modelling beyond the integrated circuit, so that a chip can be analysed together with packaging and shielding. The practical limit for a model size is now above 10 million segments. Progress is illustrated in Figure 4.

4. Conclusion
Parameter extraction S-EDA tool capability increased dramatically over the last 15 years, with most progress over the last 5 years stimulated by commercialisation and user uptake, as well as research and development funding by IARPA. Similar capability improvements are expected for other physical and system level S-EDA tools currently funded by the IARPA SuperTools project, provided that the modules are accessible to circuit design engineers.

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**Figure 4.** _InductEx_ and its numerical engines – progress over 15 years.
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