Symmetrical polarization splitter/rotator design and application in a polarization insensitive WDM receiver

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Abstract: In integrated photonics, the design goal of a polarization splitter/rotator (PSR) has been separating the TE0 and TM0 modes in a waveguide. This is a natural choice. But in theory, a PSR only needs to project the incoming State Of Polarization (SOP) orthogonally to its output ports, using any orthogonal mode basis set in the fiber. In this article, we introduce a novel PSR design that alternatively takes the linear combination of TE0 and TM0 (TE0 +/- TM0) as orthogonal bases. By contrast, existing approaches exclusively use TE0 and TM0 as their basis set. The design is based on two symmetric and robust structures: a bi-layer taper and a Y-junction, and involves no bends. To prove the concept, we incorporated it into a four-channel polarization insensitive wavelength division multiplexing (PI-WDM) receiver fabricated in a standard CMOS Si photonics process. 40 Gb/s data rate and 0.7 +/- 0.2 dB polarization dependent loss (PDL) is demonstrated on each channel. Lastly, we propose an improved PSR design with 12 μm device length, < 0.1 dB PDL, < 0.4 dB insertion loss and < 0.05 dB wavelength dependence across C-band for both polarizations. Overall, our PSR design concept is simple, easy to realize and presents a new perspective for future PSR designs.

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References and links

1. R. Soref, “The past, present, and future of silicon photonics,” IEEE J. Sel. Top. Quantum Electron. 12(6), 1678–1687 (2006).
2. T. Baehr-Jones, T. Pinguet, P. Lo Guo-Qiang, S. Danziger, D. Prather, and M. Hochberg, “Myths and rumours of silicon photonics,” Nat. Photonics 6(4), 206–208 (2012).
3. S. Assefa, S. Shank, W. Green, M. Khater, E. Kiewra, C. Reinholm, S. Kamlapurkar, A. Rylyakov, C. Schow, F. Horst, H. Pan, T. Topuria, P. Rice, D. M. Gill, J. Rosenberg, T. Barwicz, M. Yang, J. Proesel, J. Hofrichter, B. Offrein, X. Gu, W. Haensch, J. Ellis-Monaghan, and Y. Vlasov, “A 90nm CMOS integrated nano-photonics technology for 25Gbps WDM optical communications applications,” in IEEE International Electron Device Meeting (2012), pp. 33–8.
4. D. Knoll, S. Lischke, L. Zimmermann, B. Heinemann, D. Micsik, P. Ostrovskyy, G. Winzer, M. Kroh, R. Barth, T. Grabolla, K. Schulz, M. Fraschke, M. Lisker, J. Drews, A. Trusch, S. Krüger, S. Marschmeyer, H. H. Richter, O. Fursenko, Y. Yamamoto, B. Wohlfelk, K. Petermann, A. Beling, Q. Zhou, and B. Tillack, “Monolithically integrated 25Gbit / sec receiver for 1.55μm in photonic BiCMOS technology,” in Optical Fiber Communications (2014), p. Th4C.4.
5. L. Chrostowski and M. Hochberg, Silicon Photonics Design (Cambridge University Press, 2015).
6. E. C. M. Pennings, R. J. Deri, R. Bhat, T. R. Hayes, and N. C. Andreadakis, “Ultracompact, all-passive optical 90 degrees -hybrid on InP using self-imaging,” IEEE Photon. Technol. Lett. 5(701), 5–7 (1993).
7. C. Z. Zhang, Y.-J. Chiu, P. Abraham, and J. E. Bowers, “25 GHz polarization-insensitive electroabsorption modulators with traveling-wave electrodes,” IEEE Photon. Technol. Lett. 11(2), 191–193 (1999).
8. A. Sugita, A. Kaneko, K. Okamoto, M. Itoh, A. Himeno, and Y. Ohnori, “Very low insertion loss arrayed-waveguide grating with vertically tapered waveguides,” IEEE Photon. Technol. Lett. 12(9), 1180–1182 (2000).
9. T. Barwicz, M. R. Watts, M. Popović, P. T. Rakich, L. Socci, F. X. Kärntner, E. P. Ippen, and H. I. Smith, “Polarization-transparent microphotonic devices in the strong confinement limit,” Nat. Photonics 1(1), 57–60 (2007).

10. N.-N. Deng, F. Feng, S. Liao, X. Wang, P. Dong, H. Liang, C.-C. Kung, W. Qian, J. Fong, R. Shafahi, Y. Luo, J. Cunningham, A. V. Krishnamoorthy, and M. Asghari, “30GHz Ge electro-absorption modulator integrated with 3 μm silicon-on-insulator waveguide,” Opt. Express 19(8), 7062–7067 (2011).

11. VTT silicon photonics platform through ePIXfab,” http://www.epixfab.eu/technologies/vttsp.

12. A. Novack, Y. Liu, R. Ding, M. Gould, T. Baehr-Jones, Q. Li, Y. Yang, Y. Ma, Y. Zhang, K. Padmaaraj, K. Bergmen, A. E. J. Lim, G. Q. Lo, and M. Hochberg, “A 30 GHz silicon photonic platform,” in IEEE International Conference on Group IV Photonics GFP (2013), pp. 7–8.

13. Imec’s integrated silicon photonics platform (ISIIPP25G),” http://www2.imec.be/en/services-and-solutions/silicon-photonics.html.

14. CEA-Leti silicon photonics platform,” http://www-leti.cea.fr/en/How-to-collaborate/Collaborating-with-Leti/Integrated-silicon-photonics.

15. A. Mekis, S. Gloeckner, G. Masini, A. Narasimha, T. Pinguet, S. Sahni, and P. De Dobbeleare, “A grating-coupler-enabled CMOS photonics platform,” IEEE J. Sel. Top. Quantum Electron. 17(3), 597–608 (2011).

16. D. C. Lee, D. Feng, C.-C. Kung, J. Fong, W. Qian, X. Zheng, J. E. Cunningham, A. V. Krishnamoorthy, and M. Asghari, “Monolithic chip-to-chip WDM optical proximity coupler utilizing Echelle grating multiplexer/demultiplexer integrated with micro mirrors built on SOI platform,” in IEEE Photonics Society Summer Topical Meeting Series (2010), pp. 215–216.

17. M. Cherchi, S. Ylinen, M. Harjanne, M. Kapulainen, and T. Aalto, “Dramatic size reduction of waveguide bends on a micron-scale silicon photonics platform,” Opt. Express 21(15), 17814–17823 (2013).

18. E. Timurdogan, C. M. Sorace-Agaskar, J. Sun, E. Shah Hosseini, A. Bberman, and M. R. Watts, “An ultralow power athermal silicon modulator,” Nat. Commun. 5, 4008 (2014).

19. Y. Liu, R. Ding, Y. Ma, Y. Yang, Z. Xuan, Q. Li, A. E. Lim, G. Q. Lo, K. Bergman, T. Baehr-Jones, and M. Hochberg, “Silicon Mod-MUX-Ring transmitter with 4 channels at 40 Gb/s,” Opt. Express 22(13), 16431–16438 (2014).

20. H. Fukuda, K. Yamada, T. Tsuchiizawa, T. Watanabe, H. Shinojima, and S. Itabashi, “Ultrasmall polarization splitter based on silicon wire waveguides,” Opt. Express 14(25), 12401–12408 (2006).

21. D. Dai and J. E. Bowers, “Novel ultra-short and ultra-broadband polarization beam splitter based on a bent directional coupler,” Opt. Express 19(18), 18614–18620 (2011).

22. Y. Xu, J. Xiao, and X. Sun, “Compact polarization beam splitter for silicon-based slot waveguide using an asymmetrical multimode waveguide,” J. Lightwave Technol. 32, 4282–4284 (2014).

23. L. Chen, C. R. Doerr, and Y. K. Chen, “Compact polarization rotator on silicon for polarization-diversified circuits,” Opt. Lett. 36(4), 469–471 (2011).

24. D. Vermeulen, S. Selvaraja, P. Verheyen, P. Absil, W. Bogaerts, D. Van Thourhout, and G. Roelkens, “Silicon-on-Insulator polarization rotator based on a symmetry breaking silicon overlay,” IEEE Photon. Technol. Lett. 24(6), 482–484 (2012).

25. H. Guan, Y. Ma, R. Shi, A. Novack, J. Tao, Q. Fang, A. E.-J. Lim, G.-Q. Lo, T. Baehr-Jones, and M. Hochberg, “Ultracompact silicon-on-insulator polarization rotator for polarization-diversified circuits,” Opt. Lett. 39(16), 4703–4706 (2014).

26. P. Dong, C. Xie, L. Chen, L. L. Buhl, and Y. K. Chen, “112-Gb/s monolithic PDM-QPSK modulator in silicon,” Opt. Express 20(26), B624–B629 (2012).

27. D. Dai and J. E. Bowers, “Novel concept for ultracompact polarization splitter-rotator based on silicon nanowires,” Opt. Express 19(11), 10940–10949 (2011).

28. W. Yuan, K. Kojima, B. Wang, T. Koike-Akino, K. Parsons, S. Nishikawa, and E. Yagyu, “Mode-evolution-based polarization rotator-splitter design via simple fabrication process,” Opt. Express 20(9), 10163–10169 (2012).

29. Y. Ding, H. Ou, and C. Puicheret, “Wideband polarization splitter and rotator with large fabrication tolerance and simple fabrication process,” Opt. Lett. 38(8), 1227–1229 (2013).

30. W. D. Sacher, T. Barwicz, B. J. F. Taylor, and J. K. S. Poon, “Polarization rotator-splitters in standard active silicon photonics platforms,” Opt. Express 22(4), 3777–3786 (2014).

31. W. D. Sacher, Y. Huang, L. Ding, T. Barwicz, J. C. Mikkelsén, B. J. F. Taylor, G. Q. Lo, and J. K. S. Poon, “Polarization rotator-splitters and controllers in a Si3N4-on-Si integrated photonics platform,” Opt. Express 22(9), 11167–11174 (2014).

32. J. Wang, B. Niu, Z. Sheng, A. Wu, W. Li, X. Wang, S. Zou, M. Qi, and F. Gan, “Novel ultra-broadband polarization splitter-rotator based on mode-evolution tapers and a mode-sorting asymmetric Y-junction,” Optics Express 22(11), 13565–13571 (2014).

33. L. Liu, Y. Ding, K. Vynd, and J. M. Hvam, “Silicon-on-insulator polarization splitting and rotating device for polarization diversity circuits,” Opt. Express 19(13), 12646–12651 (2011).

34. H. Guan, A. Novack, M. Streshinsky, R. Shi, Q. Fang, A. E. Lim, G. Q. Lo, T. Baehr-Jones, and M. Hochberg, “CMOS-compatible highly efficient polarization splitter and rotator based on a double-etched directional coupler,” Opt. Express 22(3), 2489–2496 (2014).

35. J. Wang, B. Niu, Z. Sheng, A. Wu, X. Wang, S. Zou, M. Qi, and F. Gan, “Design of a SO₂ top-cladding and compact polarization splitter-rotator based on a rib directional coupler,” Opt. Express 22(4), 4137–4143 (2014).

36. Y. Xiong, D. X. Xu, J. H. Schmid, P. Cheben, S. Janz, and W. N. Ye, “Fabrication tolerant and broadband polarization splitter and rotator based on a taper-etched directional coupler,” Optics Express 22(14), 17458–17465 (2014).
SOI thickness: multi-micron SOI (usually 3μm) with low-confinement modes [10,11] and having low PDL, high performance PSR devices. However, this approach depends on both polarizations [9]. Given the ability to very easily scale to complex systems-on-chip, this chip, we can achieve low PDL without forcing the entire on-chip device library to deal with and rotates the polarizations of the fiber into two parallel but physically separate channels on-polarization – by creating a single polarization splitter/rotator (PSR) device which both splits polarization dependent loss (PDL) [6–8].

Single-polarization input). Considerable engineering went into developing devices with low connected to the laser with expensive polarization maintaining fiber, and accepting only exception of lasers (typically transmitting TE polarization) and sometimes modulators (often for data transmission systems have been forced to be polarization-independent, with the devices were constrained to accepting both polarizations. Historically, most optical devices switches, ROADM's, attenuators – and for receivers, it has historically been the case that graceful with both polarizations is of the essence. For anything inside the network – designs, especially receivers [5]. For low-cost, high-volume applications, being able to deal projections of TE and TM to an on-chip waveguide. This is a serious issue for many on-chip fabrication processes [1]. Building photonics in SOI also offers paths to integration with CMOS and bipolar electronics, either monolithically or through bonding-based integration [2–4]. One of the central challenges in developing practical silicon photonic systems-on-chip is to address the polarization incompatibility between a circular single mode fiber and a rectangular on-chip waveguide.

Polarization in an on-chip waveguide is restrained to transverse electrical (TE) and transverse magnetic (TM), which by default have very different effective indices, unless the waveguide is either low-confinement or square. In a single mode fiber, polarization is not maintained but instead changes randomly with environmental variations, causing random projections of TE and TM to an on-chip waveguide. This is a serious issue for many on-chip designs, especially receivers [5]. For low-cost, high-volume applications, being able to deal gracefully with both polarizations is of the essence. For anything inside the network – switches, ROADM’s, attenuators – and for receivers, it has historically been the case that devices were constrained to accepting both polarizations. Historically, most optical devices for data transmission systems have been forced to be polarization-independent, with the exception of lasers (typically transmitting TE polarization) and sometimes modulators (often connected to the laser with expensive polarization maintaining fiber, and accepting only single-polarization input). Considerable engineering went into developing devices with low polarization dependent loss (PDL) [6–8].

In silicon photonics, we have an opportunity to leverage complexity in order to deal with polarization – by creating a single polarization splitter/rotator (PSR) device which both splits and rotates the polarizations of the fiber into two parallel but physically separate channels on-chip, we can achieve low PDL without forcing the entire on-chip device library to deal with both polarizations [9]. Given the ability to very easily scale to complex systems-on-chip, this plays to the advantages of the silicon photonics platform. However, this approach depends on having low PDL, high performance PSR devices.

To address the issue, major silicon photonics platforms gravitate toward to two types of SOI thickness: multi-micron SOI (usually 3um) with low-confinement modes [10,11] and submicron SOI (usually 220nm, 250nm, or 300nm) [12–15]. For multi-micron SOI waveguides, polarization independent circuits can be built due to low confinement of optical

1. Introduction

In addition to transistors, silicon-on-insulator (SOI) material has been proven to be a suitable substrate material for photonic devices, thanks to its high index contrast, tight manufacturing tolerances, compatibility with complementary metal-oxide semiconductor (CMOS) fabrication processes [1]. Building photonics in SOI also offers paths to integration with CMOS and bipolar electronics, either monolithically or through bonding-based integration [2–4]. One of the central challenges in developing practical silicon photonic systems-on-chip is to address the polarization incompatibility between a circular single mode fiber and a rectangular on-chip waveguide.

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modes. However, this SOI platform usually requires very large bend radius (250 µm in [16]). Although well-engineered Euler bends with radius smaller than 10µm has been reported recently [17], it is still hard to build dense and energy efficient photonic devices like micro-ring modulators [18,19]. It is also challenging to build efficient high-speed Mach-Zehnder modulators and photo detectors in such a platform.

Presently, submicron platforms are emerging as the dominant ones for large-scale integration. The width of a single mode waveguide in such platform is usually ~2 times larger than its thickness in order to provide strong mode confinement, thus enabling tight bends (radius <2.5 µm in [18]). But high polarization dependence (birefringence) is introduced at the same time. The performance of photonic devices such as directional couplers and modulators is usually very different for TE and TM modes. For submicron platforms, polarization conversion is needed at the interface between optical fiber and on chip photonic integrated circuits (PIC). After light is coupled onto the silicon chip, a polarization splitter and rotator (PSR) is used to separate the incoming TE and TM light component and convert them into TE modes at the two output ports, so that the remainder of the PIC can operate in only one mode.

Many efforts have been made to improve performance of the PSRs on SOI platforms, especially in the past four years. In some designs, polarization splitter [20–22] and polarization rotator [23–25] are reported individually. One can construct a PSR by combining a splitter followed by a rotator [9,26], or a rotator followed by a splitter [27–32]. In the latter case, the rotator usually rotates TM0 mode into some intermediate modes such as TE1 mode, with TE0 mode undisturbed. In other designs, polarization splitting and rotating happens simultaneously [33–36]. To characterize a PSR, important metrics such as polarization conversion efficiency (PCE), insertion loss (IL), polarization crosstalk, PDL as well as footprint, fabrication complexity, and fabrication tolerance must be considered. The state-of-the-art experimentally demonstrated performance of CMOS compatible PSRs have > 97% PCE, ~0.5-1 dB IL, 1 dB PDL and ~15 dB crosstalk with device lengths vary from ~20 to ~500 µm [26,30,31,34].

To the best of our knowledge, all reported PSR designs use pure TE0 and TM0 mode as basis set. That is to say, the incoming TE0 component is directed to one output port, while TM0 component is directed to the other port (rotated to TE0 mode). However, the separation of pure TE0 from the TM0 mode is not required. In fact, the State Of Polarization (SOP) of the input optical signal has been scrambled in the optical fiber during transmission, and the pure TE0 and TM0 component does not hold a unique advantage over other orthogonal bases. By breaking this constraint, we have a much wider design space, which enables us to build more optimal devices.

In this paper we introduce a novel PSR that utilizes the linear combination of TE0 and TM0 as orthogonal bases. The orthogonal bases of this PSR are rotated by 45 degrees compared with conventional PSRs, in other words, 45deg polarized incoming light relative to the orientation of the chip (TE0+/−TM0) is fully directed to one output. This design is symmetric in geometry, offers great design freedom to eliminate PDL, and is easy to realize. Our design also presents a new perspective for integrated PSR designs in the future.

In order to prove the concept, we’ll demonstrate a four-channel polarization insensitive wavelength division multiplexing (PI-WDM) receiver (RX) employing a prototype 45-degree PSR. 40 Gb/s data rate with 0.7 +/- 0.2 dB PDL is achieved on each channel (highest single-channel data rate and lowest PDL among reported SOI PI-WDM RXs to date, to the best of our knowledge). Lastly, we’ll propose an improved ultra-compact 45-degree PSR design with 12 µm device length, < 0.1 dB PDL, < 0.4dB simulated IL and < 0.05dB wavelength dependence across C-band for both polarizations.
2. Principle of the 45-degree PSR

A PSR is a device that converts the two orthogonally polarized modes received from the fiber into two copolarized, spatially separated modes [37]. Supposing TE0 goes to top branch and TM0 goes to bottom branch (rotated to TE0) at the output ports, the relation between output modes \( \begin{bmatrix} E_{TE0}^{top} \\ E_{TE0}^{bot} \end{bmatrix} \) and input modes \( \begin{bmatrix} E_{TE0}^{in} \\ E_{TM0}^{in} \end{bmatrix} \) could be expressed as

\[
\begin{bmatrix} E_{TE0}^{top} \\ E_{TE0}^{bot} \end{bmatrix} = J \begin{bmatrix} E_{TE0}^{in} \\ E_{TM0}^{in} \end{bmatrix},
\]

where \( J \) is the Jones’ matrix of PSR. From the definition, any device with unitary Jones’ matrix can serve as a PSR.

Figure 1(a) shows the principle of conventional PSR. The goal of a conventional PSR is to separate TE0 and TM0 and rotate TM0 into TE0. For ideal conditions (no IL and no polarization crosstalk), we write \( J \) for conventional PSR,

\[
J = \begin{bmatrix} 1 & 0 \\ 0 & e^{i\phi} \end{bmatrix},
\]

where \( \phi \) is the phase difference between TE and TM path.

Figure 1(b) shows the principle of a 45-degree PSR. As light propagates along the device, the TM0 mode is first rotated into a TE1 mode by a rotator while the TE0 mode is left undisturbed. The TE0 and TE1 modes are then separated in a splitter, which produces two distinct TE0 modes. The splitter functions as a 3dB divider and can be implemented with a symmetric Y-junction.

A detailed schematic of a 45-degree PSR showing the spatial evolution of the mode profile is illustrated in Fig. 1(c). The TM0-to-TE1 rotation is realized by a Si bi-layer taper similar to those referenced in [30,38]. Both TE1 and undisturbed TE0 mode are then split via a Y-junction. The Jones’ matrix for an ideal 45-degree PSR is:
\[ J = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -e^{i\phi} \\ 1 & e^{i\phi} \end{bmatrix}. \] (3)

It is worth mentioning that Eq. (3) can be interpreted as multiplying Eq. (2) by a rotation matrix at 45-degree rotation angle. Thus the orthogonal bases of the PSR have been rotated by 45 degrees compared with conventional designs.

For a pure TE0 input, the input vector is \([1, 0]\), the output is \([1/\sqrt{2}, 1/\sqrt{2}]\) which means the optical field in the top and bottom output waveguides are equal and in phase. Similarly, for pure TM0 input \([0, 1]\), the output optical fields are equal but out of phase. If an input polarization is 45deg polarized \((1, 1)\) or \((1, -1)\), the output can be completely routed to the top or bottom output waveguide, given \(\phi\) is an integer multiple of \(\pi\).

Due to differences of effective index \((n_{\text{eff}})\) in different optical modes, time skew can be an intrinsic limitation of the PSR design. Considering a 100\(\mu\)m long device with 220 nm thick top Si and 500 nm wide channel waveguide at the input \((n_{\text{eff,TE0}} = 2.45\) and \(n_{\text{eff,TM0}} = 1.78\)) the time skew between TE path and TM path at the output is estimated to be no bigger than 0.2 ps, which is not a major limitation of timing jitter for data transmissions at 40 Gb/s or less.

Fig. 2. (a) Layout of the prototype 45-degree PSR design. (b) Micrograph of the fabricated device.

Based on the principles stated above, a prototype 45-degree PSR is designed from a linear bi-layer taper followed by a Y-junction on 220nm SOI, as shown in Fig. 2(a). The total device length is 44.3 \(\mu\)m, including the routing bends of the Y-junction. The simulated insertion loss is 0.68 dB for TE0 and 0.78 dB for TM0. The device (together with the RX system in Section 3) is fabricated using a 248nm lithography CMOS-compatible process on an 8-inch SOI wafer through an OpSIS-IME multi-project-wafer (MPW) run [12]. A micrograph of the fabricated prototype PSR is given in Fig. 2(b).

3. Design and characterization of a four-channel PI-WDM receiver

3.1. Design of a four-channel PI-WDM receiver

To prove the concept of this design, we constructed a four-channel polarization-insensitive wavelength division multiplexed (PI-WDM) receiver (RX) system. The schematic of the system is depicted in Fig. 3(a). Light with arbitrary polarization is first coupled to a Si nanotaper edge coupler from a lensed fiber and then separated by a 45-degree PSR, followed by two mirrored 1 x 4 WDM demultiplexers (DeMUXs). Schematic of the DeMUX is shown at the bottom of Fig. 3(a). Finally, the light in both branches combines at the gain peaking photo-detector (GPD) [39]. Different from the GPD in [39] where light can only come from one waveguide, the GPD here is tapered to two directions, as illustrated at the top right of Fig. 3 (a), to absorb light from two separate waveguides. We refer to it as bi-directional PD. The four-channel WDM DeMUX consists of two stages of unbalanced MZI, as shown at bottom of Fig. 3(a). The MZIs have integrated thermal tuners to align the spectra. Performance of the thermal tuner is similar to our previous report [40].

The entire receiver system has a footprint of 2.4 x 2.4 mm². A micrograph of fabricated system is shown in Fig. 3(b). Unfortunately characterization structure of a single PSR device is not available due to the space limitation in the MPW run.
3.2. PDL measurement

To characterize the RX system, the center wavelengths of the WDM DeMUX need to be aligned for all four channels. The four channels (CH1, CH2, CH3 and CH4) are defined in Fig. 3(a), corresponding to the four GPDs in micrograph of Fig. 3(b), counting from top to bottom, respectively. A rough spectrum alignment can be quickly achieved by sending CW laser input with scrambled polarization and correct wavelength while maximizing the photocurrent of each channel.

Rough aligned spectra are shown in Fig. 4(a). The channel spacing is measured to be 6.5nm. The entire spectra are well aligned across a 50nm range around 1550nm. Channel crosstalk is less than $-11$ dB. Figure 4(b) depicts theoretical wavelength response of the WDM DeMUX for reference. Compared with theoretical calculations, channel crosstalk is degraded in the real system, due to alignment accuracy as well as the non-ideal 3dB splitting ratio and wavelength dependence of the directional couplers (DCs).

In order to measure the PDL in each channel accurately, we set up a 10 Gb/s non-return-to-zero on-off-keying (NRZ-OOK) data transmission link in combination with an inline wavelength sweep. The data link setup is sketched in Fig. 5(a). The tunable CW laser is first modulated by a commercial modulator with a 10 Gb/s PRBS$^{31}$-1 (Pseudorandom binary sequence) data pattern and then amplified by an erbium-doped fiber amplifier (EDFA) to overcome the optical loss in the link. The amplified signal then goes through a polarization controller (PC) and a polarization scrambler (PS) before it is coupled to the RX chip. The GPD is biased at 2V through a bias-tee during measurement.
On each channel, we first enable the PS, fine tune the phase tuners in the DeMUX so the noise on the ‘0’ and ‘1’ rails on the eye diagram are minimized (recorded as ‘On’ condition). Then we disable the PS, and adjust the polarization controller manually to find the polarization states where the eye amplitude is maximized (‘Off Max’ condition) or minimized (‘Off Min’ condition), and record the spectral sweep.

The eye diagrams are recorded in Fig. 5(b), showing good channel-to-channel uniformity. The inline spectrum sweeps are plotted in Fig. 5(c). The shaded area between Off Max and Off Min indicates PDL of each channel. As anticipated, scrambled (i.e., On condition) spectrum mostly sits inside the shaded area of related channel. Note the noise level is increased and shows strong wavelength dependence due to the introduction of an EDFA. The channels crosstalk is reduced from −9 dB at 1530.5 nm (CH1) to −14 dB at 1550 nm (CH4).

PDL is quantified from both eye amplitude and the spectrum sweeps, shown in Table 1. The PDL of eye diagram is calculated by dividing the amplitudes of Off Max and Off Min, i.e., \(10 \times \log_{10}(\text{Off Max}/\text{Off Min})\). The result is in the second row of Table 1. The PDL from sweeps can be simply calculated by subtracting photocurrents in dB scale. Row3–5 shows PDL regarding different wavelength ranges with respect to channel center wavelengths, to give a fair comparison. For clarity: Row 2 (“Eye Diagram”) represents the results of the eye-diagram based measurements of PDL, while rows 3-5 show the results of various ways of interpreting the swept spectrum measurements in order to extract the PDL. The two measurements align to within 0.35dB.

But overall, the results from sweeps match quite well with the eye diagram testing. CH1 and CH2 have slightly higher PDL from both eye diagram and wavelength sweeps, possibly due to slightly misalignment of the WDM DeMUX. Overall, the receiver demonstrates an excellent PDL of 0.7+/−0.2dB. This is higher than the 0.1dB PDL predicted by the simulation on the 45-deg PSR. The extra PDL is introduced by the edge coupler, non-ideal 3dB DCs and unbalanced thermal tuner losses.

During measurement, the input power to the chip is kept at 5dBm. Considering a typical 0.75 A/W responsivity at 2V bias [39], the received peak power can be calculate from Fig. 5(c) to be around −1.2 dBm. Thus, the total passive loss of the RX is about 6.2dB, including silicon edge coupler, 45-degree PSR, DeMUX, and the routing waveguides.
Table 1. Quantified PDL measurement

| PDL (dB)            | CH1   | CH2   | CH3   | CH4   | Avg  | Std  |
|---------------------|-------|-------|-------|-------|------|------|
| Eye diagram         | 0.78  | 1.00  | 0.54  | 0.77  | 0.77 | 0.19 |
| Peak wavelength     | 0.45  | 1.02  | 0.64  | 0.82  | 0.73 | 0.24 |
| +/- 0.5 nm          | 0.48  | 0.99  | 0.53  | 0.71  | 0.68 | 0.23 |
| Entire spectrum     | 0.74  | 1.08  | 0.52  | 0.52  | 0.72 | 0.26 |

3.3. 40 Gb/s NRZ-OOK data transmission

The above PDL measurement in a 10 Gb/s data link has proven the functionality of the 45-degree PSR. Meanwhile, a PI-WDM system itself is interesting for investigation considering its importance in non-coherent silicon photonic detectors [41–43]. Therefore we further push our system from 10 Gb/s to 40 Gb/s. The data link setup is identical to that described previously, except for now we are using a 40Gb/s pulse pattern generator (PPG) with PRBS231-1 data pattern. The RF probe is switched to a 50-Ohm terminated configuration in order to reduce RF reflection as in [18,44] while bias voltage is changed from 2V to 4V to increase PD bandwidth.

The measured 40Gb/s eye diagrams are shown in Fig. 6. All four channels show open eyes with very good channel-to-channel uniformity. Also all the four channels present very small polarization dependence. PDL is estimated to be 0.3 – 0.8 dB by reading the amplitudes. Although the PDL estimation is less accurate than in the 10 Gb/s measurement due to larger noises in 40 Gb/s eye diagrams, the overall result is consistent. To conclude, we demonstrate 40Gb/s/channel data transmission in a PI-WDM RX system enabled by a novel 45-degree PSR. To the best of our knowledge, we believe this system reveals highest single-channel data rate with lowest PDL among reported PI-WDM RX on-chip systems to date.

4. An improved ultra-compact 45-degree PSR

The prototype of the 45-degree PSR we designed has a simulated loss of 0.68 dB for TE0 and 0.78 dB for TM0 with ~50 μm device length. There is still much space left for improvement. Since the entire device is symmetric in geometry, it is well suited for finite difference time domain (FDTD) coupled particle swarm optimization (PSO), as we’ve demonstrated in designing high performance waveguide Y-junction and crossing [45,46]. The optimization can be divided into two stages. The first stage is to optimize the TM0-to-TE1 bi-layer taper. Here we migrate the same bi-layer taper (9 μm long, 97% PCE) as in our ultra-compact polarization rotator design [25]. Adiabatic linear tapers can be used if footprint is not a constraint. The second stage is to optimize a Y-junction, therefore procedures in [45] can be
used. Instead of compact Y-junction, Y-splitters based on adiabatic couplers can also be used to potentially reduce back reflection.

Following this method, we realized an improved 45-degree PSR design. The design has very low and well-balanced insertion loss: ~0.35dB for TE0 and ~0.25 dB for TM0 (Fig. 7(a)), with PDL < 0.1dB across 1520nm–1570nm (more than entire C-band). It’s worth noting that TM0 loss here is 0.1 dB lower than TE0, which is hard for conventional asymmetric PSRs since extra loss is often introduced when rotating TM0 to TE0. Moreover, the Y-junction part offers great design freedom to control PDL. One can engineer the TE0 and TE1 loss by engineering the geometry of a Y-junction, even without the assistance of PSO. In some cases, it is even possible to design a PSR that has compensated PDL of edge coupler to completely eliminate the PDL. Since no directional-coupler-like structure is introduced, the device is also ultra-broadband. For both polarizations, the wavelength dependence is < 0.05 dB across 50nm range.

The output transmittance as a function of polarization angle (consider linear polarization) is also simulated (Fig. 7(b)). The power equally splits at single TE0 (0 degree and 180 degree) and TM0 (90 degree) input. While at equalized TE0 and TM0 components (~45 degree and ~135 degree), the power is mainly routed to only one branch (bottom branch and top branch for 45 degree and 135 degree, respectively). This is the major feature of 45-degree PSR. Note that in real designs, the angle may slightly shift from 45-degree due to PDL and phase error. The polarization crosstalk can be read at the null point of either branch, which is around –17 dB.

Figure 7(c) demonstrates how the 45-degree PSR functions with E-field plot at three specific input polarizations states: TE0 (top), TM0 (middle) and 45-degree polarization (bottom). One can clearly see the in-phase output for TE0, anti-phase output for TM0 and single branch output (with weak crosstalk) at 45-degree polarization. The device is ultra-compact, only 12 μm excluding the routing waveguide bends (20 μm if these are included).

5. Conclusions

In summary, we proposed a novel symmetric PSR design, which we call a ‘45-degree PSR’. This PSR takes TE0+/−TM0 as orthogonal bases for polarization splitting and rotation, different from any conventional PSRs, which perform on pure TE0 and TM0 bases. To proof the concept of the 45-degree PSR, we demonstrated a 40 Gb/s data transmission in a four-channel PI-WDM RX system with only 0.7 +/− 0.2 dB PDL. To the best of our knowledge, we believe this RX has the highest single-channel data rate and lowest PDL compared to other
PI-WDM RXs reported to date. Finally, we proposed an improved 45-degree PSR design with 12 μm device length, < 0.1 dB PDL, < 0.4dB simulated insertion loss and < 0.05dB wavelength dependence across C-band for both polarizations. This design shows dramatic improvement in device length, PDL and bandwidth compared to conventional PSRs. The 45-degree PSR design concept we proposed replaces asymmetrical directional-coupler-like structures with a symmetric and compact single layer Y-junction to realize polarization separation, which dramatically reduces the design complexity but meanwhile enhances the bandwidth and fabrication tolerance. Our work presents a new perspective for integrate PSR designs in future.

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