A novel SEU tolerant memory cell for space applications

Dianpeng Lin\textsuperscript{1,2}a, Yiran Xu\textsuperscript{1,2}, Xiaoyun Li\textsuperscript{1,2}, Xin Xie\textsuperscript{1,2}, Jianwei Jiang\textsuperscript{1,2}, Jiangchuan Ren\textsuperscript{1,2}, Huilong Zhu\textsuperscript{1,2}, Zhengxuan Zhang\textsuperscript{1}, and Shichang Zou\textsuperscript{1}

\textsuperscript{1} Shanghai Institute of Micro-system and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China
\textsuperscript{2} University of Chinese Academy of Sciences

a) Dianpeng.Lin@outlook.com

Abstract: In this paper, an improved design of a radiation hardened memory cell (RHMC), based on the SEU (single event upset) physics mechanism and reasonable transistor size, is proposed. The memory cell can enhance the reliability for space radiation environment, which also can offer differential read operation for robust sensing. With the help of 90 nm standard digital CMOS technology, the simulation demonstrates that the proposed radiation hardened memory cell has the ability to recover an SEU in any one sensitive node and provides multiple-node upsets protection. The comparisons for previous several hardened memory cell are also executed, which shows the proposed memory cell keeps advantages of low power and high stability.

Keywords: radiation hardened memory cell, single event upset, space radiation, static random access memories

Classification: Integrated circuits

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1 Introduction

The SRAMs are widely used in digital information processing and control system, and play a key role in terms of power, delay, area, and critical reliability [1]. With the technology scaling down, the memory cells SRAMs (Static Random Access Memories) have lower supply voltage and smaller node capacitance, which makes them more susceptible to radiation particles, such as alpha particles, heavy ion and cosmic rays. In space exploration and high energy physics experiment, single event upset (SEU) is a primary reliability concern, because the SEU can disturb the state of SRAMs, leading to system function disorder and causing serious consequences [2]. When radiation particles pass through the sensitive node of SRAMs, it will release electron-hole pairs along its path. Under the action of electric field, the holes move toward the source region of the transistor, while the electrons move toward the drain region end of the transistor. When these electrons are accumulated to a certain extent, the stored state in this sensitive node will be changed [2]. Therefore, it is necessary to study and design SRAM cell that has the ability of resisting SEU.

2 Previous radiation hardened memory cells

Using circuit-level radiation hardened memory cells to provide tolerance against SEU is a less area, delay, and power technique compared to system-level design. Up till now, some radiation hardened designs are proposed to alleviate the effects of SEU on memories. For example, in [3], a 10T hardened SRAM cell using ten transistors is proposed, which is named as Quatro10T cell. With the help of a negative feedback, it can recover from $1 \rightarrow 0$ SEU. However $a \rightarrow 1$ SEU can flip the state of the cell. In Fig. 1(a), when node QB is flipped from 0 $\rightarrow$ 1, state of the cell will be changed. In [4], based on stacked structure, two kinds of 10T memory cell (PMOS stacked-10T (PS-10T) and NMOS stacked-10T (NS-10T)) were proposed to resist SEU happening. However they can’t provide full SEU immunity, because NS10T memory cell can not resist 1 to 0 SEU. In Fig. 1(b), when node A is flipped from 1 $\rightarrow$ 0, the state of the cell will be changed; while PS10T can only resist 0 to 1 SEU. In Fig. 1(c), when node D is flipped from 0 $\rightarrow$ 1, the state of the cell will be changed.

In [5] a new 13T SRAM cell structure is proposed. In Fig. 4(d), with the help of the refreshing mechanism, the 13T memory adopts four switches cut off the
feedback loop to prevent SEU propagating back to its starting node. For example, if node QB is flipped to state 1, node Q will hold its initial state 1 because of the transistors P3, P4, N3, and N4 closed by the control signals. Then node QB will recover to its initial state 0 by opened transistor P2. And in memory storage time, the 13T SRAM cell holds the storage status by using the refresh control signals. Besides, it takes advantage of hysteresis effect of Schmitt trigger to improve reliability. However, due to the refreshing mechanism, this memory design needs extra circuit, which means covering larger area of the SRAM chip. Moreover, the single-ended structure is not common for commercial use.

3 Proposed SEU hardened SRAM cell circuit design

A. Cell Structure and Behavior

The proposed SEU tolerant SRAM bit-cell design is shown in Fig. 2. Two access transistors, P7 and P8, connect the bit-lines (BL and BLN) with the storage nodes Q and QB. Besides cross coupled transistors pairs N1 and N2 are also the storage nodes, which create the redundancy of data for SEU tolerant. Suppose the stored data is 1(Q = 1, QB = 0, S1 = 1, S0 = 0) for the proposed RHMC. In the hold operation, when word line WL is in 1 state, access transistors P7 and P8 are turned off. Transistors P1, P4, P6, N1 and N3 are turned on, while the other

Fig. 1. (a) Quatro10T cell, (b) PS10T cell, (c) NS10T cell, (d) 13T cell
transistors are turned off. The proposed memory cell steadily maintains its initial stored value.

Before normal read operation, the bit-lines are primarily pulled up to high potential by the pre-charge circuit. When the read operation begins, the word-line is set to 0. The state of node Q remains 1, and the state of QB is 0. Thus the driven transistors P6 and P8 discharge BLB. When the voltage difference happening between the bit-lines is enough, a sense amplifier in memory will recognize the voltage difference and output the stored state.

Finally, to change the stored data of the proposed memory cell, the word-line WL is discharged to 0. Then the BLB is charged to VDD, simultaneously the BL is pulled down to 0. As a result, the state of Q is discharged to 0, which turns on the transistors P2 and P3. Then, the state of nodes QB and S0 are charged to VDD because of the opened PMOS. At last the transistors N2 and N4 are turned on by the state of S0 and QB, and the S1 is discharged to 0.

B. SEU Recovery Analysis

Considering the state (S1 = 1, S0 = 0, Q = 1, QB = 0) shown in Fig. 2 we can find that the nodes S1, S0 and QB are surrounded by the reverse-biased drain junctions of a transistor biased in the OFF state [2], which makes these nodes of the cell easily affected by radiation particles. Node Q is not affected by radiation particles because the state of Q is 1 and Q is only surrounded by PMOS transistors. On the basis of SEU physics mechanism, when a heavy ion hits PMOS transistors around Q, only a positive transient pulse occurs which will not change the state of Q. The SEU robustness of the proposed RHSC is discussed detailedly.

1) If node S1 is flipped to 0 by radiation particle, transistor P5 is turned on and transistor N1 is turned off temporary. However, with the help of larger size of transistor P1, the state of Q can hold its initial state. We design that the size of transistor P1 is 2.3 larger than that of transistor P5. At last, the states of Q and QB

![Fig. 2. Proposed radiation hardened memory cell RHMC.](image-url)
are not changed which make the transistor P4 open all the time. Thus, the state of S1 will be charged to VDD.

2) If the stored data in node S0 is changed to 1 by radiation particle, it goes high and turns on the transistor N2. At the same time, the transistor P6 is turned off temporary, which makes the nodes QB in a high impedance state. QB holds its initial state, which makes transistor N4 be turn off and P4 be turned on. As a result, S1 can hold its initial state 1, and turns of transistor N1. Besides, the disturbance of node S0 cannot be propagated to node Q. S0 will be discharged 0 through the opened transistors N1 the N3.

3) If the node QB is struck by heavy ion, it goes high. Transistor P1 is turned off and transistor N4 is turned on temporary, which make the node Q1 in a high impedance state. The disturbance of node QB cannot be propagated to node S0, because the transistors N1 and N3 are keeping on all the time. With the help of state of S0, QB is discharged to 0 through the opened transistor P6. At last, QB will recover to its initial state 0.

4) When node pair S0–S1 is flipped due to charge sharing, transistors P5 and N2 are turned on and transistors N1 and P6 are turned off temporary. At this time, P1 and P5 are opened at the same time. As analysis above, we design that the size of transistor P1 is 2.3 larger than that of transistor P5. And the node Q can hold its initial state 1 due to larger size of transistor P1. Thus the disturbance of pair node S0–S1 cannot be propagated nodes Q and QB, which makes the transistors P4 and N4 be on and off state. At last the state of S1 will be charged to VDD through transistor P4, and the state of S0 will be pulled down to state 0 through opened transistors N1 and N3.

4 Evaluation

A. SEU Recovery Simulation and analysis

By the use of 90 nm standard digital CMOS technology, the performance and SEU recovery of the proposed SRAM cell is simulated by the simulation tool Cadence. For fair comparisons, all SRAM cells are design by the same sized transistors, and simulation parameters are set 1.2 V power supply at room temperature.
To simulate impact of a SEU induced by particle happening in the proposed SRAM cell, a double exponential current pulse is used [6, 7, 8, 9]. As is shown in Fig. 3(a), a current source is added to the drain terminal of the PMOS, which is used to mimic a positive transient pulse. In Fig. 3(b), similarly, a current source is added to the drain terminal of the NMOS to generate a negative transient pulse at NMOS.

Before SEU simulation, we write state 1 into the SRAM cell at the beginning. After a while, the SRAM cell is in hold state, and state of node Q is set to 1(QB = 0, S1 = 1, S0 = 0). Soon afterwards, to imitate a single event transient (SET), a double exponential current pulse is injected into the sensitive nodes QB, S1, S0 respectively. And voltage responses of nodes QB, S1, S0 are shown in the Fig. 4. From the simulation results, we can see that there are no flips happening in the memory cell for all the sensitive nodes. At 20 ns, SET current strikes node QB, and a $0 \rightarrow 1$ transient fault is occurred at node QB. It takes about 2 ns for QB to recover to its initial state 0 from 1. At 20 ns, a $1 \rightarrow 0$ transient fault is appeared at node S1 when SET current hits node S1. It takes 1.5 ns to recover to its initial state 1. Besides, when SET current hits node S0 at 20 ns, a $0 \rightarrow 1$ current is observed at node S0. Then, it takes 1 ns to recover to its original state 0. At last, a $1 \rightarrow 0$ transient fault and a $0 \rightarrow 1$ transient fault are appeared at node S1 and S0 simultaneously when SET current hits pair nodes S1 and S0. As above analysis, the pair nodes S1 and S0 take 2 ns to recover to their initial state.

**B. Comparisons of access time, area, and power consumption for various SRAMs cells**

The performance of the proposed design RHMC is compared with previous radiation hardened cells standard 6T cell, Quatro10T, PS10T, NS10T, and 13T. We
have made a comparison of these parameters including area, power consumption, read access time, write access time and transistors number. The definition of read access time is the time interval from the active word line edge crossing its threshold (50% of VDD) to bit lines developing 50 mV differential voltage [10]. Besides a 0.3 pF capacitance is added to each bit line. The definition of write access time is the time interval from midpoint of active word line edge to the intersection of cell’s two storage nodes [10]. The performance results of the parameters for comparative SEU hardened SRAM cells are shown in Fig. 5. And the performance results of the parameters in Fig. 5 have been normalized to that of 6T memory cell.

From Fig. 5, we can see that the proposed memory cell has the 2nd area. In order to obtain better radiation hardness in circuit design, two more transistors are added in the design compared to previous hardened cell Quatro10T, which will cover a larger area. Compared with other hardened cell, the power consumption of the proposed memory cell is lowest, which is suitable for low power radiation application. For our RHMC, its write access time is 87.2%, 109.3%, 129.7% and 46.7% of Quatro10T, PS10T, NS10T and 13T cells, respectively. The simulation results of read access time in Fig. 5 show that our proposed RHMC has the highest read access time. That is because, in order to provide full SEU immunity NMOS access transistors are replaced by PMOS transistors (P7 and P8), and two pull-down transistors are replaced by PMOS transistors (P5 and P6). These improvements can prevent any negative transient pulse occurring at nodes Q and QB, and obtain a better SEU fault tolerance capability for the proposed RHMC, while reduce the read access time of the proposed RHMC. In general, as the simulation results of SEU Recovery and Comparisons shown, the proposed RHMC has more radiation hardness in circuit design with modest performance degradation which makes it a good choice for critical space applications.
5 Conclusion

In this paper, an improved radiation hardened memory cell is proposed, which has highly reliable and low-power capability and offers differential write and read operation. The proposed memory cell can provide full immunity for any single sensitive node and provide multiple-node upsets protection. For the proposed RHMC, having a high read access time is the only deficiency because of PMOS access transistors and stacked structure, which is not suitable for high speed application. However, the main target of these radiation hardened memory cells is to tolerant SEU, thus, from a low-power radiation hardened application designer point of view, the proposed RHMC is suitable for providing full immunity against SEU.