Coupled electron and thermal transport simulation of self-heating effects in junctionless MOSFET

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Abstract.
This paper explores self-heating effects on junctionless gate-all-around nanowire MOSFET using self-consistently coupled 3D full band electro-thermal transport. The self-consistent algorithm begins by supplying the heat generation data from the 3D electron Monte Carlo with 2D quantum correction to the phonon Monte Carlo. Subsequently, the phonon Monte Carlo transports the phonons introduced from the electron simulation and considers their scattering through the anharmonic three-phonon processes. The anharmonic three-phonon decay and the use of full dispersion facilitate a detailed description of heat transfer and the determination of the temperature map. We compare the performance of gate-all-around junctionless against the conventional inversion mode gate-all-around MOSFET. Our results indicate that junctionless MOSFET has less self-heating effects than the conventional inversion mode device, particularly at the limits of high currents.

1. Introduction
Thermal management and power dissipation issues in microprocessors are quickly emerging as the ultimate bottleneck to improving the performance of consumer/commercial electronics. Controlling device temperature and power dissipation is a key to sustaining electronic devices with longer battery life and improves the overall device reliability and life expectancy. As such, thermally conscious blueprints has become in recent years the focal concern of semiconductor roadmaps, at all design phases, as the temperature at the chip level and within a single transistor rises for future electronic devices [1, 2]. Without proper thermal management, inordinate power dissipation can potentially bring to end integrated circuit functionality. In this regard, coupled electro-thermal simulation model that self-consistently couple the electronic and phonon transport is essential in creating a cycle that will push designs to have lower carbon footprints and in creating environmentally conscious electronics that minimize waste.

Recently, junctionless (JL) transistor has been introduced to circumvent the adversity encountered in forming ultra-shallow junction [3, 4]. The idea behind junctionless transistors is similar to that of a gated resistor: the channel and the S/D regions are doped with the same polarity (n- or p-type) and concentration. As such, there are no junctions formed between the S/D regions and the channel; hence, considerably simplifying the fabrication process. In
addition, junctionless transistors operate as depletion-mode (DM) devices and rely heavily on
the use high workfunction gate and the ultrathin body. In this paper we employ a phonon Monte
Carlo Transport (pMC) coupled to a 3D full band electrical Monte Carlo simulator (MoCa) with
2D quantum corrections [5], to examine the electro-thermal transport of junctionless Multigate
MOSFET.

2. Thermal MoCa: Self-consistently Coupled electron and phonon Monte Carlo
In order to capture the details of self-heating in nanoscale devices, we need to carefully model
phonon generation and transport and couple it to the electronic transport in a self-consistent
manner. The self-consistency between the electronic and thermal simulations is critical to
obtaining meaningful results in ultrascaled multi-gate MOS devices because of the strong self-
heating effect which arises out of the small physical dimensions of the device. Thermal MoCa [5]
self-consistently couples 3D electron Monte Carlo with full phonon dispersion and 2D quantum
correction (electrical MoCa) with a phonon Monte Carlo (pMC) which includes the influence
of anharmonic phonon decay. The full self-consistent two-way coupling of electron and phonon
populations is achieved in two steps added to the standard electron and phonon Monte Carlo
simulations. The phonon data is transferred from the electrical MoCa to the pMC simulator.
The pMC computes all the phonon interactions and then allows the phonons to travel using the
velocities obtained from the full phonon dispersion. The energy of all the phonons in the phonon
Monte Carlo step is calculated from their momenta using the full phonon dispersion relationship.
Once all the phonon interaction has been computed by the pMC, the next step is to use that
data to compute the temperature distribution across the device. The simulation domain in the
thermal transport is divided up into a mesh of small cubes with 1 nm sides and the energy of all
the phonons residing in each of the cubes is tallied. Subsequently, the total energy in each cube is
used as a source term in the heat diffusion equation which is then solved iteratively to obtain the
steady-state temperature distribution in the entire simulation domain. The temperature map
obtained from the thermal transport step (pMC + heat equation) is fed back to the particle
Monte Carlo with temperature dependent scattering table, and the process is repeated in a
self-consistent manner until convergence criterion is met. The inclusion of anharmonic phonon
decay, temperature dependent scattering rate, and full electron and phonon dispersion helps
create a clear picture of heat transfer and provides a comprehensive way to access self-heating
in nanoscale devices. The reader is referred to reference [5] for a more complete description of
the details of the electrical and thermal transport used in this work.

3. Discussion and results
A key consideration in junctionless MOSFET design is to employ a large metal workfunction
capable of fully depleting the channel at \( V_G = 0 \). Our previous work [6] on n-channel
junctionless MOSFET, using a metal workfunction of 5.15 eV, has demonstrated that even
for cross-sections as thin as \( t_{si} = 5 \text{ nm} \), the junctionless doping concentration must be less than
5 \( \times 10^{19} \text{ cm}^{-3} \) in order to regulate the off performance (leakage current) and achieve acceptable
\( I_{on}/I_{off} \) ratio [6]. Based on this, we employ a square cross-sectional length \( t_{si} = h_{si} = 5 \text{ nm} \) and
a doping density of \( 4 \times 10^{19} \text{ cm}^{-3} \). Additionally, the gate length \( (L_G) \) and gate oxide thickness
\( (t_{ox}) \) for the simulations presented here are 20 nm and 1 nm, respectively.

We plot the average velocity profile and temperature distribution of a fully-depleted gate-
all-around junctionless device (doping density = 4 \( \times 10^{19} \text{ cm}^{-3} \) and \( t_{si} = h_{si} = 5 \text{ nm} \)) in Fig.
1 a) and b), respectively. The temperature distributions were obtained after solving the heat
diffusion equation with Dirichlet (fixed) boundary conditions at the boundaries of the simulation
region. This can be seen in the temperature profiles of Fig. 1b) where the temperature at the
boundaries of the simulation region always stays at 300K. The results indicate inconsiderable
self-heating effect, due to the low current drive, as demonstrated by the negligible change in
average velocity between the electrical MoCa (uncoupled) and thermal MoCa, as well as the relatively low temperature distribution across the device. In order to explore this further, we benchmark the performance of JL GAA MOSFET with the conventional IM GAA. To ensure fair comparison, we simulate a JL and conventional IM GAA MOSFET with comparable power ($V_D \cdot I_D$) as shown in Fig. 2. We observe that the velocity degradation due to self-heating as well as the peak (maximum) temperature is higher for the conventional IM device. It is interesting to note that the average velocity of the inversion mode device (Fig. 2b) is higher than the saturation velocity for much of the channel ($x = 35-55$ nm), while the junctionless device shows that hot electrons (avg. velocity $\geq 1 \times 10^7$ cm/s) are mostly localized at the vicinity of the channel-drain region in both Figs. 1a) and 2b). Furthermore, looking at the peak temperature as a function of the overall power dissipation as well as the variation of drain current as a function of doping (Fig. 3) reveals that the constraints set by the requirement to fully deplete the junctionless MOSFET limits that junctionless MOSFET to mainly low power applications. At such limits, despite the JL outperforming IM MOSFET, the differences in temperature is not very appreciable, as was observed in Fig. 2. Additionally, Fig. 3 highlights that the JL transistor will notably outperform the conventional MOSFET at the limit of high currents. Higher currents require doping density in excess of $5 \times 10^{19}$ cm$^{-3}$, however, this leads to devices that are hard to turn off, as was discussed earlier even for cross-sections as small as
4. Conclusions

We have studied the self-heating behavior of junctionless gate-all-around MOSFET and benchmarked it against conventional inversion mode gate-all-around MOSFET using our in-house 3D full band coupled electro-thermal Monte Carlo simulator which explicitly takes into account the anharmonic three-phonon decay. Our results indicate that junctionless gate-all-around MOSFET has less self-heating effects as compared to conventional multi-gate MOSFET, particularly for applications that require high power. Suitable high workfunction metal gate (> 5.15 eV) as well as novel JL design schemes which will constrain the off-current to acceptable limits at $V_G = 0$ V needs to explored in order to facilitate high power operation of JL MOSFET.

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