Generation of the Single Precision BLAS library for the Parallella platform, with Epiphany co-processor acceleration, using the BLIS framework

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Abstract—The Parallella is a hybrid computing platform that came into existence as the result of a Kickstarter project by Adapteva. It is composed of the high performance, energy-efficient, manycore architecture, Epiphany chip (used as co-processor) and one Zynq-7000 series chip, which normally runs a regular Linux OS version, serves as the main processor, and implements “glue logic” in its internal FPGA to communicate with the many interfaces in the Parallella. In this paper an Epiphany-accelerated BLAS library for the Parallella platform was created (which could be suitable, also, for similar hybrid platforms that include the Epiphany chip as a coprocessor). For the actual instantiation of the BLAS, the BLIS framework was used. There have been previous implementations of Matrix-Matrix multiplication, on this platform, that achieved very good performances inside the Epiphany chip (up to 85% of peak), but not so good ones for the complete Parallella platform (due to inter-chip data transfer bandwidth limitations). The main purpose of this work was to get closer to practical Linear Algebra applications for the entire Parallella platform, with scientific computing in view.

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1. Introduction

In recent times there has been interest in the use of hybrid platforms (mostly CPUs with GPUs or Manycore accelerators) for scientific computation in large clusters. On the other hand RISC-based clusters, and ARM-based ones in particular, are also of interest, among other things, because of the low power consumption that is achievable on those architectures, and because new consumer products have made them ubiquitous (smartphones, tablets, etc.), lowering their cost. It is possible to think that the same way the consumer PC “explosion” gave many cheap hardware for use in modern HPC clusters (directly or indirectly), the “mobile” products could lead to new improvements in HPC infrastructure.

The Parallella platform [1] has both: it’s a hybrid platform based on an ARM CPU, and a manycore RISC device as a co-processor (the Epiphany) [2]. In this work the real and practical possibilities of the Parallella platform for Scientific Computing are explored. To have a starting point, the Linpack benchmark was chosen to be run on a cluster of Parallella nodes, but it was found that there was no (Epiphany accelerated) BLAS implementation for the platform. Therefore, a BLAS library was “instantiated” with the BLIS framework [3], after writing an Epiphany accelerated sgemm micro-kernel for it.

The idea for the micro-kernel was to use a “SUMMA-like” algorithm [4], that could improve the performance over current implementations (that use Cannon’s [5]). The achieved results, for the Matrix-Matrix Multiplication performance, were the best for this platform that are presently known to the author [6] [7] [8] (if the host processing and off-chip data transfer is taken into account).

In the following sections a very brief overview of the Parallella Board is given and then the current solution implementation, for instantiating the BLAS library, is explained. It was followed a “top-bottom” approach, in which the highest level parts of the system are explained first and the low-level parts later. In section 4 the results for a number of benchmarks are shown and in section 5 the conclusions and future work are stated.

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2. The Parallella board

The Parallella board [2] has one Zynq 7010 or 7020 chip acting as “the host processor”, one Epiphany chip acting as a “co-processor”, and a 1GB DRAM chip, of which 32MB are accessible to both the host and coprocessor (shared DRAM). It also contains many interfaces, like Ethernet, USB, a slot for an SD card, etc., to communicate with other hardware. The Zynq SoC [2] can be basically thought as a dual-core ARM Cortex-A9 CPU, with an FPGA embedded, and many on-chip interfaces. The FPGA is used to implement the “e-link” that is needed to communicate with the Epiphany chip.

1. sgemm: “Single Precision, General Matrix Multiplication”
That communications interface also allows the Epiphany chip to access the shared portion of RAM (32MB).

The Epiphany chip [10] consists of a 2D array of cores (“eCores”) connected by a mesh Network-on-chip. Each core contains a RISC CPU, a DMA engine, 32 KB of local memory and a Network interface (see figure [1]).

To program the Parallella architecture there are different options. The one chosen here was the eSDK [11] provided by Adapteva, which consists of a series C functions that allow the communication between a host and the Epiphany SoC (grouped in the “e-hal” library), and between eCores within the Epiphany (grouped in the “e-lib” library). Among other things, the host can load programs to individual eCores, write and read the eCores’ local memory, and interrupt them.

The “standard” model for accelerating a normal C function running on the host would be:

1) The host runs initialization code, and defines workgroups
2) The host loads kernel programs to the workgroups
3) The host sends the input data (either directly or through the shared RAM)
4) The host signals the workgroups to start
5) The coprocessor gets the input data (from shared RAM or local memory) and processes it
6) The coprocessor sends the output data (to shared RAM or local memory)
7) The coprocessor signals the end of the calculations
8) The host gets the results and continues with the execution of the main process

It is important to note that the Epiphany kernels can be written in C (although it is not always possible to achieve the best performance in that language, and some assembly code may be needed).

The “micro-kernel” is part of the host process. It is called “micro-kernel” by using the BLIS nomenclature (it is the kernel of the bigger “sgemm” function inside the generated BLAS). It is not to be confused with the “Epiphany kernel” which runs in the coprocessor.

3. Software Architecture

3.1. BLIS

BLIS is a portable software framework for instantiating high-performance BLAS-like dense linear algebra libraries with the “Epiphany kernel” which runs in the coprocessor. When invoked, it generates a new BLAS-like API that its creators made to improve the old BLAS library, but also generates the classic FORTRAN BLAS library, and allows to write custom C micro-kernels to accelerate the resulting BLAS functions. That is the use that was given on this work. A micro-kernel was written to accelerate the “sgemm” function by offloading the main calculations to the Epiphany coprocessor. When a BLAS user (may be any scientific software, or library like LAPACK, ScaLAPACK, etc.) calls the “sgemm” function, the BLIS code divides the input and output matrices conveniently and sends small predefined multiplications to be performed by the micro-kernel.

The custom micro-kernel, after performing some initialization tasks, calls the Epiphany to do the heavy part of the calculations, does some post-processing, and then returns the partial results to the bigger sgemm function.

The problem that the (BLIS-generated) sgemm should solve is: given \( A \in M_{M \times K} \), \( B \in M_{K \times N} \), \( C_{in} \in M_{M \times N} \), then calculate \( C_{out} = \alpha A \cdot B + \beta C_{in} \), possibly transposing some of the matrices, and taking into account their correct representation in memory (leading dimensions), where \( M, N \) and \( K \) are arbitrary.

3.2. A Separate Linux process

The first task of the micro-kernel\(^2\) is to initialize the communications with the Epiphany chip and reset the system (or parts of it), it defines the shared blocks of RAM, then defines the workgroups (one on this case), loads the coprocessor kernels (only one in this case), and starts the workgroups. When the coprocessor kernel finishes the calculations (possibly many “coprocessor tasks”), the micro-kernel has to free the allocated shared RAM, and close the connection to the coprocessor.

All that operations, on one hand, take a lot of time, and on the other, it was found that some of the “initialize/finalize” functions of the eSDK had technical problems when called many times by the same process (in this case the BLAS process calling the micro-kernel many times would be doing so). The solution for those problems was to place the initialization and finalization code in an entirely different process that runs as a “linux service” (in the research version is just a different process but it could be easily converted to a Linux daemon). With that solution in mind, we will now have a Host-Coprocessor shared RAM, and also a Host-Host shared RAM. They will be called the HC-RAM and HH-RAM, respectively. Of course if it was possible to use the same space for both communications some time could be saved, but that was not yet implemented on this work.

The basic scheme is this: The BLAS sgemm function calls the micro-kernel, the micro-kernel sends its input data to a predefined place in the HH-RAM (using POSIX

\(^2\) The “micro-kernel” is part of the host process. It is called “micro-kernel” by using the BLIS nomenclature (it is the kernel of the bigger “sgemm” function inside the generated BLAS). It is not to be confused with the “Epiphany kernel” which runs in the coprocessor.

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Shared Memory tools) and passes the control to the “service process” (with a semaphore). The service process has already initialized all the necessary structures, has established communication with the coprocessor, and loaded the kernel, which is waiting for a signal to start processing. It gets the data from the HH-RAM, and runs the “sgemm inner micro-kernel” that is explained below.

### 3.3. sgemm inner micro-kernel

The process of calculation of the micro-kernel is as follows. The input matrices \((a1, b1)\) are divided in blocks of \(K_{SUB}\) columns and rows respectively (they are divided in the “k dimension”). The main loop iterates on those blocks, sending one \((m \times K_{SUB})\)-size block from input \(a1\), and one \((K_{SUB} \times n)\)-size block from input \(b1\) on each iteration (see figure 2). Those input blocks for an “Epiphany Task” will be called \(a_{i_1}\) and \(b_{i_1}\), respectively. The “Epiphany Task” takes care of performing the outer product of each column of \(a_{i_1}\) with each row of \(b_{i_1}\) that the micro-kernel has sent, and it performs a partial sum of those products. The result is the partial result matrix (for task \(i\)): \(c_{i_1}\). Each of those \(K_{SUB}\) partial results (that are \((m \times n)\) in size) can then be summed by the (host) sgemm inner micro-kernel, or can be accumulated in the coprocessor local memory, depending on the implementation (see figure 2). After that, the micro-kernel multiplies the resulting matrix by \(\alpha\) and adds \(\beta \cdot c_{in}\), to produce the sgemm micro-kernel final result. It stores it in the HH-RAM and signals the main process (sgemm outer micro-kernel) that the calculation is done.

The data exchange between host and co-processor is done via the shared RAM (HC-RAM). The process of sending the inputs is interleaved with the Epiphany Task (while the task is executing on the co-processor the host is sending the next \(K_{SUB}\)-block to the HC-RAM). To achieve that interleaving there are two buffers reserved for each input block, and a shared control variable (“selector”) that tells the co-processor in which buffer the input is, for the current iteration.

There is another shared control variable (“command”) that tells the coprocessor what to do in the current iteration:

- **command = 0** Clear the inner buffers (initialization) and proceed with one Epiphany Task. Don’t send the results back.
- **command = 1** Proceed with one Epiphany Task. Don’t clear buffers, or send results.
- **command = 2** Proceed with one Epiphany Task and send the results back. Don’t clear buffers.
- **command = 3** “There will be a unique iteration”: Clear the buffers, do one Epiphany Task, and send the results back.

Using the “command” variable, the host micro-kernel can tell the coprocessor to do the initialization steps only once, then accumulate the results of many \(K_{SUB}\)-blocks, and in the last iteration send the final result back. Thus a lot of time is saved (most importantly the time needed to “send the results back”). When that scheme is used, the algorithm will be called “An Accumulator”, and it reduces the output times and postprocessing ratio (or) to near zero as \(K\) is made larger. The disadvantage of accumulating is that the results (of \(m \times n\) size) must be stored fully in the local memory, and that limits the maximum possible size of \(m\) and \(n\). \(m\) and/or \(n\) increases are needed to reduce the...
input time ratio \((ir)\). So, a clear compromise exists between improving the \(or\) and the \(ir\) ratios.

### 3.4. Epiphany kernel

Due to the memory restrictions it is very important to organize the code and buffers in the local memory. In figure 3 it is shown the local memory map, for one core, in this implementation.

![Figure 3. Local memory mapping for one core. A and B are the inputs. RES2 is a buffer to store the entire result part that corresponds to this core, and is also used as one of the temporary communications buffers in the “K Iteration”, while RES1 is used as the other temporary communications buffer. The stack and some control variables have a reserved region. The first bank is used by the kernel’s code.](image)

#### 3.4.1. Epiphany Task.
The outer layer of the Epiphany kernel will be called an “Epiphany Task”\(^3\). Again, the algorithm is “SUMMA-like”\(^4\). The input is divided between the cores in blocks of \((m \times \text{CORES} \times n)\) size for \(a_{ti}\) and \((K\text{SUB} \times \text{CORES} \times n)\) size for \(b_{ti}\) (those block will be called \(a_{ti-cj}\) and \(b_{ti-cj}\)). Each core will calculate the corresponding outer products and sum over \(K\text{SUB} \times \text{CORES}\) of them to obtain a partial result \((c_{ti-cj})\) that, in turn, will be summed with the partial results of the other cores (resulting \(c_{ti}\)). It is important to note how this inter-core summing is achieved.

Each core is the “owner” of one part of the final matrix result, which it will store after the Epiphany Task is run. The partition could be made arbitrarily, but on this implementation it was chosen to divide the results matrix in blocks of \(n\) columns, each. That was done in order to make the reorganization of the output matrix easier (as it is stored column-major). It also allows for the “b-streaming” implementations, in which the input matrix \(a_{ti-cj}\) is totally stored in local memory, but the \(b_{ti-cj}\) input matrix is retrieved “as needed” by the coprocessor (in blocks of \(NSUB-\text{CORES}\)), as will be explained later.

In this “input storage - output storage” scheme it can be readily seen that the input needed to calculate the output results of one core lies scattered around the other cores. Usually, the solution would be to move partial input data within the cores, as moving results would be more costly, but on this case (due to some Epiphany special characteristics) the implementation moves the partial results instead. The idea is to make use of the fact that the Epiphany cores can do one “multiply-add” and one “store into another core’s memory” on the same clock cycle, so the results inter-core movement can be done “for free”, which can’t be done for the inputs. An inter-core pipeline (figure 7) was designed to move those intermediate results, as will be explained below. Resuming, the core that is responsible of a certain calculation is not necessarily responsible of the final storage of it, and the storage scheme can be chosen arbitrarily (on this implementation divided by column blocks).

![Figure 4. One Epiphany Task.](image)

#### 3.4.2. Epiphany Column Iteration.
The \(b_{ti}\) input matrix to the Epiphany Task is divided in \(\text{CORES}\) blocks of size \(K\text{SUB} \times \text{CORES}\), that correspond (ultimately) to the cores’ output storage blocks. Furthermore, each of those blocks are divided in blocks of size \(m \times NSUB\), of the final Epiphany Task result matrix. Each Epiphany Column Iteration consists of \(\text{CORES}\) “Epiphany K Iterations”, that will be described in the next subsection. On an Epiphany Column Iteration, each core calculates \(\text{CORES}\) partial results of size \(m \times NSUB\) and in the end stores a final result block of size \(m \times NSUB\) (that means that, in total, there are \(\text{CORES}\) of those final result blocks calculated). After \(\frac{m}{NSUB}\) Epiphany Column Iterations, the Epiphany Task is completed.

#### 3.4.3. Epiphany K Iteration.
On each “Epiphany Column Iteration” is divided into \(\text{CORES}\) “Epiphany K Iterations”\(^3\). Each Epiphany K Iteration a partial result block of size \(m \times NSUB\) is calculated by each core, and sent to the next core in the defined pipeline (figure 7) to be accumulated with

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3. Some definitions: \(\text{CORES}\) is the number of cores in the Epiphany chip. \(K\text{SUB}\) is the number of columns of \(a1\) and rows of \(b1\) that are sent to the Epiphany chip on each Epiphany Task. \(NSUB\) is the number of columns of one subMatmul result.
other partial results. The identity of the next core is fixed, but the position, in the final results matrix, of the block that is calculated depends on the current iteration number as much as on the id of the core that performs the calculation.

On every K Iteration, a partial block (corresponding to a partial sum of blocks in the current “Column Iteration” position), that will ultimately end in the core number $(ownCoreid - iter_k - 1) \mod (CORES)$, is sent to the next core. Thus, after CORES iterations every core has its own results block.

As an example, on iteration zero, core 0, calculates one partial block corresponding to core 15, and sends it to core 1. On iteration two it will calculate a block corresponding to core 14 and sends it to core 1, and so on. On iteration $CORES - 1$, it calculates a partial block corresponding to core 1, and sends it to core 1, and in the final iteration it calculates its own corresponding block and sends it to a different destination depending on the value of the “command” variable. If the command asks to send the results out, it will copy them to the HC-RAM. Otherwise, if the results are to be accumulated, core 0 sends its results to core 1 as in previous iterations (when new input data arrives this will correctly accumulate the new results with the old).

For sending and receiving the partial results, two buffers are defined and are interchanged on even and odd K iterations. One of the buffers has a size to hold the entire final result $(m \times n)$, but is used, on each Epiphany Column Iteration, in blocks of size $m \times NSUB$ (it doesn’t change in the K Iterations loop). There is a second, fixed, buffer of size $m \times NSUB$. On each K Iteration, one of the buffers is the holder of the “previous accumulated result” and the other is used to store the current result (in the next core). The initial buffer is defined so that in the last K Iteration the results are in the (big, final results) RES2 buffer. Before and after every K Iteration a barrier is used to synchronize the cores.

3.4.4. subMatmul. The function “subMatmul” could be thought as “the single-core version of the Epiphany K Iteration”. It is just a single-core matrix-matrix multiplication function, that accepts inputs of size $m \times KSUB \times CORES$ for $a$, and $KSUB \times n$ for $b$, and outputs the resultant $m \times NSUB$ product matrix. This function was initially implemented in C language, but as it became clear that it was the critical function in the kernel, it was then implemented in assembly language. The implementation was strongly based on that of the previous work [6], which achieved on-chip performances close to 85% of the peak. That implementation is based on a macro “doMult” that basically multiplies one scalar with an array of size 32. It makes use of the Epiphany core’s special features to achieve great performances (see section VII of [6] for details).
The assembly version has fixed input and output sizes: \( a \in M_{192 \times 4}, b \in M_{4 \times 4}, C_{in}, C_{out} \in M_{192 \times 4} \). The previous result and next result pointers, are passed as parameters. In this implementation the doMult macro was repeated 4 times (as matrices are of size 4 in the “k” dimension), which means that the partial results will be accumulated 4 times in the internal registers, before sending them back to memory. As the length of one “doMult result vector“ is 32, a loop that repeats the process 6 times was necessary, to calculate a complete 192 column. After that inner loop, another outer loop iterates on the \( (NSUB = 4) \) b columns and repeats the process.

![Figure 8. Scheme of the subMatmul function.](image)

4. Results

4.1. Custom Tests

All the processing times (in these tests) were measured in the host side with functions from the “time.h” C library. In the case of the kernel called from the same OS process, the times where measured with the “clock()” function. In the case of the kernel called from a different process (which is the actual implementation that was compiled for BLIS), the times are measured with calls to `clock_gettime(CLOCK_MONOTONIC,&time)`. That was necessary because the “clock()” function would give results only for the main process. The results of both measurements can be seen in tables 1 and 2.

4.2. BLIS Tests

After the “custom” tests, the BLIS (and BLAS) library was compiled with the micro-kernel, and the BLIS standard tests were run. The micro-kernel used is the one that calls a different OS process to calculate the results. As can be seen in table 3 the results are very similar to those of the “custom” tests.

In table 4 the tests (from the “BLIS testsuite”) for the whole sgemm function, are shown with \( m = n = K = 4096 \). It can be seen that the performance penalty, with respect to the kernel performance, is not too big.

As the version of the HPL Linpack Benchmark code that was readily available to the author was intended for use with Double Precision, and with the goal of making a first test, that would further establish the correctness and robustness of the solution, a “dgemm” kernel was implemented, for the BLIS framework which, in fact, sends the data to the “sgemm inner kernel” to do the calculations (downcasting the inputs, and upcasting the outputs). The precision of the results is, therefore, expected to be close to that of Single Precision. It was a workaround to be able to reuse the already available HPL code. In the process, some performance was lost, as can be seen in table 5 That version was called the “false dgemm”.

In table 6 the results for the whole “false dgemm” function are shown.

### Table 1. Custom Tests results for the sgemm kernel called from the same process \((m=192, n=256, K=4096)\).

| Description                                      | Time (s) | %  | GFLOPS/s |
|--------------------------------------------------|----------|----|----------|
| Host reference code                              | 3.778169 | 100| 0.107    |
| Input loading and host preprocessing (*)         | 0.094648 | 82.9| -        |
| Coprocessor work (*)                             | 0.105652 | 92.6| -        |
| Host data retrieving and post-processing         | 0.005272 | 4.6| -        |
| Total sgemm µ-kernel                             | 0.114114 | 100| 3.529    |
| Mean Relative Error                              |          |    | 8.73e-08 |
| Maximum Relative Error                           |          |    | 5.83e-07 |

(*) Input loading and coprocessor work are done in parallel, which explains that the sum of the percentage column, for the sgemm µ-kernel, is larger than 100

### Table 2. Custom Tests results for the sgemm kernel called from a different process \((m=192, n=256, K=4096)\).

| Description                                      | Time (s) | %  | GFLOPS/s |
|--------------------------------------------------|----------|----|----------|
| Host reference code                              | 3.776418 | 100| 0.107    |
| Total sgemm µ-kernel                             | 0.158303 | 100| 2.543    |
| Mean Relative Error                              |          |    | 8.73e-08 |
| Maximum Relative Error                           |          |    | 5.83e-07 |

### Table 3. BLIS SGEMM kernel results \((m=192, n=256, K=4096)\).

| blis_<dt><op>_<params>_<stor> | GFLOPS | residue |
|--------------------------------|--------|---------|
| blis_dgemm_nn_ccc              | 2.630  | 1.18e-07 |

In table 4 the tests (from the “BLIS testsuite”) for the whole sgemm function, are shown with \( m = n = K = 4096 \). It can be seen that the performance penalty, with respect to the kernel performance, is not too big.

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4.3. HPL Linpack Tests

Finally, the High Performance Linpack Benchmark [12] was run with the parameters and results specified in table 7. It was run with a process grid of $1 \times 1$, in one node.

The results of the HPL benchmark showed that the sgemm implementation works correctly, up to Single Precision, but the performance is far lower than the one for the sgemm operation alone. The lower performance could be explained as due to a poor choice of algorithm parameters for the benchmark, or by the influence of the other BLAS functions that are called, in particular the Level-2 BLAS operations. Those Level-2 operations should not account for most of the computations, but if their performance is very low, compared to the Level-3 operations, they could be the limiting factor.

5. Conclusion and Future Work

An Epiphany accelerated, complete BLAS library was instantiated by the use of the BLIS framework. The performance of the Matrix-Matrix multiplication kernel achieved was better than in any other implementation before (as to the author’s knowledge), when program loading and initialization are not taken into account (which is the standard in previous work [6] [7] [8]). When trying to get a more practical kernel, to be used as a Linux service, the performance gets lower, due to the interprocess communication (which could, most likely, be improved), but gives still an interesting result for a first BLAS implementation. The results for the High Performance Linpack are far lower than expected, given the sgemm results. That may be explained due to a poor choice of algorithm parameters or to the low performance limiting factor.

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5.1. A “b-streaming” Solution

One way to improve the \( ir \) ratio would be to use a solution in which the values of \( B \) are only copied to the local memory as needed. That solution could make use of more free space for the input \( A \).

5.2. An “output-streaming” Solution

If the output is not entirely stored locally, it is possible to use bigger values for \( m \) and \( n \). In that kind of solutions, though, it is not possible to accumulate results for more than one \( KSUB \) block, in the coprocessor. The shrinking of \( RES2 \), makes some more space available for the input \( A \). Also it is possible to increase the value of \( m \) by reducing the value of \( KSUB \), but if that is done one has to make more partial results sums in the host. This idea was implemented in a previous version. Initially the idea was that summing two buffers that are stored in RAM memory would be fast enough for the host. Regrettably the access, by the host, to the shared portion of the RAM memory (HC-RAM) was very slow (at the moment it is accessed by the eSDK “\( e\_read \)” function), thus limiting that kind of improvements (bigger \( m,n \) means better \( ir \) ratio). It is very possible that a faster way to read from that region of the external memory exists, in which case the “output-streaming” solution could achieve better performance. It was found that it was possible to access the shared memory region with a normal C pointer, but the performance results were even worse than when using the standard “eSDK” function call. Therefore, as the access to other portions of the RAM (non-shared) is very fast, it is assumed that there is a penalty due to the hardware configuration or FPGA implementation for the shared-RAM access. The “output-streaming” implementation was what the author originally had in mind when implementing the “SUMMA-like” algorithm.

A possible memory map for that solution would be as in figure 9.

![Figure 9. Possible local memory mapping for one core in the “Output-streaming” solution. A and B are the inputs (B is not completely stored in local memory). RES1 and RES2 are used as temporary results buffers. The stack and some control variables have a reserved region. The first bank is used by the kernel’s code.](image.png)

5.3. NEON or FPGA acceleration

For both, the level-2 BLAS operations and the summing of partial results by the Epiphany, the NEON SIMD engine in the ARM host or the FPGA in the Zynq could be used.

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References

[1] A. Olofsson, T. Nordström, and Z. UI-Abdin, “Kickstarting high-performance energy-efficient manycore architectures with epiphany,” arXiv, no. 1412.5538, Dec 2014.
[2] Parallella-1.x Reference Manual, Adapteva, Inc., rev 14.09.09.
[3] F. G. Van Zee and R. A. van de Geijn, “BLIS: A framework for rapidly instantiating BLAS functionality,” ACM Transactions on Mathematical Software, vol. 41, no. 3, pp. 14:1–14:33, 2015. [Online]. Available: http://doi.acm.org/10.1145/2764454
[4] R. A. van de Geijn and J. Watts, “Summa: Scalable universal matrix multiplication algorithm,” Austin, TX, USA, Tech. Rep., 1995.
[5] L. E. Cannon, “A cellular computer to implement the kalman filter algorithm,” Ph.D. dissertation, Bozeman, MT, USA, 1969, aAT7010025.
[6] A. Varghese, B. Edwards, G. Mitra, and A. P. Rendell, “Programming the adapteva epiphany 64-core network-on-chip coprocessor,” in Proceedings of the 28th International Parallel & Distributed Processing, Phoenix, USA, May19–23, 2014, pp. 984–992.
[7] Y. Sapir, “Scalable multiplication of big matrices,” Adapteva, Inc., Tech. Rep., 2012.
[8] J. A. Ross, D. A. Richie, S. J. Park, and D. R. Shires, “Parallel programming model for the epiphany many-core coprocessor using threaded MPI,” arXiv, no. 1506.05442, 2015.
[9] Zyqn 7000 documentation. [Online]. Available: http://www.xilinx.com/products/silicon-devices/soc/zyqn-7000.html#documentation
[10] Epiphany Architecture Reference, Adapteva, Inc., 2013, rev 14.03.11.
[11] Epiphany SDK Reference, Adapteva, Inc., 2013, rev 5.13.09.10.
[12] Netlib’s high-performance linpack benchmark (HPL). [Online]. Available: http://www.netlib.org/benchmark/hpl
[13] Parallella community forum. [Online]. Available: http://www.parallella.org/forums

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