On hyperbolic laws of capacitor discharge through self-timed digital loads

Alexandre Yakovlev1,*†, Alexander Kushnerov2, Andrey Mokhov1 and Reza Ramezani1

1School of Electrical and Electronic Engineering, Newcastle University, Newcastle upon Tyne, NE1 7RU, UK
2Department of Electrical and Computer Engineering, Ben-Gurion University of the Negev, Beersheba, Israel

SUMMARY

A new model to predict the dynamic behavior of a self-timed autonomous digital system powered by a capacitor is derived. The model demonstrates the hyperbolic shape of the discharging process on the capacitor. It allows a symbolic analysis of the discharging process for complex digital loads comprised of series (stack) and parallel configurations of digital circuits. For example, for a stack configuration, important non-trivial relationships between the hyperbolic discharging rates have been derived based on the knowledge of the velocity saturation index (alpha) of the semiconductor devices used in the digital part. For a realistic (modern complementary metal oxide semiconductor (CMOS) devices) value of alpha = 1.5, the discharging process for a stack of two identical circuits proceeds nearly three times slower than that of any of the stand-alone circuits. This shows a potential way of extending the lifetime of the energy sources by means of stacking self-timed circuits. Although the analysis is based on configurations consisting of ring oscillators in CMOS technology, the analysis method can be extended to other types of self-timed systems and other semiconductor technologies in which the instantaneous switching activity of the digital load is determined by the instantaneous voltage levels provided by the capacitive power transfer mechanism. The analytical derivations have been validated by simulations and experiments carried out with real hardware. © 2014 The Authors. International Journal of Circuit Theory and Applications published by John Wiley & Sons, Ltd.

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1. INTRODUCTION

The paper investigates the dynamic behavior of a circuit consisting of a rechargeable energy storage element and an active digital load, which consumes power from the storage element. In its simplest form, such a circuit consists of a capacitor and a ring oscillator. The importance of this study comes from the fact that such a circuit will form a core component in emerging autonomous electronic systems such as nodes in wireless sensor networks (WSNs) and internet of things (IoT). These nodes will be less reliant on batteries only and will increasingly employ energy-harvesting sources. The reason for that is that replacing batteries in such applications is either costly or impossible. Consider, for example, a network of sensors embedded in the concrete of road to measure traffic. Another example is a set of sensors that must extract power from a surrounding energy field and report measurements of selected field points to a central monitor. Such sensors have to be self-powered, and preferably self-timed, that is, not dependent on the external clock signal but rather deriving their own timing conditions based on the instantaneous levels of power [1]. When energy supply is

*Correspondence to: Alexandre Yakovlev, School of Electrical and Electronic Engineering, Newcastle University, Newcastle upon Tyne, NE1 7RU, UK.
†E-mail: alex.yakovlev@newcastle.ac.uk

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prohibitively sporadic and intermittent, the system cannot afford having power regulators, which incur overheads [2]. Therefore, it is important to investigate the ways of designing systems in which the power source is simply a capacitor whose charge can drive some digital logic directly, without any special regulation. Studying such combinations, a capacitor and switching logic powered by it, is however an entirely novel subject that is not covered in any textbook on circuit theory. Typically textbooks either talk about resistor–capacitor (RC) circuits or at best switching capacitors with external fixed frequency clocking [3, 4].

The first discovery on this path was made recently in [5, 6]. Paper [5] presented a self-powered voltage sensor based on charge to code converter, using a sampling capacitor and a self-timed counter whose operation was powered by the capacitor. The code produced by the counter was thus proportional to the charge stored in the capacitor and hence to the input voltage. It was observed that the discharging process in this configuration did not accord with the classical rules of linear RC circuits. It was following a non-linear process, which looked more like a hyperbola. Later in [6], the same authors investigated this process analytically, by considering the simplest possible configuration—a capacitor and a ring oscillator, presented in Figure 1(a). They derived close formula expressions proving, indeed, the hyperbolic character of the discharging process. The main difference between classical exponential and hyperbolic processes is that in the exponential process, the amplitude of the capacitor’s voltage does not determine the time step, which is completely defined by the time constant, that is, the capacitance and resistance of the load.

In the hyperbolic case, the time step is not constant; it varies with the voltage, and this has the effect of non-linear (or time varying) resistance. Figure 1(b) shows that the frequency of oscillation of the inverter ring lowers with time. This fact is associated with the dependence of the delay of an inverter on the supply voltage. The delay, in turn, is different for superthreshold and subthreshold modes. Thus, another result of [6] was that the exact law of hyperbola in the discharging process depends on whether the circuit operates in the superthreshold or subthreshold mode. It was found that in the strong superthreshold mode, that is, where $V_{dd} \gg V_t$, the hyperbolic law of the capacitor voltage is very close to $V(t) = 1/(wt + 1)$, where $w$ is the discharge rate (denoted by $a$ in [6]). This law is obtained for the case of the parameter $\alpha$, the velocity saturation index [7], being equal to 2 (for Shockley model), which is of course a bit of exaggeration because for metal oxide semiconductor field effect transistors (MOSFETs) this parameter is typically less than 1.5 and for recent short-channel MOSFETs even

![Figure 1](image_url)
closer to 1.3 [8]. Nevertheless, this simplification is fairly convenient because it corresponds to the ‘rule of thumb’ linear relationship between the supply voltage and the frequency of digital circuitry powered by this voltage (in strong superthreshold mode). The important result of discovering the hyperbolic rule of discharge is that the predictions of energy decay based on constant impedance of the load would be highly inaccurate and will be inappropriate for autonomous systems powered by a capacitor.

This paper will build on the previous knowledge from [5, 6] and investigate ways of designing systems based on the hyperbolic laws. In particular, the paper investigates compositional techniques for modeling digital switching loads and thus paves the way toward the modular construction of self-timed circuits with capacitive power transfer. For example, with the equivalents of series and parallel connections of digital loads, it will be possible to perform a simple circuit analysis and predict the parameters of the dynamic behavior of circuits built out of subcircuits.

The core of our investigation is the mathematical derivation of the effective discharge rate for the composite system from the discharge rates of the constituents in the case of series and parallel connections. This derivation builds on the hypothesis about the possibility of applying Kirchhoff’s laws to series and parallel connections of digital loads. According to our derived formula, for example, for the series connection, the rate of discharging a capacitor (i.e. the rate of fall of the hyperbola) can be slowed down three to four times for the case of stacking two identical ring oscillators, compared with the rate of a single oscillator.

Once the formulas for the effective discharge rate are obtained, a validation of this hypothesis is performed at three different levels. Firstly, we consider a simple theoretical model of switched capacitors and charge distribution and identify potential sources of error in applying the theoretical formulas. Secondly, we perform behavioral simulation experiments using a convenient simulation environment in which we use switched capacitors and voltage-controlled oscillators (VCOs) to mimic the behavior of the studied configurations. These simulations show that our theoretical hypothesis and predictions come fairly close to the simulated results for the basic case of $\alpha = 2$. Finally, we stage a real physical experiment by building circuits consisting of a capacitor and ring oscillators made of discrete elements. These experiments clearly show the correctness of our predictions and moreover demonstrate that our theoretical hypothesis and predictions hold for $\alpha = 1.5$, which is a realistic value for the complementary metal oxide semiconductor (CMOS) technology at the level of small to medium scale integration. The main contributions of this paper can be summarized as follows:

- A generalized hyperbolic model of the process of discharging a capacitor through a self-timed switching load in the form of a ring oscillator that may be applied to a range of CMOS technologies (for arbitrary $\alpha$);
- Theoretical expressions for deriving the effective discharge rates for series and parallel connections;
- Theoretical, simulation and physical experimental validation of the derived hyperbolic discharge rates.

There are at least two main reasons why the knowledge of our new model is important. Firstly, equipped with such a technique, it would be possible to avoid lengthy simulation processes when studying scaling of the performance and power of complex hybrid systems, consisting of capacitors and digital switching components. The practical significance of these results is hard to predict now, but one important practical implication of this study is an effective way of prolonging the discharge rate and hence extending the life of the energy source by using the series (stacking) connection of self-timed digital loads. It is well known that CMOS logic is fundamentally fast, which may not always be a good thing (because it computes and uses energy very quickly!) for some new applications in the area of IoT. The only way to slow it down is by putting CMOS circuits in low-voltage conditions. Stacking circuits in series and forcing them to share the charge from the source is what helps to last their computing activity for much longer. Our paper provides an appropriate theoretical underpinning behind such stacking.

Secondly, studying circuits that exhibit hyperbolic decay in such a simple analog form, without resorting to complex numerical methods, will help address the needs of many applications in biology, economics, psychology and other fields that need hyperbolic decay models. For example, we can envisage a development of a programmable analog-digital fabric that could simulate massively parallel behavior of individuals whose material or other interests are subject to hyperbolic depreciation laws [9].
2. BACKGROUND: ANALYSIS OF RING OSCILLATOR

We first recall the model used in [6] to describe the ring oscillator shown in Figure 1(a). Switching activity in any digital circuit, built from CMOS gates, connected to an energy source is in fact a process of charging and discharging its parasitic capacitances through p-type metal-oxide-semiconductor (PMOS) and n-type metal-oxide-semiconductor (NMOS) transistors respectively. In a simple ring oscillator, consisting of odd number of inverters \( N \), each inverter receives the output of the previous inverter being flipped. Accordingly, the current inverter makes a transition from low to high or from high to low as shown in Figure 2(a).

Let us denote the sum of the capacitance of the drain diffusion of PMOS and NMOS and the capacitance of the wires and the fan-out gates as an equivalent (parasitic) capacitor \( C_p \), attached at the output of each inverter [10]. During the transition from low to high, the PMOS is on and NMOS is off, so \( C_p \) is charged from the main supply. This constitutes the major part of energy consumption in the inverter. In the opposite way, a high to low transition discharges \( C_p \). At this state, the energy, which was taken from the main supply before, is discharged through NMOS. Obviously, what is described here is a simplification of the actual processes in the circuit where the acts of switching of adjacent inverters and hence charging and discharging of the parasitic capacitors partly overlap. We also prefer to ignore some aspects of circuit behavior here, such as short-circuit effects, to enable us to use simple first-order analytic approximations of the system that already has non-linear effects, which we focus upon in this work. The operation of the ring oscillator can be explained in three states, shown in Figure 2(b).

Configuration ① represents the circuit state when no charging or discharging action takes place. Thus, it is the situation when \( C \) is connected to the ring oscillator, but no switching action has been fired. Every other (say, odd numbered) inverter output is at logical ‘1’, that is, the corresponding capacitor \( C_p \) is charged to the voltage level equal to that of \( C \). The remaining inverter outputs are at logical ‘0’, and their capacitors \( C_p \) are empty. This state also describes the circuit status between two successive switching events. The system is in state ② when a switching occurs. One of the charged capacitors \( C_p \) (of the inverter that is supposed to switch from 1 to 0) is gradually discharged. There is no energy transfer from the source capacitor during this state. In state ③, the discharged capacitor

![Figure 2. Charge switching: transistor switching (a), and the circuit state at dynamic switching (b), where \( N \) is the number of inverters.](image-url)
associated with the next inverter in the ring (which is supposed to switch from 0 to 1) starts receiving charge from the source capacitor. This is the only state that draws energy from the source capacitor. Note that, in real operation, an overlap exists between states ② and ③; however, to simplify the analysis, we consider them as distinct states.

If we step up one level of abstraction, above the exponentials involved at each state of charging and discharging the current parasitic cap, we can concentrate only on the charge division at each step, which we call the $V$ drop. The timing aspect, that is, the propagation delay involved in the charging and discharging state, can be considered separately. The $V$ drop in this circuit can be found by the law of conservation of charge (refer to [11]), which redistributes between the capacitors $C_T = C + C_i$ and $C_p$ according to their capacitances. At the $i$th step, charge equilibrium occurs at

$$V_{i+1} = KV_i = K^iV_0$$  \hspace{1cm} (1)

where

$$K = \frac{C_T}{C_T + C_p}$$  \hspace{1cm} (2)

is the coefficient of decaying voltage at each switching action (or ‘charge division coefficient’). Because $C_T \gg C_p$, $K$ is only slightly less than one. Thus, the switching index $i$ determines the voltage at each step. This process is shown in Figure 3, where for the sake of better illustrating the effect of charge division, we exaggerate the ratio so that $K$ is much smaller than one. Let us now consider the delay of such steps. The propagation delay of an inverter is a function of supply voltage, which determines the behavior of its NMOS and PMOS transistors. For operation above the transistor threshold (superthreshold region), the time of switching (propagation delay) is approximately reciprocal to $V$, for $\alpha = 2$.

However, below threshold (subthreshold region), the propagation delay becomes a more complex function of $V$. The following is a model for the propagation delay of a single inverter proposed in [12]:

$$t_d = \begin{cases} 
  t_{\text{sup-th}} = \frac{pC_pV}{(V - V_i)\alpha} & V > V_i \\
  t_{\text{sub-th}} = \frac{pC_pV}{I_0e^{\frac{V}{N_s}}} & 0 < V \leq V_i 
\end{cases}$$  \hspace{1cm} (3)

where $p$ is the fitting parameter, $\alpha$ is the velocity saturation index, $I_0$ is the drain current at $V_{gs} = V_t$, and $N_s = m kT/q$ ($m$ is the subthreshold slope factor, $1/N_s \approx 28$) [7]. The overall elapsed time at step $i$ is conveniently represented by the sum of the individual propagation delays of the steps. Thus, the physical time $t$ is also determined by the increments of the switching index. The solution for the discharging process in the distinctive superthreshold

Figure 3. $V$ drop over time.
region, under the assumption of $\alpha=2$, was derived (using a geometric series sum technique, inspired by [11]) in [6]

$$V_N = \frac{AK}{(1-K)t + AK} = \frac{1}{wt + 1}$$

(4)

where

$$A = 2pC_p \quad \text{and} \quad w = \frac{1-K}{AK}$$

(5)

Voltage $V_N$ in Equation (4) is normalized to the initial voltage of the capacitor at time 0. Parameter $\alpha$ is strongly technology dependent, and in modern technologies, it scales down to $\alpha=1.5$ or even 1.3 [8]. As a result, the actual hyperbola changes according to $\alpha$ and can be generalized as:

$$V_N = \frac{1}{(wt + 1)^{1/(\alpha-1)}}$$

(6)

where

$$w = \frac{1-K^{\alpha-1}}{AK^{\alpha-1}}$$

(7)

It is clear that with a smaller value of $\alpha$, the rate of the voltage drop is reduced. However, because of the changed inverse power law in Equation (6), the discharging process may go faster. In near-threshold and subthreshold region, the character of the discharging process is fairly complicated because of the exponential increase of the delay as voltage drops, and this significantly reduces the rate of the voltage drop as a result of logic switching. Eventually, the switching process stops. The remaining charge decay is mainly determined by the leakage current.

We should, again, remark on the idealized picture of the discharge process described above, where we assume that the energy of the main capacitor is spent only on switching actions associated with the parasitic capacitances of the inverters. We ignore here many effects inherent in modern (submicron) semiconductor devices, such as temporary short-circuit state between PMOS and NMOS transistors. This state is certainly more pronounced as the voltage lowers and becomes near threshold; in which case, other static leakage components contribute to the capacitor discharging process. These partially active and partially passive resistive elements should be considered if one builds a more general model, but the complexity of such a model would rise considerably, and developing such a model is outside the scope of this paper. An interested reader could refer to paper [6], where they can find the comparison of a more accurate hyperbolic analytical model and the results of Cadence/Spice simulations for a ring oscillator built at the 180-nm technology node.

3. COMPOSITIONAL METHOD

In the following, we will assume that we operate in a distinctive superthreshold mode, where we can use the hyperbolic characteristic of Equations (4) or (6). Also, we will initially take $\alpha=2$ for simplicity, although the analysis is then generalized to the case of arbitrary $\alpha$ in a straightforward way. (As shown in the experimental section, for the used ICs, we evidently have $\alpha=1.5$). Let us consider the entire digital circuit as a one-port and derive the differential equation for the voltage given by Equation (4):

$$\frac{dV}{dt} = \frac{-w}{(wt + 1)^2} = -wV^2$$

(8)

Besides, we can write
\[ i_C(t) = -C \frac{dV_C}{dt} = \frac{wC}{(wt + 1)^2} = wCV_C^2 \]  \hspace{1cm} (9)

This is a non-linear differential equation, which can be compared by analogy to the linear equation, which would describe the process of discharging a capacitor through a constant resistor \( R \), namely \( \dot{V} = -wV \), where \( w = 1/(RC) \). By analogy, the coefficient \( w \) can be regarded as a rate of the voltage fall. The value of \( -C \cdot V \) defines the discharging current \( i \) in both linear and non-linear cases. Hence, in the non-linear case for the current flowing through the switching circuit, we can write \( i = wCV^2 \), which effectively means that the circuit can be emulated by either non-linear or time-varying resistor [13]:

\[ R(V) = \frac{1}{wCV} \quad \text{or} \quad R(t) = \frac{wt + 1}{wC} \]  \hspace{1cm} (10)

It is possible to eliminate the dependence of the time-varying resistor on \( C \). Indeed, because of Equation (5), we can express

\[ w = \frac{1 - K}{AK} = \frac{1}{2pC_T} \]  \hspace{1cm} (11)

which is under a fairly reasonable assumption that \( C_T \approx C \) yields \( w \approx 1/2p \), such that Equation (10) becomes dependent on the fitting parameter \( p \)

\[ R(V) \approx \frac{2p}{V} \quad \text{or} \quad R(t) \approx \frac{2p(wt + 1)}{wC} \]  \hspace{1cm} (12)

Equation (8) can be generalized, to adhere to Equation (4), for arbitrary \( \alpha \) as

\[ \frac{dV}{dt} = -wV^\alpha \]  \hspace{1cm} (13)

Naturally, at this point, we would like to investigate the behavior of such circuits when they are configured in series (called here ‘stacking’) and parallel. Refer to Figure 4 for illustration. Our investigation will proceed through several stages. We first explore two hypotheses about stack and parallel configurations based on the use of voltage and current Kirchhoff’s laws (KVL and KCL respectively). Using these laws, we will derive the equivalent value for the voltage drop rate \( w \) for the stack and parallel configurations of the ring oscillators as a function of the individual drop rates \( w_1 \) and \( w_2 \) of the two stand-alone circuits. After that, we will verify our hypothesis about the results of the application of KVL and KCL by analyzing the behavior of the series and parallel configurations.

![Figure 4. Basic connections of one-ports: stand-alone circuits, series (stack) and parallel configurations.](image-url)
against the stand-alone circuit. This analysis will be based on examining the effect of a switching inverter on the corresponding capacitor switching and charge sharing. After that, in the two subsequent sections, we will validate our analysis by simulations and physical experiments with real circuits.

Let us assume for the stack case that the circuit obeys KVL and KCL:

\[
\begin{align*}
V &= V_1 + V_2 \\
i_C &= i_{C1} = i_{C2}
\end{align*}
\]  

(14)

or

\[
\begin{align*}
\frac{dV}{dt} &= \frac{C_1}{C} \frac{dV_1}{dt} + \frac{C_2}{C} \frac{dV_2}{dt}
\end{align*}
\]  

(15)

which for \(C = C_1 = C_2\) is reduced to

\[
\begin{align*}
V &= V_1 + V_2 \\
wV^a &= w_1 V_1^a = w_2 V_2^a
\end{align*}
\]  

(16)

Let us express \(V_1\) and \(V_2\) by \(V\)

\[
\begin{align*}
V_1 &= \left(\frac{w}{w_1}\right)^\alpha V \\
V_2 &= \left(\frac{w}{w_2}\right)^\alpha V
\end{align*}
\]  

(17)

Because \(V = V_1 + V_2\), we can write

\[
V = \left(\frac{w}{w_1}\right)^\alpha V + \left(\frac{w}{w_2}\right)^\alpha V
\]  

(18)

By eliminating \(V\) and rearranging the terms between the left and right hand sides, we will have

\[
\left(1 + \frac{1}{w} \right)^\frac{1}{2} = \left(1 + \frac{1}{w_1}\right)^\frac{1}{2} + \left(1 + \frac{1}{w_2}\right)^\frac{1}{2}
\]  

(19)

such that

\[
w^\alpha = \frac{w_1 w_2}{\sqrt{w_1 + w_2}}
\]  

(20)

Now, for the parallel case, we assume

\[
\begin{align*}
V &= V_1 = V_2 \\
i_C &= i_{C1} + i_{C2}
\end{align*}
\]  

(21)

or

\[
\begin{align*}
\frac{dV}{dt} &= \frac{C_1}{C} \frac{dV_1}{dt} + \frac{C_2}{C} \frac{dV_2}{dt}
\end{align*}
\]  

(22)

which for \(C = C_1 = C_2\) is reduced to
Because $V = V_1 = V_2$, we immediately can write

$$w = w_1 + w_2$$ (24)

The above shows that in the parallel case, the equivalent rate of discharge is a sum of the rates of the components, and hence, the main capacitor $C$ discharges faster. However, for the stacked case, the capacitor discharges slower. For example, for $\alpha = 2$, if we stack two identical circuits, each with a discharge rate $w_1$, then their stack will discharge the capacitor with the rate $w_1/4$, according to Equation (4).

At this point, it is however important to note the following. We apply Kirchhoff’s laws under certain ‘assumptions’. Why? Because we assume here that after we connect our initially stand-alone elements into a stack or parallel composition, the capacitive source of charge for these components in the composition remains the same as before (i.e. $C = C_1 = C_2$). Basically, this is analogous to say that in the case with RC circuits, when we connect two resistors in series or in parallel to work with the same capacitor, their composition behaves also as a resistor and that each component in the composition has the same relation to the capacitor as when they were connected to it individually. In our case, with the switching components, that is, ring oscillators, our assumptions help us to guarantee that when a component, say circuit 1, which used to be connected to the main capacitor $C$ on its own to produce the behavior described by $V_i = 1/(w_1t + 1)$, retains the same source of charge $C$ in the composition and that the parasitic capacitances of each of the component circuits share charge outside the main charge flow from $C$. Thus, with our assumption, the reliance on Kirchhoff’s laws makes our derived algebraic rules a hypothesis that requires experimental validation. Such a validation will be performed in the next section.

4. CHARGE REDISTRIBUTION STATIC ANALYSIS

In the succeeding texts, we will compare the effect of a switching inverter (i.e. charging its parasitic capacitor) in a stand-alone ring oscillator circuit with the effect of a similar switching in a stack of two (for simplicity, identical) ring oscillators. We will analyze this relationship by determining the corresponding discharge rates using equivalent capacitance equations. Thus, this analysis will either support the fact that the ratio between the discharge rates is close to 4 (for $\alpha = 2$) under some reasonable assumptions about the relative values of the capacitances involved, or disprove it. Let us first consider the case of a stand-alone oscillator. Its equivalent circuit is shown in Figure 5 and consists of the main supply capacitor $C$, the capacitor $C_1$ associated with the total sum of the charged parasitic capacitors of the inverters in the ring that have the logic value ‘1’, and the parasitic capacitor $C_p$ of the inverter that is currently being switched from logical 0 to 1.

![Figure 5. Equivalent circuit for the stand-alone circuit.](image-url)
The charge division coefficient between the initial state and the next state (when the inverter’s output has been charged) is as follows:

\[ K_o = \frac{C + C_1}{C + C_1 + C_p} \]  

(25)

The relative portion of the charge that has been transferred to the newly added inverter is

\[ 1 - K_o = \frac{C_p}{C + C_1 + C_p} \]  

(26)

This value also reflects the portion of the relative voltage drop as a result of this switching action. Let us denote \( C_1 = \gamma C \) and \( C_p = \delta C_1 \). This enables us to express the \( 1 - K_o \) characteristic in relative terms, hence

\[ 1 - K_o = \frac{\delta \gamma}{1 + \gamma + \delta \gamma} \]  

(27)

According to our findings in Section 2, this value \( 1 - K_o \) is what determines the voltage drop rate in the stand-alone circuit, which is \( w = (1 - K)/AK \).

Let us now turn to the equivalent circuit for the one-sided switching shown in Figure 6. Here, we retain the same \( C \), but instead of the single total capacitor \( C_1 \), we have two serially connected \( C_1 \) and \( C_2 \) and still the switching inverter’s capacitance \( C_p \).

Let, for simplicity, \( C_1 = C_2 \). In this case, the charge division coefficient between the initial state and the next state is

\[ K_s = \frac{C + \frac{C_1}{2}}{C + \frac{(C_1 + C_2)C_1}{2C_1 + C_p}} = \frac{(2 + \gamma)(2 + \delta)}{2(2 + \delta + \gamma + \delta \gamma)} \]  

(28)

The voltage drop portion in the stack is defined by

\[ 1 - K_s = \frac{\delta \gamma}{2(2 + \delta + \gamma + \delta \gamma)} \]  

(29)

Let us now consider the ratio

\[ \frac{1 - K_o}{1 - K_s} = 2 \left( \frac{2 + \delta + \gamma + \delta \gamma}{1 + \gamma + \delta \gamma} \right) \]  

(30)

![Figure 6. Equivalent circuit for the one-sided switching.](image)
Note, that if in Equation (30), both $\gamma \to 0$ and $\delta \to 0$ (this is a realistic assumption because $C \gg C_1$ and $C_1 \gg C_p$), then

$$\frac{1 - K_o}{1 - K_s} \to 4$$  \hspace{1cm} (31)

If $\gamma \to 0$ but $\delta = 0.1$, then Equation (30) tends to 4.2. This number closely approximates the ratio between the corresponding discharge rates $w_o$ (stand-alone) and $w_s$ (stack) because it is easy to see that under the above assumptions about $\gamma$ and $\delta$, it is true that

$$\frac{AK_o}{AK_s} \approx 1$$  \hspace{1cm} (32)

Hence, by Equations (31) and (32), $w_o/w_s \to 4$. Remember that this has been derived for $\alpha = 2$. As we saw in the preceding texts, our derivations under the assumptions of KVL and KCL also led us, thanks to Equation (20), to $w_o/w_s = 4$.

The intuitive explanation of the significant slowdown of the discharge rate in the stack case is as follows. In the stand-alone circuit, $C_p$ ‘pinches’ a portion of the charge from the charged section $C + C_1$ under the full voltage across $C$. In the stack case, $C_p$ pinches a much smaller amount of charge as a result of the effect of voltage division in the series connection of $C_1$ and $C_2$. This reduces the size of the pinch by the factor of 2. The other factor of 2 (to make it 4) is related to the fact that the propagation delay between the switching events is greater as a result of the effect of voltage division and hence the fact that the inverter delay is inversely proportional to the applied voltage.

The scenario when only one inverter is switching in the stack most of the time is quite realistic. However, one might be interested in the situation when two inverters are switching simultaneously, one in the top ring and the other in the bottom ring. This is reflected by the circuit shown in Figure 7.

Let us again derive the charge division coefficient and the corresponding voltage drop portion. Again, assuming that $C_1 = C_2$

$$K_{s2} = \frac{C + C_2}{C + \frac{C_1 + C_2}{2}} = \frac{2C + C_1}{2C + C_1 + C_p}$$  \hspace{1cm} (33)

and

$$1 - K_{s2} = \frac{C_p}{2C + C_1 + C_p} = \frac{\delta \gamma}{2 + \gamma + \delta \gamma}$$  \hspace{1cm} (34)

Figure 7. Equivalent circuit for the two-sided switching.
In this case, we are interested in the following ratio:

\[
\frac{1 - K_\alpha}{1 - K_{\alpha 2}} = \frac{2 + \gamma + \delta \gamma}{1 + \gamma + \delta \gamma}
\]  

(35)

which tends to 2 as both \(\gamma\) and \(\delta\) tend to 0.

The overall behavior of the stack is obviously a combination of the cases shown in Figures 6 and 7. We hypothesize that it is dominated by the case shown in Figure 6, where the ratio \(w_1/w_2 = 4\). Nevertheless, the scenario of Figure 7 would obviously attenuate the effect of having the ratio of 4; hence, in practice for \(\alpha = 2\), the actual slowdown ratio is likely to be less than 4. This attenuation is caused by the ‘mutual side effect’ between the top and bottom circuits on the overall charge distribution as the charge is consumed from the shared main supply \(C\) plus the stack of \(C_1\) and \(C_2\). This analysis shows that the direct application of the analysis for the composition using KVL and KCL is certainly subject to a systematic error caused by the previously mentioned mutual side effect of charge sharing.

5. BEHAVIORAL MODEL

The compositional method proposed in Section 3 has been validated by simulations in PSIM 9.0. The simulation setup is presented in Figure 8 and consists of the switched capacitor circuits discussed in Section 4, a number of VCOs, and computational block. These VCOs emulate the effect of the switching process in an idealized (refer to our comments, at the end of Section 2, about the ‘non-idealities’ of the submicron CMOS technology) ring oscillator shown earlier in Figure 2(b), where the instantaneous value of the delay between the adjacent switching actions is determined by the instantaneous value of the voltage on the parasitic capacitor (emulating the inverter that is currently switching). Each VCO consists of the controlled current source, which charges the capacitor \(C_x\) to produce a ramp voltage. When this voltage crosses the level of 0.1 V (logical ‘1’ of the first inverter), \(C_x\) is disconnected from the source and instantly discharged. This produces a short spike, which is converted into two anti-phase square waves by D flip-flop. These two complementary signals control the switches commutating the corresponding capacitor \(C_p\). The current frequency of these signals is proportional to the current value of input voltage. The computational block receives three decaying voltages as an input data and calculates five waveforms as described in the following.

For the configuration shown in Figure 8, the computational block is connected with the models of the two stand-alone one-poles circuit 1 and circuit 2, each being connected to the main capacitor \(C\), and the model of a series (stack) configuration of the identical copies of those circuits, also connected to the same capacitor \(C\). A similar simulation setup was made for studying the parallel configuration (not shown in this figure). The parameters of the circuit components in Figure 8 correspond to the parameters of the real components used in the experimental setup (Section 6), namely \(N = 23\), \(C = 10nF\), \(C_1 = C_2 = (N/2 - 1)C_{in}\), and \(C_{p1} = C_{p2} = C_{in}\), where \(C_{in} = 3.5pF\) is the input capacitance of the inverters 74LVU04. In each VCO, the gain of the voltage-controlled current source, \(G = 1\), and \(C_x = 1nF\).

Let us return to the particular case of \(\alpha = 2\), for which \(V_C\) is given by Equation (4). Because \(V_C\) can be measured in the simulation, we express the parameter \(w\) as

\[
w_{1,2}(t) = \left( \frac{1}{V_{1,2}(t)} - 1 \right) \frac{1}{t}
\]  

(36)

Substituting Equation (36) and \(\alpha = 2\) into (20), we obtain \(w_{eq}(t)\) for the stack case

\[
w_{eq}(t) = \frac{w_1(t)w_2(t)}{\left( \sqrt{w_1} + \sqrt{w_2} \right)^2}
\]  

(37)

whereas for the parallel case, \(w_{eq}(t)\) is simply

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Substituting either Equation (36) or (37) back into Equation (4), we obtain

\[ V_{eq}(t) = \frac{1}{w_{eq}(t) + 1} \]  

which is shown in Figures 9 and 11 for the stack and parallel case respectively and demonstrates an excellent agreement with the measured waveforms.

The composition formulas in Equations (37) and (38) are validated in Figures 10 and 12, where the waveforms of the discharge rates \( w(t) \) and \( w_{eq}(t) \) match each other well. (Note. We should remind that the unit of discharge rate \( w \) is assumed to be 1/s in all diagrams and tables.)

It should be noted however that these waveforms slightly deviate from the ideal constant in their initial section. This may be explained by the fact that the initial frequency of VCO is not precisely matching the actual voltage on the capacitors. The values quickly settle to constant, steady-state
parameters, which are given in Table I. These figures show that the ratio between the stand-alone and stack configurations is very close to 4.

6. EXPERIMENTAL RESULTS

The goal of this experiment was to check whether the theoretical and behavioral models of the capacitor-oscillator circuits (in their idealized forms as noted above in Section 2) and their stack and
parallel compositions would hold in physical implementations. The experiment was carried out with small scale integration components, which we believed was well suited for our purposes, as we wanted, at this stage of our research, to avoid the non-idealities caused by very large scale integration, such as reduced in-logic parasitic capacitances (down to fFs), static leakage at most voltages and transient short-cuts. One helping factor was that inverters and interconnects in small-scale integration would create sufficient parasitic capacitances to emphasize the effects we were interested in. Our main interest here was to see how stack and parallel compositions affect the effective discharge rate. A reader interested in the behavior of CMOS implementation in UMC 180-nm technology may look into [6] and see the hyperbolic decay of a stand-alone component. In the future, we are planning to fabricate both stack and parallel compositions in modern technology nodes as well.

An experimental setup, shown schematically in Figure 13, was built around the low-voltage Si-gate CMOS inverters 74LVU04 and bidirectional CMOS switches MAX4678 with an on-resistance of 1.2Ω (two in parallel). In order to remain in the superthreshold region for as long as possible, the value of $V_{in}$ was chosen to be 6 V. The supply capacitor $C=10nF$ is charged and discharged through the two switches controlled by the non-overlapping clocks $\phi_1$ and $\phi_2$ provided by the external circuit (not shown). Each cycle of $\phi_1$ and $\phi_2$ corresponds to one charging and discharging process for $C$ and the ring oscillators.

The frequency of both clocks was 10 kHz with duty cycle 20%. In all the cases, the number of the inverters in the ring oscillator is $N=23$. Figure 14 shows the voltage drop across $C$ in the stand-alone circuit and its output oscillations for a single discharging action. The former waveform plays a role of reference in the following validation of the compositional formulas in Equations (20) and (24).

Figures 15 and 16 display the measured $V_C$ and $V_o$ in the stack and parallel cases of Figure 13(a) and 13(b) respectively.

As evident, all the experimental waveforms have some bias voltage, $V_b$, such that Equation (6) should be modified as

$$V_C = \frac{V_{in} - V_b}{(wT + 1)^{1/(a-1)}} + V_b$$

(40)

Table I. Steady-state discharge rates obtained in the simulation for the stand-alone, stack and parallel circuits.

|                  | $w_1 \times 10^6$ | $w_2 \times 10^6$ | $w \times 10^6$ | $w_{eq} \times 10^6$ |
|------------------|-------------------|-------------------|-----------------|---------------------|
| Stack            | 1.739             | 1.739             | 0.4352          | 0.4348              |
| Parallel         | 1.739             | 1.739             | 3.468           | 3.478               |
Figure 13. Experimental setup for the stack (a) and parallel (b) configurations.

Figure 14. Stand-alone oscillator case. Envelope trace $V_C$, oscillating trace $V_o$, vertical scale $1\text{V/}\text{div}$, horizontal scale $10\mu\text{s/}\text{div}$.

Figure 15. Stacked oscillators case. All the voltages are referenced to ground. Top and bottom envelope traces: $V_C$ and the middle point between the oscillators respectively; top and bottom oscillating traces: $V_{o1}$ and $V_{o2}$ respectively. Vertical scale $1\text{V/}\text{div}$, Horizontal scale $10\mu\text{s/}\text{div}$. 

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Based on this expression, we have fitted the curve in Figure 14 with $w = 440 \times 10^3$ and $\alpha = 1.5$ as shown in Figure 17. Because the number of inverters is the same in both oscillators, we expect $w_1 = w_2$. Substituting this equality into Equations (20) and (24), we obtain $w = w_1/2^\alpha$ and $w = 2w_1$ for the stack and parallel case respectively (Table II). The ratio between the discharge rates of the stand-alone and stack is $400/155.6 \approx 2.83 < 3$.

The values from Table II were substituted into Equation (40) to build the hyperbolas for the stack and parallel case, which are shown in Figures 18 and 19 respectively. These experiments clearly show the correctness of our predictions and moreover demonstrate that our results hold for the value of $\alpha = 1.5$, which is a realistic value for the CMOS technology at the level of small-scale to medium-scale integration.

7. RELEVANT THEORETICAL AND PRACTICAL WORKS

The theoretical model of a digitally discharged capacitor and the technique used to derive the closed form expression in Equation (4) (from [6]), described in Section 2, bear resemblance of early works...
on charge pumps [11,14] and storage counters using pulse-switched capacitors [3, 4]. Interestingly, such a technique was first proposed about a century ago by Karapetoff in [11] and was based on the charge conservation law. The author arrived at the geometric series, which described the process of settling the output voltage (transient response) in a voltage doubler. An elegant way to obtain the same closed form expression was proposed in [3] and is cited briefly in [4]. It employs the fact that the derivative of the exponential is the exponential itself. An advanced transient analysis of charge pumps using a similar approach was presented much later in [14]. It allowed one to attain the minimum values of capacitors for a given switching frequency and vice versa. The dynamic behavior of a simple switched capacitor DC/AC converter was analyzed in [15] using the (discrete) sampled data approach. Recent studies of power transfer in microsystems with scavenged energy have mainly focused on developing models. For example, [16] presents a model for a capacitive power transfer including the bridge rectifier.

Because the switching frequency is constant, any of the approaches [16], [11,14,3, 4] leads to the exponential charging of the output capacitor. Thus, the charging is done through some (constant) equivalent resistance. The principal difference between the approaches [16], [11,14,3, 4] and the one proposed here is that in our case, the control of the switching process is not clocked externally but is generated within the system. The shape of the switching pulse is determined by the instantaneous value of the voltage on the capacitor. This aspect is brought by the needs of extracting energy for digital switching directly from the capacitive storage. On a practical side, the idea of voltage stacking to provide implicit voltage regulation and reduce supply current by the factor of 4 has been presented in [17] in the framework of 3D die stacking. This work is of course different from our study in the problems being tackled and overall context, although we thought it would be interesting to mention it here.

Figure 18. Stacked oscillators case. Top traces: measured curve (crosses) and fitted curve (boxes). Bottom trace: bias voltage.

Figure 19. Parallel oscillators case. Top traces: measured curve (crosses) and fitted curve (boxes). Bottom trace: bias voltage.
Besides the power transfer and conversion issue, the derivation presented in the paper can be considered as a contribution in studying the discrete-time systems, which are known to be connected with different non-linear phenomena [18].

8. CONCLUSION

The paper derives a model for the process of discharging a capacitor directly through a self-timed digital circuit. The model, when built for CMOS logic in its superthreshold region, shows strong hyperbolic character. The paper shows how this model can be extended to a compositional case, that is, to series and parallel configurations of digital loads. This investigation has thus an important value and originality in a circuit theoretic sense, as typically capacitors are connected either to passive components (e.g. inductors, resistors, diodes) or clock-driven active elements and hence result in typically linear analytics. The practical value of this paper can potentially be quite broad. For example, it may provide a way of predicting energy utilization in capacitive power transfer mechanisms used for digital load in WSNs and IoT applications. Another possible future application is in underpinning mathematical models of economic or biological processes that are known to exhibit hyperbolic depreciation with a simple analog–digital simulation framework, but this is a longer term goal in our research.

Further research will go into the investigation of more complex analytical models of circuits involving capacitors and CMOS digital loads. For example, the submicron effects, such as shortcuts during the transient switching of PMOS and NMOS transistors and static leakage (in above-threshold, near-threshold and subthreshold regions) could be checked as to how they may affect the discharge rates. First, we plan to carry out extensive post-layout simulations in Cadence. Secondly, we could add the above effects to the elementary step model, initially represented by Equations (1) and (2), which are currently only governed by the charge redistribution relationships. The submicron effects will add extra elements to the step model, and its solution will produce a more complex step-wise equation than Equation (1). We believe, however, that the complexity could be confined within the step-level model and we could still benefit from the elegance of the iterative construction and geometric series sum of [6], which helped us to derive Equations (4) and (6). The hyperbolic character will certainly remain in the overall process, but it will also reflect some exponential component as a result of the passive resistance associated with leakage.

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