Status of and performance estimates for QCDOC *

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QCDOC is a supercomputer designed for high scalability at a low cost per node. We discuss the status of the project and provide performance estimates for large machines obtained from cycle accurate simulation of the QCDOC ASIC.

Introduction

QCDOC\textsuperscript{1,2} was designed for a cost-effective balance between memory bandwidth, floating point performance and communication performance when running massively parallelised double precision QCD codes. As shall be seen, our simulations suggest QCDOC should scale to exceptionally large machine sizes on a fixed scientifically interesting lattice volume - or equivalently QCDOC will operate efficiently on very small local volumes. This gives the focussed compute power necessary to simulate much lighter quark masses than are accessible today, at a cost of 1 US-dollar per sustained MegaFlop.

Hardware Overview

The QCDOC design is based on an application specific integrated circuit, or ASIC. We use IBM System-On-a-Chip technology to integrate all the node logic on a single silicon chip. The CPU core is a PowerPC 440\textsuperscript{3} whose FPU\textsuperscript{4} can execute one operate instruction per clock cycle. Peak performance of two flops per clock is obtained by using fused multiply-add instructions. The on-chip features include 4MByte of embedded DRAM memory and its controller, a memory controller for off-chip DDR memory, an Ethernet interface, and a custom serial communications unit (SCU) linked by a number of on-chip busses.

The prefetching edram controller (PEC) has been custom designed by our colleagues at IBM Research, and provides ample bandwidth for the FPU. It automatically prefetches two read streams, and is multi-ported allowing remote communication to overlap local computation without contention.

The SCU hardware implements a 6 dimensional hyper-torus, with bi-directional low latency links. The aggregate 1.5GByte/s inter-node bandwidth easily supports QCD with 1 Gflop of local floating point all the way down to $2^4$ local volumes. The DMA engines in the SCU transfer complex patterns between nodes while the local floating point calculation proceeds uninterrupted.

The high dimensionality of the network both increases the communication bandwidth of the machine, and gives very symmetric local volumes when distributing the problem over very many nodes in four, or even five, dimensions. This yields the most favorable surface to volume ratio.

\*Presented by PAB at Lattice 2002, Boston.
Table 1
Performance of double precision assembler kernels produced using the speaker’s code generator. Very high fractions of the 1Gflop raw peak, and even higher fractions of the theoretical peak, are obtained. Some compiled code figures are included to show that reasonable performance can be obtained without undue pain.

| Operation            | Mflops/node |
|----------------------|-------------|
| SU3-SU3              | 800         |
| SU3-2spinor          | 780         |
| DAXPY                | 190         |
| ZAXPY                | 450         |
| DAXPY-Norm           | 350         |
| CloverTerm/asm       | 790         |
| CloverTerm/gcc       | 150         |
| CloverTerm/xlc       | 300         |

Hardware Status
The QCDOC ASIC design is functionally complete, and the preliminary design release is undergoing timing driven physical layout at IBM Raleigh. Verification is on-going with release to manufacture expected by mid fall and first silicon at the end of this year. Large prototype machines are expected in spring 2003.

Software Environment
Two widespread and standard compilers are being used, namely the IBM xlc compiler and the GNU gcc C and C++ compilers. Debug facilities are provided by a port of the full featured RISCWatch remote debug tool.

The standard runtime support libraries are a popular GNU Public License libc released by Cygnus\(^2\). Runtime libraries are available for performing communication over the physics network via the SciDac QMP interface which is in turn implemented on top of a native SCU interface.

Assembler optimised QCD kernels will be freely available.

Node kernels
The use of the PowerPC means that standard operating systems could in principle be run on the nodes. However, to scale to very small local volumes it is essential that, in addition to very low latency hardware, we avoid unnecessary software latency.

We will use a lean node kernel to avoid scheduler overhead and use the PowerPC virtual memory (VM) hardware to protect, but not translate, memory pages. This gives both the benefits of robust and graceful error recovery, and the benefits of zero-copy SCU transfers without VM gymnastics.

Host operating system
The host for QCDOC will be an SMP Unix server with multiple Gigabit links to the Boot/Diagnostic/IO Ethernet network. A multi-threaded qdaemon will boot and manage the machine partitions, and service socket-based connections to these partitions from a number of client programs. Sufficient functionality has already been implemented to boot and download code to PowerPC boards in parallel.

Performance in simulation
As part of the design verification programme a number of benchmarks and stress tests have been written, to both check functional correctness and that design goals are met. We shall present performance figures for some of these tests, where we have taken a “nominal” 500MHz CPU, and made reasonable assumptions about the interconnect wire length.

Table 2 shows a sample of common vector operations performed in Lattice QCD codes. Most

Table 2
Sample performance of red-black fermion operators in cycle accurate simulation. The Wilson and Clover kernels were generated using the speaker’s C++ code scheduler, while the Staggered operator was hand coded by Calin Cristian. The codes are very efficient even when all sites are on multiple boundaries.

| Operation            | Local Vol. | Mflops/node |
|----------------------|------------|-------------|
| Wilson $D_{eo}$      | $2^4$      | 470         |
| Wilson $D_{eo}$      | $4^4$      | 535         |
| Clover $D_{eo}$      | $2^4$      | 560         |
| Clover $D_{eo}$      | $4^4$      | 590         |
| Staggered $D_{eo}$   | $2^4$      | 370         |
| Staggered $D_{eo}$   | $2^4.4^2$  | 430         |

\(^2\)Popularised in the Cygwin software package
Figure 1. Estimated performance per node for assembly coded Wilson dslash operators as a function of local volume. Roughly two orders of magnitude better scalability is observed for QC-DOC.

Table 2 shows performance measurements of optimised implementations of various preconditioned Fermion operators in double precision. In these operators unpaired adds and multiplies set an upper limit (e.g. 780Mflops for the Wilson kernel) somewhat below the “raw” peak. The communication overhead is entirely taken into account, and the performance is excellent despite having to communicate each site over four wires in the $2^4$ case.

**Scalability**

Performance characteristics at small local volumes are critical to scaling. Figure 1 shows the estimated performance of QCDOC on double precision Wilson dslash code (omits global summation time) distributed in four dimensions. At the smallest volumes the entire operation takes roughly 20 $\mu$s, with eight communications in this time. For comparison we overlay a Myrinet Alpha 21264 cluster running single precision assembler code distributed in three dimensions.

Given the fast linear algebra and the scalable matrix multiply the remaining hurdle to be overcome by an iterative solver is global summation. The SCU has “pass-thru” hardware assist for global sums and broadcasts. The global sum has been benchmarked in simulation, and we use the mixture of matrix multiplies, linalg and gsums in the CG algorithm to predict the performance on large machines on Wilson HMC in Table 3.

**Conclusions**

QCDOC is progressing well with large machines due in 2003. Simulations indicate these machines will run QCD at high efficiency on the largest machines, while having a low cost per sustained Megaflop and low power consumption.

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