**Abstract:** This paper proposes an alternative way to implement a linearly tunable CMOS voltage differencing transconductance amplifier (VDTA). It has been designed by using the floating current source (FCS) and the current squaring circuit. The circuit achieves its linear tunability by squaring the long-tail biasing current of the FCS. In this way, the transconductance gains of the proposed CMOS VDTA can be varied linearly through adjusting the DC bias currents. As an application example, the proposed VDTA is used in the design of an actively tunable voltage-mode multifunction filter. The derived filter possesses the following desirable properties: simultaneous realization of three standard filter functions; employment of only two grounded capacitors; and electronic tunability of the natural angular frequency and the quality factor. The performance of the proposed circuit and its filter design application were examined by PSPICE simulations with TSMC 0.25-mm CMOS real process technology.

**Keywords:** Voltage Differencing Transconductance Amplifier (VDTA); Current Squareer; MOS analog circuits; Low-voltage circuits; Electronically tunable.

**1 Introduction**

A brief review of the recently reported active elements and an introduction to several new controllable elements are given in [1]. Among other things, the voltage differencing transconductance amplifier (VDTA) is one of attractive active devices with two-parameter control [2-6]. This device is a modified version of the previously introduced current differencing transconductance amplifier (CDTA) element, in which the current differencing unit at the input stage is replaced by the voltage differencing unit. Usually, the VDTA solution can be realized by composing two voltage-controlled current sources, which are interconnected internally. Each of them provides two independent transconductance gains \( g_mF \) and \( g_mS \), which are electronically adjustable by external DC biasing currents [5]. Therefore, the VDTA element is very useful in active circuit synthesis and quite suitable for electronically controllable analog circuits. Another advantageous feature of this element is that it can easily be used for transconductance-mode solutions due to its input signals being voltages while the output signals are current [2]. Several CMOS reali-
izations of the VDTA circuit have been described in the literature [2-4]. Previously, the CMOS implementation of the VDTA employing basic floating current sources (FCSs) and supply voltages of ±0.9 V was introduced in [2]. The improved CMOS VDTA was suggested in [3], in which the ideal current sources are realized with swing cascade current mirrors. This kind of current mirrors is used because it has good accuracy and high-output impedance, and the minimum output voltage swing is approximated to $2V_{DS(sat)}$ [7]. In [4], the design of the CMOS VDTA was also reported, where both transconductance sections were derived from the structure presented in [5]. In this structure, the well-known configuration of multiple-output second-generation current conveyor (MO-CCII) has been supplemented to obtain the required number of current outputs of the first transconductance section. However, their major disadvantage though is the well-known fact that their performance (namely the gain $g_{m}$) is directly proportional to the square root function of the external DC biasing current. Due to this the tunability is non-linear, and their linear transconductance ranges are rather limited.

The motivation of this paper is to develop the CMOS VDTA with linearly tunable transconductance. To this aim, the proposed CMOS VDTA utilizes the floating current source (FCS) in its voltage-to-current conversion. In the presented work, the CMOS current squaring functional circuit with the output current proportional to the square of the input current is employed as a biasing circuit for the FCS. The main feature of the proposed VDTA is that it exhibits an ability to linearly tune its transconductance gains by electronic means through the external DC biasing current. To illustrate the application of the proposed VDTA, the design of active voltage-mode multifunction filter with single input and triple outputs is considered. It realizes simultaneously the three standard biquadratic filters namely lowpass (LP), bandpass (BP) and highpass (HP) from each output of the circuit. Orthogonal electronic programmability of $\omega$ and $Q$ is also discussed in detail. PSPICE simulations with TSMC 0.25-µm CMOS process parameters are also reported, which demonstrate the linearity and effectiveness of the proposed VDTA and its application.

2 Basic concept of the VDTA

Basically, the VDTA is an alternative versatile active building block, having five high-impedance terminals, as symbolically shown in Fig.1. The characteristic between terminal voltages and currents can be described by the following matrix relation:

$$
\begin{bmatrix}
i_p \\
i_n \\
i_z \\
i_x \\
i_y
\end{bmatrix} = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
g_{mF} & -g_{mF} & 0 & 0 & 0 \\
0 & 0 & g_{mS} & 0 & 0 \\
0 & 0 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
v_p \\
v_n \\
v_x \\
v_z \\
v_y
\end{bmatrix},
$$

where $g_{mF}$ and $g_{mS}$ are the first and second transconductance gains of the VDTA, respectively. In (1), the differential input voltage applied across the p and n terminals ($v_p - v_n$) is converted to a current flowing out of the z terminal ($i_z$) by $g_{mF}$. Similarly, a voltage across the z terminal ($v_z$) is transformed to the current outward from the x+ and x- terminals by $g_{mS}$.

3 Basic functional circuits

3.1 Current-squaring circuit

Fig.2 shows a current squaring circuit (M1-M3) based on the square-law characteristic of MOS transistors biased in the strong inversion region [8-10]. The current-controlled biasing circuit (M4-M5) is introduced in order to supply the bias voltage $V_B$, where $I_B$ is the bias current. Assuming that all transistors are properly biased to operate in saturation mode and obey the ideal square-law function, the relation between the output current $I_{SQ}$ and the input current $I_B$ is given below.

$$
I_{SQ} = \frac{I_B^2}{8I_A}.
$$

To guarantee a proper operation, the input current $I_B$ is restricted within the range:

$$
-4I_A < I_B < 4I_A.
$$
We observe from eq. (2) that $I_{SQ}$ is the squaring function of $I_B$ with the gain equal to $(1/8)I_A$. In addition to eq. (2), the current $I_{SQ}$ is ideally temperature insensitive.

### 3.2 Floating Current Source

Fig.3 shows the circuit diagram of the floating current source (FCS) [11], which will be used as a fundamental circuit for exhibiting the transconductance gain of the proposed VDTA. The circuit can be viewed as two long-tailed differential pairs of PMOS and NMOS connected in parallel. It converts the differential input voltage ($v_{id} = v^+ - v^-$) into two balanced output currents $i_{o+}$ and $i_{o-}$. The NMOS transistors $M_4$ and $M_5$ are identical and the PMOS transistors $M_6$ and $M_7$ are also identical. Assuming that all the transistors are working in saturation region, an effective small-signal transconductance of the FCS can be expressed as [11]:

$$g_m = \frac{i_{o+}}{v_{id}} = \frac{i_{o-}}{v_{id}} = \frac{g_{mn} + g_{mp}}{2},$$  

where $g_{mn}$ and $g_{mp}$ are respectively the transconductance values of the NMOS and PMOS transistors, equal to:

$$g_{mn(p)} = \sqrt{K_{n(p)} I_0}.$$  

In above expression, $K_{n(p)} = \frac{\mu_{n(p)} C_{ox} W}{2 L} \mu_{n(p)}$ is the average carrier mobility for NMOS and PMOS transistors, $C_{ox}$ is the gate-oxide capacitance per unit area, $W$ and $L$ are the effective channel width and length, and $I_0$ is the external DC bias current. Evidently from eqs.(4) and (5), the $g_m$ value of the FCS circuit in Fig.3 is proportional to a square-root of the control current $I_C$.

4 Proposed linearly tunable VDTA

A complete circuit diagram of the proposed linearly tunable VDTA (LT-VDTA) and its symbol are shown in Fig.4. Basically, it consists of two FCSs ($M_{9F}$-$M_{11F}$ and $M_{9S}$-$M_{11S}$) in Fig.3 and two current squaring circuits ($M_1$-$M_3$) in Fig.2. The current-controlled DC level-shifting circuit $M_{B1}$-$M_{B2}$ and $I_A$ provide a bias voltage $V_B$ for the circuit. As seen in Fig.4, the currents $I_{SQF}$ and $I_{SQS}$ are mirrored to be the bias currents $I_{OF}$ and $I_{OS}$ of two FCSs by means of the current mirrors $M_{4F}$-$M_{8F}$ and $M_{4S}$-$M_{8S}$, respectively. It can be arranged that if $(W/L)_6 = (W/L)_5 = 8(W/L)_4$ and $(W/L)_5 = (W/L)_4$, then, using eq.(2) and considering $I_{OF} = 8I_{SQF}$ and $I_{OS} = 8I_{SQS}$, we have:

$$I_{OF} = \frac{I_{BF}^2}{I_A},$$  

and

$$I_{OS} = \frac{I_{BS}^2}{I_A}.$$  

Substituting eqs.(6) and (7) into (5), and solving for the first and second transconductance gains of the proposed LT-VDTA in Fig.4, the results are:

$$g_{mF} = K_m I_{BF},$$  

and

$$g_{mS} = K_m I_{BS},$$
where
\[ K_m = \frac{\sqrt{K_n} + \sqrt{K_p}}{2\sqrt{I_A}}. \]  
(10)

Since \( K_n \) is considered as a constant value, eqs. (8) and (9) imply that the transconductances \( g_{mF} \) and \( g_{mS} \) of the proposed LT-VDTA can be adjusted electronically and linearly by \( I_{BF} \) and \( I_{BS} \), respectively. As was stated earlier, in order for the proposed circuit to operate correctly, the linear operating condition for the input controlling currents \( I_{BF} \) and \( I_{BS} \) is bounded according to eq.(3).

Owing to the performance of the traditional FCS stage used in the proposed LT-VDTA structure of Fig.4, the output resistances at terminals \( z, x+ \) and \( x- \) are not high enough for some applications. In order to increase the output resistance level, the improved FCS [12] can be employed for this structure. However, while the output resistance value is improved, the output voltage swing drops by up to \( V_{DSAT} \).

5 Simulations, results and discussions

For all the circuits examined in this work, the computer simulations with PSPICE are performed using model parameters of TSMC 0.25-\( \mu \)m CMOS technology. The transistor sizes used for simulation are listed in Table 1. Bias voltages were \( \pm V = 1.5 \) V and bias currents \( I_A \) were 50 \( \mu \)A.

### Table 1: Transistor sizes of the proposed LT-VDTA in Fig.4.

| Transistors       | W (\( \mu \)m) | L (\( \mu \)m) |
|-------------------|---------------|---------------|
| \( M_{B1} - M_{B2} \) | 7             | 0.25          |
| \( M_{1F} - M_{2F} \) | 6             | 0.25          |
| \( M_{1S} - M_{2S} \) | 49            | 0.25          |
| \( M_{4F} \) | 6.2          | 0.25          |
| \( M_{4S} \) | 17           | 0.25          |
| \( M_{7F} \) | 24           | 0.25          |

The CMOS current squaring circuit in Fig.2 is simulated. Fig.5 illustrates the DC current transfer curves of the current squaring circuit in Fig.2, obtained for the input controlling current \( I_B \) value ranging from -200 \( \mu \)A to 200 \( \mu \)A. It can be deduced from the simulation results that the circuit performs the current squaring operation as expected.

### Figure 5: DC current transfer curves of the current squaring circuit in Fig.2.

In order to demonstrate the linear tuning performance of the proposed LT-VDTA in Fig.4, the simulation for the
transconductance $g_{mf}$ is carried out. Fig.6 shows the $g_{mf}$ variations as a function of the input controlling current $I_{BF}$. In these plots, the simulated results and the expected values are compared, and in good agreement over a considerable input range from 20 $\mu$A to 180 $\mu$A. It is clear from the curves that the proposed circuit can be tuned linearly by means of the current $I_{BF}$.

![Figure 6](image_url)

**Figure 6**: Expected and simulated $g_{mf}$ of the proposed LT-VDTA of Fig.4 as a function of $I_{BF}$.

The DC transfer functions of the proposed LT-VDTA in Fig.4 are also simulated and shown in Fig.7, with $V_{id} = (V_p - V_n)$ continuously changing from -400 mV to 400 mV, and $I_{BF}$ being equal to 50 $\mu$A, 100 $\mu$A and 150 $\mu$A, respectively. For $I_{BF} = 150$ $\mu$A, the circuit has a linear region over ±180 mV and non-linearity error is less than 9.16%.

![Figure 7](image_url)

**Figure 7**: Simulated DC transfer characteristics between $V_{id}$ and $I_{bf}$ with tuning $I_{BF}$.

To study the AC transfer characteristic of the proposed LT-VDTA, the simulated frequency responses for $g_{ms}$ when $I_{BS}$ is swept from 50 $\mu$A to 150 $\mu$A with 50 $\mu$A step size are plotted in Fig.8. According to Fig.8, the useful bandwidth of about 400 MHz can be observed. In addition to the simulation results, the maximum power dissipation is 6.25 mW, when $V_{id} = 180$ mV, and $I_{BF} = I_{BS} = 150$ $\mu$A. The quiescent power dissipation is 1.34 mW, when $V_{id} = V_{BF}$ and $I_{BS}$ are zero.

![Figure 8](image_url)

**Figure 8**: Simulated frequency characteristics of $g_{ms}$ with tuning $I_{BS}$.

### 6. Active voltage-mode multifunction filter realization

To demonstrate the effectiveness of the proposed LT-VDTA, an active voltage-mode multifunction filter of Fig.9 is realized as a design example [13]. The circuit consisting of two proposed LT-VDTAs in Fig.4 and two grounded capacitors realizes three standard biquadratic filtering functions, i.e. lowpass (LP), bandpass (BP) and highpass (HP), simultaneously without changing its configuration and without the need to impose component constraints. Straightforward analysis of Fig.9 using eq.(1) yields the following three voltage transfer functions.

$$H_{LP} = \frac{V_{LP}(s)}{V_{in}(s)} = H_0 \left( \frac{g_{mf2}g_{ms2}}{C_1C_2} \right) \left( \frac{1}{D(s)} \right), \quad (11)$$

$$H_{BP} = \frac{V_{BP}(s)}{V_{in}(s)} = H_0 \left( \frac{g_{mf2}}{C_1} \right) \left( \frac{s}{D(s)} \right), \quad (12)$$

and

$$H_{HP} = \frac{V_{HP}(s)}{V_{in}(s)} = H_0 \left( \frac{s^2}{D(s)} \right), \quad (13)$$

where

$$H_0 = \frac{g_{mf1}}{g_{ms1}}. \quad (14)$$
\[ D(s) = s^2 + \left( \frac{g_{mf2}g_{ms2}}{g_{ms1}C_1} \right) s + \left( \frac{g_{mf1}g_{mf2}g_{ms2}}{g_{ms1}C_1C_2} \right), \]  

and \( g_{mf1} \) and \( g_{mf2} \) (\( i = 1, 2 \)) are respectively first and second transconductance gains of the \( i \)-th LT-VDTA. It follows from eqs.(11)-(15) that the natural angular frequency (\( \omega_o \)) and the quality factor (\( Q \)) of the filter are

\[ \omega_o = \sqrt{\frac{g_{mf1}g_{mf2}g_{ms2}}{g_{ms1}C_1C_2}}, \]  

and

\[ Q = \sqrt{\frac{g_{mf1}g_{ms1}C_1}{g_{mf2}g_{ms2}C_2}}. \]  

Figure 9: Actively tunable voltage-mode multifunction filter realization using the proposed LT-VDTAs.

To achieve independent filter parameter control, a proper design can be developed by setting equal transconductances such that \( g_{mf1} = g_{mf2} = g_{ms1} \) and \( g_{mf1} = g_{mf2} = g_{ms2} \), then \( \omega_o \) and \( Q \) from eqs.(16) and (17) turn to

\[ \omega_o = \sqrt{\frac{g_{ms1}}{C_1C_2}}, \]  

and

\[ Q = \sqrt{\frac{g_{ms1}}{g_{ms2}C_1C_2}}. \]

The parameter \( \omega_o \) can be tuned separately by changing \( g_{mf1} \). The transconductance ratio of \( g_{ms1} \) and \( g_{ms2} \) can be used for an adjustment of the parameter \( Q \). However, if independent electronic control is needed, only \( g_{ms1} \) could be used for \( Q \) control.

Furthermore, from eqs.(16) and (17), the active and passive sensitivities of \( \omega_o \) and \( Q \) can be expressed as:

\[ S_{\omega_o}^{\omega_o} = -S_{\omega_o}^{g_{ms1}} = \frac{1}{2}, \quad S_{\omega_o}^{g_{ms1}} = -\frac{1}{2} \]  

and

\[ S_{Q}^{Q} = -S_{Q}^{\omega_o} = \frac{1}{2}, \quad S_{Q}^{\omega_o} = -S_{Q}^{g_{ms2}} = \frac{1}{2} \]

Both are low, and equal to 0.5 in magnitude.

As a design example, the multifunction filter of Fig.9 has been realized to obtain the LP, BP and HP responses with the natural angular frequency \( f_o = \omega_o / 2\pi \approx 5.50 \text{ MHz} \) and the quality factor \( Q = 1 \). For this purpose, the circuit components were set to: \( I_{BF1} = I_{BF1} = I_{BS1} = I_{BS1} = 70 \mu\text{A} \) (\( g_{mf1} = g_{mf1} = g_{ms1} = g_{ms1} = 0.66 \text{ mA/V} \)), and \( C_1 = C_2 = 20 \text{ pF} \). The simulated LP, BP and HP amplitude responses of the circuit are shown in Fig.10, where the simulated values of \( f_o \) were found to have a maximum deviation of 2.83% from the expected values. In this simulation, the total power consumption of the designed filter is about 4.51 mW.

Figure 10: Simulated AC transfer responses for the actively voltage-mode multifunction filter in Fig.9.

In Fig.11, the electronic adjustment of the BP characteristic is illustrated by simulating multiple values of \( f_o \) (i.e. \( f_o = 4.50 \text{ MHz}, 7.60 \text{ MHz}, \) and \( 11.35 \text{ MHz} \)), and keeping a constant \( Q = 1 \). Its responses for three values of \( f_o \) are obtained by tuning identical bias currents \( I_{BF1} = 50 \mu\text{A}, 100 \mu\text{A}, \) and \( 150 \mu\text{A} \), respectively.
The simulation results of the BP response for variable $Q$ and fixed $f_0$ are given in Fig.12. In this way, the values of $Q$ were tuned via LT-VDTA 1, for $Q = 5, 7, 10$, which correspond to $I_{B1}(i.e., I_{BF1} = I_{BS1}) = 250 \mu A, 350 \mu A, 500 \mu A (g_m1 = 2.40 mA/V, 3.33 mA/V, 4.86 mA/V)$. A constant $f_0 = 4.50 MHz$ was set with the bias currents of LT-VDTA 2, i.e., $I_{B2} = I_{BF2} = I_{BS2} = 50 \mu A (g_m2 = 0.57 mA/V)$.

**Figure 12:** Simulated BP responses of Fig.9 with tuning $Q$.

### 7 Conclusions

In this work, a linearly and electronically tunable CMOS VDTA circuit is realized. The circuit realization is based on floating current sources (FCSs) for implementing the transconductance stages. The CMOS current squaring circuit is used for supplying the long-tail bias current of the FCS stages. Its transconductance gains are linearly tuned and accurately determined by the external DC supplied currents. The use of the proposed VDTA is illustrated with a realization of an electronically tunable voltage-mode multifunction filter, which employs two VDTAs and two grounded capacitors. PSPICE simulations, performed using TSMC 0.35-$\mu m$ CMOS technology and confirming the performance of the proposed circuit and its application, are also given.

### 8 Acknowledgements

This work was supported by King Mongkut’s Institute of Technology Ladkrabang Research Fund [grant number KREF116001]. The author is grateful to Mr. Natchanai Roongmuanpha for his circuit simulation on an earlier version of the manuscript. Also, the author gratefully acknowledges the constructive comments and suggestions of all the anonymous reviewers, which have been very useful in the preparation of the revised version of the manuscript.

### 9 References

1. D. Biolek, R. Senani, V. Biolkova, Z. Kolka, “Active elements for analog signal processing: classification, review, and new proposals”, Radioengineering, vol.17, no.4, pp.15-32, 2008.
2. A. Yesil, F. Kacar, H. Kuntman, “New simple CMOS realization of voltage differencing transconductance amplifier and its RF filter application”, Radioengineering, vol.20, no.3, pp. 632-637, 2011.
3. A. Yesil, F. Kacar, “Electronically tunable resistor-less mixed mode biquad filters”, Radioengineering, vol.22, no.4, pp.1016-1024, 2013.
4. J. Jerabek, R. Sotner, K. Vrba, “Electronically adjustable triple-input single-output filter with voltage differencing transconductance amplifier”, Rev. Roum. Sci. Techn.– Électrotechn. et Énerg., vol.59, no.2, pp.163-172, 2014.
5. J. Satansup, W. Tangsrirat, “Compact VDTA-based current-mode electronically tunable universal filters using grounded capacitors, Microelectron. J., vol.45, no.6, pp.613-618, 2014. [https://doi.org/10.1016/j.mejo.2014.04.008](https://doi.org/10.1016/j.mejo.2014.04.008)
6. W. Tangsrirat, S. Unhavanich, “Voltage differencing transconductance amplifier-based floating simulators with a single grounded capacitor”, Indian J. Pure & Appl. Phys., vol.52, no.6, pp.423-428, 2014.
7. P. E. Allen, D. R. Holberg, CMOS Analog Circuit Design, New York : Oxford, 2002.
8. K. Bult, H. Walliga, “A class of analog CMOS circuits based on the square-law characteristic of an MOS transistor in saturation”, IEEE J. Solid-State Circuits, vol.SC-22, no.3, pp. 357-365, 1987. [https://doi.org/10.1109/jssc.1987.1052733](https://doi.org/10.1109/jssc.1987.1052733)
9. O. Landolt, E. Vittoz, P. Heim, “CMOS self-biased euclidean distance computing circuit with high dynamic range”, Electron. Lett., vol.28, no.4, pp.352-354, 1992. [https://doi.org/10.1049/el-19920220](https://doi.org/10.1049/el-19920220)
10. C. Popa, “CMOS logarithmic curvature-corrected voltage reference by using a multiple differential
structure”, Rev. Roum. Sci. Techn.– Électrotechn. et Énerg., vol.55, no.4, pp.436-444, 2010.

11. A. F. Arbel, L. Goladminz, “Output stage for current-mode feedback amplifiers, theory and applications”, Analog Integr. Circ. Signal Process., vol.2, no.3, pp. 243-255, 1992. 
https://doi.org/10.1007/bf00276637

12. M. Altun, H. Kuntman, “Design of a fully differential current-mode operational amplifier with improved input-output impedances and its applications”, Int. J. Electron. Commun. (AEU), vol.62, no.3, pp. 239-244, 2008.
https://doi.org/10.1016/j.aeue.2007.03.020

13. J. Satansup, W. Tangsrirat, “Voltage-mode multifunction filter using VDTA and grounded capacitors”, Proc. the 6th Conf. Electrical Eng. Network of Rajamangala University of Tech. 2014 (EENET 2014), pp.533-536, 2014.

Arrived: 11. 04. 2019
Accepted: 21. 05. 2019