Area Efficient Reconfigurable Buffer for NoC Router

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Abstract. In the current research, FPGA-based architecture of the Noc device reconfigurable router is suggested. Proposed router specification entry is done with the Verilog Hardware Description Language. The latest research has a five-channel router and a crossbar switch (east, west, north, south and local). Each channel has buffers and multiplexers. FIFO buffer stores data, and multiplexer monitors the input and output of data. The channel contains FIFO architecture and multiplexers. The crossbar switch is then planned and five other channels. Reducing the number of LUTs in the proposed work decreased the router area. A report is given for the number of LUTs used in a router. Results obtained indicate the area efficiency of the proposed router over existing method.

Keywords: Buffer, FIFO, LUTs, NOC.

1. Introduction
The Conventional Chip System (SOC) consists of bus, cable delay, noise, problems with power dissipation and signals. A network on a chip, which provides a high-performance networking infrastructure, is called an on-chip communication interconnection architecture. Networks-on-Chip has all the requirements required for the production of future SoCs. It is managed by a network of communicating routers and point-to-point networks. Colliding between packaging is considered an unavoidable issue by a conventional computer network and computer networks' ultimate aim is to reduce area probability. Management of buffers is not a recent issue, but still needs consideration. This increases the output to immediately use the unused buffers. In the experiments performed by the buffers, NoCs were the biggest consumers of leakage power, with crossbars, arbiters, buffers and connections, dissipating about 64% of the overall power budget. This considered the buffers as candidates to maximize leakage capacity, since there were still 85% of idle buffers, even at high loads. The consumption of buffers is also high with regard to dynamic capacity, and it is increasingly increasing as the packet flow increases.

Our basic contribution is designed to provide the router with some reconfiguration logic that makes adjustments to the use of buffers on each input channel in compliance with communication needs. The idea is that each input channel should provide buffer units to and from nearby channels for a given bandwidth. If the whole buffer is not needed for a channel, it can loan buffer word slots to nearby
channels. The findings show that the buffers used by the same router are unreliable and the improvements made with the new strategy can be achieved.

2. Related work

The buffer share of the latest router architectures has recently been analyzed and compared. The chip system has been suggested by a number of recent works, [1-3] the failing to regularly use a buffer is abused through the network and its power gate is extended to buffers that are rarely in use. This design choice has a significant performance advantage instead of shutting down the buffers, because the virtual channel buffer still is able to accept network packages [4-6]. Installation options are not yet available. The use of buffers in a chip network varies widely across the network. Power gates allow the turn off of buffers that are rarely used. A new pipelined router design [7-8], They based on reducing latency in the router. Primarily certain router components have been defined by taking critical paths that bind the router frequency. Limitations placed by a part called, arbiter, on router output. Thus, the builder has made many smaller arbiters. [9] Solution has been provided for the critical communication problem between multiple IP cores. The initial router architecture on chip interconnect network NoC was integrated in the Module. Device has a parametric router design on chip interconnect network. [10-11]. Rising electronic systems requirements are one of the main factors for the advancement of integrated circuit technology. Multiprocessing is the solution for meeting potential application requirements. Efficient on-board communication is important for multiple processing over heterogeneous operational units [11]. Network-on-Chip (NoC) is the overall on-chip connectivity principle that offers high performance, the essential prerequisite for addressing modern systems' complexity. All links in NoC can be used for the simultaneous transmission of data that ensures high parallelism and makes the replacement of traditional communication architectures such as joint buses attractive.

Comparison of packet delay and XY routing algorithm results with OE routing algorithm. The problem of architectural hindered contact and clock. In the architecture built, in which the buffer size can be reconfigured. This approach will reduce the excessive latency, power dissipation. The architecture is also an productive field. [12-13]. It defined the integration of different components into the NoC architecture as well as the modeling of reconfigurable components, such as IP cores and fixed IPs. This work provides a fresh design method for customizing the routers in a network-on-chip for reconfigurable buffer systems over [13]. More coordination mechanisms are increased as the complexity of the NoC architecture increases. To reduce the buffer demand and increase the device output, a wormhole flow control has been proposed. But a packet can take several intermediate switches simultaneously. On the other hand [14-19]. When a packet occupies a channel buffer in traditional NoC architectures, only blocking the original message does not allow the actual channels to be used on other channels. This raises the issue of deadlock and livestock.

3. Proposed system

A new add-on module will decide which FIFOs will accept the received packet that are available on the network. Finally, communicating with both output ports is responsible for passing the received packet onto its downstream routers according to the route method employed.

Here, a FIFO can accept packets from the directly connected upstream router as FIFOs for the Base routers, but from other ports. Transfer logic: Apply a routing algorithm to select the correct output port for the packet path. The Flexible router's operations are the same as the base router, but in the case of a dispute it will be special. In terms of contention, the Flexible Router shall not wait until one or more free slots are available to the required full FIFO, such as the Base Router, Nevertheless, the FFC searches for a free slot in any suitable non-full FIFO throughout the router by asking for FIFOs that are not complete in other input ports and returns the application to the upstream router when it finds a free slot. The kit is then passed to the chosen FIFO. The Robust Router will then function in the same way as the Base Router does in the same way as the Base Router does. Every port of entry only has one physical channel linking all channels of virtual input port.
These have no completely specific, virtual channels and the buffer length can be altered in real time for each virtual channel. In addition, flits on the next input port that have the same output are shared with the VC buffer. The buffer area between the current input port and the next port is split and the split area can also be actively requested based on real demand for traffic. The buffer input is divided in a clockwise direction in order to keep it simple. Eastern port, for example, only the south port buffer tool can be used. Further buffers are used by the port to transfer further data, utilizing the buffer resources entirely. application-oriented NoC, the traffic at the router's ports is special.

Some regulations are established to allow other adjacent channels to use buffers from one channel. If a channel fills its FIFO, it can give its neighbors more buffer terms. The channel first asks the right Neighbour for buffer terms and attempts to borrow from the left neighbor FIFO if it is still in need of more buffers. In order to monitor its stored flows, certain signals from each channel must be sent to the nearby channels. Every channel must therefore know how many buffer terms its own channel and its adjacent channels use and also how much its own buffer is used by the next channels. This number is informed by a control block.
The entire router therefore needs to support dynamic configuration to satisfy the generality requirements. Architecture of the router includes mechanism for allocating the buffer inter port. At the one side, as per the data needs of intelligent allocation of buffer resources, the channel can be automatically configured by various ports. In another hand, VC in same ports takes the flexible linked list as a means of realizing changeable buffer length and storing the flits based in calculated output.

The first two bits are used in an 8-bit packet to show the address of the next NOC router. In this job, the block diagram as shown is displayed. Four new directions have added fewer storages to the support buffer that will boost performance. 1. It’s the first step that has been taken. The block was built in theory with the previous iterations of homogeneous routers, which had all resources automatically allocated, and which could not be modified during design times, which presented problems of a more sluggish rejection of data when used in different channels. Four other directions (North East, North West, South East and South West) are presented with the planned architecture which will contribute to multidirectional steps. Newly added details from your neighbour shares fifo to save your data. In contrast with the previous one, dates from one direction can now be route to seven directions, where the data from one direction can be routed only in three directions. The newly developed architecture offers more routes for data routing so that the critical path time of a network can decrease and the IC speed can be helpful. We now follow the rectilinear path of stonier tree to cut the data path to the router with this newly developed architecture.

The input port includes an actual channel, which is connected to all virtual input port channels and does not have a fully separate virtual channel and the buffer length can be modified in real time for any virtual channel. Only flits with the same output are shared with the VC buffer at adjacent input port. Based on the actual traffic request, a dedicated buffer zone can be requested between the current port and the nearest port of entry. The input buffer is shared in the rectangular direction to keep it simple. For instance, eastern port can use a buffer resource only for south port. More buffers will complete a port requiring more data, so that the buffer functions shown in figure 2 can be used entirely.

| Parameters                  | Generic router | Virtual channel router | Proposed router |
|-----------------------------|----------------|------------------------|-----------------|
| Buffer/Buffer less          | Buffered       | Buffered               | Buffered        |
| Types of buffer             | Simple buffer  | Virtual channel as buffer | Flexible buffer |
| Probability of data loss    | High           | Medium                 | Low or negligible |
| Hand shaking                | No             | No                     | No              |

The two adjacent ports set up common buffer space. The buffer state will change in time when a buffer space is borrowed or loaned. The buffer is connected in a clockwise direction on the entire router. One system uses two multiplexers to automatically monitor the input tampon and to share the tampon with the nearby terminal only. When a port receives large quantities of data well outside its independent buffer, it will ask the data to be processed from the specific port. Based on fixed exclusive buffer sources, the inter-port buffer allocation process prevents changing internal programming mechanisms and ensures communication requirements. We can see that the buffer value is reconfigurable. Uses an improved control logic buffer.
4. Results and Discussion
The benefit of reconfigurable buffered is realized in the proposed design. The packet traversal is performed by a buffer network at medium load condition the packet traversal is through reconfigurable buffer.

Figure 3. Simulation results of FIFO

Figure 4. RTL view of proposed router
It offers better performance than generic NoC router. This article introduced a resource efficient Noc that would support rearrangement for mode changes. A NoC expands a current NoC and offers guaranteed-service inter processor communication.

![Simulation result of proposed method](image)

**Figure 5.** Simulation result of proposed method

Introduction of the planned design is measured in terms of the worst-case reconfiguration time, cost of hardware and overall service frequency. Compared to generic router, proposed router area shown in table 2. The proposed router received percent less delay than the generic router and when compared to the virtual channel router in Table1. Reducing pipeline stages in each router leads to reduced delay for packets, which in effect reduces average latency shown in figure 3a. RTL view of proposed method is shown in figure 3b and simulation results of proposed router shown in figure 4.

| Parameters | Existing method | Proposed method |
|------------|-----------------|-----------------|
| Slices     | 338             | 306             |
| LUT's      | 1267            | 1124            |
| FF's       | 924             | 908             |

**Table 2.** LUT’s comparison of proposed with existing method

The processing nodes can be separated by location into three different groups with traditional NoC mesh corner, edge and central nodes. The comparison between proposed with existing method shown in fig 5. Three, four and five I / O ports need routers based on these categories. Thanks to the distributed and independent controlling logic, routers can be designed to comply with this requirement with the required hardware without any additional effort.
Therefore, for any number of I/O ports the Architecture is completely configured. By simply doubling the input portion of the unit and increasing a crossbar on the output side the number of I/O ports can be increased to any amount. FIFO input buffer and cross-point input buffer to increase performance and reduce HOL. The architecture of the cross-point input buffer will optimize output. For each input output pair, there is one buffer. However, we can streamline buffer design in the cross-point buffer architecture for an application such NoC features. The IP core must be mapped in the basic application design flow of NoC. Router design using reconfigurable buffer is implemented at the RTL level using Verilog HDL in this paper. Design is synthesized using Xilinx and modeled using ISIM 14.7 for router-proposed region evaluation. In conventional static router is used on chip throughout the network. Nevertheless, it does not acknowledge the applications' need for traffic. This will result in lower buffer usage and will drain valuable buffer space on the router.

5. Conclusion
This paper proposes efficient router architecture to boost network efficiency including mechanism for internal-port allocation. The new router architecture will increase buffer efficiency without impacting network output by modifying the Buffer input unit of Noc router. Future work an application for real-time analysis can be used with different techniques of routing available and comparable to existing routers. In addition, different technologies may be implemented for efficiency enhancements such as multicast and network surveillance. Recently a domain language was implemented in [12] for a particular distributed architecture. In order that we increase the degree of abstraction from application layers, we expect a similar approach for further creation of NoC systems includes improving the latency process by which reconfigurable buffers are associated with input ports.

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