Design and Development of Non-Linearly Controlled Class-D Audio Amplifier

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Abstract: A systematic and simple approach to develop a 20 W audio frequency range switch mode amplifier is presented in this paper. A non-linear sliding mode (SM) technique-based low cost analog controller enables the realized amplifier to deliver highly linear and efficient operation throughout the audio frequency spectrum. The theoretical aspects and practical limitations in the design and realization of subsystems, such as the signal conditioning stage, power stage and sliding mode controller, are considered, while the viable solution is also stated and justified. The hardware realization scheme is also elaborated, based on which the laboratory prototype is fabricated. Hardware results with a 4 Ω resistive load are given on which the performance of the amplifier is evaluated. The total harmonic distortion (THD) below 1% and 73% efficiency at peak load make the amplifier well suited for high quality audio application.

Keywords: audio amplifier; Class D technique; non-linear control; sliding mode control

1. Introduction

The clear and faithful sound of a home audio system is vital for a good listening experience. Basic equipment employed to fill a venue with quality sound are an audio amplifier and loudspeaker. On receiving signal from an audio source (mic, CD/DVD, pen drive, etc.), the audio amplifier amplifies the input signal with the desired gain. The amplified signal is then applied to the loudspeaker, which extracts power from the amplifier to produce sound.

For the accurate reproduction of sound, the linearity of an audio amplifier in the frequency band of 20 Hz to 20 kHz is the decisive feature. Linear amplifiers (Classes A, B, and AB) used in low-power audio applications offer high linearity but suffer from poor efficiency. The class AB amplifier is widely used among linear amplifiers due to its high efficiency and highly linear operation; however, at the actual listening level, the efficiency rarely exceeds 20% [1]. Other amplifiers classes, such as Classes D, E and F, also exist. Class E and Class F amplifiers are highly efficient but they find applications in radio frequency and microwave range [2]. The Class D amplifier exhibits high efficiency, which makes it well suited for audio applications.

With the advent of Class D technology, the audio industry is on the verge of replacing conventional analog amplifiers with switch mode amplifiers. The driving force behind the paradigm shift is close to 100% efficiency of switch mode operation [3,4]. Highly efficient Class D amplifiers, besides having greater run time for battery-powered audio devices,
also provide the benefit of compact size and high portability, even for high-power audio applications [3].

Open loop architecture-based Class D amplifiers, though highly efficient, suffer from poor linearity. Besides device non-ideality, such as rise/fall time, turn on/off time and turn on/off delay, etc., the half/full bridge power stage is chiefly responsible for reduced linearity of the amplifier [6]. Additionally, the conventional pulse width modulation (PWM) based audio amplification technique demands a highly accurate triangle carrier generator for satisfactory audio performance [6–8]. Additionally, the open loop architecture introduces low frequency power supply noise, which severely degrades the audio quality of amplifier [6]. All the drawbacks associated with open loop architecture and amplifier topology limits the use of Class D amplifier to low quality audio applications.

Closed loop operation can deliver improved linearity performance, high disturbance rejection and noise immunity. However to realize a PWM-based closed loop controlled amplifier demands unrealistic open loop bandwidth, around 20 MHz, and a high frequency carrier generator for audio grade amplification. For the same reason, a closed loop controlled amplifier using the PWM technique becomes impractical [9,10]. A non-linear controller, such as a hysteresis controller, has much wider control bandwidth, equal to switching frequency, in comparison to linear controller [11]. However, such an amplifier suffers from poor audio quality and the low disturbance rejection problem [6,11–15]. Using sliding mode control (SMC), the non-linear control technique, the closed loop operation can be realized at a significantly lower switching frequency [6,11,15]. Additionally, the advantages of high immunity to parameter variation, accurate reference tracking and no requirement of carrier signal [16–20] led to the selection of the SM technique for controlling the amplifier. Besides these, the simple circuit realization with low component count in designing controller gave motivation to use the SM technique for the development of a highly efficient, mid-power audio amplifier.

For effective description of presented work, the organization of the paper is given as follows. Section 1 discusses the theoretical aspects to develop the constituent blocks of the amplifier. A detailed discussion on the power stage parameters, functioning of the controller and decision on the control parameters is presented in this section. On the basis of selected parameters, the selection of active/passive components and realization of hardware is presented in Section 2. Performance validation is done by extensive testing of the amplifier. A series of tests were carried out to judge the efficiency, linearity and disturbance/noise rejection property of the amplifier, which are described in Section 3. To validate the suitability of the amplifier for actual conditions, the amplifier was tested with a loudspeaker load. The sample results of these tests are discussed in same section. On the basis of the theoretical/practical aspects, performance and shortcomings of the amplifier, a brief conclusion is given in Section 5 of the paper.

2. Amplifier Development

The sliding mode controlled amplifier (SMCA) consists of the signal conditioning stage and amplification stage. The signal conditioning stage (SCS) of SMCA receives input audio signal, \( v_s \), from the audio source. The output of SCS is pre-amplified signal, \( v_{ref} \), which is applied to the main amplification stage for power amplification. The output of the main amplifier then drives the loudspeaker. The detailed working of each SMCA stage is described in the following sections.

2.1. Signal Conditioning Stage

Figure 1 illustrates the block diagram of the SCS. Pre-amplification of the pre-amplified signal and signal biasing are the main functions of this block.
The pre-amp block amplifies the input audio signal, $v_{\text{ref}}$, with desired gain, while the adder circuit augments the amplified signal with positive/negative dc bias. Biased signal, $v_{\text{bias}}$, serves as a reference to the main amplifier.

2.2. Amplification Stage

The amplification stage, core of the amplifier, enhances the RMS voltage of the incoming reference signal, $v_{\text{ref}}$. The output of the amplification stage powers the loudspeaker system with an amplified signal, which transforms the audio signal into an acoustic signal. The amplification stage of SMCA consists of a band limited output stage and a non-linear controller. The description of these constituents and overall control scheme is presented in the following subsections. The schematic of the band limited output stage is shown in Figure 2. The power stage (PS) of the switching amplifier constitutes complementary switches S1, S2, arranged in a half bridge configuration, and voltage source, $V_{dc}$.

![Figure 2. Output stage of audio amplifier.](image)

The output voltage, $v_l$, of the power stage is the pulse density modulated (PDM) signal of amplitude $V_{dc}$. To extract amplified audio signal, $v_o$, from PDM signal, $v_l$, a band pass filter (BPF) is cascaded with the PS. The BPF is formed using high pass (HPF) and low pass (LPF) filters whose corner frequencies, $f_h$ and $f_l$, respectively, determine the lower and upper limits of the BPF. For this application, corner frequencies $f_h$ and $f_l$, listed in Table 1, are chosen to accommodate the full audio band. The LPF consists of the inductor, $L_f$, and capacitor, $C_f$. To render high pass characteristics, the capacitor, $C_b$, and load impedance $Z$ are utilized. The value of passive components chosen to realize HPF and LPF are listed in Table 1.

Table 1. $f_h$, $f_l$ and component values of BPF [21].

| $f_h$ (Hz) | $f_l$ (kHz) | $L_f$ (µH) | $C_f$ (µF) | $C_b$ (mF) | $Z(r_s)$ (Ω) |
|-----------|-----------|------------|-----------|---------|-------------|
| 4         | 24        | 20         | 2.35      | 10      | 4           |

Frequency response of the transfer function, $v_o(s)/v_l(s)$ (is given in Figure 3) with the loudspeaker load, modeled as a 4 $Ω$ resistor, to mimic its low frequency behavior. It clearly highlights the complete audio band coverage by the BPF.
The state space equations [22] of the output stage are given as

\[
\frac{d}{dt} \begin{bmatrix} i_l \\ v_c \\ i_o \end{bmatrix} = \begin{bmatrix} A \end{bmatrix} \begin{bmatrix} i_l \\ v_c \\ i_o \end{bmatrix} + \begin{bmatrix} V_{dc} \\ \frac{1}{L_f} \\ 0 \end{bmatrix} U
\]

(1)

where

\[
\begin{bmatrix} A \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_f} & 0 \\ \frac{1}{C_f} & 0 & -\frac{1}{L_f} \\ \frac{1}{r_s C_f} & 0 & -\frac{1}{r_s C_f} + \frac{1}{C_b} \end{bmatrix}
\]

(2)

and

\[
U = \begin{cases} 
1 & \text{S1 ON & S2 OFF} \\
0 & \text{S1 OFF & S2 ON}.
\end{cases}
\]

(3)

The voltage \(v_o\) drives the loudspeaker, which transforms the electrical signal into the audio output. The low-frequency component of the speaker current, \(i_o\), is related to the amplifier output as

\[
v_o = r_s \cdot i_o.
\]

(4)

Control Strategy

The closed loop strategy of SMCA is shown in Figure 4.

The reference \(v_{ref}\) and scaled output voltage \(\beta \cdot v_c\) are applied to the summer block. Here, \(\beta (\beta < 1)\) is the scale factor which yields the desired amplifier voltage gain of \(1/\beta\). The summer block constitutes a comparator, which produces error signal \(e\). This signal, \(e\), when applied to the SMC, results in the plant input, \(U\), which is given by (5).

\[
U = \begin{cases} 
0 & \text{S2 ON (S1 OFF)} \\
1 & \text{S2 OFF (S1 ON)}.
\end{cases}
\]

(5)

The state vector, \(X = [x_1 \ x_2]^T\), is given by (6).

\[
\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} e \\ \dot{e} \end{bmatrix} = \begin{bmatrix} v_{ref} - \beta v_c \\ \dot{x}_1 \end{bmatrix}
\]

(6)
Phase portraits of the states \((x_1, x_2)\), for control input \(U = 1\) and \(U = 0\), are depicted in Figure 5.

When \(U = 1\), the upper switch \(S_1\) is on, and states \(x_1\) and \(x_2\), starting from the arbitrary state, converge at point \((x_1 = v_{\text{ref}} - \beta \cdot V_{\text{dc}}, x_2 = 0)\) of the state space. For \(U = 0\), the lower switch \(S_2\) turns on, and the state trajectory starting from any arbitrary location, in state space, finally settles at point \((x_1 = v_{\text{ref}}, x_2 = 0)\). In the sliding mode control technique, states \(x_1\) and \(x_2\) form a switching surface, \(S\), around which the control action is determined \([16–22]\). The switching surface is defined as

\[
S = \alpha \cdot x_1 + x_2 = [\alpha \ 1][X] = [\lambda][X].
\]  

\((7)\)

**Figure 5.** Phase portrait when (a) \(S_1\) ON (b) \(S_2\) ON.

The coefficient \(\alpha\) in \((7)\) is termed as a sliding coefficient. The coefficient \(\alpha\), a control parameter, is chosen to determine the slope of the error trajectory, \(e(t)\). Figure 6 depicts a sliding line, which is obtained by setting \(S = 0\). The line \(\alpha \cdot x_1 + x_2 = 0\) bisects the entire phase plane, depicted in Figure 6.

**Figure 6.** Phase portrait when \(U = 1\) and \(U = 0\).

The state \((x_1, x_2)\), belonging to either side of sliding line, is aimed at the line \(S = 0\) by the controller output \(U\). The control action \(U\), defined as

\[
U = \begin{cases} 
0 & \text{when } S < 0 \\
1 & \text{when } S > 0
\end{cases},
\]

\((8)\)

compels states to hit the sliding line \(S = 0\). To ensure that after hitting the sliding line, the phase portrait continues on the sliding line, the following condition, known as the existence condition \([16–24]\), must be satisfied
\[
\lim_{S \to 0} S \dot{S} < 0. \tag{9}
\]

On entering the sliding zone, the state \(x_1\) follows the trajectory

\[
x_1(t) = x_1(t_0) e^{-\alpha(t-t_0)} \tag{10}
\]
to settle at the origin, where \(t_0\) refers to the instant when the phase portrait first hits the line \(S = 0\). The selection of coefficient \(\alpha\) is based on the requirement of error minimization for the highest frequency component present in the audio signal. Hence, value \(\alpha\), listed in Table 2, is taken such that error minimizes within a quarter cycle of the 20 kHz audio signal. For circuit realization, the switching function, \(S\), is rendered in terms of the circuit parameters as

\[
S = \alpha (v_{\text{ref}} - \beta v_c) + \frac{d}{dt} \left( v_{\text{ref}} - \beta v_c \right). \tag{11}
\]

However, very high differential gain, \(\alpha\), required to realize (11) using op-amps may lead to their saturation [23,25]. Besides very high \(\alpha\), the differentiation of noise and switching components in \(\beta v_c\) leads to noise amplification, which causes poor audio quality. Hence, using (1), the derivative \(\dot{v}_c\) is replaced by \((i_c/C_f)\), and the updated function \(S'\) is given as

\[
S' = \frac{S}{\alpha} = (v_{\text{ref}} - \beta v_c) + \frac{1}{\alpha} \left( \frac{dv_{\text{ref}}}{dt} \right) - \frac{1}{\alpha} \left( \frac{\beta}{C_f} \right) i_c. \tag{12}
\]

The emulated function \(S'\), besides scaling down the differential gain to unity, ensures the realizable gain of other components using the op-amps. Additionally differentiation of the switching frequency signals and noise is also avoided.

The comparator, depicted in Figure 7a, synthesizes the plant input \(U\) to drive the amplifier’s power stage. However, switching devices, such as the transistor and MOSFETs, have finite switching times, which prevent exact synchronization with the comparator output.

To achieve SM operation using finite switching speed devices, the comparator is replaced by a hysteresis band, which, besides assuring quasi-sliding mode operation, also restricts the switching frequency to an arbitrary finite value. The hysteresis block is shown in Figure 7b while the updated switching command is given as

\[
U = \begin{cases} 
0 & \text{when } S < -\Delta h \\
1 & \text{when } S > \Delta h 
\end{cases} \tag{13}
\]

where \(2\Delta h\) is the band gap depicted in Figure 7b. The frequency at which the amplifier switches is given as [22,24]

\[
f = \left( \frac{\beta v_c}{2\alpha \Delta h s L_f C_f} \right) \left( 1 - \frac{v_c}{V_{\text{dc}}} \right) = \left( \frac{v_c}{V_{\text{dc}}} \right) \left( 1 - \frac{v_c}{V_{\text{dc}}} \right). \tag{14}
\]

The capacitor voltage, \(v_c\), which ensures precise command following, is

\[
v_c = \left( \frac{1}{\beta} \right) (v_{\text{ref}}) = v_{\text{bias}} / \beta + \bar{v}_c \tag{15}
\]
where $\tilde{v}_c$ comprises frequency components in audio range. With the consideration of small signal operation, the substitution of (15) in (14) results in (16), which can be split as

$$
\frac{f}{f} = \frac{v_{bias}}{\beta k_c} \left( 1 - \frac{v_{bias}}{\beta V_{dc}} \right) + \frac{\tilde{v}_c}{k_c} \left( 1 - \frac{\beta \tilde{v}_c}{\beta V_{dc}} + 2 \frac{v_{bias}}{\beta V_{dc}} \right)
$$

where $f$ is the quiescent frequency and $\tilde{f}$ denotes excursions around $f$.

Figure 8 depicts the bias point, $(v_n/2, f_n/4)$, and variation of normalized frequency, $f_n$, versus the normalized voltage, $v_n$. The normalized frequency, $f_n$, and normalized voltage, $v_n$, are defined as

$$f = f/f_{nom} \quad \text{where} \quad f_{nom} = V_{dc}/k_c, \quad (17)$$

$$v_n = v_c/V_{dc} \quad (18)$$

respectively. This central biasing [26] helps to achieve the maximum amplitude and the lowest possible THD in the output voltage, for a given set of circuit parameters, which has the additional advantage of ensuring least heating of the speaker voice coil. The HPF filters out the DC voltage from the capacitor voltage, $v_c$, which serves input to the speaker as amplified input voltage, $v_o$.

The parameter values chosen to design the amplifier are tabulated in Table 2.

![Figure 8. Plot of normalized voltage versus frequency.](image)

### Table 2. Amplifier parameters.

| $\alpha$ | $\beta$ | $\Delta h$ | $V_{dc}$ |
|---------|---------|------------|---------|
| $3 \times 10^5$ | 0.2 | 25 mV | 35 V |

3. Hardware Implementation of SMCA

The schematic of SMCA, shown in Figure 9, comprises three blocks, specifically, the signal conditioning stage (SCS), sliding mode technique-based SM controller (SMC) and output power stage (PS). Active and passive elements, such as op-amps, resistors and capacitors, are utilized to realize the SCS and SMC block. The selection criterion of op-amp are the operating voltage, unity gain-bandwidth, slew rate and noise specification, while the selection of passive components is based on operational requirement. A 60 V, 100 W DC power source, N-channel MOSFET, inductor and capacitor are used to develop the power stage of the amplifier. A detailed discussion on selection of MOSFET is presented in this section, while the selection of the inductor and capacitor was already discussed.
Figure 9. Control scheme of the audio amplifier.

A feeble input from an audio source is received by the SCS block. On receiving the audio input, the SCS block pre-amplifies the signal. The function of augmenting the DC bias to a pre-amplified audio signal is performed in this block also. The control operation of the amplifier’s output stage is performed by the SMC block. The arithmetic operations, such as scaling, summing, difference, etc., to realize the SCS and SMC block are performed by op-amp using the fixed-value resistors. The operational details of the SCS and SMC block are given as follows. The SCS block utilizes op-amp SC1, SC2 and SC3 to synthesize the reference signal $v_{\text{ref}}$. The op-amp OPA1632 is chosen to realize SC1. It has a gain bandwidth product of 180 MHz. Increased dynamic range, low input offset voltage and noise immunity are additional features to prefer OPA1632 over the standard op-amp. This op-amp ensures 34 dB single stage gain, $a$, without injecting any significant noise and offset in the output signal.

The selection of the resistances, $R$ and $aR$, to realize gain “$a$” can be done in many ways. The criterion for selecting the gain setting resistor, for the present case, is explained using Figure 10.
Considering a fixed gain of 20 dB, an op-amp based amplification stage is shown in Figure 10a. The gain setting resistor chosen is in the range of tens of ohms, the reason being that the low value of resistance introduces very little thermal noise voltage in the output. The relation between noise voltage, $V_n$, and resistance is given as

$$V_n = \sqrt{\frac{4k_B T B r_a}{r_a}}$$

where $k_B$ is the Boltzmann constant ($=1.34 \times 10^{-23}$), $T$ is the temperature in Kelvin (K), $B$ is the bandwidth in Hz, and $r_a$ is the value of the resistance at 300 K (27 °C) [27]. The effect of parasitic capacitance, $C_p$, is another important consideration for selecting a low resistance value. The parasitic capacitance $C_p$, in order of pF, along with resistances $r_1$ and $r_2$, is shown in Figure 10a. For $r_1 = r_a$, $r_2 = 10r_a$ and $C_p (=1$ pF), Figure 10b depicts gain-phase deviation from the ideal fixed gain over the audio range for low, medium and high values of $r_a$.

As shown in Figure 10b, using gain setting resistors of low values, the op-amp tracks the desired characteristic (20 dB, 0°) well beyond the audio spectrum. However, for high output voltage, $v_o$, gain resistors of low values draw current, $i_2$, of high magnitude, which pass through the feedback resistance $r_2$. The general purpose op-amps have a current sourcing capability of a few mA, which causes the device to overload. Prolonged overloading causes significant power loss and excessive heating of the op-amp, which eventually leads to device failure. Hence, a low value of gain setting resistances is avoided.

Conversely, a very high value (in mega-ohms) of the gain setting resistance leads to significant thermal noise in the input signal of the pre-amplifier. The noisy signal gets amplified by the op-amp effect which has poor input–output linearity. Besides poor linearity, a larger delay between the input–output signal, depicted in Figure 10b, is caused by high gain setting resistances. Because of the problems mentioned above, with a low/high value of the gain setting resistances, a medium value of resistances (in the range of 1–100 KΩ) is chosen here. Advantages of a medium value of resistances are zero phase shift between the input–output signal, shown in Figure 10b, and insignificantly low noise injection in the output signal. The op-amp used to realize amplifier SC2, SC3 is TLE2082, which is a general purpose op-amp. The amplifier SC2 transforms double-ended signal, $a \cdot v_s$, into a single ended signal, $-a \cdot v_s$. Biasing and final amplification of the signal is performed by amplifier SC3. The gain of amplifier SC3 is set at 2. The bias signal, $V_{bias}$, is fixed at $\beta \cdot (V_{dc}/2)$, which ensures biasing of the amplifier at the peak of the normalized frequency versus switching frequency plot, Figure 8.

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**Figure 10.** (a) Op-amp circuit for signal amplification gain “a”. (b) Bode plot of $v_o(s)/v_i(s)$ utilizing low, high and medium values of resistance $r_a$. 

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The signal $v_{ref}$, coming from the SCS block, becomes the input of the SMC block. $v_{ref}$ acts as the reference for SMCA. The amplifier SM1, realized using TLE2082, compares $v_{ref}$ with the feedback signal $\beta \cdot v_c$ to generate error signal, $e$. The signal $\beta \cdot v_c$, fed back to SM1, is sensed using a resistive network, which is placed across voltage $v_c$. The resistors $R_a$ and $R_b$ realize a resistive network, which sets the feedback coefficient, $\beta$, according to (20).

$$\beta = \frac{R_b}{(R_a + R_b)} \quad (20)$$

A high value of the resistances, $R_a$ and $R_b$, is chosen, in the range of 10–100 KΩ, as compared to the loudspeaker load so that the feedback circuit has negligible loading on the amplifier. The scaled differentiation of $v_{ref}$ is performed by the amplifier DEDT. The op-amp used to realize DEDT is OPA4142, an ultra low noise op-amp. The transfer function, $G_{dif}(s)$, of the realized differentiator is

$$G_{dif}(s) = \frac{\tau_\alpha \cdot s}{\tau_d \cdot s + 1} \quad (21)$$

where

$$\tau_\alpha = \frac{1}{\alpha} = R_{d1}C \quad \& \quad \tau_d = R_{d2}C. \quad (22)$$

The frequency response of the ideal and actual differentiator is depicted in Figure 11. The value of components $R_{d1}$ and $C$, listed in Table 3, assure the gain of $(1/\alpha)$ in the audio band.

![Figure 11. Magnitude/Phase versus frequency plot of ideal and practical differentiator.](image)

Another important feature of the realized differentiator is that the high frequency noise is not amplified. To ensure this, the corner frequency ($f_c$) given by

$$f_c = \frac{1}{2\pi \tau_d} \quad (23)$$

of DEDT is kept at 120 kHz. Consequently, a phase deviation of $8^\circ$, from ideal phase lag of $90^\circ$, is observed in the output waveform. The value of $R_{d2}$ to fix $f_c$ at 120 kHz is listed in Table 3.

Table 3. Circuit parameters of SMCA.

| $a$    | $R$   | $R1$    | $R2$    | $Rp$  | $C$   | $R_{d1}$ | $R_{d2}$ | $R_{sh}$ | $V_p$ | $V_{CC}$ |
|--------|-------|---------|---------|-------|-------|----------|----------|----------|-------|----------|
| 34 dB  | 5 KΩ  | 100 Ω   | 2.1 KΩ  | 200 Ω | 1 nF  | 790 Ω    | 1.2 KΩ   | 0.1 Ω    | 5 V   | 15 V     |
Realization of sliding function $S'$ is carried out by amplifier SM2. The sliding function $S'$, re-written as follows, realized is the aggregation of the components coming from op-amp SM1, DEDT and IA, respectively, by the adder circuit:

$$S' = (v_{ref} - \beta v_c) + \frac{1}{\alpha} \left[ \frac{dv_{ref}}{dt} \right] - \frac{1}{\alpha} \left[ \frac{\beta}{C_f} \right] i_c. \quad (24)$$

The aggregation function is performed by the adder circuit, which utilizes op-amp TLE2082 to realize SM2 and resistors, $R$. As already discussed, SM1 supplies error, $e$, whereas scaled differentiation signal $a^{-1} \cdot (dv_{ref}/dt)$ is provided by op-amp DEDT. The third component of sliding function $S'$ is provided by the instrumentation amplifier (IA). The functioning of amplifier IA is discussed later. The output signal, $S'$, of op-amp SM2 is applied to comparator H. The inverting terminal, of the comparator H, is connected to signal $S'$, while the non-inverting terminal is connected with a voltage feedback network, which sets the input limit of hysteresis band. Unlike the standard op-amp configured as a comparator, a dedicated comparator IC, with very low response time and high voltage gain is used to compare signal, $S'$, with the hysteresis band. The comparator H, which is a high speed, open collector comparator, uses an external pull up resistor, $R_p$, to drive the high level state at the desired voltage, $V_h$. The output of the comparator, H, is the control signal, $U$, the binary levels of which are 0 and $V_b$ volts. The relationship among comparator parameters and hysteresis band, $2\Delta h$, is given as

$$2\Delta h = \frac{R_1 \cdot V_b}{R_1 + R_2 + R_p}, \quad (25)$$

and the parameters to render the hysteresis band of 50 mV are listed in Table 3.

The control signal $U$ is then applied to the gate driver. The driver chosen, IC IRS20124, is capable of driving power MOSFETs arranged in a half bridge configuration. Selectable dead time and over-current protection of the switch are inherent features of the gate driver IC. A 45 ns dead time was opted for in the present application. By choosing the recommended value of the resistors selected, dead time was implemented. On receiving control signal $U$, the driver IC generated pulse $G$ and complementary pulse $\bar{G}$ to drive high and low side MOSFETs in the power stage.

The power stage, PS, constitutes the DC source $V_{dc}$, MOSFETs $S_1$ and $S_2$ and filter network, BPF, formed by aggregating HPF and LPF. The corner frequency and selection of passive components to render high/low pass filter were already discussed. The explanation to realize third component of the sliding function $S'$, (24), is given here. The op-amp INA111BU, an instrumentation amplifier (IA), is specifically chosen to realize scaled current $(\frac{\beta}{\alpha} C_f) i_c$. The voltage across shunt resistor $R_{sh}$, which is placed in the path of current $i_c$, replicates the down-scaled current $i_c$. The IA amplifies the voltage across the shunt resistor, $R_{sh}$, by a fixed gain, $G$, to realize the desired component of $S'$ [21]. To ensure desired gain $G$, of the instrumentation amplifier, an external resistor $R_g$ is chosen in accordance with the following condition.

$$G = 1 + \frac{50 \times 10^3}{R_g}. \quad (26)$$

MOSFET selection is based on the criterion of maximum efficiency. For this purpose, the computation of efficiency, $(\eta)$, for available devices having equal drain to source breakdown voltage ($BV_{DSS}$) is performed as follows

$$\eta = \frac{P_1}{P_{con} + P_{sw} + P_g + P_L}. \quad (27)$$

$P_{con}$, $P_{sw}$, $P_g$ and $P_L$ in (27) denote conduction loss, switching loss, gate driver loss and load component, respectively. The test condition for efficiency calculation is listed in Table 4 [21].
Table 4. Test condition to evaluate efficiency, $\eta$ [21].

| Parameter          | Condition |
|--------------------|-----------|
| $V_{dc}$           | 35 V      |
| $I_o$              | 2.5 A     |
| Power              | 20 W      |
| Frequency ($f_{sw}$) | 400 (kHz) |

The conduction loss, $P_{cond}$, is calculated as

$$P_{cond} = I_o^2 \times R_{ds(on)}$$  \hspace{1cm} (28)

where $R_{ds(on)}$ is the drain source on the resistance of the MOSFET, while the switching loss $P_{sw}$, (29), has three loss components. The first loss component is due to the finite turn on/off, $t_r/\tau_f$, time of the MOSFET, while the second loss component is associated with the charging of the output capacitor, $C_{oss}$. The third loss component is because of the reverse recovery charge, $Q_{rr}$, of the MOSFET body diode.

$$P_{sw} = 0.5I_o V_{dc}(t_r + \tau_f)f_{sw} + 0.5C_{oss}V_{dc}^2 f_{sw} + 0.5Q_{rr} V_{dc} f_{sw}$$  \hspace{1cm} (29)

The gate power loss, at the gate driver operating voltage, $V_{CC}$, listed in Table 3, is calculated as

$$P_{gate} = 2 \cdot Q_S \cdot V_{CC} \cdot f_{sw}$$  \hspace{1cm} (30)

where $Q_S$ is the charge required by the gate to fully turn on the MOSFET. Based on the operating condition given in Table 4, the loss components, total loss and efficiency, $\eta$, of the available devices are listed in Table 5.

Table 5. Loss components and efficiency of the various switching MOSFETs [21].

| MOSFET          | Conduction Loss (W) | Switching Loss (W) | Gate Loss (W) | Total Loss (W) | $\eta$ (%) |
|-----------------|---------------------|--------------------|---------------|----------------|------------|
| IRFI4212H-117   | 0.453               | 0.628              | 0.144         | 1.225          | 94.2       |
| IRFI6644        | 0.081               | 1.276              | 0.420         | 1.778          | 91.8       |
| IRFI6645        | 0.219               | 0.481              | 0.168         | 0.86           | 95.8       |
| IRFB4212        | 0.453               | 1.057              | 0.180         | 1.690          | 92.2       |

On the basis of percentage efficiency, listed in Table 5, the IRFI6645 is the most appropriate device for this application. Despite the advantage of high efficiency, the miniaturized footprint of IRFI6645 hinders the mounting of the device on the printed circuit board (PCB). Hence the IRFI4024H-117P, second most efficient device in the Table 5, available in the 5 pin through-hole package, is chosen to fabricate the power stage [21]. In addition to ease in the device mounting, the half bridge configuration of the two n-channel MOSFET in IRFI4024H-117P ensures enhanced noise immunity and compact PCB layout. The greatest advantage of selecting IRFI4024H-117P is no requirement of the heat sink for the presented design.

The power stage is cascaded with the filter network to render the output stage of the amplifier. The controller produces the complementary gate pulses, $G$ and $\bar{G}$, to switch the devices, S1 and S2, on and off [21]. The switching action of devices resulted in pulse train, $v_l$. The voltage $v_l$, a pulse density modulated signal, has a binary level. The high level (HL) equals source voltage $V_{dc}$, while the low level equalizes with the system ground. The amplifier output $v_o$, extracted from $v_l$ using the BPF, drives the loudspeaker system.

4. Performance of SMCA with R-Load

Photograph of the experimental set-up which includes amplifier, load, power supply, input signal source and measuring instruments is shown in Figure 12. Overall, three sets
of experiments were performed; among them, the 1st set was conducted to evaluate the amplifier’s signal amplification performance. The robustness property of the amplifier was evaluated by the 2nd set of experiments, whereas the disturbance rejection property was probed using the 3rd set of experiments. Details of each set of experiment are given as follows.

For the first set of experiments, the desired voltage gain of the amplifier was fixed at 28 dB. A 4 \(\Omega\), 100 W resistor was used to load the amplifier during these tests. Verification of the amplifier’s gain was done by recording the input–output voltage waveform at 1 kHz. Figure 13a depicts \(v_s\) and \(v_o\) waveforms at the 1 W power level. The observed gain is 28.6 dB, which is very close to the desired gain, while a phase shift of \(-3.15^\circ\) highlights the amplifier’s impressive command following. Figure 13b depicts the input–output linearity using the frequency spectrum of the output \(v_o\). Clearly, every harmonic component in the \(v_o\) spectrum is attenuated to a magnitude lower than 40 dB of the fundamental component, which validates the excellent input–output linearity.

For the second set of experiments, the voltage waveform and frequency spectrum plot of \(v_o\) at frequency 200 Hz and 8 kHz are also presented. Figure 14a depicts
the time domain performance of the amplifier at 200 Hz, for which the gain and phase lag are 28.8 dB and 4°, respectively. The frequency spectrum is given in Figure 14b, which depicts well-attenuated harmonic components.

Figure 14. (a) $v_s$ and $v_o$ waveforms at 200 Hz: $v_o$ (1 volt/div), $v_s$ (0.1 volt/div), timescale: (1 microsecond/div) (b) frequency spectrum of 200 Hz output voltage.

The input–output voltage waveform at 8 kHz is depicted in Figure 15a, the performance metrics are 28.1 dB and $-33.3^\circ$. The harmonic spectrum of $v_o$ at 8 kHz is given in Figure 15b which confirms minimal noise in the output signal. Besides faithful amplification, high linearity of the output signal is evident from these experiments since harmonic components are attenuated to below $-40$ dB level of the fundamental component.

Figure 15. (a) $v_s$ and $v_o$ waveforms at 8 kHz: $v_o$ (1 volt/div), $v_s$ (0.1 volt/div), timescale: (50 microsecond/div) (b) frequency spectrum of 8 kHz output voltage.

To validate the command following over the entire audio band, a frequency response test was performed. In this test, the frequency of the input signal monotone was swept from 20 Hz to 20 kHz. A schematic of the sweep test is given in Figure 16a. The frequency response analyzer (FRA) sweeps the frequency of the input signal $v_s$, while keeping its amplitude constant. The input ($v_s$), output ($v_o$) and frequency data are recorded throughout the sweep. The gain-phase plot of the acquired data is shown in Figure 16b. Clearly, the observed gain of 28.6 dB is in close approximation with the desired value of 28 dB. However, the phase plot reveals the frequency-dependent delay in signal $v_o$. Excluding the delay, these plots justify the admirable command following by the amplifier.
To further evaluate linearity of the amplifier, the total harmonic distortion (THD) of the output signal $v_o$, at 1 W power level, in the 1–10 kHz range was calculated and plotted. Since the amplifier’s input signal, $v_s$, itself contains harmonic components, an algorithm to accurately calculate the THD of the output signal, $v_o$, is developed, which is illustrated in Figure 17. Notations used in the algorithm are explained in Table 6.

![Algorithm for THD calculation](image)

**Figure 17. Algorithm for THD calculation.**
Table 6. Description of the notations in THD algorithm.

| Notation | Description |
|----------|-------------|
| \( n \)  | component number, \( n = 1, 2, 3, 4 \ldots \leq 20 \) |
| \( n = 1 \) | fundamental component |
| \( n = 2, 3, \ldots \) | harmonic component |
| \( i \) | harmonic number, \( i = 2, 3, 4, \ldots \leq 20 \) |
| \( v_{s_n} \) | \( n \)th component in frequency spectrum of \( v_s \) |
| \( v_{o_n} \) | \( n \)th component in frequency spectrum of \( v_o \) |
| \( a \) | Gain of fundamental component |
| \( v_{oh_i} \) | Adjusted \( i \)th harmonic of \( v_o \) |

The frequency spectrum of the input and output voltage, \( v_s \) and \( v_o \), respectively, are recorded from the scope. Using the gain \( a \), given as

\[
a = \frac{v_{o1}}{v_{s1}},
\]

the harmonic component, \( v_{oh_i} \) (here, \( i \) ranges from \( i = 2, 3, 4 \ldots \) to \( i \leq 20 \)), in the output voltage, \( v_o \), is calculated as given in Figure 17. Negative components of \( v_{oh_i} \) are replaced by a small positive number (=0.005). Loops shown in Figure 17 ensure updated values of the harmonic components, \( v_{oh_i} \), which the THD uses, given as

\[
THD(\%) = \sqrt{\frac{(v_{oh_2})^2 + (v_{oh_3})^2 + \ldots}{v_{o1}}},
\]

of the output voltage is calculated. The graph of THD versus frequency is depicted in Figure 18. THD well below 1% is observed, within the audio spectrum, which signifies excellent input-output linearity.

![Figure 18. THD (%) at 1 W.](image)

The amplifier’s performance at the peak load is demonstrated in Figure 19.
The input–output waveform, Figure 19a, and frequency spectrum plot of $v_o$, depicted in Figure 19b, establishes an excellent command following and linearity of the amplifier.

To validate the linearity of the amplifier with actual musical signal, the input, $v_s$, to output, $(i_o)$, response with the 4 Ω loudspeaker load is given in Figure 20. Since the audio output of the loudspeaker is directly proportional to the speaker current [28,29], thus, the load current, $i_o$, is taken as the output parameter. Two distinct samples of experimentally obtained speaker current, $i$, in response to the two arbitrary audio reference signals, $v_o$, are shown in Figure 20a,b, respectively.
To evaluate linearity among $v_s-i_o$ quantitatively, the metric sample correlation coefficient $r_{sm}$, defined as

$$r_{sm} = \frac{s_{xy}}{s_x s_y} \quad (33)$$

is used, where $s_x$ and $s_y$ are the standard deviations of the input ($v_s$) and output ($i_o$) signals, and $s_{xy}$ is their covariance [30].

The correlation coefficients, $r_{sm}$, of these two samples, along with three more distinct samples, are given in Table 7. The mean value of $r_{sm}$ over all the sample signals is also stated in the table, which reveals that 82% of the input audio is faithfully converted into acoustic signal.

| Sample No. | 1   | 2   | 3   | 4   | 5   |
|------------|-----|-----|-----|-----|-----|
| $r_{sm}$   | 0.80| 0.82| 0.83| 0.81| 0.82|
| Mean($r_{sm}$) |     |     |     |     | 0.816 |

The efficiency plot of the amplifier, in useful audio range, is shown in Figure 21. The test was carried out at peak loading condition; the result obtained exhibited efficiency in the range of 55% to 75%. Efficient performance of amplifier occurred in the frequency range of 500 Hz to 5 kHz.

![Figure 21. Efficiency versus frequency plot at 20 W loading.](image)

In the second set of experiments, the robustness property was investigated by applying a step change in the amplifier loading. Figure 22a depicts the waveform $v_s, v_o$ and $i_o$ when subjected to load increment, from 11 W to 14 W (roughly 25% of load addition). Evidently, $v_o$ is unaffected by incremental loading. In addition, Figure 22b depicts the waveform when the amplifier is relaxed by reducing the load from 20 W to 16 W. Undoubtedly, the amplifier output voltage, $v_o$, remains unaffected from load reduction too.

Amplifier’s disturbance rejection property was validated using the third set of experiments. The scheme for the test is depicted in Figure 23.

The single phase bridge rectifier with relatively small capacitor $C_{dc}$ (=10 µF) was chosen as power source ($V_{dc}$) of the amplifier. The DC output voltage of this provisional supply contains ±10% ripple in the output voltage. The frequency spectrum of the source is plotted in Figure 24, which depicts the presence of 100 Hz, 200 Hz, ..., components in the DC voltage source.
Figure 22. $v_s$, $v_o$ and $i_o$ waveform: $v_s$ (0.5 Volt/div), $v_o$ (10 volt/div), $i_o$ (2 amp/div). (a) Incremental loading of amplifier, timescale: (500 micro-second/div). (b) Decremental loading of amplifier, timescale: (1 milli-second/div).

Figure 23. Disturbance rejection test setup.

Figure 24. FFT plot of power source, $v_o$. 
The harmonic component of power source resemble as disturbance signal to the amplifier. To validate the disturbance rejection property of the amplifier, the experiment was performed at 1 W at the 1 kHz level. The captured waveforms are depicted in Figure 25a.

![Waveforms for PSR test.](a)

Figure 25. (a) Waveforms for PSR test. (b) FFT plot of $v_o$.

From the FFT plot of $v_o$, Figure 25b, it is confirmed that the disturbance component present in the source imparts a negligible impact on the output voltage. The 100 Hz component of $v_o$ is curtailed at the $-35$ dB level, while other components (200 Hz, 300 Hz, . . .) are attenuated to an even lower level, with a 1 kHz reference audio signal. This shows the superior power supply disturbance rejection quality of the amplifier.

5. Concluding Remark

A systematic approach to develop a 20 W SM control based switch mode audio amplifier is presented. The functioning of each constituent block in the amplifier, design methodology and selection of components are discussed in sufficient detail. With an emphasis on the analog realization of the SM controller, the theoretical and practical aspects of design, such as the selection of sliding coefficient $\alpha$, realization of viable sliding surface $S$ using active and passive components, selection/realization of hysteresis band, deciding the optimal biasing point of the amplifier, etc., are discussed thoroughly. On the basis of the presented design, a 20 W lab prototype is developed. The fabricated amplifier is tested extensively with 4 \( \Omega \) resistive load. The linearity, robustness and disturbance rejection property of the amplifier are tested. All the results obtained exhibit a high degree of performance to qualify for the high quality audio amplification. With the coil type loudspeaker as the load, the actual musical signal test is conducted on the amplifier, which reveals 82% correlation between the input audio signal and loudspeaker driving current. Further enhancement in the input–output correlation would surely increase the audio quality of audio system.

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