DEDICATED FRONT-END AND READOUT ELECTRONICS DEVELOPMENTS FOR REAL TIME 3D DIRECTIONAL DETECTION OF DARK MATTER WITH MIMAC.

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Abstract. A complete dedicated electronics, from front-end to back-end, was developed to instrument a MIMAC prototype. A front end ASIC able to monitor 64 strips of pixels and to provide their individual “Time Over Threshold” information has been designed. An associated acquisition electronics and a real time track reconstruction software have been developed to monitor a 512 channel prototype. This auto-triggered electronic uses embedded processing to reduce the data transfer to its useful part only, i.e. decoded coordinates of hit tracks and corresponding energy measurements. The electronic designs, acquisition software and the results obtained are presented.

1 Introduction

Directional detection of dark matter is known to be a promising search strategy of galactic Dark Matter (Spergel et al. 1988, Ahlen et al. 2010). Recent studies have shown that, within the framework of dedicated statistical data analysis, a low exposure directional detector could lead either to a high significance discovery of galactic Dark Matter (Billard et al. 2010, Billard et al. 2011) or to a conclusive exclusion (Billard et al. 2010).

A gaseous micro-TPC matrix, filled with either $^3$He, CF$_4$ or C$_4$H$_{10}$ has been developed within the MIMAC project (Santos et al. 2007). To demonstrate the relevance of the concept, specific front-end ASIC and a dedicated acquisition electronic were developed in order to equip a prototype detector featuring an anode of 10.85 x 10.85 cm$^2$ where 2 x 256 strips are monitored. This auto-triggered acquisition electronic uses embedded processing to reduce data transfer to its useful
part only, i.e. decoded coordinates of hit tracks and corresponding energy measurements. To be fully exploited, an acquisition software with on-line monitoring and track reconstruction has been written.

This paper is organized as follows: section 2 presents the detector and its readout principle, section 3 describes the front end ASIC developed for MIMAC. Section 4 describes the acquisition board and the algorithm embedded in the FPGA. Finally, the acquisition software and the on-line 3D reconstruction strategy are presented in section 5. Eventually, a short summary is given in section 6.

2 MIMAC detector readout principle

As shown in fig. 1, the MIMAC prototype µTPC is composed of a pixelized anode featuring 2 orthogonal series of 256 strips of pixels (X and Y) (Iguaz et al. 2011) and a micromesh grid defining the delimitation between the amplification (grid to anode) and the drift space (cathode to grid). Each strip of pixels is monitored by a current preamplifier and the fired pixel coordinate is obtained by using the coincidence between the X and Y strips (the pixel pitch is 424 µm). A coincidence is defined as having at least one strip of pixels fired in each direction (X, Y) at the same sampling time. The ionization energy of the recoil energy is obtained by instrumenting the micromesh grid with a Charge Sensitive Pre amplifier (CSP).

As illustrated in fig. 2 the coordinates in the anode plane (X, Y) are reconstructed by collecting primary electrons produced in the drift region. Knowing the electron drift velocity, the third dimension (Z) is obtained by sampling the anode
signal every 20 ns. Note, that due to the multiplexed readout of the anode, each time slice picture is rectangular.

Fig. 2. The coordinates in the anode plane (X, Y) are reconstructed by collecting primary electrons produced in the drift region. Knowing the electron drift velocity, the third dimension (Z) is obtained by sampling the anode signal every 20 ns. Due to the multiplexed readout of the anode, each time slice picture is rectangular.

3 Front end ASIC

3.1 Requirements

In the early stage of the project it was decided to design an ASIC in order to be able to fulfill the final objective, which is to equip about 2500 chambers of 1024 strips of pixels (512+512). This minimizes space requirement and power demand and allows cost reduction on a large scale. After going through a first prototype phase, 16 channels ASICs equipping a $2 \times 96$ strips of pixels chamber (Richer et al. [2010]), a 64 channel version was designed. This was determined to be a good balance between integration scale on one side and complexity, fabrication yield and available packages on the other side.

To be able to recover the third coordinate (Z) of the track, a fast switching current comparator having a threshold as low 200 nA must be designed in order to have a precise time over threshold measurement of each current preamplifier output. This requirement is driven by the worst case where the recoil energy is as low as 500 eV in a chamber having its gain limited to 3000 and where the diffusion is maximized (i.e interaction at the farthest of the anode) and the recoil track is parallel to the anode (the charge deposit is distributed along different strips). Another strong system requirement is to minimize the board level interconnection to allow an easy integration with a readout system.
3.2 Design details

The front end ASIC, whose block diagram is shown in fig. 3, is composed of 4 groups of 16 channels. Each channel is composed of a current preamplifier having a gain of 15, a fast comparator (modified CMOS inverter kept in linear region) and a 5 bit DAC for setting the threshold. A trade-off was made between the DAC resolution and the achievable preamplifier offset. The DAC dynamic range, and thus its design complexity can be greatly reduced by using an autozero preamplifier. This kind of amplifier measures periodically (every second) its offset during a few dozen µs and determines the compensation to apply to reduce the residual output offset. The 5 bit DAC is designed with a 200 nA LSB (input equivalent: 13.3 nA).

The comparator outputs are sampled at a 50 MHz rate and serialized at 400 MHz, thereby reducing the interconnection by a factor of 8 and diminishing the power consumption. The serial outputs rely on the Low Voltage Differential Signaling (LVDS) standard to lower the electronic noise. It should be noted that using the same reference clock allows synchronous sampling between ASICs.

A slow serial link is used to configure the 64 DACs and to individually enable/disable each channel (kill eventual dead channels, ...).

The ASIC was fabricated in AMS SiGe CMOS 0.35 µm and has surface of 3.9 mm x 5.8 mm = 22 mm². It uses a total power of 445 mW (110 mA @ 3.3 V, 55 mA @ 1.5 V).

Fig. 4 shows the typical DAC threshold and minimal threshold dispersion over one representative ASIC, where the latter is determined by recording the current pulse amplitude required to trigger a channel at a fixed DAC setting. The

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**Fig. 3.** Front end ASIC block diagram. The 64 channels are decomposed in 4 groups of 16 channels. Each channel is composed of a current preamplifier having a gain of 15, a fast comparator (modified CMOS inverter kept in linear region) and a 5 bit DAC for setting the threshold. A serial link is used to configure the DAC. The comparator outputs are transferred serially.
O. Bourrion: MIMAC electronics

Fig. 4. Typical DAC threshold and minimal threshold dispersion over one representative ASIC.

plot shows that the DAC levels are totally homogeneous but that the effective thresholds have a few spikes remaining. This is explained by the offset correction efficiency dispersion between channels, which in turn has an influence on the minimum signal detected at a given threshold.

4 Readout electronics

4.1 Electronic board overview

The readout electronic, which is an upgrade of a previous work (Bourrion et al. 2010), comprises 8 dedicated ASICs, a FPGA, a flash ADC and an USB interface for DAQ and slow control (see fig. 5). The connection between the anode located inside the chamber and the electronics at ambient pressure is done via an airtight interface (Igaz et al. 2011). Each strip input is equipped with a discharge protection. The hit strip information, that is sampled at a rate of 50 MHz, is transferred by 8 LVDS serial links at 400 MHz to a unique processing FPGA. This FPGA allows the auto-triggering and does the first level event building.

In parallel to the anode signal processing, the grid signal is fed to flash ADC and sampled at 50 MHz. While keeping a very good energy resolution, an estimation of the charge deposit through time can be obtained off-line by deriving the digitized CSP signal.

The board has a dimension of 25 cm × 25 cm and uses 9.4 W in operation.

4.2 FPGA firmware

As shown in fig. 6 the FPGA deserializes the data received from the ASIC and for each group of 16 channels a local trigger is built (OR). The first level processing starts at this stage, i.e. when a coincidence exists between X and Y strips, a
Fig. 5. Block diagram of the acquisition board. It comprises 8 dedicated ASICs, a FPGA, a flash ADC and an USB interface for DAQ and slow control interface.

Fig. 6. Block diagram of the ASIC interface. It comprises the data deserializer, the local trigger building, intermediate buffering and the first level processing.

local recording takes place (start date + positions). In theory, a single event would be defined as continuously firing strips. Unfortunately, the primary electron distribution can be noncontinuous, therefore untriggered strips can split the track (clusters). To cope with this, the recording is actually stopped when there are no more fired strips for a preset number of clock cycles.

Most of the time a few strips only are fired, hence by using an adequate data encoding (shown in table 1), the data payload per event can be reduced. For instance, when 2 strips in X and 2 strips in Y are fired in the same time slice, taking advantage of the encoding, only 64 bit are transferred instead of 512. This
Table 1. Position data encoding.

| Bit # | [15..13] | 12 | [11..10] | [9..8] | [7..4] | [3..0] |
|-------|----------|----|----------|-------|-------|-------|
| Content | 0 | X or Y | ASIC# | Group# | 0 | ch# |

The first encoding and processing stage is done in parallel for the X and Y side. At the following stage, dedicated state machines search and aggregate data from the same time slice in order to perform the first level event building. This association is done in several stages, in order to concentrate more and more the data, and to present a single buffer to the USB interface.

The energy measurement is done in parallel to the position processing. The CSP signal recording is armed by the position triggering, but given the fact that the signal path delay is different for the anode and the grid signal, the actual recording is performed when the grid integrated signal is digitized. As a consequence of the low level signal compared to the noise level, a slope condition, which is more robust and noise immune than using a simple level threshold, is used. Taking advantage of the FPGA, dedicated filtering techniques are implemented (CIC and FIR filters) to further enhance the signal to noise ratio without degrading the event signal shape.

Consequently to the parallel processing, the position and energy data are recorded in separate FIFOs for USB readout.

5 Acquisition software

The first task of the acquisition software is to re-associate the position and the energy data. It uses the position information which is provided in a list of X/Y coordinates fired per time slice. Knowing that an event is defined as continuously triggering strips, the algorithm basically searches continuous triggering position (in time) and searches a discontinuity (time tag jumps by more than the preset value) to close the event. Once the event is defined, the energy information with a corresponding time tag is associated. The event building is then finished and contains directly the coordinates of the fired strips coordinate for each time slice and the corresponding digitized grid signal.

The second task of the acquisition software is to provide a real time display (see fig. 7). The Graphical User Interface (GUI) provides 3 projections of the track (XY-XZ-YZ), the number of fired strips per time slice, the Track CSP digitized signal and its derivative. It also offers the possibility to search (energy, duration, ...) and display a specific recoil track. An energy histogram of the run is also built on line and displayed on an other tab (not shown in fig. 7).

6 Summary

A complete dedicated solution from front-end to back-end was developed to instrument a MIMAC prototype (256 × 256). Several MIMAC electronics can be
Fig. 7. Screenshot of the real time display. The 3 projections of the track (XY-XZ-ZY), the number of fired strips per time slice, the grid digitized signal and its derivative can be seen.

connected per computer and the event building developed can be performed in several stages provided a common time tagging electronic board is designed and a synchronization upgrade is implemented.

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