A High Throughput List Decoder Architecture for Polar Codes

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Abstract—While long polar codes can achieve the capacity of arbitrary binary-input discrete memoryless channels when decoded by a low complexity successive cancelation (SC) algorithm, the error performance of the SC algorithm is inferior for polar codes with finite block lengths. The cyclic redundancy check (CRC) aided successive cancelation list (SCL) decoding algorithm has better error performance than the SC algorithm. However, current CRC aided SCL (CA-SCL) decoders still suffer from long decoding latency and limited throughput. In this paper, a reduced latency list decoding (RLLD) algorithm for polar codes is proposed. Our RLLD algorithm performs the list decoding on a binary tree, whose leaves correspond to the bits of a polar code. In existing SCL decoding algorithms, all the nodes in the tree are traversed and all possibilities of the information bits are considered. Instead, our RLLD algorithm visits much fewer nodes in the tree and considers fewer possibilities of the information bits. When configured properly, our RLLD algorithm significantly reduces the decoding latency and hence improves throughput, while introducing little performance degradation. Based on our RLLD algorithm, we also propose a high throughput list decoder architecture, which is suitable for larger block lengths due to its scalable partial sum computation unit. Our decoder architecture has been implemented for different block lengths and list sizes using the TSMC 90nm CMOS technology. The implementation results demonstrate that our decoders achieve significant latency reduction and area efficiency improvement compared with other list polar decoders in the literature.

Index Terms—polar codes, successive cancelation decoding, list decoding, hardware implementation, low latency decoding

I. INTRODUCTION

Polar codes [3] are a significant breakthrough in coding theory, since they can achieve the channel capacity of binary-input symmetric memoryless channels [3] and arbitrary discrete memoryless channels [4]. Polar codes of block length $N$ can be efficiently decoded by a successive cancelation (SC) algorithm [3] with a complexity of $O(N \log N)$. While polar codes of very large block length ($N > 2^{20}$ [5]) approach the capacity of underlying channels under the SC algorithm, for short or moderate polar codes, the error performance of the SC algorithm is worse than turbo or LDPC codes [6].

Lots of efforts [6]–[8] have already been devoted to the improvement of error performance of polar codes with short or moderate lengths. An SC list (SCL) decoding algorithm [6] performs better than the SC algorithm. In [6]–[8], the cyclic redundancy check (CRC) is used to pick the output codeword from $L$ candidates, where $L$ is the list size. The CRC-aided SCL (CA-SCL) decoding algorithm performs much better than the SCL decoding algorithm at the expense of negligible loss in code rate.

Despite its significantly improved error performance, the hardware implementations of SC based list decoders [9]–[13] still suffer from long decoding latency and limited throughput due to the serial decoding schedule. In order to reduce the decoding latency of an SC based list decoder, $M$ ($M > 1$) bits are decoded in parallel in [14]–[16], where the decoding speed can be improved by $M$ times ideally. However, for the hardware implementations of the algorithms in [14]–[16], the actual decoding speed improvement is less than $M$ times due to extra decoding cycles on finding the $L$ most reliable paths among $2^M L$ candidates, where $L$ is list size. A software adaptive SSC-list-CRC decoder was proposed in [17]. For a (2048, 1723) polar+CRC-32 code, the SSC-list-CRC decoder with $L = 32$ was shown to be about 7 times faster than an SC based list decoder. However, it is unclear whether the list decoder in [17] is suitable for hardware implementation.

In this paper, a tree based reduced latency list decoding algorithm and its corresponding high throughput architecture are proposed for polar codes. The main contributions are:

- A tree based reduced latency list decoding (RLLD) algorithm over logarithm likelihood ratio (LLR) domain is proposed for polar codes. Inspired by the simplified successive cancelation (SSC) [18] decoding algorithm and the ML-SSC algorithm [19], our RLLD algorithm performs the SC based list decoding on a binary tree. Previous SCL decoding algorithms visit all the nodes in the tree and consider all possibilities of the information bits, while our RLLD algorithm visits much fewer nodes in the tree and considers fewer possibilities of the information bits. When configured properly, our RLLD algorithm significantly reduces the decoding latency and hence improves throughput, while introducing little performance degradation.

- Based on our RLLD algorithm, a high throughput list decoder architecture is proposed for polar codes. Compared with the state-of-the-art SCL decoders in [10], [12], [15], our list decoder achieves lower decoding latency and higher area efficiency (throughput normalized by area).

More specifically, the major innovations of the proposed decoder architecture are:

- An index based partial sum computation (IPC) algorithm is proposed to avoid copying partial sums directly when one decoding path needs to be copied to another. Compared with the lazy copy algorithm in [6], our IPC algorithm is more hardware friendly since it copies only
path indices, while the lazy copy algorithm needs more complex index computation.

- Based on our IPC algorithm, a hybrid partial sum unit (Hyb-PSU) is proposed so that our list decoder is suitable for larger block lengths. The Hyb-PSU is able to store most of the partial sums in area efficient memories such as register file (RF) or SRAM, while the partial sum units (PSUs) in [9], [10], [12] store partial sums in registers, which need much larger area when the block length in larger. Compared with the PSU of [10], our Hyb-PSU achieves an area saving of 23% and 65% for block length $N = 2^{13}$ and $2^{15}$, respectively, under the TSMC 90nm CMOS technology.

- For our RLLD algorithm, when certain types of nodes are visited, each current decoding path splits into multiple ones, among which the $L$ most reliable paths are kept. In this paper, an efficient path pruning unit (PPU) is proposed to find the $L$ most reliable decoding paths among the split ones. For our high throughput list decoder architecture, the proposed PPU is the key to the implementation of our RLLD algorithm.

- For the fixed-point implementation of our RLLD algorithm, a memory efficient quantization (MEQ) scheme is used to reduce the number of stored bits. Compared with the conventional quantization scheme, our MEQ scheme reduces the number of stored bits by 17%, 25% and 27% for block length $N = 2^{10}$, $2^{13}$ and $2^{15}$, respectively, at the cost of slight error performance degradation.

Note that the SSC and ML-SSC algorithms reduce the decoding latency by first performing it on a binary tree and then pruning the binary tree. Inspired by this idea, our RLLD algorithm performs the SC based list decoding algorithm on a binary tree. The low-latency list decoding algorithm [17] also performs the list decoding algorithm on a binary tree. Our work [1] and the decoding algorithm in [17] are developed independently. While both our RLLD algorithm and the low-latency list decoding algorithm in [17] visit fewer nodes in the binary tree so as to reduce the decoding latency, there are some differences:

- Compared with the decoding algorithm in [17], our RLLD algorithm visits fewer nodes. Illuminated by the ML-SSC algorithm, our RLLD algorithm processes certain arbitrary rate nodes [18] in a fast way.

- When a rate-1 node [18] is visited, our RLLD algorithm employs a less complex and hardware friendly algorithm to compute the returned constituent codewords.

- Our RLLD algorithm is based on LLR messages, while the algorithm in [17] is based on logarithm likelihood (LL) messages, which require a larger memory to store.

In terms of hardware implementations, compared with state-of-the-art SC list decoders [9], [10], [12], [13], [15], [16], our high throughput list decoder architecture shows advantages in various aspects:

- For the high throughput list decoder architecture, LLR message is employed while LL message was used in [9], [10], [15], [16]. The LL based memories require more quantization bits and a larger memory to store. The area efficient memory architecture in [10] is employed to store all LLR messages. LLR messages were also employed in [12], [13]. However, the register based memories in [12], [13] suffer from excessive area and power consumption when $N$ is large.

- Our list decoder architecture employs a Hyb-PSU, which is scalable for polar codes of large block lengths. The register based PSUs of the list decoders in [9], [10], [12] suffer from area overhead when the block length is large. Instead of copying partial sums directly, our scalable PSU copies only decoding path indices, which avoids additional energy consumption.

Note that the SSC and ML-SSC algorithms reduce the decoding latency at the cost of certain performance degradation. In contrast, existing SC list decoders in [6], [13] usually selects the $L$ most reliable candidates.

The rest of the paper is organized as follows. Related preliminaries are reviewed in Section II. The proposed RLLD algorithm is presented in Section III. The high throughput list decoder architecture is presented in Section IV. In Section V the implementation and comparisons results are shown. At last, the conclusion is drawn in Section VI.

II. PRELIMINARIES

A. Polar Codes

Let $u_0^{N-1} = (u_0, u_1, \ldots, u_{N-1})$ denote the data bit sequence and $x_0^{N-1} = (x_0, x_1, \ldots, x_{N-1})$ the corresponding codeword, where $N = 2^n$. Under the polar encoding, $x_0^{N-1} = u_0^{N-1}B_NF^{n-1}$, where $B_N$ is the bit reversal permutation matrix, and $F = \begin{bmatrix} 1 & 1 \\ 1 & 0 \end{bmatrix}$. Here $\otimes$ denotes the $n$th Kronecker power, $F^{n-1} = F \otimes F^{(n-1)}$ and $F^{0} = 1$. For $i = 0, 1, \ldots, N-1$, $u_i$ is either an information bit or a frozen bit, which is set to zero usually. For an $(N, K)$ polar code, there are a total of $K$ information bits within $u_0^{N-1}$. The encoding graph of a polar code with $N = 8$ is shown in Fig. 1.

B. Prior Tree-Based SC Algorithms

A polar code of block length $N = 2^n$ can also be represented by a full binary tree $G_n$ of depth $n$ [18], where each node of the tree is associated with a constituent code. For example, for node 1 shown in Fig. 2 the correspondent constituent code is the set $\{(s_{20}, s_{22}, s_{24}, s_{26})\}$, where each
From the root node, all nodes in a tree are activated in a recursive way for the SC algorithm. Once \( \beta_v \) for the last leaf node is generated, the codeword \( x_v^{N-1} \) can be obtained by combining and propagating \( \beta_v \) up to the root node.

The SSC decoding algorithm in [18] simplifies the processing of both rate-0 and rate-1 nodes. Once a rate-0 node is activated, it immediately returns the all zero vector. Once a rate-1 node is activated, a constituent codeword is directly calculated by making hard decisions on the received soft information vector as shown in Eq. (1). The ML-SSC decoding algorithm [19] further accelerates the SSC decoding algorithm by performing the exhaustive-search ML decoding on some resource constrained arbitrary rate nodes, which are called ML nodes in [19]. For an ML node with layer index \( t \), the constituent codeword passed to the parent node \( p_v \) is

\[
\beta_v = \arg\max_{x \in C} \sum_{i=0}^{2^{n-t}-1} (1 - 2x[i])\alpha_x[i],
\]

where \( C \) is the constituent code associated with node \( v \).

### C. LLR Based List Decoding Algorithms

For SCL decoding algorithms [6], [9], [13], when decoding an information bit \( u_v \), each decoding path splits into two paths with \( \hat{u}_v \) being 0 and 1, respectively. Thus 2\( L \) path metrics are computed and the \( L \) paths correspond to the \( L \) minimum path metrics are kept. The list decoding algorithms [6], [9] are performed either on probability or logarithmic likelihood (LL) domain. In [13], an LLR based list decoding algorithm was proposed to reduce the message memory requirement and the computational complexity of LL based list decoding algorithm. For decoding path \( l (l = 0, 1, \cdots, L - 1) \), the LLR based list decoding algorithm employs a novel approximated path metric

\[
PM_l^{(i)} = \sum_{k=0}^{i} D(L_n^{(k)}[l], \hat{u}_k[l]),
\]

where \( D(L_n^{(k)}[l], \hat{u}_k[l]) \) is set to 0 if \( h(L_n^{(k)}[l]) \) equals \( \hat{u}_k[l] \) or \( L_n^{(k)}[l] \) otherwise. Here \( L_n^{(k)}[l] \) is defined as \( \log \frac{W_n^{(k)}(\hat{u}_0^{k-1} \cdots \hat{u}_k-1 \hat{u}_k^{(l)} | 0)}{W_n^{(k)}(\hat{u}_0^{k-1} \cdots \hat{u}_k-1 \hat{u}_k^{(l)} | 1)} \) and \( y_0^{N-1} = (y_0, y_1, \cdots, y_{N-1}) \) is the received channel message vector.

### III. REDUCED LATENCY LIST DECODING ALGORITHM

#### A. SCL Decoding on A Tree

Similar to the SSC decoding algorithm, we also perform the SC based list decoding algorithms [6], [9] on a full binary tree \( G_n \) [17]. The SCL decoding is initiated by sending the received channel LLR vector to the root node of \( G_n \). As shown in Fig. 3, without losing generality, each internal node \( v \) in \( G_n \) is activated by receiving \( L \) LLR vectors, \( \alpha_v,0, \alpha_v,1, \cdots, \alpha_v,L-1 \), from its parent node \( v_p \) and is responsible for producing \( L \) constituent codewords, \( \beta_v,0, \beta_v,1, \cdots, \beta_v,L-1 \), where \( \alpha_v,l \) and \( \beta_v,l \) correspond to decoding path \( l \) for \( l = 0, 1, \cdots, L - 1 \). Suppose the layer index of node \( v \) is \( t \), \( \alpha_v,t \) and \( \beta_v,t \) have \( 2^{n-t} \) LLR messages and binary bits, respectively, for \( l = 0, 1, \cdots, L - 1 \).
Once a non-leaf node $v$ is activated, it calculates $L$ LLR vectors, $\alpha_{v,L,0}, \alpha_{v,L,1}, \cdots, \alpha_{v,L,L-1}$, and passes them to its left child node $v_L$, where

$$\alpha_{v,L,i}[l] = f(\alpha_{v,L}[2i], \alpha_{v,L}[2i+1])$$  \hfill (4)

for $0 \leq i < 2^{n-t}-1$ and $l = 0, 1, \cdots, L-1$. Here $f(a, b) = 2\tanh^{-1}(\tanh(a/2) \tanh(b/2))$ and can be approximated as:

$$f(a, b) \approx \text{sign}(a) \cdot \text{sign}(b) \min(|a|, |b|).$$  \hfill (5)

Node $v$ then waits until it receives $L$ codewords, $\beta_{v,L,0}, \beta_{v,L,1}, \cdots, \beta_{v,L,L-1}$, from $v_L$. In the following step, node $v$ calculates another $L$ LLR vectors, $\alpha_{v,R,0}, \alpha_{v,R,1}, \cdots, \alpha_{v,R,L-1}$, and passes them to its right child node $v_R$, where

$$\alpha_{v,R,i}[i] = g(\alpha_{v,L}[2i], \alpha_{v,L}[2i+1], \beta_{v,L}[i]) = \alpha_{v,L}[2i](1 - 2\beta_{v,L}[i]) + \alpha_{v,L}[2i+1]$$  \hfill (6)

for $0 \leq i < 2^{n-t}-1$ and $l = 0, 1, \cdots, L-1$.

At last, after node $v$ receives $L$ codewords, $\beta_{v,R,0}, \beta_{v,R,1}, \cdots, \beta_{v,R,L-1}$, from $v_R$, it calculates $\beta_{v,0}, \beta_{v,1}, \cdots, \beta_{v,L-1}$ and passes them to its parent node $v_p$, where

$$(\beta_{v,L}[2i], \beta_{v,L}[2i+1]) = (\beta_{v,L}[i] \oplus \beta_{v,R,L}[i], \beta_{v,R,L}[i]),$$  \hfill (7)

for $0 \leq i < 2^{n-t}-1$ and $l = 0, 1, \cdots, L-1$.

For $l = 0, 1, \cdots, L-1$, $PM_l$ is the path metric associated with decoding path $l$ and is initialized with 0. When a leaf node $v$ associated with an information bit is activated, decoding path $l$ splits into two paths with $\beta_{v,l}$ being 0 and 1, respectively. Note that the layer index of a leaf node is $n$, hence $\alpha_{v,L}$ and $\beta_{v,L}$ have only one LLR and binary bit, respectively, when node $v$ is a leaf node. For the SCL decoding, $2L$ expanded path metrics are computed, where

$$PM_l^j = PM_l + D(\alpha_{v,L,j}),$$  \hfill (8)

for $j = 0, 1$ and $l = 0, 1, \cdots, L-1, D(\alpha_{v,L,j}) = 0$ if $h(\alpha_{v,L})$ equals $j$. Otherwise, $D(\alpha_{v,L,j}) = |\alpha_{v,L}|$. Suppose the $L$ minimum expanded path metrics are $PM_{0_l}^{0_l}, PM_{0_l}^{1_l}, \cdots, PM_{0_l}^{L_l-1}$, which correspond to the $L$ most reliable paths, then $\beta_{v,l} = j_l$ for $l = 0, 1, \cdots, L-1$. Decoding path $a_l$ will be copied to decoding path $l$ before further partial sum and LLR vector computations. For each decoding path $l$, path metric is also updated with $PM_l = PM_l^j$. When a leaf node $v$ associated with a frozen bit is activated, $\beta_{v,l} = 0$ for $l = 0, 1, \cdots, L-1$. The updated path metric is $PM_l = PM_l + \Delta_{v,l}$ for $l = 0, 1, \cdots, L-1$. The SCL algorithm on a tree described above is equivalent to the SCL algorithms in [6], [9].

B. Proposed RLLD algorithm

In this paper, a reduced latency list decoding (RLLD) algorithm is proposed to reduce the decoding latency of SC list decoding for polar codes. For a node $v$, let $I_v$ denote the total number of leaf nodes that are associated with information bits. Let $X_{th}$ be a predefined threshold value and $X_0$ and $X_1$ be predefined parameters. Our RLLD algorithm performs the SC based list decoding on $G_n$ and follows the node activation schedule in Section III-A except when certain type of nodes are activated. These nodes calculate and return the codewords to their parent nodes while updating the decoding paths and their metrics, without activating their child nodes. Specifically:

- When a rate-0 node $v$ is activated, $\beta_{v,l}$ is a zero vector for $l = 0, 1, \cdots, L-1$.
- When a rate-1 node $v$ with $I_v > X_{th}$ is activated, $\beta_{v,l}$ is just the hard decision of $\alpha_{v,L}$ for $l = 0, 1, \cdots, L-1$. For polar codes constructed in [20], [21], we observe that the polarized channel capacities of the information bits corresponding to rate-1 nodes with $I_v > X_{th}$ are greater than those of the other information bits. Hence, for rate-1 nodes with $I_v > X_{th}$, our RLLD algorithm considers only the most reliable candidate codeword for each decoding path due to a more reliable channel.
- When a rate-1 node $v$ with $I_v \leq X_{th}$ is activated, the returned codewords are calculated by a candidate generation (CG) algorithm, which is proposed later.
- Let $l$ denote the layer index of node $v$. When an arbitrary rate node $v$ with $I_v < X_0$ and $2^{n-t} < X_1$ is activated, each decoding path splits into $2^l$ paths. From now on, such an arbitrary rate node is called fast processing (FP) node. A metric based search (MBS) algorithm, which is proposed later, is used to calculate the returned codewords.

Moreover, our RLLD algorithm works on a pruned tree. As a result, our RLLD algorithm visits fewer nodes than the SCL algorithm in [6], [9]. The full binary tree is pruned in the following ways:

- Starting from the complete tree representation of a polar code, label all FP nodes such that the parent node of each of them is not an FP node. Note that an FP node $v$ is an arbitrary rate node with $I_v < X_0$ and $2^{n-t} < X_1$. For each labeled FP node, remove all its child nodes.
- Based on the pruned tree from the previous step, label all rate-0 and rate-1 nodes such that the parent node of each of these rate-0 and rate-1 nodes is not a rate-0 and rate-1 node, respectively. In the next, remove all child nodes of each of labeled rate-0 and rate-1 node.

The leaf nodes of the pruned tree from the above two steps consist of rate-0, rate-1 and FP nodes. The non-leaf nodes of the pruned tree are arbitrary rate nodes.

When a rate-1 node with $I_v > X_{th}$ or a rate-0 node is activated, ideally $PM_l$ is updated with $PM_l + \Delta_{v,l}$ for $l = 0, 1, \cdots, L-1$. This completes the description of our RLLD algorithm.
0, 1, · · · , L − 1, where \( \Delta_{e,l} = \sum_{i=0}^{L-1} D(\alpha_{e,l}[i],\beta_{e,l}[i]) \). For each rate-1 node with \( I_v > X_{th} \), \( \Delta_{e,l} = 0 \) since \( \beta_{e,l} \) is the hard decision of \( \alpha_{e,l} \). However, for a rate-0 node, \( \Delta_{e,l} \) could have a non-zero value. For our RLLD algorithm, \( \Delta_{e,l} \) is also set to 0 for each rate-0 node, since the resulting performance degradation is negligible. By setting \( \Delta_{e,l} = 0 \), we no longer need to calculate \( \alpha_{e,l} \) sent to a rate-0 node.

1) Proposed CG Algorithm: When a rate-1 node with \( I_v \leq X_{th} \) is activated, instead of considering \( 2^{I_v} \) candidate codewords for each decoding path, since there are at most \( L \) codewords from the same decoding path that could be passed to the parent node, it is enough to find only the \( L \) most reliable codewords among \( 2^{I_v} \) candidates for each decoding path. When \( I_v \) is large (e.g. \( I_v \geq 32 \)), finding the \( L \) most reliable codewords is computationally intensive and lacks efficient hardware implementations. For our RLLD algorithm, we considers only the \( W(W < L) \) most reliable codewords among \( 2^{I_v} \) candidates for each decoding path. In this paper, \( W \) is set to 2, since it results in efficient hardware implementations at the cost of negligible performance loss.

When \( W = 2 \), the proposed CG algorithm, shown in Alg. 1 is used to calculate the codewords passed to the parent node. Besides, the CG algorithm also outputs \( L \) list indices, \( a_0, a_1, · · · , a_{L−1} \), which indicate that decoding path \( a_l \) needs to be copied to path \( l \). Suppose the layer index of such a rate-1 node \( v \) is \( t \). For each decoding path \( l \), there are \( 2^L = 2^{2^{I_v}−1} \) candidate codewords that could be passed to the parent node \( v_p \). However, our CG algorithm considers only the most reliable codeword \( C_{v,1,0} \) and the second most reliable codeword \( C_{v,1,1} \). In order to find these two codewords, each candidate codeword \( C_{v,l,j} \) is associated with a node metric

\[
NM_{l}^j = \sum_{k=0}^{L-1} m_k[\alpha_{e,l}[k]]
\]

for \( j = 0, 1, · · · , 2^L − 1 \), where \( m_k = 0 \) if \( C_{v,l,j}[k] \) equals \( h(\alpha_{e,l}[k]) \) and 1 otherwise. As a result, the smaller a node metric is, the more reliable the correspondent candidate codeword is. Based on Eq. (9), \( C_{v,1,0} = h(\alpha_{e,l}) \) is the hard decision of the received LLR vector \( \alpha_{e,l} \). \( C_{v,1,1} \) is obtained by flipping the \( k_{M,l} \)-th bit of \( C_{v,1,0} \), where \( k_{M,l} \) is the index of the LLR element with the smallest absolute value among \( \alpha_{e,l} \).

Each decoding path splits into two paths and has two associated candidate codewords. Alg. 1 calculates \( 2L \) expanded path metrics \( PM_{l}^j \) for \( l = 0, 1, · · · , L−1 \) and \( j = 0, 1 \) to select \( L \) codewords passed to the parent node. The \( \min_{i} \) function in Alg. 1 finds the \( L \) smallest values among \( 2L \) input expanded path metrics. Once \( \beta_{v,l} \) for \( l = 0, 1, · · · , L−1 \) are computed, decoding path \( a_l \) is copied to decoding path \( l \) before further operations.

2) Proposed MBS Algorithm: When an FN node is activated, each current decoding path expands to \( 2^L \) paths, each of which is associated with a candidate codeword. Similar to the CG algorithm, the proposed MBS algorithm calculates \( L \) codewords passed to the parent node and \( L \) path indices, \( a_0, a_1, · · · , a_{L−1} \). The calculation of returned codewords are shown as follows.

- For each candidate codeword \( C_{v,l,j} \) calculate its corresponding node metric \( NM_{l}^j \) for \( j = 0, 1, · · · , 2^L − 1 \) and \( l = 0, 1, · · · , L−1 \).
- Calculate \( 2^L \) expanded path metrics \( PM_{l}^j \) for \( l = 0, 1, · · · , L−1 \) and \( j = 0, 1, · · · , 2^L−1 \).
- Find \( L \) expanded path metrics among \( 2^L \) ones. The correspondent candidate codewords are passed to the parent node \( v_p \).

To calculate the node metric, we propose a new method with low computational complexity. In the literature, two methods can be used: the direct-mapping method (DMM) shown in Eq. (15) and the recursive channel combination (RCC) [16]. In terms of computational complexity, the former needs \( 2^L(2^{I_v}−1) \) additions, where \( N = 2^n \) and \( t \) is the layer index of an FN node \( v \). The RCC needs \( \sum_{i=1}^{n−t−1} 2^{2^{I_v}−i−1} + 2^L \) additions. Compared to the DMM, the RCC approach needs fewer additions. For our RLLD algorithm, we want to compute these \( 2^L \) node metrics in parallel. However, the parallel hardware implementations of the DMM and RCC algorithms require large area consumption. To discuss these in more detail in Section IV.C.

In this paper, a hardware efficient node metric computation method, which takes advantage of both the DMM and the RCC, is proposed. The proposed method, referred to as the DR-Hybrid (DRH) method, is shown in Alg. 2 where \( C_{v}[2i : 2i+1] = (C_{v}[2i], C_{v}[2i+1]) \), and \( r \) is represented by a binary tuple of length two, i.e. \( r = r_0 + 2r_1 \).

In our method, the RCC approach is used to calculate \( \theta_{l,i} \) first. Then, the DMM is carried out.

Algorithm 1: The proposed CG algorithm

| input | \( \alpha_{v,0}, \alpha_{v,1}, · · · , \alpha_{v,L−1} \) |
|-------|----------------------------------|
| output| \( \beta_{v,0}, \beta_{v,1}, · · · , \beta_{v,L−1} \), \( a_0, a_1, · · · , a_{L−1} \) |

1 for \( l = 0 \) to \( L−1 \) do
2 \( k_{M,l} = \arg \min_{k \in \{0,1,···,L−1\}} |\alpha_{e,l}[k]| \)
3 \( NM_{l}^0 = 0 \); \( C_{v,l,0} = h(\alpha_{e,l}) \)
4 \( NM_{l}^1 = |(\alpha_{e,l}[k_{M,l}]])| \); \( C_{v,l,1} = \text{Flip}(C_{v,l,0}, k_{M,l}) \)
5 \( PM_{l}^j = PM_l + NM_{l,j}^j \) for \( j = 0 \) to \( 1 \)
6 \( \left( PM_{l,0}^0, · · · , PM_{l,2^L−1}^0 \right) = \text{min}_{L}(PM_{l,0}^0, PM_{l,0}^1, · · · , PM_{l,2^L−1}) \)

for \( l = 0 \) to \( L−1 \) do
7 \( \beta_{v,l} = C_{v,a_l,b_l} \); \( PM_l = PM_{l,2^L−1}^0 \)

Algorithm 2: DR-Hybrid method

1 for \( l = 0 \) to \( L−1 \) do
2 \( / * \text{------------RCC-------------} * / \)
3 for \( i = 0 \) to \( 2^{n−t−1}−1 \) do
4 \( \text{for } r = 0 \) to \( 3 \) do
5 \( \theta_{l,i}([r_0, r_1]) = (1 - 2r_0)\alpha_{v,l}[2i] + (1 - 2r_1)\alpha_{v,l}[2i + 1] \)
6 \( / * \text{------------DMM-------------} * / \)
7 for \( j = 0 \) to \( 2^L−1 \) do
8 \( NM_{l}^j = \sum_{i=0}^{2^{L−1}−1} \theta_{l,i}(C_{v,l}[2i : 2i + 1]) \).


The DRH method needs $4 \times 2^{n-t-1} + 2^{I_e} (2^{n-t-1} - 1)$ additions. Take $X_0 = 8$ and $X_1 = 16$ as an example, the DMM, RCC and DRH methods need 3840, 864 and 1824 additions. Though our DRH method needs more additions than the RCC, it results in a more area efficient hardware implementation when all $2^{I_e}$ node metrics are computed in parallel, since the RCC method needs more complex multiplexors.

Once we have $2^{I_e}$ node metrics and corresponding candidate codewords, $2^{I_e}$ $L$ expanded path metrics $PM_l = PM_t + NM_j$ for $l = 0, 1, \ldots, L - 1$ and $j = 0, 1, \ldots, 2^{I_e} - 1$ can be computed. The next step is selecting $L$ returned codewords and their corresponding expanded path metrics.

Since directly finding the $L$ minimum values from $2^{I_e}L$ ones is computationally intensive and lacks efficient hardware implementations, a bitonic sequence based sorter [10] (BBS) implementations, a bitonic sequence based sorter [10] (BBS) ones is computationally intensive and lacks efficient hardware implementations. Take

$$X_0 = 2^{I_e} - L (\sum_{i=1}^{L-1} i) + 2^{I_e} - 2L$$

compare-and-switch (CS) units [10], where each of them has one comparator and two 2-to-1 multiplexors and $s = \log_2(2^{I_e}L)$. In order to simplify the hardware implementation, a two-stage sorting scheme was proposed in [16], where the first stage selects $q (q < L)$ smallest node metrics from $2^{I_e}$ ones for each decoding path. The second stage selects the $L$ smallest metrics from the $Lq$ expanded path metrics produced by the first stage. Compared with the direct sorting scheme [10], [15], the hardware implementation of the two-stage sorting scheme is more efficient at the cost of certain error performance degradation.

In this paper, our MBS algorithm employs the two-stage sorting scheme and improves the first stage in the following two aspects:

- Instead of using a fixed $q$, our MBS algorithm employs a dynamic $q_{i,v,L}(q_{i,v,L} \leq L)$, which is a power of 2 and depends on both $I_e$ and $L$.
- An approximated sorting (ASort) method, which leads to an efficient hardware implementation, is used to select $q_{i,v,L}$ metrics from $2^{I_e}$ ones, though these sorted metrics are not always the $q_{i,v,L}$ smallest ones.

Our ASort method is illustrated as follows:

- When $2^{I_e} \leq 2L$, the BBS with $2L$ inputs and $L$ outputs is used to select the $q_{i,v,L}$ minimum node metrics from $2^{I_e}$ ones.
- When $2^{I_e} > 2L$, all $2^{I_e}$ node metrics are divided into $q_{i,v,L}$ groups:

$$NM_1^{q_{i,v,L} - 1}, \ldots, NM_1^{(q_{i,v,L} - 1)m}, \ldots, NM_1^{(q_{i,v,L} - 1)m - 1}.$$

Here $m = \frac{2^{I_e}}{q_{i,v,L}}$. The two minimum node metrics of each group are first computed. The BBS computes the minimum $q_{i,v,L}$ node metrics among $2q_{i,v,L}$ ones.

After the first stage of sorting, the number of expanded path metrics $N_c$ be $2L, 4L, \ldots, L \times L$. The second stage of sorting is the same as that in [16]. A binary tree of $2L$-L BBSes are employed to sort the final $L$ minimum expanded path metrics. Take $N_c = 4L$ as an example, there are $4L$ extended path metrics: $PM_{l_0}^{h_0}, PM_{l_1}^{h_1}, \ldots, PM_{l_{4L-1}}^{h_{4L-1}}$, then $PM_{l_0}^{h_0}, PM_{l_1}^{h_1}, \ldots, PM_{l_{4L-1}}^{h_{4L-1}}$ and $PM_{l_0}^{h_0}, PM_{l_1}^{h_1}, \ldots, PM_{l_{4L-1}}^{h_{4L-1}}$ are applied to two $2L$-L BBSes, respectively. Thus, $2L$ metrics are selected. Then the $2L$-L BBS is employed again to generate the final $L$ minimum extended path metrics: $PM_{l_0}^{h_0}, PM_{l_1}^{h_1}, \ldots, PM_{l_{L-1}}^{h_{L-1}}$.

C. Parameters of Our RLLD Algorithm

For our RLLD algorithm, the returned codewords from rate-1 nodes with $I_e > X_{th}$ are obtained by making hard decisions on the received LLR vectors. The other rate-1 nodes are processed by our CG algorithm. Note that both the hard decision approach and our CG algorithm could cause potential error performance degradation since ideally we should consider $2^{I_v}$ candidate codewords for each decoding path. With more rate-1 nodes (decreasing $X_{th}$) being processed by the hard decision approach, the decoding latency could be reduced at the cost of more error performance degradation. Besides, in order to save computations, path metrics remain unchanged when a rate-0 node is activated, which may cause error performance degradation.

The choices of $X_0$ and $X_1$ are tradeoffs between implementation complexity and achieved decoding latency reduction. Ideally, we want $X_0$ and $X_1$ to be as large as possible so that more data bits could be decoded in parallel. Since the number of adders needed by Alg. [2] is proportional to $2^{X_0}X_1$, the values of $X_0$ and $X_1$ are limited by hardware implementations.

For the two-step sorting scheme of our MBS algorithm, we want $q_{i,v,L}$ to be as small as possible so that the sorting complexity could be minimized. However, reducing $q_{i,v,L}$ could degenerate the resulting error performance, since ideally we need to consider the $L$ most reliable candidate codewords for each decoding path. As a result, the selections of $q_{i,v,L}$ are tradeoffs between sorting complexity and error performance.

D. Comparison with Related Algorithms

If we perform the SC based list decoding algorithms [6], [9] on a tree, then all $2N - 1$ nodes of the tree will be activated. For our RLLD algorithm, denote $n_a$ as the number of activated nodes. Then we have $n_a < 2N - 1$, where $n_a$ is determined by the block length $N$, the code rate, the locations of frozen bits and the parameters $X_0$ and $X_1$, $X_0$ and $X_1$ are used to identify all FP nodes. The reduction of the number of activated nodes will transfer into reduced decoding latency and increased throughput. Take the $(8, 3)$ polar code in Fig. [2] as an example, suppose $X_0 = 1$ and $X_1 = 2$, then only 5 nodes (nodes 0, 1, 2, 5, and 6) need to be activated by our RLLD algorithm, whereas the algorithms in [6], [9] need to activate all 15 nodes.

The CA-SCL decoding algorithm was also performed on a binary tree in [17]. Compared with the low-latency list decoding algorithm [17], our RLLD algorithm employs the proposed MBS algorithm to process FP nodes, while FP nodes were processed by activating its child nodes in [17]. Our MBS algorithm results in decreased decoding latency at the cost of potential error performance loss. Besides, our RLLD algorithm takes a simpler approach when a rate-1 node is activated. When a rate-1 node is activated, a Chase-like
algorithm was used to calculate the \( L \) codewords passed to the parent node in [17]. Compared to the Chase-like algorithm, our CG algorithm has lower computational complexity and is more suitable for hardware implementation because:

1. The Chase-like algorithm in [17] was performed over log-likelihoods (LL) domain while our method is performed over LLR domain. Compared with our LLR based method, it takes more additions to calculate related metrics for the Chase-like algorithm.

2. For each decoding path, the Chase-like algorithm considers \( 1 + \binom{c}{1} + \binom{c}{2} \) candidate constituent codewords, where \( c = 2 \) in [17]. In contrast, our method considers only two constituent codewords, which leads to simpler hardware implementations.

3. In order to find the \( L \) best decoding paths and their constituent codewords, the Chase-like algorithm creates a candidate path list. The final \( L \) candidates are determined by inserting and removing elements from the list. The Chase-like algorithm is suitable for software implementations. However, the hardware implementations of the Chase-like algorithm has not been discussed in [17]. On the other hand, with a bitonic based sorter [10] (BBS), the \( L \) most reliable decoding paths can be decided in parallel for our CG algorithm.

\[ \text{E. Simulation Results} \]

For an \((8192, 4096)\) polar code, the bit error rate (BER) performances of the proposed RLLD algorithm as well as other algorithms are shown in Fig. 4. In Fig. 4, CS\( \_\_ \)denotes the CA-SCL decoding algorithm with \( L = x \), where CRC-32 is used. RX-\( y \) denotes the RLLD algorithm with \( L = x \) and \( X_{th} = y \). The values of \( q_{1, L} \)'s under different list sizes and \( I_v \)'s are shown in Table I. For all simulated algorithms, the additive white Gaussian noise (AWGN) channel and binary phase-shift keying (BPSK) modulation are used. For all simulated RLLD algorithms, \( X_0 = 8 \) and \( X_1 = 16 \).

| \( I_v \) | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|-----|---|---|---|---|---|---|---|---|
| 2   | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 4   | 2 | 4 | 4 | 4 | 4 | 4 | 4 | 2 |
| 16  | 2 | 4 | 8 | 8 | 8 | 8 | 8 | 2 |
| 32  | 2 | 4 | 8 | 8 | 8 | 8 | 4 | 2 |

Based on the simulation results shown in Fig. 4, we observe that R2-8 performs nearly the same as CS2 and R2-64. When the list size increases, compared with CS4, R4-8 shows obvious error performance degradation when BER is below 10\(^{-7} \). The degradation is reduced by increasing \( X_{th} \) to 128, as we observe that R4-128 performs nearly the same as CS4. When the list size further increases (e.g. \( L = 16 \) and 32), at low BER level, the error performance degradation exists even when \( X_{th} = 256 \). As shown in Fig. 4, R16-256 and R32-256 are worse than CS16 and CS32 when BER is below 10\(^{-5} \) and 10\(^{-6} \), respectively. Note that for the \((8192, 4096)\) polar code in this paper, \( I_v \) of a rate-1 node is at most 256. The simulation results of a \((1024, 512)\) polar code show similar phenomena.

\[ \text{IV. HIGH THROUGHPUT LIST POLAR DECODER ARCHITECTURE} \]

\[ \text{A. Top Decoder Architecture} \]

\[ \text{Fig. 4. BER performance for an (8192, 4096) polar code} \]

\[ \text{Fig. 5. Decoder top architecture} \]
In this paper, based on the proposed RLLD algorithm, a high throughput list decoder architecture, shown in Fig. 5, for polar codes is proposed. In Fig. 5, the channel message memory (CMEM) stores the received channel LLRs, and the internal LLR message memory (IMEM) stores the LLRs generated during the SC computation process. With the concatenation and split method in our prior work [10], the IMEM is implemented with area efficient memories, such as register file (RF) or SRAM. The proposed architecture has L groups of processing unit arrays (PUs), each of which contains T processing units [5] (PUs) and is capable of performing either the f or the g computation in Eqs. (5) and (6), respectively. The hybrid partial sum unit (Hyb-PSU) in Fig. 5 consists of T computation units, Cu0, Cu1, ···, CuT-1, which are responsible for updating the partial sums of L decoding paths, respectively. The path pruning unit (PPU) in Fig. 5 finds the list indices and corresponding constituent codewords for L survival decoding paths. The control of our decoder architecture can be designed based on the instruction RAM based methodology in [22].

Both our high throughput list decoder architecture in Fig. 5 and that in [10] employ a parallel partial processing method. Besides, both architectures contain a channel message memory and internal message memory. However, compared to the architecture in [10], the major improvements of our list decoder architecture are:

(a) Instead of LL messages, our high throughput list decoder architecture employs LLR messages, which result in more area efficient internal and channel message memories.

(b) The PPU in Fig. 5 implements our CG and MBS algorithms, while the PPU in [10] is just a sorter which selects L values among 2L ones. Due to the proposed PPU, our decoder architecture achieves much higher throughput than that in [10].

(c) Our list decoder architecture employs a novel Hyb-PSU, which is more area and energy efficient than that in [10]. Our Hyb-PSU is based on the proposed index based partial sum computation algorithm. When a decoding path need to be copied to another one, instead of copying partial sums directly our Hyb-PSU copies only decoding path indices. In contrast, the PSU in [10] copies path sums directly, which incurs additional energy consumption. Our Hyb-PSU stores most of the partial sums in area efficient memories, while the PSU in [10] stores all the partial sums in area demanding registers. Hence, our Hyb-PSU is scalable for larger block lengths.

B. Memory Efficient Quantization Scheme

For an SC or SCL decoder, the message memory occupies a large part of the overall decoder area [3], [10]. An SCL decoder needs a channel message memory and an internal message memory. For an LLR based SCL decoder, the channel memory stores N channel LLR messages. The internal message memory stores Ln LLR matrices: \( P_{l,t} \) for \( l = 0,1, \cdots, L-1 \) and \( t = 1,2, \cdots, n \), where \( P_{l,t} \) has \( 2^{n-t} \) LLR messages.

For a fixed point implementation of our RLLD algorithm, it is straightforward to quantize all LLRs in the internal memory with \( Q \) bits. In this paper, a memory efficient quantization (MEQ) scheme is proposed to reduce the size of the internal memory. \( f(a,b) \) in Eq. (9) has the same magnitude range as those of \( a \) and \( b \), while the magnitude range of \( g(a,b,s) \) in Eq. (9) is at most twice of those of \( a \) and \( b \) (\( s = \text{either 0 or 1} \)). Since \( P_{0,t} \), \( P_{1,t} \), ···, \( P_{L-1,t} \) are computed based on \( P_{0,t-1} \), \( P_{1,t-1} \), ···, \( P_{L-1,t-1} \), for a decoding path \( l \), the LLRs in \( P_{l,t} \) may need a greater magnitude range than that of the LLRs in \( P_{l,t_2} \), where \( t_1 > t_2 \). Suppose each channel LLR is quantized with \( Q_c \) bits, the proposed MEQ scheme is as follows:

(1) Suppose all LLRs within the internal memory are quantized with \( Q_m \) bits, determine the minimal \( Q_m \) such that the error performance degradation of the fixed point performance is negligible.

(2) Let \( t_1, t_2, \cdots, t_r \) be \( r \) integers, where \( t_1 \leq t_2 \leq \cdots \leq t_r \leq n \) and \( r = Q_m - Q_c \). Denote \( P_t = (P_{0,t}, P_{1,t}, \cdots, P_{L-1,t}) \). Suppose LLRs associated with \( P_{1}, P_{2}, \cdots, P_{t_1} \) are quantized with \( Q_c \) bits and the remaining LLRs are quantized with \( Q_m \) bits. Decide the maximal \( t_1 \) such that the resulting fixed point error performance degradation is negligible. Once \( t_1 \) is decided, suppose the LLRs within \( P_{t_1+1}, P_{t_1+2}, \cdots, P_{t_r} \) are all quantized with \( Q_c+1 \) bits, find the maximal \( t_2 \) such that the corresponding error performance degradation is negligible. In this way, \( t_3, \cdots, t_r \) are decided in a serial manner so that \( P_{t_i+1}, P_{t_i+2}, \cdots, P_{t_{i+1}} \) are quantized with \( Q_c+i \) bits for \( 1 \leq i \leq r-1 \), and \( P_{j} \) are quantized to \( Q_m \) bits for \( j > t_r \).

With the proposed MEQ scheme, the number of bits saved for the internal memory is

\[
N_B = \sum_{j=1}^{r+1} \sum_{t=t_j-1+1}^{t_j} L 2^{n-t}(Q_c + j - 1),
\]

where \( t_0 = 0 \) and \( t_{r+1} = n \) are introduced for convenience.

In order to show the effectiveness of our MEQ scheme, the error performances of our RLLD algorithm with the proposed MEQ scheme are shown in Fig. 6 where the RLLD algorithm with our MEQ scheme is compared with the floating-point CA-SCL decoding algorithm, floating-point RLLD algorithm, and RLLD algorithm with a uniform quantization scheme for three different polar codes, (1024, 512), (8192, 4096) and (32768, 29504) with \( X_{th} = 32, 128, 1024 \), respectively. For all fixed-point decoders, each channel LLR is quantized with \( Q_c = 5 \) bits. For the RLLD algorithm with uniform quantization, each LLR in the internal memory is quantized with \( Q_m = 6 \) bits for the length 2^10 and 2^13 polar codes. For the polar code with a length of 2^15, the uniform quantization takes 7 bits. For our MEQ scheme, \( Q_m = 7 \). Since \( Q_m - Q_c = 2 \), we need to determine two integers, \( r_1 \) and \( r_2 \), for our MEQ scheme. When \( N = 2^{10}, 2^{13} \) and \( 2^{15} \), \( (r_1, r_2) = (1, 2), (3, 4) \) and (4, 5), respectively. As shown in Fig. 6, the performance degradation caused by our MEQ scheme is small. Compared with the uniform quantization, the proposed MEQ scheme reduces the number of stored bits by 4.5%, 13.5% and 27.2% for \( N = 2^{10}, 2^{13} \) and \( 2^{15} \), respectively. For all the simulation results shown in Fig. 6 list size \( L = 4 \).
C. Proposed path pruning unit

When a rate-1 node with \( \alpha_v \leq X_{th} \) or an FP node is activated, each decoding path splits into multiple ones and only the \( L \) most reliable paths are kept. The PPU in Fig. 5 implements our CG and MBS algorithms, and is responsible for calculating \( L \) returned codewords, \( \beta_{e,0}, \beta_{e,1}, \ldots, \beta_{e,L-1} \), and \( L \) path indices, \( a_0, a_1, \ldots, a_{L-1} \). For \( l = 0, 1, \ldots, L-1 \), decoding path \( l \) copies from decoding path \( a_l \) before further decoding steps.

Take \( L = 4 \) as an example, the proposed PPU is shown in Fig. 7 which can be easily adapted to other \( L \) values. Our PPU in Fig. 7 has two types of node metric generation (NG) units, NG-I and NG-II, which compute the node metrics for a rate-1 node and an FP node, respectively. NG-I and NG-II correspond to decoding path \( l \). For decoding path \( l \), the expanded path metrics \( P\alpha_M \)'s are obtained by adding the node metrics to the path metric PM\( _l \), which is stored in the path metric registers (PMR) and initialized with 0.

When a rate-1 node is activated, NG-I outputs two node metrics for \( l = 0, 1, \ldots, L-1 \). After \( 2L \) expanded path metrics are computed, a stage of metric sorter (MS\( _{2L-L} \)) selects the \( L \) minimum metrics and their corresponding codewords from \( 2L \) ones. The metrics sorter MS\( _{2L-L} \) implements the \( \text{min}_L \) function in Alg. 1 and can be constructed with a BBS. When an FP node is activated, \( L \) NG-II modules implement the first part of our two-stage sorting scheme. For each decoding path, \( q_{L,v,l} \), node metrics and their correspondent codewords are computed. The tree of metric sorters sort the \( L \) minimum metrics among \( q_{L,v,l} \), \( L \) ones. This is achieved by \( \log_2 q_{L,v,l} \) stages of metric sorters, where \( q_{L,v,l} \) is a power of 2. The output expanded path metrics of the last stage of metric sorter are saved in the PMR. The corresponding codewords of the selected \( L \) expanded path metrics are also chosen. The related circuitry is omitted for brevity.

The micro architecture of NG-I is shown in Fig. 8. The most complex part of NG-I is finding the minimum LLR magnitude and its corresponding index among the LLR vector \( |\alpha_{e,l}| \triangleq (|\alpha_{e,l}[0]|, |\alpha_{e,l}[1]|, \ldots, |\alpha_{e,l}[L-1]|) \). Since the node metric of the most reliable candidate codeword is always 0, we need to compute \( \text{NM}_l^1 = |\alpha_{e,l}[k_{M,l}]| \) in Fig. 8 which is the node metric of the second most reliable candidate codeword, with a corresponding index \( k_{M,l} \). For our list decoder architecture, for each decoding path, at most \( T \) LLRs are computed in one clock cycle, since we have only \( T \) PUs per decoding path. The Min-1 unit in Fig. 8 is capable of finding the minimum value, mLLR, and its corresponding index, mIdx, from at most \( T \) parallel inputs. When \( \alpha_v \leq T \), \( \text{NM}_l^1 = \text{mLLR} \) and \( k_{M,l} = \text{mIdx} \). \( C_{v,l,0} = h(\alpha_{e,l}) \) in Fig. 8 is the hard decision of \( \alpha_{e,l} \), which is the most reliable candidate codeword. The second most reliable candidate codeword is obtained by flipping the \( k_{M,l} \)-th bit of \( C_{v,l,0} \).

When \( \alpha_v > T \), suppose \( T \) is a power of 2, then \( \alpha_v \) can be divided by \( T \). During each clock cycle, only \( T \) LLRs are fed to NG-I\( _v \), and the minimum value and its corresponding index are computed in a partial parallel way. The minimum value and associated index of the first \( T \) inputs are stored in mLLR and mIdx, respectively. The minimum value of the second group of \( T \) inputs is compared with the current value stored in mLLR, and is stored in mLLR if it is smaller than the current value of mLLR. This repeats until the whole LLR vector \( \alpha_{e,l} \) is processed. At last, the minimum value of \( |\alpha_{e,l}| \) and its index are stored in mLLR and mIdx, respectively. The hard decoding of \( \alpha_{e,l} \) is stored in the hard decoded constituent codeword memory (HCM0), and is copied to HCM1 when the second most reliable constituent codeword is computed.

The micro-architecture of NG-II\(_v \) under \( X_0 = 8 \) and \( X_1 = 16 \) is shown in Fig. 9 where the block MUX4T256 includes 256 4-to-1 multiplexers. Our NG-II\(_v \) consists of two parts: the first part calculates \( 2^L \) node metrics, \( \text{NM}_l^0, \text{NM}_l^1, \ldots, \text{NM}_l^{2^L-1} \), based on Alg. 2 and the second part implements the first stage sorting of our MBS algorithm. For \( L = 4 \), when \( 2^L > 2L \), the \( 2^L \) metrics are first divided into four groups. The Min-2 \(_L \) block is modified slightly to find the two minimum node metrics and their associated indices.
for each metric group. The MS₈₋₄ block calculates the final output metrics. When 2ᴺ = 2L = 8, the MS₈₋₄ blocks work directly on the 2L = 8 expanded path metrics. When 2ᴺ ≤ L, the expanded path metrics are output directly. As shown in Figs. 7 to 9 our PPU has long critical path delay, since there are many levels of logic from the inputs to outputs. Pipelines should be used to improve overall decoder frequency.

Based on the DMM method in Eq. (9), the node metric computation part needs 2ᴺ(2ᴺ−1)L adders and 2ᴺ(2ᴺ−1)2 to-1 multiplexers, where N = 2ᴺ and t is the layer index of an FP node v. Based on the RCC method, it takes (∑ₜ₌₁ᴺ−₁ 2ᴺ−t−1L + 2ᴺ) L adders, 2ᴺ+1L 2ᴺ−t−1L to-1 multiplexers and 4 × 2ᴺ−t−1L 2-to-1 multiplexers. In contrast, based on our DRH method, it takes 4 × 2ᴺ−t−1 + 2ᴺ(2ᴺ−t−1−1) adders, 2ᴺ+1L 2ᴺ−t−1-1 to-1 and 4×2ᴺ−t−1-1 2-to-1 multiplexers. Table II compares hardware resources needed by the DMM, RCC and DR-Hybrid methods where X₀ = 8, X₁ = 16, and αᵣ,v[j] (0 ≤ j < 2ᴺ−t) is a 6-bit LLR. As shown in Table II the DRH method requires the smallest total area. Besides, the implementations based on DMM, RCC and DRH have roughly the same critical path delay.

**TABLE II**

| HARDWARE RESOURCES NEEDED BY DIFFERENT METHODS PER LIST |
|-----------------|---------|---------|---------|
|                 | DMM     | RCC     | DRH     |
| # of adders     | 3840    | 864     | 1824    |
| # of MUX₂⁻₁     | 4096    | 32      | 32      |
| # of MUX₂⁵⁶⁻₁   | 0       | 512     | 0       |
| total area (# of NAND3) | 313,967 | 1,673,810 | 229,449 |

**D. Proposed hybrid partial sum unit**

For the list decoder architectures in [9], [10], all partial sums are stored in registers and the partial sums of decoding path l’ are copied to decoding path l when decoding path l’ needs to be copied to decoding path l. The PSU in [9] and [10] needs L(N−1) and L(N−1) single bit registers to store all partial sums, respectively. Thus, for large N, the register based PSU architectures in [9], [10] are inefficient for two reasons. First, the area of the PSU is linearly proportional to N. For large N (e.g. N > 2¹⁵), the area of PSU is large since registers are usually area demanding. Second, the power dissipation due to the copying of partial sums between different decoding paths is high when N is large.

1) Proposed Index Based Partial Sum Computation Algorithm: In order to avoid copying partial sums directly, an index based partial sum computation (IPC) algorithm is proposed in Algorithm 3 where pᵣ[z] (l = 0, 1, ..., L − 1 and z = 0, 1, ..., n) is a list index reference. Cᵣ,z for l = 0, 1, ..., L − 1 and z = 0, 1, ..., n are partial sum matrices [9], [10]. Cᵣ,z has 2ⁿ-z elements, each of which stores two binary bits.

For our RLLD algorithm, once a rate-0, rate-1 or an FP node sends L codewords to its parent node, the partial sum computation is performed after decoding path pruning. Let t denote the layer index of such a node v. Let (Bₙ₋₁, Bₙ₋₂, ..., B₀) denote the binary representation of the index of the last leaf node belonging to node v, where Bₙ₋₁ is the most significant bit. Let tₑ = n − j, where j is the smallest integer such that Bⱼ = 0. If Bⱼ = 1 for j = 0, 1, ..., n − 1, tₑ = 0. Once βᵣ,0,βᵣ,1, ..., βᵣ,L−1 are calculated, decoding path l’ may need to be copied to path l before the following partial sum computation. Under this circumstance, the index references are first copied, where pᵣ[z] is copied to pᵣ[z] for z = tₑ, tₑ−1, ..., 0. The lazy copy algorithm was proposed in [6] to avoid copying partial sums directly. However, the lazy copy algorithm is not suitable for hardware implementation due to complex index computation. The PSU in [10] copies all partial sums belonging one decoding path to the corresponding locations of another decoding path.

**Algorithm 3:** Index Based Partial Sum Computation (IPC) Algorithm

```
input : tₑ, t₁(v,β₁,0,β₁,1, ..., β₁,L−1)
output: Cᵣ,t₁[j][0] for l = 0, 1, ..., L − 1 and
       j = 0, 1, ..., 2ᴺ−tₑ

1 for l = 0 to L − 1 do
2     for j = 0 to 2ᴺ−tₑ − 1 do
3         if v is the left child node of its parent node then
4             Cᵣ,t₁[j][0] = βᵣ,e[j]; pᵣ[t] = l
5         else
6             Cᵣ,t₁[j][1] = βᵣ,t[j]
7       end if
8 if v is the left child node of its parent node then exit
9 for l = 0 to L − 1 do
10    for j = 0 to 2ᴺ−z − 1 do
11      v₀ = Cᵣ,z+l₁[0][0]; v₁ = Cᵣ,z+l₁[1][1]
12      if z == tₑ then
13          Cᵣ,z[2j][0] = v₀ + v₁; Cᵣ,z[2j + 1][0] = v₁
14          pᵣ[z + 1] = pᵣ[z] = l
15      else
16          Cᵣ,z[2j][1] = v₀ + v₁; Cᵣ,z[2j + 1][1] = v₁
17          pᵣ[z + 1] = l
```

2) Micro Architecture of the Proposed Hybrid Partial Sum Unit: Based on our IPC algorithm, a Hyb-PSU is proposed with two improvements. First, some partial sums are stored in
memory, while others are stored in registers. Second, instead of partial sums, only list index matrices are copied. These two improvements reduce the area and power overhead of partial sum computation unit when $N$ is large. The Hyb-PSU consists of $L$ computation units, $CU_0, CU_1, \ldots, CU_{L-1}$, where the micro architecture of $CU_l$ is shown in Fig. 10(a) and is described as follows.

(a) Let $m$ be a predefined integer parameter. For block length $N = 2^n$, $CU_l$ consists of $n$ stages, where the first $n - m + 1$ stages are a binary tree of the type-I and type-II unit processing elements (PEs) shown in Figs. 10(b) and 10(c), respectively. Stage $z (z \geq m)$ has $2^{n-z}$ PEs. Each of the remaining $m - 1$ stages has the same circuitry.

(b) Two types of PEs are used in the PE tree in Fig. 10(a). Suppose the maximal length of a constituent word that is returned from a rate-0, rate-1 or FP node is $2^n$, then stage $z (z \geq n - \mu)$ employs only the type-I PEs. The remaining stages in the PE tree employ the type-II PEs.

(c) Compared with the type-I PE, the type-I PE has an extra data load unit (DLU). For $PE_{z,j}$ within stage $z (j = 0, 1, \ldots, 2^n - 1)$, the binary outputs, $o_{l,z,j}$ and $o_{l,z,j+1}$, are connected to $b_{l,z-1,j}$ and $b_{l,z-1,j+1}$, respectively. The wired connections are not shown in Fig. 10(a) for simplicity.

(d) $BM_{l,z} (z \leq m - 1)$ is a bit memory with $c_{w,z} = 2^n$ words, where each word contains $T$ bits. $T$ is the number of processing elements belonging to a decoding path in a partial parallel list decoder. For our memory compiler, if $c_{w,z}$ is greater than a threshold value, then $BM_{l,z}$ is implemented with an RF. If $c_{w,z}$ is even greater than another threshold value, then $BM_{l,z}$ is implemented with an SRAM.

(e) The connector module (CN) has two $T$-bit inputs and two $T$-bit outputs. The connections between the outputs and inputs are

$$
\begin{align*}
O_0[j] &= I_0[j] + I_1[j] & 0 \leq j < T/2 \\
O_0[j + 1] &= I_1[j] & 0 \leq j < T/2 \\
O_1[j + T] &= I_0[j] + I_1[j] & T/2 \leq j < T \\
O_1[j + 1 + T] &= I_1[j] & T/2 \leq j < T
\end{align*}
$$

(11)

(f) For our Hyb-PSU, $L$ computation units are needed. For each PE within $CU_l$, $m_{l,z,j}$ in Figs. 10(b) and 10(c) is the output of an $L$-to-1 multiplexer whose inputs are $d_{0,z,j}, d_{1,z,j}, \ldots, d_{L-1,z,j}$, where $L - 1$ of them are from other computation units. For each CN, $M_{l,z}$ is the output of an $L$-to-1 multiplexer whose inputs are $D_{0,z}, D_{1,z}, \ldots, D_{L-1,z}$.

3) Computation Schedule of Our Hybrid Partial Sum Unit: Once the returned codewords $\beta_{v,0}, \beta_{v,1}, \ldots, \beta_{v,L-1}$ are computed, the path pruning unit also outputs $L$ indices $a_0, a_1, \ldots, a_{L-1}$, where $a_l$ needs to be copied to decoding path $l$. For $l = 0, 1, \ldots, L - 1, \beta_{v,l}$ is first loaded into stage $t$ by the DLU in Fig. 10(b), and the output partial sums in Alg. 3 come out from stage $t_c$. For stage $t_c$ if $\beta_{v,l}$ is sent from a rate-0 node, then the control signal $LZ_2$ is 0, since $\beta_{v,l} = 1$. Otherwise, LD$_2 = 0$ and $LZ_2 = 1$. For the other stages, LD$_2 = 1$ and $LZ_2 = 1 (z \neq 1)$.

For all partial sums within the partial sum matrix $C_{l,z}$, we divide them into two sets: $C_{l,z}'$ and $C_{l,z}''$, where $C_{l,z}'$ consists of $C_{l,z}[j][0]$ for $j = 0, 1, \ldots, 2^n - 1$ and $C_{l,z}''$ consists of the other partial sums within $C_{l,z}$. For each $C_{l,z}$, our Hyb-PSU stores only $C_{l,z}'$, in the registers or bit memory of stage $z$. As shown in Alg. 3 for $z = t - 1$ to $t_c + 1$, $C_{l,z}'$ is computed in serial. At last, $C_{l,t_c}$ is computed. For our Hyb-PSU, after loading the returned $L$ codewords into stage $t$, for $z = t - 1$ to $t_c + 1$, $C_{l,z}'$ is computed on-the-fly and passed to the next stage as shown in Fig. 10.

When $t_c \geq m$, $C_{l,t_c}'$ is computed in one clock cycle and is output from stage $t_c$, where $C_{l,t_c'}[j][0]$ is set to $s_{l,t_c,j}$ produced by the type-I and type-II PEs for $j = 0, 1, \ldots, 2^n - 1$. When $t_c < m$, $C_{l,t_c'}$ is computed in $2^n - t_c$ cycles, and $T$ updated partial sums are computed in each clock cycle. Since decoding path $a_l$ needs to be copied to path $l$, for $z = t, t - 1, \ldots, t_c + 1$, the computation of $C_{l,z}''$ is based on $C_{l,z}'$ and $C_{l,z+1}$. Hence, the multiplexers within stage $z$ are configured so that $m_{t,z,j} = d_{a_l,z,j}$ for $z \geq m$. When $z < m$, $M_{l,z} = Q_{a_l}$.

4) Comparisons with Related Works: Compared to the partial sum computation architectures in [9, 10], the proposed Hyb-PSU architecture has advantages in the following two aspects.

(1) The proposed Hyb-PSU is a scalable architecture. The PSU architectures in [9, 10] require $L(N - 1)$ and $L(N/2 - 1)$ single bit registers, where $N = 2^n$ is the block length. Hence, they will suffer from excessive area overhead when the block
length $N$ is large. In contrast, the proposed Hyb-PSU stores $L(N-1)$ bits and most of these bits are stored in RFs or SRAMs, which are more area efficient than registers.

(2) The architectures in [9], [10] copy partial sums of a decoding path to another decoding path when needed, while our Hyb-PSU copies only index references. We define the copying of a single bit from one register to another as a single copy operation. When decoding path $l'$ needs to be copied to path $l$, the PSU in [10] requires $N_1 = 2^{n-1} - 1$ copy operations, while our Hyb-PSU needs only $N_2 = (n+1) \log_2 L$ copy operations. Since the value of $L$ for practical hardware implementation is small, our lazy copy needs much fewer copy operations than direct copy.

In this paper, when $L = 4$ and $T = 128$, for $N = 2^{13}$ and $2^{15}$, the proposed hybrid partial sum unit architecture is implemented with $m = 3$ and $m = 5$, respectively, under a TSMC 90nm CMOS technology. Our partial sum computation unit consumes an area of 0.779mm$^2$ and 1.31mm$^2$ for $N = 2^{13}$ and $N = 2^{15}$, respectively.

To the best of our knowledge, those decoder architectures in [9], [10], [13], [24] are the only for SC based list decoding algorithms of polar codes. However, in [9], [13], [24], the partial sum computation unit architecture was not discussed in detail and the implementation results on the PSU alone are not shown. Hence, we compare our proposed Hyb-PSU with that in [10]. When $L = 4$, the partial sum unit architecture in [10] for $N = 2^{13}$ and $2^{15}$ consumes an area of 1.011mm$^2$ and 3.63mm$^2$, respectively, under the same CMOS technology. All PSUs are synthesized under a frequency of 500MHz. Our Hyb-PSU achieves an area saving of 23% and 63% for block length $2^{13}$ and $2^{15}$, respectively.

### V. Implementation Results and Comparisons

To compare with prior works, we implement our high throughput list decoder architecture for three polar codes with lengths of $2^{10}$, $2^{13}$ and $2^{15}$, respectively, and rates 0.5, 0.5 and 0.9, respectively. The last polar code is intended for storage applications. For each code, three different list sizes are considered: $L = 2, 4, 8$. All our decoders are synthesized under the TSMC 90nm CMOS technology using the Cadence RTL compiler. The area efficiency (AE) of a partly parallel decoder architecture depends on the number of PSUs. In order to make a fair comparison with prior works in [10], [12], [16], the number of PSUs for each decoding path of our implemented decoders is selected to be 64 when $N = 2^{10}$. When $N = 2^{13}$ and $2^{15}$, the number of PSUs per decoding path is 128 for our decoders. The list decoders in [27] are based on a line architecture, which requires $N/2$ PSUs.

A total of 3, 4 and 6 pipeline stages, respectively, are inserted in the PPU for decoders with $L = 2, 4$ and 8, respectively. The number of pipeline stages needed for our PPU is determined by the longest data path. For each $v_i \in S'_V$, if node $v_i$ is a rate-1 node with $I_v \leq X_{th}$, $N_p^{(i)}$ depends on the number of PSUs in a decoding path: when $I_v < T$, $N_p^{(i)} = 2$ for all our implemented decoders; otherwise, $N_p^{(i)} = 4$ for all our decoders, since the minimum value of a received LLR vector is calculated in a partial parallel way, which incurs extra clock cycles. When node $v_i$ is an FP node, $N_p^{(i)}$ relates to $q_{L_e,L}$. Depending on the detailed value of $q_{L_e,L}$, we may use different data paths when computing the $L$ minimum expanded path metrics. The locations of all pipelines are arranged so that fewer clock cycles are needed when the $q_{L_e,L}$ is smaller. In Table VI we list the detailed value of $N_p^{(i)}$ with respect to $I_v$ and $L$.

The selection of $X_{th}$ is a trade-off between AE and error performance. When increasing $X_{th}$, more rate-1 nodes will be processed by our CG algorithm. Hence, $N_p$ increases and the resulting NIT decreases. Meanwhile, the corresponding error performance is better especially in high SNR region. Our high throughput list decoder architecture supports all $X_{th}$ values. For all our implemented decoders, $X_{th}$ is large enough so that all rate-1 nodes are processed by our CG algorithm. In this setup, for each implemented decoder, $N_D$ is maximized with respect to $X_{th}$, and hence the throughput of
TABLE III
IMPLEMENTATION RESULTS FOR N = 2¹⁰, R = 0.5

| L  | proposed | [12] | [10] | [15] | [16] |
|----|----------|------|------|------|------|
|    | Frequency (MHz) | 423 | 403 | 289 | 384 |
|    | Cell Area (mm²) | 1.98 | 3.83 | 7.22 | 0.88 |
|    | # of Decoding Cycles | 337 | 371 | 404 | 2592 |
|    | NIT (Mbps) | 666 | 570 | 374 | 168 |
|    | Latency (us) | 0.79 | 0.92 | 1.39 | 3.06 |
|    | AE (Mbps/mm²) | 336 | 148 | 51 | 191 |

†The decoder architecture in [10] has been re-synthesized under the TSMC 90nm CMOS technology. * These are the original implementation results based on a 65nm CMOS technology. †These are the scaled results under the TSMC 90nm CMOS technology.

TABLE IV
IMPLEMENTATION RESULTS FOR N = 2¹³, R = 0.5

| L  | proposed | [12] | [10] | [15] | [16] |
|----|----------|------|------|------|------|
|    | Frequency (MHz) | 416 | 398 | 289 | 847 |
|    | Cell Area (mm²) | 3.42 | 6.46 | 12.26 | 6.48 |
|    | # of Decoding Cycles | 2146 | 2367 | 2576 | 20736 |
|    | NIT (Mbps) | 839 | 723 | 479 | 167 |
|    | Latency (us) | 5.16 | 5.94 | 8.91 | 24.48 |
|    | AE (Mbps/mm²) | 245 | 111 | 39 | 26 |

†These results are estimated conservatively. †The decoder architectures in [10], [16] have been re-synthesized under the TSMC 90nm CMOS technology. The number of PU per decoding path is 128.

TABLE V
IMPLEMENTATION RESULTS FOR N = 2¹⁵, R = 0.9004

| L  | proposed | [12] | [10] | [15] | [16] |
|----|----------|------|------|------|------|
|    | Frequency (MHz) | 367 | 359 | 286 | 847 |
|    | Cell Area (mm²) | 6.22 | 11.89 | 23.13 | 25.68 |
|    | # of Decoding Cycles | 6070 | 6492 | 6895 | 96576 |
|    | NIT (Mbps) | 1949 | 1772 | 1323 | 258 |
|    | Latency (us) | 16.53 | 18.08 | 24.11 | 114.02 |
|    | AE (Mbps/mm²) | 313 | 149 | 57 | 11 |

†These results are estimated conservatively. †The decoder architectures in [10], [16] have been re-synthesized under the TSMC 90nm CMOS technology. The number of PU per decoding path is 128.

Our decoder architecture in Tables III, IV and V is the minimum achieved by our decoders. For each code, the corresponding error performance is better than that of the RLLD with the MEQ in Fig. 6.

TABLE VI
N_P^(s) WITH RESPECT TO I_v AND L

| I_v | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|-----|---|---|---|---|---|---|---|---|
| L = 2 | 2 | 2 | 2 | 3 | 3 | 3 | 3 | 3 |
| L = 4 | 2 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| L = 8 | 2 | 3 | 4 | 5 | 5 | 6 | 5 | 3 |

The implementation results are shown in Table III, IV and V. The implementation results show that our decoders outperform existing SCL decoders [10], [12], [15] in both decoding latency and area efficiency. Compared with the decoders of [12], the area efficiency and decoding latency of our decoders are 1.59 to 32.5 times and 3.4 to 6.8 times better, respectively. The area efficiency and decoding latency of our decoders are 3.9 to 21.5 times and 5.5 to 13 times better, respectively, than the decoders of [10]. Compared with decoders of [16], our decoders improve the area efficiency and decoding latency by 1.12 to 12 times and 2.8 to 9 times, respectively. When N = 2¹⁰, the area efficiency and decoding latency of our decoders are 3.8 to 4.2 times and 3.58 to 3.84 times better, respectively, than the decoders of [15]. Compared with the decoders of [15], our decoders would show more significant improvements in area efficiency and decoding latency when N is larger.

Based on the implementation results shown in Tables III, IV and V, it is observed that when the block length is fixed, as the list size L increases, the area efficiency and decoding latency will decrease and increase, respectively, because:

- It takes more memory to store internal LLRs when L increases.
- The number of pipeline stages within our PPU will increase when L increases, which in turn increases the overall decoding clock cycles.

The latency reduction and area efficiency improvement of our decoders are due to the reduced number of nodes activated in the decoding. However, the area and frequency overhead of the proposed PPU somewhat dilute the effects due to decoding clock cycles reduction. For example, our decoder reduces the number of decoding cycles to approximately ½ of that of the decoders in [12] for L = 2, 4 and 8. However, the
reduction in decoding cycles does not fully transfer into the improvement in decoding latency and area efficiency. Based on our implementation results, take \( L = 2 \) as an example, the PPU occupies 61.99%, 40.16% and 25.40% of the area of the whole decoder, for \( N = 2^{10}, 2^{13} \) and \( 2^{15} \), respectively. Compared with the decoders with \( N = 2^{10} \) and \( 2^{13} \), the effects on the area efficiency caused by the area overhead of PPU are smaller for decoders with \( N = 2^{15} \). Keeping \( T \) unchanged, as \( N \) increases, the area of the PPU increases very slowly while the total area of all LLR memories is proportional to \( N \). Hence, for larger \( N \), PPU occupies a smaller percentage of the total area of a whole decoder. When list size \( L \) is fixed, as \( N \) increases, the latency reduction and area efficiency improvement compared with other decoders in the literature will be greater.

VI. CONCLUSION

In this paper, a reduced latency list decoding algorithm is proposed for polar codes. The proposed list decoding algorithm results in a high throughput list decoder architecture for polar codes. A memory efficient quantization method is also proposed to reduce the size of message memories. The proposed list decoder architecture can be adapted to large block lengths due to our hybrid partial sum unit, which is area efficient. The implementation results of our high throughput list decoder demonstrate significant advantages over current state-of-the-art SCL decoders.

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