Abstract—Since its inception the memristive fuse has been a good example of how small numbers of memristors can be combined to obtain useful behaviours unachievable by individual devices. In this work, we link the memristive fuse concept with that of the Complementary Resistive Switch (CRS), exploit that link to experimentally demonstrate a practical memristive fuse using TiOx-based ReRAM cells and explain its basic operational principles. The fuse is stimulated by trains of identical pulses where successive pulse trains feature opposite polarities. In response, we observe a gradual (analogue) drop in resistive state followed by a gradual recovery phase regardless of input stimulus polarity: echoing traditional, binary CRS behaviour. This analogue switching property opens the possibility of operating the memristive fuse as a single-component step change detector. Moreover, we discover that the characteristics of the individual memristors used to demonstrate the memristive fuse concept in this work allow our fuse to be operated in a regime where one of the two constituent devices can be switched largely independently from the other. This property, not present in the traditional CRS, indicates that the inherently analogue memristive fuse architecture may support additional operational flexibility through e.g. allowing finer control over its resistive state.

Index Terms—Memristor, RRAM, memristive fuse, complementary resistive switch, analogue memory

I. INTRODUCTION

The development of a bio-inspired computation paradigm capable of demonstrating practical applications has long been a holy grail of electronics and neuroscience research. This effort has been primarily driven by the immense opportunity to be found in the powerful complementarity that exists between the fast, reliable and precise Von Neumann-based computers and the self-adaptive, massively parallel and fault-tolerant biological systems we see in nature. However, efforts in that direction have so far been hampered by the sheer complexity involved in emulating biological processes in silico. Thus far, a number of approaches have tried to attack this problem by harnessing the power of Personal Computers (PCs) [1]. Micro-Processor Units (MPUs) [2], Field-Programmable Gate Arrays (FPGAs) and Graphics Processing Units (GPUs) [3] as well as bespoke systems exploiting analogue Complementary Metal-Oxide Semiconductor (CMOS) technologies [4], [5]. The common problem with these approaches, however, is that they all employ fundamental components and design methodologies originally conceived for Von-Neumann-based computation. The resulting power and area costs associated with building bio-inspired systems of any appreciable scale (e.g. see [6]) have prompted the evolution of alternative approaches.

Alexander Serb, Ali Khiat and Themistoklis Prodromakis are with the Nano Group, ECS, University of Southampton, Highfield, Southampton SO17 1BJ.
Corresponding author email: A.Serb@soton.ac.uk
This work was supported by EPSRC EP/K017829/1 and EU-FP7 RAMP.

One such approach exploits recent advances in the field of nanoelectronic devices that exhibit the phenomenon of resistive switching [7], often referred to as ‘memristors’ [8]. Memristors boast a simple, two-terminal structure and an ability to react to external voltage/current stimuli by changing their resistive states [9] as seen in the examples of Fig. 1a,b. These properties, in turn, allow them to act both as single-component memory elements (including synapses [10], [11], [12], [13]) and as computational elements [14], [15], which raises the possibility of shifting much neuro-computational complexity to new components designed specifically to exhibit biological neuron- or synapse-like characteristics. These behavioural aspects, in tandem with continuous advances in the electrical and scalability characteristics of memristors [16], [17] indicate a possible route towards truly scalable bio-inspired systems. The flexibility and possibilities offered by this approach are reflected in the variety of memristor implementations and biologically relevant applications investigated so far. These include synapse implementations (analogue synapses supporting Spike Timing-Dependent Plasticity (STDP) implemented through metal-oxide- (MOx) or Phase Change Memory-based (PCM) devices [18], [19], binary stochastic synapses through Spin-Torque Transfer (STT) devices [20] etc.), small neural networks [21], neural activity sensors [22] and a host of others, e.g. [23], [24].

Beyond their use as single-component memory/synapses, memristors can also exhibit interesting properties when op-
A. Memristor device fabrication and testing

The tested memristive devices are based on metal-insulator-metal (MIM) structure fabricated on 200 nm insulating SiO$_2$ film, which was thermally grown on silicon wafer. The bottom and top electrodes (BE, TE) were deposited via electron beam evaporation technique, where the active layer was deposited by reactive magnetron sputtering. All layers were patterned and defined by conventional optical lithography and lift-off processes. Oxygen plasma cleaning step was carried out before each material deposition for obtaining more reliable and better quality devices. The final stack consists of Pt/TiO$_x$/Pt/Ti with respective thicknesses of 10/25/10/5 nm. A Ti layer was needed for adhesion purposes and the resulting TiO$_x$ film was near stoichiometric. Figures 1(d,e) depict a schematic view and SEM micro-photograph of a single memristor cell respectively.

All experiments performed towards this work employed an upgraded version of the memristor characterisation instrument reported in [27]. All devices involved were probed directly on-wafer via a probe-card as illustrated in Fig. 3(d). The BE was always kept grounded and all quoted voltages refer to the TE.

B. Memristive fuse basic operation concept

The operation of the memristive fuse arises naturally from the resistive switching characteristics of its constituent memristors, and specifically the link between input voltage and degree of resistive switching under fixed-duration pulsed stimulation. The sensitivity of switching to input voltage amplitude can be assessed by applying a series of voltage pulse train ramps to each device and measuring the resistive state of the Device Under Test (DUT) at the end of each train as seen in Fig. 1(b) and described in detail in [28]. Subsequently the resistive state change precipitated by each voltage level tested is assessed and the relation between resistive state change ($\Delta R$) and applied voltage is summarised in a ‘voltage sensitivity’ plot (or ‘switching’ plot). Measured and fitted switching plots for pulse duration fixed at 100 $\mu$s are shown in Fig. 2(a) for the two devices used to implement the memristive fuse in section III. The fitting model used is a simple, empirical, four parameter model:

\[
\text{parameter model:}
\]

Such unconventional components that find no direct equivalent in nature may prove useful for complementing the field of bio-inspired computation (‘beyond bio-inspired computation’). In this work, we experimentally demonstrate a practical memristive fuse consisting of two metal-oxide-based solid state memristors and show how its intrinsic properties allow it to function as a rudimentary step detector. Section II describes the typical behaviour of individual memristors, presents measured electrical characterisation data from solid-state devices and explains how two exemplars can be combined to result in a memristive fuse. Section III shows experimental results illustrating fuse behaviour whilst section IV provides a brief overview of practical fuse operation considerations including avenues for further exploration. Finally, section V concludes the paper.
Fig. 3. Memristive fuse implementation: a) Switching function for the two devices used to construct the memristive fuse and fittings to model in eq. \( \text{eq.} \). Associated fitting parameters are in Table I. Convention for forward and reverse bias regions (pale blue and red respectively) of memristor operation also shown. b) Connectivity of test devices for memristive fuse experiments in this work. c) Example of a ‘switching load line’ for the two devices from (a) connected as indicated in (b) and with pulse bias voltage \( V_b \) slightly lower than 3 V.

![Diagram of memristive fuse implementation](image)

**TABLE I**

| Parameter | M1 | M2 | Units |
|-----------|----|----|-------|
| \( V_{th}^+ \) | 1.07 | 0.71 | V |
| \( V_{th}^- \) | -0.52 | -0.45 | V |
| \( a_+ \) | 235.2 | 439.4 | \( \Omega/V^2 \) |
| \( a_- \) | -91.8 | -298.2 | \( \Omega/V^2 \) |

Base resistive state: \( \approx 3.3 \) \( \Omega \)
Resistive state range: \( 3.0 - 3.6 \) \( \Omega \)

\[ \Delta R(V_b) = \begin{cases} 
  a_+ \cdot (V_b - V_{th}^+)^2, & V_b > V_{th}^+ \\
  0, & V_{th}^- < V_b < V_{th}^+ \\
  a_- \cdot (V_b - V_{th}^-)^2, & V_b < V_{th}^- 
\end{cases} \]  

where \( \Delta R(V_b) \) is the change in resistive state, \( a_+, a_- \) fitted scaling parameters, \( V_{th}^+, V_{th}^- \) the fit-estimated thresholds of the memristor and \( V_b \) the bias voltage applied across it. Memristor resistive state read-out operations are in all cases carried out at a standardised read-out voltage of \(+0.2 \) V and resistive state is formally defined as static resistance at that voltage level. This is necessary in order to provide a comparable means of assessing resistive state for devices that may feature non-linear I-V characteristics.

The shape of the switching plot strongly determines memristive fuse operation: drawing inspiration from the load line analysis technique we can combine the switching load line for an anti-serial connection of two devices as shown in Fig. 3(b). Fig. 3(c) shows a load line example for switching under positive bias voltage \( V_b \). Because of the anti-serial connection, the switching load line consists of the positive \( V_b \) segment of the voltage sensitivity function of M2 and the negative \( V_b \) segment for M1. Given some initial resistive state for each device and assuming that the voltage-dependence of the switching rate of each device is relatively independent of its running resistive state (approximately true within a sufficiently small resistive state range) we can use the switching load line to start extracting information on the expected, conceptual behaviour of the memristive fuse.

We begin by noting that pulsing the memristive fuse at \( V_b \) will always cause M1 and M2 to experience an decrease/increase in their resistive states respectively and hence their potential divider voltage \( (V_x) \) increases with each applied pulse, as marked in Fig. 3(c). Notably, the precise trajectory of \( V_x \) will depend on both the shape of the switching plot and the precise shape of the IV curves of the devices involved, but the effects are always the same: a) the balance of voltage distribution between the two devices in the divider shifts from one device to the other and b) eventually, M2 will saturate at its operational resistive state ceiling (‘reset’ process) and M1 will saturate at its resistive state floor (‘set’ process) therefore stabilising the memristive fuse at a relatively high resistive state; similar to the HRS state in the traditional, binary CRS.

Furthermore we observe that the pulse voltage amplitude has been set in such way that the switching load lines form a ‘bottleneck’, i.e. a region in the divider voltage space whereby both memristors experience relatively small changes in resistive state. For appropriate initial values of \( V_x \) (as in example of Fig. 3(c)) the net effect is that during the early stages of pulsing at constant amplitude \( V_b \) the memristive fuse will experience a drop in overall resistance driven by M1 whilst in later stages it will experience a rise in overall resistance driven by M2. This intermediate stage where the fuse features relatively low resistive state is similar to the traditional CRS LRS where both devices in the complementary switch are at their resistive state floors. Memristive fuse operation is similar when the polarity of \( V_b \) is reversed. We have thus created a simple, analogue circuit component that encodes the accumulation of many same polarity pulsing events as an HRS whilst reacting to unexpected, anti-polar pulsing events by dropping its resistive state, as shown in Fig. 3(e).

III. EXPERIMENTAL RESULTS

The proposed memristive fuse topology was tested experimentally using the devices from Fig. 3(a) connected anti-serially as illustrated in Fig. 3(a). Results are shown in Fig. 4. Following initialisation to a saturated state the memristive fuse reacts to two trains of pulses with opposite polarities and suitably chosen amplitudes in a qualitatively similar manner: exhibiting a sharp, initial ‘dip’ followed by a slower ‘recovery’ phase as projected.

We notice that the two ‘dip and recovery’ responses are subtly different. With negative stimulus polarity the dip is
operating regimes is a complex topic that merits further,
interrelation between operating voltages and memristive fuse
inaccessible in the traditional CRS topology. The precise
their operational resistive state ceilings; a situation normally
exert control on only one of the two devices in the memristive
requires further, dedicated study. The ability to selectively
of M1 and if so under what specific biasing circumstances
M2 can be achieved throughout the entire resistive state range
voltage sensitivity plot for M2, although at higher voltages in
comparison to solo operation of M2. Whether this isolation of
M2 can be achieved throughout the entire resistive state range
of M1 and if so under what specific biasing circumstances
requires further, dedicated study. The ability to selectively
exert control on only one of the two devices in the memristive
fuse may allow access to far more flexible modes of fuse
operation, for example opportunities to set fuse resistive state
to an `ultra-HRS` level where both constituent memristors at
their operational resistive state ceilings; a situation normally
inaccessible in the traditional CRS topology. The precise
interrelation between operating voltages and memristive fuse
operating regimes is a complex topic that merits further,
dedicated study.

IV. Discussion

In this work we used a simplified description of memristor
operation in section II in order to offer a basic, concept-
level explanation of the observed fuse ensemble functionality.
However, practical memristive devices typically exhibit rich
dynamics far beyond what our ‘well-behaved’ switching plots
can capture. Let us review our assumptions and consider the
implications when they no longer hold:

‘The switching plot can be modelled by a monotonic
function of bias voltage’: In practice it has been observed
that devices can exhibit non-monotonic switching plots like
the example in [28] (Fig. 4(b2)) where the switching plot
exhibits a curvature reminiscent of \( f(x) = a \cdot x^3 \). Such
switching characteristics would imply that the switching load-
lines in Fig. 3(c) might cross for appropriately selected bias
voltages and thus automatically define fixed points that the
memristive fuse could be forced to converge to (attractors) if
initialised within the corresponding basin of attraction (Fig.
6(a)). Nevertheless, so long as the memristive fuse constituent
devices are operated at a voltage where the switching load
lines do not cross, the fundamental behaviours seen in section
III are in principle preserved.

‘The switching function is independent of running resistive
state’: In practice this dependence can be very complex, but in
the simple case where running resistive state influences switch-
ability in an approximately multiplicative way we can describe
the effect through a window function which ‘stretches’ the
switching function (and therefore also the switching load-
lines in Fig. 3(c)) might cross for appropriately selected bias
voltages and thus automatically define fixed points that the
memristive fuse could be forced to converge to (attractors) if
initialised within the corresponding basin of attraction (Fig.
6(a)). Nevertheless, so long as the memristive fuse constituent
devices are operated at a voltage where the switching load
lines do not cross, the fundamental behaviours seen in section
III are in principle preserved.

In this work we used a simplified description of memristor
operation in section II in order to offer a basic, concept-
level explanation of the observed fuse ensemble functionality.
Overall, in this work we have: a) presented an analogue generalisation of the well-known CRS concept, b) provided a simple and intuitive link between basic device characteristics and expected memristive fuse operation, c) showed experimental evidence of fuse behaviour in metal-oxide memristor pair ensembles and d) made some important observations regarding the expected influence of three key memristor properties on the precise fuse characteristics (voltage sensitivity of switching, resistive state-dependence of switching, I-V non-linearity). We have also concluded that whilst they will undoubtedly affect behaviour quantitatively, the qualitative aspects of fuse behaviour are expected to be conserved so long as a few simple but fundamental assumptions hold. Our discussion highlighted the emergence of a wealth of complexities as the traditional, binary CRS is generalised to a memristive fuse; complexities that must either be mitigated to allow good single-component step detector operation or engineered to allow the memristive fuse to fulfil entirely different functions in a single component (both currently under investigation). Finally, we have offered a glimpse into how the inherent properties of the proposed memristive fuse may allow it to find interesting applications, exemplifying its ability to act as a simple, two-terminal, single-component step detector.

V. Summary

Fig. 6. Understanding the complexity of the memristive fuse behaviour. a) If switching functions are not monotonic in $V_x$ then the fuse can potentially react to stimuli of appropriate amplitude $V_b$ by converging their resistive states towards/away from specific attractors/repellers. b) The dependence of switching voltage sensitivity to the running resistive state of each constituent device of the fuse implies that as the fuse changes state the switching load line and consequently the shape of the ‘bottleneck’ area is constantly being reshaped. c) Non-linearities and asymmetries in device I-V render predicting line and consequently the shape of the ‘bottleneck’ area is constantly being reshaped. d) Non-linearities and asymmetries in device I-V render predicting line and consequently the shape of the ‘bottleneck’ area is constantly being reshaped.

a) Change in ‘as measured’ $R(M_1) / R(M_2)$ ratio translates into a shift of the potential divider voltage in the expected direction the qualitative behaviour of the memristive fuse will be preserved. The precise conditions under which this shall occur are a subject of further study. The memristive fuse’s intrinsic properties hint towards some interesting applications: The observed relationship between dip and recovery indicates an inherent ability of the fuse to respond quickly and strongly when a series of many pulses of the same polarity is suddenly interrupted by stimuli of the opposite polarity, i.e. to detect sudden changes in input signal polarity regardless of the actual polarities of all stimuli involved. This opens up the possibility for the application of the memristive fuse as a rudimentary, single-component step detection element for bio-inspired computation. When operated in such manner long series of same polarity events in the input data-stream will be encoded into high fuse resistive state. In biological terms, the memristive fuse will therefore act as a ‘direction of change-independent’ variation of the classical adaptable neuron 1. Notably, higher level applications exploiting this behaviour have already been proposed where memristors are connected in square 26 or hexagonal 30 pixel grids, i.e. connectivity patterns similar to those observed in the outer plexiform layer of the retina 31, for the purpose of image edge detection in a biomimetic fashion.

1Which responds to sudden increases in input stimulation with a transient increase in its firing rate.

References

[1] H. Markram, “The blue brain project,” Nature Reviews Neuroscience, vol. 7, no. 2, pp. 153–160, 2006.
[2] S. B. Furber, F. Galluppi, S. Temple, and L. A. Plana, “The spinnaker project,” Proceedings of the IEEE, vol. 102, no. 5, pp. 652–665, 2014.
[3] L. E. Givon and A. A. Lazar, “Neurokernel: An open source platform for emulating the fruit fly brain,” PloS one, vol. 11, no. 1, 2016.
[4] N. Qiao, H. Mostafa, F. Corradi, M. Oswald, F. Stefanini, D. Sumislawski, and G. Indiveri, “A reconfigurable on-line learning spiking neuromorphic processor comprising 256 neurons and 128k synapses,” Frontiers in neuroscience, vol. 9, p. 141, 2015.
[5] J. Schemmel, D. Briiderle, A. Gribl, M. Hock, K. Meier, and S. Millner, “A wafer-scale neuromorphic hardware system for large-scale neural modeling,” in Proceedings of 2010 IEEE International Symposium on Circuits and Systems, May 2010, pp. 1947–1950.
[6] E. Stromatias, F. Galluppi, C. Patterson, and S. Furber, “Power analysis of large-scale, real-time neural networks on spinnaker,” in Neural Networks (IJCNN), The 2013 International Joint Conference on, Aug 2013, pp. 1–8.
[7] R. Waser and M. Aono, “Nanoionics-based resistive switching memories,” Nature materials, vol. 6, no. 11, pp. 833–840, 2007.
[8] L. Chua, “Memristor-the missing circuit element,” IEEE Transactions on circuit theory, vol. 18, no. 5, pp. 507–519, 1971.
[9] L. O. Chua and S. M. Kang, “Memristive devices and systems,” Proceedings of the IEEE, vol. 64, no. 2, pp. 209–223, 1976.
[10] P.-F. Chiu, M.-F. Chang, C.-W. Wu, C.-H. Chuang, S.-S. Sheu, Y.-S. Chen, and M.-I. Tsai, “Low store energy, low vddmin, 802 nonvolatile latch and sram with vertical-stacked resistive memory (memristor) devices for low power mobile applications,” Solid-State Circuits, IEEE Journal of, vol. 47, no. 6, pp. 1483–1496, 2012.
[11] T. Serrano-Gotarredona, T. Masquelier, T. Prodromakis, G. Indiveri, and B. Linares-Barranco, “Stdp and stdp variations with memristors for spiking neuromorphic learning systems,” 2013.
[12] S. L. Wei, E. Vasilaki, A. Khiat, I. Salaoru, R. Berdan, and T. Prodromakis, “Emulating long-term synaptic dynamics with memristive devices,” arXiv preprint arXiv:1509.01998, 2015.
[13] H. Mostafa, A. Khiat, A. Serb, C. G. Mayr, G. Indiveri, and T. Prodromakis, “Implementation of a spike-based perceptron learning rule using ti0.2 x memristors,” Frontiers in neuroscience, vol. 9, 2015.
[14] R. Berdan, E. Vasilaki, A. Khiat, G. Indiveri, A. Serb, and T. Prodromakis, “Emulating short-term synaptic dynamics with memristive devices,” Scientific reports, vol. 6, 2016.
Alexander Serb (M’11) is a research fellow at the Electronics and Computer Science (ECS) dept., University of Southampton, UK. His research interests are: instrumentation, algorithms and applications for RRAM testing, and neuro-inspired engineering.

Ali Khiat is an Experimental Officer at Southampton Nanofabrication Centre, University of Southampton. His current main research interests are micro-/nanofabrication, optimisation, metrology and characterisation of memristors and memristive devices.

Themistoklis Prodromakis (M’08) is a Reader in Nanoelectronics and EPSRC Fellow at the Nano Group and the Southampton Nanofabrication Centre of ECS at University of Southampton. His research interests are on bio-inspired devices for biomedical applications.