A thin silicon thermoelectric nanowire characterization platform (TNCP) equipped with nanoporous electrodes for electrical contact formation

S. Hoda Moosavi1*, Michael Kroener1, Maxi Frei2, Fabian Frick1, Sven Kerzenmacher2, and Peter Woias1

1Laboratory for Design of Microsystems, Department of Microsystems Engineering – IMTEK, Freiburg, Germany, 2Laboratory for MEMS Applications, Department of Microsystems Engineering – IMTEK, Freiburg, Germany

*Email: hoda.moosavi@imtek.uni-freiburg.de

Abstract. We report on the fabrication of a silicon platform for the thermoelectric and structural characterization of single nanowires, equipped with nanoporous electrodes. Controlled wafer thinning to a thickness of 160 µm results in platform chips, which can be inserted into Transmission Electron Microscopes (TEM) for the nanowire’s structural composition analysis. Our fabrication approach comprises the Bosch process (ICP), and “dicing before grinding” techniques to achieve this small thickness. To study the idea of developing a “plug-and-measure” platform, we have developed a novel approach for self-adhesion between a contact electrode and a nanowire by nanoporous electrodes. Due to the increased surface-to-volume ratio and increased van-der-Walls forces nanowires stick firmly to the electrodes for a good thermal and electrical connection. This innovative technique does also avoids, in best case, separate steps for contact formation.

1. Introduction
The day-by-day increasing demand for energy sources, fossil fuels, and other scarce resources reveals the indispensability of development of “clean” energy supplies. Among most of the energy-consuming technical processes waste heat is eventually dissipated into the ambient and not used further. Thermoelectric energy harvesting, which uses this else lost energy to power small embedded systems, offers a chance to thereby improve energy efficiency. Therefore, lots of effort has been put into the search for finding better thermoelectric materials [1–3]. Due to enhanced scaling effects, thermoelectric nanostructures are predicted to be more efficient compared to bulk material [4]. This, however, must be examined precisely for nanostructures, such as nanowires. The presented platform is designed to measure these properties and its functionality is proven by a thermoelectric nanowire assembled to it by means of dielectrophoresis phenomena [3]. Yet, nanowire assembly alone is not a guarantee to get a proper electrical contact between electrodes and the nanowire. Different techniques are available to form such an electrical contact; these are focused ion beam deposition (FIB) [1], as well as using shadow masks [3]. Both techniques are time-intensive approaches and require special facilities to be performed. Another wafer-scale, assembly technique is based on covering the electrodes with low temperature solders [5]. That technique, however, relies on a complicated
cleanroom process. Here we suggest improving the contact by making the platform electrodes nanoporous. The porous platinum electrodes are fabricated by a special electro deposition technique [6,7]. As a result of the increased surface-to-volume ratio the stickiness between the nanowire and the electrode is increased. This can be taken as a proof of concept, indicating that surface treatment investigations in this field are promising.

2. Thermoelectric Nanowire Characterization Platform (TNCP)
Several platforms for thermoelectrical nanowire characterization have been developed [8–10]. However, a comprehensive investigation of the specimen’s thermoelectric behaviour also relies on studying its chemical composition and growth direction. We have therefore developed the first platform enabling thermoelectric measurement in addition to structural analysis via Transmission Electron Microscopy (TEM) [3,5,11,12]. TEM compatibility requirements include a suspended specimen to avoid electron scattering, and also a TNCP chip diameter less than 3 mm, and a thickness of less than 200 µm.

2.1. TNCP design
Our final TNCP design, a silicon chip of 2 mm × 2 mm × 160 µm, includes a membrane structure to assure a proper thermal insulation during measurements, as well as low electron scattering in the TEM. It also is equipped with measurement electrodes and micro heaters for the Seebeck measurements. The TNCP design is shown in Figure 1.

![Figure 1. The TNCP design.](image)

2.2. TNCP fabrication
The fabrication process starts with a 380 µm thick silicon wafer, coated with 300 nm SiO₂/Si₃N₄ (Fig. 2-a). The wafer’s frontside is processed with Pt sputtering, lithography and IBE to generate the metallization structure, followed by a backside and frontside etching at the mask layer via lithography and RIE process in succession (Fig. 2-b). STS-ICP is performed to form the 360 µm deep backside trenches (Fig. 2-c). In another step, an ICP process is utilized to open the 20 µm frontside trenches

![Figure 2. TNCP Fabrication processes.](image)

![Figure 3. Veeco [wyko NT 9100] white light profilometer results, (a): scanning the TNCP backside indicates the chip’s proper thickness of 160 µm. (b): profilometer image from the TNCP’s backside trench. The membrane thickness is (appr.) 20 µm.](image)
and to generate the membrane structure (Fig. 2-d). However, it is very probable that as soon as the trench is opened, the plasma penetrates to the membrane’s backside and causes underetching. Protective resist spin coating is not an option due to the large aspect ratio of the opening in the backside. This problem was solved by modifying the ICP process. The wafers exposed to the plasma in ICP are Helium cooled from the backside. By reducing the maximum Helium flow rate from 25 to 16 SCCM, as soon as a through hole is generated in the wafer, the Helium leak rate increases and the process is terminated automatically. With this process modification the expected membrane thickness is reached (Fig. 3-b), without the requirement of expensive SOI wafers. Afterwards the wafer is partially diced to a depth of 160 µm. 220 µm rear grinding is performed at DISCO Hi-TEC Europe GmbH which leads to the diced 160 µm TNCP platforms (Fig. 2-e, Fig. 3-a).

3. Nanoporous Platinum

It has been shown that a Bi₂Te₃ nanowire assembled onto the TNCP shows a contact resistance in the order of GΩ [3], indicating that no electrical contact with the underlying platinum layer is established. If the nanowire would be automatically contacted after the assembly, without the need for further processing, this would highly increase the platform’s ease-of-use. Our idea is to contact the nanowire by maximizing the area between the nanowire and the electrode surface, making use of Van-der-Waals forces. We also assume that current will find more ways of flowing through thin non-conductive layers on the nanowire surface (e.g. oxide) which otherwise prohibit electrical contact. The larger contact surface in our approach is achieved by producing nanoporous platinum electrodes.

3.1. Fabrication

Our strategy for fabrication of porous platinum relies on the galvanic co-deposition of Cu and Pt, and subsequent electrochemical dealloying of the non-noble Cu component. Deposition and dissolution times have strong influence on the structure and stability of the layers, with high ratios of dissolution-to-deposition time leading to less dendritic structures. The optimized time for deposition and dissolution is found to be 9 s and 4.5 s, respectively [6]. The deposition and dealloying potentials are -0.5 V and 0.7 V, respectively. Using these parameters, we performed several deposition cycles to find the suitable number for our application. As a result, already one cycle gives rise to the expected porous structure, as shown in Figure 4-a.

![Figure 4. (a): SEM-picture of the porous electrodes of TNCP. (b): A nanowire assembled on the realized nanoporous Pt electrodes by dielectrophoresis phenomena.](image)

3.2. Measurement

The nanowire assembly to the platform is performed using dielectrophoresis technique [3], as shown in Figure 4-b. As a result of increased surface-to-volume ratio the stickiness between the nanowire and the electrode is increased. A good clue for that is shown in Figure 5-a. The nanowire breakage over the gap happened during droplet evaporation in a dielectrophoresis assembly. The force from the droplet pressure change during the evaporation was higher than the mechanical strength of the nanowire and fractured it in the gap. Yet, the remaining parts of the nanowire on the electrode were intact and unmoved. This observation demonstrates that the stickiness between the nanoporous electrodes and the nanowire is enhanced due to an increased contact surface area. In the electrical measurements, a two point measurement on an assembled Bi₂Te₃ nanowire yields a resistance value of 0.92 MΩ ± 0.06 MΩ (Fig. 5-b). This magnitude in comparison to the GΩ values obtained on unprocessed TNCPs reported by [3] shows an enhancement. Although no reliable electric contact is achieved (which would
be approximately 2000 Ω [12]), still the surface treatment for automatic nanowire assembly to the electrodes deserves further investigation.

Figure 5. (a): The electrode and nanowire adhesion enhancement. (b): I-V curve of a Bi$_2$Te$_3$ nanowire, on a porous electrode.

4. Conclusion and outlook
We have successfully fabricated a TEM compatible chip for nanowire characterization. The fabrication is based on the dicing before grinding technique. We have presented the electrodeposition parameters to achieve a nanoporous micro electrode. The nanowires assembled to such a platform stick properly to the electrodes as a result of the enhanced common area. The electrical measurement showed a reduced resistance between nanowire and the nanoporous electrode, compared to planar electrodes. To sum up, although no reliable electrical measurement is achieved, still this proof of concept indicates that surface treatment investigation in this field can be promising. For future experiments, it would be desirable to get the nanowires into even closer physical contact with the electrode, for example by letting the nanowire to sink into and be surrounded by a nanowire grass grown on the electrodes.

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References
[1] D. Kojda, R. Mitdank, et al. 2014 Semicond. Sci. Technol. 29 124006. doi:10.1088/0268-1242/29/12/124006
[2] D. Kojda, R. Mitdank, et al., 2015 Phys. Rev. B 91 1–13. doi:10.1103/B.91.024302
[3] Z. Wang, S.H. Moosavi, et al. 2015 in: O. Eibl, K. Nielsch, N. Peranio, F. Voelklein (Eds.), Thermoelectric Bi$_2$Te$_3$ Nanomater., first, Wiley
[4] L.D. Hicks, M.S. Dresselhaus, 1993 Phys. Rev. B 47 16631–16634. doi:10.1103/B.47.16631
[5] S.H. Moosavi, M. Kroener and P. Woias 2016 Sens. Actuators A: Phys., http://dx.doi.org/10.1016/j.sna.2016.05.006
[6] C. Köhler, A. Kloke, et al. 2013 J. Power Sources. 242 255–263. doi:10.1016/j.jpowsour.2013.05.035
[7] A. Kloke, C. Köhler, et al., 2012 Adv. Mater. 24 2916–2921. doi:10.1002/adma.201200806
[8] S. Karg, P. Mensch, et al., 2013 J. Electron. Mater. 42 2409–2414. doi:10.1007/s11664-012-2409-7
[9] L. Shi, D. Li, et al., 2003 J. Heat Transfer. 125 881. doi:10.1115/1.1597619
[10] F. Voelklein, M.C. Schmitt, et al. 2011 in: A. Hashim (Ed.), Nanowires - Implementations Applications, doi:10.5772/19656
[11] S.H. Moosavi, M. Kroener and P. Woias 2015 Procedia Eng. 120 210–214. doi:10.1016/j.proeng.08.612
[12] Z. Wang, S.S. Adhikari, et al., 2013 IEEE 26th Int. Conf. Micro Electro Mech. Syst., pp. 508–511. doi:10.1109/MEMSYS.2013.6474290