Design and Implementation of Wireless Transmission System Based on Zedboard and AD9361

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Abstract. With the development and application of software radio technology, WLAN communication protocol shows great advantages. This design uses Zedboard system board and AD9361 radio frequency board to build software radio platform, designs a point-to-point wireless transmission system based on COFDM. The experimental results show that the system can transmit data stably.

1. Introduction

COFDM is a multi-amplitude and multi-frequency modulation mode. The influence of wireless channel environment will result in the wrong transmission of data on some subcarriers, and channel coding is an effective compensation technique. Error codes on deep fading subcarriers can be corrected by channel coding [1].

Considering the current development of software radio, the Zynq-7000 [2] full-programmable chip of Xilinx Company is adopted as the core chip of software radio, and the RF module is built with AD9361 agile radio transceiver to build the whole software radio platform. In addition, combined with COFDM technology, the design of point to point wireless transmission system is completed.

2. Hardware architecture

2.1. Hardware platform

The hardware architecture of the system is mainly composed of Zedboard and RF modules. Zedboard is responsible for receiving video data streams and processing baseband signals. The AD9361 RF module is responsible for A/D and up/down conversion, sending signals to the wireless channel.

The Zedboard [3] processor platform is characterized by two parts, the Processing System and the Processing Logic. The processor system consists of two ARM Cortex-A9 processors. The programmable logic device resources include 215K logic units and 13 Mb BRAM, which can be used to speed up logic design. Data is transferred between PS and PL through AXI bus [5]. In this way, ARM is used as software control unit and FPGA is used as hardware acceleration unit. The coordination design of Hardware and software controls the wireless transmission of the whole system data stream.

The AD9361 [6] operating frequency range is 70 MHz to 6 GHz, covering most of the licensed and license-free bands, supporting tunable 200 kHz to 56 MHz channel bandwidth. The transmitter uses a direct frequency conversion architecture to achieve higher modulation accuracy and lower noise [6]. At the same time, the standard FMC interface is provided to achieve seamless connection with Zedboard.
2.2. Transmission Hardware architecture

![System Architecture - Transmission](image1)

![System Architecture - Receiving](image2)

**Figure 1.** Structure block diagram of wireless video transmission system

The wireless transmission system architecture based on COFDM is shown in Figure 1. (a) and (b) represent respectively sender and receiver of the system. The depth of video data captured by the digital camera is 24 bits, the frame rate is 60 fps, the resolution is 1080P and the compressed data rate is 14.93 Mbps. Video stream is transmitted to Zedboard through Ethernet port. Under control of upper application program of PS, data stream is transmitted to PL part via AXI bus after cache. After the baseband processing modules such as channel coding, modulation and IFFT transform, the complete COFDM frame is transmitted to AD9361 through FMC bus, and the digital signal is converted into analog signal and sent out by antenna.

At the receiving, the signal is received by antenna. After converting into digital signal by AD9361, the digital data is sent to Zedboard through FMC bus for baseband inverse processing, and finally sent to the data processing device through the network port.

3. Software system

3.1. Baseband system

![Baseband system - Transmission](image3)

![Baseband system - Receiving](image4)

**Figure 2.** Baseband system
As shown in Figure 2, the baseband system is implemented on the basis of OFDM technology. The data stream is sent down to the baseband processing module in byte form through AXI bus and converted into serial bit stream and then entered the scrambler, the purpose is to avoid the occurrence of long string 0 or 1, which is helpful to the timing recovery of the receiver. After that, the data is used in the forward error correction coding. The convolutional coding method with variable code rate is adopted here. In order to avoid the burst errors on the receiver decoding, the encoded data need to be interleaved. The interleaved data stream is mapped to in-phase (I) and quadrature (Q) signals by 16QAM. After inserting the pilot, the interleaved data stream is modulated to each carrier by IFFT processing. Then the preamble sequence is added to form a complete COFDM frame and sent to AD9361. Due to the flexibility of software radio, different coding rates and modulation modes can be selected according to different transmission conditions to obtain the transmission rates ranging from 6Mb/s to 54Mb/s [7]. Adopting 64-point IFFT means that the sampling interval is 0.05us, so the sampling frequency should be at least 20Msample/s, so the main clock frequency of the system is set to 20MHz.

The receiving process is to achieve the reverse operation opposite to the transmitter. AD9361 divides the received data into I/Q channels and sends it to the synchronization module after frequency conversion and digital-to-analog conversion. After synchronization, the data is transformed by FFT and sent to the channel compensation module. After compensating the amplitude and phase of the subcarriers, the data can be demodulated, de-interleaved, then sent to the decoder for channel decoding, and finally restored to the original bit stream data.

3.2. Frame structure

Figure 5 shows the COFDM frame structure, which consists of two parts: frame head and valid data. The frame head consists of three parts: short training sequence, long training sequence and signaling [7].

The timing synchronization, carrier frequency offset estimation and channel estimation of the receiver are all performed by training symbols. The signal symbol contains the type of modulation, the encoding rate and the length of the data, which are very important to the receiver. Data symbol contains useful information.

![Figure 3. Frame structure](image)

3.3. Upper control system

For the convenience of software development, Xilinx platform provides a LWIP protocol stack [8] for embedded development. This protocol can be regarded as a simplified version of TCP/IP protocol, with which software development is greatly facilitated. The upper layer control software system flow is shown in Figure 6.

First, initialize the LWIP protocol stack, then receive network packets, send and receive data through Ethernet. The data transmission of Ethernet is based on IP address and MAC address of master and slave device. At first, the system sent ARP broadcast packets. The receiver receives the ARP packet and makes a judgment. After judgment is passed, an ARP reply packet will be fed back and the sender's MAC address will be told. The sender sends the packet containing destination IP and MAC address to receiver according to MAC address. After receiving packets, the receiver determines whether UDP packets or TCP packets. UDP packets are discarded directly, and TCP packets are sent to the underlying physical link.
3.4. Configuration and control of AD9361

During the configuration process, AD9361 register control information is written to memory (DDR) on Zedboard through Ethernet interface, then transmitted to RF end through SPI interface to realize RF parameter and working state configuration.

The working state of AD9361 is controlled by state machine. It is operated by FDD and TDD. The system adopts FDD mode. The specific state transition diagram is as follows [9]:

1) SLEEP: sleep state, disable AD9361 clock and baseband PLL
2) WAIT: wait state, turn off synchronization, reduce power consumption;
3) ALERT: alert state to enable synchronization;
4) FDD: enabling transmission and reception channels;
5) FDD FLUSH: refresh digital filter and digital link.
4. System test

4.1. Simulation and verification of communication links

In order to verify the performance of the system better, a set of wireless communication platform is built on Matlab. Figure 8 shows the setup interface of simulation platform, which can adjust the system parameters such as frame length, modulation mode and so on arbitrarily to verify the reliability of system in different situations.

![Figure 6. Simulation system configuration interface](image)

As shown, the bit error rate is almost 0.

![Figure 7. Simulation result](image)

4.2. Test and verification of wireless transmission system

Build the platform according to connection of Figure 1. The left side is sending end and receiver on the right side. After system is powered on, the card initializes automatically. When the blue light is on and the red light flashes, the transmitter and receiver begin to work.

![Figure 8. System object display](image)
As shown in Figure. 11, the bandwidth of waveform is about 20MHz, and the central carrier is about 2.435GHz. According to the results, the relevant parameters of AD9361 are correctly configured and the system works normally.

![Emission signal spectrum](image1)

**Figure 9.** Emission signal spectrum

Figure 12 shows the real-time video sent and received. By contrast, the picture is consistent.

![Video picture](image2)

**Figure 10.** Video picture

5. **Conclusion**

In this paper, a point-to-point video transmission system is designed and implemented based on Zedboardand COFDM software radio platform, and the implementation process of key modules of system is introduced in detail. After testing, the system can stably modulate and demodulate data, and can complete the real-time transmission of video, which verifies the availability and correctness of the system. The system has short development cycle, low power consumption, high expansibility and flexibility, and has a good application prospect.
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References
[1] Qiaopin Liu, Juntang Dong. Application of OFDM technology in 4G mobile communication system [J]. Electronic Test, 2014, (05): 102-104.
[2] Crockett L H. The Zynq book : embedded proces-sing with the ARM Cortex-A9 on the Xilinx Zynq-7000 all programmable So C [M]. Strathclyde Academic Media, 2014.
[3] Pengren Ding. Design and Implementation of Software Radio Platform Based on ZYNQ [D]. Beijing: Beijing University of Posts and Telecommunications, 2015.
[4] Yinyu Zhang. Implementation of IEEE802.11 Physical Layer Communication Based on Zedboard [D]. Beijing: Beijing University of Posts and Telecommunications, 2015.
[5] Liang Fang. Design of video transmission system based on Zedboard and software radio [J]. Electronic Design Engineering, 2017, 25 (01): 148.
[6] Hao Jiang, Zhi Zhang. Design and implementation of Software Defined Radio Platform Based on AD936 [J]. Video Engineering, 2015, 39 (15): 53.
[7] Zhiguo Zhi, Shaohua Hong, Kangsheng Chen. Baseband Design of OFDM communication system based on XILINX FPGA [M]. Zhejiang: Zhejiang University Press, 2009.
[8] Dong Kong, Jianhong Zheng. Transplantation and application of embedded TCP/IP protocol stack LWIP on ARM platform [J]. Communications Technology, 2008, (06): 38-40.
[9] Ze Hao. Design and implementation of software radio hardware platform based on AD9361 [D]. University of Electronic Science and technology of China, 2012.