Influence of active layer thickness on the cut-off frequency of a-IGZO thin film transistors

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Abstract. Design optimizations like channel length and gate/contact overlap length scaling are generally used for cut-off frequency ($f_T$) enhancement of thin film transistors (TFT). But channel length scaling leads to mobility degradation due to contact resistance ($R_C$). $R_C$ in TFTs is directly proportional to the transfer length ($L_T$), and is inversely proportional to the overlap length ($L_OV$). $L_T$ depends upon the metal/semiconductor interfacial resistivity, the vertical bulk resistance and the semiconductor sheet resistance. For the same interfacial contact properties, active layer thickness ($T_a$) scaling can be effectively utilized for lowering the vertical bulk resistance thereby lowering $L_T$ and enhancing $f_T$. To study the effect of thickness scaling on the bandwidth of TFT based amplifiers, a-IGZO thin film transistor of effective channel thickness of 70nm is first fabricated and characterized. Density of states model of this TFT is extracted and numerical simulations are used to study the influence of active layer thickness scaling. By varying the channel lengths from 10µm to 100µm, transfer line method of contact resistance estimation, is used to extract $L_T$ and $R_C$ of devices. As the active layer thickness is varied from 70µm to 30µm it is found that $L_T$ decreases from 1 µm to 60 nm, due to lower vertical bulk resistance. This results in a lower $R_C$ and higher $\mu_{\text{eff}}$, facilitating further scaling of $L_OV$, leading to enhanced $f_T$ of the device.

1. Introduction
Amplifier circuits using amorphous-Indium Gallium Zinc Oxide (a-IGZO) semiconductor based thin film transistors (TFTs), have been widely reported [1]-[3], but their practical applications still remain limited due to certain bottlenecks inherent to the technology like low transconductance originating from low intrinsic mobility, higher process margins required and higher susceptibility to process variations which especially challenge the implementation of analogue circuits like amplifiers using a-IGZO TFTs. None of the reported amplifier with a usable gain above 15dB was able to achieve MHz operation. In amplifying applications, the device cut-off frequency ($f_T$) is one of the primary figure of merit and has to be simultaneously optimized along with intrinsic device gain. $f_T$ is defined as the frequency at which the current gain of a device equals unity. A transistor can be used as an amplifier upto this frequency, above it the transistor becomes an attenuator [4]. $f_T$ is related to transconductance


\( (g_m), \) gate capacitance \((C_{ch})\), effective mobility \((\mu_{eff})\), gate overdrive voltage \((V_{\text{dual}})\), channel length \((L)\), channel width \((W)\) and gate-contact overlap length \((L_{OV})\) as given below.

\[
f_T = \frac{g_m}{2\pi C_{ch}} = \frac{\mu_{\text{eff}} V_{\text{dual}}}{2\pi L (L + 2L_{OV})} \tag{1}
\]

The design optimizations that can be adopted for high frequency operation are channel length and overlap length scaling and operating the device at higher overdrive voltage while process optimizations resulting in enhanced mobility and lower threshold voltages can also be used to increase the operating bandwidth. While we go for the various design optimizations using \(L\) and \(L_{OV}\) scaling [5], the influence on the two critical parasitic components: overlap capacitance \((C_{OV})\) and contact resistance \((R_c)\), are the primary considerations. Channel length scaling without overlap length scaling leads to mobility degradation due to increased contribution from contact resistance towards the total device resistance. The relation between mobility and \(f_T\) is not straightforward as given in equation (1) and is interlinked to other design parameters, like \(L, V_{\text{dual}}\) and \(L_{OV}\) through the influence of \(R_c\) [5] as given below.

\[
\mu_{\text{eff, sat}} = \mu_0 (1 - \left( \frac{W_{\text{ox}} R_c V_{\text{dual}}}{L + \mu_0 W_{\text{ox}} R_c V_{\text{dual}}^2} \right)^2) \tag{2}
\]

\[
f_T = \mu_0 (1 - \left( \frac{\frac{\mu_0 W_{\text{ox}} R_c V_{\text{dual}}}{L + \mu_0 W_{\text{ox}} R_c V_{\text{dual}}^2} \right)^2) \frac{V_{\text{dual}}}{2\pi L (L + 2L_{OV})} \tag{3}
\]

\[
R_c = \frac{1}{\mu_0 C_{\text{ox}} W (V_{gs} - V_{th0})} \times L_T \times \coth \left( \frac{L_{OV}}{L_T} \right) \tag{4}
\]

\( R_c \) is related to transfer length \(L_T\) and \(L_{OV}\) by equation (4), where \(\mu_0, C_{\text{ox}}\) and \(V_{th0}\) are the intrinsic mobility, oxide capacitance per unit areaand intrinsic threshold voltage respectively. \(L_T\) represents the effective area of charge transfer between gate and the contact and is equal to \(\frac{r_{cy}}{r_{cx}}\). Here \(r_{cy}\) is the vertical component of contact resistance and is the sum of the interfacial contact resistance between the metal and the semiconductor, and the bulk resistivity of the vertical region of the semiconductor between the contact and the channel. Resistance \(r_{cx}\) is horizontal component equal to the sheet resistance of the channel. Reducing \(L_T\) reduces \(R_c\) and facilitates scaling of \(L_{OV}\) without mobility degradation. Scaling of \(L_{OV}\) reduces \(C_{OV}\) and enhances \(f_T\).

In this paper we analyze the effect of active layer thickness on device cut-off frequency. It is known that channel thickness scaling reduces the vertical bulk resistance associated with the channel region, hence reducing \(L_T\). Through TCAD simulations we first find the contact resistance and \(L_T\) of two sets of devices A and B, with active layer thickness 70nm and 30nm respectively, through the Transfer Line Method (TLM). Channel thickness is also prone to process variations and hence such a study can bring out the intensity with which the variation in semiconductor thickness can negatively influence circuit parameters.

2. Device Fabrication and Numerical Modelling

a-IGZO TFT devices were fabricated with channel length 40\(\mu\)m, width 100\(\mu\)m, source/drain contact length 20 \(\mu\)m and gate-contact overlap length 10\(\mu\)m. A 50 nm thick Mo gate electrode was formed on a glass substrate by DC sputtering and photolithography after which 80nm thick \(\text{Al}_2\text{O}_3\) gate dielectric was deposited by ALD. a-IGZO active layer was deposited by DC sputtering (Ar-50sccm, \(\text{O}_2\)-1sccm) with a target of mol percentage 1 : 1 : 1 (\(\text{InO}_3\) : \(\text{Ga}_2\text{O}_3\) : \(\text{ZnO}\) forming a 70nm thick active layer.
50nm thick Mo source/drain contacts were defined by DC sputtering and patterning as shown in figure 1(a). The devices were passivated using ALD deposited Al₂O₃ layer.

![Figure 1](image_url)

**Figure 1.** (a) Micrograph of the fabricated TFT (b) TCAD device dimensions

Current to density of states (DOS) mapping was used to extract the TCAD model of the a-IGZO based TFT geometry given in figure 1(b). The DOS parameters [6] of the a-IGZO TFT along with its material properties and interface parameters are varied to fit the simulated device transfer characteristics to that of the measured characteristics (see table 1). The DOS profile of the a-IGZO TFT, thus obtained, is used for the analysis and simulation of the TFT characteristics. An additional n+ doped layer of semiconductor below each contact emulates the realistic case of unintentional contact region doping which is seen in a-IGZO TFTs, where even metals with large workfunction difference with a-IGZO like Mo, acts as near ohmic contacts with very low contact resistance. This doped layer is assumed to be 10nm thick. The thickness of the active semiconductor layer (Tₐ) was set to 70nm (for devices of Set A) and 30nm (for devices of Set B) for the analysis of transfer length. W was fixed at 100μm, while L was varied from 10μm to 100μm for TLM studies. The contact length, Lc and overlap length, LOV were fixed at 20μm and 10μm respectively. Cox of 80 nm thick Al₂O₃ gate dielectric layer was measured from the MIM structures fabricated on the same substrate and was found to be 102nF/cm².

| Symbol | Value | Unit | Description                  |
|--------|-------|------|-------------------------------|
| N_C    | 5×10¹⁸ | cm⁻³ | Effective conduction band DOS |
| N_TA   | 1.55×10²⁰ | cm⁻³ | Shallow acceptor-like trap DOS |
| W_TA   | 0.03  | cm⁻³/ eV | Shallow acceptor-like trap slope |
| N_TD   | 1.55×10²⁰ | cm⁻³ | Shallow donor-like trap DOS |
| W_TD   | 0.110 | cm⁻³/ eV | Shallow donor-like trap slope |
| N_GA   | 3.2×10¹⁷ | cm⁻³ | Deep acceptor-like trap DOS |
| E_GA   | 1.2   | eV | Deep acceptor-like trap mean energy |
| W_GA   | 0.1   | cm⁻³/ eV | Deep acceptor-like trap slope |
| N_GD   | 1×10¹⁶ | cm⁻³ | Deep donor-like trap DOS |
| E_GD   | 2.95  | eV | Deep donor-like trap mean energy |
| W_GD   | 0.1   | cm⁻³/ eV | Deep donor-like trap slope |
3. Results and Discussion

Numerical simulations were used to extract the electrical characteristics of devices from Set A and Set B ($T_a$ of 70nm and 30nm respectively). Six devices from each set with channel lengths 10µm, 20µm, 40µm, 60µm, 80µm and 100µm were used to extract the contact properties using Transfer Line Method (TLM). The results from TLM analysis of the two sets are shown in figure 2. We find that higher value of $R_C$ (10kΩ) was reported in [7] with a third quadrant crossing of TLM lines for a film thickness of 70nm and Mo contacts, while extremely low values of $R_C$ (in tens of ohms and even approaching negative values) was reported for 40nm IGZO in [8] with a first quadrant crossing. The results for devices of Set A and Set B follow the same trend and figure 2 (c) and (d) show that the $R_C$ decreases drastically as we scale the film thickness. In a-IGZO TFTs when a common crossing point does not exist, the x intercept of the TLM lines has been taken as rough estimate of gate voltage dependent $L_T$ [7]. But a more accurate solution for $L_T$ can be obtained by solving for equation (5) using a semi-empirical method suggested by Jung et al. [9] (see figure 3 (a)-(d)).

$$x_{\text{intercept}} = \frac{-2L_T}{\tanh\left(\frac{L_O}{L_T}\right)}$$ (5)

The values of $\mu_0$ (7.6cm²/Vs) and $V_{th0}$ (2.7V) of both Set A and B, obtained from TLM were found to be same. The value of $L_T$ obtained from graphical method along with $\mu_0$ and $V_{th0}$ were used to find the relation of $R_C$ with $L_OV$ using equation (4) (see figure 3 (e) and (f)). It is found that the overlap lengths can be reduced to less than 1µm without significantly increasing $R_C$ in devices of Set A. While for devices in set B, the overlap length can be decreased to a value as low as 100nm without affecting $R_C$ or leading to mobility degradation.

![Figure 2](image URL)

**Figure 2.** TLM analysis of devices from (a) Set A (b) Set B; $R_C$ versus gate voltage (c) Set A (d) Set B

In figure 4, equation (3) and (4) are used to find the relation between $f_T$ and $L_{OV}$ for different $T_a$ at $V_{dsat}$ of 3V and $L$ of 10 µm. It is found that when thickness is scaled below the Debye length (38 nm) of the active layer, to 30 nm, $L_{OV}$ downscaling, can penetrate into the nanometer regime (up to 100nm) to enhance $f_T$, while for thicker channel of 70 nm, $L_{OV}$ scaling below 1µm deteriorates $f_T$. This
The deteriorating effect stems from the larger contact area required for current transfer owing to larger $L_T$ (1.6µm). Thus as $L_{OV}$ is reduced below 1µm, the positive effect of decreased overlap capacitance, is counteracted by the degradation in mobility owing to increased $R_C$ and the end result is an $f_T$ which is almost reduced to half of its peak value (at $L_{OV}=L_T$), i.e., from 300kHz to 170kHz, when $L_{OV}$ decreases by a decade from 1µm to 100 nm. This result is in agreement with the experimental observation in [10] that as channel thickness is reduced from 50nm to 10nm, $R_C$ is reduced and this decreased $R_C$ leads to an increase in $\mu_{eff}$ in thinner devices, despite the popular notion that thinner channels tend to have lower mobility due to larger defects in the bulk-dielectric interface of the channel. Hence our analysis of thickness dependence of $f_T$, through the extraction of thickness dependent transfer length proves that thickness scaling can be adapted as a frequency optimization technique. Further analysis of the effect of thickness scaling on device intrinsic gain is required when we go for optimization from the angle of simultaneous gain-bandwidth enhancement of amplifiers.

**Figure 3.** Graphical method for $L_T$ estimation (a) Set A (b) Set B; $L_T$ versus gate voltage (c) Set A (d) Set B; Contact resistance variation with $L_{OV}$ for different $L_T$ (e) Set A (f) Set B.
4. Conclusion
Analysis of the effect of active layer thickness variation in a-IGZO based TFTs, on unity gain cut-off frequency was carried out. TLM along with graphical method of $L_T$ extraction were utilized to extract $R_C$ and $L_T$. At $V_{dsat}$ of 3V, the $L_T$ of devices with thickness 30nm and 70nm were found to be around 60nm and 1µm respectively. The behavior of $R_C$ under $L_{OV}$ scaling was utilized to analytically predict the cut-off frequency characteristics. It was seen that $L_{OV}$ downscaling from 10µm leads to $f_T$ enhancement in both devices of 70nm thickness and 30nm thickness upto $L_{OV}$ of 1µm, due to reduced overlap capacitance. But in devices of thickness 70nm when $L_{OV}$ is scaled lower than $L_T$ of 1µm, $f_T$ deteriorated to half its optimum value at $L_{OV} = L_T$ despite the decreased $C_{OV}$, due to mobility degradation under increasing $R_C$. On the other hand the $L_{OV}$ of 30nm thick devices could be brought down all the way to 100nm with corresponding increase in $f_T$, since dependence of $R_C$ on $L_{OV}$ is trivial as long as $L_{OV}$ is greater than $L_T$. Thus any device achieves its optimum value of $f_T$ under overlap scaling at the point $L_{OV} = L_T$. Hence $T_e$ scaling can results in $L_T$ reduction, facilitating $L_{OV}$ scaling and $f_T$ enhancement. Effect of active layer thickness on device threshold voltage and saturation current has to be further investigated to estimate the cumulative response of amplifier gain and bandwidth to TFT active layer thickness variations.

5. References
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