Latch up effect under electromagnetic pulse

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Abstract. The physics of CMOS Latch-Up (latchup) under high power microwave radiation is discussed.

1. Introduction
There has been a significant interest in the understanding the susceptibility of an electronic system to the electromagnetic interference effects due to the high power microwave (HPM) radiation. In particular, the interest is focused on the potential errors of the electronic system function introduced as a result of the electromagnetic pulse (EMP) radiation attack. A number of prior test reports have indicated that intensive EMP might cause the electronic system failures, as extensive as complete shutdown or abort of operations due to the complex interference effects of the inner circuits, and even a permanent physical hardware damage [1-4].

The electronic device level effects studies are required in order to better understand the electronic circuits effects, including the latchup, under the HPM radiation. For this review, the CMOS inverters are chosen in digital circuits device level effects studies, due to their widespread usage as an electronic component. Any typical CMOS device has an inverter in the input and output stage. The latch-up effects are the traditional inherent destruction phenomena.

2. The latch up physics
The latchup is a CMOS integrated circuit failure mechanism that is characterized by an excessive current flow between the power supply and the ground rails [6-11]. It may be a temporary transitional state that is eliminated upon removal of the exciting stimulus, a catastrophic state, requiring a shutdown of the system in order to clear the state and recover the function, or a fatal state requiring the replacement of the damaged device.

More specifically, a latch-up is the creation of a low-impedance path between the power supply rails of a MOSFET circuit, triggering a follow-up parasitic structure. The parasitic structure is usually equivalent to a thyristor (or Silicon Controlled Rectifier SCR), a PNPN structure which acts as a PNP and an NPN transistors stacked next to each other. In the CMOS technology, there are a number of the intrinsic bipolar junction transistors (Fig.1). These transistors can create problems when the combination of n-well/p-substrate results in the formation of parasitic PNPN structures. Triggering these thyristor-like devices leads to a shorting of the Vdd and GND lines, usually resulting in the destruction of the chip or a system failure. This thyristor can be triggered into latchup by the electrical conditions or by the radiation environment. Although these stimuli initiate latchup in a very different ways, the conditions for latch-up are the same.
Figure 1. a) Intrinsic BJTs in the CMOS technology b) Equivalent circuit of CMOS latch-up.

Consider the structure in Figure 1 [6]. The n-p-n-p structure is formed by the source n+ of the NMOS, the p-substrate, the n-well and the p+ source of the PMOS. A circuit equivalent is also shown in Fig.1. This simplified circuit can be used to understand how the latchup susceptibility is affected by the operating conditions and structural changes to the PNPN region. The feedback loop shown in Figure 1 is composed of cross-coupled parasitic PNP and NPN bipolar junction transistors (BJTs) and decoupling resistors R(pwell) and R(nwell). Under the normal bias conditions, the parasitic BJTs conduct very little current and regenerative feedback does not occur in this loop. The both junctions of each bipolar junction transistors are reversed biased, \( V_{BE} < 0 \) and \( V_{BC} < 0 \), so that very little current goes through the device (a thyristor). This corresponds to the "off" state of the device. However, any BJTs can be triggered first into the forward-active mode, and then in the saturation mode when both junctions of the bipolar transistors are forward biased, \( V_{BE} > 0 \) and \( V_{CB} > 0 \). During this triggering a significant current and the regenerative feedback is produced, which introduces a low impedance path between the supply voltage (\( V_{DD} \)) and ground (GND). As shown in Figure 1, the base/collector junction of both of the BJTs (i.e., the N-well/P-substrate junction) initially is reverse biased under the normal conditions. Therefore, to trigger the two BJTs into the forward active mode, it is only necessary to forward bias their emitter/base junctions, which are the source/body junctions of the MOSFETs. The n+ and p+ sources are tied directly to the power rails and are heavily doped, so their potentials are fixed. However, the bodies of the NMOS and PMOS transistors shown in Figure 1 are biased through the substrate R(pwell) and R(nwell) resistances, respectively. These resistances shunt the emitter/base junctions of the PNP and NPN transistors. Therefore, the potential drops across these resistances cause the emitter/base junctions to be forward biased. If a triggering event causes only one of these two junctions to be forward biased (0.6-0.7 V), then the corresponding BJT enters the forward active mode and forces current through the base resistance of the other BJT, and can, therefore, cause it to also enter the forward active mode, thereby establishing the latchup. Turn-on of any one of the BJT on and the SCR action will occur when both junctions are forward biased, \( V_{BE} > 0 \) and \( V_{CB} > 0 \). This corresponds to the low resistance "on" state.

It is important to remember that the two conditions are necessary for catch-up to occur:

1) both parasitic bipolar transistors must be biased into the saturation state; furthermore, since both transistors are in the saturation state, a significant amount of minority carriers is accumulated in the base region of each transistor;

2) the product of the parasitic bipolar transistor current gains must be greater than or equal to one.
3. Experimental reports

Here is presented a review of some experimental results of the HPM radiation effects and examine the
destruction and malfunction of on the CMOS structures caused by the high power microwaves. During
the HPM interference, electromagnetic pulse or radiofrequency (RF) radiation energy usually couples
into the interior electronics of a system through the following two generic paths: the front-door
coupling and the back-door coupling.[5,11]. The coupling is a kind of mechanism whereby microwave
energy is delivered to equipment under the test (EUT) through a circuit line. The front-door coupling
examples are the intensive EM signal couples into the front-end receivers in the communication and
radar systems through the antenna. The back-door coupling means EM radiation couples through the
apertures in the system shielding structure, such as ventilation et al. The interconnected wires and
power cables are also considered as the strong back-door coupling ways.

The growing attention has been focused on the threat posed by the HPMs, EMPs and RF (EM)
radiation, which can be coupled into electronic system intentionally from EM sources or
unintentionally due to the proximity to the environmental EM signals. The EM radiation results in
temporary or permanent upset, or physical hardware damage. It is necessary to note that the CMOS
digital circuits could be triggered not only by EM radiation but in other various ways such as the ESD
pulse, cosmic ray, heavy ion particles, etc.

The CMOS digital circuits, as another example of modern information devices, also can experience
the serious failures and malfunctions because of the thermal secondary breakdown caused by high
power microwaves. As these devices are mostly comprised of the integrated circuits and
microelectronics, which are sensitive to the microwaves. This is caused by the over-current when the
reverse voltage is biased to the PN junction region [3]. The computer networks, PC mainboards, and
basic logic components experiments in the TEM waveguide indicated that the system susceptibility
becomes more sensitive as the system complexity increases [2]. The test results had shown that the
field threshold depends on the type of radiation and the type of circuit component as well, and it
changes from 0.2 KV/m for UWB radiation for some computer network up to the 120 KV/m for the
EMP radiation of the CMOS logic components.

In the publication [4] the authors have investigated the malfunction of the CMOS IC inverter under
a certain critical field strength. The critical value of the field strength is dependent on many factors.
First, there are constant influencing factors such as chip fabrication technology and chip layout of
the CMOS IC. Also, there are variable factors such as switching states of the transistor. Because of these
uncertain outcomes, the critical value of field strength varies randomly. The destruction threshold
(DT) values of the studied inverters are changing from 8 kV/m up to 12.5 kV/m. The power supply
current of the CMOS IC inverter also changes under high power microwave radiation.

An internal chip analysis of destructed semiconductor was carried out using an optical microscope.
The inverter devices were separated into single inverter gates each with an input (A) and output (Y)
and two connectors for the supply voltage ($V_{CC}$) and the ground (GND). The distribution of the
destruction on the chip indicated that the primary destruction was to the inverter gates in the $V_{CC}$
and GND sides. A microscopic analysis of the inverter devices statistically shows three different levels of
damage, as indicated in Figure 2.

The damage became more severe with the increasing field strength. At a field strength of level 1
the component destruction on the chip had occurred. When field strength of level 2 the melting
processes mainly damaged the IC-lines. A field strength of level 3 exceeding 13.1 kV/m led mostly to
bond wire destruction.

4. Uncovering the different latchup mechanisms

In reality, the latchup mechanisms discussed earlier are far more complicated. The authors [5,9] have
stated that both the MOSFET sources and the drains participate in the latchup. Figures 3, 4 show the
cross-section of an N-well CMOS inverter that includes the parasitic BJTs on both the sources and the
drains [6,9].
That MOSFET drains contribute to the formation of BJTs. According to publication [7], the drains can be less susceptible to the latchup than other similarly-positioned sources, for some reasons, but as noted previously, the latchup may be triggered in a drain and then spread to a source, or that the source and drain of the same MOSFET can participate in latchup simultaneously. Figure 5 shows the triggering parasitic thyristors under the output signal. However, an integrated CMOS circuit as mentioned can be triggered in the various conditions:

a) the CMOS logic devices will latch-up when exposed to a strong enough voltage transient on either an input pin or a supply pin;
b) an electrostatic discharge can trigger the parasitic thyristor;
c) at the abnormal applications and misuse of the CMOS ICs at or beyond its rated maximum the voltage range and the presence of inductive transients;
d) the latch-up can be initiated by the dV/dt effect;
e) the high-power microwave interference can also trigger latch-ups.

Figure 5. Cross-section of an N-well CMOS inverter showing parasitic bipolar transistors on both the MOSFET sources and drains

It's very important to notice that several triggering conditions from a) to d) inclusive, may be as well produced by the last condition - by the high-power microwave interference. The signals induced at any pin of the IC by the EM radiation may be any polarity, any meaning, and any velocity. So, the EM radiation pulse may induce any triggering condition.

5. Conclusion
The high power microwave radiation on CMOS inverter (the main device of the digital circuits) causes the latchup effects. The high power microwave radiation may be the main factor of the malfunction or irreversible physical destruction of CMOS inverter. The physical mechanisms of latchup are discussed.

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