The AD and ELENA orbit, trajectory and intensity measurement systems

R. Marco-Hernández,‡, † D. Alves,⁎ M.E. Angoletta,⁎ O. Marqversen,⁎ J. Molendijk,⁎
E. Oponowicz,⁎, 1 R. Ruffieux,⁎ J. Sánchez-Quesada⁎ and L. Søby⁎

⁎Beams Department, European Organization for Nuclear Research (CERN),
385 Route de Meyrin, Meyrin, Switzerland

‡Unidad de Electrónica, Instituto de Física Corpuscular (IFIC, Universitat de València-CSIC),
Catedrático José Beltrán 2, Paterna, Spain

1School of Physics and Astronomy, University of Manchester,
Oxford Road, Manchester, U.K.

E-mail: Ricardo.Marco@ific.uv.es

ABSTRACT: This paper describes the new Antiproton Decelerator (AD) orbit measurement system and the Extra Low ENergy Antiproton ring (ELENA) orbit, trajectory and intensity measurement system. The AD machine at European Organization for Nuclear Research (CERN) is presently being used to decelerate antiprotons from 3.57 GeV/c to 100 MeV/c for matter vs anti-matter comparative studies. The ELENA machine, presently under commissioning, has been designed to provide an extra deceleration stage down to 13.7 MeV/c. The AD orbit system is based on 32 horizontal and 27 vertical electrostatic Beam Position Monitor (BPM) fitted with existing low noise front-end amplifiers while the ELENA system consists of 24 BPMs equipped with new low-noise head amplifiers. In both systems the front-end amplifiers generate a difference (delta) and a sum (sigma) signal which are sent to the digital acquisition system, placed tens of meters away from the AD or ELENA rings, where they are digitized and further processed. The beam position is calculated by dividing the difference signal by the sum signal either using directly the raw digitized data for measuring the turn-by-turn trajectory in the ELENA system or after down-mixing the signals to baseband for the orbit measurement in both machines. The digitized sigma signal will be used in the ELENA system to calculate the bunched beam intensity and the Schottky parameters with coasting beam after passing through different signal processing chain. The digital acquisition arrangement for both systems is based on the same hardware, also used in the ELENA Low Level Radio Frequency (LLRF) system, which follows the VME Switched Serial (VXS) enhancement of the Versa Module Eurocard 64x extension (VME64x) standard and includes VITA 57 standard Field Programmable Gate Array Mezzanine Card (FMC). The digital acquisition

‡Corresponding author.
Field Programmable Gate Array (FPGA) and Digital Signal Processor (DSP) firmware shares many common functionalities with the LLRF system but has been tailored for this measurement application in particular. Specific control and acquisition software has been developed for these systems. Both systems are installed in AD and ELENA. The AD orbit system currently measures the orbit in AD while the ELENA system is being used in the commissioning of the ELENA ring.

**Keywords:** Beam-line instrumentation (beam position and profile monitors; beam-intensity monitors; bunch length monitors); Data acquisition concepts; Digital electronic circuits; Digital signal processing (DSP)
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1 Introduction

The AD [1] and the ELENA [2] are synchrotron machines used to decelerate and provide low energy antiprotons to different antimatter physics experiments at CERN. About $3 \cdot 10^7$ antiprotons are injected at 3.57 GeV/c in AD and extracted at 100 MeV/c after Radio Frequency (RF) manipulation and several stages of electron cooling and stochastic cooling. The ELENA ring will further decelerate antiprotons coming from AD down to 13.7 MeV/c, corresponding to a kinetic energy of 100 keV. Figure 1 shows a schematic view of the AD and ELENA deceleration cycles. ELENA is currently being commissioned and its main motivation is to increase the antiproton production efficiency of the AD, since the number of antiprotons trapped will be increased by a factor of ten. The ELENA deceleration cycle is expected to last about 20 s and the intensity expected will range from $10^7$ to $3 \cdot 10^7$ particles. The revolution frequency will vary in AD from 1.59 MHz down to 174.5 kHz while in ELENA it will decrease from 1.056 MHz to 144 kHz. The ELENA ring radius is six times lower (4.83 m) than the AD ring radius (29 m). The beam position (closed orbit or trajectory) and bunched intensity can be measured when the beam is bunched, i.e. the RF system is on. For the electron or stochastic cooling processes the RF system will be off and the beam will be debunched. During this periods the debunched beam intensity, the momentum spread and the mean revolution frequency can be obtained by performing longitudinal Schottky measurements [3].

![Figure 1](image.jpg)

**Figure 1.** Schematic view of the AD deceleration cycle (left side) and the ELENA deceleration cycle (right side). The periods when the beam is bunched (RF is ON) are marked on both cycles.

The original AD closed orbit measurement system [4] had to be replaced since it was not able to measure the orbit during the deceleration ramps with changing revolution frequency. This is due to its multiplexed signal acquisition design, reading out signals from one BPM at a time and allowing a complete orbit measurement every 1.2 s. On the other hand, the new ELENA ring will require a system for measuring the beam orbit and, in a second stage, the trajectory. Moreover, the bunched intensity and the Schottky measurements had to be implemented in the same system so that it can be used as a secondary intensity measurement system in ELENA and, eventually, as the main system in the future [2]. Therefore, it was decided to use the same hardware and common firmware blocks for the digital acquisition in both the AD and ELENA systems.

The AD orbit measurement system consists of 32 horizontal and 27 vertical electrostatic BPMs mounted in quadrupole correction magnets around the AD ring. A low-noise head amplifier close (70 cm) to each BPM generates a difference (delta) and sum (sigma) signals from the BPM electrode signals. The head amplifiers outputs are sent differentially to the AD control room rack, which is
approximately 100 m away from the AD ring. The reception amplifiers and the digital acquisition system are installed in this rack. The digital acquisition system digitizes and processes these signals in order to obtain the closed orbit measurement.

The ELENA orbit, trajectory and intensity system is based on 20 electrostatic BPMs mounted inside the dipole and quadrupole correction magnets around the ELENA ring and 4 BPMs placed in the electron cooler. The system has also low-noise head amplifiers installed close (10 cm) to each BPM sensor. The single-ended output delta and sigma signals from each amplifier are transported over 50 m of cables to the rack in the ELENA control room and connected to the reception amplifiers and to the digital acquisition system. A single-ended transmission has been chosen in the ELENA system since a higher signal amplitude is available than in the AD system and a lower noise immunity is required. In this case, the digital acquisition system will also calculate the trajectory and intensity as well as the closed orbit.

The main components of the system in ELENA (BPMs, head amplifiers, reception amplifiers and digital acquisition system) have been designed from scratch. The BPMs and the head amplifiers of the original AD system have not been changed, they are being used in the new AD orbit measurement system until their upgrade by the end of 2017.

2 Sensors and front-end electronics

2.1 Beam position monitors

The BPMs used in AD were originally designed for the Antiproton Collector [5], which was upgraded to the AD in 1999. These BPMs consist of stainless-steel electrodes with a diameter of 84 mm mounted in a stainless steel tube with ceramic spacers. Two semi-sinusoidal electrodes are used to derive the difference signal while an annular electrode provides the sum signal. The ensemble is fitted inside the vacuum chamber in different quadrupole correction magnets. For $10^7$ particles and a bunching factor equal to one, an electrode peak voltage signal of 4.2 $\mu$V is obtained, giving a minimum BPM differential sensitivity of 100 nV/mm [4].

The ELENA BPMs are made of two diagonally-cut stainless steel electrodes attached with three glass-ceramic spacers to a stainless steel support tube, as it can be seen in figure 2. A feedthrough and a contact pin are used in each electrode to read out the electrode signal. The inner diameter of the electrodes is 66 mm, they have a thickness of 1 mm and they are separated 10 mm from the support tube. The electrodes length is 120 mm. Two of these elements are inserted in a vacuum chamber of 100 mm diameter to be able to measure the beam horizontal and vertical position. The electrode capacitance to the grounded vacuum chamber is about 17 pF while the BPM minimum differential sensitivity is 90 $\mu$V/mm for $10^7$ particles [2].

2.2 Head amplifiers

The AD head amplifier [4] consists of a transimpedance differential amplifier with $2\times6$ parallel Junction Field Effect Transistor (JFET). The delta signal is derived from this high impedance (5 M$\Omega$) input stage from the signals of the BPM semi-sinusoidal electrodes. The input equivalent voltage noise density of the differential input stage is 0.6 nV/\sqrt{Hz}. The sigma signal is produced directly from the BPM annular electrode signal by means of a JFET input voltage amplifier stage.
The head amplifier output differential delta and sigma signals are generated by means of two output buffer stages implemented with high speed voltage feedback operational amplifiers. The gain of the delta outputs (47 dB or 20 dB) can be selected by means of a digital control signal, although only the high gain setting is used in the new AD orbit measurement system. For this gain setting, the bandwidth is 10 kHz-20 MHz and the Common Mode Rejection Ratio (CMRR) is better than 66 dB below 10 MHz. The head amplifier also features an analogue calibration input signal and two Transistor Transistor Logic (TTL) digital control signals in order to simulate the maximum positive/negative beam displacement as well as a centred beam for calibration purposes.

The ELENA head amplifier [6] is based on a low-noise charge amplifier input stage connected to each BPM electrode. Figure 3 shows a picture of the ELENA head amplifier. The charge amplifier consists of a folded cascode formed with two parallel JFET transistors in combination with a pair of PNP/NPN bipolar junction transistors. An emitter follower isolates the cascode output node from the load capacity of a non-inverting current feedback amplifier. The signal gain is inversely proportional to the feedback capacitance (1 pF) while the total input capacitance (BPM electrode, input cable and JFET input capacitances) has been minimized to 50 pF to reduce the voltage noise gain of the charge amplifier. After the charge amplifiers, a sum and a difference stages have been implemented with low-noise differential amplifiers which provide a CMRR higher than 60 dB below 10 MHz. The single-ended output delta and sigma signals are buffered by two output cable drivers. The voltage input noise density of the ELENA head amplifier is 0.4 nV/√Hz. The delta output gain (46 dB) is 6 dB higher than the sigma gain (40 dB) to profit from the full output range. The gain calibration is carried out by injecting a known voltage signal through a 1 pF capacitor connected to each head amplifier input. Short (10 cm) input 75 Ω coaxial cables have been used to connect the BPM electrodes to the head amplifier inputs to minimize the input capacitance. These cables are loaded with 8 ferrites (3E5 ferroxcube material with a relative magnetic permittivity of 8000) and shielded with a metallic screen to obtain a common-mode magnetic shielding higher than 40 dB against conducted interference from the ELENA bunching cavity.
2.3 Other front-end electronics

The AD system has other front-end electronic modules including a splitter that is used to derive the analogue calibration signal required by each of the 59 head amplifiers from two common calibration signals (horizontal and vertical) which are generated by the digital acquisition system. There is also a power supply and digital calibration control module in charge of powering the head amplifiers as well as of distributing the two digital TTL calibration signals required by each head amplifier.

The ELENA system has only an additional front-end electronic module which distributes the head amplifier’s power supply levels and the two analogue calibration signals needed by each head amplifier. Since the ELENA head amplifiers do not need to include relays for the analogue calibration inputs due to their charge amplifier input stages, the two digital control calibration signals and the associated relays have been implemented in this module in contrast to the AD head amplifier, which needs to have the relays in the head amplifier board.

2.4 Reception amplifiers

The AD system reception amplifiers transform the input differential delta and sigma signals into single-ended signals which are connected to the Analogue to Digital Converter (ADC) of the digital acquisition system. These amplifiers have a bandwidth of 560 Hz-80 MHz and a midband gain of 6 dB. The ELENA system reception amplifiers are very similar to the AD system ones except for the singled-ended inputs and the mid-band gain of 12 dB with the same bandwidth.

3 Measurement principle

3.1 Orbit measurement

The closed orbit measurement system is used to monitor the beam orbit response so that corrections can be calculated and applied. In both the AD and ELENA systems the horizontal and vertical closed orbits are calculated by obtaining the beam position from each BPM around the ring as the difference signal divided the sum signal delivered by the corresponding head amplifier. The
difference between the induced charge in each electrode will give the beam center of mass, while the sum signal will be proportional to the bunched beam charge. Therefore, the position of a bunched beam can be obtained independently of the beam intensity by normalizing the difference signal by the sum signal.

The delta and sigma signals from the head amplifiers are digitized and digitally down-converted to baseband, using the AD or the ELENA revolution frequency and the RF harmonic in a local oscillator to select the first harmonic of the beam signal for calculating the position. After low pass filtering and decimating, the position for each BPM is calculated from the In-phase and Quadrature (I/Q) complex data according to:

$$
\text{Pos}(t) = k \left( \frac{1}{\Sigma_{\text{cal}}} \right) \left( \Re \left\{ \frac{I_1(t) + jQ_1(t)}{I_2(t) + jQ_2(t)} \right\} - \frac{\Delta}{\Sigma_{\text{zero}}} \right) + BPM_{\text{off}}
$$

where $k$ is the BPM sensitivity, $BPM_{\text{off}}$ is the BPM offset, $\Delta \Sigma_{\text{cal}}$ is the calibration slope and $\Delta \Sigma_{\text{zero}}$ is the calibration offset. The digital acquisition system includes a calibration procedure to obtain the calibration parameters required in equation (3.1). Three consecutive calibration acquisitions, simulating the maximum positive and negative beam displacements as well as a centred beam are performed to get three different values of the $\Delta \Sigma$ signal for each BPM. The calibration offset value ($\Delta \Sigma_{\text{zero}}$) for each BPM will be directly taken from the averaged calibration value obtained for a centred beam while the calibration slope ($\Delta \Sigma_{\text{cal}}$) for each BPM will be given by:

$$
\frac{\Delta}{\Sigma_{\text{cal}}} = \frac{\frac{\Delta}{\Sigma_{\text{plus}}} - \frac{\Delta}{\Sigma_{\text{minus}}}}{2}
$$

with $\Delta \Sigma_{\text{plus}}$ and $\Delta \Sigma_{\text{minus}}$ the averaged calibration values obtained for the maximum positive and maximum negative beam displacements respectively. The calibration procedure can be performed on user demand at the beginning of the deceleration cycle (when no beam is present). The orbit can be measured continuously during the deceleration cycle whenever the beam is bunched using this method. A position resolution of 0.1 mm, an accuracy of 0.3-0.5 mm and a time resolution of 20 ms are required for the closed orbit measurement in both AD and ELENA systems.

### 3.2 Trajectory measurement

The trajectory of the bunched beam will be measured in ELENA at injection in order to help minimize injection misalignments from the AD and correct the coherent oscillations of the beam. The bunched beam trajectory is calculated by measuring the beam position at each BPM during the first 100 turns of each deceleration cycle. This is carried out by dividing the peak values of the first 100 pulses after the beam injection of the digitized delta signal by the digitized sigma signal from each head amplifier. A position resolution of 0.1 mm and an accuracy of 0.3-0.5 mm are required for the trajectory measurement. The same BPM and calibration parameters as in the orbit measurement case can be used for the trajectory measurement.

### 3.3 Bunched intensity measurement

The bunched beam intensity will be measured in ELENA using a dedicated system based on AC beam transformers [2]. However, the ELENA orbit and trajectory system will also be used, as an
auxiliary system, to measure the intensity of the bunched beam. The bunched intensity can be measured by digitally integrating every pulse of the sum signal for each BPM. The baseline value of the digitized sigma signal is also calculated and subtracted in order to obtain the area of each sigma pulse, which is proportional to the bunched intensity. The pulse-by-pulse measurements of all BPMs are averaged and the result can be averaged over a user selectable number of beam turns. The proportionality constant required to get the intensity value will be calculated by means of a cross-calibration with the primary ELENA bunched intensity measurement system.

### 3.4 Longitudinal Schottky measurement

The longitudinal Schottky measurements [6] with coasting beam will be carried out in ELENA by means of the system based on AC beam transformers. As in the bunched intensity measurement case, the ELENA orbit and trajectory system will be also used, as an auxiliary system, to measure a given Schottky harmonic of the beam intensity power spectral density and to calculate longitudinal beam parameters like the frequency spread (Δf), the momentum spread (Δp), and the number of particles (N).

The longitudinal Schottky measurements will be performed by summing the sigma signals coming from all the head amplifiers corresponding to the 20 BPMs distributed around the ELENA ring in order to further improve the SNR by 13 dB, when compared to a single BPM (around 6 dB). The digital down-conversion of each sigma digitized signal to baseband is carried out, using the ELENA revolution frequency in the local oscillator, to select a given harmonic of the beam signal for measuring the required Schottky harmonic. A time of flight correction for each BPM is performed during the down conversion. It is proportional to the azimuthal position of each BPM in the ELENA ring and to the cable delay from each BPM to the digital acquisition system. This time of flight is calculated by the digital acquisition system for the bunched intensity measurements. Then, the down converted signal is low-pass filtered and decimated. Afterwards, the squared complex Fast Fourier Transform (FFT) of consecutive I/Q samples is calculated, they are averaged and the head amplifier noise subtracted to obtain the Schottky voltage power spectral density measurement every second. From this magnitude, the total number of beam particles and the momentum spread can be derived. A cross-calibration with the primary ELENA Schottky measurement system will be also required.

### 4 Digital acquisition system

#### 4.1 Systems layout

The digital acquisition hardware for both the AD and ELENA systems is based on a hardware family developed at CERN for the new RF systems [7]. This hardware family follows the VXS [8] enhancement of the VME64x standard [9], which supports switched serial transmission over a new highspeed P0 connector. The FMC standard [10] is used for the daughter boards.

Figure 4 shows the AD digital acquisition system layout. The AD digital acquisition system is distributed in two Versa Module Eurocard (VME)-VXS crates working independently, where the horizontal and the vertical BPM signals are grouped. The horizontal crate contains nine VXS-DSP-FMC carriers while the vertical crate contains eight. In both crates, one of these
carriers (M1) holds a FMC-Master Direct Digital Synthesizer (MDDS) and a FMC-ADC board, another carrier (M2) holds a FMC-ADC and a FMC-Slave Direct Digital Synthesizer (SDDS) and the rest of carriers (S1 to S7 or S8 depending on the crate) hold two FMC-ADCs. A CERN VME Timing Receiver module (CTRv) provides the triggers related to the AD cycle while a digital module generates the calibration digital control signals in each crate.

A common RF clock, which is a programmable higher harmonic of the AD revolution frequency \(f_{\text{REV}}\), is used for digitizing the BPM signals, at the FMC-ADC boards, and for generating the calibration analogue signals, at the FMC-SDDS boards, as well as for the associated low level signal processing at the FPGAs. A Revolution Frequency pulsed signal Tag (TAG) marks the revolution frequency and synchronizes all boards in the system. The RF clock and TAG signals are generated from the revolution frequency by a FMC-MDDS board. The revolution frequency value is calculated during the AD cycle by the DSP of the VXS-DSP-FMC carrier M1 from the value of the magnetic field of the main dipoles, whose evolution is provided by means of two pulsed signals (BUP and BDOWN).

Figure 4 shows the ELENA digital acquisition system layout. In this case, only one VME-VXS crate contains seven VXS-DSP-FMC carriers. One carrier (M1) holds a FMC-MDDS board and a FMC-ADC board, another carrier (M2) holds a FMC-ADC board and a FMC-SDDS board and the other five carriers (S1 to S5) hold two FMC-ADC boards. A CTRv provides the triggers related to the ELENA cycle while a digital module generates the calibration digital control signals in each crate, like in the AD system.

The ELENA system also works using a common RF clock whose frequency is a programmable higher harmonic of the ELENA \(f_{\text{REV}}\). However, the ELENA \(f_{\text{REV}}\) value is received from the LLRF crate trough the VXS switch B board via optical fibre instead of being calculated from the main dipoles magnetic field. Moreover, the ELENA orbit system will send the radial position during the ELENA cycle, i.e. the averaged position of the horizontal BPMs, through the same VXS switch board by means of another optical fibre to the LLRF crate.
Figure 5. Block diagram of the ELENA digital acquisition system. Men A20: master VME board. PU H: Horizontal Pick-Up. PU V: Vertical Pick-Up.

4.2 VXS Switch board

The VXS Switch board performs the interconnection of the VXS-DSP-FMC carriers via full-duplex Giga-bit serial links by means of the VXS transmission. Each VME-VXS crate contains two VXS Switch boards which are positioned at a starpoint, allowing the routing of a total of eight full-duplex links of up to 3.125 Gbit/s between any payload slot. In both AD and ELENA systems, the VXS Switch board A carries out the communication among VXS-DSP-FMC carriers by means of the VXS fabric through the VME-VXS crate, like a hand-shaking procedure to synchronize all the boards. The VXS Switch board B is used to distribute the RF clock and TAG signal. Additionally, the VXS Switch board B performs the communication with the LLRF crate in the ELENA system by means of two optical fibres.

4.3 VXS-DSP-FMC carrier

The VXS-DSP-FMC carrier accommodates a DSP (ADSP-21368) and two Xilinx Virtex 5 FPGAs, known as the Main FPGA (XC5VLX110T) and FMC FPGA (XC5VSX95T). Two dedicated full-duplex VXS channels from each VXS-DSP-FMC carrier are routed to the VXS Switch board B to distribute the RF clock and TAG signals. The other six full-duplex VXS channels, combined to form three 32 bit data paths, are used to transfer 10b8b-encoded data between VXS-DSP-FMC carriers at a raw link rate of 2 Gbit/s or 100 MSPS (32 bit). Each VXS-DSP-FMC carrier can host up to two FMC daughter boards with a high-pin count format. The VXS-DSP-FMC carrier also contains several memory banks for observation purposes. In particular, two 4Mx18 bit banks are clocked at 100 MHz and two 1Mx4x18 bit banks use the common RF clock.

4.4 Rear Transmission Modules

A Rear Transition Module (RTM) is connected to each VXS-DSP-FMC carrier through the J2/P2 connector. It carries all major secondary power supplies required by the VXS-DSP-FMC carrier. The RTM front panel provides sixteen digital inputs and eight digital outputs, directly interfaced to the Main FPGA using stacked LEMO 00 connectors. The digital inputs can be configured as
These digital inputs/outputs are used to connect the trigger signals generated by the timing module, e.g. the start and end of the AD and ELENA cycle, as well as to implement the timing and interlock wired daisy-chains required by both systems. Figure 6 shows a picture with a VXS-DSP-FMC carrier (with a FMC-MDDS and a FMC-ADC boards mounted), a VXS Switch and a RTM.

Figure 6. Picture of a VXS-DSP-FMC carrier with a FMC-MDDS and a FMC-ADC mounted (left side), a VXS Switch board (middle) and a RTM (right side).

4.5 FMC-MDDS board

The FMC-MDDS board generates the RF clock and the TAG synchronization signals. The RF clock can range from 62.5 MHz to 125 MHz at any revolution frequency harmonic from 1 to 1023. It needs a 10 MHz input reference clock to operate. Two independent channels are synchronized to the same input reference. The board includes a 32 bit direct digital synthesizer core (AD9858) with 232 MHz frequency resolution. It also features the possibility of distributing the RF clock and TAG signal either through VXS switch or a front panel eSATA connector.

4.6 FMC-SDDS board

The FMC-SDDS produces the analogue calibration signals required by the head amplifiers. This board is based on an AD9747 Digital to Analogue Converter (DAC) and features four independent channels with 16 bits resolution and a programmable gain switching of 18 dB. The output is DC coupled, with a 40 MHz analogue bandwidth and a full scale, peak output voltage of 3.6 V. The sampling rate of the DAC mezzanine can go up to 250 MSPS.

4.7 FMC-ADC board

The FMC-ADC board is used to digitize the BPM delta and sigma signals. This board has been designed specially to fulfill the low-noise requirements of the AD and ELENA orbit, trajectory and intensity measurement systems. It has four independent AC coupled channels, with programmable gain from 0 dB to 20 dB in 0.5 dB steps. The input signal range of each channel will vary from 700 mV peak to peak over 50 Ω for the 0 dB gain setting down to 300 mV for the 20 dB gain setting. Two dual, 16 bit ADCs (AD9286) digitize the input signals with a sampling rate up to 125 MSPS. The bandwidth of each channel is limited to 40 MHz. The noise voltage density level is 5.8 nV/√Hz for the 20 dB gain setting and 27 nV/√Hz for the 0 dB gain setting.
4.8 FPGA firmware

The FPGA firmware in each VXS-DSP-FMC carrier has been distributed between the Main FPGA and the FMC FPGA. Figure 7 shows the block diagram of the Main FPGA and the FMC FPGA firmware. The Main FPGA firmware implements the essential infrastructure for the system communication and data exchange. It includes the following communication channels:

- **VME64x** (address of 32 bits/data of 32 bits or data of 64 bits in multiplexed block transfers).
- **DSP** (address of 16 bits/data of 32 bits).
- **VXS full-duplex dual 32 bit link** with a transfer rate of 100 MHz (carrier-to-carrier).
- **Communication and data exchange** with the FMC FPGA (full-duplex 32 bit Gigabit links).
- **Different I2C links** to control the RTM or the VXS Switch boards.

![Figure 7. Block diagram of the firmware implemented in the Main FPGA and the FMC FPGA.](image)

The communication architecture is configured to avoid arbitration on any of the link or bus interfaces to have a simpler and more reliable system. The Main FPGA firmware also contains other useful blocks such as:

- a dual, 128 channel timing generator.
- 16 channel, 32 bit x 1024 vector function generators.
- 48 channel, 32-bit x 2048 programmable digital signal observation.
The Main FPGA firmware allows for remote updating of the FPGA and DSP software. Finally, numerous diagnostic functions are available. The Main FPGA firmware is the same for all boards and the capabilities are enabled or disabled by software depending on the desired board functionality.

The FMC FPGA firmware accommodates the custom FMC hardware control and data processing blocks. Digital signal observation is also possible by means of configurable buffers clocked with the RF clock and located in the fast memory on the VXS-DSP-FMC carrier board. These buffers will be used for the trajectory measurements in the ELENA system. The firmware code in the FMC FPGA is tailored to the specific FMC hardware through the instantiation of FMC Intellectual Property (IP) cores, i.e. each daughter board is complemented by an FPGA IP core running on the FMC FPGA. These IP cores are developed in independent version-controlled libraries through a collaborative design while the FMC FPGA common firmware is held in a separate library. The FMC FPGA firmware instantiates the corresponding IP core in each slot. The ensemble of FMC daughter board and the corresponding IP core implements the functionality of a FMC-MDDS, FMC-Digital Down-Converter (DDC) or a FMC-SDDS.

The FMC-MDDS generates the RF clock signal for all daughter boards at a high \( f_{\text{REV}} \) harmonic as well as a TAG signal, at a \( f_{\text{REV}} \), to synchronize in phase all FMC-DDC and FMC-SDDS channels in the system. The FMC-MDDS is programmed to operate at harmonic 70 and 140 in the AD orbit system and at harmonic 106 and 212 in the ELENA orbit, trajectory and intensity system to minimize the digitalization quantization noise in the FMC-ADC boards. The FMC-MDDS harmonic can only be changed in powers of two during the AD or ELENA cycle from its initial value. Table 1 shows the RF clock frequency values expected for the revolution frequency variation in the AD and ELENA cycles according to the aforementioned harmonic values.

**Table 1.** RF clock frequency value variation during the AD and ELENA cycle for the programmed FMC-MDDS harmonic values.

| AD cycle | Momentum (Gev/c) | \( f_{\text{REV}} \) (MHz) | FMC-MDDS harmonic | \( f_{\text{RFCLK}} \) (MHz) |
|----------|------------------|-----------------------------|-------------------|-----------------------------|
|          | 3.57-2           | 1.591-1.49                  | 70                | 111.3-104.3                 |
|          | 2.0-3            | 1.49-0.892                  | 70                | 104.3-62.5                  |
|          | 2.0-3            | 0.892-0.52                  | 140               | 125-70                      |
|          | 0.3-0.1          | 0.5-0.174                   | 140               | 70-24.4                     |

| ELENA cycle | Momentum (Gev/c) | \( f_{\text{REV}} \) (MHz) | FMC-MDDS harmonic | \( f_{\text{RFCLK}} \) (MHz) |
|-------------|------------------|-----------------------------|-------------------|-----------------------------|
|             | 100-35           | 1.056-0.589                 | 106               | 111.9-62.5                  |
|             | 100-35           | 0.589-0.365                 | 212               | 125-77.4                    |
|             | 35-13.7          | 0.365-0.148                 | 212               | 77.4-31.37                  |

The FMC-SDDS generates RF analogue signals of programmable \( f_{\text{REV}} \) harmonic and phase. Data acquisition and control are carried out in I/Q coordinates. The analogue calibration signals generated in both the AD and ELENA systems with the FMC-SDDS are sinusoidal signals with a
fixed frequency of 1 MHz during calibration. The analogue calibration signals peak to peak voltage is 2 V for the ELENA system and 1.6 V for the AD system. During the data acquisition in the AD and ELENA cycle, the FMC-SDDS outputs are programmed so that they follow the $f_{\text{REV}}$ harmonic of the FMC-DDC, which is very useful for diagnosis purposes.

Figure 8 shows the FMC-DDC hardware and firmware block diagram for one channel. The FMC-DDC performs digitization, down-conversion, low-pass filtering and decimation. The DDC is a homodyne receiver that converts the selected beam revolution harmonic into a baseband I/Q signal. The AD sampling clock and the local oscillator are locked to the RF clock, so the local oscillator frequency and phase is controlled to select the required beam revolution harmonic. A baseband low pass filtering and a decimation stage have been implemented by means of a first order Cascaded Integrator Comb (CIC) filter. The decimation factor and the differential delay of the CIC filter can be modified.

![FMC-ADC hardware and FMC FPGA DDC IP core firmware block diagram for one channel.](image)

Figure 8. FMC-ADC hardware and FMC FPGA DDC IP core firmware block diagram for one channel. HPF: High Pass Filter. LPF: Low Pass Filter. LNA: Low Noise Amplifier. NCO: Numerically Controlled Oscillator.

Table 2 summarizes the harmonic and CIC filter parameters for the AD and ELENA systems. The phase of the down-converted I/Q signal can be varied so as to compensate the beam time of flight and cable delay differences of each input channel. The raw digitized data coming from the ADC can be stored for the trajectory measurements. Up to 262144 samples can be stored per channel. The FMC-DDC also uses these raw digitized data in order to calculate the area between the signal and its baseline as well as the signal period and offset with regard to the TAG signal for the sigma channels.
Table 2. DDC harmonic values and CIC filter parameter values used for the AD and ELENA orbit, trajectory and intensity systems.

| AD orbit measurement                      |
|-------------------------------------------|
| CIC differential delay    | 140 |
| CIC decimation factor       | 140 |
| Harmonic (third deceleration ramp) | 3   |
| Harmonic (rest of the cycle)  | 1   |

| ELENA orbit, trajectory and bunched intensity measurement |
|----------------------------------------------------------|
| CIC differential delay    | 212 |
| CIC decimation factor       | 212 |
| Harmonic (extraction)  | 4   |
| Harmonic (rest of bunched periods) | 1 |

| ELENA Schottky measurement |
|-----------------------------|
| CIC differential delay    | 4   |
| CIC decimation factor       | 1   |
| Harmonic                   | 53  |

4.9 DSP firmware

The DSP firmware performs the core data treatment and system control, such as the acquisition and data processing from the FMC-DDCs and the on-line control of all the FMC daughter boards. It depends entirely on the functionality of the VXS-DSP-FMC carrier hosting the DSP itself, allowing full system customization.

The DSP firmware of the M1 VXS-FMC-DSP carrier controls the FMC-MDDS operation and acquires data from two BPMs via the FMC-DDC daughter board. In the AD system, this DSP firmware also calculates the revolution frequency during the AD cycle from the value of the main dipoles magnetic field while in the ELENA system the revolution frequency value is received from the LLRF crate. The hand-shaking via VXS communication to synchronize all the FMC-DDC daughter boards is also controlled by the M1 DSP firmware. The DSP firmware of the M2 VXS-FMC-DSP carrier controls the FMC-SDDS operation for the calibration and acquires data from BPMs by means of an FMC-DDC daughter board. The DSP firmware of the other VXS-FMC-DSP carriers is configured to acquire data from 4 BPMs using two FMC-DDC daughter boards per carrier.

The DSP firmware is developed in C code as an interrupt driven finite state machine. Figure 9 shows the finite state machine implemented in the DSP firmware. Two interrupts govern the finite state machine, IRQ1 and IRQ0. The interrupt IRQ1 is triggered by software and it has priority over IRQ0. The IRQ1 interrupt is used to configure the system with the parameters required to carry out a specific type of acquisition, e.g. calibration or standard acquisition, once each AD or ELENA cycle. On the other hand, the interrupt IRQ0 is generated periodically each 10 µs by the Main FPGA of the corresponding VXS-DSP-FMC carrier after the start of cycle hardware trigger has
been received from the CTRV module. This interrupt is used to perform the cycle acquisition tasks according to the DSP role (M1, M2 or S) until the end of cycle hardware trigger is received from the CTRV module. The DSP firmware will only acknowledge the IRQ0 interrupts during the AD or ELENA cycle if it has been correctly configured previously after receiving an IRQ1 interrupt, otherwise the DSP firmware will not perform any action.

![Finite state machine implemented in the DSP firmware.](image)

Figure 9. Finite state machine implemented in the DSP firmware.

Regarding the DSP data processing from the FMC-DDC daughter boards, in the AD system the DSP firmware only calculates the position according to equation (3.1) from the I/Q baseband complex data. However, in the ELENA system the DSP firmware will also perform the calculation of the bunched intensity and the Schottky voltage power spectral density with coasting beam. The bunched intensity will be calculated by the DSP from the data already processed by the specific blocks of the FMC-DDC firmware (baseline and signal areas for each pulse). The complex FFT and other data processing required for calculating the longitudinal Schottky parameters (number of particles and momentum spread) will be also carried out by the DSP firmware. Both for the bunched intensity and the longitudinal Schottky measurements, the M1 DSP will collect the data coming from the M2 and S1-S5 DSPs via the VXS bus in order to perform the averaging of the BPM sigma signals for the bunched intensity measurement and the sum of the sigma signals for the Schottky measurement. In the ELENA system, the M1 DSP will also collect the horizontal BPM positions and it will average them to calculate the radial position for the LLRF system. The trajectory data can be directly read out by the software without any need of DSP firmware processing.
5 Software

Dedicated real-time and communication software has been developed in order to: perform the post-processing of the acquired data, control calibration timing and signals and perform the real-time orchestration of control/configuration and acquisition tasks synchronous with machine timing. Being developed using a standard CERN C++ software framework (FESA: Front End Software Architecture) [12] the software also ensures a seamless integration of the measurements into the AD and ELENA operational control systems. The software runs on a MEN-A20 VME-based CPU board with 1GB of DDR2 RAM and an INTEL Core 2 Duo L7400 CPU with two cores working at a clock frequency of 1.5GHz. The operating system is based on version 6 of CERN’s tailored Scientific Linux distribution featuring a RedHat Message Real-Time Grid patched kernel. In the AD system each VME-VXS crate has its own software running independently, so that the horizontal and vertical crates work in parallel. In the ELENA system, a single VME-VXS crate is used for both the horizontal and vertical BPMs.

Hardware access for reading out the data and controlling the digital acquisition system is performed by reading and writing in specific control, data and status registers of each VXS-DSP-FMC carrier boards. These registers are accessed via the VME bus of the VME-VXS crate. After a power-cycle of reset, the AD and ELENA static system initialization is carried out by means of custom Python and BASH (Bourne-Again SHell) scripts automatically executed during boot. The software configures the hardware for normal acquisition or calibration, depending on user request, in advance prior to every beam injection. Subsequently, it waits for the end of the acquisition to readout the acquired data and make it available straightaway (to operators, physicists and instrumentation experts) just before re-configuring the hardware prior to the next beam injection.

6 Development and experimental tests

The voltage noise density level of the first version of the FMC-ADC board, described in [7], was measured in order to verify whether this level was below 30 nV/√Hz, which is the maximum level required for measuring in both the AD and ELENA systems to neglect the FMC-ADC noise contribution. The measurements were performed with a special laboratory test-bench using only an M1 VXS-DSP-FMC carrier type with a FMC-MDDS board and the FMC-ADC board under test. Custom software based on python scripts was used to acquire and process the data. The measurements were carried out with the FMC-ADC inputs left open.

Figure 10 (left side) shows the voltage noise density level measured on one channel of the first version of the FMC-ADC board. It can be seen that there are noise peaks up to 100 nV/√Hz over the full measurement bandwidth (DC to 16 MHz). These peaks were caused by the on-board DC-DC switching converters used to generate the power supply levels (±5V and 1.8V) required by the input analogue electronics to have DC-coupled inputs. It was therefore decided to redesign the FMC-ADC board to reduce the voltage noise density level well below 30 nV/√Hz. The current FMC-ADC boards used in the AD and ELENA systems have AC-coupled inputs, so that the analogue input stages can be powered with positive levels (10V and 1.8V) generated with low-noise linear regulators instead of using DC-DC switching converters. Moreover, the analogue sections of the ADCs are also powered with linear regulators. Figure 10 (right side) shows the voltage noise
density level measured on one channel of the new FMC-ADC board. It can be seen that the noise density level is below 10 nV/√Hz over the full measurement bandwidth (DC to 32 MHz).

Figure 10. On the left side, measured voltage noise density level (nV/√Hz) vs. frequency (kHz) for one channel of the first version of the FMC-ADC board (DC-coupled inputs). On the right side, measured voltage noise density level (nV/√Hz) vs. frequency (MHz) for one channel of the new FMC-ADC board (AC-coupled inputs).

A prototype version of the system with only the M1 VXS-DSP-FMC carrier without VXS communication was tested in December of 2014 in AD as proof of concept of the system, with data from two BPMs acquired successfully. A second prototype version of the system was tested in AD with real beam since August of 2015. It consisted of a VME-VXS crate holding the M1 VXS-DSP-FMC carrier, the M2 VXS-DSP-FMC carrier, another six (S1-S6) slave VXS-DSP-FMC carriers, a CTRV timing module as well as a digital module to generate the calibration digital control signals. The aim was to acquire data from all vertical BPMs and to test all the features of the final system (VXS communication, calibration procedure, position resolution, etc.) in real conditions. For this test, the noisier DC-coupled version of the FMC-DDC boards were used until the new AC-coupled FMC-DDC boards were available.

Figure 11 (left side) shows the position measurement for a vertical BPM during the first flat top and deceleration ramp in the AD cycle (3.57-2 GeV/c). It can be seen that a position signal is obtained from 35 s onwards, corresponding to the time when the beam is bunched. A resolution of 0.068 mm was obtained. The resolution was improved to 0.037 mm in subsequent measurements carried out with the new AC-coupled FMC-DDC boards. Figure 11 (right side) shows the position measurement for the vertical plane of all BPMs during the first flat top (AD cycle time 35.55 s). The green line corresponds to the original AD orbit system while the blue line corresponds to the prototype version of the AD new orbit system. The minimal differences between both systems are due to the fact that the original AD orbit system measurement is performed in a multiplexed fashion during 1.2 s, therefore the AD cycle measurement time for the vertical BPMs does not correspond exactly to 35.5 s.

The acquisition and control software used in this prototype was based on custom Python scripts. These scripts mimicked the desired functionality for the final software and were also used for the software development.
Figure 11. On the left side, measured positon (mm) for a vertical BPM vs. AD cycle time (ms) during the AD cycle first flat top and deceleration ramp. On the right side, position measurement (mm) for the vertical plane of all BPMs during the AD cycle first flat top (35500 ms). The green line corresponds to the original AD orbit system and the blue line to the prototype version of the AD new orbit system.

7 Installation and commissioning in AD and ELENA. Status and future plans

The production of the digital acquisition hardware was launched for the AD and ELENA systems as well as for the future Low Energy Ion Ring (LEIR) orbit and Schottky measurement systems. Table 3 shows the number of units produced and tested of each type of board as well as the number of units which passed the quality tests and are operational.

| Board type    | Units produced | Units operational | Failure rate (%) |
|---------------|----------------|-------------------|------------------|
| VXS-DSP-FMC   | 48             | 39                | 18.75            |
| RTM           | 33             | 32                | 3                |
| VXS Switch    | 13             | 13                | 0                |
| FMC-MDDS      | 8              | 6.5               | 18.75            |
| FMC-SDDS      | 8              | 8                 | 0                |
| FMC-ADC       | 84             | 84                | 0                |

The quality tests consisted basically in verifying the critical aspects for each board to work correctly (smoke tests with thermal camera, power supply levels verification, etc.) as well as its basic functionality. A specific test protocol was defined for each board type. The functionality tests for each board were automated by means of Python software scripts. They ranged from testing the FPGA Gigabit links of the VXS-DSP-FMC carriers and the VXS Switch boards, or the digital inputs/outputs of the RTMs, to verify the passband flatness, gain and harmonic distortion of each FMC-ADC channel. For the VXS-DSP-FMC carriers and VXS switch boards additional Joint Test Action Group (JTAG) boundary scan tests were performed. In these tests, the connectivity of the devices' pins connected to the JTAG chain (FPGAs, DSP, etc.) was verified as well as the FMC interfaces using a special FPGA FMC test board.
A batch of 24 BPMs and 30 head amplifiers have been produced for the ELENA system. A test protocol was carried out to check the performance and verify the quality of each amplifier. The power consumption, the bias point, the gain and the output noise were verified for each unit. The BPMs linearity was checked and the electrode capacitance to ground was measured.

The new AD orbit measurement system was installed in October of 2016. It worked in parallel with the original AD orbit system during two months in order to compare their measurements and validate the new orbit measurement system. Figure 12 shows the AD horizontal orbit (top side) and the vertical orbit (bottom side) measured with the new system (green dots) and the original system (pink dots) corresponding to an AD cycle time of 87800 ms (end of third decelerating ramp and beginning of last flat top). It can be seen that the measurements of both systems agree well. The new AD orbit measurement system was validated and original AD orbit system was dismantled in January of 2017 (with the exception of the BPMs and the head amplifiers which will be upgraded at the end of 2017).

The ELENA ring is being commissioned since November of 2016. The ELENA orbit, trajectory and intensity system was installed in October of 2016. The BPMs and amplifiers of the system were used to acquire the first beam signals with the beam not bunched. The system will be able to measure as soon as the LLRF system becomes operational and the beam could be bunched. In a first stage, only the orbit is going to be measured with the ELENA system. Currently, the turn-by-turn position (trajectory) can be measured in half of the BPMs, although a modification in the FMC FPGA DDC IP core is ongoing in order to measure the trajectory for all the BPMs. The current DSP version deployed in the ELENA system VXS-DSP-FMC carriers only includes the orbit measurement. The bunched intensity and Schottky measurements will be included throughout the ELENA ring commissioning (during 2017) since these measurements need to be cross-calibrated with the primary ELENA bunched intensity and Schottky measurement systems.

Once the trajectory measurement for all the channels has been implemented in the ELENA system, it will be also included as a new feature in the AD orbit system. Finally, a new FPGA firmware version is being developed in order to operate with a fixed frequency RF clock (122 MHz) and overcome the low sampling frequency issue in the ADC with low revolution frequency values.
in the AD and ELENA cycles as well as the need of FMC-MDDS harmonic change during the AD and ELENA cycle. This new FPGA firmware version will affect both the Main FPGA firmware and the FMC FPGA firmware (common firmware and IP cores for FMC-MDDS, FMC-SDDS and FMC-DDC). The new firmware will be used both in the ELENA LLRF system and the AD and ELENA orbit, trajectory and intensity systems.

8 Summary

The new AD and ELENA orbit, trajectory and intensity measurement systems have been designed and implemented. The BPMs and the front-end electronics used in both systems have been described. The measurement principles used in both systems have been discussed. The digital acquisition system layout has been presented with special emphasis. The hardware boards used in both systems as well as the FPGA firmware and DSP firmware developed for the AD and ELENA systems have been depicted. The main characteristics of the control and acquisition software used in both system have been explained. The most important development milestones and experimental tests carried out have been also pointed. The required front-end electronics and digital acquisition hardware were produced and tested. The AD orbit system has been installed and it is working successfully. The ELENA orbit, trajectory and intensity measurement system has been also installed. The front-end electronics are being used for the ELENA ring commissioning. The orbit will be measured when the RF system becomes operative and the beam will be bunched. In a second ELENA ring commissioning stage, the trajectory and intensity measurements will be able to be performed. Finally, a FPGA firmware update is being developed to improve the operation of the AD and ELENA systems.

A Glossary

**AD** Antiproton Decelerator. 0–10, 12–20

**ADC** Analogue to Digital Converter. 5, 8, 10, 12, 13, 16–19

**BPM** Beam Position Monitor. 0, 2–8, 10, 14–20

**CERN** European Organization for Nuclear Research. 0, 2, 7, 16

**CIC** Cascaded Integrator Comb. 13, 14

**CMRR** Common Mode Rejection Ratio. 4

**CTRV** CERN VME Timing Receiver module. 8, 15, 17

**DDC** Digital Down-Converter. 12–15, 17, 19, 20

**DSP** Digital Signal Processor. 1, 7–12, 14–20

**ELENA** Extra Low ENergy Antiproton ring. 0–10, 12–16, 18–20

**FFT** Fast Fourier Transform. 7, 15
The text is a list of abbreviations and their definitions, followed by a references section. The abbreviations include:

- **FMC** Field Programmable Gate Array Mezzanine Card. (0, 7–20)
- **FPGA** Field Programmable Gate Array. (1, 9, 11–14, 18–20)
- **I/Q** In-phase and Quadrature. (6, 7, 12, 13, 15)
- **IP** Intellectual Property. (12, 13, 19, 20)
- **JFET** Junction Field Effect Transistor. (3, 4)
- **JTAG** Joint Test Action Group. (18)
- **LEIR** Low Energy Ion Ring. (18)
- **LLRF** Low Level Radio Frequency. (0, 1, 8, 9, 14, 15, 19, 20)
- **MDDS** Master Direct Digital Synthesizer. (8, 10, 12, 14, 16, 20)
- **RF** Radio Frequency. (2, 6–10, 12, 13, 19, 20)
- **RTM** Rear Transition Module. (9–11, 18)
- **SDDS** Slave Direct Digital Synthesizer. (8, 10, 12–14, 20)
- **TAG** Revolution Frequency pulsed signal Tag. (8–10, 12, 13)
- **TTL** Transistor Transistor Logic. (4, 5, 10)
- **VME** Versa Module Eurocard. (7–9, 16, 17)
- **VME64x** Versa Module Eurocard 64x extension. (0, 7, 11)
- **VXS** VME Switched Serial. (0, 7–12, 14–19)

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