MSP: An FPGA-Specific Mixed-Scheme, Multi-Precision Deep Neural Network Quantization Framework

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Abstract

With the tremendous success of deep learning, there exists imminent need to deploy deep learning models onto edge devices. To tackle the limited computing and storage resources in edge devices, model compression techniques have been widely used to trim deep neural network (DNN) models for on-device inference execution. This paper targets the commonly used FPGA (field programmable gate array) devices as the hardware platforms for DNN edge computing. We focus on the DNN quantization as the main model compression technique, since DNN quantization has been of great importance for the implementations of DNN models on the hardware platforms. The novelty of this work comes in twofold: (i) We propose a mixed-scheme DNN quantization method that incorporates both the linear and non-linear number systems for quantization, with the aim to boost the utilization of the heterogeneous computing resources, i.e., LUTs (look up tables) and DSPs (digital signal processors) on an FPGA. Note that all the existing (single-scheme) quantization methods can only utilize one type of resources (either LUTs or DSPs for the MAC (multiply-accumulate) operations in deep learning computations. (ii) We use a quantization method that supports multiple precisions along the intra-layer dimension, while the existing quantization methods apply multi-precision quantization along the inter-layer dimension. The intra-layer multi-precision method can uniform the computation overhead and at the same time preserve the model accuracy as the inter-layer approach.

Our proposed mixed-scheme, multi-precision (MSP) DNN quantization framework achieve 70.47% Top1 accuracy in ResNet-18 on the ImageNet dataset. We also validate the proposed MSP framework on two FPGA devices i.e., Xilinx XC7Z020 and XC7Z045. We achieve 3.53x speedup in end-to-end inference time on the ImageNet, comparing with the fixed-point quantization method.

1 Introduction

Deep neural networks (DNNs) have been employed in various of tasks with outstanding performance, such as convolutional neural networks (CNNs) for computer vision (LeCun, Bengio, and Hinton 2015), recurrent neural networks (RNNs) for natural language processing (NLP) (Bishop 2006; Goodfellow, Bengio, and Courville 2016). However, due to the large model size and extremely intensive computation, it is still challenging to deploy these DNN models on edge devices.

To support broad applications of deep learning, such as autonomous vehicles, wireless access points, robotic vision and control, smart health devices, etc., there are two aspects to enable DNNs under these resource constrained circumstances. First is to utilize specialized hardware platform for the inference of DNNs. Extensive research efforts have been dedicated to various kind of edge-computing platforms such as ASICS (Application Specific Integrated Circuits) (Mao et al. 2018; Hegde et al. 2018; Han et al. 2016a), FPGAs (Sharma et al. 2016; Li et al. 2018; Zhang et al. 2015; Shi et al. 2019), and embedded CPUs/GPUs (Leng et al. 2019; Niu et al. 2020; Han et al. 2016b).

The other is DNN model compression which explores the potential of algorithm and hardware co-design and finds better trade-offs between task performance (accuracy, etc.) and hardware efficiency (latency, power consumption, etc.). There are in general two techniques for model compression: DNN pruning (Lym et al. 2019; Shi et al. 2020b); Han et al. 2015; Liu et al. 2019) and quantization (Courbariaux, Bengio, and David 2015). These techniques can make models work with significantly smaller model sizes and fewer operations. Therefore, these compression techniques become a must-do step for deployment on edge devices. Here we only focus on the quantization approach, which becomes imperative to hardware acceleration especially on the FPGA and ASIC platforms. By representing weights with fewer bits, weight quantization can directly reduce model size and accelerate inference speed.

In this paper, we propose the novel Mixed-Scheme, Multi-Precision (MSP) Quantization Framework specifically for the FPGA devices, which achieves unprecedented hardware efficiency without sacrificing accuracy at low bit width (e.g., 4-bit). Our contributions are as follows:

- We develop a hardware-friendly sum-of-power-of-two (SPOT) quantization scheme, which can mitigate the accuracy degradation of the vanilla power-of-two (PoT) scheme while can still take advantage of bit shifting operation to accelerate computation.

*Equal contribution.
• We propose a novel Mixed Scheme Quantization (MS) to fully utilize the heterogeneous resources of FPGAs. To be more specific, based on available DSP and LUT modules in different FPGAs, we can finalize the corresponding ratio of SPoT and fixed-point quantization scheme, so that both module can be fully exploited.

• Rather than using a different precision in the first and last layers, or employing inter-layer multi-precision for extreme compression rate, we propose an Intra-Layer Flexibility, which can be applied to all layers in a DNN model, achieving lossless accuracy performance without damaging hardware efficiency.

2 Related Work and Motivation
In this section, we summarize quantization schemes and compare them in terms of their hardware deployment implications and accuracy degradation. Further, we also briefly discuss recent works on neural network quantization. Finally, we describe the motivation of our FPGA-specific MSP quantization.

2.1 Quantization Schemes
Based on whether the distances between the quantization levels are equal or not, there are linear and non-linear quantization schemes. In terms of bit width, we can also classify neural network quantization into categories of single-precision or multi-precision.

Linear Number System Linear quantization schemes contain binary, ternary, and fixed-point number systems. Binary or ternary uses extremely low-bit weight representation for DNNs, which can achieve very high inference computing efficiency by eliminating multiplications, but sacrifice accuracy. Representative binary quantization methods include Binaryconnect [Courbariaux, Bengio, and David 2015], Binaryized Neural Network (BNN) [Courbariaux et al. 2016], XNOR-net [Rastegari et al. 2016], and ABC-Net [Lin, Zhao, and Pan 2017]. Ternary quantization schemes are implemented in TWN [Li, Zhang, and Liu 2016], TTQ [Zhu et al. 2017], and [He and Fan 2019].

On the other hand, fixed-point quantization uses more bits of weight representation to preserve accuracy. For example, compared with the floating-point (e.g. 32 bits), fixed-point quantization can use 4-bit to represent the weights with negligible accuracy loss. Fixed-point quantization scheme has been implemented with different methods/algorithms. DoReFa-Net [Zhou et al. 2016] first explored it by introducing hyperbolic tangent transformation to weights and activations, with scaling factors to minimize quantization error. PACT [Choi et al. 2018] improved this method by adding a parameterized clipping threshold to activations. DSQ [Gong et al. 2019b] developed an evolving training method to gradually approximate STE. QIL [Jung et al. 2019] parameterized the quantization interval and trained it with task loss, avoiding access to the original training data. µL2Q [Cheng et al. 2019] introduced data distribution loss during training to minimize quantization error. LSQ [Esser et al. 2019] proposed a differentiable method to learn the quantizer for each layer jointly with parameters.

Fixed-point quantization still needs multiplication operations, which execute on DSPs of FPGA. However, the DSP resources are limited, e.g., ranging from 240 to 1,540 DSP slices in Xilinx Kintex-7 series, which becomes the bottleneck of merely employing fixed point quantization.

Non-Linear Number System Miyashita et al. [Miyashita, Lee, and Murmann 2016] first replaced fixed-point quantizer with logarithmic representation to exploit bit shift operations and accelerate inference. We refer this kind of non-linear number system as power-of-two (PoT) quantization. In this way, the multiplication of input (a fixed-point number) and weight (a PoT number) can be replaced by bit shift operation and can be executed as shown below,

\[ 2^b \times a = \begin{cases} 
  a << b, & b > 0 \\
  a, & b = 0 \\
  a >> b, & b < 0 
\end{cases} \] (1)

where \(2^b\) is the quantized weight, \(a\) is the input value.

Followed the PoT scheme, INQ [Zhou et al. 2017] split weights into groups and iteratively quantize the model to low bit-width. Leng et al. [Leng et al. 2018] employed ADMM training technique to increase the accuracy of extremely low-bit-width DNNs. Li et al. [Li, Dong, and Wang 2020] introduced a reparameterization of clipping function to get better-defined gradients, and employed weight normalization to stabilize training.

Even though PoT can reduce the computation by replacing the multiplication to bit shift operation, the distance between the quantization levels grows up exponentially, causing PoT suffered from significant accuracy degradation. Li, Dong, and Wang [2020] proposed additive power-of-two (APoT) to reduce the accuracy degradation of power-of-Two. However, APoT uses more bit shift and addition while increasing the bit width for the weight quantization. For example, APoT uses 3 bit-shift and 2 addition for 6-bit weight representation, which only pursues the less accuracy degradation but does not consider the hardware availability ratio. Besides, APoT alternatively assigns the value of Power-of-two to each part (e.g. in 5-bit quantization, APoT assigns \(\{0, 2^{-1}, 2^{-3}, 2^{-5}\}\) to the first part and \(\{0, 1, 2^{-2}, 2^{-4}\}\) to the second part), which is hard to deploy the quantized DNN models for hardware implementations.

Bit Width Selection The majority of previous works [Zhou et al. 2016; Choi et al. 2018; Zhang et al. 2018] etc. assign same bit width to all layers, which we refer as single-precision quantization. The other track [Dong et al. 2019; Shen et al. 2020] optimizes bit width for each individual layer so that maximum compression rate can be achieved with minimum degradation of accuracy. We refer this methodology as multi-precision quantization. It is to solve Hessian matrix to determine bit width for each layer. The general idea is to assign more bits to layers that are sensitive to quantization error. In fact, very few works are strictly single-precision quantization, because the first and last layers affect much more on accuracy. Therefore, current researches follow [Han et al. 2015] to quantize first and last
mixed-scheme (MS) quantization can be applied to both DSPs and LUTs, we propose to utilize a combination of hardware (FPGA) resources, which is coming from mixed-scheme, multi-precision (MSP) quantization to quantize the first and the last layers while preserving the accuracy. Based on the optimal ratio given from hardware (FPGA) resources, we propose an improved version of PoT quantization, called mixed-scheme (MS) quantization, applying the two quantization methods respectively to different filters within a DNN layer. MS allows another dimension to choose appropriate scheme according to weight distribution, which is beneficial to accuracy.

We also observe that existing works do not quantize or use no less than 8 bits for fixed point weight representation for the first and last layers (Courbariaux, Bengio, and David 2015; He and Fan 2019; Ren et al. 2019), and most multi-precision works (Dong et al. 2019; Shen et al. 2020) also employ such inter-layer flexibility. The deployment of these models on FPGA for inference needs different configurations for different layers. So we explore a novel multi-precision (MP) quantization to quantize the first and the last layer while preserving the accuracy. Based on the optimal ratio given from hardware (FPGA) resources, we propose the multi-precision (MSP) quantization enjoying two benefits, i.e., (1) better utilization of the FPGA resources of FPGA, which is coming from mixed-scheme, and (2) zero accuracy degradation, which is due to multi-precision.

3 Quantization Formulation

In this section, we first formulate typical fixed point and power-of-two quantization schemes. Then we improve the vanilla PoT with a summation method, namely sum-of-power-of-two (SPoT) quantization to better fit weight distribution so as to preserve accuracy with minor computation overhead introduced. Lastly we give the algorithm to perform quantization aware training.

3.1 Fixed Point Quantization

As mentioned in Section 2, the most intuitive way to perform quantization is to map the full precision parameters to low bit width uniform representations. The weight representation can be defined as follows:

\[ Q^{FP}(m, \alpha) = \pm \alpha \times \{0, \frac{1}{2^{m-1} - 1}, \frac{2}{2^{m-1} - 1}, \ldots, 1\}. \]

where \( Q^{FP} \) refers to quantized numbers, \( m \) is the bit width and \( \alpha \) is a scaling factor. And the mapping function from a 32-bit floating-point weight \( w \) into the quantized weight \( \hat{w} \) by \( m \)-bit fixed-point representation is as follows:

\[ \hat{w} = \prod_{Q^{FP}(m, \alpha)} w \]

\[ = \alpha \cdot h^{-1}(\frac{1}{2^m - 1} \cdot \text{round}(2^m - 1 \cdot h([w, \alpha]))) , \]

where \( \prod_{Q^{FP}(m, \alpha)}() \) denotes the quantizer function to project onto \( Q^{FP}(m, \alpha) \); the function \( h() \) transforms a value within \([-1, +1]\) into the range of \([0, 1] \), for example we can use \( h() = \tanh() / 2 + 0.5 \); and \([w, \alpha] \) clips \( w \) according to

\[ [w, \alpha] = \begin{cases} -1, & w < -\alpha \\ [w/\alpha], & -\alpha \leq w \leq \alpha \\ 1, & w > \alpha \end{cases} \]

3.2 Power of Two (PoT) Quantization

In order to replace multiplications with bit shifting operations, we need to make weights in the form of powers-of-two. The quantized weight values by PoT scheme with an \( m \)-bit weight representation are as follows:

\[ Q^{P2}(m, \alpha) = \pm \alpha \times \{0, \frac{1}{2^{m-1-2}}, \frac{1}{2^{m-1-3}}, \ldots, 1\} \]

The mapping from continuous parameters to PoT number system is defined by

\[ \hat{w} = \prod_{Q^{P2}(m, \alpha)} w \]

\[ = \begin{cases} \alpha \cdot h^{-1}(2^{\text{round}(\log_2 h')}), & h' > 2^{-2^m + 1} \\ 0, & h' \leq 2^{-2^m + 1} \end{cases} \]

\[ h' = h([w, \alpha]) \]

from which we can infer another disadvantage of pure PoT quantization. Increasing bit width merely increases resolution around mean area, but has no effect at the tail, as displayed in Figure [1].

3.3 Sum of Power of Two (SPoT) Quantization

Sum-of-power-of-two (SPoT) can be considered as an improved version of power-of-two (PoT) quantization, which can also replace the multiplications with bit-shift operations. The quantization levels are defined as follows:

\[ Q^{SPoT}(m, \alpha) = Q_1^{P2}(m_1, \alpha) + Q_2^{P2}(m_2, \alpha) \]

Where \( m_1 \) has a larger range and \( m_2 \) has a smaller range \((m_1 \geq m_2) \). Then all quantization levels set are a combination of lower bit-width PoTs. In Figure [1], we take the 6-bit SPoT quantization as an example. First, SPoT needs 1 bit for...
the sign, then we split the rest 5 bit to the smaller range \( m_1 \) (3bit) and the larger range \( m_2 \) (2bit). In Figure 1, number 0.625 can be represented by \( 2^{-3} + 2^{-1} \), then \( 2^{-3} \) can be decoded in “011” in smaller range \( m_1 \) and \( 2^{-1} \) can be decoded in “10” in larger range \( m_2 \). Therefore, when multiplying an input value by weight “101101”, we shift the input right 3 bit and 1 bit, respectively, and sum the two results up.

Figure 1 also shows a notable shortcoming of PoT. PoT has very high precision around the mean, but the tail ends present very low precision. It causes a mismatch with the weight value distribution. Thus, PoT suffers from non-negligible accuracy degradation. On the other hand, the proposed SPoT has relatively even quantization intervals, which is close to that of fixed-point quantization levels. Therefore, the SPoT can achieve similar accuracy performance as the fixed-point quantization scheme.

### 3.4 Quantization-Aware Training Algorithm

Quantization is a projection from the continuous value to discrete number system, which makes the gradients flowing from loss function zero everywhere during backpropagation. There are two approaches to address this issue. One is employing a Straight Through Estimator (STE) \(^{(Bengio, \text{ Leonard, and Courville} 2013; Yin et al. 2018)}\) to set the gradient to constant value 1 as

**Forward**: \( y = \text{round}(x) \)

**Backward**: \( \frac{\partial y}{\partial x} = 1_{x \in R} \)

(8)

The other is the Alternating Direction Method of Multipliers (ADMM) \(^{(Leng et al. 2018)}\) to iteratively solve the parameters with a target quantization scheme as the optimization constraint. These two methods are equivalent in terms of convergence, but ADMM algorithm shows more flexibility as gradients can not be defined appropriately by STE in some specific tasks. In this paper, we perform ADMM for weight and STE for activation quantization. We will not include detailed derivations of ADMM due to space, please refer to the mentioned previous work.

### 4 MSP Framework

#### 4.1 Mixed-Scheme (MS) Quantization

Relying on SPoT quantization only or fixed point quantization only will not achieve the optimal performance on FPGA devices. Thus, we propose the mixed-scheme quantization (MS). In each layer of a DNN, we split parameters into two parts, one uses SPoT while the other is quantized under fixed point quantization scheme. Besides, on the algorithm level, in each layer, the weight matrix can be obtained by transforming the weight tensor into a 2D GEMM matrix. The distribution of weights in different rows is rather random. For rows that have smaller variances (have more Gaussian-like weight distributions), SPoT scheme is a better fit; while for rows with larger variances (more uniform-like distribution), using fixed-point scheme can avoid high quantization error. In our work, the optimal ratio of SPoT to fixed-point is determined by available resources on FPGA devices, instead of
serving for accuracy. Usually, the utilization of DSPs needs to be maintained at 100% to take full advantage of the DSP resource. Incorporating with DSP, we would like to assign appropriate workload on LUTs and make them finish simultaneously, and therefore enhance the throughput.

### 4.2 Multi-Precision (MP) Quantization

We further propose a novel mixed-precision quantization scheme (MP) to achieve lossless performance compared with the original full precision DNN models, as illustrated in Figure 2. In image classification task, first and last layers are extremely sensitive. Thus, most of the existing works do not quantize or use no less than 8-bit fixed-point weight representation for the first and last layers to maintain accuracy (Courbariaux, Bengio, and David 2015; He and Fan 2019; Ren et al. 2019). Recent work (Zhu et al. 2019; Gong et al. 2019) has investigated FPGA-based inference engine supporting different quantization bits adaptively. However, such online reconfiguration ability inside each PE incurs non-negligible hardware overhead. Besides, such inter-layer flexibility in quantization bits brings about only minor accuracy improvement, even if sophisticated search method for per-layer quantization bits is employed (Wang et al. 2019; Lou et al. 2019).

To overcome this challenge, we propose *Multi-precision quantization (MP)* for our quantization scheme. In each layer, we preserve the 5% weights to use the 8-bit weight representation. Based on the average distance between the weight and the nearest 4-bit weight quantization level in each row (i.e. average quantization error) of the weight matrix. We determine the rows with highest 5% average quantization error to be 8-bit, while still using the 4-bit weight representation for the rest. The overall DNN accuracy can be maintained as long as 5% of weights in each layer are quantized using 8 bits. Even if the rest of the weights (in all layers) are quantized using very few bits. This is because in *intra-layer flexibility*, the weights quantized using 8 bits can be trained to mitigate the imprecision caused by those weights quantized using fewer bits. This mitigation happens in every layer. On the other hand, in the prior inter-layer flexibility, the majority of layers will be quantized with fewer bits. The resultant imprecision cannot be mitigated within a layer and will be accumulated across layers. It is difficult to recover the accumulated imprecision by limited layers quantized with more bits.

Besides algorithm-level advantages, the proposed intra-layer flexibility also exhibits an advantage at the FPGA hardware level. Recall that the same quantization scheme (e.g., 4-bit for 95% of weights and 8-bit for the rest of 5%) is applied to all layers of a DNN. At FPGA configuration time for a specific DNN inference task, one could allocate a portion of PEs for the low-bit portion of computation and the rest of PEs for the 8-bit portion, and this works for every layer. As for traditional inter-layer multi-precision scheme, it’s almost impossible to perform online reconfiguration, that is, the PEs assigned to execute 8-bit first/last layers is vacant while processing the middle layers.

Figure 2: Illustration of a DNN integrating the proposed intra-layer flexibility with the FPGA-specific quantization scheme and comparison with the other state-of-the-art quantization works. \(k\) refers to the bit width of each layer. Generally, the middle layers share same bit width (e.g. \(k_2 = k_3 = \ldots = k_{n-1}\)), but for multi-precision works, different bit widths are employed in the middle layers (e.g. \(k_1 \neq k_3\)).

### 4.3 Mixed-Scheme, Multi-Precision (MSP) Quantization Framework

To fully utilize all on-chip resources, we propose Mixed Scheme, Multi-Precision Quantization (MSP) framework as the combination of MS and MP. Based on the optimal ratio of SPoT/Fixed-point given by the hardware (FPGA) resource (e.g. 2:1 for XC7Z045). We further give the optimal ratio of SPoT/Fixed-point/8bit is 65:30:5, which can (1) better utilize the resource of the FPGA, (2) have the highest throughput (GOPS)/lowest latency, and (3) achieve lossless accuracy performance compared with the original full precision model. The detailed implementation is shown in Algorithm 1.

### 5 Evaluation

#### 5.1 Experiment Setup

We evaluate our novel MSP on image classification tasks with convolutional neural networks (CNNs). We use no extra data augmentations other than those already employed for training the 32-bit floating-point baseline models. Our quantization training algorithm uses step or cosine learning rate decay and \(\ell_2\) regularization, following training algorithms of the baseline models. Our experiments are implemented with server-grade machines running Ubuntu 18.04, CUDA 10.2 and PyTorch 1.5. Our models are trained on NVIDIA TITAN RTX GPUs and GeForce RTX 2080Ti GPUs. We evaluate with the deep residual net (ResNet-18) (He et al. 2016), which generalizes well for varieties of tasks, as well as the lightweight MobileNet-v2 model (Sandler et al. 2018). We test on CIFAR-10, CIFAR-100 (Krizhevsky 2009), and ImageNet ILSVRC-2012 (Krizhevsky, Sutskever, and Hinton 2012) datasets. DNN models for CIFAR-10 and CIFAR-100 datasets are trained from scratch, and quantized for 150 epochs. For ImageNet dataset, pre-trained models in 32-bit floating-point are used, and quantized for 90 epochs. The initial learning rates are \(8e - 3\) for CIFAR-10, \(4e - 3\) for CIFAR-100, \(1e - 2\) for ImageNet.
Quantization Scheme | Bit width (Wght./Actv.) | ResNet-18 Accuracy (%) Top1 (N/Y) Top5 (N/Y) | MobileNet-v2 Accuracy (%) Top1 (N/Y) Top5 (N/Y)
---|---|---|---|
CIFAR-10
Baseline | 32/32 | 93.62 | - | 92.51 |
PoT | 4/4 | 92.97 / 92.14 | - | 91.34 / 90.92 |
Fixed | 4/4 | 93.43 / 92.97 | - | 92.34 / 91.76 |
SPoT | 4/4 | 93.47 / 92.94 | - | 92.72 / 91.83 |
MS | 4/4 | 93.53 / 92.98 | - | 92.57 / 91.99 |
MP | 4/4 | - / 93.63 | - | - / 92.54 |
MSP | 4/4 | - / 93.72 | - | - / 92.58 |
CIFAR-100
Baseline | 32/32 | 74.49 | 92.70 | 71.48 | 91.98 |
PoT | 4/4 | 73.88 / 72.97 | 92.14 / 91.65 | 68.68 / 67.11 | 90.06 / 89.21 |
Fixed | 4/4 | 74.37 / 73.88 | 92.31 / 91.72 | 71.16 / 70.22 | 91.63 / 90.88 |
SPoT | 4/4 | 74.33 / 73.97 | 92.49 / 92.03 | 71.13 / 70.21 | 91.69 / 90.85 |
MS | 4/4 | 74.58 / 74.03 | 92.51 / 92.05 | 71.21 / 70.25 | 91.74 / 90.92 |
MP | 4/4 | - / 74.54 | - / 92.61 | - / 71.49 | - / 91.82 |
MSP | 4/4 | - / 74.61 | - / 92.69 | - / 71.51 | - / 91.97 |
ImageNet
Baseline | 32/32 | 69.76 | 89.08 | 71.88 | 90.29 |
PoT | 4/4 | 68.20 / 67.11 | 87.14 / 85.93 | 69.93 / 67.88 | 88.63 / 86.83 |
Fixed | 4/4 | 69.72 / 68.66 | 88.67 / 87.54 | 71.26 / 69.23 | 90.18 / 88.03 |
SPoT | 4/4 | 69.74 / 68.48 | 88.71 / 87.92 | 71.32 / 69.76 | 90.17 / 88.42 |
MS | 4/4 | 70.11 / 69.22 | 89.41 / 88.33 | 71.26 / 69.31 | 90.04 / 88.11 |
MP | 4/4 | - / 69.99 | - / 89.12 | - / 71.68 | - / 90.22 |
MSP | 4/4 | - / 70.47 | - / 89.52 | - / 71.73 | - / 90.27 |

Table 1: Result from different quantization schemes for the ResNet-18 and MobileNet-v2 DNN models on CIFAR-10, CIFAR-100, and ImageNet datasets. Y/N: With/Without quantization of the first and the last layer.

| Methods | Top-1 (%) | Top-5 (%) | quant. 1st l. | quant. Last l. |
|---|---|---|---|---|
| Baseline | 69.76 | 89.08 | - | - |
| Dorefa (Zhou et al. 2016) | 68.10 | 88.10 | × | × |
| PACT (Choi et al. 2018) | 69.20 | 89.00 | × | × |
| DSQ (Gong et al. 2019) | 69.56 | N/A | × | × |
| QIL (Jung et al. 2019) | 70.10 | N/A | × | × |
| µL2Q (Cheng et al. 2019) | 65.92 | 86.72 | 16bit | × |
| LQ-NETS (Zhang et al. 2018) | 69.30 | 88.80 | × | × |
| MSP (ours) | 70.47 | 89.52 | ✓ | ✓ |

Table 2: Comparisons with existing works with ResNet-18 model on ImageNet dataset for 4 bit quantization.

5.2 Accuracy Performance

Tables 1 and 2 summarize quantization results for image classification task. We use PRSPot:F fixed:8-bit = 65 : 30 : 5, which is the optimal ratio validated from resource utilization results on FPGA. MSP obtains the minimum accuracy degradation.

The accuracy increase of MSP compared to PoT, Fixed, SPoT, MS or MP results from several aspects. First, combining SPoT and Fixed makes the quantized DNN weights fit the original weight distribution better. Besides, leave 5% weight with 8-bit, which is “intra-layer flexibility” can achieve lossless performance even the first and the last layer are quantized. In addition, model compression could slightly increase accuracy when weight bit-width ≥ 4, as quantization noise can potentially act as regularization that benefits generalization and addresses overfitting.

Tables 2 compares our MSP with existing DNN quantization works including Dorefa (Zhou et al. 2016), PACT (Choi et al. 2018), DSQ (Gong et al. 2019), QIL (Jung et al. 2019), LQ-NETS (Zhang et al. 2018). Those works and our MSP start with the same pre-trained models with the same baseline accuracy. Table 2 shows that Dorefa, PACT, DSQ, µL2Q, and LQ-NETS have up to 3.84% accuracy degradation, only QIL reports lossless accuracy performance. Our MSP increases accuracy by 0.71% compared with the floating-point model. Note that those works above they do not quantize the first
| Device    | Ratio (SpO/T/4-bit/8-bit) | Utilization | Throughput (GOPS) |
|-----------|--------------------------|-------------|-------------------|
|           |                          | LUT | DSP | BRAM36 | FF | ResNet-18 on ImageNet | MobileNet-v2 on ImageNet |
| XC7Z020   | 0:1:0                    | 12.2K | 220 | 39 | 9.4K | 31.8 | 25.6 |
|           | 1:1:0                    | 22.9K | 220 | 49 | 14.5K | 51.6 | 47.4 |
|           | 1.5:1:0                  | 28.3K | 220 | 56 | 17.1K | 58.2 | 55.3 |
|           | 60:35:5 (MSP)            | 31.1K | 220 | 59 | 20.5K | 73.8 | 58.7 |
| XC7Z045   | 0:1:0                    | 41.8K | 900 | 160 | 31.3K | 120.5 | 102.8 |
|           | 1:1:0                    | 93.4K | 900 | 194 | 65.7K | 195.3 | 190.6 |
|           | 2:1:0                    | 145.0K | 900 | 225.5 | 111.6K | 244.5 | 236.5 |
|           | 65:30:5 (MSP)            | 151.4K | 900 | 245 | 114.2K | 325.0 | 262.2 |

Table 3: Performance of various DNN applications on hardware under different settings.

| Device | Ratio | MSP | MSP | MSP | MS | MS | MS | Fixed | Fixed | PoT | PoT | PoT | SPoT | SPoT |
|--------|-------|-----|-----|-----|----|----|----|-------|-------|-----|-----|-----|------|------|
| DSP    | 8-bit FP     | 5%  | 5%  | 10% | 5% | 0  | 0  | 0     | 0     | 0   | 0   | 0   | 0    | 0    |
|        | 4-bit FP     | 30% | 0   | 95% | 50%| 50%| 50%| 33%   | 100%  | 0   | 0   | 0   | 0    | 0    |
|        | 4-bit SPoT   | 65% | 95% | 90% | 0  | 50%| 50%| 67%   | 0     | 0   | 0   | 100%| 100%| 0    |
| LUT    | 4-bit PoT    | 0   | 0   | 0   | 0  | 0  | 0  | 0    | 100%  | 0   | 0   | 0   | 0    | 0    |
|        | 65:30:5 (MSP)| Y   | Y   | Y   | N  | N  | N  | N     | N     | N   | Y   | Y   | N    | Y    |

Table 4: Ablation study of ResNet-18 on ImageNet. Y/N: With/Without quantization of the first and the last layer. The results are measured on XC7Z045.

and the last layer, only µL2Q uses 16bit weight representation for the last layer. On the other hand, MSP quantizes the first and the last layer while still can achieve the lossless accuracy performance.

### 5.3 Hardware Efficiency

To present the performance with real-world applications, we employed different CNN models with the proper SpO/T/fixed-point/8-bit ratios on the two devices. The networks ResNet-18 and MobileNet-v2 are implemented based on the ImageNet dataset. The performance results of each network under various hardware configurations are displayed in Table 3. Generally, the utilization of DSP is always 100%, by increasing the ratio of SpO/T, the utilization of the other resource has improved (e.g. from 19% to 69% on LUT in XC7Z045). On the other hand, the heterogeneous \(GEMM_{SPoT}\), \(GEMM_{fixed}\), and \(GEMM_{8-bit}\) cores improve the throughput by \(2.2 \times -2.7\times\) with the optimal design compared to utilizing the \(GEMM_{fixed}\) core only (e.g. the throughput from 120.5 to 325.0 GOPS on ResNet-18 in XC7Z045).

### 5.4 Ablation Study

We experiment over different quantization configurations to validate the proposed MSP scheme. Note that all the percentages refer to the ratio of employed quantization scheme in the main body of a DNN, since first and last layers are specified separately. As shown in Table 4, single scheme quantization (fixed point [Zhou et al. 2016], PoT, SpO/T) shows no advantage in both accuracy and speed (FPGA latency in our work). Plus, simply quantizing first and last layer into low bit width introduces noticeable accuracy degradation. With our Mixed Scheme (MS) method, execution speed is increased significantly because of efficient utilization of both DSP and LUTs. We can also observe slight improvement in accuracy, because the dual schemes are organized to better fit weight distribution, as described in [3]. Finally we employ our intra-layer mixed precision (MP) to mitigate the need of high bit widths in first and last layers, further improving speed and achieving comparable accuracy.

### 6 Conclusion

This work proposes a mixed-scheme (MS) quantization method that combines the sum-of-power-of-2 (SpO/T) quantization scheme and the traditional fixed-point quantizer. Multiplications under the SpO/T scheme can be replaced with bit shifting and addition operations using the FPGA LUT resources, and the fixed-point operations can be executed efficiently on DSP modules, therefore the heterogeneous resources on FPGA are fully exploited. Furthermore, we also develop a novel intra-layer multi-precision (MP) method to mitigate the need of high bit widths in first and last layers while still preserving accuracy. As a new dimension for mixing bit width, our MP is much more hardware friendly compared to inter-layer multi-precision quantization works. Finally, we combine the MS and MP to MSP, as an ensemble of SpO/T, low-bit fixed point and 8bit quantization. MSP achieves best accuracy results as well as fastest inference speeds on FPGA compared to prior arts. With optimal SpO/T/fixed-point/8bit ratios, our FPGA-specific quantization scheme can not only achieve 70.47% Top1 accuracy in ResNet-18 on the ImageNet dataset but also speedup 3.53× inference time compared with pure fixed point quantization on FPGA devices.
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