Optimizing the Stability of FETs Based on Two-Dimensional Materials
by Fermi Level Tuning

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Abstract

Despite the enormous progress achieved during the past decade, nanoelectronic devices based on two-dimensional (2D) semiconductors still suffer from a limited electrical stability. This limited stability has been shown to result from the interaction of charge carriers originating from the 2D semiconductors with defects in the surrounding insulating materials. The resulting dynamically trapped charges are particularly relevant in field effect transistors (FETs) and can lead to a large hysteresis, which endangers
stable circuit operation. Based on the notion that charge trapping is highly sensitive to the energetic alignment of the channel Fermi-level with the defect band in the insulator, we propose to optimize device stability by deliberately tuning the channel Fermi-level. Our approach aims to minimize the amount of electrically active border traps without modifying the total number of traps in the insulator. We demonstrate the applicability of this idea by using two differently doped graphene layers in otherwise identical FETs with Al$_2$O$_3$ as a gate oxide mounted on a flexible substrate. Our results clearly show that by increasing the distance of the Fermi-level to the defect band, the hysteresis is significantly reduced. Furthermore, since long-term reliability is also very sensitive to trapped charges, a corresponding improvement in reliability is both expected theoretically and demonstrated experimentally. Our study paves the way for the construction of more stable and reliable 2D FETs in which the channel material is carefully chosen and tuned to maximize the energetic distance between charge carriers in the channel and the defect bands in the insulator employed.

**Keywords:** Fermi-level tuning, field-effect transistor, oxide defects, defect bands, 2d materials, graphene, hysteresis, bias-temperature instability, reliability

Two-dimensional (2D) semiconductors hold the promise of revolutionizing nanoelectronics. Their inherent atomic layer thinness makes them a plausible candidate for ultimately scaled field-effect transistors (FETs) at the end of the roadmap of silicon technology. In contrast to silicon, 2D semiconductors retain sizable mobilities at thicknesses below 1 nm, a thickness which would also suppress short-channel effects in FETs, thereby allowing for channel lengths $L < 5$ nm. In addition, the flexible integration of 2D materials in van der Waals heterostructures opens up new design options for highly energy efficient transistors which overcome the limitations of thermal charge carrier injection. Beyond advancing modern nanoelectronics, 2D materials can be used for many other applications, from photonics and optoelectronics over neuromorphic computing to nano-electro-mechanical systems (NEMS), radio-frequency devices, Hall sensors and various gas and biological sensors.

Overall, theoretical prospects and available prototypes indicate a bright future for 2D
material based devices. Nevertheless, all application scenarios depend on the requirement that devices need to show stable operation throughout their lifetime, as defined by the stability of the threshold voltage $V_{TH}$. In graphene FETs (GFETs) the threshold voltage corresponds to the charge neutrality or Dirac voltage ($V_{Dirac}$), as the gate voltage where the current is at its minimum.\textsuperscript{12} When using FETs as switches in digital logic, the circuitry inherently relies on stable $V_{TH}$ of all FETs it comprises. Also applications in radio-frequency electronics rely on a stable operating point and in gas sensors for example the shift of $V_{TH}/V_{Dirac}$ can serve as measurement signal,\textsuperscript{13} thus unrelated drifts of these properties lead to measurement errors. In consequence, it is essential that FETs show minimal instabilities of the threshold voltage regardless of previous biasing, switching frequencies or temperatures.

However, stability studies on 2D FETs are scarce and typically show that their stability is at least two orders of magnitude worse\textsuperscript{14,15} compared to silicon based FETs.\textsuperscript{16,17} Typical measurements of FET stability are the evaluation of the hysteresis in the transfer characteristics\textsuperscript{18} and of the stability of the threshold voltage under prolonged periods of applied elevated gate biases and temperatures, the bias temperature instability (BTI).\textsuperscript{16} As a root cause for these phenomena early on charge trapping inside the gate oxide has been identified,\textsuperscript{19} where, facilitated by elevated gate biases and temperatures, charges are transferred between the channel and the gate oxide in a phonon mediated transition with charging time constants spanning a wide range from ns up to years.\textsuperscript{20} In optimized and stable silicon FETs these border traps in the gate oxide close to the channel determine the long-term stability and reliability,\textsuperscript{17,21} but in 2D material based FETs border traps are responsible for limited device stability on shorter time scales.\textsuperscript{22} In a first approximation, the energy levels of the defects follow a normal distribution around the average defect levels, forming defect bands,\textsuperscript{23} as in amorphous gate oxides the local surroundings of every defect differ leading to a variation in the defects’ trap levels.\textsuperscript{24} As a consequence, the overall density of border traps and the widths of the corresponding defect bands could be considerably reduced when using crystalline insulators, such as hexagonal boron nitride (hBN) or calcium fluoride (CaF$_2$).\textsuperscript{25}
However, these insulators are difficult to synthesize and come with numerous technological challenges. For example, at the current state of the art crystalline hBN can only be grown at temperatures above 1200 °C and CaF$_2$ requires a crystalline silicon (111) substrate for growth, allowing only back-gated configurations. In addition, hBN is unsuitable for use as a scaled gate insulator because of its small dielectric constant. Therefore, it would be an important breakthrough if stable FETs based on 2D semiconductors could be built based on common amorphous gate oxides such as SiO$_2$, Al$_2$O$_3$ or HfO$_2$.

Here, we address the need of stable 2D FETs by suggesting a novel engineering approach. We aim to build stable 2D FETs by carefully selecting 2D materials and tuning their Fermi level ($E_F$) such that $E_F$ does not come near to any defect band in the amorphous gate oxide during device operation. This can be realized by careful selection of the 2D material and the amorphous gate oxide and by doping the layer to move $E_F$ to the desired location. Our approach thus constitutes a stability-based design which targets to form a metal-oxide-semiconductor (MOS) system with a minimal amount of electrically active border traps without actually modifying the total number of traps in the insulator. We demonstrate that in this way, both electrical stability and reliability of 2D material based FETs can be improved. We apply our design method to GFETs with an aluminum oxide (Al$_2$O$_3$) layer as gate oxide, where we tune $E_F$ in one batch of devices by p-doping the graphene layer, thereby validating this approach. The proposed stability-based design could act as a game changer which might allow to fabricate stable 2D material based FETs, neuromorphic memory elements and sensors in the future.

Fermi Level Tuning for Stable 2D FETs

Our stability-based design approach is based on the analysis and the design of the band diagram of the MOS system, see for example a top-gated GFET in Figure 1a which forms a MOS system out of aluminum (metal), Al$_2$O$_3$ (oxide) and graphene (semiconductor). By
cutting through the MOS stack the corresponding band diagram is obtained, as indicated by the arrow in Figure 1a to the left. Every material is characterized in this view by its electron affinity, thus the energetic distance of the conduction band edge to the vacuum level and its band gap. In the case of metals and semi-metals, the work function, the energetic distance of $E_F$ to the vacuum level determines the energetic location of charge carriers. At the core of our design approach lies the knowledge about the energetic position of the oxide’s defect bands and their alignment to $E_F$.

This energetic position of defect bands in amorphous oxides is an intrinsic material property, as defect bands are related to certain defective atomic configurations inside the amorphous material which result in slightly varying trap levels depending on the local surroundings of the defects. In effect, the superposition of the trap levels of many atomic defects forms the defect band, characterized by the average energetic trap level $E_T$ and the standard deviation of the trap level distribution $\sigma_{E_T}$. In order to experimentally determine the energetic location of defect bands, the oxide defect states can be probed by electrical measurements which analyze conductance variations in MOS systems or by electron paramagnetic resonance measurements which detect the magnetic moment of unpaired electrons. Also, defect bands can be located with ab-initio calculations where possible defect states and their prevalence are analyzed, thereby identifying electrically active defect configurations like oxygen vacancies or hydrogen-related defects. Currently, the energetic locations of oxide defect bands are known for SiO$_2$, HfO$_2$, and Al$_2$O$_3$.

Based on the band alignment of the graphene work function to the defect bands in Al$_2$O$_3$, we can predict the electrical stability of the threshold voltage in these FETs. In the band diagram to the left of Figure 1a, the work function of graphene amounts to 3.9 eV, thus graphene’s $E_F$ is in the middle of the Al$_2$O$_3$ defect band. This value of $E_F$ corresponds to n-doped graphene, for example using self-assembled monolayers with amine functional groups as a substrate. Due to the alignment of the graphene Fermi level within the defect band, charge traps in the oxide will frequently capture and emit charges. As the applied gate
Figure 1: (a) The schematic image to the left shows a top gated GFET with an Al₂O₃ gate oxide. For a cut through the GFET along the indicated arrow, the energetic alignment of the Fermi level to the defect band in the aluminum gate oxide is shown. In the band diagram to the left the device is electrically unstable with respect to variations in the threshold voltage as the Fermi level is aligned within the defect band. In the band diagram to the right the Fermi level has been shifted downwards rendering the device more stable. (b) To the left the charge transfer of electrons flowing through the WS₂ channel to traps in the HfO₂ gate oxide is illustrated schematically. This situation is depicted in the left band diagram where the Fermi level is aligned close to the conduction band edge rendering the device unstable. If the Fermi level is instead aligned close to the valence band edge, the FET is stable. (c) In this band diagram the possible range of the graphene Fermi level which is attainable via doping is shown as a grey shaded region. The Fermi level can be continuously tuned within this region. (d) The injection of electrons and holes from the band edges of WS₂ is shown. In a semiconductor, the number of layers modifies the band gap and doping determines whether electrons or holes will be the majority carriers and thus govern device stability.
voltage modifies the charging probabilities of the defects according to the electric field,\textsuperscript{20} $V_{\text{TH}}$ depends on previous biasing and a pronounced hysteresis will be visible as well as considerable $V_{\text{TH}}$ drifts during prolonged periods of applied gate biases.

However, the FET stability can be tuned by moving $E_F$ down via p-doping the graphene layer, as depicted in the band diagram to the right of Figure 1a. Here, $E_F$ of graphene amounts to 5.1 eV, as achieved through p-doping for example by depositing gold nanoparticles on the graphene surface.\textsuperscript{38} As graphene’s Fermi level is located below the Al$_2$O$_3$ defect band, charge transfer is unlikely and rare. Therefore, the oxide defects are electrically inactive, resulting in stable $V_{\text{TH}}$ throughout device operation, independent of applied biases. In graphene, doping with different adsorbates and substrates yields a quasi-continuous variation of the Fermi level within 3.4 eV and 5.1 eV\textsuperscript{39,40} which can be used to tune the Fermi level during device design to minimize the impact of oxide defect bands.

When designing FETs based on 2D semiconductors, the stability-based design process needs to be adapted, see Figure 1b for a schematic drawing of a WS$_2$ FET with a HfO$_2$ top gate oxide. If the Fermi level is aligned close to the conduction band, electrons within WS$_2$ are the majority charge carriers dominating the current flow in Schottky barrier FETs.\textsuperscript{41} As the conduction band edge of WS$_2$ is aligned within the electron trapping defect band of HfO$_2$, charge transfer to oxide defects is frequent. If WS$_2$ were p-doped instead of n-doped, holes at the valence band edge would be the majority, see the band diagram to the right of Figure 1b. As the valence band edge of WS$_2$ is located below the hole trapping band in HfO$_2$, a charging of oxide defects is very improbable. Therefore, for p-doped WS$_2$ in combination with a HfO$_2$ gate oxide there are no electrically active oxide traps, leading to a stable $V_{\text{TH}}$ during device operation. It should be noted that for 2D semiconductors the charges are always injected from the conduction or valence band edge respectively. Thus, when designing a stable n-type or p-type MOSFET suitable combination of 2D semiconductor to oxide needs to be chosen.

Possibilities for tuning the stability in the context of stability-aware device design are illustrated in Figures 1c and 1d. By doping the graphene layer, graphene’s $E_F$ can be tuned
within the whole grey shaded area in Figure 1c. Thus, the design freedom for stability based device design is large in graphene based FETs, and the role of SiO$_2$ defect bands can be reduced with an $E_T$ alignment in the middle of the two defect bands and the impacts of the Al$_2$O$_3$ defect band can be minimized for p-doped graphene layers. For 2D semiconductors like WS$_2$, the design freedom for stability aware design is smaller. In Figure 1d it is shown that either the conduction or the valence band edge can be chosen via doping. However, n-type WS$_2$ will presumably be electrically unstable for these three amorphous oxides and electrically stable p-type FETs could be designed using Al$_2$O$_3$ or HfO$_2$.

**Figure 2:** (a) At the top the calculated distance of the MoS$_2$ Fermi level to its conduction band edge is shown. The hysteresis width $\Delta V_H$ is extracted at the threshold voltage, defined as $E_T$ being located at 50 meV below the conduction band edge. From simulated transfer characteristics of the MoS$_2$ FETs based on SiO$_2$, shown below, the constant current criterion of $I_{crit} = 4.8 \times 10^{-5}$ µA/µm was used to evaluate $\Delta V_H$. (b) The hysteresis width $\Delta V_H$ is shown on a logarithmic scale as a function of the distance of the oxide trap level $E_T$ to the MoS$_2$ conduction band edge $E_C$. If $E_{CB}$ is moved 82 meV down, away from the trap band, the hysteresis width will improve by one order of magnitude. (c) At two different locations of $E_C$, namely at $E_T - E_C = 0.168$ eV in dark blue and 0.25 eV in light blue corresponding to the colors of the dotted lines in (b), the band diagrams of the MoS$_2$/SiO$_2$ system are shown, demonstrating how fewer oxide traps change their charge state if the conduction band edge is shifted down, leading to a hysteresis width reduced by one order of magnitude, see (b).

It should be noted that small energy shifts of conduction or valence band edges can be sufficient to considerably improve device stability. In Figure 2, we used the previously developed drift-diffusion based TCAD methodology$^{42}$ to give an estimate for the improvement of the hysteresis width in FETs based on 2D semiconductors due to shifts of the conduction band edge $E_{CB}$, for a detailed description of the simulation methodology see the Supporting Information (SI), Figure S1. We evaluated the hysteresis width at $V_{TH}$, defined here as the
voltage where the Fermi level is located only $-0.05\,\text{eV}$ below the conduction band edge, see Figure 2a in a model system of monolayer MoS$_2$ with SiO$_2$ serving as a gate oxide. Based on the criterion for $E_F - E_{CB}$ a constant current criterion was defined and the hysteresis width was evaluated as a function of varying distance of the trap level $E_T$ to $E_{CB}$. For an oxide defect band width of $\sigma_{E_T}$ of $0.07\,\text{eV}$ the hysteresis width can be reduced by one order of magnitude if the conduction band edge is shifted $82\,\text{meV}$ downwards, as illustrated in the band diagrams in Figure 2c. These small shifts of the conduction or valence band edges can be achieved by transitioning from monolayers to bulk material as shown in 1d. For example in WS$_2$, conduction and valence band edges shift by approximately $160\,\text{meV}$ when using bilayers instead of monolayers or by about $370\,\text{meV}$ when using bulk WS$_2$ instead of monolayers, as the band gap is gradually reduced. Thus, we would expect that n-type WS$_2$ FETs with an HfO$_2$ gate oxide are most stable when using bulk WS$_2$ as a channel compared to thinner WS$_2$ layers. Independently, graphene with its continuous tunability of $E_F$ over an interval of nearly $2\,\text{eV}$ provides the largest design freedom and because of the possibility to tune the Fermi level in graphene by a few $100\,\text{meV}$ through moderate doping we chose a graphene/Al$_2$O$_3$ model system to experimentally verify our stability-based design approach.

Graphene Fermi Level and Al$_2$O$_3$ Defect Bands

We examine GFETs fabricated on mechanically flexible polyimide (PI) substrates with graphene monolayers forming the channel with an area of $W \times L = 100\mu\text{m} \times 160\mu\text{m}$, see Figure 3a. In the top-gated device layout a 40nm thick, amorphous Al$_2$O$_3$ layer grown by atomic layer deposition serves as gate oxide. We compare two nearly identical batches of GFETs with differently doped channel layers, as the graphene layers were purchased from different vendors using different parameters for the chemical vapor deposition process and the layer transfer. Type 1 graphene shows a smaller work function and in consequence a smaller distance of $E_F$ to the Al$_2$O$_3$ trap band ($E_T$). This small value of $E_T - E_F$ predicts
electrically unstable devices. In contrast, Type 2 graphene is p-doped with a higher distance of $E_F$ to $E_T$, predicting electrically more stable FETs. In addition, the layer quality of Type 1 and Type 2 is different, revealing a higher concentration of defects in graphene in Type 2 graphene, for details see their respective Raman spectra in the SI, Figure S2.

Figure 3: In (a) the schematic to the left shows the cross section while the optical microscope image to the right shows a top view of the device layout. The output ($I_D$-$V_D$) characteristics of a representative device of Type 1 are given in Figure (b) and the transfer ($I_D$-$V_G$) characteristics in Figure (c). Type 2 GFETs have the same layout as Type 1 GFETs, but are based on a different CVD grown graphene layer from another vendor. In Figure (d) the transfer ($I_D$-$V_G$) characteristics of a representative device based on Type 2 graphene are shown. In Figure (e) the mean current and voltage at the Dirac point are compared for the two graphene types. These values were calculated from the transfer characteristics measured on 5 different GFETs of every type using $V_D = 0.1$ V and a sweep time $t_{SW} = 1$ s.

To assess functionality and performance of our GFETs, the standard device characteristics, namely the output ($I_D$-$V_D$) and transfer ($I_D$-$V_G$) characteristics, are shown in Figures 3b and 3c for a representative Type 1 GFET. We observe ambipolar device operation with kinks in the output characteristics at higher $V_D$, features typical for GFETs. When com-
paring the transfer characteristics for Type 1 graphene with Type 2 graphene in Figure 3d, it can be seen that the higher quality of Type 1 leads to higher current densities. Based on two-probe measurements of the $I_D-V_G$s we estimate the field-effect mobilities to reach up to 5000 cm$^2$/Vs on Type 1 GFETs, four times higher than the average mobility of about 600 cm$^2$/Vs on Type 2 GFETs. These results are expected based on the Raman analysis and originate from the higher amount of defects in Type 2 graphene. Negatively charged dopants in Type 2 lead to a higher variability and shift $V_{\text{Dirac}}$ towards more positive voltages, see Figure 3e. A more positive $V_{\text{Dirac}}$ corresponds to a higher p-doping of the sample and correlates with a higher work function ($E_W$).\textsuperscript{38,46} Pristine graphene has a work function of 4.56 eV,\textsuperscript{47} which is shifted towards higher values by p doping\textsuperscript{38,48} and towards smaller values by n doping.\textsuperscript{37,46} In order to estimate Fermi level location in the two graphene types, we approximate the charge carrier concentration $n$ at 0 V gate bias based on the analytic approximation for the drain current of a MOSFET in the linear region

$$n = \frac{I_D(V_G = 0 \text{ V})}{\mu_{\text{eff}} W L q V_D}. \quad (1)$$

This expression gives a p-doping density for Type 1 graphene of $n_1 = 8.2 \times 10^{11}$ cm$^{-2}$ and for Type 2 graphene of $n_1 = 4.7 \times 10^{12}$ cm$^{-2}$, thus Type 2 graphene is more p-doped by an additional doping density of approximately $3.9 \times 10^{12}$ cm$^{-2}$. These hole densities in the graphene layers at 0 V gate voltage determine the work function via\textsuperscript{37,49}

$$E_W = \hbar \nu_F \sqrt{\pi n} \quad (2)$$

with the Fermi velocity of graphene $\nu_F = 1.1 \times 10^6$ ms$^{-1}$. In consequence, we estimate $E_{W_1}$ of Type 1 graphene to be 4.7 eV and $E_{W_2}$ of Type 2 graphene to be 0.2 eV higher at 4.9 eV.

To further analyze our model system we fabricated devices with Type 1 graphene but using thermal SiO$_2$ on silicon and quartz substrates instead of the flexible PI layer. In addition, the quality of the interface between graphene and Al$_2$O$_3$ was modified by transferring
single-layer CVD-grown hBN layers before the ALD deposition or by sputtering ∼ 2 nm thick aluminum as a seed layer for the Al₂O₃ growth process. As will be seen in the discussion of these results in the SI Figure S3, the substrate primarily impacts the maximum current density whereas the quality of the interface with the Al₂O₃ impacts device stability.

(a)

(b)

(c) Type 1.

(d) Type 2.

Figure 4: In (a) the band diagram illustrates the alignment of the Al₂O₃ defect band to the graphene of Type 1 and Type 2. To the left, the location of defect bands as extracted from experiments is shown: [1], [2], [3], [4], [5], [6], [7], [8], [9]. To the right, the alignment of the defect band caused by oxygen vacancies and Al interstitials in amorphous Al₂O₃ is shown according to the DFT calculations presented by Dicks et al. [6]. In (b) the active region which is probed by measurements in the [−5 V, 5 V] and [−10 V, 10 V] range is shown for two defect band alignments for Type 1 GFETs. In (c) schematic band diagrams show the charging and discharging of defects in Al₂O₃ for Type 1 graphene with a work function of E_W = 4.7 eV. In (d) the band diagrams for Type 2 graphene with E_W = 4.9 eV are shown.

To accurately determine the alignment of E_T in graphene to the electron trapping band of the amorphous Al₂O₃ gate oxide at ET, the precise location of the oxide defect band is essential. Several studies have investigated the alignment of this defect band using trap spectroscopy by charge injection and sensing (TSCIS), [32, 50] BTI [51, 52] and hysteresis measurements. [53] Obtained defect band alignments of Al₂O₃ from literature are shown in Figure 4a,
with parameters listed in Table S1 in the SI. Based on density functional theory (DFT) calculations, this defect band can be associated with either oxygen vacancies\textsuperscript{54,55} or aluminum interstitials.\textsuperscript{54} We use for our study a normally distributed defect band with the mean defect level being located at $E_C - E_T = 2.15 \pm 0.3$ eV below the conduction band edge of Al$_2$O$_3$. The electron affinity ($\chi$) of Al$_2$O$_3$, which determines the location of the conduction band edge, varies in literature. Here, we use 1.96 eV as obtained from internal photoemission measurements.\textsuperscript{56} We use the same level as in\textsuperscript{53} of 4.1 eV which is below the level of 3.4 eV obtained in most other experimental references.\textsuperscript{50,52} However, the theoretical value of 4 eV\textsuperscript{54} is closer to our estimate of the defect bands’ location. In addition, for all measurement ranges used in our work, we probe only the lower part of a potentially wider defect band further up, as measured by other methods.\textsuperscript{51} This is illustrated in Figure 4b, where the regions which can be probed by measurements are shaded in light red and yellow. These shaded regions reach the upper edge of the defect band used in this work but cover only the lower part of the wider defect band reported by Franco \textit{et al.}\textsuperscript{51} For Type 1 graphene $E_F$ is aligned within the defect band (small $E_T - E_F$, electrically unstable), see Figure 4c, whereas it is aligned below the defect band for Type 2 graphene (high $E_T - E_F$, electrically stable), see Figure 4d. We will see in the next sections that the 200 meV downwards shift of the Fermi level of Type 2 graphene is sufficient to render the $V_{\text{Dirac}}$ of these GFETs more stable.

Hysteresis dynamics

As the observed hysteresis depends critically on the voltage ranges used for the gate voltage sweeps, we compare the bias ranges used with ranges for various applications in Figure 5a. State-of-the-art silicon transistors operate at an electric gate field of 10 MV/cm estimated based on the equivalent oxide thickness (EOT),\textsuperscript{57} up to which logical switches should show stable operation. As our devices employ an aluminum oxide layer of 40 nm physical thickness as a gate oxide, their EOT amounts to $\sim$17 nm. When used in radio-frequency (RF) circuits
the electric gate fields span from 3.5 MV/cm to 8.1 MV/cm\textsuperscript{58–61} and thus the gate oxide fields we investigate here are standard operation conditions for RF applications. If on the other hand GFETs are used as sensors in the form of phototransistors\textsuperscript{62,63} or Hall elements,\textsuperscript{64} moderate gate fields of up to 1 MV/cm are sufficient to maximize responsivity.

Figure 5: In (a) the electrical oxide fields for measured voltage ranges are compared to voltage ranges for various applications. The field up to which GFETs should show stable operation is shown at the top in dark blue\textsuperscript{57} and the ranges we use here are shown in purple below. Application scenarios are from [1],[60,2],[61],[3],[59],[4],[58],[5],[64],[6],[7]. In (b) the hysteresis in the transfer characteristic measured on 5 different GFETs is shown, illustrating the variability of the devices. In (c) the hysteresis width as a function of $1/t_{SW}$ is shown for 5 different devices for each graphene type. Full circles stand for Type 1 GFETs and empty triangles for Type 2 GFETs, the solid and dashed lines are guides to the eye for Type 1 and Type 2 respectively. In (e) the Dirac point shifts of the up and down sweep are shown with empty/full symbols for $V_{\text{Dirac,down}}/V_{\text{Dirac,up}}$. In (f) the hysteresis width for Type 1 and Type 2 is shown.

As a first step in the hysteresis evaluation on our prototypes, we compare the double sweep transfer characteristics for a small voltage range of $[-5 V, 5 V]$ on five GFETs based on Type 1 graphene in Figure 5b. We see little variability which is confirmed when studying
the hysteresis width $\Delta V_H$ as a function of the inverse sweep time, the sweep frequency $(f = 1/t_{SW})$. In Figure 5c the hysteresis width as a function of the sweep frequency is shown for five GFETs based on Type 1 and five GFETs based on Type 2. Type 2 devices show a considerably higher variability of $\Delta V_H$ than Type 1 devices, which is linked to the increased variability of $V_{\text{Dirac}}$ on Type 2, see Figure 3e. In addition, on Type 2 GFETs the hysteresis is higher and for both types the largest hysteresis is observed for the slowest sweeps as there the largest number of oxide defects can change their charge state. An increased bias range of $[-10 \text{ V}, 10 \text{ V}]$ increases the hysteresis, because more oxide defects become accessible for charge transfer, as can be seen in Figure 5e. To shed more light on this behavior, the dynamics of the Dirac voltage shifts are analyzed as a function of the sweep frequency in Figure 5d. For the $[-5 \text{ V}, 5 \text{ V}]$ sweep, $V_{\text{Dirac,up}}$ and $V_{\text{Dirac,down}}$ as a function of the sweep frequency show similar slopes for both types. However, for the $10 \text{ V}$ sweep range and Type 1, $V_{\text{Dirac,up}}$ is shifted to more negative voltages in slow sweeps, while $V_{\text{Dirac,down}}$ is shifted to more positive voltages. This indicates that for large sweep ranges on Type 1 GFETs, a significant amount of electrons are emitted from oxide traps between $-10 \text{ V}$ and $V_{\text{Dirac,up}}$, whereas for Type 2 charge trapping in this interval can be neglected. This reversed drift of $V_{\text{Dirac,up}}$ to more negative voltages for slow sweeps results in an increase in the hysteresis width in Type 1 GFETs, see Figure 5e. An increased hysteresis at large sweep ranges for Type 1 confirms our hypothesis, as in Type 1 GFETs $E_F$ is closer to the Al$_2$O$_3$ defect band.

In fact, the band alignment shown in Figures 4c and 4d explains the larger hysteresis in Type 1 GFETs in comparison to Type 2 satisfactorily: In Type 1 GFETs biased at $V_{\text{Dirac}}$, a considerable number of defects is negatively charged. If a negative voltage is applied, these defects discharge due to the band bending and thus $V_{\text{Dirac}}$ is shifted to more negative voltages during a slow up-sweep (Figure 5d). In Type 2 GFETs, in contrast, the Fermi level is located below the defect band at $V_{\text{Dirac}}$, as its Fermi level has been shifted down by 200 meV via p-doping. Thus, most defects are neutral at the Dirac voltage. If a long time is spent with the GFET biased at negative voltages, the charge states do not change and the location of
\( V_{\text{Dirac}} \) during the up sweep is stable independent from the sweep time.

In short, the higher \( E_T - E_F \) of Type 2 graphene with respect to the \( \text{Al}_2\text{O}_3 \) defect band leads to a smaller hysteresis width for large sweep ranges. In turn, the threshold voltage in Type 2 GFETs is more stable, as predicted by our stability-based design approach. At small gate bias ranges and fast hysteresis sweeps, Type 2 devices suffer from more charge trapping at the unclean interface with the \( \text{Al}_2\text{O}_3 \), and the hysteresis is similar or even higher in Type 2 devices compared to Type 1 (see Figures 5c and additional data in SI, Figure S4). For fast sweeps, fast traps at the unclean interface in Type 2 GFETs increase the hysteresis, giving the impression of a frequency independent hysteresis width (Figure 5e). Type 1 GFETs exhibit a cleaner interface but a smaller \( E_T - E_F \) with respect to the \( \text{Al}_2\text{O}_3 \) defects, strongly degrading the GFETs during slow sweeps. For high gate bias ranges and slow sweeps, the border traps of the \( \text{Al}_2\text{O}_3 \) dominate device stability, thus more stable operation of Type 2 GFETs is observed. These results confirm that it is the alignment of the \( \text{Al}_2\text{O}_3 \) defect band to graphene \( E_W \) which determines the GFETs’ stability and that this alignment can be deliberately tuned by doping the graphene layer.

**Stability under static gate bias**

For evaluating the long-term stability of the GFETs, we analyzed the Dirac voltage shifts \((\Delta V_{\text{Dirac}})\) after static elevated gate voltages \((V_{\text{G,high}})\) were applied for varying charging times \((t_{\text{charging}})\). We record the magnitude of the initial \( \Delta V_{\text{Dirac}} \) shift and monitor the recovery after the increased gate biasing period with fast \( I_D-V_G \) sweeps at logarithmically spaced recovery times. In Figure 6a the fast \( I_D-V_G \) sweeps recorded during the recovery from negative gate biasing (NBTI) at \(-10\) V are shown.

NBTI measured by subjecting the devices to a gate bias of \(-10\) V for increasingly long charging times is shown in Figure 6b for Type 1 GFETs and in Figure 6c for Type 2 GFETs. As designed, the \( V_{\text{Dirac}} \) shifts are smaller on Type 2 devices than on Type 1 devices. GFETs
Figure 6: In a BTI measurement the FET is subjected to extended periods of elevated gate bias and the drifts of the Dirac voltage during the degradation and recovery periods are recorded, see (a) for a Type 1 device subjected to −10 V for 1 ks. In (b) a Type 1 FET is subjected for increasing time spans to elevated NBTI gate bias of −10 V, resulting in a larger degradation than observed for the same conditions on Type 2 FETs in (c). When applying to the GFETs an elevated PBTI voltage level of 10 V in (d), the Dirac voltage device subjected to −10 V, resulting in a larger degradation than observed for the same conditions on Type 2 FETs in (c). When applying to the GFETs an elevated PBTI voltage level of 10 V in (d), the Dirac voltage of Type 1 devices drifts more and hardly recovers (see (e)) in comparison with their Type 2 counterparts (f). In order to avoid an impact of the measurement history, the measurements shown were performed on different devices.

Based on Type 2 graphene are more stable with respect to long-term degradation because graphene’s $E_F$ is further away from the Al$_2$O$_3$ defect band, see Figure 4d. Therefore, on Type 2 GFETs fewer oxide traps change their charge state during negative gate bias, resulting in smaller shifts of $V_{\text{Dirac}}$ which also recover faster as the traps which emit electrons are located closer to the interface and thus have smaller time constants. For more details, see the recovery traces of NBTI at −5 V in the SI, Figure S5. In Figure 6d the fast $I_D$-$V_G$ sweeps measured after a positive bias at 10 V are shown, together with the corresponding recovery traces for Type 1 GFETs in Figure 6e and for Type 2 GFETs in Figure 6f. For both device
types degradation when applying positive biases (PBTI) are higher than NBTI shifts, as the Fermi level in graphene is at the lower edge of the Al₂O₃ defect band, see Figure 4c. Thus, the number of defects which can become more negatively charged during positive bias is larger than the number of defects which can emit one of their electrons during negative bias. As the picture of charge transfer to oxide defects in Al₂O₃ explains these observations to full satisfaction, these results confirm our stability-based design approach, as we successfully designed Type 2 GFETs to be more stable. By p-doping Type 2 graphene, $E_F$ was moved further away from the Al₂O₃ defect band, thus reducing the amount of charge trapping.

Interestingly, throughout all charging times the shifts on Type 1 devices do not recover whereas the shifts on Type 2 devices recover completely. The most surprising observation is that this is also true for a short time of only 1 s. This observation was confirmed when subjecting the devices to a smaller gate bias voltage of 5 V, see the SI Figure S5. To explain the permanent component of BTI degradation, the creation of defects in Al₂O₃ has to be hypothesized. In silicon FETs using SiO₂ as a gate dielectric the permanent component of BTI has been associated with gate-sided hydrogen release. In this model hydrogen diffuses under prolonged biasing conditions through the oxide and creates new oxide defects which cause permanent voltage shifts. We speculate that a similar mechanism of bias facilitated oxide defect creation in the Al₂O₃ is responsible for the permanent PBTI observed on our GFETs, which will need to be investigated by future studies.

Conclusions

We have presented the idea that electrically stable FETs based on 2D materials can be designed by tuning the energetic alignment of the Fermi level to reduce the impact of the defect bands in amorphous gate oxides. This approach is founded on the premise that charge trapping at the border traps in amorphous oxides is the key reason which leads to the strong variations in the threshold voltage in 2D FETs and their reduced long-term stability. Based
on these facts we suggested a design approach to improve device stability by tuning the Fermi level in 2D materials. In 2D semiconductors the design options mainly lie in choosing suitable materials depending on n- or p-doping or varying the thickness of the layers to minimize the role of known defect bands in the oxides. In graphene, there is more design freedom as the graphene Fermi level can be tuned continuously over a range of up to 2 eV. Thus, we demonstrated the validity of our design approach using GFETs with Al₂O₃ as a top gate oxide and two different types of graphene which only differ in their respective doping and thus their Fermi level alignment. Our measurement results on these two GFET types have shown, that the GFETs based on more p-doped Type 2 graphene with the higher \( E_F \) have a smaller hysteresis and an increased stability of the Dirac voltage when subjected to prolonged elevated gate biases. These results confirm the validity of our stability based design approach and suggest that more stable 2D material based FETs could be built by minimizing the impact of defect bands in the gate oxides in the design process.

Our approach holds the promise of fabricating electrically stable 2D FETs and is universally applicable to all insulators. We expect that it will lead to further improvements in the electrical stability of devices based on crystalline insulators where the impact of narrow insulator defect bands can be further reduced than in amorphous oxides. Nevertheless, it remains to be clarified in future studies which levels of electrical stability can be attained with these Fermi level tuned systems based on amorphous oxides and on crystalline insulators, respectively. In addition, stability-based design relies on the knowledge about the defect bands in the oxide which is at the moment incomplete. Thus, it cannot be excluded that in parts of the oxide band gap which is at the moment thought to be free of defect bands, new defect bands might be discovered. Therefore, while the potential gains of taking the stability-based perspective into account from the beginning of the design process could be high, there are currently many unknowns related to feasibility and practicability of the suggested design paradigm which will need to be addressed in future studies.
Methods

Device fabrication: Our top-gated GFETs were fabricated on spin coated polyimide (PI) substrates using photolithography. First, the flexible substrate was prepared by spin coating PI in liquid form on a Si wafer and subsequently curing the layer. The thickness of the solidified PI film was about 8\(\mu\)m. During the fabrication process, a rigid Si substrate was used as a support layer. In the next step a CVD grown graphene layer was transferred to the PI substrate. We study two batches of GFETs where the channel is formed by graphene samples purchased from different vendors, namely vendor 1 (Type 1) and vendor 2 (Type 2). For Type 1 devices the CVD graphene was transferred from the copper growth substrate using a PMMA assisted wet transfer method,\textsuperscript{66} for Type 2 GFETs the transfer was performed by vendor 1. The Type 1 graphene flake covered an area of \(2 \times 2\) cm and was of higher quality than the Type 1 flake which covered a 6 inch wafer. The different quality of the graphene layers was confirmed by Raman spectroscopy, for details see the supporting information. The graphene layer was patterned in an oxygen plasma etch step to form channels of a length \((L)\) of 160\(\mu\)m and a width \((W)\) of 100\(\mu\)m. In the next step, the source and drain contacts were deposited by sputtering 50\,nm Ni, followed by a lift-off process. This step was followed by growing 40\,nm of Al\(_2\)O\(_3\) with atomic layer deposition (ALD) on top of the devices to form the gate oxide in a top-gated configuration. In order to finalize the GFETs, the top-gate electrode was fabricated by sputtering 10\,nm of Ti and 150\,nm of Al and patterned in a lift-off process. To be able to contact source and drain pads, vias were opened through the Al\(_2\)O\(_3\) with wet buffered oxide etchant.

Measurement technique: Our electrical measurements were performed in vacuum at room temperature and in complete darkness. The devices were examined with the PI supported on a silicon wafer. From two-probe measurements we extracted the field-effect mobility of the GFETs and found it to be 4000\,cm\(^2\)/Vs for Type 1 graphene and 1000\,cm\(^2\)/Vs for Type 2 graphene. The Hall mobility of both samples was found to be slightly higher. The hysteresis was analyzed by measuring the double sweep \(I_D-V_G\) characteristics using different sweep
times $t_{sw}$ and sweep ranges $V_{G_{minthe}}$ to $V_{G_{max}}$. The hysteresis width $\Delta V_H$ was extracted as the difference between the forward and reverse sweep $V_{Dirac}$. As was suggested in our previous work, we expressed the hysteresis dynamics using the $\Delta V_H(1/t_{sw})$ traces. Finally, the BTI degradation/recovery dynamics were analyzed using subsequent degradation/recovery rounds with either fixed stress time $t_{deg}$ and increasing high voltage levels $V_{G,high}$, or fixed $V_{G,high}$ and increasing $t_{deg}$. During the recovery period we apply a constant recovery voltage of $V_{G,\text{recovery}} = 1$ V between the sweeps. This voltage is chosen to be close to the charge carrier equilibrium at $V_{Dirac}$. In order to avoid artifacts from fast traps charged during the sweep, the down sweep $I_D-V_G$ is used to monitor the recovery of NBTI. The characteristics obtained when using up sweeps to measure NBTI recovery are shown in the SI Figure S6. For positive bias temperature instability (PBTI) measurements, the recording of the up sweep minimizes artifacts, thus we used $I_D-V_G$ sweeps from negative to positive voltages for the evaluation of PBTI. As was suggested in our previous study on GFETs, we expressed the BTI degradation magnitude using Dirac point voltage shift $\Delta V_{Dirac}$ and plotted it versus the relaxation time $t_r$. In order to gain more statistics, all our measurements were repeated on several devices.

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References

(1) Akinwande, D. et al. Graphene and two-dimensional materials for silicon technology. *Nature* 2019, 573, 507–518.

(2) English, C. D.; Shine, G.; Dorgan, V. E.; Saraswat, K. C.; Pop, E. Improved contacts to MoS2 transistors by ultra-high vacuum metal deposition. *Nano Letters* 2016, 16, 3824–3830.

(3) Fiori, G. et al. Electronics based on two-dimensional materials. *Nature Nanotechnology* 2014, 9, 768–779.

(4) Liu, Y.; Huang, Y.; Duan, X. Van der Waals integration before and beyond two-dimensional materials. *Nature* 2019, 567, 323–333.

(5) Iannaccone, G.; Bonaccorso, F.; Colombo, L.; Fiori, G. Quantum engineering of transistors based on 2D materials heterostructures. *Nature Nanotechnology* 2018, 13.

(6) Mak, K. F.; Shan, J. Photonics and optoelectronics of 2D semiconductor transition metal dichalcogenides. *Nature Photonics* 2016, 10.

(7) Sangwan, V. K.; Hersam, M. C. Neuromorphic nanoelectronic materials. *Nature Nanotechnology* 2020, 15, 517–528.

(8) Lemme, M. C. et al. Nanoelectromechanical sensors based on suspended 2D materials. *Research* 2020, 2020, 25.

(9) Schwierz, F.; Pezoldt, J.; Granzner, R. Two-dimensional materials and their prospects in transistor electronics. *Nanoscale* 2015, 7, 8261–8283.

(10) Wang, Z.; Shaygan, M.; Otto, M.; Schall, D.; Neumaier, D. Flexible Hall sensors based on graphene. *Nanoscale* 2016, 8, 7683–7687.
(11) Mortazavi Zanjani, S. M.; Holt, M.; Sadeghi, M. M.; Rahimi, S.; Akinwande, D. 3D integrated monolayer graphene Si CMOS RF gas sensor platform. *npj 2D Materials and Applications* 2017, 1, 1–8.

(12) Martin, J. et al. Observation of electron-hole puddles in graphene using a scanning single-electron transistor. *Nature Physics* 2008, 4, 144–148.

(13) Fu, W.; Jiang, L.; van Geest, E. P.; Lima, L. M.; Schneider, G. F. Sensing at the Surface of Graphene Field-Effect Transistors. *Advanced Materials* 2017, 29, 1–25.

(14) Yang, S.; Park, S.; Jang, S.; Kim, H.; Kwon, J. Y. Electrical stability of multilayer MoS2 field-effect transistor at various temperatures. *Physica Status Solidi - Rapid Research Letters* 2014, 8, 714–718.

(15) Illarionov, Y. et al. Improved Hysteresis and Reliability of MoS2 FETs with High-Quality CVD Growth and Al2O3 Encapsulation. *IEEE Electron Device Letters* 2017, 38, 1763–1766.

(16) Stathis, J. H.; Zafar, S. The negative bias temperature instability in MOS devices: A review. *Microelectronics Reliability* 2006, 46, 270–286.

(17) Grasser, T. et al. Analytic modeling of the bias temperature instability using capture/emission time maps. *Technical Digest - International Electron Devices Meeting, IEDM 2011*, 27.4.1–27.4.4.

(18) Late, D. J.; Liu, B.; Matte, H. S. S. R.; Dravid, V. P.; Rao, C. N. R. Hysteresis in single-layer MoS2 field effect transistors. *ACS Nano* 2012, 6, 5635–41.

(19) Thomas, J. E.; Young, D. R. Space-Charge Model for Surface Potential Shifts in Silicon Passivated with Thin Insulating Layers. *IBM Journal of Research and Development* 1964, 8, 368–375.
(20) Grasser, T. Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities. *Microelectronics Reliability* **2012**, *52*, 39–70.

(21) Fleetwood, D. M. et al. Effects of oxide traps, interface traps, and "border traps" on metal-oxide-semiconductor devices. *Journal of Applied Physics* **1993**, *73*, 5058–5074.

(22) Illarionov, Y. Y. et al. The Role of Charge Trapping in MoS$_2$/SiO$_2$ and MoS$_2$/hBN Field-Effect Transistors. *2D Materials* **2016**, *3*, 035004.

(23) Kaczer, B. et al. A brief overview of gate oxide defect properties and their relation to MOSFET instabilities and device and circuit time-dependent variability. *Microelectronics Reliability* **2018**, *81*, 186–194.

(24) Goes, W. et al. Identification of oxide defects in semiconductor devices: A systematic approach linking DFT to rate equations and experimental evidence. *Microelectronics Reliability* **2018**, *87*, 286–320.

(25) Illarionov, Y. Y. et al. Insulators for 2D nanoelectronics: the gap to bridge. *Nature Communications* **2020**, *11*.

(26) Shi, Z. et al. Vapor-liquid-solid growth of large-area multilayer hexagonal boron nitride on dielectric substrates. *Nature Communications* **2020**, *11*.

(27) Illarionov, Y. Y. et al. Ultrathin calcium fluoride insulators for two-dimensional field-effect transistors. *Nature Electronics* **2019**, *2*, 8–13.

(28) Knobloch, T. et al. The performance limits of hexagonal boron nitride as an insulator for scaled CMOS devices based on two-dimensional materials. *Nature Electronics* **2021**, *4*, 98/108.

(29) Blöchl, P. E. First-principles calculations of defects in oxygen-deficient silica exposed to hydrogen. *Physical Review B - Condensed Matter and Materials Physics* **2000**, *62*, 6158–6179.
(30) Rzepa, G. et al. Comphy - a compact-physics framework for unified modeling of BTI. *Microelectronics Reliability* **2018**, *85*, 49–65.

(31) Shluger, A. In *Handbook of Materials Modeling: Applications: Current and Emerging Materials*; Andreoni, W., Yip, S., Eds.; Springer International Publishing: Cham, 2020; pp 1013–1034.

(32) Degraeve, R. et al. Trap spectroscopy by charge injection and sensing (TSCIS). *International Electron Devices Meeting, IEDM* **2008**, 10–13.

(33) Nagumo, T.; Takeuchi, K.; Hase, T.; Hayashi, Y. Statistical characterization of trap position by RTN measurement of multiple individual traps. *International Electron Devices Meeting, IEDM* **2010**, 628–631.

(34) Weeks, R. A. The many varieties of E’ centers: a review. *Journal of Non-Crystalline Solids* **1994**, *179*, 1–9.

(35) Muñoz Ramo, D.; Gavartin, J. L.; Shluger, A. L.; Bersuker, G. Spectroscopic properties of oxygen vacancies in monoclinic HfO_2 calculated with density functional theory. *Physical Review B* **2007**, *75*, 1–12.

(36) Grasser, T. et al. On the microscopic structure of hole traps in pMOSFETs. *IEEE International Electron Devices Meeting* **2014**, 21.1.1–4.

(37) Park, J. et al. Work-function engineering of graphene electrodes by self-assembled monolayers for high-performance organic field-effect transistors. *Journal of Physical Chemistry Letters* **2011**, *2*, 841–845.

(38) Shi, Y. et al. Work function engineering of graphene electrode via chemical doping. *ACS Nano* **2010**, *4*, 2689–2694.

(39) Kwon, K. C.; Choi, K. S.; Kim, S. Y. Increased work function in few-layer graphene sheets via metal chloride Doping. *Advanced Functional Materials* **2012**, *22*, 4724–4731.
(40) Wittmann, S. et al. Dielectric Surface Charge Engineering for Electrostatic Doping of Graphene. *ACS Applied Electronic Materials* **2020**, *2*, 1235–1242.

(41) Appenzeller, J.; Zhang, F.; Das, S.; Knoch, J. *2D Materials for Nanoelectronics*; CRC Press, 2016; Chapter 8, pp 207–234.

(42) Knobloch, T. et al. A Physical Model for the Hysteresis in MoS2 Transistors. *IEEE Journal of the Electron Devices Society* **2018**, *6*, 972–978.

(43) Jo, S.; Ubrig, N.; Berger, H.; Kuzmenko, A. B.; Morpurgo, A. F. Mono- and bilayer WS2 light-emitting transistors. *Nano Letters* **2014**, *14*, 2019–2025.

(44) Wang, Z. et al. Flexible One-Dimensional Metal-Insulator-Graphene Diode. *ACS Applied Electronic Materials* **2019**, *1*, 945–950.

(45) Schwierz, F. Graphene transistors. *Nature Nanotechnology* **2010**, *5*, 487–496.

(46) Kwon, K. C.; Choi, K. S.; Kim, B. J.; Lee, J. L.; Kim, S. Y. Work-function decrease of graphene sheet using alkali metal carbonates. *Journal of Physical Chemistry C* **2012**, *116*, 26586–26591.

(47) Yan, R. et al. Determination of graphene work function and graphene-insulator-semiconductor band alignment by internal photoemission spectroscopy. *Applied Physics Letters* **2012**, *101*.

(48) Seo, J. T. et al. Manipulation of graphene work function using a self-assembled monolayer. *Journal of Applied Physics* **2014**, *116*.

(49) Zhang, Y. et al. Giant phonon-induced conductance in scanning tunnelling spectroscopy of gate-tunable graphene. *Nature Physics* **2008**, *4*, 627–630.

(50) Zahid, M. B. et al. Applying complementary trap characterization technique to crystalline γ-phase-Al2O3. *IEEE Transactions on Electron Devices* **2010**, *57*, 2907–2916.
(51) Franco, J. et al. Suitability of high-k gate oxides for III-V devices: A PBTI study in In_{0.53}Ga_{0.47}As devices with Al_2O_3. *IEEE International Reliability Physics Symposium Proceedings* 2014, 6–11.

(52) Putcha, V. et al. Impact of slow and fast oxide traps on In_{0.53}Ga_{0.47}As device operation studied using CET maps. *IEEE International Reliability Physics Symposium Proceedings* 2018, 5A.31–5A.37.

(53) Illarionov, Y. et al. Energetic Mapping of Oxide Traps in MoS_2 Field-Effect Transistors. *2D Mater.* 2017, 4, 025108.

(54) Dicks, O.A. and Cottom, J. and Shluger, A.L. and Afanas’ev, V.V., The Origin of Negative Charging in Amorphous Al_2O_3 Films: the Role of Native Defects. *Nanotechnology* 2019, 30, 205201.

(55) Guo, Y.; Li, H.; Robertson, J. AlN and Al oxy-nitride gate dielectrics for reliable gate stacks on Ge and InGaAs channels. *Journal of Applied Physics* 2016, 119.

(56) Afanas’ev, V. V.; Stesmans, A.; Tsai, W. Determination of interface energy band diagram between (100)Si and mixed Al-Hf oxides using internal electron photoemission. *Applied Physics Letters* 2003, 82, 245–247.

(57) IEEE, *IRDS More Moore*; 2020; pp 1–30.

(58) Lemme, M. C.; Member, S.; Echtermeyer, T. J.; Baus, M.; Kurz, H. A Graphene Field-Effect Device. *IEEE Electron Device Letters* 2007, 28, 282–284.

(59) Kedzierski, J. et al. Graphene-on-insulator transistors made using C on Ni chemical-vapor deposition. *IEEE Electron Device Letters* 2009, 30, 745–747.

(60) Wei, W. et al. Mechanically robust 39 GHz cut-off frequency graphene field effect transistors on flexible substrates. *Nanoscale* 2016, 8, 14097–14103.
(61) Bonmann, M. et al. Graphene field-effect transistors with high extrinsic $f_T$ and $f_{max}$.

*IEEE Electron Device Letters* **2019**, *40*, 131–134.

(62) Mueller, T.; Xia, F.; Avouris, P. Graphene photodetectors for high-speed optical communications. *Nature Photonics* **2010**, *4*, 297–301.

(63) Konstantatos, G. et al. Hybrid Graphene–Quantum Dot Phototransistors with Ultra-high Gain. *Nat. Nanotechnol.* **2012**, *7*, 363.

(64) Uzlu, B. et al. Gate-tunable graphene-based Hall sensors on flexible substrates with increased sensitivity. *Scientific Reports* **2019**, *1*, 1–7.

(65) Grasser, T. et al. Gate-sided hydrogen release as the origin of ”permanent” NBTI degradation. *International Electron Devices Meeting, IEDM* **2016**, 20.1.1–20.1.4.

(66) Suk, J. W. et al. Transfer of CVD-grown monolayer graphene onto arbitrary substrates. *ACS Nano* **2011**, *5*, 6916–6924.

(67) Illarionov, Y. et al. Bias-Temperature Instability in Single-Layer Graphene Field-Effect Transistors. *Appl. Phys. Lett.* **2014**, *105*, 143507.