Measurement of Power Dissipation Due to Parasitic Capacitances of Power MOSFETs

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Abstract

Analysis of the switching losses in a power MOSFET is crucial for the design of efficient power electronic systems. Currently, the state-of-the-art technique is based on measured drain current and drain-to-source voltage during the switching intervals. However, this technique does not separate the switching power due to the resistance of the MOSFET channel and due to the parasitic capacitances. In this paper, we propose a measurement method to extract the power dissipation due to the parasitic capacitances of a MOSFET, providing useful information for device selection and for the design of efficient power electronic systems. The proposed method is demonstrated on a basic boost converter. The proposed method shows that the existing method underestimates the turn-On losses by 41% and overestimates the turn-Off losses by 35%.

Index Terms

Channel current, current diversion phenomenon, \( C_{\text{OSS}} \) losses, efficiency, power losses, power MOSFET, switching losses.

I. INTRODUCTION

With the increase in demands for electricity and the explosion in renewable energy technologies, power electronics is playing a vital role in benefiting society. The progress of power electronic systems is being driven by advancements in power semiconductor devices [1]. As the market for power devices continues to grow, it is becoming increasingly important to select the appropriate power device for a given application. One of the most important parameters for selection of a power device is its power dissipation, and so an understanding of the power losses is crucial.

The most commonly used power switching device, the power MOSFET, exhibits two types of losses: switching losses and conduction losses. Operation at high frequencies is desirable to reduce the overall converter size but, on the other hand, it also results in an increase in the MOSFET switching losses. Therefore, to obtain a high efficiency design, it is necessary to accurately determine the switching losses of the power MOSFET.

The current state-of-the-art technique for measuring switching loss of a power MOSFET is performed by integrating the product of the drain-to-source voltage \( (v_{DS}) \) and drain current \( (i_D) \). However, the dynamic characteristics of a power MOSFET are affected by the various parasitic capacitances in the device [2]. These are not considered when applying the standard technique, which leads to underestimation and an overestimation of the power losses during the turn-On and turn-Off intervals, respectively. In order to account for these capacitances, we need to know the difference between the total current through the drain terminal \( (i_D) \) and the current flowing through the channel \( (i_{CH}) \).

The ability to separate \( i_{CH} \) from \( i_D \) enables proper analysis of charging and discharging of the effective output capacitance \( (C_{OSS}) \) and its corresponding power dissipation. This knowledge aids in the selection of the appropriate MOSFET for a particular application. In response to this need, various modeling and simulation techniques have been used to analyze the difference between \( i_{CH} \) from \( i_D \) and the impact of this difference on the switching power losses [3]–[9]. Although simulation-based analyses provide useful insights, measurements with real MOSFETs and in real circuits are necessary to obtain the ultimate results. Unlike simulation
and modeling, the only current that can be measured in a packaged MOSFET is the current flowing through the drain terminal. It appears that this has been seen as an unavoidable limit and, consequently, no measurement results separating $i_{CH}$ from $i_D$ have been reported. In this paper, we show how to avoid this perceived limit by employing a combination of static and dynamic measurements, which results in a novel experimental method for extracting $i_{CH}$ of a power MOSFET. With this technique, measured switching losses can be split into contributions due to the parasitic capacitances and due to the channel resistance. We demonstrate our technique by applying it to the practical measurements of a boost converter.

This paper is divided into the following sections: Section II will discuss the limitations of the current existing technique for measuring power losses. Section III will give a detailed description of the experimental setup and the measuring instruments. Proposed methodology for extracting $i_{CH}$ is presented in Section IV. The results and discussions are presented in Section V. Section VI will conclude and foreshadow potential future work.

**II. LIMITATIONS OF THE EXISTING POWER ANALYSIS TECHNIQUES**

In order to show the limitations of the existing technique for analysis of switching power loss, a typical boost converter utilizing a power MOSFET is selected and shown in Fig. 1.

**FIGURE 1.** Typical boost converter.

**FIGURE 2.** Measured switching waveforms of a power MOSFET while operating as the switch in the boost converter shown in Fig. 1; $V_{DS}$ is the measured drain-to-source voltage, $V_{GS}$ is the measured gate-to-source voltage, $I_D$ is the measured drain current flowing into the power MOSFET, $t_{ON}$, $t_{OFF}$, and $t_{CON}$ are the turn-On, turn-Off, and conduction intervals, respectively.

Fig. 2 shows the experimental switching waveforms measured across the power MOSFET for a single period.

According to the existing method, the power dissipated in a power MOSFET during switching intervals ($P_{SW}$) is obtained by integrating the product of the measured voltage ($V_{DS}$) and the measured current ($I_D$) [10]:

$$P_{SW} = f \int V_{DS}(t) \times I_D(t) dt$$

(1)

Here, $f$ represents the switching frequency and the integration is performed during the switching intervals, $t_{ON}$ and $t_{OFF}$. The turn-On losses ($P_{ON}$), and turn-Off losses ($P_{OFF}$) are shown in Fig. 3. Together, these constitute the switching losses ($P_{SW}$). Note that the $P_{OFF}$ losses are higher than $P_{ON}$ losses due to the charging of the inductor during the conduction period. Similarly, the conduction losses ($P_{CON}$) in a MOSFET (as depicted in Fig. 3) can also be calculated by (1) using $t_{CON}$ as the integration interval.

**FIGURE 3.** Power losses corresponding to the switching waveforms depicted in Fig. 2 for a single period.

Estimation of the switching losses in a power MOSFET using (1) is widely performed by many researchers and manufacturers [10]–[14]. However, with the advancement in MOSFETs for high voltage applications, it was realized that the effective output capacitance ($C_{OSS}$), which is defined as the sum of the gate-to-drain capacitance ($C_{GD}$) and the drain-
During the turn-Off interval, \( V_{DS} \) dissipates it in the channel of the MOSFET during the turn-On interval. Initial attempts to include the losses due to the channel of the MOSFET equivalent circuit while charging and discharging of the MOSFET. Hence, it is obvious that, during switching intervals depicted in Fig. 2, the measured drain current \( i_D \) is not equal to \( i_{CH} \).

Castro et al. [5] demonstrated the current displacement phenomenon in superjunction MOSFETs using a mixed-mode simulation approach. They developed an analytical model to obtain \( i_{CH} \) and used this current to determine the switching power losses:

\[
P_{SW} = \int v_{DS}(t) \times i_{CH}(t) dt
\]

Using (3), Castro et al. [5] found that the modification does not affect the total switching loss, but it redistributes the losses between \( P_{ON} \) and \( P_{OFF} \). They also showed that without the current displacement phenomenon, the \( P_{ON} \) and \( P_{OFF} \) losses were underestimated and overestimated by 25% and 200%, respectively [5]. Hence, it is quite evident from their results that the switching losses in a MOSFET should be obtained with \( i_{CH} \) rather than \( i_D \).

Two other groups [8], [9], have also estimated the switching loss by modeling \( i_{CH} \) for specific power MOSFETs and SiC transistors. However, in a real life scenario, \( i_{CH} \) flows inside a packaged MOSFET and cannot be directly measured, while calculating it by analytical modeling is time consuming and device-specific [5]–[9]. In Section IV, we aim to address these limitations by proposing a measurement method to extract \( i_{CH} \) for all types of transistors.

### III. EXPERIMENTAL SETUP

We have used the typical boost converter, shown in Fig. 1, to explain the new measurement method using real experimental data. The components we used for this boost converter are listed in Table 1. The converter is operated at a switching frequency of 50 kHz using an AFG1022 function generator. In order to measure the voltages \( v_{GS}(t_s) \) and \( v_{DS}(t_s) \) and the current \( i_D(t_s) \) with sufficient accuracy, probes and oscilloscopes of sufficient bandwidth must be used [19]. For this reason, a careful selection of the measurement setup was required, and is listed in Table 2. Note that the effect of parasitic capacitance of the probes on the measurements is negligible due to low operating switching frequency. Furthermore, MATLAB is used for processing the measured data.

### TABLE 1. Components of the boost converter.

| No. | Circuit Element | Value/Model |
|-----|----------------|-------------|
| 1.  | L              | 90.7 \( \mu \)H |
| 2.  | C              | 220 \( \mu \)F |
| 3.  | MOSFET         | IRF540      |
| 4.  | Diode          | SR310       |
| 5.  | \( R_S \)      | 10 \( \Omega \) |
| 6.  | \( R_L \)      | 50 \( \Omega \) |

The static \( I-V \) characteristics for the power MOSFET IRF540 were measured with Agilent Power Device Analyzer.
TABLE 2. Description of the measurement system.

| Part No. | Manufacturer | Description          | Bandwidth | Measured Signal |
|---------|--------------|----------------------|-----------|-----------------|
| DPO7104 | Tektronix    | Digital Phosphor Oscilloscope | 1 GHz     | -               |
| THDP0200| Tektronix    | Differential Probe    | 200 MHz   | $V_{DS}$ & $V_{GS}$ |
| TCP0030 | Tektronix    | Current Probe         | 120 MHz   | $I_D$           |

(B1505A) using four-point probe measurement. The setup to measure static $I$-$V$ characteristics is shown in Fig. 5 and will be explained in detail in the next section.

IV. PROPOSED METHOD

A. EXTRACTING $i_{CH}$ FOR TURN-ON INTERVAL

The MOSFET is operating as a switch in the boost converter and is in the turn-On mode when $V_{GS}$ is larger than the threshold voltage. As discussed in Section II, during the turn-On interval, $C_{OSS}$ discharges its energy into the channel of the MOSFET and is shown by the equivalent circuit in Fig. 6(a).

During the MOSFET turn-On operation, the instantaneous value of rising gate-to-source voltage, $V_{GS}(t_s)$, and falling drain-to-source voltage, $V_{DS}(t_s)$, can be measured by the setup described in the previous section. The measured results are shown in Fig. 6(b) where $t_s$ is the sample time at which the measurement is performed.

To explain the method of extracting the channel current $i_{CH}(t_s)$ from the measured drain current $i_D(t_s)$, we will focus on the specific sampling time $t_s = 0.46 \mu s$. At that instant of time, the measured voltage between the drain and the source is $V_{DS}(t_s) = 1.01$ V, the measured voltage between the gate and the source is $V_{GS}(t_s) = 4.07$ V, and the measured drain current is $I_D(t_s) = 0.27$ A, as shown in Fig. 6. Now we need to determine how much current $i_{COSS}(t_s)$ is supplied by $C_{OSS}$ and is discharged into the channel of the MOSFET at $t_s = 0.46 \mu s$. Due to the nonlinear voltage dependency of both $C_{DS}$ and $C_{GD}$, calculating the current flowing through the equivalent capacitance $C_{OSS} = C_{DS} + C_{GD}$ is quite challenging and unreliable. Hence, much better option is to determine the channel current $i_{CH}(t_s)$.

In order to extract $i_{CH}$ at the sample time $t_s = 0.46 \mu s$, the same MOSFET is taken out of the boost circuit and is measured at static condition using instruments described in Section III. While measuring the MOSFET in static conditions, the same bias voltages are applied to the MOSFET, which are $V_{DS} = V_{DS}(t_s) = 1.01$ V and $V_{GS} = V_{GS}(t_s) = 4.07$ V, as shown in Fig. 7(a). Traditionally, $I$–$V$ characteristics are measured by sweeping $V_{DS}$ from 0 to the required value, for set values of $V_{GS}$. However, device heating due to the continuous power dissipation could increase the temperature and impact the measured results. To avoid this issue, high grade instruments such as the Agilent Power Device Analyzer provide the option of pulsed $I$–$V$ measurements. An important feature for measuring static $I$–$V$ characteristics is that the measuring instrument takes some finite amount of time.
FIGURE 7. (a) MOSFET is set at static (DC) voltages $V_{GS}(t_s) = V_{GS} = 4.07$ V and $V_{DS}(t_s) = V_{DS} = 1.01$ V to measure the corresponding static (DC) current $I_{CH} = I_D$. (b) Pulsed I-V measurement using Agilent Power Device Analyzer with the transient settling time of 50 ms.

to settle down the transients, as illustrated in Fig. 7(b). In our example, when the bias voltages are pulsed to $V_{GS} = 4.07$ V and $V_{DS} = 1.01$ V, the Agilent Power Device Analyzer takes approximately 50 ms to settle down the transients before the drain current is measured.

In principle, $I_{CH}$ can be calculated by using a suitable model for the static current–voltage characteristics of the MOSFET. To illustrate this point, we can use the simple equation for a MOSFET in triode region [20]:

$$I_D = I_{CH} = \beta \left[(V_{GS} - V_T)V_{DS} - V_{DS}^2/2 \right] \quad (4)$$

To use this equation, we need to know the values of the threshold voltage ($V_T$) and the transconductance parameter ($\beta$) for the specific MOSFET that is used in the practical circuit. To enable circuit simulation, many manufacturers provide complex MOSFET models with extracted parameter values, but these models may not provide sufficiently precise match to the experimental I–V characteristics of specific MOSFETs. Therefore, static measurements of $I_{CH}$ are much more simple and reliable.

A MOSFET operating in a circuit has continuously changing voltages and currents, which results in a large number of sampling points. Therefore, it is quite impractical to manually measure the MOSFET static behavior at each of these sample points. In order to solve this issue the I–V characteristics of the power MOSFET IRF540 are measured with a small step size. In our example, the power MOSFET IRF540 was measured with the step size of 50 mV for $V_{GS}$ and $V_{DS}$. The points between the measured values were interpolated using spline interpolation in MATLAB, which did not cause errors because the measurements were performed with sufficiently small step size of 50 mV. Hence, the data collected from the measured I–V characteristics with such great resolution served as a lookup table to extract $i_{CH}(t_s)$ for corresponding $V_{GS}(t_s)$ and $V_{DS}(t_s)$ values during the entire turn-On interval. The obtained current $i_{CH}(t_s)$ is shown in Fig. 8. The difference $i_{CH}(t_s) - i_D(t_s)$ is equal to the current from the discharging capacitance $C_{OSS}$.

B. EXTRACTING $i_{CH}$ FOR TURN-OFF INTERVAL

As discussed in Section II and illustrated by the equivalent circuit in Fig. 9(a), $C_{OSS}$ is charged during the turn-Off interval. Again, the instantaneous value of the falling

FIGURE 8. The extracted $i_{CH}$ during turn-On interval is plotted alongside $V_{GS}$, $V_{DS}$, and $I_D$.
U. Jadli et al.: Measurement of Power Dissipation Due to Parasitic Capacitances of Power MOSFETs

FIGURE 9. (a) Equivalent circuit of the MOSFET operating in the boost circuit during the turn-Off interval, showing that \(i_D\) splits into \(i_{CH}\) and \(i_{COS}\). The values of the voltages and the current correspond to the sample time of \(-0.42\ \mu s\). (b) Switching waveforms of the MOSFET operating in the boost converter during the turn-Off interval (\(t_{\text{OFF}}\)).

gate-to-source voltage, \(v_{GS}(t_s)\), and the rising drain-to-source voltage, \(v_{DS}(t_s)\), can be directly measured by the setup described in Section III and the results are shown in Fig. 9(b), where \(t_s\) is the sample time at which the measurement is performed.

Taking as an example \(t_s = -0.42\ \mu s\), the measured voltage between the drain and the source is \(v_{DS}(t_s) = 2.02\ \text{V}\), the measured voltage between the gate and the source is \(v_{GS}(t_s) = 4.12\ \text{V}\), and the measured drain current is \(i_D(t_s) = 0.61\ \text{A}\), as shown in the Fig. 9. Analogously to the turn-On interval, we need to determine how much current \(i_{CH}(t_s)\) is flowing through the channel of the MOSFET at that instant of time. Just like it was done for the turn-On interval, we use the measured \(I-V\) characteristics of the MOSFET to obtain the current for the bias voltages of \(V_{DS} = v_{DS}(t_s) = 2.02\ \text{V}\) and \(V_{GS} = v_{GS}(t_s) = 4.12\ \text{V}\) and the result is \(i_D = i_{CH}(t_s = 0.42\ \mu s) = 0.42\ \text{A}\). Repeating this procedure, \(i_{CH}(t_s)\) can be obtained for the entire turn-Off interval, and the result is shown in Fig. 10.

The obtained results for both turn-On and turn-Off intervals are discussed in detail in the next section.

V. RESULTS AND DISCUSSION

The previous section clearly shows the effectiveness of the proposed method to extract \(i_{CH}\) during switching intervals. During turn-On interval, the extracted \(i_{CH}\) is larger than \(i_D\) because \(C_{OSS}\) is discharging into the channel of the MOSFET. During the turn-Off interval, the extracted \(i_{CH}\) was smaller than the \(i_D\), reflecting the fact that \(i_D\) is divided between \(i_{CH}\) and the current charging \(C_{OSS}\), i.e. \(i_{COS}\). This is consistent with the current displacement phenomenon discussed in Section II.

A. VALIDATION OF THE PROPOSED METHOD

To further validate the proposed method, we use the energy conservation principle. According to this principle, the estimation of energy loss by the MOSFET using the extracted \(i_{CH}\) should match the estimation by the prevailing calculation using \(i_D\). The only difference between these two approaches will be the distribution of power during the turn-On and turn-Off intervals. The turn-On (\(E_{\text{ON}}\)) and turn-Off (\(E_{\text{OFF}}\)) energy losses obtained by both methods are shown in TABLE 3. Both equations, (1) and (3), use the same integration limits. For \(E_{\text{ON}}\), the integration limits are defined from the start to the end of the falling \(v_{DS}\) waveform, as shown

![Figure 10. The extracted \(i_{CH}\) during turn-Off interval is plotted alongside \(v_{GS}, v_{DS},\) and \(i_D\).](image)

| Energy Losses | Calculated by \(\int v_{DS}(t) \times i_D(t)\)dt | Calculated by \(\int v_{DS}(t) \times i_{CH}(t)\)dt |
|---------------|---------------------------------------------|---------------------------------------------|
| \(E_{\text{ON}}\) | 0.30 \(\mu\)J | 0.51 \(\mu\)J |
| \(E_{\text{OFF}}\) | 1.00 \(\mu\)J | 0.74 \(\mu\)J |
| \(E_{\text{OFF}} = E_{\text{ON}} + E_{\text{OFF}}\) | 1.30 \(\mu\)J | 1.25 \(\mu\)J |

TABLE 3. Calculation of energy losses.
in Fig. 8. For $E_{OFF}$, the integration interval is from the start to the end of the rising $v_{DS}$ waveform, as shown in Fig. 10. It is clear from TABLE 3 that the total switching energy loss ($E_{SW}$) from both methods is quite similar. In other words, our method of using extracted $i_{CH}$ adheres to the energy conservation principle. There is a slight discrepancy, which is due to limited measurement accuracy.

We would like to provide further insight on the power distribution within MOSFET by plotting $P_{ON}$ and $P_{OFF}$ of IRF540 using both methods. The results are shown in Fig. 11. It is clear from this figure and the data in TABLE 3 that the existing method using $i_D$ underestimates the turn-On losses by 41.2% and overestimates the turn-Off losses by 35.1%. Castro et al. [5] documented similar finding on superjunction MOSFETs using analytical modeling. This percentage of energy loss distribution depends on both the voltage and the MOSFETs used. The usage of different MOSFETs will change $C_{OSS}$ and, hence, will change the energy loss distribution. Furthermore, $C_{OSS}$ of each MOSFET depends on the voltage across the MOSFET, which means the energy loss distribution for turn-On and turn-Off will be different for different voltages.

It is also worthwhile to note that the energy conservation principle holds only if the energy stored in the $C_{OSS}$ during turn–Off interval is being dissipated during the turn-On interval. At a particular voltage, using the fixed value of $C_{OSS}$ from the datasheet for calculating the stored energy can result in a huge error [21]. Hence, with the help of the extracted $i_{CH}$, it is quite easy to obtain the current $i_{OSS}$ flowing through the $C_{OSS}$ during the switching intervals, which is given as:

$$i_{OSS}(t) = |i_{CH}(t) - i_D(t)|$$

Here, the absolute sign in (5) is used to simplify the $C_{OSS}$ energy calculation. Using (5), the energy stored/dissipated by the $C_{OSS}$ can be calculated as:

$$E_{stored/dissipated} = \int v_{DS}(t) \times i_{OSS}(t) dt$$

TABLE 4 shows the energy that is stored and dissipated by $C_{OSS}$ of IRF540. We use the same integration limits to calculate the energy losses. It is evident from TABLE 4 that the conservation of energy is preserved and therefore supports the justification for removing the $C_{OSS}$ loss term from (2) as described by Xiong et al. [3]. A slight difference is credited to the limited measurement accuracy. The empirical results that are shown in TABLES 3 and 4 validate the proposed method.

**TABLE 4. Calculation of $C_{OSS}$ energy.**

| Energy | Value   |
|--------|---------|
| Stored in the $C_{OSS}$ | 0.26 $\mu$J |
| Dissipated by the $C_{OSS}$ | 0.22 $\mu$J |

**B. ENERGY DISSIPATION DURING THE CONDUCTION INTERVAL**

To obtain the total energy loss during the complete switching period $T = t_{ON} + t_{OFF} + t_{CON}$, we need to add the energy losses during the conduction interval. During the conduction interval the channel current is equal to the drain current flowing through the MOSFET. Hence, the conduction loss can be obtained using either current and is given by:

$$E_{CON} = \int v_{DS}(t) \times i_{CH}(t) dt = R_{DS(ON)} \int i_{CH}^2(t) dt$$

Here, $R_{DS(ON)}$ is the drain to source on-state resistance, which is generally provided by the manufacturers in the datasheets. For better power-conversion efficiency, the device manufacturers keep $R_{DS(ON)}$ to minimum so that the conduction losses of the MOSFET can be minimized.

As can be seen from (7), there are two options to estimate conduction losses. One from the measured $v_{DS}$ and $i_{CH}$ and another from the datasheet $R_{DS(ON)}$ and the measured $i_{CH}$. However, referring to Fig. 8 and Fig. 10, it is clearly noticeable that the extraction of $i_{CH}$ is only performed during $t_{ON}$ and $t_{OFF}$, and not during the $t_{CON}$. This is due to the low $R_{DS(ON)}$ of the IRF540 whose value is given in the datasheet as 77 m$\Omega$. Lower $R_{DS(ON)}$ results in very small drain to source voltage in the conduction region—in order of millivolts. Since the values of $v_{DS}$ are so small, the extraction of $i_{CH}$ is quite challenging due to the limited sensitivity of the differential probes. Moreover, if the measurement error of small $v_{DS}$ is large, it will eventually result in a large error in the extracted $i_{CH}$. Therefore, instead of measuring $v_{DS}$,
$R_{DS(on)}$ from the datasheet can be easily used to estimate conduction losses.

**C. IMPACT OF THE SWITCHING FREQUENCY ON THE ENERGY DISTRIBUTION**

From (1) and (3), it is clear that the switching loss in the switch is directly proportional to the switching frequency. Using the same boost configuration, we varied the operating frequency and the resulting distribution of energy losses by the MOSFET during turn-On and turn-Off intervals is shown in Fig. 12. It is evident that the error in estimating the distribution of energy losses during switching intervals is significant if the energy loss is calculated by $\int v_{DS} \times i_{DS} dt$. Although the total switching losses are the same, there are implications for the design of the control circuitry in terms of minimizing the switching losses. Furthermore, different switching strategies critically rely on the accurate estimation of the switching losses. Hence, the proposed method can be very helpful when designing converters with high efficiency.

![FIGURE 12. Energy losses distribution with increasing frequency.](image)

**VI. CONCLUSION**

The proposed experimental method to extract $i_{CH}$ inside MOSFETs is successfully demonstrated in order to calculate switching power loss due to the parasitic capacitances. The power dissipation measured by the proposed method is not affected by the voltage dependence of the parasitic capacitances. Hence, this versatile and facile method can be applied to any device, either in simulation or experiments. In this paper, we test it on IRF540 that is employed as a switch in a basic boost converter. For comparison, the energy losses in the device during switching were calculated using both the new and the existing method. This comparison demonstrated that the new method can accurately measure the distribution of energy loss during turn-On and turn-Off intervals. Furthermore, the new method can be used to determine accurately the energy stored in the MOSFET’s output capacitances. The results obtained by the proposed method are also compared to the existing method for different switching frequencies. The difference between the distributions of energy losses shows the importance of the proposed method when designing more efficient power circuits. Another implication of this finding is that circuit designers can use it to select the most suitable transistor for converter configurations at specific voltage and frequency.

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