Abstract
As its price per bit drops, SSD is increasingly becoming the default storage medium for cloud application databases. However, it has not become the preferred storage medium for key-value caches, even though SSD offers more than 10× lower price per bit and sufficient performance compared to DRAM. This is because key-value caches need to frequently insert, update and evict small objects. This causes excessive writes and erasures on flash storage, since flash only supports writes and erasures of large chunks of data. These excessive writes and erasures significantly shorten the lifetime of flash, rendering it impractical to use for key-value caches. We present Flashield, a hybrid key-value cache that uses DRAM as a “filter” to minimize writes to SSD. Flashield performs light-weight machine learning profiling to predict which objects are likely to be read frequently before getting updated; these objects, which are prime candidates to be stored on SSD, are written to SSD in large chunks sequentially. In order to efficiently utilize the cache’s available memory, we design a novel in-memory index for the variable-sized objects stored on flash that requires only 4 bytes per object in DRAM. We describe Flashield’s design and implementation and, we evaluate it on a real-world cache trace. Compared to state-of-the-art systems that suffer a write amplification of 2.5× or more, Flashield maintains a median write amplification of 0.5× without any loss of hit rate or throughput.

1 Introduction
Flash has an order of magnitude lower cost per bit of storage compared to DRAM. Consequently it has become the preferred storage medium for hot data that requires high throughput and low latency access. For example Google [24] and Facebook [20] use it for storing photos, and databases like LevelDB [3] and RocksDB [5] are deployed on top of flash.

However, flash is not used for key-value caches, an essential infrastructure tier for modern web scale applications. This is surprising because these caches are typically deployed in a dedicated remote cluster [21] or on a physically remote data center [4, 1]. As a result, all accesses incur a network access time of 100 µs or more, hence flash can provide essentially the same access latency as DRAM. Furthermore, since the performance of caches is primarily determined by the amount of memory capacity they provide [11, 10], and the cost per bit of SSD is more than 10× lower than DRAM, flash promises significant financial benefits compared to DRAM. Table 1 demonstrates the cost difference between DRAM-only cache and hybrid cache, both with 4.25 TB capacity. The total TCO difference would be even greater due to power costs, since flash consumes significantly lower power compared to DRAM.

The reason flash has not been adopted as a key-value cache is that cache workloads wear out flash drives very quickly. These workloads typically consist of small objects, some of which need to be frequently updated [21, 6]. But flash chips within SSDs can only be written a few thousand times per location over their lifetime. Further, SSDs suffer from write amplification (WA). That is, for each cache object write, several more bytes are written to the actual flash chips at the device level. The reason is that flash pages are physically grouped in large blocks. Pages must be erased before they can be overwritten, but that can only be done in the granularity of blocks. The result is that over time, these large blocks typically contain a mix of valid pages and pages whose contents have been invalidated. Any valid pages must be copied to other flash blocks before a block can be erased. This garbage collection process creates device-level write amplification (DLWA) that can increase the amount of data written to flash by orders of magnitude. Modern SSDs

| Hybrid cache | DRAM-only cache |
|--------------|----------------|
| Count | Cost | Count | Cost |
| Dell 2×10 core server with 256 GB DRAM | 1 | $7700 | 17 | $130,900 |
| Samsung 1 TB enterprise SSD | 4 | $4800 | 0 | 0 |
| Total | $12,500 | $130,900 |

Table 1: The cost of a hybrid SSD and DRAM cache server with combined capacity of 4.25 TB, versus the cost of multiple DRAM-only cache servers with the same aggregate capacity.
exacerbate this by striping many flash blocks together (512 MB worth or more) to increase sequential write performance ([2.1, [26]).

To minimize the number of flash writes, SSD storage systems are constrained to writing data in large contiguous chunks. This forces a second-order form of write amplification called cache level write amplification (CLWA). CLWA occurs when the cache is forced to re-locate objects to avoid DLWA. For example, when a hot object occupies the same flash block as many items that are ready for eviction, the cache faces a choice. It can evict the hot object with the cold objects, or it can rewrite the hot object as part of a new, large write. Therefore, in existing SSD cache designs, objects get re-written multiple times into flash. These challenges will become even greater over time, since it is projected that as flash density increases, its durability will continue to decrease [13].

We present Flashield, a design for a hybrid key-value cache that uses both DRAM and SSDs. Our contribution is a novel caching strategy that significantly extends the lifetime of SSDs such that it is comparable to DRAM by minimizing the number of writes to flash. Our main observation is that not all objects entering the cache are good candidates for placement in SSD. In particular, the cache should avoid writing objects to flash that will be updated or that will not be read in the near future. However, when objects first enter the cache, it does not know which objects are good candidates for SSD and which are not. Therefore, the key idea in Flashield’s design is that incoming objects into the cache always spend a period of time in DRAM, during which the cache learns whether they are good candidates for flash storage. If they indeed prove themselves as flash-worthy, Flashield will move them into flash. If not, they are never moved into flash, which minimizes the resulting write amplification. Since the flash layer is considerably larger than DRAM (e.g., 10× larger), objects moved to flash on average will remain in the cache much longer than those that stay in DRAM.

To dynamically decide which objects are flash-worthy under varying workloads, we implement the filtering algorithm using machine-learning based Support Vector Machine (SVM) classification. We train a different classifier for each application in the cache. To train the classifiers, we design a light-weight sampling technique that uniformly samples objects over time, collecting statistics about the number of past accesses and the time between accesses. The classifier is used to predict whether an object will be read more than t times in the future and determine its suitability to be stored in flash. We term this metric flashiness.

The second main idea in Flashield’s design is its novel DRAM-based lookup index for variable-length objects stored on flash that only requires less than 4 bytes of DRAM per object. Since the flash layer’s capacity is much larger than the DRAM’s, a native lookup index for objects stored on flash would consume the entire capacity of the DRAM. Our index consumes a relatively small amount of memory by not storing the location of the objects and their corresponding keys. Instead, for each object stored on flash, the index contains a pointer to a region in the flash where the object is stored, and it stores an additional 4 bits that specify a hash function on the object key that indicates the insertion point of the object in its region on flash. The index leverages bloom filters to indicate whether the object resides on flash or not without storing full keys in DRAM. On average, Flashield’s lookup index only requires 1.03 reads from the SSD to return an object stored on it.

We implement Flashield in C and evaluate its performance under a commercial trace. We show that compared with RIPQ [26], the state-of-the-art SSD key-value cache, Flashield reduces write amplification by a median of 5× and an average of 16×, while maintaining the same average hit rates. We show that when objects are read from SSD, Flashield’s read latency and throughput is close to the SSD’s latency and throughput, and when objects are written to the cache or read from DRAM, its latency and throughput are similar to that of DRAM-based caches.

This paper makes three main contributions:

1. Flashield is the first SSD storage system which uses DRAM as a filter for deciding which objects to insert into flash.
2. Flashield’s novel flash lookup index takes up less than 4 bytes per object in DRAM by not storing the direct location of objects and their keys.
3. Flashield is the first key-value cache that uses a machine-learning based algorithm and lightweight temporal sampling to predict which objects will be good candidates for flash.

As new generations of flash technology can tolerate even fewer writes [13], our dynamic admission control to flash can be extended to other systems beyond caches, such as flash databases and file systems.

2 The Problem

Building a cost-effective SSD-based cache requires solving two conflicting challenges. SSDs perform poorly and wear out quickly unless writes are large and sequential. The lifetime of an SSD is defined by flash device manufacturers as the amount of time before a device has a non-negligible probability of producing uncorrectable read errors. The lifetime of an SSD depends on several factors, including the number of writes and erasures (termed program-erase cycles), the average time between refresh
cycles of the SSD cells, the cell technology, the error correction code and more. The typical lifetime of a flash cell is between 3-5 years assuming it is written 3-5 times a day on average. This conflicts with the characteristics of cache workloads. Caches store small objects with highly variable lifetimes; this drives caches to prefer small random I/O for reads and writes which will wear flash drives out quickly.

The key metric that helps us track device wear is write amplification. Many write patterns force the SSD to perform additional writes to flash in order to reorganize data. The ratio of the bytes written to flash chips compared to the bytes sent to the SSD by the application is called write amplification (WA). A WA of 1.0 means each byte written by the application caused a one byte write to flash. A WA of 10.0 means each byte written by the application caused an extra 9 bytes of data to be reorganized and rewritten to flash.

2.1 Device-level Write Amplification

Device-level write amplification (DLWA) is write amplification that is caused by the internal reorganization of the SSD. The main source of DLWA comes from the size of the unit of flash reuse. Flash is read and written in small (~8 KB) pages. However, pages cannot be rewritten without first being erased. Erasure happens at a granularity of groups of several pages called blocks (~256 KB). The mismatch between the page size (or object sizes) and the erase unit size induces write amplification when the device is at high utilization.

For example, when an application overwrites the contents of a page, the SSD writes it to a different, fresh block and maintains a relocation mapping called the flash translation layer (FTL). The original block cannot be erased yet, because the other pages in the same block may still be live. When the flash chips are completely occupied, the SSD must erase blocks in order to make room for newly written pages. If there are no blocks where all of the pages have been superseded by more recently written data, then live pages from several blocks must be consolidated into a single flash block. This consolidation or garbage collection is the source of DLWA. If a device is at 90% occupancy, then its DLWA can be very high. Figure 1 measures this effect. It shows DLWA under sequential and random writes. The measurements were taken on a 480 GB Intel 535 Series SSD using SMART. For each data point, 4 TB of randomly generated data is written either randomly or sequentially to the raw logical block addresses of the device with varying buffer sizes. Specifically, in the random workload the logical block space is broken into contiguous fixed buffer-sized regions; each write overwrites one of the regions at random with a full buffer of random data. The sequential workload is circular; regions are overwritten in order of their logical block addresses, looping back to the start of the device as needed. For both patterns, we varied the space utilization of the device by limiting writes to a smaller portion of the device’s logical block addresses.

The results show that random, aligned 1 MB flash writes experience a nearly 8× DLWA. This is surprising, since flash erase blocks are smaller than 1 MB. The reason for this write amplification is because SSDs are increasingly optimized for high write bandwidth. Each flash package within an SSD is accessed via a relatively slow link (50-90 MB/s today); SSDs stripe large sequential writes across many flash packages in parallel to get high write bandwidth. This effectively fuses several erase blocks from several packages into one logical erase block. A 1 MB random write marks a large region of pages as ready for erase, but that region is striped across several erase units that still contain mostly live pages. Others have corroborated this effect as well [26].

There are two ways to combat this effect. The first is to write in units of $B \cdot W$ where $B$ is the erase block size and $W$ is how many blocks the SSD stripes writes across. Our results show that a cache would have to write in blocks of 512 MB in order to eliminate DLWA. The second approach is to write the device sequentially, in FIFO-order at all times. This works because each $B \cdot W$ written produces one completely empty $B \cdot W$ unit, even if writes are issued in units smaller than $B \cdot W$. Figure 1 shows that 8 MB sequential writes also eliminate DLWA.

This means our cache is extremely constrained in how it writes data to flash. To minimize DLWA the cache must write objects in large blocks or sequentially. In either case, this gives the cache little control on precisely which objects should be replaced on flash.

2.2 Cache-level Write Amplification

Writing to flash in large segments (contiguous chunks of data) is a necessary but not sufficient condition for minimizing the overall SSD write amplification. The main side effect of writing in large segments is cache-level write amplification (CLWA). CLWA occurs when objects that were removed from the SSD are re-written to it by the cache eviction policy. If the size of the seg-
The state-of-the-art system, RIPQ [26], an SSD-based photo caching system that caches large immutable objects, tries to minimize CLWA by inserting objects that were read \( k \) times in the past together. When objects are first inserted into the cache, they are buffered in memory, and periodically they are moved into flash together as a segment with other objects that have been read the same number of times. The idea is that objects that were read \( k \) times in the past might share a similar future eviction rank. For example, an object that was read once is stored on flash in the same segment with other objects that were read once. The rationale is that objects in the same segment will have a similar lifetime, so when it comes time to evict the segment, most of its objects will be cold and will not have to be re-written. In addition, segments that contain objects that have been read fewer times will be evicted faster than segments with objects that have been read many times.

In order to test this strategy, we simulated the CLWA of RIPQ (the implementation is not publicly available) with the Memcached trace, using a segmented LRU with 8 queues. We also compared it with a victim cache policy, a naïve approach where the SSD simply serves as an L2 cache (i.e., every object evicted from DRAM is written to SSD). This policy is used by TAO [7], Facebook’s graph data store, which leverages a limited amount of flash as a victim cache for data stored in DRAM. The simulation assigns the same amount of memory for each application in the trace, with a ratio of DRAM to SSD of 1:7. So for example, if an application was originally assigned 1 GB in the trace, the simulation would assign it a capacity of 128 MB of DRAM and 896 MB of SSD.

The results of the simulation are presented in Table 3. The results show that while RIPQ considerably improves upon victim cache, it still suffers from a very high CLWA. Note that the victim cache would suffer from an even greater total WA, because it also suffers from DLWA (since it does not write to flash in large segments). The reason RIPQ suffers from CLWA, is twofold. First and most importantly, RIPQ automatically writes all incoming objects to flash. Even objects that will never be read again or are frequently updated, will be written to flash. Second, when the frequency of reads of a certain object changes, it creates additional writes. For example, if an object was read twice over a period of time after it was written, it is grouped with other objects that were read twice on flash. However, if a burst occurred and it was read five more times, RIPQ needs to rewrite it to group it with other higher ranking objects. Since the objects are much smaller than the segment size, and there is a relatively high ratio of writes in the trace, RIPQ struggles to guarantee that objects that have been read around the same time will be stored in the same segment.

This example teaches us two lessons on how to minimize CLWA. First, not every object that is written by the application to the cache, should necessarily be stored
on SSD. For example, objects that are updated soon after
they are first written or objects that have a low likelihood
of being read in the future. However, the occurrence of
such objects varies widely across different applications.
For example, in some applications of the Memcached
trace, more than half of written objects are never read
again, and in some applications, a vast majority of ob-
jects are read many times and should be written to the
cache. Second, due to the disparity between the segment
size and the object size, it is difficult to guarantee that
objects that were similarly ranked by the eviction policy
will be stored in physically adjacent regions on SSD.

Both of these insights motivate us to design Flashield,
a cache that successfully minimizes CLWA.

3 Design

This section presents Flashield’s design. The design goal
is to minimize cache-level write amplification, while
maintaining the highest possible hit rate. Flashield is a
hybrid key-value cache that uses both SSD and DRAM.
The key insight of Flashield’s design is to use DRAM as
a filter, which prevents moving objects into flash that will
be soon thereafter evicted or updated.

Figure 3 illustrates the lifetime of an object in
Flashield. Objects are first always written to DRAM.
After the object is read for the first time, Flashield starts
collecting features that describe its performance. These
contain information about how many times and how fre-
quently the object has been accessed. At any point in
time during its duration in DRAM, an object may be
evicted by Flashield’s eviction algorithm. Periodically,
Flashield moves a segment (e.g., 512 MB) composed of
many DRAM objects into flash. Flashield utilizes a ma-
chine learning classifier to rank the objects based on their
features. If the object passes a rank threshold, it will be
considered as a candidate to move to flash. The candi-
dates to flash are then ranked based on their score, which
determines the order they are moved by Flashield into
flash. After it gets moved to flash, an object will live in
the cache for a relatively long duration. It will get moved
out of flash once its segment is erased from flash, in FIFO
order. At that point, the object will be evicted if it is low
in terms of eviction priority, or it will get re-inserted into
DRAM if it has a high eviction priority.

In Flashield, DRAM serves three purposes. First, it is
used as a filter to decide which objects should be inserted
into SSD. Second, it stores the metadata for looking up
objects on flash. Third, it serves as a caching layer for
objects before they are moved to SSD and for objects that
are not candidates for SSD. In the rest of this section, we
focus on the first and second roles of DRAM.

3.1 DRAM as a Filter

In Flashield, DRAM serves as a proving ground for mov-
ing objects into flash. When objects are first written into
DRAM, Flashield does not have any a-priori knowledge
whether they will be good candidates for flash. Further-
more, given the great diversity of applications that utilize
key-value caches, applications have varying access pat-
terns.

A strawman approach for determining which objects
are flash-worthy is to rank them based on simple met-
rics like time-to-last-access or access frequency, as done
by standard cache replacement polices like LRU or LFU.
However, simply ranking objects is insufficient, because
it is difficult to set a single threshold for flash-worthiness
that will work for all applications. For example, we can
set a threshold requiring that an object will be read more
than once before it enters flash. Such a threshold proves
too stringent for certain applications where the access
patterns are long and may cause excessive misses due
to premature evictions, and too lenient for other applica-
tions where many objects would be unnecessarily written
to flash.

Instead of using a one-size-fits-all approach, machine
learning can be used as a way to dynamically learn which
objects are a good fit for flash for each individual appli-
cation. In order to apply a machine learning classifier,
we need to define the metric we are trying to estimate
and the features that can predict the metric.

We define flashiness as a metric that predicts whether
an object will be a good fit for flash. An object that has a
high flashiness score is an object that meets two criteria.
First, it is an object that will be accessed several times in
the near future. This guarantees that it will not be evicted
by the cache’s eviction function. Second, it needs to be
immutable in the near future, since updating an object in
SSD requires an additional write and erasure.

Both of these criteria can be captured by predicting
the number of times an object will be read in the near fu-
ture (e.g., one hour), while it is stored on DRAM. If the
object is evicted or updated during this period, we only
count the number of reads until the object was evicted
or updated. Initially, we tried predicting this number using a logistic regression. We ran this classifier on a commercial Memcachier trace and found the prediction was highly inaccurate. After trying different features and classifiers, we found it is difficult to accurately predict how many times an object will be accessed in the future.

Therefore, instead of predicting the number of times an object will be accessed in the near future, Flashield uses a binary classifier, using Support Vector Machine (SVM), which predicts whether an object will be accessed more than \( n \) times in the near future. Table 4 provides the accuracy \( \frac{tp}{tp+fp} \), where \( tp \) is true positives and \( fp \) is false positives) and recall \( \frac{tp}{tp+fn} \), where \( fn \) is false negatives) for the classifier when it tries to predict whether an object will be accessed at least once in the future, using a training time of one day. Note that the accuracy varies widely across applications when the recall is 100%. This indicates that for certain applications (e.g., application 1), it is harder to accurately measure flashiness based on the history of requests than for other applications.

We experimented with several different features related to the number and frequency of object requests. Based on that, our design uses the following five features: number of past reads to the object, the average time between these reads, the time between the last two reads, the maximum time between subsequent reads and the time it took for the first read after the object was written.

Figure 4 depicts the relationship of these features with predicting whether an object will be accessed more than once in the next hour. It buckets the number of future hits in the Y axis, as a function of each feature on the X axis.

Note that the threshold \( n \), the number of times an object will be read in the future, can be used by the system to indicate how sensitive it is to write amplification. If the system is very sensitive to write amplification, it can set \( n \) to a relatively high number (e.g., 10 or 100), which will ensure that Flashield will only move objects into flash which it predicts will be read many times in the future. On the other hand, if the system is more sensitive to hit rate, \( n \) will be set as a low number (e.g., 1). In addition, Flashield allows the operator to set a fixed limit on the flash write rate to maintain a certain target lifetime (e.g., 5 years).

### 3.2 DRAM as an Index for Flash

The lookup indexes for flash and DRAM are both stored in memory. Since we use DRAM also as a filter, the design goal of the indexes is that they will consume a minimal amount of space on DRAM.

We decided to use an in-memory index for objects stored in flash for two reasons. First, since the index needs to be frequently updated, if it were stored in flash it would create significant write amplification. Second, storing the index in DRAM more than halves the latency, since otherwise, each lookup for a key would require an extra read from flash.

A naïve index would contain the identity of the keys stored in flash, the location of the values, and their position in an eviction queue. However, such an index would be prohibitively expensive. If we take an example of a 6 TB flash device with an average object size of 257 bytes (equal to the average object size of the top 20 applications in the Memcachier trace), storing a hash of the key for each object that avoids collisions requires at least 8 bytes, storing the exact location of each object would be 43 bits, and keeping a pointer to a position in a queue would be 4-8 bytes. Storing 17 bytes per object on DRAM would require 406 GB of DRAM. This would take up (or exceed) all of the DRAM of a high end server.

Instead, we design a novel in-memory lookup index for variable-sized objects with an overhead of less than 4 bytes per object. Rather than directly storing the location of the SSD object, the index has two separate fields: segment number and predefined hash function ID. The segment number points to a contiguous segment in flash where the object is stored. The output of the predefined hash function indicates the object location inside the segment. We chose to utilize 16 pre-defined hash functions since increasing the number of hash functions beyond that provided negligible improvement in the flash utilization. We explore the flash utilization in §5.3. Note that since data is written to flash sequentially, a segment sizes of 8 MB or larger achieves minimal DLWA. We use 512 MB segments in order to reduce the indexing overhead.

Flashfield does not store the identities of keys in the index but instead only stores them in the flash device, as part of the object. In order to identify hash collisions in the lookup table, Flashield compares the key from flash. To limit the number of flash reads during key lookup and avoid complex table expansions, the lookup table is a configurable multiple-choice hash table without chains. During lookup, pre-defined hash functions are used one by one, such that if the key is not found, the next hash

| App | Accuracy | Recall |
|-----|----------|--------|
| 1   | 39.0%    | 100.0% |
| 3   | 92.2%    | 100.0% |
| 19  | 95.3%    | 100.0% |
| 18  | 96.9%    | 100.0% |
| 20  | 77.6%    | 100.0% |

Table 4: Accuracy and recall of SVM classifier for predicting if an object will be accessed at least once in the future, for the top 5 applications in the Memcachier trace in terms of number of requests.
function is used. If all hash functions are used and the key was still not found then Flashield returns a miss. Similarly if a collision happens during insertion, the key is re-hashed with the next hash function to map it to another entry in the lookup table. If all hash functions are used and there is still a collision, the last collided object is evicted to make space for the new key.

To reduce the number of excess reads from the flash in case of hash collisions, Flashield utilizes an in-memory bloom filter for each segment, which indicates whether a key is stored in the segment. We decided to use a bloom filter per segment, rather than a global bloom filter, since each segment is immutable, which eliminates the need to support deletions. We use bloom filters with a false positive rate of 1%. For the Memcached trace, this translates to an average of 1.03 accesses to flash for every hit in the flash and an extra memory overhead of 10 bits per item. Figure 5 summarizes Flashield’s lookup process.

Instead of utilizing a full eviction queue with a linked list of pointers, Flashield uses the CLOCK algorithm [12]. To evaluate this design choice, we ran the top 5 applications in the Memcached trace in a simulation and compared the results between the CLOCK algorithm and LRU. The results show that while CLOCK slightly decreases the overall hit rate, the overall effect is negligible. The results led to us to assign only 2 index bits for the CLOCK algorithm. We describe the CLOCK algorithm in §4.3.

The hashtable entry format is summarized in Figure 6. The index contains an extra bit that indicates whether the object is scheduled for deletion from flash (§4).

4 Implementation

This section presents the implementation details of Flashield. We implemented Flashield in C. Most of the cache functionality was implemented from scratch, except for the transport, dispatch, request processing, and the hash table for DRAM objects, which are borrowed...
from Memcached 1.4.15. Flashield has four main functions: reads, writes, moving data to flash and eviction. Figure 7 depicts the high level components of Flashield’s architecture.

For incoming reads, Flashield first checks whether the object exists in the hash table for DRAM objects, which is based on Memcached’s hash table. If not, it checks whether the object exists in flash using a separate hash table for flash objects. If the object exists either in DRAM or flash, Flashield returns it, otherwise the request is counted as a miss. Incoming writes and updates are always written first into DRAM. In the case of updates, the updated object is written in to DRAM, and the old version is invalidated. Flashield maintains free space in the size of a segment (e.g. 512 MB) in DRAM for incoming writes.

Flashield uses a configurable number of worker threads that process the client requests in parallel. To maintain enough free space on DRAM, Flashield utilizes a dedicated cleaner thread. The cleaner works in the background, and is not part of the critical path for requests. When the free space on DRAM drops below a segment size, if there are enough objects that meet a threshold for their flashiness score and the flash write rate limit was not reached, the cleaner will buffer them into a segment and move them into flash. Objects are moved to flash in an order based on their flashiness score. When the SSD is full, the cleaner will remove the last segment from flash based on FIFO order.

For eviction, Flashield maintains a global priority rank for all objects, whether they are stored in DRAM or flash. Objects are evicted from Flashield based on this global priority. By default the priority is an approximation of LRU. If the next object for eviction is in DRAM, Flashield simply evicts it. If the next object for eviction is in flash, Flashield marks it as a ghost object, and it will be evicted when its segment is removed from flash. Note that the movement of data from DRAM into flash is decoupled from eviction. They are conducted in parallel and use different metrics to rank objects. Objects that are moved between the flash and DRAM always keep their global priority ranking. When there are not enough objects in DRAM that meet a threshold for their flashiness score, or the flash write rate limit is reached, the cleaner will buffer them into a segment and use different metrics to rank objects. Objects that are evicted from Flashield based on this group based on their size. Larger objects go first, because they require more contiguous space than smaller objects. In this process, some objects will not have available space in the segment. Flashield skips these objects and tries to insert them again next time it creates a new segment. We evaluate the resulting segment utilization in Section 5.3.

4.2 Classifier Implementation

Flashield’s flashiness score is computed based on five features for each object, which track information about its past hits. Since these features depend on information across multiple object accesses, the features for an object are only generated after an object has been read at least once. If an object has never been read, its flashiness score is automatically equal to zero.

Flashield periodically trains a separate classifier for each application. For the week-long commercial traces we used, we found that a training period of one day at the beginning of the trace was sufficient for classifying flashiness for the whole week.

The naïve way to train the classifier would be to update the features at each access to the DRAM. However, this approach may oversample certain objects, which can create an unbalanced classifier. For example, if a small set of objects account for 99% of all accesses, multiple sets of features would be created for these objects, and the flashiness estimation would be biased towards popular objects.

To tackle this problem, we implemented a sampling technique that generates a single sample for each object, chosen uniformly over all of its accesses during the training period. Instead of updating the features at each object access, with do it only with a probability of 1/n, where n is the number of times the object was read so far.

To illustrate this sampling technique, consider the following example. Suppose an object was written in time $t = 0$ and read for the first time at $t = 1$. Its features vector will be: $[1, 1, 1, 1, 1]$ (number of past reads, average time between reads, time between last two reads, maximum time between subsequent reads, time of first read).

Since the number of reads is equal to 1, the feature vector generated by its first read will be the feature we use for training at a probability of 1. If a second read arrives at $t = 1.5$, then the features after the second read will be: $[2, 0.75, 0.5, 1, 1]$. Flashield will keep the second set of features with a probability of 1/2, since the number of reads is equal to 2. This is equal to uniformly sampling the features from the first or second access. Each subsequent access will be sampled at a uniform probability of
1/n, and the probability of prior accesses to be sampled will also be uniform.

After collecting the samples for a day, we measure the number of times each of the objects is hit in the subsequent hour. This number is used as the target function for the training. After these two periods, Flashield trains the classifier using these training samples and labels.

4.3 Eviction

Flashield utilizes the CLOCK algorithm to rank objects for eviction. Each object has two bits in its hash table entry that signify priority. In order to approximate LRU, when the object is read, its bits are all set to 1. MFU (Most Frequently Used) is approximated by incrementing the bits by 1 at each read.

Each time it needs to free up space, Flashield walks through all the object entries in round-robin order and decrements their CLOCK entries. It stops decrementing the entries once it reaches an object that has a CLOCK entry equal to zero, which is the next object for eviction. If the next object for eviction is in DRAM, it is simply deleted. If the object is in flash, it cannot evict it immediately, since erasing a small amount of data from flash creates write amplification. Instead, it is marked as ghost object which means it is scheduled for eviction once its segment is removed from flash.

Flashield approximates which objects are at the top of the global eviction rank (including flash and DRAM). These objects are defined as hot objects. It maintains a hot data threshold to approximate the amount of hot data in the cache. If the amount of hot data exceeds the hot data threshold, Flashield triggers an eviction to reduce it.

The hot data threshold (HDT) is computed by:

\[ HDT = DRAM + SSD \cdot hot \]

Where DRAM is the available capacity of DRAM excluding the lookup table and free space needed for incoming writes and for buffering data into flash. SSD is the total size of the SSD, and hot is the percentage of objects on flash that are not ghosts. By default, hot is set to 70%, which means that approximately 30% of the objects on flash are ghost objects.

Ghost objects can still be accessed after they were marked as ghosts, since they are not immediately removed from flash. If a ghost object is accessed, we mark it as a hot object (we set the ghost bit to zero). As a result if the amount of hot data exceeds the hot data threshold, Flashield will do a round of decrementing the hash table CLOCK bits, until it finds a sufficient number of flash objects with CLOCK bits of zero, which can be marked as ghosts. Note that in this case, we do not evict low ranking objects from DRAM, but only mark flash objects as ghosts. We do this in order to avoid evicting an object from DRAM after a flash read, which could cause the DRAM to be underutilized. Therefore, objects from

| App | Flashield 1 Hit % | Flashield 10 Hit % | Flashield 100 Hit % | RIPQ Hit % | RIPQ Hit % | RIPQ CLWA | Victim Cache Hit % | Victim Cache CLWA |
|-----|------------------|--------------------|---------------------|-----------|-----------|-----------|---------------------|------------------|
| 2   | 98.8%            | 90.0%              | 88.9%               | 99.5%     | 99.5%     | 99.6%     | 99.6%               | 99.6%            |
| 7   | 98.6%            | 90.0%              | 88.9%               | 99.5%     | 99.5%     | 99.6%     | 99.6%               | 99.6%            |
| 10  | 83.1%            | 83.1%              | 83.1%               | 99.5%     | 99.5%     | 99.6%     | 99.6%               | 99.6%            |
| 20  | 98.1%            | 90.0%              | 88.9%               | 99.5%     | 99.5%     | 99.6%     | 99.6%               | 99.6%            |
| 23  | 96.0%            | 90.0%              | 88.9%               | 99.5%     | 99.5%     | 99.6%     | 99.6%               | 99.6%            |
| 29  | 90.1%            | 90.0%              | 88.9%               | 99.5%     | 99.5%     | 99.6%     | 99.6%               | 99.6%            |
| 31  | 97.3%            | 90.0%              | 88.9%               | 99.5%     | 99.5%     | 99.6%     | 99.6%               | 99.6%            |

Table 6: Hit rates and CLWA of Flashield using a threshold of one read future read, RIPQ and victim cache.

| App | Flashield 1 Hit % | Flashield 10 Hit % | Flashield 100 Hit % | RIPQ Hit % | RIPQ Hit % | RIPQ CLWA | Victim Cache Hit % | Victim Cache CLWA |
|-----|------------------|--------------------|---------------------|-----------|-----------|-----------|---------------------|------------------|
| 2   | 98.8%            | 90.0%              | 88.9%               | 99.5%     | 99.5%     | 99.6%     | 99.6%               | 99.6%            |
| 7   | 98.6%            | 90.0%              | 88.9%               | 99.5%     | 99.5%     | 99.6%     | 99.6%               | 99.6%            |
| 10  | 83.1%            | 83.1%              | 83.1%               | 99.5%     | 99.5%     | 99.6%     | 99.6%               | 99.6%            |
| 20  | 98.1%            | 90.0%              | 88.9%               | 99.5%     | 99.5%     | 99.6%     | 99.6%               | 99.6%            |
| 23  | 96.0%            | 90.0%              | 88.9%               | 99.5%     | 99.5%     | 99.6%     | 99.6%               | 99.6%            |
| 29  | 90.1%            | 90.0%              | 88.9%               | 99.5%     | 99.5%     | 99.6%     | 99.6%               | 99.6%            |
| 31  | 97.3%            | 90.0%              | 88.9%               | 99.5%     | 99.5%     | 99.6%     | 99.6%               | 99.6%            |

Table 7: Hit rates and CLWA of Flashield using a flashiness prediction threshold of 1, 10 and 100 future reads.

DRAM only get evicted due to incoming writes.

5 Evaluation

In this section we evaluate the end-to-end performance of Flashield compared to existing systems using the Memcachier traces, measure its performance using a synthetic microbenchmark, and evaluate the effects of individual trade-offs we made in its design.

5.1 End-to-end Performance

We compare the end-to-end hit rate and write amplification of Flashield to RIPQ and the victim cache policy, by re-running applications from the Memcachier traces against a simulation of the three systems. Each one of the policies uses the same amount of memory that was allocated in the Memcachier trace, with a ratio of 1:7:1 doubling of DRAM and SSD. We run Flashield with a threshold of one future read. In other words, objects that are predicted to have at least one future read are deemed sufficiently flash-worthy. Since Flashield utilizes a separate SVM for each application, we compare the results of individual applications. To simulate RIPQ with 8 insertion points, and therefore at least 8 different segments on flash, we only run the simulation with applications that were allocated a sufficient amount of memory by Memcachier.

Table 6 presents the results of running the simulation against these applications. The results show that Flashield achieves significantly lower CLWA than RIPQ and victim cache. The median CLWA of Flashield is 0.54, the median of RIPQ is 2.85 and the median of victim cache is 3.67. Even though Flashield uses a low threshold for flashiness of one future read, it still prevents
a large number of writes that are not a good fit for SSD from being written to flash. Flashield and RIPQ have an almost identical hit rate. Both have a lower hit rate than victim cache, but victim cache suffers from significantly higher CLWA (and much higher overall WA due to its DLWA).

Table 7 compares Flashield with different flashiness prediction thresholds. While the results vary from application to application, generally speaking, the higher the threshold the lower the WA and the lower the hit rate. Note that in some applications, such as in application 2, this trade off does not hold, since we train the classifier individually on each application, and each application performs differently.

Table 8 depicts the results when we vary the ratio of DRAM and SSD, while keeping the total amount of memory constant for each application. The results show that if we reduce the amount of DRAM too much, the hit rate drops. This is due to the fact that when the DRAM is low, objects do not have enough time to prove themselves as flashy enough to be moved to SSD. Note that we used a smaller segment size in these runs, in order to display results for a 1:15 ratio of DRAM.

### 5.2 Microbenchmarks

In the case of both Memcached and Facebook, Memcached is not CPU bound, but rather memory capacity bound [11]. Since the Memcached traces are fairly sparse in terms of their rate of requests, we ran a set of synthetic microbenchmarks to stress the performance of the system to measure its throughput and latency.

Our microbenchmarks run on 4-core 3.4 GHz Intel Xeon E3-1230 v5 (with 8 total hardware threads), 32 GB of DDR4 DRAM at 2133 MHz with a 480 GB Intel 535 Series SSD. All experiments are compiled and run using the stock kernel, compiler, and libraries on Debian 8.4 AMD64. The microbenchmark requests are based on sequential keys, with the average object size as Memcached. We disabled the operating system buffer cache to guarantee that SSD reads are routed directly to the SSD drive. Since the performance of SSD and DRAM is an order of magnitude different, we separately measured SSD and DRAM hits. Finally, we measured the latency and throughput of Memcached 1.4.15 as a baseline.

Table 9 presents the throughput and latency of the microbenchmark experiment. The latency and throughput of DRAM hits in Flashield are very similar to the latency and throughput of Memcached. While the average latency of SSD hits is significantly higher than DRAM, their latencies become similar when deploying over the network (network access times are typically 100 µs or more). The miss latency of Flashield is similar to the latency of DRAM hits, because all of Flashield’s lookup indices are stored in DRAM, and the only case it needs to access flash in a miss is when one of the in-memory bloom filters returns a false positive. The write throughput and latency of Flashield were identical to Memcached, because writes always enter Flashield’s DRAM.

### 5.3 Utilization on Flash

When moving data from DRAM to flash, Flashield tries to allocate space for objects in different possible insertion points in the flash segment, using pre-defined hash functions. If no space is found for the object, Flashield skips the object and will try to insert it next time it moves a segment to flash.

Figure 8 depicts the utilization of Flashield’s flash allocation algorithm. To measure the utilization, we ran Flashield’s allocation algorithm on the Memcached trace with different number of hash functions over a segment size of 512 MB. The allocation greedily tries to allocate space to more data and measures the resulting utilization. Note that after the segment reaches about 60% utilization, its utilization curve gradient decreases, since when Flashield tries to allocate objects there is a higher proba-
bility of collisions with other existing objects in the segment. Using 16 hash functions, it takes about 1 GB of objects to reach a 99% utilization, and on average each object needs to be hashed 8.2 times until it finds an insertion point with enough space.

6 Related Work

There are several systems that try to extend the lifetime of flash for the purpose of a key value cache.

6.1 SSD-based Key Value Caches

RIPQ [26], Facebook’s photo cache, reduces write amplification by buffering data in memory before writing to flash, and by co-locating similarly prioritized content on flash. However, RIPQ suffers from more than 5× higher write amplification than Flashield. This is due to two main reasons. First, in RIPQ all content is written to flash. In contrast, by using DRAM as a filter for objects that are frequently updated or never accessed, Flashield significantly reduces the number of writes to flash. Second, since RIPQ constantly co-locates objects with similar priorities in flash, it frequently rewrites the same objects into flash. In addition, TAO [7], Facebook’s graph data store, uses a limited amount of flash as a victim cache for data stored in DRAM. Therefore, it suffers from a high rate of writes, because items which are not frequently accessed are written into flash.

A couple of systems try to support SSD-based caches by modifying the SSD’s Flash Translation Layer (FTL). Duracache [18] tries to extend the life of the SSD cache, by dynamically increasing the flash device’s error correction capabilities. This requires at the minimum modifying the FTL, and in order to achieve high performance it would require to modify the ASIC itself. Shen et al [25] allow the cache to directly map keys to the device itself, and remove the overhead of the flash garbage collector. Unlike both of these systems, Flashield does not require any changes in the flash device, and addresses the main cause of write amplification in caches, which is cache-level write amplification.

In addition, there are several systems that utilize Flash as a block-level cache for disk storage [15, 14, 23, 22, 2, 28]. In particular, Pannier [15] and Nitro [14] are block-level caches that reduce write amplification by caching objects that are read frequently and updated infrequently. However, unlike Flashield, they do not utilize DRAM as a filter for SSD to further reduce write amplification.

Cheng et al [9] present an offline analysis of the trade-off between write amplification and eviction policies in block-level caches. They generalize Belady’s MIN algorithm to flash-based caches, and demonstrate that LRU-based eviction is still far from their proposed optimal oracle eviction policy. However, they do not provide an online algorithm and an implementation that reduces write amplification of SSD-based caches.

6.2 SSD-based Key Value Stores

There are many key-value storage systems designed for SSD. These are typically not suitable for the cache use case, since they incur high levels of write amplification.

For example, LevelDB [3] and RocksDB [5] are key-value stores based on Bigtable [8] that are frequently deployed on SSD devices. Both of these stores incur a write amplification of more than 3× (and even as high as 10× or more) [16, 19, 27], because they use Log-structure Merge-trees (LSM), and incur an additional write each time an object moves to a new level.

WiscKey [19] improves the performance and write amplification of LevelDB by only sorting the keys, without sorting the values in the log. Even though it significantly reduces the write amplification of LevelDB, it still suffers from up to 4-5× write amplification when the workload contains small values. Similarly, LSMtree [27] also improves the performance and write amplification of LevelDB by leveraging a trie to make compaction more efficient. However, it still suffers from a write amplification of up to 5×, and requires two accesses to flash for each read from flash.

SILT [17] is a flash database that minimizes the index stored in memory, by utilizing space efficient indexing techniques, like cuckoo hashing and entropy-coded tries. We were inspired by some of these techniques in the design of Flashield’s flash index. However, unlike Flashield, SILT is not optimized for write amplification: in order to compress the in-memory index, each object is written more than twice on flash, and up to 20 times under certain workloads [27]. In addition, unlike Flashield, SILT assumes fixed sized objects.

7 Conclusions

SSD faces unique challenges to its adoption as a key-value cache, since the small object sizes and the frequent rate of evictions and updates creates excessive writes and erasures on flash storage. We presented Flashield, the first key-value cache that uses DRAM as a filter for objects that are not ideal for SSD. Our main insight was that many of the objects written to key-value caches are never read and frequently updated, and can be filtered dynamically. Flashield profiles objects using light-weight machine learning, and dynamically learns and predicts which objects are the best fit for flash storage. To efficiently utilize the DRAM both as a filter and as a cache, we designed a novel in-memory index that supports variable objects with an overhead of less than 4 bytes per object. We implemented Flashield, and showed that it reduces write amplification to a median of 0.5 compared to existing systems, which suffer from 5× more write amplification, and much shorter SSD lifetimes.
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