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Design Optimization of Double-Gate Isosceles Trapezoid Tunnel Field-Effect Transistor (DGIT-TFET)

Hwa Young Gu and Sangwan Kim *

Department of Electrical and Computer Engineering, Ajou University, Suwon 16499, Korea; dogn1006@ajou.ac.kr
* Correspondence: sangwan@ajou.ac.kr

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Abstract: Recently, tunnel field-effect transistors (TFETs) have been regarded as next-generation ultra-low-power semiconductor devices. To commercialize the TFETs, however, it is necessary to improve an on-state current caused by tunnel-junction resistance and to suppress a leakage current from ambipolar current ($I_{AMB}$). In this paper, we suggest a novel TFET which features double gate, vertical, and trapezoid isosceles channel structure to solve the above-mentioned technical issues. The device design is optimized by examining its electrical characteristics with the help of technology computer-aided design (TCAD) simulation. As a result, double-gate isosceles trapezoid (DGIT) TFET shows a much better performance than the conventional TFET in terms of ON-state current ($I_{ON}$), $I_{AMB}$, and gate-to-drain capacitance ($C_{GD}$). It is confirmed that an inverter composed of DGIT-TFETs can operate with less than 1 ns intrinsic delay time and negligible voltage overshoot.

Keywords: tunnel field-effect transistors (TFETs); ambipolar current; scaling; subthreshold swing; FinFET

1. Introduction

Over the past several decades, complementary metal-oxide-semiconductor (CMOS) technologies have been scaled down to improve integration densities and performance [1–3]. As the integration density increases, however, the increase of power consumption becomes an emerging main concern. Since the power dissipation is proportional to the square of supply voltage ($V_{DD}$), future CMOS devices should be operating with low $V_{DD}$. However, MOS field-effect transistors (MOSFETs) have a limit of 60 mV/dec subthreshold swing ($S$) at room temperature because they are based on a thermionic carrier injection. As a result, it is fundamentally impossible to lower $V_{DD}$ maintaining a high on-off current ratio ($I_{ON}/I_{OFF}$) [4]. Therefore, a sharp-switching device, based on a novel operating mechanism, is needed to achieve sub-60 mV/dec-S, and hence ultra-low power operation. Recently, tunnel FETs (TFETs) have been extensively investigated as one of the promising candidates for a next-generation low-power logic element [5–11]. Because TFETs inject charges through a band-to-band tunneling (BTBT) mechanism from a source to a channel, abrupt switching is possible compared to conventional MOSFETs with drastically reduced $I_{OFF}$ [12–14]. In addition, they are able to inherit MOSFETs technologies with minimum cost and maximum efficiency with the help of similar structure and process to MOSFETs used in current CMOS technologies [15].

However, TFETs have some technical challenges to be solved for succeeding or alternating MOSFETs. First, they suffer from a low-level $I_{ON}$ and a worse $S$ than expectation due to a high tunnel resistance [16]. A multi-gate structure and a narrow bandgap material (e.g., SiGe or Ge) are regarded as promising strategies to address the above-mentioned issues by improving gate controllability and BTBT efficiency [16–18]. In addition, heterojunction is preferred to suppress the $I_{OFF}$ caused by Shockley-Read-Hole (SRH) recombination, which is exponentially increased in narrow band-gap...
materials [19]. However, in case of a conventional lateral-channel structure, there is a process capability issue for forming SiGe-Si heterojunction [20], with abrupt doping profile aligning with gate.

The second technical challenge is ambipolar current ($I_{AMB}$), which is attributed to the BTBT at the channel-to-drain junction and causes a conduction of current during both positive and negative gate voltages ($V_{GS}$) [21]. Lowering a drain doping concentration ($N_D$) and introducing an underlap between gate and drain have been studied to address it [22,23]. Because TFETs have low-level driving currents, the effect of increasing resistance (e.g., drain resistance and contact resistance), due to a lightly doped drain, is negligible. However, if the driving current of TFETs is eventually improved, it will not be an ultimate solution because it will act as a new bottleneck in current drivability [24]. Similarly, the length of drain underlap region (DU) should be minimized since it increases parasitic resistance and degrades integration density.

Therefore, in this paper, a new structure TFET is proposed to address the abovementioned issues (i.e., $I_{ON}$, $I_{OFF}$, and $S$), simultaneously. In addition, its electrical characteristics are analyzed and optimized using technology computer-aided design (TCAD) simulation [25]. This paper is organized as follows: In Section 2, the key features of device design, and the parameters used in TCAD, simulation are described. In Section 3, the device design is optimized in terms of direct current (DC) and alternating current (AC) characteristics, depending on the several design parameters. Finally, the results are summarized and concluded in Section 4.

2. Double-Gate Isosceles Trapezoid TFET (DGIT-TFET)

Figure 1 shows a structure of double-gate isosceles trapezoid TFET (DGIT-TFET) studied in this work. It adopts a double-gate (DG) structure to enhance gate controllability over the channel. It features a vertical channel structure, in which the source and drain are located at a narrow top, and relatively thick bottom regions, respectively. The vertical structure is advantageous, not only for increasing the integration density without any areal penalty, but also for adopting a selective epitaxial layer growth (SEG) technique to improve $I_{ON}/I_{OFF}$ with the help of heterojunction [26]. In this study, the Si$_{1-x}$Ge$_x$-channel is overlapped with the gate by 15 nm considering the process margin in SEG process (Figure 1). It is also helpful to improve the $I_{ON}$ further by using pseudo-direct BTBT when the Ge mole fraction is increased [16,18,27]. The channel length ($L_{CH}$) is set by 30 nm to exclude short-channel effects and equivalent gate oxide thickness ($T_{OX}$) is set by 0.5 nm assuming high-k dielectric. The other important design parameters are summarized in Table 1, unless otherwise noted [28]. The electrical characteristics of DGIT-TFET, depending on the design parameters are investigated, and analyzed using Synopsys Sentaurus™ (Synopsys, Mountain View, CA, USA) [25]. For a rigorous examination, Shockley-Read-Hall (SRH) and dynamic non-local BTBT models are used after calibration. In detail, $A$ and $B$ parameters in Kane’s model is changed as in [18], to consider both indirect and direct BTBT components, simultaneously. The modified local density approximation (MLDA) model is also used for the consideration of quantum effect.
A bulk-Si substrate can alternate the SOI with the help of vertical structure of DGIT-TFET. The sequential in-situ, doped epitaxial growths are performed for channel (i.e., lightly doped p-Si and Ge layers) and source (i.e., highly doped p+ Ge layer) (c). After patterning tapered structure, conventional shallow trench isolation (STI) process is performed by oxide gap-fill, chemical mechanical polishing (CMP), and STI wet-etching processes in sequence (d). The length of DU can simply be adjusted by changing STI-oxide wet-etching time. After dopant activation, atomic layer deposition (ALD) for high-k gate oxide is followed by metal gate deposition (e). Finally, double-gates are formed by side-wall spacer technique, with an appropriate over-etching, to avoid gate-to-source overlap (f). The back-end-of-line (BEOL) processes are not shown here, since the conventional techniques are applicable.

Table 1. Parameters of double-gate isosceles trapezoid (DGIT-TFET) using technology computer-aided design (TCAD) simulation.

| Abbreviations | Definitions                        | Values                      |
|---------------|------------------------------------|-----------------------------|
| \( N_S \)     | source doping concentration         | Boron, \( 1 \times 10^{20} \) \( \text{cm}^{-3} \) |
| \( N_B \)     | channel doping concentration        | Boron, \( 1 \times 10^{17} \) \( \text{cm}^{-3} \) |
| \( N_D \)     | drain doping concentration          | Arsenic, \( 1 \times 10^{20} \) \( \text{cm}^{-3} \) |
| \( L_{CH} \)  | channel length                      | 30 nm                       |
| \( L_S = L_D \)| charge neutral region length        | 20 nm                       |
| \( T_{OX} \)  | equivalent gate oxide thickness    | 0.5 nm                      |
| \( T_S \)     | source region thickness             | 5 nm                        |
| \( T_D \)     | drain region thickness              | 20 nm                       |
| \( V_{DS} \)  | drain voltage                       | 1 V                         |
| \( \phi_m \)  | gate work function                 | 4.0 eV                      |

The \( n \)-channel DGIT-TFET can be fabricated by the process flow, shown in Figure 2. Starting with a silicon-on-insulator (SOI) wafer (a) drain region is formed by arsenic (As) ion implantation (b). A bulk-Si substrate can alternate the SOI with the help of vertical structure of DGIT-TFET. The sequential in-situ, doped epitaxial growths are performed for channel (i.e., lightly doped p-Si and Ge layers) and source (i.e., highly doped p+ Ge layer) (c). After patterning tapered structure, conventional shallow trench isolation (STI) process is performed by oxide gap-fill, chemical mechanical polishing (CMP), and STI wet-etching processes in sequence (d). The length of DU can simply be adjusted by changing STI-oxide wet-etching time. After dopant activation, atomic layer deposition (ALD) for high-k gate oxide is followed by metal gate deposition (e). Finally, double-gates are formed by side-wall spacer technique, with an appropriate over-etching, to avoid gate-to-source overlap (f). The back-end-of-line (BEOL) processes are not shown here, since the conventional techniques are applicable.
In order to estimate the effect of asymmetric body thickness ($T_B$) in DGIT-TFET (i.e., thin source and thick drain) on its electrical characteristics, drain current ($I_D$) as a function of $V_{GS}$ with different $T_B$ are examined in the conventional DG-TFET structure (Figure 3a). The simulation results show that the $I_{ON}$ and $S$ are improved as $T_B$ becomes thinner (Figure 3b). It is attributed to the improved gate controllability over the channel, which is confirmed by the increase in electric field at source-to-channel junction as $T_B$ decreases (Figure 3c). Unfortunately, there is a drawback that the $I_{AMB}$ is also increased with the thinner $T_B$ since tunnel barrier width ($W_{TUN}$) at channel-to-drain junction is decreased as well (Figure 3d). On the other hand, it is expected that the DGIT-TFET’s asymmetric source/drain thicknesses will allow it to achieve high $I_{ON}$ and low $I_{OFF}$, simultaneously.
3. Design Optimization of DGIT-TFET

Figure 4a shows the transfer characteristics of DGIT-TFET by changing the drain thickness \((T_D)\) from 5 to 50 nm, while the source thickness \((T_S)\) is fixed at 5 nm considering process capability and compatibility with sub-7 nm technology node [29]. In case of 5 nm-thick \(T_D\), DGIT-TFET is identical to the conventional DG-TFET in Figure 3a,b which shows improved \(I_{ON}\) but suffers from \(I_{AMB}\). On the other hand, it is clear that DGIT-TFET can suppress \(I_{AMB}\), without any \(I_{ON}\) and 5 degradation, by increasing \(T_D\) (Figure 4a). The simulation result shows that \(I_{AMB}\) is reduced approximated 2 orders of magnitude as \(T_D\) increases from 5 nm to 20 nm, since the electric field at the channel-to-drain junction is decreased efficiently.
Performances are examined as well. In case of TFET, unlike to the MOSFET, gate-to-drain capacitance ($C_{GD}$) dominates entire gate capacitance ($C_{GG}$) while gate-to-source capacitance ($C_{GS}$) is negligible [30]. Therefore, $C_{GD}$ as a function of $V_{GS}$, is examined with the various $T_D$ from 5 to 50 nm-thick. Figure 4b shows that $C_{GD}$ is increased proportionally to the $T_D$, due to the increase of drain area. It is problematic for high-speed and low-power CMOS logic applications, since the $C_{GD}$ is directly related to the Miller capacitance, which increases voltage over/under-shoots and delay time [31]. In other words, there is a trade-off between $I_{AMB}$ and $C_{GD}$ in terms of $T_D$. As shown in Figure 5, the $C_{GD}$ remarkably increases when $T_D \geq 20$ nm while the amount of decreasing $I_{AMB}$ is negligible. Therefore, the optimum $T_D$ is determined as 20 nm.

In addition to the increase in $T_D$, another strategy is required to suppress $I_{AMB}$ and $C_{GD}$, simultaneously. As shown in Figure 6a, if the DU (i.e., the length of drain underlap region) is increased, the $I_{AMB}$ is further decreased. This result is obvious based on the previous studies [32,33]. However, DGIT-TFET can minimize the DU because $I_{AMB}$ is already restrained by large $T_D$. It is beneficial, not only for the small parasitic resistance, but for the high integration density. Moreover, Figure 6a clearly shows that if the DU increases more than 10 nm, the $I_{OFF}$ becomes worse in spite of the longer DU due to the significant SRH leakage. The DGIT-TFET with 10 nm-DU shows smaller $I_{AMB}$ and $C_{GD}$ than that for 0 nm-DU with the amount of about 2.1, and 3.5 orders of magnitudes, respectively (Figure 6a,b). Considering these results, the optimum DU can be determined as ~10 nm. The adoption of drain underlap region can be realized easily without any aggressive process capability issue by changing the height of STI oxide. The detail about the influence of $C_{GD}$ on voltage overshoot during CMOS operation will be discussed at the end of this section.

**Figure 4.** DGIT-TFET’s (a) $I_D$ and (b) $C_{GD}$ as a function of $V_{GS}$ while the $T_D$ changes from 5 to 50 nm.
Figure 5. $I_{\text{AMB}}$ and $C_{\text{GD}}$ depending on $T_D$ from 5 to 50 nm.

Figure 6. (a) $I_D$ and (b) $C_{\text{GD}}$ curves of DGIT-TFET as a function of $V_{\text{GS}}$ while the DU changes from 0 to 15 nm.

As above-mentioned, the vertical-structured DGIT-TFET is compatible to the SEG process for Si$_{1-x}$Ge$_x$/Si heterojunction formation. It is worthwhile to study the effects of heterojunction on DGIT-TFET’s driving current, since the use of a narrow bandgap material can reduce the tunnel resistance drastically. Figure 7b shows transfer characteristics of DGIT-TFET according to the Ge mole fraction ($x_M$) at source-channel junction (Figure 7a). If $x_M$ increases, $I_{\text{ON}}$ is effectively improved, without increasing $I_{\text{AMB}}$, due to the decrease of BTBT resistance. In case of 100%-xM, $I_{\text{ON}}$ is increased more than two-orders of magnitude from that for sub-70%-xM cases because direct band-to-band tunneling (BTBT) can be utilized [16,18,27].

Last of all, the transient characteristics of CMOS inverter composed of $n$-channel DGIT-TFET and $p$-channel DGIT-MOSFET are investigated by changing DU. In this case, 100%-xM is used as a
source-channel junction for best performance. As shown in Figure 8, it is clear that DGIT-TFET inverter can be operated with less than 1 ns intrinsic delay time. There is a considerable voltage overshoot for the 0 nm-DU due to the large Miller capacitance; $C_{GD}$. It is necessary to address this issue since it is problematic in terms of power consumption, reliability, and so on. As shown in the inset of Figure 8, the overshoot phenomenon is significantly suppressed as DU increases with the help of decreased $C_{GD}$ (Figure 6b). If 10 nm-DU (the optimized length considering $I_{OFF}$ and $C_{GD}$) is adopted in DGIT-TFET, overshoot voltage becomes ~30 % of that for 0 nm-DU.

![Figure 6b](image)

**Figure 6.** (a) ID and (b) CGD curves of DGIT-TFET as a function of DU = 0, 2.5, 5, 7.5, 10, 15 nm.

![Figure 7](image)

**Figure 7.** (a) The structures of heterojunction Si$_{1-x}$Ge$_x$ according to changing Ge mole fraction from 0 to 100 % on source and source-side channel. (b) $I_D$ as a function of $V_{GS}$ for the structures in (a). As the Ge mole fraction of Si$_{1-x}$Ge$_x$ is higher, the $I_{ON}$ level is accordingly higher.

![Figure 8](image)

**Figure 8.** Transient responses of CMOS inverter composed of n-channel DGIT-TFET and p-channel DGIT-MOSFET during the input signal rising. The inset shows the voltage overshoots can be efficiently suppressed as DU increase. The graph with open symbols also compares in case the conventional structure without tapering (i.e., DG-TFET) is used as a pull-down device. The overshoot trends are exactly matched with $C_{GD}$ characteristics shown in Figures 4b and 6b.
4. Summary

In this paper, a novel vertical-channel DG TFET, with asymmetric source/drain area, has been proposed and optimized by using TCAD simulations. It can achieve improved DC, as well as AC performances (i.e., improved $I_{ON}$, suppressed $I_{AMB}$ and $C_{GD}$), with the help of its geometrical benefits. Since the proposed structure is compatible with the SEG process, its performance can be further improved by adopting Si$_{1-x}$Ge$_x$ heterojunction at source-channel junction, with high xM. In addition, its high compatibility with state-of-the-art FinFET process flow promises its feasibility of a readily introduction to the current CMOS technology as a successor and/or supplementary for MOSFETs.

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