Full-Range LED Dimming Driver With Ultrahigh Frequency PWM Shunt Dimming Control

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\textbf{ABSTRACT} This paper explores an ultrahigh dimming frequency Light-Emitting Diode (LED) pulse width modulation (PWM) shunt dimming driver that achieves the full-range dimming. Firstly, the dimming frequency is improved to 20kHz for avoiding flicker and audible noise in high dimming requirements application, such as film and television shooting. Secondly, this paper reduces dimming ratio loss at ultrahigh dimming frequency by removing output capacitor. As a result, given 1% dimming ratio is achieved. Subsequently, for improving LED current square waveform at ultrahigh dimming frequency, it is necessary to suppress parasitic oscillation at the falling edge in LED current. Therefore, this paper proposes a method which connects a fast recovery diode with LED in series. In such way, parasitic oscillation at the falling edge in LED current is suppressed. Meanwhile, linear dimming performance is improved such as dimming linearity of low ratio and circuit reliability. Finally, a 120 W experimental prototype is built to drive an LED array comprising 9 LEDs in parallel and 15 LEDs in series. The switching frequency and dimming frequency of prototype are 500 kHz and 20 kHz, respectively. In addition, it achieves full dimming range of 1% to 99.99%.

\textbf{INDEX TERMS} Output capacitance, PWM shunt dimming, ultrahigh dimming frequency, full-range dimming, parasitic parameters.

\section{I. INTRODUCTION}
The light-emitting diodes (LEDs) have attracted much attention due to its advantages, such as long lifespan (approximately 25,000 to 50,000 hours), high luminous efficacy (250 lm/W), small size, and zero pollution \cite{1}–\cite{3}. LED has been widely used in many applications, including street lighting, office lighting, residential lighting and film and television shooting \cite{1}–\cite{4}.

LED illuminance is related to the forward current. Due to the non-linear relationship between its voltage and current, a small voltage variation may cause dramatic change of the forward current, thereby leading to a change in LED illuminance \cite{18}. Therefore, to better control LED illuminance and fully utilize its energy-saving, it is necessary to control a constant current driver using the corresponding dimming method to drive the LED \cite{3}, \cite{6}, \cite{19}, \cite{20}. There are mainly two types of LED dimming methods: amplitude-modulation (AM) dimming and pulse-width-modulation (PWM) dimming \cite{3}, \cite{6}, \cite{21}. Smooth current can be obtained by using AM dimming method, which adjust the LED illuminance by directly changing forward current amplitude. It is easy to control but its dimming lacks linearity and leads to a noticeable shift in the chromaticity coordinates \cite{3}. Therefore, AM dimming method cannot be used for high lighting quality requirements applications. PWM dimming involves the control of LED illuminance by adjusting the time taken for constant current to flow through an LED (i.e. dimming ratio). Because the current amplitude has not changed, as a result, pronounced shift in color temperature is prevented \cite{19}. Therefore, PWM dimming method is suitable for high quality LED lighting applications, such as film and television shooting. However, PWM dimming causes flicker if a low dimming frequency is used, which may affect human health and other equipment. For preventing flicker, improving dimming frequency is an efficient method. When dimming frequency is above 1kHz more or less, flicker is not perceived by the human eyes. Whereas, there are some facilities such as
film and television shooting, photographic equipment is more sensitive to flicker than human eyes. It is necessary to further improve dimming frequency. When dimming frequency is synchronous or much higher than camera frames, flicker can be avoided well. In addition, when dimming frequency is lower than 20 kHz, audible noise is produced due to the magnetostrictive effects of the inductors and the piezoelectric effects of the capacitors. Increasing the dimming frequency is also an effective method for eliminating audible noise [5], [22], [23]. Study [5] performs discontinuous conduction mode (DCM) control on a buck converter without an output capacitor using DC driving technology. It controls LED illuminance by adjusting the number of current pulses in the dimming period. By this means, the goals of no flicker and cost optimization are achieved. However, the accuracy of current control is reduced. Study [8] carries out constant current PWM dimming using a dual-bus buck converter and increases the efficiency of converter. Nevertheless, only experimental verification of low-dimming frequency is conducted.

There are three main PWM dimming schemes, namely PWM enable dimming, PWM series dimming, and PWM shunt dimming [6], [21]. PWM enable dimming performs high-frequency on-off switching by applying a logic-level PWM signal. However, the presence of delay time and rise time increases the time taken for the LED current to reach a constant current value. Thereby further improvement in dimming frequency is affected. PWM series dimming is a dimming method based on LED voltage control. As LED voltage fluctuation can easily cause LED current fluctuation, so a large output capacitor is needed to store energy [3], [21]. PWM shunt dimming realizes dimming by connecting the load to a switch in parallel. This method can achieve high dimming frequency and wide dimming range. But short-circuit switching may cause system stability problem, as well as LED current spike and parasitic oscillation. Snubber circuits such as RC and CD are used to absorb the current spike. And a damping resistor connected in series in the loop is used to suppress parasitic oscillation [8], [21].

Due to the non-linear relationship between LED illuminance and dimming ratio, illuminance is more sensitive to change within a low dimming ratio range. The tendency of LED illuminance changing with dimming ratio is shown in Fig. 1. Curve 1 represents the relationship between dimming ratio and LED illuminance. As shown, LED illuminance becomes gradually stronger as dimming ratio increases. Curve 2 denotes the difference in LED illuminance at every 10% dimming ratio within the range of 0% to 100%. Based on Curve 2, it can be concluded that the peak difference of LED illuminance occurs within the dimming ratio of 10% to 20%. However, when the dimming ratio is larger than 20%, the difference of LED illuminance gradually decreases. Hence, it is necessary to fully utilize the dimming capability of the LED at low ratio (<20%). Study [23] uses average current mode control to achieve constant current output in a buck converter without an output capacitor. Meanwhile, it realizes an offline LED driver with dual purposes, namely illumination control and visible light communication (VLC). Both of high dimming frequency and good dimming linearity are obtained. But this paper only provides experimental waveforms within a dimming range of 20% to 80%. Subharmonic oscillation is eliminated in [24] by using average current control (ACC). Besides, the dual-phase mode is employed to achieve good current balance and small current ripples. However, this experiment only exhibits a dimming range of 20% to 80% at a dimming frequency of 20 kHz. The accuracy of average LED current control is enhanced through an autozeroed integrator as stated in [25]. In addition, the employment of a fast-settling technique allows a LED driver to reach steady state within three switching cycles after the dimming signal is triggered. Unfortunately, experimental verification is still conducted within a dimming range of 5% to 95%.

At present, many topologies are used for dimming control, such as buck [5]–[8], boost [9], buck-boost-buck [10], flyback [11], buck-flyback-buck [3], half-bridge [12], Cuk [27], and resonant circuits [2], [13]–[17]. These topologies achieve one or more optimization goals, including high efficiency, wide dimming range, wide input voltage range, and cost-saving, through their corresponding control strategies.

PWM shunt dimming method is beneficial for ultrahigh dimming frequency and full-range dimming. In addition, a buck converter is used widely due to its simplicity, high reliability and high efficiency. Based on the above two points, this paper selects three-switch buck converter as dimming topology. However, in the dimming topology, the switching frequency will be decreased when LED current is zero to increase converter efficiency. Therefore, the inductor current will fluctuate periodically with dimming frequency. And audible noise is produced if dimming frequency is lower than 20 kHz. Besides, flicker should also be not perceived by high quality lighting requirement applications and human eyes. In order to eliminate audible noise and avoid flicker, the dimming frequency is improved as high as 20 kHz in this paper.

Subsequently, both the full-range dimming and better LED current square waveform at ultrahigh dimming frequency should be achieved. During ultrahigh-frequency PWM shunt dimming, the output current pulse width is relatively narrow and short. Therefore, the converter should have enough fast...

**FIGURE 1.** LED light illuminance at different dimming ratios.
response speed to reduce dimming ratio loss and improve low ratio dimming capacity. Besides, to obtain better LED current square waveform and improve linear dimming performance, it is necessary to suppress parasitic oscillation at the falling edge in LED current.

For achieving the full-range dimming and obtaining better LED current square waveform at ultrahigh dimming frequency, the following studies are carried out:

1) Builds the mathematical model consisting of parasitic parameters. The effect of parasitic parameters on system stability and performance of output port is analyzed.

2) Increases response speed of output port by removing output capacitor. In such way, dimming ratio loss is reduced and low ratio dimming capacity is improved.

3) Suppresses parasitic oscillation of LED current to obtain better LED current square waveform. Meanwhile, linear dimming performance is also improved such as dimming linearity of low ratio and circuit reliability.

This paper is mainly divided into four sections. Section II investigates the effect of parasitic parameters on system stability by establishing a mathematical model of the three-switch buck converter consisting of parasitic parameters. Section III analyzes the effect of output capacitance and parasitic parameters on ultrahigh frequency dimming in detail. Meanwhile, a method for suppressing oscillation at falling edge of LED current is proposed. Section IV presents the experimental results. Section V concludes this paper.

II. SYSTEM MODELING AND STABILITY ANALYSIS WITH CONSIDERATION OF PARASITIC PARAMETERS

The specific converter topology is shown in Fig. 2(a). \( Q_1 \) is the main switch, and \( Q_2 \) is the synchronous switch. Based on the general buck converter, a dimming switch, \( Q_3 \), which is used for output short-circuit, is connected at both ends of the LED in parallel. Inductor current closed-loop control is performed to maintain inductor current at a constant value \( I_{\text{ref}} \). Ultrahigh-frequency PWM shunt dimming is achieved by adjusting the duty cycle of \( V_{g-Q3} \). Fig. 2(b) shows the ideal waveforms, where \( V_{g-Q1} \) is driving voltage of \( Q_1 \), and \( V_{g-Q3} \) is driving voltage of \( Q_3 \). When \( Q_3 \) is turned off, the converter turns into a general buck converter. At this point, \( Q_1 \) and \( Q_2 \) are switched at a high switching frequency (such as 500 kHz), and LED is driven by a constant current \( I_{\text{ref}} \). When \( Q_3 \) is turned on, \( Q_1 \) and \( Q_2 \) are switched at a low switching frequency (such as 50 kHz) to reduce switching losses and improve efficiency. LED voltage is nearly clamped to zero, and it is lower than bias voltage of LED. LED is as an open circuit and LED current is zero. It’s shown that the duty cycle of \( Q_3 \) complements the dimming ratio, \( D_{\text{dim}} \). Thus, a lower duty cycle of \( Q_3 \) results in a higher dimming ratio \( D_{\text{dim}} \). In other words, a lower duty cycle of \( Q_3 \) leads to longer LED constant current driving time and higher LED illuminance.

It should be noted that, the switching frequency of \( Q_1 \) is changeable with \( V_{g-Q3} \). Therefore, the inductor current \( i_L \) fluctuates periodically with dimming frequency actually.

And audible noise is produced if dimming frequency is lower than 20 kHz. In this paper, the dimming frequency is 20kHz, noise audible to human ears which caused by switching converter is eliminated.

This paper considers three main parasitic parameters, including LED junction capacitance \( C_J \), \( Q_3 \) drain-source capacitance \( C_{DS} \), and long wires parasitic inductance \( L_g \). To decrease wires loss, long wires is thick enough and parasitic resistance \( R_s \) is small enough generally. It is not vital for oscillation suppression. Therefore, this paper neglects \( R_s \). The schematic diagram of converter considering these parasitic parameters is shown in Fig.3.

Meanwhile, the LED equivalent circuits in different cases are also shown in Fig.3. As can be seen, high frequency LED equivalent circuit (in case of high frequency LED current) is formed by ideal diode, bias voltage \( V_D \), series equivalent resistance \( R_0 \) and parallel capacitor \( C_J \). Thereby low frequency LED equivalent circuit (in case of low frequency LED current) could be obtained by removing \( C_J \).

In addition, for analyzing the effect of parasitic parameters on system stability and performance of output port, high frequency LED dynamic equivalent circuit (in case of high frequency LED current and \( U_{\text{LED}} > V_D \)) also need to be built.

A. HIGH FREQUENCY LED DYNAMIC EQUIVALENT CIRCUIT

The high frequency LED dynamic equivalent circuit could be obtained by parallel connection of the low frequency LED
The dynamic equivalent circuit (in case of low frequency LED current and $U_{LED} > V_D$) and $C_1$. Therefore, the low frequency LED dynamic equivalent circuit is established firstly.

Based on [26], the $V-I$ relationship of LED could be expressed by
\[
i_{LED} = a_1 u^2_{LED} + a_2 u_{LED} + a_3 (U_{LED} > V_D) \tag{1}
\]
where $i_{LED}$ is the LED current and $U_{LED}$ is the LED voltage. $a_1$, $a_2$, $a_3$ are the characteristic coefficients. Based on (1), the low frequency LED dynamic mathematical model is expressed
\[
\begin{align*}
i_{LED} &= k \hat{u}_{LED} \\
k &= 2a_1 V_{LED} + a_2
\end{align*} \tag{2}
\]
\[
\hat{u}_{LED} \text{ is the fluctuation of } i_{LED} \text{ and } U_{LED} \text{ respectively, } V_{LED} \text{ is the steady voltage of LED; and } k \text{ is relative coefficient. Based on (2), it can be seen that the low frequency LED dynamic equivalent circuit is an equivalent changeable resistor } 1/k. \text{ Therefore, the high frequency LED dynamic equivalent circuit which is shown in Fig.3 is obtained by parallel connection of } 1/k \text{ and } C_1.
\]

**B. STABILITY ANALYSIS WITH CONSIDERATION OF PARASITIC PARAMETERS**

Due to the existence of $Q_3$, the operating state of three-switch buck converter can be divided into LED driving state when $Q_3$ is turned off, and output short-circuit state when $Q_3$ is turned on. Stability of the system consisting of parasitic parameters in both two states is analyzed to verify system stability.

1) **STABILITY ANALYSIS IN LED DRIVING STATE**

Fig 4 shows the total high frequency dynamic equivalent circuit in LED driving state (with $Q_3$ turned off). The mathematical model of three-switch buck converter under this condition is expressed by
\[
\frac{I_L(s)}{d(s)} = \frac{A_1 s^3 + (L_L C_0 U_{in}) s^2 + A_2 s + U_{in}}{A_3 s^4 + (L_L LC_0) s^3 + A_4 s^2 + (L + L_L) s + 1/k} \tag{3}
\]

According to the Routh stability criterion, the system is absolutely stable. Please refer to the appendix for the Routh tabulation. It is evident that the effect of parasitic parameters is not vital for absolute stability of the system in LED driving state.

2) **STABILITY ANALYSIS IN OUTPUT SHORT-CIRCUIT STATE**

Fig 5 shows the total high frequency dynamic equivalent circuit in the output short-circuit state (with $Q_3$ turned on). $R_d$ is the on-resistance of $Q_3$. In this case, the mathematical model of three-switch buck converter is expressed by
\[
\frac{I_L(s)}{d(s)} = \frac{(C_3 L_q U_{in} C_{out} R_d / k) s^3 + B_1 s^2 + B_2 s + B_3}{(C_3 L_q C_{out} R_d / k) s^4 + B_4 s^3 + B_5 s^2 + B_6 s + R_d C_{out} / k} \tag{5}
\]

\[
\begin{align*}
B_1 &= L_q U_{in} C_{out} C_1 / k + C_{out} L_q U_{in} R_d \\
B_2 &= C_{out} L_q U_{in} + R_d U_{in} C_{out} C_1 / k + C_{out} R_d U_{in} / k \\
B_3 &= U_{in} C_{out} / k + C_{out} U_{in} R_d \\
B_4 &= C_{out} C_3 L_q / k + L_q L_{out} C_{out} R_d \\
B_5 &= C_{out} L_q L + C_3 L_{out} C_{out} / k + C_{out} C_3 L_q R_d / k + L_{out} R_d / k \\
B_6 &= L_q C_{out} R_d + C_{out} L / k + R_d L C_{out}
\end{align*} \tag{6}
\]

FIGURE 3. LED equivalent circuits and schematic diagram of converter considering parasitic parameters.
Similarly, according to the Routh stability criterion, the system is also absolutely stable. Please refer to the appendix for the Routh tabulation. Therefore, the effect of parasitic parameters is not vital for absolute stability of the system in output short-circuit state as well.

The mathematical model is expressed by
\[
\frac{I_{LED}(s)}{I_L(s)} = \frac{sC_J + k}{sL_gC_0s^2 + L_gC_0ks^2 + (C_0 + C_J)s + k}
\]  

Fig 7 shows the frequency characteristic of the network under different values of \(C_{out}\). It is shown that as \(C_{out}\) increases, amplitude crossover frequency \(\omega_c\) decreases, while the response speed of the network decreases. Thus, the rise time becomes longer.

**FIGURE 6.** High frequency output port dynamic equivalent circuit considering parasitic parameters.

**III. THE EFFECT OF OUTPUT CAPACITANCE AND PARASITIC PARAMETERS ON ULTRAHIGH FREQUENCY DIMMING**

As seen from Fig 3, all the three parasitic parameters (\(C_J\), \(C_{DS}\), and \(L_g\)) and output capacitor \(C_{out}\) are located outside the inductor current closed loop. Thus, the effect of those parameters on ultrahigh frequency dimming can be analyzed by establishing a mathematical model of output port. In this section, the effect of \(C_{out}\) on dimming ratio loss is firstly analyzed. Subsequently, the effect of three main parasitic parameters on performance of output port is also presented. In addition, the mechanism for the formation of oscillation at falling edge in LED current is studied in detail. Finally, an oscillation suppression method is proposed to obtain better LED current square waveform and linear dimming performance at ultrahigh dimming frequency. Fig 6 shows the high frequency output port dynamic equivalent circuit comprising the parasitic parameters.

**A. EFFECT OF \(C_{out}\) ON DIMMING RATIO LOSS**

The effect of \(C_{out}\) on dimming ratio loss is shown in two aspects. Namely, the rise time \(t_r\) and the delay time \(t_d\).

1) **THE EFFECT OF \(C_{out}\) ON RISE TIME**

The high frequency output port dynamic equivalent circuit in LED driving state with \(C_{out}\) is shown in Fig.6.

![High frequency output port dynamic equivalent circuit considering parasitic parameters.](image)

**FIGURE 7.** Frequency characteristic under different values of \(C_{out}\).

**FIGURE 8.** Waveforms of LED current under different values of \(C_{out}\).

**2) THE EFFECT OF \(C_{out}\) ON DELAY TIME**

From Fig 8, \(t_{d1}, t_{d2}, t_{d3}\), and \(t_{d4}\) are the delay time of LED current corresponding to \(C_{out1}, C_{out2}, C_{out3}\), and \(C_{out4}\) respectively. \(t_{d1}, t_{d2}, t_{d3}\), and \(t_{d4}\) are the actual delay time of LED current corresponding to \(C_{out1}, C_{out2}, C_{out3}\), and \(C_{out4}\). It’s clearly shown \(t_{d1} < t_{d2} < t_{d3} < t_{d4}\) and \(t_{d1} \approx 0\).

Hence, the following conclusion can be drawn. As \(C_{out}\) increases, the rise time becomes longer, and the dimming ratio loss increases.

The high frequency output port dynamic equivalent circuit in LED driving state with \(C_{out}\) is shown in Fig.6.
calculated by

$$t_d = \frac{C_i V_D}{I_{ref}} = \frac{(C_{out} + C_{DS}) V_D}{I_{ref}}$$ (8)

$V_D$ is bias voltage of LED. $I_{ref}$ is the constant LED current.

Based on (8), it’s clearly shown $t_{d1} < t_{d2} < t_{d3} < t_{d4}$ and $t_{d1} \approx 0$. Hence, as $C_{out}$ increases, the delay time becomes longer, and the dimming ratio loss increases.

In summary, as $C_{out}$ increases, both the rise time and delay time increase, and the dimming ratio loss increases. When given dimming ratio is low, $t_i + t_d$ is probably larger than given dimming time, $i_{LED}$ could not even reach the constant current value, and thus LED could not be driven normally.

### B. EFFECT OF PARASITIC PARAMETERS ON LED CURRENT SQUARE WAVEFORM

The effect of three main parasitic parameters on performance of output port is presented after removing $C_{out}$. In addition, the mechanism for the formation of oscillation at falling edge in LED current is studied in detail.

#### 1) THE EFFECT OF PARASITIC PARAMETERS ON PERFORMANCE OF OUTPUT PORT IN LED DRIVING STATE

The high frequency output port dynamic equivalent circuit in LED driving state without $C_{out}$ is shown in Fig.6. The LED current-to-inductor current transfer function is expressed by

$$\frac{I_{LED}(s)}{I_L(s)} = \frac{SC_1/k + 1}{(C_LkC_{DS}/k)s^3 + (L_gC_{DS})s^2 + Ds + 1}$$ (9)

$$D = C_{DS}/k + C_1/k$$ (10)

Fig 9 shows its corresponding frequency characteristic of the output port under different parasitic parameters.

In the frequency characteristic, resonance peak $M_r$ represents the relative stability of output port; resonance frequency $\omega_r$ represents the speed of dynamic response; Based on Fig 9, it indicates that relative stability of the output port increases as $C_{DS}$ and $L_g$ increase but decreases as $C_L$ increases. The response speed of the output port decreases as $C_{DS}$, $L_g$, and $C_L$ increase.

#### 2) THE EFFECT OF PARASITIC PARAMETERS ON PERFORMANCE OF OUTPUT PORT IN OUTPUT SHORT-CIRCUIT STATE

The high frequency output port dynamic equivalent circuit in output short-circuit state without $C_{out}$ is shown in Fig.6. The LED current-to-inductor current transfer function is expressed by (11). On this basis, it is evident that the output port is a second-order oscillation element when $Q_3$ is turned on, while resonance occurs at $C_L$ and $L_g$.

$$\frac{I_{LED}(s)}{I_L(s)} = \frac{(SC_1/k + 1)R_d}{(C_L/k)s^2 + (C_1R_d/k + L_g)s + (R_d + 1/k)}$$ (11)

Fig 10 shows the frequency characteristic of the output port under different parasitic parameters.

Based on Fig 10, it is shown that as $L_g$ increases, both resonance peak $M_r$ and resonance frequency $\omega_r$ decrease. Namely, relative stability of the output port increases and the response speed of the output port decreases. At the same time, the output port is a second-order oscillation element, where $M_r$ and $\omega_r$ also represent oscillation amplitude and oscillation frequency in the time domain, respectively. Therefore, as $L_g$ increases, oscillation amplitude decreases and oscillation frequency decreases.

Similarly, as $C_L$ increases, resonance peak $M_r$ increases and resonance frequency $\omega_r$ decreases. Both the relative stability and response speed of the output port decrease. Moreover, oscillation amplitude increases but oscillation frequency decreases. At the same time, bandwidth frequency $\omega_b$, which means damping, basically does not change with $C_L$. The oscillation time (also the settling time) is only related to the
response speed of the output port. Therefore, oscillation time increases as $C_J$ increases.

Fig. 11 shows the simulation waveforms of falling edge in LED current under different values of $L_g$ and $C_J$. In this Fig.11(a), $I_{Lg1}$, $I_{Lg2}$, and $I_{Lg3}$ are LED current values corresponding to $L_{g1}$, $L_{g2}$, and $L_{g3}$, respectively. The oscillation peaks at $I_{Lg1}$, $I_{Lg2}$, and $I_{Lg3}$ are noted as $A_1$, $A_2$, and $A_3$. $t_1$, $t_2$, and $t_3$ are times when the first oscillation peak appears at $I_{Lg1}$, $I_{Lg2}$, and $I_{Lg3}$, respectively. It can be seen that $A_1 > A_2 > A_3$, $t_1 < t_2 < t_3$. It indicates that an increase in $L_g$ results in a decrease in the oscillation amplitude and oscillation frequency at the falling edge of LED current.

Based on Fig.11(b), $I_{Lc1}$, $I_{Lc2}$, and $I_{Lc3}$ are LED current values corresponding to $C_{J1}$, $C_{J2}$, and $C_{J3}$, respectively. The oscillation peaks at $I_{Lc1}$, $I_{Lc2}$, and $I_{Lc3}$ are noted as $B_1$, $B_2$, and $B_3$. $t_4$, $t_5$, and $t_6$ are times when the third oscillation peak appears at $I_{Lc1}$, $I_{Lc2}$, and $I_{Lc3}$, respectively. It is shown that $B_1 < B_2 < B_3$, $t_4 < t_5 < t_6$. It is observed that an increase in $C_J$ results in an increase in the oscillation amplitude and a decrease in the oscillation frequency at the falling edge of LED current. Meanwhile, it is also shown that $t_4 < t_5 < t_6$, indicating an increase in $C_J$ causes an increase in oscillation time.

Table 1 summarizes the effect of parasitic parameters on LED current and the performance of output port.

| Parasitic Oscillation Suppression Method |
|------------------------------------------|
| $C_{ds}$ | $L_g$ | $C_J$ |
|↑↓|↑↓|↓|

$↑↓$ show the changing trend of parasitic parameters for improving the corresponding performance. Where $↑$ indicates an increase, and $↓$ indicates a decrease.

Parasitic oscillation at the falling edge of LED current is not beneficial for further improvement of LED current square waveform at ultrahigh dimming frequency. Therefore, it is necessary to suppress the current parasitic oscillation.

### C. PARASITIC OSCILLATION SUPPRESSION METHOD

Based on the above analysis, oscillation occurs at the falling edge in LED current due to $C_J$ and $L_g$. From Table 1, it is obvious that reducing $C_J$ could lower both oscillation amplitude and oscillation time. Besides, it can also improve the relative stability and response speed of output port.

However, it is difficult to directly reduce $C_J$. Therefore, this paper proposes a method which connects a fast recovery diode $D_f$ with LED in series. In such way, $C_J$ is reduced indirectly and the current parasitic oscillation is suppressed. Better LED current square waveform could be obtained. Meanwhile, linear dimming performance is also improved such as dimming linearity of low ratio and circuit reliability. Fig.12 shows the schematic diagram of the dimming driver.
When $Q_3$ is turned off, $D_f$ conducts current and LED is driven normally. When $Q_3$ is turned on, $D_f$ is turned off quickly and resonance occurs among $C_J$, $C_{Df}$ and $L_g$. The equal capacitance $C_{eq}$ is expressed by

$$C_{eq} = \frac{C_J C_{Df}}{C_J + C_{Df}} < \min(C_J, C_{Df}) \quad (12)$$

$C_{eq}$ is smaller than $C_J$, which is equivalent to indirectly reduce LED junction capacitance. The oscillation amplitude and oscillation time both are reduced. Fig. 13 shows the related simulation waveforms.

$\text{FIGURE 13. Simulation waveforms without and with a fast recovery diode.}$

$I_{LO1}$ and $I_{LO2}$ are corresponding current values without and with a fast recovery diode when $Q_3$ is turned on. From Fig 13, it is shown that by connecting a fast recovery diode, the oscillation time and oscillation amplitude can be significantly reduced.

The traditional method which series an external damping resistor $R_r$ with LED can also reduce oscillation amplitude and oscillation time by increasing damping of output port. The proposed method has following advantages compared with the traditional method:

1) Simplify the design process. The value of $R_r$ depends on specific value of $L_g$ and $C_J$. However, it is unnecessary in the proposed method because $C_{eq}$ must be smaller than $C_J$.

2) Reduce power loss. A larger $R_r$ will result in a larger power loss. In comparison, the forward voltage of $D_f$ is relatively smaller.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

An 800W AC/DC dimming system prototype is built in the laboratory, as shown in Fig. 14. The dimming system includes three stages, and the proposed three-switch buck dimming driver is stage 3. Input current from grid is continuous and sin waveform, the input current of three-switch buck dimming driver (dimming driver for short) is switching due to the buck topology.

$\text{FIGURE 14. System block diagram of prototype.}$

Table 2 presents the specific parameters of the three-switch buck dimming driver (stage 3), and Fig.12 shows the schematic diagram of the dimming driver.

$\text{TABLE 2. Parameters of the three-switch buck dimming driver.}$

| Parameter                      | Value                           |
|--------------------------------|---------------------------------|
| Input voltage, $V_i$           | 60 V                            |
| Output constant current, $I_o$ | 2.5 A                           |
| LED voltage, $V_{LED}$         | 48 V                            |
| High switching frequency, $f_w$| 500 kHz                         |
| Inductance, $L$                | 150 uH                          |
| Dimming frequency, $f_{dim}$   | 20 kHz                          |
| Bias voltage of LED, $V_D$     | 40 V                            |
| Long wires inductance, $L_g$   | 1.3 μH(20kHz)                   |
| 970nH(500kHz)                  | 900nH(1MHz)                     |
| 620pF(20kHz)                   | 650pF(500kHz)                   |
| 680pF(1MHz)                    |                                 |
| LED junction capacitance, $C_J$| 23mΩ                            |
| $Q_1$, drain-source capacitance, $C_{D1}$ | 392pF                  |
| $Q_1$, $Q_2$, $Q_3$            | SIR680DP                        |
| Output diode $D_f$             | DSEP15-06A                      |
| Snubber capacitance, $C_s$     | 3nF                             |
| Snubber resistance, $R_s$      | 20Ω                             |
| Junction capacitance of diode, $C_{Df}$ | 12pF                |
| turn-on voltage set by chip, $V_{turn}$ | 15V                |

The paper compromises 60V as the input voltage of three-switch buck dimming driver. There are three reasons:

1) When the input voltage of dimming driver is lower, input current RMS is larger at the same output power. Therefore, the dimming driver efficiency is decreased.

2) If any LED bead is breakdown, those LED beads in series will extinguish, the higher input voltage of dimming driver means more LED beads in series. Hence, high input voltage is not conducive to fault tolerance of LED lighting system.

3) The dimming driver is the backward stage of LLC converter. When the input voltage of dimming driver...
(namely, the output voltage of the LLC converter) is larger, it is difficulty to choose LLC MOSFET due to its larger on-resistance (Lower voltage Si MOSFET has lower on-resistance). Hence, too high input voltage of the dimming driver (LLC synchronous rectification MOSFET limited output voltage within 80V) will not conducive to improve the LLC efficiency.

**FIGURE 15. The prototype of dimming driver.**

Fig.15 shows the prototype of dimming driver. As Fig. 15(a) shows, each lamp holder includes cold and warm light LED beads. Therefore, two identical 120W LED dimming drivers are needed which is shown in Fig 15(b). This paper only shows one channel experiment waveforms.

**A. VERIFICATION OF THE EFFECT OF THE OUTPUT CAPACITANCE**

When the given dimming ratios are 50% and 10%, respectively, the actual dimming ratios (namely actual constant current dimming ratio) under different values of $C_{out}$ are shown in Table 3.

| Given dimming ratio | $C_{out}$ | delay time $t_d$/μs | rise time $t_r$/μs | Actual dimming ratio |
|---------------------|----------|----------------------|-------------------|---------------------|
| 50%                 | 0 nF     | 0                    | 0                 | 0%                  |
|                     | 100 nF   | 1.8                  | 0.8               | 45.2%               |
|                     | 200 nF   | 3.4                  | 1.5               | 40.6%               |
|                     | 300 nF   | 5                    | 2.5               | 36.5%               |
| 10%                 | 0 nF     | 0                    | 0                 | 10%                 |
|                     | 100 nF   | 1.8                  | 0.8               | 5.1%                |
|                     | 200 nF   | 3.4                  | 1.5               | 0%                  |
|                     | 300 nF   | Unable to measure    | Unable to measure | 0%                  |

Based on Table 3, both $t_r$ and $t_d$ are about zero when $C_{out}$ is 0nF. The actual dimming ratio is consistent with the given dimming ratio. But both $t_r$ and $t_d$ increase as output capacitance increases. The actual dimming ratio decreases gradually. Furthermore, the actual dimming ratio is 0 when output capacitance reaches a certain value.

For the sake of clarity, Fig. 16 shows the experimental waveforms at given 50% dimming ratio when $C_{out}$ are 300 nF and 0 nF, respectively. Fig. 17 shows the experimental waveforms at given 10% dimming ratio when $C_{out}$ are 300 nF and 0 nF, respectively. In these figures, $I_L$ is the inductor current; $I_{LED}$ is the LED current; $V_{SW}$ is the drain-source voltage of Q2; and $V_{g-Q3}$ is the driving voltage of Q3.

Based on Fig. 16(b) and Fig. 17(b), when LED current is zero, Q1 operates in low switching frequency to improve efficiency. When LED current is constant value, Q1 operates in 500kHz. Therefore, the inductor current fluctuates periodically with dimming frequency. Besides, it’s noted that regardless of whether the given dimming ratio is 50% or 10%, when $C_{out}$ is 0nF and Q3 is turned off, $I_{LED}$ rises to a constant value of 2.5 A almost without $t_r$ and $t_d$, so the actual dimming ratio is consistent with the given dimming ratio.

Based on Fig. 16(a), when the given dimming ratio is 50% and Q3 is turned off, $t_r$ and $t_d$ are obvious due to the larger $C_{out}$ of 300nF. And the sum of $t_r$ and $t_d$ is about 13.5%
of dimming period. The actual dimming ratio is 36.5%. In addition, TPS92641 is a chip of LED voltage control mechanism. The switching frequency of $Q_1$ is decided by detecting LED voltage. $t_d$ includes $t_{s1}$ and $t_{s2}$. During $t_{s1}$, the LED voltage is lower than turn-on voltage $V_{\text{turn-on}}$ set by chip. The main switch $Q_1$ works at a low switching frequency. During $t_{s2}$, LED voltage becomes higher than turn-on voltage $V_{\text{turn-on}}$ set by chip, $Q_1$ starts to work at a high switching frequency (500kHz).

Based on Fig. 17(a), the given dimming time is almost 5$\mu$s when the given dimming ratio is 10%. However, $t_d$ is almost also 5$\mu$s by (8). Therefore, it is impossible to achieve LED constant current drive.

Consequently, the above experiment has verified that dimming ratio loss increases as $C_{\text{out}}$ increases. And the actual dimming ratio is consistent with given dimming ratio when $C_{\text{out}}$ is removed. Low ratio dimming capacity at ultrahigh dimming frequency is improved. However, as can be seen from Figs. 16-17, an obvious parasitic oscillation occurs at the falling edge in LED current, while an obvious current spike also occurs at the rising edge in LED current. Fig. 18 shows the magnified waveform of parasitic oscillation. The oscillation amplitude is about 2A and oscillation time is approximately 2.5$\mu$s. The oscillation frequency is about 5MHz.

**FIGURE 17.** Experimental waveforms at given 10% dimming ratio when (a)$C_{\text{out}}$=300 nF, and (b) $C_{\text{out}}$=0 nF.

**FIGURE 18.** Magnified waveform of oscillation at the falling edge in LED current without $D_f$.

B. VERIFICATION OF THE METHOD FOR SUPPRESSING OSCILLATION AT FALLING EDGE IN LED CURRENT

In this paper, the RC snubber circuit is connected in parallel to the dimming switch $Q_1$ to absorb current spike at the rising edge in LED current. The fast recovery diode DSEP15-06A is connected in series with LED to suppress parasitic oscillation at the falling edge in LED current.

**FIGURE 19.** Experimental waveforms after adding the RC snubber circuit and $D_f$ at given (a) 50% dimming ratio and (b) 10% dimming ratio.

Fig. 19 shows the experimental waveforms after adding the RC snubber circuit and $D_f$. Fig. 19(a) and Fig. 19(b) show...
the experimental waveforms at given 50% and 10% dimming ratio, respectively. By comparing Fig. 16(b) and Fig. 19(a), it’s worth noting that the RC snubber circuit absorbs current spike at the rising edge. Moreover, parasitic oscillation at the falling edge is suppressed with $D_f$. The same conclusion can be obtained by comparing Fig. 17(b) and Fig. 19(b). Fig. 20 shows the magnified waveform of parasitic oscillation at the falling edge in LED current with $D_f$. As seen, the oscillation amplitude decreases to 1 A, and the oscillation time is approximately 100 ns.

The experiment waveforms have verified that connecting LED in series with the fast recovery diode can significantly reduce oscillation amplitude and oscillation time at the falling edge in LED current. And both LED current square waveform and linear dimming performance at ultrahigh dimming frequency are improved. Moreover, the RC snubber circuit can also absorb the current spike at the rising edge in LED current. And the lifespan of LED could be prolonged.

C. VERIFICATION OF ULTRAHIGH-FREQUENCY FULL-RANGE DIMMING

Fig. 21 shows the experimental waveforms at the given 1%, 5%, 20%, and 99.99% dimming ratios after adding RC snubber circuit and $D_f$. It’s observed that the actual dimming ratio is consistent with the given dimming ratio in full dimming range. In addition, the RC snubber circuit can absorb current spike at the rising edge during full dimming range, while $D_f$ can suppress current parasitic oscillation at the falling edge during full dimming range.

Fig. 22 shows the dimming driver efficiency at different dimming ratios. Based on Fig. 22, the efficiency is reduced when the converter includes RC snubber circuit and a fast recovery diode. The difference between curve1 and curve2 is little at low dimming ratio. However, when dimming ratio is larger than 30%, curve2 is about 3% lower than curve1, and curve2 becomes stable at a level larger than 80%. This peak efficiency of curve2 is 85.3%.

The efficiency of the converter is a little bit low due to hard switching. Therefore, it is possible to improve efficiency by...
soft switching technology. Limited to the length of this paper, it will not be described here.

V. CONCLUSION
This paper investigates an ultrahigh dimming frequency, full-range LED dimming driver based on three-switch buck converter. The effect of parasitic parameters on system stability and performance of output port is analyzed. In addition, the mechanism for formation of parasitic oscillation at the falling edge of LED current is presented. Besides, the effect of output capacitance on dimming ratio loss is also studied. On that basis, low ratio dimming capacity at ultrahigh dimming frequency is improved by removing output capacitor. Moreover, LED current parasitic oscillation in falling edge is suppressed by adding a fast recovery diode to connect with LED in series. As a result, better LED current square waveform is obtained. And dimming linearity of low ratio and circuit reliability are improved.

Finally, the experiments of a 120W dimming driver are presented. The switching frequency and dimming frequency are 500 kHz and 20 kHz respectively. 1% to 99.99% full-range dimming is achieved and the peak efficiency is approximately 85.3%.

APPENDIX

LED driving state:

\[
\frac{I_L(s)}{d(s)} = \frac{A_1 s^3 + (L_g C_o U_{in}) s^2 + A_2 s + U_{in}}{A_3 s^4 + (L_g L_C o) s^3 + A_4 s^2 + (L + L_g) s + 1/k}
\]

\[
s_1 C_1 C_o L_g L/k \quad s_2 L_g L_C o \quad s_3 L_g L_C o/k \quad s_4 C_1 L_g L^2 /k^2
\]

Short-circuit state:

\[
\frac{I_L(s)}{d(s)} = \frac{(C_1 L_g U_{in} C^2_{out} R_d /k) s^3 + B_1 s^2 + B_2 s + B_3}{(C_1 L_g C^2_{out} R_d /k) s^4 + B_4 s^3 + B_5 s^2 + B_6 s + R_d C_{out} /k}
\]

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