Development of custom radiation-tolerant DCDC converter ASICs

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ABSTRACT: Based on a detailed study of the radiation tolerance of high-voltage transistors, 2 commercial CMOS technologies have been selected for the design of synchronous buck DCDC converter ASICs. Three prototype converters have been produced, embedding increasingly sophisticated functions. The electrical and radiation performance of these prototypes is presented.

KEYWORDS: Voltage distributions; Radiation-hard electronics; Radiation damage to electronic components

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1 Introduction

In view of an improved power distribution scheme for LHC detectors’ upgrades, we are developing radiation and magnetic field tolerant DCDC converters [1]. Installed on-detector, close to the Front-End circuits to power, they will provide an output voltage of 5–1.2V from an input of about 10V, and with an output current capability of up to 3A. The converter uses a few passive components (resistors, capacitors, inductors) and a radiation-tolerant Application-Specific Integrated Circuit (ASIC) embedding the high voltage switches and all control circuitry required to provide stable output power. Different prototypes of DCDC converter ASICs have been developed and are discussed in this paper.

1.1 Radiation tolerant CMOS technologies for DCDC converters

The successful development of a radiation-tolerant converter ASIC requires an adequate semiconductor technology capable of integrating both the conventional low-voltage CMOS devices (transistors, capacitors, resistors) and additional transistors with higher voltage capability — up to 14–20 V for a converter rated at 10 V of input voltage. These transistors are often constructed as Lateral Diffusion transistors, LDMOS.

Several commercial technologies offering the above feature have been studied to assess their response radiation in terms of Total Ionizing Dose (TID) and displacement damage effects [2]. Two technologies appear to provide adequate radiation performance, in different CMOS technology nodes (0.25 and 0.35 μm). While the 0.35 μm technology is mature and stable, the LDMOS devices in the 0.25 μm process are still being optimized for high speed and their design is evolving in different generations. Our radiation test covers generations 2A and 2B, with overall electrical and radiation performance exceeding those of the 0.35μm LDMOS. For this reason the quarter micron process has been chosen as the baseline for the converter’s design — with the 0.35μm as excellent backup.

TID and displacement damage are not the only threats posed by radiation to electronics circuits. High voltage transistors can also be subject to Single Event Burnout (SEB), with potentially
destructive consequences. Careful assessment of SEB sensitivity requires both the availability of
dedicated test structures and the costly access to a Heavy Ion accelerator facility. Therefore this
measurement has not been performed during the first technology selection, but later and only on
the two selected processes.

2 Prototype DCDC converter ASICs

Three DCDC converter ASIC prototypes have been developed. The first, defined as DCDC35B in
the following, is prototyped in the 0.35 \( \mu \)m technology, while the other two (P25A and P25B) are
fabricated in the 0.25 \( \mu \)m process.

2.1 The DCDC35B converter prototype

This circuit uses only N-channel LDMOS as power switches and includes the main building blocks
of the converter, but still requires a regulated 3.3 V supply voltage to be provided from off-chip.
Moreover, it uses a rather simple soft-start procedure and it does not include any protection fea-
ture (for over-current or over-temperature events). Measurements indicate that, despite the lack of
protection features, the prototype is reliably functional in a very wide range of operational condi-
tions: input voltage in the range of 6–12 V, output currents up to 3A, switching frequency of 1 to
3.5 MHz, inductance values of 200–700 nH. Efficiencies are varying between 70 and 80% in the
most useful conditions, with a large contribution from the parasitic resistance due to the packaging
and the choice for the on-chip metal stack to distribute the power. This indicates that the efficiency
can be improved sensibly in this technology.

A complete study concerning the radiation tolerance has been made on DCDC35B samples.
TID effects have been measured using the CERN-PH-ESE X-ray irradiation system. The converter
is kept in standard operational conditions during room-temperature irradiation and subsequent an-
nealing. Figure 1 shows the evolution of the converter’s efficiency as a function of TID. The initial
efficiency drop and subsequent recovery at higher TID correlate well with the leakage current of the
LDMOS as measured on individual evaluation transistors. The antagonist contribution of charges trapped in the oxide and of interface states explains this evolution, already observed in other low-voltage technologies [3]. This suggests that the high dose rate irradiation used in our test (300 Mrad in about 4 days) is an absolute worst case, and that in the real application the efficiency decrease will be smaller.

Proton irradiation has been performed at the CERN IRRAD1 facility (24 GeV/c), on unbiased converters at room temperature, to evaluate the effect of displacement damage. Neither the functionality nor the efficiency of the samples is sensibly affected by irradiation up to the maximum fluence of $5 \times 10^{15}$ p/cm$^2$.

Possible sensitivity to Single Event Effects (SEE), and in particular to destructive SEB, has been measured at the Heavy Ion beam of UCL-CRC (Louvain-la-Neuve, Belgium). The use of a high penetration ion cocktail, where the minimum range of ions in silicon is about 80 $\mu$m, ensures a large charge deposition in silicon below the 5 layers of metallization used for our prototypes. This deep range also guarantees that the charge deposition is much larger than for an ion with equivalent Linear Energy Transfer (LET) locally created in the ASIC by nuclear interaction, which is the mechanism inducing SEEs in our application. During the test, two functional DCDC35B samples are exposed to the heavy ion beam, both with and without the presence of a load resistor (output current of 0 or 0.5 A). The input voltage is increased up to 12 V, and two different heavy ion species are selected for an LET of 21 and 31 MeVcm$^2$mg$^{-1}$. Statistical significance is ensured by increasing the ion flux and integrating it over tens of minutes: more than 200,000 ions with LET of 31 hit the on-chip LDMOS transistors when an input voltage of or above 10 V is applied. The continuous monitoring of the output voltage (2.5 V) during the full exposure does not reveal any anomalous behavior. The circuits are fully functional during and after irradiation, indicating that LDMOS in this technology are very resilient to SEB — certainly well enough for our application.

Given the relatively large number of samples available, and the solidity of the circuit, the DCDC35B converter has been largely used in system-level tests by groups working on the upgrade of both the CMS and ATLAS tracker detectors.

2.2 The DCDC25A converter prototype

At the end of the radiation tests on the semiconductor technologies mentioned in 1.1, subsequent to the DCDC35B design, prototyping activity is moved to the higher performance 0.25 $\mu$m process. A first converter in this technology, DCDC25A [4], uses different polarity transistors as switches: an N and a P-channel LDMOS of generation 2A. An additional voltage needs hence to be provided to the chip to correctly drive the PMOS transistor (at Vin-2.5 V). DCDC25A integrates the control loop with a sophisticated handling of the dead times during the switching of the power transistors and a simple soft start circuitry, but requires external voltages to be provided to power the control circuitry (2.5 and Vin-2.5 V) as well as the bandgap reference voltage. It also does not include any protection feature. Unfortunately, due to a misunderstanding in the organization of the first MPW run in this very young technology, only a handful of working samples have been delivered, packaged in sealed plastic packages. For this reason the DCDC25A prototype has not been radiation tested.

The electrical performance of the samples is excellent, the converters being able to provide a stable output voltage in a very wide range of operational conditions: input voltage in the range of
5–11 V, output currents up to 3 A, switching frequency of 0.5 to 3.5 MHz, inductance values of 200–700 nH. A detailed extraction of the different contributions to the losses (affecting the efficiency) allows for the creation of a model to predict the converter’s efficiency in any condition. Figure 2 shows how the predicted values are well in agreement with the measurements over a large range of output voltages. It is also possible to see that the efficiency for stepping-down the voltage from 10 to 2.5 V reaches about 83–84%, an excellent value when considering the large losses on the air-core inductor. Again, the contribution of the parasitic resistance linked to the packaging technology used (QFN48 packages) is not negligible and better results could be reached in a final implementation with a more sophisticated packaging. Due to the superior performance of the LDMOS in this technology, and to a more careful optimization work in the design, the efficiency over the full range is higher than for DCDC35B, and in particular at high frequency (above 1.5 MHz) and for small inductance values.

2.3 The DCDC25B converter prototype

Just before the design of a second and improved prototype (DCDC25B) in the same technology, the Foundry introduced LDMOS transistors of generation 3, with unknown radiation performance, as replacement to those from generation 2A and/or 2B. As a consequence, the new prototype uses N and P-channel LDMOS of generation 3 and also another device not used before, the isolated N-channel LDMOS (whose source and body terminals can be biased at a potential different than gnd). DCDC25B integrates on-chip regulators to derive the required voltages (2.5 and Vin–2.5 V) from the unique input voltage (10 V) and the on-chip generation of the bandgap reference voltage. It also uses a much more sophisticated soft-start procedure and includes an over-current protection circuit. This makes the design very close to a possible final converter implementation.

The electrical performance of the delivered samples is excellent in terms of efficiency, which is even higher than for DCDC25A. However the samples are systematically failing during measurements with permanent damage of the component. This happens more often, although not
necessarily, in some specific operational condition. Detailed measurements indicate that electrical latch-up is at the origin of the failure. This mode of failure represents a real risk in synchronous converters, where a large area diode is necessarily forward biased at each switching cycle and this can inject large currents in the substrate. However, it is not observed in DCDC25A indicating a possible important difference between the generation 2 and 3 LDMOS. Design techniques to reduce the current injection are known, but they need to be tuned to the specificities of each technology. It should be added that anyway this electrical problem is not the only element preventing the use of generation 3 LDMOS for our application.

If during X-ray irradiation tests the functionality of DCDC25B samples is only mildly affected, unbiased proton irradiation at IRRAD1 strongly affects the converters. None of the 5 samples exposed to fluences between 1 and $10 \times 10^{15}$ p/cm$^2$ is operational after irradiation. The measurement of individual generation 3 LDMOS transistors irradiated with protons at the same time evidences serious degradation in the electrical performance, especially for the P-channel and the isolated N-channel devices. It appears hence that displacement damage heavily affects the electrical characteristics of generation 3 transistors. Moreover, heavy ion irradiation of dedicated test structures of generation 3 LDMOS transistors performed again at UCL-CRC reveals a strong sensitivity of the N-channel LDMOS to SEB. Burnout events are observed at an input voltage of 8V or more during exposure to heavy ions with LET of 10 MeVcm$^2$mg$^{-1}$, while no SEB is observed for the P-channels in the whole explored range of voltage (up to 13 V) and LET (up to 31 MeVcm$^2$mg$^{-1}$).

All the above points out that the generation 3 LDMOS devices do not qualify for the use in a radiation-tolerant converter ASIC. In collaboration with the foundry, we are starting a study to find out the best design option for a radiation tolerant LDMOS.

3 Conclusion

After the study of the radiation response of high-voltage transistors in 5 available technologies, 2 of them have been selected for the design of DCDC converter ASIC prototypes in the 0.25 and 0.35 $\mu$m nodes. Three such prototypes have been produced, with increasingly sophisticated features. Their electrical performance confirms the value of our design choices, and the acquisition of the competence and tools necessary for a successful development. However, the introduction of new LDMOS transistors in the 0.25 $\mu$m technology induces unprecedented problems both to the electrical (insurgence of destructive latch-up) and radiation performance of the most recent and complete ASIC. The design of other prototypes in that technology has to wait the availability of a set of LDMOS transistors satisfying our radiation requirements, and work in that direction has been started in collaboration with the Foundry. At the same time, the successful qualification of the ASIC prototype developed in the ‘backup’ 0.35 $\mu$m technology to all radiation effects (TID, displacement damage, SEB) indicates that this technology can be used for the production of a complete and fully radiation tolerant converter.

References

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