Abstract—Spiking neural networks (SNNs) have achieved orders of magnitude improvement in terms of energy consumption and latency when performing inference with deep learning workloads. Error backpropagation is presently regarded as the most effective method for training SNNs, but in a twist of irony, when training on modern graphics processing units (GPUs) this becomes more expensive than non-spiking networks. The emergence of Graphcore's Intelligence Processing Units (IPUs) balances the parallelized nature of deep learning workloads with the sequential, reusable, and sparsified nature of operations prevalent when training SNNs. IPUs adopt multi-instruction multi-data (MIMD) parallelism by running individual processing threads on smaller data blocks, which is a natural fit for the sequential, non-vectorized steps required to solve spiking neuron dynamical state equations. We present an IPU-optimized release of our custom SNN Python package, snnTorch, which exploits fine-grained parallelism by utilizing low-level, pre-compiled custom operations to accelerate irregular and sparse data access patterns that are characteristic of training SNN workloads. We provide a rigorous performance assessment across a suite of commonly used spiking neuron models, and propose methods to further reduce training run-time via half-precision training. By amortizing the cost of sequential processing into vectorizable population codes, we ultimately demonstrate the potential for integrating domain-specific accelerators with the next generation of neural networks.

Index Terms—Accelerators, IPU, snnTorch, spiking neural networks

I. INTRODUCTION

REPURPOSING GPUs from graphics rendering to training deep neural networks has effectively shaped an entire decade of advances in artificial intelligence (AI) [1]–[5]. This can be attributed to the numerous processor cores in GPUs that enable high parallelization of easily decomposable instructions, which are essential for the large number of matrix operations that take place in neural networks.

But a significant discrepancy arises: the cost of training deep learning algorithms in data centers sits between 100s and 100,000s of watts, whereas brain-driven cognition is bounded to approximately 10-20 W. This gap in performance has driven the neuromorphic engineering community to explore new algorithms, architectures, circuits, and devices that apply principles of neural processing to modern neural networks [6]–[11]. Spiking neurons transmit information in voltage bursts known as ‘action potentials’, which are characterized as discrete events in many neural coding studies. As such, SNNs distribute information over time, where most neurons are dormant at any instantaneous moment in time. This reduces memory access frequency, which is one of the dominant costs in deep learning workloads [12]–[16].

When it comes to training via gradient descent, there are next to no accelerators optimized for SNN workloads. The most common uses for neuromorphic hardware are: 1) inference using fixed weights where training takes place ‘offline’, or 2) online learning using simple plasticity rules, such as spike time-dependent plasticity (STDP). If SNNs are so efficient, why are there no accelerators that can perform backpropagation on SNN models? While feedforward computation is cheap, in a twist of irony, gradient-based optimization of SNNs is less efficient than its non-spiking counterpart. There are several reasons for this drop in efficiency: 1) the time complexity of backpropagation through time (BPTT) means each time step instantiates an additional neural network. Memory usage scales linearly with time; 2) biological neurons are more complex than artificial neurons, and 3) the non-differentiability of spikes means that a direct application of automatic differentiation is incompatible with SNNs. In effect, GPUs and many accelerators have not been optimized for sequential instruction sets that are required by spiking neurons: multiply-accumulate → state update → thresholding → surrogate gradient calculations.

While the current market of accelerators are tailored to conventional DL workloads, this paper seeks to explore the use of accelerators that are better tailored for the types of operations that are characteristic of SNNs [17]–[19]. In particular, Intelligence Processing Units (IPU, Graphcore) include a feature set that are a natural fit for training SNNs via error backpropagation. By coupling highly-parallel multi-instruction multi-data (MIMD) processing to sparse, spike-based tensors, we take a stride towards extracting the benefits from DL accelerators and porting them to neuromorphic algorithms.

The contributions of this paper are as follows:

- Our SNN Python framework, snnTorch, is released for IPU compatibility using low-level, pre-compiled custom operations;
A variety of benchmarks are assessed to demonstrate up to 21.3× peak improvement in throughput over NVIDIA A100 GPUs when training SNNs; a series of corner cases are identified where GPUs converge to accelerator performance in recurrent SNNs; In much the way that brains distribute firing rates across pools of neurons, we demonstrate how the use of population codes can significantly accelerate the training process.

This paper presents the first analysis of the suitability and performance of IPUs in handling neuromorphic workloads when trained using approaches prevalent in deep learning.

II. BACKGROUND

A. Spiking Neural Networks

The adoption of deep learning-based techniques to training SNNs can be dated back to 2002, when Bohte et al. treated the firing time of a spiking neuron as a trainable, regression problem [20]. Since the advent of CUDA-accelerated Python packages with built-in automatic differentiation (autodifferentiation) engines (e.g., PyTorch [21], Tensorflow [22], JAX [23]), the broader approach in recent years has been to apply a generalized backpropagation algorithm to an unrolled computational graph of spiking neurons (Figure 1(a-b)) [24]–[29]. BPTT adopts techniques used to train recurrent neural networks (RNNs), where sequences are instead interpreted as discrete time-steps of finite duration [30], [31].

While a variety of detailed models are used to accurately emulate biological neurons, the simplest models are more commonly used in large-scale simulations. This can be attributed to several reasons: i) calculating the solution is computationally cheap, ii) simplifying an action potential to a single-bit event promotes sparse computations, and iii) applying gradient descent to stiff equations (e.g., with sharp bifurcations) can lead to instability when training a network.

SNNs adopt the same topological structure as non-spiking networks. The main difference is that artificial neuron models are swapped out for time-varying spiking neurons. Time-evolution is modeled in a sequential structure. Specific details regarding the types of neuron models used are provided in the experimental results (Section IV).

B. Neuromorphic Processors

The neuromodulatory processes in the brain that leverage spikes to promote learning remain somewhat shrouded in mystery, which has inspired the development of several research-based neuromorphic processors. Two prolific examples include Loihi developed by Intel Labs [32], [33], and SpiNNaker initiated at the University of Manchester [34], [35], both of which have roused neuromorphic research ecosystems where hardware access is offered both remotely and physically to the broader research community. While such neuromorphic processors remain to be optimized for gradient-based learning, they have incited much interest in how neurobiological processes can be modelled in-silico. These processors allow users to explore how programmable learning rules can modulate plastic synapses.

The push towards data-driven benchmarks from deep learning has led to the adoption of gradient-based learning rules to be used with SNNs, which is far better suited for non-convex optimization, but demand far more computational resources when compared to biophysically motivated learning rules. Training SNNs via gradient descent compounds upon several challenges:

- **Temporal Credit Assignment**: The BPTT learning rule requires storage of all gradients over time, where memory complexity scales with $O(nT)$ where $n$ is the number of neurons and $T$ is the duration of time.
- **Weight Credit Assignment**: Routing gradients from the network’s output back to plastic synapses requires the data path of the forward operation to be stored. The
gradient of every synapse has an independent pathway, which scales the cost of communicating gradients to apply weight updates.

- **Non-differentiable operations:** In leaky integrate-and-fire neuron models, a hard threshold is often applied to the membrane potential to elicit a voltage spike at the axon. This is a non-differentiable operation, and thus, incompatible with gradient descent.

1) **Temporal Credit Assignment:** The temporal credit assignment problem can be addressed by adopting real-time recurrent learning (RTRL) techniques, to avoid having to store gradients in time [36]. The cost of doing so is that memory complexity now scales with $O(n^3)$, where the cubic term discourages broad adoption in large-scale networks. Approximations of RTRL recently inspired the development of a lightweight SNN training accelerator for fixed, dense architectures [37], [38].

2) **Non-differentiable Operations:** Surrogate gradient descent is used to bypass non-differentiable operators, where the final calculated gradients are a sufficient approximation [6], [39]. This adds to computational cost, as analytical methods to computing derivatives (e.g., dual numbers [40]) must be supplemented with manually-determined heuristics (surrogate gradients); i.e., training SNNs via surrogate gradients is not as modular as non-spiking networks.

3) **Low-cost Inference:** The high cost of training SNNs using non-local learning algorithms can be partially offset by the incredibly cheap cost of using SNNs in solely feedforward operations. It has been shown that SNNs can offer 2–3$\times$ orders of magnitude improvement over non-spiking alternatives [13]. In general, this motivates offline training of SNNs typically using GPUs, where deployment can take place on low-power SNN accelerators. Several recent studies have leveraged programmable microcode of neuromorphic research processors to adopt BPTT variants on a single chip [41], [42]. At present, these methods are constrained to fixed neuron models and network architectures, not yet generalized to convolutional networks. Despite these limitations, such methods offer a promising alternative for online deployment of BPTT-like training of SNNs to what we propose here. Rather than taking BPTT to processors optimized for SNNs, we use IPUs to compile and train SNNs using accelerators optimized for backpropagation.

C. **Intelligence Processing Units**

IPUs are designed to facilitate deep learning workloads by processing fine-grained operations across a large number of parallel threads. The ability to process individual threads on sub-blocks offers a two-fold benefit on SNN workloads over single-instruction-multiple-data/thread (SIMD/SIMT) GPUs: i) instructions from different network layers can be concurrently processed, where the constraints of contiguous vectorized data is no longer a performance bottleneck, and ii) MIMD processing can accelerate applications with irregular and sparse data access without incurring performance degradation. This is optimal for spike-based workloads which include additional processing overhead in computing the state-driven dynamics of spiking neuron models (Figure 1c-d).

Each IPU Mk2 core consists of 1,472 high performance processor cores, where each processor core and a locally accessible in-processor memory unit form a tile. The IPU tile contains six processor threads, totaling 8,832 processor threads when operating in parallel. This amounts to a total of roughly 900 MB of memory and 250 TeraFLOPS of compute for the Mk2 GC200 IPU hardware which ran the experiments on this paper. Each core is connected directly to the IPU-Exchange, which is capable of transferring 8 TBps of data between IPU tiles. There is no global memory, and specialized hardware is incorporated for common neural network operations, such as convolutions and matrix multiplications.

IPUs follow a graph processing pipeline where programs are compiled into a logical execution graph. This graph is composed of alternating state and computation vertices. Each vertex consists of machine instructions that can execute in parallel, provided they write to independent parts of a tensor. Upon completion of a compute step, data is exchanged between tiles as part of the exchange phase of the bulk synchronous parallel (BSP) execution model.

Adopting this BSP execution model benefits bandwidth-limited neural network, as overlapping memory-bound computation and communication can lead to bandwidth contention and data collision [43], [44]. BSP eliminates the need for message buffers and global memory, though as a result, all inter-core communication must be planned during model compilation [45]. In practice, once the model has been compiled once, it can be cached and subsequently reused.

D. **snnTorch**

A variety of gradient-based SNN libraries have been open-sourced, most of which are written in Python for syntactical ease, and several of which are built on top of commonplace deep learning packages [25], [46]–[50]. Most approaches compose primitive functions together wrapped as a spiking neuron node, where gradients are analytically calculated using reverse autodifferentiation in the backend. As spikes are represented as discontinuous voltage bursts, they are non-differentiable. PyTorch allows users to override gradients with custom functions, and so has become a common backend for the implementation of surrogate gradient descent in SNNs [6], [39].

`snnTorch` is adopted as the toolbox because it is: i) designed with PyTorch as its backbone, so pre-existing interfaces can be used to lower composable PyTorch functions into IPUs, ii) several features are unique to `snnTorch` in the context of gradient-based learning, such as using population-based embeddings to accelerate the training process, and iii) quantization-aware training has been integrated into the state-space of spiking neuron models, which can be used in mixed- and low-precision accelerators.

Several alternative options are available for accelerating SNNs using CUDA-based libraries. **SpikingJelly** provides a CuPy backend [48]. **GenN** uses CUDA-generated code to implement an approximate form of BPTT [38], [51], and **lava/dl** incorporates the most commonly used functions/neurons as optimized CUDA code, while other libraries mostly depend on the deep learning package’s CUDA acceleration.
To summarize, prior approaches for faster gradient-based training of SNNs include:

- Utilizing microcode to enable neuromorphic processors to track gradients.
- Using custom CUDA backends to accelerate SNNs on GPUs, and
- Using pre-existing interfaces to CUDA via pre-existing deep learning libraries (e.g., PyTorch).

The first option is burdened with instruction set-level definitions that must be tailored for a given network architecture, and the latter two are limited by SIMD/SIMT processing. We take a wholly different approach by adapting Python-level SNN descriptions that leverage low-level, pre-compiled operations customized to an IPU accelerator harnessing MIMD architectures. This approach to distributed memory amongst IPU cores can be used to reduce data movement, thus amortizing the costs of weight and temporal credit assignment.

### III. METHODS

#### A. Neuron Models

1) **Leaky Integrate-and-Fire Neuron**: The dynamics of a leaky integrator neuron are as follows [52, 53]:

\[
\tau \frac{du}{dt} = -u + iv,
\]

where \( u \) is the membrane potential of the neuron, \( i \) is the current injection to the neuron, \( r \) is the equivalent resistance of the ion channels of the neuron, \( \tau = rc \) is the time constant of the passive membrane. Equation 1 can be solved using the forward Euler method:

\[
u_t = \beta u_{t-1} + (1 - \beta) i_t,
\]

where \( \beta = e^{-1/\tau} \) is the inverse time constant of the neuron membrane potential, and the subscript \( t \) refers to time. When the membrane potential exceeds the threshold \( u_{thr} \), an output spike is generated:

\[
z_t = \begin{cases} 1, & \text{if } u_t > u_{thr} \\ 0, & \text{otherwise.} \end{cases}
\]

To introduce learnable parameters, the current injection term is replaced with a weighted input \((1 - \beta)i \leftarrow wx\). For notational brevity, the contribution of a single weighted input is used:

\[
u_t = \beta u_{t-1} + wx_t - z_{t-1} u_{thr},
\]

The final term introduces a reset mechanism to the neuron. The unrolled computational graph depicting the operation of the neuron is shown in Figure 2(a).

2) **Current-based Leaky Integrate-and-Fire Neuron**: If the leaky integrate and fire can be thought of as a low-pass filter, the current-based method can be thought of as a pair of low-pass filters. The input synaptic current is modeled as an AMPA-receptor with a rapid rise time and gradual decay, which then modulates the membrane potential of the neuron:

\[
i_t = \alpha i_{t-1} + wx_t,
\]

\[
u_t = \beta u_{t-1} + i_t - z_{t-1} u_{thr},
\]

where \( \alpha = e^{-1/\tau_{syn}} \) is the inverse time constant of the synaptic current, and \( \tau_{syn} \) is the equivalent time constant of the synaptic current in an analogous way to \( \tau \), with the computational graph illustrated in Figure 2(b).

3) **Recurrent Spiking Neurons**: Both of the above neuron types can be adapted to include explicit recurrent connections. The output spikes are weighted and appended to the input. Formally, a recurrent leaky integrate-and-fire neuron is represented by:

\[
u_t = \beta u_{t-1} + wx_t + z_{t-1}(v - u_{thr}),
\]

where \( v \) is the recurrent weight.

#### B. Custom Operations on IPUs

The ‘Poplar SDK’ interfaces popular deep learning frameworks directly into IPU programming. The IPU uses an autodifferentiation engine independently of PyTorch’s backend, and as such, spiking neuron models that depend on surrogate gradient descent are not compilable by default. Custom operations must be written in C++ and pre-compiled into machine-level codelets that are accessible to users via Python.

Our approach pre-compiles the surrogate gradient operator at the time \( snnTorch \) is imported. A custom operation is defined for the threshold-shifted Heaviside function (see (3)) implemented in C++, which is compiled thus generating a shared library object that can be dynamically linked in Python at runtime. This allows for the IPU-build of \( snnTorch \) to be syntactically near identical to CPU/CUDA-based usage, abstracting away machine-level complexities from the user. The surrogate gradient operator is co-located in the same

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**Algorithm 1 Using Custom Operations with IPU**

**Require:** Custom operation defined in C++

**Require:** Makefile used to generate the Shared Object

**Require:** Custom operation’s shared object

1. Define custom operation in a C++ file
2. Use the Makefile to generate the shared object
3. Load the Custom Operation’s Shared Object.
IPU core which reduces the impact of non-modular function calls that are needed when overriding the autograd module in PyTorch. This is sequenced via pseudo-code in Algorithm 1 and illustrated in Figure 3.

Specifically, (3) is a non-differentiable function. This function is replaced in the backward pass with the user’s choice of approximation. For example, a straight-through-estimator simply bypasses the non-differentiable operator [54]. Alternative approaches use functional approximations of the Heaviside operator by smoothing out the discontinuous step, e.g., the fast-sigmoid function:

$$\tilde{z} = \frac{(u - u_{thr})}{(1 + |u - u_{thr}|)}$$

$$\frac{\partial z}{\partial u} \leftarrow \frac{\partial \tilde{z}}{\partial u} = \frac{1}{(1 + |u_{thr} - u|)^2}$$

where the left-arrow denotes substitution, and the tilde in \(\tilde{z}\) represents an approximation.

C. Network Architecture

For this paper, two network types were tested on four different types of hardware. The hardware tested include: the NVIDIA A100, NVIDIA V100, NVIDIA GTX 1080, and the Graphcore IPU Mk2. The networks tested are designed to fit a single processor to avoid comparisons that are I/O-limited. The architectures include: a 3-layer dense SNN (DSNN) and a 3-layer convolutional SNN (CSNN). Despite the small size of the networks, these were trained over multiple time steps which led to near-full memory utilization. Leaky integrate-and-fire neurons are used for all experiments unless otherwise specified, and most spiking simulations are performed across 25 time steps. For experiments measuring throughput, the MNIST dataset is used in the interest of speed [55]. For experiments that account for loss-based metrics (e.g., accuracy), CIFAR-10 is used [56]. The various architectures used are specified in Table I. 5C12 refers to a 5 × 5 convolutional kernel with 12 channels. MP2 refers to a 2 × 2 max-pooling operator. Unless otherwise specified (e.g., in experiments that sweep across different architecture parameters), these networks are used for the experiments that follow with the AdamW optimizer used in all cases [57]. Where relevant, experiments were repeated five times to generate error bars.

## IV. Experimental Results

The following experiments have been conducted to benchmark IPU performance:

- Baseline FLOPS (floating point operations per second)
- Baseline Throughput
- Throughput across batch sizes
- Throughput across architectures
- Throughput across neuron models
- Compute time spent on spiking vs. static dynamics
- Mixed precision throughput
- Population coding: throughput and accuracy
- Power usage per operation

All experiments that follow account for the entire training process using BPTT, including the forward-pass, gradient calculation, and weight update.

### A. Baseline FLOPS

Before performing IPU vs. GPU performance comparisons, we first assess the performance of a spiking network against equivalent, non-spiking artificial neural networks (ANNs) on the IPU. One FLOP is defined as one fused multiply-add floating point operation, calculated using the fivcore Python Library. The FLOP comparison can be seen in Table I. On average, the IPU improves TFLOPS by 4.6× when compared to the A100, 6.4× over the V100, and 10× over the GTX1080.

Interestingly, the performance of the spiking network is marginally better for the dense case than the non-spiking network. This may be because the IPU has been optimized for handling different types of concurrent operations, where processing neuron state-based computations are relatively simple operators when compared to large-scale matrix-vector multiplication. On the other hand, the TFLOPS when running the convolutional SNN drops by approximately 57% from non-spiking to spiking networks on the IPUs.

### Table I: Network Architecture

| Network | Architecture |
|---------|--------------|
| DSNN    | 784–1000–10  |
| CSNN    | 5C12–MP2–5C64–MP2–10 |

Fig. 3. Data path of input tensors on GPU and IPU. (a) GPU: One instruction is applied to all elements of an input tensor while spiking neuron state and surrogate gradient computations are stalled in the instruction pipeline. (b) IPU: Spiking neuron state and surrogate gradient computations are pre-compiled into machine-level codelets, and concurrently processed with the neural network (NN) matrix-vector-multiplication step.
### TABLE II
SNN VS ANN TFLOPS (TRAINING)

| Network Type | IPU   | A100  | V100  | GTX1080 |
|--------------|-------|-------|-------|---------|
| DNN          | 1.02  | 0.22  | 0.16  | 0.10    |
| DSNN         | 1.04  | 0.22  | 0.16  | 0.10    |
| CNN          | 3.24  | 0.70  | 0.51  | 0.33    |
| CSNN         | 1.85  | 0.40  | 0.29  | 0.19    |

### TABLE III
DSNN THROUGHPUT

| Metric | IPU   | A100  | V100  | GTX1080 |
|--------|-------|-------|-------|---------|
| Average Power | 92.12W | 60.51W | 55.71W | 49.29W  |
| Average Throughput (images/s) | 46297.17 | 9858.92 | 7207.24 | 4639.89 |
| Throughput/Watt | 502.59 | 162.93 | 129.4 | 94.4 |

### TABLE IV
CSNN THROUGHPUT

| Metric | IPU   | A100  | V100  | GTX1080 |
|--------|-------|-------|-------|---------|
| Average Power Used | 92.37W | 68.86W | 61.99W | 55.44W  |
| Average Throughput (images/s) | 15566.16 | 5608.43 | 3883.89 | 2635.54 |
| Throughput/Watt | 168.16 | 81.44 | 62.65 | 47.54 |

### B. Baseline Throughput

Throughput is measured in terms of 1000s of images per second, and accounts for the wallclock time commencing from the forward pass, the backward pass, and concludes once the weight update is completed. A batch size of 128 images is used by default. Each network is trained over 60 epochs. To obtain error bars, this is repeated 20 times on each hardware. The throughput is calculated by:

- measuring the wallclock time to process one minibatch,
- dividing the batch size by the wallclock time.

1) DSNN Throughput: The results from the DSNN are tabulated in Table III. The IPU can train an average of 46,297 images per second, which is 3.1× higher than the A100, 6.4× higher than the V100, and 9.9× higher than the GTX1080. Error bars across multiple trials are illustrated in Figure 4(a). The standard deviation for the IPU is approximately 3,623 images.

2) CSNN Throughput: With respect to the CSNN, there is a much larger number of computations being performed leading to a decrease in throughput for both IPUs and GPUs. The IPU training throughput is 15,566 images per second. This is 2.1× more than the A100, 4× higher than the V100, and 5.9× greater than the GTX1080. The standard deviation for the IPU is approximately 3,623 images.

### C. Throughput Across Batch Size

As networks increase in size, memory limits constrain the maximum possible batch size that is permissible. This problem is exacerbated in SNNs which also consume memory for each additional simulated time step. To measure this effect, the batch size was swept from 8 to 128, with throughput results shown in Figure 4(b). On inspection, there is far less variance in performance for IPUs. This is especially important where a large number of time steps must be simulated, and the maximum batch size decreases. Close attention is given to the smallest tested batch size, as real-world batch sizes in continual learning workloads are ‘1’. For the smallest tested batch size (n = 8), the performance improvement of the IPU over the A100 for both CSNN and DSNN is more than one order of magnitude (14×).

### D. Throughput Across Architectures

Network architecture is varied for both the DSNN and CSNN and throughput is measured. For the DSNN, the number of neurons in the hidden layer is increased, and for the CSNN, the kernel depths of the first two convolutional filters are increased.

1) DSNN Throughput: GPUs are completely insensitive to increasing the number of neurons, as shown in Figure 5(a). This indicates that for a small network, a large number of cores available are underutilized. On the other hand, the margin of improvement with the IPU increases with smaller networks. This is because different operations can be parallelized to improve utilization of the large number of IPU cores available.

2) CSNN Throughput: The throughput of varying CSNN architectures is illustrated in Figure 5(b). In contrast to DSNNs, larger convolutional kernels decrease the throughput of GPUs. The larger number of computations involved in convolutions indicates that the GPU cores are now fully utilized.
E. Alternative Neuron Models

Several other spiking neuron models are increasing in usage in the context of SNNs. Recurrent spiking neuron models, e.g., (7), have been shown to achieve better performance on datasets with temporal complexity [59]. Current-based neuron models, e.g., see (5) and (6), are better suited for learning precise spike timing, as the membrane potential trace is differentiable with respect to time. Throughput for a recurrent SNN is shown in Figure 6(a), and that of an SNN composed of current-based neurons is shown in Figure 6.

The performance of V100s remains relatively unaffected by more complex neuron models, which causes the performance gap with IPUs to narrow. This highlights a potential opportunity to improve resource allocation during compilation. There are more steps to process these more exotic neuron models, and so more cores are allocated to handling those operations. This comes at the cost of less resources available to process synaptic operations, where computational complexity scales with $O(n^2)$.

F. Spiking vs. Static Dynamics

To verify the above theory, the ratio of time spent calculating the dynamics of spiking neurons (i.e., solving (3) and (4)) is compared against the amount of time spent on matrix-vector multiplication. The results are shown in Figure 7(a), demonstrating that IPUs provide better balance between neuronal and synaptic operations. In the CSNN, the amount of compute time allocated to solving state-driven dynamics is exactly equivalent to the duration of time spent on synaptic operations. This is beneficial for simple neuron models, but where more complex neurons are concerned, may require further optimization during compile time. Further improvements could be obtained by exploiting function outlining which merges repeatable code-blocks for execution on identical cores in IPUs. This can reduce the overhead allocated to solving state dynamics, and free up more cores to run synaptic operations.

G. Mixed Precision Performance

Mixed precision training reduces the bit-width needed for computation, which comes with an associated wallclock time reduction. This is often with minimal, if any, impact on network performance. The default full precision (32b) mode is compared to half precision (16b) training, with results shown in Figure 8(b). The difference for all cases is marginal because gradients continue to be calculated in full precision.

V. ACCELERATION USING POPULATION CODES

A. Biological Plausibility

At present, the most common approach to determining the predicted class is to select the neuron with the highest firing count. This is equivalent to using a rate coded SNN. In neurophysiology, it is thought that rate codes alone cannot be the dominant encoding mechanism in the primary cortex. One of several reasons is because the background neuronal firing rate is roughly 0.1 – 1 Hz, which is far slower than the reaction response time of animals and humans.

But if multiple neurons are grouped with their collective spikes counted cumulatively, then it becomes possible to measure a firing rate for a population of neurons in a very short window of time. Assigning a population of neurons to individual classes is also known as using a ‘population code’. Population coding adds credibility to the biological plausibility of rate-encoding mechanisms.

B. Population Codes in Unsupervised Learning

In the past, it has been common practice to increase the number of neurons at the output layer of a network, and cluster the response of various neurons together. This practice has been limited to networks trained using spike timing-dependent plasticity. Neurons would be assigned classes based on which assignments led to the highest accuracy. As such, using a
population code where multiple neurons were assigned per class typically led to a boost in classification accuracy in unsupervised learning tasks. This is because more neurons means more permutations of neuron assignments that can increase accuracy. The shift from unsupervised learning to gradient-based supervised learning has made population codes a diminishing practice when training SNNs, as targets are pre-assigned before training commences. We find that using population codes offers alternative benefits when training SNNs.

C. Population Codes in Gradient-based Learning

These benefits are grounded in the fact that accelerators are optimized for parallel operations rather than sequential operations. Using a population of neurons redistributes the time cost over space instead, i.e., larger dimension matrix-vector multiplications can be used instead of repeatedly applying matrix-vector multiplications with smaller dimensions. We run a series of experiments to show population codes further accelerate throughput with a marginal impact on accuracy. Because accuracy is now of interest, we assess performance on the CIFAR-10 dataset as MNIST is broadly recognized as being too simple.

1) Experimental Setup: Similar network architectures as described in Table I are used. For the DSNN, the number of input neurons is increased due to the larger dimensionality of the CIFAR-10 dataset (32×32×3) over that of the MNIST dataset (28×28×1). The same holds true for the terminal layer of the CSNN.

2) Training Throughput: A comparison of throughput across various output neurons and with different precision (half and full) are shown in Figure 8. One single simulation time step is used. Performance follows a very similar trend to that of varying network architectures in Figure 3 where GPUs perform identically as the output population increases. At the IPU’s best, optimal throughput is approximately 145,000 images per second. This is 37× better than the original baseline performance (despite using bigger images with 3 channels), and approximately twice as fast as the best GPU. At its lowest throughput, performance of the IPU and A100 converges in the DSNN experiment. When population codes are applied to CSNNs, the A100 skyrockets in performance and becomes invariant to architectural changes. The large number of terminal synaptic operations dominates the total cost of the network, completely outweighing state-based neuronal operations. This places the A100 in the lead in population-based CSNN benchmarks.

3) Accuracy: As a coarse-grain measure of accuracy, the DSNN model was used to provide an idea as to how population codes impact training performance. The DSNN is trained over 5 epochs to determine whether it is possible to train networks in one single time-step, where each neuron is constrained to only firing a maximum of once. Results are illustrated in Figure 9, where a baseline accuracy of 52.2% is obtained without using population codes (i.e., 10 output neurons simulated over 25 time steps). This accuracy is almost reached when 500 output neurons are used, assigning 50 output neurons per class. As a matter of interest, indefinitely increasing the output neuron count does not continue to increase performance. Based on prior approaches to constructing models, network depth should be increased commensurately to network width to avoid leaning towards either end of the bias-variance trade-off [60].

We note that the target here is not state-of-the-art accuracy, but rather, to assess whether single time-step learning is possible at all. Our results indicate that equal performance to multiple time-steps can be met by using population codes, verified on a simple DSNN architecture.

VI. OUTLOOK AND CONCLUSION

SNNs and conventional neural networks have overlapping features that can be concurrently optimized, and IPUs have demonstrated promising suitability for most operations that are characteristic of training SNN workloads. We flip the conventional approach to ASIC-driven SNN training by tailoring pre-compiled microcode to a domain-specific accelerator, rather than reconfiguring neuromorphic chips to handle back-propagation approximations on fixed network architectures. Our results show promising performance gains (throughput, TOPS/W, accuracy) can be made by porting the advances made in deep learning accelerators to SNNs. We also indicate the types of hardware optimizations that benefit gradient-based learning in SNNs, such as MIMD processing, functional outlining, and balanced compilations of neuronal and synaptic operators, and how population encoding can be used to better utilize parallelism across both IPUs and GPUs. These features together enable high performance training and inference speeds with IPUs on SNNs.

All code used to generate these results is made openly accessible to enable the research community to accelerate their own custom SNNs on IPUs, and can be installed via PyPi. Population encoding has been integrated into snnTorch, with a corresponding interactive notebook that enables users to train population encoded SNNs on both IPUs and GPUs alike.

CONFLICT OF INTEREST

A. Titterton, A. Gopiani, and T. Santos are employees at Graphcore. The remaining authors have no conflicts of interest to declare.

1URL: https://snntorch.readthedocs.io/en/latest/tutorials/tutorial_pop.html
[46] J. C. Knight, A. Komissarov, and T. Nowotny, “PyGeNN: a Python library for GPU-enhanced neural networks,” *Frontiers in Neuroinformatics*, vol. 15, p. 659005, 2021.

[47] J. K. Eshraghian, M. Ward, E. Neftci, X. Wang, G. Lenz, G. Dwivedi, M. Benamoun, D. S. Jeong, and W. D. Lu, “Training spiking neural networks using lessons from deep learning,” *arXiv preprint arXiv:2109.12894*, 2021.

[48] W. Fang, Y. Chen, J. Ding, D. Chen, Z. Yu, H. Zhou, Y. Tian, and other contributors, “Spikingjelly,” [https://github.com/fangwei123456/spikingjelly](https://github.com/fangwei123456/spikingjelly) 2020, accessed: YYYY-MM-DD.

[49] H. Hazan, D. J. Saunders, H. Khan, D. Patel, D. T. Sanghavi, H. T. Siegelmann, and R. Kozma, “Bindsnet: A machine learning-oriented spiking neural networks library in python,” *Frontiers in neuroinformatics*, vol. 12, p. 89, 2018.

[50] C. Pehle and J. E. Pedersen, “Norse - A deep learning library for spiking neural networks,” Jan. 2021, documentation: [https://norse.ai/docs/](https://norse.ai/docs/). [Online]. Available: [https://doi.org/10.5281/zenodo.4422025](https://doi.org/10.5281/zenodo.4422025).

[51] J. C. Knight and T. Nowotny, “Efficient GPU training of LSNNs using eProp,” in *Neuro-Inspired Computational Elements Conference*, 2022, pp. 8–10.

[52] P. Dayan and L. F. Abbott, *Theoretical neuroscience: Computational and mathematical modeling of neural systems*. MIT press, 2005.

[53] L. Lapicque, “Recherches quantitatives sur l’excitation electrique des nerfs traitée comme une polarization.” *J. of Physiol. and Pathology*, vol. 9, pp. 620–635, 1907.

[54] G. Hinton, N. Srivastava, and K. Sehwag, “Neural networks for machine learning, 2012,” *Coursera, video lectures*, 2012.

[55] Y. LeCun, “The mnist database of handwritten digits,” [http://yann.lecun.com/exdb/mnist/](http://yann.lecun.com/exdb/mnist/), 1998.

[56] A. Krizhevsky, G. Hinton *et al.*, “Learning multiple layers of features from tiny images,” *Technical Reprt*, 2009.

[57] D. P. Kingma and J. Ba, “Adam: A method for stochastic optimization,” *arXiv preprint arXiv:1412.6980*, 2014.

[58] G.-q. Bi and M.-m. Poo, “Synaptic modifications in cultured hippocampal neurons: dependence on spike timing, synaptic strength, and postsynaptic cell type,” *Journal of neuroscience*, vol. 18, no. 24, pp. 10 464–10 472, 1998.

[59] N. Perez-Nieves, V. C. Leung, P. L. Dragotti, and D. F. Goodman, “Neural heterogeneity promotes robust learning,” *Nature communications*, vol. 12, no. 1, pp. 1–9, 2021.

[60] S. Zagoruyko and N. Komodakis, “Wide residual networks,” *arXiv preprint arXiv:1605.07146*, 2016.