Investigation of drain current transient behavior in SLS TFTs with the DLTS technique

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Abstract. In this work, the study of drain current overshoot transients of thin film transistors (TFTs) fabricated by excimer laser sequential lateral solidification (ELA SLS) process is presented. Drain current transient behavior, is ascribed to carrier capture/emission processes within the transistors’ Si body, and represents complex mechanisms differently responding at dark and under illumination conditions. Additionally, the thickness of the Si body film, which is an important parameter for the material structure evaluation, ranged from 30nm to 100nm. The results were stemmed by deep level transient spectroscopy (DLTS) technique and measurements were conducted within the temperature interval of 200K to 400K. The impact of illumination, contributes mainly at lower temperatures through electron-hole generation processes, compensating though carrier freeze-out phenomena.

1. Introduction
Polysilicon thin film transistors (TFTs) are key pixel switching elements for active-matrix liquid-crystal displays (AMLCDs). TFT fabrication is based on non-refractory substrates, such as glass or plastic that limit the maximum allowed processing temperature. In the near future, a complete computer system fabricated on such substrates by excimer laser re-crystallization, the so-called system-on-panel, is rendered more than a promising prospective [1]. The study of the electrical properties of TFTs, is considered an important step for device scalability as well as for high-resolution applications. Although the static characteristics have been extensively investigated, the available information on the transient behaviour is of restricted range. The novelty of the present work is to demonstrate evidence for the drain current transient behaviour of the TFTs, under dark and illumination conditions. This behaviour will be ascribed to the carrier capture/emission mechanisms within the Si-body film.

2. Experimental
Polysilicon TFTs were fabricated in films formed by crystallization of amorphous silicon. The initial hydrogenated a-Si films (a-Si:H) were deposited at 320°C by plasma enhanced chemical vapor deposition (PECVD) on quartz substrates. The film thickness ranged from 30nm to 100nm. After deposition, the a-Si:H films were subjected to a dehydrogenation annealing step, at 500°C for 2h in
nitrogen ambient, to remove the excess hydrogen. The resulting a-Si films were transformed to polysilicon ones by excimer laser annealing (ELA), using the sequential lateral solidification process (SLS). This process results in a polysilicon film composed of long crystal domains (grains) [2], separated by roughly parallel grain boundaries [3].

All the devices were floating body (FB), n-channel MOSFETs, fabricated using a non-self-aligned top metal gate structure. The devices were aligned so that the grains be parallel to the direction of drain current conduction. The gate dielectric was a 100nm thick PECVD SiO₂ film. The intrinsic active region of all TFTs (width x length) was 200µm x 8µm.

The static characteristics of the transistors were extracted using a Keithley 236 SMU in order to monitor the drain current, and a Keithley 6487 pico-ammeter/voltage source which provided the gate bias and measured the gate current. The I DS-VGS transfer characteristics were recorded at 300K with V DS=50mV and V GS swept from –5V to +5V. The slope of a line fitted to the I DS-V GS curve at the point of maximum transconductance, and the intercept of that line on V GS axis, yielded the extrapolated threshold voltage. The subthreshold slope was extracted from the maximum slope of the I DS-V GS characteristic, drawn in semilog scale. The subthreshold swing was used to calculate the deep trap states density in the vicinity of the intrinsic Fermi level.

The DLTS assessment was based on recording drain current transients ΔI D(t) immediately after the device transition from on- (accumulation) to off- (strong inversion) state, under dark and under white illumination conditions. The duration of the off-state was kept constant at 100msec. All measurements were carried out in the linear region of MOSFET operation (50mV between drain-source terminals), in order to prevent further ageing of the devices. The DLTS experimental infrastructure, consisted of an SR570 current amplifier which also provided the drain bias, and DAQ card which digitized the drain signal. The drain current was sampled in the 0-256ms time interval with a 1ms sampling rate. All the DLTS measurements were performed with the devices placed in a liquid nitrogen cryostat and the temperature was controlled in the range of 200K to 400K. The switch-on transients were recorded and stored under thermal equilibrium conditions at every 1K step.

3. Results and discussion

The existence of grains in Si-body films introduce localized states, underneath grain boundaries, statistically distributed in energy over the energy gap. These states are positively or negatively charged according to whether are donor- or acceptor-like and to relative position of the Fermi level. Their energy distribution follows a Gaussian formula [4]. In addition, their origin is determined by the nature of the disorder in the poly-Si bond structure such as dangling bonds, and by the local electronic potential fluctuations resulting in stress fields in the region of structural irregularities. Dangling bonds along with structural strain produce an inhomogeneous broadening of the discrete levels in the gap [5].

3.1. ELA SLS TFTs with 50nm-thick Si-body

The drain current transients ΔI D(t) of 50nm-thick TFTs are shown in figure 1. An analysis of the presenting data under dark and illumination conditions, revealed that the transient decay exhibited a multi-exponential (not a power-law) time dependence of the general form ΔI D(t) = ΣA i(T)exp(-t/τ i), with the time constants τ i fairly dependent on temperature. In figure 1, it is evident that, there is a critical temperature T max = 270K where transients of maximum amplitude are observed. However, when the transients are recorded while the sample is under illumination this effect disappears, with the magnitude of the transients monotonically decreasing with increasing temperature. We shall try to investigate the mechanisms responsible for the transient response, considering independently the carrier capture and emission processes during on-/off-state.

In a n-channel MOSFET electrons are captured during the on-state and emitted during off-state [6,7]. Electron capture process will emerge as soon as the channel is established. This process affects electron traps mainly located in the vicinity of the channel, rather than deeper in the Si-body. The latter option is more complex, because electrons need to surpass the band bending barrier before they got captured.
During the on-state, the drain current will be determined by the electron trapping process and also by the mobility variation due to grain boundary potential modulation. Such a complex mechanism may be the origin of multi-exponential mechanisms, that fitted the recorded drain transient data. Since carrier emission rate decreases with decreasing temperature [8], the on-state transients vanish at low temperatures. This sequence can adequately interpret the abrupt decrease of the transient amplitude below $T_{\text{max}}$. Above $T_{\text{max}}$ the leading mechanism governing the on-state drain current transients seems to involve hole emission process [9], as it is described below.

![Figure 1. Drain current transients of 50nm-thick TFT under dark and illumination conditions.](image)

The hole contribution to the drain current transient behaviour, during the on-state, is accomplished through hole emission process. Particularly, holes are emitted during the on-state and captured during the off-state. In our case the poly-Si film is intrinsic, and hence holes before being captured must follow a preceding thermal generation process from deep states. The concentration of trapped holes in a donor-like trap will depend on both the temperature and the off-state duration. The trapped holes in bulk and interface states will decrease the potential barrier height and increase the carrier mobility. On the subsequent on-state the trapped holes will be emitted. As a result an increase of potential barrier height will occur along with a simultaneous decrease in channel carrier concentration. Consequently, above $T_{\text{max}}$, the magnitude of drain current transients will decrease.

Under illumination electron-hole pair generation occurs. The Fermi level beneath grain boundaries, splits into electron and hole quasi-Fermi levels, $E_{\text{Fn}}$ and $E_{\text{Fp}}$, respectively. The shift $\Delta E_p = E_{\text{Fn}} - E_{\text{Fp}}$ encompasses much more localized states than at steady state where $\Delta E_p = 0$ (dark), and hence more traps, especially those near the midgap, will act as efficient recombination centers [5]. Thus, the increasing recombination current via grain boundary recombination centers, leads to faster drain current transients. Therefore, for time interval less than 1msec, the amplitude of the recorded transients $\Delta I_D(t)$ decreases significantly.

3.2. ELA SLS TFTs with 30- nm-thick Si-body and 100-nm-thick Si-body

In figure 2 the transients $\Delta I_D(t)$ of 30- and 100-nm-thick TFTs are presented. They exhibit similar behaviour, under dark and illumination conditions. It is worth mentioning, that they follow the same multi-exponential time dependence as in the case of 50nm-thick TFTs. During the off-state, the rate $e_n$ that electrons are emitted by the interface states closer to the channel vicinity, obeys the general form

$$e_n \propto \frac{\sigma_n T^2}{\exp(E/KT)}$$

where $\sigma_n$ is the capture cross section of the trap, and $E$ the energy of the localized
state [8]. It is obvious that $e_v$ increases rapidly with increasing temperature. The behaviour of electron-hole pairs generation, under optical illumination, follows the scenario described in the previous paragraph, resulting in the lowering of the barrier height that grain boundary induces so. By plotting $I_d(t)$ versus $1000/T(K)$ the slope of the linear region of the curve represents an activation energy that corresponds to the height of the barrier height [10]. When the MOSFET is illuminated, this height lowers [5]. The calculations yield activation energy of 25.1meV under dark, and 17.8meV under illumination.

![Figure 2. Drain current transients of 30nm- and 100nm-thick TFTs, under dark and illumination conditions.](image)

As for the case of 30nm-thick TFTs, the respective calculation yields barrier heights of one order of magnitude less, since the reduction of the channel dimension, enables drain current flow of smaller current density.

4. Conclusions
We have investigated the drain current transient behaviour of ELA SLS TFTs with long grains. The results are extracted by DLTS technique, under dark and illumination conditions. The experimental data indicated that carrier capture/emission processes within the Si-body, are responsible for the transient amplitude decay. In particular, hole emission process is more dominant than electron trapping. Holes generated from deep states are captured during off-state and emitted during on-state. Illumination mainly affects drain transient behavior at lower temperatures, compensating though carrier freeze-out phenomena, through electron-hole pair generation.

5. References
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