Single Switch Module Type DC-DC Converter With Reduction in Voltage Stress

DHAFER ALMAKHLES1, (Senior Member, IEEE),
JAGABAR SATHIK MOHAMED ALI1,2, (Senior Member, IEEE),
J. DIVYA NAVAMANI2, (Senior Member, IEEE), A. LAVANYA2, (Senior Member, IEEE),
AND M. S. BHASKAR1, (Senior Member, IEEE)

1Renewable Energy Laboratory, College of Engineering, Prince Sultan University, Riyadh 11586, Saudi Arabia
2Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology, Kattankulathur, Tamil Nadu 603203, India

Corresponding authors: J. Divya Navamani (divyateddy1@gmail.com) and Jagabar Sathik Mohamed Ali (jsali@psu.edu.sa)

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ABSTRACT This paper proposes a new generalized switched-inductor-capacitor module for a non-isolated dc-dc converter with low voltage dc source applications. Further, the proposed module can be extended to an n number of modules to achieve high voltage gain. The derived structure has low voltage stress on power components. This structure benefits the designer by allowing him/her to choose a low $r_{DS(ON)}$ switch due to the low voltage stress across the semiconductor devices, resulting in high efficiency and low cost. In most dc/dc converters, the voltage stress on the output diode will equal the output (high) voltage ($V_o$). But in the case of the proposed topology, the diode voltage will be the difference between $V_o$ and the input voltage ($V_i$), which eases the reverse recovery problem. The key metrics of the derived topology, such as component count, voltage stresses, and gain factor, are analyzed to compare with similar existing topologies. The scaled down prototype setup is developed for 200 W with an efficiency of 93%. Finally, various experimental results are discussed for the different duty cycles.

INDEX TERMS DC-DC converter, modular structure, reactive elements, step-up converter, voltage stress.

I. INTRODUCTION

Recently, solar photovoltaic (PV) sources have been predominantly used in low and medium power applications due to the availability of solar radiation in good potential areas. There is a slow switch from fossil-fuel-based power generation to renewable-based generation systems in developing countries due to the depletion of fossil fuels in the world. PV energy generation is used in many places, and it is connected to both stand-alone and grid-connected PV applications. The converter plays a vital role in these applications for boosting the DC-Link voltage. In the design of a grid-connected PV system, cost and energy demand are the major factors to be considered. Even for residences, the grid-connected PV system is mostly preferred because it avoids the battery cost and the benefits earned by the customer from the green tariff.

The major demerits of the usage of PV systems for any application are power quality issues due to the power converters, intermittent solar irradiance; and the maximum power point tracking [1]. In addition to these issues, the usage of traditional boost converters also creates certain drawbacks such as high-power loss, switch stress, inrush input current, and low efficiency [2], [3]. These problems can be overcome by developing various high gain converters with features like high voltage gain, reduced stress on semiconductor devices, and an extension of topology. In a grid-connected PV system, the bulky three-phase transformer can be neglected by replacing a conventional boost converter with a high gain dc-dc converter. In the modern grid-connected PV system, the transformerless inverter is connected to the PV source through the high gain dc-dc converter [4]. In the last decade, several techniques such as cascading [5], voltage-lift, coupled-inductor [6], [7], voltage multiplier [8], and so on have been used to develop high gain DC-DC converter topologies.
The majority of high gain dc-dc topologies are derived from switched-inductor/switched-capacitor (SI/SC) cells [9], [10], [11], [12]. This switched-capacitor-based high gain DC-DC converter is used as a medium power application to reduce the issues related to the current ripple [13]. A Switched-Inductor (SI) cell is used in the novel topology derivation, which is made up of inductors and diodes [14]. In this SI cell, the inductors are connected in parallel to charge to the input voltage, and they are connected serially in the next mode to discharge into the load. Furthermore, these SI cells combine with other high gain techniques to enhance the gain of the converter [15]. However, the component count is increased with this type of integration. Further, there are several DC-DC converter topologies that are presented in [16], [17], [18], and [19]. In [16], a symmetric and asymmetrical type-high boost converter is proposed. In the symmetric configuration, the maximum output voltage gain is five times higher than the input voltage. Furthermore, this topology uses two switches that are operated in complementary mode, and the efficiency is high at a high input voltage. Another new topology with a voltage gain of five is introduced in [17], and in this topology a new active switched-inductor cell is presented. The presented topology is similar to that [16], but the number of active devices (diodes) is reduced. Most of the power losses occurred on the switches due to their high switching frequency. The topology is verified experimentally, and results are concluded with a maximum efficiency of 94.27%. The triple voltage gain converter is proposed with a reduction of switch voltage stress in [18]. The switch stress is reduced by adding an additional switch series to a conventional SI boost converter. The total number of magnetic components is two, but the gain is less than [16], [17]. However, the voltage stress across the power components is high. To provide a highly efficient grid-connected PV system, the reduction of voltage stress on power components and power loss minimization are necessary. This paper presents a new extended generalized high gain DC-DC converter topology with a reduction of voltage stress on power components.

The advantages of the proposed DC-DC converter are:

- Low voltage stress on semiconductor devices and capacitors.
- Voltage stress on the capacitor is less than output voltage.
- Single Switch DC-DC Converter and easy to achieve MPPT method due to the presence of a single switch.
- Modular structure - the proposed topology can be extended to n modules for high voltage gain.
- Less number of components and compact size.

The paper is organized as follows: The power circuit of the proposed single switch module type DC-DC converter is discussed in section II. The detailed switching state for both discontinue and continuous conduction modes (DCM and CCM) is presented with mathematical expressions in section III and IV. The efficiency calculation and comparisons of the proposed converter with recent converter are shown in sections V and VI, respectively. The experimental work and observed results are discussed in section VII. Finally, the paper is concluded in section VIII.

II. SINGLE SWITCH MODULE TYPE DC-DC CONVERTER

Fig. 1 shows the generalized structure of the proposed Single Switch Module Type DC-DC Converter with the n module, and each module is connected in parallel to the single DC source (V_g) through switch S. Each module consists of one inductor, one capacitor, and one diode. Furthermore, the diodes (D_{L1}, \ldots, D_{Ln-1}) are used on the lower side to interconnect each module. Each module component is named as a diode (D_{UL1}, \ldots, D_{Ul}), inductor (L_1, \ldots, L_n) and a capacitor (C_1, \ldots, C_n). The output side diode D_o is connected in parallel to the DC source and in series to the n^{th} capacitor. The output capacitor (C_o) is connected between positive terminals of source and load. The advantage is stress across the C_o will be lower than the output voltage. The switch is connected at the end of the n^{th} module to provide the high voltage gain.
The number of capacitors \(N_{\text{Cap}}\), inductors \(N_{\text{Ind}}\) diodes \(N_{\text{Dio}}\) and MOSFETs \(N_{\text{MOS}}\) is obtained from,

\[
\begin{aligned}
N_{\text{Cap}} &= n + 1 \\
N_{\text{Ind}} &= n \\
N_{\text{Dio}} &= 2n \\
N_{\text{MOS}} &= 1
\end{aligned}
\]  

III. OPERATING PRINCIPLE

The proposed converter operation is explained in different conduction modes as follows,

A. CONTINUOUS CONDUCTION MODE

The proposed converter operates in two states as follows,

State-I: In this state, switch \(S\) is conducting and diodes \(D_{U1}, D_{L1}, D_{U2}, D_{L2}, \ldots, D_{Un}, \) and \(D_{Ln-1}\) are forward biased. The active and passive components in the circuit are considered as ideal and therefore the voltage drop and the resistance across semiconductor devices during ON-state are neglected, and the capacitor is considered as ripple-free. The input source magnetizes both the inductors \(L_1, L_2, \ldots, L_n\) along with capacitors \(C_1, C_2, \ldots, C_n\) through switch \(S\). The capacitor \(C_o\) is discharged through the load \(R_o\). During this mode, \(D_o\) is reversed biased. The equivalent circuit of the converter for this state is shown in Fig. 2(a). Significantly, all the inductors are magnetized by the input voltage, which is connected in parallel with capacitors \(C_1, C_2, \ldots, C_n\). The same current flows through both \(L - C\) combinations as shown in the equivalent circuit. The voltages across each
inductor and capacitor are given by,

\[ V_{L1} = V_{L2} = \cdots = V_{Ln} = V_g \]
\[ V_{C1} = V_{C2} = \cdots = V_{Cn} = V_g \]  \hspace{1cm} (2)

The summation of inductors currents is given by,

\[ \sum_{j=1}^{n} i_{Lj} = i_g - i_{Co} - \sum_{k=1}^{n} i_{Ck} \]  \hspace{1cm} (3)

From (3), the current through inductor can be calculated as,

\[ i_{Lj} = \frac{i_g - i_{Co} - \sum_{k=1}^{n} i_{Ck}}{n} \quad \text{where} \quad j = 1, 2, \cdots, n \]  \hspace{1cm} (4)

**State-II:** In this state, inductors \( L_1, L_2, \ldots \) and \( L_n \) and capacitors \( C_1, C_2, \ldots \) and \( C_n \) are demagnetized in series to provide energy to the load \( R_o \) through the diode \( D_o \). During this state, power switch \( S \) is not conducting, diodes \( D_{U1}, D_{L1}, D_{U2}, D_{L2}, \ldots, D_{Un}, \) and \( D_{Ln-1} \) are reversed biased, and diode \( D_o \) is forward biased. The equivalent circuit for this state is shown in Fig. 2(b). The summation of inductors voltages is given by,

\[ \sum_{j=1}^{n} V_{Lj} = V_g + \sum_{k=1}^{n} V_{Ck} - V_o \]  \hspace{1cm} (5)

where \( V_o \) is the output voltage. From (5), the voltage across inductor can be calculated as,

\[ V_{Lj} = \frac{V_g + \sum_{k=1}^{n} V_{Ck} - V_o}{n} \quad \text{where} \quad j = 1, 2, \cdots, n \]  \hspace{1cm} (6)

The voltage across each capacitor is obtained by

\[ V_{C1} = V_{C2} = \cdots = V_{Cn} = V_g \]  \hspace{1cm} (7)

By substituting (7) in (6), the voltage across inductor is obtained as,

\[ V_{Lj} = \frac{(n+1)V_g - V_o}{n} \quad \text{where} \quad j = 1, 2, \cdots, n \]  \hspace{1cm} (8)
According to inductor volt-second balance principle, the average voltage across inductor is zero. Therefore,
\[
\sum_{\text{State - I}} \frac{V_{L_j}}{DT} + \sum_{\text{State - II}} \frac{V_{L_j}}{(1 - D)T} = 0 \tag{9}
\]
where, \(D\) is the duty cycle. By substituting the values of state I and II voltage across inductor from (2) and (8) in (9),
\[
V_gD + \frac{(n + 1)V_g - V_o}{n} (1 - D) = 0 \tag{10}
\]
From (10), the voltage gain of converter is obtained by,
\[
M_{ccm} = \frac{V_o}{V_g} = \frac{(n + 1) - D}{1 - D} \tag{11}
\]
where, \(M_{ccm}\) is the voltage gain of the converter. The current and voltage waveforms for active and passive components are shown in Fig. 3(a).

It is noteworthy to mention that the current through inductors will be different if unequal inductances are used. However, finally, the voltage gain will be the same. The detailed derivation of unequal inductances for switched networks is given in [16] and [18].

B. DISCONTINUOUS CONDUCTION MODE

The transition of the converter operation from CCM to DCM occurs, when the load resistance value is increased, the inductance value is less or at a low switching frequency. In this case, the converter is operate in three different states as follows:

State-I: In this state, initially, inductors \(L_1, L_2, \ldots \) and \(L_n\) currents are at zero and then reach the maximum magnitude at the end. The equivalent circuit is the same as one in state-I of CCM. The ripple in inductors \(L_1, L_2, \ldots \) and \(L_n\) currents are calculated as follows,
\[
\Delta i_{L_j} = \frac{V_gD_1T_s}{L_j} \quad \text{and} \quad j = 1, 2, \ldots, n \tag{12}
\]
where \(D_1\) is the duty cycle for state I, \(T_s\) is total switching time period.

State-II: In this state, initially, inductors \(L_1, L_2, \ldots \) and \(L_n\) currents are at maximum magnitude and then reach zero at the end. The equivalent circuit is the same as one in state-II of CCM. The ripple in inductors \(L_1, L_2, \ldots \) and \(L_n\) currents are calculated as follows,
\[
\Delta i_{L_j} = \frac{(n + 1)V_g - V_o}{nL_j}D_2T_s \quad \text{and} \quad j = 1, 2, \ldots, n \tag{13}
\]
where \(D_2\) is the duty cycle for state II.

State-III: In this state, initially, the currents through inductors \(L_1, L_2, \ldots \) and \(L_n\) are zero. The switch S is in OFF condition and all the diodes are reverse-biased. The output capacitor \(C_o\) provides the necessary current to the load. The equivalent circuit is the same as one in state-II of CCM. The voltage and current waveforms in DCM operation are shown in Fig. 3(b). Fig. 4 shows the diode current \(i_{D0}\) waveform of the converter functioning in DCM mode.

By comparing the inductor current ripple of state I and II, the voltage gain in terms of duty cycle \(D_1\) and \(D_2\) is obtained by,
\[
\frac{V_o}{V_g} = \frac{(n + 1)}{n}D_1 \tag{14}
\]
The expression for duty cycle \(D_2\) can be written as,
\[
D_2 = \frac{2D_1V_g}{V_o - 3V_g} \tag{15}
\]
From Fig.4, the average current through diode \(D_0\) i.e is obtained by,
\[
I_{D0} = \frac{i_{Lj}^\text{peak}}{2} D_2T_s = \frac{V_gD_1D_2T_s}{2L_j} \quad \text{and} \quad j = 1, 2, \ldots, n
\]
where \(i_{Lj}^\text{peak}\) is the peak current through inductors. By applying capacitor charge balanced principle,
\[
I_{D0} = \frac{V_gD_1D_2T_s}{2L_j} = \frac{V_o}{R_o} \quad \text{and} \quad j = 1, 2, \ldots, n \tag{17}
\]
Eliminate the \(D_2\) by substituting (15) in (17). As a results, the quadratic equation is obtained as follows,
\[
V_o^2 - (n + 1)V_oV_g - \frac{n^2V_g^2}{K_j} = 0 \tag{18}
\]
where \(K_j\) is normalised time constant of inductor \(L_j\), and \(K_j = \frac{2L_j}{RT_s}\). By solving (18), the voltage gain of the converter in DCM is obtained by,
\[
M_{dcn} = \frac{(n + 1) + \sqrt{(n + 1)^2 + 4nD_1^2}}{2K_j} \tag{19}
\]

IV. BOUNDARY CONDUCTION MODE

The converter works in boundary conduction mode when the magnitude of the voltage gain of converter in CCM and DCM is same. By equating (19) and (11), the critical value of normalised time constant of inductor \(L_j\) i.e. \(K_j^\text{crit}\) is obtained by,
\[
K_j^\text{crit} = \frac{D(1 - D)^2}{(n + 1) - D} = \frac{D(1 - D)}{M_{ccm}} \tag{20}
\]
Fig. 5 shows the condition to operate converter in CCM and DCM mode. When \(K_j = \frac{2L_j}{RT_s} < K_j^\text{crit}\), the converter operates in DCM mode.
V. EFFICIENCY ANALYSIS

The power loss distribution is calculated for every component in the circuit for the purpose of determining the converter efficiency. The parasitic resistance of reactive components and the ON state resistance of the semiconductor devices influence the converter’s efficiency. The proposed converter \((n = 2)\) is considered where the ideal components are replaced by realistic components, as shown in Fig 6, to determine the efficiency. Based on the circuit, the power loss in each component is calculated. The total switching loss in switch \(S\), diode loss, inductor loss, and capacitor loss are calculated as follows:

The switch losses are bifurcated into switching and conduction losses. The conduction power loss across switch \((P^c_{\text{con}})\) can be calculated by

\[
P^c_{\text{con}} = \frac{2n_i^2D}{(1-D)^2}R_{dc}
\]  

(21)

The switching power loss across switch \((P^s_{\text{swi}})\) can be calculated by

\[
P^s_{\text{swi}} = i_{\text{on}} + i_{\text{off}}(V_o - V_g)\frac{i_oD}{(1-D)}
\]  

(22)

The power loss across diode \((P_d)\) is calculated by,

\[
P_d = \frac{(n + 1)i_oDV_{fd}}{1-D} + i_oV_{fd} + \frac{n_i^2D}{(1-D)^2} + \frac{n_i^2R_{fd}}{1-D}
\]  

(23)

The power flow in the converter components is shown in Fig 7. The switching and conduction loss in switch \(S\) are calculated as 1.56 W and 1.53 W, respectively. Based on the considered cut-in voltage for all diodes is 0.95 V the forward resistance as 0.0475 Ω, the total diode losses of all the three diodes are calculated as 6.26 W. The total capacitor conduction losses are calculated as 4.97 W. Based on the parasitic resistance of the inductor, the total losses are calculated as 0.936 W. The loss breakdown of the proposed converter is shown in Fig. 8 along with the converter [16].
For an output power of 284.7 W, the efficiency is found to be 94.9%. A converter presented in [16] is considered for efficiency comparison with the same input voltage of 40 V and output voltage of 200 V. The efficiency of converter [16] is calculated as 90% for the given parameters. Therefore, almost 5% increase in efficiency is obtained from the proposed converter compared to converter [16]. Fig. 8(c)-(e) depicts the losses of semiconductor devices with $n$ modules at various power ratings. Since the semiconductor losses are predominant losses compared to passive devices, they are considered for analysis. For 50 W rating, the conduction loss of the switch for a single module ($n = 1$) is 2.8% and when the number of modules is increased to 3, the loss is reduced to 0.2%. For $n = 3$, the 500W rating switch conduction loss is 2.2%. Therefore, the proposed work is suitable for higher power ratings with increased module numbers.

**VI. COMPARISON OF THE CONVERTERS**

In order to authenticate the performance and the attributes of the proposed converter, a comparison between the proposed converter and existing topologies in terms of voltage gain and voltage stress of semiconductor devices is presented. The key parameters like voltage and current stress for various components of the proposed converter are listed in Table 1. From Table 2, it is evident that the proposed converter is superior in terms of total component count, the number of inductors, semiconductor voltage stress, and voltage gain compared to existing topologies. Moreover, the voltage gain is five times the duty ratio of 0.5, which is better than the converters listed in Table 2.

Fig. 9 illustrates the stress across the components in terms of input voltage, and it gives an easy view of the maximum voltage across the power components. Figs. 10(a) and 10(b) shows the comparison of the voltage gain and total voltage stress for the various duty cycles, respectively. This shows that the proposed converter’s total semiconductor voltage stress is lower than the available structures in the literature. This can be made even lower by choosing a power switch with a lower on-state resistance. The current stress of the switch is analysed and compared with the quadratic boost converter topology to show its superiority. The current stress of a single switch in the proposed topology is $\frac{2IVO}{1-D}$, whereas for a quadratic boost converter, the current stress is $\frac{IVO}{(1-D)^2}$. A comparative study is performed for the gains 4 to 6 and presented in Fig. 10(c). From this comparative analysis, it is observed that the switch current stress is low for the proposed topology when compared with the QBC.

**VII. RESULTS AND DISCUSSION**

A prototype of a 300 W proposed converter was implemented and tested in the laboratory to validate the performance and functionality. The inductor and capacitor values are chosen the same as used in the simulation. The converter has been fabricated as per the design given in Table 3 and experimental setup with converter prototype is shown in Fig. 11.
All the results obtained from the converter are measured by using a digital storage oscilloscope, DSO-X3034T. The gain value of each module and corresponding voltages is shown in Fig. 12. The experimental results are shown in Fig. 13(a)-(i) and confirm the proposed converter’s operating principle and analytical derivations. The steady-state waveforms are captured for an input voltage of 40 V and a duty cycle of 0.5 to produce an output voltage of 200 V. Fig. 13(a) shows the gating pulse with a duty cycle of 0.5, the input voltage of 40 V, and the output voltage of 200 V. To prove the steady-state analysis, inductor voltage and currents are illustrated in Figs. 13(b) and (c). Moreover, the voltage gain of the converter with two cells is validated for the duty cycles of 0.8 and 0.4. The corresponding gate pulse with input and output voltage is presented in Fig. 13(d)-(e). The observed

![Image of experimental setup and prototype of proposed converter](image)

**FIGURE 11.** Experimental setup and prototype of proposed converter.

**TABLE 1.** Voltage and current stress.

| Parameter | Maximum Voltage Stress | Maximum Current Stress |
|-----------|------------------------|-----------------------|
| $C_1 \rightarrow V_{C1} = V_o$ | $L_1 \rightarrow i_{L1} = \frac{V_o}{R}$ |
| $C_2 \rightarrow V_{C2} = V_o$ | $L_2 \rightarrow i_{L2} = \frac{V_o}{R}$ |
| $C_o \rightarrow V_{C0} = \frac{2V_o}{1-D}$ | $D_o \rightarrow i_{D0} = i_o$ |
| $S \rightarrow V_S = V_o - V_o$ | $D_{U1} \rightarrow i_{DU1} = \frac{V_o}{R}$ |
| $D_{U1}, D_{U2}, D_{L1} \rightarrow V_{DU1} = V_{DU2} = V_{DL1} = 2V_o$ | $D_{U2} \rightarrow i_{DU2} = \frac{V_o}{R}$ |
| $D_o \rightarrow V_o = \frac{2V_o}{1-D}$ | $S \rightarrow i_s = \frac{2V_o}{(1-D)}$ |

**TABLE 2.** Performance comparison of the converters.

| Parameters | QBC | A-SI [16] | A-SI/P-SC [17] | mSIBC [18] | [19] | Proposed (n = 2) |
|-----------|-----|-----------|----------------|-------------|-----|-----------------|
| CH/DuST | 2/2/3/1/8 | 1/3/4/2/10 | 3/3/2/2/10 | 1/2/3/2/10 | 5/3/24/1/10 |
| Voltage Gain ($G_o$) | $\frac{1}{(1-D)\cdot \sqrt{2}}$ | $\frac{1+2D}{(1-D)}$ | $\frac{1+D}{(1-D)}$ | $\frac{1+D}{(1-D)}$ | $\frac{1+D}{(1-D)}$ |
| $V_{peak}$ | $V_o$ | $S_1 : \frac{1+2V_o}{3}$ | $S_1 : \frac{V_o}{1-D}$ | $S_1 : \frac{V_o}{1-D}$ | $S_1 : \frac{V_o}{1-D}$ |
| | $S_2 : \frac{2+V_o}{3}$ | $S_2 : \frac{V_o}{1-D}$ | $S_2 : \frac{V_o}{1-D}$ | $S_2 : \frac{V_o}{1-D}$ | $V_o - V_o$ |
| $V_{diode}^{pk}$ | $D_{1a}, D_{1b} : \frac{V_o - V_o}{3}$ | $D_{1a} : \frac{V_o - V_o}{2}$ | $D_{1b} : \frac{V_o - V_o}{2}$ | $D_{1a} : \frac{V_o - V_o}{2}$ | $D_{1b} : \frac{V_o - V_o}{2}$ |
| | $D_{1c} : \frac{2V_o}{1-D}$ | $D_{2a} : \frac{2V_o}{1-D}$ | $D_{2b} : \frac{2V_o}{1-D}$ | $D_{2a} : \frac{2V_o}{1-D}$ | $D_{2b} : \frac{2V_o}{1-D}$ |
| $I_{rms}$ | $\frac{I_o \cdot \sqrt{2}}{1-D}$ | $\frac{I_o \cdot \sqrt{2}}{1-D}$ | $\frac{I_o \cdot \sqrt{2}}{1-D}$ | $\frac{I_o \cdot \sqrt{2}}{1-D}$ | $\frac{I_o \cdot \sqrt{2}}{1-D}$ |
| Transformer | $\frac{P_{o} \cdot \sqrt{2}}{1-D}$ | $\frac{P_{o} \cdot \sqrt{2}}{1-D}$ | $\frac{P_{o} \cdot \sqrt{2}}{1-D}$ | $\frac{P_{o} \cdot \sqrt{2}}{1-D}$ | $\frac{P_{o} \cdot \sqrt{2}}{1-D}$ |
| Output Voltage | $\frac{3V_o}{1-D}$ | $\frac{3V_o}{1-D}$ | $\frac{3V_o}{1-D}$ | $\frac{3V_o}{1-D}$ | $\frac{3V_o}{1-D}$ |

$C/duST$: Capacitor/duST: Switch Total Components, $V_{peak}$: peak switch voltage, $V_{diode}^{pk}$: peak diode voltage, $I_{rms}$: Switch RMS Current, $P_{o}$: Switch Utilization Factor, $V_{peak}$: Total semiconductor voltage stress.

**FIGURE 12.** Voltage stress across each power components.
average current through the inductors $L_1$ and $L_2$ for a 40 V input voltage with a duty cycle of 0.5 is 1.5 A. The currents of the inductors $L_1$ and $L_2$ shown in Fig 13(b) confirm the average inductor current expression $i_0/(1 - D)$. It is also observed that the converter operates in continuous conduction mode, and inductors $L_1$ and $L_2$ current have an increasing and decreasing slope in the ON and OFF state due to charging and discharging, respectively. The capacitor and diode currents are shown in Figs. 13(f)-(g), respectively. The experimental inductors’ currents $i_{L1}$ and $i_{L2}$ are shown with their corresponding voltages $V_{L1}$ and $V_{L2}$ in Fig 13(h), confirming the charging and discharging operation of inductors. It is observed that both the inductors are charged by the input voltage of 40 V. Fig. 13(i) shows evidence for the derivation of switch voltage and capacitor voltage waveforms $C_1$ and $C_o$. The reduced voltage stress across the various components in the derived topology is validated by the experimental results. The voltage across the switch is $V_o - V_g = 200 - 40 = 160 V$, which is confirmed in Fig. 13(i). The plot of efficiency

### TABLE 3. Experimental parameters.

| Parameters       | Values          |
|------------------|-----------------|
| Power            | 300 W           |
| Input voltage    | 40 V            |
| Output voltage   | 120 V-240 V     |
| Duty cycle       | 0.5-0.8         |
| Switching frequency | 50 kHz        |
| MOSFET           | 600V/50A        |
| Diode            | 300 V, 10 A     |
| Inductors        | $100 \mu F, 10 A, 0.15$ |
| Capacitors       | $100 \mu F$     |
for the various input power levels is shown in Fig. 14. It is observed that the proposed have 95% efficiency when input power 300W.

VIII. CONCLUSION
This paper analyzed the novel high voltage gain dc–dc converter extendable cell structure with improved gain. The proposed converter is modular with a single switch and intended to be built to achieve high voltage gain with a reduced number of active and passive components. The converter has a lower voltage stress across the capacitor and the switch, which reduces the rating of the components. Therefore, the switch losses are lower compared to similar structured existing converters, and the cost and size of the converter are low. A comprehensive investigation is presented based on operational modes analysis, steady-state analysis in DCM and CCM modes, and efficiency analysis. It is observed that the proposed converter operates with a high efficiency of 95% at 285 W. The experimental results of the prototype validate the potential capability of the proposed converter. The presented results prove that the voltage gain of the converter is high, and it progressively increases with the number of cells while the voltage stress across the active and passive components is reduced. The theoretical analysis is validated and its feasibility is tested by the experimental results. The proposed topology is suitable for medium output power standalone rooftop PV application.

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DHAFER ALMAKHLES (Senior Member, IEEE) received the B.E. degree in electrical engineering from the King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia, in 2006, and the master’s (Hons.) and Ph.D. degrees from The University of Auckland, New Zealand, in 2011 and 2016, respectively. Since 2016, he has been with Prince Sultan University, Saudi Arabia, where he is currently the Chairperson of the Communications and Networks Engineering Department and the Director of the Science and Technology Unit. He is also the Leader of the Renewable Energy Research Team and the Laboratory with Prince Sultan University. His research interests include the hardware implementation of control theory, signal processing, networked control systems, and sliding mode.
JAGABAR SATHIK MOHAMED ALI (Senior Member, IEEE) received the B.Eng. degree in electronics and communication engineering from Madurai Kamaraj University, Madurai, India, in 2002, and the M.Eng. and Ph.D. degrees from the Faculty of Electrical Engineering, Anna University, Chennai, India, in 2004 and 2016, respectively. He is currently an Associate Professor with the Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology, Chennai. He is also a Postdoctoral Fellow with the Renewable Energy Laboratory, College of Engineering, Prince Sultan University, Riyadh, Saudi Arabia. He was a consultant of various power electronics companies for the design of power electronics converters. He has authored more than 60 articles publications in international refereed journals and conference proceedings. His current research interests include multilevel inverters, grid-connected inverters, and power electronics converters and its applications to renewable energy systems. He received the certificate of recognition from the IEEE Madras Section for paper published in the year 2019–2021. He is serving as a Regular Reviewer for several journals, including the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS, and the IET Power Electronics.

A. LAVANYA (Senior Member, IEEE) received the B.E. degree in electrical and electronics engineering from Madras University, India, in 2001, the M.E. degree in power electronics and industrial drives from Satyabhama University, in 2005, and the Ph.D. degree in topological derivation of dual input DC-DC converter topologies for hybrid energy system application from the SRM Institute of Science and Technology, Chennai, India, in 2021. She is currently working as an Assistant Professor with the Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology. She has authored more than 30 articles publications in international journals and conference proceedings. Her current research interests include multiport DC-DC converters, solar PV systems, and DC-DC converters in electric and hybrid electric vehicle. She is the Life Member of IEI and ISTE.

J. DIVYA NAVAMANI (Senior Member, IEEE) received the B.E. degree in electrical and electronics engineering from Madras University, India, in 2001, the M.E. degree in power electronics and industrial drives from Sathyabama University, in 2005, and the Ph.D. degree in design of non-isolated high gain DC-DC converter topologies for automotive lighting application from the SRM Institute of Science and Technology, Chennai, in 2019. She is currently working as an Associate Professor with the Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology. She has authored more than 40 articles publications in international journals and conference proceedings. Her current research interests include high gain dc-dc converters, solar PV systems, microbial fuel cell, renewable energy systems, and DC-DC converters in electric and hybrid electric vehicle. Design of Non-Isolated High Gain DC-DC Converter Topologies for Automotive Lighting Application with the SRM Institute of Science and Technology, in 2019. She is the Life Member of IEI and ISTE. She is serving as a Regular Reviewer for several journals, including IEEE Access, the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS, and the IET Power Electronics.

M. S. BHASKAR (Senior Member, IEEE) received the bachelor’s degree in electronics and telecommunication engineering from the University of Mumbai, Mumbai, India, in 2011, the master’s degree in power electronics and drives from the Vellore Institute of Technology, VIT University, India, in 2014, and the Ph.D. degree in electrical and electronic engineering from the University of Johannesburg, South Africa, in 2019. He was a Postdoctoral Researcher with his Ph.D. tutor at the Department of Energy Technology, Aalborg University, Esbjerg, Denmark, in 2019. He worked as a Researcher Assistant at the Department of Electrical Engineering, Qatar University, Doha, Qatar, from 2018 to 2019. He worked as a Research Student at the Power Quality Research Group, Department of Electrical Power Engineering, Universiti Tenaga Nasional (UNITEN), Kuala Lumpur, Malaysia, from August 2017 to September 2017. He is currently with the Renewable Energy Laboratory, Department of Communications and Networks Engineering, College of Engineering, Prince Sultan University, Riyadh, Saudi Arabia. He has authored 150 plus scientific papers with particular reference to DC/DC and DC/AC converter, and high gain converter. He received the Best Paper Research Paper Awards from IEEE-GPECOM’20, IEEE-CENCON’19, IEEE-ICCPCT’14, IET-CEAT’16. He is a IEEE Industrial Electronics Society, IEEE Power Electronics Society, IEEE Industry Applications Society, IEEE Power and Energy Society, IEEE Robotics and Automation Society, IEEE Vehicular Technology Society, Young Professionals, various IEEE councils, and Technical Communities. He is a reviewer member of various international journals and conferences, including IEEE and IET. He received IEEE Access Award “Reviewer of Month,” in January 2019, for his valuable and thorough feedback on manuscripts, and for his quick turnaround on reviews. He is an Associate Editor of IET Power Electronics and a Topic Editor of MDPI Electronics, Switzerland.

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