Strategies for Electronics Test
Craig Pynn (McGraw-Hill Book Co., New York, 1986, 174 pp., $19.95)

Reviewed by Kemon Taschiglou

Surprisingly, few comprehensive books have been written on automatic testing of electronic assemblies. This text, although valuable, is not one of them, serving only as an introductory primer and tutorial. The author does a good job within this context, however, covering basic testing issues well. He suggests that it is possible to classify faults and the test coverage of testers, and then to match the classifications selectively to achieve the optimum test strategy.

In developing his theme, Pynn provides useful definitions of tester types and their interrelationships, environmental screens, simulators and emulators, fixtures, and beds of nails. He supplies these definitions in a logical historical perspective, matching the technological evolution of semiconductor devices and circuits, and he backs them up with an extensive 90-word glossary.

He succinctly summarizes the conflicting considerations and the complexity of decision-making for devising test strategies in the typical context of broad product mix, shortening life cycles and learning curves, and varying yields. Also useful are his delineation of “current” and “latent” faults and his cost-efficiency curve in Chapter 6. His separation of cost categories into “acquisition→adaption→operational” aptly emphasizes the evolutionary aspect of testing costs.

Pynn develops an original diagrammatic model for classifying at several levels the wide variety of types of faults encountered. Different processes and circuit boards show differing profiles of fault distribution on this model. These profiles serve as the foundation for determining test strategy.

He then classifies tester types by function and by their ability to detect these classes of faults. This information is applied in a second diagrammatic model—of test efficiency by tester type—which overlays on the fault profile. In this way, he deduces a number of useful generalizations about test strategy, which are described in Chapter 5.

The book falls short, however, of actually applying the models, tracking any decision-making examples in real-life situations. More important, Pynn merely alludes to the problem of overlapping test coverage for various tester types. He acknowledges that it complicates the selection of test strategies, but his warning is not strong enough. This overlap is one of the issues that make finding the optimum strategy so difficult; to overlook it can lead to erroneous conclusions.

He also neglects to mention the condition associated with his conventional definition of test coverage: namely, the value of any test operation for any fault category depends on whether there are preceding test operations. For example, a functional test following an in-circuit test may have a test coverage for shorts of 85%, but that figure is 85% of the faults left over after in-circuit test. Without the in-circuit test, the functional test’s coverage for shorts would increase significantly.

Pynn tells us more than once that he will discuss the economic considerations in devising test strategies. When the explanation finally does come, however, it offers only generalizations—albeit useful ones—but without quantities attached. He hardly deals with the economics of test strategy. He would have helped us by at least, referring to the seminal work published on the subject by Brendan Davis (The Economics of Automatic Testing, McGraw-Hill, 1982).

These shortcomings suggest that the very title of the book, Strategies for Electronics Test, is somewhat misleading. Similarly, the book’s chapter headings when listed show a coherent overall structure and flow, but their contents do not always fulfill their promise.

Chapter 2, “Achieving Minimum Defects,” introduces the useful concepts just mentioned for classifying defects, but says little of value about how to reduce them. Chapter 9, “Why Process Control Is Vital,” describes well various forms of data collection and several practical arrangements for linking design and test, and gives a neat hierarchical structure for process control; but it does not tell us why process control is vital.

“Misleading” is also an appropriate word for a number of Pynn’s technical statements. For example, he introduces the well-known Poisson distribution as “a way of linking process yield to average faults.” He applies it in developing capacity, but says little else about its application. The implication is that we can expect to see this relationship in test results on the production line. Better to tell us why observed process yields usually exceed those implied by the Poisson from the observed average faults—especially early in process routing—and how the extent of this departure from the Poisson indicates the degree of systematic, as opposed to random, faults.

In Chapter 4, Pynn develops straightforward formulas for determining total time on the tester. With some simplifying assumptions, he gives examples to show how to concentrate on variables that provide the greatest leverage to increase throughput. He appropriately emphasizes that such choices involve considering yield, diagnosis time, and handling time, not merely raw process or test time.

These generalizations are useful. The simplifying assumptions, however, obscure other issues important in determining test strategy. For example, Pynn tells us to use the factor (1−yield) to determine the number of times boards go through the retest loop. He neglects to point out, however, that this factor applies only for inspection testers, which detect all detectable faults in one pass.

Functional testers, on the other hand, detect one fault at a time; the factor is equal to the average number of faults. The values of the two factors will be wider apart as as the yield drops, a difference of 20% at yields of 70%. This gap is significant in determining the optimum arrangement of inspection tester and functional tester, especially when considering the functional tester
where the diagnosis time tends to be much higher than the test and handling time.

I also question Pynn's terminology. In Chapter 4, the term “hurdle rate” is applied as a production-level criterion; I have never seen it so applied. Hurdle rate is commonly applied in financial accounting, referring to the internal rate of return from capital expenditures. Because hurdle rate as a financial accounting term is often considered in the purchase of automatic test equipment, Pynn's usage can be confusing.

Acquisition cost is usually treated as a capital expenditure. To treat it in Chapter 6 in the same context as acquisition cost and operating cost disregards the common accounting practice of amortizing it over many periods. In addition, the term “transfer function,” referring to the truth table of a digital printed circuit board, can be misleading. While this reference is not precisely untrue, transfer function suggests an analytical procedure and a statement that is algebraic in nature.

Particularly notable is the ending of this book, a few paragraphs under the heading “Eliminating Testing.” Pynn suggests that testing could be eliminated by improving manufacturing quality. How much more powerful the book would have been had he introduced this concept at the beginning and repeated with examples throughout the book. It so naturally follows from his inspiring and perceptive introduction, “The Renaissance In Manufacturing.”

The author's orientation toward the role of testing in manufacturing is enshrined, unfortunately, by the conventional wisdom of the ATE industry: The purpose of automatic test equipment is to find faults and permit them to be repaired at the lowest possible cost. Gradually, this philosophy is being replaced by the recognition that testing is the driving engine for identifying faults so that their causes can be successively eliminated—ultimately permitting the successive elimination of testers themselves.

Kemon Tasicoglou founded The Kemon Company three years ago to provide a service called QA (Quality Impact analysis), a procedure to improve quality and to lower test costs in electronics manufacturing. Previously he worked at Teradyne, primarily in marketing, focusing on the economic justification of test equipment. He originated the 10-to-1 rule of increasing cost of faults on the production line. Tasicoglou holds a BSEE from MIT and an MBA from the Harvard Business School.

October 1987

- Int'l Conf. Computer Design, October 5-8, Rye Brook, New York. Contact Prathima Agrawal, AT&T Bell Labs, 600 Mountain Ave., Rm 3D-480, Murray Hill, NJ 07974; (201) 582-6943.

- Compas 87, October 5-9, Tokyo. Contact Kosui Yasui, Business Center for Academic Societies Japan, Yamazaki Bldg., 4F, 2-40-14, Hongo, Bunkyo-Ku, Tokyo 113, Japan; 81 (3) 817-5831 or Stephen S. Yau, Northwestern Univ., Dept. of EEC, Evanston, IL 60201; (312) 491-3641.

- Systems for Manufacturing Excellence Conf. and Expo, October 12-16, Long Beach, California. Contact Gregg Balke, SME Technical Activities Dept., One SME Dr., PO Box 930, Dearborn, Michigan 48121; (313) 271-1500.

November 1987

- Int'l Conf. Computer-Aided Design, November 9-12, Santa Clara, California. Contact ICCAD-87 Secretary, Mentor Graphics, CRC 400 Zanker Rd., San Jose, CA 95112; (408) 436-1500.

- Symp. Int'l Test and Evaluation Assoc., November 10-12, Boston. Contact William M. Stein, Mite Corp., MS G105, Burlington Rd., Bedford, MA 01730; (617) 271-8238.

1987 Distinguished Lecture Tour, Region 9 (Latin America), November 2-15, 1987. IEEE member applicants should send letter indicating interest in tour, resume and one-page summary of proposed technical lecture in power, computer, or communications fields by July 1, 1987 to Arthur P. Stern, Transnational Relations Committee Chairman, c/o Barbara Ettinger, TRC Administrator, IEEE Hqtrs., 345 E. 47th St., New York, NY 10017-2394.

IEEE Conf. Computer Workstations, March 7-10, 1988, Santa Clara, California. Conference theme: advanced computer workstations and their software environments, hardware and software technology, applications and performance evaluation. Submit six copies (5000 words max.) with author's name and address on cover sheet only (to ensure impartial reviewing) by July 29, 1987 to Lawrence Stewart, DEC Systems Research Ctr., 130 Lytton Ave., Palo Alto, CA 94301.

- Int'l Conf. Communications, June 12-15, 1988, Philadelphia. Submit complete manuscript (3000 words max.) with title page containing 100-word abstract, author's name, complete address, topic name and topic number by September 1, 1987. Call John S. Ryan, (201) 949-4632, for further instructions.

- Int'l Symp. Circuits and Systems, June 7-9, 1988, Espoo, Finland. Submit four copies of extended summary (1000 words min.) describing original work with sufficient detail, salient concepts, novel features, category, author's name, affiliation and complete address by October 1, 1987 to Hiro Hartimo, Dept. of Technical Physics, Helsinki Univ. of Technology, SF-02150 Espoo, Finland.