Hybrid Static/Dynamic Schedules for Tiled Polyhedral Programs

Tian Jin
Computer Science Department
Haverford College
tjin@haverford.edu

Nirmal Prajapati, Waruna Ranasinghe, Guillaume Iooss, Yun Zou, Sanjay Rajopadhye
Computer Science Department
Colorado State University
[First.Last]@colostate.edu

David Wonnacott
Computer Science Department
Haverford College
davew@cs.haverford.edu

Abstract

Polyhedral compilers perform optimizations such as tiling and parallelization; when doing both, they usually generate code that executes “barrier-synchronized wavefronts” of tiles. We present a system to express and generate code for hybrid schedules, where some constraints are automatically satisfied through the structure of the code, and the remainder are dynamically enforced at run-time with data flow mechanisms. We prove bounds on the added overheads that are better, by at least one polynomial degree, than those of previous techniques.

We propose a generic mechanism to implement the needed synchronization, and show it can be easily realized for a variety of targets: OpenMP, Pthreads, GPU (CUDA or OpenCL) code, languages like X10, Habanero, Cilk, as well as data flow platforms like DAGuE, and OpenStream and MPI. We also provide a simple concrete implementation that works without the need of any sophisticated run-time mechanism.

Our experiments show our simple implementation to be competitive or better than the wavefront-synchronized code generated by other systems. We also show how the proposed mechanism can achieve 24% to 70% reduction in energy.

1. Introduction

The ongoing evolution and increasing complexity of modern computer architecture creates new challenges to the goal of tuning software for optimal performance. For example, the exact time for any event, across multiple levels of the computer/memory hierarchy, is increasingly unpredictable because of latency and bandwidth differences in accesses to various levels of caches, and instruction pipelining and reordering, performed in the microarchitecture. Indeed, most machines can be abstracted as coupled microarchitectural modules interacting more like “data-flow engines,” rather than simple “data-paths” controlled by finite state machines.

To meet these challenges we must create tools applicable to varied target architectures. The development of the polyhedral model [20, 21, 40, 43, 44] enables analyses like automatic parallelization on a significant class of programs, and transformations like loop tiling [28, 51] to be applied at a scope where it is most valuable [53]. While challenges remain in expanding the domain of the polyhedral model, it is already widely used in research [6, 39, 55] and commercial [36] compilers.

State of the art polyhedral compilers first choose a schedule that identifies the potentially tilable dimensions, and also the inherently sequential dimensions within the iteration spaces of the program. Subsequently they generate code that visits the inherently sequential dimensions in serial order, tiles the tilable dimensions, and executes the tiles in parallel, typically via an outer sequential loop that enumerates “wavefronts” of tiles, such that every tile depends only on tiles from “strictly previous” wavefronts. A sequential for loop around an OpenMP parallel for loop, together with a barrier between consecutive wavefronts, provides a convenient and portable mechanism to express this execution.

As many authors note, such static control structures have a number of drawbacks [3, 7, 8, 16, 30, 57]. First, they induce unnecessary synchronization—any tile of wavefront $w$ must wait for all tiles of wavefront $w - 1$. Second, such over-constrained schedules may prevent other optimizations like loop fusion [30]. Third, it suffers what we call the affinity problem: data needed for a tile may not reside in that (or any) core’s cache at the start of tile execution—other tiles in the previous wavefront may have evicted it. This has a cost on both time and energy, although “multipass wavefront schedules” can reduce it [57].

To address these drawbacks, many authors suggest compiling even “regular” programs such as dense linear alge-
background or polyhedral loops to a data-flow runtime/library on shared memory platforms [3][7][30] or distributed memory machines [8][16][58] or hybrid systems [16]. Similar solutions are also available on accelerators [8][16][45]. Regardless of the specific target language/platform, we call this data-flow runtime synchronization, since many are inspired by earlier work on general purpose data-flow computing systems [47][48].

However, data-flow runtime systems incur overheads in: task synchronization, memory for managing task state, and most importantly, task creation/spawning. All systems synchronize the dependences of each tile, and some have a memory overhead that is directly proportional to the total number of tiles. Some even construct the entire task graph at compile time. Significantly, all existing data-flow systems for polyhedral programs create and launch one task per tile. This not only contributes to inefficiencies in context switching and scheduling overhead, but also suffers from the affinity problem: the time/processor when/where a tile is eventually scheduled is decided by the data-flow run-time.

In this paper, we show that for polyhedral programs, such approaches are overkill, and develop a very simple, domain-specific solution. Our granularity of task creation/spawning is not a tile, but what we call a virtual processor: a sequence or “slice” of tiles. This reduces the number of tasks created by a polynomial degree and the synchronization tests by a constant factor (see the asymptotic complexity analyses in Sec. 6). We use a partial order view of polyhedral time [56] to define hybrid static-dynamic schedules, provide their legality conditions, and show how this leads to an algorithm to separate dependences guaranteed to be statically satisfied from those which must be satisfied via a run-time check (see Sec. 5). We then formalize the precedence obligations of these checks, and develop a self-scheduling run-time mechanism (in Sec. 4) that guarantees these dependences without any of the overheads of a full fledged data-flow run-time system.

Our solution is also generic, and leads to a single code generator framework to produce code with target-agnostic synchronization “stubs,” that can be filled in with primitives for a variety of targets, such as OpenMP, C+Pthreads [26], CUDA [37], X10 [12], Habanero [9], Cilk++ [31], OpenStream [38], and under simple instances, also MPI. Furthermore, it also allows us to cleanly isolate issues like deadlock that often depend on some specific properties of the target.

We provide an implementation of the synchronization stubs for two platforms: OpenMP and C+Pthreads. The lightweight runtime leads to significant performance gains in both time and energy (see Sec. 7).

2. Background

We now describe the background on polyhedral compilation needed to make the paper self contained. Some of our explanations are (deliberately) simplistic in order to convey the main intuitions concisely.

The polyhedral framework lets compilers reason about loop nests in terms of executions or instances of statements rather than statements themselves. Consider the code of Figure 1, which we will use as a simple running example. It implements the following equation ($H[M−1,N−1]$ is the desired output):

\[
H[x,y] = \begin{cases} 
0 & \text{if } x = 0 \lor y = 0 \\
\text{foo}(H[x−1,y],H[x,y−1]) & \text{otherwise}
\end{cases}
\]

(1)

The polyhedral model lets a compiler reason about an $M \times N$ set of executions of that statement (labelled S), which we could express in the notation of isl [49] as

$$[N,M] \rightarrow \{(i,j) | 1 \leq i < M \land 1 \leq j < N\}$$

This representation lets the compiler reason about iteration spaces of unknown size by describing potentially infinite sets of integer points with a finite set of affine equality and inequality constraints on integer variables (i.e., they reason about sets of integer points inside a potentially unbounded polyhedron). While decision algorithms for this domain have high complexity, they typically perform well in this context due to the simplicity of the constraints involved [42].

Array dataflow analysis [20][41] (ADA) lets the compiler extract the flow of information in the code, for example recreating the otherwise clause of the original equations at the top of Figure 1 by identifying the sources of the two values arriving at iteration $(i,j)$ of Statement $S$ from earlier.

Figure 1. REX (Running EXample)

Figure 2. Polyhedral Compilation: the Polyhedral Reduced Dependence (hyper) Graph (PRDG) serves as the intermediate representation, with Piecewise Quasi-Affine Functions (PQAFs) describing transformations of this representation.

The polyhedral model lets a compiler reason about iteration spaces of unknown size by describing potentially infinite sets of integer points with a finite set of affine equality and inequality constraints on integer variables (i.e., they reason about sets of integer points inside a potentially unbounded polyhedron). While decision algorithms for this domain have high complexity, they typically perform well in this context due to the simplicity of the constraints involved [42].

Array dataflow analysis [20][41] (ADA) lets the compiler extract the flow of information in the code, for example recreating the otherwise clause of the original equations at the top of Figure 1 by identifying the sources of the two values arriving at iteration $(i,j)$ of Statement $S$ from earlier.

Figure 2. Polyhedral Compilation: the Polyhedral Reduced Dependence (hyper) Graph (PRDG) serves as the intermediate representation, with Piecewise Quasi-Affine Functions (PQAFs) describing transformations of this representation.

The polyhedral model lets a compiler reason about iteration spaces of unknown size by describing potentially infinite sets of integer points with a finite set of affine equality and inequality constraints on integer variables (i.e., they reason about sets of integer points inside a potentially unbounded polyhedron). While decision algorithms for this domain have high complexity, they typically perform well in this context due to the simplicity of the constraints involved [42].

Array dataflow analysis [20][41] (ADA) lets the compiler extract the flow of information in the code, for example recreating the otherwise clause of the original equations at the top of Figure 1 by identifying the sources of the two values arriving at iteration $(i,j)$ of Statement $S$ from earlier.
executions of $S$:
\[
\{(i, j) \rightarrow (i - 1, j) \mid 2 \leq i \leq M \land 1 \leq j \leq N\}
\cup \{(i, j) \rightarrow (i, j - 1) \mid 1 \leq i \leq M \land 2 \leq j \leq N\}
\]

This representation provides the information needed to test the legality of any reordering of iterations. We can furthermore use the polyhedral framework to find the flow of information among tiles, and use that to determine the possible legal execution orderings of tiles.

Figure 2 illustrates the flow of a typical polyhedral compiler. The input program may be in any standard imperative language, possibly with annotations as to which part of the code is to be analyzed using polyhedral techniques. The front end produces descriptions of the iteration spaces and the inter-iteration dataflow (as discussed above) among all statements; depending on the set of transformations to be applied, it may also record the memory address written by each iteration. These data structures are collectively known as the Polyhedral Reduced Dependence (hyper) Graph (PRDG), and serve as the intermediate representation for a polyhedral compiler. Additional analysis steps (or programmer direction) are used to define program transformations as a set of functions on the iteration space. Like the descriptions of iteration spaces and dataflow, these are represented via affine constraints on integer variables, or the union of several such representations, known as (Piece-wise) Quasi-Affine Functions (PQAF’s). The PQAF’s for the program transformations can be fed (along with the PRDG) into a code generator \[49\] or used iteratively to transform the PRDG itself.

2.1 Polyhedral Reduced Dependence (hyper) Graph

Figure 3 gives the PRDG for REX. Nodes correspond to statements (with corresponding iteration spaces shown to the right). Although the loop contains only one statement ($S$), a pseudo-statement $In$ is automatically generated to define the source of live-in array elements. PRDG hyper-edges are used to describe dependences; there are several variants on this technique. Here, we use one hyper-edge for each region within the iteration space, and our hyper-edges have one source node and possibly multiple destination nodes. For each destination node $Y$ of a hyper-edge we identify an “input-output pair” with the 4-tuple $(X, Y, D, f)$, where $X$ is the source of the hyper-edge, $f$ and $D$ are respectively the value and the constraints of one of the case derived through the ADA.

For example, for REX, the $S$ node depends on the $In$ node for both its inputs in the first iterations of the $i$ and $j$ loops. Similarly there are three other cases:

- for $i = j = 1$ (Edge e3), both references are $\bot$, and
- for $i = 1, j > 1$ (Edge e4), the first reference is $\langle i, j \rangle$ and the second one is $\bot$.

2.2 Tiling and the Tiled PRDG

In polyhedral compilation, tiling is possibly the most critical transformation. It groups computations/iterations into tiles, which are executed atomically. There is a huge amount of literature on the subject of tiling, including the feasible space of “legal” tiling hyperplanes, the choice of “good” tiling hyperplanes and tile sizes that seek to optimize a wide range of cost functions, addressing locality, coarse-grain and/or fine-grain parallelism, etc. This is completely orthogonal to our work. We assume that a tiling has been chosen. We present a simplified description of how tiling affects the program representation.

Tiles can be of various shapes (e.g., parallelogram, hexagon) and sizes important attribute of tiling is the tile size, for which there are two main choices: fixed, or parametric. With fixed-size tiling, the resulting program remains polyhedral and can be further analyzed and transformed using polyhedral techniques. However, it means that when the space of tile sizes is to be explored, say by auto-tuners, the code generation and compilation must be done repeatedly. Moreover, it precludes delayed binding of tile sizes. Parametric tiling, on the other hand allows such delayed binding of tile sizes, but since it is inherently a nonlinear transformation, the program is no longer polyhedral, and cannot be further analyzed, transformed or optimized. Recently, Iooss et al. \[27\] introduced monoparametric tiling that provides a compromise: it remains a polyhedral transformation, but allows only a single tile size parameter. In this paper, our goal is to further analyze and/or transform the program after tiling, so we use fixed-size or monoparametric tiling.

Tiling introduces a new set of indices called tile indices which identifies a tile in the computation. Depending on the number of original dimensions that are tiled, the total number of indices could increase by up to a factor of 2.

In this paper, we are only interested in the inter-tile dependences. By analyzing these dependences (provided the program remains polyhedral, i.e., if we use fixed-size or monoparametric tiling), we can build the tiled PRDG which considers the tiles of a program at points in an iteration space, and the dependences across them. Here, all the domains associated with the nodes and affine functions associated with the hyper-edges are projections on the tile indices of the original domains and dependences. Thus, the tiled PRDG will be very similar to the original PRDG, except that the labels on the hyper-edges now represent inter-tile dependences, and the domains and the functions of this representation. Indeed, for REX, the PRDG is (coincidentally) isomorphic to the original PRDG (see Figure 3).
We achieve “coarse-grain” parallelization using a hybrid maps every point in the domain associated with the node to and Yuki et. al [56] formalizes partial order schedules, and loops in OpenMP). Recent work by Verdoolaege et. al [50] order is actually a partial order dral compilation tools to generate code where the execution important to note that in this early work time is viewed as a other one, \(t_2\) iff \(t_1\) precedes \(t_2\) in the lexicographic order. It is 3. Hybrid Schedules

For the purpose of this paper, we assume that the program has been tiled, and the specific problem we address is its subsequent “coarse-grain” parallelization. We start with the program representation in the form of a Tiled PRDG, where each node represents a “sort” or “signature” of tiles, the domain of the node defines the set of instances of tiles of that particular sort, and hyper-edges define inter-tile dependencies. We achieve “coarse-grain” parallelization using a hybrid schedule that is partially static and partially dynamic.

**Definition 1.** For any node \(X\) in the PRDG, an \(m\)-dimensional schedule \(\theta_X\) is an affine function that maps every point to an integer vector \(\vec{t} \in \mathbb{Z}^m\).

There is a large body of work on how such schedules can be determined, including optimality conditions under a range of cost models [13, 15, 21, 53, 43, 44]. When extended to multi-dimensional time [22], precedence is the lexicographic order; an \(m\)-dimensional time stamp, \(t_1\) happens before another one, \(t_2\) iff \(t_1\) precedes \(t_2\) in the lexicographic order. It is important to note that in this early work time is viewed as a total order: given two distinct time vectors, it is always possible to determine which one occurs before the other. Such schedules are routinely used, albeit in an ad-hoc manner, by polyhedral compilation tools to generate code where the execution order is actually a partial order (e.g., “outer-parallel” for loops in OpenMP). Recent work by Verdoolaege et. al [50] and Yuki et. al [56] formalizes partial order schedules, and we use a similar notion here.

**Definition 2.** For any node \(X\) in the PRDG, a hybrid static-dynamic (HSD) schedule, \(\theta_X\) is an affine function that maps every point in the domain associated with the node to an integer \(n\)-vector \(\vec{t}\), called the space-time, or the processor-time vector. An HSD schedule has the following properties.

- For some integer \(k\), \(0 \leq k \leq n\) the first \(k\) dimensions of \(\vec{t}\) are called the (virtual) processor/space dimensions, and the remaining \(n - k\) dimensions, are called the (local) time dimensions. The corresponding subvectors of \(\vec{t}\) are \(\vec{t}_p\) and \(\vec{t}_t\), and the function \(\theta_X\) has two components: \(\pi_X\) and \(\tau_X\): \(\vec{t}_p = \pi_X(z)\) and \(\vec{t}_t = \tau_X(z)\).

- Space-time vectors form a partial order: \(\vec{t}'\) happens before \(\vec{t}\) iff \(\vec{t}' = \vec{t}_p'\) and \(\vec{t}_t'\) precedes \(\vec{t}_t\) in the lexicographic order; if \(\vec{t}_p' \neq \vec{t}_p\), the two are incomparable.
- \(\theta_X\) is a bijection.

**Definition 3.** An HSD schedule for a program is a set of HSD schedules, one for each node in its PRDG, that maps iteration points to a common space-time, i.e., with the property that \(n\) and \(k\) are identical for all variables.

3.1 Partial Legality

We now describe (some of) the legality conditions that HSD schedules must satisfy. Informally, whenever \(X[z]\) depends on \(Y[f(z)]\), and the two instances are both assigned the same processor, the respective time steps of these two points must satisfy (strict) lexicographic precedence, so as to ensure that the “producer happens before the consumer.”

**Definition 4.** An HSD schedule for a PRDG is said to partially respect an input-output pair \((X, Y, D, f)\), iff

\[
\forall z \in D, \pi_X(z) = \pi_Y(f(z)) \Rightarrow \tau_X(z) > \tau_Y(f(z))
\]

An HSD schedule for a PRDG partially respects a hyperedge of the PRDG iff it partially respects all the input-output pairs of the hyper-edge.

An HSD schedule for a PRDG is partially legal iff it partially respects all the hyper edges of the PRDG.
Note that our definition of legality, and respecting dependences/hyper edges is silent about what happens when the producers and consumers are mapped to distinct (virtual) processors. This is because, time stamps where this does not hold, are not comparable, and require a separate mechanism to enforce the legality of the final program. Regardless of how this mechanism is implemented, it does not need to satisfy all instances of all program all dependences, but rather a subset, that we call the residual dependences.

3.2 Residual PRDG and full Legality

Algorithm 1 describes how to isolate the residual dependences, in the form of a transformed PRDG, called the Residual PRDG (RPRDG).

Algorithm 1: Constructing the Residual PRDG

For the REX in Fig 3 the RPRDG will have same two nodes with two edges from node S to itself. e1 \((i_b > 0 \land j_b > 0)\): \((i_b, j_b) \mapsto S(i_b - 1, j_b)\) and e2 \((i_b > 0 \land j_b = 0)\): \((i_b, j_b) \mapsto S(i_b - 1, j_b)\).

There is a plethora of languages and associated run-time systems [8–12, 19, 25, 26, 31, 46, 58] to ensure dependences are dynamically satisfied. However, because we are dealing with polyhedral programs, a very small number of simple abstractions are sufficient.

Before proceeding further, we perform a simple transformation on the RPRDG (following the dotted lines in Fig. 3). We use our HSD schedule functions \(\theta_X, \theta_Y, \ldots\) (recall that they are all bijections) to "rename/reindex" the program so that all nodes, domains, and dependences are brought into a common set of space-time coordinates, \(z = (\tilde{p}, \tilde{t})\), the for any node, \(X, D_X\) denotes the set of space-time coordinates where tiles with signature \(X\) are to be executed. Consider an input-output pair \((D, X, Y, f)\), and let us separate out the space and time components. Let or \(\tilde{z} = (\tilde{p}, \tilde{t}) \in D\), and let

\[
\begin{align*}
  f(\tilde{z}) &= \left( \begin{array}{c}
  f_p(\tilde{z}) \\
  f_t(\tilde{z})
  \end{array} \right) = \left( \begin{array}{c}
  \pi(\tilde{p}, \tilde{t}) \\
  \tau(\tilde{p}, \tilde{t})
  \end{array} \right).
\end{align*}
\]

The dynamic dependences obligations of each input-output pair in the RPRDG, are as follows.

**Proposition 5.** The tile with signature \(X\) at \(\tilde{z} = (\tilde{p}, \tilde{t})\) cannot be executed until the following constraint holds:

If \(\tilde{z} \in D\) then the tile with signature \(Y\) at space-time coordinates \((\pi(\tilde{p}, \tilde{t}), \tau(\tilde{p}, \tilde{t}))\) must have completed execution.

4. A Self-Scheduling Runtime

Our strategy for dynamically satisfying residual dependences is simple and consists of the following elements. We maintain a global, shared data structure (an array) called \(\text{State}_X\) that stores the status of tiles with signature \(X\) on each (virtual) processor. The \(i_p\)-th entry in this array is an \((n - k)\)-tuple of integers, representing the most recent time-step that processor \(i_p\) has completed.

Each processor executes a sequential program that visits tiles allocated to it in the lexicographic order of its local time stamp. At each iteration, it executes the following steps:

- Call a meta-function acquire\((X, \tilde{p}, \tilde{t})\), to ensure that all its residual dependences have been satisfied (as per Prop. 5).
- Execute TileX\((\tilde{p}, \tilde{t})\)
- Call a meta-function update, to (atomically) store \(\tilde{t}\) in \(\text{State}_X[\tilde{p}]\).

This program maintains, the following invariant

**Proposition 6.** If the value of \(\text{State}_X[\tilde{p}]\) is \(\tilde{t}\), then TileX\((\tilde{p}, \tilde{t})\) has been successfully executed.

Note that our scheme has none of the overheads of a typical run-time system: worker queues, schedulers, shared data structures, cactus stacks, etc. Not even a mutex—all the writes to the \(\text{State}\) arrays are guaranteed to be exclusive write. Key scheduling decisions are made directly in the control structure of the generated code (hence the term "self-scheduling") and this is why we see significant performance gains.

4.1 Implementing the Acquire Function

It follows from Props. 5 and 6 that all that acquire must ensure is that for each input-output pair, \((D, X, Y, f)\) whose source node is \(X\),

- First, test if the current space-time coordinates, \((\pi(\tilde{p}, \tilde{t}), \tau(\tilde{p}, \tilde{t}))\) belong to \(D\)
- If so, ensure that (wait until) the \(\pi(\tilde{p}, \tilde{t})\)-th entry in \(\text{State}_Y[\tilde{p}]\) is lexically greater than or equal to \(\tau(\tilde{p}, \tilde{t})\).

Note how this is completely target agnostic. In fact, our implementation uses a simple busy wait. The cost of the implementation is a finite number (per input-output pair of the RPRDG) of evaluations of simple affine functions of the current space-time coordinates, which are about as complicated as affine address or loop bound calculations in a
4.2 Avoiding Deadlock

If we implement the acquire as a simple busy wait may lead to deadlock: a process executing a busy wait uses processor resources, and this may prevent the (virtual) processor that is supposed to execute the “producer tile” from advancing. Because the programs we deal with are polyhedral, there is a simple way to avoid deadlock. It requires two elements.

- An additional legality condition on the HSD Schedule: for every input-output pair \((X, Y, D, f)\) in the RPRDG, the following condition must hold.

  \[
  \forall z \in D, \pi_X(z) \geq \pi_Y(f(z))
  \]

  Informally, this states that the producer-consumer mapping among processors is in a “lexicographically increasing” direction.

- Ensure (or develop a run-time mechanism that does so) that when virtual processors are mapped to physical resources, it is in the lexicographically increasing order. This ensures that once a processor starts, a non-preemptive scheduler will not deadlock.

5. Code Generation

This section first describes how to modify the PRDG \(\mathcal{H}\) to insert acquire and update statements. Then presents the code structure and challenges in implementations for different target platforms/runtimes (i.e. Pthreads, GPU/CUDA and X10).

Algorithm 2 describes the steps in modifying the PRDG \(\mathcal{H}\) to add acquire and update statements. We take PRDG \(\mathcal{H}\), residual PRDG \(\mathcal{H}'\) and HSD schedule as inputs. For each node in the residual PRDG \(\mathcal{H}'\) we add a new node to \(\mathcal{H}\). These nodes correspond to the acquire statements. The domain of the node is same as the domain of the corresponding node in \(\mathcal{H}'\). The schedule of the node is set such that it get executed as the first statement of the tile. The left hand side of the statement (XAcquire) is a dummy scalar variable. The right hand side of the statement (rexp) is a union of acquire function expressions, each with domain \(D_e\) - domain of corresponding edge in \(\mathcal{H}'\). acquire itself is a dummy function which takes dependences as arguments. These dependence functions are expressed as check functions with \(f(z)\) as argument. \(f(z)\) is a \(n\)-tuple of integers where first \(k\) integers corresponds to the virtual processor coordinate \(\vec{p}\) and rest corresponds to the time step \(t\) on which the current tile depends. For each target platform, check function must be implemented in such a way that it returns only when the \(\vec{p}\) reaches the time \(t\). For the update statement, we add only one node to \(\mathcal{H}\) and we set the domain as the union of domains of all the nodes in \(\mathcal{H}\). The schedule is set to execute it as the last statement in the tile. Memory allocation is \(z \rightarrow \pi(z)\) where the dimension of memory is \(k\) - number of processor dimensions. For rest of the nodes in the \(\mathcal{H}\) the schedule is updated so that they get executed in between acquire and update statements.

For the REX we add 2 nodes for acquire statements and one for update statement to the PRDG. Statement corresponds to edge \(e1\) in RPRDG is XAcquire1 = acquire(check(\(i_b - 1, j_b)\)) where the domain of the expression \(\{i_b, j_b| i_b > 0 \land j_b > 0\}\). The statement for \(e2\) is same except for the domain of the expression. The update statement is update(\(i_b, j_b\) with domain \(\{i_b, j_b | 0 \leq i_b \leq M_b \land 0 \leq j_b \leq N_b\}\)

The final step in code generation involves implementation of acquire and update functions for different target platforms.

Each target has its own language specific synchronization constructs. In order to show the expressiveness of our technique for a variety of targets, we provide target specific implementation for Pthreads here. The outline and issues for implementations in CUDA and X10 are described in an appendix that has been omitted due to space constraints.
5.1 Pthreads

Our Pthreads implementation relies on pthread mutex operations to control access to the queue of Blocks, and a blend of busy-waiting and mutex operations to implement of CHECK and UPDATE as each block progresses through tiles.

Figure 1 shows the code for the work claiming action to be performed by each thread to declare the ownership of a block of work. As this is used infrequently (once per block start), we expect the overall performance impact of pthread mutex operations to be negligible.

```c
void* Process_block() {
    int t1, t2;
    // mutexptr guards access to task_ptr
    // task_ptr always gives lex. minimum
    // unclaimed block
    pthread_mutex_lock (&mutexxptr);
    t1 = __Queue[task_ptr];
    task_ptr++;
    pthread_mutex_unlock (&mutexxptr);
    // this process now executes tiles,
    // possibly waiting at tile entry
    for (t2=0; t2<nTiles(t1); t2++)
        Tile(t1, t2);
}
```

Listing 1. pthread code for block claiming

Figures 2 and 3 show the code run upon entrance and exit to tile t of a processor p As this code is executed (repeatedly, in the case of UPDATE) for each tile, overhead must be kept low. Busy-waiting is an appealing option, at least in the frequent case of rectangular iteration spaces with uniform dependences, as (in such cases) a thread may arrive at the start of a tile at about the time the sources have completed, and furthermore we hope to minimize the number of times a thread switches away from its current block.

While the busy wait can reduce the energy cost of unnecessary switching among threads, lengthy busy waits can waste both time and energy. Thus, we perform a fixed number of iterations of busy waiting (2, as in Figure 2), after which we resort to pthread mutex operations.

```c
Listing 2. pthread code for CHECK
```

```
// Upon exit from time step t inside // a processor p
int update(int p, int t) {
    //mutex ensures exclusive access
    //to timestamp array
    pthread_mutex_lock (&mutexxsync);
    __STATUS_[b]=1;
    pthread_cond_broadcast(&sync_cv);
    pthread_mutex_unlock (&mutexxsync);
}
```

Listing 3. pthread code for UPDATE

5.2 CUDA

This section describes the CUDA code structure for REX and challenges of a GPGPU implementation. For the CUDA implementation of the hybrid schedules, we introduced several changes compared to the classic wavefront parallel implementation. In wavefront parallel code, there is a kernel call per each wavefront but for the hybrid schedule there is only one kernel call with \( t \) thread-blocks in a 1D grid (b is the size of the tile along processor dimension). Each thread-block responsible for the execution of one column of tiles. The code structure of the CUDA kernel is shown in Listing 4.

The update and check functions are executed only by the first thread of the thread-block and all the other threads wait on a `syncthreads()`. The update function simply set the value of array at processor index to the time index of the tile (see Listing 6). The check function is a busy wait until the value of array at processor index becomes the time index of the tile that depends on (see Listing 6).

There are CUDA specific issues that need solutions for this method to work. The variables that are accessed by multiple Streaming Multiprocessors (SMs) must be accessed in a way that it skips the L1 cache which is private to the SM. This can be achieved by skipping L1 for the whole kernel by specifying a compiler flag or for each variable individually.

The main challenge is avoiding deadlocks caused by the synchronization mechanism combined with the scheduling mechanism of CUDA thread-blocks. The execution order of thread-blocks is undefined. If we statically assign the 1st column of tiles to the 1st thread-block, 2nd column to the 2nd thread-block and so on, then we assume that the thread-blocks are scheduled in ascending order which contradicts with CUDA programming semantics. If the last set of thread-blocks get scheduled first, CUDA kernel deadlocks since all the thread blocks are waiting for previous thread-blocks to finish the depending tiles but there is no resources to schedule these thread-blocks. Hence, we need to allocate the column number dynamically to the thread-block at run-time. We use
a simple mechanism proposed by Yan et al. [54] based on atomic increment function in CUDA. The first computation of the thread-block is to increment a variable in global memory using first thread and use the returned value as the tile column to process (see Listing 7). Irrespective of which thread-block get scheduled next, it will pickup the next available tile column to process.

```c
// pick the next available column of tiles
if (threadIdx == 0)
    p = getNextColumnofTiles();
sycnthreads();
Status[0] = 0;

// T time iterates over tiles
for (t in 0...(T-1)) {
    // ACQUIRE / CHECK state
    if (threadIdx == 0)
        acquire(check(p-1, t));
sycnthreads();

    // Execute Tile(p, t);
    
    // UPDATE status
    if (threadIdx == 0)
        update(p, t);
sycnthreads();
}
```

Listing 4. CUDA code structure for REX-HSD

```c
check(p, t) {
    while (Status[p] < t) {;
}
}
```

Listing 5. CUDA code structure check function

```c
update(p, t) {
    Status[p] = t;
}
```

Listing 6. CUDA code structure update function

```c
getNextColumnofTiles(p, t) {
    return atomicInc(&columnCount);
}
```

Listing 7. CUDA code structure to get the next available column id of tiles

5.3 X10 Code Generation

As with the other target platforms/run-time systems, we can implement the Acquire/State protocol for the X10 language [12]. Listing 8 shows X10 code structure. We spawn new “activities” in X10, that correspond to asynchronously executing threads. The when clause does a wait until the State variable has a value of the current time stamp t. However, the wait construct in X10, does not cause a busy wait, rather the X10 run-time system manages waiting ‘activities, and liberates resources for other activities. Hence resources are available for, and X10 guarantees that there will be no deadlock “by construction.” So no special deadlock avoidance mechanism is needed. As soon as State is updated by the producing process, all activities waiting on its value are woken up and placed in the ready queue by the run-time system.

```x10
Status[0] = 1; // base case
// P processors
for (p in 0...(P-1))
    // spawn an activity per processor
    async {
        // T time
        for (t in 0...(T-1))
            // ACQUIRE / CHECK state
            when (Status[p-1] >= t) {
                // Execute Tile(p, t)
                Status[p] = t; // UPDATE
            }
    }
```

Listing 8. X10 code structure for Rex-HSD

6. Asymptotic Overhead

We now quantify three main overheads of our system (number of processes, number of synchronizations, and memory overhead) and show that they are better, asymptotically, than those of previously proposed methods. Recall that we are working with a program representation at the tile level, in the form of a tile PRDG, and that our schedules are n-dimensional, which corresponds to the maximum number of dimensions in the original computation. Each PRDG node represents a specific “tile signature” and is associated with a domain that enumerates the set of tile instances with that signature. These domains are polyhedral sets, parameterized by one or more size parameters. For simplicity of the presentation here, we assume that there is a single size parameter, S. Hence the asymptotic “work” complexity of the original program in $\Theta(S^n)$, a degree-n polynomial.

If we use fixed size tiling, the number of tiles remains $\Theta(S^n)$ asymptotically. If we use mono-parametric tiling using a single tile size parameter, b, and if we set $M = \frac{S}{b}$, it is $\Theta(M^n)$. Let us first discuss fixed size tiling.

**Lemma 7.** The total number of dependence instances is $\Theta(S^n)$.

The total number of dependences that are statically [c.f. dynamically] satisfied is $\Theta(S^n)$.

The proof follows from the fact that (i) every instance of a tile has a constant number of other tiles on which it depends, (ii) in the worst case all/n of the the dependences are statically satisfied, and (iii) tile size is a constant size.

**Synchronization Overhead** The immediate conclusion of this is that the overheads of any synchronization mechanism is as large as a constant factor of the total execution time. Note
that the mere “constant factor,” by which tiling mitigates this can be relatively high (e.g., many tens of thousands if the tile is $16 \times 32 \times 256$, a typical value).

As a result, the total number of run-time checks that the generated code will perform is, asymptotically the same regardless of what specific scheme is used, provided the proposed scheme is efficiently implemented. However, the specific choice of the schedule, as well as the nature of the underlying synchronization mechanism, may affect the constant factors.

This also implies that all proposed schemes, if implemented in the best possible way, will be only within a constant factor of each other.

Mono-parametric tiling provides us with an additional tunable parameter, the tile size $b$. As a result, the overhead is no longer a constant fraction of the total computation of the program, but rather, polynomial in $M = \frac{n}{b}$ of exactly the same degree. Also note that even with mono-parametric tiling, it is unlikely that $b$ will grow asymptotically at the same rate as $S$.

**Memory Overhead** We now address the memory overhead of our proposed scheme. Note that the overhead corresponds to the memory allocated to the auxiliary variable State as introduced in Section 3. Recall that each process maintains its “current state” as an $(n-k)$-tuple of integers, representing the most recent local time stamp it has completed. We use a shared array to maintain this.

**Lemma 8.** The memory overhead of the HSD schedule is $\Theta(S^b)$, a polynomial whose degree is the number of processor dimensions of the schedule.

The proof is straightforward since $\Theta(1)$ space is required for each virtual processor, and the union of the images of the domains of all the nodes in the PRDG yields a $k$-dimensional union of polyhedra, parameterized by the size parameter, $S$. The number of integer points in such a polyhedron is a $k$-degree polynomial.

And finally, note that as mentioned earlier, all previous techniques [3, 7, 8, 16, 30].

**Comparison with other techniques** We now compare the overhead of our approach with other techniques proposed in the literature. As stated above, all reasonable approaches have the same asymptotic complexity in terms of the number of synchronization, it’s only in the memory overhead that they may differ.

• Kong et al. [30] propose a technique that compiles tiled polyhedral programs to the OpenStream dataflow language [38]. In their approach, there is a “flag” that takes up one byte for every synchronization between tasks. Hence the memory overhead of their approach is $\Theta(S^n)$. Dathatri et al. [16] present a similar technique that targets distributed memory systems and therefore also handles communication. Their performance overheads are similar.

| Benchmark | Approach |
|-----------|----------|
| Name      | Work | #Tiles | #T | #S | HSD |
| J1D_F     | N^2 | 1 | 37/2 | - | - | 1 |
| J2D_F     | N^2 | 1 | 7/3 | - | - | 1.3 |
| W3D_F     | N^2 | 1 | - | - | - | 1.3 |
| REX3D,C   | N^3 | 1 | 3 | - | - | 1.2 |
| Chol,C    | N^3 | 1 | 3 | 3 | - | 1 |
| LTM,C     | N^3 | 1 | 3 | 3 | - | 1 |
| GKT,C     | N^3 | 1 | 3 | - | - | 1 |

Table 1. Comparison of Asymptotic Overhead of the number of tiles per task (#T) and number of synchronizations per tile (#S) of other methods with ours for a number of benchmarks. For J2D_F, Belvirani et al. [5] have a factor of $b$ more tiles than all other methods, so their numbers are not reported.

• Belvirani et al. [5] propose a similar scheme for GPUs, albeit for a limited class of programs. They too suffer from an overhead of is $\Theta(S^n)$.

• Boslica et al. [7] propose a scheme to compile affine loops to the DAGuE run-time system. The overhead arises from an interplay between their compile-time transformation and the DAGuE run-time. If the Insert_Tasks calls of their Figure 1 corresponds to the creation of a DAGuE “micro-task”, and these have a representation in DAGuE of size $>0$, and the micro-task creation does not itself wait for any executing micro-tasks, this produces a memory overhead of $\Theta(S^n)$.

Table 1 compares the asymptotic complexity of other approaches [5, 8, 16, 30] with ours for a number of benchmarks that we later use in our experimental validation: Jacobi-1D (J1D), Jacobi-1D (J1D) and Wave-3D (W3D) are all stencils, REX3D is a 3D iteration space version of REX, Chol is Cholesky decomposition (Chol) and Lower Triangular Matrix Inversion (LTMI) are dense linear algebra, and two versions of Optimal String Parenthesization (OSP and OSPGKT) are dynamic programming. The last letter after the benchmarks indicate whether fixed (F) or CART (C) tiling is used.

7. Experimental Evaluation

Hybrid Static/Dynamic Scheduling algorithm is applicable to all Polyhedral programs. We conduct experiments on different types of polyhedral programs. Our experiments include benchmarks from Dynamic programming, Linear Algebra and Stencil class of programs. To compare with performance of the same kernels generated by state-of-the-art compilers, we would like to compare our generated code with both static and dynamic schedules. However, due to the difficulties involved in acquiring some of the compilers, we were only able to compare our performance with statically scheduled code with OpenMP generated by 2 polyhedral compilers PLuTo and DTiler, which are known to achieve high performance.
Table 2. Benchmarks and Target Mappings

| Benchmark & Problem size | Target Mapping 1 | Target Mapping 2 |
|--------------------------|------------------|------------------|
| J1D,F 262k × 2.62M 64k × 640k | (t, i) → (t, 2t + i) t is processor i is time | (t, i, j) → (t, 2t + j, 2t + k) t, i is processor j, k is time |
| J2D,F 1k × 2k × 2k 0.5k × 1.25k × 1.25k | (t, i, j) → (t, 2t + j, 2t + k) t is processor i, j is time | (t, i, j) → (t, 2t + j, 2t + k) t, i is processor j, k is time |
| J1D,C 262k × 2.62M 64k × 640k | (t, i) → (t, i) i is processor t is time | (i, j, k) → (i, j, k) i, j is processor k is time |
| REX3D,C (2048)³ (2048)³ | (i, j, k) → (i, j, k) i is processor j, k is time | (i, j, k) → (i, j, k) i, j is processor k is time |
| Chol,C (2400)³ | (i, j, k) → (i, j, k) i is processor j, k is time | (i, j, k) → (i, j, k) i, j is processor k is time |
| LTMI,C (2400)³ | (i, j, k) → (i, j, k) i is processor j, k is time | (i, j, k) → (i, j, k) i, j is processor k is time |

2D iteration space and (256 × 256 × 256) for kernels with 3D iteration space. The stride of our search is set to 16 in each dimension for parametrically tiled kernels, and 32 in each dimension for kernels tiled with constant sizes. The highest achieved Gigaflop number is normalized with Pluto as the baseline and reported in Figure 4 and Figure 5. We measured the execution efficiency of the kernel using the best tile sizes discovered and resultant data is shown in Table 3. In this table, LLC_DM indicates the last level cache data misses event count in millions reported directly by running perf [33] to profile specific kernels. Sync Overhead refers to the percentage of time threads spent waiting for synchronizations to take place over the entire execution time. This is directly quoted from the report generated by Allinea. Total Energy refers to the total energy consumption of the program measured with unit milliwatt-hour. This figure consists of two parts: CPU and DRAM energy consumption. We measure two data separately. The former is, again, directly quoted from Allinea performance report and the latter is obtained by accessing PowerCap [34] interface and measuring energy readings for powerzone named “dram”. Both mechanisms gather energy data by utilizing Intel Running Average Power Limit (RAPL) interface.

From Figure 4 and 5, we observe that except for the case of LTMI, the performance of benchmarks using Hybrid Static/Dynamic Schedules are not significantly behind others using wavefront schedules generated by state-of-the-art polyhedral compilers. If we compare the performance of PLuTo generated code with HSD F and DTiler with HSD C, we can observe that the maximum performance loss was 2%(J1D) and 4%(Cholesky) respectively.

Moreover, as evidenced by our execution efficiency data on three of the four kernels with 3 dimensional iteration space, kernels with Hybrid Static/Dynamic Schedules are consistently the most energy-efficient ones. On average, our DTiler and PLuTo counterparts used 1.5x and 1.4x as much energy as HSD kernels consumed respectively. Therefore in many cases, adopting a Hybrid Static/Dynamic schedule can

Table 3. Machine configuration

| Architecture Parameters | Processor | E3-1231v3 | E5-2650v2 |
|-------------------------|-----------|-----------|-----------|
| Base Frequency          | 3.4 GHz   | 2.6 GHz   |
| Turbo Boost Frequency   | 3.8 GHz   | 3.4 GHz   |
| Number of Cores         | 4         | 8         |
| Number of Threads       | 8         | 16        |
| L3 Cache                | 8 MB      | 20 MB     |
| L2 Cache                | 256 KB/core | 256 KB/core |
| L1 Cache                | 12 KB/core | 32 KB/core |
| Instruction Set Extensions | AVX 2.0 | AVX |
| Max Memory Bandwidth    | 25.6 GB/sec | 59.7 GB/sec |
| Max # of Memory Channels| 2         | 4         |
improve the energy efficiency of a program at no cost or very little cost.

LTMI is indeed an outlier in our benchmarks. By examining the vectorization report we were able to identify that potential unaligned data access in parametric tiled programs (DTiler and Monoparam alike) can present significant obstacles to vectorization. However, this is a limitation of our input program, not a restriction of our runtime mechanism.

Lastly, our runtime scheduling policy mandates that each processor must follow a strictly lexicographically ascending order within the block and finish all of the work within a block before being preempted. Such policy essentially guarantees a multi-pass execution of the iteration space, which was previously proven [57] to exhibit energy efficiency but was only applicable to stencil kernels.

8. Related Work

The combination of automatic loop transformation and dataflow run-time synchronization has been explored on a number of occasions. Our work is novel in several respects; here, first we list the novel features of our approach and then discuss specific other systems.

Motivation for, and experimental validation of, prior dataflow run-time synchronization systems has focused primarily on execution speed, typically framed in terms of issues of idle processors and load balance, rather than energy use. Note that cache misses impact both speed and energy use. Although it may be possible to hide (via prefetching) the delay of a cache miss, it is not possible to offset the energy consumption. Our approach, like prior work, prevents the unnecessary idling of processors due to overly strict wavefront synchronization. Unlike other work, our approach can ensure locality statically, without reliance on luck or run-time locality analysis, thanks to our specification of process coordinates.

Our use of processor coordinates also provides an unusually tight coupling between compile-time transformation/scheduling and run-time scheduling and synchronization, resulting in scalability and overhead advantages for our implementation. By using one thread per slice of tiles rather than per tile, we reduce the number of threads, thus demanding less storage for thread contexts and performing fewer thread-switches. For synchronization overhead we use one integer per slice of tiles, rather than one Boolean value per tile.

Bosilca et al. [7] present a static analysis to derive the dataflow patterns of nested C loops that use calls to PLASMA library routines [18] to perform “tile-based dense linear algebra algorithms.” They use this inter-tile dataflow information to construct a set of tasks to be executed by the DAGuE run-time system [8]. DAGuE uses data-flow run-time synchronization, and employs a system of local and global queues in the run-time system, organized to “favor the cache reuse effect” [8, Section 3.2]. They also report execution speeds that beat ScaLAPACK and equal hand-tuned codes on a distributed system based on Xeon chips with with a total of 648 cores. They do not discuss energy consumption.

While this study focuses on a manycore system, a port of the PLASMA library and the DAGuE run-time system would provide a broad multi-target system. We believe that the dataflow

| Kernel | Code | LLC DM millions | Sync Overhead % | Total Energy milli-walthour |
|--------|------|-----------------|-----------------|-----------------------------|
|        |      |                 |                 |                             |
| J2D    | DTiler | 22              | 3.7x            | 15.10 10x                   |
| Pluto  |      | 39              | 6.5x            | 19.60 13x                   |
| HSD F  | 6     | 1.50            |                 | 20.2 1.4x                   |
| DTiler | 30    | 4.3x            | 4               | -0.72x 51.0 1.5x            |
| Pluto  | 7     | 1x              | 11.90           | 2.2x 58.7 1.7x              |
| HSD C  | 7     | 5.50            |                 | 34.8                 |
| Cholesky | DTiler | 16             | 5.3x            | 8.50 1x 15.7 1.6x          |
| Pluto  | 3     | 1x              | 28.60           | 3.4x 12.1 1.24x            |
| HSD C  | 3     | 8.30            |                 | 9.7                   |

Table 4. Execution Efficiency
among tiles of our tiled PRDG from Section 2.2 is essentially similar to the inter-tile dataflow collected by Bosilca et al., but note that our system is not restricted to a library of specific tile operations for square tiles [18, Section 2.1.1]. In our approach affinity between tiles of the same block arises automatically, rather than relying on a run-time system, and (as discussed earlier) our approach spawns asymptotically fewer threads.

Kong et al. [30] describe an algorithm that uses the polyhedral model to compile C loop nests into the task-parallel dataflow language OpenStream [38]. They motivate their work in terms of locality improvement between subsequent loops that manipulate the same array, rather than between the tiles of a single loop nest, and demonstrate that it can produce much lower memory traffic and execution time than two different approaches to loop fusion (as well as performance results for codes that require tiling). Like Bosilca et al., they do not measure energy consumption, and do not provide a static mechanism to ensure inter-tile locality (they note that affinity information could be derived from their representation, but “the current OpenStream implementation we used does not allow provision of scheduling guidelines and therefore locality opportunities were often lost due to the task firing policy of OpenStream” [30, Section 5]).

The PeerWave approach proposed by Belviranli et al. [5] uses data-flow runtime synchronization for GPGPU code that executes tiled loop nests. The approach was implemented only for GPGPU’s, and experimental results focus primarily on run-time speed, and the authors also noted a minor improvement in L2 cache misses but discuss its relevance to execution speed rather than energy consumption. Their synchronization code [5, Algorithm 2] uses one Boolean value per tile, rather than one integer per tile thread, leading to the potential scaling issues discussed above. Moreover, they only implemented the core of their approach for 2D iteration spaces, and handle higher dimensional domains by a sequence of PeerWave parallelizations of just the inner two loops. This causes them to lose significant benefits of tiling and locality.

One important special case of our analysis is the absence of any inter-block dataflow, i.e., “synchronization-free parallelism.” In this situation, all blocks can execute concurrently, each on its own processor. Techniques for uncovering schedules with synchronization-free parallelism date back at least to the work of Lim and Lam [32], and was extended to handle non-affine cases by Beletska et al. [4]. Our contribution focuses on issues of synchronization and locality, not scheduling, and is orthogonal to this and other scheduling work.

In addition to the aforementioned implemented systems, some early work suggested the use of dataflow-based synchronization without providing an actual implementation. Kelly and Pugh [29] discussed the possibility of moving barriers further out within a nest of loops, and using “post-and-wait style synchronization” as part of their mechanism for estimating communication cost. They did not, however, investigate actual code generation for such a system. Similarly, Wonnacott [52] suggested that tiles might start as soon as their input data was ready, but did not provide an implementation.

Alias and Plesco [1] proposed a similar process in the context of high-level synthesis of process networks where processes are linked through communication channel. Each channel is associated with a synchronization unit which might decide to freeze a producer or a consumer process if it is too advanced in its computation and might start violating the legality of the program.

Our simple idea of deadlock avoidance via lexico-positive communication in the processor space is based on early ideas from systolic array synthesis. Derrien et al. [17] showed that the lexico-positive interconnections were a necessary condition for Locally Parallel, Globally Sequential (LPGS) partitioning [23]. Greibl [24] proposed a scheme called “forward communication only” for an early polyhedral code generator, that imposed such a condition, although it was not strictly necessary for their codes.

A preliminary version of this work was presented as a poster; details are omitted for the double-blind review.

9. Conclusion

Traditionally the polyhedral model and many techniques at the foundation of languages and compilation have exploited the fact that information available at compile time, i.e., static analysis, would lead to efficient code. Recently, this idea has been challenged by the argument since machines are so incredibly complex, and therefore static techniques alone are not going to yield good performance, as evidenced by the popularity of auto-tuning, and data-flow techniques, even for highly regular, e.g., polyhedral programs.

The traditional wavefront approach to scheduling and synchronizing the execution of tiled loop nests has a number of significant drawbacks that have been observed by many authors. The overly strict synchronization semantics can cause needless idling of processors. It can force processors to flush useful data from cache to switch to another tile in the same wavefront. And the semantics of barrier synchronization do not fit some target infrastructures (e.g., CUDA) naturally.

We have shown that these problems can be resolved, while retaining the benefits of the polyhedral loop transformation framework, by (i) making the virtual processor coordinates an explicit part of the mapping. Within this single framework, we can generate code for diverse targets, allowing each to use appropriate mechanisms to address issues of synchronization mechanism, deadlock avoidance, data affinity, etc. Our performance tests of our Pthreads-based multi-core code shows that our approach uses less energy than other systems, either by reducing execution time or by providing competitive execution time with far better cache performance.
References

[1] C. Alias and A. Plesco. Procd de synthse automatique de circuits, dispositif et programme d’ordinateur associs. Patent Application, October 2015. Filing number PCT/FR2015/050969.

[2] Allinea. Allinea performance reports, 2016. URL http://www.allinea.com/products/allinea-performance-reports

[3] M. M. Baskaran, N. Vydyanathan, U. K. R. Bondhugula, J. Ramanujam, A. Rountev, and P. Sadayappan. Compiler-assisted dynamic scheduling for effective parallelization of loop nests on multicore processors. In Proceedings of the 14th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming, PPoPP ’09, pages 219–228, New York, NY, USA, 2009. ACM. ISBN 978-1-60558-397-6. doi:10.1145/1504176.1504209 URL http://doi.acm.org/10.1145/1504176.1504209

[4] A. Beletska, W. Bielecki, A. Cohen, and M. Palkowski. Synchronization-free automatic parallelization: Beyond affine iteration-space slicing. In Proceedings of the 22Nd International Conference on Languages and Compilers for Parallel Computing, LCPC’09, pages 233–246, Berlin, Heidelberg, 2010. Springer-Verlag. ISBN 3-642-13373-8, 978-3-642-13373-2. doi:10.1007/978-3-642-13374-9_16 URL http://dx.doi.org/10.1007/978-3-642-13374-9_16

[5] M. E. Belviranli, P. Deng, L. N. Bhuyan, R. Gupta, and Q. Zhu. PeerWave: Exploiting wavefront parallelism on gpus with peer-sm synchronization. In Proceedings of the 29th ACM on International Conference on Supercomputing, ICS ’15, pages 25–35, New York, NY, USA, 2015. ACM. ISBN 978-1-4503-3559-1. doi:10.1145/2751205.2751243 URL http://doi.acm.org/10.1145/2751205.2751243

[6] U. Bondhugula, A. Hartono, J. Ramanujam, and P. Sadayappan. Pluto: A practical and fully automatic polyhedral program optimization system. In ACM Conference on Programming Language Design and Implementation, pages 101–113, Tuscon, AZ, June 2008. ACM SIGPLAN.

[7] G. Bosilca, A. Bouteiller, A. Danalis, T. Herault, and J. Dongarra. From serial loops to parallel execution on distributed systems. In Proceedings of the 18th International Conference on Parallel Processing, Euro-Par’12, pages 246–257, Berlin, Heidelberg, 2012. Springer-Verlag. ISBN 978-3-642-32819-0. doi:10.1007/978-3-642-32820-6_25 URL http://dx.doi.org/10.1007/978-3-642-32820-6_25

[8] G. Bosilca, A. Bouteiller, A. Danalis, T. Herault, P. Lermariner, and J. Dongarra. Dague: A generic distributed dag engine for high performance computing. Parallel Comput., 38(1-2):37–51, Jan. 2012. ISSN 0167-8191. doi:10.1016/j.parco.2011.10.003 URL http://dx.doi.org/10.1016/j.parco.2011.10.003

[9] Z. Budimlić, V. Cavé, R. Raman, J. Shirako, S. Taşlılar, J. Zhao, and V. Sarkar. The design and implementation of the habanero-java parallel programming language. In Proceedings of the ACM International Conference Companion on Object Oriented Programming Languages and Applications Companion, OOPSLA ’11, pages 185–186, New York, NY, USA, 2011. ACM. ISBN 978-1-4503-0942-4. doi:10.1145/2048147.2048198 URL http://doi.acm.org/10.1145/2048147.2048198

[10] Budimlić, Zoran and Burke, Michael and Cavé, Vincent and Knobe, Kathleen and Lowney, Geoff and Newton, Ryan and Palsberg, Jens and Peixotto, David and Sarkar, Vivek and Schlimbach, Frank and Taşlılar, Sağan. Concurrent collections. Sci. Program., 18(3-4):203–217, Aug. 2010. ISSN 1058-9244. doi:10.1155/2010/521797 URL http://doi.acm.org/10.1155/2010/521797

[11] B. Chamberlain, D. Callahan, and H. Zima. Parallel programability and the chapel language. Int. J. High Perform. Comput. Appl., 21(3):291–312, Aug. 2007. ISSN 1094-3420. doi:10.1177/1094342007078442 URL http://dx.doi.org/10.1177/1094342007078442

[12] P. Charles, C. Grothoff, V. Saraswat, C. Donawa, A. Kielstra, K. Ebcioğlu, C. von Praun, and V. Sarkar. X10: An object-oriented approach to non-uniform cluster computing. In Proceedings of the 20th Annual ACM SIGPLAN Conference on Object-oriented Programming, Systems, Languages, and Applications, OOPSLA ’05, pages 519–538, New York, NY, USA, 2005. ACM. ISBN 1-59593-031-0. doi:10.1145/1094811.1094852 URL http://doi.acm.org/10.1145/1094811.1094852

[13] A. Darte and Y. Robert. Constructive methods for scheduling uniform loop nests. IEEE Transactions on Parallel and Distributed Systems, 5(8):814–822, Aug 1994.

[14] A. Darte and Y. Robert. Affine-by statement scheduling of uniform and affine loop nests over parametric domains. Journal of Parallel and Distributed Computing, 29(1):43–59, February 1995.

[15] A. Darte, L. Khachiyan, and Y. Robert. Linear scheduling is nearly optimal. Parallel Processing Letters, 1(2):73–82, December 1991.

[16] R. Dathathri, R. T. Mullapudi, and U. Bondhugula. Compiling affine loop nests for a dynamic scheduling runtime on shared and distributed memory. ACM Trans. Parallel Comput., 3(2):12:1–12:28, July 2016. ISSN 2329-4949. doi:10.1145/2948975 URL http://doi.acm.org/10.1145/2948975

[17] S. Derrien, S. Rajopadhye, and S. Sur-Kolay. Combined instruction and loop parallelism in array synthesis for FPGAs. In ISSS 2001: 14th International Symposium on System Synthesis, pages 165–170, Montreal, Canada, September 2001. ACM/IEEE.

[18] J. Dongarra, J. Kurzac, J. Langou, J. Langou, H. Ltaief, P. Luszczek, A. YarKhan, W. Alvaro, M. Faverge, A. Haidar, J. Hoffman, E. Agullo, A. Buttari, and B. Hadri. PLASMA users guide: Parallel linear algebra software for multicore architectures, version 2.3. Sep. 2010. URL http://icl.cs.utk.edu/projectsfiles/plasma/pdf/users_guide.pdf

[19] T. El-Ghazawi and L. Smith. Upc: Unified parallel c. In Proceedings of the 2006 ACM/IEEE Conference on Supercomputing, SC ’06, New York, NY, USA, 2006. ACM. ISBN 0-7695-2700-0. doi:10.1145/1188455.1188483 URL http://doi.acm.org/10.1145/1188455.1188483

[20] P. Feautrier. Dataflow analysis of array and scalar references. International Journal of Parallel Programming, 20(1):23–53,
[21] P. Feautrier. Some efficient solutions to the affine scheduling problem. Part I. one-dimensional time. *International Journal of Parallel Programming*, 21(5):313–347, 1992.

[22] P. Feautrier. Some efficient solutions to the affine scheduling problem. Part II. multidimensional time. *International Journal of Parallel Programming*, 21(6):389–420, 1992.

[23] J. A. B. Fortes and D. Moldovan. Data broadcasting in linearly scheduled array processors. In *Proceedings, 11th Annual Symposium on Computer Architecture*, pages 224–231, 1984.

[24] M. Griebl, C. Lengauer, and S. Wetzal. Code generation in the polytope model. In *Proc. Int. Conf. on Parallel Architectures and Compilation Techniques (PACT’98)*, pages 106–111. IEEE Computer Society Press, 1998.

[25] P. N. Hilfinger, D. Bonachea, D. Gay, S. Graham, B. Liblit, G. Pike, and K. Yelick. Titanium language reference manual. Technical report, Berkeley, CA, USA, 2001.

[26] IEEE. ISO/IEC/IEEE Standard 9945:2009: Information technology – Portable Operating System Interface (POSIX) Base Specifications. ISO/IEC/IEEE Std. 9945:2009, 2009. URL http://www.iso.org/iso/iso_catalogue/catalogue_tc/catalogue_detail.htm?csnumber=50516.

[27] G. Iooss, S. Rajopadhye, C. Alias, and Y. Zou. Monoparametric tiling is a polyhedral transformation. Research Report RR-8802, INRIA Grenoble - Rhône-Alpes ; CNRS, Oct. 2015. URL https://hal.inria.fr/hal-01219452.

[28] F. Irigoin and R. Triolet. Supernode partitioning. In *Conference Record of the Fifteenth ACM Symposium on Principles of Programming Languages*, pages 319–329, 1988.

[29] W. Kelly and W. Pugh. Minimizing communication while preserving parallelism. In *Proceedings of the 1996 International Conference on Supercomputing*, May 1996.

[30] M. Kong, A. Pop, L.-N. Pouchet, R. Govindarajan, A. Cohen, and P. Sadayappan. Compiler/runtime framework for dynamic dataflow parallelization of tiled programs. *ACM Trans. Archit. Code Optim.*, 11(4):61:1–61:30, Jan. 2015. ISSN 1544-3566. doi: 10.1145/2687652 URL http://doi.acm.org/10.1145/2687652.

[31] C. E. Leiserson. The cilk+ concurrency platform. In *Proceedings of the 46th Annual Design Automation Conference*, DAC ’09, pages 522–527, New York, NY, USA, 2009. ACM. ISBN 978-1-60558-497-3. doi: 10.1145/1629911.1630048 URL http://doi.acm.org/10.1145/1629911.1630048.

[32] A. W. Lim and M. S. Lam. Maximizing parallelism and minimizing synchronization with affine transforms. In *Proceedings of the 24th ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages*, POPL ’97, pages 201–214, New York, NY, USA, 1997. ACM. ISBN 0-89791-853-3. doi: 10.1145/263699.263719 URL http://doi.acm.org/10.1145/263699.263719.

[33] I. Linux Kernel Organization. perf: Linux profiling with performance counters, 2016. URL https://perf.wiki.kernel.org/index.php/Main_Page.

[34] I. Linux Kernel Organization. Power capping framework, 2016. URL https://www.kernel.org/doc/documentation/power/powercap/powercap.txt.

[35] C. Maurus, P. Quinton, S. Rajopadhye, and Y. Saouter. Scheduling affine parameterized recurrences by means of variable dependent timing functions. In S. Y. Kung and E. Swartzlander, editors, *International Conference on Application Specific Array Processing*, pages 100–110, Princeton, New Jersey, Sept 1990. IEEE Computer Society.

[36] B. Meister, A. Leung, N. Vasilache, D. Wohlford, C. Bastoul, and R. Lethin. Productivity via automatic code generation for FGAS platforms with the R-Stream compiler. In *APGAS’09 Workshop on Asynchrony in the FGAS Programming Model*, Yorktown Heights, New York, June 2009.

[37] J. Nickolls, I. Buck, M. Garland, and K. Skadron. Scalable parallel programming with cuda. *Queue*, 6(2):40–53, Mar. 2008. ISSN 1542-7730. doi: 10.1145/1365490.1365500 URL http://doi.acm.org/10.1145/1365490.1365500.

[38] A. Pop and A. Cohen. OpenStream: Expressiveness and data-flow compilation of OpenMP streaming programs. *ACM Trans. Archit. Code Optim.*, 9(4):53:1–53:25, Jan. 2013. ISSN 1544-3566. doi: 10.1145/2400682.2400712 URL http://doi.acm.org/10.1145/2400682.2400712.

[39] L. Pouchet, U. Bondhugula, C. Bastoul, A. Cohen, and J. Ramanujam. Combined iterative and model-driven optimization in an automatic parallelization framework. In *In SC ’10: International Conference on High Performance Computing, Networking, Storage and Analysis*, pages 1–11, New Orleans, LA, 2010. IEEE Computer Society Press.

[40] W. Pugh. The Omega test: a fast and practical integer programming algorithm for dependence analysis. *Communications of the ACM*, 35(8):102–114, Aug. 1992.

[41] W. Pugh and D. Wonnacott. Eliminating false data dependencies using the Omega test. In *SIGPLAN Conference on Programming Language Design and Implementation*, pages 140–151, San Francisco, California, June 1992.

[42] W. Pugh and D. Wonnacott. Constraint-based array dependence analysis. *ACM Trans. Program. Lang. Syst.*, 20(3):635–678, 1998. ISSN 0164-0925.

[43] P. Quinton and V. Van Dongen. The mapping of linear recurrence equations on regular arrays. *Journal of VLSI Signal Processing*, 1(2):95–113, 1989.

[44] S. V. Rajopadhye, S. Purushothaman, and R. M. Fujimoto. On synthesizing systolic arrays from recurrence equations with linear dependencies. In *Proceedings, Sixth Conference on Foundations of Software Technology and Theoretical Computer Science*, pages 488–503, New Delhi, India, December 1986. Springer Verlag, LNCS 241.

[45] W. Ranasinghe. Reducing off-chip memory accesses of wavefront parallel programs in graphics processing units. Master’s thesis, Colorado State University, Computer Science Department, 2014.

[46] J. Reinders. *Intel Threading Building Blocks*. O’Reilly & Associates, Inc., Sebastopol, CA, USA, first edition, 2007. ISBN 9780596514808.

[47] M. Sato, Y. Kodama, S. Sakai, Y. Yamaguchi, and Y. Koumura. Thread-based programming for the EM-4 hybrid dataflow machine. In *Proceedings of the 19th Annual International
[48] B. Theobald. Kevin. *Earth: An Efficient Architecture for Running Threads*. PhD thesis, McGill University, Montreal, Canada, May 1999.

[49] S. Verdoolaege. *isl: An integer set library for the polyhedral model*. In *Proceedings of the Third International Congress Conference on Mathematical Software*, ICMS’10, pages 299–302, Berlin, Heidelberg, 2010. Springer-Verlag. ISBN 3-642-15581-2, 978-3-642-15581-9. URL http://dl.acm.org/citation.cfm?id=1888390.1888455.

[50] S. Verdoolaege, S. Guelton, T. Grosse, and A. Cohen. *Schedule trees*. In *IMPACT’14: International Workshop on Polyhedral Compilation Techniques*, Vienna, Austria, January 2014.

[51] M. E. Wolf and M. S. Lam. *A data locality optimizing algorithm*. In *ACM SIGPLAN ’91 Conference on Programming Language Design and Implementation*, 1991.

[52] D. Wonnacott. *Using Time Skewing to eliminate idle time due to memory bandwidth and network limitations*. In *International Parallel and Distributed Processing Symposium*. IEEE, May 2000.

[53] D. Wonnacott. *Achieving scalable locality with Time Skewing*. *International Journal of Parallel Programming*, 30(3):181–221, June 2002.

[54] S. Yan, G. Long, and Y. Zhang. *Streamscan: Fast scan algorithms for GPUs without global barrier synchronization*. In *Proceedings of the 18th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, PPoPP ’13, pages 229–238, New York, NY, USA, 2013. ACM. ISBN 978-1-4503-1922-5. doi:10.1145/2442516.2442539 URL http://doi.acm.org/10.1145/2442516.2442539.

[55] T. Yuki, V. Basupalli, G. Gupta, G. Iooss, D. Kim, T. Pathan, P. Srinivas, Y. Zou, and S. Rajopadhye. *Alphaz: A system for analysis, transformation, and code generation in the polyhedral equational model*. Technical report, Technical Report CS-12-101, Colorado State University, 2012.

[56] T. Yuki, P. Feautrier, S. Rajopadhye, and V. Saraswat. *Array dataflow analysis for polyhedral x10 programs*. In *Proceedings of the 18th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, pages 23–34, New York, NY, USA, 2013. ACM. ISBN 978-1-4503-1922-5. doi:10.1145/2442516.2442520 URL http://doi.acm.org/10.1145/2442516.2442520.

[57] Y. Zou and S. Rajopadhye. *Automatic energy efficient parallelization of uniform dependence computations*. In *Proceedings of the 29th ACM on International Conference on Supercomputing*, ICS ’15, pages 373–382, New York, NY, USA, 2015. ACM. ISBN 978-1-4503-3559-1. doi:10.1145/2751205.2751245 URL http://doi.acm.org/10.1145/2751205.2751245.

[58] S. Zuckerman, J. Suetterlein, R. Knauerhase, and G. R. Gao. Using a "codelet" program execution model for exascale machines: Position paper. In *Proceedings of the 1st International Workshop on Adaptive Self-Tuning Computing Sys-