A Linear Algebraic Approach to Model Parallelism in Deep Learning

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Abstract

Training deep neural networks (DNNs) in large-cluster computing environments is increasingly necessary, as networks grow in size and complexity. Local memory and processing limitations require robust data and model parallelism for crossing compute node boundaries. We propose a linear-algebraic approach to model parallelism in deep learning, which allows parallel distribution of any tensor in the DNN. Rather than rely on automatic differentiation tools, which do not universally support distributed memory parallelism models, we show that parallel data movement operations, e.g., broadcast, sum-reduce, and halo exchange, are linear operators, and by defining the relevant spaces and inner products, we manually develop the adjoint, or backward, operators required for gradient-based training of DNNs. We build distributed DNN layers using these parallel primitives, composed with sequential layer implementations, and demonstrate their application by building and training a distributed DNN using DistDL, a PyTorch and MPI-based distributed deep learning toolkit.

1 Motivation & Background

Training deep neural networks (DNNs) on extreme-scale super computers is a challenging problem, however, it is increasingly a necessary component of modern computational and data science workflows. For extremely large problems in scientific machine learning (SciML; e.g., those in physics-guided ML [1] which require integration of parallel partial differential equation (PDE) solvers) [2,3] and other large multi-dimensional or volumetric data processing problems, such as video processing or seismic data processing, limitations on local memory and processing power (even with modern large memory GPUs) require robust parallelism models to cross the compute-node boundary. Data parallelism is ubiquitous in deep learning, but model parallelism has been harder to achieve. In particular, this is because the “model” in large deep neural networks is highly irregular and has no uniform spatial structure to induce the sparseness that is typical in large-scale parallel problems. To achieve a fully parallelized deep neural network training algorithm, we focus on enabling parallelism by distributing any tensor in a network including learnable parameters, inputs, and outputs.

Recently, multiple frameworks have been developed which partially address the distributed deep learning problem. These frameworks build from, or into, popular frameworks such as PyTorch [4] and Tensorflow [5], which natively support data parallelism, to add support for pipelining [6], or limited support for some model parallelism over some aspects of the network [7,8,9,10]. Native support for distributed learning is also slowly appearing in the popular frameworks. Parallelism in individual aspects of deep learning, such as convolutional layers has also been investigated [11], as well as application of some applications to parallel physics-driven network structures in, e.g., seismic

*https://rjh.io

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inversion \cite{12}. However, current approaches only provide partial solutions and we lack a complete, integrated framework for treating the distributed learning problem. Here, we aim to provide such a framework. While this manuscript generally addresses “model” parallelism within a single network gradient calculation, our framework readily admits classical data parallelism and pipelining.

Automatic (or algorithmic) differentiation (AD) is among the most important tools that computational science has contributed to the democratization of deep learning. Given an implementation of a computer algorithm for evaluating a non-linear function $F$, forward-mode AD produces an implementation of an algorithm for evaluating the action of the $F$, the Jacobian of $F$, and backward- or adjoint-mode AD produces an algorithm for evaluating the action of $F^*$, the adjoint of the Jacobian of $F$ \cite{13}. In computational science problems, such as PDE-constrained optimization \cite{14}, AD is frequently applied to forward computation kernels to develop correct adjoint kernels necessary for numerical optimization. In deep learning, it is used for similar tasks in the construction of gradient calculations needed to invert for the parameters in composite non-linear functions, such as DNNs.

However, AD tools, especially those in widely used deep learning frameworks, have limited support for the message-passing operations required to run codes on distributed memory supercomputers, hampering the development of fully parallel deep learning codes. Historically, some AD tools \cite{15} have provided limited support for differentiating distributed memory parallel codes, e.g., enabled via the Message Passing Interface (MPI) \cite{16}. However, such support is not ubiquitous. Fortunately, as we will show, the operations necessary for distributed memory parallelism are linear. Consequently, we do not need to appeal to AD to generate the adjoint operations needed for gradient calculation. Instead, we exploit the definition of the adjoint operator, careful definitions of the spaces they act upon, and the inner products on those spaces, to build a set of primitive operations, and their adjoints, to describe data movement in computers and distributed memory supercomputers.

As we will demonstrate, these operations can be embedded into a deep learning framework using the framework’s native interface for specifying new functions, and composited with existing network layers or functions. Thus, the data movement operations, and their adjoints, become merely another function for the framework’s automatic differentiation tool to operate on. We have implemented a proof-of-concept in our distributed deep learning tool, DistDL, using MPI (via mpi4py \cite{17}) and PyTorch for CPU functions. This restriction is not a limitation of our model, only a restriction of our current implementation: there are no major technological impediments to transitioning this model to large-scale hybrid CPU-GPU supercomputers.

2 Linear algebraic memory model

Let $\mathbb{F}$ be the space of relevant computer numbers, e.g., integers or IEEE floating point numbers. If $F : \mathbb{F}^m \rightarrow \mathbb{F}^n$ is a linear operator, then $F = \mathcal{F}$ is its Jacobian and the adjoint of the Jacobian, $F^*$, is defined by the adjoint relationship,

$$\langle \mathcal{F} x, y \rangle_{\mathbb{F}^n} = \langle x, \mathcal{F}^* y \rangle_{\mathbb{F}^m},$$

where $\mathbb{F}^k$ represents a $k$-length subset of a computer’s memory. For the purposes of this development, we take the inner product to be the standard Euclidean inner product,$^3$

$$\langle a, b \rangle_{\mathbb{F}^k} = \sum_{i=0}^{k-1} a_i b_i \quad a, b \in \mathbb{F}^k.$$  \hspace{1cm} (2)

Thus, with a concrete implementation of $F$, we can derive and implement concretely the coherent associated $F^*$, and we can exploit these implementations in a deep learning framework’s AD tool, such as PyTorch’s autograd. In general, the data realized in the subsets of the memory are subsets of tensors. In defining these operations, we make no assumptions about the rank, ordering, size, or layout of the tensor, though these do matter in a practical implementation.

To build parallel primitives for deep learning, we must first understand the nature of $\mathbb{F}^k$ and of the operators on it. In the ensuing discussion, we consider the concept of “a computer’s memory” to be extremely inclusive. While it is easiest to consider $\mathbb{F}^k$ to be the main memory of a single CPU of a

$^3$We avoid the term communication because our model applies beyond classical distributed memory settings.

$^1$When $F$ is the space of floating point numbers, the inner product must be constructed carefully, especially in parallel environments, because floating point arithmetic is not commutative.
single compute node (or worker), this framework admits auxiliary memories, such as those attached to GPU accelerators, remote memory on other compute nodes or cloud instances, or even disk.

Here, we develop linear representations of primitive memory operations and their adjoints, which we will use to develop parallel data movement primitives and more complex distributed neural network layer structures. We are careful to point out that the manual procedure that we outline is essentially how adjoint-mode AD works. However, we find it useful to view these operations from a linear-algebraic perspective, rather than from the typical computation-graph perspective used in AD. Most AD tools are generally incapable of handling all possible data movement operations within our inclusive memory model, so we must be able to build the operations manually. Thus, our framework provides the theoretical glue necessary to implement these operations when they are not available natively. Moreover, in manual implementations we can make some optimizations that AD-generated codes cannot make, as some operations appear only implicitly in forward codes, but must appear explicitly in adjoint codes, or vice versa. In this manuscript we err on the side of being explicit, while practical implementations may not explicitly include all operations, except during validation.

**Allocation** The allocation of a subset of memory, to be realized by \( x_b = 0_b \), for a program that already has space for \( x_a \) available, is a linear operation \( A_b : \mathbb{F}^m \to \mathbb{F}^n \),

\[
A_b x = \begin{bmatrix} I_a \\ O_b \end{bmatrix} [x_a] = \begin{bmatrix} x_a \\ 0_b \end{bmatrix},
\]

(3)

where \( I_a \) is an identity operator on the original subset and \( O_b \) is a zero operator on the new subset. The adjoint of allocation, \( A_b^* \), is derived through the standard inner product, which we detail in Appendix A. \( A_b^* \) is the transpose of \( A_b \), and acts on a realization \( y \) from \( \mathbb{F}^n \),

\[
A_b^* y = A^T_b y = [I_a \ O_b] \begin{bmatrix} y_a \\ y_b \end{bmatrix} = [y_a].
\]

(4)

The adjoint of allocation is thus deallocation, and similarly the deallocation primitive \( D_b \) has allocation as its adjoint, \( D_b^* = A_b \).

We use a liberal definition of “allocation” that goes beyond classical memory allocation operations (e.g., \texttt{malloc}() in C) because these operations are describing the semantics of an implementation, not syntax. Allocation is any operation which brings memory into scope, including formal allocation, the addition of data to the stack, creation of a reference, etc. In the context of a neural network layer, this means that if data is not checkpointed for use in the adjoint phase during the forward phase, it goes out of scope or is “deallocated” when the forward function completes.

**Clear** The clear operator, \( K_b \), sets a realization of a subset of \( x \), \( x_b \), to \( 0 \). The operation, \( K_b : \mathbb{F}^m \to \mathbb{F}^m \), is realized by,

\[
K_b x = \begin{bmatrix} I_a \\ O_b \end{bmatrix} [x_a] = \begin{bmatrix} x_a \\ 0_b \end{bmatrix},
\]

(5)

and it is trivially self-adjoint, \( K_b^* = K_b \).

**Add** The add operator, \( S_{a \to b} : \mathbb{F}^m \to \mathbb{F}^m \), performs in-place summation \( x_a \) to \( x_b \),

\[
S_{a \to b} x = \begin{bmatrix} I_a \\ I_a \end{bmatrix} [x_a] = \begin{bmatrix} x_a \\ x_a + x_b \end{bmatrix}.
\]

(6)

The adjoint of an add is also an add, but in the reverse direction,

\[
S_{a \to b}^* y = \begin{bmatrix} I_a \\ I_a \end{bmatrix} [y_a] = \begin{bmatrix} y_a + y_b \\ y_b \end{bmatrix} = S_{b \to a} y.
\]

(7)

**Copy** The copy operator, which copies data from the subset \( x_a \) to \( x_b \), has both in-place and out-of-place forms, made distinct only by the semantics of an implementation. An in-place copy is the composition of clear and add while an out-of-place copy is the composition of allocate and add. This may seem pedantic, as “\( x = c \);” is more concise than “\( x = x * 0 \); \( x = x + c \);”, but the

\[\text{The adjoint is strongly dependent on the inner product and is not always the matrix transpose.} \]

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distinction becomes important for defining higher-level operations. We define the operators and adjoints below, and justify the construction in Appendix A.

\[
\begin{align*}
    C_{a \rightarrow b} &= S_{a \rightarrow b} K_b \\
    C_{a \rightarrow b}^* &= K_b S_{b \rightarrow a}
\end{align*}
\]

The choice of in-place or out-of-place operation impacts only implementation decisions when defining higher-level operations, so we do not distinguish them in the sequel.

**Move** The move operator moves a realization \( x_a \) to \( x_b \), and similar to copy, has in-place and out-of-place forms given below, which we justify in the Appendix A.

\[
\begin{align*}
    M_{a \rightarrow b} &= K_a S_{a \rightarrow b} K_b \\
    M_{a \rightarrow b}^* &= K_b S_{b \rightarrow a} K_a = M_{b \rightarrow a}
\end{align*}
\]

Again, the choice of in-place or out-of-place forms impacts only some implementation decisions.

### 3 Linear algebraic primitives for data movement

Using these primitive memory operations, we construct linear operators representing several standard parallel data movement primitives and their adjoints. To accommodate operations on distributed memory computers, we now consider the definition of the memory space to include all memories on a compute cluster. While we discuss operations as if the parallel workers are distinct compute nodes, this distinction is made explicit only by the communication library, such as MPI, and our model is independent of communication back-end. In the ensuing discussion, we will generally assume that operations are out-of-place – communicating data results in a new memory allocation on the “receiving” worker. While this is generally not best practice in large-scale simulation, out-of-place operations better fit PyTorch’s computation and AD model. The one exception in this presentation is the halo exchange, which we will describe as an in-place operation, following from standard practice in large-scale simulation. Adapting internal mechanics of out-of-place operations to in-place operations has no bearing on the outcome. Thus, if such an implementation is preferred in performance environments, it is of minor consequence.

For brevity, we will not show allocations or deallocations, but their implicit presence may be felt. While we generally express data movement using copy, if the primal realization is deallocated without further use after the copy, the copy may be expressed as a move. In practice, many operations we make explicit are needed only theoretically. For example, in the adjoint halo exchange we express clears on the exchange buffers for mathematical consistency, but these are handled implicitly when assigning data to the buffers.

**Send and Receive** The most basic distributed memory data movement operation, from which all others can be derived, is the send-receive operator. In a concrete implementation, the send-receive pair requires two function calls (send and receive) by separate workers, but from a linear-algebraic perspective, the send-receive operator is simply a copy \( C_{a \rightarrow b} \), where the subsets \( x_a \) and \( x_b \) are on the two different workers. Consequently, the adjoint also follows from above. While the send-receive operation is not self-adjoint, a practical implementation of its adjoint requires a receive-send pair, but the add operation may not be equivalent to assignment, as it is in the forward operation.

**Scatter and Gather** The scatter primitive is essentially a sequence of send-receive pairs, where subsets of \( x_a \) are copied to multiple other workers. Linear-algebraically, this is a block-diagonal matrix with send-receive blocks. The adjoint derivation follows from the previous discussion. If the data movement operations are equivalent to move, then the adjoint operation becomes an instance of the gather primitive, which collects data from multiple workers into one subset on one worker, otherwise communication still follows the gather pattern but the summation must be respected.

**Broadcast** A critical parallel primitive, the broadcast, is identified and implemented in many distributed memory deep learning tools \([4, 7, 8]\) because it is necessary to distribute network parameters
to multiple workers. A broadcast, $B_{a→\{k\}}$, is a linear operator from a one realization on subset $x_a$ to $k$ realizations on subsets $x_0, \ldots, x_{k-1}$ and is $k$ copy operations,

$$B_{a→\{k\}} x_a = \begin{bmatrix} C_{a→0} \\ C_{a→1} \\ \vdots \\ C_{a→k-1} \end{bmatrix} x_a = \begin{bmatrix} x_a \\ \vdots \\ x_a \end{bmatrix} = x_{\{k\}}.$$  \hfill (8)

While the above “implementation” scales linearly with $k$, the canonical logarithmic broadcast implementation has an equivalent representation. For in-place versions, the first copy is an identity operator. Then, the adjoint of the broadcast is,

$$B_{a→\{k\}}^* y_{\{k\}} = \begin{bmatrix} C_{a→0}^* \\ C_{a→1}^* \\ \vdots \\ C_{a→k-1}^* \end{bmatrix} y_{\{k\}} = \sum_{i=0}^{k-1} K_i S_i → a y_i = y_a.$$  \hfill (9)

The summation term is the key to understanding the adjoint broadcast implementation: the adjoint of the broadcast is a sum-reduction.

**Sum-reduce and all-reduce**  The sum-reduce primitive, of equal importance with the broadcast, represents summation of $k$ subsets into $x_a$ and its derivation follows the reverse of the broadcast. The sum-reduce operator, $R_{\{k\}→a} = B_{a→\{k\}}^*$, and its adjoint, $R_{\{k\}→a}^* = B_{a→\{k\}}$, is a broadcast.

While the all-reduce operator is not necessary in our implementation, some distributed convolution formulations make use of the operation \[11\]. In our framework, an all-reduce is simply the composition of a sum-reduce and a broadcast, $A_{\{k\}→\{a\}} = B_{a→\{k\}} R_{\{k\}→a}$, and is trivially self-adjoint, as $A_{\{k\}→\{k\}} = R_{\{k\}→a} B_{a→\{k\}} = B_{a→\{k\}} R_{\{k\}→a} = A_{\{k\}→\{k\}}$.

**Generalized all-to-all**  In a DNN layer, the input, output, and parameter tensors have different dimension and shape, which strongly influences load balance. Consequently, parallel performance may require a change in a tensor’s parallel decomposition when composing layers. This is performed by an all-to-all operation, which takes the appearance of a matrix transpose, and is also referred to as a shuffle \[11\]. For generalized tensors with generalized partitions, data stored in one worker’s memory may need to be copied to any other worker in the destination partition, essentially a scatter operation. Then, in a linear algebraic sense, the all-to-all operation is a block permutation matrix, where the blocks are send-receive operators for all simultaneous scatters. A similar result as for gathers above, holds for the adjoint of all-to-all.

**Halo exchange**  In classical large-scale simulation, a decomposition of the relevant spatial domain allows for effective model parallelism: large variables are distributed to different workers according to the spatial decomposition. When a differential operator is sparse, physical interactions are local and minimal data, found near the domain boundaries, needs to be shared between adjacent workers. In neural networks, analogous situations arise for layers featuring small, sliding kernels, such as convolutional layers and pooling layers. For each worker to correctly apply the computational kernel, minimal data, found near the domain boundaries, needs to be shared between adjacent workers. The exchange of this boundary data between workers is known as a ghost exchange or halo exchange.

In finite difference-based simulation, the halo regions are regular in size. In \[11\], a halo exchange algorithm for convolutional kernels is presented in the context of a convolutional layer, assuming similar regularity. Compact, centered kernels, such as convolutional kernels without striding or dilation, with carefully chosen domain decompositions will tend to have regularly sized halo regions. However, for many use common use-cases in deep learning, e.g., for one-sided pooling kernels, for centered kernels without tailored partition sizes, and when load balance is driven by the output tensor, we have observed that halo regions can have unbalanced structure. We have illustrated a number of examples of this irregular structure in Appendix \[H\].

Due to this irregular structure, we use the linear-algebraic framework to define an algorithm for generalized halo exchange in distributed deep learning, as well as its adjoint. In our algorithm, we neither make any assumptions on the rank of the input and output tensors (only that they are the same) nor the structure of the kernel. As computational load on a given worker is driven by the volume
of that worker’s output subtensor, we assume that the output tensor is optimally load balanced and derive the necessary input tensor halo sizes in each dimension from there. We assume that the tensors are sensibly decomposed, relative to kernel size, so that halos require data from directly adjacent worker neighbors only. The portion of the distributed tensor that is owned by a worker is the bulk region and the halo exchange ensures that a worker has copies of the necessary portions of its neighbor’s bulk regions in its halo region.

All halo regions, both left and right, from all dimensions of a rank-\(d\) tensor may have different thickness. The thicknesses are determined by the minimum and maximum global indices of the worker’s output tensor and the size, stride, dilation, and padding parameters of the kernel. From a linear-algebraic perspective, the halo exchange is a sequence of send-receive operations. For efficiency, we assume that the halo exchange is in-place, so the input and output realizations are on the same memory subset. Following the linear-algebraic view, the halo exchange operator for one worker exchanging with its neighboring workers in one dimension is,

\[ H = K_T C_T C_E K_S, \]  

where \(K_S\) the setup operator, clears the exchange buffers, \(C_E\) the exchange operator, copies from the bulk region to the send buffer, \(C_T\) the teardown operator, clears from the current worker’s send buffer to the neighboring worker’s receive buffer, and vice versa, \(C_U\) the unpack operator, copies from the receive buffer to the halo region, \(K_T\) the teardown operator, clears on the exchange buffers. For \(d\)-rank tensors, the exchange is performed one dimension at a time, in a nested manner to ensure proper communication of data in corner cases [18]. Thus, the full exchange operator is,

\[ H = K_{T_{d-1}} C_{U_{d-1}} C_{E_{d-1}} C_{P_{d-1}} K_{S_{d-1}} \ldots K_T C_U C_E C_P K_S, \]  

with corresponding adjoint,

\[ H^* = K_{S_{d}} C_P C_E C_U K_{T_{d}} K_{S_{d}} C_P C_E C_U K_{T_{d}} \ldots K_{S_{d-1}} C_P C_E C_P K_{S_{d-1}}. \]

In practice, clearing the exchange buffers is implicit. We illustrate the generalized, unbalanced forward and adjoint halo exchanges in Appendix B. This view justifies an observation that has been used in production PDE-constrained optimization codes for some time [19]: in the adjoint of halo exchange, there is an add operation into the bulk tensor. This is ultimately because the three copy operations, at the center of each part of the exchange, copy data from the bulk of one worker to the halo region of another and the ensuing adjoint phase must produce an add.

**Implementation** In our distributed deep learning library, DistDL, we have provided implementations of many necessary primitives for PyTorch autograd. In parallel environments, verification of correctness using numerical gradient validation is difficult. Fortunately, data movement operations are linear and we can exploit the fact that the forward operator is its own Jacobian, \(F = F^*\), and the definition of the adjoint to establish an equivalent test for correctness. We say that an implementation of \(F^*\) is coherent with \(F\) if the adjoint test is satisfied,

\[
\frac{\langle Fx, y \rangle_{\mathbb{F}^n} - \langle x, F^* y \rangle_{\mathbb{F}^m}}{\max \{\|Fx\|_{\mathbb{F}^n}, \|y\|_{\mathbb{F}^m}, \|x\|_{\mathbb{F}^n}, \|F^* y\|_{\mathbb{F}^m}\}} < \varepsilon \quad \forall x \in \mathbb{F}^m, \forall y \in \mathbb{F}^n.
\]  

4 Model parallel layers

The parallel primitives defined in the previous section are sufficient for assembling implementations of common neural network layer functions. We broadly categorize neural network layers into three classes: sparse layers, dense layers, and point-wise layers. The classes are distinguished by the locality of interaction between degrees-of-freedom in the input tensor due to the layer function. This locality determines which tensors are distributed, how they are distributed, and which parallel data movement primitives are necessary. Point-wise layers, such as activation functions that operate on individual degrees-of-freedom, are embarrassingly parallel. Native implementations of these functions can be used in distributed neural networks without further intervention and we omit them from the ensuing discussion. While we give the algorithm for the adjoint pass of the composit ed distributed layer, we only have to provide the deep learning framework with the forward algorithm: all necessary adjoint data movement operations are already provided to the AD tool. In the subsequent development, all rank-\(d\) tensors are partitioned along each dimension by a \(d\)-length partition vector, which describes the number of workers in each dimension.

\[\text{This is also true for standard simulations, but the data sizes are generally fixed over a single time-step, so we do not usually think this way.}\]
Sparse layers  Sparse layers are characterized by the use of a small, sliding kernel function over the input tensor to map to output tensors. Such functions include those with learnable network parameters, like the weights and biases in convolutional layers, and those without, such as pooling layers.

Among this class of layers, pooling layers are the most straightforward to parallelize. Assume the input and output tensor $x$ and $y$ have feature-space dimension $D$ and over-all shape $n_b \times n_c \times m_0 \times \cdots \times m_{D-1}$ and $n_b \times n_c \times n_0 \times \cdots \times n_{D-1}$, where $n_b$, $n_c$, $m_1$, and $n_i$ are the batch, channel, and feature-space dimensions, respectively. For both tensors, distributed over a partition $P$ with shape $1 \times P_1 \times P_0 \times \cdots \times P_{D-1}$, the distributed pooling algorithm and the adjoint of its Jacobian are:

Forward Pooling Algorithm
1: Input: $x$
2: $\hat{x} \leftarrow Hx$
3: $\hat{y} \leftarrow Pool(\hat{x})$
4: Output: $\hat{y}$

Adjoint Pooling Algorithm
1: Input: $\delta y$
2: $\delta x \leftarrow [\delta Pool]^*(\delta y)$
3: $\delta x \leftarrow H^*\delta x$
4: Output: $\delta x$

The algorithm does not rely on linearity in the pooling operation, so any pooling operation is permitted, including average and max pooling. The halo exchange $H$ is strongly dependent on the pooling kernel size, stride, dilation, and padding parameters. In practice, padding and unpadding shims are required to address cases where halos are needed or extra input is provided (e.g., those in Appendix B).

Convolutions are a frequent target for parallelization \[9\] and were targeted by \[11\] to improve strong parallel scalability. Ultimately, we seek weak scalability as we are interested in problems where the input tensors can have billions of degrees-of-freedom. Anticipating that these tensors will be decomposed over potentially hundreds of workers, we avoid the explicit all-reduce operation often described. Instead, we formulate the layer so that the all-reduce appears implicitly: a broadcast in the forward implementation naturally induces a sum-reduce in the adjoint phase.

Assume a similar structure as for the pooling layer, except that the learnable weights $w$ have shape $n_{co} \times n_{ci} \times k_0 \times \cdots \times k_{D-1}$, where $n_{ci}$ and $n_{co}$ are the input and output channel sizes and $k_i$ is the kernel size, and are distributed over partition $P_r$ with shape $P_{co} \times P_{ci}$. To avoid multiple counting of the bias, assume that the learnable part of the bias is only present on one $P_{co} \times 1$ subpartition of $P_r$.

For $P_r$ and $P_y$ with shapes $1 \times 1 \times P_{ci} \times P_0 \times \cdots \times P_{D-1}$ and $1 \times P_{co} \times 1 \times P_0 \times \cdots \times P_{D-1}$, a work partition $P_w$ with shape $1 \times P_{co} \times P_{ci} \times P_0 \times \cdots \times P_{D-1}$ and using broadcast and reduce operations that are similar to the NumPy broadcasting rules \[20\] along partitions, the generalized distributed convolution layer and the adjoint of its Jacobian are:

Forward Convolution Algorithm
1: Input: $x$
2: $\tilde{x} \leftarrow Hx$
3: $\tilde{w} \leftarrow B_{P_r \rightarrow P_y} w$
4: $\tilde{b} \leftarrow B_{P_r \rightarrow P_y} b$
5: $\hat{x} \leftarrow B_{P_r \rightarrow P_y} x$
6: $\hat{y} \leftarrow Conv(\tilde{w}, \tilde{b}, \hat{x})$
7: $y \leftarrow R_{P_y \rightarrow P_r} \hat{y}$
8: Output: $y$

Adjoint Convolution Algorithm
1: Input: $\delta y$
2: $\delta \hat{y} \leftarrow B_{P_y \rightarrow P_r} \delta y$
3: $\delta \tilde{w}, \delta \tilde{b}, \delta \hat{x} \leftarrow [\delta Conv]^*(\delta \hat{y})$
4: $\delta x \leftarrow R_{P_y \rightarrow P_r} \delta \hat{x}$
5: $\delta b \leftarrow R_{P_y \rightarrow P_r} \delta \tilde{b}$
6: $\delta w \leftarrow R_{P_y \rightarrow P_r} \delta \tilde{w}$
7: $\delta x \leftarrow H^*\delta x$
8: Output: $\delta x$

If the tensors are distributed over the feature-space exclusively, or over channels exclusively, the algorithm can be significantly simplified by removing multiple broadcasts or reductions. Distributed up-sampling and down-sampling layers are constructed similarly.

Dense layers  Dense layers are characterized by full-connection between input and output degrees-of-freedom, often through the affine function $y = Wx + b$, where $W$ is a dense $n_{fo} \times n_{fi}$ matrix and $n_{fo}$ and $n_{fi}$ are the number of output and input features. Optimal parallelism in such layers is found through a distributed generalized matrix-matrix multiplication, or GEMM, algorithm \[21\]. Optimal GEMM structure and performance is dependent on the computing environment, the size and rank of the tensors, and is an area of open research. We present an implementation based on the primitives above, recognizing that depending on the partitioning of workers, most production distributed GEMM implementations will have similar flavor. A distributed affine layer has similar

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6 The additional dimensions aid the broadcasting pattern but do not impact the result.

7 The main difference is our broadcast is source-to-destination only, while NumPy broadcast is bi-directional.
setup as the distributed convolution, except that the weight tensor is $n_{fo} \times n_{fi}$, where $n_{fo}$ and $n_{fi}$ are the number of features in and out, and is distributed on $P_w$, a $P_{fo} \times P_{fi}$ partition. The learnable bias, of size $n_{fo}$, is present only on one $P_{fo} \times 1$ subset of $P_w$, to avoid any issue with multiple-counting of the bias. For simplicity, we assume that the layer is fully-connected and that input and output tensors $x$ and $y$ have size $n_b \times n_{fi}$ and $n_b \times n_{fo}$, and are distributed on partitions $P_x$ and $P_y$, with shape $1 \times P_{fi}$ and $1 \times P_{fo}$, respectively. The extension to arbitrary tensor dimensions is similar to the distributed convolution layer. The algorithm and the adjoint of its Jacobian are:

**Forward Affine Algorithm**

1. Input: $x$
2. $\hat{x} \leftarrow B(P_x) \rightarrow \{P_w\} x$
3. $\hat{y} \leftarrow \text{Affine}(\hat{w}, \hat{b}; \hat{x})$
4. $y \leftarrow R(P_w) \rightarrow \{P_y\} \hat{y}$
5. Output: $y$

**Adjoint Affine Algorithm**

1. Input: $\delta y$
2. $\delta \hat{y} \leftarrow B(P_y) \rightarrow \{P_w\} \delta y$
3. $\delta \hat{w}, \delta \hat{b}, \delta \hat{x} \leftarrow [\delta \text{Affine}]^*(\delta \hat{y})$
4. $\delta \hat{x} \leftarrow R(P_w) \rightarrow \{P_x\} \delta \hat{x}$
5. Output: $\delta x$

5 Example

![Image](image.png)

Figure 1: Global structure of a distributed Lenet-5 network in DistDL.

We have implemented a number of the above layers in DistDL, as a demonstration of the effectiveness of our model. These implementations explicitly rely on PyTorch’s underlying implementation of the base layer function. Using our distributed convolution, pooling, and affine layers, as well as some transpose layers as glue, we have implemented a distributed implementation of the Lenet-5 convolutional neural network [22]. We emphasize that this is not intended as a performance implementation, rather our aim was to validate the mathematical framework that we have developed. The DNN itself is parallelized over a small number of workers (4), due to Lenet-5 and MNIST’s tiny size, the underlying components satisfy adjoint tests for much larger tensors and partitions.

Figure 1 shows a high-level diagram of the distributed network and worker-specific details are given in Appendix C along with detailed experimental parameters. Over 50 trials, training over the standard MNIST training data set with random initial network parameters, 10 epochs, and $n_b = 256$, the sequential and distributed networks produce equivalent results: an average of 98.54% and 98.55% correct predictions on the standard test data set.

6 Outlook & Future Developments

We have presented a linear-algebraic framework for data movement for distributed deep learning. Using this framework, we have demonstrated that common neural network functions can be implemented in a distributed environment using the developed parallel primitives. As a proof of concept, we have restricted our concrete implementation to a CPU implementation using MPI. Concrete, performance driven realizations of these algorithms will be highly dependent on the target super computing architecture and the DNN structure. For example, we anticipate that this framework will be particularly useful when applied to the large volumetric data sets and the physics-informed neural networks [23, 24] currently being investigated for PDE constrained optimization, such as seismic inversion. In any scenario, to achieve production-level performance on current extreme-scale, hybrid CPU-GPU supercomputers, and to leverage the increasing power of GPUs on smaller machines, a proper concrete implementation will need to be adapted to use Remote Direct Memory Access [25] (RDMA) or alternative interfaces to GPU-to-GPU communication technologies, such as the GPU support in recent MPI implementations [26]. This is an area of ongoing development.
### Broader Impact

We anticipate that these developments will have no ethical or societal consequences distinct from any other development in high-performance computing (HPC) technology. However, these developments provide a future path to democratize HPC technology with deep learning, the same way that the broad availability of PyTorch, Tensorflow, and cloud computing technologies have democratized ML. Any positive or negative outcome arises strictly from the application selection of the user. Only those with access to parallel computers will have immediate advantage from this work, though the model can be applied to local shared-memory computers, too. If a parallel training job fails, lost time and money are the negative consequences. There are no underlying biases present in this approach.

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Appendix A Derivations

A.1 Derivation of the adjoint of allocation

Assume the allocation $A : \mathbb{F}^m \to \mathbb{F}^n$, $x = [x_a] \in \mathbb{F}^m$, and $y = [y_a] \in \mathbb{F}^n$. Then, under the standard inner product, the adjoint of $A_b$ is,

$$\langle A_b x, y \rangle_{\mathbb{F}^m} = \sum_{i=0}^{n-1} (A_b x)_i y_i = \sum_{i=0}^{m-1} (I_a x_a)_i y_i = \sum_{i=0}^{m-1} x_i y_i$$

Then, the adjoint is,

$$M = \sum_{i=0}^{m-1} x_i (I_a y_a)_i = \sum_{i=0}^{m-1} x_i (I_a y_a + O_b^T y_b)_i = \langle x, A_b^T y \rangle_{\mathbb{F}^m} = \langle x, A_b^* y \rangle_{\mathbb{F}^m}.$$ 

Derivations of the adjoints of $K_b$ and $S_{a \to b}$ follow similarly for the standard inner product.

A.2 Construction of copy

The in-place copy operator, $C_{a \to b} : \mathbb{F}^m \to \mathbb{F}^m$, takes input $x = [x_a] \in \mathbb{F}^m$ and produces output

$$x = [x_a] \in \mathbb{F}^m.$$ 

Then, the adjoint is,

$$C_{a \to b}^* = (S_{a \to b} K_b)^* = K_b^* S_{a \to b}^* = K_b S_{b \to a}.$$ 

The out-of-place copy operator, $C_{a \to b} : \mathbb{F}^m \to \mathbb{F}^n$, takes input $x = [x_a] \in \mathbb{F}^m$ and produces output

$$\hat{x} = [x_a] \in \mathbb{F}^n.$$ 

Then, the adjoint is,

$$C_{a \to b}^* = (S_{a \to b} A_b)^* = A_b^* S_{a \to b}^* = D_b S_{b \to a}.$$ 

A.3 Construction of move

The in-place move operator, $M_{a \to b} : \mathbb{F}^m \to \mathbb{F}^m$, takes input $x = [x_a] \in \mathbb{F}^m$ and produces output

$$x = [0_a] \in \mathbb{F}^m.$$ 

Then, the adjoint is,

$$M_{a \to b}^* = (K_a S_{a \to b} K_b)^* = K_b^* S_{a \to b}^* K_a^* = K_b S_{b \to a} K_a.$$ 

The out-of-place move operator, $M_{a \to b} : \mathbb{F}^m \to \mathbb{F}^m'$, takes input $x = [x_a] \in \mathbb{F}^m$ and produces output

$$\hat{x} = [x_a] \in \mathbb{F}^m', \text{ and } \mathbb{F}^m' \text{ is a different memory subset of the same size. Thus,}$$

Then, the adjoint is,

$$M_{a \to b}^* = (D_a S_{a \to b} A_b)^* = A_b^* S_{a \to b}^* D_a^* = D_b S_{b \to a} A_a.$$ 

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Appendix B  Halo exchange

B.1 Irregularly structured halo regions

The subsequent examples show the impact of different kernel parameters and tensor partitions on the halo regions for some different kernels and input sizes. In each case, the driver for the computational load balance is the output distribution. Consequently, absent any padding, assuming the input comes from another layer with the same property, the input is also balanced. While we show 1-D examples for simplicity of presentation, the same patterns emerge in multidimensional cases, with more complex interactions between the halo regions.

In the following figures, bulk regions are illustrated in solid black lines and halo regions are given in dashed lines. The numbers, arrows, and braces illustrate the access pattern. Directional arrows indicate the input influence on output, numbers in the input tensor are indices, and numbers in the output tensor are the input index at the root of the kernel for that output index. We have selected these examples for their representative behavior and the kernel parameters are commonly used in many DNNs.

“Normal” convolution  Assume a centered convolution kernel with size $k = 5$, input tensor size $n = 11$, partition size $P = 3$, and assume a zero-padding of width 2 is implicitly added to the input boundaries. In Figure B2 we illustrate that this situation yields the “normal”, uniform halo sizes.

Unbalanced convolution  Assume a centered convolution kernel with size $k = 5$, input tensor size $n = 11$, partition size $P = 3$, and assume a no padding is added to the input boundaries. Then the output length is $m = 7$. In Figure B3 we illustrate that this situation yields unbalanced halo sizes, where the first and last workers have large, one-sided halos and the middle worker has small, balanced halos.

Simple unbalanced pooling  Assume a right-looking pooling kernel with size $k = 2$, stride $s = 2$, input tensor size $n = 11$, partition size $P = 3$, and no padding or dilation. In Figure B4 we illustrate that this situation yields both unbalanced halos and unnecessary data in the input tensor. For the first worker, there is no halo. For the second worker, only the right-side has a halo, with size 1. The last worker does not have any halo, but to produce the same output as the sequential case for this input, the first entry of the input tensor actually has to be removed when the input is provided to the local pooling operator.

Complex unbalanced pooling  Assume a right-looking pooling kernel with size $k = 2$, stride $s = 2$, input tensor size $n = 20$, partition size $P = 6$, and no padding or dilation. In Figure B5 we illustrate that this situation yields many ranks with unbalanced halos and unnecessary data in the input tensor. For the first and second workers, there are no halos. The third worker has a right halo but no left halo. The 4th worker has 1 extra input on the left and a halo of length 2 on the right. The
5th worker has 2 extra input on the left and a halo of length 1 on the right. The final worker has no halos, but one extra input on the left. In cases with extra input data, those entries of the input tensor actually has to be removed when the input is provided to the local pooling operator.

Figure B4: Halo sizes induced by a $k = 2$ right-looking kernel, with stride 2.

Figure B5: Halo sizes induced by a $k = 2$ right-looking kernel, with stride 2.

B.2 Generalized tensor halo exchange

Here we illustrate the generalized, unbalanced halo exchange on a rank-2 tensor, partitioned by a $P = 2 \times 2$ partition. While the algorithm works for tensors of arbitrary rank with arbitrary partitions, a rank-2 tensor is sufficient to illustrate the concept. In Figure B6, we have partitioned the tensor into 4 unequal, but load-balanced domains. The colors will be maintained throughout subsequent figures to help illustrate data ownership. The differences in size are exaggerated for clarity. As seen in Figure B7a, where gray regions are the halo region, workers 0 and 2 require no data from workers 1 and 3, but share width 3 data with them, workers 0 and 1 require width 2 data from workers 2 and 3, workers 2 and 3 require width 4 data from workers 0 and 1, and there are interior halos only. We have chosen the vertical dimension to perform the first exchange.

Figure B6: Data before forward halo exchange for $P = 2 \times 2$ partition of a rank-2 tensor.

Figure B7 illustrates the sequence of copy operations in the forward halo exchange algorithm. After two steps (Figures B7b and B7c, the final exchanged result is in Figure B7d. The exchange pattern is nested to minimize communication volume, as for larger, higher-rank tensors these volumes grow quickly. The gray arrows in the second exchange phase indicate that no data needs to be shared. We have omitted the action on the send and receive buffers, for clarity.

Figure ?? illustrates the sequence of add-clear operations in the adjoint halo exchange algorithm. Figure B8a shows the starting state, where each rank has input data starting in its halo regions. After two steps (Figures ?? and ??, the final exchanged result is in Figure ??a. The checkerboard patterns indicate summation. The gray arrows in the adjoint of the second exchange phase indicate that no data needs to be shared. We have omitted the action on the send and receive buffers, for clarity.
Appendix C  Distributed Lenet-5

C.1 Global network architecture

In Figure C10, we show the full structure of the distributed Lenet-5 network, including all necessary shims and sub-layers. The parallel distribution of learnable parameters is provided in Table 1. The transpose layers are used to create better load balance on the inputs and outputs and their selection is system and implementation dependent. We also make use of transpose layers to distribute input data and collect outputs (not shown).

C.2 Experimental parameters

The experimental parameters for comparing sequential and distributed versions of Lenet-5 are reported here. The training data consists of the standard 60,000 MNIST training data set, broken into batches of size 256. Because the distributed network requires a fixed batch size, the final 96 images are dropped from the data set, for both networks. The test data consists of the standard 10,000 MNIST test data set, broken into batches of size 256. Because the distributed network requires a fixed batch size, the final 96 images are dropped from the data set, for both networks. The sequential network is implemented in PyTorch using PyTorch’s native neural network modules. The distributed network is implemented using DistDL’s distributed neural network models, as shown in Figure C10. Each network was trained 50 times, with random initial weights, over 10 epochs. The Adam optimizer, with learning rate $\alpha = 0.001$, was applied to the cross-entropy loss function. This experiment was
(a) Setup of adjoint halo exchange.

(b) Adjoint of second phase halo exchange.

(c) Adjoint of first phase halo exchange.

(d) Result of adjoint halo exchange.

Figure B8: Adjoint unbalanced halo exchange for \( P = 2 \times 2 \) partition of a rank-2 tensor.

Figure B9: Data after adjoint halo exchange for \( P = 2 \times 2 \) partition of a rank-2 tensor.

run on an Intel Xeon E3-1505M with 32 GB of RAM. Source implementation has been tested and verified on Virginia Tech’s Cascades cluster.
| Layer | Function | Worker 0          | Worker 1 | Worker 2 | Worker 3 |
|-------|----------|-------------------|----------|----------|----------|
| C1    | Conv     | $w : (6, 1, 5, 5)$| None     | None     | None     |
|       |          | $b : (6)$         |          |          |          |
| S2    | Pool     | None              | None     | None     | None     |
| C3    | Conv     | $w : (16, 6, 5, 5)$| None     | None     | None     |
|       |          | $b : (16)$        |          |          |          |
| S4    | Pool     | None              | None     | None     | None     |
| C5    | Affine   | $w : (60, 200)$   | $w : (60, 200)$ | $w : (60, 200)$ | $w : (60, 200)$ |
|       |          | $b : (60)$        |          |          |          |
| F6    | Affine   | $w : (42, 60)$    | $w : (42, 60)$ | $w : (42, 60)$ | $w : (42, 60)$ |
|       |          | $b : (42)$        |          |          |          |
| Output| Affine   | $w : (5, 42)$     | $w : (5, 42)$ | $w : (5, 42)$ | $w : (5, 42)$ |
|       |          | $b : (5)$         |          |          |          |

Table 1: Learnable parameters per worker, per layer.
Figure C10: Global view of the distributed Lenet-5. Sequential layers and those from the underlying deep learning framework are purple, distributed layers and primitives are brown, green, and pink.