A Programmable Frequency Divider With a Full Modulus Range and 50% Output Duty Cycle

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ABSTRACT Programmable frequency dividers with wide modulus range and 50% output duty cycle are highly desirable in the design of frequency synthesizers and phase-locked loops. However, most of the conventional dividers cannot simultaneously achieve a 50% output duty cycle and full modulus range. A programmable frequency divider with a full modulus range, 50% output duty cycle and low phase noise is presented in this paper. To achieve a 50% output duty cycle, the divider employs a novel programmable down-counter based on a modified D flip-flop with a load function. The divider, which was fabricated in a standard 0.18-µm CMOS process, achieves a full 1 to 256 modulus range, 50% output duty cycle, and can operate up to 2.3 GHz with a 1.8-V supply voltage and a power consumption of 3.4 mW. The measured phase noise is −141 dBc/Hz at the frequency offset of 1 MHz when the divider is working at a 1-GHz operational frequency and a division ratio of 10.

INDEX TERMS Duty cycle, full modulus range, programmable frequency divider, phase noise.

I. INTRODUCTION

Advanced system-on-chips (SoCs) typically consist of a wide variety of modules operating in different dedicated clock domains. For example, multicore processors dynamically adjust the clock frequency for each core to optimize operational speed, power and heat management [1], [2]. Fractional-N phase-locked loops (PLLs) and frequency synthesizers are commonly used as clock generators to meet diverse requirements. The programmable frequency divider is one of the major blocks in frequency synthesizers and PLLs [3]–[5]. The desired features of a programmable frequency divider include high speed, low power, low phase noise, wide modulus range, 50% output duty cycle and high drive capability. A wide modulus range enables a PLL to generate clock signals covering a wider frequency range and improves reusability to shorten time-to-market schedules. The output duty cycle is critical for high-speed programmable frequency dividers. The drive capability of a frequency divider is affected by the output duty cycle. The preferred output duty cycle is 50% to obtain the longest pulse width, which increases the driving capability with the same current. Moreover, with a 50% duty cycle, circuits have equal time to settle when the clock signal is high or low, which is critical for high-speed variable-clock systems. However, it is very challenging to achieve a 50% output duty cycle for odd division.

A programmable counter is commonly used as a simple programmable frequency divider. To extend the modulus range, a programmable divider based on a dual-modulus prescaler and two programmable counters was presented in [6]. The dual-counter architecture not only increases the hardware overhead and power consumption but also represents a substantial load at the output of the prescaler, leading to speed degradation. Counter-based dividers have been extensively studied in the literature [7]–[9]. In [7], a parallel counter based on a state look-ahead structure is employed to minimize the speed degradation introduced by the increase of the divider bit size. To reduce the number of counters in a programmable frequency divider, a divider based on a shared counter is reported in [8]. However, it cannot achieve a full modulus range. Another widely used divider architecture...
is a 2/3 divider based on a chain of $n$ cells, where each cell provides both divide-by-2 and divide-by-3 functions. The integer division ratios range from $2^n$ to $2^{n+1} - 1$ [10]. This technique extends the division ratio range greatly. Several 2/3 dividers have been reported [5], [11], [12]. However, they cannot achieve division ratios that are lower than $2^n$, and they have a relatively low output duty cycle for odd division. In [13], a programmable frequency divider with a nearly 50% output duty cycle is presented. A division ratio-identifying circuit is proposed to correct the duty cycle. However, the output duty cycle decreases as the frequency division ratio decreases.

Note that state-of-the-art programmable frequency dividers cannot achieve a full modulus range and 50% output duty cycle simultaneously. To address this issue, a new programmable frequency divider based on a 0.18-µm CMOS process is presented in this paper. The proposed divider achieves a full modulus range from 1 to 256 and a 50% output duty cycle for all division ratios. The proposed divider employs a novel programmable down-counter based on modified D flip-flops, thus requiring only one counter. In contrast, conventional programmable counter-based dividers utilize two counters, which introduce more power consumption and speed degradation. The simulations and test results verify that the proposed programmable frequency divider achieves low phase noise, a 50% output duty cycle and a full modulus range from 1 to 256 without significantly increasing power consumption.

The rest of this paper is organized as follows: The architectures of conventional programmable frequency dividers are reviewed in Section II. The proposed programmable frequency divider is described in Section III. The measurement results are presented in Section IV. Finally, conclusions are drawn in Section V.

II. PREVIOUS WORK

Programmable counter-based and 2/3-divider-based programmable frequency dividers account for the majority of previous programmable frequency divider structures [8], [14], [15]. This section discusses these two classic programmable frequency divider structures and some state-of-the-art techniques to further improve the speed, phase noise and modulus range.

A. PROGRAMMABLE COUNTER-BASED DIVIDER

The structure and the operation principle of the programmable counter-based divider are shown in Fig. 1 (a). It consists of a dual-modulus prescaler (DMP), a programmable swallow counter (SC) and a programmable counter (PC). The division ratio of the dual-modulus prescaler is set to be $N_{PR}$ and $N_{PR} + 1$ when the modulus control signal $MC$, which is generated by the programmable swallow counter, is 0 and 1, respectively. Assuming the initial value of $MC$ is 0, the division ratio of the DMP is $N_{PR}$. The SC counts the cycles of the output signal of the DMP up to $S$. The modulus control signal $MC$ is changed from low to high when the value of the SC reaches $S$. On the other hand, the PC counts the cycles of the output signal of the DMP up to $P$, and then both counters, the SC and PC, are reset by the reset signal generated by the PC. Its frequency division ratio $N$ is given by

$$N = S \times (N_{PR} + 1) + N_{PR} \times (P - S) = S + N_{PR} \times P$$ (1)

Note that the division ratio $N$ is determined by three parameters. Therefore, the programmable-swallow-counter-based...
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Dividers have a relatively wide modulus range. However, there are two counters driven directly by the DMP, leading to a larger output load capacitance for the DMP, which degrades the high-speed operation. On the other hand, the two counters continue working, resulting in higher power consumption. A programmable divider based on a single programmable counter serving as both SC and PC was reported in [8] to save power. The speed of the programmable counter can be improved by incorporating a modified end of count (EOC) generation scheme that relaxes the timing constraint [16].

B. 2/3 Divider

Another commonly used programmable frequency divider structure is 2/3-divider, as shown in Fig. 1(b) [10]. It consists of a chain of 2/3-divider cells. The divider cell is in divide-by-3 mode when both the \( \text{MODI} \) and \( P_i \) are high; otherwise, it operates as a 2-divider. When a division period begins, the last cell on the chain has a high \( \text{MODI} \) and generates the signal \( \text{MOD}_{N-1} \); then, each cell reclocks \( \text{MOD}_{N-1} \) and outputs it to the preceding cell in the chain. The period of the output signal of the conventional 2/3-divider-based programmable frequency divider can be expressed as

\[
T_{out} = \left( 2^n + 2^{n-1}P_n + 2^{n-2}P_{n-1} + \cdots + 2P_2 + P_1 \right) \times T_{in}
\]

where \( n \) is the number of cascaded 2/3-divider cells, \( T_{in} \) is the period of the input clock signal, and \( P_1, P_2, \ldots, P_n \) are programming values. The division ratio range is from \( 2^n \) to \( 2^{n+1} - 1 \). Therefore, conventional 2/3 divider cannot achieve a full modulus range.

To extend the modulus range, a programmable frequency divider based on a chain of 2/1 dividers was proposed in [12], in which a full modulus range from 1 to 256 was achieved for an eight-stage divider. The conventional 2/3 divider cell was implemented by DFFs and logic gates [10], [17]. The delay and power consumption of the 2/3 divider cell can be further reduced by using low-leakage true single-phase clock (TSPC) flip-flops [18].

C. High-Frequency Divider Based on BiCMOS Technologies

For millimeter-wave (mm-wave) applications, several programmable frequency dividers in SiGe BiCMOS technology have been reported to achieve ultra-high-speed and low-noise operation [19]–[21]. A 17 GHz 2/3-divider-based programmable frequency divider fabricated in 130 nm SiGe BiCMOS technology was presented in [19]. To reduce the phase noise, the prescaler between VCO and the programmable divider is abandoned, and the high-frequency input clock signal is directly handled by the divider. A synchronization flip-flop driven by the input clock is employed at the output to reduce the jitter accumulation of the divider. However, since a prescaler can reduce the input frequency of other blocks, a high-frequency prescaler is critical for increasing the maximum operating frequency. In [20], a high-frequency prescaler was used with a dual-counter to achieve a high operational frequency up to 57 GHz. The phase noise floor of bipolar dividers can be lower than -150 dBc/Hz [21] but at the cost of higher power dissipation and fabrication cost.

Note that none of the aforementioned programmable frequency dividers can simultaneously achieve a 50% output duty cycle and full modulus range. This can be addressed by adding a duty-cycle corrector [22]. However, this method does not work well when the output duty cycle is less than 9%, and it brings additional power consumption and cost.

III. PROPOSED DESIGN

A. Basic Concept

The basic concept of the proposed programmable frequency divider is illustrated in Fig. 2. A programmable down-counter, which cyclically counts \( N \) clock cycles, is utilized to generate three pulse signals, \( \text{Pulse0}, \text{Pulse1} \) and \( \text{Pulse2} \). \( \text{Pulse0} \) is generated when the value of the down-counter is equal to \( N - 1 \). \( \text{Pulse1} \) is generated by delaying the signal \( \text{Pulse0} \) by half of a clock period. The timing of \( \text{Pulse2} \) is determined by the parity of the division ratio. According to the parity of \( N \), the proposed programmable frequency divider has two different processing schemes to generate a divided-by-N/2 signal.
1) If \( N \) is even, the signal \( \text{Pulse2} \) is generated when the value of the down-counter is equal to \((N-2)/2\). The divider performs an OR operation on \( \text{Pulse0} \) and \( \text{Pulse2} \) to generate the divided-by-N/2 signal; then, we can obtain the divided-by-N signal by using a 2-divider.

2) If \( N \) is odd, the signal \( \text{Pulse2} \) is generated when the value of the down-counter is equal to \((N-3)/2\). By performing an OR operation on \( \text{Pulse1} \) and \( \text{Pulse2} \), the divided-by-N/2 signal is generated, and then we can obtain the divided-by-N signal by using a 2-divider.

3) Finally, the generated divided-by-N/2 signal is forwarded to a 2-divider to obtain a divided-by-N signal with a 50% output duty cycle.

Note that whether \( N \) is even or odd, the output duty cycle of the proposed method is 50%. Compared with conventional programmable counter-based dividers, the proposed programmable frequency divider reduces the number of counters, leading to lower power consumption and phase noise. It also achieves a wider modulus range.

**B. ARCHITECTURE**

The architecture of the proposed programmable frequency divider is shown in Fig. 3 (a). It consists of a pulse generator, an output control logic and a programmable down-counter based on a modified DFF. The operating principle is demonstrated in Fig. 3 (b). \( \text{CLK} \) is the input clock signal, \( D[7:0] \) is an 8-bit programming signal, and \( \text{Fout} \) is the output signal.

The value of the down-counter is initially \( D[7:0] \) when the counter counts down to 0. Based on the previously discussed basic concept, the pulse signals \( \text{Pulse0}, \text{Pulse1} \) and \( \text{Pulse2} \) are generated with the down-counter and the pulse generator. The relationship between the division ratio \( N \) and the programming data \( D[7:0] \) is defined as follows:

\[
N = \begin{cases} 
1, & D[7 : 0] = \text{H'}\text{FF} \\
D + 2, & D[7 : 0] = \text{H'}00 \sim \text{H'}\text{FE} 
\end{cases}
\]  

As shown in Fig. 3 (b), the operational principle of the output control logic can be characterized as:

\[
\text{Fout} = \begin{cases} 
\text{CLK}, & D = \text{H'}\text{FF}(N = 1) \\
\text{Pulse0}, & D = \text{H'}00(N = 2) \\
\text{OR(\text{Pulse0}, \text{Pulse1})}, & D = \text{H'}01(N = 3) \\
\text{OR(\text{Pulse0}, \text{Pulse2})}, & D \text{ is even, except H'00 (N is even, except } N = 2) \\
\text{OR(\text{Pulse1}, \text{Pulse2})}, & D \text{ is odd, except H'01 and H'FF (N is odd, except } N = 1 \text{ and } N = 3) 
\end{cases}
\]
When $D[7:0] = \text{H'00}$ ($N = 2$), $Pulse0$ is a divided-by-2 signal; hence, $Fout = Pulse0$. Note that the duty cycle of $Pulse0$ is 50% when $N = 2$.

When $D[7:0] = \text{H'01}$ ($N = 3$), $Pulse0$ is a divided-by-3 signal, but its duty cycle is 33.3%. The OR operation is performed on signals $Pulse0$ and $Pulse1$, and we obtain a divided-by-3 signal with a 50% duty cycle. When $D$ is even (H’00 excluded), a divided-by-N/2 signal is generated by carrying out the OR operation on signals $Pulse0$ and $Pulse2$; then, we can obtain a 50% duty-cycling divided-by-N signal by using a 2-divider.

When $D$ is odd (H’01 and H’FF excluded), the OR operation is performed on signals $Pulse1$ and $Pulse2$, a divided-by-N/2 signal is generated, and then we can obtain a 50% duty-cycling divided-by-N signal by carrying out the divided-by-2 operation.

C. PROGRAMMABLE DOWN-COUNTER BASED ON MODIFIED D FLIP-FLOPS

The 8-bit programmable down-counter in the proposed programmable frequency divider is shown in Fig. 4(a). It can be divided into a loop-counting controller and a down-counter based on modified DFFs. $Q[7:0]$ is the 8-bit output signal of the counter. The modified DFF, as shown in Fig. 4(a), has two data input terminals (D1 and D2), two clock signal input terminals (CLK and $CLK'$), a setting control terminal LD and two output terminals ($Q$ and $\bar{Q}$). The two input data D1 and D2 of the DFF are selected according to the value of LD and forwarded to the output. The terminal D1 is equivalent to the D terminal of the conventional DFF. The terminal D2 is connected to the programming signals to reset the value of the down-counter to $D[7:0]$. Therefore, the proposed down-counter with modified DFFs does not require additional resetting logic circuits.

The waveforms of the programmable down-counter are presented in Fig. 4(b). When $LD$ is low, $Q = D1$. When $LD$ is high, $Q = D2$. When $Q[7:0] = \text{H’00}$, which means a down-counting cycle is finished, a positive pulse is generated by the loop-counting controller and sent to the $LD$ terminals of the 8 DFFs to reset the number of the down-counter to $D$. When $LD$ is low, the down-counter starts to count. Note that the number of clock periods in a counting cycle is $D + 2$.  

![Simulated waveforms of the proposed divider at 2.3 GHz operating frequency and 139 division ratio.](image)
Therefore, the division ratio $N$ is equal to $D + 2$, as shown in (3).

**IV. EXPERIMENTAL RESULTS**

The proposed programmable frequency divider is implemented in a 0.18-µm CMOS process, as shown in Fig. 5, and occupies 37200 µm$^2$. In contrast to previous work, the proposed programmable frequency divider achieves a full modulus range from 1 to 256, low phase noise and 50% output duty cycle.

Fig. 6 presents the simulated waveforms of the proposed divider at 2.3 GHz operating frequency and 139 division ratio. It can be seen that the waveforms are consistent with the concept demonstrated in Fig. 2(b). The output duty cycle is 50.2%. Fig. 7 shows the simulated output duty cycle of the proposed divider working at a 2 GHz operation frequency and a frequency division ratio of 139. The output duty cycle varies from 49.7% to 50.7% at five different process corners and different supply voltages ranging from 1.6~2 V.

Fig. 8 shows the measured input and output phase noise of the proposed programmable frequency divider. The measured phase noise of the proposed programmable frequency divider is -122 and -140 dBC/Hz at frequency offsets of 1 kHz and 1 MHz, respectively, where the programmable frequency divider operates at a 1.8-V supply voltage, a 1-GHz operation frequency and a frequency division ratio of 10. At an offset of 100 kHz, the difference between the input and output phase noise is 18.6 dB, which is close to the ideal value of 20dB. At higher offset frequencies, the difference between input and output phase noise decreases because divider noise contributes significantly to the output noise. The phase noise of this circuit is much lower than that of the divider in [11] and is comparable to that of the programmable frequency divider in [4]. Compared with conventional programmable counter-based dividers, the proposed programmable frequency divider reduces the number of counters, hence reduces the phase noise.

Fig. 9 presents the measured operational frequency, power consumption and power efficiency of the proposed programmable frequency divider at various supply voltages varying from 0.6 V to 2 V. The proposed programmable frequency divider can operate at 2.3 GHz with a 1.8-V supply voltage. The power consumption and power efficiency are 3.4 mW and 0.68 GHz/mW, respectively.

Table 1 presents the comparison of the performance between the proposed and other programmable frequency dividers. The proposed divider achieves the best performance in terms of the output duty cycle and modulus range. Note that the proposed divider is the only one that achieves a 50% output duty cycle in the full modulus range, and it also achieves low phase noise. The operating frequency of the proposed divider.
divider is comparable to that of the divider in [3] and [5], but lower than other counterparts. This is mainly because the 0.18-μm CMOS process has a disadvantage in speed compared with the deep submicron processes. The proposed divider occupies a larger die area compared with [11] and [12] due to the increased hardware overhead introduced by the complex workflow shown in Fig. 3(b).

V. CONCLUSION
This paper presents a new programmable frequency divider based on a novel programmable down-counter. In contrast to the conventional programmable counter-based programmable frequency dividers that utilize two counters, the proposed divider utilizes a single down-counter to implement Integer-N frequency division with a full modulus range. The proposed circuit was designed and fabricated in a 0.18-μm process. The measurement results show that the proposed divider achieves a full 1 to 256 modulus range, −141 dBC/Hz phase noise at the frequency offset of 1 MHz and a 50% output duty cycle with a 1.8-V supply voltage.

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