Design of Low Power and Failure Free SRAM Cell Using Read Assist Circuits

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Abstract. Static Random Access Memory (SRAM) is one of the main peripherals in all the Very-large-scale Integrated (VLSI) chips, which enact a vital part in all executable applications. The write ability and read stability are prime factors with low power supply and improve operation speed with temperature, process, and voltage variations. In VLSI design, the System on Chip (SoC) performance is improved by applying low power supply and change in few Pico seconds of cycle times or memory access. The read/write operation is not accurate in lower supply voltage because it will not flip to the desired voltage levels. For improving performance, proposed an SRAM cell to flip to the desired voltage levels to reduce readability failures in low supply voltages. The additional requirement is needed to increase the chip’s performance with lower supply voltages, and continuously additional circuit techniques are needed for obtaining the SRAM memory’s readability and writing ability. In this paper, different performance improvement methods of SRAM memory cells are analyzed. The reduced word line voltage read assist circuit is designed for the SRAM memory cell.

Keywords: SRAM, VLSI, CMOS, memory, system on a chip, Read Assist and Write Assist

1. Introduction

Very-large-scale integration (VLSI) is made possible with a combination of thousands of transistors inbuilt into a single chip. The advanced semiconductor techniques are adopted by Metal oxide semiconductor (MOS) integrated circuits. The memory chips are one of the best examples of VLSI. In earlier days, without memory, devices did not show effective throughput by integrated chips [1]. The technology is developed by adding various features ICs are inbuilt into one chip. In earlier days, the integrated circuits contain only a few transistors, the number of transistors are dynamically increased, and logic gates are fabricated in the present days. Moore's law suggested that the enriched parameter features like speed reduced voltage and decreasing the size [2]. The static memories are shown a vital role in the performance of any integrated chip [3]. The static random access memory (SRAM) one of the best memory; it is widely used in electronic systems for high speed and low power compared to other memory devices [4]. In real-time applications,
SRAM stability is one of the main challenges in semiconductor memory, and it is affected by write margin. The robustness and cell stability were measured with a Static noise margin (SNM)[5]. The SRAM bit cell stability is also based on the mode of SRAM operation. There is a limitation in stability due to the SRAM cell's minimum power supply (V_{min})[5].

2. Literature Survey

In the designing of SRAM cells, different methods are used for the efficient operation of circuits. In this section, the review of various methods used in designing SRAM cells is discussed briefly [6].

Yajuanet al. proposed an 11T SRAM cell where error correction coding is used to improve the soft error immunity. The write margin (WM) and read static noise margin (RSNM) also improved using read/write assist techniques. RSNM of 19.8x for 6T SRAM and 0.96x for 8-Transistor SRAM is achieved in 40nm CMOS technology. The leakage power also reduced in 6T SRAM by 53.3%, and 8T SRAM is 44.5% [6]. Pal et al. proposed the HFWA9T shows 2.87 times greater stability in reading operation compared to 7T SRAM cell and exhibits 3.37 times greater read stability than single-ended disturb free (SEDF9T) SRAM [7]. Selvakumar et al. proposed a solution for better functionality of sense amplifier for SRAM cell. It is achieved an output voltage of 1.2V, which is available with an addition of an inverter at its output side and also has a similar PMOS and NMOS circuit. The cell size is reduced by 40%, and access time is reduced by 400%. These results are achieved by implementing a circuit using Microwind 3.1 with 45nm&32 nm technologies [8].

Lin et al., proposed Resistive Random Access Memory (RRAM) based averaged 7T1R Static non-volatile RAM (NV-SRAM). The proposed method provides a 154% increase in reading Static noise margin compared to 6T nSRAM, and also, the speed of reading operation is improved by 23%. The static write margin is increased by 88.6% for writing “1” with respect to 6T SRAM at 1.2 V supply. Because of using single-bit line subword line driver technology, the dynamic power is effectively reduced [9]. Surana et al. proposed a single-ended 6T (SE6T) SRAM, which reduced around 50% dynamic power with respect to standard 6Transistor SRAM with similar BitErrorRate (BER) [10]. In this paper, the read-write port with two pass transistor 6Transistor SRAM gates are eliminated in 7T-SRAM and read port with two transistors like 8Transistor Static RAM and a cell node pair equalizers are also installed. The current conflict problem is solved by eliminating the current drive-through pass gates in the reading and write operations of SRAM [11].

Ahmad et al., In this paper, with the help of write 0/1 and power cut off techniques in 11T-1 and 11T-2 cells are eliminated [12]. In [13] defined failure modes of SRAM operation at low supply voltages. Demonstrated the read stability improvement of SRAM cell with the help of the Read Assist method. Explained stability of SRAM for various methods for process changes like scaling of V_{dd} and Vt [14]. Reddy et al., in this paper, analyzed various write and read assist methods, and the benefits of these methods are also demonstrated; the impact on stability and read/write abilities of SRAM is also explained [15].

Farkhani et al., in this paper, the write operation is improved by proposing a new write assist method where the access transistors are strengthened at both sides (i.e., bitLine and bitLineBar) of SRAM. Anil et al., in this paper, proposed a modified latched type sense amplifier, and based on sensing delay and offset voltage, the comparison of yield is given for 28nm technology [16]. Taehui et al., discussed various sense amplifier circuits in 65nm technology. He analyzed the most popular latch-type sense Amplifiers: voltage- and current-latched sense amplifiers. Furthermore, a suitable latch-type sense amplifier scheme is suggested [17].

3. Conventional 6T SRAM Cell

SRAM is one of the best volatile memories; it can retain stored information as long as power is supplied.
The random access memory means that a group of cells will perform read or write randomly; there is no specific order for accessed. The periodic refreshes are necessary for dynamic RAM (DRAM) or no power needed for data retention for non-volatile memory.

Figure 1: Circuit of standard 6Transistor Static RAM

Figure 1 represents a standard 6Transistor Static RAM, which contains two access MOSFETs and 2 inverters. The circuits were designed by two inter-connected inverters (M1 and M4) with two pass transistors (M5 and M6). The pass transistors are connected by complementary bit lines (BLB/BL). A word line joins the pass transistors. These word lines and bit lines are helpful to perform read-write operations. This conventional cell work with three modes with its margin like HOLD, write and read. Generally, the word line is followed by lower voltage, i.e., GND in standby mode, and back-to-back inverter transistors are connected to maintain data properly in stable operation. In write operation mode, the bit lines are connected to the driver ckt's negative voltage levels in write mode. The write information is stored in the internal storage when the WL bit is enabled. The read operation is done by a word line connected to Vdd and precharged to Vdd. Due to this, the bit line discharged through M6 and M3 transistors with the differential voltage developed across lines, the cell state of the sense amplifier can be detected.

3.1. Failure Modes of SRAM Cell
In Static RAM, there are three failure modes: readable, with the ability, and read stability. In a read operation, whenever the read bit line discharged in a particular time is lower than the sense amplifier offset, and then readability failure will occur, as shown in Figure 4 and read stability pass in Figure 5. In a write operation, whenever, internal cell node voltage not reached the required voltage level, then write ability failure occurred as shown in Figure 2 and write operation success in Figure 3. Whenever the bit cell content suddenly flipped, then read stability failures occurred in a read operation of the memory.

Figure 2: Failure in write operation  
Figure 3: Write operation success
4. SRAM Cell With reading Assist Circuit

The failures of the SRAM memory cell can be overcome by using additional circuits like reading/write assist circuits. One read assist circuit used in SRAM to overcome readability failures is the "Reduced word line voltage read assist circuit," shown in Figure 6.

![Figure 6: Reduced word line voltage Read assist circuit.](image)

To maintain the circuit's stability, initially, the voltage of the word line is reduced to Vt using a CMOS device. The circuit makes use of a connection of semiconductor diode. In a read operation, the world line voltage is reduced by the NMOS threshold. The Vd is without any degraded when the PMOS is ON (P1); this is due to the PMOS transistor that dispenses strong Vd. In a read operation, making 'ren' high and the NMOS transistors (N1, N2, and N3) are active and N3 transistors connected to Vd, which does not deliver the high Vd, it provides lesser than Vd (VdVtn). The same procedure is repeated to all the transistors. The number of transistors is increased for more voltage reduction. The read assists circuit is kept in a word line-driven area in the SRAM cell, as shown in Figure 7.

![Figure 7: The SRAM cell with a reduced word line voltage read assist circuit.](image)
The 6T SRAM memory cell using reduced word line voltage read assist technique is designed in 180nm CMOS technology, as shown in Figure 7. This circuit will reduce the readability failures and improves the static noise margin (SNM). Because of using this technique, the write ability issue will arise due to reading the word line voltage, which can be overcome with the help of a write assist circuit for a selected write operation. The proposed read assists circuit will reduce around 5% of the power consumption and improves around 15% of the reading margin.

5. Conclusion
In this paper, various designing techniques for SRAM cells are analyzed, and an SRAM memory cell with a reduced word line Read assist circuit is designed. The failure metrics like read and write failures are identified at low voltage supply. The operation of SRAM at lower voltage levels leads to read/write failures. The readability and write-ability of the SRAM memory cell were improved with read/write assist methods. The write margin and read static noise margin also increased using read/write assist techniques. The performance of the SRAM cell is improved by using the reduced word line read assist circuit.

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