Designing Efficient and High-performance AI Accelerators with Customized STT-MRAM

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Abstract—In this paper, we demonstrate the design of efficient and high-performance AI/Deep Learning accelerators with customized STT-MRAM and a reconfigurable core. Based on model-driven detailed design space exploration, we present the design methodology of an innovative scratchpad-assisted on-chip STT-MRAM based buffer system for high-performance accelerators. Using analytically derived expression of memory occupancy time of AI model weights and activation maps, the volatility of STT-MRAM is adjusted with process and temperature variation aware scaling of thermal stability factor to optimize the retention time, energy, read/write latency, and area of STT-MRAM. From the analysis of modern AI workloads and accelerator implementation in 14nm technology, we verify the efficacy of our designed AI accelerator with STT-MRAM (STT-AI). Compared to an SRAM-based implementation, the STT-AI accelerator achieves 75% area and 3% power savings at iso-accuracy. Furthermore, with a relaxed bit error rate and negligible AI accuracy trade-off, the designed STT-AI Ultra accelerator achieves 75.4%, and 3.5% savings in area and power, respectively over regular SRAM-based accelerators.

Index Terms—STT-MRAM, AI accelerator, Deep Learning hardware

I. INTRODUCTION

The demand for Deep Learning and Artificial Intelligence (AI) is growing at a rapid pace across a wide range of applications such as, self-driving vehicles, image and voice recognition, medical imaging and diagnosis, finance and banking, defense operations, etc. Because of these data-driven analytics and AI boom, demands in deep learning and AI will emerge at both data centers and the edge [1]–[3]. In a recent market research [1], it has been reported that AI-related semiconductors will see a growth of about 18 percent annually over the next few years - five times greater than the rate for non-AI applications. By 2025, AI-related semiconductors could account for almost 20 percent of all semiconductor demand, which would translate into about $67 billion in revenue [1]. As a result, significant R&D efforts in developing AI accelerators - optimized to achieve much higher throughput in deep learning compared to GPUs - are underway from academia, big techs, as well as startups [2]. In AI technology innovation and leadership, high-throughput AI accelerator hardware chips will serve as the differentiator [1], [3].

On-chip memory capacity plays a significant role in the performance and energy efficiency of AI tasks [2]–[5]. In AI accelerator, off-chip Dynamic Random-Access Memory (DRAM) accesses can take 200 times and 10 times more energy compared to the local register file and global buffer memory, respectively [4]. Larger on-chip buffer memory is needed to minimize DRAM accesses, and it can improve the energy efficiency and speed of the accelerator. However, conventional Static Random-Access Memory (SRAM) based solutions suffer from area constraints and leakage power at advanced technology nodes [6], [7], which is a major concern for the energy-constraint IoT domain. STT-MRAM has the potential to replace SRAM as the global buffer in high-performance AI accelerators that require large on-chip memory [3], [8]. For AI accelerators used in inference-only applications, the pre-trained weights need to be stored on-chip. As conventional embedded Flash storage suffers from scalability and reliability issues at advanced nodes [7], emerging memory-based solutions are required for AI accelerators. As analyzed in detail in [9], because of weight reuse in Deep Learning, radiation-induced soft errors in the memory block of the accelerator can impact the accuracy of AI models. This is especially a concern for safety-critical applications such as autonomous vehicles with rigid FIT requirements [9], and STT-MRAM can be a better option for these types of applications.

At scaled technologies (e.g., 10nm and newer), static energy loss from the high leakage current dominates the overall energy dissipation in DRAM and SRAM technologies [7]. Although Trench cap based embedded DRAM (eDRAM) has a higher density compared to SRAM, the leakage power and scaling challenges of eDRAM at advanced process nodes make it less competitive in the future technology roadmap [7]. Beyond 28nm node eFlash faces scaling challenges, and eMRAM technology becomes superior over eFlash because of its lower write voltage and energy, higher endurance, lower area, and faster read/write time [10]. The emerging resistive RAM (RRAM) and Phase Change (PCM) based cross-point memory suffers from endurance, reliability and variability problems [7], [11]. Among all the emerging embedded memory technologies, STT-MRAM is one of the most promising due to its high energy efficiency, write endurance (e.g., more than 1 million cycles), high cell density, high-temperature data retention capability, operating voltage comparable with CMOS logic, and immunity to soft errors [6], [7], [12]–[16]. Moreover, STT-MRAM is highly compatible with CMOS and requires only 2 to 6 extra masks in the backend-of-the-line (BEOL) process [6], [13]. Because of the leakage power issue, beyond a certain memory size, embedded MRAM becomes more energy efficient compared to SRAM [6].

While performing Deep Learning/AI tasks, the throughput
of the AI accelerator primarily depends on, (i) the number of Processing Elements (PE), and (ii) the size of on-chip buffer memory [2, 3]. As a result, area-efficiency is of paramount importance for AI accelerators, and the critical design goal is to increase PE density and on-chip memory capacity. Because of compact size ( 6F² of STT-MRAM vs. 100F² of SRAM [17], [18]), STT-MRAM has the potential to outperform conventional SRAM as the on-chip memory in accelerators. At iso-memory capacities, the MRAM module occupies much lower area compared to SRAM [6]. Additionally, for power constraint mobile/edge/IoT applications, STT-MRAM based AI accelerators can significantly minimize static power compared to SRAMs. However, the higher write energy and write latency of conventional eMRAM can be a deterrent in their full adoption in AI accelerators. In this paper, we present a methodology to design efficient AI accelerators with customized STT-MRAM that can provide high bit cell density while still ensuring fast write speed and decreased write energy. We achieve this feat by analyzing the volatility requirement of weight and input/output feature-map (ifmap/ofmap) data on-chip, and scaling the eMRAM’s retention time accordingly without incurring unacceptable bit error rates.

To the best of our knowledge, this is the first extensive work on designing AI/Deep Learning accelerators with STT-MRAM based on-chip memory systems. The key contributions and highlights of this paper are,

- We present an innovative runtime reconfigurable core design that can be optimized for both dot products of convolution layers and matrix multiplications of fully connected layers.
- We derive the analytical expressions of occupancy times of weights and input/output feature maps in the global memory of the AI accelerator between different stages (i.e., Conv. layer followed by Conv., Conv. layer followed by Fully-Connected (FC) layer, and FC-FC) of AI/Deep Learning operation. Guided by this data activity duration, we scale the retention time of STT-MRAM and customize the design for application as the global buffer memory in energy-efficient AI accelerator. We consider Process variations and runtime Temperature fluctuations in this scaling procedure to ensure negligible read/write Bit Error Rates (BER) and retention failures across all corners.
- Based on detailed design space exploration using state-of-the-art AI/Deep Learning models, an AI accelerator system and MRAM technology co-design framework is presented with the key innovations, - (i) Optimizes STT global buffer size to minimize DRAM accesses. (ii) A novel scratchpad-assisted STT-MRAM based global buffer architecture is presented to minimize the writes to the MRAM by bypassing writes of the partial ofmaps to the scratchpad. (iii) For inference-only tasks, to store the trained weights a specially customized embedded STT-MRAM - as a Flash replacement - with optimized retention time (e.g., 3 to 4 years) and robust BER is used.
- To further improve the energy and area efficiency, we exploited the inherent error tolerance of Deep Learning/AI models and created two STT-MRAM banks for the global buffer. For the first bank, the thermal stability factor is scaled further to a relaxed BER, and the less critical half of the weights/ifmap bits (e.g., LSB groups) are stored in this memory block. The second bank has scaled retention time with a robust BER, and the other remaining half of the bits (e.g., MSB groups) are stored in this bank.

The rest of the paper is organized as follows. The background is discussed in Section II. STT-MRAM based optimum AI/Deep learning accelerator design methodology is presented in Section III. The AI accelerator-aware eMRAM technology co-design methodology is presented in Section IV. We present Simulation Results in Section V, Related work in Section VI, and Conclusions in Section VII.

II. BACKGROUND

A. Deep Neural Networks

At the core of Deep Learning/AI is the Deep Neural Network (DNN). Modern state-of-the-art DNN consists of stacks of Convolution layers to extract the objects’ features and a few Fully Connected layers at the end to classify them. Convolutions are element-wise dot products between matrix (or vector) and matrix. In convolution, kernels convolve over input feature maps (ifmap) to extract embedded features and generate the output feature maps (ofmap) by accumulating the partial sums (psums) as shown in Fig. 1. Each fmap and filter is a 3D structure consisting of multiple 2D planes, and a batch of 3D fmap is processed by a group of 3D filters in a layer. Activation functions (e.g., ReLU) operate on the results before they go to the MaxPooling layer. The computations of a convolutional layer can be expressed as:

\[
\text{Output fmaps (ofmap)} = \text{Convolution Operation (ifmap)}
\]

Figure 1: Convolution and fully connected layer operations
the output activation \((X_o)\) of a layer is obtained by multiplying the input activation \((X_i)\) matrix/vector with the weight matrix \((W)\) followed by the addition of a bias term, and finally passing the result through a non-linear function such as ReLU, \(X_o = ReLu(X_i \ast W + b)\).

**B. Deep Learning/AI Hardware Accelerators**

SIMD, or Systolic array based hardware optimized for matrix (or vector)-matrix multiplication, is the present state-of-the-art hardware to accelerate AI operations \([2, 3]\). The systolic array is only optimized for matrix-matrix multiplication, but it cannot perform the dot product necessary for convolution layers. Mapping the convolution dot products into the matrix multiplications by converting the activation maps into the Toeplitz matrix and the kernel weights into a row vector is a popular solution to address this problem. Nonetheless, it involves redundant data in the input feature map which give rise to inefficient memory storage, and complex memory access pattern \([2]\). More recently, heterogeneous architectures are evolving that have optimized cores for Convolution and FC layers \([5]\). While this solves the complications regarding Toeplitz matrix conversion, it incurs area overhead. Because when convolution core is active, FC core remains idle, wasting circuit area. In response to the existing issues, in this paper, we propose a novel concept of a reconfigurable core capable of efficiently performing both convolution dot products and matrix multiplications based on the operation-dependent (i.e., convolution or fully-connected) control signal.

**C. Memory System in AI/Deep Learning Hardware**

The memory system is one of the vital metrics in determining the performance of AI hardware. Each off-chip DRAM access is 100 to 200 times more energy costly than any ALU operation or a local memory (e.g., register file/scratchpad) access \([2]\). As a result, most energy-constraint AI hardware leverage a memory hierarchy of register file, global buffer, and DRAM. Moreover, a significant amount of memory is required to store the pre-trained weights for inference-only applications. The larger the global buffer memory, the more energy-efficient the AI hardware is due to lower DRAM access. Most of the existing DNN hardware use SRAM both as Global Buffer and Register file and eFlash as weight storage memory \([2]\). Because of the large size of SRAM and static energy loss due to high leakage at scaled nodes (e.g., 10nm and newer), the global buffer size cannot be increased beyond a certain threshold energy-efficiently. eFlash starts to suffer from scaling challenges even at earlier technology such as 28nm \([10]\). The benefits of our proposed Δ-customized STT-MRAM as a replacement of both the SRAM-based global buffer and the eflash-based weight storage memory are many-fold: higher memory capacity, lower read-write latency and energy, and higher endurance against soft errors.

III. EFFICIENT AI/DEEP LEARNING HARDWARE

Fig. 2 depicts the top-level architecture of the accelerator containing the proposed reconfigurable core and MRAM-based memory system. The following sections describe the dataflow in convolution and systolic mode and formulate the memory occupancy time in each mode.

**A. Reconfigurable Core**

The architecture and workflow of our proposed Reconfigurable Core are quite simple but powerful enough to support both matrix multiplication and convolution dot product at runtime configuration. The reconfigurable core consists of three MAC modules and four Multiplexers. Each MAC contains a BFloat16 multiplier and an FP32 adder \([19, 20]\) to accommodate both training and inference. If only inference is desired, the hardware can be 8-bit int8 type \([2, 3]\). The multipliers take input feature maps and filter weights as inputs and pass the results to their neighboring adders to be added with the previous partial sum results. The multiplexers act as mode selectors of the core. When Mode is de-asserted, the MACs are disconnected from each other and their outputs are collected downward to reflect the systolic array architecture (Fig. 3(b)). On the other hand, when Mode is asserted, three MACs collectively act as a convolution block that performs three dot products parallelly and produces one partial sum (Fig. 3(c)). In this case, adder3 adds the outputs of multipliers and multiplier2 to produce the intermediate sum. Meanwhile, adder1 adds the multiplier1 output with the previous partial sum. These operations occur concurrently, provided that the input activations and filter weights are assigned to the multipliers parallelly. Once the outputs from adder3 and adder1 are ready, adder2 sums them up to produce the PE_OUT. The building block containing three MACs and four Multiplexes is defined as a Process Element (PE) block for convolution in this work. Fig. 3 illustrates the functionality of the Reconfigurable core in systolic array mode (b) and convolution mode (c).

**B. STT-MRAM Based On-Chip Memory System**

The prime criteria of memory to sustain as an on-chip memory are: high density, low read/write latency and energy. Conventional STT-MRAM suffers from high read/write energy and latency. However, in the case of on-chip memory/global buffer, the intrinsic non-volatility property of STT-MRAM can be compromised to minimize the read/write energy and latency by adjusting the thermal stability factor (Δ). Considering the data retention time in the global buffer, Δ can be scaled down to achieve a significant reduction in read/write energy, latency, and increase in cell density. This subsection will formulate necessary expressions to calculate the data retention time in the
global buffer for the most time-consuming AI operations, such as the convolution layer and fully connected layer operations. The derived expressions will help us to precisely determine the maximum data retention time in global buffer, and thus help to scale down Δ.

Deep Learning/AI operations are layer-wise sequential operations, meaning the current layer’s output acts as input to the following layer. To formulate the data retention time between two consecutive layers, in inference mode, we define \( T_1 \) as the time required by the accelerator to generate the ofmap of one layer. Once the ofmap of one layer is generated, it goes through Maxpooling and Activation functions (e.g., ReLU) to serve as the input to the following layer. We refer \( T_{pool\_rela} \) as the time required to perform the Maxpooling and ReLU operations. The time required to generate the ofmap of the following layer is termed as \( T_2 \). Finally, \( T_{ret} \) is the data retention time in memory between two consecutive convolution (or fully connected) layers.

1) Retention time for Conv-Conv layers: In convolution mode, each PE block of the array performs the dot product between the input feature maps (ifmaps) and weights. Each unit PE block’s size is defined as \( P_s \), where \( P_s \) represents the number of elements the MAC module can process. The ifmaps and kernel weights are loaded into the PE array from global buffer memory, and the PE array computations occur in parallel. Without loss of generality, in our analysis, we adopted the Row Stationary data flow where kernel rows are loaded into the PE blocks and kept stationary, and ifmaps are loaded and shifted according to the stride size \( [2, 4] \). The partial sums are accumulated vertically to generate the output feature maps (ofmaps). This process is repeated until a complete ofmap is generated. Setting \( Mode = 1 \) in the Muxes of the PE blocks (Fig. 3) ensures that the Reconfigurable core is acting as a Convolution core.

To calculate \( T_1 \), we formulate an expression that helps us estimate the time required to generate the output (ofmap) of a convolution layer. We assume that the operations related to the next output channel will be assigned in the accelerator array only after all the MAC operations related to the previous output channel have been completed. In other words, in an iteration of the accelerator array, the input channels present in it are all related to the same output channel. In addition to simplifying the PE scheduling procedure, this assumption also aligns with our goal of obtaining a convolution layer’s worst-case completion time.

For layer \( n - 1 \), a single row of a partial ofmap (i.e., ofmap corresponding to one kernel and one input channel) will require, \( (k_h \ast |k_w| / P_s) \) PE blocks (symbol meanings are given in Table 1), implying that a partial ofmap for a single input channel will require, \( N_{ofmp\_rw} \ast k_h \ast |k_w| / P_s \) PE blocks. (The \( \lceil x \rceil \) symbol means ceil operation where the result is rounded to the nearest larger integer). An example of convolution operation inside the core in Conv. mode is shown in Fig. 3.

Next, we find out how many partial ofmaps (i.e., how many input channels) can be fitted in the full accelerator array in one step. This number is obtained by dividing the total available PE blocks in the accelerator array, \( W_A \ast H_A \), by the number of PE blocks required for one input channel. The total number of required steps (i.e., number of times the complete accelerator array will be used) for all input channels \( (N_{in\_ch}) \) for one 3D filter (i.e., one output channel), \( N_{steps\_per\_ch} \) can be expressed as,

\[
N_{steps\_per\_ch} = \left\lceil \frac{N_{in\_ch} \ast k_h \ast N_{ofmp\_rw} \ast \lceil \frac{T_{cl}}{\lceil T_{cl} / N_{bat} \rceil} \rceil}{W_A \ast H_A} \right\rceil
\]

(2)

The details of the symbols used in Equations (2)-(6) can be found in Table 1. Inside the accelerator, time for each of the above steps,

\[
t_{per\_step} = T_{cl} \ast N_{cyc\_per\_stp} \ast N_{ofmp\_cl} \ast N_{bat}
\]

(3)

\( N_{cyc\_per\_stp} \) refers to the total clock cycles required in the accelerator, for one image of the batch, to perform, (i) dot products between the kernel and ifmap elements, (ii) partial sum accumulation of the dot products, and (iii) partial sum of ofmap of previous input channel with current channel. This term depends on the circuit-level implementation of accelerator hardware. The term \( N_{ofmp\_cl} \) appears in Equation (4) because the kernel needs to be shifted (i.e., according to the stride...
parameter of convolution) this many times to generate the partial ofmap for each input channel. \( N_{\text{bat}} \) appears in the equation since each image from the mini-batch will be serially processed [4]. In between each input channel operations, the partial sum of ofmaps of the input channels will be stored in the scratchpad to be accumulated to the next input channel’s partial ofmaps to finally create the full ofmap output for that particular output channel and filter. The total time required to generate each output channel/ofmap, \( t_{\text{per out ch}} \) is given by,

\[
t_{\text{per out ch}} = N_{\text{steps per out ch}} \times t_{\text{per step}}
\]

(4)

If there are a total of \( N_{\text{out ch}} \) output channels, then the total time required to generate the full ofmap (i.e., for all output channels) is, \( T_1 = t_{\text{per out ch}} \times N_{\text{out ch}} \). Using Equations (2) - (4), the \( T_1 \) term can be expressed with the following equation. All parameters in Equation (5) are for Conv. layer \( n - 1 \).

\[
T_1 = \left[ \frac{N_{\text{in ch}} \times k_h \times N_{\text{ofmap rw}} \times \left[ \frac{1}{H} \right]}{W_A \times W_A} \right] \times T_{\text{clk}} \times N_{\text{cy c per step}} \times N_{\text{ofmap cl}} \times N_{\text{bat}} \times N_{\text{out ch}}
\]

(5)

The ofmap of layer \( n - 1 \) will act as ifmap to next layer \( n \) after passing through the ReLU and MaxPool layers. The \( \text{ifmap}_n \) should be retained in the memory until layer \( n \) has finished reading it to generate its output ofmap. A closer look into the situation will reveal that the input data read time for layer \( n \) is related to the ofmap generation time. This implies that the \( \text{ifmap}_n \) data need to be in the memory for a maximum duration of time that is equal to the time required for complete ofmap generation. Considering the above facts, we first calculate ofmap generation time using the similar methods of Equations (2) - (5) and then assign it as \( T_2 \). All parameters in Equation (6) are for Conv. layer \( n \).

\[
T_2 = \left[ \frac{N_{\text{in ch}} \times k_h \times N_{\text{ofmap rw}} \times \left[ \frac{1}{H} \right]}{W_A \times W_A} \right] \times T_{\text{clk}} \times N_{\text{cy c per step}} \times N_{\text{ofmap cl}} \times N_{\text{bat}} \times N_{\text{out ch}}
\]

(6)

ReLU and MaxPool layers take relatively much shorter time and also do not involve complex computations as Conv. layers do. Therefore, we can directly estimate \( T_{\text{pool relu}} \) from hardware implementation of ReLU and MaxPool layers. Combining \( T_1 \), \( T_2 \), and \( T_{\text{pool relu}} \), we can estimate the required data retention time, \( T_{\text{ret}} \), in memory between two consecutive Conv. layers in inference phase.

\[
T_{\text{ret conv}} = T_1 + T_{\text{pool relu}} + T_2 \quad \text{(7)}
\]

2) Retention time for FC-FC layers: To perform the computations associated with FC layers, the Reconfigurable Core transforms into the Systolic array. This is achieved by disabling the Mode signal of the Muxes present in the PE blocks. In this section, we formulate an expression to estimate the time required to compute the output of an FC layer. The systolic array shown in Fig. 3(b) has \( H_A \times W_{SA} \) MAC modules. Because of the reconfigurable feature of the core, \( W_{SA} = P_A \times W_A \). The weights are loaded into the array according to the capacity of the systolic array implying that the number of weights can be loaded into the array in one step is equal to the number of MACs present in the array, \( N_{\text{wt per step}} = H_A \times W_{SA} \). If the total number of weights is greater than the number of weights the array can accommodate in one step, i.e., \( N_{\text{tot wt}} > N_{\text{wt per step}} \), using the concept of divide & conquer in matrix multiplication (Fig. 5(b)) we find out how many steps (i.e., number of times we need to load new weights to the accelerator array) are required to complete the computation with all elements of the weight matrix. The number of steps required to complete the computation with all weights is, \( \left[ \frac{m_{fc}/H_A}{n_{fc}/W_{SA}} \right] \). (For symbol meanings see Table 1). In every step, the array is loaded with \( N_{\text{wt per step}} \) weights, inputs are streamed from left to right, and the partial sums move downward to be collected in accumulators [3]. The clock cycles required to complete each step are \( N_{\text{cyc per step}} \) that depends on the circuit-level implementation of systolic array hardware and the dimension of systolic array core. Combining the above terms, and considering there are \( N_{\text{bat}} \) images in the mini-batch, time required to generate the output of FC layer \((n - 1)\), \( T_1 \), is expressed in Equation (9), where all parameters are for FC layer \((n - 1)\).

\[
T_1 = \left[ \frac{m_{fc}/H_A}{n_{fc}/W_{SA}} \right] \times T_{\text{clk}} \times N_{\text{cy c per step}} \times N_{\text{bat}}
\]

(9)

FC layer \( n \) will consider the output of previous FC layer \((n - 1)\) as its input. The output of FC\(_{n-1}\) should be stored in the memory until FC\(_n\) has completed reading it for generating its output. With this reasoning, we calculate the output generation time for FC\(_n\) following the above method and assign it as \( T_2 \). All parameters of Equation (9) are for FC layer \( n \).
Two consecutive FC layers do not have MaxPooling layer in between. Therefore, we can find the data retention time, $T_{ret_{fc-fc}}$, for an FC layer followed by another FC as,

$$T_{ret_{fc-fc}} = T_1 + T_2$$

C. Retention time of Convolution layer followed by FC layer

The retention time between a Convolution layer followed by an FC layer is also expressed as,

$$T_{ret_{conv-fc}} = T_1 + T_{pool\_relu} + T_2$$

Here, $T_1$ is the time required to generate the Conv. layer of map and $T_2$ is the time required to generate the FC layer output.

Using the above expressions of weight, ifmap, and ofmap occupancy times in global buffer memory, for a particular accelerator hardware architecture and the operating clock frequency, we can estimate the maximum retention time required for STT-MRAM based global buffers. The MRAM Write and Read times will be added with the above retention time expressions. As the MRAM Read/Write times are orders of magnitude lower (i.e., less than 10ns) compared to the retention times $T_1$ and $T_2$ which are in the ms or s range as explained in Section IV, we did not explicitly add the MRAM Read/Write time with the above retention time ($T_{ret}$) expressions.

IV. OPTIMIZING STT-MRAM FOR AI ACCELERATORS

A bit cell of STT-MRAM consists of a Magnetic Tunnel Junction (MTJ) for storing the bit and an access transistor to read/write the bit. The MTJ contains two ferromagnetic layers, one with fixed magnetic orientation, and another free layer whose orientation can be switched externally by an applied current. The orientation of the free layer relative to the reference layer represents the state of the stored bit; parallel orientation refers to logic 0, while anti-parallel orientation refers to logic 1. Fig. 6 depicts the cell schematic, read, and write operations.

Where, $E_b$ = Energy Barrier of free layer, $k_B$ = Boltzmann Constant, $T$ = Temperature, $H_K$ = Anisotropy field, $M_S$ = Saturation Demagnetization, $V$ = Volume of MTJ.

Critical current, $I_c$, is defined as the minimum current required to flip the state of the free layer [18], [21], [22]. The critical switching current is modeled as [21], [22]:

$$I_c = \left(\frac{4e k_B T}{h}\right) \star \frac{\alpha}{\eta} \star \Delta \star \left(1 + \frac{4\pi M_{eff}}{2H_K}\right)$$

Where, $e$ = electron charge, $k_B$ = Boltzmann Constant, $T$ = Temperature, $h$ = Plank’s Constant, $\alpha$ = LLGE damping constant, $\eta$ = STT-MRAM efficiency parameter, $4\pi M_{eff}$ = Effective demagnetization field, and $H_K$ = Anisotropy field.

2) Retention Time & Retention Failure: Once data is written, MTJ should retain its state, even if the power source is removed, until any external force is applied to flip the state. However, due to thermal noise, the logic state might get flipped unintentionally. The maximum time MTJ can retain its non-volatility is known as data retention time. The retention failure probability for a given time period $t_{ret}$ is [21], [22]:

$$P_{RF} = 1 - \exp \left[-\frac{t_{ret}}{\tau*\exp(\Delta)}\right]$$

Where, $t_{ret}$ = retention time, $\tau$= technology constant.

3) Read Disturbance (RD): To read a bit from STT-MRAM, read current $I_r$, much less than the critical current $I_c$, is flown from bit line through the access transistor and MTJ. Fig. 6 shows that writing 1 and reading (both 0 & 1) share the same current path. This can sometimes cause the unintentional switching of the bit-cell content resulting in Read Disturbance (RD). For read current $I_r$ and read latency $t_r$, the probability of RD can be modeled as [21], [22]:

$$P_{RD} = 1 - \exp \left[-\frac{t_r}{\tau*\exp(\Delta(1 - \frac{t_r}{\tau}))}\right]$$

4) Write Error Rate (WER): Writing a bit cell requires a write current $I_w$, larger than $I_c$, to be flown between BL to SL as shown in Fig. 6. Because of the stochastic nature of the write operation, the switching time of MTJ varies from access to access [18], [21], [22]. If the write current is terminated before the free layer has successfully changed its state, the write operation can be erroneous. For write pulse width $t_{wp}$, the Write Error Rate (WER) is [21], [22]:

$$WER_{bit} = 1 - \exp \left[-\frac{-\pi^2 \Delta \left(1 - \frac{t_{wp}}{\tau}\right)}{4\left(1 + \frac{t_{wp}}{\tau}\right)}\right]$$

B. Customizing STT-MRAM For AI Accelerators

1) Scaling Thermal Stability Factor: To achieve typical retention period of 10 years, the thermal stability factor, $\Delta \geq 60$ is required [10], [13], [18], [21]–[23]. However, such a long retention time may be unnecessary depending on the application. For example, if MRAM is used as the global buffer memory in AI accelerators, then the retention time can be significantly scaled depending on the weight and input/output feature-map data occupancy time (e.g., $ms$ to $s$ range) in that memory. If STT-MRAM is used as eFlash replacement for pre-trained weight storage for AI inference tasks, then 3 to 5 years retention might be enough instead of 10 years. From Equation (12), it is
seen that by adjusting the volume (i.e., area and/or thickness) of the MTJ the thermal stability factor ($\Delta$) can be scaled. In other words, considering the target operating temperature range of the AI accelerator and the expected life-time of the data, scaling down of thermal stability factor will improve area efficiency by increasing the memory bit-cell density. Moreover, with scaled $\Delta$ and bit-cell area, the cell would require a lower operating current, thus saving energy.

2) Optimizing Read/Write Latency and Energy at Target WER and RD: Recent state-of-the-art STT-MRAMs can compete or outperform SRAMs in all aspects except write energy and write latency [6], [13], [14]. However, for AI accelerator applications, by scaling $\Delta$ and the retention time of STT-MRAM we can circumvent the write energy and latency limitations. Equation (16) implies that write latency, $t_{write} \propto \ln(\Delta)$ at constant write error rate. We can exploit this relationship to reduce the write latency with scaling down of $\Delta$. From Equation (14) we infer that retention time $t_{ret}$ is exponentially proportional to $\Delta$. Thus, depending on the desired retention period of STT-MRAM in AI accelerator, we can optimally scale down $\Delta$, and also minimize write latency at that target retention time. However, Equation (16) also implies an inverse relationship between write latency and write error rate, which hinders us from aggressively scaling down write latency at the desired $\Delta$. Fortunately, to boost the writing speed at the scaled $\Delta$, we can keep $I_w$ higher (e.g., close to the pre-scaled value), and this can assist in designing a STT-MRAM with high write-speed [18]. Recently, high-speed write has been experimentally demonstrated in [16] by optimizing the free layer materials. We can identify the optimum $\Delta$ and $I_w$ that minimizes write latency, write energy while still satisfying the WER and retention time requirements for the AI accelerator. As depicted in Equation (13), with scaling of $\Delta$ the critical current $I_c$ decreases linearly, and hence read current $I_r$ also decreases. At this scaled $\Delta$ and $I_r$, the read latency can also be scaled by adjusting the sense amplifier reference voltage [6], [18]. Equation (15) implies that at scaled $\Delta$, the shortened read pulse duration will also ensure that the Read Disturb rate is within the acceptable target.

C. Addressing Process and Temperature Variation

The performance of MRAM can degrade due to the process and temperature variations [6], [13], [24]. Process-induced variations in free layer thickness in MTJ, and in access transistor channel length/width and threshold voltage contribute to the performance variations in MRAM. From Silicon measurement data in [6], the standard deviation ($\sigma$) of MTJ diameter variation was reported to be 2.1% of the mean. Magnetic Anisotropy field ($H_K$) is another source of process variation in STT-MRAM.

Figure 7: Impact of process and temperature variation on thermal stability factor ($\Delta$).

The bit-cells are placed compactly on the layout, as a result, the bit-cell to bit-cell variations within the same die/chip are minimal, and the process variation is dominated by the chip-to-chip variations. $\Delta$ increases with an increase in MTJ diameter and $H_K$ due to process variation, and a decrease in temperature from the nominal value (Fig. 7 and Equation 12). An increase in $\Delta$ increases critical current ($I_c$) which eventually increases the write current ($I_w$) (Equation 14 and 16). Given the smaller write pulse, write failure occurs when supplied $I_w$ is less than the required $I_{w_{\text{required}}}$. Worst-case occurs when both, (i) the supplied $I_w$ decreases due to the access transistor being in the slow process corner, and (ii) the required $I_{w_{\text{required}}}$ increases due to increase in $\Delta$ resulting from Process and runtime Temperature (PT) variations. On the other hand, decrease in $\Delta$ beyond a minimum due to PT variation will result in retention failure (Equation 14).

To protect the desired $\Delta_{scaled}$ against the worst-case PT variation, appropriate Guard-Band needs to be added. The $\Delta_{PT_{GuardBanded}}$ is chosen to cover both the worst-case $4\sigma$ range (i.e., 99.993% of the samples) of process variation and high temperature operating scenario as shown in Equation 17.

$$\Delta_{scaled} \leq (\Delta_{PT_{GuardBanded}} - 4\sigma) \cdot (T_{nom}/T_{hot})$$

Equation 17)

The chip samples located on the right side of the process variation distribution (i.e., $\mu + n \cdot \sigma$, where $n \geq 1$) of $\Delta_{PT_{GuardBanded}}$ will experience larger $\Delta$ as shown in Fig. 7 and 8. Additionally, at cold temperatures, the $\Delta$ will further increase to $\Delta_{PT_{MAX}}$ as shown in Equation 18. Although the higher $\Delta_{PT_{MAX}} > \Delta_{scaled}$ will be benign for retention time, the required write current will increase in this scenario to confine the write time and Write Error Rate (WER) of these samples within the nominal bound. Designing the write driver for this worst-case scenario will dissipate unnecessary power for all other non-worst-case samples. To address this, we propose a dynamically adjustable write driver depicted in Fig. 9. The proposed write-driver circuit provides additional write current in extreme PT conditions. The Process and Temperature Monitor (PTM) block continuously monitors the process and temperature changes. In addition to adjusting the write current according to process variation profile of the MRAM chip/die, the PTM also senses the runtime temperature and adjusts the current dynamically by turning on/off the additional PMOS transistors (Fig. 9). For example, at the nominal process and temperature, the extra transistors can be off, however, at PT-induced rise in $\Delta$ the transistors can be individually activated to ensure successful write.

![Figure 8: Distribution of read/write currents with process variation. Worst-case occurs when worst process corners experience $T_{hot}$ or $T_{cold}$.](image)
In summary, we design the MTJ with higher $\Delta_{PT,GuardBanded}$ than the desired $\Delta_{scaled}$ to accommodate potential degradation in thermal stability from worst-case $4\sigma$ process variation and runtime high temperature, and proposed a write-driver with controllable current drive to address the high write-current demand at cold temperature and slow process corner.

D. MRAM Write Energy Optimization in Accelerator with ScratchPad

Addressing the fact that the write energy of STT-MRAM is higher than the read energy, we propose an innovative scratchpad-assisted MRAM global buffer architecture to minimize the write frequency in STT-MRAM, and thus further optimize the energy. Reduced write-frequency is achieved by using a small global SRAM scratchpad, typically in the KB range (details in Section V), in addition to a large (i.e., MB range) global STT-MRAM buffer. When the accelerator PE array generates partial ofmaps (i.e., ofmap corresponding to each input channel), they need to be stored somewhere in memory to be added to the next partial ofmap to produce the complete ofmap of an output channel. The reason behind these partial-ofmap writes is that the accelerator might not produce the complete ofmap in one step. Between the subsequent steps, the partial ofmap result from the previous step needs to be written in the memory to be subsequently read and accumulated with the partial ofmap result from the following step. Adding this small SRAM scratchpad memory (for intermediate ofmap writes) with MRAM global buffer further improves the energy efficiency of MRAM-buffer-based deep learning accelerators. In summary, our proposed scratchpad-assisted MRAM memory architecture provides energy efficiency by, (i) minimizing the STT-MRAM write frequency, and (ii) additionally, at a smaller size, SRAM is more energy-efficient than STT-MRAM.

V. RESULTS AND ANALYSIS

A. Design Space Exploration for Selecting Memory Capacity

Nineteen widely used state-of-the-art deep learning models were analyzed to design and validate our STT-MRAM based AI accelerator with the reconfigurable core. Fig. 10(a) shows the model sizes both in 8-bit int8 (left Y-axis) and 16-bit BrainFloat16 (BF16) (right Y-axis) datatypes. For inference-only accelerator int8 datatype and hardware suffice, however, if full-scale training or transfer-learning is desired then BF16 hardware and data-type are necessary.

The models’ sizes imply that around 280MB and 140MB of STT-MRAM is required as non-volatile (NVM) weight storage memory to store the pre-trained models using BF16 and int8 datatypes, respectively. The STT-MARM non-volatile weight storage memory can replace the currently used eFlash memory as an efficient alternative. Fig. 10(b) and (c) represent the input/output featuremap and weight size ranges of all models for convolution layers both in int8 (left Y-axis) and BF16 (right Y-axis) formats, and these data helps us to estimate the maximum required global buffer (GLB) memory size to avoid DRAM accesses during each convolution layer operation. In the cases of fully-connected layer operations, only the featuremaps, usually in KB range for most of the models, are stored in the GLB, and the weights, around 200MB in size for the largest model in BF16, are directly assigned from DRAM (or weight-storage NVM) to the systolic array for matrix multiplications. Hence, we ignored the fully connected layers’ weight and activation sizes from design space analysis for selecting on-chip GLB memory capacity.

![Figure 9: Modified Write Driver](image)

![Figure 10: (a) Complete sizes of widely used AI models. (b) Activation map (ofmap/fmap) sizes, (c) Weight sizes for Conv layers.](image)

![Figure 11: Required capacity of global buffer with varying batch sizes to avoid DRAM access during inference.](image)
batch sizes. For smaller batch-size (i.e., \(\leq 2\)), a maximum of 12MB of GLB would be enough for int8 datatype. With 12MB on-chip GLB memory, most of the models, except a few (e.g., Darknet53, VGG19, Nasnetlarge, Xception, etc.), can support larger batch-sizes such as 8. For BF16, 12MB would suffice for batch size 1 for all models. If pruned models [2] are used, batch of more images can be fit into the GLB. For high-performance accelerators that operate with larger batches of data, the GLB size can be further increased.

When a Conv. layer data - ifmap, weight, and ofmap - do not fit into GLB at one attempt, extra DRAM accesses are needed, incurring extra energy and latency. Fig. 12 (a) shows, if a GLB of 12MB is used, even larger batch sizes, such as 8, the extra DRAM access-related latency is zero for most of the models (int8 case), and around 2ms for few models. For BF16 datatype, the extra DRAM access latency increases slightly but is within 10ms. Fig. 12 (c) depicts that if the GLB size is 12MB, for most of the models in int8 datatype extra DRAM access-associated energy reduces to zero. For BF16 datatype, most models would need a few extra DRAM accesses (Fig. 12 (d)). The DRAM access energy and latency were calculated for dual-channel DDR4-2933 DRAM with 64bit data bus.

B. Memory Retention Time Estimation for AI Models and Accelerator Architecture

The data retention time in GLB for the models (in BF16 datatype) are calculated using Equations 5-11 (Section III) and the post-layout timing results from the implementation of our proposed reconfigurable accelerator core at 14nm technology (Table II). The results for 42x42 MAC array and batch size 16, presented in Fig. 13 show that the maximum data retention time in GLB for all models is less than 1.5s where most models have retention time less than 0.5s. The retention time goes even smaller (in ms range) for int8 datatype as the clock cycle reduces significantly (usually 1-2 clock cycles) in int8 version hardware. Fig. 14(a) shows the maximum retention time for all models (in BF16 datatype) for fixed batch size 16 and varying MAC array sizes, whereas Fig. 14 (b) shows the maximum retention time needed for a fixed MAC array size of 42x42 for varying batch sizes. From the figures, it is evident that further reduction in retention time can be achieved by using the proper combination of batch and MAC array sizes.

C. Customizing STT-MRAM for AI Accelerator

Using Equation (14), we analyzed the impact of thermal stability factor (\(\Delta\)) on retention time within certain Bit Error Rates (BER). To identify the target BER of STT-RAM for applications in pre-trained weight storage and global buffer (GLB) memory, we first analyzed the size of modern AI models. From Fig. 10 (a), it can be seen that a few hundred MBs would be enough to store the pre-trained weights, within this memory capacity we choose BER in the order of \(10^{-9}\) (i.e., 1 bit-flip per 1 billion bits). Given the worst-case cumulative BER can occur from Retention Failure (RF), Read Disturb (RD), and Write Error (WE), the worst-case bit-flips for VGG16 at this BER is about 12 bits. This BER is negligible and cannot make any impact on the AI task's accuracy [25]. Fig. 15 (a) shows that...
with $\Delta = 39$ we can ensure the loaded pre-trained weight will successfully remain in the accelerator for about 3 years at this target BER, which is enough given that AI models are replaced frequently with better ones. To address Process variation and runtime Temperature fluctuation, we chose $\sigma = 2.1\%$ of mean, $T_{\text{max}} = 120^\circ\text{C}$ ($393\text{K}$) and $T_{\text{cold}} = -20^\circ\text{C}$ ($253\text{K}$) in the Equations [17 and 18] as discussed in Section IV(C) and adjust $\Delta = 39$ to $\Delta_{PT} = 55$ after guard-banding. 

For GLB memory, we can lower the $\Delta$ and retention time much lower according to the average occupancy time of weight and input/output fmaps in the accelerator’s GLB memory. Also, since this memory size is within few tens of MB (e.g., 12MB), we can increase the BER to $10^{-8}$, which will cause less than 3 bit-flips in the worst-case (i.e., considering BER from Retention Failure (RF), Read Disturb (RD), and Write Error (WE)) at this memory size. The accuracy impact of deep learning models at this BER and memory size is negligible [25].

Next, we analyze the impact of scaling $\Delta$ on the read pulse width. If the read pulse width is large then the chances of RD increase. Moreover, with scaling $\Delta = 19.5$ (after Guardbanding $\Delta_{PT, GB} = 27.5$), the required read current also decreases. As a result, a significant reduction in read energy is also possible. In our study of $\Delta$ scaling impact of read/write latency, as the base-case STT-MRAM we used the chip-implemented (for 10 years retention) data of [6, 13]. Fig. 15 (c), (e) uses base-case (i.e., $\Delta = 60$) from [6], and (d), (f) from [13]. With the scaling of retention time, the write latency only scales as a factor of $\ln(\Delta)$, to further decrease the write latency we can use the write current as another knob as discussed in Section IV. The write latency scaling are shown in Fig. 15 (e), (f).

We used Destiny memory modeling tool [17] to compare STT-MRAM area and energy with SRAM while $\Delta$ is scaled down. Although theoretically, STT-MRAM has a minimum area of $6F^2$, however, silicon results show that MRAM area scaled by 70% compared to SRAM at 14nm node [6]. We modified the Destiny tool to incorporate this silicon observation. The results for scaled $\Delta$ at 14nm technology node are shown in Fig. 16. We see a significant advantage from STT-MRAM beyond 4MB capacity. Compared to SRAM, the area scales by more than ten times at iso-memory-capacity (Fig. 16(b),(d)). Similarly, for STT-MRAM the relative energy efficiency improves as the memory capacity increases (Fig. 16(a),(c)). These results imply STT-MRAM can offer significant performance gains at future high-performance AI accelerators that will use large on-chip buffer memory.

D. Energy Optimization with Variable Retention MRAM Banks

We further improved the efficiency in STT-AI Ultra accelerator with two separate MRAM banks of, $\Delta = 19.5$ (after PT guard-band $\Delta_{PT, GB} = 27.5$), and $\Delta = 12.5$ ($\Delta_{PT, GB} = 17.5$). The first half of the weight/fmap bits are considered significant (MSB group) and stored in $\Delta_{PT, GB} = 27.5$ bank, and the rest of the LSB groups in $\Delta_{PT, GB} = 17.5$ bank. For the LSB group at $\Delta_{PT, GB} = 17.5$ we relaxed the BER to $10^{-5}$ as shown in Fig. 17. The relative gains in energy and area at $\Delta_{PT, GB} = 17.5$ are shown in Fig. 16(c), (d).

E. Optimizing Energy with Scratchpad for Partial Ofmaps

Our simulation results show that for STT-MRAM the write energy is about 70% more than the read energy at scaled $\Delta$. As described in Section IV (D), using a small SRAM scratchpad for writing the intermediate partial ofmaps instead of the MRAM can significantly reduce the write frequency and save energy. Fig. 18 shows the partial ofmap size distribution. For BF16 data type, we see that 52KB (26KB for int8) scratchpad will fit most of the models in one attempt. The normalized energy improvements of proposed scratchpad-assisted MRAM system is shown in Fig. 19 for ResNet-50 model and 14nm technology.
Figure 17: $\Delta$ scaling with relaxed BER for LSB bit groups. (a) Retention, (b) Read, and (c) Write latency within target BER. (Base case, $\Delta = 60$, data modeled after [13]).

Figure 18: Maximum size of partial ofmaps.

Figure 19: Comparison of buffer memory energy dissipation for, (i) SRAM, (ii) MRAM, and (iii) MRAM with scratch pad architectures.

F. Accelerator Implementation

We implemented our AI accelerator architecture with re-configurable cores (i.e., in Fig. 3), at RTL level using BF16 hardware as BF16 can support both inference and training. We used Synopsys 14nm standard cell library [26] to complete synthesis, and place and route of the design. The post-layout CLK cycle data for the PE/MAC are shown in Table II. The top-level view of physical design from ICC2 tool [26] is shown in Fig. 20. We used Synopsys 14nm memory compiler to create the SRAMs for our baseline accelerator. Results from post-layout and timing-closed accelerator design are shown in Table III, where Row 7 shows the area and power for the base-line accelerator with 12MB global buffer memory. Next, to implement MRAM based STT-AI accelerator, we estimated areas and power data from the Destiny [17] tool at scaled $\Delta$ and modeled those as blackbox in the physical design part in Synopsys ICC2 [26] for 14nm node. The 52KB SRAM Scratchpad is divided into two banks with individual CLK/power gating. Rows 4 and 8 show that the STT-AI accelerator offers significant area and leakage energy savings. The STT-AI Ultra accelerator achieves further improvements in power and area as shown in Row 9 in Table III.

G. Accelerator Performance with ImageNet Dataset

Next, we modeled our hardware and STT-MRAM BERs in PyTorch [27] and ran inference for pre-trained AlexNet, VGG16, and ResNet-50 models with ImageNet benchmark to
obtain Top-1 and Top-5 accuracy results. As expected, with STT-MRAM having $\Delta_{PT, GB} = 27.5$, there were no accuracy loss compared to the baseline SRAM version. However, for STT-AI Ultra accelerator, with $BER = 10^{-5}$ in half of the bits (LSB group in lower $\Delta$ STT-MRAM bank), we observed negligible (less than 1% normalized) accuracy loss as shown in Fig. [21].

VI. RELATED WORK

Over the last decade, STT-MRAM technology has been extensively researched for its high-endurance, radiation hardness, non-volatility, and high-density memory properties. The prior works on STT-MRAM applications can be broadly categorized into two domains: (i) Its use as the last-level cache memory in processors; (ii) Its application in emerging Process-in-Memory (PIM) based computing paradigm.

Several studies [29–31] have demonstrated the excellence of STT-MRAM over other NVM technologies in PIM setting due to complex and tunable resistance dynamics achieved through its spin-transfer torque mechanism and simultaneous access to multiple word-lines of the same array. [29] proposed an STT-MRAM based crossbar arrays where the internal resistance states - which were used to mimic the weights of the models - of STT-MRAM were tuned to support non-uniform quantization. This study provided energy efficiency and loss reduction, however, additional circuitry. Digital to Analog Converter (DAC) and Analog to Digital Converter (ADC) were needed to support the PIM workflow. Some studies, such as, [32] used the PIM architecture, where the MAC operation was simplified to addition/subtraction, and bit-wise operation by manipulating the models’ parameters. [31] mapped the LeNet5 model to a synaptic cross-bar array of STT-MRAM memory cells for inference and showed improved performance in terms of area, leakage power, energy over SRAM for 65nm to 7nm technology node. However, major challenges of PIM over conventional Deep Learning/AI are - (i) requirements of additional hardware circuitry, such as DAC, ADC, which results in area overhead; (2) quantization of weights to be represented with fewer bits resulting in lower precision; (3) in digital PIM, extra manipulation of models’ algorithm is needed to replace MAC with the bit-wise operation; and (4) in most of the cases, PIM is only suitable for inference-only applications. Although PIM-based analog architectures provide fast execution, the performance, energy efficiency, and reliability of analog PIM still lags behind the state-of-the-art DNN/AI models and their corresponding hardware accelerators [2].

While some research leveraged the scalable property of thermal stability factor of STT-MRAM to replace SRAM-based cache memory, others used the error tolerance property of certain applications and designed STT-MRAM based energy-efficient cache with approximate storage. In [33], the retention time of STT-RAM was scaled to implement cache memory that can compete with SRAM-based caches, and DRAM-like refresh was used to compromise the ultra-low retention time. In [34], [35] STT-MRAM based approximate cache was proposed to exploit the error-resilience property of some specific applications. Unlike previous studies, [36] proposed a hybrid STT-MRAM design for cache for different applications depending on the run-time requirements without compromising any reliability degradation. In [23], area-and-retention-time-scaled STT-MRAM was presented as DRAM replacement. In [37] a hybrid of SRAM and 3D-stacked STT-MRAM based AI accelerator was proposed for real-time learning where eMRAM acted as weight storage memory for infrequently accessed and updated layers, such as all convolutional layers and first few fully connected layers for a Transfer Learning followed by Reinforcement Learning algorithm. However, due to the use of typical slow and write-power-hungry STT-MRAM, this study could not completely exploit STT-MRAM to substitute SRAM and eventually used SRAM for storing weights of the last few fully connected layers which are accessed and updated frequently in transfer learning-based reinforcement learning setting.

In summary, prior notable research on STT-MRAM applications focused on implementing last-level cache memory, designing in-memory computing architectures, and high-capacity 3D-stacked memory as DRAM replacement for DNN hardware. Our work is the first to present a detailed analysis on the feasibility of using STT-MRAM as high bandwidth on-chip buffer memory in DNN/AI accelerator hardware that can offer much larger capacity at lower energy and area costs compared to SRAM. Moreover, for complete DNN model storage in edge inference devices, non-volatility relaxed STT-MRAM design is presented as an alternative to eflash which suffers from scaling limitations at advanced technology nodes.

VII. CONCLUSIONS

In this paper, we demonstrated the design of highly efficient AI/Deep Learning accelerators that utilize emerging STT-MRAMs. Based on detailed design space exploration we designed the STT-MRAM based global buffer to minimize DRAM access latency and energy, as well as reduce the area and power of the MRAM buffer. We presented an innovative runtime-reconfigurable core optimized for both dot products and matrix multiplication in convolution and fully-connected layers, respectively. A scratchpad-assisted STT-MRAM global buffer design has been demonstrated that reduces the frequency of energy-dominant write operations of the partial of maps during convolution. Using actual data occupancy times in memory for AI tasks, we guide the STT-MRAM thermal stability factor scaling. We showed that with STT-AI accelerator 75% area and 3% power savings are possible at iso-accuracy. Furthermore, with STT-AI Ultra, 75.4%, and 3.5% savings in area and power, respectively, over regular SRAM-based accelerators at minimal accuracy trade-off.

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