Beyond Moore’s technologies: operation principles of a superconductor alternative

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Purpose of this paper is a review of superconducting technology principles of operation and memory circuits design, showing 250 Gflops/W. It is understood that besides other issues of exaflops computer like large space and complex cooling infrastructure, the energy efficiency makes the next step in high performance computing to be extraordinarily difficult, even with planned advances in complementary metal-oxide-semiconductor (CMOS) technology\textsuperscript{10}. Future of high performance computing is most likely associated with one of alternative “Post-Moore’s” technologies where energy dissipation is drastically lower. It is expected that leader will be determined by 2030, while 2020 – 2030 will be the “decade of diversity”. In this paper, we consider one of the most promising candidates for leadership – the superconductor digital technology. Basic element switching energy here is of the order of 10\textsuperscript{-19} J, with no penalty for signal transfer. For a certain algorithm superconducting circuits were shown to be up to seven orders of magnitude more energy efficient than their semiconductor counterparts, including power required for cryogenic cooling\textsuperscript{13}.成熟 level of superconductor technology can be illustrated by the notional prototype of the superconducting computer being developed under IARPA program “Cryogenic computing complexity”\textsuperscript{13}. This is a 64 bit computing machine operating at 10 GHz clock frequency with throughput of 10\textsuperscript{13} bit-op/s and energy efficiency of 10\textsuperscript{-15} bit-op/J at 4 K temperature. Prospective study shows that superconductor computer could outperform its semiconductor counterparts by two orders of magnitude in energy efficiency, showing 250 Gflops/W\textsuperscript{13}

Keywords: superconductor digital electronics; superconducting computer; energy-efficient computing; superconductor logics; Josephson memory

Introduction

World’s largest chipmaker Intel “has signaled a slowing of Moore’s Law\textsuperscript{14}. The company has decided to increase the time between future generations of chips. “A technology roadmap for Moore’s Law maintained by an industry group, including the world’s largest chip makers, is being scrapped\textsuperscript{12}.

Three years ago Bob Colwell (former Intel chief IA-32 architect on the Pentium Pro, Pentium II, Pentium III, and Pentium IV) described stagnation of semiconductor technology in the following sentence\textsuperscript{13}.

- Officially Moore’s Law ends in 2020 at 7 nm, but nobody cares, because 11 nm isn’t any better than 14 nm, which was only marginally better than 22 nm.
- With Dennard scaling already dead since 2004, and thermal dissipation issues thoroughly constrain the integration density – effectively ending the multicore era: “Dark Silicon” problem (only part of available cores can be run simultaneously).

The mentioned fundamental changes are most clearly manifested in supercomputer industry. Energy efficiency becomes a crucial parameter constraining its headway\textsuperscript{16}. Power consumption level of the most powerful modern supercomputer Sunway TaihuLight\textsuperscript{15} is as high as 15.4 MW. It corresponds to peak performance of 93 petaflops (1 petaflops is 10\textsuperscript{15} floating point operations per second). Power consumption level of the next generation – exaflops (10\textsuperscript{18} flops) supercomputers is predicted\textsuperscript{2} to be in the sub-GW level. It is comparable to power generated by a small powerplant and results in an unreasonable bill of hundreds of million dollars per year.

Following roadmap,\textsuperscript{4,5} goal power consumption level of exaflops supercomputer should be of the order of \sim 20 MW. It corresponds to energy efficiency of 20 pJ/flop or 50 GFlops/W. Unfortunately, energy efficiency of modern supercomputers is an order less than required. For example, the energy efficiency\textsuperscript{17} of the Sunway TaihuLight is 6 Gflops/W. It is understood that besides other issues of exaflops computer like large space and complex cooling infrastructure, the energy efficiency makes the next step in high performance computing to be extraordinarily difficult, even with planned advances in complementary metal-oxide-semiconductor (CMOS) technology\textsuperscript{10}.

It is worth to mention that low energy efficiency leads to high power consumption and also limits clock frequency at the level of 4 – 5 GHz. This frequency limit occurs due to “temperature” limitations posed to integration level and switching rate of transistors. Note that cryogenic cooling of semiconductor chips will not solve the problem\textsuperscript{11,12}.

Future of high performance computing is most likely associated with one of alternative “Post-Moore’s” technologies where energy dissipation is drastically lower. It is expected that leader will be determined by 2030, while 2020 – 2030 will be the “decade of diversity”. In this paper, we consider one of the most promising candidates for leadership – the superconductor digital technology. Basic element switching energy here is of the order of 10\textsuperscript{-19} J, with no penalty for signal transfer. For a certain algorithm superconducting circuits were shown to be up to seven orders of magnitude more energy efficient than their semiconductor counterparts, including power required for cryogenic cooling\textsuperscript{13}. Maturity level of superconductor technology can be illustrated by the notional prototype of the superconducting computer being developed under IARPA program “Cryogenic computing complexity”\textsuperscript{13}. This is a 64 bit computing machine operating at 10 GHz clock frequency with throughput of 10\textsuperscript{13} bit-op/s and energy efficiency of 10\textsuperscript{-15} bit-op/J at 4 K temperature. Prospective study shows that superconductor computer could outperform its semiconductor counterparts by two orders of magnitude in energy efficiency, showing 250 Gflops/W\textsuperscript{13}.

Purpose of this paper is a review of superconducting logic and memory circuits principles of operation and
analysis of their issues in respect to computer circuits design. We certainly do not claim to be comprehensive while considering only the most common solutions. Our review contains two main parts describing logic and memory, correspondingly.

In the first part we start with examination of physical basis underlying logic circuits operation. Superconductor logics are presented by two main branches: digital single flux quantum (SFQ) logics and adiabatic superconductor logic (ASL). Basic principles of SFQ circuits operation are shown on example of the most popular rapid single flux quantum (RSFQ) logic. It’s energy efficient successors and competitor, LV-RSFQ, ERSFQ, cSFQ and reciprocal quantum logic (RQL), are considered subsequently. ASL is described in the historical context of its development for ultra energy efficient reversible computation. The modern status is presented by two implementations of this logic. It can be noted that superconducting adiabatic cells are used also in quantum computer circuits like the ones fabricated by D-Wave Systems.

The second part of the review is devoted to cryogenic memory. Four approaches are described: SQUID-based memory, hybrid Josephson-CMOS memory, Josephson magnetic random access memory (JMRAM), and orthogonal spin transfer magnetic random access memory (OST-MRAM). They are presented in historical order of their development. In the end of each part of our review we briefly discuss major challenges and directions of possible further research in the studied area.

Review

I. LOGIC

A. Physical basis underlying logic circuits

The fundamental physical phenomena underlying superconducting logic circuits operation is the superconductivity effect, the quantization of magnetic flux and the Josephson effects. The first one enables ballistic signal transfer not limited by power necessary to charge capacitance of interconnect lines. It provides the biggest advantage in energy efficiency in comparison to conventional CMOS technology. Indeed, superconducting microstrip lines are able to transfer picosecond waveforms without distortions with speed approaching the speed of light, for distances well exceeding typical chip size, and with low crosstalk. This is the basis for fast long-range interactions in superconducting circuits.

Note that absence of resistance (R = 0) leads to absence of voltage (V = 0) in a superconducting circuit in stationary state. Superconducting current flow corresponds not to electrical potentials difference (the voltage $V = \delta \phi$) but to difference of superconducting order parameter phases $\delta \theta$, accordingly. Superconducting order parameter corresponds to superconducting electrons wave function $|\psi|e^{i\theta}$ in Ginzburg – Landau theory. Magnetic flux $\Phi$ in a superconducting loop of inductance $L$ provides an increase of superconducting phase along the loop and results in permanent circulating current $I = \Phi / L$. This ratio is analogous to Ohm’s law $I = V/R$. It allows to write linear Kirchhoff equations for superconducting circuits.

The quantization of magnetic flux introduces fundamental difference between CMOS and superconducting circuits operation. It follows from uniqueness of superconducting electrons wave function. Indeed, increase of superconducting phase along a loop corresponds to magnetic flux as $\Phi = (\Phi_0/2\pi) \oint \nabla \theta \, dl$ (where $\Phi_0 = h/2e \approx 2 \times 10^{-15}$ Wb is the magnetic flux quantum, $h$ is the Planck constant, and $e$ is the electron charge). Fulfillment of this relation is possible if $\oint \nabla \theta \, dl = 2\pi n$ (where $n$ is integer) and therefore $\Phi = n\Phi_0$. Magnetic flux in a superconducting loop can take only values multiple to the flux quantum, accordingly.

Physical representation of information is typically based on the quantization of magnetic flux. For example, presence or absence of SFQ in a superconducting loop can be considered as a logical unity “1” or zero “0”. Note that information is physically localized due to such representation. This is a fundamental difference compared to information representation in semiconductor circuits. The localization leads to deep analogy between superconducting logic cells and von Neuman cellular automata where short-range interactions are predominant.

The nonlinear element in superconducting circuits is the Josephson junction. It is a weak link between two superconductors, e.g., the most used superconductor–isolerator-superconductor (SIS) sandwich. One of the most important Josephson junction parameters is its critical current, $I_c$. This is the maximum superconducting current capable of flowing through the junction. Josephson junction can be switched from superconducting to resistive state by increasing the current above $I_c$. Transition to resistive state allows to change magnetic flux in a superconducting loop, and hence to perform a digital logic operation.

Dynamics of SIS junction is commonly described in the frame of the resistively shunted junction model with capacitance (RSJC). This model presents Josephson junction as a parallel connection of the junction itself transmitting superconducting current, $I_s$, only, a resistor and a capacitor with corresponding currents, $I_r = \frac{V}{R}$ and $I_{cap} = C \frac{\partial V}{\partial t}$, where $t$ is time. The total current through the junction is the sum, $I = I_s + I_r + I_{cap}$. This model is based on DC and AC Josephson effects which determine the superconducting current $I_s$ and voltage $V$.

The DC Josephson effect describes the superconducting current-phase relation (CPR). For SIS junction it is $I_s = I_c \sin \varphi$, where $\varphi = \Phi / \Phi_0$ is the superconducting order parameter phase difference across the Josephson junction. It is called the Josephson phase. By presenting the relation between superconducting order parameter phase and magnetic flux as $\varphi = 2\pi \Phi / \Phi_0$, we note that CPR couples current with the magnetic flux in a super-
conducting loop. Josephson junction acts as a nonlinear inductance in the circuits, accordingly.

The AC Josephson effect binds the voltage on Josephson junction in resistive state with the superconducting phase evolution as $V = (\Phi_0/2\pi)\partial\varphi/\partial t$. According to this relation, increase of the Josephson phase in $2\pi$ is accompanied by appearance of the voltage pulse across the junction such that $\int Vdt = \Phi_0$. Therefore, a single switching of the Josephson junction into resistive state corresponds to transmission of SFQ pulse through the junction. The energy dissipated in the switching process is $E_J \approx I_c\Phi_0 = 2 \times 10^{-19}$ J, taking typical $I_c \approx 0.1$ mA. The typical critical current value is conditioned by working (liquid helium) temperature, $T = 4.2$ K. For proper circuits operation it should be about three orders higher than the effective noise current value, $I_T = (2\pi/\Phi_0)k_BT \approx 0.18$ $\mu$A, where $k_B$ is the Boltzmann constant.

Characteristic frequency of the Josephson junction switching process is determined by Josephson junction parameters, $\omega_c = (2\pi/\Phi_0)I_cR_n$, where $I_cR_n$ product is the Josephson junction characteristic voltage, and $R_n$ is the junction resistance in the normal state. Since SIS junctions possess large capacitance, they are usually shunted by external resistors to avoid LC-resonances. The resistance $R_n$ is approximately equal to resistance of the shunt $R_s \approx R_n$ because $R_s$ is much smaller than own tunnel junction resistance. For Nb-based junctions the characteristic frequency is of the order of $\omega_c/2\pi \sim 100 - 350$ GHz (the characteristic voltage is at the level of $0.2 - 0.7$ mV). Superconducting digital circuits are predominantly based on tunnel junctions because of high accuracy of their fabrication process and high characteristic frequencies.

By expressing the currents $I_c$, $I_r$ and $I_{cap}$ of RSJC model through the Josephson phase $\varphi$, we can present the total current flowing through the junction in the following form:

$$I/I_c = \sin \varphi + \omega_c^{-1}\varphi + (\beta_c\omega_c^{-2}\varphi, (1)$$

where $\beta_c = \omega_c R_n C$ is the Stewart-McCumber parameter reflecting capacitance impact, and dot denotes time differentiation. This Equation 1 is quite analogous to the one for mechanical pendulum with the moment of inertia $\beta_c/\omega_c^2$ (capacitance here is analogous to mass), the viscosity factor $1/\omega_c$ (resistance determines damping), and the applied torque $I/I_c$. This simple analogy allows to consider superconducting digital circuit as a net of coupled pendulums.

Pendulum $2\pi$ rotation is accompanied by subsequent oscillations around stable equilibrium point (Figure 1). In Josephson junction dynamics they are called “plasma oscillations”. Plasma oscillations frequency is $\omega_p = \omega_c/\sqrt{\beta_c} = \sqrt{2\pi I_c/\Phi_0 C}$. For proper logic cell operation these oscillations should vanish before subsequent Josephson junction switching. Compliance with this requirement can be achieved with $\beta_c \approx 1$, $\omega_p \approx \omega_c$.

Clock frequency is accordingly less than $\omega_c$, and is under 100 GHz in practical circuits.

Complexity of a superconducting circuit realizable on a chip is determined by Josephson junction dimensions. Area of Josephson junction is closely related to its critical current density, $j_c$. This parameter is one of the most important in the standard Nb-based tunnel junction fabrication process. It is fixed by material properties of insulating interlayer Al$_2$O$_3$ between superconducting Nb electrodes, and its thickness $d \approx 1$ nm. The critical current density value lies typically in the range $j_c = 10 - 100$ $\mu$A/$\mu$m$^2$. The corresponding Josephson junction specific capacitance is $c \approx 40 - 60$ F/$\mu$m$^2$. Variation in Josephson junction critical current, $I_c = a j_c$, is obtained by variation of its area, $a$. It is accompanied by variation of Josephson junction capacitance, $C = ac$. The shunt resistance is adjusted in accordance with the mentioned condition, $\beta_c = 1$, as $R_n = \Phi_0/2\pi j_c c/a$. Its area is defined by Josephson junction area $a$, minimum wiring feature size ($0.5 - 1$ $\mu$m), and sheet resistance of used material (2 - 6 $\Omega$ per square for Mo or MoN$\text{$_x$}$ ($\mu$m$^2$).

While own Josephson junction weak link area is typically $a \sim 1$ $\mu$m$^2$ for $j_c = 100$ $\mu$A/$\mu$m$^2$, its total area with the shunt is by an order lager. Corresponding Josephson junctions available density on a chip is $10^7$/cm$^2$. Superconducting circuit complexity becomes limited to 2.5 million junctions per 1 cm$^2$ nowadays under assumption that only a quarter of chip area can be occupied by Josephson junctions (with taking interconnects into account). The circuit can be further expanded using multi-chip module (MCM) technology.

B. Digital SFQ logics

1. SFQ circuit basic principles of operation

Data processing in SFQ circuits can be discussed on an example of RSFQ cells operation. RSFQ data bus is shown in Figure 2. It is a parallel array of superconducting loops composed of Josephson junctions (shown by crosses) and superconducting inductances. This struc-
ture is called the Josephson transmission line (JTL). SFQ can be transferred along this JTL by successive switchings of Josephson junctions. The switching is obtained by summing the SFQ circulating current and the applied bias current $I_b$. Josephson junction transition into resistive state leads to SFQ circulating current redistribution toward the next junction. The redistribution process ends by the next junction switching and successive returning of the current junction into the superconducting state.

This example shows the basic principle of SFQ logic cells operation. It reduces to summation of currents, which are SFQs currents and bias currents. This summation leads (or not leads) to successive Josephson junction switching resulting in reproduction (or not reproduction) of SFQ. In RSFQ convention arrival of an SFQ pulse during clock period to a logic cell has a meaning of binary “1”, while absence of the one means “0”.

Figure 3 illustrates an example of clocked readout of information from a RSFQ logic cell. Clocking is performed by means of SFQs application to the cell. Upper JTL in Figure 3 serves for SFQ clock distribution. SFQs are allotted to the cell through extra branch coupled to the JTL as shown. Note that Josephson junction clones SFQ at the branch point. Readout operation is performed by a couple of junctions marked by dotted rectangle. This couple is commonly called the decision making pair. Existence (or absence) of an SFQ circulating current in the logic cell loop makes the lower junction to be closer (or father) to its critical current compared to the upper junction. Clocking SFQ switches the lower (or upper) junction, correspondingly. SFQ reproduction by the lower junction means logical “1” to the output, while SFQ absence from the ones means logical “0”.

One can note a couple of typical SFQ circuits features from the presented example. Considered logic cell acts as a finite state machine. Its output depends on a history of its input. This particular cell operates as a widely used D flip-flop (“D” means “data” or “delay”) – the basis of shift registers. Note that its realization is much simpler than the one of semiconductor counterparts. RSFQ basic cells are such flip-flops, and therefore RSFQ is sequential logic. This is in contrast with semiconductor logic which is combinational one (where logic cell output is a function of its present input only).

Since only one clocked operation is performed during a clock period (some operations can be performed asynchronously), a processing stage in RSFQ circuits is reduced to a few logic cells. This is also completely opposite to conventional semiconductor circuits.

2. RSFQ logic

RSFQ logic dominates in superconductor digital technology since 1990-s years. Many digital and mixed signal devices like analog-to-digital converters, digital signal and data processors were realized on its basis.

Unfortunately, energy efficiency did not matter in the days of RSFQ development. High clock frequency was thought to be the major RSFQ advantage in the beginning. Extremely fast RSFQ-based digital frequency divider (T flip-flop) was presented just about a decade later RSFQ invention. Its clock frequency was as high as 770 GHz. It is still among fastest ever digital circuits.

The first RSFQ basic cells were the superconducting loops with two Josephson junctions (commonly known as the superconducting quantum interference devices - SQUIDs). These cells were connected by resistors (so “R” was for “resistive” in the abbreviation). Power supply bus coupling was also resistive. While resistors connecting the cells were rather quickly substituted for superconducting inductances and Josephson junction, the ones in feed lines remained until recent years, see Figure 4. They determined stationary energy dissipation, $P_S = I_b V_b$, where $I_b$ and $V_b$ are the DC bias current and according voltage. The bias current is typically $I_b \approx 0.75 I_c$. The bias voltage had to be an order higher than the Josephson junction characteristic voltage, $V_b \sim 10 \times I_c R_n$, to prevent the bias current redistribution. This requirement determined the bias resistors values. Typical RSFQ cell stationary power dissipation is $P_S \sim 800 \, \text{nW}$.

Another mechanism providing power dissipation corresponds to Josephson junction switching. This dynamic
power dissipation is defined as $P_D = I_b \Phi_0 f$, where $f$ is the clock frequency. For a typical clock frequency of 20 GHz $P_D$ is at the level of $\sim 13$ nW. It is seen that the dynamic power dissipation is about 60 times less than the stationary one. Main efforts to increase RSFQ circuits energy efficiency were aimed at stationary energy dissipation decrease, accordingly. RSFQ energy efficient successors, LV-RSFQ, ERSFQ and eSFQ, are presented below.

3. **LV-RSFQ**

The first step toward $P_S$ reduction was the bias voltage decrease. Bias current redistribution between neighboring cells in low-voltage RSFQ (LV-RSFQ) is damped by introduction of inductances connected in series with bias resistors in feed lines \[31–35\].

Unfortunately, this approach limits clock frequency. Indeed, clock frequency increase is accompanied by increase of average voltage $V_{\text{ac}}$ across a cell (according to the AC Josephson effect). This in turn leads to bias current decrease proportional to $V_{\text{ac}}$. The latter finally results in the cell malfunction \[36]. This tradeoff with requirement of additional circuit area for inductances in feed lines practically limit application of this approach. Since static power dissipation is not eliminated, this is somewhat half-hearted solution. It was succeeded by another two RSFQ versions (ERSFQ and eSFQ, where “E/e” stays for “energy efficient”) where $P_S$ is totally zero.

4. **ERSFQ**

ERSFQ \[37\] is the next logical step after LV-RSFQ. Resistors in feed lines are substituted for Josephson junctions limiting bias current variation in this logic, see Figure 5. This replacement is somewhat analogous to the one which was done for resistors connecting SQUID cells in the very first RSFQ circuits. It provides possibility for the circuits to be in pure superconducting state.

Main difficulty in the bias resistors elimination is formation of superconducting loops between logic cells. Generally, logic cells are switched asynchronously depending on processing data. Average voltage and total Josephson phase increment are different across them. This results in emergence of currents circulating through neighbor cells. Being added to bias current, these currents prevent correct operation of the circuits.

Imbalance of Josephson phase increment is automatically compensated by corresponding switchings of Josephson junctions placed in ERSFQ feed lines. Since these switchings are not synchronized with clock, some immediate alteration of bias current is still possible. This alteration $\Delta I \sim \Phi_0 / L_b$ is limited by inductance $L_b$ connected in series with Josephson junction in the feed line. While large value of this inductance $L_b$ minimizes the bias current variation, its large geometric size increases the circuit area (similar to LV-RSFQ). Possible solutions of this problem are an increase of wiring layers number, and utilization of superconducting materials having high kinetic inductance. These materials can be also used for further miniaturization of logic cells themselves \[20\].

5. **eSFQ**

Another energy efficient logic of RSFQ family is eSFQ \[11,38–40\]. The main idea here is the “synchronous phase balancing”. Bias current is applied to decision making pair, see Figure 6. One Josephson junction of this pair is always switched during a clock cycle regardless data content. Therefore, average voltage and Josephson phase increment are always equal across any such pair. This prevents the emergence of parasitic circulating currents. Josephson junction in the feed line is required only for proper phase balance adjustment during power-up procedure. “It is not expected to switch during regular circuit operation” \[11\].

Achieved phase balance allows to eliminate large inductances from ERSFQ feed lines, and so eSFQ circuits occupy nearly the same area as RSFQ ones. One should note that despite of the “synchronous” nature of this logic, a method for design of eSFQ-based asynchronous circuits was proposed \[49\] making it suitable for wave-pipelined architecture.

Since RSFQ library was designed regardless synchronous phase balancing, transition to eSFQ requires its...
correction. In some cases it leads to increase of Josephson junctions number. For example, JTL should be replaced by a shift register \[^{31}\] or by “Wave JTL” \[^{32}\], or by one of its asynchronous counterparts: ballistic transmission line based on unshunted Josephson junctions \[^{33,34}\] or passive microstrip line.

Similarity of ERSFQ and eSFQ approaches allows to make an overall assessment of total increase in Josephson junctions number up to 33 – 40% compared to RSFQ circuits \[^{11}\]. Inheritance of basic cells design of RSFQ by ERSFQ makes it easier to use.

6. RSFQ logic family common features

Clock is effectively a part of data in ERSFQ circuits. This means that they are globally asynchronous.

Since clock frequency is determined by repetition rate of SFQs in clocking JTL, it can be adjusted “in flight” by logic cells according to processing data.

The bias voltage source can be implemented as a JTL fed by a constant bias current, for which the input signal is the SFQ clock applied from an on-chip SFQ clock generator, see Figure 7. Average voltage on this JTL is precisely proportional to the clock frequency, \( V_b = \Phi_0 f \), according to the AC Josephson effect. Clock control by logic cells allows to adjust this voltage or even to turn it off. The last option corresponds to circuits switching into “sleep mode” where power dissipation is totally zero. Realization of this power save mechanism at individual circuits level is possible with circuits partitioning into series connection of islands with equal bias current but different bias voltage \[^{44}\].

Since logic cells are fed in parallel in RSFQ logic family, total bias current increases proportional to Josephson junctions number. For 1 million Josephson junctions the bias current value could be unreasonably high \( I_b \approx 100 \text{ A} \). Circuits partitioning allows to keep it at acceptable level \[^{15}\] below 3 A.

7. RQL

RQL was proposed in about 2008. It was developed as an alternative to conventional RSFQ, and presented as “ultra-low-power superconductor logic” \[^{46}\]. Main difference between RQL and RSFQ is in the way of power supply \[^{47}\]. While in RSFQ it is a DC power applied to Josephson junctions in parallel through bias resistors (Figure 4), in RQL it is an AC power applied in series through bias transformers, see Figure 8.

The proposed power supply scheme possesses some advantages. (i) No DC bias current and no bias resistors means zero static power dissipation inside cryogenic cooler. Bias current is terminated off chip at room temperature. (ii) The well known RSFQ circuits design problem is the large return bias current magnetic field affecting logic cells. It is recommended \[^{45}\] to keep maximum bias current below 100 mA in RSFQ feed line. This return current is completely absent in RQL due to the mentioned off-chip bias current termination. (iii) Serial bias supply allows to keep bias current amplitude at fairly low level \( I_b \approx 1 \text{ mA} \) regardless number of Josephson junctions on a chip. There is no need for the large-scale circuit partitioning. (iv) Bias current plays a role of clock signal. There is no need for SFQ clock distribution network. (v) Clock is not affected by thermal noise.

Logical unity (zero) is presented by a pair of SFQs having opposite magnetic flux directions (or lack thereof) in RQL circuits. These SFQs can be transferred in one direction with application of inversely directed bias currents, see Figure 9. The SFQs are placed in positive/negative AC current wave half period, accordingly. Unfortunately, one AC bias current is insufficient for directional propagation of the SFQs. It can provide only periodic space oscillations of the flux quanta. RQL uses two AC bias currents with \( \pi/2 \) phase shift. RQL cells are coupled to these two feed lines in rotation (Figure 9). Such coupling produces space division of total bias cur-
operate at frequency of 50 GHz. Moreover, implementation of 8-bit carry-look-ahead adder they cover area \( \sim 5 \times 10^{-13} \) cm² requiring high-frequency power splitters. These splitters often occupy quite a large area. For example, in implementation of 8-bit carry-look-ahead adder they cover area \( \sim 2.5 \) times larger than the adder itself. One can note that power supply through transformers also limits the possibility for the circuits miniaturization.

Multiphase AC bias presents known difficulty for high-frequency design (clock skew etc.). This practically limits clock frequency to 10 GHz, while RSFQ circuits routinely operate at frequency of 50 GHz. Moreover, implementation of MCM technology becomes complicated with RQL due to possible asynchronization of chips or clock phase shift. Besides inconvenience presented by high-frequency clock supply from off-chip external source, clocking by AC bias currents eliminates possibility of clock control by logic cells. Corresponding power save mechanisms cannot be realized in RQL. In addition, one should mention RF losses in microstrip resonators which typically make up to 50% total power budget even at relatively low frequencies.

Total power dissipation of RQL and ER SFQ circuits in active mode seems similar. Static power dissipation is absent. Dynamic power dissipation is associated with Josephson junction switching in data propagation process. In RQL circuits Josephson junction is doubly switched for logical unity transfer and zero times for transfer of logical zero. In ER SFQ both unity and zero are transferred with switching of one of the Josephson junctions in decision making pair. By assuming equal number of zeros and ones in data, one comes to roughly equal estimation for energy dissipation in both RQL and ER SFQ logic. More detailed analysis shows that only adiabatic switching of logic cells improves superconducting circuits energy efficiency markedly.

C. Adiabatic superconductor logic

Considered variants of superconductor logics have been proposed for non-adiabatic irreversible computation. Logical states are separated here by energy barrier \( E_w \geq 4 \times 10^{-19} \) J ensuring proper circuit operation. Note that the energy barrier in semiconductor circuits is only two to three orders higher, \( E_w \geq 10^9 \) J. Minimal energy barrier corresponds to Landauer’s “thermodynamic limit” \( E_{\text{min}} = k_B T \ln 2 \). In this limit logic states distinguishability becomes completely lost due to thermal fluctuations.

Energy required to perform a non-adiabatic logic operation can be estimated as the energy of transition between logical states corresponding to \( E_w \). In considered superconductor logics it is the energy of Josephson junction switching, \( E_J \approx 2 \times 10^{-19} \) J. While presuming logical irreversibility, this energy can be lowered down to \( E_{\text{min}} \approx 4 \times 10^{-23} \) J (at \( T = 4.2 \) K) by using adiabatic switching process. Note that Landauer limit \( E_{\text{min}} \) in this context reflects computing system entropy change associated with an irreversible operation. At the same time, there is no such limit for physically and logically reversible process. Therefore, energy dissipated per logical operation can approach zero in adiabatic reversible circuits.

The first ever practical reversible logic gates were realized recently on a basis of adiabatic superconductor logic. History of ASL development have begun even before RSFQ invention with proposition of “parametric quantum” in 1976. This cell itself was proposed even earlier in 1954 as “rf parametron” though for different
operating regime.

It is interesting to note that the manner of parametric quantron cell operation was implemented later in a single-electron device\cite{16,24,53} in 1996. The “single-electron parametron” operation was in fact quite similar to the ones of quantum-dot cellular automata (QCA) which were proposed for computation those years\cite{24,53}.

1. **ASL circuit basic principles of operation**

   Parametric quantron is a superconducting loop with single Josephson junction shown in Figure 10 leftward. Its state is conditioned by external magnetic flux, $\Phi_e$, and current, $I_e$, controlling Josephson junction critical current $I_c$. $L$ is the loop inductance. In practice, single Josephson junction is substituted by SQUID controlled by activation current $I_{act}$. $I_{in}/I_{out}$ are input/output currents.

   \[ I_c(I_e) \]

   \[ \Phi_e \]

   \[ L \]

   \[ \Rightarrow \]

   \[ I_{act}(I_e) \]

   \[ L \]

   \[ I_{in}/I_{out} \]

   \[ \Phi_e \]

   FIG. 10: Parametric quantron notional (left) and practical (right) schematic. The cell state is conditioned by bias flux $\Phi_e$ and current $I_e$ controlling Josephson junction critical current $I_c$. $L$ is the loop inductance. In practice, single Josephson junction is substituted by SQUID controlled by activation current $I_{act}$. $I_{in}/I_{out}$ are input/output currents.

   \[ \Phi_e = \pi, \quad l = \pi \]

   \[ \Phi_e = 4, \quad l = 0.5 \]

   \[ 2 \pi U_{PQ} \]

   \[ \Phi_e \]

   \[ I_e \]

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tivation SQUID and main parametric quantron loop, it was noted that the roles of the activation and the input/output can be swapped.\textsuperscript{57}

Unfortunately, already the first designs in mid 1980-s of physically and logically reversible parametric quantron based processor\textsuperscript{59} showed this approach to be impractical. The reason for such conclusion was as follows. Logical reversibility can be achieved by temporary storage of all intermediate results.\textsuperscript{55} Together with predominance of short-range interactions this produces severe hardware overhead. Indeed, realization of 8-bit 1024-points fast convolver required almost $10^7$ parametric quantrons.\textsuperscript{59}

About 90% of them were operated just as elements of shift registers, transferring data through the processor.\textsuperscript{59} It was noted that such circuits are also featured by low speed (in comparison to RSFQ) and low tolerance to parameters variations.\textsuperscript{24}

2. Quantum flux parameton based circuits

Few years later the works on reversible circuits, the same principles of operation were utilized for development of generally non-reversible Josephson supercomputer. In this effort parametric quantron was renamed as “quantum flux parameton” (QFP).\textsuperscript{59} The major problem of QFP-based circuits was high-frequency multi-phase AC power supply (which was later borrowed by RQl). While there were different approaches elaborated for its solution,\textsuperscript{27,59} finally multi-phase AC biasing was recognized to be intractable obstacle for implementation of complex high-clock-frequency practical circuits and QFP-based approach was abandoned for some years.

Renewed interest to ASL was introduced by development of superconductor quantum computer. QFPs are utilized as qubits and couplers in adiabatic quantum optimization systems of D-Wave Systems.\textsuperscript{60,61} Another reason for the current rise of interest to ASL is Japan JST-ALCA project “Superconductor electronics system combined with optics and spintronics”.\textsuperscript{59} The idea of the project is the development of energy efficient supercomputer based on synergy of the technologies. Superconductor processor of the computing system is planned to be based on QFPs operated in adiabatic regime. The processor prototype has 8-bit simplified RISC architecture and is featured by ~25 thousand Josephson junctions and ~10 instructions. In this context, adiabatic operation of QFP was investigated in order to reduce its dynamic energy consumption down to the fundamental limit.\textsuperscript{63} Adiabatic QFP was abbreviated as AQFP in these works.\textsuperscript{50,52,63}

AQFP-based circuits were tested experimentally\textsuperscript{61} at 5 GHz clock frequency showing energy dissipation at the level of $10^{-20}$ J. Theoretical analysis reveals that AQFP can be operated with energy dissipation less than the thermodynamic limit.\textsuperscript{62} Product of energy dissipated per clock cycle on a cycle time could approach the quantum limit\textsuperscript{65} at 4.2 K cooling temperature, with utilization of standard manufacturing processes.\textsuperscript{59} Comparison of AQFP-based design with design based on CMOS FPGA, on example of implementation of Collatz algorithm, showed that the first one is about seven orders of magnitude superior to its counterpart in energy efficiency, even including the power of cryogenic cooling.\textsuperscript{13}

AQFP-based logic cells can be implemented by combining only four building blocks: buffer, NOT, constant, and branch. Together with AQFP latch\textsuperscript{59} these blocks enable design of adiabatic circuit of arbitrary complexity. Recently, 10 thousand gate-scale AQFP circuit was reported.\textsuperscript{26}

Magnetic coupling of AQFP gates is performed via transformers. Current flowing through the transformer wire cannot be too small because it ought to provide appropriate bias flux to subsequent cell despite of possible technological spread of AQFP parameters. This limits maximum wire length to about 1 mm.\textsuperscript{62} This length is further conditioned by trade-off with maximum clock frequency, which is limited to 5 GHz in practical circuits.\textsuperscript{50,52,55} This clock frequency limitation relaxes complexity of AC bias lines design. However, with circuit scale increase, lengthy distribution of clock lines is nonetheless expected to generate a clock skew between logic cell.\textsuperscript{13}

While adiabatic circuits are clearly the most energy efficient ones, their operation frequency is relatively low and the latency is relatively large. However, recently it was shown that due to intrinsic periodicity of AQFP potential energy, the cell can be operated at double or even quadruple activation current frequency with an increase of the current amplitude\textsuperscript{71}. This opens opportunity to speed up AQFP circuits up to 10 GHz or even 20 GHz clock.

3. nSQUID-based circuits

Above, we already mentioned that it is possible to swap the roles of activation current and input/output in the parametric quantron. In this case, information is represented in magnetic flux of the SQUID, while its bias current flowing through the main parametric quantron loop plays the role of excitation.

It was noted that while the SQUIDs of different such cells may be coupled magnetically, their activation current pulse can be provided sequentially using a common bias bus. For better control of the SQUID state in this scheme the value of the main parametric quantron loop inductance should be minimized. In addition, it was proposed to provide negative mutual inductance between the two parts of the SQUID loop inductance.\textsuperscript{24} SQUID with negative mutual inductance is called “nSQUID”. Its inductance is effectively decreased for the bias current but increased for the current circulating in its loop.

Successive application of activation current pulse to nSQUIDs from a common bias bus can be realized by using an SFC.\textsuperscript{24,63} Note that nSQUID-based transmis-
transmitting quantum information by using AC-to-DC converter. Power supply of different parts of large scale DC biased circuit by such voltage sources could eliminate the need for the circuit partitioning.

In general, SFQ AC biased circuits are good in design of large regular structures. The largest superconductor digital circuit is AC biased shift register containing 809 thousand Josephson junctions. It was used as a fabrication process benchmark circuit like a kind of “scan chain”.

DC power source is most convenient in terms of providing the power into the cryogenic system. Indeed, the bandwidth of microwave cables is often narrow to prevent hit inflow. In order to overcome the limitation on the maximum frequency of AC biased circuits it was proposed to use a DC-to-AC converter as on-chip power source. This converter was successfully tested in experiment providing oscillation frequency of 4.4 GHz. The output AC bias current amplitude can be tuned by varying DC bias current of the convertor. Utilization of AC-to-DC and DC-to-AC converters allows to use circuits based on different logics on a single chip, increasing the variability of design.

Physical localization of information corresponding to quantization of magnetic flux leads to another issue, especially in digital SFQ circuits. Due to low gain from Josephson junctions, the circuits are featured by low fan-out. An SFQ has to propagate through large and slow SFQ splitter tree to split information into multiple branches. The same situation is with merging of multiple outputs.

Solution of this problem can be found in utilization of magnetic control over cells by using current control line. This approach can be realized with SFQ-to-current loop converters. Similar technique can be used in merging of multiple outputs.

SFQ-to-current conversion can be realized also by Superconducting-Ferromagnetic Transistor (SFT) or by “non-Josephson” device like n-Tron. The former is the three (or four) terminal device comprising two stacked Josephson junctions. One of them, “injector”, (containing ferromagnetic layer(s)) serves for injection of spin-polarized electrons in common superconducting electrode of both junctions, thus suppressing its superconductivity. This manifests itself as redistribution of superconducting current flowing through this electrode or as degradation of “acceptor” (typically SIS junction) critical current depending on configuration of the device. While having good input/output isolation, SFT is capable of providing voltage, current, and power amplification.

n-Tron is the three terminal device comprising superconducting strip with a narrow in the middle to which the third terminal tip is connected. Current pulse from the third terminal switch off superconductivity of the nanowire, that is similar to SFT operation to some extent. Unlike Josephson junction, the nanowire in resistive state possesses several $kT$ resistance which provide high output impedance and high voltage signal. Both de-
vices can be utilized as an interface between superconductor circuit and CMOS electronics or memory depending on requirements to output signal and energy efficiency.

It is well known that the major computation time and power consumption is associated with communications between logic and memory circuitry. Logic cells possessing feature of internal memory are now being considered as possible element base for development of new, more efficient computer. Superconductor logic circuits utilizing their internal memory were named “MAGIC” (Memory And LoGIC) circuits. This concept is based on conventional ERSFQ cells involving their renaming or rewiring. It promises an increase in clock rate to above 100 GHz threshold, combined with up to ten-fold gain in functional density. In general, the mentioned quantum localization of information and high non-linearity of Josephson junctions make superconductor circuits to be ideally suit for implementation of unconventional computational paradigms like cellular automata, artificial neural networks or quantum computing.

Unfortunately, the major problem of superconductor circuits does not relate to a particular logic of computation. Low integration density in all cases limits complexity, and therefore performance of modern digital superconductor device. Possible solutions here are miniaturization of existing element base and increase of its functionality.

The first one can be performed by scaling down the SIS Josephson junction or search for other high accuracy technological processes providing nanosized junctions with high critical current density and normal-state resistance. Another direction of the research is substitution of conventional loop inductance for kinetic inductance or inductance of Josephson junction. This also allows to make the circuits more energy efficient. Indeed, Josephson junction critical current \( I_c \) and loop inductance \( L \) are linked for SFQ circuits. Their product should be \( I_c L \approx \Phi_0 \) for proper operation. While the critical current \( I_c \) has to be decreased in order to improve the energy efficiency, \( E_j \approx I_c \Phi_0 \), this leads to increase in the inductance making the circuit to be sparse. Miniaturization of inductance weakens this problem. Unfortunately, transformer remains an inherent component of the circuits which can not be miniaturized in this way.

One should note that contrary to CMOS technology where transistor layer is implemented on a substrate, Josephson junctions can be fabricated at any layer. This provides opportunity for utilization of 3D architecture. With planned technological advances, the Josephson junction density up to \( 10^8/\text{cm}^2 \) seems achievable.

Finally, Josephson junctions with unconventional current-phase relation (CPR) can be utilized in a circuit for its miniaturization. For example, the so-called “\( \pi \)”-junction (the junction with constant \( \pi \) shift of its CPR) can be used as a “phase battery” providing constant phase shift instead of conventional transformer. Control of the junction CPR phase shift can provide the change in the logic cell functioning, e.g., converting AND to OR. This mechanism can be also used for implementation of memory cell.

Historically, the problem of element base miniaturization was first recognized in development of superconductor random access memory (RAM). Since that time, the need for dense cryogenic RAM is the major stimulus for innovative research in this area.

II. MEMORY

Among the many attempts to create a cryogenic memory compatible with energy-efficient superconducting electronics, we want to single out the four most productive competing directions: (A) SQUID-based memory, (B) hybrid Josephson-CMOS memory, (C) JMRAM and (D) OST-MRAM.

A. SQUID-based memory

The presence or absence of SFQ(s) in a superconducting loop can be the physical basis for a digital memory element. Due to high characteristic frequency of Josephson junction, SQUID-based memory cells stand out with fast (few picoseconds) write/read time favorable for RAM which is indispensable for data processor. Throughout various SQUID-based RAM realizations memory element was provided with destructive or non-destructive readout. Memory cell contained according from two to ten Josephson junctions. With Josephson junction micron-scale dimensions in the late 1990-s this resulted in memory cell area of an order of few hundreds of microns squared. While power dissipation per write/read operations was at \( \mu \text{W} \) level, memory chip capacity was only up to 4 kb. In the particular 4 kb RAM memory the memory drivers and sensing circuits required \( \text{AC power which limited its clock frequency to } 620 \text{ MHz. Later, all-DC-powered high-speed SFQ RAM based on pipeline structure for memory cell arrays was proposed. Estimation showed that this approach allows up to 1 Mb memory on } 2 \times 2 \text{ cm}^2 \text{ chip operated at } 10 \text{ GHz clock frequency and featuring } 12 \text{ mW power dissipation. Still, it was never realized in experiment.}

B. Hybrid Josephson-CMOS memory

Low integration density of SQUID-based memory cells seemed to be significant obstacle to the development of low-temperature RAM with reasonable capacity. This approach was succeeded by hybrid Josephson-CMOS RAM where Josephson interface circuits were amended by CMOS memory chip. This combination allowed to develop 64 kb, 4 K temperature RAM with 400 ps read
time, and 21/12 mW power dissipation for write/read operations, accordingly.\textsuperscript{124} CMOS memory cell was composed of 8 transistors. While being fabricated in a 65 nm CMOS process, the cell size was about three orders of magnitude less than the one of its SQUID-based counterparts. Main challenge in design of this memory system was amplification of sub-nV superconductor logic signal up to the $\sim 1$ V level required by CMOS circuits. This task was accomplished in two stages. First, the signal was amplified to 60 mV using a Suzuki stack, which can be thought as a SQUID with each Josephson junction substituted by a series array of junctions for high total resistance.\textsuperscript{124} At the second step, the reached 60 mV signal drives high sensitive CMOS comparator to produce the volt output level.

Suzuki stack\textsuperscript{122} and CMOS comparator\textsuperscript{125} were optimized for best compromise of power and time performance. Their simulated power $\times$ delay product for read operation were 2.3 mW $\times$ 47 ps (0.11 pJ) and 6.4 mW $\times$ 167 ps (1.1 pJ). This made up 73% and 53% of total memory system read power and time delay, correspondingly. These results exhibit severe restriction of overall system performance by the interface circuits. Recently, it was shown that the power consumption can be significantly decreased with utilization of energy efficient ERSFQ decoders and n-Trons as high voltage drivers.\textsuperscript{129} This could provide the energy efficiency improvement up to 3 times for 64 kb, and up to 12 times for 16 Mb memory. In the latter case, the access time in a read operation is estimated to be 0.78 ns.

While the hybrid memory approach showed better memory capacity, its power consumption and time requirements are still prohibitive. It was summarized that for implementation of practical low-temperature RAM one should meet the following criteria: (i) scale: memory element dimension $< 100$ nm ($< 200$ nm pitch); (ii) write operation: $10^{-18}$ J energy with $\sim 50 – 100$ ps time delay per cell; (iii) read operation: $10^{-19}$ J energy with $\sim 5$ ps time delay per cell. An idea to meet the requirements nowadays is to bring spintronics (including superconductor spintronics) in RAM design.

\subsection{C. JMRAM}

It is possible to reduce drastically the size of superconducting memory cell by using controllable Josephson junction with magnetic interlayers instead of SQUID.\textsuperscript{122,127} Topology of such magnetic Josephson junction (MJJ) is usually of two types: (i) sandwich topology which is well suited for CMOS-compatible fabrication technology, and (ii) the one with some heterogeneity of the junction weak-link area in-plane of the layers. Below we present MJJ valves according to this classification.

\section{I. MJJ valve of sandwich topology}

Search for an optimal way of compact MJJ valve implementation remains under way now. The most obvious solution is to use two ferromagnetic layers with different magnetic rigidity in the area of the junction weak link.\textsuperscript{130,132} Critical current of such junction is determined by effects resulting from coexistence and competition of two orderings for electron spins: “superconducting” (S) (with usually antiparallel spins of electrons in the so-called “Cooper pairs”) and “ferromagnetic” (F) (with parallel ordering of electron spins). Magnetization reversal of “weak” F-layer leads to switching between collinear and anti-collinear orientations of the F-layers magnetic moments in the bilayer. This, in turn, provides alteration in the total effective exchange energy, $E_{ex}$, and hence, in MJJ critical current effective suppression. While magnetization reversal can be executed by application of an external magnetic field, the critical current can be read-out, e.g., with MJJ inclusion into decision making pair, see Figure 14. It is possible to trace some analogy between this effect and the phenomenon of giant magnetoresistance, which is actively used in conventional magnetic memory cells.

A common drawback of most MJJs is small value of their characteristic frequency ($\omega_c \sim I, R_n$) in comparison with SIS junction. Indeed, here one has to perform the magnetization reversal of weak F-layer with relatively small exchange energy in order to manipulate the total critical current against the background of its considerable suppression by the strong ferromagnet. Low $\omega_c$ outflows in slow read operation and complicates MJJ integration in SFQ logic circuits. There are several approaches to solve this problem. One of them is the use of noncollinearly magnetized ferromagnetic layers.\textsuperscript{130,132} In this case, the triplet superconducting correlations of electrons are formed in the junction weak-link area. A part of them are featured by collinear orientation of electron spins in Cooper pairs. They are unaffected by exchange field of the ferromagnets, thus increasing MJJ critical current while maintaining its normal state resistance. The “triplet” current can be controlled by external magnetic field through magnetization reversal.\textsuperscript{133} Still, this approach implies implemen-
tation of a number of additional layers (and interfaces) in the structure that reduces its critical current.

One should also note that $E_{\text{ex}}$ alteration could result in $\pi$ shift of MJJ CPR. In this case the valve can be utilized as controllable phase battery\textsuperscript{110}. Inclusion of such MJJ into SQUID loop allows fast read-out of its states\textsuperscript{110}. However, here miniaturization reduces only to replacement of the SQUID inductance by the MJJ.

Another approach is based on localization of magnetic field source outside Josephson junction weak-link area but in the nearest proximity\textsuperscript{111–119}. For example, F-bilayer can be placed on top of SIS junction. In this case, stray magnetic field penetrating into the junction area controls its critical current. If the junction S-layer neighboring the F-bilayer is thin enough, the coupling of the vector potential of the stray magnetic field to superconducting order parameter phase could also noticeably affect Josephson phase difference across SIS junction. SIS junction is utilized here just for read-out the ferromagnet state, and therefore, its characteristic frequency remains high. Still, since the strength of magnetic field is proportional to the ferromagnet volume, a possibility of miniaturization of such memory element is doubtful.

Critical current modulation can be obtained even in the structure with a single magnetic layer by changing the value of its residual magnetization\textsuperscript{115}. It is also possible to improve the characteristic frequency by the inclusion of dielectric (I) and thin superconducting (s) layers in MJJ weak-link area to increase $R_n$ and $I_c$, correspondingly\textsuperscript{118–120}. Such SIsFS valves possess characteristics close to SIS junction\textsuperscript{115}. However, compatibility with superconductors requires utilization of ferromagnets with relatively low coercive field, which are typically characterized by non-square shape of the hysteresis loop. This in turn outflows into uncertainty of MJJ critical current at zero applied magnetic field after multiple magnetization reversals. In addition, miniaturization here faces the same difficulties as in the previous approach. For these reasons, it seems especially fruitful to replace the I and F layers with two magnetic insulator IF-layers to construct a Josephson S(IF)s(IF)S valve\textsuperscript{157–159}. Its operation relies on variable suppression of superconductivity of the middle s-layer. Yet, this promising structure is complicated for fabrication.

2. MJJ valve with in-plane heterogeneity of the weak-link area

The second type of valves implies heterogeneity of the weak-link region in the junction plane providing separation of the structure into two parts. CPR of these parts can be different, e.g., the conventional CPR and the ones shifted in phase by $\pi$\textsuperscript{153,158}. Such MJJ may be thought as nanoSQUID with conventional and “$\pi$” lumped junctions. Its implementation may comprise a ferromagnetic interlayer and a sandwich containing the same F-layer and a normal metal (N) layer, see Figure 15.

If F-layer magnetization is aligned perpendicular to the nanoSQUID plane, it compensates the Josephson phase gradient across the MJJ making its critical current to be high. While the magnetization is being rotated at 90°, this effect is turned off and $I_c$ becomes low. Here for proper operation of this SF-NFS-based MJJ the flux of residual magnetization must be comparable with the flux quantum $\Phi_0$.

The second common problem of MJJ-based memory is a long time of write operation. Bit write is commonly performed by magnetization reversal of at least one of F-layers. For this reason, recording time is of an order of inverse frequency of ferromagnetic resonance. It is usually more than two orders of magnitude larger than the characteristic time of SIS junction switching. Thus, elimination of magnetization reversal from the valves operation is desired. It is worth noting that nano-sized trap for single Abrikosov vortex in the vicinity of Josephson junction\textsuperscript{161,162} allows to realize fast enough write operation. However, energy dissipation associated with annihilation of such vortex ($\sim 10^{-18}$ J) may contradict with the paradigm of energy-efficiency.

This challenge can be met with MJJ having bistable Josephson potential energy. Josephson phases of its ground states could be equal to $\pm \varphi$ ($0 < \varphi < \pi$). One can realize both write and read operations with such $\varphi$-junction on picosecond timescale\textsuperscript{163–169}. The disadvantage of this approach is the difficulties with $\varphi$-state implementation. In practice, it is possible only in the structure with heterogeneous weak-link region of a rather large size.

One more operation principle of MJJ valves relies on control of superconducting phase domains formation\textsuperscript{156}. The effect can be realized in SIsFS MJJ with sFS part substituted, e.g., for heterogeneous SF-NFS combination. The middle s-layer is broken on domains with different superconducting phases if Josephson phases of the structure parts are different, and vice versa. This process can be controlled by current injection through sFS or sFNS parts. The domain formation significantly changes the MJJ critical current. This MJJ provides fast read and write operations with no need for application of external magnetic field. Still, fabrication of compact Josephson junctions having the inhomogeneous weak-link region with reproducible characteristics is a difficult technolog-

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{figure15.png}
\caption{Cross section of SF-NFS MJJ with CPRs of its parts shifted in phase by $\pi$. Arrows show F-layer magnetization directions corresponding to the valve on/off states.}
\end{figure}
D. OST-MRAM

The next considered type of cryogenic memory is the hybrid approach combining superconducting control circuits with spintronics memory devices. Here due to spin-based interactions between atoms in the crystal lattice and electrons, orientations of ferromagnets magnetization can determine the amount of current flow. And vice versa, spin-polarized current can affect orientations of the magnetizations. The last effect is the so-called “spin transfer torque” (STT). It was suggested as a control mechanism for magnetic memory. However, high speed and low energy of write operation can not be provided with conventional spin-valve topology with collinear orientations of ferromagnets magnetizations.

Orthogonal spin transfer (OST) device allows to overcome the difficulties. This structure consists of an out-of-plane ferromagnetic polarizer (OPP), a free F-layer (FL), and a fixed F in-plane polarizer/analyzer (IPP), see Figure 16. “Write” current pulse passing through OPP provides STT effect in FL which acts to lift its magnetization out of plane. Magnetization is then rotated about the out-of-plane axis, according to Landau-Lifshitz-Gilbert equation. Current pulse applied to IPP read-out collinear or anti-collinear magnetizations of in-plane magnetized F-layers.

It is possible to obtain the necessary 180° magnetization reversal with correct selection of the write pulse amplitude and duration. Quasi-static and dynamic switching characteristics of OST devices have been analyzed at cryogenic temperatures: switching between parallel and anti-parallel spin-valve states has been demonstrated for ~ mA current pulses of sub-ns duration.

Clear advantages of the considered approach is elimination of control lines for magnetic field application, and implementation of fast magnetization reversal at sub-ns timescale. At the same time, the problems like relatively low percent of magnetoresistance, and the ones associated with possible magnetization over-rotation still prevent its practical application. The latter one can be overcome to some extend by involving both IPP and OPP polarizers into FL switching process.

One could note that application of STT effect in some of MJJ valves is of considerable interest. STT in voltage biased superconducting magnetic nanopillars (SFNFS and SFSFS junctions) has been studied for both equilibrium and nonequilibrium case. However, rich dynamics resulting from interplay of multiple Andreev reflection, spin mixing, spin filtering, spectral dynamics of the interface states, and the Josephson phase dynamics requires further research for evaluation of STT application appropriateness in superconducting memory structures.

E. Discussion

Lack of suitable cryogenic RAM is “… the main obstacle to the realization of high performance computer systems and signal processors based on superconducting electronics.” While JMRAM and OST-MRAM look as the most advanced approaches, they still require further improvement in a number of critically important areas.

Progress in considered variety of device types with no clear winner is impossible without researches on new magnetic materials like PdFe, NiFe(Nb,Cu,Mo), Co/Ru/Co, [Co/Ni]$_n$ etc., and novel magnetization reversal mechanisms. They can lead to development of new operation principles combining superconductivity and spintronics.

Inverse proximity effect at SF boundaries dictates utilization of pretty thin (at nm scale) magnetic layers. However, characteristics of memory devices typically depends exponentially on the F-layers thicknesses and significantly affected by interfacial roughness. This challenge can be met with further development of high-accuracy thin-film technological processes in modern fabrication technology.

Substantial part of circuit area, time delay and dissipated power in memory matrix is more likely to be associated with address lines rather than with memory cells. This makes optimization of intra-matrix interconnections and memory cell architecture of significant importance.

While we considered here only the most developed solutions for superconducting valves and memory elements, there are many other approaches to create nanosized controllable superconducting devices for applications in memory and logic. We can point out on our discretion: the nanoscale superconducting memory based on the kinetic inductance, and the superconducting quantum interference proximity transistors. Such concepts could bring novel idea into nanoscale design of superconducting circuits.

Conclusion

In conclusion, we discussed different superconductor logics providing fast (~ 5 − 50 GHz) and energy efficient (10$^{-19}$ − 10$^{-20}$ J per bit) operation of circuits in non-adiabatic and adiabatic regimes. The last one allows im-
plementation of the most energy efficient physically and logically reversible computations with no limit for minimum energy dissipation per logic operation. Possibilities to combine the schemes based on different logics as well as utilization of different (e.g., superconductor and semiconductor) technologies in a single device design are presented.

Considered physical principles underlying superconducting circuits operation provide possibility for development of devices based on unconventional computational paradigms. This could be the basis for a cryogenic cross-platform supercomputer, where each task can be executed in the most effective way. In our opinion, the development of superconducting circuits performing non-classical computations like cellular automata, artificial neural networks, adiabatic, reversible, and quantum non-classical computations like cellular automata, artificial neural networks, adiabatic, reversible, and quantum computing is indispensable to get all the benefits of the superconductor technology.

Low integration density, and hence low functional complexity of the devices, is identified as the major problem of the considered technology. This issue can be addressed with further miniaturization of basic elements and modernization of cell libraries, including introduction of novel devices like the ones based on nanowires or magnetic Josephson junctions.

The problem of low integration density is especially acute in RAM design. We considered here four different approaches to cryogenic RAM development with no clear winner. Progress in this area now implies elaboration of new operation principles based on synergy of different physical phenomena like superconductivity and magnetism, and appearance of novel effects, as for example, triplet spin valve memory effect or superconducting control of the magnetic state. Proposed concepts of new controllable devices could eventually change the face of superconductor technology making it universal platform of future high-performance computing.

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1. “Intel Puts the Brakes on Moore’s Law” by Tom Simonite at MIT Tech. Review, 23 March 2016. https://www.technologyreview.com/s/601102/intel-puts-the-brakes-on-moores-law/ (accessed June 02, 2017).
2. “Moore’s Law Is Dead. Now What?” by Tom Simonite at MIT Tech. Review, 13 May 2016. https://www.technologyreview.com/s/601441/moores-law-is-dead-now-what/ (accessed June 02, 2017).
3. “The Chip Design Game at the End of Moore’s Law” by Robert Colwell at “Hot Chips”, August 2013. http://www.hotchips.org/wp-content/uploads/hc_archives/hc25/HC25.15-keynote1-Chipdesign-epub/HC25.26.190-Keynotel-ChipDesignGame-Colwell-DARPA.pdf (accessed June 02, 2017).
4. Ball P. Nature 2012, 492, 174-176.
5. Service, R. F. Science 2012, 335, 394-396.
6. Markov, I. L. Nature 2014, 512, 147-154.
7. “Sunway TaihuLight”. http://www.top500.org/system/178764 (accessed June 02, 2017).
8. Brock, D.C. IEEE Spectr. 2016, 53, 54-60.
9. “SciDAC Review, 2010” by Geist, A. http://www.scidacreview.org (accessed June 02, 2017).
10. “Beyond Moore’s Law and Implications for Computing in Space” by Air Force Research Laboratory presentation, July 2, 2015. https://www.osti.gov/scitech/servlets/purl/12860528 (accessed June 02, 2017).
11. Mukhanov, O. A. IEEE Trans. Appl. Supercond. 2011, 21, 760-769.
12. Zhirnov, V. V.; Cavin, R. K.; Hutchby, J. A.; Bourianoff G. I. Proc. IEEE 2003, 91, 1934-1939.
13. Xu, Q.; Yamanashi, Y.; Ayala, C. L.; Takeuchi, N.; Ortlepp, T.; Yoshikawa, N. Design of an Extremely Energy-Efficient Hardware Algorithm Using Adiabatic Superconductor Logic. In Proceedings of 15th International Superconductive Electronics Conference, ISEC’2015, Nagoya, Japan, July 6-9, 2015; pp DS-P21.
14. “Cryogenic Computing Complexity (C3)”. https://www.iarpa.gov/index.php/research-programs/c3 (accessed June 02, 2017).
15. Holmes, D. S.; Kadin, A. M.; Johnson, M. W. Computer 2015, 48, 34-42.
16. Likharev, K.; Semenov, V. IEEE Trans. Appl. Supercond. 1991, I, 3-28.
17. Likharev, K. K.; Mukhanov, O. A.; Semenov, V. K. SQUID’85 1985, 1103-1108.
18. Ginzburg, V. L.; Landau L. D. J. Exp. Theor. Phys. 1950, 20, 1064-1081.
19. Stewart, W. C. Appl. Phys. Lett. 1968, 12, 277.
20. Tolpygo, S. K. Low. Temp. Phys. 2016, 42, 463-485.
21. “NIOBIUM PROCESS”. http://www.hypres.com/foundry/nioibiun-process/ (accessed June 02, 2017).
22. Gupta, D.; Li, W.; Kaplan, S.B.; Vernik, I.V. IEEE Trans. Appl. Supercond. 2001, 11, 731-734.
23. Filipov, T. V.; Amparo, D.; Kamkar, M. Y.; Walter, J.; Kirichenko, A. F.; Mukhanov, O. A.; Vernik, I. V. Experimental Investigation of ERSFQ Circuit for Parallel Multibit Data Transmission. In Proceedings of 16th International Superconductive Electronics Conference, ISEC’2017, Sorrento, Italy, June 12-16, 2017; pp.
Kirilyuk, A.; Kimel, A. V.; Rasing, T. *Rev. Mod. Phys.* **2010**, *82*(3), 2731-2784.

Klenov, N. V.; Kuznetsov, A. V.; Soloviev, I. I.; Bakurski, S. V.; Tikhonova, O. V. *Beilstein J. Nanotechnol.* **2015**, *6*, 1946-1956.

Murphy, A.; Averin, D. V.; Bezryadin, A. *New J. Phys.*, **2017**, *19*, 063015.

Giazotto, F.; Peltonen, J. T.; Meschke, M.; Pekola, J. P. *Nat. Phys.*, **2010**, *6*, 254-259.