A Sub-100mV Ultra-Low Voltage Level-Shifter Using Current Limiting Cross-Coupled Technique for Wide-Range Conversion to I/O Voltage

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This work was supported in part by the National Key Research and Development Program of China under Grant 2019YFB2204500 and Grant 2020YFB2205600; in part by the National Science Foundation of China under Grant 61874171; and in part by the Science, Technology and Innovation Action Plan of Shanghai Municipality, China, under Grant 1914220370.

ABSTRACT In this paper, a sub-100mV ultra-low-voltage level-shifter for wide-range voltage conversion to I/O voltage is presented. The level-shifter uses a current limiting diode-connected transistor with cross-coupled transistor structure to reduce the minimum input voltage down to 100mV while covering a wide output voltage range up to I/O supply voltage (3V). We propose an improved split-control output buffer to reduce the static current from $VDDH$ to $VSS$. The level-shifter is implemented using X-FAB 180nm HV CMOS process. The post-layout simulations show that the proposed structure achieves an average propagation delay of 7.57\,\mu s with a power consumption of 3.43nW when the supply voltages $VDDL$, $VDDH$, and input frequency are 100mV, 3V, and 1kHz, respectively. The design occupies 182.46\,\mu m\,^2 silicon area with a static power consumption of 3nW when $VDDL$ and $VDDH$ are 100mV and 3V, respectively, which is suitable for low power applications.

INDEX TERMS Differential cascode voltage switch, level-shifter, low power, sub-threshold voltage, wide voltage range.

I. INTRODUCTION

LEVEL-shifter is one of the key building blocks for wide supply operating voltage, low power applications, such as power management circuits [1], implantable circuits [2], wearable circuits [3], low power sensor circuits and edge computing circuits [4]–[7]. In these applications, some of the circuits are usually working with an ultra-low supply voltage of 200mV or even below and an operation frequency of several kilohertz to reduce the power consumption while the remaining circuits are operating at nominal supply voltage and the interface circuits through I/O are operating at a supply voltage ranging from 2.5 to 3.0V. Therefore, it is crucial for a level-shifter to convert the signals near the ultra-low supply voltage to a wide output voltage range from the nominal supply voltage (1.2V) to I/O supply voltage (3V) [8]–[23].

The associate editor coordinating the review of this manuscript and approving it for publication was Vyasa Sai.

Fig. 1 illustrates the two different types of level-shifter architectures, where the input signal, operating at a lower supply voltage, $VDDL$, is amplified to operate at a higher supply voltage, $VDDH$. Fig. 1(a) shows a conventional differential cascode voltage switch (DCVS) level-shifter. The $N$-type transistors NM1 and NM2 are the input devices, which pull the node $q1$/$q2$ to $VSS$ when the input signal $A$ is $VDDL$/$VSS$. Consequently, the output node $Q$ will be pulled to $VSS$/$VDDH$ by NM3/PM3 when $q2$ is $VDDH$/$VSS$. The proper functionality of a conventional DCVS level-shifter is highly dependent on the driving strength ratio between the $N$-type transistor NM1/NM2 and $P$-type transistor PM1/PM2 [8]. When the level-shifter is operating at an ultra-low supply voltage, $VDDL$, the $N$-type transistors are operating in the sub-threshold region, resulting in a significant reduction of the driving strength. Hence, it becomes much harder for transistor NM1/NM2 to pull node $q1$/$q2$ to $VSS$, affecting the functionality of the circuit, and limiting the input range of the circuit.
The node \( q_2 \) will be pulled to \( VDDL \) by the \( P \)-type transistor \( PM_2 \), leading to the output node \( q_1 \) transistor \( NM_1 \) will pull the node \( q_2 \) level shifter. When the input signal \( A \) is biased to \( VDDL \), the \( N \)-type transistor \( NM_1 \) will pull the node \( q_1 \) to \( VSS \). As a result, the node \( q_2 \) will be pulled to \( VDDH \) by the \( P \)-type transistor \( PM_2 \), leading to the output node \( Q \) pulled to \( VSS \) by \( NM_3 \). As illustrated in Fig. 1(b), there is no current contention problem for the CM-based level-shifter [9]. However, when the input signal \( A \) is biased to \( VDDH \), there exits a static current through transistors \( PM_1 \) and \( NM_1 \), which makes this structure unsuitable for ultra-low power applications. To minimize the static current, the Wilson CM-based level-shifter is proposed [10] to reduce the static current by introducing a feedback loop in the circuit. However, the voltage drop in the feedback loop will cause a large static current in the output buffer circuit.

To further improve the performance of level-shifters, several state-of-the-art architectures have been presented in recent years [11]–[17]. Reference [11] used a dual current mirror structure to reduce the voltage drop caused by the Wilson current mirror, achieving a delay of 30ns and a total power of 159nW when converting \( VDDL \) of 0.4V to \( VDDH \) of 1.8V. Reference [12] proposed an \( N \)-type diode-connected transistor current limiter to reduce the pull-up strength of the cross-coupled latch while achieving a delay of 25ns and a total power of 61.4nW when converting an input voltage of 0.3V to an output voltage of 1.8V. Reference [13] proposed to use diode-connected transistors with the dynamic current switching technique to ensure the correct operation over a wide \( VDDL \) range, achieving a delay of 95ns and energy per transition of 118fJ when \( VDDL = 0.35V \) and \( VDDH = 1.1V \). Reference [14] introduced a pull-up boost circuit on a single-stage DCVS architecture to reduce propagation delay and dynamic power consumption while achieving a delay of 31.7ns with energy per transition of 173fJ. Reference [15] introduced voltage differential and body biasing techniques to ensure robust level conversion at ultra-low input voltages while reducing the leakage current, achieving a delay of 21.98ns and energy per transition of 25.9fJ when the supply voltages, \( VDDL \) and \( VDDH \), are 0.3V and 1.2V, respectively. Reference [16] proposed using a level-shifting capacitor to increase the conversion range, achieving a delay of 29ns with a power consumption of 61.5nW when the supply voltages, \( VDDL \) and \( VDDH \), are 0.4V and 1.8V, respectively. Reference [17] introduced a Wilson current-mirror based level-shifter to achieve an average propagation delay of 186.3ns and energy per transition of 954fJ when the supply voltages, \( VDDL \) and \( VDDH \) are 0.3V and 0.6 to 3.3V, respectively. Although all these level-shifters cover a wide-input range, there is a lack of robust DCVS level-shifter architecture that can achieve an output voltage range up to 2.5V/3.3V.

In this paper, a level-shifter circuit is proposed that operates with a minimum input voltage of 100mV and achieves a wide output voltage range up to 3V. We propose to incorporate the current limiting diode-connected transistor with a cross-coupled transistor structure to minimize the current contention problem while achieving a very small input voltage. We also introduce an improved split-control output buffer circuit to increase the output voltage range. Hence, the proposed architecture has achieved an average propagation delay of 7.57\( \mu \)s and a dynamic power of 3.43nW with supply voltages \( VDDL \), \( VDDH \), and input frequency set to 100mV, 3V, and 1kHz, respectively. The circuit has a static power of 3nW when \( VDDL = 100mV \) and \( VDDH = 3V \).

The rest of the paper is organized as follows. Section II discusses the design and operation principles of our proposed level-shifter. Post-layout simulation results and discussions are detailed in Section III and IV. The conclusions are summarized in Section V.

**II. CIRCUIT DESIGN AND IMPLEMENTATION**

**A. DEVICE SELECTION**

Increasing the robustness of DCVS level-shifter under the ultra-low input voltage constraint can be achieved by increasing the width of critical transistors to enhance its driving capability. Due to the reverse narrow width effect (RNWE), the threshold voltage of \( N \)-type transistor, working in the sub-threshold region, will increase with the width of the transistor [24], reducing the effect of driving strength enhancement. Using a low voltage threshold (LVT) transistor reduces the transistor’s threshold voltage, allowing more voltage headroom to enhance the robustness of the circuit and reducing the propagation delay while maintaining a relatively small silicon area [25]. In our process, given the same device size, the LVT \( N \)-type transistor has a threshold \( 1.6 \times \) lower than the
regular/nominal voltage threshold $N$-type transistor (RVT) [26]. However, LVT transistors have a slightly higher leakage current compared to RVT transistors, inevitably increasing the static power consumption. Hence, LVT transistors are only used for devices that are critical to circuit functionality and performance, while RVT transistors will be used for the remaining devices to limit the leakage current.

![Circuit Diagram](image)

Fig. 2 shows the schematic diagram of the proposed level-shifter. TABLE 1. Dimension of transistors for proposed level-shifter.

| Transistor | W(μm)/L(μm) | Transistor | W(μm)/L(μm) |
|------------|--------------|------------|--------------|
| Inverter   |              | Level-Shifter |          |
| NM        | 1.32/0.18    | NM          | 1.32/0.18    |
| NM1       | 0.22/0.18 (x:2) | PM1        | 0.22/0.30    |
| NM2       | 0.22/0.18 (x:2) | PM2        | 0.22/0.30    |
| NM3       | 0.22/0.18 (x:2) | PM3        | 0.22/0.30    |
| NM4       | 0.22/0.35    | PM4        | 0.22/0.30    |
| NM5       | 0.22/0.35    | PM5        | 0.22/0.18    |
| NM6       | 0.22/0.35    | PM6        | 0.22/0.30    |

B. PROPOSED LEVEL-SHIFTER

Fig. 2 shows the schematic diagram of the proposed level-shifter. The sizes of the transistors are shown in Table 1. The input devices, NM1, NM2 and NM3 are implemented using two minimum-sized LVT transistors in parallel. This will further enhance the driving strength of the $N$-type transistor under ultra-low input supply voltages while minimizing the RNWE. However, the maximum drain-source voltage, $VDS$, of these LVT $N$-type transistors could only support a maximum voltage of 1.9V, which is not applicable under 3V power supply [26].

To ensure the transistors are working in safe operating area (SOA) [27], the two diode-connected 3V $N$-type transistors NM4 and NM5, whose maximum drain-source voltage $VDS$, and gate-source voltage, $VGS$, are 3.6V, are used as a voltage divider. We used the $N$-type diode-connected transistor in our structure as voltage divider instead of $P$-type diode-connected transistor [18] since the $N$-type transistor has much higher mobility than the $P$-type transistor. In our process, the mobility of the $N$-type transistor is $4.67 \times$ larger than the $P$-type transistor [26]. Therefore, given the same device size, using an $N$-type transistor as voltage divider allows a higher current driving capability than the $P$-type transistor, thus decreasing the delay of the circuit and reducing the static current during the transition. To prevent the breakdown of the transistors, it is important to ensure that the maximum threshold voltage variation for these transistors is within the operating margin under all process corners [26]. Hence, we have used the minimum size of the transistor for the voltage divider and the maximum threshold voltage variation is approximately 32mV under a spread of $\pm3\sigma$ [26]. Therefore, this variation is acceptable for a safe operation of our level shifter. To further ensure the safety of the LVT transistors, we have performed operation condition check (OCC) [28] simulations under all process corners. The LVT transistors’ drain-body voltage, $VDB$, is within safe limits during the transition, indicating the effectiveness of the voltage divider. We also modify the diode-connected transistors with cross-coupled transistors along with the split control output buffer, to achieve higher output swing than [18] while ensuring the stability of the circuit. The diode-connected $P$-type transistors PM3 and PM4 act as current limiters [29], easing the current contention problem between the $N$-type transistors, NM1 and NM2, and the cross-coupled $P$-type transistors, PM1 and PM2. To ensure the transistors are working in SOA, 3V $P$-type transistors are used for the cross-coupled latch as well as the current limiters. All transistors except the three LVT $N$-type transistors (NM1, NM2, and NM3) use the minimum size to reduce internal node capacitance.

C. IMPROVED SPLIT-CONTROL OUTPUT BUFFER CIRCUIT

Since the voltage of node $q2$, is between $VDN$ and $VDDH-VDP$, the output buffer of a standard inverter design suffers from the problem that when $A$ is $VSS$ (or $VDNL$), the $N$-type transistor (or $P$-type transistor) is in the near-threshold region instead of the cut-off region, leading to large static current from $VDDH$ to $VSS$. To overcome this problem, we improve the split-control output buffer [19] to support a wider output voltage range while minimizing the static current and reducing the propagation delay.

The work principles of our improved architecture can be described as follows: When the input signal $A$ changes from $VSS$ to $VDNL$, the transistors NM1 and NM3 are working in the sub-threshold region, and transistor NM2 is in the cut-off region. As a result, transistor NM1 pulls node $q1$ to $VDN$, causing transistor PM2 to pull node $p2$ to $VDDH$ and $q2$ to

1 $VDN$ and $VDP$ are the diode voltage drop of transistor NM4/NM5 and PM3/PM4, respectively.
VDDH-VDP. Subsequently, transistors PM5 and PM6 are in the cut-off and sub-threshold regions, respectively. Transistors NM3 and NM6 draw the output node Q to VSS. When A changes from VDDL to VSS, transistors NM1 and NM3 transit into the cut-off region, and transistor NM2 transits into the sub-threshold region, pulling node q2 to VDN. Transistors PM6 and NM6 are in the linear and sub-threshold regions, respectively. In the meantime, p2 is pulled to VDN+VDP by transistor PM2, allowing transistor PM5 to transit into the linear region to pull the output node Q to VDDH. Note that the voltage drop between node p2 and q2 ensures that transistor PM5 is always transited into sub-threshold region later than transistor PM6 and transited into linear region earlier than transistor PM6, reducing the static current from VDDH to VSS during transition. To speed up the pull-up process, transistor PM5 is implemented using an LVT P-type transistor instead of a 3V thick-oxide transistor. Our simulation result shows that using the LVT P-type transistor reduces the propagation delay by 16.8%, as shown in Fig. 3.

![FIGURE 3. Comparison of the Rising Edge Delay using LVT and SVT P-type transistor.](image)

III. POST LAYOUT SIMULATION RESULT

The circuit is implemented using the X-FAB 180nm HV CMOS technology. To evaluate the performance of the proposed circuit, post-layout simulations were performed. We use the inverter from the proposed circuit as the driving cell and a standard inverter from the 3V digital library as the load in the simulations. The propagation delays are calculated in the simulations using the following definitions:

(a) Rising propagation delay, \( t_{pdr} = t_{outf} - t_{inr} \), where \( t_{inr} \) is the time that the input signal rises across 20% of VDDL, and \( t_{outf} \) is time that the output signal falls across 20% of VDDH;

(b) Falling propagation delay, \( t_{pdf} = t_{outr} - t_{inf} \), where \( t_{inf} \) is the time that the input signal falls across 80% of VDDL, and \( t_{outr} \) is the time that the output signal rises across 80% of VDDH;

(c) Average propagation delay, \( t_{pd} = (t_{pdr} + t_{pdf}) / 2 \).

The layout of the circuit is shown in Fig. 4. The circuit has an area of 182.46µm². In this process, the LVT P-type transistor, PM5, is implemented in middle-voltage N-well, which requires larger spacing design constraints to the remaining devices [30]. The spacing between LVT transistors and 3V thick-oxide transistors is also relatively large, resulting in a more significant design footprint.

![FIGURE 4. Layout of the Proposed level-shifter.](image)

![FIGURE 5. Transient Results of the Proposed Level-shifter (VDDL = 100mV and VDDH = 3V).](image)

Fig. 5 shows the signal transition of our proposed level shifter circuit, where the circuit is able to operate at the minimum VDDL of 100mV to VDDH of 3V under a typical corner and temperature of 27°C at 1kHz. The proposed circuit achieves an average delay of 7.57µs and a power consumption of 3.43nW when VDDL = 100mV, VDDH = 3V, and \( f_{in} = 1kHz \). As shown in Fig. 5, the average static current of our proposed DCVS circuit and the improved SCL buffer from VDDH to VSS during transition is 1.56nA and 0.46nA, respectively, when VDDL = 100mV and VDDH = 3V. We have performed a simulation on the level-shifter using the proposed current limiting cross-coupled circuit and a conventional split-controlled output buffer under a supply voltage VDDL of 100mV and VDDH of 3V, and compared the static current with our proposed structure. The level-shifter with a conventional
SCL output buffer has an average delay of 2.4\(\mu\)s and a power consumption of 7.45nW when \(VDDL = 100\text{mV}, VDDH = 3\text{V}\), and \(f_{in} = 1\text{kHz}\). As shown in Fig. 6, the maximum static current through the conventional output buffer during transition is 2.26\(\mu\)A while the proposed structure has a maximum static current of 10.34nA, indicating the effectiveness of our new structure.

**A. PROPAGATION DELAY**

Fig. 7 shows the relationship between the propagation delay and input voltage under all process corners, while keeping the output voltage at 3V. Under the worst-case process corner, ‘ws’ (‘slow’ N-type transistor and ‘slow’ P-type transistor), our circuit works correctly under input voltage of 100mV with a propagation delay of 83.4\(\mu\)s. The propagation delay against output voltage \(VDDH\) simulated with an input voltage of 100mV under all corners is shown in Fig. 8. Our proposed level-shifter functions correctly even when \(VDDH\) decreases to 1.2V with a propagation delay of 104.5\(\mu\)s under ‘ws’ corner, demonstrating that our proposed structure is able to cover a wide output voltage range under the worst condition.

**B. POWER CONSUMPTION**

Fig. 9 shows the relationship between the dynamic power consumption of the circuit and the input voltage. The simulation was performed under all corners and a supply voltage \(VDDH\) of 3V and input frequency \(f_{in}\) of 1kHz. Our proposed level-shifter has achieved a minimum dynamic power of 1.6nW when the input voltage is 200mV under ‘wz’ corner (‘slow’ N-type transistor and ‘fast’ P-type transistor), and has the maximum dynamic power of 85.7nW when the input voltage is 700mV under ‘wp’ corner (‘fast’ N-type and ‘fast’ P-type transistors).

**C. PVT VARIATION ASSESSMENT**

The influence of temperature variation to propagation delay is evaluated under the condition \(VDDL = 100\text{mV}, VDDH = 3\text{V}, f_{in} = 1\text{kHz}\). The results are shown in Fig. 10. The proposed circuit has achieved a minimum delay of 104.5ns when the temperature is 125\(\degree\)C under ‘wp’ corner, and has the maximum delay of 235.5\(\mu\)s when the temperature is 5\(\degree\)C under ‘ws’ corner.

**D. RELIABILITY ASSESSMENT**

Monte Carlo experiment with 4000 simulations is performed under the condition \(VDDL = 100\text{mV}, VDDH = 3\text{V}, f_{in} = 1\text{kHz}\).
The results are shown in Fig. 11 with an estimated functional yield of 96.5%. The standard deviation for propagation delay and power consumption of the proposed circuit is 5.85 μs and 3.56 nW, respectively. We have also conducted a Monte-Carlo analysis with 1000 experiments under different input/supply voltages of 50mV, 100mV, 400mV, and 1V with $V_{DDH}$ of 3V and input signal frequency of 1kHz to further understand the reliability of the proposed circuit. As shown in Fig. 12, the estimated functional yield under input voltage of 50mV, 100mV, 400mV, and 1V is 41.5%, 96.5%, 100%, and 100%, respectively. To compare the reliability of the proposed circuit with the state-of-the-art level-shifters, we have optimized the transistors’ size of the level-shifter [20] to achieve optimal delay, power consumption and silicon area.

Then, we analyzed the reliability of [20] and the proposed circuit using Monte-Carlo analysis under different input/supply voltages of 50mV, 100mV, 400mV, and 1V with $V_{DDH}$ of 3V and input signal frequency of 1kHz. As shown in Fig. 13 and Fig. 14, the proposed circuit has an estimated functional yield under 50mV, 100mV, 400mV, and 1V of 49.4%, 96.7%, 100%, and 100%, respectively. The estimated functional yield of level-shifter circuit [20] with a minimum input/supply voltage of 100mV is 68.5%, which is 28% lower than our proposed architecture. Hence, our proposed architecture has clearly demonstrated an improvement made in designing a robust ultra-low voltage level-shifter for a wide-range signal conversion to I/O voltage.

**IV. BENCHMARK & DISCUSSIONS**

To evaluate the robustness of our proposed architecture, we have evaluated our design with 55nm CMOS process by adopting a similar device selection methodology and using the minimum size of the transistors for all the devices except for NM1, NM2, and NM3, who are implemented using two minimum-sized transistors in parallel. The circuit achieves an average delay of 4.8μs and power consumption of 12.1nW...
TABLE 2. Comparison with State-of-the-Art Level Shifters with Wide-Range Conversion to I/O voltage in Typical Corner (VDDL=400mV, f_in=1MHz).

| Reference | Type  | Process (nm) | Minimum VDDL (nV) | Output Voltage (V) | Average Delay (ns @ VDDH) | Static Power Saving (nW@VDDH) | Total Power Saving (nW@VDDH) | Power Saving (ns@VDDH) | PDP Saving (ns@VDDH) | Area (μm²) | PDAP (nW·μm²) |
|-----------|------|--------------|------------------|-------------------|---------------------------|---------------------------|----------------------------|-------------------|-------------------|-----------|---------------|
| [17][1]   | Hybrid  | 180          | 210              | 1.8-3.3           | -                          | 0.16@1.8V                 | -                          | -                | -                | -         | 153.01        |
| [19][1]   | DCVS   | 130          | 300              | 2.5              | 58.78@2.5V                 | 0.7248@2.5V               | 19102.5V                  | 11226.2V          | -                | -         | 71.94 x 10^5  |
| [20][2]   | DCVS   | 180          | 280              | 1.8              | 23.69@1.8V                 | 0.3@1.8V                  | 1231.1@1.8V               | 2916@1.8          | 10474            | 63        | 1.84 x 10^5   |
| [21][2]   | Hybrid  | 180          | 360              | 1.8              | 12@1.8V                    | 0.13@1.8V                 | 175@1.8V                  | 1070              | 2100@1.8V       | 14546      | 120.9        | 2.54 x 10^5   |
| [8][2]    | CM     | 180          | 360              | 1.8              | 30@1.8V                    | 0.2@1.8V                  | 158.8@1.8V                | 4770@1.8V         | 6412             | 103       | 4.91 x 10^5   |
| [22][2]   | CM     | 180          | 210              | 1.8              | 6.1@1.8V                   | 0.09@1.8V                 | 76.248@1.8V               | 246               | 465.7@1.8V      | 65677      | 35.25        | 1.64 x 10^4   |

This work[2] DCVS 180 100 1.2-3.0 22.47@1.8V 72x 1.26@1.8V 84.32@1.8V 223@3V 1895@1.8V 16122@3V 72.4 x 10^5

(1) Measurement Results. (2) Simulation Results.

TABLE 3. Comparison with Redesigned State-of-the-Art Level Shifters using our circuit parameters based on X-FAB 180nm HV CMOS Process in Typical Corner (VDDL=400mV, f_in=1MHz).

| Reference | Type  | Minimum VDDL (nV) | Output Voltage (V) | Average Delay (ns @ VDDH) | Static Power Saving (nW@VDDH) | Total Power Saving (nW@VDDH) | Power Saving (ns@VDDH) | PDP Saving (ns@VDDH) | Area (μm²) | PDAP (nW·μm²) |
|-----------|------|------------------|-------------------|---------------------------|---------------------------|----------------------------|-------------------|-------------------|-----------|---------------|
| [17][1]   | Hybrid  | 180              | 210              | 1.8-3.3           | -                          | 0.16@1.8V                 | -                | -                | -         | 153.01        |
| [19][1]   | DCVS   | 130              | 300              | 2.5              | 58.78@2.5V                 | 0.7248@2.5V               | 19102.5V                  | 11226.2V          | -                | -         | 71.94 x 10^5  |
| [20][2]   | DCVS   | 180              | 280              | 1.8              | 23.69@1.8V                 | 0.3@1.8V                  | 1231.1@1.8V               | 2916@1.8          | 10474            | 63        | 1.84 x 10^5   |
| [21][2]   | Hybrid  | 180              | 360              | 1.8              | 12@1.8V                    | 0.13@1.8V                 | 175@1.8V                  | 1070              | 2100@1.8V       | 14546      | 120.9        | 2.54 x 10^5   |
| [8][2]    | CM     | 180              | 360              | 1.8              | 30@1.8V                    | 0.2@1.8V                  | 158.8@1.8V                | 4770@1.8V         | 6412             | 103       | 4.91 x 10^5   |
| [22][2]   | CM     | 180              | 210              | 1.8              | 6.1@1.8V                   | 0.09@1.8V                 | 76.248@1.8V               | 246               | 465.7@1.8V      | 65677      | 35.25        | 1.64 x 10^4   |

This work[2] DCVS 180 100 1.2-3.0 22.47@1.8V 72x 1.26@1.8V 84.32@1.8V 223@3V 1895@1.8V 16122@3V 72.4 x 10^5

(1) Using thin oxide transistors. (2) Using MV transistors. (3) VDDL = 500mV, f_in = 200kHz. (4) VDDL = 950mV, f_in = 50kHz.

when VDDL = 100mV, VDDH = 3V, and f_in = 1kHz. The area of the circuit has been reduced to 30μm². Therefore, the area penalty of using both LVT and 3V devices under 180nm CMOS process becomes negligible under better manufacturing capability to fabricate the LVT and 3V devices in advanced CMOS technologies.

Table 2 presents the performance of our proposed architecture and the state-of-the-art level-shifters [8], [17], [19],–[22]. Similar to the evaluation methods used in [20], [31] to evaluate the state-of-art works, we have optimized the transistors’ size of all circuits to achieve optimal delay, power consumption and silicon area. We then evaluated these circuits under an input supply voltage of 400mV, the output supply voltages of 1.8V and 3.0V, and an input signal frequency of 1MHz. The benchmark result is summarized in Table 2. The Power-Delay-Product (PDP) is a common figure of merit (FoM) to evaluate the performance of the circuit. The Power-Delay-and-Area Product (PDAP) is also considered to understand the impact on the performance and area trade-offs [23], [32]. Under an input supply voltage of 400mV, an output supply voltage of 1.8V, and an input signal frequency of 1MHz, our proposed level-shifter achieves an average propagation delay of 22.47ns and total power consumption of 84.32nW. When the input supply voltage is 400mV, the output supply voltage is 3V, and the input signal frequency of 1MHz, the proposed level-shifter has the lowest average propagation delay of 14.37ns among all the works and a power consumption of 276nW.

The simulation results of the re-designed state-of-the-art works are shown in Table 3. As illustrated in Table 3, our proposed level-shifter operates with a minimum input supply voltage of 100mV and achieves the lowest PDP of 1895nW when the input voltage is 400mV, and the input signal frequency is 1MHz, the proposed level-shifter has the lowest average propagation delay of 14.37ns among all the works and a power consumption of 276nW.

V. CONCLUSION

This work presents a sub-100mV ultra-low-voltage level-shifter for wide-range voltage conversion to I/O voltage. The proposed structure uses a current limiting diode-connected transistor with a cross-coupled transistor structure to minimize the current contention problem under ultra-low input supply voltage. We also proposed an improved SCL...
output buffer to reduce the static current flowing from VDDH to VSS. Our design was implemented using X-FAB 180nm HV CMOS technology. The proposed circuit occupies an area of 182.46 µm². The post-layout simulations show that our proposed circuit has an average propagation delay of 7.57 µs with a power consumption of 3.43nW with the supply voltages VDDL, VDDH, and input frequency set to 100mV, 3V, and 1kHz, respectively. Compared to the state-of-art-works, our proposed level-shifter has achieved the lowest propagation delay of 14.37 µs, the lowest total power of 276nW, and the lowest PDP of 3966 ns·nW when VDDL = 0.4V, VDDH = 3V, and $f_{\text{in}} = 1$MHz.

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