Direct-written polymer field-effect transistors operating at 20 MHz

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Printed polymer electronics has held for long the promise of revolutionizing technology by delivering distributed, flexible, lightweight and cost-effective applications for wearables, healthcare, diagnostic, automation and portable devices. While impressive progresses have been registered in terms of organic semiconductors mobility, field-effect transistors (FETs), the basic building block of any circuit, are still showing limited speed of operation, thus limiting their real applicability. So far, attempts with organic FETs to achieve the tens of MHz regime, a threshold for many applications comprising the driving of high resolution displays, have relied on the adoption of sophisticated lithographic techniques and/or complex architectures, undermining the whole concept. In this work we demonstrate polymer FETs which can operate up to 20 MHz and are fabricated by means only of scalable printing techniques and direct-writing methods with a completely mask-less procedure. This is achieved by combining a fs-laser process for the sintering of high resolution metal electrodes, thus easily achieving micron-scale channels with reduced parasitism down to 0.19 pF mm⁻¹, and a large area coating technique of a high mobility polymer semiconductor, according to a simple and scalable process flow.

Printed organic electronics has become a widespread research field in the recent years, thanks to the increased compatibility of the fabrication techniques with flexible, low-cost substrate materials, which results in the tangible prospect of economically convenient mass production of distributed electronics1–4. Notable demonstrations have been proposed for light detectors5,6, sensors7,8, transistors9, and on their integration into truly fully-printed opto-electronic circuits10–14, setting a step forward in the adoption of this technology into real life. On the other hand, the enhancement of some desirable figures of merit still has to be appropriately approached to enable the implementation of a wide range of real applications. To this goal, it is of key importance to enhance the performance of the single organic transistors constituting the basic building block of almost any electronic circuitry.

Primarily, a transistor operation frequency suitable for more demanding applications must be guaranteed, e.g. several MHz at least in the case of addressing electronics for high-resolution flexible displays15, wireless communication devices16–18, and RFID-based item-tracking systems19,20. Yet, in the majority of works, AC operation is either not assessed or considered a secondary goal compared to DC performance, and it is only marginally developed and analyzed.

It is well established that in typical organic field-effect architectures the optimization of high-frequency operation, besides requiring the adoption of semiconducting materials guaranteeing high effective mobility21,22 and of dielectric layers with high relaxation frequency and yielding interfacial properties promoting efficient charge transport23,24, is largely determined by the reduction of the device channel length and of gate parasitic capacitance25. Nonetheless, this operation increases the influence of the charge injection limitations on the overall behavior of the device26–28. Fulfilling such requirements with a mask-less and fully solution-based process flow, albeit challenging, is highly desirable for the development of cost-effective technologies for wearable, portable and distributed applications.

However, while promising results in AC operation of organic FETs have been reported, with a maximum operating frequency as high as 27.7 MHz29, record values have been so far mainly achieved by adopting photolithographic steps30–33 and/or single crystal semiconductors34. To date, one order-of-magnitude lower operating frequencies have been demonstrated when mask-less, scalable techniques were used, with a maximum of 3.3 MHz35–37.

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In this work, we used a complete mask-less approach for the development of fully solution-processed polymer FETs capable of operating at frequencies as high as 20 MHz. In particular, we demonstrated the successful combination of printing techniques, such as large-area bar-coating\(^{41}\), and digital fs-laser sintering\(^{39-41}\). The latter is a direct writing technique for the fine patterning of a specifically formulated silver nanoparticle (Ag-NP) ink that allowed the fabrication of high-resolution conductive features down to a minimum lateral size of ~1.3 μm, to be used as electrodes for high performance polymer FETs.

**Results**

**Ag-NP ink preparation.** We have specifically developed a silver ink for the fs-laser sintering process, starting from the synthesis of AgNPs with narrow size distribution, using a mixture of sodium citrate and tannic acid as reducing and stabilizing agents in aqueous conditions\(^{42}\). Other synthesis protocols have been recently proposed using tannic acid for controlling nanoparticle size either in combination with sodium citrate\(^{43}\) or by careful control of the reaction mixture pH\(^{44}\). However, the reported conditions appear to be unsuitable for the preparation of AgNPs in such large amounts as required for conductive ink applications. We have, therefore, conducted an optimization of the reaction conditions and in particular, reagents ratio and order of addition of the reagents, to allow the preparation of 23.8 ± 4.0 nm AgNPs (Fig. 1a and b) with a production scale-up factor between 150 and 300 times and yet of comparably narrow size distribution as those previously reported in the literature\(^{42-44}\). In a typical synthesis, our method yields 20 times more AgNPs also with respect to the approach recently reported by Zhang and coworkers\(^{45}\). After synthesis, the AgNPs were concentrated by centrifugation and coated by polyvinylpyrrolidone (PVP) of relatively low molecular weight (10 kDa). The choice of this polymer allowed us to increase the stability and processability of the AgNPs colloidal solution, while keeping thin the organic layer on the nanoparticle surface, a desirable property when aiming at conductive inks. The final AgNPs-based conductive inks have silver content of approx. 7% in water as the dispersion medium.

**Fs-laser sintering process.** The AgNP ink was exploited to fabricate the device electrodes, following the process flow schematically illustrated in Fig. 1c. First, a uniform film of the conductive ink is deposited onto a substrate by spin-coating. Then, a femtosecond pulsed laser beam (λ = 1030 nm, 67 MHz repetition rate) locally heats the nanoparticle film and patterns the desired geometry of conductive features which are ~70 nm thick. As a final step, the unprocessed areas of the film are washed away using water, and only the conductive high-resolution patterns. We fabricated 190μm-long single lines varying said process parameters and measured their lateral width and electrical resistance. In Fig. 1e we relate the obtained line width with the beam power for different scanning speeds: an approximately linear dependence can be identified in the range from 5 to 30 mW, yielding linewidths from a minimum of 1.3 to 5.3 μm. A similar trend is highlighted also when testing the line width versus beam power varying the optics (0.1 mm/s, Fig. 1d).

The conductivity of the laser-sintered lines was compared to the bulk-Ag conductivity for different beam power and scanning speed (Fig. 1f). A general increase of the conductivity is observed when increasing the beam power or slowing down the scanning speed, and its value ranges between 4.5 and 21 kΩ/cm, which corresponds to a range from 0.7 to 3.3% of bulk silver conductivity. This range is in line with the typical conductivities obtained with more established direct-writing techniques, such as inkjet-printing\(^{46}\). This validates the suitability of this process and ink for the fabrication of high-resolution conductive patterns for organic electronics applications.

We then employed fs-laser sintering for the fabrication of the source and drain bottom contacts of polymer FETs, in order to benefit both from the reduction of the channel length and of the width of the contacts. Previous examples where fs-laser sintered contacts were used for organic FETs are reported in refs 41,47. Such examples either did not integrate high-resolution, reduced parasitic capacitance electrodes\(^{41}\), or adopted more expensive Au inks\(^{47}\). Both reported only bottom-gate, bottom-contacts architectures, which, while more easily accessible, are not as performing as staggered, top-gate devices for injection in downscaled channels. Indeed, very limited performance in terms of mobility were achieved (μ lower than 10^-2 cm^2/Vs for channel lengths longer than 5 μm). Therefore, previous reports do now answer the question whether fs-laser sintering is a candidate for the fabrication of high-frequency, direct-written polymer transistors, which is the main goal of the present work.

**Polymer FETs fabrication and DC characterization.** We fabricated high-resolution short- and long-channel n-type polymer FETs in a staggered, top-gate configuration (Fig. 2d), which is known to yield better charge injection properties from the contacts\(^{26}\). The fabrication process flow is illustrated in Fig. 2a. For the contacts, following the optimization process described above, the chosen laser processing parameters were set to 12 mW beam power (1.9 mW/μm²), 50X optics, 0.5 mm/s scanning speed. A typical AFM image of a fabricated contact is shown in Fig. 1g. We adopted the semiconducting co-polymer poly[N,N’-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5’-(2,2’-bithiophene), P(NDI2OD-T2) (Fig. 2c), which was deposited through bar-coating, a scalable large-area printing technique\(^{38}\). A 500 nm-thick PMMA layer was deposited through spin-coating, and finally we selectively inkjet-printed PEDOT:PSS over the channel and contact area to create the top gate contact. We fabricated devices with different channel lengths L of 1.75, 5.1 and 21.6 μm. The contact width W was 3.0 ± 0.5 μm and the channel width W was 800 μm, both constant among all devices. A micrograph of the realized pattern, prior to semiconductor deposition, is shown in Fig. 2b.
In Fig. 2e and f, we show the measured transfer curves for two long channel devices ($L = 5.1 \mu m$, red line, and $L = 21.6 \mu m$, blue line) and for a short-channel device ($L = 1.75 \mu m$). We summarize in Table 1 the extracted apparent mobilities for the full set of fabricated polymer FETs.

The devices exhibit proper $n$-type operation and in the linear regime ($V_{dd} = 5 V$) the drain current scales accordingly with the reduction of the channel length. The correct scaling is confirmed by the extracted values of linear charge mobility, which remains comparable (in the range 0.1–0.2 cm$^2$V$^{-1}$s$^{-1}$) while the channel length is scaled by one order of magnitude (Figure S2), suggesting good charge injection behavior at the semiconductor/
contact interface. We performed a first approach estimation based on the Transfer Line Method (TLM) method, which can slightly underestimate the contact resistance for the semiconductor in use, and found a normalized contact resistance $R_{cW} = 7.3 \, \Omega \cdot \text{cm}$ at $V_g = 40 \, \text{V}$ (Figure S1), indicating that the scaled electrodes fabricated with our method inject and collect charges effectively.

In the saturation regime we extracted good effective mobilities of $0.37 \, \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and $0.74 \, \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ for the devices with channel lengths $L = 21.6 \, \mu\text{m}$ and $L = 5.1 \, \mu\text{m}$ respectively ($V_g = V_d = 40 \, \text{V}$), and a high effective mobility of $0.82 \, \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ ($V_g = 22.5 \, \text{V}$, $V_d = 40 \, \text{V}$) in the case of the shortest channel length of $1.75 \, \mu\text{m}$. In the latter case, we observed a breakdown of the device at currents above $0.9 \, \mu\text{A}/\mu\text{m}$ when $V_d = 40 \, \text{V}$ and $V_g > 25–30 \, \text{V}$, so we limited the driving voltage accordingly, below the onset of breakdown. We remark how the measured effective mobilities in the saturation regime increase when shortening the channel length, in contrast with the behavior exhibited by the linear regime. In fact, we identified a gate dependence of the charge mobility in the saturation regime whose effect is amplified at shorter channel lengths (Figure S3). This behavior is not unique to our work, it is general for the semiconductor in use, it characterizes several high mobility donor-acceptor copolymers recently reported and it can be explained by an effect of the lateral field on injection and/or transport.

| Channel length [$\mu\text{m}$] | Linear mobility [$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$] | Saturation mobility [$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$] |
|-------------------------------|---------------------------------|---------------------------------|
| 1.75                          | 0.13                      | 0.82*                     |
| 5.1                           | 0.14                      | 0.74                      |
| 21.6                          | 0.22                      | 0.37                      |

Table 1. Extracted mobilities for the laser sintered OFETs. $V_g = 22.5 \, \text{V}$. 

Figure 2. OFET fabrication and DC characterization. (a) Sketch of the fabrication process, (b) optical micrograph of the bottom source and drain electrodes realized through laser sintering, (c) chemical structure of P(NDI2OD-T2), (d) sketch of the realized OFET, and (e) transfer characteristics of two devices with channel lengths $L = 5.1 \, \mu\text{m}$ and $L = 21.6 \, \mu\text{m}$ ($W = 800 \, \mu\text{m}$) and (f) transfer characteristic of a short-channel device ($L = 1.75 \, \mu\text{m}$, $W = 800 \, \mu\text{m}$).
Polymer FETs AC characterization and high-frequency operation. The successful adoption of high resolution fs-laser sintered contacts in polymer FETs allowed us to assess the impact on the maximum operational frequency of the fabricated devices. First, it is worth recalling that, at a first approximation, the final limitation to the speed of a FET is determined by the charge carrier transit time across the channel:

\[ t_{tr} = \frac{L}{\mu v E} \]

where \( v \) is the carrier velocity, \( E \) is the lateral electric field across the channel and \( V \) is the drain-to-source voltage. However, additional parasitism intervenes to reduce the actual maximum operational frequency well below this limit. In particular, the overlap capacitances insisting between gate and source/drain electrodes are the most critical in the low-resolution architectures (e.g. tens of \( \mu \)m for inkjet-printed contacts) typically adopted in organic FETs fabrications. A more appropriate figure of merit to describe the maximum operational frequency of a FET is the transition frequency \( f_t \), corresponding to the frequency at which the total AC gate, or “input”, current \( i_g \) becomes equal to the AC drain, or “output” current \( i_d \).

\[ f_t = \frac{g_m}{2 \pi (C_{gs} + C_{gd})} \]  

Figure 3. AC characterization of high-frequency OFETs. (a) Sketch of the lateral view of the realized OFETs, highlighting the different capacitances insisting across the device electrodes, (b) measured \( C_{gs} \) in depleted-channel \( (V_g = -15 \text{ V}, V_d = -15 \text{ V}) \) and in accumulated-channel \( (V_g = 25 \text{ V}, V_d = 25 \text{ V}) \) regimes for an n-type device \( (L = 1.75 \mu \text{m}) \), (c) measured source and drain capacitances for different channel lengths in depleted- and accumulated-channel regimes and (d) determination of the transition frequency for a device \( (V_g = 30 \text{ V}, L = 1.75 \mu \text{m}) \).

In order to extract \( f_t \), we measured separately \( C_{gs} \) and \( C_{gd} \) as a function of frequency for our devices. Details on the extraction methodology can be found in the Supporting Information (SI). Source and drain capacitances were measured both by operating the FETs at \( V_g = -15 \text{ V} \) and \( V_d = -15 \text{ V} \) (off-state regime), when we expect to probe only the physical overlap capacitances, and at \( V_g = 25 \text{ V} \) and \( V_d = 25 \text{ V} \) (on-state, saturation regime), when we expect an increased capacitance, due to the accumulated channel region. In Fig. 3b we show the measured \( C_{gs} \) in both regimes for a device with \( L = 1.75 \mu \text{m} \): in off-state regime a capacitance of 0.10 pF is measured, which is in very good agreement with the theoretical value of 0.096 pF, calculated for a parallel-plates capacitor model with an area corresponding to the geometrical overlap between the source and gate. When accumulating the channel, we measured a capacitance increase of 0.03 pF, which is attributed to the addition of the channel area to the electrodes overlap capacitance. We measured the gate-source capacitance in the saturation regime for different channel lengths and linearly fitted the measured data (Figure S4). The intercept of the fitted line at \( L = 0 \mu \text{m} \), which is attributed to the addition of the channel area to the electrodes overlap capacitance. We measured the gate-source capacitance in the saturation regime for different channel lengths and linearly fitted the measured data (Figure S4). The intercept of the fitted line at \( L = 0 \mu \text{m} \), which is attributed to the addition of the channel area to the electrodes overlap capacitance. The slope of the fitted line, representing the accumulated channel capacitance per unit channel length, returns 0.026 pF/\( \mu \text{m} \). If \( C_{die} \) is the dielectric capacitance per unit area, this slope can be theoretically estimated as \[ \frac{C_{die}}{L} = \frac{1}{5} WC_{die} = 0.034 \text{pF/\( \mu \text{m} \))}, \] which is in good agreement with the fitting. We also measured the gate-drain capacitance in the saturation regime: \( C_{gd} \) is equal both in accumulation and in the off-state,

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corresponding to 0.21 pF for the shortest channel length and consistently with the fact that, in this regime, we are only probing the gate/drain overlap capacitance. The good agreement between the measurements and theoretical value of $C_{gd}$ is obtained also for longer channel lengths. All capacitance data, both for $C_{gd}$ and $C_{gs}$, have been summarized in Fig. 3c. We measured the transconductance of the short-channel device in the range 1 kHz–2 MHz. Differently from the ideal behavior, a slight roll-off of this figure with frequency can be identified which reduces $g_{m}$ from 52.8 μA/V·s at 1 kHz to 42.8 μA/V·s at 2 MHz (Fig. 3d, black solid line). The maximum frequency limitation of the setup prevented the measurement of the transconductance beyond 2 MHz, and we determined the transition frequency by linearly extrapolating the measured trends of $g_{m}$ and $C_{g}$. In Fig. 3d we show the measurement and the determined $f_{t} = 20$ MHz. A simple calculation from the measured $g_{m}$ at 1 kHz and the measured $C_{g}$ according to (1), would return an $f_{t} = 24.7$ MHz. Recalling the discussion above, we validate our result by comparing the frequency obtained by AC measurements with the ultimate limit defined by the transit time of the carriers across the channel: for our shortest-channel device we obtain $t_{tr} = 0.9$ ns corresponding to an ideal cutoff frequency of $f_{tr} = \frac{1}{2\pi t_{tr}} = 170$ MHz. The extrapolated $f_{t}$ is well below the calculated cut-off frequency due to the carrier transit time, thus our estimation is not undermined by the extrapolation method.

**Discussion**

In Table 2 we compare the result obtained in this work with previous works in which the transition frequency has been explicitly measured, and we report, along with $f_{t}$, other relevant figures of merit (i.e. operational voltage and effective mobility) and fabrication details of the devices. Please note that the reported mobility values are effective parameters, largely depending on the specific device architecture.

### Table 2. Properties and fabrication techniques for the polymer FETs with the highest reported transition frequencies (listed mobility values are to be considered effective parameters, largely depending on the specific device architecture).

| $f_{t}$ [MHz] | Ref. | Semiconductors | Voltage [V] | Mobility [cm²V⁻¹s⁻¹] |
|---------------|------|---------------|-------------|----------------------|
| 27.7          | 29   | C60           | Evaporated  | 20       | 2.22               |
| 25            | 32   | Rubrene       | Single Crystal | −15   | 10.3              |
| 20            | 30   | C_{60}DNTT    | Evaporated  | −20   | 0.4              |
| 20            | 34   | DNTT          | Evaporated  | −15   | 0.44             |
| 19            | 33   | C_{60}DNTT    | Evaporated  | −10   | 2.5              |
| 11.4          | 29   | Pentacene     | Evaporated  | −20   | 0.73             |
| 10            | 30   | C_{60}DNTT    | Sol. Crystallized | −20   | 0.4              |
| 3.7           | 57   | DNTT          | Evaporated  | −3    | 0.7              |
| 1.5–2         | 23   | PBTTOR        | Spin-coated | −4    | 2.5              |

**Direct-written electrodes**

| $f_{t}$ [MHz] | Ref. | Semiconductors  | Voltage [V] | Mobility [cm²V⁻¹s⁻¹] |
|---------------|------|-----------------|-------------|----------------------|
| 20            | This work | P(NDIZOD-T2) | Printed (bar-coating) | 30       | 0.9              |
| 3.3           | 36   | P(NDIZOD-T2)   | Printed (inkjet) | 30       | 0.005             |
| 2.8           | 36   | DPFF-TT        | Printed (inkjet) | −25     | 0.024             |
| 1.6           | 25   | pBTTT          | Spin-coated  | −8     | 0.1              |

The strong enhancement of this figure of merit with respect to previous works dedicated to maskless fabrication of organic electronics, limited to 3.3 MHz in the best case, is ascribed to multiple contributions. The drastic improvement in the resolution for the definition of the FETs source and drain contacts, owing to the use of fs-laser sintered high-conductive AgNP electrodes, is combined with the bar-coating of an optimized semiconductor morphology enabling enhanced effective field-effect mobility, also thanks to good charge injection properties of such electrodes. The aforesaid fabrication strategy improves the patterning resolution of a typical direct-writing technique, e.g. inkjet printing, by more than 10 times and obeys the multiple role of reducing both the transistor channel length and the parasitic capacitance present between these electrodes and the gate. Moreover, the proposed process retains additional room for improvement in terms of reduction of the parasitic capacitance, e.g. by galvo-scanners, generated from the same laser source. A further possibility for the improvement of the throughput is the adoption of Spatial Light Modulators, which may enable the possibility to write sections of a device or a circuit in a single step. Additionally, we recall that, in a practical application, only a fraction of the features needs to be defined with a high resolution, so that the effective throughput can be further...
enhanced. In perspective, these features enable the applicability of the proposed process to large-volumes manufacturing at reduced cost of circuits incorporating polymer transistors operating beyond 20 MHz, therefore widely expanding possible applications of cheap flexible electronics.

Methods

General (NP-ink synthesis). All reagents were purchased from Sigma-Aldrich, and used without further purification: silver nitrate (nr. 209139, ACS reagent, ≥99.0%), tannic acid (nr. 403040, ACS reagent), sodium citrate tribasic dehydrate (nr. 71402, BioUltra, ≥99.5%), polyvinylpyrrolidone (nr. PVP10, average m.w. 10 kDa). All glassware employed for AgNP preparation was cleaned with conc. HNO₃ and rinsed with plenty of water. Ultrapure deionized water (Millipore purification system, 18.2 MΩ cm) was used for the preparation of all aqueous solutions. All solutions used for nanoparticle preparation were filtered through a 0.2 μm membrane filter (Whatman, cellulose acetate). AgNPs were characterized by Dynamic Light Scattering (DLS) (Zetasizer Nano ZS, Malvern Instruments). AgNP diameter was measured via TEM (JEOL JEM-1011 transmission electron microscope operating at an accelerating voltage of 100 kV). UV/Vis spectra and fluorescence measurements were carried out using a TECAN Infinite M200 Pro plate reader. The concentration of silver in the inks was determined via ICP-OES (Agilent 720 ICP-OES).

Nanoparticle synthesis. Silver nitrate (1.274 g, 7.50 mmol) was dissolved in 1.45 L of water. The solution was heated with efficient stirring and protected from light until it started to reflux followed by quick addition of 30 mL of a freshly prepared solution of sodium citrate (0.302 M, 15.1 mmol) and tannic acid (7.35 × 10⁻³ M, 3.68 × 10⁻² mmol) in water. Accordingly, the concentrations of reactants in the reaction mixture were: [Ag] = 5.00 × 10⁻³ M, [Na citrate] = 1.00 × 10⁻¹ M, and [tannic acid] = 2.45 × 10⁻³ M. The solution rapidly turned dark indicating nanoparticle formation, but heating was continued for additional 30 minutes. Heating was then removed and the reaction mixture was allowed to reach room temperature overnight. The AgNPs were then centrifuged by centrifugation (20 min at 10000 × g).

PVP-coating of AgNPs. The concentrated AgNPs were redispersed in water containing Polyvinylpyrrolidone (PVP, average m.w. 10 kDa) to afford a 50 mL mixture with [PVP] = 6.4 × 10⁻³ M. This mixture was stirred for 30 min. and then centrifuged 1 h at 10000 × g. Most of the supernatant was removed (>40 mL) and the coating procedure was repeated a second time with overnight incubation. The PVP-coated AgNPs were concentrated to approx. 10 mL by centrifugation (1.5 h at 10800 × g) and then washed with water (2 × 50 mL by centrifugation and resuspension). The aqueous AgNP solution was filtered over a 0.2 μm cellulose acetate filter before the last centrifugation. The volume of the final PVP-coated AgNP concentrate was approximately 4 mL. Each resuspension step after centrifugation included 20 min. incubation in an ultrasonic bath.

Ink preparation. 2 mL of aqueous PVP-coated AgNP concentrate were added of 16 mL of water. The AgNP suspension was centrifuged (1 h, 20 °C at 10800 × g), the supernatant removed and the AgNP pellets taken up in 40 mL of 0.2 nm, PDI 0.532, λmax 399 nm (in H2O), TEM: 23.8 ± 4.0 nm.

Femtosecond laser sintering setup. The laser setup consists of a commercial laser source (LightConversion PHAROS, based on Yb:KGW as active medium) which generates ~80 fs-long laser pulses with a repetition rate of 67 MHz, λ = 1030 nm and maximum output power of 2 W. Before reaching the sample, the beam is conditioned through an optical path which includes a software-controlled attenuator and a focalizing objective (Mitutoyo) lens whose magnifying power can be selected between 20X, 50X or 100X. The sample is positioned on a software-controlled moving stage (Aerotech ABL1000) capable of a maximum resolution of 0.05 nm. The AgNP ink is then spincoated at 1000 rpm for 40 s. After laser processing, the sample is rinsed and sonicated for 1 min with deionized water.

Contacts fabrication. Standard glass slides are used as substrate. They are cleaned in an ultrasonic bath with deionized water, acetone, 2-propanol sequentially for 5 minutes each, then oxygen-plasma treated for 1 min (100 W), and finally heated on a hotplate at 60 °C for 5 minutes. The AgNP ink is then spincoated at 1000 rpm for 40 s.

Conductive pattern characterization. Optical images are taken with a Zeiss Axio Scope.A1 microscope (100X objective), AFM images are taken with an Agilent 5500 Atomic Force Microscope and SEM images with a JEOL JSM 6010LV. Electrical characterization is performed using an Agilent B1500A Semiconductor Parameter Analyzer.

Organic FETs fabrication. P(NDI2OD-T2) (purchased from Polyera) is dissolved in mesitylene at a concentration of 5 mg/mL. After fabrication of the bottom contacts via laser sintering, P(NDI2OD-T2) is deposited through bar-coating in air atmosphere, using the same process as described in ref. 2. Then poly(methyl methacrylate) (PMMA) is spun from n-butylacetate (concentration 80 mg/mL) at 1500 rpm for 1 minute. After dielectric deposition, the devices are annealed on a hotplate for 30 min at 80 °C for residual solvent removal. PEDOT:PSS (Clevios P Jet 700) is patterned over the contacts and channel area via inkjet (using a Fujifilm Dimatix DMP-2831). The devices are then annealed at 120 °C in nitrogen atmosphere for 12 h.

Electrical characterization. The devices are measured in nitrogen atmosphere. Static characterization is performed via an Agilent B1500A Semiconductor Parameter Analyzer. Frequency performance was measured using a setup which includes an Agilent ENA Vector Network Analyzer and an Agilent B2912A Source Meter. More details on the setup can be found in Supplementary Information.
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