Low-Temperature Scanning Capacitance Probe for Imaging Electron Motion

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Abstract. Novel techniques to probe electronic properties at the nanoscale can shed light on the physics of nanoscale devices. In particular, studying the scattering of electrons from edges and apertures at the nanoscale and imaging the electron profile in a quantum dot, have been of interest [1]. In this paper, we present the design and implementation of a cooled scanning capacitance probe that operates at liquid He temperatures to image electron waves in nanodevices. The conducting tip of a scanned probe microscope is held above the nanoscale structure, and an applied sample-to-tip voltage creates an image charge that is measured by a cooled charge amplifier [2] adjacent to the tip. The circuit is based on a low-capacitance, high-electron-mobility transistor (Fujitsu FHX35X). The input is a capacitance bridge formed by a low capacitance pinched-off HEMT transistor and tip-sample capacitance. We have achieved low noise level (0.13 e/√Hz) and high spatial resolution (100 nm) for this technique, which promises to be a useful tool to study electronic behavior in nanoscale devices.

1. Introduction

Scanning probe techniques have been of great significance in studying local electronic behavior of a two dimensional electron gas (2DEG) in materials such as graphene [4] and GaAs/Al₅Ga₇As heterostructures [1][2][3]. In these techniques, images of local electron flow were obtained by having a very narrow (20 nm to 1 um) charged AFM tip scanned or positioned directly above the 2DEG while the conductance through the sample [1][4][5], or the capacitance between the sample and tip, is measured [2][3]. The later technique [2][3] uses an STM tip, which is held above the 2DEG surface and is capacitively coupled to the 2DEG immediately below. When a small AC voltage is applied between the tip and the 2DEG, the resulting flow of charge in the gas induces an oscillating image charge on the tip; that oscillation is detected by a sensitive electrometer. This technique can be very useful in mapping the local electron density. In [2][3] the technique was used to understand the Quantum Hall Effect, (QHE) which arises when 2DEG is in a strong magnetic field at low temperatures.

We plan to image the electronic density profile in graphene nanostructures and quantum dots using this technique. These nanostructures will be created on high mobility graphene-on-boron-nitride-sandwich-structures [5] and suspended graphene samples. In this paper, we present the design and
implementation of a cooled scanning capacitance probe that operates at liquid He temperatures to image electron waves in nanodevices. A metal tip is held at 20 nm above the nanoscale structure, and an applied sample-to-tip voltage creates an image charge that is measured by a cooled charge amplifier [2] adjacent to the tip. The circuit is based on a low-capacitance, high-electron-mobility transistor (Fujitsu FHX35X). The input is a capacitance bridge formed by a low capacitance pinched-off HEMT transistor and tip-sample capacitance. We use a sharp metal (tungsten) tip (1um diameter) to create an image charge on a gold plate placed on a SiO2/Si substrate. The tip is scanned at a height 20 nm above the surface of gold plate while the capacitance is measured. A model of the experimental setup was simulated in COMSOL. This model includes a metal sphere of diameter 1 um (analogue of a conducting tip) placed 20 nm above a 15 nm thick conducting metal plate that sits on top of SiO2 substrate. The experimental result and the simulation are compared and agree quite well.

2. Method

We use a scanning probe capacitance microscopy technique to image local capacitance at the scale of nanometers. As shown in figure 1, the technique uses a metal tip scanned above the sample as the capacitance between the tip and sample is measured. The sample consists of a 15 nm thick gold electrode deposited on a Si/SiO2 substrate. The tip was scanned across the edge of this plate so that corresponding change of capacitance can be measured. In addition, another experiment was done where a tip of radius 2.5 um was used. In this experiment, the distance between the tip and sample is varied while the change in capacitance is recorded.

The printed circuit board that holds both the sample and circuit sits on a piezotube that can be controlled electrically to move in x,y and z direction. The tip is held fixed on a support.

Figure 1: Schematic of experimental apparatus. Tungsten tip of diameter 1 um is scanned at 20 nm above a 15 nm gold plate deposited on top of a SiO2 substrate. The amplifier circuit measures the change in capacitance as the tip is scanned. Both the sample and circuit are mounted on a printed circuit board. The inset on the top right shows the SEM of gold plate on Silicon Substrate.

The charge sensing circuit shown in figure 2 uses a capacitance bridge circuit followed by a two-stage common base amplifier circuit. As the experiments need to be performed at low temperatures to
observe quantum mechanical effects, we use High Electron Mobility Transistors for the amplifier circuit. We chose a low noise (0.55 dB @ $f = 12$ GHz) pHEMT for this purpose.

![Schematic of pre-amplifier circuit](image)

**Figure 2:** Left image is the schematic of pre-amplifier circuit. TR1, TR2 and TR3 are High Electron Mobility Transistors. The circuit is a capacitance bridge formed by tip-sample capacitance and a reference capacitor followed by two stage common base amplifiers. The right image is the picture of the circuit on a printed circuit board.

As shown in figure 2, the capacitance between the tip and sample can be modeled as $C_{\text{sample}}$. The transistors TR1, TR2 and TR3 are HEMTs in our circuit. We use TR2 as a reference capacitor by pinching it off as a pinch voltage is applied in $V_{G2}$. The nominal source-drain capacitance for the transistor is 150 fF. As a typical capacitance bridge circuit, an ac voltage $V_{S1}$ is applied to the sample while a second ac voltage $V_{R1}$ is applied to the reference capacitor. The sample voltage $V_{R1}$ is adjusted (both phase and amplitude) such that the voltage at junction node of reference capacitor and sample capacitor is zero. This means that the bridge is balanced and any change in the sample-tip capacitance would bring the bridge off balance and hence a change in voltage at the node.

The two-stage common base amplifier circuit amplifies the small change in voltage. The first stage consists of TR1 and a resistor $R = 470$ kΩ. The value of the resistor was chosen in order to achieve maximum gain at our first stage. The transistor in this stage is operated at saturation point again to maximize gain. The second stage consists of TR3 and a resistor $R = 1$ kohms. The transistor TR3 is biased at triode region to allow maximum current so that it’s enough to drive the long cables coming out of the cryostat amplifier that sits outside the cryostat. The estimated impedance in the cables is about 5 kΩ and hence we set out output impedance of the amplifier to about 2 kΩ. The 100 pF capacitor that sits between the first stage and second stage amplifiers allows us to bias the TR2 as it only allow ac coupling between first stage and second stage circuits. The operating frequency of our experiment is set to 210 kHz (maximum frequency possible in lock-in amplifier) to minimize the 1/f noise in our signal. The bypass capacitor with a value of 100 pF has a lower cut-off frequency of 1 kHz which minimizes attenuation of signal going from stage 1 to stage 2.

The dc voltages that bias the amplifier circuits were generated using a homemade low-noise, battery-operated dc source, shown in figure 3. Two 6V batteries along with two low-noise (15.1 uV rms @ 100 kHz) adjustable output TPS7A30001 dc-dc converters were used. The output of the dc-dc converter was fed to a simple potential divider connected to a unity gain amplifier. Six different
replicas of the circuit were made to create all the necessary biasing/gate voltages for the amplifier circuits.

![Figure 3: Schematic of the dc voltage supply to biasing transistors in the preamp. The circuit consists of dc-to-dc converter that generates 6 V, followed by a potentiometer and a unity gain amplifier.](image1)

The ac voltage source for the amplifier circuit was also homebuilt to achieve a low noise figure. It consists of two 6 V batteries which are connected to a dc-to-dc converter shown in figure 4 to maintain a constant voltage supply. A Wien Bridge Oscillator (I) is used for generating a low-distortion sinusoidal wave. The components are selected such that the frequency is set to 200 kHz ($\frac{1}{2\pi RC}$). This is followed by a buffer amplifier (II) with unity gain to have low output impedance. A phase shifter (III) along with a potential divider (IV) is used for changing the phase and amplitude of the sine wave. Two copies of this circuit are used to generate two ac signals with independently adjustable phase and amplitude needed for the capacitance bridge described earlier.

![Figure 4: Schematic of variable phase and amplitude ac source. The dc-to-dc converter provides a constant power supply to the ac generator circuit. The ac generator circuit consists of four stages. Stage I is a Wien bridge oscillator, that generates sine wave of frequency 210 kHz followed by Stage II, a buffer amplifier. Stage III and IV consists of phase shifting circuit and a buffered potential divider respectively.](image2)

The dc voltage sources and ac voltage sources are put in separate enclosures for preventing ac interference into the dc source. These sources remain outside the cryostat while the preamp operates at liquid helium temperature mounted right on the scanning probe microscope. All the cables that lead to and from the preamplifier circuit are standard coaxial cables. For the purpose of mixing the dc voltage with the ac signal, a simple capacitor resistor junction is used as a mixer.

The input voltage noise of the circuit was obtained by grounding both the input terminals and measuring the output voltage noise using a lock-in amplifier. The input noise measured at the temperature 4.2 K is 20 nV/√Hz. The stray capacitance of the preamp was measured to be 1 pF. The charge noise was obtained by the relation $\Delta Q = C\Delta V = 0.13 \text{ e}^/\sqrt{\text{Hz}}$.

3. Results
3.1. Experimental results:
The experimental result of the two-dimensional capacitance scan over the edge of gold plate is shown in figure 5. The change in capacitance of 30 aF is clearly visible and a step can be noticed right along the edge of the electrode.

![Figure 5: Capacitance-scan of the two-dimensional sample. The height of plot represents change in capacitance (aF) as the tip is scanned at a height of 20 nm on top of the edge of the 15 nm gold plate. The change in capacitance is ~ 30 aF.]

To compute the spatial resolution of our scanning capacitance setup, the capacitance measurements were averaged over a range Δy = 0.30 μm of the flat edge and plotted vs. x in figure 6. The total width of the transition is Δx = 100 nm.

![Figure 6: Capacitance change vs. x averaged between -0.2 μm < y < -0.5 μm. The full spatial width of the capacitance transition is 100 nm.](image)
The change in tip-sample capacitance as the tip is swept over the edge of the conducting sheet is determined by the tip-sample distance. Figure 7 shows the measured tip-sample capacitance measured for 2.5 um radius tip as the tip-sample distance is varied, along with COMSOL simulations of the capacitance between a conducting sphere and plate. As shown, the theoretical and experimental results agree quite well for tip-sample distances less than 200 nm.

Figure 7: The tip-sample capacitance is plotted vs. tip-sample distance. The red curve shows COMSOL simulations while the blue is the experimental result. A tip with diameter 5 um was used.

3.2. Theory and Simulation:

To analyze the capacitive image of the conducting plate edge shown in figures 5 and 6, we used COMSOL simulations of the tip-sample conductance between a conducting sphere and a conducting plate in figure 8. The simulation geometry is shown on the left, where a metal sphere (reddish brown) is located at a distance of 20 nm above a conducting plate (reddish brown), on top of a SiO₂ layer (grey). The right side of figure 8 shows the image charge in the conducting plate, represented by the normal component of electric field at the plate's surface in the simulations. As seen in figure 8, the FWHM of the image charge induced by the voltage on the tip is 210 nm, which gives a spatial resolution of the half width at half maximum HWHM ~ 105 nm. This agrees with the experimental results of the scanning capacitance over the electrode edge.
The agreement between the experimental results and simulation suggests that the technique can image local capacitance with a spatial resolution $\sim 100 \text{ nm}$ when scan is performed at a tip 20 nm above the sample surface, with a tip diameter of 1 um. The noise level of the preamp circuit is $0.1\text{e}^{-}\sqrt{\text{Hz}}$. Future experiments using this setup would be to image electronic density profile in graphene edges or quantum dots [5]. It could equally be used to obtain a high-resolution two-dimensional image of local change in capacitances in other materials. This research was supported by DoE DE-FG02-07ER46422 “Imaging Electrons in Graphene”.

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