A smart method of optimizing the read/write current on PCM array

Yiyun Zhang, Houpeng Chen, Zhitang Song, Xi Li, Rong Jin, Qian Wang, Yuchan Wang, Daolin Cai, and Yueqing Wang

Shanghai Key Laboratory of Nanofabrication Technology for Memory, Shanghai Institute of Micro-system and Information Technology, Chinese Academy of Sciences, Shanghai 200050, P.R. China

a) zhang.yiyun@outlook.com

Abstract: A method for optimizing the read/write current on phase change memory array is proposed. A smart current adjustment circuit is designed to bi-directionally alter the internal read/write current. The best read/write condition based on arrays can be found through this adjustment approach. Example of a 2-dimensional shmoo test on a 16k-bit phase change array implemented in 0.13 µm CMOS technology is given. The resistance distribution can also be roughly obtained. This method, taking advantage of the peripheral circuit, provides statistical yield data on a variety of read/write current, thus offering reliable and helpful indicators for chip parameter setup and process optimization.

Keywords: phase change random access memory, memory array, current adjustment circuit, resistance distribution

Classification: Integrated circuits

References

[1] S. R. Ovshinsky and H. Fritzsche: IEEE Trans. Electron. Devices 20 (1973) 91. DOI:10.1109/T-ED.1973.17616
[2] J. Feinleib, J. deNeufville, S. C. Moss and S. R. Ovshinsky: Appl. Phys. Lett. 18 (1971) 254. DOI:10.1063/1.1653653
[3] M. Gill, T. Lowrey and J. Park: ISSCC Dig. Tech. Papers (2002) 202. DOI:10.1109/ISSCC.2002.993006
[4] S. Lai and T. Lowrey: IEDM Tech. Dig. (2001) 36.5.1. DOI:10.1109/IEDM.2001.979636
[5] K. Lee, B. Cho, W. Cho, S. Kang, B. Choi, H. Oh, C. Lee, H. Kim, J. Park, Q. Wang, M. Park, Y. Ro, J. Choi, K. Kim, Y. Kim, I. Shin, K. Lim, H. Cho, C. Choi, W. Chung, D. Kim, K. Yu, G. Jeong, H. Jeong, C. Kwak, C. Kim and K. Kim: ISSCC Dig. Tech. Papers (2007) 472. DOI:10.1109/ISSCC.2007.373499
[6] J. B. Philipp, B. Ruf, C. Ruster, D. Andres, P. Majewski, M. Kund, T. D. Happ and R. Bergmann: NVMTS (2008) 1. DOI:10.1109/NVMT.2008.4731185
[7] A. Chimenton, C. Zambelli, P. Olivo and A. Pirovano: NVSMW/ICMTD (2008) 49. DOI:10.1109/NVSMW.2008.20
[8] B. Gleixner, A. Pirovano, J. Sarkar, F. Ottogalli, E. Tortorelli, M. Tosi and R. Bez: Reliability Physics Symposium (2007) 542. DOI:10.1109/RELPHY.2007.369948
[9] H. Oh, B. Cho, W. Y. Cho, S. Kang, B. Choi, H. Kim, K. Kim, D. Kim, C.
1 Introduction

Phase change memory (PCM), which takes advantage of its reversible switching characteristic between high resistance in amorphous state and low resistance in crystalline state to realize storage [1], has become a competitive candidate among the non-volatile memory technologies. It has many features such as high speed, small cell size, good cycle ability, low power consumption, low cost and good compatibility with standard CMOS processes [2, 3, 4]. Specifically, when a phase change material is heated to a high temperature with a long-pulse current, it crystallizes and reduces its resistance as SET operation. And a ramp down current is proved to be more effective [5]. To RESET a cell into a high resistance state, a current large enough to melt it is applied for a short period, and then abruptly cut off to quench the material into amorphous phase.

The optimum current used on single phase change cell is not applicable to arrays due to parasitic effects, interference from adjacent cells as well as slight process deviation inside array. Therefore the read/write current of arrays should be carefully selected to achieve optimal yield. So far, there are some researches on phase change arrays, such as write pulse optimization [6, 7] and data retention [8], but not many on both read and write current applied on memory arrays. In this paper, a smart current adjustment circuit is designed to perform the bi-directional read/write current modulation. Accordingly, a 2-D read/write current shmoo test on memory arrays is prone to be built rather than that with specialized test equipment to provide statistical data on yield. Example of a 16k-bit phase change array implemented in 0.13 µm CMOS technology is given. The resistance distribution of SET and RESET operation can also be roughly obtained by the method without specific resistance test pads. Since the optimal read/write current abstracted from the result of arrays is more applicable than that of single cells, this method can offer reliable and helpful indicators for parameter setup and process optimization of subsequent chips.

2 Experimental setup

The 16k-bit PCM array is organized as $128 \times 128$. And the whole array is divided into eight 2k-bit blocks. Each block has a sense amplifier and a write current path, and shares the same bitlines and wordlines. Fabricated in SMIC (Semiconductor Manufacturing International Corporation) 0.13 µm CMOS standard process, the PCM unit is composed of a MOSFET and a phase change cell (1T1R). When a bitline and a wordline are selected, only one path in each 2k-bit block conducts. Eight units are simultaneously in action during an array operation, but they are physically dispersed in eight blocks. So interference from adjacent cells is reduced to the least. Fig. 1(a) is the TEM photograph of the phase change cell.
Single cell tests are operated on the test keys, which are several 1T1R phase change units integrated on the same wafer as the chips, so that they share identical process circumstances. A current-voltage curve for SET is shown in Fig. 1(b), where the current is tested with a continuous but gradually increasing DC voltage applied to the cell. The sharp turn of the curve demonstrates a good characteristic of the material, where the resistance of the phase change cell suddenly goes down, so that the stored data can be distinguished easily. A resistance-current curve for RESET is shown in Fig. 1(c), where current pulses of different amplitudes are imposed on the phase change units. And the pulse width remains 500 ns. The mean value and range of the cell resistance after each operation reveals an apparent resistance rise after pulse of 3.5 mA. The resistance reaches 100 kΩ at the pulse of 4 mA.

![Fig. 1.](image1) (a) TEM photograph of the phase change cell. (b) The I-V curve of PCM test key. (c) The R-I curve of PCM test key.

![Fig. 2.](image2) Current adjustment circuit of (a) write driver and (b) read driver

In the peripheral circuit of PCM chips, the write current is mirrored from the reference current $I_{\text{ref}}$. As shown in Fig. 2(a), the op-amp and NMOS performs as a voltage clamp circuit, so that $V_c$ is clamped to $V_{bg}$, which is a fixed voltage generated from a temperature-independent bandgap. The current varies inversely with the resistance of $R_{\text{ref}}$. In order to adjust the current, an adjustment resistor $R_{\text{adj}}$ is connected to the voltage clamp node $V_c$, and the other end of $R_{\text{adj}}$ is picked out as an external port $V_a$. With different voltages of $V_a$, the current can be flexibly adjusted. If $V_a$ equals $V_c$, the reference current is $V_a/R_{\text{adj}}$. If $V_a$ is less than $V_c$, the current through $R_{\text{adj}}$ will be added to the reference current. If $V_a$ is greater than $V_c$, the reference current will be subtracted by the current through $R_{\text{adj}}$. The reference current is summarized by Eq. (1).

The read current generation is similar to that of the write current, as shown in Fig. 2(b). $V_{\text{cell,c}}$ is the clamp voltage on the PCM array unit, which can be the same as $V_c$ or be specifically set. The gray dotted components represent the equivalent circuit of the reference cell. $R_{\text{ref,eq}}$ represents the equivalent resistance. The sense amplifier compares the current through the equivalent reference cell with that going through the PCM cell. So the
variation of $V_a$ corresponds to the variation of the resistance of the equivalent reference cell.

$$I_{\text{ref}} = \begin{cases} \frac{V_c - V_a}{R_{\text{adj}}} + \frac{V_c}{R_{\text{ref}}}, & V_a < V_c \\ \frac{V_c}{R_{\text{ref}}}, & V_a = V_c \\ \frac{V_c - V_a}{R_{\text{adj}}}, & V_a > V_c \end{cases} \quad (1)$$

In this 16k-bit PCM chip case, $R_{\text{ref}}(w) = R_{\text{adj}}(w) = 6.3 \, \text{k}\Omega$, $R_{\text{ref}}(r) = R_{\text{adj}}(r) = 100 \, \text{k}\Omega$. $R_{\text{adj}}(w)$ and $R_{\text{adj}}(r)$ represent $R_{\text{adj}}$ of write and read current driver respectively, and it is the same for $R_{\text{ref}}$. Different resistances of $R_{\text{adj}}$ provide different precision to adjust the current of both drivers. Yield is tested to evaluate the performance in pace with $V_a$ scanning from the least value. $I_{\text{ref}}$ can be calculated by Eq. (1). Both read and write adjustments cover large scales.

### 3 Results

Fig. 3(a) shows the 2-D yield test result of the 16k-bit PCM chip. The color from light to dark respectively illustrates the bit yield less than 60% to more than 99%. The upper half of Fig. 3(a) shows the SET yield and the lower half shows the RESET yield. The horizontal axis $R_{\text{ref,eq}}$ indicates the equivalent reference resistance. The vertical axis $I_{\text{set}}$ and $I_{\text{reset}}$ represent the real current going through the phase change cell during SET or RESET operation.

![Fig. 3.](image)

Fig. 3. (a) Read/write current shmoo yield test of 16k-bit PCM array (b) Resistance distribution of SET operation (c) Resistance distribution of RESET operation

In the RESET graph, the bit yield reaches a high level at the current of around 3.2 mA. Although the color of some grids are the same, the numerical values demonstrate that the yield reaches peak at around 4 mA, and then decreases with the continuously increase of reset current. An equivalent read reference resistance smaller than 93 k$\Omega$ is low enough to read out “0” in a good efficiency.

In the SET graph, the yield does not appear monotonic as RESET. At the top half of the graph, there is a slightly dark spire. When the SET current is as small as 342 $\mu$A, the cell reaches a low resistance, though not stable enough. When the current increases to 1.4 mA, the yield appears more stable. An equivalent read reference resistance larger than 66 k$\Omega$ reveals a good yield.
With the data analyzed above, it is reliable to choose an optimal read/write current by which both SET and RESET operation can achieve best yield. In this chip, a RESET current of 4 mA, a SET current of 1.5 mA and an equivalent resistance of 70 kΩ are selected (Table I). The SET and RESET bit yield can both reach 99%, and byte yield can also reach 90%. The reason why the yield cannot arrive at 100% lies in the process defect of some anomalous cells.

Several rows of the 2-D shmoo graph are extracted to exhibit the cumulative resistance distribution of SET (Fig. 3(b)) and RESET (Fig. 3(c)) roughly. SET yield denotes the percentage of memory cell, whose resistance is smaller than the intermediate read resistance. So SET yield is approximately equal to the cumulative probability of cell resistance of SET. Similarly, the RESET failure rate is approximately equal to the cumulative probability of cell resistance of RESET. The dotted line through Fig. 3(b) & (c) indicates the selected 70 kΩ read resistance. It locates in the best place where low resistance percentage begins to decrease in SET graph at the left side of the line and high resistance percentage begins to rise in RESET graph at the right side of the line.

Table I. Test range of read/write parameters in the 2D shmoo test of 16k PCM array and the optimal value selected from test results and analysis

| Read/write parameters | Test range | Optimal value |
|-----------------------|------------|---------------|
| I-reset (µA)          | From       | To            | Step | 4000 |
| I-set (µA)            | 25.5       | 4500          | 29   |      |
| R-ref_eq (kΩ)         | 9.5        | 2250          | 11   | 1500 |
|                       | 20.9       | 1556          | Exponentially | 70   |

4 Discussion

The selected RESET current of PCM array is consistent with the test key RESET R-I curve (Fig. 1(c)). But the slightly dark horizontal spire in the result of SET chip performance (Fig. 3(a)) is inconsistent with the test key SET I-V curve (Fig. 1(b)), which has only one sharp turn. The reason lies in two aspects. First, the test of I-V curves uses a step-increasing DC voltage, whose pulse width largely depends on the test equipment. However, the SET operation of array is carried out by a ramp down current pulse with preset height and width in chip test. The different SET modes lead to different inner energy accumulation and structural transformation. Second, the chip test provides statistical results, in which some irregular cases exist, rather than individual cases of a few test keys. From this standpoint, the chip test is more reliable and conforms to reality.

The RESET resistance distribution (Fig. 3(c)) varies greatly between different currents. When RESET current reaches 3.5 mA, the difference becomes smaller again. It means that the energy is already enough to make the material amorphous. But the SET resistance distribution (Fig. 3(b)) shows no big differences between different currents. Since SET operation is concerned with crystallization of GST material, the yield improvement is not only related to current pulse height but also has some connections with pulse...
width and shape. This proposed method can also be used in conjunction with other pulse modulation schemes, such as that in [9], to evaluate the chip performance more precisely.

The proposed method is better to be used in novel PCM unit structures or new kind of phase change materials. Then in the subsequent chips, the new $R_{\text{ref}}$ value can be converted by

$$R_{\text{ref, new}} = \frac{V_c}{I_{\text{ref, selected}}}$$

where $I_{\text{ref, selected}}$ can be calculated from the selected $V_a$ by Eq. (1). As to the 16k-bit array example, $R_{\text{ref, new}}^{(r)} = 217 \text{k}\Omega$, $R_{\text{ref, new}}^{(w)} = 3.7 \text{k}\Omega$. $R_{\text{adj}}$ and $V_a$ can be eliminated. Precisely, write reference resistance can be chosen respectively for SET and RESET. In the case of good process condition, a large range of reference current would make the yield acceptable. Thus several acceptable $R_{\text{ref, new}}$ can be set in chip in the form of options in circuits, such as resistor network or fuse, to modulate slightly around the optimal current. Setting options can also prevent some process deviation in subsequent manufacture. In addition, this method is also feasible for multi-level PCM arrays or extremely large scale memory arrays with proper division of array blocks and suitable sizes of components.

## 5 Conclusion

A smart method for optimizing the read/write current on PCM array is proposed. A current adjustment circuit is designed to achieve the read/write current modulation bi-directionally, which helps to accomplish a 2-D shmoo test of read/write current on 16k-bit PCM. Based on the test data, the optimal read/write condition is found with a RESET current of 4-mA height 200-ns width, a SET current of 1.5-mA height 750-ns width including ramp down and an equivalent read resistance of 70kΩ. Bit yield can reach 99% and byte yield can reach 90% under this condition. The resistance distribution of SET and RESET can also be roughly obtained without specific resistance test pads. This method can be used in conjunction with pulse modulation schemes to avoid line resistance and skewness problems. It is also feasible for extremely large memory arrays with proper division of array blocks and suitable sizes of components. The proposed method provides an intuitional means to reflect the performance of different read/write currents, so as to optimize the yield of PCM array as well as offering applicable and helpful indicators for chip parameter setup and process optimization.

## Acknowledgments

This work was supported by National Key Basic Research Program of China (2013CBA01900, 2010CB934300, 2011CBA00607, 2011CB932804), National Integrate Circuit Research Program of China (2009ZX02023-003), National Natural Science Foundation of China (61176122, 61106001, 61261160500, 61376006), Science and Technology Council of Shanghai (12nm0503701, 13DZ2295700, 12QA1403900, 13ZR1447200).