Erratum: Conductive filament evolution dynamics revealed by cryogenic (1.5 K) multilevel switching of CMOS-compatible $\text{Al}_2\text{O}_3/\text{TiO}_2$ resistive memories (2020 Nanotechnology 31 445205)

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Due to an error in the production an incorrect figure 3 was published. The correct figure 3 is published herein.

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Figure 3. Conduction mechanism analysis of the multilevel switching curves at 1.5 K. (a), (b) $\ln(I)$ vs. $\ln(V)$ plots for the SET and RESET processes in the voltage range of the MR, with the insets showing the results in the voltage range of the IR. All curves in the IR can be linearly fitted with a slope of $\sim 2$, in agreement with the SCLC model. In the MR, only the higher resistance states show linear fits of slope $\sim 4$, which suggests a trap-filling SCLC regime. (c), (d) TAT plots for the SET and RESET processes showing linear fits for the lower resistance states in the MR only. The extracted trap energy barrier values are given for the IRS and LRS. The colored symbols of the $\ln(J)$ vs. $1/E$ and $\ln(I)$ vs. $\ln(V)$ plots indicate when the transport behavior best follows the SCLC model (a), (b) and the TAT model (c), (d).
Conductive filament evolution dynamics revealed by cryogenic (1.5 K) multilevel switching of CMOS-compatible $\text{Al}_2\text{O}_3/\text{TiO}_2$ resistive memories

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Abstract
Non-volatile resistive switching devices are considered as prime candidates for next-generation memory applications operating at room temperature and above, such as resistive random-access memories or brain-inspired in-memory computing. However, their operability in cryogenic conditions remains to be mastered to adopt these devices as building blocks enabling large-scale quantum technologies via quantum–classical electronics co-integration. This study demonstrates multilevel switching at 1.5 K of $\text{Al}_2\text{O}_3/\text{TiO}_2-x$ resistive memory devices fabricated with complementary metal-oxide-semiconductor-compatible processes and materials. The $I-V$ characteristics exhibit a negative differential resistance (NDR) effect due to a Joule-heating-induced metal-insulator transition of the $\text{Ti}_2\text{O}_7$ conductive filament. Carrier transport analysis of all multilevel switching $I-V$ curves show that while the insulating regime follows the space charge limited current (SCLC) model for all resistance states, the conduction in the metallic regime is dominated by SCLC and trap-assisted tunneling for low- and high-resistance states respectively. A non-monotonic conductance evolution is observed in the insulating regime, as opposed to the continuous and gradual conductance increase and decrease obtained in the metallic regime during the multilevel SET and RESET operations. Cryogenic transport analysis coupled to an analytical model accounting for the metal-insulator-transition-induced NDR effects and the resistance states of the device provide new insights on the conductive filament evolution dynamics and resistive switching mechanisms. Our findings suggest that the non-monotonic conductance evolution in the insulating regime is due to the combined effects of longitudinal and radial variations of the $\text{Ti}_2\text{O}_7$ conductive filament during the switching. This behavior results from the interplay between temperature- and field-dependent geometrical and physical characteristics of the filament.

Keywords: $\text{Al}_2\text{O}_3/\text{TiO}_2-x$ memristor, multilevel switching, cryogenic electronics, metal-insulator transition

(Some figures may appear in colour only in the online journal)
1. Introduction

The ever-increasing improvement of nanofabrication processes has led to promising demonstration of high-quality solid-state quantum devices functioning at sub-Kelvin temperatures [1, 2]. Efforts are currently focused towards the development of silicon-based quantum systems that could be operated above 1 K [3, 4]. These works pave the way to truly scalable quantum bit architectures leveraging mature complementary metal-oxide-semiconductor (CMOS) technologies [5]. However, current classical electronic tools and rack-scale instruments used to control few-qubit systems from outside the cryostat cause major scalability, automation and performance issues hindering the fabrication of full-scale quantum computers. Overcoming these roadblocks therefore requires fully integrated cryogenic quantum–classical interfaces able to control qubits from inside refrigerators. Such interface would be composed of CMOS-based digital and analog electronics, enabling mixed-signal control systems [6–10]. In that scope, non-volatile cryogenic memory technologies hold a key role to store data related to qubit states and error correction algorithms. While standard dynamic random-access memory-based cryogenic systems have been investigated at 77 K [11, 12], emerging nanoscale resistive memory devices with better scalability could play a key role to enable large-scale quantum systems.

Resistive random-access memory (RRAM) based on cross-bar arrays of non-volatile resistive memories are considered as prime candidates for next generation high-density data storage applications [13, 14]. Device quasi-static and dynamic non-linearity, multi-bit programming precision and variability are all examples of challenges preventing large-scale adoption of RRAM technology [15]. Additionally, cryogenic applications such as quantum–classical interfaces require low electrical noise and power dissipation. Fundamental investigations have to be conducted on resistive memories in cryogenic conditions to both demonstrate reversible, non-volatile and multilevel resistive switching and to better understand the conductive filament geometry evolution during switching. In recent years, studies on temperature-dependent binary switching behavior and conduction mechanisms of devices based on transition metal oxides have been reported for temperatures down to 4 K [16–24]. However, this temperature remains above the temperature range required by quantum systems (0.02–1.5 K), still preventing any co-integration of those technologies. We recently reported binary resistive switching of Al2O3/TiO2: x/TiN devices at 1.5 K for the first time [25]. At that temperature, such memories based on TiO2 exhibit negative differential resistance (NDR) effects related to a Joule-heating-induced metal-insulator transition (MIT) of the TiO2 conductive filament (CF) [19, 20]. The resulting highly non-linear current-voltage characteristics could be leveraged for the implementation of selector-free multibit memory crossbar arrays [26]. It is now necessary to better understand the switching mechanisms of resistive memories in advanced cryogenic conditions. In the case of TiO2-based devices, their typical gradual multilevel switching behavior must be investigated at 1.5 K in order to harness this property for cryogenic analog memristive-based electronics.

In this work, we report and investigate multilevel resistive switching of TiN/Al2O3/TiO2: x/TiN memory devices conducted at 1.5 K. Full switching cycles are first performed between 300 and 1.5 K, revealing MIT-induced NDR effects below 110 K. Analysis of the current-voltage (I–V) curves are then conducted for the multilevel SET and RESET processes, showing that space-charge limited current (SCLC) and trap-assisted tunneling (TAT) are dominant for specific field ranges and resistance states. While the conductance programming of the device is continuous and gradual in the metallic regime (MR), the insulating regime (IR) is characterized by a non-monotonic conductance evolution. This behavior is further investigated thanks to an analytical model accounting for transport mechanisms, resistance states and NDR effects, all based on a two-phase switching-dependent variable geometry cylindrical CF.

2. Methods

The studied devices are resistive memory crosspoints with a symmetrical 2 µm wide TiN electrode architecture and a switching stack made of Al2O3/TiO2: x. The fabrication process was conducted on thermally oxidized 1 × 1 cm2 silicon substrates. All lithography steps were done using contact ultraviolet (UV) lithography. The 80 nm thick TiN bottom electrodes (BE) were fabricated with a CMOS-compatible damascene process involving UV lithography, plasma etching of SiO2, TiN sputter deposition and chemical-mechanical planarization (CMP). In order to improve the gradual switching characteristics of the devices [27] and reduce leakage current, a 1.4 nm thick layer of Al2O3 was deposited by plasma-enhanced atomic layer deposition at 200 °C with a Picosun R-200 advanced ALD system, using Trimethylalumminium (TMA) as a precursor (pulse/purge time of 0.1/2 s, 14 cycles). The deposition of the 30 nm thick switching layer made of non-stoichiometric TiO2: x was performed by direct current reactive sputtering using a Ti target and an argon-oxygen gas flow rate ratio of 40:2 (scm). The pressure and sputtering power were set to 4.4 mTorr and 150 W respectively. A 15 nm thick Ti layer was then deposited by evaporation on top of the TiO2: x switching material in order to create an oxygen vacancy gradient beneficial for the switching performance. This layer also acts as a trapping layer for the diffusing oxygen ions. Finally, the 220 nm thick TiN/Al top electrodes (TE) were fabricated by evaporation. Figure 1(a) shows a schematic cross-section detailing the thicknesses of all materials.

Measurements were conducted on two devices from 300 to 1.5 K with an Agilent E5270B parametric measurement in a Janis variable temperature insert (VTI) cryostat. For all measurements, the BEs were grounded and the signals were applied to the TEs. Prior to any resistive switching, a current-controlled forming process was conducted with a compliance of \( I_c = 500 \mu A \). The average resistance of the BEs and TEs.
were measured at each temperature, allowing the calculation of the voltage $V_{\text{mem}}$ across the switching region by subtracting the drop of voltage $V_{\text{applied}}$ from the applied voltage $V_{\text{mem}}$ across the device.

### 3. Results and discussion

Figure 1(b) shows binary resistive switching operations performed at 300 and 1.5 K, with the current plotted against $V_{\text{mem}}$ data. The $I$–$V$ characteristics at 300 K are typical of TiO$_2$-based devices with gradual SET/RESET processes [28]. The highly nonlinear curves and NDR effects observable at 1.5 K are caused by the Joule-heating-induced MIT of the Magnéli phase Ti$_2$O$_7$ inside the CF [19, 25], known to occur in the temperature range of 120–155 K [29, 30]. The temperature-dependent $I$–$V$ curves of a device in low-resistance state (LRS) depicted in figure 1(c) allow to pinpoint the critical cryostat temperature of $T_c \approx 110$ K.

Multilevel resistive switching operations are then successfully performed at 1.5 K, as shown in figure 2(a). The multilevel SET process is achieved with current-controlled incremental switching where $I_{\text{applied}}$ goes from 0.8 mA to 2.5 mA with a step of $\Delta I_{\text{SET}} = 0.1$ mA. The current-controlled method allows to avoid any abrupt growth of the CF induced by a positive feedback effect during the SET operation [31], thus promoting a more gradual switching and better endurance. The multilevel RESET procedure is then conducted by voltage-controlled incremental switching with $V_{\text{applied}}$ comprised between $-2.5$ V and $-5$ V with a step of $\Delta V_{\text{RESET}} = -0.25$ V. This corresponds to a voltage $V_{\text{mem}}$ across the device of $-0.48$ V and $-1.61$ V respectively. The values of differential conductance $dI/dV$ measured at $V_{\text{applied}} = 0.47$ V visible in figure 2(a) range from 335 $\mu$S to 1420 $\mu$S during the multilevel SET, then go from 1337 $\mu$S to 470 $\mu$S during the multilevel RESET. The insets illustrate the $I$–$V$ curves for the SET and RESET processes in semi-logarithmic scale centered on the NDR effects. One can notice a non-monotonic and partly inverse conduction evolution (ICE) in the IR with respect to the continuous conductance increase in the MR for both SET and RESET procedures. For the SET process, the high-resistance state (HRS) in the MR indeed corresponds to an intermediate-resistance state (IRS) in the IR (point A), while an IRS in the MR corresponds to the LRS in the IR (point B). Regarding the RESET process, the LRS and HRS in the MR become respectively the IRS and LRS in the IR (points D and E).

To better illustrate this behavior, figure 2(b) shows the differential conductance values in the IR and the MR measured at 0.2 V and 0.47 V respectively for each multilevel switching cycle. As previously mentioned for TiO$_2$-based memory devices, the multilevel conductance evolution in the MR exhibits a continuous and gradual increase (decrease) during the SET (RESET) process. However, in the IR the conductance exhibits a non-monotonic evolution, where its value first increases from 10.3 $\mu$S up to 13.5 $\mu$S (points A and B), then decreases down to 8.6 $\mu$S revealing the ICE compared to the MR (point C), to finally increase again up to 9.3 $\mu$S (point D). Regarding the RESET process, the conductance first decreases slightly down to $\sim 9$ $\mu$S, only to increase after the 8th RESET operation to reach 11.4 $\mu$S (point E). These observations indicate that for a reliable read and usage of the conductance state in the scope of cryogenic high-density memory applications, the read voltage $V_{\text{READ}}$ should be carefully chosen to be both in the MR and below the writing voltage $V_{\text{WRITE}}$.

In order to better understand the difference in the conductance evolution between the insulating and metallic regimes of the device, we perform a conduction mechanism analysis based on the $I$–$V$ curves of the multilevel resistive switching at 1.5 K. Similarly to previous transport analysis conducted on TiO$_2$-based devices at low temperature [25, 32], we found

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**Figure 1.** (a) Schematic cross-section view of the resistive memory studied. (b) Semi-logarithmic plot of resistive switching cycles performed at 300 K (red lines) and 1.5 K (blue lines). The bottom left inset shows the forming process with a current compliance of $I_f = 500$ $\mu$A. The schematics in the bottom right corner illustrates the crosspoint structure. (c) $I$–$V$ curves for LRS in function of $V_{\text{mem}}$.
that SCLC and TAT are the dominant conduction mechanisms. Figure 3 shows the results of the \( \ln(I) \) vs. \( \ln(V) \) and \( I/E \) plots, corresponding to the SCLC and TAT models respectively, where oxygen vacancies act as traps and whose current density is described as [33]

\[
J_{\text{SCLC}} = \frac{9}{2} \varepsilon_0 \varepsilon_r \mu \theta \frac{T^2}{L^2} \tag{1}
\]

and

\[
J_{\text{TAT}} = A \exp \left( -\frac{8 \pi \sqrt{3 q m^*}}{3 h} \Phi_T^{3/2} \right). \tag{2}
\]

Here, \( \varepsilon_0 \) is the vacuum permittivity, \( \varepsilon_r \) is the dielectric constant of the switching stack, \( \mu \) is the electron mobility, \( \theta \) is the ratio of free and shallow trapped charge, \( L \) is the thickness of the active stack, \( A \) is a constant, \( q \) is the electronic charge, \( m^* \) is the effective mass of the electron in the oxide \((\sim 9 m_0)\) for the electrons in TiO\(_2\) [34], \( h \) is the Planck’s constant, \( E \) is the electric field and \( \Phi_T \) is the energy of the trap below the oxide conduction band minimum. The linear fits of the \( \ln(I) \) vs. \( \ln(V) \) plots of the multilevel SET and RESET processes depicted in figures 3(a) and (b) can be described by \( I \propto V^m \), where the index \( m \) is the slope of the fit. These results suggest that SCLC is dominant in all resistance states at low bias (i.e. insulating regime, see insets), but only in high-resistance states at high bias (i.e. metallic regime). In the IR, the slope of \( m \approx 2 \) indicates that the current level is controlled by the oxygen vacancies acting as traps \((I \propto V^2)\). The slope of \( m \approx 4 \) in the MR indicates that the conduction is governed by the power law \( I \propto V^m \), corresponding to the SCLC model where the traps are being filled. According to the \( \ln(I) \) vs. \( I/E \) plots for the MR shown in figures 3(c) and (d), the dominant transport mechanism gradually changes from trap-filling SCLC to TAT as the resistance state gradually change from HRS to LRS. This transition could be explained by the increase in length of the conductive filament during the multilevel switching, which seems to remain only partially formed even after the last SET process. As the gap between the tip of the CF and the bottom electrode closes, the trap-controlled transport of the electrons is replaced by a single trap-assisted tunneling event. Using the slope of the fits and the equation (2), trap energy barrier values of around 16 and 21 meV were extracted for IRS and LRS respectively. These values are in agreement with previous studies on similar devices characterized at 1.5 K [25].

Following these experimental results, a current-controlled conduction model accounting for the MIT-based NDR effects and the different resistance states was employed in order to gain further insights into the ICE between the IR and MR. This model is based on a 2D analytical approach initially developed by Pickett et al [19]. Figure 4(a) illustrates one half of the system considered, along with the corresponding equivalent circuit diagram. The system is composed of a cylindrically symmetric CF of length \( L_{CF} \) and radius \( r_{CF} \), separated from the bottom electrode by a gap of length \( w \). The MIT contribution to the model comes from the CF being considered as a two-phase channel made of a self-heating metallic core of radius \( r_{met} \) and resistivity \( \rho_{met} \), surrounded by an insulating shell of radius \( r_{ins} \) and resistivity \( \rho_{ins} \) and thermal conductivity \( \kappa \). The normalized radius of the CF can be defined as \( u = r_{met}/r_{CF} \). The current- and temperature-dependent variation of \( u \) is described by

\[
u(I_{mem}, T_{amb}) = \exp \left( \frac{1}{2} W_0 \left( \frac{4 \pi \kappa \rho_{met}}{\kappa_{back} \rho_{mem}} \right) \right) \tag{3}
\]
Figure 3. Conduction mechanism analysis of the multilevel switching curves at 1.5 K. (a, b) \( \ln(I) \) vs. \( \ln(V) \) plots for the SET and RESET processes in the voltage range of the MR, with the insets showing the results in the voltage range of the IR. All curves in the IR can be linearly fitted with a slope of \( \sim 2 \), in agreement with the SCLC model. In the MR, only the higher resistance states show linear fits of slope \( \sim 4 \), which suggests a trap-filling SCLC regime. (c, d) TAT plots for the SET and RESET processes showing linear fits for the lower resistance states in the MR only. The extracted trap energy barrier values are given for the IRS and LRS. The colored symbols of the \( \ln(J) \) vs. \( 1/E \) and \( \ln(I) \) vs. \( \ln(V) \) plots indicate when the transport behavior best follows the SCLC model (a, b) and the TAT model (c, d).

where \( W_0(x) \) is the zero-branch Lambert \( W \) function, \( T_{\text{MIT}} \) and \( T_c \) are the MIT and cryostat temperatures respectively and \( I_{\text{mem}} \) is the imposed current inside the memristor \([19]\). The conduction mechanism inside the CF is considered to be Ohmic, such as

\[
V_{\text{CF}}(I_{\text{mem}}, u) = R_{\text{CF}}(u) \cdot I_{\text{mem}} = G_{\text{CF}}(u)^{-1} \cdot I_{\text{mem}} \tag{4}
\]

where \( V_{\text{CF}} \) is the voltage across the CF and \( R_{\text{CF}} \) is the total resistance of its two cylindrical phases. In this case, the conductance \( G_{\text{CF}}(u) \) is described by

\[
G_{\text{CF}}(u) = \frac{\pi r_{\text{CF}}^2}{L_{\text{CF}}} \left( \frac{u}{\rho_{\text{met}}} + \left( \frac{1-u}{\rho_{\text{ins}}} \right)^2 \right). \tag{5}
\]

Based on the previous carrier transport analysis results, the gap of length \( w \) is considered as an oxygen vacancy-rich cylindrically symmetric suboxide of radius \( r_{\text{CF}} \), whose conduction behavior follows the SCLC model for all resistance states at low current (i.e. in the IR and just after the NDR effect). Using equation (1), the corresponding voltage \( V_{\text{subox}} \) that depends on the gap \( w = D_{\text{mem}} - L_{\text{CF}} \) is expressed by

\[
V_{\text{subox}} = \sqrt{\frac{8 I_{\text{mem}} (D_{\text{mem}} - L_{\text{CF}})^2}{9 \pi r_{\text{CF}}^2 \rho_{\text{met}}^2 \mu \theta}}. \tag{6}
\]

As depicted in the equivalent circuit shown in figure 4(a), the total voltage \( V_{\text{mem}} \) seen by the switching stack during a current-controlled NDR is thus defined by \( V_{\text{mem}} = V_{\text{CF}} + V_{\text{subox}} \). Figure 4(b) shows theoretical \( I-V \) curves calculated with the model compared to experimental data of multilevel SET operations exhibiting NDR effects at 1.5 K. The model successfully reproduce the overall behavior observed in figure 2, namely the non-monotonic conductance evolution in the IR and the continuous conductance increase in the MR. Best fitting physical and geometrical parameters are given in table 1 \([29, 35, 36]\). The \( L_{\text{CF}} \) and \( R_{\text{CF}} \) values used to fit the different resistance states are visible in figure...
4(c). Additionally, the contributions of the CF and the suboxide to the normalized total voltage drop $V_{\text{mem}}$ across the device are plotted in figure 4(d) for each resistance state. The data depicted in figures 4(c) and (d) suggest that difference in conductance evolution between the IR and the MR originates from the interplay between the geometry and the MIT-driven conduction state of the CF. Indeed, the initial conductance increase from HRS to IRS1 (points A and B in figure 2(b)) observable for both conduction regimes of the CF can be explained by an increase of its radius $r_{\text{CF}}$, accompanied by a slight decrease of its length $L_{\text{CF}}$. This behavior leads to an increase of the section $S = \pi r_{\text{CF}}^2$ of the CF, resulting in an increase of the conductance of the device. After the IRS1, one can notice that the subsequent multilevel SET operations induce both an increase of $L_{\text{CF}}$ and a decrease of $r_{\text{CF}}$. In the IR, the CF is the main contributor to the total voltage drop $V_{\text{mem}}$ (see figure 4(d)) due to its insulating phase having a higher resistivity than the suboxide. Hence, the growth of the CF provokes a decrease in conductance in this case. However, the opposite behavior is observed in the MR, because of the highly conducting state of the CF in this regime, as illustrated by its negligible contribution to the voltage $V_{\text{mem}}$ compared to the suboxide (figure 4(d)).

The way $L_{\text{CF}}$ and $r_{\text{CF}}$ evolves during the multilevel switching stems from a competition between thermal- and field-activated effects [37] exacerbated at low temperature. The widening of the CF between HRS and IRS1 is the result of the strong self-heating-induced temperature gradient between the CF and the rest of the active junction at 1.5 K. This phenomenon activates the diffusion of the oxygen vacancies in the vicinity of the TE towards the center of the CF due to the Soret effect [38]. At such low voltage, this results in an increase
of the CF radius in the absence of any field-induced drifting towards the BE. However, from IRS1, the increasingly high applied fields force the thermoactivated oxygen vacancies to drift, which leads to a rapid growth of the CF characterised by a decrease of $r_{CF}$. From these elements, we can assume that the increase in conductance observed at the end of the SET procedure in the IR (points C and D in figure 2(b)) could be attributed to a new widening of the CF induced by the thermal field-assisted accumulation of oxygen vacancies. Similarly, the ICE observed during the multilevel RESET process is in agreement with the expected shrinking and widening of the CF.

4. Conclusions

We report successful multilevel resistive switching of CMOS-compatible TiN/Al2O3/TiO2/Ti/TiN memory devices at 1.5 K, exhibiting a Joule-heating-induced MIT at a critical ambient temperature of 110 K. The conductance increase/decrease in the metallic regime is continuous and gradual, contrary to the insulating regime characterized by a non-monotonic conductance evolution. The carrier transport analysis shows that the main conduction mechanisms in the partially formed filament are SCLC and TAT, the latter being only dominant in the metallic regime for low-resistance states. These results represent direct observations of the interplay between the Joule-heating-dependent conducting regimes and the geometry evolution of the filament, which are respectively impacted by the applied field range and the switching process. The implementation in an analytical model of the transport mechanisms, the MIT-based NDR effects and the geometry-driven conductance states of the filament allows to calculate I–V characteristics with conductance evolution behaviors in good agreement with experimental measurements. This approach reveals both longitudinal and radial evolution dynamics of the conductive filament, resulting from a competition between the diffusion and drift phenomena of oxygen vacancies induced by the strong temperature gradient (Soret effect) and the increasingly high applied electric field respectively. Our study in cryogenic temperature conditions of multilevel resistive switching of TiO2-based devices exhibiting MIT sheds new light on the switching mechanism in oxide-based memories, while highlighting the potential of such highly scalable devices for on-chip cryogenic high-density memory.

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