Fast Modeling L2 Cache Reuse Distance Histograms Using Combined Locality Information from Software Traces

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Abstract—To mitigate the performance gap between the CPU and the main memory, multi-level cache architectures are widely used in modern processors. Therefore, modeling the behaviors of the downstream caches becomes a critical part of the processor performance evaluation in the early stage of Design Space Exploration (DSE). In this paper, we propose a fast and accurate L2 cache reuse distance histogram model, which can be used to predict the behaviors of the multi-level cache architectures where the L1 cache uses the LRU replacement policy and the L2 cache uses LRU/Random replacement policies. We use the L1 reuse distance histogram and two newly proposed metrics, namely the RST table and the Hit-RDH, that describing more detailed information of the software traces as the inputs. The output of our model is the L2 cache reuse distance histogram, based on which the L2 cache miss rates can be evaluated. We compare the L2 cache miss rates with the results from gem5 cycle-accurate simulations of 15 benchmarks chosen from SPEC2006. The average absolute error is less than 5%, while the evaluation time can be sped up by 7.38 times. We also extend our model into a multi-core architecture in which two cores share a unified L2 cache. The error of our model in this case is less than 7%.

Keywords—Analytical model, Reuse distance histogram, Stack distance histogram, Multi-level caches.

I. INTRODUCTION

As the speed gap between the CPU and the main memory keeps increasing, multi-level caches are widely utilized in modern processors to improve the performance. Considering the high accuracies, in many early studies, researchers prefer to use cycle-accurate simulators to evaluate their designs [1]. However, as the complexity of architecture design spaces and the size of workloads are continuously growing, the simulation time is becoming unacceptably high. Compared with cycle-accurate simulations, analytical models can provide faster performance estimations and architectural insights. They are normally based on software statistical information profiled from the workload traces. Since caches exploit memory accessing localities, Reuse Distance Histogram (RDH) and Stack Distance Histogram (SDH), which can be profiled by a binary instrumentation tool, have become the most important metrics for analytical models of caches with Random and LRU replacement policies [2][3]. However, because the profiled histograms merely reflect the memory accesses to the L1 caches, these two metrics cannot be directly used to predict behaviors in the downstream caches, i.e., the L2 and L3 caches.

In previous researches, there are many analytical models proposed to evaluate the performance of different cache architectures [4][5]. However, most of these models use pure probability formulas to predict the behaviors of a certain level cache, in which mathematical expectations and constant ratios are widely used instead of more accurate probability distributions. In fact, these values or probabilities used to describe the software trace information are closely related to the workloads. Using constant values in the model is inaccurate and cannot reflect the details of the distance histograms and, thus, brings large errors. That is the reason why most previous models only provide the cache miss rates of the target caches without more insightful distance histograms. Furthermore, their models usually require the replacement policy of the target cache being LRU. Because as long as the proportion of the references with stack distances less than the associativity is accurate, the miss rate of an LRU cache can be calculated easily and accurately. Therefore, the accuracies of these miss rate models are not sensitive to the precisions of the distance histogram. For example, Fig. 1 gives the L1 SDH of cactusADM from SPEC2006 predicted by StatStack [5] from the L1 RDH. Although StatStack can give the accurate prediction of the miss rate, the distance histogram shown in Fig. 1 is not accurate enough. The predicted histogram has a high peak around 25, but the peak appears around 50 in the actual distance histogram with a significantly lower height. However, because the proportion of references with the stack distance less than the associativity (4-way, in this example) is similar, the miss rates calculated by two distances histograms are also similar (actual miss rate: 0.0247; predicted miss rate: 0.0202).

Fig. 1. L1 SDH from StatStack
In addition, the profiled information used in previous models is either RDH or SDH, without any combinations of these two metrics. However, a single RDH or SDH is incapable to describe all information of the software traces. RDH cannot be directly used to analyze the “filter effect” of the L1 LRU cache because only the stack distance of a reference can be utilized to determine whether it is missing in the LRU cache. SDH, on the other hand, filters identical references in a reuse epoch and cannot be directly used to derive the L2 RDH.

Based on the above considerations, it is not enough to analyze the L2 RDH merely through the L1 RDH or the L1 SDH due to their incompleteness. In this paper, we propose two new metrics, namely the Reuse-and-Stack-Transfer (RST) table and Hit-RDH, to describe more detailed information of the software trace from CPU. Our model, which takes L1 RDH, RST table, Hit-RDH and corresponding cache parameters as inputs, can infer the accurate L2 RDH without the detailed simulations of the cache architecture. With the help of StatCache [4] and StatStack [5], the L2 RDH can be used to calculate the L2 cache miss rate for L2 Random cache and L2 LRU cache, respectively. We also give an application case study of our model in a multi-core scenario. In this application case, we use our model to predict the L2 RDHs of each core and merge them into the unified L2 RDH of the shared L2 cache by StatCC [6], from which the miss rate can be predicted.

Our work improves the related works in the following two aspects:

- Proposing two new metrics to describe more detailed information of software traces, which can be profiled from conventional method without significant time overhead.
- Providing an analytical model, which is more accurate and more time efficient than prior probability models, to derive the L2 RDH from L1 RDH that can be used to predict the corresponding L2 cache miss rate.

The rest of the paper is organized as follows: Sections 2 introduces the related works. Section 3 reviews the background of the analytical model for caches. Section 4 introduces two new metrics for describing the information of software traces. In section 5, we propose an analytical model equation set to predict the L2 RDH. In section 6, we give the solution for the scenarios when the L1 cache and the L2 cache have different number of cache sets. The evaluation results of our model are exhibited in section 7. Section 8 provides an application case of our model in a multi-core system. Section 9 concludes this paper.

II. RELATED WORKS

The related cache modeling methodologies can be divided into two parts. The first part is for the models that focus on one certain level caches, especially the L1 cache. Erick Berg et al. [4] presented an analytical model, StatCache, to estimate the L1 cache misses with the Random replacement policy. This model is fed with the RDH profiled from the memory references. It is basically composed of two equations forming an equation set. By solving the equation set, we can get the miss rate of the Random cache. David Eklov et al. [5] developed StatStack model to convert the RDH into the SDH from which the L1 LRU cache misses can be predicted. Xiaoyue Pan et al. [7] provided a framework based on the Markov chain to predict the cache misses under three replacement policies, namely Random, LRU and PLRU. For the out-of-order processors, K Ji et al. [8] used artificial neural networks to address the effects of the stack distance migration that caused by out-of-order executions.

The second part is for the models for multi-level cache architectures. K Ji et al. [9] [10] used the L1 cache SDH to predict the multi-level cache misses based on a total probability formula. It considers all the possible situations of distance distributions in a reuse epoch, which makes the complexity of the algorithm extremely high. Jasmine Madonna S et al. [11] proposed an analytical model to calculate the L2 cache miss rate based on the analysis of the influence of inclusive/exclusive relationship between the L1 cache and the L2 cache. Nevertheless, the output of their model only gives the L2 miss rate without the more insightful L2 RDH. In addition, the above two models can only be applied in an LRU-LRU multi-level cache architecture. Venkatesh T G et al. [12] and David Eklov et al. [6] have proposed methods to construct the L2 shared cache RDH. However, the inputs of their models are profiled from the direct upstream cache instead of the CPU, which can only be obtained via the time-consuming simulations of the multi-level cache architecture.

In our previous work [13], we put forward a new metric to describe the characteristics of software traces, by which the proposed model can get a relatively accurate L2 RDH under the low L1 miss rates scenarios. However, the model requires that the L1 cache and the L2 cache have the same number of cache sets, which limits the usage scope of the model in real processor architectures. To overcome these constrains, we refine this model in this paper and extend our model into a multi-core scenario.

III. BACKGROUND

Before we introduce the new metrics and our model, we first need to review some basic terminologies used in our following discussions.

**Reuse distance**: The reuse distance is the number of references between two consecutive references accessing to the same cache line. If the cache line is accessed for the first time, its reuse distance is defined as infinite. For example, the reuse distance of the second A in Fig. 2 is 5 (there are five references, \(x_1, x_2, x_3, x_4\) and \(x_5\), between the two ‘A’s’).

![Fig. 2. A reuse epoch](image-url)
Stack distance\(^1\): The stack distance is the number of distinct references between two consecutive references accessing to the same cache line. In Fig. 2, the stack distance of the second A is 3 (There are three distinct references, \(x_2, x_4\), and \(x_5\), between the two ‘A’s).

Reuse/Stack Distance Histogram (RDH/SDH): The RDH/SDH records the numbers of references for each reuse/stack distance in the memory traces.

Reuse epoch: A reuse epoch is the cache accessing history between two consecutive references accessing the same cache line, such as the reuse epochs formed by the two ‘A’s (\(x_1, x_2, x_3, x_4\), and \(x_5\)) and the two ‘B’s (\(x_2, x_3\), and \(x_4\)) in Fig. 2.

Our model is fed with the L1 RDH and the newly introduced RST and Hit-RDH metrics. Our model outputs the predicted L2 RDH, which is injected into the L2 cache. Based on the replacement policy the L2 cache applied, we can use StatCache or StatStack to calculate the miss rate of the L2 cache.

IV. RST Table and Hit-RDH

In previous studies, the stack distance theory \([5]\) is the most important method to analyze the performance of the LRU cache. For the Random caches, StatCache \([4]\) is used to calculate the miss rate based on the RDH. These methods only output the cache miss rates and none of them analyze the “filter effect” of the L1 cache. The information of the software traces will be changed after accessing the L1 cache because some memory references may hit in the L1 cache and be filtered from accessing the L2 cache. However, the memory traces, or the distance histograms, which are normally profiled by a binary instrumentation tool, only reflect the memory accesses to, instead of from, the L1 cache. Therefore, prior models are very limited in the L2 cache modeling.

To describe the “filter effect” of the L1 cache, we propose two new metrics, namely the Reuse-and-Stack-Transfer (RST) table and Hit-RDH in this paper. RST table is a two-dimensional matrix, which records the information of the RDH and the SDH in a given trace profiling interval in the L1 cache.

\[ Prs[i][j] = \frac{RST[i][j]}{\sum_{k=0}^{i} RST[i][k]} \]  

(1)

For each memory reference in a profiling interval, we can easily calculate its reuse distance and stack distance by maintaining two reference queues for each cache set. As shown in Fig. 5, if cache reference \(A\) comes, we first search the reuse reference queue in reverse order to find if the reference \(A\) has been accessed in recent history. To get the reuse distance of the newly coming \(A\), we just count the number of references between these two references of \(A\). Then, we insert this \(A\) to the reuse reference queue. If we want to get the stack distance, we first need to do the same steps as the reuse distance. Then, we delete the reference \(A\) found in the recent history (evicting the previous reference \(A\) we found in the stack reference queue). Based on this method, we can get the reuse distance and the stack distance for each memory reference and construct the RST table. More details about the extraction of the reuse distance and the stack distance could be found in \([9]\) \([14]\).

\(^1\)Some prior researchers also define the stack distance as “reuse distance”. However, we restrictively distinguish these two concepts in our paper.
Another metric introduced in this paper, called Hit-RDH, is also a two-dimensional matrix. Fig. 6 shows an example of Hit-RDH. The red circle in Fig. 6 means that in all the reuse epochs with the reuse distance of 4, the number of reuse epochs that have 2 references hitting in the L1 cache is 310. In other words, in each of these 310 reuse epochs, there are 2 references hitting in the L1 cache. By using the same method as constructing the RST table, we just need to compare the stack distance with the L1 associativity every time we update the RST table and add a hit flag for the current reference in the references queue. When a reference comes, the hit number is the number of references with hit flag between its reuse epochs. We can accumulate the element HitRDH[rd][hit number] by one, in which rd is the reuse distance of the reuse epoch. By the Eq. (2), we can also get the distribution of the number of references hit in the corresponding reuse epoch, called \( P_{\text{hit}} \).

\[
P_{\text{hit}}[rd][n] = \frac{\text{HitRDH}[rd][n]}{\sum_{k=0}^{\text{rd}} \text{HitRDH}[rd][k]}
\]

V. L2 CACHE RDH MODEL

To simplify our discussion of the L1 cache “filter effect”, we first assume that: (1) the L1 cache equips with the LRU replacement policy; (2) the L1 cache and the L2 cache have the same number of sets (we will extend out model to different L1/L2 sets in section VI). Based on the stack distance theory, if the stack distance of a reference is larger than or equal to the LRU-cache associativity, the reference must be a cache miss. In other words, the references with stack distance smaller than the L1 associativity will hit in the L1 cache without accessing the L2 cache. However, we cannot derive the L2 RDH directly from the L1 SDH because the SDH does not record the information about how many times a certain reference is reused in a reuse epoch. For example, Fig. 7 shows a reuse epoch of \( A \). We assume that the L1 associativity is 2. References \( x_0 \) and \( x_6 \) construct the reuse epoch of \( A \). The references \( x_3 \) will hit in the L1 cache because the stack distance of \( x_3 \) is 4, which is less than the L1 associativity. Although reference \( C \) has appeared twice (reference \( x_2 \) and reference \( x_5 \)), reference \( x_5 \) will still be a miss because its stack distance is 2. Based on the above analysis, only reference \( x_3 \) hits in the L1 cache and others will be leaked to the L2 cache. If the references \( x_0 \) and \( x_6 \) miss in the L1 cache, the reuse distance of the second reference \( A(x_6) \) in the L2 cache is counted by the references in the reuse epoch missing in the L1 cache, i.e., the reuse distance of the second A in the L2 cache is 4.

If we want to predict the L2 RDH from the distance information of the L1 cache, for a reuse epoch of a reference in the L1 cache, we have to know how many references hit (or miss) in the L1 cache. Then, we can calculate the number of references leaked into the L2 cache and the corresponding reuse distance of the L2 cache. However, by the L1 SDH, the stack distance of a reference is not the total number of the references in its reuse epoch, which means we are unable to calculate the reuse distance of the L2 cache by judging how many references are missing in the L1 cache. For example, the stack distance of the second \( A \) in Fig. 7 is 3 (there are 3 distinct references, i.e., \( B \), \( C \) and \( D \), between two \( A \)s), and there is only one reference, \( x_3 \), hitting in the L1 cache. However, we cannot get the L2 reuse distance of the second \( A \), which is 4 in this case, merely based on the stack distance information. Therefore, the only way to calculate the reuse distance of L2 cache is that we get the reuse distance of the reuse epoch of a reference and determine how many references in this reuse epoch are missing.

In our model, for a reference in the L1 cache, we first use the \( Prs \) table to get a distribution of its possible stack distances. By the definition of \( Prs \) table, we know \( RDH(i) \times Prs[i][j] \) denotes how many references with the reuse distance of \( i \) have the stack distance of \( j \), where \( RDH(i) \) is the appearance number of references with the L1 reuse distance of \( i \) and \( Prs[i][j] \) can be considered as the ratio that the references with the reuse distance of \( i \) and the stack distance of \( j \). If \( j \) is smaller than the L1 associativity, \( RDH(i) \times Prs[i][j] \) references will hit in the L1 cache and not be leaked into the L2 cache. We subtract the number of the L1 hit references from each \( RDH(i) \), as Eq. (3) shows, to get an intermediate histogram \( MissRDH \).

\[
MissRDH(i) = RDH(i) \times \left( 1 - \sum_{j=0}^{L1\text{-assoc}-1} Prs[i][j] \right)
\]

Note that \( MissRDH \) is not the L2 RDH yet, which only reduces the number of the references of each reuse distance in the L1 RDH. For example, for a given L1 reference with reuse distance of \( i \), if there is one L1 cache hitting in its reuse epoch, the \( MissRDH(i) \) will be adjusted to \( MissRDH(i) = RDH(i) - 1 \). However, the actual \( L2RDH(i-1) \) should be increased by one because the reuse epoch with L1 reuse distance \( i \) now is changed to a L2 reuse epoch with reuse distance of \( i-1 \). Therefore, to get the L2 RDH, we still need to adjust the number of each reuse distance. Some references
with higher reuse distance may be counted to lower reuse distance in L2 cache, as shown in the step 2 of Fig. 6.

After the step 1 in Fig. 8, the value of each point in the MissRDH is the number of references with the original corresponding reuse distance that are misses in the L1 cache, but the actual reuse distance of these references in the L2 cache have not been adjusted because of the “filter effect”. In step 2, we use the proportion $P_{hit}$ to adjust MissRDH. By the definition, $P_{hit}[rd][n]$ means that in all the reuse epochs with the reuse distance of $rd$, the proportion of how many reuse epochs have the number of hit references of $n$ in their reuse epochs. If the reuse distance of a reuse epoch in the L1 cache is $rd$ and the reuse distance in the L2 cache is $i$, that means there are $rd - i$ references in the reuse epoch will hit in the L1 cache and the ratio of these references is $P_{hit}[rd][rd - i]$. Eq. (4) shows the way to get the L2 RDH from MissRDH. In this equation, $MissRDH(rd) \times P_{hit}[rd][rd - i]$ means that in all reuse epochs of the references with the reuse distance of $rd$ (the number is $MissRDH(rd)$), the probability of these reuse epochs have the number of $rd - i$ hit references is $P_{hit}[rd][rd - i]$. In other words, there are averagely $i$ references missing in the L1 cache for each reuse epoch with the reuse distance of $rd$. The number of references miss in the L1 cache construct the reuse distance of the reuse epoch in the L2 cache, as Fig. 9 shows. In Fig. 9, we assume that the references at both ends (two references of $A$) are missing in the L1 cache. Reference $x_3$ and reference $x_6$ hit in the L1 cache and will not access the L2 cache. Other references ($x_1, x_2, x_4, x_5$) are missing in the L1 cache and accessing the L2 cache, which construct the reuse epoch in the L2 cache. After accumulating all the number of reuse epochs which may have the number of L2 hit references of reuse distance $i$, we can get the actual reference number with the L2 reuse distance of $i$, i.e., $L2RDH(i)$. Eq. (4) gives the formula of this process.

$$L2RDH(i) = \sum_{rd=0}^{rd} MissRDH(rd) \times P_{hit}[rd][rd - i] \quad (4)$$
In this section, we use gem5 simulator [15] to evaluate our model [15]. The cache architecture used in the experiments has two levels and the detailed configurations are shown in Table 1. Fifteen benchmarks chosen from SPEC2006 benchmarks are used to evaluate our proposal. We compared the L2 RDH curves and the L2 miss rates with the outputs of the cycle-accurate gem5 simulations. The L2 cache miss rates of our model can be evaluated by StatCache and StatStack depending on the replacement policy the L2 cache applied.

| Configuration options | Configuration parameters |
|-----------------------|--------------------------|
| L1 cache size          | 16KB, 32KB               |
| L1 cache associativity | 2-way, 4-way             |
| L1 replacement policy  | LRU                      |
| L2 cache size          | 64KB, 128KB, 512KB       |
| L2 cache associativity | 8-way, 16-way            |
| L2 replacement policy  | LRU, Random              |

Fig. 11 and Fig. 12 show the comparisons of the L2 RDHs of four benchmarks from gem5 simulations and our model under two different cache configurations. The x-axis is the reuse distance and the y-axis is the number of references of the corresponding reuse distance in the L2 cache. We simulate 500 million instructions for each benchmark. In these two configurations, the L1 cache and the L2 cache have the same number of sets. From these figures, we can find that the outputs of our model reflect most of the characteristics of the L2 RDH curves from gem5 simulations. We set 1024 as the maximum distance, which means reuse distances larger than 1024 are counted as 1024. Because the number of references with the reuse distance larger than 400 is almost zero, the figures just show the L2 RDHs with the reuse distance from 0 to 400. Fig. 13 give the comparison results of L2 cache miss rates of all fifteen benchmarks under four configurations. Random replacement is applied in the L2 caches under config1 and config2. We use StatCache to evaluate the miss rates of the L2 Random cache. LRU replacement policy is used in the L2 cache under config3 and config4. StatStack is used to calculate the miss rates of the L2 LRU cache. In order to rule out the errors caused by StatCache and StatStack, we compare the calculated miss rates by our model with the miss rates calculated from the L2 RDH extracted from gem5 simulations. The average absolute errors under four scenarios are 1.9433%, 3.823%, 1.8287% and 3.8687%, respectively.

From Fig. 13, we can find a strange phenomenon that the L2 cache miss rates under the config2 and config4 are higher than the L2 cache miss rates under the config1 and config3, in which the cache size and associativity in config2 and config4 are larger than those of config1 and config3. This is because the traces poured into the L2 caches are different caused by the L1 cache “filtered effect” (L1 cache configurations are different). In config2 and config4, the L1 caches have larger size and associativity, which could utilize the memory reference locality better. The references with good locality are more easily hitting in the L1 cache with larger size and associativity. On the contrary, the locality of the references missing in the L1 cache and leaked into the L2 cache are not so good (many of these references are cold misses). That is the
reason why the miss rates of the L2 cache under config2 and config4 are higher than the L2 miss rates in config1 and config3.

To verify our hypothesis that there are too many cold misses during the beginning of the system, we conduct experiments with 1 billion instructions to warm up the multi-level cache architecture. Then, we profile the trace information of the following 500 million instructions and evaluate the multi-level cache architecture again. The results are shown in Fig. 14 and Fig. 15. The grey bars mean the miss rates of the L2 cache without warming up the caches. We can see that after warming up the caches, the miss rates would decrease, which is caused by the decreasing of the cold misses.

Fig. 13. Comparisons of L2 miss rates

Fig. 14. Comparisons of L2 miss rates with/without warming up (L1 16KB 2-way LRU; L2 64KB 8-way LRU)

Fig. 15. Comparisons of L2 miss rates with/without warming up (L1 16KB 2-way LRU; L2 64KB 8-way LRU)

To evaluate our model under the cache architectures with different number of sets in the L1 cache and the L2 cache, we conduct the experiments under four different cache configurations. The ratios of sets of the L1 cache and the L2 cache are 1:2 or 1:4. Fig. 16 gives the comparisons of the L2 RDHs under the cache configurations with the set number ratio of 1:2 (L1 16KB 2-way, L2 128KB 8-way). Fig. 17 gives the comparisons under the cache configurations with the set number ratio of 1:4 (L1 32KB 4-way, L2 512KB 16-way). In Fig. 16 and Fig. 17, we can see that around the reuse distance of 30 in cactusADM, the results of our model smooth the characteristics of the L2 RDHs. In the tail of the L2 RDHs of bzip2 in Fig. 16 and Fig. 17, there are some low peaks in the
simulated curves, but the results from our model cannot reflect these subtle fluctuations. We believe that these errors are caused by the usage of the fixed probability of \( P_{\text{same}} \). The actual \( P_{\text{same}} \) of each reference may be different, which means the \( P_{\text{same}} \) is actual a probability distribution instead of a fixed ratio (in our experiments, however, we consider \( P_{\text{same}} \) as the fixed ratio of the number of sets in the L1 cache and the L2 cache). Fig. 18 shows the comparisons of the L2 miss rates based on the L2 RDHs from gem5 simulations and our model. The average absolute errors under the four different cache configurations are 4.3166%, 9.9571%, 4.1573% and 9.4838%, respectively.

![Fig. 16. Comparisons of the L2 RDH between gem5 simulation results and our model (L1 16KB 2-way, L2 128KB 8-way)](image)

![Fig. 17. Comparisons of the L2 RDH between gem5 simulation results and our model (L1 32KB 4-way, L2 512KB 16-way)](image)

The average error of all the results in the above experiments of calculating the miss rates is 4.9229%. We guess there are two reasons causing the errors. The first is the errors from StatCache and StatStack. The second reason is that we use a fixed ratio of \( P_{\text{same}} \) instead of probability distributions, which is why the errors increased when the associativity increased.

![Fig. 18. Comparisons of L2 miss rate (L1 and L2 have different set number)](image)
Table. 2 Hardware Configurations of our profiling platform

| CPU           | Intel(R) Core(TM) i7-4790 CPU @3.60GHz, 4 cores / 8 threads |
|---------------|-------------------------------------------------------------|
| RAM           | 8GB DDR3 1600MHz ×2                                         |
| Storage       | 1TB HDD SATA3                                               |
| OS            | Ubuntu 18.04.1 LTS                                          |

Table. 2 shows the hardware configurations of the profiling platform in our experiment system. Fig. 19 gives the comparison of the profiling time between our model and conventional models. Besides the RDH and the SDH, compared with conventional models, our model profiles RST table and Hit-RDH additionally. From Fig. 19, we can see that the time spent in profiling these two new metrics can be ignored compared with the total simulation time.

Fig. 20 shows the comparisons of evaluation time of gem5 detailed simulations and our model. Simulations of multi-level cache architecture are very time-consuming. Our model can avoid doing this process and the average evaluation time can be sped up by 7.38 times. We can see that the acceleration of evaluation of benchmark 429.mcf improves most. Because 429.mcf is a memory-intensive benchmark, which produces more memory references than other benchmarks.

VIII. Multi-core Application

In modern processors, a single core is unable to meet the needs of performance. Multi-core processors are gradually replacing single-core processors. Our model can be utilized for each CPU core in multi-core systems.

In this case, we use our model in the scenario with two CPU cores. The two-core architecture is shown in Fig. 21. Two CPU cores with their private L1 data cache and L1 instruction cache share the unified L2 cache. We use our model to calculate the L2 RDH for each CPU core. However, because two CPU cores shared the L2 cache, we need to use StatCC [6] to merge the individual L2RDHs for each CPU core and output the L2 RDH for the L2 cache. As in the case of a single core, we use StatCache or StatStack to calculate the L2 miss rate for L2 Random or LRU cache, respectively. The architecture parameters are shown in table 2.

Table. 2 Multi-core Architecture Configurations

| Configuration options                  | Configuration parameters |
|----------------------------------------|-------------------------|
| L1 cache size (CPU0, CPU1)             | 16KB, 32KB              |
| L1 cache associativity (CPU0, CPU1)    | 2-way, 4-way            |
| L1 replacement policy (CPU0, CPU1)     | LRU                     |
| L2 cache size                           | 64KB, 256KB             |
| L2 cache associativity                  | 8-way, 16-way           |
| L2 replacement policy                   | LRU                     |

StatCC is a simple yet efficient model for estimating the shared cache miss rate of co-scheduled applications on architectures with a hierarchy of private and shared caches by multi-cores.

Fig. 22 shows the L2 miss rates calculated by our model of fifteen combinations of benchmarks from SPEC2006. In this case, the size of L1 caches of both CPU cores is 16KB with the associativity of 2 and the size of L2 cache is 64KB with the associativity of 8, which means the L1 cache and the L2 cache have the same number of cache sets. As we can see, the average absolute error is 5.06125%.
Fig. 22. The L2 miss rates calculated by our model and StatCC (L1 16KB 2-way LRU; L2 64KB 8-way LRU)

Fig. 23 gives the results of the scenario that L1 cache and the L2 cache have different numbers of cache sets. The size of L1 caches of both CPU cores is 32KB with the associativity of 4 and the size of L2 cache is 256KB with the associativity of 16 which means the number of sets in the L2 cache is twice that of the L1 caches. The average absolute error is 6.9975%.

To distinguish the errors caused by StatCC, In Fig. 22 and Fig. 23, the yellow bars are the miss rates calculated by the StatCC model, which takes the simulated L2 RDHs leaked from both CPU cores as the inputs. We consider that the errors of our model may also come from the StatCC model considering the yellow bars in Fig. 22 and Fig. 23 are not perfectly matched to the simulation results as well.

Fig. 23. The L2 miss rates calculated by our model and StatCC (L1 32KB 4-way LRU; L2 256KB 16-way LRU)

IX. CONCLUSION

In this paper, we propose two new metrics, RST table and Hit-RDH to describe more detailed information of the software traces. Helped by these two new metrics, we put forward a model, which takes the L1 RDH, RST table and Hit-RDH as the inputs and output the L2 RDH. Combined with StatCache and StatStack, our model can be applied to evaluate the L2 cache miss rate with Random or LRU replacement policies. The L1 cache RST table and Hit-RDH merely need to be profiled once for each benchmark given an L1 cache architecture and they can be re-used for evaluations of different L2 cache configurations. Compared with the results from gem5 simulations, the evaluation time can be sped up by almost 8X and the average absolute errors for the single core and two-core scenarios are 4.9229% and 6.0294%, respectively.

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