FPGA Implementation of a Novel Image Steganography for Hiding Images

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Abstract As the complexity of current data flow systems and according infrastructure networks increases, the security of data transition through such platforms becomes more important. Thus, different areas of steganography turn to one of the most challengeable topics of current researches. In this paper a novel method is presented to hide an image into the host image and Hardware/Software design is proposed to implement our stagenography system on FPGA- DE2 70 Altera board. The size of the secret image is quadrant of the host image. Host image works as a cipher key to completely distort and encrypt the secret image using XOR operand. Each pixel of the secret image is composed of 8 bits (4 bit-pair) in which each bit-pair is distorted by XORing it with two LSB bits of the host image and putting the results in the location of two LSB bits of host image. The experimental results show the effectiveness of the proposed method compared to the most recently proposed algorithms by considering that the obtained information entropy for encrypt image is approximately equal to 8.

Keywords: host image, secret image, encryption, steganography, FPGA, DE2-70.

Categories: H.3.1, H.3.2, H.3.3, H.3.7, H.5.1

1 Introduction

The increasing complexity of data flow systems makes information security more important in data storage and transmission domains. Images are widely used in current processes and their protection from unauthorized access becomes more important. Fragile watermarking has been widely used to authentication and content integrity verification [1, 2]. Such a technique modifies the host image in order to insert the pattern but the permanent embedding distortion method is intolerable for the applications that require high quality images such as military images.
In addition, image encryption plays a significant role in information hiding [3-7]. Image hiding and encrypting algorithms range from simple spatial domain methods to more complicated and reliable frequency domains. Most of available encryption methods are proposed for common text data and are not proper for multimedia data such as images. Image encryption is somehow different from text encryption because of some inherent features of image, such as bulk data capacity and high correlation among its pixels. Thus, chaotic map ciphers and traditional cryptographic algorithms such as, RSA (Road Safety Authority) and DES (Data Encryption Standard) are no longer effective for practical image encryption, especially for an on-line communication scenario [8, 9]. In [10] image security is presented over internet through encryption/decryption of text data, however, due to large data size and real time constrains, algorithms that are good for textual data would not have the same performance on image.

Two levels of security are defined for digital image encryption as low level and high-level. In low-level security encryption, the encrypted image has degraded visual quality compared to that of the original one, but the content of the image is still visible and understandable to the viewers while in the high-level security, the content is completely scrambled and the image just looks like random noise.

In the most of natural images the values of the neighboring pixels are strongly correlated. This means that the value of any given pixel can be reasonably predicted from the values of its neighbors. Image encryption techniques try to convert an image to another one that is hard to detect. In our proposed method, the key idea is using both advantages of image watermarking and encryption in which the host image has been used both as a cipher key to distort the secret image and as host image to hide it. The hidden distorted image can easily be decrypted just by using the original host image. This technique allows transmitting high security images by hiding it in the ordinary image in which, because of a strong encryption and decreased correlation between encrypted image pixels, no one can doubt about that and predict it.

2 Proposed Algorithm

In this method both advantages of image encryption and watermarking is used for image steganography in which the host image is used as a cipher key for encryption and hiding the encrypted image.

2.1 Image encryption algorithm

Proposed method is based on distributing the secret image pixels into the host image pixels where, the size of host image is four times larger than the secret image. Using XOR operation, we can completely distort the secret image that won’t be distinguishable. The most significant factor of this algorithm is hiding encrypted image inside the ordinary image that no one doubt about that and only can be decrypted by someone who has the original image. The schematic of the proposed algorithm for encryption is shown in Figure 1.
Each pixel of secret image presented by 8 bits \((A_{7:0})\) is distributed through the pixels of the four different regions of host image. Each pixel of aforementioned regions takes two bits of the corresponding pixel of secret image (B, C, D and E take first, second, third and fourth two bits of the secret image, respectively) and XOR it with its own two LSB bits, then swap the result by its two LSB bits. This sequence is done for all pixels and as a result, each pixel of secret image is distributed in four pixels of host image. By changing of only two LSB bits of each pixel, the difference between original and watermarked image is so insignificant and can be neglected visually. As experimental results show, two LSB bits of each pixel in the host image have low cohesion with neighbor pixels. Thus to catch the best histogram and the best distorted image we used two LSB bits of pixels instead of other pairs.

By using the mentioned method, an image has been hidden easily in the host image without making any visually significant change on it. The combination of pixels for encryption is detailed in Table 1.

| Main image | Host image | Watermarked image | Encrypted image |
|------------|------------|-------------------|-----------------|
| \(A_{7:0}\) Region B : \((B_{7:0})\) | \(B'_{7:0} = [(B_{7:2}), (B_{0:1} \oplus A_{6:7})]\) | \(X_{7:0} = [(B_{0:1} \oplus A_{6:7}), (C_{0:1} \oplus A_{4:5}), (D_{0:1} \oplus A_{2:3}), (E_{0:1} \oplus A_{1:0})]\) |
| Region C : \((C_{7:0})\) | \(C'_{7:0} = [(C_{7:2}), (C_{0:1} \oplus A_{4:5})]\) | |
| Region D : \((D_{7:0})\) | \(D'_{7:0} = [(D_{7:2}), (D_{0:1} \oplus A_{2:3})]\) | |
| Region E : \((E_{7:0})\) | \(E'_{7:0} = [(E_{7:2}), (E_{0:1} \oplus A_{0:1})]\) | |

**Table 1:** Combination of pixels for encryption
2.2 Image decryption algorithm

In order to extract the hidden image, a reversed sequence of encryption process is performed. Two LSB bits of each pixel of watermarked image in different regions mixed with the corresponding pixel in original host image using XOR operator and rearranged to create the secret image as shown in Figure 2.

Using the mentioned procedure, the extracted image is exactly same as the original image without any distortion. The combination and the order of pixels in decryption process are listed in Table 2.

| Host image  | Watermarked image | Decrypted image |
|-------------|-------------------|-----------------|
| Region B : (B₀) | Region B′ : (B′₀) | A′₀ = [(B₀ ⊕ B′₀), (C₀ ⊕ C′₀), (D₀ ⊕ D′₀), (E₀ ⊕ E′₀)] |
| Region C : (C₀) | Region C′ : (C′₀) |                |
| Region D : (D₀) | Region D′ : (D′₀) |                |
| Region E : (E₀) | Region E′ : (E′₀) |                |

Figure 2: Block diagram of decryption system

Tabel 2: Combination of pixels for decryption
3 FPGA implementation (Altera DE2-70)

Altera DE2-70 board is used for hardware implementing task which includes Touch-Panel LCD, Terasic TRDB_T5M (5 Megapixel camera), SD-Card, SSRAM and two 32MB SDRAM. The platform used for implementation is shown in Figure 3.

![Figure 3: Hardware platform of image Steganography system](image)

The development is done using the Quartus II v.9 and NIOS II IDE. The implementation is divided into hardware and software sections. The image capturing is implemented in hardware, while image Steganography and displaying images in Touch-Panel LCD are done in software by the Nios II processor core. To have enough memory for frame buffering and also for manipulating data in Nios II, one of two 32MB SDRAM is used as frame buffer in hardware and other one is connected to Nios II (named as SDRAM0 and SDRAM1).

3.1 Hardware/Software Design

The hardware is created using the Hardware Description Language, Verilog and the c language based software accomplished the embedded system. The software is downloaded to NIOS II processor using NIOS II IDE which connected to CPU via JTAG UART. More details of Hardware/Software Design are explained as following.

3.1.1 Image Capture

The camera employed in this project is the Terasic TRDB-D5M [11]. To determine the size of captured frame, it is needed to configure the CMOS camera sensor. In operation, first a raw image is captured from the camera sensor, then translated to RGB (Red, Green, and Blue) format and temporarily stored in SDRAM0. The Verilog codes of these blocks are originally provided by Altera and only some slight changes applied to adapt them to the implementation requirements [12]. The detail of image
capturing process is explained in the following. Figure 4 shows the basic block diagram of the image capture part.

![Figure 4: Block diagram of the image capture block](image)

### 3.1.2 I2C Sensor Configuration

The Verilog HDL module that configures programming registers from the camera is I2C_CCD_Config.v. The aim of this module is to control and configure exposure time, resolution, and frame rate. This module uses the two-wire serial interface bus to communicate with TRDB-D5M registers. This HDL file was written originally by Altera. Only configuration values are changed to obtain output image with dimension of 800 × 480 as shown in Figure 5.

```
100 assign sensor_start_row = 24'h010036; // Start Row at 54
101 assign sensor_start_column = 24'h020010; // Start Column at 16
102 assign sensor_row_size = 24'h03030F; // Row size is 960
103 assign sensor_column_size = 24'h04063F; // Column size is 1600
104 assign sensor_row_mode = 24'h220011; // Binning Row mode is 3
105 assign sensor_column_mode = 24'h230011; // Binning Column mode is 3
```

![Figure 5: I2C Sensor Configuration values](image)

The output image has a full resolution of 2592 × 1944, but by using Skipping and Binning, it can be reduced without affecting field-of-view. In skipping mode, entire rows and columns of pixels are not sampled. For example, 2X or 3X mode skips one or two “Bayer” pair of pixels, respectively, for every pair output. Binning reduces resolution by combining adjacent same-color pixels to produce one output pixel [12]. Note that each configuration has 24 bit width, where first 16 bits for register value and last 8 bits are for register identification and Binning X3 is used to reduce the output resolution by one quarter.
3.1.3 CMOS Sensor Data Capture

The Verilog HDL file that handles data capture from the camera is `CCD_Capture.v`. It is provided by Altera and no change is needed for this design. This module is responsible to get raw data from camera sensor and sends raw data with X and Y coordinates to next module as can be seen in Figure 4.

3.1.4 Bayer Color Pattern Data to 30-bit RGB

The raw data from CMOS Sensor Data Capture module is divided into Red, Green and Blue colors by the module `RAW2RGB.v`. It is provided by Altera and no change is needed for this design.

3.1.5 Multi-Port SDRAM Controller

Captured frames are stored in the SDRAM0 temporarily. As mentioned earlier, Altera DE2-70 Development Board has two 32-MB synchronous DRAM. But only one of two 32 MB chips is used as frame buffer and the other one is added to NIOS II. To store frames, a FIFO (First In First Out) stack is used with dual-read and dual-write ports. Note that the read ports of this bank are connected to NIOS II via Avalon Bus and the write ports are connected to the output of RAW2RGB module. Thus, the bank ought to store at least 30 bits. But the ports have 16 bit Bus width. Thus a memory bank is proposed in which, the first 16 bits starting from address 0 stores 10 bit for red color and 5 bits for green color, and the second 16 bits starting from address 22'h700000 stores other 5 bits of green color plus 10 bits of blue color as shown in Figure 6.

![Figure 6: SDRAM0 memory bank](image)

```plaintext
SDRAM Controller

G[4:0] B[9:0]

R[9:0] G[9:5]

Write ports  [Connected to the output of RAW2RGB Module]

Read ports [Connected to Nios II]

Start Address (first 16 bit)

Start Address (second 16 bit)

22'h700000
```
To meet our implementation needs, the settings changed in original file provided by Altera (SDRAM_Control_4Port.v) on SDRAM0’s address range as shown in Figure 7.

```vhdl
define
begin
    rWR1_ADDR <= 0;     // Write1 Base Address
    rWR2_ADDR <= 22’h700000; // Write2 Base Address
    rRD1_ADDR <= 0;     // Read1 Base Address
    rRD2_ADDR <= 22’h700000; // Read2 Base Address
    RWR1_MAX_ADDR <= 800*480; // Write1 Maximum Base Address
    RWR2_MAX_ADDR <= 22’h700000+800*480; // Write2 Maximum Address
    rRD1_MAX_ADDR <= 800*480; // Read1 Maximum Address
    rRD2_MAX_ADDR <= 22’h700000+800*480; // Read2 Maximum Address
end
```

(Figure 7: SDRAM_Control_4Port setting)

### 3.1.6 Nios II processor core and its peripherals

Designing systems with embedded processors requires both hardware and software elements. Software involves the operations executed by processor (Nios II) and hardware includes operations directly executed by hardware on FPGA. Altera provides the SOPC Builder (System-On-a-Programmable Chip) that automates connecting software-hardware components to create a complete computer system.

The soft-core processor used in this implementation is a Nios II processor. With SOPC Builder, it is possible to specify the settings for a Nios II processor and add peripherals and select bus connections, I/O memory mappings, and IRQ assignments.

Nios II processor and its peripherals are depicted in Figure 8. Nios II core communicates with other modules using System Interconnect Fabric.

(Figure 8: Nios II processor and its peripherals)

It is worth noting that Nios II/f core is selected for our system. It is optimized with dynamic branch prediction and 6 stage pipeline, 2Kbyte Data Cache and 4Kbyte Instruction Cache. The connection of Nios II with its peripherals is depicted in Figure 9.
In the proposed implementation design, the host image is read from SD-card and the secret image is captured by CMOS slave controller. To establish a SD Card communication with Nios II, four PIO (named as sd_clk, sd_cmd, sd_dat, sd_dat3) are used that provide a synchronous serial data communication and The CMOS slave controller is originally developed by Altera. This module transfers temporarily stored frames in the SDRAM0 to the Nios II’s processor, and also send a start/stop signal to CMOS sensor data capture module. The Verilog HDL of the CMOS Controller module is cmos0.v. To display the captured (secret image), host and the result image in the Touch panel LCD, LTM controller is added to Avalon Bus. This module uses SSRAM1 (second 32MB SDRAM) as image buffer.

4 Experimental analysis

Experimental analysis of the presented algorithm has been done on several images. Barbara image of size 512 × 512 is used as the host image and Lena image of size 256 × 256 as the image that will be hidden are shown in Figure 10.a. Figure 10.b shows the watermarked image which contains encrypted image. As can be seen, the watermarked image is visually same as the original host image.

To see the result of encryption scheme, distorted image is extracted from the watermarked image and is compared with original secret image as shown in Figure 10.c.
The image extracted by the proposed decryption algorithm and the original image is shown in Figure 10.d. It can be seen that the decrypted image is absolutely clear and correct without any distortion.

Experimental result of XORing other bit-pairs of the host image for distorting the secret image are shown in Figure 11. Using the most significant bits of the host image to be XORed with the secret image bits, the distorted image is not good enough. MSB bits of neighbor pixels can’t change the secret image as well as LSB bits because of high cohesion between MSB bits of image pixels. Due to the very low variations of significant bits of host image and as moving toward the least significant bit, the variations of bits increase in the image. Thus, only two LSB bits of each pixel are used to distort the secret image.

4.1 Resistance to statistical attack

4.1.1 The gray histogram analysis

To have an encrypted image with high-level of security, the histogram of the distorted image should be distributed uniformly between different levels of gray-scales. As Figure 12 shows, the best result is obtained using two least significant bits (as shown
in Figure 12.d) and the reason of this uniformly distributed histogram lies on the fact that there is lower cohesion between LSB bits of image than MSB bits.

With a statistical analysis of Lena image and its encrypted image, the corresponding greyscale histograms are extracted as shown in Figure 13. It demonstrates that the encryption algorithm has covered up all the characters of the secret image and shows good performance of balanced 0–1 ratio, zero co-correlation and high-level security. Comparing their histograms, we can find that the pixel grayscale values of the original image are concentrated on some values, but the histograms of the encrypted images are relatively uniform, which makes the statistical attacks difficult.

![Histogram of encrypted image by using different bit-pairs of host image: (a) 7-6 bits (b) 5-4 bits (c) 3-2 bits (d) 1-2 bits.](image)

Figure 13: Left image is the histogram of Lena image and right image is its corresponding encrypted image using our proposed method.
4.1.2 Correlation coefficient analysis

To test the correlation between two adjacent pixels in secret-image and ciphered image, the following procedure was carried out. First, randomly 1000 pairs of two adjacent (in horizontal, vertical, and diagonal direction) pixels from an image are selected. Then, the correlation coefficient of each pair is calculated by using Eq. (1) [13]:

\[ r_{xy} = \frac{\text{cov}(x, y)}{\sqrt{D(x)} \sqrt{D(y)}} \]  

(1)

Where

\[ \text{cov}(x, y) = \frac{1}{N} \sum_{i=1}^{N} (x_i - E(x))(y_i - E(y)), \]

\[ E(x) = \frac{1}{N} \sum_{i=1}^{N} x_i, \quad D(x) = \frac{1}{N} \sum_{i=1}^{N} (x_i - E(x))^2 \]

x and y are grey-scale values of two adjacent pixels in the image.

Figure 14 shows the correlation distribution of two vertically adjacent pixels in the secret-image and in the ciphered image. And the correlation coefficients are shown in Table 3. These correlation analysis prove that this algorithm satisfy zero co-correlation.

Figure 14: Correlations of two vertically adjacent pixels in the secret-image and in the cipher-image: left and right images are the correlation analysis of secret image and cipher-image
4.1.3 Information entropy analysis

Information entropy is the most powerful feature that shows the randomness of image. Assume $m$ as the information source, and the formula for calculating information entropy is as Eq. (2) [14]:

$$H(m) = \sum_{i=0}^{2^n-1} p(m_i) \log_2 \left( \frac{1}{p(m_i)} \right)$$  \hspace{1cm} (2)

Where $n$ is the number of bits to represent a symbol $m_i \in m$. $p(m_i)$ represents the probability of symbol $m_i$. For a purely random source emitting $2^n$ symbols, the entropy is $H(m) = n$. For encrypted images, the entropy should ideally be $H(m) = n$. For our work (8 bits), it is the information entropy of different image samples approximately equal to 8 and these results prove that the encrypted image is very hard to be predicted as shown in Table 4.

|                | Horizontal | Vertical | Diagonal |
|----------------|------------|----------|----------|
| Plain image (secret image) | 0.9445     | 0.9701   | 0.9224   |
| Encrypted image | -0.0024    | 0.0027   | -0.0036  |

|                | Lena       | Airplane  | Pepper |
|----------------|------------|-----------|--------|
| secret image   | 7.4273     | 6.7279    | 7.5748 |
| Encrypted image(Ref. [3]) | 7.9874 | 7.9780 | 7.9860 |
| Encrypted image(Proposed method) | 7.9974 | 7.9973 | 7.9972 |

4.2 Similarity measurements between host and watermarked image

To compute the similarity between the host image and watermarked image, three different similarity measures is considered: Mean Square error (MSE), Peak Signal-to-Noise Ratio (PSNR), and Correlation. These are given by Eq. (3), Eq. (4) and Eq. (5) [15].
$$MSE = \left( \frac{1}{X \times Y} \right) \sum_{x=1}^{X} \sum_{y=1}^{Y} \left( I(x, y) - G(x, y) \right)^2 \quad (3)$$

Where $MSE$ is Mean Square Error. $X$ and $Y$ are the dimensions of the image. $I$ and $G$ are the original host and the watermarked image respectively.

$$PSNR = 10 \log_{10} \left( \frac{255^2}{MSE} \right) \quad (4)$$

Where $PSNR$ is Peak Signal-to-Noise Ratio.

$$r_{IG} = \frac{\sum_{x=1}^{X} \sum_{y=1}^{Y} I(x, y) \times G(x, y)}{\sum_{x=1}^{X} \sum_{y=1}^{Y} G(x, y)^2} \quad (5)$$

Where $r_{IG}$ is the correlation between $I$ and $G$.

The results for Similarity measurements are shown in Table 5.

| MSE       | PSNR  | $r_{IG}$ |
|-----------|-------|----------|
| $9.7275 \times 10^{-4}$ | 180.1791 | 0.9926   |

Table 1: Similarity measurements between original host image and watermarked image

5 Conclusions

In this paper a robust steganography technique has proposed for image security transmission and a Hardware/Software co-design scheme is presented to implement our stagenography algorithm on FPGA-DE2-70 board. The aim is to distribute each pixel of secret image between four pixels of host image. Due to using only two LSB bits of each pixel value for hiding image, there is insignificant difference between host image and watermarked image. The similarity of them is very critical for high security transmission. Experimental results show that, the proposed algorithm outperforms than the most recently presented technique. Lowest correlation between secret image and encrypted image, uniform histogram of encrypted image and the highest information entropy are three main features of the proposed method.

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