A Surface-Potential-Based Analytical I-V Model of Full-Depletion Single-Gate SOI MOSFETs

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Abstract: A surface-potential-based analytical I-V model of single-gate (SG) silicon-on-insulator (SOI) MOSFETs in full-depletion (FD) mode is proposed and compared with numerical data and Khandelwal’s experimental results. An explicit calculation scheme of surface potential, processing high computation accuracy and efficiency, is demonstrated according to the derivation of the coupling relation between surface potential and back-channel potential. The maximum absolute error decreases into $10^{-7}$ V scale, and computation efficiency is improved substantially compared with numerical iteration. Depending on the surface potential, the drain current is derived in closed-form and validated by Khandelwal’s experimental data. High computation accuracy and efficiency suggest that this analytical I-V model displays great promise for SOI device optimizations and circuit simulations.

Keywords: silicon-on-insulator MOSFETs; surface potential; back-channel potential; full-depletion; analytical I-V model

1. Introduction

Silicon integrated circuits (ICs) have become increasingly dense because the feature size of MOSFETs based on silicon-on-insulator (SOI) structure has not been a constraint in the sub-nanometer scale and both performance and cost improve as the feature size decreases. Up to now, there has still been considerable interest in optimizing properties of SOI MOSFETs [1–3] due to the widespread applications of SOI MOSFETs, such as sensors [4], memories [5], millimeter-wave circuits [6], and so on. Therefore, both device property optimization and IC design in the different fields imply that an analytical I-V model for accurately predicting I-V characteristics of SOI MOSFETs is imperative.

Recently, several analytical I-V models for bulk MOSFETs have been reported in the literatures [7–11] based on threshold voltage [7], inversion charge [8], and surface potential [9–11]. These models are demonstrated on the condition that the devices work in the partial-depletion (PD) mode, i.e., back-channel potential can be assumed to equate to zero or channel potential. However, these models cannot be applied into full-depletion (FD) single-gate (SG) SOI MOSFETs without any adjustment, due to the strong back-to-surface (B-S) potential coupling effect introduced by the ultrathin-body and buried oxide (BOX) in the FD SG SOI MOSFETs. Such a coupling effect increases the calculation complexity. In the meantime, some models [12–15] of multiple-gate SOI MOSFETs have been proposed, and some models of FD SG SOI MOSFETs [16–20] incorporating the B-S potential coupling effect are derived. Ravariu et al. [16] and Pandey et al. [17] developed threshold models for long- and short-channel FD SG SOI MOSFETs, respectively, by numerically solving a complicated equation about the position of the minimum back-channel potential. M. Miura-Mattausch et al. [18] also proposed
an analytical I-V model of FD SG SOI MOSFETs based on a completely potential-based description solving the Poisson’s equation iteratively together with additional equations. Here, numerical computation reduced the calculation efficiency. W. Wu et al. [19] and Y. S. Yu et al. [20] gave surface-potential-based analytical I-V models in which smoothing functions are employed. In addition, J. Huang et al. [21] described a DC model of FD poly-Si TFTs based on the assumption of B-S potential relation. Because of computation complexity, they gave up deriving B-S potential relation, leading to low computation accuracy.

In this paper, we propose a surface-potential-based analytical I-V model of FD SG SOI MOSFETs. An explicit solution of surface potential in FD SG SOI MOSFETs is solved from the 1-D Poisson’s equation and derivation of B-S potential coupling relation. This surface potential calculation scheme has high computation accuracy and efficiency, which is verified by numerical techniques. Subsequently, based on the surface potential, we present the drain current analytically and validate it with Khandelwal’s experimental data [22]. Finally, combining with simulation results of this model, we discuss the effects of the different parameters on the electrical properties of FD SG SOI MOSFETs in detail.

2. Surface Potential Explicit Calculation Scheme

For FD SG SOI MOSFETs, a crystalline silicon (c-Si) film is deposited on a BOX film, as shown in Figure 1. The x-axis is perpendicular to the plane of gate, the carrier transport occurs along the y-axis, and the z-axis is set parallel to the structural confinement direction. In addition, \( t_{ox} \) and \( t_{si} \) are gate oxide and silicon body thicknesses, respectively. Following the gradual channel approximation and neglecting the whole concentration, we can simply write the Poisson’s equation as:

\[
\frac{d^2 \varphi}{dx^2} = \frac{q}{\varepsilon_{sl}} \left[ n_0 \exp \left( \frac{\varphi - V_{ch}}{V_t} \right) + N_a \right].
\]

(1)

Here, \( \varphi \) is the electrostatic potential as a function of the variable \( x \), the free charge density is demonstrated as \( n_0 \exp \left[ (\varphi - V_{ch}) / V_t \right] \) where \( V_t \) is the thermal voltage \((kT/q)\), \( k \) is the Boltzmann constant, \( T \) is the absolute temperature, \( q \) is the magnitude of electronic charge, \( \varepsilon_{sl} \) is the dielectric permittivity of silicon, \( n_0 \) is expressed as \( n_0 = N_a \exp \left( -2V_{fp} / V_t \right) \), \( V_{ch} \) is the channel potential, \( V_{fp} \) is the quasi-Femi potential, and the doping concentration is symbolled by \( N_a \). According to Figure 1, there are three boundary conditions for (1), i.e., \( \varphi_s \) is the surface potential with \( \varphi_s = \varphi(t_{ox}) \), \( \varphi_b \) is the back-channel potential with \( \varphi_b = \varphi(0) \), and \( (d\varphi/dx)_{x=0} = 0 \).

![Figure 1. x-y cross section of silicon-on-insulator (SOI) MOSFETs.](image)

It is noted that the c-Si film thickness of SOI MOSFETs comes into a sub-nanometer (<100 nm) scale so that the devices work in the FD mode rather than the PD mode of the bulk MOSFETs. From device structure aspect, the sub-nanometer film on BOX results in the strong back-to-surface (B-S) potential coupling effect, implied by the boundary condition \( \varphi_b = \varphi(0) \) for (1). Here, \( \varphi_b \) cannot be set as a constant equating to \( V_{ch,b} \) actually it is a function as \( \varphi_s \) according to \( \varphi_b = \varphi(t_{si}) \). This function is the B-S potential coupling relation, which is to be derived as follows.
For FD SG SOI MOSFETs, the channel layer is usually in the lightly or moderately doped case, i.e., free charge density is far larger than $N_d$, yielding:

$$\frac{d^2 \phi}{dx^2} = \frac{q}{\varepsilon_{si} n_0} \exp\left(\frac{\phi - V_{ch}}{V_I}\right).$$

(2)

We can observe that the mathematical form of (1) is relatively complicated because of the inclusion of an exponent term and a constant term in the right-hand side (RHS) of the equation, so that a solution of $\phi$ cannot be solved generally up to now. However, (2) retains the clear physical meaning and becomes the simplification of (1) to help us analytically derive the B-S potential coupling relation. We integrated (2) twice to obtain this relation as:

$$\phi_s = \phi_b + 2 V_I \ln\left\{ \sec\left[ \frac{L_D}{2} \exp\left(\frac{\phi_b - V_{ch}}{2V_I}\right)\right] \right\}. \tag{3}$$

Here, $L_D$ is the Debye length with $L_D = (\varepsilon_{si} V_I / 2 q n_0)^{1/2}$.

Using the Gauss’s law, the relation $\frac{d^2 \phi}{dx^2} = \frac{q}{\varepsilon_{si} n_0} \exp\left(\frac{\phi - V_{ch}}{V_I}\right)$, and (1), we can obtain the implicit function of $\phi_s$ as:

$$C_{ox}^2 \left( \frac{V_{gs} - V_{fb} - \phi_s}{V_I} \right)^2 = 2 \frac{q \varepsilon_{si}}{V_I} \left\{ N_d \left( \frac{\phi_s - \phi_b}{V_I} \right) + n_0 \exp\left(\frac{\phi_s - V_{ch}}{V_I}\right) - \exp\left(\frac{\phi_b - V_{ch}}{V_I}\right) \right\}. \tag{4}$$

If $\phi_b$ is set as a constant with $\phi_b = V_{ch}$, then (4) degenerates to be only suitable for PD MOSFETs, i.e.,

$$C_{ox}^2 \left( \frac{V_{gs} - V_{fb} - \phi_s}{V_I} \right)^2 = 2 \frac{q \varepsilon_{si}}{V_I} \left\{ N_d \left( \frac{\phi_s - V_{ch}}{V_I} \right) + n_0 \exp\left(\frac{\phi_s - V_{ch}}{V_I}\right) - 1 \right\}. \tag{5}$$

In the PD mode, we can solve (5) only to get $\phi_b$. However, in the FD mode, we should analytically solve the equation set of (3) and (4) to get the expressions of $\phi_s$ and $\phi_b$. Obviously, there is much more computation complexity in the FD mode compared with the PD mode. Substituting (3) into (4), we can solve an explicit solution of $\phi_b$ as:

$$\phi_b = V_{ch} + V_I \ln \left( \frac{4 L_D^2 \beta}{\varepsilon_{si}} \right), \tag{6}$$

where $\beta$ is symbolled as $\beta = \sqrt{\frac{2 V_0 (2 e^r)}{W_0 (2 e^r) + 4 r}}$, $F$ is symbolled as $F = \frac{V_{gs} - V_{fb} - V_{ch}}{2 V_I} - \ln\left(\frac{2 L_D}{\varepsilon_{si}}\right)$, $r$ is the nature parameter with $r = \frac{v_{th} h_s}{\varepsilon_{si} v_I}$, and $W_0$ is the Lambert W function [23], which is the solution of $W_0(x) \exp[W_0(x)] = x$. Furthermore, substituting (6) into (4), we can derive the explicit solution of $\phi_s$ as:

$$\phi_s = V_{gs} - V_{fb} - 2 V_I W_0 \left[ \frac{\lambda}{2} \cdot D \cdot \exp\left(\frac{V_{gs} - V_{fb} - V_{ch}}{2V_I}\right) \right] + \omega. \tag{7}$$

Here, $\lambda$ is the bulk factor with $\lambda = \sqrt{2 q \varepsilon_{si} n_0 / V_I C_{ox}^2}$, $D$ can be considered as the impact fact describing the B-S potential coupling effect in FD SG SOI MOSFETs with $D = \sqrt{\sin^2 \beta + N_d \cos^2 \beta \ln(\sec^2 \beta) / 4 n_0 L_D^2 \beta^2}$, and $\omega$ is the Schroder series [24] used to improve the accuracy of the explicit solution of $\phi_s$ with $\omega = - (y / y') / (1 - 0.5 yy'' / y' / y')$. Here, $y = C_{ox}^2 \left( V_{gs} - V_{fb} - \phi_s \right)^2 - 2 q \varepsilon_{si} n_0 V_I \exp(\phi_s / V_I - \phi_b / V_I) + N_d (\phi_s - \phi_b)$, and $y'$ and $y''$ are the first and the second derivatives of $y$ versus $\phi_s$, respectively.

We compare $\phi_s$ of our scheme with that of the numerical method and show the results in Figures 2 and 3. We observe that good agreements are obtained and computational efficiency of (7) is seven times
that of the numerical method, as shown in Figure 2. Moreover, we analyze the absolute errors of $\phi_s$ in the different cases compared with the numerical results of (4) in Figure 3. First of all, the maximum errors of $\phi_s$ between (7) and the numerical results are less than $10^{-7}$ V. Then, the models of PD MOSFETs, i.e., (5), cannot be adopted into FD SOI MOSFETs and errors are up to 0.01V, because $\phi_b$ cannot be set as a constant in the FD mode. Lastly, in the process of computing $\phi_s$, $N_a$ should not be ignored even if in the lightly or moderately doped case, or else large errors would be introduced into the models.

Figure 2. Comparisons between the surface potential scheme and numerical results for different $V_{ch}$.

Figure 3. Absolute errors of $\phi_s$ between solution and numerical method vs. $V_{gs}$. Parameters used in simulations are same as those in Fig. 2.
3. Analytical I-V Model

Considering the single-gate structure of the devices, the charge-sheet model (CSM) [25] derived by Brews can be adopted to derive the drain current including the drift and diffusion components, i.e., \( I_{ds1} \) and \( I_{ds2} \), respectively. Based on the CSM and the solution of \( \varphi_s \), we get the drain current \( I_{ds} \) as:

\[
I_{ds} = I_{ds1} + I_{ds2} = -\mu \frac{W}{L} \int_{\varphi_{sa}}^{\varphi_{sd}} Q_1(\varphi_s) d\varphi_s + \mu \frac{W}{L} \int_{\varphi_{sa}}^{\varphi_{sd}} dQ_1(\varphi_s). \tag{8}
\]

Here, \( \varphi_{sa} \) and \( \varphi_{sd} \) are solutions of \( \varphi_s \) corresponding to \( V_{ch} = 0 \) and \( V_{ch} = V_{ds} \), respectively, and \( Q_1 \) is the free charge density per unit area, which can be derived by using the Gauss’s law at the interface between oxide and channel layers, yielding:

\[
Q_1(\varphi_s) = -C_{ox}(V_{gs} - V_{fb} - \varphi_s) + qN_a l_{si}. \tag{9}
\]

In (8), \( \mu \) is a typical set of universal effective charge mobility [26], including acoustical phonon [27] and surface roughness [28] scattering of the inversion layer carriers influenced from the normal field, i.e.,

\[
\mu = \frac{\mu_0}{1 + \theta_1(V_{gs})^{1/3} + \theta_2(V_{gs})^2 + \theta_3 V_{ds}}, \tag{10}
\]

where \( \mu_0 \) is the maximum extracted value of the mobility at a given doping concentration, and \( \theta_1 \) and \( \theta_2 \) are degeneration parameters introduced by phonon scattering and surface-roughness scattering due to \( V_{gs} \).

Substituting (9) and (10) into (8), we can analytically solve the expression of \( I_{ds} \) as:

\[
I_{ds} = \frac{\mu_0}{1 + \theta_1(V_{gs})^{1/3} + \theta_2(V_{gs})^2 + \theta_3 V_{ds}} \cdot C_{ox} \frac{W}{L} \cdot \left[ -\frac{1}{2}(V_{gs} - V_{fb} - \varphi_s)^2 - \frac{qN_a l_{si}}{C_{ox}} + V_1 \right] \frac{\varphi_{sd}}{\varphi_{sa}}. \tag{11}
\]

Furthermore, we match the results of (11) with Khandelwal’s experimental data [22] required from ultrathin-body SOI MOSFETs in the cases of long- and short-channels. In [22], the ultrathin-body SOI MOSFETs were manufactured, with a silicon body thickness of 8 nm and gate oxide thickness of 1.2 nm, respectively. For long-channel devices, the length of channel is 11 \( \mu \)m. For short-channel devices, the length of channel is 30 nm. The parameters used in the simulations are listed in Table 1. As shown in Figures 7–10, we can observe that such a model can give a consistent solution for both transfer and output characteristics. It is noted that, for short-channel devices, channel-length modulation (CLM) is considered by using “effective drain-source voltage” [29] in our I-V model, i.e.,

\[
V_{dseff} = \frac{a}{1 + (V_{ds}/V_{dsat})^a}. \tag{12}
\]

In (12), the parameter \( a \) is a transition factor deciding shift from the drain-to-source voltage \( V_{ds} \) to the effective drain-source voltage \( V_{dseff} \), and \( V_{dsat} \) is an extracted saturation voltage parameter. In the process of the calculation, we can substitute \( V_{dseff} \) for \( V_{ch} \) in (6) and (7) to make the model include CLM, which is equivalent with pinch-off behavior or velocity saturation.

In Figures 7 and 8, we compare the model with Khandelwal’s experimental data [22] for \( I_{ds}-V_{gs} \) and \( I_{ds}-V_{ds} \) characteristics in the long-channel device with 11 \( \mu \)m, which does not have a significant presence of channel-length modulation (CLM) in its characteristics. The excellent agreement between the model and the experimental data validates the core drain current model for long-channel devices. In Figures 9 and 10, our model is evaluated for short-channel effects by comparing \( I_{ds}-V_{gs} \) and \( I_{ds}-V_{ds} \) characteristics against Khandelwal’s experimental data [22] for a short-channel device with \( L = 30 \) nm,
which also demonstrate good model accuracy. The presence of CLM is apparent from Khandelwal’s experimental data [22] of output conductance (Figure 10) in this device. The reason why our proposed model can still capture these phenomena quite well is that we introduce “effective drain-source voltage” to describe CLM. According to the transfer characteristics shown in Figures 7 and 9, we can observe that short channel effects lead to subthreshold property degradation and a larger leakage current. According to output characteristics shown in Figures 8 and 10, we can observe that short channel effects result in obvious CLM or velocity saturation.

Table 1. Parameters for simulations in Figures 4–10.

| Symbol | Value in Figures 4 and 5 | Value in Figures 6 and 7 | Value in Figure 8 | Value in Figure 9 | Value in Figure 10 |
|--------|--------------------------|--------------------------|-------------------|-------------------|-------------------|
| \(N_a\) (cm\(^{-3}\)) | \(1 \times 10^{12}\) | \(1.08 \times 10^{11}\) | \(1 \times 10^{13}\) | \(1 \times 10^{13}\) | \(1 \times 10^{12}, 1 \times 10^{14}, 1 \times 10^{16}\) |
| \(t_{ox}\) (nm) | 1.2 | 1.2 | 20, 40, 60 | 20 | 2 |
| \(t_{si}\) (nm) | 8 | 8 | 50 | 20, 60, 400 | 10 |
| \(V_{fb}\) (V) | 0 | 0 | 0 | 0 | 0 |
| \(V_{ds}\) (V) | - | - | 0 | 0 | 0 |
| \(W\) (\(\mu\)m) | 10 | 10 | 10 | 10 | 10 |
| \(L\) (\(\mu\)m) | 11 | 0.03 | 10 | 10 | 10 |
| \(\mu_0\) (cm\(^2\)V\(^{-1}\)) | 250 | 250 | 250 | 250 | 250 |
| \(\theta_1\) (-) | 0.001 | 0.001 | - | - | - |
| \(\theta_2\) (-) | 0.001 | 0.001 | - | - | - |
| \(V_{dsat}\) (V) | - | 0.6 | - | - | - |
| \(a\) (-) | - | 2 | - | - | - |

Figure 4. Comparisons between the surface potential calculation scheme and numerical results for different \(t_{ox}\), and the drain current in (11).
Figure 5. Comparisons between the surface potential calculation scheme and numerical results for different $t_{si}$, and the drain current in (11).

Figure 6. Comparisons between the surface potential calculation scheme and numerical results for different $N_a$, and the drain current in (11).
introduce "effective drain-source voltage" to describe CLM. According to the transfer characteristics shown in Figures 4 and 6, we can observe that short channel effects lead to subthreshold property degradation and a larger leakage current. According to output characteristics shown in Figures 5 and 7, we can observe that short channel effects result in obvious CLM or velocity saturation.

Figure 7. Comparisons of transfer characteristics between our drain current model results and long-channel experimental data [22] from Khandelwal et al.

Figure 8. Comparisons of output characteristics between our drain current model results and long-channel experimental data [22] from Khandelwal et al.
Figure 9. Comparisons of transfer characteristics between our drain current model results and short-channel experimental data [22] from Khandelwal et al.

Figure 10. Comparisons of output characteristics between our drain current model results and short-channel experimental data [22] from Khandelwal et al.
4. Discussion

In this section, we give some discussions about surface potential and drain current properties influenced by the structure parameters and the doping concentration of full-depletion single-gate SOI MOSFETs, including $t_{ox}$, $t_{si}$, and $N_a$. The parameters used in the simulations are listed in Table 1. We analyze the effect from the single variable by using our model as follows.

1. The thickness $t_{ox}$ of dielectric between gate and channel rightly determines the ability of inducing charges, particularly for the strong inversion region, as shown in Figure 4. We can observe that $\phi_s$ increases as $t_{ox}$ decreases. Thin $t_{ox}$ leads to larger $C_{ox}$, and then, according to the Gauss’s law, many more free charges are introduced in the strong inversion region. It means that larger $\phi_s$ and $I_{ds}$ can be obtained in the channel.

2. The thickness $t_{si}$ of the channel film can influence $\phi_b$ but not $\phi_s$. According to Figure 5, $t_{si}$ is larger and $\phi_b$ becomes larger. It is implied by the simplified Poisson’s equation (1) only including the doping concentration. Simultaneously, $I_{ds}$ is affected by $t_{si}$ lightly, because the free charges in the inversion layers are confined to a very thin layer with the order of 10–100Å [30]. That is also shown in Figure 5, graphed by our model.

3. Finally, we can observe from Figure 6 that $\phi_s$, $\phi_b$, and $I_{ds}$ are in positive correlation with the doping concentration $N_a$, because $N_a$ directly decides the value of the free charge density.

5. Conclusions

In this paper, we provided a surface-potential-based analytical $I$-$V$ model for full-depletion single-gate silicon-on-insulator MOSFETs with lightly or moderately doped channels. Based on deriving analytically the back-to-surface potential coupling relation, we solved the explicit solution of the implicit surface potential function by using the Lambert $W$ function, and matched this solution with the numerical iteration method. Considering single-gate structure and ultrathin channel film, the drain current was derived analytically on the basis of the charge sheet model, and good agreements with experimental data were obtained. Finally, we gave the discussions about influences of the structure parameters and the doping concentration on the electrostatic properties of the devices. As a result, accurate simulation results demonstrate that our model can predict electrostatic properties of full-depletion single-gate silicon-on-insulator MOSFETs.

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