Optimal Mapping for Near-Term Quantum Architectures based on Rydberg Atoms

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Abstract—Quantum algorithms promise quadratic or exponential speedups for applications in cryptography, chemistry and material sciences. The topologies of today’s quantum computers offer limited connectivity, leading to significant overheads for implementing such quantum algorithms. One-dimensional topology displacements that remedy these limits have been recently demonstrated for architectures based on Rydberg atoms, and they are possible in principle in photonic and ion trap architectures. We present the first optimal quantum circuit-to-architecture mapping algorithm that exploits such one-dimensional topology displacements. We benchmark our method on quantum circuits with up to 15 qubits and investigate the improvements compared with conventional mapping based on inserting swap gates into the quantum circuits. Depending on underlying technology parameters, our approach can decrease the quantum circuit depth by up to 58% and increase the fidelity by up to 29%. We also study runtime and fidelity requirements on one-dimensional displacements and swap gates to derive conditions under which one-dimensional topology displacements provide benefits.

Index Terms—Quantum Computing, Quantum Circuit Mapping, Topology Displacements, Rydberg Atoms, CAD

I. INTRODUCTION

The availability of ever-increasing quantum resources in contemporary quantum computers promises disruptive applications in drug design [1], chemistry [2], material sciences [3] and cryptography [4]. However, the computation of quantum algorithms facilitating advances in these fields is limited by large error rates and short decoherence times in current quantum computers [5], [6]. Furthermore, in most quantum computing technologies such as ion traps [7]–[10], superconducting circuits [11]–[13], Rydberg atoms [14] and NV centers [15] only a subset of qubit-qubit interactions defined by the topology of a quantum computer are supported at a time. Quantum algorithms can be made compliant with a quantum computer topology through quantum circuit mapping. Quantum circuit mapping, however, incurs further errors during quantum algorithm computations since additional operations, e.g. swap gates, need to be inserted into the computation [16], [17]. It is therefore crucial to reduce the overhead incurred by quantum circuit mapping to extend the set of feasible quantum algorithm computations in current noisy and intermediate-scale quantum computing technology [5].

Quantum computing architectures based on Rydberg atoms are characterized by long decoherence times, high-fidelity quantum gates [18], multi-qubit interactions [19] and the capability to dynamically change their topology during the computation of a quantum algorithm [20]–[22]. They are therefore a promising candidate for near-term quantum computing and physical realizations are currently investigated by research groups [23] and startups such as QUERA [24] and Pasqal [25]. However, the topology changes supported by quantum computers based on Rydberg atoms have not been explored for quantum circuit mapping, yet.

Topology changes, which do not manipulate the quantum state per se, can have lower error rates than swap gates. Moreover, one topology change can have the same effect as multiple swap gates, potentially reducing the circuit’s depth and increasing the probability to complete the circuit within the limit given by the decoherence time. The computational reach of quantum technologies supporting topology changes, such as Rydberg atoms, may therefore be extended.

In this work, we develop an optimal method that exploits the topology changes available in Rydberg atom quantum computing technologies for quantum circuit mapping by:

• developing a novel formal model for one-dimensional topology changes and extending it with a given formal model for swap gate insertion.
• evaluating the developed quantum circuit mapping method on intermediate-scale quantum circuits.
• characterizing technology parameters that enable an improved quantum circuit mapping through topology changes supported by near-term Rydberg architectures.

The remainder of this work is structured as follows. In section II the principles of quantum computing are introduced. Section III introduces quantum architectures based on Rydberg atoms and topology changes supported by near-term devices. Section IV introduces quantum circuit mapping and reviews related work. Section V introduces a novel formal model that considers topology changes supported by the Rydberg atoms platform and discusses how to use this model for conventional quantum circuit mapping using swap gates. Section VI shows the improvement in quantum circuit depth and fidelity by considering such topology changes for different technology parameters on intermediate-scale quantum circuits. Section VII concludes the work.

II. QUANTUM COMPUTING

A quantum computer performs computations on the quantum state of n-qubits as specified by external control. The basic
unit of information in quantum computing is the qubit, which describes a two-level quantum system [26]. The quantum state of one qubit can be described as

$$|\psi\rangle = \alpha_0 |0\rangle + \alpha_1 |1\rangle,$$

(1)

where $|i\rangle$ are the computational basis states with $\alpha_i$ complex probability amplitudes whose magnitudes must sum up to one. If more than one complex probability amplitude is larger than zero, the state is said to be in a superposition. The measurement of a state $|\psi\rangle$ yields the result $i$ with probability $|\alpha_i|^2$. If the result $i$ was measured, the state typically collapses to the computational basis state $|i\rangle$. Quantum gates describe quantum state transformations by defining changes to the complex probability amplitudes of the state. A quantum computer typically supports a subset of quantum gates, e.g. IBM’s quantum computers currently support quantum gates for specific single-qubit rotations and the controlled-not (CX) two-qubit quantum gate. Furthermore, a quantum computer may only support multi-qubit gates between specific qubits [8], [11], [27]. Such qubit-qubit interaction constraints are described by the topology graph of a quantum computer.

Figure 1 depicts the steps required to perform a quantum algorithm on a quantum computer. A quantum algorithm describes how to transform a quantum state such that the solution to a computational problem is yielded. Before executing a quantum algorithm on a target quantum computer, the algorithmic description must first be compiled to a quantum circuit that contains supported quantum gates and is then mapped to the topology of the target quantum computer. We call the latter compilation step quantum circuit mapping and model them through changes to the topology graph of the quantum computer.

A topology graph represents the qubits and possible qubit-qubit interactions in a quantum computer. The topology graph $G = (P, E)$ contains one vertex for each qubit in the quantum computer and one edge $e = (u, v)$, if qubit $u$ and qubit $v$ in the quantum computer can interact with each other, i.e. participate in a multi-qubit gate. A topology graph change is a removal or an addition of at least one edge to the graph.

In this work, one-dimensional topology displacements are considered. Figure 2 shows a $3 \times 2$ grid where the rows are shifted relatively to each other in three different ways ($a$, $b$ and $c$). In topology change $a$, the qubits in the first row are displaced to the right side. The second topology change $b$ displaces qubit 0 and qubit 1 to the left side by one and keeps qubit 2 in position. It would also be possible to displace qubit 2 to the right side in the same topology change. The topology change $c$ is not permitted since the relative position of qubit 0 and qubit 1 in the first row are swapped.

Depending on the physical realization of a quantum computer, a subset of topology graph changes are supported. Quantum computing technologies such as superconducting qubits and NV centers do not support deliberate changes in qubit-qubit interaction during the computation of a quantum algorithm and can therefore be represented by one static topology graph for quantum circuit mapping purposes [11], [15]. In contrast, quantum computing technologies based on photons, ion traps and Rydberg atoms can change the qubit-qubit interactions by physically moving qubits [33], [34] or changing other operational parameters [27]. In photonic quantum computers the qubit arrangement, and thus the qubit-
qubit interaction, can be changed arbitrarily by placing mirrors [33] or waveguides [35]. In ion trap quantum computer realizations, electromagnetic fields can be applied to support arbitrary topology changes [27]. Other ion trap quantum computers allow to physically move their ions depending on the placement and operation of electrodes in the quantum computer [33].

IV. QUANTUM CIRCUIT MAPPING

Quantum circuit mapping assigns each computation \( c \) in a quantum circuit \( U \) a location \( l \in L = \mathcal{P}(P) \setminus \{\} \) on a quantum computer to a set of qubits \( P \) and a time step \( t \in \{1, ..., T\} \) [36], [37]. A computation \( c \) may be a quantum gate, measurement or other operation and requires the specification of at least one qubit. A location \( l \) may be one or multiple qubits on a quantum computer. The primary objective of quantum circuit mapping is to adapt a quantum circuit to the topology \( G = (P, E) \) of a quantum computer such that the qubit-qubit interaction requirements of each computation \( c \) are satisfied, i.e. all multi-qubit gates are assigned to multiple vertices \( p \in P \) that are connected according to \( E \). If two successive computations were specified on the same qubits in the quantum circuit but are assigned to different vertices during quantum circuit mapping, the mapping procedure must use operations such as swap gates [36] or quantum teleportation [17].

Figure 1 shows the topology graph for a six-qubit quantum computer and a six-qubit quantum circuit containing two qubit gates. Consider the two-qubit quantum gates CX(1, 3) and CX(2, 4) between qubit pair 1, 3 and qubit pair 2, 4. They can not be performed directly by the quantum computer since its topology does not support these interactions. However, the quantum circuit in figure 1 can be mapped by swapping the qubit state of 1 with 4 before and after computing the considered two-qubit quantum gates.

Besides the adaptation to the topology of a quantum computer, quantum circuit mapping may be performed subject to secondary objectives that typically are expected to reduce the incurred error during a quantum algorithm computation. Such secondary objectives are typically the minimization of operations inserted by quantum circuit mapping and the minimization of the resulting quantum circuit depth [16], [36]–[40]. However, further objectives have been proposed such as reduction of concurrent operations that incur crosstalk errors [41], the maximization of circuit fidelity [42], [43] or mapping operations to qubits that have demonstrated lower error rates during calibration protocols [42], [44].

Heuristic [16], [38], [40]–[42], [44] and optimal [36], [37], [39] algorithms for quantum circuit mapping have been proposed. Prior quantum circuit mapping approaches relying on swap gate insertions consider topology graphs that remain constant during the computation of the quantum circuit [36], [38]–[42], [44]. Quantum circuit mapping methods specifically for ion trap quantum computers consider arbitrary qubit-qubit interactions through a sequence of topology graph changes [33], [45]. However, these works do not consider swap gate insertions alongside topology changes. In this work, swap gates and topology graph changes are both considered for quantum circuit mapping.

Fig. 3. Individual steps of the developed quantum circuit mapping method for a quantum circuit \( U \), topology graph \( G' = (P, E') \) and maximal considered time steps \( T \).

V. QUANTUM CIRCUIT MAPPING FOR NEAR-TERM QUANTUM ARCHITECTURES BASED ON RYDBERG ATOMS

In this section we describe how a quantum circuit mapping can be computed by constructing and solving a satisfiability modulo theories (SMT) model \( \mathcal{M} \). Model \( \mathcal{M} \) is the union of a model \( \mathcal{R} \) that describes valid topology changes in a near-term Rydberg architecture and a model \( \mathcal{S} \) that describes the effect of swap gate insertions on the quantum circuit.

Figure 3 shows the steps of the developed quantum circuit mapping method for a quantum circuit \( U \) and a topology graph \( G = (P, E) \). First, the topology graph \( G \) is extended to yield a graph \( G' = (P, E') \) that includes edges for all qubit-qubit interactions that can be supported by valid topology graph changes. The model \( \mathcal{M} = \mathcal{R} \cup \mathcal{S} \) is then constructed from the input quantum circuit \( U \), topology graph \( G' \) and the maximum quantum circuit depth \( T \). A solver then tries to determine valid assignments to \( \mathcal{M} \) subject to further optimization objectives such as the minimization of the quantum circuit depth or the maximization of the circuit fidelity.

If the solver returns a valid assignment to \( \mathcal{M} \), then the obtained quantum circuit mapping is optimal with respect to the chosen objective function. Otherwise, model \( \mathcal{M} \) is modified by increasing the maximum quantum circuit depth \( T \) while retaining the original quantum circuit \( U \) and extended topology graph \( G' \). This process is repeated until a valid assignment to \( \mathcal{M} \), i.e. a quantum circuit mapping, is found. Optimality is guaranteed with this approach, if the value of the employed objective function becomes worse for an increasing quantum circuit depth. Otherwise, a sufficiently large initial maximum quantum circuit depth \( T \) must be chosen that allows arbitrary qubit permutations and topology changes for each computation in the quantum circuit \( U \).

The following sections assume that \( P \) is the set of qubits accessible in a quantum computer, \( Q \) are the qubits in a quantum circuit \( U \) and \( T \) is the maximum quantum circuit depth (or: last time step) considered for quantum circuit mapping. \( R \) (\( C \)) is the number of rows (columns) in the topology and also a function that maps a qubit \( p \in P \) to its corresponding row (column) in \( G \). Constraints that define the domain of a variable \( v \in R \cup S \) have been omitted.

A. Topology Graph Extension

The first step is to construct the extended topology graph \( G' = (V, E') \) according to topology displacements supported by near-term Rydberg atom architectures (see section III). We assume the Rydberg platform to initially have a topology \( G \)

\[ G = (P, E) \]
where qubits are connected to their nearest neighbors and arranged in a $C \times R$ grid. We model arbitrary displacements of qubits in one row along the x-axis of the grid such that the order of the qubits in the row is maintained. The resulting extended topology graph $G'$ is shown in figure 3. Since the qubits can be displaced along the x-axis of the grid, an arbitrary qubit $q$ of row $r$ can interact with an arbitrary qubit $u$ of a neighboring row $r'$. Since the relative position of qubits in the same row may not change, qubits $q, q'$ in the same row can only interact if $(q, q') \in E$, where $E$ is the edge set of the original topology graph $G$. Therefore, the edge set $E'$ of $G'$ is defined by

$$E' = E \cup \{q, u\} \mid q \in r, u \in r'\). \quad (2)$$

The topology graph extension introduces $O(C^2 R)$ edges to $G$ for a $C \times R$ grid.

### B. Modeling One-Dimensional Topology Displacements

The next step in the developed method is to define how a topology graph can change from one time step to another and which edges in $G'$ are available for computation in a specific topology displacement. Given the extended topology graph $G' = (P, E')$ and the maximum considered quantum circuit depth $T$ the model of one-dimensional topology displacements (see section III R) contains the following variables:

- $p_{p, t}, u \in \mathbb{N}$ for $p \in P, \forall t \in \{1, ..., T\}$ — represents the displacement of a qubit $p$ at time $t$, where a value of 0 indicates no displacement, a positive value indicates a displacement to the right side and a negative value indicates a displacement to the left side.
- $EN_{p, u, t} \in \mathbb{B}$ for $p, u \in P, \forall t \in \{1, ..., T\}$ — indicates whether an edge in the extended topology graph $G'$ is available for a multi-qubit computation.

One-dimensional topology displacements are characterized by a fixed order of qubits in the same row for all time steps $t \in T$. Each qubit $p \in P$ is assigned a displacement $\eta_{p, t} \in \mathbb{N}$ that is constrained by:

$$\left(\eta_{p, t} \leq \eta_{r, t}\right) \land \left(\eta_{r, t} \leq \eta_{p, t}\right), \quad (3)$$

where $r \in \{u \in P \mid (C(u) > C(p)) \land (R(u) = R(p))\}$ and $l \in \{u \in P \mid (C(u) < C(p)) \land (R(u) = R(p))\}$.

The displacements of qubit $p$ and qubit $u$ support an edge $e = (p, u) \in G'$ for a multi-qubit quantum gate computation at time $t$ if the displacements are equal

$$EN_{p, u, t} := (\eta_{p, t} = \eta_{u, t}) \quad (4)$$

for qubits $p, u$ that are in the same row and

$$EN_{p, u, t} := (C(p) + \eta_{p, t}) = (C(u) + \eta_{u, t}) \quad (5)$$

for qubits $p, u$ that are in neighboring rows.

A topology displacement may require a runtime of $t_d \in \{1, ..., T\}$ time steps. A mismatch in displacement $\eta_{p, t} \neq \eta_{p, t+1}$ on a qubit $p \in P$ between time step $t$ and $t + 1$ therefore implies that no other operation may be computed on $p$ in $t' \in \{t - t_d, ..., t\}$. The runtime $t_d$ is a user-specified input to the optimization problem based on the experimentally measured duration of the displacement.

### C. Formal Swap Gate Insertion Model

Solving a swap gate insertion model $S$ yields a quantum circuit mapping that inserts swap gates to adapt a quantum circuit $U$ to a topology graph $G$. A swap gate insertion model defines an assignment of qubits $Q$ in a quantum circuit $U$ to the qubits of a quantum computer topology $P$ for each considered time step. Furthermore, each computation $c \in U$ is assigned a location $l \in L = P(P) \setminus \{}$ for each time step.

In general, a swap insertion model $S$ constrains the assignment to the following variables:

- $\pi_{q, t} \in P$ for $q \in Q, \forall t \in \{1, ..., T\}$ — represents the assignment of a qubit $q$ in the input quantum circuit $U$ to a qubit $p \in P$ in the quantum computer.
- $l_c \in L \forall c \in U$ — indicates the location $l$ of a computation in the input quantum circuit $U$.
- $z_c \in \{1, ..., T\}$ for $c \in U$ — indicates the time step $t$ of a computation in the input quantum circuit $U$.

under the following conditions:

- Each computation $c \in U$ is assigned a location $l$ that satisfies the qubit requirement of $c$ and a time $t$ that satisfies the computation order defined in $U$.
- Each $q \in Q$ is assigned at most one $p \in P$, i.e. the assignment $\pi_{q, t}$ is unique at any fixed time step for all qubit $q \in Q$.
- If a computation $c \in U$ is assigned a location $P' = \{p_1, ..., p_n\}$ at time $z_c$, the qubits $Q' = \{q_0, ..., q_n\}$ specified by $c$ must have been assigned to $P'$, i.e $\pi_{q_i, z_c} = p_i \forall q_i \in Q', p_i \in P'$.
- The assignment $\pi_{q, t} = p$ may only change to $\pi_{q, t+1} = p$ if there exists an edge $(p, u)$ in the topology graph $G$.

For each change in qubit assignment $(\pi_{u, t} \neq \pi_{u, t+1})$ a swap gate is inserted into the quantum circuit $U$. Furthermore, operations may have individual runtimes $t_i \in \{1, ..., T\}$ that must be considered, i.e. a qubit $p \in P$ is occupied with at most one operation in any time step $t$.

Combining a swap insertion model $S$ with a model $R$ for topology changes requires two more constraints:

- A swap or multi-qubit computation may only act on pairs of qubits $p, u \in P$ in a certain time step $t$ if $EN_{p, u, t}$ indicates that the edge between $p$ and $u$ is available in the topology at time $t$.
- Either a single-qubit gate, a multi-qubit gate, a topology displacement or a swap gate may act on a qubit at the same time step.

Several formal swap gate insertion models were proposed in the state of the art [37], [39], [43]. The swap insertion model $S$ described in this section is generic and compatible with these approaches. In our experiments reported in section VI we will be using the specific model from [43].
D. Optimization Objectives

Optimization objectives such as minimizing the number of inserted swap gates, maximizing the fidelity of the resulting quantum circuit or minimizing the resulting quantum circuit depth are crucial for obtaining a quantum circuit mapping that incurs low errors on the target quantum computer.

In model $M$, the depth minimization and quantum circuit fidelity can be defined as:

- minimize quantum circuit depth: $\min_{c \in U} z_c$.
- maximize quantum circuit fidelity:
  $$\max \sum_{c \in U} \log(f_c) + \sum_{s \in S} \log(f_s) + \sum_{d \in D} \log(f_d),$$

where $f_c$ is the fidelity of a computation $c$, $S$ is the set of swap gates, $f_s$ is the fidelity of a swap gate $s \in S$, $D$ is the set of one-dimensional topology displacements and $f_d$ is the fidelity of a displacement $d \in D$.

**Example — One-dimensional topology displacements improve quantum circuit mapping:** We will now demonstrate model $M$ on a quantum circuit that can be mapped with less overhead using one-dimensional topology displacements than using only swap gate insertions. Consider the six-qubit quantum circuit and the $3 \times 2$ topology grid $G$ in figure 1. The quantum circuit consists of six two-qubit gates out of which two quantum gates CX(1, 3) and CX(4, 2) cannot be computed on the specified topology graph $G$ directly. Through the developed model $M$, a quantum circuit mapping based on one-dimensional topology displacements or swap gate insertion can be computed.

Let the runtime of the swap gate and the topology displacement be $t_d$ and the runtime of all other operations be $t_i = 1$. The two two-qubit gates to the left of the dashed line in figure 1 can be computed directly in the first time step of the quantum computation. In the case of a quantum circuit mapping using swap gate insertions, the quantum gates CX(1, 3) and CX(4, 2) can be computed in time step $t_d + 2$ by inserting either set of swap gates $s_0 = \{\text{swap}(1,4)\}$ or $s_1 = \{\text{swap}(1,0), \text{swap}(4,5)\}$. If $s_0$ is computed until time step $t_d + 2$, the remaining two-qubit gates can be computed directly and would require another insertion of swap $s_0$. This would lead to a resulting quantum circuit depth of $3 + 2t_d$. If $s_1$ is computed until time step $t_d + 2$, CX(0, 1) requires another swap. In this case, the resulting quantum circuit depth is again $3 + 2t_d$.

VI. Evaluation

In this evaluation, we investigated the improvement in quantum circuit depth and quantum circuit fidelity when introducing one-dimensional topology displacements to quantum circuit mapping in addition to swap gates. The improvement was evaluated for different technology parameters such as the fidelity of swap gates, and the runtime of topology displacements and swap gates.

We evaluated the developed quantum circuit mapping method on quantum circuits with up to 15 qubits and a maximum depth of 76. The evaluated quantum circuits compute arithmetic functions [46], Bernstein-Vazirani (BV) [47] or the quantum Fourier transformation (QFT) [48]. In addition, quantum circuits with multiple layers of two-qubit CX gates between random pairs of qubits were generated and evaluated. For each evaluated quantum circuit with qubits $Q$, the topology graph was chosen to be a $C \times R$ grid where $R$ is the number of rows and $C$ is the number of columns such that $|Q| \leq C \cdot R$ and $C, R$ minimal.

The developed SMT model with the swap gate insertion model from [43] was solved using the Z3 solver [49]. The average runtime of the solver was roughly 20 minutes.

A. Quantum Circuit Depth

Each quantum circuit was successively evaluated with a swap gate and topology displacement runtime ranging from one to four time steps. Figure 6 shows the reduction in quantum circuit depth when using topology displacements in conjunction with swap gates for quantum circuit mapping.

If the runtime of swap gates and topology displacements is equal, the average reduction in quantum circuit depth ranges
from 0.8% to 2% depending on the actual runtime. If the swap runtime is smaller than the topology displacement runtime, the mapping procedure will typically fall back to inserting swap gates instead of using topology displacements unless one topology displacement can solve more qubit-qubit interaction requirements than one swap gate at a particular time step of the quantum circuit computation. For the evaluated quantum circuits, this is never the case if the swap runtime equals one time step and the topology displacement runtime is larger than one time step. However, if the swap runtime is two time steps and the topology displacement runtime is four time steps, a quantum circuit depth reduction of 0.4% on average can be observed.

In contrast, if the swap runtime is larger than the topology displacement runtime, an average quantum circuit depth reduction of up to 31.3% can be observed. The exact quantum circuit depth improvement depends on the ratio $r$ between the swap gate runtime and topology displacement runtime. If this ratio is 2 the reduction in quantum circuit depth is 16.3% on average.

As evident from the diagonal entries of the matrix in figure 6, $rr$ is not the only factor that determines the quantum circuit depth reduction. In the diagonal, the ratio of the two runtimes is always 1, i.e. take the same number of time steps. However, the depth reduction ranges from 0.8% to 2%. This difference stems from the quantum circuit structure, i.e. the number and position of single- and multi-qubit gates.

The impact of the circuit structure is also evident in figure 7. The developed method does not reduce the depth of QFT quantum circuits at any evaluated combination of swap gate runtime and topology displacement runtime. However, for arithmetic quantum circuits, the quantum circuit depth reduction is up to 58.3%. If $r$ is 1, the quantum circuit depth reduction is up to 45%. With decreasing $r$, the structure of the quantum circuit becomes insignificant for the reduction of quantum circuit depth: if the swap gate is twice as fast as the topology displacement, the maximum quantum circuit depth reduction is roughly 13%. At even faster swap gates, the topology displacements do not have a tangible impact on the quantum circuit depth reduction.

**B. Fidelity**

The fidelity was set to 1 for topology displacements since we expect these restricted atom movements through optical tweezers to not have an impact on the quantum state of the qubits. The evaluated quantum circuits were then investigated with a swap gate fidelity of $f_s \in \{0.999, 0.995, 0.99, 0.97, 0.95\}$. Figure 8 shows the improvement in fidelity when using one-dimensional topology displacements in addition to swap gates compared to a quantum circuit mapping with noisy swap gates only. Using topology displacements in addition to swap gates lead to a maximal fidelity improvement of 29% at a swap gate fidelity of 0.95. However, for every evaluated swap gate fidelity there existed quantum circuits whose fidelity did not improve, i.e. no swap gate could be replaced by a topology displacement. At the largest evaluated swap gate fidelity (0.999), the fidelity improved by 0.3% on average. For the lowest evaluated swap gate fidelity (0.95), the quantum circuit fidelity improved by 15% on average. These results show that depending on the exact technology parameters, one-dimensional topology displacements can incur a significant improvement in fidelity or barely have an effect on the fidelity of the quantum circuit computation.

**VII. Conclusion**

In this work a novel optimal quantum circuit method was developed that can exploit one-dimensional topology displacements available in near-term quantum architectures based on Rydberg atoms. For the evaluated quantum circuits and technology parameters, the developed method incurred a quantum circuit depth reduction of up to 58% and a fidelity improvement of up to 29%. We demonstrated that quantum circuit mapping can be improved through one-dimensional topology displacements if the swap gate fidelity is lower than 0.999 or the swap gate runtime is not much lower than the topology displacement runtime. The developed method can be used to map quantum circuits to near-term quantum architectures based on Rydberg atoms and provides technology parameters for experimentalists that can help extend the algorithmic opportunities of near-term Rydberg architectures.
