Frequency signal acquisition of scalar atomic magnetometer based on using TDC and FPGA

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Abstract. An improved equal precision frequency measurement method is presented for acquisition of frequency signal output from high sensitivity scalar atomic magnetometers. The frequency range to be measured is from 75 kHz to 350 kHz with a resolution better than 0.01 Hz, and the sampling rate should be at least 10 Hz. To meet the requirements on dynamic range, measurement accuracy and speed, at least eight significant digits must be kept. The TDC and FPGA are used to improve the traditional equal precision method. The FPGA acts as the controlling and computing centre, while the TDC measures the time deviation to eliminate the counting error of ±1 reference signal. A prototype frequency detector is fabricated and tested. The measured data show that the design is viable and further improvement is possible.

1 Introduction

With the emergence of high-resolution and high-sensitivity magnetometer, aeromagnetic measurements for geologic and resources surveying have drawn much attention [1]. The airborne scalar atomic magnetometer plays the key role to collect the magnetic anomaly fields. However, the magnetic sensors usually do not give the magnetic field values directly but output the Larmor precession frequencies. Typically, the range of measured magnetic field is 20000nT-100000nT, the accuracy is 0.005nT, and the sensitivity is 0.0006nT [2]. The corresponding Larmor coefficient between the magnetic field signal and the frequency signal is 3.49857 Hz/nT for Cs atomic magnetometer, thus the range of frequency output from the magnetometer is 70kHz-350kHz. Because the accuracy of the magnetometer is 0.005nT, and the range of geomagnetic field in China does not exceed 60000nT, eight significant digits of collected data is the minimum requirements, that is, the accuracy of frequency acquisition must keep up to at least eight significant digits. Also, it is usually required that the data acquisition rate is at least 10 Hz, thus the collector acquisition speed must be high enough. The traditional frequency measurement methods, including the direct frequency measurement and periodic frequency measurement methods, are all hard to meet the requirements on acquisition speed and acquisition accuracy simultaneously.

The purpose of this paper is to design a frequency detector that can meet the abovementioned requirements. The key elements to be used include the Time-to-Digital Conversion (TDC) chip and the FPGA. The design is based on the equal precision frequency measurement method. The FPGA is used as a controlling and computing centre in the scheme, and the TDC is used to accurately measure the time deviation existing in the two ends, which can effectively eliminate the ±1 reference signal.
counting error in equal precision frequency measurement method. We will demonstrate that both the measurement accuracy and measurement speed can meet the requirements.

2 Improvement of equal precision frequency measurement Method

The measuring principle of equal precision frequency measurement method is described as follows. The measured signal period is counted during the preset gate, and the count value is \( M \). We take this \( M \) cycle time as the actual gate, and the reference signal period is counted during the actual gate. The count value is \( N \) \cite{3}. The waveform diagram and block diagram of the equal precision frequency measurement method are shown in Figure 1 and Figure 2, respectively. It is apparent that the frequency of the signal to be measured is

\[
f_x = \frac{M}{N} f_0
\]  

(1)

where \( f_0 \) is the frequency of the reference signal.

![Figure 1: The principle waveform diagram](image1)

![Figure 2: The principle block diagram](image2)

As it can be seen from the waveform diagram, the counting time of counter 2 is not synchronized with the actual gate, so that there exists a count error of ±1 reference signal. This is the most important measurement error of the equal precision frequency measurement method.

The ACAM company’s TDC chip is based on the signal through the internal gate of the transmission delay to carry out high-precision time interval measurement \cite{4,5}. It has two measurement ranges. In the range 1, the minimum resolution is 65ps, measuring range is 2.0ns-1.8us, and the two stop channels share a start channel. Figure 3 shows this gate circuit delay structure.
Using the TDC chip to measure the time deviation between the counting time of the counter 2 and the actual gate, it is possible to eliminate the counting error of ±1 reference signal, thereby correcting the count result $N$ of the counter 2, and to achieve the purpose of improving the measurement accuracy [7]. The waveform of its measurement principle is shown in Figure 4:

$\Delta u = \frac{dt'_0}{dt'} - \frac{dt'_0}{dt}$

Thus, the measured signal $f_x$ of (1) is modified to be

$$f_x = -\frac{M}{N - \Delta u} f_0$$

3 Gray code counter

In this paper, the counter 1 and counter 2 are Gray code counters. Gray code has a distinct feature, that is, any two adjacent numbers are only one bit different, and this feature plays an important role in the digital system. In binary count, there are usually difference of many bits between two adjacent numbers. For instance, there are 5 bit changes from 01111 to 10000, but in the actual circuit, this 5 bit changes cannot happen at the same time. Some other uncertain codes (such as 11111, 00000, etc.) may
appear temporarily in the count, which may lead to circuit status errors and result in unpredictable results.

Counter 1 and Counter 2 are 32-bit Gray code counters. After the count is complete, the Gray code is converted into a binary code to obtain the binary $M$ and $N$ for the calculation of the formula (3). In this design, the structure of 1-bit and 3-bits Gray code counters are shown in Figure 5 and Figure 6, respectively. Other Gray code counters are similar.

4 Design and measurement results
We chose the Altera Corporation Cyclone IV series EP4CE22F17C6N FPGA chip. It is low cost, has excellent performance, can meet the design needs. The reference signal is provided by a high-stability, high-precision thermostatic crystal oscillator ROX252S4 with a stability up to 1E-8. The structure block diagram of the collector is shown in Figure 7, and the main hardware circuit is shown in Figure 8.

As it is shown in the figures, the FPGA acts as a control centre that controls the TDC’s operating mode, initiates and stops the measurements. When the TDC measurement is completed, the FPGA receives the TDC measurement data through the SPI and completes the solution of the formula (2) to
obtain the time deviation $\Delta u$. At the meantime, the FPGA counts the frequency signal $f_x$ and the reference signal $f_0$ in the gate time to obtain $M$ and $N$. Then FPGA calculates the accurate $f_x$ by (3) and sent it to the next module for analysis and processing. To complete the above tasks, the FPGA resources are used, and the utilization is shown in Figure 8.

![Figure 8: The utilization of FPGA](image)

A prototype frequency detector has been designed and fabricated according to the description above. A total of five times of measurements have been carried out and the results are given in Table 1. The measured data show that the minimum accuracy of the collected data has reached eight significant digits when the gate time is 100ms. It can be seen from the Table 1 that the maximum frequency error is smaller than 0.05 Hz, which amounts to an error for magnetic field value 0.014 nT. It can be estimated that the standard deviation is smaller than 0.023 Hz, which amounts to an error for magnetic field value 0.0065 nT.

![Figure 9: Main hardware circuit diagram](image)
Table 1: The measurement results (kHz)

| True Value | First Time      | Second Time     | Third Time      | Fourth Time     | Fifth Time      |
|------------|----------------|-----------------|-----------------|-----------------|-----------------|
| 70         | 69.999950280   | 69.999950450    | 69.999950445    | 69.999950494    | 69.999950678    |
| 100        | 99.999980301   | 99.999980716    | 99.999980690    | 99.999980590    | 99.999980574    |
| 200        | 199.99999013   | 199.99999013    | 199.99999012    | 199.99999015    | 199.99999014    |
| 300        | 300.000000624  | 300.000000609   | 300.000000617   | 300.000000621   | 300.000000630   |
| 350        | 350.000000412  | 350.000000425   | 350.000000408   | 350.000000465   | 350.000000423   |

5 Conclusion
An improved equal precision frequency measurement method based on using TDC and FPGA is proposed in this paper. It may be used for frequency signal acquisition output from a high-sensitivity scalar atomic magnetometer. The design and fabrication cost is not expensive. Investigation to further increase the significant digits is underway.

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