Analysis of on-off current ratio in asymmetrical junctionless double gate MOSFET using high-\textit{k} dielectric materials

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**ABSTRACT**

The variation of the on-off current ratio is investigated when the asymmetrical junctionless double gate MOSFET is fabricated as a SiO$_2$/high-\textit{k} dielectric stacked gate oxide. The high dielectric materials have the advantage of reducing the short channel effect, but the rise of gate parasitic current due to the reduction of the band offset and the poor interface property with silicon has become a problem. To overcome this disadvantage, a stacked oxide film is used. The potential distributions are obtained from the Poission equation, and the threshold voltage is calculated from the second derivative method to obtain the on-current. As a result, this model agrees with the results from other papers. The on-off current ratio increases as the permittivity of the high dielectric material increases, but that is saturated at the relative permittivity of 20 or more. The on-off current ratio is in proportion to the arithmetic average of the upper and lower high dielectric material thicknesses. The on-off current ratio of 10$^4$ or less is shown for SiO$_2$, but the on-off current ratio for TiO$_2$ (\textit{k}=80) increases to 10$^7$ or more.

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1. INTRODUCTION

Recently, transistors used in system and memory semiconductors form a three-dimensional structure. The most commonly used transistor is the FinFET structure, which has three gates formed around the channel to more effectively control the charges in the channel. Three-dimensional transistors have been studied in various forms such as not only FinFET structure but also double gate (DG) structure and cylindrical structure [1]-[5]. In particular, the double gate structure is developing the junctionless accumulation type, doping the source, drain and the channel equally as well as the junction-based inversion type [6]-[10]. It is reported that the process is easier and the short channel effects are reduced further in the junctionless accumulation type than the inversion type DGMOSFET [11]-[13]. Scaling not only increases channel doping but also greatly reduces the gate oxide thickness. In general, a problem of increasing the gate parasitic current from quantum-mechanical tunneling has been proposed when the thickness of SiO$_2$ used as a gate oxide film decreases [14]-[15]. As described above, the gate parasitic current increases due to the decreasing in the gate oxide thickness. To solve this problem, an oxide film with a high permittivity is being used. A thicker thickness can be used in a high permittivity oxide than SiO$_2$ since the EOT is increased to maintain the same gate capacitance. Thus, the oxidation process will be very easy. However, dielectric materials with high permittivity have difficulty in forming good interface with the silicon channel and have smaller band gaps than SiO$_2$, causing another problem [16]. To solve this problem, researches are being made.

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to stack SiO$_2$ and high permittivity materials [17]-[20]. In this case, not only the interface with the silicon channel is excellent but also the band-offset between silicon and the high permittivity materials can be increased [21]. Increasing the band offset is an important factor in reducing the gate parasitic current.

In this paper, we analyze the on-off current ratio of the asymmetrical junctionless double gate (JLDG) MOSFET having stacked gate oxide film using high-$k$ dielectric materials and SiO$_2$. The on-off current ratio is used as a measure of the parasitic current in the subthreshold region and is an important short channel effect [22]-[24]. Amin et al. analyzed the gate tunneling currents in the symmetrical junctionless DGMOSFETs using SiO$_2$/high-$k$ stacked gate oxide films [25]. Priya et al. presented the subthreshold swing of the junctionless DGMOSFET when the dielectric materials of gate oxide films were SiO$_2$, Al$_2$O$_3$, Y$_2$O$_3$, HfO$_2$/ZrO$_2$, La$_2$O$_3$, and TiO$_2$ with the relative permittivities of from 3.9 to 80 [26]. In this paper, we analyze the on-off current ratio according to channel dimension, oxide thickness, and permittivity of oxide film for the junctionless DGMOSFET with stacked gate oxide, using potential distribution model that can be used in symmetrical as well as asymmetrical JLDG MOSFET. For this purpose, the potential distribution model presented by Ding et al. for the asymmetrical DGMOSFET is revised to be applied to the asymmetrical JLDG MOSFET [27]. The on-off current ratio will be analyzed when the permittivities of stacked upper and lower gate oxides are different, using the threshold voltage model suggested.

2. THE ON-OFF CURRENT AND THRESHOLD VOLTAGE OF THE ASYMMETRICAL JLDG MOSFET

Figure 1 shows a cross-sectional view of the asymmetrical JLDG MOSFET. The channel as well as the source/drain is heavily doped with $n^+$, and the gate metal is $p^+$ polysilicon. $\varepsilon_{SiO2}$ is a permittivity of SiO$_2$ used to maintain the excellence and band-offset of the interface with silicon channel, and a thickness is 1 nm. The $\varepsilon_1 = k_1\varepsilon_0$ and $t_{ox1}$ represent the permittivity and the upper gate oxide thickness with the relative permittivity $k_1$, respectively, and the $\varepsilon_2 = k_2\varepsilon_0$ and $t_{ox2}$ represent the permittivity and the lower gate oxide thickness with the relative permittivity $k_2$, respectively. The relative permittivity are simulated for the range of between 3.9 and 80. These ranges are the relative permittivities of generally used dielectric materials such as SiO$_2$, Al$_2$O$_3$, Y$_2$O$_3$, HfO$_2$/ZrO$_2$, La$_2$O$_3$, and TiO$_2$. $V_{gt}$ and $V_{gb}$ are applied to the upper and lower gate contacts, respectively, and $V_s$ is the voltage applied at the source and $V_d$ at the drain voltage. To obtain the potentials in the channel of the asymmetrical JLDG MOSFET, the following Poisson equation is used [27].

$$\frac{\partial^2 \phi(x, y)}{\partial x^2} + \frac{\partial^2 \phi(x, y)}{\partial y^2} = \frac{qN_d}{\varepsilon_{si}}$$  \hspace{1cm} (1)

Where $\varepsilon_{si}$ is the permittivity of silicon, and $N_d$ is channel doping concentration. Boundary conditions required when solving (1) are indicated in the references [27]. As a result, the potential distribution is as in (2):

$$\phi(x, y) = V_s + \frac{V_d x}{L_x} + \sum_{n=1} \left( C_n e^{n\pi y/L_y} + D_n e^{-n\pi y/L_y} - f_n L_y/n\pi \right) \sin \frac{n\pi x}{L_x}$$  \hspace{1cm} (2)

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\[
f_n = \begin{cases} \frac{4qN_d}{n \pi \nu}, & n: \text{odd positive integer} \\ 0, & n: \text{even positive integer} \end{cases} \quad k_n = \frac{n \pi}{L_n},
\]

where the constant \(C_n\) and \(D_n\) denoted in reference [28].

The on-current is the drain current corresponding to the threshold voltage and off-current is the drain current at \(V_{gd}=V_{gs}=0\) V. To calculate the threshold voltage by the second derivative (SD) method [29] in the drain current vs. the gate voltage curve, the current-voltage equation is used.

\[
I_d = \frac{q n_i \mu_n W k T}{L} \left[ 1 - \exp \left( -\frac{-q V_d}{k T} \right) \right] \int_0^{\phi_n} \exp \left( \frac{q \phi(x, y)}{k T} \right) \, dx
\]

where \(k, T, n_i, \mu_n\) and \(W\) are Boltzmann’s constant, absolute temperature, the intrinsic electron concentration, the electron mobility, and a channel width, respectively.

The relationship between the drain current and gate voltage, the threshold voltage obtained using the SD method, and the corresponding ratio of on-off current, \(I_{on}/I_{off}\), are shown in Figures 2(a) and 2(b). Figure 2 is the results in the case of the channel length 20 nm, silicon thickness 10 nm and \(t_{ox1}=t_{ox2}=t_{SiO2}=1\) nm. Also, the case of the relative permittivity of \(k_1=k_2=3.9\) for the upper and lower gate oxide films is compared with that of the asymmetrical structure having the relative permittivity of \(k_1=9\) for the high-\(k\) upper gate oxide and the relative permittivity of \(k_2=25\) for the high-\(k\) lower gate oxide.

![Figure 2](image)

**Figure 2.** The relationship between the drain current and gate voltage; (a) extractions of \(I_{on}/I_{off}\) ratio and (b) threshold voltages derived from SD method when the parameters are the relative permittivities of the upper and lower oxides

As shown in Figure 2(b), the threshold voltage defines as the peak of the second derivative derived from the drain current-gate voltage relationship extracted by (3). The drain current at the corresponding threshold voltage is extracted from Figure 2(a). In addition, the current at \(V_{gd}=V_{gs}=0\) V is extracted to determine the on-off current ratio. As known in Figure 2(a), the threshold voltage increases from 0.54 V to 0.72 V, and the on-off current ratio increases about 450 times from \(2.8 \times 10^4\) to \(1.27 \times 10^7\) when the relative permittivities of the upper and lower gate oxide increase from \(k_1=k_2=3.9\) to \(k_1=9\) and \(k_2=25\). It can be found
that the increasing of power dissipation due to the increase in the threshold voltage can not only be offset by the increase in the on-off current ratio but also can be greatly reduced. In this paper, we observe the change of the on-off current ratio due to the change of channel dimension, the upper and lower oxide thickness and, the relative permittivities of the upper and lower oxides through this calculation process.

3. THE ON-OFF CURRENT RATIO OF THE ASYMMETRICAL JLDG MOSFET

To demonstrate the validity of this method, the on-off current ratios are compared with those of the published paper [17] in Figure 3. It can be seen that it agree well with the model of Islam et al. [17], which has fixed relative permittivities of \(k_1=7\) and \(k_2=20\), respectively. It was found that the on-off current ratio is greatly increasing as compared with the case of only using SiO\(_2\) as the upper and lower gate oxide films. Therefore, the change of the on-off current ratio is investigated using the model presented in this paper.

![Figure 3. Comparisons of \(I_{\text{on}}/I_{\text{off}}\) ratio of this model and the reference paper [17] for the asymmetrical JLDG MOSFET](image)

Figures 4(a) and 4(b) indicate the changes in the on-off current ratio in the case of using SiO\(_2\), Al\(_2\)O\(_3\), Y\(_2\)O\(_3\), HfO\(_2\)/ZrO\(_2\), La\(_2\)O\(_3\), and TiO\(_2\) as the high-\(k\) upper and lower gate oxide films. This is the case of fixing the upper and lower gate oxide film thickness with \(t_{\text{ox1}}=t_{\text{ox2}}=1\) nm. As found in Figure 4(a), the on-off current ratio increases as the relative permittivity of the high-\(k\) upper and lower gate oxide films increases. Figure 4(a) shows the same result even when the relative permittivities of the upper and lower gate oxides are interchanged.

In Figure 4(a), the dots are the case where the relative permittivities of the upper and lower gate oxides are equal. In other words, it is the case that a DGMOSFET has a symmetrical structure. Compared to the case of the symmetrical structure, the on-off current ratio is increasing when the relative permittivity is high at either the upper or the lower. It can also be observed that the on-off current ratio saturates as the relative permittivity increases.

Namely, it is observed that the increasing rate of the on-off current ratio is significantly decreased when anyone among the relative permittivities of the high-\(k\) upper and lower gate oxides is 20 or more. The on-off current ratio is shown in Figure 4(b) according to the channel length for the symmetrical JLDG MOSFET having the equal structure of the upper and lower gate oxides. As shown in Figure 4(b), as the channel length decreases, the short channel effect is observed while the on-off current ratio decreases significantly. As described above, the on-off current ratio is saturated when the relative permittivity is 20 or more. Especially, the on-off current ratio is around \(10^4\) at the channel length 20 nm in the case of SiO\(_2\) but increases to around \(10^6\) in the case of TiO\(_2\). Therefore, the use of SiO\(_2\) can be pointed out as a big problem in terms of the on-off current ratio as the channel length reduces.

In addition to the channel length, the silicon thickness also affects the short channel effect. The change of the on-off current ratio with the change of silicon thickness is shown in Figure 5(a). As the silicon thickness is increased, the short-channel effect occurs seriously and the on-off current ratio decreases rapidly as observed in Figure 5(a). Unlike the channel length, the change of the on-off current ratio for the silicon thickness was almost constant with the change of the silicon thickness. Comparing with Figure 4(b), the on-off current ratio can increase to more than \(10^8\) even in SiO\(_2\) in the case of the silicon thickness of less than 7 nm even if the channel length is 20 nm. Thus, the change of silicon thickness has a greater influence on the
on-off current ratio than the change in the channel length. As known in Figures 4(b) and 5(a), the on-off current ratio shows a large change according to the relative permittivity when the relative permittivities of the high-k upper and lower gate oxides are 20 or less. Therefore, the on-off current ratio may be stably maintained if the high-k gate oxide film having a relative permittivity of 20 or more is used.

Using the oxide thickness as a parameter, the on-off current ratio according to the change of the relative permittivity is shown in Figure 5(b). As the oxide thickness reduces, the on-off current ratio increases as shown in Figure 5(b). The smaller the relative permittivity of the high-k gate oxide film is, the more sensitive the on-off current ratio is for the change of the oxide film thickness. In particular, in the case of SiO₂ with a relative permittivity of 3.9, the on-off current ratio decreases from 10⁴ for the oxide thickness 1 nm to about 2 for the gate oxide thickness 3 nm. Therefore, in the case of SiO₂, the oxide thickness should be kept below 1 nm.

Figure 4. \( I_{on}/I_{off} \) ratios; (a) with the relative permittivities as parameters, and (b) with channel length as parameter for the asymmetrical JLDG MOSFET

Figure 5. \( I_{on}/I_{off} \) ratios; (a) with silicon thickness as parameter, and (b) with the high-k oxide thickness as parameter for the symmetrical JLDG MOSFET

It is very difficult to fabricate an oxide film of less than 1 nm, so a new oxide material must be used. Note that the difference of the \( I_{on}/I_{off} \) due to the change in the oxide film thickness is to a negligible extent as the relative permittivity increases. In particular, in the case of TiO₂ with a relative permittivity of 80, the change in the on-off current ratio according to the change in the oxide thickness can be almost ignored. As such, when a dielectric having a high relative permittivity is used as the gate oxide, the on-off current ratio may be increased even if there is the problem of a reduction in the band gap and the band offset to operate as the oxide film.

Figure 6 shows the on-off current ratio according to the arithmetic average for the thicknesses of the high-k upper and lower gate oxides when a parameter is the relative permittivity. The relative permittivities
corresponding to the points of each graph are indicated, and the results of the curve fitting into $ab^x$ are shown with the line in Figure 6. By the exponential fitting, the relationship of (4) is established between the on-off current ratio and the arithmetic average of the high-\textit{k} upper and lower gate oxide thicknesses.

$$I_{on}/I_{off} = ab^{(t_{ox1}+t_{ox2})/2}$$

$$\log(I_{on}/I_{off}) = \log a + \log b \left( \frac{t_{ox1} + t_{ox2}}{2} \right)$$

(4)

The values of $\log a$ and $\log b$ are described in Table 1 for the relative permittivity. As can be observed in Figure 6, the logarithmic on-off current ratio is linearly proportional to the arithmetic average for the thicknesses of the upper and lower gate oxides. It can be found that the on-off current ratio reduces as the relative permittivity decreases. Also, the absolute value of $\log b$ representing the rate of change of the on-off current ratio for the arithmetic average of the high-\textit{k} oxide thickness reduces with the increasing of the relative permittivity as known in Table 1. In the case of SiO$_2$, the absolute value of $\log b$ is about six times larger than that of TiO$_2$, and the on-off current ratio decreases rapidly as the arithmetic average of the high-\textit{k} upper and lower oxide thickness increases. It can be seen that the SiO$_2$ ($k = 3.9$) shows a low on-off current ratio of $10^4$ below even with an arithmetic mean of about 1 nm in the simulated conditions. As the relative permittivity increases, the changing rate of the logarithmic value of the on-off current ratio for the arithmetic average of the oxide thickness decreases; in particular, it is found that the change in the oxide thickness was hardly affected in case of TiO$_2$. That is, the on-off current ratio shows less than one-order change when the arithmetic average of the high-\textit{k} upper and lower gate oxide thicknesses varies from 1 nm to 5 nm. Also, it can be observed that as the arithmetic mean for the thickness of the high-\textit{k} upper and lower gate oxide films increases, the on-off current ratio greatly changes according to the relative permittivity.

![Figure 6. $I_{on}/I_{off}$ ratios for the arithmetic average of the high-\textit{k} upper and lower gate oxide thicknesses with the relative permittivity as parameter](image)

| Relative permittivities | $A$ (log$a$) | $B$ (log$b$) |
|-------------------------|--------------|--------------|
| 3.9                     | $5.55 \times 10^7$ | 0.053 |
|                         | (4.74)       | (-1.28)     |
| 9                       | $4.20 \times 10^7$ | 0.056 |
|                         | (7.62)       | (-1.25)     |
| 15                      | $1.34 \times 10^8$ | 0.122 |
|                         | (8.13)       | (-0.91)     |
| 25                      | $2.23 \times 10^9$ | 0.242 |
|                         | (8.35)       | (-0.62)     |
| 30                      | $2.49 \times 10^9$ | 0.295 |
|                         | (8.40)       | (-0.53)     |
| 80                      | $3.18 \times 10^9$ | 0.598 |
|                         | (9.50)       | (-0.22)     |
4. CONCLUSION

In this paper, the on-off current ratio of the asymmetrical JLDG MOSFET using the stacked gate oxide has been analyzed. The on-off current ratio is the measure of a parasitic current in the subthreshold region and affects power dissipation. The threshold voltage was extracted by SD method for on-current determination, and the validity of the presented model was proved by comparison with the published paper. As the relative permittivity of the high-$k$ oxide increased, the on-off current ratio increased, and the change in silicon thickness had a more influence on the on-off current ratio than the channel length. The on-off current ratio was saturated when the high-$k$ gate oxide films with a relative permittivity of 20 or more were used in the upper and lower. In a DGMOSFET having a channel length 20 nm and a silicon thickness 10 nm, an on-off current ratio showed about $10^4$ nm in the case of SiO$_2$ when the thickness of the high-$k$ oxide is 1 nm, but the on-off current ratio can be increased to $10^5$ or more if a material having a relative permittivity of 20 or more is used. The logarithmic on-off current ratio was linearly in proportion to the arithmetic average of the high-$k$ upper and lower oxide thicknesses, and the rate of change of the on-off current ratio for the arithmetic average increased as the relative permittivity decreased, but the on-off current ratio is reduced significantly with decreasing of the relative permittivity. Particularly, it was observed that it was hardly affected by the change in the oxide film thickness when TiO$_2$ ($k=80$) was used as the high-$k$ oxide film. Therefore, a reasonable on-off current ratio can be obtained even at the thick gate oxide thickness and the band-offset that occurs at the interface of the silicon channel and the high-$k$ dielectric material can be reduced, and interfacial nonuniformity may be solved due to the smooth interface between silicon and SiO$_2$ if the gate oxide is stacked with SiO$_2$ and a high-$k$ dielectric material in an asymmetrical JLDG MOSFET.

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