Design and implementation of carry Look ahead generator in reversible logic using nano QCA

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Abstract

The idea of reversible logic is another emerging architecture that has developed its ground in research area. This argument implied zero heat dissipation at the device. According to the physical laws of quantum mechanical effect and the law of coulomb the function and heat relations are satisfied. In this paper, a carry-looking generator is built using reversible logic and its QCA have been reported. To achieve the proposed design use was made of Toffoli and BJN gate. Comparing simulation outcomes to theoretical values verifies the design. The proposed model is tested and simulated using version 2.0.3 of the QCA Designer method.

Keywords: Quantum dot Cellular Automata (QCA); Reversible logic; Toffoli and BJN gate; QCADesigner

1. Introduction

A power consumption is the most difficult field in nano scale logic design. There is a growing need for a new technology that can provide less power dissipation nano size circuits. QCA provides high density applications, low power consumption and high switching speed [1]. Because of these properties quantum gates were targeted for their enabling computational reversibility functions. The computing systems’ weakness of heat dissipation is the primary driving force that draws attention to reversibility. Reversible logic preserves the knowledge that is similar to energy and momentum conservation in physics.

The reversibility inherent leads to a new frame function, which results in zero heat dissipation. In QCA reversibility is one to one mapping of output inputs. Landau indicated in 1961 that the loss of one bit of information cost would be greater than the amount of KTLn2 energy joules [2]. This indicates the irreversible processes do not maintain information and are loss-making. In addition to the strength of the theoretical definition, some essential interpretation was obtained by Bennet. The Bennet clock mechanism achieves less power dissipation than the KTLn2 switch. Reversibility is a notion that requires bijective action. It indicates both
backward and forward tracks for a machine are possible at any time \cite{9}. Care should be taken when developing reversible logic circuit mapping, as fanout is not permitted. The Contribution list is as follows.

- The building blocks of a reversible system should be individually reversible.
- The number of inputs and outputs has to be always equal.

The emerging reversibility concept attracts the VLSI designer because CMOS suffers the nano-scale power dissipation problem. If used successfully to design reversible circuits, the new design will lead to ultra low-power systems.

2. Background

2.1 QCA REVIEW

Craig Lent and Al have developed a new paradigm of the calculation architecture called Quantum dot Cellular Automata to address the problem of size reduction in CMOS technology. QCA cells were realised through several physical implementations of these semi-conductor methods and metal islands are the most promising because of their high density of operation and integration \cite{3}.

There are four quantum dots to this QCA technology consisting of an array of cells each. The electrons occupy two Quantum Points diametrically opposite. There are two polarisation levels, which correspond to the electrons. The polarisation is \( P=+1 \) when the electrons are in the lower left and higher right and the polarisation \( P=-1 \) when it is in the lower right and higher left as shown in Figure 1. The planar crossings may also be achieved by using a turned version 45° of a cell \cite{8}.

![Figure 1 QCA cell with four quantum dots](image)

The logical information can propagate from the input to the output of the cell by the force of repulsion. The fundamental QCA logic primitives are QCA wire, QCA inverter and QCA majority gate \cite{7}. The binary signal propagates from input to output because of electrostatic interactions. 90° and 45° QCA wires can be used as shown in the Figure 3. The QCA inverter is created by orienting the cells at 45° to each other to take opposite polarizations as shown in below Figure 2.

![Figure 2 QCA inverter](image)
2.2 QCA CLOCKING

Synchronization and energy restoration are important to proper QCA signal propagation [4]. This can be obtained by implementing unique clocking scheme in four phases as shown in Figure 4. The Launder and Bennet are suggesting two forms of clocking. Typically, the Launder clocking scheme is used in circuits.

It has four distinct zones flipping, keeping, releasing and relaxing where each zone is moved by 90° relative to the previous zone as shown in Figure 5. The clocking strategies in combination with design strategies will contribute to the idea of physical reversibility. More over each QCA clock zone consists of at least two cells to maintain the clock zone effect as mentioned in Table 1.

![Figure 3 QCA wire](image)

![Figure 4 Clocking in QCA](image)

![Figure 5 Clock phase shift in QCA](image)
2.3 REVERSIBLE COMPUTING

When the input bits are lost some amount of energy is wasted. Reversible logic circuits, by recycling energy into the device, prevent energy loss [5]. When coupled with logic gates, Bennet suggested that very low power consumption is possible in logic circuits.

A gate is reversible when each separate input has a distinct output. The reversible gates are one of the benefits of being balanced. Combining the reversible gate with no constant inputs a circuit satisfies the functions of the balance.

We can use garbage outputs to satisfy unbalanced functions [6]. Reversible computing analyses the ratio of the resources used to logical computation. It can be calculated at logical level by one to one configuration between the circuit.

To prevent the destruction of data bits during logical operation, they are designed to reduce power consumption. The data bits in reversible computation are preserved that lead to the development of reversible gate. The reversible gate should have the following characteristics,

- Minimum garbage outputs.
- Minimum input constants.
- Minimum area.
- Minimum number of gates.

Several reversible gates have been developed as shown in the Figure 6. Two important types are Toffoli and BJN gate.

| Clock Pulse | Potential Barrier | Polarization state of the cells |
|-------------|-------------------|--------------------------------|
| Hold        | Held High         | Polarized                      |
| Switch      | Low to High       | Polarized                      |
| Relax       | Low               | Polarized                      |
| Release     | Lowered           | Polarized                      |

Table 1 Operation of QCA clock pulses

Figure 6 Reversible gates
3. Proposed Work

3.1 BJN Gate

The BJN gate is a three input reversible gate that maps input to corresponding output. Here, \((A, B, C)\) are the inputs and \((P, Q, R)\) are outputs. The BJN gate is shown in the Figure 7.

![Figure 7 BJN Gate](image)

The Reversible carry lookahead generator operates based on AND and OR gates. By setting the third input to zero, the BJN gates can be made to perform OR operation between the first two inputs. Figure 8 indicates an OR gate centred on the BJN port. The QCA representation Diagram of BJN gate is shown in the Figure 9.

![Figure 8 BJN Based OR Gate](image)

![Figure 9 QCA Representation of BJN Gate](image)

3.2 TOFOLLI Gate

The Tofolli gate is a three input reversible gate that maps input to corresponding output. Here, \((A, B, C)\) are the inputs and \((P, Q, R)\) are outputs. The Tofolli gate is shown in the Figure 10.

![Figure 10 TG Gate](image)

The lookahead generator Reversible Carry operates based on AND and OR gates. By setting the third input to zero the Tofolli gates can be made to perform AND operation between the first two inputs. Here the garbage values are the outputs \(P\) and \(Q\), and \(R\) is equal to \(A.B\). Figure 11 displays AND gate dependent on Tofolli. The QCA representation Diagram of TG gate is shown in the Figure 12.
3.3 Carry Lookahead Generator

In successive binary addition the speed of adding is restricted by propagation time for carry information. If the signal has no enough time to propagate, the outcome will not be accurate. The most commonly used technique to reduce carry propagation time is the carry lookahead logic.

The concept of generating and propagating the carries is used in this. The general logic expression carry lookahead generator is

\[ C_{i+1} = G_i + P_i C_i \]  

(1)

Here \( C_i \) is the input carry at stage \( i \), \( G_i \) represents carry generate \( G(A,B) \) is used to represent the binary predicate.

\[ G(A,B) = A \cdot B \]

\[ P_i C_i = A \oplus B, \]  

it represents the carry propagate, as it shows the carry of \( i \)th signal broadcast into the \((i+1)\)th stage (i.e) whenever \( P_i = 1 \), the input carry will be propagated to the corresponding output carry. In case if the \( P_i = 1 \) the carry generate is 0, then eqn(1) can be written as \( C_{i+1} = C_i \). Thus if \( C_i = 1 \), the input of 1 origins an output carry of 1. Similarly if \( C_i = 0 \) the output carry of 0 is originated. The value of \( P_i \) depends on input of \( A_i \) and \( B_i \),

\[ P(A,B) = A + B \]

where A+B is logical disjunction. By substituting the value of ‘i’, the output for three bit logic circuit can be written as,

\[ C_1 = G_0 + P_0 C_0 \]  

(2)

\[ C_2 = G_1 + P_1 C_1 \]  

(3)

\[ C_3 = G_2 + P_2 C_2 \]  

(4)

The logic circuit is shown in figure 13. The three bit carry lookahead generator circuit requires six AND and three OR operations.
The reversible gates are used for these operations. The reversible carry three toffol gates and three BJN gates. QCA-based logic expression of the proposed three-bit reversible carry lookahead generator.

\[
\begin{align*}
    c_1 &= r_2(r_1(p_0,c_0,0),g_0,0) \\
    c_2 &= r_2(r_1(p_1,c_1,0),g_1,0) \\
    c_3 &= r_2(r_1(p_2,c_2,0),g_2,0)
\end{align*}
\]

The corresponding circuit in QCA is given in the Figure 14 and the outputs are compared with truth table for circuit of carry lookahead generator as mentioned in Table 2.

The carry lookahead generator circuit in QCA structure is shown in Figure 15.
4. Result Analysis

4.1 Simulation Parameters

The design implementation and simulation is achieved through QCADesigner 2.0.3. The bistable simulation is carried out with 18X18 nm QCA cell.

4.2 Simulation output of Toffoli gate

The simulation result of the proposed Toffoli Reversible Gate based AND gate is shown in the Figure 16 and the result is compared with truth table as shown in the Table 2.

4.3 Simulation output of BJN gate

The simulation result of the proposed BJN Reversible Gate based OR gate is shown in the Figure 17 and the result is compared with the truth table as shown in the Table 2.
4.4 Simulation output of carry look ahead adder

The simulation result of the proposed carry lookahead generator using toffoli and BJN reversible gate is shown in the Figure 18 and the result is compared with the truth table as shown in the Table 2. The performance analysis of BJN, Tofolli and CLAG circuit is been shown in the Table 3 with its cell count and cell area.
5. Conclusion

This paper has been planned and implemented using the Toffoli and BJN gates in QCA nano technology, reversible full adder and carry look forward generator. The circuit operation has been checked according to the table of truths. This carry lookahead generator circuit will serve as a significant building block for the design of faster reversible parallel adder with low energy dissipation.

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