Woodpecker-DL: Accelerating Deep Neural Networks via Hardware-Aware Multifaceted Optimizations

Yongchao Liu, Yue Jin, Yong Chen, Teng Teng, Hang Ou, Rui Zhao, Yao Zhang
Ant Group, China
{yongchao.ly, jinyue.jy, cy119846, teng.t, ouhang.oh, rui.rz, yao.zhang}@antgroup.com

Abstract

Accelerating deep model training and inference is crucial in practice. Existing deep learning frameworks usually concentrate on optimizing training speed and pay fewer attentions to inference-specific optimizations. Actually, model inference differs from training in terms of computation, e.g., parameters are refreshed each gradient update step during training, but kept invariant during inference. These special characteristics of model inference open new opportunities for its optimization. In this paper, we propose a hardware-aware optimization framework, namely Woodpecker-DL (WPK), to accelerate inference by taking advantage of multiple joint optimizations from the perspectives of graph optimization, automated searches, domain-specific language (DSL) compiler techniques and system-level exploration. In WPK, we investigated two new automated search approaches based on genetic algorithm and reinforcement learning, respectively, to hunt the best operator code configurations targeting specific hardware. A customized DSL compiler is further attached to these search algorithms to generate efficient codes. To create an optimized inference plan, WPK systematically explores high-speed operator implementations from third-party libraries besides our automatically generated codes and singles out the best implementation per operator for use. Extensive experiments demonstrated that on a Tesla P100 GPU, we can achieve the maximum speedup of 5.40 over cuDNN and 1.63 over TVM on individual convolution operators, and run up to 1.18 times faster than TensorRT for end-to-end model inference.

1 Introduction

Convolutional neural network (CNN) models [1–4] usually have high computational cost subject to batch size, number of weight parameters and image size. Hence, graphics processing units (GPUs) have been playing a central role in CNN model training and inference, owing to its high compute power exposed by massive parallelism. Popular deep learning frameworks such as Caffe [5], TensorFlow [6], Mxnet [7] and PyTorch [8] all provide built-in support for GPUs. However, these frameworks mainly focus on improving programming productivity and training performance. Under such circumstances, a few model-inference optimization works have been proposed. They generally work as follows: (i) taking as input a trained model from the aforementioned deep learning frameworks, and (ii) generating an optimized implementation for deployment in production. Typical works include XLA [9] (applicable to training as well), TVM [10], Glow [11], Tensor Comprehensions [12], nGraph [13], OpenVINO [14], and TensorRT [15].

The architecture of a deep neural network (DNN) can be abstracted as a computational graph with operators as nodes and tensors representing data movement as edges. In practice, computation
within operators often dominates the whole execution, in contrast to data movement between operators. In this case, faster execution of individual operators would lead to prominent acceleration of model inference. Therefore, hardware vendors devote considerable efforts to manually tuning the performance of key primitive functions that are widely used by deep learning applications. These primitives are commonly offered as a collection of libraries, allowing for practitioners to leverage the latest architectural features and refinement in primitive implementations. Existing deep learning frameworks heavily rely on these highly engineered libraries such as MKL-DNN [16] on CPUs and cuDNN [17] on GPUs. Although these libraries are usually very efficient, there may still be significant room for performance improvement. This is because given a specific primitive, manual tuning is usually unable to explore the whole optimization space, thus possibly missing better implementations. Moreover, these libraries do not implement the full set of primitives needed by deep learning models, leaving the implementation and optimization of those unsupported ones to users. As a matter of fact, implementing high-performance novel primitives is essentially challenging even for experts. This motivated the development of domain-specific language (DSL) compilers to lower programming barrier and thereby allow for non-expert users to write high-performance primitives with no need of deep knowledge of hardware and associated parallel programming models. Typical DSL compilers include Halide [18], DLVM [19], Diesel [20], TIRAMISU [21] and Triton [22].

In principle, accelerating primitives intends to optimize the inference at the operator level. However, after examining popular deep learning models, existing works further observed optimization opportunities from patterned subgraphs that allow for fusing consecutive operators to reduce or even eliminate data movement between the operators fused. Note that implementing a fused operator by invoking primitive functions of component operators one after another is actually unable to reduce data movement overhead between operator calls, making operator fusion ineffective at all. Taking GPU as an example, one effective approach is to write one CUDA [23] kernel function for the fused operator and complete the whole computation within only one kernel launch to eliminate the intermediate data movement overhead mentioned above. The benefits gained from this in-placed implementation inspired us to perform global optimizations at the graph level. Typical optimizations include fusing operators, removing redundant operations (e.g. identify and dropout), functionally equivalent subgraph substitution [24] and etc. Similar to writing primitives unsupported by vendor-specific libraries, implementing efficient kernels for fused operators is also challenging to users. One promising approach is to resort to DSL compilers.

Have examined existing works on model inference acceleration, we observed that none of them has ever made attempts on leveraging system-level exploration to identify best-performing operator functions additionally from third-party implementations. In this situation, we propose Woodpecker-DL (WPK), a hardware-aware optimization framework that leverages multifaceted optimizations based on local and global graph optimization, automated searches with genetic algorithm [25] and reinforcement learning (RL) [26], automatic high-quality code generation by a customized DSL compiler, and system-level exploration to exploit third-party superiorities. Our contributions can be summarized from the following two aspects. On one hand, we proposed an automated optimization framework for model inference acceleration by taking advantage of an ensemble of systematic optimizations coming from computational graph, automated searches, DSL compilers and third-party libraries. This framework allows for non-expert users to achieve high-speed model inference with no need of deep understanding of the underlying hardware architectures and parallel programming models. On the other hand, we developed an automated hardware-aware search method based on RL, named RL-search, besides genetic algorithm. These automated searches free users from the tedious and laborious exploration of the vast search spaces exposed by device-specific primitives.

2 Methods

In principle, WPK consists of four components: graph optimization, automated search, runtime engine, and custom operators bound to third-party engines. The graph optimization component takes a graph model as input, then performs functionally equivalent transformations to simplify graph structures, and finally outputs the specification that guides automatic code generation per operator in the optimized graph. The automated search component accepts the specifications exported by the graph optimization component and couples genetic search and RL-search with our customized Halide compiler to generate efficient codes for each operator. Our runtime engine collects the operator functions generated by automated searches, and drives the data flow expressed by the optimized graph.
to complete inference. In addition to our proprietary runtime engine, WPK allows for encapsulating our generated operator functions into custom operators that comply with the standards defined by existing deep learning frameworks (e.g. TensorRT, TensorFlow and PyTorch). Figure 1a shows the architectural overview of WPK.

2.1 Graph optimization

Computational graph optimization has become a standard procedure in accelerating deep neural networks. Most approaches apply pre-defined rules to identify sub-graphs that can be equivalently simplified and substituted. In WPK, we have used the following approaches: constant folding, operator fusion and data layout transformations. Constant folding applies to sub-graphs whose output values can be computed statically beforehand. Operator fusion aims to compress the computation with a sub-graph into one equivalent novel operator in order to reduce the communication overhead between operators in the sub-graph as well as improve hardware usage efficiency due to the increase of compute intensiveness within the novel operator. Data layout transformations aims to identify the better data layouts for the inputs to a given operator in order to get faster execution on the target hardware. It needs to be stressed that for operator fusion and data layout transformations, we must compose the corresponding implementations of those novel operators newly created in the optimization process. In WPK, we employed rule-based optimizations and defined pattern-based specifications to guide the generation of operator functions accordingly.

2.2 Automated Searches

Our automated searches intend to identity most efficient codes per operator according to code-generation specifications tailored for a specific architecture. Instead of merely searching hand-engineered libraries, we choose to take advantage of a customized Halide compiler to generate codes just-in-time under the guidance of our search algorithms. Since Halide can support a wide spectrum of processors including x86/ARM CPUs and GPUs, WPK naturally supports these architectures as well. Nonetheless, our paper will merely investigate optimization techniques on CUDA-enabled GPUs [23].

Halide compiler Halide is a DSL compiler based on the concept of functional programming. A Halide program is actually C++ code written using the functions (Func type), variables (Var type) and other types (e.g. Expr) defined in Halide library. These functions and expression definitions are embedded in C++ syntax by means of operator overloading on the corresponding types. Halide is defined based on the concept of separating algorithm from schedule, where algorithm declares what to compute and schedule represents the decisions about how to map and run the algorithm efficiently on a target device. The following code snippet gives a simple convolution implementation in Halide C++ syntax.

```c++
// Express the algorithm.
```
Buffer<float> in(256, 256);
Buffer<float> filter(3, 3);
RDom r(filter);
Func conv;
conv(x, y) = sum(filter(r.x, r.y) * in(x+r.x-1, y+r.y-1));
// Schedule with tunable parameters x_size and y_size;
Var xi, yi;
conv.gpu_tile(x, y, xi, yi, x_size, y_size);
// Generate codes and execute them on the target.
Target target = get_gpu_target_from_environment();
Buffer<float> out = conv.realize(256, 256, target);

Generating codes  As mentioned above, we employ Halide to generate codes for operator functions. Intuitively, given an algorithm description, we could make attempts to find an optimal schedule by enumerating all possible configurations in the whole schedule space exposed by Halide. However, this approach will incur huge computation and could result in prohibitively long runtimes, thus inapplicable to practical use. In our implementation, we adopted a semi-automatic approach based on schedule templates. This approach pre-defines one or more schedule templates for a given algorithm, then exposes a set of tunable hyper-parameters to let practitioners instantiate, and finally exploits automated search in the tunable parameter space to identify specific parameter values that are capable of directing optimal code generation. For instance, x_size and y_size are tunable parameters in the code snippet shown above. Moreover, due to its confined search spaces, this semi-automatic approach is obviously advantageous to whole-space search approaches in terms of speed. In our implementation, schedule templates are all composed by domain-specific experts, and are fed into Halide at the runtime to generate codes with the assistance of our automated searches.

2.3 Genetic search

Genetic algorithms are a family of meta-heuristic optimization algorithms inspired by the principles of natural selection and genetics. These algorithms mimic evolutionary processes by performing crossover, mutation and selection operations. In practice, they are capable of advancing, with high robustness, to optimal solutions to complicated optimization problems.

Search space  In WPK, genetic search is used to identify an optimal configuration for code generation per operator on the target hardware. A configuration is encoded as a parameterized vector (or chromosome in the parlance of genetics) \( s = \{c_0, c_1, ..., c_{n-1}\} \) of \( n \) elements with each element \( c_i \) (\( 0 \leq i < n \)) corresponding to a numerical parameter (or gene with respect to chromosomes) having a finite range. The full set of all configurations \( \{s\} \) constitute the search space \( S \) of our genetic search. A configuration is hardware-dependent in some sense and is used to instantiate a schedule template.

Implementation  Our implementation follows the typical procedure of genetic algorithms, which generally consists of four steps: (i) Step1 initializes a population \( a \) of \( |a| \) configurations that are randomly generated, (ii) Step2 calculates the fitness value for each configuration in the population, (iii) Step3 performs genetic operations including crossover, mutation and selection, and (iv) Step4 repeats Step2 and Step3 until the convergence condition is met. In Step1, any randomly generated configuration will be verified first in order to meet certain constraints. For instance, the total number of threads in a thread block cannot exceed 1024 on a CUDA-enabled GPU. In this case, we must ensure that the product of all dimension values is positive and \( \leq 1024 \) for a thread block. In Step2, for each individual \( a_i \), we first compile the generated codes just-in-time as per the hardware configuration, then execute them to get the runtime, and finally set the function of runtime, denoted as \( f(a_i) \), as its fitness value.

Step3 first calculates the selection probability \( p(a_i) \) (refer to Equation (1)) for \( a_i \), and sorts the population in decreasing order of selection probability.

\[
p(a_i) = \frac{f(a_i)}{\sum_{i=1}^{|a|} f(a_i)} \quad (1)
\]

Subsequently, we select top \( k \) (\( 1 \leq k \leq |a| \)) elites with the highest probabilities. These elites are always selected and passed to the next generation. In addition to these elites, we will further reproduce some off-springs from individuals with less fitness in order for more exploration. Assuming the
expected next-generation population size is $|a'| (|a'| \geq k)$, we employ a roulette wheel selection approach to randomly select parents for any of the remaining $|a'| - k$ children and crossover to reproduce off-springs. This selection first computes the cumulative probabilities from the selection probabilities of the $m$ ($m \leq |a|$) individuals that will participate in the crossover. In this case, the cumulative probability $P(a_i) (1 \leq i \leq m)$ of the $i$-th individual is calculated by Equation (2).

$$P(a_i) = \sum_{j=1}^{i} p(a_j)$$

(2)

Based on this equation, we used an inverse sampling approach to select candidates. More specifically, after getting $P(a_i)$, we generate a random number $v$, which is uniformly distributed in $[0, 1]$, and compare $v$ with $P(a_i)$ to select individuals. If $P(a_{i-1}) < v \leq P(a_i)$, the $i$-th individual will be selected. In sum, the core idea of our selection is to make more healthy individuals breed more and less healthy ones to breed fewer or even nothing.

Step4 will stop the evolutionary process as long as the convergence condition is reached, i.e. the runtimes of all individuals in the current generation are close enough. Additionally, note that the population size from generation to generation may vary in our implementation.

2.4 Reinforcement learning search

Besides genetic search described in [23], we have developed RL-search, an automated search algorithm based on RL. Given an operator, we model schedule template parameter optimization as an RL problem, and adopt the proximal policy optimization (PPO) [26] approach to predict one action only, i.e. instantiating the schedule template with a concrete parameter configuration. PPO is a new family of policy gradient methods for RL. Unlike standard policy gradient methods [27] performing one gradient update per data sample, PPO enables training with mini-batch updates. In addition, RLLib [28] is used to implement our search algorithm (see Figure [16]).

State space We introduced a feature vector $O$ to represent our observation, where all possible values of $O$ form our state space. For different operators, we could use distinct observation representation. For 2D convolutions that are basically most time-consuming in CNN models [29], the observation $O_{conv}$ is 17-dimensional and defined as

$$O_{conv} = (N, C_{in}, C_{out}, K_h, K_w, H, W, Stride, Padding, T_x, T_y, T_z, Tile_x, Tile_y, Tile_z, Tile_{rz}, \alpha_t)$$

where $N$ is the batch size, $C_{in}$ (and $C_{out}$) is the number of input (and output) channels, $K_h$ (and $K_w$) is the number of rows (and columns) in a filter matrix, $H$ (and $W$) is the image height (and width), $Stride$ is the stride and $Padding$ is the padding mode (i.e. SAME or VALID in our case). $T_x$, $T_y$, and $T_z$ denote the number of CUDA threads in the $x$, $y$ and $z$ coordinate direction of a thread block, respectively, while $Tile_x$, $Tile_y$ and $Tile_z$ are the tile sizes that will be processed by a single CUDA thread in the $x$, $y$ and $z$ coordinate direction, respectively. $Tile_{rz}$ represents the split and unroll size in a reduce domain, $\alpha_t$ ($t \geq 1$) is the runtime moving average of the operator at time step $t$. In our implementation, $\alpha_t$ is empirically calculated as follows:

$$\alpha_t = \alpha_{t-1} \times 0.8 + \beta_t$$

(3)

where $\beta_t$ denotes the runtime of the operator at time step $t$, and $\alpha_0$ is initialized to be zero.

Action space We used a discrete action space and developed a DNN to predict actions from observations. The DNN is composed of four fully-connected (FC) layers (with 512, 1024, 1024 and 512 hidden sizes in order) associated with an activation function $\text{tanh}$, $\text{tanh}$, $\text{selu}$ and $\text{selu}$ functions in order) each, followed by a dropout layer with a keep probability of 15%, and a FC layer with a linear activation. The output of the network is fed into a multinomial distribution to sample actions. The output of the multinomial distribution is used as actions to update the parameter values (e.g. $Tile_{rz}$ in $O_{conv}$) in our state space, where an action updates one parameter at a time and multiple rounds of action predictions are required in order to perform the same number of parameter updates.
As mentioned above, our RL agent employs the PPO algorithm, whose computation requires computing an estimator of the policy gradient and plugging the estimator into a stochastic gradient ascent algorithm. We adopted the generalized advantage estimator proposed in [26], defining the estimator $\tilde{A}_t$ of advantage function at time step $t$ as

$$\tilde{A}_t = \delta_t + (\gamma \mu)\delta_{t+1} + \cdots + (\gamma \mu)^{T-t+1} \delta_{T-1}$$

where

$$\delta_t = r_t + \gamma V(s_{t+1}) - V(s_t)$$

and $V(s_t)$ is the score returned by a learned state-value function at time step $t$.

Our loss function $L_t(\theta)$ combines the policy surrogate loss $L_t^{\text{clip}}(\theta)$ with a value function loss $L_t^{VF}(\theta)$, and is further augmented with the addition of an entropy bonus to ensure sufficient exploration, as done in [26]. Therefore, we defined the final loss function as

$$L_t(\theta) = \tilde{E}_k[L_t^{\text{clip}}(\theta) - c_1 L_t^{VF}(\theta) + c_2 S(\pi_\theta)(s_t)]$$

where $c_1$ and $c_2$ are coefficients and are set to 0.15 and 20 in our implementation, respectively. $S$ denotes an entropy bonus and $L_t^{VF}$ the square-error loss $V_\theta(s_t) - V_t^{\text{target}}$. Please refer to RLlib [23] for more implementation details.

### 2.5 Integration with TensorRT

TensorRT is a state-of-the-art inference platform on CUDA-enabled GPUs. One special feature of TensorRT is that it allows for users to customize operators via plugins. Based on this feature, we can conveniently integrate WPK-generated codes with TensorRT. (see Figure 2a). As mentioned in [1], WPK performs system-level exploration to further use high-performance third-party implementations per operator additionally. This means that we not only take advantage of efficient codes generated by our DSL compiler, but also fully exploit the implementations from third-party libraries (e.g. cuDNN or TensorRT) that outperform ours. Taking TensorRT as an example, for some operator, if its TensorRT implementation is superior to ours, we will use this TensorRT implementation in our optimized inference plan. This type of system-level exploration significantly distinguishes WPK from all existing compiler frameworks including XLA, TVM and nGraph.

**Figure 2**: (a) diagram illustrating the integration of WPK into TensorRT, and (b) speedups of WPK and TVM relative to cuDNN.

**Network** We adopted a model-free method which obtains the runtime of the operator by directly interacting with the target hardware. In our implementation, the reward $r_t$ at time step $t$ is defined as:

$$r_t = \alpha_{t-1} - \min\{\beta_t, 2\alpha_{t-1}\}$$

The rationale behind $r_t$ is that if $\beta_t$ is less than the historical moving average $\alpha_{t-1}$, we return a positive reward calculated from the runtime difference, and otherwise, a negative reward. If $\beta_t$ is considerably large, say $\beta_t > 2\alpha_{t-1}$ in our implementation, we will clamp its value to $2\alpha_{t-1}$, resulting in the reward of $-\alpha_{t-1}$.

As mentioned above, our RL agent employs the PPO algorithm, whose computation requires computing an estimator of the policy gradient and plugging the estimator into a stochastic gradient ascent algorithm. We adopted the generalized advantage estimator proposed in [26], defining the estimator $\tilde{A}_t$ of advantage function at time step $t$ as

$$\tilde{A}_t = \delta_t + (\gamma \mu)\delta_{t+1} + \cdots + (\gamma \mu)^{T-t+1} \delta_{T-1}$$

where

$$\delta_t = r_t + \gamma V(s_{t+1}) - V(s_t)$$

and $V(s_t)$ is the score returned by a learned state-value function at time step $t$.

Our loss function $L_t(\theta)$ combines the policy surrogate loss $L_t^{\text{clip}}(\theta)$ with a value function loss $L_t^{VF}(\theta)$, and is further augmented with the addition of an entropy bonus to ensure sufficient exploration, as done in [26]. Therefore, we defined the final loss function as

$$L_t(\theta) = \tilde{E}_k[L_t^{\text{clip}}(\theta) - c_1 L_t^{VF}(\theta) + c_2 S(\pi_\theta)(s_t)]$$

where $c_1$ and $c_2$ are coefficients and are set to 0.15 and 20 in our implementation, respectively. $S$ denotes an entropy bonus and $L_t^{VF}$ the square-error loss $V_\theta(s_t) - V_t^{\text{target}}$. Please refer to RLlib [23] for more implementation details.

**2.5 Integration with TensorRT**

TensorRT is a state-of-the-art inference platform on CUDA-enabled GPUs. One special feature of TensorRT is that it allows for users to customize operators via plugins. Based on this feature, we can conveniently integrate WPK-generated codes with TensorRT. (see Figure 2a). As mentioned in [1], WPK performs system-level exploration to further use high-performance third-party implementations per operator additionally. This means that we not only take advantage of efficient codes generated by our DSL compiler, but also fully exploit the implementations from third-party libraries (e.g. cuDNN or TensorRT) that outperform ours. Taking TensorRT as an example, for some operator, if its TensorRT implementation is superior to ours, we will use this TensorRT implementation in our optimized inference plan. This type of system-level exploration significantly distinguishes WPK from all existing compiler frameworks including XLA, TVM and nGraph.
Figure 3: (a) performance comparison among three search methods, and (b) genetic search speed on individual convolution operators.

3 Experiments

We used ResNet-18 \cite{ResNet} to evaluate WPK and its counterparts on a Tesla P100 GPU. ResNet-18 is an image classification model trained with Caffe and accepts inputs with NHWC data layout format. In terms of end-to-end inference, given an operator, we used both genetic search and RL-search to identify optimal code generation configurations and single out the best for use. WPK was integrated with TensorRT as described in \cite{25} for inference performance assessment. Additionally, the input shape has $N = 1$, $C = 3$, $H = 224$ and $W = 244$.

3.1 Individual convolution operators

Firstly, we compared WPK to TVM and cuDNN using the individual convolution operators extracted from ResNet-18. In this test, we categorize convolution operators into distinct groups under the following criterion: two convolution operators are considered computationally identical if they have the same input/output shape, filter matrix size, stride and padding. In this test, we directly used the well-optimized ResNet-18 model built-in TVM for fair comparison. By using the performance of cuDNN as the baseline, Figure 2b shows the speedups of WPK and TVM relative to cuDNN. From the figure, we can observe that WPK and TVM run 2.54× and 2.06× faster than cuDNN on average, as well as 5.40× (on convolution c5) and 3.89× (on convolution c11) at the maximum, respectively. Interestingly, neither WPK nor TVM is always superior to cuDNN. In comparison with TVM, WPK outperforms the former by a factor of 1.24 on average and 1.63 at the maximum. However, we did not compare with TensorRT, because the overall runtime of TensorRT cannot be broken down as per operator, due to the more complex graph optimizations applied to the model by itself.

3.2 RL search performance

Secondly, we compared RL-search with genetic search. RL-search failed to perform better than genetic search on individual convolutions of ResNet-18. Furthermore, the former was observed to have much higher randomness than the latter, in terms of search time and best operator speed. Nonetheless, we fortunately found that the former yielded superior performance on some convolution operators in another CNN model used in production. Table 1 gives the information of the convolutions on which RL-search outperforms genetic search, while Figure 3a shows the speedups of random search, genetic search and RL-search, relative to cuDNN \cite{17}. From the figure, both RL-search and genetic search consistently outperform random search. In particular, RL-search performs better than genetic search for each case, with speedups ranging from 1.09 to 1.66.

3.3 Genetic search speed

Thirdly, we evaluated the search speed of our genetic search on individual operators of ResNet-18 (see Figure 3b). In our implementation, we employed multi-threading to accelerate code compilation as
Table 1: Convolutions on which RL-search outperforms genetic search.

| Name  | H    | W    | C_{in} | C_{out} | K_h × K_w | Stride |
|-------|------|------|--------|---------|-----------|--------|
| conv1a| 112  | 96   | 3      | 64      | 3 × 3     | 1      |
| conv1b| 110  | 94   | 64     | 96      | 3 × 3     | 2      |
| conv2 | 54   | 46   | 96     | 128     | 3 × 3     | 2      |
| conv3 | 26   | 22   | 128    | 256     | 3 × 3     | 2      |
| conv4 | 12   | 10   | 256    | 512     | 3 × 3     | 1      |

well as generation, and introduced a caching mechanism to reuse search results. The average search time is 8.9 minutes, with the minimum and maximum times of 1.4 and 27.9 minutes respectively. These times are reasonably acceptable in our production, since the search process is normally conducted offline. In addition, our caching mechanism can further expedite the search process for a family of models that are composed from the same backbone model (e.g. ResNet).

3.4 End-to-end inference

Finally, we used ResNet-18 to assess the end-to-end inference speed of WPK, TVM and TensorRT. As mentioned in [25] WPK can exploit system-level exploration to take advantage of TensorRT operator implementations that run faster than the codes generated by our own compiler. Performance evaluation revealed that WPK is neck-by-neck with TVM, while TensorRT performs worst. WPK runs $1.18 \times$ faster than TensorRT. Note that WPK was observed to have selected some TensorRT operators that outperform WPK-generated codes. Excluding these TensorRT operators incorporated only results in very marginal performance loss of 2%.

4 Related Work

Compiler-based inference acceleration frameworks have been becoming more popular recently. XLA [9] is the first work in this research direction, which was initially specialized to TensorFlow models and currently can be applied to optimize PyTorch models as well. XLA lowers operators into primitive linear algebra operations and calls into backend-specific libraries for execution on different backends. TVM [10] is an end-to-end compiler framework with Halide at the core, which first optimizes a computational graph, then converts the optimized graph into intermediate representations and finally compiles to executable codes on a specific target device. This work was further enhanced by AutoTVM [31] to enable automatic optimization of tensor operators. Compared to TVM, WPK provides broader capability by enabling system-level exploration as described before, i.e. we aim to achieve fastest speed by singling out operator implementations not only from ours but also from third-party libraries. NeoCPU [32] is built upon TVM and aims to optimize CNN inference on CPUs by taking advantage of wide SIMD instructions. nGraph [13] adopts a similar workflow to TVM, but was further extended to support encrypted data with homomorphic encryption [33]. Some other compiling frameworks (e.g. Tensor Comprehensions [12], and Glow [11]) were also developed.

5 Conclusion

WPK is part of Woodpecker that is an efficient compiler framework for heterogeneous computing based on software-hardware co-design, and targets to accelerate deep learning applications by taking advantage of multiple joint optimizations from graph optimization, automated searches, compiling technique and system-level exploration. In this paper, we have presented two automated search methods based on genetic and RL algorithms, respectively. In comparison with cuDNN, TVM and TensorRT, our performance evaluation demonstrated the superiority of WPK in terms of both accelerating individual convolution operators and end-to-end inference. More specifically, on a Tesla P100 GPU, we can achieve the maximum speedup of 5.40 over cuDNN and 1.63 over TVM in terms of individual convolutions, and run up to $1.18 \times$ faster than TensorRT with respect to end-to-end model inference. Although we have merely investigated the capability of WPK in accelerating inference in this paper, WPK can actually be applied to accelerate training and we plan to conduct this research as part of our future work. In the end, we would like to note that optimizing device placement of operators in a multi-device environment [34, 35] is also an interesting research direction.
References

[1] A. Krizhevsky, I. Sutskever, and G. E. Hinton, “Imagenet classification with deep convolutional neural networks,” in Advances in neural information processing systems, pp. 1097–1105, 2012.

[2] S. Ren, K. He, R. Girshick, and J. Sun, “Faster r-cnn: Towards real-time object detection with region proposal networks,” in Advances in neural information processing systems, pp. 91–99, 2015.

[3] J. Lin, C. Gan, and S. Han, “Tsm: Temporal shift module for efficient video understanding,” in International Conference on Computer Vision, 2019.

[4] K. He, G. Gkioxari, P. Dollár, and R. Girshick, “Mask r-cnn,” in Proceedings of the IEEE international conference on computer vision, pp. 2961–2969, 2017.

[5] Y. Jia, E. Shelhamer, J. Donahue, S. Karayev, J. Long, R. Girshick, S. Guadarrama, and T. Darrell, “Caffe: Convolutional architecture for fast feature embedding,” in Proceedings of the 22nd ACM international conference on Multimedia, pp. 675–678, ACM, 2014.

[6] M. Abadi, P. Barham, J. Chen, Z. Chen, A. Davis, J. Dean, M. Devin, S. Ghemawat, G. Irving, M. Isard, et al., “Tensorflow: A system for large-scale machine learning,” in 12th USENIX Symposium on Operating Systems Design and Implementation, pp. 265–283, 2016.

[7] T. Chen, M. Li, Y. Li, M. Lin, N. Wang, M. Wang, T. Xiao, B. Xu, C. Zhang, and Z. Zhang, “Mxnet: A flexible and efficient machine learning library for heterogeneous distributed systems,” in Neural Information Processing Systems Workshop on Machine Learning Systems, 2015.

[8] A. Paszke, S. Gross, F. Massa, A. Lerer, J. Bradbury, G. Chanan, T. Killeen, Z. Lin, N. Gimelshein, L. Antiga, et al., “Pytorch: An imperative style, high-performance deep learning library,” in Advances in Neural Information Processing Systems, pp. 8024–8035, 2019.

[9] G. inc., “Xla is a compiler-based linear algebra execution engine,” 2019. https://www.tensorflow.org/xla.

[10] T. Chen, T. Moreau, Z. Jiang, L. Zheng, E. Yan, H. Shen, M. Cowan, L. Wang, Y. Hu, L. Ceze, et al., “Tvm: An automated end-to-end optimizing compiler for deep learning,” in 13th USENIX Symposium on Operating Systems Design and Implementation, pp. 578–594, 2018.

[11] N. Rotem, J. Fix, S. Abdulrasool, G. Catron, S. Deng, R. Dzhabarov, N. Gibson, J. Hegeman, M. Lele, R. Levenstein, et al., “Glow: Graph lowering compiler techniques for neural networks,” arXiv:1805.00907, 2018.

[12] N. Vasilache, O. Zinenko, T. Theodoridis, P. Goyal, Z. DeVito, W. S. Moses, S. Verdoollaenge, A. Adams, and A. Cohen, “Tensor comprehensions: Framework-agnostic high-performance machine learning abstractions,” arXiv:1802.04730, 2018.

[13] S. Cyphers, A. K. Bansal, A. Bhiwandiwalla, J. Bobba, M. Brookhart, A. Chakraborty, W. Constable, C. Convey, L. Cook, O. Kanawi, et al., “Intel ngraph: An intermediate representation, compiler, and executor for deep learning,” in Proceedings of the Conference on Systems and Machine Learning, 2018.

[14] I. inc., “Intel openvino toolkit,” 2019. https://software.intel.com/en-us/openvino-toolkit.

[15] N. inc., “Nvidia tensorrt programmable inference accelerator,” 2019. https://developer.nvidia.com/tensorrt.

[16] I. inc., “Intel® math kernel library for deep learning networks,” 2019. https://software.intel.com/en-us/articles/intel-mkl-dnn-part-1-library-overview-and-installation.

[17] S. Chetlur, C. Woolley, P. Vandermerch, J. Cohen, J. Tran, B. Catanzaro, and E. Shelhamer, “cudnn: Efficient primitives for deep learning,” arXiv:1410.0759, 2014.

[18] J. Ragan-Kelley, C. Barnes, A. Adams, S. Paris, F. Durand, and S. Amarasinghe, “Halide: a language and compiler for optimizing parallelism, locality, and recomputation in image processing pipelines,” in Acm Sigplan Notices, vol. 48, pp. 519–530, ACM, 2013.

[19] R. Wei, L. Schwartz, and V. Adve, “Dlvm: A modern compiler infrastructure for deep learning systems,” in 31st Conference on Neural Information Processing Systems, 2017.

[20] V. Elango, N. Rubin, M. Ravishankar, H. Sandanagobalane, and V. Grover, “Diesel: Dsl for linear algebra and neural net computations on gpus,” in Proceedings of the 2nd ACM SIGPLAN International Workshop on Machine Learning and Programming Languages, pp. 42–51, ACM, 2018.
R. Baghdadi, J. Ray, M. B. Romdhane, E. Del Sozzo, A. Akkas, Y. Zhang, P. Suriana, S. Kamil, and S. Amarasinge, “Tiramisu: A polyhedral compiler for expressing fast and portable code,” in *Proceedings of the 2019 IEEE/ACM International Symposium on Code Generation and Optimization*, pp. 193–205, IEEE Press, 2019.

P. Tillet, H. Kung, and D. Cox, “Triton: an intermediate language and compiler for tiled neural network computations,” in *Proceedings of the 3rd ACM SIGPLAN International Workshop on Machine Learning and Programming Languages*, pp. 10–19, ACM, 2019.

E. Lindholm, J. Nickolls, S. Oberman, and J. Montrym, “Nvidia tesla: A unified graphics and computing architecture,” *IEEE micro*, vol. 28, no. 2, pp. 39–55, 2008.

Z. Jia, O. Padon, J. Thomas, T. Warszawski, M. Zaharia, and A. Aiken, “Taso: Optimizing deep learning computation with automatic generation of graph substitutions,” in *The 27th ACM Symposium on Operating Systems Principles*, ACM, 2019.

J. H. Holland *et al.*, *Adaptation in natural and artificial systems: an introductory analysis with applications to biology, control, and artificial intelligence*. MIT press, 1992.

J. Schulman, F. Wolski, P. Dhariwal, A. Radford, and O. Klimov, “Proximal policy optimization algorithms,” *arXiv:1707.06347*, 2017.

V. Mnih, A. P. Badia, M. Mirza, A. Graves, T. Lillicrap, T. Harley, D. Silver, and K. Kavukcuoglu, “Asynchronous methods for deep reinforcement learning,” in *International conference on machine learning*, pp. 1928–1937, 2016.

E. Liang, R. Liaw, P. Moritz, R. Nishihara, R. Fox, K. Goldberg, J. E. Gonzalez, M. I. Jordan, and I. Stoica, “Rllib: Abstractions for distributed reinforcement learning,” in *Proceedings of the 35th International Conference on Machine Learning*, 2017.

X. Li, G. Zhang, H. H. Huang, Z. Wang, and W. Zheng, “Performance analysis of gpu-based convolutional neural networks,” in *2016 45th International Conference on Parallel Processing*, pp. 67–76, IEEE, 2016.

K. He, X. Zhang, S. Ren, and J. Sun, “Deep residual learning for image recognition,” in *Proceedings of the IEEE conference on computer vision and pattern recognition*, pp. 770–778, 2016.

T. Chen, L. Zheng, E. Yan, Z. Jiang, T. Moreau, L. Ceze, C. Guestrin, and A. Krishnamurthy, “Learning to optimize tensor programs,” in *Advances in Neural Information Processing Systems*, pp. 3389–3400, 2018.

Y. Liu, Y. Wang, R. Yu, M. Li, V. Sharma, and Y. Wang, “Optimizing cnn model inference on cpus,” in *2019 USENIX Annual Technical Conference*, pp. 1025–1040, 2019.

F. Boemer, Y. Lao, R. Cammarota, and C. Wierzyński, “ngraph-he: a graph compiler for deep learning on homomorphically encrypted data,” in *Proceedings of the 16th ACM International Conference on Computing Frontiers*, pp. 3–13, ACM, 2019.

A. Mirhoseini, A. Goldie, H. Pham, B. Steiner, Q. V. Le, and J. Dean, “A hierarchical model for device placement,” 2018.

D. Narayanan, A. Harlap, A. Panishayee, V. Seshadri, N. R. Devanur, G. R. Ganger, P. B. Gibbons, and M. Zaharia, “Pipedream: Generalized pipeline parallelism for dnn training,” in *27th ACM Symposium on Operating Systems Principles*, 2019.