Future Large-Scale Memristive Device Crossbar Arrays:Limits Imposed by
Sneak-Path Currents on Read Operations

Yansong Gao\textsuperscript{a,*}, Omid Kavehei\textsuperscript{b}, Damith C. Ranasinghe\textsuperscript{c}, Said F. Al-Sarawi\textsuperscript{a}, Derek Abbott\textsuperscript{a}

\textsuperscript{a}School of Electrical and Electronic Engineering, The University of Adelaide, Adelaide, SA, Australia 5005
\textsuperscript{b}School of Electrical and Computer Engineering, Royal Melbourne Institute of Technology, Victoria 3001, Australia
\textsuperscript{c}School of Computer Science, The University of Adelaide, SA 5005, Australia

Abstract

Passive crossbar arrays based upon memristive devices, at crosspoints, hold great promise for the future high-density and non-volatile memories. The most significant challenge facing memristive device based crossbars today is the problem of sneak-path currents. In this paper, we investigate a memristive device with intrinsic rectification behavior to suppress the sneak-path currents in crossbar arrays. The device model is implemented in Verilog-A language and is simulated to match device characteristics readily available in the literature. Then, we systematically evaluate the read operation performance of large-scale crossbar arrays utilizing our proposed model in terms of read margin and power consumption while considering different crossbar sizes, interconnect resistance values, HRS/LRS (High Resistance State/Low Resistance State) values, rectification ratio and different read-schemes. The outcomes of this study are understanding the trade-offs among read margin, power consumption, read-schemes and most importantly providing a guideline for circuit designers to improve the performance of a memory based crossbar structure. In addition, read operation performance comparison of the intrinsic rectifying memristive device model with other memristive device models are studied.

Keywords: Memristive device, Memristor, Crossbar array memory, Verilog-A, Sneak-path current, RRAM, Read margin, Power consumption.

1. Introduction

The two-terminal memristive device based crossbar array is a promising candidate for future non-volatile memories attributing to its low-power and small-area overhead, 3D integration, fast switching speed, compatibility with standard CMOS technology and simple fabrication process\cite{1,2}. However, ultra-high density integration of memristive devices in crossbar arrays still faces a number of challenges such as magnitude of sneak-path (leakage) currents, relatively high variation of device operation, and poor reproducibility. The most significant of these challenges that must be overcome to realize large-scale crossbar array memory is that of sneak-path currents, which demands reduction in leakage currents through unselected devices while reading the memory array.

To circumvent sneak-path currents in emerging crossbar memory arrays, several approaches have been proposed. One of those techniques uses two back-to-back bipolar memristive elements shown in Fig.1(a). This approach resonates with the immense success of CMOS technology in which either the pull-up (composed of p-type transistor) or the pull-down (composed of n-type transistor) network is active at a given time; such a complementary configuration greatly limits the short-circuit currents through the operating circuit. For memristive circuits a similar configuration, known as complementary resistive switch (CRS) is utilized\cite{3,4,5}, however, this configuration relies on the polarity difference between the two back-to-back connected memristive elements. Therefore, at a given time, only one of the devices is either in the LRS (Low Resistance State) or HRS (High Resistance State). This indicates that the total resistance of this configuration in equilibrium is always at the highest value, hence, limiting sneak-path currents through unselected cells within the crossbar array. Despite these features, this approach is shown to be not very successful given the relatively large footprint and significant hurdles in a successful miniaturization\cite{6}. In addition, a reading operation on a CRS is destructive and the multilevel bits offered by a memristive device can no longer be exploited\cite{6}.

Alternatively, the other two approaches using a selector device to reduce the sneak-path currents are: one-transistor-one-memristive device (1T1M), shown in Fig.1(b); and one-diode-one-memristive device (1D1M) structures\cite{7,6}, shown in Fig.1(c). Using a transistor as the selecting device at each crosspoint raises the footprint of each cell and consequently its three-dimensional stack-
The memristive device with intrinsic rectifying behavior. In particular, we: (i) provide a Verilog-A behavioral model of a memristive device with intrinsic rectifying behavior based on published fabricated device parameters; (ii) evaluate read operation performance of large-scale arrays while considering different interconnect resistance values, HRS/LRS values, rectification ratios and different read-schemes utilizing our proposed model; (iii) demonstrate the effectiveness of this special type of memristive device as an approach to reduce sneak path effects in a crossbar structure; (iv) demonstrate the advantages of the memristive device with intrinsic-rectifying behavior by comparing with a linear memristive device (without rectification capability) and 1S1R structure, shown in Fig. 1(e) and (c), respectively.

The rest of the paper is organized as follows: in Section 2 we describe read margin and read-schemes for a crossbar array. The memristive device behavioral model along with Verilog-A code are provided; in Section 3 we evaluate our memristive device model within a passive crossbar array and analyze the read operation performance of crossbar arrays, specifically in terms of read margin and power consumption; read operation comparison with other memristive devices and discussions are presented in Section 4 followed by conclusions in Section 5.

2. Crossbar Array and Device Model

2.1. Crossbar Array

A crossbar array is comprised of two layers of parallel electrodes that are crossed perpendicularly, which act as word-lines or bit-lines. At each crosspoint, an element is formed, which can be programmed to the LRS or HRS to represent either a logic ‘1’ or ‘0’ when proper voltages are applied to word-lines and bit-lines. Unfortunately, as stated in Section 1, this promising memory architecture severely suffers from sneak-path currents, hence the need for appropriate approaches to suppress them. Because the sneak-path currents aggravate read/write operation performance of crossbar array and hence, limit the maximum size of a crossbar. The source of sneak-path current is shown in Fig. 2. As discussed earlier, one possible approach to suppress sneak-path currents and hence improve read/write operation performance is through using a memristive device with intrinsic rectifying behavior.

To simplify the read operation with large crossbars, in the following simulations a single sense resistor is used to sense the state of the memristive device instead of using sense amplifier. To obtain the best read margin, the sense resistor value, $R_{sense}$, is calculated based on [10]:

$$R_{sense} = \sqrt{R_{ON}R_{OFF}}.$$

The read margin, RM, is defined as:

$$RM = \frac{V_{out}(LRS) - V_{out}(HRS)}{V_{WS}}.$$
where $V_{WS}$ is the read voltage applied to the selected word-line shown in Fig. 2. While $V_{out}(LRS)$ and $V_{out}(HRS)$ are the voltages measured in $R_{sense}$ resistor when the target-cell is in LRS and HRS, respectively. In the literature, there are a number of read-schemes for crossbars that includes V/2, V/3 and F-F (Floating-Floating), where $V$ is the rail-to-rail (maximum) potential difference. The voltage bias requirements for these read-schemes are shown in Fig. 2.

Due to the influence from sneak-path currents and total interconnect resistance, the output voltage swing is dependent on the stored data and the position of the cell to be read within the array. Additionally, taking the interconnect resistance into account, the read margin will deteriorate further if the target-cell is located in the furthest corner from the word/bit-line voltage sources—in case of Fig. 2 this would be the top right corner cell. In this paper, we only evaluate operation performance under this worst-case position.

2.2. Memristive Device Model with Intrinsic Rectifying Behavior

The memristive device model with intrinsic rectifying behavior is investigated in this subsection. Besides the intrinsic rectifying behavior, the memristive device also shows well-defined threshold voltage and abrupt resistance switching. In the following, we use a simplified mathematical model for this special memristive device to match the rectifying and threshold voltage behaviors that are empirically reported in [12, 13, 14]. Subsequently we provide a Verilog-A based model.

A memristive device has a state variable $\omega \subset [0, 1]$ corresponding to the value of its memristance $R_m$. The $R_{m}$ is a function of $\omega$, which follows

$$R_m = \begin{cases} R_{OFF}(R_{ON}/R_{OFF})^\omega, & (v \geq 0) \\ R_{OFF}, & (v < 0) \end{cases}$$

where $v$ is the applied voltage. According to Eq. 3 $R_m = R_{OFF}$ when $\omega = 0$, while $R_m$ is in $R_{ON}$ state if $\omega = 1$.

The memristive device is observed with a well-defined threshold voltage. On one hand, if the absolute biased voltage applied to the memristive device is smaller than the threshold voltage, the state variable stays unchanged or changes minimally. On the other hand, once the bias voltage is larger than the threshold voltage, the state variable changes abruptly. Here we use symmetric threshold voltages, which can be different in practical memristive device implementations. The dynamic switching behavior of the memristive device is defined as:

$$\frac{dw}{dt} = \begin{cases} \alpha(v - V_{TH}), & (v \geq V_{TH}) \\ \alpha(v + V_{TH}), & (v \leq -V_{TH}) \\ \beta v, & \text{otherwise}, \end{cases}$$

where $V_{TH}$ is the threshold voltage. The $\alpha$ and $\beta$ coefficients are programming rates. Here, we set $\beta = 0$ assuming that the smaller voltage does not alter the state variable, and hence, does not perturb the memristance during read operation [17].

The developed behavioral model is created in Verilog-A language is given in Appendix. Simulated I-V characteristic curve with intrinsic rectifying behavior is shown in Fig. 3.
3. Results and Analyses

In this section, the aforementioned memristive device model is placed into crossbar array to study the read margin and power consumption under different crossbar sizes, read-schemes, interconnect resistance values, rectification ratios (assuming a fixed $R_{OFF}/R_{ON}$ ratio for the defined memristive device model) and $R_{ON}$ value when the rectification ratio is constant.

Simulations were carried out using Cadence tools, then data is extracted for post-processing in MATLAB. In these simulations the interconnect resistance is taken into consideration to produce a more realistic assessment of the crossbar array. The default parameters used in following simulations are listed in the Table 1. Here, we mainly focus on the reading rather than the writing operation performance. For the following simulation we assume no change to the device memristance when a reading voltage in the order of 1 V is applied to the word/bit-lines when assuming a threshold voltage of 1.5 V.

Table 1: List of parameters used in the memristive device and array simulations.

| Parameter                | Value                |
|--------------------------|----------------------|
| High resistance state $R_{OFF}$ | $5 \times 10^8 \Omega$ |
| Low resistance state $R_{ON}$    | $5 \times 10^5 \Omega$ |
| Sense resistor $R_{sense}$       | $1.58 \times 10^7 \Omega$ |
| Interconnect resistance $r_{wire}$ | $5 \Omega$ |
| Threshold voltage $V_{TH}$       | 1.5 V                |
| Ratio of $R_{OFF}/R_{ON}$        | $1 \times 10^3$      |
| $\alpha$                    | $2.5 \times 10^8 (V s)^{-1}$ |
| $\beta$                     | $0 (V s)^{-1}$      |

3.1. Read-Schemes and Crossbar Size

The read margin and power consumption under different crossbar sizes using different read-schemes are studied based on the device model developed earlier. The size of the crossbar is from 4 $\times$ 4 up to 128 $\times$ 128. The considered read-schemes are V/2, V/3 and F-F.

Read operation performance results are shown in Figs 4 & 5. Fig. 4 illustrates that the V/3 read-scheme has the best read margin, while the F-F read-scheme has the worst read margin when the crossbar size increases to 8 $\times$ 8. The significant drop in read margin using the F-F read-scheme can be attributed to the exponential increase in the number of sneak current paths inside the crossbar array, despite the use of the intrinsic rectifying behavior. Note that the F-F read-scheme has the largest read margin when the crossbar size is small (here it is 4 $\times$ 4). In terms of the other two read-schemes, there is a slight decrease in the read margin for large array sizes.

Power consumption is presented in Fig. 5. The power consumed when the target memristive device stays either in the HRS or LRS is measured separately. It can be seen that the different power consumptions in the HRS and LRS is very small (almost the same), except for the F-F read-scheme when the crossbar size is small (smaller than 8 $\times$ 8 in our study). In overall, the F-F read-scheme consumes less power, whereas the V/2 read-scheme consumes the largest power. In particular power consumption when using F-F read-scheme is only a very small fraction of other two read-schemes, especially when using a large crossbar array size.

Based on these simulations the V/3 read-scheme has the best performance considering the trade-off between read margin and power consumption for large-scale crossbar arrays.

3.2. Interconnect Resistance

The influence of interconnect resistance on read operation performance is shown in Fig. 6. As the interconnect resistance increases, the read margin decreases, while the power consumption reduces—in the other words, power consumption benefits from the increase in interconnect resistance. The read margin drops by 50% as the inter-
connect resistance rises from 5 Ω to 320 Ω. In order to achieve a high read margin performance, the interconnect resistance should be as small as possible despite the fact that a larger interconnect resistance can result in a slight improvement in the overall power consumption.

Sources of read margin deterioration caused by interconnect resistance are: (i) voltage drops across the selected word/bit-lines; (ii) the unbalanced rising and falling voltage potential on unselected word/bit-lines, resulting in increasing many leakage current paths flowing into the selected bit-line.

![Figure 6: Read margin and power consumption influence as a function of interconnect resistance. The crossbar size is fixed at 64 × 64. The V/2 read-scheme is used.](image)

3.3. Different Memristive Device Parameters

3.3.1. Resistance of ON/OFF

The Fig. 7 shows the influence of the ON/OFF resistance on read operation. To ensure the ratio of HRS/LRS is kept constant during the simulation, the \( R_{OFF} \) value is changed accordingly. As a result, the sensing resistor, \( R_{sense} \) also needs to be changed to meet the requirement set by Eq. 1.

The read margin improves if the \( R_{ON} \) resistance increases. The overall power consumption also improves as the \( R_{ON} \) resistance increases. It appears that increasing \( R_{ON} \) resistance produces improved performance with respect to both read margin and power consumption. However, it should be noted that there are still trade-offs among read margin, power consumption and read speed during read operation. For fast access times into memristive device based crossbar memory, higher resistance of the cross-point cell always aggravates access speed.

3.3.2. Rectification Ratio Dependence

In this part, the \( R_{ON} \) resistance remains unchanged, while the rectification ratio (here, it is also the ratio of HRS/LRS according to the mathematical model) changes to different values. The read margin and power consumption as functions of rectification ratios are shown in Figs. 8 & 9 respectively.

![Figure 7: Read margin and power consumption as a function of \( R_{ON} \) resistance. The crossbar size is fixed at 64 × 64. Rectification ratio is a constant value, \( 10^3 \). The V/2 read-scheme is used.](image)

![Figure 8: Read margin as a function of different rectification ratios under different read-schemes. The crossbar size is fixed at 64 × 64. \( R_{ON} \) is fixed at \( 5 \times 10^5 \) Ω.](image)

It can be seen from Fig. 7 that read margin improves as the rectification ratio increases, especially for the the F-F read-scheme, which verifies that sneak currents can be suppressed significantly by memristive device with intrinsic rectifying behavior.

Power consumption almost stays constant for V/2 and V/3 read-schemes as the rectification ratio increases. While the power consumption with respect to F-F read-scheme reduces exponentially with increasing the rectification ratio.

4. Comparison and Discussion

We have presented a systematic evaluations and analyses on the read operation performance of a crossbar array in Section 3. In this section, we firstly compare our proposed model with one linear memristive device model. Secondly, we further compare the device model with the ISIM structure. Intuitively one might suppose that increasing nonlinearity of the selector device in ISIM structure is going to always improve the read operation performance of
the 1S1M structure. However, the following simulations demonstrate this is not the case.

![Simulated I-V curve](image)

**Figure 9:** Power consumption as a function of rectification ratios under different read-schemes. The crossbar size is fixed at 64×64. \(R_{\text{ON}}\) is fixed at \(5 \times 10^5 \Omega\).

### 4.1. Comparison with the linear Memristive Device

The I-V characteristic of linear memristive device model (with linear resistance behavior in LRS State) is shown in Fig. [10](image), which has same parameter settings in Fig. [3](image) except the rectifying behavior. We conduct the read margin and power consumption performance evaluation by using the linear memristive device model. The results are shown in Figs. [11](image) & [12](image). It can be seen that both of the read margin and power consumption performance deteriorate in comparison with the results in Figs. [4](image) & [5](image). For read margin, the V/3 read-scheme still has the best performance and the F-F illustrates the worst read margin that is similar to results obtained in Section [3](image). Without self rectifying behavior, the sneak-path currents cannot be effectively suppressed, resulting in severely decreased read margin. Especially for the F-F read-scheme, the read margin is too small for practical application, even when considering small array size. Unlike the read margin performance, if the memristive device with self rectifying behavior employed does not see obvious deterioration as the size increases up to \(128 \times 128\), the read margin employing linear memristive device suffers from a significant degradation as the crossbar size increases.

The V/3 read-scheme has a worse power consumption than the V/2 read-scheme, which does not follow the results presented in Section [3](image) where the V/3 read-scheme has better power performance than the V/2 read-scheme. In addition, the other difference between the results in Section [3](image) and the results in Fig. [12](image) is that the power consumption increases faster as the size of crossbar increases when using a linear memristive device.

![Current vs Voltage](image)

**Figure 10:** Simulated I-V curve of the behavioral model without intrinsic rectifying characteristic. Simulation settings is same to Fig. [3](image). Inset figure shows the same I-V curve but the y-axis is on a logarithmic scale.

### 4.2. Comparison with the 1S1M Structure

In this part, we compare the read operation performance of the model presented in this paper with 1S1M structure. For 1S1M structure, the memory cell is made up of a selector and a memristive device. The selector has the characteristic of allowing both polarities to conduct beyond a threshold. The mathematical model is defined as [10]:

\[
I_{\text{sel}} = \gamma \times \sinh(\alpha \times V), \quad \text{where} \quad \alpha = k \times p, \quad \text{(5)}
\]

the \(\gamma\) is a conductance parameter and \(k\) determines the nonlinearity of the selector. Here, the \(p = 18.4\) is set to the same value presented in [11](image). To model the 1S1R structure, we connect one selector with one resistor acting as a memory cell. Here, \(R_{\text{ON}}\) and \(R_{\text{OFF}}\) are set to \(5 \times 10^5\) and \(5 \times 10^8\), respectively, the rest of the parameters are
the same as given in Table 1. During these simulations, the value of $\gamma$ is kept fixed, while $k$ was changed to determine the nonlinearity of the selector, which influences the read operation performance. Results are shown in Figs. 13 & 14. It can be seen that there exists an optimum nonlinearity for the selector to achieve the best read margin, in contrast to the results when the rectification ratio is increase, which always results in an increased read margin as discussed in Section 3.3.2. So using the 1S1M structure, there is an issue that the nonlinearity should be cautiously considered along with the forward current $I_{ON}$ to acquire the maximum read margin. In addition, the power consumption always increases regarding for the 1S1M structure when the $k$ increases, which is also different from the power consumption results reported in Section 3.3.2 that which is not affected by the increase of rectification ratio, moreover, the F-F read-scheme does benefit from the rise of rectification ratio.

5. Conclusion

In this paper, the read operations of the crossbar array are studied with the proposed memristive behavioral model. Based on extensive simulation results, we verify that rectification behavior significantly improve the read margin. In addition, we provide circuit design guidelines that the V/3 read-scheme shows the best read margin and demonstrated that the F-F read-scheme presents the worst read margin as the crossbar size increases. However, the F-F read-scheme has the best power consumption performance due to a very small fraction of power consumption in comparison with the power consumed by the other two read-schemes (V/2 and V/3 read-schemes). Moreover, the interconnect resistance influence on read performance is also studied, which suggests that the resistance should be kept as small as enough to achieve better read margin. Furthermore, read operation dependence on memristive device parameters is investigated. Based on the numerical results, higher HRS/LRS resistance—if the read speed has met with the requirement—and higher rectification ratio are desirable. Finally, we demonstrate the advantages of pursuing this intrinsic rectifying behavior within memristive device based on two comparisons in Section 4. From comparison in Section 4.1 we confirm that, as expected, the rectification does suppress sneak-path currents in crossbar memory leading to an improved figure-of-merit for the read operation. In terms of comparison in Section 4.2, we show that increasing the nonlinearity of selector in 1S1M structure does not always lead to better read operation performance. In contrast, it can deteriorates the read margin and power consumption figure-of-merits without careful selection of this parameter. So the memristive device with intrinsic rectifying behavior is a significant improvement over alternative schemes for a crosspoint cell in the crossbar array memory.
6. Appendix

module memristor (p,n);
  inout p; //positive terminal
  inout n; //negative terminal
  //electrical p, n;
  //parameter definition and default values
  parameter real rof=5E8;
  parameter real ron=5E8;
  parameter real Vth=1.5;
  parameter real winit=1;
  parameter real r=5E5;
  parameter real r=5E8;
  parameter real beta=0;
  real dwdt;
  real w_normal_last;
  real w_normal;
  real R;
  real first_iteration;
  real stop;
  //////////////////////////////////////////////////
  analog begin
    if (first_iteration==0) begin
      w_normal_last=winit;
      //if this is the first iteration , start with winit;
    end
    if (V(p,n) >= Vth) begin
      dwdt=alpha*(V(p,n)-Vth);
    end else if (V(p,n) <= -Vth) begin
      dwdt=alpha*(V(p,n)+Vth);
    end else begin
      dwdt=beta*V(p,n);
    end
    w_normal=idot(dwdt, w_normal_last, stop);
    if ((w_normal>1)&& absolutep(V(p,n)>0)) begin
      w_normal_last=1;
      stop=1;
    end else if ((w_normal<0)&& absolutep(V(p,n)<0)) begin
      w_normal_last=0;
      stop=1;
    end else if (stop!=0) begin
      w_normal_last=w_normal;
      stop=0;
    end
    if (V(p,n)< 0) begin
      R=rof;
    end else if (V(p,n)>= 0) begin
      R=rof*(pow(ron/rof, w_normal));
    end
    I(p,n)=+ V(p,n)/R;
    first_iteration=1;
  end
endmodule

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