Analytical model and simulation-based analysis of a work function engineered triple metal tunnel field-effect transistor device showing excellent device performance

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Abstract
In this study, the authors propose a work function engineered (WFE) triple metal (TM) tunnel field-effect transistor (TFET) device, which exhibits lower subthreshold slope (SS) and better on to off current ratio in comparison with conventional double gate TFET and dual metal TFET device. An analytical model is formulated to study the performance of the proposed device. A simulation-based study of these TFET devices has been carried out with the help of 2D TCAD (Technology Computer Aided Design) Sentaurus device simulator for different channel length values in order to validate our proposed mathematical model. The source side n+ pocket in the proposed triple metal (TM) TFET device enhances tunnelling probability thus increasing on current and off current is controlled by another n-pocket near drain side. Significantly lower subthreshold slope (less than 10 mV/decade), high transconductance (in the order of 10 S/μm), low energy-delay product (24.601 fJ-ns/μm) obtained for TM WFE TFET makes this device more suitable for digital logic and RF (Radio Frequency) application.

1 | INTRODUCTION

Tunnel field-effect transistor (TFET) has become a promising and potential device for use in low power application. TFET may act as a possible alternative of metal oxide semiconductor field effect transistor in very large scale integration circuit because of its excellent immunity against short channel effects, inherent capacity of handling low operating voltage, lower leakage current and lower subthreshold swing. However, the problem lies with lower on-state current and ambipolar behaviour of the TFET device which affects its performance. Ambipolarity means the conduction of current in TFET for both positive and negative gate bias. In a conventional TFET, the positive and negative gate voltages reduce the tunnelling barrier width at source/channel and drain/channel interfaces, resulting in increase of current in both the cases. Since the inherent ambipolarity of TFET is undesirable for CMOS logical circuit design, care should be taken to suppress the ambipolar current at negative gate bias. Several techniques like applying low bandgap materials [1], high-k gate oxide [2], dopant engineering, implementation of multi-material gate TFET structures [3], vertical TFETs [4, 5] have been utilized over the last few years to enhance on current (Ion). Furthermore, different methods such as employment of high band gap material on the drain side or decreasing the doping concentration of drain region help to mitigate the problem of ambipolar behaviour. But these techniques increase the series resistance of the device, hence deteriorating on-state current. Therefore, a novel technique needs to be evolved which can improve the on current and suppress the ambipolar behaviour of the device. In this study, we propose a work function engineered (WFE) triple metal (TM) gate TFET structure which uses single gate material with different work function values for tunnel gate, control gate and auxiliary gate as shown in Figure 1. Moreover, source and drain region of the device are formed by applying charge plasma concept with suitable work function so that the problem of random dopant fluctuation [6–8] and expensive thermal budget [9, 10] can be ignored. The choice of work function values for three gate metals and dielectrics of oxide are made in such a way that better on current, lower off current (Ion) and hence better on current to off current ratio are achieved, which matches better
with the standard requirements of International Technology Roadmap for Semiconductor (ITRS) [11]. Now the major hindrance lies in complex and difficult manufacturing process of triple work function for gate electrode. In this regard, high-dose nitrogen implantation technique can be helpful to achieve proper integration of triple work functionality of gate material. Molybdenum is used as gate material [12] in our proposed device. To further improve on current, narrow band gap, heterostructures or strained materials can be used. Moreover, Radio frequency (RF) performance of the device has also been investigated and due to its low energy-delay product (EDP), the device can be used for low power RF application. The performance of the proposed structure can easily be realized using commercial 2D numerical device simulator. In our case, the simulation of the device has been carried out in 2D Technology Computer Aided Design (TCAD) Sentaurus. But to get detailed understanding of the device performance in terms of its physical behaviour, an accurate analytical model is needed, which would also be helpful for circuit-level design. The authors in [3] used similar approach of modelling for a TM double gate TFET device in which a parabolic potential distribution is assumed in the channel region. This approximation does not predict correct sinusoids at the semiconductor/oxide interface, thus not giving a good estimate of the device’s characteristics length. Hence in this study, we choose evanescent mode of modelling which correctly predicts the device’s behaviour in the entire channel region. Moreover, the device performance is also compared with a WFE dual metal TFET device and a conventional TFET device as shown in Figure 1 in order to show how much the performance has been improved. For ease of reference, WFE dual metal TFET device and WFE TM TFET device are renamed as TFET I and TFET II, respectively, in remaining part of this study.

The potential model of the device is derived from Poisson’s equation considering the influences of both mobile charge term and depletion charge term. The expression for band to band tunneling (BTBT) generation rates are then obtained using Kane and Kleyshy model. By integrating the BTBT generation rate over the entire tunneling region yields drain current. This mathematical model also predicts the impacts of auxiliary gate work function and control gate work function on surface potential and drain current.

The rest of the study has been organized as follows. Section 2 presents schematic view of the proposed device along with important simulation parameters. A mathematical model is developed in Section 3. Device performance analysis has been discussed with the help of simulation graphs and data in Section 4. Finally, Section 5 concludes the study.

### 2 | DEVICE STRUCTURE AND ITS FABRICATION

In this study, WFE dual metal TFET device and WFE TM TFET device are renamed as TFET I and TFET II, respectively. The cross-sectional views of conventional TFET, TFET I and TFET II considered for our study, are shown in Figure 1. In TFET II, high-κ dielectric Al₂O₃ is used as oxide under M1, M2 and comparatively low-κ dielectric SiO₂ is used as oxide under M3. The method of using WFE technique together with a suitable gate oxide material in TFET can control the density of carriers in the channel region either making it more n-type or p-type. The use of proper work function value of M3 together with SiO₂ as gate oxide in TFET II prevents to reduce the tunnelling barrier width at drain/channel interface, hence

**Figure 1** Cross-sectional view of (a) Conventional TFET, (b) proposed device TFET I, (c) proposed device TFET II; TFET, Tunnel field-effect transistor; TFET, Tunnel field-effect transistor.
suppressing ambipolarity. The suppression of ambipolarity can be explained from the energy band diagram presented in Figure 2. The energy band diagram of the proposed device under zero bias condition indicates its inherent characteristic of having larger barrier width near drain side, which prevents reduction of tunnelling barrier width on application of negative gate bias. All essential device parameters used for simulation are given in Table 1. For our investigation, we consider \( L = 30 \text{ nm} \) and \( L = 50 \text{ nm} \). If \( L = 50 \text{ nm} \) is considered, then total length distribution in R2 and R3 of TFET I would be 10 and 40 nm, and length distribution in R2, R3 and R4 of TFET II would be 10, 30 and 10 nm. The depletion regions present near source/channel junction and near drain/channel junction are also taken into account as found in Figure 1. In next section we derive a mathematical model considering these depletion regions as well. The work function of all metals starting from source to drain region in our proposed TM TFET device are chosen to follow this order \( \phi_S = \phi_{m1} < \phi_{m2} < \phi_{m3} < \phi_{D} \), where \( \phi \) is the work function of metal. The lower work function for the tunnel gate in case of TM TFET device can reduce the depletion width at source/channel interface causing more band bending and lowering tunnel barrier width. Hence, on current is improved. On the other hand, use of higher work function in auxiliary gate (as compared to work function value of metal used in drain for charge plasma technique) helps to lower off current or ambipolar current. This TM gate structure with different work functions thus helps to improve switching characteristics and \( I_{on}/I_{off} \) ratio more than the method discussed in [13]. Moreover, an Al\(_{2}\)O\(_3\) layer can be built on Si film using atomic layer deposition (ALD) technique which reduces the chance of trap charges interfering at the Si/Al\(_{2}\)O\(_3\) interface. This technique of oxide deposition provides excellent integrity and fine controlability on atomic scale thickness [14]. ALD is technique of depositing thin layer of material (oxide or metal) with thickness varying from micrometre to nanometre ranges, on the surface of the semiconductor. The steps that are followed in a single cycle of ALD technique are:

- First precursor is exposed in the reactor chamber to form an initial layer on the semiconductor substrate
- Evacuation of the excess first precursor and the by-products
- The second precursor is exposed
- Removal of the excess second precursor and by-products
- The process is continued until the required film thickness is achieved

The source region is formed by depositing a suitable source metal (Platinum) with work function 5.93 eV over Al\(_{2}\)O\(_3\) layer, so that \( p^+ \) charge carriers can be induced in this region. The drain region is formed by depositing a suitable drain metal (Hafnium) with work function 3.9 eV over Al\(_{2}\)O\(_3\) layer, so that \( n^- \) charge carriers can be induced in this region. The thickness of the oxide layer is kept much bigger than 1 nm in order to avoid any gate to channel tunnelling.

3 | MODEL DEVELOPMENT

For accurate modelling of channel potential, we consider four region (R1, R2, R3, R4) in TFET I and five region (R1, R2, R3, R4, R5) in TFET II including source and drain depletion region for both TFET devices as demonstrated in Figure 1. The region R1 lies under tunnel gate M1 which witnesses the generation of electrons by the process of band-to-band tunnelling. The 2D electrostatic potential in channel region can be solved from 2D Poisson’s equation which includes both generation of electrons by the process of band bending and lowing tunnel barrier width. Hence, on current is improved. On the other hand, use of higher work function in auxiliary gate (as compared to work function value of metal used in drain for charge plasma technique) helps to lower off current or ambipolar current. This TM gate structure with different work functions thus helps to improve switching characteristics and \( I_{on}/I_{off} \) ratio more than the method discussed in [13]. Moreover, an Al\(_{2}\)O\(_3\) layer can be built on Si film using atomic layer deposition (ALD) technique which reduces the chance of trap charges interfering at the Si/Al\(_{2}\)O\(_3\) interface. This technique of oxide deposition provides excellent integrity and fine controlability on atomic scale thickness [14]. ALD is technique of depositing thin layer of material (oxide or metal) with thickness varying from micrometre to nanometre ranges, on the surface of the semiconductor. The steps that are followed in a single cycle of ALD technique are:

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Abbreviation: TFET, tunnel field-effect transistor.

\[ C_{oxi} \left[ V_g - V_{FBi} - \psi_{Li}(t_0) \right] = \xi_s \frac{\partial \psi_{Li}(y)}{\partial y} |_{y=t_0} \]  

(5)

where, \( t_0 = t_s/2 \), \( V_{FBi} \) is the flat band voltage, \( C_{oxi} \) is oxide capacitance per unit area in respective region. The initial solution of \( \psi_{Li}(y) \) as obtained following the method reported in [13] is given by the following:

\[ \psi_{Li}(y) = \psi_{oi} = V + V_i \ln(B_i/2\delta) \]  

(6)

Using the initial guess of \( \psi_{Li}(y) \) in (1), the final solution of \( \psi_{Li}(y) \) is formulated as the following:

\[ \psi_{Li}(y) = a_1 \frac{y^2}{2} + \frac{a_2 t_s^2}{B_i} \ln \left( \sec \left( \frac{B_i}{t_0} y \right) \right) + \psi_{oi} \]  

(7)

where,

\[ a_1 = \frac{q}{\epsilon_{si}} N \]  

(8)

\[ a_2 = \frac{q}{2\delta \epsilon_{si}} n_i B_i \]  

(9)

\[ \delta = q n_i t_s^2 / (4\epsilon_{si} V_i) \]  

(10)

\[ V = \frac{V_{di}}{L} \]  

(11)

\( B_i \) can be evaluated by combining (4), (5) and (6) as expressed below:

\[ \frac{2\epsilon_{si} V_i B_i}{t_0} \tan B_i + C_{oxi} V_i \ln \left( \frac{B_i^2}{2\delta} \sec^2(B_i) \right) = C_{oxi} \left( V_g - V_{FBi} - V \right) \]  

(12)

Now, 2D electrostatic potential \( \psi_{2D}(y) \) can be solved from Laplace equation (using separation of variables method) given by the following:

\[ \frac{\partial^2 \psi_{2D}(x, y)}{\partial x^2} + \frac{\partial^2 \psi_{2D}(x, y)}{\partial y^2} = 0 \]  

(13)

The solution of \( \psi_{2D}(x, y) \) is expressed as the following:

\[ \psi_{2D}(x, y) = \left( a_i e^{\frac{\lambda_i}{t_0} (x-x_{-1})} + b_i e^{\frac{-\lambda_i}{t_0} (x-x_{-1})} \right) \cos \left( \frac{\lambda_i}{t_0} y \right) \]  

(14)

where, \( \lambda_i \) is Eigen value and derived from the following:

\[ \lambda_i \tan \lambda_i = \frac{C_{oxi} t_0}{\epsilon_{si}} \]  

(15)

For TM TFET device, the unknown coefficients \( a_i \) and \( b_i \) are calculated done with the help of the following boundary conditions:

\[ \psi_{2D1} \bigg|_{x=x_0} = V_S - \psi_{01}(y) \]  

(16)

\[ \psi_{2D1} \bigg|_{x=x_1} = V_{R1} - \psi_{01}(y) \]  

(17)

\[ \psi_{2D2} \bigg|_{x=x_1} = V_{R1} - \psi_{02}(y) \]  

(18)

\[ \psi_{2D2} \bigg|_{x=x_2} = V_{R2} - \psi_{02}(y) \]  

(19)

\[ \psi_{2D3} \bigg|_{x=x_2} = V_{R2} - \psi_{03}(y) \]  

(20)

\[ \psi_{2D3} \bigg|_{x=x_3} = V_{R3} - \psi_{03}(y) \]  

(21)

\[ \psi_{2D4} \bigg|_{x=x_3} = V_{R3} - \psi_{04}(y) \]  

(22)

\[ \psi_{2D4} \bigg|_{x=x_4} = V_{R4} - \psi_{04}(y) \]  

(23)
\[
\psi_{aDS} \big|_{x=x_l} = V_R - \psi_{t0}(y)
\]  
(24)

\[
\psi_{aDS} \big|_{x=x_s} = V_D - \psi_{t0}(y)
\]  
(25)

where, \(V_S\) and \(V_D\) are found by \(V_S = -\frac{K}{q} \ln \left(\frac{N}{n_i}\right)\) and \(V_D = V_{ds} + \frac{K}{q} \ln \left(\frac{N}{n_i}\right)\), \(N_S\) and \(N_D\) are the source and drain doping concentration, \(K\) is Boltzmann constant. \(V_R\) represents surface potential at the junction of any two regions and can be solved by assuming continuous electric flux and surface potential at the interface of two regions.

The tunnelling length can be defined by the length of tunnelling which starts from the source end and ends where the surface potential in region R2 falls by \(E_G/2\), where \(E_G\) is band gap energy. By this definition, tunnelling length \(L_T\) can be expressed by the following:

\[
L_T = L_d \cosh^{-1} \left[ \frac{\psi_{source} - V_{gs} + V_{FB2}}{\psi_{source} - E_G/2 - V_{gs} + V_{FB2}} \right]
\]

\[
-L_d \cosh^{-1} \left[ \frac{\psi_{source} - E_G/2 - V_{gs} + V_{FB2}}{\psi_{source} - V_{gs} + V_{FB2}} \right]
\]  
(26)

where, \(L_d\) is the Debye length. The average electric field \(E_{avg}\) at lower \(V_{gs}\) is estimated by the following:

\[
E_{avg} = \frac{\psi_{source}(x_1, t_0) - V_S}{L_1}
\]  
(27)

and at higher \(V_{gs}\)

\[
E_{avg} = \frac{\psi_{source}(x_1, t_0) - V_S}{L_T}
\]  
(28)

Now substituting \(E_{avg}\) into Kane and Kleysh’s model for BTBT current [15], the equation for current density can be established as the following:

\[
I_D = A \times L_T \times \left( \frac{E_{avg}}{E_0} \right)^p \times \exp \left( -\frac{B}{E_{avg}} \right)
\]  
(29)

where, \(A\) and \(B\) are the tunnelling parameters whose default values are \(4 \times 10^{14} \text{ V/cm}^3\) and \(2 \times 10^7 \text{ V/cm}\), respectively, as used in simulation [15], \(P = 2.5\) for phonon-assisted tunnelling process. In this work, we focus on phonon-assisted tunnelling process, because Silicon is an indirect band gap semiconductor. Now if we ignore band gap narrowing effects, then the factors \(A\) and \(B\) can be expressed by [16].

**Figure 3** Comparison of transfer characteristics curve of conventional TFET, TFET I and TFET II having \(L = 50\) nm at \(V_{ds} = 0.5\) V and \(V_{ds} = 1\) V; TFET, tunnel field-effect transistor

**Figure 4** Comparison of transfer characteristics curve of TFET I and TFET II having \(L = 30\) nm at \(V_{ds} = 0.5\) V (marked in black colour) and \(V_{ds} = 1\) V (marked in red colour); TFET, tunnel field-effect transistor

**Figure 5** The calibration of transfer characteristics curve obtained from our model w.r.t. [2, 18].

**Figure 6** Drain characteristic curve of TFET I and TFET II for \(L = 50\) nm at \(V_{gs} = 0.5\) V (marked in blue colour) and \(V_{gs} = 1\) V (marked in black colour)
The transverse acoustic phonon and the transverse optical phonon are the two main contributions of phonon to the tunnelling current. Here, in our study, we consider the transverse optical phonon since the default parameters used in [16] are calibrated with this process.

**Formulation of** $C_{gs}$, $C_{gs}$, and $C_{gd}$

The parasitic capacitances associated with terminal charges of our proposed TFET device can be modelled by following Ward-Dutton method which is used to effectuate the separation of charges into a source charge ($Q_s$) and drain charge ($Q_d$) based on quasi-static condition [17]. The terminal charges $Q_s$ and $Q_d$ are defined by the following:

$$Q_s = W \int_0^L \left(1 - \frac{x}{L}\right) Q_i(x) dx \quad (35)$$

$$Q_d = W \int_0^L \frac{x}{L} Q_i(x) dx \quad (36)$$

where, $W$ represents the net effective width of the layer on which the external biases are applied, $Q_i$ is the inversion charge density which varies along the channel length. The inversion charge density $Q_i(x)$ is simply defined by the following:

$$Q_i(x) = \frac{V_{gs} - V_{FB} - \psi_i(x, t_0)}{C_{oxi}} \quad (37)$$

where, $\psi_i(x, t_0)$ is the position dependent surface potential in respective region.

The total charge on the gate terminal is the following:

$$Q_g = -(Q_s + Q_d) \quad (38)$$

The parasitic capacitances between any two external terminals are then obtained from the following:

$$C_{gs} = -\frac{dQ_g}{dV_s} \quad (39)$$

$$C_{gd} = -\frac{dQ_g}{dV_d} \quad (40)$$
\[ C_{gg} = \frac{dQ_g}{dV_g} \]  \hspace{1cm} (41) 

where, \( V_g \), \( V_s \) and \( V_d \) are bias applied at gate, source and drain terminals.

4 | RESULTS AND DISCUSSION

In this section, the performance of the proposed TFET device is analysed with the help of modelled data and TCAD simulation results. In 2D simulation, some important physics models such as concentration dependent model and electric field dependent mobility model, SRH and Auger recombination model, bandgap narrowing model and non-local band-to-band tunnelling models are utilized. Non-local band-to-band tunnelling model is used to include the effect of tunnelling process. As device channel thickness considered in our case is 10 nm, quantum mechanical effects have not been included in this work.

The transfer characteristics curves obtained for all the devices as shown in Figure 1 are compared at different bias condition and presented in Figure 3. The similar curves are also obtained considering relatively shorter device length (\( L = 30 \, \text{nm} \)) as displayed in Figure 4.

As observed from Figure 3, the simulated drain current value of conventional TFET having \( L = 50 \, \text{nm} \) is found to be \( 6.92 \times 10^{-11} \, \text{Ampere} \) at \( V_{ds} = 1 \, \text{V} \) and \( V_{gs} = 0.5 \, \text{V} \) which is in consistent with the reported data in \([2, 18]\) (also shown in Figure 5), hence the simulation is calibrated. The simulated \( I_{on} \) of TFET I and TFET II device are improved by approximately 30 times and 4.3 \times 10^3 times, respectively, compared with normal Si TFET at \( V_{gs} = V_{ds} = 0.5 \, \text{V} \). At \( V_{gs} = V_{ds} = 1 \, \text{V} \), the improvement in \( I_{on} \) is found to be approximately 850 times and 14 times, respectively, for TFET II and TFET I device.

The overall improvement in subthreshold slope (SS) as noticed from Figures 3 and 4 is due to having shorter electron tunnelling distance under M1 in both TFET I and TFET II device.

![Figure 9](image_url)  
**FIGURE 9** \( I_{on} \) variation of proposed devices with \( L = 30 \, \text{nm} \) at different work function values of M1 and specific bias condition \( V_{gs} = 1 \, \text{V} \), \( V_{ds} = 0.5 \, \text{V} \); TFET, tunnel field-effect transistor

![Figure 8](image_url)  
**FIGURE 8** Comparison of transfer characteristics curve of 30 nm TFET I and 30 nm TFET II at fixed \( V_{ds} = 0.5 \, \text{V} \) and different work function values of gate M1 (SS for TFET I and TFET II are found to be 20 mV/dec and 10 mV/dec for all work function values of M1); TFET, tunnel field-effect transistor; SS, subthreshold slope

![Figure 10](image_url)  
**FIGURE 10** Transconductance curve of (a) TFET I, (b) TFET II and (c) conventional TFET device with \( L = 50 \, \text{nm} \) at \( V_{ds} = 1 \, \text{V} \); TFET, tunnel field-effect transistor
from modelled data. Lower DIBL values achieved for TFET II device confirms its better device controllability over the gate. Furthermore, the DI BL values for different $L$ as listed in Table 2 indicate that DIBL can be improved if we consider higher $L$.

The effects of work function engineering of M1 gate in TFET I and TFET II devices are carefully examined in this section which determines the optimization of the device performance. Figure 8 exhibits transfer characteristics curves of TFET I and TFET II for different work function values of M1. The variation of $I_{on}$ with respect to work function values are also plotted in Figure 9.

It is found from Figure 9 that $I_{on}$ values for TFET II decrease abruptly when work function of M1 ($\Phi_{M1}$) exceeds 3.9 eV. But for TFET I, $I_{on}$ values decrease slowly. When $\Phi_{M1}$ is varied from 3.7 to 4.2 eV, the value of $\Phi_{M2}$ and $\Phi_{M3}$ are kept fixed at 4.25 and 4.5 eV, respectively, for device TFET II. It is also observed from Figure 8 that variation of $\Phi_{M1}$ and $\Phi_{M2}$ does not influence SS to vary for both TFET I and TFET II devices. The reduction of $\Phi_{M1}$, the lateral tunnelling distance decreases and thus $I_{on}$ increases.

The transconductance values extracted from modelled $I_C$, $V_{gs}$ curve for TFET I and TFET II for $V_{ds} = 1$ Vis displayed in Table 2. It is also noticed from Figure 10 that peak transconductance for device TFET I and TFET II is occurred at $V_{gs} = 0.4$ V and $V_{gs} = 0.3$ V (with $g_m$ values are $2.87 \times 10^{-6}$ S/μm and $1.85 \times 10^{-7}$ S/μm, respectively) whereas, for conventional TFET, it happens at $V_{gs} = 0.8$ V and at comparatively low value ($6.79 \times 10^{-9}$ S/μm). The improved peak transconductance is attributed to proper work function engineering of M1 gate in the proposed devices. Moreover, the total gate capacitance ($C_{gg}$) along with gate to source capacitance ($C_{gs}$) and gate to drain capacitance ($C_{gd}$) for all three devices are examined at some fixed bias condition (i.e. $V_{ds} = V_{gs} = 0.5$ V) and tabulated in Table 3.

The $C_{gg}$ values obtained from model actually gives the summation of $C_{gs}$ and $C_{gd}$. It is found that at $V_{ds} = V_{gs} = 0.5$ V, $C_{gg}$ is lowest in TFET I ($3.504 \times 10^{-15}$F/μm) which indicates highest cut off frequency for TFET I. Moreover, a device with high cut off frequency ($f_T$) is desired to be used for RF application. In this study, the parameters $f_T$ and $f_A$ (the gain BW product at dc gain of 10) as defined by (23) and (24) are calculated for TFET I and TFET II.

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

### TABLE 4

| Parameters | TFET I | TFET II | Conventional TFET |
|------------|--------|---------|-------------------|
| $C_{gg}$   | $7.3504 \times 10^{-15}$ (F/μm) | $1.753 \times 10^{-14}$ (F/μm) | $1.56 \times 10^{-15}$ (F/μm) |
| $C_{gs}$   | $3.7056 \times 10^{-11}$ (F/μm) | $5.845 \times 10^{-15}$ (F/μm) | $7.76 \times 10^{-16}$ (F/μm) |
| $C_{gd}$   | $3.7056 \times 10^{-11}$ (F/μm) | $5.845 \times 10^{-15}$ (F/μm) | $7.76 \times 10^{-16}$ (F/μm) |
| $g_m$      | $4.15 \times 10^{-5}$ (S/μm) | $4.26 \times 10^{-7}$ (S/μm) | $6.79 \times 10^{-9}$ (S/μm) |

Abbreviation: TFET, tunnel field-effect transistor.

### TABLE 3

A list of numerical values of parasitic capacitances and transconductance ($g_m$) extracted from analytical model of 50 nm long TFET I, TFET II and conventional TFET device at $V_{ds} = V_{gs} = 0.5$ V
\[ f_A = \frac{g_m}{2\pi 10C_{gd}} \]  

(43)

Due to improved \(g_m\) and low value of \(C_{gd}\), better \(f_T\) and \(f_A\) values are achieved for TFET II at \(V_{gs} = V_{ds} = 0.5\) V. For TFET I, TFET II and conventional TFET, the values of \(f_T\) and \(f_A\) are given by 0.36 and 7.24 GHz, 1.39 and 0.28 GHz, 0.69 and 0.14 MHz, respectively.

The EDP of TFET I and TFET II device are also investigated which is defined by the product of intrinsic switching energy (\(C_{gs}V_{DD}^2\)) and switching delay (\(C_{gs}V_{DD}/I_{on}\)).

Table 4 shows the EDP, intrinsic switching energy (\(E_{in}\)) and the switching delay (\(t_{sw}\)) values for TFET I and TFET II at \(V_{gs} = V_{ds} = 0.5\) V.

The EDP value found for device TFET II is low because of its higher \(I_{on}\) and lower \(C_{gs}\). Thus, lower EDP value obtained for TFET II makes it suitable for low power RF application.

5 | CONCLUSION

In this study, performance of a dual metal TFET device and a TM TFET device (with different channel length values) is analysed based on mathematical modelling and result of numerical simulation. TM TFET device having optimized metal work function values exhibit better dc performance at low-supply voltage. With the help of calibrated simulation, the device performance has also been compared with conventional TFET. Improvement in device performance has been achieved by application of gate work function engineering technique. TFET I and TFET II with \(L = 50\) nm yields approximately 30 times and \(4.5 \times 10^4\) times improved drain current, respectively; at \(V_{gs} = V_{ds} = 0.5\) V, and very small average SS (less than 10 mV/decade) in comparison with conventional TFET device. Moreover, better \(I_{on}/I_{off}\) (in order of \(10^{14}\)) is obtained in TFET II device at \(V_{gs} = V_{ds} = 0.5\) V. High \(f_T\) of 1.39 GHz, high peak \(g_m\) of 4.26 \(\times 10^{-7}\) S/\(\mu\)m, low EDP of 24.601 fJ/ns/\(\mu\)m achieved for TFET II device at \(V_{gs} = V_{ds} = 0.5\) V makes this device suitable for any low-power digital, analogue or RF application.

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