Architecting Optically-Controlled Phase Change Memory

Aditya Narayan∗, Yvain Thonnart†, Pascal Vivet†, Ayse Coskun∗ and Ajay Joshi∗

∗Boston University, Boston, MA 02215, USA; Email: {adityan, acoskun, joshi}@bu.edu
†Univ. Grenoble Alpes, CEA, List, Grenoble, France; Email: {yvain.thonnart, pascal.vivet}@cea.fr

Abstract—Phase Change Memory (PCM) is an attractive candidate for main memory as it offers non-volatility and zero leakage power, while providing higher cell densities, longer data retention time, and higher capacity scaling compared to DRAM. In PCM, data is stored in the crystalline or amorphous state of the phase change material. The typical electrically-controlled PCM (EPCM), however, suffers from longer write latency and higher write energy compared to DRAM and limited multi-level cell (MLC) capacities. These challenges limit the performance of data-intensive applications running on computing systems with EPCMs.

Recently, researchers demonstrated optically-controlled PCM (OPCM) cells, with support for 5 bits/cell in contrast to 2 bits/cell in EPCM. These OPCM cells can be accessed directly with optical signals that are multiplexed in high-bandwidth-density silicon-photonic links. The higher MLC capacity in OPCM and the direct cell access using optical signals enable an increased read/write throughput and lower energy per access than EPCM. However, due to the direct cell access using optical signals, OPCM systems cannot be designed using conventional memory architecture. We need a complete redesign of the memory architecture that is tailored to the properties of OPCM technology.

This paper presents the design of a unified network and main memory system called COSMOS that combines OPCM and silicon-photonic links to achieve high memory throughput. COSMOS is composed of a hierarchical multi-banked OPCM array with novel read and write access protocols. COSMOS uses an Electrical-Optical-Electrical (E-O-E) control unit to map standard DRAM read/write commands (sent in electrical domain) from the memory controller on to optical signals that access the OPCM cells. Our evaluation of a 2.5D-integrated system containing a processor and COSMOS demonstrates 2.14× average speedup across graph and HPC workloads compared to an EPCM system. COSMOS consumes 3.8× lower read energy-per-bit and 5.97× lower write energy-per-bit compared to EPCM. COSMOS is the first non-volatile memory that provides comparable performance and energy consumption as DDR4 in addition to increased bit density, higher area efficiency and improved scalability.

I. INTRODUCTION

Today’s data-driven applications that use graph processing [31], [53], [56], [79], machine learning [16], [30], [91], or privacy-preserving paradigms [4], [20], [82] demand memory sizes on the order of hundreds of GBs and bandwidths on the order of TB/s. The widely-used main memory technology, DRAM, is facing critical technology scaling challenges and fails to meet the increasing bandwidth and capacity demands of these data-driven applications [38], [41], [42], [48], [58], [96]. Phase Change Memory (PCM) is emerging as a class of non-volatile memory (NVM) that is a promising alternative to DRAM [34], [40], [46], [47], [71], [72]. PCMs outperform other NVM candidates owing to their higher reliability, increased bit density, and better write endurance [14], [17], [62], [93]. In PCMs, data is stored in the state of the phase change material, i.e., crystalline (logic 1) or amorphous (logic 0) [64], [94]. A SET operation triggers a transition to crystalline state, and a RESET operation triggers a transition to amorphous state. PCMs also enable multi-level cells (MLC) using the partially crystalline states. Higher MLC capacity enables increased bit density (bits/mm²).

PCM cells are typically controlled electrically (we refer to them as EPCM cells), where different PCM states have distinct resistance values. Main memory systems using EPCM cells are designed using the same microarchitecture and read/write access protocol as DRAM systems [45], [85]. EPCM cells are SET or RESET by passing the corresponding current through the phase change material (via the bitline) to trigger the desired state transition. The state of the EPCM cells is read out by passing a read current and measuring the voltage on the bitline. EPCM systems, however, are limited to 2 bits/cell [14], [18], [62] due to resistance drift over time, have 3−4× higher write latency than DRAM leading to lower performance [6], [45], consume high power due to the need for large on-chip charge pumps [36], [66], [90], and have lower lifetime than DRAM due to faster cell wearout [70].

Recent advances in device research have demonstrated optically-controlled PCM cells (we refer to them as OPCM cells) [19], [27], [28], [78]. OPCM cells exhibit higher MLC capacity than EPCM cells (up to 5 bits/cell [52]). Moreover, high-bandwidth-density silicon-photonic links [84], [87], which are being developed for processor-to-memory communication, can directly access these OPCM cells, thereby yielding higher throughput and lower energy-per-access than EPCM. These two factors make OPCM a more attractive candidate for main memory than EPCM.

Since the optical signals in silicon-photonic links directly access the OPCM cells, the traditional row-buffer based memory microarchitecture and the read/write access protocol encounter critical design challenges when adapted for OPCM. We need a complete redesign of the memory microarchitecture and a novel access protocol that is tailored to the OPCM cell technology. In this paper, we propose a COmbined System of Optical Phase Change Memory and Optical Links, COSMOS, which integrates the OPCM technology and the silicon-photonic link technology, thereby providing seamless high-bandwidth access from the processor to a high-density memory. Figure 1 shows a computing system with COSMOS. COSMOS includes a hierarchical multi-banked
OPCM array, E-O-E control unit, silicon-photonic links, and laser sources. The multi-banked OPCM array uses 3D optical integration to stack multiple banks vertically, with 1 bank/layer. The cells in the OPCM array are directly accessed using silicon-photonic links that carry optical signals, thereby eliminating the need for electrical-optical (E-O) and optical-electrical (O-E) conversion in the OPCM array. These optical signals are generated by an E-O-E control unit that serves as an intermediary between the memory controller (MC) in the processor and the OPCM array. This E-O-E control unit is responsible for mapping the standard DRAM protocol commands sent by the MC onto optical signals, and then sending these optical signals to the OPCM array. The major contributions of our work are as follows:

1) We architect the COSMOS, which consists of a hierarchical multi-banked OPCM array, where the cells are accessed directly using optical signals in silicon-photonic links. The OPCM array design combines wavelength-division-multiplexing (WDM) and mode-division-multiplexing (MDM) properties of optical signals to deliver high memory bandwidth. Moreover, the OPCM array contains only passive optical elements and does not consume power, thus providing cost and efficiency advantages.

2) We propose a novel mechanism for read and write operation of cache lines in COSMOS. A cache line is interleaved across multiple banks in the OPCM array to enable high-throughput access. The write data is encoded in the intensity of optical signals that uniquely address the OPCM cell. The readout of an OPCM cell uses a 3-step operation that measures the attenuation of the optical signal transmitted through the cell, where the attenuation corresponds to a predetermined bit pattern. Since the read operation is destructive, we design an opportunistic writeback operation of the read data to restore the OPCM cell state.

3) We design an E-O-E control unit to interface COSMOS with the processor. This E-O-E control unit receives standard DRAM commands from the processor, and converts them into the OPCM-specific address, data, and control signals that are mapped onto optical signals. These optical signals are then used to read/write data from/to the OPCM array. The responses from the OPCM array are converted by the E-O-E control unit back into standard DRAM protocol commands that are sent to the processor.

Evaluation of a 2.5D system with a multi-core processor and COSMOS demonstrates 2.15× higher write throughput and 2.09× higher read throughput compared to an equivalent system with EPCM. For graph and high performance computing (HPC) workloads, when compared to EPCM, COSMOS has 2.14× better performance, 3.8× lower read energy-per-bit, and 5.97× lower write energy-per-bit. Moreover, COSMOS provides a scalable and non-volatile alternative to DDR4 DRAM systems, with 5.6% higher performance and similar energy consumption for read and write accesses. With DRAM technology undergoing critical scaling challenges, COSMOS presents the first non-volatile main memory system with improved scalability, increased bit density, high area efficiency, and comparable performance and energy consumption as DDR4 DRAM.

II. BACKGROUND

In this section, we discuss the basic operation of an OPCM cell along with its properties, and the silicon-photonic links that enable optical signals to directly access the OPCM cells.

A. OPCM Cell

$Ge_2Sb_2Te_5$ (GST) is a well-known phase change material that exhibits high contrast in electrical property (resistance) and optical property (refractive index) between its two states, in addition to long data retention time and nanoscale size [55], [75], [94]. Thus, GST has been widely used as a storage element in a PCM cell (EPCM and OPCM cells). An OPCM cell consists of only a GST element, and does not use a separate access transistor as an EPCM cell. Figure 2 shows the structure of an OPCM cell, where the GST is integrated on a waveguide [52], [78]. The waveguides are fabricated using a $SiO_2$ layer deposited over a $SiO_2$ layer [51]. The GST layer is covered with a layer of Indium-Tin-Oxide (ITO) to prevent oxidation. The optical signals to read and write the OPCM cell lie in the C band ($1530\text{nm} - 1565\text{nm}$) and L band ($1565\text{nm} - 1625\text{nm}$) of the telecommunication spectrum.

B. Write Operation in OPCM Cells

For write operation, i.e., SET or RESET, the optical signal traversing through the waveguide is coupled to the GST element. The energy of this optical signal heats the GST element and triggers a state transition. For RESET operation, i.e., switching the GST element to an amorphous state (a-GST), an optical pulse of $180pJ$ energy is applied to the GST element for $25\text{ns}$ [52]. For SET operation, i.e., switching the GST element to a fully crystalline state (c-GST), an optical pulse with an energy of $130pJ$ is applied to the GST element for $25\text{ns}$ [52]. The transition of the GST state to a partially crystalline state requires different values of pulse energies ($60 - 130pJ$) applied for varying durations ($50 - 25\text{ns}$) [52].

\textsuperscript{1}COSMOS-based computing system is agnostic of the integration technology. However, 3D-integrated systems raise thermal concerns and 2D systems result in large system footprints and communication overheads.
C. Read Operation in OPCM Cells

The readout mechanism for an OPCM cell uses the high contrast in the refractive indices of a-GST (3.56) and c-GST (6.33) [57]. When an optical signal is passed through the GST element, the higher refractive index of c-GST results in an increased optical absorption by the GST element. Rios et al. [78] demonstrate that c-GST absorbs 79% of the input optical signal and allows transmission of only 21% of the optical signal. In contrast, a-GST transmits 100% of the optical signal. The transmission of partially crystalline states lies between 100% and 21% [78]. An OPCM cell is, therefore, read out by sending a sub-\(ns\) optical pulse through the GST element and measuring the transmitted optical intensity of the output pulse. This transmitted intensity corresponds to a pre-determined bit pattern, thus allowing the readout of the stored data in the GST element.

D. High MLC Capacity of OPCM Cells

In OPCM cells, the read operation uses the refractive index of the GST state to determine the stored value. Unlike the resistance value used in EPCM cells, the refractive index experiences minimal drift over time [52], [78]. This enables designing OPCM cells with multiple stable partially crystalline states with each having unique refractive index. Prior works have demonstrated that it is possible to reliably program an OPCM cell to contain more than 34 unique partially crystalline states [52], [100], which enables an OPCM cell to have an MLC capacity of up to 5 \(bits/cell\). Using a higher capacity MLC enables the read and write operation of a higher number of bits per access, thereby increasing the memory throughput.

E. Silicon-Photonic Links

In a computing system that uses a main memory composed of OPCM cells, optical signals in silicon-photonic links can directly read/write the cells. The silicon-photonic links provide higher bandwidth density at negligible data-dependent power compared to electrical links [9], [10], [43]. In addition, these silicon-photonic links have single-cycle latency, in contrast to electrical links that often take 3 – 4 cycles each for a memory request and a memory response. Moreover, we can multiplex multiple optical signals (up to 32 signals) in a single waveguide, resulting in dense WDM [44]. MicroRing Resonators (MRRs) can modulate these optical signals at data rates up to 12\(Gbps\) [5], [67], [86] giving a peak memory throughput of 384\(Gbps\) per link. Therefore, it is possible to design densely multiplexed silicon-photonic links that can directly access the OPCM cells, further increasing the memory throughput.

III. Motivation

In this section, we first describe the typical EPCM architecture and then explain why such an architectural design is impractical for OPCM arrays. Figure 3 shows the architecture of EPCM [40], [45]. The EPCM array is a hierarchical organization of banks, blocks, and sub-blocks [45]. During read or write operation, the EPCM first receives a row address. The row address decoder reads the appropriate row from the EPCM array into a row buffer. The EPCM next receives the column address, and the column address multiplexer selects the appropriate data block from the row buffer. The bitlines of the selected data block are connected to the write drivers for write operation or to the sense amplifiers for read operation. For write operation, the charge pumps supply the required drive voltage to the write drivers, which corresponds to SET or RESET operation. For read operation, a read current is first passed through the GST element in the EPCM cell through an access transistor [45]. Then, sense amplifiers determine the voltage on the bitline to read out logic 0 or logic 1.

Naively adapting the EPCM architecture for OPCM, by just replacing the EPCM cells with OPCM cells raises latency, energy and thermal concerns, thereby rendering such a design impractical. To understand these concerns, let us consider an OPCM array that uses the EPCM architecture from Figure 3 with either an optical row buffer or an electrical row buffer. Such an OPCM array architecture has following limitations:

**Limitations with optical row buffer:** An optical row buffer can be designed using a row of GST elements, whose states are controlled using optical signals. When a row is read from the OPCM array using an optical signal, the data is encoded in the signal’s intensity. This intensity is not large enough to update the state of the GST elements in the optical row buffer. So the read value first needs to be converted into an electrical signal. Based on this value, an optical signal with the appropriate intensity is generated to write the value into the
optical row buffer. Essentially we perform an extra O-E and E-O conversion. This necessitates the use of photodetectors, receivers, transmitters and optical pulse generators, which adds to the energy and latency of a memory access. Hence, an optical row buffer is not a viable option.

Limitations with electrical row buffer: An electrical row buffer can be designed either using capacitor cells as in DRAM or using phase change materials controlled using electrical current as in EPCM. In both cases, the row buffer is accessed using electrical signals. This increases the access latency and energy, and creates thermal issues as follows:

1) Impact on read latency: Upon receiving a row address from the MC on electrical links, the address first needs to be converted to an optical pulse, which is then used to read data from OPCM cells. After optical readout of an entire row from OPCM array, the data has to be converted back into electrical domain to store it in the row buffer. These two operations require an E-O and an O-E conversion, respectively, inside the OPCM array. These additional E-O/O-E conversions adds a latency of 25 – 30 cycles for each read access [7].

2) Impact on write latency: When writing data from the row buffer to the OPCM array, a set of sense amplifiers reads the data from the electrical row buffer. This row buffer data is then mapped onto optical signals with appropriate intensities using a pulse generation circuitry within memory. The optical signals are then used to write the data to the OPCM cells. Therefore, the write operation requires three E-O/O-E conversions, which adds a latency of 40 – 45 cycles for each write access [7].

3) Impact on read/write energy: The energy spent in the peripheral circuitry for optical signal generation and readout, as well as in the circuitry for E-O-E conversion increases the active power dissipation within memory [7], [61], [63]. Since each read/write operation encounters multiple E-O-E conversions, the energy per read and write access rises considerably high (> 200pJ/bit) [25].

4) Thermal issues: The MRRs used in the OPCM array are highly sensitive to thermal variations [65]. The thermal variations due to active electrical circuits within memory lowers the reliability of the MRR operation. Such a design calls for active thermal and power management in OPCM, which contributes to a power overhead of 10 – 30W [3]. Furthermore, using silicon-photonic links in combination with OPCM requires additional E-O and O-E conversions with this EPCM architecture that exacerbate the above discussed problems. Hence, we argue for the need to redesign the microarchitecture and the read/write access mechanisms that are tailored to the properties of the OPCM cell technology and the associated silicon-photonic link technology.

IV. COSMOS ARCHITECTURE

In this section, we describe the microarchitecture of the high-throughput OPCM array in COSMOS. The key innovation of our proposed microarchitecture is enabling direct access of OPCM cells by the optical signals in the silicon-photonic links. This direct access avoids the extra E-O and O-E conversions that are required if we were to adapt the EPCM architecture for COSMOS. Our OPCM array microarchitecture is a hierarchical multi-banked design that maximizes the degree of parallelism for read and write accesses within the array using a combination of WDM and MDM. A distinguishing feature of our OPCM array design is that it does not contain any active circuits that consume power, i.e., it only contains passive optical devices. Figure 4 illustrates the detailed microarchitecture of our proposed OPCM array in COSMOS that uses GST as the phase change material. We describe each component of the proposed architecture, particularly focusing on how to access an OPCM cell in the optical domain with minimal E-O and O-E conversions.

A. OPCM Tile

An OPCM tile (see Figure 4c) consists of an \( n \times n \) array of GST elements, i.e., OPCM cells. The GST elements are placed on top of waveguide crossings as shown in Figure 4d. This organization enables every OPCM cell to be accessed using a unique pair of optical signals: one on the associated row and one on the associated column. We need a total of \( n \) unique optical signals with wavelengths \( \lambda_1, \lambda_2, \ldots, \lambda_n \) that are routed in the rows (one per row waveguide), and \( n \) unique optical signals with wavelengths \( \lambda_{n+1}, \lambda_{n+2}, \ldots, \lambda_{2n} \) that are routed in the columns (one per column waveguide). Wavelengths \( \lambda_1 \) to \( \lambda_n \) together form the Tile Row Access (TRA)-channel, and wavelengths \( \lambda_{n+1} \) to \( \lambda_{2n} \) together form the Tile Column Access (TCA)-channel. A TRA-channel (and similarly each TCA-channel) is mapped to one or more waveguides depending on the number of wavelengths that can be multiplexed in a waveguide. Owing to MLC, each OPCM cell stores \( b_{cell} \) bits. The total capacity of an OPCM tile is \( n^2 \cdot b_{cell} \). A maximum of \( n \) cells can be read/written in parallel from a single tile, which gives us a peak throughput of \( n \cdot b_{cell} \) bits per read/write access for a tile.

B. OPCM Bank

Figure 4b shows the organization of an OPCM bank. The OPCM bank is composed of an array of \( m \times m \) OPCM tiles, and has a total capacity of \( m^2 \cdot n^2 \cdot b_{cell} \) bits. The OPCM bank uses \( m \) TRA-channels, one for each row in the bank, and \( m \) TCA-channels, one for each column in the bank to communicate with the E-O-E control unit. Each TRA-channel uses \( \lambda_1 \) to \( \lambda_n \), and each TCA-channel uses \( \lambda_{n+1} \) to \( \lambda_{2n} \). We design a hierarchical array of OPCM cells (\( m^2 \) tiles with \( n^2 \) OPCM cells per tile) instead of a large monolithic array (\( m^2 \cdot n^2 \) OPCM cells), as designed by Feldman et al. [27], [28] to decrease the laser power by the optical signals. With our proposed design, the laser sources only need to support \( 2n \) unique optical signals (in the range of \( \lambda_1 \) to \( \lambda_{2n} \)) instead of the \( m \cdot 2n \) unique optical signals that would be required in a large monolithic array. We utilize MRRs to couple the optical signals of each TRA-channel and TCA-channel to its corresponding tile. We need \( n \) MRRs that are tuned to \( \lambda_1 \) to \( \lambda_n \) in each of the \( m \) TRA-channels.
and $n$ MRRs that are tuned to $\lambda_{n+1}$ to $\lambda_{2n}$ in each of the $m$ TCA-channels.

C. Multi-banked OPCM Array

Figure 4a shows the proposed multi-banked organization of the OPCM array using MDM. We interleave a cache-line across multiple banks. There are $p$ banks, each supporting one of the $p$ spatial modes of the $2n$ optical signals. Bank 1 only uses mode 1 of all optical signals $\lambda_1$, ..., $\lambda_n$ and $\lambda_{n+1}$, ..., $\lambda_{2n}$. Bank 2 only uses mode 2 of all optical signals, and so on. The waveguides connecting the OPCM to the E-O-E control unit are multi-mode waveguides, which carry all the $p$ spatial modes of optical signals. We employ single-mode MRRs [89], [97] that couple a single spatial mode of optical signals from the multi-mode waveguide to a bank. Multiple prior works have exploited MDM property of optical signals coupled with WDM to design high-bandwidth-density silicon-photonic links [54], [92].

D. Address Mapping in COSMOS

Figure 4e shows an example mapping of the physical address received by the MC to the physical location of cells within the OPCM array in COSMOS. A cache line of 64B is stored in a total of 128 OPCM cells with 4bits/cell. We interleave the cache line across 4 different banks. Within a bank, we map the 128-bit chunk of a cache line to a tile. The tile has $32 \times 32$ cells, and so we map that 128-bit chunk to an entire row within a tile. The row (column) field of physical address in the MC is mapped to the row ID of tile (column ID of tile) field and the row ID of cell (column ID of cell) field. In Figure 4e, we show how the different fields of the physical address $0x10301FC0$ are mapped to bank ID, row ID of tile, column ID of tile, row ID of cell, and column ID of cell.

V. ACCESS PROTOCOL IN COSMOS

To enable high-throughput access of OPCM cells within the OPCM array, we propose a novel read and write access protocol for COSMOS. When the MC issues a read or write operation, the row address and column address are entered into the Row Address Queue and Column Address Queue, respectively, and the write data is entered into the Data Buffer in the E-O-E control unit.

A. Writing a cache line to OPCM array

To write a cache line to the OPCM array, the E-O-E control unit identifies the bank ID, the row ID and column ID of the tile, and the row ID and column ID of the cell within a tile using the address mapping. In our example with $32 \times 32$ array of cells in a tile, when writing 128-bit chunk of a cache line, we end up updating all the cells in a row (any misaligned accesses are handled on the processor side). Hence, for writes at cache line granularity, the column ID within a tile is not used. The E-O-E control unit determines the optical intensity that is required at each OPCM cell in the row to write the 128-bit chunk of the cache line. It then breaks down the optical intensity into two signals, one with a constant intensity of $I_0$ and the other with a data-dependent intensity of $I_i$, where $i = 1, 2, ..., 128$. The E-O-E control unit modulates the constant intensity $I_0$ onto the optical signal corresponding to the row (selected by the row ID of cell) within a tile. The E-O-E control unit then modulates the data-dependent optical intensities (i.e., $I_1$, $I_2$, ..., $I_{128}$) onto the optical signals corresponding to the columns within the tile. The E-O-E control unit transmits the row signal $I_0$, and the column optical signals $I_1$, $I_2$, ..., $I_{128}$ in parallel to write the cache line in the OPCM array. The superposition of the optical signals, i.e., $I_0 + I_1, I_0 + I_2, ..., I_0 + I_{128}$ updates the state of the OPCM cells. Note that since a cache line is spread across 4 banks, the E-O-E control unit modulates data on optical signals to write to an OPCM tile in each of these 4 banks. None of the optical signals individually carries sufficient intensity to trigger a state transition at any cell, so none of the other cells along the row or column are affected.

B. Reading a cache line from OPCM array

To read a cache line from OPCM array, the E-O-E control unit transmits sub-ns optical pulses along all the columns
in a tile that contain the cache line and measures the pulse attenuation. However, there are multiple OPCM cells along each column and so the output intensity of optical signals will be attenuated by all cells in that column. It is, therefore, not possible to determine the OPCM cell values using a one-pulse readout. Hence, we use a three-step process for read operation of OPCM array in COSMOS.  

1. To read a cache line, the E-O-E control unit first determines the bank ID, row ID and column ID of tile, row ID and column ID of cell. The E-O-E control unit transmits a read pulse $RD_1$ through all the columns in a tile containing the cache line. Note that since a cache line is spread across 4 banks, the E-O-E control unit transmits $RD_1$ on the 4 different optical modes corresponding to the 4 banks. Each read pulse is attenuated by all the OPCM cells in the column. The attenuated pulses are received by the E-O-E control unit, which records the intensities of these attenuated pulses as $I_{1,1}$, $I_{2,1}$, ..., $I_{128,1}$. These intensities are converted into electrical voltage and stored as $V_{1,1}$, $V_{2,1}$, ..., $V_{128,1}$.  

2. The E-O-E control unit then transmits a RESET pulse to the OPCM cells of the cache line, i.e., all the cells along a row within a tile. All the cells along the row are now amorphized and have 100% optical transmission. This RESET operation in step 2 of the read operation destructs the original data in the OPCMs.  

3. The E-O-E control unit then sends a second read pulse $RD_2$ through all the columns of a tile containing the cache line. Each read pulse is again attenuated by all OPCM cells in the column. Given that step 2 amorphized all OPCM cells of the cache line, the output pulse intensities are different from those in step 1. The attenuated pulses are received by the E-O-E control unit, which records the intensities of these attenuated pulses as $I_{1,2}$, $I_{2,2}$, ..., $I_{128,2}$. These intensities are converted into electrical voltage and stored as $V_{1,2}$, $V_{2,2}$, ..., $V_{128,2}$. The E-O-E control unit computes the difference of the stored voltages of steps 1 and 3, i.e., $V_{1,1} - V_{1,2}$, $V_{2,1} - V_{2,2}$, ..., $V_{128,1} - V_{128,2}$. This difference is used to determine the cache line data stored in the OPCM cells.

C. Opportunistic Writeback after Read

The RESET operation in step 2 of the read operation destructs the original data in the OPCMs. We, therefore, perform an opportunistic writeback of the cache line to the OPCM cells. After completing the 3 steps of the read operation, the read data and the address are saved into a holding buffer in the E-O-E control unit. When there are no pending read or write operations from the MC, the E-O-E control unit reads the data and its address from the holding buffer and writes the data back to the OPCM array. This writeback operation does not block any critical pending read and write operations coming from the MC. The dependencies in read and write requests between the holding buffer and the data buffer is handled in the E-O-E control unit. For a Read-After-Read case, the second read operation reads the data from the holding buffer if present. If the data is not in the holding buffer then the second read operation just uses the 3-step process + writeback (described above) to complete the read operation. For a Write-After-Read case, if the write address matches the read address and there is an entry for that read in the holding buffer, then the corresponding entry in the holding buffer is invalidated. The write data is then entered into the data buffer and then written into the appropriate OPCM array. The Write-After-Write and Read-After-Write are not an issue as the E-O-E control unit processes them in order.

VI. E-O-E CONTROL UNIT DESIGN

Our proposed E-O-E control unit provides the interface between the processor and the OPCM array. The MC sends standard DRAM access protocol commands to the E-O-E control unit. The E-O-E control unit maps these commands onto optical
signals that read/write the data from/to OPCM array. Given that OPCM cells do not require Activate, Precharge and Refresh operations, the E-O-E control unit does not take any action for these commands. Though we can design a COSMOS-specific MC and the associated read/write protocol, our goal is to enable the COSMOS operation with a standard MC in any processor. The E-O-E control unit uses the following five sub-units to read from and write to the OPCM array: data modulation unit (DMU), address mapping unit (AMU), pulse selector unit (PSU), pulse amplification unit (PAU), and pulse filtering unit (PFU). Each OPCM bank has a dedicated set of these five sub-units in the E-O-E control unit. Figure 5a shows the design of the E-O-E control unit in COSMOS and the internals of these sub-units.

Figure 5b illustrates the sequence of operations in the E-O-E control unit for write operation to a bank containing $512 \times 512$ tiles with $32 \times 32$ cells per tile (same design as that used in Figure 4e). The AMU in the E-O-E control unit first receives the row address and then the column address from MC (Step 1). Depending on the addresses, the PSU in the E-O-E control unit selects the appropriate optical signals using the address mapping explained in Section IV-D (Step 2). The PSU selects one optical signal and 32 optical signals for writing to 32 cells in a tile. In parallel with the write address, the DMU in the E-O-E control unit receives the write data from the MC (Step 3). The DMU generates a unique bias current for each of the 32 optical signals depending on write data and applies the currents to the semiconductor optical amplifiers (SOA) in the PAU (Step 4). The SOAs amplify the optical signals to the required intensities. These amplified signals and the optical signal traverse through the silicon-photonic links to the appropriate OPCM cells in the bank, and SET/RESET the cell (Step 5). The E-O-E control unit incurs a latency of $T_{EO}$ cycles to map the address and data onto optical signals, resulting in a peak throughput of $1/T_{EO}$.

Figure 5c illustrates the sequence of operations in the E-O-E control unit for the 3-step read operation from a bank. In the first step, the AMU receives the row and column addresses from MC and selects the appropriate 32 optical signals in the PSU using the address mapping explained in Section IV-D (Step 1.1). The DMU generates a low-intensity readout pulse ($RD_1$) and the PAU modulates this pulse on the 32 optical signals (Step 1.2). The optical signals traverse through the silicon-photonic link and then through the columns in the tile. The optical signals lose intensity as they pass through all the OPCM cells in their associated columns (Step 1.3). The intensities of these attenuated signals are recorded by the PFU (Step 1.4). The PFU then converts the optical intensities into electrical voltages, $V_{11}, V_{21}, ..., V_{321}$ (Step 1.5). In the second step, the DMU generates an optical intensity that corresponds to a RESET pulse. This RESET pulse is mapped onto the appropriate optical signals and these signals are sent to the OPCM array (Step 2.1). The signals traverse through the silicon-photonic links and amorphize the OPCM cells corresponding to the read address (Step 2.2). In the third step, the DMU generates another readout pulse ($RD_2$) and the PAU modulates this pulse on a set of 32 optical signals (Step 3.1). These signals traverse through the silicon-photonic links and then through the appropriate columns in the tile. These signals too loses intensity as they pass through all the OPCM cells in their associated columns (Step 3.2). The PFU records these attenuated signals (Step 3.3) and converts these optical signals into electrical voltages $V_{12}, V_{22}, ..., V_{322}$ (Step 3.4). Finally, the PFU computes $V_{11} - V_{12}, V_{21} - V_{22}, ..., V_{321} - V_{322}$ to determine the data (Step 3.5) and sends the data to the MC. The PFU also writes this data back to the holding buffer in the DMU (Step 3.6).

### VII. Evaluation Methodology

#### A. Multicore System with COSMOS

We use an 8-core processor for our evaluation. We primarily evaluate COSMOS with 4-bit MLC OPCM cells (given that OPCM cell with 5 bits/cell has been prototyped [52]) against an EPCM with 2 bits/cell. Table I details the processor and memory configurations. For processor-memory networks, we consider electrical as well as silicon-photonic links, with 1 GT/s transfer rate per link. We obtain a peak bandwidth of 64 GB/s in EPCM and 256 GB/s in COSMOS.

The OPCM array in COSMOS is organized as a single rank connected to a memory channel on the MC via the E-O-E control unit. Each one of the 8 OPCM banks has its dedicated set of DMU, ATU, PSU, PAU, and PFU sub-unit in the E-O-E control unit. The average SET latency is $t_{SET} + t_{EOE} = 165$ ns, the RESET latency is $t_{RESET} + t_{EOE} = 30$ ns, and the read latency is $t_{read}$ (time for 3-step read operation) + $t_{EOE}$, i.e., 30 ns. A maximum of $t_{SET}/t_{EOE} = 32$ writes can be issued from the E-O-E control unit to OPCM in parallel. So, we can write $32 \times b_{cell}$ bits in parallel. A maximum of $t_{read}/t_{EOE} = 5$ reads is issued from the E-O-E control unit to OPCM in parallel. So, we can read $5 \times b_{cell}$ bits in parallel. We use a holding buffer that is large enough (16 cache line slots from our evaluations) to avoid stalling any read/write memory requests from the MC.

| Processor, On-chip caches | 8-core, 1GHz x86 ISA, Out-of-Order, 192 ROB entries, dispatch/fetch/issue/commit width=8 |
|--------------------------|-------------------------------------------------------------------------|
| L1 caches                | 32KB split L1 IS and DS, 2-way, 2-cycle hit, 64B, LRU, write-through, MSHR: 4 instruction & 32 data |
| L2 cache                 | Shared L2S, 2MB, 8-way, 20-cycle hit, 64B, LRU, write-back, MSHR: 32 (I & D) |
| Main memory (2GB)        | 4 banks, 8 devices/rank, 1 rank/channel, bus width = 64, burst length = 4 |
| EPCM [21]                | $t_{SET} = 120\text{ns}$, $t_{RESET} = 50\text{ns}$, $t_{read} = 60\text{ns}$, $t_{BURST} = 4\text{ns}$ |
| OPCM array in COSMOS [52], [78] | 8 banks, 1 rank/channel, 1 device/rank, bus width = $32 \times b_{cell}$, burst length = 8 |
|                          | $t_{SET} = 160\text{ns}$, $t_{RESET} = 25\text{ns}$, $t_{read} = 25\text{ns}$, $t_{BURST} = 1\text{ns}$, $t_{EOE} = 5\text{ns}$ |

| Processor, On-chip caches | 8-core, 1GHz x86 ISA, Out-of-Order, 192 ROB entries, dispatch/fetch/issue/commit width=8 |
|--------------------------|-------------------------------------------------------------------------|
| L1 caches                | 32KB split L1 IS and DS, 2-way, 2-cycle hit, 64B, LRU, write-through, MSHR: 4 instruction & 32 data |
| L2 cache                 | Shared L2S, 2MB, 8-way, 20-cycle hit, 64B, LRU, write-back, MSHR: 32 (I & D) |
| Main memory (2GB)        | 4 banks, 8 devices/rank, 1 rank/channel, bus width = 64, burst length = 4 |
| EPCM [21]                | $t_{SET} = 120\text{ns}$, $t_{RESET} = 50\text{ns}$, $t_{read} = 60\text{ns}$, $t_{BURST} = 4\text{ns}$ |
| OPCM array in COSMOS [52], [78] | 8 banks, 1 rank/channel, 1 device/rank, bus width = $32 \times b_{cell}$, burst length = 8 |
|                          | $t_{SET} = 160\text{ns}$, $t_{RESET} = 25\text{ns}$, $t_{read} = 25\text{ns}$, $t_{BURST} = 1\text{ns}$, $t_{EOE} = 5\text{ns}$ |
B. Simulation Framework

We model the architectural specifications of the system in gem5 [15]. We conduct full-system simulations in gem5 with Ubuntu 12.04 OS and Linux kernel v4.8.13. We fast-forward to the end of Linux boot and execute each workload for 10 billion instructions. The main memory models for DDR4 are based on DRAMSim2 [77]. For modeling EPCM and OPCM, we integrate NVMain2.0 [68] in gem5.

C. Workloads

We simulate graph applications from GAP-BS benchmark [12] and HPC applications from NAS-PB benchmark [8]. We evaluate the graph applications on three different input datasets from SNAP repository [49]: Google web graph (google), road network graph of Pennsylvania (roadNetPA), and Youtube online social network (youtube). For HPC applications from NAS-PB benchmark, we use the large dataset. We execute 8 threads of these applications in a workload.

VIII. Evaluation Results

A. COSMOS vs EPCM

1) Performance: We compare EPCM (2bit MLC or EPCM-2bit) that uses 64 processor-to-memory electrical links with COSMOS (4bit OPCM cells, or COSMOS-4bit) that also uses 64 processor-to-memory silicon-photonic links, and with COSMOS-4bit that uses 256 processor-to-memory silicon-photonic links. Figure 6 shows the overall performance (execution time in seconds) for systems with these three configurations. Compared to the EPCM-2bit with 64 electrical links, COSMOS-4bit with 64 silicon-photonic links has on average 1.52× better performance across all workloads. This performance improvement is due to the higher bits/access throughput of COSMOS resulting from higher MLC capacity and the single-cycle latency in silicon-photonic links. Increasing the number of silicon-photonic links from 64 to 256 further improves the system performance. Compared to EPCM-2bit using 64 electrical links, we observe performance improvement of 2.14× on average for graph and HPC workloads with COSMOS-4bit using 256 silicon-photonic links. These performance benefits are due to denser WDM in silicon-photonic links. The key takeaway from this comparison is that even though the OPCM cells suffer from long write latency similar to EPCM cells, the superior MLC capacity of OPCM cells that are directly accessed by high-bandwidth-density silicon-photonic links improves the system performance in COSMOS.

2) Throughput: Figures 7a and 7b show the read and write throughput, respectively, of COSMOS-4bit with 256 silicon-photonic links, and EPCM-2bit with 64 electrical links. Compared to EPCM-2bit with 64 electrical links, COSMOS-4bit with 256 silicon-photonic links theoretically has 8× higher peak throughput, i.e., 2× due to higher MLC capacity and the 4× due to the increased number of processor-to-memory links. Therefore, it is possible to issue increased number of parallel read and write operations in COSMOS-4bit. From figure 7a and figure 7b we observe that COSMOS-4bit has 2.09× higher read throughput and 2.15× higher write throughput, respectively, than EPCM-2bit for graph and HPC workloads. This increased read and write throughput of COSMOS-4bit hides the long write latencies. Figure 7c shows that the average memory latency (read+write) of COSMOS-4bit is 33% lower than EPCM-2bit across all workloads. The key insight from this study is the increased read and write throughput provided by the higher MLC capacity and the silicon-photonic links hides the long write latencies of OPCM cells in COSMOS.

3) Energy Consumption: The primary contributors to the overall power consumption during the read and write operations are the different active components in the E-O-E control unit and the laser sources that drive the silicon-photonic links. The OPCM array in COSMOS consists of only passive optical devices, so it does not consume any active or idle power. The electrical power consumed in the laser source is proportional to its optical output power, which in turn depends on the optical losses in the path of the optical signal and the minimum power required to switch the farthest GST element. Table II lists the optical losses in the various components and the

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**TABLE II: Optical power budget for 2GB COSMOS.** The table shows optical power losses and SOA gain along the optical path from laser source to OPCM cells.

| Loss/gain component | Single | Total |
|---------------------|--------|-------|
| Coupling loss        | −1dB   | −1dB [11] |
| MRR drop loss (E-O-E control) | −0.5dB [32] | −0.5dB |
| MRR through loss (E-O-E control) | −0.05dB [32] | −3.2dB |
| Propagation loss (Laser to SOA)      | −0.3dB/cm [81] | −0.09dB |
| SOA gain             | +20dB   | +20dB |
| Propagation loss (SOA to OPCM)        | −0.3dB/cm [81] | −0.09dB |
| Bending loss         | −0.167dB [81] | −0.167dB |
| MRR drop loss (OPCM) | −0.5dB [32] | −0.5dB |
| MRR through loss (OPCM) | −0.05dB [32] | −3.2dB |
| Propagation loss (in OPCM) | −0.03dB/cm [81] | −4.91dB |
| Max. power required to SET the GST | 155pW/250ns [52] | −2.67dBm |
| Power per optical signal | −7.22dBm ≈ 0.19mW |
| Laser wall-plug efficiency | 20% |
| **Total laser power** | 16.38W |

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![Fig. 6: Performance comparison of COSMOS with EPCM.](image-url)
maximum switching power required at the GST element in decibels (dB). The various optical losses and SOA gains are obtained from prior characterization works [11], [32], [52], [81]. By accounting for the wall-plug efficiency, we calculate the minimum required laser power per optical signal as 0.95mW. Aggregating the laser power for all optical signals required in a 2GB COSMOS system, we get a total laser power of 16.38W.  

In the E-O-E control unit, the current-DAC in DMU and the ADC in PFU consume 0.3mW each [74]. For OPCM-4bit, 32 write operations can be issued in parallel per bank, i.e., we can write $32 \times b_{cell} \times 8 = 128B$ in parallel with an average write latency of 160ns. That aggregates to writing 2 cache lines of 64B each in parallel. A cache line is interleaved across 4 banks and is row aligned in an OPCM tile. Therefore, we need 4 row optical signals and 4 $\times 32$ column optical signals to write a cache line. Therefore, the total power of the laser, SOAs and DACs in the E-O-E control unit for writing 2 cache lines in parallel aggregates to 334.8mW. This equates to 40.68pJ/bit for writing to COSMOS-4bit.

For read operation, up to 5 read operations can be issued in parallel per bank, i.e., $5 \times b_{cell} \times 8 = 20B$ bits in parallel, with a read latency of 25ns. The total power of the laser, SOA, DAC, and ADC in E-O-E control for 5 parallel read operations is 9.3mW, resulting in a read energy of 11.6pJ/bit for COSMOS-4bit. The energy consumed in the electrical links connecting the processor and the E-O-E control unit is $< 1pJ/bit$ [22]. For EPCM, we use NVSim [25] to compute the energy-per-bit for read and write operations. The opportunistic writeback operation in COSMOS uses the same energy as that required for write operation. Table III shows the energy-per-bit for EPCM-2bit and COSMOS-4bit. The read and write energy-per-bit of COSMOS-4bit are $3.8 \times$ and $5.97 \times$ lower, respectively, than that of EPCM-2bit.

We assume all laser sources are ON all the time. Development of laser power management techniques is left for future work.

### B. Sensitivity Analysis of COSMOS

1) **MLC values:** Rios et al. gave the first demonstration of a 2-bit OPCM cell operation [78]. Advances in optical signaling and control have resulted in the demonstration of denser multilevel OPCM cells. Li et al. demonstrated 5-6 bits per OPCM cell [52]. Further prototypes have demonstrated scalable integration of OPCM cell arrays in silicon and silicon nitride platforms [28], [51]. With the maturity in optical integration technologies, OPCM technology with 8 bits/cell is expected in the near future [52]. We compare the systems performance of COSMOS that uses OPCM cells with different MLC capacities, ranging from 2 bits/cell to 8 bits/cell, for the same number of silicon-photonic links (see Figure 8). The performance across applications increases, on average, by 39.2% and 26.4% as the MLC capacity of OPCM cells increases from 2 bits/cell to 4 bits/cell and from 4 bits/cell to 8 bits/cell, respectively. An OPCM cell with higher MLC capacity will provide higher memory throughput.

2) **Number of Silicon-Photonic Links:** We compare the performance of COSMOS-4bit with different number of silicon-photonic links (see Figure 9). Multiplexing a higher number of optical signals in silicon-photonic links enables parallel read and write accesses of a higher number of OPCM cells. Due to this increased throughput, the overall system performance improves as the number of silicon-photonic links increases. We observe a performance improvement of 29.3% (on average) for COSMOS-4bit with 256 silicon-photonic links over COSMOS-4bit with 64 links.

3) **Holding Buffer:** Figure 10 shows the system performance comparison with and without the holding buffer. In absence of the holding buffer, the read data needs to be written back to the OPCM cells immediately after readout because the

### Table III: Energy-per-bit for read and write accesses.

| Energy-per-bit (pJ/bit) | EPCM-2bit | COSMOS-4bit |
|------------------------|-----------|-------------|
| Write                  | 243       | 40.68       |
| Read                   | 44.5      | 40.68       |
| Opportunistic Writeback| NA        | 40.68       |

![Fig. 7: (a) Read throughput, (b) Write throughput, (c) Average memory latency](image)

![Fig. 8: Performance comparison of COSMOS with different MLC.](image)

![Fig. 10: System performance comparison of COSMOS with holding buffer.](image)
when the DB in the E-O-E control unit is empty, ensuring MLC capacities. Here, we assume that for a given memory is COSMOS size in bytes (2

et al. lifetime using the equation proposed by Qureshi determine the average write rate We estimate the COSMOS endurance of OPCM cells also depend on the read rate. We in COSMOS also includes a write (RESET) in step 2, the often we write to that cell [70]. Given that the read operation incurs a total latency of readout latency (25ns) + writeback latency (160ns). In contrast, when the E-O-E control unit consists of a holding buffer, the read data is stored in the holding buffer at the end of read operation. The data from the holding buffer is written back to the OPCM cells only when the DB in the E-O-E control unit is empty, ensuring that the writeback operation does not stall any critical read and write operations. Using the highest read and write rate of the workloads that we evaluated, we determine that a holding buffer with 16 cache line slots, i.e., 1KB, is enough to avoid any memory read/write stalls. The holding buffer occupies 1000 μm² area and can be integrated into the E-O-E control unit with minimal overhead.

### C. Endurance Analysis of COSMOS

Similar to EPCM, OPCM cells have lower endurance due to cell wearout. The OPCM cell endurance depends on how often we write to that cell [70]. Given that the read operation in COSMOS also includes a write (RESET) in step 2, the endurance of OPCM cells also depend on the read rate. We determine the average write rate We estimate the COSMOS lifetime using the equation proposed by Qureshi et al. [71]:

\[ Y = \frac{W_m}{B \times F \times S} \]

where, \( Y \) is lifetime in years, \( W_m \) is maximum allowable writes per cell (10⁶ for OPCM cells [52], [78]), \( B \) is write rate in Bytes/cycle (average read+write rate across graph and HPC workloads), \( F \) is core frequency in Hz (1GHz), and \( S \) is COSMOS size in bytes (2GB, 4GB and 8GB).

Figure 11 plots the average lifetime for OPCM with different MLC capacities. Here, we assume that for a given memory size, all MLC options use the same number of silicon-photonic links. Hence, the COSMOS with 8-bit OPCM cells has higher effective throughput than the COSMOS with 4-bit OPCM cells and so an application running on COSMOS-8bit runs faster than an application running on COSMOS-4bit. As a result, for an application, even if the absolute number of memory writes is same for both COSMOS-8bit and COSMOS-4bit, the number of writes/second to COSMOS-8bit is higher than the number of writes/second to COSMOS-4bit. Hence, the lifetime of COSMOS-8bit is lower than that of the COSMOS-4bit and COSMOS-2bit.

### D. Area Analysis of the OPCM Array

To design the OPCM array in COSMOS, we use the prototype of a GST element developed by Rios et al. [75], [78] and the MRR dimensions from prior work as shown in Table IV. We use 3D stacking for OPCM array, with different banks stacked vertically (one bank per layer). The multi-mode waveguides in the interposer are routed vertically, and at each layer single-mode MRRs filter out the mode of all optical signals that belong to its corresponding bank. For a 2GB 4-bit OPCM array with 8 banks, a single bank consists of 1024 tiles with 32 cells/tile and a row and column of MRRs as shown in Figure 4b. A bank, therefore, is composed of 1024 × 32 GSTs along a row/column with \((1024 \times 32 - 1) \times 50\mu m\) of separation between GSTs, and a single row/column of MRRs at the beginning. Using the dimensions of these optical devices listed in Table IV, we calculate the area of a 2GB OPCM array and its bit density and report it in Table V.

We compare the area and bit density of the 3D-stacked OPCM array in COSMOS with DDR4, 3D-stacked HBM2.0 and EPCM-2bit memory system (see Table V). With current OPCM cell footprints, 3D-stacked OPCM-4bit has 1.2× and 2.9× lower bit density than DDR4 and HBM2.0, respectively, and 1.25× higher bit density than EPCM-2bit. 3D-stacked

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### Table IV: Dimensions of optical devices in the OPCM array.

| Optical device | Dimension |
|----------------|-----------|
| GST           | 500nm × 500nm [75], [78] |
| Separation between adjacent GSTs | 50μm [33] |
| MRR diameter  | 5μm [50]   |

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3The tile size is limited by the number of unique optical signals in C and L bands with sufficient guardbands (32 in our case). The number of banks depends on the number of unique electromagnetic modes that can be supported (8 in our case).
TABLE V: Bit density (bits/mm²) of memory technologies.

| Memory technology | Area of 2GB memory (mm²) | Bit density (bits/mm²) |
|-------------------|---------------------------|------------------------|
| DDR4              | 224mm² [2]                | 9.14MB/mm²             |
| HBM2.0            | 91.99mm² [39]             | 22.26MB/mm²            |
| EPCM-2bit         | 336mm² (simulated [25])   | 6.095MB/mm²            |
| 3D OPCM-4bit      | 268.43mm² (calculated)    | 7.63MB/mm²             |
| 3D OPCM-8bit      | 67.1mm² (calculated)      | 30.52MB/mm²            |

Fig. 12: Performance comparison of OPCM with DDR4 DRAM.

OPCM-8bit has 3.4×, 1.4× and 5× higher bit density than DDR4, HBM2.0 and EPCM-2bit, respectively. Nevertheless, device-level research efforts have demonstrated that GST elements are highly scalable and can retain the electrical and optical characteristics at amorphous and crystalline states [73], [88]. An aggressive chip prototype with 200nm × 200nm GST element with 50nm separation has been recently fabricated [33]. These aggressive optical fabrication technologies promise achieving several orders higher densities for OPCM arrays than current DRAM technologies.

E. COSMOS vs DRAM

The overarching goal of COSMOS is to replace DRAM systems that are used widely in computing systems. We noted that though all other NVM systems (in their current form) provide non-volatility, data persistence and high scalability, their poor performance negates their benefits and makes them impractical to replace DRAM systems. We, therefore, compare the performance and energy of DDR4 with 64 electrical links, DDR4 with 256 silicon-photonic links [13], COSMOS-4bit with 256 silicon-photonic links, and COSMOS-8bit with 256 silicon-photonic links. Figure 12 shows the overall system performance across the four configurations. For DDR4, replacing 64 electrical links with 256 silicon-photonic links provides 32% average performance improvement. This improvement results from the higher throughput due to dense WDM and single-cycle latency of silicon-photonic links. With COSMOS-4bit, we obtain 5.6% improvement in performance compared to DDR4 with 64 electrical links. This is in stark contrast to EPCM-2bit, which performs 3 – 4× worse than DDR4. COSMOS-8bit with 256 silicon-photonic links performs 30.6% better than DDR4 with 64 electrical links and 2.1% better than DDR4 with 256 silicon-photonic links. The increased read and write throughput due to the higher MLC capacity and dense WDM silicon-photonic links reduces the average memory access latency of COSMOS. Figure 7c shows the the average memory latency in COSMOS is 33.64ns across all workloads, which is lower than DDR4 DRAM (40ns). Moreover, from Table III we observe that energy-per-access for write operation in COSMOS-4bit is similar to that of DDR4 DRAM (40pJ/bit [1]) and the energy-per-access for read operation in COSMOS-4bit is 3.45× lower than DDR4 DRAM (40pJ/bit [1]).

Though we evaluate DDR4 memory with silicon-photonic links, such a system encounters several design challenges. To support silicon-photonic links in DDR4, memory requests from MC require an E-O conversion in MC and an O-E conversion in memory, and memory responses from DDR4 require an E-O conversion in memory and an O-E conversion in MC. Effectively, we need two extra conversions on the memory side. The active peripheral circuitry to support E-O-E conversions within memory increases the power density and raises thermal concerns. Due to the high thermal sensitivity of MRRs, there is a need for active thermal management. The power and resulting thermal concerns affect the reliability of optical communication in DRAM systems.

We observe that COSMOS with 4 bits/cell OPCM array demonstrates similar performance and energy characteristics as current DDR4 systems, while COSMOS with 8 bits/cell OPCM array improves performance. This is particularly exciting as COSMOS exhibits zero leakage power, better scaling and non-volatility, making it a viable replacement for DRAM in the near future.

IX. RELATED WORK

A. Phase Change Memories

Several works have proposed architectural and management policies to address the PCM challenges and have designed EPCM systems either as a standalone main memory, as part of hybrid DRAM-PCM systems or as a storage memory between DRAM and flash memory [6], [26], [34], [35], [37], [40], [46], [47], [69], [71], [72], [83], [85], [95], [98]. Most of these efforts have focused on addressing the long write latency and high write energy. A summary of these efforts is shown in Table VI. Hybrid DRAM-PCM systems leverage the higher bit density in PCMs for improved performance, but at the cost of higher write energy [34], [46], [47], [71], [72]. To address PCM cell wearout, the techniques to enhance the write endurance include rotation-based wear leveling [70], process variation-aware leveling [24], [103], and writeback minimization and endurance management [29]. Due to lower write endurance, PCM cells are also susceptible to malicious write attacks. Common strategies employed in EPCMs to thwart these attacks include write-efficient data encryption [99], multi-way wear leveling [101], or randomized address mapping [80]. These techniques can be readily deployed in OPCM.

While several approaches discussed above address EPCM limitations, EPCM is not yet a viable alternative for DRAM.
TABLE VI: Survey of research efforts to improve write performance and write energy for using EPCM as main memory. The performance gains and energy reductions are shown in comparison to a naive EPCM system. (NR: Not reported)

|                                | Fine-grained power budgeting [35] | Write truncation [37] | Dynamic write consolidation [95] | Logical decoupling & mapping [98] | Proactive SET [69] | Partition-aware scheduling [83] | Double-XOR mapping [26] | Boosting rank parallelism [6] | Optical control with silicon-photonic links |
|--------------------------------|----------------------------------|-----------------------|----------------------------------|----------------------------------|-------------------|-------------------------------|------------------------|-----------------------------|----------------------------------|
| Performance gains              | 76%                              | 26%                   | 17.9%                            | 19.2%                            | 34%               | 28%                           | 12%                    | 16.7%                       | 2.31×                            |
| Energy reductions               | NR                               | NR                    | 13.9%                            | 14.4%                            | 25%               | 20%                           | NR                     | NR                          | 4×                               |

In Table VI, we see that optical control of PCMs combined with silicon-photonic links significantly improves performance and lowers energy, without using any of the complementary methods provided in prior work.

B. Silicon-Photonic Links and OPCM Cells

Silicon-photonic links have enabled high bandwidth-density and low-energy communication between processor and memory [10], [11], [13], [23], [59], [60], [84], [86], [87]. To provide high DRAM internal bandwidth, Beamer et al. [13] proposed a joint silicon-photonic link and electro-photonic DRAM design. However, the O-E-O conversion in DRAM adds to the latency. Optical control of memory cells can avoid this O-E-O conversion and enable signals in the silicon-photonic links to directly access the cells and deliver higher memory throughput.

Several recent efforts have prototyped GST-basd PCM cells with optical control. Rios et al. demonstrate the optical control of multi-bit GST-based PCMs with fast readout and low switching energies [78]. Zhang et al. [102] present an approach to selectively couple optical signals from MRR to GST. Feldman et al. [27], [28] design a prototype of a monolithic OPCM array based on waveguide crossing but not a comprehensive memory microarchitecture and access protocol to interface with the processor. Subsequent efforts demonstrate higher bit density per GST [52], in-memory computing on PCM cells using optical signals [76], basic arithmetic operations in OPCM [27], [28], and a behavioral model for neuromorphic computing [19]. We are the first to propose a comprehensive OPCM microarchitecture with custom read/write access protocols, and design an E-O-E control unit to interface the OPCM array with the processor.

X. CONCLUSION

EPCM systems suffer from long write latencies and high write energies, yielding poor performance and high energy consumption for data-intensive applications. In contrast, OPCM technology provides the opportunity to design high-performance and low-energy memory systems due to its higher MLC capacity and the direct cell access via high-bandwidth-density and low-latency silicon-photonic links. Adapting the current EPCM design architecture for OPCM systems, however, raises major issues in terms of latency, energy and thermal concerns, thereby rendering such a design impractical. We are the first to architect a complete memory system, COSMOS, which consists of an OPCM array microarchitecture, a read/write access protocol tailored for OPCM technology, and an E-O-E control unit that interfaces the OPCM array with the MC. Our evaluations show that, compared to an EPCM system, our proposed COSMOS system provides 2.09× higher read throughput and 2.15× higher write throughput, thereby reducing the execution time by 2.14×, read energy by 1.24×, and write energy by 4.06×.

We show that COSMOS designed with state-of-the-art technology provides similar performance and energy as DDR4. This is a significant finding as future higher-density OPCM cells are expected to provide better performance. Our promising first version of an COSMOS architecture opens doors for new architecture-level, circuit-level, and system-level methods to enable practical integration of OPCM-based main memory in future computing systems. Moreover, the high-throughput and scalable OPCM technology ushers in interesting research opportunities in persistent memory, in-memory computing, and accelerator-specific memory designs.

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