Applying ZCT to Two-Phase Boost Converter with IGBT Switches Used

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Abstract: A zero-current-transition (ZCT) strategy is proposed herein. This strategy is applied to a two-phase boost converter with isolated gate bipolar transistors (IGBTs) used as main switches. However, IGBTs have a current tail during the switch-off interval. Consequently, the proposed constant-frequency ZCT strategy along with common-ground auxiliary switches is employed to decrease the switching loss generated by the current tail. Furthermore, the light-load efficiency can be upgraded by regulating the switch-off instants and switch-on times of the two auxiliary switches. Moreover, two phases are interleaved with one phase having a phase difference of 180° from the other phase, and controlled by a current-sharing controller so that the input current can be distributed between the two phases as evenly as possible. Moreover, only one current sensing circuit is required to obtain information on currents in the two main switches. Above all, the number of phases can be extended with easy control of the ZCT and current balance.

Keywords: current balance; interleaved; IGBT; two-phase boost converter

1. Introduction

In recent years, due to the impact of the energy crisis, power supply products must have several features, such as power saving, stability and small size, etc. To meet these features, switching power supply will become the trend in power supply development in the future. However, due to the parasitic inductance and parasitic capacitance of the power switch elements in the traditional switching power supply, the power switch will cause switching loss under operation [1]. In addition, due to the parasitic inductance and parasitic capacitance of the power switch elements in the traditional switching power supply, the power switch will cause switching loss under operation [1]. In addition, if the insulated gate bipolar transistor (IGBT) is used as a power switch, the current tail during the turn-off period will increase the switching loss.

Based on the above, the literature [2–4] uses the resonant zero-current switching (ZCS) technique to reduce the switching loss due to hard switching, but the corresponding power switch must withstand extremely high resonant currents, thereby increasing the conduction loss. In addition, since the resonant inductor and the resonant capacitor have a fixed execution time, the ZCS technique requires the use of variable frequency control, so the filter is not easy to design. In the literature [5–9], ZCS techniques with pulse width modulation (PWM) are used. Although this PWM ZCS technique has improved the problem of increased conduction loss and difficulty in filter design, the power switch is still subjected to extremely high resonant inductor currents. In addition, there are many additional components used in [9].

To conquer the shortcomings of the PWM ZCS technique, the zero-current transition (ZCT) [10–12] can be realized by fixed frequency control and does not need to increase the current stress of the power switch, thereby reducing the conduction loss and making the filter design easy. In [12], there is a floating auxiliary switch used.

In the following, more papers with a ZCT turn-off are described. The literature [13] starts with the introduction of the conventional ZCT converter. The advantage of this circuit is that it can realize the ZCT turn-off of the main switch without increasing the voltage	
stress of the main switch, but the disadvantage is that the main switch is hard-switched during the turn-on period, increasing the current stress of the main switch, while the auxiliary switch is also hard-switched during the turn-on and -off period. In [14], a novel improvement is provided by putting a ZCT auxiliary circuit on the secondary side of the circuit, so that the main switch can achieve a ZCT turn-off, although the main switch has no additional current stress during the turn-on period, but on the contrary, the main switch has additional current stress during the turn-off period. The main switch in [15] has no additional current stress during the turn-on period, but the drawback is that the auxiliary switch is floating, which increases the design difficulty of the drive circuit to some extent. In [16], an upgraded method is used to direct the inductive energy that causes the auxiliary switch to have additional voltage stress to the output side through the transformer, and both the main switch and auxiliary switch can achieve a ZCT turn-off, which makes the efficiency improve effectively, but the demerit is that the circuit is complex and has too many switching elements, which increases the difficulty of circuit analysis. In [17], although the circuit is simple and there is no additional current stress on the main switch during the turn-on period, the disadvantage is that the voltage stress on the main switch and auxiliary switch is too large, which requires the use of high voltage withstanding IGBTs and hence increases the cost.

On the other hand, many power supply products nowadays take multiphase interleaved control [18–20] to increase the output power. However, the line impedance of each phase is not equal. Consequently, it is necessary to add current sharing control [21–23] to distribute the load current evenly in each phase. Furthermore, since the current sharing control should sample the current of each phase, a traditional multi-phase interleaved power supply should have a current sampling circuit for each phase to feedback the current signal of each phase so that the load current can be equally distributed in each phase.

In this paper, we propose a two-phase interleaved boost converter with main IGBT switches having the ZCT turn-on by using the proposed auxiliary circuits, along with the proposed current sensing technique. The basic operating principle and mathematical deduction for the proposed topology are described in detail, then its feasibility is evaluated by the IsSpice software, and finally, a physical prototype, with the FPGA chip utilized as a system control kernel, is provided to demonstrate its effectiveness.

2. Proposed Converter

Figure 1 shows the proposed two-phase interleaved converter with a new zero current transition. Since this paper adopts the Interleaved PWM technique, the respective duty cycle of one phase differs by 180° from that of the other and does not overlap with each other. Accordingly, the operating principle of the single-phase circuit will be analyzed.

For analysis convenience of analyzing the proposed converter in each operating state, the following assumptions are made first: (i) The active power switch and the passive power switch are ideal; (ii) the input current is constant and the input inductance is much larger than the resonance inductance, which can be considered as a constant current source; (iii) the output voltage is fixed and the output capacitance is much larger than the resonant capacitance, so it can be regarded as a constant voltage source and (iv) Both the capacitance and inductance have no parasitic resistance.

From the above assumptions, the single-phase equivalent circuit will be shown in Figure 2.
is the current flowing through the main switch

Prior to the circuit analysis shown in Figure 2, the relevant component symbols are defined as follows: (i) $V_o$ is the output DC voltage, $v_{gm}$ is the gate signal of the main switch $S_m$, $v_{Sm}$, is the voltage on the main switch, $v_{Da}$ is the gate signal of the common-grounded auxiliary switch $S_a$, $v_{Sa}$ is the voltage on the auxiliary switch, $v_{Do}$ is the voltage on the auxiliary diode $D_o$, $v_{Do}$ is the voltage on the output diode $D_o$, and $v_{Cr}$ is the voltage on the resonant capacitor $C_r$ and (ii) $I_{in}$ is the DC current flowing through the input inductor, $i_{Sm}$ is the current flowing through the main switch $S_m$, $i_{Sa}$ is the current flowing through the auxiliary switch $S_a$, $i_{Da}$ is the current flowing through the auxiliary diode $D_a$, $i_{Do}$ is the current flowing through the output diode $D_o$, and $i_{Lr}$ is the current flowing through the resonant inductor $L_r$. The internal diode $D_{sa}$ is connected in parallel with $S_a$.

According to the on/off situation of the switching elements and the state of the energy storage elements, the main operating waveforms of the converter, shown in Figure 3, can be divided into seven over one switching cycle.
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**State 1 \(0 \leq t \leq t_1\):** As shown in Figures 3 and 4, when the time reaches \(t_0\), the main switch \(S_m\) is on and the rest of the switch elements are in the off state. At the same time, the input current \(I_{in}\) flows through \(S_m\).

![Figure 3. Main operating waveforms.](image)

![Figure 4. Current flow of state 1.](image)
According to Figure 3, the following equations can be obtained as

\[
\begin{align*}
    i_{lr}(t) &= 0 \\
    v_{cr}(t) &= v_{cr}(t_0)
\end{align*}
\]  \tag{1}

The time experienced in this state, called \( \Delta t_1 \), is

\[
\Delta t_1 = t_1 - t_0 = DT_s - \Delta t_2 - \Delta t_3 - \Delta t_4
\]  \tag{2}

where \( \Delta t_2 \) is the time experienced in state 2, \( \Delta t_3 \) is the time experienced in state 3, \( \Delta t_4 \) is the time experienced in state 4, and \( D \) is the duty cycle.

State 2 \([t_1 \leq t < t_2]\): As shown in Figures 3 and 5, when the time reaches \( t_1 \), the auxiliary switch \( S_a \) is turned on, and the output voltage \( V_o \), resonant inductor \( L_r \), and resonant capacitor \( C_r \) form a resonant circuit. At the same time, the resonant capacitor voltage \( v_{cr} \) rises gradually from \( v_{cr}(t_0) \), and the resonant inductor current \( i_{lr} \) starts to fall from zero. Once the voltage \( v_{cr} \) rises to zero, the operating state proceeds to state 3.

\[
\begin{align*}
    i_{lr}(t_1) &= 0 \\
    v_{cr}(t_1) &= v_{cr}(t_0)
\end{align*}
\]  \tag{3}

According to Figure 3, the following equations can be obtained as

\[
\begin{align*}
    i_{lr}(t) &= \frac{v_{cr}(t_0) - V_o}{Z_r} \sin \omega_r(t - t_1) \\
    v_{cr}(t) &= V_o + [v_{cr}(t_0) - V_o] \cos \omega_r(t - t_1)
\end{align*}
\]  \tag{4}

The time experienced in this state, called \( \Delta t_2 \), is

\[
\Delta t_2 = t_2 - t_1 = \frac{1}{\omega_r} \sin^{-1} \left( \frac{-Z_r i_{in}}{v_{cr}(t_0) - V_o} \right)
\]  \tag{5}

State 3 \([t_2 \leq t < t_3]\): As shown in Figures 3 and 5, when the time reaches \( t_2 \), the resonant inductor \( L_r \) and resonant capacitor \( C_r \) resonate continuously, and the resonant capacitor voltage \( v_{cr} \) rises from zero, whereas the resonant inductor current \( i_{lr} \) decreases continuously. When the resonant capacitor voltage \( v_{cr} \) is equal to the output voltage \( V_o \), the resonant inductor current \( i_{lr} \) climbs upward from the reverse peak current. Once the resonant inductor current \( i_{lr} \) climbs to zero, the operating state enters state 4.

\[
\begin{align*}
    i_{lr}(t_2) &= 0 \\
    v_{cr}(t_2) &= v_{cr}(t_0)
\end{align*}
\]  \tag{3}

According to Figure 3, the following equations can be obtained as

\[
\begin{align*}
    i_{lr}(t) &= \frac{v_{cr}(t_0) - V_o}{Z_r} \sin \omega_r(t - t_2) \\
    v_{cr}(t) &= V_o + [v_{cr}(t_0) - V_o] \cos \omega_r(t - t_2)
\end{align*}
\]  \tag{4}

The time experienced in this state, called \( \Delta t_3 \), is

\[
\Delta t_3 = t_3 - t_2 = \frac{1}{\omega_r} \sin^{-1} \left( \frac{-Z_r i_{in}}{v_{cr}(t_0) - V_o} \right)
\]  \tag{5}

State 4 \([t_3 \leq t \leq t_4]\): When the resonant capacitor voltage \( v_{cr} \) is equal to zero, and the auxiliary switch \( S_a \) is turned off. At the same time, a resonant circuit with resonant inductor \( L_r \) and resonant capacitor \( C_r \) is resonant continuously, and the resonant capacitor voltage \( v_{cr} \) decreases to zero, whereas the resonant inductor current \( i_{lr} \) increases continuously. Once the resonant inductor current \( i_{lr} \) increases to zero, the operating state enters state 4.

\[
\begin{align*}
    i_{lr}(t_3) &= 0 \\
    v_{cr}(t_3) &= v_{cr}(t_0)
\end{align*}
\]  \tag{3}

According to Figure 3, the following equations can be obtained as

\[
\begin{align*}
    i_{lr}(t) &= \frac{v_{cr}(t_0) - V_o}{Z_r} \sin \omega_r(t - t_3) \\
    v_{cr}(t) &= V_o + [v_{cr}(t_0) - V_o] \cos \omega_r(t - t_3)
\end{align*}
\]  \tag{4}

The time experienced in this state, called \( \Delta t_4 \), is

\[
\Delta t_4 = t_4 - t_3 = \frac{1}{\omega_r} \sin^{-1} \left( \frac{-Z_r i_{in}}{v_{cr}(t_0) - V_o} \right)
\]  \tag{5}
The initial conditions of this state are
\[
\begin{aligned}
    i_{Lr}(t_2) &= -I_{in} \\
    v_{Cr}(t_2) &= 0
\end{aligned}
\]  
(6)

According to Figure 3, the following equations can be obtained to be
\[
\begin{aligned}
    i_{Lr}(t) &= -I_{in} \cos \omega_r (t-t_2) - \frac{V_o}{Z_r} \sin \omega_r (t-t_2) \\
    v_{Cr}(t) &= V_o - V_o \cos \omega_r (t-t_2) + Z_r I_{in} \sin \omega_r (t-t_2)
\end{aligned}
\]  
(7)

The time experienced in this state, called \(\Delta t_3\), is
\[
\Delta t_3 = t_3 - t_2 = \frac{1}{\omega_r} \cos^{-1} \left( \frac{v_{Cr}(t_0) V_o - V_o^2}{V_o^2 + I_{in}^2 Z_r^2} \right)
\]  
(8)

State 4 \([t_3 \leq t \leq t_4]\): As shown in Figures 3 and 6, when the time reaches \(t_3\), the auxiliary switch is cut off, and the resonant inductance \(L_r\) and resonant capacitance \(C_r\) continue to resonate, making the auxiliary diode conductive. At the same time, the resonant inductance current \(i_{Lr}\) rises to the input current \(I_{in}\). As the resonant inductance current \(i_{Lr}\) rises to the input current \(I_{in}\), the main switch current \(i_{Sm}\) drops to zero. At this time, if the main switch is turned off, the ZCT of the main switch can be realized, and this state ends.

![Figure 6. Current flow of state 4.](image)

The initial conditions of this state are
\[
\begin{aligned}
    i_{Lr}(t_3) &= 0 \\
    v_{Cr}(t_3) &= 2V_o - v_{Cr}(t_0)
\end{aligned}
\]  
(9)

According to Figure 3, the following equations can be obtained as
\[
\begin{aligned}
    i_{Lr}(t) &= \frac{V_o - v_{Cr}(t_0)}{Z_r} \sin \omega_r (t-t_3) \\
    v_{Cr}(t) &= V_o + [V_o - v_{Cr}(t_0)] \cos \omega_r (t-t_3)
\end{aligned}
\]  
(10)

The time experienced in this state, called \(\Delta t_4\), is
\[
\Delta t_4 = t_4 - t_3 = \frac{1}{\omega_r} \sin^{-1} \left( \frac{Z_r I_{in}}{V_o - v_{Cr}(t_0)} \right)
\]  
(11)

State 5 \([t_4 \leq t \leq t_5]\): As shown in Figures 3 and 7, when the time reaches \(t_4\), the main switch \(S_m\) is cut off. At the same time, the resonant inductance \(L_r\) and resonant capac-
ittance $C_r$ continue to resonate. According to Kirchhoff’s current law, it can be known that $I_{in} = i_{Da} = i_{Sa} + i_{Lr}$. Since the resonant inductance current $i_{Lr}$ is greater than the input current $I_{in}$, the internal diode of the auxiliary switch, called $D_{Sa}$, is conductive. The moment the resonant inductance current $i_{Lr}$ drops to the input current $I_{in}$, the operating state enters state 6.

![Figure 7. Current flow of state 5.](image)

The initial conditions of this state are

$$\begin{align*}
i_{Lr}(t_4) &= I_{in} \\
v_{Cr}(t_4) &= V_o + V_o \cos(\omega_r \Delta t_4)
\end{align*}$$

(12)

According to Figure 3, the following equations can be obtained as

$$\begin{align*}
i_{Lr}(t) &= \frac{v_o \cos(\omega_r \Delta t_4)}{Z_r} \sin \omega_r (t - t_4) \\
&+ I_{in} \cos \omega_r (t - t_4) \\
v_{Cr}(t) &= V_o + [V_o \cos(\omega_r \Delta t_4)] \cos \omega_r (t - t_4) \\
&- Z_r I_{in} \sin \omega_r (t - t_4)
\end{align*}$$

(13)

The time experienced in this state, called $\Delta t_5$, is

$$\Delta t_5 = t_5 - t_4 = \frac{1}{\omega_r} \sin^{-1} \left( \frac{[V_o + V_o \cos(\omega_r \Delta t_4)] I_{in} Z_r}{[V_o \cos(\omega_r \Delta t_4)]^2 + I_{in}^2 Z_r^2} \right)$$

(14)

State 6 [$t_5 \leq t \leq t_6$]: As shown in Figures 3 and 8, when the time reaches $t_5$, the resonant inductor $L_r$ and resonant capacitor $C_r$ resonate continuously, thus causing the resonant inductor current $i_{Lr}$ to drop from the input current $I_{in}$. According to Kirchhoff’s current law, it can be known that $I_{in} = i_{Do} + i_{Lr}$. The resonant inductor current $i_{Lr}$ is smaller than the input current $I_{in}$, thereby making the internal diode of the auxiliary switch, called $D_{Sa}$, cut off and the output diode $D_o$ conductive. As soon as the resonant inductor current $i_{Lr}$ drops to zero, the operating state enters state 7.
According to Figure 3, the following equations can be obtained as

\[
\begin{align*}
\text{State 6:} & \quad \begin{cases} 
  i_{Lr}(t) = I_{in} \\
  v_{Cr}(t) = 0 
\end{cases} \\
\text{State 7:} & \quad \begin{cases} 
  i_{Lr}(t) = I_{in} \cos \omega_r(t - t_5) \\
  v_{Cr}(t) = -Z_r I_{in} \sin \omega_r(t - t_5) 
\end{cases} \\
\end{align*}
\]

The time experienced in this state, called \( \Delta t_6 \), is

\[
\Delta t_6 = t_6 - t_5 = \frac{1}{\omega_r} \sin^{-1} \left( \frac{-v_{Cr}(t_0)}{Z_r I_{in}} \right)
\]

State 7 \([t_5 \leq t \leq t_7]\): As shown in Figures 3 and 9, when the time reaches \( t_6 \), the resonance of resonant inductor \( L_r \) and resonant capacitor \( C_r \) is over; the resonant inductor current \( i_{Lr} \) has dropped to zero, so the auxiliary diode \( D_a \) is cut off, which is like the demagnetization state of the input inductor of the traditional boost converter.

According to Figure 3, the following equations can be obtained as

\[
\begin{align*}
\text{State 7:} & \quad \begin{cases} 
  i_{Lr}(t) = 0 \\
  v_{Cr}(t) = v_{Cr}(t_0) 
\end{cases} 
\end{align*}
\]
The time experienced in this state, called $\Delta t_6$, is

$$\Delta t_7 = t_7 - t_6 = (1 - D)T_s - \Delta t_5 - \Delta t_6$$  \hspace{1cm} (19)

3. Proposed Current Sharing Strategy

Since the proposed system uses the interleaved PWM technique, the two phases have a $180^\circ$ difference in their individual gate driving signals and do not overlap their individual duty cycles with each other. Accordingly, a new current sampling method is adopted herein. In this paper, we use a new current sampling method to obtain two-phase current signals with only one current sampling circuit, which reduces one current sampling device, one filter circuit, and one analog-to-digital converter (ADC). Figure 10 shows the proposed two-phase current sampling method, where the sampling device for the two-phase current, the main switch current of the first phase, and the main switch current of the second phase are shown. In this system, a current sampling resistor $R_c$ is connected in series with the emitters of the main switches of two phases. Based on the digital controller, the first-phase current is sampled from $t_0$ to $t_1$ time, and the second-phase current is sampled from $t_2$ to $t_3$ times so that the information of the two-phase current signals can be obtained.

**Figure 10.** Proposed sampling method: (a) Relationship between TLP250 and IGBT; (b) Relationship between two TLP250s and $R_c$.

3.1. Design of Current Sensing Resistor $R_c$

Prior to this section, the system specifications will be given as shown in Table 1.
Table 1. System specifications.

| Specification                        | Value or Condition          |
|--------------------------------------|-----------------------------|
| Input Voltage \((V_i)\)              | 250 V                       |
| Output Voltage \((V_o)\)             | 400 V                       |
| Rated Output Current \((I_{o,rated})\)/Rated Output Power \((P_{o,rated})\) | 2.5 A/1 kW                  |
| Min. Output Current \((I_{o,min})\)/Min. Output Power \((P_{o,min})\) | 0.625 A/0.25 kW             |
| Switching Frequency \((f_s)\)/Switching Period \((T_s)\) | 50 kHz/20 \(\mu s\)        |
| Operating Mode                       | Continuous Current Mode (CCM) |
| Input Inductance                     | 1.66 mH                     |
| Output Voltage Ripple                | Smaller than 0.15% of \(V_o\) |

3.1.1. Maximum Input Inductor Current

Since this converter operates in CCM from light load to rated load, the corresponding duty cycle \(D\) is shown as below:

\[
D = 1 - \frac{V_i}{V_o} = 1 - \frac{250}{400} = 0.375 \tag{20}
\]

The input inductor current ripple \(\Delta I_{Li1}\) can be obtained as follows:

\[
\Delta I_{Li1} = \frac{V_i D T_s}{L_{i1}} = \frac{250 \times 0.375 \times 20 \mu \text{H}}{1.66 \text{mH}} \approx 1.13 \text{A} \tag{21}
\]

The maximum input inductor current \(I_{Li1,max}\) can be obtained as follows:

\[
I_{Li1,max} = I_{Li1} + \frac{1}{2} \Delta I_{Li1} = 2 + \frac{1}{2} \times 1.13 \approx 2.57 \text{A} \tag{22}
\]

3.1.2. Current Sensing Resistance

Figure 10a shows the isolated gate driver TLP-250 connected between gate G after resistor \(R_2\) and emitter E of the IGBT, whereas Figure 10b shows the current sensing resistor \(R_c\) for the two phases. From these two figures, it is noted that since the low-level output voltage of the gate driver is connected to point E, the current in the gate driver does not flow through \(R_c\), which will guarantee that the IGBT works in the saturation region with \(V_{CE(sat)}\) smaller than 2.5 V, which is verified by experiment. The following will talk about how to obtain the value of \(R_c\).

Since the used current sensing resistor \(R_c\) has the loss, this loss due to \(R_c\) is set at 0.04% of the rated output power, that is, the power dissipated on \(R_c\) is 400 mW. The current, due to the gate driver, does not flow through \(R_c\) because the low-level output voltage of the gate driver is connected to point E.

According to Figure 10b, the rms value of the current flowing through \(R_c\) is

\[
I_{c,rms} = \sqrt{\frac{1}{0.5 T_s} \int_{0}^{D T_s} i_{Sm1}^2 dt} = \sqrt{2(I_{Li1,max}^2 - 2I_{Li1,max}^2 D + \frac{2}{3} \Delta I_{Li1}^2 D)} = 3.935 \text{A} \tag{23}
\]

Based on (23), two 0.1 Ω resistors connected in parallel are used as the current sensing resistor, where each resistor has a power dissipation of 200 mW, corresponding to the prescribed power dissipation. Since the maximum current flowing through \(R_c\) is equal to \(I_{Li1,max}\), the maximum voltage on \(R_c\) is 0.1285 V. In addition, the maximum input voltage of the ADC is 5 V. Therefore, the voltage gain of the differential amplifier is set at 20, and hence, the ratio of voltage to current is 1 V/1 A and the maximum voltage on \(R_c\) is 2.57 V, corresponding to the ADC requirement.
3.1.3. Current Sharing Controller

In this paper, the average current method is used to make the input current evenly distributed between the two phases, as shown in Figure 11. For the average current method to be considered, the sampled current signals of two phases are averaged to generate the current sharing reference command $I_{ref}$. Sequentially, each phase current is subtracted from this reference command to generate the current error signal and then feeds this error signal to the corresponding current sharing compensator to obtain the required control force. After this, this control force is added with the voltage control force created from the voltage compensator to control the corresponding switch of each phase, so that current sharing, as well as output voltage stabilization, can be achieved.

![Figure 11. Block diagrams of the average current method.](image)

4. Design of Resonant Components

This section introduces the resonant component design according to the given system specifications, the resonant inductors and resonant capacitors of two phases are designed. The system specifications are shown in Table 1. First, the on-time of the auxiliary switch should be given, and after this, the values of the resonant components will be calculated under the rated condition as the worst condition. Accordingly, the ZCT operation under the light condition can be guaranteed, and this can be verified by measured waveforms, to be seen later.

From Sec. 2, the turn-on time of the auxiliary switch is used to determine the resonance time. If the auxiliary switch conduction time is too long, it is easy to cause an excessive increase in conduction loss, whereas if the turn-on time of the auxiliary switch is less than the sum of the cut-off delay time $T_{d(off)}$ and falling time $T_f$ of the IGBT, the resonance inductor $L_r$ and the resonance capacitor $C_r$ will resonate several times and affect the operation of the auxiliary circuit. According to Figure 12, the on-time of the auxiliary switch must be greater than the sum of $T_{d(off)}$ and $T_f$. Therefore, to reduce the effect of the resonance frequency on PWM switching, the resonance period is set between 0.05 times the switching period and 0.1 times the switching period, that is, the resonance period locates between 1 $\mu$s and 2 $\mu$s, so the turn-on time of the auxiliary switch is taken as 1.5 $\mu$s.
Therefore, the peak current of the resonant inductor must be larger than the peak current of the input inductor, and the resonant impedance can be obtained as

\[
2I_{Li1,max} = \frac{V_o - v_{Cr}(t_0)}{Z_r} \Rightarrow Z_r = \frac{V_o - v_{Cr}(t_0)}{2I_{Li1,max}}
\]  

(25)

As shown in Figure 3, the following equation can be approximately obtained to be

\[
\frac{v_{Cr}(t_0)}{Z_r I_{Li1,max}} = \frac{Z_r I_{Li1,max}}{v_{Cr}(t_0) - V_o}
\]  

(26)

Substituting (22) and (25) into (26) yields the initial resonant capacitance across the voltage as

\[
v_{Cr}(t_0) = \frac{6V_o - \sqrt{36V_o^2 + 12V_o^2}}{6} = -62V
\]  

(27)

By substituting (25) into (26) and (27), the values of the resonant inductor and resonant capacitor can be obtained to be

\[
\begin{align*}
L_r &= \frac{Z_r}{\omega r} \approx 40\mu H \\
C_r &= \frac{1}{\omega r Z_r} \approx 5nF
\end{align*}
\]  

(28)

As shown in Figure 3, the maximum voltage across the resonant capacitor is \(2V_o - v_{Cr}(t_0)\), i.e., 862 V. Therefore, the resonant capacitor takes a 1.5 kV Mylar capacitor, and the resonant inductor adopts a Sendust core manufactured by CHANGSUNG, with the model number CS270125, 18 turns, and the wire diameter No. 16 AWG.

5. System Configuration

In Figure 13, the main power stage is composed of a two-phase interleaved step-up converter with a ZCT auxiliary circuit, whereas the peripheral circuit includes a gate driver circuit, a voltage sampling circuit, a two-phase current sampling circuit and an analog-to-digital converter; in the controller, the FPGA is used as the control kernel to realize the fully digital interleaved PWM control. The Cyclone II series FPGA chip, manufactured by Altera Co., has a product number of EP2C20F484C8.
6. Simulated and Experimental Results and Discussions

6.1. Simulated and Measured Waveforms

The simulation shown in Figure 14 is based on the IsSpice software. In the following, the simulated and experimental results are obtained at rated load. Moreover, in Table 2, the part numbers used for the switches and diodes in the simulation and experiment can be configured according to the system specifications and the main operating waveforms.

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**Figure 13.** System circuit configuration.

**Figure 14.** IsSpice simulation of the proposed circuit with selected component models and parameters.
Table 2. Part numbers used for the switches and diodes on simulation and experiment.

| Switch and Diode | Part Number |
|------------------|-------------|
| **Simulation**   |             |
| Main Switches $S_{m1}$ and $S_{m2}$ | STGP10NC60H |
| Aux. Switches $S_{a1}$ and $S_{a2}$ | STGP10NC60HD |
| Output Diodes $D_{o1}$ and $D_{o2}$ | IN3903 |
| Aux. Diodes $D_{a1}$ and $D_{a2}$ | IN3903 |
| **Experiment**   |             |
| Main Switches $S_{m1}$ and $S_{m2}$ | MGM5N50 |
| Aux. Switches $S_{a1}$ and $S_{a2}$ | SKM25GB |
| Output Diodes $D_{o1}$ and $D_{o2}$ | BYV29 |
| Aux. Diodes $D_{a1}$ and $D_{a2}$ | BYV29 |

Figure 15 shows the gate driving signals for main switches $v_{gm1}$ and $v_{gm2}$, and auxiliary switches $v_{ga1}$ and $v_{ga2}$. Figure 16 shows the gate driving signal for the phase-1 main switch $S_{m1}$, called $v_{gm1}$, the voltage across $S_{m1}$, called $v_{Sm1}$, and the current flowing through $S_{m1}$, called $i_{Sm1}$. Figure 17 shows the zoom-in of Figure 16. Figure 18 shows the gate driving signal for the phase-1 auxiliary switch $S_{a1}$, called $v_{ga1}$, the voltage across $S_{a1}$, called $v_{Sa1}$, and the current flowing through $S_{a1}$, called $i_{Sa1}$. Figure 19 shows the zoom-in of Figure 18. Figure 20 shows the voltage on the resonant capacitor, called $v_{Cr1}$, and the current flowing through the resonant inductor, called $i_{Lr1}$.

![Figure 15](image1.png)

**Figure 15.** Waveforms relevant to gate driving signals: (1) $v_{gm1}$; (2) $v_{ga1}$; (3) $v_{gm2}$; (4) $v_{ga2}$ for (a) simulation and (b) experiment.

![Figure 16](image2.png)

**Figure 16.** Waveforms relevant to $S_{m1}$: (1) $v_{gm1}$; (2) $v_{Sm1}$; (3) $i_{Sm1}$ for (a) simulation and (b) experiment.
Figure 17. Zoom-in of Figure 17: (1) $v_{gm1}$; (2) $v_{Sm1}$; (3) $i_{Sm1}$ for (a) simulation and (b) experiment.

Figure 18. Waveforms relevant to $S_{a1}$: (1) $v_{ga1}$; (2) $v_{Sa1}$; (3) $i_{Sa1}$ for (a) simulation and (b) experiment.

Figure 19. Zoom-in of Figure 19: (1) $v_{ga1}$; (2) $v_{Sa1}$; (3) $i_{Sa1}$ for (a) simulation and (b) experiment.
Figure 20. Waveforms relevant to $C_1$ and $L_1$: (1) $v_{C1}$; (2) $i_{L1}$ for (a) simulation and (b) experiment.

Figure 21 shows the gate driving signal for the phase-2 main switch $S_{m2}$, called $v_{gm2}$, the voltage across $S_{m2}$, called $v_{Sm2}$, and the current flowing through $S_{m2}$, called $i_{Sm2}$. Figure 22 shows the zoom-in of Figure 21. Figure 23 shows the gate driving signal for the phase-2 auxiliary switch $S_{a2}$, called $v_{Sa2}$, the voltage across $S_{a2}$, called $v_{Sm2}$, and the current flowing through $S_{a2}$, called $i_{Sm2}$. Figure 24 shows the zoom-in of Figure 23. Figure 25 shows the voltage on the resonant capacitor, called $v_{Cr2}$, and the current flowing through the resonant inductor, called $i_{Lr2}$. Figure 26 shows the gate driving signals $v_{gm1}$ and $v_{Sm1}$, and the resonant inductor currents $i_{Lr1}$ and $i_{Lr2}$.

Figure 21. Waveforms relevant to $S_{m2}$: (1) $v_{gm2}$; (2) $v_{Sm2}$; (3) $i_{Sm2}$ for (a) simulation and (b) experiment.

Figure 22. Zoom-in of Figure 23: (1) $v_{gm2}$; (2) $v_{Sm2}$; (3) $i_{Sm2}$ for (a) simulation and (b) experiment.
Figure 23. Waveforms relevant to $S_{a2}$: (1) $v_{gm2}$; (2) $v_{Sm2}$; (3) $i_{Sm2}$ for (a) simulation and (b) experiment.

Figure 24. Zoom-in: (1) $v_{gm2}$; (2) $v_{Sm2}$; (3) $i_{Sm2}$ for (a) simulation and (b) experiment.

Figure 25. Waveforms relevant to $C_{r2}$ and $L_{r2}$: (1) $v_{C_{r2}}$; (2) $i_{L_{r2}}$ for (a) simulation and (b) experiment.
Figure 26. Waveforms relevant to $L_1$ and $L_2$: (1) $v_{gm1}$; (2) $v_{gm2}$; (3) $i_{L1}$; (4) $i_{L2}$ for (a) simulation and (b) experiment.

6.2. Waveform Comments

The simulated and experimental results are similar to some extent except for oscillation. From Figure 15, $v_{gm2}$ is shifted by 180 degrees from $v_{gm1}$ whereas $v_{oa2}$ is shifted by 180 degrees from $v_{oa1}$. Figure 17 shows $S_m1$ has turn-off ZCT. Figure 19 shows $v_{Sa1}$ and $i_{Li1}$, corresponding to near ZCS. Figure 20 shows $v_{Cr1}$ and $i_{Li1}$, also corresponding to Figure 3. Figure 22 shows $S_m2$ has turn-off ZCT. Figure 24 shows $v_{Sa2}$ and $i_{Li2}$, corresponding to near ZCS. Figure 25 shows $v_{Cr2}$ and $i_{Li2}$, also corresponding to Figure 3. Figure 26 shows $i_{L2}$ is shifted by 180 degrees from $i_{L1}$, the average values of the two currents are almost the same, meaning that the output current is almost distributed between the two phases.

In Figure 16 or Figure 21, there are four phenomena to be described. One is the current spike in $i_{Sm1}$ or $i_{Sm2}$ is due to the reverse recovery current of $D_{a1}$ or $D_{a1}$, and the voltage $v_{Sm1}$ or $v_{Sm2}$ during the turn-on period is smaller than the maximum on-voltage drop $V_{CE(sat)}$ of 2.5 V based on the STGPI0NC60H datasheet, thereby making sure that $S_m1$ or $S_m2$ are operated in the saturation region. Another is that $i_{Sm1}$ or $i_{Sm2}$ will have a small increase when the voltage across $S_m1$ or $S_m2$ rises since the IGBT needs time to withdraw injected carriers at the emitter of the IGBT during the turn-off period. The other is that as $S_a1$ or $S_a2$ is on instantaneously, the corresponding $D_{a1}$ or $D_{a2}$ is on, so some of the currents in $S_m1$ or $S_m2$ will be shifted to $S_a1$ or $S_a2$, resulting in a current dip in current $i_{Sm1}$ or $i_{Sm2}$.

In Figure 18 or Figure 23, there are two ringing voltages on $v_{Sa1}$ or $v_{Sa2}$ to be described. One is that since the reverse recovery current of $D_{sa1}$ or $D_{sa2}$ will flow to the resonant path, the first ringing voltage on $v_{Sa1}$ or $v_{Sa2}$ will occur. The other is when $S_m1$ or $S_m2$ turn on instantaneously, the reverse recovery current of $D_{a1}$ or $D_{a2}$ will flow to the resonant path through $D_{sa1}$ or $D_{sa2}$, so the second ringing voltage on $v_{Sa1}$ or $v_{Sa2}$ will occur.

In Figure 20 or Figure 25, the peak value of the resonant inductor current is smaller than the designed value due to the presence of parasitic resistance in the actual circuit, and the peak value of the resonant capacitor voltage is larger than the designed value due to the tolerance of the resonant capacitance. From Figure 27, it is noted that at light load, the main switches $S_m1$ and $S_m2$ still have ZCT turn-off, corresponding to the requirements.
6.3. Light-Load Efficiency Improvement

Figure 27 shows the waveforms of $S_{a1}$ under 25% load by not adjusting the on-time and off-triggering moment of $S_{a1}$. As can be seen from this figure, when the proposed converter is operated under a light load, the current flowing through $D_{a1}$ is larger than that under a rated load. Therefore, the reverse recovery current of this diode is larger than that under a rated load, so a voltage spike on $S_{a1}$ is likely to be caused. Figure 28 shows the waveforms of $S_{a1}$ under 25% load by adjusting the on-time and off-triggering moment of $S_{a1}$. The peak value of the voltage spike will be reduced from 620 V to 460 V, thereby making the light-load efficiency improved. This description can be applied to phase-2 $S_{a2}$.

Figure 28. Waveforms related to phase-1 $S_{a1}$ under 25% load without the on-time and off-triggering moment of $S_{a1}$ adjusted: (1) $v_{g_{a1}}$; (2) $v_{S_{a1}}$; (3) $i_{S_{a1}}$. 

Figure 27. Waveforms under 25% load: (1) $v_{g_{m1}}$; (2) $v_{S_{m1}}$; (3) $i_{S_{m1}}$ for (a) $S_{m1}$; (1) $v_{g_{m2}}$; (2) $v_{S_{m2}}$; (3) $i_{S_{m2}}$ for (b) $S_{m2}$. 

[Diagrams of waveforms showing voltage and current waveforms at different loads and illustrating the efficiency improvement process.]
6.4. Efficiency Measurement

Figure 30 shows the efficiency measurement block diagram. From this figure, a current sampling resistor is connected in series with the input current path. The input current and input voltage are multiplied to obtain the input power. To measure the output power, an electronic load, named Prodigit 3254, is used to provide the required load current, and a digital voltmeter, named Fluke 8050 A, is used to measure the output voltage, which is multiplied by the load current to obtain the output power. Eventually, the output power at each load is divided by the corresponding input power to obtain a curve of efficiency versus load current shown in Figure 31. In Figure 31, there are three cases to be compared. Case 1 has the ZVT turn-on without the on-time and the off-triggering instant of $S_{a1}$ and $S_{a2}$ adjusted. Case 2 has the ZVT turn-on with the on-time and the off-triggering instant of $S_{a1}$ and $S_{a2}$ adjusted. Case 3 has no ZVT. From this figure, Case 2 has better light-load efficiency than the other two. The rated load efficiencies for Case 1, Case 2 and Case 3 are 96.3%, 96.4% and 94.8%, respectively. Since the power loss relevant to the tail current is quite difficult to estimate [24], we use the rated-load efficiencies for Case 3 and Case 1 to figure out the individual power losses of 54.8 W and 38.4 W, respectively, and then the power loss associated to the falling current can be approximately estimated out by the difference in power loss between these two cases, equal to 16.4 W.

**Figure 29.** Waveforms related to phase-1 $S_{a1}$ under 25% load with the on-time and off-triggering moment of $S_{a1}$ adjusted: (1) $v_{g1}$; (2) $v_{g2}$; (3) $i_{g1}$.

**Figure 30.** Efficiency measurement block diagram.
6.5. Comparison between the Existing and the Proposed

In Table 3, the literature [14] has the least number of main switches, and the main switches have a hard turn-on and ZCS turn-off; however, the main switches will have large current stresses when they are turned off. In [9], the main switches have a large voltage spike when they are turned off. Additionally, although the auxiliary switches have turn-off ZVS and ZCS, they are turned off with higher voltage surges so that the components with higher voltage withstand are needed. The output diode, although it has a turn-on near ZCS and turn-off ZVZCS in [9], there are high resonance voltages and resonance currents, resulting in the need for a higher voltage and current-withstanding components for the output diode. The auxiliary diode has a soft switching function in every literature except for [14]. The maximum efficiency is the highest in [13]; however, the average efficiency of [13] is not the highest. Although the maximum efficiency of the proposed circuit is not the highest, its average efficiency has been improved by using an auto-tuning technique, and hence the practicality of this circuit has been greatly increased.

Table 3. Comparison of the existing and the proposed.

| Ref. | Switch | Main Switch | Aux. Switch | Output Diode | Aux. Diode | Max. Eff. |
|------|--------|-------------|-------------|--------------|------------|----------|
| [9]  | 4      | Hard ZCS   | Near ZCS ZVS ZCS ZVS ZCS ZVS ZVS ZVS Near ZCS | -           | -          | 96.7%    |
| [13] | 4      | Hard ZCS   | Near ZCS ZCS ZCS Hard Hard Near ZCS | -           | -          | 98.5%    |
| [14] | 3      | Hard ZCS   | Near ZCS ZCS ZVS ZCS ZCS - - ZVS Near ZCS | -           | -          | 92.2%    |
| [15] | 4      | Hard ZCS   | Near ZCS ZCS Near ZCS Near ZCS ZCS ZVS | -           | -          | 95.5%    |
| [16] | 6      | Hard ZCS   | Near ZCS ZCS Near ZCS Near ZCS Near ZVSNear ZCS ZCS ZVS Near ZCS | -           | -          | 97.6%    |
| [17] | 4      | Hard ZCS   | Near ZCS ZCS Near ZCS Near ZCS ZCS ZVS ZCS ZVS Near ZCS | -           | -          | 98%      |
| Proposed | 4 | Hard ZCS   | Near ZCS ZCS Near ZCS Hard ZVS Near ZCS | -           | -          | 96.4%    |

7. Conclusions

This paper proposes a fully digital multiphase interleaved boost converter with a fixed-frequency ZCT. The proposed auxiliary circuits used to realize the ZCT with the common-grounded auxiliary switches are added to the traditional boost converter to reduce the switching loss caused by the hard switching of IGBTs. In addition, the overall efficiency of the converter can be improved by adjusting the on-time and off-trigger times of the auxiliary switch. Furthermore, a current-sharing control along with a two-phase interleaved control is used to distribute the input current evenly among the phases. In addition, a new current sampling method is used, which requires only one sampling circuit to simultaneously return the current signals of the two-phase main switches. Above all, the number of phases can be extended, still possessing easy control of the ZCT and current sharing.
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