A design of flash analog-to-digital converter in 180 nm CMOS process with high effective number of bits

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Abstract. High speed flash analog-to-digital converters are used in modern high-performance telecommunication systems. Furthermore, high effective resolution of such converter should be provided. The paper presents a design of a flash analog-to-digital converter with high effective number of bits. As an example, the 8-bit flash ADC in 180 nm CMOS has been implemented. Simulation confirms efficiency of proposed design. The effective resolution of presented design achieves 6.9 bits.

1. Introduction
Increasing of data processing rate is one of the main issues of modern telecommunication system design. Analog-to-digital converters (ADC) are an essential part of digital signal processing unit in modern high-performance telecommunication systems [1, 2, 3]. Flash ADCs have the highest conversion rate compare to other converter types and has no alternatives in applications with sampling rate around 1 GS/s and higher. Practical resolution of the flash converters does not exceed eight bits due to exponential increasing of the number of elements. If such converter provides high effective number of bits the design of a digital processing unit could be simplified.

The common flash analog-to-digital converter consists of the following parts: sample-and-hold device, analog part, digital part and output flip-flops. Sample-and-hold device stores input analog signal during conversion. The analog part consists of a comparator array and a resistor string. The signal from sample-and-hold device is directly simultaneously compared with a set of reference voltages, generated by the resistor string. If the compared signal level exceeds the corresponding reference voltage level, the logical one appears at the comparator output. Otherwise, logical zero will be set at the output of the corresponding comparator. The thermometer code is formed at the output of the comparator array and passed to the digital part. The digital part of the flash ADC is a thermometer-to-binary encoder. The output flip-flops provide synchronization with the subsequent devices of digital processing unit.

Non-idealities, such as circuit component mismatches, lead to loss in effective number of bits of analog-to-digital converters [4]. Effective resolution of the flash ADC is basically decreased due to comparator offsets and bubble errors occurred in the thermometer code. Using array of redundant comparators allows to suppress influence of these effects on the effective number of bits.

2. Proposed ADC architecture
The sample-and-hold device consists of a CMOS switch and capacitance to store input signal level. The switch using in presented ADC design is shown in figure 1 [5]. Additional transistors M1, M3,
M4, M6 are used to compensate leakage of the clock pulses to the signal processing circuit through the parasitic capacitance of M2 and M5.

The analog part architecture of the proposed ADC is based on using the array of redundant comparators [1]. As shown in [6], for 6-bit flash ADC with three comparators per bit median loss in effective resolution is about 0.4 bit. A further increase in the number of comparators reduces loss no more than by 0.1 bit. Therefore, in this work three comparators and majority element (figure 2) are used to represent each bit in thermometer code at the output of comparator array instead of single comparator in conventional flash ADC. Such approach allows to decrease comparator offsets and use simple comparators. Signals from comparator outputs are passed to the majority element. The output signal of majority element is the logical one, if output signals of two or more comparators are nonzero and the logical zero in other cases.

![Figure 1. Switch used in sample-and-hold device.](image1)

![Figure 2. Block of three comparators and majority element.](image2)

Proposed comparator circuit is shown in figure 3. Gates of transistors M5 and M6 are connected to supply voltage for operation in the saturation mode. The additional transistor in the current source allows increasing the linearity of ADC conversion curve and extension of input voltage range.

The encoder converts the thermometer code from the comparator array into the binary code. The ROM-based [1, 7, 8] architecture is the fastest one among encoder architectures. Furthermore, conversion rate could be increased with modified ROM-based circuit, which uses the input bits numbers and based on \(a \cdot \overline{b}\) logical element and NAND in the least significant bit [8]. Instead of common thermometer-to-one-hot encoder the modified array of logical elements \(a \cdot \overline{b}\) is used to generate intermediate signals \(Z_i\). The example of 3-bit thermometer-to-binary encoder with proposed architecture is presented in figure 4.

![Figure 3. Comparator.](image3)

![Figure 4. 3-bit encoder.](image4)
The least significant bit $Y_{N-1}$ of $N$-bit encoder depends only on the odd intermediate signals $Z_k$ as

$$Y_{N-1} = \sum_{k=0}^{N-1} Z_{2k+1}$$  \hspace{1cm} (1)

The next output bit $Y_{N-2}$ depends only on intermediate code bits $Z_k$, that are multiples of two. The value on $Y_{N-1}$ depends on intermediate code bits that are multiples of 2'.

$$Y_{N-1-i} = \sum_{k=1}^{i} Z_{2k}$$  \hspace{1cm} (2)

Intermediate code values $Z_k$ are obtained from the input thermometer code bits $X_j$ as

$$Z_{2^{N-1}-1} = X_{2^{N-1}-1}$$  \hspace{1cm} (3)

$$Z_{2k} = X_{2k} \cdot \overline{X_{2k+2}}$$  \hspace{1cm} (4)

$$Z_{2k+1} = X_{2k+1} \cdot \overline{X_k}$$  \hspace{1cm} (5)

Where $K$ is the number of the nearest to $X_j$ even signal, located on the higher-order bit of the output code or the logical zero, if there is no such $X$. For example, intermediate signal $Z_{252}$ has no even signal, located on the higher order bit, i.e. $Y4 - Y0$. So $X_k = 0$ and $Z_{252} = X_{252}$. The $X_{252}$ is the nearest even signal, located on higher order bit $Y5$ for $Z_{250}$ located on bit $Y6$. Therefore, according to equation (5), $Z_{250} = X_{250} \cdot \overline{X_{252}}$. Example of switch placement for even intermediate signals of 8-bit encoder and appropriate equations is presented in figure 5.

Output flip-flop circuit is based on pass-through transistors and logical inverters (figure 6).

**Figure 5.** Example of switch placement for 8-bit encoder with equations for intermediate signals.

**Figure 6.** Flip-flop circuit.
3. ADC simulation
The proposed 8-bit flash ADC has been simulated using CAD Cadence Virtuoso for 180 nm CMOS with supply voltage 1.8 V. The ADC conversion curve is presented in figure 7. The conversion curve increases monotonically and has no missing codes. The difference between calculated and simulated upper and lower bounds is no more than 1 LSB. The maximum conversion rate of the proposed ADC is 900 MS/s, average power consumption – 42 mW. The proposed ADC achieves effective resolution 6.9 bits. Integral nonlinearity (INL) is no more than 0.9 bit. The value of differential nonlinearity is 0.03 bit. The main ADC parameters in comparison with known analogs are presented in Table 1.

![Figure 7. ADC conversion curve.](image)

### Table 1. Comparison with previously published results.

| Parameter          | Value |
|--------------------|-------|
| This work          |       |
| Technology, nm     | 180   |
| Resolution, bit    | 8     |
| Power, mW          | 42    |
| Performance, GS/S  | 0.9   |
| INL, bit           | 0.9   |
| DNL, bit           | 0.03  |
| ENOB, bit          | 6.9   |

| Parameter          | This work | [1] | [9] | [10] | [11] |
|--------------------|-----------|-----|-----|------|------|
| Technology, nm     | 180       | 90  | 65  | 65   | 90   |
| Resolution, bit    | 8         | 8   | 8   | 7    | 8    |
| Power, mW          | 42        | -   | 21  | 20.7 | 207  |
| Performance, GS/S  | 0.9       | 0.65| 2   | 2    | 1.25 |
| INL, bit           | 0.9       | 3.1 | 0.61| 0.64 | 1.1  |
| DNL, bit           | 0.03      | 0.05| 0.14| 0.58 | 1.3  |
| ENOB, bit          | 6.9       | 6.8 | 6.5 | 6.04 | 6.9  |

4. Conclusions
The design of 8-bit flash analog-to-digital converter in 180 nm CMOS with high effective number of bits has been presented. The proposed ADC implementation in various CMOS technologies shows low
loss in effective resolution and low differential nonlinearity. In comparison with known results presented ADC has the lowest DNL while loss in effective number of bits is almost the same. Such results are obtained due to using the array of redundant comparators with three comparators per bit. This allows to decrease comparator offsets and use simple comparator circuit.

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