Abstract: This paper projects a high performance decoupled current control using a dq synchronous reference frame for single-phase inverter. For the three-phase inverter the conversion from AC to DC with Proportional Integral controller grants to obtain steady state error for AC Voltages and currents but has a few challenges with the single-phase systems. Hence, an orthogonal pair (β) is created by shifting the phase by one quarter cycle with respect to the real component (α) which is needed for the transformation from stationary to rotating frame. The synchronous reference frame control theory helps in controlling the AC voltage by using DC signal as the reference with the proportional integral controllers. The implementation of the control is done with two-stage converter with LCL filter for a single-phase photovoltaic system. A modified MPPT Incremental conductance algorithm along with decoupled current control helps in regulating the active and reactive power infused into the grid where the power factor is improved, the efficiency of the system is increased above 95% and total harmonic distortion for current is also reduced to 3%. The results have been validated using MATLAB.

Keywords- Photovoltaic(PV), boost converter, Maximum Power Point Tracking (MPPT), Maximum Power Point (MPP), Incremental conductance (IC), dq Synchronous Reference Frame (SRF), Phase Shifted Pulse Width Modulation (PSPWM), Phase locked loop (PLL), Total Harmonic Distortion (THD).

1. INTRODUCTION

Presently, worldwide infrastructure of electrical system is going through a major change, due to increase in the electrical energy demand, politics in energy systems, issues due to environmental conditions and an accelerated technological improvement, exclusively in power electronics sectors [1]. Rising count of renewable sources is the key to forthcoming worldwide viability. Increasing in number of distributed generators and renewable sources needed new technologies for the development of the grid in order to improve the reliability of the power supply and power quality [2]. The power electronics strategy performs an extensive aspect in combination of renewable sources to grid and in distribution generation[3].

For integrating utility grid along with the renewable resources, converters using two-stages are adopted. The first stage is DC-DC converter system for photovoltaics. Usually, this stage operates with MPPT and the input voltage gets boosted to an applicable level for the next stage. There are several maximum power point algorithm techniques [4-6].Among several types of MPPT perturb and observe algorithm and IC methods are more regularly used[7]. P&O logic is often used because of its simplicity; one drawback it has is several oscillations around the maximum power point. So IC algorithm is superior exclusively in fast changing environmental circumstances. IC algorithm can precisely track the maximum power point, with fewer oscillations and quicker response thus efficiency of the tracking is improved [8-10]. In extension, many alterations to variable step size is incorporated in the IC algorithm to achieve greater efficiency towards the MPP [11-13]. Step up converters are used to obtain regulated voltage output from an unregulated dc voltage input [14-16]. Where the input source can be taken from renewable resources such as PV system. The primary function of the later stage is an inverter for most of the systems is to assure that the maximum power obtained has to be injected into the grid smoothly and stably with quality power.

Multilevel inverter topology is one of the main attractive systems because of their extension of voltage to a higher value and for greater power.CHBMLI is more suitable where dc voltage sources are available separately and suitable for applications like photovoltaic, batteries and fuel cells[17-19]. To enrich the contents of harmonics of single-phase inverter using multilevel topologies, a fewer modulation techniques are discussed as in [20-23]. PLL for synchronizing with grid for a current control strategy is a very big endeavour. Several types of PLL is explained as in [24]. The closed loop control strategy using dq synchronous frame for three phase system is well matured in research section[25&26]. Using single-phasesystem, it is a challenging task to generate error at zero steady state. Hence, single-phase inverter current generates an orthogonal pair[27&28]. As synchronous reference, frame regulators operate on dc quantities it has better improvement than stationary reference frame regulators so that it removes steady state error and generates better transient response and has the potential of transmitting active and reactive power[29]. A filter is required between grid and the inverter to smoothen the waveform.

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A DQ Synchronous Reference Frame Current Control for Grid Connected Photovoltaic Systems using Single Phase Cascaded H Bridge Multilevel Inverter

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LCL filter is treated as a better choice when compared with respect to L and LC filter due to its design compactness and cost effective [30-32]. The transformer less inverter, for the grid connected system provide the better cost benefit and also reaches the better efficiency [33-35].

In this paper, the interfacing between the PV system and grid is shown along with two stage converter. The first stage is boost converter. Pulse for boost converter switch is generated using modified IC algorithm, with this algorithm the steady state response is very fast. The second stage is the inverter where a closed loop using dq SRFControl strategy for single-phase system with filter is adopted for grid photovoltaic system. It is implemented using a PI controller. The pulses for the inverter switches are given using the modified PSPWM method. The simulation is verified using MATLAB tool. Efficiency of proposed work in simulation is about 97% and THD is 3% for grid current, which satisfies the IEEE standard grid current value.

II. SCHEMATIC REPRESENTATION OF THE PROPOSED SYSTEM

![Fig. 1. Block diagram of single-phase SRF current control using CHBMLI](image)

Proposed systems consist of dual stages, for renewable sources integration with grid-connected system. This system has four control strategies. The first control method is IC algorithm, a modified algorithm is adopted in this paper in order to track MPP and to generate pulse for first stage dc-dc boost converter switch. Secondly modified PSPWM [23] is adopted to generate pulses for inverter. Thirdly LCL filter is to reduce the THD. Finally, current taken from filter output and grid voltages given to dq SRF current controller method through PLL to develop sine wave, a reference signal and pulses are created by comparing with carrier signals for CHBMLI switches. PLL is mainly used to control frequency and to synchronise the phase for the proposed system with grid. The block diagram is shown in Fig 1.

III. Control Techniques for the suggested system

Proposed model is detailed with two-stage inverter. Input source is taken from solar and its maximum power is tracked using modified variable IC algorithm. The pulses generated by this are applied to first stage of boost converter switch. Second stage is CHBML, output of this inverter is connected to LCL filter for reducing harmonic contents. A closed loop current control using d-q SRF is adopted and a sine reference wave is generated which is then compared with carrier waves of PSPWM and the developed pulses are given to the inverter switches.

A. Modified IC algorithm

The algorithm is developed using variable step size IC method. Proposed algorithm depends only on the transformation in the power of PV. Where ΔP/ΔV=0 reaches at the MPP as in expressions in conventional model. Proposed flowchart is illustrated in Fig.2. In modified algorithm Δd_{max} with some constant value is fixed based on the duty cycle. If Δd is higher than that of the Δd_{max} then Δd should be equaling to Δd_{max} else Δd=Δd+Δd_{max} then the algorithm follows with ΔV=0 as in conventional IC. Direct control logic is used, hence PI is needed to sustain MPP, which depends only with respect to power change as in [13].

\[
\Delta d = N|\Delta P|
\]  

\[(1)\]

![Fig. 2. Flowchart for Modified IC algorithm](image)
$N$ states the scaling factor, which maintains the step-size to accord at intervals of the tracking certainty and its convergence speed. Excluding the denominator by $\Delta V$ in the proposed technique makes the algorithm simpler and also tracks the maximum power and gives improved efficiency. Parameter values for PV panel used is detailed in Table 1.

| Components                  | Values for PV Model |
|-----------------------------|---------------------|
| Current at Short Circuit ($I_{DC}$) | 8.7 A               |
| Current at the Maximum ($I_{mpp}$) | 8.2 A               |
| Maximum Power ($P_{max}$) | 150.88 W            |
| Series Cells               | 60                  |
| Voltage at the Maximum ($V_{mpp}$) | 18.4 A             |
| Voltage at Open Circuit ($V_{oc}$) | 22.8 V         |

(a) Designing of PV dc link:

This acts as a load-balancing device. This helps by securing the inverter circuit from temporary electromagnetic interference, voltage spikes and surges. DC link capacitor is an important necessary element to accomplish the improved performance of the system. DC link is calculated using the expression (2).

$$C_{pv} = \frac{V_{pv} \times D}{4 \times L_{dc} \times \Delta V_{pv} \times f_{dc}^2}$$ (2)

Where, $V_{pv}$ is the PV voltage used in this system. D, duty cycle of boost converter. $L_{dc}$ is converter-inductor value. $\Delta V_{pv}$ is 2% of the PV voltage. $f_{dc}$ is converter frequency.

B. Designing of step up converter

In this paper dc-dc boost converter is utilized and the gating pulse for the switch is generated from IC algorithm where the maximum power is tracked. Step up converter is illustrated in Fig. 3.

![Fig. 3. Circuit diagram of step up Converter](image)

Duty cycle (D) is calculated as shown in the below expression[14-16]

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - D}$$ (3)

The boost converter inductor value is calculated using the expression (4)

$$L = \frac{(V_{IN}) \times D}{(\Delta I_{L}) \times f}$$ (4)

The capacitance value is calculated by

$$C = \frac{(V_{OUT}) \times D}{(AV_{OUT}) \times f \times R_{Load}}$$ (5)

$R_{Load}$ is calculated using $(V_{OUT})^2 / P_{IN}$

Where, the $I_{IN}$ is 8.2A, $V_{IN}$ is 18.4V, $P_{IN}$ is 150.88W. The Calculated $L$ is 260µH, $C$ is 52µF, $\Delta I_{L}$ is assumed 40% and $\Delta V_{OUT}$ is assumed 1%. The $R_{Load}$ is 80.2Ω.

(a) Designing of inverter dc link:

Capacitor in between converter and inverter is determined using expression (6).

$$C_{dc} = \frac{P_{MAX}}{2 \times \omega_{grid} \times v_{ripple} \times V_{dc}}$$ (6)

here, $P_{MAX}$ is output maximum power of boost converter for each PV, $f_s$ is the switching frequency, $v_{ripple}$ represents the amplitude of MPP voltage and it is considered to be less than 6% of the voltage MPP and for the proposed system it is considered as 2.5%. $V_{dc}$ is voltage output of boost converter, and ‘$\omega_{grid}$’ is grid frequency. The calculated $C_{dc}$ value is 4748 µF.

C. Multilevel Inverter (CHBMLI)

In medium and high power applications, Cascaded H Bridge (CHBMLI) multilevel inverter plays a vital role. This resides number of series H Bridges, each h bridge is connected with separate DC source. Renewable resources such as solar, fuel cells, battery can be replaced instead of each DC source. Seven levels incorporated in this paper. The levels are calculated with expression $2N+1$. Here $N$ denotes the number of levels. This arises with seven different output voltages such as $+3V_{dc}, +2V_{dc}, +1V_{dc}, 0, -1V_{dc}, -2V_{dc}$, and $-3V_{dc}$. CHBMLI seven level is illustrated in Fig. 4. PV source is used as an input DC source. The switching pattern is shown in Table II.

![Fig. 4. Circuit Diagram of CHBMLI with grid](image)
The inverter $I_{d}$ current should be in phase with grid $V_{\text{grid}}$ to send the actual power to the grid system. Hence dqSRF controller approach is adopted. Orthogonal signal pair for voltage grid and $I_{d}$ are created to convert into SRF from stationary reference frame, since the adopted controller is utilised for a single phase system. For single-phase, it is a very challenging issue to achieve zero steady state error at grid frequency. Hence, SRF control helps in creating two phases by generating an orthogonal pair, which is shown in Fig. 5. The PLL is utilised to track the grid phase angle.

The inverter $I_{d}$ current is used to generate its pair $I_{q}$. The grid voltage is used to generate its pair $V_{\text{grid}}$ [36]

$$V_{d}(t) = V \cos(\alpha t)$$

$$V_{q}(t) = V \sin(\alpha t)$$

The phase angle $\Phi$ is pretended to be $0$ ($\Phi = 0$) in order to supply actual power. Hence the expression (12) becomes

$$I_{d} = I_{\text{max}}$$

Where $I_{\text{max}}$ is the maximum current output from inverter.

The error signal is developed from expressions (14) and (15)

$$e_{d}(t) = I_{d} - I_{d}(t)$$

$$e_{q}(t) = I_{q} - I_{q}(t)$$

Where $I_{d}$ is obtained using dc voltage from boost converter, it is the reference current which develops the True power and supplied to the grid. $I_{q}$ is the reference current which develops the reactive power and is zero.

Inverter in dq system the continuous time state equation relies upon the inverter model in the SRF controller coupling condition on the inverter side and is given in the expression (16) and (17)

$$V_{d} = V_{\text{grid}} + R_{i} i_{d} + L \frac{di_{d}}{dt} - \omega L i_{q}$$

$$V_{q} = L \frac{di_{q}}{dt} + V_{\text{grid}} + R_{i} i_{q} + \omega L i_{d}$$

The $d$ and $q$ decoupling condition on the controller side is given in the expression (18) and (19)

$$V_{d} = V_{\text{grid}} - \omega L i_{q} + k_{p} + k_{i} \left(i_{d} - i_{d}^{*}\right)$$

$$V_{q} = V_{\text{grid}} + \omega L i_{d} + k_{p} + k_{i} \left(i_{q} - i_{q}^{*}\right)$$

In the above expression the reference signal $V_{a}$ is used for the PSPWM. The tuned value for $k_{i}$ is 4.58 and $k_{p}$ is 0.02.

(b) Design of modified PSPWM for CHBMLI:

Modified PSPWM technique in this system is shown in Fig. 6 [23]. The carrier wave signals are selected with respect to the expression ($n-1$)/2, where $n$ is number of levels.

$$I_{d} = I_{\text{max}}$$

$$I_{q} = I_{\text{max}}$$

$$I_{d}^{*} = I_{d} - I_{d}(t)$$

$$I_{q}^{*} = I_{q} - I_{q}(t)$$

In the above expressions the reference signal $V_{a}$ is used for the PSPWM. The tuned value for $k_{i}$ is 4.58 and $k_{p}$ is 0.02.

(b) Design of modified PSPWM for CHBMLI:

Modified PSPWM technique in this system is shown in Fig. 6 [23]. The carrier wave signals are selected with respect to the expression ($n-1$)/2, where $n$ is number of levels.
\[ \theta = \frac{360}{n-1} \frac{2}{n} \]  

120° phase difference is generated between each carrier signals with expression (21). This algorithm is developed similar to an phase opposition disposition (POD) logic for the phase shifting technique. The reference signal which is created with the help of closed loop control is then compared with the carrier signals and the generated pulses are applied to the inverter switches.

![Fig. 6. Modified phase shifted pulse width modulation for cascaded h bridge inverter](image)

(c) Design of filter using LCL method:

The design of the converter side inductance value in to reduce the ripples that has been developed by the voltage source inverter and is calculated using the expression (22). The LCL filter circuit diagram is depicted in Fig. 7.

![Fig. 7. Filter design circuit using LCL](image)

The inductor placed in the inverter side is estimated using the expression as in [32]

\[ \frac{V_{dc}}{6.4 \ast f_{SW} \ast I_{peak}} \leq L_{INV} \leq \frac{V_{dc}}{2.4 \ast f_{SW} \ast I_{peak}} \]  

(22)

\[ V_{dc} \] is dc voltages given to CHBMLI, \( f_{SW} \) is switching frequency, \( I_{peak} \) is gridcurrent maximum value. The capacitor for filter is estimated using the equation [32]

\[ C = \frac{0.05 \ast P_{rated}}{\omega_{g} \ast V_{GRID}^{2}} \]  

(23)

\[ f_{res} = \frac{1}{2\pi} X \sqrt{\frac{L_{INV} + L_{GRID}}{L_{INV} \ast L_{GRID} \ast C}} \]  

(24)

\[ R_{d} = \frac{1}{3 \ast \omega_{res} \ast C} \]  

(25)

\( P_{rated} \) is peak power, \( \omega_{g} \) is angular frequency of grid and \( V_{GRID} \) is grid voltage root mean square, \( f_{res} \) is the frequency due to resonance, \( R_{d} \) is the resistor due to damping.

The grid side inductor value is calculated using the expression

\[ L_{GRID} = r \ast L_{INV} \]  

(26)

The percentage of the factor \( r \), between \( L_{INV} \) and \( L_{GRID} \) is used in this model as 0.6 to find the grid Inductance value. The parameter values for the design of the filters are shown in Table III.

| Parameters | Values |
|------------|--------|
| Inductor at inverter side (L_{INV}) | 3.76 mH |
| Inductor at grid side (L_{GRID}) | 2.256 mH |
| Capacitor Value for filter (C) | 1.362 \mu F |
| Damping Resistor (R_d) | 10 \Omega |
| Resonance frequency (f_{res}) | 3632 Hz |
| Fundamental frequency | 50 Hz |
| Switching frequency | 5 kHz |
| Voltage at DC (V_{dc}) | 330 V |
| Grid Voltage (V_{GRID}) | 230 V |

### IV. SIMULATION ANALYSIS RESULTS

Simulation results of proposed system are analyzed and same is compared with conventional IC algorithm. Proposed and conventional system is even analyzed for different irradiances such as 1000 W/m², 400 W/m² and 700 W/m² respectively. For the conventional variable step IC algorithm, the ripple is more when compared to the modified algorithm.

Fig. 8 illustrates modified variable step size IC algorithm and Fig. 9 shows the conventional Variable step size IC algorithm for 1000 W/m² Irradiance level. Fig. 10, and Fig. 11 depicts waveforms for conventional and modified IC for different irradiance levels. Fig. 12 Shows voltage at dc link capacitor and boost voltage are same.

![Voltage waveforms](image)

![Current waveforms](image)
A DQ Synchronous Reference Frame Current Control for Grid Connected Photovoltaic Systems using Single Phase Cascaded H Bridge Multilevel Inverter

Fig. 8. Modified Variable step size IC Waveforms (a) V and I of PV output at 1000 W/m² (b) Current at the output of the dq Synchronous Ref Frame (c) Output power injected to the Grid

Fig. 9. Conventional Variable Step Size IC Waveforms (a) V and I of PV output at 1000 W/m² (b) Current at the output of the dq Synchronous Ref Frame (c) Output power injected to the Grid

Fig. 10. Modified Variable step size IC Waveforms for different Irradiance levels 1000 W/m², 400 W/m², 700 W/m² (a) Current and Voltage at the output of PV (b) Current at the output of the dq Synchronous Ref Frame (c) Output power injected to the Grid
Fig. 11. Conventional Variable step size IC Waveforms for different Irradiance levels 1000 W/m², 400 W/m², 700 W/m². (a) Current and Voltage at the output of PV. (b) Current at the output of the dq Synchronous Reference Frame. (c) Output power injected to the Grid.

Fig. 12. Output voltage of the DC link and the Boost.

Fig. 13. dq Synchronous Reference frame voltage of the grid.

Fig. 14. α and β voltages created by the orthogonal pair.

Fig. 15. Grid voltage and grid current.

Fig. 16. Synchronisation of the inverter and grid voltage.

Fig. 17. V and I at the output of boost converter.
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With 113.6V, Fig.13 shows the grid voltage after connected to d-q synchronous reference frame control. The proposed system is single phase hence generating zero steady state at grid frequency is a challenging task hence an orthogonal signal is generated and the generated alpha beta is shown in Fig.14. Voltage and current at output of grid should be in phase and is illustrated in Fig.15. The inverter and grid voltage is also synchronized and is shown in Fig.16. The voltage and current at the output of the boost converter is depicted in Fig.17. THD of the proposed model is reduced to 3% shown in Fig. 18 and conventional model with 3.15% is shown in Fig. 19. A proposed circuit is better than conventional system.

V. CONCLUSION

In this paper an extensive d-q Synchronous reference frame current control method for CHBMLI for single phase grid interfaced PV is analyzed and verified. The DC voltages of the inverter is replaced by means of solar PV system. A modified variable step size IC is adopted to track MPP and same is analyzed with conventional IC algorithm. This improves the output power at the grid side. An LCL filter is used in order to suppress the lower frequency harmonics. A modified phase shift is used for inverter switches. Phase locked loop is used for voltage and current grid synchronization. The proposed system is analyzed with different irradiance levels. Since no transformer is used the system is also cost effective. The overall efficiency of the system is about 98.7%. THD of grid current is 3% and satisfies IEEE Standard value.

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