V/C Digital Controlled DC-DC Converter

R.Sravani, P.Deepak Reddy

Abstract: In this paper, the switching of dc-dc converter using voltage/current digital control is proposed. It is the combination of existed digital average voltage and digital average current controls. The stability analysis of V/C digital controlled dc-dc converter is derived by using sampled data model. The transient analysis of V/C digital controlled dc-dc converter is also derived by using z-domain small signal model. The proposed V/C digital controlled dc-dc converter has over current protection, fast load transient response, no sub-harmonic oscillations at any value of duty cycle, and wider stability range. The proposed system is analyzed with a simple buck converter. The output voltage and inductor current weighting factors influence the stability boundary and transient performances of V/C digital controlled dc-dc converter. The stability analysis and transient analysis is investigated and verified by circuit simulations.

Keywords: sampled data modelling, stability analysis, transfer function, transient analysis, z-domain small signal modelling.

I. INTRODUCTION

As electronic technology develops, the electronic appliances power supply performance requirements are increasing. They should have faster load transient response, higher output voltage accuracy, wider stability range and over current protection. The performance of switching dc-dc converter is affected by control technique [1]-[4]. The stability and transient performances can effectively improved by enhancing the control technique of switching dc-dc converter [5]. The basic voltage control is easy but low input and load transient responses [6]. Therefore, the requirements of the power supply for advanced electronic appliances cannot satisfy with voltage control.

In V² control the inner loop utilizes the output voltage wavelet as control signal based on voltage control. It exhibits rapid load transient response but has less anti-interference ability. It is because of having insufficient amplitude of the inner-loop voltage wavelet. It is eliminated by placing a capacitor having large equivalent series resistance (ESR) at the output, with this it can operate in stable state and does not manifest over current protection [5],[7]-[9]. In current control the inner loop control signal is the switch current or inductor current. It gives rapid input response and dynamic anti-interference ability. Current control has over current protection but the load transient performance is objectionable [5],[10]-[12]. In V²C control the inner loop control signal is the combination of the inductor current and the output voltage. Accordingly it combines both advantages of voltage and current mode controls [5] i.e., over current protection in current control and rapid load transient performance of V² control additionally it has dynamic anti-interference ability [13],[14]. The disadvantage of V²C control circuit has obstacles in designing and working and when the duty cycle is above 0.5 it generates sub-harmonic oscillations, as it is a peak-ripple based control method [14],[15].

Now a day’s digital technology is improving day by day as it is advantageous than analog technology. They are increment of processing capabilities and low cost. The digital control is also more and more feasible for low to medium power switching and high frequency converters [16]-[26]. From the research it is known that the digital control deals with some modulations, such as triangle, trailing and leading-edge. They get rid of sub-harmonic oscillations [18]-[20]. A digital average voltage proposed by Liu et al [21] has rapid load response and no sub-harmonic oscillations but it can operate only with high valued capacitor ESR at the output. It doesn’t provide over current protection. Digital peak control has been proposed by G. Zhou [23] has no sub-harmonic oscillations and the duty cycle exceeds 0.5 but the controlling of inner loop signal peak value to be enhanced when current wavelet and voltage wavelet is high. To get most advantageous performance for dc-dc converters capacitor charge balance [24] is proposed but its control algorithm is very complex. A talented control scheme to manage power converter has been introduced in the field of power electronics i.e., model predictive control [26]. The contribution of this paper is as follows. A V/C digital controlled dc-dc converter is propose to eliminate the above discussed drawbacks which manifests with wider stability, fast load transient response, less sub-harmonic oscillation at any value of duty cycle, over current protection and high output voltage accuracy. To study the influence of inductor current and output voltage weighting factors on load transient performance and stability the z-domain small-signal modeling and sampled-data modeling have been used, respectively. Including that the robustness of V/C digital controlled buck converter is analyzed. The paper is systematized as follows. In session-II working principle and control algorithm of V/C digital control and the robustness of V/C digital control are analyzed with the help of buck converter. In session-III the load transient performances and stability are analyzed by using the z-domain small-signal modeling and sampled-data modeling, respectively, and stability boundary is obtained. On the load transient response and stability the effect of the output voltage and inductor current weighting factors are analyzed. MATLAB Simulation results are shown in session-IV. Finally, the paper is concluded in session-V.

Revised Manuscript Received on August 20, 2020.

* Correspondence Author
R.Sravani*, M.tech, Department of Electrical and Electronics Engineering, Lakireddy Bali Reddy College of Engineering, Mylavaram, India. E-mail: sravanirangadharara1997@gmail.com

P.Deepak Reddy, Associate Professor, Department of Electrical and Electronics Engineering, Lakireddy Bali Reddy College of Engineering, Mylavaram, India. E-mail: pdeepakr@gmail.com

DOI:10.35940/ijrte.C4295099320
Published By: Blue Eyes Intelligence Engineering and Sciences Publication
II. ANALYSIS OF V/C DIGITAL CONTROLLED DC-DC CONVERTER

A. Principle of V/C Digital Control

The circuit diagram of V/C digital controlled buck converter is shown in Fig-1. The V/C digital controlled buck converter circuit has input voltage $V_{IN}$, capacitor $C_O$, MOSFET M, inductor $L_O$, free-wheeling diode D and output capacitor equivalent series resistance $R_{ESR}$, load resistor $R_O$, digital pulse width modulation (DPWM), digital proportional-integral-differential compensator (D-PID) and analog to digital converter (ADC). Some physical quantities are represented as, capacitor voltage as $V_{CO}$, capacitor current as $I_{C0}$, inductor current as $I_{L0}$, inductor voltage as $V_{L0}$, output current as $I_O$, and output voltage as $V_O$, while sampling value of $V_O$ as $V_{OS}$, sampling value of $I_L$ as $I_{LS}$, and control signal as $V_C$, ADC sampling clock signal as $V_{CK}$, as digital reference voltage as $V_{REF}$, gate signal as $V_G$, switching period as $T$, rising slope of $V_S$ as $S_1$, falling slope of $V_S$ as $S_2$, duty cycle of $n^{th}$ cycle as $D_n$ and duty cycle of $(n+1)^{th}$ cycle as $D_{n+1}$.

The operating waveforms of sampling signal $V_S$ and $V_G$ is shown in Fig-2, where $V_S$ is the sum of $I_{LS}$ and $V_{OS}$. The steady state operating waveforms are represented in solid lines and the transient waveform with perturbation signal $V_P$ is represented in dashed lines. The $V_S$ can be obtained by $S_1$, $S_2$ and $T$.

When perturbation occurred V/C digital control forces $V_S(n)$ to made equal to $V_C$ by controlling the duty cycle. The operating principle of V/C digital controlled dc-dc converter is as follows. At the beginning of the nth cycle $V_S(n)$ is high and mosfet M is switched ON. At that time the clock pulse $V_{CK}$ enables the ADC to sample the $I_{LS}$ and $V_O$ and the $I_{LS}$ and $V_O$ is obtained to form $V_S$. At the same time $(n+D_n/2)T$ the $V_G$ is low and M is switched OFF again at the time $(n+1-D_n/2)T$ is switched ON and remains ON until the end of the $n^{th}$ cycle. DPWM gives duty cycle $D_n$ based on $V_C$, $T$, $V_S$ and D-PID calculates $V_C$ based on $V_{OS}$ and $V_{REF}$.

B. Algorithm Implementation of V/C Digital Control

At the beginning of each cycle, ADC samples the $V_O$ and $I_{LS}$ and is hold during that cycle. The $V_S$ is obtained as

$$V_S(n) = W_1I_{LS}(n) + W_2V_{OS}(n)$$

Where $W_1$ and $W_2$ are the output voltage and inductor current weighting factors, respectively. When $W_1=0$, the V/C digital control act as DAV and when $W_2=0$, the V/C digital control act as DAC control. So these are the two special cases of V/C control.

Now the sampling signal $V_S(n)$ can be expressed as

$$V_S(n+1) = V_S(n) + \frac{S_2D_nT}{2} - \frac{S_1D_nT}{2}$$

Where $S_1$ and $S_2$ can be expressed as

$$S_1 = \frac{(W_1+W_2R_{ESR})V_{IN} - V_O}{L_0},$$

$$S_2 = \frac{(W_1+W_2R_{ESR})V_O}{L_0}.$$
C. Robustness Analysis of V/C Control Algorithm

From the derived algorithm of V/C digital control it is seen that the control relies upon on the assumptions that the input voltage, the output voltage, the switching period and the inductance are known. The DSP system’s clock decides the switching period and practically its variation can be neglected. However, the working conditions or aging, change in temperature will affect the value of the inductor. It may also have considerable tolerances and the output voltage and input voltage are the same. The results exhibit that the control has good robustness and the deviation of the inductance and output voltage does no longer have an impact on the stability of algorithm [18]. The robustness analysis L0 and VIN of V/C digital controlled buck converter are discussed in this section. The error between the practical value and the designed value of inductor is represented as ΔL. Consider that at the beginning of first cycle the converter is stable, then at the beginning of (n-1)th cycle a voltage disturbance ΔV_s(n-1) is inserted, the new slopes can be expressed as

\[ S_1' = \left( W_1 + W_2 R_{\text{ESR}} \right) \frac{V_{IN} - V_O}{L_0 + \Delta L_0}, \]
\[ S_2' = \left( W_2 + W_2 R_{\text{ESR}} \right) \frac{V_{IN} - V_O}{L_0 + \Delta L_0} \]  

Where S_1' is new rising slope and S_2' is new falling slope of V_s. Then, at the beginning of the nth cycle the disturbance of V_s can be obtained as

\[ \Delta V_s(n) = V_C(n - 1) - [V_s(n - 1) - \frac{S_1'D_{n-1}T}{2} - \frac{S_2'D_{n-1}T}{2}] \]
\[ = D_{n-1}T(S_1 - S_1') + D_{n-1}T(S_2 - S_2') \]
\[ = -\frac{\Delta V_s(n - 1)}{L_0 + \Delta L_0} \]  

Similarly, with practical input voltage V_{IN}\Delta V_{IN} at the beginning of the nth cycle the disturbance of V_s can be expressed as

\[ \Delta V_s(n) = \frac{\Delta V_{IN}}{V_{IN}} \Delta V_s(n - 1) - \frac{\Delta V_{IN} R_{\text{ESR}} TV_O}{V_{IN} L_0} \]

From this it is clear that as long as ΔL_0<<L_0 and ΔV_{IN}<<V_{IN}, the inductor tolerance and input tolerance no longer affects the control performance, in practical applications it is difficult to meet. Finally we can justify that even though the circuit parameters have small variation the V/C digital control is robust and can maintain converter in stable state.

III. STABILITY AND TRANSIENT ANALYSIS OF V/C CONTROLLED BUCK CONVERTER

The V_s is linear when the output capacitor ESR is large as in the above analysis. In some cases the ESR is small when for output filtering multiple parallelled ceramic capacitors are utilized, so the effect of the nonlinearity of V_s on the stability of V/C digital control is considerable. So we have to analyze the stability boundary for V/C digital control related to ESR. It is done by using sampled data modeling. The DAV and DAC are the two individual cases of V/C digital control. The two controls have two different load transient performances. The V/C digital control load transient performance is affected by and the output voltage and inductor current weighting factors. The transient analysis is done by z-domain small signal modeling.
At $T = n+1$ again the diode D is forward biased when mosfet M is switched off. At $T = n+1$ the capacitor voltage $V_{CO}(n+1)$ and inductor current $I_{LO}(n+1)$ can be expressed as

$$I_{LO}(n+1) = I_{LO}(n + 1 - \frac{D}{2}) + S_{L} \frac{T_{ON}(n)}{2T_{IN}(n)}$$

$$V_{CO}(n+1) = V_{CO}(n + 1 - \frac{D}{2}) + \frac{1}{C_{O}} \int_{I_{LO}(n)}^{I_{LO}(n+1)} V_{CO} dt$$

$$= V_{CO}(n + 1 - \frac{D}{2}) + \frac{3 S_{L} T_{ON}(n)}{2}$$

From equation (6), in nth cycle the $T_{ON}$ of mosfet M can be obtained as

$$T_{ON} = \frac{V_{C}(n) - V_{S}(n)}{S_{1} + S_{2}} + \frac{S_{3} T}{S_{1} + S_{2}}$$

The complete sampled-data model of the V/C digital controlled buck converter composed in equations (4.2)–(4.5).

For stability analysis a jacobian matrix is derived in the steady-state point by linearizing the nonlinear functions $I_{LO}(n+1)$ and $V_{CO}(n+1)$ with respect to $I_{LO}(n)$ and $V_{CO}(n)$. The Jacobian matrix $J$ is written as

$$J = \begin{bmatrix} J_{11} & J_{12} \\ J_{21} & J_{22} \end{bmatrix}$$

Where $I_{LO}(n)$ and $V_{CO}(n)$ steady-state values are denoted by $I_{LO}$ and $V_{CO}$, respectively. From (3.3) and (4.1)–(4.5), $J_{11}$, $J_{12}$, $J_{21}$, and $J_{22}$ can be obtained as

$$J_{11} = \frac{\partial I_{LO}(n+1)}{\partial I_{LO}(n)} = 0$$

$$J_{12} = \frac{\partial I_{LO}(n+1)}{\partial V_{CO}(n)} = -\frac{W_{2}}{W_{1} + W_{2}R_{ESR}}$$

$$J_{21} = \frac{\partial V_{CO}(n+1)}{\partial I_{LO}(n)} = \frac{2C_{O}}{2}$$

$$J_{22} = \frac{\partial V_{CO}(n+1)}{\partial V_{CO}(n)} = 1 - \frac{W_{2}T}{2C_{O}(W_{1} + W_{2}R_{ESR})}$$

Then, the eigen values $\lambda_{1}$ and $\lambda_{2}$ of $J$ are derived as

$$\lambda_{1,2} = \frac{J_{11} + J_{22} \pm \sqrt{(J_{11} + J_{22})^{2} - 4(J_{11}J_{22} - J_{12}J_{21})}}{2}$$

The stability of the V/C digital controlled buck converter needs that the two eigen values should be inside the unit circle. Therefore, the eigen values are $|\lambda_{1,2}| < 1$ if

$$R_{ESR} > R_{CRIT} = \frac{T}{2C_{O}} - \frac{W_{1}}{W_{2}}$$

Where $R_{CRIT}$ is the minimum value of ESR where the system work steadily. The equation (18) represents V/C digital controlled buck converter stability boundary condition. From equation (18), we can say that the duty cycle doesn’t affect the stability of V/C digital controlled buck converter, it can be found by output capacitor, switching period and inductor current and output voltage weighting factors. In full range of the duty cycle when ESR is larger than $R_{CRIT}$ the system can work stably. The system is unstable when the ESR of output capacitor is smaller than $R_{CRIT}$, but by raising the $W_{1}/W_{2}$ ratio the system can be made stable.

**B. Load Transient Performance Analysis using z-domain Small Signal Modeling**

From the theoretical view, in order to research the transient performance of V/C digital controlled buck converter, the z-domain small-signal modeling is executed. The open loop transfer functions of buck converter from $V_{G}$ to $I_{LO}$, $V_{G}$ to $V_{O}$ are $G_{VD}(s)$, $G_{ID}(s)$, and $Z_{OUT}(s)$, respectively [28], and they can be expressed as

$$G_{VD}(s) = \frac{V_{IN}R_{D}(C_{O}R_{ESR}s + 1)}{L_{O}C_{O}(R_{O} + R_{ESR})s^{2} + (C_{O}R_{O}R_{ESR} + L_{O})s + R_{C}}$$

$$G_{ID}(s) = \frac{V_{IN}(C_{O}(R_{O} + R_{ESR})s + 1)}{L_{O}C_{O}(R_{O} + R_{ESR})s^{2} + (C_{O}R_{O}R_{ESR} + L_{O})s + R_{C}}$$

$$Z_{OUT}(s) = \frac{C_{O}R_{O}R_{ESR}L_{O}s^{2} + R_{D}L_{O}s}{L_{O}C_{O}(R_{O} + R_{ESR})s^{2} + (C_{O}R_{O}R_{ESR} + L_{O})s + R_{C}}$$

From the theoretical view, in order to research the transient performance of V/C digital controlled buck converter, the z-domain small-signal modeling is executed. The open loop transfer functions of buck converter from $V_{G}$ to $I_{LO}$, $V_{G}$ to $V_{O}$ are $G_{VD}(s)$, $G_{ID}(s)$, and $Z_{OUT}(s)$, respectively [28], and they can be expressed as

$$G_{VD}(s) = \frac{V_{IN}R_{D}(C_{O}R_{ESR}s + 1)}{L_{O}C_{O}(R_{O} + R_{ESR})s^{2} + (C_{O}R_{O}R_{ESR} + L_{O})s + R_{C}}$$

$$G_{ID}(s) = \frac{V_{IN}(C_{O}(R_{O} + R_{ESR})s + 1)}{L_{O}C_{O}(R_{O} + R_{ESR})s^{2} + (C_{O}R_{O}R_{ESR} + L_{O})s + R_{C}}$$

$$Z_{OUT}(s) = \frac{C_{O}R_{O}R_{ESR}L_{O}s^{2} + R_{D}L_{O}s}{L_{O}C_{O}(R_{O} + R_{ESR})s^{2} + (C_{O}R_{O}R_{ESR} + L_{O})s + R_{C}}$$

Here, the transfer function from $I_{O}$ to $I_{LO}$ of buck converter denoted by $A_{1}(s)$, which is

$$A_{1}(s) = \frac{R_{C}R_{ESR}}{(R_{O} + R_{ESR})L_{O}s^{2} + 2\xi\omega_{s}^{2}}$$

Where,

$$\xi = (C_{O}R_{O}R_{ESR} + L_{O})/(2(L_{O}C_{O}R_{O}R_{ESR}))^{1/2}$$

The z-domain transfer functions can be obtained from s-domain form by applying the Tustin approximation [28], which can be expressed as

$$G_{VD}(z) = \frac{V_{IN}T^{2}(2C_{O}R_{ESR} + T)z^{2} + 2Tz - 2C_{O}R_{ESR}}{L_{O}C_{O}(\alpha_{1} z^{2} + \alpha_{2} z + \alpha_{3})}$$

$$G_{ID}(z) = \frac{V_{IN}T^{2}(2C_{O}R_{O}R_{ESR} + T)z^{2} + 2Tz - 2C_{O}R_{O}R_{ESR}}{L_{O}C_{O}(\alpha_{1} z^{2} + \alpha_{2} z + \alpha_{3})}$$

$$Z_{OUT}(z) = \frac{2C_{O}R_{ESR} + T)z^{2} - 8C_{O}Tz - 2T + 4C_{O}R_{ESR}}{C_{O}(\alpha_{1} z^{2} + \alpha_{2} z + \alpha_{3})}$$

$$A_{1}(z) = \frac{(2C_{O}R_{ESR} + T)z^{2} + 2Tz + \frac{T}{R_{O} + R_{ESR}}}{(\alpha_{1} z^{2} + \alpha_{2} z + \alpha_{3})}$$

Where

$$\alpha_{1} = 4(1 + \frac{R_{ESR}}{R_{O}}) + \frac{T^{2}}{L_{O}C_{O}} - 2T \frac{R_{ESR}}{L_{O}} + \frac{1}{C_{O}R_{O}}$$
\[\alpha_1 = \frac{2T^2}{L_0C_0} - 6\left(1 + \frac{R_{\text{ESR}}}{R_0}\right)\]

\[\alpha_2 = 4\left(1 + \frac{R_{\text{ESR}}}{R_0}\right) + \frac{T^2}{L_0C_0} - 2T\left(\frac{R_{\text{ESR}}}{L_0C_0} + \frac{1}{C_0R_0}\right)\]

\[\beta = \frac{4L_0C_0(R_0 + R_{\text{ESR}})}{R_0}\]

As in Fig-2, each variable is the combination of an ac component and dc component which replicate the response to this disturbance as indicated in

\[\tilde{V}_C(\alpha) = V_c + \bar{V}_c(\alpha)\]

\[\tilde{V}_S(\alpha) = V_s + \bar{V}_s(\alpha)\]

\[\tilde{D}(\alpha) = D + \bar{D}(\alpha)\]

(22)

Where \(V_c\), \(V_s\), and \(D\) are the dc components, and \(\bar{V}_c(\alpha), \bar{V}_s(\alpha), \) and \(\bar{D}(\alpha)\) are the ac components. Neglecting the nonlinear ac terms and substitute (22) into (4), the ac small-signal equation and dc equation can be obtained as

\[\tilde{V}_c = V_s + (S_1 + S_2)DT - S_1 T\]

\(\bar{V}_c(\alpha) = \bar{V}_s(\alpha) + (S_1 + S_2)T\bar{D}(\alpha)\)

(23)

The ac small-signal equation can be rephrase as

\[\bar{D}(\alpha) = \frac{L_0}{(W_1 + W_2R_{\text{ESR}})V_{\text{IN}}T}\left[\bar{V}_c(\alpha) - \bar{V}_s(\alpha)\right]\]

(24)

By converting equation (24) to the z-domain, the \(D(z)\) can be obtained as

\[D(z) = F[V_c(z) - V_s(z)]\]

(25)

Where \(F = L/(W_1 + W_2R_{\text{ESR}}V_{\text{IN}}T)\)

By ignoring the delays and quantization errors of ADC, the transfer function of ADC can be stated as

\[G_{\text{ADC}} = \frac{2^N}{V_{\text{REF}}}\]

(26)

Where \(V_{\text{REF}}\) is the reference voltage of ADC and \(N\) is the number of bits of ADC. Based upon D-PID algorithm as (4) the compensator is designed. The related D-PID z-domain representation can be stated as

\[G_c(z) = K_f + K_i \frac{z}{z-1} + K_d \frac{z-1}{z}\]

(27)

The V/C digital controlled buck converter z-domain small-signal diagram is achieved based on (21)–(27) and is shown in Fig-5. By using Mason’s law the closed-loop output impedance transfer function can be derived, and it is expressed as

\[Z_{\text{OUT}}(z) = \frac{G_{\text{ADC}}(z)}{G_c(z)}\]

Fig-5 - V/C digital Controlled Buck Converter z-domain small signal diagram

The V/C digital controlled buck converter z-domain small-signal diagram is achieved based on (21)–(27) and is shown in Fig-5. By using Mason’s law the closed-loop output impedance transfer function can be derived, and it is expressed as

\[Z_{\text{OUT}}(z) = \frac{G_{\text{ADC}}(z)}{G_c(z)}\]

(28)

Based on the z-domain small signal modeling and above analysis, the simulation of V/C digital controlled buck converter is done by using MATLAB by selecting the circuit parameters as required. The closed loop output impedance magnitude is increased by keeping \(W_2\) constant and increasing \(W_1\) which gives slower load transient response speed. The closed loop output impedance magnitude is decreased by keeping \(W_1\) constant and increasing \(W_2\) which gives the faster load transient response speed. Therefore, it can be finalized that the output voltage and inductor current weighting factors influence the load transient performance of the system. The system has inferior load transient response when the ratio of \(W_1/W_2\) increases and the system has superior load transient response when the ratio of \(W_1/W_2\) decreases

Table-1 - V/C digital controlled buck converter components and its significance

| Component       | significance |
|-----------------|--------------|
| Input voltage   | 100V         |
| Switching period| 0.02s        |
| Output inductor | 0.5H         |
| Output Capacitor| 20 μF        |
| ESR of capacitor| 500 Ω        |
| Load resistance | 10 Ω         |

Based on the earlier transient performance and stability analyses, it can be finalized that when the ratio of \(W_1/W_2\) is huge, the load transient response of the system becomes narrow but the range of system stability becomes broad. Therefore, the choice of \(W_1\) and \(W_2\) is the tradeoff between the load transient responses stability of the system.
V/C Digital Controlled DC-DC Converter

Fig-7 - Output voltage and inductor current simulation waveforms of V/C digital controlled buck converter. (a) $V_o = 30 \text{V}$ and $D < 0.5$. (b) $V_o = 70 \text{V}$ and $D > 0.5$

Fig-8 - Output voltage and inductor current simulation waveforms with different $W_1$, $W_2$ and $R_{ESR}$. (a) $W_1 = 2$, $W_2 = 0.006$, and $R_{ESR} = 200\Omega$. (b) $W_1 = 2$, $W_2 = 0.006$, and $R_{ESR} = 300\Omega$. (c) $W_1 = 2$, $W_2 = 0.008$, and $R_{ESR} = 300\Omega$.

Table-II - Load transient performance simulation results of V/C digital controlled buck converter in three cases

| Weighting Factors | Load steps from 10A to 20A | Load steps from 20A to 10A |
|-------------------|---------------------------|---------------------------|
|                   | Undershoot voltage/V | Setting time/S | Overshoot voltage/V | Setting time/S |
| $W_1=1, W_2=0$ | 50 | 1.3 | 140 | 0.5 |
| $W_1=0.5, W_2=0.5$ | 30 | 0.5 | 80 | 0.4 |
| $W_1=0, W_2=1$ | 20 | 0.2 | 50 | 0.2 |

IV. SIMULATION RESULTS OF V/C DIGITAL CONTROLLED BUCK CONVERTER

To verify the transient performance and stability analysis of proposed control, simulation of V/C digital controlled buck converter is carried out by using MATLAB. The parameters used in simulation as the same as in table-I.

A. Stability performance verification

To verify the stability boundary condition of V/C digital controlled buck converter, on the system stability the influence output voltage and inductor current weighting factors and duty cycle are examined by simulation. Taking $W_1=0.5$ and $W_2=0.5$, V/C digital
controlled buck converter is simulated and waveforms of inductor current and output voltage are shown in Fig-6 representing the situation \( D > 0.5 \) and \( D < 0.5 \). As shown in Fig-6, the system is stable either \( D < 0.5 \) or \( D > 0.5 \) and the sub-harmonic oscillation are eliminated in the system. Therefore, it can prove that at any value of duty cycle the V/C digital controlled buck converter is stable when the ESR of output capacitor satisfies the stability boundary condition, and the system has good output voltage accuracy.

The simulation waveforms of V/C digital controlled buck converter are shown in Fig-8 with different \( W_1 \), \( W_2 \) and \( R_{ESR} \). The weighting factors are chosen as \( W_1=2 \), \( W_2=0.006 \) in Fig-8(a) and (b). The \( R_{CRIT} \) is obtained as 170\( \Omega \) by (18). When \( R_{ESR}=200\Omega \), the ripple is small and the output voltage is stable and it is shown in shown in Fig-8(a) and (b). When \( R_{ESR}=300\Omega \), the ripple becomes large as the low-frequency oscillation occurs. According to (18), keeping \( W_1 \) is as constant i.e., 2, increasing \( W_2 \) from 0.006 to 0.008, \( R_{CRIT} \) becomes 250\( \Omega \). In Fig-8(c) the simulation waveform with \( R_{ESR}=300\Omega \) are shown. From Fig-8(c), it can be observed that the low-frequency oscillations are eliminated and the output. In the above simulation waveforms the stability boundary of V/C digital controlled buck converter is accurate. At any value of duty cycle V/C digital controlled buck converter has output voltage accuracy and it is stable. By regulating the ratio of \( W_1/W_2 \) the stability range can be extended.

B. Load Transient Performance Verification

In this section, three cases are assumed to verify the load transient response of V/C digital controlled buck converter simulation output waveforms. They are 1) \( W_1 \) and \( W_2 \) are 1 and 0 respectively; 2) \( W_1 \) and \( W_2 \) both 0.5; 3) \( W_1 \) and \( W_2 \) are 0 and 1 respectively. Fig-9 and 10 shows the transient analysis simulation waveforms of input current and output voltage. In Fig-9 the load steps from 8A to 20A. In Fig-10 load steps from 20A to 8A. To compare three cases, the overshoot and undershoot voltages and settling times of output voltage have been viewed in Table-II.

When the ratio of \( W_1/W_2 \) is small the output voltage overshoots or undershoots is reduced and the load transient response is sooner. When the ration of \( W_1/W_2 \) is high the output voltage overshoots or undershoots is increased and the load transient response goes slow down.
V/C Digital Controlled DC-DC Converter

From this we can justify the by adjusting the inductor current and output voltage weighting factors of V/C digital control can attain rapid load transient performance.

The simulation results show that the inductor current and output voltage weighting factors of V/C digital control influence the load transient performance and the stability of the system. When the ratio of $W_1/W_2$ increases the stability range of V/C digital controlled buck converter becomes wider but the load transient response becomes inferior, when the ratio of $W_1/W_2$ decreases the narrow stability range of V/C digital controlled buck converter becomes, but the load transient response becomes superior. Therefore, the value of $W_1$ and $W_2$ is tradeoff between the load transient responses and the stability of the system.

The advantages of the V/C digital control are mentioned below. It has over current protection, perfect power management, and over voltage protection. It has good stability at any value of duty cycle, good robustness to the system parameters and strong anti-interference ability. Additionally, its dependence on ESR of output capacitor can be adjusted by changing the ratio of the output voltage and inductor current weighting factors. The V/C digital control has fast load transient performance, and can be adjusted by changing the ratio of the output voltage and inductor current weighting factors.

V. CONCLUSION

In this paper, the circuit and operating principle of V/C digital controlled buck converter is discussed. Sampled data modeling has been analyzed to obtain the stability boundary condition of V/C digital controlled buck converter, which shows that V/C digital control can work stably at any value of duty cycle and does not suffer the ESR limitation by adjusting the ratio of the output voltage and inductor current weighting factors. The V/C digital control technique has tough parameter tolerance. It is shown by robustness analysis. In addition, the z-domain small signal model has been analyzed to obtain the load transient response of V/C digital controlled buck converter which shows that the load transient performance of V/C digital control can be improved by adjusting the ratio of the output voltage and inductor current weighting factors. Finally, it is proven by simulation that the proposed V/C digital control has high voltage regulation accuracy, wide range of stability, and fast load transient response, good robustness and can achieve over current protection.

REFERENCES

1. K.-H. Cheng, C.-W. Su, and H.-H. Ko, “A high-accuracy and high-efficiency on-chip current sensing for current-mode control CMOS DC/DC buck converter,” in Proc. IEEE 15th Int. Conf. Electron. Circuits Syst., Aug./Sep. 2008, pp. 458–461.
2. Y.-C. Lin, C.-J. Chen, D. Chen, and B. Wang, “A ripple-based constant on-time control with virtual inductor current and offset cancellation for DC power converters,” IEEE Trans. Power Electron., vol. 27, no. 10, pp. 4301–4310, Oct. 2012.
3. K. Yao, Y. Ren, and F. C. Lee, “Critical bandwidth for the load transient response of voltage regulator modules,” IEEE Trans. Power Electron., vol. 22, no. 6, pp. 1454–1461, Nov. 2008.
4. Y. Chi, X.-Q. Lai, and H.-X. Du, “Fast transient response high-accuracy current-sensing technique for step-up DC–DC converter,” Electron. Lett., vol. 51, no. 7, pp. 577–579, Apr. 2015.
5. G. Zhou, J. Xu, and J. Wang, “Constant-frequency peak-ripple-based control of buck converter in CCM: Review, unification, and duality,” IEEE Trans. Ind. Electron., vol. 61, no. 3, pp. 1280–1291, Mar. 2013.
6. R. Mammano, “Switching power supply topology voltage mode vs. current mode,” Unitrode Corp., Merrimack, NH, USA, Unitrode Design Note DN-62, 1994.
7. C.-S. Huang, C.-Y. Wang, J.-H. Wang, and C.-H. Tsai, “A fast-transient quasi-V2 switching buck regulator using AOT control,” in Proc. IEEE Asian Solid-State Circuits Conf., Nov. 2011, pp. 53–56.
8. C.-C. Fang and C.-I. Chyi, “Subharmonic instability limits for V2controlled buck converter with outer loop closed-open,” IEEE Trans. Power Electron., vol. 31, no. 2, pp. 1657–1664, Feb. 2016.
9. G. Zhou, S. He, X. Zhang, and S. Zhong, “Critical output-capacitor ESR for stability of V2 controlled buck converter in CCM and DCM,” Electron. Lett., vol. 50, no. 12, pp. 884–886, Jun. 2014.
10. D. M. Mitchell, “An experimental investigation of current-injected control for constant-frequency switching regulators,” IEEE Trans. Power Electron., vol. PE-1, no. 3, pp. 167–174, Jul. 1986.
11. W. Tang, F. C. Lee, and R. B. Ridley, “Small-signal modeling of average current-mode control,” IEEE Trans. Power Electron., vol. 8, no. 2, pp. 112–119, Apr. 1993.
12. C. Restrepo, J. Calvente, A. Romero, E. Vidal-Iliarte, and R. Giral, “Current-mode control of a coupled-inductor buck–boost DC–DC switching converter,” IEEE Trans. Power Electron., vol. 27, no. 5, pp. 2536–2549, May 2012.
13. F. Wang, J. Xu, and B. Wang, “Comparison study of switching DC–DC converter control techniques,” in Proc. IEEE Int. Conf. Commun. Circuits Syst., Jun. 2006, pp. 2713–2717.
14. C. Mi, J. Xu, G. Zhou, and Y. Jin, “On the stability of V2 controlled boost converter in continuous conduction mode,” in Proc. IEEE 6th Int. Power Electron. Motion Control Conf., May 2009, pp. 1300–1304.
15. W. Huang, “A new control for multi-phase buck converter with fast transient response,” in Proc. IEEE 16th Annu. Appl. Power Electron. Conf. Expo., Mar. 2001, pp. 273–279.
16. P. Cortés, M. P. Kazmierkowski, R. M. Kennel, D. E. Quevedo, and J. Rodriguez, “Predictive control in power electronics and drives,” IEEE Trans. Ind. Electron., vol. 55, no. 12, pp. 4312–4324, Dec. 2008.
17. Z. Zhang et al., “Predictive control with novel virtual-flux estimation for back-to-back power converters,” IEEE Trans. Ind. Electron., vol. 62, no. 5, pp. 2823–2834, May 2015.
18. J. Chen, A. Prodic, R. W. Erickson, and D. Maksimovic, “Predictive digital current programmed control,” IEEE Trans. Power Electron., vol. 18, no. 1, pp. 411–419, Jan. 2003.
19. G. Zhou, J. P. Xu, and Y. Y. Jin, “Improved digital peak voltage predictive control for switching DC–DC converters,” JET Power Electron., vol. 4, no. 2, pp. 227–234, Feb. 2011.
20. G. Zhou, J. Xu, and Y. Jin, “Elimination of subharmonic oscillation of digital-average-current-controlled switching DC–DC converters,” IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2904–2907, Aug. 2010.
21. X. Liu, G. Zhou, M. Leng, and S. Zhou, “Digital average voltage control for switching DC–DC converters,” in Proc. IEEE 48th Annu. Southeast Power Electronics Motion Control Conf., May 2016, pp. 1156–1160.
22. J. Xu, G. Zhou, and M. He, “Improved digital peak voltage predictive control for switching DC–DC converters,” IEEE Trans. Ind. Electron., vol. 56, no. 8, pp. 3222–3229, Aug. 2009.
23. G. Zhou, J. Xu, J. Wang, and Y. Jin, “Comparison study on digital peak current, digital peak voltage, and digital peak voltage/peak current controlled buck converter,” in Proc. IEEE 4th Conf. Ind. Electron. Appl., May 2009, pp. 799–804.
24. G. Feng, E. Meyer, and Y.-F. Liu, “A new digital control algorithm to achieve optimal dynamic performance in DC-to-DC converters,” IEEE Trans. Power Electron., vol. 22, no. 4, pp. 1489–1498, Jul. 2007.
25. P. Karamanakos, T. Geyer, and S. Manias, “Direct voltage control of DC–DC boost converters using model predictive control based on enumeration,” in Proc. IEEE 15th Int. Power Electron. Motion Control Conf., Sep. 2013, pp. DS2c.10–DS2c.12.
26. L. Cheng, P. Acuna, R. P. Aguilera, M. Ciobotaru, and J. Jiang, “Model predictive control for DC-DC boost converters with constant switching frequency,” in Proc. IEEE 2nd Annu. Southern Power Electron. Conf., Auckland, New Zealand, Dec. 2016, pp. 1–6.
27. R. Redl and J. Sun, “Ripple-based control of switching regulators—An overview,” IEEE Trans. Power Electron., vol. 24, no. 12, pp. 2669–2680, Dec. 2009.
28. G. F. Franklin, J. D. Powell, and M. L. Workman, Digital Control of Dynamic Systems, 3rd ed. Reading, MA, USA: Addison-Wesley, 1998.
29. K.-H. Cheng, C.-W. Su, and H.-H. Ko, “A high-accuracy and high-efficiency on-chip current sensing for current-mode control CMOS DCDC buck converter,” in Proc. IEEE 15th Int. Conf. Electron. Circuits Syst., Aug./Sep. 2008, pp. 458–461.

30. Guohua Zhou, hongbo zhao, W.Z, S.Xu “Digital average voltage/digital average current predictive control for switching dc-dc converters,” IEEE Journal of emerging and selected topics in power electronics, vol.6, no.4, December 2018.

AUTHORS PROFILE

Sravani.R was born in 1997. She received diploma in electrical and electronics engineering from SABTET, Andhra Pradesh, India in 2015. She received B.Tech degree in electrical and electronics engineering from JNTU, Kakinada, India in 2018 and she is pursuing M.Tech in “Power electronics and Drives” from JNTU, Kakinada. Her area for interest include power electronics and drives, control of dc-dc converters.

Deepak Reddy.P was born in 1981. Received B.Tech degree in electrical and electronics engineering from JNTU, Hyderabad, India in 2002, and he received the M.Tech degree from vellore institute of technology, vellore, India in 2005, and he is pursuing Ph.D. on “Modeling and Analysis of Control Techniques for DC-DC Buck converter” from GITAM University, Hyderabad. He worked as a Asst.Prof., in at SVITS, Mahaboobnagar, Currently he is working as an Associate Professor in Dept. of EEE in Lakireddy Bali Reddy college of Engineering, Mylavaram, India. His areas of interest include power electronics and drives, ac–dc converter with power factor correction, SMPS and Active power filters for Harmonic compensation, dc-dc converters. He presented more than 10 publications in international journals. He is a Life member of ISTE, Life member of IETE.