Research Article

Design of Multichannel Multirate Signal Acquisition System Based on FPGA

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With the continuous advancement of science and technology, the fields of national defense, astronomy, industry, agriculture, and so on often require real-time acquisition of voltage, current, temperature, pressure, flow, and other signals, and the real-time requirements for signal acquisition are getting higher and higher. The traditional temperature acquisition method is to use the single chip or DSP as the control core to design the temperature monitoring system. However, this method has certain defects and cannot meet many high-demand signal acquisition occasions. On the one hand, most functions of this system are realized by software, and the operation of software will occupy part of the system sampling time, thus reducing the system sampling rate; on the other hand, the logic of the system to complex peripheral circuits cannot be well controlled. And Field Programmable Gate Array (FPGA) has characteristics such as parallel processing, controllability, and processing speed; therefore, the signal acquisition system with FPGA as the control core can realize high-speed signal collection. This paper studies the signal acquisition based on FPGA. In the signal acquisition system, FPGA is the control core of the whole system, and the relevant function modules of the control system complete the signal acquisition task. The acquisition control module is mainly to control the channel selection switch and the A/D converter to work, that is, to generate the logic control signal of multichannel selection and the control sequence of A/D conversion, so as to complete the acquisition and control of the multichannel analog input signal. The FPGA-based signal acquisition control system has the characteristics of short development cycle, flexible design, low cost, and high reliability. FPGA is an ideal architecture for signal acquisition, and the FPGA-based signal acquisition technology has very broad application prospects.

1. Introduction

Digital signal processing technology, as an emerging technology of multidisciplinary integration, has become increasingly mature after decades of development and is also favored by people, especially in the field of communication [1]. Digital TI and Altera, the world leaders in the field, have successively developed digital processing platforms for DSP development boards. The advent of these platforms has brought great convenience to digital signal processing, but these platforms can only identify digital signals but cannot identify digital signals in daily life. In the acquisition of analog signals, as well as digital-to-analog conversion, a lot of development is still needed [2, 3]. At present, the commonly used signal acquisition system controlled by single-chip microcomputer or DSP is not reliable enough, the acquisition speed is not fast enough, the real-time performance is not strong enough, the external circuit is relatively complicated, and it is easily disturbed by the external environment [4]. Therefore, it is very meaningful to design and develop a high-speed acquisition system with strong anti-interference ability and stable operation.

Field Programmable Gate Array (FPGA) is developed on the basis of Programmable Array Logic (PAL), Generic Array Logic (GAL), Erasable Programmable Logic Device (EPLD), and so on [5, 6]. The design with FPGA as the core can be understood as a kind of semicustom circuit. Its appearance not only makes up for the deficiency of custom
circuit but also overcomes the deficiency of previous programmable device logic gate. It is a new product in the field of contemporary electronic design [7–9]. The acquisition system with FPGA as the control core has the following three advantages: first, the FPGA chip has rich scalability and high integration, and the hardware description language (Verilog and VHDL) of the FPGA is highly modifiable, which makes the system designed on the basis convenient for designers to flexibly modify dynamically and upgrade in the future [10]. Second, the system logic with FPGA as the control core can be completely completed by hardware, which shortens the acquisition time occupied by software operation and improves the system performance; in addition, FPGA has parallel processing capability, which greatly improves the real-time performance of the acquisition system [11–13]. Third, the FPGA is compatible with IP cores such as DSP, which greatly shortens the development cycle of the acquisition system. In recent decades, the technology of signal acquisition and processing has been developing continuously under the background of the rapid development of computer technology [10, 14]. At present, there are the following four ways to collect and process signals. (1) The PC-based signal acquisition and processing system performs A/D conversion on the collected analog signals and then sends them to the PC for processing. This method is not very flexible and has too many limitations. (2) Signal acquisition and processing system based on single-chip microcomputer: as a highly integrated microcomputer, single-chip microcomputer overcomes the shortcomings of the previous generation of computer digital acquisition and is a better choice in occasions where real-time requirements are not high. (3) Signal acquisition and processing system based on DSP: the DSP chip occupies a place in signal acquisition and processing by virtue of its powerful computing power, high precision, and strong real-time processing of acquired signals. (4) Combination of DSP and FPGA: the idea of adopting this acquisition method is to combine the advantages of the two. On the one hand, the powerful digital signal processing capability of DSP is used to complete the signal processing, and on the other hand, the powerful logic control capability of FPGA is used to realize the control of peripheral circuits.

This paper mainly studies the signal collection technology based on FPGA. In the signal collection system designed in this paper, FPGA is the control core of the whole system, and the relevant function modules of the control system complete the task of signal collection and processing [15, 16]. The FPGA-based control includes the FPGA-based integrated control module used to control the channel selection switch and the AD converter, complete the selection of multichannel analog input signals, and sample the four channels of analog signals after the multichannel selection switch [17]. The FPGA-based control system implemented in this design can complete the acquisition of high-speed real-time signals, and the system has high precision and strong versatility and can be widely used in various signal processing fields, with high research value and broad application prospects [18, 19].

2. Materials and Methods

2.1. The Basic Structure of FPGA. The structure of FPGA is divided into three parts: programmable logic block CLB, input/output module IOB, and interconnection resource IR. Its structure is shown in Figure 1.

When the FPGA is working, the FPGA development software will automatically compile the design input such as Hardware Design Language (HDL) or schematic diagram into a data stream and download it to the on-chip RAM, which is determined by the data stream downloaded to the RAM. We design the logical relationship of the circuit. When the FPGA is powered off, the data in the RAM disappear, and the FPGA returns to a white film. According to the data flow in the RAM, the logic relationship of the designed circuit is different, which is the so-called programmable characteristic.

2.2. Design Scheme

2.2.1. Selection of Signal Processor. Because FPGA has the characteristics of high clock frequency, flexible design, abundant I/O resources, and easy expansion, as well as the advantages of FPGA in parallel signal processing, FPGA is selected as the control and processing chip of the whole system in this design. The FPGA chip selected in this design is the Cyclone II series EP2C35F672C6 of Altera Corporation, which contains 35 18 × 18 hardware multipliers and a large-capacity on-chip memory M4KRAM, which makes this FPGA chip very suitable for use as a signal processor.

2.2.2. The Choice of Algorithm. In this design, the FFT algorithm will be used to complete the signal processing. The Fast Fourier Transform (FFT) algorithm is an important mathematical tool for analyzing signal processing. It is not a completely new algorithm but is developed from the Discrete Fourier Transform (DFT) algorithm. The appearance of FFT algorithm has greatly increased the flexibility of digital signal processing and has become a powerful tool for signal analysis and processing at this stage. Therefore, the FFT algorithm is widely used in many fields; for example, in the field of real-time signal processing and image signal processing, the FFT algorithm is used to process signals.

2.2.3. Choice of Development Platform. The hardware development platform chosen for this design is the DE2 development platform of Altera Corporation. The DE2 development platform is an FPGA multimedia development platform launched by Altera. It provides users with a wealth of peripherals and multimedia features and has a flexible and reliable peripheral interface design.

The hardware resources provided on the DE2 development platform are Altera Cyclone II series FPGA EP2C35F672C6, which consists of 35000 logic units and has 105 M4K RAM blocks on-chip; each M4K RAM block consists of 4K (4096) bits of data RAM plus 512 bits of parity bits, a total of 483840 bits. There are 35 18 × 18 hardware...
3. Results and Discussion

In the field of industrial control, single-chip microcomputer or DSP is often used to control the A/D converter to realize signal acquisition and corresponding processing. However, the clock frequency of the single-chip microcomputer is low, and its functions are mainly realized by software programming. Therefore, due to the limitation of its instruction cycle and processing speed, it is difficult to use a single-chip microcomputer to complete the control of multiple channels and multiple A/Ds and the corresponding data. Therefore, the sampling control system implemented by the single-chip microcomputer is not suitable for the high-speed acquisition field. Although DSP chips have strong digital signal processing capabilities and are good at processing complex operations, it is difficult for DSP chips to complete the logic control of peripheral devices. The FPGA has the characteristics of flexible design modification, rich I/O resources, and good at parallel signal processing, so that the sampling control module implemented by FPGA can meet the requirements of multichannel high-speed acquisition.

3.1. Design of the Hardware Part. The hardware part of the acquisition control module mainly includes multichannel selection switch, A/D conversion circuit, and multichannel sampling control circuit realized by FPGA. The hardware structure diagram of the integrated control module is shown in Figure 2.

3.1.1. Multichannel Selector Switch. The multichannel selector switch selected in this design is AD7506, which is a 16-channel multichannel selector switch. Its working principle is that the enabling terminal EN determines the working state of AD7506. When the enable terminal EN is valid, it means that the multichannel selection switch is selected, and EN is active at high level, so when EN is at high level, the AD7506 is in operational condition. The selection of its output channel number is determined by its four-bit address bit A3A2A1A0. The collection control module implemented in this design has 64 collection signal input channels, which are divided into 4 groups, each of which is 16 groups. Four pieces of AD7506 are required to realize the channel selection of 64 analog input signals. 4 groups of signals are, respectively, sent to the A/D converter through an AD7506. The FPGA controls the work of these 4 AD7506s; that is, the FPGA generates the chip select signals and channel selection timing of the 4 AD7506s. The pinout diagram of the multichannel selector switch AD7506 is shown in Figure 3.

3.1.2. A/D Conversion Circuit. In the sampling control module, the function of the A/D conversion circuit is to convert the collected analog signal into a digital signal, so that the subsequent signal processing module can process the converted digital signal accordingly. For an A/D converter, it has two very important performance parameters: conversion speed and conversion accuracy. The conversion speed and accuracy will directly affect the performance of the system, so it is very important to choose an A/D converter with appropriate parameters.

The A/D converter selected in the integrated control module of this design is AD7862 produced by AD Company, which is a dual-channel 12-bit AD conversion chip with fast speed and low power consumption. The A/D converter chip has the following features.

The chip integrates two 12-bit AD converters that can work at the same time, can input 4 channels of analog signals, and can convert two input signals at the same time. The working voltage is 5KV, the sampling rate is 250 kspS, and the conversion time is 4us. The input range of the variable is optional: ±10 V (AD7862-10), ±2.5 V (AD7862-3), and 0–2.5 V (AD7862-2).
The working principle of AD7862 is that the chip integrates two 12-bit AD converters that can work at the same time, so that it can complete the 2 channels of any one of the two groups of AB channel signals (VA1, VA2 and VB1, VB2). The analog signal is sampled at the same time, and the conversion time is 4 us. The A0 pin of the chip is a multi-channel selection signal, and its function is to select the input of the analog signals of the two groups of AB channels. When it is high level, A/D conversion is performed on the 2 input analog signals of the B group channel at the same time. CS is the chip select signal of the chip, which is used to control whether the chip is in working state. RD is the signal read control terminal, which controls the read operation of the signal. That is, the read control of the converted digital signal is completed by CS and RD. When the select signal CS is valid (CS is active low) and RD is active (RD is active low), the digital signal o after AD conversion can be read from the 12-bit data bus at one time.

The working timing diagram of the D converter AD7862 is shown in Figure 4. According to the working timing diagram of AD7862, we can see that when the CONVST signal is on the falling edge, the synchronous track/hold amplifier inside AD7862 will simultaneously maintain the 2-channel input analog signal of group A or group B selected by the A0 signal. At this time, the level of the BUSY pin will change from low level to high level, and the high level will last for 4 us, indicating that A/D conversion is being performed during this period. After the conversion time of 4 us, the level of the BUSY pin will change from high level to low level, indicating that the A/D conversion has been completed, and the data are stored in the output latch at this time. When the chip select signal CS is valid, which means that the AD converter is selected, the signal of the RD pin will control the reading of the converted digital signal. By sending continuous pulses to the RD pin, the converted result can be read; that is, according to whether the multiplexing signal A0 is high level (group B) or low level (group A), the first read pulse after A/D conversion will read the conversion result of VAI or VBI, and the second read pulse will read the conversion result of VA2 or VB2. The result of the read will be read out in one go through the 12-bit data bus.
When the A/D conversion circuit is working, the FPGA-based acquisition control module will generate control signals for AD7862, including chip select signals, multiplex selection signals, read control signals, and CONVST signals, thereby controlling AD7862 to complete the work of analog signals to digital signals conversion. The result after analog-to-digital conversion is read out and sent to the FPGA for processing through a 12-bit data bus.

3.2. Design of Software Part. The software design of the acquisition control module also includes two parts: the multichannel selection module based on FPGA control and the A/D conversion module based on FPGA control.

3.2.1. Multichannel Selection Module Based on FPGA Control. The function of the multichannel selection module based on FPGA control is mainly used to generate the control signals of 4 pieces of AD7506, including the chip selection signal and the four-bit address bit signal. The chip AD7506 performs periodic chip selection. When a certain piece of AD7506 chip is selected, the multichannel selection control module generates a four-bit address bit control signal and selects the channel number to be output according to the four-bit address bit control signal. Thus, each AD7506 can periodically select 16 analog input signals. Figure 5 shows the multichannel selection control module designed and generated in the Quartus II development software. The module has two input signal terminals and two output signal terminals, CLK1 is the clock multiplier input terminal, ENA is the enable signal input terminal, the output terminal INHOUT [3..0] is used to generate a four-bit chip select signal, and the output terminal PORTOUT [3..0] is used to generate the four-bit address bit signal to complete the selection of the output channel.

3.2.2. A/D Conversion Module Based on FPGA Control. The A/D conversion module based on FPGA control is mainly used to generate the control signals of AD7862, including the multiplex selection signal A0, the chip selection signal CS, and the read control signal RD. The AD7862 is controlled to complete the analog-to-digital conversion, and the converted result is read out through the data bus. The A/D conversion control module designed and generated in the QuartusII development software is shown in Figure 6.

There are four input signals and three output signals in this module. CLK is the clock input signal, RST is the reset signal, CONV is the start signal of AD conversion, and BUSY_ADC is the signal that is being converted. CS_ADC, RD_ADC, and AO are used to control the reading of the converted result.

The FPGA-based A/D conversion control module uses a finite state machine (FSM) to generate the working sequence of AD7862. There are 7 states state 0–state 6 in the finite state machine. State 0 is the initial state; that is, the AD7862 is initialized in this state. State 1 is the conversion start state, in which the conversion start signal CONVST is changed from high level to low level, indicating that the conversion starts. In state 2, the BUSY pin level from low level to high level means that the conversion is in progress. In the state 3, the level of the BUSY pin will be judged. If the BUSY pin is high level, it means that the conversion has not ended, and it is necessary to continue to wait for the low level, indicating that the conversion is over. In state 4, it changes the level of CS and RD pins from high level to low level and reads VAI or VB1. In state 5 again, the levels of CS and RD pins are set high. In the state 6, the levels of CS and RD pins are changed from high level to low level again, and VAI2 or VB2 is read out. The state transition diagram of the finite state machine is shown in Figure 7.
4. Conclusion

(1) This paper mainly studies the signal acquisition technology based on FPGA. With the continuous development of FPGA technology, DSP modules are generally integrated in new FPGA chips, and even soft/hard core processors are embedded. Coupled with the advantages of FPGA in signal parallel processing, FPGA is used to realize signal acquisition. It has become possible to control and complete the processing of digital signals. This paper completes the design of the acquisition control module based on FPGA. The hardware part completes the hardware connection between FPGA and AD7862, and the software part completes the design of the multichannel selection module based on FPGA control and the AD conversion module based on FPGA control, thus realizing the FPGA control of multichannel signal acquisition.

(2) At present, the application of FPGA to the field of signal processing has become a development trend, and FPGA has the incomparable advantages of single-chip microcomputer and DSP. This subject has completed the research of FPGA-based signal acquisition technology and designed a FPGA-based control system. Although it can complete the corresponding functions, its performance is not very stable, and there is still a lot of work to be done. The FPGA-based control system can complete the acquisition of multichannel analog signals, the FFT processing of digital signals, and the storage of the processing results. In addition, the system can also expand the function of displaying the processing results, the function of communicating with the PC, and the function of wireless transmission, which are the future research directions of this design.

Data Availability

The figures used to support the findings of this study are included in the article.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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