Parameter Extraction Technique for Evaluation of Inductive and Capacitative Elements of Three-Winding Coupled Inductor

Bilal Ahmad, Member, IEEE, Prasad Jayathurathnage, Member, IEEE, Wilmar Martinez, Senior Member, IEEE, and Jorma Kyyrä, Member, IEEE

Abstract—Wide-bandgap devices have enabled miniaturization of magnetic components to enhance the power density of the converter. However, parasitic components become dominant at higher switching frequencies that actuate unwanted electromagnetic interference issues. Therefore, it is critical to model and evaluate them in compact magnetic structures. Since multiwinding coupled inductive structures are essential part of multiphase converters, this article introduces a measurement method to compute the parasitic elements of a three-winding coupled inductor. Results of the proposed method are verified by measuring the high-frequency emissions of the high-step-up converter with two inductor structures. Both inductors had similar inductances but different physical dimensions. With application of the proposed measurement methodology, parasitic capacitances of both inductors were computed. Results showed that one inductor structure has higher parasitic capacitance than the other. Since high-frequency emissions of the converter directly depend on the parasitic capacitance of the inductor structure, the emission profile of the converter showed that the converter indeed had lower noise peaks when the inductor with lower capacitance was employed. Hence, these results validate the capacitance trend as predicted by the proposed modeling technique. This method can be employed to any multiwinding coupled inductor to compute its parasitics to optimize the required electromagnetic interference filters.

Index Terms—Electromagnetic interference (EMI), gallium nitride (GaN), high-frequency modeling, high-step-up (HSU) converter, three-winding magnetic components, wide-bandgap (WBG) semiconductors.

I. INTRODUCTION

SUPERIOR switching properties of wide-bandgap (WBG) semiconductor devices can enable a power converter to achieve higher conversion efficiencies with smaller cooling and passive component requirement [1]–[5]. However, faster transition times, a characteristic of WBG devices, result in a higher commutation $\frac{dv}{dt}$ and $\frac{di}{dt}$ at switching nodes that may increase the electromagnetic interference (EMI) generation in power converters [6], [7]. Higher EMI would require larger common-mode (CM) and differential-mode (DM) filters to comply with standards, which would be opposed to the objectives of having high efficiency and high power density in the converter, which are essential objectives in modern power electronics applications [8].

It has been shown in [6] that a 50–90% reduction in hard switching losses in variable-speed drives can be achieved by replacing conventional Si devices with WBG devices, although it comes with a disadvantage of 20–30 dB increase in high-frequency noise. The authors of [7], [9], and [10] concluded that EMI generation by GaN switches can be reduced by increasing the gate resistance and, hence, reducing the voltage transition time. However, a higher gate resistor makes switching transition slower. Moreover, if the full fast switching capability of GaN switches were employed, EMI emissions would be drastically increased in comparison to the case of Si-based converters under similar operating conditions. Kim et al. [11] also concluded that by the use of WBG switches in cascaded boost converters, higher EMI is generated in a high-frequency spectrum, and it is emphasized that for converters with WBG switching devices, more attention needs to be paid to methods to reduce the ringing and parasitics in the circuit for EMI reduction. However, for the sake of comparison of WBG devices with Si devices, these studies did not study the EMI generation after optimizing the converter for GaN or SiC devices. As the magnitude of the EMI emissions also depends on the impedance of its propagation path in addition to its sources (switching devices) [12]–[16], it is paramount to study the EMI generation of WBG-based converters with passive components optimized for high-frequency operation.

In [17], CM noise of a boost-type power factor correction circuit is reduced by the application of equivalent parallel capacitance (EPC) of two inversely coupled inductors. Similarly, Fu et al. [18] showed that by reducing the interwinding capacitance (IWC) of a two-winding transformer, CM emissions of an LLC dc–dc converter are attenuated by 52 dB. In [19], it has been demonstrated that by canceling the EPC of a line inductor, emissions can be reduced by 22 dB in the high-frequency region. Hence, it is safe to deduce that parasitic capacitance...
of an inductor or a transformer plays a critical role in propagation of high-frequency noise. However, the magnitude of this capacitance depends on the physical structure and the winding configuration of an inductive component [20]–[23]. Since multiphase coupled inductors offer outstanding advantages by improving efficiency and power density along with reducing the number of required passive components in a power electronics converter [24]–[27], it is vital to have an accurate high-frequency model with emphasis in the capacitive effects for optimizing the power converter design in order to have a high performance.

In addition, ferriteless printed circuit board (PCB) transformers and windings have become an attractive approach for high-frequency and high-power-density converters [28]. Therefore, modeling of high-frequency parasitic capacitances in PCB-based planar transformers is also a critical requirement. For example, Neugebauer and Perreault [28] presented an application of a two-winding coupled air core planar inductor to cancel the parasitic inductance of capacitor to enhance the filter performance for the high-frequency converter. However, EMI emissions revealed that for frequency components beyond 6 MHz, the effectiveness of this technique reduced enormously due to the parasitic capacitances in the inductor structure. Hence, by accurately modeling and minimizing these capacitances during design phase, the operating frequency range of such inductor structures can be increased.

Multiple studies [29]–[37] have presented various modeling techniques, including reluctance models, inductance dual models, gyrator–capacitor models, and extended cantilever to model the inductances in an \( n \)-winding coupled inductor. Calculation of multiple parasitic elements in a two-winding coupled inductor, including turn–turn, layer–layer, layer–core, and winding–winding capacitances, with analytical and empirical formula-based models has been presented in [38] and [39]. It was shown that for a physics-based model, either a lumped-circuit or energy-conservation-based model can be used. However, for both these modeling techniques, exact physical geometry (material of winding insulation, thickness of bobbin, and material of winding separators) must be known. Zhao *et al.* [38], [39] also pointed out that grounding of the magnetic core could result in a 5× to 100× increase in the layer-to-core capacitance. Hence, for accurate modeling of a medium-voltage or high-voltage inductor, grounding of the core cannot be neglected.

An extensive model based on theoretical and experimental parameter extraction of a two-winding coupled toroidal CM choke, including parasitic capacitances, is also presented in [40] and [41], respectively. However, an extensive model with inductances and parasitic capacitances for a multiwinding (more than two windings) coupled inductor is still needed to be addressed. As, it is clear that there is a need for accurate models capable of representing multiwinding magnetic components and their parasitic effects in high frequency with the purpose of reducing EMI emissions in power converters. Hence, in this article, the experimental parameter extraction technique is utilized to develop an inductive and capacitive model of a three-winding inductor with a ladder structure shown in Fig. 1. Since the design example for this study is only restricted to low-voltage applications, grounding of core is not considered in the analysis.

**The major scientific contributions of this study include the following:**

1) a detailed measurement method for extracting the parasitic inductive and capacitive parameters of the complete model of the multiwinding inductors;

2) identification and equivalent/mathematical modeling of eight measurement cases (cf. Figs. 2 and 3) to measure the numerical values of all parasitic elements in a three-winding coupled inductor;

3) systematic analysis of the parasitic effects of the multiwinding coupled inductors with different sizes to evaluate the effects of parasitic components at different switching frequencies; and

4) bringing up important consideration for designing high-frequency power converters with the aim of increasing power density: Have to be careful about parasitics for system-level optimization of power converters with multiwinding coupled inductors.

The rest of this article is organized as follows. Theoretical analysis of the modeling technique is presented in Section II. Section III presents a summary of the selected high-step-up (HSU) converter to validate the modeling technique along with the design methodology of the required inductor structure.
Experimental validation of the proposed model is presented in Section IV. Finally, Section V concludes this article.

II. IMPEDANCE MODEL OF THE THREE-WINDING INDUCTOR

The characterization of a three-winding inductor with its high-frequency effects is discussed in this section. An illustration of a three-winding coupled inductor using an E-core is shown in Fig. 1(a). Note that the terminals of the three windings are named as $i_{a,b}$, where $i$ is the winding number (1, 2, or 3) and the subscript a (or b) represents the same polarity in all windings. This terminology convention will be repeatedly used throughout this article. The equivalent circuit of the high-frequency model of a three-winding inductor is shown in Fig. 1(b), where self-inductances of the windings $L_i$ ($i \in 1, 2, 3$) and mutual inductances between windings $M_{ij}$ ($i, j \in 1, 2, 3$) represent the magnetic interactions between coils. Besides the inductive quantities, parasitic capacitances between different elements that arise from the electric field distribution should be carefully studied in high-frequency applications [42]. The origin of the parasitic capacitance comes from the charge distribution among the winding turns and the core material. In order to model complex distributed capacitances, two main capacitance types are introduced: EPC and IWC. As illustrated in Fig. 1(b), EPC $C_{pi}$ ($i \in 1, 2, 3$) represents the parasitic capacitances between turns in the same winding, while IWC $C_{ij}$ ($i, j \in 1, 2, 3$) represents the distributed capacitances between different windings.

Then, the proposed parameter extraction method in this article is introduced. To this end, low- and high-frequency models are discussed separately. If the frequency is much less than the minimum resonance frequency considering any inductance and capacitance combination, then the impedance of all the capacitances is much larger than that of the inductor. Therefore, all the parasitic capacitances can be considered as open-circuited. Hence, in the low-frequency range, we consider only the self-inductance and mutual inductance for the model. On the other hand, when the frequency is high, both inductances and parasitic capacitances should be taken into account. It should also be noted that all the circuit parameters except the parasitic resistances are assumed to be dispersionless (i.e., the variation of the parameter value with respect to the frequency is negligible).

A. Low-Frequency Model

In this section, the method for estimating self-inductance and mutual inductance using the low-frequency model is discussed. Self-inductances of each winding are measured at low frequency, while all the other windings are kept open. As the measurement frequency is much lower than the resonant frequency, all the windings other than the measured one will have negligibly low coil currents, which makes effects of parasitic capacitances and mutual inductances negligible at the measured frequency. Next, for mutual inductance measurement, four different measurements (namely, test cases a–d) are made with series-connected windings, as illustrated in Fig. 2. Note that the direction of the flux generated by each winding is illustrated with red and blue arrows in Fig. 2. Depending on the generated flux directions in the core, effective inductances of the four test cases can be computed as

$$
L_a = (L_1 + L_2 + L_3) - 2(M_{12} + M_{13} + M_{23})
$$

$$
L_b = (L_1 + L_2 + L_3) - 2(-M_{12} + M_{13} - M_{23})
$$

$$
L_c = (L_1 + L_2 + L_3) - 2(-M_{12} - M_{13} + M_{23})
$$

$$
L_d = (L_1 + L_2 + L_3) - 2(M_{12} - M_{13} - M_{23})
$$

where $L_{a,b,c,d}$ are the measured equivalent inductances of the four test cases a, b, c, and d, respectively. The mutual inductances between three windings (i.e., $M_{12}$, $M_{13}$, and $M_{23}$) can easily be calculated in terms of $L_{a,b,c,d}$ as

$$
M_{12} = \frac{1}{8}(-L_a + L_b + L_c - L_d)
$$

$$
M_{13} = \frac{1}{8}(-L_a - L_b + L_c + L_d)
$$

$$
M_{23} = \frac{1}{8}(-L_a + L_b - L_c + L_d)
$$

B. High-Frequency Model

In this subsection, the high-frequency model of a three-winding inductor is discussed in detail, and the method for calculating the parasitic capacitance is presented. To this end, we performed the impedance analysis of three types of measurements, namely, parallel winding measurements ($m_A$), series winding measurement ($m_B$), and short-circuited winding measurements ($m_C$), as illustrated in Fig. 3. In all the three types of measurements, at least one of the three windings is short-circuited, and the measurement leads are connected across the other two windings. The measurement cases are named to the winding numbers that are connected with the measurement leads, for example, $m_{A,13}$ means that winding 2 is short-circuited and windings 1 and 3 are connected to the measurement leads, as shown in Fig. 3.

For the subsequent impedance analysis, it is assumed that the parasitic effects from connecting wires and measurement leads are negligible. Each measurement test and their equivalent circuit derivations are described as follows.

1) Parallel Winding Measurement Tests ($m_A$): In the parallel winding measurement test, one winding is short-circuited and other two windings are connected in parallel with opposite polarities, while the impedance across parallel connections is measured. For example, the winding configuration for $m_{A,13}$ where the second winding is shorted [see Fig. 4(a)]. The equivalent circuit of $m_{A,13}$ is also shown in Fig. 4(a). For the sake of clarity, connected terminals are illustrated with the same color. With such configuration, equivalent impedance can be simplified to parallel $LC$ connections. The equivalent parallel inductance ($L_{A,ij}$) and capacitance ($C_{A,ij}$) of test case $m_{A,13}$ can be derived as

$$
L_{A,ij} = \frac{L_i L_j - M_{ij}^2}{L_i + L_j + 2M_{ij}}
$$

$$
C_{A,ij} = C_{pi} + C_{pj} + C_{ij} + \frac{C_{ik} C_{jk}}{C_{ik} + C_{jk}}
$$

where subscripts $i$ and $j$ correspond to the measured windings, while subscript $k$ corresponds to the short-circuited winding.
2) Series Winding Measurement Tests ($m_B$): Similarly, in the series winding measurement test, one winding terminal is short-circuited, while the other two windings are connected in series. The equivalent circuit of an example configuration $m_{B,13}$ is illustrated in Fig. 4(b). Similar to the previous case, the circuit can be represented as a parallel $LC$ circuit, and the equivalent inductance and the capacitance can be derived as

$$L_{B-ij} = \frac{L_i L_j - M_{ij}^2}{L_i + L_j - 2M_{ij}}$$

$$C_{B-ij} = C_{ij} + \frac{C_{ik} C_{jk}}{C_{ik} + C_{jk}} + \frac{C_{pi} C_{pj}}{C_{pi} + C_{pj}}$$

where the measurement leads are connected to windings $i$ and $j$, while the winding $k$ is short-circuited.

3) Short-Circuit Winding Measurement Tests ($m_C$): Finally, during the short-circuited winding measurement test, all the winding terminals are short-circuited and the measurement leads are connected to two windings, as shown in Fig. 4(c). In this measurement configuration, all the inductances are short-circuited and the equivalent circuit turns out to be completely capacitive. The equivalent capacitance $C_{C-ij}$ can be written as

$$C_{C-ij} = C_{ij} + \frac{C_{ik} C_{jk}}{C_{ik} + C_{jk}}$$

where the indexes $i, j,$ and $k$ have the same meaning as the previous test cases.

After solving (4), (6), and (7) for all terminal connections, equations to estimate EPCs ($C_{pi}$) and IWCs ($C_{ij}$) are formed and shown in (8) and (9), respectively:

$$C_{pi} = \frac{1}{2} (C_{A-ij} + C_{A-ik} - C_{A-jk}
- C_{C-ij} - C_{C-ik} + C_{C-jk})$$

$$C_{ij} = \frac{2 \prod_{mn} C_{x_{mn}} (C_{x_{jk}} C_{x_{ik}} - C_{x_{ij}} (C_{x_{jk}} + C_{x_{ik}}))}{\sigma_1 - 2(\gamma_{12} + \gamma_{23} + \gamma_{13})}$$

where

$$\sigma_1 = C_{x_1^2} C_{x_{13}^2} + C_{x_2^2} C_{x_{23}^2} + C_{x_2^2} C_{x_{13}^2},$$

$$\gamma_{12} = C_{x_1^2} C_{x_{13}^2} C_{x_{23}},$$

$$\gamma_{23} = C_{x_1^2} C_{x_{13}^2} C_{x_{23}},$$

$$C_{x_{mn}} = C_{B-mn} - C_{C_{pm} + C_{pm}},$$

and $mn \in \{12, 13, 23\}$.

The detailed measurement procedure which is also shown in Fig. 5 is explained with a design example in the following sections.

III. DESIGN EXAMPLE OF A THREE-WINDING INDUCTOR IN AN HSU CONVERTER

To evaluate and verify the aforementioned model of a multiwinding inductor and the proposed measurement technique, an HSU two-phase interleaved boost converter with a three-winding coupled inductor is chosen. The detailed analysis of the HSU converter topology is presented in [43]. In this section, the converter operation and design of required inductor structure has been presented.

A. Converter Topology and Operation

This converter requires a magnetically coupled inductor composed of three windings in a single core. To achieve this specific
magnetic integration, a three-leg magnetic structure is used. Such an structure can be achieved with different core shapes, including EI, EE, EER, EC, etc. In these shapes, each winding is possible to be installed in each leg of the core. The external windings are directly coupled to each other, and an air gap may be installed in each external leg in order to suppress dc flux induction. The converter topology with the required inductor structure is shown in Fig. 6.

Each external winding, $L_1$ and $L_3$, is connected to the power source, and the central winding $L_C$ is located between the cathodes of $D_1$ and $D_2$.

In this converter, the turn ratio between the central winding $N_C$ and the external windings $N_e$ is defined as $N$, assuming $N_e = N_1 = N_3$. This converter has a high voltage gain due to the presence of the central winding in the coupled inductor and its location between the diodes. This central winding is influenced by the magnetic fluxes produced by the external windings that are directly coupled, as seen in Fig. 7.

### B. Inductor Design

As presented in [43], this HSU converter has a particular current ripple behavior, due to the special structure of the coupled inductor, and thereby, a particular flux operation is present in the magnetic core. Both electrical and magnetic operations in the converter are important for the coupled inductor design because the ripple current in the windings and the magnetic flux in the core should be limited to avoid wire overcurrents and magnetic saturation in the core. In this context, the design procedure is based on the maximum output power and the ratio of inductor ripple current as follows.

**Step 1:** After extracting the parameters and constructing the magnetic and electrical models of the three-winding coupled inductor, the flux variations in each duty cycle mode are obtained, and therefore, the ripple current $I_{ripp}$ can be extracted, as presented in [43]:

$$I_{ripp-d<0.5} = \frac{(1 + 2N)(1 - 2D)}{(L + M)((1 + N) - D(1 + 2N))}V_iDT_s$$  \hspace{1cm} (10)

$$I_{ripp-d>0.5} = \frac{2D - 1}{D(L + M)}V_iDT_s$$  \hspace{1cm} (11)

where $D$ is the duty cycle of both semiconductor switches, $L$ and $M$ are the self-inductance and mutual inductance of both external windings, respectively, and $T_s$ is the switching period.

According to the duty cycle cases (lower or higher than 0.5), the maximum output power is calculated and the ratio of the inductor ripple current is decided from the point of view of the output power. With such variations, the ratio between the magnetic reluctance of central leg $R_{mc}$ and external leg $R_{mo}$ is calculated from the core geometry. Such a ratio also implies the derivation of the coupling factor between the windings. Detailed information can be found in [43].

**Step 2:** Once the suitable ratio of magnetic reluctances for a defined set of specifications is defined, the next point is to determine the number of turns of the windings. Such number of turns and the ratio between external and central turns are selected based on the condition of not exceeding the maximum flux in each leg, which was found in Step 1. Detailed information about this step can be found in [44].

**Step 3:** With the number of turns defined, the magnetic reluctances are also calculated using several possible air-gap lengths depending on the selected magnetic material. To validate the suitable parameters of $R_{mo}$ and $R_{mc}$ values from the prototype, the classic reluctance calculations can be used

$$R_{mc} = \frac{l_e}{\mu_0\mu_r A_e} + \frac{l_g}{\mu_0 A_e}$$  \hspace{1cm} (12)
Steps 1–3 are iteratively conducted until suitable values of reluctances and number of turns are obtained keeping the rules of not exceeding maximum fluxes and maximum current ripples.

**Step 4:** Each inductance (mutual, leakage, and self) value is validated based on the selected values from steps 1–3. After several iterations and once the design meets the specifications and constraints defined by the designer, it can be constructed and tested. For this specific case, the inductors designed and constructed were validated with test as it is presented in the next section.

### IV. Experimental Validation

The high-frequency emissions of a converter depend on the magnitude of the parasitic elements of the inductor [23], [45]. Hence, to demonstrate the application of the modeling technique presented in this article, EMI measurements of the HSU converter (cf. Section III) with two different inductor designs are performed. This section first presents the design procedure of the inductor prototypes considering the specifications and evaluation of their parasitic elements and then compares the EMI results of the HSU converter with both designed inductors at different switching frequencies.

#### A. Design of Inductor Prototypes

For the converter parameters given in Table I, two inductor structures with identical magnetic parameters but with different physical dimensions are designed by following the procedure explained in Section III-B. Both inductor prototypes are shown in Fig. 8, and their parameters are summarized in Table II.

#### B. Parameter Extraction

Once the inductor prototypes are constructed, self-inductances of each winding and the mutual inductances between them are measured considering the low-frequency model using an LCR meter, and they are presented in Table IV. Next, the equivalent capacitances are estimated by performing the measurements described in Section II. First, impedance parameters of different test configurations are measured using a network analyzer (R&S ZND). Real and imaginary components of the measured impedance parameters are then plotted against the frequency to verify that their profile is same as the equivalent impedance presented in Section II. Next, measured impedance curves for series and parallel winding test cases (i.e., m_A and m_B) are fitted with the general impedance equation of parallel resonant RLC circuit to estimate the EPCs of the rest cases [i.e., capacitances in (4) and (6)]. During this curve fitting, measured self-inductance and mutual inductance are used to increase the accuracy of the curve fitting. The measured and estimated (using curve fitting) impedance profiles for both inductors are shown in Figs. 9 and 10. Next, the equivalent capacitances of the short-circuit winding measurement test is measured using the LCR meter.

It can be seen that the estimated impedance characteristics with equivalent inductance and capacitance values coincide accurately with the measured results. It must be noted that for each
TABLE III
MEASURED EQUIVALENT CAPACITANCE FOR ALL TEST CASES

| Case   | ETD59 | ETD49 |
|--------|-------|-------|
| CA-13  | 19.6  | 22.6  |
| CA-23  | 24.2  | 26.9  |
| CA-12  | 24.0  | 25.8  |
| CB-13  | 20.9  | 20.3  |
| CB-23  | 22.2  | 20.8  |
| CB-12  | 23.1  | 22.1  |
| CC-13  | 5.9   | 6.3   |
| CC-23  | 8.9   | 8.8   |
| CC-12  | 8.8   | 8.5   |

TABLE IV
MEASURED PARAMETERS OF INDUCTORS

|                      | ETD59 | ETD49 |
|----------------------|-------|-------|
| Self Inductance - L1 | 313.9 | 300.6 |
| L2                   | 1.6   | 1.6   |
| L3                   | 304.1 | 305.2 |
| Mutual Inductance - M12 | 386.9 | 398.7 |
| M23                  | 417.4 | 402.2 |
| M13                  | 32.5  | 32.2  |
| EPC - C P1           | 6.8   | 7.8   |
| C P2                 | 8.4   | 9.6   |
| C P3                 | 6.8   | 8.5   |
| Inter-Winding Capacitance - C 12 | 8.9 | 8.5 |
| C23                  | 8.8   | 8.8   |
| C31                  | 5.9   | 6.3   |

Fig. 10. Measured and estimated impedance profiles for test cases A and B (m_A and m_B) (ETD-49).

Once values of equivalent capacitances for all test cases are known, values of C_{pi} and C_{ij} for all three windings are calculated using (8) and (9) and summarized in Table IV. It can be easily seen that the EPC of the smaller core type (ETD49) is noticeably higher than that of the larger core type (ETD 59) due to the compact turn distribution in the smaller core. On the other hand, IWCs are almost comparable for both types of cores, which could be due to twofold effects: a larger gap between windings reduces the IWC, while a large area of the core legs increases the IWC.

C. Conducted Emission Measurement

Conducted high-frequency noise of the HSU converter (cf. Fig. 7) is measured by a test setup shown in Fig. 11. A 5-μH line impedance stabilization network (LISN) with 50-Ω output impedance and a spectrum analyzer are utilized to view the frequency spectrum of conducted noise. Operation parameters of the HSU converter are kept same for all the test cases (cf. Table I). Frequency range of 150 kHz–50 MHz for emissions measurement is selected, as the purpose of noise measurements is not to check the compliance with certain EMI standard but to demonstrate the effect of inductor parasitics on noise peaks. A 20-dBm attenuator is used in all measurements at the input of the spectrum analyzer for its channel protection. Emissions with both inductor designs at switching frequencies of 500 kHz, 750 kHz, and 1 MHz are shown in Figs. 12–14, respectively.

It must be noted that both inductors (cf. Fig. 8) are designed for the HSU converter operation at a switching frequency of 500 kHz. As required inductance to ensure that input current ripple does not exceed over 20% of input current at 750 kHz and 1 MHz would be lesser than the inductance required at 500 kHz, hence the number of turns could have been reduced. But for the sake of comparison of their conducted emissions, all tests are performed with same inductor designs while ensuring that magnetic cores do not saturate.
Fig. 13. Conducted emissions at the switching frequency of 750 kHz.

Fig. 14. Conducted emissions at the switching frequency of 1 MHz.

Fig. 15. Difference between emissions of the converter with inductors ETD49 and ETD59.

To help visualize the results, converter emissions with inductor ETD59 [cf. Fig. 8(a)] are subtracted from emissions with inductor ETD49 [cf. Fig. 8(b)] and are presented in Fig. 15. Since ETD49 has higher EPC than ETD59 (cf. Table IV), it can be seen that it also has higher noise peaks. Especially beyond the frequency range of 20 MHz, difference between their noise peaks becomes more evident. It can also be seen that as the switching frequency increases from 500 kHz to 1 MHz, difference in between noise peaks of two inductors is also increased. Especially around the frequency range of 40 MHz in Fig. 15, noise difference has been increased from almost 15 dB-μV at the switching frequency of 500 kHz to 20 dB-μV at the switching frequency of 1 MHz.

V. CONCLUSION

This article proposes a modeling methodology for multiwinding coupled inductors, including high-frequency effects. A series of high-frequency impedance measurements with different terminal connections were performed on a three-winding coupled inductor to evaluate its parasitic capacitances. It should be noted that the proposed empirical method can be applied to an arbitrary multiwinding coupled inductor. However, the number of test cases increases linearly with the increase in the number of windings, which may necessitate automated measurement rig for such a higher number of measurements. On the other hand, the proposed method can readily be applied with two-winding coupled inductors.

Two inductor prototypes with identical magnetic design and different physical dimensions were designed and constructed to validate the proposed modeling technique. Measured impedances and equivalent estimated impedance profiles for all measurement test cases of both inductors have shown to match with a very minimal error up to 30 MHz. Results showed that ETD-49 has higher parasitic capacitance than that of ETD-59. High-frequency emissions of the converter are directly related to the parasitic capacitance of the inductor. Hence, to verify the results, conducted emissions of an HSU converter with GaN switching devices were measured at three different switching frequencies (500 kHz, 750 kHz, and 1 MHz), and tests were conducted for both inductor designs. EMI measurements validated that when the inductor with higher parasitic capacitance is employed, the converter has indeed higher noise peaks. This validates the trend of capacitances as predicted by the proposed modeling technique.

It has been shown that when using a smaller inductor (core type ETD49) and higher EPC, the converter presents higher noise peaks compared to a larger inductor (core type ETD59) with lower EPC. The difference between noise emissions becomes prominent when the converter’s switching frequency is increased, resulting in larger EMI filter requirements to comply with standards. The results of this study show that although ETD49 has twice the power density of ETD59, it is very critical to optimize the high-frequency parasitic elements of the inductor structure for the overall system optimization of the high-frequency converter. Therefore, the study of this article brings up a vital consideration of parasitic effects in designing high-power density converters, in particular, operating at high switching frequencies. The proposed parasitic capacitance estimation method is not only limited to three-winding inductors, but can, in principle, be applied to arbitrary multiwinding inductors. This article also provides required tools to compute and optimize the parasitics of multiwinding coupled inductor structures to enhance the high-frequency performance of the converter.
REFERENCES

[1] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, “SiC versus Si—Evaluation of potentials for performance improvement of inverter and dc/dc converter systems by SiC power semiconductors,” IEEE Trans. Ind. Electron., vol. 58, no. 7, pp. 2872–2882, Jul. 2010.

[2] M. Chintalvali, P. Otaduy, and B. Ozpineci, “Comparison of Si and SiC inverters for IPM traction drive,” in Proc. IEEE Energy Convers. Congr. Expo., 2010, pp. 3360–3365.

[3] J. Millán, P. Godignon, X. Perpiñá, A. Pérez-Tomás, and J. Rebollo, “A survey of wide bandgap power semiconductor devices,” IEEE Trans. Power Electron., vol. 29, no. 5, pp. 2155–2163, May 2014.

[4] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, and D. J. Costinet, “Evaluation of switching performance of SiC devices in PWM inverter-fed induction motor drives,” IEEE Trans. Power Electron., vol. 30, no. 10, pp. 5751–5759, Oct. 2014.

[5] F. Xue, R. Yu, and A. Q. Huang, “A 98.3% efficient GaN isolated bidirectional dc/dc converter for DC microgrid energy storage system applications,” IEEE Trans. Ind. Electron., vol. 64, no. 11, pp. 9094–9103, Nov. 2017.

[6] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark, “An experimental investigation of the tradeoff between switching losses and EMI generation with hard-switching in Si, Si-SiC, and all-SiC device combinations,” IEEE Trans. Power Electron., vol. 29, no. 5, pp. 2393–2407, May 2013.

[7] D. Han, S. Li, W. Lee, W. Choi, and B. Sarlioglu, “Trade-off between switching loss and common mode EMI generation of GaN devices-analysis and solution,” in Proc. IEEE Appl. Power Electron. Conf. Expo., 2017, pp. 843–847.

[8] M. Pahlevanizhad, D. Hamza, and P. K. Jain, “An improved layout strategy for common-mode EMI suppression applicable to high-frequency planar transformers in high-power dc/dc converters used for electric vehicles,” IEEE Trans. Power Electron., vol. 29, no. 3, pp. 1211–1228, Mar. 2014.

[9] M. Tian et al., “EMI modeling and experiment of a GaN based LLC half-bridge converter,” in Proc. 9th Int. Conf. Power Electron. ECCE Asia, 2015, pp. 1961–1966.

[10] D. Han, S. Li, Y. Wu, W. Choi, and B. Sarlioglu, “Comparative analysis on conducted CM EMI emission of motor drives: WBG versus Si devices,” IEEE Trans. Ind. Electron., vol. 64, no. 10, pp. 8353–8363, Oct. 2017.

[11] T. Kim, D. Feng, M. Jang, and V. G. Agelidis, “Common mode noise analysis for cascaded boost converter with silicon carbide devices,” IEEE Trans. Power Electron., vol. 32, no. 3, pp. 1917–1926, Mar. 2017.

[12] H. Zhang, L. Yang, S. Wang, and J. Puukko, “Common-mode EMI noise modeling and reduction with balance technique for three-level neutral point-clamped topology,” IEEE Trans. Ind. Electron., vol. 64, no. 9, pp. 7563–7573, Sep. 2017.

[13] Z. Zhang, B. He, D.-D. Hu, X. Ren, and Q. Chen, “Common-mode noise modeling and reduction for 1-MHz eGaN multisetup dc-dc converters,” IEEE Trans. Power Electron., vol. 34, no. 4, pp. 3239–3254, Apr. 2019.

[14] Y. D. Huang, F. C. Lee, and Q. Li, “Analysis and reduction of common mode EMI noise for resonant converters,” in Proc. IEEE Appl. Power Electron. Conf. Expo., 2014, pp. 566–571.

[15] P. Kong, S. Wang, F. C. Lee, and Z. Wang, “Reducing common-mode noise in two-switch forward converter,” IEEE Trans. Power Electron., vol. 26, no. 5, pp. 1522–1533, May 2011.

[16] Y. P. Chan, B. M. H. Pong, N. K. Poon, and J. C. P. Liu, “Common-mode noise cancellation in switching-mode power supplies using an equivalent-transformer modeling technique,” IEEE Trans. Electromagn. Compat., vol. 54, no. 3, pp. 594–602, Jun. 2012.

[17] S. Wang and F. C. Lee, “Common-mode noise reduction for power factor correction circuit with parasitic capacitance cancellation,” IEEE Trans. Electromagn. Compat., vol. 49, no. 3, pp. 537–542, Aug. 2007.

[18] D. Fu, S. Wang, P. Kong, F. C. Lee, and D. Huang, “Novel techniques to suppress the common-mode EMI noise caused by transformer parasitic capacitances in dc-dc converters,” IEEE Trans. Ind. Electron., vol. 60, no. 11, pp. 4968–4977, Nov. 2013.

[19] S. Wang, F. C. Lee, and J. D. Van Wyk, “Inductor winding capacitance cancellation using mutual capacitance concept for noise reduction application,” IEEE Trans. Electromagn. Compat., vol. 48, no. 2, pp. 311–318, May 2006.

[20] P. Kong and F. C. Lee, “Transformer structure and its effects on common mode EMI noise in isolated power converters,” in Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo., 2010, pp. 1424–1429.
[45] S. Wang, F. C. Lee, and W. G. Odendaal, “Characterization and parasitic extraction of EMI filters using scattering parameters,” IEEE Trans. Power Electron., vol. 20, no. 2, pp. 502–510, Mar. 2005.

Bilal Ahmad (Member, IEEE) received the B.Sc. degree in electrical engineering from the University of Engineering and Technology, Lahore, Pakistan, in 2013, and the M.Sc. degree in electrical engineering with specialization in power electronics in 2016 from Aalto University, Espoo, Finland, where he is currently working toward the Doctorate degree in power electronics.

He is part of Industrial Electronics and Electric Drives Research Group, Aalto University. His research interests include practical challenges in implementation of high-frequency, power-dense, and highly efficient power electronics converters. His research activities also include optimization of parasitic elements in magnetic components for reduction of high-frequency noise from converters.

Prasad Jayathurathnage (Member, IEEE) received the B.Sc. degree in electronics and telecommunications engineering from the University of Moratuwa, Moratuwa, Sri Lanka, in 2009, and the Ph.D. degree in electrical and electronic engineering from Nanyang Technological University, Singapore, in 2017.

He is currently a Postdoctoral Researcher with Aalto University, Espoo, Finland. He has worked at the Queensland University of Technology, Brisbane, QLD, Australia, and Rolls-Royce@NTU Corporate Laboratory, Singapore. His research interests include high-frequency power converters and wireless power transfer.

Wilmar Martínez (Senior Member, IEEE) received the M.Sc. degree in electrical engineering from the Universidad Nacional de Colombia, Bogotá, Colombia, in 2013, and the Ph.D. degree in power electronics from Shimane University, Matsue, Japan, in 2016.

He was a Commissioning Scientist with the Toyota Technological Institute, Nagoya, Japan, in 2016, and a Postdoctoral Researcher with Aalto University, Espoo, Finland, in 2017. In 2018, he was a Visiting Researcher with the Power Electronic Systems Group, ETH Zürich, Zürich, Switzerland. Since 2018, he has been an Assistant Professor with the Department of Electrical Engineering, Katholieke Universiteit Leuven, Diepenbeek, Belgium.

Jorma Kyyrä (Member, IEEE) received the M.Sc., Lic.Sc., and D.Sc. degrees in electrical engineering from Aalto University, Espoo, Finland, in 1987, 1991, and 1995, respectively.

Since 1985, he has been with Aalto University in various positions. He has been an Associate Professor of Power Electronics and a Professor of Power Electronics with Aalto University since 1996 and 1998, respectively. From 2008 to 2009, he was the Dean of the Faculty of Electronics, Communications and Automation, Aalto University, where he is currently the Head of the Department of Electrical Engineering and Automation. From 2009 to 2011, he was the Vice-President of Aalto University. His research interests include power electronics at large. The power electronics group at Aalto University has expertise, e.g., in power electronics for ac drives, dc–dc converters, modeling of converters, filtering of electromagnetic interference, power factor correction, and distributed power systems.