VLSI Implementation of Fault Tolerance Multiplier based on Reversible Logic Gate

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Abstract. Multiplier is one of the essential component in the digital world such as in digital signal processing, microprocessor, quantum computing and widely used in arithmetic unit. Due to the complexity of the multiplier, tendency of errors are very high. This paper aimed to design a 2x2 bit Fault Tolerance Multiplier based on Reversible logic gate with low power consumption and high performance. This design have been implemented using 90nm Complementary Metal Oxide Semiconductor (CMOS) technology in Synopsys Electronic Design Automation (EDA) Tools. Implementation of the multiplier architecture is by using the reversible logic gates. The fault tolerance multiplier used the combination of three reversible logic gate which are Double Feynman gate (F2G), New Fault Tolerance (NFT) gate and Islam Gate (IG) with the area of 160µm x 420.3µm (67.25 mm\textsuperscript{2}). This design achieved a low power consumption of 122.85µW and propagation delay of 16.99ns. The fault tolerance multiplier proposed achieved a low power consumption and high performance which suitable for application of modern computing as it has a fault tolerance capabilities.

1. Introduction
In advanced technology, the requirement to design a basic components such as multiplier with high speed, low power consumption and low area is an essential as multiplier massively used in arithmetic logic unit, microprocessor and various applications. To fulfill this, implementation using a compact Very Large Scale Integration (VLSI) could contribute to the needs. VLSI allows thousands of transistors into a single chip. It gave a huge impact in semiconductor industries and many more recent technologies [2].

The main parameter to determine the performance of the multiplier is by adding the number of partial products in parallel multipliers. There are few techniques to perform multiplication operation such as Array multiplier, Wallace Tree multipliers and Booth Multiplier. These techniques suitable for hardware implementation of binary multiplier using Complementary Metal Oxide semiconductor (CMOS) technology [1][4][5]. The choice of the approaches depending on the latency, design complexity, throughput and area. Array or tree of full adder’s architecture to sum partial products is used to obtain an efficient parallel multiplier.
One of the techniques to design a multiplier is by using the reversible logic which able to optimize the power [6], [9], [10] and increase the performance [7]. In [7], they implemented the 4x4 bit reversible fault tolerant multiplier circuit using VHIC hardware description language (VHDL) with the propagation delay of 19.1ns. The reversible fault tolerant multiplier in [8] used Urdhva Tiyagbhayam aphorisms from the ancient Vedic Mathematics to improve the speed.

2. 2x2 bit fault tolerance multiplier architecture

The proposed fault tolerance multiplier consist of three types of reversible logic gates [3] which are Double Feynman Gate (F2G), New Fault Tolerance Gate (NFT) and Islam Gate (IG). A reversible logic gate has equal number of input and output terminals and there is one to one mapping between them. A gate or a circuit is called reversible if there is a one-to-one correspondence between its input and output patterns. The reversible logic computation means the input can be recovered back from the output and the output can be obtained from the input or also known as loss-less logic.

There are two types of reversible logic which is Basic Reversible gate and Fault tolerance gate. Fault-tolerance is the property that enables a system to operate even if there is the present of error. The circuit of the multiplier is shown in Figure 1. Pin G is a garbage bits which is an additional outputs that is not used for further computation. When multiplying 2 numbers, there will be a partial product (P). P0 is obtained by vertical multiplication of A0 and B0. Then P1 is obtained by the crosswise multiplication and addition of the partial products are A1B0 and A0B1. P2 is obtained by the multiplication of A1 and B1. Finally P3 is obtained from the carry generated from the calculation of P2. P3 represent the final result term. The multiplier is implemented using fault tolerant reversible gates (also known as parity preserving gates).

Fault tolerant reversible gate exhibits a fault tolerant property. If the system itself composed of fault tolerant gate then it exhibits a fault tolerant property because it preserves a parity and provides a fault detection at the primary output and no intermediates checking is required. The fault tolerant reversible implementation of logical expression uses fault tolerant gates or parity preserving gates which are four double Feynman gates, four NFT and two IG to implement 2x2 bit multiplier. The simplified equations on how to obtain P0, P1, P2 and P3 is shown in (2.1).

\[
P0 = A0 \cdot B0 \\
P1 = A1 \cdot B0 \oplus A0B1 \\
P2 = A0 \cdot A1 \cdot B0 \cdot B1 \oplus A1B1 \\
P3 = A0 \cdot A1 \cdot B0 \cdot B1 \text{ (carry generated from } P2) \tag{1}\]

\([\text{P}0=\text{A0} \cdot \text{B}0] \]
\([\text{P}1=\text{A1} \cdot \text{B}0 \oplus \text{A0B}1] \]
\([\text{P}2=\text{A0} \cdot \text{A1} \cdot \text{B}0 \cdot \text{B}1 \oplus \text{A1B}1] \]
\([\text{P}3=\text{A0} \cdot \text{A1} \cdot \text{B}0 \cdot \text{B}1 \text{ (carry generated from } P2)\] (1)
2.1. Double Feynman Gate (F2G)

Double Feynman Gate (F2G) is a 3x3 gate where the input are A, B and C and the output are P, Q and R which uses the combination of XOR gate [3]. Figure 2 (a), (b) and (c) show the Double Feynman Gate (F2G) block diagram, transistor level diagram and layout, respectively.

(a).
2.2 New Fault Tolerance Gate (NFT)
New Fault Tolerance Gate (NFT) is a 3x3 gate which the input are A, B and C and the output are P, Q and R. It can perform NOT, OR, XOR, NAND and AND function. It used the combination of XOR gate, NOT gate and AND gate. Figure 3 (a), (b) and (c) show the New Fault Tolerance (NFT) gate block diagram, transistor level diagram and layout, respectively.
Figure 3. New fault tolerance gate (NFT) (a) block diagram, (b) transistor level diagram and (c) layout

2.3 Islam Gate (IG)
Islam Gate (IG) is a 4x4 gate which the input are A, B, C and D and the output are P, Q, R and S. It can perform XOR and AND function. Figure 4(a), (b) and (c) show the Islam gate block diagram, transistor level diagram and layout, respectively.
3. Results and discussion

The design simulation was run on the Synopsys Simulation and Analysis Environment (SAE). The simulation is carried out using 1.2V supply voltage with a load capacitor of 1fF. The 2x2 bit fault tolerance multiplier circuit consists of 102 PMOS and 102 NMOS, thus the total number of transistor is 204 transistors. Based on the observation from the output simulation waveforms of the circuit as shown in Figure 5, when the input $A_0= A_1= B_0= B_1= 1$, the output of the multiplier is $P_0=1$, $P_1=0$, $P_2=0$ and $P_3=1$. This obtained result from the simulation matched with the 2x2 multiplier truth table in Table 1. From the simulation, the power consumption was measured from the average output voltage with the average input current of the circuit. The voltage is 1.05mV and the current is 117mA make the total power consumption is 122.85uW and the total propagation delay is 16.99ns.

![Diagram](image)

Figure 4. Islam gate (IG) (a) block diagram, (b) transistor level diagram, and (c) layout
Figure 6 shows the layout of the 2x2 bit fault tolerance multiplier circuit with the area of 160µm x 420.3µm (67.25 mm²).

![Diagram of 2x2 bit fault tolerance multiplier circuit]

**Figure 5. Output waveform of the 2x2 bit fault tolerance multiplier**

**Table 1. Truth Table of 2x2 Bit Multiplier**

| A0 | A1 | B0 | B1 | P0 | P1 | P2 | P3 |
|----|----|----|----|----|----|----|----|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |
| 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  |
| 0  | 1  | 1  | 0  | 0  | 0  | 0  | 0  |
| 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  |
| 1  | 0  | 0  | 1  | 0  | 0  | 0  | 1  |
| 0  | 1  | 1  | 0  | 0  | 0  | 1  | 0  |
| 0  | 1  | 1  | 1  | 0  | 0  | 1  | 1  |
| 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| 1  | 0  | 1  | 0  | 0  | 0  | 1  | 0  |
| 1  | 0  | 1  | 1  | 0  | 1  | 1  | 0  |
| 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0  |
| 1  | 1  | 0  | 1  | 0  | 0  | 1  | 1  |
| 1  | 1  | 0  | 0  | 1  | 1  | 0  | 0  |
| 1  | 1  | 1  | 1  | 1  | 0  | 0  | 1  |
Figure 6. 2x2 bit fault tolerance multiplier layout

4. Conclusion
The proposed 2x2 bit fault tolerance multiplier based on reversible logic gate achieved a power consumption of 122.85µW and propagation delay of 16.99ns with the area of 160µm x 420.3µm (67.25 mm²). This design achieved a low power consumption and high performance which is suitable for application of modern computing which requires a fault tolerance capabilities.

Acknowledgement
This work was financial supported by RAGS Grant Vot Number R067.

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