Impedance modeling and analysis of multi-stacked on-chip power distribution network in 3D ICs

Yang Wang1 · Gang Dong1 · Wei Xiong1 · Dongliang Song1 · Zhangming Zhu1 · Yintang Yang1

Received: 17 May 2022 / Accepted: 1 September 2022 / Published online: 16 September 2022
© The Author(s), under exclusive licence to Springer Science+Business Media, LLC, part of Springer Nature 2022

Abstract
An accurate impedance modeling of a multi-stacked on-chip power distributed network (PDN) based on through-silicon-vias (TSVs) is vitally important to estimate the electrical performance in three-dimensional integrated circuits (3D ICs). This paper proposes a method for calculating the impedance matrix of the multi-stacked on-chip PDN, which mainly consists of arbitrarily distributed TSVs and grid-type on-chip PDNs. First, a real stack-up structure of a multi-stacked on-chip PDN is separated into discrete components intentionally. Then, the equivalent lumped circuit models of all discrete components are assembled into a whole to build the transmission matrix of the multi-stacked on-chip PDN through the relationship between the nodal voltage and the nodal current. Finally, the impedance matrix can be derived through the transmission matrix. In this paper, the coupling of the arbitrarily distributed TSVs and the distributional effect of the on-chip PDN are considered in the impedance matrix through the transmission matrix method (TMM). The proposed method replaces the simulation of the complex equivalent circuit model with the matrix calculation. The verification results show that the deviation of resonant frequency is about 6% and the conversation of the simulation time is about 99.9% compared with the HFSS model. It can accurately and quickly calculate the impedance of the multi-stacked on-chip PDN.

Keywords Multi-stacked on-chip PDN · TSV array · Coupling · Transmission matrix method

1 Introduction

In recent years, with the rapid development of electronic terminals, electronic systems have developed toward higher speed, higher bandwidth, lower power consumption, and so on. Three-dimensional integrated circuits (3D ICs) are widely used for some unique advantages, such as shorter interconnection and heterogeneous integration [1–3]. But the problems such as signal integrity (SI), power integrity (PI), and electromagnetic interference (EMI) become more and more serious in the higher frequency systems [4]. Simultaneous switching noise (SSN) often leads to unwanted noise in power distribution networks (PDNs), and then, the induced power supply fluctuation will cause problems with signal integrity in the system. A major challenge faced by 3D ICs is how to deliver clean power to the active circuits, especially on the topmost chip [5]. Fundamentally, PDN systems have a low value of the impedance in the frequency range of interest to effectively reduce noise. The low-frequency impedance is principally determined by off-chip components in 3D ICs, while the high-frequency impedance is determined by the multi-stacked on-chip structure concerned in this paper [6–8]. Through-silicon-vias (TSVs) penetrating the stacked chips act as key interconnect channels to connect stacked chips and thus realize the circuit conduction as shown in Fig. 1. These chips may have different functions to implement a heterogeneous system. The power and ground TSVs, respectively, connect on-chip PDNs that consist of the multilayer power and ground grid metal into a whole as the important electrical pathways to supply the power source for active circuits.

A compact and accurate impedance modeling can help optimize power distribution networks during the early stages of design. The primary objective is to develop an accurate and quick model to predict the PDN impedance. On-chip PDN conditions such as the effective inductance and capacitance at the active circuit affected by the size of the PDN and the number and position of TSVs are very important to precisely evaluate the impedance of 3D stacked on-chip
PDNs. As the frequency is closing to a higher value (GHz), even a small TSV inductance can produce several numbers of high impedance peaks induced by the parallel resonances of the TSV and on-chip PDN inductances and capacitances [9]. It will induce a larger noise near the frequency point of the peak impedance. In 3D PDNs, a large number of TSVs are placed in the Si substrate. Multiple and randomly located ground TSVs may be shared by multiple power TSVs in the TSV array. The coupling between P/G TSVs which is affected by the number and distribution of TSVs cannot be ignored because it seriously influences on the power supply noise [10]. In the previous analysis, a uniform distribution of power/ground TSVS (P/G TSVs) was assumed frequently. Although a uniform distribution is preferable to suppress the worst voltage drop in 3D PDNs, it may not be a practical design choice due to the area constraint. In some designs, TSVs are only assigned in the whitespace around circuit modules [11, 12]. Too many TSVs in the whitespace will increase the size of the die and may cancel out their benefits. So minimizing the number of TSVs is an important goal for the optimization of PDNs during the design flow. It brings difficulties to obtain and analyze 3D PDN impedance because there exists complicated electromagnetic coupling among TSVs. Knowing the effect of the number and assignment of P/G TSVs on the impedance in advance is helpful to minimize the number of TSVs at the beginning of the design.

A considerable CPU run time is required to analyze the complex multi-stacked on-chip PDN structure through finite element simulation software such as ANSYS HFSS. Many published studies have reported the impedance models of PDN systems rather than finite element simulation. For the plate-shaped PDN, the analytical methods are used to calculate the impedance such as the resonant cavity method [13, 14], the imaging method [15], the transfer matrix method [16, 17], and boundary element method [18]. With the development of IC technology, mesh-type and grid-type PDNs are usually designed since the plate-shaped PDN is easy to peel off during the fabrication process. The segmentation method is the basic method to analyze complex PDN structures. Some researchers have built the equivalent circuit models for the 3D PDNs using the lumped circuit models of on-chip PDNs and TSVs to analyze the impedance of the PDNs by SPICE simulations [19–22]. Others propose a hybrid approach combining the full-wave EM simulation and the circuit model to obtain accurate impedance of the PDN [23, 24]. Most of these studies focus on the influence of the regular TSV array on the PDN impedance, but few studies focus on the influence of the irregular TSV array with complex couplings. In Ref. [20], the proposed model of the regular P/G TSV array has a limitation in the assumption of uniform current magnitude distributions across all power and ground TSVs in the uniform distributed TSVs during the extraction of the partial TSV inductances. It leads to the inaccurate partial TSV inductances in a real multiply stacked PDN which has an uneven power distribution. In Refs. [25, 26], it uses a segmentation method to model the PDNs with multiply pairs of P/G TSVs. It considers the effects of P/G TSV pairs to estimate the impedance of the 3D stacked PDN. It is no longer applied if TSV pairs are close to each other because there is greater coupling between them. And it is unsuitable for the arbitrarily distributed TSVs which multiple grounded TSVs are shared by multiple power TSVs. There are two TSV design schemes, namely the irregular TSV placement and the regular TSV placement for the design of 3D ICs [27]. For the irregular TSV placement, the matrix-based calculation using a segmentation method can accelerate the calculation speed for the PDN impedance estimation and solve the complexity problem of building a SPICE circuit due to the lots of coupling. In this paper, a matrix calculation method is proposed to solve the PDN impedance of multi-stacked chips based on TMM rather than the simulations of the HFSS and SPICE. The P/G TSVs in the TSV array can be regular distributed or arbitrarily distributed. The coupling between the TSVs and the distributional effect of the on-chip PDN is considered. The test ports of the model can be TSV connection ports or ports of any interested nodes on the on-chip PDN of every tier. The multi-stacked on-chip PDN impedance is calculated quickly and accurately by the proposed method. It shows the advantages of large savings in computer run time and flexibility and versatility in applications.

The paper is organized as follows. In Sect. 2, a typical multi-stacked on-chip PDN structure based on TSVs is given and a detailed derivation of the impedance matrix is presented. In Sect. 3, the impedance obtained by the proposed method for different TSV distributions is compared. The accuracy of the proposed method is verified with the results obtained from HFSS. Compared with the results of HFSS and other methods, it concludes that the proposed method
2 Modeling and analysis of the multi-stacked on-chip PDN impedance

A locally simplified multi-stacked on-chip PDN in stacked 3D ICs is shown in Fig. 2, where active layers are face-to-back (F2B) stacked. The grid-type PDN is usually used for the on-chip PDN because it is efficient when it comes to design with a limited area and it is not easy to peel off. The grid-type on-chip PDN is composed of orthogonal metal wires in two interconnection layers, where power wires and ground wires are routed alternately in the same interconnection layer with an identical pitch and connected to corresponding wires in the next interconnection layer by a large of micro-vias. The P/G TSV array in silicon substrate connects adjacent on-chip PDNs to achieve power delivery. In this paper, bumps are simplified as an extension of the TSV metal. The impedance matrix of the multi-stacked on-chip PDN can be derived by using separated P/G TSV array and on-chip PDN models through TMM.

For an on-chip PDN model, a quasi-static solver can be applied if the dimension of a network is much less than one-tenth of the wavelength of interest ($\frac{0.1}{Î»}$). The grid-type on-chip PDN can be divided into a lot of periodic unit cells with a lumped element model for each cell. As shown in Fig. 3, the P/G grid is divided into $(N - 1) \times (M - 1)$ unit cells modeled with a distributed network of RLCG elements. The equivalent circuit of each grid unit cell consists of the resistance ($R_u$), inductance ($L_u$), conductance ($G_u$), and capacitance ($C_u$) which can be accurately calculated as (1), where
$L_p$ and $L_w$ are the pitch and width of the metal line of the mesh grid. Parameters with subscripts of CMS and Micro represent parameters per unit length in the coplanar multistrip type transmission line and the conductor-backed coplanar multistrip type transmission line, respectively. More details of the calculating procedure are presented in [28].

\[
R_u = (2L_p - L_w)R_{CM} + L_w R_{M}
\]

\[
L_u = (2L_p - L_w)L_{CM} + L_w L_{M}
\]

\[
C_u = 2(2L_p - L_w)C_{CM} + 2L_w C_{M}
\]

\[
G_u = 2\pi f C_u \tan(\delta)
\]

According to the relationship between the nodal voltage and the nodal current, the admittance matrix of the P/G grid ($Y_{P/Ggrid}$) in \(N \times M\) nodes can be expressed as:

\[
Y_{P/Ggrid} = \begin{bmatrix}
Y_{11} & -Y_{12} & 0 & 0 & \cdots \\
-Y_{12} & Y_{22} & -Y_{23} & 0 & \cdots \\
0 & -Y_{23} & Y_{33} & -Y_{34} & \cdots \\
\vdots & \vdots & \vdots & \ddots & \vdots \\
0 & 0 & 0 & \cdots & Y_{MM}
\end{bmatrix}
\]

(2a)

\[
Y_{11} = Y_{MM} = \frac{1}{2} Y_{22} = \cdots = \frac{1}{2} Y_{(M-1)(M-1)}
\]

\[
= \begin{bmatrix}
\frac{r_e}{4} + \frac{1}{Z_s} & -\frac{1}{Z_s} & 0 & \cdots & 0 \\
-\frac{1}{Z_s} & \frac{r_e}{4} + \frac{1}{Z_s} & -\frac{1}{Z_s} & \cdots & 0 \\
0 & 0 & \cdots & \frac{r_e}{4} + \frac{1}{Z_s} & -\frac{1}{Z_s} \\
0 & 0 & \cdots & 0 & \frac{r_e}{4} + \frac{1}{Z_s}
\end{bmatrix}
\]

(2b)

\[
Y_{12} = Y_{23} = \cdots = Y_{(M-1)M}
\]

\[
= \begin{bmatrix}
\frac{1}{2Z_s} & 0 \\
\frac{1}{Z_s} & \cdots \\
\frac{1}{Z_s} & \cdots \\
0 & \frac{1}{2Z_s}
\end{bmatrix}
\]

(2c)

\[
Z_s = R_u + j\omega L_u
\]

\[
Y_p = j\omega C_u + G_u
\]

As the size of the P/G grid increases, the number of the unit cells is increasing rapidly and the size of the admittance matrix of the P/G grid is bigger. The matrix calculation will become more complex and time-consuming. In the impedance calculation of a multi-port network, the input impedance of one port is obtained under the condition that the input currents of other uninterested ports are zero. To simplify the matrix and speed up the calculation, the matrix transformations are as follows. The relationship between voltages and currents in nodes of the grid metal is rewritten as:

\[
\begin{bmatrix}
I_a \\
I_b
\end{bmatrix} = \begin{bmatrix}
Y_{aa} & Y_{ab} \\
Y_{ba} & Y_{bb}
\end{bmatrix} \begin{bmatrix}
V_a \\
V_b
\end{bmatrix}
\]

(3)

where $I_a$ and $V_a$ are the current and voltage vector in the interested nodes, $I_b$ and $V_b$ are the current and voltage vector in the neglected nodes. For simplifying the admittance matrix of the P/G grid, the neglected nodes can be seen as open circuits and these nodal currents are limited to zero as (4). Then, these nodes are deleted from the grid nodes, only remaining the interested nodes.

\[
\begin{cases}
I_a = (Y_{aa} - Y_{ab} Y_{bb}^{-1} Y_{ba}) V_a \\
I_b = 0
\end{cases}
\]

(4)

So the simplified admittance matrix ($Y_{sim}$) in only interested nodes can be derived as:

\[
Y_{sim} = Y_{aa} - Y_{ab} Y_{bb}^{-1} Y_{ba}
\]

(5)

For a multi-stacked on-chip PDN, the P/G TSVs connecting adjacent on-chip PDNs can be randomly distributed. The nodes with power TSVs connecting are regarded as the nodes of interest to reduce the admittance matrix. The transmission matrix for a multi-port network can be derived in terms of the concerned nodal voltages and nodal currents and can be represented to relate the voltages and currents as:

\[
\begin{bmatrix}
V_{in} \\
I_{in}
\end{bmatrix} = \begin{bmatrix}
T_a & T_b \\
T_c & T_d
\end{bmatrix} \begin{bmatrix}
V_{out} \\
I_{out}
\end{bmatrix}
\]

(6)

So the transmission matrix of a single on-chip PDN in the vertical direction ($T_{PDN}$) can be written in a simpler form as:

\[
T_{PDN} = \begin{bmatrix}
1 & 0 \\
y_{sim} & 1
\end{bmatrix}
\]

(7)

It is not ignored that the electromagnetic coupling exists among the P/G TSV array as the frequency increases. To simplify the analysis of the coupling, the TSV array is considered as the multi-conductor interconnection and established the T-shaped network topology of the equivalent circuit model. Without a doubt, the equivalent circuit model becomes extremely complicated as the number of TSVs
increases. This paper replaces the simulation of the complex equivalent circuit with using the matrix computation. All the values of lumped elements in the model of TSVs as depicted in Fig. 4 are given in the closed-form formulas as [29]. A ground TSV is arbitrarily set as the reference marked with 0. The values of the self-inductance \((L_{ii})\) and mutual inductance \((L_{ij})\) of other TSV metals can be calculated as:

\[
L_{ii} = \frac{\mu_0 h_{\text{metal}}}{\pi} \ln \frac{P_{ij}}{r_{\text{TSV}}} \\
L_{ij} = \frac{\mu_0 h_{\text{metal}}}{2\pi} \ln \frac{P_{ij}P_{ji}}{P_{ij}r_{\text{TSV}}} 
\]  

(8a)  

(8b)

where \(\mu_0\) is the permeability of the vacuum, \(P_{ij}\) is the distance between the TSV marked with \(i\) and the TSV marked with \(j\), \(h_{\text{metal}}\) is the length of the TSV metal, and \(r_{\text{TSV}}\) is the radius of the TSV. Considering \(N\) TSVs in which there are \(m\) power TSVs and \(n\) ground TSVs, all ground TSVs which are shorted represent the current return path. Based on the definition of the loop inductance with the size of \(m \times m\), it is rewritten as [30]:

\[
\begin{cases}
V_p = j\omega L_{eq}I_p \\
V_g = 0
\end{cases}
\]

(9)

where \(V_p\) and \(I_p\) are the \(m \times 1\) voltage and current vectors of \(m\) power TSVs, respectively, \(V_g\) is the \(n \times 1\) voltage vector of \(n\) ground TSVs. Then, the effective loop inductance \((L_{eq})\) of the TSV array is yielded. When regarding each outer edge of the TSV as an equipotential surface, the equivalent inductance of Si substrate \((L_{\text{Si,eq}})\) in a homogeneous medium can be calculated as derived in (8) and (9). Next, simplify calculate the effective capacitance \((C_{\text{Si,eq}})\) and conductance \((G_{\text{Si,eq}})\) matrix of the silicon substrate as [31]:

\[
C_{\text{Si,eq}} = \frac{\mu_0 \varepsilon_0 \varepsilon_{\text{Si}} L_{\text{Si,eq}}}{2 \pi r_{\text{TSV}}} \\
G_{\text{Si,eq}} = \frac{\sigma_{\text{Si}}}{\varepsilon_0 \varepsilon_{\text{Si}}} C_{\text{Si,eq}}
\]

(10a)  

(10b)

The internal impedance \((Z_{in})\) for a TSV metal can be expressed as:

\[
Z_{in} = \frac{h_{\text{metal}} \sqrt{\varepsilon_0 \mu_0 \sigma_{\text{TSV}} I_0 (r_{\text{TSV}} \sqrt{\varepsilon_0 \mu_0 \sigma_{\text{TSV}}})}}{2\pi r_{\text{TSV}}} \frac{I_1 (r_{\text{TSV}} \sqrt{\varepsilon_0 \mu_0 \sigma_{\text{TSV}}})}{I_1 (r_{\text{TSV}} \sqrt{\varepsilon_0 \mu_0 \sigma_{\text{TSV}}})}
\]

(11)

where \(I_0\) and \(I_1\) are the modified Bessel functions of order zero and one, respectively. The effective internal impedance matrix \((Z_{\text{in,eq}})\) of the TSV array can be obtained in the similar way to (9). The linear capacitance of a TSV can be expressed as:

\[
C_{\text{OX}} = \frac{2\pi \varepsilon_0 \varepsilon_{\text{Si}} h_{\text{Si}}}{\ln \left(\frac{r_{\text{TSV}} + r_{\text{OX}}}{r_{\text{TSV}}}\right)}
\]

(12)

Next, \(Z_{eq}\) is given by \(1/(j\omega C_{\text{OX}})\) to calculate the effective linear capacitance matrix \((C_{\text{OX,eq}})\) as also similar way to (9). The effective linear capacitance matrix of the TSV array is extracted from \(Z_{\text{in,eq}} = (j\omega C_{\text{OX,eq}})^{-1}\). The impedance and admittance of the PG TSV array can be expressed as:

\[
Z_{\text{TSV}} = Z_{\text{in,eq}} + j\omega L_{\text{eq}}
\]

(13a)

\[
Y_{\text{TSV}} = \left(\frac{1}{j\omega C_{\text{OX,eq}}} + \frac{1}{G_{\text{Si,eq}} + j\omega C_{\text{Si,eq}}}\right)^{-1}
\]

(13b)

The transmission matrix of the TSV array \((T_{\text{TSV}})\) can be derived as:

\[
T_{\text{TSV}} = \frac{1}{2} \begin{bmatrix} \frac{Z_{\text{TSV}}}{1} & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} 1 & \frac{Z_{\text{TSV}}}{1} \\ 0 & 1 \end{bmatrix}
\]

(14)

Finally, the separated on-chip PDNs and TSV arrays are assembled into a whole. According to the cascade of the multi-port network as shown in Fig. 5, the transmission matrix of the multi-stacked on-chip PDN combining multiple on-chip PDNs and TSV arrays \((T_{\text{total,n}})\) can be expressed as:

\[
T_{\text{total,n}} = T_{\text{PDN,n}} \cdot T_{\text{TSV,n,n-1}} \cdots T_{\text{PDN,2}} \cdot T_{\text{TSV,2,1}} \cdot T_{\text{PDN,1}}
\]

(15)

where \(T_{\text{PDN,n}}\) is the transmission matrix of the on-chip PDN of tier \(n\), \(T_{\text{TSV,n,n-1}}\) is the transmission matrix of the TSV array between tier \(n\) and tier \(n-1\). The impedance matrix

Fig. 4 The partial equivalent circuit model of a TSV array

© Springer
of the multi-stacked on-chip PDN ($Z_{\text{total}_n}$) can be derived from $T_{\text{total}_n}$ as:

$$Z_{\text{total}_n} = \begin{bmatrix} T_{\text{total}_n a}^{-1} & T_{\text{total}_n c}^{-1} \\ T_{\text{total}_n c} & T_{\text{total}_n d} \end{bmatrix}^{-1}$$

(16)

The impedance matrix describes the voltage-current correlation over the connection ports of the PDN at different frequencies. The coupling effect between TSVs through matrix calculation is considered in the arbitrary distributed P/G TSVs. For the impedance of the ports of any interested nodes on the on-chip PDN of every tier, it can be derived from the Z-matrix transformation of the black box model as shown in Fig. 6. α segment is expressed as a single on-chip PDN where interested ports ($p$) are. β segment is expressed as the remaining part of the multi-stacked on-chip PDN. The interconnection between them is replaced by the interconnected ports denoted $c$-ports on the α segment and $d$-ports on the β segment. $p$ and $q$ ports are the concerned ports of the α and β segments. The Z-matrices of α, β, and γ segments are, respectively, partitioned into submatrices corresponding to the interested and connected ports as:

$$Z_{\alpha} = \begin{bmatrix} Z_{pp} & Z_{pc} \\ Z_{cp} & Z_{cc} \end{bmatrix}$$

(17a)

$$Z_{\beta} = \begin{bmatrix} Z_{dd} & Z_{dq} \\ Z_{qd} & Z_{qq} \end{bmatrix}$$

(17b)

$$Z_{\gamma} = \begin{bmatrix} Z_{pp} & Z_{pq} \\ Z_{qp} & Z_{qq} \end{bmatrix}$$

(17c)

$Z_{\alpha}$ and $Z_{\beta}$ can be replaced, respectively, by different $Z_{\text{total}_n}$ due to different segments. According to the continuity of the voltage and current on ports $c$ and $d$, $Z_{\gamma}$ can be calculated as:

$$Z_{\gamma} = \begin{bmatrix} Z_{pp} - Z_{pc}Z'_{dp} & Z_{pc}Z'_{dq} \\ Z_{qd}Z'_{dp} & Z_{qq} - Z_{qd}Z'_{dq} \end{bmatrix}$$

(18)

where $Z'_{dp} = [Z_{cc} + Z_{dd}]^{-1}Z_{cp}$ and $Z'_{dq} = [Z_{cc} + Z_{dd}]^{-1}Z_{dq}$.

3 Validation and analysis of the proposed method

To verify the accuracy of the proposed method of the impedance estimation in the TSV-based multi-stacked on-chip PDN structure, a double-stacked grid-type on-chip PDN is constructed and its parameter description is listed in Table 1. It has a horizontal size of $1\text{mm} \times 1\text{mm}$.

Table 1 The model parameters and its values

| Symbol | Parameter description | Value |
|--------|-----------------------|-------|
| $L_w$  | Width of the metal line | 10 μm |
| $L_p$  | Pitch of the metal line | 50 μm |
| $L_t$  | Thickness of the metal line | 1 μm |
| $L_d$  | Vertical distance between the metal layers | 0.6 μm |
| $r_{TSV}$ | Radius of the TSV metal | 5 μm |
| $h_{Si}$ | Height of the Si substrate | 50 μm |
| $h_{metal}$ | Length of the TSV metal | 60 μm |
| $t_{OX}$ | Thickness of the oxide liner | 0.2 μm |
| $p_{TSV}$ | Pitch between power and ground TSVs | - |
| $\sigma_{TSV}$ | Conductivity of the TSV metal | $5.8 \times 10^7$S/m |
| $\sigma_{Si}$ | Conductivity of silicon | 10 S/m |
| $\varepsilon_0$ | Permittivity of vacuum | $8.85 \times 10^{-12}$S/m |
| $\varepsilon_{Si}$ | Permittivity of silicon | 11.9$\varepsilon_0$ |
| $\varepsilon_{OX}$ | Permittivity of oxide | $4\varepsilon_0$ |
| $\mu_0$ | permeability of vacuum | $4\pi \times 10^{-7}H/m$ |
The ordinary cylindrical TSVs filled with copper are applied in the TSV array. Designers need to arrange these TSVs properly to meet signal integrity, power integrity, and heat dissipation requirement. Fig. 7 shows two different TSV assignments. For a regular TSV distribution, P/G TSVs are uniformly distributed on the nodes with an identical pitch. For an arbitrary TSV distribution, P/G TSVs are only assigned in the whitespace around the circuit modules. Therefore, P/G TSVs can be arranged in any position of the substrate that is dependent on the distribution of the circuit modules. Multiple and randomly located ground TSVs can be shared by multiple power TSVs. Without good planning and optimization, the over-design P/G network may create congestion problems for the later signal routing resources that are over-used. In the constructed structures, the regular TSV distributions are shown in Fig. 8, which includes the different number of TSV pairs and the uniform TSV distributions with the different scales of the TSV array. The proposed model is used to calculate the impedance of which the result is compared with the full-wave method and previous models. Due to the difficulty in the fabrication of complete multi-stacked on-chip PDNs, a frequency-domain simulation to extract Z-parameters is conducted ranging from 0.1GHz to 40 GHz with a 3D electromagnetic (EM) solver, ANSYS HFSS to verify the accuracy of the proposed method. Lumped ports for the analysis of the PDN input impedance are located on the topmost on-chip PDN.

As shown in Fig. 9, the PDN impedance curves have similar characteristics which mainly have three resonant frequencies ($f_1$, $f_2$, and $f_3$) below 20GHz. These frequencies are caused by the series and parallel resonances of the equivalent capacitance of the P/G grid ($C_{P/G\text{grid}}$), the equivalent inductance of the P/G grid ($I_{P/G\text{grid}}$), and the equivalent inductance of the TSV array ($L_{TSV}$). As the number of TSVs increases, $f_2$ moves to a higher frequency and it is eliminated if the number of TSVs is large enough. In this situation, $f_3$ is...
equal to $f_1$. So the deviation from the resonance frequency of the HFSS model such as $f_1$ is compared to verify the accuracy of the proposed method. The results of the proposed method show good agreement with the results of the HFSS model. The deviation of $f_1$ is about 6%. Not only the PDN impedance but also the simulation time for the three methods are compared as shown in Table 2. The simulation is performed on a computer with 16 cores (at 3.0 GHz) and 256 GB of RAM. The conservation of the CPU run time is about 99.9% compared with the HFSS model. The proposed model leads to a larger saving in CPU run time than using HFSS simulation. It only takes a tiny computing time compared with the full-wave method. Therefore, it is concluded that the proposed model is accurate and efficient to estimate the impedance of the multi-stacked on-chip PDN with the regular TSVs connecting. Comparatively, the benefit of the proposed method is that it can deal with the complicated TSV array including not only the regularly distributed TSVs but also the arbitrarily distributed TSVs in 3D PDNs. The arbitrarily distributions of TSVs are constructed as shown in Fig. 10. The whitespace around the circuit models is, respectively, across, peripheral, and combined distribution in the substrate, and TSVs are only assigned in the whitespace. To enable power TSVs to be connected directly to the power wires without the need for the extra redistribution layer, power TSVs are placed designedly at the location of the intersection of the two-layer of the power metal wires so that it can reduce the wiring area. Ground TSVs are placed designedly at the location of the intersection of the two-layer of the ground metal wires. The impedances of three test ports marked with port 1, 2, and 3 are calculated and qualitatively analyzed. The results are shown in Fig. 11. In the range of the lower frequency, the impedance shows capacitive which is determined by the $C_{P/G\ grid}$ and the equivalent capacitance of the TSV array ($C_{TSV}$). As the number of TSVs increases, the total capacitance is increasing so that impedance is decreasing. As the frequency goes up, the impedance shows inductive which is determined by the $L_{P/G\ grid}$.

### Table 2
Comparison of results with several kinds of different methods

| Cases in Fig. 8 | Methods                  | Deviation of $f_1$ | CPU run time | Time conservation |
|-----------------|--------------------------|--------------------|--------------|-------------------|
| a               | HFSS model               | –                  | 1h 23min 30s | –                 |
|                 | The proposed model       | 4.2%               | 7.03 s       | 99.94%            |
|                 |                          | 6.5%               | 8.57 s       | 99.88%            |
|                 |                          | 5.9%               | 10.06 s      | 99.89%            |
|                 | Model in [25]            | 11.1%              | 1min 12s     | 98.56%            |
|                 |                          | 13.8%              | 1min 18s     | 98.89%            |
|                 |                          | 12.6%              | 2min 05s     | 98.61%            |
| b               | HFSS model               | –                  | 2h 39min 48s | –                 |
|                 | The proposed model       | 6.2%               | 13.47s       | 99.86%            |
|                 |                          | 5.9%               | 15.91s       | 99.85%            |
|                 | Model in [20]            | 10.9%              | 40.96s       | 99.57%            |
|                 |                          | 9.5%               | 2min 13s     | 98.71%            |

![Fig. 10](image-url) Three kinds of arbitrary distributions of P/G TSVs. a cross b peripheral c combined

![Fig. 11](image-url) The comparison of three kinds of arbitrary distributions of P/G TSVs for the PDN impedance
since the $L_{TSV}$ decreases to a very small value that can be neglected if the number of TSVs is large enough.

The impedance of the PDN should stay at a low level to ensure power integrity. Aspects that the influence of the impedance for the multi-stacked on-chip PDN and methods to decrease the impedance are studied. Fig. 12 shows several kinds of low density and arbitrary P/G TSVs connecting between tier $n$ and $n-1$. The impacts of the number of TSVs on the impedance of the multi-stacked on-chip PDN are explored. Fig. 13 compares four input impedances at the center of the toper tier for the double-stacked on-chip PDNs with four kinds of arbitrary TSV array connecting as shown in Fig. 12. Four PDN impedance curves have similar characteristics. Careful observation reveals that the difference in the input impedance of the lower frequency range is slight. The reason is that the impedance of the lower frequency range is caused by the total capacitance which consists of $C_{TSV}$ and two times $C_{P/G\text{grid}}$. As the number of TSVs increases, the capacitance of TSVs is gradually larger and the total capacitance is only larger slightly, but the effective inductance of the power TSVs is smaller. The resonance frequency $f_1$ goes to the higher frequency range with an increased ground TSV number compared to case $a$ with $b$ and $c$, which can affect the relative distance between the frequency of the impedance peak and the clock frequency, but the impact is getting smaller with more ground TSVs compared case $b$ with $c$ as it is shown that the impedance curves tend to be approximately the same. Therefore, it needs to add more power TSVs as shown in case $d$ if higher $f_1$ and $f_2$ are wanted, and $f_2$ will be eliminated because of the enough TSVs.

To determine the effects of the number of stacked tiers on the impedance, it varies from two to four. Fig. 14 shows the comparison of three input impedances at the center of the topest tier for the multi-stacked on-chip PDNs with the TSV array connecting as shown in case $c$ in Fig. 12. The P/G grid and TSV capacitances increase with the number of stacked tiers increasing so that the impedance below the series resonant frequency ($f_1$) is decreased. $f_1$ moves to a lower frequency range, but the lowest parallel resonance frequency $f_2$ and $f_3$ moves to a higher range.

Fig. 12 Different number of TSVs connecting between tier $n$ and $n-1$. a 4P1G b 4P5G c 4P9G d 9P16G

Fig. 13 The comparison of the input impedance at the center of the toper tier for the double-stacked on-chip PNDs with four kinds of TSV arrays connecting, respectively, as shown in Fig. 12

Fig. 14 The comparison of the input PDN impedance at the center of the topest layer depended on the different numbers of the tiers
frequency \( (f_2) \) of them moves to the lower frequency range with the higher PDN impedance peak. As a result, it needs to pay more attention to designing the future heterogeneous 3D IC because a higher-stacked on-chip PDN is more difficult to keep minimizing the low PDN impedance.

To determine the effect of the size of the stacked on-chip PDN on the impedance, the scales of the sizes of four-stacked on-chip PDNs are varied from 0.7 to 2.2. The uniform density distribution of TSVs is adopted. Fig. 15 shows the comparison of three input impedances at the center of the topmost tier for the four-stacked on-chip PDNs with the TSV array connecting as shown in case d in Fig. 12. When the scale of the stacked on-chip PDN is increased, the impedance below series resonant frequency \( (f_1) \) is decreased because the P/G grid and TSV capacitances increase. \( f_1 \) moves to the lower frequency range. The parallel resonance becomes less and less obvious in the high-frequency range.

**4 Conclusion**

The proposed model can reflect the various arrangements of the P/G TSVs for estimating the multi-stacked on-chip PDN impedance in 3D ICs. The separated power/ground grid units of the on-chip PDN are modeled as the transmission line using the frequency-dependent RLGC parameters, and the TSV array is modeled using the theory of multiconductor transmission lines. The coupling between the arbitrarily distributed TSVs and the distributional effect of the on-chip PDN is considered. Then, the impedance of the multi-stacked on-chip PDN is derived by the transmission matrix method through the cascade. It replaces the simulation of the complex SPICE circuit in which there exists lots of coupling with the matrix calculation method. It is computationally efficient and leads to a large saving in CPU run time. For the complicated structure, it is also accurate and scalable to analyze the impedance in the pre-design stage and help designers achieve a 3D PDN quickly and reliably.

**Acknowledgements** This research was supported in part by the National Natural Science Foundation of China (Grant Nos. 62021004, 61934006 and 61574106); and in part by the Industry University Research Project of Chongqing IC Innovation Research Institute, Xidian University (Grant No. CQIRI-2022CXY-05).

**Data Availability** Enquiries about data availability should be directed to the authors.

**Declarations**

**Conflict of interest** The authors have not disclosed any conflict of interests.

**References**

1. Lau, J.H.: Overview and outlook of three-dimensional integrated circuit packaging, three-dimensional si integration, and three-dimensional integrated circuit integration. J. Electr. Packag. 136(4), 040801 (2014). https://doi.org/10.1115/1.4028629
2. Mahajan, R., Sankman, B.: 3D Packaging Architectures and Assembly Process Design, pp. 17–46. Springer, Cham (2017)
3. Lu, T., Serafy, C., Yang, Z., Samal, S.K., Lim, S.K., Srivastava, A.: TSV-based 3-D ICs: design methods and tools. IEEE Trans. Comput.-Aided Des. Integr. Circ. Syst. 36(10), 1593–1619 (2017). https://doi.org/10.1109/TCAD.2017.2666604
4. Li, E.-P.: Electrical Modeling and Design for 3D System Integration: 3D Integrated Circuits and Packaging Signal Integrity Power Integrity and EMC. Wiley, Hoboken, New Jersey (2012)
5. Swaminathan, M., Engin, E.: Power Integrity Modeling and Design for Semiconductors and Systems. Prentice Hall Press, USA (2007)
6. Swaminathan, M., Kim, J., Novak, I., Libous, J.P.: Power distribution networks for system-on-package: status and challenges. IEEE Trans. Adv. Packag. 27(2), 286–300 (2004). https://doi.org/10.1109/TADVP.2004.831897
7. Xu, J., Bai, S., Nalla, K., Sapozhnikov, M., Drewniak, J.L., Hwang, C., Fan, J.: Power delivery network optimization approach using an innovative hybrid target impedance. In: 2019 IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity (EMC+SIPI), pp. 211–216 (2019). https://doi.org/10.1109/ISEMC.2019.8825309
8. Kim, J., Lee, W., Shim, Y., Shim, J., Kim, K., Pak, J.S., Kim, J.: Chip-package hierarchical power distribution network modeling and analysis based on a segmentation method. IEEE Trans. Adv. Packag. 33(3), 647–659 (2010). https://doi.org/10.1109/TADVP.2010.2043673
9. Pak, J.S., Kim, J., Cho, J., Lee, J., Lee, H., Park, K., Kim, J.: On-chip pdn design effects on 3d stacked on-chip pdn impedance based on tsv interconnection. In: 2010 IEEE Electrical Design of Advanced Package & Systems Symposium, pp. 1–4 (2010). https://doi.org/10.1109/EDAPS.2010.5682994
10. Zhu, W., Wang, Y., Dong, G., Yang, Y., Song, D.: MTL-based modeling and analysis of the effects of TSV noise coupling on the power delivery network in 3D ICs. J. Comput. Electron. 19(7), 543–554 (2020). https://doi.org/10.1007/s10825-020-01466-w
11. Knechtel, J., Markov, I.L., Lienig, J., Thiele, M.: Multiobjective optimization of deadspace, a critical resource for 3d-ic integration. In: 2012 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 705–712 (2012)
12. Wu, Q., Zhang, T.: Design techniques to facilitate processor power delivery in 3-D processor-dram integrated systems. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 19(9), 1655–1666 (2011). https://doi.org/10.1109/TVLSI.2010.2053565
13. Na, N., Swaminathan, M.: Modeling and transient simulation of planes in electronic packages for gbd systems. In: IEEE 8th Topical Meeting on Electrical Performance of Electronic Packaging (Cat. No.99TH8412), pp. 149–152 (1999). https://doi.org/10.1109/EPEP.1999.819214
14. Wang, J., Lu, J., Chu, X., Liu, Y., Li, Y.: Modeling of multilayered power/ground planes based on resonant cavity algorithm. IEEE Access 6, 67360–67372 (2018). https://doi.org/10.1109/ACCESS.2018.2876886
15. Yang, D.-C., Wei, X.-C.: Impedance calculation of power and ground planes by using imaging methods. In: 2012 Asia-Pacific Symposium on Electromagnetic Compatibility, pp. 37–40 (2012). https://doi.org/10.1109/AP EMC.2012.6237851
16. Kim, J.-H., Swaminathan, M.: Modeling of irregular shaped power distribution planes using transmission matrix method. IEEE Trans. Adv. Packag. 24(3), 334–346 (2001). https://doi.org/10.1109/6040.938301
17. Kim, J.-H., Matoglu, E., Choi, J., Swaminathan, M.: Modeling of multi-layered power distribution planes including via effects using transmission matrix method. In: Proceedings of ASP-DAC/VLSI Design 2002. 7th Asia and South Pacific Design Automation Conference and 15th International Conference on VLSI Design, pp. 59–64 (2002). https://doi.org/10.1109/ASPDAC.2002.994886
18. Zhang, L., Juang, J., Kiguradze, Z., Pu, B., Jin, S., Wu, S., Yang, Z., Li, E.-P., Fan, J., Hwang, C.: Efficient dc and ac impedance calculation for arbitrary-shape and multilayer pdn using boundary integration. IEEE Transa. Signal Power Integr. 1, 1–11 (2022). https://doi.org/10.1109/TSIPI.2022.3164037
19. He, H., Lu, J.J.-Q.: Modeling and analysis of PDN impedance and switching noise in TSV-based 3-D integration. IEEE Trans. Electron Devices 62(4), 1241–1247 (2015). https://doi.org/10.1109/TED.2015.2396914
20. Pak, J.S., Kim, J., Cho, J., Kim, K., Song, T., Ahn, S., Lee, J., Lee, H., Park, K., Kim, J.: PDN impedance modeling and analysis of 3D TSV IC by using proposed P/G TSV array model based on separated P/G TSV and chip-PDN models. IEEE Trans. Compon. Packag. Manuf. Technol. 1(2), 208–219 (2011). https://doi.org/10.1109/TCMP.2010.2101771
21. Kim, K., Lee, W., Kim, J., Song, T., Kim, J., Pak, J.S., Kim, J., Lee, H., Kwon, Y., Park, K.: Analysis of power distribution network in tsv-based 3d-ic. In: 19th Topical Meeting on Electrical Performance of Electronic Packaging and Systems, pp. 177–180 (2010). https://doi.org/10.1109/EPEPS.2010.5642575
22. Hu, Q.-H., Zhao, W.-S., Fu, K., Wang, D.-W., Wang, G.: On the applicability of two-bit carbon nanotube through-silicon via for power distribution networks in 3-D integrated circuits. IET Circ. Devices Syst. 15(1), 20–26 (2021). https://doi.org/10.1049/cds.2021.12010
23. Zou, G., Wen, X., Yang, S., Ding, L., Ding, W., Yang, Y.: An integral equation hybrid method for the impedance calculation of the grid power distribution network with an arbitrary shape. IEEE Trans. Magn. 55(6), 1–4 (2019). https://doi.org/10.1109/TMAG.2019.2904099
24. Cho, K., Kim, Y., Kim, S., Park, H., Park, J., Lee, S., Shim, D., Lee, K., Oh, S., Kim, J.: Fast and accurate power distribution network modeling of a silicon interposer for 2.5-D/3-D ICs with multilayer TSVs. IEEE Trans. Compon. Packag. Manuf. Technol. 9(9), 1835–1846 (2019). https://doi.org/10.1109/TPCOM.2019.2895083
25. Kim, K., Yook, J.M., Kim, J., Kim, H., Lee, J., Park, K., Kim, J.: Interposer power distribution network (PDN) modeling using a segmentation method for 3-D ICs with TSVs. IEEE Trans. Compon. Packag. Manuf. Technol. 3(11), 1891–1906 (2013). https://doi.org/10.1109/TPCOM.2013.2276050
26. Kim, K., Hwang, C., Koo, K., Cho, J., Kim, H., Kim, J., Lee, J., Lee, H.-D., Park, K.-W., Pak, J.S.: Modeling and analysis of a power distribution network in TSV-based 3-D memory IC including P/G TSVs, on-chip decoupling capacitors, and silicon substrate effects. IEEE Trans. Compon. Packag. Manuf. Technol. 2(12), 2057–2070 (2012). https://doi.org/10.1109/TPCOM.2012.2214482
27. Lim, S.K.: Regular Versus Irregular TSV Placement for 3D IC, pp. 3–40. Springer, New York (2013). https://doi.org/10.1007/978-1-4419-9542-1_1
28. Hwang, C.S., Kim, K.Y., Pak, J.S., Kim, J.H.: Modeling of an on-chip power/ground meshed plane using frequency dependent parameters. J. Electromagn. Eng. Sci. 11(11), 192–200 (2011). https://doi.org/10.5515/JKIEES.2011.11.3.192
29. Qu, C., Ding, R., Liu, X., Zhu, Z.: Modeling and optimization of multilayer TSVs for signals shield in 3-D ICs. IEEE Trans. Electromagn. Comput. 59(2), 461–467 (2017). https://doi.org/10.1109/TEM C.2016.2608981
30. Paul, C.R.: Analysis of Multiconductor Transmission Lines 2e. Wiley, Hoboken, New Jersey (2008)
31. Engin, A.E., Narasimhan, S.R.: Modeling of crosstalk in through silicon vias. IEEE Trans. Electromagn. Comput. 55(1), 149–158 (2013). https://doi.org/10.1109/TEM C.2012.2206816

Publisher’s Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.