ReS\textsubscript{2}/h-BN/Graphene Heterostructure Based Multifunctional Devices: Tunneling Diodes, FETs, Logic Gates, and Memory

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A 2D heterostructure consisting of few-layer direct bandgap ReS\textsubscript{2}, a thin h-BN layer, and a monolayer graphene (Gr) for application to various electronic devices is investigated. Metal-insulator-semiconductor (MIS)-type devices with 2D van-der-Waals (vdW) heterostructures are recently studied as important components to realize various multifunctional device applications in analogue and digital electronics. The tunnel diodes of ReS\textsubscript{2}/h-BN/Gr exhibit light tunable rectifying behaviors with low ideality factors and nearly temperature independent electrical characteristics. The devices behave like conventional MIS-type tunnel diodes for logic gate applications. Furthermore, similar vertical heterostructures are shown to operate in field-effect transistors with a low threshold voltage and a memory device with a large memory gate for future multifunctional device applications.

1. Introduction

An assembly of several 2D crystals via a weak van-der-Waals (vdW) interaction in one vertical stack exhibits various exciting physical phenomena.\cite{1,2} The unique electronic transport properties in the 2D heterostructures via band alignment modulation, is the key to utilize them in multifunctional high performance electronic devices.\cite{3,4} The use of a vdW heterostructure with various atomically flat 2D materials makes it possible to realize various electronic primary components such as diodes, transistors, capacitors, and memory devices, which would make it possible to integrate multifunctional devices on a single chip. 2D-heterostructure-based metal-insulator-semiconductor (MIS)-type devices have various potential applications in analogue and digital electronics.\cite{3,4} For instance, insulating atomically flat hexagonal boron nitride (h-BN) can function as a 2D tunneling layer between a conductor and a semiconducting channel thus allowing perfectly planar charge injection across the atomically flat interface without various charge trapping sites derived from dangling bonds.\cite{5,6} Such quantum tunneling can make it possible to realize vertical MIS-type two-terminal diodes with the superior and temperature independent functionality, which is an advantage for integrated circuit technology.\cite{7,8,9,10} Thus the heterostructure of vdW materials allows to create vertical diodes for logic gate operation in future digital electronics. The opportunity for increasing the integration density is expected to be greater in vertically stacked MIS-type-tunnel-diode-based logic gates circuits. Compared with conventional Si 3D semiconductor-based electronic devices, all-2D layered materials and their heterostructures are expected to be superior for application to quantum tunnel diodes with high performance and less temperature dependence.

Field-effect transistors (FETs) and non-volatile memory (NVM) devices have been studied experimentally and theoretically because large-scale CMOS compatible three-terminal FETs are convenient for application to integrated circuit technology. A highly insulating h-BN layer can be used as a 2D dielectric layer for ReS\textsubscript{2} FET operation with atomically flat graphene (Gr) as a local gate, where the strong electrostatic modulation of ReS\textsubscript{2} channel conduction can be achieved. This can efficiently reduce the operating bias for ReS\textsubscript{2} FETs with a reasonable ON/OFF ratio for low power operation. In another application to a memory device, a Gr layer isolated from the ReS\textsubscript{2} channel with insulating h-BN can be used as a floating gate for charge storage. However, many challenges and problems still remain to be overcome before we can realize real device applications, and these include temperature dependence, high operating voltage, low operation speed, poor reliability, low integration density, low optical absorption, and poor sensing bandwidth. Recent studies with direct bandgap multilayer ReS\textsubscript{2} (~1.4–1.5 eV) have reported various electronics and optoelectronics applications.\cite{11,12,13,14} Different MIS-type device structures have been explored using 2D material based heterostructures\cite{15,16,17,18,19,20} as has their device application\cite{21} and logic gate operation.\cite{22,23,24} However, little work has been reported on ReS\textsubscript{2} based heterostructure in relation to MIS-type tunnel diodes with a view to using these diodes for logic...
gate operation and the heterostructure for multifunctional device applications. By contrast, for transistor operation, the ON/OFF current ratio is always compromised due to the application of a low gate field, and for memory operation it is always critical to obtain a large memory window for future multilevel memory operation in ultrathin nanoelectronics.

The main purpose of this study is to build multifunctional devices using 2D-layered vdW materials as basic building blocks for diodes, for FETs operating at a low bias, and for logic gate applications and NVM applications. Different layered material components were included in the vdW stack via a multistep transfer process to realize multifunctional device applications. Recently, we have developed a laser-assisted NVM device for multi-level storage applications using a heterostructure consisting of various 2D materials. A similar heterostructure device can be used for logic gate device applications, which further expands the possibilities to multi-functional device applications. Quantum tunneling phenomena can be incorporated in a designed heterostructure in order to obtain almost temperature independent operation in the fabricated diodes. ReSe₂/h-BN/Gr vertical MIS-like heterostructures as quantum tunneling diodes (QTDs) are studied in detail by characterizing the gate electric field dependence, temperature dependence and incident light excitation. We then realize logic gates operation by using a vertical MIS-type tunnel diode. The vertical geometry can lead to tunnel devices with a high rectification ratio and an atomically flat 2D surface as high tunneling area for a large turn-on current and a low turn-on voltage. The fabricated diodes were realized by direct tunneling (DT) at a lower field strength and Fowler–Nordheim (FN) tunneling by the application of a high-strength electric field. These tunnel diodes can be used to design various logic gates. We obtained a large rectification, low ideality factor, temperature independent tunnel diodes, and their logic gate operation. Furthermore, similar heterostructure can be used for other active electronic devices such as low operating bias FETs transistors and memory devices by arranging different electrical contacts, which are described in the second part of this work. The key parameter of achieving multifunctionality of the device is the fine tuning of the h-BN thickness. The reduction of h-BN layer thickness enables low bias operating FETs, high gate bias modulated NVM operation and vertical MIS-type tunnel diodes. We found that h-BN thickness of 3–5 nm is suitable for the both tunneling, namely DT and FN-tunneling, leading to applications like vertical tunnel MIS-type diodes. Whereas, the h-BN thickness of 6–10 nm is applicable for FN-tunneling, where low bias operating FETs and high gate bias modulated NVM devices can be fabricated. This study provides an overview of the use of all-2D atomically-flat layered materials to realize various electronic components including diodes, gate-tunable diodes, low bias operating FETs, logic gate devices, and memory devices for multifunctional electronic device applications. These devices are candidates for use in the future smart technology Internet-of-Things (IoT) as building blocks in next generation VLSI architectures, which can potentially enable all opto-electrical logic processing and quantum information processing.

2. Results and Discussion

2.1. MIS-Type Diode Performance and Logic Gate Operation

A MIS-type diode structure for logic gate application is a vdW heterostructure consisting of multilayer h-BN ReSe₂ supported by high-quality ReSe₂ as a tunneling layer, where we placed monolayer Gr beneath the h-BN as a conductive layer. The 2D nanosheets were directly exfoliated on top of a polydimethylsiloxane (PDMS) stamp and transferred to the top of another nanosheet on the SiO₂/Si substrate. The standard dry transfer method was used to transfer various large-area high-quality 2D flakes onto an arbitrary substrate. The device fabrication is described in detail in the experimental section. In a vdW heterostructure with ReSe₂ as a semiconducting layer will have to reduce scattering from the charged impurities of the substrate and interfacial impurities resulting from the presence of the atomically flat vdW material h-BN. Figure 1a–c, respectively, show an optical image of the different components used to fabricate the heterostructure, and AFM images of the insulating layer h-BN and the top ReSe₂ layer obtained with a line scan.

We confirmed the crystalline quality of the transferred ReSe₂ layer by Raman spectroscopy (Figure 1d), which indicated the high crystallinity and high chemical purity of the ReSe₂ flake material. The ReSe₂ layer was a few atomic layers (~3 nm) thick, which was further verified with an AFM scan and with a line profile monitoring the thickness. We observed typical E₂g (in-plane vibration mode) and A₁g (out-of-plane vibration mode) peaks at 162 and 212 cm⁻¹, respectively, along with other labeled peaks. The Raman spectrum of Gr (Figure 1e,f) exhibits a crystalline monolayer signature as it has a 2D/G peak integral intensity ratio greater than 2 and a narrow (and symmetric) 2D peak width (FWHM) of 22.1 ± 0.5 cm⁻¹ at 2680.4 cm⁻¹. Other Raman peak signatures were present, namely that of an E₂g in-plane phonon caused by the CC stretching vibration mode and of a D peak at 1350 cm⁻¹, which is related to defects. The h-BN signature was observed in the E₁g peak, which is the in-plane phonon vibration mode (Figure 1e) at 1366.4 cm⁻¹, where the thickness was ~9 nm as monitored from the AFM topography image and the line profile (Figure 1e,f). Choosing the right h-BN thickness is very important in terms of promoting DT and/or FN tunneling and we employed h-BN layers with a thickness of 5–9 nm for both electron and hole tunneling. Varying the thickness of h-BN can make it possible to realize various different applications including MIS-type diodes. FETs with a low threshold voltage and memory applications, which are discussed in subsequent sections. It is worth noting that various defect levels and/or trap levels have also been reported in h-BN layers and ReSe₂, which might also affect the tunneling process.

First, we tested p⁺⁺Si back-gated few-layer ReSe₂ channel-based FET devices (Inset Figure 2a) at room temperature to identify the majority carrier transport using the conventional solid gate dielectric. The representative transfer characteristics (I_d–V_g; sweep V_d) and output characteristics (I_d–V_g) for different V_g values are represented in Figure 2a, and they suggest that ReSe₂ has n-type conductance with natural electron doping. The linear output characteristics (I_d–V_g; inset Figure 2a) shows effective ohmic contacts with the Cr/Au electrodes. The electrical
Figure 1. a) Optical image of a fabricated multilayer ReS$_2$/h-BN/Gr heterostructure before the addition of electrical contacts. b,c) Height profile corresponding to the solid green line in the inset surface topography AFM image for h-BN and ReS$_2$ layers, respectively. d) Raman spectra taken from the top surface of the ReS$_2$ flake in the ReS$_2$/h-BN/Gr heterostructure. e,f) The Raman spectrum was collected from the region corresponding to the h-BN and Gr/SiO$_2$, respectively. The inset shows an optical image of the device after the addition of electrical contacts.

Figure 2. a) A typical transfer curve ($I_d$ vs $V_g$) of a ReS$_2$ FET device, showing n-type characteristics. The insets show the output curve with the SiO$_2$ back gate $V_g$ varying in 10 V steps and an optical image of the ReS$_2$ FET. Device performance of MIS-type diode: b) Output curve measured across the heterostructures for three different diodes. The insets show an optical image of the tested device and a schematic illustration of the MIS-type diode. c) A linear and log-scale plot with diode equation fitting that shows an ideality factor of 1.7. The inset shows the FNT-curve fitting in the high field region and a schematic band diagram obtained during FN-tunneling. d) Output characteristics curves: drain current ($I_d$) versus $V_d$ for different control gate biases $V_g$. The inset shows the energy band diagram of a ReS$_2$/h-BN/Gr heterostructure with a positive drain voltage at a Gr terminal.
performance of the MIS-type diodes, namely the current versus voltage ($I–V$) curves, was measured across the heterostructure device consisting of a few-layer ReS$_2$/h-BN/Gr to demonstrate the formation of vertical MIS-type diodes with high rectification and a low turn-on voltage. We evaluated the electrical characteristics ($I–V$) of the fabricated diodes as shown in the optical image in Figure 2b inset. An h-BN tunnel barrier thickness of \( \approx 5 \) nm was used for MIS-type diodes application. During the electrical probe measurements, the Gr was connected to the drain electrode and the n-type ReS$_2$ was connected to the source electrode. Here, the Gr layer was found to be initially hole doped from the absorption of oxygen and/or water molecules from the air.\[^{25}\] Typical $I–V$ characteristics of fabricated diodes show that all the MIS-type diodes exhibited a highly rectifying feature (Figure 2b). Room temperature output characteristics with different bias voltages are shown in Figure S1, Supporting Information, where electron accumulation and hole inversion in the ReS$_2$ layer are clearly observed. A small ideality factor ($\eta$) of 1.7 (Figure 2c) was extracted from the forward-bias characteristics after fitting with the standard n–p diode forward-bias equation:

$$I_s = I_r \left( e^{V_{ds} / \eta k_B T} - 1 \right)$$  \hspace{1cm} (1)

where $I_r$, $q$, $k_B$, and $T$ represent the reverse-bias saturation current, electron charge, Boltzmann constant and absolute temperature of the junction, respectively. This suggests that high quality interfaces were formed between those ReS$_2$, h-BN and Gr layers with minimal interface recombination/generation of carriers. We also found that the $I–V$ characteristics of the diodes are less likely to be temperature dependent (Figure S2, Supporting Information). Notably, we can fit the Fowler–Nordheim tunneling (FNT) relation in the high electric field region of the tunneling current-voltage curve. The FNT equation is expressed as follows:

$$\ln \frac{I(V)}{V_{ds}^3} = \ln \frac{A q^2 m^* \phi_B}{8 \pi h m^* d^2} - \frac{8 \pi d p_0^0 \sqrt{2m*}}{3k_B V_{ds}}$$  \hspace{1cm} (2)

where $A$, $\phi_B$, $q$, $m$, $m^*$, and $d$ are the effective contact area, barrier height, electron charge, free electron mass, effective electron mass, barrier width of the tunneling layer of h-BN and Planck’s constant, respectively. The FNT equation (Equation 2) fitted (Inset Figure 2c) under the condition of a forward bias tunneling current in a high applied electric field is shown in the linear region of the $\ln(I(V)/V^3)$ versus $(1/V)$ plot.\[^{27}\] The electron Schottky barrier height between Gr and h-BN ($\phi_B$) of 1.2 eV, was extracted from the FNT equation fitted in the forward bias region, which is lower than the reported value of 2.7 eV.\[^{27}\] This analysis shows the possibility of FNT-tunneling based electronic conduction in the vertical MIS-type diode in a high applied field with the assistance of defects. Various defect levels and/or trap levels of h-BN could be incorporated in the heterostructure device to promote increased tunneling current in the vertical direction to further increase the ON current, which could be the reason for obtaining the low barrier height value. One can provide more direct evidence to distinguish DT and FNT by local excitation with a focused laser beam.\[^{27}\] Furthermore, we modulate the diode performance by using a gate induced electric field and/or varying the incident laser intensity as follows. We applied a back-gate voltage (control gate bias $V_g$) to the degenerately doped silicon substrate ($p^+\text{Si}$) to tune the tunnel current versus voltage characteristics via electrostatic coupling and the systematic shifting of the Fermi level of the ReS$_2$ channel along with band alignment across the ReS$_2$/h-BN/Gr heterostructure. The representative output characteristics ($I_r–V_g$) of the FET structure with different $V_g$ values (−40 V to +40 V) showed a non-linear drain current, representing good rectifying behavior, and gate-induced modulation of drain current was observed (Figure 2d). The flat band alignment of ReS$_2$/h-BN/Gr has type-II band alignment, and the positive forward bias band alignment of the structure is shown in the inset in Figure 2d. It is a scenario whereby under a forward bias condition, the majority of the carrier electrons move from the ReS$_2$ tunnel to the Gr to form a high drain current. Whereas with a reverse bias, the electrons tunneling from Gr to ReS$_2$ are suppressed by depletion in ReS$_2$ at a positive bias resulting in the production of less tunnel current. Under dark condition, the tunneling current from Gr to ReS$_2$ is dominated due to high carrier density in Gr, whereas under light illumination the tunneling current is dominated from ReS$_2$ to Gr due to highly increase photo-generated carriers in ReS$_2$. When positive drain voltage is applied to the Gr electrode, the photo-generated carrier (i.e., majority carrier electron) from ReS$_2$ can tunnel efficiently to Gr, which can be seen from the band alignment (Figure S3, Supporting Information), which produce high photocurrent in the MIS-type diode structure.

We investigated the optoelectrical conduction process in the MIS-type diode structure with the possibility of light-assisted modulation in the rectification performance. Furthermore, the optical excitation might result in a new functionality for tuning the device application in digital optoelectronics. Here we found that visible laser illumination (532 nm) produced a photocurrent, which was gate tunable and the photocurrent generation mainly depended on the photoconductive gain in the semiconducting ReS$_2$, which is almost linear power law dependent in a low bias operation. The turn-on voltage of the diode is modulated via different light intensities (Figure 3a). Rectification ratio under different light intensity is provided in Table S1, Supporting Information. The heterostructure forms a type-II band alignment (inset Figure 3a) with the top optically active ReS$_2$ layer. Photo-excited carrier generation at the ReS$_2$ semiconducting layer and carrier separation across the tunnel layer of h-BN to the conducting material Gr make further tuning the diode performance, which is more prominent in the FN-tunneling region. Thus, in the positive high drain bias (forward bias) region we have observed a high photogenerated current (Figure 3a), which has an almost linear power dependence at a different bias (Figure 3b). On the other hand, possible defect and/or trap states located between the Gr Fermi level and the ReS$_2$ valence band enable hole transfer from Gr to ReS$_2$ via the h-BN layer. In one possible scenario the accumulated holes in h-BN defect states will further transfer to ReS$_2$ since a type-I band alignment is formed between the h-BN defect states and ReS$_2$. The photogenerated current is tunable under a global gate bias as shown in Figure 3c under different drain biases. It
should be noted that the photocurrent slowly increases as the gate bias increases from −60 V to +60 V (Figure 3d).

Next, we investigate logic gate operation using parallel MIS-type diodes with a low turn-on voltage, which can be used for more complex and functional electronic devices. It should be mentioned that an assembly of more MIS-type diodes would produce a multiple-input-based OR gate logic operation.

We demonstrated a simple circuit, where tunneling diodes are connected in parallel to the output voltage monitor to form logic circuits. “OR” logic gate operation is demonstrated. The input bias at the diodes can be either high or low and the obtained output is always high (Figure 4a, b). 3D schematic (Figure 4b inset) for the diode with a V_in drain terminal at Gr, where a pair of ReS_2/h-BN/Gr diodes with a common source terminal at the ReS_2 is at the V_out monitor along with another diode in parallel as shown in the inset of the Figure 4b schematic measurement circuit. The output voltage levels were monitored with the four possible logic address level inputs: (0,0); (0,1); (1,0); (1,1). Here, the logic 0 input is −2 V and the logic 1 input is +2 V. In this circuit, the output is low (logic 0) when both input voltages are low (−2 V), and the output is high (logic 1), when either or both of the input voltages are high (+2 V). The output voltage levels (Figure 4b, d) resemble the “OR” logic gate operation as shown in the Figure 4d inset truth table. As different diodes have different ON currents, turn-ON voltages and/or ON (forward)/OFF (reverse) current ratios, the “1” state of the logic output voltage shows a slight periodic modulation with time (Figure 4b). Small modulations in the output voltage at a high level (logic 1, Figure 4b) do not affect the basic operation of the logic gates because the low turn-on voltage contributions are reproducible and can be readily accounted for when defining the 0 and 1 logic states. If both inputs are logic low or high, which change periodically as shown in Figure 4c, then the output voltage (Figure 4d) we record is low or high in the same frequency and it alters in accordance with the input frequency. We have shown the “OR” logic gate operation for multiple inputs in Figure S4, Supporting Information. Similarly, another logic gate (“AND” logic) operation can be demonstrated as shown in Figure S5, Supporting Information. Due to high rectifying characteristics, these diodes can be used as temperature independent logic gate components.

2.2. FETs at Low Threshold Voltage and Memory Operation Demonstration

A similar vertical heterostructure can be further explored for various electronic devices including a FET with low bias operation and an NVM. Here, we further explored the possibility of using the same device structure by changing and arranging the electrode connection in the circuit. Various applications including diodes, logic gates, transistors, and memory operation confirm the possibility of using a multifunctional device, whose individual functionality can be tuned further under laser
light excitation to allow the possibility of use in the optoelectronics domain. First, a few-layer h-BN gate dielectric with a thickness of \( \approx 9 \) nm is used for ReS\(_2\) FET operation, where the bottom Gr electrode is used as a gate terminal. The local gated ReS\(_2\) FET performance, that is, the transfer and output characteristics, are shown in Figure 5a,b. As the positive gate bias at Gr terminal is gradually increased, the Fermi level enters the higher conduction band of a large density of states indicating the strong capacitive coupling of the chemical potential of Gr to the electronic band in the few layer ReS\(_2\) channel (Figure 5a).

This ReS\(_2\) transistor exhibits a clear n-type characteristic with an ON/OFF current ratio of \( \approx 10^4 – 10^5 \). The output characteristics are slightly non-linear in the low bias region, which could be due to the formation of asymmetric contact and their asymmetric gate field modulation. Notably, the gate modulated drain current was observed at a low gate bias of 2V, which makes it possible to demonstrate ReS\(_2\) FETs that operate at low power. A very low negative threshold voltage (\(-0.16\) V) further confirms the natural n-doping conductance of the few layer ReS\(_2\) channel, which is advantageous in terms of building a CMOS circuit for low power operation. ReS\(_2\) FETs with h-BN as their back gate dielectric provide superior transistors with negligible hysteresis in the transport characteristics. This could be due to the atomically flat 2D surface of the dielectric and channel material with a 2D atomically thin gate with the absence of interface defect states. Compared with the \( p^{++}\)Si back-gated few-layer ReS\(_2\) channel-based FET device (Figure 2a), this Gr/h-BN/ReS\(_2\) FET device has a high threshold voltage for low power operation.

On other hand, we can use same heterostructure as an NVM device as shown in Figure 5c,d. In this memory application, Gr acts as a floating gate that stores charges from the ReS\(_2\) channel material. With global gate \( p^{++}\)Si control FET operation, the sweep-gate-bias-dependent drain current exhibits a large hysteresis (Figure 5a, Figure S6 on logarithmic scale), which indicates a memory operation with a large memory window that depends on the applied gate bias value. Here a high positive and negative gate electric field with a small drain bias induced carrier tunneling across a thin h-BN layer (\( \approx 9 \) nm thickness) to store and erase carriers in the floating gate Gr layer and thus demonstrate the two memory states of the device operation, namely write/program (binary "1") and erase (binary "0"). Good data retention properties of the NVM devices were achieved in the time range of \( \approx 10^4 \) s (Figure S7, Supporting Information). The transfer characteristics \( I_d – V_g \) for different gate bias \( V_g \) (max) ranges represent large hysteresis windows, which can be tuned by the maximum gate bias (Figure S8, Supporting Information). The details of NVM operation with extended multilevel operation under laser excitation with a similar device structure have been reported elsewhere.\(^{25}\) Here, we achieved NVM operation under a moderate electric field with a \(+/-10\) V gate bias, which can be further reduced if we use high quality h-BN as the dielectric layer for the control gate \( p^{++}\)Si instead of using a SiO\(_2\) dielectric layer. For an all 2D-material-based NVM device.
with low gate bias operation, the FG-Gr can be isolated by both a top h-BN (≈6–10 nm thick) and a bottom h-BN (≈30–40 nm thick) subsequently insulated with another bottom Gr as a control gate electrode. That multi-stack heterostructure will help us to realize a NVM memory device operating at very low power for multibit applications, which will be further studied in future work with extra functionality and a laser tunable optoelectronic NVM device. We have discussed various uses starting with vertical MIS-type diodes, low power transistor operation, logic gate operation and memory device applications for future ultrathin nanoelectronics based multifunction devices.

3. Conclusion
We described various multifunctional electronic devices with an ReS₂ based 2D heterostructure. We reported a vertical MIS-like configuration as a quantum tunneling diode structure and the logic gate operation when using tunnel diodes with a detailed characterization of the gate electric field dependence, temperature dependence and incident light excitation. The vertical geometry can lead to the high rectification of tunnel devices with an atomically flat 2D surface as a high tunneling area for a large turn-ON current. The fabricated parallel diodes facilitate both DT at a lower field strength and FN tunneling with the use of a high-strength electric field, which we used to design logic gates that depended on the various combinations we used. We obtained a large rectification, low ideality factor, temperature independent tunnel diodes and their “OR” logic gate operation. We demonstrated ReS₂ FETs operating at a low bias and an NVM device with a large memory window in the same heterostructure device. These devices are candidates for future 2D ultrathin electronic devices, namely diodes, transistors and memory devices, as building blocks for logic circuits in next generation VLSI architectures, which can potentially enable all-optical logic processing and quantum information processing in the modern smart IoT technology.

4. Experimental Section

Device Fabrication and Measurement Techniques: Standard dry-transfer techniques[31,32] were used to prepare a heterostructure consisting of ReS₂, h-BN and Gr. Initially a SiO₂ (285 nm)/Si substrate was used, which was treated with oxygen plasma to remove contaminants and to induce surface modification with functional silanol groups (Si-OH).[28] Then mechanically exfoliated Gr flakes from highly oriented pyrolytic graphite (HOPG) were deposited on the surface of the plasma treated SiO₂ at a substrate temperature of 180 °C. Next an h-BN layer and ReS₂ flakes were transferred to the top of the Gr/SiO₂ sample using the dry transfer procedure. Standard electron beam lithography (EBL, ELS-7000, FT125 KV) techniques were used to pattern the electrodes on the fabricated heterostructure device. An electron beam sputtering unit was used to deposit Cr/Au (Cr: 5 nm in 0.03 nm/s deposition rate, Au: 50 nm, 0.15 nm s⁻¹ deposition rate in a high vacuum of 10⁻⁵ Pa).

All electrical measurements were performed with the standard two-probe and three-probe measurements configuration. The
current–voltage (I–V), current–time (I–t) and all the optoelectrical characteristics (photocurrent-time) of the device were measured using an Agilent 2636A and a semiconductor device analyzer (Agilent B1500A) source-measurement unit. The devices were tested in a high-vacuum chamber (5 × 10⁻³ Pa) in a Lakeshore probe station at room temperature. A diode laser (532 nm, diode-pumped solid-state DPSS laser) was used for the optoelectrical response. An atomic force microscope (Nikon/SHIMADZU, model SPM-9700HT, scanning probe microscope) and a Raman microscope (Nanophoton, model Ramanplus, 532 nm laser, with ×100 – 0.9 N.A. objective lens and 1200 lines/mm grating) were used for the thickness measurement and sample characterization, respectively.

Supporting Information
Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements
This research was supported by the World Premier International Center (WPI) for Materials Nanoarchitectonics (MANA) of the National Institute for Materials Science (NIMS), Tsukuba, Japan with a Grant-in-Aid for Scientific Research (JSPS KAKENHI Grant No./Project/Area No. 17F17360). A part of this study was supported by the NIMS Nanofabrication Platform and NIMS Molecule & Material Synthesis Platform in Nanotechnology Platform Project sponsored by the Ministry of Education, Culture, Sports, Science, and Technology (MEXT), Japan.

Conflict of Interest
The authors declare no conflict of interest.

Keywords
2D materials, graphene, heterostructures, multifunctional devices, ReS₂, tunnel diodes

Received: September 22, 2020
Revised: November 5, 2020
Published online: November 30, 2020

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