Three-Dimensional TID Hardening Design for 14 nm Node SOI FinFETs

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Abstract: The fin field-effect transistor (FinFET) has been the mainstream technology on the VLSI platform since the 22 nm node. The silicon-on-insulator (SOI) FinFET, featuring low power consumption, superior computational power and high single-event effect (SEE) resistance, shows advantages in integrated circuits for space applications. In this work, a rad-hard design methodology for SOI FinFETs is shown to improve the devices’ tolerance against the Total Ionizing Dose (TID) effect. Since the fin height direction enables a new dimension for design optimization, a 3D Source/Drain (S/D) design combined with a gate dielectric de-footing technique, which has been readily developed for the 14 nm node FinFETs, is proposed as an effective method for SOI FinFETs’ TID hardening. More importantly, the governing mechanism is thoroughly investigated using fully calibrated technology computer-aided design (TCAD) simulations to guide design optimizations. The analysis demonstrates that the 3D rad-hard design can modulate the leakage path in 14 nm node n-type SOI FinFETs, effectively suppress the transistors’ sensitivity to the TID charge and reduce the threshold voltage shift by >2×. Furthermore, the rad-hard design can reduce the electric field in the BOX region and lower its charge capture rate under radiation, further improving the transistor’s robustness.

Keywords: SOI FinFET; 14 nm node; TID hardening; design methodology; TCAD simulation

1. Introduction

The fin field-effect transistor (FinFET) has been the mainstream technology on the VLSI platform [1–5]. In the past decade, FinFETs have been aggressively scaled, and the 14/16 nm node is currently the most widely used technology. In comparison with traditional devices, an ultra-thin fully depleted channel and high-κ gate dielectric technology are adopted in FinFET [2], contributing to its superior short-channel effect suppression as well as performance enhancement. The superior performance and low power consumption in advanced FinFET VLSI meet the requirements of computational power and energy efficiency in future aerospace electrical systems. Moreover, FinFET based on the silicon-on-insulator (SOI) process can largely suppress the impact of transient currents induced by a single-event effect (SEE). By isolating the active channel and the substrate using the buried oxide (BOX) layer [6,7], SEE-induced soft errors can be prevented. Moreover, SOI FinFET exhibits a comparable tolerance to the Total Ionizing Dose (TID) radiation to the bulk counterpart [8] and thus guarantees its survivability in space application. Therefore, because of its superior performance and radiation tolerance, SOI FinFET shows great potential in future aerospace electronic devices.

Despite the superior SEE tolerance, SOI devices and ICs are sensitive to the Total Ionizing Dose (TID) effect [9–11], causing critical limitations to their applications in long-term missions such as deep space explorations. More importantly, device scaling brings new challenges regarding the TID tolerance in advanced technology nodes [12–14]. When the channel length is reduced from 130 nm to 50 nm, the threshold voltage shift ($\Delta V_{TSAT}$) caused by the TID effect increases by 2–3× [12]. Furthermore, geometry scaling is expected...
to degrade the transistors’ TID tolerance. Therefore, SOI FinFETs’ TID hardening is of extensive significance for their application in deep space missions.

To enhance the IC’s lifetime under radiation, transistors’ TID hardening techniques have been widely investigated, as shown in Table 1 [15–19]. By adopting the double SOI structure [15,20,21] or the ground plane implantation method [16], the body bias can be utilized to cancel out the $\Delta V_{TSAT}$. In the dummy gate-assisted SOI [17] or by adjusting the back-channel implantation [18], the built-in potential is utilized to suppress the TID-induced leakage current. STI material optimization [19] has also been proposed for TID hardening in planner SOI transistors. However, these techniques, designed based on planner processes, are not compatible with the commercial SOI FinFET process flow. Despite various works that have investigated FinFETs’ TID tolerance and the effect’s governing mechanism [12–14,22–24], to the authors’ best knowledge, few have proposed a process-compatible rad-hard design. Therefore, it is absolutely critical to propose a TID hardening design methodology for SOI FinFETs.

Table 1. Reported TID hardening methodology based on SOI technology and their compatibility with SOI FinFETs.

| Reference                | TID Hardening Methodology                      | SOI FinFET Compatible |
|--------------------------|------------------------------------------------|------------------------|
| Y. Huang et al. [15]     | Double SOI                                     | N                      |
| M. Gaillardin et al. [16]| Ground plane implantation under the BOX        | N                      |
| Y. T. Roh et al. [17]    | Dummy gate-assisted SOI                        | N                      |
| C. Liu et al. [18]       | Back-channel adjustment                        | N                      |
| C. Peng et al. [19]      | STI oxide nitridation                          | N                      |
| This work                | 3D S/D & gate dielectric optimization          | Y                      |

In this work, 14 nm node SOI FinFET’s TID sensitivity is systematically investigated to guide design optimization. Since the fin height direction enables a new dimension for design optimization, a three-dimensional (3D) Source/Drain (S/D) design combined with a gate dielectric de-footing technique—developed by the Institute of Microelectronics, Chinese Academy of Science (IMECAS) [25,26]—is proposed for SOI FinFETs’ TID hardening. Fully calibrated TCAD analysis shows that the rad-hard design can effectively suppress the transistors’ sensitivity to the TID charge and reduce the $\Delta V_{TSAT}$ by $\geq 2\times$. At the same time, the reduced electric field in the BOX region can lower its charge trapping rate under radiation, further improving the transistor’s TID tolerance.

2. 3D Design for TID Hardening

To improve the TID tolerance in 14 nm node SOI FinFET devices, a radiation hardness design combining a 3D S/D design and a gate dielectric de-footing process is proposed. The schematics of the rad-hard SOI FinFET are shown in Figure 1. The objective of the 3D design is to enhance the gate electrostatic control near the fin bottom.
The S/D module engineering has been shown to be a critical factor for DC/analog performance enhancement in sub-14 nm nodes [27–29]. Advanced S/D formation technologies, such as the 3D S/D recess and re-epitaxy [27] adopted by Applied Materials and IBM as well as the 3D spacer formation technique [25] integrated with IMECAS’s FinFET process, have been developed to precisely control the vertical profile (in the fin height direction). These technologies enable new dimensions of freedom for design optimizations. Compared to the conventional vertically uniform S/D module (Figure 1a), the proposed 3D S/D design features a suppressed local dopant encroachment near the sub-fin (Figure 1b), forming a vertically non-uniform profile featuring reduced dopant encroachment near the fin bottom. In this work, the 3D S/D developed by IMECAS (Figure 2a) [25] is utilized for TID hardening. In this process, the local spacer thickness is controlled to be much larger than the value of that near the fin top. Ions are obliquely implanted into the source and drain region, leaving a relatively lightly doped fin bottom blocked by the local spacer. The 3D S/D design increases the effective channel length near the fin bottom, reducing the local drain fringing field and improving the local electrostatic control [30].

In addition, a gate dielectric optimization, featuring reduced gate dielectric thickness and enhanced electrostatic control near the fin bottom, can be adopted for TID hardening. The corresponding processes have been successfully integrated into commercial and research FinFET platforms [2,31]. By over-etching the BOX in the sacrificial SiO$_2$ removal process [25], the dielectric fin foot (Figure 1c) can be removed, reducing the gate dielectric thickness near the fin bottom (Figure 1d). Therefore, the local gate electrostatic control can be improved with minimal modification in the process flow.

Figure 1. Comparison between a conventional SOI FinFET and the proposed 3D design. (a) A 3D schematic of a conventional SOI FinFET with a vertically uniform S/D, (b) a 3D schematic of the SOI FinFET with the proposed 3D S/D design, (c) the fin cross-section in a conventional SOI FinFET and (d) the fin cross-section in with an optimized gate dielectric.
3. Results and Analysis

3.1. Structure Setup for TID Hardening Evaluation

To evaluate the effectiveness of the rad-hard design, numerical simulations are utilized to compare the TID’s impact on device performance in both conventional SOI FinFETs and the proposed rad-hard design. The simulated structures are shown in Figure 2. The rad-hard design combines the 3D S/D design (Figure 1b) and the gate dielectric optimization (Figure 1d). In advanced technology nodes, both the device performance and the TID effect have become increasingly sensitive to detailed geometry parameters [10–14,27–29]. Therefore, realistic module parameters instead of idealized geometries are required to improve the accuracy of the analysis. This study refers to the 14 nm node FinFET experimental results (Figure 3) fabricated by IMECAS. In realistic FinFETs, a taper angle is designed in the fin etching process to ensure the mechanical reliability of the structure. In the gate dielectric formation process, a SiO$_2$ layer is formed by surface oxidation before the high-k dielectric deposition to reduce the interface defect concentration. The oxidation rate at the fin bottom is higher than that near the fin top, resulting in an oxide fin foot with a thicker interfacial layer and a larger equivalent oxide thickness (EOT). In this work, key parameters such as the active fin’s geometry and the channel length are set according to the TEM parameter extraction results (Table 2). FinFETs with both conventional and optimized S/D and the gate dielectric modules are simulated and compared.

Figure 2. Simulated SOI FinFET structures for TID hardening evaluation. (a,b) 3D schematics of a conventional design and the proposed rad-hard design, respectively; (c,d) fin cross-sections in a conventional device and the rad-hard device, respectively.
Figure 3. The 14 nm node FinFET process results for physical parameter extraction. (a) The 3D S/D’s TEM and (b) the fin geometry fabricated by IMECAS [25]. The extracted physical parameters are listed in Table 2.

Table 2. Physical parameters used in 14 nm node SOI FinFET simulations.

| Physical Parameters                        | Conventional Design | Rad-Hard Design |
|-------------------------------------------|---------------------|-----------------|
| Fin top width (nm)                        | 10                  |                 |
| Fin height (nm)                           | 25                  |                 |
| Fin pitch (nm)                            | 40                  |                 |
| Taper angle (°)                           | 79                  |                 |
| Channel length (nm)                       | 20                  |                 |
| Fin top spacer length (nm)                | 10                  |                 |
| S/D doping concentration (cm⁻³)           | 2 × 10²⁰             |                 |
| Channel doping concentration (cm⁻³)       | 10¹⁶                |                 |
| Junction doping diffusion gradient (nm/dec)| 5                  |                 |
| Fin top EOT (nm)                          | 1.0                 |                 |
| Fin bottom spacer length (nm)             | 10                  | 30              |
| Fin bottom EOT (nm)                       | 1.2                 | 1.0             |
| Oxide footing                             | Yes                 | No              |

3.2. Physical Model Setup

In this work, Sentaurus TCAD tools [32] are used to evaluate the effectiveness of the rad-hard design. A density gradient model is used to accurately capture the carrier quantum confinement in the active fins. A drift-diffusion model with modified saturation velocity [33] and thin-film mobility [4,34] is used to emulate the quasi-ballistic transport. The simulation platform can accurately predict the performance of 14/10 nm node FinFET [29], adding credibility to this analysis. According to [35], it is not high-κ gate dielectric technology but the BOX that is most sensitive to TID irradiation. Therefore, a uniformly distributed charge layer is added to the active fin/BOX interface to investigate the device’s TID response and the charge density is set to be 4 × 10¹¹ cm⁻², corresponding to the trapped charge generated by the 1Mrad(Si) TID irradiation [36–38].

3.3. TID Hardening Result

The proposed rad-hard design improves the TID tolerance of the device by reducing the sensitivity of it to TID charges. The transfer characteristics of the 14 nm node SOI FinFETs with and without rad-hard design are shown in Figure 4. The rad-hard design can effectively reduce the TID-induced ΔV_{TSAT} (defined as a constant current threshold voltage and extracted at I_{DS} = 1 μA/μm) from 109 mV to 53 mV (factor >2×). It is also worth noting that the rad-hard design does not degrade device performance. The simulated SOI FinFETs’ electrical parameters are listed in Table 3. It is worth noting that the 3D design features a 14 mV/dec improved SS, together with a 15% higher I_{ON} compared to conventional
SOI FinFETs, suggesting that TID hardening can be achieved without sacrificing device performance.

Figure 4. Comparison of the (a) log scale and (b) linear scale transfer characteristics’ drift caused by the total dose radiation in SOI n-FinFETs with and without reinforcement.

Table 3. Simulated electrical characteristics of 14 nm node SOI FinFETs with various designs and radiation conditions.

| Electrical Characteristics | Conventional Design before Radiation | Conventional Design after Radiation | 3D Design before Radiation | 3D Design after Radiation |
|---------------------------|-------------------------------------|-----------------------------------|---------------------------|--------------------------|
| Threshold Voltage (V)     | 0.329                               | 0.220                             | 0.258                     | 0.205                    |
| On-state Current (A/µm)   | $5.80 \times 10^{-4}$               | $6.85 \times 10^{-4}$             | $6.71 \times 10^{-4}$     | $7.17 \times 10^{-4}$    |
| Off-state Current (A/µm)  | $1.0 \times 10^{-10}$               | $3.5 \times 10^{-9}$              | $1.0 \times 10^{-10}$     | $8.2 \times 10^{-10}$    |
| Sub-threshold Swing (mV/dec) | 79.0                 | 85.9                             | 64.9                      | 67.4                     |
| Transconductance (mS/µm)  | 1.96                                | 2.13                              | 1.51                      | 1.56                     |

3.4. Analysis and Discussion

3.4.1. TID Effect’s Mechanism in SOI FinFETs

The most significant impact of the TID effect is the $\Delta V_{\text{TSAT}}$ [9–11], which is governed by two factors: the trapped charge density and its coupling to the sub-threshold current path. The first factor is proportional to the electric field perpendicular to the channel/BOX interface [38]. The second factor is determined by the distance between the current path and the BOX (where the trapped charge exists). Therefore, the TID’s impact can be effectively suppressed by reducing the electric field in the BOX together with shifting the leakage current towards the fin top.

In FinFETs with a realistic tapered fin, the sub-threshold current’s distribution is controlled by the local gate electrostatic control as well as the drain fringing field [29]. In an SOI FinFET with a 150 nm $L_G$ (Figure 5a), the drain fringing field is relatively weak, resulting in an almost uniform sub-threshold energy barrier profile in the channel (Figure 5b). The current density is higher near the fin top, which is caused by the extra top gate control (Figure 5c). Therefore, its coupling effect to the TID-induced trapped charge is reasonably weak. Meanwhile, the low drain fringing field leads to a moderate off-state electric field in the BOX (Figure 5d) and a relatively low charge-trapping rate, further suppressing the transistor’s sensitivity to the TID irradiation.
Figure 5. Simulation results of a long channel ($L_G = 150 \text{ nm}$) SOI n-FinFET. (a) Schematics of the simulated device, (b) the potential energy distribution in channel region, (c) the sub-threshold current distribution in the tapered fin and (d) the distribution of the electric field in the BOX perpendicular to the channel/BOX interface.

However, the TID’s impact becomes more critical as the transistors scale down. This is dominated by the drastically increased drain fringing field in ultra-scaled devices. In a tapered fin, the local $T_{Si}$ near the fin bottom is larger than that near the fin top (Figure 2c) and thus results in a reduced local gate electrostatic control. This phenomenon has been thoroughly discussed in [30,39]. Therefore, the drain fringing field has a stronger impact on the virtual cathode (analogous to the DIBL effect in planar FETs), forming a localized virtual cathode (Figure 6a). Instead of forming an almost uniform current distribution in the SOI FinFET with a 150 nm $L_G$ (Figure 5c), a localized sub-threshold current path is formed near the fin bottom (Figure 6b). The reduced distance between the current path and the BOX results in an extensively stronger coupling, increasing the TID’s impact on device performance. TCAD simulations show that the device becomes significantly more sensitive to the TID irradiation. The $\Delta V_{TSAT}$ induced by a $4 \times 10^{11} \text{ cm}^{-2}$ TID charge increases by 48 mV (from 61 mV to 109 mV, 1.8×) as the $L_G$ scales (Figure 7). This trend is consistent with experimental results [22], adding credibility to the analysis. In addition, the higher electric field in the BOX (Figure 6b) also increases the charge trapping rate [38], further reducing SOI FinFET’s TID tolerance. Therefore, it is of great significance to develop a TID hardening technique for ultra-scaled SOI FinFETs.
Figure 6. Simulation results of the 14 nm node SOI n-FinFET without TID hardening. (a) The potential energy distribution in channel region, (b) the sub-threshold current distribution in the tapered fin and (c) the distribution of the electric field in the BOX perpendicular to the channel/BOX interface.

Figure 7. Comparison of the (a) log scale and (b) linear scale transfer characteristics’ drift caused by the total dose radiation in long channel ($L_G = 150$ nm) and 14 nm node ($L_G = 20$ nm) SOI n-FinFETs.

3.4.2. TID Hardening Methodology

Physical interpretation shows that the relatively low TID tolerance in conventional 14 nm node SOI FinFET is strongly influenced by the localization of the sub-threshold current path. Therefore, the TID hardening design focuses on suppressing the drain fringing field and improving the gate electrostatic control, especially near the fin bottom where the leakage path occurs. This can be effectively achieved by combining the 3D S/D module and the gate dielectric de-footing process (Figure 8a). The former suppresses the fin bottom dopant encroachment and reduces the local drain fringing field [29], while the latter enhances the local gate electrostatic control. Both optimizations contribute to increasing the barrier energy near the fin bottom, resulting in a virtual cathode shifted...
towards the fin top (Figure 8b). The sub-threshold current path modulation (Figure 8c) suppresses the coupling effect to the trapped charge in the BOX and therefore reduces the $\Delta V_{TSAT}$ by $>2\times$, as shown in Figure 4.

4. Conclusions

In this work, an innovative TID hardening design, combining a 3D S/D doping technique and a gate dielectric de-footing process, is proposed for 14 nm node SOI FinFETs, and the optimization methodology is well established. The strong coupling between the localized leakage path near the fin bottom and the radiation-induced trapped charge in the BOX is identified as the dominating factor in the increasingly critical TID effect in aggressively scaled SOI FinFETs. By improving the gate electrostatic control close to the fin bottom, the rad-hard design can effectively shift the leakage path toward the fin top. As a result, the $\Delta V_{TSAT}$ is effectively reduced by $>2\times$ from 109 mV to 53 mV without degrading device performance. Moreover, the TID charge capture rate is also reduced by suppressing the electric field in the BOX, further enhancing the device's robustness. The optimization methodology in this work can provide guidance for irradiation resistance improvement in advanced devices, paving the way for their application in future deep space exploration missions.
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