TCAD based study of parameters affecting the electrical performance of organic thin-film transistors

Abhishek Singh and Manish Kumar Singh*

Department of Electronics Engineering, Harcourt Butler Technical University, Kanpur, UP, INDIA-208002

* E-mail: manish.rs.mst14@iitbhu.ac.in

Abstract – Field effect transistors (FETs) are widely used in integrated circuits of electronic devices. Mostly silicon-based FETs are used for commercial purposes, but with the recent advancement in organic electronics – organic thin-film transistors (OTFTs) have become trending research topics nowadays. Modeling of organic FETs helps in understanding various electrical characteristics of the device such as on current, threshold voltage, off current, on/off ratio, and so on. Optimization of these factors is needed to enhance the working and overall performance of thin-film transistors. In this paper, the comparative study of the device having bottom-gate with electrode contact on top and bottom of organic semiconductor has been done based on the effects of organic semiconductor's thickness variation, dielectric thickness variation, and dielectric material variation on pentacene based organic transistors.

Keywords – Poole-Frenkel mobility, the density of defect states, oxide capacitance, bottom-gate configuration, On/off ratio.

1. Introduction

Organic electronics is developing fast, and numerous researches are going on in this field as it provides specific additional features over conventional silicon-based electronics such as – low-temperature processing, mechanical flexibility, low cost, and so on. Various flexible substrates like glass [1], plastic [2], etc., are used in making different organic devices – organic transistors, light-emitting diodes [3], radio frequency identification tags (RFIDs), active-matrix displays, sensors providing flexibility and cheaper cost of production as an additional benefit [4-7]. Earlier polythiophene was considered as an insulator and was mostly used in the packaging industry, but later in 1978 Heeger et al. developed charge transport phenomenon in the organic material and then later more research were reported in this field to enhance the mobility of the organic materials for its efficient application in the electronic devices as active material [8-9].

An organic transistor or organic thin-film transistor (OTFT) consists of organic semiconductor (OSC) compounds as an active layer material and consists of three electrodes – gate, drain, and source. By applying a variable voltage at the gate terminal, the output current of the device is controlled, and it can be made to operate in three different regions – cut off, linear, and saturation [10]. Unlike silicon-
based metal insulator semiconductor field-effect transistor (MISFET), organic transistor works in the accumulation mode. There are various geometries of OTFT depending on the location of the electrode placed concerning the OSC and oxide – 1. Top gate configuration, and 2. Bottom gate configuration [11-12].

Finite element modeling and analytical modeling techniques are used to understand the various electrical characteristics such as - off current, threshold voltage, on current, and so on, which helps in designing and enhancing multiple electrical characteristics of devices [13]. Here, in this paper, finite element-based modeling and simulation of 2D pentacene-based OTFT have been performed using SILVACO ATLAS tool. Performance and analysis of bottom-gate configuration-based devices have been done and effect on various electrical parameters – off current, on/off ratio, on current, threshold voltage, sub-threshold swing, on varying channel length, an oxide material, oxide thickness, and electrode material is being discussed.

2. Device Structure

In the bottom-gate device configuration, the gate is placed at the bottom of the device, and based on the location of the other two contacts – drain and source with respect to OSC; it's further divided into two types – a. Top contact, and b. Bottom contact, as shown in figure 1.

![Figure 1. Bottom gate schematic of OTFT (a) Bottom gate top contact (BGTC), (b) Bottom gate bottom contact (BGBC).](image)

In order to compare different electrical characteristics of bottom gate top contact and bottom gate bottom structure, channel length variation has been done from 2.5 µm to 40 µm, different oxide material having a different dielectric constant varied from 3 to 23 was used. Pentacene was used as the organic semiconductor material, source, and drain electrode of Aluminium having thickness 20 µm, and the gate electrode of gold with thickness 20 µm were simulated. Various device dimensions taken into consideration are summarized in table 1.
Table 1. Various device dimensions used in the bottom-gate configuration

| Dimensional Parameters                        | Values  |
|-----------------------------------------------|---------|
| The thickness of the source and the drain electrode | 30 µm   |
| The thickness of the gate electrode           | 20 µm   |
| Length of channel                             | 10 µm   |
| Width of channel                              | 220 µm  |
| Organic semiconductor thickness               | 30 nm   |
| Dielectric thickness                         | 5.7 nm  |

3. Atlas simulation

Finite element-based simulation of bottom-gate configuration OTFT is performed using SILVACO ATLAS TCAD tool. This tool does the simulation on the finite elements of the devices based on the various equations and models. There are different mobility models, and as per the requirements, the correct mobility model has been chosen, and fine meshing of the device has also been performed in order to get more accurate analysis and results.

Poisson’s and continuity equations are used by ATLAS to measure different electrical characteristics of these devices. Poole-Frenkel (PF) mobility model describes the mobility of charge carriers in organic transistors. ATLAS uses these equations along with other comparisons as per the device modeling and helps in studying and analyzing different results as per need.

3.1 Poisson’s equation

It defines the relation between local charge densities and electrostatic potential. It is expressed by the relationships shown in equations 1 and 2.

\[
\nabla \cdot (\varepsilon \nabla \Psi) = -\rho \tag{1}
\]

\[
\nabla \cdot (\varepsilon \nabla \Psi) = -q(p - n + N_d^+ - N_a^-) \tag{2}
\]

Where \(\varepsilon\) represents local permittivity of semiconductor, \(\Psi\) represents electrostatic potential, \(\rho\) represents local space charge density, \(n\) represents electron density, \(p\) represents hole density, \(N_a^-\) represents ionized acceptor density and \(N_d^+\) represents ionized donor density. Intrinsic Fermi potential is always taken as a reference potential in simulation by this tool. Resultant of all fixed and mobile charges, including holes, electrons, and ionized impurities, are taken as local space charge density [14].

3.2 Continuity equation

For holes and electrons, equation 3 and 4 represents a continuity equation.

\[
\frac{\partial n}{\partial t} = \frac{1}{q} \nabla J_n + G_n - R_n \tag{3}
\]

\[
\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla J_p + G_p - R_p \tag{4}
\]

Where \(p\) and \(n\) represent hole and electron concentrations, \(J_p\) and \(J_n\) represent hole and electron current densities, \(G_p\) and \(G_n\) represent generation rates for holes and electrons, \(R_p\) and \(R_n\) represent recombination rates for holes and electrons respectively, and \(q\) represents fundamental electronic
charge. ATLAS tool uses both the continuity equation in simulation; however, as per the specific model, a particular equation can be chosen to work while others can be deactivated for that model [14].

3.3 Poole Frenkel Mobility model
There are numerous models available in this tool, and as per the requirement of the device modeled, particular mobility model(s) can be set as active, and simulation will be performed as per the model selected. PF mobility model was used in the simulation of pentacene based OTFT. This model is represented by equation 5

\[
\mu(E) = \mu_0 \exp\left[\frac{\Delta}{kT} + \left(\frac{\beta}{kT} - \gamma\right)\sqrt{E}\right]
\]

Where \(\mu_0\) represents zero-field mobility, \(\mu(E)\) represents field-dependent mobility, \(\Delta\) represents zero-field activation energy, \(k\) represents Boltzman constant, \(E\) represents an electric field, \(\gamma\) represents a fitting parameter, \(\beta\) represents Poole-Frenkel factor, and \(T\) is the temperature. Trapped charges carriers are thermally excited due to the enhanced field, and Poole-Frenkel conduction takes place [15].

3.4 The density of defect states
It dominates various properties of polycrystalline or amorphous thin-film transistors. It is defined as the combination of four different components – donor like exponential band tail function \(g_{TA}(E)\), acceptor like exponential band tail function \(g_{TA}(E)\), donor like gaussian deep state function \(g_{GD}(E)\) and acceptor like gaussian deep state function \(g_{GA}(E)\), where \(E\) represents state energy and these terms are defined using relations given in equation (6) - equation(9).

\[
g_{TA}(E) = N_{TA} \exp\left[\frac{E-E_T}{W_{TA}}\right]
\]  
\[
g_{TD}(E) = N_{TD} \exp\left[\frac{E-V}{W_{TD}}\right]
\]  
\[
g_{GA}(E) = N_{GA} \exp\left[-\left[\frac{E-GA}{W_{GA}}\right]^2\right]
\]  
\[
g_{GD}(E) = N_{GD} \exp\left[-\left[\frac{E-E_GD}{W_{GD}}\right]^2\right]
\]

Here, in the above equation, \(E_c\) represents conduction band energy, \(E\) represents trap energy, \(E_v\) represents valence band energy, and subscripts A, D, G, T represents acceptor state, donor state, gaussian (deep level) and tail respectively [14]. Various parameters taken into consideration for device simulation are described in Table 2.

| Parameters | Values |
|------------|--------|
| Effective density of states in valence \((N_v)\) and conduction \((N_c)\) band | \(1 \times 10^{21}\) cm\(^{-3}\) |
| Bandgap at 300K | 2.8 eV |
| Doping concentration | \(7 \times 10^{17}\) cm\(^{-3}\) |
| Permittivity of pentacene | 4.0 |
| The work function of Au (Source & Drain) | 5.1 |
| The work function of Al (Gate) | 4.28 |
| Poole-Frenkel factor (hole) | \(7.758 \times 10^{-5}\) eV(cm/V)\(^{1/2}\) |
| Zero field activation energy (hole) | \(1.792 \times 10^{-2}\) eV |
For better improvement in the device (OTFT) performance such as obtaining low threshold voltage, high output current, higher mobility, higher on/off ratio, etc. various device parameters need to be optimized. The following section describes the effects of various variations done in device specifications done in order to enhance and study their effects on different electrical characteristics.

4. Results and discussion

Modeling and simulation of the drain current characteristics of an organic transistor are supported by the equations 10 and 11 above the threshold voltage for both linear($V_{DS} \ll V_{GS}$) and saturation($V_{DS} \sim (V_{GS} - V_T)$) region of operation respectively when the channel length is in range of 10-50 µm [16].

\[ I_D = \frac{W}{L} \mu C \left[ (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right] \]  
\[ I_D = \frac{W}{2L} \mu C (V_{GS} - V_T)^2 V_{DS} \]  

Where L represents channel length, W represents channel width, µ represents mobility, C represents the capacitance of oxide and is denoted by equation 12

\[ C_{ox} = \frac{\varepsilon_{ox}}{d_{ox}} \]  

The threshold voltage is given by $V_T$, drain to source voltage is given by $V_{DS}$, and the gate to source voltage is given by $V_{GS}$.

4.1 Comparison of the bottom-gate having top contact and bottom contact structure

In both the configurations taken into consideration in this paper, there’s the only structural difference in the placement of source and drain contacts concerning the organic semiconductor. Table 3 shows the various electrical characteristics of both configurations obtained after simulation, as per the data mentioned in table 1 and table 2. Figure 2 shows the transfer curve, which is approximately the same for both the configurations in the lower range of gate voltage; however, when the gate voltage is increased beyond 10V, slight variations can be observed. Hence, the device with bottom contact configuration shows better results with the increment of gate voltage due to unlike path travelled by carriers between source and drain contact [14]. Both the devices show approximately the same results, and as per the requirement and feasibility of device fabrication, any device structure can be chosen.

| Characteristics         | BGTC         | BGBC         |
|-------------------------|--------------|--------------|
| Threshold Voltage (V)   | -0.525       | -0.594       |
| $I_{on}$ (A)            | $-5.723 \times 10^{11}$ | $-6.098 \times 10^{11}$ |
| $I_{off}$ (A)           | $-5.424 \times 10^{15}$ | $-5.387 \times 10^{15}$ |
| Ion/Ioff                | $1.0 \times 10^{4}$  | $1.1 \times 10^{4}$  |
| Subthreshold swing (V/decade) | 0.347      | 0.341        |
4.2 Effect of organic semiconductor thickness variation

The thickness of the organic semiconductor helps in controlling the off current of the device [17]. By reducing the thickness of the organic semiconductor layer, leakage current or off current of the device is reduced, and a very slight improvement in on current is also observed, which eventually enhances the off to on switching speed or on/off ratio of the device. Figure 3 shows the transfer curve of both the configuration indicating a slight variation in the on current. Table 4 shows the variation in different electrical parameters on varying the semiconductor thickness from 10nm to 50nm, and it can be noticed clearly that off current decreases by reducing the thickness of semiconductor, which enhances on/off ratio at smaller thickness. Hence, for reducing the leakage current and enhancing device performance thickness of the semiconductor should be taken as low as possible, taking into consideration that it does not hamper other electrical parameters.

Table 4. Variation in electrical parameters on the varying thickness of semiconductor.

| OSC Thickness | Device Type | Threshold Voltage (V) | $I_{on}$ (A) | $I_{off}$ (A) | $I_{on}/I_{off}$ | Sub-Threshold Swing (V/decade) |
|---------------|-------------|-----------------------|--------------|--------------|-----------------|-------------------------------|
| 10 nm         | BGTC        | -0.629                | $-5.958 \times 10^{-11}$ | $-1.601 \times 10^{-19}$ | $3.737 \times 10^{8}$ | 0.038                         |
|               | BGBC        | -0.661                | $-6.048 \times 10^{-11}$ | $-2.395 \times 10^{-22}$ | $2.540 \times 10^{11}$ | 0.036                         |
| 20 nm         | BGTC        | -0.571                | $-5.558 \times 10^{-11}$ | $-2.301 \times 10^{-18}$ | $2.541 \times 10^{7}$ | 0.048                         |
|               | BGBC        | -0.627                | $-6.091 \times 10^{-11}$ | $-2.223 \times 10^{-18}$ | $2.74 \times 10^{7}$ | 0.062                         |
| 30 nm         | BGTC        | -0.525                | $-5.738 \times 10^{-11}$ | $-5.424 \times 10^{-15}$ | $1.0 \times 10^{4}$ | 0.347                         |
|               | BGBC        | -0.594                | $-6.098 \times 10^{-11}$ | $-5.387 \times 10^{-15}$ | $1.1 \times 10^{4}$ | 0.341                         |
| 40 nm         | BGTC        | -0.484                | $-5.625 \times 10^{-11}$ | $-3.942 \times 10^{-14}$ | $1.4 \times 10^{3}$ | 0.846                         |
|               | BGBC        | -0.560                | $-6.106 \times 10^{-11}$ | $-3.947 \times 10^{-14}$ | $1.5 \times 10^{3}$ | 0.841                         |
| 50 nm         | BGTC        | -0.444                | $-5.546 \times 10^{-11}$ | $-1.055 \times 10^{-13}$ | $5.2 \times 10^{2}$ | 1.143                         |
|               | BGBC        | -0.527                | $-6.112 \times 10^{-11}$ | $-1.057 \times 10^{-13}$ | $5.7 \times 10^{2}$ | 1.138                         |
4.3 Effect of dielectric thickness variation

The dielectric thickness of the oxide used in the organic transistor was varied from 2nm to 10nm, and various electrical characteristics observed for both the configurations are tabulated in Table 5. Transfer curves are shown in Figure 4. On decreasing the thickness of the oxide, the capacitance of oxide is increased as per the relation mentioned in equation 12, which in turn results in the increment of the drain current (on-current). Hence, at lower oxide thickness, the higher drain current is observed, which enhances the on/off ratio and sub-threshold swing. Still, the threshold voltage is increased at lower dielectric thickness compared to higher dielectric thickness.

Figure 3 (a) Transfer curve of BGTC device, (b) Transfer curve of BGBC device
Table 5. Variation in electrical parameters on varying dielectric thickness

| Dielectric Thickness | Device Type | Threshold Voltage (V) | $I_{on}$ (A) | $I_{off}$ (A) | $I_{on}/I_{off}$ | Sub-Threshold Swing (V/decade) |
|----------------------|-------------|-----------------------|--------------|--------------|-----------------|--------------------------------|
| 2 nm                 | BGTC        | -0.611                | $-1.564 \times 10^{-9}$ | $-3.247 \times 10^{-15}$ | $4.87 \times 10^{4}$ | 0.284                          |
|                      | BGBC        | -0.677                | $-1.730 \times 10^{-10}$ | $-3.216 \times 10^{-15}$ | $5.3 \times 10^{4}$ | 0.277                          |
| 4 nm                 | BGTC        | -0.563                | $-8.054 \times 10^{-11}$ | $-4.358 \times 10^{-15}$ | $1.84 \times 10^{4}$ | 0.318                          |
|                      | BGBC        | -0.630                | $-8.676 \times 10^{-11}$ | $-4.322 \times 10^{-15}$ | $2.00 \times 10^{4}$ | 0.312                          |
| 6 nm                 | BGTC        | -0.519                | $-5.446 \times 10^{-11}$ | $-5.624 \times 10^{-15}$ | $9.6 \times 10^{3}$ | 0.352                          |
|                      | BGBC        | -0.588                | $-5.701 \times 10^{-11}$ | $-5.586 \times 10^{-15}$ | $1.0 \times 10^{4}$ | 0.346                          |
| 8 nm                 | BGTC        | -0.477                | $-4.122 \times 10^{-11}$ | $-7.039 \times 10^{-15}$ | $5.8 \times 10^{3}$ | 0.387                          |
|                      | BGBC        | -0.547                | $-4.354 \times 10^{-11}$ | $-7.002 \times 10^{-15}$ | $6.2 \times 10^{3}$ | 0.381                          |
| 10 nm                | BGTC        | -0.437                | $-3.320 \times 10^{-11}$ | $-8.596 \times 10^{-15}$ | $3.8 \times 10^{3}$ | 0.422                          |
|                      | BGBC        | -0.508                | $-3.488 \times 10^{-11}$ | $-8.559 \times 10^{-15}$ | $4.0 \times 10^{3}$ | 0.416                          |
Dielectric material plays a vital role in defining the electrical characteristics of the organic transistor as it helps in determining oxide capacitance, which is directly related to drain current as per the equations 10 and 11. Here, the dielectric material of the device is changed, and materials are taken such that their permittivity varies from 3.9 to 26.0. Table 6 shows the variation in electrical parameters on modifying dielectric material, and Figure 5 shows the transfer curve of both the configuration with a different dielectric material. Materials having high permittivity helps in attaining high oxide capacitance as per equation 12, and thus drain current value is enhanced, but threshold voltage is increased. Hence, in order to enhance the maximum on current threshold voltage is compromised, in addition to this better lower sub-threshold swing is obtained and on/off ratio is enhanced on taking dielectric material having high permittivity.

Table 6. Variation in electrical parameters on varying dielectric material

| Dielectric Material (Permittivity) | Device Type | Threshold Voltage (V) | $I_{on}$ (A) | $I_{off}$ (A) | $I_{on}/I_{off}$ | Sub-Threshold Swing (V/decade) |
|-----------------------------------|-------------|-----------------------|--------------|--------------|------------------|-----------------------------|
| SiO$_2$ (3.9)                    | BGTC        | -0.367                | -2.464 x 10$^{-11}$ | -1.172 x 10$^{-14}$ | 2.1 x 10$^{3}$ | 0.484                      |
|                                  | BGBBC       | -0.439                | -2.573 x 10$^{-11}$ | -1.168 x 10$^{-14}$ | 2.2 x 10$^{3}$ | 0.479                      |
| Si$_3$N$_4$ (7.5)                | BGTC        | -0.497                | -4.648 x 10$^{-11}$ | -6.362 x 10$^{-15}$ | 7.3 x 10$^{3}$ | 0.371                      |
|                                  | BGBBC       | -0.566                | -4.924 x 10$^{-11}$ | -6.323 x 10$^{-15}$ | 7.7 x 10$^{3}$ | 0.365                      |
| Al$_2$O$_3$ (8.5)                | BGTC        | -0.525                | -5.723 x 10$^{-11}$ | -5.424 x 10$^{-15}$ | 1.0 x 10$^{4}$ | 0.347                      |
|                                  | BGBBC       | -0.594                | -6.09 x 10$^{-11}$  | -5.387 x 10$^{-15}$ | 1.1 x 10$^{4}$ | 0.341                      |
| HfO$_2$ (22.0)                   | BGTC        | -0.601                | -1.309 x 10$^{-10}$ | -3.462 x 10$^{-15}$ | 3.7 x 10$^{4}$ | 0.291                      |
|                                  | BGBBC       | -0.666                | -1.437 x 10$^{-10}$ | -3.430 x 10$^{-15}$ | 4.1 x 10$^{4}$ | 0.284                      |
| Ta$_2$O$_5$ (26.0)               | BGTC        | -0.610                | -1.535 x 10$^{-10}$ | -3.267 x 10$^{-15}$ | 4.7 x 10$^{4}$ | 0.284                      |
|                                  | BGBBC       | -0.676                | -1.697 x 10$^{-10}$ | -3.236 x 10$^{-15}$ | 5.2 x 10$^{4}$ | 0.278                      |
Figure 5 (a) Transfer curve of BGTC device, (b) Transfer curve of BGBC device, showing the effect of dielectric material variation.

5. Conclusion

Here, in this paper, it was observed that lower organic semiconductor thickness should be taken in order to lower the leakage current and enhance the on/off ratio. The dielectric thickness should be taken as low as possible in order to design more efficient device characteristics, and lastly, the dielectric material having high permittivity can be taken for the applications requiring higher on current. In all these cases, in order to enhance one particular characteristic, the cost is to be paid by other electrical characteristics. So, while designing a device, all the parameters must be taken into consideration, and a trade-off should be maintained so that a better and enhanced device is made.
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