FSpiNN: An Optimization Framework for Memory- and Energy-Efficient Spiking Neural Networks

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Abstract—Spiking Neural Networks (SNNs) are gaining interest due to their event-driven processing which potentially consumes low power/energy computations in hardware platforms, while offering unsupervised learning capability due to the spike-timing-dependent plasticity (STDP) rule. However, state-of-the-art SNNs require a large memory footprint to achieve high accuracy, thereby making them difficult to be deployed on embedded systems, for instance on battery-powered mobile devices and IoT Edge nodes. Towards this, we propose FSpiNN, an optimization framework for obtaining memory- and energy-efficient SNNs for training and inference processing, with unsupervised learning capability while maintaining accuracy. It is achieved by (1) reducing the computational requirements of neuronal and STDP operations, (2) improving the accuracy of STDP-based learning, (3) compressing the SNN through a fixed-point quantization, and (4) incorporating the memory and energy requirements in the optimization process. FSpiNN reduces the computational requirements by reducing the number of neuronal operations, the STDP-based synaptic weight updates, and the STDP complexity. To improve the accuracy of learning, FSpiNN employs timestep-based synaptic weight updates, and adaptively determines the STDP potentiation factor and the effective inhibition strength. The experimental results show that, as compared to the state-of-the-art work, FSpiNN achieves 7.5x memory saving, and improves the energy-efficiency by 3.5x on average for training and by 1.8x on average for inference, across MNIST and Fashion MNIST datasets, with no accuracy loss for a network with 4900 excitatory neurons, thereby enabling energy-efficient SNNs for edge devices/embedded systems.

Index Terms—Framework, optimization, spiking neural networks, SNNs, spike-timing-dependent plasticity, STDP, unsupervised learning, adaptivity, memory, energy-efficiency, edge devices, embedded systems.

I. INTRODUCTION

T

HE spiking neural networks (SNNs) are rapidly gaining research interest since they have shown great potential in completing various machine learning tasks, while exhibiting high biological plausibility [1]–[5]. That is, the SNNs mimic the behavior of biological spiking networks through (i) event-driven processing, and (ii) spike-timing-dependent plasticity (STDP)-based unsupervised learning. The event-driven processing potentially enables low power/energy computation in the neuromorphic hardware, such as [6] [7], due to its sparse spiking-based computation. The STDP-based learning enables SNNs to learn information from the unlabeled data, which is desired for real-world applications, as gathering unlabeled data is easier and cheaper than labeled data [8]. Thus, SNNs bear the potential to obtain better algorithmic performance (e.g., classification accuracy) with lower power/energy consumption than other neural network algorithms in the unsupervised-learning settings [1].

A. Targeted Research Problem

In an SNN architecture with STDP [9] (depicted in Fig. 1(a)), each excitatory neuron is expected to recognize a class in the dataset, hence the connecting synapses from the same excitatory neuron have to learn the input features of a specific class (a detailed architecture discussion is provided in Section II-A). Previous works [10]–[14] focus on improving the classification accuracy, but at the cost of a huge amount of additional computations, which leads to high energy and high memory footprint. For instance, the state-of-the-art work in [11] improves the effectiveness of the STDP-based learning by updating the weights every two or three postsynaptic spikes, to ensure that the update is essential. This reduces the number of weight updates, but requires a 2-bit counter for each excitatory neuron to keep track of the number of postsynaptic spikes. Moreover, it needs a total of 200 neurons (100 excitatory and inhibitory neurons), to achieve ~74% accuracy in MNIST digit classification [1]. Although all these techniques result in an improvement in the classification accuracy, they incur high computational, energy, and memory costs. This is not desirable for embedded applications with stringent constraints (for instance, in terms of computations, energy, and memory).

Fig. 1. (a) An SNN architecture considered in this work is from [9] [11]. (b) A large-sized SNN typically achieves higher classification accuracy, e.g., the accuracy of an 1MB-sized SNN with a total of 200 neurons (100 excitatory and inhibitory neurons) is lower than a 211MB-sized SNN with a total of 9800 neurons (4900 excitatory and inhibitory neurons) on MNIST [10].

1Note: unlike deep neural networks (DNNs), the research for the unsupervised learning-based SNNs is still in early stage and mostly use small datasets like MNIST and Fashion MNIST. We adopt the same test conditions as used widely by the SNN research community [9]–[15].
In the following, we present a motivational case study to illustrate the compute, memory, and communication requirements for an SNN executing on different hardware platforms, and highlight the associated research challenges.

B. Motivational Analysis and Associated Research Challenges

In Fig. [1](b), we observed that a large-sized SNN typically achieves higher classification accuracy and consumes a larger memory footprint. It shows that to achieve 92% accuracy in MNIST digit classification, the SNN requires a total of 9800 neurons (4900 excitatory and inhibitory neurons) with 3 epochs of training, and consumes more than 200MB of memory. On the other hand, most of the SNN hardwares employ a limited size of on-chip memory (e.g., less than 100MB) [17]–[20], which makes running a large-sized network (whose size is larger than the on-chip memory) energy-consuming. The reason is that this condition requires a high number of memory accesses, whose energy is typically higher than the compute operations [21]–[23]. Previous work in [24] observed that the memory accesses are dominant, consuming about 50%-75% energy of SNN processing in different hardware platforms [17]–[19] (see Fig. 2).

We also observed that there are inefficient computations that hinder SNNs to achieve higher energy-efficiency, that come from complex neuronal and STDP operations. They require exponential calculations for computing the membrane and threshold potential decay, and the synaptic trace and weight dependence, respectively (see details in Section I). Furthermore, there are ineffective STDP operations that come from spurious weight updates, which occur when the synapses of a neuron learn the overlapped features from different classes, thereby degrading the recognition capability of the neuron and also consuming energy. This happens since the general STDP rule updates the synaptic weight every pre- and post-synaptic spike (see details in Section I).

**Required:** An optimization technique is required to reduce SNNs’ memory and energy requirements for both training and inference processing, while maintaining the classification accuracy, thereby enabling their deployment on memory/energy-constrained embedded systems. However, developing such an optimization technique poses different design challenges as discussed below.

**Associated Research Challenges:** The high memory requirements mainly come from a large number of parameters, such as synaptic weights and neuron parameters. Reducing these parameters may degrade the classification accuracy. Hence, the parameter reduction should be done by identifying and eliminating the non-significant parameters. Furthermore, bit-width quantization may also be employed, but it can also lead to accuracy degradation. To overcome the limitations of the above optimization methods, the targeted research question is: if and how can we refine the STDP-based learning technique such that the classification accuracy is improved at minimal overhead.

C. Our Novel Contributions

To address the above challenges, we propose FSpiNN, a novel optimization framework for memory- and energy-efficient spiking neural networks for both training and inference, that employs the following key techniques (see an overview in Fig. 3) to overcome the above-discussed research challenges.

1) **Optimization of the neuronal and STDP operations** by reducing (i) the inhibitory neurons through direct lateral inhibitory connections, (ii) the presynaptic spike-based weight updates, and (iii) the STDP complexity through elimination of the exponential calculation in the weight dependence part.

2) **An algorithm for improving the accuracy of STDP-based learning** by (i) minimizing the spurious weight updates through timestep-based operations, and (ii) effectively potentiating the weight in each update through an adaptive potentiation factor, and (iii) providing an effective competition among neurons through an adaptive inhibition.

3) **SNN quantization to compress the bit-width of network parameters:** It employs a fixed-point format by rounding to the nearest value, thereby providing a trade-off between the classification accuracy and the memory requirements.

4) **An algorithm to find the memory- and energy-aware SNN model:** It incorporates the memory and energy requirements in the optimization process, and employs a search algorithm to find the desired model.
II. Preliminaries

A. Spiking Neural Networks

Spiking Neural Networks (SNNs) are considered as the third generation of neural network computation models [25], since they exhibit high biological plausibility. They mimic the behavior of biological spiking networks, i.e., action potentials or spikes are used to convey information. The SNN computational model is composed of spike/neural coding, network architecture, neuron model, synaptic model, and learning rule [26].

Spike Coding: It converts the information into a sequence of spikes (spike train). Various spike coding methods have been studied in the literature, such as rate, temporal, rank-order, and phase coding schemes [27]–[30]. Here, we consider rate coding, since it has demonstrated high accuracy when employed in unsupervised learning-based SNNs. Rate coding converts the intensity of a pixel to a spike train. Typically, a higher intensity pixel is converted into a higher number of spikes than a lower intensity pixel.

SNN Architecture: It consists of spiking neurons and interconnecting synapses. Here, we consider the architecture in Fig. 1(a), since it has demonstrated robustness when performing different variants of STDP rules for unsupervised learning [9]. It consists of input, excitatory, and inhibitory layers. The input layer contains an input image, where every pixel is connected to all excitatory neurons. In this manner, each excitatory neuron has to recognize a class in the dataset, and the connecting synapses from the same neuron have to learn the features of the corresponding class. The excitatory neurons are connected to inhibitory neurons in a one-to-one connection. Each spike from an excitatory neuron triggers the corresponding inhibitory neuron to generate a spike that will be delivered to all excitatory neurons, except for the one from which the inhibitory neuron receives a connection. This inhibition provides competition among excitatory neurons. Here, a winner-takes-all (WTA) mechanism is employed.

Neuron Model: It represents the neuron dynamics and defines neuronal operations. Here, we consider the Leaky Integrate-and-Fire (LIF) neuron model presented in [9] since it has the lowest computational complexity compared to other biological plausible models [31], which is in-line with our objective. Note, LIF has also been widely adopted by the neuromorphic hardware community. The model describes the dynamics of membrane potential \( V \) as stated in Eq. 1

\[
\tau_v \frac{dV}{dt} = (E_{rest} - V) + g_e(E_{exc} - V) + g_i(E_{inh} - V)
\]  

(1)

Term \( \tau_v \) is the membrane time constant. \( E_{exc}, E_{inh} \) are the equilibrium potentials of the excitatory and inhibitory synapses, respectively. \( E_{rest} \) is the resting membrane potential. And, \( g_e, g_i \) are the conductances of the excitatory and inhibitory synapses, respectively. The membrane potential \( V \) is increased at the occurrence of the incoming spike, otherwise it decays exponentially. When the membrane potential reaches the threshold potential \( (V_{th}) \), it generates a spike and goes back to the reset potential \( (V_{reset}) \). Afterwards, the neuron is in the refractory period in which it cannot generate spike(s). Fig. 4 shows the illustration of the neuronal dynamics of LIF neuron model.

At the system level, we consider adding an adaptive thresholding mechanism to ensure that a neuron does not dominate the spiking activity, and to enable different neurons to recognize different input features, as has been demonstrated in [9]. Therefore, the membrane threshold is not determined by \( V_{th} \) only, rather by the sum of \( V_{th} + \theta \), where \( \theta \) is increased each time the neuron generates a spike, otherwise the membrane threshold decays exponentially.

![Fig. 4. Illustration of the neuronal dynamics of LIF model.](image)

Synaptic Model and Learning Rule: A synapse is modeled by the conductance change and synaptic weight \( w \), i.e., when a presynaptic spike arrives at a synapse, the conductance is increased by the synaptic weight \( w \), otherwise it decays exponentially. The synaptic weight \( w \) is defined by the spike-timing-dependent plasticity (STDP) learning rule, which will be discussed in Section II-B. The synaptic model is stated as Eq. 2

\[
\tau_g \frac{dg}{dt} = -g_e \text{ and } \tau_g \frac{dg}{dt} = -g_i
\]  

(2)

The term \( \tau_g \) denotes the time constant of an excitatory postsynaptic potential, and \( \tau_g \) denotes the time constant of an inhibitory postsynaptic potential.

B. Spike-Timing-Dependent Plasticity (STDP)

The synaptic weight change is dependent on the timing correlation between presynaptic and postsynaptic spikes, known as spike-timing-dependent plasticity (STDP) rule [32]. Although there are several variants of STDP [9], we consider the general STDP (i.e., pair-wise weight-dependent STDP) as the baseline, since it has been extensively used by previous works [9] [10] [14] [33]. It updates the synaptic weight every presynaptic and postsynaptic spike, based on its temporal correlation with the most recent postsynaptic and presynaptic spike, respectively. To improve the simulation speed, the weight changes in STDP are computed using synaptic traces [34]. Eq. 3 is the most common and general form of STDP operation used in literature.

\[
\Delta w = \begin{cases} 
-\eta_{pre}x_{post}w^\mu & \text{on presynaptic spike} \\
\eta_{post}x_{pre}(w_m - w)^\mu & \text{on postsynaptic spike}
\end{cases}
\]  

(3)

\( \Delta w \) is the synaptic weight change. \( \eta_{pre} \) and \( \eta_{post} \) are the learning rate for a presynaptic and postsynaptic spike, respectively. \( x_{pre} \) and \( x_{post} \) are the presynaptic and postsynaptic traces/history, respectively. \( w_m \) is the maximum
weight allowed, \( w \) is the previous weight value, and \( \mu \) is the weight dependence factor. Every time a presynaptic spike occurs, \( x_{\text{pre}} \) is set to 1, otherwise \( x_{\text{pre}} \) decays exponentially. Similar processing is done for the postsynaptic spike using \( x_{\text{post}} \) (see Fig. 5).

\[ \Delta w \]

**Requirement**

**Neuron model**

**(neuron-i)**

**Spike coding**

**Run the model**

**Postsynaptic spike train**

**Dataset**

**Optimized SNN model**

**Fixed-Point SNN Quantization**

**(Section III-C)**

1) **Optimize the processing of neuronal and STDP operations** (details in Section III-A):

- Reduce the number of neuronal operations by replacing the inhibitory layer with the direct lateral inhibitory connections. It removes the inhibitory neurons and substitutes the function of spikes from the inhibitory neurons with spikes from the excitatory neurons.
- Reduce the number of STDP-based synaptic weight updates by eliminating the presynaptic spike-based weight updates. The updates happen only when the postsynaptic spikes occur, which indicates that the synapses learn the input features effectively.
- Reduce the STDP complexity by fixing the weight dependence factor \( \mu \) to 1, hence eliminating the complex exponential calculation.

2) **Improve the accuracy of STDP-based learning** through the following means (details in Section III-B):

- Timestep-based synaptic weight updates aim to minimize the spurious weight updates that are induced by postsynaptic spikes, thereby ensuring that each update is essential.
- Adaptive STDP potentiation factor makes use of the number of postsynaptic spikes to ensure how strong the potentiation should be applied in each weight update. It compensates for the loss of accuracy induced by the STDP simplification.
- Adaptive inhibition strength aims to proportionally provide competition among the excitatory neurons by applying a proper inhibition strength to other neurons. It is derived from an experimental analysis that investigates the accuracy of different inhibition strength values.

3) **Fixed-Point SNN Quantization** (details in Section III-C) to further compress the bit-width of SNN parameters. It employs the rounding to the nearest value technique, and explores the trade-off between the accuracy and memory requirements for different quantization levels.

4) **A design space exploration algorithm to find the SNN model that fulfills the memory and energy budgets** (details in Section III-D). It integrates a search algorithm with the proposed optimization to obtain a model that offers a good trade-off in memory, energy, and accuracy.

**A. Optimizing the Computational Requirements of Neuronal and STDP Operations**

Reducing the number of neuronal operations: Our experiments in Fig. 7 illustrate that the number of postsynaptic spikes generated from excitatory neurons is less than the presynaptic spikes. Therefore, the number of incoming spikes required to trigger an inhibitory neuron to spike is less than the excitatory ones, and the inhibitory neuron typically has a smaller range of active membrane potential (between reset potential \( V_{\text{reset}} \) and threshold potential \( V_{\text{th}} \)) compared to the excitatory ones. This indicates that the inhibitory neurons have different parameters from excitatory ones to be saved in memory. Hence, a large number of neurons utilized in the inhibitory layer will consume a considerable amount of memory and energy. Moreover, each inhibitory neuron needs to process only a small number of incoming spikes to generate the inhibition spike. Therefore, the use of inhibitory neurons could be optimized further to reduce the memory and energy requirements.
Reducing the number of STDP-based synaptic weight updates: In the unsupervised SNNs, each neuron has to recognize features that belong to a specific class, so that each neuron can generate the highest number of spikes to represent its recognition category. To achieve this, the general STDP rule presented in Eq. 3 updates the synaptic weight in every event of a pre- and post-synaptic spike. However, previous work [11] observed that there are spurious weight updates which may decrease the accuracy of learning. The spurious updates are observed in two conditions: (i) when the neurons spike unpredictably in the early phase of learning, due to the random weight initialization, and (ii) when a neuron generates spikes for patterns that belong to different classes, but share common features, thereby causing the synapses to learn the overlapped features from different classes. Therefore, the STDP-based weight updates that are induced by these pre- and post-synaptic spikes might not learn the input features effectively, and hence decreasing the recognition capability of the neuron and consuming energy. We exploit this observation in a new way to optimize the SNN computations, while preserving the classification accuracy.

Proposed Optimization: We propose to eliminate the presynaptic spike-based weight updates to reduce the spurious weight updates that are induced by the presynaptic spikes. Therefore, the learning will focus on the condition when postsynaptic spikes happen, which indicates that the connecting synapses effectively learn the input features. It also reduces the computational energy as the number of presynaptic spikes is higher than the postsynaptic ones, as shown in Fig. 8.

Reducing the STDP Complexity: The change in each synaptic weight ($\Delta w$) is updated using an STDP operation that requires complex exponential calculations for the synaptic trace and weight dependence parts (see Eq. 3). We observed that the value of the weight dependence factor ($\mu$) is typically less than 1 [11], which makes it expensive to compute. Therefore, the use of weight dependence factor could be optimized to achieve further energy-efficiency.

Proposed Optimization: We propose to fix the weight dependence factor $\mu$ to 1, thereby simplifying the computation of STDP operations. However, we observed that only fixing the weight dependence factor value may degrade the classification accuracy across different sizes of the network, as shown in Fig. 9. Therefore, we propose a technique for improving the STDP-based learning (discussed in Section III-B) to compensate for the loss of this $\mu$ simplification, and to maintain the accuracy.
B. Improving the Accuracy of STDP-based Learning

We observed that for each input image, at least a single excitatory neuron is expected to recognize the input features and generate the highest number of spikes to represent the recognition of the corresponding class. Therefore, information regarding the number of postsynaptic spikes should be leveraged and used to improve the accuracy.

Proposed Solution: We propose an algorithm to improve the accuracy of STDP-based learning by employing timestep-based synaptic weight updates, and adaptively determining the STDP potentiation factor \( k \) and the inhibition strength. Timestep-based synaptic weight updates aim to reduce the spurious weight updates that are induced by the postsynaptic spikes. Therefore, our technique updates the weight once within a timestep, as long as at least there is a postsynaptic spike (see Fig. 10).

![Fig. 10. Overview of the timestep, synaptic weight updates, and number of accumulated postsynaptic spikes \((N_{\text{spikes}})\) in our proposed technique.](image)

We also propose an adaptive STDP potentiation factor \( k \), which aims at determining how strong the potentiation should be in each weight update, by leveraging the number of postsynaptic spikes. To do this, our technique accumulates the number of postsynaptic spikes observed from the first time when the spike trains of an input image are presented to the network, until the time when a weight update is performed (denoted as \( N_{\text{spikes}} \) in Fig. 10). The number of postsynaptic spikes is used to determine the potentiation factor \( k \), as formulated in Eq. 4. Term \( \max N_{\text{spikes}} \) denotes the maximum number of accumulated spikes, and \( N_{\text{spikes\_th}} \) denotes the number of threshold spikes, which normalizes the value of \( \max N_{\text{spikes}} \). Afterwards, the potentiation factor \( k \) is used to compute the synaptic weight change \( \Delta w \), as formulated in Eq. 5. The synaptic weight update is conducted for the excitatory neuron that generates the highest number of postsynaptic spikes (i.e., the winning neuron). In this manner, the confidence level of learning is expected to increase over time when presenting the spike trains of an input image.

\[
k = \left\lceil \frac{\max N_{\text{spikes}}}{N_{\text{spikes\_th}}} \right\rceil \quad (4)
\]

\[
\Delta w = k_\text{post} \times x_{\text{pre}} (w_m - w) \quad (5)
\]

Furthermore, balancing the strength of excitatory and inhibitory synaptic conductance is important as it makes the inhibition neither too strong, nor too weak. Too strong inhibition means that once the winning neuron is selected, it strongly prevents other excitatory neurons from firing, thereby dominating the recognition of input features (ineffective competition). Meanwhile, too weak inhibition means that it does not necessarily provide competition among the excitatory neurons, thereby giving no influence to the overall learning process (no competition). Previous work in [9] observed that the ratio between the excitatory and inhibitory strengths have an important role to balance the learning process. Towards this, we performed an experimental analysis to investigate the accuracy in different inhibition strength conditions and different datasets to justify the generality of the effective ratio conclusion. The results are presented in Fig. 11. Our analysis shows that when the inhibitory strength is too weak or too strong, the accuracy is sub-optimal. We observed that two comparable accuracy points are obtained using the ratio of 2x-4x. Therefore, we propose to use an adaptive inhibition strength that provides a proper competition among the excitatory neurons, by applying an inhibition strength equal to 2x-4x of the excitatory strength.

![Fig. 11. Impact of different ratio values between inhibitory and excitatory strengths when running the MNIST and Fashion MNIST datasets. When the ratio is too weak or too strong, the accuracy is sub-optimal.](image)
Algorithm 1 Pseudo-code for improving the accuracy of STDP-based learning

**INPUT:** (1) Number of training dataset ($D_{train}$);
(2) Simulation time for an input image ($t_{sim} = 350$);
(3) Timestep ($t_{step} = 4$);
(4) SNN parameters: number of excitatory neurons ($n_{exc}$), number of synapses-per-neuron ($n_{syn}$), number of accumulated postsynaptic spikes ($N_{spikes}$);
(5) STDP parameters: learning rate ($\eta_{post} = 0.01$), max. weight value ($w_{max} = 1$), previous weight value ($w$), number of threshold spikes ($N_{spikes} = 10$), potentiation factor ($k$);
(6) Postsynaptic spike event ($\text{spike}_\text{post}$);

**OUTPUT:** Synaptic weight update ($\Delta w$);

**BEGIN**

**Initialization:**
1. $\Delta w[n_{exc}, n_{syn}] = \text{zeros}[n_{exc}, n_{syn}]$;
2. $N_{spikes}[n_{exc}] = \text{zeros}[n_{exc}]$;
3. $x_{pre} = \text{zeros}[n_{exc}, n_{syn}]$;

**Process:**
4. for ($d = 0$ to ($D_{train} - 1$)) do
5. for ($t = 0$ to ($t_{sim} - 1$)) do
6. for ($i = 0$ to ($n_{exc} - 1$)) do
7. if $\text{spike}_\text{post}$ then
8. $N_{spikes}[i] += 1$;
9. monitor $x_{pre}[i, :]$;
10. end if
11. end for
12. if (($t \mod t_{step}) == 0$) then
13. $\text{max}N_{spikes} = \text{max}(N_{spikes})$;
14. $j \leftarrow \text{index} (\text{max}(N_{spikes}))$;
15. $k = \lceil (\text{max}N_{spikes}/N_{spikes}, \text{th}) \rceil$;
16. $\Delta w[j, :] = k\eta_{post}x_{pre}[j, :](w_{max} - w)$;
17. end if
18. end for
19. end for
20. return $\Delta w$;

**END**

SNN parameters (i.e., synaptic weights) to the accuracy, using a rounding to the nearest value technique with the rounding half-up rule. It approximates the values that are half-way between two representable numbers by rounding them up. The fixed-point number can be written in $(Q_i, Q_f)$ format, with $Q_i$ and $Q_f$ are the integer and fractional part, respectively. The total number of bits (wordlength $N$) in the fixed-point format consists of the number of bits for the integer part $N_i$ and the fractional part $N_f$ (i.e., $N = N_i + N_f$). The precision of the fixed-point format $\epsilon$ is defined as $\epsilon = 2^{-N_f}$ and it is used to define the quantized number $x_q$.

$$x_q = \left[ x + \frac{\epsilon}{2} \right] \tag{6}$$

D. Design Space Exploration (DSE) Algorithm for the Memory- and Energy-Aware SNN Model

To provide better applicability in many application scenarios, the proposed optimizations need to fulfill the given memory and energy requirements. Towards this, we also propose a DSE algorithm to find an SNN model whose memory and energy (for both the training and inference) are within the given memory and energy budgets, while maintaining the accuracy. The main idea is to incrementally increase the size of SNN model (i.e., number of excitatory neurons) and evaluate whether the currently investigated model satisfies the memory and energy budgets. If so, the DSE will evaluate whether the accuracy is better. If the accuracy is the same, the DSE will select the smaller model to keep the memory and energy consumption low. In this manner, our FSpiNN framework can support many applications where the memory and energy are constrained. The pseudo-code of the algorithm is presented in Algorithm 2.

Algorithm 2 Pseudo-code for the DSE algorithm

**INPUT:** (1) Memory requirement ($\text{mem}$);
(2) Energy requirement for training ($E_{train}$);
(3) Energy requirement for inference ($E_{inf}$);
(4) SNN model ($\text{model}$): number of the excitatory neurons ($\text{model.n}_{exc}$), model size ($\text{model.mem}$), energy of model for training ($\text{model.E}_{train}$), energy of model for inference ($\text{model.E}_{inf}$), accuracy of model ($\text{model.acc}$);
(5) Number of additional excitatory neurons ($n_{add}$);

**OUTPUT:** SNN model ($\text{model}$);

**BEGIN**

**Initialization:**
1. $\text{model.n}_{exc} = 0$;
2. $\text{model.size} = 0$;
3. $\text{acc\_saved} = 0$;

**Process:**
4. while $\text{model.size} \leq \text{mem\_req}$ do
5. if ($\text{model.n}_{exc} > 0$) then
6. perform training using Algorithm 1;
7. monitor $\text{model.E}_{train}$;
8. if ($\text{model.E}_{train} \leq E_{train}$) then
9. perform inference;
10. monitor $\text{model.E}_{inf}$ and $\text{model.acc}$;
11. if ($\text{model.E}_{inf} \leq E_{inf}$) and (model.acc > $\text{acc\_saved}$) then
12. $\text{acc\_saved} = \text{model.acc}$;
13. save model;
14. end if
15. end if
16. end if
17. $\text{model.n}_{exc} += n_{add}$;
18. end while
19. return $\text{model}$;

**END**

IV. Evaluation Methodology

Fig. 12 illustrates the experimental setup with different steps, to evaluate our proposed framework. We used a Python-based SNN simulator [35] for evaluating the accuracy of the SNN. We run the SNN simulations on three different types of GPUs, namely Nvidia GeForce GTX 1060 [36], GTX 1080 Ti [37], and RTX 2080 Ti [38] (the detailed
Specifications of the evaluated networks.

| Specification       | Net100  | Net400  | Net900  | Net1600 | Net2500 | Net3600 | Net4900 |
|---------------------|---------|---------|---------|---------|---------|---------|---------|
| Architecture        | Pascal  | Pascal  | Pascal  | Pascal  | Pascal  | Pascal  | Pascal  |
| Cuda Cores          | 1280    | 3584    | 4352    | 4352    | 4352    | 4352    | 4352    |
| Memory              | 6GB GDDR5 | 11GB GDDR5 | 11GB GDDR6 | 11GB GDDR6 | 11GB GDDR6 | 11GB GDDR6 | 11GB GDDR6 |
| Interface Width     | 192-bit | 352-bit | 352-bit | 352-bit | 352-bit | 352-bit | 352-bit |
| Bandwidth           | 8Gbps   | 11Gbps  | 14 Gbps | 14 Gbps | 14 Gbps | 14 Gbps | 14 Gbps |
| Power               | 120W    | 250W    | 250W    | 250W    | 250W    | 250W    | 250W    |

Datasets: We used the MNIST [16] and Fashion MNIST [41] datasets, as they are widely used for evaluating the accuracy of SNNs [2]. MNIST represents a simple dataset, while Fashion MNIST represents a more complex dataset [15]. Each dataset has 60,000 images for training and 10,000 images for test, each having a dimension of 28x28 pixels.

Input Encoding: Every pixel of an image from the dataset is converted into a Poisson-distributed spike train whose firing rate is proportional to the intensity of the pixel. A higher intensity pixel is converted into a higher number of spikes than a lower intensity pixel. The spike train from each pixel is presented to the network for 350 ms duration.

Classification: In the training, the synaptic weight updates are performed without label information as it is unsupervised learning. Therefore, an additional mechanism is required to categorize the excitatory neurons for classification. The neurons are categorized based on their highest response to different classes over one presentation of the training set (1x epoch of training). Here, the labels are used to assign each neuron with a specific class. Afterwards, the response of the class-assigned neurons is used to measure the accuracy.

Comparisons: We compared our proposed framework with two state-of-the-art designs, i.e., the general pair-wise weight dependence STDP-based SNN (baseline) [9], and the enhanced self-learning STDP-based SNN (SL-STDP) [11]. The sizes of networks considered in the evaluation are the networks with a different number of excitatory neurons: 100, 400, 900, 1600, 2500, 3600, and 4900. For conciseness, we refer them to as Net100, Net400, Net900, Net1600, Net2500, Net3600, and Net4900, respectively. To provide fair comparisons, we recreated the baseline [9] and the SL-STDP [11], and then simulated them using the same SNN simulator [35]. We also used the same approach for obtaining the memory footprint and the energy. That is, we extracted the size of SNN model from simulation to evaluate the memory footprint, and we used the nvidia-smi utility to report the power and recorded the simulation time, which are then used to estimate the energy.

We also kept the hyper-parameter values the same for different sizes of networks. In particular, we used 1x epoch of training because the network will be trained with a full training set once. Moreover, an SNN model trained with 1x epoch of training is adopted by a wide-range of SNN community and considered as a completely trained network [10] [11] [13] [33].

V. Results and Discussions

A. Maintaining the Classification Accuracy

Results for the MNIST Dataset: Fig. 13(a) shows the accuracy after 1x epoch of training for MNIST. It shows that our FSpinn maintains (and even improves in certain cases) the accuracy across different sizes of networks as compared to other designs. Following are the detailed accuracy improvements achieved by FSpinn:

- Label-1: In Net100, FSpinn achieves 13.2% improvement with 89.2% accuracy.
- Label-2: In Net400, FSpinn achieves 7.3% improvement with 95.6% accuracy.
- Label-3: In Net900, FSpinn achieves 2.4% improvement with 94.4% accuracy.
- Label-4: In Net1600, FSpinn achieves 2.2% improvement with 95.4% accuracy.
- Label-5: In Net2500, FSpinn achieves 0.8% improvement with 90% accuracy.
- Label-6: In Net3600, FSpinn achieves 4.8% improvement with 92.8% accuracy.
- Label-7: In Net4900, FSpinn achieves 2.4% improvement with 92.4% accuracy.

These results indicate that a larger network is harder to train. For instance, the accuracy achieved in Net100 and Net900 are 89.2% and 94.4% respectively, but the accuracy improvements in Net100 and Net900 are 13.2% and 2.4% respectively. The reason is that, a larger network has more synapses to train for effectively learning the input features, thereby requiring more careful training (e.g., hyper-parameter tuning). This condition may cause the accuracy of the larger
networks lower than the smaller ones in certain cases. For instance, the accuracy achieved in Net4900 is 92.4%, which is lower than the accuracy in Net900 (i.e., 94.4%). Furthermore, Fig. 13(b) shows the synaptic weights and its classification matrix, and Fig. 13(c) shows the confusion matrix for Net400. These results show the common confusions, such as when identifying between digits 3 and 8, 4 and 9, etc. The reason is that, the connecting synapses from the same neuron learn the common features (shape) from these classes. Hence, the same neuron generates the highest number of spikes for different classes, thereby resulting in more frequent false classifications.

**Results for the Fashion MNIST Dataset:** Fig. 14(a) shows the accuracy after 1x epoch of training for Fashion MNIST. It shows that our FSpiNN still maintains (and even improves in certain cases) the accuracy across different sizes of networks as compared to other designs. Following are the detailed accuracy improvements achieved by FSpiNN:

- **Label-1:** In Net100, FSpiNN achieves 14.2% improvement with 60.2% accuracy.
- **Label-2:** In Net400, FSpiNN achieves 5.2% improvement with 64.8% accuracy.
- **Label-3:** In Net900, FSpiNN achieves 3.6% improvement with 66% accuracy.
- **Label-4:** In Net1600, FSpiNN achieves 3.5% improvement with 68.8% accuracy.
- **Label-5:** In Net2500, FSpiNN achieves 3% improvement with 60.6% accuracy.
- **Label-6:** In Net3600, FSpiNN achieves 27% improvement with 64.4% accuracy.
- **Label-7:** In Net4900, FSpiNN achieves 11% improvement with 61.6% accuracy.

Here, we observed the same trend as observed in MNIST. A larger network has the potential to achieve higher accuracy because more neurons are available for recognizing more feature variations. This trend is shown in Fig. 14(a) for Net100-Net1600 and Net3600-Net4900. At the same time, a larger network is harder to train because more synapses have to effectively learn input features. Therefore, a larger network may achieve lower accuracy than the smaller ones in cases where the synapses are not effectively trained. This trend is shown in Fig. 14(a) for Net1600-Net3600. The reason is that, in our experiments, we kept the same hyper-parameter tuning across different sizes of networks, and only performed 1x epoch of training. Therefore, the accuracy of a larger network could still be improved through more effective hyper-parameter tuning (e.g., more training
epochs), as suggested from Fig. 15. The results in Fig. 15 indicate that employing multi-epoch training can increase the accuracy, since the same features in the training set are learned multiple times by the network. The accuracy improvement in the earlier epoch is typically higher than in the later ones, thereby only relying on multi-epoch training may incur high energy consumption, without gaining significant accuracy improvement in the end. To address this, our FSpiNN employs the adaptive potentiation factor and inhibition strength, which increase the confidence of learning over time in the training. The results also show that our FSpiNN achieves the highest accuracy across different epochs as compared to state-of-the-art designs. Moreover, FSpiNN with 1x training epoch achieves higher accuracy than state-of-the-art designs with 3x training epochs. These results show the effectiveness of the learning algorithm in FSpiNN.

![Accuracy vs. quantization for MNIST dataset for Net400.](image)

**Fig. 16.** Accuracy vs. quantization for MNIST dataset for Net400.

**Results for the Fashion MNIST Dataset:** Label-1 in Fig. 17 shows that FSpiNN achieves better accuracy than the baseline and the SL-STDP, when the minimum bit-width of quantization is 8 bits. The reason is that, the 8-bit (or more) format in the FSpiNN provides sufficient levels of weight values to modulate the input spikes from MNIST images, and induce each neuron to recognize a specific digit class. In 8-bit precision, our FSpiNN achieves 91.6% accuracy, while the baseline and the SL-STDP achieve 87.6% and 82%, respectively. It indicates that the accuracy achieved by the FSpiNN 8-bit is slightly less than the FSpiNN FP32 (pointed by the label-2), but still higher than the baseline and the SL-STDP with FP32 precision (pointed by the label-3 and label-4, respectively). Therefore, the FSpiNN 8-bit offers no accuracy loss with a reduced bit-width for MNIST.

![Accuracy vs. quantization for Fashion MNIST dataset for Net400.](image)

**Fig. 17.** Accuracy vs. quantization for Fashion MNIST dataset for Net400.

These experimental results also show that, for both MNIST and Fashion MNIST datasets, the quantization levels with less than 8-bit precision do not provide sufficient unique information for distinguishing features of different classes in the input images. This condition reduces the efficacy of STDP learning of the synapses and recognition capability of the neurons, thereby leading to low classification accuracy. Furthermore, a reduced bit-width is beneficial since it leads to a reduced memory requirement and energy consumption.
which will be discussed in Section V-C and Section V-D. Note, the users can select the quantization level based on the trade-off consideration in the design specifications (e.g., accuracy, memory, and power/energy budget).

C. Reducing the Memory Requirements

Fig. [18] shows the memory requirements of different designs across different sizes of networks for both the training and inference phases. Label-1 shows that the Net3600 and Net4900 that employ the baseline or the SL-STDP techniques, consume more than 100MB, thereby making them difficult to be deployed on embedded systems. On the other hand, our FSpiNN without quantization (FP32) achieves 1.8x and 1.9x memory savings as compared to the baseline, for Net3600 and Net4900, respectively. The reason is that the FSpiNN FP32 removes the inhibitory neurons completely, thereby avoiding their parameters to be saved in the memory. After applying quantization, the memory requirement is reduced even more. The FSpiNN 16-bit achieves about 3.6x and 3.7x memory savings, while the FSpiNN 8-bit achieves about 7.3x and 7.5x memory savings, when compared to the baseline for Net3600 and Net4900, respectively. Fig. [18] also shows that the FSpiNN 8-bit consumes about 0.16MB-28MB for Net100-Net4900, thereby making the networks easier to be deployed on embedded systems. Furthermore, if we consider the accuracy that the quantized designs can achieve, we can select the FSpiNN design that offers a good trade-off between high accuracy and acceptable memory footprint.

![Memory Footprint Graph](image)

Fig. 18. Memory requirements for different sizes of networks (i.e., Net100, Net400, Net900, Net1600, Net2500, Net3600, and Net4900) and different quantization levels (i.e., FP32/without quantization, 16-bit, and 8-bit).

D. Energy-Efficiency Improvements

Fig. [19] and Fig. [20] illustrate the energy-efficiency across different sizes of networks and different GPUs for MNIST and Fashion MNIST datasets, respectively. These figures show that the SL-STDP achieves higher energy-efficiency than the baseline in training phase, and our FSpiNN achieves the highest energy-efficiency among all designs in both training and inference phases.

**Training:** The SL-STDP improves the energy-efficiency by 1.1x-1.2x compared to the baseline, across different sizes of networks and GPUs, for both MNIST and Fashion MNIST. The reason is that, the SL-STDP and the baseline have similar computational complexity in the inference phase. Meanwhile, the FSpiNN FP32 improves the energy-efficiency by 1.3x-1.9x (MNIST) and by 1.1x-1.4x (Fashion MNIST) compared to the baseline. The improvements mainly come from the elimination of the inhibitory neurons. After applying quantization, the FSpiNN 16-bit and FSpiNN 8-bit improve the energy-efficiency even more than FSpiNN FP32. That is, the FSpiNN 16-bit achieves 1.4x-2.6x (MNIST) and 1.2x-2.1x (Fashion MNIST), while FSpiNN 8-bit achieves 1.4x-2.9x (MNIST) and 1.3x-2.3x (Fashion MNIST), compared to the baseline.

Furthermore, if we consider the classification accuracy and memory footprint that the quantized designs can achieve, we can select the FSpiNN design that offers a good trade-off in the accuracy, memory, and energy-efficiency. For instance, the FSpiNN 8-bit achieves energy-efficiency improvements by 4.3x (MNIST) and by 2.7x (Fashion MNIST) in training (see labels-1 in Fig. [19] and Fig. [20]), and by 2x (MNIST) and by 1.6x (Fashion MNIST) in inference (see labels-2 in Fig. [19] and Fig. [20]), compared to the baseline in Net4900, while obtaining 7.5x memory saving with an accuracy of ~92% for MNIST and ~61% for Fashion MNIST. The experimental results in Fig. [19] and Fig. [20] also suggest that our FSpiNN framework is scalable for different sizes of networks and can be used for other systems where different types of GPUs are deployed, such as embedded systems with embedded GPUs.

Note that this work is not about justifying SNNs over deep neural networks (DNNs). Rather, we consider what necessary optimizations are required if the SNNs make it to a real-world system following an increasing trend of the neuromorphic computing, due to their benefits in energy-efficient spike-based computations and unsupervised learning. Moreover, there is a substantial difference in the underlying learning mechanism between the SNNs (with the unsupervised learning) and the DNNs (with the supervised learning), thus we cannot directly compare the accuracy of the unsupervised SNNs with the supervised DNNs. Previous work [42] has observed that the accuracy of the DNNs (with the supervised back-propagation algorithm) is generally higher than the SNNs (with the unsupervised STDP algorithm), because the unsupervised STDP algorithm does not have labels when updating the weights, hence it is less effective than the supervised ones. Furthermore, in the SNN community, many different optimization aspects are explored, and they have the potential to be incorporated into our FSpiNN framework. For instance, the works in [43] and [44] focus on generating...
precise spike sequences like the real-world observation. They target a different optimization purpose compared to the one targeted by our FSpiNN framework. However, they can still be incorporated in the FSpiNNs’ optimization flow for generating precise spike sequences. This illustrates the flexibility of our FSpiNN for integration with other optimization techniques.

VI. CONCLUSION

In this paper, we proposed a novel FSpiNN framework that synergistically employs different techniques to reduce the memory footprint and to improve the energy-efficiency of SNNs, while maintaining their accuracy. Experimental results illustrate the benefits and efficiency of the proposed framework, compared to the state-of-the-art designs, across different sizes of networks and different datasets (MNIST and Fashion MNIST). For instance, in a network with 4900 excitatory neurons, our FSpiNN achieves 7.5x memory saving and 3.5x energy-efficiency improvement on average for training and by 1.8x on average for inference, with no accuracy loss. In short, our proposed framework enables efficient embedded SNN implementations for the next-generation smart embedded systems.

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