ABSTRACT: We have developed a novel detector concept based on Modified Internal Gate Field Effect Transistor (MIGFET) wherein a buried Modified Internal Gate (MIG) is implanted underneath a channel of a FET. In between the MIG and the channel of the FET there is a depleted semiconductor material forming a potential barrier between charges in the channel and similar type signal charges located in the MIG. The signal charges in the MIG have a measurable effect on the conductance of the channel. In this paper a double MIGFET pixel is investigated comprising two MIGFETs. By transferring the signal charges between the two MIGs Non-Destructive Correlated Double Sampling Readout (NDCDSR) is enabled.

The proposed MIG radiation detector suits particularly well for low-light-level imaging, X-ray spectroscopy, as well as synchrotron and X-ray Free Electron Laser (XFEL) facilities. The reason for the excellent X-ray detection performance stems from the fact that interface related issues can be considerably mitigated since interface generated dark noise can be completely avoided and interface generated $1/f$ and Random Telegraph Signal (RTS) noise can be considerably reduced due to a deep buried channel readout configuration.

Electrical parameters of the double MIGFET pixel have been evaluated by 3D TCAD simulation study. Simulation results show the absence of interface generated dark noise, significantly reduced interface generated $1/f$ and RTS noise, well performing NDCDSR operation, and blooming.
protection due to an inherent vertical anti-blooming structure. In addition, the backside illuminated thick fully depleted pixel design provides a homogeneous radiation entry window, low crosstalk due to lack of diffusion, and good quantum efficiency for low energy X-rays and NIR light.

These facts result in excellent Signal-to-Noise Ratio (SNR) and very low crosstalk enabling thus excellent X-ray energy and spatial resolution. The simulation demonstrates the charge to current conversion gain for source current readout to be 1.4 nA/e.

**KEYWORDS:** X-ray detectors; Photon detectors for UV, visible and IR photons (solid-state) (PIN diodes, APDs, Si-PMTs, G-APDs, CCDs, EBCCDs, EMCCDs etc); Radiation-hard detectors; Detector modelling and simulations II (electric fields, charge transport, multiplication and induction, pulse formation, electron emission, etc)
1 Introduction

It is generally known that Gamma rays, X-rays, and electrons with energies below the minimum threshold for bulk defects (∼ 300 keV) generate only defects in the dielectrics, at the dielectric silicon interface, and the interface between dielectrics [1]. The build-up of the interface damage increases dark current generation from depleted interfaces. If the interface-generated dark current can mix with the signal charges the build-up of the interface damage will increase the dark noise and thereby reduce the Signal to Noise Ratio (SNR) as well as the useful lifetime of the detector and particularly so in X-ray (and/or electron) detection applications or imaging applications utilized in radioactive environments. The radiation-induced interface damage also affects the read noise in surface channel or shallow buried channel devices since it increases the amount of interface defects and thereby interface generated 1/f and RTS noise.

Besides having low dark and read noise it is important for X-ray detectors and for silicon Near Infra-Red (NIR) optimised image sensors to have a thick fully depleted Back-Side Illuminated (BSI) design. The full depletion is important in order to insure that no charge is lost due to recombination and in order to minimize crosstalk by preventing diffusion. BSI is required in order to provide a thin homogeneous radiation entry window, which enables 100% fill factor and the detection of very low energy X-ray photons. A thick detector, on the other hand, improves the Quantum Efficiency (QE) for NIR light and higher energy X-rays (important e.g. in X-ray fluorescence spectroscopy).

There are currently a number of pixelated detector architectures, which are described in more detail below. None of them offer, however, the combination of very low noise, low crosstalk, high QE for NIR light and X-rays, as well as durability against radiation damage. The reason for this is that a thick fully depleted BSI detector having very low read noise and being free of interface generated dark noise has not been realised so far. There are fully depleted backside illuminated Charge Coupled Devices (CCDs) utilising a regular gate architecture [2, 3] and CCDs [4] utilising a pn gate architecture (the original pn gate CCD architecture was introduced in [5]) enabling relatively
low read noise. In thick fully depleted BSI CCDs interline transfer architecture is not feasible and thus the only options are full frame and frame transfer architectures. In case reasonable frame rate (e.g. video rate) is desired then the frame transfer architecture is the only option. The problem with frame transfer architecture is that it suffers from smear [6] even though it is less prone to it than full frame architecture. The problem at least with [2, 3] is also that it suffers from interface generated dark noise during the charge transfer period.

Thick fully depleted BSI pixels can be realised also with simple pin (p type, intrinsic, n type) pixels wherein an n⁺ collection node is connected either to a hybridized readout chip or to pixel specific integrated readout circuitry. Both of them are typically realized with a three transistor (3T) Complementary Metal Oxide Semiconductor (CMOS) pixel architecture but the 3T pixel architecture suffers from interface generated dark noise and high read noise [7, 8]. The pinned photo-diode structure [7, 9] utilised in 4T CMOS pixels enables BSI configuration as well as more or less complete removal of the interface generated dark noise [7, 8]. Thick fully depleted 4T pixels are, however, notoriously difficult to realise — the authors are not aware of any being realised so far.

Another problem in CCDs and CMOS image sensor technologies is that they utilise a readout configuration which is hereby referred to as External Gate Readout Configuration (EGRC) since the signal charge is brought to a MOS gate of a readout transistor, i.e., the gate is not located inside the semiconductor substrate but on top of it. A formidable problem in EGRC is that in Correlated Double Sampling (CDS) readout procedure (which is a mandatory requirement for accurate measurements) the signal charge is destroyed when it is brought to the external gate. This means that the signal charge can be readout accurately only once and thus one cannot mitigate the read noise by performing multiple readouts. It is important to note that the read noise can be removed by signal amplification but on the other hand the amplification process itself increases considerably the noise manifested by excess noise factor [7, 10].

A disadvantage of EGRC is also that the effect of 1/f and RTS noise on the read noise and thus on SNR is difficult to mitigate. By far the major part of the 1/f and RTS noise stems from the interface and thus by utilizing a buried channel readout transistor [11] the 1/f and RTS noise can be reduced — the deeper the channel the smaller the 1/f and RTS noise. However, the deeper the buried channel in EGRC the smaller the signal and the available voltage swing. Another problem is also that in EGRC the spurious signal due to a charge trapped at the semiconductor interface beneath the gate is always larger than the signal produced by a signal charge on the sense node and the deeper the buried channel the larger this difference is. A third reason is that the smaller the amount of signal charges the shallower the buried channel is, meaning that the smaller the signal the more there will be 1/f and RTS noise. This effect results in also non-linearity issues. These reasons reduce the beneficial effect of a deep buried channel on SNR in EGRC. One could also remove the interface generated 1/f and RTS noise in EGRC by utilising a JFET type diffusion gate instead of the MOS gate but this reduces considerably the available voltage swing and signal size as well as increases the depleted interface area next to doping belonging to the sense node. The latter fact increases the dark current generation rate at the sense node necessitating faster readout.

It is possible to reduce the read noise without introducing additional noise through NDCDSR, i.e., through accurate non-destructive signal readout. The NDCDSR has been demonstrated in an Internal Gate Readout Configuration (IGRC) [12] (the initial IG readout architecture was introduced in [13]). The problem is, however, the very large and unpractical pixel size as well as
manufacturability issues. The latter fact stems from the fact that in IGRC signal charges modulate an oppositely charged current running in the transistor channel, which is next briefly explained. Let us assume that there is a fully depleted n doped Internal Gate (IG) collecting signal charges beneath a hole surface channel that is closed for the time being. Next let us assume that the n doping of the IG is larger at a certain location which means that at this location there are more positively charged dopant atoms beneath the channel increasing the potential at the IG and at the interface above, i.e. the IG at this location will be more attractive for signal electrons but it will be more difficult to open the hole channel at this location than at other locations. This means that it is very difficult to match the location of the minimum channel threshold of the readout transistor with the signal charge potential minimum leading to poor tolerance against process fluctuations.

In the IGRC of \cite{12, 14} a surface channel readout transistor is utilized resulting in a lot of $1/f$ and RTS noise \cite{11}. The high $1/f$ and RTS noise means that a considerable amount of NDCDS measurements need to be performed in order to reduce the $1/f$ and RTS noise to a negligible level. The problem is that generally in IGRC a circular readout transistor is more or less mandatory in order to improve the manufacturability but the circular readout transistor inhibits the use of a deep buried channel. One could also reduce $1/f$ and RTS noise by utilizing a circular JFET in conjunction with the IGRC, but it would have a negative impact on the manufacturability.

As it will be shown in this work thick fully depleted BSI deep buried channel double MIG image sensors have several benefits: they offer NDCDSR, interface generated dark noise and image lag free operation, very low $1/f$ and RTS noise, 100% fill factor, excellent QE for low energy X-rays up to several keV as well as for NIR and visible light, very low crosstalk, inherent vertical anti-blooming mechanism, very fast operation, as well as good manufacturability with existing CMOS manufacturing lines.

The good manufacturability stems from the fact that the current running in the channel of the readout transistor is composed of similar charges to the signal charges situated in the MIG modulating the current of the readout transistor. This arrangement is realized by placing a potential barrier formed of fully depleted semiconductor material in between the channel and the MIG. The advantage is that the location of lowest potential energy for signal charges in MIG is well aligned with the location of lowest channel threshold.

The potential barrier between the channel and the MIG prevents also the mixing of signal charges with interface-generated charges meaning that a MIG sensor does not suffer from interface generated dark noise. Similarly this potential barrier separates also the signal charges from the interface during signal charge transfer (transfer is required in NDCDSR). Thus the MIG image sensor is not prone to image lag. The potential barrier enables vertical anti-blooming, i.e., when the MIG starts to be full of signal charges then the excess charges will flow over the potential barrier preventing the signal charges from spreading into neighbouring pixels.

The low $1/f$ and RTS noise is due to the fact that a deep buried channel can be utilized in a MIG sensor since non-circular readout transistor design is enabled. Besides the deeper the buried channel the bigger the signal is, and secondly, the smaller the signal the smaller the $1/f$ and RTS noise is. The latter fact is because the less there is charge in the MIG the deeper the buried channel is.

As already previously explained the good QE for NIR light and low energy X-rays up to several keV, the 100% fill-factor, and low crosstalk are due to the thick fully depleted BSI design.
Another reason for the low crosstalk is the fact that current mode readout (i.e. readout of source or drain current) is enabled meaning that capacitive coupling between pixels is minimised since during readout all the nodes of the pixel and all the lines connecting the pixel are held at constant designated potentials. Since only current signal and no potential signal is attached to the readout line (source or drain line) there is no capacitive coupling between the readout lines. In case source current in the source line and the drain current in the drain line are proceeding into opposite direction and the source and drain lines are located close to each other (e.g. on top of each other) there will be neither inductive coupling to the source and drain lines of neighbouring pixel columns. In voltage mode readout (typically Source Follower (SF) readout [7]) the voltage along read lines (in the SF readout the readout line is the source line which is connected to a constant current source and the readout is performed by reading out the potential on the source line) couples to the sense nodes (in SF configuration the sense node comprises the floating diffusion, the gate of the source follower transistor, and the source of a reset transistor) of other pixels that are readout simultaneously. The reason why very fast readout is enabled stems from the fact that in current mode readout operation the readout lines are at constant potential. In voltage mode readout, on the other hand, the potential on the read lines is continuously altered and the capacitive charging of the read line takes time, which slows the readout process.

The NDCDSR enables very low read noise and it stems from the fact that the read noise is small (due to very low level of interface generated 1/f and RTS noise) and because it is further possible to average out the overall read noise by performing multiple CDS measurements meaning that the MIG sensors offer very good energy resolution for very low energy X-rays originating e.g. from Lithium. The facts that the MIG sensors do not suffer from interface problems (no interface generated dark noise, very low level of interface generated 1/f and RTS noise, no image lag) means that MIG sensors are inherently tolerant to X-rays and electrons having energies below 300 keV. The lack of interface problems has also the additional benefit that it should enable very low noise detectors to be made from semiconductor materials (e.g. Germanium) having much worse interface quality than silicon, which is often not possible with other detector technologies since they suffer from interface issues.

2 Double modified internal gate field effect transistor detector

In the thick fully depleted BSI deep buried channel double MIGFET pixel the signal charge can be transferred back and forth between the two MIGs of the pixel. Both MIGFETs have a buried internal gate (MIG) implanted directly underneath their conducting channels. As can be seen from the cross-section on figure 1(b), Source 1 (S1), Gate 1 (Gate1), Drain 1 (D1) and MIG1 belong to the first MIGFET and Source 2 (S2), Gate 2 (Gate2), Drain 2 (D2) and MIG2 belong to the second MIGFET. Between these two MIGFETs there is a Transfer Gate enabling transfer of the stored signal charge between the two MIGs, which is necessary for the NDCDSR. One or preferably both nodes S1 and S2 are connected on separate vertical lines, which are connected to separate CDS readout circuits. The D1 and D2 can be both connected to the same vertical line or to a node, which is common to the whole pixel matrix. The Gate1, Gate2, and Transfer Gate nodes are connected to separate horizontal lines. The top view of the pixel is presented in figure 1(a).
Figure 1. (a) Front side view of the Double MIGFET Detector wherein the four small transistors are optional selection transistors which can be utilised e.g. in order to create pixel specific reset. (b) Cross-section of the Double MIGFET Detector.

The pixel comprises a 50 \( \mu \text{m} \) thick fully depleted n\(^-\)type BSI silicon substrate and has dimensions of 8 by 8 \( \mu \text{m}^2 \). The front side of the device is manufactured utilizing a 0.18 \( \mu \text{m} \) or smaller minimum line width 5 V CMOS process. The only change that is required to the CMOS process is to adjust it to the lower substrate doping of high resistivity wafers (preferably 200 mm float zone wafers). The thinning of the wafer can be performed with TAIKO (a wafer back grinding process that uses a grinding method developed by DISCO) process [15] after which backside implantation, laser annealing, and chip sawing may be performed.

The upper part of the pixel (i.e. front side) comprises a stack of n-type buried channel and MIG layers in between of which there is a p-type barrier layer. It also has a Shallow Trench Isolation (STI) and a p-well surrounding the pixel. The p-well effectively reduces the crosstalk and prevents blooming. Besides, one can place n-type selection transistors into the p-well in order e.g. to enable pixel specific reset. There are additional n-type implants in the MIG layer beneath Gate1 and Gate2 referred to as MIG1 and MIG2 and used for the storing of signal electrons. In this design the p \(^+\) backside layer is held always at \(-7\) V, the D1 & D2 always at \(+5\) V, the S1 & S2 always at \(+4.5\) V, and the p\(^+\) backside layer at \(-7\) V. The operational range of the Gate1, Gate2, and Transfer Gate is from 0 V to \(+5\) V.

3 Full 3D TCAD simulation study

The performance of the pixel has been studied by simulating operational steps. The 3D simulation results are obtained with the (Synopsys) TCAD software tool [16–18]. The first step is reset of the
Figure 2. (a) Electrostatic potential distribution during reset on a 2D cross-section of a 3D simulation of the pixel structure. The potential curves on vertical cut lines A, B, and C are depicted on figure 3. (b) Electron density distribution during reset on a 2D cross-section of the 3D simulated pixel. There is no charge left in the MIGs.

pixel, when all the charge present in the pixel is removed. The second step is integration, when charge accumulates in the MIGs. The third step is the non-destructive CDS procedure comprising non-destructive charge transfer from one MIG to another in between non-destructive readouts. In this paper we present simulation results for the pixel at $-40^\circ$C.

3.1 Reset

At first, the pixel reset operation is performed in order to remove any charge form the MIGs. The charge is removed into the nodes D1 and D2 by applying a reset potential configuration wherein the transfer gate is at $+4\,\text{V}$ ($+4.5\,\text{V}$ or $+5\,\text{V}$ could be equally well used) and nodes Gate1 and Gate2 are at $0\,\text{V}$. A two dimensional (2D) cross-section of the electrostatic potential distribution of the three dimensional (3D) simulation of the pixel in the reset potential configuration is shown in figure 2(a). Figure 2(b) represents the electron density distribution on the same cross-section. Electrostatic potential distribution on the vertical cut-lines A, B, and C indicated in figure 2(a) are presented in figure 3.

Based on figures 1 and 2(a) one can see that during reset there is no electrostatic potential barrier from the two MIGs (located underneath G1 and G2) towards the drain contact (D1 and D2) and thus complete and very fast reset is enabled. One can also deduce from figure 2(b) (and from 2(a)) that during reset electrons flow from the depleted substrate to the drains and that interface generated electrons do not flow into the substrate (there is a potential barrier that prevents electrons located at the interface or in the source, drain, or channel to enter into the substrate, MIG layer, or into the MIGs; this can also be deduced from the electrostatic potential distributions on cut-lines A and B presented in figure 3).
3.2 Integration

The reset of the pixel is followed by an integration period wherein the nodes Gate1 and Gate2 are simultaneously biased at $+1.5\, \text{V}$ and Transfer Gate is biased at 0 V (or alternatively at a slightly higher potential such as $+1\, \text{V}$). The biasing of Gate1 and Gate2 nodes during integration is such that the channels underneath the gates are closed, i.e., the corresponding pixel row is not selected for readout.

In figure 4(a) the electrostatic potential distribution and in figure 5 the electron current distribution on a cross-section of the pixel is depicted at the end of the integration period. At this point 964 electrons are collected into the two MIGs (482 electrons in each MIG); the potential barrier from the MIG towards the drain contact is 0.74 V and the potential barrier in between the MIGs is 0.58 V. It can be deduced from figures 4(a) and 5 that the interface generated electrons are effectively prevented from entering into the MIGs and MIG layer. It can be also seen from figure 5 that there is a sufficient barrier between two pixels meaning that vertical anti-blooming mechanism is enabled.

3.3 Basic CDS measurement procedure

After the integration period and in the beginning of the readout period a readout potential configuration is first applied wherein the nodes Gate1 and Gate2 are at $+3.5\, \text{V}$ and the Transfer Gate is at 0 V. At this stage one can already measure with the first or second or both MIGFETs whether the pixel is in saturation and if so one could use the logarithmic dependence of the readout result to expand the dynamic range. The preferable way for readout in the proposed pixel is source current mode readout [19] wherein the value of the electric current at the source node is measured when all nodes of the pixel are held at fixed potentials as shown in figure 7(a).

Next a charge transfer procedure is applied to the pixel wherein 0 V is first applied to the Gate2. Then the Transfer Gate is set to $+2.5\, \text{V}$ — this potential configuration is referred to as the transfer stage, which is depicted in figure 6(a). Then the Transfer Gate is quickly set back to
Figure 4. (a) Electrostatic potential distribution during integration on a 2D cross-section of the 3D simulated pixel when 964 electrons are located in the two MIGs (482 electrons in each MIG); the potential barrier from the MIG towards the drain is 0.74 V. The potential barrier between the two MIGs is 0.58 V. The potential curves on vertical cut lines D, E, F, and G are depicted on figure 4(b). (b) Electrostatic potential during integration on vertical cut-lines D, E, F, and G depicted on figure 4(a). The signal charges in the MIG have a much smaller barrier (0.74 V) towards the drain than towards neighbouring pixels (potential maximum of G subtracted from the local potential maximum of F at the depth of around 1 µm). This means that vertical anti-blooming mechanism is enabled, i.e., excess signal charges flow into the drain and not to neighbouring pixels (or to the source which would increase the noise).

Figure 5. Electron current distribution during integration on a 2D cross-section of the 3D simulated pixel when 964 electrons are located in the two MIGs (482 electrons in each MIG). The interface leakage current is effectively prevented from entering into the MIG layer.
0 V, and finally the Gate2 is brought back to $+3.5$ V. At this stage the pixel is back to the readout potential configuration and all the 964 signal charge electrons are located in MIG1 as depicted on figure 7(b).

One can now perform the first part of the CDS procedure for the second MIGFET (located on the right hand side) by storing the readout result of the second MIGFET. Next the Gate1 is brought to 0 V, then $+2.5$ V is applied to the Transfer Gate, after which the Transfer Gate is brought back to 0 V, and finally the Gate1 is brought back to $+3.5$ V. The pixel is now back at the measurement stage but all 964 signal charge electrons are located in MIG2.

At this stage one can perform the second part of the CDS procedure for the second MIGFET by storing the readout result of the second MIGFET. The final CDS readout result for the second MIGFET is obtained by subtracting the first readout result from the second one (or vice versa). In our case it is $41.9 \mu A - 40.5 \mu A \approx 1.34 \mu A$. The charge to current conversion gain is obtained by dividing $1.34 \mu A$ by 964 electrons resulting in $1.4 \text{nA/e}$. It is important to note that during the CDS readout process of the second MIGFET all the potentials on the nodes of the second MIGFET remained fixed.

If desired one can perform during the second part of the CDS procedure for the second MIGFET also the first part of the CDS procedure for the first MIGFET by storing the readout result (obtained e.g. with different gain setting) of the first MIGFET. Then the Gate2 is brought to 0 V, next the Transfer Gate is set to $+2.5$ V after which it is brought back to 0 V, and then the Gate2 is brought back to $+3.5$ V after which one can perform the second part of the CDS procedure for the first MIGFET by storing the readout result of the first MIGFET. The final CDS readout result for the first MIGFET is obtained by subtracting the first readout result from the second one. If desired one can perform during the second part of the CDS procedure for the first MIGFET again
the first part of the CDS procedure for the second MIGFET, i.e., one could sequentially perform as
many CDS measurements as desired with both of the MIGFETs.

From the electrostatic potential distribution presented in figure 6(a) one can see that during the
transfer stage there is no potential barrier from the energetically non-preferable MIG towards the
energetically preferable MIG. The potential barrier from the energetically preferable MIG towards
the drain contact is 0.5 V. The electron density distribution during the charge transfer is presented
in figure 6(b) from which it can be deduced that all the 964 electrons are successfully transferred
to the left MIG.

The electrostatic potential distribution during the measurement potential configuration when
the 964 electrons are in the left hand side MIG is depicted in figure 7(a). The minimum potential
barrier from the MIG having 964 electrons towards the drain contact is 0.88 V and the potential
barrier from the MIG having 964 electrons to an empty MIG is 0.74 V.

4 Conclusions

The 8 µm pitch double MIG pixel structure designed for a slightly modified 0.18 µm or smaller
line width 5 V CMOS process was presented and simulated in 3D. On the basis of this study, it is
suggested for use in low light imaging as well as low energy X-ray applications. The reason is that
the pixel does not suffer from interface issues (i.e. there is no interface generated dark noise, no
interface generated image lag, and virtually no interface generated 1/f and RTS noise).
The reason for the lack of interface generated dark noise and image lag is due to the fact that in the simulated MIG pixel structure there is always a big enough potential barrier in between the signal charges and the depleted interfaces. The very low interface generated $1/f$ and RTS noise stems from the deep buried channel — the potential difference from the bottom of the buried channel to the interface is 0.45 V to 0.68 V throughout the length of the buried channel.

Furthermore the 50 $\mu$m thick fully depleted BSI pixel design offers several advantages such as 100% fill factor, high QE for NIR and visible light as well as low energy X-rays up to several keV, low crosstalk, anti-blooming, and very high readout speed. The last mentioned fact is due to the current mode readout as well as due to the fact that at reset and charge transfer stages there are no potential barriers hindering the signal charge transport.

The anti-blooming is due to the fact that the potential barrier for signal charges situated in MIG is always much lower towards the drain than towards the neighbouring pixels (and towards source node which is important from noise point of view) as can be seen from the cut-lines D, E, F, and G in figure 4(b). In the measurement and transfer potential configuration the signal charges are located underneath the gate biased at higher positive voltage than during integration and thus the anti-blooming protection is even better during other modes than during integration.

From the above results one can see that the transfer stage limits the Non-Destructive Correlated Double Sampling Full Well Capacity (NDCDSFWC) of the pixel, i.e., the maximum amount of signal charge that can be successfully stored, read out, and transferred from one MIG to another. The reason for this is that the barrier for signal charges located in the MIG to escape to drain or to an empty MIG is by far the smallest during the transfer stage. At the level of 964 signal electrons no charge loss was identified. The NDCDSFWC is estimated to be somewhere in between 1000 and 2000 electrons at $-40^\circ$C which relates to (3.6 keV to 7.3 keV). This may seem limited but one should acknowledge that the pixel design is preliminary. If a larger pixel size is used and/or the pixel design is optimised according to the FWC it is possible to considerably increase the NDCDSFWC.

According to the 3D simulations the Charge Conversion Gain for 964 electrons at $-40^\circ$ Celsius is 1.4 nA per signal electron. The simulations also show that the thick fully depleted BSI MIG pixel design possesses considerably better spatial and energy resolution for low energy X-rays as well as better low light imaging capability than a previously simulated thin front side illuminated double MIG pixel structure [20].

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