A systematic approach to designing a wide-current range, MOS capacitor-based switched-capacitor DC-DC converter with an augmenting LDO

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Summary
Switched-capacitor DC-DC converters (SC DC-DC) are analyzed for loss sources, voltage regulation integrity, start-up latency, and ripple size, while the trade-offs between these metrics are derived. These analyses are used to design a SC DC-DC that achieves high efficiency in a wide load current range. Four-way interleaving was employed to reduce the output ripple and efficiency loss due to this ripple. The design can be reconfigured to achieve gains of 1/3 and 2/5 for inputs ranging between 1.4 and 3.6 V to generate output voltage range of 0.4 to 1.27 V and can supply peak load current of 22 mA. It uses thin-oxide MOS capacitors for their high density and achieves 75.4% peak efficiency with an input frequency of 100 MHz and a load capacitor of 10 nF. An augmenting LDO that only regulates during sudden load transients helps the converter respond fast to these transients. The chip was implemented using a 65-nm standard CMOS process.

KEYWORDS
augmenting LDO, frequency control loop, interleaving, switched-capacitor converter efficiency, switched-capacitor DC-DC converter

1 | INTRODUCTION

Energy efficient systems have been the focus of both the research and development community in the last decade with the increasing interest in IoT applications, medical sensor technologies (personal/body area networks) and sensor networks for smart homes/cities. These applications require extremely energy-efficient and low-cost solutions for maximum durations of autonomous operation without the need to charge or change the battery.\(^1\)

CMOS is the preferred technology for building such systems due to its wide availability, low cost, and suitability for high integration. Low supply voltages of recent CMOS technologies necessitate efficient ways to regulate the higher battery or harvested voltages to suitable levels for the technology that is used.\(^2\) Traditionally, LDOs and switching (buck) regulators are used for regulating voltages, but they are inefficient or are large in size and costly.\(^3,4\) Recent efforts have focused on using on-chip inductors to implement buck regulators with limited success due to the inherent small value and low-Q of these inductors.\(^3\)

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Switched-capacitor DC-DC converters (SC DC-DCs) have received recent attention as the alternative way of achieving high-efficiency power conversion. Although, on-resistance of switches, limited Q of capacitors, and non-zero equivalent output resistance of the converter due to limited capacitor size and switching frequency speed cause the efficiency to drop, it is still possible to design fully integrated SC DC-DCs with high conversion efficiency for moderate output power levels.2,3,5,6

Main contributions of this paper are analyzing the design tradeoffs of SC DC-DCs in a unique approach and using the results of these analyses to come up with a systematic way of choosing design parameters (switch widths, switching frequency vs output current) using a tool like MATLAB. Similar analysis was introduced in Le et al3 and Seeman and Sanders7 previously, but their contribution to practical design procedure is limited. Le et al3 solves analytically for the optimal total loss; however, their solution is too complicated to be used practically in the design procedure. Seeman and Sanders7 defines the loss sources similar to Le et al3 and finds the optimal power loss mathematically. Rather than giving a systematic design approach, they use various topologies to verify their analysis. Additionally, our work derives start-up and response time of the converter to current load as a function of load and flying capacitor sizes for the first time. Le et al2 and Ramadass et al6 use frequency and capacitor scaling techniques, respectively, to control the losses and output fluctuations due to fast transients. These techniques are prone to generation of unknown frequency tones on the regulated supply and have increased losses due to additional control circuitry. El-Damak et al5 and Ramsden8 use ferroelectric capacitors and SOI technology, respectively, to minimize losses; however, their design analysis is limited, and these technologies are not available in bulk CMOS, which is the preferred technology.

A fully integrated converter was implemented in 65-nm bulk CMOS technology using thin-oxide MOS capacitors with a peak efficiency of 75.4% using all the analyses presented here. The design supports gain ratios of 1/3 and 2/5 with more than 50% conversion efficiency while supplying load currents of 100 μA to 22 mA and operating from 1.4 to 3.6-V supply voltages to generate output voltages in the range of 0.4 to 1.27 V. The design also uses an augmenting ultra-low-power LDO to respond to fast load current transients as a novelty.

2 | SWITCHED-CAPACITOR DC-DC CONVERTER DESIGN ANALYSIS

Switched-capacitor DC-DC converter design involves many trade-offs between various design criteria such as efficiency, power density, supply integrity, ripple size, and complexity. In order to optimize for 1 or more of these criteria, optimal switch sizes, flying capacitor sizes, and switching frequency need to be chosen for a given load current. In this section, we will analyze the trade-offs in detail and give a guideline to achieve a concurrent optimization for these design criteria.

2.1 | Operation principle

In order to establish a foundation for the analysis of the SC DC-DCs, we would like to first briefly explain the operation principle of these circuits. Figure 1A shows the circuit level diagram of a sample 3:1 step down converter.
There are 2 phases that the switches of the converter operate in. Turning the switches on and off in each phase alternates the mode of the converter between common mode and gain mode.\textsuperscript{3} The internal flying capacitors are charged from the input during the common mode, and they deliver charge to the output during the gain mode. The switches $S_1$, $S_4$, and $S_7$ are on in the common mode ($\varphi_1$) as shown in Figure 1B, and the 2 flying capacitors have $(V_{IN} - V_{OUT})/2$ across them. In the gain mode ($\varphi_2$), switches $S_2$, $S_3$, $S_5$, and $S_6$ are turned on, and all the flying capacitors are connected in parallel between the output and ground as shown in Figure 1B. They now deliver the charge stored in each capacitor to the load capacitor until the voltages on all capacitors are equalized. The duty cycle of the clocks for each phase is set to 50\% to maximize the charge transfer period. In steady state, the output voltage equals to approximately one third of the value of the input voltage source with some ripple on the top, which means that the gain of the converter is 1/3. Similar explanations can be extended to other conversion ratios.

A large load capacitor is not necessary in the design as long as the converter can charge up the output node much faster than the load current discharges it; however, an adequate size load capacitor is usually used to minimize ripple on this voltage. This capacitor serves as a charge bucket to supply the load current. Although the converter is more resilient to instantaneous load current jumps with the use of a large capacitor, it slows down the initial start-up of the converter because it requires more time to charge up. Moreover, for systems where the on/off-time ratio is small, a sizable amount of power is lost to charge up the output each time the system turns on, assuming a fully discharged load capacitor.

### 2.2 Converter loss analysis

There are various loss mechanisms in SC DC-DCs, which limit their efficiency. These losses can be summed up in 4 categories: losses due to the equivalent output resistance of the converter, switching, bottom-plate parasitic, and the control circuitry. While some of these loss mechanisms have identical drift with the design parameters, others are affected adversely for a given load condition. Thus, in order to find a global optimization for the converter design, loss mechanisms as a function of design parameters need to be analyzed and determined accordingly.

The first of the losses mentioned earlier is the intrinsic loss to all types of regulators. Figure 2 shows a generic linear model for regulators in general,\textsuperscript{3} and same model applies to the SC DC-DC discussed in this paper. $R_{OUT}$ defines the deviation of the regulator from an ideal voltage source and causes undesirable power dissipation. Some work in literature has extensive analysis on the estimation of this output resistance.\textsuperscript{3,5} In SC DC-DCs, 2 factors contribute to this effective output resistance: the on-resistance of the switches used in the design and the equivalent switched-capacitor resistance.

Because the charge transferred from the input to the output goes through all the switches in the network, each switch contributes to the overall power loss with a weight factor. $S_1$, $S_4$, and $S_7$ in Figure 1 are connected in series from input to the output during phase $\varphi_1$. All the charge transferred to the flying capacitors go through these resistors, and this phase is active half of the clock cycle; hence, they have a weight ratio of 1/2. During $\varphi_2$, each flying capacitor supplies half of the charge transferred to the load, and again this phase is the active half of the period; hence, the weight factor for each switch is 1/4. Consequently, overall power dissipation due to the switches can be estimated as in Equation 1. Same analysis can be extended to multi-phase SC DC-DCs:

$$P_{RSW} = I_L^2 \sum \frac{R_{on switch}}{R_{on switch}} \cdot \text{weight}_n$$

\textbf{FIGURE 2} Linear model of a DC-DC converter [Colour figure can be viewed at wileyonlinelibrary.com]
where $I_L$ is the load current, $R_{onsw}$ is the switch resistance, and $S_{weight}$ is the weight for each switch. $S_{weight}$ specifies the ratio of the load current that flows through each switch during operation.

For our example in Figure 1, assuming all the switch on resistances are equal, this power dissipation can be estimated to be

$$P_{Raw} = I_L^2 R_{onsw} \left( \frac{1}{2} + \frac{1}{2} + \frac{1}{4} + \frac{1}{4} + \frac{1}{4} + \frac{1}{4} + \frac{1}{4} \right) = \frac{5}{2} I_L^2 R_{onsw}. \tag{2}$$

In order to completely quantify the losses due to $R_{OUT}$, the equivalent switched-capacitor resistance for the converter needs to be calculated as well. The net charge transferred to the output during 1 clock cycle can easily be written as the difference of the charge on the flying capacitors at the ends of each cycle. Equating this to the charge lost during each clock cycle due to the load current, we can solve for the minimum voltage that the output goes down to.

$$Q_{net} = AC_{fly}(V_i - V_{o, min}) - BC_{fly} V_{o, min} = I_L T_{period} \tag{3}$$

$$V_{o, min} = \frac{AC_{fly} V_i - I_L T_{period}}{C_{fly}(A + B)} \tag{4}$$

Equation 4 shows the minimum output voltage level at the end of the discharge phase. Coefficients A and B are specific to each conversion ratio configuration and are scaling factors for the total charge stored in the flying capacitors during the 2 phases. For a conversion gain of 1/3, A and B are equal to 1 and 2, respectively, and are calculated as follows.

During $\phi_1$, 2 $C_{fly}$ are connected in series, and each sees $(V_i - V_{o, min})/2$ across them. So, the total charge stored is $2^*C_{fly}*(V_i - V_{o, min})/2$; hence, A = 1. Similarly, during $\phi_2$, 2 $C_{fly}$ are connected in parallel to the output node. So, the total charge is $2^*C_{fly} * V_{o, min}$; hence, B = 2. Because of charging and discharging in between the 2 phases, the output goes up and down by an amount $\Delta V$ from this value of $V_{o, min}$. The charge dissipated in the load during $\phi_2$ comes from the flying capacitors in the absence of any load capacitor and causes the output voltage to drift down by $\Delta V$. It can be written in terms of the load current as

$$\Delta V = \frac{\Delta Q_{o}}{BC_{fly}} = \frac{I_L T_{period}}{2} = \frac{I_L}{C_{flyout} 2 f_{sw}} \tag{5}$$

where $C_{flyout}$ is the total equivalent flying capacitance looking back from the load during phase $\phi_2$. This is equal to the amount of capacitance charged during $\phi_1$ to replace the dissipated charge. For our example in Figure 1, this capacitance is the parallel combination of the 2 flying capacitors, therefore is equal to $2C_{fly}$. The frequency $f_{sw}$ is equal to $1/T_{period}$. Now, we can approximate the average output voltage using Equations 4 and 5:

$$V_{OUT} = V_{o, min} + \frac{\Delta V}{2} \tag{6}$$

Assuming the switch on-resistances are zero, power dissipation due to the equivalent switched-capacitor resistor can be derived by multiplying the overall drop in $V_{OUT}$ by the load current, $I_L$,

$$P_{Csw} = (V_{o, ideal} - V_{OUT}) I_L = \frac{(3B-A)I_L^2}{4B(A + B)C_{fly} f_{sw}} \tag{7}$$

where $V_{o, ideal}$ is given by Equation 4 when the load current is equal to zero. It can be deduced from Equation 7 that the equivalent output resistance due to capacitor switching is given by

$$R_{Csw} = \frac{(3B-A)}{4B(A + B)C_{fly} f_{sw}} \tag{8}$$

Apart from the losses mentioned earlier, any parasitic capacitor in the network causes additional power loss due to switching activity. These capacitive losses stem mainly from the top/bottom plate capacitors of the flying capacitors and interconnect capacitors. As the converter switches between the 2 phases $\phi_1$ and $\phi_2$, internal nodes swing between 2 different values. For instance, the bottom plate terminal of the top flying capacitor in Figure 1 swing to $2V_{OUT}$ and ground.
between the 2 phases. Hence, any parasitic capacitor to ground at this node dumps charge equal to \(2C_{\text{Par}} V_{\text{OUT}}\) to ground during each cycle. Similar undesired power dissipation occurs in all the internal nodes of the converter core. Sum of all the power loss can be given by:

\[ P_{C_{\text{par}}} = \sum_n (M_n V_{\text{OUT}})^2 C_{n, \text{par}} f_{\text{sw}} \]  

(9)

where \(M_n\) specifies the ratio of the voltage swing at each node compared with \(V_{\text{OUT}}\). Equations 7 and 9 can be used to find an optimal flying capacitor size by equating them and solving for \(C_{\text{fly}}\). Analytical solution for the capacitor size is usually very large for practical on-chip capacitor areas, so the rule of thumb is to use as large flying capacitor as possible in the design. This capacitor size is usually limited by the available die area, and the total flying capacitor size used in the design and in all our analysis is 4 nF unless otherwise specified.

Similar to parasitic capacitance losses, the gate capacitors of the switches used in the converter cause additional undesired power dissipation as the switches toggle on and off. Similarly to Equation 9, this portion of the overall power dissipation can be given as:

\[ P_{C_{\text{g}}, \text{sw}} = \sum_n V_{G,n}^2 C_{G,n} f_{\text{sw}}. \]  

(10)

\(V_{G,n}\) in this equation is the control voltage swing at the gate of each individual switch. Similarly, \(C_{G,n}\) is the equivalent gate capacitance of each switch.

It is apparent from Equations 7, 9, and 10 that there exists an optimal frequency for the converter to operate at for a given load current. This usually requires some sort of a feedback control loop to control the switching frequency or switching regularity (usually through hysteresis) of the converter. Both the frequency/hysteresis control loop and all the auxiliary digital circuitry may require considerable digital circuit overhead that are switching at the converter clock frequency. Considering both the dynamic and static power dissipation in the digital control circuitry, the power dissipation can be estimated as follows.

\[ P_{\text{Dig, cont}} = \sum_n V_{\text{sup},n}^2 C_{\text{fsw},n} f_{\text{sw},n} + V_{\text{sup},n} I_{\text{ss}} \]  

(11)

This equation assumes multiple supply and frequency domains shown as \(V_{\text{sup},n}\) and \(f_{\text{sw},n}\). While the digital control circuitry works at a constant frequency, the circuitry that generate the non-overlapping switching clocks change their frequency as the switching frequency is scaled to optimize the efficiency and various frequency domains form inside the converter. Frequency scaling can be done in various ways ranging from a simple PLL to cascaded frequency dividers.

Equations 2, 7, 9, 10, and 11 can be used to find an analytical equation that provides the optimal frequency and the total switch size for maximum power efficiency of a given conversion ratio as shown in Le et al.\(^3\) Intuitively, power dissipation in Equation 7 reduces, while it increases in Equations 9, 10, and 11 as the switching frequency increases, which proves the existence of an optimal operating frequency for maximum power efficiency for a given load current, gain ratio, flying capacitor, and total switch sizes. Similarly, power dissipation decreases in Equation 2 but increases in Equation 10 with increasing switch sizes.

For a practical approach, a tool similar to MATLAB can be used to find the optimal frequency and switch width values for the design using the power equations given above. Figure 3 shows the efficiency of the converter as a function

![FIGURE 3](https://wileyonlinelibrary.com)
of switch size and switching frequency for a given load current. This graph is drawn for the topology given in Figure 1 but can be extended to any converter topology. It is clear from this figure that for each load current value, a range of switch size and switching frequency values can be picked up in the proximity of maximum efficiency. By generating a similar graph for various load current values, total switch size to give a near optimal efficiency across a wide range of load current values can be found. Although there is an optimal switch size for each load condition, by using these plots, a suitable value for switch sizes can be picked to achieve high efficiency across a wide range of load conditions.

Once the total switch width sizes are decided on using the method discussed previously, we can use the same set of equations to plot the efficiency as a function of switching frequency and load current amount. This results in an optimal frequency for each load current to give a set of peak efficiencies, as shown with the red line in Figure 4, for the total switch size of around 1 mm used in our design. In order to maximize the efficiency across a wide range of load currents, we need to make sure that the switching frequency follows the peak trend shown in this figure. This can be done by measuring the load current and changing the frequency to operate the converter at the highest efficiency, as discussed in the next section.

2.3 | Peak efficiency operation and voltage regulation integrity

In order to design a robust and efficient converter, it is quite important to quantify the integrity of regulation for the converter and achieve this integrity at the peak efficiency. Equation 6 gives the output voltage level for a given load and switching frequency condition for a specific converter. Also, switching frequency is optimized for peak efficiency for a certain load current as shown in Figure 4. This necessitates that the switching frequency decision is continuously re-evaluated for changing load currents to maximize the efficiency and keep the regulation integrity at the same time. In order to achieve this, load current level needs to be measured and fed back to a frequency scaling loop to control the frequency for optimal efficiency.

Although the easiest way to quantify the load current is to insert a resistor in series with the load and measure the voltage drop across it, there are drawbacks in this approach as it increases the output ripple and power loss due to the series resistance included in the current path. Also, wide range of load current requires that this resistor made programmable and calibrated for acceptable performance. Another approach is using Hall-Effect sensors to mitigate these issues, but this increases the complexity enormously.

An alternate approach to measure the load current appears in light of Equation 6. Figure 5 shows the output voltage as a function of the switching frequency and load current. It is clear from this graph that the output voltage drops...
dramatically at high load currents if the switching frequency is low. Keeping the frequency high solves this issue, but as seen in Figure 4, this causes the efficiency to suffer. An optimal solution can be found by mapping the peak efficiency line \((f_{sw} \text{ vs } I_{load})\) in Figures 4 to 5 directly and designing a control circuitry to operate the converter along this optimal line. This line shown in red in Figure 5 gives an output voltage value for each switching frequency and load current pair. Because the output voltage is related to switching frequency as shown in this graph, we can measure the voltage at the output and change the frequency accordingly. The red peak efficiency line in Figure 5 corresponds to an output voltage of around 1 V for our example in Figure 1, and an optimal switching frequency can be chosen to keep the output voltage at this level. The scheme to achieve optimization of power efficiency along with regulation integrity is described in detail in Section 3, the proposed design part.

### 2.4 Converter start-up time

Another important parameter for DC-DC converters in general is the response time during initial start-up or load transients. In order to analyze the response time of a typical converter, we will start with the start-up time from a cold start. During each clock period, an amount of charge is transferred from the input to the output and stored on the load capacitor, \(C_L\). The voltage increase at the load can be quantified assuming preservation of charge during each clock period.

\[
Q_{φ1} = A C_{fly} (V_i - V_o) + V_o C_L
\]

\[
Q_{φ2} = (V_o + ΔV_o) (BC_{fly} + C_L)
\]

Equating 12 and 13, incremental voltage at the output after each clock cycle can be found.

\[
ΔV_o = \frac{AC_{fly} V_i - (A + B) C_{fly} V_o}{BC_{fly} + C_L}
\]

Using the incremental voltage at the output after each clock cycle, we can come up with an equation for the output voltage after \(n\) clock cycles.

\[
V_{o,n} = V_{o,n-1} + ΔV_{o,n} = \frac{n A C_{fly} V_i - \sum_{x=1}^{n-1} (A + B) C_{fly} V_{o,x}}{BC_{fly} + C_L}
\]

We can now solve for the time that is required for the converter output to reach a certain level. As expected, increasing \(C_L\) increases the time for the converter to settle down because the voltage steps shown in Equation 14 are smaller. \(C_{fly}\) has a more complex effect on the rise time, but for \(C_L\) values considerably larger than \(C_{fly}\), increasing \(C_{fly}\) reduces the initial rise time of the output. Figure 6 shows the output voltage rise time for the example in Figure 1 as a function of \(C_{fly}\) and \(C_L\) sizes.

### 2.5 Output ripple and interleaving

Output current and voltage ripple size in steady-state operation is a main concern for SC DC-DCs. While minimizing the undesired current ripples in the load increases efficiency as discussed in Le et al., reduced voltage ripples is critical for creating a cleaner supply. In steady state, assuming that the load capacitor is much larger than the flying capacitors, the output voltage drifts down by the same amount during the common mode and gain mode. This creates a repetitive charge up and down of the output voltage, which is defined as the output ripple. Using the charge dissipated during the gain mode, we can estimate the output ripple by:

\[
ΔV_o = \frac{ΔQ_L}{BC_{fly} + C_L} = \frac{I_L}{BC_{fly} + C_L} \frac{T_{period}}{2} = \frac{I_L}{BC_{fly} + C_L} \frac{1}{2 f_{sw}}
\]

This equation assumes that the charge transfer between the flying and load capacitors is very fast and the output voltage reaches the maximum value quickly. This is the case when the on-resistance of the switches are small and the capacitor voltages equalize rapidly; hence, most of the time in gain mode is used for the discharging of the total load capacitor with the load current. This condition results in worst case ripple voltage. It is apparent from Equation 16 that there are...
various approaches that can be employed to reduce the ripple size. Firstly, the size of both the flying and the load capacitors has an adverse effect on the ripple size; hence, their size is maximized as much as possible. However, $C_{fly}$ size is limited by the chip area, and $C_L$ is limited by the required time to start up the converter or to respond to load transients. Similarly, frequency has an adverse effect on the ripple size as well, i.e., increasing switching frequency reduces the ripple size. Nevertheless, switching frequency is usually optimized for maximum converter efficiency; hence, its value is bounded by a limit.

In the case that the on-resistance of the switches are higher or the switching frequency is high, the ripple deviates from this worst case equation. For light load condition, most of the charge transferred goes to the load capacitor and increases the output voltage close to the value given in Equation 16. For higher load currents, most of the charge transferred is used to supply the load current; hence, the voltage rise on the output capacitor is limited. Consequently, in the case that the charge sharing is not much faster than the discharge rate, ripple increases with reduced load current to approach the value given in Equation 16.

Another very common and effective way to reduce ripple size is utilizing interleaving in the design. In this approach, the converter is divided into many scaled down unit converters. These unit converters are operated by phase separated non-overlapping clocks in order to charge the load capacitor in smaller portions. Because the output is charged in smaller steps and multiple times in a clock cycle, $T_{period}$ given in Equation 16 is effectively reduced by the number of interleaving stages without actually increasing the switching frequency.

3 | PROPOSED SC DC-DC DESIGN

3.1 | Frequency scaling loop

The proposed converter uses a 4-way interleaving along with a dynamic frequency control loop, as shown in Figure 7. Analysis in Section 2 and simulations were used to decide on an external load capacitor value of 10 nF, which is optimized for an acceptable start-up time of less than 5 μs with the smallest possible average ripple size of 10 mV. The load capacitor can be reduced further at the cost of larger ripple size and integrated on the chip, e.g., an integrated load capacitor of 4 nF will simply double the size of the solution. The utilized control loop measures $V_{OUT}$ and uses this information to operate the converter at the optimal frequency across a wide range of current values as shown in Figure 4. Consequently, tight output voltage regulation can be achieved at all load currents, and the efficiency can be kept high simultaneously.

The input clock for the converter is 100 MHz nominally, and scaled down versions of this clock are used as the multiphase clock for the converter core as well as the control circuitry. The converter loop starts at the lowest switching frequency that is 1/128th of the nominal input clock rate. The clock generator produces 4 equally spaced clock phases and their non-overlapping inversions in order to be used in the 4-interleaving cores. Using non-overlapping clock phases in each core is important to separate the 2 phases of the circuit operation and minimize direct path losses. Each clock and
its non-overlapping inversion is shown as PHI1 and PHI2, respectively, in Figure 8 and goes into 1 of the 4-way interleaving cores to switch it between the 2 phases as shown in Figure 9.

In order to implement the dynamic frequency scaling technique utilized in the converter, 2 comparators are used to compare the output voltage against 2 reference voltages offset from the desired output voltage that gives the highest efficiency, in positive and negative direction as shown in Figure 7. These 2 levels are used to create a dead-band where V_{OUT} settles to. If V_{OUT} is less than V_{ref1}, an accumulator counts up once every 512 reference clock cycles. This provides adequate time for the converter to settle down in between 2 consecutive accumulator values. Each time the accumulator counts up, division ratio of the input clock is halved. Once V_{OUT} settles between the reference voltages or the accumulator output reaches the maximum value, the loop stops. Oppositely, if the converter runs at a higher frequency than optimal, V_{OUT} will settle higher than V_{ref2} and the accumulator starts counting down to reduce frequency until V_{OUT} settles between the reference voltages or minimum switching frequency is reached. The optimal reference voltages for our example in Figure 1 were found to be 1.04 and 1 V from the analysis in Section 2. This scheme and the chosen values ensure that frequency-load current curve of the converter follows the peak line in Figure 4.

![FIGURE 7](image1.png)  
Top level block diagram of the SC DC-DC converter

![FIGURE 8](image2.png)  
Transistor-capacitor implementation of the SC DC-DC converter core [Colour figure can be viewed at wileyonlinelibrary.com]
3.2 | Converter core

Figure 8 shows 1 of the 4-interleaving cores used in the design. Only gain ratios 1/3 and 2/5 are used to limit the voltage levels to values suitable for 2.5 and 1.2-V switches (P25, N25, N12) with a 3.3-V input. These switches have less on-resistance with less parasitic capacitance compared with 3.3-V switches. Switch positions during PHI1 and PHI2 for each of these gain configurations are given in Figure 9A,B, respectively. Two switches are implemented using pass-gates because the PMOS helps with the initial charge transfer and NMOS has lower resistance at steady state. Furthermore, 2 switches named N12 are implemented using 1.2-V devices for the same reason given earlier. Each of the 4 flying capacitors in a core is implemented using P-type core MOS capacitors (1.2 V) for their high density of 8fF/um² and are 275 pF in size. These P-type capacitors are in P-wells, and these wells are isolated from the substrate with deep-N-wells. These deep-N-wells are floated to reduce the total parasitic capacitance by placing the 2-junction capacitors (P-well-to-N-well and N-well-to-P-substrate) in series. Each flying capacitor causes 0.5 μA of gate leakage that results in a total of 8-μA gate leakage, which adds to the losses of the converter. This leakage only affects the efficiency of the converter at very low load currents.

The voltages across the switches and capacitors never exceed their maximum ratings in steady-state operation. If the load capacitor is not charged initially, voltages during start-up can exceed the maximum reliable voltage ratings, but they never exceed the breakdown voltage levels of the transistors. Furthermore, in few cycles, the load capacitance is charged up to the steady-state operation values which are within the maximum reliable voltage levels. This initial transition is expected to be much less than the overall operation duration of the module; hence, the expected degradation on the lifetime is negligible. Protection circuits can also be included to ramp up the input voltage during turn-on for increased reliability.

In order to limit the losses given in Equation 10 that are due to the switching of the gate capacitance of the switches, gate drive for each switch is defined between 3.3 and 0 V, V_OUT and 0 V, or 3.3 V and V_OUT to reduce unnecessary swing. Gate drive for each switch is specified in Figure 8 via control signal naming where VDD33 is the 3.3-V supply and V_OUT is the SC DC-DC output voltages. Range for each gate is defined considering voltage swings at the terminals of these switches, eg, if the drain or source terminal of a NMOS device switches from 3.3 V to V_OUT, the driver for the MOS switch works between 3.3 V and V_OUT rather than between 3.3 V and GND. Similarly, if the naming of the signal ends with OUT_GND, the driver for this signal is supplied directly from the OUT node. By running start-up simulations across PVT (−40 to 85°C) with different load conditions, we have verified that the converter starts up without any issues.
3.3 | Augmenting LDO

Although described loop helps the converter work at high efficiencies over a wide range of load currents, it is slow to respond to sudden changes in the load. In order for the converter to respond quickly to these disturbances, a low-power, augmenting LDO as shown in Figure 1 was implemented and placed in parallel with the SC DC-DC. The reference voltage for the LDO is set slightly lower than \( V_{\text{ref}2} \). In case a sudden positive change occurs in the load current, the output voltage drops because the switching frequency is optimized for the lower load current and it cannot supply the required charge. When \( V_{\text{OUT}} \) drops below \( V_{\text{ref}3} \), LDO starts regulating the output and limits the drop at the output to slightly less than \( V_{\text{ref}3} \). Simulations show that depending on the step size, the drop can be as large as \( V_{\text{OUT}}/2 \) without the augmenting LDO. This causes a big concern because the digital circuits may lose state, and such glitches may reset the analog circuits.

The LDO was implemented as a 2-stage amplifier and can supply as high as 20 mA during transitions. In order to minimize the impact on efficiency, it dissipates less than 10 uA when idle. The dominant pole for the LDO was placed at the output node owing to the 10-nF load capacitor of the SC DC-DC. Because the output current of the LDO varies from 0 A to 20 mA during operation, the dominant pole moves closer to non-dominant poles at the high end of the current range. Consequently, the phase margin of the LDO becomes marginal but is guaranteed by design to be more than 30° across PVT with careful design.

4 | EXPERIMENTAL RESULTS

The design was fabricated in a 65-nm standard CMOS process by UMC with an active design area of 720 × 800 μm\(^2\). Figure 10 shows the chip photo with the converter highlighted.

Figure 11 shows efficiency vs load current measurements with 3.3-V input for the 2 gain configurations with an input clock of 50 and 100 MHz; 1/3 configuration shows a peak efficiency of 75.4% at 4.36-mA load current. The efficiency is higher than 50% over a current range of 100 uA to 20 mA; 2/5 configuration has a peak efficiency of 74.2% at 11.5 mA with the efficiency being higher than 50% over the current range of 300 uA to 22 mA.

Measured \( V_{\text{OUT}} \) for 3.3 V input was between 0.936 and 1.1 V for \( G = 1/3 \), and between 1.08 and 1.32 V for \( G = 2/5 \) as shown in Figure 12, with the low values occurring at higher output currents due to higher IR drop across \( R_{\text{OUT}} \) given in Figure 2. The reference voltages are set to 1.04 and 1 V for the 1/3 gain setting, to 1.2 and 1.25 V for the 2/5 gain setting according to our previous analysis. Increasing the switching frequency reduces the \( R_{\text{OUT}} \) of the converter until switch on-
resistances become dominant. Once the switch on-resistances dominate the $R_{OUT}$ or the switching frequency is maximized, $V_{OUT}$ reduces linearly to values lower than the reference value with increasing load current as seen at the high current range of Figure 12. At very low output currents and once the switching frequency is at its minimum value, this drop is insignificant; hence, $V_{OUT}$ reaches the theoretical value above the reference level.

In order to verify the operational input range of the converter, we swept the input voltage from 3.6 V, which is the peak safe voltage for the IO devices, down to the smallest possible value with a 500-Ω load resistance and the results are shown in Figure 13. Output voltage scales linearly with the input voltage for most of the sweep range as expected. Efficiency for both configurations is almost constant for inputs as low as 1.8 V. Although the efficiency drops dramatically below 1.8 V, the converter is still operational for input voltages greater than 1.4 V for both gain configurations.

Figure 14 shows the change in the switching frequency as a function of the load current. The frequency scales between $f_{clk}/128$ and $f_{clk}$ gradually as the load current increases. At low output loads, the frequency settles to the lowest value due to the limited division ratio implemented. As the load current increases, the loop increases the switching frequency to keep the efficiency high and prevent the output ripple becoming too large. Measured average output ripple was around 10 mV with a maximum of 25 mV across all load and frequency conditions.

A 3-bit resistive load DAC was implemented on-chip to test sudden changes in the load current. The DAC is configured from 8 KΩ to 62.5 Ω in 8 steps. This enables fast switching of the load from a small value to a large value. Figure 15 shows $V_{OUT}$ with a load current jump from 1 to 9 mA with and without the augmenting LDO enabled. Results show that, when the augmenting LDO is disabled, $V_{OUT}$ drops to as low as 533 mV (top graph) before the SC DC-DC can recover it.
FIGURE 13  Efficiency and output voltage vs input voltage [Colour figure can be viewed at wileyonlinelibrary.com]

FIGURE 14  Switching frequency vs I_{load} for the 2 gain settings and input clocks [Colour figure can be viewed at wileyonlinelibrary.com]

FIGURE 15  V_{OUT} transient to I_{load} step with LDO OFF (top) and ON (bottom) [Colour figure can be viewed at wileyonlinelibrary.com]
by increasing the switching frequency, which approximately takes 15 us. When the LDO is enabled, it holds the output voltage at the level of Vref3 (bottom graph), which is 900 mV in this case. In the meantime, the SC DC-DC increases the switching frequency to take over the regulation from the augmenting LDO, which goes back to the idle state, and increases the output voltage to a value between Vref1 and Vref2. The output voltage being much higher than 900 mV in Figure 15 ensures that the LDO is in idle state.

Table 1 shows the performance summary and the comparison of the current design with the state of the art. Although references 3, 5 demonstrate higher peak efficiency than the proposed work, they use special process options of SOI technology and ferroelectric trench capacitors to reduce bottom plate parasitic capacitance.

### 5 | CONCLUSION

In this work, we have analyzed SC DC-DCs for loss sources, efficiency, and response time with a unique approach. Analytical and practical design procedures have been highlighted to guide engineers in their design efforts. With the help of MATLAB, these guidelines were used to design a converter systematically as the main contribution of this work. The design utilizes 4-way interleaving and a frequency scaling loop to keep the efficiency high across a wide range of load currents. The converter uses thin oxide MOS capacitors with gain ratios of 1/3 and 2/5, works from 1.4 to 3.6 V supply voltage range, and the peak efficiency is 75.4%. It can supply as high as 22 mA current to the load. An augmenting LDO helps the converter respond to fast transients in the load current by regulating the output during these transients until the SC DC-DC responds to the current step by increasing its switching frequency.

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