Fault Current Limiter Dynamic Voltage Restorer (FCL-DVR) With Reduced Number of Components

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Abstract—In this article, a new dual-function fault-current limiter-dynamic voltage restorer (FCL-DVR) topology is proposed. The proposed structure, in addition to performing routine FCL tasks, can be used to improve the voltage quality of point of common coupling. A salient feature of this FCL-DVR is its reduced number of semiconductor switches and gate drive and control circuit components. Perhaps, variety structures of FCL-DVR have been proposed but most distinctive feature of proposed structure is lower power loss. The operation modes and the control strategy of the FCL have been presented and studied. In addition, the proposed structure has been compared with other structures to prove the efficiency of the proposed structure. The simulation results as well as experimental outcomes from a laboratory scaled-down prototype are provided, which prove the efficiency and feasibility of the proposed structure.

Index Terms—Dynamic voltage restorer (DVR), fault current limiter (FCL), power quality, voltage compensation.

NOMENCLATURE

- \( C_1 \) Output filter capacitance (F).
- \( L_m \) Magnetizing inductance (mH).
- \( L_r \) Leakage inductance (mH).
- \( U_{comp} \) Series injected voltage (V).
- \( t_f \) Time of fault occurrence (S).
- \( L_t \) Total of inductance of source, transmission line and transformer leakage inductance (mH).
- \( R_t \) Total resistance of source and transmission line (Ω).
- \( L_L \) Load inductance (mH).
- \( R_l \) Load resistance (Ω).
- \( \omega_0 \) Natural frequency of the network (Hz).
- \( Z_{\text{FCL}} \) Impedance of FCL.
- \( Z_{\text{Line}} \) Impedance of transmission line.
- \( \alpha \) Percentage of line voltage variation after fault.
- \( V_{LR} \) Voltage drop in the transformer leakage inductance.
- \( a \) Turns ratio of the transformer.
- \( \lambda \) Ratio of injected voltage to line voltage.
- \( P_{\text{core}} \) Iron loss of transformer (W).
- \( P_{\text{cu}} \) Copper loss of transformer (W).
- \( P_{\text{igbt}} \) IGBT losses (W).
- \( R_T1 \) Resistance of the primary winding (Ω).
- \( R_T2 \) Resistance of secondary winding (Ω).
- \( V_{\text{CES}} \) Forward blocking voltage of IGBT (V).

I. INTRODUCTION

THE PROMOTION of modern electric power system and their interconnections has led to the high fault currents levels that may go beyond of the maximum short-circuit ratings of the switchgears in some points of the grid. Despite advantages of modern networks, large power networks exhibit some problematic issues such as high complexity, lower security, and high-level fault currents [1], [2]. Furthermore, these power networks suffer from the probable decrease in the quality of the load voltage due to the nonlinear loads and high penetration of renewable energy systems. On the other hand, in a competitive electricity market, the voltage improvement is very crucial, and companies must improve the quality of the power provided to the consumer in order to gain more share of the electricity market. Also, by increasing the number of sensitive loads, importance of the power quality becomes a priority in the operation of power delivery system.

Among different types of disturbances that can occur in the power system, such as voltage sags, voltage swells, imbalances, frequency deviations, flicker, and harmonics interruption, voltage sag is known to produce the most devastating impact on the loads [3], [4]. Voltage sag is mainly a result of short-circuits in the grid. Studies have shown that 92% of all disturbances in the industrial distribution systems are voltage sags, transients, and momentary interruptions [5], [6]. The importance of the power quality has prompted installation of power conditioning equipment to mitigate voltage disturbances. Many solutions are available to improve power quality [7]. Among these solutions, dynamic voltage restorer (DVR) is the most deployed solution to compensate for voltage sags [8]. DVR consists of a voltage source inverter (VSI) to inject voltage in series with the line, injection transformer, and a dc link for voltage sag interval. The DVR injects voltage to compensate the sag and as a result, the load voltage remains almost constant.

Manuscript received August 4, 2020; revised October 7, 2020 and December 22, 2020; accepted December 29, 2020. Date of publication January 14, 2021; date of current version September 22, 2021. (Corresponding author: Pedram Ghavidel.)

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/JESTIE.2021.3051586.

Digital Object Identifier 10.1109/JESTIE.2021.3051586

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Today, with increasing number of faults and increase in the current amplitude at the time of the occurrence of the fault, the need for installation and use of fault current limiting to protect the network becomes a necessity. An efficient design of FCL should have a low number of elements and a simple control circuitry. In addition, it must limit the fault current efficiently and improve the voltage quality perfectly. From costs perspective, a structure with less number of elements is usually economical. Recently, different types of FCLs are presented with different features [9]–[11], [27]. Whereas the need for a structure that can limit the fault currents is investigated in the literature, a simultaneous voltage sag compensation or harmonics compensation is studied just in few literatures such as [9]–[12]. In [9], a novel structure is proposed with both fault current limiting ability and DVR functionality. Proper control strategy in this structure enables the low power loss during short-circuit limiting and voltage restoration. This can reduce the current of power supply during fault current limiting. In [10], a dynamic-voltage conditioner is analyzed to find the fault current limiting availability. Therefore, within the proper range, the opening time of upstream circuit breaker can be guaranteed. In [11], a virtual impedance based FCL is proposed to be used in downstream DVRs. This structure can insert high series impedance to line to reduce the fault current. In [12], active solutions for embedding fault current limiters into dynamic voltage conditioner are investigated. An auxiliary controller for downstream FCL in a radial distribution line by means of a DVR is presented in [8]. This control scheme has two inner and outer loops for providing damping for the transients caused by the DVR filter and controlling the injected voltage magnitude and phase angle of the faulty phase to interrupt the fault current and restore the PCC’s voltage, respectively. In [13]–[15], virtual current-limiting impedance technique is used to create high impedance during fault. To this end, a virtual RL impedance upon sensing of a voltage sag will be inserted to the line. However, this can cause circulating active power through the series and shunt converter. To alleviate this issue, the flux-charge model scheme which only insert a virtual inductor in series with line, is recommended in [13]–[15]. In comparison with RL feedforward scheme, this method can limit the line current by absorbing of nearly zero active power by the converter. Unlike [13]–[15] which recommend fixed virtual impedance insertion, in [16], the FCL–DVR behaves as a virtual inductance with a variable value. Since inductance is utilized to avoid large swings in this scheme, the real power absorption is inevitable, and the dc-link capacitor will be aged quickly. Another scheme to achieve both DVR and FCL functionalities is to use the filter inductor as a part of the LC filter under normal operation conditions, as well as an impedance to limit the fault current under fault conditions [17]–[19]. In [20], a FCL–DVR is proposed by combining various topologies. In the fault condition, the controller deactivates the converter in faulty phase and activates the dc-link semiconductor switches, therefore, an equivalent bridge-type current limiter will be established to restrict the fault current [20]–[21].

In [8], the voltage sag in the presence of superconducting FCL (SFCL) is investigated. The superconductor based FCLs have a low or no power loss during normal and fault conditions, so they are attractive in industry [26]–[27]. However, in recent years due to the high technology demands and higher costs of the superconductive materials, application of nonsuperconductor FCLs is recommended [1], [9]. Apart from the great diversity of FCL’s structures, an effective FCL should have the following characteristics:

1. Limit the fault current in the shortest possible time to prevent stability issues.
2. Exhibit low losses especially during the normal operation of power network.
3. Should have no impact on the network operation during normal operation.
4. Minimal number of elements.
5. Low price.

In this article, the proposed structure can compensate the voltage sag as well as limit the fault current effectively while having a minimum number of elements. To this end, the proposed FCL–DVR uses an active impedance and voltage injection strategy. The main features of this structure are as follows:

1. The simplicity of the power circuit topology.
2. Fewer numbers of elements compared with most of the existing structures of FCL–DVR, which reduces the construction costs. Because of the necessity of FCL for effectively limit the fault current and given the widespread use of the FCL in power system, this feature is one of the major contributions of the proposed structure. In addition, it should be noted that based on field experience, power switches are the most vulnerable components in the power electronics systems [28]–[30]. Therefore, the proposed FCL–DVR would be a promising topology from the reliability point of view.
3. In addition to limiting the fault current, the proposed structure can also improve voltage quality by compensation of voltage sag like a general DVR. The fault location is at PCC and FCL–DVR is supposed to control the voltage at the point of common coupling (PCC).

II. PROPOSED FCL-DVR

Generally, due to the configuration of both FCLs and DVRs, they can only perform a singular function, that is either limiting the fault current or compensating the voltage sags, respectively. A structure which can perform both functions would be very attractive to the industry because it will have the ability to protect sensitive loads from utility’s most common voltage quality problem such as voltage sags, while at the same time protecting the utility electrical installations from damaging fault currents. This will make it possible to avoid catastrophic shutdowns due to breakdown of power switches caused by high fault currents. The proposed structure considers both abovementioned features. Based on Table I, the number of elements used in the proposed structure has decreased. Furthermore, the implementation of the proposed structure is much simpler compared to structures used in [31] and [32]. The proposed FCL–DVR is shown in Fig. 1. By comparing the proposed structure with that presented in [31], it is shown that using only two IGBTs a simpler structure is realized in this article, that can both limit the fault current and...
compensate the voltage sag. The circuit configuration of this FCL-DVR consists of a transformer, two IGBTs, two reverse diodes, and a dc voltage source. Generally, the dc energy source of DVR is selected based on the design and manufacturer of the DVR. Since DVR is for injecting only for a short time, dc capacitors and batteries drawn from the line through a rectifier are frequently used. However, other dc power sources that can be used are supercapacitors, superconducting magnetic storage units, and flywheels. In this case, the $V_{dc}$ of test setup is provided from a 10 V dc power supply. The transformer is used for magnetic coupling between the main line and the control circuit or FCL-DVR [33], [34]. The primary side of the transformer is placed in series with the main line. Transformer turn ratios would be adjusted based on the voltage and current stresses on the elements on the secondary side of the transformer and voltage sag that may occur in the system. The capacitor $C_1$ is used as an output filter. Inductor $L_m$ is used as the magnetizing inductance of the transformer and it is considered as the current limiting element in a limiting mode. DC voltage source is used to compensate the voltage of the load side. It should be noted that during voltage restoration function, transformer can experience more flux-linkage two times higher than normal condition. Therefore, in order to avoid transformer saturation, the rating flux should be double that of the steady-state limit. The circuit has three modes of operation as follows:

1) normal mode,
2) voltage sag compensation mode,
3) fault current limiting mode.

The abovementioned modes of operation are explained in following parts.

**A. Normal Mode**

In this mode, the system operates without any problem, and the FCL-DVR bears no effect on the operation of the system.

**B. Voltage Compensation Mode**

The equivalent circuit of this mode is shown in Fig. 2. In the normal operation that voltage compensation is not needed, two switches $S_1$ and $S_2$ are ON, and the dc source is ineffective.

Fig. 2. Equivalent circuit of network in the compensation mode.

The circuit has three modes of operation as follows:

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\begin{center}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline
Reference & Number of transformers & Number of switches in 3 phases & Number of DC sources in 3 phases & Power losses in 1 phase mode & Compensation voltage sag & Limiting current ability \\
\hline
[1] & 2 & 1 & 0 & $P_{loss} = \left( i_{f1}R_{f1} + i_{f2}R_{f2} \right) i_{f1} + \left( 2V_{dc} + V_{sh} + r_f I_f \right) I_f$ & NO & YES \\
\hline
[23] & 1 & 1 & 1 & $P_{loss} = \left( i_{f1}R_{f1} + i_{f2}R_{f2} \right) i_{f1} + \left( \sqrt{2}I_L + 2V_{dc} + V_{sh} \right) I_f$ & NO & YES \\
\hline
[24] & 1 & 6 & 0 & $P_{loss} = P_{core} + R_{f1} i_{f1}^2 + R_{f2} i_{f2}^2 + V_{sh} i_{f1} i_{f2}$ & NO & YES \\
\hline
[22] & 2 & 24 & 3 & $P_{loss} = P_{core} + R_{f1} i_{f1}^2 + R_{f2} i_{f2}^2 + V_{sh} i_{f1} i_{f2}$ & YES & YES \\
\hline
[9] & 2 & 10 & 0 & N/A & YES & YES \\
\hline
The proposed structure & 1 & 6 & 3 & $P_{loss} = P_{core} + R_{f1} i_{f1}^2 + R_{f2} i_{f2}^2 + V_{sh} i_{f1} i_{f2}$ & YES & YES \\
\hline
\end{tabular}
\end{center}
```
inverter and create $U_{\text{comp}}$ at the primary side of the transformer and thus compensate the voltage sag. Therefore, the power quality improves.

C. Fault Current Limiting Mode

When a fault occurs in the network, this mode commences operation. In this mode, turn-off commands are sent to the switches $S_1$ and $S_2$ by the control circuit. Therefore, fault current will pass through $L_m$ and the fault current will be limited. Hence, the fault current is limited by $L_m$. Therefore, contrary to other structures, the fault current has been limited and voltage compensation is performed at once.

III. THEORETICAL ANALYSIS

A. Circuit Analysis

In this section, operation modes of circuit during normal and faulty condition will be discussed. In the first mode, when the network is in a normal state, the switches $S_1$ and $S_2$ are ON. Therefore, the FCL-DVR has no effects on the grid voltage and current. The effect of $C_1$ is negligible since operating frequency is 50 Hz. The equivalent circuit of this mode is shown in Fig. 3. The circuit equation for this mode is

$$V_m \sin \omega t = (L_t + L_l + L_r) \frac{di_L}{dt} + (R_t + R_l) i_L. \quad (1)$$

Solving (1), the line current is obtained as

$$i_L = \frac{V_m}{Z} \sin (\omega t - \varphi) \quad (2)$$

where

$$Z = \sqrt{R_{\text{total}}^2 + \omega^2 L_{\text{total}}^2} \quad (3)$$

$$\varphi = \tan^{-1} \frac{\omega L_{\text{total}}}{R_{\text{total}}} \quad (4)$$

$$R_{\text{total}} = R_S + R_l \quad (5)$$

$$L_{\text{total}} = L_t + L_l + L_r. \quad (6)$$

In the second mode, when a fault occurs, the current will start to increase. In order to limit the current, the switches $S_1$ and $S_2$ should be turned off. The equivalent circuit of the fault mode is shown in Fig. 4. The line current equation in fault mode is

$$V_m \sin \omega t = (L_t + L_l + L_m) \frac{di_L}{dt} + (R_t + R_l) i_L. \quad (7)$$

B. Voltage Sag

The fault current will cause synchronous disturbance in the network and insulation damage and it will create a voltage sag in PCC. The equivalent circuit of the system during the normal operation is shown in Fig. 5. From Fig. 5, the voltage at PCC can be written as

$$V_{PCCN} = |V_S| \left| \frac{Z_L}{Z_L + Z_S + Z_T} \right|. \quad (10)$$

In (10), $Z_L$ is the total line impedance and load impedance. The $Z_S$ and $Z_T$ are impedances of the source and transformer leakage inductance, respectively. Now, if a fault occurs, based on the equivalent circuit of the system shown in Fig. 6, the equation of PCC voltage at fault mode can be written as

$$V_{PCCF} = |V_S| \left| \frac{Z_{\text{Line}} + Z_{FCL}}{Z_{\text{Line}} + Z_{S} + Z_{T} + Z_{FCL}} \right|. \quad (11)$$

Since $|Z_L| >> |Z_{FCL}|$, PCC voltage at normal mode, $V_{PCCN}$ is greater than the voltage at fault mode $V_{PCCF}$. As $V_{PCCN} >
a voltage sag is created in PCC. This voltage sag can be higher if the fault current is not limited. In this case, \(| Z_{FCL} |\) is almost zero in (11) and \(| V_{PCC} |\) decreases significantly. It necessitates the use of DVR along with the FCL. The proposed structure, which limits the fault current also compensate the voltage sag.

C. Voltage Stress of Switch

To quantify the rating of switches associated with each of the compared FCL-DVR, total voltage rating of the switches (TVRS) is considered that can be a good measure to compare the economic justification of proposed FCL-DVR. The voltage stress of switches is calculated in two modes.

1) Fault Current Mode: In the faulty mode, the switches \(S_1\) and \(S_2\) endures approximately the same voltage stress, and the voltage stress is defined by the following equation:

\[
V_{\text{Stress}} = V_{\text{max}}. \tag{12}
\]

The voltage across inductor \(L_m\) in the normal mode is zero and when the fault occurs, the switches are turned \(\text{OFF}\) and the voltage on \(L_m\) can be written from Fig. 4

\[
V_{Lm} = V_s - V_{Lr}. \tag{13}
\]

The line current and voltage in normal operation mode are

\[
I_S = I_m \sin(\omega t) \tag{14}
\]

\[
V_S = V_m \sin(\omega t). \tag{15}
\]

When the fault occurs, the switches have high voltage stress so the voltage stresses are obtained as follows:

\[
V_{S1\text{max}} = V_{S2\text{max}} = \frac{V_{Lm}}{a} \tag{16}
\]

\[
V_{Lm} = V_s - V_{Lr} \tag{17}
\]

\[
V_{S1\text{max}} = V_{S2\text{max}} = \frac{\alpha V_m}{a} + V_{DC}. \tag{18}
\]

The voltage stress in the half-negative period is

\[
V_{S1\text{max}} = V_{S2\text{max}} = -\frac{\alpha V_m}{a} + V_{DC}. \tag{19}
\]

Since the magnitude of \(V_{sl\text{max}}\) is positive, the fault current cannot pass through the reverse biased diodes. According to the fact that \(L_m \gg L_r, V_{Lr}\) can be neglected. Turns ratio of transformer is derived as

\[
V_{Sag} = \lambda V_{Line} \tag{20}
\]

\[
U_{\text{Comp}} \approx V_{Sag} \tag{21}
\]

\[
U_{\text{Comp}} = aV_{ac,\text{inv}} \tag{22}
\]

\[
a = \frac{\lambda V_{Line}}{V_{ac,\text{inv}}} \tag{23}
\]

where “\(a\)” as turns ratio of the transformer is fixed and should be considered in the primary design of FCL-DVR.

2) Compensation Mode: If necessary, the structure will increase the voltage of the transformer to compensate the voltage drop on line. It is important to note that the switches have complementary operation. The voltage stress of switches is calculated as follows:

\[
V_{S1\text{max}} = V_{S2\text{max}} = 2V_{DC}. \tag{24}
\]

In (22) and (23), \(V_{ac,\text{inv}}\) is the inverter output voltage.

D. Power Losses Calculation

In this section, the power loss of the proposed structure is calculated. The equivalent circuit of the transformer is shown in Fig 7. From Fig. 7, the power loss in normal and compensation modes are

\[
P_{\text{loss}} = P_{\text{trans}} + P_{\text{igbt}}
\]

\[
= P_{\text{core}} + P_{\text{cu}} + V_{\text{igbt}}i_{\text{Line}}^2
\]

\[
= P_{\text{fe}} + R_{T1}i_{\text{pri}}^2 + R_{T2}i_{\text{sec}}^2 + V_{\text{igbt}}i_{\text{Line}}^2. \tag{25}
\]

In faulty mode, the transformer loss is the only part of power loss which can be derived as

\[
P_{\text{loss}} = P_{\text{trans}} = P_{\text{core}} + P_{\text{cu}} = P_{\text{fe}} + R_{T1}i_{\text{pri}}^2 + R_{T2}i_{\text{sec}}^2. \tag{26}
\]

E. DC Voltage Selection

When short-circuit fault happens, the FCL-DVR will almost completely maintain the dc voltage. Since the voltage sag mainly is not high, therefore, it is not essential to produce high compensation voltage. To ensure the stability of supply voltage, the value of dc-link voltage should be higher than the secondary side peak voltage of series and shunt transformers [32]. The dc link voltage is estimated as

\[
V_{DC} \leq 0.65V_{CES}. \tag{27}
\]

F. \(L_m\) Design

During fault limiting period, \(| Z_T | \gg | Z_L + Z_s |\). Therefore, the fault current can be written as

\[
I_F = \frac{U_S}{Z_T + Z_s + Z_L} \approx \frac{U_S}{Z_T} = \frac{U_S}{\omega L_{m,\text{Max}}}. \tag{28}
\]
Also, the fault current is $\lambda$ times of the rated load current
\[ I_F = \lambda I_{L,max}. \] (29)

Therefore, $L_{m}$ can be achieved as
\[ L_{m,Max} = \frac{U_S}{\omega \lambda I_{L,max}}. \] (30)

### G. Series Transformer Design

The capacity and ratio of series transformer should be designed based on the maximum fault current limiting capacity. In (29), the fault current is defined as $\lambda$ times of the rated load current. The rated load current can be calculated as
\[ I_{L,max} = \frac{S_{Load}}{V_S}. \] (31)

The maximum fault current can be achieved based on (28)–(31) as follows:
\[ I_{F,max} = \lambda I_{L,Max} = \frac{U_S}{k^2 \omega I_L}. \] (32)

Therefore, the turn ratio of series transformer is derived as
\[ k = \frac{U_S}{\lambda I_{L,Max} \omega I_L}. \] (33)

Also, the capacity of series transformer can be achieved as
\[ S_T = \lambda I_{L,Max} U_S. \] (34)

### IV. Comparison of the Proposed FCL-DVR With Other Similar Topologies

In Table I, the proposed structure is compared with other available FCLs, DVRs, and FLC-DVRS. To this end, there are some important benchmarks which should be considered in the comparison. These benchmarks are number of transformers, number of switches, number of dc sources, power loss, and voltage sag compensation capability. To make a fair comparison, it is assumed that all structures are considered in three-phase operational mode.

From Table I, the proposed structure has a smaller number of elements and least power loss. It should be noted that there is some configuration without voltage compensation capability with lower number of switches. However, among structures with both sag voltage compensation and current limiting capability, the proposed structure has the lowest number of active switches.

Another important benchmark is the number of transformers in the FCL. This is mainly because of transformer limitations during fault and their high price. The proposed structure needs only one transformer for operation.

The power loss of different structures is derived and given in Table I. As expected, the proposed FCL–DVR has lower loss in comparison with other structures. This is mainly because of lower number of components in the circuit. The structures in [9] and [22] have both the above-mentioned capabilities. However, they have more loss and number of elements than the proposed structure.

![Fig. 8. Simulation waveforms of load current during fault and voltage sag compensation modes.](image)
based on the time of fault occurrence, it can experience positive or negative peak current.

B. Voltage Sag Compensation

According to Figs. 8–11, between 100 and 200 ms that voltage sag has been created and the voltage is reduced by about 28%. It can be seen, by proper control circuit, the required voltage is created to compensation and $V_{\text{Load}}$ remains almost unchanged. The total harmonic distortion of source voltage with and without voltage sag compensation are shown in Figs. 12–13, respectively. It is clear cut that the unwanted harmonics in PCC voltage is reduced considerably.

VI. EXPERIMENTAL RESULTS

The proposed structure was developed to prove the feasibility and operation of the circuit. The supply voltage is set to be 63 V, the ratio of the transformer is 1:5, and capacitor filter is $20 \mu F$. The circuit parameters and manufacturer numbers of the components are given in Table III. In this experiment, BUP314 IGBTs are used. Also, the microcontroller in this setup is based on ARM Cortex-M4 core. The $V_{\text{dc}}$ of test setup is provided from a 10 V dc power supply. The laboratory testbed for the FLC-DVR is as shown in Fig. 14. Because of limitation of elements in the laboratory, the power rating of the experimental is lower than simulation and listed in Table III.

It should be noted that the simulation results are presented based on the values in real applications to provide more insights. However, due to the experimental limitations in the lab, the setup is tested at low power range. It is shown that the trajectory of result in both simulation and experiment are confirming each other.
The second event is short-circuit between 0.25S and 0.35S. In Fig. 15(c), after fault occurrence, the fault current limitation strategy is performed to compensate sag voltage. As it can be seen, the proposed structure not only compensates voltage sag but also can limit fault current. In this test setup, the difference between input and output power is about 5%, which shows decent efficiency of proposed FCL–DVR. This is mainly because of lower number of active switches during normal operation.

VII. CONCLUSION

In this article, a new fault current limiter–DVR with reduced number of switches is proposed. The proposed structure has been analyzed and operational modes are explained. The proposed structure utilizes fewer elements in comparison with the structures presented before for fault current limiter-DVR. This issue directly has effect on cost as the most important factor in industry. On other hand, switches have considerable losses while they have been switching. Hence, the power losses have been reduced. Therefore, the efficiency of the proposed circuit is better in comparison to presented FCL–DVR structures in the literature. This claim was verified by theoretically and experimentally. Furthermore, the proposed FCL–DVR not only limits the fault current but also completely compensates the voltage sag and improves power quality simultaneously. The simulation results and experimental results can prove the feasibility of structure in limiting the fault current and improving the voltage quality by compensation for utility voltage sag.

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