Encrypted Operator Computing: an alternative to Fully Homomorphic Encryption

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We introduce a new approach to computation on encrypted data – Encrypted Operator Computing (EOC) – as an alternative to Fully Homomorphic Encryption (FHE). EOC can be viewed as a reversible computation performed in a transformed (encrypted) frame of reference on transformed (encrypted) data, with both the transformation and the data, as well as the function to be computed, hidden from adversaries. Encryption is implemented via a fast-scrambling two-stage cipher based on shallow random reversible circuits of long-ranged 3-bit gates, organized in a hierarchical tree structure [1]. The special feature of this cipher, essential in establishing the polynomial overhead of EOC, is that it implements permutations, which cannot be distinguished from random via polynomial attacks, with as few as $O(n \log n)$ gates. Encrypted functions are expressed as a concatenation of a polynomial number of “chips”, $n$-input/$n$-output reversible functions, the outputs of which are expressed as ordered Binary Decision Diagrams (OBDDs). OBDDs are normal forms that only expose the functionality of the chip but hide its precise circuit implementation. The $O(\log n)$ depth of the cipher allows us to prove analytically that the output OBDDs are polynomial in size, establishing individual chips as examples of Best Possible Obfuscators introduced by Goldwasser and Rothblum [2]. To extend single-chip security to the concatenation of chips we ad random pairs of NOT gates, which are split apart and distributed across the system, for each recursive step in our construction. This randomization process, which is amplified by the nonlinearity of the cipher, scrambles the functionality of individual chips but preserves that of the whole circuit, thus enhancing the security of the full computation beyond that conferred by Best Possible Obfuscation of individual chips. While the paper focuses on symmetric encryption, we also present a generalization to public–private encryption.

I. INTRODUCTION

Addressing privacy is perhaps the biggest challenge in manipulating and extracting information from data. Even if state-of-the-art computational tools, such as machine learning, have the potential to transform some areas of medical research, privacy concerns limit access to patient data and greatly impede the discovery process. Similarly, sharing cross-border information could significantly reduce financial crime (e.g., money laundering), an effort currently impeded by local, national and regional regulations that limit the sharing of personally identifiable information. As a result, a Holy Grail of cryptography is the development of techniques capable of carrying out computations directly on encrypted data. Over the past five decades, computer scientists have made progress in accomplishing this task via homomorphic encryption [3], a scheme in which operations, such as addition and multiplication, commute with encryption.

To date, the most promising encryption schemes that have this homomorphic property for both addition and multiplication [4] are based on lattice problems [3], and require the addition of noise to the data. This type of approach is referred to as Somewhat Homomorphic Encryption (SWHE). The main issue with SWHE is that the noise is amplified with multiple homomorphic encryption operations, and reaches a threshold (the “noise budget”) beyond which one can no longer correctly decrypt the results. The breakthrough in addressing this challenge is due to Gentry [6], who, in 2009, showed that fully-homomorphic encryption (FHE) could be obtained by a bootstrapping process that refreshes the encryption, thereby reducing the noise, by evaluating homomorphically the decryption and subsequent re-encryption of the data. This operation requires passing a copy of the secret key, itself encrypted using the private key, to the evaluator.

Enormous effort has been directed towards building libraries that implement both SWHE and FHE schemes [7–12]. Advances have also been made in devising schemes for approximate arithmetic [13] that allow for computations of, for example, the multiplicative inverse and logistic functions. However, there are still severe limits to the practicality of these methods, which remain applicable to low-precision and low-depth computations. For instance, a division of two 64-bit precision numbers is simply prohibitive, let alone other common operations like trigonometric functions, square root, etc.

Here we present a different paradigm that we refer to as Encrypted Operator Computing (EOC), in which operations are carried out on encrypted data via an encrypted
program based on reversible computation \[^{1}\], without any addition of noise to the data. Reversible logic allows us to formulate computation on encrypted data in terms of operators (gates) in a transformed frame acting on transformed state vectors (data). The change of frame hides information about both the operators (the program) and the state (the data).

In order to make the above notions concrete, we first introduce the principal actor of EOC, the block cipher \(E\): a random permutation implemented as a reversible computation that maps a plaintext \(x \in \{0,1\}^n\) to a ciphertext \(E(x) \in \{0,1\}^n\), with the inverse of \(E\), \(E^{-1}\), defining the decryption function. (An asymmetric encryption extension is enabled by a choice of probabilistic encryption in combination with the access to addition and multiplication operations on encrypted data, as presented below.) Henceforth, we use a quantum-physics-inspired notation in which we represent a permutation \(E\) acting on a binary string \(x \in \{0,1\}^n\) as an operator \(\hat{E}\) acting on a state \(|x\rangle \equiv |x_0 x_1 \ldots x_{n-1}\rangle\):

\[
\hat{E} |x\rangle = |E(x)\rangle.
\]  

(1)

Since \(\hat{E}\) represents a permutation, it is unitary and real: \(\hat{E}^{-1} = \hat{E}^\dagger = \hat{E}^\top\). Generically, any reversible function, \(F\), is translated into an operator, \(\hat{F}\), such that \(\hat{F} |x\rangle = |F(x)\rangle\).

We proceed by defining the transformation

\[
\hat{F}^E \equiv \hat{E} \hat{F} \hat{E}^{-1},
\]  

(2)

which we refer to as conjugation of the operator \(\hat{F}\) by the operator \(\hat{E}\). This transformation can then be used to rewrite the encryption of \(F(x)\)

\[
\hat{E} |F(x)\rangle = \hat{E} \hat{F} |x\rangle
\]  

\[
= \hat{E} \hat{F} \hat{E}^{-1} \hat{E} |x\rangle = \hat{F}^E |E(x)\rangle.
\]  

(3)

Thus the operator \(\hat{F}^E\) implements computation on encrypted data, which can be thought of as computation in a unitarily-transformed basis. We stress that this approach is different from HE, in which case, for some specific function \(F\) and specific encryption scheme \(E\) (not generally implemented reversibly), \(E(F(x)) = F(E(x))\), implying that the corresponding operators commute, i.e., \(\hat{E} \hat{F} = \hat{F} \hat{E}\). By contrast, EOC applies to any reversible function \(F\) and the operators \(\hat{E}\) and \(\hat{F}\) do not commute. The key advance made in this paper is identifying a scheme to obfuscate the operators (circuits) \(\hat{F}^E\), which is enabled by two specific elements: the unitary transformation form of the conjugation operation; and a multi-stage cipher \(E\), motivated by our work on scrambling by classical circuits in Ref. \[^{1}\], which implements, via shallow circuits of depth of \(O(\log n)\), permutations that cannot be distinguished from random via polynomial attacks.

The actual implementation of EOC proceeds by (i) decomposing \(F\) as a circuit of \(M\) elementary gates (NOTs, CNOTs, and Toffoli gates), \(\hat{F} = \hat{f}_M \cdots \hat{f}_2 \hat{f}_1\); and (ii) carrying out the conjugation operation in Eq. (2) by exploiting the use of probabilistic encryption in order to eliminate one of the stages of the cipher of Ref. \[^{1}\]. Specifically, we employ a two-stage cipher, \(\hat{E} = \hat{N} \hat{L}\), where the operators \(\hat{L}\) and \(\hat{N}\) represent, respectively, a reversible circuit of \(O(\log n)\) layers of special (inflationary) linear 3-bit gates and a reversible circuit of \(O(\log n)\) layers of special (super-)nonlinear 3-bit gates. More precisely, we first conjugate \(\hat{F}\) with \(\hat{L}\), gate-by-gate:

\[
\hat{F}^E = \hat{E} \hat{f}_M \cdots \hat{f}_2 \hat{f}_1 \hat{E}^{-1}
\]  

\[
= \hat{N} \left( \hat{L} \hat{f}_M \hat{L}^{-1} \right) \cdots \left( \hat{L} \hat{f}_2 \hat{L}^{-1} \right) \left( \hat{L} \hat{f}_1 \hat{L}^{-1} \right) \hat{N}^{-1}
\]  

(4)

where each \(\hat{f}_i = \hat{L} \hat{f}_i \hat{L}^{-1} = \hat{g}_{i,1}\cdots\hat{g}_{i,2} \hat{g}_{i,1}\) is a circuit of \(Q_i\) elementary gates \(\hat{g}_{i,q}\), \(q = 1, \ldots, Q_i\), that exposes no more information than necessary to recover the chip’s functionality. For individual chips, this last step realizes the Best Possible Obfuscation via POBDDs introduced by Goldwasser

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\[^{1}\] We concentrate on reversible functions \(F\) as any function can be computed using reversible logic if one allows for the introduction of ancilla bit lines \[^{15}\], which are also included in the state vector.
and Rothblum [2]. We stress that the two-stage process outlined above only requires polynomial overhead, as it yields a polynomial number of POBDDs. This hinges on the \( O(\log n) \) depth of each of the two stages: the shallow depth ensures that the linear stage leads to a polynomial number of gates, and that the nonlinear stage produces POBDDs for each of those gates. An intuitive way to understand the polynomial scaling of our scheme is that, with a shallow cipher of depth \( O(\log n) \), an exponential growth of complexity with the number of layers only translates into a polynomial overhead (in \( n \)).

To be concrete, the complexity of the EOC is determined by the expansion factor due to the conjugation with \( L \) and the sizes of the BDDs following conjugation with \( N \). We show that the former brings an overhead factor of \( Q_i \leq n^{v_3} \) for every elementary gate \( \hat{f}_i \) of \( \hat{F} \), with \( v_3 = 3 \log_2 \frac{7}{\gamma} \approx 3.67 \), and that the latter yields at most \( n^\gamma \) nodes, with \( \gamma = \log_3 7 \approx 1.77 \), for each of the \( n \) BDDs of the chip. The overall time complexity of EOC (per gate of \( \hat{F} \)) is therefore bounded by \( n^{v_3+2} \) or \( n^{v_3+1} \) if the BDDs of a chip are evaluated in series or in parallel, respectively. The space required, as measured by the number of nodes in all BDDs, is bounded by \( n^{v_3+\gamma+1} \).

Concerning the security of the EOC scheme, since the form of each chip, namely, \( \hat{s}_{N}^{N} = N \hat{g}_{i,q} N^{-1} \), is known to an adversary, one should ask whether Best Possible is “Good Enough” in ensuring that one cannot walk back from the output BDDs and learn information essential for decryption. Below we argue that the structure of conjugation leads to erasure of information in a “dark zone”, outside of the “light cone” associated with the layer-by-layer growth of the chip footprint that is seeded by the initial gate \( \hat{g}_{i,q} \). The “dark zone” is simply invisible to the BDDs, and therefore Best Possible Obfuscation is, indeed, good enough in obfuscating individual chips.

However, the result of conjugation of the full function \( \hat{F}^E \) involves the concatenation of a large (but polynomial) number of chips. Best Possible Obfuscation cannot be applied to the full function \( \hat{F}^E \), since combining multiple chips into one would lead to exponential-size BDDs for the \( n \) output lines of the full computation. Is then Best Possible Obfuscation of individual chips sufficient to guarantee the obfuscation of a concatenation of multiple chips? Can correlations extracted from the collections of BDDs representing multiple chips be integrated so that what is erased in one chip becomes visible in another?\(^2\)

\(^2\) One may ask whether correlations among the \( n \) output BDDs for a single chip may reveal more information about the cipher than a BDD for a single output. Since for a single chip the information lost through the “dark zone” is the same for all outputs (because it is seeded by the same initial gate), this question is not as relevant as that for the case of multiple chips.

In the absence of a concrete way of addressing these questions, we take advantage of the freedom of inserting random identities in the form of random pairs of NOTs which are then distributed across the system between conjugation with consecutive layers of \( N \). Because of the injection of random pairs of NOTs between chips, construction of chips must be carried in parallel, for each layer of \( N \). This randomization process leaves the sizes of chip BDDs unchanged, but scrambles the functionality of individual chips while preserving the functionality of the concatenation of chips representing the entire function. The addition of randomness washes out correlations among chips and confers a greater level of security for the full function \( \hat{F}^E \) than provided by the Best Possible Obfuscation of individual chips.

It is the combined action of (i) the spreading gates across bitlines induced by the linear stage of conjugation; (ii) the Best Possible Obfuscation of individual chips built via conjugation by non-linear gates; and (iii) the incorporation of randomness in the non-linear stage, which scrambles the functionality of individual chips, that defines the obfuscation of \( \hat{F}^E \) in Eq. (2), the central result of our paper and the defining feature of EOC.

This paper is organized as follows. We start in Sec. II by describing one of the two critical elements of the EOC approach: a two-stage block cipher \( \hat{E} = N L \) inspired by the work in Ref. [1]. The second critical element is the unitary transformation form of the conjugation operation, explained above, which we implement for the linear (\( \hat{L} \)) and nonlinear (\( \hat{N} \)) stages of the cipher in Secs. III and IV, respectively. The security of EOC is discussed in Sec. V; and conclusions and a discussion of future directions are presented in Sec. VI. A brief introduction to reversible computing, and to conjugation rules that follow from the non-commutativity of gate operators are given in Appendix A; other relevant details are presented in Appendices B and C.

II. EOC-ENABLING CIPHER

Essential in the formulation of our EOC scheme is the existence of shallow multi-stage ciphers of depth \( O(\log n) \) that are secure to polynomial attacks [1]. In this section we use the tools and intuition built in Ref. [1] to introduce ciphers that incorporate two new elements: (i) “garbage” bits for probabilistic encryption, which are critical for computation on encrypted data; and (ii) ancilla bits, which are used to define reversible-circuit-representations of any Boolean function. As explained below, these new elements enable a shorter two-stage cipher, a simplification which points the way to lower overhead practical implementations of EOC, and also allows us to analytically extract bounds on the number and sizes of chip BDDs (ses Sec. IV A).
FIG. 1. Structure of the two-stage cipher consistent of $\log_2 n$ layers of inflationary linear reversible 3-bit gates, followed by $\log_3 n$ layers of super-nonlinear reversible 3-bit gates. The cipher acts on $n$ bitlines, of which $n_d$, $n_a$, and $n_g$ represent, respectively, data, ancillae, and garbage lines.

A. Probabilistic encryption and garbage bits

In order to implement secure computation on encrypted data one requires multiple encryptions of a given datum, a feature that can be realized, for example, by employing probabilistic encryption. To illustrate this point suppose that one possesses unique encryptions of both False and True. Given access to the XOR operation on encrypted data, one can easily determine which one of the encryptions represents which of the two Boolean values: XORing one encrypted Boolean with itself or with the other value yields False or True, respectively, thus revealing the plaintext identities of the Boolean values. If instead there are exponentially many encryptions of both False and True and XORing any of those covers uniformly the allowed (exponential many) possibilities, one can no longer use the trivial attack presented above to distinguish the Boolean states in polynomial time.

Allocating $n_g$ inputs of the $n$-bit register of the block cipher to “garbage” bits, each chosen randomly as 0 or 1, enables one-to-exponentially-many encryptions for any datum. The rest of the register is divided into $n_d$ bits of data and $n_a$ ancilla bits, the latter of which are all set to 0 initially and returned to 0 in the output of any reversible computation. Fig. 1 illustrates the $n$-bit register architecture implied above. Within this scheme, there are $2^{n_g}$ encryptions of each of the possible $2^{n_d}$ choices of data.

As illustrated in Fig. 1 and already implied above, the implementation of EOC described in the current paper is based on a two-stage cipher, the behavior of which we analyze on the basis of the detailed understanding gained in Ref. [1]. More specifically, the injection of randomness through the presence of $n_g$ garbage bits on the input side diminishes the effectiveness of plaintext attacks, quantified in Ref. [1] through out-of-time-order correlation (OTOC) functions of strings of Pauli operators, which represent plaintext/ciphertext measurements and actions (e.g., bit-flips) carried out by an adversary. The randomized bits are equivalent to initializing the evolution in the space of strings with a random superposition of macroscopic strings, of weight of order $n_g/2$. Following the analysis of Ref. [1], $\log_2 n$ layers of linear inflationary gates applied to a superposition of macroscopic initial strings leads to the exponential decay (in $n$) of correlators such as those representing the Strict Avalanche Criterium (SAC). The nonlinear stage further increases the entropy, saturating it to its equilibrium value, which includes both the extensive (in $n$) and universal $O(1)$ contributions. Equivalently, as discussed in Ref. [1], the nonlinear layers are responsible for making the output functions unlearnable via Boolean polynomial fitting. It is the presence of garbage bits in the initial state, which leads to the exponential decay of OTOCs after the first linear stage and the saturation of the entropy after the non-linear stage, that allows us to eliminate the third (linear) stage of the three-stage cipher of Ref. [1] and secures the two-stage cipher shown in Fig. 1 from polynomial plaintext attacks.

B. Ancilla bits and ciphertext attacks

While the EOC scheme does not give adversaries direct access to the output bits of the cipher, we note that the incorporation of ancillae renders the two-stage cipher secure to any polynomial number of ciphertext attacks, i.e., attacks from the output side. We can analyze the effectiveness of a ciphertext attack by considering the probability that the reverse computation, starting from a certain output, yields a valid input – one with exactly $n_a$ zeros for the ancillae. This information can be extracted from the SAC OTOC computed by traversing the circuit in Fig. 1 from right to left and using the methods of Ref. [1]. Even if initial strings are not inflated (due to the absence of a linear stage on the output end of the $n$-bit cipher), and the string entropy is not saturated, the probability of flipping an ancilla bit reaches $1/2 - \epsilon$, where $\epsilon$ scales to zero faster than polynomial in
Therefore the probability that running the cipher in reverse leads to a valid input with all ancillae set to 0 is \((1/2 - \epsilon)^{\alpha n}\); and thus, the two-stage cipher is also exponentially secure to ciphertext attacks.

### C. Public-private encryption enabled by probabilistic encryption

We remark that the same probabilistic encryption allows us to extend EOC to asymmetric encryption, where a public key can be chosen to be any of the \(2^{n_2}\) distinct encryptions of 1. Given access to the addition and multiplication operators on encrypted data, an encryption of 1 allows for the encryption of any number. We refer to this method of public-private encryption – via the combination of probabilistic encryption and access to addition and multiplication operators on encrypted data – as "dynamical" encryption.

#### D. Multiple registers

Finally, another extension of the work presented in Ref. [1], important in the design of practical implementations of EOC, is the incorporation of multiple registers carrying multiple sets of input data. The discussion of these cases follows the formulation of the EOC scheme outlined in the introduction if one replaces the encryption and decryption operators \(\hat{E}\) and \(\hat{E}^{-1}\) with tensor products of operators acting independently on each of the registers. Specifically, two registers \(A\) and \(B\), containing data \(x_A\) and \(x_B\) are encrypted with reversible circuits \(E_A\) and \(E_B\), respectively. (We note that circuits \(E_A\) and \(E_B\) can be the same or different.) In this construction, the operator \(\hat{E}\) in Eq. (2) is replaced by the two-register operator \(\hat{E} \equiv \hat{E}_A \otimes \hat{E}_B\), with the operator \(\hat{F}\) representing the function \(F\), which acts on both \(x_A\) and \(x_B\), now bridging across the two registers, as illustrated in Fig. 2.

![Fig. 2. Conjugation of a function \(F\) (operator \(\hat{F}\)) that acts on data contained in two separate registers, \(A\) and \(B\), encrypted with encrypted with reversible circuits \(E_A\) and \(E_B\), each of which is structured as a two-stage cipher as shown in Fig. 1.](image)

Having established the properties of the two-stage cipher, we now proceed with the explicit implementation of the conjugation operations defined in Eq. (4).

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3 Within the formalism of Ref. [1], following the application of \(\ell_N = \log_2 n\) layers of nonlinear gates, a weight 1 string increases to \(\sim \ell^2 N = n^\alpha\), with \(\alpha = \log_2 r\) (with \(0 < \alpha < 1\), since \(1 < r < 3\)), corresponding to a string density \(\rho \sim n^{\alpha - 1}\). The square of the SAC OTOC, past the \(\ell_L = \log_2 n\) linear layers, then scales as \(q \sim (1 - 2\rho)^{\ell_L} \sim e^{-2\rho n^\alpha}\). Thus, the probability that an ancilla bit is flipped reaches \(1/2\) with stretched-exponential corrections.

### III. Conjugation by Linear Gates

The conjugations with \(\ell\) layers of linear inflationary gates are implemented gate-by-gate. Conjugation by a single inflationary gate involves interchanging gates according to commutation rules derived from circuit equivalences (which we refer to as "collisions") and then applying simplifications that follow from operator identities derived via simple Boolean algebra. Appendix A presents a self-contained discussion of collision and simplification rules that allow us to derive the rules for conjugation of elementary gates (NOT, CNOT, or Toffoli) with each of the linear inflationary gates of the linear stage of the cipher, \(L\).

As an illustration, Fig. 3 shows the conjugation of a gate with a control bit overlapping with one of the three bitlines of the inflationary gate and its inverse, which are both broken up into CNOTs of both polarities. The dashed line indicates that other possible control and the target bitline of the gate to be conjugated lie outside of the three bitlines of the inflationary gate and its inverse. By alternating between collision and simplification rules in Appendix A and one arrives at the two gates in Fig. 3; the controls of both of these gates touch bitlines different from that touched by the control of the original gate. These two gates commute since their other controls and target (those attached to the dashed lines) act identically on the same bitlines.

Following the procedure illustrated above, we derive the set of rules describing conjugation by all types of inflationary gates and all possible overlap configurations of their bits with the target and controls of the gate being conjugated. These rules are presented in Appendix B and Figures B.2, B.3, B.4, and B.5 summarize the rules for conjugating NOTs, CNOTs, and Toffoli gates. (The
FIG. 3. An example of conjugation of a controlled gate by an inflationary gate depicted as the dashed box containing CNOTs (see Appendix B for the decomposition of the 144 inflationary gates in terms of CNOTs). In the case shown, a control bit of the gate being conjugated overlaps with one of the 3 bitlines of the inflationary gate. The equivalent circuit is obtained through a sequence of substitutions according to the collision and simplification rules in Appendices A1 and A2. Notice that, as a result of conjugation, memory of the control bit (overlapping with the inflationary gate) of the original (“mother” gate) is lost and two bitlines acquire controls associated with two offspring gates. The example worked out explicitly in Fig. 3 above corresponds to case C4 of Fig. B.2. These rules are not exhaustive: for nearly every case there is a plurality of other equivalent but different configurations of offspring gates. For instance, one can flip polarities of controls using the polarity mutation rules of Appendix A2.

The conjugation through multiple layers of inflationary gates, which follows from the recursive application of the conjugation rules from Figs. B.2–B.5 should be viewed as a branching process, with controls and targets scattering and touching an increasing number of bitlines as more layers of inflationary gates are deployed. This process increases the number of gates, but each of these gates has no more controls than the original gate, a consequence of the linearity of inflationary gates. The growth in the number of gates and the scattering of targets and controls across all bitlines of the circuits leads to ambiguity and loss of information about the specific gate $\hat{f}_i$ that is being conjugated. The example of Fig. 3 already illustrates the mechanism for this behavior: one original gate splits into two offsprings, with their respective controls scattering elsewhere.

The most effective mechanism for the loss of information on the location of the gate being conjugated comes from the fact that, once the hierarchical assignment of triplets of bits entering the gates of the cipher of Ref. 11 are made, the bitlines are randomly permuted. The permutation, $\pi$, and its inverse, $\pi^{-1}$, appear on the input side of $E$ and on the output side of $E^{-1}$, respectively. The action of conjugating a NOT, CNOT, or Toffoli by the permutation $\pi$ shuffles the bitlines, and the memory of the initial position of the target and controls is lost. Below we focus on the number of gates that are generated through the conjugation of a NOT, a CNOT, or a Toffoli gate by inflationary gates.

A. Initial NOT gate

The conjugations in cases A1-A3, B1-A3, C1-C3, and D1-D3 in Fig. B.2(a) increase the number of NOTs, and (b) scatter their positions across bitlines. Notice that once multiple NOTs occupy the same bitline they can be simplified using that NOT $2^i = 1$, i.e., only the parity of the number of NOTs is important. The problem of computing the average density of NOT gates on each bitline after $\ell$ linear layers of conjugation is analogous to the problem of the evolution of an initial weight 1 string into a macroscopic string, carried out in detail in Ref. 11. We point the reader to the results of that work, which concludes that after the $\log_2 n$ layers of inflationary gates one reaches an equilibrium string density equal to $1/2$, which corresponds to a random distribution of NOTs across all bitlines.

We remark that the initial growth of the number of gates follows the scaling law $\sim (7/3)^\ell$, before the pairwise simplification of the NOTs on the same bitline is taken into account. This rate simply follows from the observation that, depending on the bitline position of the NOT relative to the inflationary gate [see cases A1-A3, B1-A3, C1-C3, and D1-D3 in Fig. B.2(a)], there results 2 NOTs in 2/3 of cases and 3 NOTs in 1/3 of them; hence the average 7/3.
B. Initial CNOT gate

The analysis for the scatterings that result from the conjugation of an initial CNOT gate with linear inflationary layers mirrors that given above for the NOT gate. Conjugation leads to scattering of both the control and target of the gate. When the control and target bitlines overlap with two different inflationary gates, as for instance in cases A4 and A1 of Fig. B.2, respectively, they scatter independently. In that case, the separate analysis for control and target closely parallels that for NOT gates. The new element in the analysis comes from processes such as the one depicted in case A7 of Fig. B.3 in which both the control and target bitlines overlap with a single inflationary gate.

In the large $n$ limit, the processes in which the target and control scatter independently dominate, and one can thus estimate the number of CNOTs resulting from the conjugation with $\ell$ layers of inflationary gates as $N_{g} \sim (7/3)^{2\ell}$. In this estimation, controls and targets contribute a factor of $(7/3)^{\ell}$ each, as a result of their scatterings occurring independently. It is important to note that all scattering processes where control and target are scattered by the same inflationary gate (e.g., that in case A9 of Fig. B.3) lead to a slower increase in the number of gates than when they are scattered independently. More precisely, all these processes yield at most $4 < (7/3)^2$ gates per conjugation. Therefore, the approximate result derived from the “independent bitline approximation” above, in fact, provides an exact upper bound,

$$N_{g}^{\text{CNOT}} \leq \left(\frac{7}{3}\right)^{2\ell}. \quad (6)$$

C. Initial Toffoli gate

The analysis for an initial Toffoli gate parallels those for NOTs and CNOTs. In particular, the independent bitline approximation leads to the scaling $N_{g} \sim (7/3)^{3\ell}$, which, for the same reasons expressed for the case of the CNOT conjugations, provides an exact upper bound,

$$N_{g}^{\text{Toffoli}} \leq \left(\frac{7}{3}\right)^{3\ell}. \quad (7)$$

In closing the discussion of conjugation by linear gates, we summarize its main results, namely that (a) memory of the initial elementary gate (NOT, CNOT, or Toffoli) is lost; and (b) the upper bound for the expansion factor for the number of gates of the conjugated circuit is $n^{\nu k}$, with $\nu_k = k \log_2(7/3)$, with $k = 1, 2, 3$ for an initial NOT, CNOT, and Toffoli gate, respectively. The end result of conjugation by the linear stage of the cipher $\hat{L}$ will serve as the input into the second stage of conjugation, implemented by layers of non-linear gates in $\hat{N}$, as described next.

IV. CONJUGATION BY NONLINEAR GATES

Each of the elementary gates (NOTs, CNOTs, and Toffoli’s) of the circuit resulting from conjugation with the linear stage $\hat{L}$ of the cipher is then conjugated with the remaining, nonlinear part $\hat{N}$ of the cipher, according to Eq. (5). We cast the reversible circuit resulting from the conjugation by nonlinear gates as a collection of chips, $\hat{\mathcal{g}}_{i,q}^{\hat{N}} = \hat{\mathcal{g}}_{i,q} \hat{N}^{-1}$, defined in detail below.

A chip implements a reversible computation on an $n$-bit register represented by the reversible function $h(x)$, where $x$ is an $n$-bit input and $h(x)$ is the $n$-bit output. The binary function $h_i(x)$ encodes the $i$-th output bit of $h(x)$, and such function can be encoded as a BDD. The function $h_i(x)$ may not depend on all the $n$ input bits, but instead its domain is a subset $b[h_i]$ of those inputs; we denote as the width of the $i$-th BDD the cardinality, $|b[h_i]|$, of that set. The footprint $b[h]$ of the chip $h$ is the union $b[h] \equiv b[h_0] \cup b[h_1] \cup \cdots \cup b[h_{n-1}]$, and the width of the chip the cardinality $|b[h]|$.

Let us consider the conjugation of the chip $h$ by a 3-bit nonlinear gate $g$, starting with the BDD representation of the Boolean functions $h_i(x), i = 0, \ldots, n - 1$. Our aim is to obtain the BDD representation of the Boolean functions $h_i^g(x), i = 0, \ldots, n - 1$, where $h_i^g(x) = g(h(x)^{-1})$ is the result of the conjugation of $h$ by $g$. The gates $g, g^{-1} \in S_8$ act on three bits labeled by $j_1 < j_2 < j_3$, and their action can be expressed as three Boolean output functions, $g_{j_1}, g_{j_2}, g_{j_3}$ and $g_{j_1}^{-1}, g_{j_2}^{-1}, g_{j_3}^{-1}$. The Boolean expression for $h_i^g(x)$ are constructed in two steps:
Starting with BDDs expressing the \( h_i \), \( i = 0, \ldots, n - 1 \), one constructs the BDDs for the \( \tilde{h}_i \), \( i = 0, \ldots, n - 1 \) of step 1 by using the composition rules for BDD manipulation \cite{15}, and from those one proceeds to construct the BDDs for the \( h_i^g, i = 0, \ldots, n - 1 \) using the apply rules \cite{15}.

These operations of gate conjugation through BDD manipulation are carried out for all gates in a layer of nonlinear gates. The procedure is then iterated for all layers of the nonlinear circuit \( \hat{N} \). At the end of the process, we have a reversible operator encoded as a vector of (at most \( n \)) BDDs – the chip. The footprint of the chip grows with the number of layers of conjugation, and so do the sizes of the BDDs, i.e., the number of terminal and non-terminal nodes of the BDDs contained in the chip. The size of the chip is defined as the size of the largest BDD in the chip. (We remark that the sizes of BDDs depend on the variable order, and we choose to work with different variable orders for each of the BDDs associated with different output bits in order to reduce the BDD sizes.) Below we study the growth of the footprint and size of the chips with the number of layers of conjugation via \( \hat{N} \). We consider the fully-packed tree-structured \( \hat{N} \) described in Ref. [1], which allows us to show analytically that, for \( \log n \) layers of nonlinear gates, the size of the BDDs scale polynomially in \( n \).

### A. Scaling of the size of BDDs

For simplicity, we consider the case of an initial NOT gate, and then use these results in the generalization to CNOT and Toffoli gates in Sec. [IV B]. Suppose the NOT gate acts on bitline \( t \). When this NOT gate is sandwiched between 3-bit gates \( g, g^{-1} \), one obtains a 3-bit permutation that acts on a triplet of bits \( (\pi(i_0), \pi(i_1), \pi(i_2)) \), where \( i_{z_0} \) is obtained from \( i = \pi^{-1}(t) \) according to the tree structure, described in Ref. [1], by replacing its least significant trit by \( z_0 = 0, 1, 2 \) (notice that one of \( i_0, i_1, i_2 \) must be equal to \( i \)). Each of the three output bits is a Boolean function represented by a BDD of footprint \( x_{\pi(i_0)}, x_{\pi(i_1)} \) and \( x_{\pi(i_2)} \), of width 3. Upon conjugating with the second layer, the width of the chip increases to 9, encompassing the bits \( \pi(i_{z_0z_1}), z_0, z_1 = 0, 1, 2 \), with the index \( i_{z_0z_1} \) obtained by substituting the two least significant trits of \( i \) by \( z_0 \) and \( z_1 \). Continuing along this path, after the \( \ell \)-th layer the chip will have grown to width \( 3^\ell \), encompassing bits \( \pi(i_{z_0z_1 \ldots z_{\ell-1}}), z_0, z_1, \ldots, z_{\ell-1} = 0, 1, 2 \), where \( i_{z_0z_1 \ldots z_{\ell-1}} \) are obtained by manipulating the first \( \ell \) trits of \( i \). We note that the tree-like growth of the chip described above, and illustrated in Fig. [4] ensures that every bitline covered at level \( \ell \) of the conjugation scheme is always accompanied by two freshly touched bitlines at the next level, \( \ell + 1 \).

The scaling of the size of the BDDs associated with the \( 3^\ell \) outputs of the chip after \( \ell \) layers of conjugation can also be obtained recursively. As illustrated in Fig. [5], we start with the BDD for the NOT gate, which has one non-terminal node with the variable \( x_{\pi(i)} \) and the two terminal nodes, \( \top \) and \( \bot \), using Knuth’s notation of Ref. [17] for true and false, respectively. The BDDs resulting from conjugation with the first layer, which touches the bitline \( \pi(i) \) via a single gate, \( g \), results in a chip with three outputs, \( h_{\pi(i_0)}^g h_{\pi(i_1)}^g \) and \( h_{\pi(i_2)}^g \), each encoded in a BDD with three inputs, \( x_{\pi(i_0)}, x_{\pi(i_1)} \) and \( x_{\pi(i_2)} \). These BDDs can be constructed following the prescription above. The first step is the calculation of \( h_{\pi(i)}^g \) through the substitution \( x_{\pi(i)} \leftarrow g_{\pi(i)}^{-1}(x_{\pi(i_0)}, x_{\pi(i_1)}, x_{\pi(i_2)}) \) [see Eq. (8)]. This corresponds to the replacement of the single, non-terminal node \( \pi(i) \) in Fig. [5] by the non-terminal nodes of a BDD involving three variables: the original \( x_{\pi(i)} \) and the two fresh variables that appear in the triplet with bitline \( \pi(i) \) (recall that one of \( i_0, i_1 \) or \( i_2 \) equals \( i \)). In Fig. [5] we illustrate this substitution with the worst-case scenario in which the function \( g_{\pi(i)}^{-1} \) is represented by a BDD with 7 non-terminal nodes, the maximum size BDD on three variables. We remark that the other two \( h \) functions, expressing the outputs of the two fresh bitlines involved in the triplet with \( \pi(i) \) (two of \( \pi(i_0), \pi(i_1), \pi(i_2) \)) simply equal the corresponding output bits from \( g_{\pi(i_0)}^{-1}(x_{\pi(i_0)}, x_{\pi(i_1)}, x_{\pi(i_2)}) \), as they are not affected by the original NOT gate.

The next step is to implement the calculation of
already described above, the tree structure of the cipher.

At level $\ell = 0$ the chip has a 1-bit footprint containing only $i$. At level $\ell = 1$, the footprint encompasses 3 bitlines, $i_0, i_1$ and $i_2$, which are obtained from $i$ by replacing its lowest significant trit by 0, 1, and 2, respectively. Notice that one of $i_{z_0}, z_0 = 0, 1, 2$, equals $i$ itself; the other two are fresh bitlines, aced to the footprint. At level $\ell = 2$, the chip encompasses 9 bitlines, $i_{z_0}i_1, z_0, z_1 = 0, 1, 2$, which are obtained from the 3 bitlines of the previous level by replacing the second lowest significant trit $z_1$ in each of $i_{0,1,2}$ and $i_2$ by $z_1 = 0, 1, 2$. One of the $i_{z_0}i_1, z_1 = 0, 1, 2$ equals $i_{z_0}$, while the other two values of $z_1$ correspond to the fresh bitlines added to $i$, for each of $z_0 = 0, 1, 2$. The recursion proceeds similarly for levels $\ell > 2$.

The three-gate structure of the cipher implies that each of these three gates adds two fresh variables accompanying each of the bitlines activated by the first layer. Following the first step described in Eq. (9), each of $\tilde{h}_{\pi(i_{z_0})}, z_0 = 0, 1, 2$, is implemented via the three substitutions,

$$\begin{align*}
x_{\pi(i_{0})} &\leftarrow g_{\pi(i_{0})}^{-1}(x_{\pi(i_{0})}, x_{\pi(i_{01})}, x_{\pi(i_{02})}) \\
x_{\pi(i_{1})} &\leftarrow g_{\pi(i_{1})}^{-1}(x_{\pi(i_{10})}, x_{\pi(i_{11})}, x_{\pi(i_{12})}) \\
x_{\pi(i_{2})} &\leftarrow g_{\pi(i_{2})}^{-1}(x_{\pi(i_{20})}, x_{\pi(i_{21})}, x_{\pi(i_{22})})
\end{align*}$$

(Again, notice that one of the indices $i_{z_0}i_0, i_{z_1}i_1$ or $i_{z_2}i_2$ is the same as the original $i_{z_0}$.) The substitution amounts to replacing the non-terminal nodes $\pi(i_{0}), \pi(i_{1}),$ and $\pi(i_{2})$ by small BDDs for the functions $g_{\pi(i_{0})}, g_{\pi(i_{1})},$ and $g_{\pi(i_{2})}$, respectively. Each replacement of $\pi(i_{z_0})$ by BDDs with nodes $\pi(i_{z_0}0), \pi(i_{z_0}1)$ and $\pi(i_{z_0}2), z_0 = 0, 1, 2,$ leads to an increase in the total number of nodes of the BDDs for the $h_{\pi(i_{z_0})}, z_0 = 0, 1, 2$. In the worst-case scenario, these substitutions inflate the number of nodes by a factor of 7 (the maximum number of non-terminal nodes in a BDD on three variables). It is critical to note that, as a consequence of the tree structure, this inflation happens independently for each of the three nodes $\pi(i_{z_0}), z_0 = 0, 1, 2,$ and thus, the overall increase of the BDDs for $h_{\pi(i_{z_0})}, z_0 = 0, 1, 2,$ is additive instead of multiplicative.

The three 9-variable $h_{\pi(i_{z_0})}, z_0 = 0, 1, 2$, were constructed from the $h_{\pi(i_{z_0})}$ of the previous level of conjugation, where the variable $x_{\pi(i_{z_0})}$ appears last in the
corresponding BDD. Thus, through the substitutions in Eq. (10), \( x_\pi(i_{z_0}) \), \( x_\pi(i_{z_1}) \), and \( x_\pi(i_{z_2}) \) are the last 3 variables appearing in the BDDs for \( \pi(i_{z_0}) \), \( z_0 = 0, 1, 2 \). Moreover, these \( \pi(i_{z_0}) \) are each accompanied by two \( \pi \) functions that only depend on the same 3 variables, and represent the outputs associated with the two fresh bitlines involved in the triplet with \( \pi(i_{z_0}) \). The second step which completes the conjugation with the second layer, in Eq. (9), is to build

\[
\begin{align*}
\pi'(i_{z_1}) &= g'(i_{z_1}) \pi(i_{z_0}) \pi(i_{z_2}), \\
\pi''(i_{z_1}) &= g''(i_{z_1}) \pi(i_{z_0}) \pi(i_{z_2}), \\
\pi'''(i_{z_1}) &= g'''(i_{z_1}) \pi(i_{z_0}) \pi(i_{z_2}),
\end{align*}
\]  

(11)

where \( z_1 = 0, 1, 2 \). Each of the arguments for each of the three equations above contain one of the 9-variable \( \pi(i_{z_0}) \) along with its two companion 3-variable \( \pi \)s. Because the 3 variables in the two 3-variable \( \pi \)s always appear last in the BDD for the 9-variable \( \pi \), no new nodes are required to build the BDDs for \( \pi', \pi'' \) and \( \pi''' \), in the worst-case scenario in which the substitutions involve 7 non-terminal nodes, again, the maximum for a 3-variable BDD.

Finally, in preparation for conjugation with the next layer, we order the last 3 variables of each of the \( \pi', \pi'' \) and \( \pi''' \) so that \( x_\pi(i_{z_0}) \), \( x_\pi(i_{z_1}) \), and \( x_\pi(i_{z_2}) \) appear, respectively, as the last variable of the BDDs describing \( \pi'(i_{z_1}) \), \( \pi''(i_{z_1}) \), and \( \pi'''(i_{z_1}) \), \( z_1 = 0, 1, 2 \). In other words, \( x_\pi(i_{z_0}) \), \( z_0, z_1 = 0, 1, 2 \), are placed as the last variables of the BDDs for their corresponding output bitlines, \( \pi(i_{z_0}) \), of the 9-bit chip.

These steps can be repeated for conjugation with the subsequent layers: as illustrated in Fig. 6 nodes \( \pi(i_{z_0}, \ldots, z_{\ell-1}) \) are substituted by a BDD with nodes labeled as \( \pi(i_{z_0}, \ldots, z_{\ell-1}) \), \( z_\ell = 0, 1, 2 \) that represent a function \( g_\pi^{-1}(i_{z_0}, \ldots, z_{\ell-1}) \) of three variables \( x_\pi(i_{z_0}, z_{\ell-1}) \), \( z_\ell = 0, 1, 2 \). The figure displays the worst-case scenario, in which 7 non-terminal nodes replace the original node. Note that the LO and HI branches of the substituted node \( \pi(i_{z_0}, \ldots, z_{\ell-1}) \) are replaced, respectively, by the branching lines terminating at the \( \perp \) and \( \top \) nodes of the substituted BDD. As with previous layers, the general iteration proceeds with the second step of conjugation, Eq. (9), followed by the reordering that places the input variable on each bitline as the last one in that line’s output BDD.

The above construction, based on the tree structure of the cipher, allows us to place bounds on the size of the BDDs describing the outputs of the chip, after conjugation with \( \ell \) layers. If the BDDs for each output of the chip have size bounded by \( B_{\text{max}}(\ell) \) at level \( \ell \), then at level \( \ell + 1 \) the maximum size satisfies the recursion

\[
B_{\text{max}}(\ell + 1) - 2 = 7 \left[ B_{\text{max}}(\ell) - 2 \right],
\]

(12)

which reflects the increase in the number of non-terminal nodes by a factor of at most 7. (There are always two terminal nodes, hence the subtraction of 2 on both sides.) Seeding the recursion with \( B_{\text{max}}(0) = 3 \) (the size of the BDD representing a simple NOT operation) yields

\[
B_{\text{max}}(\ell) = 7^\ell + 2.
\]

(13)

In Appendix C we present an alternative derivation of this bound that uses the linear network model of computation explained by MacMillan [19], Bryant [20], and Knuth [17].

After conjugation with all the \( \ell = \log_3 n \) layers of our cipher, the footprint of the BDD saturates, covering all of the n bitlines. For this value of \( \ell \) one reaches

\[
B_{\text{max}}(\log_3 n) = n^{\log_3 7} + 2 \sim n^{1.7712}.
\]

(14)

Adding the sizes of the BDDs for all the output bits of the chip yields its volume \( V(\ell) \), i.e., the total number of terminal and non-terminal nodes needed to represent all the outputs of the chip. For the same value of \( \ell \) that saturates the footprint, i.e., \( 3^\ell = n \), one obtains the bound on the volume,

\[
V_{\text{max}}(\log_3 n) = n \left(n^{\log_3 7} + 2 \right) \sim n^{2.7712}.
\]

(15)
The above arguments prove that chip BDDs are polynomial-sized, i.e., they are POBDDs, establishing individual chips as implementations of Best Possible Obfuscation \[2\], a result whose significance is discussed in the context of EOC security in Sec. V.

### V. EOC SECURITY

The security of the EOC scheme hinges on whether or not one can recover significant information about \( \hat{E} = NL \) and \( \hat{F} \), given access to the collection of chips that represents the encrypted function \( \hat{F} \). We address this question in two steps: the first concerns the security of a single chip in isolation, and the second the security of the entire collection of chips.

#### A. Single chip

As mentioned above, our process of building the chip via conjugation with the cipher \( \hat{E} \) implements Best Possible Obfuscation, introduced by Goldwasser and Rothblum [2]. Their paper considered a class of functions that are computable by POBDDs, and showed that normal form POBDDs are themselves the best-possible obfuscators of those functions. For that class, the best-possible obfuscator (which outputs the POBDD) is also an indistinguishability obfuscator [21]. The critical question addressed in this section is whether, in the context of a circuit built via conjugation, Best Possible Obfuscation is “Good Enough”, i.e., whether the chip POBDDs hide the nonlinear gates in \( \hat{N} \) and the initial gate being conjugated.

We proceed by considering a simple example of a small chip built via conjugation of a single NOT gate with only one layer of nonlinear gates, as depicted in Fig. 7a. The NOT gate can be viewed as a chip at level \( \ell = 0 \), and the result of conjugation is a 3-bit chip at level \( \ell = 1 \), written in operator form as \( h = \hat{\sigma} \sigma_1 \hat{\sigma}^{-1} \), where \( \sigma_1 \) is the NOT operator that flips the value of bit 1, \( x_1 \rightarrow \bar{x}_1 \). The functionality of the 3-bit chip is encoded in three BDDs, \( h_i(x_1, x_2, x_3), i = 1, 2, 3 \), describing the outputs of the gate operator \( h \). While the BDDs are unique normal forms, there are multiple ways of factoring the operator \( h \). Examples are illustrated in Fig. 7. For instance, in Fig. 7a, we inserted identities in terms of SWAP gates exchanging bit lines 1 and \( i = 2 \) or 3. In Fig. 7b, we also randomly inserted pairs of NOT gates on each of the three bit lines, and absorb them into a redefinition of the 3-bit gate and its inverse. (One may go further and introduce a random reversible 2-bit gate in \( S_4 \) and its inverse acting on bits 2 and 3, and absorb these gates onto the 3-bit gates.) These simple examples illustrate multiple factorizations of \( h \) and reflect ambiguities in its factors: the initial NOT being conjugated could have been in bitline \( i = 2, 3 \) instead of 1, and the cipher gate could have been \( \tilde{g} \) instead of \( g \), with any choice of placement of NOTs on any of the three bitlines. Meanwhile, BDDs do not distinguish particular factorizations, as they only encode the functionality of the product, \( h \).

#### B. Extension to CNOT and Toffoli gates

We start by considering a situation in which all the bitlines acted on by a CNOT or a Toffoli gate overlap with a single gate of the first layer of \( \hat{N} \). In this case, the conjugation by that gate would result in a 3-variable BDD, no different in structure from those encountered above in the context of the conjugation of the NOT gate by the first layer of \( \hat{N} \). In this case, the scaling of the BDDs following conjugation with the subsequent layers will proceed analogously, as these layers will bring fresh variables, leading to the same scaling of the BDD size with the number of layers as above. On the other hand, the case in which the bitlines acted on by the CNOT or Toffoli gate overlap with a gate in more distant layers of the conjugation process, the scaling becomes less favorable (albeit still polynomial). Instead of going through the more complex derivation of bounds in this context, we explore a simplification lended by considering a system with two registers, as discussed in Sec. [11] a configuration which, in any case, is needed if one is to operate on (e.g. add or multiply) two data values.

Let us first consider the case of a CNOT gate. When the target and control bitlines land in different registers, the line of argument follows the discussion of the NOTs above, with the same scaling of the size of the BDDs with the size of the individual registers. When the target and control act on bitlines in the same register, we can use SWAP gates to move either the control or target to the other register. In this case, we increase the number of gates to be conjugated by a factor of 3 – the original CNOT is replaced by three gates, two SWAPs and a CNOT, all bridging two registers. We thus increase the number of chips three-fold, but reduce the conjugation problem to one similar to that already encountered for NOT gates.

In the case of a Toffoli gate, regardless of the position of the bitlines on which the gate acts, one can use SWAPs to move bitlines so that two of them overlap with a gate in the first layer of \( \hat{N} \) in one register, with the third bitline located in the other register. The cost of this move is the addition of at most four SWAPs, thus increasing the number of chips by a factor of 5. Again, with this movement of bitlines via SWAPs we reduce the conjugation problem to one similar to that already considered above without changing the scaling of the size of the BDDs associated with individual chips.
FIG. 7. Equivalent factorizations of (a) $\hat{h} = \hat{g} \sigma_1^x \hat{g}^{-1}$, where $\sigma_1^x$ corresponds to a NOT gate placed on bitline 1. (b) The NOT gate can be moved, for example, to bitline 2 by absorbing SWAP gates between lines 1 and 2 into the right of $\hat{g}^{-1}$ and into the left of $\hat{g}$, yielding the factorization $\hat{h} = \hat{g}' \sigma_2^x \hat{g}^{-1}$. (c) Independent pairs of either identity or NOT gates (shown in matching colors) can be inserted and then absorbed to the left and right, respectively, into the gates $\hat{g}^{-1}$ and $\hat{g}'$ of (b), yielding the factorization $\hat{h} = \hat{g}'' \sigma_2^x \hat{g}''^{-1}$.

One can generalize the example above to chips build after arbitrary layers of conjugation. In particular, chips at level $\ell + 1$: (i) do not contain sufficient information to determine which bitlines the chip at level $\ell$ acted on; and (ii) cannot distinguish among the multiple choices of bit negations, inserted in pairs on any of the fresh bitlines (those not contained in the chip at level $\ell$). Due to these ambiguities, it is impossible, by examining only the BDDs, to reverse the hierarchical structure that determines how bits are grouped in triplets for the placement of the 3-bit gates of the cipher and the exact 3-bit gates that were deployed. Basically, information is erased (not only concealed) in the process of assembling a single chip via conjugation.

We also note that, in the course of conjugation, gates in the $\ell + 1$-th layer of $\hat{N}$ that do not touch the bits of the chip at level $\ell$ simply annihilate in pairs, and thus information on those gates is erased. Trivially, the BDDs are insensitive to these gates. The information lost has a simple interpretation in the context of operator spreading in physical systems (see, for example, Ref. [22]): it corresponds to the dark region outside of the light cone of influence that develops through the unitary evolution of an operator, in our case the initial gate being conjugated. This notion is illustrated in Fig. 8, where we depict, for simplicity, a one-dimensional ($D = 1$) version of the tree-like ($D \to \infty$) packing of 3-bit gates in each layer.

FIG. 8. Region of influence of a 1-bit NOT gate (red square in the middle) in the course of conjugation. The circuits to the left and right of the NOT gate represent $\hat{N}^{-1}$ and $\hat{N}$, respectively. For simplicity, the figure displays a one-dimensional ($D = 1$) “brickwall” arrangement of the fully packed circuit of 3-bit gates. (The description generalizes to all dimensions $D$, including the tree-like structure corresponding to $D \to \infty$.) Each 3-bit gate is depicted as a rectangle, with the horizontal (“time”) direction represents the order of the computation. The 3-bit gates depicted as dark rectangles – the collection of which defines the “dark region” – are not affected by the NOT gate in the middle and annihilate pairwise (a $g^{-1}$ from $\hat{N}^{-1}$ and a $g$ from $\hat{N}$). Thus these gates are “invisible” and do not enter in the composition of the chip. By contrast, the 3-bit gates depicted as light rectangles do contribute to the buildup of the chip and are contained within the “past” and “future” light cones (shown as light blue squares) to the left and right of the NOT, respectively.

The arguments given above reinforce the fact that, at the level of a single chip, Best Possible Obfuscation is indeed "Good Enough" in removing access to the cipher and in hiding the gate being conjugated. What is not a priori obvious is what level of security Best Possible Obfuscation of individual chips confers to the concatenation of chips representing the full function $F^E$. Can correlations extracted from the full collection of BDDs describing multiple chips reveal any details about the cipher?
B. Multiple chips: injecting randomness

Below, instead of answering this question, we obviate it by incorporating randomness, which washes out correlations among chips by scrambling the functionality of individual chips while preserving the functionality of the full computation. Below we present the construction of a new set of chips, $\hat{g}^N_{i,q,\eta}$, that incorporates randomness, the presence of which is symbolized by $\eta$. For notational simplicity we group the subscripts $i,q$ into a super index $I$, and concentrate on the construction of the chip by that label, i.e., that initiated by $\hat{g}_I$. All chips at level $\ell + 1$ are built recursively (and in parallel) from the chips at level $\ell$, according to the following three-step process: (1) randomly insert pairs of either identity operators or NOTs on internal wires connecting two level-$\ell$ chips, $I$ and $J$ (see Fig. 9a); (2) on the edges that received a pair of operators, absorb one operator into the output of the chip on the left and the other into the input of the chip on the right; and (3) proceed with conjugation by layer $\ell + 1$ of $\hat{N}$ (see Fig. 9b), in the exact same manner described in Sec. IV this time in synchrony for all gates that emerged from the linear stage of the cipher that, together, represent the full function $\hat{F}^E$.

![Figure 9: Construction of the chips that incorporate the injection of randomness.](image-url)

This process illustrated in Fig. 9 randomizes the functionality of individual chips while preserving the functionality of $\hat{F}^E$. We also stress that, in general, the NOT gates that are injected into the chips do not commute with the nonlinear gates in $\hat{N}$ and thus, the scrambling effect of the NOTs is nonlinearly amplified through the conjugation process.

Randomization induced via absorption of NOTs in the second step above is trivially reflected in the BDDs of all resulting chips. For every input of a chip that incorporates a NOT, one flips the decision branches of the corresponding nodes (with that input variable) of the BDDs, i.e., a solid branch (or true) is switched to a dashed branch (or false), and vice-versa. Similarly, for every output of the chip that incorporates a NOT, one swaps the $\top$ and $\bot$ terminal nodes. Notice that the BDD
retains its size, as no new nodes are created by the randomization process. The third step of the process, the conjugation with the next layer, proceeds exactly as before (see Sec. [IV]) and thus, the bounds on the scaling of the sizes of BDDs obtained in Sec. [V.A] remain unchanged.

Another way of evaluating the effect of the randomization process is to consider in more detail the ambiguity it adds to a chip beyond that already present in the absence of randomness (i.e., that already accounted for in our discussion of the single chip above). Recall that, in the absence of randomness, we argued that there was ambiguity in the choice of negations in 2/3 of the bitlines of the chip, corresponding to the fresh bits present in the chip at level $\ell + 1$ but absent in the chip at level $\ell$. In the presence of the added randomness, the ambiguity is extended to every bitline, including the 1/3 of the lines inherited from the chip at the previous level. The BDDs are oblivious to 2/3 of negations because they are normal forms, and scrambled by the other 1/3 of negations.

While it is difficult to quantify the amount of information that an adversary can extract about the cipher from the full collection of chips representing $F^E$, the arguments above provide a lower bound on what cannot be extracted: one cannot resolve whether bitlines are negated or not in between the layers of $N$. In other words, one cannot resolve between a layer $\hat{N}_\ell$ and another putative layer $\hat{N}_\ell = \hat{N}_\ell \hat{P}_\ell$, where $\hat{P}_\ell$ is a layer of random NOTs. There are $2^{n \log_3 n}$ possibilities for incorporating negations before all layers, so building $F^E$ increases entropy by, at the very least, $\Delta S = n \log_3 n$. It is possible that this increase in entropy is sufficient to guarantee that one cannot break the encryption. The situation parallels that of the Advanced Encryption Standard (AES), where all information about the cipher is exposed except for the bitwise XORs in the AddRoundKey iterations. In the case of AES, the negations are deterministically generated round-by-round from the key. While the parallel to AES is not a proof of security (and AES has not yet been formally proved secure either), we note that the entropy generated in EOC is superextensive in $n$, while that in AES scales linearly with the size of the key. We further note that the above estimate of the entropy is a very conservative lower bound to the information lost in assembling the chips, as it does not account for the lack of knowledge about, for example, (1) the specific gates in $S_8$ that are used, beyond the effects of negations above; and (2) the connectivity of the gates in the cipher, i.e., the triplets of bits on which each of the 3-bit gates act on.

We conclude that inserting randomness confers significantly higher security to EOC than provided by Best Possible Obfuscation of individual chips, which by itself may be sufficient to make EOC of practical use already in the absence of disorder.

VI. CONCLUSIONS AND OPEN DIRECTIONS

This paper introduces EOC as an alternative to Fully Homomorphing Encryption. Intuitively, our approach can be viewed as performing the computation of an operator (function) $\hat{F}$ in a transformed frame (defined via a unitary transformation, $F^E = \hat{F} \hat{E} \hat{E}^{-1}$) in which the transformed operator $\hat{F}^E$ (the encrypted program) acts on transformed state vectors $\hat{E} | x \rangle = | E(x) \rangle$ (the encrypted data). The touchstone of EOC is the capacity to hide both the transformation $\hat{E}$ and the program $\hat{F}$. The progress made in this paper is made possible by our previous work [1] on ciphers that are secure to polynomial attacks with as few as $O(n \log n)$ gates. As outlined above, it is the two-stage structure, $\hat{E} = \hat{N} \hat{L}$, which involves first applying $\log_3 n$ layers of linear gates drawn at random from a set of 144 special 3-bit inflationary gates, implemented by $\hat{L}$, followed by $\log_3 n$ layers of nonlinear gates in $\hat{N}$, that confers the fast scrambling property of the cipher. The encrypted operator $\hat{F}^E$ is expressed as a sequence of chips, with the $n$ outputs of each chip expressed as BDDs.

We placed exact analytical upper bounds on the growth of both the number of gates in the course of conjugation with $\hat{L}$ and on the footprint and size of BDDs during conjugation with $\hat{N}$. In particular, we showed that, after conjugation with $\log_3 n$ layers of $\hat{L}$, the number of gates increases by a factor of $n^{\gamma_3}$ for every conjugated elementary gate, with $\nu_3 = 3 \log_2 \frac{7}{3} \approx 3.67$; and, after conjugation with $\log_3 n$ layers of $\hat{N}$, each of the $n$ BDDs of the chip grow by at most a factor of $n\gamma$, with $\gamma = \log_3 7 \approx 1.77$. It thus follows that the time complexity of EOC (per conjugated gate) is bounded by $n^{\nu_3+\gamma}$ or $n^{\nu_3+\gamma+1}$ if the chip BDDs are evaluated in series or in parallel, respectively; and that storage space required, as measured by the number of nodes in all BDDs, is bounded by $n^{\nu_3+\gamma+1}$.

Having established the polynomial complexity of EOC with $n$, we turned to the question of its security. There are three contributing mechanisms to the loss of information that, taken together, determine the security of the approach. The first is based on the unitary-transformation form of conjugation (which contains both $\hat{E}$ and $\hat{E}^{-1}$), and involves complete erasure of information: gates that do not touch the footprint of the chip at a particular level of conjugation annihilate in pairs and thus, as conjugation proceeds layer by layer, gates of the cipher outside of the “light cone” are simply invisible. The second mechanism is the compression of information enabled through the representation of chip outputs as collections of polynomial-sized BDDs, which are normal forms that only expose the minimum information required to establish functionality. As discussed in the body of the paper, a BDD-based chip realizes the notion
of Best Possible Obfuscation introduced by Goldwasser and Rothblum, \cite{2} which, in turn, we argue is sufficient to ensure the security of individual chips. However, the level of security that Best Possible Obfuscation implies for the concatenation of chips representing the result of the full computation of $F^E$ is not a priori obvious. In this paper we circumvented this issue by incorporating a third (external) source of obfuscation; namely, before each level of conjugation by a nonlinear layer, we add random pairs of NOTs (identities) between chips, which are then separated and incorporated into inputs and outputs of chips connected by a given bitline. This randomization process scrambles the functionality of individual chips while preserving the functionality of the overall conjugated circuit. This injection of randomness across the system confers stronger security for the fully conjugated circuit than provided by Best Possible Obfuscation of individual chips, as it washes out correlations among chips that might have revealed revealed information on the cipher $E$ or function $F$.

We argued that, with the injection of randomness, layers of negation interspersed between layers of nonlinear gates cannot be resolved, suggesting that entropy of order $O(n \log n)$ is, at minimum, generated. How to precisely quantify the total information, either invisible (i.e., truly erased) or just obfuscated through the combination of nonlinear conjugation and random insertions, remains an open question. Future work is needed in order to develop a formal framework for quantifying the actual entropy of conjugated circuits and their associated BDDs, analogous to the statistical mechanics approach to the security of shallow log $n$-depth ciphers based on string entropy and out-of-time-ordered correlators (OTOCs) described in Ref. \cite{1}. It is appealing to speculate that the insights on random classical circuits built on the mapping to string space can be extended to the study of more general reversible circuits and their compression via BDDs.

We remark, for practical purposes, that the flexibility afforded us by the presence of garbage bits can be used to greatly decrease the overhead of implementing EOC. The significant simplification amounts to replacing the linear stage of Fig. \ref{fig:fig1} with a specially designed single layer of inflationary gates. In this case, one can deploy the conjugation scheme with the BDDs including this one linear layer (along with $\log_2 n - 1$ nonlinear layers). Correspondingly, the polynomial complexity drops by a factor of $n^{\nu_3}$. In particular the execution-time overhead becomes $n^2$ or $n^1$ if the chip BDDs are evaluated in series or in parallel, respectively.

In closing, we stress that the EOC framework – based directly on logic elements as building blocks – makes a hardware implementation natural. For example, by implementing EOC in silicon (e.g., in field programmable gate arrays – FPGAs) one could reach speeds of computation on encrypted data limited only by state-of-the-art electronics. Such a practical deployment of EOC would impact all aspects of data science for which security and privacy are essential.

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**Appendix A: Reversible logic equivalences: collisions, simplifications, and factorizations**

Any reversible circuit associated with an even permutation can be broken down into elementary NOT, CNOT, and Toffoli controlled gates (odd permutations require an additional ancilla bit). The NOT gate negates bit $j$ irrespective of all others: $x_j \rightarrow \bar{x}_j = x_j \oplus 1$. The CNOT gate negates (the “target”) bit $j$ conditional on whether another (“control”) bit $i$ is 0 or 1: $x_j \rightarrow x_j \oplus x_i$. Finally, the Toffoli gate negates (the ”target”) bit $j$ conditional on whether (“control”) bits $i_1$ and $i_2$ are both true: $x_j \rightarrow x_j \oplus x_{i_1} x_{i_2}$.

More generally, one can define controlled gates with controls over $n$ bit lines. (These gates can be broken down into smaller gates with $n < 2$ using the factorization rules below.) Consider a Boolean expression $B(x_{i_1}, \ldots, x_{i_n})$ that depends on the logic variables $x_{i_1}, \ldots, x_{i_n}$ in bit lines labeled by $i_1, \ldots, i_n$. A generic control gate should negate a target bit $j \neq i_1, \ldots, i_n$, i.e. $x_j \rightarrow \bar{x}_j$, if $B$ is True ($B = 1$), and leave $x_j$ untouched if $B$ is False ($B = 0$). In other words, a target bit, $j$, that is acted on by this gate will be modified as follows:

$$x_j \rightarrow x_j \oplus B(x_{i_1}, \ldots, x_{i_n}), \quad j \neq i_1, \ldots, i_n. \quad (A1)$$

We shall concentrate on Boolean expressions that can be expressed as a product involving either the variables $x_{ik}$ or their negation $\bar{x}_{ik}$,

$$B(x_{i_1}, \ldots, x_{i_n}) = (x_{i_1} \oplus \sigma_1) \ (x_{i_2} \oplus \sigma_2) \cdots (x_{i_n} \oplus \sigma_n), \quad (A2)$$

where the variables $\sigma_k = 0, 1$, for $k = 1, \ldots, n$, determine the polarities of the $n$ controls entering the expression for $B$: $x_k \oplus 0 = x_k$, and $x_k \oplus 1 = \bar{x}_k$. 
To describe a controlled gate, \( g \), we need the following information: the bit line corresponding to the target bit \( t(g) \) and the Boolean expression acting on the control bits, which is cast as a set \( C(g) \) of pairs with the control bits and their polarities. In the example above, \( t(g) = j \) and \( C(g) = \{(i_1, \sigma_1), \ldots, (i_n, \sigma_n)\} \). We denote by \( b(C) \) the set of only the bits \( \{i_1, \ldots, i_n\} \), and by \( |C| \) the number of control bits in \( C(g) \) (\( |C| = n \) in the example). We also refer to the target bit \( t(g) \) as the “head” of the gate and the set \( C(g) \) as its “tail”, which contains all the information on the controls, i.e., the control bits and their polarity for the controlled-Boolean expression.

The NOT, CNOT, and Toffoli gates are particular examples of controlled-Boolean gates. The NOT corresponds to a constant \( B = 1 \), which depends on no other bits \((C = \emptyset, |C| = 0)\). The CNOT has \(|C| = 1\), and corresponds to one of two possible Boolean functions, \( B = x_{i_1} \) or \( B = \overline{x}_{i_1} \), associated to positive or negative polarity controls, respectively. The Toffoli gate has \(|C| = 2\), and corresponds to one of four possible Boolean functions: \( B = x_{i_1} x_{i_2} \), \( B = \overline{x}_{i_1} x_{i_2} \), \( B = x_{i_1} \overline{x}_{i_2} \), or \( B = \overline{x}_{i_1} \overline{x}_{i_2} \) depending on the choice of polarities of the controls.

An example of a gate with \(|C| = 3\) controls is one with \( B = x_{i_1} x_{i_2} \overline{x}_{i_3} \).

Here it is useful to introduce the simplified graphical representation of a control gate illustrated in Fig. A.1. The Boolean expression representing controls (tail) is lumped into a single control box, \( X \), which can cover multiple bit lines, that are not necessarily consecutive. While we often omit control bit lines that go in and out of the control box, when particular control bits play a significant role (e.g., in collisions, see below) they are pulled out of the box and shown explicitly.

We next introduce equivalence rules for the action of multiple Boolean-controlled gates which reflect the non-commutativity of the actions of sequential gates. (Similar rules have been discussed in the context of circuit simplification, e.g., Ref. [23].) We refer to these circuit equivalences as “collision” rules, as they express the fact that interchanging the order of two non-commuting controlled gates \( \hat{g} \) and \( \hat{h} \) requires inserting “debris” gates in between. More precisely, when \( g \) and \( h \) do not commute, i.e., \( \hat{g} \hat{h} \neq \hat{h} \hat{g} \), then \( \hat{g} \hat{h} = \hat{h} D \hat{g} \), in which case the “debris” \( D = h^{-1} \hat{g} \hat{g}^{-1} \) can also be broken down in terms of controlled gates. (In the particular case when \( g \) and \( h \) commute, \( D = 1 \).)

### 1. Collision rules for controlled gates

The collision rules are illustrated graphically in Fig. A.2. The simplest examples, of commuting gates,

\[
\begin{align*}
&\begin{array}{c}
  \text{FIG. A.1. A simplified representation of a Boolean control gate.}
  \text{The target bit is marked by a \( \oplus \). The control (tail) bits are lumped into a box, here represented by \( X \). Notice that control bits inside the box can be negated (white circle) or not (black circle). The bit lines going in and out of the box are omitted.}
\end{array}
\end{align*}
\]

\( \hat{g} \) and \( \hat{h} \), are shown in Figs. A.2(a) and A.2(b). These represent cases in which (a) there is no overlap between the target bit of one gate and the control bits of the other, and vice-versa; or (b) the gates share the same target bit (coinciding heads). Hereafter we refer to these cases as no collision and head-on-head collision, respectively. A non-trivial collision occurs when the target line of one gate overlaps with control lines of the other. Clearly, in this situation the gates do not commute, and interchanging their order requires the insertion of additional "debris" gates in order to preserve the functionality of the original order. Figs. A.2(c) and A.2(d) illustrate non-trivial collisions cases, which we refer to as one-headed and two-headed collisions, respectively.

### 2. Simplification and polarity mutation rules

In addition to the collisions in Figs. A.2(c) and A.2(d), which proliferate the number of gates through the addition of debris, there are also simplifying collisions resulting in complete or partial annihilation and thus a reduction in the number of gates. For instance, as seen in Fig. A.3, two gates can annihilate each other completely, if they are identical, or combine into a single gate if they only differ by one control bit.

There are also some collisions of commuting gates where it is possible to change the polarity of the controls, from negated to non-negated and vice-versa, as illustrated in Fig. A.4.
FIG. A.2. Collision rules. (a) No-collision rule: The head of one gate does not share a bit line with any of the bits of the other gate, and vice versa. Notice that tails $X$ and $Y$ can overlap and run over some common bit lines. (b) Head-on-head collision rule: The heads share the same bit line. Notice that the tails $X$ and $Y$ can overlap. (c) One-head collision rules for four gate types and configurations: The head of one gate shares a bit line with a bit in the tail of the other gate, but not vice versa. The gates with both $X$ and $Y$ correspond to having the product $XY$ as control. The tails $X$ and $Y$ can overlap. (d) Two-head collision rules for four gate types and configurations: The head of one gate shares a bit line with a bit of the tail of the other gate, and vice versa. Again, the gates with both $X$ and $Y$ correspond to having the product $XY$ as control, and the tails $X$ and $Y$ can overlap.

FIG. A.3. Simplification rules for gates acting on the same target bit. (a) Annihilation. (b) Control bit elimination. (c) and (d) Control bit reversal.

3. Factorization rules

Finally, we can factorize a gate with tail $XY$ into products of gates with smaller tails by using the one-headed collision rules in Fig. A.2(c), as illustrated in Fig. A.5. Notice that the factorization of the tail $XY$ into $X$ and $Y$
pieces may be done in several different ways, and that there is also freedom in choosing the bit line on which an additional control is placed.

Appendix B: Rules for conjugation by inflationary gates

In this section we present the rules for conjugation of controlled gates by inflationary gates, which are depicted in Fig. B.1. There are four topologies, labelled A, B, C and D, which are used in categorizing the conjugation rules that are explained in pictures in Figs. B.2, B.3, B.4 and B.5.
FIG. B.2. Conjugation rules for six inequivalent gate configurations for each of the four classes of inflationary gates (A, B, C, and D). Each case comprises two circuits: pre- and post-conjugation (left and right, respectively). The gate being conjugated is shown with blue lines on the left circuit, surrounded by the inflationary gate block and its inverse (CNOT gates with black lines). The controls in the inflationary block gates have different colors so that their influence on the polarities of controls of offspring gates can be tracked down. The offspring gates on the right circuits have either blue lines (when they correspond to the original gate being conjugated) or red (when they are new gates). Cases A1-A3, B1-B3, C1-C3, and D1-D3 apply to the conjugation of NOT, CNOT, and Toffoli gates, while the other cases apply only to CNOT and Toffoli gates as they require at least one control bit to overlap with bitlines touched by the inflationary gates (the configurations shown in this figure correspond to having a target or a control bit outside the range of the inflationary gates; additional cases are shown in Figs. B.3 and B.4). The dashed lines indicate connections that CNOT and Toffoli gates may have to additional controls bits. In a few cases (A5, B4, B6, and C4), the polarity of the control of an offspring gate depends on the relative polarity of three controls (e.g., two from the inflationary gate and one from the gate being conjugated), with the minority polarity winning.
FIG. B.3. Conjugation rules for CNOT gates for the six configurations when both target and control fall within the range of bitlines touched by an inflationary gates. The same notation and conventions of Fig. B.2 apply here. Notice that in some cases gates from the inflationary blocks survive the conjugation. For conciseness, when a control polarity depends on polarities from multiple pre-conjugation gates, a polarity variable “x” is inserted and defined below the circuit where it is utilized. Circuits resulting from conjugations are not necessarily unique and other equivalent circuits are possible. We choose those with the smallest number of gates and which minimize the the appearance of pre-conjugation gates.
FIG. B.4. Conjugation rules for the twelve Toffoli gate configurations of classes A and B where at least two bits fall within the range of bitlines touched by an inflationary gates. The same notation and conventions of Figs. B.2 and B.3 apply here. The double contour line in some controls indicate negation of the polarity. When there are multiple options for circuits post-conjugation, a gate configuration that minimizes the presence of the original Toffoli gate or the total number offspring gates is chosen.
FIG. B.5. Similar to Fig. B.4 but for classes C and D.

Appendix C: Bound on BDD sizes using a linear network model

The scaling of the size of the BDDs associated to the $3^\ell$ outputs of the chip after $\ell$ layers of conjugation can also be obtained recursively deploying the linear network model explained in Refs. [16, 17, 19]. Here we rederive the bound in Eq. (13) using this method.

After the first layer of conjugation, the three outputs $h_{\pi(i_0)}, h_{\pi(i_1)}$ and $h_{\pi(i_2)}$ of the chip can be encoded each in a BDD with three inputs, $x_{\pi(i_0)}$, $x_{\pi(i_1)}$ and $x_{\pi(i_2)}$. We can represent the Boolean expression for each of the outputs, for instance $h_{\pi(i_0)}$, as the result from a linear network model of computation [16, 17], which is a useful representation that allows us to put bounds on the sizes of the BDDs, as we show below. Figure C.1a depicts the linear network model. Each of the modules (square boxes) takes a signal through wires, each representing a bit of information, from the module on its left and one signal from the input variables on top of the module. Any function of 3 bits can be computed by such a linear network model of computation, using 3 modules. In the worst case scenario, the linear network operates as follows: (1) the information on the first input variable is passed from the first to the second module using a single wire; (2) the information on the first two variables is passed from the second to the third module using two wires; and, finally (3) the Boolean function of 3 variables is computed by the third module with the information from the previous two modules. (We note that this computation is carried solely by moving information unidirectionally from one module to the next.)
variables $x$ in a similar fashion, we restructure the modules with input $x$ of the second, and two wires from the second to the third. These internal wires contain the additional information to the second, and two wires from the second to the third. The worst-case is depicted, in which one additional bit must be passed between the first and second modules, and two additional bits must be passed between the second and third modules.

The BDDs resulting from conjugation by the second layer can be constructed following the prescription in Sec. IV. For example, for the conjugation with the gates $(g$ and $g^{-1})$ that overlap with bit $i(x_0)$, we first obtain the BDD for $\tilde{h}(i(x_0))$ following the first step described in Eq. (8). The tree structure of the fully-packed cipher circuit implies that two fresh variables will be added, those that join $\pi(i_0)$ in the triplet of bits acted on by $g$ and $g^{-1}$. One can extend the linear network model by local restructuring of the module for which $x_\pi(i_0)$ is the input, as shown in Fig. C.1(b), breaking it into 3 modules, each with input variables $x_\pi(i_{10}z_1)$, $z_1 = 0, 1, 2$. These three variables are those corresponding to the bits in a triplet with $i(x_0)$ (one of them is $x_\pi(i_0)$ itself). This splitting of one module into three only requires the addition of wires running internally between those three modules (see Fig. C.1(b)): one wire running from the first module to the second, and two wires from the second to the third. These internal wires contain the additional information to calculate the output of $g^{-1}$ needed for the substitution of $x_\pi(i_0) \leftarrow g^{-1}_{\pi(i_0)}(x_\pi(i_{10})x_\pi(i_1)x_\pi(i_2))$, see Eq. (8). In a similar fashion, we restructure the modules with input variables $x_\pi(i_1)$ and $x_\pi(i_2)$. The result is a linear network model to compute $\tilde{h}\pi(i_0)$ given nine input variables, $x_\pi(i_{10}z_1), z_0 = 0, 1, 2$.

We remark that while $\tilde{h}\pi(i_0)$ depends on 9 variables, the $\tilde{h}$ variable associated with the other two fresh bits that form the triplet with $\pi(i_0)$ (two of $\pi(i_{00}), \pi(i_{01})$, and $\pi(i_{02})$, with the third being $\pi(i_0)$ itself) simply equals the corresponding output bits from $g^{-1}(x_\pi(i_{00}), x_\pi(i_{01}), x_\pi(i_{02}))$.

The next step is to implement the calculation of $h^g_{\pi(i_0)}(x) = g_{\pi(i_0)}(\tilde{h}_\pi(i_0), \tilde{h}_\pi(i_1), \tilde{h}_\pi(i_2))$, as prescribed in Eq. (9). If one arranges $x_\pi(i_0)$ to appear as input to the rightmost module (this can always be done for each separate output of the chip), no additional wires between the modules need to be added in order to compute $h^g_{\pi(i_0)}$ from $\tilde{h}_\pi(i_0)$.

These steps can be repeated recursively for conjugation with the subsequent layers: a module from the previous layer is broken down into three consecutive modules. In addition to the wires entering (on the left) and exiting...
The size of the BDDs can be bounded given the number of wires $a_m^{(ℓ)}$ connecting consecutive modules, labelled $m − 1$ and $m$, of the linear network [16, 17]:

$$B \leq B_{\text{max}}(ℓ) = \sum_{m=0}^{3^ℓ} 2^a_m^{(ℓ)} = \sum_{m=0}^{3^ℓ-1} 2^a_m^{(ℓ)} + 2 ,$$  \hspace{1cm} (C2)

where we used that the last module has a single output wire, $a_{3^ℓ} = 1$. Using the recursion for the number of wires

$$B_{\text{max}}(ℓ + 1) - 2 = \sum_{p=0}^{3^ℓ} 2^a_p^{(ℓ+1)} = \sum_{m=0}^{3^ℓ-1} 2^a_m^{(ℓ+1)} + 2^a_{3^ℓ+2} .$$

Seeding the recursion with $B_{\text{max}}(0) = 3$ (the size of the BDD representing a simple NOT operation) yields

$$B_{\text{max}}(ℓ) = 7^{ℓ} + 2 ,$$  \hspace{1cm} (C4)

the same result as in Eq. (13).
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