A 10-bit 0.41-mW 3-MSps R-I DAC with full-swing output voltage

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Abstract: For medical implantable devices, power consumption is the most important design consideration. This is because only medium data rate and medium resolution are required in such applications. In addition, rail-to-rail output swing is desired if power supply voltage is near 1 V. In order to achieve low power consumption with medium data rate and resolution, this paper proposes a low-power resistor-string and current-steering hybrid digital-to-analog converter (R-I DAC) with a full-swing output signal. It adopts a current-direction control which makes the output current of the current-steering block flow bi-directionally through the feedback resistor. The proposed structure can achieve full-swing output. It consumes half of the total current of the conventional single-ended current-steering DAC for the same output swing. A 10-bit full-swing R-I DAC prototype is implemented by 180-nm CMOS technology. The measured effective number of bits (ENOB) is 8.9 bits. The settling time of pulse response is 300 ns which corresponds to 3.3 MHz sampling frequency. Chip area is 0.22 mm\(^2\). For 1.25 V single power supply, the output swing is 1.024 V. The power consumption is 0.41 mW for a full-swing sinusoidal input of 40.82 kHz at a 3.125 MS/s sampling clock.

Keywords: digital-to-analog converter (DAC), high-swing, hybrid, low power

Classification: Integrated circuits

References

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1 Introduction

Portable and implantable devices powered by battery generally require chips with high-swing in/out signal and low power consumption [1]. Firstly, under low supply voltage, signal with higher swing tends to have better signal-to-noise ratio. So the anti-interference capability can be improved by increasing the signal amplitude. The supply voltage may be as low as 1.2 V. Signal with high swing means reaching or close to ground voltage and power supply voltage [2, 3]. Secondly, because the life time is a prime performance for a portable/implantable devices, low-power consumption is mandatory.

Resistor or capacitor based architecture are commonly used to implement low-power digital-to-analog converters (DACs). Although they have some merits, such as low power and high swing, they have major drawbacks of slow response time and large die size. Therefore they are seldom adopted for high resolution and high speed applications. Current-steering DAC (CS-DAC) operates at high speed, but consumes large power. To tradeoff among power consumption, resolution, and speed, the resistor-string and current-steering hybrid digital-to-analog converter (R-I DAC) was proposed in [4].

The R-I DAC is an alternative solution for low-power, medium resolution, and medium speed applications. It has a hybrid segmented structure which adopts resistor-string as least-significant-bits (LSBs) and current-steering array as most-
significant-bits (MSBs). The R-I DAC combines the low-power feature of resistor-string and the high speed feature of current-steering array to compromise speed and power consumption. As a result, R-I DAC consumes less power to achieve medium speed. The measurement results of R-I DAC in [4] are 9-bit precision, 1.74 mW power consumption, and 20 MSps speed [4]. Although R-I DAC has many merits, its lowest output voltage can only reach 0.4 V. As 0.4 V accounts for a third of 1.2 V supply voltage, the available signal swing is too small, making R-I DAC not practical [4, 5, 6]. So it is necessary to increase the output swing of R-I DAC for low-voltage and low-power applications.

The increase of the output swing of current-steering based DAC is crucial for low supply voltage, which gains great attention. In 2015, Geunyeong and Minkyu proposed a full-swing CS-DAC by using both PMOS and NMOS current source array, together with a quaternary switch [7]. It has high speed (up to hundreds MHz). But it consumes high power, up to 19 mW, which is not acceptable in medical implantable applications. In 2010, Przyborowski and Idzik used an extra NMOS current mirror in a PMOS CS-DAC with output amplifier to improve the swing [8]. It can achieve high-swing and low power consumption. But it has a low-speed (200 KSps), which is not acceptable in many medical implantable applications either. In 2017, Huang and Yu used a voltage-controlled-current-source to generate a biasing current in order to eliminate the limitation of output swing [5]. The biasing current flows through the feedback resistor, generating a voltage drop at the output. The voltage drop removes the effect of the biasing voltage of the current source at the output. So the output voltage of the R-I DAC can reach as low as the ground and as high as power supply. Although the method of using a voltage-controlled-current-source improves the output swing, the power consumption is increased, which is not suitable for the applications demanding stringent low power consumption.

To further decrease the power consumption of [5], in this paper, we propose a novel R-I DAC with current-direction control. We adopt a PMOS current mirror to eliminate the output swing limitation of the R-I DAC. In contrast to [8], the current mirror in this paper uses low-voltage cascode scheme instead of gain-boosting. This current mirror scheme does not need an additional amplifier as does in gain-boost technique. So it improves the speed and reduces power simultaneously. It can not only solve the problem of limited output swing, but also further improve the power consumption and speed.

2 The proposed full-swing R-I DAC

The proposed R-I DAC with current-direction control is shown in Fig. 1. The three least-significant-bits (LSBs) \( b_2-b_0 \) are implemented by resistor-string voltage divider. The six middle-significant-bits (Mid-SBs) \( b_8-b_3 \) are implemented by current-steering array. The current-steering array consists of current source array and thermometer-decoder&switches. The most-significant-bit (MSB) \( b_9 \) controls current-direction control. The output \( V_p \) of the resistor-string voltage divider connects to the positive input of the output amplifier. The current \( I_{op} \) and \( I_{on} \) flow from the current-direction control block to thermometer-decoder&switches block.
The current-direction control block generates a direction-controlled output current $I_o$. The current $I_o$ flows through the feedback resistor $R_{FB}$ to generate voltage drop $I_o R_{FB}$. This voltage drop and the resistor-string output voltage $V_p$ are added at the output amplifier. The sum gives the final voltage output of the R-I DAC, which is expressed as

$$V_{OUT} = \frac{V_{dd}}{2} - I_U \cdot (2^3 - 1)R_U + (2^2b_2 + 2^1b_1 + b_0) \cdot I_U \cdot R_U$$

$$- b_9(2^5b_8 + 2^4b_7 + \ldots + 2b_4 + b_3 + 1) \cdot I_U \cdot (2^3 R_U)$$

$$+ b_9(2^5b_8 + 2^4b_7 + \ldots + 2b_4 + b_3) \cdot I_U \cdot (2^3 R_U) \quad (1)$$

In Eq. (1) and Fig. 1, $R_U$ is the unit resistance of the resistor-string. The resistance of the feedback resistor $R_{FB}$ is $2^3$ times of $R_U$. The biasing current $I_R$ of the resistor-string is identical to the unit current $I_U$ in the current sources array. The matching between LSBs and MSBs is ensured by the matching of $R_{FB}$ with $R_U$ and $I_R$ with $I_U$. The $V_{OUT}$ is biased at $Vdd/2 - 7 * I_U * R_U$, and varies up by $511 * I_U * R_U$ and down by $512 * I_U * R_U$. So $V_{OUT}$ can achieve full swing if $512 * I_U * R_U = Vdd/2 - 7 * I_U * R_U$ holds.

The input $b_8-b_3$ are decoded by a thermometer decoder to control switches $SW_{1-63}$. When $b_8-b_3$ are all 1’s, the switches connect to $I_{op}$. Otherwise they connect to $I_{on}$. The $b_9$ controls a multiplexer (with input $B$ and $C$, output $X$ and $Y$) in the current-direction control. When $b_9$ is 1, $B$ connects with $X$ and $C$ connects with $Y$. When $b_9$ is 0, $B$ connects with $Y$ and $C$ connects with $X$. In the current-direction control, the output of current mirror $I_{mn,M}$ flows into node $B$ of the multiplexer. The current $I_{mM}$ and $I_{op}$ in Fig. 1 are provided by the current source array to make the current mirror transistors work in saturation region. The current mirror makes
$I_{bn} + I_{on} = I_{bp} + I_{on,M}$ hold. Since $I_{bn} = 5I_U$ and $I_{bp} = 4I_U$, we have $I_{on,M} = I_{on} + I_U$. This current relationship is used to calculate the $V_{OUT}$.

Fig. 2 shows the implementation of current-direction control which consists of a current mirror and a multiplexer. The current mirror uses low-voltage cascode scheme, instead of gain-boosting as [8] which further enhances the output resistance. Because the variation of voltage $V_n$ is small, low-voltage cascode scheme provides large enough output resistance to meet the precision requirement of the current mirror [8]. Besides, the gain-boosting needs an additional amplifier. This amplifier not only limits the response speed of the current mirror, but also increases the power consumption. Therefore, our design adopts a low-voltage cascode scheme. The switch unit in the multiplexer is implemented by a NMOS transistor, instead of NMOS and PMOS complementary scheme. Although the on-resistance of complementary switch is low, it consumes more die size and power than a single NMOS. In addition, because the on-state NMOS switches work in strong inversion region in all voltage-supply range, its on-resistance is small enough to transport output current [9, 10, 11]. So the use of single NMOS switch to implement multiplexer is adopted to meet the design requirements.

### 3 Measurement and comparison

The proposed 10-bit full-swing R-I DAC is implemented using Global Foundry standard 180-nm CMOS technology. The chip micrograph is shown in Fig. 3.

The core die size is 0.45 mm × 0.48 mm. The power supply is from 1.25–1.5 V and typical value is 1.35 V. The total power consumption is 0.41 mW for a full-swing sinusoidal input of 40.82 kHz at a 3.125 MS/s sampling clock. The total static current consumption of R-I DAC is 275 µA. The unit current $I_U$ of current-source array is 2.5 µA. The full swing of current $I_o$ flowing through feedback resistor is 160 µA. The current $I_{bp}$ in Fig. 1 is 10 µA. The output amplifier consumes about 90 µA. The feedback resistance $R_{FB}$ is 3.2 kΩ. The unit resistance of resistor-string is 400 Ω. The ramp response, the pulse response, and the spectrum are tested, respectively.
Fig. 4(a) shows the measured full-swing output voltage for a ramp input with 1-LSB step, where x-axis is the time. The magnification of a small area is also shown in Fig. 4(a). The worst case linearity error occurs at the transition when 3 bits of LSBs switch from all 1’s to all 0’s and add 1 to the middle-significant-bits, for example, changing 00...00,111 to 00...01,000. Such linearity error can be seen clearly in differential-nonlinearity (DNL) and integral-nonlinearity (INL), as shown in Fig. 4(b). The magnification of a small area is also shown in Fig. 4(b). We can see the DNL fluctuates with a period of 8. Such linearity error is common in the segmented architectures. The maximum DNL is 2 LSB, which happens at the transition when the 3-bit LSBs switch from all 1’s to all 0’s and add 1 to the middle-significant-bits.

The measured maximum DNL is approximately 2 LSB, which means the measured equivalent resolution number is 9 for our chip. Without calibration, the measured DNL is 1-bit worse than the designed one, which is quite normal for resolution number around 10 [6, 12]. The measured nonlinearity is acceptable in many applications, e.g. implantable chip where the most important is not high resolution because 9-bit DAC is good enough for most physiological signals. Low power dissipation is the most important specification in implantable applications because the power supply is obtained by battery or energy radiation. Therefore the tradeoff among resolution, speed, output swing, and power dissipation needs to be considered carefully.

When the input of b9 switches from 0 to 1, the current-direction control changes the direction of current Io. In Fig. 4(b), we can see that the DNL of before and after transition of b9 are almost the same. It indicates that the current-direction control has little effect on the static linearity.

Fig. 5 shows the measured full-swing pulse response of the proposed R-I DAC. The output of the DAC connects with the probe (with the attenuation of 10× and the parasitic capacitance of 16 pF) through a series 1-kΩ resistor. The output swing range is 170 mV–1.17 V. The settling time is 300 ns.

Fig. 6 shows the measured output spectrum of the proposed R-I DAC. The DAC output is connected with the input of a spectrum analyzer through a series 4.7 kΩ resistor. Fig. 6(a) shows the spectrum of the DAC with an input frequency of 40.82 kHz and a 3.125 MS/s sampling clock. Fig. 6(b) is the measured dynamic
performance of the DAC, including spurious-free dynamic range (SFDR), total harmonic distortion (THD), signal to noise ratio (SNR), and effective number of bits (ENOB) for different input frequencies. In Fig. 6(a), the measured SFDR is
43.08 dB with 40.82 kHz sine-wave input. In Fig. 6(b), with the input signal frequency increasing from 400 Hz to 400 kHz, the dynamic performances get worse by different degrees. The THD has the worst performance. It drops from 55.9 dB to 33.1 dB. The ENOB drops from 8.9 bits to 5.2 bits. The ENOB is better at low frequency than high frequency. With frequency increasing, in addition to device mismatch, the glitches, timing mismatch error, and high frequency parasitic become more prominent and finally dominant. So the ENOB becomes worse at high frequency.

Table I presents the performance comparison of our work with three state-of-the-art DACs. All DACs have full swing single-ended voltage output. However reference [7] does not use an output amplifier for the reason of high-speed application because output amplifier is the bottleneck of the dynamic performance in high-speed. Other DACs use output amplifier as trans-conductance and buffer. They can drive a wide range of load with less loading effect.

In Table I, the resolution, area, output swing, speed, and power consumption of DACs are compared. In order to estimate the overall performance, the figure-of-merit (FOM) and area efficiency (AE) are introduced [5, 13, 14]. The FOM
measures the achievable resolution and speed per unit die size and power. The larger the FOM, the better the overall performance is. Table I shows that this work has better overall performance than others at low frequency. With frequency increasing, the ENOB and FOM of this work decrease because low-power output amplifier becomes the bottleneck of the dynamic performance at high speed. Some low-frequency applications such as precision DACs are insensitive to frequency performance [8]. Most datasheets of commercial precision DACs do not give specifications of frequency performance [1]. This work is designed for the precision

Table I. Comparison of the state-of-the-art designs.

| Output Type | [8] 2010TNS | [7] 2015TCAS-II | [5] 2017MEJ | This work |
|-------------|-------------|----------------|-------------|-----------|
| Full-swing (Buffered) | Full-swing (Unbuffered) | Full-swing (Buffered) | Full-swing (Buffered) |
| Technology | 0.35 µm CMOS | 0.11 µm CMOS | 0.18 µm CMOS | 0.18 µm CMOS |
| Architecture | current steering + amplifier | current steering + output selector | current steering + amplifier | Resistor-string & current steering + amplifier |
| Resolution (bit) | 10 | 6 | 6 | 10 |
| SNDR (dB) | - | 35 | 27.91 | 33.1 to 55.2 |
| ENOB (bits) | - | 5.52 | 4.34 | 5.2 to 8.9 |
| SFDR (dBc) | - | 43 | 44 | 36.5 to 52.7 |
| FS<sup>(B)</sup> Current (mA) | 0.05 | 1.65 | 0.5 | 0.16 |
| FS output voltage (V) | 2.5 | 3.2 | 1 | 1 |
| Supply Voltage (V) | 3.3 | | | |
| DNL/INL (LSB) | 0.42/0.42 | 0.7/0.7 | 0.05/0.33 | 2/2.4 |
| Sample rate (MS/s) | 0.5 | 1000 | 20 | 3.125 |
| Power Consump. (mW) | 0.6 | 19.1 | 1.5 | 0.41 @1.35 V supply |
| Area (mm<sup>2</sup>) | 0.18 | 0.46 | 0.12 | 0.22 |
| FOM<sup>(F)</sup> Static<sup>(C)</sup> | 4.74 | 7.28 | 7.11 | 16.55 |
| (×10<sup>5</sup>) | - | 5.22 | 2.25 | 1.27 |
| AE<sup>(G)</sup> (×10<sup>-8</sup>) | - | 1002 | 593 | 599 to 46<sup>(E)</sup> |

A) The label “-” means parameters not given in the reference.
B) FS: Full-Scale.
C) For low frequency applications, the ENOB 8.9 is used to calculate FOM for our work and 10 or 6 is used for others work, respectively. Since we use ENOB 8.9 in the calculation, the effect of poor nonlinearity (DNL/INL) has been included.
D) For high frequency applications, the ENOB 5.2 is used to calculate FOM for our work and 5.52 or 4.34 is used for others work.
E) 5.2 bit and 8.9 bit are used to calculate AE, respectively.
F) FOM = \( \frac{2 \times \text{sampling rate}}{\text{area} \times \text{power}} \)
G) AE = \( \frac{\text{area} \times \text{power}}{\text{ENOB}} \)
low-power medium-speed applications. Our goal is making best tradeoff among power dissipation, resolution, output swing, and speed. It is mostly used in low speed applications, such as implantable devices. So relatively poor frequency performances at high frequency is acceptable. Comparing with [7] and [5], this work achieves higher resolution number at similar cost. Comparing with [8], this work achieves higher working speed.

The area efficiency measures how much die size needed to implement per resolution number. The smaller the AE, the better efficiency is. Comparing with [7] and [5], this work achieves better area efficiency. Because the propose high-swing R-I DAC adopts hybrid structure (resistor-string and current-steering array) and the current-direction control, it can realize high resolution number at relatively small die size.

4 Conclusion

In this paper, we have proposed a novel R-I DAC. It adopts a hybrid structure and a current-direction control. This R-I DAC has a full-swing single-ended output voltage (0.17–1.17 V for 1.25 V supply), 300 ns settling time, and 0.41 mW power consumption. The performance comparison shows that this work has better overall performance and area efficiency. The proposed high-swing R-I DAC is especially suitable for low supply voltage (as low as 1.2 V), low power consumption (lower than 1 mW), and medium speed (around 10 MHz).

Acknowledgments

This work was supported in part by National key R&D plan (Grant number 2016YFC0105002 and 61674162), Shenzhen Key Lab for RF Integrated Circuits, Shenzhen Shared Technology Service Center for Internet of Things, Guangdong government funds (Grant numbers 2013S046 and 2015B010104005), Shenzhen government funds (Grant numbers JCYJ20160331192843950), and Shenzhen Peacock Plan.