Design of 12T SRAM cell for low power dissipation

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Abstract. The present semiconductor industry is developing quite quickly. Mobile and portable devices are becoming small for each day and moreover there is a rising demand for extended battery power. With these demands it is significant for researchers to emphasis on the leakage capacity in standby mode. For the exact communication, SRAM was intended with DSP, processor and applications with lowpower devices. The design engineer emphases mostly on the making of low energy consuming, higher bandwidth and large memory capacity. Memory is an essential part of majority of these systems as well as it is also reduced as the system size reduces. High processing architecture as well as low power is consequently a foremost concern. The robustness of static random access memory cells is other important factor. This paper proposed the architecture design of 12T SRAM for the reduction minimization of power leakages or power consumption during the sleep transistor. This supports in the minimization of the leakage in the CMOS transistor. Based on the parameters like write delay, read delay, write voltage, read voltage, and power consumption at various temperature are compared to the existing SRAM architecture of 6T, 7T and 8T, we acquire reduced power consumption in the proposed 12T SRAM architecture.

1. Introduction
The need for low power / energy consumption of the integrated ICs, is increasing rigidly through the success of wearable and portable electronic components as well as the omnipresent implementation of sensor networks in wireless communication. The supply voltage of the integrated circuits has been reduced in the near/sub-threshold values if the frequency is not a major issue in order to decrease the energy/ power consumption of these circuits. The embedded chips include essential elements which make a major contribution to overall power / energy use [16] in the static random access memory devices. Nonetheless, owing to the severe damage in the noise margin with static read and the capacity with write enable, in addition to the rigorous impacts of the leakage current with read bitline[17], a regular six transistor (6T).

SRAM track usually supplied by the foundry has not been ranged to near/ sub-thresholdvalues. Designing an ultralow power Static Random Access Memory circuit is vital for embedded chips used in wearable or portable electronics components. The topology of the Static Random Access Memory cell is revamped to allow many numbers of transistors to maximize the noise gap with static read, also to boost write performance, and decrease the leakage present in read bitline [18]. On the other hand,
the compilers of the memory must be implemented in a difficult and conventional way, given the presence of analog signal and pre-loaded circuitry with sensor amplifiers in the SRAM array as the analog signal. An alternative in performing the ultralow power operation for Static Random Access Memory circuits is the architecture of the standard cell based memory (SCM) elements [19]. To construct the Static Random Access Memory modules by using regular logic cells, all the inputs as well as outputs are made electrical signals. The automated model cells can be implemented fully through the peripheral devices. The current Electronic Design Automated software can therefore be utilized to conduct logical synthesis along with automated positioning, routing to produce the net list and configuration with the necessary arrays of SRAM [20]. For the applications of embedded system, the arrays of SRAM in rapid generation are highly desirable in which a huge number of different sized memory elements are required. In comparison, write and read operations are executed similarly through the use of modern standard cells as the transmission of signal in conventional combinational circuits that assures huge data reliability and good capacity of write operation [21]. The biggest problem with the SCM cells is the overhead in each cell with huge area. Compared to conventional 6T SRAM cell, each SCM cell has the layout region that could be greater for two to three times than 6T SRAM. Nevertheless, the area output of the total SRAM system has been much higher compared with the SRAM regular cell-based circuit relative to the earlier implementation of SRAM circuits with ultralow voltage. It happens while there is a memory array of relatively little size, so that peripheral circuit greatly supplied to the entire array area [7]. A novel robust 12T SRAM based on standard cell for ultralow voltage and ultralow power applications is proposed in this article. In Complementary Metal Oxide Semiconductor to minimize the leakage, a lower supply voltage is powered to the circuit which, in turn, the speed of the circuit is lowered. By using the lower threshold voltage for the transistors, the delay can be reduced, however this further reduces the flow rate again (especially the flow cycle). Different conditions have presented and the implementation of a memory cell with a low standing leakagein addition to practical reliability necessities a better optimization. The important data reliability loss in the cells occurs when a higher voltages and smaller measurements are induced. In order to achieve high range performance and low write energy consumption, three transistors are utilized on every column of Static Random Access Memory cells. During the three-stage reading cycle, reading delays and power consumption are minimized. In addition, parallel cross-coupling feedback with the proposed SRAM 12T cell, ensures high data stability and writing ability.

This is how the article is arranged. Section II reviews the existing SRAM standard cell-based circuits. Sections III in which the problem statement was depicted and Section IV present and evaluate a proposed novel 12T SRAM based on standard cell circuit. Section V depicts the summary of the paper.

2. Literature survey

In [1], a modern 12T memory cell that is energy-efficient is suggested to help architecture hardened radiation (RHD) in close-to-threshold voltage resistance multi-node (SEMNU) single-event upsets. Through monitoring cross-coupled PMOS devices of inverters through foolish access transistors, the radiation complexity of the proposed storage cell will be increased. In STMicroelectronics 6, we had validated the proposed memory cell. In [2] they propose an overall reduction in the amount of VMIN and resources per service with a 12ST-based SRAM-bit cell to promote the process variance sensitive write- capability. In [3] a halve select 12T SRAM free cell features an input cutting tool to enhance the ability to write and separate reading paths in order to improve reading stability. The write and read capabilities are 2.84 and 1.95 respectively better than the normal 6T cell at 0.4V.

In [4] presents the SRAM, a compiler that targets small to medium array sizes and provides a solution with smaller area compared to traditional 6T-based SRAMs, with the one-port random access memory of ultralow voltage. The design uses a 12T write and the read upset free bit-cell. Array architecture uses a read-modifying writing scheme to enable masking and multiplexing columns for bit-write (BW). The Built-inside Self-Test (BIST) and Synchronous Writing Through (SWT) methods have testability, while the Sleep-and Shutdown Methods Power Management (PM) alternative is included. In [5] a9-Transistor(TG9T)SRAMbitcellpower-efficienttransmissiongategathasbeenproposed. In [6] Optimized MTJ (Approximate Calculation Application (AC) Procedure, focused on resistive ternary information addressable memory
(ReTCAM). In [7] a new 12 T SRAM cell is introduced that is used to improve reliability with an Schmitt control circuit and to reduce the leakage current in standby mode with a transistor. In [8] discusses the phenomenon of crucial linear transfer of energy (LET) and the charge obtained by scaling the technology of each circuit. In [9] Propose modified 12 T SRAM cell (WWL12 T) FinFET and selfrefreshing. To increase the FinFET's reliability and performance, the double-k gate isolator and symmetric distance is used. In [10] the 12 T static random access memory (SRAM) cell dependent on the one-ended Schmitt signal (ST). Cross-point data-conscious writing framework is used in the planned cell and therefore promotes interlocking architecture to minimize soft errors. The proposed cell is not interrupted by reading because the bit line is completely isolated from the data storage node. In [11] presents a 12 T 2RW SRAM low voltage with parallel exposure and blocked interruption to improve the performance without degradation. The suggested SRAM cell reduces interference by splitting reading from internal nodes and minimizes the probability of worst case stability with a 6 percent region cost. Furthermore, hierarchical bitlines, a virtual ground technology and the minimum voltage and energy consumption will be further reduced. In [12] the design based on the 12 transistor (12 T) cell is proposed for the low power and variability-aware static random access memory (SRAM). In [13] an advanced 12 T Static Random Access Memory (SRAM) cell with the following advantages: decreased leakage current and increased efficiency utilizing 180NM technology was proposed. In [14] Presents a 9 T static random access memory (SRAM) cell with a single-ended Schmitt signal. The architecture suggested offers improved reading stability when ST-based inverters are used. In [15] the introduction of the Schmitt Trigger (ST) enhanced switching functionality, reduced the power outages and increased the SNM. Upon applying the memistor to the SRAM trigger Schmitt, the cell was not fragile and the SNM improved more.

3. Problem statement
The SRAM technology suffered a lot due to leakage issues. There are several other existing technologies that are there, but they are all not useful. Hence there is a need for an effective method to overcome the leakage issues in the SRAM technology. We would propose a new SCM with parallel cross-coupling logic that will reduce expenses, time, power, and memory complexity.

4. Proposed methodology
This proposed method implemented to decrease write and read energy consumption in order to maintain high data reliability and write skills on the current 12 T SRAM low power circuit. With the use of advanced 65-nm CMOS materials, all transistors in SRAM cells use smallest channel length (60 nm) and channel width (80 nm). The transistor has shared the every column of SRAM cells. For physical design, the proposed static random access cell has been implemented and described as a standard cell and are treated in analogous manner to the sleep transistors utilized while routing and planning.

The proposed method can handle an upto 4 bit that consists of a block. Such four bits are interpreted by mask transistors, gate transistors, four pairs of intertwined cross coupled inverters, read buffer and writer entry transistors. Based on the stacked nMOS configuration theory, the read buffer is used. The leakage voltage has been avoided by this configuration. It contains a line to pick the signal you need, called as BPS [Block Pick Signal]. The typical 12T cell process is carried on as follows. BPS is set to 0V to enforce write operation. And therefore the word line is permitted. Likewise, BPS is set at 1V for a read operation, as well as the word line is stopped. Therefore the line of terms serves as an ON-Off turn. Figure 1 shows the schematic representation of the proposed methodology for the design of 12T static random access memory.
For LBL to discharge, a supply voltage VDD is carried out. This will shut the read buffers off, in effect. In the meantime, the full VDD supply voltage has preloaded to RBLs and the word lines are retained at 0V. During the read process, the block mask transistors are enforced to persist in the OFF place. To hold the transistor in ON stage, the word line is restricted for the transfer accesses. As a consequence, through the pass gate transistor the data stored in a single cell is distributed to the RBL from LBL. When the data is stored, it discharges the RBLs. These RBLs are located on the blocks of the given column and row. After the read process ends, word lines are connected at zero voltage to switch OFF the transistors pass-gate. The best way to minimize energy consumption through the use of 12T SRAM is to do so. This novel configuration is built. It minimizes energy consumption as a result of standby, read wait, writing delays, etc. Experimentally demonstrated by implementing the parallel cross coupling logic in 12 T SRAM which is the best way to save energy use and operating delays.

The size of memory cell is also minimized with the lower processing nodes. The current memory cell leakage factor will be increased thereby. The intersection of leakage, gate leakage and multithreshold leakage current are various additives which triggers the 12 T static random access memory cell leakage. However in lower-technologies, multi threshold leakage current is predominant. When the leakage current is off, the voltage of transistor gate is less than the voltage at its highest and contains mostly of a diffusion stream; the transistor gate voltage is the lowest. It is represented by the following equation (1),

\[
L_{multi} = \mu_0 D_0 (W/L)(KT/Q)^{2(N-1)} \exp[q(V_{gs} - V_t) (1/nPT)] [1 - \exp(-qV_{cs}/PT)] \tag{1}
\]

The circuit consists of M6 transistors. RBL and BL are also utilized, which act as output as well as input lines respectively from the memory cell. The cell leakage element must be calculated for estimation. The cell ratio is the reader-sized ratio to the connection transistor through the processing, in addition the PR-to-access ratio is the load-transistor ratio across the whole write activity. Equation (2) and (3) gives the read and write operation respectively.

During Read operation,
\[ CR = \frac{W}{l} n \]  

During write operation
\[ PuR = \frac{(W/l)p}{(W/l)n} \]

Where PuR is the pull ratio and CR is the cell ratio.

In the proposed architecture, we had analyzed the 12T static random access memory cell, for every write operation the energy consumption of complex bit-lined has also estimated. To motivate this, we examine as a design for two columns of static random access memory cells (i.e., four bit lines). Each of static random access memory cell has been connected to the ground (GND) until the write process. After the written service, two bit lines from GND to VDD has been paid. The estimation of 12T static random access memory cell for a complex energy consumption is carried out using the equation (4).

\[ P_{12T} = P_{\text{Bitline}_{-1}} = \left( \frac{1}{2} CV_{DD} \right)^{2} = 4CV_{DD}^{1/2} \]

Regarding to our 12T-SRAM cells mentioned, after the written process the four bit voltages are GND, \(1/2VDD\), \(1/2VDD\), and \(VDD\). As the expectation to charge is only from \(1/2VDD\) to \(VDD\) line, the robust 12T SRAM cell has prompted to the complex power consumption.

\[ P_{12T}\text{-SRAM} = P_{\text{Bitline}} = \frac{1}{4} C\left(V_{DD}/2\right)^{2} = \frac{1}{4} CV_{DD}^{1/2} \]

It can be seen from the above equation (5) that the planned system would reduce the electricity consumption. The projected power consumption is less than typical 6 T or 8 T owing to leakage of power consumption. Figure 2 shows the design of proposed 12T SRAM in cadence tool.

**Figure 2.** Proposed 12T SRAM architecture

4.1. Leakage power calculation

Multi-threshold leakage and gate leakage are the main sources of SRAM leakage capacity. This is where a technique for the elimination of multi-threshold leakage and the leakage of robust 12T-SRAM cells is implemented and suggested. However, even if the body distortion is presented, the leakage current present is less than 8 percent of total power. Therefore, eliminating leakage is not our original design intent. The potential energy usage of 12 T leakage is less than the conventional system. The small energy consumption difference was found owing to the various pre-loaded bitline voltages as given in equation (6). In a Robust 12- T SRAM data manager, bit lines BL1 and BL1 N are preloaded onto "1" and word line write on "0" while the gate-leakage is induced from the source to the gate by the CMOS transistorswitch.

\[ LC_{12T\text{ SRAM}} = C_{\text{wn ctrl}} + C_{\text{rdctrl}} + C_{\text{dec}} + C_{\text{wn col}} + C_{\text{rd col}} + C_{\text{mem core}} \]
5. Result and discussion
The new method results in an effective 12 T SRAM design for power consumption, and the research that is being developed further shows that 12T cells can be extremely valuable for modeling SRAM cells relative to standby, write and read operation. The tool used to design this system is Cadence EDA.

Different temperature conditions in reserve mode are recognized in the capacity with power dissipation of the suggested cell along with recommended robust 12T SRAM Cell. The estimated dissipation of the current rely upon the various temperature. Figure 3 shows the study of the temperature in different static random access memory cell types.

![Power Dissipation at Different Temperature](image1.png)

Figure 3. Power Dissipation at Different Temperature

![Read and write delays of the 12T SRAM arrays](image2.png)

Figure 4. Read and write delays of the 12T SRAM arrays

From the figure 4, note that when compared to the previous methodologies, the 12T SRAM circuit has still shorter propagation delay owing to the considerably lengthier read access delay of the existing 12T SRAM circuit.

Figure 5 shows the memory array in idle mode for the leakage power consumption. The minimum channel length is utilized for every transistors in order to reduce the area layout of the memory cell, for the proposed robust 12T SRAM cell. When compared to the existing array of memory, the leakage power consumption of the proposed 12T SRAM array is consequently little.
higher. While the supply voltage VDD brings down to 0.2 V, there is an increase in 12T SRAM array with the leakage overhead rises from 0.8% to 8.8%, compared to the existing array of memory.

![Figure 5: Leakage power consumption](image)

### 6. Conclusion
The Cadence EDA used for the design of SRAM cells has been developed and modeled here. The results from the simulation showed that the 12 T SRAM cell circuits proposed has decreased leakage power consumption. With increasing supply voltages and increased temperatures with specific supply voltage, leakage power increases. Total power used is also substantially reduced for all planned loops. Nevertheless, the trustworthiness of the proposed circuits is jeopardized because leakage current is minimized for the individual states in the proposed circuit. Thus the low power 12T SRAM has been used.

### References
[1] Kumar C I and Anand B 2019 A Highly Reliable and Energy Efficient Radiation Hardened 12T SRAM Cell Design IEEE Transactions on Device and Materials Reliability
[2] Sharma P Gupta S Gupta K and Pandey N 2020 A low power subthreshold Schmitt Trigger based 12T SRAM bit cell with process-variation-tolerant write-ability *Microelectronics Journal* vol 104703
[3] Sharma V Bisht P Dalal A Gopal M Vishvakarma S K and Chouhan S S 2019 Half-select free bit-line sharing 12T SRAM with double-adjacent bits soft error correction and a reconfigurable FPGA for low-power application *AEU-International Journal of Electronics and Communications* vol 104 pp 10-22
[4] Sinangil M E Lin Y T Liao H J and Chang J 2019 A 290 mV 7 nm Ultra Low Voltage One Port SRAM Compiler Design Using a 12T Write Contention and Read Upset Free Bit-Cell *IEEE Journal of Solid-State Circuits* vol 54 pp1152-1160
[5] Pal S Bose S Ki W H and Islam A 2020 A highly stable reliable SRAM cell design for low power applications *Microelectronics Reliability* vol 105 p113503
[6] Suresh Kumar R and Manimegalai P 2019 implementation of Neural Network with ALE for EEG Signal Processing *Current Sig Trans Therapy* vol 14 pp1-7
[7] Upadhyay G Rajput M A and Saxena M N 2017 An Analysis of Novel 12T SRAM Cell with Improved Read Stability *Int J Innov Res Eng Appl Sci* vol 3
[8] Yusop N S Nordin A N Khairi M A and Hasbullah N F 2018 The impact of scaling on single event upset in 6T and 12T SRAMs from 130 to 22 nm CMOS technology *Radiation Effects and Defects in Solids* vol 173 pp 1090-1104
[9] Yadav N Shah A P and Vishvakarma S K 2017 Stable reliable and bit-interleaving 12T SRAM for space applications: a device circuit co-design *IEEE Transactions on Semiconductor Manufacturing* vol 30 pp 276-284

[10] Suresh Kumar R and Manimegalai P 2020 Near lossless image compression using parallel fractal texture identification *Biomedical SigProc and Contl* vol 58 p 101862

[11] Wang B Zhou J and Kim T T H 2017 A 0 4 V 12T 2RW dual-port SRAM with suppressed common-row-access disturbance *Microelectronics journal* vol 69 pp 78-85

[12] Yadav A and Nakhate S 2016 Low standby leakage 12T SRAM cell characterisation *International Journal of Electronics* vol 103 pp 1446-1459

[13] Thakare P V and Tembhurne S 2016 A power analysis of SRAM cell using 12T topology for faster data transmission *Int J Sci Technol Eng* vol 2 pp 441-446

[14] Suresh Kumar R, Dhanagopal R, Menaka R and Ramesh R 2020 IoT based Drowsiness detection, Monitoring and Controlling System *International Journal of Advanced Science and Technology*, Vol. 29, No. 03, pp. 8543 – 8549.

[15] Nikitha L Bhargavi N S and Kariyappa B S 2019 Design and Development of Non-volatile Multi-threshold Schmitt Trigger SRAM Cell *In Emerging Research in Electronics Computer Science and Technology* Springer Singapore pp. 877-884

[16] Alioto M 2012 Ultra-low power VLSI circuit design demystified and explained: A tutorial *IEEE Transations on Circuits and System* vol 59 pp 3-29

[17] Sinangil M Verma N and Chandrakasan A 2008 A reconfigurable 65 nm SRAM achieving voltage scalability from 0.25-1.2 V and performance scalability from 20 kHz-200 MHz *Proc. of the IEEE European Solidstate Circuits Conference* pp. 282-285

[18] Dhanagopal R and Muthukumar B 2019 A Model for Low Power High Speed and Energy Efficient Early Landslide Detection System Using IoT *Wireless PersCommun* https://doi.org/10.1007/s11277-019-06933-7

[19] Meinerzhagen P Sherazi S M Y Burg A and Rodrigue J N 2011 Benchmarking of standard-cell based memories in the sub-VT domain in 65-nm CMOS technology *IEEE Journal of Emerging and Selected Topics in Circuits and Systems* vol 1 pp 173-182

[20] Muthukumar B Dhanagopal R and Ramesh R 2019 KYP modeling architecture for cardiovascular diseases and treatments in healthcare institutions *J Ambient Intell Human Comput.* https://doi.org/10.1007/s12652-019-01653-z

[21] Dhanagopal R KrishnamurthiV and Rajaram A 2017 Mitigating the Soft Errors and Controlling the Voltage Level of VLSI Devices – MSCV *Journal of Computational and Theoretical Nanoscience (CTN)* Vol 14 pp. 3209-3219 https://doi.org/10.1166/jctn.2017.6618.