Insulated gate and surface passivation structures for GaN-based power transistors

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Abstract
Recent years have witnessed GaN-based devices delivering their promise of unprecedented power and frequency levels and demonstrating their capability as an able replacement for Si-based devices. High-electron-mobility transistors (HEMTs), a key representative architecture of GaN-based devices, are well-suited for high-power and high frequency device applications, owing to highly desirable III-nitride physical properties. However, these devices are still hounded by issues not previously encountered in their more established Si- and GaAs-based devices counterparts. Metal–insulator–semiconductor (MIS) structures are usually employed with varying degrees of success in sidestepping the major problematic issues such as excessive leakage current and current instability. While different insulator materials have been applied to GaN-based transistors, the properties of insulator/III-N interfaces are still not fully understood. This is mainly due to the difficulty of characterizing insulator/AlGaN interfaces in a MIS HEMT because of the two resulting interfaces: insulator/AlGaN and AlGaN/GaN, making the potential modulation rather complicated. Although there have been many reports of low interface-trap densities in HEMT MIS capacitors, several papers have incorrectly evaluated their capacitance–voltage (C–V) characteristics. A HEMT MIS structure typically shows a 2-step C–V behavior. However, several groups reported C–V curves without the characteristic step at the forward bias regime, which is likely to the high-density states at the insulator/AlGaN interface impeding the potential control of the AlGaN surface by the gate bias. In this review paper, first we describe critical issues and problems including leakage current, current collapse and threshold voltage instability in AlGaN/GaN HEMTs. Then we present interface properties, focusing on interface states, of GaN MIS systems using oxides, nitrides and high-κ dielectrics. Next, the properties of a variety of AlGaN/GaN MIS structures as well as different characterization methods, including our own photo-assisted C–V technique, essential for understanding and developing successful surface passivation and interface control schemes, are given in the subsequent section. Finally we highlight the important progress in GaN MIS interfaces that have recently pushed the frontier of nitride-based device technology.

Keywords: AlGaN, GaN, HEMT, MIS structure, C–V, interface state

(Some figures may appear in colour only in the online journal)
A development of a stable MIS gate structure has been a challenging target in field-effect-transistors (FETs) using traditional III–V semiconductors such as GaAs, InP, InGaAs, etc. Among them, InGaAs MISFETs have gained much attraction due to their excellent carrier transport properties. In fact, the electron mobility in this system is more than 10 times higher than in silicon at a comparable sheet density, making the integration of the InGaAs MISFET on the Si platform highly desirable [22–24]. The MIS gate structure requires a dielectric free of trapped charge and other defects, few interfacial electronic states and high reliability. However, unlike Si, there have been no native oxides for III–V semiconductors that meet these requirements. In addition, various kinds of insulators/III–V structures prepared by a standard chemical vapor deposition (CVD) showed poor interface properties mainly arising from high-density interface states. The atomic layer deposition (ALD) technique opened the door for manufacturing III–V MOSFETs, because the ALD can provide relatively high-quality oxides/III–V interfaces. Ye et al. [25] reported epoch-making performance from a GaAs MOSFET with an ALD Al₂O₃ gate, showing high gain and good RF characteristics. They later demonstrated significantly improved device performance on Al₂O₃-gate InGaAs MOSFETs with higher InAs compositions in the InGaAs channel [26]. Furthermore, very high effective channel mobilities over 4000 cm² V⁻¹ s⁻¹ were reported in ALD Al₂O₃-gate InGaAs MOSFETs [27, 28].

However, instability issues related to I–S interface states still remain in the InGaAs and GaAs MOSFETs [29]. In this relation, frequency dispersion at accumulation bias is a commonly observed feature in the experimental capacitance–voltage (C–V) characteristics of MOS structures using GaAs, InP and InGaAs [30–36], as shown in figure 2. To explain this instability behavior, the border trap (BT) model was proposed [37]. This model assumes defect levels inside the gate insulator, as shown in figure 3(a). In this case, BTs have long time constants as they interact with the conduction band electrons via tunneling, leading to large frequency dispersion even at accumulation bias [38, 39]. The disorder-induced gap state (DIGS) model [40, 41], as schematically shown in figure 3(b), can well explain frequency dispersion at accumulation bias. In this model, it is assumed that disordered region at the semiconductor surface includes defects, dangling bonds and lattice displacement (disorder in bond lengths and angles), thereby producing electronic states with density distributions in both energy and space. When interface states have space distribution, electron capture/emission processes also include tunneling effects. Recently, Galatage et al. [36] reported a comparison of the BT and DIGS models by fitting both models to experimental data. Although both models suggested that frequency dispersion was caused by high-density electronic states within 0.8 nm from the crystalline semiconductor surface, they claimed that the experimental capacitance frequency dispersion in accumulation can be well explained by the DIGS model. This led them to conclude that frequency dispersion is indeed due primarily to disorder induced gap states in the semiconductor side. Moreover, since
the C–V frequency dispersion in InGaAs MOS structures has been observed for a variety of dielectrics including Al₂O₃, HfO₂, ZrO₂, LaAlO, HfAlO, etc, it is unlikely that the same BT would have almost the same energy from the InGaAs conduction band edge can be consistently reproduced using different dielectric materials.

To develop a MIS gate applicable to practical devices, characterization of MIS interface properties have become of utmost importance for understanding the underlying physics required for circumventing problematic issues. Although different insulator materials have been used to GaN-based transistors including HEMTs, the resulting insulator/III-N interfacial properties are still not fully understood. This is partly due to the higher degree of complexity involved in these structures. In comparison with a conventional MIS structure having a single semiconductor layer, it is difficult to characterize the insulator/AlGaN interfaces in a MIS HEMT because it has two interfaces: insulator/AlGaN and AlGaN/GaN.
making the potential modulation rather complicated. In addition, the emission efficiency of electrons from the wide-gap interface states to the conduction band is very limited at room temperature (RT). For example, in the case of AlGaN with an Al composition of 30% ($E_G \sim 4.0 \text{eV}$), the time constant for electron emission to the conduction band is estimated to be in the $10^{10} - 10^{20} \text{s}$ range for near-midgap states at RT [42]. In this case, the charge condition of such deeper states cannot be changed by bias sweeping in a standard $C-V$ measurement. Although there have been many reports of low interface-trap densities in HEMT MIS capacitors, several papers may have incorrectly evaluated their $C-V$ characteristics. A HEMT MIS structure typically shows a 2-step $C-V$ behavior [42]: one in the negative gate voltage regime that represents the total series capacitance of AlGaN and insulator layers, and the other in the positive gate voltage regime representing only the insulator capacitance. However, several groups reported $C-V$ curves without the characteristic step at the forward bias regime. This is likely due to the high-density states at the insulator/AlGaN interface impeding the control of the gate over the AlGaN surface potential.

Eller et al [43] systematically reviewed surface and interface properties of GaN and AlGaN, including surface electronic/pinning models, reliability issues, surface treatment processes and dielectric passivation processes. Roccaforte et al [44] reported the review on dielectric technologies for SiC and GaN power devices, e.g. effects of interface states on channel mobility and stability of threshold voltage in SiC MOSFETs and improvement of device performance in GaN MOS HEMTs. In this article, we review insulated gate and surface passivation technologies for GaN-based MIS transistors including HEMT devices. First, we describe critical issues and problems including leakage current, current collapse and threshold voltage instability in AlGaN/GaN HEMTs. Then we present interface properties, focusing on interface states, of GaN MIS systems using oxides, nitrides and high-$\kappa$ dielectrics. Next, the properties of a variety of AlGaN/GaN MIS structures as well as different characterization methods, including our own photo-assisted $C-V$ technique, essential for understanding and developing successful surface passivation and interface control schemes, are given in the subsequent section. Finally, we highlight the important progress in GaN MIS interfaces that have recently pushed the frontier of nitride-based device technology.

2. Instability issues in GaN-based HEMTs

2.1. Leakage currents in Schottky gates

Although significant progress has been achieved in GaN-based high-power/high-frequency electronic devices and ultraviolet photodetectors, surface-related problems still need an immediate solution. One of these issues is excessive leakage current through Schottky gate structures, which not only impedes device reliability but also degrades power efficiency and noise performance in such devices. In addition, del Alamo and Joh [45], Wu et al [46] and Meneghesso and co-workers [47–49] pointed out a strong correlation between the leakage current via the Schottky gate edge on the drain side and electrical as well as structural degradation of AlGaN/GaN HEMTs. They indicated that a high electric field at the gate edge under off-bias condition induces electrically active defects in the AlGaN barrier due to inverse piezoelectric effect, providing a path for excess gate current.

To control reliability and degradation issues in Schottky gate GaN HENTs, we have to clarify the underlying leakage mechanism. Yu et al [50] and Miller et al [51, 52] discussed the leakage mechanism in GaN and AlGaN Schottky interfaces on the basis of the field-emission (FE) tunneling transport assuming a triangular Schottky potential, as shown in figure 4(a). However, unreasonably higher donor densities than the actual doping concentration were required in their calculation for reproduction of the experimental data. Thus, they speculated that the excessively high leakage current is due to some other processes such as defect-assisted tunneling or variable-range-hopping conduction through threading dislocations. Other groups also suggested the trap-assisted tunneling model (figure 4(b)) to explain the leakage mechanism in the reverse bias region [53, 54]. However, such models require an unlikely multi-step tunneling process or defect continuum...
Figure 5. Schematic illustration of thin surface barrier (TSB) model. (Reprinted from [57], copyright 2004 with permission from AIP Publishing.)

with a wide energy band throughout a depletion region in the GaN or the AlGaN layer. As shown in figure 4(c), Sawada et al [55], meanwhile, suggested a surface patch model with different Schottky barrier heights to explain forward current characteristics.

Kotani et al [56] and Hashizume et al [57] proposed an entirely different model called the thin surface barrier (TSB) model for both forward and reverse current transport in GaN and AlGaN Schottky barriers. Here, it is assumed that the effective width of the Schottky barriers is reduced due to the presence of unintentional surface defect donors, and that thermionic field emission (TFE) or FE though the resultant TSB gives the major current leakage path in both forward and reverse directions, as shown in figure 5. They calculated $I-V-T$ characteristics of GaN Schottky diodes with different density distributions of surface donors. Using the TSB model, they were able to explain the temperature dependences of measured $I-V$ curves systematically. In particular, the TSB model reasonably reproduces various types of complicated $I-V-T$ behavior in the reverse bias region. The most possible surface donors are nitrogen-vacancy ($V_N$) related defects [58, 59]. It is well known that Schottky contacts fabricated on the dry-etched GaN and AlGaN surfaces showed significant leakage currents [60, 61]. Indeed, plasma-assisted dry etching processes can induce a high density of $V_N$-related defects on the GaN and AlGaN surfaces [62, 63], enhancing TFE leakage transport via the $V_N$-related level. Recently, Hayashi et al [64] reported that a 2D simulation involving the TSB model well explained the gate-drain leakage characteristics of AlGaN/GaN HEMTs in a wide range of reverse bias voltage. They clarified that a leakage path between the gate and 2DEG at the gate edge on the drain side becomes dominant under higher drain-gate bias condition due to the concentration of high electric field at the gate edge.

Suda et al [65] precisely characterized Schottky diodes fabricated on free-standing $n$-GaN substrates with a low dislocation density of $2 \times 10^6 \text{cm}^{-2}$. They measured reverse $I-V$ curves on the GaN diodes with different carrier densities, and showed that the measured curves excellently agree with the calculated curves on the basis of the TFE model without the need for fitting parameters (such as surface defect donors), as shown in figure 6. This indicates that Schottky diodes on the GaN layers with high crystalline quality (with low dislocation density) shows ideal $I-V$ characteristics according to the simple TFE model. In comparison, high leakage currents with strong bias dependence and weak temperature dependence are still observed in Schottky gates fabricated on AlGaN/GaN and InAlN/GaN structures [64, 66, 67], suggesting that the TFE transport enhanced by surface defect levels (TSB model) is dominant, which is related to relatively poor crystalline quality of thin AlGaN and InAlN barrier layers.

2.2. Current collapse

While GaN-based devices have recently reached the commercial product status, several problems still remain, and one such example of highest priority is the current collapse [68–70]. Current collapse is an important issue, because it may lead to a critically high ON-resistance ($R_{ON}$) immediately following device switching from OFF-state to ON-state. According to the widely accepted ‘virtual gate’ model [69], as shown in figure 7, a high OFF-state drain bias voltage induces electron trapping at the AlGaN surface states via a tunneling injection at the gate edge on the drain side. Subsequently, surface trapping depletes the underlying 2DEG and increases the drain resistance, leading to the increased dynamic $R_{ON}$, i.e. current collapse.

The current collapse (increase in $R_{ON}$) is strongly dependent on the drain voltage during the off-state stress [71, 72]. On the basis of the gate injection and surface-hopping model [70, 73], electron conduction via trap-to-trap hopping can be promoted with the application of increasing drain voltage. Consequently, this may lead to the widening of the ‘virtual gate’ from the gate edge until some further distance on the G–D access region. Using Kelvin probe force microscopy, Cardwell et al [74] demonstrated that trapping could extend as far as several hundred nanometers from the drain-side gate edge. After applying the off-state drain stress of 200V to the AlGaN/GaN HEMT, Katsuno et al [75] observed electric field-induced second-harmonic signal within 2 µm from the gate edge on the drain side, corresponding to surface charging region. Tajima and Hashizume [76] and Nishiguchi et al [77] investigated current collapse behavior of AlGaN/GaN
HEMTs using dual-gate structure. They showed that the off-state gate stress induces ‘virtual gates’ along both sides of the gate edges expanding toward both the drain and source directions. They also found that off-stress induced surface charging region can extend as far as 0.5 \( \mu \text{m} \) from the gate edge toward the drain side.

Several groups pointed out that an acceptor-type bulk trap in the GaN layer is one of the candidate traps that induce current collapse in AlGaN/GaN HEMTs. Nakajima et al. [78] demonstrated that a deep acceptor level is correlated with current collapse phenomena. However, their calculation result indicated that such deep acceptor with a relatively high density of \( 5 \times 10^{16} \text{ cm}^{-3} \) caused only 10% reduction of drain current after an off-state bias stress. Recently, Faramehr et al. [79] reported that the contribution of a bulk acceptor trap to off-state-induced current collapse was negligible in AlGaN/GaN HEMTs even when the GaN layer includes a bulk acceptor trap with a density of \( 2 \times 10^{16} \text{ cm}^{-3} \). There have been no reports of epitaxial GaN layers including deep levels with densities higher than \( 5 \times 10^{16} \text{ cm}^{-3} \) [80, 81]. In addition, surface passivation structure is effective in mitigating current collapse due to a relatively low state density at the \( \text{SiN}_{x}/\text{III-N} \) interface [21, 89–91]. Green and co-workers [20] were the first to demonstrate the efficacy of the \( \text{SiN}_{x} \) passivation of AlGaN/GaN HEMTs for reducing surface trapping effects, thus leading to increased output RF power. Derluyn et al. have reported that the in situ MOCVD deposition of \( \text{SiN}_{x} \) on the AlGaN surface significantly improved the DC performance of AlGaN/GaN HEMTs [92]. Meanwhile, epitaxial GaN cap layers have also been employed to modify device surface potential in order to decrease current dispersion [93–95]. While those methods have been demonstrated to be effective, current collapse still persists at high voltage switching stages even when using a combination of aforementioned schemes [85].

2.3. Threshold voltage (\( V_{TH} \)) fluctuation in AlGaN/GaN MIS HEMTs

While keeping the merits of conventional Schottky-gate-based HEMTs, i.e. a high density of 2DEG at the AlGaN/GaN interface, high cutoff and maximum frequencies, and thermal and chemical stability of AlGaN and GaN, MIS HEMTs offer many advantages over Schottky-gate-based HEMTs, such as...
lower gate leakage current, mitigation of current collapse, a wider range of allowable gate voltage sweep, and higher maximum drain current and output power. These features are crucial for applications in high-power and high-temperature electronics, particularly for realizing low on-resistance and normally-off high-power FETs.

Although various kinds of insulator materials have been applied to improve the performance of AlGaN/GaN MIS HEMTs, several problems remain unsolved. The most serious issue is the $V_{TH}$ instability. Several papers reported that different bias conditions induce varying degrees of $V_{TH}$ shifts in MIS HEMTs [96–98]. Lu et al [96] and Johnson et al [98] reported that a higher positive biasing of the MIS HEMTs induces larger $V_{TH}$ shift toward the forward bias direction. As shown in figure 8, Lu et al [96] reported from the pulsed $V_{G}–I_D$ measurement that higher gate-bias stress caused the larger $V_{TH}$ shift in their Al$_2$O$_3$-gate AlGaN/GaN HEMTs. A similar $V_{TH}$ fluctuation was also observed in SiO$_2$-or SiN-gate AlGaN/GaN HEMTs [99, 100]. Fixed charges in insulator films [101, 102], BTs in insulator films near the insulators/AlGaN interfaces [96, 99, 100] and interface states at the insulators/AlGaN interfaces are involved in the $V_{TH}$ shift mechanism. Tapajna et al [97] discussed the effect of interface states on the $V_{TH}$ shift in Al$_2$O$_3$-gate AlGaN/GaN HEMTs. Many papers reported that high densities of electronic states still exist at the insulators/AlGaN interfaces. The charging state of the interface traps varies with the gate bias (surface potential), and deeper electronic states with long time constants for electron emission contribute to a slow $V_{TH}$ fluctuation.

Yang et al [103] demonstrated that surface nitridation of GaN/AlGaN/GaN structure using remote N$_2$ plasma is effective in improving the sub-threshold gate control and $V_{TH}$ stability of Al$_2$O$_3$-gate HEMTs. Hori et al [104] reported that N$_2$O radical treatment can decrease interface states at the Al$_2$O$_3$/AlGaN interface, resulting in the improved stability of $V_{TH}$ even after applying an off-stress gate bias. Van Hove et al [105] utilized in situ SiN$_x$ as an interfacial control layer, and reported improved operation stability with a small $V_{TH}$ fluctuation in the SiN/Al$_2$O$_3$ gated AlGaN/GaN HEMTs. On the basis of a systematic characterization of interface states, further investigation is absolutely necessary to control electronic states at insulator/(Al)GaN interfaces for improved $V_{TH}$ stability of AlGaN/GaN MIS HEMTs.

### 3. Interface properties of (Al)GaN MIS structures

#### 3.1. Band lineups at insulators-(Al)GaN structures

For designing an MIS transistor or a surface-passivated transistor using a wide-gap semiconductor, it is important to understand the band lineup between the insulator and the semiconductor involved. Figure 9 shows the plot of energy gap versus specific permittivity for nitride semiconductors and insulators with a wide range of permittivity. It is a common knowledge that a higher value of dielectric constant leads to a higher value of transconductance $g_m$ in MIS transistors. In this regard, various types of gate stacks utilizing high-$\kappa$ insulators have been applied to GaN-based MIS transistors. In addition, a large band-offset energy is required at the insulator/(Al)GaN interface for the suppression of leakage current, in particular for device operation under forward bias condition. Among the insulators shown in figure 9, Al$_2$O$_3$ is one of the most attractive dielectric materials for power MIS devices because it combines all the desired properties such as large bandgap, relatively high dielectric constant, and high breakdown field (~10 MV cm$^{-1}$).

### Table 1. Experimentally obtained band offsets from GaN and AlGaN MIS structures reported in literatures.

| Structure       | Deposition method | $E_G$ (eV) | $\delta E_C$ (eV) | $\delta E_V$ (eV) | Estimation method | Reference |
|-----------------|-------------------|------------|-------------------|-------------------|-------------------|-----------|
| SiO$_2$/GaN     | JVD               | —          | 3.2               | 2.3               | F–N plot          | [108]     |
|                 | Plasma oxidation of Si | —      | 2.0               | 3.6               | XPS               | [109]     |
|                 | PEALD             | 8.9        | 3.2               | 2.3               | XPS               | [110]     |
| SiN$_x$/GaN     | ECR-CVD           | —          | 0.7               | 0.8               | XPS               | [21]      |
|                 | Plasma nitridation of Si | —      | −0.6              | 2.1               | XPS               | [111]     |
| Al$_2$O$_3$/GaN | ALD               | 6.7        | 1.2               | 2.1               | F–N plot          | [104]     |
|                 | ALD               | —          | 1.2               | 2.1               | C–V              | [101]     |
|                 | PEALD             | 6.7        | 2.1               | 1.2               | XPS               | [110]     |
| Sapphire/GaN    | MBE(GaN)          | —          | 1.7               | 3.7               | XPS               | [112]     |
| Ga$_2$O$_3$/GaN | Anodic oxidation  | —          | 0.9               | 0.6               | P–F plot          | [113]     |
|                 | EB evaporation    | —          | 1.0               | 0.3               | XPS               | [114]     |
| HfO$_2$/GaN     | Plasma oxidation of Hf | —        | −0.1              | 2.5               | XPS               | [115]     |
|                 | ALD               | —          | 0.5               | 1.7               | XPS               | [116]     |
|                 | PEALD             | 5.8        | 1.5               | 0.9               | XPS               | [110]     |
| Cd$_2$O$_3$/GaN | EB evaporation    | 5.4        | 0.55              | 1.45              | XPS               | [117]     |
| La$_2$O$_3$/GaN | MBE               | —          | 0.63              | 1.47              | XPS               | [118]     |
| SiN$_x$/Al$_2$O$_3$/GaN$_{0.75}$ | ECR-CVD | 4.9 | 0.1  | 0.7  | XPS | [21] |
| Al$_2$O$_3$/Al$_{0.75}$Ga$_{0.25}$N | Plasma oxidation of Al | 7.0 | 0.8  | 2.1  | XPS | [21] |
| Al$_2$O$_3$/Al$_{0.75}$Ga$_{0.25}$N | ALD | 6.9 | 1.2  | 1.8  | XPS | [119] |
| HfO$_2$/Al$_{0.75}$Ga$_{0.25}$N | ALD | 5.9 | 0.9  | 1.1  | XPS | [119] |
ranges from 6.7 to 7.0 eV, which is lower than that
guide dielectrics are very
high-κ dielectrics used in the insulated gate structures. On the other
hand, the resulting leakage current may arise at forward bias when these insu-
losses. Although SiO2 film has a low permittivity as shown in figure 9, it remains attractive for MIS HEMT applications because of its large bandgap and chemical stability.

As mentioned in section 3.1, the Al2O3 dielectric material has a large bandgap, a relatively high dielectric constant, and a high breakdown field. In addition, there has been substantial progress in ALD technology, simplifying the application of Al2O3 to gate and passivation structures in GaN transistors [133, 134]. In fact, Ye et al [134] first demonstrated excellent electrical characteristics, such as low gate leakage current, high drain current, high g[m] and high channel mobility, in Al2O3-gate AlGaN/GaN HEMTs. The ALD process realized good Al2O3/n-GaN interface with a low state density of around $1 \times 10^{11}$ cm$^{-2}$ eV$^{-1}$ at $E_C - 0.8$ eV [135, 136]. When using Al2O3, however, special attention should be given to subsequent process temperature. From TEM investigations, Hori et al [135] observed that the as-deposited ALD-Al2O3 layer has an amorphous-phase structure and that the Al2O3/GaN interface is uniformly flat. However, annealing at 800 °C, a typical temperature for the formation of ohmic electrodes, generated a large number of microcrystallized regions in the Al2O3 layer, causing a marked increase in the leakage current of the Al2O3/GaN structure. Toyoda et al [137] also reported that annealing procedures at 800 °C resulted in the phase transformation of Al2O3 films from amorphous to crystalline. To address this issue, a surface protection layer is indispensable to avoid the chemical bond disorder on the (Al)GaN surface during the annealing process.

Esposto et al [101] and Son et al [102] inferred that fixed charges in Al2O3 films can shift flat-band voltages in the C–V curves of the Al2O3/n-GaN capacitors. The physical origin of the fixed charges, however, is still unresolved. Choi et al [138] theoretically predicted that the oxygen vacancies in Al2O3 introduce transition levels close to the conduction band edge of GaN, and they can act as BTs at the Al2O3/n-GaN interface. On the other hand, it is also likely that other kinds of defects such as the Al vacancy and interstitial act as fixed charges in Al2O3 [138]. As for reliability of the ALD Al2O3 layer, Kikuta et al [139] reported a time-to-breakdown ($t_{BD}$) value at 3 MV cm$^{-1}$ of more than 40000 years at RT for an ALD-Al2O3 film. However, the $t_{BD}$ significantly decreased to $10^5$–$10^7$ s when temperature was raised to 250 °C.

The formation of a native oxide of AlGaN is rather appealing, because the oxidation process consumes the AlGaN
barrier layer, leading to the recessing of AlGaN and the subsequent local depletion of the 2DEG underneath the AlGaN oxide. On top of these, the native oxide of AlGaN itself can serve as a gate insulator for limiting the leakage current and for increasing the allowable gate voltage swing. These features are attractive for realizing normally-off device operation. Medjdoub et al [140] have demonstrated a normally-off AlN/AlGaN MIS HEMT with a native-oxide gate fabricated by selective dry oxidation of AlN at 900 °C. Greco et al [141] also reported that the annealing in O₂ at 900 °C produced crystalline native oxide at the AlGaN surface of the AlGaN/GaN structure. They showed that the oxidation process increased the lattice parameters as well as the mosaicity of the underlying semiconductor layers and significantly decreased the electron density at the AlGaN/GaN interface. However, aside from the fact that dry oxidation requires a high-temperature experimental condition it is very difficult for the dry oxidation to obtain an oxide of uniform thickness and a flat interface at the oxide/(Al)GaN interface [142–144]. One of the alternative techniques for the oxidation of AlGaN is by electrochemical process using low energies at RT in air. Mistele and co-workers [145] were the first to report AlGaN/GaN HEMTs with a native-oxide gate formed by the photoelectrochemical oxidation of AlGaN in a KOH-based solution. Eventually, Harada et al [146] demonstrated normally-off operation from AlGaN/GaN HEMTs with recessed-oxide-gate structure formed by selective electrochemical oxidation. The recessed-oxide-gate HEMT with an oxide thickness of 20 nm showed good gate control of drain current with a threshold voltage of +1.2 V and a flat native oxide/AlGaN interface.

3.3. Nitrides/(Al)GaN structures

SiNₓ film is widely used for surface passivation of GaN-based transistors. Hashizume et al [21, 58] demonstrated that the SiNₓ deposition on N₂-plasma treated surfaces can produce a good SiNₓ/n-GaN interface with a state density as low as 1 × 10¹¹ cm⁻² eV⁻¹ at EＣ - 0.8 eV. The reason for the low interface state densities at the SiNₓ/n-GaN interface is not yet fully understood. It is likely that nitrogen radicals generated during the SiNₓ deposition process control the formation of nitrogen-vacancy-related defects at the GaN surface [58, 59], leading to suppressed interface electronic states generation. In fact, the N₂-plasma surface treatment of the GaN and the AlGaN surface led to reduction of electronic state densities at the SiN/GaN interface [58] and improvement of device performance in SiN-passivated AlGaN/GaN HEMTs [147]. Green et al [20] were the first to apply SiNₓ passivation to the AlGaN/GaN HEMTs, and observed significant improvement of microwave output power from these devices as a consequence. SiNₓ gate was also used at AlGaN/GaN MIS HEMTs [122, 148, 149], from which significant reduction of current collapse was achieved. However, relatively high gate leakage current, in particular at forward bias, was observed in SiNₓ gate HEMTs [21, 148, 149], due to the small conduction band offset (∆E_C) between SiNₓ and (Al)GaN, as pointed out in the previous section.

The in situ deposition of SiNₓ by MOCVD is a promising process in the sense that it can be performed in the same growth chamber and in the same growth sequence as the rest of the layer stack [92]. During the final growth stage of the AlGaN/GaN structure by metal organic CVD, SiNₓ layer was in situ deposited using NH₃ and SiH₄ on the AlGaN surface at 1020 °C. Derluny et al [92] obtained improved I–V characteristics from AlGaN/GaN MIS-HEMTs with a 3.5 nm thick in situ SiNₓ gate layer. The in situ process realized an oxide-free SiNₓ/AlGaN interface [150]. From the high-resolution transmission electron microscopy (HR-TEM) analysis, Takizawa et al [151] reported that the in situ SiNₓ has a single crystalline structure. Moreover, Van Hove et al [105] have also demonstrated that an AlGaN/GaN MIS-HEMT with a stable threshold voltage and a low current collapse can be achieved using an in situ SiNₓ/Al₂O₃ bilayer gate structure.

As shown in figure 9, the AlN film is also attractive as gate insulator and surface passivation layers. Hashizume et al [152] were the first to report relatively low densities of electronic states in the range of 10¹¹ cm⁻² eV⁻¹ at the AlN/n-GaN interface. Tsurumi et al [153] demonstrated the fabrication of AlGaN/GaN HEMTs with a polycrystalline AlN surface passivation layer, taking advantage of the low thermal resistance of the AlN. They reported that the AlN-passivated HEMT showed a 30% higher drain current and a 66% lower R_S at 1020 °C compared with those of HEMTs with SiNₓ surface passivation. Recently, a monolayer-level ALD-AlN layer was used as an interfacial control layer for the Al₂O₃-gate AlGaN/GaN HEMTs [154].

3.4. High-ƙ dielectrics/(Al)GaN structures

High-ƙ insulators are attractive for achieving high g_m in MIS transistors. Recently, relatively good I–V characteristics were reported from AlGaN/GaN HEMTs with high-ƙ gate insulators [155–159]. Deen et al [155] and Kikkawa et al [156] reported high g_m values obtained from Ta₂O₅-gate AlGaN/GaN HEMTs. On the other hand, Yang et al [157] demonstrated LaLuO₃-gate AlGaN/GaN HEMTs showing good electrical performance such as high g_m, low gate leakage, small V_T fluctuation, and weak current collapse. Hatano et al [158] showed improved operation stability in AlGaN/GaN HEMTs with an Al₂O₃/ZrO₂ bilayer gate dielectric. Highly uniform epitaxially-grown NiO films prepared by MOCVD on AlGaN/GaN structure have also been reported [159]. However, the resulting NiO/AlGaN/GaN diode structure showed large leakage currents according to Poole–Frenkel mechanism, indicating the presence of electrical active defects in the MOCVD NiO [160]. Fiorenza et al [161] also reported epitaxial CeO₂ crystals grown by MOCVD on AlGaN/GaN structure. Although they observed relatively high C–V behavior, high values of leakage current were observed at forward bias for the MOS HEMT structure. Very recently, Chiu et al [162] reported CeO₂-gate AlGaN/GaN HEMTs fabricated using molecular beam deposition, and demonstrated good operation performance such as high g_m, low gate leakage, small sub-threshold swing (SS) and improved current collapse behavior. Meanwhile, Colón
and Shi [163] fabricated AlGaN/GaN MOS HEMTs using different high-κ dielectrics such as HfO\textsubscript{2}, HfO\textsubscript{2}/Al\textsubscript{2}O\textsubscript{3}, HfAlO\textsubscript{3}, and HfSiO\textsubscript{3} grown by ALD and compared their performance. Although they concluded that HfAlO\textsubscript{3} is the most promising insulating material, the HfAlO\textsubscript{3}-gate HEMT still showed a low $g_m$-pronounced current collapse and high interface state density. In addition, Deen et al [155] and Hayashi et al [164] reported severe $V_{TH}$ fluctuations from HEMTs with HfO\textsubscript{2}-gate dielectric materials while Stoklas et al [165] described similar instability issues in HEMTs with ZrO\textsubscript{2}-gate dielectric materials. Therefore, further investigation is necessary to gain better understanding of and improved performance from high-κ insulators/(Al)GaN interfaces.

3.5. Effects of pre-deposition process and post-deposition annealing on MIS interface properties

Eller et al [43] reviewed surface processing of GaN such as wet chemical treatments, vacuum-annealing processes, gas annealing processes and ion/plasma treatments in detail. We here focus on surface treatment and post-deposition annealing processes that are effective in improving GaN MIS interface properties. Hossain et al [166] investigated wet treatments in solutions using H\textsubscript{2}O\textsubscript{2}/H\textsubscript{2}SO\textsubscript{4} (piranha), (NH\textsubscript{4})\textsubscript{2}S, and 30% HF, and showed that the smallest flat-band voltage shift for the Al\textsubscript{2}O\textsubscript{3}/n-GaN sample was achieved by the H\textsubscript{2}O\textsubscript{2}/H\textsubscript{2}SO\textsubscript{4} treatment. However, the MOS samples after three processes showed almost the same values of $D_n$ of $1 \times 10^{12}$ cm\textsuperscript{-2} eV\textsuperscript{-1}. On the other hand, Chakroun et al [167] evaluated the $C$–$V$ characteristics of SiO\textsubscript{2}/n-GaN structures with pre-treatments by KOH, HCl, NH\textsubscript{4}OH and HF solutions. They reported that the treatment in KOH and HCl solutions resulted in the best RT $C$–$V$ characteristics close to the calculated curve. However, even in this sample, a hysteretic behavior was observed with gate voltage sweeping between $-3$ and $3$ V.

The H-plasma is often used to reduce native oxides and contaminants at the GaN surface. The H-plasma process, however, may simultaneously cause a chemical reaction with GaN and AlGaN surfaces to form volatile NH\textsubscript{3} groups, resulting in the formation of N-vacancy related defects and the degradation of GaN MIS interface properties [58, 59]. As described in section 3.3, on the other hand, the N-plasma treatment is effective in reducing $D_n$ in SiN\textsubscript{x}/GaN interfaces, probably due to subduction of N-vacancy related defects as well as due to a cleaning effect on the GaN surface [59]. Chen et al [168] reported that a combination of NH\textsubscript{3} and N\textsubscript{2} plasma treatments before the deposition of Al\textsubscript{2}O\textsubscript{3} by ALD significantly improved the AlGaN/GaN MOS HEMT performance due to the reduction of state densities at the Al\textsubscript{2}O\textsubscript{3}/AlGaN interface. They demonstrated that the NH\textsubscript{3} plasma treatment removes native oxides and the subsequent N\textsubscript{2}-plasma process produces N-terminated AlGaN surface with compensation of N-vacancy related defects.

A post-deposition annealing in N\textsubscript{2} is generally used for the stabilization of GaN MIS interface properties, probably due to relaxation of dangling bonds and/or point defects at the GaN surface (insulator/GaN interface) during the annealing process. As mentioned in section 3.2, a high-temperature annealing ($\sim$900 °C) was effective in achieving good SiO\textsubscript{2}/GaN interfaces with relatively low state densities [126–129]. On the other hand, the annealing temperature for the Al\textsubscript{2}O\textsubscript{3}/GaN structure is limited below 700 °C due to the phase transformation of the Al\textsubscript{2}O\textsubscript{3} film from amorphous to crystalline. Winzer et al [169] recently reported that annealing at 500 °C in O\textsubscript{2} is more efficient for decreasing interface states of the Al\textsubscript{2}O\textsubscript{3}/GaN structure than annealing at the same temperature in N\textsubscript{2}. Long et al [170] and Winzer et al [169] demonstrated that the annealing process at 400–500 °C using H\textsubscript{2}/N\textsubscript{2} forming gas was promising to passivate interface states at the Al\textsubscript{2}O\textsubscript{3}/GaN interface, correlating the passivation effect with the incorporation of H atoms at the interface. However, it was found that the forming gas annealing drastically increased leakage currents of the Al\textsubscript{2}O\textsubscript{3}/GaN structure [169].

4. Characterization of electronic states at insulator/(Al)GaN interfaces using HEMT MOS diodes

4.1. Interpretation of HEMT MIS $C$–$V$ characteristics

For practical device applications, in-depth understanding of insulator/AlGaN or insulator/InAlN interfaces using HEMT MIS structures is necessary. In this regard, precise interpretation of measured $C$–$V$ characteristics from HEMT MIS structures is a key requirement. In this regard, precise interpretation of measured $C$–$V$ characteristics from HEMT MIS structures is necessary. Although there have been many reports of low interface-trap densities in HEMT MIS capacitors, several papers have incorrectly evaluated their $C$–$V$ characteristics, underestimating the actual interface state density for wide-gap semiconductors. A HEMT MIS structure typically shows a two-step $C$–$V$ behavior [42]. However, numerous reports showed $C$–$V$ curves without the characteristics step at the forward bias regime. When the gate voltage sweeping is confined within the reverse bias region, the resulting $C$–$V$ curve often gives rise to misleadingly low density of electronic states at the insulator/AlGaN interfaces [171–173].

To interpret the typical two-step $C$–$V$ behavior, Miczek et al [174] developed a calculation tool using a numerical solver of the Poisson equation based on the 1D Gummel
algorithm, taking into account the fixed charge at the AlGaN/GaN interface originating from spontaneous and piezoelectric polarization as well as the charge in the electronic states at the insulator/AlGaN interface. Figure 12 shows an example of calculated MIS $C$–$V$ curves neglecting interface state density (ideal curves) for various insulators [175]. The characteristic two-step behavior is reproduced in the calculations. To evaluate the effects of interface states on the $C$–$V$ characteristics, Mizue et al [42], and Yatabe et al [175] carried out calculations for the Al$_2$O$_3$/AlGaN/GaN structure, taking into account state density distribution ($D_s(E)$) consisting of acceptor- and donor-like states separated by the charge neutrality level $E_{CNL}$ [106, 174, 176, 177]. They used an electron emission time constant from interface states to the conduction band, evaluated using Shockley–Read–Hall (SRH) statistics, to identify the energy range of the interface states responsible for the observed $C$–$V$ behavior [178]. At an insulator-semiconductor interface, the crystalline periodicity of the semiconductor is terminated. In addition, disorder in atomic-bond arrangement can be induced at the semiconductor surface. In this case, separation of conduction and valence bands is insufficient, resulting in the penetration of bonding and anti-bonding states into the forbidden band (bandgap) from the valence and conduction bands, respectively [176, 179]. Therefore, the charging character of interface states also reflects those of the valence and conduction bands [176]. Namely, a negative charge appears in the conduction band if a state is occupied by an electron (acceptor-like character), and valence band state is positively charged when being unoccupied (donor-like character). Thus, it can be assumed that the interface state continuum consists of a mixture of acceptor-like and donor-like states, and their branch point act as the $E_{CNL}$. This model is often used as a density distribution of interface states [43, 180, 181].

An example of the calculated $C$–$V$ curves for the Al$_2$O$_3$/AlGaN/GaN structure is shown in figure 13 [175]. In the forward bias region, the $C$–$V$ slope drastically decreases with increasing interface state density. In this bias regime, the nearly flat potential of the AlGaN layer can lead to electron transfer from the AlGaN/GaN interface to Al$_2$O$_3$/AlGaN interface. Simultaneously, electron trapping at the Al$_2$O$_3$/AlGaN interface is highly probable. The occupied acceptor-type states produce excess negative charges, which screen the applied gate electric field, suppressing the potential modulation of the AlGaN layer. This causes the stretch out of the $C$–$V$ curve in the forward bias regime, as seen in a standard MOS diode. If an insulator-AlGaN structure includes very high interface state densities, then the step 1 will not be observed even with high forward bias applied [182, 183]. On the other hand, at around the threshold bias (step 2), the Fermi level ($E_F$) is located far below the valence band maximum of AlGaN at the Al$_2$O$_3$/AlGaN interface. This makes electron occupation of interface states no longer a function of the gate bias [42, 175], leading to the absence of stretch-out behavior in the $C$–$V$ curve. In addition, the SRH statistics predicts very long time constants of electron emission from deep states to conduction band. Due to the associated long emission time constants, electrons captured in deep-lying acceptor-like traps remain trapped and act as negatively fixed charges at RT, even when a large negative bias is applied to the gate electrode. This leads to the parallel $C$–$V$ shift ($V_{TH}$ shift) at step 2 toward the positive bias direction with respect to the ideal $C$–$V$ curve, as evident in figure 13.

4.2. $D_s(E)$ estimation at insulator(Al)GaN interface

By fitting the calculation results to the experimental $C$–$V$ curves, Yatabe et al [175] reported determination of $D_s(E)$ at Al$_2$O$_3$/AlGaN interfaces in HEMT MOS structures. Figure 14 shows the comparison between the calculated and experimental $C$–$V$ curves of the Al$_2$O$_3$/AlGaN/GaN interface with and without the inductively coupled plasma (ICP) dry etching of the AlGaN surface. To evaluate near-midgap electronic states at insulator/AlGaN interfaces at RT, Mizue et al [42] have developed a photo-assisted $C$–$V$ method using monochromatic lights with photon energies less than the bandgap of the AlGaN. The basic concept of photo-ionization effects of interface states under a monochromatic light with energy less that the bandgap of AlGaN is schematically shown in

![Figure 13](image13.jpg)  
**Figure 13.** Calculated $C$–$V$ curves of 20 nm-Al$_2$O$_3$/AlGaN/GaN structure, taking into account the effect of interface electronic states. (Reprinted with permission from [175], copyright 2014 by the Japan Society of Applied Physics.)

![Figure 14](image14.jpg)  
**Figure 14.** Comparison between calculated and experimental $C$–$V$ curves of Al$_2$O$_3$/AlGaN/GaN structure with and without the ICP dry etching of AlGaN surface. (Reprinted with permission from [175], copyright 2014 by the Japan Society of Applied Physics.)
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Figure 15. Schematic illustration of (a) photo-assisted electron emission at the Al₂O₃/AlGaN interface, (b) photo-assisted C–V characteristics and (c) interface state charge and energy range corresponding to the voltage shift, ΔV, in photo-assisted C–V curves. (Reprinted with permission from [175], copyright 2014 by the Japan Society of Applied Physics.)

In this method, the first step is application of a high enough forward gate voltage (V_G) to observe the insulator capacitance under dark condition to the HEMT MOS structures. At this state, almost all of interface traps are filled with electrons under a nearly flat band condition. Then, the gate bias is swept toward a value more negative than the V_TH, where a monochromatic light with photon energy of hν₁ is illuminated to the sample surface. Consequently, this effectively induces photo-assisted electron emission from the interface states within the energy range corresponding to the photon energy range, as schematically shown in figure 15. The subsequent V_G sweeping after switching the light off results in the parallel C–V curve shift toward the reverse bias direction, corresponding to the change in the interface state charge Q_it (hν₁), because the ionized state act as a fixed charge at a bias near V_TH. Using different photon energies, a systematic C–V shift according to the photon energy can be observed, as shown in figure 15. The voltage shift difference (ΔV) between two photon energies corresponds to the interface charge difference, ΔQ_it, in the energy range Δhν. The state density can be simply estimated using the observed ΔV as given by the following equation [42]:

\[ D_d(E = E_{AV}) = \frac{C_{TOTAL} \Delta V}{q \Delta h\nu}, \]  

(1)

where C_TOTAL is the total capacitance of insulator and AlGaN while E_{AV} is the average interface energy.

Mizue et al [42] and Yatabe et al [175] reported systematic and parallel C–V shifts toward the reverse bias direction with increasing photon energy. Ozaki et al [184] also observed a similar parallel C–V shift in an ALD-Al₂O₃/n-GaN/AlGaN/GaN structure. These results indicate that the interface states near midgap or at deeper energies indeed act as fixed charges in this bias range. On the other hand, some groups have reported photo-assisted C–V characterization of MIS structures using a light source with photon energies larger than the GaN bandgap [185, 186]. In this case, holes are generated and accumulated at insulator/AlGaN and AlGaN/GaN interfaces. In addition, interaction of holes with the interface states especially at reverse bias has to be considered. This makes the charge dynamics in HEMT MIS structures complicated and the evaluation of interface state very difficult. Recently, Matys et al [187, 188] proposed a simulation method for the photo-assisted C–V characteristics, taking into account the electron-hole generation and the recombination processes as well as the hole capture process at the interface states. Comparing their calculation results to the experimental data, they were able to estimate the state density distribution at the Al₂O₃/AlGaN interface near the valance-band maximum of AlGaN.

Using the combination of the numerical fitting of C–V curves and the photo-assisted C–V method, for the first time, Yatabe et al [175] estimated the state density distribution of the Al₂O₃/AlGaN interfaces with and without the ICP dry etching of the AlGaN surface, as shown in figure 16. The sample without the ICP etching of AlGaN showed state densities of around 1 × 10^{13} cm⁻² eV⁻¹ or less near the midgap.
On the other hand, much higher state densities were obtained at the Al₂O₃/ICP-etched AlGaN interface. TEM observations revealing the surface chemistry of AlGaN during the ICP etching together with the DLTS results reported by Fang et al. [62], indicated that ICP etching caused monolayer-level interface roughness, disorder of the chemical bonds and formation of various types of defect complexes at the AlGaN surface, leading to poor C–V characteristics due to high-density interface states at the Al₂O₃/AlGaN interface. Tang et al. [189] investigated SiO₂/n-GaN-based capacitors and FETs fabricated on etched GaN surfaces by Cl₂-based ICP. They demonstrated that ICP etching increased the interface state density and decreased the field-effect mobility in the FET channel. Kim et al. [136] also reported that the ICP etching caused slight disorder of the chemical bonds at the GaN surface and monolayer-level interface roughness at the Al₂O₃/GaN interface, resulting in poor C–V characteristics due to high-density interface states including V₅-related levels.

4.3. Relevant characterization methods for HEMT MIS interfaces

The conductance method is often employed in HEMT MIS structures for analyzing interface states. Using this technique, careful attention should be given to the Eᵥ position at the insulator/AlGaN interface. For example, some papers reported conductance analysis in the reverse bias range on HEMT MIS structures [190–192]. At the reverse bias regime, however, the interface states could not be responsible for the conductance peak in the conductance–frequency (G–f) curve, because of their associated long emission time constants. Indeed, Shih et al. [193] pointed out that the conventional conductance method is viable only for a narrow range of forward bias voltages, and invalid for the analysis of deeper interface states. In addition, Ramanan et al. [194] and Yang et al. [195] pointed out that the conductance method severely underestimates state densities at insulators/AlGaN (or InAlN) interfaces when a very thin AlN interlayer is included in the heterostructures. Shih et al. [193] proposed a unique characterization method using forward-bias G–f characteristics at high temperatures. From an analysis based on the G–f–T (temperature) mapping, they estimated an energy range of interface states responding to the G–f measurement and gate-control efficiency related to an interface state density.

Frequency dispersion is one of characteristic features of an MIS gate on AlGaN/GaN heterostructures [104, 119, 196]. Fagerlind et al. [197] and Hori et al. [104] utilized the frequency dispersion characteristics of the C–V curves in the positive bias range for estimating interface state densities. They evaluated the MIS interface electronic state densities near the conduction-band edge for HEMT MIS structures. Recently, Yang et al. [195] measured temperature- and frequency-dependent C–V characteristics of Al₂O₃/GaN/AlGaN/GaN structures in the temperature range from 25 to 200 °C and in the frequency range from 1 KHz to 10 MHz. They carried out a precise analysis on interaction between interface state and conduction band at each measurement temperature using the SRH statistics, and estimated Dᵦ(E) distribution at energies from

-EC = −0.2 eV to EC = −0.8 eV. Yang et al. [195] and Ramanan et al. [194] applied a pulsed I–V method to Al₂O₃-gate AlGaN/GaN HEMTs and HfAlO-gate AlGaN/GaN HEMTs. From the \( V_{TH} \) shift induced by either changing the pulse height or the quiescent gate voltage, they were also able to estimate the \( Dᵦ(E) \) distribution in their devices.

5. Recent progress in GaN MOS interfaces and MOS transistors

Significant progress in crystal growth of GaN and its related semiconductors enables us to obtain a free-standing GaN substrate and a homo-epitaxial GaN layer on GaN substrate with a relatively low dislocation density \( (N_{DIS}) \) of \( 1 \times 10^6 \) cm\(^{-2} \) or less. Kyle et al. [198] reported a homo-epitaxial n-GaN \( (N_{DIS} = 2 \times 10^6 \) cm\(^{-2} \) with a carrier density of \( 3.7 \times 10^{16} \) cm\(^{-3} \) showing a mobility of 1265 cm\(^2\) V\(^{-1}\) s\(^{-1}\) at RT and
3320 cm$^2$ V$^{-1}$ s$^{-1}$ at 113 K. Kizilyalli et al [199] fabricated p$^+$n junction on a GaN substrate with $N_{DIS} = 1 \times 10^4$ cm$^{-2}$. The net doping density, $N_D - N_A$, and the thickness of the n-type drift layer were 2.0–5.0 $\times 10^{15}$ cm$^{-3}$ and 40 $\mu$m, respectively. They obtained a high breakdown voltage over 4 kV and low leakage currents at reverse bias up to the breakdown voltage. Hu et al [200] also reported excellent properties of GaN p$^+$n diodes grown on a GaN substrate with a dislocation density of $\sim 10^6$ cm$^{-2}$. The p$^+$n diode with an 8 $\mu$m drift layer ($N_D - N_A = 2.5 \times 10^{15}$ cm$^{-3}$) showed a blocking voltage of over 1.4 kV and an $R_{ON}$ of 0.12 m$\Omega$ cm$^2$, giving the highest figure-of-merit ever reported in any semiconductor system. In addition, as described in the section 2.2, Schottky diodes on the GaN layers with a low dislocation density shows ideal $I$–$V$ characteristics according to the simple TFE model. These results indicate highly improved crystalline quality of the current n-GaN epitaxial layers grown on GaN substrate.

The improved crystalline quality of GaN on GaN also has become a driving force for developing vertical-type GaN MIS transistors. Kanechika et al [201] reported a vertical GaN transistor with a combination of an MOS HEMT channel and a p-GaN blocking layer, as shown in figure 17(a). In this device, they used a selective regrowth of AlGaN/GaN layer and an SiO$_2$ gate structure. Chowdhury and co-workers [202, 203] reported a similar device using a Mg-implanted blocking layer and a SiN gate structure. Kodama et al [204] successfully fabricated a trench-type GaN MOSFET. For the trench structure, they used a combination of ICP dry etching and subsequent wet etching with tetramethylammonium hydroxide (TMAH). Recently, Oka et al [205] also reported a trench-type GaN MOSFET (figure 17(b)), demonstrating a blocking voltage over 1.2 kV, $V_{TH}$ of 3.5 V and $R_{ON}$ of 1.8 m$\Omega$ cm$^2$. It was expected that an ALD-deposited SiO$_2$ gate on the dry-etched p-GaN surface could realize device operation with an inverted channel. However, the $V_{TH}$ was much lower than the expected value calculated using the Mg doping density and the gate capacitance. The development of processing technologies such as ion implantation and healing of surface damage will improve the device performance of trench-type GaN MOSFETs.

A key issue for vertical type GaN MISFETs is still control of MIS interfaces. In this regard, we here introduce a stable GaN MOS interface with low densities of electronic states. Figure 18 shows the Al$_2$O$_3$/n-GaN/n$^+$-GaN structure. These results indicate highly improved crystalline quality of the current n-GaN epitaxial layers grown on GaN substrate.

![Topical Review](image)

**Figure 18.** Schematic illustration of Al$_2$O$_3$/n-GaN/n$^+$-GaN structure.

![Topical Review](image)

**Figure 19.** $C$–$V$ characteristics of Al$_2$O$_3$/n-GaN/n$^+$-GaN MOS diodes (a) without and (b) with post-deposition annealing process obtained in wide measurement frequency range from 1 Hz to 1 MHz at RT.
reverse bias voltage of \(-10\) V, as shown in figure 19(b). The \(C-V\) curves of the bias-annealed sample are very close to the calculated curve (broken line) in a very wide frequency range of \(1\) Hz–\(1\) MHz. In addition, there was no hysteresis in the \(C-V\) curve at RT with back and forth sweeping of gate voltage between \(-10\) and \(10\) V. Moreover, the \(C-V\) characteristics at \(200\) °C remained almost unchanged, as compared to the \(C-V\) curves at RT.

Although the reason for the improved \(C-V\) behavior after the reverse-bias annealing is not clarified yet, we think that relaxation of dangling bonds and defects at the GaN surface is enhanced under reverse bias condition. In III–V semiconductors with ionic bonding nature, deep levels or gap states often have strong interaction with the host lattice, e.g. EL2 level in GaAs and DX center in AlGaAs [206, 207], because of their localized wave functions. In this case, an electron occupation state (capture or emission of electron) at a deep level can be coupled with neighboring lattice vibration, causing lattice relaxation or distortion. During the reverse-bias annealing at \(300\) °C, it is expected that interface states and surface defect levels are empty of electrons. This can change bonding configuration of neighboring atoms, thereby leading to enhanced relaxation of dangling bonds and defects at the \(Al_2O_3/GaN\) interface. In case of the annealing at \(300\) °C under forward bias condition \((V_G = +5\) V), we confirmed that the interface state density distribution was almost the same with that of the sample with the post-deposition annealing. Thus the electron occupation condition of interface states during the annealing process is an important factor for controlling interface state densities. Further study is necessary to understand the passivation mechanism on interface states.

These results indicate that the present process realizes a stable MOS interface with low interface state density less than \(1 \times 10^{11}\) cm\(^{-2}\) eV\(^{-1}\) at around \(E_C = 0.5\) eV, when the MOS structure is fabricated on a high-quality GaN layer with a low dislocation density. However, during fabrication of a practical MOSFET, the GaN surface is usually subjected to dry-etching, ion-implantation and a high-temperature annealing processes. As mentioned in the previous section, these fabrication steps degrade MOS interface properties, i.e. increasing interface state densities or generating surface defects on the GaN surface. The next (final) step is the interface control of an insulated gate on the processed GaN surface.

As for HEMT devices, some control processes have been applied to insulated gate structures. Several groups [184, 208, 209] reported relatively good \(C-V\) characteristics and FET performances of MIS (MOS)-HEMTs using insulator-GaN/AlGaN/GaN structures with a thin GaN cap layer, which are compatible to those of insulator-AlGaN/GaN structures. Recently, Šapajna et al [196] reported almost same \(D_A\) distribution for \(Al_2O_3\)-HEMT structures with and without a GaN cap layer. Van Hove et al [105] and Ronchi et al [210] demonstrated AlGaN/GaN HEMTs with stable threshold voltage \((V_{TH})\) and weak current collapse achieved using an \(in\ situ\) SiN/ALD-Al\(_2\)O\(_3\) and an \(in\ situ\) SiN/PEALD- SiN\(_2\) bilayer gates. Chan et al [211] reported that (Al, Si)/O dielectric grown by MOCVD was attractive for achieving GaN MOS structures with low interface state densities. Liu et al [154] and Yang et al [212] applied a monolayer AlN as an interfacial layer to AlGaN/GaN MOS HEMTs with an ALD-Al\(_2\)O\(_3\) gate, as shown in figure 20. They demonstrated small frequency dispersion in \(C-V\) characteristics of Al\(_2\)O\(_3\)/AlN/AlGaN/ GaN MOS diodes and a small \(V_{TH}\) shift in AlGaN/GaN MOS HEMTs. Application of insulated gates to InAlN/GaN HEMTs also leads to significant reduction of gate leakage currents and improvement of cutoff and maximum oscillation frequencies [213–215]. To control the \(V_{TH}\) fluctuation in a normally-off HEMT, Nakazawa et al [216] demonstrated an Al\(_2\)O\(_3\)-gate AlGaN/GaN HEMT fabricated without using dry etching process. They carried out a selective regrowth of AlGaN on 5 nm AlGaN/GaN epi-layer in the source/drain and related access regions, and reported less \(V_{TH}\) shift compared with the conventional recess-gate MOS HEMT fabricated by ICP dry etching.

Recently, Guo and del Alamo [217] carried out positive-bias temperature instability (PBTI) measurements on normally-off AlGaN/GaN MIS HEMTs using SiO\(_2\) and Al\(_2\)O\(_3\)/ SiO\(_2\) as dielectric films, e.g. precise evaluation of changes in \(V_{TH}\), SS and gate leakage current after applying positive bias stress to MIS HEMTs. They demonstrated that characteristics of the \(V_{TH}\) shift and the SS increase induced by the positive bias stress are similar to those observed in Si, SiC and conventional III–V MOSFETs. Consequently, they proposed that such instability issues arise from two mechanisms: electron trapping in the oxide and generation of interface states at the oxide/GaN interface. Meanwhile, Meneghesso et al [218] reported significant correlation between the \(V_{TH}\) shift and the leakage current under the positive bias stress of AlGaN/GaN MIS HEMTs with SiN\(_x\) and Al\(_2\)O\(_3\) dielectrics, pointing out that a possible reason for the \(V_{TH}\) shift is electron trapping in the dielectric. Wu et al [219] also measured PBTI characteristics in recessed/insulated gate AlGaN/GaN MIS HEMTs with plasma-ALD SiN\(_x\) and ALD Al\(_2\)O\(_3\). They reported that gate dielectric defects inside the SiN\(_x\) are much more easily accessible under lower positive bias stress compared with Al\(_2\)O\(_3\) gate dielectric, indicating that Al\(_2\)O\(_3\) gate dielectric is indeed promising for improving the PBTI reliability. From the time-dependent dielectric breakdown (TDD) measurement, Takashima et al [131] reported that the reliability of ALD-SiO\(_2\)/GaN structures were related to the surface treatment process of GaN before the SiO\(_2\) deposition. Kachi [4] pointed out
that the TDDB lifetime of ALD Al2O3 at the electric field of 3 MV cm⁻¹ is more than 20 years, and hence it is applicable to power devices for automotive applications. Meneghesso et al [218] also measured the TDDB characteristics of AlGaN/GaN MIS HEMTs with SiNₓ and Al₂O₃ dielectrics. Since time to failure of devices indicated a Weibull distribution with slopes larger than 1.0, they demonstrated high robustness for ALD SiNₓ and Al₂O₃. For practical applications, stability and reliability characterization of GaN-based MIS transistors is becoming more and more relevant and important.

6. Summary

Although recent years have witnessed GaN-based devices delivering their promise of unprecedented performance and demonstrating their capability as an able replacement for Si-based devices, a practical and reliable approach towards associated stability and reliability issues should be developed. For widespread implementation and commercialization of GaN-based transistors, it is becoming undeniable that the MIS structure will play a major role.

For practical transistor applications, low leakage current, dependable current control, stable threshold voltage, high µm and wide dynamic range of input voltage are required from an MIS system. In view of these points, various GaN MIS structures were reviewed and discussed, particularly focusing on interface states that are deeply related to stability issues of MIS transistors. As for insulated gate applications, SiO₂ and Al₂O₃ are considered attractive insulator materials due to their favorable dielectric properties such as large bandgap and high chemical stability. With suitable pre-deposition treatment and post-deposition annealing, stable SiO₂/GaN and Al₂O₃/GaN structures with low interface state densities using epitaxial GaN crystals can be achieved as reported in literature. The remaining issue is the interface control of the MOS structures fabricated on the processed GaN surfaces such as those subjected to dry-etching, ion-implantation and high-temperature annealing steps. Although the bandgap of SiNₓ (≈5.0 eV) is not sufficiently large for the insulated gate application, SiNₓ is an important material for surface passivation of GaN-based transistors. In particular, in situ deposition of SiNₓ during the MOCVD growth process can improve the operation stability of GaN HEMTs. Various types of high-κ insulators have also been applied to the gate structures of GaN transistors. However, further investigation on chemical stability and interface properties of high-κ/GaN structures is still needed.

For a MIS gate structure application to AlGaN/GaN or InAlN/GaN heterostructures, characterization of electronic state properties at the insulator/AlGaN (InAlN) interfaces critical to device operation is very important. On this account, we reviewed pertinent results from literature including accurate C–V calculation, photo-assisted C–V, conductance, frequency- and temperature-dependent conductance, frequency-dependent C–V and pulsed I–V methods. Using the combination of numerical fitting of C–V curves and photo-assisted C–V method, the state density distributions of the Al₂O₃/AlGaN interfaces were determined in the energy range between EC and midgap.

In summary, in this work, we have described critical issues and problems including leakage current, current collapse and threshold voltage instability in GaN-based HEMTs. The nature and characteristics of different AlGaN/GaN MIS structures essential for achieving successful surface passivation and interface control schemes were also discussed. Lastly, we highlighted important current progress in GaN MIS interfaces that have recently pushed the frontier of nitride-based device technology. On the final note, nevertheless, we believe that further investigation and understanding of interface states are absolutely necessary for achieving reliable and unquestionable operation stability in GaN-based MIS transistors including MIS HEMTs.

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