Calibration and performance of the readout system based on switched capacitor arrays for the Large-Sized Telescope of the Cherenkov Telescope Array

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ABSTRACT

The Cherenkov Telescope Array (CTA) is the next-generation ground-based very-high-energy gamma-ray observatory. The Large-Sized Telescope (LST) of CTA is designed to detect gamma rays between 20 GeV and a few TeV with a 23-meter diameter mirror. We have developed the focal plane camera of the first LST, which has 1855 photomultiplier tubes (PMTs) and the readout system which samples a PMT waveform at GHz with switched capacitor arrays, Domino Ring Sampler version 4 (DRS4). To measure the precise pulse charge and arrival time of Cherenkov signals, we developed a method to calibrate the output voltage of DRS4 and the sampling time interval, as well as an analysis method to correct the spike noise of DRS4. Since the first LST was inaugurated in 2018, we have performed the commissioning tests and calibrated the camera. We characterised the camera in terms of the charge pedestal under various conditions of the night sky background, the charge resolution of each pixel, the charge uniformity of the whole camera, and the time resolutions with a test pulse and calibration laser.

Keywords: Cherenkov Telescope Array, Large-Sized Telescope, calibration, switched capacitor array, DRS4

1. INTRODUCTION

The Cherenkov Telescope Array (CTA) is the next-generation ground-based observatory for very-high-energy gamma rays. The CTA consists of three types of telescopes with different mirror areas to cover a wide energy range (20 GeV–300 TeV) with an order of magnitude higher sensitivity than the predecessors. Among those telescopes, the Large-Sized Telescope (LST) is designed to detect low-energy gamma rays between 20 GeV and a few TeV with a 23 m diameter mirror. To make the most of such a large light collection area (about 400 m²), the focal plane camera must detect as much reflected Cherenkov light as possible. We have developed each camera component to meet the CTA performance requirements for more than ten years and performed quality-control tests before installing the camera to the telescope.

The first LST (LST-1) was inaugurated in October 2018 in La Palma, Spain (Figure 1). After the inauguration, various calibration tests were performed to adjust hardware parameters and verify the camera performance. In parallel, we have been developing the analysis software to extract physical parameters from low-level data, taking into account some intrinsic characteristics of the switched capacitor arrays, Domino Ring Sampler version 4 (DRS4), used for sampling the waveform of a Cherenkov signal. In this contribution, we describe the hardware design of the LST camera in Section 2, a procedure for low-level calibration in Section 3, and the readout performance of the LST camera after the hardware calibration with a dedicated analysis chain in Section 4.

2. HARDWARE DESIGN OF THE LST CAMERA

2.1 Overview

Figure 2 (left) shows a frontal view of the focal plane camera of the first LST. The camera has 1855 photomultiplier tubes (PMTs) organized in 265 modules, which are seven-pixel units shown in the Figure 2 (right). Each module has seven PMTs with light guides, a slow control board, a readout board based on DRS4, a trigger mezzanine,
Figure 1. The first Large-Sized Telescope (LST-1).

Figure 2. The focal plane camera of the LST-1. Left: A frontal view of the camera. Right: A PMT module before installing in the LST-1 camera. Each PMT is equipped with a light guide, and seven PMTs are connected to a readout board based on the DRS4 chip. A trigger mezzanine is attached to the backside of the readout board. Backplane boards are located on the backside of the camera cabinet, and attached to the modules after module installation.

and a backplane board. Besides, a single Trigger Interface Board (TIB) and a cooling system are in the LST camera structure.

Figure 3 shows a block diagram of the readout system. For detecting Cherenkov lights, each module has seven PMTs with light guides. A high voltage for each PMT is generated by the Cockcroft-Walton circuit controlled by the slow control board. The anode current signal from each PMT is converted to voltage by the current-mode pre-amplifier designed for the CTA, and connected to the readout board based on DRS4 chips. Those signals are split into three lines with different main amplifiers on this readout board: a high-gain channel, a low-gain channel, and a trigger channel. The high-gain channel is more important to detect dim air showers and achieve lower energy threshold of the LST. In addition to the high-gain channel, it can achieve a wide dynamic range between 0.1 and more than 1000 photoelectrons (p.e.) by using the low-gain channel.

The amplified signals need to be sampled at \( \sim 1 \text{ GHz} \) to suppress the contamination from the O(ns) night-sky background (NSB) to shower images. A modern flash analog-to-digital converter (FADC) can sample waveforms continuously at GHz rates. However, a FADC is expensive in general and has a high power consumption with large heat dissipation. Therefore, we adopted DRS4 chips instead of FADCs to achieve the GHz waveform sampling with low power consumption. The DRS4 chips constantly sample the waveform of signals on the low-gain and high-gain lines at 1 GHz frequency. The sampled signal is digitized by an external low-speed analog-to-digital converter (ADC) after the readout board receives the trigger signal.

In parallel, two levels of event triggering are performed with the LST camera. Trigger channel signals are transferred to the analog trigger mezzanine and combined in each module (level 0). The combined signals are sent to neighboring modules through backplane boards. The signals from three modules are combined to generate a digital trigger pulse with a dedicated threshold for each module (level 1). When the level 1 camera
trigger is generated on the trigger mezzanine board, this digital trigger signal is propagated to the central module through backplane boards and sent to the Trigger Interface Board (TIB) connected to the central one. The TIB in each telescope has a common timing reference and share the trigger signal among multiple telescopes to generate a stereo trigger in a given small coincidence time window. The TIB waits for the $\sim 4 \mu s$, which are needed to generate the stereo trigger, then sends the trigger back to the central module. This trigger is propagated to all of the modules from the central one. The synchronicity of trigger reception in all modules is asserted by adding individual, calibrated delays to the central trigger signal on each backplane board.

When a field-programmable gate array (FPGA) on the readout board receives the trigger signal, it stops the DRS4 sampling and reads out the stored charges. The analog output from DRS4 is digitized by an external 33 MHz ADC chip with a 12-bit resolution (0.24 mV/ADC). The digitized data blocks are sent to the FPGA and transferred to a data acquisition (DAQ) server through four 10 Gb ethernet links for each telescope by using the SiTCP protocol. The DAQ server receives the data from all of the modules and also other event information such as the trigger and the absolute time from other subsystems, and builds complete single telescope events. Central CTA DAQ software gathers the complete events from the telescopes, then compresses and stores them in ZFITS format. Those raw data can be analyzed by low-level data processing algorithms for the CTA, ctapipe, and a dedicated analysis chain for the LST, lstchain.

The main calibration tool of the LST-1 is the calibration laser box located at the center of the mirror structure. The laser generates UV pulses with a pulse width of 400 ps at full width at half maximum, and the laser intensity can be controlled by using neutral density filters. The calibration laser is used for a dedicated calibration run before the standard observations and for taking interleaved calibration events during the observations at a low rate.

2.2 DRS4

The Domino Ring Sampler ASICs have been developed at the Paul Scherrer Institute (PSI), Switzerland, for the MEG experiment. The latest version, DRS4, is also used in the MAGIC experiment. The DRS4 chip has nine differential input channels with 950 MHz bandwidth. Each channel has 1024 storage capacitors whose write switches are operated via a chain of inverters, called a domino wave circuit. The sampling speed can be changed from 700 MHz up to 5 GHz according to the reference clock from the FPGA. This reference clock is based on an external 10 MHz clock signal propagated from the TIB through the backplane boards. By the common clock, all the DRS4 chips of the LST camera are completely synchronized. It is possible to cascade up to eight DRS4 channels for a deep sampling depth. Cascading is realized in the following way; there is an 8-bit register in the chip, each bit of which corresponds to one DRS4 channel. A channel is activated only when the corresponding
bit of the register is high. The sampling depth can be summed by connecting the same signal line to multiple channels of DRS4, then activating them one after another. For the LST, four DRS4 channels are cascaded, which means the signal of each input is sampled in 4096 capacitors and the sampling depth is \( \sim 4 \) \( \mu \)s in the case of 1 GHz sampling. Eight DRS4 chips are mounted on the readout board, and each chip is connected to two PMT channels. We use a region of interest (ROI) mode to read the stored signals from a part of the capacitors. We set a size of an ROI to 40 capacitors (40 ns) to reduce the dead time.

3. CALIBRATION METHOD OF DRS4 OUTPUT DATA

The low-level calibration for some intrinsic features of DRS4 is required to correctly estimate the charge value and arrival time of each PMT signal from raw data. Hereafter, we assume that the pulse height of a single photoelectron signal at a high gain channel is about 25 ADC counts (6 mV).

3.1 Time Lapse Correction and Baseline Subtraction for Individual Capacitors

There are two corrections to calibrate the DRS4 pedestal values: a time-lapse correction and a cell-wise baseline correction. The pedestal values are related to the time lapse from the last readout of each capacitor (\( \Delta T \)). Figure 4 (left) shows a relation between \( \Delta T \) and pedestal values. It is known that this relation can be well fitted by a power-law function.\(^{25}\) Each DRS4 chip has common fitting parameters to all capacitors, and those parameters mildly depend on individual DRS4 chips. We can compensate for this effect using this fitting function. This feature disappears and the time lapse correction is not needed when \( \Delta T \) is larger than around 60 ms. To find the cell-wise pedestal, it is needed to apply this correction with nominal parameters to remove the \( \Delta T \) dependence or to use only data with larger \( \Delta T \). Figure 4 (right) shows the pedestal values of each capacitor in a single domino chain (1024 capacitors). It is well known that there is a step structure in the distribution, with the 511th cell as a boundary. The differences of those pedestal values between the capacitors are much larger than the noise in a single capacitor.

Those parameters depend on the temperature. Figure 5 (left) shows a relation between temperature and relative cell-wise pedestal values. The temperature in a chamber is controlled from 10\(^\circ\)C to 50\(^\circ\)C at laboratory and measured with a sensor on the readout board. The mean gradient with respect to the temperature is 0.5 ADC/\(^\circ\)C. The cooling system can maintain the temperature inside the camera within ±5\(^\circ\)C, which allows the pedestal values to be kept stable at ±0.6 mV, corresponding to ~0.1 p.e. at a high gain channel. Figure 5 (right) shows \( \Delta T \) curves for different temperatures. Those curves approach zero with larger \( \Delta T \) at higher temperatures.

To prepare the parameters of the fitting function for the time lapse correction and cell-wise pedestal, a dedicated pedestal data with a random Poisson trigger is needed. If triggers are generated at a constant frequency,
it causes structures in the last reading time of individual capacitors due to the folding of the frequency of triggers with the sampling frequency of DRS4 chips (beating effects). On the other hand, random triggers could give more similar conditions to what happens during the standard observations when the shower triggers are generated following Poissonian statistics. A random trigger can be generated in FPGA on the readout boards based on random numbers generated by a linear feedback shift register. The frequency of the random trigger can be controlled by slow control commands, and 2 kHz is used for the pedestal run to cover various $\Delta T$. This dedicated pedestal run is performed daily after powering up the camera, when temperature is sufficiently stable.

3.2 Spike Correction

Two consecutive cells in ROI have a spike feature under a certain condition as shown in Figure 6 (left). The spike height is always 40–50 ADC counts, corresponding to 1–2 p.e.. The position of the spike depends on the last capacitors recording signal in the previous event. Although the reason for this feature is not interpreted perfectly, it is suggested that those spikes could be caused by remaining read bits at the previous readout. Figure 6 (right) shows the relation between the position of spike cells and the last capacitors recording signal in the previous readout window. The spike cells are defined as ones which have higher ADC counts than 15 ADC in this figure. Since this relation is predictable, and these features appear without exceptions, we can compensate for this feature by interpolating between neighbor cells or subtracting ADC counts corresponding to the pulse height. DRS4 chips on all of the modules are running based on the common clock reference, and domino waves of all DRS4 chips are basically synchronized as described in Section 2.2. Thus, a similar region of capacitors in the domino wave of all pixels is read out for every event. It is possible that most of the pixels have such spike cells in the readout window when the conditions are fulfilled.

In this Figure 6 (right), a periodic pattern is also seen at every 32nd capacitor, which was already known in the MAGIC experiment. This feature seems to be related to the structure of DRS4 chips, which is segmented into 32 parts with 32 capacitors for each channel. Those capacitors sometimes have larger ADC counts. Though it is difficult to predict the condition and correct it, we revealed that this effect is shown only when $\Delta T$ is larger than about 100 ms. This effect is therefore negligible at a standard trigger rate (9–10 kHz) for the observation.

3.3 Pulse Peak Time Correction

A sampling frequency in a DRS4 chip is not perfectly constant. Each capacitor has a cell-wise fixed sampling interval in addition to a small random jitter. This interval varies from one capacitor to another by about 10%. Basically, a timing calibration of switched capacitor arrays to obtain the individual sampling intervals needs a reference signal such as a sine wave. However, there is no such equipment on the readout boards. We have thus developed alternative methods for a pulse peak time correction and an integrated charge correction individually.
Figure 6. Spike features of the DRS4 chips. Left: Waveform of seven channels including spike cells. Right: Relation between the spike cell ID and the last capacitor ID in the readout windows of the previous events. Those cell IDs are computed by an operation of modulo 1024. There are predictable consecutive spikes (blue) and unpredictable ones (orange) at every 32nd capacitor (gray dotted lines).

Figure 7. Relation between the pulse peak time and the first capacitor ID in a readout window of a given pixel. Red crosses show the mean peak time in each binning, and those data points are expanded into a Fourier series (yellow line).

If we assume constant sampling frequency contrary to the fact, a pulse peak time depends on a readout position in the domino wave. Figure 7 shows a relation between the first capacitor id of the readout window and the pulse peak time with the assumption of constant sampling intervals. Since this relation is common for each channel on the same DRS4 chip, the first capacitor id is folded into modulo 1024. The dispersion of the pulse peak time depending on the first capacitor corresponds to integrated sampling intervals at each part of the domino ring between the first capacitor in the readout window and pulse peak position. In the case of calibration-laser events used for this method, the laser signal is located at the center of the readout window. Thus, we can correct these sampling intervals of \( \sim 20 \) capacitors by using a Fourier series expanded from this relation. This relation depends on the pulse position in the readout window because a number of capacitors in front of the pulse peak is different. Therefore, we are currently developing a method to correct the pulse peak time independent of the pulse position in the window.
3.4 Integrated Charge Correction

The sampling inhomogeneity described in the previous section also affects the integrated charge, which is the product of ADC counts and time. Instead of using the individual sampling intervals, we use a method using test pulses to find the weighting factor for the charge integration instead of the sampling intervals. Figure 8 shows a concept of the method to obtain the weighting factor. Firstly, we need test pulse data with large statistics (one million of events allows the accuracy of \( \sim 3\% \)). Those test pulses must be driven by clocks which are different from the one used for DRS4, in order to avoid synchronisation between test pulses and domino waves, sweeping uniformly the relative time between both. With those test pulse events, we count the number of events for each capacitor that has a peak. In the ideal case, the i-th capacitor has a peak when the actual pulse peak is located between a middle of sampling interval of the i-th capacitor and one of the neighboring capacitor. We will use the ratio of this number to the total number of events as a weighting factor. When we define this weighting factor as \( w_i \) and sampling interval as \( t_i \) of the i-th capacitor, those relations are explained by the Equation (1).

\[
w_i = \frac{t_i + t_{i+1}}{2} \times \frac{\text{a number of events with a peak at the i-th capacitor}}{\text{a total number of events}} \times 1024 \text{ ns}
\]  

To compensate for the uneven sampling time intervals, we have only to integrate the product of ADC counts and the weighting factor for each capacitor. This procedure corresponds to a trapezoidal integration of waveforms as shown in the Equation (2).

\[
\text{Charge} = \sum_{i=n}^{n+m} \frac{ADC_i + ADC_{i+1}}{2} \times t_{i+1} \sim \sum_{i=n}^{n+m} \frac{t_i + t_{i+1}}{2} \times ADC_{i+1} = \sum_{i=n}^{n+m} w_i \times ADC_i
\]  

This inhomogeneity does not have a large effect for small numbers of photoelectrons because the statistical uncertainty is much larger than one from this effect. On the other hand, this correction is important to evaluate the charge of a large signal, especially above a thousand photoelectrons. Since it strongly affects the spread of the charge distribution of such signals, it can bias the excess noise factor method.  

4. READOUT PERFORMANCE

4.1 Noise Level

We evaluated a standard deviation of pedestal value as an index of a noise level after the dedicated corrections described in Section 3. Figure 9 (left) shows the distribution of pedestal ADC at each cell after each correction step. Each step of the correction works well to compensate each component, and the standard deviation of the pedestal at the high gain channel is 7.0 ADC counts (0.28 p.e.) after all corrections. Since the charge value is derived from the integration of ADC values among multiple cells, we investigated the effect of a number of integrated cells on the standard deviation of the pedestal. Figure 9 (right) shows the standard deviation of the pedestal integrated with different numbers of cells. Here, we evaluated the standard deviation of the pedestal as one divided by a square root of the number of integrated cells assuming that the noise is not correlated. If noise components are random, this parameter should be the same with a different number of integrated cells. However, this parameter is higher with more integrated cells. A possible reason is that some noise components have a lower frequency than the charge sampling rate. The eight-cell integration is used to derive the charge of Cherenkov signal for the standard analysis. Hereafter, the eight-cell integration is used to evaluate a noise level.

Figure 10 (left) shows a distribution of pedestal value with the eight-cells integration among all pixels in the camera without a high voltage applied to PMTs. The mean value is 18.2 ADC counts, which corresponds to 0.21 p.e., assuming that a charge value of a single photoelectron signal is 80–90 ADC counts. This noise component is contributed only by electronics. On the other hand, background light are the dominating source of noise during standard observations. Figure 10 (right) shows the standard deviation of the pedestal with a high voltage applied to PMTs under the different NSB levels. Due to three types of attenuation factors, which are different pixel by pixel, we used the normalized anode current divided by the attenuation factor of each pixel to
Figure 8. Concept of the method to find the weighting value with test pulse. Three test pulses are shown as dotted lines (black, blue, green), and sampled data points at each capacitor are shown as circles. Peak points of each waveform are indicated by filled circles, and others are indicated by open circles. In the ideal case, the i-th capacitor have peak points when test pulse peaks are located between a middle of sampling interval of the i-th capacitor and one of the neighboring capacitor (gray shadow region). In this figure, such cases correspond to blue and green pulses. The probability that the i-th capacitor have peak points corresponds to a ratio of gray shadow region to sum of sampling intervals of all capacitors.

Figure 9. Left: A pedestal distribution with a unit of ADC counts at each cell after each step of the corrections: pedestal subtraction (blue), $\Delta T$ correction (orange), and spike correction (green). Right: Standard deviations of the pedestal by integrating different numbers of cells for the high gain (blue) and the low gain (orange) channels. Error bars on each point show the standard deviation of this parameter among all 1855 pixels in the LST-1 camera.
evaluate the relationship with the same parameters for all pixels. A fitting function indicates that this relation is well described by a square-root function with an offset. The fitting parameters are almost the same among all pixels. This relation holds even at 10 times higher than the dark NSB level.

### 4.2 Charge Uniformity

For a homogeneous response of the camera, it is needed to adjust high voltages for all pixels to get the same amount of output charges from PMTs against the calibration laser. This procedure is called high-voltage flat-fielding. Figure 11 shows the charge distribution at a high-gain channel before and after the high-voltage flat-fielding in the same night in August 2020. The standard deviation of this distribution with the calibration laser was improved by the high-voltage flat-fielding from 3.0% to 1.9%. The previous high-voltage flat-fielding was performed in January 2020 and the PMT gain was varied after that time.

### 4.3 Charge Resolution

Figure 12 shows the charge resolution of all pixels at both high-gain and low-gain channels with test pulses before and after the timing correction described in Section 3.3. We used test pulses with an amplitude of 60–70 p.e. for high-gain channels and ~1000 p.e. for low-gain channels. The charge resolutions at the high-gain and low-gain channels are 6–8% and 4–6% before the correction and 3–5% and 2–3% after the correction, respectively. This sampling interval correction improved the charge resolutions of all pixels.

### 4.4 Time Resolution

Figure 13 (left) shows a distribution of pulse peak time with a calibration laser at a given pixel before and after peak time corrections. The pulse peak is given by the center of gravity between eight cells around the peak. Before the correction, the standard deviation is 1.7 ns. After the relative correction described in Section 3.3, the standard deviation is improved to 0.9 ns. Absolute correction is done to compensate for the effect of timing jitter of the trigger or the calibration laser itself by subtracting the mean peak time among all pixels in the camera for every event. Figure 13 (right) shows a distribution of the standard deviation of pulse peak distributions for all pixels in the camera after each step of the correction. Before the correction, the distribution has a tail.
Figure 11. Mean charge value with calibration laser data before the high-voltage flat-fielding (blue) and after the high-voltage flat-fielding (orange).

Figure 12. Charge resolutions of all pixels measured with test pulses at high gain channels (left) and low gain channels (right) before and after the sampling interval correction.
component with poor time resolution. Those components disappeared after the correction. The mean value of this distribution referred to as time resolution is 1.0 ns after the relative correction and 0.4 ns after the absolute correction.

5. SUMMARY
We have developed the focal plane camera, which has 1855 PMTs and readout boards based on the ultra-fast waveform sampling DRS4 chips. The first LST was inaugurated in October 2018 in Spain, and various hardware calibration tests were performed. In parallel, we have been developing the analysis chain to compensate for the intrinsic features of the DRS4 chips. For this low-level calibration, it is firstly needed to extract parameters on the pedestal values for the time-lapse correction and cell-wise pedestal subtraction from the dedicated pedestal run with the random trigger. Furthermore, spike correction is also needed to remove the consecutive two spike cells. Sampling time inhomogeneity makes an effect on charge integration and pulse peak extraction. Thus, it is needed to prepare weighting factor and Fourier expansion parameters, respectively.

After the dedicated low-level calibration, we evaluated the readout performance of the camera. The noise level of the readout board corresponds to 0.21 p.e. with 8-cell integration. Mean charge distribution taken with a calibration laser has a standard deviation of 1.9% after the high-voltage flat-fielding. We confirmed that the sampling inhomogeneity correction is working well, and the charge resolution with test pulses is around 2–4% after the correction. After the peak time correction to compensate for the chip-dependent features, the mean time resolution in the camera is 1.0 ns after the relative correction and 0.4 ns after the absolute correction.

ACKNOWLEDGMENTS
We gratefully acknowledge support from the agencies and organizations listed under Funding Agencies at this website: http://www.cta-observatory.org/. We also acknowledge the great help from Open-It Consortium on the hardware development of the DRS4 readout board. SN is supported by JSPS KAKENHI Grant Number JP19J11940, and PG and JS are supported by the Narodowe Centrum Nauki grant No.2019/34/E/ST9/00224.

REFERENCES
[1] The Cherenkov Telescope Array Consortium. http://www.cta-observatory.org/.
[2] Konno, Y. et al., “Development of the quality control system of the readout electronics for the large size telescope of the Cherenkov Telescope Array observatory,” Nuclear Instruments and Methods in Physics Research A 824, 349–352 (July 2016).
[3] Sakurai, S., Depaoli, D., Lopez-Coto, R., et al., “The calibration of the first Large-Sized Telescope of the Cherenkov Telescope Array,” in [36th International Cosmic Ray Conference (ICRC2019)], International Cosmic Ray Conference 36, 780 (July 2019).

[4] Cortina, J. for the CTA LST project, “Status of the Large Size Telescopes of the Cherenkov Telescope Array,” in [36th International Cosmic Ray Conference (ICRC2019)], International Cosmic Ray Conference 36, 653 (July 2019).

[5] Toyama, T. et al., “Novel Photo Multiplier Tubes for the Cherenkov Telescope Array Project,” in [International Cosmic Ray Conference], International Cosmic Ray Conference 33, 1178 (Jan. 2013).

[6] Toyama, T. et al., “Evaluation of the basic propertied of the novel 1.5 in. size PMTs from Hamamatsu Photonics and Electron Tubes Enterprises,” Nuclear Instruments and Methods in Physics Research A 787, 280–283 (July 2015).

[7] Mirzoyan, R. et al., “Evaluation of Photo Multiplier Tube candidates for the Cherenkov Telescope Array,” Nuclear Instruments and Methods in Physics Research A 824, 640–641 (July 2016).

[8] Mirzoyan, R. et al., “Evaluation of novel PMTs of worldwide best parameters for the CTA project,” Nuclear Instruments and Methods in Physics Research A 845, 603–606 (Feb. 2017).

[9] Hadasch, D. et al., “Development of Slow Control Boards for the Large Size Telescopes of the Cherenkov Telescope Array,” in [34th International Cosmic Ray Conference (ICRC2015)], International Cosmic Ray Conference 34, 1024 (July 2015).

[10] Sanuy, A. et al., “Wideband (500 MHz) 16 bit dynamic range current mode PreAmplifier for the CTA cameras (PACTA),” Journal of Instrumentation 7, C01100 (Jan. 2012).

[11] Kubo, H. et al., “Development of the Photomultiplier-Tube Readout System for the CTA Large Size Telescope,” in [International Cosmic Ray Conference], International Cosmic Ray Conference 33, 2823 (Jan. 2013).

[12] Masuda, S. et al., “Development of the photomultiplier tube readout system for the first Large-Sized Telescope of the Cherenkov Telescope Array,” in [34th International Cosmic Ray Conference (ICRC2015)], International Cosmic Ray Conference 34, 1003 (July 2015).

[13] Gascon, D. et al., “Reconfigurable ASIC for a low level trigger system in Cherenkov Telescope Cameras,” Journal of Instrumentation 11, P11017 (Nov. 2016).

[14] Tejedor, L. A. et al., “An Analog Level 1 Trigger Prototype for CTA,” IEEE Transactions on Nuclear Science 60, 251–258 (Feb. 2013).

[15] López Moya, M. et al., “A Trigger Interface Board to manage trigger and timing signals in CTA Large-Sized Telescope and Medium-Sized Telescope camera,” in [35th International Cosmic Ray Conference (ICRC2017)], International Cosmic Ray Conference 301, 808 (Jan. 2017).

[16] Uchida, T., “Hardware-Based TCP Processor for Gigabit Ethernet,” IEEE Transactions on Nuclear Science 55, 1631–1637 (June 2008).

[17] Hoffmann, D. et al., “40 Gbps data acquisition system for NectarCAM,” in [Journal of Physics Conference Series], Journal of Physics Conference Series 898, 032015 (Oct. 2017).

[18] Lyard, E. et al., “End-to-end data acquisition pipeline for the Cherenkov Telescope Array,” in [35th International Cosmic Ray Conference (ICRC2017)], International Cosmic Ray Conference 301, 843 (Jan. 2017).

[19] Pence, W., Seaman, R., and White, R. L., “A Tiled-Table Convention for Compressing FITS Binary Tables,” arXiv e-prints, arXiv:1201.1340 (Jan. 2012).

[20] https://github.com/cta-observatory/ctapipe.

[21] https://github.com/cta-observatory/cta-lstchain.

[22] Palatiello, M. et al., “Test results of a prototype device to calibrate the Large Size Telescope camera proposed for the Cherenkov Telescope Array,” in [35th International Cosmic Ray Conference (ICRC2017)], International Cosmic Ray Conference 301, 857 (Jan. 2017).

[23] Ritt, S., Dinapoli, R., and Hartmann, U., “Application of the DRS chip for fast waveform digitizing,” Nuclear Instruments and Methods in Physics Research A 623, 486–488 (Nov. 2010).

[24] Aleksić, J. et al., “The major upgrade of the MAGIC telescopes, Part I: The hardware improvements and the commissioning of the system,” Astroparticle Physics 72, 61–75 (Jan. 2016).
[25] Sitarek, J. et al., “Analysis techniques and performance of the Domino Ring Sampler version 4 based readout for the MAGIC telescopes,” *Nuclear Instruments and Methods in Physics Research A* **723**, 109–120 (Sept. 2013).

[26] Stricker-Shaver, D., Ritt, S., and Pichler, B. J., “Novel Calibration Method for Switched Capacitor Arrays Enables Time Measurements With Sub-Picosecond Resolution,” *IEEE Transactions on Nuclear Science* **61**, 3607–3617 (Dec. 2014).

[27] Gaug, M. et al., “Calibration of the MAGIC Telescope,” in *29th International Cosmic Ray Conference (ICRC29), Volume 5*, *International Cosmic Ray Conference* **5**, 375 (Jan. 2005).