Formal Definitions of Memory Consistency Models

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Abstract

Shared Memory is a mechanism that allows several processes to communicate with each other by accessing –writing or reading– a set of variables that they have in common.

A Consistency Model defines how each process observes the state of the Memory, according to the accesses performed by it and by the rest of the processes in the system. Therefore, it determines what value a read returns when a given process issues it. This implies that there must be an agreement among all, or among processes in different subsets, on the order in which all or a subset of the accesses happened.

It is clear that a higher quantity of accesses or processes taking part in the agreement makes it possibly harder or slower to be achieved. This is the main reason for which a number of Consistency Models for Shared Memory have been introduced.

This paper is a handy summary of [2] and [3] where consistency models (Sequential, Causal, PRAM, Cache, Processors, Slow), including synchronized ones (Weak, Release, Entry), were formally defined. This provides a better understanding of those models and a way to reason and compare them through a concise notation.

There are many papers on this subject in the literature such as [11] with which this work shares some concepts.

1 Fundamentals

A memory is a system that accepts two operations: write and read. These operations can be issued by any process from the set \( P \); and
are related to one of the variables in the set $\mathcal{V}$. As usual, write sets a new value for a variable, whereas read returns the value associated with a variable. For sake of simplicity and without loss of generality, we assume that $\mathcal{P} \subset \mathbb{N}$, all variables are of type $\mathbb{N}$, and that writes are uni-valued (a given value may be written only once).

We designate write and read operations with the following notation.

**Definition 1 Write and Read**

- $w(i, v, a)$ to denote that process $i \in \mathcal{P}$ writes the value $a \in \mathbb{N}$ to the variable $v \in \mathcal{V}$.

- $r(i, v, a)$ to denote that process $i \in \mathcal{P}$ reads $a \in \mathbb{N}$ from the variable $v \in \mathcal{V}$.

\[\square\]

**Definition 2 Sequence-Execution**

A sequence-execution of a memory system is a sequence of write and read operations. For a given execution $\alpha$, its associated total order $<^{\alpha}$ is trivially defined as

\[o_1 <^{\alpha} o_2 \equiv \alpha = \alpha' \alpha'' o_2 \alpha''\]

\[\square\]

We can apply a condition $c$ to filter a sequence-execution $\alpha$ as well as an order $<^{\alpha}$.

**Definition 3 Filtering**

- $\alpha|c =$

\[
\left\{ \begin{array}{l}
\epsilon \iff \alpha = \epsilon \\
o (\alpha_1|c) \iff c(o) \iff \alpha = o \alpha_1 \\
\alpha_1|c \iff \neg c(o)
\end{array} \right.
\]

- $o_1(<^{\alpha}|c)o_2 \equiv o_1 <^{\alpha} o_2 \land c(o_1) \land c(o_2)$

\[\square\]
Common filters include

• \((\square | i : P)\), \(\square\) (sequence or order) restricted to actions process \(i\).
• \((\square | v : V)\), \(\square\) restricted to actions on variable \(v\).
• \((\square | w)\), \(\square\) restricted to write actions.
• \((\square | r)\), \(\square\) restricted to read actions.
• \((\square | w(i, \cdot, \cdot))\), \(\square\) restricted to write actions by process \(i\).
• \((\square | w(\cdot, v, \cdot))\), \(\square\) restricted to write actions on variable \(v\).
• \((\square | (a, b)) \equiv (\square | a) \cup (\square | b)\)

We only consider \textit{valid} executions. An execution is valid when every read gets its value from a \textit{previous} write.

\textbf{Definition 4 Valid Execution}

\(\alpha\) is a valid execution \(\equiv\)

• \(r(\cdot, v, a) \in \alpha \Rightarrow \alpha = \alpha_1 w(\cdot, v, a) \alpha_2 r(\cdot, v, a) \alpha_3\)

• \(w(i, v, a) \in \alpha \equiv \alpha | w(\cdot, v, a) = w(i, v, a)\) \textit{(writes are uni-valued)}

Valid executions are not meant to capture “real time” accurately (time is relative in a distributed system). We are only forbidding that a read gets a value random value or either a value from the future.

A valid execution \(\alpha\) defines two relationships: writes-to and process order.

\textbf{Definition 5 Writes-to and Process Order}

For a valid execution \(\alpha\):

• writes-to relates a read and the write which set the value:
  \[
  o_1 \mapsto_\alpha o_2 \equiv o_1 = w(\cdot, v, a) \in \alpha \land o_2 = r(\cdot, v, a) \in \alpha
  \]
process order relates all the actions by the same process:

\[ o_1(i, \cdot, \cdot) <^\alpha_{PO} o_2(j, \cdot, \cdot) \equiv i = j \land o_1 <^\alpha o_2 \]

Alternate definition:

\[ a <^\alpha_{PO} b \equiv (\exists i \in P \mid (\alpha|i) = \alpha_1 a \alpha_2 b \alpha_3) \]

The transitive closure of the writes-to and the program order relations defines a partial order over the actions of a valid execution \( \alpha \) called the causal relation.

**Definition 6** Causal Relation

\[ <^\alpha_{CR} \equiv (\rightarrow_\alpha \cup <^\alpha_{PO})^* \]

A valid execution is consistent if it contains no read fetching an overwritten value.

**Definition 7** Consistent Execution

\( \alpha \) is consistent \( \equiv \)

\[ r(i, v, a) \in \alpha \Rightarrow \left\{ \begin{array}{l} \alpha = \alpha_1 w(j, v, a) \alpha_2 r(i, v, a) \alpha_3 \land w(j, v, a) \rightarrow r(i, v, a) \\ \alpha_2|w(\cdot, v, \cdot) = \epsilon \end{array} \right. \]

A key concept used for defining models is linearization which captures the idea of extending a partial order to a total one while respecting consistency.

**Definition 8** Linearizability

A relation \( <^\gamma \) is consistently linearizable (it has a consistent linear extension, linearizable for short) \( \equiv \)

\[ (\exists \beta : \text{sequence of the actions in } \alpha \mid: \beta \text{ is consistent} \land <^\gamma \subseteq <^\beta) \]
Because $\beta$, the sequence proving the linearizability of a given $<_{\gamma}$, is consistent, we have $\rightarrow_{\alpha} \subseteq <_{\beta}$. And because $<_{\beta}$ is a total order including $<_{\gamma}$ the closure of $<_{\gamma}$ and $\rightarrow_{\alpha}$ satisfies

$$(<_{\gamma} \cup \rightarrow_{\alpha})^* \subseteq <_{\beta}$$

and it is, obviously, acyclic; as well as $<_{\gamma}$ and $\rightarrow_{\alpha}$ are.

In order to show that a sequence, $\beta$, proves that $<_{\gamma}$ is linearizable, is enough for $\beta$ to include all actions in $<_{\gamma}$ plus the writes not yet included and necessary for any read in $<_{\gamma}$. The rest of actions of $\alpha$ can be trivially added to the end of $\beta$, only having to obey $\rightarrow_{\alpha}$ since they are not in $<_{\gamma}$.

It’s much easier to understand and to reason on executions when depicted in a diagram-execution, where process actions are visually separated and the causal relation is explicit. Notation can also be simplified. As an introduction of concepts, consider the diagram-execution in figure 1.

![Figure 1: A diagram-execution.](image)

Time increases from left to right in the diagram. Horizontal arrows express process order. Diagonal arrows denote writes-to order. By definition of process order and by the condition that reads always get values previously written, valid diagrams may not have arrows pointing left. Aside from this, diagrams don’t reflect (unless stated) when events happened in real time. Hence, the fact that $w(2, y, 2)$ is to the right of $w(1, x, 1)$ doesn’t imply that $w(2, y, 2)$ happened necessarily later.

Clearly, a diagram-execution defines a set of sequence-executions: those ones respecting process order and writes-to as expressed by the diagram-execution.
2 Consistency Models

2.1 Sequential Consistency

The first memory model we introduce is sequential consistency [9]. Compared with the rest of models we shall discuss, this one corresponds to the common understanding on how a memory behaves in absence of a global clock.

A sequentially consistent memory provides a total ordering of writes (all processes agree on the order in which memory accesses happened) and ensures that every read gets always the last value written to its variable.

Definition 9 Sequential Consistency

\( \alpha \) is an execution by a Sequential memory \( \equiv \)

\[ \langle \alpha \rangle_{PO} \text{ is consistently linearizable.} \]

\( \square \)

Note the implications of this definition. If \( \beta \) is the required consistent linear extension of \( \alpha \), then \( \langle \alpha \rangle_{CR} \subseteq \langle \beta \rangle \) (and \( \langle \alpha \rangle_{PO} = \langle \beta \rangle_{PO} \), \( \mapsto \mapsto \alpha \mapsto \mapsto \beta \)).

Figure 2: Sequential execution.

As a first example, note that the execution in figure 2 is sequential. This consistent linear extension \( w(2, x, 2) \ w(1, x, 1) \ r(1, x, 1) \ r(2, x, 1) \) is the proof.

However, the execution in figure 3 is not sequential.

Works like [10] suggest that, in a distributed system, a sequential memory can’t be simulated with waiting-free write and read operations: the process issuing an operation must wait for the response from at least one different process in order to ensure the common view of memory accesses. This fact led to the proposal of memory models with fewer consistency requirements.
2.2 Causal Consistency

The causal consistency memory model [1] allows two processes to disagree on the order of writes only in case they are causally unrelated.

Causal dependencies are very easy to identify on diagram-executions because two operations are causally related if there is a path from one of them to the other.

**Definition 10 Causal Consistency**

α is an execution by a Causal memory ≡

\[(\forall i \in \mathcal{P} \mid \llbracket C_{\alpha} \rrbracket(i, w) \text{ is consistently linearizable})\]

\[\square\]

\[\begin{array}{c}
  w(x)1 \rightarrow r(x)2 \\
  w(x)2 \rightarrow r(x)1
\end{array}\]

Figure 4: Causal execution.

The execution α in figure 4 is causally consistent because

\[
\llbracket C_{\alpha} \rrbracket(1, w) = \begin{array}{c}
  w(x)1 \rightarrow r(x)2 \\
  w(x)2
\end{array}
\]
and $\alpha_{CR}|(2, w) = \begin{array}{c}
w(x)1 \\
\downarrow \\
w(x)2 \\
\downarrow \\
r(x)1 \\
\end{array}$

Figure 5: PRAM execution.

The execution in figure 5 is PRAM consistent because $\alpha_{PO}|(1, w) = \begin{array}{c}
w(x)1 \\
\end{array}$

2.3 PRAM Consistency

The Pipelined RAM memory model [10] further relaxes requirements. It allows two processes to disagree on the order of writes if they are issued by different processes.

**Definition 11** PRAM Consistency

$\alpha$ is an execution by a PRAM memory $\equiv$

$(\forall i \in \mathcal{P} \mid \alpha_{PO}|(i, w) \text{ is consistently linearizable})$

\[\square\]
have consistent linear extensions. However, it is not causally consistent because

has no consistent linear extension.

### 2.4 Cache Consistency

This model, [7], focus on the consistency of each variables separately. All processes must agree on the order of accesses to the same variable, but they are allowed to disagree on accesses to different variables.

#### Definition 12 Cache Consistency

α is an execution by a Cache memory \(\prod\) \(\equiv\)

\[(\forall v \in V : <_PO | v \text{ is consistently linearizable})\]

□

The execution α in figure 6 is Cache consistent because
Figure 6: Cache execution.

\[
\alpha^P_{\mathcal{O}} | x = \begin{array}{c}
w(x)1 \\
\downarrow \\
r(x)1
\end{array} \quad \begin{array}{c}
w(x)2 \\
\downarrow \\
r(x)1
\end{array} \quad \begin{array}{c}
w(y)3 \\
\downarrow \\
r(y)3
\end{array}
\]

and \[
\alpha^P_{\mathcal{O}} | y = \begin{array}{c}
w(y)3 \\
\downarrow \\
r(y)3
\end{array}
\]

have consistent linear extensions. However, it is not PRAM nor causally consistent because

\[
\alpha^P_{\mathcal{O}} | (2, w) = \alpha^C_{\mathcal{R}} | (2, w) = \begin{array}{c}
w(x)1 \\
\downarrow \\
r(x)1
\end{array} \quad \begin{array}{c}
w(x)2 \\
\downarrow \\
r(x)1
\end{array} \quad \begin{array}{c}
w(y)3 \\
\downarrow \\
r(y)3
\end{array}
\]

does not have a consistent linear extension.

### 2.5 Processor Consistency

This model, also defined in [7], could be viewed as the intersection of the PRAM and Cache consistency models. But, actually, it is a little stronger than just this.

**Definition 13** Processor Consistency

\( \alpha \) is an execution by a PROC memory \( \equiv \)
\( \forall i, j \in P \mid <_{PO}^{\alpha} | (i, w) \text{ and } <_{PO}^{\alpha} | (j, w) \) have, respectively, consistent linear extensions \( \beta_i \) and \( \beta_j \)
\[ \land (\forall x \in V \mid \beta_i|w(\cdot, x, \cdot) = \beta_j|w(\cdot, x, \cdot)) \]
have the following consistent linear extensions:

\( \beta_1 = w(3, x, 3) \ w(1, x, 1) \ w(2, y, 2) \)
\( \beta_2 = w(3, x, 3) \ w(1, x, 1) \ r(2, x, 1) \ w(2, y, 2) \)
\( \beta_3 = w(2, y, 2) \ r(3, y, 2) \ w(3, x, 3) \ w(1, x, 1) \ r(3, x, 1) \)

which, additionally, satisfy
\( \beta_1 | w(\cdot, x, \cdot) = \beta_2 | w(\cdot, x, \cdot) = \beta_3 | w(\cdot, x, \cdot) \)
\( \beta_1 | w(\cdot, y, \cdot) = \beta_2 | w(\cdot, y, \cdot) = \beta_3 | w(\cdot, y, \cdot) \)

However, it is clear that \( \alpha \) is not causally consistent.

It’s worth to mention that there are executions that, being PRAM and Cache consistent executions, are not Processor consistent. For example, consider the execution \( \alpha \) in figure 8.
and $\prec_{PO}^\alpha y = \begin{array}{c}
\end{array}$

are consistently linearizable. $\alpha$ is also PRAM because

$\prec_{PO}^\alpha |(1, w) = \begin{array}{c}
\end{array}$

have consistent linear extensions. But it is not Processor consistent because the order of writes on $x$ in the unique linear extension of $\prec_{PO}^\alpha |(2, w)$ is different from the order in the linear extensions of $\prec_{PO}^\alpha |(3, w)$.

Finally, there is also the case of executions being Causal consistent and Cache consistent but not Processor consistent. Consider the execution $\alpha$ in figure 9.

$\alpha$ is Cache consistent because
Figure 9: Causal and Cache execution.

\[<^\alpha_{PO} | x = \]

\[<^\alpha_{CR} | (1, w) = \]

\[<^\alpha_{CR} | (2, w) = \]

and \[<^\alpha_{PO} | y = \]

have consistent linear extensions.

In addition, \(\alpha\) is Causal because
\begin{align*}
<_{CR}^\alpha | (3, w) = \begin{array}{c}
\rightarrow w(x)1 \rightarrow w(y)2 \\
\rightarrow w(x)3 \rightarrow r(x)1
\end{array}
\end{align*}

have consistent linear extensions. However, all the consistent linear
extensions of $<_{PO}^\alpha | (1, w) = <_{CR}^\alpha | (1, w)$ and $<_{PO}^\alpha | (3, w) = <_{CR}^\alpha | (3, w)$
have different orders for $w(2, x, 1)$ and $w(3, x, 3)$.

2.6 Slow Consistency

This model, \cite{8}, is a weaker version of both PRAM and Cache Consistency.

\textbf{Definition 14} Slow Consistency
\begin{quote}
$\alpha$ is an execution by a Slow memory $\equiv$
\end{quote}
\begin{quote}
$(\forall v \in V, i \in P | (<_{PO}^\alpha | (i, w(\cdot, v, \cdot)))$ is consistently linearizable)$
\end{quote}
\[\square\]

\begin{center}
\begin{tikzpicture}
\node (x1) at (0,0) {$w(x)1$};
\node (x2) at (1,0) {$w(x)2$};
\node (y1) at (2,0) {$w(y)3$};
\node (y2) at (2,-1) {$w(y)4$};
\node (r1) at (3,0) {$r(y)4$};
\node (r2) at (3,-1) {$r(y)3$};
\node (r3) at (3,-2) {$r(x)1$};
\draw[->] (x1) -- (x2);
\draw[->] (x1) -- (y1);
\draw[->] (x2) -- (y1);
\draw[->] (x2) -- (y2);
\draw[->] (y1) -- (r1);
\draw[->] (y2) -- (r2);
\draw[->] (r1) -- (r2);
\draw[->] (r2) -- (r3);
\end{tikzpicture}
\end{center}

Figure 10: Slow execution.

It is easy to see that figure 4 shows a Slow (and Causal and PRAM) execution that is not Cache. On the other hand, the execution in figure 6 is Slow (and Cache) but not PRAM. Combining them, see figure [10] we can build a Slow execution not being Cache nor PRAM. It is Slow because
\begin{itemize}
\item $<_{PO}^\alpha | (1, w(\cdot, x, \cdot))) = \begin{array}{c}
\rightarrow w(x)1 \rightarrow w(x)2 \rightarrow w(y)3 \rightarrow r(y)4
\end{array}$
\end{itemize}
has this consistent extension: $w(1, x, 1) w(1, x, 2) w(1, y, 3) w(2, y, 4) r(1, y, 4)$
2.7 Relations among Consistency Models

Some indications on how consistency models are related appeared in past sections. Here, we are summarizing them. First, table 1 compiles the definitions of the consistency models.

From these definitions, it immediately follows that

1. Execution $\alpha$ is sequential $\Rightarrow$ $\alpha$ is a Causal, PRAM, Cache and Processor execution as well. This is, a Sequential memory is also a Causal, PRAM, Cache and Processor memory.

2. Execution $\alpha$ is Causal $\Rightarrow$ $\alpha$ is a PRAM execution.

3. Execution $\alpha$ is Processor $\Rightarrow$ $\alpha$ is a PRAM and Cache execution.

4. Execution $\alpha$ is PRAM $\Rightarrow$ $\alpha$ is a Slow execution.
\[ \alpha \in \text{Model} \equiv \text{Sequential} \begin{equation} \forall i \in \mathcal{P} : (\leq_{\text{PO}}^i | (i, w) \text{ is consistently linearizable}) \end{equation} \]

Causal \[ \begin{equation} \forall i \in \mathcal{P} : (\leq_{\text{PO}}^i | (i, w) \text{ is consistently linearizable}) \end{equation} \]

PRAM \[ \begin{equation} \forall i \in \mathcal{P} : (\leq_{\text{PO}}^i | (i, w) \text{ is consistently linearizable}) \end{equation} \]

Cache \[ \begin{equation} \forall v \in \mathcal{V} : (\leq_{\text{PO}}^v \text{ is consistently linearizable}) \end{equation} \]

Processor \[ \begin{equation} \forall i,j \in \mathcal{P} : \leq_{\text{PO}}^i | (i, w) \text{, } \leq_{\text{PO}}^j | (j, w) \text{ have, respectively, consistent linear extensions } \beta_i, \beta_j \text{ and } (\forall x \in \mathcal{V} : \beta_i | w(\cdot, x, \cdot) = \beta_j | w(\cdot, x, \cdot))) \end{equation} \]

Slow \[ \begin{equation} \forall v \in \mathcal{V}, i \in \mathcal{P} : (\leq_{\text{PO}}^i | (i, w(\cdot, v, \cdot))) \text{ is consistently linearizable} \end{equation} \]

Table 1: Definition of Consistency Models

- Execution \( \alpha \) is Cache \( \Rightarrow \) \( \alpha \) is a Slow execution\(^1\)

Now, we gather a set of executions in order to proof some non-existent relationships among models.

1. Causal, PRAM, non-Sequential, non-Cache, non-Processor.

\[ \begin{array}{c}
    w(x_1) \rightarrow r(x_2) \\
    \downarrow \downarrow \\
    w(x_2) \rightarrow r(x_1)
\end{array} \]

2. PRAM, non-Sequential, non-Causal, non-Cache, non-Processor.

\(^1\)For this case, recall that

- \( \leq_{\text{PO}}^i | (i, w(\cdot, v, \cdot)) = (\leq_{\text{PO}}^i | i) \cup (\leq_{\text{PO}}^i | w(\cdot, v, \cdot)) \)

- The reason for an execution \( \alpha \) being Cache but not Slow, is not that \( \leq_{\text{PO}}^i | w(\cdot, v, \cdot) \) can’t be linearized, or otherwise \( \leq_{\text{PO}}^i | v \) would also fail to be, thus not being Cache either.

- But it is neither the case that there is a Cache execution which can’t be extended without respecting \( \leq_{\text{PO}}^i | i \). This would imply that \( o_1(x) \leq_{\text{PO}}^i a_2(y) \) (with \( x \neq y \)) and that \( o_2(\leq_{\text{PO}}^i | x \cup \to_{\alpha} o_2) \). This latter is not possible, since neither \( \leq_{\text{PO}} \) nor \( \to_{\alpha} \) can reach, by definition, actions before \( o_2 \).
3. Cache, non-Sequential, non-Causal, non-PRAM, non-Processor.

4. Processor, non-Sequential, non-Causal, PRAM, Cache.

5. PRAM, Cache, non-Sequential, non-Causal, non-Processor

6. Causal, Cache, PRAM, non-Sequential, non-Processor.
7. Slow, non-PRAM, non-Cache, non-Causal, non-Sequential, non-Processor.

\[ w(x)_1 \rightarrow w(x)_2 \rightarrow w(x)_3 \rightarrow r(y)_4 \]

Table 2 summarizes how memory models are related. When a given memory model does not implies another different one, the number refers to the execution in the previous list that proves it.

| Model x \( \Rightarrow \) Model y | Seq. | Causal | PRAM | Cache | Proc. | Slow |
|---------------------------------|------|--------|------|-------|-------|------|
| Sequential                      | •    | •      | •    | •     | •     | •    |
| Causal                          | (1)  | •      | •    | •     | (1)   | (1)  |
| PRAM                            | (2)  | (2)    | •    | (1)   | (1)   | •    |
| Cache                           | (3)  | (3)    | (3)  | •     | (3)   | •    |
| Processor                       | (4)  | (4)    | •    | •     | •     | •    |
| Slow                            | (7)  | (7)    | (7)  | (7)   | (7)   | •    |
| PRAM \( \land \) Cache         | (5)  | (5)    | •    | •     | •     | (5)  |
| Causal \( \land \) Cache       | (6)  | •      | •    | •     | (6)   | •    |
| Causal \( \land \) PRAM \( \land \) Cache \( \land \) Proc. | (†) | • | • | • | • | • |

Table 2: Model Relationships
We have found an execution that is Causal, PRAM, Cache and Processor consistent at the same time, but it is not a Sequential execution. This fact is explained in section A.

### 3 Relaxing Process Order

So far, all models have been defined upon the same notion of Process Order. Now, we point out that Process Order can also be relaxed without breaking its essence: Lazy Process Order.

Lazy Process Order is a subset of Process Order, where original relationships are preserved for a read and subsequent writes, and among operations on the same variable.

**Definition 15** Lazy Process Order

\[ o_1 <_{LPO} o_2 \equiv \]

\[ o_1 <_{PO} o_2 \land \left\{ \begin{array}{l} o_1 = r(\cdot, \cdot, \cdot) \\ \lor \\ o_1 = \cdot(x, \cdot) \land o_2 = \cdot(\cdot, x, \cdot) \end{array} \right. \]

In order to justify Lazy Program Order, consider this execution:

\[ w(x)1 \rightarrow w(x)2 \]

\[ \downarrow \downarrow \downarrow \]

\[ w(y) \rightarrow r(x)? \]

where a memory system ensures that the global order of writes is \( w(1, x, 1)w(1, x, 2)w(2, y, \cdot) \). At a given moment, the value 1 is available at process 2, but value 2 is not yet ready. If Process Order must be respected, the read have to wait until value 2 is available. But \( w(2, y, \cdot) \) and \( r(2, x, ?) \) are not related under Lazy Process Order. Hence, it is allowed for the read to get value 1.

A case of this situation is also the Cache execution shown in figure 3 in page 10.
4  Synchronized Consistency Models

In addition to write and read accesses, a memory system can support synchronization primitives in order to simplify the coordination among the processes communicating through it. These primitives can be used to set up dependencies among the rest of memory accesses, and to mark points where the state of the memory is made common to all the processes.

In order to define these type of models we have to introduce a set of synchronization variables $S$, and the following operations.

**Definition 16  Acquire and Release**

- $rel(i, s)$ to denote that process $i \in \mathcal{P}$ releases the variable $s \in S$.
- $acq(i, s)$ to denote that process $i \in \mathcal{P}$ acquires the variable $s \in S$.

Now, the definition of *valid execution* is extended to include the fact that these primitives guarantee mutual exclusion.

**Definition 17  Valid Execution**

$\alpha$ is a valid execution $\equiv$

$\alpha|_{(w,r)}$ is valid according to definition 4 \land for $\beta = \alpha|(acq, rel)$ and any synchronization variable $s$

\[\begin{cases} 
\beta|s = \epsilon \\
\beta|s = acq(i, s)rel(i, s)\beta' \land \beta' \text{ is a valid execution}
\end{cases}\]

Now, the definition of *valid execution* is extended to include the fact that these primitives guarantee mutual exclusion.

As of the previous definition, we define the *mutual exclusion* order for a valid execution.

**Definition 18  Mutual Exclusion Order**

$a <_{ME} b \equiv$

$(\exists s \in S : \alpha|s = \alpha_1a_2b\alpha_3 \land \alpha \text{ is valid.})$
The relationship between a release operation and the corresponding subsequent acquire gaining the mutual exclusion right over the synchronization variable can be defined like a read-write analogy for synchronizations.

**Definition 19**  **Writes-to for Synchronizations**

\[ \text{rel}(i, s) \rightarrow_{\alpha} \text{acq}(j, s) \equiv \]

\[ \alpha|\text{acq}(\cdot, s), \text{rel}(\cdot, s)) = \alpha_1 \text{rel}(i, s) \text{acq}(j, s) \alpha_2 \]

**Definition 20**  **D−, D+, D and <SO**

Every synchronization action \( o \) has two associated sets \( D_{-}(o) \) and \( D_{+}(o) \) that group, respectively, the ordinary accesses intended to precede and follow \( o \).

The Synchronization Order (SO) formalizes this idea on how synchronizations induce the ordering of the rest of actions.

\( D(s) \) is the set of ordinary accesses dependent on synchronization variable \( s \).

\[ a <_{\text{SO}}^{\alpha} b \equiv \]

\[ \begin{cases} 
  a <_{\text{ME}}^{\alpha} b \\
  \lor \\
  a \in D_{-}(b) \\
  \lor \\
  b \in D_{+}(a) \\
  \lor \\
  (\exists c \in \alpha \mid a <_{\text{ME}}^{\alpha} c <_{\text{ME}}^{\alpha} b) 
\end{cases} \]

The minimum consistency that synchronized models support is Slow consistency. This is, between two consecutive synchronizations, the order among writes on the same variable by the same process will be respected.
Definition 21  Synchronized Consistency Model
\( \alpha \) is an execution by a Synchronized memory \( \equiv \)

\[ (\forall v \in V, i \in P : \langle i, v \rangle_s \cup (\langle i, v \rangle_o \mid (i, w(\cdot, \cdot))) \text{ is consistently linearizable} ) \]

Different Synchronized Models are defined and distinguished by means of \( D^- \) and \( D^+ \).

The following table gathers the definitions of the main Synchronized Models: Weak [5], Release [6], and Entry [4].

| Model   | Definition                                                                 |
|---------|----------------------------------------------------------------------------|
| Weak    | \( D^-(o) = \{ e : e <^\alpha_{PO} o \} \)                                |
|         | \( D^+(o) = \{ e : o <^\alpha_{PO} e \} \)                                |
| Release | \( D^-(\text{rel}(\cdot, \cdot)) = \{ e : e <^\alpha_{PO} \text{rel}(\cdot, \cdot) \} \) |
|         | \( D^+(\text{acq}(\cdot, \cdot)) = \{ e : \text{acq}(\cdot, \cdot) <^\alpha_{PO} e \} \) |
| Lazy    | \( D^-(\text{acq}(\cdot, \cdot)) = \{ e : (\exists \text{rel} \mid \text{rel} \rightarrow^\alpha \text{acq}(\cdot, \cdot)) : e <^\alpha_{PO} \text{rel} \} \) |
| Release | \( D^+(\text{acq}(\cdot, \cdot)) = \{ e : \text{acq}(\cdot, \cdot) <^\alpha_{PO} e \} \) |
| Entry   | \( D^-(\text{acq}(\cdot, s)) = \{ e : (\exists \text{rel} \mid \text{rel}(\cdot, s) \rightarrow^\alpha \text{acq}(\cdot, s)) : e <^\alpha_{PO} \text{rel} \} \) |
|         | \( \land e \in D(s) \} \)                                              |
|         | \( D^+(\text{acq}(\cdot, s)) = \{ e : \text{acq}(\cdot, s) <^\alpha_{PO} e \land e \in D(s) \} \) |
A When an Execution has a Consistent Linear Extension

As we know, a consistent linear extension of a given relation $\sim_\alpha$ may not, by definition, have read operations fetching an overwritten value. Therefore, whenever an execution contains a related write-read pair, $w \mapsto r$, and a different write $w'$, all on the same variable; it is necessary that $w'$ is either before or after $w \mapsto r$ in any linear extension. In addition, linear extensions do respect some other relation $\sim$ as well; usually Process Order or Causal relations, maybe restricted.

The point is: how $w \mapsto r$ is related to $w'$ in $\sim$? If $w' \sim w$, there is no need to introduce any new dependency; as well as it is the case for $r \sim w'$, because either $w' \sim w \mapsto r$ or $w \mapsto r \sim w'$ already defines their relative order in a linear extension.

But for the cases $w \sim w'$ and $w' \sim r$ we can infer new dependencies to be held in every consistent linear extension.

**Definition 22** co extension of $\sim_\alpha$

- **WW dependency**
  \[ w' \rightarrow_{co}^\sim w \equiv w \mapsto_\alpha r \land w' \sim_\alpha r \]

- **RW dependency**
  \[ r \rightarrow_{co}^\sim w' \equiv w \mapsto_\alpha r \land w \sim_\alpha w' \]

- **co extension of $\sim_\alpha$**
  \[ co(\sim_\alpha) = (\sim_\alpha \cup \rightarrow_{co}^\sim)^* \]

Figure 11: Causal execution with CO dependencies.

Let’s show some examples of executions augmented with $<_{CO}$ dependencies. In figure 11 we can see a causal execution with WW
dependencies added: \( w(1, x, 1) \xrightarrow{r(2, x, 1)} w(2, x, 1) \land w(2, x, 2) \xrightarrow{r(2, x, 2)} w(1, x, 1) \xrightarrow{r(1, x, 2)} r(1, x, 1) \). This execution is not sequentially consistent. CO dependencies have created a cycle in the graph that just shows us there is no consistent linear extension for it.

Figure 12: Cache execution with CO dependencies.

Just one more example. Figure 12 shows a Cache execution with just a RW dependency added: \( w(1, x, 1) \xrightarrow{r(2, x, 1)} w(1, x, 1) \xrightarrow{r(1, x, 2)} r(1, x, 1) \). Again, this execution is not sequentially consistent and the RW arrow makes the graph cyclic.

By applying co\((\sim_\alpha)\) once, we obtain a new \(\sim'\) binary relation which can be used again to discover new CO dependencies. Hence, let’s generalize the co operator.

**Definition 23** \( CO(\sim_\alpha) \)

\[
CO(\sim_\alpha) = \lim_{n \to \infty} co(\cdots co(\sim_\alpha))
\]

□

When a new CO dependency is added, new ones could be found when co is applied again. But because executions are finite, the limit exists.

It easily follows from its definition that the acyclicity of \( CO(\sim_\alpha) \) is a necessary condition for \(\sim_\alpha\) to have a consistent linear extension. The reverse statement is not true. There are non-consistently linearizable executions with a cycle-free CO extension.

This can happen in executions with *unrelated* \( w r w' \) triplets: operations on the same variable with \( w \xrightarrow{r} r \) and \( w' \) not related either to \( w \) or \( r \). For some executions, it could occur that any choice, \( w' \xrightarrow{w} w \) or \( r \xrightarrow{w'} \), to obtain a linear extension leads to an overwritten value for a different variable. Consider the diagram-execution in figure...
with horizontal lines for process order, and arrows for write-to relationship as usual. Each one of the rest of arrows indicate a causal dependency, induced by a chain of write-to (on different variables) and process order actions. The particular actions of the chain are not shown to keep the diagram as simple as possible.

The actions shown in figure [13] are unrelated triplets on different variables, easily recognizable by shape and color. For each one of them, there is no path between $w'$ and the pair $w$ and $r (w \rightarrow r)$.

Figure 13: Non-Sequential execution with acyclic CO.

Let’s consider the triplet on variable $x$. Because there is no imposed WW nor RW dependency, in order to have a consistent linear extension:

- If we add a WW dependency $w(x)' \leadsto w(x)$ (WW1), it appears the path $w'(a)$ $w'(x)$ $w(x)$ $r(a)$ which forces a WW dependency $w'(a) \leadsto w(a)$ (WW2). But now, the following path exists: $w(b)$ $w'(a)'$ $w(a)$ $w'(b)$ $w'(x)$ $w(x)$ $r(b)$ with $w'(b)$ between $w(b) \leftrightarrow r(b)$ and therefore preventing it from being linearizable.
The following figure shows this case:

- If we add a RW dependency $r(x) \leadsto w'(x)$ (RW1), then, $w(d) \rightarrow r(x) \rightarrow w'(x) \rightarrow w'(d)$ implies a new RW dependency $r(d) \leadsto w'(d)$ (RW2). Now, there exists the path $w(c) \rightarrow r(x) \rightarrow w'(x) \rightarrow w'(c) \rightarrow r(d) \rightarrow w'(d) \rightarrow r(c)$ where $w'(c)$ is between $w(c) \rightarrow r(c)$. This case is represented here:

In sum, the execution in figure 13 is a case where the CO extension
of $<_PO$ is acyclic but the execution does not have a consistent linear extension.

Finally,

- Because each process in the execution of figure 13 has at most one read $r$ and $w$ ($w \rightarrow r$) and $w'$ are not causally related, it is clear that the execution is Causal.

- The following sequence:

$$w(b) \ r(b) \ w'(a) \ w(a) \ r(a) \ w'(b) \ w'(x) \ w(x) \ r(x) \ w(d) \ r(d) \ w(c) \ r(c) \ w'(d) \ w'(c)$$

is a consistent extension of $<_PO | (i, w)$, for all processes simultaneously, which proves the execution in figure 13 is Processor.
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