Towards High Performance, Portability, and Productivity: Lightweight Augmented Neural Networks for Performance Prediction

Ajitesh Srivastava¹, Naifeng Zhang¹, Rajgopal Kannan², and Viktor K. Prasanna¹

¹ University of Southern California, Los Angeles, CA 90089
{ajiteshs,naifengz,prasanna}@usc.edu
² US Army Research Lab-West
rajgopal.kannan.civ@mail.mil

Abstract. Writing high-performance code requires significant expertise of the programming language, compiler optimizations, and hardware knowledge. This often leads to poor productivity and portability and is inconvenient for a non-programmer domain-specialist such as a Physicist. More desirable is a high-level language where the domain-specialist simply specifies the workload in terms of high-level operations (e.g., matrix-multiply(A, B)) and the compiler identifies the best implementation fully utilizing the heterogeneous platform. For creating a compiler that supports productivity, portability, and performance simultaneously, it is crucial to predict performance of various available implementations (variants) of the dominant operations (kernels) contained in the workload on various hardware to decide (a) which variant should be chosen for each kernel in the workload, and (b) on which hardware resource the variant should run. To enable the performance prediction, we propose lightweight augmented neural networks for arbitrary combinations of kernel-variant-hardware. A key innovation is utilizing mathematical complexity of the kernels as a feature to achieve higher accuracy. These models are compact to reduce training time and fast inference during compile-time and run-time. Using models with less than 75 parameters, and only 250 training data instances, we are able to obtain a low MAPE of 13% significantly outperforming traditional feed-forward neural networks on 40 kernel-variant-hardware combinations. We further demonstrate that our variant selection approach can be used in Halide implementations to obtain up to 1.5× speedup over Halide’s autoscheduler.

Keywords: Lightweight augmented neural networks · Performance prediction · Productivity · Portability · Compiler · Heterogeneous Platforms

1 Introduction

With various heterogeneous technologies emerging today, there have been unprecedented opportunities for accelerating applications. Application-specific in-
Integrated circuits (ASICs) provide highly specialized implementations but require expertise in implementation and are specialized for one application. On the other hand, CPUs, GPUs, and FPGAs provide more flexibility and are easier to program, but are much slower compared to ASICs. Providing the flexibility in applications and ease of implementation while reaching the speedup offered by ASICs has been the focus of many recent works. Even writing a CPU/GPU code to get most out of available hardware requires programming expertise, hardware knowledge, and time. Further, that optimized code may not be ‘portable’, i.e., may not work well on a different platform. Finally, a domain-specialist such as a physicist is expected to know the operations involved in their workload, but not the details of their highly-optimized implementations. This is important for ‘productivity’, i.e., implementing the desired workflow with few lines of code, not worrying about the code optimizations.

With the objective of achieving high performance, portability and productivity, we are building a compiler that executes a high-level domain specific language on heterogeneous platforms aligned with recent DARPA projects. The user will write a high level code which can be broken down in high-level operations (matrix multiplication, convolution, etc.), we call kernels. The user only specifies the operation with the inputs such as matrix-multiply(A, B) without worrying about optimized implementation of the actual multiplication, thus enabling high productivity. It is the compiler’s job to automatically identify how to best execute this code by distributing the kernels among the available hardware configurations on the platform.

In order to identify a high performance execution plan, the compiler should be able to predict the performance of a kernel on various hardware resources. This enables the following decisions: (i) Variant selection: A compiler may have several variants implementing the kernel on the same hardware in its library with potentially different performances, e.g., boost library vs eigen library for matrix multiplication. The variation may also come from setting certain parameters in the implementation that affect the runtimes, such as compilation flags and other tunable parameters of the implementation. Given the input, which variant should be selected? (ii) Mapping to hardware: The workload is a collection of possibly interdependent kernels. Each kernel can be mapped to various available hardware resources (CPUs, GPUs, etc.). For each kernel-hardware pair, there may be a different kernel variant that is optimal. Having accurate kernel performance models is crucial for these decisions. We acknowledge that our approach to designing this compiler is not suited for compiling arbitrary low-level code as we rely on already available implementations of certain kernels. However, the kernels chosen in the paper dominate the runtime of many workflows including machine learning. In fact, our chosen kernels covers > 80% of the workflows in the DARPA SDH program. We emphasize that predicting the execution time is more useful than simply knowing the better variant or hardware resource for individual kernels. For instance, suppose, we want to execute two matrix multiplications that do not have any data dependencies on a platform containing a CPU and a GPU. The first one involves matrices of size 100 and
the second of size 10000. While the first multiplication alone may be faster on GPU, it should still be scheduled on the CPU so that the GPU is available for the second which is the larger multiplication.

To enable **portability**, the compiler must support learning performance models of execution times $T(K_i, H_j)$ on arbitrary platforms. We do not assume any access to hardware profilers or details of the kernel implementation. The kernel implementations on various hardware are treated as black-boxes and we can only manipulate the inputs to the implementations. This makes our approach easily extensible, when a new implementation of a kernel is added to the library. These performance models can be trained during compiler installation by generating benchmark datasets for each kernel (along with its variants) on the available hardware. To make this feasible, the models must be lightweight so that they can learn quickly with small training data without overfitting. Once the models are trained, the compiler will be ready for scheduling kernels at compile-time. The prediction may also be needed at runtime. The exact input to the kernel may not be known at compile-time, and therefore, the mapping decisions (which variant to select and where to run) will have to be made dynamically at runtime. Making the models compact is necessary to ensure that they do not constitute a significant portion of the runtime. Here, we build performance models for four ubiquitous kernels [4] found in common workflows (i) Matrix-Matrix Multiplication, (ii) Matrix-Vector Multiplication, (iii) Matrix Convolution, and (iv) Max-Pooling. We propose a novel approach called Augmented Neural Network (NN+C) which are extremely lightweight and utilize the time complexity function to perform execution time prediction. Specifically, our contributions are the following.

- We propose novel lightweight neural network models for kernel performance prediction on CPUs and GPUs.
- We demonstrate that the lightweight models are portable to more than 40 kernel-variant-hardware combinations. Results from 40 of them have been discussed that include 4 kernels each of which have 2 variants on 3 CPUs each and 2 variants on 2 GPUs each.
- We demonstrate that our models achieve low MAPE of 13% with a small training set in a short amount of training time outperforming traditional feed-forward networks for all 40 kernel-variant-hardware combinations.
- We demonstrate that our performance models can be used to identify the best implementation of a kernel where thousands of variants can exist with significantly different runtimes. Specifically, for Halide [7] implementation of Blur filter our approach results in up to $1.5 \times$ speed up over Halide autoscheduler.

## 2 Related Work

Most existing works focus on predicting the performance of the whole specific workload. Huang et. al. [8] use sparse polynomial regression to predict the execution time of arbitrary programs. In [9], a neural network is used to predict the
execution time of a workload. On the other hand, [10] proposes feature selection from workloads to identify similar applications for which the runtimes are known and predicting the runtime for the given application using mean or linear regression. These approaches are limited to one or similar applications, and will require retraining for every application, and thus is not a scalable approach. Further, it is not clear what type of workloads will result in good predictions and if similar approach can be ported to other hardware. Instead, we perform predictions at a coarse-level building blocks of a program on various hardware. If a compiler can predict performance at coarse level operations (kernels such as matrix multiply) on available hardware, it can make mapping decisions accordingly. For this, we consider four kernels that are dominant in many other workloads. Therefore, instead of being tied to a particular workflow, our approach applies to many, such as the entire class of deep learning workloads.

Other existing works [11,12] rely on the instruction set architecture or hardware-specific metrics, which can potentially be used to predict kernel (instead of workload) performance. However, this would require explicit knowledge of the hardware and corresponding profilers, and thus will reduce portability. Our approach enables a black-box treatment of the kernels, and allows prediction without knowing the specific architecture or implementation details. Table 1 summarizes the works closest to ours. Although, we do not compare our approach against the above mentioned works quantitatively, as they are for different objectives, we do show a comparison against their chosen machine learning models (neural networks and linear regression) and show that our lightweight augmented neural networks achieve superior accuracy. Finally, our work is different from [13] as they focus on performance prediction of hardware using hardware profiling instead of performance of dominant operations.

| Approach                        | Workload Coverage | Portability       |
|--------------------------------|-------------------|-------------------|
| Workload-specific [8][9][10]    | Low               | N/A               |
| ISA/Hardware specific [11][12]  | High              | Low/Medium        |
| Our work                       | Medium            | High              |

3 Proposed Approach

**Problem Definition:** For each operation on an arbitrary platform with arbitrary implementations, given corresponding inputs, find a lightweight model which accurately predicts the execution time using a small amount of training time.

To solve this problem, we propose Augmented Neural Network (**NN+C**). The key idea of **NN+C** is utilizing known mathematical function $f(K,H)$ as an extra input to NN. For example, in matrix-matrix multiplication, besides
using basic features such as matrix dimensions, matrix density as inputs, we calculate the number of total operations during matrix-matrix multiplication. Therefore, \( f(K, H) = m \times n \times k \). \( f(K, H) \) for MV, MC, and MP is also calculated similarly. The lightweight aspect enables fast decision making during compile-time as well as run-time. These augmented neural networks provide the flexibility to incorporate any tunable parameter available for the kernel and the hardware.

3.1 Neural Network Structure

The structure of NN+C is shown below in Figure 1. Inputs are (1) known mathematical function \( f(K, H) \), (2) kernel parameters \( K_i \), such as input matrix dimension and matrix density, (3) hardware/code-optimization parameters \( H_i \), for example, how many threads are used in multi-threaded implementation and other controllable features that may affect the runtime such as compilation flags. The neural network also contains hidden layer(s). Output layer only has one node, which is the predicted execution time. The number of hidden layers varies given different kernels and different inputs, resulting in different models for each kernel. Further, the models for a given kernel differ for CPU and GPU due to different inputs. This results in eight different neural network structures (for four kernels and two hardware configurations). In CPU we use multi-threading and take number of threads as an input. However, the structure of the models remain the same irrespective of the implementation of the kernel, and the type of CPU (or GPU). Only the weights of the models will change that are learned during training.

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Fig. 1: Structure of Augmented Neural Network (NN+C)
3.2 Model Inputs

Matrix-Matrix Multiplication ($A_{m,n} \times B_{n,k}$). Inputs are the dimensions of the matrices $m$, $n$, and $k$, densities of matrix $A$ ($d_1 = \frac{\text{number of non-zero entries}}{m \times n}$) and of matrix $B$ ($d_2$), and the number of threads we utilize during multi-threading on CPU, $N_{thd}$, which is an extra input for operations on CPU and not present for GPU. We augment the neural network with $c = f(K, H)$, i.e., roughly the total number of operations in the kernels. In this case, $c = m \times n \times k$.

Matrix-Vector Multiplication ($A_{m,n} \times B_{n,1}$). Inputs are $m$, $n$, $d$, $c$, $N_{thd}$ as defined above. $m$ and $n$ are dimensions of matrix $A$. $d$ is the density of matrix $A$ and the density of vector $B$ is set as 1. $c$ is the number of operations, $c = m \times n$. $N_{thd}$ is the number of threads.

Matrix Convolution ($A_{m,n} \ast B_{r,r}$). Inputs are $m$, $n$, $d$, $c$, $N_{thd}$ as defined above, and $r$ is the dimension of square matrix $B$. $d$ is the density of matrix $A$ and the density of square matrix $B$ is set as 1. The number of operations is given by $c = (m - r + 1) \times (n - r + 1) \times r^2$. $N_{thd}$ is the number of threads.

Max-Pooling ($A_{m,n} \ast B_{s,s}$). Inputs are $m$, $n$, $d$, $c$, $N_{thd}$ as defined above, and $s$ is the dimension of square matrix $B$. $d$ is the density of matrix $A$ and the density of square matrix $B$ is set as 1. The number of operations is given by $c = \left\lceil \frac{m}{s} \right\rceil \times \left\lceil \frac{n}{s} \right\rceil \times s^2$. $N_{thd}$ is the number of threads.

4 Experiments

4.1 Platforms and Optimizations

To demonstrate portability of our models we conducted our experiments on five platforms: Intel(R) Xeon(R) CPU E5-2650 v2 @ 2.60GHz (Xeon), Intel(R) Core i7-8750H CPU @ 2.20GHz (I7), Intel(R) Core i5 CPU @ 2.30GHz (I5), NVIDIA Tesla K40c (Tesla) and NVIDIA Quadro K420 (Quadro).

To perform the kernel operations on CPU, we used Eigen library and Boost library in C++. Eigen/Dense and Eigen/Sparse, uBLAS/matrix and uBLAS/matrix_sparse are used to optimize dense and sparse matrix in each kernel. Multi-threading was also used in Eigen to vary the number of threads. However, it is difficult to vary the number of threads without heavily changing the code structure in Boost library. Owing to our black-box approach, we used single thread in Boost library. Among our platforms, Xeon has 32 cores, 64 threads; I7 has 12 cores, 24 threads; and I5 has 2 cores, 4 threads. For all operations on GPU we used two implementations of CUDA to optimize, one through global memory and one through shared memory. This results in 10 implementations of each kernel: 2 variants of 3 CPUs and 2 variants on 2 GPUs.
4.2 Datasets

We measured the performance of four kernels on each platform: matrix-matrix multiplication (MM), matrix-vector multiplication (MV), matrix convolution (MC) and max-pooling (MP). Other kernels such as LU decomposition and Blur filter were also evaluated, but their results have been omitted due to brevity. For each kernel-variant-hardware combination (there are 40 such combinations), we generated 500 instances of data, where 250 instances were used to train the model and 250 instances to test. Each data instance was generated randomly with ranges of parameters as described in Table 2. While the experiments may be conducted with a different set of ranges, we chose these ranges as they are common sizes for deep learning workflows. Since we use multi-threading on CPU, all operations on CPU take an extra input $N_{thd}$, which is randomly generated between 1 to the maximum threads supported by the given platforms.

Table 2: Parameters for data generation

| Kernels                 | Parameters                                                                 |
|-------------------------|-----------------------------------------------------------------------------|
| Matrix-Matrix Multiplication | $m, n, k \in \{1, 2, 3, \ldots, 1024\}$  
  $d_1 \in \{1, \frac{1}{2}, \frac{1}{4}, \ldots, \frac{1}{2^{\log_2 m \times n}}\}$  
  $d_2 \in \{1, \frac{1}{2}, \frac{1}{4}, \ldots, \frac{1}{2^{\log_2 n \times k}}\}$ |
| Matrix-Vector Multiplication | $m, n \in \{1, 2, 3, \ldots, 1024\}$  
  $d \in \{\frac{1}{2}, \frac{1}{4}, \frac{1}{8}, \ldots, \frac{1}{2^{\log_2 n \times m}}\}$ |
| Matrix Convolution       | $r \in \{3, 5, 7\}$  
  $m, n \in \{r, r + 1, r + 2, \ldots, 1024\}$  
  $d \in \{1, \frac{1}{2}, \frac{1}{4}, \ldots, \frac{1}{2^{\log_2 m \times n}}\}$ |
| Max-Pooling              | $r \in \{2, 3, 4, 5\}$  
  $s \in \{1, 2\}$  
  $m, n \in \{r, r + 1, r + 2, \ldots, 1024\}$  
  $d \in \{1, \frac{1}{2}, \frac{1}{4}, \ldots, \frac{1}{2^{\log_2 m \times n}}\}$ |

4.3 Models

Our augmented neural network models are built under TensorFlow framework. Each model is kept under 100 parameters to maintain lightweight and a short training time. Except for the model for matrix-matrix multiplication on CPU which has 3 dense layers, all the other models have 2 dense layers. All models use ReLU as activation function. Learning rate is set to 0.0001. Loss function is chosen to be mean squared error. Each epoch included training with full batch. The number of parameters of each model as well as its average training time are shown in Table 3.
Table 3: Number of parameters and average training times

|    | MM | MV | MC | MP |
|----|----|----|----|----|
| CPU| 75, 30s | 71, 26s | 73, 25s | 73, 20s |
| GPU| 73, 26s | 61, 12s | 71, 25s | 73 15s |

4.4 Baselines

We compare our method against four baselines: (1) Neural Network (NN). NN is same as the implementation of NN+C except that NN does not take the number of operations as an extra input. (2) Constant (Cons). In Cons, we only take the number of operations as an input and try to predict execution time using linear regression. (3) Linear Regression (LR). We take the same inputs as NN but use linear regression in LR. (4) Non-Linear Regression (NLR). In NLR we take same inputs as NN (and LR) but use non-linear regression with tanh as the activation function.

4.5 Evaluation Metrics

We used mean absolute error (MAE) to evaluate the predictions \{\hat{t}_1, \hat{t}_2, \ldots, \hat{t}_N\} obtained by the baselines and our models w.r.t. the ground truth \{t_1, t_2, \ldots, t_N\}:

\[
MAE = \frac{1}{N} \sum_i |t_i - \hat{t}_i|.
\]

MAE was chosen as the primary metric as ultimately these performance prediction models will be used to measure absolute execution times which will be the sum of execution times of several kernels in the critical path of the workload. Therefore, it will be affected by absolute errors than mean absolute percentage error (MAPE). We also report MAPE.

\[
MAPE = \frac{100}{N} \sum_i \frac{|t_i - \hat{t}_i|}{t_i}.
\]

5 Results

Figures 2 shows a visualization of using NN+C to predict kernel performance on two platforms. We choose the results of I5 and Tesla to represent the results on CPU and GPU, respectively. We pick matrix dimension as x-axis, plotting against execution time in seconds to visualize prediction. A line joining two points in the plot indicates the corresponding prediction and ground truth. Note that very few points have a significant misprediction. Tables 4, 5, 6, and 7 quantify these results using MAE.

For all five kernels using any implementation, NN+C produces the lowest MAE in predictions. Ranking from the highest accuracy (lowest error) on average
Fig. 2: Performance predictions of four kernels using NN+C
### Table 4: Matrix-Matrix Multiplication

|          | Eigen | Boost | CUDA Global Memory | CUDA Shared Memory |
|----------|-------|-------|--------------------|-------------------|
| ×10⁻⁴ s | Xeon I7 | I5  | Xeon I7 | I5  | Tesla | Quadro | Tesla | Quadro |
| NN+C     | 426    | 428   | 639    | 3470 | 5370  | 2.07   | 2.15  | 0.954 | 1.04  |
| NN       | 590    | 1050  | 779    | 8730 | 9170  | 4.28   | 2.27  | 7.10  | 2.96  |
| Cons     | 1960   | 693   | 1350   | 12810 | 9530  | 2.25   | 2.27  | 1.12  | 1.10  |
| LR       | 2050   | 675   | 2400   | 22270 | 14450 | 21.8   | 21.7  | 8.49  | 8.45  |
| NLR      | 1650   | 1210  | 2220   | 18700 | 11350 | 2.07   | 2.07  | 1.12  | 1.10  |

### Table 5: Matrix-Vector Multiplication

|          | Eigen | Boost | CUDA Global Memory | CUDA Shared Memory |
|----------|-------|-------|--------------------|-------------------|
| ×10⁻⁴ s | Xeon I7 | I5  | Xeon I7 | I5  | Tesla | Quadro | Tesla | Quadro |
| NN+C     | 4.25   | 2.76  | 7.52   | 114  | 72.9  | 0.115  | 0.122 | 0.0893 | 0.104 |
| NN       | 7.38   | 5.78  | 8.94   | 143  | 83.6  | 0.116  | 0.156 | 3.16   | 1.14  |
| Cons     | 11.0   | 7.63  | 11.6   | 156  | 86.9  | 0.384  | 0.386 | 0.0980 | 0.125 |
| LR       | 25.0   | 14.0  | 24.7   | 189  | 99.9  | 0.636  | 0.640 | 0.244  | 0.247 |
| NLR      | 13.7   | 10.5  | 14.6   | 174  | 93.0  | 0.155  | 0.155 | 0.0925 | 0.138 |

### Table 6: Matrix Convolution

|          | Eigen | Boost | CUDA Global Memory | CUDA Shared Memory |
|----------|-------|-------|--------------------|-------------------|
| ×10⁻⁴ s | Xeon I7 | I5  | Xeon I7 | I5  | Tesla | Quadro | Tesla | Quadro |
| NN+C     | 400   | 480   | 179    | 206  | 115   | 130   | 77.9  | 1.22   | 2.39   | 2.90  |
| NN       | 419   | 531   | 351    | 356  | 122   | 243   | 0.979 | 1.47   | 2.21   | 3.68  |
| Cons     | 1310  | 1110  | 1150   | 254  | 157   | 244   | 4.34  | 4.48   | 5.81   | 5.93  |
| LR       | 2510  | 1560  | 2330   | 872  | 521   | 744   | 5.75  | 5.89   | 5.56   | 5.73  |
| NLR      | 1820  | 1200  | 1580   | 694  | 442   | 592   | 2.91  | 2.96   | 3.38   | 3.53  |

### Table 7: Max-Pooling

|          | Eigen | Boost | CUDA Global Memory | CUDA Shared Memory |
|----------|-------|-------|--------------------|-------------------|
| ×10⁻⁴ s | Xeon I7 | I5  | Xeon I7 | I5  | Tesla | Quadro | Tesla | Quadro |
| NN+C     | 106   | 66.1  | 134    | 55.2 | 34.9  | 95.2   | 742   | 784    | 2.73  | 3.66  |
| NN       | 119   | 91.0  | 229    | 67.8 | 44.2  | 129    | 1680  | 1360   | 5.43  | 4.60  |
| Cons     | 3190  | 73.0  | 290    | 155  | 79.1  | 172    | 4200  | 4210   | 3.14  | 4.44  |
| LR       | 581   | 342   | 526    | 250  | 158   | 266    | 8430  | 8420   | 4.27  | 6.55  |
| NLR      | 418   | 232   | 363    | 191  | 112   | 190    | 6530  | 6520   | 3.46  | 4.67  |

### Table 8: Aggregated MAPE error of NN+C vs NN

|          | MM | MV | MC | MP | CPU | GPU |
|----------|----|----|----|----|-----|-----|
| NN+C     | 17.69%| 10.54%| 13.06%| 10.72%| 15.18%| 10.09%|
| NN       | 36.48%| 15.67%| 17.38%| 14.40%| 23.90%| 16.50%|
to the lowest is: (1) NN+C, (2) NN, (3) Cons, (4) NLR, (5) LR. The accuracy of NN is closer to NN+C compared to other methods. NN+C and NN also provide a more stable performance across variants and platforms in predicting each operation. Cons has a good prediction for kernels on GPU. Performance of LR and NLR are worst among all kernels on all platforms.

Overall, NN+C predicts more accurately for kernels on GPU than those on CPU. As we can see in Figure 2, matrix-matrix multiplication on CPU is the worst predicted operations. As for matrix-matrix multiplication, NN+C leads to 0.0498s MAE on CPU on average using Eigen and 2.11 × 10⁻⁴s on GPU on average using Global Memory. This is around 10% of the average execution time. A possible reason is that matrix-matrix multiplication has four different implementations within the same library (Eigen or Boost), making it harder to predict through one model – dense matrix multiplied with dense matrix, dense matrix multiplied with sparse matrix, sparse matrix multiplied with dense matrix, and sparse matrix multiplied with sparse matrix.

We report the average error in MAPE for the four kernels and the two hardware classes (CPU, GPU) in Table 8. For each kernel, MAPE was aggregated over all hardware and variants. For each hardware class, MAPE was aggregated over all the kernels, variants and specific device. We show the comparison of NN+C against the best performing baseline NN. NN+C significantly outperforms NN in all cases. In fact, for MM, MAPE for NN+C is less than half of that of NN suggesting that a simple neural network is far inferior than our augmented neural networks.

|        | MM    | MV    | MC    | MP    |
|--------|-------|-------|-------|-------|
| CPU    | 6.46x, 19.21x | 5.96x, 1.99x | 10.73x, 2.21x | 6.61x, 2.48x |
| GPU    | 4.04x, 8.23x | 4.78x, 1.98x | 1.95x, 1.99x | 2.07x, 1.98x |

**Unconstrained Augmented Neural Networks.** To enable fast inference, our models are kept extremely lightweight – less than 75 weights. Also, we only generate 500 data instances for each kernel-variant-hardware combination, out of which 250 are used to train our models. In order to assess how much of the performance is compromised due to these restrictions, we build similar NN+C models with more parameters and generate larger dataset with 5000 data instances (2500 instances are used to train and 2500 to test). Figure 3 illustrates the comparison between lightweight models and unconstrained models in terms of error. Overall, MAE achieved by lightweight NN+C is kept under 0.08s and by unconstrained NN+C is kept under 0.02s. Specifically, on CPU, using unconstrained NN+C, MM, MV, MC, and MP have a decrease on average MAE of 0.04s, 0.004s, 0.02s, and 0.008s, respectively. On GPU, using unconstrained NN+C, MM, MV, MC, and MP have a decrease on average MAE of 1 × 10⁻⁴s, 3 × 10⁻⁶s, 2 × 10⁻⁵s, and
$1 \times 10^{-4}$s, respectively. However, accuracy comes at the cost of increased model size and the overall time as summarized in Table 9. If the training and inference time are not constrained, then one can use our unconstrained (larger and more accurate) augmented models. However, we envision that lightweight models may be necessary due to the following reasons: (a) At compile-time many kernels need to be evaluated: Consider VGG16 inference that requires $>1$M 2D-Convolutions. At a given layer, there can be $>100$K 2D-Convolutions, each of which may have different execution times not only due to heterogeneous hardware, but also due to different sparsity. This number of Convolutions will multiply with the factor of number of parallel image classification pipelines. (b) Some decisions may have to be made at runtime: Some kernels may be only instantiated at runtime, which is the only time performance prediction inference has to be performed. In such scenarios, the inference should have an insignificant impact on the total runtime.

6 Demonstration of Variant Selection

As a crucial application of our performance prediction approach, we demonstrate that it can be used to pick the best variant for a given kernel, i.e., picking the best available code among several options. This may mean choosing between a CPU and a GPU implementation or identifying compilation flags that will
be best suited for the kernel. To show the variant selection capability of our approach we choose a scenario where number of variants can be extremely high. Further, we choose a different kernel than the four discussed thus far to show generalizability of our approach.

We consider the kernel Blur implemented in Halide [7]. A Halide code decouples the functional program from its execution “schedule” that determines various aspects of the execution such as ordering of the loops, degree of unrolling loops, and vectorization strategy. The schedule description may be seen as a combination of shape (feature space) and parameters. For instance, `blur.y.tile(x, y, xi, yi, 128, 256)` defines two dimensions of the shape and the parameters 128 and 256 determine the tunable parameters along these dimensions. Changing the schedule does not affect the output of the code, but it may significantly affect the runtime. Therefore, each schedule generates a variant of the same kernel, and our task is to identify the best variant to use. We train our compact augmented neural networks with additional inputs representing the schedule features. This allows us to quickly estimate runtimes of the code with various schedule parameters without actually executing the code. Halide provides an autoscheduler that attempts to identify the best schedule itself. We run the autoscheduler to identify the shape/feature space and ignore the suggested parameters. Within this feature space we generate candidate schedules $S = \{s_1, s_2, s_3, \ldots, s_N\}$, where each $s_i$ is a vector of parameters, and find $s = \arg \min_i P_{NN}(s_i)$, where $P_{NN}(s_i)$ represents the predicted runtime. Figure 4 shows the comparison of execution times for varying input sizes. Our predicted best schedule produces a runtime close to the true best schedule within the candidate set in all cases. Further, the plot shows that using our predictions, we were able to outperform Halide’s autoscheduler, getting up to 1.5× speedup.

![Fig. 4: Runtime comparison of variants obtained from auto-scheduler and our approach.](image-url)
7 Conclusion

We have proposed a novel lightweight augmented neural network model (NN+C), to predict kernel performance on CPUs and GPUs. Our approach is designed in support of creating compilers with high productivity, portability and performance. To show that our models are portable to different platforms with different implementations, we have evaluated our model on several CPUs and GPUs with multiple optimizations, resulting in a total of 40 kernel-variant-hardware combinations. Our models significantly outperformed the baselines including standard neural network. We have shown that our approach can be used to identify best variants even when the number of variants is extremely high. We do so by demonstrating a 1.5× speedup over Halide autoscheduler. In future work, we will build prediction models for other popular kernels. These models will be used to perform optimized mapping of kernels in workflows for various heterogeneous platforms.

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