A Desktop Electric Machine Emulator Implementation Method Based on Phase Voltage Reconstruction

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ABSTRACT An electric machine emulator (EME) system plays a fundamental role in design and validation of hardware and software for power electronic converters and electric drives. In this paper, a desktop digital signal processor (DSP)-based EME is developed for power converters function test. The principle of EME is demonstrated with mathematical derivation. Since the instantaneous phase voltage is either power supply voltage or ground, high-rated voltage sensors are not suitable for DSP-based EME to obtain the average voltage in a pulse-width modulation cycle. To accurately acquiring phase voltages, a method which reconstructs the phase voltage considering the amplitude and duty cycle error is proposed. Voltage drops, dead time, propagation delay, parasitic rising and falling time delay are all considered in reconstructed voltages based on voltage-second balance theory. This is accomplished without any assistant physical circuits. Based on the reconstructed phase voltages, reference current is derived in motor model by using second order Runge-Kutta method. Factors affecting phase voltage accuracy are verified by simulations step by step. The simulation and experimental results support the validity of the proposed method.

INDEX TERMS Electric machine emulator (EME), phase voltage reconstruction, compensation time.

I. INTRODUCTION

The development and validation of power electronics of motor control units (MCU) are facing great challenges since the existing facilities do not fit desired requirements. A test bench called electric machine emulator (EME) or power-level hardware-in-the-loop (PHIL) emerges in such situation. Compared with dyno test bench, EME holds the merits of low cost, short time-to-market cycle, testing extreme conditions, etc. Therefore, it is widely used in electric vehicles [1], [2], aerospace [3], wind power generation [4] and other fields.

The principle of EME system is to mimic the motor electrical characteristics via current tracking. The target current is calculated by motor model whose input is phase voltages. A typical EME schematic diagram is shown in Fig. 1. It consists of output filters, power amplification unit (PA), interface algorithms (IA), real-time digital system (RTDS) and sampling circuits. The function of output filter is to filter high-frequency phase current harmonics caused by inverters. The structure of output filters can be L [5] or LC [6] or LCL [7] type. Comparisons are carried out in [8] in four aspects and it concludes that the LCL type has better performance but needs accurate state equation, or else the system will be unstable. L type is a first-order system which has better robustness. Paper [9] gives out L type inductance selection form according to the max current tracking slope and max current fluctuation restriction. PA is the core part to output voltages to regulate the current. Paper [10] points out that ideal PA owns the traits of unit gain, infinite bandwidth and no time delay. The frequently-used PA is switched-mode type which can be classified as two-level inverter and multi-level inverter. Multi-level PA [11]–[13] can reach higher output frequency and lower current harmonics via parallel connection and phase-shift sinusoidal pulse-width modulation (PS-SPWM) control, which is always used in Field Programmable Gate Array (FPGA)-based EME system.
This structure may bring complexity like common mode current [5] and branch current balance problem [14]. As for IA part, IA realizes the current tracking algorithm of target current by RTDS and sampling current. Paper [15] adopts PI controller which is simple, but it may lead to instability of current tracking when operation state changes. Paper [16] combines back electromagnetic force feedforward control and PI control to increase stability. Paper [17] compares the stability and accuracy of five different IAs. Paper [18] proposes an accurate evaluating method based on transfer function. RTDS includes FPGA and DSP. FPGA [19] owns the traits of fast speed (over 500KHz) and high accuracy. DSP-based EME can lead to lower price for partial function testing.

As for sampling circuits in EME system, current is captured by high precision current sensor directly. The sampling voltage is the input of motor model which will transfer the sampling error to motor model and influence the accuracy of system. The terminal voltage sampling method can be divided into two types: the high-rated AD chip to capture the instantaneous line-line voltage [20] and the voltage integrator to calculate equivalent voltage in a given time [21]. The high-rated AD chip (higher than 1MHz) can just be used on FPGA-based EME system since the motor model calculating frequency is at about 1MHz or higher. It is not suitable for DSP-based EME system with 10KHz model calculating frequency. For DSP-based EME system, the latter method is a better choice. Paper [22] uses the voltage integrator to capture the terminal voltage indirectly which will cause sampling error with the existing of lowpass filter or resetting of the integrator. In a specific condition, the integral time is equal to PWM period and the terminal voltage can be obtained by real PWM capturing with a comparator circuit [23], but this method does not consider the voltage drops of diodes and insulated gate bipolar translators (IGBTs). Thus, an accurate and reliable equivalent phase voltage sampling method is necessary.

In this paper, an accurate phase voltage sampling method based on phase voltage reconstruction used on DSP-based EME system is proposed. Section II introduces the principle of EME. Section III are the proposed phase voltage reconstruction method. Section IV and V are simulation and experimental verification of the proposed method. Section VI lays the conclusion.

II. PRINCIPLE OF EME

The implementation schematic of EME system in this paper is shown in Fig. 2. Compared with Fig. 1, this implementation substitutes the regenerative system with direct current (DC) power supply or battery and the energy is absorbed directly. Meanwhile, the line voltage sampling unit is removed. The MCU inverter and EME inverter are both voltage source two-level converters and have independent power supply.

A. MATHEMATICAL DERIVATION OF EME

The mathematical model of EME is derived based on Fig. 2 schematic. The power supply of MCU and EME are defined as $U_{DC}$ and $U_{dc}$ respectively. Points $O$ and $N$ are reference ground for MCU and EME. The operation of upper inverter is defined as $S_x = 1$, $x \in \{A, B, C, a, b, c\}$, while
$S_i = 0$ for lower inverter operation. $L_f$ and $R_f$ are output filter inductance and its equivalent resistance. $i_s$ are phase current.

According to Kirchhoff voltage law,

$$U_{AO} = U_{Aa} + U_{aN} + U_{NO}$$  \hspace{1cm} (1)

where,

$$U_{AO} = S_A \cdot U_{DC}, \quad U_{Aa} = L_f \frac{di_a}{dt} + R_f i_a, U_{aN} = S_a \cdot U_{dc}.$$  \hspace{1cm} (2)

Equation (1) can be rewritten as (2).

Similarly, we can get the other two phase equations. For motor model, we can obtain (3) based on Kirchhoff current law.

$$i_a + i_b + i_c = 0$$  \hspace{1cm} (3)

Adding three phase voltage equation, reference point voltage can be written as

$$U_{NO} = \frac{U_{DC}}{3} (S_A + S_B + S_C) - \frac{U_{dc}}{3} (S_a + S_b + S_c)$$  \hspace{1cm} (4)

One can deduce mathematical model of EME by introducing (4) into (2)

$$\frac{U_{DC}}{3} (2S_A - S_B - S_C) = L_f \frac{di_a}{dt} + R_f i_a + \frac{U_{dc}}{3} (2S_a - S_b - S_c)$$  \hspace{1cm} (5)

The expression of $d$-$q$ rotating coordinate axis (6) can be obtained using PARK transformation from (5).

$$\begin{cases} U_{q,mcu} = L_f \frac{di_q}{dt} + R_f i_q + \omega L_i d + U_{q,eme} \\ U_{d,mcu} = L_f \frac{di_d}{dt} + R_f i_d - \omega L_i q + U_{d,eme} \end{cases}$$  \hspace{1cm} (6)

Equation (6) is the foundation of current control. We can derive the mathematical model of PMSM in $d$-$q$ axis, $i_d$ and $i_q$ are $d$-axis and $q$-axis currents, $U_{d,mcu}$ and $U_{q,mcu}$ are $d$-axis and $q$-axis voltages of EME part, $U_{d,mcu}$ and $U_{q,mcu}$ are $d$-axis and $q$-axis voltages of MCU part.

$$\begin{align*}
U_{q,mcu} &= L_f \frac{di_q}{dt} + R_f i_q + \omega_L L_i d + U_{q,eme} \\
U_{d,mcu} &= L_f \frac{di_d}{dt} + R_f i_d - \omega L_i q + U_{d,eme}
\end{align*}$$  \hspace{1cm} (7)

$$ \begin{align*}
U_{d,mcu} &= L_f \frac{di_d}{dt} + R_f i_d - \omega_L L_i q + U_{d,mcu} \\
T_e &= \frac{3}{2} n_p (\psi i_q - \psi q i_d) \\
T_e - T_L - B \omega &= \frac{J \omega}{dt}
\end{align*}$$  \hspace{1cm} (8)

(A) VOLTAGE DISTORTION ANALYSIS

Insertion of dead time, nonideal characteristics of inverters like turn-on/-off delays, voltage drop of inverters and parasitic capacitor of switching device are the prime reasons for voltage distortion. This paper takes dead time, propagation delay, turn-on/-off time, voltage drops and parasitic capacitor influence into consideration. The voltage distortion analysis is shown in Fig. 4. $PWM_{Ideal}$ is the ideal given PWM, $PWM_{DT}$ inserts the dead time, $PWM_{DT+TR}$ considers the propagation delay and turn-on/-off time. $U_{Ideal}$, $U_{Actual}$ and $U_{DT}$ are ideal output terminal voltage, actual output terminal voltage and equivalent actual output terminal voltage. The current is defined as positive when it flows from MCU to EME, vice versa.
In Fig. 4, the definitions of symbols are listed as follows. $T_d$ is the dead time; $T_{on}$, $T_{off}$, $T_{don}$, $T_{doff}$ are propagation delay of rising edge, propagation delay of falling edge, turn-on delay and turn-off delay respectively; $T_r$ and $T_f$ are equivalent rising time and falling time based on voltage-second balance theory; $T_{PWM}$ and $T_H$ are PWM period and high voltage duration time, respectively; $U_{DC}$, $U_D$, $U_F$ are dc bus voltage, diode voltage drop and IGBT feedforward voltage drop respectively; $\Delta T_{rise}$ and $\Delta T_{fall}$ are the total delay of the rising edge and falling edge, respectively.

**B. VOLTAGE MAGNITUDE RECONSTRUCTION**

The magnitude of output terminal voltage is influenced by the voltage drops of diodes or IGBTs. The voltage drops directly depend on the current value and the sign of current. A precise current measurement is required to determine the voltage drops. Since a precise current sensor is essential for EME system to operate current tracking, it is not an issue. We just need to get the voltage drop values of diodes and IGBTs. Usually, the forward voltages of semiconductor components of the same type, voltage and power class are in the same order. The voltage drops of diode and IGBT can be tested directly. The voltage drops of IGBT and diodes are shown in Fig. 5 and Fig. 6. $V_{CE}$ and $V_{EC}$ is IGBT voltage drop and diode voltage drop, respectively. The relationship between current and voltage drops is shown in Fig. 7. $U_{AL}$ represents the terminal voltage of phase A and only the low voltage part is shown.

**C. PULSE WIDTH RECONSTRUCTION**

The pulse width error between ideal and actual pulse width is demonstrated in Fig. 4. $T_e$ is defined as pulse width error.
One can obtain $T_c$ equation from $\Delta T_{\text{rise}}$ and $\Delta T_{\text{fall}}$.

$$
\begin{align*}
\Delta T_{\text{rise}} &= T_d + T_{\text{ton}} + T_{\text{don}} + T_r \\
\Delta T_{\text{fall}} &= T_{\text{toff}} + T_{\text{doff}} + T_f \\
T_c &= T_d + (T_{\text{ton}} - T_{\text{toff}}) + (T_{\text{don}} - T_{\text{doff}}) + (T_r - T_f) \\
&= T_d + (T_r - T_f) \quad (i > 0) \\
&= -T_d + (T_r - T_f) \quad (i < 0)
\end{align*}
$$

(13)

In equation (13), dead time $T_d$ can be considered as constant. For transformation time $T_{\text{ton}}, T_{\text{toff}}$ and turn-on/-off time $T_{\text{don}}, T_{\text{doff}},$ they change little from the rising edge to the falling edge since the current can be seen as a constant in a PWM period. They can be seen as offsets, but not affect the value of $T_c$. Therefore, equation (13) can be simplified to (14).

$$
T_c = \begin{cases} 
T_d + (T_r - T_f) & (i > 0) \\
-T_d + (T_r - T_f) & (i < 0)
\end{cases}
$$

(14)

As for rising time $T_r$ and falling time $T_f$, they cannot be counteracted since the charging and discharging effect of parasitic capacitor of IGBT differ a lot even in a same current condition. Hence, the effect of rising time $T_r$ and falling time $T_f$ will be studied in detail.

As mentioned above, rising time $T_r$ and falling time $T_f$ are affected by current amplitude and polarity and parasitic capacitor. The influence can be elaborated by (15)

$$
v = i_r t / C_p
$$

(15)

where, $v$ is terminal voltage, $C_p$ is the sum of parasitic capacitor of upper and lower switch, $i_r$ is current at the rising edge which is assumed as constant in $T_d$ time.

We define a critical current $I_c$ shown in (16), in which current, the terminal voltage reaches $U_{\text{DC}}$ at the time of $T_d$ in the function of capacitor.

$$
I_c = U_{\text{DC}} C_p / T_d
$$

(16)

When current at the rising edge $T_r$ is positive, the time $T_r$ is short enough to be omitted since the parasitic capacitor is connected to positive pole of DC link directly after the upper switch is under operation. Fig. 8(a) shows the equivalent rising time at various current according to voltage-second balance theory which is demonstrated that the blue shadow area equal to the red shadow area. According to Fig. 8(a), we derive the rising time $T_r$ as (17). In which, $G_H$ and $G_L$ are gate signal of upper switch and lower switch, respectively.

$$
T_r = \begin{cases} 
\frac{U_{\text{DC}} C_p}{-2i_r} & (i_r \leq -I_c) \\
T_d - \frac{i_r T_d^2}{2U_{\text{DC}} C_p} & (-I_c < i_r < 0) \\
0 & (i_r > 0)
\end{cases}
$$

(17)

Similarly, when current at the falling edge $T_f$ is negative, the time $T_f$ is short enough to be omitted since the parasitic capacitor is connected to negative pole of DC link directly after the lower switch is under operation. Fig. 8(b) shows the equivalent falling time at various current. The falling time $T_f$ at various current can be written as (18).

$$
T_f = \begin{cases} 
0 & (i_f < 0) \\
T_d - \frac{i_f T_d^2}{2U_{\text{DC}} C_p} & (0 < i_f < I_c) \\
\frac{U_{\text{DC}} C_p}{2i_f} & (i_f \geq I_c)
\end{cases}
$$

(18)

The experimental result at the condition of $T_d = 3\mu s$, $U_{\text{DC}} = 210V, C_p = 1nF$ is shown in Fig. 9. It coincides with the conclusion above.

### D. PHASE VOLTAGE RECONSTRUCTION CONSIDERING BOTH FACTORS

Take phase A as an example, $i_A$ is the current of phase A, equation (18) can be obtained.

$$
T_c = \begin{cases} 
\frac{i_A T_d^2}{2U_{\text{DC}} C_p} & (-I_c < i_A < I_c) \\
T_d - \frac{U_{\text{DC}} C_p}{2i_A} & (i_A \geq I_c \ or \ i_A \leq -I_c)
\end{cases}
$$

(19)
The terminal voltage error in one operation period can be concluded according to the voltage-second balance principle. When current $i_A$ is positive, we can get:

$$
\Delta U_A = \frac{T_c}{T_{PWM}} \cdot (U_{DC} + U_D - U_F) + \frac{T_H}{T_{PWM}} \cdot U_F + (1 - \frac{T_H}{T_{PWM}}) \cdot U_D \quad (20)
$$

When current $i_A$ is negative, we can derive:

$$
\Delta U_A = -\frac{T_c}{T_{PWM}} \cdot (U_{DC} + U_D - U_F) - (1 - \frac{T_H}{T_{PWM}}) \cdot U_F - \frac{T_H}{T_{PWM}} \cdot U_D \quad (21)
$$

The value $T_{PWM}$ and $T_H$ can be obtained by the transfer of MCU. This makes the MCU is open for EME, which can be in situation that low-cost EME is setup by the same producer of MCU. We can get the equivalent terminal $U_A$ voltage via (22).

$$
U_A = T_H U_{DC} - \Delta U_A \quad (22)
$$

With the same principle, we can get the equivalent voltage of phase B and C. The phase voltage of A defined as $U_{phA}$ can be reconstructed by (23).

$$
U_{phA} = \frac{2U_A - U_B - U_C}{3} \quad (23)
$$

And the same for phase voltage B and C.

### TABLE 1. Parameters of EME.

| Items                | Values    |
|----------------------|-----------|
| $U_{dc}$             | 30V       |
| Model Calculating Step Size | 100μs   |
| Model Calculating Method | Second Order Runge-Kutta |
| Filter Inductor      | 5mH       |
| Inductor Resistance  | 0.3Ω      |

### IV. SIMULATION RESULTS

The voltage drops and PWM transfer nonlinearity can be analyzed and verified in simulation, respectively. To verify the effectiveness of the reconstruction method, an EME simulation model is built up on Matlab/Simulink according to EME principle in Section II. The EME setup parameters and PMSM parameters are shown in TABLE 1 and TABLE 2, respectively. A reference PMSM model is also setup as a comparison to further verify the effectiveness. The command signals of reference PMSM model are the same as the EME system. The simulation adopts $V/f$ open-loop control strategy. The simulation result analyses mainly focus on the comparison of voltage waveforms and current waveforms among ideal EME output without considering the nonlinearity, EME output using captured voltage value and EME output adopting reconstruction method. Since voltage is the prerequisite for current response, the voltage error and current error are both displayed.

### TABLE 2. Parameters of PMSM.

| Items                | Values    |
|----------------------|-----------|
| Rated Power          | 750W      |
| Rated Voltage        | 200V      |
| Rated Current        | 4A        |
| Rated Torque         | 2.4N·m    |
| Rated Speed          | 3000r/min |
| Poles Pairs          | 4         |
| D axis Inductance    | 5.14mH    |
| Q axis Inductance    | 5.16mH    |
| Flux Linkage         | 0.089Wh   |
| Stator Resistance    | 1.2Ω      |

### FIGURE 10. Simulation results when considering the voltage drops only.

**A. VOLTAGE MAGNITUDE RECONSTRUCTION VERIFICATION**

The effects of voltage drops are demonstrated in this section, and non-ideal characteristics of inverters are ignored. Fig. 10(a) green curve is the ideal PWM output voltage, blue curve is the voltage captured by high-precision voltage sensor as a reference, and red curve is the voltage reconstructed using the proposed reconstruction method. So do Fig. 11(a) and Fig. 12(a). Since the voltage drops are neglected, the ideal voltage is larger than captured and reconstructed voltage. The captured and reconstructed voltage almost coincide with each other which means the voltage reconstruction method is effective. Compare the reconstructed voltage with the captured voltage and ideal output voltage, we obtain the voltage error shown in Fig.10(b). Current is the result of voltage via PMSM model calculation, three corresponding
current is shown in Fig. 10(c). The current using the reconstructed voltage can track the current using captured voltage.

### B. PULSE WIDTH RECONSTRUCTION VERIFICATION

The effects of EME inverter non-ideal characteristics like dead time insertion and transfer delay are considered in this section, other conditions remain ideal. The simulation results are shown in Fig. 11. From Fig. 11(b), one can see that the insertion of dead time and transformation delay lead to square wave voltage error. Fig. 11(c) shows the duty cycles of the corresponding voltage in Fig. 11(a). Fig. 11(d) shows the current comparison.

### C. PHASE VOLTAGE RECONSTRUCTION VERIFICATION CONSIDERING BOTH FACTORS

This part takes the both factors into consideration. Fig. 12 demonstrates the simulation results. The figures are corresponding to Fig. 11. We can conclude that the reconstructed voltage and current can perfectly track those captured by the voltage sensors.

### V. EXPERIMENTAL RESULTS

The experimental platform is set up to verify the method, the parameters are same as TABLE 1 and TABLE 2. The processors of MCU and EME are both DSP28335. The inserted dead time is 3us.

#### A. PHASE VOLTAGE RECONSTRUCTION

Since the voltage drops and non-ideal characteristics of inverters cannot be verified independent, this part gives the comprehensive experimental verification results. Constant $V/f$ control strategy at 10V/14Hz is carried out. The results demonstrate the reconstruction method is effective.

#### B. SAME METHOD USED FOR EME COMPENSATION

Since the EME part adopts the same voltage source inverter as the MCU, the EME inverter will have voltage output distortion which will cause the current distortion. The real output voltage and the target output voltage of EME are not...
the same due to the existing of voltage drops, dead time and transfer delay. Fig. 14 gives out the current clamping phenomenon caused by voltage distortion. One can see that the distortion pollutes the current output harmonics which do not exist in real current. It is necessary to compensate the voltage distortion for EME inverters which will largely improve the current harmonics performance. Fig. 15 gives out the current output analysis without and with the voltage compensation method. Compare Fig. 15(a) and Fig. 15(b), we can see the total harmonics distortion (THD) of the compensated waveform is largely decreased.

**VI. CONCLUSION**

In this paper, a desktop DSP-based EME system is setup for the validation of power converters and electric drives. A method is proposed to improve the EME accuracy without using any high-speed high-accuracy voltage sensors. It reconstructs the phase voltages by considering the voltage drops and non-ideal characteristics of voltage source converters. Voltage drops, dead time, propagation delay, parasitic rising and falling time delay are all considered in reconstructed voltages based on voltage-second balance theory. Simulation and experimental results demonstrate the proposed method can improve the EME current tracking accuracy. Moreover, the developed method can also be applied for EME compensation which can reduce the inverter harmonics.

**REFERENCES**

[1] S. Uebener, “Application of an e-machine emulator for power converter tests in the development of electric drives,” in *Proc. Eur. Electr. Vehicle Congr.*, Nov. 2012, pp. 1–9.

[2] L. Herrera, C. Li, X. Yao, and J. Wang, “FPGA-based detailed real-time simulation of power converters and electric machines for EV HIL applications,” *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1702–1712, Mar. 2015.

[3] X. Liu and A. J. Forsyth, “Active stabilisation of a PMSM drive system for aerospace applications,” in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2008, pp. 283–289.

[4] F. Huerta, R. L. Tello, and M. Prodanovic, “Real-time Power-Hardware-in-the-Loop implementation of variable-speed wind turbines,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 1893–1904, Mar. 2017.

[5] K. Saito and H. Akagi, “A power Hardware-in-the-Loop (P-HIL) test bench using two modular multilevel DSCC converters for a synchronous motor drive,” *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 4563–4573, Sep. 2018.

[6] R. Sudharshan Kaarthik, K. S. Amritkumar, and P. Pillay, “Emulation of a permanent-magnet synchronous generator in real-time using power hardware-in-the-loop,” *IEEE Trans. Transport. Electrific.*, vol. 4, no. 2, pp. 474–482, Jun. 2018.
[7] Y. Srinivasa Rao and M. C. Chandorkar, “Real-time electrical load emulator using optimal feedback control technique,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 4, pp. 1217–1225, Apr. 2010.

[8] S. Lentijo, S. D’Arco, and A. Monti, “Comparing the dynamic performances of power Hardware-in-the-Loop interfaces,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 4, pp. 1195–1207, Apr. 2010.

[9] C. Nemec, O. Lehmann, M. Heinze, and J. Roth-Stiefler, “Optimal inductor setup for a power-hardware-in-the-loop machine emulator,” in *Proc. IEEE 10th Int. Conf. Power Electron. Drive Syst. (PEDS)*, Apr. 2013, pp. 364–369.

[10] F. Lehfuss, G. Lauss, P. Kotsamopoulos, N. Hatzigiorgi, P. Crolla, and A. Roscoe, “Comparison of multiple power amplification types for power Hardware-in-the-Loop applications,” in *Proc. Complex. Eng. (COMPENG)*, Jun. 2012, pp. 1–6.

[11] S. Grubic, B. Amlang, W. Schumacher, and A. Wenzel, “A high-performance electronic hardware-in-the-loop drive-load simulation using a linear inverter (LinVerte),” *IEEE Trans. Ind. Electron.*, vol. 57, no. 4, pp. 1208–1216, Apr. 2010.

[12] A. Schmitt, M. Gommeringer, C. Rollbuhler, P. Pomnitz, and M. Braun, “A novel modulation scheme for a modular multiphase multilevel converter in a power hardware-in-the-loop emulation system,” in *Proc. IECON 41st Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2015, pp. 1276–1281.

[13] C. Nemec and J. Roth-Stieflow, “Ripple current minimization of an interleaved-switched multi-phase PWM inverter for three-phase machine-emulation,” in *Proc. Eus. Conf. Power Electron. Appl.*, Sep. 2011, pp. 1–8.

[14] G. J. Capella, J. Pou, S. Ceballos, J. Zaragoza, and V. G. Agelidis, “Current-balancing technique for interleaved voltage source inverters with magnetically coupled legs connected in parallel,” *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1335–1344, Mar. 2015.

[15] K. S. Amritkumar, R. S. Kaarthik, and P. Pillay, “A versatile power-hardware-in-the-loop-based emulator for rapid testing of transportation electric drives,” *IEEE Trans. Transport. Electrific.*, vol. 4, no. 4, pp. 901–911, Dec. 2018.

[16] A. Schmitt, J. Richter, U. Jurkewitz, and M. Braun, “FPGA-based real-time simulation of nonlinear permanent magnet synchronous machines for power hardware-in-the-loop emulation systems,” in *Proc. IECON 40th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2014, pp. 3763–3769.

[17] W. Ren, M. Steurer, and T. L. Baldwin, “Improve the stability and the accuracy of power Hardware-in-the-Loop simulation by selecting appropriate interface algorithms,” *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1286–1294, Jul./Aug. 2008.

[18] L. Yang, J. Wang, Y. Ma, J. Wang, X. Zhang, L. M. Tolbert, F. F. Wang, and K. Tomovic, “Three-phase power converter-based real-time synchronous generator emulation,” *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1651–1665, Feb. 2017.

[19] D. Majstorovic, I. Celanovic, N. D. Teslic, N. Celanovic, and V. A. Katic, “Ultralow-latency Hardware-in-the-Loop platform for rapid validation of power electronics designs,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4708–4716, Oct. 2011.

[20] A. C. Oliveira, C. B. Jacobina, and A. M. N. Lima, “Improved dead-time compensation for sinusoidal PWM inverters operating at high switching frequencies,” *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2295–2304, Aug. 2007.

[21] A. G. Jack, D. J. Atkinson, and H. J. Slater, “Real-time emulation for power equipment development—Part 1: Real-time simulation,” *IEEE Pro. Electr. Power Appl.*, vol. 145, no. 2, pp. 92–97, Mar. 1998.

[22] H. J. Slater, D. J. Atkinson, and A. G. Jack, “Real-time emulation for power equipment development—Part 2: The virtual machine,” *IEEE Pro. Electr. Power Appl.*, vol. 145, no. 3, pp. 153–158, May 1998.

[23] G. Liu, D. Wang, Y. Jin, M. Wang, and P. Zhang, “Current-detection-Independent dead-time compensation method based on terminal voltage A/D conversion for PWM VSI,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 7689–7699, Oct. 2017.

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