Research and Design of Wireless Network Time Synchronization Module Based on IEEE1588 Protocol

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Abstract. Wireless network systems have many problems, such as low data transmission rates, limited coverage, limited measurement node capacity, and low time synchronization accuracy, especially the millisecond-level time synchronization accuracy can no longer meet the needs of the market. Therefore, it is urgent to find a more accurate time synchronization technology solution. At the same time, the accuracy of the time synchronization of the IEEE1588 protocol in a distributed wired network can reach the nanosecond level, so it is extremely important to introduce it into a wireless network to achieve more accurate time synchronization in the wireless network. This paper is the research and design of high-precision time synchronization module for wireless network based on IEEE1588 protocol. It mainly uses ARM + FPGA + WLAN structure to design time synchronization module. According to the actual test of the module, it can be known that the time synchronization accuracy that the wireless network time synchronization mode can achieve is as high as 150ns, which can fully meet the needs of the wireless market for time synchronization accuracy.

1. Introduction
With the continuous development of 5G and IOT technology, the technology of time synchronization has also been continuously developed. Nowadays, combining wireless networks and high precision time synchronization is particularly challenging. Wireless distributed measurement systems based on low-rate personal area network technologies has common problems: low data transmission rates, low time synchronization accuracy, and so on. In the distributed measurement process based on WLAN, although it can solve the problems such as low data transmission rate in distributed measurement based on personal area network technology, its synchronization accuracy is usually in the order of ms and its coverage is also limited. However, with the help of hardware timestamps, the accuracy of time synchronization can reach sub-microsecond levels. The IEEE1588 protocol was originally used for industrial control that required strict timing coordination. In order to comply with the rapid growth of the demand for high-precision time synchronization in communication networks, IEEE1588 is already applied to equipment, optical transmission equipment[1].

This article is the design of a high-precision wireless network time synchronization module based on the IEEE1588 protocol, which is implemented using a combination of software and hardware. The core module mainly includes three parts: WLAN, ARM, and FPGA. Through experimental tests, the time synchronization accuracy that this module can achieve is up to about 150ns, and the maximum fluctuation range of the slave clock and the master clock is 400ns, which can meet the market's requirements for time synchronization accuracy of wireless networks.
2. Basic principles of the IEEE1588 protocol

The principle of precise clock synchronization of IEEE1588 protocol proposed delayed response mechanism, which is shown in the following figure:

![IEEE1588 protocol delayed request response mechanism](image)

In the figure 1, the process of the delayed request response mechanism is as follows: First, the master clock sends a synchronization message sync to the slave clock, and records the time t1 at which the synchronization message is transmitted to the slave clock. At the same time, the slave clock will record the arrival time t2 of the message. After the synchronization message is sent, the master clock will then send a follow-up message Follow_up to the slave clock, which contains t1 information. After receiving the follow-up message from the clock, the slave clock will then send a delay request message Delay_req to the master clock, and record the departure time t3 of the message. When the master clock receives a Delay_req message, it records the time of arrival of the message t4. Finally, the master clock sends a delay request response message Delay_resp to the slave clock. Delay_resp contains the time t4 when the master clock receives Delay_req. After the above process, t1, t2, t3, and t4 information can be obtained from the clock[2].

Assume that the error between the slave clock and the master clock is offset, and the average network delay of IEEE1588 packets transmitted between the master and slave clocks is Delay. According to the synchronization process described above:

\[
offset = \frac{1}{2} [(t4 - t3) - (t2 - t1)] \quad (1)
\]

\[
delay = \frac{1}{2} [(t4 - t3) + (t2 - t1)] \quad (2)
\]

According to the above two formulas, the time offset between the master and slave clocks and the average delay delay can be obtained. The slave clock can adjust its own clock information through time deviation and average delay, so as to achieve high-precision synchronization of master and slave time.

3. Research and design of clock synchronization module for wireless network based on IEEE1588 protocol

3.1 Research of time synchronization module in wireless network

Because the time deviation and path delay in figure 1 are based on the ideal case. However, in the actual network measurement and control system, there will be many influencing factors, such as
timestamp accuracy, transmission link asymmetry, inherent network delay jitter, clock crystal drift. To achieve the high-precision clock synchronization, two factors that have a greater impact are the asymmetric transmission link and the master-slave clock crystal drift and jitter. In the calculation of offset and delay, it is assumed that the transmission link of the message in the network is symmetric, but the transmission on the actual network will pass through the switch and other equipment, which will cause the problem of unequal message transmission delay [3]. In this paper, because the clock crystal is not studied, the clock is still assumed to be standard. It mainly uses a combination of software and hardware to timestamp the network layer and the data link layer to reduce the path delay’s effect of time synchronization accuracy in the wireless network. At present, according to the implementation methods, they can be roughly divided into three methods: software method, hardware method, and software-hardware combination method. The advantage of software-hardware is to combine software and hardware synchronization, so as to achieve higher clock synchronization accuracy at a lower cost, which is usually applicable to large-scale wireless networks [4].

For the actual wireless network, the time synchronization module is set as the master and slave clock respectively. At this time, the working principle of the wireless network time synchronization module is as follows:

![Figure 2. Working principle of wireless network time synchronization module.](image)

As shown in figure 2, in a wireless network environment, because most WLAN modules on the market currently encapsulate the data link layer and the physical layer, the time stamp cannot be obtained at the MII interface between the physical layer and the data link layer. Because scheme C has many limitations in the wireless network, this scheme mainly uses the second scheme B. Scheme B is a combination of software and hardware for timestamping. It combines the hardware stamping of scheme C with the actual situation of the wireless network WLAN module. It is the best solution for the current wireless network environment. It can achieve time synchronization accuracy at the microsecond level, which is much higher than the software-only synchronization method of scheme A, which can meet the needs of high-precision time synchronization in the wireless network environment [5].

### 3.2 Design of time synchronization module in wireless network

This article is based on the combination of software and hardware to achieve high-precision time synchronization module design for wireless networks. The main structure is composed of WLAN chip, ARM chip, and FPGA chip. Among them, the ARM platform uses the embedded S5P6818 CPU of Samsung, which has the characteristics of rich peripheral interfaces and convenient driver development, which is suitable as a software development platform for this subject; The FPGA uses the AX4010 development board of ALINX Company, which has the characteristics of fast speed and
abundant logic resources, and is suitable for implementing LXI high-precision clock and high-speed data acquisition; The WLAN module adopts WM-G-MR-09 of Huanlong Electric. The WiFi chip supports the 802.11b/g wireless network mode. The packaged WLAN module can easily implement wireless access to the device and effectively shorten the project development time[6].

The overall structure of the hardware design of the wireless network time synchronization module designed in this paper is as follows:

![Figure 3. Hardware structure of wireless network time synchronization module.](image)

In the figure 3, the S5P6181 and WM-G-MR-09 module cooperate to implement wireless network access and message triggering functions, the control channel part and AX4010 complete data acquisition functions, and provide external interfaces such as USB interface, RS232 serial port; AX4010 module realizes data acquisition, including differential receiver circuit, serial-parallel conversion circuit, data recombination and recovery circuit. The main function is to collect the conditioned digital signal, provide conditions for storage and triggering, and the most important thing is to realize the synchronization message of S5P6181 platform to achieve the function of time stamping; The WM-G-MR-09 module realizes wireless access of the master and slave clocks, that is, the master clock sends synchronization messages to the slave clock and receives feedback messages from the slave clock through the wireless network. Finally, the sending and receiving of messages between the master clock and the slave clock of the wireless network is realized; Power module design is the key to the entire circuit design. High-quality power design can reduce system failures by more than half; The clock module is the heartbeat of the ARM processor. A good clock will make the system circuit work more stable; Reset modules generally include hardware reset, watchdog reset, software reset and other types; Other modules such as: storage module, temperature module[7].

Since the timestamp obtained at a location closer to the bottom layer is more accurate, for the existing wireless chip, the timestamp obtained at the MAC layer is the time closest to the real time of sending or receiving a message under the existing hardware conditions. In order to obtain the time stamp at the MAC layer, the WM-G-MR-09 module and the SDIO interface of the ARM control platform S5P6818 need to be connected to the ordinary I/O port of the FPGA AX4010. AX4010 uses the corresponding logic circuit to record the current time stamp of the high-precision clock module when the relevant message is detected[8].

In the actual network environment, there are many factors that affect the accuracy of the master and slave clocks, such as the clock's own crystal jitter, external ambient temperature, and path delay. In order to maintain master-slave clock synchronization at all times, the master and slave clocks periodically send and receive messages, so that a relatively high-precision time synchronization can be achieved in a wireless network environment[9].

4. Test and analysis of wireless network time synchronization module

The wireless network time synchronization module can be used as a slave clock or master clock in a
single network, and it can also be used as a boundary clock or gateway clock in two networks. When used as a master clock, the time synchronization module will use the network to provide time to multiple other devices; when used as a slave clock, the time synchronization module will rely on the remote master clock to recover time information. In this article, one time synchronization module is set as the master clock and the other is set as the slave clock to test the wireless network time synchronization module. The test scheme is shown in the figure below[10]:

![Test process of time synchronization module.](image)

In the figure 4, the wireless network time synchronization module is set as the master and slave clocks, and the working mode is set to the default, that is, the synchronization message sync is sent once every second and the delay request message delay_req once every two seconds. Among them, S5P6181 works with WM-G-MR-09 module to realize wireless network access and message triggering functions; The main function of the AX4010 module is to achieve time stamping of the synchronous messages output by the S5P6181 platform; WM-G-MR-09 module realizes the wireless access of the master and slave clocks, in order to realize the sending and receiving of wireless network synchronization messages; The computer is only used to detect messages, not participate in clock communication, by using WIRESHARK software, capture all communication messages of the master and slave clock.

The test results in the default working mode of the wireless network time synchronization module and the afterglow diagrams during time synchronization are shown in the following figures:

![Test results of wireless network time synchronization module.](image)

![Afterglow diagram of wireless network time synchronization module.](image)
As shown in figure 5 and 6, the yellow curve represents the clock signal of the master clock, and the blue curve represents the clock signal of the slave clock. It can be seen from Figure 5 that when the master and slave clocks use the default mode, the synchronization accuracy of the master and slave clocks can reach 150ns and the afterglow diagram shows that the fluctuation of the slave clock is about 400ns.

5. Conclusion
In this paper, the design of the wireless network time synchronization module based on the 1588 protocol proposed uses the structure design of “S5P6181 + AX4010 + WM-G-MR09”, which achieves the time synchronization of wireless network through a combination of software and hardware. It can be obtained through experimental tests that the accuracy of the time synchronization achieved by the wireless network time synchronization module designed in this paper is about 150ns, and the maximum fluctuation range of the slave clock and the master clock is 400ns. The accuracy of the wireless network time synchronization that can be achieved is already very high and can meet the requirements of the market for the accuracy of wireless network time synchronization. This article mainly studies the effect of path delay on time synchronization accuracy, but does not involve the stability of clock crystals. Next, the influence of clock crystal drift and jitter on time synchronization is included in the research scope, and optimization research is mainly carried out from the aspect of algorithms.

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