Radiation Induced SET Impact on DG-FINFET based LC-VCO Design

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Abstract

In wireless communication system, the supply voltage should be as low as possible to increase operation time of the system. This shows how importance the low-power circuits are in this field. Recently, there has been considerable interest in the use of Fin type Field Effect Transistor (FinFET) technology to implement RF components such as low-noise amplifiers (LNAs), mixers, and voltage-controlled oscillators (VCOs). VCOs are critical building blocks in modern wireless communication system which is mainly used in Phase Locked Loop. This work describes designing and simulation of Double Gate (DG) FinFET based Inductor (L) and Capacitor (C) tank VCO and the radiation effect of single event transient (SET) on the topology. The LC VCO topology is implemented with 30 nm DG-FinFET technology with 1V as DC power supply voltage which oscillates at 32.61 GHz frequency, results the VCO draws 64.97 µA current and an average power consumption of 64.97 µW. The measured phase noise of the topology is -120.54dBc/Hz at 1 GHz offset frequency and Figure of Merit (FOM) is - 162.68 dBc/Hz at 1 GHz offset frequency.

Keywords: DG-FinFET, Figure of Merit, Low Power, Phase noise, Single Event Transient (SET), Voltage Control Oscillator

1. Introduction

The rapid growth in wireless communication has led to an increased demand for wireless gadgets that are low cost, power, and compact in size¹. Improved CMOS technology and the CMOS process offer a higher density of integration and low power consumption. This helps its use in wireless communication² with the development of the System on Chip (SoC) approach that enables integration of whole CMOS RF circuits on a single chip. To increase system operation time the supply voltage should be as minimal as possible in wireless communication domain³. This shows how importance low-power circuits are. Recently, there has been considerable interest in the use of FinFET technology to implement RF components like low-noise amplifiers (LNAs), mixers, and voltage-controlled oscillators (VCOs). VCOs are the important building blocks in modern wireless communication system⁴. ASCMOS technology is scaling down drastically which results in reliability issues for the next generation devices and circuits.

Technology trends like downscaling transistor size, using of new material, and SoC approach continues the sensitivity of the system to Single Event Effects (SEE). These SEEs alter the normal behavior of the semiconductor based circuits which are induced by a single high energy ionizing particle⁵. These effects result in either in data corruption or transient disturbance in the circuits. SEE are of destructive and non-destructive effects. Single Event Upset (SEU), Single Event Transient (SET), and Single Event Functional Interrupt (SEFI) come under these effects. SET is the transient response which is due to the energetic particle strike and refers to a current or voltage pulses passing through the circuit.

This paper describes Double Gate Fin type Field Effect Transistor (DG-FinFET) based Inductor (L) and Capacitor (C) tank VCO and the impact of radiation-
induced SET phenomenon. The LC-VCO uses P and N-channel DG-FinFETs in the cross-connected pair. This is a so-called current reused LC-VCO. Giga Hertz (GHz) frequency and low power (µW) DG-FinFET LC-VCO design approach is considered in this work. VCO design involves trade-off among the parameters like phase noise, power, and tuning range. Figure 1 shows a trade-off triangle indicating good phase noise, low power consumption, and less tuning range and vice-versa.

The remaining part of this paper is organized as follows:- Section II describes Theory of DG-FinFET and VCO. Section III describes operation of DG-FinFET LC-VCO circuit topology and the impact of SET radiation on the LC-VCO Topology. Section IV gives simulation results.
results of the DG-FinFET LC-VCO circuit topology. Section V gives conclusion and future direction.

2. Theory of DG-FinFET and VCO

2.1 DG-FinFET

As CMOS is scaling down significantly gate controllability over the channel is no longer exists, which leads to Short Channel Effects (SCEs). In order to achieve better gate controllability over the channel, FinFETs are introduced.

Figure 2 and figure 3 shows the 3D view of N-channel DG-FinFET and P-channel DG-FinFET structure respectively designed using Synopsys Technology Computer Aided Design (TCAD) simulator tool. Table I gives the various device dimensions and doping concentration values of the device. An \( I_D - V_{GS} \) characteristic of N-channel DG-FinFET device is shown in figure 4.

2.2 Voltage Control Oscillator

By definition Oscillator is the one which exhibits periodically time varying signal. VCO is an oscillator which provides voltage signal at a specific frequency when supplied with Direct Current (DC) power. The frequency of VCO can be varied by the tuning the voltage applied to its tuning part. In general, any oscillator can be modeled either as a single two port (feedback oscillator model) circuit or as two one port circuits connected together (negative resistance model). For feedback oscillator model it has to satisfy Barkhausen criteria, which are necessary but not sufficient. In negative resistance model, the equivalent parallel resistance (real part (RP) of total impedance) of the resonator must be exactly balanced by negative resistance produced by active circuit at the oscillation frequency. Thus the condition for oscillation to be sustained can be expressed by

\[
\left(\text{RP}\{Z_T(S)\} + \text{RP}\{Z_A(S)\}\right)\big|S = j\omega_0 = 0
\]

The oscillation frequency is given as

\[
\omega_0 = \frac{1}{\sqrt{LC}}
\]

Among different topologies for compensation of losses in tank circuit, cross coupled differential -Gm LC-VCO topology is the common choice for RF Integrated Circuit (IC) which gives better spectral purity. Figure 5 shows typical cross couple differential -Gm LC-VCO. The losses in tank circuit can be compensated by the negative resistance of two cross coupled NMOS pair and PMOS pair devices. The frequency of oscillation can be obtained by applying DC power supply to its tuning

| Table 1. Device Dimensions |
|---------------------------|
| Parameter | Abbreviation | Value |
| Lg         | Gate Length  | 30 nm |
| Tox        | Gate oxide thickness | 1 nm |
| W          | Fin Width    | 4 nm  |
| H          | Fin Height   | 4 nm  |
| Na         | Channel Doping Concentration | 1x10^{16} \text{ cm}^{-3} (N-DG-FinFET) |
|           |             | 1x10^{16} \text{ cm}^{-3} (P-DG-FinFET) |
| Ns, Nd     | Source and Drain Doping Concentration | 1x10^{20} \text{ cm}^{-3} (N-DG-FinFET) |
|           |             | 1x10^{20} \text{ cm}^{-3} (P-DG-FinFET) |
| SL         | Source Length | 15 nm |
| SH         | Source Height | 15 nm |
| qf         | Work Function | 4.3 eV (N-DG-FinFET) |
|           |             | 4.9 eV (P-DG-FinFET) |

Figure 4. \( I_D \) vs. \( V_{GS} \) of N-channel DG-FinFET.
part. The frequency can be varied by varying the tuning voltage. The enhanced version of -Gm LC-VCO topology has been discussed in the next section.

3. DG-FinFET LC-VCO Design

3.1 DG-FinFET LC-VCO Topology

The current reuse\(^{11}\) differential DG-FinFET LC-VCO topology is shown in the figure 6 and its 3D view is shown in figure 7. The topology consists of cross coupled DG N-channel FinFET (N1) as driver and DG P-channel FinFET (P1) device as load, where both contribute negative resistance to compensate the loss due to tank circuit. The total negative resistance of the cross coupled devices is defined as

\[
R = \frac{-2}{G_{mn} + G_{mp}}
\]

Where \(G_{mn}\) and \(G_{mp}\) are trans conductance of N1 and P1 respectively. The tank circuit comprises on chip inductor and parallel combination of DG P-channel FinFET varactors in accumulation mode.

The N1 and P1 stack as switch model shown in figure 6. Now apply DC power supply voltage source terminal of P1 and the tuning voltage to varactor device. As soon as the tuning voltage is applied the losses of the tank circuit are compensated and the topology starts to oscillate. By varying the tuning voltage we can get different frequency of oscillations. During the positive half cycle of the oscillator output, both P1 and N1 are closed (figure 6a). In this period, current flow through the tank from a DC supply to ground that charges the tank. During the next half cycle, the switches are opened (figure 6b) and tank discharges in this period. Surprisingly, this topology draws the current from DC supply only during positive half cycle of its oscillation, during negative half cycle it reuses the tank discharge current and continues the output signal. This technique reduces the power consumption of the oscillator to nearly half compared to conventional oscillator.

The current in the tank circuit is controlled by P1 and N1 which influences the tank performance and amplitude of output voltage. The topology operates with 1V DC power supply.

The phase noise\(^6\) of VCO denoted as \(L(f_m)\) called “script L of \(f_m\)” and FOM\(^{12}\) can be expressed as follows:

\[
L(f_m) = F(KT/P_s)(f_o/\sqrt{Q}f_m^2)
\]

\[
FOM = L(f_m) - 20\log(f_o/f_m) + 10\log(P_{DC}/1mw)
\]

Where \(f_o\) is oscillation frequency, \(f_m\) is frequency offset, Q is quality factor of resonator LC tank, \(P_s\) is signal power of oscillator, \(K\) is Boltzmann constant, \(T\) is absolute temperature, \(P_{DC}\) is VCO power consumption, \(F\) is noise factor for active device in saturation mode.

3.2 Set Radiation On The LC-VCO Topology

SET were first presented in bipolar linear circuits in 1993\(^{13}\). SET may be caused due to the generation of charge which is due to the single particle (either proton or heavy ion) passing through the sensitive node of the circuit\(^{14}\). SETs in linear devices are different from other SEE like SEU in memory. Each SET has its unique characteristics like amplitude, waveform, duration, polarity, etc. The above mentioned characteristics depend on device technology, particle energy, device supply voltage, particle impact location, and output load.

The SET is imitated by a double exponential current source which is focused on the sensitive node of the topology, i.e., the drain terminal of the cross coupled FinFET pair. The double exponential current pulse is hav-
ing a rise time of 2ns and a fall time of 2.2 ns and the peak amplitude of 2 mA has been adjusted to retrieve the experimental behavior of the oscillator. The effect of this results in distorted complementary output of the VCO.

4. Simulation Results

The DG-FinFET with 30nm technology is designed and simulated. The DG-FinFET draws an average current of 64.97μA with 1V DC supply results an average low power of 64.97μW. At the maximum voltage of 1V the oscillator takes 1.407 ns time to reach the steady state oscillation. The phase noise -120.54dBc/Hz at 1GHz offset frequency and FOM is -162.68dBc/Hz at 1GHz offset frequency. The complementary output of the LC-VCO is shown as in figure 8. Figure 9 shows the frequency variation with respect to tuning voltage.

The tuning voltage vs. Average power dissipation curves before and after radiation strike with reference to

Figure 6a. Current reuse DG-FinFET LC-VCO with P-channel DG-FinFET varactor tank.

Figure 6b. Operation of VCO design a) Positive half cycle, and b) Negative half cycle of output.

Figure 7. 3-D view of DG-FinFET LC-VCO.
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Figure 8. Complementary output waveform of DG-FinFET LC-VCO topology.

Figure 9. Frequency vs. Tuning Voltage curve.

Figure 10. Variation of average power dissipation before radiation.

Figure 11. Variation of average power dissipation after radiation.
5. Conclusion and Future Scope

The DG-FinFET LC-VCO is simulated using 30 nm technology node and the characteristics are studied. In this work, the DG-FinFET LC-VCO topology operates at GHz frequency range with low power consumption and the impact of SET radiation on the topology is presented. This work can be extended to the design of radiation hardened LC-VCO topology which does not alter the steady state response of the circuit under SET radiation environment.

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7. References

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