THD analysis for symmetrical five level and seven level cascaded multilevel inverter

Fahimah Kaja Mohideen¹, Nor Ashbahani Mohamad Kajaan¹², Zainuddin Mat Isa¹², Norkharziana Mohd Nayan¹², Mohd Hafiz Arshad¹²³ and Saidatul Shema Saad¹³

¹School of Electrical Systems Engineering, Universiti Malaysia Perlis, Pauh Putra Campus, 02600, Arau, Perlis, Malaysia
²Centre of Excellence for Renewable Energy (CERE), School of Electrical Systems Engineering, Universiti Malaysia Perlis, Pauh Putra Campus, 02600, Arau, Perlis, Malaysia
³Electrical Technology Faculty, Universiti Malaysia Perlis, Pauh Putra Campus, 02600, Arau, Perlis, Malaysia

Email: ashbahani@unimap.edu.my

Abstract. Total Harmonic Distortion (THD) is one of the problems in the multilevel inverter. This paper discussed a brief review of THD in different cascaded H-bridge multilevel inverter topologies of five levels and seven levels at the output waveforms. The five levels inverter contains eight switches while seven levels inverter used twelve switches. Each single H-bridge inverter circuit is fed by equally independent DC source for both inverters. The inverter uses MOSFET as the switching point and acts as the controller for a fundamental switching operation. The switching value has been set at the gating block to control the operation of the MOSFET switching. Several waveforms and simulation findings are provided to validate the quality of the proposed topology.

1. Introduction
Multilevel inverters are an electronically controlled device capable of generating desired alternating voltage at the output by using a lower DC voltages as an input. Generally, two-level inverter is used to generate an AC voltage from a DC voltage. However, it tends to have higher losses on the switching and the harmonic voltage and hence resulting the harmonic current to be exist in the loop and the losses are also generated. Multilevel inverter is taking certain advancement in order to overcome the advantages of the existing conventional inverter. By using multilevel inverter, the output rates can be raised to more than two in order to generate a pure sinusoidal waveforms of different levels at the output voltages as shown in Figure 1. It is increasingly attentive, known for its high voltage operating capabilities, relatively small losses in switching, highly efficient and low in Electromagnetic Interference (EMI) [1]. The concept of multilevel inverter have become increasingly popular in power applications these days, as multilevel inverters with lower harmonic distortion and reduced electromagnetic interference are capable to suit the growing demand for rated power and linked energy performance [2]. There are few types of multilevel inverter that has been classified into several group. There are three types of multilevel inverter that is widely used and recognised [3], which are diode clamped (neutral clamp) type, capacitor clamped type (replacing the diode with the capacitor, also known as flying capacitors type) and cascaded H-bridge multilevel inverter.
The role of this topology has received increased attention across a number of discipline in recent years as their ability to generate output voltage with less THD, as well as the harmonics in the output can be suppressed and percentage of losses can be decreased. This inverter topology is developed to produce an AC source that is almost similar like a pure power generation source to use in AC load. It is possible to obtain a smooth waveform by increasing the inverter circuit levels. The more the levels, the smoother the output voltage waveform will be. In addition, this inverter consists of combinations of single phase H-bridge inverter circuit and it is connected in series which are fed by independent DC source become cascaded single phase H-bridge inverter. Figure 2 shows the type of waveform and only the modified and sine wave has produced by inverter and suitable to use by AC load. A modified sine wave has been generated by inverter is similar with a square wave but assemble at zero for moment before rises or falls to look related more in shape to a sine wave and tries to match such as sine wave as shown in Figure 2.

Since the inverter is used to supply a load involving an AC with a DC voltage source, understanding the quality of the AC output voltage or current is very useful and this can be impressed in terms of THD. A high voltage output should be introduced to achieve low THD but, as the voltage level rises, the quantity of switches increases which lead to high voltage sources, cost, volume, control complexities and efficiency [6]. The need for such an inverter is primarily to be used in industries and in real applications for the quality performance of the power system. There is no need for transformers
and filters while these inverters are being used. Installation costs and harmonics are therefore decreased [7].

2. The Concept of Cascaded H-Bridge Multilevel Inverter

2.1. Single Phase H-Bridge Inverter

Basically, the concept of H-Bridge inverter or also known as Full-Bridge, which is the inverter circuit which consists of four main switches and the arrangements in H shape such as shown in Figure 3. Throughout this application, by closing and opening the switches in an adequate sequence, an AC output is extracted from a dc input. The output voltage level for single phase H-bridge inverter consists of positive (+V), negative (-V) and zero (0) values. The positive value has been produced when the switching for switch 1 (S1) and switch 4 (S4) closes at same time. Then, the negative value will be produced when switching for switch 2 (S2) and switch 3 (S3) were closed at the same time. The zero level can be provided by two conditions such as switch for S1 and S2 are closed (on) and switch for S3 and S4 are open (off) at the same time or vice versa [8]. Periodic load voltage switching between + Vdc and -Vdc results in a square wave voltage throughout the load. While this alternating output is non-sinusoidal, for some applications it may be an appropriate AC waveform.

![Figure 3. A typical 3 level H-Bridge Inverter Arrangement [8].](image)

2.2. Cascaded Inverter Configuration

The output voltage level is generated in cascaded inverter configuration by combining each of the single phase different H-bridges configuration that connected in series to develop a multilevel waveform. The multilevel waveform is the sum of inverter output after single phase H-bridge inverter has cascaded with the other various single phase H-bridge inverters with separated DC source. The topology advocated a concept of generating an AC voltage waveform that used a separated DC input that bound in each H-bridge inverter. These DC voltages can be exactly the same or dissimilar. The performance of each H-bridge can be non-identical three levels, resulting in an almost sinusoidal waveform, even without any filtering [9]. The final AC output waveform is produced by cascading the individual H-bridge output waveform. Based on the number of DC source in a cascaded H-bridge inverter, the multilevel waveform output voltage level can define by equation (1), where s shows the number of individual DC source that connected to each H-bridge inverter.

\[ m = 2s + 1 \] (1)

If the total of separated DC source is equal to two, then the multilevel waveform output that will be produced by inverter is five level. Figure 4 shows a single phase configuration of an m-level cascaded
inverter. The results of the eleven level cascaded H-bridge inverter can be seen in Figure 5. Each stage in the inverter level will produce different output waveforms by using appropriate switching control methods. The final output voltage from point a to n are as in equation (2).

\[ V_{an} = V_{a1} + V_{a2} + V_{a3} + V_{a4} + V_{a5} \]  

(2)

3. Simulation of a Single Phase Cascaded H-Bridge Inverter Circuit

The basic principle of H-bridge switching can be applied to other circuits which can generate additional amounts of output voltage. The H-Bridge topology has the advantage of its reduced number of the device [9]. Such voltages of multilevel output are more likely sine in quality and thus reduce harmonic content. In symmetrical cascaded multilevel inverter, the power sources in each H-bridge cell are in the same value. The inverter output waveform obtained by switching the power semiconductor devices, integrating full bridge inverters connected in cascade. Thus, the output voltage is the sum of the voltage of each full bridge module. This type of inverter avoids the use of interlocking diodes, capacitors voltage balancing float also a low THD can be obtained by controlling the gate trigger of the different voltage levels [12].

3.1. Five level Cascaded H-Bridge Multilevel Inverter

The five level cascaded H-bridge inverter circuit consists of two single H-bridge inverter circuits as shown in Figure 6. Each H-bridge circuits been supply with DC voltage as input giving a total of two inputs (V1 and V2). Each single H-bridge consist of four MOSFET, total of eight switches for all stage cell (S1, S2, S3, S4, S5, S6, S7 and S8) in arrangement of H shape and each MOSFET connected with one gating block for switching MOSFET. The cascaded H-bridge inverter circuit has 90V\textsubscript{DC} supply into each single H-bridge inverter circuit. Every MOSFET assigned with individual gating parameters for switching purposes to produce suitable waveform pattern. To obtain the desired level in output voltage
for five level inverter, switches are operated according to Table 1. It is apparent from the Table 1 that the ‘ON’ and ‘OFF’ state for the switches are represented by both 0 and 1. In each output voltage line for this inverter, four MOSFET need to be turn ‘ON’ while remaining four will remains ‘OFF’.

![Figure 6. Configuration of an m-level single phase cascaded H-bridge Inverter.](image)

|        | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | Voltage level |
|--------|----|----|----|----|----|----|----|----|---------------|
| 0      | 1  | 1  | 0  | 0  | 0  | 1  | 1  | 0  | + V<sub>DC</sub> |
| 1      | 1  | 1  | 0  | 0  | 0  | 1  | 1  | 0  | + 2V<sub>DC</sub> |
| 1      | 1  | 1  | 0  | 0  | 1  | 1  | 0  | 0  | 0V            |
| 1      | 1  | 1  | 0  | 0  | 1  | 0  | 0  | 1  | - 2V<sub>DC</sub> |
| 1      | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 1  | - V<sub>DC</sub> |

### 3.2. Seven level Cascaded H-Bridge Multilevel Inverter

In seven level cascaded H-bridge inverter, three single H-bridge inverter circuits as shown in Figure 7 is required to generate the desired output waveform. The circuits are fed by the same magnitude of independent DC voltage source at each H-bridge (V<sub>1</sub>, V<sub>2</sub> and V<sub>3</sub>) and also consists of twelve MOSFET (S<sub>1</sub>, S<sub>2</sub>, S<sub>3</sub>, S<sub>4</sub>, S<sub>5</sub>, S<sub>6</sub>, S<sub>7</sub>, S<sub>8</sub>, S<sub>9</sub>, S<sub>10</sub>, S<sub>11</sub> and S<sub>12</sub>) in H shape arrangement. DC input voltage supply for each H-bridge cell is 60V. Therefore, the gating block will produce pattern of switch as in waveform of the switch for power MOSFET and each gating block was defined with different gating pattern of a switch. The switching operation to obtained the output waveform for the seven level multilevel inverter are given in the Table 2. In Table 2, 1 and 0 are respectively indicates the ‘ON’ and ‘OFF’ state of the switches. It can be observed from state changes in Table 2, six switches will conduct at a time to generate the required level in each output voltage line.
Figure 7. Configuration of an m-level single phase cascaded H-bridge Inverter.

Table 2. Output voltage levels for seven level of multilevel inverter.

| S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 | S11 | S12 | Voltage level |
|----|----|----|----|----|----|----|----|----|-----|-----|-----|---------------|
| 1  | 0  | 0  | 1  | 1  | 0  | 0  | 1  | 1  | 0   | 0   | 1   | +3V<sub>DC</sub> |
| 1  | 0  | 0  | 1  | 1  | 0  | 0  | 1  | 1  | 0   | 0   | 1   | +2V<sub>DC</sub> |
| 1  | 0  | 0  | 1  | 0  | 0  | 1  | 1  | 0  | 0   | 0   | 1   | +V<sub>DC</sub>  |
| 0  | 0  | 1  | 1  | 0  | 0  | 1  | 1  | 0  | 0   | 1   | 1   | 0V           |
| 0  | 1  | 1  | 0  | 0  | 0  | 1  | 1  | 0  | 0   | 1   | 1   | -V<sub>DC</sub> |
| 0  | 1  | 1  | 0  | 0  | 1  | 1  | 0  | 0  | 0   | 0   | 1   | -2V<sub>DC</sub>|
| 0  | 1  | 1  | 0  | 0  | 1  | 1  | 0  | 0  | 0   | 1   | 0   | -3V<sub>DC</sub>|

4. Analysis of the Output Voltage and THD for Single Phase Cascaded H-bridge Inverter Circuit

In order to examine the ability of both five level and seven level cascaded H-bridge inverter to generate all possible positive and negative level symmetrically in output voltage waveform, both been set with different value of switching angle. For simulation purposes, each value of DC voltage sources is 60V and frequency of output voltage are assumed to be 50Hz.

4.1. Output Voltage for Five level and Seven Level Multilevel Inverter

Output phase voltage for five level and seven level inverter circuit is shown in Figure 8 and Figure 9 and it is confirmed that both inverters could generate all desired positive and negative levels. The maximum output voltage obtained from the circuit simulation for five and seven level inverter is +180V while minimum value shows -180V, as can be seen from Figure 8 and Figure 9. The waveform of the output voltage can be considered by configuring the value of the input DC voltage. The
configuration of the voltage can determine the level of the waveform. The level of waveform produced by the H-bridge inverter circuit is five level waveform.

Figure 8. Output voltage waveform of five level H-bridge inverter circuits.

Figure 9. Output voltage waveform of seven level H-bridge inverter circuits.

4.2. THD in Five level and Seven Level Multilevel Inverter

Since it is the purpose of the inverter to use a DC voltage source to supply load required an AC, the quality of the AC output voltage or current should be described in terms of THD. The simulation results for THDV and THDI are as shown in Figure 10 and Figure 11 for both multilevel configurations. The THD of the output voltage in seven level is lower than five level by approximately 7%. Increasing number of level for the inverter, on the other side results in better THD values but increased the power switching losses [13]. The harmonic voltage value of each odd harmonic has been computed and tabulated in the Table 3 and Table 4 for each set of the inverters after the output voltage spectrum were acquired. For each set of the inverters, the n\(^{th}\) value of harmonic currents of each odd harmonic had also been determined and computed into the tables. For these harmonics, harmonic currents are determined by the load and amplitude of the voltage. As the n\(^{th}\) number of harmonics grows, the number of components in the harmonic voltage declines while the value of the respected impedance are increased, resulting in low currents for higher order of harmonic components.
Hence, only the beginning harmonic conditions in array are the significant concern. Realize why the current terms are relatively small for all but the first few frequencies.

**Figure 10.** THD percentage for H-bridge inverter circuits at five level.

**Figure 11.** THD percentage for H-bridge inverter circuits at seven level.

**Table 3.** Amplitudes of $n^{th}$ harmonic voltages and currents of a five levels multilevel inverter.

| n  | F$_n$ (Hz) | V$_n$ (V) | I$_n$ (A) |
|----|------------|-----------|-----------|
| 1  | 50         | 130.91    | 0.1309    |
| 3  | 150        | 0.26      | 0.0026    |
| 5  | 250        | 19.13     | 0.0191    |
| 7  | 350        | 10.50     | 0.0105    |
| 9  | 450        | 1.53      | 0.0015    |
Table 4. Amplitudes of \( n \)th harmonic voltages and currents of a seven levels multilevel inverter.

| \( n \) | \( F_n \) (Hz) | \( V_n \) (V) | \( I_n \) (A) |
|-------|---------------|-------------|-------------|
| 1     | 50            | 159.96      | 0.1600      |
| 3     | 150           | 9.96        | 0.0010      |
| 5     | 250           | 9.10        | 0.0091      |
| 7     | 350           | 4.44        | 0.0044      |
| 9     | 450           | 3.23        | 0.0032      |

5. Conclusion

The Cascade type of H-Bridge multilevel inverter proposed in the design used a symmetrical arrangement for the switching circuits with different identical DC sources. Through rising the phase levels of an output voltage, low harmonic distortions are achieved, generating a staircase waveform [12]. H-Bridge is designed to deliver five and seven levels of output for a single phase inverter. As a number of levels in the configuration increases, percentage of the THD will be decreases with significant percentage difference. Higher voltage output should be implemented to achieve low THD, but as the voltage level rises, the amount of switches will be increased, resulting in a high amount of sources of voltage, costing, volume, difficult to control and low effectiveness [14]. Advanced structure levels can be certainly prefer, providing good power quality with less THD [15].

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