Reliability characteristics of metal/ferroelectric-HfO$_2$/IGZO/metal capacitor for non-volatile memory application

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A metal/ferroelectric (FE)-HfO$_2$/IGZO/metal capacitor was fabricated and investigated for 3D high-density memory application. The sharp interface obtained without atomic interdiffusion. The capacitor shows ferroelectricity with a IGZO capping layer. The endurance and retention measurement show that the capacitor has up to 10$^8$ program/erase endurance cycles and a 10 year retention, respectively. The capacitor does not show the wake-up effect, which is beneficial for circuit design and manufacturing. The asymmetric imprint effect is attributed to the different band modulation in the accumulation and depletion states of IGZO.

Recently, the Internet of Things and artificial intelligence have been in need of a large memory capacity to store and analyze a large amount of data. Due to the constraint of power supply, high-density and low-power non-volatile memories are needed.

Among various non-volatile memories, the ferroelectric field effect transistor (FeFET) is a promising candidate for high-density, low-power application.\(^{(1-6)}\) Due to its field-driven operation, FeFET has advantages such as non-destructive readout, high program/erase speed, and low power consumption. Since ferroelectricity was reported in doped HfO$_2$,\(^{(7)}\) HfO$_2$-based FeFET has attracted more attention because of its high scalability and high CMOS compatibility. Toward even higher density, a 3D vertical structure has been proposed.\(^{(8-12)}\) A 3D vertical stacked FE-HfO$_2$ structure has been recently estimated,\(^{(13)}\) and a 3D vertical NAND type FeFET and its memory operation have been demonstrated.\(^{(14)}\) Poly-Si was used as a material for the vertical structure. However, there are several challenges with poly-Si channel such as high thermal budget, low mobility of the very thin poly-Si channel, and an interfacial layer with a low dielectric constant between HfO$_2$ and poly-Si. To overcome these challenges, a FeFET with an oxide semiconductor channel has been proposed.\(^{(15-17)}\) Due to its high mobility with very thin body,\(^{(18-23)}\) IGZO is suitable for fast access speed. The IGZO FeFET also benefits from a nearly-zero interfacial layer between the IGZO channel and gate oxide, and thus it has less voltage loss. However, the reliability characteristics of metal/FE-HfO$_2$/IGZO has not been fully investigated, yet.

In this paper, we fabricate and characterize the ferroelectric property of FE-HfO$_2$ with a IGZO cap. Then, we investigate the impact of the IGZO cap on the reliability of the fabricated capacitor regarding endurance and retention characteristics. Lastly, an imprint effect on the capacitor is studied.

We fabricated FE-HfO$_2$ capacitors on an N$^+$ Si substrate. Figure 1(a) shows the sectional and plane view of fabricated capacitor and the process flow. Thirty nm TiN is deposited on RCA-cleaned N$^+$ Si substrate by RF sputtering. 15 nm 50% Zr-doped HfO$_2$ (HZO) is deposited by atomic layer deposition (ALD) at 250 °C. Eight nm IGZO is deposited by RF sputtering and patterned by diluted hydrochloric acid. RTA is done at 500 °C in N$_2$/O$_2$ (O$_2$:3%) ambience for 10 s. Ten nm Ti and 100 nm Al are deposited by EB evaporation and patterned by lift-off. The top electrode size is smaller than IGZO mesa size, because of the offset in lithography for top Ti/Al electrode as shown in Fig. 1(a). The polarization charge is formed after annealing.

The coercive field is about 1 MV cm$^{-1}$ which is typical for HZO capacitors. As the sweep voltage increases, the P–V curve becomes saturated at a high sweep voltage and the P$_r$ increases. Figure 2(b) shows the transient current–V curves of the fabricated capacitor. The polarization switching current become larger as the P–V curve becomes saturated due to the sweep voltage increasing. A leakage current is observed in the 5 V I–V curve which explains the reason the 5 V P–V curve is not completely closed in Fig. 3(a). Note that IGZO is in the accumulation state under positive bias voltage (program) and in the depletion state under negative bias voltage (erase). This difference is seen in the C–V curve of the positive and negative polarization states as shown in Fig. 2(c). In the positive polarization state, the capacitance is large with the accumulation capacitance of the IGZO layer in series. In the negative polarization state, the capacitance is small with the depletion capacitance of the IGZO layer in series.

Next, we characterize the ferroelectricity of the fabricated TiN/HZO/IGZO/Ti capacitor. A 1 kHz triangular voltage waveform is used to measure the ferroelectricity of the fabricated capacitor. A force voltage is applied on the bottom TiN electrode and the ground voltage is applied on the top Ti/Al electrode as shown in Fig. 1(a). The polarization charge is measured with different sweep voltages as shown in Fig. 2(a). Remanant polarization (2P$_r$) are from 19 μC cm$^{-2}$ to 30 μC cm$^{-2}$ in the sweep voltage range from 3 V to 5 V as shown in the inset of Fig. 2(a). The coercive field is about 1 MV cm$^{-1}$ which is typical for HZO capacitors. As the sweep voltage increases, the P–V curve becomes saturated at a high sweep voltage and the P$_r$ increases. Figure 2(b) shows the transient current–V curves of the fabricated capacitor. The polarization switching current become larger as the P–V curve becomes saturated due to the sweep voltage increasing. A leakage current is observed in the 5 V I–V curve which explains the reason the 5 V P–V curve is not completely closed in Fig. 3(a). Note that IGZO is in the accumulation state under positive bias voltage (program) and in the depletion state under negative bias voltage (erase). This difference is seen in the C–V curve of the positive and negative polarization states as shown in Fig. 2(c). In the positive polarization state, the capacitance is large with the accumulation capacitance of the IGZO layer in series. In the negative polarization state, the capacitance is small with the depletion capacitance of the IGZO layer in series.

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program/erase cycles. The inset of Fig. 3(a) shows the changes of P–V curves along program/erase cycles. Different from the metal/HZO/Si structure capacitor, the metal/HZO/IGZO/metal capacitor does not show the wake-up effect, which is beneficial for circuit design and manufacturing. This indicates that, unlike the metal/HZO/Si capacitor, amorphous IGZO facilitates preferentially forming of the ferroelectric orthorhombic phase and no significant charge redistribution occurs during cycling. In the case of the metal/HZO/Si capacitor, oxygen vacancies near the interface between the electrode and HZO becomes the charge trapping site. However, the HZO/Si interface is more critical for endurance properties than the metal/HZO interface. This is because the capacitance mismatch of interfacial layer (IL) with a low dielectric constant and FE-HfO2, a large voltage is applied on the IL, which eventually results in the breakdown of the IL. During cycling, the electric field is redistributed, the increased charge trapping pins domain switching, and then fatigue occurs. Further charge trapping and defect generation cause breakdown. In the case of the metal/HZO/IGZO/metal capacitor, owing to the nearly-zero low-k interfacial layer and low-defect interface between HZO and IGZO, such enhancement of the charge trapping can be avoided. The fabricated capacitor mitigates such degradation by cycling and realizes at least 10^8 program/erase cycles before breakdown.

For the retention measurement, a ±4 V 1 kHz triangle signal is used to program and erase corresponding to accumulation and depletion in IGZO, respectively. During the retention time, the electrodes of the capacitor are connected to the ground. The P_r is measured by using a 4 V triangle signal after the retention time as shown in Fig. 3(b). Figure 3(c) shows the retention characteristics. The erase state has a worse retention characteristic because the depleted IGZO layer induces larger depolarization fields. A 10 year retention is expected from the extrapolation.

Figure 4(a) shows the P–V curves of the retention measurement at the program and erase state at room temperature. A large asymmetric imprint is observed. Figure 4(b) shows the extracted shift of coercive voltage (V_c) in program and erase state. V_c horizontally shifts in the positive direction after erase by the negative voltage on the bottom electrode. On the other hand, V_c horizontally shifts in the negative direction after program by the positive voltage. As reported, the imprint effect is caused by charge trapping. To illustrate the imprint effect, band diagrams of a TiN/HZO/IGZO capacitor in the program and erase state are simulated in Fig. 4(c). The remanent polarization (P_r) in simulation is 30 μC m^−2 as we measured using a 5 V sweep voltage in Fig. 2(a). According to the simulation results, the TiN/HZO interface has a 1.8 eV band offset which is larger than the band offset (1.5 eV) of the IGZO/HZO interface. Due to the workfunction difference and polarization charge, the internal bias voltage drops on HZO as shown in Fig. 4(c). The horizontal shift after erase is relatively smaller than that after program. This is because the impact of the electron injection from the TiN electrode with a midgap workfunction is small due to the high barrier height and the opposing electric field as shown in Fig. 4(c). On the
other hand, the horizontal shift after program is larger than that after the erase. This is because IGZO has a wide band gap and small band offset to HZO, and the electron injection from IGZO is promoted as shown in Fig. 4(c).

$|P_r|$ apparently decreases at $10^5$ s in the erase state as shown in Fig. 4(a). This is because of the large depolarization field caused by the depletion layer in IGZO. In the program state, however, $P_r$ does not significantly decrease at $1 \times 10^5$ s because IGZO is in accumulation and the depolarization field is small.

The $V_c$ shift caused by the imprint effect can be recovered by storing the opposite state. Figure 5(b) shows the measured $P–V$ curves of the fabricated device, which illustrate the imprint effect and recovery. Figure 5(a) explains the measurement method. First, a program state is written into the pristine device and the $P–V$ curve of the device is immediately measured after programming to avoid the imprint effect. The device is now in the program state again. After the long time delay, which is regarded as the retention time, the $P–V$ curve is measured. A positive $V_c$ shift is observed due to the imprint effect described above. Next, an erase state is written into the device and the $P–V$ curve is immediately measured after erase. The $P–V$ curve is recovered. While the device is erased again. After the long time delay, the $P–V$ curve is measured. A positive $V_c$ shift is
observed due to the imprint effect described above. The inset of Fig. 5(b) shows the extracted $V_N$ of the measured $P$–$V$ curves. The asymmetric imprint effect can be recovered by storing the opposite state by detrapping trapped charges. $P_r$ reduction, however, cannot be fully recovered because some of the remaining trapped charges pin domain switching.

In conclusion, we fabricated a TiN/HZO/IGZO/Ti capacitor and investigated its reliability characteristics. The fabricated device shows a high endurance characteristics up to $10^8$ cycles without wake-up owing to the nearly-zero interface layer between HZO and IGZO. A more than 10 year retention is expected from measurement. The asymmetric
imprint effect in the program and erase state was uniquely observed due to the asymmetric structure of the metal/HZO/IGZO/metal capacitor.

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Fig. 4. (Color online) (a) Measured \( P-V \) curves of the fabricated capacitor in program and erase state at room temperature. (b) Extracted shift of \( V_c \) in program and erase state. Red and black show positive \( V_c \) (\( V_c^+ \)) and negative \( V_c \) (\( V_c^- \)), respectively. (c) Simulated band diagrams of the metal/HZO/IGZO/metal capacitor to illustrate the asymmetric imprint effect in program and erase state. 0 V is applied on the top and bottom electrodes.

Fig. 5. (Color online) (a) Voltage waveform to apply for imprint and recovery measurement. (b) Measured \( P-V \) curves with different device state. The inset is the extracted \( V_c \) where the imprint and its recovery are indicated.

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