Phase Angle Control Based Three-phase DVR with Power Factor Correction at Point of Common Coupling

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Abstract—This paper investigates the ability of correcting the power factor at the point of common coupling (PCC) of the source side using dynamic voltage restorer (DVR). By applying the phase angle control (PAC) method, the DVR compensating voltage will be injected with a specific phase angle and magnitude in series with the transmission line, which leads to a power factor angle shift of the resultant load voltage. As a result, the source voltage is always in phase with the source current under different load conditions, which means that the power factor correction is achieved at the PCC of the source side. A laboratorial prototype of the DVR is utilized to verify the proposed control algorithm. The experimental results validate that an approximate unity power factor can be maintained at the source side.

Index Terms—Dynamic voltage restorer (DVR), voltage sag and swell compensation, phase angle control (PAC) method, power factor correction.

I. INTRODUCTION

NOWADAYS, the percentage of the critical loads (e.g., computer numerical control equipment, programmable logic controllers, chip manufacturing factory) integrated in the power system has increased rapidly [1]. The critical loads are sensitive to the supply voltage power quality problems such as voltage sag, swell, harmonic distortion, etc. The afore-mentioned voltage power quality problems may result in shutting down and even damaging of the critical loads [2], [3]. Therefore, it is essential to maintain the load-side voltage at sinusoidal waveform to protect the critical loads [4].

The dynamic voltage restorer (DVR) is a commonly used device to deal with voltage-related power quality problems [5] - [19]. DVRs are connected near the load side through long and often unreliable feeders. The basic configuration of the three-phase DVR is illustrated in Fig. A1 of Appendix A.

A typical DVR consists of a three-phase six-switch voltage source converter (VSC) to achieve DC/AC conversion, a DC voltage source to supply the DC link of the VSC, a filter to suppress the switching harmonics of the VSC, and a series transformer to obtain the series voltage injection at the distribution line. The DC link can also be supported by a parallel converter and a distribution generator (DG). The detailed configurations of a parallel converter and a DG supported DVRs are presented in Appendix B. The operation principle of the DVR is to inject a voltage of specific phase angle and magnitude in series with the distribution line in order to form a rated sinusoidal load voltage [5] - [19]. In the literature, the DVR can operate in various compensation modes, including the pre-sag mode [7], [8], the in-phase mode [9], [10], the self-supported mode [11] - [16], and the energy-optimized mode [17] - [19]. Specifically, besides the ability to maintain the desired sinusoidal waveform at the load side, the DVR can optimize the energy handled by it, or operate at capacitor-supported mode without DC link active power supply. It is noted that the focus of previous works is on the load voltage side or the DVR itself. The power factor at the point of common coupling (PCC) of the source side has seldom been the focus of researchers.

It is well known that power factor plays a crucial role in the power transmission system [4]. To transfer a certain amount of electrical power, the current magnitude on the transmission line is higher with a lower power factor. The size of the transmission line conductor must increase accordingly in order to handle the higher current magnitude. Hence, the manufacture cost of the transmission system is increased. The higher current magnitude will also increase the transmission line losses, as the line losses are proportional to the square of the current magnitude [4]. Furthermore, a higher current will result in a higher voltage drop along the transmission line. Thus, the voltage profile becomes poor. All the afore-mentioned disadvantages of low power factor will reduce the efficiencies of power transmission and generation. In this case, the power supply companies will impose a penalty against the customer of low power factor. Therefore, it is important to correct the power factor at the PCC. In this paper, we attempt to improve the controller of DVR to correct the power factor at the PCC without compromising the voltage sag and swell compensation at the load side.
In [7], [10], [13], [18], [20], [21], the phase angle control (PAC) methods have shown good performance in coordinating the power handled by DVR. By adjusting the phase angle and magnitude of the injection voltage, the DVR can operate in different modes, and the power supplied by the source and DVR are coordinated. For example, if the injection voltage is in quadrature with the source current, the DVR will operate in the self-supported mode [11]-[16]. That is, the DVR will only supply part of the load reactive power. If the injection voltage is in phase with the source voltage, the DVR will operate in the in-phase mode [9], [10]. In this case, the DVR will support part of the load active and reactive power demand. In this paper, we attempt to utilize the PAC method in the DVR controller to achieve the power factor correction at the PCC as well as the voltage sag and swell compensation. Specifically, the load power factor angle is tracked using the instantaneous power theory. By making the controllable phase angle between the source voltage and load voltage equal to the obtained load power factor angle, the DVR can handle all the load reactive power demand. In this way, the unity power factor can be maintained at the PCC of the source side.

The rest of the paper is organized as follows. Section II describes the fundamentals of the PAC method. The controller design of DVR is presented in Section III. The experimental results are shown in Section IV. Section V concludes this paper.

II. FUNDAMENTALS OF PAC METHOD

A. Types of DVR Injection

The phasor diagrams of the DVR are illustrated in Figs. 1 and 2. The locus of $V_L$ and $I_L$ are illustrated with dashed lines. As $V_L$ has a rated magnitude and a controllable phase angle $\delta$, $V_L$ can follow the locus by changing $\delta$. Correspondingly, $I_L$ will follow its own locus.

1) Case 1
When the injected voltage of the DVR $V_{DVR1}$ is in phase with the source voltage $V_S$, the resultant load voltage $V_{L1}$ will also be in phase with $V_S$ as illustrated in Fig. 1. The angle between the load current $I_{L1}$ and $V_{L1}$ is the load power factor angle $\phi$.

2) Case 2
When the voltage of the DVR $V_{DVR2}$ is injected with a phase angle $\gamma$ and magnitude to guarantee the load voltage $V_{L2}$ at the desired magnitude with a phase angle shift $\delta$, the resulting load current $I_{L2}$ will have a corresponding phase angle shift $\delta$ as illustrated in Fig. 1 [11]-[19]. The angle between $I_{L2}$ and $V_{L2}$ remains unchanged when the load is not changed.

3) Case 3
Let us consider a specific situation of Case 2. If $\delta$ can be maintained at an amount equal to $\phi$ under all load power factor conditions, the load current $I_*'$ in the specific case will be always in phase with $V_S$, which is presented in Fig. 2. As the current at the PCC of the source side $I_s$ is equal to $I_*'$, the unity power factor is achieved at the PCC. We then need to calculate the specific magnitude reference $V_{DVR}^*$ and phase angle reference $\gamma$ of the DVR injection voltage to keep the source voltage always in phase with the source current.

\[ V_{DVR}^* = \sqrt{(V_L^* \cos \phi - V_S)^2 + (V_L^* \sin \phi)^2} \]  

B. Calculation of Magnitude Reference and Phase Angle Reference

From Fig. 2, the magnitude reference of the DVR injection voltage can be calculated as:

\[ V_{DVR}^* = \sqrt{(V_L^* \cos \phi - V_S)^2 + (V_L^* \sin \phi)^2} \]  

where $V_L^*$ is the desired load voltage magnitude, and $\phi$ is the instantaneous load power factor angle.

The phase angle reference of the DVR injection voltage can be computed as follows:
\[ y' = \begin{cases} \arctan \left( \frac{V_L' \sin \phi}{V_L' \cos \phi - V_S} \right) & V_L' \cos \phi > V_S \\ 180^\circ - \arctan \left( \frac{V_L' \sin \phi}{V_S - V_L' \cos \phi} \right) & V_L' \cos \phi \leq V_S \end{cases} \] (2)

It is noted that in (1) and (2), the value of \( V_S \) can be obtained at the PCC of the source side. If the value of \( \phi \) can be calculated instantaneously under all load conditions, the required magnitude reference and phase angle reference of the DVR injection voltage can be obtained.

C. Computation of \( \phi \)

\( \phi \) can be calculated by utilizing the \( p-q \) theory of Akagi [22] as follows:

\[ p_L = v_{L,a}i_{L,a} + v_{L,b}i_{L,b} \] (3)

\[ q_L = v_{L,a}i_{L,b} - v_{L,b}i_{L,a} \] (4)

where \( p_L \) and \( q_L \) are the instantaneous active and reactive load power, respectively; and \( v_{L,a}, v_{L,b} \) and \( i_{L,a}, i_{L,b} \) are the \( \alpha \) and \( \beta \) components of the measured load voltage and current \((v_{L,abc} \text{ and } i_{L,abc})\) after the Clarke transformation [21]. Once \( p_L \) and \( q_L \) are obtained, the load apparent power will be computed as:

\[ s_L = \sqrt{p_L^2 + q_L^2} \] (5)

\( \phi \) is calculated as:

\[ \phi = \arcsin \left( \frac{q_L}{s_L} \right) \] (6)

By obtaining the instantaneous load power factor angle \( \phi \), the desired magnitude and phase angle of DVR injection voltage are known values.

D. Calculation of Voltage References for DVR

To maintain the load-side voltage at a nominal value and achieve power factor correction at the PCC of the source side, the DVR voltage references can be generated as follows:

\[ v_{DVR,a}^* = \sqrt{2} V_{DVR} \sin (\omega t + y') \] (7)

\[ v_{DVR,b}^* = \sqrt{2} V_{DVR} \sin (\omega t - \frac{2}{3} \pi + y') \] (8)

\[ v_{DVR,c}^* = \sqrt{2} V_{DVR} \sin (\omega t + \frac{2}{3} \pi + y') \] (9)

where \( v_{DVR,k}^* \) (\( k = a, b, c \)) is the injection voltage reference; and the synchronization phase angle \( \omega t \) can be obtained from the synchronized source voltage \( v_{S,abc} \) by utilizing the phase-locked loop (PLL) controller [5] - [7]. Based on the generated DVR injection voltage references, the controller is designed in the next section.

III. DVR CONTROLLER DESIGN

The signal flow diagrams of the DVR controller are illustrated in Fig. 3. The measured parameters in the control process are source voltage \( v_{S,abc} \), load voltage \( v_{L,abc} \), load current \( i_{L,abc} \) and DVR injection voltage \( v_{DVR,abc} \).

A. Generation of \( \phi \)

Figure 3(a) illustrates the process of generating the instantaneous \( \phi \) in the controller of DVR. The measured load voltage \( v_{L,abc} \) and load current \( i_{L,abc} \) are transformed from \( abc \) frame to \( a\beta \) frame by Clarke transformation. The obtained \( v_{L,αβ} \) and \( i_{L,αβ} \) are utilized to calculate the instantaneous load reactive and active power \((q_L \text{ and } p_L)\) via Fig. 3(a) and 3(b). Then \( \phi \) is computed using (6). A low pass filter (LPF) is applied to avoid rapid change in the value of \( \phi \).

B. Generation of DVR Injection Voltage References and Gate Signals

The magnitude of the source voltage \( V_S \) can be obtained by calculating the root-mean-square (RMS) value of the measured source voltage \( v_{S,abc} \). After that, the desired load voltage magnitude \( V_L^* \), the calculated \( \phi \), and \( V_S \) are used to compute the magnitude reference \( V_{DVR}^* \) and phase angle reference \( y' \) of the DVR injection voltage by (1) and (2). A PLL controller can be utilized to obtain the \( \omega t \) from the measured \( v_{S,abc} \). Then \( V_{DVR}^* \), \( y' \), and \( \omega t \) are used to generate the three-phase voltage references \( v_{DVR,abc}^* \) following (7) - (9). \( v_{DVR,abc} \) and measured DVR injection voltage \( v_{DVR,abc} \) are compared in the hysteresis controller to generate the gate signals (G1, G2, …, G6) for the switches (S1, S2, …, S6) the VSC, as shown in Fig. 3(b).
C. Hysteresis Controller

Generally, in the hysteresis controller, the DVR injection voltage reference \( v_{\text{DVR}_{\text{abc}}} \) is compared with the measured DVR injection voltage \( v_{\text{DVR}_{\text{abc}}} \) for each phase, as shown in Fig. 3(c). The errors are sent to the hysteresis comparators. Then the outputs of the comparators are the gate signals utilized to control the switches of VSC. The width of the hysteresis band is \( 2 \times 0.1 \text{ V} \). We take the voltage of Phase a as an example. When the measured DVR injection voltage of Phase a \( v_{\text{DVR}_{\text{a}}} \) is higher than the reference voltage \( v_{\text{DVR}_{\text{a}}}^{*} \) and the error is bigger than \( 0.1 \text{ V} \), the hysteresis comparator will output a “0” signal. The gate signals G1 and G2 are set to “0” and “+1”, respectively. Then S1 will be closed and S2 will be open. As a result, \( v_{\text{DVR}_{\text{a}}} \) will decrease. When \( v_{\text{DVR}_{\text{a}}} \) is reduced to the value of \( v_{\text{DVR}_{\text{a}}}^{*} \), the output of the hysteresis comparator is still a “0” signal. Switches S1 and S2 remain at their previous states. The value of \( v_{\text{DVR}_{\text{a}}} \) will keep on decreasing. When the value of \( v_{\text{DVR}_{\text{a}}} \) is lower than that of \( v_{\text{DVR}_{\text{a}}}^{*} \), and the error is greater than \( 0.1 \text{ V} \), the hysteresis comparator will output a “+1” signal. The gate signals G1 and G2 become “+1” and “0”, respectively. Then S1 will be open and S2 will be closed. Consequently, the value of \( v_{\text{DVR}_{\text{a}}} \) will increase. The aforementioned process will ensure that the error between \( v_{\text{DVR}_{\text{a}}} \) and \( v_{\text{DVR}_{\text{a}}}^{*} \) is always within \([-0.1, +0.1]\]. The similar hysteresis control processes are applied in phase b and phase c.

IV. EXPERIMENTAL RESULTS

Based on the controller developed in Section III, the experimental results are carried out to validate the voltage sag/swell compensation ability and power factor correction function of DVR. The schematic of the laboratorial prototype of DVR is presented in Fig. 4. In the hardware setup, the HEWLETT PACKARD 6834B programmable AC power source is utilized as the AC supply of the system. The SEMIKRON three-phase insulated gate bipolar transistor (IGBT) based inverter is used as the VSC of DVR. The IGBT module serial number is SKM75GB12T4. The Chroma 62012P-600-8 programmable DC power source is adopted to support the DC link of VSC. The resistor bank and the inductor bank are connected at the load side of the system. The voltage ratio of the transformer is 1. The filter can mitigate the high frequency harmonics from the IGBT-based VSC. The dSPACE 1103 is utilized as the digital signal processor to realize the control of the IGBT-based VSC. The LeCroy oscilloscope is used to observe and capture the voltage and current waveforms. The FLUKE 434 energy analyzer is utilized to measure the power factors at the source and load sides. The parameters of the hardware setup are summarized in Table I. The experimental results are presented in Sections IV-A and IV-B.

![Schematic of laboratorial prototype of DVR](image)

**TABLE I**

| Parameter | Value |
|-----------|-------|
| Nominal phase voltage of HEWLETT PACKARD 6834B programmable AC power source \( (V_{\text{abc}}) \) | 42 V |
| Nominal frequency of HEWLETT PACKARD 6834B programmable AC power source \( (f) \) | 50 Hz |
| Supply voltage of Chroma 62012P-600-8 programmable DC power source \( (V_{\text{dc}}) \) | 55 V |
| Load power factor (PF) | 0.7 lagging/0.9 lagging |
| Voltage ratio of series transformer \( (n) \) | 1 |
| Filter inductance \( (L_{f,a}, L_{f,b}, L_{f,c}) \) | 6.3 mH |
| Filter capacitance \( (C_{f,a}, C_{f,b}, C_{f,c}) \) | 20 μF |
| Filter resistance \( (R_{f,a}, R_{f,b}, R_{f,c}) \) | 10 Ω |
| Sampling time of dSPACE 1103 \( (T_{s}) \) | 50 s |

A. Voltage Sag and Swell Compensation Results

In Fig. 5(a), it can be observed that the source voltage drops from the nominal voltage \( (42 \text{ V}) \) to a sag voltage \( (30 \text{ V}) \). The duration of each sag condition is \( 0.1 \text{ s} \), i.e., 5 cycles. By injecting the DVR compensation voltage as illustrated in Fig. 5(b), the load voltage in Fig. 5(c) can remain at the nominal value. From Fig. 6(a), each voltage swell condition \( (54 \text{ V}) \) lasts for \( 0.1 \text{ s} \), i.e., 5 cycles. The load voltage in
Fig. 6(c) can still remain at the rated value due to the DVR injection voltage presented in Fig. 6(b).

B. Power Factor Correction Results

In the experiment of power factor correction, a power factor step change is set from 0.7 lagging to 0.9 lagging to verify the power factor correction performance of the proposed PAC method under different load conditions. Meanwhile, the source is operating under a sag condition ($V_s = 30 \text{ V}$). In order to have a clear illustration of the phase angle difference between the current and voltage, only the current and voltage of phase a are presented.

1) Experimental results without PAC method

The experimental results of DVR without the PAC method are presented in Fig. 7 and Table II.

![Fig. 6. Experimental results of DVR with voltage swell. (a) Source voltage $v_{S,abc}$. (b). DVR injection voltage $v_{DVR,abc}$. (c) Load voltage $v_{L,abc}$.](image-url)

![Fig. 5. Experimental results of DVR with voltage sag. (a) Source voltage $v_{S,abc}$. (b). DVR injection voltage $v_{DVR,abc}$. (c) Load voltage $v_{L,abc}$.](image-url)

![Fig. 7. Experimental results of DVR without PAC method. (a) Dynamic performance with load step change. (b) Phase angle difference before step change. (c) Phase angle difference after step change.](image-url)
means that the power factor correction can be realized under different load conditions. The ratio between $P_S$ and $P_L$ as well as the ratio between $Q_S$ and $Q_L$, still satisfies the equations derived in Appendix D.

### TABLE II

**Power Factor of System Without PAC**

| Power factor                        | Value |
|-------------------------------------|-------|
| Load-side power factor before step change | 0.69  |
| Source-side power factor before step change | 0.68  |
| Load-side power factor after step change | 0.90  |
| Source-side power factor after step change | 0.89  |

From Fig. 7(a), it can be observed that a load step change happens during the operation of the DVR. The source voltage $v_{s,a}$ is under the sag condition ($V_s = 30\text{ V}$), while the load voltage $v_{L,a}$ is the nominal value ($V_L = 42\text{ V}$) after compensation. Before step change, due to the absence of the PAC method, the load voltage $v_{L,a}$ is in phase with the source voltage $v_{s,a}$ as illustrated in Fig. 7(b). Meanwhile, $v_{s,a}$ lags the source current $i_{s,a}$ by $45.6^\circ$, which is the power factor angle before step change (arccos $0.7 = 45.6^\circ$). The measured power factors of the load side and source side before the step change are shown in Table II as 0.69 and 0.68, respectively. It is noted that the power factors are nearly the same at load and source sides, which means that there is no power factor correction at the source side. The ratio between $P_S$ and $P_L$ as well as the ratio between $Q_S$ and $Q_L$, satisfies the equations derived in Appendix C. After step change, $v_{s,a}$ is still in phase with $v_{s,a}$ as presented in Fig. 7(c), while $v_{s,a}$ lags $i_{s,a}$ by $25.8^\circ$, which is the power factor angle after step change (arccos $0.9 = 25.8^\circ$). The measured power factors of the load side and source side after the step change are presented in Table II as 0.90 and 0.89, respectively. It can be concluded that there is still no power factor correction at the source side. The ratio between $P_S$ and $P_L$ as well as the ratio between $Q_S$ and $Q_L$, still satisfies the equations in Appendix C.

2) Experimental results with PAC method

The experimental results of DVR with the PAC method are presented in Fig. 8 and Table III. We generate the same load step change as illustrated in Fig. 8(a). $v_{s,a}$ is in the sag condition ($V_s = 30\text{ V}$), while $v_{L,a}$ is the nominal value ($V_L = 42\text{ V}$) after compensation. It can be seen from Fig. 8(b), before step change, as the PAC method is applied, $v_{L,a}$ lags $v_{s,a}$ by $45.6^\circ$, which is the power factor angle before step change (arccos $0.7 = 45.6^\circ$). At the same time, $v_{s,a}$ is in phase with $i_{s,a}$, which means a unity power factor is achieved at the source side. The measured power factors of the load side and source side before the step change are presented in Table III as 0.69 and 0.97, respectively. It is noted that an approximate unity power factor is achieved at the source side. The ratio between $P_S$ and $P_L$ as well as the ratio between $Q_S$ and $Q_L$, satisfies the equations derived in Appendix D. As presented in Fig. 8(c), $v_{L,a}$ lags $v_{s,a}$ by $25.8^\circ$, which is the power factor angle after step change (arccos $0.9 = 25.8^\circ$). $v_{s,a}$ is still in phase with $i_{s,a}$, which means the unity power factor can be maintained at the source side in different load conditions. The measured power factors of the load side and source side before the step change are presented in Table III as 0.90 and 0.99, respectively. It can be observed that an approximate unity power factor can still be maintained, which

### TABLE III

**Power Factor of System With PAC**

| Power factor                        | Value |
|-------------------------------------|-------|
| Load-side power factor before step change | 0.69  |
| Source-side power factor before step change | 0.97  |
| Load-side power factor after step change | 0.90  |
| Source-side power factor after step change | 0.99  |

### V. CONCLUSION

In this paper, the PAC method has been applied to control the DVR, which provides the power factor correction at the
PCC of the source side without compromising the voltage sag and swell compensating ability of DVR. Specifically, the DVR compensating voltage is injected with a specific magnitude and phase angle, which leads to a power factor angle shift of the resultant load voltage. Correspondingly, the source voltage is always in phase with the source current in different load conditions.

A hardware prototype has been built to validate the performance of the proposed PAC method. The experimental results have demonstrated that an approximate unity power factor can be maintained at the source side, so that the power factor correction is achieved at the PCC of the source side.

APPENDIX A

The configuration of the three-phase DVR system is illustrated in Fig. A1.

Fig. A1. Configuration of three-phase DVR system.

APPENDIX B

The configurations of a parallel converter and a DG supported DVRs are presented in Fig. B1 and B2, respectively. In Fig. B1, it is noted that the active power required by the DVR as well as the power losses to maintain the DC link voltage, is supported by the parallel converter uninterruptedly [23]. Eventually, the active power is from the grid source. In Fig. B2, the DG can support the active power required by the DVR. Thus, the amount of active power delivered to the load is larger than that supplied from the grid source.

Fig. B1. Configuration of parallel converter supported DVR.

Fig. B2. Configuration of DG supported DVR.

APPENDIX C

Without the PAC method, the active power \( (P_L) \) and reactive power \( (Q_L) \) at the load side and source side can be calculated as:

\[
P_L = V_L I_L \cos \phi \quad (C1)
\]

\[
Q_L = V_L I_L \sin \phi \quad (C2)
\]

\[
P_S = V_S I_S \cos \phi \quad (C3)
\]

\[
Q_S = V_S I_S \sin \phi \quad (C4)
\]

Without the PAC method, the ratio between \( P_S \) and \( P_L \) as well as the ratio between \( Q_S \) and \( Q_L \), can be derived as:

\[
\frac{P_S}{P_L} = \frac{V_S}{V_L} \quad (C5)
\]

\[
\frac{Q_S}{Q_L} = \frac{V_S}{V_L} \quad (C6)
\]

APPENDIX D

With the PAC method, the active power \( (P_L) \) and reactive power \( (Q_L) \) at the load side and source side can be computed as:

\[
P_L = V_L^* I_L^* \cos \phi \quad (D1)
\]

\[
Q_L = V_L^* I_L^* \sin \phi \quad (D2)
\]

\[
P_S = V_S I_S \quad (D3)
\]

\[
Q_S = 0 \quad (D4)
\]

With the PAC method, the ratio between \( P_S \) and \( P_L \) as well as the ratio between \( Q_S \) and \( Q_L \), can be derived as:

\[
\frac{P_S}{P_L} = \frac{V_S}{V_L^* \cos \phi} \quad (D5)
\]

\[
\frac{Q_S}{Q_L} = 0 \quad (D6)
\]

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The text includes references to various research works and academic achievements. It discusses topics such as dynamic voltage restorer (DVR) for unbalanced and distorted loads, control strategies for DVR, and optimization of energy injection. The text also mentions the contributions of different authors to these fields, highlighting their academic and professional backgrounds.

The text concludes with the recognition of specific individuals. It notes that Jian Ye received a B.Eng. degree in electrical engineering and automation from Wuhan University, Wuhan, China, in 2012, and M.Sc. and Ph.D. degrees in power engineering from the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, in 2013 and 2018, respectively. His research interests include connecting renewable energy sources, energy devices to microgrids, and power quality compensation.

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