Abstract—This paper presents the first multiband mm-wave linear Doherty PA in silicon for broadband 5G applications. We introduce a new transformer-based on-chip Doherty power combiner, which can reduce the impedance transformation ratio in power back-off (PBO) and thus improve the bandwidth and power-combining efficiency. We also devise a “driver-PA co-design” method, which creates power-dependent uneven feeding in the Doherty PA and enhances the Doherty operation without any hardware overhead or bandwidth compromise. For the proof of concept, we implement a 28/37/39-GHz PA fully integrated in a standard 130-nm SiGe BiCMOS process, which occupies 1.8mm². The PA achieves a 52% −3-dB small-signal S21 bandwidth and a 40% −1-dB large-signal saturated output power (P_{sat}) bandwidth. At 28/37/39GHz, the PA achieves +16.8/+17.1/+17-dBm P_{sat}, +15.2/+15.5/+15.4-dBm P_{1dB}, and superior 1.72/1.92/1.62 times efficiency enhancement over class-B operation at 5.9/6.7-dB PBO. Moreover, the PA demonstrates multi-Gb/s data rates with excellent efficiency and linearity for 64QAM in all the three 5G bands. This PA advances the state of the art for Doherty, wideband, and 5G silicon PAs in mm-wave bands. It supports drop-in upgrade for current PAs in existing mm-wave systems and opens doors to compact system solutions for future multiband 5G massive MIMO and phased-array platforms.

Index Terms—5G, broadband, integrated circuits, Doherty, efficiency, linearity, massive MIMO, multiband, phased array, power amplifier, power back-off, reconfiguration, silicon, SiGe BiCMOS, transformer.

I. INTRODUCTION

Multiple use cases in future fifth-generation (5G) wireless systems, such as enhanced mobile broadband (eMBB), target multi-Gb/s user-experienced data rates [1]. Such ultra-high throughput will not only augment existing wireless data communication, but also enable numerous emerging applications such as augmented reality (AR), virtual reality (VR), and mixed reality (MR) [2], [3].

To achieve multi-Gb/s data rates, the 5G wireless systems are evolving towards mm-wave [4], [5]. The Federal Communications Commission (FCC) has opened multiple mm-wave frequency bands for 5G development in the United States, including spectra around 28, 37, and 39GHz [6]. Different regions in the world are interested in various mm-wave frequency bands for 5G (Fig. 1) [6], [7]. Moreover, the mm-wave 5G systems will extensively leverage massive multiple-input multiple-output (MIMO) and phased-array architectures to improve the link performance by strengthening desired signal and enhancing interference rejection. As a result, multiband mm-wave 5G systems are highly desired to facilitate future international/cross-network roaming and MIMO diversity. Together with existing wideband mm-wave antenna arrays [8]-[10], multiband mm-wave 5G circuits will greatly shrink the form factor of future massive MIMO and phased-array 5G systems. On top of the evolution towards mm-wave, the future 5G systems will leverage spectrum-efficient modulations such as high-order quadrature amplitude modulations (QAMs) to achieve high data rates for given spectrum resource [1]. These 5G waveforms have large peak-to-average power ratios (PAPRs) and lead to circuit design challenges [11]. Mobile devices utilizing mm-wave 5G techniques, such as 5G handsets and VR headsets, should be energy efficient in power back-off (PBO) to extend the battery life and ease the thermal management. Also due to the high PAPR, these mm-wave 5G systems need to be highly linear in a wide power range for both their amplitude and phase responses to ensure the quality of service and thus user experience.

Power amplifier (PA) is often the most power-hungry block in a wireless transceiver and need to handle large signals. Therefore, PA often governs the energy efficiency and linearity of a wireless transmitter [12], [13]. Significant progresses in the silicon-based mm-wave PA have been made in the past decade [14]-[43]. Wideband mm-wave PAs using distributed topologies [17] or high-order passive networks [30] have been demonstrated in literature. However, they often compromise efficiency due to inefficient active circuits or passive networks. Advanced distributed PA designs improve the efficiency with...
increased overhead in the power management unit [32]. In parallel, various PA BBO efficiency enhancement techniques have been demonstrated at mm-wave. However, many of them entail challenges for the large modulation bandwidth in broadband 5G applications. Mode-switching PAs [26], [36] entail challenges to achieve dynamic power-mode switching at the speed of 5G signals’ envelopes. Outphasing PAs require the generation of high-speed outphasing signals, which demands significant baseband overhead [23]. Envelope tracking (ET) PAs require high-speed supply modulators with wide dynamic ranges, and state-of-the-art ET designs demonstrate modulation bandwidth only up to tens of MHz [44], [45]. Compared with others, Doherty PAs fundamentally can support the wide modulation bandwidth in broadband 5G applications [46]-[51]. However, Doherty PAs require complex power combiners, which could be lossy and limit the carrier bandwidth. In addition, Doherty PAs demand careful cooperation between at least two PA paths to ensure the efficiency and linearity. Although digital-intensive Doherty PAs in recent research address this issue at sub-6GHz [52]-[59], their direct extension to mm-wave bandwidth 5G could result in unaffordable baseband overhead. Consequently, existing mm-wave Doherty PAs in silicon exhibit limited BBO efficiency enhancement.

Therefore, wideband mm-wave PA in silicon with efficiency enhancement is an urgent-yet-unmet need for 5G massive MIMO and phased-array systems. We demonstrate the first mm-wave linear Doherty PA in silicon, which achieves substantial BBO efficiency enhancement and supports three mm-wave 5G bands with multi-Gb/s data rates [60]. Section II and III present the introduced transformer-based low-loss/broadband Doherty power combiner and power-dependent Doherty PA uneven-feeding scheme, respectively. They are two enabling techniques that address the challenges in conventional mm-wave Doherty PA designs. Sections IV shows the implementation details and test results.

II. TRANSFORMER-BASED LOW-LOSS AND BROADBAND DOHERTY POWER COMBINER

Doherty PA is generally comprised of multiple PA active cells, a Doherty power combiner, and an input network (Fig. 2a). The input network balances the phases of PA paths to ensure efficient power combiner at the PA output. The Doherty power combiner plays critical roles. It performs not only power sum, but also active load modulation that enhances the efficiency of PA active circuits. Its performance has large impacts on the PA efficiency and bandwidth and often dominates the chip area in fully integrated Doherty PAs. This section first reviews the conventional approaches of two-way Doherty power combiners and then introduces a new low-loss, broadband, and compact design.

In the following analyses, we assume that the main and auxiliary PAs share the same supply voltage, and the maximum RF current of the auxiliary PA is α times the maximum RF current of the main PA. In a symmetric Doherty PA, α equals one, and the second efficiency peak ideally happens at 6-dB PBO. In asymmetric Doherty PAs, the second efficiency peak happens at <6-dB PBO or >6-dB PBO when the auxiliary PA is weaker (α<1) or stronger (α>1) than the main PA. We derive the desired relationship between the RF currents of the main and auxiliary PAs as

\[ i_{aux} = \begin{cases} 
(1+\alpha)i_{main} - \frac{2}{1+\alpha}, & \frac{2}{1+\alpha} \leq i_{main} \leq \frac{2}{1+\alpha} \\
0, & 0 \leq i_{main} < \frac{2}{(1+\alpha)^2} 
\end{cases} \]

where \( i_{main} \in [0, \frac{2}{1+\alpha}] \) and \( i_{aux} \in [0, \frac{2\alpha}{1+\alpha}] \) are the normalized RF currents of the main and auxiliary PAs [61]. Fig 2b illustrates the symmetric case (α=1). By these definitions, the sum of maximum \( i_{main} \) and \( i_{aux} \) is independent to α, and the Doherty PA peak output power \( P_{out} \) remain constant when α varies. The BBO level in decibel is calculated as 20log\[10\{2/(1+\alpha)i_{main}\}\] [61], and the load-pull impedances of the main and auxiliary PAs at the Doherty PA peak \( P_{out} \) are defined as \((1+\alpha)R_{opt}/2\) and \((1+\alpha)R_{opt}/(2\alpha)\), respectively.

A. Conventional Doherty Power Combiners

1) Parallel Doherty Power Combiners

Most conventional Doherty power combiners derive from a two-λ/4-line-based architecture in Fig. 3. These Doherty power combiners perform parallel power combining for current-mode PAs and achieve true Doherty load modulation.

In this architecture, the λ/4 line TL2 down scales the PA load impedance for high PA \( P_{out} \). It transforms \( R_{L} \) to \( R_{opt}/2 \) at all PA \( P_{out} \) levels, and its characteristic impedance is

\[ Z_{opt} = \frac{R_{opt}R_{L}}{2} \]  

The other λ/4 line at the main PA output, TL1, in Fig. 3, performs as an impedance inverter, and its characteristic impedance is derived as

![Fig. 2. (a) Conceptual diagram of a Doherty PA. (b) Ideal cooperation between the main and auxiliary paths in a symmetric two-way Doherty PA.](Image)
$$Z_{01} = \frac{1 + \alpha}{2} R_{\text{opt}}.$$  \hspace{1cm} (3)

To implement these \(\lambda/4\) lines in silicon, conventional integrated designs often employ transmission lines [27], \(\pi\)-network approximations using lumped elements [62]-[65], or transformer-based solutions [54], [55]. However, any implementations derived from this two-\(\lambda/4\)-line-based Doherty power combiner inherently suffer high impedance transformation ratios (ITRs) in PBO for the impedance inverter. When the auxiliary PA is on, i.e., \(i_{\text{main}} \geq 2/(1+\alpha)^2\), \(2/(1+\alpha)\), the ITR of TL1 in Fig. 3 is derived as

$$\text{ITR}_{\text{Conv}} = \left[\frac{1 + \alpha}{2 + \alpha} - \frac{1}{\sqrt{2}} \frac{1 + \alpha}{i_{\text{main}}}\right]^2.$$  \hspace{1cm} (4)

Note that the term in the square bracket in (4) is always \(\geq 1\). (4) implies two important mathematical insights. First, for any given \(\alpha > 0\), \(\text{ITR}_{\text{Conv}}\) monotonically increases when \(i_{\text{main}}\) decreases. In other words, the ITR of TL1 in Fig. 3 gradually increases during PBO, until the auxiliary PA is off (Fig. 4). For example, \(\text{ITR}_{\text{Conv}}\) in the symmetric design is unity at the peak \(P_{\text{out}}\) and is as high as four times at 6-dB PBO. Note that such implementations derived from this two-\(\lambda/4\)-line-based Doherty power combiner compromises the asymmetric design techniques. Note that these deteriorations in passive efficiency and bandwidth are independent to the Doherty PA peak \(P_{\text{out}}\).

2) Series Doherty Power Combiners

Researchers demonstrate Doherty PAs that use series power combiners summing the power from current-mode PAs and achieve true Doherty load modulation. However, in order to properly terminate the series-combining transformer at the auxiliary PA side when the auxiliary PA is off, additional matching networks [29], [65], [66] or switches [47] are required at the auxiliary PA output, which either demand extra chip area or degrade reliability. Removing these overhead at the auxiliary PA output leads to Doherty-like operation and degraded PA efficiency [67], [68]. Doherty PAs that use series power combiners together with voltage-mode PAs such as switched-capacitor PAs [69] have been recently developed at sub-6GHz [50]-[52]. They achieve true Doherty load modulation without the overhead of passives or switches at the auxiliary PA output. However, designing efficient voltage-mode PAs at mm-wave entails challenges.

B. Low-Loss and Broadband Doherty Power Combiner

1) Theoretical Analyses Based On the \(\lambda/4\)-Line Model

In the field of microwave theory and techniques, a three-\(\lambda/4\)-line-based Doherty power combiner is presented (Fig. 5) [70]-[74]. It combines power from two current-mode PAs and achieves true Doherty load modulation. In this network, the \(\lambda/4\) line at the main PA output, TL1 in Fig. 5, acts as an impedance inverter, and its characteristic impedance is derived as

$$Z_{01} = (1 + \alpha) \sqrt{\frac{R_{\text{opt}} R_L}{2}}.$$  \hspace{1cm} (5)

Meanwhile, the characteristic impedances of the two \(\lambda/4\) lines at the auxiliary PA output, TL2 and TL3 in Fig. 5 should satisfy

$$Z_{02} = \frac{2R_L}{\sqrt{R_{\text{opt}}}}, \quad Z_{03} = \frac{(1 + \alpha)R_L}{2}.$$  \hspace{1cm} (6)

\(Z_02\) and \(Z_03\) can be arbitrarily chosen in their physically achievable range, as long as their ratio meets (6). For example, if choosing \(Z_02 = Z_{03} = (1 + \alpha)\sqrt{R_{\text{opt}} R_L}/2\), \(Z_01 = (1 + \alpha)R_L\).

When the auxiliary PA is on, i.e., \(i_{\text{main}} \geq 2/(1+\alpha)^2\), \(2/(1+\alpha)\), the ITR of TL1 in Fig. 5 is derived as

$$\text{ITR}_{\text{Conv}} = \begin{cases} \beta, & \text{if } \beta \geq 1 \\ \beta/\beta, & \text{if } \beta < 1 \end{cases}. $$  \hspace{1cm} (7)

where

$$\beta = \frac{R_{\text{opt}}}{2R_L} \left[\frac{1 + \alpha}{2 + \alpha} - \frac{1}{\sqrt{2}} \frac{1 + \alpha}{i_{\text{main}}}\right]^2.$$  \hspace{1cm} (8)

Compared with \(\text{ITR}_{\text{Conv}}\), the additional factor of \(R_{\text{opt}}/2R_L\) in (8) leads to fundamental changes. Mathematically, \(\beta\) is not always \(\geq 1\) when the auxiliary PA is on. Therefore, we split (7) into two cases to ensure that \(\text{ITR}_{\text{Conv}} \geq 1\). Physically, this means that the ITR has become dependent on \(R_{\text{opt}}\) and thus the Doherty PA peak \(P_{\text{out}}\).

To explore the characteristics of this three-\(\lambda/4\)-line-based Doherty power combiner in more depth, we consider two scenarios. First, in the symmetric design (\(\alpha = 1\)) with a given \(R_{\text{opt}}\) (and thus peak \(P_{\text{out}}\)), (8) is simplified as
\[ \beta(\alpha = 1) = \frac{2R_{\text{opt}}}{R_{L}(3 - \frac{1}{i_{\text{main}}})} = \frac{R_{\text{opt}}}{2R_{L}} \cdot \text{ITR}_{\text{Conv}}(\alpha = 1). \quad (9) \]

In (4), we observe the monotonicity of ITR\text{Conv} with respect to \( i_{\text{main}} \). The factor of \( R_{\text{opt}}/2R_{L} \) in (9) can eliminate this monotonicity for ITR\text{Intro}. For example, \( R_{\text{opt}}=41.3\Omega \) in our prototype; during PBO, ITR\text{Intro} in the symmetric design first decreases from 2.42 at the peak \( P_{\text{out}} \) \( (i_{\text{main}}=1) \) to unity at 4.7-dB PBO \( (i_{\text{main}}=0.583) \), and then increases to 1.65 at 6-dB PBO \( (i_{\text{main}}=0.5) \) (Fig. 6). Compared with the two-\( \lambda/4 \)-line-based design, the ITR is reduced by 2.42 times at 6-dB PBO while achieving the same peak PA \( P_{\text{out}} \). Such reduction in the ITR enhances passive efficiency in PBO and bandwidth. Second, considering the ITR at the second efficiency peak, we substitute \( i_{\text{main}}=2/(1+\alpha)^2 \) into (8), and

\[ \beta(i_{\text{main}}) = \frac{2}{(1+\alpha)^2} = \frac{(1+\alpha)^2R_{\text{opt}}}{2R_{L}} \cdot \text{ITR}_{\text{Conv}}(i_{\text{main}}) = \frac{2}{(1+\alpha)^2}. \quad (10) \]

Unlike ITR\text{Conv}, ITR\text{Intro} at the second efficiency peak may not monotonically increase with respect to the asymmetric ratio \( \alpha \), again due to the additional factor of \( R_{\text{opt}}/2R_{L} \). In fact, the asymmetric design technique using a stronger auxiliary PA may be leveraged to minimize the ITR at the second efficiency peak and enhance the passive efficiency. For example, if \( R_{\text{opt}}<R_{L}/2 \), the auxiliary PA can be designed as \( (\sqrt{2R_{L}/R_{\text{opt}}}-1) \) times strong as the main PA so that no impedance transformation is required at the second efficiency peak. In other words, we may combine the three-\( \lambda/4 \)-line-based Doherty power combiner with the asymmetric Doherty PA design technique to simultaneously achieve enhanced passive and active efficiencies in deep PBO. Since \( R_{\text{opt}}=41.3\Omega-R_{L}/2 \) in our prototype, we choose the symmetric design. As per our previous discussion, the three-\( \lambda/4 \)-line-based Doherty power combiner achieves 2.42 times ITR reduction at the second efficiency peak in the symmetric design (Fig. 6). Such ITR reduction enhances passive efficiency in PBO and bandwidth.

2) Transformer-Based Low-Loss and Broadband Doherty Power Combiner

The three-\( \lambda/4 \)-line-based Doherty power combiner has been demonstrated in board-level designs [76]-[80]. However, the direct implementation of three \( \lambda/4 \) lines on-chip can be area consuming. We introduce a new transformer-based solution to achieve this three-\( \lambda/4 \)-line-based low-loss and broadband Doherty power combiner [60]. It only occupies a two-transformer footprint, which is very compact. It also absorbs device parasites, which is a broadband practice.

Fig. 6. ITR of the impedance inverter in the three-\( \lambda/4 \)-line-based parallel Doherty power combiner. (R_{\text{opt}}=41.3\Omega).

Next, we describe the process of network synthesis for the new transformer-based Doherty power combiner. First, the three \( \lambda/4 \) lines in Fig. 5 are approximated using \( \pi \)-networks (Fig. 7a). TL1 and TL2 are approximated using low-pass \( \pi \)-networks, and TL3 is approximated using a high-pass \( \pi \)-network. To compensate the phase responses of the \( \pi \)-networks and ensure in-phase power combining at the Doherty PA output, the input phases of the two PA paths are offset accordingly (Fig. 7a). In the second step, two ideal transformers are inserted into this network (Fig. 7b). In the third step, the inductors and capacitors in the three \( \pi \)-networks are reorganized (Fig. 7c). Series inductors are paired with shunt inductors, and four inductors form two groups. Now, we can notice two on-chip transformer models [81]. In other words, series and shunt inductors are absorbed as the leakage and magnetization inductors of two on-chip transformers. As a result, the three-\( \lambda/4 \)-line-based Doherty power combiner is realized in a two-transformer footprint (Fig. 7d). C1 and C2 in Fig. 7d can absorb the parasitic capacitances of PA active cells, and C3 in Fig. 7d can absorb the parasitic capacitances at the Doherty PA output such as pad capacitances.
Based on this process of network synthesis, the closed-form design equations of all the parameters in this network are derived. In the following discussions, we will show the derivations in the symmetric Doherty PA design. Denote the turn ratios and magnetic coupling coefficients of the two transformers as \( n_1 \) and \( k_1 \) for TF1 in the main PA path and \( n_2 \) and \( k_2 \) for TF2 in the auxiliary PA path. The ideal transformers in the on-chip transformer models bring adjustments to (5) and (6). The characteristic impedance of the CLC low-pass \( \pi \)-network in the main PA path is now

\[
Z_{0, LP_{main}} = \frac{k_1}{n_1} \sqrt{2R_{op}R_L}. \tag{11}
\]

The characteristic impedances of the CLC low-pass and LCL high-pass \( \pi \)-networks in the auxiliary PA path now satisfy

\[
Z_{0, HP_{aux}} = \frac{n_2}{k_2} \sqrt{2R_{op}R_L}. \tag{12}
\]

From (11), \( L_{p1} \), the primary inductance of TF1, and \( C_1, C_3 \) in Fig. 7d are calculated as

\[
L_{p1} = \frac{Z_{0, LP_{main}}}{\omega(1-k_1^2)} = \frac{k_1}{\omega(n_1/k_1)^2} \sqrt{2R_{op}R_L}, \tag{13}
\]

\[
C_1 = \frac{1}{\omega Z_{0, LP_{main}}} = \frac{n_1}{\omega k_1 \sqrt{2R_{op}R_L}}, \tag{14}
\]

and

\[
C_3 = \left(\frac{k_2}{n_2}\right)^2 C_1. \tag{15}
\]

Furthermore, we utilize the physical constraint posed by the relationship between the leakage and magnetization inductances in the transformer model. The magnetization inductances in TF1 and TF2, \( L_{m1} \) and \( L_{m2} \), have

\[
Z_{0, HP_{aux}} = \frac{n_2}{k_2} \sqrt{2R_{op}R_L}. \tag{16}
\]

Then, \( L_{p2} \), the primary inductance of TF2, and \( C_5 \) in Fig. 7d are calculated as

\[
L_{p2} = \frac{Z_{0, HP_{aux}}}{\omega(n_2/k_2)^2 k_2^2} = \frac{n_2}{\omega (n_2/k_2)^2} \sqrt{2R_{op}R_L}, \tag{19}
\]

and

\[
C_5 = \frac{1}{\omega Z_{0, HP_{aux}}} = \frac{1-k_2^2}{\omega n_2 k_2 \sqrt{2R_{op}R_L}}. \tag{20}
\]

When \( n_1=n_2, L_{p1} \) in (13) equals \( L_{p2} \) in (19). In other words, the two transformers have the same primary inductance if their turn ratios are the same. From (17),

\[
Z_{0, HP_{aux}} = \frac{n_2^2}{1-k_2^2}. \tag{21}
\]

Based on (12) and (21), we solve \( k_2 \) as

\[
k_2 = \sqrt{n_2^2 R_{op}/(2R_L) + 4 - n_2^2 R_{op}/(2R_L)}. \tag{22}
\]

In summary, for given load-pull impedance \( R_{op}, n_1, k_1, \) and \( n_2 \), all the design parameters in the introduced transformer-based Doherty power combiner can be calculated, as (13)-(15), (19), (20), (22)-(24).

Fig. 8 shows our implemented transformer-based Doherty power combiner. It occupies a two-transformer footprint, which is very compact. Fig. 9 shows the simulated effective load impedances based on 3D EM. The beauty of this result is that \( k_2 \in (0,1) \) is always true, which aligns with the physical meaning of \( k_2 \). Using the solved \( k_2 \), we calculate

\[
C_2 = \frac{1}{\omega Z_{0, HP_{aux}}} = \frac{n_2^2}{\omega (1-k_2^2) Z_{0, HP_{aux}}} = \frac{n_2^2 (1-k_2^2)}{\omega n_2 k_2 \sqrt{2R_{op}R_L}}. \tag{23}
\]

and

\[
C_4 = \left(\frac{k_2}{n_2}\right)^2 C_1. \tag{24}
\]

In summary, for given load-pull impedance \( R_{op}, n_1, k_1, \) and \( n_2 \), all the design parameters in the introduced transformer-based Doherty power combiner can be calculated, as (13)-(15), (19), (20), (22)-(24).

Fig. 8 shows our implemented transformer-based Doherty power combiner. It occupies a two-transformer footprint, which is very compact. Fig. 9 shows the simulated effective load impedances seen by the main and auxiliary PAs. The real parts achieve true Doherty load modulation, and the imaginary parts are tuned out for both PAs without using any extra passive matching networks or switches. Fig. 10 compares the simulated passive efficiency and bandwidth of our transformer-based Doherty power combiner with the conventional two-\( \lambda \)/4-line-based design. We observe substantial passive efficiency improvement in PBO and bandwidth enhancement for the introduced Doherty power combiner.

III. POWER-DEPENDENT DOHERTY PA UNEVEN-FEEDING SCHEME

The introduced transformer-based low-loss and broadband Doherty power combiner addresses the challenge on the passive
design in integrated Doherty PAs. On the active side, a two-way Doherty PA demands careful cooperation between the main and auxiliary PAs to ensure the efficiency and linearity. To address this challenge, we introduce a power-dependent Doherty PA uneven-feeding scheme [60].

Fig. 2b shows the desired current relationship between the main and auxiliary PAs in the ideal Doherty operation. The auxiliary PA should be off in the low-power region, and after it is turned on in the high-power region, its current need to increase rapidly. To achieve the late turning-on of the auxiliary PA, the analog Doherty PA often biases the auxiliary PA in class-C and the main PA in class-AB. To achieve the rapidly increasing current from the auxiliary PA, the conventional analog Doherty PA often adopts dynamic biasing that provides higher biasing levels for the auxiliary PA as the PA input power ($P_{in}$) increases [65]. However, the dynamic biasing circuit is loaded by the large power cells, and it need to track the envelope, which has three to five times bandwidth expansion on top of the input modulated signal. As a result, conventional Doherty PAs using the dynamic biasing technique entail challenges for broadband 5G applications.

Our introduced power-dependent Doherty PA uneven-feeding scheme facilitates the rapid increase of the auxiliary PA current and achieves enhanced Doherty operation without hardware overhead or bandwidth sacrifice. Fundamentally, the introduced scheme leverages the different $P_{in}$ dependences of the input impedances in the differently biased main and auxiliary PAs using bipolar transistors. When the PA $P_{in}$ increases, the class-C-biased auxiliary PA is gradually turned on, and its effective transconductance increases. As a result, its input conductance increases significantly (dashed green line in Fig. 11). On the other hand, the input impedance of the class-AB-biased main PA remain almost the same when the PA $P_{in}$ changes (dashed red line in Fig. 11). We introduce a “driver-PA co-design” method that leverages the different $P_{in}$ dependences and creates adaptive uneven feeding for the main and auxiliary PA final stages (Fig. 11). The main and auxiliary drivers share the same biasing, and the blue curves in Fig. 11 show their power-gain load-pull contours. Solid red and green lines in Fig. 11 show the load impedances seen by the main and auxiliary drivers, respectively, which are transformed from the input impedances of the main and auxiliary PAs by the inter-stage matching networks. When the $P_{in}$ increases, the load impedance trajectory of the auxiliary driver travels from the low-power-gain region to the high-power-gain region, while the load impedance trajectory of the main driver almost stays on a constant power-gain circle. As a result, the auxiliary PA final stage is fed by an expanding $P_{in}$ that generates its rapidly increasing output current in the high-power region. Existing uneven-feeding techniques achieve uneven power division at the Doherty input, which is coupled with the input matching and limits the design freedom [82]-[85]. We achieve power-dependent adaptive uneven feeding by the introduced “driver-PA co-design” method without hardware overhead and sacrificing modulation bandwidth.

IV. EXPERIMENTAL RESULTS

A. PA Implementation

For the proof of concept, we implement a 28/37/39-GHz multiband Doherty PA for broadband 5G applications (Fig. 12). It is prototyped in a GlobalFoundries 130-nm SiGe BiCMOS process and occupies 1.8mm$^2$ (Fig. 13).

The input signal is first processed by an on-chip transformer-based differential quadrature hybrid [86], which splits the input power and performs 90° phase shifts. The quadrature hybrid is loaded by nine-section varactor-loaded transmission lines. The
varactor control voltages in the main and auxiliary paths can be independently tuned, which adjusts the relative phase between the two paths and extends the carrier bandwidth of a Doherty PA [55], [87]. Our design uses one varactor setting for 28GHz and the other varactor setting for 37/39GHz (Table I). The varactor-loaded transmission lines also form high-order loads for the quadrature hybrid, which ensures wideband input matching for different varactor settings.

The PA is comprised of two stages. Both stages adopt the neutralization technique that enhances the power gain and stability [19]. The driver stage is connected to the varactor-loaded transmission lines with transformer-based matching. The inter-stage matching between the driver and PA final stage is designed to achieve the introduced power-dependent uneven-feeding scheme.

B. Measurement Results

1) Continuous-Wave (CW) Measurement

The PA is first characterized using CW signals. Fig. 14 and Fig. 15 show the measured small-signal S-parameters and large-signal saturated $P_{out}$ ($P_{sat}$) and $P_{1dB}$, which demonstrate broadband performance. The small-signal $S_{21}$ achieves a $-3$-dB bandwidth of 23.3-39.7GHz (52% fractional bandwidth). The $-1$-dB $P_{sat}$ bandwidth covers 28 to 42GHz (40% fractional bandwidth).

Fig. 16 shows measured PBO performance. At 37GHz, this PA achieves $+17.1$-dBm $P_{sat}$, $+15.5$-dBm $P_{1dB}$, 27.6% peak collector efficiency (CE), and 22.6% peak power added efficiency (PAE). Compared with a normalized class-B/class-A PA, the Doherty operation achieves 1.92/3.86 times efficiency enhancement at 6-dB PBO. The PA also demonstrates excellent amplitude and phase linearity at 37GHz. The AM-PM is 1.3° from the small signal to $P_{1dB}$. Without changing the varactor controls, the PA achieves $+17$-dBm $P_{sat}$, $+15.4$-dBm $P_{1dB}$, 28.2% peak CE, and 21.4% peak PAE at 39GHz. The Doherty efficiency enhancement at 6.7-dB PBO is 1.62/3.51 times over the class-B/class-A operation. After changing the band setting by reconfiguring the varactor controls (Table I), the PA
achieves +16.8-dBm Psat, +15.2-dBm P1dB, 29.4% peak CE, and 20.3% peak PAE at 28GHz. The Doherty efficiency enhancement at 5.9-dB PBO is 1.72/3.39 times over the class-B/class-A operation. Owing to the introduced Doherty power combiner and adaptive uneven feeding scheme, the PA achieves superior PBO efficiency improvement in all the three 5G bands.

2) Modulation Measurement

The PA is then characterized using modulated signals. In the measurements, we calibrate out the non-ideal effects due to cables, off-chip components, and instruments in the setup via the equalization function in the vector signal analysis (VSA) software [88]. The coefficients of the equalization filter are determined by the through tests without our PA.

Fig. 17 shows the measurement results using 500M-Sym/s 64QAM (3Gb/s). In the 37/39/28-GHz 5G bands, the PA delivers +9.5/+9.3/+9.2-dBm average P_{out}, 19.2/17.2/18.5% average CE, −30.3/−28.7/−27-dB rms error vector magnitude (EVM), and −28.2/−29.8/−28.4-dBc adjacent channel power ratio (ACPR). Fig. 18 shows the measurement results using 1G-Sym/s 64QAM (6Gb/s) at 28GHz. The PA achieves +7.2-dBm average P_{out}, −26.6-dB rms EVM, and −25.4-dBc ACPR. These measurements verify the multiband linear Doherty performance in high-speed dynamic operations.

Table II summarizes the performance of our PA and makes comparisons with state-of-the-art mm-wave PAs in silicon.

Fig. 16. Measured PBO performance at 28GHz, 37GHz, and 39GHz.

Fig. 17. Measurement results for 500M-Sym/s 64QAM (3Gb/s) at 28GHz, 37GHz, and 39GHz.
V. CONCLUSION

We present the first multiband mm-wave linear Doherty PA in silicon for 5G applications. To address the unmet challenges in conventional designs, we introduce a transformer-based low-loss and broadband on-chip Doherty power combiner and a power-dependent Doherty PA uneven-feeding scheme based on a “driver-PA co-design” method. Our prototype demonstrates multi-Gb/s data rates in three mm-wave 5G bands with excellent efficiency and linearity. Our PA advances the state of the art for Doherty, wideband, and 5G silicon PAs in mm-wave bands. Moreover, our PA allows the drop-in upgrade for current PAs in existing mm-wave systems and opens doors to compact system solutions for future multiband 5G massive MIMO and phased-array platforms.

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Table II

| Technology     | 130nm SiGe | 45nm SOI CMOS | 40nm CMOS | 28nm CMOS | 130nm SiGe | 28nm CMOS | 28nm CMOS | 180nm SiGe |
|----------------|------------|---------------|-----------|-----------|------------|-----------|-----------|------------|
| Architecture   | Multiband Doherty | Slow-wave CPW Doherty | Inductively coupled resonator | Asymmetric combiner | Class-AB with AM-PM compensation | Inductive source degeneration | Four-way power combined |
| Power gain (dB) | 20.2 | 21.0 | 23.2 | 16.9 | 18.4 | 14.2 | 12.8 | 12.8 |
| Efficiency (%)  | 46.6 | 48.1 | 49.6 | 41.3 | 45.9 | 35.1 | 35.5 | 35.5 |
| Modulation      | 64-Gb/s | 64-Gb/s | 64-Gb/s | 64-Gb/s | 64-Gb/s | 64-Gb/s | 64-Gb/s | 64-Gb/s |
|                | 12.8-Gb/s | 12.8-Gb/s | 12.8-Gb/s | 12.8-Gb/s | 12.8-Gb/s | 12.8-Gb/s | 12.8-Gb/s | 12.8-Gb/s |
|                | 25.6-Gb/s | 25.6-Gb/s | 25.6-Gb/s | 25.6-Gb/s | 25.6-Gb/s | 25.6-Gb/s | 25.6-Gb/s | 25.6-Gb/s |
|                | 7.2-Gb/s  | 7.2-Gb/s  | 7.2-Gb/s  | 7.2-Gb/s  | 7.2-Gb/s  | 7.2-Gb/s  | 7.2-Gb/s  | 7.2-Gb/s  |
|                | 4.2-Gb/s  | 4.2-Gb/s  | 4.2-Gb/s  | 4.2-Gb/s  | 4.2-Gb/s  | 4.2-Gb/s  | 4.2-Gb/s  | 4.2-Gb/s  |
|                | 2.4-Gb/s  | 2.4-Gb/s  | 2.4-Gb/s  | 2.4-Gb/s  | 2.4-Gb/s  | 2.4-Gb/s  | 2.4-Gb/s  | 2.4-Gb/s  |
|                | 1.2-Gb/s  | 1.2-Gb/s  | 1.2-Gb/s  | 1.2-Gb/s  | 1.2-Gb/s  | 1.2-Gb/s  | 1.2-Gb/s  | 1.2-Gb/s  |
|                | 0.6-Gb/s  | 0.6-Gb/s  | 0.6-Gb/s  | 0.6-Gb/s  | 0.6-Gb/s  | 0.6-Gb/s  | 0.6-Gb/s  | 0.6-Gb/s  |
|                | 0.3-Gb/s  | 0.3-Gb/s  | 0.3-Gb/s  | 0.3-Gb/s  | 0.3-Gb/s  | 0.3-Gb/s  | 0.3-Gb/s  | 0.3-Gb/s  |
|                | 0.1-Gb/s  | 0.1-Gb/s  | 0.1-Gb/s  | 0.1-Gb/s  | 0.1-Gb/s  | 0.1-Gb/s  | 0.1-Gb/s  | 0.1-Gb/s  |

* Read from the reported figures. ** Without pads. † Statically tuned biasing.
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