A SiGe 3-stage LNA for automotive radar application from 76 to 81 GHz

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Abstract. This paper presents the simulation results of the W-band 3-stage low noise amplifier which is designed in 0.13 μm SiGe BiCMOS technology. The LNA achieves a peak $S_{21}$ of 24.1 dB and noise figure of 6 dB at 80 GHz with 3 dB bandwidth of 14 GHz from 73 to 87 GHz. $S_{11}$ is better than 11 dB. The simulated input 1 dB compression point is −23 dBm at 80 GHz with low power consumption of 26 mW from 1.2 V voltage supply. Layout area is 0.36 mm².

1 Introduction

Low noise amplifier (LNA) is the key element of the receiving path of any transceiver. The function of the LNA is pre-amplification of weak signals induced in the antenna without significantly degrading the signal-to-noise ratio. W-band LNAs are used in radars for various purposes (76-77 GHz long range automotive radars for adaptive cruise control and collision avoidance, 77-81 GHz short range parking radars [1], radars for non-contact level measurement [2], etc.), as well as in high speed wireless communication links with data rates up to 80 Gbit/s [3].

An important condition for the development of W-band systems is the emergence of electronic components and devices with acceptable parameters and cost. This paper presents the simulation results of the W-band LNA for radar application from 76 to 81 GHz which is designed in 0.13 μm SiGe BiCMOS technology process with current-gain cutoff frequency/maximum oscillation frequency ($f_T/f_{max}$) of 300/500 GHz.

2 Amplifier design

Fig. 1 shows a detailed schematic diagram of W-band low noise amplifier with device parameters, supply and bias voltages. The LNA consists of 3-stage using cascode topology to reduce the influence of the Miller effect and obtain high gain.

The technique described in [4] was used for the simultaneous optimal matching of noise and input impedance. All transistors biased at current density that minimizes noise figure (NF). Transistor sizes are selected such that the real part of the optimum noise impedance is approximately equal to the source impedance at the 80 GHz. To obtain the maximum power transfer the LNA input impedance is matched to the source impedance (50 Ω). Microstrip

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transmission lines (TL) in combination with integrated MIM capacitors are used as matching elements. TL are based on microstrip geometry (top and bottom metal layers). The sizes of TLs are summarized in Table 1.

The supply voltage is 1.2-1.8 V while the base voltage of transistors Q1, Q3, Q5 is 0.9 V which leads to the collector currents of about 7-8 mA. According to simulation, obtained current density is optimal for achieving low NF and high gain.

Fig. 1. Schematic of the 3-stage cascode LNA.

| Microstrip TL | Length ($\mu$m) | Width ($\mu$m) |
|---------------|----------------|---------------|
| TL1           | 70             | 7             |
| TL2, TL6, TL10| 40             | 15            |
| TL3, TL7, TL11| 85             | 15            |
| TL4, TL8, TL12| 30             | 15            |
| TL5, TL9, TL13| 90             | 7             |

The layout of the mm-wave LNA is shown in Fig. 2. It occupies 740×480 $\mu$m (0.36 mm$^2$) with pads and 563×308 $\mu$m (0.17 mm$^2$) without pads. Contact pads have dimensions of 80×80 $\mu$m. Distance between their centers is 150 $\mu$m (standart probe station pitch). Input and output RF pads were custom designed with the dimensions 53.33×80 $\mu$m to reduce parasitic capacitances, and also the edges were trimmed to further decrease the parasitic capacitance.

Fig. 2. Full layout of the 3-stage cascode LNA.
3 Simulation results

In the W-band, the pads capacitance and package parasitic elements cannot be neglected in the simulation process. The paper [5] presents the results of measurements of flip-chip ball grid array (FCBGA) package parasitic resistances, capacitances and inductances. Using this data and equivalent circuit for FCBGA-package interconnect effects from [6], a virtual test bench was designed for more correct LNA simulation.

The simulated $S_{21}$ and $S_{11}$ versus frequency at different supply voltages are shown in Fig. 3. The LNA at standard 1.2 V has a peak gain of 24.1 dB at 81 GHz with 3 dB bandwidth (BW) of 73-87 GHz. The $S_{11}$ is less than $-10$ for 70-110 GHz. The simulated $S_{22}$ (not shown) is less than $-7$ dB at 3 dB BW. At supply voltage 1.8 V parameters change slightly (3 dB BW expands to 16 GHz, $S_{21} > 20.5$ dB, $S_{11} < -9.5$ dB).

![Graph showing $S_{21}$ and $S_{11}$](image)

**Fig. 3.** Simulated $S_{21}$ (a) and $S_{11}$ (b) at different supply voltages.

Fig. 4 shows the simulated NF versus frequency characteristic at different temperatures (−40 °C, 27 °C and 125 °C) and supply voltages (1.2 V and 1.8 V). The LNA achieves NF of 5.5-6.6 dB for frequencies 73-87 GHz at standard 1.2 V and 27 °C. As the temperature rises, the noise figure increases as expected, but remains below 10 dB at 125 °C and 1.8 V. The amplifier demonstrates minimum NF of 3.6 dB at 73 GHz and −40 °C.

The minimum achievable noise figure ($NF_{min}$) is less than NF on average by 0.5 dB at 27 °C (not shown).

Fig. 5 shows the simulated input 1 dB compression point ($IP_{1dB}$) versus frequency from 73 to 87 GHz at 1.2 V and 1.8 V supply voltages. $IP_{1dB}$ is more than $-23.7$ dBm.
Table 2 compares the simulated LNA with other CMOS and BiCMOS amplifiers at similar operating frequencies. As in [7-10], a figure of merit (FoM) was applied to for evaluating the performance of wideband LNAs. FoM takes the main LNA parameters and defined as

$$FoM = \frac{S_{21} \cdot BW}{(F-1) \cdot P_{DC}},$$  \hspace{1cm} (1)
where $S_{21}$ is the average power gain in magnitude; $BW$ is the 3-dB bandwidth in GHz; $F$ is the noise figure in magnitude, and $P_{DC}$ is the power consumption in mW.

**Table 2.** Summary of the simulated W-band LNA and comparison to state-of-the-art mm-wave LNAs.

| Year | 2010 [11] | 2012 [12] | 2015 [13] | 2018 [14] | 2019 [This work]|
|------|-----------|-----------|-----------|-----------|-----------------|
| Technology | 0.18 $\mu$m SiGe BiCMOS | 0.25 $\mu$m SiGe-C BiCMOS | 65 nm CMOS | 45 nm CMOS SOI | 0.13 $\mu$m SiGe BiCMOS |
| 3-dB BW (GHz) | 14.5 (69-83.5) | 12 (66-78) | 15 (69-84) | 16 (80-96) | 14 (73-87) |
| $S_{21}$ (dB) | 13.1-14.5 | 21.3-23 | 11-13.1 | 10-12 | 21.1-24.1 |
| $S_{11}$ (dB) | $<-8$ | $<-5$ | $<-10$ | $<-7$ | $<-11$ |
| NF (dB) | 6.9 | 7.6-8.4 | 7-7.2 | 4.2-5.6 | 5.5-6.6 |
| $IP_{1dB}$ (dBm) | $-11.4$ | $-18$ | $-16$ | $-21$ | $-23$ (80 GHz) |
| $P_{DC}$ (mW) | 37 | 40 | 24 | 4.7 | 26 |
| Area (mm$^2$) | 0.41 | 0.79 | 0.17 | 0.42 | 0.36 |
| $FoM$ (GHz/mW) | 0.49 | 0.73 | 0.7 | 2.01 | 1.07 |

*Simulation results

**4 Conclusion**

The W-band 3-stage cascode low noise amplifier using 0.13 $\mu$m SiGe BiCMOS process with $f_T/f_{max}$ of 300/500 GHz is presented in this paper. The LNA has a high $S_{21}$ of $>21$ dB, NF of 5.5 to 6.6 dB in 3-dB BW of 14 GHz. The $S_{11}$ is lower than $-10$ dB from 70 to 110 GHz. The simulated input $IP_{1dB}$ is $-23$ dBm at 80 GHz. The supply voltage and power consumption are 1.2 V and 26 mW, respectively. The layout area is 0.36 mm$^2$ with all of the contact pads and 0.17 mm$^2$ without pads.

The amplifier is expected to integrate in the front-end transceiver of single-chip automotive 77-81 GHz short range radar.

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