dCSR: A Memory-Efficient Sparse Matrix Representation for Parallel Neural Network Inference

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Abstract—Reducing the memory footprint of neural networks is a crucial prerequisite for deploying them in small and low-cost embedded devices. Network parameters can often be reduced significantly through pruning. We discuss how to best represent the indexing overhead of sparse networks for the coming generation of Single Instruction, Multiple Data (SIMD)-capable microcontrollers. From this, we develop Delta-Compressed Storage Row (dCSR), a storage format for sparse matrices that allows for both low overhead storage and fast inference on embedded systems with wide SIMD units. We demonstrate our method on an ARM Cortex-M55 MCU prototype with M-Profile embedded systems. We show that our method achieves competitive performance on an ARM Cortex-M55 MCU prototype with M-Profile embedded systems, compression ratios and increases throughput over dense methods by up to 2.9× for sparse matrix-vector multiplication (SpMV)-based kernels and 1.06× for sparse matrix-matrix multiplication (SpMM). This is accomplished through handling the generation of index information directly in the SIMD unit, leading to an increase in effective memory bandwidth.

Index Terms—pruning, sparse neural networks, simd, embedded systems, compression

I. INTRODUCTION

With neural network (NN) applications moving closer and closer to the edge, ever smaller devices and faster running them. Use cases like wakeword detection [1] or the processing of sensor data [2] have sparked a growing interest in very small NNs, run on deeply embedded systems, often as one task among others. On these devices, memory consumption is a major concern. Memory consumption drives implementation cost through chip area that has to be dedicated to it. It also strongly impacts power consumption, since it is memory transactions—rather than compute operations—that drive the power demand of an embedded application [3]. These reasons make the memory usage of models a major concern when deploying NNs on embedded systems. At the same time, the increasing availability of advanced Single Instruction, Multiple Data (SIMD) capabilities on small devices [4], [5] allows for much faster, parallel computation and widens the memory-performance gap [6] along with the disparity between overall available compute and memory capacity in the system.

While a reduction of model parameters can often be achieved through architectures that are highly specialized for a certain task [7], pruning of weights in existing models might offer a more accessible alternative for reducing parameter counts. Different from dedicated architectures, pruning is applicable to a wide range of models without expert knowledge and orthogonal to other common techniques like quantization [8]. The use of unstructured pruning, however, is often discouraged because the induced sparsity cannot be easily exploited for gains in memory consumption or throughput. A storage scheme that aims to eliminate the zero values in the pruned network requires additional indexing information to regenerate the position of each non-zero element in a layer’s weight matrix. This added overhead can easily outweigh the underlying data and impose a significant memory penalty for pruned networks [9].

While improving the throughput of sparse matrix calculations has long been an area of active research [10], there is less work on reducing their memory consumption. Many of the techniques developed for computation on sparse networks target desktop-class processors or hardware accelerators. To the best of our knowledge, there are no solutions that target embedded processors with parallel Instruction Set Architectures (ISAs).

In this work, we therefore propose Delta-Compressed Storage Row (dCSR). With dCSR, we create a lightweight solution that enables low-overhead storage of sparse NN layers with minimal effort required for extracting the sparse index structure. To achieve this, dCSR utilizes embedded SIMD instructions in order to parallelize index generation as well as sparse inference. Different to prior work [11]–[13], dCSR is a pure software implementation and does not rely on additional hardware, significantly lowering the effort required to implement it in a real-world application. Similar to many
compression schemes, groups of index elements in dCSR can be of varying bitwidth. dCSR differs in that it makes sure that each part of the representation is byte-aligned in memory.

Our contributions are:

- A detailed analysis of the distinct features of embedded hardware for NN inference and the impact of pruning on a set of NN architectures when deployed.
- A matrix encoding that enables pruning as a means of lowering network parameter counts. We reduce NN size by up to 74% while at the same time yielding a speedup of up to 2.96 over dense inference for certain layer types in our evaluation. This is achieved through a unique balance of a low memory footprint and fast extraction.

II. BACKGROUND

A. Compressed Storage Row

The most widely used format to encode sparse matrices is the Compressed Storage Row (CSR) format. CSR uses three arrays to represent a sparse matrix as shown in Fig. 1: the values array contains the non-zero values of the matrix in a contiguous array. The col_idx array holds the column index of each non-zero value. Lastly, the row_ptr array contains the start index of each row in the values and col_idx array. Note that the per-element size in the column index array is determined by the number of columns, while the magnitude of the row pointers is upper-bounded by the number of non-zero values. A variant of CSR is Block Compressed Storage Row (BCSR), in which non-zero blocks of fixed size are stored instead of single values. This increases storage overhead because not all zero elements can be eliminated. The format is sometimes preferred because it can speed up calculations, particularly for matrices with an inherent structure.

B. Relative Indexing

A method to reduce the overhead of CSR and its derivatives that is commonly seen in sparse network accelerators is the encoding of the distance between two adjacent non-zero elements, rather than their absolute column indices. Particularly for the sparsities seen in NN weight matrices, which are typically much lower than in scientific sparse matrix applications, Relative Indexing yields a significant saving in memory. In this representation, each column index difference is represented in a fixed number of bits. If there are gaps that are too large to be encoded in this fixed size, a padding value of zero is inserted in them.

C. General-Purpose Compression

Another way of reducing the memory footprint of sparse networks that sees some use in practical scenarios is simply applying a generic data compression algorithm after pruning when deploying it over a low-bandwidth channel. Because of the large number of zeroes, the sparse network can achieve higher compression ratios than its dense counterpart. After transmission, the network is extracted on the device, and inference is run the same as on a dense network. Deflate, the most widely used general-purpose data compression algorithm consists of two stages. The LZSS stage initially identifies repeated sequences of symbols and replaces each repetition with a backward reference to the first occurrence of the sequence. The Huffman coding stage then assigns symbols of different bitwidth to symbols in the uncompressed input, depending on their frequency. In Huffman coding is used to further increase the compression ratio of a sparse network.

III. METHODS

Relative Indexing already targets encoding of sparse matrices for memory-constrained systems. It is a robust and simple method that can achieve good compression ratios. However, we identify two shortcomings that make it hard to use outside of dedicated hardware.

a) Inter-element dependency: To calculate the column index of an element, the cumulative sum of all previous relative indices in the same row needs to be known. While this is not a problem in purpose-built hardware and for floating-point inference, it becomes an issue for quantized inference on embedded systems. To understand why that is, we need to look at one of the peculiarities of quantized networks: the different sizes of accumulator register and weights/activation values. Different sizes are required because products of weights and activations can be expected to overflow the bounds of their base type. This seemingly small detail has a large impact on the iteration order: for quantized inference, iteration needs to be done horizontally, rather than vertically. Because SIMD units for quantized operation accumulate over several multiplication results at once, they process adjacent weight-activation pairs within one row in parallel. In contrast, GPUs and desktop CPUs typically process multiple adjacent rows in parallel, one column at a time. This makes the ability to recover the indices of adjacent elements in one row in parallel highly important for good utilization of parallel hardware in an embedded context.

b) Computational Overhead: For higher sparsities, the amount of padding inserted by the Relative Indexing Algorithm will grow. Even when assuming a perfect decoding stage, this directly translates into degraded throughput because each padding element also causes a multiplication with zero and a memory access into the activations during inference.

Other idiosyncrasies of quantized inference on embedded SIMD units that make a large number of common optimization techniques developed for desktop applications intractable are the re-quantization from 32-bit to 8-bit of values after inference and the format of scatter/gather instructions for 8-bit elements. For ARM M-Profile Vector Extension (MVE),
currently the most mature embedded SIMD ISA (the RISC-V Vector Extension still has “draft” status at the time of writing), these instructions only handle unsigned 8-bit offset values. The first means that the cost for well-established performance optimizations like loop tiling and every other technique that relies on the output array for intermediate storage [19] would be vastly increased through repeated quantizations and re-quantizations of intermediate results. The second implies that storing absolute indices of array elements like it is done in CSR is detrimental to performance if the number of columns may exceed 256. Indices need to be decomposed into a per-element offset that must not exceed the range \([0, 255]\) and an adjusted array base pointer that is passed to the scatter/gather instruction. CSR would require such a decomposition at runtime for every index element, creating significant overhead for index generation.

We address these points with a combination of two different techniques. One is Delta-Linear Encoding (DLE), an encoding scheme that ensures that per-element values are kept small for reduced storage overhead and independent of each other for parallel computation. The second method is Dynamic Bitwidth Extension (DBE), a decomposition of elements that allows for per-element values to be of varying bitwidth and still retain proper memory alignment.

A. Delta-Linear Encoding

While the row index array in CSR only grows with \(O(n)\) of the matrix dimensions, the column indices array grows quadratically. In practice, this means that the main emphasis of optimizing for low memory consumption should be put on reducing the size of the column indices array. As stated above, there must not be a dependency between adjacent elements in the index calculation. In order to achieve this, we first predict an elements index using a linear mapping of its position in the column indices array and only store the deviation (the delta value) from that prediction.

Assume a column index \(c_i\) that is stored at position \(i\) in the column indices array. We decompose \(c_i\) into a mapping function \(f(i)\) and the deviation from it: \(\Delta c_i = c_i - f(i)\). While sparse matrices with an inherent structure might require different choices for \(f(i)\), we find that for the low-magnitude pruning scheme used, weights do not seem to be concentrated in certain areas of the weight matrix. Instead, they exhibit a uniformly random pattern. This makes a linear mapping \(f(i) = i \cdot m + n\) a sensible default. We can derive the slope of this linear function as the average distance between two adjacent elements from the number of non-zero elements in the row of the sparse matrix \(k_s\) and the row length of the dense matrix \(k_d\). This gives us a slope of \(m = \lfloor k_d/k_s \rfloor\) that will produce relatively small deviations of values for \(\Delta c_i\) within one row. The slope is rounded to the nearest integer to enable integer-only runtime calculations.

For practical applications, we group several consecutive delta elements into SIMD runs \(S_j\) of length \(g\). This gives us the group-wise linear mapping function

\[
c_i = \left\lfloor \frac{k_d}{k_s} \right\rfloor (i \mod g) + \Delta c_i
\]

In this representation, only the \(\Delta c_i\) part contains information that needs to be stored explicitly, while the first part of the equation can be inferred at runtime. For each SIMD group \(S_j = \{\Delta c_i, \Delta c_{i+1}, \ldots, \Delta c_{i+g-1}\}\) will be kept. To make sure that each element within the SIMD unit is unsigned and minimize the numerical value of delta values within a group at the same time, we assign a group-wise y-axis intercept \(n_j\):

\[
n_j = \min S_j
\]

which we can remove from the per-element values

\[
S'_j = \{\Delta c_i - n_j, \Delta c_{i+1} - n_j, \ldots, \Delta c_{i+g-1} - n_j\}
\]

At runtime, \(n_j\) now describes the base pointer for the group. The offset and base pointer of an element \(c_{i,j}\) in lane \(i\) of SIMD group \(j\) can be reconstructed as

\[
c_{i,j} = i \cdot \left\lfloor \frac{k_d}{k_s} \right\rfloor + \Delta c_{i,j} + n_j
\]

Subtracting the minimum from \(S'_j\) brings all delta elements within \(S'_j\) into the range \([0, \max S_j - \min S_j]\), ensuring that only the minimal number of bits is required to encode them. To reduce the memory footprint for each group further, we apply the same linear decomposition that we did above for elements in groups to the base pointer delta values \(n_j\). The aim is to not encode the average distance between two groups explicitly as it is redundant and usually large. The average distance between two groups is the number of elements in the group multiplied by the average distance between them \(g \cdot \lfloor k_d/k_s \rfloor\). The y-axis intercept can be omitted as long as matrix density is not highly irregular. To reconstruct \(n_j\) with zero-based indexing, the calculation of \(n_j\) can be expressed as

\[
n_j = j \cdot \left\lfloor \frac{k_d}{k_s} \right\rfloor \cdot g + \Delta n_j
\]

Alternatively, \(n_j\) can be stored incrementally, similar to the encoding of column indices in Relative Indexing.

\[
n_j = \begin{cases} 
\Delta n_j & \text{for } j = 0 \\
 n_{j-1} + \left\lfloor k_d/k_s \right\rfloor \cdot g + \Delta n_j & \text{otherwise}
\end{cases}
\]

In both cases, \(\Delta n_j\) is the only part of the equation that needs to be put into memory. We find that the latter encoding produces a more even distribution of values with lower magnitude in our evaluation, although at the cost of introducing an interdependence between groups. The process of deriving a base pointer and per-element offsets from the delta representation is shown in Fig. 2.

Some boundary conditions need to be ensured. The calculation of per-element offset values must not overflow the bounds given by the width of the SIMD lane. In addition, \(\Delta n_j\) also must not overflow its base type (an 8-bit signed integer in our implementation). We insert padding to ensure that all of these
conditions hold. To do this, we employ a greedy algorithm that in each iteration inserts a zero value into the middle of the largest gap in the row until no overflow occurs.

B. Dynamic Bitwidth Extension

While DLE reduces the size of column index elements within a group, it can only guarantee the upper bound for these values that was achieved during the padding insertion. Simply encoding every column index’ delta value using the size of this upper bound would be too wasteful for many memory-constrained applications. Lower bitwidths that are not an even divisor of the machine word size (like five, six or seven bit) on the other hand cannot directly be represented in memory in a way that makes it easy to load them in parallel at runtime. Having the greatest element of a row determine the bitwidth for all other elements in a row also means that a single outlier value might lead to a lot of wasted memory when other elements would be representable with fewer bits.

To address these issues, we decompose each group of delta elements into a base value with a fixed number of bits as well as several groups of extension bitmasks as shown in Fig. 3. Every bitmask contains one bit per SIMD lane that marks whether or not the bit is set in the encoded value. Masks that would be all-zero are not created. The extension bits can dynamically be added to the base value at runtime if more bits than available in the base value are required. The decomposition is done separately for each SIMD run. Through this, each SIMD run can be encoded in the number of bits required for the largest element in this run, reducing the impact of rare outlier values to a single SIMD group rather than an entire row. The size of the mask is determined by the number of SIMD lanes which can be expected to be a power of two; the extension bitmasks do not cause issues with memory alignment because of this. Because the number of extension bitmasks is not fixed per group, we need to be able to infer how many of them need to be consumed for a given group at runtime. Each group maintains a tracking bitmap for this purpose. This tracking bitmap has one bit for every bit position that might be extended. If the bit is set to one, there exists a bitmask for this position that needs to be consumed at runtime; if it is set to zero, there is no bitmask for this position.

For our implementation, we choose a base value size of four bits, with bits five, six and seven being extensible. A fixed-size base value is not strictly necessary for the algorithm, as any integer could also fully be decomposed into only a set of extension bitmasks. We introduce the base values because the re-composition at runtime incurs some overhead. It therefore makes sense to only dynamically add bit positions that have a high likelihood of not being present in a significant number of groups; for the lowest four bits, we find that this is not the case which is why they are always stored as-is. To make the 4-bit base values easily accessible in memory, we interleave two adjacent groups so that the base values of the first group occupy the upper nibble, while the base values of the second group occupy the lower nibble as shown in Fig. 4. The benefit of this scheme is that when executing a parallel load, each base value is loaded into the correct SIMD lane. Accessing the values for either group can be done through a single parallel shift or bitwise-or operation. The bitmasks occupy a multiple of a byte and are stored contiguously without interleaving.

We show the inverse process of combining tracking bitmap, extension bitmasks and base values into delta values in Fig. 5. When recomposing the original value at runtime, we iterate over all extensible bit positions. If the corresponding bit is not set in the tracking bitmap the iteration is complete and we continue with the next position. If the bit is set we load the next bitmask from memory and advance the mask pointer. We then do a parallel bitwise-or operation with the current bit position. The mask is used to apply this operation only to the lanes that need to be extended in this group. The binary lane
masking feature that is essential for this is present in ARM MVE as well as the RISC-V Vector Extension.

![Parallel Reconstruction of a group delta values from groupwise interleaved base values, tracking bitmap and extension bitmasks](image)

C. Row Buffering

While the extraction process of indices is lightweight, it is beneficial to reuse intermediate results when possible. In pointwise convolution (PWC) layers, every row of the sparse matrix is multiplied with every column of the activation matrix, allowing for repeated use of the same row of weights once decoded. Keeping element indices in memory once they are generated is therefore an attractive option to reduce the overhead of the extraction process further. Buffering can be carried out in one of two ways.

a) Value Buffering: In Value Buffering (VB) mode, the indices for the current row are generated from the base values, tracking bitmasks and extension bitmasks. Furthermore, the values for the current row are loaded from memory. The indices are then used to scatter the matrix values into the appropriate positions of the zero-initialized row buffer. The row buffer is now the reconstruction of the same row as it would appear in a dense matrix and can be multiplied with the input activation using dense kernels. In this mode, the dCSR kernel is a simple compression/decompression scheme that cannot benefit from the reduced number of effective computations in a sparse matrix by skipping multiplications with zero. In practice, this can be preferable because gather memory accesses are significantly slower than dense and aligned memory accesses on most hardware. The reduced number of operations therefore might only outweigh the slow gather instructions for high sparsities.

b) Index Buffering: When executing in Index Buffering (IB) mode, the indices themselves are recomposed from their DBE representation and written to the row buffer. The base pointer steps are also computed and buffered. The inference kernel then loads the pre-computed base pointers and gather offsets from memory and uses them to load the corresponding activation values using a gather memory access. In this mode, only operations with non-zero weights are carried out at the cost of potentially slower memory accesses.

The size for the row buffer can be upper-bounded to the size of one matrix row ahead of time. IB requires some additional memory for base pointer steps which is upper-bounded by the maximum number of groups in a row. The equilibrium point between the two modes depends on the matrix characteristics as well as the target hardware. For fully-connected (FC) layers, a similar reuse of weights is not possible since each element in the weight matrix is only used exactly once. The FC kernel will therefore always use extracted values directly to generate a gather instruction into the activation memory.

IV. RESULTS AND DISCUSSION

A. Setup

We use the set of depthwise separable convolutional neural networks (DS-CNNs) for keyword spotting from [20] as a reference. For each network architecture, we train a dense base model that is subsequently pruned to increasing levels of sparsity. We deviate from the original architecture by adding Dropout [21] after the input convolution as well as each depthwise separable convolution block to address the overfitting seen in the original publication. We also omit an increased stride for the first depthwise separable block in the larger architectures. All base models are trained for 50 epochs on the Google Speech Commands v2 dataset [22]. The models are trained using an Adam Optimizer with a linear learning rate decay from an initial rate of $5 \cdot 10^{-3}$ to the final learning rate of $1 \cdot 10^{-4}$.

The base network is pruned to sparsities between 70% and 95% in increments of 5% (the term sparsity refers to the percentage of elements that are set to zero here). We prune only the weights of the PWC and FC layers in the network because they account for the majority of the network’s memory footprint. The input convolution as well as the depthwise convolutions and all biases remain dense. The low-magnitude pruning layer from the Tensorflow [23] Model Optimization Toolkit is used to prune each network over 40 epochs followed by 40 epochs of retraining. We show the degradation of accuracy for each model in Fig. 6. By targeting only layers with high parameter counts, we can achieve noticeable reductions in the number of active parameters for these layers without a significant impact on the model’s accuracy.

All training scripts, conversion tools to dCSR and Tensorflow lite (TFlite) micro [24] inference kernels as well as the dense and sparse reference models are made publicly available [25].

![Degradation of accuracy through pruning of PWC and FC layers per DS-CNN architecture. Accuracies reported for floating-point models.](image)
We attribute this effect primarily to the fact that our models were trained on the enlarged version 2 of the dataset with 105k values for the row pointer and column index arrays because it model with lower sparsity. This gap closes increasingly for the large architecture with 90% sparsity. dCSR does not achieve small model and achieves similar results for the medium and indicate that both formats produce significant overhead. Relative quantization of weights to eight bit. Memory footprints are a block size of \(2^{2}\) layers in all surveyed models. For BCSR, we further assume for sparse tensors). For CSR and BCSR, we assume 16-bit matrices, a variant of BCSR is used to encode sparse tensors is the de facto standard for scientific computation on sparse though they are not optimized for low overhead. While CSR techniques. We include CSR and BCSR for reference, even though they are not optimized for low overhead. While CSR is the de facto standard for scientific computation on sparse matrices, a variant of BCSR is used to encode sparse tensors in TFlite (not TFlite micro, where there is currently no support for sparse tensors). For CSR and BCSR, we assume 16-bit values for the row pointer and column index arrays because it is the smallest memory-aligned integer size that can encode all layers in all surveyed models. For BCSR, we further assume a block size of \(2, 2\). Reported compression ratios are after quantization of weights to eight bit. Memory footprints are based on the sizes of a model’s weights and biases and exclude overhead from the TFlite Flatbuffer data structure. The low compression ratios for CSR and BCSR in Fig. 7 indicate that both formats produce significant overhead. Relative Indexing is superior to general-purpose compression for the small model and achieves similar results for the medium and large architecture with 90% sparsity. dCSR does not achieve the same compression ratios as Relative Indexing for the small model with lower sparsity. This gap closes increasingly for the two larger architectures with higher sparsity.

### B. Compression

To assess the memory footprint of dCSR, we compare its overall memory consumption with that of other established techniques. We include CSR and BCSR for reference, even though they are not optimized for low overhead. While CSR is the de facto standard for scientific computation on sparse matrices, a variant of BCSR is used to encode sparse tensors in TFlite (not TFlite micro, where there is currently no support for sparse tensors). For CSR and BCSR, we assume 16-bit values for the row pointer and column index arrays because it is the smallest memory-aligned integer size that can encode all layers in all surveyed models. For BCSR, we further assume a block size of \(2, 2\). Reported compression ratios are after quantization of weights to eight bit. Memory footprints are based on the sizes of a model’s weights and biases and exclude overhead from the TFlite Flatbuffer data structure. The low compression ratios for CSR and BCSR in Fig. 7 indicate that both formats produce significant overhead. Relative Indexing is superior to general-purpose compression for the small model and achieves similar results for the medium and large architecture with 90% sparsity. dCSR does not achieve the same compression ratios as Relative Indexing for the small model with lower sparsity. This gap closes increasingly for the two larger architectures with higher sparsity.

### Table I

| Layer                  | Parameters                                      | S               | M               | L               |
|------------------------|-------------------------------------------------|-----------------|-----------------|-----------------|
| 1 \( \times \) 2D Conv | Channels, Kernel Size, Stride                   | 64, (10,4), (2,2) | 172, (10,4), (2,1) | 276, (10,4), (2,1) |
| \( \rightarrow \) \( n \times \) 2D DSConv | Number of Blocks \( (n) \), Channels, Kernel Size, Stride | 4, 64, (3,3), (1,1) | 4, 172, (3,3), (1,1) | 5, 276, (3,3), (1,1) |
| \( \rightarrow \) 1 \( \times \) 2D AveragePooling | Size                                            | (2,2)           | (2,2)           | (2,2)           |
| \( \rightarrow \) 1 \( \times \) Fully-Connected | Size                                            | (12, 1536)      | (12, 10320)     | (12, 16560)     |

![Figure 7](image_url)

A breakdown of the contributions of metadata, padding elements and active weights to the overall memory footprint of the compressed sparse matrix is given in Table II. Relative Indexing produces lower amounts of metadata per non-zero element, but does so at the cost of inserting a high amount of padding into the values arrays. For the small architecture, the padding overhead of Relative Indexing is 3.6% of the values array, while the medium and large models require the insertion of 21.9% and 25.7% additional zero values. dCSR also inserts padding, but its greedy search results in a much lower amount. The inserted padding of dCSR totals 0% (S), 3.8% (M) and 3.4% (L) additional elements. The larger overhead for dCSR altogether—despite the higher amount of padding inserted for Relative Indexing—can be explained by two things: smaller matrices incur more overhead in dCSR because base indices need to be stored, even for partially filled SIMD groups like we illustrate in Fig. 4. Handling metadata like tracking bitmaps and base pointer delta values facilitate fast execution at runtime, but increase the overhead further. Also, dCSR cannot only limit the effect of outlier values to a group, not individual elements. A single outlier in a SIMD group still causes the creation of extension bitmasks for all the other elements in the group. A strength of dCSR is that it handles matrices with regions of high sparsity better through its flexible encoding of bitwidths, resulting in fewer padding elements being inserted for larger, more sparse matrices.

### C. Embedded SpMM

To analyze the overhead of our algorithm, we demonstrate the extraction and sparse inference as dedicated kernels within the TFlite micro framework. The compression of supported weight tensors inside a TFlite model takes place ahead of time as part of the model conversion. Extraction and inference is implemented in C using ARM MVE intrinsics. We report the
with this optimization in place, dCSR outperforms CMSIS-NN. The difference is a fully adapted version of the CMSIS-NN kernel that adopts an efficient MAC-based calculation of the indices, which reduces the pressure on the system’s memory interface. Despite the increased number of arithmetic instructions, the speedup achieved by value-buffered dCSR over the optimized CMSIS-NN kernel is significant, particularly for the evaluated hardware and sparsities. The speedup achieved by value-buffered dCSR over the optimized CMSIS-NN kernel is largely due to the reduced pressure on the system’s memory interface.

A closer look at the time spent in the extraction stage shows that both implementations of dCSR only require around 50% of the cycles needed by Relative Indexing to restore matrix indices from their representation in memory, with the index-buffered variant requiring 20% to 25% fewer cycles when compared to the value-buffered version due to not having to load weight values from memory. Lossless compression/decompression based on the general-purpose Deflate algorithm does not reach the equilibrium point at which the slow gather memory accesses produce lower overhead compared to a dense kernel for the evaluated hardware and sparsities. The speedup achieved by value-buffered dCSR over the optimized CMSIS-NN kernel despite the increased number of arithmetic instructions is largely due to the reduced pressure on the system’s memory interface.

We find that our index-buffered implementation does not reach the equilibrium point at which the slow gather memory accesses produce lower overhead compared to a dense kernel for the evaluated hardware and sparsities. The speedup achieved by value-buffered dCSR over the optimized CMSIS-NN kernel despite the increased number of arithmetic instructions is largely due to the reduced pressure on the system’s memory interface.
A drawback of large sparse architectures is that they cannot weights of these layers account for the 77.2% and 82.0% of the with higher sparsity. In SpMV, a balance of a fast unpacking consumption compared to their small dense counterparts. This sparse networks offer a better accuracy with lower memory the model’s final accuracy. We compare the memory footprint them will matter most. In addition, we find that pruning early model’s memory footprint after 8-bit quantization, so pruning onward for 80% and 93% sparse networks respectively). The in the network (from the 12th CIFAR-10 task [30] with images scaled up to 96×96px) trained on the Imagenet [29] dataset for classification on the of padding for Relative Indexing further reduces throughput. In contrast to Relative Indexing, dCSR has two other benefits that help in achieving a high throughput. The index offset values already reside in the SIMD unit after calculation; in Relative Indexing, they need to be calculated in the scalar domain and then transferred to the SIMD unit. Secondly, the larger amount of padding for Relative Indexing further reduces throughput.

**E. Case Study: Sparse MobileNetV2**

We apply a similar strategy as above to the MobileNetV2 [28] architecture. We initially tune a dense network that was pre-trained on the ImageNet [29] dataset for classification on the CIFAR-10 task. [30] with images scaled up to 96px × 96px as a baseline (BL). We prune only the last PWC and FC layers in the network (from the 12th and 11th inverted residual block onward for 80% and 93% sparse networks respectively). The weights of these layers account for the 77.2% and 82.0% of the model’s memory footprint after 8-bit quantization, so pruning them will matter most. In addition, we find that pruning early layers with low parameter counts disproportionately reduces the model’s final accuracy. We compare the memory footprint after pruning and encoding of the sparse layers with dCSR to those of dense MobileNetV2 models with a reduced width multiplier in Table [III]. Our evaluation confirms that large sparse networks offer a better accuracy with lower memory consumption compared to their small dense counterparts. This observation is consistent with findings in previous work [9]. A drawback of large sparse architectures is that they cannot profit from reduced arithmetic operations to the same degree that small dense networks can. Sparsity is a vital tool, however, when maximizing accuracy in a given memory envelope.

We compare the speedup in total cycles for both target layer types in Fig. [11]. For the 80% sparse MobileNetV2, the performance of dCSR for PWC is slightly below that of the optimized CMSIS. This is because some of the weight matrices are of irregular shape with many more rows than columns, which incurs the per-row overhead in dCSR more often. Because of the increased sparsity in the 93% sparse model, index-buffered dCSR now yields a significant speedup over other implementations through omitting multiplications with zero. The results for the networks’ FC layer corroborate our findings from the keyword spotting application in that high sparsities result in increased throughput over dense inference for dCSR-encoded matrices.

**V. CONCLUSION**

In this work, we introduced dCSR, a novel sparse matrix representation that helps materialize the benefits of pruning in embedded hardware with SIMD capabilities. We showed that even small NNs might still be over-parameterized and can be pruned to significant sparsities at a marginal loss in accuracy. For a typical embedded NN application, dCSR achieves a reduction in size of 62.6% to 80.8% for the targeted layers and 50.0% to 74.1% for the entire network after quantization. This is complemented by an increase in end-to-end throughput on our target hardware. The speedup is achieved through reduced memory transactions combined with a parallel extraction of indices from their representation in storage through SIMD instructions. Especially for SpMV operations in NNs, which

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**Figure 10. Speedup of FC layer inference over CMSIS-NN**

**Figure 11. Speedup for target layers on sparse MobileNetV2 over CMSIS-NN**

**Table III**

| Sparsity | Width Multiplier | Accuracy [%] | Size [KiB] |
|----------|------------------|--------------|-------------|
| 0%       | 0.5              | 93.89        | 1364.9      |
| 0%       | 0.75             | 94.44        | 2220.3      |
| 80%      | 1.0              | 94.03        | 1127.1      |
| 93%      | 1.0              | 92.69        | 695.7       |

**Sparsity Width Multiplier Accuracy [%] Size [KiB]**

| BL | dCSR | dCSR-VB | CMSIS-NN | Optimized CMSIS-NN |
|----|------|---------|----------|-------------------|
| 0% | 1.0  | 94.44   | 2220.3   |                   |
| 0% | 0.75 | 93.89   | 1364.9   |                   |
| 80%| 1.0  | 94.03   | 1127.1   |                   |
| 93%| 1.0  | 92.69   | 695.7    |                   |
are memory-bound and often account for a large portion of the network weights, our method promises a significant reduction both in size and inference time. Looking at the current trajectory of embedded systems, it seems likely that they will follow the path of desktop systems with compute capacity growing at a more rapid pace than memory, both in speed and availability. The dCSR method shows a way of closing this coming gap for NNs by harnessing the increasing computational potential to reduce memory consumption.

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