A full-duplex transceiver for 20-Gbps high-speed simultaneous bidirectional signaling across global on-chip interconnections

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Abstract
This paper presents a high-speed simultaneous bidirectional transceiver (SBT) for on-chip wireline communications. A MOS hybrid transistor is utilized to split the received data from the superimposed signal at both ends of the on-chip interconnection with the assistance of two drivers, namely main and auxiliary. Moreover, a high-pass filter (HPF) is used as a differentiator to generate the echo cancelation signal. Consequently, the echo-cancelation for simultaneous bidirectional signaling (SBS) is realized by the combination of the hybrid device and the differentiator. The proposed SBT has been designed and evaluated using 28-nm CMOS technology over a narrow 5-mm on-chip interconnection, which possesses 11.9-dB loss at the Nyquist frequency (half a bit rate). The energy-efficiency of the proposed full-duplex transceiver (FDT) for 20-Gbps simultaneous bidirectional data transmission is 0.147 PJ/b/mm. The performance results show that the proposed SBT has better overall performance compared to the previous architectures reported in the literature to date. The layout of the presented SBT occupies a low area of 1574 μm².

KEYWORDS
echo-cancelation, full-duplex, high-speed, low-voltage, on-chip interconnect, transceiver

1 | INTRODUCTION

System on chips (SoC) contains several integrated circuits (IC) and high-speed data transmission between these ICs is a critical issue that affects the performance of a SoC. To provide the required connectivity, the demand for the on-chip global interconnects is increasing. With the continuous downscaling of CMOS technologies, the speed of the VLSI systems has been increased. Although, the on-chip global interconnects have not scaled at the same rate. In other words, the on-chip interconnections have kept in the same length while the width of them can be reduced due to scaling in the cost of increased electrical resistance. Consequently, the RC dominated on-chip interconnects have become a major bottleneck in the realization of systems on a chip using scaled-down technologies.1,2

Some unidirectional signaling schemes have been presented to obtain higher data-rates with better energy-efficiency across on-chip global interconnects3–6 by utilizing different techniques such as data modulation, resistively and
The proposed SBT includes a hybrid transistor \( (M_{\text{hybrid}}) \), the main and the auxiliary drivers, an echo-cancelation (EC) block, and a trans-impedance amplifier (TIA). The hybrid MOS device is used not only to separate the transmitted and received signals from each other at both sides of the on-chip interconnect, but also employs low-impedance capacitive driven solutions, and current-mode signaling.\(^{7–16}\) Besides, some half-duplex signaling solutions have been presented in the literature.\(^{17–20}\) However, the overall bandwidth of the system reduces to half because of the time-sharing between the receiving and the transmitting cycles. The simultaneous bidirectional signaling solution can be used to overcome the time-sharing problem. Therefore, full-duplex transceivers have been reported significantly for off-chip interconnections like cables or transmission lines (TLs) in PCBs.\(^{21–26}\) However, off-chip simultaneous bidirectional transceivers (SBTs) are not appropriate designs for on-chip interconnections due to their high power consumption and behavior difference between the off-chip and on-chip transmission lines.

Lately, SBTs have been presented over on-chip interconnections.\(^{27–33}\) A current-mode SBS for on-chip interconnection is studied in Huang et al.,\(^ {27}\) which has overall poor performance. The authors are presented a current-mode differential SBT in Huang et al.\(^ {28}\) by utilizing an adaptive impedance-matching structure. However, the maximum achievable data rate of 5 Gbps is reported across a 1-mm-short on-chip interconnect. Afterward, a SBS solution has been presented and less than 2-Gbps data rate is attained at the price of increased power consumption.\(^ {29}\)

A hybrid circuit topology has been proposed in.\(^ {30}\) The designers are tried to improve the achievable data-rate by employing a MIMO (eight-parallel interconnects and transceivers) architecture. Nevertheless, a 2 Gb/s/channel data rate can be achieved over a 3-mm-short interconnect. Another detailed analysis of a SBT is provided in Wary and Mandal.\(^ {31}\) This current-mode design employs a directional inverter/buffer (DIB) circuit to reverse the transmitting (outbound) signal whilst it passes the inbound signal with the same phase and a certain amplification. Then, the outbound and the inbound signals are separated from each other by adding two signals with proper ratios on both sides of the DIB by using a transconductor circuit. Nevertheless, a low data-rate of 4 Gbps is obtained. Moreover, authors are used a replica-based transceiver in Wary and Mandal,\(^ {32}\) and hence, 10-Gbps speed is reported.

In this paper, an alternative solution is proposed to overcome the problems in the attainment of high-speed FDTs over the on-chip interconnections and improve the performance of the previously reported SBT in Ebrahimi Jarihani et al.\(^ {33}\) A transistor is utilized as a hybrid device to employ the impedance-matching at both sides of the on-chip interconnection, separating the transmitting and the incoming signals and also carrying out voltage-mode echo cancelation with the assistance of an auxiliary and a main drivers. In addition, using the compensation capacitance \( (C_c) \) in \(^ {33}\) not only creates the similar loading effects in the presented topology for better echo cancelation in voltage-mode but also lowers the overall bandwidth of the system and limits the maximum achievable data-rate to 16 Gbps at full-duplex operation. Nevertheless, the presented topology\(^ {33}\) is incapable to eliminate the high-frequency components of the self-interlace signal which appears as spikes in the middle of the received data (due to the propagation delay of the interconnect) coming from tranceiver in the other end of the interconnect. In the proposed SBT, a \( R \) high-pass filter (HPF) is utilized as a differentiator to eliminate residual echo by generation cancelation current and perform better echo-cancelation by the incorporation of a hybrid device. As the SBT transmits and receives the data on the same interconnect simultaneously, the interconnect utilization is increased by 2X in comparison with the unidirectional transmission which reduces the chip area significantly. After all, the performance of the proposed SBT was assessed by post-layout simulation results that are realized in 28-nm CMOS process across a 5-mm on-chip interconnection.\(^ {34}\) Thanks to the proposed SBT, the high speed of 20 Gbps is achieved.

The rest of the paper is organized as follows: Section 2 describes the architecture of the proposed SBT. Section 3 analyses the transistor level of design and the simulation results are discussed in Section 4. Lastly, the paper is concluded in Section 5.

### 2 Architecture Design

SBTs or FDTs use an identical interconnection for transmitting and receiving signals at the same time for a twofold increase in the data-rate. This forms a superimposed signal by the combination of inbound \( (V_{\text{in}}) \) and outbound \( (V_{\text{out}}) \) signals at both sides of the interconnect. Therefore, SBT suffers from the self-interposition owing to the superposition of the inbound and outbound signals. To separate the received data from the superimposed signal and perform echo-cancelation, a hybrid circuitry and/or echo-cancelation block is required. Thus, a new architecture to perform echo cancelation in SBTs with comprehensive analysis is presented. A single-ended block drawing of the presented SBT is illustrated in Figure 1.

The proposed SBT includes a hybrid transistor \( (M_{\text{hybrid}}) \), the main and the auxiliary drivers, an echo-cancelation (EC) block, and a trans-impedance amplifier (TIA). The hybrid MOS device is used not only to separate the transmitted and received signals from each other at both sides of the on-chip interconnect, but also employs low-impedance \( R \) high-pass filter (HPF) and outbound \( (V_{\text{out}}) \) signals at both sides of the interconnect. Therefore, SBT suffers from the self-interposition owing to the superposition of the inbound and outbound signals. To separate the received data from the superimposed signal and perform echo-cancelation, a hybrid circuitry and/or echo-cancelation block is required. Thus, a new architecture to perform echo cancelation in SBTs with comprehensive analysis is presented. A single-ended block drawing of the presented SBT is illustrated in Figure 1.

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termination to enhance the bandwidth of the system. Moreover, it converts the variations in its source-gate voltage \( V_{sg} \) to a small-signal drain current \( i_D \) by virtue of its transconductance \( g_m \).  

Nevertheless, by producing identical (equal magnitude and in-phase) signals at the source and the gate of the \( M_{hybrid} \) \( (V_g = V_{ob}) \), \( V_{sg} \) variation will not be a function of the outbound signal. Accordingly, the \( i_D \) of the hybrid transistor is predominantly a function of the inbound signal \( V_{ib} \) from the SBT on the other end of the interconnection, which is sensed on \( V_{sg} \). Afterward, the detected inbound or received voltage signal \( V_{ib} \) is converted to the inbound current \( I_{ib} \) by the \( g_m \) of the hybrid transistor.

The main driver generates the signal \( V_g \) at the gate of the \( M_{hybrid} \) for transmitting. However, \( M_{hybrid} \) acts as common-drain (CD) in the transmitting functionality of the SBT. Thus, the signal at the source of \( M_{hybrid} \) is \( V_{ob,M} = \alpha V_g \), which is created by the main driver while \( \alpha = A_{v(DC)} < 1 \). To realize echo cancelation, the gate and the source voltages of the \( M_{hybrid} \) must be in-phase with equal amplitude. To fulfill the above-mentioned condition, an auxiliary driver is utilized in the SBT. It generates the signal \( V_{ob,A} = \beta V_{ob} \) as a function of the steering current \( i_{tx} \) and \( \beta \), which is stemming from the auxiliary driver and the impedance seen by its output \( (R_A) \). Mathematically, \( V_{ob} \) can be expressed by Equation 1 at both ends of the interconnection.

\[
V_{ob} = V_{ob,M} + V_{ob,A} = \alpha V_g + \beta V_{ob}
\]  

In order to obtain \( V_{ob} = V_g \) and in turn having zero echo signal, \( \alpha + \beta \) must be equal to 1. Consequently, the auxiliary and the main drivers produce the superposition signal \( V_{ob} \) altogether. However, the loading is different at nodes A and B, which leads to the leakage of the strong transmitted signal into the receiver. Therefore, the full-duplex operation that deals with the received signal may comprise the undesirable signal \( I_e \) as residual echo, which is stemming from the ill-matched \( V_{ob} \) and \( V_g \) signals and includes the high-frequency components.

Therefore, considering the SBTs at both ends of the interconnect which transmits data simultaneously, the drain current is the combination of two components. The current that comes from the far-end SBT \( I_{ib} \) and the echo signal \( (I_e) \) as the leakage near-end current. To eliminate the \( I_e \), an echo-canceling current \( (I_c) \) is generated by the EC block which is approximately equal and opposite to \( I_e (I_c = -I_e) \). Finally, the received current signal \( (I_{rx} = I_{ib} + I_e + I_c) \) is amplified and converted into the output received voltage \( V_{rx} \) by the TIA for further processing.

3 | CIRCUIT DESIGN

Figure 2 shows the single-ended transistor-level schematic of the proposed FDT. The main driver generates a significant portion of the outbound signal. At the design of the main driver, a structure similar to the hybrid branch is used to minimize the process mismatches. The portion of the transmitted signal, which is generated by the main driver \( (V_{ob,M} = \alpha V_{g,B}) \) can be calculated by the following equations:
\[
\alpha = A_{VC/CD} = \frac{g_{m1}}{g_{m1} + R_{L_A}}, \text{ where } R_{L_A} = (R_{int} + 1/g_{m1})||r_{o2}||r_{o5}
\]

\[
V_{g,B} = \frac{[1 + (g'_{m1} + g'_{mb1})r'_{o1}]}{r'_{o1} + (g'_{m1} + g'_{mb1})r'_{o1}r'_{o2} + r'_{o2} + R'}i_{tx,M}
\]

where \(V_{g,B}\) is the gate-voltage created by the main driver at node \(B\), \(i_{tx,M}\) is the current steering from the main driver, and \(R_{int}\) is the ohmic resistance of the interconnection.

A simple differential pair including \(M_3\), \(M_4\) and \(M_5\) transistors, is utilized as an auxiliary driver. The \(M_4\) and \(M_5\) transistors can operate in both ON or OFF modes, according to the applied pseudorandom binary sequence (PRBS) data. These transistors will be operated in the saturation region in their ON state and the driver will benefit from a higher output impedance. Moreover, the steering current \(i_{tx,A}\) from \(M_3\) device is used to control the amplitude of the outbound signal at node \(A\) and fulfill the echo-cancelation condition. Consequently, the auxiliary driver generates the minor portion of the transmitting signal, which can be expressed as

\[
V_{ob,A} = R_Ai_{tx,A}, \text{ where } R_A = 1/g_{m1}||R_{int} + 1/g_{m1}||r_{o2}
\]

The hybrid circuitry consists of two transistors (\(M_1 \& M_2\)) and a resistor. The transistor \(M_2\) and resistor \(R\) are used to bias the transistor \(M_1\), which operates as a hybrid device.

Generally, a transceiver suffers from the signal distortion, reflection, and attenuation in the lack of proper termination for impedance matching. Therefore, impedance matching between the transceivers and the interconnect is an important issue. Unlike the off-chip transmission lines, termination with the characteristic impedance (\(Z_c\)) of the TL is not required for on-chip interconnections. Because the characteristics and behavior of the on-chip and off-chip interconnections are different. However, the bandwidth of the full-duplex systems can be enhanced by employing a low-impedance termination at both sides of the interconnection,\(^\text{11}\) which leads to better signal integrity and lower bit error rate (BER). Thus, low-impedance termination is performed by the impedance seen from the source of the hybrid transistor (\(\approx 1/g_{m}\)).

However, perfect echo-cancelation can be performed in the flat portion of the transmitting signal (contain the low-frequency components) by using \(M_{\text{hybrid}}\) auxiliary and main drivers. This is because of the RC dominated behavior of
the on-chip interconnects. The interconnect capacitance \(C_{\text{int}}\) is almost 1 PF for the used on-chip interconnection, which has a length of 5 mm\(^3\) while the total junction capacitances for \(M_1\), \(M_2\), and \(M_5\) are approximately 60 fF. Therefore, the rise/fall times are slower due to the large capacitance in node A \((C_A = C_{\text{int}} + C_{D2} + C_{S1} + C_{DS} \approx C_{\text{int}})\). On the other hand, the signal \(V_{g,B}\) has a faster rise/fall times in node B. Therefore, the hybrid device cannot eliminate the self-interface of the SBT completely by the help of the auxiliary driver. Therefore, some uncanceled echo signal \(I_e\) which includes the high-frequency components leakages into the receiver.

\(I_e\) appears similar to spikes at rising/falling edges and it is proportional to the derivative of the transmitting signal. Hence, a high-pass filter (HPF) which acts as a differentiator\(^\text{36}\) is employed to produce the echo-canceling signal \(I_c\). The transfer function of a first-order RC HPF is

\[
H_{\text{HPF}}(s) = \frac{sR_fC_f}{1 + sR_fC_f} \approx sR_fC_f, \text{ if } \omega \ll \omega_c
\]

where \(\omega_c = \frac{1}{R_fC_f}\) is the corner frequency of the HPF. According to Equation (5), the echo-canceling signal \(I_c(t)\) is proportional to Equation (6). Moreover, the series resistor \(R_s\) is used to attenuate the echo-canceling signal.

\[
I_c(t) \propto R_fC_f \frac{d}{dt} V_{g,B}(t)
\]

So as to evaluate the echo cancelation functioning of the proposed full-duplex transceiver, the following steps have been performed. First, the proposed transceiver is evaluated in half-duplex mode. Therefore, PRBS data is applied only to the near-end transceiver. So, the far-end one is kept in its receiver mode. In this case, the signal at the output node of the near end transceiver is fundamentally the echo signal \(I_e\). To eliminate the echo signal \(I_e\), the values of the \(C_f\), \(R_f\), and \(R_s\) are optimized to generate the corresponding echo-canceling signal \(I_c\) approximately equal and opposite to \(I_e\) \((I_c \approx I_e)\). Finally, the signal is applied to SBTs at both ends of the interconnect to perform simultaneous bidirectional signaling. In this case, the output current signal is the sum of \(I_e\) and \(I_{ib}\). The simulated waveforms are plotted in Figure 3.

![](figure3.png) **FIGURE 3** Echo-cancelation operation

It shows that a good amount of echo-cancelation is performed. Even though there is still some amount of uncanceled echo-signal, however, the residual echo or noise signal \(I_n\) is insignificant in comparison with the amplitude of the received signal from the far-end transceiver in full-duplex operation. Therefore, the received signal \((I_{rx} + I_n)\) is detectable in the presence of the residual echo.
RESULTS AND DISCUSSION

The transistor-level implementation of the proposed SBT has been realized in TSMC 28-nm standard CMOS technology. Figure 4 indicates the layout of the proposed SBT has a small area of 33.2 μm × 47.7 μm. To evaluate the functionality of the proposed SBT, the post-layout simulations are carried out and its performance was evaluated across an on-chip link. The on-chip interconnect which is used for simulations has a length of 5 mm and width of 0.6 μm while there is 1-μm distance between the interconnect and the adjacent shield layers.34

The simultaneous bidirectional signaling has been performed by transmitting 10-Gbps data from each of the SBTs at both sides of the on-chip interconnection. Consequently, a total data-rate of 20 Gbps is obtained (i.e., bit period is 100 ps). The applied data streams are $2^7 - 1$ random bit patterns, which are produced by an on-chip PRBS generator.37 Figure 5 illustrates the differential voltage eye diagrams of the received data for both FDTs.

The eye diagrams have a vertical opening of 165 and 170 mV and horizontal openings of 79 and 78 ps, respectively. The random and peak to peak jitters of the eyes for both FDTs are almost 5 and 22 ps, respectively. To perform 20-Gbps full-duplex operation, each transceiver consumes 14.7-mW power from 0.9 V supply voltage. Thus, the SBT including TIA has an energy efficiency of 0.147 pJ/b/mm. The transmitted and the received data pattern of one of the SBTs can be seen in Figure 6.

Higher bit rates reduce the sampling/bit period. Subsequently, the jitter measured as a percentage of the bit period and referred to as unit interval (UI) affects the signal integrity significantly which may translate in increased bit errors. Therefore, the bit error rate (BER) performance of the SBTs at both ends of the interconnect has been evaluated.

Figure 7 shows the horizontal (timing) bathtub curves have 29% UI and 31% UI at BER of $10^{-12}$, respectively.

The robustness of the echo-cancelation against the process, supply voltage, and temperature (PVT) variations was also tested. For this purpose, these variations are applied to the SBT at 2 × 10-Gbps full-duplex operation. The variations of horizontal and vertical eye openings for the different process corners are shown in Figure 8. The worst-case performance occurs in the slow-slow (SS) corner where the vertical and the horizontal openings are reduced to 105 mV and 64 ps, respectively. Nevertheless, the eye is still open enough and leads to reliable data detection.

The performance of the SBT was then evaluated while the supply voltage varies in the range of 0.85 to 0.95 V. The simulation results are plotted in Figure 9A and shows that the eye opening increases by increasing the supply voltage and contrariwise. Similarly, the variation of the horizontal and the vertical eye openings are observed by varying the temperature from −20°C to 100°C. The simulation results are shown in Figure 9B. By decreasing the temperature from
room temperature to \(-20\degree \text{C}\) and increasing to \(100\degree \text{C}\), the vertical eye opening increases by 6% and decreases by 15%, respectively. Nonetheless, the horizontal opening changes less than 10 ps for the whole range.

Figure 10 shows the variation of the maximum height and width of the eye for 200 runs of Monte Carlo simulation. Based on the mean and the standard deviation values given in Figure 10, it can be concluded that the proposed SBT is satisfactorily durable against the device mismatches.

Previously reported designs are implemented in different CMOS technologies and a brief explanation about these solutions have been given in the introduction. However, most of the architectures are unidirectional and only a few numbers of SBTs are reported in the literature. Table 1 summarizes the performance comparison of the proposed SBT with the state-of-the-art full-duplex transceivers over on-chip interconnects.
FIGURE 7  (A and B) Horizontal bathtub curves for both of the simultaneous bidirectional transceivers (SBTs) at full-duplex signaling of 20 Gbps

FIGURE 8  Vertical and horizontal eye openings for different process corners

FIGURE 9  Variation of vertical and horizontal eye opening with change in (A) supply voltage and (B) temperature
Thanks to the proposed SBT, the maximum achievable data rate is doubled with respect to Wary and Mandal\textsuperscript{32} and improved by 25\% in comparison with Ebrahimi Jarihani et al.\textsuperscript{33} Therefore, the proposed solution has the highest data rate (20 Gbps) among the previously reported FDTs while consuming comparable power.\textsuperscript{28}–\textsuperscript{33} The design reported in Wary and Mandal\textsuperscript{32} is superior in terms of energy-efficiency while this solution offers a lower data-rate of 10 Gbps. It can be imagined that the performance of the solution described in\textsuperscript{28} will be degraded by using longer on-chip interconnections. Resistance and insertion loss of the interconnections will be increased by diminishing the width of them. Moreover, it leads to consuming more power and also a reduction in the overall bandwidth of the full-duplex system. For this reason, the performance of the proposed SBT is assessed over a narrow link. In conclusion, the overall performance of the proposed SBT is superior compared with the state-of-the-art.

### CONCLUSIONS

This paper presented a 20-Gbps high-speed transceiver architecture for simultaneous bidirectional data transmission over an on-chip interconnection. A hybrid transistor is used to split the received signal from the superimposed signal at both ends of the interconnection and accomplish echo-cancelation with the additional usage of a differentiator. In addition, the hybrid device is utilized as an active low-impedance termination to enhance the operation bandwidth of the

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**TABLE 1** Comparison of the proposed architecture with the state-of-the-art

| References | \textsuperscript{28a} | \textsuperscript{29b} | \textsuperscript{31b} | \textsuperscript{32a} | \textsuperscript{30a} | \textsuperscript{33c} | This work\textsuperscript{c} |
|------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Technology (nm) | 180 | 180 | 180 | 65 | 65 | 28 | 28 |
| Supply voltage (V) | N/A | 1.8 | 1.8 | 1 | 1.1 | 0.9 | 0.9 |
| Interconnect length (mm) | 1 | 5 | 5 | 5 | 3 | 5 | 5 |
| Interconnect width (μm) | N/A | N/A | 2 | 1.5 | 2 | 0.6 | 0.6 |
| Data rate (Gbps) | 5 | 0.92 | 4 | 10 | 2 | 16 | 20 |
| Energy efficiency (pJ/b) | 3.8 | 9.48 | 0.95 | 0.38 | 1.54 | 0.8 | 0.735 |
| Area (μm\(^2\)) | — | 4200 | 1275 | — | 1364 | 1581 | 1574 |

\textsuperscript{a}Schematic Simulated results.
\textsuperscript{b}Measured results.
\textsuperscript{c}Post-layout simulated results.
transceiver. The proposed SBT structure has been realized in 28-nm low power CMOS technology with a supply voltage of 0.9 V. The FDT has an energy-efficiency of 0.147 pJ/b/mm for full-duplex data transmission of 20 Gbps. The performance of the proposed FDT has been validated by performing post-layout simulations and results have been carried out over an on-chip interconnection with a length of 5 mm and narrow width of 0.6 μm. The results show the robustness of the SBT to the introduced PVT variations and device mismatches while performing FD operation. The proposed architecture achieves the highest data rate among the previously reported SBTs, which makes it suitable for high-speed die-to-die on-chip wireline communications like SoC applications.

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**CONFLICT OF INTEREST**
The authors declare no conflict of interest.

**DATA AVAILABILITY STATEMENT**
Data sharing not applicable.

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