L³U-net: Low-Latency Lightweight U-net Based Image Segmentation Model for Parallel CNN Processors

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ABSTRACT
In this research, we propose a tiny image segmentation model, L³U-net, that works on low-resource edge devices in real-time. We introduce a data folding technique that reduces inference latency by leveraging the parallel convolutional layer processing capability of the CNN accelerators. We also deploy the proposed model to such a device, MAX78000, and the results show that L³U-net achieves more than 90% accuracy over two different segmentation datasets with 10 fps.

KEYWORDS
neural networks, image segmentation, low latency, edge cnn processor

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1 INTRODUCTION
Semantic segmentation is one of the fundamental computer vision tasks that assign each pixel of an image with a predefined label. This task is effectively utilized for many applications like video surveillance, autonomous vehicle guidance, robotics, and biomedical image analysis. For most of these applications, real-time processing with high-resolution inputs and the low energy consumption is critical as many of these applications are designed to be a part of battery-powered devices like drones or personal gadgets. This makes TinyML research essential to develop applications that can run on hardware using mWs of power, KBs of RAM, and less than KBs of flash [27].

With the advance of deep learning (DL), the performance of semantic segmentation models has been improved significantly and now very accurate results are possible. There are various approaches in the literature for this task that differ in particular aspects such as network architecture, cost function, training strategies, training data, etc. [25]. The initial approaches adopt fully convolutional networks (FCN) [19, 21] where the global context information cannot be efficiently used. To add more contextual information to FCN approaches, Conditional Random Fields (CRFs) and Markov Random Fields (MRFs) are integrated back to the DL approaches. Liu et al. proposed a CNN model that enables MRFs in a single forward pass [20].

One of the most popular image segmentation approaches uses convolutional encoder-decoder model architectures. Noh et al. [26] proposed to use transposed convolution (deconvolution) layers to reconstruct the segmentation map from the VGG 16-layer network and present promising results on PASCAL VOC 2012 dataset. U-net [28] and V-Net [24] are popular auto-encode-based approaches. These architectures are different from [26] as there are residual connections between specified encoding and decoding layers. Various modified U-net models have also been used for many different applications like 3D image segmentation [9] or land use determination [8, 32, 35]. U-net is still a prevalent approach, and many recent studies propose modifications like adding dense skip connections [14] or proposing attention-based U-net architectures [12, 16] for different applications. Weng et al. [34] proposed a neural architecture search (NAS) approach to search highly accurate U-net-based models for medical image segmentation effectively.

DeepLab [4] family models are another group of commonly preferred semantic segmentation DL models that effectively utilize dilated (a.k.a. atrous) convolutions. This operator controls the resolution at which the features are computed in the DL models. By increasing the dilation parameter, the field of the view of the utilized kernels is increased to deal with larger context effectively without increasing the number of model parameters. Further improvements are proposed to this model [5–7]. Finally, DeepLab v3+, which combines cascaded and parallel dilated convolution modules and uses an auto-encoder approach, achieved an 89% mean intersection over union (mIoU) score.

A study [25] compares many other approaches like attention-based, generative or recurrent neural networks, as well as other popular approaches like RefineNet [17]. Nevertheless, these methods are not deployable to low-power, low-memory edge devices due to their high architectural and computational requirements.
Most of them cannot achieve real-time inference speeds. Besides, the existing studies on TinyML semantic segmentation are minimal. [23] proposes to use a new convolutional module, efficient spatial pyramid (ESP), efficient computation, memory, and power. A human-machine collaborative design strategy is used in [18] to create networks with customized module-level macro architecture and micro-architecture designs specifically for semantic segmentation tasks. A modified dilated convolution approach is also proposed in [10], where many layers are optimized for this task, and the backbone is changed with MobileNetV2 [29]. Despite these approaches reducing the computational load and testing on edge, they are not applied on TinyML hardware. Bahl et al. proposed a lightweight encoder-decoder model with depthwise separable convolutions and decreasing memory usage by removing skip connections between encoder and decoder [2]. The model is also realized on an FPGA, and its results are given on very low-resolution satellite images. Another recent work demonstrates an attention condenser neural network, AttendSeg, and its results on CamVid dataset [33], which is stated as deployable to a tiny edge device.

This study introduces a very lightweight U-net-based encoder-decoder model to solve the semantic segmentation problems on tiny battery-powered hardware. A data reforming (i.e., folding) approach is also proposed to be used for hardware composed of parallel CNN processor units. This strategy also enables the hardware to handle higher spatial resolution images. The complete design is implemented on a low power edge device, MAX78000 [1], which is shown as the most energy-efficient CNN inference hardware in the market [11, 22, 31]. To summarize, our contributions are:

- A fully CNN very lightweight modified U-net model for semantic segmentation problems,
- A data folding approach that enables higher resolution throughput for parallel CNN processing hardware architectures,
- An implementation of the proposed approach on such a device, MAX78000, and presentation of the results in terms of accuracy, speed, and energy consumption.

The remainder of this paper is organized as follows: In Section 2, we present the proposed data folding technique. The proposed network architecture is detailed in Section 3. The model deployment platform is described in Section 4. We evaluate the proposed models in Section 5.3 trained with the datasets presented in Section 5.1. The training approach and parameters are presented in Section 5.2. Finally, Section 6 summarizes the results.

2 DATA FOLDING TECHNIQUE

Inference latency plays a critical role for neural network accelerators at the edge since it directly affects those resource-constrained devices’ frame-per-second (FPS) performance metrics. The convolution operation is parallelizable in the channel domain, and this feature has already been utilized in neural network accelerators [1]. The initial layers of CNN networks generally have the highest spatial resolution and spatial size, whereas they have the lowest channel counts compared to deeper layers of the network. These initial layers induce a significant proportion of the entire network’s latency since only a small number of cores can be used to process the small number of input channels that are big in spatial size. However, the spatial resolutions decrease for most network architectures, and the channel counts increase as the network proceeds over the following layers. Therefore, these middle layers are more suitable for parallel processing. U-net is an example of such networks, and the highest spatial resolution is in the initial layers. In the original U-net architecture, the input image consists of only one channel, and its size is 572x572 [28]. Suppose U-net is deployed in a neural network accelerator. In that case, only one processor core out of many will be active and busy processing the big input, which generates a significant amount of all network latency.

To optimize the latency of the initial layers and to distribute the uneven processor loads to many processor cores more evenly, we propose a novel technique, data folding. Applying this technique and performing a regular convolution with stride=1 is mathematically equivalent to strided convolutions; however, the latency is reduced by distributing the processing load to the parallel cores. The proposed data folding technique works by creating downsampled versions of the input data by first shifting in height and width, then combining those downsampled versions of the original data in the channel domain. Although the spatial resolution appears to shrink, all of the original information is fed to the network by increasing the channel count. Consequently, the data becomes more suitable for parallel processing since more channels mean more processing cores can be utilized for the same amount of data processing. Likewise, the processing latency drops as each processor needs to handle smaller data due to lowered resolution after folding.

In Fig. 1, the folding of input data of 3x8x8 size into 48x2x2 is illustrated, where the shapes are given as channel size x height x width format (CHW). As shown, the channels of the folded data are the downsampled versions of the original channels. In this example, the folding factor, α, is assumed to be 4. The downsampled data from each channel with sampling offsets are placed through the channels of the new kernel, where the sampling offsets vary between 0 to α − 1 in both height and width axes. In Fig 1, blue channels show the downsampled data with sampling offset is equal to 0 for both height and width. On the other hand, yellow channels illustrate the downsampled data with sampling offset is equal to 0 for the height but 1 for the width. Yellow channels follow the blue channels stacked in the channel axis. Likewise, other downsampled versions with increasing offset values are stacked further. Figure 2 shows an example of a folded image when α is 2.

Since the data in the neighbor pixels are folded into channels, the same data portion can be processed with a smaller 2d convolutional kernel after the folding. In Fig. 3 A, the data with a shape \(N_{ch} \times N_{h} \times N_{w}\) is shown. The 2d convolutional kernel with a side length equal to \(\alpha \times k\) is illustrated with a yellow square prism in the same figure. After folding, the 3d data matrix takes the shape of \(\alpha^2 \times N_{ch} \times \frac{N_{h}}{\alpha} \times \frac{N_{w}}{\alpha}\). The data in the slice of the kernel highlighted in yellow in Fig. 3 A is now placed in another square prism. The side length of this prism is now \(k\) instead of \(\alpha \times k\) as seen in Fig. 3 B. Therefore, the same data can be accessed with a smaller convolutional kernel after folding. Data folding not only changes the kernel lengths, but also the stride parameter. Since the spatial dimensions shrink after folding, any step in these shrink dimensions corresponds to larger steps in the original data tensor. Numerically, a convolution stride of \(s\) in the folded tensor corresponds to a stride of \(\alpha \times s\) in the original
where there is no data folding. The yellow bar shows the case with data folding. The input data is assumed to have three channels, e.g., RGB channels of an image, and the processor is assumed to have at least 48 parallel cores. It is noteworthy that as $\alpha$ doubles, the processor load on each active processor is quartered if enough idle processors exist. The folding factor must be chosen based on the number of parallel cores and the desired stride on the original tensor. Higher folding factors result in greater steps in the shift of the convolutional kernel in the original tensor.

3 PROPOSED L^3U-NET ARCHITECTURE

The U-net model [28] is a CNN model that has a condensing path to obtain the context and a symmetrical expanding path to provide accurate localization. There are connections between these paths at different resolutions in the U-net model to allow information shared through the network. To achieve low latency and energy while providing high performance in edge devices, we propose a model that combines the data folding technique with a small version of the U-net architecture.

Because of the data reshaping limitations of the chosen deployment platform, we utilize data folding only at the beginning layer of the proposed architecture. To reverse the folding action and create the segmentation map with the same resolution of the input image, data unfolding is applied at the end of the network. This operation is simply a tensor reshaping. In Fig. 5, the proposed UL-net architecture is illustrated. In the figure, the input image has three channels, and its size is 352x352. With data folding, a 48x88x88 shaped input tensor is obtained. In this spatial resolution, the architecture sequentially contains three Conv2d layers with 1x1 kernel and one Conv2d layer with 3x3 kernel. In the spatial

![Figure 1: Visualization of the proposed data folding technique](image1)

![Figure 2: Example for input image folding for $\alpha=2$. The original image is 3x352x352 and the folded image is 12x176x176.](image2)

![Figure 3: 2D convolution operation before and after folding](image3)

![Figure 4: Distribution of convolution operations per processor with regard to the number of input data channels.](image4)
resolution contraction path, there are three Conv2d 3x3 layers with a 2x2 MaxPool preceding each of them. After the contraction path, three ConvTranspose2d operations take place in the expanding path. Between the contraction and expanding paths at each resolution, skip layers and channel-wise concatenations exist to facilitate information exchange and gradient propagation. After the resolution is increased back to 88x88, two Conv2d layers with 3x3 kernel and four Conv2d layers with 1x1 kernel are utilized to create the segmentation map.

All of the Conv2d layers contain batch normalization (BatchNorm), and before quantization-aware training (QAT) starts, the BatchNorm layers are fused into the weights and biases of the preceding Conv2d layers. The total number of parameters of the proposed architecture is 278,176 for four-class segmentation and 277,004 for two-class segmentation.

4 DEPLOYMENT PLATFORM

The proposed model is intended for deployment on CNN inference engines that work at the edge. As an example deployment platform, Analog Devices MAX78000 is chosen in this study. MAX78000 is an Ultra-Low-Power Arm Cortex-M4 processor with FPU-based MCU with CNN accelerator that targets battery-powered neural network-based applications at the edge [1]. MAX78000 has a weight memory of 442KB, and 1, 2, 4, or 8-bit weights are supported. As layers, it supports both Conv1D and Conv2D as convolution operations, 2D transposed convolution layer, linear layer, pooling layers, and element-wise operations. MAX78000 has 64 parallel processors. Each can only read from specific segments of the data memory but can write to the entire data memory. The CNN parallelization is performed at the input channels. Hence each input channel or group of input channels are processed by a different processor. The proposed data folding method leverages this feature by assigning the same load to a higher number of channels which results in an increase of parallelism.

5 EXPERIMENTS

5.1 Dataset

This study conducts experiments on two different datasets, and we present two possible edge applications. The first dataset, the Analog Devices MAX78000 is chosen in this study. MAX78000 is an Ultra-Low-Power Arm Cortex-M4 processor with FPU-based MCU with CNN accelerator that targets battery-powered neural network-based applications at the edge [1]. MAX78000 has a weight memory of 442KB, and 1, 2, 4, or 8-bit weights are supported. As layers, it supports both Conv1D and Conv2D as convolution operations, 2D transposed convolution layer, linear layer, pooling layers, and element-wise operations. MAX78000 has 64 parallel processors. Each can only read from specific segments of the data memory but can write to the entire data memory. The CNN parallelization is performed at the input channels. Hence each input channel or group of input channels are processed by a different processor. The proposed data folding method leverages this feature by assigning the same load to a higher number of channels which results in an increase of parallelism.

5.2 Training

To be deployed on MAX78000, the model needs to be quantized to at most 8-bit integers. Since simple post-quantization methods cause performance degradation [31], QAT is employed in this study. The QAT approach implements the fake (a.k.a. simulated) quantization approach of [15]. When training L*U-net, an Adam optimizer is used with an initial learning rate of 0.001. For the CamVid dataset, the training takes 100 epochs, and QAT starts at epoch 40. The learning rate is halved two times at the 20th and 80th epochs. For the AISegment dataset, the training takes 200 epochs. QAT starts at epoch 150, and the learning rate is halved three times at the 50th, 100th and 140th epochs. In this study, all weights are quantized to 8-bits, and batchnorm parameters are fused into convolutional layers before the QAT starts.

5.3 Results

The results of the proposed approach for the two selected datasets are summarized in Table 1.

![Table 1: Sample implementation results of proposed approach](image)

| Dataset   | Pixel-to-Pixel Accuracy (%) | mIoU (%) | Latency (ms) | Energy/Inf. (mJ) |
|-----------|-----------------------------|---------|--------------|------------------|
| CamVid    | 91.05                       | 84.24   | 95.1         | 7.3              |
| AISegment | 99.19                       | 98.09   | 90.3         | 6.9              |

As seen from these samples, the model accurately segments the regions, except for very tiny structures. For the four-class CamVid dataset, our approach provides better accuracy than many of the edge approaches in the literature AttendSeg [33] or EdgeSegNet [18]. As these works give their results for 32-class segmentation, it is not possible to compare the results in terms of accuracy, only model size and complexity of the operations. Our approach has 4x and 30x fewer parameters; 10x and 100x fewer MAC operations [18, 33]. In addition, with the proposed data folding approach, we were able to
run the model on a battery-powered edge device, MAX78000, with an inference speed up to 10 fps.

The model output for the AISegment dataset is the binary class label of each pixel, and Fig. 7 includes a model input image and removed background by L\textsuperscript{3}U-net model. A reference model, [30], provides 98\% mIoU for 224x224 image with a floating-point model that has 8x more parameters than ours. In that sense, L\textsuperscript{3}U-net is a more effective approach requiring less memory and less computation for larger input data.

Lastly, we provide energy measurements of the L\textsuperscript{3}U-net model on MAX78000. According to the results, with an AA alkaline battery, it is possible to calculate over 1.5 million inferences using the proposed model and setup. To the best of our knowledge, no other study gives these values for semantic segmentation at the edge; so we provide these results for future studies.
6 CONCLUSION

We presented L^U-net, a lightweight U-net-based fully CNN model which is also deployed to a tiny edge device, MAX78000. We also proposed a data folding approach that reduces the latency and enables processing of higher resolution input images for a multi-core CNN inference engine, MAX78000. The experiments performed show that L^U-net is capable of providing 91% and 99% accuracy for four- and two-class segmentation examples at a speed of 10 fps.

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