Design of Real Time Video Image Acquisition and Processing System Based on FPGA

Peifeng Chen
Jilin Radio and TV University Jilin, China
quake0490@sina.com

Abstract. Based on characteristics of instantaneously, large capacity and miniaturization of digital image acquisition and processing technology, a real-time video image acquisition and processing circuit system was designed, FPGA was used as the center of controlling the whole system and the center of processing image data. With DDR2 SDRAM the core component of high speed storage module, and CMOS 7670 the video image acquisition device. Through the Quratus II and Modelsim software for edge detection algorithm and the control process, each module of the hardware design and simulation, the realization of the video images from the collection and storage to the treating and display, which shows smooth, clear and real-time.

1. Introduction
With the continuous development of society, video image acquisition and processing technology Many industries play a very important role in the field, such as military, security Full surveillance, industrial vision and other fields, and all walks of life for video images Collection and treatment technologies are also becoming increasingly demanding. High speed, real-time is one of the main development trends. At present, video image acquisition and processing technology the development is mainly divided into two categories: First, based on the PC in the relevant specific.

On the basis of PCIe collecting board cards, video images are performed through software Rationale; second, use related integrated hardware such as DSP, MCU, FPGA, etc. Video image collection and processing. Relatively speaking, the latter's handling effect not as good as the former, but it is more suitable for real-time, small size, and convenient use. The demands of industry. FPGA field programmable logic gate column, using parallel operation mode, and High frequency of operation, can be used for real-time operation and processing of large amounts of data, in Communication field, image processing and other aspects of obvious advantages Therefore, this design The FPGA is chosen as the control and data processing center of the system.

1.1. General overview of the system
The video acquisition processing system based on FPGA can be divided into: video acquisition Module, image storage module, data processing module and image display module. Work the process is: First, FPGA conducts the camera through the IIC bus protocol Initializing configuration, camera focusing work, capturing images, and then, collecting. The video data is continuously written to DDR2 SDRAM
through the IFO buffer in the store, read the video data through the FIFO buffer, and then select Sex processes the readout video image data and finally shows on the VGA Show video images.

1.2. Central Control Unit

FPGA. From the perspective of FPGA hardware development, using EDA to develop software And hardware description language Verilog programming, the development of FPGA chips, Get the hardware functions required by its engineering. Comparing traditional hardware designs Hair, reducing device waste and multiple welding workload, design process it is also more flexible, convenient and efficient. In addition, FPGA implements the control and processing of each module, except and In addition to the advantages of line data processing, it must have more I/O ports and abundant Logic units, etc. In view of this, the Cyclone developed by Alter was selected IV series EP4CE 617 C8. This FPGA has 179 I/O connections the mouth, 62,792 logic units, 392 multipliers, and low power consumption.

Video Image Acquisition Module. CMOS OV 7670 image sensor, small size, small operating voltage,640 × 380 pixels, you can choose to wear noise reduction, digital conversion, frequency division and other work Can be a good video image acquisition choice. FPGA Through IIC Bus Association Discuss and initialize the configuration of the CMOS camera. Before the IIC bus is written, The SCLK and SDAT pins of the CMOS camera must have pull resistors. When the IIC bus is written, first write the device address, the initial address of the CMOS It is 0x42, followed by the register address, and finally the data is written. After the IIC bus communicates with the CMOS data, the CMOS camera is configured Control register. Clock configuration when working using an external clock, the FPGA The clock frequency is designed to better control the CMOS camera. PLL register Configure zero division frequency, enable internal linear voltage regulator LDO, internal voltage operation Stable. The Verilog partial code configured is:

```
SET_OV7670 +19: LUT_DATA = 16 'h1180;
SET_OV767: 5: LUT_DATA = 16 'h6b00;
```

Other related control registers are configured with horizontal image and off color Bar, video format RGB565 and other functions. Make sure it works fast on the system. The video image data with high reliability and strong information were collected under the line.

1.3. System storage module

DDR2 SDRAM. DDR2 SDRAM as system memory, selected within 1 GB the DDR 2 800 series SDRAM is stored as memory. DDR2 working hours Bell frequency is 200 MHz [2] , with fast reading and writing, high integration, storage The characteristics of large capacity and low cost. Its operating rate is ordinary SDRAM 4 times, can better achieve the system real-time requirements. DDR2 can not only work under the control of the system clock, but can also work independently. Operation, such as self-refresh, self-charging purification, etc., whose control is complex.Therefore, DDR2 SDRAM control is constructed using the quartus II self-brought IP kernel Manufacturer. At the same time, the Altera digital PHY is also generated. PHY is the connection. DDR2 kernel controller and external DDR2 Device Bridge. PHY owned Four-layer interface, which is a user logic interface with local_ * class, and a band the external DDR2 chip interface of the mem_class, with CTL _ * and ctl_mem _ *the interface between PHY and the IP controller. The use of IP kernel controller transfers DDR2 complex control operations Become a user's simple read and write timing operation, so the DDR2 storage module can Design is divided into clock, reset, initialization, control, data channel and arbitration, etc.. Submodule. The data channel submodule establishes DDR2 connection FIFO the passageway to the register.

IFO. IFO is a first-in, first-out memory with no address definition, using Easy. FIFO can only read and write data in order, ensuring the security of the data. Therefore, in most cases, it is used as a system data buffer. In the core of Quartus II, a controller for asynchronous IFO is established. Asynchronous FIFO, that is, reading and writing clock signals are inconsistent, which is conducive to the number of images According to the buffer. Wrusedw signals control the reading and writing of data. As Wrusedw equals FIFO depth value 4(for ease of reference, imitate FIFO Depth is 4), which means FIFO is empty,
Write Req signal is valid, can only write into the data. Wrusedw is 0, indicating that IFO is full, Read Req signal has Effect, can only read data. Wrusedw is the remaining value, read and write data please all requests can be executed.

2. Video Image Processing Module

2.1. Overall algorithm optimization

According to the rules of the SM3 algorithm, after the message is preprocessed, each 512-bit groups can be calculated in parallel. Introducing the SM3 algorithm (2), (3) the budget is used as the algorithm kernel. First pair of generated 512 bits Group to schedule whether the first level of the algorithm core is idle, Select the kernel module that you want to input. Use multiple kernel modules Block to flexibly increase throughput and reduce latency.

2.2. Optimization of Algorithm Core

Iterative compression calculation of 512 bits after grouping. This one. Part of it is the place that consumes the most resources. 132 outreach students in progress. Formed W0, W1 ... W67, W0’, W1’ ... W63 ‘ and 64 rounds the process of substituting ABCDEF GH is the main factor that affects performance.

Optimization of message extension. In the calculation of 132 extended words, each T1Time lost. Into a group of 512-bit messages, each level of running water handles different messages at the same time one round of calculations. It takes T1 to calculate a set of Wj, Wj ‘values. According to the principle of parallelism, T1The shortest is 7clk1 (clk1 is a message extension the working clock). But in order to match the subsequent 64 compression iteration. Combine, can do the appropriate delay and increase the water series.

Optimization of compressed iterations. For compressed functions, increase the number of ABCDEF GH registers Number, and use a 64 pipeline operation. Each Matching Time T2 Run a round of calculations of 512 bits of data, 64 streams at the same time, One round of calculations for processing different data, every passing time T2.Water down Level 1, so that in continuous input, after calculating the first data Time required (64 * T2) After that, you can use every T2 The speed of time lost Out of a set of register ABCDEF GH values, and then perform XOR operations Output the last hash value. In single-level calculations, the longest delay calculation process is:

\[
\begin{align*}
SS1 & \leftarrow ((A \ll 12) + E + (Ti \ll j)) \ll 7 \\
SS2 & \leftarrow SS1 (A \ll 12) \\
TT1 - GGj & (E, F, G) + H + SS1 + W’j \\
TT2 - GGj & (E, F, G) + H + SS1 + Wj
\end{align*}
\]

Last time. Addition operation, multiple addition operations executed in parallel to reduce addition operations. In this way, five levels of operations are performed in turn, that is, five clock cycles can be to calculate the values for SS1, SS2, TT1, and TT2. A similar method is used for P0 (TT2) calculations. That is, P0 (TT2) can be calculated after three clock cycles Value. Calculate SS1, SS2, TT1, and TT2 take five cycles and calculate P0 (TT2) takes 3 cycles, of which 1 cycle can overlap, so a total of 7 clock cycles. The clock cycle here is the working clock of the compressed iteration module clk2, IE T2 = 7clk2.

2.3. Optimization analysis

By parallel processing at the same time as message extension and compression iteration and the design of the pipeline structure can significantly improve the SM3The operating speed of the algorithm kernel is reduced while the delay is reduced. After Max {T1, T2} can perform a set of ABCDEF GH calculator calculations. In After each algorithm completes the calculation of the first-level iterative register, it is sufficient Receive new data input and call through multiple algorithms Obviously
improving performance, it can also be based on the actual performance requirements and the corresponding clock frequency to add or reduce the number of kernel modules. To achieve the corresponding performance targets. Achievement and results

3. Video Image Processing Module
In this paper, the image data are processed by Sobel edge detection. Edge the meaning of edge detection is that it can obtain the edge information of the target object, which is conducive to target identification and tracking. Sobel edge detection algorithm has a small amount of calculation, the advantage of high precision detection is also the most commonly used image edge processing method one. Sobel Edge Detection Algorithm Process: First, establish the Sobel operator template, it contains two sets of $3 \times 3$ operator matrix templates across the vertical. Secondly, using the horizontal and vertical matrix operators and the original image Pixel points perform plane volume integration operations to calculate the X and Y directions first derivative gradient value \cite{7}, as follows:

$$G_x = F(X, Y) = F(X + 1, Y + 1) + 2 F(X, Y + 1) + F(X - 1, Y + 1) - F(X - 1, Y - 1) - 2 F(X, Y - 1) - F(X + 1, Y - 1)$$

$$G_y = F(X + 1, Y) = F(X + 1, Y + 1) + 2 F(X + 1, Y) + F(X + 1, Y + 1) - F(X - 1, Y - 1) - 2 F(X - 1, Y) - F(X - 1, Y + 1)$$

Then, the calculated X and Y direction gradient values are square sum. Then open the square to get the gradient value of the center point. The following formula:

$$G(X, Y) = G_x^2 + G_y^2$$

Aunt. Finally, the center point gradient value is compared with the set threshold value, which is greater than the threshold is the edge point, the output is black, and the threshold is less than the normal point, lose Out of white. The implementation of Sobel edge detection includes buffer module and calculation convolution module. And do level processing module. Among them, the buffer module uses a RAM based shift Register a $Ltshift\_Taps$, convolution calculation module uses 6 programmable multiplications Water is calculated by $atmul\_add$ and 2 parallel additive $parall\_add$ Peaceful vertical gradient value, then obtained by floating point square root $altfr\_sqrt$ Center point value. Door level processing module is a comparison of thresholds.

4. Conclusion
Real-time video image acquisition and processing technology is widely used in monitoring and industry Visual and other fields. This system makes full use of its high speed and large size with FPGA core Data processing ability and hardware programming design, combined with related devices, real now the video image collection, processing and display. Experimental results, clear picture. Clear, smooth, good effect. At the same time, on this basis, the edge of the object is added Edge detection is also of practical significance in object tracking and recognition.

References
\cite{1} Tianjie, Yuguanglong, Qiaozhongtao, etc. Based on FPGA high-speed video images in real time Collection and processing system design [J]. Electronic Devices, 2016, 39 (3).
\cite{2} Wangcheng, Wu Caihaining, Wu Jihua. Alter FPGA / CPLD design [M]. Beijing: People's Post and Telecommunications Press, 2011.
\cite{3} Li Yuan. FDR/DRR2 interface FIFO design [D]. Xi'an: Xi'an Electronics University of Science and Technology, 2009.
\cite{4} Wuhouhang. Example: FPGA: first-hand experience that can be directly used in engineering projects Inspection [M]. Beijing: Machinery Industry Press, 2016.
\cite{5} Mei Ao-han. Design and Design of Wireless Image Acquisition and Transmission System Based on FPGA Research [D]. Hefei: Anhui University, 2016.
\cite{6} Ding Jisheng. Research and implementation of digital image processing algorithm based on FPGA [D]. Hefei: Hefei University of Technology, 2015.
\cite{7} Rollin. Research and Implementation of Fast Image Processing Algorithm Based on FPGA [D].
Chongqing: Chongqing Jiaotong University, 2015.

[8] Mamiao, Fanyangyu, Xiesong, etc. Image edge based on gray system theory Edge Detection New Algorithm [J]. Chinese Journal of Graphics and Graphics, 2003, 10 (10): 1136-1139.

[9] Tong Haifeng. Optimization Design of Video Image Edge Detection Based on FPGA [D].