Power Efficient Bit Lines: A Succinct Study

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Abstract. Reducing the consumption of power in VLSI circuits is challenging. A low power circuit in multi-port memories for power consumption reduction in bit lines is presented here. In this circuit the power of wide gates used in memory bit lines is decreased by reducing the voltage swing of the pull-down network. Wide gates were simulated and the results showed 40% lower power consumption. Processors are another component where power dissipation is high. Various methods are used to decrease the power dissipation. A number of methods reduce bus transitions to limit the power dissipation.

Keywords: VLSI circuits, Low power, Pull Network, ADC

1. Introduction

Dynamic circuit network is an advanced computer networking technology. Dynamic circuits have certain advantages over static ones hence the dynamic circuits are used in read-out paths. The major component of read paths is bit lines which can be local or global. Significant dynamic power of the read-out paths is consumed in the bit lines. This consumption of power can be almost 70% for the register files. As the size and read port are increased the power consumption in the bit lines is also increased. Using low power dynamic circuits, the power consumption can be reduced [1].

In current VLSI chip designs Dynamic voltage scaling is used to decrease the power utilization. This requires an effective monitoring of the supply voltages. Sensors to sense the voltage at specific locations are integrated in the chip for an effective and robust DVS system. The continuous expansion of CMOS technology in the chip leads to process variations. Thus, more locations on the chip need to be monitored for voltage variations and more need for voltage sensor and its area and power consumption. An ADC delay line with input stacking voltage was used for power supply delay line. A very low resolution of 12 μV/LSB, 1mW power consumption and 0.45 mm² area was achieved. A sampling rate of 1 GHz can be reached with these delay line ADC’s [2].

The electronic systems used on aircraft, artificial satellites and spacecraft are called avionics. The power usage in the digital processors significantly affects the performance of the avionic systems. There are several encoding methods developed to decrease the power utilization. In digital circuit the charging and discharging of node capacitance is where most of the power is dissipated [3]. The peak and average power dissipation is directly related to the speed of the processors. In military applications this is a major issue as the speed of the processors is very high and hence the power dissipation is also
high. Different methods have been developed to decrease the power utilization. The switching in the bus is the major source of power dissipation. Thus, reducing the switching in the bus is one way to reduce the power on the bus. This also reduces the cross-talk [4]. IOT brings opportunities and new types of applications. Network chips use Ternary content addressable memory (TCAM) for data routing. As TCAM usage increases, energy utilization becomes a critical challenge. Different techniques are used to reduce the power utilization of TCAM [5].

2. Literature Review

A 65 nm CMOS technology-based delay line ADC is implemented for on-chip voltage sensing. This is tested, implemented and analysed. High accuracy is achieved as observed from the measured results. The ADC consumes only 14 μW for its operation and occupies an area of 9000 μm² [6]. DRAMs can be integrated in logic circuits due to recent advances in technology. DRAMs occupy lesser space compared to SRAMs. Thus, DRAMs can be used as caches in the integrated circuits. One issue with DRAM is that it needs to be refreshed at small time intervals to retain the data. This increases the power utilization even when it is idle. Longer refresh times introduce errors in the data which can be mitigated by using Error Correction Code (ECC). This will reduce the power consumption [7]. High data rate communication over long wires is approximated as series capacitance and resistive load in the required frequency range. Capacitive driver is preferable for better power efficiency. With low power gigabit communication is achieved. 2 Gb/s data transfer over 10 mm is achieved in a 90 nm CMOS chip [8]. DRAMs are proposed as a low voltage charge transfer sense amplifier. It is used in two different modes namely dynamic pre-sensing latch and double boosting sensing node. The double boosting has two capacitors and is highly sensitive for low voltage. The dynamic pre-sensing latch is placed between the bit-line and increases the voltage difference and decreases the delay time sensing compared to earlier reports [9].

SRAM is used to save dynamic power by extracting the energy in bit line capacitors. During each write cycle the load to clock is fixed. The fixed load feature of the energy extraction significantly reduces the power dissipation. Thus, this method achieves significant reduction in power dissipation than the usual SRAM design [10].

3. Methodology

Circuit diagram of proposed delay-line ADCN bit-wide bus is shown in Figure 1. C denotes the capacitance, R is the resistance, and V is the voltage.

![Figure 1: Model of an ‘N’ Bit-Wide Bus](image)

\[ p = (a_1 C_1 + a_L C_L) V^2 f \]  

Where,
- \( a_L \) represents the conventional switching activity (ST) of the lines
- \( a_L \) represents the inter-wire switching activity (CT)
- \( a_1 C_1 \) and \( a_L C_L \) represents the switched inter-wire and substrate capacitance
Driver is determined by the voltage difference the moving charges feel during the current flow. Hence, the driver becomes more efficient as the driver output tracks the gradually swinging power-clock more closely. Figure 1 shows the schematics and output waveforms of our proposed energy recovery driver. Dotted lines denote power-clocks and solid lines denote driver outputs. This driver comprises a pair of load driving pass transistors two evaluation transistors, two pairs of driver activation blocks controlled by feedback from the driver output and a pair of inverters driving the pass transistors. The activation blocks serve the most important role of allowing the driver output to track the power-clock while preventing unnecessary switching. Since energy recovery drivers are powered by oscillating power clocks, the output of the driver also oscillates even when the driver input remains unchanged. Hence, this mechanism to prevent the idle switching increases driver efficiency. The driver charge path has two modes of operation depending on the level of the driver output. If out is low and PC increases above MP is turned on to charge the driver output. Since MN is turned off and MP is assuming in is low, a pull up path is formed from Vdd to X1. Hence, through inverter, MP is turned on to charge the load in an energy recovery manner. As PC and out reaches full rail, MP is turned off and MN is turned on pulling down X1 to Gnd, hence turning MP off. If out is at high level, MP remains turned off regardless of in to prevent unnecessary swing of driver output. Since MP is turned off and MN is turned on

![Figure 1: Schematics of energy recovery drivers and corresponding output waveforms](image)

**Figure 2:** Schematics of energy recovery drivers and corresponding output waveforms

**Table 1:** Shows the comparative analysis

| Author                        | Title                                                                                     |
|-------------------------------|-------------------------------------------------------------------------------------------|
| Mohammad Asyaei, et al.       | “Low Power Dynamic Circuit for Power Efficient Bit lines”                                 |
| Sida Amy Shen, et al.         | “ADC for On-chip Voltage Sensing”                                                        |
| Shuang Xie, et al.            | “A Power and Area Efficient 65 nm CMOS Delay Line ADC for On-chip Voltage Sensing”       |
| Pedro Reviriego               | “Low Power embedded DRAM Caches using BCH code Partitioning”                             |
| Eisse Mensink, et al.         | “Power Efficient Gigabit Communication Over Capacitively Driven RC-Limited On-Chip Interconnects” |
| Joohee Kim, et al.            | “Fixed-Load Energy Recovery Memory for Low Power”                                         |
| Choongkeun Lee, et al.        | “Highly Robust and Sensitive Charge Transfer Sense Amplifier for Ultra-Low Voltage DRAMs” |
| Eisse Mensink                 | “Power Efficient Gigabit Communication Over Capacitively Driven RC-Limited On-Chip Interconnects” |
4. Result
The power consumption is reduced and noise is also lower in the proposed new dynamic circuit. By applying the circuit techniques, the power consumption is reduced. In this VLSI a greater number of transistors are connected together and this dynamic circuit network is an advanced computer technology. So, we are used techniques in methodology that gives the low power efficiency for dynamic circuit. The fabrication any chip design is easy by very large-scale integration.

5. Applications
- The part of semiconductor and communication technologies. It is integrated circuits on a single chip. It is the technique of implementation circuit designing. so ,the low power dynamic circuit of power efficiency bit lines
- The accuracy and the design of an circuit is easy through this chip
- The power consumption also low taken

6. Conclusion
Finally, A low power dynamic circuit for power efficiency bit lines the dynamic circuit is switched technologies that are characteristics of traditional network systems and the IC’s is limited set of function that they perform so, the advanced version is used that is VLSI. So, the efficiency is desired output must be obtained.

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