Demonstration of Fin-Tunnel Field-Effect Transistor with Elevated Drain

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Abstract: In this paper, a novel tunnel field-effect transistor (TFET) has been demonstrated. The proposed TFET features a SiGe channel, a fin structure and an elevated drain to improve its electrical performance. As a result, it shows high-level ON-state current ($I_{ON}$) and low-level OFF-state current ($I_{OFF}$); ambipolar current ($I_{AMB}$). In detail, its $I_{ON}$ is enhanced by 24 times more than that of Si control group and by 6 times more than of SiGe control group. The $I_{AMB}$ can be reduced by up to 900 times compared with the SiGe control group. In addition, technology computer-aided design (TCAD) simulation is performed to optimize electrical performance. Then, the benchmarking of ON/OFF current is also discussed with other research group’s results.

Keywords: band-to-band tunneling; tunnel field-effect transistor; low operating power device; tunneling resistance; sub-threshold swing; ambipolar current; elevated drain

1. Introduction

Numerous studies about tunnel field-effect transistor (TFET) have been performed by several research groups as a promising device for an ultra-low power operation [1–4]. In case of metal-oxide-semiconductor FETs (MOSFETs), there exist a theoretical limit of 60 mV/dec subthreshold swing (SS) at 300 K-temperature because their carrier injection is based on the thermionic emission [5,6]. On the other hand, TFETs are relatively independent to the Boltzmann distribution since the function tail is removed by forbidden gap and the band-to-band tunneling (BTBT) dominates the carrier injection from source to channel [7,8]. Thus, the SS can be reduced to less than 60 mV/dec at RT, which allows the supply voltage ($V_{DD}$) to be decreased drastically, maintaining high ON-state current ($I_{ON}$). In addition, its fabrication process is highly compatible with that of MOSFETs. In spite of these advantages, however, the TFETs have some technical issues to be employed for a real application. First, it suffers from low-level ON-state current which is mainly attributed to the high tunnel resistance at source-to-channel junction [9–11]. In order to solve this, the Ge material has been adopted for its low bandgap and direct BTBT tunneling [12]. However, It is difficult to make a heterojunction using Ge material [12]. Second, a BTBT at channel-to-drain junction increases OFF-state leakage current ($I_{OFF}$); ambipolar current ($I_{AMB}$). Since these issues degrade TFET circuit’s electrical performance such as operation speed and power consumption, they should be addressed [13–16].

The purpose of this paper is to demonstrate a novel TFET which achieves larger $I_{ON}$ and smaller $I_{AMB}$ than that of conventional Si TFETs. As shown in Figure 1, the proposed TFET features a fin channel structure for improved gate controllability and a SiGe channel for higher $I_{ON}$ as reducing...
After 13 min process in the SC-1 solution, the SiGe fin width is reduced to 39.5 nm as shown in the inset (d). Some part of Si on active regions are removed by photolithography and reactive ion etching (RIE) processes forming SiGe source and channel while the remaining Si on mesa becomes raised drain region. In addition, its feasibility for better performance is examined by technology computer-aided design (TCAD) simulation. Last of all, based on the measurement and optimized results, the benchmarking of ON/OFF current ratio (I_{ON}/I_{OFF}) and SS with the state-of-the-art TFETs is also discussed.

**2. Device Fabrication**

The key process steps for the proposed TFETs are described in Figure 2a. First, silicon-on-insulator (SOI) thickness is decreased by using wet oxidation followed by SiO_2 wet etching. Then, SiGe and Si layers are grown on the SOI substrate by metal organic chemical vapor deposition (MOCVD). The process condition is as follow: a gas mixture of H_2 at 20 sccm, SiH_4 at 20 sccm, and GeH_4 at 90 sccm is used at 670 °C during 61 s for 300 Å-thick SiGe. Auger electron spectroscopy (AES) and transmission electron microscope (TEM) image confirm a single crystalline Si_{0.7}Ge_{0.3} is well grown on Si substrate (Figure 3) as ion implantation is performed at 10 keV-acceleration energy, 7°-tilted angle and 8 \times 10^{14} ions/cm^2-dose. Then, SiN_2 is deposited by plasma-enhanced CVD (PECVD) as an etching mask during an active patterning (c). PECVD nitride is adopted since it is low temperature insulator (SOI) thickness is decreased by using wet oxidation followed by SiO_2 wet etching. Auger electron spectroscopy (AES) and transmission electron microscope (TEM) image confirm a single crystalline Si_{0.7}Ge_{0.3} is well grown on Si substrate (Figure 3) as ion implantation is performed at 10 keV-acceleration energy, 7°-tilted angle and 8 \times 10^{14} ions/cm^2-dose. Then, SiN_2 is deposited by plasma-enhanced CVD (PECVD) as an etching mask during an active patterning (c). PECVD nitride is adopted since it is low temperature process with 400 °C and 20 s, in which the implanted dopants in the drain region can rarely diffuse. (d) Some part of Si on active regions are removed by photolithography and reactive ion etching (RIE) processes forming SiGe source and channel while the remaining Si on mesa becomes raised drain region. In case of channel, an additional patterning is conducted by mix-and-match process of e-beam lithography and photolithography to form 50 nm-width active fin (Figures 2d and 4).

The SiGe/Si fin width is further reduced by standard cleaning-1 (SC-1) solution which consists of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2), and de-ionized wafer (H_2O) [17,18]. The NH_4OH:H_2O_2:H_2O ratio is 1:8:64 in which the etching rate of the SiGe is ~0.85 nm/min. After 13 min process in the SC-1 solution, the SiGe fin width is reduced to 39.5 nm as shown in the inset of Figure 4. As shown in Figure 2e, an 1 nm-thick Si capping layer is deposited by selective epitaxy growth (SEG) followed by dry oxidation for a gate dielectric. It has been demonstrated that this process can efficiently prevent defects which could be induced between SiO_2 and SiGe [19]. The capacitance equivalent thickness (CET) of gate dielectric is confirmed as 3.4 nm from the capacitance-voltage (C-V) curve shown in Figure 5. (f) For a short-channel gate, sidewall spacer technique is applied: n-type doped polycrystalline-Si (poly-Si) is deposited by low pressure CVD (LPCVD) and etched by Si RIE process after photolithography for a gate pad. As a result, ~76 nm-length gate is defined self-aligning.
to the drain (Figure 6). After that, BF$_2$ implantation with 10 keV-acceleration energy, 7°-tilted angle and $8 \times 10^{14}$ ions/cm$^2$-dose is performed for a source region. The dopant activation is performed by rapid thermal process (RTP) with 900 °C and 5 s. Note that all processes for gate, source and drain formation are self-aligned to each other and can be compatible with state-of-the-art ultra-short channel technology. Finally, as a back-end-of line (BEOL), high plasma density (HDP) oxide is deposited as an interlayer dielectric (ILD) and metal layers (Ti/TiN/Al/TiN stacks) are deposited by physical vapor deposition (PVD) after contact formation. (g) Then, all of processes are summarized in the flow graph.

Figure 2. Fabrication process flow of the proposed TFETs. The flow graph summarize all the fabrication process briefly.

Figure 3. Auger electron spectroscopy (AES). The SiGe layer contains 30% Ge.

For the control samples, the planar Si and SiGe TFETs were fabricated. In the case of SiGe TFET, Si$_{0.7}$Ge$_{0.3}$ layers with a thickness of 30 nm are grown on SOI (100) substrates. The SOI layer is lightly p-doped ($1 \times 10^{15}$ cm$^{-3}$) with a thickness of 70 nm. For additional comparison, the Si TFET is fabricated on a 100 nm-thick SOI wafer. The gate stack consists of 200 nm poly-Si layer and 3 nm
SiO₂. After gate patterning, source and drain region are defined through photolithography and ion implantation processes. The ion implantation and BEOL processes are same with the processes in proposed TFET.

Figure 4. Cross-sectional view of scanning electron microscope (SEM) image which demonstrates Si fin etching. The inset shows top view of SEM image after fin etching and SC-1 reduction processes.

Figure 5. Measured C-V curves of MOS capacitors. The measured CET is 3.4 nm.

Figure 6. Cross-sectional SEM image which demonstrates raised drain and sidewall gate structure. The 76 nm-length gate self-aligning to the drain is well defined.
3. Measurement and Results

Figure 7a shows the transfer characteristics of the proposed device with the various drain voltages ($V_{DS}$). The SS is extracted at $V_{DS}$ of 0.1 V and a turn-ON voltage ($V_{\text{turn-ON}}$) is defined as gate voltages ($V_{GS}$) where BTBT first occurs. The $I_{\text{OFF}}$ and $I_{\text{ON}}$ are extracted when $V_{GS}$ is $V_{\text{turn-ON}}$ and gate overdrive ($V_{OV} = V_{GS} - V_{\text{turn-ON}}$) is equal to 2 V, respectively. The minimum SS is 81 mV/dec and $I_{\text{ON}}/I_{\text{OFF}}$ is $2.8 \times 10^4$. Figure 7b shows the output characteristics of the proposed TFET with the various $V_{GS}$. Note that, the conventional planar devices suffer from short channel effect (SCE) due to their weak gate controllability over the channel [20,21]. Generally, the SCE can be confirmed with drain induced current enhancement (DICE) in transfer curves and increase of saturation current in output characteristics. According to the measured results, however, there is no obvious SCE in the proposed TFET as shown in Figure 7a,b.

![Figure 7. (a) Transfer and (b) output characteristics of proposed TFET.](image)

The proposed TFET’s electrical characteristics are compared with that for planar Si and SiGe TFETs as control groups. Figure 8 shows the transfer characteristics of both groups at 1.0 V-$V_{DS}$. The SS and $I_{\text{ON}}$, $I_{\text{AMB}}$ and $I_{\text{ON}}/I_{\text{OFF}}$ are extracted from the curves and summarized in Table 1. The proposed TFET shows superior performance than the control ones in the several aspects. First, the SS of proposed device, which is measured at $V_{\text{turn-ON}}$ is 81 mV/dec whereas 151 mV/dec and 87 mV/dec are measured in planar Si and SiGe TFETs, respectively. Second, the proposed TFET shows 139 nA/μm-$I_{\text{ON}}$ which is 34 times and 5 times bigger than that for Si and SiGe TFETs, respectively. Last of all, the $I_{\text{AMB}}$ can be reduced by up to $10^3$ times compared with the SiGe TFET. These results are attributed in part to the SiGe’s narrow bandgap at the source area and in part to the strong gate-to-channel coupling with the help of fin-structured channel [22]. In addition, the elevated drain area reduces the BTBT between the channel and the drain by Si bandgap [23].

|                        | Si TFET | SiGe TFET | Propose TFET |
|------------------------|---------|-----------|--------------|
| SS ($V_{DS} = 0.1$ V)  | 151 mV/dec | 87 mV/dec | 81 mV/dec    |
| $I_{\text{ON}}$        | 4 nA/μm  | 21 nA/μm  | 139 nA/μm   |
| $I_{\text{AMB}}$       | 13 pA/μm | 16 nA/μm  | 18 pA/μm     |
| $I_{\text{ON}}/I_{\text{OFF}}$ | $4 \times 10^3$ | $2.7 \times 10^3$ | $2.8 \times 10^4$ |
4. Discussion

The objective of this study is to demonstrate the TFET with high $I_{ON}$ and low $I_{AMB}$. Compared with planar TFETs which is fabricated with the same processes, there is no doubt that the proposed structure is effective to improve electrical performance. However, the measured results imply that it requires further optimization for the better performance than the other strategies [25–37]. Therefore, the proposed TFET’s feasibility for the better performance is examined by TCAD simulations using Synopsys Sentaurus™. Above all, BTBT parameters in Kane’s tunneling model are calibrated by measured results [17]. In the simulations, to calculate BTBT generation rate ($G$) per unit volume in the uniform electric field, Kane’s model is used and fitted parameters are as follows (Equation (1)).

$$G = A \left( e \alpha \beta \right) \exp \left( -\frac{e \alpha}{kT} \right) \quad (1)$$

where $F_0 = 1 \text{ V/m}$, $P = 2.5$ for indirect BTBT. Prefactor $A$ and exponential factor $B$ are the Kane parameters and $F$ is the electric field. Both linear and log scale simulated transfer characteristics are.

Figure 8. Transfer characteristics of the proposed TFET and conventional planar TFETs with Si and SiGe channels.

The proposed TFET has remarkable electrical characteristics as shown above. However, the $I_{OFF}$ of proposed TFET near zero $V_{GS}$ is higher than that of planar Si TFET (Figure 8). In order to confirm the mechanism precisely, transfer characteristics with various temperature are investigated. As shown in Figure 9, drain current ($I_D$) is relatively independent to the $V_{GS}$ at around 0 V while it increases rapidly as a function of temperature. The result confirms that this current is dominated by Shockley–Read–Hall (SRH) generation–recombination [24].

Figure 9. Transfer characteristics of the proposed TFET in the range of 298–348 K.
measured results [17]. In the simulations, to calculate BTBT generation rate ($G$) per unit volume in the uniform electric field, Kane’s model is used and fitted parameters are as follows (Equation (1)).

$$G = A \left( \frac{F}{F_0} \right)^P \exp \left( -\frac{B}{F} \right)$$

(1)

where $F_0 = 1 \text{ V/m}$, $P = 2.5$ for indirect BTBT. Prefactor $A$ and exponential factor $B$ are the Kane parameters and $F$ is the electric field. Both linear and log scale simulated transfer characteristics are well matched to experimental data when $A: 1 \times 10^{14} \text{ cm}^{-1}\cdot\text{s}^{-1}/B: 3 \times 10^6 \text{ V/cm}$ are applied to TFETs. Then, the thickness of the gate dielectric is analyzed. Unlike advanced technologies, the proposed TFET uses 3.4 nm thick SiO$_2$ as the gate dielectric. Thus, if the gate dielectric is adjusted to 1 nm, the proposed TFET can obtain higher $I_{ON}$ at the low $V_{GS}$ (Figure 10). Figure 11 compares the $I_{ON}/I_{OFF}$ as a function of SS for the device shown in this paper and that in the previous articles [25–37]. Compared with the other Si based TFETs, the optimized TFET shows a remarkable performance in terms of minimum SS and $I_{ON}/I_{OFF}$.

Figure 10. Transfer characteristics of the proposed TFETs with various CET.

Figure 11. Performance comparison of TFETs. $I_{ON}/I_{OFF}$ of TFETs as a function.
5. Conclusions

In this paper, a novel TFET with SiGe fin channel and elevated drain has been introduced. The SiGe fin channel included small-bandgap and better electrostatic controllability which are leading high $I_{\text{ON}}$ and low SS, compared to conventional planar TFETs. Furthermore, the elevated drain could yield lower $I_{\text{AMB}}$ due to the increased physical distance between channel and drain. Considering these features, we have examined and demonstrated the fabrication processes of the proposed device. In addition, based on the measured results, the proposed TFET is calibrated by TCAD simulation. In order to optimize the device into state-of-the-art technique, the proposed device with thin gate dielectric is also simulated. The results proved that the device showed the improved $I_{\text{ON}}$ current and smaller SS. Consequently, these features of the proposed device will be available for compensating the weaknesses of conventional TFETs. Therefore, it will be one of the promising candidates for next-generation devices.

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References
1. Choi, W.Y.; Park, B.G.; Lee, J.D.; Liu, T.J.K. Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec. IEEE Electron Device Lett. 2007, 28, 743–745. [CrossRef]
2. Wang, P.Y.; Tsui, B.Y. Band engineering to improve average subthreshold swing by suppressing low electric field band-to-band tunneling with epitaxial tunnel layer tunnel FET structure. IEEE Trans. Nanotechnol. 2016, 15, 74–79. [CrossRef]
3. Kim, S.W.; Choi, W.Y.; Kim, H.; Sun, M.C.; Kim, H.W.; Park, B.G. Investigation on hump effects of L-shaped tunneling filed-effect transistors. In Proceedings of the Silicon Nanoelectronics Workshop (SNW), Honolulu, HI, USA, 10–11 June 2012; pp. 1–2. [CrossRef]
4. Mishra, A.; Pattanaik, M.; Sharma, V. Double gate vertical tunnel FET for hybrid CMOS-TFET based low standby power logic circuits. In Proceedings of the Emerging Research Areas and 2013 International Conference on Microelectronics, Communications and Renewable Energy (AICERA/ICMiCR), 2013 Annual International Conference, Kanjirapally, India, 4–6 June 2013; pp. 1–4. [CrossRef]
5. Knoch, J. Nanowire Tunneling Field-Effect Transistors. Semicond. Semimet. 2016, 94, 273–295. [CrossRef]
6. Long, P.; Wilson, E.; Huang, J.Z.; Klimbeck, G.; Rodwell, M.J.; Povolotskyi, M. Design and simulation of GaSb/InAs 2D transmissionenhanced tunneling FETs. IEEE Electron Device Lett. 2016, 37, 107–110. [CrossRef]
7. Sun, S.W.; Tsui, P.G. Limitation of CMOS supply-voltage scaling by MOSFET threshold-voltage variation. IEEE J. Solid-State Circuits 1995, 30, 947–949. [CrossRef]
8. Frank, D.J.; Dennard, R.H.; Nowak, E.; Solomon, P.M.; Taur, Y.; Wong, H.S.P. Device scaling limits of Si MOSFETs and their application dependencies. Proc. IEEE 2001, 89, 259–288. [CrossRef]
9. Kim, S.W.; Kim, J.H.; Liu, T.J.K.; Choi, W.Y.; Park, B.G. Demonstration of L-shaped tunnel field-effect transistors. IEEE Trans. Electron Devices 2016, 63, 1774–1778. [CrossRef]
10. Leonelli, D.; Vandooren, A.; Rooyackers, R.; Verhulst, A.S.; De Gendt, S.; Heyns, M.M.; Groeseneken, G. Performance enhancement in multi gate tunneling field effect transistors by scaling the fin-width. Jpn. J. Appl. Phys. 2010, 49, 04DC10. [CrossRef]
11. Gandhi, R.; Chen, Z.; Singh, N.; Banerjee, K.; Lee, S. CMOS-Compatible Vertical-Silicon-Nanowire Gate-All-Around p-Type Tunneling FETs With ≤ 50-mV/decade Subthreshold Swing. IEEE Electron Device Lett. 2011, 32, 1504–1506. [CrossRef]
12. Kim, S.W.; Choi, W.Y. Hump Effects of Germanium/Silicon Heterojunction Tunnel Field-Effect Transistors. IEEE Trans. Electron Devices 2016, 63, 2583–2588. [CrossRef]
13. Verhulst, A.S.; Vandenbergh, W.G.; Maex, K.; Groeseneken, G. Tunnel field-effect transistor without gate-drain overlap. *Appl. Phys. Lett.* **2007**, *91*, 053102. [CrossRef]

14. Anghel, C.; Chilagari, P.; Amara, A.; Vladimirescu, A. Tunnel field effect transistor with increased ON current, low-k spacer and high-k dielectric. *Appl. Phys. Lett.* **2010**, *96*, 122104. [CrossRef]

15. Anghel, C.; Gupta, A.; Amara, A.; Vladimirescu, A. 30-nm tunnel FET with improved performance and reduced ambipolar current. *IEEE Electron Devices Letters* **2011**, *32*, 141–146. [CrossRef]

16. Narang, R.; Saxena, M.; Gupta, R.S.; Gupta, M. Assessment of ambipolar behavior of a tunnel FET and influence of structural modifications. *J. Semicond. Technol. Sci.* **2012**, *12*, 482–491. [CrossRef]

17. Kobayashi, H.; Ryu, J.; Shingyouji, T.; Shimamukai, Y. Study of Si etch rate in various composition of SiC1 solution. *Jpn. J. Appl. Phys.* **2008**, *47*, 1–5. [CrossRef]

18. Sun, M.C.; Kim, G.; Kim, H.; Kim, S.W.; Kim, H.W.; Lee, J.-H.; Shin, H.; Park, B.G. Patternning of Si nanowire array with electron beam lithography for sub-22 nm Si nanoelectronics technology. *Microelectron. Eng.* **2013**, *110*, 141–146. [CrossRef]

19. Palmer, M.J.; Braithwaite, G.; Grasby, T.J.; Phillips, P.J.; Prest, M.J.; Parker, E.H.C.; Whall, T.E. Effective mobilities in pseudomorphic Si/SiGe/Si p-channel metal-oxide-semiconductor field-effect transistors with thin silicon capping layers. *Appl. Phys. Lett.* **2001**, *78*, 1424–1426. [CrossRef]

20. Kim, M.; Wakabayashi, Y.; Nakane, R.; Yokoyama, M.; Takenaka, M.; Takagi, S. High Ion/Ioff Ge-source ultrathin body strained-SOI tunnel FETs. In Proceedings of the 2014 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 15–17 December 2014; pp. 1–4. [CrossRef]

21. Zhang, J.; De Marchi, M.; Gaillardon, P.E.; De Micheli, G. A Schottky-barrier silicon FinFET with 6.0 mV/dec subthreshold slope over 5 decades of current. In Proceedings of the 2014 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 15–17 December 2014; pp. 1–4. [CrossRef]

22. Jain, P.; Rastogi, P.; Yadav, C.; Agarwal, A.; Chauhan, Y.S. Band-to-band tunneling in Ge source lateral tunnel field effect transistor: Thickness scaling. *J. Appl. Phys.* **2017**, *122*, 014502. [CrossRef]

23. Kim, H.W.; Kim, J.H.; Kim, S.W.; Sun, M.C.; Park, E.; Park, B.G. Tunneling field-effect transistor with Si/SiGe material for high current drivability. *Ipn. J. Appl. Phys.* **2014**, *53*, 06E12. [CrossRef]

24. Mookerjea, S.; Mohata, D.; Mayer, T.; Narayanan, V.; Datta, S. Temperature-Dependent I–V Characteristics of a Vertical InGaAs Tunnel FET. *IEEE Electron Device Lett.* **2010**, *31*, 564–566. [CrossRef]

25. Jeon, K.; Loh, W.Y.; Patel, P.; Kang, C.Y.; Oh, J.; Bowonder, A.; Park, C.; Park, C.S.; Smith, C.; Majhi, P.; et al. Si tunnel transistors with a novel silicided source and 46mV/dec swing. In Proceedings of the 2010 symposium on VLSI technology (VLSIT), Honolulu, HI, USA, 15–17 June 2010; pp. 121–122. [CrossRef]

26. Chang, H.Y.; Adams, B.; Chien, P.Y.; Li, J.; Woo, J.C. Improved subthreshold and output characteristics of source-pocket Si tunnel FET by the application of laser annealing. *IEEE Trans. Electron Devices* **2013**, *60*, 92–96. [CrossRef]

27. Leonelli, D.; Vandooren, A.; Rooyackers, R.; Verhulst, A.S.; Huyghebaert, C.; De Gendt, S.; Heyns, M.M.; Groeseneken, G. Novel architecture to boost the vertical tunneling in tunnel field effect transistors. In Proceedings of the 2011 IEEE International SOI Conference (SOI), Tempe, AZ, USA, 3–6 October 2011; pp. 1–2. [CrossRef]

28. Mayer, F.; Le Royer, C.; Damlencourt, J.F.; Romanjek, K.; Andrieu, F.; Tabone, C.; Previtali, B.; Deleouis, S. Impact of SOI, SiO1–xGeOx and GeO1 substrates on CMOS compatible tunnel FET performance. In Proceedings of the 2008 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 15–17 December 2008; pp. 1–5. [CrossRef]

29. Moselund, K.E.; Bjork, M.T.; Schmid, H.; Ghoneim, H.; Karg, S.; Lortscher, E.; Riess, W.; Riel, H. Silicon nanowire tunnel FETs: Low-temperature operation and influence of high-κ gate dielectric. *IEEE Trans. Electron Devices* **2011**, *58*, 2912–2916. [CrossRef]

30. Gandhi, R.; Chen, Z.X.; Singh, N.; Banerjee, K.; Lee, S.J. Vertical Si-nanowire n-type tunneling FETs with low subthreshold swing (<50 mV/decade) at room temperature. *IEEE Electron Device Lett.* **2011**, *32*, 437–439. [CrossRef]

31. Walke, A.M.; Vandooren, A.; Rooyackers, R.; Leonelli, D.; Hikavyy, A.; Loo, R.; Verhulst, A.S.; Koo, K.-H.; Huyghebaert, C.; Groeseneken, G.; et al. Fabrication and Analysis of a Si/Si0.55Ge0.45 Heterojunction Line Tunnel FET. *IEEE Trans. Electron Devices* **2014**, *61*, 707–715. [CrossRef]

32. Chen, Y.H.; Yen, L.C.; Chang, T.S.; Chiang, T.Y.; Kuo, P.Y.; Chao, T.S. Low-temperature polycrystalline-silicon tunneling thin-film transistors with MILC. *IEEE Electron Device Lett.* **2013**, *34*, 1017–1019. [CrossRef]
33. Kim, S.H.; Kam, H.; Hu, C.; Liu, T.J.K. Germanium-source tunnel field effect transistors with record high ION/IOFF. In Proceedings of the 2009 Symposium on VLSI Technology, Honolulu, HI, USA, 16–18 June 2009; pp. 178–179.

34. Morita, Y.; Mori, T.; Migita, S.; Mizubayashi, W.; Tanabe, A.; Fukuda, K.; Matsukawa, T.; Endo, K.; O’uchi, S.; Liu, Y.X.; et al. Synthetic electric field tunnel FETs: Drain current multiplication demonstrated by wrapped gate electrode around ultrathin epitaxial channel. In Proceedings of the 2013 Symposium on VLSI Technology (VLSIT), Kyoto, Japan, 11–13 June 2013; pp. T236–T237.

35. Morita, Y.; Mori, T.; Migita, S.; Mizubayashi, W.; Tanabe, A.; Fukuda, K.; Matsukawa, T.; Endo, K.; O’uchi, S.; Liu, Y.X.; et al. Performance enhancement of tunnel field-effect transistors by synthetic electric field effect. IEEE Electron Device Lett. 2014, 35, 792–794. [CrossRef]

36. Villalon, A.; Le Royer, C.; Nguyen, P.; Barraud, S.; Glowacki, F.; Revelant, A.; Selmi, L.; Cristoloveanu, S.; Tosti, L.; Vizioz, C.; et al. First demonstration of strained SiGe nanowires TFETs with ION beyond 700 µA/µm. In Proceedings of the 2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers, Honolulu, HI, USA, 9–12 June 2014; pp. 1–2. [CrossRef]

37. Villalon, A.; Le Royer, C.; Cassé, M.; Cooper, D.; Prévitali, B.; Tabone, C.; Hartmann, J.-M.; Perreau, P.; Rivallin, P.; Damlencourt, J.-F.; et al. Strained tunnel FETs with record ION: First demonstration of ETSOI TFETs with SiGe channel and RSD. In Proceedings of the 2012 Symposium on VLSI technology (VLSIT), Honolulu, HI, USA, 12–14 June 2012; pp. 49–50. [CrossRef]