Electrical Coupling of Monolithic 3D Inverters (M3INVs): MOSFET and Junctionless FET

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Abstract: In this paper, we investigated the electrical coupling between the top and bottom transistors in a monolithic 3-dimensional (3D) inverter (M3INV) stacked vertically with junctionless field-effect transistor (JLFET), which is one of candidates to replace metal-oxide-semiconductor field-effect transistors (MOSFET). Currents, transconductances, and gate capacitances of the top N-type transistor at the different gate voltages of the bottom P-type transistor as a function of thickness of inter-layer dielectric ($T_{ILD}$) and gate channel length ($L_g$) are simulated using technology computer-aided-design (TCAD). In M3INV stacked vertically with MOSFET (M3INV-MOS) and JLFET (M3INV-JL), the variations of threshold voltage, transconductance, and capacitance increase as $T_{ILD}$ decreases and they increase as $L_g$ increases, and thus there is a strong coupling in M3INV at the range of $T_{ILD} \leq 30$ nm. In M3INV, the coupling between stacked JLFETs in M3INV-JL is larger than that between MOSFETs in M3INV-MOS at the same $T_{ILD}$ and $L_g$. The switching threshold voltage ($V_m$) and noise margins (NMs) of M3INV are calculated from the voltage transfer characteristics (VTC) simulated with TCAD mixed-mode. As the gate lengths of M3INV-MOS and M3INV-JL increase, the $V_m$ variations increase and decrease, respectively. The smaller the gate lengths of M3INV-NOS and M3INV-JL, the larger and smaller the variation of $V_m$, respectively. The noise margin of M3INV-MOS is larger and better for inverter characteristics than one of M3INV-JL. M3INV-MOS has less electrical coupling than M3INV-JL.

Keywords: 3D monolithic inverter; MOSFET; junctionless FET; electrical coupling

1. Introduction

Since metal-oxide-semiconductor field-effect transistors (MOSFETs) were developed, the performance of semiconductor integrated circuits has been steadily developed in accordance with Moore’s Law [1]. Semiconductor devices with the gate length of less than 10 nm, which are core technologies required for the 4th industrial revolution such as artificial intelligence (AI), internet of thing (IOT), cloud computing, big data, and virtual reality [2], have been developing. As the process technology advances by scaling-down, the physical limitations of silicon-based semiconductor processes and the increased integration have led to the problems in thermal budget, delay, and power consumption [3]. In order to solve such problems, various types of researches related on developments of semiconductor materials, process technology, and devices have been actively carried out [4]. The monolithic 3-dimensional (3D) integrated-circuit (M3IC), which vertically stacks each tier on a previously fabricated tier, is one of the promising techniques to break the physical limits [5,6]. This technology is more advantageous in density, delay, and cost because of the smaller length of the Via than the existing parallel integration which makes devices on each wafer and connects them with through-silicon via (TSV) between wafers [7]. This is one of the main problems with M3IC which has the reduction the thermal budget of the MOSFETs in the 2nd and subsequent tiers on the M3DIC [8,9]. MOSFET and junctionless field-effect transistor (JLFET) have opposite operating principles. The MOSFET controls...
the current through depletion and inversion, and the JLFET controls the current with or without depletion. MOSFET has different source/drain and channel doping types (n/p), whereas JLFET use one doping type for source/drain and channel. Therefore, JLFET is advantageous in terms of thermal budget because the dopant activation process of the MOSFET is unnecessary. The thermal budget of upper tier is constrained by maximum thermal budget of the lower tier or tiers. JLFET has little effect of short channel effect, which is a major problem in MOSFET, and shows good performance in terms of carrier mobility. In order to solve the thermal budget problem, enhance the immunity of mobility degradation, and possess the simplicity of fabrication, JLFET [10,11] on M3IC has been proposed as the replacement of MOSFET [12].

M3IC technology stacking field-programmable gate-array (FPGA) logics and sensor devices have been reported, but the M3IC consisted of stacked MOSFETs and its thickness of interlayer dielectric (ILD), \( T_{ILD} \), between vertically stacked devices was over 100 nm so that there are no electrical coupling between stacking devices [9]. Recently, a study considering the electrical coupling between stacked devices has been performed when the ILD in monolithic 3D inverter (M3INV) consisting of MOSFETs is very thin (i.e., \( T_{ILD} < 50 \) nm) [13,14]. Interlayer coupling in monolithic 3D static random access memory (M3SRAM) stacked vertically with tunnel field-effect transistor (TFET) and MOSFET has been investigated in terms of stability and performance [15]. However, no research has been reported on the electrical coupling between the upper and lower devices of the M3IC consisting of JLFET [16] which can replace the MOSFETs.

Therefore, it is necessary to investigate the electrical interaction between devices in M3IC stacked with the next generation devices. In this paper, we will introduce the electrical coupling in terms of thickness variation of ILD in M3INV stacked vertically with JLFETs, compared with one with MOSFETs. The structures and simulation method of the M3INV with MOSFETs or JLFETs will be introduced (Section 2), and the electrical coupling of upper device at different gate voltage of lower devices, simulated with the DC/AC device parameter, will be investigated (Section 3). In Section 4, electrical characteristics of two types of M3INV (MOSFETs and JLFETs) will be explained. Finally, Section 5 concludes.

2. Structure and Simulation Method

Figure 1 shows two types of M3INV structures used in the simulation. The M3INV consists of N-type and P-type transistors in the upper and lower tiers, respectively. Figure 1a,b are schematics of M3INV consisting of MOSFET (M3INV-MOS) [5] and JLFET (M3INV-JL) [12], respectively. The doping concentrations of source/drain, LDD, and channel in MOSINV-MOS are \( 10^{21}, 10^{18} \), and \( 10^{15} \) cm\(^{-3} \), respectively [13,14]. The doping concentrations of source/drain and channel of M3INV-JL is \( 10^{20} \) and \( 10^{19} \) cm\(^{-3} \), respectively [12]. The detailed parameters in both M3INV-MOS and M3INV-JL are shown in Table 1. Three types of structures for both M3INV-MOS and M3INV-JL are simulated: gate lengths/gate oxide thicknesses are 20/0.9 nm, 30/1 nm, and 50/1.1 nm, respectively [14]. SiO\(_2\) was used for the regions in gate oxide, ILD, and bulk oxide (Box). Figure 1c shows the equivalent circuit of M3INV-MOS and M3INV-JL. Silvaco’s technology computer-aided-design (TCAD) simulator ATLAS [17] was used in this simulation. The models used in the simulation are CVT, SRH, AUGER, and FERMI. The leakage currents of both MOSFET and JLFET in each M3INV were set equal to \( 10^{-8} \) A, in order to simulate the inverter characteristics with same leakage current condition. The \( V'_{th} \) variation, \( g_m \) variation, \( C_{ngng} \) variation, \( V_m \), and noise margin of both M3INV-MOS and M3INV-JL were compared through TCAD simulation.
Figure 1. Schematics of two types of monolithic 3-dimensional (3D) inverter (M3INV) cell structure. (a) Structure of M3INV-MOS and (b) structure of M3INV-JL. (c) Equivalent circuit of M3INV-MOS (M3DINV-JL).

Table 1. Device/electrical parameter descriptions and dimensions.

| Symbols | Description | Value/Unit |
|---------|-------------|------------|
| \(C_{ngng}\) | Total gate capacitance of the top transistor | F |
| \(\Delta V_{Cngng}\) | Difference of \(V_{ngs}\) at maximum \(dC_{ngng}/dV_{ngs}\) of the top transistor at between \(V_{pgs} = 0\) and 1 V | F |
| \(\Delta V_{gm}\) | Difference of \(V_{ngs}\) at maximum \(g_m\) of the top transistor at between \(V_{pgs} = 0\) and 1 V | S |
| \(\Delta V_{th}\) | Difference of \(V_{th}\) of the top transistor at between \(V_{pgs} = 0\) and 1 V | V |
| \(\varepsilon_{ox}\) | Oxide dielectric constant | 3.9 |
| \(\varepsilon_{si}\) | Silicon dielectric constant | 11.8 |
| \(\varepsilon_{ILD}\) | ILD dielectric constant | 3.9 |
| \(g_m\) | Transconductance \(g_m = dI_{nds}/dV_{ngs}\) or \(dI_{pds}/dV_{pgs}\) | S |
| \(I_{nds}/I_{pds}\) | Drain-source currents of top/bottom transistors | A |
| \(L_c\) | Contact length | 50 nm |
| \(L_g\) | Gate length | 20/30/50 nm |
| \(L_{LDD}\) | Lightly-doped drain length | 10 nm |
| \(T_{BOX}\) | Buried-oxide thickness | 30 nm |
| \(T_{c}\) | Contact thickness | 6 nm |
| \(T_{g}\) | Gate thickness | 30 nm |
| \(T_{ILD}\) | ILD thickness | variable |
### Table 1. Cont.

| Symbols | Description                                      | Value/Unit |
|---------|--------------------------------------------------|------------|
| $T_{ox}$ | Gate-oxide thickness                             | 0.9/1/1.1 nm |
| $T_{si}$ | Silicon-channel thickness                        | 6 nm |
| $T_{sub}$ | Silicon substrate thickness                      | 50 nm |
| $T_{sw}$ | Sidewall thickness                               | 31 nm |
| $V_{IN}$ | Input voltage of M3INV                            | V |
| $V_{m}$ | Switching threshold voltage of the M3INV          | V |
| $V_{ngs}$ | Gate-source voltages of top/bottom transistors   | V |
| $V_{Lds}$ | Drain-source voltages of top/bottom transistors  | V |
| $V_{OUT}$ | Output voltage of M3INV                          | V |
| $V_{sub}$ | Substrate voltage                                | V |
| $V_{th}$ | Threshold voltage * of the top transistor        | V |

* The threshold voltage $V_{th}$ is defined as $V_{ngs}$ when $I_{ndt} = 10^{-7}$ A.

### 3. DC/AC Characteristics

Figures 2 and 3 show the drain current-gate voltage ($I_{ndt}$-$V_{ngs}$) characteristics of two types of top N-type transistors ($L_G = 20$ and 50 nm) in M3INV-MOS and M3INV-JL at the different gate voltages (=0 and 1 V) of bottom P-type transistor, respectively. The solid lines and dotted lines indicate $I_{ndt}$-$V_{ngs}$ characteristics of top N-type transistors with $L_G = 20$ nm at two different gate voltages (=0 V and 1 V) of the bottom P-type transistors, respectively, and the squares and the circles $I_{ndt}$-$V_{ngs}$ characteristics of top N-type transistors with $L_G = 50$ nm at two different gate voltages (=0 V and 1 V) of the bottom P-type transistors, respectively. Figure 2 show $I_{ndt}$-$V_{ngs}$ characteristics of top N-type MOSFET in M3INV-MOS in the case of $T_{ILD} = 10$ nm and 100 nm, respectively. Figure 3 show $I_{ndt}$-$V_{ngs}$ characteristics of top N-type JLFE in M3INV-JL in the case of $T_{ILD} = 10$ nm and 100 nm, respectively. When $T_{ILD} = 10$ nm, it can be observed that the threshold voltage of top N-type transistors was clearly shifted due to the gate voltage of bottom P-type transistor. On the other hand, in the case of $T_{ILD} = 100$ nm, no threshold voltage shift of top N-type transistors occurs when the gate voltage of bottom P-type transistors changes.

![Figure 2](image-url)

*Figure 2. Current-voltage characteristics of the top N-type metal-oxide-semiconductor field-effect transistor (MOSFET). (a) $I_{ndt}$-$V_{ngs}$ characteristics at $V_{pgs} = 0$ (solid lines and filed circles) and 1 V (dotted lines and empty squares) in the case of ILD = 10 nm and (b) $I_{ndt}$-$V_{ngs}$ characteristics at $V_{pgs} = 0$ (solid lines and filled circles) and 1 V (dotted lines and empty squares) in the case of $T_{ILD} = 100$ nm. The lines and symbols denote $L_G = 20$ and 50 nm, respectively. We use W/L = 0.2/0.03 μm.*
Figure 3. Current-voltage characteristics of the top N-type junctionless field-effect transistor (JLFET). (a) $I_{th}$-$V_{pgs}$ characteristics at $V_{pgs} = 0$ (solid lines and filled circles) and 1 V (dotted lines and empty squares) in the case of ILD = 10 nm and (b) $I_{th}$-$V_{pgs}$ characteristics at $V_{pgs} = 0$ (solid lines and filled circles) and 1 V (dotted lines and empty squares) in the case of $T_{ILD} = 100$ nm. The lines and symbols denote $L_G = 20$ nm and 50 nm, respectively. The channel width $W = 0.2 \mu m$.

Figure 4 show $\Delta V_{th}$, $\Delta V_{gm}$, and $\Delta V_{Cngn}$ versus $T_{ILD}$ at different gate lengths ($L_G = 20$, 30, and 50 nm) of the top N-type transistors in both M3INV-MOS and MOSINV-JL, respectively. The filled and empty symbols denote simulation results of the top N-type transistors in both M3INV-MOS and M3INV-JL, respectively, and the squares, circles, and triangles denote those at $L_G = 20$, 30, and 50 nm, respectively. As $T_{ILD}$ decreases, $\Delta V_{th}$, $\Delta V_{gm}$, and $\Delta V_{Cngn}$ increases at both M3INV-MOS and M3INV-JL. When $T_{ILD}$ is over 30 nm, $\Delta V_{th}$, $\Delta V_{gm}$, and $\Delta V_{Cngn}$ are below 50 mV, the coupling between stacked transistors in both M3INV-MOS [14] and M3INV-JL can be ignored. As $L_G$ increases in both M3INV-MOS and M3INV-JL, $\Delta V_{th}$, $\Delta V_{gm}$, and $\Delta V_{Cngn}$ increase. $\Delta V_{th}$, $\Delta V_{gm}$, and $\Delta V_{Cngn}$ of M3INV-JL has larger than those of M3INV-MOS as $T_{ILD}$ decreases, and the average variations of $\Delta V_{th}$ and $\Delta V_{gm}$ in M3INV-JL are smaller than those in M3INV-MOS as $L_G$ increases, but the variation of $\Delta V_{Cngn}$ does not depend on $L_G$ at both M3INV-MOS and M3INV-JL. As the channel length decreases, $PN^+$ junction in M3DINV-MOS makes the effective channel length decrease, resulting in short-channel effects (SCEs), but the junctionless in M3DINV-JL can make the SCEs decrease [18–20]. Because JLFET is more immune than MOSFET with PN junction in terms of SCE, the average variations of $\Delta V_{th}$ and $\Delta V_{gm}$ in M3INV-JL are smaller than those in M3INV-MOS as $L_G$ decreases. In the case of both M3INV-MOS and M3INV-JL, these results are dependent on the bottom-gate voltage variation ($\Delta V_{pgs}$) are similar to the classical capacitive coupling ratio $\gamma = (\Delta V_{th}/\Delta V_{pgs})$ of asymmetric double-gate (DG) ultra-thin body silicon on insulator (UTB-SOI) MOSFET [21] because both structures of the top N-type transistors in M3INV-MOS and M3INV-JL are similar to one of asymmetric DG UTB-SOI MOSFET. As $T_{ILD}$ decreases, $\gamma$ increases [14,21], as follows.

$$\gamma = \frac{T_{ox} + \frac{\epsilon_{ox} X_{bar}}{\epsilon_{ Si}}}{T_{ILD} + \frac{\epsilon_{ox} X_{bar}}{\epsilon_{ Si}} (T_{SI} - X_{bar})},$$

where $X_{bar}$ means the distance between the front SiO$_2$/Si interface and barycenter location of charge in the silicon channel [22] of the top N-type transistors in both M3INV-MOS and M3INV-JL. Because the barycenter of the top N-type transistors in M3INV-MOS and M3INV-JL are located close to the front SiO$_2$/Si interface and the center in silicon-channel, respectively, $\gamma$ of the top N-type transistors in M3INV-JL is higher than one of M3INV-MOS, as shown in Figure 4. The threshold conditions of M3INV-MOS and M3INV-JL define strongly-inverted and fully-depleted in all the channel, respectively. In the threshold regime of M3INV-MOS and M3INV-JL, the back SiO$_2$/Si interfaces on both top N-type transistors are depleted without any accumulation [21] and inversion [20], respectively.
It is noted that dependence of back-gate voltage for full-depletion in all the channel of M3INV-JL is larger than one for strong inversion of M3INV-MOS.

4. Inverter Characteristics

Mixed-mode circuit simulation of ATLAS was used to verify the inverter characteristics by both M3INV-MOS and M3INV-JL including the electrical coupling.

Figures 5 and 6 show the voltage transfer characteristics (VTC) of M3INV-MOS and M3INV-JL, respectively. Figures 5a and 6a show the simulation results of \( L_G = 20 \) nm and Figures 5b and 6b show those of \( L_G = 50 \) nm. M3INV-MOS shifts VTC from right to left as \( T_{ILD} \) increases, but M3INV-JL shifts VTC from left to right as \( T_{ILD} \) increases.

Figure 7 shows \( \Delta V_m \) versus \( T_{ILD} \) of both M3INV-MOS and M3INV-JL. As \( T_{ILD} \) decreases, \( \Delta V_m \) increases. When \( T_{ILD} \) is over 30 nm, \( \Delta V_m \) are below 10 mV, and thus the coupling in the structures can be ignored. In the case of M3INV-MOS, the larger \( L_G \), the larger \( \Delta V_m \), but in the case of M3INV-JL, the smaller \( L_G \), the larger \( \Delta V_m \).
Figure 5. Voltage transfer characteristics of M3INV-MOS cell with (a) $L_G = 20$ nm and (b) $L_G = 50$ nm. $V_{dd}$ (= 1 V) is DC-biased.

Figure 6. Voltage transfer characteristics of M3INV-JL cell with (a) $L_G = 20$ nm and (b) $L_G = 50$ nm. $V_{dd}$ (= 1 V) is DC-biased.

Figure 7. $\Delta V_m$ of M3INV-MOS and M3INV-JL cells at different channel lengths. Filled and empty symbols denote $\Delta V_m$ of M3INV-MOS and M3INV-JL with $T_{ILD} = 5, 10, 50, \text{and } 100$ nm, respectively.
Figure 8 show the static noise margin (SNM) windows of M3INV-MOS and M3INV-JL with \( L_G = 20 \) nm, respectively. The SNMs were measured as noise margin high (NM\(_H\)) and noise margin low (NM\(_L\)) extracted from VTCs of M3INV-MOS and M3INV-JL. Figure 9 shows the noise margins of M3INV-MOS and M3INV-JL at different \( L_G \)s and \( T_{ILD} \)s. In the case of M3INV-MOS, SNM increases as \( T_{ILD} \) decreases. On the other hand, in the case of M3INV-JL, SNM decreases when \( T_{ILD} \) decreases. When \( T_{ILD} \) is over 30 nm, the maximum variations of SNM of both M3INV-MOS and M3INV-JL are below 20 mV, and thus the coupling in both structures can be also ignored.

Figure 8. Static noise margin (SNM) characteristics of (a) M3INV-MOS cell and (b) M3INV-JL cell. Here \( L_G = 20 \) nm and \( V_{dd} = 1 \) V. Black, red, green, and blue lines denote the coupled voltage transfer characteristics (VTCs) of M3INV-MOS and M3INV-JL with \( T_{ILD} = 5, 10, 50, \) and 100 nm, respectively.

Figure 9. SNMs of M3INV-MOS and M3INV-JL cells at different \( T_{ILD} \)s. Filled and empty symbols denote SNMs of M3INV-MOS and M3INV-JL with \( T_{ILD} = 5, 10, 50, \) and 100 nm, respectively. Squares, circles, and triangles denote SNMs of M3INV-MOS and M3INV-JL with \( L_G = 20, 30, \) and 50 nm, respectively.

Figure 10 show the transient responses of M3INV-MOS and M3INV-JL with \( L_G = 20 \) nm at different \( T_{ILD} \)s, respectively. Table 2 shows the propagation delays extracted from the transient response in Figure 10. As \( T_{ILD} \) decreases, propagation delays of M3INV-MOS and
M3INV-JL increase and decrease, respectively. As $L_G$ increases, propagation delays of both M3INV-MOS and M3INV-JL increase. When $T_{ILD}$ is over 30 nm, the maximum variations of propagation delay of both M3INV-MOS and M3INV-JL are below 0.2 ps, and thus the coupling in the structures can be also ignored.

![Figure 9. SNMs of M3INV-MOS and M3INV-JL cells at different TILDs. Filled and empty symbols denote SNMs of M3INV-MOS and M3INV-JL with $T_{ILD}$ = 5, 10, 50, and 100 nm, respectively. Squares, circles, and triangles denote SNMs of M3INV-MOS and M3INV-JL with $L_G$ = 20, 30, and 50 nm, respectively.](image)

Figure 9. SNMs of M3INV-MOS and M3INV-JL cells at different TILDs. Filled and empty symbols denote SNMs of M3INV-MOS and M3INV-JL with $T_{ILD}$ = 5, 10, 50, and 100 nm, respectively. Squares, circles, and triangles denote SNMs of M3INV-MOS and M3INV-JL with $L_G$ = 20, 30, and 50 nm, respectively.

Table 2. Propagation delay of M3INV-MOS and M3INV-JL at different $L_G$s and $T_{ILD}$s.

| $T_{ILD}$ | $L_G$ | MOS Delay [ps] | MOS Delay [ps] | MOS Delay [ps] | MOS Delay [ps] | JL Delay [ps] | JL Delay [ps] | JL Delay [ps] | JL Delay [ps] |
|-----------|-------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| 5 nm      | 20 nm | 4.42           | 4.18           | 4.56           | 4.58           | 6.56           | 5.84           | 6.42           | 6.93           |
| 10 nm     | 20 nm | 4.39           | 4.82           | 4.52           | 5.21           | 6.5            | 6.42           | 6.93           | 7.01           |
| 30 nm     | 20 nm | 4.37           | 5.43           | 4.49           | 5.57           | 6.43           | 6.42           | 7.01           | 7.06           |
| 50 nm     | 20 nm | 4.36           | 5.52           | 4.48           | 5.7            | 6.42           | 7.01           | 7.06           | 7.13           |
| 70 nm     | 20 nm | 4.35           | 5.55           | 4.47           | 5.72           | 6.41           | 7.06           | 7.13           | 7.19           |
| 100 nm    | 20 nm| 4.34           | 5.57           | 4.46           | 5.74           | 6.4            | 7.1            | 7.19           | 7.25           |

5. Conclusions

In this paper, we investigated the electrical coupling through the threshold voltage, transconductance, and gate capacitance variation according to $T_{ILD}$ of M3INV-MOS and M3INV-JL through TCAD simulation and compared the VTC and $V_m$ and SNM characteristics in M3INV-MOS and M3INV-JL. In both M3INV-MOS and M3INV-JL, $\Delta V_{th}$, $\Delta V_{gm}$, and $\Delta V_{C_{nn}}$ increase as $T_{ILD}$ decreases. The smaller $L_G$, the larger $\Delta V_{th}$ and $\Delta V_{gm}$, but $\Delta V_{C_{nn}}$ is not significant. In addition, as $T_{ILD}$ increased, M3INV-MOS and M3INV-JL shifted VTCs from right to left and from left to right, respectively. The larger $L_G$, the larger and smaller $\Delta V_m$ of M3INV-MOS and M3INV-JL, respectively. The noise margin and inverter characteristics of M3INV-MOS is larger and better than those of M3INV-JL. M3INV-MOS has less electrical coupling in terms of $\Delta V_{th}$, $\Delta V_{gm}$, $\Delta V_{C_{nn}}$, $\Delta V_m$, $N_{MH}$, $N_{ML}$, and propagation delay than M3INV-JL. When $T_{ILD}$ is over 30 nm, $\Delta V_{th}$, $\Delta V_{gm}$, and $\Delta V_{C_{nn}}$ are below 50 mV, $\Delta V_m$ are below 10 mV, the maximum variations of SNM of both M3INV-MOS and M3INV-JL are below 20 mV, and the maximum variations of propagation delay of both M3INV-MOS and M3INV-JL are below 0.2 ps, and thus the coupling in the structures can be ignored.

![Figure 10. Transient responses at different TILDs. (a) M3INV-MOS cell and (b) M3INV-JL cell. Here $L_G$ = 20 nm and $V_{dd}$ = 1 V.](image)

Figure 10. Transient responses at different TILDs. (a) M3INV-MOS cell and (b) M3INV-JL cell. Here $L_G$ = 20 nm and $V_{dd}$ = 1 V.
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