Investigation of a novel 5nm top bottom gated junctionless FinFET for improved switching and analog performance

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Abstract: In this work, we have designed a Novel Top-Bottom Gated Junctionless (JL) Fin-Shaped Field Effect Transistor (FinFET) Structure. The main idea of designing this structure is to improve the output efficiency and reduce the Short Channel Effects (SCEs). This paper analyzes the Analog Performance of a Novel Junctionless FinFET Structure with 5nm Gate length investigated on Silvaco Atlas Technology Computer Aided Design (TCAD) Tools and compared to Conventional Junctionless Bulk FinFET Structure. This Novel JL FinFET has gates on both sides of the substrate, hence the name Top-Bottom Gated (TBG) FinFET. It is determined that the proposed novel device enhances the switching ratio by almost 100 times, hence improving the transconductance and output current. Our device also shows improvement in the output conductance over the conventional JL FinFET. The simulation results show that the Novel TBG JL FinFET structure has better $I_{ON}/I_{OFF}$ and thus reduces the short channel effects than the conventional bulk FinFET more effectively.

Keywords: FinFET, Junctionless, Short Channel Effects, Analog, Switching Ratio, Transconductance.

1. INTRODUCTION

Nowadays the need for electronic devices has grown a lot and new technologies are being invented everyday [1]. The current generation demands for improved performance as well as lower power consumption. Thus the requirement for scaling down these devices and designing more power efficient devices becomes more and more imperative. Downturning the conventional Metal-Oxide Semiconductor (MOS) structures leads to gate losing control over the channel due to Short Channel Effects (SCEs), which leads to device degradation and decreased performance [2]. These short channel effects namely Drain Induced Barrier Lowering (DIBL), Subthreshold Swing and velocity scattering can cause high power consumption and transit time delays [2]. Therefore to improve the gate control over the channel, there is a need for having more than one gate around the channel. Thus FinFET device comes into the picture as it has gate on three sides of the channel and hence reduced short channel effects as compared to the MOSFET devices [3]. Most of the Semiconductor and Electronic Chip Manufacturing companies are turning to FinFET structures for their next generation processors and processing units [4-6]. These FinFET structures can help in further aiding the Moore’s Law for devices having gate length less than 20nm [7]. Consequently in this paper, we have examined the analog performance parameters of a Novel Junctionless (JL) FinFET structure and compared its performance to that of conventional JL FinFET. A novel structure has been reported wherein the gate is wrapped around the channel on three sides but the main feature of the proposed device is the continuation of this three sided gate on top as well as bottom (TBG) of the device. Along with this a
conventional JL FinFET is presented for better comparison. Thus we have proposed this device design for better switching and analog parameters.

2 DEVICE DESIGN AND SIMULATION METHODS

Figure 1 displays the Novel Top-Bottom Gated Junctionless (TBG-JL) FinFET structure. Gates are present on both top and bottom side of the substrate as compared to gate only above the substrate in the case of Conventional Junctionless (JL) FinFET.

In the TBG JL FinFET, the fins are extending on both sides of the substrate, 12nm above the substrate and 5nm below the substrate to have a Top-Bottom Gated Structure. This improves the control of gate over the channel as compared to the conventional Junctionless FinFET thereby enhancing the switching ratio.

The device has 5nm fin width for both top and bottom fins. The gate oxide thickness is kept at 2nm [8].

The simulated n-type TBG JL FinFET device has $5.0 \times 10^{18}$ ($cm^{-3}$) doping concentration for source, channel and drain.

The Table 1 shows the device parameters for the Novel TBG JL FinFET device. The structures have 35nm device length, 20nm source/drain length, 5nm gate length but different device heights. The Conventional JL FinFET has total 25nm device height whereas the Novel TBG JL FinFET has 33nm device height due to addition of an extra fin below the substrate [8].

This proposed device TBG JL FinFET has been simulated on Silvaco Atlas TCAD Simulator [9]. The device simulation in Silvaco Atlas is divided into five main steps, namely the Specification of the Device Structure, Specification of Material Models, Selecting Numerical Models, Specification of the Solution and Analyzing the Results. Structure Specification basically involves defining the mesh grid for the device by using the mesh points and spacing, defining various regions in device, electrode and doping definition for the device. Material Model Specification involves defining the materials to be used in the device and choosing the physical models for the device. Numerical Method Selection is used to decide the mathematical models to be used for device simulation. Further, for solving the device bias conditions, Newton Trap Method is used. The device temperature was kept at $T=300K$ for the analysis on Silvaco TCAD. Solution Specification and Result Analysis uses the extract and solve for running the simulations and extracting the required parameters [9].
3 SIMULATED RESULTS AND DISCUSSION

Several device performance parameters namely Transconductance ($g_m$), Output Conductance ($g_d$), Transconductance Generation Factor (TGF) ($g_m/I_d$), Early Voltage ($V_A$) ($I_d/g_d$) are germane to the discussion while analyzing the Analog Performance of FinFET devices [7].

A switch allows an ON current $I_{ON}$ when it is ON and an OFF current $I_{OFF}$ when it is turned off. And therefore for devices which are designed to operate as switches, we have the same mechanism. For an ideal case the OFF current should be ideally zero and the ON current is decided by the external circuit.

When considering the case of solid state devices that are designed to work as a switch, eg. MOSFET or FinFET transistor, the OFF current is not zero but has a very small value. It is the current passing in the transistor for $V_{gs}=0$ and $V_{ds}=V_{dd}$. Short Channel Effects (SCEs) and leakage current can lead to large values of OFF current when the device is scaled down.

The ON current $I_{ON}$ is decided by the Device Width to Length (W/L) ratio and the excess voltage of the transistor $V_{gs} = V_{th}$ in addition to the mobility of carriers. So it becomes imperative to maximize the $I_{ON}/I_{OFF}$ ratio to reduce transistor losses [10].

Figure 2 depicts the switching ratio ($I_{ON}/I_{OFF}$) of the FinFET structures and clearly indicates that the novel TBG JL FinFET has better switching because of higher ON-current ($I_{ON}$) as compared to conventional JL FinFET structure [1].
Figure 3 depicts the transfer characteristics and transconductance for the conventional JL FinFET and novel TBG JL FinFET device. Threshold voltage ($V_{th}$) for Novel TBG JL FinFET is 0.402 V and for Conventional JL FinFET is 0.404V. It implies that the Novel TBG JL FinFET device has higher drain current which is not as dependent on $V_{ds}$ in the saturation region as compared to conventional JL FinFET. We further notice that on increasing the gate voltage, the drain current keeps on increasing up to saturation. This results in higher transconductance values in the novel TBG JL FinFET device.

Figure 3 shows the transconductance ($g_m$) of FinFETs for the value of gate bias from 0 to 1.8 V.

The expression for transconductance is given by:

$$g_m = \frac{\partial I_d}{\partial V_g}$$

The input conductance (Transconductance) is proportional to the linear gain of a device. It measures the changes in output current with respect to changes in the input voltage$V_{gs}$ while keeping $V_{ds}$as constant [7]. Therefore, the value of $g_m$ is extracted from the slope of the $I_{ds} - V_{gs}$ curve. Novel TBG JL FinFET Device shows higher values of transconductance for same gate voltages as compared to the conventional JL FinFET. Thus the device exhibits superior behaviour in terms of transconductance and thus implies additional control over drain current of input gate voltage.
Transconductance Generation Factor of a device is defined as the ratio of the transconductance of the device to the drain current \[g_m/I_d\] \[7\]. When the device is in the weak inversion regime, it can achieve its highest value of \(g_m/I_d\) \[7\]. Devices having high efficiency should have higher value of Transconductance Generation Factor (TGF).

As the device can operate at lower input voltages, thus it leads to improvement in the device performance. The change in transconductance generation factor with respect to gate voltage is shown in figure 4.

\[\text{Output Conductance } (g_d) = \frac{\partial I_d}{\partial V_d}\]

\[\text{Early Voltage } V_A = \frac{I_d}{g_d}\]

\[\text{Intrinsic Gain } A = \frac{g_m}{g_d}\]

![Figure 4. Variation of Output Conductance \((g_d)\) with Drain Voltage for both devices](image)

By comparing the figures we see that the novel TBG JL FinFET offers higher value of TGF as compared to the Conventional JL FinFET.
Figure 6. Variance of Early Voltage with Drain Voltage for both devices

Early Voltage ($V_A$) is a parameter describing the variation of drain current in the saturation region of operation with Drain Voltage ($V_{ds}$) [7]. An ideal transistor would operate as an ideal current source in the mode of operation where the transistor is capable of amplifying the signals that are applied on its input when it is biased to operate in the active or saturated region of operation [13].

Real transistors show a small increase in their drain current with drain bias ($V_{ds}$). This is due to widening of space charge region in the channel of the MOSFET or FinFET transistor. High value of Early Voltage is preferred for Analog Performance of device [13]. Our device TBG JL FinFET shows higher value of Early Voltage for same values of drain voltage as compared to Conventional JL FinFET structure as seen in figure 6, thus it has better analog performance and amplifying capacity.

Figure 7. Variation of Electric Field for Novel TBG JL FinFET Device

There is an improvement seen with respect to Short Channel Effects for the novel TBG JL FinFET as compared to the conventional structure. Subthreshold Swing for our device is 13.67 mV/decade which is far better than the ideal value of 60 mV/decade at 300K. Thus low values of $g_d$ and high value of $g_m/I_d$ implies that it is a good fit for Analog circuits and Analog Applications [2].

Early Voltage $I_{ON}/I_{OFF}$ ratio and $I_{ON}$ current are high for our Novel TBG JL FinFET device due to the addition of fin at the bottom of the substrate leading to larger dimensions of fin as compared to conventional JL FinFET structure [7, 11].
Figure 7 depicts the superiority of Novel TBG JL FinFET Device as compared to the conventional FinFET structure with respect to hot carrier effects near drain end. The Electric Field near the drain end is considerably low, thus reducing the hot carrier effects up to a huge extent [8]. High electric field near the drain end can lead to heating of the carriers which causes increase in the carrier velocities, thereby increasing their energies. These carriers can cause scattering bringing about device degradation and breakdown.

High Electric Field near the drain end can also lead to other Short Channel Effects (SCEs) such as Velocity Saturation. Velocity Saturation occurs when a strong electric field causes the carriers to reach their maximum velocity [14]. This can lead to decrease in transconductance in saturation mode. The transit time of carriers becomes more, thus leading to delays in switching. Thus our device helps in reducing the short channel effects as it has low electric field near the drain end.

4. CONCLUSION

In this work, analysis of the analog parameters of novel TBG JL FinFET at the gate length of 5nm is done. The novel device (i.e., TBG JL FinFET) shows reduced short-channel effects. Decreased $I_{OFF}$ in case of TBG JL FinFET over the conventional JL FinFET lead to an increase in switching ratio (grown by 100 times). There is also a significant improvement in the drain current and lowered output conductance. The hot carrier effects are also reduced as the Electric Field near the drain end has lower values. Hence for high performance analog applications, our device can be a viable option at gate length of 5nm.

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