Development of Pair Monitor

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The pair monitor is a beam profile monitor at interaction point (IP) for the international linear collider (ILC). We have designed and developed the pair monitor as a silicon pixel sensor which is located at about 400 cm from IP. As the first step to develop the pair monitor, the readout ASIC was developed. In this paper, test results of the readout ASIC and the future plan are reported.

1 Introduction

At ILC, measurement of the beam profile at IP is important to keep high luminosity of $2 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. The beam size at IP is 639 nm, 5.7 nm, and 300 $\mu$m for horizontal ($\sigma_X$), vertical ($\sigma_Y$), and longitudinal beam size ($\sigma_Z$), respectively. Since the beam size, especially $\sigma_Y$, is very small, the beam profile monitor is required to measure the beam size within 1 nm accuracy.

The pair monitor will be used to check the beam profile at the interaction point (IP). Measuring the distribution of the electron-positron pairs generated during the beam crossing \cite{2}. The generated electrons and positrons are scattered by the magnetic field produced by the oncoming beam, which is a function of the transverse size ($\sigma_X$, $\sigma_Y$) and intensity of the beam. For that reason, the deflected particles should carry information of the transverse beam size, especially in their angular distribution. The pair monitor will be located at 400 cm from IP as shown in Fig. \ref{fig1} where is in front of the BeamCal \cite{3}. In our previous studies, the pair monitor has performance to measure the beam size with about 10% accuracy \cite{4}.

We have studied design of the pair monitor and developed the prototype of the readout ASIC. In this paper, test results of the readout ASIC and the future plan are reported.

1.1 Design concept of pair monitor

There are some requirements to the pair monitor to be used for the beam profile monitor at ILC. The pair monitor is required to measure the beam profile at the interaction point, and the measurement results must be feedback to the next train to keep the high luminosity.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure1.png}
\caption{A schematic view of the forward region. The pair monitor will be located in front of the BeamCal, where is about 400 cm from IP.}
\label{fig1}
\end{figure}

LCWS/ILC 2008
For that reason, the pair monitor must measure the hit distributions for train by train, and the data should be readout within the inter-train time (~200 ms). Since the pair monitor will be put at about 400 cm from IP and close to the beam pipe, the radiation dose on the pair monitor becomes large. For example, the radiation dose was estimated as about 10 Mrad/year at the radius of 1.8 cm from the extraction beam pipe in the GLD geometry [5]. Although the radiation dose decreases rapidly for the larger radius, the pair monitor should have radiation tolerance above 1 Mrad/year.

To achieve these requirements, the design concept of the pair monitor was considered. The sensor is assumed as a silicon pixel sensor whose pixel size is $400 \times 400 \mu m^2$ and thickness is about $200 \mu m$. The size of the sensor layer is 10 cm radius. In the sensor layer, two holes for the injection and extraction beam pipes will be prepared, whose radius is 1.0 cm and 1.8 cm, respectively. The total readout channel will be about 200,000. The readout ASIC will be bump-bonded to the sensor, and measures the hit counts on the detector to obtain the hit distributions of the pair backgrounds. At that time, it is not necessary to obtain the information of the energy deposit. Based on this design concept, development of the pair monitor was started.

1.2 Development of readout ASIC

We have developed the readout ASIC for the pair monitor. It is designed to count the number of hits to obtain the hit distribution on the detector. From our previous studies, the statistics for about 150 bunches is enough to extract the beam information on the detector. Therefore, the number of the hit is counted for 16 timing parts in one train, which corresponds to 167 (= 2670/16) bunches in the current nominal ILC design. The hit counts for each timing parts are read within the inter-train time (200 ms). A silicon pixel sensor with the thickness of about $200 \mu m$ is assumed as a detector candidate, whose signal level is about 15,000 electrons. The readout ASIC is designed to satisfy these requirements.

The readout ASIC consists of the distributor of the operation signals, shift register to specify a readout cell, data transfer to the output line, and 36 readout cells. A readout cell consists of the amplifier, comparator, 8-bit counter, and 16 count registers as shown in Fig. 2. They are aligned to 6 x 6 for the X and Y directions. In the previous readout ASIC, MIM (Metal Insulator Metal) capacitors were not prepared at threshold block due to mistake in
the layout mask. Therefore, the signal line between pre-amplifier and differential amplifier was snapped 8.

After modification of layout design, the prototype ASIC was produced with 0.25 µm TSMC process as shown in Fig. 3. Its layout was made by Digian Technology Inc. 6, and the production was done by the MOSIS Service 7. The chip size is 4 × 4 mm², and the readout cell size is 400 × 400 µm². In the readout cells, bonding pads are prepared to attach the sensors by bump-bonding. For the response test of the readout ASIC, the chip is covered with a PGA144 package.

2 Response test of readout ASIC

Figure 4: Output signals from the counter block. TP shows the test-pulse, and Q1, Q2, and Q3 show the counter bit. The hit count is output with Gray code.

For the response test of the readout ASIC, the test system was constructed, based on the VME system. A GNV-250 module was used for the operation and data readout, which was developed as the KEK-VME 6U module. The readout ASIC is attached on the test-board, and connected to the GNV-250 module. Since a FPGA is equipped on the GNV-250 module, logic for data processing could be easily modified. To readout all the hit counts from 16 count registers in each pixel (36 pixels), we prepared a FIFO in the FPGA. All the hit counts are stored in it, then, they are sent to a computer.

At first, the response of the amplifier block was checked. The amplifier block consists of the pre-amplifier, threshold block, and differential amplifier as shown in Fig. 2. The monitor output is prepared to check the internal signals after the pre-amplifier and differential amplifier. In the previous ASIC, the signal from the pre-amplifier could not be sent to the differential amplifier due to the problem in the MIM capacitor. We could observe all the monitor outputs for new readout chip, therefore, the amplifier block was confirmed to works correctly.

For the next step, a function of the counter block was checked. Fig. 4 shows the output signals from the counter block, which was designed to use Gray code. Since the number of the hits was output correctly, the hit count was read from the count registers by a computer. Fig. 5 shows the relation between a number of the input pulse and that of the hit counts read from one of the count registers, which was obtained with about 1 MHz counter rate. It was confirmed that there is no bit lost in the data.

2.1 Pair monitor with SOI technology

For the next step, we plan to develop the pair monitor with SOI (Silicon On Insulator) technology. The SOI technology is the technique to electrically separate the transistors from Si layer. It realizes to prepare the sensor and readout ASIC on the same wafer without bump-bonding. Since we already developed the readout ASIC with usual CMOS technology, its design can be used for the readout circuit. In addition, the circuit is completely free from
latch-up because the device substrates are electrically separated each other. We, however, still need a delicate study on the total ionization dose effect. Even with a deep submicron process on a very thin Si layer, the devices are easy to be affected by a positive charge trapped in a BOX layer.

This project was already started as collaboration with KEK and Tohoku university. For the next production, only the readout ASIC will be developed without a sensor block to check its response independent of the sensor. The design was already fixed, and the first prototype will be delivered in 2009.

2.2 Conclusions

We developed the pair monitor for the beam profile monitor at ILC. The new readout ASIC was developed in 2008 which was modified to implement the MIM capacitor at the threshold block. All the components were confirmed to work correctly by the response test. For the next step, we plan to develop the pair monitor with SOI technology. The first prototype will be developed in 2009.

3 Acknowledgments

The authors would like to thank all the member of the FCAL collaboration [9] for all their help. This study is supported in part by the Creative Scientific Research Grant No. 18GS0202 of the Japan Society for Promotion of Science and promotion of collaborative research programs in universities with KEK.

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Figure 5: The relation between a number of the input pulse (N_{TP}) and that of the hit counts read from one of the count registers (N_{OUT}), which was obtained with about 1 MHz counter rate. No bit lost was observed in the data.