Pixel Detectors

N. Wermes 1
Physikalisches Institut der Universität Bonn, Germany

Abstract

Pixel detectors for precise particle tracking in high energy physics have been developed to a level of maturity during the past decade. Three of the LHC detectors will use vertex detectors close to the interaction point based on the hybrid pixel technology which can be considered the 'state of the art' in this field of instrumentation. A development period of almost 10 years has resulted in pixel detector modules which can stand the extreme rate and timing requirements as well as the very harsh radiation environment at the LHC without severe compromises in performance. From these developments a number of different applications have spun off, most notably for biomedical imaging. Beyond hybrid pixels, a number of monolithic or semi-monolithic developments, which do not require complicated hybridization but come as single sensor/IC entities, have appeared and are currently developed to greater maturity. Most advanced in terms of maturity are so called CMOS active pixels and DEPFET pixels. The present state in the construction of the hybrid pixel detectors for the LHC experiments together with some hybrid pixel detector spin-off is reviewed. In addition, new developments in monolithic or semi-monolithic pixel devices are summarized.

1. Hybrid pixel detectors for the LHC experiments

The truly challenging requirements on detectors operation close to the interaction points at the LHC are on spatial resolution, on timing precision, and most importantly on the long term operation performance and radiation tolerance to particle fluences as high as $10^{15} \text{n}_{eq}/\text{cm}^2$. At present, these demands are only met by so-called hybrid pixel detectors, for which the particle sensing element, the sensor, and the integrated electronics circuitry, the readout chip, are separate entities. They are mated by a hybridization technique, known as bump and flip-chip technology. All of the LHC-collider-detectors ALICE [1,2], ATLAS [3,4], and CMS [5,6], LHCb (for the RICH system) [7] at the LHC, and the CERN fixed target experiment NA60 [8], employ the hybrid pixel technique to build large scale (up to $\sim 2\text{m}^2$) pixel detectors. Pixel area sizes are typically $50 \times 400 \text{µm}^2$ as for ATLAS or $100 \times 150 \text{µm}^2$ as for CMS. The detectors are arranged in cylindrical barrels of 2 to 3 layers and disks covering the forward and backward regions.

A. The sensors

The discovery that oxygenated silicon is more radiation hard, with respect to the non-ionizing energy loss of protons and pions [9] than standard silicon, allows operation of pixel detectors at the LHC for which the radiation is most severe due to their proximity to the interaction point. Sensors with $n^+$ electrodes in n-bulk material have been chosen to cope with the fact that type inversion occurs after about $\Phi_{eq} = 2 \times 10^{12} \text{cm}^{-2}$. After type inversion to p-type bulk material the $pn$-diode sits on the electrode side, from which the depletion zone develops into the bulk, thus allowing the sensor to be operated partially depleted. For the Super-LHC, a name termed for an LHC-upgrade programme which targets a luminosity of $10^{35} \text{cm}^{-2}\text{s}^{-1}$ and hence scales the environment at the LHC by a factor ten in all aspects, new sensor technologies are needed to cope with the radiation hardness demands. Figures 1(a) and (b) show photographs of the sensor wafers of ATLAS and CMS, respectively, which both use oxygenated silicon as the sensor material.
B. The FE electronics

The challenge in the design of the front-end pixel electronics [10] can be summarized by the following requirements: low power (≈ 50 μW per pixel), low noise and threshold dispersion (together ≲ 200e), zero suppression in every pixel, on-chip hit buffering, and small time-walk to be able to assign the hits to their respective LHC bunch crossing. The pixel groups at the LHC have reached these goals in several design iterations using first radiation-soft prototypes, then dedicated radhard designs, and finally using deep submicron technologies. For ATLAS the full production quantity of chip wafers has been processed and tested with an average yield of 82%. CMS yields are in the same order and ALICE chip yields are 51% with a chip area of 13.5 × 15.8 mm². While CMS uses analog readout of hits, ATLAS obtains pulse height information by means of measuring the time over threshold (ToT) for every hit. Figure 2(a) shows the distribution of measured thresholds of an ATLAS front-end chip. The dispersion of about 600 e⁻ can be lowered to below 50 e⁻ by a 7-bit tuning feature implemented in the chip. Figure 2(b) illustrates the effect of time walk for small signals. For efficient signal detection within a defined time of 20 ns with respect to the bunch crossing an overdrive of about 1200e⁻ is necessary. The bunch crossing occurs every 25 ns.

The hit information is extracted as follows: A 40 MHz Gray coded clock is transmitted to all pixel cells. If the pixel circuit detects a hit signal (analog) it generates digital hit information. The hit data (address and time stamp) are transmitted to the bottom of the chip and temporarily stored in end of column buffers outside pixel matrix. The buffers monitor the age of each hit data and delete hits when no trigger coincidence occurs. Hits having their time stamp coincident with the LV1 trigger are finally read out.

![Figure 1. Photographs of the ATLAS (a) and CMS-disks (b) pixel sensor wafers.](image1)

![Figure 2. (a) Dispersion of the pixel thresholds before and after tuning. (b) In-time threshold and overdrive for a typical threshold setting of 4000±200e⁻.](image2)
C. Hybridization

ATLAS pixel modules are hybridized by two vendors (one using indium one solder) at a rate of about up to $2 \times 20$ per week. The fraction of broken, bridged or missing bumps is at the level of $10^{-4}$. Above 85% of all modules have less than 0.1% of bad bumps. About 10-15% of the modules arriving from the vendor have a chip with an unacceptably high number of bump failures and need to be reworked, i.e. removing the FE-chip from the module and flip-chipping of a new one. The success fraction of this operation is 99% for solder and 80% for indium, mostly due to the fact that In-bumps are flatter and remnants of dirt in the reworking process do more harm. The total reject fraction of modules to date is 1% and 14% [14] for PbSn- and Indium bumped modules, respectively.

D. The modules

The CMS and ATLAS modules (cf Fig. 5(a)) typically have $2 \text{ cm} \times 6.5 \text{ cm}$ area consisting of 16 FE-chips bump-connected to one silicon sensor. The I/O lines of the chips are connected via wire bonds to a kapton flex circuit glued atop the sensor. The flex houses a module control chip responsible for front end time/trigger control as well as event building. The total thickness at normal incidence is in excess of 2.5\% $X_0$. The modules are arranged in barrel-ladders or disk-sectors as shown in Fig. 5(b) for the case of ATLAS.

Production pixel modules are scrutinized by extensive tests in the lab, among them their analog and digital functionality, noise and threshold performance, response to an X-ray source scan, as well as temperature cycling of modules and also of assembled ladders. For ATLAS modules, after tuning the threshold spread is well below $100e^-$ and the mean value of the noise distribution is between $150e^-$ and $200e^-$ (cf. Fig. 6). The quadratic sum of both is many sigmas away from the typical threshold setting of $3000e^-$ or above, a requirement at LHC in order to keep the noise hit occupancy low. In order to qualify the modules for their placement inside the ATLAS pixel detector arrangement, a ranking factor based on pixel efficiency, sensor quality, noise and threshold performance, and rework penalty is introduced and a cut is placed to qualify the modules as barrel layer B, 1, or 2 or as disk modules. Based on a sample of about 1300 modules to date 54% of the produced modules meet the most demanding qualification as B-layer modules. Finally, complete ladders of 13 module undergo a so-called system test, i.e. a test procedure involv-
ing the complete readout chain of ATLAS, including micro-cables, conversion into optical signal and clock transmission and their routing over the full cable length in ATLAS. Comparison to module standalone tests show no significant changes in the performance.

E. Radiation tolerance

Most challenging at LHC is the requirement on radiation tolerance of the pixel detector which is exposed to (mostly) pion fluences of \(10^{15} \text{n}_{\text{eq}}/\text{cm}^2\) or 500 kGy during 10 years of LHC operation. The advancement of oxygenated silicon and deep submicron chip technology made a long life time in such an environment possible. Figures 7(a)-(c) show the comparison of critical performance figures before and after irradiation of ATLAS pixel modules. In parts the received dose of the modules was well in excess of that expected for 10 years operation at the LHC. After irradiation to 500 kGy the mean collected charge fraction has been measured to be \(\sim 80\%\) and the in-time efficiency, i.e. the efficiency for hit detection within 20 ns after the bunch crossing, is 97.8 ± 0.1%.

An important characterization figure is the in-time efficiency, which in test beams, at which the arrival of the beam particles is asynchronous to the system clock, can be determined by plotting the hit efficiency as a function of the delay between the arrival time and the clock edge, measured by a TDC. It is mandatory that a high efficiency is reached somewhere inside a plateau. The width and flatness of the plateau is a measure of some kind of margin that exists. The plateau width decreases after irradiation from originally 14 ns to 9.7 ns. Figure 8 shows a comparison between irradiated and not irradiated pixel sensors regarding the amount of trapping. By measuring the charge collection efficiency under inclined angles different depths for the charge deposition in the sensor can be addressed and hence trapping can be studied.
Figure 7. Comparisons of ATLAS pixel modules before and after irradiation to doses up to 100 Mrad. Hit map, noise and threshold dispersions (top), spatial resolution in the 50 µm direction of the pixels at 10° incidence angle (center), and the hit efficiency (bottom). The in-time efficiency of a hit to be earlier than 25 ns is determined in test beams relative to a fixed delay of the trigger counters. The highest point of the plateau shows the in-time efficiency. The width of the plateau characterizes the available margin during operation.

as shown by Fig. 8. After 10 years at the LHC the charge collection efficiency is about 80%. The charge yield as a function of depth can be translated into an electron carrier life time of \( \tau = 4.1 \pm 0.6 \) ns.

F. Support structures and total thickness

For ALICE the demands imposed by the physics are different than for ATLAS and CMS. While the track density (\( \sim 80 \) hits/cm\(^2\)) with 8000 charged particles per rapidity interval for central heavy ion collisions is truly formidable, the radiation level of 5 kGy or \( 6 \times 10^{12} \text{n}_{\text{eq}}/\text{cm}^2 \), due to the much lower collision rate, is much lower than for pp collisions. As a consequence cooling to temperatures below 0°C as for CMS and ATLAS is not mandatory, but instead very thin materials for a small total radiation length are aimed for. The reduced cooling requirement (24°C) allows the use of a very light weight structure with 40µm wall thickness PHYNOX tubes and a total contribution of 0.3%\(X_0\). Together with thin sensors (200 µm) and chips (150 µm) an ALICE module (1.28 cm \( \times \) 7.0 cm, 5 readout chips bonded to one sensor) arrives at a total radiation length per layer of only 0.9%.

Figure 8. Charge collection efficiency as a function of the depth of the track traversing the detector.

Figure 9. Support structures of the ATLAS (carbon-carbon), CMS (carbon-fibre), and ALICE (carbon-fibre) pixel detector global support structures.
The CERN heavy ion experiment NA60 [15] has used LHC-type pixel detectors for the first time in a running experiment. The setup of the NA60 pixel tracker is shown in Fig. 10 (top). For the initial running the ALICE-LHCb chip was used. Eight 4-chip (Fig. 10(bottom left)) and eight 8-chip planes provide track reconstruction with 12 pixel hits on a track. The sensors have been exposed to a radiation dose of 120 kGy and were operated through type inversion. Due to the inhomogeneous irradiation the inner part of the planes has received a larger dose than the outer, which is demonstrated by the hit multiplicity pattern taken with a lowered bias voltage in Fig. 10(bottom right). The improvement in physics from the operation of the pixel vertex detector has been reported in [15]. The Indium target position can be resolved to $20 \mu m$ in the direction transverse to the beam and $200 \mu m$ in the longitudinal direction. The meson resonances $\rho$ and $\omega$ could be detected with a resolution of 23 MeV in the di-muon invariant mass. In 2005, data for p-nucleus running at a beam intensity of $2 \times 10^9$ p/burst and an interaction rate of one per 25 ns has been taken. In order to cope with such LHC-like data rates, four planes using ATLAS production modules were added to the setup.

Figure 10. Pixel detector tracker in the NA60 experiment (top) consisting in total of 16 track hit planes, four of these using ATLAS production modules. The pixel planes(bottom left) were operated through partial type-inversion, with the results demonstrated in the hit-multiplicity plot (bottom right).

II. SPIN-OFF FROM HYBRID PIXEL DETECTORS INTO OTHER FIELDS

A. X-ray imaging using counting pixel detectors

Spin-off from hybrid pixel detectors in particle physics has most directly arisen in imaging applications as detectors that accumulate the incident radiation by the counting of individual radiation quanta in every pixel cell. This technique offers many features which are very attractive for X-ray imaging: full linearity in the response function, in principle an infinite dynamic range, optimal exposure times and a good image contrast compared to conventional film-foil based radiography, thus avoiding over- and under-exposed images. The analog part of the pixel electronics is in parts close to identical to the one for LHC pixel detectors while the periphery has been replaced by counting circuitry [16]. The same principle is also used for protein-crystallography with synchrotron radiation [17,18].

The challenges which are to be addressed in order to be competitive with integrating systems are: high speed ($> 1$ MHz) counting with a range of at least 15 bits, operation with very little dead time, low noise and particularly low threshold operation with small threshold dispersion values. In particular, the last item is important in order to allow homogeneous imaging of soft X-rays of energies in the energy range below 10 keV. It is also mandatory for a differential energy measurement, realized so far as a double threshold with energy windowing logic [19,20,21], which can enhance the contrast of an image as the shape of the X-ray energy spectrum is different behind different absorbers (e.g. bone or soft tissue). Finally, for radiography, high photon absorption efficiency is mandatory, requiring the use and development of high-Z sensors and their hybridization.

The MEDIPIX collaboration [21] uses the MEDIPIX2 chip with $256 \times 256$, $55 \times 55 \mu m^2$ pixels fabricated in a $0.25 \mu m$ technology, energy windowing via two tunable discriminator thresholds, and a 13 bit counter. The maximum count rate per pixel is about 1 MHz. Fig. 11(a) a single chip module together with an image of a bee taken using 14 keV X-rays [21]. A Multi-Chip module with 2x2 chips using high-Z CdTe sensors is shown in Fig. 11(b) using the MPEC chip [22], together with two X-ray images. The MPEC chip features $32 \times 32$ pixels ($200 \times 200 \mu m^2$), double threshold operation, 18-bit counting at $\sim 1$ MHz per pixel as well as low noise.
values (∼120e with CdTe sensor) and threshold dispersion (∼1e after tuning) [23,22]. A technical issue here is the bumping of individual die CdTe sensors which has been solved using Au-stud bumping with Indium-filling [24].

B. Counting pixels in protein crystallography

In protein crystallography with synchrotron radiation [17] the challenge is to image many thousands of Bragg spots from X-ray photons with energies of ∼12 keV (corresponding to resolutions at the 1 Å range) or higher, scattering off protein crystals. This must be accomplished at a high rate (∼1-1.5 MHz/pixel) and by systems with a high dynamic range. The typical spot size of a diffraction maximum is 100 – 200μm, calling for pixel sizes in the order of 100 – 300μm. The high linearity of the hit counting method and the absence of so-called “blooming effects”, i.e. the response of non-hit pixels in the close neighborhood of a Bragg spot, makes counting pixel detectors very appealing for protein crystallography experiments. Counting pixel developments are made for the ESRF (Grenoble, France) [25] and the SLS (Swiss Light Source at the Paul-Scherrer Institute, Switzerland) beam lines. A photograph of the PILATUS 1M detector [26] at the SLS (∼10^6 217μm×217μm pixels, 18 modules, 20×24 cm^2 area) is shown in Fig. 12(a).

A systematic limitation and difficulty is the problem that homogeneous hit/count responses in all pixels, also for hits at the pixel boundaries or between pixels where charge sharing plays a role must be maintained by delicate threshold tuning (cf Fig. 12(b)). Fig. 12(c) shows a flat-field image obtained with a PILATUS module, which demonstrates that this principle problem can be overcome [27]. Figure 12(d), shows some Bragg spots obtained with a 10s exposure to 12 keV synchrotron X-rays [28]. Some spots are contained in only one pixel, others spread over a few pixels due to charge sharing. This demonstrates the intrinsically good point resolution of the system. Figure 12(e) is a reconstructed electron density map of the thaumatin crystal [27]. Alternative developments which aim to improve the active/inactive area ratio for protein-crystallography X-ray detection are so-called 3-D silicon sensors (strip or pixels) [29]. A detailed account can be found in [30].

III. CHALLENGES IMPOSED BY A SUPER-LHC

The radiation levels expected at an LHC upgrade, called Super-LHC or SLHC, are a factor of ten higher than at the LHC, i.e. to 10^{16} n_{eq}/cm^2. There are mainly three effects as a consequence [31].

1. A change of the effective doping concentration (higher depletion voltage necessary, under-depletion)
2. An increase of leakage current (increase of shot noise, thermal runaway)
3. An increase of charge carrier trapping (loss of charge)

Several routes to cope with this are being pursued, among them the development of even more radiation hard silicon based on oxygenated float-zone (DOFZ), Czochralski (Cz) and epitaxial silicon [31]. For this review I would like to address in this context two new approaches which are more linked to pixel detectors: diamond pixel detectors and 3D-silicon devices.

A. Diamond Pixels

CVD-Diamond as a sensor material has been developed by the CERN R & D group RD42 for many years [32]. Charge collection distances approaching 300 μm has also triggered the development of a hybrid pixel detector using diamond as sensors [33,34]. The non-uniform field distribution inside CVD-diamond, which originates from the grain structure in the charge collecting bulk (cf. Fig. 14(a)) introduces polarization fields inside the sensor due to charge
trapping at the grain boundaries which superimpose on the biasing electric field. This results in position dependent systematic shifts in the track reconstruction with a typical average grain size of 100µm - 150µm [35]. Diamond sensors with charge collection distances in excess of 300µm have been fabricated and tested [36]. Single chip pixel modules as well as a full size wafer scale 16-chip module assembled using ATLAS front-end chips have been built and tested. Figure 13(a) and (b) show the diamond pixel detector and a hit response pattern obtained by exposing the detector to a $^{109}$Cd source of 22 keV $\gamma$ rays, which deposits approximately 1/4 of the charge of a minimum ionizing particle. The single chip module has been tested in a high energy (180 GeV) pion beam at CERN, the module in a $\sim$4 GeV electron beam at DESY. Figure 13(c) and (d) show position correlation and the charge distribution of the diamond pixel detector in a high energy beam, respectively. A spatial resolution of $\sigma = 12$µm has been measured with the single chip module at high energies with 50µm pixel pitch. A technical challenge to produce a wafer scale module lies in the hybridization process, i.e. bump deposition and flip-chipping. Figure 14 shows the 16-chip diamond module (Fig. 14(b)) and its tuned threshold map (Fig. 14(c)) with a very small dispersion of only 25e$^-$ and good bump yield homogeneity. One chip was damaged during test beam by electrostatic discharge. The rms of the position residuals was measured to 24 µm in the DESY 6 GeV beam [34]. This value is dominated by the multiple scattering contribution from the beam telescope.
B. 3D silicon sensors

So-called 3D silicon detectors have been developed [29] to overcome several limitations of conventional planar Si-pixel detectors, in particular in high radiation environments, in applications with inhomogeneous irradiation and in applications which require a large active/inactive area ratio such as protein crystallography [18]. A 3D-Si-structure (Fig. 15(a)) is obtained by processing the n⁺ and p⁺ electrodes into the detector bulk rather than by conventional implantation on the surface. This is done by combining VLSI and MEMS (Micro Electro Mechanical Systems) technologies. Charge carriers drift inside the bulk parallel to the detector surface over a short drift distance of typically 50µm. Another feature is the fact that the edge of the sensor can be a collection electrode itself thus extending the active area of the sensor to within few µm to the edge. Edge electrodes also avoid inhomogeneous fields and surface leakage currents which usually occur due to chips and cracks at the sensor edges. The main advantages of 3D-silicon detectors, however, come from a different way of charge collection and the fact that the electrode distance is short (50µm) in comparison to conventional planar devices at the same total charge. This results in a fast (1-2 ns) collection time, low (< 10V) depletion voltage and, with edge electrodes in addition, a large active/inactive area ratio of the device (cf. Fig. 15(b)).

The technical fabrication is much more involved than for planar processes and requires a bonded support wafer and reactive ion etching of the electrodes into the bulk. A compromise between 3D and planar detectors, so called planar-3D detectors maintaining the large active area, use planar technology but with edge electrodes [37], obtained by diffusing the dopant from the deeply etched edge and then filling it with poly-silicon. Prototype detectors using strip or pixel electronics have been fabricated and show encouraging results with respect to speed (3.5 ns rise time) and radiation hardness (≫ 10¹⁵ protons/cm²) [38]. 3D-pixel detectors with LHC-type frontend electronics have not been successfully built yet, although the hybridization imposed no problem compared to standard hybrid pixel devices. A fabrication of 3D-pixel structures adapted to the ATLAS FE-chip is underway [39].

IV. MONOLITHIC AND SEMI-MONOLITHIC PIXEL DETECTORS

Monolithic pixel detectors, in which amplifying and logic circuitry as well as the radiation detecting sensor are one entity, are in the focus of present developments. To reach this ambitious goal, optimally using a commercially available and cost effective technology, would be another breakthrough in the field. The present developments have been much influenced by R&D for vertex tracking detectors at future colliders such as the International Linear e⁺e⁻ Collider (ILC) [40]. Very low (≪1% X₀) material per detector layer, small pixel sizes (∼20µm × 20µm) and a high rate capability (80 hits/mm²/µs) are required, due to the very intense beamstrahlung of narrowly
focussed electron beams close to the interaction region, which produce electron positron pairs in vast numbers. High readout speeds with typical line rates of several 10 MHz and a 40\(\mu\)s frame readout time are necessary.

At present, two developments have already reached some level of maturity: so called CMOS active pixels and DEPFET pixels. Other promising approaches, not mentioned in this review, are amorphous a-Si:H layers for charge collection superimposed on standard CMOS ASICS [41] as well as so called SOI-sensors [42], which use a high-ohmic Si-substrate with full charge collection wafer-bonded to a CMOS electronics layer. Both active layers (sensor and CMOS) are isolated by an insulating layer through which a via-contact is made. These concepts are still in their early development phases but offer new possibilities once larger scale production is mastered.

### A. CMOS active pixels

In some CMOS chip technologies a lightly doped epitaxial silicon layer of a few to 15\(\mu\)m thickness between the low resistivity silicon bulk and the planar processing layer can be used for charge collection [43,44,45]. The generated charge is kept in a thin epi-layer atop the low resistivity silicon bulk by potential wells that develop at the boundary and reaches an n-well collection diode by thermal diffusion (cf. Fig. 16(a)). With small pixel cells collection times in the order of 100 ns are obtained. The charge collecting epi-layer is – technology dependent – at most 15\(\mu\)m thick and can also be completely absent. The attractiveness of active CMOS pixels lies in the fact that standard CMOS processing techniques are employed and hence they are potentially very cheap. CMOS active pixel sensor development are pursued by many groups which partially collaborate in various projects (BELLE-upgrade,STAR-upgrade,ILC,CBM at GSI) who use similar approaches to develop large scale CMOS active pixels, also called MAPS (Monolithic Active Pixel Sensors) [44]. A recent review can be found in [46]. The sensor is depleted only directly under the n-well diode. The signal charge is hence very small (<1000e) and full charge collection is obtained only in the depleted region under the n-well electrode (cf Fig. 16(b)). Low noise electronics is therefore the challenge in this development. Matrix readout of MAPS is performed using a standard 3-transistor circuit (line select, source-follower stage, reset) commonly employed by CMOS matrix devices, but can also include current amplification and current memory [47]. In the active areas only nMOS transistors are permitted because of the n-well/p-epi collecting diode which does not permit other n-wells. For an image two complete frames are subtracted from each other (correlated double sampling, CDS) to eliminate base levels, 1/f and fixed pattern noise (see Figure 17). In a second step pedestals and common mode noise are subtracted to extract the signal and to determine the remaining noise. Detector sizes up to 19.4\(\times\)17.4 mm\(^2\) with 1M pixels have been tested. The smallest pixel pitch was 17\(\mu\)m. Frame speeds of 10\(\mu\)s for 132x48 pixels have been reached for the BELLE development, with a noise figure of 30-50e\(^-\) [48]. With other pixel matrices with slower readout noise values of 15-20 e\(^-\), S/N ratios larger than 20 and spatial resolutions of 1.5\(\mu\)m (5\(\mu\)m) for 20\(\mu\)m (40\(\mu\)m) pitch have been measured [46]. The presently favored technology is the AMS 0.35\(\mu\)m OPTO process, which possesses a 10\(\mu\)m thick epitaxial layer. Regarding radiation hardness MAPS appear to sustain non-ionizing radiation (NIEL) to \(~10^{12}\) n\(\text{eq}\). The effects of ionizing radiation damage (IEL), the main damage source at the ILC, are thresh-
old shifts and leakage currents in and between nMOS transistors. The damage effects are less severe when short readout integration times ($\sim 10 \mu s$) are used. This way doses of about 10 kGy can be tolerated [46].

The present focus of further development lies in improving the radiation tolerant design, making 50$\mu$m thin detectors, making larger area devices for instance by stitching over reticle boundaries [49], and increasing the charge collection performance in the epi-layer by triple-well [50] or other techniques [51,52,53].

B. DEPFET pixels

In so-called DEPFET pixel sensors [54] FET transistor is implanted in every pixel on a sideway depleted [55] bulk. Electrons generated by radiation in the bulk are collected in a potential minimum underneath ($\sim 1\mu$m) the transistor channel (internal gate) thus modulating its current (Fig. 18). Electrons collected in the internal gate are completely [56] removed by a clear pulse applied to a dedicated contact outside the transistor. Amplification values of $\sim 300$ pA per collected electron in the internal gate have been achieved. Further current amplification and storage enters at the second level stage. The bulk is fully depleted yielding large signals and the small capacitance of the internal gate offers low noise operation, for a very large S/N ratio. This in turn can be used to fabricate very thin devices. Thinning of pn-diodes to a thickness of 50$\mu$m using a technology based on wafer bonding and deep anisotropic etching has been successfully demonstrated [57].

DEPFET pixels are being developed for three very different application areas: vertex detection in particle physics [58,59,60], X-ray astronomy [61,62] and for biomedical autoradiography [63]. With single pixel structures noise figures below 5e$^-$/ and energy resolutions of 131 eV for 6 keV X-rays have been obtained at room temperature [64]. The challenges for an ILC vertex detector are: small pixel cells ($\sim 20 \times 30 \mu m^2$), thin, radiation hard sensors ($\sim 50\mu$m), and fast readout ($\geq 10$-20 MHz per matrix row of 520x4000 pixels). This is pursued by a Bonn-Mannheim-MPI Munich collaboration.

Readout of a DEPFET matrix is done by selecting a row by a gate voltage from a sequencer chip (SWITCHER) to the external gate. The drains are connected column-wise delivering their current to a current-based readout chip (CURO) with amplification and current storage at the bottom of the column [65,64]. Both chips have been developed at close to the desired speed for a Linear Collider. A sketch of a module made of DEPFET sensors is shown in fig. 19(top). Figure 19(bottom) shows a DEPFET pixel matrix readout system used in the testbeam.

The radiation tolerance, in particular against ionizing radiation, which is expected to doses of 2 kGy due to beamstrahlung at the ILC, again is a crucial question. Irradiation with 30 keV X-rays up to doses of $\sim 10$ kGy, about five times the amount expected at the ILC, have lead to transistor threshold shifts of only about 4 V. Threshold shifts of this order can be coped with by an adjustment of the corresponding gate voltages supplied by the SWITCHER chip. The estimated power consumption for a five layer DEPFET pixel vertex detector at the ILC – assuming a power duty cycle of 1:200 – is only $\sim 5W$. Such a performance renders a very low mass detector without cooling pipes feasible.

A DEPFET pixel matrix with $128 \times 64$ pixels has
Figure 19. (top) Sketch of a ILC first layer module with thinned sensitive area supported by a silicon frame. The enlarged view shows a DEPFET matrix and a DEPFET double pixel structure, respectively, (bottom) photographs of a DEPFET matrix readout system (left). The sequencer chips (SWITCHER II) for select and clear are placed on the sides of the matrix, the current readout chip (CURO II) at the bottom; (right) stack of the hybrid together with readout, ADC, and control boards operated in the testbeam.

been tested in a 6 GeV electron beam at DESY. The noise values obtained for the full system in the test beam including sampling noise of the CURO chip is $225\,e^{-}$ (see Fig. 21(a)). The S/N ratio is 144.

Figure 20 shows a hit in the DEPFET matrix together with two typical events with different hit clusters. The event on Fig. 20(right) is most likely explained by and consistent with the emission of a delta-ray which remains in the sensor. This also qualitatively demonstrates the good reconstruction capabilities to be expected from a DEPFET vertex detector. At 6 GeV beam energy the spatial residuals are still multiple scattering dominated. Residuals on the order of $10\,\mu m$ are obtained, while with the large S/N value of 144 true space resolutions in the order of $2\,\mu m$ should be possible.

V. SUMMARY

The large pixel detectors for LHC experiments, based on the hybrid pixel technology, constitute the state of the art in pixel detector technology. These detectors are in construction and the maturity of the technology, including radiation tolerance to 500 kGy doses, has been proven. Immediate spin-off developments are hybrid pixel detectors with counting capability in which radiation quanta are individually counted. These developments open up a new approach to radiological imaging as well as to protein crystallography with synchrotron radiation. Monolithic or semi-monolithic detectors, in which detector and readout ultimately are one entity, are currently being developed in various forms, largely driven by the needs for particle detection at the ILC. Most mature at present are CMOS active pixel sensors using standard commercial technologies on low resistivity bulk, and DEPFET-pixels, which maintain high bulk resistivity for charge collection.
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