Mitigation of Arsenic Contamination on the Back Side of Si Wafer Using SiO$_2$ Protection Layer for III-V on Si Heterogeneous Epitaxy

Sung-Kyu Lim,a,b Do-Kwyn Kim,c,d Hae-Chul Hwang,a Jin-Su Kim,a Won-Sang Park,c Young-Dae Cho,d Chan-Soo Shin,a Won-Kyu Park,d Jung-Hee Lee,f Dae-Hyun Kim,c,z and Hi-Deok Lee.b

aNational Nano Fab Center, Daejeon 305-338, Korea 
bDepartment of Electronics Engineering, Chungnam National University, Daejeon, Korea 
cSchool of Electronics Engineering, Kyungpook National University, Daegu, Gyeongbuk 702-701, Korea 
dKorea Advanced Nano Fab Center, Suwon, Gyeonggi 443-270, Korea 

In this paper, we have investigated a pathway to mitigate the arsenic (As) cross-contamination on a back side Si wafer during GaAs growth by metal-organic chemical vapor deposition (MOCVD). Without a proper protocol doing a III-V on Si heterogeneous epitaxy, we have observed high levels of the As concentration on the back side Si wafer, easily in excess of $1 \times 10^{16}$ atoms/cm$^2$ by secondary ion mass spectrometry (SIMS) analysis and $10^{15}$ atoms/cm$^2$ by total reflection X-ray fluorescence (TXRF) analysis, after GaAs growth on Si. This known level of contamination on wafers would disqualify them for fabrication in existing Si VLSI fabs. In order to mitigate the As cross-contamination, we have proposed a SiO$_2$ protection layer on the back side of the Si wafer. From both SIMS and TXRF analysis, the proposed scheme has dramatically lowered the back side as concentration to $1.5 \times 10^{10}$ atoms/cm$^2$ by SIMS and $1.0 \times 10^{10}$ atoms/cm$^2$ by TXRF.

© The Author(s) 2016. Published by ECS. This is an open access article distributed under the terms of the Creative Commons Attribution 4.0 License (CC BY, http://creativecommons.org/licenses/by/4.0/), which permits unrestricted reuse of the work in any medium, provided the original work is properly cited. [DOI: 10.1149/2.0351606jss] All rights reserved.

Manuscript submitted December 9, 2015; revised manuscript received April 18, 2016. Published April 27, 2016.

Results and Discussion

In this work, we have observed high levels of the As concentration on the back side Si wafer during GaAs growth by metal-organic chemical vapor deposition (MOCVD). Without a proper protocol doing a III-V on Si heterogeneous epitaxy, we have observed high levels of the As concentration on the back side Si wafer, easily in excess of $1 \times 10^{16}$ atoms/cm$^2$ by secondary ion mass spectrometry (SIMS) analysis and $10^{15}$ atoms/cm$^2$ by total reflection X-ray fluorescence (TXRF) analysis, after GaAs growth on Si. This known level of contamination on wafers would disqualify them for fabrication in existing Si VLSI fabs. In order to mitigate the As cross-contamination, we have proposed a SiO$_2$ protection layer on the back side of the Si wafer. From both SIMS and TXRF analysis, the proposed scheme has dramatically lowered the back side as concentration to $1.5 \times 10^{10}$ atoms/cm$^2$ by SIMS and $1.0 \times 10^{10}$ atoms/cm$^2$ by TXRF.

Experimental

Two different types of 200-mm Si wafers with (001) orientation were prepared to evaluate the back side as cross-contamination after an 1.5-μm-thick GaAs layer was grown by MOCVD. One is without SiO$_2$ protection layer, and the other with 200 nm-thick SiO$_2$ protection layer deposited by plasma-enhanced chemical-vapor-deposition (PECVD) on the back side Si wafer. The MOCVD toolset used in this work is Aixtron-Crius which is capable of growing III-V materials on 300-mm Si wafers. Here, the reasons why we chose the GaAs are as follows: i) It has about 4% lattice mismatch to Si, which makes the selective growth of the GaAs on the Si wafer somewhat easier, and ii) It is very popular to grow GaAs layers by MOCVD for optoelectronic applications. Growth procedures for the GaAs layer are as follows: after dipping in 100:1 HF solution for 30 sec, a thermal cleaning of the Si surface was performed at 730°C for 5 min in the H$_2$ ambient to remove native oxides in the MOCVD reactor. Subsequently, the substrate temperature decreased to 400°C to uniformly initiate the nucleation of the GaAs seed layer, followed by high-temperature GaAs bulk-growth at 670°C, 160 mbar. We have prepared four different samples to analyze the As contamination: Sample-A without oxide protection layer after GaAs growth, Sample-B without oxide protection layer after etching grown GaAs by wet chemical, Sample-C with oxide protection layer after GaAs growth, and Sample-D with oxide protection layer after etching the oxide protection layer by HF chemical solution. More details are provided in the next section.

In order to investigate the contaminations on the back side of two Si wafers, we have performed the transmission electron microscopy...
As expected, the use of the amorphous SiO2 protection layer on the back side Si wafer is too small to be inspected by SEM and optical microscope. Instead, we show in Fig. 1a. However, those parasitic crystalline GaAs particle growths and formations on the back side Si wafer, as shown in Fig. 1a, sample-A) and with SiO2 protection layer (Fig. 1c, sample-C). In each case, we dipped both wafers into a mixture of H3PO4/H2O2/DI (1/1/25) for 10 min after GaAs growth, aiming to intentionally etch the 1.5 μm-thick GaAs layers (Fig. 1b, sample-B). Finally, we dipped the sample-B wafer into an HF solution to etch the SiO2 protection layer (Fig. 1d, sample-D). After GaAs growth on bare Si wafers by MOCVD, it can be seen that there were significant amounts of parasitic crystalline GaAs particle growths and formations on the back side Si wafer, as shown in Fig. 1a. However, those parasitic crystalline GaAs particles are too small to be inspected by SEM and optical microscope. Instead, we used the TEM analysis to visually identify those particles to begin with. As expected, the use of the amorphous SiO2 protection layer on the back side of the Si wafer was effective in mitigating the parasitic growth of the GaAs layer since the adsorption of reactant species such as As and Ga would be reduced on the amorphous SiO2 protection layer. This prohibits the nucleation of GaAs layers on the back side. Also, the use of the SiO2 protection layer prevents pre-contaminated As particles from the susceptor of the MOCVD from diffusing into the Si wafer. At each stages, both SIMS and TXRF measurements were utilized to look into the distribution of the As atoms across the back side of the wafer. Figures 2a and 2b show the distribution profile of the As concentration from the back side of the Si wafer along the depth direction, by SIMS. Here, the primary raster size is 130 × 130 μm² and secondary analysis area has a diameter of 63 μm, respectively. For the wafer without SiO2 protection layer, the As concentration is excessive on the back side, since the regions of the single-crystallized parasitic GaAs growth and cross-contaminations of the As from the susceptor occur, as discussed earlier. Interestingly, we find that there still exist significant amounts of the As atom distribution as high as 2 × 10^{20} atoms/cm² on the back side surface of the Si wafer, even after we etch the wafer in a mixture of a H3PO4/H2O2/DI solution to remove the grown GaAs materials. This is because the As atoms have already been diffused into the Si wafer during GaAs growth at high temperature. As a result, there are a lot of As atoms inside the back side Si wafer with around 100 nm depth. However, when the SiO2 protection layer is used on the back side prior to the GaAs growth, it leads to more than 10³ times reduction in the As contamination on the back side of the Si wafer, as shown in Fig. 2b. After etching the SiO2 protection layer by HF, it is also confirmed that the level of the back side As concentration measured by SIMS is less than 10^{13} atoms/cm² (Fig. 2b). Figure 3 shows the areal As concentration on the back side Si wafers by TXRF, using spot measurements with area of 500 μm² and scan duration of 500 sec. Compared to the average value of the Si wafers without SiO2 protection layer (sample-A and -B), the As contamination of sample-B which has the H3PO4-based wet etching, yields a reduction from 1.97 × 10^{14} atoms/cm² (sample-A) to 1.08 × 10^{14} atoms/cm² (sample-B) which is similar to the...
As contamination significantly decreases to 1.53 $\times 10^{10}$ atoms/cm$^2$ by MOCVD, in realizing the heterogeneous integration of InGaAs materials onto Si platform. In trying to eliminate this, we have successfully proposed the protocol using the SiO$_2$ protection layer on the back side and its removal process by HF solution. Having this protocol employed, the back side As concentration decreases to 1.0 $\times 10^{10}$ atoms/cm$^2$ by TXRF. The results of this work show how to minimize contamination on the back side of Si wafers after III-V epitaxy, which will be an essential requirement for their introduction into VLSI infrastructures.

**Acknowledgments**

This work was supported by both grants from the R&D Program funded by the Ministry of Science, ICT and future planning (MSIP), (grant No. NRF-2014M3A7B5073451) and the BK21 Plus program at Kyungpook National University funded by the Ministry of Education (21A20131600011). Both Sung-Kyu Lim and Do-Kywn Kim contributed equally to this work.

**References**

1. R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, M. Metz, and M. Radosavljevic, “Benchmarking nanotechnology for high-performance and low-power logic transistor applications,” *IEEE Trans. Nano.*, 4(2), 153, (2005).
2. M. Rodwell, “Technology development and design for 22 nm InGaAs/InP-channel MOSFETs,” in *Proc. 18th IEEE IPRM Conf.*, May 2008, pp. 1.
3. D.-H. Kim, J. A. del Alamo, J.-H. Lee, and K.-S. Seo, “Performance evaluation of 50 nm In0.7Ga0.3As HEMTs for beyond-CMOS logic applications,” in *IEDM Dig.*, 2005, pp. 767.
4. D. Antoniadis and A. Khakifrooz, “MOSFET performance scaling: Limitations and future options,” in *IEDM Dig.*, 2008, pp. 253.
5. S. Datta, T. Ashley, J. Brask, L. Buckle, M. Doczy, M. Emery, D. Hayes, K. Hilton, R. Jeffries, T. Martin, T. J. Phillips, D. Wollis, P. Wilding, and R. Chau, “85 nm

---

**Figure 4.** 2D mapping of As areal concentration for back side Si wafers by TXRF (sample-A, -B, -C and –D).

---

Conclusions

In this work, we have observed the significant As cross-contamination on the back side of the Si wafer after GaAs growth by MOCVD, in realizing the heterogeneous integration of InGaAs materials onto Si platform. In trying to eliminate this, we have successfully proposed the protocol using the SiO$_2$ protection layer on the back side and its removal process by HF solution. Having this protocol employed, the back side As concentration decreases to 1.0 $\times 10^{10}$ atoms/cm$^2$ by TXRF. The results of this work show how to minimize contamination on the back side of Si wafers after III-V epitaxy, which will be an essential requirement for their introduction into VLSI infrastructures.
gate length enhancement and depletion mode InSb quantum well transistors for ultra high speed and very low power digital logic applications,” in *IEDM Dig.*, 2005, pp. 763.

6. N. Waldron, C. Merckling, W. Guo, P. Ong, L. Teugels, S. Ansari, D. Tsvetanova, F. Sebahi, D. H. van Dorp, A. Milein, D. Lin, L. Nyns, J. Mitard, A. Pourghaderi, B. Douhard, O. Richard, H. Bender, G. Boccardi, M. Caymax, M. Heyns, W. Vandervorst, K. Barla, N. Collaert, and A. V.-Y. Thean “An InGaAs/InP Quantum Well FinFet Using the Replacement Fin Process Integrated in an RMG Flow on 300 mm Si Substrates,” in *VLSI Tech. Dig.*, 2014, pp. 1.

7. N. Waldron, G. Wang, N. D. Nguyen, T. Orzali, C. Merckling, G. Brammertz, P. Ong, G. Winderickx, G. Hellings, G. Eneman, M. Caymax, M. Meuris, N. Horiguchi, and A. Thean, “Integration of InGaAs Channel n-MOS Devices on 200 mm Si Wafers Using the ART Technique,” *ECS Trans.*, 45(4), 115 (2012).

8. K. Saga, R. Ohno, D. Shibata, S. Kobayashi, and K. Surokah “Behavior of Transition Metals Penetrating Silicon Substrate through SiO2 and Si3N4 Films by Arsenic Ion Implantation and Annealing” *ECS J. Solid State Sci. and Tech.*, 4(5), 131 (2015).

9. M. Takiyama “Influence of Metallic Contamination on LSI Fabrication,” *Nippon Steel Technical Report*, no. 83, 2001, pp. 95.