Upgrade of Tile Calorimeter of the ATLAS Detector for the High Luminosity LHC.

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Abstract.

The Tile Calorimeter (TileCal) is the hadronic calorimeter of ATLAS covering the central region of the ATLAS experiment. TileCal is a sampling calorimeter with steel as absorber and scintillators as active medium. The scintillators are read out by wavelength shifting fibers coupled to photomultiplier tubes (PMT). The analogue signals from the PMTs are amplified, shaped and digitized by sampling the signal every 25 ns. The High Luminosity Large Hadron Collider (HL-LHC) will have a peak luminosity of $5 \times 10^{34} cm^{-2} s^{-1}$, five times higher than the design luminosity of the LHC. TileCal will undergo a major replacement of its on- and off-detector electronics for the high luminosity programme of the LHC in 2026. The calorimeter signals will be digitized and sent directly to the off-detector electronics, where the signals are reconstructed and shipped to the first level of trigger at a rate of 40 MHz. This will provide a better precision of the calorimeter signals used by the trigger system and will allow the development of more complex trigger algorithms. Three different options are presently being investigated for the front-end electronic upgrade. Extensive test beam studies will determine which option will be selected. Field Programmable Gate Arrays (FPGAs) are extensively used for the logic functions of the off- and on-detector electronics. One hybrid demonstrator prototype module with the new calorimeter module electronics, but still compatible with the present system, may be inserted in ATLAS at the end of 2016.

1. Introduction

ATLAS (A Toroidal LHC ApparatuS) [1] is a general purpose detector designed to study proton-proton and heavy ions collisions at the Large Hadron Collider (LHC) at CERN (Geneva, Switzerland). The ATLAS hadronic Tile Calorimeter (TileCal) [2] is a sampling calorimeter composed of steel plates and approximately 460000 plastic scintillator tiles. It is divided longitudinally in four cylindrical sections; the two central “long barrel” segments (LBA, LBC) and shorter “extended barrel” segments (EBA, EBC) at each end (figure 1). Each cylindrical section is composed of 64 wedge-shaped modules, and the scintillators in each module are divided into individual cells. Light from the side of each cell is collected by wavelength shifting fibers, and read out by two photomultiplier tubes (PMTs) located in insertable “drawers” within the back girders of each module, along with the high-voltage and readout electronics. A total of 9852 PMTs are needed for the complete readout of TileCal (figure 1).

In order to maximize the physics potential of the LHC, the accelerator and detectors are being upgraded [4] for an instantaneous luminosity of around $5 \times 10^{34} cm^{-2} s^{-1}$ and a total integrated luminosity of 3000 $fb^{-1}$ over ten years of running. This will present significant challenges for
ATLAS data taking, with increased pileup from close to 200 simultaneous events per bunch crossing. An upgrade program to replace the current TileCal on- and off-detector electronics is underway in order to meet the new requirements for high-luminosity running. The upgrade aims include improving the latency, achieving high readout rates, helping to improve event selection and coping with the higher radiation levels.

2. The demonstrator

The on-detector TileCal electronics [3] are installed along with the PMTs in one so-called “super drawer” per module. In the current system, each super drawer is mechanically divided into two “drawers” that function together as a single unit. Analog PMT signals are amplified and shaped in front-end boards and then sent to boards where the pulses are digitized and stored in pipeline buffers to await readout upon a level-1 trigger accept. In a separate signal path, projective “towers” of calorimeter cells are summed into single analog pulses that are sent to the Level-1 Calorimeter Trigger (L1Calo) for event selection. Data from events selected by the Level-1 trigger are read out over optical links by interface boards to the off-detector Read Out Drivers (ROD). Optical fibers from the Timing Trigger and Control (TTC) system provide each module with clocks, trigger signals, and control and configuration capabilities. The High Voltage (HV) system and Low Voltage Power Supply (LVPS) are controlled and monitored by the Detector Control System (DCS).

For Phase II the aim is to replace the current system with a more modularized one, in which each superdrawer (figure 2) comprises four independent “mini-drawers” for simplified access and service (figure 1). The signals from the PMTs will be shaped and amplified in the front-end boards (FEB) behind each PMT and digitized in the “main board” present in each mini-drawer. A “daughter board” will read out the sampled data over high-speed optical links to off-detector “Tile Preprocessor” boards. All cell data from every bunch crossing will be read out continuously, which will mean transitioning from the current 256 optical links and total data rate of 165 Gbps to 8192 optical links and approximately 80 Tb/s.

To evaluate the upgrade concept in realistic conditions, a demonstrator [11] is being designed for an upgraded system that can be run in selected ATLAS modules while maintaining
compatibility with the current system (figure 2) to avoid compromising data taking.

![Superdrawer and demonstrator concept](image)

**Figure 2.** Superdrawer and demonstrator concept. In yellow new electronics, in green: adaptor boards for compatibility with the legacy system and in blue: legacy system electronics.

### 3. Low Voltage Power Supply and High Voltage Power Supply solutions

The Low Voltage Power Supply (LVPS) [5] system is located at the end of the modules in the outer side of the calorimeter and supplies a +10V power (figure 3) to the on-detector electronics. Each on-detector board then uses Point-of-Load regulators (POLs) to supply the locally needed voltages. For increased system reliability, each Mainboard (MB) and Daughterboard (DB) is functionally separated into independent halves. Each half processes the PMTs from one side of the module and additionally has a separate, redundant low voltage feed that is capable of powering both halves of the mini-drawer if one feed fails. In the case of one side failing completely, each of its cells is still read out by the other side.

Two different approaches are under study for the High Voltage Power Supply (HVPS). An on-detector solution [6] uses one HV board per minidrawer, that provides up to 12 channels of high-voltage control. This card is radiation hard and communicates with the off-detector side by slow control signals via the daughterboard. An alternative, remote solution [7] distributes the HV for each PMT from off-detector by routing 12 HV cables to each mini-drawer. Since the HV source is placed off detector, the radiation hardness of the electronic components for this solution is not a concern.

![Power connectivity block diagram using a LVPS and the on-detector HV solution](image)

**Figure 3.** Power connectivity block diagram using a LVPS and the on-detector HV solution.
4. Front-end solutions
Three different solutions for the front-end boards (FEBs) are being evaluated, each with their own corresponding motherboard:

(i) the modified 3-in-1 card [8] which is a redesign of the legacy front-end boards, but with better linearity and lower noise
(ii) the FATALIC-ASIC solution [9] which includes ADCs in a front-end ASIC
(iii) the charge-integrating QIE ASIC solution [10]

The three alternatives have similar approaches based on “all in one cards” that hold different electronic designs for each solution. The modified 3-in-1 card and the FATALIC alternatives are pulse shaper solutions, based on simple electronic components and a complex ASIC design respectively; while the QIE design is based on a gated integrator ASIC. The present demonstrator system is based on the modified 3-in-1 solution, for its ability to provide compatibility with the legacy system.

The mainboard solutions provide the control, monitoring and readout of the FEBs, and deliver digitized data to the daughterboard. All three mainboards are designed with double redundancy in mind. The 3-in-1 mainboard prototype [12] is divided into halves, each half hosting six FEBs from one side of the module. Each half mainboard reads out and supplies low voltage to the FEBs, sends digitized signal and distributes power to its corresponding daughterboard, and sets gains and controls the charge injectors on each 3-in-1 channel.

All three solutions are being extensively studied in test beams and the results will help determine which optimum solution will be selected for the insertion in ATLAS.

5. The Daughterboard
Control and communication between the front-end and off-detector electronics are performed by the daughterboard [13], which also has a double redundant design. The daughterboard (figure 4) is compatible with all three mainboard designs, the on-detector HV board and the Cs calibration system. It is also in charge of recovering the system clock and distributing it to the front-end system via the GBTx ASICs [15]. The main functionalities are programmed in dual Kintex 7 FPGAs. Current and temperature monitoring of both FPGAs and the mini-drawer environment are also performed. Communication is provided by a redundant pair of QSFP optical transceivers, each allowing high speed communication at $4 \times 9.6 \text{ Gbps}$ uplink and $4 \times 4.8 \text{ Gbps}$ downlink.

6. The TilePreprocessor
The Tile Preprocessor (TilePPr) [16] is the main component of the back-end electronics. The current prototype for the demonstrator project provides compatibility between the current and the upgraded system. The TilePPr prototype (figure 4) can control and read out one complete TileCal super drawer (four mini-drawers). Its functionality includes receiving and processing digital data from the daughterboards, decoding and distributing Trigger Timing and Control (TTC) signals to the front-end electronics for configuration and synchronization with the LHC clock. It also provides control and monitoring of the high voltage power supplies through a Detector Control System (DCS) interface. Through the demonstrator phase and up to the Phase-II upgrade the TilePPr prototype will also serve as the interface between the legacy Read Out Driver (ROD) and the demonstrator, as well as a test bench for the development of new real time data processing algorithms for reconstruction of energy, timing and quality factors for the L0/L1 trigger in Phase II and as a test bench for the proposed Felix readout concept [14].

The TilePPr is a complex board with three different FPGAs for implementing all the needed functionalities. SFP modules are used for receiving TTC signals and communicating with the legacy system, while a minipod tx module provides ribbon fiber output links to the L0/L1 trigger.
Four QSFP modules provide communication links to the daughterboards. Another important design consideration is the low-jitter clocking circuitry for assuring clean clock domains for the FPGAs and high-speed optical links.

The first TilePPr prototypes have been designed, produced and tested as part of the TileCal Demonstrator project.

7. Radiation Tolerance
All parts of the front-end system need to be qualified for running in a radiation environment. Since the demonstrator is a project under constant development, several parts are being or will soon be tested for verifying the radiation requirements of TileCal (figure 4).

The system has been designed to be radiation tolerant by using multiple redundancy on the electronic design [3], radiation tolerant components, Triple Mode Redundancy (TMR) in the FPGAs, redundant links, cyclic redundancy check (CRC) data protection, and the use of the radiation-hard GBT ASIC [15] with forward error correction (FEC) for sending the downstream data off-detector.

Figure 4. Left: Daughterboard revision 4. Right Tile Preprocessor Prototype.

Figure 5. Left: Radiation levels in ATLAS. Right: Ongoing work on the different radiation tests for the demonstrator. (TID: Total Ionizing Dose, NIEL: Non-Ionizing Energy Loss and SEE: Single Event Upsets)
8. Conclusions
The demonstrator project is still under development. Some testing remains to be done of both the electronics functionality and the radiation radiation hardness of the system. The strategies followed for the design of the system are meant to cover the possible difficulties that could arise given the high requirements to be met for Phase-II. The results of the 2016 testbeams will guide the final design of the hybrid demonstrator system to be installed in ATLAS.

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