Optimization of Low-Voltage-Operating Conditions for MG-MOSFETs

SOUMAJIT GHOSH\(^1\) (Graduate Student Member, IEEE), M. MIURA-MATTAUSCH\(^1\) (Fellow, IEEE), T. IIZUKA\(^1\) (Member, IEEE), HAFIZUR RAHAMAN\(^2\), AND H. J. MATTAUSCH\(^1\) (Senior Member, IEEE)

\(^1\)HiSIM Research Center, Hiroshima University, Higashihiroshima 739-8530, Japan
\(^2\)School of VLSI Technology, Indian Institute of Engineering Science and Technology at Shibpur, Howrah 711103, India

CORRESPONDING AUTHOR: S. GHOSH (e-mail: ghoshoumajit@hiroshima-u.ac.jp)

ABSTRACT

Adaptive threshold-voltage controlling of thin-film multi-gate (MG) MOSFETs, using independent back-gate biasing, is applied for realizing latency and power optimization. The controlling-method validity for low-voltage operation is analyzed with the compact model HiSIM-MG, considering all internally induced charges specific for MG controlling. Current-drivability degradations, due to back-gate-charge contribution under positively-biased back-gate voltage and existence of an optimized operating condition, are confirmed. The optimized operating condition is shown to keep the back-gate charge under the weak inversion with a corresponding relatively small back-gate charge. It is also demonstrated, that an input-voltage optimization accompanies the back-gate-voltage optimization, sustaining the optimized low power loss with low input voltage. Circuit-performance improvement of 27% by about 30% reduction of substrate thickness, while keeping switching-power loss small, is also verified.

INDEX TERMS

CMOS circuit, low-power operation, MG-MOSFET, and SOTB-MOSFET.

I. INTRODUCTION

Thin film multi-gate (MG) MOSFETs are widely acknowledged as an attractive alternative for low-voltage-circuit applications, due to an additional independently-controllable back-gate [1]–[3]. The Silicon on thin SOI layer (ETSOI) MOSFET has been widely studied with relatively thick Buried Oxide (BOX) [4]–[7], where the body is separated from the substrate by a BOX layer to reduce the effects of parasitic capacitances and undesired punch-through currents [8]. This helps to achieve better switching performance, and thus the ETSOI structure has been widely applied for RF circuits. Together with the thin SOI layer, the thin BOX (SOTB) MOSFET [9]–[12] is one of the MG-MOSFET derivatives [13]. Bidirectional gate control improves the subthreshold characteristics significantly. It has been demonstrated, that the influence of the back-gate control is an important factor for performance and power-loss optimization. Supply-voltage \((V_{dd})\) scaling is one of the most effective ways to reduce dynamic power loss, as it has a quadratic relationship with the switching loss [14]–[15]. However, scaling down the supply voltage weakens the front-gate control over the channel, especially for short-channel-length devices, due to the lateral-field dominance, produced by the source/drain junction depletion extension [16]–[18]. This degrades the subthreshold slope. Therefore, to significantly strengthen the vertical electric field dominance over lateral field, a contribution from the back-gate is essential, and this is what multi-gate structure offers. In an MG-MOSFET structure, both front- and back-gate-controlled currents constitute the overall drain current \((I_{ds})\). In the subthreshold condition, a weaker front-gate-controlled-current contribution is inadequate for fast switching operation. Positive back-gate biasing is essential to increase the back-gate-controlled current. However, the efficiencies of front- and back-gate-current control by \(V_{gs}\) and \(V_{bg}\), respectively, are vastly different in nature, due to different oxide thicknesses (FOX and BOX) and presence of an additional substrate region underneath BOX. Although positive back-gate biasing increases the drain current, its efficiency varies over a wide range of values [19].

Our investigation focuses on \(V_{bg}\)-control efficiency for back-gate-current generation and its impact on circuit...
performance. The near- or sub-threshold region is specifically analyzed, as it is highly attractive for the purpose of improving the energy efficiency. As a substitute for measurement data, 2D-device simulations [20] are used in the analysis. By applying the developed compact model HiSIM_MG [21], the key factors for optimizing circuit performance and device structure are clarified. It is demonstrated, that an independent control of the MG-MOSFET gates provides the necessary optimization freedom for simultaneously achieving the requirements of both low switching loss and sufficiently high switching speed.

II. MG-MOSFET FEATURES AND THEIR MODELING

The SOTB-MOSFET structure, applied in our investigation, is shown in Fig. 1a, where also the device parameters and their values are listed. Figure 1b depicts the $I_{ds}-V_{gs}$ characteristics of 2D-device simulation for different back-gate voltages ($V_{bg}$). The extracted threshold voltage $V_{th}$ is plotted in Fig. 1c as a function of $V_{bg}$. This extraction is done with the GMLE method, which has been verified to provide reliable results for advanced MOSFET generations [22]. It can be seen, that $V_{th}$ is reduced drastically for $V_{bg} > 0$, which is used to realize low-power operation [23]. The main effect of a positive $V_{bg}$ is the additional formation of a back-gate charge $Q_b$, as schematically depicted in Fig. 2a. The surface potentials $\phi_s$ and $\phi_b$ at front and back gate are compared in Fig. 2b as a function of $V_{gs}$ for different $V_{bg}$ values. The threshold condition occurs, when either of the potential values $\phi_s$ and $\phi_b$ reaches $\Phi_B$. It can be seen roughly, that the threshold condition is mainly determined by the back-gate potential $\phi_b$ for $V_{bg} > 0$ and by the front-gate potential $\phi_s$ for $V_{bg} < 0$.

We have developed the compact model HiSIM_MG, which is applicable for independent-gate control of MG-MOSFETs. The model can be utilized for common-gate control as well as for more advanced technologies such as those of SOTB-MOSFETs. Our main focus here is to analyze the $Q_b$ contribution of the SOTB-MOSFET generation in circuits. For this purpose, all possible induced charges within the device are considered explicitlly, together with the deep current flow near the BOX side. The Poisson equation is used together with the Gauss law to derive the $V_{gs}$ dependency of the total charge as [24]–[27]

$$V_{gs} - V_{fb} - \phi_s = \frac{Q_s + Q_b + Q_{dep} + Q_{bulk}}{C_{FOX}}$$  \hspace{1cm} (1)

where $Q_s$, $Q_b$, and $Q_{bulk}$ are the carrier charges at front gate, back gate and the opposite side of BOX, respectively, as depicted in Fig. 2a. $Q_{dep}$ describes the depletion charge within the channel. The Poisson equation is solved iteratively together with the boundary conditions at the different material junctions [28], [30]. Figure 1b reveals, that HiSIM_MG can realize a good fit to the 2D device simulation results for any bias conditions.

For $V_{bg} \leq 0$, mostly $\phi_s$ dominates over $\phi_b$ (see Fig. 2b), which indicates that the inversion charge $Q_s$ at the front-gate side is giving the major contribution, while the influence of the back-gate-inversion charge $Q_b$ is significantly smaller. Fig. 3 depicts the charge distribution of $Q_s$ and $Q_b$ as a function of $V_{bg}$. An operation condition with smaller $V_{bg}$ improves the subthreshold swing but reduces the gate overdrive ($V_{gs} - V_{th}$), because $V_{th}$ increases as demonstrated in Fig. 1b.

For $V_{bg} > 0$, on the contrary, $\phi_b$ starts to increase as a function of $V_{gs}$ first and $\phi_s$ follows, resulting in $Q_b$ domination over $Q_s$ for smaller $V_{gs}$. Under such a condition, the MOSFET has degraded subthreshold slope, because higher $V_{bg}$ introduces a $Q_b$-originated current flow deep inside the SOI layer. Here, $Q_b$ is not easily controlled by $V_{gs}$ but rather
by $V_{bg}$ through $T_{box}$. The gate control is kept sufficiently high for a thin SOI-layer thickness, however, so that the sub-threshold slope degradation is not so obvious in our studied case.

**III. EFFICIENCY OF BACK-GATE CONTROL IN A CIRCUIT**

With the use of HiSIM-MG, a CMOS-inverter circuit (see Fig. 4a) is investigated to analyze the switching-power loss with different $V_{bg}$ values for high (1V) and low (0.4V) $V_{dd}$ cases. Figure 5 shows the schematic explanation of the two different operation conditions with the simulated $I_{ds} - V_{gs}$ characteristics, depicted in Fig. 1b. As demonstrated in this figure, the voltage range of both $0 \leq V_{gs} \leq 1V$ and $0 \leq V_{gs} \leq 0.4V$ becomes insufficient to ensure lower static-power loss at higher $V_{bg}$. Thus, upper and lower limits of the gate-input pulse are scaled up and down by an input-voltage scaling $\Delta V_{in}$, respectively, so that switching can complete while leakage currents are negligible, as shown in Fig. 4b. Figure 6 depicts the power loss as a function of $\Delta V_{in}$ at low $V_{dd}$, separately for the switching-power loss (Fig. 6a) and the static-power loss (Fig. 6b). Even though the switching-power loss is only lightly dependent on $\Delta V_{in}$, the static loss can be reduced drastically by adjusting $\Delta V_{in}$ for such a CMOS-inverter circuit.

The $\Delta V_{in}$ value is fixed to 0.6V hereafter to limit the static loss below 0.2 $\mu$W, keeping an identical value for any bias conditions of $V_{bg}$. Figure 7 compares the simulated switching performance for the two $V_{dd}$ conditions with various $V_{bg}$ values. As can be seen in Fig. 7a, higher-voltage operation of $V_{dd} = 1V$, doesn’t show any significant delay change for the inverter-output-voltage transition even at higher $V_{bg}$, which is explainable by the fact, that higher $V_{dd}$ drives the MOSFET to operate far beyond the threshold condition, eliminating the $V_{bg}$ dependence of $\phi_s$, i.e., indicating a strong-inversion attainment. Rather, the $V_{dd} = 1V$ case is compromised by a substantial switching-power loss, being mostly due to the current increase, caused by the effective $V_{gs}$ increase by $\Delta V_{in}$ (see also Fig. 5). Namely, efficiently controlled $\phi_s$ (and hence $Q_s$) improves the transition delay significantly.

For low-voltage operation ($V_{dd} = 0.4V$), the output-voltage transition happens in the sub-threshold region, which
FIGURE 6. (a) The switching-power loss in CMOS-inverter remains weakly coupled with input-pulse scaling (increasing $\Delta V_{in}$), as it doesn’t influence the transition region apart from a slight slope deviation. (b) On the other hand, Static power loss reduces significantly for higher $\Delta V_{in}$ values. For $V_{bg} > 1V$, without $V_{in}$ scaling, static power loss is relatively high and comparable to the switching-power loss.

provides more efficient $V_{gs}$ control along with stronger $V_{bg}$ dependence. At $V_{bg} = 0$, the contribution of the surface charge $Q_s$ still dominates during the transition. Therefore, relatively large $V_{gs}$ is required, as reflected by the higher delay value in Fig. 7b. On the contrary, $Q_b$ starts to control the transition as $V_{bg}$ increases, and the transition delay becomes smaller. Therefore, ample opportunities are available for $0V < V_{bg} \leq 2.0V$ to achieve optimization with respect to $V_{bg}$.

As discussed in the previous section, $0V < V_{bg} \leq 1.0V$ limits the generation of $Q_s$, resulting in only small influence on the switching performance. Figure 8 illustrates the extracted results for delay time ($\tau_d$) and averaged power loss ($P_{\text{switching loss}}$), using the simulation results shown Fig. 7. For the low-$V_{dd}$ case, it is evident that $1V < V_{bg} < 1.5V$ is the optimum window, where delay-time ($\tau_d$) reduction is possible while power-loss increase is kept small. Our investigation reveals that $V_{bg}$ of $1.2V$ provides the lowest power loss with simultaneously short $\tau_d$.

The results shown in Figs. 7 and 8 are those at fixed $\Delta V_{in}$ of $0.6V$. However, it is essential for low $V_{th}$ devices, especially with negative $V_{th}$, to operate additionally with scaled input pulses for realizing an appropriate switching performance. Since the switching loss is not much dependent on $\Delta V_{in}$, $\Delta V_{in}$ is optimized only for the static loss. Figure 9a depicts the minimum $\Delta V_{in}$ values, extracted from the result shown in Fig. 6, as a function of $V_{bg}$ together with the boundary condition of $V_{gs} + \Delta V_{in} > V_{th}$. This $\Delta V_{in,\text{min}}$ is considered as the optimized value in accordance with $V_{bg}$, demonstrating that such an optimization can be done successfully as depicted in Fig. 9b. It can be seen, that the simultaneous optimization of $\Delta V_{in}$ sustains the power loss of the higher input voltage. As can be seen in Fig. 3, both $Q_s$ and $Q_b$ are contributing for the formation of the threshold condition at $0V < V_{bg} \leq 1.5V$. However, $Q_b$ alone
TABLE 1. Scope for back-gate biasing in MG-MOSFET.

| $V_{bg}$ | -1V to 0V | 0V to 1.2V | 1.2V to 2V |
|----------|-----------|------------|------------|
| High $Q_{th}$, $Q_{th}$ | Suitable for low power application although inefficient power-loss scaling. $Q_{th} < Q_{th}$, $Q_{th}$ | No latency degradation but power-loss increase. $Q_{th} > Q_{th}$, $Q_{th}$ | |
| Low $Q_{th}$, $Q_{th}$ | Small power-loss but high latency. $Q_{th} < Q_{th}$, $Q_{th}$ | Small power-loss and improved latency. $Q_{th} = Q_{th}$, $Q_{th}$ | Latency improvement but power-loss increase. $Q_{th} > Q_{th}$, $Q_{th}$ |

TABLE 2. Structural scaling parameters.

| Parameters | Original | Optimized |
|------------|----------|-----------|
| $T_{SOI}$ | 12nm | 8nm |
| $T_{BOX}$ | 10nm | 6nm |

FIGURE 9. (a) Extracted $\Delta V_{in,min}$ from the results shown in Fig. 6 as a function of $V_{bg}$ (b) simulation results of output voltage $V_{out}$ and switching power loss $P_{switching loss}$ with the extracted $\Delta V_{in,min}$ values for $V_{bg} = 1V$ and 1.5V, which are different for different $V_{bg}$ values as can be seen in (a). In spite of $\Delta V_{in}$ reduction, no power loss increase is observed.

starts to contribute to the switching at $V_{bg} = 1.2V$. Table 1 summarizes the scope of MG-structure back-gate biasing for high and low $V_{dd}$ cases.

IV. STRUCTURAL OPTIMIZATION FOR LOW POWER LOSS

For further improvement of the power loss, the validity of a structural optimization is investigated. To reduce the switching loss, $V_{gs}$ controllability must be improved. At the same time the $Q_{th}$ contribution must be increased to enable the low voltage application. To fulfill these contradicting requirements, $T_{BOX}$ is reduced together with $T_{SOI}$. The modifications are summarized in Table 2, where the rest of the overall device size is kept the same. $I_{ds} - V_{gs}$ characteristics for the optimized structure are depicted in Fig. 10 and show good agreement with 2D-simulation results, using identical model parameters as for the original structure (see Fig. 1b), except for the device-structure parameters. This verifies the accuracy of the developed model. Figure 11 compares the results for the 2 device structures. Down-scaling of the $T_{SOI}$ layer allows $Q_{th}$ to be decreased due to increased $V_{gs}$ control. Contradictorily, $T_{BOX}$ scaling allows $Q_{th}$ to be increased. At lower $V_{bg}$ ($0V < V_{bg} \leq 1.2V$), the $T_{SOI}$-scaling contribution dominates over that of $T_{BOX}$ due to the relatively small $Q_{th}$ (see Fig. 3), whereas for higher $V_{bg}$ the reverse holds true because $Q_{th}$ becomes more important. The magnitude of $Q_{th}$ is strongly dependent on $V_{bg}$ and $T_{SOI}$. As observed in Fig. 11a, $I_{ds}$ decreases for the scaled structure with higher $V_{th}$ when $0V < V_{bg} \leq 1.2V$. Beyond that, $I_{ds}$ increases with lower $V_{th}$. Fig. 12 summarizes the $V_{th}$ values as a function of $V_{bg}$. The reduction of $V_{th}$ as a function of $V_{bg}$ is quite drastic for the scaled structure. Hence, in regards of switching-loss improvements, $0V < V_{bg} \leq 1V$ is a comfortable region for circuit operation with scaled devices, without sacrificing a small power loss. Figure 11b demonstrates, that a switching-loss reduction of 27% can be achieved with the studied structure scaling at constant $V_{bg} = 1V$, which would not be possible for $V_{bg} = 0V$.

V. CONCLUSION

The SOI-MOSFET with thin SOI and BOX thicknesses was investigated with HiSIM_MG, to verify the back-gate-voltage $V_{bg}$ contribution for low power operation. It was found, that the relative electrostatic controllability of carriers within the SOI layer by front gate and back gate varies...
mostly due to the slow transition in a CMOS inverter. It increases, which results in a switching-power-loss increase depending on the operating region when increasing $V_{bg}$. This is shown that the input-voltage scaling is additionally efficient to achieve the desired low-power operation. A specific range of $V_{bg}$ ($0V < V_{bg} ≤ 1.2V$ for the studied case), where both performance and power loss are optimal, is validated to be suitable for low-voltage operation. This refers to the condition, where $Q_b$ is still kept under the weak-inversion condition. Within this $V_{bg}$-bias range, multi-stage cascaded circuits can be operated without $\Delta V_{th}$ scaling and with minimal switching-power-loss. Structural device optimization in high-density circuits is found to yield 27% lower switching-loss for about 30% reduced substrate thicknesses. It is also demonstrated, that the MG-MOSFET optimization can be successfully performed by applying the compact model HiSIM_MG.

**REFERENCES**

[1] N. Sugii et al., “Ultralow-power SOTB CMOS technology operating down to 0.4 V,” J. Low Power Electron. Appl., vol. 4, no. 2, pp. 65–76, Jun. 2014, doi: 10.3399/jlpea.0420065.

[2] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Rokor, P. K. Ko, and C. Hu, “Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI,” IEEE Trans. Electron Devices, vol. 44, no. 3, pp. 414–422, Mar. 1997, doi: 10.1109/16.556151.

[3] Y. Yamamoto et al., “Ultralow-voltage operation of silicon-on-thin BOX (SOTB) 2Bit SRAM down to 0.37 V utilizing adaptive back bias,” in Proc. Symp. VLSI Technol., Jun. 2013, pp. T212–T213.

[4] D. Hisamoto, T. Kaga, Y. Kawamoto, and E. Takeda, “A fully-depleted lean-channel transistor (DELTIA)—A novel vertical ultra thin SOI MOSFET,” in Int. Electron Devices Meeting Tech. Dig., Dec. 1989, pp. 833–836, doi: 10.1109/IEDM.1989.74182.

[5] E. Suzuki et al., “Highly suppressed short-channel effects in ultrathin SOI n-MOSFETs,” IEEE Trans. Electron Devices, vol. 47, no. 2, pp. 354–359, Feb. 2000, doi: 10.1109/16.822280.

[6] O. Faynot et al., “Planar fully depleted SOI technology: A powerful architecture for the 20nm node and beyond,” in Proc. Int. Electron Devices Meeting, Dec. 2010, pp. 3.2.1–3.2.4, doi: 10.1109/IEDM.2010.5703287.

[7] Y. Kado et al., “Substantial advantages of fully-depleted CMOS/SIMOX devices as low-power high-performance VLSI components compared with its bulk-CMOS counterpart,” in Proc. Int. Electron Devices Meeting, Dec. 1995, pp. 635–638, doi: 10.1109/IEDM.1995.499300.

[8] J. P. Colinge, “Subthreshold slope of thin-film SOI MOSFET’s,” IEEE Electron Device Lett., vol. 7, no. 4, pp. 244–246, Apr. 1986, doi: 10.1109/EDL.1986.26359.

[9] S. Makovejev et al., “Wide frequency band assessment of 28 nm FDSOI technology platform for analogue and RF applications,” in Proc. 15th Int. Conf. Ultimate Silicon (ULIS), Apr. 2014, pp. 53–56, doi: 10.1109/ULIS.2014.6813904.

[10] R. Tsuchiya et al., “Silicon on thin BOX: A new paradigm of the CMOSFET for low-power high-performance application featuring wide-range back-bias control,” in Proc. Int. Electron Devices Meeting IEDM Tech. Dig., Dec. 2004, pp. 631–634, doi: 10.1109/IEDM.2004.1419245.

[11] T. Ishigaki et al., “Silicon on thin BOX (SOTB) CMOS for ultraslow standby power with forward-biasing performance booster,” in Proc. 38th Eur. Solid-State Device Res. Conf., Sep. 2008, pp. 198–201, doi: 10.1109/ESSDERC.2008.4681732.

[12] Q. Liu et al., “Ultra-thin-body and BOX (UTBB) fully depleted (FD) device integration for 22 nm node and beyond,” in VLSI Symp. Tech. Dig., Jun. 2010, pp. 61–62, doi: 10.1109/VLSIT.2010.5556120.

[13] J.-P. Colinge, “Multigate transistors: Pushing Moore’s law to the limit,” in Proc. Int. Conf. Simulat. Semicond. Processes Devices (SISPAD), Sep. 2014, pp. 313–316, doi: 10.1109/SISPAD.2014.6931626.

[14] S.-M. Kang and Y. Leblebici, “MOS inverters: switching characteristics and interconnect effects,” in CMOS Digital Integrated Circuits: Analysis and Design. New York, NY, USA: McGraw-Hill, 1999, pp. 196–258.
[15] N. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective. Boston, MA, USA: Pearson Educ., 2005.

[16] F. Á. Herrera et al., “Advanced short-channel-effect modeling with applicability to device optimization—Potentials and scaling,” IEEE Trans. Electron Devices, vol. 66, no. 9, pp. 3726–3733, Sep. 2019, doi: 10.1109/TED.2019.2931749.

[17] F. Á. Herrera, M. Miura-Mattausch, T. Iizuka, H. Kikuchihara, Y. Hirano, and H. J. Mattausch, “Modeling of short-channel effect on multi-gate MOSFETs for circuit simulation,” in Proc. Int. Symp. Devices Circuits Syst. (ISDCS), 2020, pp. 1–4, doi: 10.1109/ISDCS49393.2020.9263000.

[18] F. Á. Herrera et al., “Leading-edge thin-layer MOSFET potential modeling toward short-channel effect suppression and device optimization,” IEEE J. Electron Devices Soc., vol. 7, pp. 1293–1301, 2019, doi: 10.1109/JEDS.2019.2948648.

[19] S. Ghosh, M. Miura-Mattausch, T. Iizuka, H. Rahaman, and H. J. Mattausch, “Operating-condition optimization of MG-MOSFETs for low-voltage application,” in Proc. Electron Devices Technol. Manuf. Conf. (EDIM), Oita, Japan, Mar. 2022, pp. 97–99.

[20] ATLAS User’s Manual, Silvaco, Inc., Santa Clara, CA, USA, Apr. 2018.

[21] HiSIM_SOTB User’s Manual, Hiroshima Univ., Hiroshima, Japan, 2017.

[22] M. Tsuno, M. Suga, M. Tanaka, K. Shibbaha, M. Miura-Mattausch, and M. Hirose, “Physically-based threshold voltage determination for MOSFET’s of all gate lengths,” IEEE Trans. Electron Devices, vol. 46, no. 7, pp. 1429–1434, Jul. 1999, doi: 10.1109/6.772487.

[23] B. Hoefflinger, “ITRS: The international technology roadmap for semiconductors,” in The Frontiers Collection. Heidelberg, Germany: Springer, Oct. 2011, pp. 161–174, doi: 10.1007/978-3-642-23096-7_7.

[24] R. S. Muller and T. I. Kamins, “MOS field-effect transistors I: Basic theories and models,” in Device Electronics for Integrated Circuits, 2nd ed. New York, NY, USA: Wiley, 1986, pp. 422–474.

[25] S. M. Sze, “MIS diode and CCD,” in Physics of Semiconductor Devices, 2nd ed., New York, NY, USA: Wiley, 1981, pp. 362–430.

[26] Y. Taur and T. H. Ning, 3 in Fundamentals of Modern VLSI Devices. New York, NY, USA: Cambridge Univ. Press, 1998, pp. 120–128.

[27] M. Miura-Mattausch, H. J. Mattausch, and T. Ezaki, The Physics and Modeling of MOSFETs. Singapore: World Sci., Jun. 2008, doi: 10.1142/6159.

[28] M. Miura-Mattausch et al., “Compact modeling of SOI MOSFETs with ultrathin silicon and BOX layers,” IEEE Trans. Electron Devices, vol. 61, no. 2, pp. 255–265, Feb. 2014, doi: 10.1109/TED.2013.2286206.

[29] M. Miura-Mattausch, S. Amakawa, M. Miyake, H. Kikuchihara, S. Baba, and H. J. Mattausch, “HiSIM-SOI: Complete surface-potential-based model valid for all SOI-structure types,” in Proc. IEEE Int. SOI Conf. (SOI), 2010, pp. 1–4, doi: 10.1109/SOI.2010.5641416.

[30] N. Sadachika et al., “Completely surface-potential-based compact model of the fully depleted SOI-MOSFET including short-channel effects,” IEEE Trans. Electron Devices, vol. 53, no. 9, pp. 2017–2024, Sep. 2006.