LETTER

A high gain 79-GHz low noise amplifier using inductor-embedded neutralization technique

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Abstract This paper presents a 79 GHz low noise amplifier (LNA) design featuring high gain fabricated in a 40-nm CMOS process. To make better use of active devices, we propose an inductor-embedded neutralization technique. The implemented prototype consists of four-stage common-source amplifiers using the proposed technique and transformer-based matching networks. The measurement results show that the amplifier realizes a peak gain of 23 dB at 79 GHz with 14.4 mW power dissipation and 0.4 mm² area occupation. The LNA achieves a minimum noise figure (NF) of 6.3 dB.

Keywords: low noise amplifier, neutralization technique, embedding inductors

Classification: Microwave and millimeter-wave devices, circuits, and modules

1. Introduction

Over the past years, the CMOS millimeter-wave circuit research has attracted enormous attention [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11] as the CMOS technology node scales. Among components of a wireless system, the low noise amplifier (LNA) is a particularly crucial one since it is required to offer a high gain to reduce the noise contribution of subsequent circuits [9, 12, 13, 14], thus elevating the system sensitivity. However, the LNA in CMOS still has many difficulties in attaining high gain and becomes a power-consuming block when the operating frequency enters the millimeter-wave regime. The neutralization technique has been a useful and popular method in the amplifier design to provide higher signal magnification [15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25]. Nevertheless, it is still not an effective way to make maximum use of the active devices. [26, 27, 28] introduced a solution to realize the maximum available gain. Unfortunately, the structure suffers from bulky passive devices and inflexible biases for active devices.

In this paper, a differential amplifier employing an inductor-embedded neutralization technique is proposed. Compared with the conventional neutralization structure, the proposed topology achieves a higher gain. Circuit design and results are presented as follows.

2. Circuit design

The structure in Fig. 1(a) is the traditional differential common source amplifier. The parasitic capacitance, Cgd, deteriorates the gain of transistors [15], especially for millimeter-wave applications. As shown in Fig. 1(b), the capacitive neutralization method is commonly adopted to mitigate the effect of Cgd. The proposed topology depicted in Fig. 1(c) embeds extra inductors, Lg and LD, to further enhance the amplifier gain. Seeking to exhibit the benefit of embedding inductors, Fig. 2 presents traces of the simulated maximum available gain, Gmax, corresponding to different capacitances and inductances at 79 GHz with the quality factor of inductors equaling to 10. The results show that embedding inductors can raise the Gmax in the flat-gain region where the neutralization capacitance is chosen to ensure stability. About 1 dB gain enhancement is obtained for one stage with Lg of 20 pH and LD of 10 pH.

The schematic of the proposed four-stage amplifier is shown in Fig. 3. Compared with the inductive load (about 90 pH) of the MOS transistors, the required embedding inductances (10 pH and 20 pH) are relatively smaller. Accordingly, Lg and LD are implemented by the interconnect lines with specific lengths, which is different from the classic design approach reducing the lines as much as possible. The classic and proposed gain cell implementations are de-
Fig. 2 Simulation results of $G_{\text{max}}$ versus neutralization capacitance.

Fig. 3 Proposed low noise amplifier schematic.

Fig. 4 (a) Classic gain cell. (b) Proposed gain cell. (c) $S_{21}$ and NF comparison of two topologies.

Fig. 5 Balun model in EM simulator.

Fig. 6 Imbalance results of the balun.

Fig. 7 Chip photograph of the proposed LNA.

Fig. 8 Simulation and measurement results of the circuit.

Fig. 9 Measured stability factor and delta.

Fig. 10 NF measurement setup.

makes better use of the MOS transistors.

An input balun is employed to transform a single-ended signal to a differential signal and provide impedance matching. A metal-oxide-metal (MOM) capacitor amid the balun windings is connected to the tap of the secondary winding for reducing the balun’s differential imbalance issue. The capacitor made of metal M1-M7 offers an ac ground path. The balun’s model in the EM simulator and imbalance results are depicted in Fig. 5 and Fig. 6, respectively. The amplitude difference (AD) and phase difference (PD) between the differential terminals are 26.25 dB and 5 degrees at 79 GHz benefiting from the MOM capacitor.

For the sake of noise performance, the transistors in the design are biased at an optimum current density of 150 $\mu$A/um [1, 29, 30]. In our circuit, the stacked transformer structure implemented by the top two metal layers, ultra-thick metal (UTM) and M7, is utilized to obtain a maximum coupling factor, i.e., $k$, of 0.81 at 79 GHz, which is beneficial to reduce the loss of the matching networks [31].

3. Results

The chip photograph of the proposed LNA is shown in Fig. 7. The total chip size is 1.0 mm $\times$ 0.4 mm. The simulation and measurement results of the circuit are presented in Fig. 8. According to measured scattering parameters via vector network analyzer, calculated stability factor and delta are demonstrated in Fig. 9. The proposed LNA realizes a maximum gain of 23 dB with a 14.4-mW dc power dissipation from a 0.4-V source. The corresponding minimum stability factor is 7.2, indicating the unconditional stability of the design. The amplifier provides a minimum NF of 6.3 dB. The NF measurement setup is depicted in Fig. 10.
To attain an accurate NF result, the DUT has to offer enough gain. Therefore, two DUTs are cascaded with bonding wires, whose effects are subtracted according to the Friis equation [12]. Meanwhile, the amplifier has a measured OP1dB of $8.2 \text{dBm}$ at 79 GHz. Performance comparison with other amplifier designs [2, 10, 11, 32] is summarized in Table I. This work achieves a relatively high gain with relatively low power dissipation. The achieved NF is slightly higher due to the higher loss of the input balun with a MOM capacitor.

### 4. Conclusion

In the LNA design, high gain is a critical requirement to decrease the noise contribution of cascading blocks. Compared with the conventional neutralization structure, the proposed design employs an inductor-embedded neutralization technique to enhance the LNA gain. The design realized in a 40-nm CMOS technology achieves a maximum gain of 23 dB at 79 GHz with a dc power dissipation of 14.4 mW.

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