FeFET-based non-volatile III-V/Si hybrid optical phase shifters

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Abstract: Optical phase shifters are essential elements in photonic integrated circuits (PICs) and function as a direct interface to program the PIC. Non-volatile phase shifters which can retain the information without a power supply, are highly desirable for low-power static operations. Here we demonstrate a non-volatile optical phase shifter by driving a III-V/Si hybrid metal-oxide-semiconductor (MOS) phase shifter with a ferroelectric field-effect transistor (FeFET) operating in the source follower mode. Owing to the various polarization states in the FeFET, we obtained multistate non-volatile phase shifts up to $1.25\pi$ with a CMOS-compatible operation voltage. Furthermore, we proposed a crossbar array architecture to simplify their controls in large-scale PICs and verified its feasibility by confirming the selective write-in operation of a targeted FeFET with a negligible disturbance to the others. This work paves the way for realizing large-scale non-volatile programmable PICs for emerging computing applications such as deep learning and quantum computing.

Introduction

As Si-based complementary metal-oxide-semiconductor (CMOS) electronics are approaching the physical limit of miniaturization, photonic integrated circuits (PICs) are playing increasingly important roles in computing and information processing to harness the unique advantages of photons. Photons tend to have weak interactions with each other and therefore are linear and parallel by nature, making them particularly suitable for a variety of parallel tasks such as matrix multiplication1–3. Direct processing of these tasks in the optical domain can significantly reduce the delay and potentially consume less energy than using electronics4. To deal with diverse tasks, the PIC must be reconfigurable and programmable, which is realized by tailoring the on-chip transmission property via optical phase shifters5. The phase shifter is an essential component of PIC that shifts the phase of light by altering the refractive index of the optical waveguide. Further through the coherent interference between the light in adjacent waveguides, phase shifters function as a direct interface to configure the PIC. Phase shifters based on various mechanisms have been realized6–9, yet most of them are volatile: the information will be lost once the power is turned off. Non-volatile phase shifters, by contrast, can retain the information without a power supply, and thus can significantly simplify the control complexity and reduce the power consumption during static operations.

Non-volatile phase shifters can be realized in several ways. These based on low-loss phase-change materials (PCMs) such as Sb2Se3 are being intensively investigated10–20. Phase transition of the PCM provides a non-volatile change in the refractive index, but the electrical switching through Joule heating usually requires a high voltage incompatible with CMOS drivers when switching the PCM from the crystalline state to the amorphous state17. Another approach
relies on ferroelectric materials such as barium titanate (BTO) embedded into the waveguide to obtain a non-volatile phase shift via the Pockels effect\textsuperscript{21}, but its operation also requires a high voltage of up to 12 V\textsuperscript{22}. In addition to the issue of high operation voltages, for a large-scale PIC which may have hundreds of non-volatile phase shifters, the individual control of all phase shifters is tremendously challenging. Methods that can simplify the control of all phase shifters have not been proposed yet in previous works.

Here we demonstrate a non-volatile optical phase shifter by driving a III-V/Si hybrid metal-oxide-semiconductor (MOS) phase shifter with a Si ferroelectric field-effect transistor (FeFET) based on hafnium zirconium oxide (HZO)\textsuperscript{23–27}. The voltage-driven MOS phase shifter enables efficient and ultralow-power (sub-nW level) phase modulation with a CMOS-compatible voltage via free carriers accumulated at the MOS interface\textsuperscript{7,28}. The FeFET operates in the source follower mode\textsuperscript{29,30}, in which its output voltage is shifted by a non-volatile threshold voltage determined by the polarization state in the ferroelectric layer. By applying a voltage pulse to the gate of the FeFET to configure the threshold voltage, thereby configuring the voltage applied to the MOS phase shifter, we demonstrate multistate non-volatile phase shifts with the proposed scheme. Furthermore, we propose a crossbar array architecture to significantly simplify the control of phase shifters in large-scale PICs. We verify the feasibility of the proposed architecture by observing responses of the threshold voltage of the FeFET in various states. This work paves the way for the realization of large-scale non-volatile programmable PICs, which can ultimately enable ultrafast and energy-efficient information processing in the optical domain.

Results

Principle. The proposed scheme is illustrated in Fig. 1. The hybrid MOS phase shifter is formed by n-InGaAsP, Al\textsubscript{2}O\textsubscript{3}, and p-Si layers. If a positive voltage is applied between the n-InGaAsP and p-Si, free electrons and holes accumulate at the InGaAsP and Si MOS interfaces, respectively and therefore alter the refractive index through the plasma dispersion effect\textsuperscript{31}. Since the electron-induced refractive index change in InGaAsP is more than ten times greater than that in Si, the hybrid MOS phase shifter enables efficient and low-loss phase tuning. During static operations, since the power consumption is only determined by the leakage current of the MOS capacitor, ultralow power operations can be realized. Previously, we have demonstrated such low-loss, efficient, and ultralow-power (0.18 nW) hybrid MOS phase shifters\textsuperscript{7,28,32,33}. The FeFET contains a thin ferroelectric HZO layer as the gate dielectric, in which the polarization direction can be reoriented by an external electric field applied through the gate terminal and retained afterward\textsuperscript{23}. The HZO-based FeFET is compatible with the CMOS process and can exhibit strong ferroelectricity at room temperature even with a several-nanometers-thick HZO layer\textsuperscript{26}. Depending on the polarization state, the threshold voltage of the FeFET is continuously tunable and stored non-volatilely. For a FeFET driving a capacitor in the source follower mode\textsuperscript{29}, the output voltage (V\textsubscript{o}) is approximately given by

\[
V_o = \begin{cases} 
0 & (V_g < V_{th}) \\
V_g - V_{th} & (V_{th} < V_g < V_i + V_{th}), \\
V_i & (V_g > V_i + V_{th}) 
\end{cases}
\]  

where V\textsubscript{th}, V\textsubscript{g}, V\textsubscript{i} are the threshold voltage, gate voltage, and input voltage, respectively [see Fig. 1(b)]. For a fixed V\textsubscript{g}, the output voltage can be tuned by adjusting the non-volatile threshold voltage. Therefore, by driving the MOS
phase shifter with a FeFET operating in the source follower mode, non-volatile phase shifts can be obtained. In this work, the MOS phase shifter and the FeFET are fabricated separately for proof-of-concept demonstration purposes, but in principle, they can be integrated on the same chip.

**Non-volatile operations.** We demonstrate non-volatile phase shifting operations by driving a 1.5-mm-long III-V/Si hybrid MOS phase shifter on one arm of an asymmetric Mach-Zehnder interferometer (AMZI) with an HZO-based FeFET (gate length/width: 25/100 µm). The typical characteristic of our fabricated FeFETs is provided in the supplementary. A microscope image of the AMZI is shown in Fig. 2(a). The source follower operation of the FeFET is first characterized, as shown in Fig. 2(b). By applying a negative reset pulse (-3 ~ -2 V, 10 ms in our experiments) to the gate, the FeFET exhibits a high threshold voltage, resulting in a lower $V_o$; by applying a positive voltage pulse to the gate, the threshold voltage decreases, resulting in a higher $V_o$ for the same $V_g$. As shown in Fig. 2(b), $V_o$ is tuned by 0.78 V between the low $V_{th}$ and the high $V_{th}$ states at a $V_g$ of 0.8 V. The tunable range of $V_o$ is determined by the memory window of the FeFET.\(^{34,35}\) Previously, an HZO-based FeFET with a large memory window of 3.12 V has been demonstrated.\(^{36}\)

The source terminal of the FeFET is then electrically connected to the MOS phase shifter, and the transmission spectra of the AMZI are measured when $V_g$ and $V_b$ [see Fig. 1(b)] are 0.8 V and -0.5 V, respectively. The negative bias ($V_b$) is applied to the MOS phase shifter to preset it into the accumulation state [see Fig. S1(b) in the supplementary]. An obvious shift of the AMZI spectrum is confirmed, as shown in Fig. 2(c), indicating that an optical phase shift is induced by the change in $V_o$ of the FeFET. Since the FeFET operates with the same $V_g$ and $V_b$ between the low $V_{th}$ and high $V_{th}$ states, a non-volatile optical phase shifter is successfully achieved. We further apply increasing voltage pulses from 2 V to 3 V to the gate after a reset pulse [Fig. 2(d)], then measure the $V_o$ and extract the phase shift from the spectra after each pulse. As the polarization in the HZO film gradually changes with the increasing voltage pulse, multistate $V_o$ are obtained, as shown in Fig. 2(e). Since the phase shift is almost linearly proportional to $V_o$ as shown in the inset of Fig. 2(e), multistate phase shifts up to $1.25\pi$ are successfully demonstrated. Meanwhile, it can be seen that $V_o$ only changes slightly for pulse voltages within the range of 2.0 ~ 2.2 V. Therefore, we use 2 V pulses to set the FeFET into the initial state in the following experiments.

**Crossbar array control.** For large-scale PICs, the individual control of all phase shifters has been a long-standing problem. Traditionally, $N^2$ phase shifters require $N^2$ driving channels, resulting in significant control difficulties for $N > 100$. Here, we propose a crossbar array architecture for FeFET-based non-volatile MOS phase shifters to simplify their control in large-scale PICs, as illustrated in Fig. 3(a). This “2T1C” architecture, which consists of 2 transistors (one FeFET and one non-ferroelectric FET) and 1 capacitor (the MOS phase shifter), uses horizontal word lines and vertical bit/select lines to selectively control a single phase shifter in the array, as shown in Fig. 3(b). In this architecture, the word lines and the bit lines require individual controls, while all the select lines only need be driven digitally by a single channel. Therefore, the required driving channels are reduced to $2N+1$.

Figure 3(c) shows the approach to selectively reset a target FeFET in the array. A negative voltage pulse ($V_{reset}$) is applied to the corresponding word line. In order to not disturb other FeFETs connected to the same word line, all select lines are turned on and the same $V_{reset}$ is simultaneously applied to all other bit lines. The ON-state select lines switch on the non-ferroelectric FETs so that the source and the drain terminal of each FeFET have the same electric potential.
In this way, an inverse electric field is only established in the target FeFET during the reset pulse. It is important to note that a weaker electric field along the same direction does not overwrite the polarization state induced by a previous stronger electric field. By using a -2 V reset voltage, the non-target FeFET in the state 4 experiences an effective +2 V voltage pulse, which does not affect its current polarization state because the write-in voltages in this scheme are higher than 2 V, as can be seen from Fig. 2(e).

To program a target FeFET in the crossbar array, voltage pulses (V_{wl}, V_{bl}) are applied to the corresponding word line and bit line, respectively, with other word and bit lines remaining inactive, as shown in Fig. 3(d). The V_{wl} and V_{bl} are chosen to only activate the target FeFET, without disturbing the rest. Depending on the voltages applied to each terminal, the FeFETs in the proposed architecture can experience the 4 different states shown in Fig. 3(d) and Fig. 4(a). Ideally, only the target FeFET (state 1) is affected and all other FeFETs (states 2-4) should be unaffected. To verify this, we emulate these states with a single FeFET and observe the response of its threshold voltage in these states. For state 1, we first set the FeFET to the initial state by applying a positive voltage pulse (2 V, 10 ms) to the gate and then apply various V_{wl} and V_{bl} pulse combinations to the FeFET. For each combination, the shift of threshold voltage with respect to the initial state is extracted and shown in Fig. 4(b). As can be seen, for voltage differences (V_{wl}- V_{bl}) beyond 2.2 V, the threshold voltage decreases as desired; for voltage differences smaller than the initial voltage pulse (2 V), the shift of threshold voltage is negligible. For state 2, we apply various V_{wl} pulses ranging from 0.2 V to 1.8 V to the gate and characterize the source follower operation after each pulse. All the results are plotted in Fig. 4(c), with the inset showing the shift of threshold voltage with respect to the initial state. Similarly, Fig. 4(d) shows the results for state 3 after various V_{bl} pulses ranging from -0.2 V to -1.8 V. We can see that for both states, the shifts of threshold voltage are negligible provided that the voltage difference between V_{wl} and V_{bl} is smaller than the initial voltage pulse (2 V). For state 4, it is obvious that no changes will occur since no voltages are applied to the FeFET. Therefore, by emulating different states the FeFET can experience in the crossbar array, we verified that it is possible to program a single phase shifter using the proposed architecture.

**Discussion.** We compare the performance of our non-volatile phase shifter with those of previous works in Table 1. The non-volatile phase shifter demonstrated in this work simultaneously enables a CMOS-compatible operation voltage, multistate operations, and the compatibility with crossbar array control. The endurance of our non-volatile phase shifter is primarily determined by the FeFET. An HZO-based FeFET with 10^{11} endurance cycles has been demonstrated recently, suggesting that a high endurance is possible for our scheme by improving the FeFET.

| Ref. | Type                      | Operation voltage                        | Multistate operation | Crossbar array control |
|------|---------------------------|------------------------------------------|----------------------|------------------------|
| [10] | PCM (Ge_{2}Sb_{2}Se_{3}Te_{1}) | 13 V (crystallization), 24 V (amorphization) | Not demonstrated     | Not proposed           |
| [13] | PCM (Sb_{2}S_{3})         | 1 V (crystallization), 6 V (amorphization) | Not demonstrated     | Not proposed           |
| [16] | PCM (Sb_{2}Se_{3})        | 6.2 V (crystallization), 21 V (amorphization) | Yes                  | Not proposed           |
Conclusion

We have demonstrated a non-volatile optical phase shifter by driving a III-V/Si hybrid metal-oxide-semiconductor (MOS) phase shifter with a ferroelectric field-effect transistor (FeFET) operating in the source follower mode. With a 1.5-mm-long phase shifter, we obtained multistate non-volatile phase shifts up to 1.25 \( \pi \). Furthermore, we proposed a crossbar array architecture to simplify their controls in large-scale PICs and verified the feasibility by emulating various states experienced by the FeFETs. This work paves the way for the realization of large-scale non-volatile programmable PICs, which can ultimately enable ultrafast and energy-efficient information processing in the optical domain.

Methods

Device fabrication. To fabricate the III-V/Si hybrid asymmetric MZI, a Si-on-insulator (SOI) wafer with a 220-nm-thick Si layer was doped by boron implantation, aiming at a p-type doping concentration of \( 3 \times 10^{17} \text{ cm}^{-3} \). The Si rib waveguide (rib width: 1 \( \mu \)m, slab thickness: 110 nm) was formed by electron-beam lithography (EBL) and inductively coupled plasma (ICP) etching. Then, a 200-nm n-doped (\( 5 \times 10^{15} \text{ cm}^{-3} \)) \( \text{In}_{0.68}\text{Ga}_{0.32}\text{As}_{0.7}\text{P}_{0.3} \) layer (\( \lambda_g = 1.37 \mu \text{m} \)) was bonded to the Si waveguide using a 5-nm \( \text{Al}_2\text{O}_3 \) as the bonding interface, deposited by atomic layer deposition (ALD) at 200 ºC. The InGaAsP mesas were defined by EBL and reactive ion etching (RIE). After the deposition of \( \text{SiO}_2 \) cladding and via formation, a Ni/Au metal layer (50 nm / 400 nm) was deposited by electron-beam (EB) evaporator and then lifted off to form contact pads. FeFETs were fabricated on a p-type (001) Si substrate with the source and drain regions doped by phosphorus ion implantation, following a similar process described in Ref. 25. The substrate was cleaned and soaked in a HCl-H₂O₂-H₂O mixed solution (the SC-2 solution) to prepare 0.6-nm-thick \( \text{SiO}_2 \), which functions as the interfacial layer between Si and HZO. Then, 10-nm-thick ferroelectric HZO films were prepared by atomic layer deposition at 300°C using tetrakis(ethylmethylamino)zirconium, tetrakis(ethylmethylamino)hafnium, and H₂O. TiN gate electrodes were deposited by sputtering and patterned to obtain a gate width of 100 \( \mu \text{m} \) and various gate lengths. The devices were annealed at 400°C for 30 s to form the ferroelectric phase in HZO.

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Data availability
Data underlying the results presented in this paper are available from the corresponding author upon reasonable request.

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Author contributions
H.T. and K.T. fabricated the optical chip and the FeFETs, respectively. R.T. and K.W. performed the experiments. All authors contributed to preparing the manuscript. M.T. and S.T. supervised the project.

Competing interests
The authors declare no competing interests.
Fig. 1. Schematic diagrams. a. Schematic diagram of the FeFET-based non-volatile III-V/Si hybrid MOS optical phase shifter. The FeFET operates in the source follower mode, in which its output voltage is shifted by a non-volatile threshold determined by the polarization state in the ferroelectric layer. The voltage-driven MOS phase shifter enables efficient and ultralow-power phase modulation via free carriers accumulated at the MOS interface. b. Cross-sectional schematic structure of the FeFET and the III-V/Si MOS phase shifter. The FeFET contains a thin Hf$_{0.5}$Zr$_{0.5}$O$_2$ film as the ferroelectric layer. The MOS phase shifter is formed by n-InGaAsP, Al$_2$O$_3$, and p-Si layers.
Fig. 2. Non-volatile operations. a. A fabricated AMZI with 1.5-mm-long III-V/Si hybrid MOS phase shifters integrated on the two arms. b. Source follower operations of a FeFET in two states with different threshold voltages. The threshold voltages are changed by applying pulse voltages to the gate. c. Measured transmission spectra of the AMZI when the MOS phase shifter on one arm is driven by the FeFET. d. After an initial negative voltage pulse to reset the FeFET, positive voltage pulses from 2 V to 3 V are applied to the gate sequentially. After each pulse, the output voltage of the FeFET ($V_o$) and the AMZI spectrum are measured. The phase shift is then extracted from the AMZI spectrum. e. Measured $V_o$ and the extracted phase shift as a function of the pulse voltage described in d. The inset shows the relationship between the phase shift and $V_o$. 
Fig. 3. Crossbar array architecture.  

**a.** Imagined scene of a hybrid integrated circuit consisting of a photonics layer, an electronics layer, and crossbar array metal wires. FeFETs in the electronics layer drive the phase shifters in the photonics layer.  

**b.** Schematic diagram of the “2T1C” crossbar array architecture, which consists of two FETs (one ferroelectric and the other non-ferroelectric) and one capacitor (the MOS phase shifter).  

**c.** Voltage configurations for resetting a target FeFET in the crossbar array. The ON-state select lines switch on the MOSFETs so that the source and the drain terminal of each FeFET have the same electric potential.  

**d.** Voltage configurations for programming a target FeFET in the crossbar array. $V_{wl}$ and $V_{sl}$ are chosen to only activate the target FeFET, without disturbing the rest.
Fig. 4. Responses of FeFETs in various states. a. Four different states experienced by the FeFETs during write-in operations in the crossbar array. Ideally, only the target FeFET (state 1) is affected and all other FeFETs (state 2-4) should be unaffected. b. Shifts of the threshold voltage of a FeFET in state 1. After an initial pulse (2 V, 10 ms), the source follower operations of the FeFET under various combinations of $V_{wl}$ and $V_{bl}$ are characterized, from which the threshold voltages are extracted. c-d. Source follower operations of a FeFET in state 2 after various $V_{wl}$ pulses (c) and in state 3 after various $V_{bl}$ pulses (d), respectively. The insets show the shift of the extracted threshold voltage with respect to the initial state.
Supplementary Information

FeFET-based non-volatile III-V/Si hybrid optical phase shifters

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I. III-V/Si hybrid MOS phase shifter
The III-V/Si hybrid MOS phase shifter enables efficient and ultralow-power (sub-nW level) phase modulation with a CMOS-compatible voltage. Figure S1(a) shows the simulated mode profile in the phase shifter region. The MOS interface lies near the central region in order to obtain a high modulation efficiency. The characterized phase shift as a function of the applied voltage for the 1.5-mm-long phase shifter is shown in Fig. S1(b). The linear region (> 0.5 V) shows a slope of 1.89 π/V, corresponding to a $V_{\pi L}$ of 0.079 V·cm. The modulation efficiency can be further enhanced with improved designs. Previously, we have demonstrated a high modulation efficiency of 0.047 V·cm [1].

II. HZO-based FeFET
FeFETs based on hafnium zirconium oxide (HZO) have promising applications in non-volatile memory and in-memory computation. Figure S2 shows the measured $I_d-V_g$ characteristics of an HZO-based FeFET with a gate length/width of 50/100 µm. The rising gate voltage induces the polarization change in the HZO layer and therefore causes the hysteresis in the $I_d-V_g$ curve.

**Fig. S1.** a. Simulated mode profile in the phase shifter region. b. Characterized phase shift as a function of the applied voltage for the 1.5-mm-long phase shifter.

**II. HZO-based FeFET**
FeFETs based on hafnium zirconium oxide (HZO) have promising applications in non-volatile memory and in-memory computation. Figure S2 shows the measured $I_d-V_g$ characteristics of an HZO-based FeFET with a gate length/width of 50/100 µm. The rising gate voltage induces the polarization change in the HZO layer and therefore causes the hysteresis in the $I_d-V_g$ curve.
We then consider the output voltage of a FET driving a capacitor in the source follower mode [2], as shown in Fig. 1(b). Under the condition of $V_{th} < V_g < V_i + V_{th}$, it is well known that the FET is working in the saturation regime and the current flowing between the drain and the source is given by

$$I_d = \frac{W}{2L} \mu_n C_{ox} (V_{gs} - V_{th})^2,$$  \hspace{1cm} (S1)

where $W$ and $L$ are the channel width and length, respectively, $\mu_n$ is the effective electron mobility, $C_{ox}$ is the gate oxide capacitance per unit area, $V_{gs}$ is the voltage difference between the gate and the source [equals to $V_g - V_o$ in Fig. 1(b)]. Since the FET is driving a capacitor in our scheme, $I_{ds}$ is always 0 in the steady state. Therefore, we have $V_{gs} = V_{th}$, from which we obtain

$$V_o = V_g - V_{th}.$$  \hspace{1cm} (S2)

References

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[2] Razavi, B. Design of analog CMOS integrated circuits. (Mcgraw-Hill Education, 2020).