Novel Modeling Approach to Analyze Threshold Voltage Variability in Short Gate-Length (15–22 nm) Nanowire FETs with Various Channel Diameters

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Abstract: In this study, threshold voltage ($V_{th}$) variability was investigated in silicon nanowire field-effect transistors (SNWFETs) with short gate-lengths of 15–22 nm and various channel diameters ($D_{NW}$) of 7, 9, and 12 nm. Linear slope and nonzero y-intercept were observed in a Pelgrom plot of the standard deviation of $V_{th}$ ($\sigma V_{th}$), which originated from random and process variations. Interestingly, the slope and y-intercept differed for each $D_{NW}$, and $\sigma V_{th}$ was the smallest at a median $D_{NW}$ of 9 nm. To analyze the observed $D_{NW}$ tendency of $\sigma V_{th}$, a novel modeling approach based on the error propagation law was proposed. The contribution of gate-metal work function, channel dopant concentration ($N_{ch}$), and $D_{NW}$ variations (WFV, $\Delta N_{ch}$, and $\Delta D_{NW}$) to $\sigma V_{th}$ were evaluated by directly fitting the developed model to measured $\sigma V_{th}$. As a result, WFV induced by metal gate granularity increased as channel area increases, and the slope of WFV in Pelgrom plot is similar to that of $\sigma V_{th}$. As $D_{NW}$ decreased, SNWFETs became robust to $\Delta N_{ch}$ but vulnerable to $\Delta D_{NW}$. Consequently, the contribution of $\Delta D_{NW}$, WFV, and $\Delta N_{ch}$ is dominant at $D_{NW}$ of 7 nm, 9 nm, and 12, respectively. The proposed model enables the quantifying of the contribution of various variation sources of $V_{th}$ variation, and it is applicable to all SNWFETs with various $L_G$ and $D_{NW}$.

Keywords: variability modeling; threshold voltage; SNWFET; ultrashort gate-length; Pelgrom’s law; nanowire diameter; metal gate granularity; dopant diffusion

1. Introduction

Gate-all-around (GAA) silicon nanowire field-effect transistors (SNWFETs) are considered as a viable option for future device architecture due to their adequate gate-controllability with GAA structures [1–3]. However, ultrascaled SNWFETs suffer from severe threshold voltage ($V_{th}$) variation because the device-to-device variation increases with the decrease in the effective channel width ($W_{eff}$) and gate-length ($L_G$) [4,5]. According to previous studies, random variations such as metal gate granularity (MGG), line edge roughness (LER), and random dopant fluctuation (RDF) cause $V_{th}$ variation in ultrascaled GAA transistors [6–10]. Additionally, the $V_{th}$ variation is also induced by the process variations such as junction gradient and channel thickness variation [11–17].

Therefore, several simulations and models have been recommended to analyze the contribution of multiple sources to $V_{th}$ variation. First, technology computer-aided design (TCAD) simulations are suitable for analyzing the influence of variation sources, but it is difficult to predict the cause of variation inversely from measured $V_{th}$ variation [6–10]. Second, simulation program with integrated circuit emphasis (SPICE)-based models can be applied to analyze the variation sources of measured $V_{th}$ variation, but it consumes time and makes an error because all devices should be calibrated [15]. Last, models based on
the error propagation law have been proposed [16,17]. These modeling approaches enable extraction of the contribution of each variation source to the standard deviation of $V_{\text{th}}$ ($\sigma_{V_{\text{th}}}$) fast and accurately because they directly model $\sigma_{V_{\text{th}}}$. However, the error propagation law-based model to analyze the $V_{\text{th}}$ variability of SNWFET has not been suggested.

Previously, $V_{\text{th}}$ variability in SNWFETs was investigated considering various $L_G$ using a SPICE-based model [15]. However, the study did not consider the effect of channel dopant concentration ($N_{\text{ch}}$) variation and nanowire diameter ($D_{\text{NW}}$) change. Furthermore, although $D_{\text{NW}}$ influences $W_{\text{eff}}$, electrostatics, and quantum effect [18], the $D_{\text{NW}}$ tendency of $V_{\text{th}}$ variability in SNWFET with short $L_G$ has not been thoroughly investigated.

Therefore, in this study, we quantitatively analyzed the sources of $V_{\text{th}}$ variation in SNWFETs with short $L_G$ (15–22 nm) and multiple $D_{\text{NW}}$ (7, 9, 12 nm). A novel modeling approach based on the error propagation law is proposed to estimate the contribution of multiple variation sources to the $V_{\text{th}}$ variability. The dominant variation source of $V_{\text{th}}$ variation is analyzed for each $D_{\text{NW}}$ by using the proposed model. Additionally, the standard deviation of $N_{\text{ch}}$ ($\sigma_{N_{\text{ch}}}$) and $D_{\text{NW}}$ ($\sigma_{D_{\text{NW}}}$) according to $L_G$ is presented.

2. Device Structure and Modeling Methods
2.1. Structure and Possible $V_{\text{th}}$ Variation Sources of SNWFETs

Figure 1 depicts the schematic and $V_{\text{th}}$ variation sources of SNWFETs, fabricated using the same process flow reported in [19,20]. The SNWFETs adopted Mid-gap TiN metal gate, gate oxide thickness ($t_{\text{ox}}$) of 3.4 nm, and (110) channel direction. The gate and nanowire trimming process was used to obtain $L_G$ varying from 15 to 22 nm and $D_{\text{NW}}$ of 7, 9, and 12 nm. In this process, $D_{\text{NW}}$ variation ($\Delta D_{\text{NW}}$) was caused by LER occurred at the nanowire (NW) edges and under- or over-etching of the NW [21]. MGG occurred in the TiN metal gate and generated the metal work function variation (WFV) [22]. The transmission electron microscope (TEM) image shows many grain boundaries exist in the TiN metal gate, gate oxide thickness ($t_{\text{ox}}$) of 3.4 nm, and (110) channel direction. The gate and nanowire trimming process was used to obtain $L_G$ varying from 15 to 22 nm and $D_{\text{NW}}$ of 7, 9, and 12 nm. In this process, $D_{\text{NW}}$ variation ($\Delta D_{\text{NW}}$) was caused by LER occurred at the nanowire (NW) edges and under- or over-etching of the NW [21]. MGG occurred in the TiN metal gate and generated the metal work function variation (WFV) [22]. The transmission electron microscope (TEM) image shows many grain boundaries exist in the TiN metal gate, gate oxide thickness ($t_{\text{ox}}$) of 3.4 nm, and (110) channel direction. The gate and nanowire trimming process was used to obtain $L_G$ varying from 15 to 22 nm and $D_{\text{NW}}$ of 7, 9, and 12 nm. In this process, $D_{\text{NW}}$ variation ($\Delta D_{\text{NW}}$) was caused by LER occurred at the nanowire (NW) edges and under- or over-etching of the NW [21]. MGG occurred in the TiN metal gate and generated the metal work function variation (WFV) [22].

![Figure 1. Schematic of the silicon nanowire field-effect transistor (SNWFET) and possible $V_{\text{th}}$ variation sources.](image)

Figure 2a depicts the $I_D$–$V_G$ characteristics of SNWFETs with $L_G$ = 15 nm and $D_{\text{NW}}$ = 7 nm at a drain bias of 0.05 V. About 50 samples were measured per device condition. Here, $V_{\text{th}}$ was extracted at $I_D = 10^{-7} \times \pi D_{\text{NW}}/L_G$ using the constant current method. The fluctuation of extracted $V_{\text{th}}$ shows the process and random variation affect the physical characteristics
of SNWFETs. Figure 2b illustrates a quantile plot of $V_{\text{th}}$ for each $D_{\text{NW}}$ in SNWFETs with an $L_{\text{G}}$ of 15 nm, which shows the distribution of $V_{\text{th}}$. The distribution of $V_{\text{th}}$ predominantly follows the theoretical normal distribution for all device conditions, which indicates that sufficient $V_{\text{th}}$ values were obtained to analyze $\sigma V_{\text{th}}$.

Figure 3 is the Pelgrom plot of $\sigma V_{\text{th}}$ in SNWFETs for each $D_{\text{NW}}$, showing the trend of $\sigma V_{\text{th}}$ as channel area changes. The slope of the Pelgrom plot, defined as the Pelgrom coefficient ($A_{\text{vt}}$), represents the effect of random variation [4]. The y-intercept of the Pelgrom plot is also observed, indicating the effect of the process variation and short channel effect [12,24]. Remarkably, the values of $A_{\text{vt}}$ and y-intercepts differed for each $D_{\text{NW}}$, and the $\sigma V_{\text{th}}$ is smallest in median $D_{\text{NW}}$ of 9 nm. We anticipated that this result implies a trade-off relationship between the various variation sources. Hence, a novel modeling approach is proposed to analyze the contribution of each variation source to $\sigma V_{\text{th}}$.

![Graphs showing $V_{\text{th}}$ fluctuation and Pelgrom plot](image_url)

Figure 2. (a) $V_{\text{th}}$ fluctuation in $I_D - V_G$ of silicon nanowire field-effect transistors (SNWFETs) with $L_{\text{G}} = 15$ nm and $D_{\text{NW}} = 7$ nm. $V_{\text{th}}$ is directly extracted using the constant current method at $I_D = 10^{-7} \pi D_{\text{NW}}/L_{\text{G}}$. (b) Quantile plot of $V_{\text{th}}$ of the SNWFET with $L_{\text{G}} = 15$ nm.

![Pelgrom plot](image_url)

Figure 3. Pelgrom plot for $V_{\text{th}}$ variation of the silicon nanowire field-effect transistors (SNWFETs).
2.2. Proposed $\sigma V_{th}$ Model of SNWFETs

Figure 4 shows the proposed modeling flow to analyze the contribution of WFV, $\Delta N_{ch}$, and $\Delta D_{NW}$ to $\sigma V_{th}$. To model $\sigma V_{th}$, we started from a physical model for $V_{th}$ of SNWFET, as follows [25,26]:

$$V_{th} = \Phi_M - \Phi_S - qN\cdot ch\left(\frac{\pi r_{nw}^2}{C_{ox}} + \frac{r_{nw}^2}{4\epsilon_{si}}\right) + \frac{h^2}{4\pi m^* q r_{nw}^2},$$

(1)

where $\Phi_M$ denotes the work function of the TiN gate metal; $\Phi_S$ represents the work function of silicon channel calculated as $X_{si} - E_g/2 + kT/q \cdot \ln(N_{ch}/n_i)$, where $X_{si}$ is the electron affinity and $E_g$ is the band gap of silicon; $r_{nw}$ indicates the radius of NW; $\epsilon_{si}$ and $\epsilon_{ox}$ represent the dielectric constant of silicon and oxide, respectively; $h$ denotes the Planck constant; and $m^*$ indicates the effective mass of an electron. $C_{ox}$ represents the oxide capacitance calculated as $2\pi\epsilon_{ox}/\ln(1+t_{ox}/r_{nw})$. The possible $V_{th}$ variation sources in Equation (1) are $\Phi_M$, $N_{ch}$, $D_{NW}$, and $t_{ox}$ variations. Among them, $t_{ox}$ is not considered because its variation and effect are very small and negligible [11,12,27]. Although the variation of effective channel length ($L_{eff}$) is not considered directly, $N_{ch}$ variation partially represents $L_{eff}$ variation because S/D dopant diffusion and $L_G$ variation change $N_{ch}$ and $L_{eff}$ simultaneously.

Hence, considering three identical variation sources of WFV, $\Delta N_{ch}$, and $\Delta D_{NW}$, $\sigma V_{th}$ can be expressed based on the error propagation law as

$$\sigma V_{th}^2 = \sigma \Phi_M^2 + \left(\frac{\partial V_{th}}{\partial N_{ch}} \sigma N_{ch}\right)^2 + \left(\frac{\partial V_{th}}{\partial D_{NW}} \sigma D_{NW}\right)^2.$$  

(2)

To analyze $\sigma V_{th}$ using Equation (2), the sensitivity of $V_{th}$ against variation sources and their standard deviation should be extracted. First, the standard deviation of metal work function ($\sigma \Phi_M$) can be estimated by the existing WFV model for SNWFETs, as follows [22]:

$$\sigma \Phi_M = RGG \times SL = \frac{G_{size}}{L_G(D_{NW} + 2t_{ox})\pi} \times SL,$$

(3)

where $RGG$ is the ratio of average grain size to the gate area, $SL$ is the sensitivity of $\sigma V_{th}$ against $RGG$, and $G_{size}$ is the grain size of the metal gate. Here, $G_{size}$ can be estimated from

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**Figure 4.** Flowchart of the proposed $\sigma V_{th}$ modeling process.
a TEM image of the TiN metal gate of SNWFETs. SL of SNWFETs can be obtained from previous research based on TCAD simulation [22].

Second, the sensitivity of $V_{th}$ against $\Delta N_{ch}$ and $\Delta D_{NW}$ can be obtained by calculating the partial differentiation of Equation (1), as follows:

$$
\frac{\partial V_{th}}{\partial N_{ch}} = \frac{kT}{q N_{ch}} - q r_{nw}^2 \left( \frac{\ln(1 + t_{ox}/r_{nw})}{2 \varepsilon_{ox}} + \frac{1}{4 \varepsilon_{si}} \right),
$$

(4)

$$
\frac{\partial V_{th}}{\partial D_{NW}} = -\frac{q N_{ch} r_{nw}}{2} \left( \frac{1}{\varepsilon_{ox}} \left( 2 \ln \left( 1 + \frac{t_{ox}}{r_{nw}} \right) - \frac{t_{ox}}{t_{ox} + r_{nw}} \right) + \frac{1}{\varepsilon_{si}} \right) - \frac{h^2}{2 \pi m^* q r_{nw}^3},
$$

(5)

where $k$ denotes the Boltzmann constant. Here, $N_{ch}$ can be extracted where Equation (1) best fits to measured $V_{th}$. Finally, $\sigma N_{ch}$ and $\sigma D_{NW}$ are extracted when Equation (2) best fits the square of the measured $\sigma V_{th}$.

The proposed model obtains the $V_{th}$ sensitivity against $\Delta N_{ch}$ and $\Delta D_{NW}$ through simple calculation and extracts the standard deviation of each variation source by fitting the model to the measured $\sigma V_{th}$. Therefore, the contribution of multiple variation sources to $\sigma V_{th}$ can be directly and quickly modeled and analyzed using the proposed model without any TCAD or SPICE simulation. Furthermore, the proposed $V_{th}$ modeling flow is expected to be applied to analyze $\sigma V_{th}$ in most multigate devices with various $L_G$ and channel thicknesses.

3. Results and Discussion

3.1. $V_{th}$ Modeling Results of SNWFETs

$N_{ch}$ is extracted where Equation (1) fitted $V_{th}$ versus $D_{NW}$ with high accuracy in SNWFET with $L_G$ of 15 nm, as shown in Figure 5a. Figure 5b shows $N_{ch}$ increases as $L_G$ decreases because more dopant diffused to the center of the channel from S/D even with the same S/D junction gradient. The sensitivity of $V_{th}$ against $\Delta N_{ch}$ and $\Delta D_{NW}$ was calculated by substituting $N_{ch}$ and other parameters in Equations (4) and (5).

![Figure 5](image-url)

(a) Measured (black dots) and modeled (blue line) values of $V_{th}$ as a function of $D_{NW}$. (b) Extracted $N_{ch}$ as a function of $L_G$. 

3.2. $V_{th}$ Standard Deviation Modeling Results of SNWFETs

3.2.1. Extraction of $G_{size}$ and WFV of SNWFETs

$G_{size}$ should be determined from the TEM image of the TiN metal gate of the SNWFET to analyze WFV. Figure 6a shows a schematic of the grain boundaries based on TiN metal gate TEM image [19]. $G_{size}$ was measured as the average of values obtained by dividing the length of TiN metal in the TEM image ($L_{TEM}$) by the number of intersections between grain boundaries and horizontal lines ($N_{int}$), as follow [28]:

$$G_{size} = \frac{\sum_{i=1}^{N_{line}} L_{TEM} / (N_{int} + 1)}{N_{line}}$$

where $N_{line}$ is the number of horizontal lines. The distance between the lines was set to 5 nm, as shown in Figure 6a. Consequently, $G_{size}$ measured using Equation (6) was 11.8 nm in SNWFETs. According to previous research, the value of SL is 105 V/nm in SNWFETs [22]. $\sigma\Phi_m$ was calculated by putting obtained $G_{size}$ and SL into Equation (3), and Figure 6b shows $\sigma\Phi_m$ as a function of the square root of the channel area. Interestingly, the trend and value of the slope in Figure 6b ($A_{WFV}$) are very similar to $A_{vt}$ for each $D_{NW}$. It means WFV induced by MGG is the dominant random variation component of $V_{th}$ variation in the SNWFETs.

![Figure 6](image-url)

(a) Grain boundaries estimated from [19] and red horizontal lines to estimate $G_{size}$ of TiN metal gate of SNWFETs. (b) Pelgrom’s plot only considering work function variation (WFV) by metal gate granularity (MGG).

3.2.2. The Contribution of Variation Sources to $\sigma V_{th}$ for Each $D_{NW}$

Figure 7 shows that Equation (2) accurately fitted the measured $\sigma V_{th}$ with the relative root mean square error of 0.3% where $\sigma N_{ch} = 1.11 \times 10^{18}$ cm and $\sigma D_{NW} = 0.743$ nm. WFV and $D_{NW}$ are slightly correlated because $D_{NW}$ is included in Equation (3), which can affect the modeling accuracy. However, assuming the occurrence of $\Delta D_{NW}$ of 0.743 nm, the possible WFV fluctuation is only by 2.4% of total $\sigma V_{th}$, and does not change the $D_{NW}$ tendency of $\sigma V_{th}$ induced by each variation source. The $D_{NW}$ tendency of $\sigma V_{th}$ can be explained by the different contributions of the three variation sources, which are represented using pink (WFV), red ($\Delta N_{ch}$), and green ($\Delta D_{NW}$) lines in Figure 7. The modeling results are shown considering $L_C = 15$ nm; however, the model was also applied to SNWFET with other $L_C$, and the modeling accuracy and trend of each variation sources are very similar. Although $A_{MGG}$ decreases when $D_{NW}$ decreases, the contribution of WFV increases owing to the decrease in the channel area. As $D_{NW}$ decreases, SNWFETs become robust to
\(\Delta N_{ch}\)-induced \(V_{th}\) variation. This is because the influence of depletion charge and surface potential is reduced proportional to \(r_{nw}^2\) because of the improvement in gate-controllability, as shown in Equation (4). Conversely, SNWFETs become vulnerable to \(\Delta D_{NW}\)-induced \(V_{th}\) variation because the sensitivity of \(V_{th}\) to quantum effect is proportional to \(1/r_{nw}^2\), as indicated in Equation (5). Consequently, the contribution of \(\Delta D_{NW}\), WFV, and \(\Delta N_{ch}\) is dominant when at \(D_{NW}\) of 7 nm, 9 nm, and 12, respectively.

\[\text{Figure 7. Model fitting results (blue line) considering WFV (pink line), } \Delta N_{ch} (\text{red line}), \text{ and } \Delta D_{NW} (\text{green line}) \text{ for the measured value of squared } \sigma V_{th} (\text{black dots}). \text{ The model fits were extrapolated for } D_{NW} \text{ of 6 and 15 nm (dashed line).} \]

3.2.3. The Tendency of \(\sigma N_{ch}\) and \(\sigma D_{NW}\) as \(L_G\) Changes

Figure 8 shows both \(\sigma N_{ch}\) and \(\sigma D_{NW}\) increases as \(L_G\) decreases. This result means that RDF and LER occur because their influence increases as the device dimension decreases. However, the degree of \(\sigma N_{ch}\) and \(\sigma D_{NW}\) increase is small, about 5%, as \(L_G\) decreases from 22 to 15 nm. In addition, we already verified WFV by MGG is the dominant random variation component of \(V_{th}\) variation in Section 3.2.1. Hence, most \(\Delta N_{ch}\) and \(\Delta D_{NW}\) originated from process variation sources, which causes non-zero y-intercept in Figure 3.

\[\text{Figure 8. Extracted } \sigma N_{ch} \text{ (black line) and } \sigma D_{NW} \text{ (blue line) as function of } L_G. \]
4. Conclusions

The contribution of WFV, $\Delta N_{ch}$, and $\Delta D_{NW}$ in $V_{th}$ variation of SNWFET was quantitatively analyzed for each $D_{NW}$ using the novel modeling approach. The sensitivity of WFV against the channel area is similar to that of $\sigma V_{th}$. As $D_{NW}$ decreases, SNWFETs became robust to $\Delta N_{ch}$ but vulnerable to $\Delta D_{NW}$. The dominant variation sources differed for each $D_{NW}$. Hence, the strategy to improve the variability of SNWFETs should be different for each $D_{NW}$. Furthermore, with slight modifications, the proposed modeling approach and results are expected to be used in most multigate devices, including FinFET and nanosheet FET.

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