A high voltage diode with partial n+ adjusting region embedded at the anode side

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Abstract A novel high voltage diode featuring partial n⁺ adjusting region embedded at the anode side is proposed and analyzed by device simulation in this paper. The low and inverted on-state carrier profile is obtained to realize the fast and soft recovery behavior. The simulations show that the proposed diode achieves a 21% reduction in the reverse peak current compared with the conventional diode. What’s more, such partial n⁺ adjusting region results in the parasitic npn transistor triggered during reverse recovery, and electrons are injected into the pn⁻ junction to inhibit the peak electric field, improving the dynamic ruggedness.

Keywords: dynamic avalanche, current filament, high voltage diode, reverse recovery

Classification: Power devices and circuits

1. Introduction

Great challenge for the high voltage diode above 3.3 kV in the IGBT application is to ensure the fast and soft recovery behavior, especially the dynamic avalanche capability under extreme over-stress operating condition [1, 2]. Such high di/dt, high parasitic inductance L and high supply voltage V_F can provoke the appearance of dynamic avalanche, leading to the diode destruction [3, 4, 5, 6, 7]. In previous work, the p⁺nn structure has been proposed to improve the reverse recovery behavior [8, 9]. The conventional anode structure, however, is limited to improve the fast and soft recovery behavior, because of the larger carrier concentration at the anode side than at the cathode side for the uniform carrier lifetime [3, 10, 11]. In addition, the carrier lifetime technologies, for instance electron or proton irradiation [12, 13, 14, 15, 16], were introduced to provide a low plasma density in front of p⁺ emitter to improve the fast and soft recovery behavior. Some new cathode structures including the Field Charge Extraction (FCE) cathode [17, 18, 19] and the Controlled Injection of Backside Holes (CIBH) structure [20, 21] were also proposed to improve the dynamic ruggedness. Nevertheless, these cathode structures are only to suppress the second electric field peak at the cathode side by injecting the holes into the n⁻n junction [11, 18, 22], while leading to an unexpected increase in the reverse peak current density (J_RM), hence the power loss increases as well.

In this paper, a novel high voltage diode with the n⁺ adjusting region at the anode side is proposed, and the mechanisms that the npn transistor is triggered and the electric field is modulated by electrons during reverse recovery are studied and simulated. This structure realizes the improved fast recovery behavior and the dynamic avalanche capacity compared with the conventional diode.

2. Device structures and operating mechanism

Fig. 1(a) and (b) show the structure schematics of the conventional diode (CD) and the proposed n⁺ adjusting region diode (NARD), respectively. Two diodes have the same n⁻ base, the same p buffer layer at the anode side, and the same n⁺ emitter and n buffer layer at the cathode side.

The n⁻ base doping is N_p = 2.3 × 10^{13} cm⁻³ and realizes a blocking capability of 3.3 kV. The p and n buffer layers are both the Gaussian doping profiles, and the corresponding surface doping concentrations are 8 × 10^{15} cm⁻³ and 1.0 × 10^{16} cm⁻³, respectively. However, the only difference is that the highly doped n⁺ adjusting region with a surface doping concentration of 1.0 × 10^{20} cm⁻³ are embedded in the p⁺ emitter in the NARD, and the width of the n⁺ adjusting region (W_n) is 5.2 µm.

During reverse recovery, the NARD structure is equivalent to a conventional diode in parallel with an npn transistor, in which the n⁺ adjusting region of the anode side acts as the emitter, and the p buffer layer acts as the base, and the n⁻ base of the diode represents the collector, as shown in Fig. 1(b). The local current flow of the anode side during reverse recovery in the NARD is illustrated in Fig. 1(c). At the initial stage of reverse recovery, the holes extracted from the n⁻ base flow laterally across the p buffer layer underneath the n⁺ adjusting region of the anode side.

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As a result, the current \( I_p(x) \) flows through the p⁺ emitter, leading to the voltage drop \( V_F(t) \) across the resistance \( (R_p) \) of the p buffer layer. With the increase of reverse current density, when the reverse voltage \( V_F(t) \) is equal to \( V_{bi} \) about 0.7 V, the parasitic npn transistor is triggered, and electrons of the n⁺ adjusting region start to inject into the p buffer layer.

The condition for the forward biasing of the pn⁺ junction at the anode side during reverse recovery can be derived by two dimensional analysis. From the Fig. 1(c), the reverse current flows through the p buffer layer from the middle of the n⁺ adjusting region (at point A) to the p⁺ emitter (at point B). The current flowing through a variation part \( (dx) \) in the p buffer layer along the anode side direction is expressed by \( dI_p \). Therefore, the reverse current flowing through the p buffer layer from the middle of the n⁺ adjusting region (at point A) to \( x \) is given by

\[
I_p(x) = \int_0^x dI_p = \int_0^x J_R L dx = J_R L x
\]  

(1)

where \( L \) is the length of the n⁺ adjusting region perpendicular to the cross section of two dimension. The p buffer resistance of the dX thickness is given by

\[
dR_p = \frac{d\rho_p}{dx}
\]  

(2)

where \( \rho_p \) is the sheet resistance in the p buffer layer beneath the n⁺ adjusting region. The voltage drop caused by the current in dX is expressed by \( dV_F(x) \). Therefore, the total voltage drop between point A to point B is as follows:

\[
V_F(A) = \int_0^{W_p/2} dV_F dx = \int_0^{W_p/2} J_R \rho_p x dx = \frac{1}{8} J_R \rho_p W_p^2
\]  

(3)

where \( W_p \) denotes the width of the n⁺ adjusting region, and \( \rho_p \) can be expressed as [18, 23]

\[
\rho_p = \frac{1}{q \mu_p [N_{ap} + p(t)] H_p}
\]  

(4)

where \( H_p \) is the depth of p buffer layer, \( N_{ap} \) is the doping concentration of p buffer layer, \( p(t) \) is the hole density of p buffer layer during reverse recovery, \( \mu_p \) is the hole mobility. The triggered condition of the parasitic npn transistor is as follows

\[
V_F(t) = \frac{J_R(t) W_p^2}{8 q \mu_p [N_{ap} + p(t)] H_p} \geq V_{bi} \approx 0.7 \text{ V}
\]  

(5)

Based upon the Eq. (5), it can be concluded that the injection efficiency of the npn transistor mainly depends on \( J_R(t), W_p, N_{ap} \) and \( H_p \).

### 3. Results and analyses

The diodes were simulated by the Sentaurus-TCAD software. Auger and Shockley-Read-Hall recombination models, carrier-carrier scattering, doping dependent and electric field dependent mobility models, and avalanche generation model were taken into account [3]. An over-stress condition with \( V_{dc} = 2.5 \text{ kV}, J_F = 100 \text{ A/cm}^2, L = 1.25 \mu \text{H} \) and \( dV/dt = 2000 \text{ A/\mu s} \) was considered during reverse recovery.

Fig. 2(a) shows the forward conduction characteristics of two diodes. The carrier lifetimes in the simulation are adjusted to have the same forward voltage drop \( V_F = 2.25 \text{ V} \) at the rated current density \( J_{rated} = 100 \text{ A/cm}^2 \). The carrier lifetimes for the conventional diode are \( \tau_p = 0.5 \mu \text{s} \) and \( \tau_n = 2.5 \mu \text{s} \), and for the NARD \( \tau_p = 0.75 \mu \text{s} \) and \( \tau_n = 3.75 \mu \text{s} \). Compared with the conventional diode, the forward voltage drop in the NARD increases below \( J_{rated} = 100 \text{ A/cm}^2 \) (shown in the illustration), due to the lower carrier density in front of the n⁺ adjusting region. This leads to the inverted carrier profile, i.e., the carrier concentration of the cathode side is larger than the anode side, as shown in Fig. 2(b). It is critical to obtain the fast and soft recovery behavior [10].

Fig. 3 compares the reverse breakdown characteristics at \( T = 300 \text{ K} \) and at \( T = 400 \text{ K} \) in two diodes. The p buffer layer was carefully designed to prevent the electric field from punching through the n⁺ adjusting region under static blocking condition. Therefore, the NARD has the same breakdown voltage as the conventional diode at the onset of static avalanche. However, it shows a lower leakage current both at room and high temperatures, because of larger carrier lifetimes in the n⁻ base. Even under high avalanche current density, the NARD structure still exhibits the same positive and negative differential resistance branches as the conventional diode, which attributes to the buffer layers at both sides, leading to the improvement of static avalanche capability [24, 25, 26, 27].

The comparison of reverse recovery characteristics in two diodes are shown in Fig. 4. The dotted line represents the electron current density at the anode side during reverse recovery in the NARD. It shows that the parasitic npn transistor at the anode side is triggered at \( t = 1.705 \mu \text{s} \). Compared with the conventional diode, the NARD shows the faster reverse recovery with a reduced time of 40 ns and the lower reverse peak current density with a 21% reduc-
tion. These are attributed to the lower on-state carriers stored in front of the p buffer layer and the less carriers generated by weak dynamic avalanche during reverse recovery in the NARD, and the less extracted holes compensated by the injected electrons of the npn transistor.

![Fig. 3. Comparison of reverse breakdown characteristics at \( T = 300 \text{ K} \) and at \( T = 400 \text{ K} \) in two diodes.](image1)

![Fig. 4. Comparison of reverse recovery characteristics of two diodes during reverse recovery.](image2)

The dynamic avalanches are analyzed by the evolution of electric field distributions at different times in two diodes, as shown in Fig. 5. For the conventional diode, at the pn\(^{-}\) junction the electric field gradient in the n\(^{-}\) base region can be given by [28, 29]

\[
\frac{dE}{dy} = \frac{q(N_D + p_e)}{\varepsilon} 
\]

(6)

where \( p \) is the on-state holes, \( p_e \) is the avalanche generated holes, and \( N_D \) is the ionized donors in the n\(^{-}\) base region. This leads to a high peak electric field strength of \( E_{pn^{-}} = 2.27 \times 10^5 \text{ V/cm} \) at the pn\(^{-}\) junction at \( t_4 = 1.85 \mu\text{s} \). A strong Egawa field [27, 30, 31] occurs, and this may lead to the diode failure. The electric field crowding is caused by the current filament generated by dynamic avalanche, because the electric field inside the current filament is higher [3, 4, 5, 6, 7]. For the NARD, however, electrons are injected by the npn transistor, and the electric field gradient is then given by

\[
\frac{dE}{dy} = \frac{q(N_D + p_e + p_{av})}{\varepsilon} 
\]

(7)

where \( n \) is the electrons injected by the npn transistor. The electrons compensate the holes injected on-state and generated by dynamic avalanche, resulting in the decrease of the peak electric field strength at the pn\(^{-}\) junction. In Fig. 5(b), at \( t_1 = 1.7 \mu\text{s} \), the peak electric field strength at the pn\(^{-}\) junction reaches a maximum value \( E_{pn^{-}} = 2.04 \times 10^5 \text{ V/cm} \). Then it decreases dramatically after the npn transistor triggering at \( t_2 = 1.75 \mu\text{s} \). As a result, the dynamic avalanche at the pn\(^{-}\) junction decreases. In the NARD, the less avalanche generated electrons at the pn\(^{-}\) junction move towards the cathode side, leading to a lower \( E_{pn^{-}} = 1.48 \times 10^5 \text{ V/cm} \) as well. This avoids the strong dynamic avalanches at both sides.

![Fig. 5. Evolution of electric field distributions at different times in (a) the conventional diode (\( x = 79 \mu\text{m} \)) and in (b) the NARD (\( x = 60 \mu\text{m} \)).](image3)

Fig. 6 shows the dependence of the electron injection efficiency \( \gamma_n (J_n/J_R) \) on \( W_n \), \( H_p \) and \( N_{ap} \) in the NARD. The electron injection efficiency \( \gamma_n \) of the npn transistor is determined by \( V_f(t) \) of Eq. (5). Hence, as explained in Eq. (5), \( \gamma_n \) is also dependent on \( W_n \), \( H_p \) and \( N_{ap} \). It is obvious from this figure that \( \gamma_n \) increases with the increase of \( W_n \), and decreases with the increases of \( H_p \) and \( N_{ap} \). It also shows that the npn transistor is triggered into its on-state mode earlier for a increase in \( \gamma_n \). In Fig. 6(b), the npn transistor maintains the turn-off state during reverse recovery when \( H_p \) increases to 19 \( \mu\text{m} \). These are in agree with Eq. (5).

The relationship between the electron injection efficiency (\( \gamma_n \)) and the peak electric field strength of pn\(^{-}\) junction at the anode side has been added, as shown in Fig. 7. For the conventional diode, with the carrier extraction of the n\(^{-}\) base, the peak electric field strength at the pn\(^{-}\) junction increases gradually. At \( t_4 = 1.85 \mu\text{s} \), the electric field strength reaches the maximum of \( E_{pn^{-}} = 2.27 \times 10^5 \text{ V/cm} \), due to the current filament generated by dynamic avalanche. Then the peak electric field strength decreases.

For the NARD, the electric field strength reaches the maximum of \( E_{pn^{-}} = 2.04 \times 10^5 \text{ V/cm} \) before the electron injection (\( t_1 = 1.7 \mu\text{s} \)). The npn transistor is triggered at \( t = 1.705 \mu\text{s} \), and the holes including that of on-state injection and the avalanche generation are compensated by injected electrons, leading to the decrease of peak electric...
field. With the $\gamma_n$ reaching the peak at $t_3 = 1.8 \, \mu s$, the minimum of electric field strength occurs. Meanwhile, the reverse current density reaches its peak value ($J_{RM}$), and thereafter the plasma layer disappears. This leads to the rising of electric field distribution in the n$^+$ base, provoking the peak electric field strength of the pn$^-$ junction increases again.

4. Conclusion

A novel high voltage diode featuring partial n$^+$ adjusting region embedded at the anode side is proposed. The triggering condition of $V_P(t) \geq 0.7 \, V$ for the parasitic npn transistor is derived in relation to the parameters of $W_n$, $H_p$ and $N_{eq}$. The npn transistor is triggered with the increase of reverse current density during reverse recovery. The electrons are injected to compensate the holes at the pn$^-$ junction. The simulations show that the peak electric fields decrease at both sides, and the dynamic avalanche capability is improved. Moreover, it shows a lower leakage current without sacrificing reverse blocking voltage.

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References

[1] T. Minato and K. Sato: “Future trend of Si power device,” IEICE Electron. Express 11 (2014) 20142002 (DOI: 10.1587/exle.11.20142002).
[2] J. Xie, et al.: “A snapback-free reverse conducting IGBT with recess and floating buffer at the backside,” IEICE Electron. Express 14 (2017) 20170677 (DOI: 10.1587/exle.14.20170677).
[3] L. Zhang and C. Wang: “Influence of carrier lifetime distribution on the current filament in high voltage diode,” Microelectronics Reliab. 72 (2017) 75 (DOI: 10.1016/j.microrel.2017.04.001).
[4] C. Wang, et al.: “Inhibition of peak electric field shifting on current filaments of high voltage diode,” Microelectronics. Reliab. 94 (2019) 13 (DOI: 10.1016/j.microrel.2019.01.008).
[5] H. Schulze, et al.: “Limiting factors of the safe operating region for power devices,” IEEE Trans. Electron Devices 60 (2013) 551 (DOI: 10.1109/TED.2012.2225148).
[6] R. Baburske, et al.: “ Destruction behavior of power diodes beyond the SOA limit,” ISPSD (2012) 365 (DOI: 10.1109/ISPSD.2012.6229097).
[7] R. Baburske, et al.: “Cathode-side current filaments in high-voltage power diodes beyond the SOA limit,” IEEE Trans. Electron Devices 60 (2013) 2308 (DOI: 10.1109/TED.2013.2264839).
[8] M. Chen, et al.: “Analysis of a p$^+$ n$^−$ n$^+$ diode structure,” ISPSD (2008) (DOI: 10.1109/ISPSD.2008.4538921).
[9] S. Matthias, et al.: “Field shielded anode (FSA) concept enabling higher temperature operation of fast recovery diodes,” ISPSD (2011) 88 (DOI: 10.1109/ISPSD.2011.5980797).
[10] J. Lutz: “Fast recovery diodes - reverse recovery behaviour and dynamic avalanche,” ICM (2004) 11 (DOI: 10.1109/ICMEL.2004.1314549).
[11] J. Lutz, et al.: Semiconductor Power Devices: Physics, Characteristics, Reliability (Springer, Berlin, 2011) 426.
[12] J. Vobecký, et al.: “Impact of the electron, proton and helium irradiation on the forward I–V, characteristics of high-power P–I–N diode,” Microelectronics. Reliab. 43 (2003) 537 (DOI: 10.1016/S0026-2714(03)00023-4).
[13] L. Pina and J. Vobecký: “High-power silicon P–I–N diode with cathode shorts: The impact of electron irradiation,” Microelectronics. Reliab. 53 (2013) 681 (DOI: 10.1016/j.microrel.2013.02.008).
[14] J. Vobecký and P. Hazdra: “Advanced local lifetime control for higher reliability of power devices,” Microelectronics. Reliab. 43 (2003) 1883 (DOI: 10.1016/S0026-2714(03)00320-2).
[15] J. Vobecký, et al.: “Crossing point current of electron and proton irradiated power P–I–N diodes,” Microelectronics. Reliab. 40 (2000) 427 (DOI: 10.1016/S0026-2714(99)00244-9).
[16] P. Hazdra, et al.: “Axial lifetime control in silicon power diodes by irradiation with protons, alphas, low and high-energy electrons,” Microelectronics J. 35 (2004) 249 (DOI: 10.1016/S0026-
[17] A. Kopta and M. Rahimo: “The field charge extraction (FCE) diode: A novel technology for soft recovery high voltage diodes,” ISPSD (2005) 83 (DOI: 10.1109/ISPSD.2005.1487956).

[18] C. Wang and L. Zhang: “An analysis of the dynamic avalanche mechanism of an improved FCE diode with a deep p+ adjusting region,” J. Semicond. 36 (2015) 044006 (DOI: 10.1088/1674-4926/36/4/044006).

[19] S. Matthias, et al.: “Inherently soft free-wheeling diode for high temperature operation,” ISPSD (2013) 335 (DOI: 10.1109/ISPSD.2013.6694416).

[20] M. Chen, et al.: “A novel diode structure with controlled injection of backside holes (CIBH),” ISPSD (2006) 1 (DOI: 10.1109/ISPSD.2006.1666058).

[21] H. P. Felsl, et al.: “The CIBH diode - great improvement for ruggedness and softness of high voltage diodes,” ISPSD (2008) 173 (DOI: 10.1109/ISPSD.2008.4538926).

[22] J. Lutz, et al.: “The nn+ junction as the key to improved ruggedness and soft recovery of power diodes,” IEEE Trans. Electron Devices 56 (2009) 2825 (DOI: 10.1109/TED.2009.2031019).

[23] B. Jayant Baliga: Fundamentals of Power Semiconductor Devices (Springer, Raleigh NC, 2012) 930.

[24] B. Heinze, et al.: “Influence of buffer structures on static and dynamic ruggedness of high voltage FWDs,” ISPSD (2005) 215 (DOI: 10.1109/ISPSD.2005.1487989).

[25] H. P. Felsl, et al.: “Effects of different buffer structures on the avalanche behaviour of high voltage diodes under high reverse current conditions,” IEE Proc. Circ. Devices Syst. 153 (2006) 11 (DOI: 10.1049/ip-cds:20050060).

[26] B. Heinze, et al.: “Ruggedness analysis of 3.3 kV high voltage diodes considering various buffer structures and edge terminations,” Microelectronics J. 39 (2008) 868 (DOI: 10.1016/j.mejo.2007.11.023).

[27] C. Wang and L. Zhang: “Peak electric field shifting induced by avalanche injection under static avalanche in high voltage diode,” IEICE Electron. Express 14 (2017) 20170627 (DOI: 10.1587/elex.14.20170627).

[28] J. Lutz and R. Baburske: “Dynamic avalanche in bipolar power devices,” Microelectron. Reliab. 52 (2012) 475 (DOI: 10.1016/j.microrel.2011.10.018).

[29] J. Vobeczky and P. Hazdra: “Dynamic avalanche in diodes with local lifetime control by means of palladium,” Microelectronics J. 39 (2008) 878 (DOI: 10.1016/j.mejo.2007.11.003).

[30] H. Egawa: “Avalanche characteristics and failure mechanism of high voltage diodes,” IEEE Trans. Electron Devices ED-13 (1966) 754 (DOI: 10.1109/T-ED.1966.15838).

[31] L. Zhang, et al.: “Destruction behavior in high voltage diode with the field limiting ring termination,” IEICE Electron. Express 16 (2019) 20190076 (DOI: 10.1587/elex.16.20190076).