DESIGN AND ANALYSIS OF CASCADED H BRIDGE NINE-LEVEL INVERTER IN TYPHOON HIL

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Abstract. As the pressure on renewable energy resources like wind and solar is growing continuously because of the tremendous rise in electrical energy consumption, inverters are playing an important part. The problem with the conventional two-level inverter is that it has high harmonic pollution and low power rating. These problems limit the use of these inverters in high power applications. Therefore, the trend towards multilevel inverters is gaining more and more interest in researchers these days. In multilevel inverters, by providing a certain switching sequence, various voltage levels can be generated in a staircase manner as close as possible to a sinusoidal waveform. In this paper, Cascaded H Bridge (CHB) based nine-level inverter is designed using Typhoon Hardware-in-loop (HIL) Simulator. The Typhoon HIL Simulator is a real-time simulator that gives real-time results. The designed multilevel inverter has been analyzed for different levels. The obtained results reveal that with the increase in number of levels, the Total Harmonic Distortion (THD) of the inverter reduces.

Keywords: Multilevel, THD, Switching, Typhoon HIL, Inverter.

1. Introduction

The energy crisis is one of the grave problems that humankind is facing these days. Due to the continuous increase in population, the consumption of electrical energy is increasing continuously and hence its demand. Therefore the trend towards renewable energy sources is gaining more and more attention[1][2]. Renewable energy being clean has very low environmental impacts. The major source of renewable energy is the sun, but the output of solar photovoltaic (PV) based renewable energy sources is pure dc in nature and is not usable to consumers, hence it must be converted into smooth ac waveform[3][4]. Inverters are used for such purposes. But the output of a simple two-level inverter (+Vdc and -Vdc) contains a lot of harmonics which need to be filtered out[5][6]. If the same inverter is used for high power applications then the switches will face high current and voltage[7]. Moreover, the high-frequency application is also hindered by such an inverter because of high power losses. To address all these problems, Multilevel Inverters (MLI) are used which produce a staircase type of waveform close to sinusoidal by using appropriate switching combination along with different DC voltage sources[8]–[10]. The so-called ‘Multilevel’ starts at three levels. MLI’s also reduce harmonics to a large extent and consequently the filter size and power losses also get reduced remarkably[11]–[13]. One of the biggest weakness of conventional converters which prevent their use in high power applications
is high harmonic pollution, limited power rating and high switching frequency. In case of MLI, there is less distortion in the output voltage because of multiple levels and also low switching loss because of lower switching frequency[14]–[16]. There are various topologies of MLI’s. Cascaded H Bridge (CHB), Flying Capacitor (FC) and Diode Clamped (DC) topologies being the prominent ones[17]–[19]. CHB based MLI’s are very commonly used in industry and high-power applications because they require a lesser number of components in comparison to FC and DC topology and hence are considered superior[20]–[22].

In this paper, Typhoon Hardware-in-Loop (HIL) Simulator is used for the design and analysis of CHB based multilevel inverter (MLI). The main advantage of using Typhoon HIL is that it is a real-time simulator and hence there is a very small variation between the obtained results and practical results. This paper is organized as follows. First of all, the description of CHB based nine-level inverter topology is presented. Then comes the modeling of described inverter topology in Typhoon HIL Simulator which is followed by the analysis and results of the described nine-level inverter. Finally, a comparison between different levels is drawn and the paper is concluded.

2. Description
MLI primarily consists of dc voltage sources, switching devices and a control circuit for the desired switching. By using controlled switching sequences, various voltage levels can be obtained and the resultant is close to a sinusoidal waveform. Figure 1. shows CHB based nine-level inverter. There are sixteen semiconductor switches along with four voltage sources of the same voltage rating. For generating ‘n’ different voltage levels in the output, we require (2n - 2) switches. Eight switches conduct in one cycle. For generating ‘V’ volts, switches S1, S4, S5, S7, S9, S11, S13 and S15 are required to conduct. For generating ‘-V’ volts, switches S2, S3, S6, S8, S10, S12, S14 and S16 are required to conduct. Similarly, other voltage levels can be obtained. To obtain a staircase type of voltage waveform close to a sinusoidal waveform, the switches are properly operated and allowed to conduct only for a particular time period. Also, with the increase in the number of output voltage levels, there is a considerable reduction in THD as well.

The complete switching sequence for a CHB based nine-level inverter is given in Table 1.
Table 1. Switching sequence for CHB Nine-Level Inverter.

| States → | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|----------|---|---|---|---|---|---|---|---|---|
| Switches | -4V | -3V | -2V | -V | 0 | V | 2V | 3V | 4V |
| S1       | 0 | 0 | 0 | 0 | - | 1 | 1 | 1 | 1 |
| S2       | 1 | 1 | 1 | 1 | - | 0 | 0 | 0 | 0 |
| S3       | 1 | 1 | 1 | 1 | - | 0 | 0 | 0 | 0 |
| S4       | 0 | 0 | 0 | 0 | - | 1 | 1 | 1 | 1 |
| S5       | 0 | 0 | 0 | 0 | - | 1 | 1 | 1 | 1 |
| S6       | 1 | 1 | 1 | 1 | - | 0 | 0 | 0 | 0 |
| S7       | 1 | 1 | 1 | 1 | - | 0 | 0 | 0 | 0 |
| S8       | 0 | 0 | 0 | 0 | - | 1 | 1 | 1 | 1 |
| S9       | 0 | 0 | 0 | 0 | - | 1 | 1 | 1 | 1 |
| S10      | 1 | 1 | 1 | 1 | - | 0 | 0 | 0 | 0 |
| S11      | 1 | 1 | 0 | 0 | - | 1 | 1 | 0 | 0 |
| S12      | 0 | 0 | 1 | 1 | - | 0 | 0 | 1 | 1 |
| S13      | 0 | 0 | 0 | 0 | - | 1 | 1 | 1 | 0 |
| S14      | 1 | 1 | 1 | 1 | - | 0 | 0 | 0 | 1 |
| S15      | 1 | 0 | 0 | 0 | - | 1 | 1 | 1 | 0 |
| S16      | 0 | 1 | 1 | 1 | - | 0 | 0 | 0 | 1 |

3. Modeling of CHB Nine-Level Inverter in Typhoon HIL

In order to model CHB nine-level inverter in Typhoon HIL, open the Typhoon HIL Schematic editor and create a new model. From the library explorer in the Contactors section click on the Non-Ideal Contactor and insert Single Non-Ideal Contactor (Contactors > Non-Ideal Contactors > Single Non-Ideal Contactor). Double click on it and model it as a switch and change zero current to required current. From the library explorer in the sources section, insert voltage source and keep its voltage constant at 12V. Assuming the inverter shown in fig. 1. to be made of four modules, make a similar module by connecting two switches in series at one side and another two sides on the other side and clamping a voltage source. For a nine-level output, make three more modules and connect them as shown in fig. 1. Now, insert resistance block from passive elements in the library explorer and connect it between the upper module and lower module as shown in fig. 1. From the measurements section, insert voltage measurement and connect it in parallel to the resistor. Moreover, for the total harmonic distortion (THD) measurement, go to the Signal Processing section click on the Power measurement section and insert the THD block and connect it to the voltage measurement block. Before connecting the THD block to voltage measurement block, double click on the voltage measurement block and change signal processing from false to true. In order to see the THD at supervisory control and data acquisition (SCADA) window, a probe (namely THD) is connected as well.

The most important part of modeling multilevel inverter is the switching sequence. Square wave Source can be used for triggering of switches and can be inserted from the signal processing section by clicking on Sources (Signal Processing > Sources > Square wave source). Double-clicking on it will enable it for model and control (for controlling duty cycle and phase delay).

The full switching pattern (duty cycle and phase delay) for a CHB nine-level inverter is presented in Table 2.

As evident from Table 2, for a nine-level output, one complete cycle is divided into eighteen parts. Switch 1 has a duty cycle of 8/18 p.u. and is given a phase delay of 17/18 p.u. Similarly,
other switches are controlled by allowing them to conduct for a fixed time period and by giving them a certain phase delay. Some switches conduct discontinuously that is why they have more than one duty ratio and phase delays as evident from Table 2. Based on these switching patterns, different voltage levels are generated and the resultant waveform is a staircase type close to sinusoidal. When all the connections are done then save the model and after that compile it. After compiling, load the model in HIL SCADA for analysis purposes which is given in the next section.

4. Results and Discussion

Once the model is loaded in HIL SCADA, create a new panel. From the widget library in the monitoring section insert Digital Display. Double click on it and select the output parameter as an analog signal. Also, select the quantity to be shown on the digital display. Here, we are interested to see THD so Probe namely THD is selected. To obtain the output voltage waveform, Capture/Scope has been used (from the monitoring section in the widget library). One can have the image of the model in the panel as well by saving the model as an image prior to loading it in HIL SCADA. Now run the HIL SCADA. After running the HIL SCADA, it is found that for a nine-level inverter THD is coming out to be 15.61% (as shown in Fig.2)

The output voltage waveform of the CHB based nine-level Inverter is shown in Fig. 3. The obtained output voltage waveform is a staircase type of voltage which is close to the sinusoidal waveform (as required). The peak of voltage waveform is 48V (as expected) and THD is 15.61.

5. Comparative Evaluation

Similar models (CHB) have been made for three-level, five-level and seven-level output and THD was calculated. The results of these models are presented in fig. 4. The desired result is obtained by using an appropriate switching sequence and allowing a particular switch to conduct for a fixed period by giving a certain phase delay. The complete switching pattern showing duty ratio

| Switch | Duty cycle (p.u.) | Phase delay (p.u.) |
|--------|-------------------|--------------------|
| 1      | 8/18              | 17/18              |
| 2      | 8/18              | 8/18               |
| 3      | 8/18              | 8/18               |
| 4      | 8/18              | 17/18              |
| 5      | 8/18              | 17/18              |
| 6      | 8/18              | 8/18               |
| 7      | 1/18, 1/18, 6/18 | 17/18, 10/18, 6/18 |
| 8      | 6/18, 1/18, 1/18 | 16/18, 8/18, 1/18  |
| 9      | 8/18              | 17/18              |
| 10     | 8/18              | 8/18               |
| 11     | 2/18, 2/18, 4/18 | 17/18, 11/18, 6/18 |
| 12     | 4/18, 2/18, 2/18 | 15/18, 8/18, 2/18  |
| 13     | 8/18              | 17/18              |
| 14     | 8/18              | 8/18               |
| 15     | 3/18, 3/18, 2/18 | 17/18, 12/18, 5/18 |
| 16     | 2/18, 3/18, 3/18 | 14/18, 8/18, 3/18  |
and phase delay of the above-mentioned models is presented in Tables 3, 4 and 5 respectively for obtaining three, five and seven-level output.

For a three-level output, two switches conduct at a time. For a five-level output, four switches conduct at a time. So, in general for an ‘M’ level output, ‘M-1’ switches need to conduct simultaneously. Table 6. presents the comparison of different multilevel inverters (CHB based). Comparison has been drawn by taking into account the number of levels, number of switches and the number of voltage sources. Because the presence of such components in the inverter makes it bulky and uneconomic.

It can be concluded from Table 3 that with the increase in the number of levels, the number
Figure 4. The different output voltage level of CHB topology

Table 3. Switching pattern of Three Level Inverter.

| Switch | Duty cycle (p.u.) | Phase delay (p.u.) |
|--------|------------------|-------------------|
| 1      | 2/6              | 5/6               |
| 2      | 2/6              | 2/6               |
| 3      | 2/6              | 2/6               |
| 4      | 2/6              | 5/6               |

Table 4. Switching pattern of Five Level Inverter.

| Switch | Duty cycle (p.u.) | Phase delay (p.u.) |
|--------|------------------|-------------------|
| 1      | 4/10             | 9/10              |
| 2      | 4/10             | 4/10              |
| 3      | 4/10             | 4/10              |
| 4      | 5/10             | 9/10              |
| 5      | 4/10             | 9/10              |
| 6      | 4/10             | 4/10              |
| 7      | 1/10, 1/10, 2/10 | 9/10, 6/10, 3/10  |
| 8      | 2/10, 1/10, 1/10 | 8/10, 4/10, 1/10  |

of switches and voltage sources increases but there is a drastic reduction in the total harmonic distortion (THD). It implies that in an MLI, more the number of output voltage levels lesser is the THD and hence more is the efficiency.

6. Conclusion
In this paper, modeling and analysis of CHB nine-level inverter are presented using Typhoon HIL Simulator. The modeling of the nine-level inverter is done in Schematic Editor and the analysis is done in HIL SCADA. CHB topology was chosen because of its superiority over other topologies. Different levels of CHB based multilevel inverter can be obtained by using an appropriate switching sequence. The comparison between different levels, number of switches, number of voltage sources and THD is drawn and it was found that more the number of levels lesser is the THD. Typhoon HIL was used for simulation purpose and hence the obtained results are real-time results.
Table 5. Switching pattern of Seven Level Inverter.

| Switch | Duty cycle (p.u.) | Phase delay (p.u.) |
|--------|-------------------|--------------------|
| 1      | 6/14              | 13/14              |
| 2      | 6/14              | 6/14               |
| 3      | 6/14              | 6/14               |
| 4      | 6/14              | 13/14              |
| 5      | 6/14              | 13/14              |
| 6      | 6/14              | 6/14               |
| 7      | 1/14, 1/14, 4/14  | 13/14, 8/14, 5/14  |
| 8      | 4/14, 1/14, 1/14  | 12/14, 6/14, 1/14  |
| 9      | 6/14              | 13/14              |
| 10     | 6/14              | 6/14               |
| 11     | 2/14, 2/14, 2/14  | 13/14, 8/14, 4/14  |
| 12     | 2/14, 2/14, 2/14  | 11/14, 6/14, 2/14  |

Table 6. Comparison of different MLI models (CHB)

| S. No. | Levels of MLI | No. of switches | No. of voltage sources | THD(%) |
|--------|---------------|-----------------|------------------------|--------|
| 1      | 3             | 4               | 1                      | 31.45  |
| 2      | 5             | 8               | 2                      | 20.46  |
| 3      | 7             | 12              | 3                      | 16.98  |
| 4      | 9             | 16              | 4                      | 15.61  |

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