Partial Isolation Type Buried Channel Array Transistor (Pi-BCAT) for a Sub-20 nm DRAM Cell Transistor

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Received: 14 October 2020; Accepted: 5 November 2020; Published: 13 November 2020

Abstract: In this paper, we propose a new buried channel array transistor structure to solve the problem of current leakage occurring in the capacitors of dynamic random-access memory (DRAM) cells. This structure has a superior off current performance compared with three previous types of structures. In particular, the proposed buried channel array transistor has a 43% lower off current than the conventional asymmetric doping structure. Here, we show the range of the effective buried insulator parameter according to the depth of the buried gate, and we effectively show the range of improvement for the off current.

Keywords: gate induced drain leakage (GIDL); buried channel array transistor (BCAT); on current ($i_{on}$); off current ($i_{off}$); potential drop width (pdw); asymmetric doping structure

1. Introduction

As the dynamic random-access memory (DRAM) cell size decreases, DRAM reduces the size of the line width and length of the gate [1,2]. As a result, this increases the short-channel effect of the conventional planar MOSFET [3,4]. In order to increase the channel length of the gate, a recessed channel array transistor that increases the length of the channel by providing a recessed channel area below the existing gate is proposed [5]. The recessed channel array transistor improves the short channel effect, but has the problem that the long channel length decreases the on current [6]. Likewise, Fin field effect transistor (FinFET) with three-sided channels improves the short-channel effect and on current, but the off current increases because of the increase in the area of the overlapped region of the gate and drain [7,8]. To compensate for this, a saddle-type FinFET is proposed by adding gates on both sides of the recessed channel array transistor [9–11]. However, the saddle-type FinFET has an increased gate induced drain leakage (GIDL) because of its wider overlapped regions of gate and drain compared with the recessed channel array transistors [12]. RFFinFET is a structure that improves gate induced drain leakage, and unlike a saddle-type FinFET structure, the side gate areas of RFFinFET are installed only in the channel area [13,14]. The buried channel array transistor that is currently being manufactured is a structure in which the gate is buried in the structure of RFFinFET, and the overlapped region between the gate and drain is reduced [15,16]. However, there is a limit to the amount the overlapped region of gate and drain under the structure can be reduced. In addition, the continuous reduction in the size of the line width requires a cell size of less than 20 nm, and the high doping concentration increases the GIDL [17]. To solve this problem, the existing structure currently being manufactured needs to be improved. This paper proposes a structure that is partially isolated in the area below the storage node of the buried channel array transistor (Pi-BCAT) for a DRAM cell transistor of less than 20 nm [18–21]. In addition, the current of buried channel-array transistors with
the same size and similar shape as the existing fabricated structure (asymmetric doping structure) are compared [22–24]. Next, the parameters of the buried insulator are introduced, and the optimized values are proposed. The structures presented in this paper are fabricated using a 3D device simulation (sentaurus TCAD). These device structures use a Gaussian distribution of the doping concentration in order to provide a reliable doping profile [25–27].

2. Device Structure

The partial isolation type buried channel array transistor (Pi-BCAT) is a structure that has a buried insulator at a certain depth from the storage node of the buried channel array transistor (BCAT). Figure 1 shows the 3D structure of a Pi-BCAT. In Figure 1, the first of the important parameters, $L_{in}$, is the distance between the gate oxide and the insulator, while the second is the silicon film thickness, which is the distance from the storage node contact surface to the buried insulator.

![3D structure of a partial isolation type buried channel array transistor (Pi-BCAT).](image)

Figure 1. 3D structure of a partial isolation type buried channel array transistor (Pi-BCAT).

The third is the gate depth, which means the distance to the buried gate based on the storage node contact surface. Figure 2 shows a cross-sectional view of $x$–$z$ when $y = 0$ for two saddle RFinFET structures and three buried channel array transistor structures all possessing the same cell sizes. Figure 2a shows the structure of a saddle RFinFET, while Figure 2b shows a Pi-RFinFET with a buried insulator in the doping region at the bottom of the storage node in the structure of Figure 2a [27]. Figure 2c shows an asymmetric doping structure (asymmetry) with a short doping junction depth at the bottom of the storage node, and a long doping junction depth at the bottom of the bit line.
contact. Figure 2d shows a doping junction depth with a longer area at the bottom of the storage node than in Figure 2c. Figure 2e shows a Pi-BCAT structure with a buried insulator in the doping region below the storage node in the structure of Figure 2d. The device parameters in Figure 2 are as follows: In Figure 2a,b, gate recess depth = 120 nm and the peak doping concentration is $1.05 \times 10^{20}$ cm$^{-3}$. In Figure 2c–e, gate depth = 80 nm, gate recess depth = 150 nm, peak doping concentration of BCAT = $1.45 \times 10^{20}$ cm$^{-3}$, short junction depth = 82–92 nm, long doping junction depth = 134–141 nm. In Figure 2b, the parameters of the insulator are $L_{in} = 6$ nm, silicon film thickness = 30 nm, end depth = 95 nm, and in Figure 2e, $L_{in} = 6$ nm, silicon film thickness = 60 nm, and end depth = 145 nm.

Figure 2. A cross-sectional view of $y = 0$ x–z in the doping distributions of five structures.

3. Results and Discussion

Figure 3 numerically compares the on/off current of five structures (Saddle RFinFET, Pi-RFinFET, asymmetry, long doping junction BCAT, and Pi-BCAT). We defined the gap between the equipotential lines as the potential drop width (PDW). Compared with the buried channel array transistor with an asymmetric doping structure (Figure 2c), the saddle RFinFET has a lower peak doping concentration than the other three buried channel array transistor structures, because the saddle RFinFET has a wider overlapped region between the gate and the drain than the BCAT structure. The data to note in Figure 3 is for the off current, and the off current of each device is $I_{off,saddle} = 7.7 \times 10^{-13}$ A, $I_{off,Pi-RFinFET} = 4.89 \times 10^{-13}$ A, $I_{off,Asymmetry\_BCAT} = 5.95 \times 10^{-14}$ A, $I_{off,Long\_doping\_junction} = 1.84 \times 10^{-13}$ A, and $I_{off,Pi-BCAT} = 2.54 \times 10^{-14}$ A. Figure 3 shows that the off current is higher than that of other BCAT structures, even though the peak doping concentration is lowered. Pi-RFinFET is a structure manufactured according to the reference, and an insulator is added to the doping region at the bottom of the storage node of the saddle RFinFET. As a result, the on current decreases because of the buried insulator, but the off current decreases by increasing the potential drop width of the overlapped region between the gate and the drain. In the case of a long doping junction structure, the doping region is relatively wider than that of the asymmetric doping structure. As a result, the channel length is short and the on current is high. However, the off current of the long doping junction structure increases relatively compared to the asymmetric doping structure, because the overlapped region between the gate and the drain increases. In Pi-BCAT, it partially offsets the on current reduction phenomenon that occurs in the buried insulator as it increases the on current, which is an advantage of the long doping junction structure. In addition, as the dielectric constant of the insulator (SiO$_2$: 3.9) is smaller than that
of silicon (Si: 11.8), the internal electric field of the insulator is small. In addition, by increasing the potential drop width in the silicon region around the insulator according to the boundary conditions of Gauss’s law, GIDL becomes lower. As a result, the on current decreases by 20% compared with the asymmetry doping structure, but the off current decreases by 58%.

Figure 3. Numerical comparison of on/off current in five structures.

Figure 4 shows a linear Log current graph of five structures (saddle RFinFET, Pi-RFinFET, asymmetry, long doping junction BCAT, and Pi-BCAT). The \( I_{\text{off}} \) values of each structure in the red circle corresponding to the gate voltage = −0.5 V are in the following order: Pi-BCAT < asymmetry < long doping junction BCAT < Pi-RFinFET < saddle RFinFET. The structures of saddle RFinFET and BCAT have different values of \( I_{\text{off}} \) because of the difference in the area of the gate, while asymmetry and long doping junction BCAT have different \( I_{\text{off}} \), owing to the difference in the overlapped region of the gate and drain. In the case of the Pi-RFinFET and Pi-BCAT structures, in which the insulators are buried, they have a smaller \( I_{\text{off}} \) than the general structures (saddle RFinFET and long doping junction BCAT) for the difference in permittivity and the boundary conditions of Gauss’s law between the insulator and silicon.

Figure 4. Linear (\( V_{\text{DS}} = 0.1 \) V) and Log (\( V_{\text{DS}} = 1.2 \) V) current graph of five structures.
Figure 5 shows a numerical comparison of the $g_{m,\text{max}}$ (maximum transconductance) and subthreshold slope (SS) of five structures (saddle RFInFET, Pi-RFinFET, asymmetry BCAT, long doping junction BCAT, and Pi-BCAT). In the case of $g_{m,\text{max}}$, compared with the asymmetric doping structure (asymmetry), the long doping junction structure has a wide doping region and a short channel length, therefore $g_{m,\text{max}}$ is high. In Pi-BCAT, compared with the asymmetric doping structure, because of the buried insulator, the doping area decreases and the resistance increases, so $g_{m,\text{max}}$ decreases. In the case of SS, the difference between N-type doping and P-type doping is largely designed for the long doping junction structure compared with the asymmetric doping structure. As a result, the depletion width increases, and the SS of the long doping junction structure is relatively large compared with the asymmetry structure. Compared with the long doping junction BCAT, Pi-BCAT has a smaller electric field. As a result, SS decreases because the depletion width becomes smaller.

![Figure 5. Maximum transconductance ($g_{m,\text{max}}$) and subthreshold slope (SS) comparison of five structures.](image.png)

Figure 6 is a numerical comparison of the $V_{th}$ and drain induced barrier lowering (DIBL) of the five structures (saddle RFInFET, Pi-RFinFET, asymmetry BCAT, long doping junction BCAT, and Pi-BCAT). In the case of $V_{th}$, as the long doping junction structure has a higher N-type doping concentration compared with the region than the asymmetric doping structure (asymmetry), the energy level of the N-type doping region is relatively low. As a result, $V_{th}$ is relatively low. In Pi-BCAT, the energy level of the insulator ($\text{SiO}_2$) is higher than that of silicon. Because of the relatively high energy level of the insulator ($\text{SiO}_2$), the energy level of silicon is raised by the boundary conditions of Gauss’s law, and $V_{th}$ is raised. In the case of DIBL, the gate channel length of the long doping junction BCAT is shorter than the gate channel length of the asymmetric doping structure, so the DIBL becomes larger. In the case of Pi-BCAT, the DIBL is small, as the insulator causes most of the high potential to be located in the doping region at the bottom of the storage nodes.
Figure 6. $V_{th}$ and drain induced barrier lowering (DIBL) comparison of five structures.

Figure 7 compares the $I_{on}$ and $I_{off}$ values of Pi-BCAT according to the length of $L_{in}$ in the Pi-BCAT. As $L_{in}$ decreases, both the on and off currents decrease, showing that the off-current’s decrease is relatively significantly compared with that of the on current. Comparing the on and the off currents of the asymmetric doping structure as a measure, the on current is 80% and off current is 42% at $L_{in} = 6$ nm for Pi-BCAT.

Figure 8 shows the electrostatic potential distribution according to the length of the $L_{in}$ in Pi-BCAT ($V_{GS} = -0.5$ V and $V_{DS} = 1.2$ V), with Figure 8a $L_{in} = 6$ nm and Figure 8b $L_{in} = 12$ nm. The red dotted circle area is the high potential area where band to band tunneling (BTBT) occurs. Dotted arrows indicate a potential drop width from 1.2 V to 0 V. As the length of $L_{in}$ increases, the potential in the BTBT region where the gate and drain overlap increases. In addition, as the buried insulator area
decreases, the silicon area increases. Therefore, the potential drop width near the gate oxide decreases. As a result, the BTBT region has a high potential and a strong electric field, so the off current increases.

![Electrostatic potential distribution](image)

**Figure 8.** Electrostatic potential distribution according to the $L_{in}$ of Pi-BCAT.

Figure 9 shows the electric field and BTBT in the cut line. The BTBT regions of $L_{in} = 6$ nm and 12 nm are marked with blue lines. At $L_{in} = 6$ nm and 12 nm, the value of the peak electric field is almost the same. When $L_{in} = 6$ nm, the BTBT region is 68 to 86 nm, and when $L_{in} = 12$ nm, the BTBT region is 72 nm to 94 nm. In the case of $L_{in} = 6$ nm in the BTBT region, the integral of the E-Field is $1.29 \times 10^{-2}$ V/µm, and in $L_{in} = 12$ nm, the integral of the total electric field is $1.51 \times 10^{-2}$ V/µm. When $L_{in}$ is long, the area of the insulator decreases and the area of the silicon increases, so the region of the BTBT widens and the electric field increases because the influence of the insulator decreases. This increases the off current.

![Electric field-Z and band-to-band generation](image)

**Figure 9.** Electric field-Z and band-to-band generation according to $L_{in} = 6$ nm and 12 nm of Pi-BCAT.
Figure 10 compares the on/off current values using the silicon film thickness of Pi-BCAT. Increasing the silicon film thickness means that the high doping area becomes larger, and the on current increases. Likewise, until the silicon film thickness is 60 nm, the off current does not show a big change, but when the silicon film thickness is more than 60 nm, it increases sharply. This is because when the silicon film thickness of the buried insulator increases, the potential drop width in the area where BTBT mainly occurs decreases, so GIDL increases. However, when the silicon film thickness exceeds the gate depth, the influence on the potential drop width of the area where BTBT mainly occurs decreases and reaches saturation.

![Figure 10](image-url)

**Figure 10.** Changes in $I_{on}$ and $I_{off}$ according to the silicon film of Pi-BCAT.

Figure 11 shows the potential distribution plot according to the silicon film thickness in Pi-BCAT ($V_{GS} = -0.5\,V$ and $V_{DS} = 1.2\,V$), with (a) silicon film thickness = 30 nm, (b) silicon film thickness = 60 nm, and (c) silicon film thickness = 90 nm. When the silicon film thickness is small, the Pi-BCAT has a long potential drop width because of the boundary conditions of Gauss’s law of the insulator. However, as the size of the silicon film thickness gets closer to the gate depth, the potential drop width becomes smaller, and when the silicon film thickness is 70 nm compared with a gate depth $= 80$ nm, the potential drop width becomes shorter than the existing Pi-BCAT. When the silicon film thickness becomes longer than 70 nm, the position of the insulator gradually deviates from the area where BTBT mainly occurs, and as a result, after decreasing, GIDL becomes constant.
Figure 11. Electrostatic potential distribution according to the silicon film thickness of Pi-BCAT.

Figure 12 shows the on/off current graph of Pi-BCAT according to the length of $L_{in}$ in Pi-BCAT with a gate depth of 70 nm. Similar to Figure 6, the on/off currents decrease as $L_{in}$ decreases, but compared to the on current, the off current decreases significantly. In particular, it corresponds to 80% of the on current of the asymmetry junction BCAT at $L_{in} = 5$ nm, because the doping concentration is relatively concentrated in the contact area compared with a gate depth = 80 nm.

Figure 13 plots the on/off current according to the silicon film thickness of Pi-BCAT when the gate depth is 70 nm. Similar to Figure 9, as the silicon film thickness increases, both the on/off currents increase, but compared with the on current, the off current increases significantly above the silicon film thickness = 50 nm. However, when the silicon film thickness exceeds the gate depth, the effect on the...
potential drop width in the area where BTBT mainly occurs is reduced, and the off current reaches a saturation value and then decreases.

Figure 13. Ion and Ioff change at a gate depth = 70 nm in Pi-BCAT according to the silicon film thickness.

Figure 14 shows the on/off current graph of Pi-BCAT according to the length of the \( L_{\text{in}} \) in Pi-BCAT with a gate depth = 90 nm. Similar to Figures 6 and 11, as \( L_{\text{in}} \) decreases, the on/off currents decrease, but the off current decreases significantly compared with the on current. In particular, it corresponds to 80% of the on current of the asymmetry doping structure at \( L_{\text{in}} = 6 \) nm, and the off current tends to decrease significantly.

Figure 15 shows the on/off current graph according to the silicon film thickness of Pi-BCAT at 90 nm of the gate depth. Similar to Figures 9 and 12, as the silicon film thickness increases, both the on/off currents increase. When the silicon film thickness exceeds 70 nm, the off current increases sharply. However, when the silicon film thickness exceeds the gate depth, the off current reaches the saturation value, and then decreases.

Figure 14. Change of Ion and Ioff according to Lin in Pi-BCAT at a gate depth = 90 nm.
Figure 15. $I_{on}$ and $I_{off}$ change according to the silicon film thickness in Pi-BCAT at a gate depth = 90 nm.

Figure 16 shows the optimal parameter at each gate depth of 70, 80, and 90 nm in the Pi-BCAT. According to the gate depth, the optimal value of $L_{in}$ gradually increases. This is because as the gate depth increases, the doping concentration near the gate decreases. As a result, the optimal $L_{in}$ increases. The BTBT generation region is determined according to the gate depth. Therefore, the longer the gate depth, the longer the optimal silicon film thickness.

Figure 16. Optimal parameters ($L_{in}$ and silicon film thickness) in Pi-BCAT at gate depths = 70 nm, 80 nm and 90 nm.
Table 1 shows the $L_{in}$ and silicon film thickness of Pi-BCAT according to 80% of the on current in asymmetry BCAT at gate depths = 70 nm, 80 nm, and 90 nm. In addition, the off current of Pi-BCAT compared with asymmetry BCAT according to each gate depth of 70 nm, 80 nm, and 90 nm are 38%, 33%, and 38%. This is a three times improvement in the off current performance of asymmetry BCAT.

| Gate Depth | Optimal Value | 70 nm | 80 nm | 90 nm |
|------------|---------------|-------|-------|-------|
| $L_{in}$   |               | 5 nm  | 5.5 nm| 5.75 nm|
| Silicon film thickness | | 50 nm | 60 nm | 70 nm |
| $I_{on,Pi-BCAT}$ | | $2.21 \times 10^{-6}$ A | $2.25 \times 10^{-6}$ A | $2.31 \times 10^{-6}$ A |
| $I_{off,Pi-BCAT}$ | | $5.44 \times 10^{-14}$ A | $1.98 \times 10^{-14}$ A | $7.50 \times 10^{-14}$ A |
| $I_{on,Pi-BCAT}/I_{on,Asymmetry BCAT}$ | | 80% | 80% | 80% |
| $I_{off,Pi-BCAT}/I_{off,Asymmetry BCAT}$ | | 38% | 33% | 38% |
| $S_{SS}$ | Asymmetry BCAT | 65.0 mV/dec | 65.4 mV/dec | 66.0 mV/dec |
| $S_{SS}$ | Pi-BCAT | 66.225 mV/dec | 66.475 mV/dec | 66.725 mV/dec |
| $g_{m,max}$ | Asymmetry BCAT | $7.22 \times 10^{-6}$ A/V | $7.40 \times 10^{-6}$ A/V | $7.64 \times 10^{-6}$ A/V |
| $g_{m,max}$ | Pi-BCAT | $5.74 \times 10^{-6}$ A/V | $6.00 \times 10^{-6}$ A/V | $6.16 \times 10^{-6}$ A/V |
| $DIBL$ | Asymmetry BCAT | 1.81 mV/V | 3.63 mV/V | 4.73 mV/V |
| $DIBL$ | Pi-BCAT | 0.45 mV/V | 0.95 mV/V | 1.45 mV/V |

4. Conclusions

This paper proposes a structure with a partial isolation area under the storage node of the buried channel array transistor. In the partial insulation buried channel array transistor, as the length of $L_{in}$ for the buried insulator decreases, the on current decreases, but the off current falls significantly. In addition, the optimum point of length of the silicon film thickness of the buried insulator is determined by the gate depth. Therefore, the degree of the buried insulator can be set through the on/off current trend data according to the $L_{in}$ and silicon film thickness provided in this paper. In particular, although the partial isolation type buried channel array transistor structure with an optimized buried insulator compared with the conventional structure with an asymmetry doping structure shows some loss of the on current, the off current has the relatively very low value of 40%, showing an improved performance in terms of reducing leakage current in memory devices.

**Author Contributions:** Formal analysis, J.-h.P.; Investigation, G.K.; Supervision, M.J.L.; Writing—original draft, J.-s.L.; Writing—review & editing, H.D.C. All authors have read and agreed to the published version of the manuscript.

**Funding:** This work was supported in part by the National Research Foundation of Korea (NRF) grant funded by the Korean government (MSIT; grant number 2018R1A2B600821613) and in part by Korea Institute for Advancement of Technology(KIAT) grant funded by the Korea Government(MOTIE) (I0011931, The Establishment Project of Industry-University Fusion District) and in part by Samsung Electronics (grant number 2019-0184).

**Conflicts of Interest:** The authors declare no conflict of interest.

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Electronics 2020, 9, 1908

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