Constant Depth Bucket Brigade Quantum RAM Circuits Without Introducing Ancillae

Alexandru Paler, Oumarou Oumarou, Robert Basmajian

University of Transilvania, B-dul Eroilor 29, 500036, Brașov, România

Johannes Kepler University, Altenberger Str. 69, 4040, Linz, Austria and

University of Passau, Instr. 43, 94032, Passau, Germany

Bucket brigade quantum RAM (QRAM) circuits were proposed for their advantageous addressing of the memory. Another quality of these circuits is that queries, once the addresses are determined, can be parallelised. State-of-the-art error-corrected formulation of these circuits, however, had to be decomposed into the Clifford+T gate set, and the initial parallelism was lost in the process. By using advantageous Toffoli gate decompositions, and without introducing any additional ancilla qubits, we construct bucket brigade QRAM circuits with a constant depth. This depth is reduced from \(O(2^n)\) to \(O(q)\) in the worst case when the QRAM is queried for any of its \(2^n\) memory cells being used. Incidentally, the presented construction has a T-count more than half smaller, compared to the existing Clifford+T formulations. The construction shows that, if quantum hardware would not be a scarce resource, exponential query speed ups are possible compared to state-of-the-art quantum read-only memory (QROM) designs.

I. INTRODUCTION

Quantum random access memory (QRAM) circuits were proposed for writing and reading information during quantum information processing. However, their practical utility is debatable due to the exponential costs associated to explicitly storing and retrieving information. Nevertheless, QRAM and their read-only-variant QROM [1] are still capturing the attention of researchers due to their conceptual similarity to classical RAMs, and due to the fact that they are subroutines of relevant quantum algorithms.

QRAMs are described in the form of quantum circuits. Information is stored on the wires/qubits, while quantum gates are used to compute the addresses (e.g. FANOUT and FANIN in Fig. [1]) and the effective read and write operations (e.g. QUERY in Fig. [1]). For a QRAM with \(2^n\) distinct memory cells (each storing a single bit), there are \(q\) bits necessary to address any of the cells. A QRAM circuit takes as input a superposition \(|\text{adr}_j\rangle\) addresses to be queried (\(a\) are complex amplitudes), and outputs the contents of the memory cell \(m_j\) addressed by \(|\text{adr}_j\rangle\).

\[
\sum_{j=0}^{2^n-1} \alpha_j |\text{adr}_j\rangle |0\rangle_{\text{QRAM}} \xrightarrow{\text{FANOUT}} \sum_{j=0}^{2^n-1} \alpha_j |\text{adr}_j\rangle |m_j\rangle
\]

The bucket brigade QRAM variant was proposed to reduce the number of quantum gates executed until a memory location is addressed and queried. In order to achieve this, the memory location indices are computed after executing a FANOUT tree: the leaves of the tree are control bits indicating if a specific memory cell should or not be queried.

A bucket brigade QRAM circuit consists of three sub-circuits (regions): 1) FANOUT where an exponential number of ancilla bits \(b_i\) is used to store control bits for referencing the corresponding memory cells \(m_i\); 2) QUERY where the memory bits \(m_i\) are queried and the results are stored on the ancilla wire \(|\text{target}\rangle\); 3) FANIN (the uncomputation of FANOUT) in order to maintain reversibility, where the \(b_i\) bits are returned to their initial \(|0\rangle\) state. The three sub-circuits can be easily recognised in Fig. [1]. The Toffoli gates targeting the lowest wire correspond to QUERY, the sub-circuit to the left of QUERY is FANOUT, and the sub-circuit to the right of QUERY is FANIN.

The state-of-the-art Clifford+T formulation of the bucket brigade quantum circuits [2] was obtained from the original formulation [3] and decomposing the Toffoli gates into known Clifford+T gate sequences. The authors of [2] mentioned that important resource savings could be possible if the CCZ/Toffoli transformation is

---

[1] Constant Depth Bucket Brigade Quantum RAM Circuits Without Introducing Ancillae

[2] A bucket brigade circuit consisting of CNOTs and Toffoli gates. The controlled gates from the diagram use @ for controls and the X for target wires. The address wires are named \(a\), the memory cells holding single bits are \(m\). The classical bits stored on the wires \(b\) determine which memory wires to read/write.

FIG. 1. A bucket brigade circuit consisting of CNOTs and Toffoli gates. The controlled gates from the diagram use @ for controls and the X for target wires. The address wires are named \(a\), the memory cells holding single bits are \(m\). The classical bits stored on the wires \(b\) determine which memory wires to read/write.

---

* [alexandrupaler@gmail.com]
employed in an advantageous manner for the compilation of QRAM. This work continues on that line of thought and illustrates some of the possible improvements. First, the depth is exponentially reduced by parallelising the Toffolis in the QRAM QUERY region. Second, the herein presented method achieves a linear width improvement compared to the state-of-the-art from [2], where parallelisation was obtained by introducing four ancillae for each Toffoli gate. Our method is ancillae free, and reduces the width by a factor of four. Third, the presented QRAMs have a T-count which is almost double to QROM [1], and approximately half compared to the QRAMs from [2] (c.f. $T_{bbs}$, $T_{rom}$, $T_{bpb}$ in the following section).

The Toffoli construction used in this paper can be interpreted as the enabler of trading depth for width between QROM and QRAM: it exponentially increases the width, while it exponentially decreases the depth. Fig. 2 illustrates the improvements obtained by parallelising the QRAM circuits.

In the following, the Results section presents exact resource counts for the proposed bucket brigade QRAMs, and includes a detailed comparison to other QRAM variants layouts. The Methods section discusses how quantum gate level parallelism is achieved, and illustrates how Clifford+T decompositions of Toffoli gates can be used in an advantageous manner for each QRAM sub-circuit. Finally, we present empirical evidence to conjecture that the presented optimisation technique could be applicable to many types of circuits based on multi-controlled-operations [4], such as various adders and multipliers.

In order to achieve a fair comparison between QRAM circuit implementations, we consider $2^n \leq 2^q$, $n \leq q$, being the number of memory queries, and $2^q$ the number of memory cells $m_i$, such that $0 < i < 2^q$. The worst case for the number of queries, as used in [2], is for $n=q$.

II. RESULTS

The advantage of bucket brigade QRAM queries is that these can be parallelised. The gate level parallelism used in this work is conceptually very similar to classical instruction level parallelism (see Section IIIA). In practice, however, the QRAM gate parallelism was lost when translating these circuits to Clifford+T – an often necessary step for estimating the computational resources required for quantum error-correction [5]. The width (number of wires, not considering the memory cells $m_i$), T-count, and the depth of the QRAM circuits [2] are:

$$Q_{bbs}=q+2^q+5$$
$$T_{bbs}=21 \cdot 2^q-28$$
$$D_{bbs}=21 \cdot 2^q+2q-26$$

The disadvantage of bucket brigade QRAMs is the fact that an exponentially high number of ancilla $b_i$ bits has to be computed in order to achieve parallelism. The exponential overhead is far from ideal, when considering that quantum hardware resources are and will remain very scarce. For this reason, the QROM was proposed in [1]. It does not require the $b_i$ bits, but queries are strictly sequentialised (one after the other). By using optimised Toffoli decompositions, the T-count of the QROM is linear in the number of queries $2^n$ (the authors of [1] used $L$ for the number of queries). The formulas for width ($Q_{rom}$) and depth ($D_{rom}$) do not refer to the memory cells $m_i$.

$$Q_{rom}=q+1$$
$$T_{rom}=4 \cdot 2^n-4$$
$$D_{rom}=10 \cdot 2^n+c \cdot O(2^n)$$

Using parallelisable CCZ/Toffoli decompositions, the bucket brigade construction presented in the following has a reduced T-count, and a depth exponentially shallower than the circuits from [2].

$$Q_{bpb}=q+2^q+1$$
$$T_{bpb}=T_{fanout}+T_{query}=(4 \cdot 2^q)+(6 \cdot 2^n)$$
$$D_{bpb}=D_{fanout}+D_{query}+D_{fanin}=10 \cdot 2^n+11+(4 \cdot q)$$

The equivalent quantum volume of the circuit being protected by the surface code is not evaluated in this work, although the parallelism is achieved by using a surface-code compliant parallel CNOT construction. This choice is motivated by the fact that having exponentially reduced the depth and the T-count, but by maintaining the exponentially large width (compared to QROM, $Q_{rom} \ll Q_{bpb}$) is still detrimental – the hardware footprint is prohibitively high. For future work, it will be reasonable to estimate the resources necessary for surface code protection, but when these QRAMs are included in practical quantum algorithms. As a note, QRAM query time is exponentially shorter after exponentially reducing the depth of circuits. The estimations in [2] mention 0.35 ms for querying a 4KB QRAM (15 bit addresses). The presented optimisation would reduce the query time by a factor of $2^{15}$ to approximately 11 ns.

III. METHODS

This work assumes that, in general, two gates $G_1$ and $G_2$ can be parallelised if their commutator $[G_1,G_2]=0$. From a functional perspective, it does not matter in which order the gates are applied: in an ideal setting, the gates can be executed without one depending on the output of the other. This approach to quantum gate parallelism is very similar to classical computing instruction-level parallelism. It should be also noted, that the available level of parallelism in a circuit does not guarantee the same level of execution speed-up. Quantum circuits need to be mapped to hardware, or be compiled to error-corrected structures, and the underlying architecture determines the achievable speed-up which can be less than the ideally observed quantum gate level parallelism.
A. Parallel CNOTs

For the purpose of this work, two CNOTs are parallel if they either share the controls, or no wires at all (see Fig. 6). CNOTs can also share the target, but this fact will not be used herein. Most of the Clifford+T decompositions are compiled and optimised due to the inherent necessity for quantum error-correction, and this kind of CNOT parallelism is supported by the surface code [6] (braided and lattice surgery variants), for example.

As mentioned previously, the surface code support does not imply that the full parallelism is always achievable. The layout of the circuit and the availability of hardware resource play a significant role. However, for the presented QRAM construction, the maximum parallelism is possible by ordering the wires in pairs, in an arrangement similar to the one presented in [3] (see Eq. 4). If the QRAM circuit would be executed un-error-corrected directly on a quantum chip, the connectivity of the chip determines the achievable speed-up.

\[ a_0, \ldots, a_q, \ldots, b_i, m_i, b_{i+1}, m_{i+1}, \ldots \text{target} \] (4)

B. Parallelisable CCZ

The three qubit Toffoli gate is in general derived from the CCZ gate, which is a controlled application of the two-qubit CZ gate. The CCZ flips the sign of phase of a state if there is a |1⟩ on all of the gate’s three input wires (qubit and wire are used interchangeably). Thus, the phase flip can be expressed as \((-1)^{xyz}\), where \(x,y,z\) are the bit values of the inputs: the phase is multiplied by \(-1\) if all three bits are 1, and no phase flip is applied otherwise \((-1)^0=1\). It has been shown by [4], and more recently in [7], that the following Boolean formula is useful for expressing the CCZ through CNOTs and T gates.

\[ 4xyz=x+y+z-(x\oplus y)-(y\oplus z)-(x\oplus z)+(x\oplus y\oplus z) \] (5)

The T gate rotates the phase of a state by \(\pi\), and \(-1=\omega^4=e^{\pi i}\), such that \((-1)^{xyz}=\omega^{4xyz}\). Thus, seven T gates are necessary, each conditioned on one of the parity sums from Eq. 5.

Eq. 5 is a recipe for generating valid CCZ gate decompositions. Seven parity sums are computed by using CNOTs and T gates, while ensuring that two conditions are met. The first condition is for the T gates to be applied at the right moment, when the necessary bit parities are stored on any of the wires. Second, the parities on each of the three wires have to be uncomputed in order to reflect a correct functionality. Ancillae used for parity computations have to be uncomputed, too. Due to the form of Eq. 5 containing seven parities, the number of ancillae seems to be bounded by seven, but in practice the maximum is four, because three of the parities are formed by single bits values. Consequently, the literature includes a large number of decompositions of the CCZ in terms of Clifford+T gates. Some decompositions were used to obtain T-depth one, while others because they did not require ancillae.

In the following we use a CCZ decomposition that maintains the Toffoli gate parallelism when decomposed into Clifford+T. The decomposition is obtained after making the observation that two Toffoli gates are parallel whenever they are arranged like in Fig. 7. There are two non-trivial situations: a) one wire is shared; b) two
Effectively, a Toffoli gate can be obtained by surrounding the wires to the wires share a single wire. It can be noticed that the wire in Fig. III B can be used whenever two CCZ/Toffoli gates are parallelisable decomposition of CCZ. The decomposition of Toffoli gates, there has to exist a Clifford+T control is shared. In this figure two wires are shared. The two either be applied to; left) the same qubits acting as controls, or right) the target qubit and a shared control. Note: In the left diagram, the second Toffoli is not necessary and can be replaced with two CNOT gates, one before and another one after the first Toffoli gate.

Another practical observation is that, whenever two Toffoli gates are parallel, these can be formulated as CCZ gates which share one or two controls out of the three.

In order to implement parallel Clifford+T decompositions of Toffoli gates, there has to exist a Clifford+T parallelisable decomposition of CCZ. The decomposition in Fig. III B can be used whenever two CCZ/Toffoli gates share a single wire. It can be noticed that the wire $|q1\rangle$ acts only as a control for the CNOTs, which are applied to the wires $|q0\rangle$ and $|q2\rangle$, and the T gate commutes with the control of the CNOTs.

The wire ordering in Fig. III B does not play any role, because the output will still reflect the $(-1)^{|q3\rangle}$ phase flip. Effectively, a Toffoli gate can be obtained by surrounding the CCZ with two Hadamards on any of the wires. Advantageous configurations are whenever the Hadamards are placed such that the wire corresponding to $|q1\rangle$ is shared. The presented technique is similar to template based quantum circuit optimisation [8], in the sense that the most advantageous Toffoli rewrite rule is chosen from the three possible decompositions based on the expected gate parallelism. During the writing of the manuscript, we found out that the decomposition from has been also presented in [9], but its effect on the parallelisation of Toffoli/CCZ gates has not been described in the subsequent literature.

C. FANOUT: Shared Control

Whenever two Toffoli gates share a control, the CCZ gate is decomposed such that the shared wire is the one that enables parallelism (i.e. $|q1\rangle$ in Fig. III B). This scenario appears in the FANOUT region of the QRAM.

D. QUERY: Shared Target

The QUERY is formed by a sequence of Toffoli gates conditioned by distinct pairs of $(|b_i,m_i\rangle)$ wires. The only wire shared is the target. Therefore, the decomposition from Fig. III B can be used, but by making $|q1\rangle$ correspond to the target. For two consecutive Toffolis the H gates on the target wire will cancel, as illustrated in Fig. 10. T-count optimisation is a side-effect of this kind of parallelism because along the shared target wire the T gates can pairwise be transformed into S gates.
circuit (see following section).

the computed AND bit is not necessary anymore in the is left with a phase shift, which has to be reversed, once

in some circumstances (see Section III G).

Simplification is not illustrated. Furthermore, half of the column of T gates at the beginning of the circuit could be eliminated

FIG. 11. Two Toffoli gates sharing a target wire. Two of the T gates on the target wire can be reduced to an S gate. Simplification is not illustrated. Furthermore, half of the column of T gates at the beginning of the circuit could be eliminated in some circumstances (see Section III G).

E. FANOUT: Compute Logical AND

Approximate gates have been discussed since [4], but their relevance for quantum circuit design was recognised once T-count optimisation became urgent. This is the case for the approximate CCZ/Toffoli which uses four T gates like in Fig. 12. The approximate Toffoli is also called a logical AND, when the target is an ancilla initialised to \( |0 \rangle \). However, after a logical AND the state is left with a phase shift, which has to be reversed, once the computed AND bit is not necessary anymore in the circuit (see following section).

![Diagram of a logical AND gate.](image)

FIG. 12. The parallelisable logical AND has two wires acting always as control. This circuit is similar to the one from [1]. The target wire cannot be shared for parallelisation. If the qubit \(|a2\rangle\) is initialised into \(|0\rangle\), at the end of this computation will be in the state \((-1)^{a_0a_1}|a_0a_1\rangle\) which represents up to a phase shift the correct value of the Boolean AND operation between \(a_0\) and \(a_1\).

Due to their lower T-count it is preferable, whenever possible, to use logical AND gates instead of more general CCZ/Toffoli gates. Two logical ANDs sharing a control can be decomposed like in Fig. 13.

F. FANIN: Uncompute Logical AND

The inverse of the logical AND is its uncomputation. Because the \(b_i\) qubits are ancillary, their usage is not necessary after the queries have been executed. Thus, these can be measured and a correctional CZ gate can be applied conditionally on the measurement result.

G. The parallel bucket brigade QRAM

The parallelised QRAM circuit is obtained by concatenating the parallelised circuits for FANOUT, QUERY and FANIN (e.g. Fig. 5). One of the surprising results is that the depth of the FANOUT is constant with respect to \(q\) (cf. Eq. 3): the depth is reduced from \(O(Q\log Q)\) to \(O(\log Q)\). This indicates that there is a significant speedup in computing \(Q\) sums of the form \(b_i = \sum_{i=0}^{q-1} (a_i \cdot 2^i)\) where \(a_i\) are the bits of the address state vectors used as input to the QRAM (even in superposition).

Another interesting observation is that the T-count \(T_{lat}\) can be reduced with additional \(2^n\) T gates if, after applying the QUERY, the memory is not entangled to the rest of the computation. In that case, the T gates on the \(m_i\) wires will affect only the global phase of the \(m_i\) states. This can be seen if the decomposition from Fig. 11 is used in reversed gate order, such that, for example, in Fig. 11 half of the T gates applied to \(c_i\) in the leftmost column appear at the end of the circuit.
through measurements. However, the major disadvantage of logical ANDs is their sequential nature, and being uncomputed simulations. Thus, by using parallel Toffoli gate decompositions one could obtain a T-count comparable to logical AND formulations. However, the major disadvantage of logical ANDs is their sequential nature, and being uncomputed through measurements.

FIG. 13. Two Toffoli gates sharing a control wire. Parallelisation with logical AND versions of the Toffoli gate.

Thus, by using parallel Toffoli gate decompositions one could obtain a T-count comparable to logical AND formulations. However, the major disadvantage of logical ANDs is their sequential nature, and being uncomputed through measurements.

FIG. 14. Logical AND uncompute. HM represents the measurement in the X basis (a Hadamard gate followed by a measurement in the computational basis). Depending on the measurement result a CZ gate correction is applied (here shown always and not conditioned on measurement result). The CZ gate is decomposed with the target being on the wire that is not shared. All measurements can be parallelised and the correction can be applied depending on the individual measurement results. In this figure, a parallel CNOT is applied for the case when both corrections would be required.

FIG. 15. Parallelising operations by introducing Toffolis (0) represents a negative control) reduces computational depth, but, in the worst case where no other optimisations are available, it increases T-count. These circuit identities are inverse to the ones from [11].

The literature on quantum (reversible) circuit optimisation using templates is very rich, and includes a multitude of heuristics and methods of how to reduce T-counts, T-depths, Toffoli gate counts, Hadamard gate counts etc. A general approach may use the circuit identities below. It may seem counter intuitive, that it is more advantageous to include T gates while not introducing ancilla: in Fig. 15 a single Toffoli is transformed into two Toffoli gates, thus the number of T gates increases from 7 to 14. However, the introduced T gates may cancel, due to efficient Toffoli gate parallelism in the overall circuit.

IV. CONCLUSION

The depth of the bucket brigade QRAM circuits, when formulated with Clifford+T gates, is independent of the number of queries. This capability is achieved without introducing ancillae.

It is certain that quantum hardware is a very scarce resource, and methods that trade T-count for ancillae do not take into consideration that, whenever fault-tolerance has to be achieved, ancillae have to be error-corrected, too. Hardware resources have to be provisioned for the ancillae, and, although it may seem surprising, the cost of fault-tolerance is not associated with T state distillations but with Clifford operations (and this includes ancillae no being used for long times, i.e. carry ripple adders)

The intensity of heuristics and methods of how to reduce T-counts etc. A general approach may use the circuit identities below. It may seem counter intuitive, that it is more advantageous to include T gates while not introducing ancilla: in Fig. 15 a single Toffoli is transformed into two Toffoli gates, thus the number of T gates increases from 7 to 14. However, the introduced T gates may cancel, due to efficient Toffoli gate parallelism in the overall circuit.

FIG. 15. Parallelising operations by introducing Toffolis (0) represents a negative control) reduces computational depth, but, in the worst case where no other optimisations are available, it increases T-count. These circuit identities are inverse to the ones from [11].

Future work will parallelise quantum circuits using templates like the one presented in [15] without introducing ancillae, and analyse the obtained sequentialised layouts for the purpose of quantum resource estimation.

ACKNOWLEDGMENTS

A.P. was supported by a Google Faculty Research Award, and the NUQAT project funded by the University Transilvania Brasov. We thank Olivia Di Matteo for her very valuable feedback during the preparation of the circuits and the writing of the manuscript.

[1] R. Babbush, C. Gidney, D. W. Berry, N. Wiebe, J. McClean, A. Paler, A. Fowler, and H. Neven, Encoding electronic spectra in quantum circuits with linear t complexity, Physical Review X 8, 041015 (2018).
[2] O. Di Matteo, V. Gheorghiu, and M. Mosca, Fault tolerant resource estimation of quantum random-access memories, arXiv preprint arXiv:1902.01329 (2019).
[3] S. Arunachalam, V. Gheorghiu, T. Jochym-O’Connor,
M. Mosca, and P. V. Srinivasan, On the robustness of bucket brigade quantum ram, New Journal of Physics 17, 123010 (2015).

[4] A. Barenco, C. H. Bennett, R. Cleve, D. P. DiVincenzo, N. Margolus, P. Shor, T. Sleator, J. A. Smolin, and H. Weinfurter, Elementary gates for quantum computation, Physical review A 52, 3457 (1995).

[5] A. Paler, D. Herr, and S. J. Devitt, Really small shoe boxes: On realistic quantum resource estimation, Computer 52, 27 (2019).

[6] A. Paler, A. G. Fowler, and R. Wille, Synthesis of arbitrary quantum circuits to topological assembly: Systematic, online and compact, Scientific reports 7, 1 (2017).

[7] C. Gidney, Halving the cost of quantum addition, Quantum 2, 74 (2018).

[8] D. Maslov, C. Young, D. M. Miller, and G. W. Dueck, Quantum circuit simplification using templates, in Design, Automation and Test in Europe (IEEE, 2005) pp. 1208–1213.

[9] M. Amy, D. Maslov, and M. Mosca, Polynomial-time t-depth optimization of clifford+ t circuits via matroid partitioning, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 33, 1476 (2014).

[10] A. Paler and R. Basmadjian, Clifford gate optimization and t gate scheduling: Using queueing models for topological assemblies, arXiv preprint arXiv:1906.06400 (2019).

[11] M. Z. Rahman and J. E. Rice, Templates for positive and negative control toffoli networks, in International Conference on Reversible Computation (Springer, 2014) pp. 125–136.