We introduce a deep-recessed gate architecture in $\beta$-Ga$_2$O$_3$ delta-doped field-effect transistors (FETs) for improvement in dispersion and breakdown properties. The device design incorporates an unintentionally doped (UID) $\beta$-Ga$_2$O$_3$ layer as the passivation dielectric. To fabricate the device, the deep-recess geometry was developed using BCl$_3$ plasma-based etching at $\sim$5 W reactive ion etching (RIE) power to ensure minimal plasma damage. Etch damage incurred with plasma etching was mitigated by annealing in vacuum at temperatures above 600 °C. A gate-connected field-plate edge termination was implemented for efficient field management. Negligible surface dispersion with lower knee walkout at high V$_{DS}$, and better breakdown characteristics compared to their unpassivated counterparts were achieved. A three-terminal OFF-state breakdown voltage of 315 V, corresponding to an average velocity (1–2 × 10$^7$ cm/s) [9] which when combined with high saturation current density, and unity current gain cut-off frequency (RF) electronics [3], [4]. This is primarily driven by the availability of superior quality, large-area monocrystalline $\beta$-Ga$_2$O$_3$ bulk substrates with different orientations from low-cost melt-based methods [5]–[7], a feature distinctive to $\beta$-Ga$_2$O$_3$ technology since the structure simultaneously provides control of surface-related dispersion and excellent field management.

Index Terms—$\beta$-Ga$_2$O$_3$, DC-RF dispersion, R$_{ON}$ degradation, deep-recess, delta-doping, epitaxial passivation, field management, field-plate.

I. INTRODUCTION

Currently, there is extensive interest for exploring $\beta$-Ga$_2$O$_3$ (band gap $\sim$ 4.6 eV) based devices for next-generation high-power switching [1], [2] and radio frequency (RF) electronics [3], [4]. This is primarily driven by the availability of superior quality, large-area monocrystalline $\beta$-Ga$_2$O$_3$ bulk substrates with different orientations from low-cost melt-based methods [5]–[7], a feature distinctive to $\beta$-Ga$_2$O$_3$ among all the wide bandgap materials [8]. Besides, the ultra-wide bandgap enables a high breakdown field ($\sim$8 MV/cm) [9] which when combined with high saturation velocity (1–2 × 10$^7$ cm/s) [10], [11] and electron mobility (250–350 cm$^2$/V·s) [12] quantifies to one of the best figure of merits for power switching [13], [14] and amplification [15] amidst contemporary wide bandgap materials. This widespread interest in $\beta$-Ga$_2$O$_3$ has prompted research groups to develop lateral and vertical transport devices in the form of Schottky barrier diodes [16]–[21] and field-effect transistors (FETs) [22]–[32] with excellent performance indices.

Of the various lateral $\beta$-Ga$_2$O$_3$ based FETs demonstrated in literature, delta-doped FETs [4], [24], [33] were shown to manifest high sheet charge density at improved mobility, high ON-current density, and unity current gain cut-off frequency besides appreciable breakdown characteristics at low ON-resistance ($R_{ON}$). The efficacy of these lateral FETs is however limited by the peak electric field at the drain-side edge of the gate, as in all lateral wide bandgap transistor topologies [34]. The exposed semiconductor surface in the gate–drain access region is susceptible to this high field that lead to charge trapping in surface states, thereby resulting in DC-RF dispersion and dynamic $R_{ON}$ degradation [35], [36]. Although the presence of buffer traps also contribute to
the process, charge trapping in surface states is argued to be the primary source of this degradation [35], [38]. For the rest of the article, we refer to this degradation as dispersion.

To realize delta-doped FETs with excellent performance, dispersion incurred by the presence of deep-level states in the buffer from semi-insulating Fe-doped substrate was reduced by using thick buffer layers [33]. To mitigate the surface-related dispersion for these FETs, passivation of the semiconductor surface is essential. Although silicon dioxide (SiO$_2$) [26], [27], [37] and silicon nitride (SiN$_x$) [32] have been investigated as passivation dielectrics on $\beta$-Ga$_2$O$_3$ FETs, the semiconductor–dielectric interface is far from ideal as the dielectrics were deposited ex situ. On the other hand, epitaxial passivation [39], wherein the dielectric is grown in situ with the device epitaxial stack to function as the passivation layer could outperform the ex situ deposited dielectrics due to their improved interfacial properties. The phenomenon is further enhanced for a delta-doped FET with unintentionally doped (UID) $\beta$-Ga$_2$O$_3$ being used as the device cap as well as the epitaxial passivation layer since the design ensures the absence of a semiconductor–dielectric interface near regions of the device that experience the highest electric fields. Furthermore, the high dielectric permittivity of the $\beta$-Ga$_2$O$_3$ passivation layer can enable superior breakdown characteristics when combined with optimal field-plate designs for field management. Indeed, epitaxial passivation previously investigated on gallium nitride high electron mobility transistors (GaN HEMTs) using UID GaN as the passivation dielectric displayed excellent dispersion and breakdown properties [40], [41].

This article focuses on the development of epitaxial passivation for $\beta$-Ga$_2$O$_3$ delta-doped FETs. Such a novel architecture would require etching of UID $\beta$-Ga$_2$O$_3$ underneath the gate to form a deep-recess pattern that differentiates the passivation layer from the cap layer. The deep-recess was patterned using BCl$_3$ plasma-based dry etching. Damage incurred by BCl$_3$ plasma during deep-recess was found to degrade two-terminal source–drain current characteristics. Hence, we investigated techniques to restore current density after deep-recess. With optimal plasma etch conditions alongside a damage recovery anneal step, the source–drain current was restored and field-plated $\beta$-Ga$_2$O$_3$ delta-doped FETs with epitaxial passivation that exhibited negligible dispersion and enhanced breakdown characteristics were developed.

II. DEVICE GROWTH AND FABRICATION DETAILS

The epitaxial stack for the delta-doped FET was grown in an oxygen plasma-assisted molecular beam epitaxy (PAMBE) chamber on (010) oriented Fe-doped $\beta$-Ga$_2$O$_3$ semi-insulating substrates commercially available from Tamura Corporation [57]. The growth was realized in a gallium-deficient regime with a growth rate $\sim$3 nm/min. An O$_2$ plasma power of 300 W, chamber pressure of $\sim$1.5 $\times$ 10$^{-3}$ Torr, gallium beam equivalent pressure (BEP) of $\sim$8 $\times$ 10$^{-8}$ Torr, and substrate temperature of 700 °C were maintained during the growth. Before initiating the growth, the substrate was heated to 800 °C and a surface cleaning process using O$_2$ plasma was carried out for 10 min. The delta-doping profile was realized with Si as the dopant. To delta dope UID $\beta$-Ga$_2$O$_3$, the Si cell shutter was opened for 3 sec with cell temperature maintained at 900 °C without growth interruption. This specific combination of the shutter time and cell temperature was chosen to target charge density $\sim$10$^{13}$ cm$^{-2}$. Prior to setting the Si cell to the desired temperature, the cell was heated at 1150 °C for 15 min to remove the residual oxide that forms on top of the Si target in the cell.

The epitaxial structure (starting from the substrate) comprises a 450 nm UID $\beta$-Ga$_2$O$_3$ buffer, an Si delta-doped sheet, and 160 nm of UID $\beta$-Ga$_2$O$_3$ to function as the cap (40 nm) plus the passivation layer (120 nm). A 2-D schematic of the device epitaxial stack that also portrays the final deep-recessed design is shown in Fig. 1(a). The as-grown surface displayed a smooth morphology as measured using atomic force microscopy (AFM) with an rms roughness of 1.5 nm [Fig. 1(b)]. To fabricate the device, source–drain ohmic contacts were first formed using a patterned regrowth process flow. In this process, a 500 nm thick sacrificial SiO$_2$ layer was deposited on the as-grown sample in a plasma-enhanced chemical vapor deposition (PECVD) chamber at 250 °C. Source and drain regions were then lithographically defined on the SiO$_2$ layer. 470 nm of SiO$_2$ underneath the defined region was etched using CF$_3$/O$_2$/Ar plasma-based dry etch in a PlasmaTherm SLR 770 inductively coupled plasma-reactive ion etching (ICP-RIE) system at 120 W RIE, 120 W ICP, and a chamber pressure of 5 mTorr. The remaining 30 nm SiO$_2$ was conformally etched in a diluted buffer oxide etch (BOE) to expose the $\beta$-Ga$_2$O$_3$ surface. Using SiO$_2$ as the hard mask, $\sim$190 nm $\beta$-Ga$_2$O$_3$ underneath the pattern was etched to reach the delta-doping profile using BCl$_3$ plasma in ICP-RIE (20 sccm BCl$_3$, 30 W RIE, 200 W ICP, and 5 mTorr chamber pressure). Degenerately doped $\beta$-Ga$_2$O$_3$ with layer thickness $\sim$50 nm and a targeted doping density of $\sim$10$^{20}$ cm$^{-3}$ was then regrown in these recessed regions using PAMBE. After growth, $\beta$-Ga$_2$O$_3$ that rests on top of the sacrificial oxide was lifted off by etching SiO$_2$ in BOE. Following lift-off, n$^+$-Ga$_2$O$_3$ would exist only on the patterned source–drain contact regions. A Ti/Au (30/130 nm) metal stack was then evaporated on the regrown contact regions, followed by N$_2$ anneal at 470 °C for 1 min to form the ohmic metal contact. Mesa isolation was performed using BCl$_3$ plasma. To form the deep-recess pattern, UID $\beta$-Ga$_2$O$_3$ underneath the gate was etched using BCl$_3$ plasma to segregate the passivation layer.
from the cap layer. The process incurred substantial plasma damage causing degradation of the two-terminal source–drain current. This etch induced damage was subsequently recovered by using a damage recovery anneal step which is discussed in detail in Section III. Thereafter, formations of gate and field-plate terminals constituted the final fabrication step. The inherent nature of the deep-recess pattern allowed for a controlled misalignment of the gate mask (toward the drain) on top of the recessed area to simultaneously define the Schottky gate and the field-plate contact in the same lithography process. With a gate mask misalignment of 0.4 μm that corresponds to the field-plate length (L_{FP}), e-beam deposited Ni/Au (30/100 nm) was used to form the gate plus the field-plate metal contact.

### III. Etch Damage Control

To define the channel/gate region of the device, 120 nm of UID β-Ga$_2$O$_3$ was etched using BC$_3$ plasma in an ICP-RIE chamber. A chamber pressure of 5 mTorr, 20 sccm BC$_3$, 30 W RIE, and 200 W ICP (etch rate = 32 nm/min) were initially adopted as the etching parameters. A drastic reduction in the two-terminal source–drain current density (from ~0.3 A/mm to ~10 μA/mm) was observed after the recess. The degradation was attributed to damage incurred by BC$_3$ plasma during the etch, also reported for (201) β-Ga$_2$O$_3$ [42] and other semiconductor technologies [43]–[45]. To reduce the damage due to BC$_3$ plasma, a minimal plasma intensity of ~5 W RIE (40 V dc bias) with no ICP power was used at a chamber pressure of 5 mTorr, and BC$_3$ flow of 20 sccm. The recipe resulted in an etch rate of ~2.7 nm/min, with a recessed sidewall angle of ~50° with respect to the device surface, extracted using AFM measurements. The etched regions exhibited similar surface morphology and roughness as that of the as-grown β-Ga$_2$O$_3$ surface in Fig. 1(b). The deep-recessed structures described below in this work used the ~5 W RIE condition. Although low plasma damage was anticipated for the recipe, current degradation was still observed after the recess. Further, investigation revealed that the degradation was independent of plasma power, chamber pressure, and BC$_3$ flow rate.

For (201) β-Ga$_2$O$_3$ Schottky barrier diodes, Yang et al. [42] had observed that annealing at 400 °C–450 °C for 10 min in an Ar ambient was effective toward passivating the damage incurred by the BC$_3$/Ar plasma. Therefore, to revive the source–drain current after recess, the etched devices were annealed at 400 °C for 10 min in N$_2$ ambient in a rapid thermal anneal (RTA) chamber. However, only 20%–30% of the initial current density could be recovered after anneal. Increasing the annealing temperature (T_{anneal}) to 450 °C showed a negligible increase in drain current compared to 400 °C. Further increase in T_{anneal} to 500 °C was seen to degrade the Ti/Au ohmic contact. Similar results were also observed for annealing in Ar ambient in the RTA chamber. Since annealing at atmospheric pressure in N$_2$ or Ar ambient did not enable recovery of current density, we attempted vacuum annealing in an ultrahigh vacuum anneal chamber (not RTA) at a pressure of ~3.5 × 10$^{-7}$ Torr for a longer duration (60 min).

A typical two-terminal source–drain current profile for a 1.8 μm source–drain separation for the sample as-grown, after recess, and after annealing is shown in Fig. 2(a). Annealing in vacuum was seen to enable higher T_{anneal} without degradation of the ohmic contact. More than 90% of the initial current density could be recovered at 600 °C. Beyond 600 °C, a negligible increase in the current density was observed, i.e., the revived current was seen to nearly saturate after T_{anneal} > 600 °C. The current recovery for both vacuum and N$_2$ anneal is plotted for a typical source–drain voltage (V_{DS}) of 10 V in Fig. 2(b). The vacuum anneal was also experimented on the recess etches carried out with high RIE (30 W) and ICP (200 W) powers. However, only 50% of the total current density could be recovered. This implies that the current recovery index is a function of the plasma power, the anneal temperature, and pressure. Further, optimization is required for complete recovery of the depleted current. Alternatively, dry etching using different plasma recipes (Cl$_2$, SF$_6$, CHF$_3$ etc.) [59], as well as wet etching [60] could be explored to ensure no degradation in device characteristics after recess.

Hall measurements were carried out at room temperature before the deep-recess to estimate the sheet charge density. A Hall mobility of 73 cm$^2$/Vs at a sheet charge density of 1.2 × 10$^{13}$ cm$^{-2}$ was measured. Degradation in source–drain current after the recess (before anneal) was observed to be in agreement with reduction in the Hall sheet charge density from 1.2 × 10$^{13}$ to ~10$^{10}$ cm$^{-2}$. To qualitatively understand this phenomenon of charge degradation with recess, photoluminescence (PL) measurements were carried out with an excitation laser wavelength of 232 nm on large-area samples (5 × 5 mm$^2$). The PL spectra of a bare Fe-doped β-Ga$_2$O$_3$ substrate, the as-grown delta-doped epitaxial stack, the stack after recess, and after anneal are plotted in Fig. 3(a). As seen from the figure, intensity of PL transitions that exist for the as-grown sample diminishes after deep-recess. The spectrum however is seen to reappear for the “after anneal” sample. To zero down to the wavelengths involved, the individual spectrum for the “as-grown” and the “after anneal” samples is plotted in Fig. 3(b) and (c) with Gaussian distribution to fit the experimental data. The Gaussian fits for the “as-grown” spectrum de-convoluted the emission band into three dominant peaks at 370 nm (3.36 eV), 410 nm (3 eV), and 480 nm (2.6 eV). These transition peaks are attributed to radiative
recombination of electrons from the conduction band edge with holes in the acceptor bands (gallium vacancies) that give rise to UV-blue emissions as reported in the literature [46]. These peaks were extensive for the as-grown sample but diminished for the deep-recessed sample. The depletion in free electrons in turn results in a decrease in PL transitions thereby decreasing the PL intensity. The theory is further supported by a decrease in the Hall sheet charge density after recess.

The annealed sample showed almost identical peak positions and intensity in the PL spectrum, suggesting that annealing at high temperatures was effective toward mitigating the deep level states and electron trapping in the epitaxial layers caused by BCl3 plasma. The Hall sheet charge density also recovered to $\sim 9.3 \times 10^{12} \text{ cm}^{-2}$ after annealing ($T_{\text{anneal}} > 600{ }^\circ\text{C}$). Although a detailed investigation is required to quantitatively confirm the hypothesis, similar observations for plasma damage during etch and recovery after anneal for other semiconductor technologies do exist in the literature [45].

IV. RESULTS AND DISCUSSION

With formation of gate and field-plate terminals after the recovery of source–drain current, the electrical characteristics of the device were measured using a Keysight 1500A semiconductor device parameter analyzer. The three-terminal transfer characteristics of the device ($I_{DS}-V_{GS}$) with $L_{SD}$ (separation between source–drain regrowth edges) = 5.4 $\mu$m, $L_G$ (gate length) = 0.65 $\mu$m, and $L_{GD}$ (gate to drain regrowth edge separation) = 2.7 $\mu$m for a device width ($W_D$) of 75 $\mu$m is shown in Fig. 4(a). For this device, the length of the gate recess is 1.8 $\mu$m, the gap size between the gate and recess sidewall is 1.15 $\mu$m, and spacing between source regrowth and recess sidewall is 0.85 $\mu$m. The dimensions were confirmed from scanning electron microscope (SEM) images. A high $I_{ON}/I_{OFF}$ ratio of $10^7$, pinchoff voltage of $-10$ V, and a low off-state leakage current of $3 \times 10^{-8}$ A/mm were measured for the device. The output curves ($I_{DS}-V_{DS}$) of the device are shown in Fig. 4(b). A saturated drain current density of 180 mA/mm was measured $V_{GS} = 2$ V and $V_{DS} = 15$ V. This current density was found to increase with decrease in $L_{SD}$.

To investigate for dispersion, pulsed $I–V$ measurements were carried out in a Keithley 4200-SCS parameter analyzer with an on-state pulswidth of 5 $\mu$s and 0.1% duty cycle. The off-state quiescent bias point was set at $V_{GSQ} = -15$ V (below pinch-off) and $V_{DSQ} = 15$ V (at saturation), where $Q$ in the subscript differentiates a pulsed voltage from a dc voltage. Negligible dispersion was observed for the devices biased at pulsed $I–V$ conditions as shown in Fig. 5(a). As expected, the pulsed $I–V$ drain current at saturation ($I_{DSQ,sat}$) was higher than the corresponding dc values due to the absence of self-heating. The dispersion characteristics were better compared to the unpassivated delta-doped FETs reported in [33]. This is primarily due to the fact that the exposed/unpassivated surface in the gate–drain access region for the deep-recessed FET, i.e., the top facet of the passivation layer, is far-off from the delta-doped channel. The surface states in this facet are not

![Image](49x204)

**Fig. 3.** (a) Room temperature PL spectra of an Fe-doped (010) $\beta$-Ga2O3 template, the as-grown epitaxial stack, the stack after deep-recess, and after annealing. Gaussian peak fits of PL spectra are shown for (b) as-grown sample and (c) sample after annealing. Three dominant transitions at $\sim 370$, $\sim 410$, and $\sim 480$ nm are seen. These transitions are suppressed in the PL spectra of the recessed sample as seen in (a) while they reoccur after anneal.

![Image](49x192)

**Fig. 4.** (a) $I_{DS}-V_{GS}$ and (b) $I_{DS}-V_{DS}$ characteristics of the deep-recessed FET. The device exhibits a pinchoff voltage of $-10$ V, an $I_{ON}/I_{OFF}$ ratio of $10^7$, and a maximum $I_{ON}$ of $\sim 180$ mA/mm.

![Image](49x80)

**Fig. 5.** (a) DC and pulsed $I_{DS}-V_{DS}$ curves at off-state bias ($V_{GSQ}$, $V_{DSQ}$) = (−15, 15 V). (b) Normalized change in $R_{ON}$ versus off-state $V_{DSQ}$ compared to an unpassivated delta-doped FET.
prone to high electric fields from the gate edge. The large separation as such is effective toward suppressing the trapping effects on the delta-doped channel from the surface states. The phenomenon is further enhanced by the absence of a definite $\beta$-$\text{Ga}_2\text{O}_3$/dielectric interface on the gate–drain plane that is exposed to high fields, which is precisely the situation for the surface states of the unpassivated delta-doped FETs.

To estimate the degree of knee walkout/ON-resistance ($R_{ON}$) degradation, difference in $R_{ON}$ ($\Delta R_{ON}$) for different ($V_{GSS}$, $V_{DSQ}$) off-state bias points normalized to $R_{ON, (0,0)}$ [$R_{ON}$ extracted for ($V_{GSS}$, $V_{DSQ}$) = (0, 0)] for the deep-recessed epitaxially passivated FET is compared to an unpassivated delta-doped FET in Fig. 5(b). $R_{ON}$ was extracted from the linear region of the $I_{DS}$-$V_{DS}$ curve with $V_{GS}$ at 0 V while $\Delta R_{ON}$ was calculated using the equation

$$\Delta R_{ON} = R_{ON} - R_{ON, (0,0)}. \tag{1}$$

The pulsed voltage compliance of the measuring instrument limited the extraction of $R_{ON}$ for the deep-recessed FET to $V_{DSQ}$ = 40 V. For the unpassivated FET, the measurement was done till $V_{DSQ}$ = 25 V, since the device presented appreciable gate leakage beyond 25 V. Compared to the steep increase in $\Delta R_{ON}$ for the unpassivated sample, the percentage change in $R_{ON}$ is lesser for the deep-recessed sample, i.e., the devices are more robust toward $R_{ON}$ degradation. The increase in $R_{ON}$ at high $V_{DSQ}$ for the deep-recessed FET is possibly due to the presence of bulk/buffer traps in the material that are activated at high fields and require further analysis.

To examine the breakdown properties of the deep-recessed FETs, the three-terminal OFF-state voltage breakdown was measured using a Keysight B1505A power device analyzer. The measurement was initiated after immersing the device under test in few drops of Fluorinert liquid to prevent air breakdown. For $L_{GD} = 1.4$ μm with the gate biased at $-15$ V, the device broke down catastrophically at $V_{DS} = 300$ V [Fig. 6(a)]. This translate to an average breakdown field of 2.3 MV/cm. On the other hand, an unpassivated FET with similar charge density ($\sim 10^{13}$ cm$^{-2}$) and architecture gave a Schottky limited breakdown of 164 V for the same $L_{GD}$ [4]. The deep-recessed FET therefore exhibits superior breakdown characteristics compared to its unpassivated counterpart.

2-D TCAD simulations were performed using SILVACO Atlas to estimate electric fields within the device at the onset of breakdown. A 2-D contour plot of the simulated electric field profile (with a recessed sidewall angle of 50°) at $V_{DS} = 300$ V and $V_{GS} = -15$ V is plotted in Fig. 6(b). As shown in the plot, the field peaks at the field-plate/passivation edge (point C in the graph). The validation of field-plate action for the deep-recess design is shown in Fig. 6(c) along a horizontal line “AB” from gate to drain. The total potential applied to the drain is normalized between the gate and the region below the field-plate edge. Since the peak field hotspot is located at the field-plate edge (point C), the device breakdown is limited by the field-plate/passivation layer edge and can be increased further through additional engineering of the passivation layer design and electrostatic fields within the device.

To access the device performance from a power switching perspective, the specific-ON resistance ($R_{ON, SP}$) of the device, normalized to $W_{D}X_{LD}$ [32], was extracted from the triode region of the $I_{DS}$-$V_{DS}$ curve at $V_{GS} = 0$ V. A power figure of merit ($V_{BR}/R_{ON, SP}$) of 118 MW/cm$^2$ was calculated for the device, which is reasonably proportionate to existing literature data for lateral and vertical $\beta$-$\text{Ga}_2\text{O}_3$ FETs benchmarked in Fig. 6(d).

V. Conclusion

In summary, we have demonstrated a deep-recessed delta-doped FET with UID $\beta$-$\text{Ga}_2\text{O}_3$ as the passivation dielectric grown in situ on the device epitaxial stack. Current depletion observed during the deep-recess etch of $\beta$-$\text{Ga}_2\text{O}_3$ by BCl$_3$ plasma, attributed to plasma damage that contributes to the emergence of deep level states in the material after recess, was mitigated through the use of a damage recovery anneal step. The FETs displayed negligible dispersion and better breakdown features compared to the unpassivated FETs, with scope for further improvement. The device architecture developed here is indeed promising to explore the potential of $\beta$-$\text{Ga}_2\text{O}_3$ for next-generation power, RF and mm-Wave device applications.

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