Vertical GaN Devices: Process and Reliability

Shuzhen Youa,*, Karen Geensa, Matteo Borgaa, Hu Liangb, Herwig Hahnb, Dirk Fahle, Michael Heuenb, Kalparupa Mukherjee, Carlo De Santic, Matteo Meneghinidi, Enrico Zanonie, Martin Bergd, Peter Ramvallie, Ashutosh Kumard, Mikael T. Björkc, B. Jonas Ohlssonc, Stefaan Decouterea

a imec, Leuven, Belgium
b AIXTRON SE, D-52134 Herzogenrath, Germany
c Department of Information Engineering, University of Padua, 35131 Padova, Italy
d RISE Research Institutes of Sweden, Scheelevägen 17, S-223 70, Lund, Sweden
e Hexagem AB, Ideon Alfa 3, Scheelevägen 15, S-223 63 Lund, Sweden

Abstract

This paper reviews recent progress and key challenges in process and reliability for high-performance vertical GaN transistors and diodes, focusing on the 200 mm CMOS-compatible technology. We particularly demonstrated the potential of using 200 mm diameter CTE matched substrates for vertical power transistors, and gate module optimizations for device robustness. An alternative technology path based on coalescence epitaxy of GaN-on-Silicon is also introduced, which could enable thick drift layers of very low dislocation density.

1. Introduction

GaN power devices have been widely recognized as promising candidates for next generation power electronics. High voltage blocking capability is key for efficiency gains in GaN power electronics. Currently, both lateral GaN HEMT and vertical GaN MOSFET are considered for achieving high breakdown voltage beyond 650V. When aiming at high voltage, lateral GaN devices are limited by the area occupancy and surface trap related reliability concerns. Contrary to the lateral GaN devices, vertical GaN devices do not require enlarged chip size for increased breakdown voltage. The breakdown voltage in vertical GaN devices can be increased by increasing the thickness of the drift region while keeping a compact chip size. Moving the peak electric field from the surface into the GaN bulk potentially minimizes the surface trapping effect and dynamic Ron in the vertical devices [1][2].

Today, GaN technology has presented transistors achieving breakdown voltages up to 1700 V and diodes with breakdown voltage up to 4000 V [3][4][5][6][7][8][9]. However, they have mostly been demonstrated only in research labs, and require special techniques/treatments that might not be suited for large scale fabrication. This paper reviews the progress and addresses key challenges in process and reliability, focusing on 200 mm CMOS-compatible technology.

We present 2 possible large diameter substrates for vertical GaN fabrication, which pave the way for industrial fabrication of this type of devices. Furthermore, the optimization of the doping level in the GaN device stack is discussed and finally the trench gate processing and the reliability of the fabricated MOSFETs are discussed.

2. Large diameter substrates for vertical GaN fabrication

2.1. Engineered CTE matched substrates.

State-of-the-art vertical GaN devices are fabricated on bulk GaN substrates, thanks to the high quality of the substrates in terms of low dislocation density and low impurity concentrations [10]. However, they are prohibitively expensive, and only small area substrates are available. Therefore, an industrially scaled process on bulk GaN substrates is not foreseen in near future. On the other end of the spectrum, several research groups have demonstrated (quasi-)vertical diodes and transistors on GaN-on-Si
substrates [11][12][13][14][15][16][17]. However, these devices have a limited drift layer thickness or a limited wafer diameter due to the large mismatch in coefficient of thermal expansion (CTE) between Si and GaN. QST® substrates, with a CTE matched poly-AlN core, can overcome these limitations and offer a breakthrough in growth of thick GaN epitaxial layer.

Qromis Substrate Technology (QST®) has been a pioneer in developing engineered substrates with SEMI standard thickness. The QST® substrate, depicted schematically in Fig. 1(a), includes a CTE matched poly-AlN core; engineered layers; buried oxide (BOX) and monocrystalline Si(111) serving as the nucleation layer for the metal–organic chemical vapour deposition (MOCVD) [18].

![Epitaxial GaN stack](image)

**Table 1.** XRD FWHM of GaN <102> and GaN <002>, comparing generation 1 & 2 epitaxy on engineered substrates, for a stack with a 3 μm thick drift layer, using a different Si doping level in the n-drift layer.

|  | GaN<102> FWHM (arcsec) | GaN<002> FWHM (arcsec) | NDn,drift (Si/cm³) |
|---|------------------------|------------------------|-------------------|
| Gen 1 | 627 | 260 | 4×10¹⁶ |
| Gen 2 | 406 | 227 | 2×10¹⁶ |

The potential of engineered QST® substrates for growing thick epitaxial layer and large wafer diameter, has been validated by several groups, by growing >10 μm, crack-free, device-quality epitaxial layers on 150mm substrates and 6 μm stack on 200mm substrates [19][20][21][22]. By introducing a dislocation reduction layer on these substrates, a low dislocation density in the order of 10⁷/cm² can be achieved[23][24]. Furthermore, these substrates have been used for fabrication of enhancement mode p-GaN gate HEMT devices, both for discrete components and monolithically integrated circuits, with (Al)GaN layers grown by means of MOCVD. Employing material grown in an AIX G5+ C Planetary Reactor® from AIXTRON, Germany, lateral devices including ICs were fabricated using imec’s advanced 200mm CMOS compatible Si pilot line [25][26][27][28]. QST® engineered substrates will be commercially available from both Shin-Etsu and Qromis for industry players [29][30] and can be scaled up in diameter to 300mm. By 2025 the price is expected to approach the one of SOI wafers, which paves the way for industrial fabrication of GaN power devices beyond 1200 V.

With respect to vertical GaN device fabrication, we demonstrated a crack-free MOCVD-grown 5.4 μm-thick GaN stack grown also in an AIX G5+ C Planetary Reactor®. The stack, shown in Fig. 1(b), consists of a 200 nm AlN nucleation layer, a strain-compensating buffer, a 1 μm unintentionally doped GaN layer, a 750 nm n⁺-GaN bottom contact, a 3 μm-thick n⁺ GaN drift layer, a 400 nm Mg-doped p-GaN channel layer and a 200 nm n⁺-GaN top contact layer. Careful engineering of the strain-compensating buffer layer is required to obtain an optimal crystal quality of the GaN-based stack. In this work we present two generations of vertical device stacks on engineered substrates. The difference in crystal quality is evident from XRD data as listed in Table 1. The XRD FWHM value was improved from 627 to 406 arcsec for the GaN <102> peak, indicating we were able to reduce the edge type dislocation density by 60% to an estimated amount of 4.5×10¹⁰ cm² [31]. The Si doping level from the generation 1 to 2, was reduced from 4×10¹⁶ cm⁻³ to 2×10¹⁶ cm⁻³ (Table 1).

The blocking voltage capability of these two generation stacks were evaluated by quasi-vertical NP diode test structures. In comparison of generation 1, generation 2 resulted in an increased breakdown voltage from 440 V to 680 V, as shown in Fig. 2(a). Benchmarked against the results from the devices on GaN-on-Si and GaN-on-GaN substrates, shown in Fig. 2(b), the breakdown voltage of the diodes in this work follows the projection of breakdown voltage versus drift layer thickness, validating the GaN on engineered substrates as a good choice for vertical device fabrication.

2.2. Coalesced nanowire GaN on Si substrates

GaN-on-Si using nanowire technology is another potential route towards thick, planar GaN drift layers with low dislocation density. The method is scalable
up to 200 mm wafers, at lower cost than standard technology due to the very thin buffer and coalesced layers needed, enabling 1200 V devices at a competitive price.

In this technology, key challenges are the pre-processing of growth templates for nanowire selective area epitaxy and coalescence of the GaN nanowires.[32][33][34] Nanowires are nucleated from patterned holes in a Si,Ni mask. Having small enough holes to effectively filter dislocations from the substrate is one of the critical elements to achieve low dislocation densities in the subsequent layers. A diffraction-based lithography method is developed for cost efficient scaling, as a full wafer can be exposed at once. Presently, holes with 110 nm diameter and a hole-to-hole coefficient of variance below 2.7% can be produced, as shown in Fig. 3(a). For coalescence on one quarter 2" GaN-on-Si template wafers, the layers show more than 90% surface coalescence coverage, and a smooth surface of 0.35 nm RMS roughness on a 2-μm-thick drift layer on top of coalesced material and a threading dislocation density of 6x10⁸ cm⁻², as shown in Fig. 3(b). These results lay the foundation for further improvements to nanowire coalescence, but also a platform for thick drift layer growth.

3. Doping in the vertical device stack

3.1. Doping optimization of the n-drift layer

Having a low background concentration in the drift layer is key for well-performing devices in the 1200 V-class and beyond. To reach the 1200 V breakdown voltage target, doping levels need to be below 1.5x10¹⁶ cm⁻³, ideally even at 1x10¹⁶ cm⁻³[35][36][37]. For reliable operation, the n-type donor (here: Si) needs to be roughly three times as large as the compensating C acceptor, i.e. for a net doping level n = Nd - Na = 1x10¹⁶ cm⁻³, the C level needs to be in the order of 5x10¹⁵ cm⁻³. A SIMS analysis of the stack of generation 1, depicted in Fig. 4 provides details on the chemical concentration of the individual layers. The n'-GaN layers are doped with 5.5x10¹⁵ Si/cc. The p-GaN layer has a 1.2x10¹⁸ Mg/cc doping level, with a net p-doping of 2x10¹⁸ cm⁻³. The drift layer has a Si doping level of 4x10¹⁶ cm⁻³ with a C background level of 1.5x10¹⁶ cm⁻³. By tuning the growth parameters, a good suppression of background carbon below 1x10⁸ cm⁻³ is achieved, allowing the reduction of the Si doping level to 2x10¹⁰ cm⁻³ in the stack of generation 2, this result in a boost of the breakdown voltage of diode, as depicted in Fig. 2(a).

Fig. 2 (a) Diode leakage curves comparing generation 1 and generation 2 epitaxy on 200 mm engineered substrates (b) Benchmark the breakdown voltage of diodes versus the drift layer thickness on various substrates.

Fig. 3 (a) < 110 nm holes with a pitch of 600 nm in 60-nm-thick SiNx growth mask layer down to the GaN-on-Si substrate. (b) AFM on a 2-μm-thick drift layer on top of coalesced material for the same substrate. A dislocation density of 6x10⁸ cm⁻² is estimated.

Fig. 4 SIMS profile of a stack of generation 1 with Si and C level of 4.0 and 1.5x10¹⁸cm⁻³ respectively.

3.2. p-GaN channel doping and activation

While designing the p-GaN layer, a good blocking capability of the reverse biased PN-diode and a low channel resistance at the p-GaN/gate trench interface must be combined. The channel
contribution to the device on-resistance, depends on both the channel length (which is defined by the p-GaN layer thickness) and on the inversion channel mobility (which increases with the p-doping). Fig. 5 depicts the correlation between $J_{D,SAT}$ and $R_{ON}$, showing reduced $R_{ON}$ and increased $I_{D,SAT}$ by reduction of p-GaN channel thickness and p-GaN Mg doping.

![Fig. 5: $J_{D,SAT}$ versus $R_{ON}$ correlation plots comparing (a) devices on engineered substrates with a different p-GaN channel length and (b) devices on Si substrates, with a different Mg doping level in the p-GaN layer.](image)

The output and transfer characteristic for a typical device with an 800 nm thick p-GaN layer is depicted in Fig. 6. For a channel length of 800 nm a current density of 0.35 kA/cm² is reached with a reasonably low $R_{ON}$ of 10 mΩ⋅cm².

On the other hand, the doping of the p-GaN layer can strongly impact the breakdown voltage. The p-GaN doping must be sufficiently high to avoid punch-through, and sufficiently low to reduce the peak electric field for device robustness [38][39].

![Fig. 6: Typical (a) output and (b) transfer characteristic of trench gate MOSFET device, with an 800 nm p-GaN channel processed on engineered substrates, with a poly-AlN core, using generation 1 GaN epitaxy.](image)

### 4. Gate processing and device reliability

The gate dielectric in a (semi-) vertical trench MOSFET, shown in Fig. 7(a), must be chosen to achieve a low channel resistance and a high breakdown of the gate dielectric. Thick gate dielectrics are desired for robustness of the gate and higher transistor off-state breakdown voltage. On the other hand, thick dielectrics degrade the drive current and $R_{ON}$. In our devices, a bilayer of a 2.5 nm Al₂O₃ and a 50 nm SiO₂ is used as gate dielectric. As shown in Fig. 7(b), increasing the thickness of SiO₂ results in lower drive current and higher $R_{ON}$.

![Fig. 7(a): Schematic cross-section of semi-vertical GaN MOSFET. (b) $J_{D,SAT}$ versus $R_{ON}$ correlation plots comparing devices on engineered substrates with different SiO₂ dielectric thickness in the gate trench region.](image)

Special attention is paid to the processing of the gate trench, as a preferential failure occurs at the corners of the gate fingers, as was indicated by the drain step stress test until breakdown, coupled with electroluminescence (EL) studies[40][41], shown in Fig. 8. Such failures were identified to have been caused by an electrical breakdown of the gate isolation at the bottom edges of the trench [42] and was correlated with the presence of several abrupt steps of the gate trench sidewall. Therefore, an optimized ALE processing and wet cleaning sequence was implemented to achieve a smooth gate trench sidewall, shown in Fig. 7(a).

![Fig. 8: Breakdown spot observed in $V_{DS}$ step stress test with electroluminescence imaging (a), and EL spot locations over both gate fingers (b).](image)
5. Conclusions

In this review paper, we have proposed two promising substrate choices to enable industrial fabrication of vertical GaN devices on large diameter substrates. In a first part, 5.4 μm-thick high quality MOCVD-grown GaN epitaxial layers on 200 mm engineered substrates, with a diode blocking capability of 680 V were demonstrated. A second substrate choice, being coalesced GaN nanowires on Si, is scalable up to 200 mm and has potential to demonstrate GaN growth with very low dislocation density. In the second part we have discussed the doping level optimization in the GaN device stack. On engineered substrates a net doping level of 1.5×10^{19} cm^{-3} has been achieved in the n-drift layer. A reference device using an 800 nm p-GaN channel with a 1.2×10^{19} Mg/cm^3 doping has been demonstrated, showing a current density of 0.35 kA/cm^2 and a reasonably low R_{Ohm} of 10 mΩ.cm^2. In the last part the trench gate reliability has been discussed, for which it is essential to implement a process which results in a smooth trench gate sidewall, combined with the use of a sufficiently thick gate dielectric.

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