Design of Fast Locking and Locking Detection System of Frequency Synthesizer

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Abstract. In some electronic reconnaissance fields, fast frequency switching is required. A radio frequency signal generator with fast lock and accurate lock time appears to be of great significance. Traditional detection requires additional equipment, which is expensive and cumbersome to operate without portability. This paper designs a simple, portable and easy-to-operate lock detection method, uses a timer to monitor the LD pin of the phase lock chip in real time, optimizes the algorithm for capturing signal edge transitions, and calculates the frequency switching time. The ADF4351 fast lock mode is combined with lock detection to improve the topology of the loop filter and speed up the lock time. With the keyboard and LCD module, a radio frequency signal source system capable of self-checking and locking time is constructed. Simulation and actual results verify that after changing the filter structure to achieve quick lock, the lock time is optimized by 16%, which verifies the effectiveness of quick lock and the accuracy of lock detection, and realizes efficient and convenient lock time detection.

1. Introduction

RF signal sources are widely used in electronic measurement, and fast lock-in is a very important requirement. However, there is no better way to detect the lock time. After consulting a large number of documents, I found that there is no fixed and reliable method to measure the frequency lock time. At present, there are two commonly used detection methods, one is to add lock detection circuit [1][2], the other is to use detection equipment, such as "spectrum analyzer measurement method", "oscilloscope direct measurement method", "VCO tuning voltage detection method", "signal source analyzer method" [3]. The additional detection circuit complicates the entire circuit design and has poor detection accuracy. The test equipment is expensive, heavy, inconvenient to carry, and lacks practical application scenarios. Detecting the tuning voltage of the VCO seems to be a good way, because after the loop is locked, the tuning voltage will stabilize again. Measuring the time difference between the two stable voltages will get the theoretical lock time, but there is always on the tuning terminal of the VCO Voltage. The signal causes a large deviation.

In this case, this work proposes a simple, convenient and easy-to-operate solution, focusing on the design of the LD lock time detection circuit and the time calculation algorithm. The system automatically controls the signal source to output dot frequency and sweep frequency signals, and cooperates with the fast lock topology to display the fast lock time on the LCD screen, which realizes the program requirements of simple calculation and lock time display.
2. Principle of phase-locked frequency synthesis

The basic structure of the phase-locked loop is shown in Figure 1. The function of the phase detector is to compare the frequency and phase difference between the input reference signal and the frequency-divided signal output by the VCO. According to this difference, an error voltage \( u_{up} \) or \( u_{down} \) is generated to control the output current of the charge pump, and then converted into a voltage value through the loop filter to adjust the VCO output frequency, and fed back to the phase detector through the frequency divider to reduce the difference between frequency and phase until the two are equal [4].

\[
\begin{align*}
\text{PFD} & \quad u_{up} \quad \text{CP} \quad V_c \quad \text{LPF} \quad V_{num} \quad \text{VCO} \quad \text{out} \\
& \quad \omega \\
& \quad N \text{ Devider}
\end{align*}
\]

Figure 1. Basic structure of PLL

3. System software and hardware design

The system uses the STM32F103 single-chip microcomputer as the main control chip to cooperate with the peripheral acquisition display and key input module. The ADF4351 phase-locked loop chip with integrated VCO is selected. The frequency output accuracy of 0.1MHz can be achieved in the range of 35MHz to 4400MHz. The output signal is passed through GS- The 1024 power divider is divided into two signals, one can be connected to a spectrum analyzer to check the spectrum of the output signal, and the other can be connected to the power conversion circuit to the A/D acquisition module to collect the voltage of the signal. The system structure diagram is shown in Figure 2.

\[
\begin{align*}
\text{Power conversion} & \quad \text{GS-1024} \\
& \quad \text{A/D acquisition} \\
& \quad \text{module} \\
& \quad \text{Timen module} \\
& \quad \text{Button module} \\
& \quad \text{Power attenuation} \\
& \quad \text{and filter module} \\
& \quad \text{ADF4351 with} \\
& \quad \text{integrated VCO} \\
& \quad \text{and third-order} \\
& \quad \text{passive loop filter} \\
& \quad \text{module} \\
& \quad \text{LCD module}
\end{align*}
\]

Figure 2. System hardware structure

3.1 Filter design for fast lock mode

In the phase-locked loop circuit, the design of the filter is relatively the most critical. The configuration of the parameters determines the loop bandwidth and phase margin of the system, which directly affects the lock time, phase noise and spurs [5]. ADIsimPLL simulation found that the higher the order of the filter, the final lock time will become longer, but as the frequency offset increases, the phase noise will decrease as the order increases.

The specific calculation of the parameters of the third-order filter is as follows [6], first the transfer function is:

\[
F(s) = \frac{1+ST_2}{S(1+ST_1)(1+ST_3)} \times \frac{1}{C}
\]

among them:

\[
C = C_1 + C_2 + C_3
\]

\[
T_2 = R_2C_2
\]
\[ T_1 T_3 = \frac{R_2 R_3 C_1 C_2}{C_1 + C_2 + C_3} \]  
(4)

\[ T_1 + T_3 = \frac{R_2 C_1 C_2 + R_2 C_2 C_3 + R_3 C_3 (C_1 + C_2)}{C_1 + C_2 + C_3} \]  
(5)

So the open loop transfer function is:

\[ H(s) = \frac{k_g k_{vco}}{j\omega N} \times \frac{1 + j\omega T_2}{j\omega (1 + j\omega T_1)(1 + j\omega T_3)} \]  
(6)

The phase margin is:

\[ \phi_w = \pi + \arctan(w T_2) - \arctan(w T_1) - \arctan(w T_3) \]  
(7)

Combining the relationship of the above formulas \( T_1, T_2, \) and \( T_3 \) obtain the corresponding values of \( T_1, T_2, \) and \( T_3 \), and then according to the gain of the open-loop transfer function as 1, the values of \( C_1, C_2, C_3 \) and \( R_2, R_3 \) can be obtained.

The topology of the loop filter is used to make the charge pump maintain the stability of the loop when increasing the current [7][8]. The topology is shown in Figure 3. The improved lock time comparison is shown in Figure 4.

3.2 Lock detection principle and design

Traditional instrument testing is too cumbersome and lacks portability. This design proposes a method based on LD pin output lock detection to detect the lock time of the output frequency. This design proposes a method based on LD pin output lock detection to detect the lock time of the output frequency.

In view of the above discussion, this design focuses on designing and optimizing the "LD level detection method" to measure the frequency lock time.

There are two methods of lock detection: analog lock detection and digital lock detection. The output stage of the analog lock indication is an N-channel open-drain structure, which requires a pull-up resistor, usually 10k to 160k, to obtain a flat high level through an integrating circuit. Analog lock detection is more complicated in circuit design, which limits its accuracy, and it is impossible to accurately judge whether it is locked [9][10].

Digital lock detection has high accuracy, easy implementation and high programmability, so this design adopts digital lock detection.

The basic principle is that the phase detector compares the phase difference between the frequency-divided signal output by the VCO and the reference signal, and sets a detection window. The principle diagram of the detection window is shown in Figure 5.
If the phase difference does not exceed this set window for N consecutive cycles, it means that the output is locked and LD becomes high, otherwise it remains low. The simulation results using ADIsimPLL are shown in Figure 6.

### 3.3. Lock detection software design

The LD detection bit is detected by the timer input capture interrupt mode, and the input capture mode can be used to measure the pulse width or measure the frequency. The specific lock time detection software implementation flowchart is shown in Figure 7 below.

![Figure 7. Lock time detection flowchart](image)

Channel 3 (PA2) of TIM2 is selected in the system to capture the low-level pulse width on PA2, PA2 is connected to LD, and the continuous low-level state on the LD pin is detected. First set the input capture as falling edge detection, and record the value of TIM2_CNT when the falling edge occurs. Then configure the capture signal to capture on the rising edge. When the rising edge comes, capture occurs, and record the TIM2_CNT value at this time. In this way, the difference between the two TIM2_CNT before and after is the low-level pulse width, so that the accurate time of the low-level pulse width can be calculated, which is the lock time in the dot frequency test system.

### 4. Experimental results and analysis

Through the hardware design and software programming in the previous sections 3.2 and 3.3, lock detection is realized. In order to verify its accuracy, the minimum sweep time of the spectrum analyzer
is 100ms, which is too far from the lock time of tens of us, so it was decided to use the simulation result as the comparison group. Observe whether the numerical difference of the lock time of the corresponding frequency and the change trend of the data following the frequency change are in line with the change trend of the simulation, and use this as the criterion for judgment. The experimental conditions are all 100KHz bandwidth and 45° phase margin. The following Figures 8 and 9 are the comparison between the actual detection and simulation results of LD before and after the quick lock is added. Figure 10 is a separate comparison of two LD detection times.

![Figure 8. Lock time without quick lock](image1)

![Figure 9. Lock time with quick lock](image2)

![Figure 10. Comparison of LD lock time with or without quick lock](image3)

As can be seen from the above three figures, our LD lock detection time curve fluctuates around the simulation value, and the error range does not exceed 20us. The lock time can be measured more accurately. After adding quick lock, simulation data improved by an average of 18%. The lock time detected by LD has also improved by 16%. The validity of quick lock and the accuracy of lock detection are verified. Figures 11 are the spectrum accuracy measured by a spectrum analyzer. Figure 12 is the full view of the work.

![Figures 11. 542.6MHz spectrum](image4)

![Figure 12. Full view of the work](image5)
5. Conclusion
This article mainly designs a radio frequency signal source output control system that uses the LD pin of ADF4351 to detect the lock time. Using STM32F1 as the main control chip, combined with TFTLCD LCD screen and keyboard input, the output frequency and lock time are displayed well. The LD lock detection also verified the effectiveness of the quick lock structure, and the actual lock time was shortened by about 16% through the LD detection. The lock time detection designed by this system is separated from expensive and large-scale test instruments, has the advantages of low power consumption, portability, and easy operation, and provides a better solution for the measurement of the lock time of the RF signal source.

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