Tunable active inductor based VCO and BPF in a single integrated design for wireless applications in 90 nm CMOS process

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Abstract
This article proposes a tunable active inductor (AI)-based voltage-controlled oscillator (VCO) and bandpass filters (BPF) on a single integrated design in 90 nm CMOS process for wireless applications. By exploiting component sharing technique through single pole double throws switching method, a common AI is shared between VCO and BPFs. As the passive inductor is replaced by the AI and shared, silicon area consumption is significantly reduced. Transforming the inductor in tunable mode benefits to eliminate MOS varactors for tuning purposes; one step forward to reduce silicon area consumption. Operating as VCO, its frequency ranges from 1.93 to 6.22 GHz (tuning scope is 105%) for tuning voltage of 0.2 ∼ 1 V. The DC power consumption varies from 1.83 to 3.84 mW, and differential output power is 3.39 to −2.99 dBm. The phase noise varies from −81.32 to −76.89 dBc/Hz, and the figure of merit has a value of −148.74 dBc/Hz at 5.03 GHz frequency. While acting as BPF, two approaches of center frequency tuning are applied. The voltage tuning yields center frequency of 8.43 ∼ 7.08 GHz along with the maximum gain of 10.29 dB at 7.81 GHz. The capacitive tuning outputs frequency tuning of 7.64 ∼ 7.06 GHz. The BPF consumes DC power of 2.56 to 2.27 mW (voltage tuning) and 2.40 mW (capacitive tuning). The proposed design occupies a layout area of 1215.6 μm². All the simulations have been performed considering parasitic elements evolved from the extraction of layout. Finally, a quantitative comparison and justification of the proposed design are made with respect to other published works.

KEYWORDS
active inductor, BPF, DC power consumption, frequency, phase noise, VCO

1 INTRODUCTION

The acceleration of leading-edge communication systems is making performance efficient radio frequency integrated circuits (RFICs) highly demandable. Voltage-controlled oscillators (VCOs) with extensive tuning range are fundamental blocks of almost all RFICs for multiband and multi-standard applications. In the evolving era of Internet of things (IoT),
connecting billions of electronic gadgets is facilitated by fast and low-cost development of VCO based analog-to-digital converters. One of the primary building blocks of incoming carrier frequency detector, that is, phase locked loop (PLL), is VCO, contributes significantly to enhance its performance. Furthermore, VCO has immense applications in designing impulse generator for ultra-wideband transmitter, digital FM modulator, and frequency synthesizer. The two most recognized VCOs’ topologies are ring VCO and LC VCO. Ring VCO provides a broader tuning range and smaller silicon area, whereas LC VCO shows excellent phase noise performance.

Another crucial component in a multi-service mobile wireless communication system is the bandpass filter (BPF). Being functional in diverse frequency bands, microwave devices such as the global system for mobile communications (GSM), wireless LAN, and the RF transceiver should be capable of transmitting and receiving band-specific signals. So, the BPF as a significant block rejects unwanted frequencies. Furthermore, BPFs, along with superior performance and optimized area, enhances the overall performance of the RF system. LC BPFs and RC BPFs are the two most widely used filters’ topologies.

Both LC VCO and LC BPFs can be designed using either an active or spiral inductor. In terms of cost-effectiveness, resistance, durability, and flexible layers implementations, the usages of spiral inductors are highly promising. Despite having advantages, the spiral inductor based design has the drawbacks of poor quality factor and significant silicon area consumption. Likewise, to design high-performance circuits with tunable frequency, the low and fixed inductance of spiral inductors along with low self-resonant frequency is a significant obstacle. But, these obstructions of spiral inductors can be rectified by replacing it with active inductors (AIs). Inherently, occupying a minimal chip area and consuming less power, high and tunable inductive value, self-resonant frequency, and high-quality factor, AIs yield tremendous performance. Nonetheless, researchers are working toward minimizing the drawbacks of AIs possessing poor noise performance since active elements are used, and additional DC static power consumed for the biasing purpose.

Exploiting the advantages of AI, this article proposes a VCO and two BPFs in a single integrated design. The proposed design works as two BPFs or a VCO at a time, and the single pole double throws (SPDT) switching system controls their modes of operations. So, the AI core for two separate applications can be incorporated. The major contribution of this research is to propose a single design that can work both as BPF and VCO. At first, the schematic is proposed, and then the layout based simulations have been conveyed to confirm its effectiveness with accuracy. Finally, process corner, temperature sweep, and Monte Carlo analysis have been done to illustrate the design’s compatibility in diverse environments.

Having studied the prior works in the relevant field, several researchers’ contributions can be mentioned. Kao et al. had proposed a tunable AI based CMOS VCO having 169% tuning range (0.6 ∼ 7.2 GHz) in 0.18 μm CMOS technology. Both inductors and varactors are exploited to achieve frequency tuning. The observed phase noise is −110.38 ∼ −86.01 dBc/Hz at 1 MHz offset and the VCO provides output power of −11.11 ∼ −3.89 dBm. However, the major constraint is the extreme DC power dissipation (49 mW from 1.8 V power supply) while generating a comparatively low output power. Ghorbel et al. had presented a digitally controlled oscillator using CMOS controllable inverters based AI. The maximum generated frequency for the 4 bits scheme is 2.45 GHz with 6.89 mW power consumption. This article also demonstrates results for 2 bits (1.45 ∼ 1.88 GHz) and 6 bits (1.82 ∼ 3.01 GHz) schemes. Kia and A’ain had designed a high tunable AI-based CMOS VCO, and its frequency range is 0.12 to 2 GHz (tuning range 94%) in 0.18 μm CMOS technology. Variation of the PN (phase noise) is from −80 to −90 dBc/Hz at 1 MHz frequency offset, and DC power dissipation is 7 mW. The output power varies from −4.7 to +11.5 dBm. Both inductance and quality factor of the core AI circuit is reconfigurable. Researchers do not bind themselves with AI-based VCO. There are also numerous subsisted examples where AIs are implemented as an alternative to the bulky counterparts. Bhuiyan et al. had shown a broad review of various AI-based BPFs, along with efficient noise elimination techniques. This review discusses current-reused AI, Karsilayan-Schaumann AI, grounded cascaded AI, and single-transistor AI-based BPFs. Performance comparison of AI based BPFs is also presented in a tabular format. Selvathi and Pown had proposed an AI based second-order BPF in TSMC 0.18 μm RF CMOS process for radiofrequency receiver applications. PMOS cascode is embedded in core AI to compensate for the resistive loss, and a controllable current source helps to tune the center frequency. Nevertheless, the major constraints are low center frequency (100 MHz) and extreme DC power dissipation (38 mW) from 1.8 V power supply. A tunable BPF based on an optimized tunable differential AI in 0.13 μm CMOS technology had been proposed by Ben Hammadi et al. in Reference 16. The center frequency is tuned from 1.16 to 3.27 GHz. The range of gain (S21) is 26.62 to 33.45 dB and consumed power from the source is 4.04 to 6.44 mW. However, the concerning issue might be the noise figure (14.48 ∼ 16.56 dB), which is due to active elements existed in the core AI.

This research article is organized into six separate sections. Section 1 introduces the research idea with literature reviews. Section 2 discusses AI, LC VCO, and LC BPF topology briefly. Section 3 shows the analysis and design of the proposed idea, whereas Section 4 validates the design through layout based simulations. Section 5 justifies the design with relevant literature reviews and illustrates the applications. Finally, Section 6 concludes the article.
2 | **AI, LC VCO, AND BPF**

### 2.1 | **AI topology**

After the first introduction of the basic AI, its performance parameters had become primary considerations of researchers. Weng and Kuo\(^\text{17}\) placed a cascode to the basic model. This results in suppression of loss that emerged from equivalent series resistance. A significant improvement was proposed by Manetakis et al in Reference\(^\text{18}\). The modification is addition regulated cascode, much reduction of loss from series resistance. To boost the inductance and quality factor of Manetakis regulated cascode AI, later, a feedback resistor was embedded by Liang et al.\(^\text{19}\) The schematic diagram, small-signal equivalent circuit (Figure 1), and the equations given below indicate the clear illustrations.

Figure 1A shows the regulated cascode AI, and Figure 1B illustrates the equivalent small-signal model of regulated cascode AI.\(^\text{11}\) Figure 1C represents the final equivalent circuit of AI. Here MOS \(M_3\) and \(M_4\) collaboratively act as regulated cascode. \(R_p, R_s, C_p,\) and \(L\) are equivalent parallel resistance, series resistance, parallel capacitance, and series inductance, respectively. The equation of series resistance is,

\[
R_s \approx \frac{g_{ds3}g_{ds4}}{g_{ds3}g_{m1}g_{m2}g_{m3}g_{m4}},
\]

\(R_s\) is called resistive loss and has an effect over the quality factor (the equation is given later). It is the reason to use regulated cascode. Here, it is clear from Equation 1 that the denominator of newly found \(R_s\) has additional \(g_{m3}, g_{m4}\) come from regulated cascode. Similarly, the feedback resistor adds an extra multiplying factor \((1 + R_f g_{ds1})\) to equivalent inductance \(L\). We can realize it from the equation of inductance as given below,

\[
L \approx \frac{C_{g2}(1 + R_f g_{ds1})}{g_{m1}g_{m2}}.
\]

These joint accompaniments by regulated cascode and feedback resistor finally boost up the quality factor. Higher quality factor aids to low the phase noise of oscillator as well as enhance the quality factor of BPF. That is why the topology is selected.

The resonant frequency \(\omega_0\) and the quality factor \(Q\) at resonant frequency are as follows,

\[
\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_{g2}C_{g2}(1 + R_f g_{ds1})}} \quad \text{and} \quad Q(\omega_0) = \frac{L}{R_s} = \frac{g_{ds1}g_{m3}g_{m4}}{g_{ds3}g_{ds4}} \sqrt{\frac{g_{m1}g_{m2}C_{g2}(1 + R_f g_{ds1})}{C_{g2}}},
\]

\[\text{FIGURE 1} \quad \text{A. Regulated cascode active inductor with feedback resistor. B, Equivalent small-signal model. C, Equivalent circuit model of AI}\]
The equations for other parameters \( C_p \) and \( R_p \) in the equivalent circuit are given below,

\[
C_p \approx C_{gs1}
\]

\[
G = \frac{1}{R_p} \approx g_{ds2} + \frac{g_{m1}}{1 + R_f g_{ds1}}.
\]

### 2.2 LC VCO and BPF

To start and sustain oscillation in a lossy LC tank, a negative resistor needs to be connected in parallel with the LC tanks. The two distinct functions of the added negative resistor are providing high voltage gain to the amplification stages to start an oscillation and making the loss of the oscillator significantly small to sustain oscillation. Cross-coupled transistor pair consisting of \( M_{1,2} \) and tail biasing current source \( J \) form the conventional differential negative resistor shown in Figure 2A. By varying the DC biasing current, the resistance of the negative resistor can be regulated. For completely diminishing the ohmic loss of the tanks, resistance of the negative resistor must be equal to that of the tank. The variable capacitor, that is, varactor shown in the figure is used for tuning purposes, which will be eliminated by the inductive tuning of the AI.\(^{20}\)

An AI itself is an RLC tank circuit and thus a BPF with the pass-band center frequency being the self-resonant frequency which can be realized through Figures 1C and 2B. The input voltage of the filter is transformed into the current flowing into the subsequent AI by the input buffer. The matching network in the front end performs impedance matching. The desired frequency selection is executed by the AI as it is an RLC tank. Sufficient driving current and matching output impedance are supplied to the load by the output buffer.\(^{20}\)

### 3 PROPOSED VCO AND BPFS IN A SINGLE INTEGRATED DESIGN

#### 3.1 Proposed design

Figure 3 shows the proposed design where a VCO and two BPFs are integrated on a single circuit. As the ideal current source is impractical to be implemented, it is replaced by a MOS operated in the saturation region. An SPDT switching system is employed to change the mode of operations. While acting as BPF, the input buffer and the output buffer are connected to the AI core, which is denoted in the figure. Similarly, as VCO, the input buffer and output buffer are separated, and then the inductor is to be attached to the cross-coupled configuration. \( M_1 = M_3 = 10 \mu m, M_2 = 11 \mu m, M_4 = 25.5 \mu m, M_5 = M_7 = 6 \mu m, M_6 = 2.5 \mu m \) are used as the width of MOSs implemented into the proposed circuit. Feedback resistor \( R_f \) has a value of 1 kΩ. When acting as BPF, \( V_{\text{tune}} \) and \( C_{\text{tune}} \) are used to regulate center frequency. In that case, \( V_{\text{con}} \) has to be replaced by \( V_b = 0.5 \) V (biasing voltage). Likewise, \( V_{\text{tune}} \) is set at 0.5 V and \( C_{\text{tune}} \) has been remained inactive while acting as VCO. \( V_{\text{con}} \) is used for the tuning purpose of the oscillation frequency of VCO. The \( V_{DD} = 1 \) V is used for both of the cases.

In the case of VCO, NMOS cross-coupled configuration is utilized where \( M_{\text{neg}} \)s are used as a negative resistor whose resistance is regulated by \( M_8 \). The differential output had been taken from Out1 and Out2 terminal. According to the
general current formula $[I_D \propto (V_{gs} - V_t)^2]$ of NMOS, the application of voltage to the gate of $M_6$ changes the current through the MOS $M_6$ and also through $M_2$. This causes to change $g_{m2}$ [as $g_m \propto \sqrt{I_D}$], which affects the inductance $L$ as per Equation 2. The variation in the $L$ changes the oscillation frequency of the oscillator, and it is a noticeable outcome. Figure 2A shows that to regulate the frequency of oscillation, we have to employ additional varactors, that is, variable capacitors due to spiral/passive inductor’s incapability to tune. These additional varactors occupy extra silicon area. However, the integration of AI facilitates us to leave the varactor as the inductor has tuning ability. Elimination of varactor helps to save significant silicon area consumption.

$M_{in}$ and $R_{in}$ together form the input buffer for the BPF circuit, converts the applied voltage to current, whereas $M_{out}$ and $R_{out}$ together form the output buffer circuit. The dotted portion marks the AI part. By changing $g_{m1}$, $g_{m2}$, or $C_{gs2}$, the inductance can be adjusted according to Equation 2. Drain current of $M_1$ can be regulated by $V_{tune}$, that is, the gate voltage of MOS $M_7$. Then the $g_m$ (as $g_m \propto \sqrt{I_D}$) of the MOS $M_1$ can be controlled, finally control over the center frequency (as $f_0 = \frac{1}{2\pi\sqrt{LC}}$). Through capacitive tuning using $C_{tune}$, a capacitor is to be connected in parallel to $C_{gs2}$, and center frequency can be adjusted by varying $C_{tune}$.

3.2 | SPDT switching system

Figure 4 depicts the SPDT switching system in the proposed design. Despite its simplicity, it has an outstanding significance in future analog circuit design. Through applying it, several analog blocks can be integrated into a single chip by sharing a similar component. A significant amount of silicon area can be saved, especially if the shared component is a bulky element. To understand the system, we have to focus on the bipolar pulse inverter circuit into it. That means when the input of the inverter is $+V_{DD}$, the output of the inverter is $-V_{DD}$. The difference from conventional CMOS inverter is another negative supply $-V_{DD}$ is connected to the source of NMOS instead of ground. A similar system is to be applied to the output buffer. Two cases of applied voltage $V_{switching}$ are given in Table 1.

By applying two signals of different frequencies (0.5 and 2 GHz) to two throws, the SPDT system can be illustrated rigorously. The amplitudes were kept the same, and the output was taken from the pole. Figure 5 shows the simulation result. The blue-colored (middle) signal is the high-frequency signal (2 GHz), the red-colored (upper) is for low-frequency signal (0.5 GHz), and the black-colored (bottom) indicates signal in the pole. For case 1, a low-frequency signal is passed; however, the high-frequency is blocked. For case 2, the opposite scenario occurs.
TABLE 1 Operating modes of SPDT switching system

| Cases | $V_{\text{switching}}$ | Gate voltage of MOS a | Gate voltage of MOS b | Operating condition of MOS a | Operating condition of MOS b | Action |
|-------|------------------------|-----------------------|-----------------------|-----------------------------|-----------------------------|--------|
| Case 1 | +1.5 V | +1.5 V | −1.5 V | Saturation and short circuit | Cut off and Open circuit | AI will be connected to VCO |
| Case 2 | −1.5 V | −1.5 V | +1.5 V | Cut off and open circuit | Saturation and short circuit | AI will be connected to BPF |

4 | SIMULATION RESULTS

4.1 | Layout of the proposed design

Despite the feasibility of conducting simulation through schematic, there is a question of accuracy through transistor-level simulation. The schematic based transistor-level simulation ignores parasitic capacitances, and resistances evolved while
doing fabrication. So, the layout of the proposed design was performed at first. Then the RC extracted layout-based simulations were done to determine the performance parameters. Metal1, Metal2, Metal3, and Polysilicon were used for the interconnecting purpose. Several issues were considered while doing the layout. Interdigitalization was done using multi-fingered transistors, which had made the layout more compact. Finally, an N+ guard ring in conventional form had been placed. To determine the parasitic inductors, RLC extraction has also been done, which calculates additional 43 parasitic inductors evolved from long interconnection. The layout in Figure 6 shows that it consumes a total area of 60 µm × 20.26 µm or 1215.6 µm².

4.2 | Simulation of VCO

By setting the value of \( V_{\text{switching}} = +1.5 \text{ V} \), the circuit can be operated as VCO. In that case, the input and output buffers are disconnected from the core AI. The control voltage had been tuned from 0.2 to 1 V, and the change of frequency occurs from 1.93 to 6.22 GHz having the tuning range of 105%. The differential output power varies from +3.39 to −2.99 dBm, and phase noise at 1 MHz offset changes from −81.32 to −76.89 dBc/Hz. Finally, the figure of merit, FOM (in dBc/Hz), considering three basic performance parameters is calculated according to Equation (3),

\[
FOM (\text{dBc/Hz}) = L(\Delta \omega) + 10 \log \left( \frac{P_{\text{diss}}}{1\text{mW}} \right) - 20 \log \left( \frac{\omega_o}{\epsilon \omega} \right),
\]

(2)

where \( L(\Delta \omega) \) is the phase noise at \( \Delta \omega \) offset frequency, \( P_{\text{diss}} \) is the DC power consumption in mW, and \( \omega_o \) is the oscillation frequency. We can also express the FOM in another form, which is in the dBF unit. The corresponding equation is given below,

\[
FOM(\text{dBF}) = 20 \log(\text{freq}) - \text{phase noise} - 10 \log(P_{\text{diss}}).
\]

(3)

Table 2 shows the performance parameters of the VCO for various tuning voltages.

Figure 7A shows the differential sinusoidal oscillation for \( V_{\text{con}} = 0.6 \text{ V} \), and Figure 7B shows the phase noise vs frequency offset. For a frequency offset of 1 MHz, the phase noise is −78.87 dBc/Hz. Figure 8A depicts the DC power consumption vs tuning voltage within the range of tuning voltages. Higher \( V_{\text{con}} \) causes more current/power to be drawn from the supply. The maximum drawn power is 3.84 mW, and the almost linear relationship can be clarified from the figure. Figure 8B demonstrates the generated oscillation frequency vs tuning voltage from where an outstanding outcome can be justified, that is, the generated frequency covers both 2.4 and 5 GHz frequency bands. In other words, this VCO can be applied for both 802.11a and 802.11b applications. Figure 8C indicates the FOM. The feature of the figure concludes that FOM, that is, the overall performance parameter of VCO is almost stable with the change of tuning voltage.

4.2.1 | Process corner analysis

In the semiconductor integrated circuit (IC) industry, an example of design-of-experiments (DoE) is process corner analysis. It means deviation of process parameters from their typical values while fabricating an IC on a semiconductor wafer. Process corners are the maximum ranges of variations, and any proposed design must have functionality within all the
Table 2: Performance parameters of VCO for varied tuning voltages

| $V_{\text{con}}$ (V) | $f_o$ (GHz) | Phase noise @ 1 MHz offset (dBc/Hz) | DC power diss. @ 1 V (mW) | Differential output power (50 $\Omega$) @ $f_o$ (dBm) | Figure of merit (FOM) |
|-----------------|-------------|-------------------------------|-------------------------|-----------------------------|------------------------|
| 0.2             | 1.93        | −81.32                        | 1.83                    | 3.39                        | −144.42                |
| 0.3             | 2.15        | −78.99                        | 1.87                    | 3.32                        | −142.93                |
| 0.4             | 3.12        | −77.41                        | 2.02                    | 2.65                        | −144.25                |
| 0.5             | 4.24        | −78.08                        | 2.29                    | 1.99                        | −147.03                |
| 0.6             | 5.03        | −78.87                        | 2.61                    | 1.49                        | −148.74                |
| 0.7             | 5.52        | −79.19                        | 2.94                    | 0.87                        | −149.34                |
| 0.8             | 5.82        | −78.70                        | 3.27                    | −0.08                       | −148.86                |
| 0.9             | 6.04        | −77.96                        | 3.57                    | −1.36                       | −148.05                |
| 1.0             | 6.22        | −76.89                        | 3.84                    | −2.99                       | −146.92                |

Figure 7: Simulation of VCO: A, differential output oscillation for $V_{\text{con}} = 0.6$ V and, B, phase noise vs frequency offset for $V_{\text{con}} = 0.6$ V

4.2.2 Temperature sweep analysis

Mobility and threshold voltage are different process parameters having a dependency on temperature, so the proposed design should have the capability to endure the variation of temperature. To check how the VCO’s properties vary with that of temperature variance, temperature sweep analysis had been performed for five different temperatures from $-50^\circ$C to $50^\circ$C. This study had been done against tuning voltage of 0.6 V. The tuning range, tuning scope (%), phase noise at 1 MHz offset, and DC power consumption is presented in Table 4.
**FIGURE 8** Simulation of VCO: A, DC power consumed for varying tuning voltage, B, frequency vs tuning voltage, and, C figure of merit vs tuning voltage of the proposed design

**TABLE 3** Data table and comments for process corner analysis

| Corners | Oscillation frequency (GHz) | DC power con. (mW) | Phase noise @ 1 MHz offset (dBc/Hz) | Tuning scope (%) | Comments |
|---------|-----------------------------|-------------------|-------------------------------------|-----------------|----------|
| SS      | 1.32 ∼ 4.55                | 1.17 ∼ 2.53       | −82.36 ∼ −74.24                     | 110.05          | Tuning scope - Good  
Power con. - Low  
Oscillation freq. - Low |
| SF      | 2.57 ∼ 5.53                | 2.01 ∼ 2.80       | −77.67 ∼ −77.35                     | 73.09           | Tuning scope - Low  
Power con. - Low  
Oscillation freq. - Good |
| FS      | 1.39 ∼ 5.83                | 1.41 ∼ 4.09       | −80.47 ∼ −74.15                     | 122.99          | Tuning scope - Highest  
Power con. – Reasonable  
Oscillation freq. – High |
| FF      | 2.61 ∼ 8.09                | 2.56 ∼ 5.53       | −80.01 ∼ −76.18                     | 102.43          | Tuning scope - Good  
Power con. – Highest  
Oscillation freq. – Highest |
Figure 9 Graphical presentation of process corner analysis: A, frequency vs tuning voltage, B, DC power consumption vs tuning voltages, and, C, variation of phase noise at 1 MHz offset with tuning voltages for SS, SF, FS, FF corners

Table 4 Data table for temperature sweep analysis

| Temp  | Oscillation frequency (GHz) | DC power con. (mW) | Phase noise @ 1 MHz offset (dBc/Hz) | Tuning scope (%) | Comments                                                   |
|-------|----------------------------|--------------------|--------------------------------------|------------------|-----------------------------------------------------------|
| −50°C | 2.23 ~ 7.95                | 1.98 ~ 4.97        | −81.37 ~ −76.09                      | 112.38           | High temperature is supportive for DC power con., but not for oscillation frequency and tuning scope. |
| −25°C | 2.11 ~ 7.30                | 1.93 ~ 4.54        | −81.53 ~ −76.43                      | 110.31           |                                                           |
| 0°C   | 2.01 ~ 6.74                | 1.88 ~ 4.18        | −81.72 ~ −76.72                      | 108.11           |                                                           |
| 25°C  | 1.94 ~ 6.25                | 1.84 ~ 3.86        | −81.36 ~ −76.92                      | 105.25           |                                                           |
| 50°C  | 1.88 ~ 5.83                | 1.80 ~ 3.58        | −81.15 ~ −76.86                      | 102.46           |                                                           |

Figure 10A depicts the frequency vs tuning voltages when the temperature is varied from −50°C to 50°C. Figure 10B depicts the variation of DC power. Figure 6C demonstrates phase noise at 1 MHz offset vs tuning voltages for different operating temperatures.

4.2.3 | Monte Carlo analysis

When ICs are manufactured, small random variations occur in the features of identically modeled devices; this is called device mismatches. Behavioral variations arise due to these mismatches in the case of both digital and analog ICs. Most
often, it is tough to make an assumption about the exact behavior of a circuit due to mismatch errors from individual devices. However, the effects of the variation of random parameters on any ICs can be analyzed through Monte Carlo Simulation. It is done by a thorough analysis of a large set of circuit instantiations due to random variation of devices.

The Monte Carlo analysis of the proposed design had been performed for both process variation and mismatch cases simultaneously for tuning voltage of 0.6 V, and 100 samples were considered for oscillation frequency, phase noise at 1 MHz offset, and DC power consumption. Figure 11 shows the statistical presentation of Monte Carlo Simulation results for frequency, DC power consumption, and phase noise. The oscillation frequency has a mean of 4.68 GHz with an SD of 0.053 GHz, where for the case of DC power consumption they are 2.60 mW (mean) and 0.039 mW (SD). Here, a very low SD occurs. Finally, in case of phase noise at 1 MHz offset, the mean is $-79.03$ dBc/Hz, having a lower SD of 0.102 dBc/Hz.

Table 5 summarizes the performance of VCO and quantitative comparison with other published designs.

### 4.3 Simulation of BPF

Here, the two AIs are acting as two separate BPFs. By setting the value of $V_{\text{switching}} = -1.5$ V, the circuit can be operated as BPF, where the input and output buffer are to be attached to the core AI. Two methods of central frequency tuning are implemented here. First, voltage tuning was achieved by altering the gate voltage, $V_{\text{tune}}$. Similarly, capacitive tuning was achieved by using an additional parallel capacitor $C_{\text{tune}}$. $V_{\text{tune}}$ was kept 0.515 V in case of capacitive tuning. Conversely, $C_{\text{tune}}$ was kept inactive while $V_{\text{tune}}$ was used for tuning purposes.
**FIGURE 11** Monte Carlo analysis: A, statistical distribution of oscillation frequency, B, DC power consumption, and (C) phase noise at 1 MHz offset for $V_{\text{con}} = 0.6$ V

**TABLE 5** Performance comparison of the VCO with other published works

| References | 21 | 22 | 23 | 24 | 25 | This work |
|------------|----|----|----|----|----|-----------|
| Technology | 45 nm CMOS | 180 nm CMOS | 90 nm CMOS | 180 nm CMOS | 90 nm CMOS | 90 nm CMOS |
| $V_{\text{DD}}$ (V) | ±1 | 1.8 | 0.9 | 1.8 | 1.2 | 1 |
| Power (mW) | 0.53 ~ 1.34 | 4.63 ~ 10.54 | 20 | 16.27 | 22 | 1.83 ~ 3.84 |
| Tuning Range (GHz) | 0.41 ~ 0.69 | 1.61 ~ 3.71 | 37.7 ~ 41.9 | 0.1 ~ 2.5 | 0.6 ~ 11.8 | 1.93 ~ 6.22 |
| Tuning Range (%) | 51.36 | 78.52 | 10.55 | 184.6 | 180.65 | 105 |
| Output Power (dBm) | — | — | — | 5 ~ 15 | — | 3.39 ~ 2.99 (differential) |
| PN@ 1 MHz (dBc/Hz) | −90.86 ~ −83.7 | −89 | −78.8 | −93 ~ −80 | −85.77 ~ −73.93 | −81.32 ~ −76.89 |
| FOM (dBc/Hz) | −139.34 ~ −145.8 | −146.5 ~ −150.1 | — | −120.88 ~ −135.84 | −127.91 ~ −141.33 | −144.42 ~ −149.34 |
| Layout Area ($\mu$m²) | 1212.5 | 2070 | — | 9600 | — | 1215.6 (VCO + BPF) |

### 4.3.1 Tuning of center frequency by $V_{\text{tune}}$

As $V_{\text{tune}}$ is increased, the drain current, $I_D$ of MOS $M_7$ declines which decreases transconductance $g_{mt}$ of the MOS $M_1$. The inductance raises, and finally, the center frequency lessens (Equation (2)). $V_{\text{tune}}$ had been varied from 0.48 to 0.54 V with an interval of 0.01 V. Table 6 exhibits basic performance parameters of the BPF when $V_{\text{tune}}$ was used to tune center...
### Table 6: Performance summary of the BPF when $V_{\text{tune}}$ is applied

| $V_{\text{tune}}$ (V) | Center freq., $f_o$ (GHz) | $S_{21} @ f_o$ (dB) | $S_{11} @ f_o$ (dB) | DC power con. (mW) | Noise figure @ $f_o$ (dB) |
|------------------------|---------------------------|---------------------|---------------------|-------------------|--------------------------|
| 0.48                   | 8.43                      | 7.20                | -33.19              | 2.56              | 22.70                    |
| 0.49                   | 8.23                      | 8.55                | -26.13              | 2.51              | 22.95                    |
| 0.50                   | 8.03                      | 9.67                | -22.76              | 2.47              | 23.18                    |
| 0.51                   | 7.81                      | 10.29               | -20.88              | 2.42              | 23.42                    |
| 0.52                   | 7.58                      | 10.25               | -20.62              | 2.37              | 23.66                    |
| 0.53                   | 7.34                      | 9.55                | -21.77              | 2.32              | 23.88                    |
| 0.54                   | 7.08                      | 8.37                | -24.04              | 2.27              | 24.16                    |

### Figure 12: Tuning of center frequency by $V_{\text{tune}}$: A, $S_{21}$ vs frequency, and, B, $S_{11}$ vs frequency

The parameters are center frequency ($f$), forward gain ($S_{21}$), return loss ($S_{11}$), DC power consumption, and noise figure.

Figure 12A,B presents forward gain $S_{21}$ (dB) and return loss $S_{11}$ (dB) with respect to frequency. The range of center frequency is observed to be from 7.08 to 8.43 GHz. At 7.81 GHz frequency ($V_{\text{tune}} = 0.51$ V), the maximum gain of 10.29 dB is obtained. The return loss $S_{11}$ is $-20.88$ dB at the same operating point.

It is observed from the noise figure vs frequency graph (Figure 13A) that, for a tuning voltage of 0.54 V, noise figure achieved a maximum value. The noise figure declines when $V_{\text{tune}}$ decreases and becomes minimum at $V_{\text{tune}} = 0.48$ V. In other words, the higher the value of center frequency, the greater the noise figure. However, a significant amount of noise figure can be observed. This is due to the presence of the active elements in the circuit. From the graph of DC power consumption vs tuning voltage (Figure 13B), we can perceive that consumed power is inversely proportional to the tuning voltage as the tuning is implemented in PMOS. At the lowest tuning voltage of 0.48 V, power consumption achieves the highest value and the raise of tuning voltage results decay in power consumption. The output power vs input power depicted in Figure 14A, and Figure 14B shows the input-referred 1-dB compression point is $-12.598$ dBm and the third-order intercept point is $-19.87$ dBm. The simulation is done considering the center frequency of 7.81 GHz ($V_{\text{tune}} = 0.51$ V).

#### 4.3.2 Tuning of center frequency by $C_{\text{tune}}$

The parallel capacitor across $C_{gs2}$, $C_{\text{tune}}$ was altered from 1 to 13 fF with a step of 3 fF. As $C_{\text{tune}}$ is in parallel with $C_{gs2}$, increased $C_{\text{tune}}$ contributes as an additive to $C_{gs2}$. It reasons to rise the inductance $L$ [as $L = \frac{C_{gs2}(1+R_{f2}R_{d2})}{\text{f_{out}R_{d2}}}$] and finally declines the center frequency [as $f_o = \frac{1}{2\pi \sqrt{LC}}$]. Table 7 shows the basic performance parameters of the BPF when tuning of center frequency was applied through $C_{\text{tune}}$. During this time, $V_{\text{tune}}$ was kept at 0.515 V.
FIGURE 13 Tuning of center frequency by $V_{tune}$: A, noise figure vs frequency, and B, DC power consumption vs tuning voltage.

FIGURE 14 Determination of, A, 1-dB compression point, and B, third order intercept point (IP3).

| $C_{tune}$ (fF) | Center freq., $f_o$ (GHz) | $S21 @ f_o$ (dB) | $S11 @ f_o$ (dB) | DC power con. (mW) | Noise figure @ $f_o$ (dB) |
|----------------|--------------------------|------------------|------------------|-------------------|--------------------------|
| 1              | 7.64                     | 10.31            | −20.63           | 2.40              | 23.39                    |
| 4              | 7.47                     | 9.93             | −21.38           | 2.40              | 22.96                    |
| 7              | 7.32                     | 9.31             | −23.03           | 2.40              | 22.58                    |
| 10             | 7.18                     | 8.58             | −25.09           | 2.40              | 22.24                    |
| 13             | 7.06                     | 7.82             | −27.74           | 2.40              | 21.93                    |

The capacitive tuning outputs the variation of center frequency from 7.64 to 7.06 GHz. Figure 15A illustrates that when $C_{tune}$ rises, the center frequency decreases as per the explanation shown above. From Figure 15A,B, we can also conclude that when $S21$ is in maximum $S11$ is minimum. It is clear from the table that power consumption has a fixed value. This is because capacitive tuning draws no additional power from the supply.

From the noise figure vs frequency (Figure 16A), it can be comprehended that as the capacitance increases and noise figure decreases. For 13 fF of $C_{tune}$, the noise figure is least, showing the best performance. It is visible from the output power vs input power graph (Figure 16B,C) that 1-dB compression point and the third-order intercept points are −40.17 and −19.68 dBm, respectively. The simulation is done considering the center frequency of 7.32 GHz ($C_{tune} = 7$ fF).
**FIGURE 15** Tuning of center frequency by $C_{\text{tune}}$: A, $S_21$ vs frequency, and B, $S_11$ vs frequency.

**FIGURE 16** Tuning of center frequency by $C_{\text{tune}}$: A, noise figure vs frequency, B, 1-dB compression point, and C, third-order intercept point (Ip3).
4.3.3 | Process corner analysis

The process corner analysis had been carried out by deeming $C_{\text{tune}} = 1$ fF and $V_{\text{tune}} = 0.515$ V. The performance parameters for all corners are tabulated in Table 8. Figure 17A,B demonstrates $S_{21}$ and noise figure with respect to frequency. To illustrate how power consumption behaves to all corners, $V_{\text{tune}}$ was varied. The result is displayed in Figure 17C. FF consumes maximum power while SS dissipates the least power from the $V_{DD}$.

4.3.4 | Temperature sweep analysis

Temperature sweep analysis had been conducted by setting the same value of $C_{\text{tune}}$ and $V_{\text{tune}}$ as in the process corner analysis. Five different temperatures were chosen from $-50^\circ$C to $50^\circ$C with $25^\circ$C interval. The performance parameters for all temperatures are summarized in Table 9. Figure 18A,B demonstrates $S_{21}$ and noise figure with respect to frequency.

### Table 8
Data table and comments for process corner analysis of BPF

| Corners | Center freq., $f_o$ (GHz) | $S_{21}$ @ $f_o$ (dB) | $S_{11}$ @ $f_o$ (dB) | Noise figure @ $f_o$ (dB) | Comments |
|---------|---------------------------|-----------------------|-----------------------|---------------------------|----------|
| SS      | 5.27                      | 3.37                  | -23.71                | 23.77                     | Though FF corner is good for high $f_o$ and gain, return loss is too high. However, FS corner shows the perfect balance among all. |
| SF      | 7.36                      | -3.626                | -25.79                | 22.37                     |          |
| FS      | 6.86                      | 10.03                 | -17.14                | 24.84                     |          |
| FF      | 10.01                     | 22.05                 | -4.08                 | 23.63                     |          |

![Figure 17](image1.png)  
**Figure 17** Process corner analysis: A, $S_{21}$ vs frequency for four corners of the BPF, B, noise figure vs frequency, and C, DC power consumption vs tuning voltage for four corners.
TABLE 9  Data table and comments for temperature sweep analysis of BPF

| Temp   | Center freq., $f_o$ (GHz) | S21 @ $f_o$ (dB) | S11 @ $f_o$ (dB) | Noise figure @ $f_o$ (dB) | Comments                                                                 |
|--------|---------------------------|------------------|------------------|---------------------------|-------------------------------------------------------------------------|
| −50°C  | 9.80                      | 21.14            | −4.076           | 21.65                      | Lower temperature is beneficial to achieve gain with higher center frequency however, not to return loss. Noise figure increases with temperature. |
| −25°C  | 8.99                      | 17.51            | −8.717           | 22.25                      |                                                                         |
| 0°C    | 8.29                      | 13.99            | −13.87           | 22.82                      |                                                                         |
| 25°C   | 7.68                      | 10.58            | −20.01           | 23.35                      |                                                                         |
| 50°C   | 7.14                      | 7.323            | −28.49           | 23.82                      |                                                                         |

Now, in terms of DC power consumption (depicted in Figure 18C), the increment of temperature is favorable to this parameter.

4.3.5 Monte Carlo analysis

The Monte Carlo analysis of the proposed design had been performed for both process variation and mismatch cases simultaneously for $C_{tune} = 1$ fF and $V_{tune} = 0.515$ V. Figure 19 shows the statistical presentation of Monte Carlo Simulation results for S21, center frequency, and DC power consumption. The S21 has a mean of 10.41 dB with an SD of 1.44 dB, where for the case of center frequency, they are 7.63 GHz (mean) and 0.1 GHz (SD). 2.39 mW is a mean value for DC power consumption with a low SD of 34.21 μW. Finally, Figure 20 depicts the layout representation of the proposed design after the insertion of it into pad frame.

Table 10 summarizes the performance for the BPF and comparison with other reported designs.
FIGURE 19  Monte Carlo analysis: statistical distribution of, A, S21, B, center frequency, and C, DC power consumption for $C_{tune} = 1$ fF and $V_{tune} = 0.515$ V

FIGURE 20  Insertion of layout in pad frame
TABLE 10 Performance comparison of the BPF with other published designs

| References | 26 | 27 | 28 | 29 | 30 | This work |
|------------|----|----|----|----|----|-----------|
| Technology | 45 nm CMOS | 180 nm CMOS | 40 nm CMOS | 90 nm CMOS | 90 nm CMOS | 90 nm CMOS |
| Filter order | 2 | 2 | 8 | 2 | 4 | 2 |
| $V_{DD}$ (V) | ±1 | — | 25.5 | 37.8 | 77.5 | 0.55 |
| Power (mW) | 0.614 | 25.5 | 37.8 | 77.5 | 0.55 |
| Center frequency (GHz) | 4.06 | 0.76~0.86 | 0.085~0.225 | 0.8~6 | 3.1~10.6 | 7.08~8.43 |
| $S21 @ f_o$ GHz | — | 6.5~18.1 | 0~20 | 16 @ 1.23 | — | 10.29 @ 7.81 |
| $NF @ f_o$ GHz | 31.34 | 34~55 | — | — | — | 23.42 |
| 1 dB comp. Point (dBm) | ~3.1 | — | +12 | — | — | −12.598 |
| Layout area ($\mu m^2$) | 1373.775 | — | 610 × 530 | — | — | 1215.6 (VCO + BPF) |

5 JUSTIFICATION AND OUTCOMES OF THE PROPOSED DESIGN

Here in this research, a novel technique is discussed. It is component sharing, that is, sharing a particular portion of the circuit for distinct purposes. The AI portions are utilized as both VCO and BPFs. So, the outcome is using the same IC AI can be implemented for two distinct applications through changing the modes of operation. Despite the simplicity of switching technique, it has an outstanding significance in the analog domain.

Second, another achievement is the implementation of AIs and its tuning ability. Most often, additional varactors are employed for tuning purposes. Now, if the spiral inductor is used, it would consume a significant chip area as it is a bulky element. In general, a passive inductor cannot be made tunable. To do it, we have to change its hardware configuration, that is, coil length, coil area, or core material. So, the addition of variable capacitors is to be needed to tune the frequency (for VCO it is oscillation frequency and for BPF it is center frequency). So, this technique requires additional area. Both of these situations are ruled out by exploiting the AI, which reduces the silicon area consumption significantly. For more rigorous realization, Table 11 given below compares the area consumed by spiral inductor based RFICs and our proposed design.

Finally, the applications of the proposed design can be mentioned. The VCO generates oscillation frequency from 1.93 to 6.22 GHz. The applications within the frequency range are tabulated (Table 12) below.

Likewise, the center frequency of the BPF is regulated from 7.08 to 8.43 GHz, which falls within the X band frequency range. The applications of this frequency band are radar technology, wireless networks, satellite communication, and so on.

TABLE 11 Area comparison of the proposed with other published designs

| References | Proposed circuit | Area consumption | Proposed design |
|------------|------------------|------------------|-----------------|
| 31         | VCO              | 193 $\mu m \times 243 \mu m = 46,899 \mu m^2$ | $60 \mu m \times 20.26 \mu m = 1,215.6 \mu m^2$ (VCO + BPF) Significantly low area consumption with respect to referred spiral/passive inductor based published works. |
| 32         | VCO              | 860 $\mu m \times 390 \mu m = 335,400 \mu m^2$ |                 |
| 33         | VCO              | 134 $\mu m \times 237 \mu m = 31,758 \mu m^2$ |                 |
| 34         | BPF              | 530 $\mu m \times 700 \mu m = 371,000 \mu m^2$ |                 |

TABLE 12 Applicable areas of the frequency generated by VCO

| Protocol | Frequency | Applications |
|----------|-----------|--------------|
| IEEE 802.11b/g | 2.4 GHz | Microwave ovens, Bluetooth applications, wireless telephones, wireless routers. |
| IEEE 802.11y | 3.7 GHz | Municipal Wi-Fi networks, networking, automation in industry, safety and security networks, wireless communication. |
| IEEE 802.11a/ac | 5 GHz | Wireless LANs, high speed wireless communication. |
| IEEE 802.11n | 2.4/5 GHz | Dual band wireless router, high throughput and secured wireless communication. |
| IEEE 802.11ax | 2.4/5/6 GHz | High frequency cellular communication, improved power management. |
6 | CONCLUSION

A tunable AI-based VCO and BPFs on a single integrated design through component sharing method have been proposed in the research article. An SPDT switching system is presented, which cooperates to change the modes of operation. As a VCO, it exhibits a tuning range from 1.93 to 6.22 GHz, and the power consumption is 1.83 ~ 3.84 mW. The phase noise varies from −81.32 to −76.89 dBc/Hz, and the FOM changes from −144.42 to −149.34 dBc/Hz. As a BPF, the voltage tuning yields center frequency of 8.43 ~ 7.08 GHz, and obtained maximum gain is 10.29 dB at 7.81 GHz. The center frequency can also be regulated through capacitive tuning (7.64 ~ 7.06 GHz). The proposed design consumes a layout area of 1215.6 μm². To check how the proposed design behaves in multifarious environments, this design has been passed through process corner analysis, temperature sweep analysis, and Monte Carlo analysis for both VCO and BPF individually. Implementation of AI based VCO and BPFs enables the reduction of noteworthy silicon area consumption, which is justified through fair comparison with other literature reviews. This technique of component-sharing will benefit future researchers to incorporate a particular component-based distinctly functioned IC.

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CONFLICT OF INTEREST

The authors declare no potential conflict of interest.

AUTHOR CONTRIBUTIONS

Omar Faruqe contributed to conceptualization-lead, data curation-lead, formal analysis-lead, investigation-lead, methodology-lead, resources-lead, software-lead, validation-lead, writing-original draft-lead, writing-review and editing-lead. Aniqa Ibna Lim contributed to validation-equal, writing-original draft-equal. Md Tawfiq Amin contributed to conceptualization-equal, supervision-equal, validation-equal, writing-review and editing-equal.

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