Designing of input/output port based on FPGA with handshaking capability

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Abstract. Input/output (I/O) port is a group of interfaces that has diverse functional structures of a data processing system to interconnect with each other. I/O port with handshaking capability is one of the powerful configurations to enable digital communication. The main intention of this project is to design prototype of an input/output port with handshaking capability using Field Programmable Gate Array (FPGA). The main reason of using the FPGA technology is it has unlimited number reprogrammed, cuts developing cost and development time. Xilinx Foundation 2.1i Series software in VHDL description was used as a development tool in this project. The VHDL codes were assimilated into a design and development atmosphere to accomplish many subtasks such as FPGA synthesis, optimization, placement, and routing. The successful design was translated, mapped, routed, and placed onto FPGA Demo Board. XC4010XLPC84 Xilinx FPGA from XC4000XL family was used as a target board. In prototype design, the FPGA pins were connected to a parallel printer port by using a coupled 25-pin DB connector, with a 36-pin Centronics connector cable. The output signals were observed and analyzed by using a logic analyzer.

1. Introduction
One of the operations that occurs in digital systems is the transmission of information from one device to another device. In computer, these transmissions of data are important because the computer can communicate with external peripherals such as keyboards, monitors, and printers. For instance, keypads or keyboards are considered as the input peripherals. Instead, monitors and printers are considered as the output devices of a computer. The classic devices for communication between computers are for both input and output, for example modems and network cards. All of the above peripherals communicate with the microcontroller by attaching them to the Input/output (I/O) ports. For instance, the 8051 microcontroller comprises four 8-bit I/O ports named P0, P1, P2, and P3. For some microcontrollers, the commands of the I/O port lines are reprogrammable so that different bits of a port can be set as inputs or outputs. In addition, microcontrollers also deliver bi-directional I/O ports. For each I/O port line of this microcontrollers can be used as inputs and otherwise outputs.

There are various types of I/O port functional configuration that are available, which can handle different characteristics of devices. There are three main configurations of I/O mode, which are simple I/O, bidirectional mode and handshaking I/O configuration. In the simple mode, each I/O port can be
configured to act as an I/O. The output ports are used to transmit signals such as control signals from a host to other peripheral devices. Meanwhile, the input ports received signals such as the status signals from other peripheral devices to a host. On the other hand, the bidirectional I/O port can provide communications with a peripheral device for both transferring and getting information. The handshaking configurations are means for transmitting I/O data to or from a precise port in combination with strobe or acknowledged signals.

However, there are limited numbers of input/output ports provided by the microcontroller. Thus, one way to overcome this problem is through expanding the input/output ports of the microcontroller by connecting them to external input/output chip. The most widely used I/O chip for interfacing peripheral equipment to the microcomputer system is 8255 chip. The PPI has 8-bit ports, which may be configured in three ways of modes. The three elementary modes of operation that can be designated are Basic I/O (mode 0), Strobed I/O (mode 1), and Bi-directional Bus (mode 2).

Handshaking refers to the signalling that occurs between two systems as one transfer data to the others with strobe and acknowledge signals. Generally, when a system wants to transfer data to another system, the sending system must inform the receiving system that the data are ready. In microcontroller, it is done by sending a signal named STROBE*. A low signal of strobe indicates that there are data to be sent. When the receiving system completely accepts the data, it informs the sender by activating a signal ACK*. Low pulses of this signal initiates the process that sends another byte of data to the receiver. Figure 1 shows the timing diagram characteristics of handshaking process.

![Figure 1. The timing diagram of handshaking process](image)

2. Field Programmable Gate Array

2.1. FPGA Based Design

In this project, an I/O port with handshaking capability is designed by using Field Programmable Gate Array (FPGA) technology. The I/O port design can provide handshaking communication between a FPGA device and a peripheral device such as a parallel port printer. The FPGA contains an array of combinational logic circuits, flip-flops, and on-chip memory that can be programmed to implement any logic circuit.

FPGAs have been widely used as one of implementation technologies for digital system design [1], [2]. Previous researches, have shown by using the FPGAs in digital systems provided flexibility, reliability, low cost, fast time-to-market, and long term maintenance [3], [4]. The findings from a research showed that FPGA architecture is capable of execution fast parallel co-occurrence matrix computable [5]. The main benefits of using FPGA are the ability to reprogrammable and can produce provable solution at lower cost [6], [7], [8].

FPGAs are becoming more and more common and used in countless applications. However, the current market now is mainly dominated by advances ASICs technology. The benefit of using ASIC, power consumption is far less than FPGA power consumption [9]. As a conclusion, FPGA technology offers a great flexibility in designing any prototype of digital system. Xilinx demo board contains XC4010XLPC8 FPGA chip from XC4000XL FPGA family that is used as a target board. The
Hardware design is supported by Xilinx Foundation series 2.1i software design environment. This software is used as a tool to design, synthesize, and simulate the digital system design. In addition, the reports generated by the synthesis tool help to acquire the particular designs concerning overhead area, speed of operation, and critical path [10].

2.2. The Objective of Project
In this project, I/O port design has to be implemented by using FPGAs to support the strobed or handshaking signals. Essentially, the I/O port transferred I/O data to or from the port in conjunction with handshaking signals. The handshaking structure delivered a great degree of flexibility and trustworthiness because the successful completion of a data transfer relied on the dynamic contribution by both units [11]. All designs had to use a CAD tool that supported the FPGAs.

In the handshaking configurations, there are three main types of signals involved, they are status signals, control signals and data signals. The control signals were used to control the handshaking operation. The peripheral sent the status signals to reply the host request or acknowledge the handshaking operation. The data lines consisted of information that had to be transferred to other parties. Printer is one example of peripheral devices that uses the handshaking signal.

The main objective of this project is to design a FPGA based prototype of an input/output port. The I/O port can provide an interface with other peripheral that needs handshaking operations such as a printer. The design was implemented by using FPGA chip. FPGA was chosen as the medium to develop the prototype as it is cost effective due to its programmability advantage. This project was also carried out to test the ability of the Xilinx FPGA chip.

In this project, the prototype was implemented on a Xilinx XC4010XLPC84 demo board. The Xilinx FPGA chip is from XC4000 family that contains 10,000 gates. The I/O port design was developed in VHDL based and schematic environment by using Xilinx Foundation Series 2.1i software. The outputs were subsequently observed and analysed using a logic analyser to verify the functionality of the I/O port.

3. Methodology
The real time of handshaking timing diagram between a printer and computer was observed by using a logic analyser. The characteristic of I/O port output signals were analysed. The I/O port handshaking unit was designed by using Xilinx Foundation 2.1i software. There were two modes of design entry used in this project, which were VHDL and schematic. The top down method was used to design the I/O port because it gives more flexibility in designing process. The design then was translated into VHDL code and schematic. VHDL language was used as the designing tool because it is synonym with the top down method. After the design was successfully drawn, it was then synthesized. The verification of design was done through functional and timing simulation process. Here, the simulations results were analysed to ensure that the design met the requirement as input/output port with handshaking capability.

Upon the success of the simulated results, the design was implemented on Xilinx XC4010XL84 demo board. A parallel printer port was used to operate as an example of peripheral that can communicate through input/output port design with handshaking capability. Again, the throughputs of input/output port were observed again by using the logic analyser. The output waveforms were analysed to make sure that design met the desired requirements. Figure 1.2 shows the project flow in designing an I/O port.

Figure 2 shows the block diagram for setup I/O port design. A logic analyser was used to display the outputs. A functional generator was used to provide a clock signal with frequency 125Hz.
Figure 2. The block diagram for I/O port setup

Figure 3 shows the FPGA demo board occupied XC4010XL Xilinx FPGA chip and an UV-EPROM chip. The FPGA chip had some of its pins connected to the UV-EPROM. The hex file was downloaded to FPGA via the UV-EPROM chip each time when the power supply was on. 7 inputs and 17 outputs FPGA pins were used to connect I/O parallel printer port. A centronic connector complimented with 25-pin DB connector cable was used as connection cable between the parallel printer ports with FPGA pins. LEDs were used as indicator for status signals.

Figure 3. FPGA Demo Board that occupied gate XC4010XL84 and UV-EPROM

The FPGA reset itself after the power was being applied. Then it read the configuration data from the UV-EPROM by supplying a sequence of addresses to the UV-EPROM inputs and storing the UV-EPROM output data in the FPGA configuration of memory cells. The Chip Max Programmer was used to download data stream file into EPROM and meanwhile the UV-ERASER was used to erase the EPROM content. Then, the logic analyser was set up. There were 16 pod probes of the analyser connected to the specific pin on the FPGA.

4. Result and discussion
The functional simulation was performed on schematic-based and HDL-based after the synthesis process. It only gave logical functional results without considering any delay implementation. The timing simulation is an important tool to verify whether the design will meet the real time requirement. The timing simulation results show that the design outputs closely matched the actual device operation.

The stimulators signals were used to stimulate the input ports with binary logic levels to analyse the response on the output ports. The simulation process was done in Waveform Viewer window. In this project, both functional and timing simulations were executed by using Logic Simulator. In this
section, the simulation results of using Logic Simulator in Xilinx Foundation 2.1 series of softwares are shown and discussed. The I/O port output signals were observed by using a logic analyser. All figures in this section are observed from I/O parallel port.

Figure 4 shows the clock signal on pod 15. The signal shows the clock signal period is 8.009ms, which is equivalent to frequency 125Hz. The clock signal synchronized the handshaking process.

Figure 4. Clock pin on pod 15

Figure 5 shows the output signals captured by logic analyser. The status pins (ACK, BUSY, FAULT, SELECT1 and, PERROR) gave signal response when the inputs signals were sent to I/O port printer. This shows the handshaking process occurred between the FPGA and the printer port. However, the printer was not operating as expected.

Figure 5. I/O port output signals

Figure 6 shows the handshaking operation between the BUSY pin and STROBE pin. The STROBE pulse width is 7.9ms, which is the same with the STROBE width pulse in Figure 3.8 in chapter 3. The BUSY signal was raised to HIGH logic when a STROBE pulse occurred. However, the BUSY pulse width (8ms) was not equivalent with BUSY pulse width in Figure 3.6 in Chapter 3. Meanwhile, the ACK signal response is shown in Figure 7. ACK signal is low after certain period indicates that the
printer has received the data inputs. This operation indicates that the printer was ready to receive another byte of data.

Figure 8 shows the delay that occurred in this design. The DATA lines should trigger to HIGH state when the CLK signal is positively triggered. However, the DATA lines are raised to HIGH logic after 24.20ms. This is not a good practice in handshaking process. The signals design should give response in minimum delay. These delays created problem in the handshaking processes. Thus, this problem gave effects to I/O port operation.

In this chapter, the results from the simulation using Logic Stimulator of the designed input/output port are analyzed to verify its operation according to the theory and algorithm. The Simulation process included the functional simulation and timing simulation.

After the design was successfully synthesized, simulated, and implemented, then the design was tested on FPGA chip. After running all the processes, it generated the bit pattern to program the FPGA. Then, the bit pattern was downloaded into the internal configuration memory cells in the FPGA to test the operations of the FPGA. The bit pattern for programming the FPGA was stored in the UV-EPROM and automatically loaded into the FPGA when the power was turned on.

The functional generator supplied the clock input with frequency 125Hz. Logic analyzer was used to capture the output signals. Then, the system outputs were observed and analyzed. The implementation result shows that I/O port can operate in handshaking operation. There were response signals on status pin when the input signals were sent to the printer port. However, the printer did not perform the printing job. This was because the input signals from FPGA pins were not compatible with the real protocol printer signals. The delay implementation also gave problems to I/O port design.

5. Conclusion
This project was carried out to design an input/output port with handshaking capability. The design of input/output port can provide a communication between a device and other peripheral devices using the handshaking signals. The input/output port was designed based on FPGA technology. In this project, the XC4010XL84 FPGA chip is used as the target board. A parallel port printer was used as peripherals to print one character. The I/O port can support handshaking signals such as to request and reply signals. Meanwhile, architecture of input/output port is designed using combination VHDL code and schematics. VHDL was chosen for this project, because of its device has independent characteristic and gives more flexibility in designing logic systems. The Foundations Series 2.1i software is used as a tool to design all characteristics of the input/output port design. Xilinx Foundation 2.1i software is used to write the VHDL codes, synthesis, simulation, and implementation process.
The implementation result shows that there are handshaking process occurred in the design. The status signal (ACK, BUSY, PERROR, FAULT and SELECTI) gave response when there were inputs signals. However, the printer did not perform the printing job. This is because the input signals sent by FPGA pins were not compatible with the real protocol signals for this printer. Moreover, the real handshaking timing diagram observed using logic analyzer might not precise with the actual signals. The delay implementation also gave effects to the I/O port design.

In conclusion, the objective of the project which is to design an input/output port based on FPGA, has been achieved. The research work also proved that FPGA can provide good performance, low power, and also save circuit board area. The flexibility of FPGA in this application allowed the rapid design adjustments to surge the required performance or functional modification. However, FPGAs loose their functionality when the power is turned off. The program has to re-download again into FPGA board when the power is on. The research work also proved that in designing a digital system prototype, FPGA can provide great performance, low power, and also save circuit size.

6. References

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