Realization of the FPGA-based reconfigurable computing environment by the example of morphological processing of a grayscale image

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Abstract. Currently, robots are increasingly being used in every industry. One of the most high-tech areas is creation of completely autonomous robotic devices including vehicles. The results of various global research prove the efficiency of vision systems in autonomous robotic devices. However, the use of these systems is limited because of the computational and energy resources available in the robot device. The paper describes the results of applying the original approach for image processing on reconfigurable computing environments by the example of morphological operations over grayscale images. This approach is prospective for realizing complex image processing algorithms and real-time image analysis in autonomous robotic devices.

1. Introduction
The ubiquitous introduction of information systems in the technological process control requires higher accuracy and operation speed of individual subsystems. As an example, we can take a wide class of data processing tasks generated by a vision system (VS), which provides control and management of technological operations. One of the main data operation is filtering and selection of areas of interest on each frame of the video stream.

The classical processing method implies transfer of scenes digitized by photosensitive matrices to a computer system that performs certain operations in the context of the problem being solved. In this connection, two approaches are used to increase the operation speed:
• increase of the computer system performance;
• improvement and optimization of the algorithms used.

The weak point of this method is serial transfer of information about each pixel of the image from the sensitive matrix to the computer system, which is a constraint that restrains achievement of the greatest performance.

The alternative approach proposed in [1] consists in direct combining sensory (photosensitive matrix) and computational (specialized homogeneous structure) systems in the form of separate layers on a single semiconductor crystal. This will allow transferring data from each matrix sensor to a separate structure calculator, which should lead to a significant increase in the system performance [2]. The main advantages of the approach include the following:
• information from each matrix sensor is processed by a separate calculator, which implies a high degree of parallelism in image processing;
• the speed of such a system does not depend on the number of sensors; it is possible to effectively scale the system without significant loss of speed, which is a weak point in systems with serial data processing.
Within our project, the homogeneous FPGA-based computing structure for morphological processing of grayscale images was realized.

2. Homogeneous computing structure for image processing
The homogeneous structure under consideration is a reconfigurable computing environment (RCE, homogeneous environment) representing a geometrically regular lattice with at least two symmetry axes (Figure 1) and single-type functional cells (calculators) at the nodes. Each functional cell is connected to neighboring cells geometrically in the same way and can be configured to perform a specific signal processing function at a given time. A signal from any cell $A$ can be transmitted to any cell $B$ of the environment (at least by means of other cells). This homogeneous medium is isotropic, which allows realizing any given function in any part or region of the environment [2].

![Figure 1. Reconfigurable computing environment.](image1)

Each calculator has a specialized structure (Figure 2) and serves to process information about one pixel of the image in the streaming mode. It allows avoiding overhead costs for intermediate transformations and serial data transmission, which are typical of the classical approach. Each calculator receives signals from neighboring calculators and from its “own” sensor of the photosensitive matrix and transmits the output signal to the neighboring calculators and the corresponding pixel of the resulting image. The operating mode of a specific calculator is set by the configurable signal, which allows it dynamic adjusting and influencing the overall processing process.

![Figure 2. Elementary calculator.](image2)
A mathematical apparatus has been developed for implementing the basic morphological operations on binary and grayscale images. Mathematical morphology allows extracting certain image components to represent and describe the shapes of objects. In morphological processing, a binary image represents a set of pixels of the foreground and background; therefore, operations performed on sets can also be performed on images.

Dilation (expansion), erosion (compression), opening and closing are the basic operations in morphological image processing. They are performed on two images: the image being processed and a special image depending on the type of operation and the task being solved. A special image is called a structural element or a mask. A mask is a matrix with a central element (i.e. with an odd number of rows and columns), which defines the form of image processing. A key element is set for each mask; the central element often becomes a key element. In this approach, only the simplest 3x3 structural element is used, all cells of which are filled with “1”.

Morphological operations realized by the calculator include dilation and erosion. More complex operations (for example, opening and closing) can be performed through the implementation of a multilayer computational structure (Figure 3), or through the implementation of push-pull processing, in which the result of one operation is fed to the input of the same calculator, but the calculator itself is tuned to performing another operation.

![Figure 3. Multilayer computing structure.](image)

This device is sufficient for the image pre-processing (reducing noise, smoothing contours, removing “gaps”, and detecting zones of interest) [3]. Because the processing of grayscale and full-color images will be performed according to the similar algorithms, you will only need to scale the structure for processing a larger data stream.

Because the morphological operations are essentially spatial filters, when processing the boundary pixels of the image, the problem of missing pixels occurs. This problem is solved by introducing a tuning signal. This signal allows encoding one of nine possible states of the neighborhood of the pixel being processed (for a 3x3 mask) including four angular, four edge and one not boundary state. In addition, this signal determines the operation performed by the computing element [1, 4, 5].

3. Selection of a hardware platform for the computational structure implementation

A single element of such a computational structure can be effectively implemented using field programmable gate array (FPGA). The choice of FPGA as a hardware platform is connected with the following factors.

• Similarity. The FPGA structure is similar to the homogeneous environment being implemented; the FPGA structure is a homogeneous matrix of programmable logic blocks connected by programmable internal connections. By recording the operations of morphological processing considered in this task in the form of logical operations, it is possible to implement the logic of calculators and connections between them based on FPGA.
• Parallelism. Logical blocks and their unions do not depend directly on each other; it allows implementing a large number of parallel computational elements on one circuit.

• Reconfigurability. Based on FPGA, it is possible to implement reconfigurable computing structures that can effectively solve complex technical problems.

• High operating speed. At the execution stage, FPGA is a certain digital device, which generally does not read commands and data from the memory, therefore the operating speed of the resulting device depends only on the actuation of logic keys and parasitic reactive processes, which provides high performance and wide optimization possibilities.

• Flexibility. FPGAs have a large number of possible rewriting cycles, which allows quick required correction of the existing configuration and continuation of operation.

• Accessibility and convenience.

As a design environment for the FPGA, we selected Quartus II 13.0 Web Edition, the simulation environment was Altera ModelSim 10.1, the language was Verilog HDL, and a programmable logic device (PLD) was Cyclone IV (EP4CGX110DF31C7).

4. Results
The first step in solving the problem was implementation of a separate pixel-processing calculator for a grayscale image in accordance with the basic operations of morphological processing. This calculator was implemented based on the research [4]. The key difference is processing of not single signals, but 8-bit buses (8-bit numbers), and complication of the logic of the morphological operations (the dilation operation corresponds to the maximum of the current neighborhood and the erosion operation corresponds to the minimum).

Using the module generating function of the Verilog language, a 100×100 matrix and all necessary connections between the elements were obtained. The initial image is loaded as a 100x100x8 bus (length, width, bit width) of binary signals using the $readmemh command. In this regard, the initial image must be a two-dimensional array, each element of which is an 8-bit luminance value of the corresponding pixel. In this format, images with the extension .pgm (portable grayscale map) are represented.

To simulate the resulting computational structure, a grayscale image of 100×100 pixels was selected as shown in Figure 4. For later processing, it was converted to pgm format followed by deleting the file metadata. The resulting image was processed using the obtained computing environment in the simulation mode. Figures 5, 6 show the results of dilation and erosion. Analysis of the timing diagram of the simulation in Quartus showed that the formation of the resulting image requires no more than 21 nanoseconds from the moment of the signal change at the input of the computing environment.

Figure 4. Initial image.
5. Conclusion
Solution of this problem resulted in implementation of a computer system based on RCE processing of arbitrary sized grayscale images. This FPGA-based computer system is well scalable and allows efficient parallelization of the spatial image processing process between simple calculators performing basic operations of mathematical morphology. Simulation of processing of a grayscale 100×100 pixels 8-bit image was performed in Quartus II 13 environment using the ModelSim 10 simulator. Analysis of the obtained results showed that the implemented structure solved the task correctly and required no more than 21 nanoseconds for forming the resulting image when simulating for FPGA Altera Cyclone IV (EP4CGX110DF31C7).

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