Rate-Flexible Fast Polar Decoders

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Abstract—Polar codes have gained extensive attention during the past few years and recently they have been selected for the next generation of wireless communications standards (5G). Successive-cancellation-based (SC-based) decoders, such as SC list (SCL) and SC flip (SCF), provide a reasonable error performance for polar codes at the cost of low decoding speed. Fast SC-based decoders, such as Fast-SSC, Fast-SSCL, and Fast-SSCF, identify the special constituent codes in a polar code graph off-line, produce a list of operations, store the list in memory, and feed the list to the decoder to decode the constituent codes in order efficiently, thus increasing the decoding speed. However, the list of operations is dependent on the code rate and as the rate changes, a new list is produced, making fast SC-based decoders not rate-flexible. In this paper, we propose a completely rate-flexible fast SC-based decoder in this paper is only 38% of the total area of the memory-based base-line decoder when 5G code rates are supported.

Index Terms—polar codes, successive-cancellation decoding, list decoding, hardware implementation.

I. INTRODUCTION

Polar codes are a family of channel codes which can provably achieve the capacity of a binary memoryless symmetric (BMS) channel with the low-complexity successive-cancellation (SC) decoding algorithm [1]. However, this capacity-achieving property under SC decoding only occurs as the code length tends towards infinity. For practical values of code length, SC decoding fails to provide a reasonable error-correction performance.

In order to improve the error-correction performance of SC decoding, SC list (SCL) [2] and SC flip (SCF) [3] decoders run multiple SC decoders in parallel and in series, respectively. Therefore, SCL improves the error-correction performance of SC at the cost of higher area occupation when implemented on hardware, while SCF improves the error-correction performance of SC at the cost of higher latency and lower throughput. With this error-correction performance improvement, polar codes were selected as a channel coding scheme for the enhanced mobile broadband (eMBB) control channel in the next generation of wireless communications standard (5G).

SC-based decoding algorithms such as SC, SCL, and SCF, suffer from high latency and low throughput when implemented on hardware. This is due to the serial nature of SC decoding in which the decoding proceeds bit by bit. In order to address this issue, polar codes where shown to be a concatenation of smaller constituent codes which can be decoded in parallel [4], [5]. These constituent codes are shown to add small implementation complexity overhead while keeping the error-correction performance of SC unchanged. In [6], more constituent codes were identified and low-complexity parallel decoders were designed to increase the throughput of SC decoders even further. It was shown in [7], [8] that the constituent codes can be decoded efficiently under SCL decoding while keeping the error-correction performance of SCL decoder unaltered. The same approach was applied to the SCF decoder in [9].

The construction of polar codes is based on the identification of reliable bit-channels through which information bits are transmitted. The remaining bit-channels carry fix values and are called frozen bits. The location of the frozen bits and of the information bits is known to the encoder and the decoder. In SC-based decoders, the frozen and information bit sequence can be either stored in a memory, or computed on-line given the bit-channel relative reliability vector and desired code rate, as proposed in [10]. In fact, the latter approach is significantly more efficient in case of multi-code decoders, and is facilitated by nested reliability vectors as those selected for the 5G eMBB control channel [11]. Therefore, in 5G, the polar encoder and decoder are provided with a vector of bit indices in descending reliability order and an information length \( K \), from which the encoder and the decoder should extract the frozen/information bit sequence. It should be noted that the number of information bits for polar codes in the 5G eMBB control channel can be any value between 12 and 1706 [12]. Thus, the encoder and the decoder should be able to support a vast range of code rates.

Fast SC-based decoders rely on the identification of the type and the length of constituent codes in a polar code. While the calculation of the frozen/information bit sequence is straightforward and can be performed by simply assigning information bits to the first \( K \) elements of the reliability vector, the direct calculation of the list of operations for fast SC-based decoders requires complicated controller logic [5]. Therefore, the identification of the type and the length of constituent codes is performed off-line and the decoding order is stored in a dedicated memory as a list of operations [5], [7], [8]. The decoder fetches the list of operations from memory to decode the constituent codes in order one by one. The main drawbacks of the aforementioned fast SC-based decoders are twofold:
first, the list of operations requires high memory usage when implemented on hardware. Second, the list of operations is highly dependent on the rate of the polar code and as the rate changes, the list of operations changes too. Therefore, for 5G applications which require the support of multiple rates, multiple lists of operations need to be stored in memory. This in turn increases the hardware implementation overhead and renders fast SC-based decoders not rate-flexible.

In this paper, we propose completely rate-flexible fast SC-based decoders by introducing a method to infer the list of operations directly in hardware by using the bit-channel relative reliability vector and without the need to store it in memory. We show that the type and the length of a constituent code in a polar code can be identified with low hardware implementation complexity, by checking only a few bits of the constituent code. We further show that the list of operations adapts with the rate of the code, allowing the resulting fast SC-based decoder to be completely rate-flexible.

We design and implement a hardware architecture for the proposed decoder and show that the memory required to store the list of operations can be completely removed, resulting in significantly lower decoder area occupation.

The remainder of this paper is organized as follows: Section II reviews polar codes, SC-based decoding algorithms, and their fast counterparts. We propose the rate-flexible fast decoder for polar codes in Section III. In Section IV, a hardware architecture to implement the proposed method is introduced. Section V provides the hardware implementation results and comparisons with state of the art. Finally, conclusions are drawn in Section VI.

II. PRELIMINARIES

A. Polar Codes

A polar code of length $N = 2^n$ that carries $K$ information bits has a rate $R = K/N$ and can be represented as $\mathcal{P}(N, K)$. It can be constructed using a lower-triangular generator matrix $G$ as

$$ x = uG, $$. (1)

where $x = \{x_0, x_1, \ldots, x_{N-1}\}$ is the vector of coded bits and $u = \{u_0, u_1, \ldots, u_{N-1}\}$ is the vector of input bits. The matrix $G = B_N F^\otimes n$ where $B_N$ is the bit-reversal permutation matrix, and $F^\otimes n$ is the $n$-th Kronecker product of the polarizing matrix $F = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$.

As $N$ goes toward infinity, the polarization phenomenon creates bit-channels that are either completely noisy or completely noiseless and the fraction of noiseless bit-channels equals the channel capacity. For finite practical code lengths, the polarization of bit-channels is incomplete, therefore, there are bit-channels that are partially noisy. In principle, a bit-channel relative reliability vector $v = \{v_0, v_1, \ldots, v_{N-1}\}$, where $0 \leq v_i < N$, is generated and fed into the encoder and the decoder based on the polarization phenomenon which shows the rank of each bit-channel. Thus, $v$ is a vector of integers such that if $v_i < v_j$, then bit-channel $i$ is more reliable (less noisy) than bit-channel $j$. The polar encoding process consists of the classification of the bit-channels in $u$ into two groups based on $v$: the $K$ good (more reliable) bit-channels which carry the information bits, and the $N-K$ bad (less reliable) bit-channels that are fixed to a predefined value (usually 0). This classification can be represented as a sequence of binary values $s = \{s_0, s_1, \ldots, s_{N-1}\}$ where

$$ s_i = \begin{cases} 0 & \text{if } v_i \geq K, \\ 1 & \text{if } v_i < K. \end{cases} $$ (2)

More formally, let $W$ be a BMS channel with input alphabet $X = \{0, 1\}$ and output alphabet $Y$, and let $\{W(y | x) : x \in X, y \in Y\}$ be the transition probabilities. In order to quantify the reliability of the channel $W$, we use the Bhattacharyya parameter $Z(W) \in [0, 1]$, that is defined as

$$ Z(W) = \sum_{y \in Y} \sqrt{W(y | 0)W(y | 1)}. $$ (3)

Hence, the good bit-channels are the ones that have the lowest Bhattacharyya parameter.

B. SC-Based Decoding

SC-based decoding algorithms can be represented as a depth-first binary tree search with priority to the left branches as depicted in Fig. 1. Two kinds of messages are passed between the nodes in the graph: the soft log-likelihood ratio (LLR) values $\alpha = \{a_0, a_1, \ldots, a_{2^T-1}\}$ which are passed from a parent node at level $\log_2(2^T) = t + 1$ to the child nodes at level $\log_2(2^T) = t$, and the hard bit estimates $\beta = \{\beta_0, \beta_1, \ldots, \beta_{2^T-1}\}$ which are passed from a child node at level $t$ to a parent node at level $t + 1$.

The $T = 2^t$ elements of the left child node $\alpha' = \{a'_0, a'_1, \ldots, a'_{2^t-1}\}$ can be computed by the $F_t$ function, and those of the right child node $\alpha'' = \{a''_0, a''_1, \ldots, a''_{2^t-1}\}$ can be computed by the $G_t$ function as

$$ a'_i = F_t(a_i, a_{i+T}), $$ (4)

$$ a''_i = G_t(a_i, a_{i+T}, \beta'_i), $$ (5)

where

$$ F_t(a, b) = 2 \arctan \left( \frac{\tanh \left( \frac{a}{2} \right) \tanh \left( \frac{b}{2} \right) }{1 - \tanh \left( \frac{a}{2} \right) \tanh \left( \frac{b}{2} \right) } \right), $$ (6)

$$ \approx \text{sgn}(a) \text{sgn}(b) \min(|a|, |b|), $$ (7)

$$ G_t(a, b, c) = b + (1 - 2c) a. $$ (8)

Assume that the vector of relative reliabilities of bit-channels $v$ is stored in memory and is available to the decoder. In SC
and SCF decoding algorithms, when a leaf node is reached, the $i$-th bit $\hat{u}_i$ can be estimated as

$$\hat{u}_i = \begin{cases} 0, & \text{if } v_i \geq K \text{ or } \alpha_i \geq 0, \\ 1, & \text{if } v_i < K \text{ and } \alpha_i < 0, \end{cases} \quad (9)$$

while in SCL decoding, at a leaf node we have

$$\hat{u}_i = \begin{cases} 0, & \text{if } v_i \geq K, \\ 0 \text{ and } 1, & \text{if } v_i < K. \end{cases} \quad (10)$$

As can be seen in (10), when an information bit is reached in SCL decoding, both of its possible values of 0 and 1 are considered. In order to limit the exponential growth in the complexity of the SCL decoder, at each bit estimation, only $L$ candidates are allowed to survive with the help of a path metric (PM) \cite{13}. To this end, a sorter module is used to rank the PMs of the $2L$ generated candidates and selecting $L$ of them with the best PMs. After the estimation of bits by (9) or (10), the left child and right child node messages $\beta^e = \{\beta_0^e, \beta_1^e, \ldots, \beta_{T-1}^e\}$ and $\beta^o = \{\beta_0^o, \beta_1^o, \ldots, \beta_{T-1}^o\}$ are used successively to calculate the 27 values of $\beta$ as \cite{1}

$$\beta_i = \begin{cases} \beta_i^e \oplus \beta_i^o, & \text{if } i < T, \\ \beta_{i-T}^e, & \text{otherwise}, \end{cases} \quad (11)$$

where $\oplus$ is the bitwise XOR operation.

The depth-first binary tree search of SC-based decoding algorithms can be represented by a list of operations. Let $b^i = \{b_{n-1}^i, b_{n-2}^i, \ldots, b_0^i\}$ represent the binary expansion of the integer $i$. The LLR value associated with $u_i$ can be calculated by a set of $F_i$ and $G_i$ operations as \cite{14}:

$$F_i, \quad \text{if } b_i = 0,$$

$$G_i, \quad \text{if } b_i = 1. \quad (12)$$

For example, the LLR value associated with $u_0$ in Fig. 1 can be calculated by performing $F_2$, $F_1$, and $F_0$, respectively, and the LLR value associated with $u_1$ in Fig. 1 can be calculated by performing $F_2$, $F_1$, and $G_0$, respectively. However, the calculation of the LLR value for $u_i$ can use the already calculated $F_2$ and $F_1$ operations in $u_0$. Let $M$ denote the minimum index in $b^i$ such that $b_{M}^i = 1$. It is only required to perform $F_t$ or $G_t$ operations with $t \leq M$ because for $t > M$, the LLR values are already calculated for previous bits. For example, the list of operations associated with the SC-based decoder of Fig. 1 can be represented as \{\{F_2, F_1, F_0, G_0, G_1, F_0, G_0, F_2, F_1, F_0, G_0, F_1, F_0, G_0\}\}. It should be noted that since the hard estimate operations of (9), (10), and (11) are performed right after $F_i$ or $G_i$ functions at a leaf node and in the same time step, we do not include them in the list of operations. The list of operations for SC-based decoders can be generated directly on hardware by simple bitwise operations \cite{13}, \cite{14}.

It is worth mentioning that the list of operations for SC-based decoders is fixed for all rates and thus SC-based decoders are rate-flexible. However, the number of time steps required to finish the decoding process in SC-based decoders is at least $2N - 4$. This limits the latency and throughput of polar codes when decoded by SC-based decoders.

### C. Fast SC-Based Decoding

In order to reduce the latency and increase the throughput of SC-based decoders for polar codes, special node structures are identified and the decoding is performed based on the LLR values at the intermediate levels in the SC-based decoding tree without the need of traversing it. It was shown in \cite{4}, \cite{5} that four special nodes can be decoded efficiently in fast simplified SC (Fast-SSC) decoding without traversing the tree at the special nodes. Let $v_i = \{v_{s_0}, v_{s_t}, \ldots, v_{s_{T-1}}\}$ represent a subset of $v$ and $s_t = \{s_{s_0}, s_{s_1}, \ldots, s_{s_{T-1}}\}$ represent a subset of $s$ corresponding to a node of length $T$ in a polar code decoding tree. The four special nodes are:

- **Rate-0 Node**: This node consists of only frozen bits, i.e., $v_i \geq K$ for any $i \in \{0, 1, \ldots, T - 1\}$ ($s_t = \{0, 0, \ldots, 0\}$).
- **Rate-1 Node**: This node consists of only information bits, i.e., $v_i < K$ for any $i \in \{0, 1, \ldots, T - 1\}$ ($s_t = \{1, 1, \ldots, 1\}$).
- **Repetition (Rep) Node**: This node consists of information bits except for the last bit which is an information bit, i.e., $v_{T-1} < K$ and $v_i \geq K$ for any $i \in \{0, 1, \ldots, T - 2\}$ ($s_t = \{0, 0, 0, 0\}$).
- **Single parity-check (SPC) Node**: This node consists of information bits except for the first bit which is a frozen bit, i.e., $v_0 \geq K$ and $v_i < K$ for any $i \in \{1, 2, \ldots, T - 1\}$ ($s_t = \{0, 1, 1, \ldots, 1\}$).

It was shown in \cite{7}, \cite{8} that these nodes can be decoded efficiently also in simplified SCL (SSCL), SSCL-SPC, fast SSCL (Fast-SSCL), and Fast-SSCL-SPC decoding without the need for traversing the tree. This is performed by estimating bits one by one at an intermediate level of the decoding tree, thus generating only $2L$ candidates and selecting the best $L$ from them, similar to the conventional SCL decoding process. This guarantees that the sorter module which selects the $L$ candidates out of $2L$ remains the same as the conventional SCL decoder. The method was also applied to the SCF decoder which resulted in the Fast-SSC decoder in \cite{9}. Recently, five new special nodes are observed in \cite{6} and efficient decoders that can be used in SC decoding were designed for them. These nodes are:

- **Type-I Node**: This node consists of frozen bits except for the last two bits which are information bits, i.e., $v_{T-3} < K$, $v_{T-2} < K$, and $v_i \geq K$ for any $i \in \{0, 1, \ldots, T - 3\}$ ($s_t = \{0, 0, \ldots, 0, 1, 1\}$).
- **Type-II Node**: This node consists of frozen bits except for the last three bits which are information bits, i.e., $v_{T-3} < K$, $v_{T-2} < K$, and $v_i \geq K$ for any $i \in \{0, 1, \ldots, T - 4\}$ ($s_t = \{0, 0, \ldots, 0, 1, 1, 1\}$).
- **Type-III Node**: This node consists of information bits except for the first two bits which are frozen bits, i.e., $v_0 \geq K$, $v_1 \geq K$, and $v_i < K$ for any $i \in \{2, 3, \ldots, T - 1\}$ ($s_t = \{0, 0, 1, \ldots, 1\}$).

\footnote{For SCL decoder, $K$ more time steps are needed to perform the PM computation and path pruning \cite{13}. For SCF decoder, additional rounds of SC decoding add to the number of required time steps.}
Fig. 2: Fast SC-based decoding on a binary tree for $\mathcal{P}(8,4)$ and $v = \{7, 6, 5, 3, 4, 2, 1, 0\}$ ($s = \{0, 0, 0, 1, 0, 1, 1, 1\}$).

- **Type-IV Node**: This node consists of information bits except for the first three bits which are frozen bits, i.e., $v_{t0} \geq K$, $v_{t1} \geq K$, $v_{t2} \geq K$, and $v_{t3} < K$ for any $i \in \{3, 4, \ldots, T - 1\}$ ($s_t = \{0, 0, 0, 1, 0, 1, 1, 1\}$).

- **Type-V Node**: This node consists of frozen bits except for the bits $T - 5$, $T - 3$, $T - 2$, and $T - 1$ which are information bits, i.e., $v_{tT-1} < K$, $v_{tT-2} < K$, $v_{tT-3} < K$, $v_{tT-4} \geq K$, $v_{tT-5} < K$, and $v_{tT-6} \geq K$ for any $i \in \{0, 1, \ldots, T - 6\}$ ($s_t = \{0, 0, 0, 1, 0, 1, 1, 1\}$).

It was shown in [15] that these new nodes can be decoded efficiently to improve the speed of SCL decoding. However, the drawback of using these new nodes when implementing the decoder on hardware is that these nodes are based on multiple bit estimations at a time, thus producing more than $2L$ candidates in each decoding step. Therefore, a large sorter is required to select the final $L$ candidates which adversely affects the hardware implementation complexity. In particular, at each decoding step, Type-I node produces $4L$ candidates to account for all the cases for its two information bits, Type-II node produces $8L$ candidates to account for all the cases for its three information bits, and Type-V node produces $16L$ candidates to account for all the cases for its four information bits. Moreover, Type-III node is decoded using two parallel SPC node decoders, and Type-IV node starts by decoding a Rep node of length four followed by four parallel SPC node decoders [15].

The pruned decoding tree for the same example as in Fig. 1 is shown in Fig. 2. If the new nodes are not taken into account, $\mathcal{P}(8,4)$ can be decoded in four time steps by traversing the tree for one level and decode the resulting Rep and SPC nodes. The resulting list of operations for the decoder would be $\{F_2, \text{Rep}_2, G_2, \text{SPC}_2\}$, where Rep and SPC represent the decoding of Rep and SPC nodes of length $T = 2^t$, respectively. However, by considering the new nodes, the decoder can immediately decode the received vector by decoding the Type-V node. The corresponding list of operations would be $\{\text{Type-V}_4\}$, where Type-V represents the decoding of Type-V nodes of length $T = 2^t$. The operations which are performed in fast SC-based decoders are summarized in Table I. Note that $F_1$ and $G_t$ operations are common between conventional SC-based and fast SC-based decoding algorithms. In the hardware implementation of fast SC-based decoders, this list of operations is stored in memory and is fed into the decoder to perform decoding [5], [7], [8].

Let us consider the example in Fig. 2. If the rate of the code changes from 1/2 to 5/8, the list of operations also changes as shown in Fig. 3. Without using the new nodes, the list of operations becomes $\{F_2, \text{Rep}_2, G_2, \text{Rate-1}\}$, and by considering the new nodes it becomes $\{\text{Type-IV}_3\}$. Therefore, as the rate changes, the list of operations changes. The resulting decoder is therefore not rate-flexible. For applications that support codes with multiple rates, for each rate, the list of operations has to be stored in memory to make the decoder flexible. However, this results in high memory usage when implemented on hardware.

### TABLE I: Different operations that are supported in SC-based decoding algorithms.

| Operation | Description | Decoder |
|-----------|-------------|---------|
| $F_t$     | Calculate $\alpha^t$ at level $t$. | SC-based |
| $G_t$     | Calculate $\alpha$ at level $t$. | SC-based |
| Rate-0$_t$| Decode Rate-0 node of length $2^t$. | Fast SC-based |
| Rate-1$_t$| Decode Rate-1 node of length $2^t$. | Fast SC-based |
| Rep$_t$   | Decode Rep node of length $2^t$. | Fast SC-based |
| SPC$_t$   | Decode SPC node of length $2^t$. | Fast SC-based |
| Type-I$_t$| Decode Type-I node of length $2^t$. | Fast SC-based |
| Type-II$_t$| Decode Type-II node of length $2^t$. | Fast SC-based |
| Type-III$_t$| Decode Type-III node of length $2^t$. | Fast SC-based |
| Type-IV$_t$| Decode Type-IV node of length $2^t$. | Fast SC-based |

Fig. 3: Fast SC-based decoding on a binary tree for $\mathcal{P}(8,5)$ and $v = \{7, 6, 5, 3, 4, 2, 1, 0\}$ ($s = \{0, 0, 0, 1, 1, 1, 1, 1\}$).

The high memory usage of storing the list of operations can be mitigated by generating the list of operations on hardware as the decoding proceeds. A rudimentary approach would be to generate the vector $s_t$ from $K$ and the vector $v_t$, using comparators, and check the pattern of information and frozen bits in $s_t$ for every encountered node. This is shown in Fig. 4 for determining Rate-0, Rate-1, Rep, and SPC nodes of length 8. It should be noted that the comparators in Fig. 4a have two inputs $A$ and $B$, and an output $C$ where

$$C = \begin{cases} 0, & \text{if } A \geq B, \\ 1, & \text{if } A < B. \end{cases} \quad (13)$$

The problem with this approach is that for nodes of large length, there is a high hardware complexity overhead in generating $s_t$ from $K$ and $v_t$, and determining the node types. Moreover, the module that generates the list of operations should account for the largest possible node which is the root node in the decoding tree with size $N$. This results in a large critical path which limits the operating frequency.

In order to tackle the above issue, the idea is to exploit the inherent order in the Bhattacharyya parameters of the bit-channels. Let $W_i$ and $W_j$ be the bit-channels corresponding
follows. Consider the transmission over a BMS channel sets.

Theorem 1. Consider a node of length \( T = 2^t \) in a polar code of length \( N = 2^u \). Then, the following properties hold:

1. If \( v_{st-1} \geq K \), i.e., \( s_{st-1} = 0 \), then the node represents a Rate-0 node.
2. If \( v_b < K \), i.e., \( s_0 = 1 \), then the node represents a Rate-1 node.
3. If \( v_{st-1} < K \) and \( v_{st-2} \geq K \), i.e., \( s_{st-1} = 1 \) and \( s_{st-2} = 0 \), then the node represents a Rep node.
4. If \( v_b \geq K \) and \( v_t < K \), i.e., \( s_0 = 0 \) and \( s_1 = 1 \), then the node represents an SPC node.

Proof. 1) Note that \( b^{T-1} = \{1, \ldots, 1\} \). By using the addition property (14), we obtain that \( W_i < W_{st-1} \) for any \( i \in \{0, 1, \ldots, T-2\} \). Hence, as \( v_{st-1} \geq K \), \( v_t \geq K \) for any \( i \in \{0, 1, \ldots, T-2\} \). This means that the polar code consists of only frozen bits, i.e., it is a Rate-0 node.

2) Note that \( b^0 = \{0, \ldots, 0\} \). By using the addition property (14), we obtain that \( W_b < W_{v_t} \) for any \( i \in \{1, 2, \ldots, T-1\} \). Hence, as \( v_b < K \), \( v_t < K \) for any \( i \in \{1, 2, \ldots, T-1\} \). This means that the polar code consists of only information bits, i.e., it is a Rate-1 node.

Recall that, if \( W_i < W_j \), then all the reliability measures of \( W_i \) are worse than those of \( W_j \), i.e., \( W_i \) has smaller mutual information, larger Bhattacharyya parameter, and larger error probability. Consequently, if \( u_j \) belongs to the frozen set, then also \( u_i \) belongs to the frozen set. Furthermore, if \( u_i \) belongs to the information set, then also \( u_i \) belongs to the information set.

By using the two properties above, it was shown in (18) that it suffices to compute the reliability of a sublinear fraction of channels in order to identify the frozen and the information sets.

Another option to find an ordering between the Bhattacharyya parameters of the bit-channels can be described as follows. Consider the transmission over a BMS channel \( W \) with Bhattacharyya parameter \( Z(W) \) and define the synthetic channels \( W^0 \) and \( W^1 \) as

\[
W^0(y_1, y_2 \mid x_1) = \sum_{x_2} \frac{1}{2} W(y_1 \mid x_1 \oplus x_2) W(y_2 \mid x_2),
\]

\[
W^1(y_1, y_2, x_1 \mid x_2) = \frac{1}{2} W(y_1 \mid x_1 \oplus x_2) W(y_2 \mid x_2).
\]

Then, the following inequalities between \( Z(W^0) \), \( Z(W^1) \) and \( Z(W) \) hold

\[
Z(W) \sqrt{2 - Z(W)^2} \leq Z(W^0) \leq 2Z(W) - Z(W)^2, \quad Z(W^1) = Z(W)^2,
\]

which follow from Proposition 5 of (11) and from Exercise 4.62 of (19). Furthermore, the bit-channel \( W_i \) corresponding to \( u_i \) is given by the recursive formula below:

\[
W_i = (((W^{b_{n-1}} b_{n-2}) \cdots b_0)
\]

In what follows, we will denote by \( Z_i \) the Bhattacharyya parameter of \( W_i \).

At this point, we are ready to state and prove the first result of this paper, which concerns the identification of Rate-0, Rate-1, Rep, and SPC nodes.

**Fig. 4:** Determination of node types for fast SC-based decoding in a node of length \( T = 8 \). (a) generation of \( s_t \) from \( K \) and \( v_t \), (b) Rate-0 node, (c) Rate-1 node, (d) Rep node, (e) SPC node.
Theorem 2. Consider a node of length $T = 2^t$ in a polar code of length $N = 2^n$. Then, the following properties hold:

1) If $v_{T-1} < K$, $v_{T-2} < K$, and $v_{T-3} \geq K$, then the node represents a Type-I node.

2) If $v_{T-3} < K$, $v_{T-2} < K$, and $v_{T-3} \geq K$, then the node represents a Type-II node.

3) If $v_0 \geq K$, $v_1 \geq K$, and $v_2 < K$, then the node represents a Type-III node.

4) If $v_0 \geq K$, $v_1 \geq K$, and $v_4 < K$, then the node represents a Type-IV node.

5) If $v_{T-3} < K$, $v_{T-2} < K$, $v_{T-3} < K$, $v_{T-4} \geq K$, $v_{T-5} < K$, and $v_{T-6} \geq K$, then the node represents a Type-V node.

Proof. 1) Note that $b^{T-3} = \{1, \ldots, 1, 0, 1\}$. By using the addition property (14) and the left-swap property (15), we obtain that $W_i < W_{T-2}$ for any $i \in \{0, 1, \ldots, T-3\}$. Hence, as $v_{T-3} \geq K$, $v_{T-2} \geq K$ for any $i \in \{0, 1, \ldots, T-3\}$. As $v_{T-1} < K$, the polar code consists of frozen bits except for the last bit which is an information bit, i.e., it is a Rep node.

4) Note that $b^4 = \{0, \ldots, 0, 1\}$. By using the addition property (14) and the left-swap property (15), we obtain that $W_i < W_{T-3}$ for any $i \in \{0, 1, \ldots, T-6\}$. Hence, as $v_{T-3} \geq K$, $v_{T-2} \geq K$ for any $i \in \{0, 1, \ldots, T-6\}$. Furthermore, note that $b^{T-3} = \{1, \ldots, 1, 0, 0\}$. Let $W$ be the transmission channel and let $z$ be the Bhattacharyya parameter of the channel defined as

$$Z_{T-3} = \left(\sqrt{2 - z^4}\right)^4.$$ 

Then, by using (17), we have that

$$Z_{T-4} \leq \left(2 - z^4\right)^4,$$

$$Z_{T-4} \leq \sqrt{2 - z^4}\sqrt{2 - z^4}(2 - z^4).$$

It is easy to check that, for any $z \in [0, 1],

$$(2 - z^4)^4 \leq \sqrt{2 - z^4}\sqrt{2 - z^4}(2 - z^4),$$

which implies that

$$Z_{T-5} \leq Z_{T-4}.$$ 

Consequently, as $v_{T-5} \geq K$, $v_{T-4} \geq K$. As a result, since $v_{T-3} < K$, $v_{T-2} < K$, and $v_{T-3} < K$, the node consists of frozen bits except for the last three bits which are information bits, i.e., it is a Type-II node.

3) Note that $b^2 = \{0, \ldots, 0, 1, 0\}$. By using the addition property (14) and the left-swap property (15), we obtain that $W_2 < W_i$ for any $i \in \{3, 4, \ldots, T-1\}$. Hence, as $v_2 < K$, $v_1 < K$ for any $i \in \{3, 4, \ldots, T-1\}$. As $v_0 \geq K$ and $v_1 \geq K$, the node consists of information bits except for the first two bits which are frozen bits, i.e., it is a Type-III node.

4) Note that $b^1 = \{0, \ldots, 0, 1, 0, 0\}$. By using the addition property (14) and the left-swap property (15), we obtain that $W_4 < W_i$ for any $i \in \{5, 6, \ldots, T-1\}$. Hence, as $v_4 < K$, $v_1 < K$ for any $i \in \{5, 6, \ldots, T-1\}$. Furthermore, note that $b^1 = \{0, \ldots, 0, 1, 1\}$. Let $W$ be the transmission channel and let $z$ be the Bhattacharyya parameter of the channel defined as

$$t-3 \text{ times} \left(\sqrt{2 - z^4}\right)^4.$$ 

In the proof of Theorem I we used the fact that for any node of length $T = 2^t$ in a polar code of length $N = 2^n$, the $n$-bit binary expansions of the integers corresponding to the bit-channels in the node are equal in the bits $\{n-1, n-2, \ldots, t\}$, and are different in the bits $\{t-1, t-2, \ldots, 0\}$. An immediate consequence of Theorem I is that, by checking only one value, we can find out if a constituent node is either a Rate-0 or a Rate-1 node. Furthermore, by checking only two values, we can find out if a constituent node is either a Rep or an SPC node. This observation significantly reduces the hardware complexity associated with the on-line node identification. In addition, the proposed approach is independent of the node length, making it suitable for codes of any length and rate. Fig. 5 shows the circuit required to generate the list of operations on-line for any node of length $T$. It can be seen that the circuit consists of only four comparators, three NOT gates, and two AND gates.

Let us now state and prove the second result of this paper, which concerns the identification of Type-I, Type-II, Type-III, Type-IV, and Type-V nodes.

Theorem 2. Consider a node of length $T = 2^t$ in a polar code of length $N = 2^n$. Then, the following properties hold:

- If $v_{T-1} < K$, $v_{T-2} < K$, and $v_{T-3} \geq K$, then the node represents a Type-I node.
- If $v_{T-3} < K$, $v_{T-2} < K$, and $v_{T-3} \geq K$, then the node represents a Type-II node.
- If $v_0 \geq K$, $v_1 \geq K$, and $v_2 < K$, then the node represents a Type-III node.
- If $v_0 \geq K$, $v_1 \geq K$, and $v_4 < K$, then the node represents a Type-IV node.
- If $v_{T-3} < K$, $v_{T-2} < K$, $v_{T-3} < K$, $v_{T-4} \geq K$, $v_{T-5} < K$, and $v_{T-6} \geq K$, then the node represents a Type-V node.
Then, by using (17), we have that
\[ Z_3 \leq (2z - z^2)^4, \]
\[ Z_4 \geq z^2 \sqrt{2 - z^2} \sqrt{2 - z^4 (2 - z^4)}. \]

Since (19) holds for any \( z \in [0, 1] \), we obtain that
\[ Z_3 \leq Z_4. \]

Consequently, as \( v_{i1} < K, v_{i1} < K \). As a result, since \( v_0 \geq K, v_{i1} \geq K \), and \( v_{i2} \geq K \), the node consists of information bits except for the first three bits which are frozen bits, i.e., it is a Type-IV node.

5) Note that \( k = 9 \). By using the addition property (14) and the left-swap property (15), we obtain that \( W_i < W_{T-9} \) for any \( i \in \{0, 1, \ldots, T-10\} \). Hence, as \( v_{T-9} \geq K, v_i \geq K \) for any \( i \in \{0, 1, \ldots, T-10\} \). By using again the left-swap property (15), we obtain that \( W_{T-6} < W_{T-4} \) and \( W_{T-7} < W_{T-4} \). By using again the addition property (14), we obtain that \( W_{T-8} < W_{T-4} \). Hence, as \( v_{T-4} \geq K, v_i \geq K \) for any \( i \in \{T-6, T-7, T-8\} \). As a result, since \( v_{T-1} < K, v_{T-2} < K, v_{T-3} < K \), and \( v_{T-5} < K \), the node is a Type-V node.

\[ \square \]

The proofs for the identification of Rate-0, Rep, SPC, Rate-I, Type-I, Type-III, and Type-V nodes are based on stochastic degradation arguments. Consequently, these proofs are general and do not depend on the fact that the frozen bits are determined according to the value of the Bhattacharyya parameter. On the contrary, the proofs for Type-II and Type-IV nodes use the inequalities (17) which are valid for Bhattacharyya parameters. However, let us point out that the strategy of the proof (use extremes of information combining bounds such as (17) in order to compare the reliability of specific channels) is general. In order to prove a similar statement for different reliability measures, one would need to find bounds of the form (17) for the desired reliability measure (e.g., mutual information, error probability). Let us further clarify that the proofs for Type-II and Type-IV nodes provide an ordering between the Bhattacharyya parameter of bit-channels. As such, they do not depend on the particular technique used to compute those Bhattacharyya parameters (Gaussian approximation [20], beta-expansion [21], Monte Carlo simulation [1], etc.). Let us also note that the Bhattacharyya parameter represents the typical performance metric employed for code construction [22]–[24].

It is also worth mentioning that since every node in the SC-based decoding tree represents a polar code constructed for a different channel [1], the results in this section are valid for all the nodes in any polar code of any length. Fig. 6 shows the circuit required to generate the list of operations on-line for any node of length \( T \), if Type-I, Type-II, Type-III, Type-IV, and Type-V nodes are considered in addition to Rate-0, Rep, SPC, and Rate-1 nodes. It can be seen that the circuit consists of ten comparators, nine NOT gates, and fourteen AND gates, in order to identify all the special nodes.

**Fig. 6:** Efficient generation of the list of operations on hardware considering new nodes.

### IV. Decoder Architecture

As a proof of concept, a decoder architecture implementing the proposed technique has been designed. It implements the layered partitioned SCL (LPSCL) decoding algorithm detailed in [23] and the Fast-SSCL-SPC algorithm introduced in [8], along with the memory-reduction techniques proposed in [26]. The LPSCL decoder decreases the memory requirements of standard SCL decoding by dividing the SC decoding tree in different partitions; the bottom part of the SC decoding tree belonging to each partition is decoded with SCL with a list size \( L_{\text{max}} \). When information needs to be passed between partitions, i.e. at the top stages of the tree, only \( L_t < L_{\text{max}} \) candidate codewords are passed, with \( L_t \) decreasing progressively as the stage \( t \) increases. The Fast-SSCL-SPC algorithm is applied to the lower stages of the tree, where \( L_{\text{max}} \) candidates are considered.

Fig. 7 shows the architecture of the proposed decoder. It
is based on a semi-parallel SCL decoder architecture, where \(L_{\text{max}}\) sets of \(N_{\text{PE}}\) processing elements (PEs) are instantiated in parallel, implementing (7) and (8). Each set works on a different candidate codeword, as explained in Section II-B. Different candidate codewords are created whenever one or more information bits are estimated. Each set of PEs relies on a dedicated memory to store the internal LLR values relative to all stages of the SC decoding tree. LLR values are quantized with \(Q_{\text{LLR}}\) bits, and represented with sign and magnitude. Each stage of the SC decoding tree requires the storage of \(2^{t-1}\) LLR values. However, given the limited number of PEs instantiated, the LLR memory is split in high stage and low stage memories. The high stage memory stores LLR values of stages with nodes of size greater than \(N_{\text{PE}}\): at stage \(t\), where \(2^t > 2N_{\text{PE}}\), a total of \(2^t/(2N_{\text{PE}})\) decoding steps are needed to descend to the lower tree level. The depth of the high stage memory is \(2^{\sum_{j=0}^{t-1} \log_2 N_{\text{PE}}+1} 2^j / N_{\text{PE}} = N / N_{\text{PE}} - 2\), while it is \(Q_{\text{LLR}} \times N_{\text{PE}}\) wide. The low stage memory stores LLR values for stages where \(2^t \leq 2N_{\text{PE}}\), and it is \(Q_{\text{LLR}}\) bits wide, while its depth is \(2^{\sum_{j=0}^{t-1} \log_2 N_{\text{PE}}-1} N_{\text{PE}} / 2^j = 2N_{\text{PE}} - 2\). High and low stage memory words are rewritten when a node belonging to the same level \(t\) is traversed. \(L_{\text{max}}\) different instantiations of both high and low stage memories are required. \(L_{\text{max}}\) separate path memories store the hard bit estimates (11) for all the tree stages as well, updating them every time that a bit is estimated. PMs, that identify the likelihood of a candidate codeword (or path) to be correct, are incremented every time a bit is estimated differently from the sign of the LLR value associated to it. They are sorted in PM memory before and after the estimation of an information bit, in order to identify the \(L_{\text{max}}\) surviving paths out of the \(2L_{\text{max}}\) created. When none of the paths coming from the splitting of a particular candidate codeword survives, all stages of its LLR memory are overwritten, along with the bit estimate and PM memories.

This baseline architecture has been modified to implement the LPSCL decoder. The bottom stages of the SC decoding tree are left unchanged, and decoded with a list size \(L_{\text{max}}\). Given the partitioning factor \(P\), the top \(\log_2 P\) stages rely on a smaller list size \(L_t\), with \(n - \log_2 P < t \leq n\), and \(L_t \geq L_{t+1}\). Consequently, only \(L_t\) LLR memories are instantiated in the upper stages, reducing the LLR memory requirements for each upper stage of a factor \(L_{\text{max}} / L_{\text{max}}\), as shown in Fig. 8. Depending on the number of instantiated PEs and on the partitioning factor, the high and/or low stage memories might need to be separated into different memory structures, each part belonging to a different layer of LPSCL and thus instantiated a different number of times, depending on \(L_t\). Since the number of surviving paths is reduced from \(L_{\text{max}}\) to \(L_t\) when ascending the decoding tree above stage \(n - \log_2 P\), the \(L_{\text{max}} - L_t\) candidate codewords with the highest PMs need to be discarded. In the baseline architecture, PMs are sorted only when an information bit is estimated, i.e. when the paths split. However, in the proposed architecture the PMs need to be sorted also when \(i \mod (N/P) = 0\), where \(i\) is the index of the codeword bit that needs to be estimated, and \(\mod\) represents the modulo operation. The decoding of a bit with such an index \(i\) identifies the completion of the decoding of a subtree of size \(N/P\), and the need to transfer information to the upper tree stages, where \(L_t < L_{\text{max}}\). The sorting of PMs allows the most reliable paths, their LLR values, and their hard bit estimates to be transferred between partitions through the memory copy mechanism addressed in Fig. 8.

The implementation of the Fast-SSCL-SPC algorithm requires more substantial modifications, that have been detailed in [8]. The hard bit estimate memory and path memories are updated according to different values depending on the node type, along with PMs. This requires different parallel instantiations of the PM computation logic, as shown in Fig. 9. More complex routing and selection logic are necessary to update memories, since multiple concurrent values need to be updated and propagated through the hard bit estimates memory structure. A sorter module for LLR values is needed in Rate-1 and SPC nodes, to identify the order with which bits are estimated: the disruption of the sequential bit estimation order that SC is based on leads to additional complexity in memory updates and control logic.

Aside from the logic needed to perform the calculations for special node PM update and bit estimations, the decoder needs to know at which point in the SC tree the special nodes are found, and what is their type. This information is used to identify the number of clock cycles needed for the decoding of a particular node, and which of the different parallel PM, path, and LLR updates are memorized. In [8], the proposed decoder architecture relied on an off-line compiler to obtain the sequence of special nodes, their size, and the stage at which they are encountered. These informations differ for every code supported by the decoder, and need to be stored in a memory. Note that the frozen and information bit sequence can be either stored in a memory, as supposed by most decoder architectures in literature, or computed on-line given the bit-channel relative reliability vector and the desired code rate, as proposed in [10]. This approach is significantly more efficient in case of multi-code decoders, and is facilitated by nested reliability vectors as those selected for the 5G eMBB control channel [11]. This is the approach taken in both the baseline and the modified architectures in this paper, by comparing each entry of the relative reliability vector \(v\) to the desired \(K\) in order to obtain \(s\).

The control unit of the modified architecture implements the proposed special node on-line identification, based on
the relative reliability vector $v$ and $K$. Fig. 5 shows the simple logic needed to identify the considered special nodes. Given the low complexity of the node identification circuit, the structure is instantiated at every decoding tree stage $t$, separately at every partition identified by LPSCL, to reduce the amount of multiplexing needed at the inputs and the possible increase in the system critical path. The logic pictured in Fig. 5 is inserted within a finite state machine (FSM) in the decoder control unit to identify the correct decoding phase, through two main control signals, $\text{NodeType}$ and $\text{NodeSize}$. A maximum $\text{NodeSize}$ value for each $\text{NodeType}$ is selected at design time, to limit the additional complexity and critical path degradation.

- While the general node type can be identified easily through the proposed identification, different decoding phases are foreseen within each special node. Thus, $\text{NodeType}$ foresees subtypes in the special node. While the Rate-0 node is a standalone node type, the Rate-1 node is divided into three subtypes: one phase is assigned to the fetching and sorting of the LLR values, a second to the estimation of the bits associated to the least reliable LLR values, and the third for the hard decision on the remainder of the bits. The Rep node is divided in two subtypes, one for the frozen bits and one for the information bit. Finally, SPC nodes foresee four subtypes: one for the concurrent fetching and sorting of LLR values and frozen bit selection, one for the bit estimations, one for the hard decision on the remaining bits, and one for the parity correction. The $\text{NodeType}$ signal is thus influenced not only by the result of the logic in Fig. 5 but also by the number of estimated bits within the special node, the stage $t$, and the current $\text{NodeType}$ subtype.

- The control unit identifies the size of the special node $\text{NodeSize}$ as $2^t$, given the current SC decoding tree stage $t$. This information is used to update the index $i$ of the codeword bit to be estimated. The index $i$ is usually updated once a leaf node has been reached and the corresponding bit estimated, but during the decoding of special nodes, it is kept fixed pointing at the first bit of the node. Once the decoding is terminated, the index is updated as $i + \text{NodeSize}$.

### V. HARDWARE IMPLEMENTATION RESULTS

The proposed decoder architecture has been described in VHDL and synthesized in TSMC 65 nm CMOS technology, at the operating conditions defined by the NCCOM corner, i.e. 1.2 V core voltage and a temperature of 298 K. Two versions
of the decoder have been implemented: one considering the proposed special node identification technique, and one based on the off-line identification and storage used in [8]. Both decoders target the 5G polar code with a code length \( N = 1024 \) [11], rely on a partitioning factor \( P = 4 \), and make use of 64 parallel PEs. The bottom part of the SC decoding tree is decoded with a list size \( L_{\text{max}} = 4 \), while for the upper stages \( L_{10} = L_9 = 2 \). Fig. 10 shows the frame error rate (FER) and bit error rate (BER) performance of the LPSCL decoder used in this paper in comparison with SCL decoding with \( L = 4 \). The curves in Fig. 10 are provided for the code rates of \( \{\frac{1}{16}, \frac{1}{8}, \frac{1}{4}, \frac{1}{2}, \frac{3}{4}, \frac{2}{3}, \frac{1}{2}, 1\} \). It can be seen that LPSCL decoding incurs negligible FER and BER performance loss with respect to SCL for all considered rates. It should be noted that the introduction of the proposed technique to infer the list of operations on the fly does not change the FER or BER performance of the decoder in comparison with the same memory-based decoder.

The channel LLR values are quantized with 4 bits and internal LLR values with 6 bits, with 2 bits assigned to the fractional part, while PMs are quantized with 8 bits [20]. The maximum node size is set to 16 for Rate-0 and Rep nodes, and to 64 for Rate-1 and SPC nodes. Table II reports the area occupation and achievable frequency for the proposed decoder, and for the decoder based on the off-line identification technique, labelled as memory-based decoder. The two decoders differ in their implementation of the control unit (CU): its area occupation \( A_{\text{CU}} \) in the proposed decoder is 24% less than that of the memory-based decoder. This is due to the fact that the information computed off-line in the memory-based case, i.e. the equivalent of the \( \text{NodeType} \) signal, needs to be inserted in an FSM analogous to that used by the control unit of the proposed decoder. This FSM handles the node subtypes and the internal counters that determine when a special node decoding is terminated. Moreover, the memory-based case needs an additional information, \( \text{NodeStage} \), to identify at which SC decoding tree stage the special node is encountered: the \( \text{NodeSize} \) information is derived from that. The \( \text{NodeStage} \) signal is inserted in its own FSM, that adds substantial complexity to the control unit, resulting in a larger \( A_{\text{CU}} \). While the contribution of \( A_{\text{CU}} \) to the total decoder area occupation \( A_{\text{total}} \) is relatively small, with \( A_{\text{total}} = 1.410 \text{ mm}^2 \) and \( A_{\text{total}} = 1.454 \text{ mm}^2 \) for the proposed and the memory-based decoders respectively, the \( \text{NodeStage} \) FSM influences signals in the \( \text{NodeSize} \) and \( \text{NodeType} \) FSM, lengthening the critical path. In particular, the state of \( \text{NodeStage} \) is combined to the \( \text{NodeType} \) and \( \text{NodeSize} \) to determine the current and future node subtypes. This leads to a lower achievable frequency \( f \), lower throughput \( T_P \), and lower area efficiency \( A_{\text{eff}} \) in the memory-based decoder in comparison with the proposed decoder, as provided in Table II.

The proposed decoder fetches four required values of the relative reliability vector from memory, compares them with \( K \), and identifies the node types efficiently. Table II also reports the external memory requirements \( \text{Mem}_{\text{ext}} \) of the proposed decoder in comparison with the memory-based decoder considering 5G code rates are supported. For a code of length 1024, the vector of relative reliabilities \( \mathbf{v} \) contains 1024 entries where each entry is stored with 10 bits. Therefore, a total of 1024 \times 10 = 10240 bits are stored in memory. For the memory-based decoder, the memory requirement is different for different values of \( K \) (different rates). This is depicted in Fig. 11 where it can be seen that the list of operations is large for medium rates and becomes small as the rate becomes very high or very low. Note that the proposed decoder is capable of supporting any code rate within a given code length which is also foreseen in 5G [12]. If the memory-based decoder is designed such that it supports all the code rates of 5G for a code of length 1024 (12 \( \leq K \leq 1024 \)), the memory requirement of it considering a 4-bit representation for \( \text{NodeType} \) and \( \text{NodeStage} \) signals is 128140 \times 8 = 1025120 bits, more than 100 times larger than the number of bits required for the proposed decoder.

Artisan dual-port SRAM compiler was used for the implementation of the external memories. Table III shows the area occupation of the external memory for the proposed decoder in comparison with the memory-based decoder. While the proposed decoder supports all the code rates, the memory requirement of the memory-based decoder depends on the number of code rates it can support. In Table III we showed four cases of memory requirements for the memory-based decoder: when it supports 5 code rates of \( \{\frac{1}{2}, \frac{1}{2}, \frac{1}{2}, 1, 2\} \), when it supports 10 code rates of \( \{\frac{1}{16}, \frac{1}{8}, \frac{1}{4}, \frac{1}{2}, 1, 2, 3, 4, 5, 7\} \), when it supports 20 code rates of \( \{\frac{1}{32}, \frac{1}{16}, \frac{1}{8}, \frac{1}{4}, \frac{1}{2}, 1, 2, 3, 4, 5, 7, 8, 11, 13, 14, 15, 17, 23, 29\} \), and when it supports all the code rates considered in 5G, similar to the proposed decoder. It can be seen that the proposed decoder occupies a smaller area in comparison with the memory-based decoder even when the memory-based decoder supports only 5 code rates. In fact, the area occupation of the memory-based decoder increases as the number of supported code rates increases. This consequently reduces the area efficiency of the memory-based decoder as can be seen in Table III. The area occupation of the proposed decoder is only 38% of that of the memory-based decoder when both decoders support all 5G code rates.

It is worth mentioning that the goal of this paper is to propose a low-complexity approach to generate the list of operations for fast SC-based decoders directly on hardware, therefore, allowing for the implementation of a fast and rate-flexible SC-based decoder. Our implementation results show that by using the proposed method, there is a negligible area occupation overhead or throughput loss in comparison with the memory-based decoders, while having a completely rate-flexible decoder.
using LPSCL decoding with \( L \) decoded using the Fast-SSCL-SPC algorithm without fore-
knowledge of the information/frozen bit sequence, regardless of rate and target \( E_b/N_0 \). On the contrary, the memory-based decoder needs to store the \( \text{NodeType} \) and \( \text{NodeStage} \) information for each considered code in an external memory of \( \text{Mem}_{\text{ext}} \) bits.

Table IV compares the proposed decoder to other architectures in the state of the art which use 64 parallel PEs. Results are reported for \( \mathcal{P}(1024,512) \) and \( L = 4 \). The architectures presented in [8] and [7] are based on the Fast-SSCL-SPC and SSCL-SPC algorithms, respectively: it is possible to add the cost of the external memory directly to their area occupation and evaluate its impact on the area efficiency, considering all the code rates in 5G are supported. These modified results are reported within parentheses. It can be seen that the external memory increases \( A_{\text{total}} \) by 131\% in [8] and by 193\% in [7]: the proposed special node identification technique is thus able to substantially limit the area occupation and increase the area efficiency in both architectures. The architecture presented in this work has higher \( A_{\text{eff}} \) and lower \( A_{\text{total}} \) than both [7] and [8]. Different design choices in terms of concurrent operations in the special nodes lead to a slightly lower \( T_P \) than [8], together with a substantially lower \( A_{\text{total}} \) and higher \( A_{\text{eff}} \).

The architectures presented in [27]–[29] do not rely on a special-node-based decoding algorithm: thus, the throughput benefits and complexity saving of the proposed node identification technique cannot be directly evaluated. Moreover, the synthesis results of [27] were reported in 90 nm technology, but they were carried out in 65 nm technology. Therefore, a factor of 90/65 was used to convert the frequency, and a factor of \((65/90)^2\) was used to convert the area of the decoder from 90 nm to 65 nm technology in [27]. The same conversion factors were used to convert to 65 nm technology the synthesis results in [28], [29], which were synthesized with a 90 nm node.

Our work shows 31\% higher throughput and 31\% lower latency with respect to the multibit decision SCL decoder.
TABLE IV: Comparison with state-of-the-art decoders.

|                     | This work | [8] | [27] | [29]\(^\dagger\) | [29]\(^\dagger\) |
|---------------------|-----------|-----|------|-----------------|-----------------|
| \(A_{\text{int}}\) [mm\(^2\)] | 1.449     | 1.797 (4.155) | 1.22 (3.578) | 0.62            | 0.73            | 2.00 |
| \(f\) [MHz]         | 955       | 840 | 961  | 498             | 692             | 558  |
| \(T_P\) [Mb/s]      | 1223      | 1338| 1146 | 935             | 551             | 1578 |
| Latency [\(\mu\)s] | 0.84      | 0.77| 0.89 | 1.10            | 1.86            | 0.66 |
| \(A_{\text{eff}}\) [Mb/s/mm\(^2\)] | 844       | 744 (322) | 939 (320) | 1508            | 755             | 789  |

\(^\dagger\)The results are originally based on TSMC 90 nm technology and are scaled to TSMC 65 nm technology.

architecture of [27], while the smaller area occupation of [29] leads to a higher \(A_{\text{eff}}\). The decoder in [28] shows lower area occupation than our work. However, the architecture proposed in this work achieves 122\% higher throughput and 55\% lower latency, leading to 11\% higher area efficiency. The high throughput SCL decoder architecture of [29] achieves higher throughput and lower latency than this work, at the cost of 38\% higher area occupation and 7\% lower \(A_{\text{eff}}\). Moreover, [29] relies on tunable parameters that can lead to more than 0.2 dB error-correction performance loss. These parameters also reduce the flexibility of the decoder, since for each code rate, a different set of parameters needs to be used. However, the decoder proposed in this paper is designed to guarantee rate-flexibility, making it suitable for 5G applications.

VI. CONCLUSION

The main drawback of the fast successive-cancellation-based decoders for polar codes is that they require to store a list of operations for each code rate in a dedicated memory. In order to tell the decoder when a special node in a code graph is reached. In this paper, we tackled this issue by proposing a technique to generate the list of operations on-the-fly directly in hardware. We proved that this technique can be applied to polar codes of any rate, therefore, removing the memory needed to store the list of operations completely. We proposed a hardware architecture for the proposed technique and showed that the total area occupation of the proposed decoder is 38\% of the base-line memory-based decoder, if 5G code rates are considered.

ACKNOWLEDGMENTS

The authors would like to thank Arash Ardakani and Harsh Aurora of McGill University for helpful discussions. S. A. Hashemi is supported by a Postdoctoral Fellowship from the Natural Sciences and Engineering Research Council of Canada (NSERC). M. Mondelli is supported by an Early Postdoc.Mobility fellowship from the Swiss National Science Foundation and by the Simons Institute for the Theory of Computing.

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