IMAGE PROCESSING ARCHITECTURES

SARAH ILYAS¹, MUHAMMAD ADEEL ASHRAF¹, MUHAMMAD AIZAZ AKMAL³

¹Department of Computer Science, University of Management and Technology, Lahore, Punjab, Pakistan
Email: S2016279006@umt.edu.pk

ABSTRACT. One type of signal processing is Image processing in which the input used as an image and the output might also be an image or a set of features that are related to the image. Images are handled as a 2D signal using image processing methods. For the fast processing of images, several architectures are suitable for different responsibilities in the image processing practices are important. Various architectures have been used to resolve the high communication problem in image processing systems. In this paper, we will yield a detailed review about these image processing architectures that are commonly used for the purpose of getting higher image quality. Architectures discussed are FPGA, Focal plane SIMPil, SURE engine. At the end, we will also present the comparative study of MSIMID architecture that will facilitate to understand best one.

Keywords: Image processing architecture, FPGA, SIMPil, SURE engine, MSIMID

1. Introduction. Image processing is a kind of signal processing in which the information is a picture, a photo or a motion picture and the output may likewise be a picture, an arrangement of highlights that are identified within the picture. Furthermore, image processing methods require handling the image as a two-dimensional signal. For the fast processing of images, various architectures are suitable for different responsibilities in the image processing practices are essential. Over the past few years, real-time image processing experienced a burst in its flexible domain. The basic determination of image processing architectures is to increase the gesture of the quality of the picture by eliminating the disruption inside the sequences. It is intended to deliver the approvals and support to associate the gap among the idea and the preparation of managing the picture or movie by offering a broad summary of recognized modules or application programs and approaches. In order to attain excessive description feedback, low expectancy catch, effective handling, and competent display, real-time image processing comprises numerous aspects of application and modules. This paper explains about how image processing architecture works and also presents the study of several image processing architectures.

Problem statement: This research explains the full discussion about various image processing architectures that are commonly used for managing or dealing with several image processing issues. In image processing structures, the most basic problem is the requirement of high communication. Typical communication results such as Ethernet or USB are sometimes not satisfactory for high resolutions and high edge rates. Thus, for the fast processing of images, various architectures are suitable for different responsibilities in the image processing methods that are necessary. In this paper, FPGA, SIMPil, and SURE engine are different architectures that are discussed in detail.

2. Related Work. The structure and execution of a Field Programmable Gate Array (FPGA) were also discussed by Divyang K et al. It is based on the high-fidelity in-depth system that is capable of managing a very big inconsistency variety. The system implements modification of the input video stream and a left-right reliability check to recover the correctness of the outcome and makes subpixel inconsistencies at 30 frames per second on 480X640 images. Acharaya also outlines an effective FPGA design built on the design of hardware for the improvement of colors in both image and video processing. The method works very efficiently for images that are taken in the very dark atmosphere as well as in the lighting atmosphere. Sek M Chai described a structural design that uses a focal plane electronic-area input/output with a kernel, small memory, and SIMD processor range as a well-organized computational result for real-time image processing. Sabrina E offers an updated research activity in the domain of focal plane image processing systems. Two main areas have been followed; reformation of an image for the purpose of image compression and image half-tonning. The working
principal of SUREengine (Pattern Restructuring Optimizer) defined by the Miura. Pattern Restructuring Optimizer is a form of complex image quality. The SUREengine working is based on the concept of pattern Restructuring. It is basically used to improve the quality of the image.

**Benefits:** Image processing methods can gain advantage from various computing architectures. Each architecture is compatible to resolve a specific task proficiently, which is verified by a complete calculation. It is likely to attain a high amount to decrease the potential of the entire routing system considerably with the support of well-known pipeline. Nowadays different architectures have to be used to make high-speed image processing methods while in previous years typical PC modules were satisfactory to accomplish the requests.

**Impact on society:** Image processing is very difficult and slow task. Thus, a well suited or high-quality choice of the useful architectures is necessary. In industrial applications, only standard PCs with a serialized processing system are used for the necessary responsibilities. It effects in high potentials and in low throughput.

**Application Areas**
- Detailed applications of FPGA involve Image and video processing stage such as laser image sensor, real time multi-object investigator, Space Radiology, Wired and wireless Communication network, Vehicle recognition and observing etc.
- The SIMPil focal plane architecture also applied in Image recognition for image density and half image tonning. It is also capable of real-time performance with increased throughput operations.
- SUREEngine used to increase the signal to noise ratio, distinction and time resolution and also offers the high quality of the image.

3. **Methodologies.** The Following have been discussed the working of numerous architectures based on image processing:

**A. Field programmable gate arrays (FPGA)**

FPGA is a system in which the user can directly be organized the finishing logic structure of the system. It comprises of an array or a collection of free origins/elements that can be automated and interrelated consequently to user requirements.

![Figure 1: Structure of FPGA](image-url)

With estimating complete responsibilities, which makes more than half of low and middle level processes, FPGAs are the best suitable to use due to their structure. Nowadays it is likely to implement computer hubs on the reconfigurable material, which means the FPGA can make the fundamental of the system, with the help of growing its dimension. Based on FPGAs, image and video processing platform (IVPP) is offered. It is a special strategic flow that integrates the h/w and s/w modules is used in Figure-2. We have made elastic or a flexible architecture which enables the client to execute real time image processing on a particular frame or multiple frames with the help of this design. The video interface portions are ready and can be organized using the Micro Blaze processor permitting the support of multiple video purposes. Without altering the front-end and the back-end data, image and video processing platform offers a vital logic to simply produced processing chunks or blocks. So the given platform can be a broad hardware solution for a broad variety of real-time image and video processing applications such as video encryption and decryption, observation, revealing and recognition.
By providing resistance to the user, several processing choices are then possible.

- Without any processing, the user can select to show the video data.
- The user can also implement real-time processing on a single structure of video data and then show the out

Figure 2: HW/SW IVPP design flow

B. **SIMD Pixel Processor architecture**

Due to the capability to perform necessary data parallelism in images, parallel architectures are most suitable for the image processing applications. The SIMD pixel processor (SIMPil) architecture basically designs a collection of pixels to every single processor. While proposing enormous parallelism, a little parallel data route supports a well-organized operation of gray scale pixels from the collection of pixels. However keeping a secure level of treating per pixel, vertical connection to the image plane permits the sensor and the processor groupings to be ascended.

**Processor architecture**

Figure 3: SIMPil architecture

Identify applicable funding agency here. If none, delete this text box.
The diagram of a distinct SIMpil knot is presented in the figure. The diagram explains by what method a particular node edges to a collection of sensors through the sample and hold circuitry, and analog to digital converters, and also how every single node is linked to one another in a system to activate in SIMD knot. Firstly, an 8-bit data route SIMpil node was executed. It comprises an 8 bit register file, an arithmetic logical unit, a shift unit, a 16-bit multiply accumulator, and 64-word local memory. The design aim of this architecture is to increase the effectiveness of the system execution. One of the architecture is the instruction set architecture which offers various types of arithmetic operations like subtraction, addition, and multiplication etc. It permits greater than 256 addressable sensors. To transform light absorptions to numerically equal values, every single node also comprises an analog to a digital integrated circuit. The SIMD implementation design permits the whole image to be tested by the system collectively.

C. SUREengine
Shimadzu Ultimate Real-time Enhancement Engine (SUREengine) is designed as a new high-speed real-time image processing machine. The main aspects that achieve the quality of the image consist of resolution, signal to noise relationship, dissimilarity such as contrast, and time resolution as well. As resolution is seriously affected by measuring device performance, the SUREengine was designed to increase the aspects of image quality as discussed previously such as signal to noise relation, contrast, and the time resolution.

Noise reduction
This new image processing device constantly separates noise elements from the signal elements in a respective image and then defeats only the noise elements. This allows to decreasing the noise from the image. Moreover, this procedure arises in real time image processing and offers further detailed noise reduction over a comprehensive series.

![Figure 4: Noise reduction process](image)

4. Comparative Study
This section covered the comparative study of previously discussed image processing architectures with Multiple SIMD (MSIMD) schemes for image processing that have some issues with their performance. Image processing difficulties commonly include large organized arrays of data and also an important factor for very fast computations. It took Two decades to cope with the issues in image processing because there are various unique structures for parallel processing. Various parallel architectures are discussed that have been established for image processing. Some of these architectures may be categorized insecurely as both SIMD processors and pipeline systems while most of the MIMD systems have been considered for the analysis of images at high-level.

In current years some multiple SIMD (MSIMD) structures have been suggested as appropriate architectures for the purpose of processing images. But there are some problems that are faced during the development of an effective MSIMD system.

D. Multiple SIMD (MSIMD) System for Image Processing
Now a days, there is a bit of awareness in the development of MIMD parallel processors. These systems can be
developed with autonomous processors for program execution that can be interconnected besides the sharing of particular memory resources. These types of systems are shown in figure 5.

Figure 5: MIMD processing system

Not only the processors are having local memory but also designed to access mutually shared memory. The interconnection network links the processors to the shared memory and shows an important design problem specifically while many processors are involved. The key benefit of the Multiple instruction multiple data system over the Single instruction multiple data system arises along with high-level image thoughtful responsibilities. For instance, the allocation of processors for examining the disconnected objects. Wherever each of the processor contracts with single object. Otherwise, some processors might be set to examine single object wherever every single processor might understand the analysis algorithm differently. Adjacent algorithms that are LOW-LEVEL executed more certainly with Single instruction multiple data system.

There are numerous suggestions regarding MSIMD, improved MIMD structural design which are planned for image processing applications. But none of these structural designs has been applied yet. The partitionable SIMD/MIMD system (PASM) is basically the structure of MSIMD’s. It includes ‘N’ processing elements as well as control units ‘Q’ whereas each of the unit administer N divided by Q (N/Q) processing elements. It means the system comprises of ‘Q’ processors in an MIMD scheme, each processor having an SIMD structure of ‘Q’ divided by N (Q/N) processing elements where N and Q represent the powers for 2 and the possibility of values is 1024 and 16 respectively. Neighboring participants in systematic organizers’ set may be vigorously connected to similar memory of a program for enhancing the number of processing elements in single instruction multiple data structure.

Hence, scheme may be divided or apportioned into multiple various sized SIMD structures that have ‘K’ divided by Q (KN/Q) processing elements and ‘K’ is the power for 2. Above all, if ‘K’ is equal to ‘Q’, then system works like single SIMD mainframe. Processing elements have interrelated by permutation system that can execute most promising permutations to move data within the elements that are being processed. Consideration of substituting network is also important for rearranging because, if the structure is organized as autonomous SIMD processors or a set of it, transmission of data for one SIMD processor does not affect with those of another [16, 17].

As SIMD system would be improved by low level image processing whereas the Multiple instruction multiple data system scheme will be enhanced for the analysis of image. Structure of multiple instruction multiple data scheme will be considerably simple than MSIMD scheme. In some situations, a data connection that is slow concerning the inner data routes of two structures can be suitable to interrelate the two systems.

The performance advantage for discussed architecture over the MSIMD system is accomplished at the disbursements of specific flexibility. There is a possibility of only two key situations when MSIMD organization can have the performance gain over parallel image processing architectures such as SIMPil, SUREengine and FPGA:

a) If low level image processing’s percentage to the analysis of image is very unreliable, also

b) If SIMD low level image processing needs processing of multiple, but very minor, sub-images.

So comparatively, we conclude that various MSIMD architectures are offered for the processing of image. But MSIMD is not simpler to organize than the discussed image processing architectures and will not be more effective for most image processing responsibilities.

Conclusion. This paper is a complete review of several image processing architectures or methods that are mostly used for higher image quality and that are commonly used for managing or dealing with several image
processing issues. To resolve high communication problem various architectures are used for different tasks in image processing systems. Architectures discussed are FPGA, Focal plane SIMPil, SUREengine. We explain different architectures with its application areas. The aim of this paper is to be valuable to the researchers and specialists who are interested in real-time image processing. In future, FPGA used in large scale integrated circuit to improve material by maintaining the consecutive software designs. Focal plane SIMPil used in X-ray image intensifier, Electromagnetic detectors and three-dimensional TVs. And last but not the least, SUREengine used to increase the performance of flat piece detectors.

![Graph showing Performance gain](image)

**Figure 6:** Performance gain

The following table shows the difference between parallel architectures with MSIMD systems.

| Parallel architectures based on SIMD/MIMD | MSIMD systems |
|-------------------------------------------|---------------|
| FGPA | SIMPil | SURE engine | During the development of effective MSIMD systems, some problems have been faced. |
| These architectures based on SIMD/MIMD schemes used to improve low level image processing and analysis of image. | It is simple and essential for fast computations and also compatible to resolve specific tasks proficiently. | The structure is not very simple than SIMD/MIMD schemes. |
| These parallel architectures are most suitable for the image processing applications. | Processing of MSIMD system is very complex so that it is not effective for most of the image processing tasks. | |

Table 1. Comparison between parallel architectures with MSIMD systems.
REFERENCES

[1] Desmouliers, C., Oruklu, E., Aslan, S., Saniee, J., & Vallina, F. M. (2012). Image and video processing platform for field programmable gate arrays using a high-level synthesis. IET Computers & Digital Techniques, 6(6), 414-425.

[2] Liu, L. F., Ma, H. M., & Lu, M. Q. (2010, December). A FPGA and Zernike moments based near-field laser imaging detector multi-scale real-time target recognition algorithm. In Information Science and Engineering (ISISE), 2010 International Symposium on (pp. 370-374). IEEE.

[3] Acharya, A., Mehra, R., & Takher, V. S. (2009). FPGA based non uniform illumination correction in image processing applications. pp349-358.

[4] Klupsch, S., Ernst, M., Huss, S. A., und Systeme, I. S., Rumpf, M., & Strzodka, R. (2002, April). Real time image processing based on reconﬁgurable hardware acceleration. In Workshop Heterogeneous Reconﬁgurable Systems on Chip (SoC) (p. 1).

[5] Xu, G. S. (2009, November). The study on real-time data processing based on CCD scanning and detecting device on FPGA. In Intelligent Computing and Intelligent Systems, 2009. ICIS 2009. IEEE International Conference on (Vol. 3, pp. 81-84). IEEE.

[6] Kemeny, S. E., Eid, S. I., Mendis, S. K., & Fossum, E. R. (1991, July). Update on focal-plane image processing research. In Charge-Coupled Devices and Solid State Optical Sensors II (Vol. 1447, pp. 243-251). International Society for Optics and Photonics.

[7] Gentile, A., Cruz-Rivera, J. L., Wills, D. S., Bustelo, L., Figueroa, J. J., Fonseca-Camacho, J. E., ... & Vargas-Gonzales, I. (1999, April). Real-time image processing on a local plane SIMD array. In International Parallel Processing Symposium (pp. 400-405). Springer, Berlin, Heidelberg.

[8] Chai, S. M., Gentile, A., Lugo-Beauchamp, W. E., Fonseca, J., Cruz-Rivera, J. L., & Wills, D. S. (2000). Focal-plane processing architectures for real-time hyperspectral image processing. Applied Optics, 39(5), 835-849.

[9] Keerthana, S., & Sathiyanakumari, K. (2017). A Brief Study of Image Processing and Techniques. Digital Image Processing, 9(1), 11-13.

[10] Gupta, P. (2013). A Survey Of Techniques And Applications For Real Time Image Processing. Journal of Global Research in Computer Science, 4(8), 30-39.

[11] Gupta, P. (2013). A Survey Of Techniques And Applications For Real Time Image Processing. Journal of Global Research in Computer Science, 4(8), 30-39.

[12] Spezzani, C., Cherifi, S., Sacchi, M., Vogel, J., Fabrizioli, M., & Panaccione, G. Laterally confined magnetic systems studied by synchrotron radiation techniques. Magnetic Properties of Laterally Confined Nanometric Structures.

[13] Elamaran, V., & Rajkumar, G. (2012). FPGA implementation of point processes using xilinx system generator. Journal of Theoretical and Applied Information Technology, 41(2), 201-206.

[14] Elphinstone, A. C., Heron, A. P., Hobson, G. S., Houghton, A., Lau, M. K., Powell, A. R., ... & Tozer, R. C. (1987). RAPAC: a high-speed image-processing system. IEE Proceedings E (Computers and Digital Techniques), 134(1), 39-46.

[15] Ahuja, N., & Swamy, S. (1984). Multiprocessor pyramid architectures for bottom-up image analysis. IEEE transactions on pattern analysis and machine intelligence, (4), 463-475.

[16] Khan, Y. D., Abid, A., Farooq, M. S., Abid, K., & Farooq, U. A Qualitative Analysis Of Feature Extraction Based Action Recognition Techniques.

[17] Butt, A. H., Rasool, N., & Khan, Y. D. (2017). A treatise to computational approaches towards prediction of membrane protein and its subtypes. The Journal of membrane biology, 250(1), 55-76.