Porting of eChronos RTOS on RISC-V Architecture

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Abstract. eChronos is a formally verified Real Time Operating System (RTOS) designed for embedded micro-controllers. eChronos was targeted for tightly constrained devices without memory management units. Currently, eChronos is available on proprietary designs like ARM, PowerPC and Intel architectures. eChronos is adopted in safety critical systems like aircraft control system and medical implant devices. eChronos is one of the very few system software’s not been ported to RISC-V. RISC-V is an open-source Instruction Set Architecture (ISA) that enables new era of processor development. Many standard Operating Systems, software tool chain have migrated to the RISC-V architecture. According to the latest trends⁴, RISC-V is replacing many proprietary chips. As a secure RTOS, it is attractive to port on an open-source ISA. SHAKTI and PicoRV32 are some of the proven open-source RISC-V designs available. Now having a secure RTOS on an open-source hardware design, designed based on an open-source ISA makes it more interesting. In addition to this, the current architectures supported by eChronos are all proprietary designs⁸, and porting eChronos to the RISC-V architecture increases the secure system development as a whole. This paper, presents an idea of porting eChronos on a chip which is open-source and effective, thus reducing the cost of embedded systems. Designing a open-source system that is completely open-source reduces the overall cost, increased the security and can be critically reviewed. This paper explores the design and architecture aspect involved in porting eChronos to RISC-V. The authors have successfully ported eChronos to RISC-V architecture and verified it on spike¹⁰. The port of RISC-V to eChronos is made available open-source by authors¹⁶. Along with that, the safe removal of architectural dependencies and subsequent changes in eChronos are also analyzed.

Keywords: eChronos, Porting, Real Time Operating Systems, RISC-V, SHAKTI
1 Introduction

Porting is the process of converting the software for the another architecture. A software has many exceptions and forms of programming specific to the architecture like memory or register allocation. To be able to run such executable file, we need porting. There are many OS porting techniques available in the literature [5] that follow trial and error approach. In this paper, we have used the hit and trial approach for porting eChronos on an open-source architecture RISC-V [11,13].

1.1 eChronos

The eChronos RTOS is a real-time operating system (RTOS) [14]. It is intended for tightly resource-constrained devices without memory management units and virtual memory support. Also, RTOS code base is designed to be highly modular so that only the minimal amount of code necessary is ever compiled into a given system image [14]. The eChronos RTOS is highly configurable and functional as shown in FIG 1 [3].

![Fig. 1. eChronos RTOS functionality](image)

1.2 RISC-V

RISC-V is an open-source hardware ISA based on Reduced Instruction Set Computer (RISC) principles. RISC-V is a layered and extensible open-source ISA
which means that it can support the implementation of well defined extensions for a given application. RISC-V offers a very flexible usage of instruction set which adds to upto RISC-V becoming more popular[4]. RISC-V is modular and flexible, which reduces the effort to develop the ancillary software for a specific processor.

1.3 Porting an operating system

Porting of OS is a time consuming process as it involves a changes to big and complex programs. Porting every specific program seems to be a bit irrational. So the solution to such a complex problem are the modern day compilers, which translates the high level language program to a platform independent code unlike the traditional compilers translating the code directly to the machine code. The intermediate language can then execute all programs and it gets translated into a sequence of machine code by a code generator to create a executable file. The use of intermediate code enhances the portability of the compiler, because only the machine dependent code (the interpreter or the code generator) of the compiler needs to be ported instead of porting the program itself. The remaining part of the code in the compiler can be treated as an intermediate code and then processed by the ported code interpreter. This reduces design efforts, because the machine independent code just needs to be developed only once to create a portable intermediate code. An interpreter is less complex to code and it follows a certain algorithm avoiding the need to be specifically port for every single program [7]. A software can be compiled and linked from source code for various operating systems and architectures. Real Time Operating System files are all architecture dependent. A small mistake in port files will lead to an easy system crash. [5,12].

2 Porting eChronos

The subsequent sections explain the step-wise process involved in the porting of eChronos for RISC-V architecture.

2.1 Prerequisites for porting eChronos on RISC-V

The following are the prerequisites

1 A Linux operating system running on personal computer with 4GB RAM.
2 A GNU based environment, that has all necessary software packages mentioned in [10].

2.2 Platform set up for eChronos

The following steps need to be done to run eChronos on an emulator,
Installation of RISC-V emulator  Follow the following steps that are listed below for the installation of RISC-V tools [1][2][9]:

1 The following packages are required for the RISC-V tools:
   autoconf automake autotools-dev curl libmpc-dev libmpfr-dev libgmp-dev
   libusb-1.0-0-dev gawk build-essential bison flex texinfo gperf libtool patchutils
   bc zlib1g-dev device-tree-compiler pkg-config
   libglib2.0-dev zlib1g-dev libpixman-1-dev

2 Set up a directory for the RISC-V tools, and the RISC-V environment variable, which we refer to in future steps.
   mkdir RISC-V
   cd RISC-V
   export RISC-V={PWD}

3 Get the RISC-V tools
   cd RISC-V
   git clone https://github.com/RISC-V/RISC-V-git
   cd RISC-V-tools
   git submodule update –init –recursive

4 Get RISC-V qemu sources, and build them:
   cd RISC-V/RISC-V-tools
   git clone https://github.com/heshamelmatare/RISC-V-qemu.git
   cd RISC-V-qemu
   git checkout sfence
   git submodule update –init dtc
   ./configure –target-list=RISC-V64-softmmu,RISC-V32-softmmu –prefix=RISC-V
   make -j8 && make install

5 Build the 64-bit toolchain
   cd RISC-V/RISC-V-tools
   sed -i’$$/build_project RISC-V-gnu-toolchain –prefix=$RISC-V/build_project
   RISC-V-gnu-toolchain –prefix=RISC-V –with-arch=rv64imafdc –with-abi=lp64’
   ./build.sh

6 Installation of eChronos
   Download and install the eChronos[4].
Fig. 2. Flow Diagram of eChronos
3 eChronos system design

The FIG.2 shows the system diagram of eChronos. The following steps explain FIG 2\[8\], that help eChronos produce an executable file (of the test program)\[14\]:

1. Ensure that there is no break in the packages installed earlier and the dependencies are installed properly. A yml file is created for the purpose of testing the version of the dependencies installed and whether they are suitable for running eChronos or not? : e.g. running 3.4 version of python needs to be verified.

2. \( /x.py \) build packages executes \( x.py \) file which uses the skeleton of the system as a reference for the order of installation. The following output files will be produced by \( x.py \):
   - release/prj–<version>.zip
   - release/<rtos–foo>–<version>.zip
   - release/<build–name>–<version>.zip

3. If the installation shows any error related to traceback like Traceback (most recent call last):

   File "prj/app/prj.py", line 1293, in start sys.exit(main()), then the installation or dependencies are not installed properly. Follow the earlier steps again properly.

4. After prj errors are removed, we have to ensure that the class standard cfg.py should contain the RISC-V architecture. Simultaneously, spike\[10\] emulator is installed. The test_setup.sh script downloads the package eChronos from Github. It contains travis to ensure that if package is missing then the alternative can be downloaded i.e. the posix version\[14\].

5. Components folder:
   - api-conditions, context-switch-RISC-V, docs, error, interrupt-event-RISC-V, message-queue, rigel, rigel.py, stack-RISC-V, task, timer-RISC-V are the necessary components that will be created once the script runs properly.

6. After ensuring a proper installation of eChronos, we test our sample program. prj/app/prj.py build <example_name> command runs the test case on eChronos RTOS and produces the binary file which can be tested on spike.

7. The block "Test case runs" is explained in detail in section 4.1.3.

3.1 Challenges encountered in porting

Porting requires the understanding of the flow of data and the subsequent changes in the system related to architecture. As eChronos is architecture dependent, there were many changes pertaining to specificity of the architecture like:
Porting of eChronos RTOS on RISC-V Architecture

General architecture similar to 8086 consists of extra data segment by default, but in case of RISC-V architecture, it has to be declared explicitly. The default edata (extra data segment) initialization is missing from RISC-V architecture so the edata declaration had to be removed from every file in eChronos. Likewise, there were some architecture dependent terms which had to be modified, so as to provide support to eChronos for RISC-V.

4 Step-wise porting of eChronos on RISC-V

eChronos initially could run only one program (test case) i.e. concurrency of task A and task B. eChronos could not run any generic program like “Hello World”. Porting eChronos on RISC-V, thus became difficult because RISC-V cannot support the execution of concurrent programs. So porting eChronos on RISC-V meant that we have to change the test case to a generic one which RISC-V can support. Thus, eChronos was first changed to support generic programs like "Hello World" and then the subsequent execution of its exe file on the RISC-V could intimate whether eChronos is ported successfully or not.

4.1 Changing test case in eChronos

Hit and trial method of porting The components section of eChronos consists of libraries like mutex, context switching and other concurrency supportive packages which are not used by our sample program. We removed all the unnecessary packages and removed their declarations from all the files like x.py core configuration, prj.py file because "build packages" command would take unnecessary time executing irrelevant packages otherwise. After ensuring correct set of packages like rigel, api-conditions, errors, doc etc. we try to modify the test case. Test case has only one external dependency i.e. print statement. "printf" could be used as one of the options but then gcc support for eChronos needs to be ensured which leads to multiple dependency issues and these issues might be difficult to track. Also, we need to port eChronos with minimal set of library dependencies and thus, we configured the print function by using write() command of stdio library which is comparatively a less complex function than printf function of gcc. Thus, a test program with least dependency is programmed and now, we have to produce its executable file to ensure that every interlinked package is working properly. This implies that if its executable file is generated, then removal of unnecessary packages was a success plus the test case is running properly on eChronos else we have to again solve the package error and keep on trying(hit and trial). Further, if risc-v linker along with this executable file, generates a system dump (which executes properly on spike too) then eChronos is successfully ported on RISC-V.

Initialization of packages The main principle of porting is to understand what lines of code to modify in accordance with the architecture and what dependencies needs to be taken into consideration. In this case the prj tool
written in python is the initial script which initializes all the packages present and creates the required directories. When prj tools runs in eChronos, project.prj is the skeleton file which runs x.py file. It states all the dependencies of packages that is required by the system to function properly. There are many components like errors, api-conditions etc which are addressed by eChronos and needs to be initialized. x.py helps in initialization of these packages.

x.py build packages
The command ./x.py will initialize the packages that are mentioned in skeleton of your system in x.py file. For instance: For RISC-V, rigel is the system name which has packages like error, test case etc. mentioned in x.py file, which helps in initial creation of sub-directories. This helps to create the build structure in a modular fashion where every module consists of .exe files of different packages initialized in x.py file.

Running an application on eChronos prj/app/prj.py build machine-RISC-V-common.example.hello is the command that runs the test case by first creating an exe file of the test case. After creating .exe files of packages using build command, we run test case using these packages. This exe file created by OS is architecture dependent and may raise some errors if OS files are corrupted or not ported correctly.

Fig. 3. machine-riscv-common.example.hello.prx
Test case is stored in the hello.c file. machine-RISC-V-common.example.hello.prx consists of skeleton of how the test case should run as shown in Fig3. It consists of the modules names which needs to be executed in the sequential order. This command searches for .prx file which contains all the files to be used for running your program stored in the system.

We will illustrate this using our model rigel.

1.) .prx file instructs the system to compile debug.c in generic folder, hello.c in generic folder, default-linker.py in RISC-V folder and build.py as mentioned in machine-RISC-V-common.example.hello.prx file.

2.) RISC-V.default-linker means that we should go to the RISC-V folder and run default-linker.py file. One thing must remembered that only .c, .py and other high level language files can run in the .prx file.

**Data flow of a running application** This section tries to explain the data flow in eChronos, when a test case run. The file "debug.h" consists of initialization of function : debug_print and debug.c consists of its declaration. The hello.c i.e. the test case uses debug.h as its header file and uses the function debug_print to print "Hello world". This requires the compilation of header files.

1.) build.py file takes the system files and some other helper files like debug.h to compile, assemble and run your hello.c file in generic folder.

2.) hello.c file just wants to print "Hello World". So for printing the command printf is not used, rather we have created the debug.c file where the print command has been declared. printf command is not used because it is a part of gcc library which is yet not ported to RISC-V. So a generic print statement is declared in debug file.

3.) The compilation of all libraries is over. Rigel model along with its components is build and the libraries used in the test case are also compiled. Only proper linking of all these files is left. The linker file default.ld is created where the linking occurs according to RISC-V architecture. Linker file of different architectures was referred while making default.ld. This linker file assumed "edata" one of the variables to be declared by default but RISC-V does not support any default declarations. So we changed "edata=null" and linking errors were solved. Thus, all the compiled files were linked.

### 4.2 Running test case on spike(RISC-V emulator)

As soon as you hit the first command, the out folder is created with rtos-<systemname> folder. Continuing further, if the second command runs with no error then the system image will be created in the <program – name> folder. This, then needs to be executed on your respective architecture as in our case it is on spike, RISC-V emulator[710].
5 Results

Running the system dump of hello.c file gave an output: "Hello World" assuming the starting address of execution of program was 10000 on the architecture. RISC-V emulator[7] has been designed in such a way that the address for the program needs to be specified above 10000 only. But its just a design issue which will not be of any problem in the real chip SHAKTI[11]. This indicates that the executable file produced by eChronos successfully ran on spike(RISC-V emulator). The output of sample program on eChronos is available (open source)[10].

Additions of any critical programs will be just a further extension of ported Hello World program provided the RISC-V supports that functionality of the program. Supposedly, a program which needs to determine the shortest path needs to be ported on RISC-V using eChronos. Program would consist of the same logic but instead of using gcc functions we will be using generic functions as seen with print in debug.h. This ensures a safe porting technique with no dependency on outer(alien) packages. Thus, eChronos is ported for RISC-V, for the base program hello world. Any additions to eChronos will be an extended version of the ported hello.c file with some extra headers files(declaring some predefined functions).

6 Conclusion

eChronos real-time operating system is ported to the RISC-V architecture and successfully executed on spike. The sample program hello.c has only one external dependency i.e. print. This is the base level porting for RISC-V that can be used as a reference for further adaptability of complex programs. Extensive porting of libraries in eChronos can be done by modifying the files in the same way as the sample program file[15].

References

1. Andrew Waterman, Yunsup Lee, D.P.K.A.: The risc-v instruction set manual, volume i: Base user-level isa. Tech. rep., UCB/EECS-2011-62, EECS Department, University of California, Berkeley (May 2016), https://www2.eecs.berkeley.edu/Pubs/TechRpts/2011/EECS-2011-62.pdf [Online; last accessed 27-May-2019]
2. Andrew Waterman, Yunsup Lee, R.A.H.C.D.P.K.A.: The risc-v instruction set (Aug 2013), http://www.hotchips.org/wp-content/uploads/hc_archives/hc25/HC25-posters/HC25.26.p70-RISC-V-Warterman-UCB.pdf
3. Andronick, J.: echronos rtos (Jan 2018), https://ts.data61.csiro.au/projects/TS/echronos/ [Online; last accessed 30-Dec-2018]
4. Bradbury, A.: The future of operating systems on risc-v (May 24, 2019), https://www.infoq.com/presentations/risc-v-future/ [Online; last accessed 24-May-2019]
5. H Marcondes, AS Hoeller, L.W.A.F.: Operating systems portability: 8 bits and beyond. vol. 50, pp. 124–130. 2006 IEEE Conference on Emerging Technologies and Factory Automation, IEEE (Sept 2006).
https://doi.org/10.1109/ETFA.2006.355371 [Online; last accessed 23-Dec-2018]

6. Holothurion: Porting (22 July 2019), https://en.wikipedia.org/wiki/Porting [Online; last accessed 23-July-2019]

7. Johnson, D.: Porting hyperkernel to the arm architecture. Tech. rep., University of Washington-CSE (2017), https://pdfs.semanticscholar.org/bb86/ea6a08c9b8c09a60036785b27aceff710d.pdf.https:// [Online; last accessed 2-Jan-2019]

8. June Andronick, Corey Lewis, C.M.: Controlled owicki-gries concurrency: reasoning about the preemptible echronos embedded operating system. pp. 10–24. MARS 2015 (2015). https://doi.org/10.4204/EPTCS.196.2 https://arxiv.org/abs/1511.04170

9. Kanter, D.: Risc-v offers simple-modular isa. Tech. rep., The Linley Group MICROPROCESSOR (March 2016), https://riscv.org/2016/04/risc-v-offers-simple-modular-isa/ [Online; last accessed 3-Jan-2019]

10. Keller, B.: Risc-v, spike, and the rocket core (Fall 2013), http://www-inst.eecs.berkeley.edu/~cs250/fa13/handouts/lab2-riscv.pdf [Online; last accessed 27-Dec-2018]

11. N. Gala, A. Menon, R.B.G.S.M.V.K.: Shakti processors: An open-source hardware initiative. 29th International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems (VLSID), Kolkata, India., IEEE (Jan 2016). https://doi.org/10.1109/VLSID.2016.130 [Online; last accessed 13-Dec-2018]

12. RIOT-OS: Family:arm.riot-os (Mar 27, 2017), https://github.com/RIOT-OS/RIOT/wiki/Family:-ARM [Online; last accessed 7-Jan-2019]

13. RISC-V: Risc-v gnu-toolchain (2017), https://github.com/riscv/riscv-gnu-toolchain [Online; last accessed 4-April-2019]

14. eChronos RTOS: The echronos real-time operating system (2017), https://github.com/echronos/echronos [Online; last accessed 4-April-2019]

15. Shubhendra Pal Singhal, M.S.: Porting of echronos rtos on risc-v architecture. preprint at (2019), https://arxiv.org/abs/1908.11648

16. Singhal, S.P.: Porting and testing on risc-v (2018), https://github.com/singhalshubh/Porting-and-Testing-on-RISCV- [Online; last accessed 3-Jan-2019]