A new closed-loop multi-level Class-D amplifier employing a fourth-order 'continuous-time sigma-delta modulator' is proposed and analysed. The proposed amplifier is intrinsically linear and it has approximately the fixed 'total harmonic distortion plus noise' against the input frequency. The corresponding circuit is designed and simulated in 180 nm technology (3.3 V), while the post-layout model of the power stage is employed. A total harmonic distortion plus noise of 0.0016%, the quiescent current of 2.6 mA, the maximum efficiency of 94%, the average switching frequency of 400–500 kHZ and an excellent 'power supply rejection ration' of 120 dB are achieved.

Introduction: The closed-loop Class-D amplifiers including 'pulse width modulation (PWM)' suffer from inherent non-linearity [1–5], such that unlike linear amplifiers, the higher loop-order cannot reduce the distortion levels [5]. The high-frequency ripples of the switching signal are resampled in the PWM section which makes PWM-residual-audisng distortion [1, 5]. To cancel this error, several solutions including an additive pulse-train in feedback path [1], the combination of 'sigma-delta (SD)' and PWM techniques with a 17-level voltage quantiser and digital time-quantised PWM [2], and a low-pass filter in feedback path [3] are introduced. All these techniques add a challenging calibration circuit [1–3] to alleviate the inherent linearity problem of three-level closed-loop PWM. Besides, a challenging design of loop-filter is needed to achieve a Power Supply Reject Ratio (PSRR) of better than 100 [3]. The 'phase-shifted carrier-modulated' multi-level Class-D amplifiers offer a calibration-free circuit [4]. However, in these amplifiers, like the three-level ones, the triangular wave generators and fast static comparators are required, and the total harmonic distortion plus noise (THD + N) increases by the second power of the input frequency.

This paper replaces the PWM-based loop by continuous-time SD modulator (CT-SDM) to guarantee an inherent linear operation, while a five-level (four-leg) power stage is employed to improve the dynamic range in a moderate switching frequency. The proposed combination, for Class-D amplifiers, obeys the classical linear amplifiers design-theory in which the higher loop-gain leads to the lower distortion. Hence, unlike all three-level conventional second-order PWM-based amplifiers, a fourth-order loop-filter is employed here, which suppresses extrinsic non-linearity and improves the PSRR. The static comparators and the triangular wave are replaced by the dynamic comparators and the square wave, respectively.

System-level analysis and design: Figure 1 shows the system-level schematic of the proposed multi-level Class-D amplifier. A CT-SDM is employed in this design, while R-C variations of the fabrication process, can be addressed by sampling frequency adjustment. The error signal of the loop \((v_o(t) - v_{OBS}(t))\) is processed in the loop-filter and then it is sampled and quantised by an \((N + 1)\)-level quantiser at \(f_s\), \(N\) digital outputs of the quantiser excite \(N\) power switches and prepare \((N + 1)\)-level output power signal, \(v_o(t)\). The output signal is fed back to the loop-filter through an optional attenuator. For a busy (i.e. rapidly and randomly varying) input signal, the two-sided power spectral density of the quantisation noise of an \((N + 1)\)-level quantiser is \(\sigma^2_w = (V_{FS}/N)^2 / (12 f_s \pi)\) [5], where \(V_{FS}\) is the full-scale voltage of the quantizer. A high-order multi-level SDM eliminates the correlation between the quantisation error and the input signal [5], such that a linear analysis of the Class-D amplifier with the additive white noise of the quantiser is permitted [5]. As shown in Figure 1, the inner feedback path (gain of \(k'\)) compensates the excess loop delay caused by limited gain-bandwidth of amplifiers, the delay of both quantiser and the power stage. For the sake of simplicity, the effects of delays and compensation path are ignored. The ‘noise transfer function (NTF)’ of Figure 1 is equal to

\[
NTF(s) = \frac{s^2 + k_4 f_s s + (k_4 + \xi) f_s^2 + (k_4 + \xi k_4) f_s^3 + k_4 f_s^4}{s^2 + k_4 f_s s + (k_4 + \xi) f_s^2 + (k_4 + \xi k_4) f_s^3 + k_4 f_s^4}
\]

Corresponding to Figure 1, \(k_4 = a_1^2\). The local feedback of the first two integrators (through the gain of \(\xi\)) provides a resonator. According to (1), two zeros of NTF are migrated from origin into the band of interest. The in-band quantisation noise of the modulator can be achieved by multiplying \(\sigma^2_w\) and (1), and then integrating over the frequency range of \([-BW, BW]\), where, \(BW\) is the bandwidth. As \(f_s > 2BW\), the NTF has a low-frequency approximation of \(NTF(f) \approx (2\pi f)^2 (2\pi f^2 + \xi f^3 + k_4 f_s^4)\). In this way, the in-band quantisation noise of sixth-order modulator is equal to

\[
IBN_6 = \frac{V_{FS}^2 \pi L}{12 \times (2L + 1) \times k_4^2 N^2 (L - 0.5)^2 \times OSR^{2L+1}}
\]

where \(OSR\) is the oversampling ratio equal to \(f_o/\pi(2\times BW)\). The resonator (gain of \(\xi\)) decreases the \(IBN_6\) by \((L - 0.5)^2\) for \(L > 2, k_4\) is equal to \(\frac{2 \times N}{12 L + 1}\) [5], where \(L\) is the modulation index \((\|k_4\| < 1)\). \(\alpha_{ELD}\) is a constant term depending on \(L, N\) and the excess loop delay (related to \(T_d\)). \(\alpha_{ELD} = 1.15\) for \(L = 4\) and \(N = 4\), which leads to \(k_4 = 0.044\), for \(L = 0.8\).

The errors of power stage (unbalance rising and falling times, the error of dead time and the clock jitter error) are added in the forward path, where any error is shaped by NTF. The main part of permitted noise power is devoted to thermal noise and only 10–15% of the noise floor can be occupied by quantisation noise. This means that, for a 16-bit Class-D amplifier, the in-band quantisation noise must be less than \(-108\) dBFS\(\rightarrow -106\) dBFS (dB related to full scale).

Three system-level parameters of \(N, OSR\) and \(L\) can be designed to achieve the targeted quantisation noise. The parameter \(N\) determines the number of inductors, half-bridges and drivers. Considering practical implementations of Class-D amplifiers [4] a five-level output \((N = 4)\) is assumed in future analysis and design. The switching frequency and so the dynamic power consumption of the power stage is proportional to \(OSR (f_s/2BW)\) which should be limited. As shown in (2), the higher order of the SDM \((L)\) leads to less in-band quantisation. On the other hand, while the number of quantisation levels is limited \((N = 4)\), the stability considerations force less aggressive noise shaping (lower \(L\) or lower \(k_4\)).

Considering relation (2), using the Schreier toolbox [5], and performing vast system-level simulations, a fourth-order SDM, \(L = 4\), a maximum modulation index of \(\|k_4\| = 0.8\) \((k_4 = 0.044)\), an OSR of 40 \((f_s = 1.6\ MHz)\) are selected for an \(IBN_6 = -107\) dB and \(V_{FS} = 3.3\ V\). The coefficients \(k_4, k_3\) and \(k_2\) are designed for stability consideration by the Schreier toolbox. The system-level parameters are reported in Table 1.

### Table 1: System-level parameters values (Figure 1)

| Parameter | Value   |
|-----------|---------|
| \(k_1, k_2, k_3, k_4\) | 0.045, 0.3557, 0.3, 0.94, 1.53 |
| \(k', \xi\) | 0.35, 0.0048 |

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Five-level class-D amplifier employing fourth-order continuous-time sigma-delta modulator

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Fig. 1 System-level model of proposed Class-D amplifier
Considering Tables 1 and 2, noise floor is devoted to the clock jitter noise and the power-stage errors. Capacitive local feedback, including resistive feedback is required. Due to the very small value of \( \Omega \) of Figure 1, to implement the local feedback path, \( 1/2 \) gives the other circuit-level parameters \( 10 \) and using (3), \( a_{i1} \). Also, the output signals of half-bridges and their inverted versions are feed-backed through a capacitor set to the last integrator (\( k^t \) of Figure 1). Although one or two OTAs can implement the fourth-order loop-filter, using four OTAs, a more robust design against circuit non-idealities is formed. A 'chain of integrators with weighted feedforward summation (CIFF)' is used to reduce the voltage swing of three first OTAs [5]. In this way, the first three OTAs process only the quantisation noise. The load, respectively. Each half-bridge carries half current of the power stage. The outputs of two upper/lower comparators are digitally multiplexed between two upper/lower half-bridges every \( M \) sampling period (e.g. \( M = 8 \)), to avoid any potential current circulation between inductors.

The output signal of rth half-bridge, \( v_{oi} \), is fed back through a resistor to the first integrator. While one side is active, the other side is OFF and generates a zero-output voltage. Therefore, the feedback signal injects unbalance common-mode voltage to the differential inputs of both first and last integrators. To alleviate this problem, all half-bridges outputs are inverted and fed back to input ports of the first and last integrators. The combination of these four signals does not include the input-signal content and just balance the common-mode voltage of differential inputs. Furthermore, this technique enhances the PSRR of the whole amplifier. According to Figure 2, all the feedback paths of the first integrator are added passively and then injected into the first integrator through \( R_{B1} \), while \( R_{B2} = 2R_{b1}/10, R_{B3} = 4R_{b1}/10 \) and \( R_{B4} = 4.5R_{b1}/10 \). Also, the output signals of half-bridges and their inverted versions are feed-backed through a capacitor set to the last integrator (\( k^t \) of Figure 1).

Although one or two OTAs can implement the fourth-order loop-filter, using four OTAs, a more robust design against circuit non-idealities is formed. A 'chain of integrators with weighted feedforward summation (CIFF)' is used to reduce the voltage swing of three first OTAs [5]. In this way, the first three OTAs process only the quantisation noise.

The load-integrator benefits from the third-order shaping of three first integrators. The main-path gain, \( k_1 \), is distributed among three first integrators, \( k_1 = k_3 \), to reduces the capacitive load of the first OTA. The voltage swings of the three first integrators are designed for moderate values satisfied by a one-stage folded-cascode OTA of Figure 3(a). According to Table 3 and Figure 2, the three first OTAs have capacitor loads, \( C_{e1} \), of \( C_{e1} = C_{e3} = 29.67 \text{pF} \), \( C_{e2} = 10 \text{pF} \) and \( C_{e3} + C_{e7} + C_{e8} = 10.25 \text{pF} \), respectively. The system-level simulations show that the first OTA requires a \( 0_0 = 2\pi \times f_s \), and three other OTAs need a \( 0_0 = 2\pi \times 2f_s \). The first OTA is designed with a current budget of 772 \( \mu \text{A} \), while the second and third OTAs are linearly scaled. Considering Figure 3(a), for three first OTAs, the gain-bandwidth is equal to \( 0_1 \approx \omega_{0p1}/C_{e1} \), where \( \omega_{0p1} \) is the transconductance of \( M_{e1} \). Usually, the current budget of folded-cascode OTA, \( I_{0e} \), is equally divided between its four legs [6]. The size of the input transistors is \( (W/L)_{in} = \omega_{0p1}/(2Q_{pC_wC_b}/4) = 2\omega (C_{e22}/Q_{pC_wC_b}) \). The overdrive voltages, \( V_{od1} \) of \( M_{e1} \) and \( M_{e1}-a \) are determined by the output voltage swing, and their size is \( (W/L)_{in}/2 = 2\omega_0/(3Q_{pC_wC_b}V_{od1}^2) \).

**Table 3. Circuit-level parameters values (Figure 2)**

| Parameter | Value | Type |
|-----------|-------|------|
| \( R_{IN1} \), \( R_{IN2} \), \( R_{IN3} \) \((k\Omega)\) | 68, 600, 600, 600 | Poly resistors |
| \( R_{FB1}, R_{FB2}, R_{FB3} \) \((k\Omega)\) | 30.6, 13.6, 27.2 | Poly resistors |
| \( C_{e1}, C_{e2}, C_{e3}, C_{e4} \) (pF) | 25.84, 2.9, 2.9, 1.04 | MIM-cap |
| \( C_{FB1}, C_{FB2}, C_{FB3} \) (pF) | 6.65, 7.13, 3.83 | MIM-cap |
| \( C_{B1}, C_{B2}, C_{B3} \) (pF) | 667, 182, 91 | MIM-cap |
| \( L, C_i, R_i \) | 60 \( \mu \text{H} \), 1 \( \mu \text{F} \), 8\( \Omega \) | Off-chip |

**Fig. 2 Circuit-level implementation of the proposed Class-D amplifier**

**Fig. 3 The designed OTAs for loop-filter of the proposed amplifier: (a) folded-cascode OTA employed in three first integrators with CMFB; (b) two-stage and Miller-compensated OTA used in the fourth integrator [6]**
The last OTA requires $0.8 \times V_{dd}$ maximum voltage-swing implemented by two-stage Miller-compensated OTA (Figure 3(b)). This OTA is designed with a current budget of $I_c = 93 \, \mu A$ for a 1.04 pF load. For symmetric slew rate, $C_t$ is selected equal to $C_L$ and the current budget of OTA is shared corresponding to Figure 3(b) [6]. The gain-bandwidth is $245 \, mW$ and the dimension of the input transistors is $(W/L)_p = 2 g_{mp} / (2 g_{mp} C_{ox} / 6) = 3 \omega_2 C_{ox} / (\mu_c C_{ox} h_0)$. The dimension of $M_{2,1,2}$ is $\mu_c / h_p$ times smaller than $M_{1,1,2}$. For a given voltage swing, the $V_{out}$ of the second stage is determined and the sizes of $M_{3,1,4}$ and $M_{4,1,4}$ is $(W/L)_p/3 = 2 h_p / (3 g_{mp} / C_{ox} V_{dd})$.

Four dynamic comparators quantize the output signal of the loop-filter, $V_{out}$. According to Figure 2, the dynamic comparators are excited by a square-wave sampling clock at the frequency of $f_{SCLK} = 1.6 \, MHz$. According to Figure 4(a), the dynamic comparator includes a preamplifier, a latch and an Set-Reset (SR)-latch. The SR-latch is designed for the minimum dimensions. The latch time is $t_{th} = (g_{mp} + g_{mn}) \times \ln(V_{th} / (k + 1) V_t) / (g_{mp} + 4 g_{mp} / 3) V_t$ [5], where $C_t$ is the parasitic capacitor, $g_{mp}$ and $g_{mn}$ are the transconductance of $M_{4,1,4}$ and $M_{5,1,4}$, and $V_t = (k + 1) V_t$ are the initial and final voltages of latch in the $k$th sampling period. The final voltage of latch is $V_{FS}$ and the minimum input voltage of comparators, in five-level quantiser, is $(V_{FS}/4)/2$, amplified by the preamplifier gain of $g_{mp}/g_{mn}$. Considering the reset time of $T_{reset} = (g_{mp} + 4 g_{mp} / 3) V_t < T_{reset}$ is achieved for the latch time. The dimensions of $M_{3,1,4}$ and $M_{4,1,4}$ are a trade-off between the maximum values of $g_{mp}$ and $g_{mn}$ and minimum value of $C_t$ achieved by simulation. $M_{3,1,4}$ need a large $L$ and a minimum $W$, while $M_{4,1,4}$ should have minimum $L$ and a reasonable $W$. Both PMOS and NMOS transistors of each half-bridge, respectively, have a channel width of 28 and 7.2 mm and a channel length of 300 and 350 nm, resulting in an ON-resistance of 180 mΩ.

There are two half-bridges on each side of the load and the whole power stage has an area of 0.287 mm². The power driver of each half-bridge excites the NMOS and the PMOS transistors individually by a chain of inverters, tapered by a one-third coefficient (Figure 4(b)). Com-\br comparators plus noise (THD + N) of the proposed amplifier for $P_{out} = 245 \, mW$ for two input frequencies of $f_{in} = 1.6525 \, kHz$ and $f_{in} = 6.25 \, kHz$

The power supply rejection is tested by applying a 200 mV peak-to-peak disturbance voltage on the supply and a 60 dBFS input signal. For different disturbance frequencies, 100 Hz–17.97 kHz, the disturbance tone is under the noise floor, and PSRR is better than 120 dB.

The simulation results (with the post-layout model of the power stage) show a power efficiency of 94% at $P_{out} = 403.5 \, mW$ ($\lambda = 0.77$) and THD $+ N$ (%) = 0.0032%. As stated before, depending on the polarity of $V_{out}$, two of four half-bridges are OFF. In the active section, on average only one of two half-bridges changes its previous state at the sampling moment. Figure 6(b) shows the average switching frequency versus the output power which is 400–500 kHz, while $f_s = 1.6 \, MHz$.

Figure 7 illustrates the output ‘power spectral density (PSD)’ of the proposed amplifier for two input frequency of 1.5625 and 6.25 kHz, and $P_{out} = 245 \, mW$ (corresponding to minimum THD $+ N$). For 1.5625 kHz input, before saturation of the last OTA, the PSD of the amplifier is distortion free, while for 6.25 kHz input the third harmonic is 104.4 dB lower than the main tone. Also, the amplifier has approximately the same THD $+ N$ for both frequencies. Table 4 compares the simulation results of this paper with the state-of-the-art results.

Conclusion: A new version of multi-level Class-D amplifiers with a CT-SDM is proposed for BTLs as a suitable alternative for PWM-based closed-loop Class-D amplifiers. Unlike PWM-based amplifiers, the THD of the proposed amplifier is approximately fixed in the whole

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**Fig. 4** The intermediate circuit between loop-filter and power stage: (a) dynamic comparator including preamplifiers followed by SR-latch; (b) power driver of half-bridge including dead-time generator (bi-stable)

**Fig. 5** Total harmonic distortion plus noise (THD + N (%)) versus output power at $f_{in} = 1.5625 \, kHz$

**Fig. 6** Circuit-level simulation results: (a) total harmonic distortion plus noise (THD + N (%)) versus input frequency for $P_{out} = 245 \, mW$ ($\lambda = 0.6$); (b) average switching frequency versus the output power (mW)

**Fig. 7** The output PSD corresponding to minimum total harmonic distortion plus noise (THD + N) for $P_{out} = 245 \, mW$ for two input frequencies of $f_{in} = 1.6525 \, kHz$ and $f_{in} = 6.25 \, kHz$
Table 4. Simulation results compared with state-of-the-art results

|                      | This work | [1]  | [2]  | [3]  |
|----------------------|-----------|------|------|------|
| Min. THD (%), min    | <0.0005,  | 0.0008, | 0.00066, | 0.004, |
| THD + N (%) (@ 1 kHz)| 0.0016    | 0.0009 | 0.00078 | 0.005 |
| Peak efficiency (%)  | 94        | 92.2  | 91    | 91   |
| \(f_s\) (kHz)        | 400–500   | 168   | 2000  | 400  |
| \(I_q\) (mA)         | 2.6       | 0.41  | –     | 3    |
| PSRR (dB)            | 120       | 99    | –     | >100 |

The proposed amplifier tends to linear amplifiers such that no linearisation technique is required. However, compared to conventional amplifiers, the proposed amplifier has a higher quantisation noise, reduced by higher loop-order and higher sampling frequency. Both higher order and higher sampling frequency propel the amplifier to the linear category more tightly. The switching frequency of this amplifier is one-fourth times of its sampling frequency comparable to the switching frequency of PWM-based amplifiers. The simulation results show a 2.6 mA quiescent current, 0.0016% minimum THD + N and efficiency of 94%, for an 8Ω BTL, while the post-layout model of power stage is used.

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References
1 Chien, S., et al.: A 0.41 mA quiescent current, 0.00091% THD + N class-D audio amplifier with frequency equalization for PWM-residual-aliasing reduction. IEEE International Solid-State Circuits Conference – (ISSCC), San Francisco, CA, pp. 352–354 (2020)
2 Karmakar, S. et al.: 23.4 A 28W −108.9dB/−102.2dB THD/THD + N hybrid SD-PWM class-D audio amplifier with 91% peak efficiency and reduced EMI emission. IEEE International Solid-State Circuits Conference – (ISSCC), San Francisco, CA, pp. 350–352 (2020)
3 Ge, T., et al.: A direct battery hookup filterless pulsewidth modulation class D amplifier with >100 dB PSRR for 100 Hz to 1 kHz, 0.005% THD + N and 16 μV noise. IEEE Trans. Power Electron. 35(1), 789–799 (2020)
4 Schinkel, D., et al.: A multiphase class-D automotive audio amplifier with integrated low-latency ADCs for digitized feedback after the output filter. IEEE J. Solid-State Circuits 52(12), 3181–3193 (2017)
5 Pavan, S., Schreier, R., Temes, G.C.: Understanding Delta-Sigma Data Converters, 2th edn. Wiley, New York (2017)
6 Razavi, B.: Design of Analog CMOS Integrated Circuits, 2nd edn. McGraw-Hill, Boston, MA (2017) https://www.amazon.com/Design-Analog-Cmos-Integrated-Circuit/dp/938706784X