The effect of interface trapped charges in DMG-S-SOI MOSFET: a perspective study

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Received 29 September 2014
Accepted for publication 21 October 2014
Published 27 November 2014

Abstract
In this paper, the existing two-dimensional (2D) threshold voltage model for a dual material gate fully depleted strained silicon on insulator (DMG-FD-S-SOI) metal-oxide-semiconductor field effect transistor (MOSFET) is modified by considering the interface trapped charge effects. The interface trapped charge is a common phenomenon, and this charge cannot be neglected in nanoscale devices. For finding out the surface potential, parabolic approximation has been utilized and the virtual cathode potential method is used to formulate the threshold voltage. The developed threshold voltage model incorporates both positive as well as negative interface charges. Finally, validity of the presented model is verified with 2D device simulator Sentaurus™.

Keywords: dual material gate (DMG), strained Si, interface trapped charge, silicon on insulator (SOI)
Mathematics Subject Classification: 2.07, 3.02, 4.13, 6.01

1. Introduction
The feature sizes of metal-oxide-semiconductor field effect transistors (MOSFETs) are being continuously decreased to increase the packing density, as very large scale integration technology advances. However, the short channel effects (SCEs) are posing serious threats for further scaling to follow the ITRS roadmap [1]. For a bulk MOSFET, continuous scaling requires increasing the channel doping to achieve a lower junction electric field in the channel. Also, the higher doping ensures the non-overlap of the source and drain depletion widths in the channel region. However, a serious amount of mobility degradation occurs because of impurity scattering in the high channel doping region [2]. To encounter this problem, various new structures with different engineering concepts have been reported to reduce the SCEs in SOI platform. Among them, strain engineering is very popular for enhancing the carrier mobility [3, 4]. Strained Si provides device performance enhancements through changes in material properties rather than changing device geometry and doping.

The conventional method of producing strained-Si is growing pseudomorphic Si epitaxial layer on relaxed SiGe alloys. By increasing the Ge content of the relaxed SiGe alloy, the amount of biaxial strain, and therefore, the magnitude of the mobility is enhanced [5–8]. However, as the Ge content is increased, the critical thickness (the thickness to which the strained-silicon can be grown without inducing misfit dislocations to alleviate the strain) is reduced. Single layer strained-silicon-on-insulator (S-SOI) is a new SiGe-free material system that combines the carrier transport advantages of strained-Si with the reduced parasitic capacitance and improved MOSFET scalability of thin-film SOI MOSFET. The single layer S-SOI is less susceptible to misfit dislocation induced leakage current while maintaining increased carrier mobility [9–11].

For the first time, Kumar et al [9] proposed a simple analytical model of threshold voltage for single layer FD-S-SOI MOSFET in 2006. They had shown the dependency of various parameters such as Ge mole fraction (X), strained silicon thickness (tSi) and doping concentration on the threshold voltage. Jin et al [12] proposed a two-dimensional (2D) threshold voltage model for DMG strained SOI MOSFET. They have discussed how effectively the device was able to suppress the hot carrier effects (HCEs) and threshold voltage roll-off. Similarly, the effect of double layer strain (i.e. strained silicon on SiGe relaxed layer) has been discussed by Bhusan et al [2]. They have also discussed the improved
which is elaborated in appendices A and B, respectively. A potential method is used for modeling the threshold voltage to formulate the surface potential and further virtual cathode potential, electric field, and threshold voltage of the DMG-FD-S-SOI MOSFET. The electric field saturation (velocity saturation), and transverse fields are considered at room temperature in the simulation.

In this work, the previously existing analytical model for surface potential, electric field, and threshold voltage for a dual material gate fully depleted strained silicon on insulator (DMG-FD-S-SOI) is modified with including the effects of interface charges. The interface charges are considered both in magnitude and polarity with an assumption that the charge distribution is uniform along the channel. Parabolic approximation method is used for solving the 2D Poisson’s equation to formulate the surface potential and further virtual cathode potential method is used for modeling the threshold voltage which is elaborated in appendices A and B, respectively. An extensive analysis is carried out to study the effect of various parameters such as Ge mole fraction, drain bias, gate length ratio variation, and interface charge variation on surface potential, electric field, and threshold voltage.

Along with the introduction, section 2 describes the device structure description that includes all the dimensions, materials and doping concentrations of DMG-FD-S-SOI MOSFET. This section also analyses the physics of the device using device numerical simulations and models activated for simulation. Section 3 comprises the modeling of surface potential, electric field, and threshold voltage. The impact of numerous device parameters on the surface potential, electric field, and threshold voltage of the DMG-FD-S-SOI MOSFET is discussed in section 4. Finally, the concluding remarks in section 5 substantiate the novelty of the paper.

2. Device structure

The schematic diagram of the DMG-FD-S-SOI MOSFET structure used for modeling and simulation is shown in figure 1. The device has uniformly doped source–drain with doping concentration of $N_D = 1 \times 10^{20} \text{cm}^{-3}$. The channel is kept lightly doped with doping concentration of $N_A = 1 \times 10^{16} \text{cm}^{-3}$. The gate oxide thickness, buried oxide thickness and the silicon are $t_{ox} = 2 \text{nm}$, $t_b = 50 \text{nm}$ and $t_{si} = 10 \text{nm}$, respectively. The damaged region due to the interface oxide trap charges ($N_F$) is shown as a black line towards the drain side.

The gate length is divided into two parts as $L_1$ and $L_2$ for the use of two different gate electrodes. The work function of the gate material is: $\phi_{M1} = 4.8 \text{ eV}$ (e.g., Cu) and $\phi_{M2} = 4.6 \text{ eV}$ (e.g., Mo). The simulation is carried out by the device simulator Sentaurus, a 2D numerical simulator from Synopsis [13]. To study the surface potential along the channel we have taken the cutline at the surface of the channel thickness across the channel of the device. To obtain accurate results for MOSFET simulation we need to account for the mobility degradation that occurs inside inversion layers. The drift-diffusion model in default of carrier transport model in Sentaurus device is activated. The basic mobility model is used, which takes into account the effect of doping dependence, high-field saturation (velocity saturation), and transverse field dependence. The impact ionization effects are ignored. The silicon band gap narrowing model that determines the intrinsic carrier concentration is activated. The solution of the device equations are done self-consistently, on the discrete mesh, in an iterative fashion. For each iteration, an error is calculated and the device attempts to converge on a solution that has an acceptably small error. The Poisson equation, continuity equations, and the different thermal and energy equations are included in simulation [13]. All the structure junctions assumed as abrupt, and the biasing conditions considered at room temperature in the simulation.

3. Analytical model formulation

3.1. Surface potential formulation

The modeling of surface potential for DMG-FD-S-SOI MOSFET is adopted from Jin et al [12], however we have considered trap charge effects/damaged region near the drain side by modifying the flat band voltage at drain side as

$$\left( V_{FB2,f} \right)_{Si} = \left( V_{FB2,f} \right)_{Si} + \Delta V_{FB,f} - \frac{qN_F}{C_{ox}},$$

where $\left( V_{FB2,f} \right)_{Si} = \phi_{M2} - \phi_{Si}$. $(V_{FB2,f})_{Si}$ is the flat band voltage of strained-Si MOSFET in the front channel under M2 region. $(V_{FB2,f})_{Si}$ is the flat band voltage of bulk Si MOSFET in the front channel for M2 region. $\Delta V_{FB,f}$ represents the amount of change in flat band voltage due to strain. $N_F$ is the interface oxide charges in both dimension and polarity and $C_{ox}$ is the gate capacitance.

By considering $qN_F$, we have remodeled the existing surface potential, electric field and threshold voltage model [9, 12, 14] to know the effect of interface trapped charges on various performance parameters of DMG-FD-S-SOI MOSFET. Finally solving the Poisson’s equation using the predefined boundary conditions with a little modification of flat band voltage near the drain side, we obtained the surface potential as below [12]

$$\phi_{si}(x) = A \exp(nx) + B \exp(-n \times x) - \frac{q}{\alpha},$$
The detailed mathematical conditioning and solution of $\phi(x)$ and $\phi_2(x)$ are given in appendix A.

### 3.2. Electric field formulation

Electric field horizontal component under metal gates M1/M2 can be calculated by differentiating the potential with respect to $x$:

$$E_1(x) = An \exp(nx) - Bn \exp(-nx),$$

$$E_2(x) = Cn \exp(n(x - L_1)) - Dn \exp(-n(x - L_1)).$$

The minimum potential of front channel can be expressed as

$$x_{\text{min}} = \frac{1}{2n} \ln \left( \frac{B}{A} \right),$$

$$\phi_{s,\text{min}} = 2\sqrt{AB} - p_1.$$

Figure 2. Variation of surface potential along the channel length, (a) for various drain voltages, (b) for different Ge mole fraction (X). Parameters used $\phi_{\text{M1}} = 4.8$ eV, $\phi_{\text{M2}} = 4.6$ eV, $N_A = 1 \times 10^{16}$ cm$^{-3}$, $t_{\text{Si}} = 10$ nm, $L = 100$ nm, $t_{\text{ox}} = 2$ nm, and $V_{\text{GS}} = 0.1$ V.

Figure 3. Variation of surface potential along the channel length for different gate length ratios ($L_1/L_2 = 1:2, 1:1, 2:1$) considering (a) positive interface charge, (b) negative interface charge. Parameters used $X = 0.2$, $N_F = +5 \times 10^{12}$ cm$^{-2}$, $N_F = -5 \times 10^{12}$ cm$^{-2}$, $\phi_{\text{M1}} = 4.8$ eV, $\phi_{\text{M2}} = 4.6$ eV, $N_A = 1 \times 10^{16}$ cm$^{-3}$, $t_{\text{Si}} = 10$ nm, $L = 100$ nm, $t_{\text{ox}} = 2$ nm, $V_{\text{DS}} = 0.1$ V and $V_{\text{GS}} = 0.1$ V.

### 3.3. Threshold voltage formulation

$$V_{\text{th}} = -\eta + \frac{\sqrt{\eta^2 - 4n^2\xi}}{2\sigma}. \quad (8)$$

A generalized evaluation method of $V_{\text{th}}$ is presented in appendix B.

### 4. Results and discussion

In this section, results obtained from theoretical models of the surface potential, electric field and threshold voltage are compared with the numerical simulation results for DMG-FD-S-SOI MOSFET. Figure 2(a) demonstrates the surface potential curve along the channel length at various values of the drain voltage. Because of the presence of dual metal, the variation of channel potential under metal gate 1 (M1) with respect to drain voltage is quite small. The drain voltage is not absorbed under M1 as it is absorbed by metal gate 2 (M2), hence the channel under M1 is screened from the changes of drain potential. As a consequence, $V_{\text{DS}}$ has only a small influence on drain current after saturation. Also, due to the dual metal gate, the variation of channel potential minima with respect to drain voltage is quite small which minimizes the drain induced barrier lowering (DIBL).


**Figure 4.** Surface potential variation along the channel length for interface charge variations (in magnitude and polarity). Parameters used: \( X = 0.2, \phi_{M1} = 4.8 \text{ eV}, \phi_{M2} = 4.6 \text{ eV}, N_x = 1 \times 10^{16} \text{ cm}^{-2}, t_{ox} = 10 \text{ nm}, L = 100 \text{ nm}, \tau_{ox} = 2 \text{ nm}, V_{DS} = 0.1 \text{ V} \) and \( V_{GS} = 0.1 \text{ V} \).

The effect in figure 2(b), the calculated and simulated values of surface potential are plotted against the horizontal distance \( x \) for \( L = 100 \text{ nm} (L1/L2 = 1:1) \) at different values of effective Ge mole fraction \( X \) in the relaxed SiGe buffer. It can be seen that the potential barrier height is decreasing with increase in \( X \). As the threshold voltage is calculated from the minimum surface potential, it is very important to choose the appropriate value of threshold voltage for the device. The device having high threshold voltage is slower. Similarly, the device having low threshold voltage has more leakage current. So, for our convenience, from figure 2(b), the middle one is considered, i.e., \( X = 0.2 \) and the value is fixed to study the effect of other parameters on surface potential for a DMG-FD-S-SOI MOSFET.

Figures 3(a) and 3(b) depict the surface potential with the metal gate length ratio variations for positive charges and negative charges in the oxide interface, respectively. As seen from the figure, the increase in the length of metal gate nearer to drain, i.e. M2, raises the minimum surface potential and shifts it towards the source side. The position of the minimum surface potential is closer to source for a greater length of M2 region than lesser M2 length. This indicates a higher SCE in the device as the M2 extends more. This will further lower the source channel barrier height and hence a higher threshold voltage roll-off. However in the case of negative interface charges, the increase of the length of M2 region decreases the minimum surface potential. This will give a higher source-channel barrier height and hence a lower threshold voltage roll-off. The shifting of the minimum surface potentials is opposite to that in the positive interface charge case i.e. the minimum surface potential point shifts towards drain side as M2 length increases.

Figure 4 shows the surface potential variation along the channel length for different amounts and polarities of interface trapped charges in the oxide. From the figure, the minimum of the surface potential is at the channel center for the device having \( N_F = 0 \) and is moving towards the source and drain side, for positive and negative interface charge cases respectively. A positive interface charge case will obligate higher SCE on the device than its negative charge counterparts due to lower barrier height. However, the device having negative interface charges will cause more DIBL effect as the minimum potential point shifts towards the drain side. So both positive and negative interface charges are undesirable for the device performance.

**Figure 5(a).** The variation of electric field distribution along the channel at different values of effective Ge mole fraction \( X \). It is evident from the figure that the electric field at the drain side considerably reduces with increase in \( X \) value. This reduction of the electric field experienced by the carriers in the channel can be interpreted as the reduction of the HCE at the drain end. Figure 5(b) shows the variation of the electric field distribution along the channel for different amounts and polarity of interface trapped charges in the oxide. From the figure, the peak of the electric field lies at the interface of the two metal gates. The device having positive interface charge will give maximum electric field peak as compared to \( N_F = 0 \) and \( N_F \) negative cases. So, positive interface charge case will obligate higher SCE on the device than its negative charge counterparts due to high electric field.

**Figure 6(a)** shows the variation of threshold voltage with the channel length for different gate length ratios \( (L1/L2 = 1:2, 1:1, 2:1) \). It is observed that SCE become serious on decreasing the channel length ratios. That means the threshold voltage is higher for the higher control gate length i.e., length of M1. This is because of the higher channel barrier height for higher gate length ratio \( (L1/L2 = 2:1) \). This is attributed to the fact that the control gate (M1) loses its control over the channel at smaller length ratios. Figure 6(b) shows the threshold voltage variation along the channel length for \( N_F = 0, \) negative and positive in the oxide. From the figure, the threshold voltage is higher in case of \( N_F = 0 \) and it is lower for positive interface charge case. This is due to the lower barrier height in the case of positive interface charge. So, the device having interface trap charges is more prone to SCEs. The threshold voltage variation against channel length for different Ge mole fractions \( X \) can also be seen from the same figure. It is observed that the threshold voltage is higher for the \( N_F = 0 \) case. Further, the variation of threshold voltage with gate length for different values of effective Ge mole fraction in the relaxed SiGe buffer is also shown in the same figure. It is observed that SCEs become apparent when the channel length is below 40–50 nm and is marked by sharp decrease in the \( V_{th} \) value. The gate-source/drain (S/D) charge sharing and source-body/drain-body built in potential barrier lowering due to overlap of the lateral source-body and drain-body depletion regions becomes significant for such short channel lengths. The \( V_{th} \) values from the analytical model are in close proximity with the simulation results.

5. Conclusion

The modified model including interface trapped charges for surface potential, electric field and threshold voltage analyses the effectiveness of DMG-FD-S-SOI MOSFET to suppress the SCEs. Due to the dual material gate introduction, there is a step function in the channel region and that will be the important factor for suppression of HCE and DIBL. An extensive analysis is carried out to study the effect of various parameters such as Ge mole fraction, drain bias, gate length ratio variation, and interface charge variation on surface potential, electric field, and threshold voltage. From the result,
the deterioration in the threshold voltage with increasing strain may be improved by increasing the length of control gate (M1). Also, by increasing the gate length ratio \( \frac{L_1}{L_2} \), DIBL and HCE can be controlled effectively. The device performance is going to deteriorate in the presence of the interface trapped charges in the oxide. The derived analytical model is compared and found to be in excellent agreement with the simulation results obtained from Sentaurus™.

**Appendix A**

The common Poisson’s equation for the potential distribution in the two strained silicon regions can be written as [12]

\[
\frac{\partial^2 \phi_1(x, y)}{\partial x^2} + \frac{\partial^2 \phi_1(x, y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{Si}}
\]

(A1)

\[
\frac{\partial^2 \phi_2(x, y)}{\partial x^2} + \frac{\partial^2 \phi_2(x, y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{Si}}
\]

(A2)

where \( \varepsilon_{Si} \) is the permittivity of strained Si film, \( N_A \) is the doping concentration of strained Si film, and \( t_{Si} \) is the thickness of strained Si film. The potential distributions in both two regions can be approximated by parabolic polynomial as [2]

\[
\phi_1(x, y) = \phi_{M1} + a_{11}(x)y + a_{12}(x)y^2
\]

for \( 0 \leq x \leq L_1, 0 \leq y \leq t_{Si} \).

\[
\phi_2(x, y) = \phi_{M2} + a_{21}(x)y + a_{22}(x)y^2
\]

for \( L_1 \leq x \leq L, 0 \leq y \leq t_{Si} \).

(3.3) and (3.4) where \( a_{11}(x) \) and \( a_{22}(x) \) are the surface potential under gate electrodes M1 and M2, respectively. The coefficients of \( a_{11}(x) \), \( a_{12}(x) \), and \( a_{22}(x) \) are the functions of \( x \) only.

The Poisson’s equation can be solved by using the following boundary conditions.

(1) Electric flux (displacement) at the gate oxide/strained Si film interface is continuous in both regions:

\[
\left. \frac{d\phi_1(x, y)}{dy} \right|_{y=0} = \frac{\varepsilon_{ox} \psi_{S1} - V_{GS1}}{t_f},
\]

(A5)

\[
\left. \frac{d\phi_2(x, y)}{dy} \right|_{y=0} = \frac{\varepsilon_{ox} \psi_{S2} - V_{GS2}}{t_f},
\]

(A6)

where \( V_{GS1} = V_{GS} - (V_{FB1} - V_{FB2}) \), which is the gate oxide thickness. The effects of trapped charges are to be considered as:
The effect of strain on band structure is considered as given in [9], where \((V_{FB1,f})_{s-Si}\) and \((V_{FB2,f})_{s-Si}\) are the flat band voltages of strained-Si MOSFET in the front channel for both the regions. \((V_{FB1,b})_{s-Si}\) and \((V_{FB2,b})_{s-Si}\) are the flat band voltages of bulk Si MOSFET in the front channel for both the regions. \(\Delta V_{FB,f}\) represents the amount of change in flat band voltage due to strain. \(N_f\) is the interface oxide charges in both dimension and polarity and \(C_{ox}\) is the gate capacitance.

(2) Electric field at the interface of the buried oxide and the back channel is continuous

\[
\frac{d\varphi_{f}(x, y)}{dy} \bigg|_{y=y_{os}} = \frac{\varepsilon_{ox}-\varepsilon_{Si}}{t_{o}} \varphi_{SUB} = \frac{d\varphi_{f}(x, y)}{dy} \bigg|_{y=y_{os}}, \quad (A7)
\]

where \(\varepsilon_{SUB} = \varepsilon_{ox} - \varepsilon_{Si}\). \(V_{SUB}\) is the substrate bias, \((V_{FB,b})_{s-Si}\) is the flat band voltage of strained silicon in the back channel and \(\varphi_{f}(x)\) is the back potential.

(3) Electric flux (displacement) and the electric potential at the M1/M2 interface is continuous

\[
\frac{d\varphi_{f}(x, y)}{dy} \bigg|_{y=y_{os}} = \frac{d\varphi_{f}(x, y)}{dy} \bigg|_{y=y_{os}}, \quad (A8)
\]

\[
\varphi_{f}(L_{1}, 0) = \varphi_{f}(L_{1}, 0). \quad (A9)
\]

(4) The surface potential at the source end is

\[
\varphi_{f}(0,0) = \varphi_{f1}(0) = V_{hi,s-si}, \quad (A10)
\]

where \(V_{hi,s-si}\) is the built-in potential of strained Si thin film [12].

(5) The surface potential at the drain end is

\[
\varphi_{f2}(L_{1} + L_{2}, 0) = \varphi_{f2}(L_{1} + L_{2}) = V_{hi,s-si} + V_{DS}. \quad (A11)
\]

Using the boundary conditions equations (A5)–(A11) we obtain coefficients and obtain the expressions for \(\varphi_{f1}(x, y)\) and \(\varphi_{f}(x, y)\). Substituting \(\varphi_{f1}(x, y)\) and \(\varphi_{f}(x, y)\) into (A1) and (A2), respectively, and substituting \(y=0\), we obtain

\[
\frac{d^{2}\varphi_{f1}(x)}{dx^{2}} - \alpha \varphi_{f1}(x) = \beta_{1}, \quad (A12)
\]

\[
\frac{d^{2}\varphi_{f2}(x)}{dx^{2}} - \alpha \varphi_{f2}(x) = \beta_{2}, \quad (A13)
\]

where

\[
\beta_{1} = \frac{qN_{A}}{e_{ox}} - 2\frac{V_{GS1}(C_{ox}+C_{G}+C_{C})}{\epsilon_{ox} C_{ox}(2\epsilon_{ox}+\epsilon_{Si})},
\]

\[
\beta_{2} = \frac{qN_{A}}{e_{ox}} - 2\frac{V_{GS2}(C_{ox}+C_{G}+C_{C})}{\epsilon_{ox} C_{ox}(2\epsilon_{ox}+\epsilon_{Si})}.
\]

The solution for (A12) and (A13) as second order non-homogenous differential equations with constant coefficients can be expressed as

\[
\varphi_{f1}(x) = A \exp(n x) + B \exp(-n x - \frac{\beta_{1}}{\alpha}), \quad (A14)
\]

\[
\varphi_{f2}(x) = C \exp\left(\frac{n (x - L_{1})}{2}\right) + D \exp\left(-n (x - L_{1}) - \frac{\beta_{2}}{\alpha}\right). \quad (A15)
\]

where \(n = \sqrt{\alpha}, p_{1} = \frac{\beta_{1}}{\alpha}\), and \(p_{2} = \frac{\beta_{2}}{\alpha}\).

Using the boundary condition (A5)–(A11) we solve for \(A, B, C,\) and \(D\)

\[
\begin{align*}
A &= (V_{hi,s-si}(1 - \exp(-nL)) + V_{DS} + (p_{1} - p_{2}) \\
&\times \cos h(nL_{2}) + p_{2} - p_{1} \exp(-nL) / (2 \sin h(nL)), \quad (A16)
\end{align*}
\]

\[
\begin{align*}
B &= (V_{hi,s-si}(\exp(nL) - 1) - V_{DS} - (p_{1} - p_{2}) \\
&\times \cos h(nL_{2}) - p_{2} + p_{1} \exp(nL) / (2 \sin h(nL)), \quad (A17)
\end{align*}
\]

\[
\begin{align*}
C &= A \exp(nL_{1}) + \frac{p_{2} - p_{1}}{2}, \quad (A18)
\end{align*}
\]

\[
\begin{align*}
D &= B \exp(-nL_{1}) + \frac{p_{2} - p_{1}}{2}. \quad (A19)
\end{align*}
\]

**Appendix B**

The minimum potential of channel can be calculated from (A14), (A15) as

\[
x_{min} = \frac{1}{2n} \ln \frac{B}{A}, \quad (B1)
\]

\[
\phi_{x,min} = 2\sqrt{AB} - p_{1}. \quad (B2)
\]

The threshold voltage \(V_{th}\) of the un-strained device can be found as follows [15]

\[
\phi_{x,min} = \phi_{th} = 2\phi_{f,si}, \quad (B3)
\]

\[
\phi_{f,si} = KT \ln \frac{N_{A}}{n_{i}}, \quad (B4)
\]

where \(K\) is the Boltzmann’s constant, \(T\) is the temperature, \(\phi_{f,si}\) is the difference between the Fermi potential and the intrinsic Fermi is level in the bulk region. \(\phi_{th}\) is the value of
surface potential at which the volumetric inversion electron charge density in the Si device is equal to the body doping.

For strained-Si SOI MOSFET the threshold condition under the front gate is modified as [2]

$$\phi_{s, \text{min}} = \phi_{th} = 2\phi_{f,\text{Si}} + \Delta \phi_{s,\text{Si}}^- \cdot x$$  \hspace{1cm} (B5)

where $\Delta \phi_{s,\text{Si}} = -\frac{\Delta E_{\text{g,Si}}}{q} + V_F \ln \frac{N_{\text{Si}}}{N_{\text{V,\text{Si}}}}$.

In the case of the DMG-FD-S-SOI structure, because of coexistence of different metal M1 and M2, the minimum surface potential is purely dependent on metal gate with the higher work function. So the threshold voltage is calculated as the value of $V_{GS}$ at which the minimum surface potential $\phi_{s, \text{min}}$ equals to $\phi_{th}$. Hence, one can determine the value of threshold voltage as the value of $V_{GS}$ by using formula (8)

$$V_{th} = -\eta + \sqrt{\eta^2 - 4\sigma^2},$$  \hspace{1cm} (B6)

where $\gamma = \exp(-nL)$, $\sigma = \frac{1}{\gamma} + \gamma - 2 - \sin h^2(nL)$,

$$V_{h1} = V_{h,\text{Si}}(1 - \gamma) + V_{DS} - (u - v) \cos h(nL_2) - \nu + \nu \gamma,$$

$$V_{h2} = V_{h,\text{Si}} \left( \frac{1}{\gamma} - \frac{1}{\gamma} \right) - V_{DS} + (u - v) \cos h(nL_2) + \nu - \nu \gamma,$$

$$\nu = \frac{C_d}{C_f} V_{SUB} - \frac{qN_{A,\text{Si}}}{C_f} - V_{\text{FB1,\text{Si}}},$$

$$\xi = V_{h1} V_{h2} - \sin h^2(nL) (\phi_{th} - u)^2,$$

$$\eta = V_{h1} \left( \frac{1}{\gamma} + 1 \right) + 2 \sin h^2(nL) (\phi_{th} - u) - V_{h2} (1 - \gamma).$$

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