Performance of the Data Handling Hub readout system for the Belle II pixel detector

Stefan Huber, Igor Konorov, Dmytro Levit, Stephan Paul, and Dominik Steffen

Abstract—The SuperKEKB accelerator in Tsukuba, Japan is providing $e^+e^-$ beams for the Belle II experiment since March 2019. To deal with the aimed peak luminosity being forty times higher than the one recorded at Belle, a pixel detector based on DEPFET technology has been installed. It features a long integration time of 20 µs resulting in an expected data rate of 20 GByte/s (160 GBit/s) at a maximum occupancy of 3%. To deal with this high amount of data, the data handling hub (DHH) has been developed. It contains all necessary functionality for the control and readout of the detector. In this paper we describe the architecture and features of the DHH system. Further we will show the key performance characteristics after one year of operation.

Index Terms—Data acquisition, Data handling, High energy physics instrumentation computing, Position sensitive particle detectors, Silicon radiation detectors

I. INTRODUCTION

SINCE the beginning of 2019 the Belle II experiment is taking data. The experiment is studying events from electron-positron collisions with beam energies of 7 GeV for electrons and 4 GeV for positrons. The design luminosity is 40 times higher than the one at the Belle experiment and shall reach up to $8 \times 10^{35}$/(cm$^2$s). The experiment is built in a shell structure around the interaction point and consists of three types of tracking detectors, namely, the pixel detector (PXD), the silicon vertex detector (SVD), and the central drift chamber (CDC). These are surrounded by detectors for particle identification and calorimetry.

In this paper we describe the implementation and performance of the readout system of the PXD, the data handling hub (DHH). It is the most demanding part in the readout chain of the Belle II experiment as it has to deal with 95% of the data.

II. THE BELLE II PIXEL DETECTOR

The Belle II pixel detector [1] is the innermost structure in the Belle II experiment. It consists of two layers of in total 40 modules, called half ladders. Two half ladders are glued together and form one ladder. Those are arranged in a cylindrical structure around the interaction point. Currently, 20 modules are installed in the running experiment, this corresponds to the full inner layer of eight ladders and two ladders of the outer layer.

The half ladders are built using DEPFET technology and provide a pixel matrix of 768×250 pixels, each. The module is controlled by the SwitcherB [2] ASIC. This chip is responsible for the running shutter operation mode, which controls the readout and clearing of the pixel information. The operation of the sensor is performed in groups of four rows, the so-called gates, which are digitized in the same readout cycle.

The readout of the pixel matrix is performed using four pairs of ASICs. Each pair reads one quarter of the columns and consists of the drain current digitizer (DCD) [2] and the data handling processor DHPT [3]. The DCD digitizes 256 detector signals at once using ADCs with 8 Bit resolution at a sampling rate of 9.5 MHz and sends the data to the DHPT. On the DHPT the data are processed with algorithms such as pedestal subtraction, zero suppression, and common mode correction. The data are then further arranged in 8b10b encoded Aurora [4] frames and sent out to the DHH system, discussed in the rest of the paper. It has to be noted that the limit for lossless data processing on the DHPT is given by a maximum occupancy of 3%.

After processing in the DHH, the data are then sent to the online selection nodes (ONSEN) [5] where they are buffered until the high-level trigger (HLT) decides to store or discard that event. Further, the HLT extrapolates the tracks measured by the rest of the Belle II experiment to the surface of the PXD.
Fig. 2. Top view of the DHH with attached RTM. The processing cards are slightly pulled out in order to show the structure.

Only hits close to the extrapolated tracks are sent further to the storage.

III. HARDWARE

The DHH system, shown in Fig. 1 and Fig. 2, is built based on the ATCA standard and utilizes eight ATCA carrier-cards for the readout of the full PXD. We equip each of these carriers with seven AMC cards: one DHC, five DHEs, and one DHI. We designed two of them, the data handling engines (DHE) and the data handling concentrator (DHC), as single-width AMC modules. The data handling insulator (DHI) has been designed in the double-width form-factor by us. The interconnection in the system is set-up in a star topology where the DHC serves as the master and is connected to each of the other modules with a single high-speed serial link. The data flow is depicted in Fig. 3.

External interfaces are implemented using rear transition modules (RTMs), they are equipped with six SFP+ transceivers. Four of them are used for sending out the data to the DAQ, one for transferring monitoring data to a local DAQ, and one for slow-control. The detector data are received by two MiniPOD receivers which are capable of handling 20 data interfaces to the detectors. Control signals are distributed to the detectors using five 20 meters long CameraLink cables attached to the front panel of the DHI. The DHE and DHC modules are based on the same hardware design Fig. 4, their functionality is implemented using a Virtex-6 VTX30T FPGA. Via the AMC connector, a maximum data rate of 5 GBit/s can be achieved between the modules while a maximum data rate of 6.5 GBit/s is achieved via the RTM. Both cards are equipped with 4 GByte of DDR3 memory mounted on a SO-DIMM slot. A configurable clock generator, Si5338, is used to reduce the jitter of the recovered clock from the Belle II time-distribution system as well as for the clocks recovered from the high-speed links to 14 ps.

A. The data handling engine

The purpose of the DHE is to process the data from one half-ladder of the PXD. The data are received via four optical links running with a 1.5 GBit/s Aurora (8b10b) link, each. These data are pre-buffered using 4 GByte of DDR3-memory organized as four FIFOs, one for each incoming data stream.

The challenge on this module comes from the long integration time of 20 µs of the detector together with trigger rates up to 30 kHz. The DHPT ASIC has a simple logic to handle these requirements. The detector information is processed by DHPT continuously with the speed of the running shutter. The trigger signal opens a 20 µs gate enabling the DHPT to send data out. If the following trigger is closer than 20 µs then the gate signal is extended for the next 20 µs. A task of the DHE is to synchronize DHPT data with a trigger by using frame and row numbers information transmitted by the DHPT. When the time between triggers is smaller than 20 µs, a part of detector data shall be shared between two or more consecutive events, Fig. 5. This is resolved by analyzing the time of arrival of the individual triggers. The DHPT emulator, implemented in the DHE, predicts which part of the readout frames corresponds to which triggeri, as shown in Fig. 6.
Using this information the data are analyzed by corresponding state machines and start/end address pointers of each event are detected. Then they are written to the dual-port random-access memory. Subsequently the pointers are transmitted to the read controller for event data extraction from this memory. There are four of such data processing streams in the DHE, one for each DHPT ASIC. At the last step of the data processing the data from four streams are merged in one sub-event and sent to the DHC.

The data processing in the DHE is capable to store up to 2000 events in the pipeline. The DHC issues a busy signal to the Belle II trigger system to prevent buffer overflow and loss of data.

In contrast to the DHE, the DHPT ASICs do not have a capability to throttle triggers in case the data rate exceeds the bandwidth of outgoing interfaces. This may happen in the first few revolution cycles after bunch injection, due to high background. In that situation the data may be scrambled and can affect the DHE data processing algorithm. The DHE performs a sanity data check at the input to minimize an impact of such data on stability of data taking. Although not all data with errors are excluded from the readout, full error diagnostic is provided via slow control.

### B. The data handling concentrator

The data processing on DHC has two different duties. As a first task, it has to provide a 5-to-1 multiplexer to merge data from 5 DHE modules and, as a second task, it has to distribute the events in a round-robin manner between four ONSEN nodes. As these two functionalities are closely coupled, they are implemented in a common framework taking advantage of buffering in the DDR3 memory. The data flow is depicted in Fig. 7.

In the first stage, the input data are pre-buffered in a local 4 kword deep FIFO which issues back pressure to the DHE in case it fills up above 95%. The data are written into the memory in a sorted way. This means the data from the first DHE for one event are written, then the data for the second one till finally the data from the last DHE are stored in the memory. The pointers from the different DHEs are passed from one writer state machine to another so after one cycle a fully assembled event is stored in the memory. Each event is stored in a predefined memory slot which can hold up to 1 MByte of data. Due to this mechanism, the DHEs with a higher index have to wait until the DHEs with a lower index have finished processing the current event. This creates the necessity to buffer the events on the DHEs to avoid any loss of data.

All five inputs are loosely synchronized between each other by transmitting pointers via trigger fifos. It allows to compensate possible interference between streams due to variation of data rates and achieve fully parallel data processing very close to the maximum speed.

The memory-pointers of the events are then passed to an output-selection state machine which decides to which ONSEN node the event shall be written. This is done based on a lookup table checking the four least-significant bits of the event number and which ONSEN nodes are currently used in the system.

Finally, one out of four data-reader state machines receives the pointers and reads a full event from the memory. Together with the trigger information a full event is assembled and sent out via a 6.5 GBit/s Aurora link to the ONSEN system.

Part of the data is needed for real-time monitoring of the system performance. To achieve that, the first output of the event builder is connected to two interfaces. One of them takes only a small fraction of the data and sends them via a UDP link to the local DAQ. In the case of detector studies, it is possible to send data only via this UDP link. In this mode of operation the maximum trigger rate is limited by the UDP bandwidth.

The DHC is designed in a way that it can handle up to 1000 triggers in a pipeline. In case a threshold of 900 triggers is
The synchronization bit synchronizes the running shutter to the revolution cycles of the accelerator. As one PXD frame corresponds to two revolution cycles, the B2TT provides a designated signal synchronously to every other revolution cycle.

The DHI allows us to configure half-ladders over JTAG protocol using 5 JTAG player cores in FPGA. The JTAG players are controlled by an input-output control software (IOC) running on the remote PC. The JTAG player core communicates with the IOC over a dedicated IPbus instance in the DHI, decodes the bitstream, shifts it into the JTAG chain, records the read back data from the detector, and sends them to the control software. The IOC communicates with the detector slow-control via the Experimental Physics and Industrial Control System (EPICS) [9]. EPICS is a framework which provides a register-based network protocol used to design distributed slow control systems. The IOC translates the high-level EPICS transaction into low-level commands for the JTAG player. The IOC memorizes the content of the JTAG registers and bit fields, which are available for read and write access over EPICS. The IOC uses these values to assemble the bitstream when the JTAG access is scheduled, and sends the bitstream to FPGA for execution. After the transaction is finished, the IOC decodes the detector reply, stores the new values, and makes them available over EPICS.

In addition to the control features, the DHI provides a precise current source, it can be used for calibration of the detector. Further, the DHI supplies the optical transmitter close to the detector with the voltage 3.3 V. It is possible to switch off all channels via the FPGA in order to avoid powering of the DHPT ASIC by DHI via the LVDS JTAG wires which provide a constant common mode voltage.

D. The Crosspoint Switch

The PXD read out system is equipped with a $144 \times 144$ crosspoint switch, originally developed for the DAQ of the COMPASS experiment [10]. The switch provides full flexibility to define optical links’ topology between the detectors and the DHH. The ONSen system needs a defined order of the detector information in the data stream which matches the order in which the regions of interest are received from the HLT. This does not coincide with the topology in which the detector is cabled. Installation of the switch gives several other advantages over a direct connection such as changeover in case of failure or mirroring the links on another DHE for monitoring or testing new features. The switch allows to monitor the optical power of each link with high precision providing good diagnostics of the optical transmitters installed close to the detector and exposed to ionizing radiation.

E. The UCF Protocol

For the data links between DHC and DHI/DHE we utilize the unified communication framework UCF [11]. This is a protocol developed for particle physics [12] experiments. It provides a clock with a jitter, measured to be 23 ps in our system at the receiving side together with a deterministic phase relation. It is possible to transmit up to 64 different data
streams via a single serial link. One stream has a deterministic latency and shall be used to transmit real-time signals of the time distribution system. In our application, we use two additional channels, one in a bidirectional way to transmit UDP frames used for the slow-control by IPbus [13] and one for transmission of the data, Fig. 9. In order to catch transmission errors the data protocol has a CRC32 checksum attached to every frame. Errors in operation are prevented by attaching a CRC16 checksum to every command word of the real-time channel, in case of a checksum mismatch the command is ignored. In that case, missing events are recovered on the DHC.

![Fig. 9. Data stream connected to the UCF link. B2TT represents the real-time signals transmitted to the DHE/DHI and includes information like triggers, synchronization, and resets.](image)

**F. Synchronization Of The System**

All detectors in the Belle II experiment are synchronized with the SuperKEKB accelerator by Belle II Trigger and Time distribution system (B2TT) [8]. The B2TT system broadcasts a 127.21 MHz clock that is generated from the accelerator’s radio frequency clock of 508.84 MHz. The trigger and synchronization information is broadcasted together with the B2TT clock using an 8b/10b encoding over serial lines.

The DHC as well as the interfaces to DHE and DHI are using the recovered 127.21 MHz clock as the main time reference. The detector is operating at a lower frequency of 76.33 MHz derived from the main clock by fractional divider 3/5. This clock is synthesized locally on the corresponding modules and special care is taken to transfer all real-time signals synchronously between the two clock domains. It is important to note that the control signals to the detector are sent-out only every 8th clock cycle of 76.33 MHz and thus the signals have to be synchronized between the two clock domains in this time frame. Taking this into consideration the transferred signals are sent out from the DHC in three fixed time intervals of 13, 13 and 14 clock cycles in the 127.21 MHz domain. This sequence repeats every 40 clock cycles and requires a minimum distance between two triggers of about 120 ns.

IV. PERFORMANCE

A. Gated Mode

The lifetime of the beam in SuperKEKB is approximately 600 s [14]. In order to operate the experiment at high luminosity, a continuous injection scheme is applied. For each ring bunches of electrons or positrons are injected with a frequency of 25 Hz. These freshly injected bunches lead to an increased background level for a few ms after their injection.

![Fig. 10. Distribution of hits during a lab measurement with activated gated mode with ten recorded events. There are two regions in which the gated mode was switched on which show an increased occupancy, indicated by the yellow color. Inside these regions bands with now hits due to the de-activated trigger signal are visible. The dotted vertical lines are pixels where zero-suppression is switched off, they are used as an optical guide. Most of the additional hits in the matrix are due to the induced pedestal oscillation as well as from hot pixels which are not taken care of in the lab setup.](image)

To make the PXD insensitive to this injection noise, the detector will be operated in gated mode [15]. While in gated mode, the detector stores the already accumulated charge in each pixel but does not store charge from radiation impinging on the detector.

As soon as a new bunch is injected into the accelerator the gated mode logic on the DHC is armed by the kick signal of the injection magnet, distributed by the B2TT. The DHC is responsible for the timing of the gated mode operation, and sends a start as well as a stop signal to the DHI. The start signal is issued shortly after the kick signal and the stop signal is issued as soon as the injection background is assumed to be low enough. Typically this is the case after a few ms. Both parameters may be tuned individually for both detector rings.

The DHI uses these signals to control the gated mode on the detector by modifying two of the control signals: trigger and veto. The veto bit is activated every revolution cycle (twice per detector frame) at the time the noisy bunch needs to pass by the
detector. An optimal value for this time is the readout duration of 10 gates corresponding to 1.04 µs. Gated mode operation significantly changes the electrical fields applied to the sensor and thus shifts the pedestal of the pixel which are activated by the rolling shutter close to the time when the gated mode is enabled. To avoid data loss due to high detector occupancy caused by the corresponding increased noise, the trigger signal is not issued during that period. The typical time constant for this pause is the duration of the readout of 20 gates or 2.08 µs. The effect is seen in Fig. [10].

During 2020 operation the gated mode has been tested [16] and the principle was proven. Still, a final tuning of the parameters as well as a detailed understanding of the pedestal oscillation has to be performed before it can be activated during data taking.

**B. Performance During Belle II Operation**

We installed and operated four DHH carriers at the Belle II experiment and operated them successfully during the runs in 2019 and 2020. As we are still in a phase where the performance of the accelerator is optimized, the trigger rates of 5 kHz are still significantly below the design rate of 30 kHz which is anticipated for the future. Further, the average detector occupancy was below 0.5% due to the not yet final luminosity of the accelerator.

In these conditions the average data rate for a single DHE was 5 MByte/s and 94 MByte/s for the installed system consisting of 20 DHEs. Peak data rates were 20 MByte/s for the DHE with the highest occupancy and 160 MByte/s for the current system.

During test runs with artificial triggers and generated data on the DHP we reached a maximum throughput of 250 MByte/s per DHE and in total 5 GByte/s. This maximum throughput limits the system performance to 17 kHz at a detector occupancy of 3%. This corresponds to a throughput of 10 GByte/s for the final system.

The throughput of the DHH is significantly above the requirements of the current operation but still a factor two below the designed performance. In order to meet the future requirements a redesign of the ATCA carrier is ongoing.

**V. CONCLUSION AND OUTLOOK**

During the last two years, we have proven that we can reliably read out the Belle II pixel detector with the DHH system. The next major milestones are the installation of the full PXD in 2022 which requires the installation of four additional DHH modules at Belle II. The trigger rates will rise in the future and thus the link speeds on UCF have to be increased to 5 GBit/s to cope with the increased data rate. We are currently redesigning the carrier card to perform this mandatory step.

An important next step, not directly related to the DHH, is the commissioning of the gated mode. Here, work is ongoing in terms of analysis and detector optimization.

Two additional upgrades for the DHH are planned. Currently we use UDP for reading out data to the local DAQ. As UDP does not have any error handling, part of the data is lost on that interface. We are currently investigating a changeover to a readout based on a commercial PCIe card which will allow us to reliably record these data.

Finally, we plan to implement a clustering algorithm in the DHE. Based on the parameters of these clusters it is possible to keep hits in the data-stream which otherwise would be disregarded by the HLT decision [17]. This is especially important for hits from slow pions which will not reach the outer tracking detector of the Belle II experiment.

**REFERENCES**

[1] C. Marinas, “The Belle II pixel detector: High precision with low material,” Nucl. Instrum. Meth. A, vol. 731, pp. 31–35, 2013.
[2] I. Perić, P. Fischer, T. H. H. Nguyen, and L. Knopf, “DCDB and SWITCHERB, the readout ASICS for BELLE II DEPFET pixel detector,” in 2011 IEEE Nuclear Science Symposium and Medical Imaging Conference, 2011, pp. 1536–1539.

[3] M. Lemarenko, T. Hemperek, H. Krüger, M. Koch, F. Lütticke, C. Mariñas, and N. Wermes, "Test results of the data handling processor for the DEPFET pixel vertex detector," JINST, vol. 8, p. C01032, 2013.

[4] Aurora 8b/10b. Xilinx, Inc. [Online]. Available: https://www.xilinx.com/products/intellectual-property/aurora8b10b.html

[5] T. Geßler, W. Kühn, J. S. Lange, Z. Liu, D. Münchow, B. Spruck, and J. Zhao, “The ONSEN Data Reduction System for the Belle II Pixel Detector,” IEEE Trans. Nucl. Sci., vol. 62, no. 3, pp. 1149–1154, 2015.

[6] AdvancedTCA® Overview, PICMG (PCI Industrial Computer Manufacturers Group) Std. [Online]. Available: https://www.picmg.org/openstandards/advancedtca/

[7] Camera Link – The Only Real-Time Machine Vision Protocol, AIA (Automated Imaging Association) Std. [Online]. Available: https://www.visiononline.org/vision-standards-details.cfm?type=6

[8] M. Nakao, “Timing distribution for the Belle II data acquisition system,” JINST, vol. 7, p. C01028, 2012.

[9] L. R. Dalesio, J. O. Hill, M. Kraimer, S. Lewis, D. Murray, S. Hunt, W. Watson, M. Clausen, and J. Dalesio, “The experimental physics and industrial control system architecture: past, present, and future,” Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, vol. 352, no. 1, pp. 179 – 184, 1994.

[10] S. Huber et al., “Intelligence Elements and Performance of the FPGA-based DAQ of the COMPASS Experiment,” PoS, vol. TWEPP-17, p. 127, 2018.

[11] D. Gaissbauer, Y. Bai, S. Huber, I. Konorov, D. Levit, S. Paul, and D. Steffen, “Unified communication framework,” in 20th IEEE-NPSS Real Time Conference, 2016.

[12] D. Gaissbauer, Y. Bai, I. Konorov, S. Paul, and D. Steffen, “Self-triggering readout system for the neutron lifetime experiment PENeLOPE,” JINST, vol. 11, no. 02, p. C02068, 2016.

[13] R. Fraizer, G. Iles, D. Newbold, and A. Rose, “Software and firmware for controlling CMS trigger and readout hardware via gigabit Ethernet,” Phys. Procedia, vol. 37, pp. 1892–1899, 2012.

[14] M. Bona et al., “SuperB: A High-Luminosity Asymmetric e+ e− Super Flavor Factory. Conceptual Design Report,” 2007.

[15] M. Valentan, E. Prinker, F. Müller, C. Koffmane, and R. Richter, “Gated mode operation of DEPFET sensors for the Belle II pixel detector,” in 2015 IEEE Nuclear Science Symposium and Medical Imaging Conference, 2016, p. 7581886.

[16] B. Spruck et al., “Belle II Pixel Detector Commissioning and Operational Experience,” PoS, vol. Vertex2019, p. 015, 2020.

[17] S. Baehr, O. Sander, M. Heck, C. Pulvermacher, M. Feindt, and J. Becker, “Online-Analysis of Hits in the Belle-II Pixeldetector for Separation of Slow Pions from Background,” J. Phys. Conf. Ser., vol. 664, no. 9, p. 092001, 2015.