Model predictive control of a hybrid stacked multicell converter with voltage balancing and fault tolerance capability

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Abstract
Due to the merits of low conduction losses and superior output power quality, a hybrid stacked multicell converter (HSMC) was put forward as a competitive alternative in the medium/low-voltage high-efficiency applications. A nine-level HSMC (9L-HSMC) can be seen as a combination of a five-level SMC (5L-SMC) and two-level half-bridge, and proper modulation and control strategy are essential for the HSMC to obtain the optimal output performance. This work develops a finite control-set model predictive control (MPC) strategy for 9L-HSMC to balance the capacitor voltages and maintain the desired outputs, rendering the absence of the linear regulator and pulse width modulation (PWM) modulator possible. The fault-tolerant operation can also be achieved flexibly when open-circuit faults occur at active bidirectional switches in the 5L-SMC bridge, and the performance is verified by simulations. Finally, experiments under several typical operating conditions are implemented to verify the effectiveness of 9L-HSMC with the developed MPC strategy.

1 | INTRODUCTION

In recent years, multilevel converters draw more and more attentions in the high-voltage large-power industry areas because of their paramount features, such as reduced device stress, superior power quality and lower power losses [1, 2]. Three typical multilevel topologies such as neutral-point-clamped (NPC), flying-clamped capacitor (FCC) and cascaded H-bridge (CHB) converters have been widely employed in various energy conversion systems. The NPC and FCC topologies suffer the inherent drawbacks of numerous devices requirement and voltage unbalance of capacitors, which limit their higher-level (over five) applications [2].

Hybrid multilevel converters (HMCs) have been put forward by combining the merits of traditional converters, which are suitable for medium- and low-voltage applications due to their high efficiency [3–5]. Several HMC topologies, such as active NPC ANPC), nested NPC and stacked multicell converter (SMC), have been proposed for various applications [6–8]. The SMC is proposed by stacking flying capacitor (FC) cells, and it draws great attentions from the academic and industrial communities because of its dramatic characteristics, such as simple structure, natural balance capability and high efficiency. An SMC is composed of FC-based cells, and a three-level T-type converter can be recognised as the SMC with two FC-based cells which own the advantage of low conduction losses [9, 10]. In low-voltage applications and switching frequency below 35 kHz, the three-level T-type converter is better than NPC [10].

Several FC-based HMCs have been put forward for medium- and low-voltage applications with reduced devices, compared with traditional SMC [11–13]. The required number of dc sources is halved by connecting two additional switches in parallel with the original SMC [11]. To reduce the number of high-frequency switches, a mixed structure of SMC was presented by increasing four switches that work at fundamental frequency [12]. Moreover, a hybrid SMC (HSMC) was put forward to reduce the high-frequency switches in [13], which is devised by introducing merely two low-frequency switches. As a result, the number of high-frequency switches in such HSMC is cut by half while the amplitude of output voltage is doubled. The nine-level HSMC (9L-HSMC) can be divided into a five-level SMC (5L-SMC) bridge and a two-level half-bridge (2L-HB; see Figure 1), where the switches of 5L-SMC and 2L-HB bridges work at
high frequency and fundamental frequency, respectively. Therefore, low power losses and good output quality are obtained for 9L-HSMC. Some other HMC topologies with reduced power devices have been proposed for high-voltage applications, such as grid-connected system [14], high-frequency link converters [15] and high-voltage direct current transmission [16]. This work is devoted to explore the overwhelming merits of the HSMCs, in terms of capabilities of voltage balancing and fault tolerance.

Capacitor voltage balancing is a critical issue for 9L-HSMC, and each FC voltage must be controlled at their references. Typically, the FC voltage can be balanced by utilising multycarrier-based pulse width modulation (PWM) along with redundant state selections [17–19]. However, these PWM-based approaches are incapable of realising multiple control targets simultaneously, such as switching frequency optimisation and fault-tolerant operation. Model predictive control (MPC) has the merits of intuition, simplicity and flexibility, offering adaptability, robustness and fast dynamic response [20]. The linear regulators and modulators are absent, thereby reducing control complexity significantly. Additionally, the multiple-objective optimisation can be realised by selecting proper weighting factors in a single cost function. In recent years, the MPC technique has been adopted and designed to meet specific requirements in various power converters [21–23] and motor drives [24, 25]. To obtain a good quality of outputs, some improved MPC approaches were put forward for various HMC topologies. A selective harmonic elimination MPC method was presented in [26] for the multilevel converters. In [27], a simplified two-stage MPC was put forward for an HMC that is a combination of ANPC with a floating H-bridge. In [28], a virtual space vector MPC was proposed for a three-phase seven-level HMC. A new Lyapunov-based MPC was developed for a seven-level packed U-cell grid-connected inverter [29].

To the best of the author’s knowledge, no study on the MPC of HSMC has been reported in prior literature. For this motivation, this work develops an MPC-based control strategy for 9L-HSMC to obtain the desired outputs as well as balancing the capacitor voltages. First, the proposed MPC method is implemented by constructing a discrete-time model of 9L-HSMC, where a cost function is defined to achieve the control objectives by evaluating all the available switching states. Afterwards, the optimum switching state that minimises the cost function will be applied for 9L-HSMC at the next sampling interval. Furthermore, with the help of bidirectional switches, the fault-tolerant operation can be achieved by using the proposed MPC-based control strategy, thereby enhancing system reliability. The post-fault configurations, operation principle and control strategies are put forward. The blocking voltages and power losses, including switching loss and conduction loss, are studied for the 9L-HSMC. Finally, the feasibility of the proposed control strategy for 9L-HSMC is validated by experiments under several typical operating conditions.

2 | HYBRID STACKED MULTICELL CONVERTERS

2.1 | Operation modes

The main circuit of 9L-HSMC is drawn in Figure 1, where \( v_d \) denotes the output phase voltage between terminals \( X_1 \) and \( X_2 \), and \( i_a \) is positive phase current (\( i_a > 0 \)). In this circuit, \( T_{11}, T_{12}, T_{21}, T_{22} \) and their complementary switches of 5L-bridge work at high-frequency PWM mode, and \( T_1, T_0 \) of 2L-bridge work at low-frequency mode. If the dc-bus voltage is equal to \( V_{dc} \), the reference values of the dc-link capacitor voltages and FC voltages must be controlled at \( V_{dc}/2 \) and \( V_{dc}/4 \), respectively.

The 9L-HSMC has 18 redundant states \( V_1 \sim V_{18} \) as listed in Table 1, where the characters \( S_i, S_j (i = 1, 2; j = 1, 2) \) are switching functions of power switches \( T_i \) and \( T_j \), respectively. The capacitor currents and their effect on the capacitor voltages are illustrated for the states \( V_1 \sim V_{18} \). Due to the state redundancy, the voltage balancing of FCs can be realised by selecting an optimum state to charge/discharge the FCs. During the positive half-cycle of current, states \( V_7 \) and \( V_8 \) can be selected to output \( V_{dc}/4 \), whereas the effect on the \( C_2 \) under states \( V_7 \) and \( V_8 \) will be opposite. Likewise, we can select \( V_{11} \) and \( V_{12} \) to output \( -V_{dc}/4 \), and this will result in discharging and charging the \( C_1 \), respectively. The output voltage \( v_d \) can be synthesised to acquire the nine levels (\( \pm V_{dc}, \pm 3V_{dc}/4, \pm V_{dc}/2, \pm V_{dc}/4, 0 \)) by selecting the proper switching state among the redundant states.

To emphasise the operating principle, Figure 2 indicates the current paths when 9L-HSMC operates at the positive half-cycle of current for outputting voltage levels \( \pm V_{dc} \) and \( \pm V_{dc}/4 \). One can find from Figures 2(a) and (b) that states \( V_1 \) and \( V_{18} \) have no impact on the FCs. As can be observed from Figures 2(c) and (d), states \( V_7 \) and \( V_8 \) are selected to output \( V_{dc}/4 \), which results in charging and discharging \( C_2 \), but no current flows through \( C_1 \). Likewise, states \( V_{11} \) and \( V_{12} \) discharge and charge \( C_1 \), but no current flows through \( C_2 \) as depicted in Figures 2(e) and (f).
TABLE 1 Switching states and output voltage for nine-level hybrid stacked multicell converter (9L-HSMC)

| States | LF cell switch $S_1$ | LF cell switch $S_{11}$ $S_{12}$ $S_{21}$ $S_{22}$ | HF cell switches $S_{1}$ $S_{2}$ $S_{3}$ $S_{4}$ $S_{5}$ $S_{6}$ $S_{7}$ $S_{8}$ | Output voltage $v_a$ | DC current $i_1$ $i_2$ $i_{k1}$ $i_{k2}$ | DC voltage $v_{1}$ $v_{2}$ | FC current $i_{f1}$ $i_{f2}$ | FC voltage $v_{f1}$ $v_{f2}$ |
|--------|---------------------|--------------------------------------------------|---------------------------------|------------------|-----------------|-----------------|------------------|------------------|
| $V_1$  | 0                   | 1 1 1 1 1                                       | $V_{dc}$                         | $i_a$ $i_a$      | $v_{a}$          | $i_a$ $i_a$      | $v_{a}$          | $i_a$ $i_a$      |
| $V_2$  | 0                   | 1 1 0 1                                         | $3V_{dc}/4$                      | $i_a$ $i_a$      | $v_{a}$          | $i_a$ $i_a$      | $v_{a}$          | $i_a$ $i_a$      |
| $V_3$  | 0                   | 0 1 1 1                                         | $3V_{dc}/4$                      | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        |
| $V_4$  | 0                   | 0 1 0 1                                         | $V_{dc}/2$                       | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        |
| $V_5$  | 0                   | 0 0 1 1                                         | $V_{dc}/2$                       | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        |
| $V_6$  | 0                   | 1 1 0 0                                         | $V_{dc}/2$                       | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        |
| $V_7$  | 0                   | 0 1 0 0                                         | $V_{dc}/4$                       | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        |
| $V_8$  | 0                   | 0 0 0 1                                         | $V_{dc}/4$                       | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        |
| $V_9$  | 0                   | 0 0 0 0                                         | $0$                              | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        |
| $V_{10}$ | 1                  | 1 1 1 1                                         | $0$                              | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        |
| $V_{11}$ | 1                 | 0 1 1 1                                         | $-V_{dc}/4$                      | $i_a$ $0$         | $v_{a}$          | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        |
| $V_{12}$ | 1                 | 1 1 0 1                                         | $-V_{dc}/4$                      | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        |
| $V_{13}$ | 1                 | 0 1 0 1                                         | $-V_{dc}/2$                      | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        |
| $V_{14}$ | 1                 | 1 1 0 0                                         | $-V_{dc}/2$                      | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        |
| $V_{15}$ | 1                 | 0 0 1 1                                         | $-V_{dc}/2$                      | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        |
| $V_{16}$ | 1                 | 0 0 0 1                                         | $-3V_{dc}/4$                     | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        |
| $V_{17}$ | 1                 | 0 0 0 0                                         | $-3V_{dc}/4$                     | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        |
| $V_{18}$ | 1                 | 0 0 0 0                                         | $-V_{dc}$                        | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        | $v_{a}$          | $0$ $i_a$        |

Note: “↑” and “↓” denote the charging and discharging of capacitors, respectively; “n” represents no current flows through the capacitors.

2.2 Potential characteristics

Any level general topology of the HSMC can be realised by stacking more FC-based cells in the SMC as demonstrated in Figure 3. Although the switches in higher-level HSMC can stand medium voltage, it is also suitable for low-voltage applications to obtain high-quality outputs because of its low power losses. If the dc-bus voltage is rated at $V_{dc}$, the voltages of $C_{f1}$ and $C_{f2}$ must be controlled to track the reference $V_{dc}/(2 \times n)$ as expressed by

$$v_{f1} = v_{f2} = \frac{V_{dc}}{2 \times n}(n - k + 1) \quad (k = 2, 3, \ldots, n). \quad (1)$$

The number of output voltage level for the $n$-cell HSMC is $4n + 1$. For example, when the stacked FC-based cell $n = 3$, the reference of $C_{f1}$ and $C_{f2}$ is $V_{dc}/3$, while the reference of $C_{f1}$ and $C_{f2}$ is $V_{dc}/6$, and the output voltage level is $(\pm V_{dc}, \pm 5V_{dc}/6, \pm 2V_{dc}/3, \pm V_{dc}/2, \pm V_{dc}/3, \pm V_{dc}/6, 0)$.

The application of the HSMC for three-phase areas (motor driver, flexible alternating current transmission systems (FACTs) etc.) can be realised like the traditional CHB. The dc-bus voltage can be supplied by one single dc source or three isolated multi-secondary transformers [14], and the recommended circuit of three-phase 9L-HSMC is presented in Figure 4. If it is applied to a compensating device, such as STATCOM, dynamic voltage regulator (DVR) and active power filter (APF), the dc source can be replaced with capacitors.

One of the critical issues of the HSMC is maintaining the FC voltage at the reference value during all conditions since it determines the quality of output voltage and current. Fortunately, there is a large number of redundant states that can be selected flexibly to balance FC voltages while obtaining the desired outputs. On the other hand, the number of power switches will be increased with the increase of voltage levels as can be seen in Figures 1 and 3. The failure rate of power switches will be increased in the long run, which may reduce system reliability. Therefore, proper modulation and control methods are required to obtain good performance while enhancing the system reliability.

For these above motivations, an MPC-based control strategy is developed for the 9L-HSMC to realise FC voltage balancing control and post-fault operations in the case of switch faults.

3 PROPOSED CONTROL STRATEGY

Due to its simplicity and flexibility, the MPC is a good option to reach the multiple control objectives in the HSMC system. Therefore, an MPC-based strategy is developed for the HSMC to minimise the errors between the outputs and their references. To achieve better tracking performance, the normalisation of state variables is implemented, which is used as an additional optimisation criterion in defining the cost function and tuning parameters.
3.1 Mathematical foundations

According to the switching states listed in Table 1, the output voltage \( v_a \) and current \( i_a \) can be formulated with \( v_f, S \) and switching functions \( S_{11}, S_{12}, S_{21} \) and \( S_{22} \):

\[
v_a(t) = \left( \frac{1}{2} V_{dc} - v_1(t) \right) S_{11} + \left( \frac{1}{2} V_{dc} - v_2(t) \right) S_{12} - V_{dc} S_1 + v_1(t) S_{21} + v_2(t) S_{22},
\]

where \( R \) and \( L \) represent the load resistance and inductance, respectively. The currents that flow through the FCs and dc-link capacitors can be expressed by

\[
\begin{align*}
  i_{f1}(t) &= (S_{11} - S_{21}) \cdot i_a(t) \\
  i_{f2}(t) &= (S_{12} - S_{22}) \cdot i_a(t) \\
  i_{c1}(t) &= - (S_1 + S_{11}) \cdot i_a(t) \\
  i_{c2}(t) &= -(2 - S_1 - S_{12}) \cdot i_a(t)
\end{align*}
\]

where \( i_{f1}(t), i_{f2}(t), i_{c1}(t) \) and \( i_{c2}(t) \) are instant currents of the FCs and dc-link capacitors; \( i_a(t) \) is the instant load current. The capacitor voltages can be therefore obtained as

\[
\begin{align*}
  v_{f1}(t) &= v_{f1}(0) + \frac{1}{C_f} \int_0^t i_{f1}(\tau) d\tau \\
  v_{f2}(t) &= v_{f2}(0) + \frac{1}{C_f} \int_0^t i_{f2}(\tau) d\tau \\
  v_{c1}(t) &= v_{c1}(0) + \frac{1}{C_d} \int_0^t i_{c1}(\tau) d\tau \\
  v_{c2}(t) &= v_{c2}(0) + \frac{1}{C_d} \int_0^t i_{c2}(\tau) d\tau
\end{align*}
\]

where \( x = 1, 2 \).

The continuous-time model described in Equations (4) and (5) is the first step to implement the estimations and predictions of the state variables for the proposed MPC algorithm. According to the mathematical foundations given in Equations (2) to (5), the control variables (phase current and capacitor voltages) are interrelated with each other. Therefore, the discrete-time predictive models of state variables can be derived from the mathematical formulations illustrated below.

3.2 Proposed MPC approach

3.2.1 Prediction of state variables

The control vector of state variables is defined as \( x = [v_{f1}, v_{f2}, v_{c1}, v_{c2}, i_a] \), and the continuous-time model described in Equations (2) to (5) must be transformed into discrete-time expressions to generate the predictive models of the state variables. The backward Euler algorithm is adopted to approximate the first-order derivation of the current \( i_a \) and it has

\[
\frac{di_a}{dt} \approx \frac{i_a(k+1) - i_a(k)}{T_s},
\]

where \( T_s \) is the sampling period.
where $T_s$ is the sampling time of the MPC, and $i_a(k), i_a(k+1)$ are the measured currents at the $k$th and $(k+1)$th sampling interval, respectively.

Substituting Equations (3) into (6) gives the predictive model of the phase current as

$$i_a(k+1) = \left(1-\frac{RL}{L}\right)i_a(k) + \frac{T_sr_z(k+1)}{L}r_z(k+1). \quad (7)$$

The predictive model of the output voltage $v_a(k+1)$ is obtained by discretising the continuous-time model in Equation (2), yielding

$$v_a(k+1) = \frac{1}{2}V_{dc} - \frac{1}{2}v_f(k)S_{k} + \left[\frac{1}{2}V_{dc} - \frac{1}{2}v_f(k)\right]S_{k+1} - V_{dc}S_{k} + v_f(k)S_{k+1} + v_f(k)S_{k+2} \quad (8)$$

The discrete-time model of capacitor currents at $k$ instant can be estimated by the following expressions:

$$
\begin{align*}
\iota_1(k) &= \left(S_{k} - S_{k+1}\right) \cdot i_a(k) \\
\iota_2(k) &= \left(S_{k+1} - S_{k+2}\right) \cdot i_a(k) \\
\iota_1(k) &= -\left(S_{k} + S_{k+1}\right) \cdot i_a(k) \\
\iota_2(k) &= -\left(2 - S_{k} - S_{k+1}\right) \cdot i_a(k)
\end{align*}
$$

By reusing the discretisation in the prediction step, we have the predictive model of capacitor voltages $v_{f_2}(k+1)$ and $v_{c_2}(k+1)$ ($\gamma = 1, 2$) at $k+1$ instant as

$$
\begin{align*}
v_{f_2}(k+1) &= v_{f_2}(k) + \frac{T_s}{C_f}i_{f_2}(k) \\
v_{c_2}(k+1) &= v_{c_2}(k) + \frac{T_s}{C_d}i_{c_2}(k)
\end{align*}
$$

3.2.2 Normalisation of state variables

As for the standard MPC algorithms, the optimum state that minimises the discrepancy between the references and measurements will be selected after the prediction of state variables. To improve the tracking performance, the dissimilarity of the variation ranges (high volts of voltage and low amperes of current) should be considered [21]. In this study, the normalisation is implemented by defining the maximum variations $\Delta V_{\text{max}}$ and $\Delta I_{\text{max}}$ of the capacitor voltages and load current, respectively. Substituting Equations (9) into (10) and arranging it, yield

$$
\begin{align*}
\Delta V_{f_1}(k) &= \frac{T_s}{C_f}\left(\left(S_{k} - S_{k+1}\right) \cdot i_a(k)\right) \\
\Delta V_{f_2}(k) &= \frac{T_s}{C_f}\left(\left(S_{k+1} - S_{k+2}\right) \cdot i_a(k)\right)
\end{align*}
$$

where $\Delta V_{f_1}(k)$ and $\Delta V_{f_2}(k)$ are the variations of the FC voltages between two adjacent sampling instants. According to the states from Table 1, the maximum variations can be obtained as

$$\Delta V_{f_1\text{max}} = \Delta V_{f_2\text{max}} = \frac{i_a}{C_f}T_s \quad (12)$$

Similarly, the maximum variations of the dc-link capacitor voltages can be expressed as

$$\Delta V_{d_1\text{max}} = \Delta V_{d_2\text{max}} = \frac{2i_a}{C_d}T_s \quad (13)$$

Substituting Equations (8) into (7) and making an approximate, the maximum variation of current $i_a$ can be calculated by

$$\Delta I_{\text{max}} = \frac{V_{dc}}{L}T_s \quad (14)$$

The variations of different state variables are depicted in Figure 5, where the variations are located within the maximum values $\Delta V_{\text{max}}, \Delta V_{f\text{max}}$ and $\Delta I_{\text{max}}$ for any measured point.

3.2.3 Optimisation criterion

The proposed MPC-based controller works in discrete time at each sampling time, which is too large than the fundamental cycle. Therefore, the reference current at $(k+1)$th sampling interval is generally approximated to be the value at $k$th. In actual operations, the reference current $i_a^*$ can be determined to realise the specific targets in different applications such as the renewable energy conversion systems, where the reference current is generated by the outer-loop controller for the real and reactive power regulation. Afterwards, the fourth-order Lagrange extrapolation method is adopted to extrapolate the reference phase current at $k+1$.

$$i_a^*(k+1) = 4i_a(k) - 6i_a(k-1) + 4i_a(k-2) - i_a(k-3) \quad (15)$$

where variables with superscript * denotes reference value. The defined cost functions contain the control objectives of minimising the deviation between the phase current $i_a(k+1)$, the capacitor voltages $v_{c_2}(k+1), v_{f_2}(k+1)$ ($\gamma = 1, 2$) and their
The implementation of the MPC approach can be divided into the following steps.

1. **Measurements**: The phase current $i_a(k)$ and capacitor voltages $v_{C1}(k)$, $v_{C2}(k)$, $v_{C3}(k)$, $v_{C4}(k)$ are measured at $k$ instant.

2. **Estimations**: The switching states designated to 9L-HSMC at ($k$-1)-th interval are not changed over one sampling cycle, which is used in the estimation of output voltage $v_o$.

3. **Predictions**: The obtained predictive models of phase current and capacitor voltages in Equations (7) to (10) utilize the estimations to predict the state variables at the ($k$+1)-th sampling interval.

4. **Optimisation algorithm**: The predictions of the phase current and capacitor voltages are evaluated for each redundant state that is listed in Table 1. Then, the optimum state which minimises the defined cost function $g$ should be applied to the HSMCs at the beginning of next sampling instant (i.e. $k$+1), and the control performance will be observed at ($k$+2)-th sampling instant.

### 3.2.4 Fault-tolerant operation

Due to their initial characteristics, the multilevel converters have a redundant switching state, which can be used flexibly to realise fault-tolerant operation by reconstructing the topologies and switching state combinations [30, 31]. There are two pairs of active bidirectional switches in 9L-HSMC, which are named inner and outer, respectively. The bidirectional switches work at high frequency, providing redundant current paths to balance the voltages of the dc-link capacitors and FCs. Moreover, it is possible to achieve the fault-tolerant operation if an open-circuit fault (OCF) occurs at the bidirectional switches. The post-fault circuits under OCFs of bidirectional switches are given in Figure 7.

Figure 7(b) shows the circuit under the OCF of inner switch $T_{12}$ or $T_{22}$, where $T_{11}$, $T_{21}$ and $T_{12}$ operate complementary with $T'_{11}$, $T'_{22}$ and $T'_{12}$, respectively. The reference voltage of $C_{11}$ and $C_{21}$ is $V_{dc}/4$, and the 5L-bridge can still be able to output five levels $\pm V_{dc}, \pm 3V_{dc}/4, \pm V_{dc}/2, \pm V_{dc}/4$ and 0 as presented in Table 2.

As shown in Figure 7(c), when the OCF occurs at the outer switch $T_{12}$ or $T'_{11}$, the 5L-bridge is degraded to a four-level bridge (viz. T-type nest NPC [31]). Here the switches $T_{11}$, $T_{21}$ and $T'_{22}$ operate complementary with $T'_{12}$, $T_{21}$ and $T_{22}$. In this case, the reference voltage of $C_{11}$ and $C_{22}$ should be set as $V_{dc}/3$, and seven voltage levels $\pm V_{dc}, \pm 2V_{dc}/3, \pm V_{dc}/3, 0$ can be obtained from Table 3.

As shown in Figure 7(d), the 5L-bridge changes into a three-level FCC bridge when OCF occurs at both inner and outer switches. In the post-fault circuit, $(T_{11}, T_{12})$ and $(T_{21}, T'_{22})$ are two complementary switching pairs. The reference voltage of $C_{11}$ and $C_{22}$ is controlled at $V_{dc}/4$, and then five levels $\pm V_{dc}, \pm V_{dc}/2, 0$ will be generated from Table 4.

As can be seen from Figure 7, the number of available switching states will be reduced in the post-fault circuits, which may decrease the balance capability of the FC voltages. Since the

![Flowchart of the proposed model predictive control strategy for 9L-HSMC system](image-url)
fault-tolerant operation is an emergency case, the proposed MPC strategy is modified for the HSMCs to achieve continuity operation. The system reliability is enhanced with reduced capacitor voltage balancing ability and deterioration of power quality.

Figure 8 shows the fault-tolerant operation modes for the HSMC under OCFs at bidirectional switches. Note that, since the switches of 2L-HB bridge work at the fundamental frequency, the probability of fault is assumed quite lower than that of 3L/4L-HSMC switching states, output voltage and effects on the FCs (fault occurs at the inner and outer bidirectional switches)

| States | $S_1$ | $S_{11}$ | $S_{21}$ | Output voltage $v_a$ | FC voltages $v_{1j}, v_{2j}$ |
|--------|-------|---------|---------|----------------|-----------------|
| $V_1$  | 0     | 1 1 1   | $V_{dc}$ | $n$            | $n$             |
| $V_2$  | 0     | 0 1 1   | $V_{dc}$ | $n$            | $n$             |
| $V_3$  | 0     | 1 0 1   | $V_{dc}$ | $n$            | $n$             |
| $V_4$  | 0     | 0 1 0   | $V_{dc}$ | $n$            | $n$             |
| $V_5$  | 0     | 0 0 1   | $V_{dc}$ | $n$            | $n$             |
| $V_6$  | 0     | 0 0 0   | $V_{dc}$ | $n$            | $n$             |
| $V_7$  | 1     | 1 1 1   | $V_{dc}$ | $n$            | $n$             |
| $V_8$  | 1     | 0 1 1   | $V_{dc}$ | $n$            | $n$             |
| $V_9$  | 1     | 1 0 1   | $V_{dc}$ | $n$            | $n$             |
| $V_{10}$ | 1   | 0 1 0   | $V_{dc}$ | $n$            | $n$             |
| $V_{11}$ | 1  | 0 0 1   | $V_{dc}$ | $n$            | $n$             |
| $V_{12}$ | 1  | 0 0 0   | $V_{dc}$ | $n$            | $n$             |
FIGURE 9 Fault-tolerant operation with OCF at single bidirectional switches. (a) Fault-tolerant mode I (inner switch fault), (b) fault-tolerant mode II (outer switch fault)

of high frequency (HF) switches in 5L-SMC bridge; thus, the circuit faults at the low frequency (LF) switches were not considered. Due to the limitation of space, the diagnosis methods of OCFs are not discussed and they can be found elsewhere [30]. After circuit faults of inner/outer bidirectional switches are localised, the corresponding fault-tolerant control must be activated. It should be noted that the proposed control strategy will not be applicable when OCF occurs at the switches $T_{11}, T_{21}, T'_{21}$ and $T'_{12}$. In this case, the zero level cannot be output in the 5L-bridge while maintaining the balance of capacitor voltages.

4 | SIMULATION RESULTS

4.1 | Fault-tolerant operation

In order to obtain the performance of the MPC-based fault-tolerant control strategy, simulations were conducted. The dc bus is supplied by a constant dc power source $V_{dc} = 50$ V, and the ac output terminal is connected in series with a linear $RL$-load ($R = 15$ Ω, $L = 4.3$ mH). The dc-link capacitor $C_d$ and the FC capacitor $C_f$ are 2200 and 1000 μF, respectively. The sampling frequency of the controller is set as 20 kHz. Figures 9 and 10 plot the voltage, current and FC voltages of 9L-HSMC with OCF occurring at the bidirectional switches. It can be seen that the current $i_a$ has no significant deterioration under fault-tolerant operation, and it shows good tracking performance even during the transient cases.

As shown in Figure 9(a), when the OCF occurs at the inner switches, 9L voltage $v_a$ remains attainable and the FC voltages $v_f^1, v_f^2$ are balanced with a voltage ripple of $\sim 0.4$ V. Due to the reduction of available switching states, there exist unexpected commutations in the phase voltage $v_a$ in order to balance the FC voltages. Figure 9(b) displays the waveforms when the OCF occurs at the outer switches, the $v_f^1, v_f^2$, are regulated from $V_{dc}/4$ to $V_{dc}/3$ after 50 ms, and then $v_a$ changes from 9L to seven level.

Once the OCF occurs at both inner and outer switches, the 5L-SMC bridge will be degraded to the FCC bridge. As shown in Figures 10(a) and (b), if the $v_f^1, v_f^2$ are controlled at $V_{dc}/6$ and $V_{dc}/4$, the $v_a$ changes from 9L to seven level and 5L, respectively. Although the voltage level of $v_a$ decreases, the amplitude of $i_a$ is not decreased and the FC voltages are still balanced and maintained at their reference values. The capacitor voltages $v_{dc1}$ and $v_{dc2}$ are balanced by using the proposed control strategy under the normal and inner switch fault modes, and the simulation waveforms are presented in Figure 11, whereas they do...
not need to be balanced under the faults of outer switches $T'_{12}$ and $T'_{11}$ since there is no current flow through the neutral point. Moreover, the THD of the output voltage $v_a$ and load current $i_a$ is studied under different operation modes by using the fast fourier transform (FFT) toolbox, and the results are listed in Table 5. The THD values are higher than that of the normal mode, which is acceptable since the fault modes are emergency cases. Overall, the desired outputs and fault-tolerant operation are both achieved as expected by using the proposed MPC-based strategies.

### 4.2 Blocking voltages of switches

The voltage stress is an essential part of the design of inverters, as it determines the volume and costs. The blocking voltage of the power device is defined as the maximum voltage stress across the device during the OFF state. The blocking voltages for each switching state under the normal and fault-tolerant modes are presented in Figure 12. The LF-cell switches have to stand full dc-bus voltage $V_{dc}$, while the blocking voltage of HF-cell switches varies from 0 to $2/3 V_{dc}$. It is possible to equip the HSMC topologies with different types of switches to explore their advantages (e.g. Si insulated gate bipolar transistors (Si-IGBTs) for HF cell and SiC metalor (SiC-oxideor (SiC-semiconductor field-effect transistor (SiC-MOSFET) for LF cell).

### 4.3 Dynamic performance

In order to verify the dynamic performance of the 9L-HSMC with the proposed control strategy, transient simulations were conducted with a step change of reference current. The results are shown in Figure 13, where the output voltage and current and FC voltages are plotted. The voltage level of $v_a$ changes from five to nine when the equivalent modulation $m$ increases from 0.3 to 0.9. The FC voltages can be balanced with the proposed MPC strategy during the transient case, and the voltage ripples are below 5% of their nominal value ($V_{dc}/4$).

### 4.4 Power losses distributions

To evaluate the effectiveness of the proposed control strategy, the power losses of the 9L-HSMC including switching loss and conduction loss are studied. The conduction losses are determined by the on-state equivalent resistance and forward voltage drops, while the switching losses are estimated by the linear approximation of voltage and current through $k$th switch [32].

The power losses were calculated by MATLAB/Simulink based on the constructed loss models. The main circuit of the 9L-HSMC is constructed by using Infineon switches (FZ400R17KE3) with a rating of 1700 V/400 A. To make the loss analysis reasonable, the dc-link voltage is set as $V_{dc} = 1$ kV in this section. Figure 14 portrays the percentage of power losses distribution for 9L-HSMC. As can be observed from

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**TABLE 5** THD of voltage and current under different operation modes

| Modes                  | Voltage THD$_v$ (%) | Current THD$_i$ (%) |
|------------------------|---------------------|---------------------|
| Normal mode            | 18.60               | 1.60                |
| Fault-tolerant mode I  | 18.78               | 1.66                |
| Fault-tolerant mode II | 48.72               | 5.09                |
| Fault-tolerant mode III| 61.35               | 6.00                |

**FIGURE 11** DC-link capacitor voltages under normal and fault-tolerant mode I

**FIGURE 12** Blocking voltages of switches for each switching state. (a) Normal mode (Figure 7(a)), (b) fault-tolerant mode I (Figure 7(b)), (c) fault-tolerant mode II (Figure 7(c)), and (d) fault-tolerant mode III (Figure 7(d))
Figure 13 shows the transient simulation results of 9L-HSMC with step change of equivalent modulation index $m$ from 0.3 to 0.9.

Figure 14(a) shows the distribution of conduction losses for each switch in 9L-HSMC. Figure 14(b) shows the distribution of switching losses.

Figure 15(a) shows the bar chart of power losses for 9L-HSMC. Figure 15(b) shows the efficiency plot versus the equivalent modulation index $m$.

5 | EXPERIMENTAL VALIDATIONS

In order to verify the developed MPC for the HSMCs, an experimental platform was built as photographed in Figure 16. The experimental HSMC system is composed of the main circuit, sensor circuits, driving boards and controller. The Infineon IGBTs (IFW15N120E) and electrolytic capacitors are used to construct the main circuit. The dc voltage is supplied by a constant dc source, while the ac output is a series connected with a pure resistor load through a filtering inductor. A real-time board/module MicroLabBox is used to implement the analog digital conversion (ADC), logical calculations and control approaches. The detailed parameters used in the experiment are summarised in Table 6.

### Table 6: Experiment Parameters

| Symbols | Parameters | Values |
|---------|------------|--------|
| $V_{dc}$ | DC-bus voltage | 50 V |
| $f_0$ | Output frequency | 50 Hz |
| $f_s$ | Sampling frequency | 20 kHz |
| $C_f$ | Flying capacitance | 1 mF |
| $C_d$ | DC-link capacitance | 2200 µF |
| $L$ | Load inductance | 4.3 mH |
| $R$ | Resistor load | 15 Ω |
| $t_d$ | Dead-band time | 2.5 µs |
Initially, the HSMC works under steady-state condition, and the experiment results are plotted in Figures 17 and 18. Here, the modulation index $m$ is 0.85 and an RL-load ($R = 15 \ \Omega$, $L = 4.3 \ \text{mH}$) is connected between the output terminals. Figure 17(a) shows the output voltage $v_{ao}$ between ac terminal $X_1$ and the neutral point $O$, whereas the phase voltage $v_a$ and current $i_a$ are given in Figure 17(b). As can be seen from Figure 17, the output voltage $v_{ao}$ and $v_a$ are obtained well with five and nine levels, respectively. Figure 18 shows the deviations of capacitor voltages ($\Delta v_{dc} = v_{c1} - v_{c2}$; $\Delta v_{fc} = v_{f1} - v_{f2}$), phase current and its reference signal. It can be found that the value of $\Delta v_{dc}$, $\Delta v_{fc}$ are nearly null and the current tracking errors are quite small, with merely small high-frequency ripples observed.

### 5.2 Dynamic performance

In order to unveil the dynamic performance of the MPC for the 9L-HSMC, several typical transient cases are investigated. Figure 19 presents the experiment waveforms of capacitor voltages under the start-up and step-changing of the dc-bus voltage $V_{dc}$ from 50 to 35 V. As can be seen from Figure 19, the $v_{c1}$, $v_{c2}$ and $v_{f1}$, $v_{f2}$ are fully balanced well and maintained at their reference values $V_{dc}/2$ and $V_{dc}/4$, respectively. Figure 20(a) and (b) demonstrate the experiment results with step decreases of the equivalent modulation index $m$ (from 0.85 to 0.6) and (from 0.85 to 0.4), respectively. As can be seen from this figure, the voltage level is degraded to seven and five, respectively. But, the FC voltages are balanced well, and no significant voltage ripples are observed even during the transient process. In addition, the measured results with the output frequency $f_{out}$ changing from 50 to 100 Hz are presented in Figure 21, which tells us that the tracking performance of the output voltage $v_a$ and current $i_a$ are verified, and no voltage spikes occur in the FC voltages, even during the transient process.

### 5.3 Sensitivity of parameter mismatches

The effect of parameter mismatches on the response of the MPC-based HSMC is also investigated, and the $R$ and $L$ that
FIGURE 20  Experiment results of 9L-HSMC with step changes at the equivalent modulation index $m$: (a) from 0.85 to 0.6, (b) from 0.85 to 0.4

FIGURE 21  Experiment results of 9L-HSMC with step changing at output frequency $f_{ou}$ from 50 to 100 Hz

FIGURE 22  Transient experiment results of 9L-HSMC working under significant mismatches of load parameters: (a) $R = 7.5$ to 20 $\Omega$, (b) $L = 2.15$ to 9 mH

6  |  CONCLUSION

This paper proposes an MPC strategy for the HSMCs with low conduction losses and superior output quality. The MPC strategy is designed to balance the capacitor voltages while obtaining the desired outputs. These control objectives are achieved by minimising the single costs function, making the complex linear regulators and PWM modulators absent. Moreover, the flexibility of the fault-tolerant operation can be reached by using the MPC-based control strategy, which enhances the system reliability. Power losses of 9L-HSMC are well evaluated, and the switching losses of the 2L-HB merely amounts to 0.2%. Experimental validations were carried out for the HSMCs under various typical operating conditions. The measured results verify the expected performance of the HSMCs in both the steady and dynamic states, confirming the effectiveness of the proposed MPC-based control strategy.

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