Realization of Strong CMOS Conforming Full Adder Circuit Using Symmetric Function Lattice Structure

Muhammad Mustapha¹, Bakhtiar Affendi Rosdi², Tengku Norliza Tengku Mohamad¹, Anis Shahida Niza Mokhtar¹

¹Department of Electrical and Electronics Engineering, Faculty of Engineering, National Defense University of Malaysia, Sungai Besi Camp, 57000 Sungai Besi, Kuala Lumpur, Malaysia
²School of Electrical & Electronics Engineering, Universiti Sains Malaysia, 14300 Nibong Tebal, Malaysia

E-mail: muhazam@upnm.edu.my, muhazam.mustapha@gmail.com

Abstract. Due to the physical limit that the IC industry may face in the future that transistors size may not be able to shrink anymore, a lot of work had been done to minimize the number of transistors used, instead of shrinking them. One of the highly researched standard circuit to reduce transistor count is the full adder as it appears in almost all computing circuits. In this paper, an alternative to CMOS technology using symmetric Boolean function lattice structure is presented to produce full adder. Symmetric functions are the functions that are invariant under input permutation. They have a special way of realization that offers some possibility to reduce the number of transistors used. Full adder falls into this class of functions. It has been found that the right full adder lattice structure based circuit only requires 22 transistors to produce the correct function for the sum and c output. This is a saving of 6 transistors compared to the standard 28-transistor CMOS full adder. The output delay is around 3.0 ns for the c output, and around 4.5 ns for the sum output.

1. Introduction

In integrated circuit (IC) technology, producing the smallest possible die area is one of the ultimate goals. This had been achieved by reducing the transistor size in the fabricated circuits. However, as the transistor size approaches a few tens of nanometers, physics of the transistor itself changes.

As the technology reaches this condition, other alternatives have been explored by researchers to achieve the same objective of reducing die size, for example, by reducing the number of transistors used to realize certain kind of circuits. Particularly, one of the most extensively studied circuit is the circuit of full adder.

The reason why researchers focus on full adder is because full adder constitutes most of the computing circuits as almost all computations will transcend to either addition or subtraction, where both of these two fundamental operations are realized using multi-bit adders built based on 1-bit full adders.

CMOS technology has its own standard 28-transistor full adder circuit. To efficiently use transistors in full adder circuit, other non-strict-CMOS approaches have been studied. Notably, two alternative technologies, i.e. pass transistor logic (PTL) [3, 13] and gate diffusion input...
(GDI) [9, 10, 11, 12] techniques have received very serious attention from the researchers to obtain full adders with fewer transistors transistor count. Some work has shown very impressive results, including full adder circuit containing as few as 6 transistors only [3].

The alternative presented in this paper is a realization of full adder using a circuit built from symmetric function lattice structure [4].

2. Related Work

Full adder is such an important and significant circuit to be concerned in digital systems that when a new switching technology is invented, full adder circuit is the first to be constructed and studied in very detailed using this new technology. For example, after the invention of carbon nanotube FET (CNTFET), researchers didn’t waste any time to start studying on how to perfect full adder circuit with it [2, 6, 14]. Even for a technology that is seemingly not a good candidate for switching - like in magnetic material technology - once a technique was invented to create switches with it, researchers quickly focus on building efficient full adders using it [8, 15]. The two MOSFET circuit families that received very intensive work to fabricate smaller transistor count full adder are the pass transistor logic (PTL) and gate diffusion input (GDI) technologies.

PTL is the technique of constructing MOSFET circuit by allowing input signals to power up transistors and current flows from the input into the channel. This technique started first by fabricating the smallest transistor count circuit for XOR/XNOR gate. The reason is because XOR/XNOR constitutes a large portion of full adder circuit (Figure 1). The researchers managed to build XOR/XNOR using only 3 transistors (Figure 2), and the resulting full adder has only 8 transistors [3]. However, such a low transistor count XOR/XNOR gate obviously suffers from serious performance issues that the perfected full adder using the same idea was using a 10-transistor XOR/XNOR gate that resulted in an 18-transistor full adder [1].

GDI on the other hands is a technique to construct gates using elements that look like CMOS inverter, but like PTL, it allows input signals to power on the inverter or become the ground.
Figure 3 shows the list of basic GDI-based gates [5]. Through a mixture of GDI technique with an even lower transistor count XOR (2-transistor XOR) gate obtained using PTL technology, a 9-transistor full adder was able to be realized [7].

3. Methodology
Unlike the techniques presented in the related work section, the alternative presented in this paper is still very close to standard CMOS full adder, but with some deviation. This proposal is based on a classic idea of symmetric Boolean functions that can be realized using a special circuit called lattice structure [4]. The complete design of the proposed lattice structure full adder is in Figure 8. This methodology section will explain stage-by-stage how that complete circuit is obtained from a lattice structure that gives the function of \( C_{out} \).

3.1. Symmetric Boolean Functions
Symmetric Boolean functions are Boolean functions that are invariant under input permutation. For 2-variable Boolean functions there are 8 such functions:

(i) \( f(a, b) = 1 = f(b, a) \)
(ii) \( f(a, b) = 0 = f(b, a) \)
(iii) \( f(a, b) = ab = ba = f(b, a) \)
(iv) \( f(a, b) = a + b = b + a = f(b, a) \)
(v) \( f(a, b) = \overline{ab} = \overline{ba} = f(b, a) \)
(vi) \( f(a, b) = a + b = b + a = f(b, a) \)
(vii) \( f(a, b) = a \oplus b = b \oplus a = f(b, a) \)
(viii) \( f(a, b) = a \oplus b = b \oplus a = f(b, a) \)

For this type of functions, there is a special circuit that can realize them with less transistors called lattice structure [4]. Figure 4 shows the lattice structure for 3-variable symmetric functions. The output of the functions are taken from the output points; if the function gives logic 1 when there are \( n \) variables having logic 1, then the output is taken from point \( n \). If the function gives logic 1 with more than one combination of logic 1s in the input, then the respective points can be combined to obtain the function.

3.2. The Symmetry of Full Adder

Table 1 shows the truth table of full adder. It is easy to understand that full adder is symmetric because the 1-bit addition of \( a + b + c_{in} \) is commutative, i.e. invariant under the input permutation.

One property of symmetric functions is that the output logic is the same for combinations of variables with the same number of logic 1s at the inputs. For the case of full adder, the output \( \text{sum} \) gives a 1 when there is one 1 in the inputs, or when there are three 1s in the input; and output \( c_{out} \) gives a 1 when there are two 1s in the inputs, or when there are three 1s in the input. These correspond to minterms 1, 2, 4 and 7 for \( \text{sum} \), and minterms 3, 5, 6 and 7 for \( c_{out} \). This property will later be used in the formation of the lattice structure circuit of the function.

| minterm | \( a \) | \( b \) | \( c_{in} \) | \( c_{out} \) | \( \text{sum} \) | No. 1s |
|---------|--------|--------|-------------|-------------|-------------|-------|
| 0       | 0      | 0      | 0           | 0           | 0           | 0     |
| 1       | 0      | 0      | 1           | 0           | 1           | 1     |
| 2       | 0      | 1      | 0           | 0           | 1           | 1     |
| 3       | 0      | 1      | 1           | 1           | 0           | 2     |
| 4       | 1      | 0      | 0           | 0           | 1           | 1     |
| 5       | 1      | 0      | 1           | 1           | 0           | 2     |
| 6       | 1      | 1      | 0           | 1           | 0           | 2     |
| 7       | 1      | 1      | 1           | 1           | 1           | 3     |

3.3. Full Adder Lattice Structure

Figure 5 shows the outputs of the original lattice structure needed to produce full adder \( \text{sum} \) function. Since \( \text{sum} \) function gives a 1 when the number of 1s in the inputs is either 1 or 3, the respective outputs of the lattice structure corresponding to that numbers are connected together (Figure 5 (a)). After that all transistors that are not in the path from those outputs can be removed (Figure 5 (b)).

For the case of \( \text{sum} \), the circuit cannot be reduced anymore, so this 9-transistor circuit as in Figure 5 (b) is the final one for both push-up and pull-down networks.
Figure 5. Lattice circuit structure to give sum output

Figure 6. Lattice circuit structure to give \( c_{\text{out}} \) output

Figure 6 on the other hands shows the outputs of the original lattice structure needed to produce full adder \( c_{\text{out}} \) function. Since \( c_{\text{out}} \) function gives a 1 when the number of 1s in the inputs is either 2 or 3, the respective outputs of the lattice structure corresponding to that numbers are connected together (Figure 6 (a)). After that, all transistors that are not in the path from those outputs can be removed (Figure 6 (b)).

For the case of \( c_{\text{out}} \), the resulting circuit can be reduced further. By inspection it is found that the minimum required circuit is a 5-transistor circuit as in Figure 7. Again, this is for both push-up and pull-down networks. Since \( c_{\text{out}} \) lattice structure uses less transistor than the \( \text{sum} \) lattice structure, \( c_{\text{out}} \) circuit will be used to obtain \( \text{sum} \) circuit as they are near complement functions (explained in Subsection 3.5).

3.4. Lattice Structure Circuit for Inverted \( c_{\text{out}} \)

To get the lattice structure circuit that gives out \( c_{\text{out}} \) as in Figure 8, the circuit in Figure 7 will be connected to ground at the left bottom point. This will give the pull-down network. The
push-up network is a similar circuit but flipped up and the PMOSs are replaced by NMOSs, and vice versa.

The lattice structure circuit does give out an inverted \( c_{\text{out}} \) function, but the signal is weak due to the presence of PMOS in the pull-down network and the presence of NMOS in the push-up network.

From the weak \( c_{\text{out}} \) signal, it is easy to obtain a strong \( c_{\text{out}} \), i.e. by inverting it. That output signal is shown in Figure 8.

3.5. Near Complement Functions

The rest of the full adder circuit in Figure 8 is to manipulate the \( c_{\text{out}} \) signal to obtain \( \text{sum} \) signal. This is possible because full adder’s \( \text{sum} \) and \( c_{\text{out}} \) are near complement functions. Near complement functions are functions that are almost complementing (inverted) to each other, except at a few minterms where they have the same outputs. For the case of \( \text{sum} \) and \( c_{\text{out}} \), the functions are complementing to each other except for minterms 0 and 7 where they have the output of 0 and 1 respectively. Due to this fact, \( \text{sum} \) function can be obtained from \( c_{\text{out}} \) by inverting it except for minterms 0 and 7. This is called selective inversion.
3.6. Multi-input Inverter
To achieve the selective inversion as suggested in Subsection 3.5, multi-input inverter is used. A multi-input inverter is an inverter with more than one inputs. The output is 1 when all inputs are 0, and the output is 0 when all inputs are 1. For all other combinations the inverter has high impedance output and can be considered unconnected to (hence will pass through) the other one input that is directly connected to the output. Such multi-input inverter is shown in Figure 8 just before the final inverter to obtain sum signal, and its truth table is in Table 2.

| a | b | cin | Output |
|---|---|-----|--------|
| 0 | 0 | 0   | 1      |
| 0 | 0 | 1   | High-Z |
| 0 | 1 | 0   | High-Z |
| 0 | 1 | 1   | High-Z |
| 1 | 0 | 0   | High-Z |
| 1 | 0 | 1   | High-Z |
| 1 | 1 | 0   | High-Z |
| 1 | 1 | 1   | 0      |

A multi-input inverter consists of PMOS transistors connected serially from the \(V_{DD}\), and NMOS transistors connected serially to ground. The signal that is to be selectively inverted will pass through in the middle. When all the inputs connected to the gates of the MOSs are 1, there is a strong connection through the NMOSs to the ground, hence the output is 0. When all the inputs connected to the gates of the MOSs are 0, there is a strong connection through the PMOSs to \(V_{DD}\), hence the output is 1.

With other input combinations, i.e. when there is at least one 1 at the PMOSs’ gate, or when there is at least one 0 at the NMOSs’ gate, there is no connection from the output in the middle to \(V_{DD}\) or ground. In this case the output is floating, hence it will pass the weak signal coming from the follower. It is obvious now that the middle signal to the multi-input inverter has to be weak otherwise the series connection of the PMOSs and NMOSs might not be strong enough to perform the selective inversion.

3.7. \(c_{out}\) Follower
For the multi-input inverter to work, it requires a weak signal. In this case, a weak \(c_{out}\) signal. This is done by passing the \(c_{out}\) signal through a follower (or buffer, located in the middle of Figure 8). The weak signal will then be passed through the multi-input inverter.

3.8. Final \(c_{out}\) and sum Outputs
Finally the correct sum signal is obtained by inverting the output of the multi-input inverter because at that stage the signal is still a weak inverted sum. The \(c_{out}\) signal on the other hands was obtained directly from the weak \(c_{out}\) that is coming out directly from the lattice structure.

4. Analysis
The main objective of this paper is to document, share and report a successful construction of a complete full adder circuit using a classic idea of symmetric function. The analysis that follows
the result at this stage is the one that would verify the correctness of the obtained functions and its conformance to contemporary technology which in this case is CMOS.

As for the correctness of the sum and \( c_{\text{out}} \) functions, Figure 9 proves that it is achieved. The figure also shows that the outputs have strong levels of almost 1.2V (\( V_{\text{DD}} \)) logic 1 and almost 0V logic 0. The reason for this is because they are pulled out from inverters. Outputs being taken from inverters is also a recommended construct in CMOS systems.

As for speed, Figure 10 shows the worst case scenario of response time that took place when \( c_{\text{in}} \) changes from 1 to 0 when \( a = 0 \) and \( b = 1 \). The value is around 3ns for \( c_{\text{out}} \) and 4.5ns for sum. All simulations are on Mentor Graphics Pyxis tool with 0.35nm technology from Siltera libraries with 1.2V \( V_{\text{DD}} \).
5. Conclusion

This paper presents a report on the design methodology of lattice structure based full adder. Though the design successfully gives the required sum and cout functions with less transistor count than the standard 28-transistor full adder, a more detailed analysis is needed to decide on any advantages or disadvantages of this design as compared to the standard one or the new designs in the related works. This is opened for the next publication of this research.

References

[1] Amini-Valashani M, Ayat M, Mirzakuchaki S. Design and analysis of a novel low-power and energy-efficient 18T hybrid full adder. Microelectronics Journal, Elsevier Science Direct, vol. 74, pp. 49-59, 2018.
[2] Firouzi S, Tabrizi S, Sharifi F, Badawy AH. High performance, variation-tolerant CNFET ternary full adder a process, voltage, and temperature variation-resilient design. Computers and Electrical Engineering, Elsevier Science Direct, vol. 77, pp. 205-216, 2019.
[3] Geetha PM, Baskaran K. Low Power Full Adder with Reduced Transistor Count. International Journal of Engineering Trends and Technology (IJETT), vol. 4, no. 5, pp. 1755-1759, 2013.
[4] Harisson MA, Introduction to Switching and Automata Theory, McGraw Hill, 1965.
[5] Hasan M, Zaman HU, Hossain M, Biswas P, Islam S. Gate Diffusion Input technique based full swing and scalable 1-bit hybrid Full Adder for high performance applications. Engineering Science and Technology, an International Journal, Elsevier Science Direct, article in press, 2020.
[6] Joqq MKQ, Bozorgmehr A, Mirzakuchaki S. A low power and energy efficient 4:2 precise compressor based on novel 14T hybrid full adders in 10 nm wrap gate CNTFET technology. Microelectronics Journal, Elsevier Science Direct, vol 104, 2020.
[7] Kumar SS, Rakesh S. A Novel high-speed low power 9T full adder, International Multi-conference on Computing, Communication, Electrical & Nanotechnology, proceedings in Materials Today: Proceedings, Elsevier Science Direct, vol 24, pp. 1882-1889, 2020.
[8] Mamaghani SB, Moaiyeri MH, Jaberipur G. Design of an efficient fully nonvolatile and radiation-hardened majority-based magnetic full adder using FinFET/MTJ. Microelectronics Journal, Elsevier Science Direct, vol 103, 2018.
[9] Morgenshtein A, Fish A, Wagner IA. Gate Diffusion Input (GDI) - A Novel Power Efficient Method for Digital Circuits: A Design Methodology. in 14th ASIC/SOC Conference, Washington DC, USA, 2001.
[10] Morgenshtein A, Fish A, Wagner IA, Gate Diffusion Input (GDI) - A Power-Efficient Method for Digital Combinatorial Circuits, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol 10, no. 5, pp. 569-581, 2002.
[11] Morgenshtein A, Fish A, Wagner IA. Gate Diffusion Input (GDI) - A Technique for Low Power Design of Digital Circuits: Analysis and Characterization. in Proc. IEEE International Symposium on Circuits and Systems, Phoenix-Scottsdale, Arizona, USA, 2002.
[12] Morgenshtein A, Shwartz I, Fish A. Gate Diffusion Input (GDI) Logic in Standard CMOS Nanoscale Process, in Proc. IEEE 26th Convention of Electrical and Electronics in Israel, Eilat, 2010.
[13] Reddy GK. Low Power-Area Pass Transistor Logic Based ALU Design Low Power Full Adder Design, in IEEE Sponsored 9th International Conference on intelligent Systems and Control (ISCO), Coimbatore, Tamilnadu, India, 2015.
[14] Tari HT, Zarandi AD, Reshadinezhad MR. Design of a high performance CNFET-based full adder cell applicable in: Carry ripple, carry select and carry skip adders. Microelectronics Journal, Elsevier Science Direct, vol 215, 2019.
[15] Zarei A, Safaei F. Power and area-efficient design of VCMA-MRAM based full-adder using approximate computing for IoT applications, Microelectronics Journal, Elsevier Science Direct, vol 82, pp. 62-70, 2018.