Performance analysis of carbon nanotubes for future high-speed VLSI on-chip interconnect applications

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Abstract

In VLSI, while we pass into a sub-micron stage, power dissipation and propagation delay problems occur mainly due to the interconnect parasitic. This motivates the designing of low power interconnects with less propagation delay. This work analyzed the crosstalk induce delay of on-chip interconnects such as copper, SWCNT, and MWCNT with resistive, CMOS and CNTFET drivers to improve the performance metrics. A two-line driver-interconnect-load (DIL) system is used to analyze the crosstalk induced delay for different interconnect lengths by calculating the equivalent R, L and C parameters of copper and CNT based interconnects. From the simulations, it has been observed that MWCNT interconnects given better performance than conventional copper and SWCNT interconnects when driving through CNTFET driver in terms of power and delay. It is almost given more than 50% lesser delay and power consumption in comparison with others. Additionally, we have performed the crosstalk peak voltage analysis for different interconnect lengths and it is evident that crosstalk can be reduced by changing the coupling and load capacitances. Moreover the MWCNTs have given a 55% lesser noise peaks than the conventional copper interconnects.

Keywords: Carbon nanotube FETs (CNFETs), CMOS, Single walled carbon nanotube (SWCNT), Multi walled carbon nanotube (MWCNT), interconnects

I. Introduction

In recent days, it is much needed to deal with low power and high-speed devices in an integrated circuit. Due to the continuous scaling of integrated circuits and frequency growing, wire propagation delay becomes a major bottleneck in estimating the performance of the system [XIII]. In practice, the interconnecting wires cannot be a simple resistor when transistor sizes enter into the nanometer ranges, it also contains parasitic components like capacitance and inductance, and all need be
considered for performance evaluation [VIII, XIX]. Thus any signal propagating through such an interconnect can be expected to be delayed.

Basically interconnects are used in routing the clock and process the logic signal to various other blocks. Interconnects are divided based on its parasitic elements and length such as local, global and semi-global interconnects [XI]. Local interconnects are very small in size, having less parasitics and cover the small distance in the chip. Semi-global is larger than local interconnects, and they provide high parasitic than local. These are basically used to connect input and output circuitry with large modules. Global interconnects are the one that provides larger parasitics because of large in size and generally used to route the clock, power supply, and other long-distance communications in various functional blocks [VI, XVI].

Normally used interconnect materials are copper and aluminum because they have a high melting point, low resistivity, ease of deposition and good adhesion to dielectrics. As technology is scaling down the resistivity of copper also increases and this imparts propagation delay on the line. Therefore, the better alternative to copper as the size shrinking is done is carbon nanotube (CNT). CNTs are the most promising materials used to work at high speed and low power interconnects. These are categorized as single-walled Carbon Nanotubes (SWCNTs) and multi-walled Carbon Nanotubes (MWCNTs) [III, X, XII]. In practice, MWCNT interconnects offers less resistance when compared to SWCNT interconnects [VII]. There are other techniques that have been proposed to reduce signal transition delays such as buffer or repeater insertion techniques, but they have not reported for CNT based interconnects [V, XV]. The researchers observed the inductance effects with buffer insertion techniques to reduce interconnect delay [I, II, IV, XVIII, XXIII]. Sandeepsaini et al. [XX] proposed an alternate buffer insertion technique for conventional copper interconnects. However, this analysis limited to conventional copper interconnects only.

In this paper, the delay analysis is extended to CNT based interconnects such as SWCNT and MWCNT interconnects with CNTFET drivers and compared with conventional copper interconnects and conventional CMOS buffers. The simulation model has been made by RLC equivalent circuit and performed the delay, power and crosstalk analysis. We have been observed that, MWCNT interconnects with aCNTFET driver has reduced the total time delay by a larger extent when compared to conventional copper interconnects with resistive and CMOS drivers. Further, the crosstalk analysis also performed by adding the model file of CNFET, and it has been observed that the combination of CNFET with MWCNT interconnects has given better performance than others. All the simulations have performed in 32nm technology nodes. The rest of the paper is organized as follows: section 2 deals about CNTFET. The performance analysis to minimize delay and power and noise is discussed in section 3. Finally, section 4 concludes the work.

II. Carbon nanotube field effect transistor

Carbon nanotubes are a new form of carbon with a perfect crystalline structure which is composed of strong C-C bonds. The carbon tube-like structures are formed by folding graphite layers into carbon cylindrical structure. This type of carbon tubes has unique properties based on the folding angle of the sheet. Based on the chirality,
the carbon nanotubes behave either metallic or semiconducting, and the semiconducting tubes properties are used in the transistors fabrication. These tubes are used as a channel instead of bulk silicon as in the typical silicon MOSFET. The channel is formed between the source and drain terminals using either a single CNT or an array of CNT’s. The typical diameter of CNTs is 1-2nm and the length in micro meter range. As compare to MOSFET, CNTFET has high conductance, this helps to a ballistic transport of carriers in the channel [IX, XIV, XXI, XXII]. The triggering voltages are also less compared to MOSFET. The fabrication process of CNTFET difficult as compared to MOSFET due to their chirality index. However, based on the chirality CNTs behaves like a metal and semiconductor. The semiconductor properties are used for making devices, and the CNTFET structure is shown in Fig. 1.

![Fig 1: Structure of CNTFET](image)

Carbon nanotube used as a channel in CNTFET between the source and drain terminals. There are two types of CNTs such as single wall nanotube (SWNT) and multi-wall nanotube (MWNT) and used any one as a channel in CNTFET. The CNTFET structure is similar to MOSFET structure, the only channel is modified with CNTs, and the principle and operation are the same as to MOSFET. The CNTFET allows the ballistic transport between source and drain, and operate with low voltages as compare to MOSFET.

**Effect of chiral vector**

CNT structure acts as metal and semiconductor based on the chirality index \((m, n)\). Chirality indicates the atomic arrangement in the CNT tube. The CNT circumference is given regarding chirality index, \(C = na_1 + ma_2\) and it is presented in Fig. 2 as two-dimensional graphene sheets where \(a_1\) and \(a_2\) are the unit vectors, \(n\) and \(m\) are integers of the hexagonal honeycomb lattice. Based on the chirality index \((m, n)\), we can decide the weather CNT is a metallic nature or semiconducting nature. If \(n = m\) or \(n-m=3i\), where \(i\) is an integer, CNT is metallic, else semiconductor [XVII]. The geometry and chirality index decided the parameters such as diameter, unit cell, and its carbon atoms, as well as the size and shape. The diameter of the CNT can be expressed as

\[
D_{CNT} = \frac{\sqrt{3}a_0}{\pi} \sqrt{n^2 + m^2 + nm} 
\]

(1)

Where is the atomic space between each carbon atom with respect to neighbor atom. \((a_0=0.142\) nm)

The chirality angle is expressed in equation (2), and it is used to measure the direction of chirality vector.

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The threshold voltage can be expressed as

$$V_{th} = a(V_\pi)/\sqrt{3qD_{CNT}}$$

(3)

where q = electronic charge, a = 2.49 Å is the lattice constant, and V_\pi = 3.033 eV is the C-C bond energy.

CNTFETs offer a chance to control the threshold voltage by varying the chiral index, or the CNT diameter. Chirality index place a major role for determining the diameter of CNT. From the HSPCIE simulations, it has been observed that a threshold voltage of CNTFET can be controlled by changing the chirality index. We have varied the different combinations of chirality vector and analyzed in table 1. From table 1 has been observed that when chirality vector (m, n) = (4, 0), threshold voltage is 0.81 V and chirality vector (m, n) = (26, 12), threshold voltage is 0.46 V. It is evident that varying the chirality vector is effecting on threshold voltage as shown in Fig. 3.

![Graphene atomic structure with a chiral vector](image)

**Fig. 2: Graphene atomic structure with a chiral vector**

| Chiral vector (m, n) | Threshold Voltage of CNTFET |
|----------------------|-----------------------------|
| (4,0)                | 0.81                        |
| (6,2)                | 0.6                         |
| (16,12)              | 0.45                        |
| (8,0)                | 0.56                        |
| (9,1)                | 0.49                        |
| (17,9)               | 0.5                         |
| (11,0)               | 0.52                        |
| (13,2)               | 0.51                        |
| (24,13)              | 0.44                        |
| (14,0)               | 0.49                        |
| (17,3)               | 0.5                         |
| (26,12)              | 0.46                        |
In addition, we have compared the delay time of copper, SWCNT, and MWCNT interconnects with CMOS driver at different interconnect lengths as shown in Fig. 4. It has been observed that the SWCNT and MWCNT bundle interconnects offer much lower propagation delay than the copper interconnects due to the linear increase in resistance of copper interconnect line.

![Fig. 3: Threshold voltage variation with chirality for CNTFET](image)

**Fig. 3:** Threshold voltage variation with chirality for CNTFET

**Fig. 4:** Comparison of delay time at different interconnect lengths.

### III. Interconnect analysis

In practice, most of the circuits have a basic building block called CMOS inverter, where we can observe the delay and latch-up effects due to parasitic elements of CMOS which do not come in the resistive driver. Interconnects with CMOS driver is the best case to analysis the signal integrity issues occur at the intermediate stage of routing. In order to make the interconnect system more practical, we considered nonlinear CMOS driver interconnect and load system for our analysis. In this work, we have performed the simulations with resistive and CMOS driver for different interconnect lengths. The RLC interconnect driving through the CMOS, and the resistive driver has shown in Fig. 5.

![Fig. 5: RLC interconnect with (a) CMOS driver and load (b) resistive driver and load](image)

**Fig. 5:** RLC interconnect with (a) CMOS driver and load (b) resistive driver and load

In this work, we have considered the conventional copper interconnects, and carbon nanotube-based interconnects such as SWCNT and MWCNT. These interconnects are driven through the resistive, CMOS and CNTFET drivers. A two line driver interconnect load (DIL) system has been made using these interconnects and drivers to analysis the crosstalk noise, power and signal transition delays at different
interconnect lengths. All the simulations have been done using DIL system by considering the conventional copper interconnect, CNT based interconnects (SWCNT and MWCNT) with resistive, CMOS and CNTFET drivers at different interconnect lengths.

Table 2: Comparison of far end delay for different drivers and interconnects by varying the interconnect length

| Interconnect length(µm) | Cu interconnect delay(ps) | SWCNT interconnect delay(ps) | MWCNT interconnect delay(ps) |
|-------------------------|--------------------------|------------------------------|-------------------------------|
| 100                     | 475.72                   | 428.15                       | 368.21                        |
| 300                     | 589.96                   | 530.96                       | 456.63                        |
| 500                     | 710.48                   | 639.43                       | 549.91                        |
| 700                     | 824.53                   | 742.08                       | 638.19                        |
| 900                     | 942.25                   | 848.03                       | 729.30                        |
| 1100                    | 1056.35                  | 950.72                       | 817.61                        |

Table 3: Comparison of power dissipation for different drivers and interconnects by varying the interconnect length

| Interconnect length(µm) | Cu interconnect power dissipation(µW) | SWCNT interconnect power dissipation(µW) | MWCNT interconnect power dissipation(µW) |
|-------------------------|----------------------------------------|------------------------------------------|------------------------------------------|
| 100                     | 42.35                                  | 36.00                                    | 32.40                                    |
| 300                     | 55.42                                  | 47.11                                    | 42.40                                    |
| 500                     | 71.86                                  | 61.08                                    | 54.97                                    |
| 700                     | 92.34                                  | 78.49                                    | 70.64                                    |
| 900                     | 110.84                                 | 94.21                                    | 84.79                                    |
| 1100                    | 126.56                                 | 107.58                                   | 96.82                                    |

The comparison of far end delay and power dissipation for conventional copper interconnects, SWCNT and MWCNT driving through the resistive, CMOS and CNTFET drivers by varying the interconnect length from 100µm to 1100µm has been shown in Table 2 and Table 3. It is also shown the far end delay and power dissipation in Fig. 6 and Fig. 7 at interconnect length 1100µm to make a clear observation of delay and power degradation. From the simulations, it is observed that the MWCNT interconnect with CNTFET driver has given a more than 50% improvement compared to other conventional interconnects.

![Fig. 6](image-url)
Further, we have analyzed with the same interconnects and drivers to estimate the crosstalk peak voltage and crosstalk peak width by considering the two line interconnect bus architecture. The crosstalk peak voltages and widths have been noted for conventional copper, and CNT based interconnects (SWCNT and MWCNT) driving through resistive, CMOS and CNTFET by varying the interconnect length from 100µm to 1100µm and shown in Table 4 and Table 5. It is also shown the noise peak voltages and widths in Fig. 8 and Fig. 9 at interconnect length 1100µm to make the clear observation of reduction of crosstalk noise with MWCNT driving through CNTFET driver. From the simulations, it is observed that the MWCNT interconnect with CNTFET driver produced a less noise at the far end of interconnect line when the influence of coupling parasitics and has shown the more than 55% improvement compared to other conventional interconnects.

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**Table 4: Comparison of crosstalk peak voltage for different drivers and interconnects by varying the interconnect length**

| Interconnect length (µm) | Cu interconnect peak voltage (mV) | SWCNT interconnect peak voltage (mV) | MWCNT interconnect peak voltage (mV) |
|--------------------------|-----------------------------------|--------------------------------------|--------------------------------------|
|                          | Resistive driver | CMOS driver | CNT driver | Resistive driver | CMOS driver | CNT driver | Resistive driver | CMOS driver | CNT driver |
| 100                      | 251.47           | 221.29      | 188.10     | 153.40          | 138.06      | 115.97     | 134.99          | 118.79      | 106.91    |
| 300                      | 268.26           | 236.07      | 200.66     | 163.64          | 147.27      | 123.71     | 144.00          | 126.72      | 114.05    |
| 500                      | 283.19           | 249.21      | 211.83     | 172.75          | 155.47      | 130.60     | 152.02          | 133.77      | 120.40    |
| 700                      | 292.81           | 257.67      | 219.02     | 178.61          | 160.75      | 135.03     | 157.18          | 138.32      | 124.49    |
| 900                      | 305.47           | 268.81      | 240.57     | 186.34          | 176.70      | 140.87     | 163.98          | 144.30      | 129.87    |
| 1100                     | 321.62           | 283.03      | 240.57     | 196.19          | 176.57      | 148.32     | 172.65          | 151.93      | 136.74    |

**Table 5: Comparison of crosstalk peak width for different drivers and interconnects by varying the interconnect length**

| Interconnect length (µm) | Cu interconnect peak width (ps) | SWCNT interconnect peak width (ps) | MWCNT interconnect peak width (ps) |
|--------------------------|---------------------------------|-----------------------------------|-----------------------------------|
|                          | Resistive driver | CMOS driver | CNT driver | Resistive driver | CMOS driver | CNT driver | Resistive driver | CMOS driver | CNT driver |
| 100                      | 195.52            | 164.24     | 147.81     | 125.13          | 110.12      | 98.00      | 113.87          | 96.79       | 87.11     |
| 300                      | 212.74            | 178.70     | 160.83     | 136.15          | 119.82      | 106.64     | 123.90          | 105.31      | 94.78     |
| 500                      | 228.95            | 192.32     | 173.09     | 146.53          | 128.94      | 114.76     | 133.34          | 113.34      | 102.01    |
| 700                      | 244.51            | 205.39     | 184.85     | 156.49          | 137.71      | 122.56     | 142.40          | 121.04      | 108.94    |
| 900                      | 258.17            | 216.86     | 195.18     | 165.23          | 145.40      | 129.41     | 150.36          | 127.80      | 115.02    |
| 1100                     | 270.36            | 227.10     | 204.39     | 173.03          | 152.27      | 135.52     | 157.46          | 133.84      | 120.46    |
In this sub section, the influence of interconnect parasitic elements such as coupling capacitance($C_{12}$), inductance($L_{12}$) and load capacitance($C_L$) on noise voltage at output end has been discussed. To evaluate the crosstalk noise voltage behavior, an increasing step signal is applied to interconnect line 1, and logic 1 ($V_{DD}$) signal is applied to interconnect line 2. Due to the parasitic coupling effect of one interconnect line on other interconnect line, an unwanted noise voltages are obtaining at output end as shown in Fig. 10 and Fig. 11. In addition, we have reduced the noise voltages by increasing load capacitance and decreasing coupling parasitic elements. The deviation in noise voltages at output end with a variation of load capacitance, coupling inductance, and capacitance is simulated with HSPICE and tabulated in Table 6 and Table 7.
Fig. 11 Noise voltages at the output end of interconnect line with a variation of load capacitance.

Table 6: Noise voltage variations with respect to the load capacitance

| Load capacitance $C_L$ (fF) | Noise peak voltage (V) |
|------------------------------|------------------------|
| 5                            | 0.149                  |
| 10                           | 0.124                  |
| 15                           | 0.11                   |
| 20                           | 0.080                  |
| 25                           | 0.065                  |

Table 7: Noise voltage variations at output end with a variation of coupling capacitance and inductance

| Different Cases | Coupling Capacitance (pF) | Coupling Inductance (µH) | Noise voltage (V) |
|-----------------|----------------------------|--------------------------|-------------------|
| Case1           | 30.8                       | 2.477                    | 0.149             |
| Case2           | 20.8                       | 1.477                    | 0.121             |
| Case3           | 10.8                       | 0.477                    | 0.072             |
| Case4           | 1.8                        | 0.177                    | 0.035             |

IV. Conclusion

The impact of driver and interconnect materials on power dissipation and delay in interconnects is analyzed, the tabular and graphical observations are reported. The CNTFET driver with MWCNT interconnect has given a better performance than conventional copper interconnects and drivers. MWCNTs have offered a more than 50% of lesser delay and crosstalk than conventional ones. Further, we have performed the crosstalk analysis by varying the interconnect length, coupling and load capacitances and eliminated the crosstalk effect by increasing load capacitor and decreasing coupling parasitics. Finally, it is evident that CNT interconnects and CNTFET drivers provide better performance than that of conventional copper interconnects in terms of power consumption, crosstalk, and signal transition delays.
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