HEAAN Demystified: Accelerating Fully Homomorphic Encryption Through Architecture-centric Analysis and Optimization

Wonkyung Jung∗, Eojin Lee∗, Sangpyo Kim∗, Keewoo Lee∗, Namhoon Kim∗, Chohong Min†, Jung Hee Cheon∗, and Jung Ho Ahn∗
*Seoul National University, † Ewha Woman’s University
gajh@snu.ac.kr

Abstract—Homomorphic Encryption (HE) draws a significant attention as a privacy-preserving way for cloud computing because it allows computation on encrypted messages called ciphertexts. Among numerous HE schemes proposed, HE for Arithmetic of Approximate Numbers (HEAAN) is rapidly gaining popularity across a wide range of applications (e.g., machine learning) because it supports messages that can tolerate approximate computation with no limit on the number of arithmetic operations applicable to the corresponding ciphertexts.

A critical shortcoming of HE is the high computation complexity of ciphertext arithmetic; especially, HE multiplication (HE Mul) is more than 10,000 times slower than the corresponding multiplication between unencrypted messages. This leads to a large body of HE acceleration studies, including ones exploiting FPGAs; however, those did not conduct a rigorous analysis of computational complexity and data access patterns of HE Mul. Moreover, the proposals mostly focused on designs with small parameter sizes, making it difficult to accurately estimate the performance of the HE accelerators in conducting a series of complex arithmetic operations.

In this paper, we first describe how HE Mul of HEAAN is performed in a manner friendly to computer architects. Then we conduct a disciplined analysis on its computational and memory-access characteristics, through which we (1) extract parallelism in the key functions composing HE Mul and (2) demonstrate how to effectively map the parallelism to the popular parallel processing platforms, multicore CPUs and GPUs, by applying a series of optimization techniques such as transposing matrices and pinning data to threads. This leads to the performance improvement of HE Mul on a CPU and a GPU by 42.9× and 134.1×, respectively, over the single-thread reference HEAAN running on a CPU. The conducted analysis and optimization would set a new foundation for future HE acceleration research.

I. INTRODUCTION

As cloud computing becomes an increasingly dominant way of providing computing resources, numerous computations are performed on datacenter servers rather than on personal devices [5], [35]. It enables the client without expensive hardware to receive services that require complex computations. However, security and privacy issues are also emerging with the growth of cloud computing [23], [51]. When a client sends private data to a server, security issues in data transfers can be resolved by sending the data after encryption. However, the data encoded by a conventional encryption method must be decrypted to perform the computation in the server. Therefore, a user have no choice but to use the cloud service with a risk of security or privacy attack (e.g., abusing) that occurs during the computation of unencrypted data.

Homomorphic Encryption (HE) [48], an encryption scheme that enables computation between encrypted data, draws significant attention as a solution to this privacy problem. By adopting HE, service providers no longer need to decrypt the clients’ private data for computation. The concept of HE was first suggested in 1978 [48]. However, the early proposals of HE were either unsafe [48] or support only one type of HE operation, namely HE addition (HE Add) or HE multiplication (HE Mul) (e.g., ElGamal [29] and Paillier [46]). In this aspect, it was difficult to put HE into serious applications for a while. However, fully HE (FHE) [31] proposed in 2009 made a major breakthrough by supporting both HE Add and HE Mul. Moreover, FHE supports bootstrapping, a method of initializing noise in encrypted data, enabling an unbounded number of HE Add and Mul without decryption.

Among numerous FHE schemes to date [12], [17], [18], [28], [30], [40], HE for Arithmetic of Approximate Numbers (HEAAN [17]), also known as CKKS (Cheon-Kim-Kim-Song) is rapidly gaining popularity [36] as it supports the approximate computation of real numbers. HEAAN enables HE Add and Mul of approximate data, where the result is almost the same as that of the original operation with a tiny error. Using HEAAN, computations can be performed without data decryption in the datacenter. However, the execution time for computation on encrypted data (ciphertext) increases by from 100s to 10,000s of times compared to that on native, unencrypted messages. Therefore, it is highly desired to reduce the computation time of HE operations to use HE practically.

There have been a large body of research on accelerating HE operations using FPGAs or GPUs. However, FPGA-based acceleration studies targeted the HE schemes (e.g., BGV [12], LTV [40], and BFV [30]) that only support computations of integer numbers [21], [25], [45], [49], [50], or operate with only limited parameter sizes [47]. They all target performing a small number of HE Mul without bootstrapping, inhibiting their applicability to a wide range of applications requiring hundreds to thousands of multiplication be performed (e.g., deep learning). GPU implementation studies [4], [7], [8], [22] do not take advantage of the algorithm’s internal parallelism sufficiently, operate on only small or limited parameters, or do not consider the cost of modulo operations.

In this paper, we demystify HEAAN, a representative FHE scheme, by describing, analyzing, and optimizing it in a manner friendly to computer architects. We first explain the
pertinent details of HEAAN, and identify that the following four functions take more than 95% of HE Mul, the most computationally expensive operation of HE: CRT (Chinese Remainder Theorem), NTT (Number Theoretic Transform), iNTT (inverse NTT), and iCRT (inverse CRT), we conduct an in-depth and disciplined analysis of the aforementioned primary functions to understand their computational complexity and access patterns on input, output, and precomputed data, which are critical for operation (e.g., modular multiplication) strength reduction, across a range of key HE parameters.

The parallelism exposed through the analysis is exploited to accelerate HE Mul on CPU and GPU, the most popular computing platforms, which are already equipped with hundreds to thousands of ALUs. In CPU, we utilize multiple cores (intercore parallelism) and AVX-512 instructions supported by the latest Intel architectures (intra-core parallelism). In GPU, we utilize massive thread-level parallelism expressible through the CUDA programming model. We further improve performance by proposing a series of architecture-centric optimizations, such as matrix transposition to better exploit memory access locality, loop reordering to expose more parallelism, and taking a synergy between precomputation and delayed modulo operations; and we estimate how much more performance gains are attainable through natively support currently emulated instructions. We achieve 42.9× and 134.1× speedup of HE Mul on CPU and GPU, respectively, compared to the single-thread reference HEAAN [1], setting a new baseline for the future HE acceleration research.

II. BACKGROUND: COMPUTATIONAL CHALLENGES OF HOMOMORPHIC ENCRYPTION (HE)

HE can be categorized into two groups, somewhat HE (SHE) and fully HE (FHE), by whether there is a limitation on the number of arithmetic operations applicable to the ciphertext. In a HE scheme, noise is accumulated during each operation; this makes the ciphertext of a SHE scheme decipherable after performing a certain number of operations. On the contrary, FHE schemes support a bootstrapping algorithm [16], which refreshes the accumulated noise. Therefore, although there is an upper bound in the number of arithmetic operations that can be consecutively applied to a ciphertext, by periodically bootstrapping it, we can continue manipulating the ciphertext with no need for decrypting it. This property makes FHE well-tailored to meet the demands of a wide range of general applications (e.g., training/inference of deep neural networks [6], [11], [19], [27]), which require a massive number of operations applied to encrypted data.

Representative FHE schemes include Brakerski-Gentry-Vaikuntanathan (BGV) [12], Lopez-Alt, Tromer, and Vaikuntanathan (LTV) [40], Brakerski/Fan-Vercauteren (BFV) [30], fast FHE over the torus (TFHE) [18], and Cheon-Kim-Kim-Song (CKKS) [17]. Among these, only CKKS supports approximate computation on real numbers, and hence it is a top candidate for many real-world applications requiring a bunch of operations on data that can tolerate tiny errors due to approximate computation. CKKS is rapidly gaining popularity in a wide range of applications exploiting HE, such as machine learning [39]. For example, the winner and the most runner-ups of a recent HE challenge about secure genome analysis competition (iDASH 2018 [36] and 2019 [37]) used CKKS or its hybrid versions. Therefore, we investigate HEAAN (HE for Arithmetic of Approximate Numbers) scheme [1], which is developed by the authors of CKKS.

HEAAN is able to perform arbitrary computation types by combining HE multiplication (simply HE Mul) and HE addition (simply HE Add), which are multiplication and addition on ciphertexts. However, the execution time of HE operations increases significantly compared to the corresponding ones on the original unencrypted messages. Table I compares the execution time for addition/multiplication of original messages and ciphertexts using a single core from the system specified in Section VI. We measure the average execution time of addition/multiplication of a complex number in a message consisting of 32,768 complex numbers. HE Mul (Add) is 36,112× (168×) slower than native message operation. When the message consists of fewer numbers, the slowdown is even higher. Considering that most approximate number operations consist of multiplication and addition, the long execution time of HE operations is an obstacle to the practical use of HE. Therefore, it is essential to accelerate HE operations, especially HE Mul as it is 448× slower than HE Add.

III. A BRIEF INTRODUCTION TO HEAAN

Prior to accelerating the most compute-intensive HEAAN operation, HE Mul, we introduce the pertinent details of HEAAN, focusing on how to convert an input message to a ciphertext through encoding/encryption steps and how to perform arithmetic operations on ciphertext in HEAAN.

A. HEAAN encryption

HEAAN converts an input message to a ciphertext through encoding and encryption steps. An input message consists of \( n \) complex numbers, each composed of a double-type real and imaginary number. The encoding step first converts an input message to a plaintext (\( \mathbf{t} \), a polynomial of at most degree \( N-1 \) with \( N \) integer coefficients. \( \mathbf{t} \) is placed in a cyclotomic polynomial ring \( R = \mathbb{Z}[X]/(X^N + 1) = c_0X^0 + c_1X^1 + \ldots + c_{(N-1)}X^{(N-1)} \) space with the magnitude of each coefficient bounded by ciphertext modulus, integer \( q \) \((\mathbf{t} \in R/qR)\). Therefore, each coefficient \( c_k \) is the residue number by \( q \), where \( q \) is a BigInt (big integer) much larger than \( 2^{64} \). The encoding step converts the floating-point numbers of an message to integer numbers after multiplying with a scaling

| Operation type | Message | Ciphertext | Slowdown |
|----------------|---------|------------|----------|
| Addition       | 2.1 ns  | 348.2 ns   | 168.2×   |
| Multiplication | 4.3 ns  | 155883.8 ns| 36112.7× |
TABLE II: Multiplicative depth ($L$) and required $N$ over $\log Q$ to guarantee 80-bit security level (an attacker needs $2^{80}$ × of modular mul & add to break with the current best algorithm.)

| $\log Q$ | Multiplicative depth ($L$) | required $N$ |
|----------|-----------------------------|-------------|
| 300      | 10                          | $2^{14}$    |
| 600      | 20                          | $2^{15}$    |
| 1,200    | 40                          | $2^{16}$    |
| 2,400    | 80                          | $2^{17}$    |

factor ($\Delta$) and then rounding down the remaining fraction numbers. Each coefficient is a $\log_q$-bit BigInt, and $n \leq \frac{N}{q}$. Then, the encryption step converts a plaintext to a ciphertext consisting of a pair of polynomials $c.ax$ and $c.bx$ using a public key pair ($pk_0$ and $pk_1$) as follows:

\[
\begin{align*}
    c.ax &= u \times pk_1 + e_1 \\
    c.bx &= u \times pk_0 + e_0 + t
\end{align*}
\]

The public key pair is generated from a secret key ($sk$).

In the equations above, $u$ is a polynomial of at most degree $(N-1)$, where each coefficient is either -1, 0, or 1 following a distribution described in [17]. $e_0$ and $e_1$ are also polynomials of at most degree ($N-1$) polynomials with random error values to ensure security, which follow a Gaussian distribution with a small standard deviation value (e.g., $\sigma = 3.2$ in [17]).

To extract the original message from a ciphertext, we first convert the ciphertext to the plaintext exploiting the following relationship between $c.ax$ and $c.bx$:

\[
\begin{align*}
    c.bx &= c.ax \times sk + t + e' \\
    c.ax &= u \times pk_1 + e_1 \\
    c.bx &= u \times pk_0 + e_0 + t
\end{align*}
\]

Then, the plaintext $t$ can be returned to the original message through decoding; in this case, the inverse of scaling factor $(1/\Delta)$ is multiplied to get the approximate values.

HEAAN limits the maximum size of the ciphertext modulus $q$ to a constant value $Q$. HEAAN chooses $p^L$ for $Q$, where $L$ is multiplicative depth, the number of consecutive HE Mul operations applicable to a ciphertext before it loses encrypted data, and $p$ is rescaling factor. The size of the message contained in a ciphertext increases exponentially as the ciphertext is multiplied repeatedly. To prevent the explosion of message size, HEAAN performs rescaling after each HE Mul by dividing the coefficients of the output ciphertext by $p$. Then the size of $q$, the ciphertext modulus, is adjusted to $q'$ where $\log q' = \log q - \log p$. Therefore, $\log q$ of a ciphertext that is just encrypted starts at $\log Q$, decreases by $\log p$ every time an HE Mul is applied, and becomes 0 after experiencing $L$ HE Mul operations, losing data. When $p$ is fixed, more HE Mul can be applied to a ciphertext with a larger $Q$ value.

To apply more HE Mul operations to a ciphertext, FHE reinitialize the ciphertext through bootstrapping. However, bootstrapping is a costly operation (reported to take in the order of minutes [14]) because it consists of dozens of HE Mul and shift operations. To reduce the overhead of bootstrapping for practical use of HE, we should use large $Q$ values to increase $L$. Also, $N$ should increase as $Q$ increases to guarantee a certain level of security in HE (see Table II). As larger $Q$ and $N$ values require more computation and data storage costs per HE Mul, it is not efficient to use too large $Q$; we discuss a further detail of this trade off in Section VIII. In this paper, we use ($p$, $L$, $Q$, $N$) of (2$^{30}$, 40, 2$^{2000}$, 2$^{16}$), respectively, which are the default values the official HEAAN repository [1] uses.

B. HEAAN computation

Arithmetic operations in HEAAN, HE Add and Mul, are through computation between the polynomials of operand ciphertexts. Here we assume that the two operand ciphertexts in HE operation have the same ciphertext modulus value $q$.

HE Add computes an output ciphertext ($c3$) from two input ciphertexts ($c1$ and $c2$) through the following operations:

\[
\begin{align*}
    c3.ax &= \text{mod}(c1.ax + c2.ax, q) \\
    c3.bx &= \text{mod}(c1.bx + c2.bx, q)
\end{align*}
\]

HE Add is relatively simple because it performs the element-wise addition of BigInt coefficients and then the modulo of $q$ for each output coefficient; mod($x$, $y$) means $x$ modulo $y$. Here the modulo operation is implemented simply by subtracting $q$ when each output coefficient is larger than $q$ because the result of each addition is smaller than $2q$.

HE Mul is much more costly than HE Add because the former requires multiplying BigInt coefficients by $N^2$ times. In this paper, we assume that $\beta$ is the size of an integer data type that a computer natively supports with high performance (e.g., $\beta = 2^{64}$ for 64-bit CPUs), which is often called a word size. A $\log_q$-bit BigInt is represented as $qLimbs$ ($\leq \log q/\log \beta$) words (see Figure 1). Then, one BigInt multiplication (simply mul) consists of ($qLimbs$) $^2$ $\log \beta$-bit word mul and $2(qLimbs)^2$–1 word addition (simply add) operations. For example, because $qLimbs$ is 19 when using the representative parameters ($N = 2^{16}$, $\log q = 1,200$, $\log \beta = 64$) summarized in Table III, 361 64-bit mul and 721 64-bit add operations are required besides carry propagation per BigInt mul. As described above, polynomial mul requires $N^2$ (=4.3 billion) BigInt mul, which requires at least 4.6 Tera 64-bit operations. To reduce the complexity of this polynomial mul, HEAAN and other HE schemes use Chinese Remainder Theorem (CRT [24]) and Number Theoretic Transform (NTT [20]).

C. CRT for reducing the complexity of BigInt mul: CRT states that for $np$ integers $\{m_i | 0 \leq i < np \}$ which are coprime with each other, the residue set $\{x_i = \text{mod}(X, m_i) | 0 \leq i < np \}$ of any integer $0 < X < \prod_{i=0}^{np-1} m_i$ is unique. HEAAN exploits CRT by defining a set of $np$ integers $\{p_0, p_1, ..., p_{np-1}\}$, where each modulus $p_i$ is a prime number smaller than $\beta$ and $\prod_{i=0}^{np-1} p_i = P > q^2$. Then, a $\log q$-bit BigInt number $B$,
TABLE III: Representative parameters in Homomorphic Encryption (HE)

| Symbol | Description                                                                 | Representative values |
|--------|-----------------------------------------------------------------------------|-----------------------|
| ∆      | Scaling factor is multiplied to the floating-point number of message to convert to integer number. | log Δ = 30            |
| p      | Rescaling factor linearly reduces the size of messages that grow exponentially during computation. | log p = 30            |
| L      | Multiplicative depth is the maximum number of possible mul of a ciphertext without bootstrapping. | 40                    |
| Q      | The maximum ciphertext modulus is equal to the initial ciphertext modulus after encryption. | log Q = 1,200         |
| q      | Ciphertext modulus starts from Q and divided by a rescaling factor p at each mul.      | log q = 1,200, 1,170, ..., 0 |
| N      | The number of coefficients of ciphertext polynomial. The degree of ciphertext polynomial is at most N-1. | 216 = 65,536          |
| n      | The number of messages. n messages are encrypted in one ciphertext.            | 32, 64, ..., 32,768   |
| β      | Word size. It is machine-dependent (264 for CPU, 232 for GPU).                  | 264 or 232            |
| qLimbs | The number of limbs of q. To represent log q-bit integer, qLimbs limbs are required. | [1,200/64] = 19       |
| np     | The number of prime numbers. We use np prime numbers to represent big integer in RNS domain. | [2,400/58] = 42       |
| P      | Product of prime numbers that are used to represent big integer.               | P = \(\prod_j p_j\)   |
| PLimbs | The number of limbs of P. To represent log(P/pj)-bit integer, PLimbs limbs are used. | max(log(P/pj)/ log β) |

which is the coefficient of the ciphertext polynomial, can be represented in the residue number system (RNS) by the set of remainders \(\{b_0, b_1, ..., b_{n-1}\}\) where \(b_i = \text{mod}(B, p_i)\).

A key property of RNS is that for adding, subtracting, and multiplying numbers represented in RNS, it is sufficient to perform the same modular operation on each pair of numbers (called a congruence relation). That is, for a pair of log\(_q\)-bit BigInt numbers \((A, B)\) and their corresponding RNS representations \(\{a_i|0 \leq i < np\}, \{b_i|0 \leq i < np\}\), the product of \(A\) and \(B\) is \(C\) represented by \(\{c_i|0 \leq i < np\}\) such that \(c_i = \text{mod}(a_i \cdot b_i, p_i)\). This relationship holds because we set \(P\) not smaller than \(q^2\) and the product of two log\(_q\)-bit BigInt numbers are smaller than \(q^2\).

Therefore, a log\(_q\)-bit BigInt number is converted into np log\(_β\)-bit data (see Figure 1) in an RNS domain, where we call the conversion a CRT function or simply CRT, and a BigInt mul is changed into np log\(_q\)-bit modular mul; and hence, the time complexity per BigInt mul is changed from \(O(q\text{Limbs}^2)\) to \(O(np)\). In general, \(q\text{Limbs}^2 \gg np\) (see Table III), so the number of operations required for BigInt mul can be greatly reduced by CRT. However, multiplying two BigInt polynomials still has a complexity of \(O(np \cdot N^2)\) because polynomial mul requires \(N^2\) coefficient mul operations.

**NTT for reducing the complexity of polynomial mul:** NTT is a discrete Fourier transform over a finite field (integer). It is well known that fast polynomial mul can be implemented by using Fast Fourier Transform (FFT) [10]. Therefore, we can translate polynomial mul with \(O(N^2)\) complexity into element-wise mul with \(O(N)\) complexity by using fast NTT, a variant of FFT limited to integer values. Although fast NTT (or simply NTT) requires transformation cost with \(O(N \log N)\) complexity, it is beneficial to use NTT when \(N\) is large enough.

The overall flow of HE Mul in HEAAN, including CRT and NTT, is depicted in Figure 2. It consists of 5 polynomial mul, where each polynomial mul performs (1) CRT, (2) NTT, and (3) element-wise modular mul, followed by (4) inverse fast NTT (\(\text{INTT}\)) and (5) RNS-to-BigInt conversion (\(\text{ICRT}\)) to return to the polynomial with BigInt coefficients. We divide the whole process into region 1 and region 2; the former multiplies and adds input ciphertexts whereas the latter transforms \(c_1.ax \times c_2.ax\), which is a region 1’s byproduct that is decrypted with \(sk^2\), into a form that is decrypted with \(sk\) (called key-switching). The evaluation key (\(evk\)) used in region 2 consists of two polynomials (\(evk.ax\) and \(evk.bx\)) where each coefficient is \(log Q^2\)-bit (= 2\(\times log Q\)-bit) long, encrypting the square of \(sk\) multiplied by a constant \(Q\). The key-switching procedure with \(evk\) is mandatory to decrypt correctly, as it removes the need for \(sk^n\) in decryption stage, which, without the key-switching, would be required after \(n\) sequential multiplications.

In region 1, \(np\) is configured to deal with \(log q^2\)-bit BigInt, the intermediate result of polynomial mul between two input ciphertexts whose coefficient size is \(log q\)-bit. By contrast, in region 2, \(np\) is set larger to represent \((log q^2 + log Q^2)\)-bit BigInt because the coefficient size of \(evk\) is \(log Q^2\)-bit long. The shift operations in region 2 reduce the amount of error that was accumulated during mul. The following additions and subtractions between the results of polynomial mul produce the result of HE Mul (\(c_3.ax\) and \(c_3.bx\)); we can get an approximate value of mul between two original messages by decrypting the result using \(sk\).

Figure 3 shows the execution time breakdown of HE Mul.
Fig. 3: HE Mul execution time breakdown (total 5,108 ms).

Algorithm 1 CRT

Input: \( \text{IN}_{\text{CRT}}(N,q\text{Limbs}), \text{TB}_{\text{CRT}}(np,q\text{Limbs}) \)

Output: \( \text{OUT}_{\text{CRT}}(N,np) \)

1: for \((i = 0; i < N; i = i + 1)\) do
2: \(\text{for } (j = 0; j < np; j = j + 1)\) do
3: \(\text{accum} \leftarrow 0\)
4: \(\text{for } (k = 0; k < q\text{Limbs}; k = k + 1)\) do
5: \(\text{accum} += \text{IN}_{\text{CRT}}[i][k] \times \text{TB}_{\text{CRT}}[j][k]\)
6: \(\text{OUT}_{\text{CRT}}[i][j] = \text{mod}(\text{accum},p_j)\)

using a single-threaded reference HEAAN in the system and configuration described in Section VI. CRT, NTT, iNTT, and iCRT account for 95.8% of the total execution time. The remaining operations, such as element-wise modular mul, account for only 4.2% of execution time. The total execution time is 5,108 ms, which is about 36,000x slower than the original message mul, as discussed in Section II. Therefore, accelerating HE Mul is essential for practical use of HE, and it is necessary to accelerate CRT, NTT, iNTT, and iCRT.

IV. AN IN-DEPTH ANALYSIS OF MAJOR FUNCTIONS IN HEAAN MULTIPLICATION

To accelerate the primary functions (CRT, NTT, iNTT, and iCRT) in HE Mul, we first conduct an in-depth analysis of how each function works. In the following descriptions, \(\text{IN}/\text{OUT}_{\text{function}}(X,Y)\) represents an \(X\) by \(Y\) matrix used as input/output of a function, while \(\text{TB}_{\text{function}}(X,Y)\) represents a precomputed table of \(X\) by \(Y\) matrix.

\(\text{CRT}\) (Algo. 1) takes \(\text{IN}_{\text{CRT}}(N,q\text{Limbs})\) representing \(N\) log \(g\)-bit BigInt numbers and produces \(\text{OUT}_{\text{CRT}}(N,np)\), the result of modulo operation on each BigInt with \(np\) different primes \(\{p_j\}_{0 \leq j < np}\). The operation consists of two stages: (1) computing matrix-matrix mul of \(\text{IN}_{\text{CRT}}\) with \(\text{TB}_{\text{CRT}}\) (7) and (2) applying modulo operations to each output element.

We first explain how to perform a modulo operation on a BigInt with a modulus smaller than \(\beta\). A BigInt \(A\) is expressed by \(q\text{Limbs}\) \(\log\beta\)-bit words, i.e. \(\sum_{k=0}^{q\text{Limbs}-1} a_k \cdot \beta^k\) where \(\{a_k\}_{0 \leq k < q\text{Limbs}}\). Then the modulo operation on the BigInt is as follows:

\[
\text{mod}(A,p_j) = \text{mod}(\sum_{k=0}^{q\text{Limbs}-1} a_k \cdot \beta^k, p_j) = \text{mod}(\sum_{k=0}^{q\text{Limbs}-1} a_k \cdot \text{mod}(\beta^k, p_j), p_j)
\]

Here because \(\beta\) and \(p_j\) are independent of the input, HEAAN precomputes \(\text{TB}_{\text{CRT}} = \text{mod}(\beta^k, p_j)\) for all \(k\) and \(j\). Therefore, \(\sum_{k=0}^{q\text{Limbs}-1} a_k \cdot \text{mod}(\beta^k, p_j)\) is performed by multiplying \(\text{IN}_{\text{CRT}}\) and \(\text{TB}_{\text{CRT}}\).

We can exploit Shoup’s modular mul (Shoup’s ModMul [50]) for the modulo operation in line 6 of Algo. 1. Shoup’s ModMul (Algo. 2) computes \(\text{mod}(X \cdot Y, p_j)\) with 3 muls and a single correction step if a value \(Y_{\text{Shoup}} = \frac{Y \cdot \beta}{p_j}\) is known in advance. It replaces a costly division operation with relatively cheaper mul, comparison, and subtraction operations. We apply the algorithm for the modular mul on \(\text{accum}\) spanning up to 3 limbs (\(\text{accum}_0 + \text{accum}_1 \cdot \beta + \text{accum}_2 \cdot \beta^2\)), using precomputed \(Y_{\text{Shoup}}\) values on \(Y = \{1, \beta, \beta^2\}\). The operations of \(\text{CRT}\) can be performed in parallel for each coefficient (total \(N\)) and each prime number (total \(np\)).

\(\text{NTT}\) implements Cooley-Tukey algorithm [20], which recursively divides an \(N\)-point FFT to \(k\) \(N/k\)-point FFTs and combines their results (called \(\text{radix-k}\) FFT). An exemplar radix-2 \(\text{NTT}\) in Algo. 3 takes a matrix \(\text{IN}_{\text{NTT}}(np,N)\) as an input and performs a butterfly algorithm \(\text{butt}\). It uses a precomputed table \(\text{TB}_{\text{W}}\) of powers of the \(2\)-\(N\)-th root of unity for all \(np\) prime numbers. For each prime, \(\text{butt}\) (Algo. 4) is called \(\log N \cdot N/2\) times. As \(\text{butt}\) requires modular mul, it also uses Shoup’s ModMul as was done in \(\text{CRT}\).

\(\text{iNTT}\) is slightly different from \(\text{NTT}\). It has a different loop order, calls inverse butterfly (\(i\text{butt}\)) instead of \(\text{butt}\), deals with a different precomputed table (consisting of the inverse powers of the primitive root of unity \(\text{TB}_{\text{invW}}\)), and finally divides each element by \(N\). However, except for the last element-wise division by \(N\), \(\text{iNTT}\) is symmetric to \(\text{NTT}\) in terms of the number and the kind of operations. Both \(\text{NTT}\) and \(\text{iNTT}\) are completely parallelizable for each prime number.

\(\text{iCRT}\) converts the matrix \(\text{OUT}_{\text{iNTT}}(np,N)\), where each element is a remainder smaller than \(\beta\), back to \(N\) log \(g\)-bit BigInts (see Algo. 5). It starts with (1) the Hadamard
TABLE IV: The number of arithmetic operations and computational complexity of major functions of HE Mul.

| CRT       | NTT & iNTT | iCRT       |
|-----------|-----------|------------|
| Multiplication | N × qLims × np | -          | N × np × PLimbs |
| Modular mul  | N × np    | np × N/2 × log N | np × (N/2 × log N + N) |
| ADC (add with carry) | N × qLims × np | -          | 2 × N × np |
| Add, Sub    | -         | np × N × log N | N × np × PLimbs |

\[
\text{Computation complexity } O(N \times qLims \times np) \quad O(N \times \log N \times np) \quad O(N \times \log N \times np) \quad O(N \times np \times PLimbs)
\]

Algorithm 5 iCRT

Input: \( \text{IN}_{\text{iCRT}}(np, N) \leftarrow \text{OUT}_{\text{INNTT}}(np, N) \)

\[ \text{TB}_{\text{invP}}(np), \text{TB}_{\text{PdivP}}(np, P\text{Limbs}) \]

Output: \( \text{OUT}_{\text{iCRT}}(N, np) \)

1: for \( (i = 0; i < N; i \leftarrow i + 1) \) do
2: for \( (j = 0; j < np; j \leftarrow j + 1) \) do
3: \[ \text{temp} = \text{mod}(\text{IN}_{\text{iCRT}}[j][i] \times \text{TB}_{\text{invP}}[j], p_j) \]
4: for \( (i = 0; i < N; i \leftarrow i + 1) \) do
5: \[ \text{accum} = 0 \]
6: for \( (j = 0; j < np; j \leftarrow j + 1) \) do
7: for \( (k = 0; k < P\text{Limbs}; k \leftarrow k + 1) \) do
8: \[ \text{accum} + = \text{temp}[j][i] \times \text{TB}_{\text{PdivP}}[j][k] \times \beta^k \]
9: \[ \text{OUT}_{\text{iCRT}}[i] = \text{mod}(\text{mod}(\text{accum}, P), q) \]

Algorithm 6 iCRT algorithm in the matrix-matrix mul form.
The first three lines are the same as Algo. 5.

4: for \( (i = 0; i < N; i \leftarrow i + 1) \) do
5: \[ \text{accum} = 0 \]
6: for \( (k = 0; k < P\text{Limbs}; k \leftarrow k + 1) \) do
7: \[ \text{accum}_{\text{small}} = 0 \]
8: for \( (j = 0; j < np; j \leftarrow j + 1) \) do
9: \[ \text{accum}_{\text{small}} + = \text{temp}[j][i] \times \text{TB}_{\text{PdivP}}[j][k] \]
10: \[ \text{accum} = \text{accum} + \text{accum}_{\text{small}} \times \beta^k \]
11: \[ \text{OUT}_{\text{iCRT}}[i] = \text{mod}(\text{mod}(\text{accum}, P), q) \]

All the major functions (CRT, iCRT, NTT, and iNTT) of HE Mul of HEAAN have massive parallelism that can be exploited by CPUs and GPUs. All the residual numbers \( (N \times np) \) can be computed in parallel on CRT, NTT and iNTT perform \( np \) independent transformations and leverage the algorithmic optimization of FFT, where \( N/k \) groups can be computed in parallel at each individual stage during FFT. Henceforth, we identify key challenges and solutions we devise in accelerating HE Mul on CPUs and GPUs.

A. Loop reordering to expose massive parallelism in iCRT

iCRT recombines the residual numbers into the integers of size \( \log q \) for each coefficient of the resulting ciphertext and hence it might be regarded that the degree of parallelism is smaller than CRT \( (N \text{ vs. } Nnp) \). However, we discover that the limited \( N \)-degree parallelism can be expanded to \( N \cdot P\text{Limbs} \)-degree parallelism by reordering two loops in iCRT (line 6 and 7 in Algo. 5); the modified algorithm is shown in Algo. 6. After reordering, the sequence of original mul between a scalar and a BigInt now becomes a matrix-matrix mul between a temp matrix and a \( \text{TB}_{\text{PdivP}} \) matrix (line 9 in Algo. 6). Then, iCRT should be modified such that the partial sum in the inner-most loop is accumulated into \( \text{accum}_{\text{small}} \) (double or triple words), rather than \( \text{accum} \) (BigInt), which is aggregated to \( \text{accum} \) at the end of the loop.

The range of modulus and \( np \) determine whether \( \text{accum}_{\text{small}} \) should be a double word or a triple word; with our representative parameters where \( \beta = 2^{64} \), using a double word is sufficient. With our loop reordering, the resulting matrix-matrix mul exposes a massive parallelism of degree \( N \cdot P\text{Limbs} \) in iCRT, providing abundant parallelization opportunities to contemporary hardware platforms.

B. Accelerating HE Mul on CPUs

The strategies a modern CPU takes to exploit parallelism from an application are twofold: populating (1) multiple cores...
and (2) ALUs supporting short-SIMD instructions within each core. For example, the Skylake-based Intel Xeon CPU we use has 24 cores per socket and each core support AVX-512 instructions, each executing eight 64-bit integer operations [26], which could lead to over 100× performance improvement compared to the baseline implementation not exploiting these parallelism. To achieve a near-maximum performance CPU provides, we exploit intra-core parallelism via utilizing AVX-512 instructions and inter-core parallelism via multi-threading. We carefully distribute operations to multiple threads and AVX-512 SIMD lanes per thread to minimize performance degradation by an inferior cache performance caused by poor data access patterns; in this, whether an input matrix follows a column- or a row-major order can vastly affect performance.

During CRT, a CPU thread takes responsibility of a portion of the $N$ coefficients (line 1 in Algo. 1), whereas each lane of an AVX-512 port performs operations on different prime numbers (line 2 in Algo. 1). During NTT and iNTT, a thread does its job on a portion of the prime numbers, (line 1 in Algo. 3), whereas each lane of AVX-512 computes a part of the coefficients (line 8 in Algo. 3). In case of iCRT, we take different approaches for the two iteration phases. During the first phase (line 1 to 3 in Algo. 5), each thread and a AVX-512 lane performs computation on a part of the $N$ coefficients. During the second iteration phase (line 4 to 11 in Algo. 6) each thread also computes on a part of the coefficients (line 4), but each lane of an AVX-512 port is on different $k$, the positional index on the limbs of $r/j_p$ (line 6).

Although the reference HEAAN library [1] supports multi-threading and exploits the same parallelism type on NTT, iNTT, and iCRT with our work, (in terms of distributing works to threads; the reference HEAAN does not implements SIMD instructions) CRT takes a different strategy.

Emulating arithmetic operations: However, AVX-512 does not support parallel 64-bit mul and 64-bit ADC (addition with carry) yet. Therefore, 64-bit mul is emulated with four parallel 32-bit mul, five 64-bit add, and five 64-bit shift instructions. Also, one 64-bit compare and one additional 64-bit add are required to handle carry per addition. This emulation narrows the performance gap between the reference HEAAN and the AVX-512 implementation. To further improve performance under this constraint, we modify Shoup’s ModMul as follows.

The original Shoup’s ModMul algorithm requires three operations: one 64-bit mul operation to compute $Q_{uh_i}$, and two 64-bit mulo operations to compute $Q_{uh_i} \cdot p_j$ and $X \cdot Y$, where $Q_u$ is an estimation of a quotient, and 64-bit mulhi (mullo) returns the upper (lower) 64-bit of a mul result which is 128-bit long. A single 64-bit mulhi operation can be emulated with four 32-bit mul ($hi \cdot hi$, $hi \cdot lo$, $lo \cdot hi$, $lo \cdot lo$), four 64-bit add, and five 64-bit shift operations. In this case, the estimated remainder can be either $r$ or $r + p_j$, which lies in a range of $[0, 2p_j]$.

However, one of the 32-bit mul ($lo \cdot lo$) for emulating 64-bit mulhi is used only for computing a carry from low 64-bit of mul. We can remove this $lo \cdot lo$ mul if the carry is ignored, and produce an approximated 64-bit mulhi ($Q_{uh_i}$) with only three mul instead of four. By applying this optimization, the estimated remainder lies in a range of $[0, 4p_j]$. As the upper bound of a remainder grows to $4p_j$, one more correction step (conditional subtraction) is needed, but the number of more expensive operations are reduced: one 32-bit mul, two 64-bit add, and one 64-bit shift instruction.

Matrix transposition in iCRT: SIMD instructions might lead to a poor cache utilization if they access a matrix storing elements in a row-major order by column direction (or vice versa), as this demands multiple cache lines at once. The resulting performance degradation is more prominent when the access stride is too large for a hardware prefetcher to be effective. iCRT experiences this issue because the matrix-matrix mul (line 9 in Algo. 6) accesses the temp matrix storing elements in a row-major order by column direction. We implicitly transfer the temp matrix using the scatter instructions in AVX-512 to address this issue.

Reducing the size of $\beta$ to $2^{32}$: We can remove the overhead of emulating 64-bit operations by using $\beta$ of $2^{32}$ instead of $2^{64}$ as AVX-512 naturally supports 32-bit mul and ADC. Using the smaller beta changes the number of instructions for mul and ADC to one, and reduces the number of instructions for modular mul to below the half. However, it also has shortcomings that $q\text{Limbs}$ should roughly be doubled to express numbers whose size is up to $q \cdot np$ also needs to be doubled because the upper bound of each prime number is $\beta$. Larger $q\text{Limbs}$ and $np$ imply bigger precomputed tables and more iterations for CRT, NTT, iNTT, and iCRT. It also increases the number of operations other than mul, modular mul, and ADC. A preliminary implementation shows no improvement in performance by using the small $\beta$ for CPUs.

C. Accelerating HE Mul on GPUs

Modern GPUs such as Volta [41] and Turing [42] have as many integer (INT32) processing units as single-precision floating-point (FP32) processing units, resulting in the multiply-accumulate throughput for INT32 numbers the same as that for FP32 numbers. Such massive throughput of integer operations makes GPU an attractive candidate for accelerating HE operations. We identify the following key points in fully exploiting the performance potential of GPUs when accelerating HE operations.

Parallelization strategies: CUDA programming model [43] for GPU has the following hierarchical structure of threads: multiple GPU threads are grouped to form a thread block and multiple thread blocks comprise a grid. A thread block is allocated to one of Streaming Multiprocessors (SMs). The threads in a thread block share the resources (e.g., shared memory) of the SM. Each thread block in a grid is allocated to each SM in a round-robin fashion, and the number of thread blocks (grid dimension) and the number of threads in a block (block dimension) are configured at each GPU kernel launch.

The basic parallelization strategy is to assign each independently computable output element in a function to a GPU thread. We launch $N \cdot np$ threads for CRT so that each thread computes one output element, which is a residue. NTT and
\texttt{int} launch $N/2 \cdot np$ threads each, where one thread performs one butterfly operation (Algo. 4) for each butterfly step using a simple radix-2 iterative NTT algorithm [34] that is also used for CPU implementation.

In case of \texttt{icrt}, a naïve parallelism strategy uses $N$-degree parallelism where one thread handles one output BigInt type coefficient. Prior studies [8], [22] took the same strategy. However, by changing the loop order as described above, we transform its core operation into a matrix-matrix mul operation, thereby taking advantage of $N \cdot \text{PLimbs}$-degree parallelism to maximize TLP. We can also exploit various optimization strategies developed for matrix-matrix mul in GPU (e.g., tiling principles in NVIDIA’s cutlass library [38]).

64-bit emulation vs. 32-bit word: As opposed to most CPUs that natively support 64-bit words, modern GPUs natively support 32-bit words and emulate 64-bit integer operations. To avoid the overhead of 64-bit emulation (whose throughput is more than an order of magnitude lower than that of the 32-bit counterpart), prior studies accelerating HE on GPU [8], [22] use 32-bit words ($\beta = 2^{32}$) and the prime numbers smaller than $\beta$. We also use 32-bit words and operations. Another advantage of using 32-bit words on GPU is that the operations with carry-in and carry-out can be used without emulation; modern NVIDIA GPUs support carry operations (e.g., addc, subc, and made in assembly-like virtual ISA, PTX [44] where the operations are called extended-precision integer arithmetic instructions). The throughput of these instructions is the same as the instructions without carry in recent GPU architectures [41], [42], enabling efficient computation on large integers without emulation.

Different strategies for BigInt modulo in \texttt{crt}: A naïve BigInt modulo is done by repetitive log$\beta$-bit shift, add, and modulo operation; for example, cuHE [22], takes this approach. By contrast, HEAAN accumulates the result of modulo on each $a_k \cdot \beta^k$ using a precomputed table in \texttt{crt}. In this case, the BigInt variable $\text{accum}$ (line 3 in Algo. 1) can span two or three words depending on $np$ and the size of each prime number. In the CPU implementation, $\text{accum}$ is guaranteed to span two words when using the representative parameters specified in Table VI, as an overflow does not happen for $np \leq 2^{64-58} = 64$ with prime numbers smaller than $2^{58}$. To guarantee $\text{accum}$ to be two-word long, we use $2^{57}$ as a lower bound of a prime for AVX-512 implementation instead of $2^{59}$ which is the default value of the reference HEAAN. However, in GPU with a 32-bit $\beta$, with primes smaller than $2^{30.2}$ only up to 4 ($= 2^{32-30}$) accumulation is allowed to guarantee that the overflow does not happen, which is nearly impossible as $np$ is 90 or higher when using the representative parameters.

To prevent the overflow, one might (1) use three-word $\text{accum}$ with an additional ADC operation added in the innermost loop to avoid expensive modulo operations, or (2) do modulo operations intermittently in the innermost loop (e.g., for every 4 accumulation in our case), to ensure that $\text{accum}$ spans only two words. We compare these strategies in Section VII.

Per-thread storage for accumulation in \texttt{icrt}: The baseline implementation of \texttt{icrt} with N-degree parallelism allocates a BigInt $\text{accum}$ (line 8 in Algo. 5) as a long array, in a per-GPU-thread manner. If $\text{accum}$ is not carefully allocated to fast storage, frequent cache thrashing might occur, leading to a significant performance degradation. The latest NVIDIA GPUs [41], [42] have a variety of storage types including register, L1 cache, L2 cache, device memory, and read-only constant memory. In the algorithm of original \texttt{icrt} (Algo. 5), $\text{temp}[j][i]$ is stored in register memory, so that it can be loaded quickly in a single cycle. On the other hand, because $\text{accum}$ is declared as a thread-local array and also it is dynamically indexed in the algorithm (e.g., used as $\text{accum}[idx]$ where $\text{idx}$ is a variable), it is not stored in register, which is the fastest storage on GPU. Instead, CUDA compiler stores it in global memory and caches into L1 and L2 (in CUDA programming model this is called local memory).

However, heavily using local memory can lead to cache thrashing when the grid dimension and block dimension increase, leading to a number of threads competing for cache, degrading overall performance. In order to mitigate the cache miss penalty, we suggest two different optimizations when using $N$ parallelism in \texttt{icrt}: (1) using fewer threads by simply reducing block dimension and grid dimension, using the grid-stride loop method [33], or (2) pinning each $\text{accum}$ array in L1 cache through allocating the array in shared memory; this is possible as the shared memory shares capacity with the L1 unified cache. (2) is similar to the implementation of CRT kernel in cuHE [22], which uses the shared memory for storing thread-local arrays. We compare the methods on cuHE’s \texttt{icrt} kernel [22] which implements Algo. 5 with $N$ parallelism, along with loop reordering with $N \cdot \text{PLimbs}$ parallelism which is explained in Section V-A.

**High-radix NTT (\texttt{int}):** Radix-2 NTT is memory-bound; GPU reads and writes a large input $IN_{\text{NTT}}(np, N)$ (dozens of megabytes with typical $np$ and $N$ values specified in Table III, exceeding the size of L1 and L2 caches of GPU) by $\log_2 N$ times. At each butt function in Algo. 3, a GPU thread reads two values of $IN$ from the device memory and writes two output values back to the device memory.

Using high radix NTT (radix-$k$ with $k > 2$) can mitigate the memory bandwidth bottleneck because each GPU thread reads and writes $k$ values within $IN$ in the butt operation performing $k$-point NTT. It changes the number of transferring $IN$ from $\log_2 N$ above to $\log_k N$, reducing the number of main memory accesses needed for NTT. However, increasing the radix is not always beneficial because, as each thread takes more than two inputs, register pressure on each GPU thread increases. Using registers more than the register file size of a streaming multiprocessor causes register spilling to local memory, leading to performance degradation with additional data loads from the main memory. Given the constraint, we use an appropriate size of radix (radix-32) to alleviate the high
pressure of main memory bandwidth and conduct a sensitivity study in Section VII.

VI. Experimental Setup

We compared the performance of the reference HEAAN [1], our AVX-512 implementation with multi-threading, and GPU implementation. We used Intel Xeon CPU (Skylake-based Xeon Platinum 8160 operating at 2.1 GHz) and NVIDIA GPU (Turing Titan RTX operating at 1.35 GHz). The CPU system consists of 24 cores per socket and each core has two AVX-512 FMA units, achieving a peak 64-bit integer performance of 1.61 TOPS per socket. Each socket has six memory channels, each equipped with DDR4-2666 DRAM modules. We did not use HyperThreading; the number of cores utilized was the same as the number of CPU threads populated. The GPU system consists of 72 streaming multiprocessors (SMs), each with 64 CUDA cores, performing up to 4,608 32-bit integer operations per cycle. The size of each L1 unified cache and L2 shared cache in the GPU is 128 KB (per SM) and 6 MB, respectively. Even if the CPU system has two CPU sockets, we only used one socket to compare it with the GPU system with a single discrete GPU.

We tabulate the key parameters for HE Mul of HEAAN on CPU and GPU in Table VI. We measured the execution time of HE Mul, excluding time for memory operations, such as malloc, free, and data transfers from host to the device for GPU. We conducted each experiment 32 times and reported the average.

VII. Evaluation

We evaluated the effectiveness of the proposed optimizations in accelerating HEAAN mul by comparing against the reference HEAAN (Ref). For CPU, our optimizations exploit both intra-core and inter-core parallelism. We compared the basic implementation utilizing AVX-512 instructions (AVX), the one with the modified Shoup’s ModMul on top of AVX (AVX-M), and the one transposing the temp matrix on top of AVX-M (AVX-MT). In the basic GPU implementation (GPU), we adopted radix-2 iterative NTT for NTT and iNTT. We modified the CRT kernel of cuHE [22], which only exploits N-degree parallelism, to exploit N-np-degree parallelism. Also, we used the iCRT kernel of cuHE. We compared GPU with the followings: the implementation optimizing CRT by using ADC instead of intermittently conducting modulo operations (GPU-C), the one adjusting the number of launching threads on top of GPU-C (GPU-CT), the one using shared memory to pin the arrays of each thread to L1 unified cache on top of GPU-C (GPU-CP), the one applying loop reordering (Algo. 6) to translate a majority of ieee computation into matrix-matrix mul to use N-P limbs-degree parallelism on top of GPU-C (GPU-CL), and the one implemented with high-radix NTT and iNTT to reduce main memory accesses and utilize GPU’s computing power more efficiently on top of GPU-CL (GPU-CLH).

We made the following key observations. First, exploiting the massive parallelism supported by modern CPUs and GPUs gives even more than 100× performance improvement in HE Mul. Table VII shows the execution time and the relative speedup of the CPU and GPU implementations after applying a series of architecture-aware optimizations. AVX-MT and GPU-CLH, the implementations giving the best performance for CPU and GPU, achieve 42.9× and 134.1× speedup, respectively, compared to the single-thread Ref. GPU-CLH performs 4.3× and 2.3× better than AVX-MT on CRT and iCRT thanks to more ALUs populated on GPU. Also, by reducing the main memory accesses through increasing the radix, GPU-CLH achieves 2.35× and 2.17× performance improvement in NTT and iNTT, respectively, compared to AVX-MT’s implementation.

Second, our CPU implementations are highly scalable across both intra-core and inter-core dimensions. AVX is effective regardless of the number of CPU threads populated, providing 2.0× and 2.7× performance gain over Ref when a single and 24 threads are utilized, respectively (see Figure 4(a) and (b)). Among the primary functions, NTT is the best in scalability, leading to 7.7× speedup for AVX over Ref when 24 threads are populated. Overall, AVX experiences 19.4× speedup when the number of populated threads increases from 1 to 24, exhibiting a better scalability than Ref (14.8×) because of the following reasons. AVX and Ref exploit parallelism in different ways for CRT as described in Section V. In Ref, each thread operates on different prime numbers (np-degree parallelism) where np is not large (e.g., 42 or 63), and hence Ref is more susceptible to a load imbalance across threads. By contrast, each thread operates on different coefficients (N-degree parallelism) in AVX, exhibiting better scalability. For iCRT, data accesses for the matrix occur in column direction during matrix-matrix mul, causing its performance memory-bound because hardware prefetching becomes ineffective. However, with 24 threads being utilized, hardware prefetching hits more frequently because a thread might access the data in the adjacent columns that are prefetched by other threads, leading to better performance.

The additional optimizations applied to the AVX-512 implementation are effective as well. Figure 4(c) shows the impact of these optimizations on each major function when 24 threads are used. In AVX-M, both NTT and iNTT are 10% faster than AVX because these functions compute modular mul frequently. iCRT experiences a 18% speedup in AVX-MT compared to AVX-M because the matrix transposition alleviates the memory-bound issue.

Third, the performance of GPU reaches close to full potential through our microarchitecture-aware optimizations.
TABLE VII: Comparing the execution time of HE Mul among a single- and 24-thread reference HEAAN (Ref-1 and Ref-24), a 24-thread optimized AVX-512 implementation (AVX-MT-24), and an optimized GPU implementation (GPU-CLH).

| Function | Ref-1 (baseline) | Ref-24 | AVX-MT-24 | GPU-CLH |
|----------|------------------|--------|-----------|---------|
| CRT      | 639.9            | 40.4   | 17.5      | 4.1     |
| NTT      | 1541.0           | 73.3   | 8.7       | 3.7     |
| iNTT     | 584.6            | 28.3   | 10.2      | 4.7     |
| iCRT     | 2126.7           | 130.1  | 45.4      | 19.4    |
| Extra    | 215.7            | 73.1   | 37.3      | 6.2     |
| Total    | 5108.0           | 345.3  | 119.1     | 38.1    |

(a) Execution time on single-thread (b) Execution time on 24-threads (c) Relative execution time and speedup per function

Fig. 4: Comparing HE Mul execution time among Ref, AVX-512 implementation (AVX), and optimized AVX (AVX-M and AVX-MT) when (a) one and (b) 24 threads are utilized, and (c) per-function speedup when using 24 threads.

Fig. 5: Comparing HE Mul execution time (a) among Ref-24, the baseline GPU (GPU), and optimized GPU (GPU-C, GPU-CL and GPU-CLH), and relative speedup of (b) GPU and GPU-C for CRT, (c) GPU and GPU-C[T/P/L] for iCRT, and (d) GPU-CL and GPU-CLH for NTT/iNTT.

Figure 5(a) shows the execution time of HE Mul on various GPU implementations compared to that of the reference HEAAN running on CPU with 24 threads (Ref-24). Even the baseline GPU implementation (GPU) outperforms Ref-24 by 1.52×. Most of the speedup comes from accelerating NTT and iNTT, iCRT in GPU, whose implementation we adopt from cuHE [22], performs poorly; it is even 1.43× slower than that in Ref-24 and takes 81.2% of total HE Mul execution time.

To reduce the execution time of iCRT, we devised the following optimizations and compared their performance in Figure 5(c). By adjusting the number of launching threads, we reduced the degree of performance impact due to cache thrashing, achieving a speedup of 4.22× (GPU-CT) compared to that of GPU. Pinning thread-local arrays to L1 cache (GPU-CP) performs better than GPU-CT, reaching 6.79× of speedup. Finally, GPU-CL was the best among all the iCRT optimizations (9.58× of speedup), by effectively exploiting N<sub>np</sub>-degree parallelism through the loop reordering explained in Section V.

Table VIII compared the execution time of CRT when using different strategies to convert a BigInt number to an array of residue numbers in an RNS domain. GPU

| Time for CRT (ms) | Speedup |
|-------------------|---------|
| GPU               | 14.95   | 1.00× |
| GPU-Mod1          | 16.80   | 0.89× |
| GPU-Mod2          | 10.47   | 1.43× |
| GPU-Mod4          | 7.56    | 1.98× |
| GPU-C             | 4.11    | 3.64× |
TABLE IX: Comparing the execution time of NTT and iNTT when altering their radix values.

| Radix | NTT Time (ms) | Speedup | iNTT Time (ms) | Speedup |
|-------|---------------|---------|----------------|---------|
| 2     | 8.73          | 1.00    | 9.76           | 1.00    |
| 4     | 4.74          | 1.84    | 5.47           | 1.78    |
| 16    | 3.65          | 2.39    | 4.88           | 2.00    |
| 32    | 3.72          | 2.35    | 4.67           | 2.09    |

TABLE X: The number of required AVX-512 instructions (add, sub, mul, shift, and cmp) for each function with \( (np, q_{\text{Limbs}}) \) of \((43, 19)\). We compared the cases where each of 64-bit mul, modular mul, and ADC is supported by emulation and by a single native instruction.

| CRT   | NTT | iNTT | iCRT |
|-------|-----|------|------|
| by emulation | 155M | 48M  | 47M  | 319M |
| by single native instr. | 27M  | 17M  | 17M  | 51M  |

does not precompute \( \text{mod}(\beta^k, p_j) \) and performs a modulo operation on every limb (one limb for \( \beta \)) of the BigInt. **GPU-Modx** means applying modulo operation every \( x \) iteration in the inner-most loop of line 5 in Algo. 1. Even if using the precomputed table, the complexity of modulo operations per iteration \((\text{GPU-Mod1})\) is even worse than GPU by \( 1.1 \times \). This is because both implementations compute the same number of modulo operations whereas GPU-Mod1 imposes more pressure on local memory utilization. Fewer modulo operations led to better performance; **GPU-Mod4** performs \( 1.98 \times \) better than GPU. By letting the partial sum \((\text{accum})\) span three words instead of two words utilizing ADC in every iteration, **GPU-C** performs best with the speedup of \( 3.64 \times \).

Figure 5(d) shows the performance improvement of NTT and iNTT by increasing their radix values. Because NTT and iNTT algorithms are mostly symmetrical, they experience a similar degree of performance improvement by \( 2.35 \times \) (NTT) and \( 2.09 \times \) (iNTT). iNTT improves slightly less because iNTT includes additional computations such as element-wise division by \( N \), which does not gain speedup from using higher radix. Table IX shows the execution time of NTT and iNTT when varying the radix values. As the radix grows from 2 to 16, the performance of NTT and iNTT increases, taking advantage of reducing the memory accesses and hence alleviating the memory bandwidth bottleneck. However, the speedup saturates when the radix rises from 16 to 32 because of the register spilling to local memory; when radix increases beyond 32, the performance deteriorates due to the higher register pressure.

**VIII. DISCUSSION**

The impact of supporting the emulated operations natively on AVX-512: As described in Section V, the cost of emulating 64-bit mul, modular mul, and ADC operations is significant in AVX-512 implementations. If some future CPUs support these instructions natively, the execution time of HE Mul could be reduced substantially. Table X summarizes the number of AVX-512 instructions required to perform each major function by comparing the cases where each of 64-bit mul, modular mul, and ADC is supported by either emulation and by a single native instruction. CRT and iCRT require just 17.3% and 15.8% of AVX-512 instructions if a future CPU supports these instructions natively, not through emulation. NTT and iNTT require one third of instructions by the instruction extension. Because HE Mul is mostly computation-bound, the significant reduction in the number of instructions would lead to a similar degree of performance improvement.

Impact of \( Q \) on the characteristics of HE Mul: \( Q \) determines multiplicative depth \( L \); a larger depth requires a bigger \( Q \). However, \( N \) must increase proportionally to \( \log Q \) to ensure a certain level of security (see Table II). Also, \( q_{\text{Limbs}} \), \( np \), and \( P_{\text{Limbs}} \) increase in proportion to \( \log Q \). Based on these relationships, the computational complexity of Table IV can be expressed in terms of \( \log Q \). The complexity of CRT and iCRT is \( O((\log Q)^3) \) whereas that of NTT and iNTT is \( O(\log(\log Q) \cdot (\log Q)^2) \). Figure 6 shows the estimated number of operations for HE Mul according to \( \log Q \). When \( Q \) is small (e.g., \( \log Q=150 \)), CRT, NTT, iNTT, and iCRT require a similar number of operations, but as \( Q \) increases, CRT and iCRT become more dominant. Overall, the total number of operations for HE Mul is proportional to \( (\log Q)^3 \).

When an application requires a large number (e.g., billions) of HE Mul, using large \( Q \) amortizes the cost of the expensive bootstrapping operation. However, using too large \( Q \) is costly because the maximum number of messages \( (n) \) that can be multiplied together by a HE Mul is \( N/2 \), where the complexity of a HE Mul is super-linear, \( O((\log Q)^3) = O(N^3) \). The \( Q \) value we mainly target is 1,200, which is large enough to amortize the cost of bootstrapping; other HE accelerators [47], [50] focused on much smaller \( Q \) values. For example, [50] used the \( Q \) value of 180 without considering bootstrapping.

Impact of \( q \) on the characteristics of HE Mul: As described in Section III, rescaling, which decreases \( \log q \) by \( \log p \), is performed after each HE Mul to prevent the amount of message information in the ciphertext from increasing exponentially. As HE Mul is repeated, \( q \) decreases, so does \( q_{\text{Limbs}} \) and \( np \). In region 1 of HE Mul, \( np \) decreases linearly with \( \log q \) because two \( \log q^2 \)-bit BitInt numbers are multiplied
per ciphertext coefficient. By contrast, in region 2, np should be set to represent \((\log q + \log Q^2)\)-bit BigInt (to multiply over the evaluation key polynomial). PLimbs has the same trend as np. Figure 7 shows the computation amount of HE Mul according to the \(\log q\) in the AVX-512 configuration of Section VI calculated based on Table IV. As np is proportional to \((\log q + \log Q^2)\) in region 2, the number of operations for HE Mul when \(\log q\) becomes 30 (the smallest number where no more HE Mul is applicable) is still 24% of that when \(\log q\) is 1,200. Also, iCRT is dominant regardless the size of \(q\).

The applicability of optimization techniques to other libraries supporting CKKS: In addition to HEAAN, there are several other libraries [2], [3], [13], [32] that support CKKS. The libraries fall into one of the two groups: libraries supporting full-RNS and non-RNS CKKS, as shown in Table XI. Non-RNS types manage each coefficient of polynomials of ciphertext in a big integer domain. By contrast, full-RNS types let the coefficient stay in an RNS domain during the whole procedure of homomorphic operations, resulting in faster operations. However, using full-RNS is less flexible because there exist rigid limitations while choosing the rescaling factor \(p\) and the modulus \(Q\). Each prime composing an RNS representation of \(Q\) in full-RNS CKKS should be set to be close to the rescaling factor \(p\) [15]. In non-RNS CKKS, by contrast, one can freely choose a rescaling factor \(p\) independent of \(Q\) without considering the approximation error existing in full-RNS CKKS. Moreover, due to these parameter limitations, the multiplicative depth of full-RNS variants is lower than an non-RNS scheme for a given security bit and error bound.

For the libraries supporting CKKS other than HEAAN, our optimizations described in Section V are partially applicable. Other non-RNS CKKS libraries can apply our optimization techniques because they use the same primary functions as HEAAN. Also, although full-RNS variants do not require \(\text{CRT}\) and \(i\text{CRT}\), the optimization techniques for \(\text{NTT}\) and \(i\text{NTT}\) can be applied. Also, we can partially apply our techniques in \(\text{CRT}\) to the functions that change the number of primes in the RNS domain (mod up/down in Table XI). mod up increases the number of primes of an RNS representation of a given big integer, whereas mod down decreases it with an additional division operation [9], [15]. Both functions can take advantage of our optimizations as their core functions are similar to applying \(\text{CRT}\) right after \(i\text{CRT}\).

### IX. Related Work

**FPGA-based HE accelerators:** There have been numerous studies [21], [25], [45], [47], [49], [50] to accelerate HE operations using FPGA. [21], [25], [45] accelerate LTV-based FHE schemes whereas [49], [50] accelerate FV-based FHE schemes. However, LTV and FV schemes have a limitation in practical use because they cannot perform approximate computations. HEAX [47] uses FPGA to accelerate Microsoft SEAL, which supports a full-RNS variant of the CKKS scheme; however, HEAX considers only small parameter sizes \((Q \leq 438\) and \(N \leq 2^{14}\)), and the full-RNS variant it targets is not as versatile as the original HEAAN we accelerate in this paper due to the limitations in choosing rescaling factors and prime numbers.

**GPU libraries for HE:** [4], [7], [8], [22] propose to accelerate the HE operations using GPUs. However, they either do not take advantage of the algorithm’s internal parallelism sufficiently, operate on only small or limited parameters, or do not consider the cost of modulo operations in GPUs. Moreover, all the aforementioned studies did not conduct a rigorous analysis of computational complexity and data access patterns of HE Mul, making it hard to assess the effectiveness of the proposed accelerators compared to the CPU or GPU implementations applying architecture-aware optimizations.

### X. Conclusion

We have demystified the key operations of HEAAN, a representative and popular FHE scheme, from a computer architect’s perspective. After identifying that multiplying the encrypted data (ciphertext) is the most computationally demanding, we accelerated the major functions of HE Mul (\(\text{CRT}, \text{NTT}, i\text{NTT},\) and \(i\text{CRT}\)) on CPU and GPU. To accelerate the major functions on CPU, we populate multiple cores by using multi-threading (inter-core parallelism) and AVX-512 instructions (intra-core parallelism). We accelerate HE Mul on GPU by effectively exploiting massive thread-level parallelism. Moreover, based on the in-depth analysis of the major functions for HE Mul, we introduced a series of architecture-aware optimization techniques such as loop reordering and matrix transposition for \(i\text{CRT}\) and taking a synergy between precomputation and delayed modulo operations for \(\text{CRT}\). Our accelerated HEAAN on CPU and GPU outperforms the reference single-thread HEAAN on CPU by 42.9× and 134.1×, respectively, in HE Mul, setting a new baseline for HE acceleration studies targeting practical usage.
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