Abstract

The Unified Power Quality Conditioner (UPQC) is a customer adjust device, which deals with the Power-Quality issues in the power distribution system. In the proposed topology allows UPQC to have a lower dc-link voltage without limiting its compensation capability. This topology also allows to maintain the dc-link voltage need of the series and shunt active filters of the UPQC. A simulation study of the suggested topology has been performed using Matlab/Simulink. In the extension for the proposed topology added with a multilevel inverter and the compensated DVR voltages. The load voltages after settlement are shown in the same determine. This clearly reveals the customized topology with multilevel inverter efficiency is better than the suggested topology with a less dc-link volts, decrease in switching function, and regular monitoring of referrals compensator voltages.

Keywords:
1. Introduction

With the progression of power electronic devices and digital control technology, the renewable energy will be linked with the distribution systems. On the other hand, with the growth of the power electronic devices, nonlinear loads and uneven loads have deteriorated the Power Quality (PQ) in the power system. Custom power devices have been proposed for improving the quality and continuity of power. The shunt part of the UPQC is known as static synchronous compensator (DSTATCOM), and it is used to reactive power compensation, harmonics reducing and balance the load currents and generate the gate signal generation.

In this work, a UPQC topology with lower dc-link voltage is considered suitable. The topology consists of capacitor in sequence with the interfacing inductor of the shunt active filter. The series capacitor allows decrease in dc-link voltage need of the shunt active filter and at the same time paying the reactive power required by the load, so as to sustain unity power factor, without limiting its efficiency. The studies are performed using simulation and specific outputs are provided in the project.

2. Conventional and Proposed Topologies of UPQC

In this area, the traditional and suggested topology of the UPQC is mentioned in details. Figure 1 reveals the power

![Figure 1. Equivalent circuit of neutral-clamped VSI topology-based UPQC.](image-url)
circuit of the neutral-clamped VSI topology-based UPQC which is regarded as the traditional topology in this research. Even though this topology needs two dc storage devices, each leg of the VSI can be managed individually, and monitoring is smooth with less number of switches in comparison to other VSI topologies. In Figure 1, Vsa, Vsb, and Vsc are source voltages of phases a, b, and c, respectively.

Figure 2 symbolizes the equivalent circuit of the suggested VSI topology for UPQC compensated system. In this topology, the system neutral has been linked with the adverse terminal of the dc bus along with the capacitor Cf in series with the interfacing inductance of the shunt active filter. It is generally known as personalized topology. Each leg of the inverter can be controlled individually in shunt active filter. Compared with the topologies described in the literature, this topology does not demand the fourth leg in the shunt active filter for three-phase four-wire system.

3. Design of VSI Parameters

The parameters of the VSI need to be developed properly for better tracking efficiency. The essential parameters that need to be taken into account while developing conventional VSI are Vdc, Cdc, Lf, Lse, Cse, and changing frequency (fsw). The design details of the VSI parameters for the shunt and series active filter are given. In accordance with the following equations, the factors of the VSI are selected for study.

3.1 Design of Shunt Active Filter VSI Parameters

Consider the active filter is linked with an X kVA system and offers with 0.5X kVA and 2X kVA managing ability under transient circumstances for n cycles. During transient, with a rise in system kVA load, the voltage across each dc-link capacitor (Vdc) reduces and the other way around. Enabling a highest possible of 25% difference in Vdc during transient, the differential power ($\Delta E_c$) across Cdc is given by

$$\Delta E_c = \frac{C_d}{2} \left[ (1.125V_{dc})^2 - (0.875V_{dc})^2 \right]$$

(1)

The change in system energy ($\Delta E_s$) for a load change from 2X kVA to 0.5X kVA is

$$\Delta E_s = \left( 2X - \frac{X}{2} \right) nT$$

(2)

Equating (1) and (2), the dc-link capacitor value is given by

$$C_{dc} = \frac{2 \left( 2X - \frac{X}{2} \right) nT}{(1.125V_{dc})^2 - (0.875V_{dc})^2}$$

(3)

Where, $V_m$ is the optimum value of the source voltage, $X$ is the kVA ranking of the system, n is number of cycles, and T period of time of each pattern. A scientific research has been performed for various principles of interfacing inductance principles with the difference of the dc-link voltage, with Vdc = $mV_m$, and it is discovered that $m = 1.6$ gives fairly good switching efficiency of the VSI. The estimated connection between $m$ and lowest (fswmin), highest possible changing frequency (fswmax) is acquired by research of the VSI, and this is given below. For changing frequency difference roughly from 6 kHz to 10 kHz, the value of $m$ is 1.58, which is taken as 1.6 in the research. Depending on this, the shunt interfacing inductance has been produced getting into account of the highest possible changing frequency and is given below:

$$m = \frac{1}{\sqrt{1 - \frac{f_{swmin}}{f_{swmax}}}}$$

(4)

$$L_f = \frac{mV_m}{4h_1 f_{swmax}}$$

(5)

where

$$h_1 = \sqrt{\frac{k_1 (2m^2 - 1)}{4m^2 f_{swmax}}}$$

(6)

Where, $h_1$ is the hysteresis band limit, $k1$ and $k2$ are proportionality constants.

3.2 Design of Series Active Filter VSI Parameters

To help make the series active filter system a first-order program, a resistor is added in sequence with the
narrow capacitor, known as switching band resistor (Rsw). The capacitor branch current is separated into two components—a fundamental current, corresponding to the fundamental reference voltage (Vref1) and a changing frequency current Isw, corresponding to the group voltage (Vsw). The DVR voltage and the current of the capacitor are given by

\[ V_{dvr} = \sqrt{V_{ref1}^2 + V_{sw}^2} \]

\[ I_{se} = \sqrt{I_{se1}^2 + I_{sw}^2} \]

\[ V_{sw} = I_{sw}R_{sw} = \frac{h_2}{\sqrt{3}} \]

\[ V_{ref1} = I_{set}X_{se} = \frac{I_{sci}}{2\pi f_j C_{se}} \] (7)

Where \( h_2 \) is the hysteresis band voltage. The resistance (Rsw) and the capacitance (Cse) values are expressed in terms of band voltage vsw and rated references voltage (Vref1), respectively and are given by

\[ R_{sw} = \frac{h_2}{I_{sw} \sqrt{3}} \]

\[ C_{se} = \frac{I_{set}}{V_{ref1} 2\pi f_j} \] (8)

\[ L_{se} = \frac{(V_{bus})R_{sw}}{4 f_{swmax} h_2} \] (9)

Where Vbus is the total dc-link voltage across both the dc-link capacitors. A design example is illustrated for a rated voltage of 230 V line to neutral and the dc-link voltage reference (Vdcref) of the conventional VSI topology has been taken as 1.6 Vm for each capacitor. The hysteresis band (h1) is taken as 0.5 A.

3.3 Design of Cf for the Proposed VSI Topology

The design of the Cf on value to which the dc-link voltage is decreased. In common, load with only nonlinear elements of voltages are very unusual and most of the electric loads are combination of the linear inductive and nonlinear loads. Under these circumstances, the suggested topology will continue to perform effectively. The design of the value of Cf is performed at the highest possible load current, i.e., with the lowest load impedance to make sure that the developed Cf will execute satisfactorily at all other running circumstances. If Smax is the highest possible kVA ranking of a system and Vbase is the base voltage of the system, then the lowest impedance in the system is given as

\[ Z_{min} = \frac{V_{base}^2}{S_{max}} = |R_j + jX_j| \] (say) (10)

\[ I_{filter} = \frac{V_{inv1} - V_{dcref}}{R_j + j(X_{cf} - X_{j})} \] (11)

\[ I_{load} = \frac{V_{dcref}}{R_j + jX_j} \] (12)

where, Xlf = 2πfL, Xl = 2πfL, Xcf = 1/2πfCf, and f is the supply frequency of fundamental voltage. Neglecting the interfacing resistance and equating the imaginary parts of the above equations gives equation (13). The essential part of inverter voltage with regards to dc-link voltage is described, as given below

\[ \frac{V_{dcref}X_{j}}{R_j^2 + X_j^2} = \frac{V_{inv1} - V_{dcref}}{(X_{cf} - X_{j})^2} \] (X_{cf} - X_{j}) \] (13)

\[ V_{inv1} = \frac{0.612V_{dc}}{2\sqrt{3}} \] (14)

\[ uV_{dc} - v_{l} = L_j \frac{di_j}{dt} + R_ji_j \] (15)

\[ (uV_{dc} - \frac{1}{C_f} \int i_j dt) - v_{l} = L_j \frac{di_j}{dt} + R_ji_j \] (16)

In common, if the filter current (If) moves from the inverter terminal to the PCC, the voltage at the inverter terminal should be at a greater prospective. Due to this purpose, in traditional VSI topologies, the dc-link voltage is managed greater than the voltage at the PCC. Equations (15) and (16) provide the KVL along the filter division for traditional topology and the suggested personalized topology, respectively.

In the personalized topology along with the series capacitor in the shunt active filter, the system neutral is linked with the adverse terminal of the dc bus capacitor. This will present a beneficial dc voltage element in the inverter outcome volts. This is because, when the top change is “ON,” +Vbus seems to be at the inverter outcome, and 0 V seems to be when the bottom switch is “ON.” Thus, the inverter outcome voltage will have dc
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Voltage element along with the ac voltage. The dc voltage is obstructed by the series capacitor, and thus the voltage across the series capacitor will be having two elements, one is the ac element, which will be in phase opposition to the PCC volts, and the other is the dc element.

The personalized topology contains only one dc capacitor as the neutral is straight linked with the adverse terminal of the dc bus, thus it prevents the need of controlling capacitor currents, which is a significant drawback of the neutral-clamped topology.

4. Using Diode-Clamped Multilevel Inverter for Better Performance

The problem of reducing harmonics in switching inverters has been the focus of research. The current trends of modulation control for multilevel inverters is to output high quality power with high efficiency Pulse Width Modulation methods are not the best solution for multilevel inverter control due to their high switching frequency. The selective harmonic elimination method has implemented as a promising modulation control method for multilevel inverters. As the number of levels increases the harmonic content of the output waveform decreases the filter size. Lower switching losses due to the devices being switched at the fundamental frequency without increasing the harmonic content in the output. Reactive power flow can be controlled, as this does not cause unbalance in the capacitor voltages. Fast dynamic response Back to back operation is possible.

The output voltage levels possible for one phase of the inverter with the negative dc voltage 0 v as a reference. State condition 1 means the switch is ON and 0 means the switch is OFF. Each phase has 5 complementary switch pairs such that turning on one of the switches of the pair requires that the other complementary switch be turned off. The switch pairs for phase legs. Table 1 also shows that in a diode-clamped multi level inverter, the switches that are on for a particular phase leg are always adjacent and in series.

5. Generation of Reference Compensator Currents Under Unbalanced and Distorted Voltages

In this work, the load currents are uneven and altered, these currents circulation through the feeder impedance and make the voltage at terminal uneven and altered. The expression for reference compensator voltages are given in equation (17). In this formula, Plavg is the common load power, Ploss signifies the changing failures and ohmic failures in actual compensator and it is produced using a capacitor voltage PI operator. The phase Plavg is acquired using a moving regular filter of one cycle window of time T in a few moments. The phrase φ is the preferred stage position between the source voltage and current

\[ i_{fa}^* = i_{fa} - i_{fa} = i_{fa} - \sqrt{3} \left( v_{fa1}^+ - v_{fa1}^* \right) \left( P_{avg} + P_{loss} \right) \]

\[ i_{fb}^* = i_{fb} - i_{fb} = i_{fb} - \sqrt{3} \left( v_{fb1}^+ - v_{fb1}^* \right) \left( P_{avg} + P_{loss} \right) \]

Table 1. Switching Properties of 5 Level Inverter

| Voltage Vdc | S_a1 | S_a2 | S_a3 | S_a4 | S_a5 | S_a6 | S_a7 |
|-------------|------|------|------|------|------|------|------|
| V_a = 4 Vdc | 1    | 1    | 1    | 0    | 0    | 0    | 0    |
| V_a = 3 Vdc | 0    | 1    | 1    | 1    | 0    | 0    | 0    |
| V_a = 2 Vdc | 0    | 0    | 1    | 1    | 1    | 0    | 0    |
| V_a = Vdc   | 0    | 0    | 0    | 1    | 1    | 1    | 0    |
| V_a = 0     | 0    | 0    | 0    | 0    | 1    | 1    | 1    |

Figure 3. A three-phase five-level diode-clamped multilevel inverter schematic.
\[ i_{fc}^{+} = i_{fc} - i_{sc}^{+} = i_{fc} - \frac{v_{c1}^+ + j(v_{a1}^+ - v_{b1}^+)}{A} (P_{avg} + P_{loss}) \]  

where

\[ \Delta = \sum_{j=a,b,c} (v_{j1}^+) \left( \tan \frac{\phi_{j1}}{\sqrt{3}} \right) \]

Figure 4. Control block diagram for UPQC.

The above algorithm gives balanced source currents after compensation irrespective of unbalanced and distorted supply.

6. Simulation Results

The compensated DVR voltages and load voltages after settlement are shown in the same determine. This clearly reveals the customized topology with multilevel inverter efficiency is better than the suggested topology with a less dc-link volts, decrease in switching function and regular monitoring of referrals compensator voltages.

6.1 Proposed Method Results

Figure 5. Simulation results with modified topology. (a) Voltage across series capacitor and load voltage in phase-a. (b) Inverter output voltage in leg-a of shunt active filter. (c) DC and fundamental values of voltage across series capacitor and inverter output voltage.
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Figure 6. Simulation results using modified topology. (a) DC capacitor voltages. (b) Source currents after compensation. (c) Voltage across the interfacing inductor in phase-a of the shunt active filter. (d) Shunt active filter currents. (e) Terminal voltages with sag, DVR injected voltages, and load voltages after compensation.

6.2 Extension Method Results with Multilevel Inverter
Figure 7. Simulation results with modified topology with multilevel inverter. (a) Voltage across series capacitor and load voltage in phase-a. (b) Inverter output voltage in leg-a of shunt active filter. (c) DC and fundamental values of voltage across series capacitor and inverter output voltage.
7. Conclusion

A personalized UPQC topology for three-phase four-wire system has been suggested, which has the ability to make up the load at a reduced dc-link voltage under non firm source. The suggested personalized topology gives the key benefits of both the traditional neutral-clamped topology and the four-leg topology. Specific relative research is made for the traditional and personalized topologies. From the research, it is discovered that the personalized topology has less regular changing frequency, less THDs in the source voltages and load voltages with decreased dc-link voltage as opposed to traditional UPQC topology.

The personalized topology with multilevel inverter performance is better than the recommended topology with a less dc-link voltage, loss of switching operation and regular tracking of recommendations compensator currents.

8. References

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