An Investigation into the $HfO_2/Si$ Interface: Materials Science Challenges and their Effects on MOSFET Device Performance

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Abstract

Since the 1960’s when Gordon Moore proposed that the transistor density in our electronic devices should double every two years while the cost is halved, the semiconductor industry has taken this statement to heart. Over the last few decades, no other industry has seen growth even comparably close to that experienced by the semiconductors industry. This has all been made possible by the unbroken string of ingenious breakthroughs by brilliant minds that have been working tirelessly to shrink down transistors. The latest of which is the use of high-k dielectrics and a return to metal gates combined with 3D-transistor architectures. This has been the enabling technology for the transition from the $90$ nm node to the $45$ nm node, allowing us to shrink our transistors further without losing additional gate control.

The fundamental reason for using a high-k gate dielectric compared to $SiO_2$ is that shrinking our gate oxide further, which is already at a few angstroms, is no longer a feasible option to gain additional gate control. High-k dielectric overcome this by exploiting the fundamental physics of capacitors and the materials science of dielectrics to provide a viable option to increase gate control without the need for successively thinner gate oxides. Hafnium Oxide ($HfO_2$) is the most studied and popular of such materials. Its high dielectric constant $\sim 16 - 25$ and interface stability with silicon at operating temperatures make it an ideal candidate for use in current CMOS technology. Intel has been using $HfO_2$ for their logic technology foundries for its $32$ nm node and Micron its partner in memory has been using $HfO_2$ for its DRAM access transistors and capacitors for the $50$ nm node, all since the early 2010’s. Despite its deceivingly simple appearance, the processes involved in the fabrication of such high-k $HfO_2/Si$ interfaces are full of process subtleties and fabrication nuances. One of the primary reasons for this is the formation of a $SiO_2$ interlayer after deposition at process temperatures ($\sim 600^\circ C - 1000^\circ C$) which degrades our final transistors gate control and ultimately the device characteristics.

In this term paper we hope to explore the physics and materials science of these high-k $HfO_2/Si$ interfaces, discussing the challenges and ways to overcome them when it comes to its actual fabrication, and how this ultimately affects our device performance. This paper is broadly divided into three sections where we look at the thermodynamics, reaction kinetics and atomic diffusion kinetics, after which we look at the effects of these parameters on device performance and fabrication.
Introduction

Moore’s law has been the guiding force for the semiconductors industry since the last few decades, enabling it to grow at unprecedented rates unmatched by any other industry. It is no understatement to say that this urge to double the transistor density while roughly halving the cost every two years has driven the enormous progress seen in the current information age. Complementary MOS-FET technology or CMOS is at the heart of all this development, offering many distinct advantages over its competitors. Especially zero static power consumption, which makes large circuits feasible and scalable. The ability to achieve high logic density on IC’s while maintaining ease in integration also played a major role in CMOS triumphing. A unique feature of CMOS, is the use of both NMOS and PMOS devices as complementary elements of a singular logic circuit thereby lending it its name. This necessitates that the fabrication of such devices take place on a shared substrate with diffusion well regions for a PMOS device always next to a NMOS device or vice-versa, as seen in Figure 1. This adds to the complexity in fabrication but with modern techniques is easily achievable and makes the resulting circuits much more compact compared to other logic paradigms. However, in recent years, as we approach atomic scale dimensions the continued miniaturization of transistor has become increasingly troublesome. Quantum effects such as DIBL, channel-length modulation and the other so called short channel effects dominate as one encroaches into further decreasing length scales. Furthermore, fabrication limitations on creating atomically thin gate oxides reliably, further drives up the cost. To combat this, engineers have looked to other routes to miniaturization. Intel in 2007 announced a breakthrough, their use of high-k dielectrics and metal gates combined with FinFET technology could provide a never before seen combination of performance and reliability. These materials have a higher dielectric constant, allowing us to fabricate thicker physical films while achieving an oxide electrical thickness (EOT) equivalent to thinner SiO$_2$ oxides by suppressing quantum mechanical effects. Initially, only the dielectric constant of oxides was considered a deciding criteria. This was however an incorrect approach, as the polarizability of the film depended not only on the materials used; most commonly transition metal oxides like ZrO$_2$, TiO$_2$ and HfO$_2$; but also on the films material properties like its crystallinity and crystallographic phase, electrical properties such as band-gap, chemical stability at the interface and overall thermodynamic

Figure 1: (a) Schematic of a CMOS transistor pair. (b) Image showing Intel’s 45 nm node CMOS using high-k dielectrics and metal-gates on strained silicon FinFET’s.
stability. \[2\] This was the enabling technology that pushed Moore’s law to the 45 nm node and beyond. From then on it was a race to see who could commercialize this technology first. \[4\] Major players like Samsung, TSMC, UMC and Globalfoundries joined the race. \[1\] This however, was not without its own challenges, many high-k dielectrics were considered as potential candidates for commercial device fabrication but a higher polarizability necessarily leads to weaker bonding thereby degrading the electrical stability and breakdown fields achievable. \[2\] This makes many high-k materials with extremely high dielectric constants like $SrTiO_3$ and $Ta_2O_3$ unsuitable for use in CMOS technology. \[2\] Consequently, weak bonding also makes the interface of these materials with silicon highly unstable causing undesired reactions with silicon at the interface. \[2\]

It is therefore helpful to build a set of criteria that the high-k dielectric must satisfy to make it suitable for CMOS applications. \[2\] Promising high-k materials should ideally have a dielectric constant between 10\textsuperscript{−}30 and a band-gap of 5 eV and maintain a band offset of at least 1 eV with the silicon substrate. \[2\] Additionally, to facilitate process feasibility the dielectric should be thermally stable at process temperature exceeding 1000 K for more than 90 sec. \[2\] This leaves the primary candidate for the high-k dielectric to be used as $HfO_2$, having a dielectric constant of \( \sim 25 \), depending on the crystallographic phase, and a relatively large bandgap of 5.7 eV. \[2\] The larger heat of formation of $HfO_2$ compared to $SiO_2$ makes it stable on the substrate at room temperature and device operating temperatures, however at process temperatures forms a $SiO_2$ or $HfSiO_4$ interlayer which degraded device performance. \[2\] At an operating voltage of 1 – 1.5 V the leakage current through a $HfO_2$ gate oxide was several orders of magnitude lower than $SiO_2$ at the same EOT. \[2\]  

In this term paper we look at the various materials science challenges associated with the fabrication of an electrically and thermodynamically stable $HfO_2/Si$ interface and explore the mechanism of interlayer formation. \[2\] \[5\] \[6\] We dive into the thermodynamics and kinetics at the interface and take a critical look at the factors that enable $SiO_2$ formation and how it can be mitigated. \[2\] \[8\] \[9\] \[10\] Finally, we look at the device performance of the gate stack compare it to a device with $SiO_2$ interlayer and analyse how it degrades device performance. \[4\] \[11\] \[12\]
The $HfO_2$—Silicon Interface

The oxide-silicon interface on a MOSFET transistor is a region of critical importance to the electrical performance of the device.\cite{2} \cite{13} \cite{14} The primary reason why silicon is used to fabricate almost all integrated circuits despite being an inferior semiconductor compared to alternatives like germanium, is the ease of growing a chemically and electrically stable oxide on its surface.\cite{2} Using high-k dielectrics as gate oxides is not a simple proposition, and introduces challenges in fabrication and device performance.\cite{2} \cite{15} The $HfO_2$—silicon interface has been extensively studied and the presence of a $SiO_2$ interlayer is well established.\cite{2} \cite{8} \cite{15} The interlayer is primarily amorphous and the trap charge density is dependent on the growth conditions of the $HfO_2$ film.\cite{2} \cite{16} \cite{17} \cite{18} Figure 3 shows the interlayer in a $HfO_2$ film annealed at a temperature of 1025°C for 20 seconds.\cite{8} The interlayer is known to reduce the effective dielectric constant of the film, effectively increasing the EOT of the film.\cite{2} \cite{4} \cite{14} \cite{19} This reduces the gate control on our channel, thus, degrading the performance of our device.\cite{2} \cite{4}

In this section we first take a closer look at the properties of $HfO_2$ and its advantages compared to other high-k dielectrics, after which we take a deeper dive into the thermodynamics of the interface and how it affects the chemical and crystallographic properties of the oxide. We then try to justify the formation of the interlayer and look at the reaction kinetics at play. Finally we try to give an atomistic picture of the underlying mechanism and ways to mitigate interlayer formation.

$HfO_2$

Structural Properties

Group $IV - B$ elements, namely $Hf$, $Zr$, $Ti$ and their oxides have gained a lot of attention in recent years for their use in CMOS technology as high-k dielectrics.\cite{2} \cite{7} Among these Hafnium Oxide ($HfO_2$) shows the most promise due to its high dielectric constant ($k \sim 22 - 25$), large band-gap ($\sim 5.7$ eV), high breakdown field ($3.9 - 6.7$ MV cm$^{-1}$), and thermodynamics stability $\Delta H_{for} = -271Kcal mol^{-1}$.\cite{2} \cite{20} The crystallographic phase of the film plays an impor-
HfO$_2$ forms a monoclinic phase at room temperature, with the Hf atom exhibiting a 7-fold coordination being surrounded by O atoms, as seen in Figure 4. The monoclinic structure has the lowest free energy of formation and the largest volume at room temperature. Upon annealing at 1024°C it undergoes a phase transformation to its tetragonal phase, and a cubic phase which is only formed when annealed at 2422°C.

As deposited thin films of HfO$_2$, however, are mostly polycrystalline often exhibiting multiple crystallographic phases. Cubic and tetragonal phases of HfO$_2$ have been observed along with the monoclinic phase at room temperature, primarily at the interface due to strains. The tetragonal phase also forms a lattice matched interface (mismatch < 5%) with (110) oriented silicon minimizing the dangling bonds at the interface. Films obtained by ALD at 500°C also exhibit an orthorhombic phase, whereas when performed at 325°C weak peaks of the tetragonal phase were also observed. Cubic nano-crystallites of HfO$_2$ were also observed at growth performed at 900°C. These characteristics are closely determined by the processing conditions under which the films are grown, complicating the formation of our gate oxide. Thus, it is preferable to grow perfectly amorphous or single crystalline HfO$_2$ films for CMOS applications. As will be discussed in following sections this is also done to ensure that oxygen diffusion at the interface can be minimized to mitigate the growth of the interlayer.

Electrical Properties

The electrical properties of HfO$_2$ have been well studied in literature. Exhibiting a bandgap of 5.7 eV, and a band-offset of around 1.5 eV with silicon, HfO$_2$ has been determined to be a suitable material for use as a high-k dielectric on silicon for a variety of reasons. The primary reason was noted to be the 4f - 5d hybridization of the hafnium atoms with the 2s and 2p subshells of oxygen, resulting in a valence band consisting of three separate sub bands separated by ionic gaps, namely the O(2d) - Hf(4f, 5d) state, O(2s) - Hf(4f) state and the Hf(5p) state. This results in the aforementioned bandgap and the existence of a light-hole (0.3m$_o$) band and a heavy-hole (8.3m$_o$) band, with the electron effective mass in the range of 0.7m$_o$ - 2m$_o$. The band diagram of monoclinic HfO$_2$ is shown in Figure 5.
The characteristics of oxygen deficient $HfO_2$ is also of great interest to us, primarily due to the fact that it shows a slight increase in the conduction band density of states.\cite{2} \cite{19} \cite{23} Extended defects in general can affect the electronic behaviour of the dielectric film, causing issues with device reliability.\cite{2} \cite{7} \cite{16} \cite{28} \cite{29} DFT studies of the oxygen vacancy diffusion in $HfO_2$ have shown that both neutral and positive vacancies preferentially segregate at grain boundaries, providing percolation path for electrons.\cite{2} \cite{28} \cite{30} Positive vacancies have a diffusion activation energy of $\sim 0.7$ eV, diffusing freely in the bulk until their inevitable accumulation at grain boundaries.\cite{25} At the interface these positive vacancies interact with silicon atoms gaining electrons from them eventually leading to larger defect cluster and interlayer formation.\cite{2} \cite{25} \cite{28}

Composition variation in the $HfO_2$ also has an important impact on the properties of the film at the interface.\cite{2} \cite{19} First principle calculations have revealed the partial occupancy of the $Hf(5d)$ orbitals results in dangling bonds, becoming one of the key defects in the film.

![Figure 5: (a) Band-structure of $m-HfO_2$.\cite{26}](image-a)

![Figure 6: (a) Band-offset of $HfO_2$ with $H$ or $O$ interface passivation compared to no interface passivation.\cite{2} (b) Band alignments in $HfO_2/SlO_x/Si$ heterostructure.\cite{2} (c) Band alignments in $HfO_2/Hf_{1-x}Si_xO_2/Si$ heterostructure.\cite{2} (d) Change in the band alignment due to annealing at different temperature.\cite{2}](image-b)
Figure 7: (a) \( HfO_2 \) films directly deposited on a (110) silicon substrate freshly after \( HF \) treatment. One can notice the clear lack of an oxide interlayer.\(^4\)

...of the culprits for the high band offset upon formation of an interlayer with silicon explored in more detail in the following section.\(^2\) The band offset of the interface is therefore highly dependent on the quality of the interface, with a theoretical range from 2.69 \( eV \) – 3.04 \( eV \) for the conduction band and 1.54\( V \) – 1.89\( V \) for the valence band.\(^2\) With heterostructures such as \( HfO_2/HfSiO_x/Si \) the band offsets are 4.75 \( eV \) for \( SiO_x \) and 2.53 \( eV \) for \( HfO_2 \).\(^2\) Annealing of the interface has been known to affect the band alignment at the interface, primarily due to chemical modification and changes in crystallography.\(^2\)\(^5\)\(^7\) These effects are summarized in Figure 6.\(^2\)

The breakdown characteristics of the oxide determine the reliability of the oxide, and ultimately the fabricated device.\(^2\)\(^11\) The mechanism of breakdown is usually by an avalanche process, beginning at a single weak point; usually a defect; resulting in a weak and localized conduction path between the gate and the substrate, called soft breakdown.\(^2\) This eventually leads to joule heating along the pathway, ultimately leading to hard breakdown.\(^2\) Oxide breakdown is usually described in terms of a Weibull distribution of the form \( F(t) = 1 - \exp\left(-\frac{t}{\alpha}\right) \), with \( \beta \) being the Weibull modulus and \( \alpha \) being the characteristic time.\(^2\) With proper engineering and process optimization an ultra-thin \( HfO_2 \) film, has been shown to meet the performance and reliability criteria for use as gate dielectric.\(^2\)\(^13\) The deposition technique used for fabrication has significant consequences on the crystallographic structure, defect density, interface states and band alignment, further explored in following sections.\(^2\)\(^13\)\(^17\)\(^20\)

**Thermodynamic & Chemical Stability**

In order to understand the impetus for the formation of the \( SiO_2 \) interlayer, one must look at the thermodynamics at the interface.\(^2\)\(^8\) Thermodynamic stability on silicon is of prime importance for any high-k dielectric, as an unstable interface would promote reaction undesired reactions resulting in a degradation of the device performance.\(^2\)\(^8\)\(^32\) In the case of \( HfO_2 \) this primarily occurs in the form of an interlayer oxidation.\(^2\)\(^8\)\(^32\) Table 1 shows the various chemical reactions that can occur at the interface and the Gibbs free-energy associated with those reaction pathways at 0\( K \) and 1000\( K \).\(^8\) Gutowski et al, performed \( DFT \) simulations of the \( ZrO_2/Si \) interface and the \( HfO_2 \) interface at 0\( K \) and at 1000\( K \) and found that...
Table 1: Possible reactions occurring at the high-k silicon interface

| Reaction                                | \(\Delta H_{DFT}\) (0K) | \(\Delta H_{exp}\) (298K) | \(\Delta H_{DFT}\) (1000K) | \(\Delta G_{exp}\) (1000K) |
|-----------------------------------------|--------------------------|----------------------------|-----------------------------|----------------------------|
| H1 \(Si + HfO_2 \rightarrow Hf + SiO_2\) | 227.9 \(KJ/mol\)       | -                          | -                           | -                          |
| H2 \(2Si + HfO_2 \rightarrow HfSi + SiO_2\) | 71.4                     | 92.1                       | -                           | -                          |
| H3 \(3Si + HfO_2 \rightarrow HfSi_2 + SiO_2\) | 68.1                     | -                          | -                           | -                          |
| H4 \(2Si + HfO_2 \rightarrow HfSi + HfSiO_4\) | 59.0                     | -                          | -                           | -                          |
| H5 \(3Si + HfO_2 \rightarrow HfSi_2 + HfSiO_4\) | 55.7                     | -                          | -                           | -                          |
| H6 \(Si + 2HfO_2 \rightarrow Hf + HfSiO_4\) | 215.6                    | -                          | -                           | -                          |
| H7 \(SiO_2 + HfO_2 \rightarrow HfSiO_4\) | -12.4                    | -                          | -                           | -                          |
| Z1 \(Si + ZrO_2 \rightarrow Zr + SiO_2\) | 165.8                    | 186.6                      | 185.6                       | 177.7                      |
| Z2 \(2Si + ZrO_2 \rightarrow ZrSi + SiO_2\) | -8.5                     | -2.4                       | -4.9                        | -11.0                      |
| Z3 \(3Si + ZrO_2 \rightarrow ZrSi_2 + SiO_2\) | -13.5                    | 5.7                        | 1.9                         | 3.3                        |
| Z4 \(2Si + ZrO_2 \rightarrow ZrSi + ZrSiO_4\) | -25.3                    | -27.9                      | -22.0                       | -17.5                      |
| Z5 \(3Si + ZrO_2 \rightarrow ZrSi_2 + ZrSiO_4\) | -30.3                    | -19.8                      | 15.2                        | -3.2                       |
| Z6 \(Si + 2ZrO_2 \rightarrow Zr + ZrSiO_4\) | 149.0                    | 161.1                      | 168.5                       | 171.2                      |
| Z7 \(SiO_2 + ZrO_2 \rightarrow ZrSiO_4\) | -16.8                    | -25.5                      | -17.1                       | -6.5                       |

\(HfO_2\) was more stable at the interface compared to \(ZrO_2\).\[^{[8]}\] He also noted that despite the chemical similarities between hafnium and zirconium, due to the higher heat of formation for \(HfO_2\) compared to \(ZrO_2\) \(\sim 42 \text{kJ/mol}\), it was more stable at the interface.\[^{[10]}\] The lower stability of hafnium silicides compared to zirconium also make it a much more viable option.\[^{[8]}\] One can also clearly observe that the formation energy for \(SiO_2\) interlayer formation at 0K is 227.9 \(\text{kJ/mol}\), incredibly unfavourable.\[^{[8]}\]\[^{[10]}\] That is if \(HfO_2\) is deposited on a perfect substrate without any native oxide, no interlayer should form, as observed in Figure 7, where \(HfO_2\) films were deposited on silicon substrates freshly treated with \(HF\).\[^{[4]}\] It was also observed that the film quality at the interface in such conditions showed considerable nucleation resulting in non uniform coverage that may cause reliability issues.\[^{[4]}\]\[^{[8]}\]\[^{[10]}\] Shin et al, reported a process flow consisting of a \(PVD\) step followed by a \(RTA\) annealing at 750\(^\circ\)C, which showed promise in eliminating the interlayer completely with careful control of the anneal times and oxygen flow concentration, as shown in Figure 9.\[^{[31]}\] \(PVD\) and annealing in presence of \(O_2\) may prove useful as described in the next section.\[^{[31]}\]

However, it must be noted that due to incomplete data, no conclusion can be drawn on the mechanism at work.\[^{[8]}\] A safe bet for the mechanism of formation at the interlayer is that, most substrates are not free of native oxide.\[^{[8]}\] However thin the oxide may be, it can act as a catalyst for growth due to the negative formation energy for reaction H7 forming \(HfSiO_4\).\[^{[8]}\]

No analysis of the thermodynamics of the system can be complete without a discussion of the phase diagram of the system shown in Figure 8.\[^{[31]}\]\[^{[10]}\] Shin et al, calculated the ternary phase diagram and the isopleth of the \(Hf – Si – O\) system from the \(Hf – Si\), \(Si – O\) and \(Hf – O\) binary phase diagrams at 500K and 1000K, as shown.\[^{[10]}\] From this we can see that the \(HfSiO_4\), with \(HfO_2\) and \(SiO_2\) as reference states, becomes favourable above a temperature of 1700K.\[^{[10]}\] It can also be seen that at 1000K \(HfO_2\) is stable on the silicon.

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Figure 8: (a) $\text{HfO}_2 - \text{Si}$ Isopleth (b) Ternary phase diagram of the $\text{Hf} - \text{Si} - \text{O}$ system at 500K \cite{9} (c) Ternary phase diagram of the $\text{Hf} - \text{Si} - \text{O}$ system at 1000K \cite{10} (d) $\text{HfO}_2 - \text{SiO}_2$ binary phase diagram. \cite{10} (e) $\text{Hf} - \text{O}$ binary phase diagram. \cite{10} (f) $\text{Hf} - \text{Si}$ binary phase diagram. \cite{10} (g) $\text{Si} - \text{O}$ binary phase diagram. \cite{10} (h) $p_\text{O}$ vs $T$ phase diagram at the interface. \cite{9}

substrate, also observed experimentally. \cite{9} \cite{11} The silicides are known to decompose in a temperature range of 382K – 670K with the most widely accepted value being 543.5K, way below most processing temperatures. \cite{2} \cite{10} However, when one observes the $\text{HfO}_2 - \text{SiO}_2$ phase diagram in the same temperature range, one can observe that $\text{HfSiO}_4$ is the stable phase, giving credence to our prior proposition for the mechanism of interlayer formation that for a silicate layer to form, the presence of a native oxide layer on the substrate surface is imperative. \cite{8} \cite{10} \cite{11} However, it has been noted that thermodynamic considerations alone cannot explain experimental observations fully. \cite{2} \cite{12} This is because another major factor determining the reactions at the interface is the availability of the reactants, primarily oxygen. \cite{9} \cite{10} Studying the system at different partial pressures therefore is imperative to optimizing any such process. Shin et al, also studies the effects of the local oxygen partial pressure ($p_\text{O}$) on the stability of the phases, when the molar ratio of hafnium to silicon at the interface is set to 1. \cite{9} \cite{10} It can clearly be seen
that under oxygen deficient ambient the growth of the silicide is promoted at the interface. As $p_o$ increases however, the oxide phase becomes stable and is in equilibrium with the silicate, providing us with a narrow but stable window where the interlayer formation can be minimized. Stremmer et al in her extensive review of the subject, investigated in literature the formation of an inter-facial layer in the $HfO_2/\text{Si}$ system under different conditions and found that upon increase of $p_o$ from $10^{-4}$ torr to $10^{-7}$ torr show a significant increase in interlayer thickness. They also propose a mechanism involving the diffusion of $\text{SiO}$ species at the interface and is discussed in detail in the following sections. In the next section we look at the growth of the interlayer and the effect that temperature and other factors have on its thickness and crystallinity.

**Growth Kinetics**

For any scalable process to be implemented at an industrial scale, the effects of process parameters must be extensively studied and optimized. Zhang et al, studied the structural evolution of an as-deposited film of $HfO_2$ films using $PE-ALD$ on a p-type silicon substrate under a $2500 \text{ W O}_2$ plasma in a $N_2$ ambient. It was clearly observed that an interlayer of $\text{SiO}_2$ was formed at the interface between the as-deposited $a-HfO_2$ and silicon, which can be attributed to the previous discussion on thermodynamics. The films were annealed at a temperature of $400^\circ\text{C}$, and one can clearly observe from the $\text{GIXRD}$ data that nano-crystallites of $m-HfO_2$ begin to form which in turn causes an increase in the surface roughness
of the film measured using AFM. HRTEM of the interface also shows that there is no change in the morphology of the interlayer which remains amorphous as shown in Figure 10 and 11. Increasing the anneal temperature to 450°C, one can start observing the transition from a fully amorphous interlayer to a partially crystalline one. A clear crystallization front can be seen propagating from the substrate upwards whose thickness increases with an increase in anneal temperatures. At a 550°C anneal one can observe a complete crystallization of the interfacial layer, which rearranges itself into a cubic phase with a lattice spacing of 2.48Å which increases to 2.56Å at 600°C. This is thought to be influenced by the migration of O atoms from the HfO₂ layer to the interfacial oxide at these temperatures, and is corroborated by the measurements that indicate an oxygen deficient HfO₂ layer and an oxygen rich SiO₂ layer. Such a mechanism is also in agreement with the observation of an increasingly oxygen deficient dielectric as the anneal temperatures are increased. At such temperatures the HfO₂ exhibits a polycrystalline orthorhombic phase with decreasing lattice spacing with increasing anneal temperatures. The maximum dielectric constant of ∼17.2 for the film was obtained at 500°C, with a decrease at higher anneal temperatures. This is presumed to be due to changes in the crystalline arrangement of the interfacial layer which increases in thickness from 1.3 nm to 1.6 nm.

Growth under a reducing ambient has also been studied extensively to prevent the formation of the interlayer, with mixed results. Although an interface that is free of SiO₂ has been achieved this usually comes at the cost of a highly oxygen deficient high-k layer, resulting in degradation of film properties. Primarily, the electrical properties of the film such as breakdown are degraded and there is a thermodynamic shift towards silicide formation, leading to overall chemical instability. Thus, it has become a necessary criteria to allow the oxidation of the high-k layer without oxidizing the underlying silicon. In the next section we shall explore the atomistic kinetics at play and look at primarily the mechanism of oxygen diffusion in the lattice and ways to mitigate it at the interface.

Atomistic Kinetics & Diffusion

To enable the growth of an electrically well behaved HfO₂ film, we have established in the previous sections that the growth needs to be performed in an oxidizing environment. This however comes with a trade-off, growth performed

![Figure 10: HfO₂ films directly deposited on a (110) substrate using PE−ALD subjected to an oxygen plasma at 2500 W annealed at (a) as-deposited (b) 400°C (c) 450°C (d) 500°C (e) 550°C (f) 600°C.](image-url)
Figure 11: (a) GIXRD of the samples annealed at different temperatures. (b) Oxygen composition of the HfO$_2$ layer after being subjected to anneals. (c) AFM of the sample surface after anneal at a temperature of (c) as-deposited (d) 400°C (e) 500°C (f) 600°C.

in an oxygen rich environment will inevitably result in the formation of an interlayer. Depending on the processing parameters used this interlayer might be a HfSiO$_4$ layer or a SiO$_2$ layer, most commonly the latter. To prevent the formation of such a layer while maintain the reliability of the dielectric film grown, it is imperative to understand the mechanism of oxygen diffusion in HfO$_2$. The kinetics of such a diffusion will inevitably involve defects in the dielectric film, therefore these are also explored in this section.

More often that not, HfO$_2$ films grown on silicon substrates are polycrystalline, even as-deposited films that are initially amorphous result in polycrystalline films when subjected to annealing. It is well known that the vacancies in such HfO$_2$ films have a low diffusion activation energy of $\sim 0.7$ eV in the bulk. Such defects however, tend to accumulate at the grain boundaries of the deposited film, resulting in diffusion pathways for incoming oxygen atoms. Such dif-

Figure 12: Schematic depiction of crystalline arrangements of the dielectric film after different anneal treatments at (a) as-deposited to 400°C (b) 450°C to 550°C (c) above 550°C.
fusion behaviour has been studied extensively in literature and has been corroborated by experimental findings.\textsuperscript{[2, 27, 25]} The value for nanoscale $HfO_2$ films grown at $p_o = 200$ mbar is even lower at $\sim 0.52$ eV, with a diffusion coefficient estimated around $\sim 10^{14} \text{ cm}^2\text{s}^{-1}$.\textsuperscript{[28, 25]} First principle studies of positive oxygen vacancies in $HfO_2$ are in excellent agreement with these results.\textsuperscript{[10, 28]} The mechanism therefore is at least partially dependent on the diffusion of oxygen from the oxidizing ambient through positive vacancies that accumulate at the grain boundaries.\textsuperscript{[28, 34]} It has also been proposed that $Si^{4+}$ and $SiO$ intermediate species and their diffusion might also have a role to play at the interface.\textsuperscript{[34]} Under moderately reducing environments, such as those created by forming gas, it has been found that the activity of these species is suppressed resulting in reduced or non-existent interlayer formation.\textsuperscript{[25, 34]} In any case, it is evident that the primary cause for interlayer formation is not only the direct reaction between the $HfO_2$ and silicon at the interface but diffusion of oxygen from the oxidizing ambient through the defects at the grain boundaries to the interface.\textsuperscript{[28, 25]} Now that we can pinpoint the cause of interlayer formation, we are in good shape to come up with measures to mitigate its formation.
Interlayer Prevention

Given the mechanism of the diffusion which forms the oxide interlayer, the primary approach to mitigate its formation is crystal clear. If the positive vacancies at the grain boundaries that enable diffusion are occupied by another less diffusive species during growth, oxygen can react with the $\text{HfO}_2$ fully oxidizing it but will not be able to migrate to the interface. Narayan et al. show this by utilizing nitrogen as the growth ambient which has a tendency to accumulate at the grain boundaries, preventing the reacting oxygen from reaching the interface in $\text{Y}_2\text{O}_3$, with similar studies also done on $\text{HfO}_2$ by other groups. Nitridation has an added benefit of forming oxy-nitrides instead of pure oxides which are well known to have a higher dielectric constant, thus, better $C - V$ performance as seen in Figure 14.

It is also possible to completely eliminate the interlayer by selectively desorbing the $\text{SiO}_2$ on the interface during growth by annealing at above 1000K, this is also known to happen in buried layers. It has also been demonstrated that addition of metallic hafnium at the interface also causes decomposition of the interlayer due to $\text{Hf}$ displacing the $\text{Si}$ in the $\text{SiO}_2$ lattice. It should however be noted that, as long as the thickness of the inter-facial oxide can be controlled, it is usually not completely destroyed due to a couple of reasons. Keeping the interlayer also has advantages that make further growth and processing more convenient.

$\text{HfO}_2$ films grown using ALD are usually grown on substrates with a thin layer of native oxide, this is because the presence of a native oxide provides better adhesion of the precursors to the surface. This acts as a nucleating layer for
the growth.\cite{2,7} It also improves the quality of the interface between the high-k dielectric and the silicon, resulting in improvements in its electrical behaviour.\cite{2,7}

The SiO$_2$/Si interface is well understood and if made of high quality and low defect layer, can help mitigate the lowering of the channel mobility that most high-k dielectrics cause.\cite{7} Recent research also suggests that the electrical behaviour of the interlayer deviates from bulk SiO$_2$, showing a lower reduction in EOT than what was expected.\cite{32}

In the next section we shall take a closer look into the effects that the interlayer has on device performance and critically discuss its advantages and disadvantages.

Effects on CMOS Device Parameters & Performance

The primary motivation for a deeper understanding of the mechanism of interlayer formation in the HfO$_2$ – Si gate stack was to understand its impact on the performance of next generation CMOS devices. A keen understanding of this phenomenon was crucial in weighing trade-off between performance enhancement and process limitations, that is if it was desirable to eliminate the interlayer at the cost of a poorer interface. In this section we look at the impact that the presence of an interlayer has on the CMOS performance factors of the device and the advantages and disadvantages that it entails.

$I_d – V_g$ Characteristics

The primary quantity controlling the overall behaviour of any MOSFET is the capacitance at the gate $C_g$, which ultimately is dependent on the effective thick-
Figure 16: (a) Schematic depiction of mobility reduction mechanisms at different oxide fields. (b) Mobility reduction according to the universal mobility model. (c) Change in the mobility with temperature as a function of field. (d) Mobility reduction as a function of EOT. (e) Electron mobilities in a 3–nm HfO$_2$/Si stack, 3.5–nm HfO$_2$/Si stack and a HfO$_2$/SiO$_2$/Si stack. (f) Added electron mobility as a function of interlayer thickness.

Mobility

The primary reason for avoiding a direct interface between the HfO$_2$ and silicon is not the EOT loss, but also the severe degradation in the mobility of carriers at the channel in such devices. One can clearly see the degradation in the mobility in a HfO$_2$/Si stack compared to a HfO$_2$/SiO$_2$/Si stack, shown in Figure 16. CMOS devices with a SiO$_2$ gate dielectric have a channel mobility close...
to the universal limit derived from Poisson’s equation. Any degradation in the channel mobility is the result of a scattering mechanism, and is accounted for in the effective mobility of the carriers in the channel given by Matthiessen’s rule. As a rule of thumb, at low fields, the scattering is limited by coulombic interactions between carriers and trapped charges. While at moderate and high fields they are primarily limited by phonon interactions and surface roughness respectively. The exact mechanism of this reduction in mobility is hard to pinpoint though several promising contenders exist. Most of the literature agrees that high-k oxides in general have a larger density of trapped charges in them, which in turn results in the carriers experiencing excessive scattering. Another mechanism proposed for the lower mobility in high-k dielectrics is carrier scattering by low frequency polar lattice vibration modes which are also the primary cause of a high dielectric constant. The dilemma arises when one realizes that this is a direct trade-off between EOT and mobility, making it an inevitable compromise. The dependence of the mobility reduction on both the temperature and the thickness of the entire gate stack indicate that both mechanism’s, coulombic and phonon scattering are operative. Devices grown with an interlayer only show a marginally lower mobility than those with SiO$_2$ gate oxides, indicating the remote scattering mechanism at play. Chau et al, suggests that this may be overcome by the screening of interface dipoles by metal electrodes, providing a concrete impetus for metal/high-k stacks. The use of a nitrogen ambient to partially nitride our oxide to create a hybrid HfON/HfO$_2$/Si stack has shown significant improvement in interface quality, leading to a significant increase in mobility.

Threshold Voltage

Another very important parameter that is affected by the formation of an interlayer is the gate potential at which strong inversion is initiated. This is commonly termed the threshold voltage of the device and can be characterized both from the transfer characteristics and the C−V trace. It is immediately noticeable that the threshold of the device without the interlayer is significantly shifted to the left towards 0V and sometimes even negative, indicating ease of strong inversion even at low gate biases. This is usually not desired as it indicates a large flat-band voltage $\sim 1$ V between the electrode and the oxide as seen in Figure 17. This is another reason polysilicon is not the preferred gate electrode in such devices due to the need of a large metal work-function to induce inversion. In silicon, the gate electrode should ideally be able to swing the fermi level by 1.1 eV to be of any use, only possible with metals in high-k devices, and are different depending on whether it is a PMOS or NMOS devices. The presence of an interlayer alleviates this problem a little by lowering the flat-band voltage, presumably by preventing dipole interactions at the interface electrode high-k interface. This effect has been demonstrated clearly by charge pumping experiments, where gate hysteresis in the C−V indicates clear presence of trapped charges as seen in Figure 14. It can also be clearly observed that oxides annealed or grown in a nitrogen ambient do not exhibit this behaviour.
trapped charges, primarily caused due to oxygen defects, $Hf^{3+}$ ions and oxygen interstitials. These can be reduced by repeated annealing of the dielectric in a nitrogen atmosphere or a forming gas ambient. This has the added benefit of compacting dielectric layers grown by ALD, the primary method used in industry for deposition.

Leakage Current

In the case of a $HfO_2/SiO_2/Si$ gate stack with an interlayer it is expected that the gate leakage current would be reduced due to an increase in the thickness of the oxide. However, the physical thickness of the oxide is not the only factor on which the leakage current is dependent, with the homogeneity of the crystalline phase; as well as the trap density playing an important role. Thicker films as expected show a lower leakage current at low biases, although this difference becomes negligible as the bias is increased. The gate current is also largely dependent on the defect density in the material and an appropriate anneal cycle can reduce gate leakage by orders of magnitude, as shown in Figure 17. This is presumed to be due to defect annihilation and passivation of the traps upon annealing. Annealing in a nitrogen ambient has also shown much promise in decreasing the leakage current as shown in Figure 14. This is most likely due to partial nitridation of the $HfO_2$ as well as the interlayer. Increasing the oxygen flow duration during the growth of the high-k layer has also shown promise, most likely due to the annihilation of the positive oxygen vacancies at the grain boundaries, that act as electron conduction pathways leading
Figure 18: (a) Leakage characteristics of films deposited by Thermal ALD.\textsuperscript{[20]} (b) Leakage characteristics of films deposited by PE - ALD.\textsuperscript{[20]} (c) Leakage characteristics of films deposited by magnetron-sputtering as a function of temperature.\textsuperscript{[14]} (d) $C - V$ trace of an amorphous $HfO_2$ film compared to the same film, which is now polycrystalline film after annealing at 700°C.\textsuperscript{[14]} (e) TEM image of the interface in a $TiN/HfO_2/SiO_2 - 2.88 nm /Si$ MOSCAP.\textsuperscript{[14]} (f) Dielectric constant as a function of thickness.\textsuperscript{[40]} (g) Gate leakage characteristics of a 20 nm $HfO_2$ film.\textsuperscript{[40]}

As deposited films also show much better leakage characteristics compared to annealed films, presumably due to their amorphous nature as observed in Figure 18, where films deposited using $PEALD$ showed significantly better switching characteristics than those deposited using Thermal ALD.\textsuperscript{[17] [20]} The degradation in the leakage characteristics of the $PEALD$ films is hypothesized to be due to the formation of polycrystalline domains in a disordered lattice, leading to defect migration and formation of leakage pathways.\textsuperscript{[27] [28]} In contrast the improvement in the polycrystalline films deposited by thermal ALD are presumed to be due to defect annihilation but further evidence is required.\textsuperscript{[14] [20]}

Conclusion
In this term paper we looked at and analysed an in depth mechanism of interlayer formation in the $HfO_2/Si$ system at the interface and provide a thermodynamic
as well as kinetic impetus for such behaviour. The structural and electrical properties of $\text{HfO}_2$ were explored briefly after which thermodynamic argument was presented.\cite{2} It was argued that the relative stability of the deposited $\text{HfO}_2$ and the highly positive Gibbs energy ($\Delta G_0 = 227.9 \text{ KJ mol}^{-1}$) for such a system could not be the root cause, hence motivating an atomistic description of the process. A detailed look at the phase diagram also showed us that the interface was relatively stable up to $\sim 1700K$ much larger than any process temperatures.\cite{2}\cite{10} This points the root cause of interlayer formation to a different source, namely the partial pressure of the oxygen in the process environment.\cite{2}\cite{10} Oxygen is a necessary component in maintaining the integrity of the film, thus, is a necessary evil.\cite{34} It was found that oxygen diffusion along the grain boundaries of the polycrystalline film were the primary culprit.\cite{28} This is primarily due to the positive vacancies in the $\text{HfO}_2$ aiding oxygen diffusion along the grain boundaries.\cite{2}\cite{28} Additionally, the diffusion of the fast $\text{SiO}_2$ species at the interface is also thought to be a contributing factor.\cite{34} This is clearly observed in oxidizing environments where the thickness of the interlayer increases on increased annealing in oxygen. We also explored some of the steps to mitigate this by the growth in a nitrogen ambient preventing diffusion of oxygen and resulting in thinner or non-existent interlayers.\cite{34} Careful annealing was also explored, though briefly.\cite{31}

The industry seems to have agreed that the interlayer is a necessary evil, on one hand, it clearly increases the $EOT$ of the device, on the other hand, it proves a much needed increase in mobility not found in direct contact devices.\cite{4}\cite{11} Such devices also show higher flat band voltage, thus, a rightward shift in their threshold voltage, usually undesired for proper scaling in $\text{CMOS}$ technology.\cite{7}\cite{11} The gate leakage characteristics could also be controlled by controlling the thickness of the interlayer.\cite{7}\cite{22} This is achievable through good process control, leading to a negligible reduction in dielectric constant even for very thin high-k films.\cite{2} In conclusion, the industry has figured out a magic formula to perfect the interface between high-k dielectrics and silicon, and while it is most likely not $\text{HfO}_2$ it is important to remember that $\text{HfO}_2$ was the material that pushed moore’s law into the 21st century making further innovation possible.\cite{11} Current literature seems to be focused on other more exotic hafnium materials like aluminates and lanthanates for future scaling, but to understand the mechanism of interlayer formation is still a fruitful endeavour.\cite{43}

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