Efficient Accelerator for Dilated and Transposed Convolution with Decomposition

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Abstract—Hardware acceleration for dilated and transposed convolution enables real time execution of related tasks like segmentation, but current designs are specific for these convolutional types or suffer from complex control for reconfigurable designs. This paper presents a design that decomposes input or weight for dilated and transposed convolutions respectively to skip redundant computations and thus executes efficiently on existing dense CNN hardware as well. The proposed architecture can cut down 87.8% of the cycle counts to achieve 8.2X speedup over a naive execution for the ENet case.

Index Terms—Hardware design, convolution neural networks (CNNs), dilated convolutional neural networks, transposed convolutional neural networks, segmentation.

I. INTRODUCTION

Convolution neural networks (CNNs) based image segmentation [7], [8] has been widely used in scene understanding, medical purposes, and action recognition during recent years for its significant improvement over traditional approaches. However, the computation of CNNs requires billions of multiplications and accumulations (MACs). Thus, hardware acceleration for CNNs is demanded to provide high parallelism for high throughput to achieve real time execution.

Various hardware accelerators [10]–[15] have been proposed recently. Typical accelerators focus on widely used convolutions with stride one (e.g. 3×3), called dense CNN in this paper [10], [11]. [10] adopts a spatial array architecture and row stationary data flow for classification [1]–[6]. [11] proposes a systolic array architecture with full reconfigurations for different convolutional kernels on classification. [15] uses different hardware units to support CNNs and recurrent neural networks. For acceleration of segmentation, a typical segmentation consists of dilated and transposed convolutions that have many zeros at the weight or input as shown in Fig. 1 which results in sparse CNN and low hardware utilization when naively mapped to a typical dense CNN hardware accelerators. Thus, for accelerators of dilated and transposed convolutions, [12] proposes an accelerator with delay cells to support dilated and transposed convolution in the segmentation. [13] provides a unified systolic array to accelerate different types of convolution. [14] uses a cascading filter structure to support transposed convolutions for generative neural networks [9]. However, most of existing accelerators are tailored for a specific task, which will incur high reconfiguration hardware cost to support different tasks.

To support dilated and transposed convolutions without high reconfiguration costs, this paper proposes to decompose input or weight for dilated and transposed convolutions respectively such that all these convolutions are reduced to normal dense CNN and easily executed on existing dense CNN hardware with no overhead. Applying this flow to a dense CNN design [16] does not need extra logic and can save 97% and 71% of cycle count for dilated and transposed convolutions in ENet [8], respectively.

II. PROPOSED METHOD

A. Overview of Segmentation

Fig. 1 shows the network architecture of segmentation that consists of an encoder, translation, and decoder. The encoder is a typical CNN with convolutions layers and pooling layers to extract high level features. Then these features are further processed with dilated convolutions that use the enlarged kernels with zero insertion to keep feature map size unchanged in the translation part. These feature maps are then upsampled to generate output with the same size as input with the transposed convolutions in the decoder. The transposed convolution enlarges input by inserting zeros between the adjacent input elements and convolves with a normal kernel to generate enlarged output. Both dilated and transposed convolutions contain a large number of zero computations. How to skip...
these zero computations without complex control cost is a challenging task for hardware accelerators.

B. Input Decomposition for Dilated Convolutions

Fig. 2 shows the weight matrices with different dilation rate $D$ (that is, the different number of inserted zeros that between the adjacent weight elements). To avoid these zero computations, we decompose input of dilated convolutions into $(1 + D)^2$ blocks with inspirations by [18]. Each block consists of input elements subsampled by $D$ from original input. Thus, as shown in Fig. 4 the $7 \times 7$ input is decomposed to 4 blocks ($4 \times 4$, $4 \times 3$, $3 \times 4$, and $3 \times 3$) for $D = 1$, or 9 blocks ($3 \times 3$, $3 \times 2$, $3 \times 2$, $2 \times 3$, $2 \times 2$, $2 \times 2$, $2 \times 3$, $2 \times 2$, and $2 \times 2$) for $D = 2$. The decomposed input blocks are then followed by standard convolution (e.g. $3 \times 3$ non-zero weights) to generate independent outputs. This decomposition makes dilated convolutions with any $D$ into dense convolutions and thus is suitable for all dense CNN accelerators.

C. Weight Decomposition for Transposed Convolutions

Fig. 3 shows a transposed convolution example that involves an enlarged $7 \times 7$ input and $3 \times 3$ weight to generate enlarged output. This convolution consists of a lot of zero computations, with only four exceptional cases as shown in Fig. 5. Based on this observations, we can decompose weight to four cases as shown in Fig. 6. These four cases are four corners ($2 \times 2$), two horizontal endpoints ($1 \times 2$), two vertical points ($2 \times 1$), and center ($1 \times 1$). We decompose weight matrices to these four blocks for transposed convolutions to avoid unnecessary zero computations. Thus, the decomposed weight matrices just needs to multiply with normal input directly without zero insertion.

D. Architecture

The proposed method decomposes dilated and transposed convolutions into several dense normal CNN, which can be executed on a dense CNN hardware. For evaluation purpose, we apply this method to our previous proposed dense CNN architecture as shown in Fig. 7 that illustrates a $n \times 3$ MAC array design of one PE block. This design is a typical systolic array type. The PE block has $n$ inputs in the same input column vector broadcasted horizontally, three weights in the same weight column vector broadcasted vertically to optimized for $3 \times 3$ convolutions, and partial multiplication summed along diagonal direction. Finally, the partial sums from PE block will be accumulated to generate output in accumulator.

Fig. 8 shows operations of dilated convolutions on this architecture. The input column vectors in each input block will be broadcasted horizontally and the corresponding weight column vectors will be broadcasted vertically and sequentially. For boundary case, to avoid unnecessary computations due to the zero paddings at the boundary, only two weight column vectors (e.g. $wb$, $wc$ or $wa$, $wb$) are multiplied with input boundary vectors (e.g. $a$, $g$, $b$, and $f$ in $D = 1$ and $a$, $g$, $b$, $e$, $c$, and $f$ in $D = 2$). For other non-boundary input, three weight vectors are multiplied with these input vectors (e.g. $c$, $e$, and $d$ in $D = 1$ and $d$ in $D = 2$). The final output will be stitched together by writing the output to the target address.

Fig. 9 shows the data flow of transposed convolutions to
compute an example as in Fig. 5. For clarity of explanation, we assume 3 blocks with 3×3 PEs in each block for Fig. 9. Thus, the problem is how to schedule the decomposed weight as in Fig. 6 to the architecture as in Fig. 7. Since we have nine input ports for weight (3 blocks with 3×3 PEs), one way is to assign all these nine weights in Fig. 6 to these nine input ports. In this assignment, we will assign weights that needs the same input since each 3×3 PE block shares the same input. Thus, the weight assignments will be as shown in Fig. 9. For this 3×3 input case, it will need three cycles to complete the convolution. In which, the idle blocks at these three cycles are due to the boundary case for this small input.

III. EXPERIMENTAL RESULT

The proposed architecture has been implemented with the TSMC 40nm CMOS technology at 500MHz and simulated with the ENet model trained on the Cityscapes dataset that is resized to 512×512 as our test case.

A. Speedup

Fig. 10 shows the performance enhancement with the proposed method on ENet. Our work can cut down 87.8% of the operations by skipping zero computation. The overall speedup over the ideal dense case can reach up to 8.2X. The ideal dense case computes all convolutions (disregarding zero or not) without considering underlying architecture constraints, which is equivalent to all multiplications and accumulations needed in the convolution. In above speedup, the cycle count of dilated convolutions has been reduced from 85% to only 2% (about 42.5X speedup) due to abundant zero computation saving. A detailed analysis shown in Fig. 11 displayed the trend of higher speedup for larger dilated rate. Fig. 11 also shows the comparison to the ideal sparse case (only compute the nonzero elements). The presented approach has reached over 83% to 98% efficiency compared to the ideal sparse case. The efficiency loss is due to the zero paddings, which has more padded zeros for larger D at the top and bottom of input. The cycle count of transposed convolutions has been reduced from 7% to only 2% (3.5X speedup). A detailed analysis shown in Fig. 12 displays our results very close to the ideal sparse case (up to 99%). The marginal loss is due to the tiled input. However, the cycle counts (9%) of general convolutions in our work is a little higher than the ideal dense case (8%) because utilization of our work is not full in the general convolutions.
Fig. 10. The performance enhancement for our work on ENet [8]. The baseline is cycle counts on the ideal dense case. The number of MACs are the same in our work and the ideal dense case.

Fig. 11. The performance of dilated convolutional layers on ENet [8]. Dilated L1, L2, L3, and L4 represent dilated rate D are 1, 3, 7, and 15, respectively.

B. Implementation and Comparison to Other Designs

Table I shows the implementation result and comparison with other designs dedicated to segmentation [12], [13]. The peak throughput is 168 GOPS for computing all the operations including zeros. With zero skipping, the throughput for ENet is 1377 GOPS. Our work also has much lower area cost than other designs dedicated for segmentation due to the simpler PE structure and controller. The area efficiency is 881 GOPS/mm² for segmentation, which is up to 5.79X higher than [12]. The power efficiency can reach up to 8.88 TOPS/W for segmentation which is 1.13X and 4.77X higher than [12] and [13], respectively. The power efficiency of [12] for dense CNN computation is higher than our work because of its lower bitwidth hardware to attain lower power consumption.

IV. CONCLUSION

This paper proposes hardware efficient execution for dilated and transposed convolutions that decompose input or weight matrices to convert these sparse computations into dense computations. This dense computation form can be executed on a general dense CNN without extra controller overhead. Our work can cut down 87.8% of the cycle count and 8.2X speedup over the ideal dense case. The area efficiency is up to 5.79X higher and the power efficiency is up to 4.77X than other designs for segmentation.

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Table I IMPLEMENTATION RESULT AND COMPARISONS WITH OTHER DESIGNS.

| Technology | 40nm | 65nm | 28nm |
|------------|------|------|------|
| Measurements | Post-layout | Post-layout | Synthesis |
| Precision | 16 fixed | 8 | - |
| On-chip SRAM (KB) | 191 | 220.5 | 114.7 |
| Frequency (MHz) | 500 | 200 | 1449 |
| Throughput (GOPS) | 168 / 1377 | 96 / 639 | 374 |
| Supply Voltage (V) | 0.99 | 1.2 | - |
| Core Area (mm²) | 1.5625 | 6.8 | - |
| Core Power (mW) | 155 | 196 | 201.1 |
| Area efficiency (GOPS/mm²) | 107 / 881 | 14 / 94 | - |
| Power efficiency (TOPS/W) | 1.08 / 8.88 | 0.49 / 3.26 | 1.86 |
| Technology scaling (process V) | 0.40 \times 0.99V | 0.79 \times 0.99V | 1.08 \times 0.99V |
| Normalized power efficiency = power efficiency \times \frac{process V}{40nm V} \times \frac{Voltage}{0.99V} | 0.59 | 0.49 | 0.99 |
| The peak throughput for computing all the operations including zeros. | - | - | - |
| The logical throughput with zero skipping on ENet [8] [12]. | - | - | - |
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