Theoretical Analysis of Multi Integrating RX Front-Ends for Lossy Broad-Band Channels

Antroy Roy Chowdhury, Shovan Maity, Student Member, IEEE and Shreyas Sen, Senior Member, IEEE

Abstract—In this paper, we present a theoretical analysis of different integrating front-ends employed in broad-band communications through lossy channels. Time-domain receivers for broad-band communication typically deal with large integrated noise due to its high bandwidth of operation. However, unlike traditional wireline systems that are typically not noise-limited, channels with high channel-loss render the input signal swing to be very small imposing several challenges in RX design as the circuits operate in the noise-limited regime. This simultaneous high integrated noise and low signal-swing limits the maximum achievable data-rate for a target bit-error-rate (BER) and deteriorates the energy-efficiency of the RX. In this work, transient, noise and gain performance of different standard signaling blocks have been obtained with closed-form expressions and are validated through spice-simulations. Multi-integrator cascade has been proposed which provides significant gain with relatively lower power consumption than the standard gain elements. Also, maximum achievable data-rate and optimum energy efficiency for different channel losses have been obtained theoretically for different architectures revealing their advantages and limitations. All the pertaining circuits have been designed in 65 nm CMOS process with a 1 V supply voltage.

Index Terms—Current integrating amplifier, broad-band communication, noise, channel-loss, wireline-like channels

I. INTRODUCTION

As different communication standards are emerging, the primary focus of any type of communication remains on the optimization of energy-efficiency, i.e the energy spent on transmitting a single bit, as well as maximizing the data-rate. In wireless communication, due to the practical form-factor of antennas and FCC limitations of usable frequency bands, modulation or frequency up-conversion in the TX followed by a demodulation or frequency down-conversion in the RX are of absolute necessity. Due to deployment of modulation/demodulation schemes and high channel loss (> 80 dB) of wireless channel, the power consumption is sufficiently high in wireless transceivers. In popular wireless techniques such as Wi-Fi, near-field communication (NFC), Zigbee, BTLE etc. the best energy-efficiency that can be achieved is close to few nJ/bit [1]. However, in wireline communication through electrical links, availability of a broad-band for transmission and significantly lower channel loss reduce the transceiver energy consumption drastically and increase the data-rate. For typical wireline applications such as backplane, ethernet, USB etc. the energy efficiency can be reduced to as low as ≈ 1 – 10 pJ/bit [2], [3], [4]. A wireline channel being low-pass with a very small low-frequency channel loss, while designing transceivers for wireline links, major emphasis is given in mitigation of inter-symbol interference (ISI) to increase the data-rate. The reason behind this is that the data-rate or speed limitation primarily comes from ISI and not from the integrated noise. Hence, analyzing the noise performance and gain provided by different signaling blocks and their implications on the overall performance of different RX architectures are largely overlooked. However, for applications which utilize broad-band channels with sufficiently large low frequency channel loss ([5]–[11]), transmitted signal gets highly attenuated which drastically degrades the BER (bit-error-rate) performance of the RX. Employing broad-band communication in such situation, even though an energy-efficient solution, necessitates the need for analyzing the noise and gain performance of different signaling blocks which essentially limits the maximum achievable data-rate.

In this work, we explore different plausible receiver (RX) architectures that can be employed for broad-band communication through lossy wireline-like channels (with channel loss > 20 dB over all frequencies, unlike the traditional wireline channels such as FR4 traces or cables). An extensive theoretical analysis of different signaling blocks, such as sampler, integrator and LNA, typically used in low-loss wireline link RXs has been carried out to find their suitability and performance while employed for high-loss applications. A theory for finding closed-form expressions for the input-referred noise of the sampler and integrator has been delineated. Multi-integrator cascades are proposed as low-power gain elements. An accurate expression for the gain of integrators has been derived and extended for multi-integrator cascades. Based on these analyses, optimum performances of different RX architectures are found as a function of the channel loss.

Rest of the paper is organized as follows: Section II provides the motivation behind the work explaining few typical examples of lossy channels which employ broad-band communication. Section III expounds different plausible RX architectures suitable for these kind of channels. Section IV deals with deriving closed-form equations and a rigorous performance analysis of different signaling blocks used in the RX architectures in terms of gain, integrated noise and power consumption. Section V utilizes the analyses of section IV to find out the performance of different RX architectures with different channel loss followed by their comparison in section VI. Section VII concludes the paper.

II. MOTIVATION: BROAD-BAND COMMUNICATION THROUGH LOSSY WIRELINE-LIKE CHANNELS

Considering the advantages of energy-efficient wireline techniques over wireless, several wireline-like communication techniques have evolved for short distance communications.
These include mm-scale proximity communication ([5, 6]) and meter-scale human-body communication ([7]-[11]). The major difference between the wireline and wireline-like channels arises from the significant loss provided by the wireline-like channels. Following are the descriptions of two major applications where wireline-like channels are being used for data-communication between devices.

A. mm-Scale Proximity Communication

In this type of communication, two devices in close proximity to each other communicate through capacitive coupling as shown in Fig. 1. Here the channel behaves like a simple capacitive divider giving a maximally flat frequency response and hence, a proximity connector can utilize wireline-like baseband signalling and mixed-signal processing for energy-efficient implementation. As the channel behaves as a capacitive divider, the channel loss or coupling loss largely depends on the coupler plate dimensions and the separation between the couplers. For a fixed coupler size, the coupling loss increases with increase in the coupler separation. [5] demonstrates a transceiver with energy efficiency ≈ 4 pJ/bit for 19 dB coupling loss and a maximum achievable coupler separation of 0.8 mm satisfying a BER of 10−12. However, with increase in coupler separation and hence the coupler loss (Fig. 1(c)), the BER increases rapidly as the total noise contributed by different sources become comparable to the signal. Hence, analysis of different conventional RX architectures, finding their limits of operation as the channel loss increases and exploring new RX architectures suitable for channels with sufficiently high loss find their role pretty important.

B. Human-Body Communication (HBC)

Another emerging example of broadband communication where channel loss turns out to be critical is human-body communication shown in Fig. 2. In this particular type of communication two wearable devices placed on two different locations of the human-body communicate among themselves by utilizing the conductivity property of the human body and using it as the communication medium. Capacitive HBC ([12], [13]) is the most widely used form of HBC, where the signal is coupled in a single ended manner in the transmitter end and also received in a similar single ended way at the receiver end. In this scenario, the body provides the forward path of communication between the devices. The return path is formed through the parasitic capacitance between the ground planes of the transmitter and receiver. The overall channel response is strongly dependent on the parasitic return path capacitance. The other primary factor, which determines the channel response, is the termination on the receiver end. A 50Ω termination at the receiver end results in high loss at low frequencies and hence a high pass response. However, a high impedance capacitive termination at the receiver end enables a flat-band response with low frequency roll off at frequencies <100kHz. For a high impedance termination, the channel loss is dependent on the ratio of the termination capacitance and the return path capacitance. However, for typical values of parameters the channel loss varies from 40-60 dB making it
a lossy channel which is flat-band until frequencies as low as 100kHz.

Note that, for the above mentioned two applications or in general any broad-band communication technique where the flat-band or low-frequency channel loss is sufficiently high (> 20 dB), the transmitted signal gets highly attenuated while reaching the RX front-end. Hence, voltage mode signaling with rail-to-rail transmitted signal swing should be utilized as opposed to current-mode signaling. Also, due to the low signal swing at the input of the RX, a simple non-return to zero (NRZ) modulation scheme shows superior BER performance over multi-level schemes such as four-level pulse amplitude modulation (PAM-4), duobinary etc. In NRZ communication, the most important component of a RX is the clocked comparator or sampler which distinguishes between the two levels of NRZ data and detects the transmitted bit. In both the aforementioned applications, integrating front-end has been utilized for serving specific purposes associated with the particular type of channel, i.e. to deal with self-resonance frequency (SRF) in proximity communication[6] and cancelling environmental interference in human-body communication[7]. However, the fact that current-integrating amplifiers or integrators can be utilized as gain elements with sufficiently lower power consumption, remains relatively unexplored in literature with a dearth of closed-form equations capturing the same. The following analyses of different RX architectures deal with an extensive analysis of different signaling blocks followed by finding the best achievable performances of different architectures on increasing the channel loss. Also, for simplifying the analysis, high-frequency roll-off (if any) of the wireline-like channel has been ignored which alleviates the need of any equalizer circuit in the RX front-end.

III. ARCHITECTURAL CHOICES

As mentioned in the previous section, for broad-band NRZ communication, a sampler at the RX front-end samples the received signal at each clock-edge and converts it into full-swing bit-pattern. Hence, a sampler or clocked comparator serves as the simplest RX. However, for practical samplers (e.g. a strongARM latch[14]) the sampling frequency is limited by the input signal swing which decreases with increase in channel-loss. Also, for applications with very high channel-loss, input referred noise of the sampler may become comparable with the signal and can degrade the bit-error rate (BER) drastically. A low-noise amplifier (LNA) can be used before the sampler which serves two important purposes, i.e. it amplifies the RX input signal and exhibits significantly lower input referred noise. However, being a continuous time amplifier its power consumption is large and increases linearly with the required bandwidth. A current-integrating amplifier or integrator[15], [16], [17], on the other hand can provide gain comparable to an LNA with lower power consumption but at the cost of relatively higher input-referred noise.

Fig. 3 summarizes the typical performance of all these blocks (in 65 nm CMOS) in terms of gain, input referred noise and power consumption for 1 Gbps data rate (i.e. 1 GHz clock frequency). Various RX front-end topology based on these three key signaling blocks are shown in Fig. 4 with the sampler as a mandatory part in each topology. In the following sections detailed analyses for all these signaling blocks are done and optimum performance of each topology for different channel losses are estimated.

IV. ANALYSIS OF SIGNALING BLOCKS

A. Sampler or clocked comparator

StrongARM latch is the most common type of sampler widely used in different applications including wireless receivers, analog-to-digital converters and memory bit-line detectors. The reason for its widespread popularity is zero static power consumption and rail-to-rail output swing.

The strongARM latch shown in Fig. 5 has four phases of operation[18]. In the reset phase (phase-I), $CLK$ is low and nodes $P, Q, X$ and $Y$ are pre-charged to $V_{DD}$. When
the strongARM latch for applications with high channel loss where input differential voltage can be quite small, one must carefully consider the dependencies of duration of each phase over the input voltage and also the total input referred noise of the strongARM latch.

1) Transient performance (Latching time consideration): Fig. 6(a) shows the transient behaviour of the strongARM latch in the sensing phase (i.e. when CLK becomes high). From the analyses in [19] and [20], duration of different phases can be expressed as

\[ t_a = \frac{2C_{P,Q}V_{TH,3,4}}{I_O} \]  
\[ t_o = \frac{2C_{X,Y}V_{TH,5,6}}{I_O} \]  
\[ t_{latch} = \frac{C_{X,Y}}{g_{m,latch}} \ln \left( \frac{1}{V_{TH,5,6}} \sqrt{\frac{I_O}{2\beta}} \frac{\Delta V_{latch}}{\Delta V_{IN}} \right) \]

where \( I_O = g_{m1,2}V_{out,1,2}/2 \) is the quiescent current provided by \( M_7 \) once CLK goes high. \( g_{m,latch} \) is the sum of the transconductances of \( M_3 \) and \( M_5 \) in the regeneration or latching phase (i.e. phase-III), \( \beta \) is the transconductance parameter of \( M_1 \) and \( M_2 \) and \( \Delta V_{IN} \) is the input differential voltage to the strongARM latch. Note that the regeneration phase is characterized by \( t_{latch} \) which in turn is governed by \( \Delta V_{latch} \) as shown in [19]. As the output of the strongARM latch needs to be sampled by a D-flip flop before the reset phase starts, sufficient time should be provided in the regeneration phase so that the differential outputs can reach \( V_{DD} \) and GND respectively. Considering this fact, duration of phase-(III+IV) is conservatively chosen to be \( 3 \times (t_a + t_o + t_{latch}) \) which gives the minimum time period of CLK to be

\[ T_{CLK,min} = \frac{1}{f_{CLK,max}} = 6(t_a + t_o + t_{latch}) \]

From eq. (3), it can be seen that as the input differential voltage \( \Delta V_{IN} \) reduces, the maximum operating frequency of the strongARM latch decreases logarithmically. Fig. 6(b) shows the variation of maximum operating frequency \( f_{CLK,max} \) with \( \Delta V_{IN} \) obtained by extracting all the parameters in eq. (1)-(3) for a typical design in 65 nm CMOS technology. As can be seen, for very small \( \Delta V_{IN} \approx 1 \text{ mV} \), \( f_{CLK,max} \) can be as small as 0.8 GHz and for larger \( \Delta V_{IN} \approx 100 \text{ mV} \), the value reaches up to 3.3 GHz. From Fig. 6(b), it may seem that with signal amplitude of even a few \( \mu \text{V} \), the strongARM latch can be operated at a speed close to 1 GHz, but practically for sub-mV signal swing, final decision will be significantly affected by the internal noise of strongARM latch. Hence, it is important to find out the total input referred noise which is addressed in the following subsection.

2) Noise performance (SNR consideration): It is interesting to note that in the reset phase, the pre-charge action of the switches \( (S_1 - S_2) \) nullifies effect of all the noise contributed by different transistors. It is when the CLK goes high, that the noise contributions of different transistors come into picture. Moreover, most of the input referred noise originates from \( M_1 \) and \( M_2 \) in the amplification phase [20] because all other

CLK goes high, amplification phase begins and the input differential voltage at the inputs of \( M_1 \) and \( M_2 \) gets converted to differential drain current which is integrated at the parasitic capacitances at nodes \( P \) and \( Q \) amplifying the input signal until \( V_P \) and \( V_Q \) drop to \( V_{DD} - V_{TH,N} \) (Fig. 6(a)). At this point \( M_3 \) and \( M_4 \) are turned on, output nodes \( X \) and \( Y \) start discharging and the circuit enters into the third phase with continuing amplification by \( M_1 \) and \( M_2 \) and a little regenerative gain provided by \( M_3 \) and \( M_4 \). The final regeneration phase begins when nodes \( X \) and \( Y \) drop below \( V_{DD} - V_{TH,F} \) turning \( M_5 \) and \( M_6 \) on. To understand the timing performance of

Fig. 5. Widely used strongARM latch topology[13]

![strongARM latch topology](image)

Fig. 6. (a) Transient behaviour of a strongARM latch in the sensing phase (i.e. phase-II,III and IV) showing the transition between different phases of operation, (b) Variation of the maximum operation frequency of strongARM latch with input voltage

![transient behaviour](image)

![frequency variation](image)
transistors start acting after phase-II when a significant gain has already accrued between nodes P and Q which then gets regenerated in rest of the phases. Hence, the input referred noise of strongARM latch would be simply the output referred noise at the end of amplification phase divided by the gain of the amplification phase given by $g_{n1,2}a_a/C_{P,Q}$. In [21], a stochastic analysis of this noise has been done. Here we show a time domain analysis based on the ergodicity property of thermal noise.

Note that in the amplification phase, as $M_3$ and $M_4$ are turned off, strongARM latch behaves like an integrator, integrating the drain currents of $M_1$ and $M_2$ over the parasitic capacitance $C_P$ and $C_Q$ at nodes $P$ and $Q$ respectively. Hence, assuming the output resistance at nodes $P, Q$ to be very large, the final differential output referred noise at the end of the amplification phase can be found by integrating the differential channel noise current $i_n$ (whose PSD $= 8KTg_{n1,2}$) of $M_1$ and $M_2$ for a duration of $t_a$. This gives the final noise voltage to be

$$V_{n,O} = \frac{1}{C_{P,Q}} \int_0^{t_a} i_n(t)\,dt \quad (5)$$

To evaluate this integral, let us first assume $i_n(t)$ to be a sine wave with amplitude $A$, frequency $f$ and initial phase $\phi$, i.e. $i_n(t) = A\sin(2\pi ft + \phi)$. For this simplest scenario, $V_{n,O}$ can be found out to be

$$V_{n,O} = \frac{A}{2\pi f C_{P,Q}} \int_0^{t_a} \left[\cos(\phi) - \cos(2\pi ft_a + \phi)\right] \, dt = \frac{A}{C_{P,Q}} \cdot TF_{\phi}(f) \quad (6)$$

From eq. (6), it can be seen that if $i_n(t)$ be a sinusoid with frequency $f$ and initial phase $\phi$, result of the integral in eq. (5) would be $TF_{\phi}(f)$ times its amplitude. But in reality, $i_n(t)$ in the time interval $0$ to $t_a$, contains all the frequency components and hence different frequency components would have different multiplication factor depending on their initial phases. Hence, the final noise voltage can be found by summing the contributions of all the frequencies present in $i_n(t)$. Fig. 7 shows the plot of $TF_{\phi}(f)$ for 5 different values of $\phi$. The rms value of the component of $i_n(t)$ obtained by passing it through a band-pass filter of bandwidth $\Delta f$ centered around frequency $f$ can be given by $\sqrt{8KT\gamma g_{n1,2} \Delta f}$. But as the initial phase corresponding to this component at frequency $f$ can eventually be anything, by pessimistic assumption we consider the multiplication factor to be $\max(TF_{\phi}(f) : \phi \in [0:2\pi])$ which is essentially the envelop $\left(TF_{env}(f)\right)$ of all the curves governed by different $\phi$. Hence, considering the noise contribution of all the components in $i_n$, the final rms noise voltage square ($V_{n,O}^2$) can be expressed as

$$\begin{align*}
V_{n,O}^2 &= \sum_f \left(\frac{\sqrt{8KT\gamma g_{n1,2} \Delta f}}{C_{P,Q}} \times TF_{env}(f)\right)^2 \\
&= \frac{8KT\gamma g_{n1,2}}{C_{P,Q}^2} \times \int_0^\infty TF_{env}^2(f)\,df
\end{align*} \quad (7)$$

Hence, the input referred noise can be given by

$$V_{n,in}^2 = V_{n,O}^2 / \left(\frac{g_{n1,2}a_a}{C_{P,Q}}\right)^2 = \frac{8KT\gamma}{g_{n1,2}a_a} \times \int_0^\infty TF_{env}^2(f)\,df \quad (8)$$

The integral in eq. (8) can be numerically evaluated to be $t_a/2$ which gives the final input referred noise expression as

$$V_{n,in}^2 = \frac{4KT\gamma}{g_{n1,2}a_a} \quad (9)$$

which exactly matches with the stochastic analysis result in [21]. Moreover, on replacing $t_a$ with (1) and substituting the value of $I_o$ one gets the expression for input referred noise as

$$V_{n,in}^2 = M \frac{KT}{C_{P,Q}} \quad (10)$$

where $M = \gamma \nu T H_{3,4}/V_{oh}$. Note that, the noise term has an usual $KT/C$-form with an additional factor-$M$. To validate this theory, input referred noise of strongARM latch has been obtained in spice simulation following the method described in [20]. Fig. 8 compares the spice result with the theoretical expression plotted by extracting transistor parameters in 65 nm CMOS.
B. Low noise amplifier

As mentioned in section III, a low noise amplifier serves two important purposes: i) it provides a gain to the inbound signal and ii) offers much lower input referred noise. The most commonly used broadband topology of a low-noise amplifier (LNA) is shown in Fig. 9, where \( R_B \) is a large resistor (realized by off-transistor in this case). The mid-band gain of this LNA can be given by

\[
A_{LNA} = (g_{m1} + g_{m2})(r_{o1}||r_{o2}) \tag{11}
\]

where \( g_{m1,2} \) is the transconductance of \( M_{1,2} \) and \( r_{o1,2} \) is its drain to source resistance. Hence the gain of the LNA is solely determined by the intrinsic gains of transistors \( M_1 \) and \( M_2 \). Also, the input referred noise of this LNA can be expressed as

\[
V_{n,IN,LNA} = \sqrt{\frac{4kT\gamma}{g_{m1} + g_{m2}}} \times B \tag{12}
\]

where \( B \) is the bandwidth of the LNA which depends on the bias current \( I_{bias} \) and effective load capacitance. Note that the bandwidth requirement of the LNA comes from the input data-rate, i.e. the bandwidth of the LNA should be larger than or equal to the data rate to avoid any signal distortion causing inter-symbol interference (ISI). For the analysis in Fig. 10, a typical design setup in 65 nm CMOS is used where sizes of the transistors are kept constant (width of \( M_1 \) is 24 \( \mu \)m and that of \( M_2 \) is 48 \( \mu \)m) and an external load capacitance \( C_L \) of 10 fF has been chosen. Fig. 10(a) shows the minimum \( I_{bias} \) required for the LNA as a function of its bandwidth. It is important to note that as the bandwidth requirement of the LNA goes down, operating region of the transistors moves from above-\( V_T \) to weak inversion and finally to depletion region. And hence, the power consumption goes down more-or-less linearly with reduction in target bandwidth. Fig. 10(b) shows the variation of the mid-band gain of the LNA with bandwidth, assuming the minimum bias current in the LNA for each target bandwidth. Note that for target bandwidths where transistors are in above-\( V_T \) region of operation, gain increases with reduction in bias current as \( g_m \) is proportional to \( \sqrt{I_{bias}} \) and \( r_o \) is inversely proportional to \( I_{bias} \) in this region. When the transistors go to weak inversion, \( g_m \) becomes proportional to \( I_{bias} \) and hence, the gain remains almost constant. Finally, in the depletion region gain falls with reduction in current as \( r_o \) becomes comparable to \( R_B \). On the other hand, the input referred noise (in Fig. 10(c)) behaves exactly the opposite to the gain, for different target bandwidths, as expected from the noise expression in eq. (12). On comparing the noise performance of strongARM latch in Fig. 8 to that of the LNA in Fig. 10(c) shows significantly lower input referred noise for the LNA. This, together with the gain plot in Fig. 10(b) substantiate the use of the LNA before the sampler for achieving higher data rate in applications with high channel loss.

C. Integrating amplifier or integrator

An integrating amplifier can be used in the RX front-end to provide gain to the received signal before sampling with significantly lower power consumption than an LNA. Fig. 11a shows the circuit diagram of the integrator which utilizes pre-charging loads. When \( CLK \) is low, the PMOS switches are on, which pre-charge the output nodes to \( V_{DD} \). As \( CLK \) goes high, the output nodes start discharging and depending on the input voltage difference, a finite voltage difference is created between the output nodes which is then sampled by the sampler at the end of integration period. Assuming large output resistance, the ratio of the output and input voltage difference or the voltage gain of the integrator can be expressed as

\[
A_{int} = \frac{g_{m1,2}T_{int}}{C_L} \tag{13}
\]

where \( g_{m1,2} \) is the transconductance of \( M_{1,2} \), \( T_{int} \) is the period of integration which equals to half of the clock period and \( C_L \) is the equivalent load capacitor at the output nodes. Note that the integrator senses the input data only in the integration phase and hence, for clock frequency same as the data-rate, the integrator integrates the input data for only half the bit-period. However, an half-rate architecture [22] can be used where two parallel integrators work on complementary clock signals with clock frequency as half the data-rate.

It is important to observe that as the integrator output is fed to the sampler realized by a strongARM latch, the common mode voltage at the output nodes at the end of integration phase should be high enough for proper operation of the strongARM latch. [19] shows that 0.7\( V_{DD} \) is the optimum input common mode voltage for the strongARM latch in terms of speed and yield. However, for 65 nm CMOS, we found that the input common mode voltage can go down to 0.6\( V_{DD} \) without degrading the speed and yield significantly. With this observation, the maximum bias current \( (I_{B,max}) \) in the integrator for \( V_{DD} = 1V \) can be expressed as

\[
I_{B,max} = \frac{(0.4V_{DD})(2C_L)}{T_{int}} = \frac{0.8C_L}{T_{int}} \tag{14}
\]

Fig. 12 shows the variation of \( I_{B,max} \) with clock frequency for \( C_L = 4 \) fF, which gives \( I_{B,max} \approx 20\mu A \) for a 1 GHz clock frequency. The common-mode droop problem associated with the integrator in Fig. 11(a) is handled in [23] by a separate common-mode boosting circuit using capacitive coupling, whereas [24] addresses the same by adding a common-mode current during the integration phase. In [17] the output common-mode voltage is kept constant by using current-source loads and a common-mode feedback (CMFB) circuit
Fig. 10. (a) Minimum bias current required for the LNA in Fig. 9 for different target bandwidths (b) gain of the LNA for different target bandwidths with minimum bias current (c) input referred noise of the LNA for different target bandwidths with minimum bias current.

Fig. 11. (a) Integrator based on pre-charging load [22], (b) modified integrator based on current-source load with common-mode feedback [17], (c) comparison of output waveform for both the integrators. Output common-mode voltage of the one with pre-charging loads keeps on decreasing, whereas the other one has a constant common-mode voltage.

as shown in Fig. 11(b). The corresponding output waveform is shown in Fig. 11(c).

From the gain expression in eq. (13) it might seem that the gain of the integrator in Fig. 11(a) can go very large for lower clock frequency as $g_{m1,2} \propto \sqrt{I_{B,\text{max}}}$ and $T_{\text{int}} \propto 1/I_{B,\text{max}}$. But practically, the gain will be different from that given by eq. (13) due to the presence of finite output resistance of the integrator. In the following portion, we derive an accurate expression for the gain of the integrator considering the drain to source resistance of $M_{1,2}$ in the integration phase.

In the integration phase, the circuit in Fig. 11(a) can be simplified as shown in Fig. 13 where $i(t) = g_{m1,2} v_{\text{in}}$, $R$ is the drain to source resistance of $M_{1,2}$ and $C_L$ is the load capacitance at the output nodes. Now, from Kirchhoff’s current law, we can write

$$i(t) = \frac{v_c(t)}{R} + C_L \frac{dv_c(t)}{dt} \quad (15)$$

on solving this differential equation and applying the initial pre-charge condition $v_c(0) = 0$, we can write

$$v_c(t) = \frac{e^{t/RCL}}{C_L} \int_0^t e^{-\tau/RCL} i(\tau)d\tau \quad (16)$$

finally substituting $i(\tau)$ with $g_{m1,2} v_{\text{in}}$ we can express the gain.
for a clock frequency \(f_{CLK}\) of 1 GHz. It can be seen, there is an excellent match between the modified theoretical expression and spice simulation. Note from Fig. [14] that, as the bias current \(I_B\) reduces for a fixed \(T_{int}\), value of \(R\) increases (as \(R \propto 1/I_B\)) and hence the two gain expressions give same results for very low \(I_B\). Now, for a particular \(f_{CLK}\), as the gain increases with \(I_B\), the maximum gain can be achieved with \(I_B = I_{B,max}\) given by eq. (14). Also, considering the fact that \(R = \frac{2}{\lambda I_B}\) (\(\lambda\) being the channel length modulation parameter) for \(I_B = I_{B,max}\) eq. (17) becomes

\[
A_{int,max} = g_{m1,2}R\left(1 - e^{-0.4\lambda}\right)
\]  

(18)

Hence, it can be concluded that the maximum gain of the integrator in Fig. [11]a for a particular clock frequency \((f_{CLK})\), is mostly governed by the intrinsic gain of the transistors \(M_{1,2}\) and it can not be made very high for lower clock frequencies. Fig. [15] shows the variation of the maximum gain \(A_{int,max}\) with clock frequency. Note that, the difference in gains of the integrators with pre-charging load (Fig. [11]a) and current-source load (Fig. [11]b)) arises from the difference in their output resistances \((R)\). For the same bias current, \(I_B\), the output resistance of the later one is half of the output resistance of the former assuming the same channel-length modulation parameter \((\lambda)\) for both PMOS and NMOS devices. This results in a lower gain for the current-source load based integrator compared to the former for the same bias current. Also, as the output common-mode voltage of the current-source load based integrator is constant, the bias current doesn’t impose any constraint over the maximum achievable gain. However, note from eq. (17) that the maximum achievable gain for the current-source based integrator for a fixed \(T_{int}\) (and hence \(f_{CLK}\)) can not exceed \(g_{m1,2}R\) which is half of the intrinsic gain of \(M_{1,2}\). Fig. [16] shows the variation of the gain of the current-source load based integrator with bias current, \(I_B\) for different clock frequencies \((f_{CLK})\). As it can be seen, the gain increases with increase in \(I_B\) and finally converges with \(g_{m1,2}R\). Also, the minimum \(I_B\) required to converge with \(g_{m1,2}R\) decreases with decrease in \(f_{CLK}\).

Coming to the noise performance of the integrator, note that the theory of input referred noise described in section IV.A.2 directly applies to the integrator in Fig. [11]a) with \(t_a\) being replaced by \(T_{int}\). Hence, the input referred noise of the integrator with pre-charging load can be given as

\[
V_{n,in} = \sqrt{\frac{4KT\gamma}{g_{m1,2}T_{int}}} \tag{19}
\]

However, for the current-source load based integrator, the PMOS current sources \(M_3\) and \(M_4\) will also contribute to the input referred noise and it can be shown that the overall input referred noise in this case can be expressed as

\[
V_{n,in} = \sqrt{\frac{4KT\gamma}{g_{m1,2}T_{int}}} \left(1 + \frac{g_{m3,4}}{g_{m1,2}}\right) \tag{20}
\]

Fig. [17] shows the variation of \(V_{n,in}\) with clock frequency for both type of integrators. Finally, it can be concluded that performance of the pre-charging load based integrator is superior to that of the current-source based integrator in
terms of gain, noise performance and power consumption. However, applications where the data rate (and hence the clock frequency) varies widely making a stable output common-mode voltage of the integrator an absolute necessity, the current-source based integrator turns out to be more effective. In all other practical applications, the pre-charging load based integrator gives superior performance. In this work, the pre-charging load based integrator has been used to analyze the performance of all the RX architectures.

D. Multi-integrator cascade: Cascading multiple integrators

As already seen, a single integrator can typically provide a gain ranging from 4.5 – 7 for all frequencies of operation. It will be interesting to see whether the gain can be further enhanced by cascading multiple integrators operating with the same clock signal as shown in Fig. 18. To understand the behavior of the cascaded integrators in Fig. 18 let us for the time being ignore the effect of the output resistance. Hence output of the first integrator and the gain can be given by

\[ v_{out,1}(t) = \int_0^t K_i v_{in} dt = K_i v_{in} t \]  

(21)

\[ A_{int,1} = K_i T_{int} \]  

(22)

where \( K_i = g_{m1,2}/C_L \). Similarly, output of the second stage and the combined gain of 2 cascaded integrators can be expressed as

\[ v_{out,2}(t) = \int_0^t K_i (K_i v_{in} t) dt = \frac{K_i^2 v_{in} t^2}{2} \]  

(23)

\[ A_{int,2} = \frac{K_i^2 T_{int}^2}{2} = A_{int,1} \times \frac{K_i T_{int}}{2} \]  

(24)

Hence, from eq. (24) it can be observed that in order that gain of 2 cascaded integrators (\( A_{int,2} \)) be larger than that of a single integrator, gain of a single integrator (= \( K_i T_{int} \)) must be greater than 2. Proceeding in the same way it can be shown that the overall gain of \( N \)-cascaded integrators would be

\[ A_{int,N} = \frac{K_i^N T_{int}^N}{N!} = A_{int,N-1} \times \frac{K_i T_{int}}{N} \]  

(25)

This is an important result which shows that for a fixed clock frequency (or, equivalently fixed \( T_{int} \)) and with single integrator gain \( A \), cascading \( [A] \) (box of \( A \)) many integrators results in maximum overall gain and the gain starts falling on cascading integrators further. Now, considering the effect of the output resistance of the integrator, using eq. (16) the overall gain of 2 cascaded integrators can be expressed as

\[ A_{int,2} = (g_{m1,2} R)^2 \left( 1 - \left( 1 + \frac{T_{int}}{RC_L} \right) e^{-T_{int}/RC_L} \right) \]  

(26)

which again matches the expression in eq. (24) if \( T_{int} << RC_L \). Fig. 19 compares the gain of 2 cascaded integrators obtained from eq. (26) to that of a single integrator. Note that 2-cascaded integrators can provide much higher gain than the LNA with even lower power consumption than the LNA.

V. PERFORMANCE OF DIFFERENT ARCHITECTURES FOR LOSSY BROADBAND CHANNELS

Based on the detailed analyses of different signaling blocks in the previous section, we are now in a position to compare the performance of each architecture in Fig. 4 for different channel loss. In the performance analysis of different topologies, a full rate RX architecture has been assumed where the clock frequency is the same as the data rate. The methodology adopted to find the maximum achievable data-rate of each architecture as a function of the channel-loss is delineated below.

For any particular topology, as the channel loss (L) increases, the input signal swing to the RX (\( v_{RX}(L) \)) reduces. Let \( A_{FE}(f) \) be the gain of the RX front-end which depends on the operating-frequency \( f \) (or, equivalently the data-rate). Then, the input voltage of the sampler is given by, \( v_{SAL}(f,L) = A_{FE}(f)v_{RX}(L) \). If \( g \) be function which maps the input voltage of the strongARM latch (\( v_{SAL} \)) to its
maximum operating frequency (Fig. 6(b)), then a data-rate \( f \) is achievable by an architecture \( \text{iff} \) \( g(A_{FE}(f)v_{SAL}(L)) \geq f \). Hence, the maximum achievable data-rate \( (f_{\text{max}}) \) for an architecture corresponding to a channel loss \( L \) is one for which the previous equality holds, i.e. \( g(A_{FE}(f_{\text{max}})v_{SAL}(L)) = f_{\text{max}} \). Note that, in this methodology, noise of the front-end has not been considered. However, with reduction in the input signal swing of RX, the input signal-to-noise ratio (SNR) reduces which in turns degrade the bit-error rate (BER) of the final received data. Hence, the total input referred noise of a topology limits the maximum channel loss it can support \( (L_{\text{max}}) \) for a target BER. Fig. 20 shows the BER vs SNR plot for NRZ communication. For wireline applications, a target BER of \( 10^{-12} \) is generally used and for mm-wave (or in general wireless) applications the preferred target BER is \( 10^{-3} \) considering the large loss of wireless channel. However, for wireline-like channels any target BER in this range can be chosen depending on the application and the value of channel loss. In the following performance analysis, while calculating the energy efficiency of different RX architectures, power consumed by the clock generation circuits and biasing circuits has not been included for simplicity and to focus on the Rx architecture dependent power.

A. Architecture I: Only sampler

Assuming a 1 V transmitted signal swing, the input signal swing of the RX \( (v_{RX}) \) can be computed as a function of the channel loss, \( L \) and maximum achievable data rate for that particular channel loss can be found following the methodology discussed earlier. Fig. 21 shows the corresponding plot. Note that, \( A_{FE}(f) = 1 \) for architecture-I. Also, as the channel loss increases, the input SNR reduces which degrades the BER of the received signal. Considering a target BER of \( 10^{-12} \), the maximum channel loss architecture-I can support is 48 dB and for a BER of \( 10^{-3} \), the maximum allowable channel loss is 55 dB. Also, as power consumption of the strongARM latch is proportional to the clock frequency (and hence to the data rate), energy efficiency of architecture-I is constant and independent of the data rate. For the design in this work the energy efficiency is found out to be 0.022 pJ/bit.

B. Architecture II: LNA + sampler

Fig. 22 shows the performance of architecture-II for different channel loss. As expected, introduction of the LNA improves the maximum data rate for each channel loss and also shifts the BER constraint curve towards right by offering lower input referred noise. The input referred noise of the RX in this case can be given as

\[
V_{n,in,RX} = \sqrt{V_{n,in,LNA}^2 + \frac{V_{n,in,samp}^2}{A_{LNA}^2}} \tag{27}
\]

From eq. (27) it can be seen that the RX input referred noise is mostly dominated by the LNA and hence is quite low comparative to that of architecture-I leading to a 10 dB improvement in maximum allowable channel loss (Fig. 22). Also, the \( V_{n,in,RX} \) is a function of data rate and hence, the BER constraint curves in Fig. 22 are not exactly vertical as in Fig. 21. Hence, after \( L_{\text{max}} \), the maximum data rate decreases rapidly while satisfying the BER constraint. Note that the minimum bias current required for the LNA varies linearly with data rate (Fig. 10(a)) rendering the energy efficiency of architecture-II to be constant which is having a value of 0.082 pJ/bit in this design.
C. Architecture III: Integrator + sampler

Fig. 23 shows the performance of architecture-III for different channel loss. Given that both the LNA in architecture-II and integrator in architecture-III are driving the same sampler (i.e. same $C_L$), performance of the integrator is subordinate to that of the LNA both in terms of gain and input referred noise. Hence, a deterioration in maximum allowable data rate and maximum achievable channel loss can be observed as compared to architecture-II. However, energy efficiency of this architecture ($\approx 0.042$ pJ/bit) is superior than that of architecture-II due to lower power consumption of the integrator. It also shows a significant improvement in the maximum data rate compared to that of architecture-I due to the additional gain provided by the integrator. Hence, architecture-III can be suitably used to achieve high data-rate with low power consumption for applications with relatively lower channel loss.

D. Architecture IV: LNA + integrator(s)+ sampler

To improve the maximum achievable data rate further for architecture-II, an integrator can be introduced between the LNA and sampler, which provides gain to the signal with lower power consumption. Fig. 24 shows the improvement in gain of the RX front-end by cascading an LNA and integrator. Using both LNA and integrator in the RX front-end ensures both lower RX input referred noise($V_{n_{in,RX}}$) as well as higher front-end gain. Note that, an alternative way to improve the gain would have been to cascade multiple LNAs. However, the LNA+integrator combination provides comparable gain to that of LNA+LNA combination with a much lower power consumption. To increase the front-end gain further, multiple integrators can be used as discussed in section IV.D. Fig. 25 shows the variation of maximum achievable data rate with channel loss for architecture-IV with both single and 2-cascaded integrators. It can be seen from Fig. 25 that the BER constraint curve remains the same for both single and 2-cascaded integrators. This is due to the fact that $V_{n_{in,RX}}$ is governed by the input referred noise of the LNA and first integrator as the large gain of the LNA and integrator combination makes the noise contribution of the next stages insignificant. Energy efficiency of architecture-IV is 0.102 pJ/bit with a single integrator and 0.122 pJ/bit for 2-cascaded integrators.

VI. COMPARISON OF DIFFERENT ARCHITECTURES

Fig. 26 compares the performance of different RX architectures. It is obvious from the previous discussions that for any given channel loss, architecture-IV with 2-cascaded integrators gives the highest maximum achievable data-rate (Fig. 26(a)). With increase in channel loss, the maximum achievable data-rate decreases with a gradual degradation in the BER performance for all the architectures. In Fig. 26(a) the dotted portion of the curves represents a BER $\geq 10^{-5}$. Fig. 26(b) shows the maximum sustainable channel loss for different RX architectures for two standard BERs. It can be seen that deploying LNA in the RX front-end extends the maximum achievable channel loss for architectures II and IV compared to the others. Hence, if the application demands high data rate even with a very large channel loss, one must deploy an LNA in the RX front-end. Note that, all these figures show the ideal performance of different architectures. In real scenario, the clocking scheme apart from the signaling blocks
may also limit the maximum data-rate and increase the energy-efficiency. However, those additional constraints have not been considered in this work as the main focus was to identify the most suitable architecture given different channel loss profile and data-rate requirements. Our previous work on interference-robust HBC [9] deploys architecture-III which achieves a data-rate of 30 Mbps for a channel loss of 60 dB and target BER of $10^{-3}$. This observation can be corroborated from Fig. 23 which shows that, for architecture-III once the channel loss exceeds $L_{max}$ ($=53$ dB), the maximum achievable data-rate decreases drastically while satisfying the target BER.

VII. CONCLUSION

The work theoretically analyzes performance of different signaling blocks that can be employed in the RX for broadband communication through lossy wireline-like channels. A new approach to theoretically estimate the input referred noise of the strongARM latch has been described and compared with simulation results. An accurate closed-form expression of the gain of the current-integrating amplifier has been developed. The work also proposes the use of multi-integrator cascade as a low-power gain element and shows how employing the same in the RX improves the gain of the front-end with low power consumption. Finally, based on the analysis of the signaling blocks, performance of different architectures have been analyzed and compared. The in-depth analysis sets a foundation for the choice of appropriate receiver architecture for lossy broadband channels, that are becoming popular in applications such as proximity communication, human body communication among others.

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