Rule-Based Optimization of Reversible Circuits

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Abstract—Reversible logic has applications in various research areas including low-power design and quantum computation. In this paper, a rule-based optimization approach for reversible circuits is proposed which uses both negative and positive control Toffoli gates during the optimization. To this end, a set of rules for removing NOT gates and optimizing sub-circuits with common-target gates are proposed. To evaluate the proposed approach, the best-reported synthesized circuits and the results of a recent synthesis algorithm which uses both negative and positive controls are used. Our experiments reveal the potential of the proposed approach in optimizing synthesized circuits.

I. INTRODUCTION

A Boolean function is called reversible if it maps each input assignment to a unique output assignment. Landauer [1] proved that using conventional irreversible logic gates leads to energy dissipation, regardless of the underlying circuit. Today, reversible logic has received considerable attention in various research areas including low-power CMOS design [2] and quantum computing [3].

Reversible logic synthesis deals with generating an efficient reversible circuit from a given reversible specification. The synthesis of reversible circuits differs from that of traditional irreversible ones with respect to the characterizations of reversible logic. For examples, loop and fanout are not allowed in reversible logic. Therefore, the available synthesis algorithms for irreversible circuits cannot be applied to reversible specifications directly.

In order to generate an efficient reversible circuit from a given specification, different scenarios have been applied in the recent years. Among them, a two-step synthesis and optimization approach has been widely used recently. In this scenario, a realization is found from a given specification first and then, further optimizations are applied in a post-processing step to improve various cost metrics (e.g., quantum cost). Local transformation [4], templates matching [5-8], and data-structure-based optimization [9] were used to simplify synthesized circuits in the past.

In this paper, we propose a rule-based optimization approach for reversible circuits to improve the quantum cost. To this end, multiple control Toffoli gates with both positive and negative controls are used. While the potential advantage of using negative control Toffoli gates for the simplification of reversible circuits has been announced
(124x537) before (e.g., see [10]), this is the first attempt to use negative control Toffoli gates for improving the quantum cost of the synthesized circuits.

The remainder of the paper is organized as follows. In Section [II] basic concepts are explained. Previous work is discussed in Section [III]. Our rule-based optimization approach is proposed in Section [IV]. Experimental results are reported in Section [V] and finally, Section [VI] concludes the paper.

II. PRELIMINARIES

An $n$-input, $n$-output, fully specified Boolean function $f : \mathbb{B}^n \rightarrow \mathbb{B}^n$ over variables $X = \{x_1, \ldots, x_n\}$ is called reversible if it maps each input pattern to a unique output pattern. In this paper, $n$ is particularly used to refer to the number of inputs/outputs of a circuit (circuit size). Outputs that are not required in the function specification are considered as garbage or auxiliary bits. An $n$-input, $n$-output gate is reversible if it realizes a reversible function. Previously, various reversible gates with different functionalities have been proposed. Among them, multiple control Toffoli gate has been used by different synthesis methods (e.g., see [6, 8, 10–15]) and is defined as:

A multiple control Toffoli gate $C^m$NOT can be written as $C^m$NOT($C; t$), where $C = \{x_{i_1}, \ldots, x_{i_m}\} \subset X$ is the set of control lines and $t = \{x_j\}$ with $C \cap t = \emptyset$ is the target line. The value of the target line is inverted iff all control lines have the required zero or one values. A control line may be positive (negative) which means that if its value is one (zero), the target is inverted. For $m=0$ and $m=1$, the gates are called NOT and CNOT, respectively. For $m=2$, the gate is called $C^2$NOT or Toffoli.

In addition to the $C^m$NOT gate, several other gate types have been proposed in the literature (see [3] for some examples). Controlled-V (controlled-V+) changes the value on its target line using the transformation given by the matrix $V$ ($V^+$) if the control line has the value of 1.

$$V = \frac{1+i}{2} \begin{bmatrix} 1 & -i \\ -i & 1 \end{bmatrix}, \quad V^+ = \frac{1-i}{2} \begin{bmatrix} 1 & i \\ i & 1 \end{bmatrix}$$

Fig. 1 shows different gate types where positive and negative controls are denoted by ● and ○ symbols, respectively.

The gates NOT, CNOT, controlled-V, and controlled-V+ (with positive controls) have been efficiently simulated in some quantum computer technologies [16]. These gates are considered as elementary gates for reversible Boolean functions. The number of elementary gates required for simulating a given gate is called quantum cost. A reversible circuit includes a set of reversible gates.
Consider a circuit of size $n$. For ($n \geq 5$), a $C^m$NOT gate ($m \in \{3, 4, \cdots, \lceil n/2 \rceil \}$) can be simulated by $12m - 22$ elementary gates if at least one positive control is available; otherwise, two extra elementary gates are required [7][10]. In addition, for $n \geq 7$, a $C^{n-2}$NOT gate can be simulated by $24n - 88$ elementary gates with no auxiliary bits if there is at least one positive control [7][10]. On the other hand, for a $C^{n-2}$NOT with only negative controls, four additional elementary gates are required [10]. Moreover, a $C^{n-1}$NOT gate can be simulated with an exponential cost $2^n - 3$ if no garbage line is available and all controls are positive [17]. A $C^{n-1}$NOT gate with at least one positive control has the same $2^n - 3$ cost. For the case of all negative controls, two additional elementary gates should be applied.

To avoid the exponential size and the need for a large number of elementary gates, several researchers used an extra garbage line for an efficient simulation of $C^{n-1}$NOT gate (e.g., [6]). Generally, the number of available bits is very restricted in today’s reversible and quantum implementations [18]. Therefore, for two circuits with equal linear costs, the one without garbage line is preferred. Note that a $C^{2}$NOT gate has the cost of 5 if at least one positive control exists. Otherwise, six elementary gates are required for the optimal implementation [19]. In addition, the quantum cost for a CNOT gate with negative control is 3.

For the purpose of optimization, two adjacent gates can be interchanged if the target of the first gate is not one of the controls of the second gate and vice versa (moving rule). In addition, two adjacent gates with the same functionalities can be canceled (deletion rule) [5].

### III. Previous Work

During the recent years, several algorithms have been proposed to address the requirements of the synthesis and optimization steps. In this section, we review optimization-related algorithms. However, as the algorithm of [11] is used in our experiments, we briefly explain it first.

A non-search based synthesis algorithm was proposed in [11] which works on the truth table columns of a given specification to gradually transform the truth table into the identity function. The algorithm always converges and it leads to a valid result very fast compared with those methods that explore the search space. Multiple control Toffoli gates with both positive and negative lines were used in this method.

In [4] a set of local transformation rules for reversible circuits was proposed. It was shown that the set was complete which means that for any two equivalent circuits, there is a sequence of transformations which change one of the circuits to the other. This rule set was used in [4] for developing a design theory for Boolean reversible circuits and improving their cost.

The application of rule set was extended in [5] where the authors introduced several transformation rules based on a set of predefined patterns called templates. According to [5], a template $T$ is a circuit with identity function which contains $m$ gates $g_1, g_2, \cdots, g_m$. Consider the first $k$ ($k > m/2$) gates of $T$ (i.e., $g_1, g_2, \cdots, g_k$) and suppose that these gates are applied in a reversible circuit in sequence. It can be verified that the set of $m - k$ gates $g_m, g_{k+2}, g_{k+1}$ can be applied instead of the initial $g_1, g_2, \cdots, g_k$ gates to reduce the gate count from $k$ to $m - k$. A similar method can be applied to reduce the quantum cost. The template-based optimization was used in several papers recently (see [6][8][10]).
The authors of [9] developed a data structure to generate and store optimal circuits for all reversible functions of size 3 and many of four inputs circuits. Using the proposed representation and algorithm, the authors guaranteed to have optimal implementations for all sub-circuits of size 3 and many of size 4 functions. In a given reversible circuit, a sub-circuit is examined if it contains less than 5 variables. Then, its optimal implementation is explored in a pre-constructed library and is replaced with the initial implementation if the optimal implementation is found.

IV. PROPOSED METHOD

In this section, after proposing a transformation rule for moving a NOT gate across a given reversible circuit, an optimization method is proposed to find the optimal realization of a sequence of gates with the same targets. Next, the proposed methods will be used to optimize the results of the available synthesis algorithms in a post-processing step.

A. NOT Reduction

By moving NOT gates through a given reversible circuit, one can delete redundant NOTs to improve the total cost according to the following rule:

**Definition 1** Pass Rule (PR): A NOT$(x)$ gate can be interchanged with its adjacent $C^{m} NOT(C;t)$ gate without changing the functionality of the circuit if at least one of the following conditions are met:

- $x \notin C, x \neq t$.
- $x \notin C, x = t$.
- $x \in C, x \neq t$. For this case, the polarity of the control $x$ of the $C^{m} NOT(C;t)$ gate is toggled. In other words, a negative control line can be considered as a positive control with two NOTs as shown in Fig. 2. Now, consider the controls in Fig. 3. Two NOT gates can be inserted after the positive control as shown in Fig. 3b which leads to Fig. 3c. See Fig. 4 for one example.

It is worth noting that by applying PR, an even number of adjacent NOTs can be canceled to reduce the quantum cost. See Fig. 5 for an example where the cost was improved from 7 to 5.

**Definition 2** Generalized Pass Rule (GPR): A $C^{n-1} NOT(C_{1};t_{1})$ gate can be interchanged with its adjacent $C^{n-2} NOT(C_{2};t_{2})$ gate without changing the functionality
of the circuit if $C_1 = C_2 \cup t_2$. In this case, the polarity of the control line $t_2$ of $C^{n-1}\text{NOT}(C_1; t_1)$ is toggled (see Fig. 6 for an example).

**B. Gates with Common Targets**

Karnaugh map (Kmap) has been extensively used to simplify small irreversible circuits in the past. On the other hand, the available optimization methods for reversible circuits, used pre-defined patterns (e.g., [10]) or well-developed data structures (e.g., [9]) or heuristics (e.g., [11]) to improve the cost of synthesized circuits.

The behavior of reversible gates differs from that of the irreversible ones (i.e., NAND, NOR, etc.) significantly. Hence, applying Kmap for the synthesis of a reversible function (i.e., from specification to circuit) may introduce some difficulties due to different gate types. In [20] a synthesis method was proposed which used a modified version of Kmap for the synthesis purpose. In this paper, we use Kmap for the optimization of sub-circuits with common targets that can be used to simplify the results of any other synthesis method.

A $C^{n-1}\text{NOT}$ gate can be represented by a Boolean expression with $n-1$ inputs and one output where gate controls act as the inputs and the target behaves as the output. Hence, a $C^{n-1}\text{NOT}$ gate can fill one cell of a Kmap of size $n$ (i.e., $n-1$ inputs, one output). In order to extract the simplified circuit, a Kmap-based cell grouping approach similar to the one used in irreversible logic is applied. Method 1 discusses the method.

**Method 1** Assume that the Kmap of a function is given. In order to extract the circuit from the given Kmap, the following rules should be followed:

a) All cells with the value 1 should be covered in at least one group.

b) The size of each group should be $2^p$ for $p \geq 0$.

c) Each cell with the value 1 can be used in an odd number of groups.

d) Each empty cell (i.e., a cell with the value 0) can be used in an even number of groups.

e) The minimum number of groups should be generated.
f) The maximum size for each group should be explored.

Cases (a) and (b) come from the Kmap for irreversible logic. Regarding (c) and (d), since each cell illustrates one $C^{n-1}$ NOT gate, the odd (even) number of groups means the odd (even) number of consecutive $C^{n-1}$ NOT gates. Applying the deletion rule reveals the proposition. The number of groups denotes the number of gates; hence the case (e) deals to the minimum number of gates. In addition, group size affects the number of control lines of the generated gate. To reduce the number of controls, the maximum size for each group should be explored (case (f)).

According to the case (d) of Method 1, empty cells in the Kmap for reversible circuits can also be covered in a group of cells with the values of 1. This characterization differs from the Kmap of irreversible logic. It is worthwhile to note that finding a realization for a given Kmap may not be unique.

**Theorem 1** Consider a Kmap grouped by applying Method 1. Each group defines a gate with $n - p$ controls where $n$ is the sub-circuit size and $2^p$ is the group size.

A group with size 1 is equal to a gate with $n - 1$ controls. Similarly, a group with size of 2 deletes one control to construct a gate with $n - 2$ controls. Repeating this process prove the theorem.

**Definition 3** Common-Target Rule (CTR): Each reversible sub-circuit of size $n$ with common targets can be optimized by applying Method 1.

Due to the lack of a Kmap with one input, CTR cannot be applied to simplify a 2-input sub-circuit. In order to model this case, the restricted CTR (i.e., R-CTR) is defined as follows:

**Definition 4** Restricted CTR (R-CTR): A positive-control CNOT near a negative-control CNOT on the same target is equivalent to a NOT applied on the same target. A negative-control CNOT immediately before or after a NOT on the same target is equivalent to a positive-control CNOT on the target. A negative control CNOT can be simplified to a positive control CNOT followed by a NOT, all gates on the same targets.

C. Examples

The following examples describe the proposed approach in more detail. It is worth noting that none of the examples, except Example 6 and Example 7, can be simplified by using the previously published optimization methods [5, 8, 9]. Since the proposed approach can use negative controls to reduce the quantum cost, it outperforms
the available methods. As shown in the experimental results section, the costs of the best-reported benchmark circuits can be improved by our method in some cases.

**Example 1** A circuit with three inputs is shown in Fig. 7-a. It can be verified that the quantum cost for this circuit is 10. Since the target lines of both gates are identical, a Kmap of size 2 can be used for the optimization (Fig. 7-c). According to Fig. 7-c, two groups are found where their sizes are $2^1=2$. It means that the optimized circuit has two gates (i.e., two groups) and each gate has one control as depicted in Fig. 7-b. It can be verified that the quantum cost for the optimized circuit is 2. Note that cells with the values 1 were grouped once and empty cells were grouped twice.

**Example 2** A reversible circuit of size 4 is shown in Fig. 8-a. The optimized circuit and its Kmap are shown in Fig. 8-b. and Fig. 8-c, respectively. It can be verified that the quantum costs for the circuit before and after the optimization are 26 and 15, respectively.

**Example 3** A reversible circuit of size 5 is shown in Fig. 9-a. The optimized circuit and its Kmap are shown in Fig. 9-b and Fig. 9-c, respectively. It can be verified that the quantum costs for the circuit before and after the optimization are 116 and 20, respectively.

As another example, consider **Example 4** where a 4-input circuit is given. In this case, cells with the values 1 fill almost all cells (for a Kmap with $M$ cells and $m$ 1-cells $m \geq \lceil M/2 \rceil$). In those cases, inverting the Kmap (using zero instead of one) and putting a NOT gate may help. See the following example for more detail.

**Example 4** A circuit of size 4 is shown in Fig. 10-a. Based on CTR, 10-b shows the realized circuit. Number of cells with the values 1 in more than four (i.e., $8/2=4$) as illustrated in Fig. 10-c. In Fig. 10-d the inverse Kmap is shown and used which leads to a $C^3$NOT followed by a NOT gate.
Example 5  A 4-input circuit with only positive controls is shown in Fig. 11-a. By applying CTR on this circuit, 11-b is resulted. The respective Kmap is shown in Fig. 11-c. Note that the term ‘abc’ is used twice in the circuit and it can be canceled. The quantum cost is improved from 18 to 13.

Applying GPR (or PR) on some circuits provides opportunities to improve the cost. See the following examples for more detail.

Example 6  A reversible circuit of size 3 is shown in Fig. 12-a. By applying PR on the circuit shown in 12-a, the circuit depicted in Fig. 12-b is resulted. It can be verified that two NOTs in 12-b can be canceled (see Fig. 12-c). Now, by applying CTR on the circuit of Fig. 12-c, the circuit given in Fig. 12-d is provided. In this example, the quantum cost is improved from 12 to 1.

Example 7  Fig. 13 shows several templates with 2 and 3 inputs introduced in [5]. In this example, we show how such templates and their generalized forms, resulted by inserting identical controls for all gates, can be obtained from the proposed approach. It can be verified that applying the proposed approach as listed below leads to the same results of [5] (cases 2.1, 2.2, 3.1, 3.3, 4.2, 4.3) or better ones (cases 4.4, 4.5).

- 2.1: PR, R-CTR
V. EXPERIMENTAL RESULTS

The proposed rule-based optimization algorithm was implemented in C++ and all of the experiments were done on an Intel Pentium IV 2.2GHz computer with 2GB memory. In order to evaluate the proposed approach, we used the algorithm of [11] which used both positive and negative control Toffoli gates. In addition, in [11] the truth table of a given reversible function is treated column-wise. Therefore, this algorithm produces sub-circuits with common-target gates in many situations. To compare our results, we used the same set of circuits as used in [11]. The synthesis results are shown in Table I. It can be seen that the proposed approach can be used to reduce the quantum cost of a given circuit with both negative and positive controls in some cases significantly.

To further analyze the method, we used the available reversible synthesized benchmarks [21]. To this end, the best-reported synthesized circuits were selected [6]. Quantum cost is used in all comparisons. For the approach of [6], the synthesis algorithm, the template matching method, the random and exhaustive driver algorithms were applied
sequentially to improve synthesis costs. A random driver performs several iterations where at each iteration, a number of random subnetworks are re-synthesized and the best circuit is forwarded to the next iteration. In addition, the exhaustive driver tries all possible subnetworks with at least 5 gates of a given network. Bidirectional and quantum cost reduction modes were also applied.

The results of applying the proposed approach on the results of [6] are shown in Table II. In this table, quantum costs for both methods are compared. While the results of [6] were improved by using different scenarios (i.e., template matching, random driver, exhaustive driver, bidirectional mode, quantum cost reduction mode), the fact that the best-reported synthesized results can be improved by using Toffoli gates with negative controls as done in the proposed approach is very interesting. The application of the proposed approach on non-reported benchmark circuits had no effect on their quantum costs and ignored in Table II to save space. Fig. 14 and Fig. 15 illustrate the synthesized circuits of [6] and ours for two benchmarks. The runtime of the proposed method is less than a second for each attempted circuit.

### Simplification of the circuits from [11]. Runtime for each circuit is less than one second.

| # Circuit | Circuit | Specification | Quantum cost | Imp. % |
|-----------|---------|---------------|--------------|--------|
| 1         | 3       | (1,0,3,2,5,7,4,6) | 18           | 17     | 5.5   |
| 2         | 3       | (7,0,1,2,3,4,5,6) | 7            | 7      | 0     |
| 3         | 3       | (0,1,2,3,4,6,5,7) | 15           | 15     | 0     |
| 4         | 3       | (0,1,2,3,5,6,7)   | 27           | 27     | 0     |
| 5         | 4       | (0,1,2,3,4,5,6,8,7,9,10,11,12,13,14,15) | 195          | 131    | 33    |
| 6         | 3       | (1,2,3,4,5,6,7,0) | 7            | 7      | 0     |
| 7         | 4       | (1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,0) | 25           | 20     | 20    |
| 8         | 4       | (0,7,6,9,4,11,10,13,8,15,14,1,12,3,2,5) | 12           | 12     | 0     |
| 9         | 3       | (2,6,5,7,1,0,4)   | 32           | 29     | 9     |
| 10        | 3       | (1,2,7,5,6,3,0,4) | 35           | 26     | 26    |
| 11        | 3       | (4,3,0,2,7,5,6,1) | 37           | 29     | 22    |
| 12        | 3       | (7,5,2,4,6,1,0,3) | 28           | 19     | 32    |
| 13        | 4       | (6,2,14,13,3,11,10,7,0,5,8,1,15,12,4,9) | 214          | 136    | 36    |
TABLE II
IMPROVING THE BEST-REPORTED COSTS OF SOME AVAILABLE BENCHMARKS. RUNTIME FOR EACH CIRCUIT IS LESS THAN ONE SECOND.

| Benchmark Function | Benchmark | n | Quantum cost 6 | Ours |
|--------------------|-----------|---|----------------|------|
| 3_17               |           | 3 | 14             | 13   |
| 4_39               |           | 4 | 32             | 30   |
| t-add-8            |           | 24| 322            | 314  |
| mod5sadder         |           | 6 | 77             | 71   |
| ed53               |           | 7 | 65             | 62   |
| hwb5               |           | 8 | 14             | 101  |
| hwb6               |           | 6 | 77             | 71   |
| hwb7               |           | 7 | 65             | 62   |
| hwb8               |           | 8 | 6709           | 6687 |
| hwb9               |           | 9 | 20223          | 20020|
| hwb10              |           | 10| 52253          | 52235|
| hwb11              |           | 14| 1211840        | 121830|

Fig. 14. Realization of the 3_17 benchmark, (a) the best-reported circuit [6], (b) the improved circuit.

VI. CONCLUSION

In this paper, an optimization approach for reversible circuits was proposed which applies a set of rules to improve the quantum cost of a given circuit. By employing both negative and positive control Toffoli gates during the optimization, it was shown that there is some room for improvement in the results of the available synthesis algorithms. To this end, we proposed a rule to reduce NOT gates of a given circuits. Next, a Karnaugh map-based optimization method was presented to optimize sub-circuits with common-target gates. To evaluate the proposed approach, one of the recent synthesis algorithms which used both negative and positive controls was selected. It has been shown that the proposed approach can reduce the quantum cost for the attempted circuits by up to 36%. Moreover, the experiments showed that our method could improve the best-reported circuits in some cases.

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Fig. 15. Realization of the mod5adder benchmark, (a) the best-reported circuit [6], (b) the improved circuit.

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