GNNear: Accelerating Full-Batch Training of Graph Neural Networks with Near-Memory Processing

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Abstract
Recently, Graph Neural Networks (GNNs) have become state-of-the-art algorithms for analyzing non-euclidean graph data. However, to realize efficient GNN training is challenging, especially on large graphs. The reasons are many-folded: 1) GNN training incurs a substantial memory footprint. Full-batch training on large graphs even requires hundreds to thousands of gigabytes of memory. 2) GNN training involves both memory-intensive and computation-intensive operations, challenging current CPU/GPU platforms. 3) The irregularity of graphs can result in severe resource under-utilization and load-imbalance problems.

This paper presents a GNNear accelerator to tackle these challenges. GNNear adopts a DIMM-based memory system to provide sufficient memory capacity. To match the heterogeneous nature of GNN training, we offload the memory-intensive Reduce operations to in-DIMM Near-Memory-Engines (NMEs), making full use of the high aggregated local bandwidth. We adopt a Centralized-Acceleration-Engine (CAE) to process the computation-intensive Update operations. We further propose several optimization strategies to deal with the irregularity of input graphs and improve GNNear’s performance. Comprehensive evaluations on 16 GNN training tasks demonstrate that GNNear achieves 30.8× / 2.5× geometric speedup and 79.6× / 7.3× (geomean) higher energy efficiency compared to Xeon E5-2698-v4 CPU and NVIDIA V100 GPU.

Keywords
near-memory processing, graph neural networks, domain-specific accelerator, machine learning

ACM Reference Format:
Zhe Zhou, Cong Li, Xuechao Wei, Xiaoyang Wang, and Guangyu Sun. 2022. GNNear: Accelerating Full-Batch Training of Graph Neural Networks with Near-Memory Processing. In International Conference on Parallel Architectures and Compilation Techniques (PACT ’22), October 8–12, 2022, Chicago, IL, USA. ACM, New York, NY, USA, 15 pages. https://doi.org/10.1145/3559009.3569670

1 Introduction
The past few years have witnessed the explosion of deep-learning techniques. To process traditional euclidean data such as 2D images, Convolutional Neural Networks (CNNs) have been invented and become the de-facto tools on diverse tasks such as image classification [36, 39, 42, 53, 88], object detection [32, 63, 82, 83], and image segmentation [70, 85, 108, 122]. However, though CNNs are powerful in image processing, they cannot process the equally pervasive non-euclidean graph data. Thus, there has been an increasing interest in Graph Neural Networks (GNNs). We notice that GNNs have brought many breakthroughs on various graph-based tasks, such as node classification [27, 31, 52], point-cloud analysis [81, 97, 104, 113], recommendation systems [1, 20, 101, 107, 119], and drug discovery [37], and smart traffic [17, 28, 120], IC design [71, 96, 117], physical system simulation [37], and drug discovery [65, 91].

Apart from algorithmic innovations, there are also some GNN accelerators designed to accelerate the inference of various GNN algorithms [11, 29, 30, 57, 59, 60, 88, 100, 121]. However, due to many challenges, neither existing accelerators nor GPU/CPU platforms can easily support GNN training at scale. Firstly, GNN training incurs a large memory footprint. To enable back-propagation, we have to buffer a huge amount of intermediate data. Even the middle-scale Reddit dataset [35] containing 114 million edges will...
take up 58 GB of memory [14] with PyG framework [22], exceeding most GPUs’ capacity. Meanwhile, as illustrated in Figure 1, the scale of graphs applied in GNN researches has been growing exponentially in recent years [16, 35, 41, 52]. Although mini-batch training strategies leveraging neighbor-sampling [9, 16, 35, 110] successfully reduce the memory requirement by limiting the training batch size, they are proved to have lower accuracy compared to full-batch training due to approximation errors [7, 35, 44, 67, 95].

Secondly, GNN training has both memory-intensive (e.g., 0.5 Ops/Byte) features/grads reduction and computation-intensive (e.g., 128 Ops/Byte) features/grads update operations. Neither PIM/NMP-based graph processing accelerators [2, 18, 74, 118, 124] (optimized for memory access) nor traditional DNN accelerators [10, 12, 13, 26, 46, 115] (optimized for computation) can handle such a heterogeneous nature in GNN training. Thirdly, the irregularity of real-world graphs will result in severe resource under-utilization and load-imbalance problems [29, 30, 105], increasing the difficulty of optimizing a GNN training system’s throughput.

To tackle these challenges, we propose GNNear, which harnesses both near-memory processing (NMP) and centralized processing to achieve high-throughput, energy-efficient, and scalable GNN training on large graphs. Specifically, we first analyze the GNN training procedure and categorize the involved operations as a sequence of memory-intensive Reduce and computation-intensive Update operations. We then adopt DIMM-based Near-Memory Engines (NMEs) and a powerful Centralized-Acceleration-Engine (CAE) to process them respectively. Such a hybrid architecture perfectly matches the algorithmic structure of GNN training and provides adequate memory capacity/bandwidth, but still suffers from resource-under-utilization and load-imbalance problems due to the irregularity of graphs. Therefore, we propose several optimization strategies concerning data reuse, data mapping, graph partition, and dataflow scheduling, etc., to improve the training throughput further. To summarize, we make the following main contributions:

- We characterize the full-batch GNN training and abstract the involved operations as memory-intensive Reduce and computation-intensive Update operations. (Section 3)
- We propose GNNear accelerator, which leverages both DIMM-based Near-Memory Engines (NMEs) and a Centralized Acceleration Engine (CAE) to provide sufficient memory capacity and match the heterogeneous nature of GNN training. (Section 4)
- We propose several optimization strategies to deal with the resource under-utilization and load-imbalance problems caused by the irregularity in real-world graphs and improve GNNear’s performance further. (Section 5)
- We conduct comprehensive experiments on various GNN training tasks to validate the superiority of GNNear accelerator over commercial CPU/GPU platforms. (Section 6)

### 2 Background

In this section we introduce the basics of GNN and GNN training. Notations are listed in Table 2.

#### 2.1 GNN Algorithm Basics

Generally, a GNN model is composed of several GNN layers. Given an input graph $G = (V, E)$, where $V$ and $E$ are sets of vertices and edges, each GNN layer computes with two-step operations illustrated in Figure 2. The operations are also abstracted as follows:

\[
\begin{align*}
\hat{h}_u^l &= \text{AGGREGATE}(\{h_v^{l-1} | v \in \mathcal{N}(u)\}) \\
\hat{h}_u^l &= \text{COMBINE}(\hat{h}_u^l)
\end{align*}
\]

At the $l$-th layer, the Aggregation step gathers each vertex $v$’s neighbor features (denoted as $h_v^{l-1}$) and uses an aggregator to merge the features. Then the aggregation result $\hat{h}_u^l$ is processed with the Combination step, which transforms $\hat{h}_u^l$ to $h_u^l$ using a neural network. After combination, $h_u^l$ serves as the input of layer $l+1$. The final layer’s outputs $h_u^l$ will be used as vertex-level representations for various downstream tasks.

The GCN algorithm [52] adopts Weighted Sum as its aggregator and combines with a fully-connected layer:

\[
d_u^l = \sum_{u \in \mathcal{N}(v)} \frac{1}{\sqrt{D_u + D_v}} h_u^{l-1}, \quad h_u^l = \text{ReLU}(d_u^l \cdot W^l)
\]

In the formula, $D_u$ and $D_v$ denote the degrees of vertex $v$ and each neighbor $u$. The neighbor features are aggregated using summation with degree-based normalization. Apart from GCN, several GNN variants are also proposed. As listed in Table 1, GCN [103] and SAGEConv [35] use Sum and Mean operators for aggregation. GAT [1] leverages a self-attention mechanism to implement its aggregator. It first calculates the attention coefficient $a_{uv}$, which measures the importance of vertex $v$ to $u$’s neighbor $w$. Then the aggregation results are the weighted sum of neighbors’ features. Except for GIN, which adopts Multi-Layer-Perception (MLP) for combination, both SAGEConv and GAT use a single fully-connected layer for combination. Without loss of generality, we use GCN as a representative example in the following discussions.

#### Table 1: Variants of GNNs

| Variant | Aggregation | Combination |
|---------|-------------|-------------|
| GCN [52] | $d_u^l = \sum_{u \in \mathcal{N}(v)} \frac{1}{\sqrt{D_u + D_v}} h_u^{l-1}$ | ReLU($d_u^l \cdot W^l$) |
| GIN [103] | $d_u^l = (1 + \epsilon) \cdot h_u^l + \sum_{u \in \mathcal{N}(v)} h_u^{l-1}$ | MLP($d_u^l \cdot W^l, b^l$) |
| SAGEConv [35] | $a_{uv} = \sigma(a^T [W^l h_u^l || W^l h_v^l])$ | ReLU($d_u^l \cdot W^l$) |
| GAT [1] | $a_{uv} = \text{Softmax}(a^T [W^l h_u^l || W^l h_v^l])$ | ELU($d_u^l \cdot W^l$) |

### Figure 2: The GNN inference workflow.
2.2 GNN Training

To learn useful information from input graphs, a GNN model first undergoes the training procedure, which can be divided into the forward pass and the backward pass. As illustrated in Figure 3, after a sequence of aggregation and combination operations, a loss function calculates loss \( L \) with the forward outputs and labels. In the backward pass, each \( \nabla \text{CB} \) step computes the gradients of weights \( W^l \) and hidden features \( h^l_v \), while \( \nabla \text{AG} \) aggregates the feature gradients for each vertex along edges. We can easily derive the formulation of \( \nabla \text{AG} \) through the chain-rule:

\[
\nabla \text{AG} : \delta^l_u = \text{mask}(\sum_{u \in (v)} \frac{1}{\sqrt{D_u + D_v}} \delta^{l+1}_{u})
\]

(4)

Where \( \delta^{l+1} \) denotes the feature gradients of vertex \( u \) at layer \( l + 1 \), namely \( \frac{\partial L}{\partial h^l_u} \), \( \text{mask}(\cdot) \) corresponds to gradients of activation function like ReLU(). Then \( \nabla \text{CB} \) computes the weight gradients with the feature gradients of each vertex \( v \):

\[
\nabla \text{CB} : \delta^l_v = \delta^l_u \cdot W^{l+1\top}, \quad \frac{\partial L}{\partial W^l} = \frac{\partial L}{\partial W^l} + \delta^l_v \cdot \delta^l_u
\]

(5)

The weight gradients \( \frac{\partial L}{\partial W^l} \) are initialized to zero at the beginning of each training epoch. The final weight gradients are used to update the model weights through gradient descent: \( W^l = W^l - \eta \frac{\partial L}{\partial W^l} \) where \( \eta \) denotes the learning rate. The training process iterates for several epochs until convergence.

The main computation in both forward and backward passes can be categorized into two different types according to their computation patterns, namely Reduce and Update. The Reduce operations aggregate features/gradadients along the edges of each destination vertex, which are abstracted as:

\[
\text{Reduce} : Y_v = \sum_{u \in (v)} \text{edge}_w(u, v) \cdot X_u
\]

(6)

Vectors \( X_u \) and \( Y_v \) can be either hidden features (forward) or feature gradients (backward), while scalars \( \text{edge}_w(u, v) \) denotes the edge weight concerning source vertex \( u \) and destination vertex \( v \) (e.g., \( \frac{\partial L}{\partial W^l} \)). Each vertex’s Reduce operation accumulates the weighted feature/gradient vectors from all its neighbors. Thus the total number of weighted vector additions for each layer is \( 2 \times |E| \).

The Update operations perform vector-matrix or vector-vector multiplications to generate new features/gradients for vertices or

| Table 2: List of Notations Used in GNN Training Algorithms |
| --- |
| Notation | Description |
| \( V, E \) | Sets of vertesxes and edges |
| \( \mathcal{N}(v) \) | The neighbors of vertex \( v \) |
| \( \mathcal{N}(v) \) | The set containing \( v \) and \( v \)’s neighbors: \( \{\mathcal{N}(v)\} \cup \{v\} \) |
| \( D_v \) | The degree of vertex \( v \) |
| \( h^l_v \) | Hidden feature vector of vertex \( v \) at the \( l \)-th layer |
| \( a^l_v \) | Aggregated feature vector of vertex \( v \) at the \( l \)-th layer |
| \( W^l \) | Weight matrix in layer \( l \) |
| \( L \) | The loss value calculated with outputs and labels |
| \( \delta^l_u \) | The gradients of \( h^l_u \), namely \( \frac{\partial L}{\partial h^l_u} \) |
| \( \delta^l_v \) | Aggregated masked gradients for vertex \( v \) |

2.3 Full-batch VS. Mini-batch Training:

On real-world tasks, the input graphs can be too large to fit into a single GPU. Mini-batch training is then proposed to mitigate this problem via neighborhood sampling [9, 16, 35, 110]. They sample vertices and their neighbors to create a mini batch that can fit into GPUs. However, it has been widely admitted that due to approximation errors, in some cases, mini-batch training achieves lower accuracy compared to full-batch training [7, 35, 44, 67, 95]. Therefore, many mini-batch training algorithms focus on proposing accurate sampling methods to improve the model accuracy [64]. For full-batching training, how to improve the training efficiency is the key problem [7, 44, 67, 95]. Considering that a system supporting full-batch training can also conduct mini-batch training by adding an extra sampler. We focus on full-batch training in this paper.

3 Challenges Analysis

3.1 Characterising GNN Training

Large Memory Footprint: The ever-increasing graph scale shown in Figure 1 poses a great challenge to full-batch GNN training. For example, training on the middle-scale Reddit dataset [35] containing 114 million edges requires 58 GB of memory to hold all the intermediate data and incurs over 300 GB of DRAM access [14] with PyG framework [22]. DGL framework [19] has an optimized memory management but is still hard to train on a larger dataset like Amazon [16] with a single GPU. According to the analysis [44], we need to buffer much temporal data during training. The Ogbn-Papers dataset containing 111 million vertices [41] consumes at least 568 GB of memory to train a two-layer model with a hidden size of 256. What is worse, the data gathering operations along edges incur \( O(L \times |E| \times d) \) memory accesses (\( L \) denotes the number of layers while \( d \) is the feature dimension), making the system also memory-bandwidth-bounded.

Training Bottlenecks: We profile the execution time of GNN training operators using PyTorch-profiler [80] on an NVIDIA V100-32GB GPU with PyG [22] framework. Four GNN algorithms introduced in Section 2 and four middle-scale graph datasets, namely PubMed (PB) [6], Flickr (FL) [110], Amazon–Computer (AC) [87], and Reddit (RD) [35], are adopted as benchmarks. According to Section 2.1, we have classified the main GNN training operations
as Reduce and Update operations to process feature/gradients aggregation and combination. The remaining operations, such as loss computation, are classified as Others. As shown in Figure 4, in general, Reduce and Update operations are the main bottlenecks during GNN training. The Reduce operations are the most time-consuming on V100 GPU in most cases, but Update operations also take considerable time on PB and FL datasets, especially for GAT. On CPU platforms, Update operations will take up more time due to CPUs’ poor computation capacity.

The Heterogeneous Nature: GNNs’ weights are usually small in size. For instance, a 4-layer GCN with input-size, output-size, and hidden-size of 256 only has about 1 MB of weights. It is feasible to store weights to on-chip SRAM and reuse them among vertices. Therefore, assuming $d_{in} = d_{out} = d$ for simplicity, where $d_{in}, d_{out}$ represent the input and output dimensions of a layer, the theoretical arithmetic intensity of Update with the form of $Y_o = X_o \cdot W$ is $\frac{2d_{in} \times d_{out}}{V_{ops} \times |V|}$. For Update operations with the form of $Y_o = X_o \cdot Z_o$, the shape transformation is $(d \times d) \cdot (1 \times d) = (d \times d)$. We have to read vectors $X_o, Z_o$ but do not need to write back the weight gradients $Y_o$. Thus, the arithmetic intensity is $\frac{d \times d}{V_{ops}} = 0.125 \times d$ Ops/Byte. On the contrary, for Reduce operations, massive amounts of features/gradients should be loaded from DRAM and can hardly be reused. Then the arithmetic intensity is $\frac{2 \times N(s) \times d_{out}}{V_{ops} \times |V|} \approx 0.5$ Ops/Byte, if using Weighted Sum as the aggregator. Obviously, Reduce operations are much more memory-intensive than Update. We also conduct CPU-based real-system profiling using Intel-Vtune [43]. As shown in Table 3, Reduce operations show a much lower arithmetic intensity and worse data locality than Update and Others, which is inefficient to accelerate with traditional neural network accelerators [10, 12, 13, 78, 115] optimized for computation-intensive workloads.

3.2 Near-Memory-Processing to the Rescue?

Recently, Near-Memory-Processing (NMP) paradigm has been proposed to provide memory-capacity proportional bandwidth and computation capacity. Chameleon [5] is a pioneering work that integrates CGRA cores to buffer-chips of DDR4 LRDIMMs [69] to enable general-purpose near-memory computation. RecNMP [48] and TensorDIMM [55] also propose to accelerate Deep Learning Recommendation Models (DLRMs) adopting such a paradigm. These works motivate us to leverage the DIMM-based NMP technique to accelerate full-batch GNN training.

However, designing a NMP accelerator suitable for full-batch GNN training is still a challenging task. Firstly, unlike DLRMs, which only need to consider the memory-intensive embedding table gathering operations [34], GNN training also has computation-bounded Update operations due to its heterogeneous nature. For instance, a two-layer GIN model (a GNN variant in Table 1) trained on Ogbn-Papers dataset with a hidden size of 256 incs more than 100 TFLOPs computation for just one iteration. It takes a server CPU several minutes to finish. Secondly, unlike DLRMs that respond to random quires, GNN training must consider the graph structure. Due to the irregularity of real-world graphs, a naive NMP-based GNN training system will have severe resource under-utilization and load-imbalance problems.

4 GNNear Architecture

To overcome the mentioned challenges, we propose GNNear, a hybrid GNN training accelerator combining both DIMM-based near-memory processing engines and a centralized acceleration engine. It matches the heterogeneous nature of GNN training and provides sufficient memory capacity for full-batch GNN training.

4.1 Overview

Design: As illustrated in Figure 5, GNNear accelerator consists of a Centralized Acceleration Engine (CAE) and multiple NMP-enabled DIMMs. The CAE resembles Google’s TPU, which equips a powerful GEMM engine and a vector-processing unit (VPU) to deal with computation-intensive Update operations. NMP-enabled DIMMs are connected to CAE’s four memory channels, each containing a Near-Memory Engine (NME) for memory-intensive Reduce operations. Such a CAE/NMEs hybrid architecture matches the heterogeneous nature of GNN training. More importantly, we can scale up the capacity, processing ability, and aggregated memory bandwidth by connecting more DIMMs to the memory channels.

Base Workflow: Figure 6 depicts the base workflow of GNNear. The input features of graph $G$ in Figure 6-(a) are initially stored in DRAM. We partition $G$’s vertices evenly and assign them to different DIMMs. In the figure, we use two DIMMs (DIMM-0 and DIMM-1) for illustration, which hold the data of blue and grey vertices, respectively. According to the GNN training flow introduced in Section 2, we traverse every destination vertex (e.g., $v_5$ in Figure 6-(b)) in each forward and backward step and conduct Reduce or Update operations. For Reduce, CAE sends customized instructions through the memory interfaces to NMEs. NMEs decode the instructions and perform partial reduction with the assigned source vertices locally (e.g., $\text{DIMM-0}$ and $\text{DIMM-1}$ compute feature vectors $a'_0$ and $a'_1$, respectively). Then, the partial results are read out by CAE (operation $\mathcal{1}$ in the figure). CAE merges these partial results (i.e., $a'_0 + a'_1$) to get the final reduction results. For Update, CAE computes with the merged results buffered on-chip or directly reads the required data without near-memory reduction. The updated features or gradients will be written back to DRAM if necessary (operation $\mathcal{2}$). After a training epoch, CAE updates the model weights with accumulated weight gradients. As Figure 6-(c) shows, in each epoch we process Reduce and Update operations of the adjacent destination vertices in a pipelined manner since...
they have no data dependency. Such a training process executes for many epochs until convergence.

With such a near-memory reduction workflow, the Reduce operations in Equation 6 are then changed to

$$Y'_v = \sum_{u \in \bar{N}(v) \cap \text{DIMM}_i} \text{edge}_w(u, v) \cdot X_u, \quad Y'_o = \sum_{i=1}^{\#\text{DIMMs}} Y'_v$$

The off-chip data read is reduced from the original $|\bar{N}(v)| \times d$ to no more than $\#\text{DIMMs} \times d$ for vertex $v$. The latter is usually much smaller than the former. Considering that NMEs in different DIMMs work in parallel, GNNear can utilize the high aggregated local bandwidth. Moreover, for computation-intensive Update operations, CAE provides sufficient computation capacity.

### 4.2 CAE Architecture

Centralized Acceleration Engine (CAE) is mainly responsible for the computation-intensive Update operations. It also merges partial reduction results $Y'_o$ produced by NMEs. As shown in Figure 5, CAE has both a GEMM engine (implemented with systolic array architecture) and a vector-processing unit (VPU). A scratchpad memory is equipped to buffer the temporary data and model weights. Four customized memory controllers support sending GNNear instructions to NMEs. A controller (can be implemented with an OoO RISC-V or ARM core) schedules the whole training process according to the input graph’s adjacent matrix and the model’s configuration. A high-bandwidth on-chip network connects all the components.

### 4.3 NME Architecture

The Near-Memory Engine (NME) resides in the buffer chip of DDR4 LR DIMM [69]. Each NMP-enabled DIMM equips one NME. In Figure 5-(c), we mark the customized components with blue. There are five main components: Instruction Register, Instruction Decoder, Execution Unit, Data Buffer, and a Controller. NME receives NMP instructions from CAE and puts them in the Instruction Register. Instruction Decoder decodes each instruction. Then, the lightweight controller starts local execution following the instruction. The Execution Unit handles data calculation. The controller is also responsible for generating regular DDR4 Command/Address and data signals (DDR.C/A and DDR.DQ) and sending them to all DRAM devices across parallel ranks in a DIMM (two ranks in the example). Since NMEs can access their local DRAM devices in parallel, the aggregated local bandwidth is much higher. Furthermore, we equip an SRAM data buffer in NME to explore data locality in graph structure (Section 4.4). Apart from near-memory processing, if NME receives standard DDR commands from the CAE-side memory controller, it will bypass execution units and directly conducts Read/Write/Precharge commands, etc.

The Execution Unit (EU for short) in each NME is responsible for near-memory partial reduction computation of Reduce operations. According to Equation 8, partial reduction is formulated as the weighted sum of $n$ feature/gradient vectors: $Y'_o = \sum_{i=1}^{\#\text{DIMMs}} \text{edge}_w(u, v) \cdot X_u$, where $\text{edge}_w$ denotes edge weight (scalar). For GCN, the edge weight is $1$. For GAT, it is an estimated importance factor. As shown in Figure 7, The EU adopts an intra-feature parallelism data flow. There are in total $m$ PEs, each computing eight elements every cycle. The results are added to partial sums stored in registers. Since each element in a vector $X_u$ shares the same edge weight, $\text{edge}_w$ is broadcast to all multipliers. Therefore, $m$ PEs compute $8 \times m$ elements of a vector in parallel. If $X_u$ is longer than $8 \times m$, it needs multiple rounds to finish the computation. EU
We design GNNear-ISA to drive the shard-based near-memory re-
erations. Partial results of $\mathbf{X}$ vertex data is loaded from DRAM devices (L-Type instruction) and then used in near-memory calculations (C-Type instruction). We partition the $R \times C$ shards into multiple R $\times$ C shards and process each shard separately. For each shard, we first load $R$ source vertices from DRAM (e.g., operation ①), then compute the partial results of $C$ destination vertices ($Y'_4, Y'_5$) are also reused by the following shards of the same column. Therefore, we have to buffer $R$ source vertices and $C$ partial sum on-chip, requiring at least $(R + C) \times d$ space. As shown in Figure 9, setting $R = 1$ and $C = 127$ brings the lowest DRAM access on both Amazon [16] and Reddit [35] datasets. It is easy to explain such a result: the $R$ dimension affects inter-shard source vertex reuse. For example, in Figure 8, if $R = 4$ then source vertex data $X_1, X_4$ (as read in step 1 and 4) can be loaded on-chip and can be reused by the following shards of the same column. Therefore, we have to buffer $R$ source vertices and $C$ partial sum on-chip, requiring at least $(R + C) \times d$ space. We assume that at most 128 data vectors can be buffered on-chip and different partial sum from different columns. As shown in Figure 9, setting $R = 1$ and $C = 127$ brings the lowest DRAM access on both Amazon [16] and Reddit [35] datasets. It is easy to explain such a result: the $R$ dimension affects inter-shard source vertex reuse. For example, in Figure 8, if $R = 4$ then source vertex data $X_1, X_4$ as always on-chip from step 1 to step 11. However, for real graphs with millions of vertices, it is natural to set $R = 1$ and $C = 127$ for the best inner-shard source vertex reuse. We call it Narrow-Shard Strategy. Moreover, the Narrow-Shard strategy supports skipping empty shards to save useless data read (e.g., step 8 to step 9 in Figure 8 skips two empty shards and avoids loading $X_2, X_3$).

4.5 Instruction Set Design

We design GNNear-ISA to drive the shard-based near-memory re-
erations. Figure 10 shows the base GNNear-ISA consists of three types of instructions: L-Type: L-Type instruction loads vertex data from DRAM devices to NME’s data buffer. According to our Narrow-Shard strategy, one data vector $X_u$ of vertex $u$ is loaded each time. Therefore, L-type instruction has Daddr and Vector_Size fields to indicate the start and address size of vertex $X_u$. NME’s controller generates standard DDR read commands according to the received L-type instruction and sends them to DRAM devices to load the data. For standard DDR4 with a burst length of 8 (Bl:8), loading a vector longer than 64B demands multiple burst-read commands.

R-Type: R-Type instruction is used to read out partial results from NME’s data buffer upon all shards within the same interval (namely a column of shards) finish computing. The Dst_Index field in L-Type (denotes the destination’s relative index within a shard) and add it to the partial results $Y'_v$. Taking operation ② in Figure 8 as an example, we multiply edge weight $e_{4-5}$ and vertex $v_5$’s data $X_4$ and then index $v_5$’s partial results $Y'_v$ with Dst_Index = 0 ($v_5$ is the first destination vertex within the shard). C-Type instructions rely on CAE to analyze the adjacent matrix and determine which edge should be processed. CAE is also responsible for calculating the edge weights. Such a design keeps the NME-side controller as light-weighted as possible.

R-Type: R-Type instruction is used to read out partial results from NME’s data buffer upon all shards within the same interval (namely a column of shards) finish computing. The Dst_Index and Vector_Size bits jointly determine which bytes to read. A sequence of R-Type instructions will be issued to read out multiple destination vertices of an interval.

All instructions have DIMM fields indicating which DIMM should receive the instruction. Since R-Type and C-Type operations do not involve DRAM data access, their latency is determined and denoted as $\text{NME_RD}$ and $\text{NME_CD}$, respectively. The L-Type instruction is decoded into standard DDR commands to read data from DRAM devices. Our data mapping guarantees that the feature bytes of a vertex will always be mapped into the same DRAM row. Thus, the latency is $tCL + \frac{\text{Vector Size}}{\text{Burst Size}} \times tBL$ (row buffer hit) or $tRC + tBCD + tCL + \frac{\text{Vector Size}}{\text{Burst Size}} \times tBL$ (row buffer miss). CAE’s memory controllers rely on these timing constraints to schedule NMP instructions. More importantly, since all the instructions are issued by CAE and then executed by NMEs under predetermined timing constraints, the NMEs do not require any explicit synchronization.

4.6 Data Mapping

Figure 11 demonstrates the base data mapping. The intermediate data during GNN training can be accessed using indexes composed by $\text{Vertex_Index}\times\text{Type}\times\text{Data}$. Data indexes the bytes within a vector. Type indicates the data’s type, including feature $h_u$, gradients...
\[ \delta_n \text{ or aggregation results } \delta_n, \text{ etc.} \] We split a vector to the parallel ranks of each DIMM for higher local bandwidth. Each sub-vector is stored sequentially in a DRAM row. Consecutive vectors are also stored in the same row. Thus, the adjacent shards are more likely to read source vertex from the same activated row (open-page policy). We store adjacent vertices in different banks for better bank-level parallelism. Note that the mapping can be adjusted according to different tasks and system configurations. For example, we can assign more column bits to Data field to hold longer feature vectors.

5 Optimizations

The proposed GNNear architecture and base workflow perfectly match the algorithmic structure of full-batch GNN training. However, it can hardly handle the irregularity of input graphs and will thereby suffer from resource under-utilization and load-imbalance problems. Therefore, we propose several optimization strategies further to improve GNNear’s performance.

5.1 Hybrid Graph Partition

The base partition strategy (Figure 6) places source vertices to DIMMs evenly. However, some real-world graphs contain enormous low-degree vertices. For instance, in Figure 12, about 50% of vertices in the Amazon graph have degrees \( \leq 25 \) (Reddit only has 12%). Too many low-degree vertices will cause severe resource under-utilization problems. An extreme case is that vertex \( v \) has 16 neighbors placed in 16 different DIMMs. Since each DIMM only contains one neighbor vertex, NMEs cannot perform the partial reduction, heavily under-utilizing the rich local bandwidth. Uneven graph partition considering graph structure information can potentially improve data locality [11, 16, 99]. Therefore, we propose a simple yet practical Hybrid Graph Partition (HGP) strategy. According to the power-law hypothesis [72], in real-world graphs, the neighbors of low-degree vertices are probably the same super-nodes. In other words, there are some “dense” rows in a graph’s adjacent matrix. Each element in these rows will incur a partial result readout operation, if these rows are placed in different DIMMs. Alternatively, we can put them into the same DIMM to improve the data locality. However, simply consolidating high-degree vertices will also cause load-imbalance problems. We choose to duplicate high-degree vertices and let each DIMM compute different destinations.

As shown in Figure 13, all vertices are still evenly partitioned among memory channels. In each channel, we evenly partition the low-degree vertices (Mode-(a)). For high-degree vertices, we duplicate them to all DIMMs and assign the computation tasks to distinct DIMMs (Mode-(b)). The red circles denote the saved vertex read (we only mark one column). Such a hybrid partition strategy reduces the data read via channel-0 from 26 to 15 in the example. We use an adjustable parameter \( \lambda \) to control the duplication ratio and ensure it will not exceed the DIMMs’ capacity. HGP can be executed offline before deploying a training task to GNNear.

Hardware Support: After adopting the HGP strategy, we have to update all the duplicated vertices, incurring more off-chip data write operations via the low-bandwidth memory channels. To tackle this challenge, we propose to update duplicated vertices using broadcast-write operations. It is feasible to support broadcast-write in a DIMM-based system since all the devices in a channel are connected to the same data and C/A buses [92]. As Figure 14 shows, we extend the GNNear-ISA and add a B-Type instruction. Unlike the other three instructions, a B-Type instruction is received and executed simultaneously by all the DIMMs in a channel. After receiving a B-Type instruction, NMEs’ controllers know that the following memory write commands are broadcast-write commands and ignore the DIMM fields in the address. As shown in the timing diagram, a single WR command following a B-Type instruction will write the same data to multiple DIMMs. To achieve this, we also place the duplicated data in the same area in each DIMM. Moreover, since we only duplicate high-degree vertices within each channel, no inter-channel broadcast is needed. The overhead of extra memory access incurred by HGP is estimated in Section 6.3.

5.2 Load-balanced Interval Scheduling

According to GNNear’s base workflow and the Narrow-Shard strategy, GNNear computes intervals sequentially (‘Interval’ denotes a column of shards computing the same destination vertices). The CAE will not send instructions for interval \( i + 1 \) before finishing interval \( i \). However, the irregularity of graphs can make the assigned shards within an interval vary among DIMMs, causing load-imbalance problems. The main idea to tackle such a problem is to start the processing of the next intervals on those idle DIMMs. To make such an idea practical, we apply the following two techniques: Window-based Scheduling: To efficiently manage the concurrent intervals, we propose a Window-based Scheduling strategy. As Figure 15 shows, we set several result FIFOs and a window buffer in CAE. Each FIFO receives partial reduction results from a single DIMM, which will be merged with the partial results stored in the
window buffer. We allow the CAE-side controller to issue instructions for interval \( i + 1 \) immediately after a DIMM finishes interval \( i \), if interval \( i + 1 \) is within the Processing window. The partial results in FIFOs will be merged with that stored in the window buffer. Once every DIMM’s results of interval \( i \) are merged, CAE commits interval \( i \) and right-shifts the Processing window. By this means, we can schedule multiple intervals concurrently and mitigate the load-imbalance problems caused by graphs' irregularity.

**Intervals Interleaving:** Our HGP strategy (Figure 13) divides an interval into two parts: the low-degree part and the high-degree part. According to the original interval index, the high-degree parts in the first four intervals (we assume a shard size of 1 for simplicity) will both be processed by DIMM-0, making it overloaded if we execute these intervals concurrently. We mitigate this problem by interleaving intervals among DIMMs. We reorganize the interval indexes and ensure that the adjacent intervals rely on distinct DIMMs to process the high-degree parts.

### 5.3 Other Optimizations

**Inter-Shard Overlapping:** In Figure 8, each shard needs a load (L-Type) and multiple edge calculation (C-Type) operations. If they are executed sequentially, either the memory devices or the execution unit will be idle at a certain time. To improve resource utilization, we consider overlapping L-Type and C-Type instructions of the adjacent shards. We use Step-5 and Step-6 in Figure 8 as an example. As shown in Figure 16, suppose the vector size is 128B, after two burst reads, \( v_2 \)’s vector has been loaded to NME’s data buffer. Then the calculation of \( e_2 \)–3, \( e_2 \)–4 can be launched immediately. In the meantime, the CAE-side controller issues the load instruction for Step-6, which is executed by NME concurrently. Step-6’s data loading overlaps with Step-5’s computing. This strategy increases the utilization of both the execution unit and DRAM devices and is easy to implement since all the operations have determined timing (Section 4.5), and we only schedule the two adjacent shards.

**Interchange the Execution Order:** Finally, for some tasks the input feature can be much longer than the hidden feature. For example, Reddit’s input feature length is 602, while the hidden size is usually 128 or 256. Actually, if aggregators are linear, the execution order of aggregation and combination can be exchanged to reduce DRAM access and save NME’s data buffer. For instance, we can calculate the combination first: \( \sum_{u_t} a_{i,u} \cdot v_{1} \), then aggregation: \( h_{i,v} = \sigma(\sum_{u_t} N(u) \frac{a_{i,u}}{N(u)} \cdot d_{u}^v) \). The original execution order incurs roughly \( 2 \times |E| \times d_1 + |V| \times d_2 \) DRAM access for the first layer, where \( d_1 \) and \( d_2 \) denote the input and output feature dimensions. After interchanging the execution order, the memory access becomes \( 2 \times |E| \times d_2 + |V| \times d_1 \). Since \( |V| < |E| \), the data access reduces about \( \frac{d_2}{d_1} \times x \). With hidden size = 256, the theoretical DRAM access reduces roughly 2.3× for Reddit.

### 6 Evaluation

#### 6.1 Methodology

**System Configuration:** Table 4 summarizes the system parameters of the GNNear prototype. For the memory system, each channel equips four DDR4-2400 LRDIMMs. According to Micron’s LRDIMM datasheet [69], each DIMM has a 32GB capacity. In total, GNNear equips 512GB of memory, which is much larger than that of V100 GPU. The timing setup is also based on this datasheet. For NME, we set 16 PEs. Each PE contains eight MACs. Running at 500MHz, an NME provides a peak performance of 128GFLOPS. For CAE, we adopt a 128 x 128 systolic array as the GEMM engine, providing about 22TFLOPS computation capacity running at 0.7GHz. The VPU is composed of 32 SIMD-16 cores and has 700GFLOPS peak performance. The scratchpad memory is 16MB, which can be flexibly divided into weight buffer, input/output buffer, edge buffer, window buffer, etc. We adopt BF16 as the data format. BF16 has the same accuracy as FP32 for NN training [47] but is more cost-efficient. We estimate CAE and NME’s area and power using 16nm and 28nm technologies, respectively. The GEMM and VPU’s area and power are measured according to TPU-v2 [45, 78], and HyGCN [105]. To estimate the overhead of NME’s logic parts, we write EU with Chisel and synthesize the generated RTL using Synopsis Design Compiler 2016 under TSMC 28nm. We get the area and power of all SRAM buffers with CACTI [76].

| Table 4: System Parameters and Configurations |
|-----------------------------------------------|
| **Memory System Configuration**               |
| DDR4-2400, 32GB LRDIMM, 4 channels x 4 DIMMs x 2 ranks | FR-FCFS, 32 entry RD/WR queue, Open policy |
| **DRAM Timing Parameters**                    |
| tRC=56, tRCD=17, tCL=17, tRP=17, tBL=4        |
| tCCD_S=4, tCCD_L=6, tRCD_S=4, tRCD_L=6, tFAW=26 |
| **NMP Parameters**                            |
| Data Buffer                                   |
| 256KB, Dual Ports, Word size = 16B            |
| Area = 0.44 mm², Power = 80.0 mW              |
| Execution Unit                                |
| 16 PEs, 8 MACs per PE @500MHz                 |
| Area = 0.42 mm², Power = 178.1 mW             |
| **CAE Parameters**                            |
| GEMM Engine                                   |
| 128x128 Systolic Array @700MHz                 |
| Area = 27.3 mm², Power = 6291.4 mW            |
| VPU                                           |
| SIMD-16 Cores x32 @700MHz                     |
| Area = 0.82 mm², Power = 296.6 mW             |
| Scratchpad Memory                             |
| 16MB, 8 Banks, Dual Ports, Word size = 64B    |
| Area= 33.7 mm², Power = 5519.2 mW             |

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components of NME incur moderate area (0.86 mm²) and power (258.1mW) overhead, given that a single DIMM usually consumes several watts and the buffer chip takes up about 100 mm² [68].

**Simulation Methodology:** To evaluate the performance of GNNear, we implement a customized GNN training framework to support our narrow-shard-based training dataflow given a graph’s adjacent matrix and the model’s configuration. It generates Reduce, Update, and other operations and sends them to a GNNear simulator. Specifically, we extend DRAMsim3 simulator [58] to support cycle-accurate near-memory reduction simulation. It is customized to support GNNear-ISA and takes NME’s timing constraints and power consumption into consideration. Note that the DRAMSim3 simulator is too slow to evaluate large graphs which even have billions of edges. Therefore we also develop a coarse-grained simulator. The CAE and VPU cycles are calculated according to their parallelism and the size of features. We model on-chip buffers’ access latency using CACTI [76] and inject these parameters into our simulator.

**Benchmarks:** Table 5 lists four benchmarking graphs, namely Ogbn-Proteins (PT) [93], Reddit (RD) [35], Yelp (YP) [111], and Amazon (AM) [16]. PT and RD are dense graphs, while YP and AM are relatively sparse. We adopt four aforementioned GCN models as benchmarking models. In the default configuration, each model has two layers with a hidden size of 256.

**Baselines:** Since there is no other full-batch training accelerator at present, we mainly compare GNNear with CPU/GPU platforms using the popular DGL framework [19]. We adopt a DGX-1 workstation equipping Xeon E5-2698-v4 CPU (4 Channels, 256GB DDR4-2400) and V100 32GB GPUs to evaluate the performance of DGL-CPU (MKL-2020.2) and DGL-GPU (CUDA-10.2/cudnn 7.6). Considering that GNNear adopts the BF16 data format (two Bytes per element) while the CPU/GPU baselines all use FP32 (four Bytes per element), we double the vector size when simulating GNNear’s data transmission for fair comparisons.

### 6.2 Main Results

**Training Throughput:** We first estimate the training throughput of GNNear and the CPU/GPU baselines. The performance is measured with end-to-end training seconds per epoch and then normalized to the CPU baseline. As depicted in Figure 17, DGL-GPU suffers from the OOM problem on the AM-GIN task due to GPU’s limited memory capacity. Though DGL-CPU successfully tackles all tasks with 256GB memory, it shows low training speed due to its limited memory bandwidth and computation capacity. GNNear demonstrates superior training speed compared to these two baselines. Specifically, GNNear achieves 30.8× and 2.5× geometric mean speedup compared to DGL-CPU and DGL-GPU, respectively.

**Energy-efficiency:** We measure GNNear’s per-epoch energy consumption and compare it with CPU/GPU baselines. The CPU system’s energy is directly estimated with PyRAPL [79]. We test the GPU’s running power using PyNVML [84] and then calculate the energy with the product of average power and per-epoch time. All values are also normalized to the CPU baseline. As shown in Figure 18, GNNear achieves 79.6× and 7.3× higher energy efficiency (geometric) compared to CPU/GPU platforms. High training throughput and low power consumption brought by the ASIC engine and saved data transmission with near-memory reduction jointly lead to GNNear’s extraordinary energy efficiency.

### 6.3 Performance Analysis

**Speedup Breakdown:** To better understand the effect of different design points, we demonstrate the speedup breakdown in Figure 19-(a). Evaluations are performed on AM-GCN task and the performance is normalized to the CPU baseline. As we can see, directly adopting CAE for GNN training gets 3.6× speedup, thanks to CAE’s higher performance over CPU. Performing near-memory reduction brings 3.8× speedup via utilizing the high aggregated in-DIMM bandwidth. Adopting the Narrow-Shard strategy to explore data reuse brings 1.1× speedup thanks to the reduced local DRAM access. The HGP strategy and load-balanced interval scheduling further contribute to 1.2× speedup. At last, inter-shard overlapping...
contributes to 1.1x speedup further by mitigating the idle time of NMEs. Note that for different tasks, these proposed optimizations show diverse impacts on GNear’s performance (for instance, RD graph gets much higher speedup from the Narrow-Shard strategy. Since AM does not need to interchagne the execution order to save memory access, we evaluate the Interchange Execution Order (IEO) strategy on RD. As shown in Figure 19-(b), IEO successfully brings 1.5x speedup on the RD-GCN task thanks to the reduced memory access in the first layer. Generally, our designs and optimizations demonstrate significant effectiveness in accelerating GNN training. 

**Roofline Analysis:** We adopt a roofline model to analyze the performance of GNear and DGL-CPU baseline on the Gin model. As shown in Figure 20-(a), the X-axis represents the operational intensity, while the Y-axis is the performance (both in log scale). The Xeon E5-2698-v4 CPU and GNear both have four memory channels, providing 76.8 GB/s bandwidth. We plot four operations using this model: CPU-Update, CPU-Reduce, GNear-Update and GNear-Reduce. As we can see, CPU-Reduce suffers from the low arithmetic intensity and is bounded by the limited memory bandwidth (the left-most triangle). In comparison, GNear’s near-memory reduction mechanism provides up to 8x higher aggregated local bandwidth. Moreover, the Narrow-Shard strategy increases the arithmetic intensity of Reduce operations. Therefore, GNear-Reduce achieves 14.5x higher performance compared to CPU-Reduce. Besides, GNear-Update also shows 25.4x speedup against CPU-Update due to the more powerful CAE and higher arithmetic intensity by buffering all the weights on-chip. 

**DRAM Access Saving:** By performing near-memory reduction, the data read via memory channels is substantially reduced. According to our profiling, the evaluated graphs can benefit from 71.3% to 97.2% off-chip memory-read saving by adopting near-memory processing, which dramatically reduces the system’s energy consumption. Assuming the off-chip IO cost is 22pJ/b, and the on-chip DRAM read cost is 14pJ/b [48], about 43.6%-59.4% of total data read energy is saved. We illustrate the number of read/write instructions of AM-GCN task under different settings (without NMP, NMP without broadcast write, NMP with broadcast write) in Figure 20-(b). As we can see, on the representative AM-GCN task, the HGP strategy incurs 1.05x extra off-chip DRAM write with a λ of 0.35 (The orange bar in the middle of Figure 20-(b)). Fortunately, as shown by the NMP+BW column in Figure 20-(b), the proposed broadcast write mechanism eliminates the extra off-chip data write and ensures that the write-back operations will not be the bottleneck. Therefore, the energy cost incurred by broadcast-write operations is merely about 8.4% of memory access energy. 

### 6.4 Design Space Exploration

**Shard Size & Window Size:** To understand the impact of shard size and window size on GNear’s performance, we first keep window = 4 and set shard from 1 to 256, and evaluate the training speedup on GCN tasks. As Figure 21-(a) shows, RD and PT are more sensitive to shard size, while the speedup on AM and YP is quickly saturated as the shard size increases. Considering that a large shard demands much more NMEs’ data buffer, we set shard = 128 in our prototype. We then explore window from 1 to 32. In Figure 21-(b), RD benefits a lot from a large window. The speedup on all the tasks increases first and then reaches a plateau. Since the space complexity of window buffer is shard $\times$ window $\times$ d, it is better to set the window size to a relatively small value (e.g., window = 4 in our prototype) to save CAE’s area and energy. 

**Duplication Ratio:** We explore HGP’s duplication ratio $\lambda$ from 0 to 0.5. As depicted in Figure 21-(c), YA and AM obtain considerable speedup from duplicating high-degree vertices. However, RD is not sensitive to $\lambda$, and PT even gets a lower speed. We infer that this is because PT and RD are dense graphs and do not have enough low-degree vertices (as Figure 12 shows, in RD, only 12% of vertices have degrees ≤ 25). The baseline even-partitioning strategy already works well. Duplicating vertices only increases their load imbalance. Therefore, we choose not to duplicate vertices on PT and RD and tentatively set $\lambda = 0.35$ on AM and YA. 

**Ranks Per DIMM:** An NME can access ranks in parallel to achieve $\#Rank \times$ higher local bandwidth. To study the benefits of rank-level parallelism, in Figure 21-(d), we explore the number of ranks per DIMM from 1 to 8. The speedup will also be saturated when near-memory reduction is bounded by the channel bandwidth or NME’s computation capacity. Adding multiple ranks in a DIMM and driving them in parallel will increase the complexity of NME’s...
interface and control logic. Therefore we consider two ranks per DIMM in our prototype.

6.5 Comparisons with Roc and DistGNN

We notice that there are some distributed GPU/CPU-based full-batch GNN training systems, such as Roc [44] and DistGNN [67], which support deep GNN models (more than two layers) and even super large graphs like Ogbn-Papers [41]. To compare with them, we add routers to CAE and connect multiple GNNear accelerators with a switch and also build a Multi-GNNear system. As shown in Figure 22, we partition the graph evenly and assign the sub-graphs to different accelerators (four GNNear accelerators are named G-0 to G-3). Each accelerator further partitions the sub-graph to its connected DIMMs. We assign Reduce and Update operations concerning different destinations to each accelerator. Moreover, accelerators transmit locally-merged partial results to each other to save inter-chip communication.

We evaluate the performance of Multi-GNNear by extending our simulator. Table 6 lists the parameters of the three systems. We assume the switch of Multi-GNNear has the same bandwidth as Roc’s NVLink. We adopt the same model and graph settings from their papers and use their reported performance numbers for comparison. In general, Multi-GNNear achieves about 3.1x speedup on Ogbn-Papers (OP) dataset (3-layer GCN, hidden size = 256) and is also 1.6x faster on AM than DistGNN with 32 CPU sockets. On deep model tasks (four-layer GCN), Multi-GNNear achieves about 2.1x speedup on AM dataset and 1.08x speedup on the RD dataset, compared to the Roc system built with eight V100 GPUs.

6.6 Comparisons with Rubik and GraphACT

Comparison with Rubik: Rubik [11] can also be used for GCN training. The main idea of Rubik is using LSH hashing to reorder the input graphs for better data locality. However, the effect of graph reordering purely depends on the pattern of graphs. The heavy pre-processing overhead (more about ten seconds on Reddit) also restricts its adoption to offline applications [30]. GNNear reduces DRAM access through near-memory processing which is a more generic solution. The pre-processing step required by HGP is more than 5x faster than Rubik, according to our evaluation. Such a light-weighted pre-processing can even be omitted when training on dense graphs (see Section 6.4).

Comparison with GraphACT: GraphACT is the state-of-the-art mini-batch GCN training accelerator, which is implemented on FPGAs. With the proposed GraphSAINT [112] mini-batch training algorithm, it reports 95.2% accuracy on the Reddit dataset. However, for full-batch training, we can achieve 96.9% accuracy [44], about 1.7 points higher than mini-batch training. GraphACT cannot support full-batch training on large graphs due to the limited memory capacity of FPGAs. Therefore, GNNear can easily outperform GraphACT in accuracy. Moreover, unlike GNNear adopting HGP strategy, GraphACT can hardly handle low-degree graphs [11].

7 Related Work

GNN Acceleration: Recently, plenty of GNN accelerators have been presented [11, 29, 57, 59, 60, 75, 89, 100, 105, 114, 121] for efficient GNN inference. As far as we know, GraphACT [109] is the only GNN training accelerator but it just supports mini-batch training on middle-scale graphs like Reddit and Yelp. Our GNNear accelerator targets the more accurate but challenging large-scale full-batch training tasks. Besides, there are also several mini-batch/full-batch training frameworks [7, 14, 23, 44, 66, 67, 73, 94, 95, 123]. They are based on general-purpose CPU/GPU platforms and cannot benefit from domain-specific hardware.

DRAM-based Near-Memory Processing: Many near-memory processing accelerators using 3D/2.5D-stacked memory have been proposed for graph processing [2, 18, 74, 118, 124], DNN acceleration [25, 38, 50, 54, 61, 86, 98, 106], GCN inference [8] or general-purpose applications [21, 24, 33, 40, 102, 116]. Due to the limited memory capacity (≤128GB) and high cost, 3D/2.5D-stacked NMP is not suitable for full-batch GNN training. Chameleon [5] proposes to adopt LRDIMMs [69] to break NMP’s capacity limitation. Several follow-up works adopt this paradigm to build efficient recommendation systems [4, 48, 49, 55, 77] or accelerate extreme classification [62]. Recently, Samsung has also disclosed a concept DIMM-NMP product called AXDIMM [51], which still adopts recommendation system as its killer application. Our work is the first to leverage DIMM-NMP to accelerate full-batch GNN training.

8 Conclusion

In this paper we propose GNNear, a hybrid accelerator architecture leveraging near-memory processing to accelerate full-batch GNN training on large graphs. GNNear matches the heterogeneous nature of GNN training by offloading the memory-intensive Reduce operations to in-DIMM Near-Memory-Engines (NMEs) and using a Centralized-Acceleration-Engine (CAE) to process the computation-intensive Update operations. To deal with the irregularity of graphs, we also propose several optimization strategies concerning data reuse, graph partitioning, and dataflow scheduling, etc. Evaluations on 16 tasks demonstrate that GNNear achieves 30.8x / 2.5x geomean speedup and 79.6x / 7.3x (geomean) higher energy efficiency compared to Xeon E5-2698-v4 CPU and V100 GPU.

Acknowledgment

We thank all the reviewers for their valuable comments. This work is supported by NSF of China (61832020, 62032001, 92064006), Beijing Academy of Artificial Intelligence (BAAI), and 111 Project (B18001).
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