EDSU: Error detection and sampling unified flip-flop with ultra-low overhead

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Abstract: EDAC (Error Detection and Correction) techniques guarantee PVT variation safety by dynamically fixing timing error instead of providing static margins. However, previous EDAC works introduce additional area, power and performance penalty, thus the benefit from timing margin eliminating is limited. In this paper, we propose a novel EDAC Flip-Flop, EDSU, with ultra-low area overhead and nearly zero performance penalty. EDSU utilizes only two more transistors than conventional D-Flip Flop and can correct timing error simultaneously with detection. The ultra-lightweight property can obviously reduce area overhead and clock load, thus improve the variation tolerance ability and energy efficiency. EDSU is implemented in a commercial processor at SMIC 40 nm technology to evaluate its benefits. Simulation result shows EDSU inserted system gains 12.5% more performance at fixed voltage, 25% more variation tolerance and 10.5% energy saving at fixed throughput than state-of-art EDAC work.

Keywords: ultra-low overhead, EDAC, unified sampling, time-borrowing, timing error tolerance

Classification: Integrated circuits

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1 Introduction

Because of CMOS material’s natural sensitivity to environment changing, variations from process, voltage, temperature, age and noise generate lots of timing faults to sequential logic based digital ICs. To maintain reliability and robustness, traditional industrial IC designs add timing margins to circuits under the most pessimistic estimation: worst-case PVT convergence. However, timing margins provide not only safety but also area and power overhead [1]. Another fact is, most circuits are produced typically and usually work at normal environment condition, so the static margins can only waste area and power at most of time. As CMOS technology shrinks and supply voltage scales down, margin requirement is explosively growing. Smaller transistor size introduces more randomness to lithography and lower supply voltage means nearer to threshold: all the negative circuit effects are enlarged [2].

To address this problem, researchers have proposed several solutions to eliminate static circuit margin. “Canary” [3, 4] uses replica critical paths to act as variation sensor: if the “canary” nodes have detected timing error, the whole system is also assumed to be dangerous and global dynamic voltage/frequency scaling (DVFS) will be applied to fix it. This approach is effective for global variations but not for local variations because the detect point cannot precisely measure the variation of every critical path all over the chip.

Another solution, which is well known as EDAC, detects data transition at the ending point of critical path, and correct the timing error through architectural methods or DVFS. By observing timing error at the exact violation point, EDAC techniques can resolve global variations as well as local variations in an “in-situ” way. Several EDAC latches and flip-flops have been proposed in recent years, and the most representative techniques are the “Razor” series: Razor I [5], Razor II [6], TDTB [7] and Razor-Lite [8], et al. In benefit of the margin eliminating from
EDAC, Razor systems have shown obvious energy reduction and efficiency improving.

However, previous EDAC latches/flip-flops introduce significant area overhead to every timing error monitor; the architectural correction methods also harm system performance due to CPI penalty brought by instruction replay/counterflow. With the development of current digital IC design, the critical path distribution becomes much tighter [8], and more balanced pipeline means the probability of timing error rises higher under same degree of variations.

In order to decrease area overhead as well as performance penalty of EDAC techniques, in this paper, we propose an ultra-low overhead error detection and sampling unified (EDSU) flip-flop with only two additional transistors to DFF. The time-borrowing based error correction scheme reduces CPI penalty to nearly zero, so the variation adaptability can be expanded from higher error rate. We implement EDSU in a commercial processor, and simulation results show EDSU inserted system gains 12.5% more performance at fixed voltage, 25% more voltage variation tolerance and 10.5% energy saving at fixed throughput than state-of-art EDAC work.

The rest of the paper is organized as follows. Chapter 2 describes the related works of EDSU. Chapter 3 introduces the design concept, circuit structure and detailed working sequence of EDSU. Chapter 4 gives design of EDSU inserted CK802 system. Chapter 5 presents the simulation result of an EDSU inserted commercial processor, and finally chapter 6 summarizes conclusion of the paper.

2 Related works

To address the area/performance problem, several new EDAC flip-flops are proposed in recent years. Razor-Lite [8] uses two virtual rails inside the conventional flip-flop to observe timing error, and 8 transistors are added to generate error signal. As 28–44 additional transistors are introduced in previous EDAC works, Razor-Lite has made a major step for area overhead reducing. On the other side, it utilizes instruction replay scheme to correct error, and 11 cycles are wasted on every timing fault. Instruction replay also demands pipeline control logic modification, and this will increase the complexity of system integrating.

R-Processor [9] comes up with a two-phase latch based design, the CPI penalty is greatly relieved and pipeline control logic need not any modify. Based on the “sparse error detection”, the area overhead is largely reduced from original high inserted rate of EDAC cell. The dynamic timing error rate can also be reduced thanks to the decrease of detected nodes. But EDAC cell in R-Processor adds 4 more transistors than Razor-Lite to ensure working safety under ultra low voltage, which means the area overhead of EDAC cell still needs to be reduced further.

The newly presented iRazor [10] has carried on to reduce transistors in EDAC cell, it has managed to detect timing error through only 1.48 equivalent additional transistors. Global clock gating is used after error correction to guarantee the time-borrowing safety. However, effective detection window is reduced to the width of “CTL” signal, and the implementation of CTL generation circuit requires precise reference to both clock edges to maintain correct function and it may need to be
reconfigured manually under different PVT variation. The global clocking gating correction is also harmful because it consumes one additional clock cycle on every timing error.

3 EDSU circuit design

Conventional master-slave DFF is consist of two latches to build the edge-trigger behavior. EDSU presents a new unified approach for error correction and normal sampling, by using only one latch along with several EDAC transistors, and accomplishes functions of conventional DFF as well as EDAC cell. Those EDAC transistors can assign input value in feedback loop of the only latch directly on detecting of inconsistency between input and output: when it is detected at clock rising edge, the assignment acts as normal sampling; when it is detected in high clock phase (the error detection window), the assignment acts as error correction.

3.1 EDSU circuit structure

The circuit structure of EDSU is shown in Fig. 1. Two internal nodes of $TINV1$, $VVDD$, and $VVSS$, can be used as two virtual supply rails [8] for transition observation: one of them will be charged/discharged when transition of $D$ is detected at high clock phase. After $VVDD$ and $VVSS$ flag timing error out, EDSU uses the error information to replace the stored value with the detected value. Note that “0” value and “1” value are detected and stored separately through $VVDD$ and $VVSS$.

![Fig. 1. Circuit structure of EDSU.](image)

The detailed working sequence is simulated by SPICE, and the waveform is shown in Fig. 2. In normal situation, $VVDD$ and $VVSS$ keeps their original potentials and they will flag timing error out when $D$ changes in high clock phase. For example, if the previous value of EDSU is “1”, the value of $S$ should be “0” and $DN$ is also “0” in high clock phase through $TG$. When $D$ “1->0” transition occurs at high clock phase (corresponding to “1->0 error” in Fig. 2), $VVDD$ is connected to $DN$ through $M2$ and pulled down to “weak 0” ($V_{th}$). High skewed $INV1$ generates a full-swing and opposite signal $VVDD$-$Inv$, which drives $QM$ to ground through $M6$ and $M7$. Then $S$ is driven to “1” through $INV3$, which makes $DN$ “1”.
As VVDD is connected to DN, it goes back to original “0”, and error flag is vanished. Since “1->0” error is eliminated, output Q of EDSU is driven to 0 through the output inverters. As a result, the aiming value of D is successfully stored in EDSU and a “TB” time is borrowed from next successive stage. VVSS-Inv works in a similar way through M5 and M8 at “0->1” transition error.

As mentioned above, EDSU regards edge sampling as a “special timing error” which occurs exactly at the rising edge of clock. For example, if “1->0” assignment of D reaches before rising edge of clock (corresponding to “edge sample 0” in Fig. 2) and DN is set to “1” before rising edge. TG is off during low clock phase, so DN and S cannot affect each other and S remains at “0”. When clock rises, TG is turned on and TINV1 is turned off. TG sets DN to value of S, and then VVDD detects this sampling demand and corrects Q in same way of correct timing error. “0->1” assignment works in a similar approach by VVSS. That is how normal sampling is finished using the same logic of timing error correction.

M9, M10 and INV4 are designed to avoid the interference from glitch of input signal. When a glitch of D happens in detection window, VVDD or VVSS may stuck at a central state because the glitch may not leave enough time for them to be set back. On this occasion, D-Inv will drive VVDD back to high through M9 or VVSS back to low through M10.

Another advantage of EDSU is meta-stability free. Meta-stability in other EDAC works happens when D changes just around the transition of clock rising edge, driving DN falls at an unstable potential. If the feedback loop of master latch is also unstable during clock rising edge, the unstable state of DN may be propagated to Q. However, in EDSU, feedback loop of the only latch is already stable at clock rising edge, and any unstable state of DN cannot be propagated.
because S has a strong drive by INV3 and it will drive DN to a stable state through back conduction of TG.

3.2 EDSU circuit parameter

EDSU accomplishes non-stall EDAC with only two more transistors than conventional master-slave DFF, thus the clock load is also reduced. Detailed circuit parameter comparison is shown in Table I.

| Parameters        | Conventional DFF | EDSU normalized |
|-------------------|------------------|-----------------|
| clock to Q delay  | 51.2 ps          | 1.6 x           |
| clock load        | 8 transistors    | 4 transistors   |
| cell area         | 4.04 µm²         | 1.065 x         |
| switching power   | 43.4 µW          | 0.952 x         |
| correction power  | -                | 1.011 x         |

Because normal sampling in EDSU passes more transistors than DFF, the clock to Q delay of EDSU is 60% longer than DFF. For most designs with normal signoff frequency, clock to Q delay of flip-flop only takes a small part of path delay, the increasing of clock to Q will not be a problem and the enlarged clock to Q time can mostly be absorbed by next stage. Dynamic power of sampling in EDSU is 0.952 x of DFF because of reducing of clock driven transistors and correction power is 1.011 x of DFF which makes high error rate running possible with limited EDAC energy consumption.

4 EDAC system implementation

We apply EDSU in a commercial embedded processor CK802. CK802 is 32-bit and 3-stage, with 1143 total registers. EDSU is inserted to replace registers at the critical path end and global error handling logics are added to the system for time borrowing safety. CK802 is physically designed in a standard industrial EDA flow at SMIC 40 nm progress, and the replacement of EDSU is performed in iteration of ECO (Engineering Change Order) progresses.

4.1 EDSU insertion flow

The design flow of EDAC CK802 is fully compatible with standard digital IC design flow. Firstly, CK802 is designed under traditional flow until "place and route". After that, the detailed path distribution can be obtained through STA tools. Next step is to decide the detection window size and then the insertion register list.

Similar to former flip-flop based EDAC works, EDSU also requires system to expand hold time constraint of critical paths to the end of EDAC window to ensure short path does not trigger error detection. So the tradeoff between window length and hold buffer number should be compromised depending on detailed path distribution. After comparison in Fig. 3, we choose the window size as 20% of
the clock period. As the detection window is decided, registers that should be replaced with EDSU are also determined.

![Graph](image)

**Fig. 3.** Determine detection window size.

The insertion of EDSU is performed in a way of ECO (Engineering Change Order) progress. To avoid iterations of analyze and insertion, detection window constraint is slightly enlarged to make sure that the sub-critical paths do not become critical paths after EDSU insertion.

### 4.2 Timing error collection

To report timing error to upper system, timing errors from every EDSU node are collected together and then latched down for further operation. For speed and area consideration, dynamic logic is used for error collection. As shown in Fig. 4, VVSS-Inv is low valid and VVDD-Inv is high valid, so dynamic “and” logic and dynamic “or” logic are used separately. To filter out the VVDD-Inv and VVSS-Inv generated by the normal sampling, the reset signal used in dynamic latches is system clock delayed for a clock-to-Q time.

![Circuit Diagram](image)

**Fig. 4.** Timing error collection circuit.
In Fig. 2, the width of valid error signal (VVSS-Inv, VVSS-Inv) seems rather narrow, but they are wide enough to be captured by dynamic logics. For example, when VVDD-Inv arises, the valid time is consist of those consequences: VVDD-Inv drives QM down through $M_6$ and $M_7$; QM drives S up through $INV_3$; S drives DN up through $TG$; DN drives VVDD up through $M_2$; VVDD drives VVDD-Inv down. The whole time of those consequences is long enough and SPICE simulation shows the error signal is successfully generated.

### 4.3 Global error handling

Error correction in EDSU is based on time-borrowing of next pipeline stage, so it may be risky when path of next pipeline is not short enough to be borrowed. To maintain safety of time-borrowing, we utilize global clock shift in time error handling approach of EDSU, similar to [11]. On every detection of timing error, the next system clock will be shifted for length of a detection window and the timing borrowed from next stage is returned back. This approach is shown in Fig. 5.

Because the high duration of clock is chosen to be 20%, five phases of clock (clk4, clk3, clk2, clk1 and clk0) are generated for clock shift. They are delayed by a detection window one by one and they are selected to be CPU clock by a set of clock control flip-flops Q4-Q0. Q4-Q0 are set to their initial value of “5b10000”, and when a timing error occurs, their values are shifted as one hot code to make the CPU clock shifted to next phase of clock.

### 4.4 Physical implementation

The physical implementation and circuit parameters of CK802 are shown in Fig. 6. The system is physical designed at 0.9 V, typical temperature and process corner in SMIC 40 nm NLL technology. The 278 EDSU replaced registers are highlighted out in system layout. With sequential area increased slicely by 0.4% and combinational area increased by 5.1%, the total area overhead of EDAC CK802 is 5.5% due to short path fixing and global error handling.

### 5 Simulation results

To evaluate the variation tolerance ability of EDSU, the system is simulated in two ways: system performance test under fixed supply voltage and system power test under voltage scaling.
Fig. 7 shows the result of overclocking running with Dhrystone benchmark at 0.9 V. As system working frequency goes up, the number of timing errors arise and time borrowing based EDSU system shows higher performance. Replay based systems limit working frequency around PoFF (Point of First Failure), but time borrowing based system can gain more throughput at same working voltage, which means energy efficiency of the system is increased. At the optimal working point of EDSU system, the error rate reaches 33.94%, and the total throughput of EDSU system is 17.1% above the baseline, 16.2% above the optimal point of replay system (Razor Lite) and 12.5% above the optimal point of clock gating system (iRazor).

| Technology   | 40nm NLL |
|--------------|----------|
| Frequency    | 200 MHz  |
| Voltage      | 0.9 V    |
| P&R Area     | 16752μm² |
| Register     | 1143     |
| Number       | 278      |
| EMFF Number  |          |
| Seq Area     | 0.4%     |
| Overhead     | 5.5%     |
| Total Area   |          |

**Fig. 6.** Physical implementation and circuit parameters of EDAC CK802.

**Fig. 7.** Overclocking result at 0.9 V.
Voltage scaling is a convenient method to evaluate variation tolerance ability. Table II shows the voltage scaling simulation of the EDSU system, compared to baseline processor, Razor Lite [8] based processor, EDL (error detection latch) in [9] based processor and iRazor [10] based processor. While R-processor in [9] is a two-phase latch based design, we only uses its EDL to replace critical registers in flip-flop based CK802. Throughput of the five systems are fixed as throughput of baseline processor at 1.0 V with 3σ process and −40°C temperature variation (baseline running at signoff frequency without timing error). Voltage of EDSU based system can be scaled down to 850 mV, while iRazor based system can only be scaled to 880 mV, which means the voltage variation tolerance ability of EDSU (150 mV) is 25% higher than iRazor (120 mV) at fix throughput. EDL in [9] based system can also be scaled to 880 mV, but its power consumption is higher than iRazor based system because of higher area overhead of EDL. Razor Lite based system can only be scaled to 890 mV because its replay based error correction scheme harms throughput largely at lower voltage. At the optimal voltage point, EDSU bases system gains 29.7% power saving than the baseline system and 10.5% than the iRazor system.

Finally, we compared the characteristics of related EDAC works in Table III, including cell type, cell transistor count, correction CPI penalty, clock load overhead, registers insertion rate, integrated cache, system area overhead and design complexity, et al. The transistor count of EDSU is 2.1% higher than iRazor [10], but iRazor needs a “local clock generation circuit” for working, which means more design complexity. Note that all the other works have on-chip cache integrated and

### Table II. Voltage scaling down evaluation

| System            | VDD/mV | Average Power/mW | Decreased |
|-------------------|--------|------------------|-----------|
| Baseline          | 1000   | 1.95             | -         |
| Razor Lite [8]    | 890    | 1.63             | 16.4%     |
| EDL in [9]        | 880    | 1.61             | 17.4%     |
| iRazor [10]       | 880    | 1.53             | 21.5%     |
| EDSU              | 850    | 1.37             | 29.7%     |

### Table III. Total comparison among EDAC works

| Design            | [8]    | [9]   | [10]  | This paper |
|-------------------|--------|-------|-------|------------|
| Cell Type         | Flip-Flop | Latch | Flip-Flop | Flip-Flop |
| Transistor count  | 32     | 36    | 25.46 | 26         |
| CPI Penalty       | 11     | 0     | 1     | 0.2        |
| Clock Load        | No change | More | Less | Less      |
| Insertion Rate    | 19.8%  | 13%   | 8.7%  | 24.3%      |
| Integrated Cache  | Yes    | Yes   | Yes   | No         |
| Area Overhead     | 4.42%  | 8.3%  | 13.6% | 5.5%       |
| Design Complexity | Medium | Complex | Complex | Easy      |

1The number of 25.46 comes from equivalence of “local clock generation average”.
the percent of system area overhead will be diluted due to the huge size of cache. The area report of EDAC CK802 does not include cache, so the system area overhead is relatively low even under highest insertion rate.

6 Conclusion

In this paper, we proposed a novel EDAC cell EDSU, with ultra-low area and performance overhead. By utilizing a unified mechanism of edge sampling and error correction, EDSU uses only two more transistors than a conventional DFF. Because of time borrowing and clock shift based in-filed error fixing, CPI penalty introduced by EDSU is ignorable. We implement EDSU in a commercial microprocessor CK802 in SMIC 40nm NLL technology. In benefit of the ultra-low overhead property, EDSU inserted EDAC processor gains significant improvement in variation tolerance and energy saving, compared to the conventional design.

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