A Compact Model for Scalable MTJ Simulation

Fernando García-Redondo
Arm Ltd, Cambridge, UK
fernando.garcia@arm.com

Pranay Prabhat
Arm Ltd, Cambridge, UK
pranay.prabhat@arm.com

Mudit Bhargava
Arm Inc, Austin, USA
mudit.bhargava@arm.com

Cyrille Dray
Arm Ltd, La Paros, France
cyrille.dray@arm.com

Abstract—This paper presents a physics-based modeling framework for the analysis and transient simulation of circuits containing Spin-Transfer Torque (STT) Magnetic Tunnel Junction (MTJ) devices. The framework provides the tools to analyze the stochastic behavior of MTJs and to generate Verilog-A compact models for their simulation in large VLSI designs, addressing the need for an industry-ready model accounting for real-world reliability and scalability requirements. Device dynamics are described by the Landau-Lifshitz-Gilbert-Slonczewsky (s-LLGS) stochastic magnetization considering Voltage-Controlled Magnetic Anisotropy (VCMA) and the non-negligible statistical effects caused by thermal noise. Model behavior is validated against the OOMMF magnetic simulator and its performance is characterized on a 1-Mb 28 nm Magnetic RAM (MRAM) memory product.

Index Terms—STT-MRAM, MTJ, Compact modeling, s-LLGS

I. INTRODUCTION

Recent advances in MTJ devices [1]–[4] open the path to the next generation of system architectures, from embedded battery-less edge devices where off-chip Flash will be replaced by embedded MRAM, to future power-efficient caches in HPC systems. STT-MRAM is being actively developed by foundries and integrated into 28 nm generation CMOS Process Design Kits (PDKs) [4].

The complex multi-layered MTJ structures have heavily non-linear magnetic and electric behaviors that depend on the device structure, the thermal and external magnetic environment, and the applied electrical stress (Figure 1). On top of this complex system of equations, the evolution of MTJ magnetization $m$ shows a stochastic behavior caused by the random magnetic field induced by thermal fluctuations.

Many MTJ models have been presented, from micro-magnetic [5], [6] approaches to macro-magnetic SPICE and Verilog-A compact models for circuit simulations [1]–[3], [7]. Compact models present in the literature account for different behavioral aspects: a better temperature dependence [1], a more accurate anisotropy formulation for particular MTJ structures [1]–[3], and the integration of Spin-Orbit Torque (SOT) for three-terminal devices [2], [3]. These prior works focus on the ability to model a specific new behavior for the simulation of a single or a few MTJ devices in a small circuit. In these approaches, the simulation of device stochasticity imposes a high computational load on the simulation, complicating the simulation of larger VLSI circuits. To address the need to simulate thousands of MTJ devices in a single memory macro, circuit designers may have to oversimplify MTJ switching to a basic interpolated behaviour, and design for worst-case fixed voltage and current targets. This hinders the design of optimized circuits.

Therefore, there is a clear need for an accurate and modular compact model accounting for the magnetization dynamics of MTJ devices yet scalable enough for the simulation of large MRAM memory macros. In this paper we present three key contributions: Section II presents a study of reliability issues in MTJ model simulation. The proposed modeling framework is presented in Section III including a modular multi-threaded s-LLGS solver validated against OOMMF [5], an efficient Verilog-A compact model for MRAM macro simulation and a solution to model thermal noise effects. Finally, in Section IV we present a case study with a 1-Mb 28 nm MRAM macro.

II. MTJ COMPUTATIONAL AND CONVERGENCE ISSUES

From early behavioral prototypes to mature, product-ready PDKs, the simulation of emerging devices is a process that requires not only research contributions capturing novel device behavior [1]–[3], [7], but also optimization stages enabling circuit design [8]. For STT-MRAM, circuit design needs the complex device dynamics to be incorporated into the standard SPICE and Cadence® Spectre [9] solvers. In this section we address the challenges of reliable and efficient simulation of MTJ devices. All results are generated using Spectre 17.1.0.583 with default settings unless noted otherwise.

The s-LLGS system resolution can easily lead to artificial oscillations if solved in a Cartesian reference system [1] when using the Euler, Gear and Trapezoidal methods provided by circuit solvers. In [10] it is studied how MTJ devices benefit from resolution in spherical coordinates, specially when using implicit midpoint and explicit RK45 methods. Additionally, Cartesian methods require [1] a non-physical normalization stage for the magnetization vector [10]. Some further issues arising from solving in a spherical reference system are detailed below.
A. $m_\phi$ Wrapping

Prior work on MTJ Verilog-A models uses a naive Euler method to integrate the magnetization vector \[ m(t) = m(t - dt) + dm(t). \] However, Equation 1 causes $m_\phi$ to exceed the \([0, 2\pi]\) physically allowed range, and grow indefinitely over time, leading to unnatural voltages that eventually prevent simulator convergence. Our solution is to use the circular integration idtmod function provided by Spectre \([8, 9]\) which wraps $m_\phi$ at $2\pi$ and prevents it from increasing indefinitely.

B. $m_\theta$ Accuracy and Minimum Timestep

Vector $m_\theta$ represents the binary state of the MTJ data bit and is the most critical component to accurately model MTJ switching. The naive integration of $m_\theta$ directly encoding Equation 1 in the Verilog-A description incurs a substantial error during a switching event, as shown in Figure 2. Reducing the timestep improves the RMS error but at the cost of a large increase in computational load. Our solution is to use the idt function for the circuit solvers provided by Spectre [9], which adapt the integration based on multiple evaluations of the differential terms at different timesteps, leading to better accuracy. Figure 2 describes the accuracy RMSE when using a naive Euler method and the idt trapezoidal solver, when compared against OOMMF reference. The graph highlights how even with a smaller timestep involving 100× more computed events, the naive integration leads to larger errors.

C. $m_\phi$ acceleration

If a larger circuit is to be simulated and fixed timesteps banned, to avoid instabilities it is essential to manage the tolerance/timestep scheme \([10]\), especially during the computation of the $m_\phi$ component. The asymptote $\frac{dm_\phi}{dt} \to \infty$ at $m_\theta = 0$ accelerates the precession mechanism \([10]\). As described by Figure 3, this requires the solver to accordingly increase its resolution. A bounded or fixed time step would fail either to provide sufficient resolution or sufficient performance.

III. PROPOSED FRAMEWORK

In this section we describe the implementation and validation of the proposed MTJ compact model addressing the challenges described in Section II, emphasizing its dynamics module computing the MTJ magnetization and proposing solutions to incorporate thermal noise effects.

A. Compact Model Structure

Figure 4 describes the implemented compact model, composed of two modules: the Conduction and Dynamics modules. The conduction scheme describing the instantaneous MTJ resistance is dependent on the foundry engineered stack. Our modular approach allows foundry-specific conduction mechanisms to complement the basic Tunnel-Magneto-Resistance (TMR) scheme \([1, 3, 11]\). The Dynamics module describes the temporal evolution of the MTJ magnetization $m$ as a monodomain nanomagnet influenced by external and anisotropy fields, thermal noise and STT \([5, 10]\), described by the s-LLGS equations \([5]\) in I.S.U.

\[
\frac{dm}{dt} = -\gamma' m \times H_{eff} + \alpha' m \times \frac{dm}{dt} + \gamma' \beta \epsilon (m \times m_p) - \gamma' \beta \epsilon (m \times m_p)
\]

where $\gamma$ and $\gamma'$ are the Gilbert damping factor and gyromagnetic ratio respectively, related by $\gamma' = \frac{\gamma \mu_0 c}{1 + \alpha^2}$. $P$ is
the polarization factor, $M_s$ is the magnetization saturation, $I$ is the current flowing through the MTJ volume $V$, $m_p$ is the pinned-layer unitary polarization direction and $\Lambda$ and $\epsilon'$ set the primary and secondary spin transfer terms respectively. The effective magnetic field for a Perpendicular Magnetic Anisotropy (PMA) is defined by the anisotropy field, the external field and the thermal induced field $H_{eff} = H_{ani} + H_{ext} + H_{th}$. The anisotropy field is composed of the PMA uniaxial term, the shape anisotropy demagnetization field, and the VCMA field [1], [3], becoming the $H_{eff}$ field:

$$H_{eff} = H_{ext} + H_{ani} + H_{demag} - H_{VCMA} + H_{th}$$

$$= H_{ext} + \frac{2K_i}{t_{fl}t_{ox}M_s}m_z - M_iN \cdot m$$

$$- \frac{2K_iR_{mti}}{t_{fl}t_{ox}M_s}m_z + N(0, 1)\sqrt{\frac{2K_iT\alpha}{\gamma M_sV_{2s}}}, \quad (3)$$

where $K_i$ is the interfacial energy constant, $t_{fl}$ and $t_{ox}$ are the free layer and oxide thicknesses, $N$ is the shape anisotropy demagnetization factor, $\xi$ the VCMA coefficient, $K_B$ the Boltzmann constant and $N(0, 1)$ a Gaussian random vector with components in $x, y, z$ meeting [10], [12] conditions.

The compact model has been implemented in Python by adapting the Scipy `solve_ivp` [13] solvers to support the $H_{th}$ simulation as a pure Wiener process. The parallel Python engine enables MC and statistical studies. The Verilog-A implementation uses `idt`/`idtmod` integration schemes with parameterizable integration tolerances.

B. Validation Against OOMMF

The compact model is validated against the NIST OOMMF MicroMagnetic Framework [5], testing our results against its OOMMF interface [6]. Following the method from [10], we use SpinXferEvolve to simulate a single magnet under an induced spin current. Figure 5 shows that Python and Verilog-A implementations compare well with OOMMF with adaptive tolerance driven computations.

C. Thermal noise and MTJ stochasticity

The random magnetic field $H_{th}$ caused by thermal fluctuations induces stochastic MTJ behaviour resulting in a non-zero Write Error Rate (WER) upon switching events. $H_{th}$ follows a Wiener process [10], [12], in which each $x, y, z$ random component is independent of each other and previous states. This implies that the computation of $H_{th}$ requires large independent variations between steps, hindering the solver’s attempts to guarantee signal continuity under small tolerances. The scenario shown in Figure 6 leads to computational errors under default solver tolerances, and excessive computational load under 1 ps bounded time steps.

Three solutions have been proposed in the literature. First, to emulate the random field by using an external current or resistor-like noise source [7]. However, SPICE simulators impose a minimum capacitance on nodes filtering the randomness response, therefore preventing a true Wiener process from being simulated. Second, to bound a fixed small timestep to the solver [1], [2], but as described before this is not feasible for large circuits. Third, to only consider scenarios where the field generated by the writing current is much larger than $H_{th}$, forcing $H_{th} = 0$ [1]. [3]. This has strong implications when moving from single to multiple successive switching event simulations. Under no $H_{th}$ thermal field, the magnetization damping collapses $m_\theta$ to either 0 or $\pi$. s-LLGS dynamics imply that the smaller the $m_\theta$ the harder it is for the cell to switch, and if completely collapsed, it is impossible. This artificial effect, depicted in Figure 6 does not have an equivalent in reality, as $H_{th} \neq 0$ imposes a random angle. Design, validation and signoff for large memory blocks with integrated periphery and control circuits requires the simulation of sequences of read and write operations, with each operation showing identical predictable and switching characteristics. However, the damping artifact discussed above prevents or slows down subsequent switches after the first event, since the subsequent events see an initial $\theta$ value vanishingly close to zero. Two solutions are proposed below.

1) Windowing Function Approach: Our first objective is to provide a mechanism for $m_\theta$ to saturate naturally to the equilibrium value given by $H_{th}$ during switching events. By redefining the evolution of $m$ on its $\theta$ component we are able to saturate its angle at $\theta_0$, the second moment of the Maxwell-Boltzmann distribution of $m_\theta$ under no external field [1]–[3]. [7]. The new derivative function $\frac{dx}{dt}m_\theta = \frac{1}{8\pi}m_\theta \frac{1}{\alpha} m_\theta$ uses a Tukey window with the form $\frac{1}{8\pi}m_\theta = w_{tukey}(m_\theta, \theta_0) \frac{1}{8\pi} m_\theta$ where

$$w(m_\theta) = \begin{cases} 0 & m_\theta < \theta_0 \\ 0.5 - \frac{\alpha}{\pi} + \frac{\sin(\pi(m_\theta - \theta_0))}{\pi} & if \quad m_\theta - \theta_0 < \frac{\theta_0}{2} \\ 1 & otherwise \end{cases}$$

(4)
The process of calibrating a particular compact model instance is described in Figure [H] and ensures the validation of Python and Verilog-A instances against OOMMF, before the regression of $c_f^i$ or $c_i^c$ coefficients takes place with a one-off stochastic simulation step as shown in Figure [I].

IV. 1-Mb MRAM Macro Benchmark

To validate scalability on a commercial product, the model is instantiated into the the 64 × 4 memory top block of the extracted netlist from a 1-Mb 28 nm MRAM macro [I], and simulated with macro-specific tolerance settings. The emulated magnetic term from Section III-C2 enables the previously impossible capability of simulating successive writes with identical transition times due to non-desired over-damping. Figure [J]—resistance/voltage units omitted for confidentiality—describes a writing operation 10 µs after power-on sequence. We combine the s-LLGS OOMMF validated dynamics with foundry-given thermal/voltage conductance dependence, providing the accurate resistance response over time. Compared to using fixed resistors, there is an overhead of 3.1 x CPU time and 1.5 x RAM usage. In return, circuit designers can observe accurate transient switching behaviour and read disturbs.

V. Conclusions

This work presents an MTJ modeling approach for large VLSI circuits. We analyze MTJ modeling challenges and propose solutions to accurately capture stochastic thermal noise effects. Accuracy is validated against OOMMF, and scalability shown by incorporation into a 1-Mb 28 nm MRAM macro. The framework code is available upon request.

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