Don’t CWEAT It: Toward CWE Analysis Techniques in Early Stages of Hardware Design

Baleegh Ahmad
New York University

Wei-Kai Liu
Duke University

Luca Collini
New York University

Hammond Pearce
New York University

Jason M. Fung
Intel Corporation

Jonathan Valamehr
Intel Corporation

Mohammad Bidmeshki
Intel Corporation

Piotr Sapiecha
Intel Corporation

Steve Brown
Intel Corporation

Krishnendu Chakrabarty
Duke University

Ramesh Karri
New York University

Benjamin Tan
University of Calgary

ABSTRACT
To help prevent hardware security vulnerabilities from propagating to later design stages where fixes are costly, it is crucial to identify security concerns as early as possible, such as in RTL designs. In this work, we investigate the practical implications and feasibility of producing a set of security-specific scanners that operate on Verilog source files. The scanners indicate parts of code that might contain one of a set of MITRE’s common weakness enumerations (CWEs). We explore the CWE database to characterize the scope and attributes of the CWEs and identify those that are amenable to static analysis. We prototype scanners and evaluate them on 11 open source designs – 4 system-on-chips (SoC) and 7 processor cores – and explore the nature of identified weaknesses. Our analysis reported 53 potential weaknesses in the OpenPiton SoC used in Hack@DAC-21, 11 of which we confirmed as security concerns.

CCS CONCEPTS
• Security and privacy → Hardware security implementation; • Hardware → Electronic design automation.

KEYWORDS
Hardware Security, CWE, RTL, Linting

1 INTRODUCTION
The cost of correcting errors in hardware designs increases considerably in later stages of the product development cycle. Despite stringent requirements on functional correctness [34], hardware bugs, including security bugs, can persist [12]. A primary reason for this stems from the difficulty in evaluating security. Defining security properties and evaluating them is a complex process, requiring rare domain expertise. While several tools exist to support designers, such as linting tools [39], they often focus on checking functional correctness and only have limited features out-of-the-box for verifying security-related properties. Such tools can be used for some security-related checking [8, 12] but considerable security-relevant expertise is required. These tools are designed to function on near-complete RTL code, performing comprehensive and time-consuming testing to ensure all aspects of a given system are compliant. However, improving security requires checks throughout the design cycle, including in the early stages of RTL design where a complete security specification is not yet available.

Recently, industry-led efforts have added hardware-related issues to the Common Weakness Enumeration (CWE) list that is hosted by the MITRE Corporation [26]. The presence of a given weakness indicates that there are "flaws, faults, bugs, or other errors in software or hardware implementation, code, design, or architecture that if left unaddressed could result in systems, networks, or hardware being vulnerable to attack" [26]. CWEs serve as a "common language" for navigating weaknesses. Identifying different weaknesses requires different levels of context about the design, designers' intent, and security policies. To the best of our knowledge, early-stage analyses of hardware-based security weaknesses are largely a manual effort [12] that includes human inspection of hardware description language (HDL) code [8]. Ideally, this process of code inspection should be supported through automated scanning, with feedback to designers as they go. This analysis subsequently complements other later-stage efforts related to simulation/testing (e.g., [25]), and formal verification (e.g., [29, 30]) as part of an overall security development lifecycle (SDL) (e.g., [14]).

In this work, we explore the practical implications and feasibility of automating the detection of hardware CWEs, focusing on a selection of weaknesses with minimal context. We investigate a set of CWEs as a case study, and we present our experience in
implementing static analysis scanners to detect them, providing insights into the process of defining, implementing, and refining CWE scanners. Following a discussion of the motivation for our work (Section 2), our main contributions are:

- We investigate the hardware CWE database for weaknesses that are potentially amenable to identification from source code analysis (Section 3).
- We propose and prototype scanners to provide security-related feedback (Section 4).
- We evaluate our proposed scanning algorithms on a series of open-source SoC and processor designs (Section 5) and discuss their limitations and other practical issues (Section 6).

## 2 BACKGROUND

### 2.1 Related Work

There are several approaches to improving the security of hardware designs, including the use of a security development lifecycle (SDL) [14] that runs in parallel with traditional functionality driven development. The **Planning** stage is the first stage for SDL where security requirements are specified. This is followed by the **Architecture** and **Design** stages, where relevant threat models are considered. Checking the design against these security threat models is carried out in the **Implementation** and **Verification** stages. While **Implementation** consists of manual checks and static analysis of code, the bulk of validation is carried out in **Verification** where security properties expressed through assertions in HDLs are verified. Physical testing is also done after fabrication. The last stage is **Release and Response**.

Several security analysis techniques can be used throughout this process. Recent work has proposed formal verification [9, 19, 29, 30, 32], Information Flow Tracking [6, 10, 21, 41], fuzz testing [22, 27, 36, 37], as well as run-time detection [20, 28, 31]. These techniques rely on simulation or they operate in the field, using complete or near-complete designs. To complement these, we focus on an earlier stage in the design process, specifically in the **implementation** phase. Our premise is that static analysis of register-transfer level (RTL) code can identify some security weaknesses, preventing them from propagating to the next stage.

Static analysis is an established approach used in software to identify errors and bugs; e.g., Lint was proposed in 1978 to analyze C code [23], and has since been adopted in many programming languages coining the term ‘Linter’. Lint algorithms try to strike a balance between accuracy and practicality, as generated warnings are acceptable only in proportion to the real bugs uncovered. If too many false positives are raised, they obscure true problems.

Several commercial and community tools offer linting capability for HDL (e.g. [1, 39]), but they focus predominantly on functional and structure checks. They are comprehensive tools with several tags and parameters that can be configured to check for custom and predefined rules. Linting has been used to handle critical hardware issues like latches and clock gate timing validation [33]. Formal linting tools have been analyzed to find bugs in RTL before synthesis [40]. The idea of continuous linting is proposed in [18] to bring design errors to the attention of designers at a faster rate. While these works highlight the capability of linting for reducing the load on the verification stage, they do not look at hardware that could be functionally correct yet insecure. It is up to the security expertise of the designer to identify a lint message relevant to security.

### 2.2 Motivation

Consider the following scenario: an RTL designer works on several hardware modules, iterating the design and periodically checking it via simulation, synthesis, or manual review. As they work, they require frequent, fast feedback – for example, a simulation tool will report syntax errors and potentially help the designer avoid design bugs. For a more thorough check, the designer could use some kind of static analysis tool, such as a **linter** to check the source code against set guidelines [7] and raise warnings or error messages.

To explore the potential limitations of linting tools, we investigated an industry tool (Tool#1), and Verilator [1]. We set Verilator in lint-only mode with the –wall flag (enables all checks and warnings) set. We set Tool#1 on the lint_rtl goal under the block-/initial_rtl methodology, appropriate for early-stage RTL design. After analyzing the hardware CWEs for those that are amenable to static analysis (discussed in Section 3), we implemented a small set of Verilog modules with weaknesses based on the examples on the MITRE website. The results are in Table 1. The default set of rules for Tool#1 could not find security-specific issues. However, as Tool#1 offers optional rules, it might be possible to find security-relevant ones. A designer must identify security-relevant tags in the 936 available rules, a challenge! We identified seven rules covering finite state machine (FSM)-related problems, race conditions, and uninitialized registers that could lead to security bugs.

We ran Tool#1, adding the identified tags to the default RTL lint rules, on the HACK@DAC’21 SoC [12, 17] and it raised 597 warnings in 84 seconds. Only 19 of the warnings were related to the optional tags with the rest raised by the default rules, representing considerable “noise,” i.e., issues not specific to security, although a designer can reduce noise by creating a custom goal with only the security-specific linting rules. With this setting, the linter was only able to detect potential issues related to state encoding in FSMs. We expected to detect FSM related issues with Tool#1 but they were not identified in our benchmarks. This probably happens because our implementation of FSMs does not follow standard FSM related patterns. Another plausible explanation is that basic lint checks with industry tools require the elaboration of the design and do not obtain all relevant information needed at the earlier analysis stage. The details of these stages are discussed in the next section. All in all, **linters are not designed specifically with security in mind** and require time and expertise to set them up for security-related tasks and to filter the results. We are thus motivated to investigate the feasibility of identifying security bugs with pre-elaboration static analysis to provide early-stage security feedback to designers.

| CWE Module Weakness Tool#1 Verilator CWEAT |
|------------------------------------------|-----------------|-----------------|-----------------|
| Locked register debug overrides lock     | ☒               | ☒               | ☒               |
| JTAG lock jtag lock signal not reset     | ☒               | ☒               | ☒               |
| JTAG lock jtag lock signal not reset     | ☒               | ☒               | ☒               |
| state machine incomplete case statement  | ☒               | ☒               | ☒               |
| state machine unreachable state          | ☒               | ☒               | ☒               |
| state machine FSM deadlock               | ☒               | ☒               | ☒               |
| Access control access set after transfer | ☒               | ☒               | ☒               |
| Peripheral sensor write signal not checked | ☒               | ☒               | ☒               |
3 STATIC ANALYSIS OF HARDWARE CWES

This work aims to improve security-specific analysis and feedback in early-stage RTL design by finding hardware CWES. However, the CWE list comprises myriad weaknesses at different levels of specificity and abstraction. We first classify the CWES based on our assessment of how amenable they are to static analysis, and then propose the framework for our CWE Analysis Techniques, CWEAT.

3.1 Classifying CWEs for Scanning

There are 96 HW CWEs on MITRE’s website [26] at the time of writing. In this section, we classify them by their amenability to detection, with our classification of the CWEs presented in Table 2.

The first delineation is whether the CWE is code-based or not. We exclude CWEs that do not originate in RTL designs (6). We consider whether the CWEs can be detected statically or dynamically (i.e., in a simulation or at run-time). Our approach focuses on CWEs that can be statically detected. CWEs such as CWE-1264, where de-synchronization between data and permission checking logic is evident only at run-time, require a different approach for detection (30 require functional simulation). We examine the CWEs that can be detected statically, classifying them based on the data required.

Some bugs may be detectable using only static analysis of the RTL code, where the source is transformed into parse-trees, performing type-inference and detecting syntax errors. Here, the created parse-trees can be further analyzed using different algorithms to extract useful information for CWE identification. These can be classified into those that are directly detectable from the code (11), or those that may require additional context (21).

Other CWEs can be further partitioned by the amount of “extra information” or context required to scan for a weakness (9 CWEs total). Static elaboration of the design entails binding instances to modules, resolving library references, processing `ifdef statements, unrolling for loops, flattening instance arrays, and replacing parameters with constants. The result after static elaboration is an elaborated parse tree. RTL elaboration then synthesizes the design using pre-defined primitives (e.g., AND, OR) and operators (e.g., add, multiply). The result of RTL elaboration is a synthesized RTL netlist. The remaining 16 CWEs do not have general symptoms among designs, so they cannot be formalized and identified, requiring manual analysis by IP security experts to detect.

As an example of the different types, consider the following. An incomplete FSM can be discovered by static analysis without any information from users (CWE-1245). In contrast, to identify the improper translation of security attributes by the fabric bridge (CWE-1311), additional information (context) regarding the fabric protocol is required. Even though several CWEs can be detected by static analysis, some issues do not manifest until the parse-tree is elaborated. For instance, incorrect default module parameters (CWE-1221) are difficult to find by static analysis. However, we can identify this issue through static elaboration, where all the parameters are calculated and propagated to each module. Moreover, cross-modular issues might demand RTL elaboration, e.g., CWE-1291. Still, some CWEs cannot be discovered at the RTL design stage, e.g., CWE-1278, which requires reverse-engineering protection.

In this work, we focus on static analysis of RTL source per-module with little to no context. Thus, CWEs that are specific to limited module-types, cross-modular CWEs, or those requiring simulation are out of scope and are the focus of our future work. We target the following five CWES as representatives for illustration.

CWE-1234: Hardware Internal or Debug Modes Allow Override of Locks. A debug or debug-related signal overrides the value of an internal security-relevant signal, e.g., a lock or access control signal. This allows adversaries to reconfigure sensitive policy values or disable security protections if they can get into debug mode.

CWE-1271: Uninitialized Value on Reset for Registers with Security Settings. Registers with sensitive information like keys, lock bits or access control bits do not default to secure postures on reset.

CWE-1245: Improper Finite State Machines (FSMs) in Hardware Logic – where FSM logic contains “gaps” which could allow adversaries to put the system in an unknown or vulnerable state.

CWE-1280: Access Control Check Implemented After Asset is Accessed – where an asset is accessible before the check on its access control signal. The asset should be accessible only after the check is successful, otherwise the security might be compromised.

CWE-1262: Improper Access Control for Register Interface – where a register value is not write-protected or is not correctly protected, i.e., untrusted users can override the signal through the register interface. The protection mechanisms for security-relevant signals must be correctly implemented to avoid data leakage.

3.2 CWEAT Framework

To assist in the detection of our targeted CWEs, we propose to create abstract syntax trees (ASTs) from Verilog source and traverse them with hand-crafted, heuristic detection algorithms (Section 4). Figure 1 illustrates the CWEAT framework, where the input is the design repository containing the source code. The design can comprise a single hardware intellectual property block (IP) through to an entire system-on-chip (SoC). Relevant source code files (in Verilog and/or SystemVerilog) are extracted from this repository and sorted in the order they should be analyzed. If a file has errors or does not have necessary dependencies, the tool ignores it. The final sorted source code list is sent to the Analyzer. The Analyzer runs on the entire set of source code files and produces N ASTs – one per module. We use Verific [5] as the front-end parser to build the ASTs. Each scanner traverses every AST according to the detection algorithm for a CWE using the associated rules and keywords. Future work can add new scanners to the framework.

We use keywords while searching for weaknesses for two reasons: (i) to locate ‘security relevant’ features in RTL (discussed in detail in Section 4), and (ii) to prune the search space for these weaknesses. The keyword-matching rules comprise matching and exclusion rules, e.g., ignoring clLock when looking for Lock. These rules could come from established design styles or might be provided by

| Detection method | CWEs | # CWEs |
|------------------|------|--------|
| Non-RTL          | 1234, 1296, 1280, 1307, 1393, 1279, 1281, 1252, 440, 1264, 1297 | 3 |
| Functional simulation | 1191, 1298, 1272, 1313, 1234, 1225, 1224, 1225, 1263, 1251, 1315 | 29 |
| Static analysis (no context) | 1304, 1352, 441, 1268, 1294, 1190, 293 | 11 |
| Static analysis (with context) | 1318, 1297, 1312, 1302, 1326, 1316, 1295, 1289, 1314 | 22 |
| Static/RTL elaboration | 1284, 1298, 1239, 1351, 1231, 1236, 1298, 1299 | 9 |
| Manual analysis | 1324, 1263, 1372, 1277, 1287, 445, 1241, 1356, 1300, 1301, 1278 | 16 |

Table 2: Classification of Hardware CWES
the designers. For our experiments, we devised keyword-matching rules by observing design styles.

4 CWE DETECTION ALGORITHMS

4.1 Preliminaries

Our heuristic detection algorithms work on the ASTs of an HDL design. The AST can be extracted by a parser of choice for the preferred HDL. Each node of the AST represents a construct defined by the formal grammar of the HDL, e.g., a declaration, an expression or a module instance. The nodes are connected together to preserve the syntax expressed in the parsed design. Figure 2 shows an example of the AST of a Verilog module.

A common design pattern to traverse ASTs is the Visitor Pattern. This pattern involves defining a procedure that will be executed for each construct of interest. When a node is traversed, if a procedure for the construct exists, it is executed; otherwise, the children nodes are traversed. This allows for a built-in recursion if a procedure for the construct exists, it is executed; otherwise, the children nodes are not traversed. A visitor accepts a node N when it starts the traversal of the sub-tree with N as root.

4.2 CWE Scanner Algorithms

Examples use a Verilog-like syntax but the concepts are applicable to all HDLs.

Algorithm 1 : CWE-1234 Detector

procedure traverse(ConditionalStatement node)
if node.if_expr.matches(lock_kw, dbg_kw, ops) then
results.append(Result(if_expr, loc))
end if
TRaverse(node.ElseStmt), TRaverse(node.ThenStmt)
end procedure

Figure 3: Traversal for CWE-1271

4.2.1 Scanner-1234: Algorithm 1 illustrates the scanner for CWE-1234. As the tree is traversed, the expression for the if statement in ConditionalStatement node(s) is fetched as if_expr. if_expr is analyzed by checking whether it matches three conditions: (i) presence of a lock keyword from a list lock_kw, (ii) presence of a debug keyword from a list dbg_kw, and (iii) presence of binary logic operators (e.g., or) that indicate ‘overriding’. If these conditions are met, the if_expr is categorized as potentially vulnerable. Relevant information is collected and appended to results. Next, the else and then statements of the ConditionalStatement are traversed sequentially. This recursion takes care of nested if-else statements.

4.2.2 Scanner-1271: Figure 3 illustrates the scanner for CWE-1271. While traversing a data declaration node, candidates for security relevant registers are gathered and marked as unsafe. These candidates are then marked as safe based on the rest of the traversal. In RTL, this happens if the security-relevant register is assigned a value inside a reset block. In the AST, this is identified through traversing various nodes based on flags set in the scanner. The flag is_reset_block is set when traversing a node which represents a reset block. The flag is_reset lhs is set when traversing a node that is the left hand side of an assignment inside a reset block.

4.2.3 Scanner-1245: has a 3-step detection strategy: (I) Find FSM variables: The scope of the module, containing the locally declared identifiers in a symbol table, is obtained. The identifiers are checked to be part of explicit FSMs and of the type Variable. Explicit FSMs are easily recognize as one-hot encodeable and are modeled with a single clocking event. Implicit FSMs are found similar after being converted to explicit FSMs. All variables linked to this FSM variable are tracked and added to a list of
variables belonging to a specific FSM.

(II) **Extract FSM transitions:** This traversal progresses according to the variables found in the previous step and gathers information from assignments of these variables. This information includes the previous state, next state, condition for transition and the location of assignment. The goal here is to collect the transitions of an FSM and add them to the FSM object.

(III) **Analyze FSM:** After relevant information is gathered, the FSM is checked for several weaknesses. These include unreachable states, FSM deadlocks, and incomplete case statements. An unreachable state is shown as S4 in Figure 4(a); it is the initial state of a transition, but there is no way to get there, i.e., S4 is not present in the final state of any transition or on reset. An FSM deadlock is shown as S4 in Figure 4(b); it is the final state of a transition, but there is no way to get out i.e., it is not the initial state of any transition. A case statement representing an FSM is analyzed for completeness in addition to these FSM vulnerabilities. Completeness is verified if there is either a default statement present or if the number of case items equals the possibilities from the size of case condition.

4.2.4 **Scanner-1280:** Figure 5 illustrates the scanner for CWE-1280. A traversal of the AST builds two lists containing information on read and write operations (reads and writes) lists respectively. The entries of the two lists are triples containing the Id, a reference to its parent SeqBlock, and its line number. After visiting the AST of the module and building the reads and writes lists, the algorithm iterates through these lists and compares each read entry with the write entries. If a read and a write have the same ids, are in the same SeqBlock, and if the read comes before the write, the updated value is not read, posing a potential weakness.

![Figure 4: FSM weaknesses](image)

(a) Unreachable state (S4)  
(b) FSM deadlock

4.2.5 **Scanner-1262:** has a 2-step detection strategy:

(I) **Find the control signals for the registers associated with write transactions:** We only focus on registers that are not properly ‘write protected’, so only signals with names containing wdata are considered. As the AST is traversed, we use a stack to record the signals in the sensitivity lists in if/else statements and assign this set of signals to the registers within the same sequential block as the control signals. Irrelevant signals in sensitivity lists that are not ‘controlling’ (e.g., clock and reset are not control signals) are pruned.

(II) **Identify registers under improper control:** After pruning, if the control signal set is empty, the corresponding register is regarded as unprotected because untrusted users could modify the register by issuing write transactions directly. We also compare the control signal sets for register arrays. Since an array of signals should have the same ‘level’ of protection, each entry should have the same number of control signals. Additionally, a warning will be raised if different entries do not have an identical set of control signals.

5 EXPERIMENTAL WORK AND RESULTS

5.1 Overview

To evaluate the practicality and limitations of the CWEAT framework, we implement the scanners detailed in Section 4 and apply them on several open-source designs. Our experiments characterize several elements of the framework, including the number of instances caught by CWEAT, the wall-clock performance of the scanners, and a detailed study of the warnings produced for an SoC. As part of our implementation, we curated a set of security-relevant keywords for signal names, the effect of which we also explore.

Table 3 lists the designs on which we evaluated CWEAT. The first four entries in the table are SoCs consisting of cores and peripherals and the remaining designs are processors only. The SoCs include several peripherals to show applicability of scanners on modules outside of the core. The designs have diversity in terms of complexity of the cores and HDL languages (Verilog and SystemVerilog) and cover two popular open-source ISAs (RISC-V and OpenRISC). As there is no ground truth about the presence of CWEs, we manually inspect the warnings in our detailed analysis (Section 5.3). We ran our experiments on an AMD Ryzen 9 3950X 16-Core Processor, 64 GB DDR4 RAM, using Ubuntu 20.04. The framework uses Verific libraries (academic license), gcc 9.4.0, and Python 3.8.10.

5.2 Initial Analysis

Table 3 summarizes the scanning results. The scanners analyzed as few as 1 to as many as 409 files per project, with up to ∼76k lines of code (LoC). The scanner for CWE-1245 found the most potential instances of that CWE across the projects, while the scanner for CWE-1234 found the least. The mean running time for scanning was ∼63 ms; producing the ASTs took around 3× the time of running the collection of scanners on average, suggesting that these static analyzers could provide fast feedback to designers. For the Hack@DAC’21 SoC, we produce 53 security warnings; this is more targeted than the 597 warnings from a commercial tool (Section 2).

To measure the portion of designs relevant to CWEs, we consider the number of ‘relevant’ AST nodes visited when running the different scanners. A node is considered ‘relevant’ if it needs to be traversed to detect the CWE. We also compare the number of relevant nodes visited by our scanners when keywords are used versus not used. This is shown in Table 4. The number of nodes traversed with keyword matches are, on average, 80.4X fewer than the number of nodes in ASTs and 16.3X fewer than nodes relevant to CWEs. Clearly, the keyword list used as part of scanning is an important aspect of making CWEAT practical.
We devised our set of keyword-matching rules based on our experience with various design styles. This includes our initial experiments with open source designs, review of bug examples in literature [8, 12, 25, 37] and participation in hardware bug hunting competitions. For additional insight, we analyzed how often signals match our keywords across the different open-source projects. The results are reported in Figure 6. The frequency values are reported in log scale due to the high range of total identifiers across designs. The keywords cover a good portion of the considered benchmarks, indicating broad applicability for a framework like CWEAT to be used out-of-the-box in different projects. While our keywords are meaningful across the designs that we considered, our goal is not to provide the best set of keywords, but to show that keywords are an effective way to build security scanners. In real-world applications, performance can be improved by designers modifying keywords.

### 5.3 Detailed Analysis

We evaluate each warning picked up by CWEAT and classify it as True Positive (T), Indeterminate (I), or False Positive (F). T means we confirmed the CWE’s presence. Ascertainment if a CWE leads to an exploitable vulnerability is out of scope of this analysis. Conversely, F means we determined that the CWE was incorrectly flagged. In cases where we could not discern an instance into T or F, we classified it as I. Figure 7 shows our classification.

![Figure 7: Classification of instances caught by CWEAT in SoCs.](image)

To explain our analysis and classifications of CWEAT’s warnings, we discuss examples found in the Hack@DAC-2021 SoC, demonstrating the use of CWEAT and providing insights into the practicalities of using this approach. There are deliberate vulnerabilities implanted in this SoC, but we do not have access to a comprehensive list of those vulnerabilities. It is also not our goal to detect those deliberately inserted vulnerabilities.

![Figure 6: Keyword frequency in select open-source HW.](image)

Table 3: CWEAT Results Summary

| Design          | Files/LoC(k) analyzed | Files/LoC(k) not analyzed | Time (ms) | Analysis/Scan | Time (s) | LoC | Files (k) |
|-----------------|-----------------------|---------------------------|-----------|---------------|-----------|-----|-----------|
| HipDAC21        | 328 / 67.3            | 112 / 18.2                | 354 / 76  | 2 / 13 17 12 9 |
| (Optimistic)    |                       |                           |           |               |           |     |           |
| HipDAC18        | 409 / 76.3            | 116 / 16.2                | 322 / 142 | 0 / 9 26 20 10 |
| (Polipusismo)   |                       |                           |           |               |           |     |           |
| HummingbirdV2   | 128 / 48.3            | 8 / 1.8                   | 254 / 27  | 0 / 1 2 0 2   |
| (E203) [35]     |                       |                           |           |               |           |     |           |
| Orpsoe          | 181 / 61.2            | 23 / 6.7                  | 229 / 175 | 0 / 0 21 0 0  |
| EHI Swerv       | 1 / 15.9              | 0 / 0                     | 744 / 142 | 0 / 0 0 0 0   |
| Ibx             | 34 / 7.6              | 3 / 1.4                   | 34 / 44   | 2 / 1 0 0 0   |
| CV32E6F         | 109 / 25.4            | 15 / 4.1                  | 111 / 21  | 5 / 4 5 0 0   |
| SCR1            | 41 / 1.4              | 4 / 0.3                   | 120 / 14  | 0 / 12 3 0 0  |
| SERV            | 15 / 2.1              | 0 / 0                     | 8 / 0.1   | 0 / 0 0 0 0   |
| Ultraembedded   | 17 / 5.7              | 1 / 0.5                   | 28 / 7    | 0 / 0 0 0 0   |
| Morilix         | 46 / 20.7             | 3 / 0.7                   | 95 / 53   | 0 / 3 0 1 0   |

Table 4: Fraction of relevant nodes for scanners. (r) is the % of nodes traversed for the scanner. (r+kw) is the % of nodes traversed because of keyword matches.

| Design          | 1234 r (%) | 1262 r (%) | 1271 r (%) | 1245 r (%) | 1280 r (%) | Total nodes (k) |
|-----------------|------------|------------|------------|------------|------------|----------------|
| Hip21           | 0.815      | 0.001      | 0.253      | 0.62       | 0.299      | 0.893          |
| Hip18           | 0.113      | 0.0005     | 0.256      | 0.642      | 0.236      | 0.641          |
| e203            | 0.361      | 0.040      | 0.221      | 0.14       | 0.258      | 0.55           |
| orpsoe          | 0.187      | 0.025      | 0.292      | 0.879      | 0.297      | 2.27           |
| scr1            | 0.235      | 0.031      | 0.3569     | 0.63       | 0.3571     | 0.532          |
| ibex            | 0.744      | 0.012      | 0.264      | 0.479      | 0.258      | 0.72           |
| cv32            | 0.118      | 0.018      | 0.279      | 0.84       | 0.213      | 0.77           |
| serv            | 0.677      | 0.016      | 0.218      | 0.422      | 0.215      | 0.88           |
| serv            | 0.646      | 0.016      | 0.261      | 0.397      | 0.219      | 0.62           |
| ultraemb        | 0.912      | 0.018      | 0.267      | 0.656      | 0.218      | 0.66           |
| morilix         | 1.782      | 0.016      | 0.275      | 0.674      | 0.254      | 1.63           |
if (ex_valid_i || eret_i || set_debug_pc_i) begin
  // or alternatively if there is no exception pending and
  if (pmp_access_type_en)
    dii_data_vld <= 1'b0;
end

always_comb begin : wfi_ctrl // wait for interrupt register
  wfi_d = wfi_q; // if there is any interrupt pending un-stall
  p = p + N;
  if (|mip_q || deq_req_i || irq_i [1]) begin
    always_comb begin : wfi_ctrl // wait for interrupt register
      wfi_d = 1'b0;
      p = p − N;
      A[WIDTH−1:0] = A[WIDTH−2:0];
    end
  end
end // code skipped for brevity

if (exponent_reg!='d0) begin //code skipped for brevity
  pmp_access_type_reg <= pmp_access_type_new;
end

if (p[WIDTH−1] == 1) begin
  if (ct_valid == 1) state <= s15;
end

for CWE-1262, CREATE picks up 9 instances: 1 T, 2 I and 6 F. One T instance is shown in Figure 12(a). As specified in Section 4.2.5, we first collect a set of control signals for reglk_mem[0], which contains jtag_unlock, en, we, reglk_ctrl[3]. Note that the sig- nals associated with clk and reset are pruned out. Since there are still four control signals for reglk_mem[0], it is write-protected. However, when we compare the control signals for the reglk_mem array, only reglk_mem[0] is controlled by reglk_ctrl[3], while other entries are controlled by reglk_ctrl[1], as highlighted in Figure 12(a). This difference might not be an issue if designers made it intentionally. Designers might use different signals to control a signal array, as shown in Figure 12(b) where each entry of acct_mem is controlled by different reglk_ctrl values. Since each entry of acct_mem represents different IPs’ access control values, and each IP has different security levels, this array may not have the same control signals. However, in Figure 12(a), only one entry of reglk_mem has different control signals, without evidence to justify its legality and is classified as CWE-1262. We present an attack scenario to exploit this bug.

5.4 User Exploit for CWE-1262

When we scanned the Hack@DAC-2021 SoC, they pointed to some files to potentially contain CWEs, including the one shown in Figure 12(a) where CWE-1262 is present. To verify the validity, we generate an attack scenario to confirm the vulnerability. As the code snippet shows, reglk_mem[0] is controlled by reglk_ctrl[3], while other bits of reglk_mem are controlled by reglk_ctrl[1]. This difference could be used by attackers if designers are not aware of it and set the reglk_ctrl[3] and reglk_ctrl[1] to 0 and 1,
respectively. The `reglk_mem` stores the control values for the registers in peripheral IPs, which appears to be `reglk_ctrl` in the modules. Once the protection for `reglk_mem` is bypassed, these control values can be reconfigured and several IPs’ registers can be modified by attackers, resulting in the security issue.

We set the REGLK_REGLK value in `reglk.h` to 0xf6, which makes `reglk_ctrl[3]` 1 and allows untrusted users to override `reglk_mem[0]` at run-time. We ran the simulation on Hack@DAC-2021 platform and issued a write transaction to bypass `reglk_ctrl` protection to modify `reglk_mem[0]`, leaving security-relevant signals in AES0, AES1, and SHA256 prone to leaks and modifications.

6 DISCUSSION AND LIMITATIONS

While developing our scanners, we faced a challenge: balancing accuracy (ratio of true positives over total instances caught by scanner) and comprehensiveness (number of true positives identified). This trade-off exists because, to increase comprehensiveness, we need to cast a wider net (increase keyword breadth) and traverse more source code. This will identify more weaknesses but can also flag more false positives. A decrease in accuracy of the tool makes it less practical to use. Conversely, if the goal is to more accurately identify weaknesses, some true positives will not be picked up, increasing the probability of weaknesses persisting in designs. While this trade-off is an important consideration for static analysis tools, the goal of this work is not to provide the best scanners, but to show that such static scanners can be implemented in a way that can be useful for designers to write more secure modules.

An approach to improve the scanners could involve “learning” the coding style of a given project, i.e., using user feedback to update the scanning. Interaction between designers and warnings generated can be used to iteratively increase accuracy. However, caution must be taken to avoid the pitfall of designers providing poor feedback (e.g., marking everything safe to avoid alarm fatigue). An example user-driven refinement is shown in Table 5, which shows the results after revising keywords in the scan of the Hack@DAC-2021 SoC. By default, we scan the design using a default list (first row). This includes matches with sensitive signal names in the `true` list and prunes out matched with the `false` list. The user can add signals they consider ‘security-relevant’ (second row). This results in more hits. The user can then mark certain signals as irrelevant by appending to the `false` list (third and fourth row). In this case, one true weakness is missed, but drastically improves the number of true positives as a fraction of the total number of instances/hits caught by the scanner.

Our approach cannot guarantee the absence of a weakness when no warnings are produced. These ‘false negatives’ exist because we use heuristic detection of patterns. In our experiments, there are no benchmarks for comparison as we are in the initial stages of classifying, gathering, and understanding weaknesses in RTL. Our experimental evaluation focused on selected open-source designs with subsequent manual inspection to gauge effectiveness of scanners. In our manual inspection, we are somewhat limited when evaluating others’ designs without complete context to understand intended implementation. Since documentation is limited and source code comments reveal partial information, evaluating instances picked up by scanners is limited by the expertise of the security evaluator. That said, if the examiner is also the designer, classification should be easier and faster. In an industry setting, there will be fewer uncertainties as documentation that conveys security-relevant information is more readily available. Design and security teams can work together to navigate potential concerns.

7 CONCLUSIONS AND FUTURE WORK

We have shown that certain CWEs can be detected during the early RTL Implementation stage. In the 11 open-source designs, 180 instances were caught by CWEAT. We evaluated the 144 found in SoCs and confirmed weakness in 35 (24.31%) of the instances. 19 (13.1%) were indeterminate and 90 (62.5%) were not weaknesses. We have also shown that CWEAT restricts the search for particular weaknesses to a smaller subset. Instead of having to go over thousands of lines of source code, the search for specific issues is limited to a few signals and modules. By adding new scanners, other CWEs could be analyzed, increasing the level of security of the design.

The CWEs are varied in nature and can be detected at various stages. This provides two concrete directions for research. Firstly, scanners can be developed for the 21 CWEs that can be detected statically with specification files as shown in Table 2. Secondly, more accurate and comprehensive scanners can be developed for the CWEs we have targeted. Both approaches aim to standardize detection of hardware weaknesses, which we believe is significant.

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