Spatz: A Compact Vector Processing Unit for High-Performance and Energy-Efficient Shared-L1 Clusters

Matheus Cavalcante*  
Domenic Wüthrich*
matheus@iis.ee.ethz.ch
domenicw@student.ee.ethz.ch
Integrated Systems Laboratory  
ETH Zürich  
Zürich, Switzerland

Matteo Perotti  
Samuel Riedel
mperotti@iis.ee.ethz.ch
sriedel@iis.ee.ethz.ch
Integrated Systems Laboratory  
ETH Zürich  
Zürich, Switzerland

Luca Benini
lbenini@iis.ee.ethz.ch
Integrated Systems Laboratory  
ETH Zürich  
Zürich, Switzerland

UNIVERSITÀ DI BOLOGNA  
BOLOGNA, ITALY

ABSTRACT

While parallel architectures based on clusters of Processing Elements (PEs) sharing L1 memory are widespread, there is no consensus on how lean their PE should be. Architecting PEs as vector processors holds the promise to greatly reduce their instruction fetch bandwidth, mitigating the Von Neumann Bottleneck (VNB). However, due to their historical association with supercomputers, classical vector machines include microarchitectural tricks to improve the Instruction Level Parallelism (ILP), which increases their instruction fetch and decode energy overhead. In this paper, we explore for the first time vector processing as an option to build small and efficient PEs for large-scale shared-L1 clusters. We propose Spatz, a compact, modular 32-bit vector processing unit based on the integer embedded subset of the RISC-V Vector Extension version 1.0. A Spatz-based cluster with four Multiply-Accumulate Units (MACUs) needs only 7.9 pJ per 32-bit integer multiply-accumulate operation, 40% less energy than an equivalent cluster built with four Snitch scalar cores. We analyzed Spatz’ performance by integrating it within MemPool, a large-scale many-core shared-L1 cluster. The Spatz-based MemPool system achieves up to 285 GOPS when running a 256 × 256 32-bit integer matrix multiplication, 70% more than the equivalent Snitch-based MemPool system. In terms of energy efficiency, the Spatz-based MemPool system achieves up to 266 GOPS/W when running the same kernel, more than twice the energy efficiency of the Snitch-based MemPool system, which reaches 128 GOPS/W. Those results show the viability of lean vector processors as high-performance and energy-efficient PEs for large-scale clusters with tightly-coupled L1 memory.

KEYWORDS

Vector Processing, SIMD, Many-Core, RISC-V Vector Extension

ACM Reference Format:
Matheus Cavalcante, Domenic Wüthrich, Matteo Perotti, Samuel Riedel, and Luca Benini. 2022. Spatz: A Compact Vector Processing Unit for High-Performance and Energy-Efficient Shared-L1 Clusters. In IEEE/ACM International Conference on Computer-Aided Design (ICCAD ’22), October 30-November 3, 2022, San Diego, CA, USA. ACM, New York, NY, USA, 9 pages. https://doi.org/10.1145/3508352.3549367

1 INTRODUCTION

The ever-growing need for computing performance under an increasingly limited power budget is the defining characteristic of modern computer architecture. As an answer to the phase-out of Moore’s Law [12] and Dennard’s scaling [7], computer architects must strive for improved scalability and energy efficiency to propel performance scaling in the post-Moore era [22]. This challenge has led to an architectural shift from exploiting high Instruction Level Parallelism (ILP) towards the exploitation of on-chip Multiple Instruction, Multiple Data (MIMD) parallelism [8].

A common architectural pattern comprises clusters of Processing Elements (PEs) that share tightly-coupled L1 memory through a low-latency interconnect [5]. Graphics Processing Units (GPUs), which dominate most of the Top500 list [21], follow this architectural pattern. For example, NVIDIA Hopper GPUs are composed of several Streaming Multiprocessors (SMs) with four tensor cores and 256 KiB of shared L1 data cache. Each tensor core controls several Fused Multiply-Add (FMA) units, with the whole SM capable of 1024 FP16/FP32 FMA operations per cycle [13].

Despite the diffusion of shared-L1 PE clusters, there is no consensus on how small their PE should be. However, evidence shows that ultra-small cores controlling large functional units can be energetically efficient [26]. Manticore [25] took this approach, using the tiny (22 KGE) Snitch core [26] to build a 4096-core system composed of four compute chiplets. Each chiplet contains 128 clusters, each featuring 128 KiB of tightly-coupled L1 memory and eight small Snitch cores equipped with large double-precision Floating Point Units (FPUs). Another example is MemPool [5], a scaled-up Snitch-based Snitch with 256 cores sharing 1 MiB of L1 Scratchpad Memory (SPM) accessible by all cores within at most five cycles of zero-load latency. However, there is a fundamental trade-off between the number of PEs and the von Neumann Bottleneck (VNB), i.e., the memory traffic and energy overhead due to the instruction fetching mechanism and related logic [4]. Therefore, maximizing the PE’s
instruction fetch efficiency is the key challenge for improving the overall system’s energy efficiency.

Instead of scaling by exploiting MIMD, the Single Instruction, Multiple Data (SIMD) parallelism tackles the VNB by executing the same instruction on several chunks of data. In particular, the vector-SIMD approach promises to reach very high performance and energy efficiency numbers without requiring the ultra-wide datapaths of packed-SIMD-based architectures [10]. Moreover, by exploiting Data Level Parallelism (DLP), vector engines are potentially the most efficient approach to tackle the VNB.

From its inception with the Cray-1 machine to the modern A64FX [23], vector processing has always been associated with supercomputers. Vector processors usually include all microarchitectural tricks to increase ILP, e.g., renaming, out-of-order execution, speculation, and branch prediction, which increase the area and energy overhead of classical high-performance vector processors. However, the defining characteristic of a vector processor is not ILP but DLP. This key observation has led to the design of more streamlined vector cores where most hardware resources are dedicated to DLP support, i.e., a wide Vector Register File (VRF) with parallel execution lanes [6]. In this vein, the idea of an embedded vector machine is gaining traction with modern vector instruction set architectures (ISAs). Arm’s M-Profile Vector Extension (MVE) [2] and the Zve+ subset of the RISC-V Vector Extension (RVV) [17] both target small vector machines for edge data-parallel processing, as opposed to high-performance computing.

Ultimately, the key benefit of a vector ISA is that the fetch and decode cost of a single vector instruction can be amortized over many data-processing cycles. In this paper, we explore for the first time vector processing as an option to build small and efficient PEs for large-scale clusters with tightly-coupled L1 memory. We propose Spatz, a compact 32-bit vector machine based on the embedded subset of the RISC-V Vector Extension version 1.0 [17]. We use Spatz as a building block to improve the performance and efficiency of a many-core cluster. The contributions of this paper are:

- The physically-driven microarchitectural design of Spatz, a parametric, small 32-bit vector unit based on the Zve32x subset of RVV version 1.0. Spatz uses a generic accelerator interface, allowing it to work in tandem with any scalar core compatible with this interface (Section 2);
- A performance analysis of Spatz and Spatz-based MemPool instances on key data-pair kernels. The resulting system is highly scalable, achieving the roofline boundary of reachable performance on a wide range of kernels and core-count configurations (Sections 3 and 4);
- The architectural exploration and physical implementation of Spatz with post-place-and-route results in the modern GlobalFoundries’ 22FDX Fully Depleted Silicon on Insulator (FD-SOI) technology. We compare the baseline MemPool design with the Spatz-based MemPools in terms of area, power consumption, energy efficiency, and area efficiency. The Spatz-powered MemPool reaches 285 GOPS, 71% higher than the baseline design, all with a power consumption 13% lower. By using Spatz as its PE, we more than double MemPool’s energy efficiency, reaching 266 GOPS/W (Section 5);
- Insights about using a small vector-processor-based PE as the building block of a large shared-L1 many-core system in terms of scalability, performance, energy efficiency, and programmability (Sections 6 and 7).

Our design is open-sourced under a liberal license¹.

2 ARCHITECTURE

Spatz is a small parametric vector unit based on the RISC-V Vector Extension (RVV) version 1.0, supporting instructions from the RVV Zve32x subset for embedded vector machines. This section describes Spatz’ architecture, highlighting its main components.

Figure 1 details the microarchitecture of Spatzₙ, a Spatz instance with N Multiply-Accumulate Units (MACUs), and its integration within the MemPool tile. Spatz has a latch-based VRF, divided into four banks with three read ports and one write port (3R1W). The VRF serves data to Spatz’ functional units. Spatz’ controller is responsible for keeping track of the in-flight vector instructions and the interface with the scalar core, in our case Snitch, which is responsible for executing scalar instructions and forwarding vector instructions to Spatz. Snitch and Spatz form a Core Complex (CC).

Figure 1: Microarchitecture of Spatzₙ, a Spatz instance with N MACUs, and its integration in a small shared-L1 cluster.

Spatzₙ is integrated within a small-scale shared-L1 cluster with 16 KiB of local memory, divided into 16 Static Random-Access Memory (SRAM) banks with 1 KiB each. Each CC has a private latch-based L0 Instruction Cache (I$) of 128 B and share 2 KiB of L1 I$. An address-based demultiplexer decides whether the CC memory requests are forwarded to the Advanced eXtensible Interface (AXI) interface or the logarithmic crossbar between the CCs and L1 SRAM banks.

2.1 Instruction Dispatch

Spatz implements a subset of the RVV ISA, version 1.0 [17]. Notably, we target the Zve32x subset, designed for small embedded vector machines with 8-bit, 16-bit, and 32-bit integer support. Out of the Zve32x subset, Spatz does not currently support vector reductions or scatter-gather operations. However, our centralized VRF means that adding support for vector permutation instructions should not affect Spatz’ microarchitecture (Section 2.3). Further extending Spatz towards full compliance with Zve32x is on our roadmap.

¹Footnote hidden for double-blind review purposes.
Spätz is processor-agnostic. It communicates with the scalar core through the generic CORE-V X-Interface accelerator interface [14]. Therefore, Spätz can interface with any core compatible with the X-Interface. Our choice of using Snitch is justified by its extremely lightweight footprint, adapted for a vector execution paradigm where most of the computation happens in the vector machine.

Unfortunately, since the interface specification is still in its infancy, it was not well-adapted for the memory bandwidth requirements of a vector machine. We extended the X-Interface to consider cases where the accelerator makes its memory accesses through a memory interface much wider than the scalar cores’ one. We guarantee ordering between Spätz and Snitch memory requests by stalling the scalar core’s Load/Store Unit while Spätz’ Vector Load/Store Unit executes a memory operation and vice-versa.

2.2 Controller
Snitch only pre-decodes vector instructions, dispatching the vector instruction and any scalar operands to the vector unit. Spätz’ controller decodes the vector instructions, keeps track of their execution, and acknowledges their completion with Snitch.

The controller also manages the Control and State Registers (CSRs) of the RVV ISA. For example, the vlen CSR defines the vector length of all vector instructions. Another important CSR is vtype, which controls the vector elements’ width and whether physical vector registers are grouped into longer logical vector registers. This grouping, called Length Multiplier (LMUL), allows for a logical vector length of eight times longer than the machines’ vector length, at the expense of fewer available logic vector registers.

Finally, the controller orchestrates the execution of the vector instructions in the functional units. The scoreboard keeps track of how many elements of each vector instruction were committed into the VRF. Hazards between vector instructions are handled through operand backpressure. Spätz supports chaining by calculating the hazards on a per-element basis.

2.3 Vector Register File
The VRF is the heart of any vector machine. In Spätz, we decided on a multi-banked multi-ported VRF with four 3R1W banks. Each bank is implemented as a latch-based Standard Cell Memory (SCM). Spätz’ VRF is also centralized and serves all Spätz’ functional units. The VRF ports match the throughput requirements of the $\text{vmacc}$ instruction, which reads three operands to produce one result. Each bank is 8\text{-}bit wide, and each of the 32 8\text{-}bit-wide vector registers occupies one row in the four VRF banks. Each VRF port is 32\text{-}bits wide, where $N$ is the number of MACUs in Spätz.

Despite the scaling issues typically associated with multi-ported VRFs [6], the VRF is not a limiting factor for the target MACU count of Spätz. Our vector unit is designed as the PE of a shared-L1 cluster, with a handful of MACUs per Spätz. We can further scale our design by replicating the shared-L1 cluster, connecting them with a low-latency L1 interconnect [5]. This replication has two benefits. First, the resulting many-core system retains its MIMD flexibility. At the same time, the vector units tackle the high-throughput and computing-intensive tasks [18]. Second, only very large problems can efficiently exploit vector machines with large MACU count [6]; hence our MIMD cluster achieves high MACU utilization even when the workload is not suitable for super-wide vectors.

The centralized VRF also helps the implementation of vector permutation instructions, e.g., a vector slide (vd[i] ← vs[i ± shamt]). A lane-based vector architecture, where the vectors of a VRF are divided into lanes based on their index $i$, would need to shuffle the elements and store them in the correct lane, with important scalability implications [6]. Thanks to its centralized VRF, Spätz can efficiently implement vector slides with a barrel shifter.

2.4 Functional Units
Spätz has three functional units: the Vector Load/Store Unit (VLSU), the Vector Arithmetic Unit (VAU), and the Vector Slide Unit (VSLDU).

2.4.1 Vector Load/Store Unit. The VLSU handles the memory interfaces of Spätz, with support for unit-strided and constant-strided memory accesses. The VLSU supports a parametric number of 32-bit wide memory interfaces. By default, the number of memory interfaces $N$ matches the number of MACUs in the design. This implies a peak operation per memory bandwidth ratio of 0.5 OP/B.

Spätz’ independent and narrow memory interfaces allow the reuse of the same 32-bit wide L1 SPM interconnect used by the scalar cores. The independent interfaces also allow fast constant-strided—and potentially scatter-gather—execution, as the VLSU does not need to coalesce requests into wide memory transfers. However, since there is no ordering guarantee between the memory responses of the individual requests, a Reorder Buffer (ROB) sits between the memory interfaces and the VRF. The ROB ensures that the memory responses are written as ordered 32\text{-}N\text{-}bit-wide words to the VRF, simplifying the chaining mechanism in the scoreboard.

2.4.2 Vector Arithmetic Unit. The VAU is Spätz’ main functional unit, hosting $N$ MACUs. The MACU supports 8-bit, 16-bit, and 32-bit elements. Each MACU has a throughput of 32 bits per cycle, regardless of the element width. Within one MACU, execution happens in a packed-SIMD fashion. Figure 2 shows the architecture of one of those MACUs. For area saving purposes, the MACU has four datapaths, one 32-bit wide, one 16-bit wide, and two 8-bit wide. Narrow operations reuse the wide datapaths.

2.4.3 Vector Slide Unit. The VSLDU executes vector permutation instructions. Examples of such instructions include vector slide up/down and vector moves. The unit operates on two private

![Figure 2: Architecture of Spätz’ MACU.](image)
32N-bit wide register banks. Between those two register banks, an all-to-all interconnect allows the implementation of any permutation. Common operations, e.g., slides, produce results at a 32N bits per cycle ratio, which matches Spatz’ other functional units’ peak throughput. The register banks also play a role similar to the ROB of Spatz’ VLSU. Not only the VSLDU does double-buffering on those registers, but it also ensures that the unit commits to the VRF in 32N-bit-wide words, which simplifies the chaining calculation in the scoreboard by increasing its granularity.

3 SPATZ-BASED PROCESSING ELEMENT

In this section, we analyze the performance of a Spatz-based PE with key data-parallel kernels. We consider two differently-sized Spatz configurations, Spatz2 and Spatz4. Their design parameters are summarized in Table 1. All Spatz configurations were designed for a peak operation per memory bandwidth ratio of 0.5 OP/B.

|                  | Spatz2 | Spatz4 |
|------------------|--------|--------|
| #MACUs           | 2      | 4      |
| Vector length [bit] | 256    | 512    |
| VRF size [KiB]   | 1      | 2      |
| Peak performance [OP/cycle] | 4   | 8      |
| Memory bandwidth [B/cycle] | 8   | 16     |

We used the shared-L1 cluster of Figure 1 as the smallest cluster with which we can analyze Spatz’ power, performance, and area (PPA). All considered clusters have four MACUs in total, either in a single Spatz2 CC, two Spatz2 CCs, or four scalar Snitch CCs.

3.1 Performance

We benchmark a single Spatz unit with key compute-bound signal processing kernels. Those kernels operate on matrices stored in local low-latency L1 memory. A Direct Memory Access (DMA) engine can be used to copy data from higher memory levels into the L1 memory, while Spatz operates on local data.

The matmul kernel, the multiplication of two \( n \times n \) matrices, is the prime example of a compute-bound kernel for large matrices. In fact, its arithmetic intensity is \( O(n) \). Spatz’ VRF allows us to tile the matrix multiplication in blocks much larger than the blocks that would fit in the register file of a scalar core. For example, using RVV’s LMULs, we can group up to eight logical vector registers into a single one. In Spatz4, this is a physical vector of 4096 bits, enough to fit 128 32-bit matrix elements. We also benchmarked our system with conv2d, the 2D integer convolution kernel. This kernel also has a large amount of data reuse, with its arithmetic intensity a function of the kernel size \( f \times f \). On a multi-core environment, each scalar core has its copy of the convolution kernel \( K \) to avoid unnecessary banking conflicts in the L1 memory. Spatz implements the conv2d algorithm with optimized vector slides.

The performance results were extracted with a cycle-accurate Register Transfer Level (RTL) simulation of the target kernels. The roofline plot of Figure 3 shows Spatz2’s and Spatz4’s performance on the matmul and conv2d kernels, together with their maximum achievable performance. Spatz4 reaches an almost-ideal MACU utilization for the considered benchmarks. The peak performance for the matmul benchmark is 3.84 OP/cycle (96.0%), and the peak performance for the conv2d benchmark is 3.95 OP/cycle (98.8%). Large kernels also reach very high performance on Spatz2. Its peak performance on the matmul kernel is 7.67 OP/cycle (95.8%) and 7.78 OP/cycle (97.2%) on the conv2d kernel.

![Figure 3: Roofline plot for Spatz2 and Spatz4 PEs running the matmul and conv2d benchmarks. The subscript numbers beside the benchmark names indicate the matrix sizes \( n \) for matmul and the kernel size \( f \) for conv2d.](image)

Figure 3 also shows how gracefully the performance of the vector unit scales for small problems. On Spatz2, even a tiny matmul8 reaches 3.54 OP/cycle (88.6%). In contrast, on Spatz4, we remark a performance degradation for this kernel size, reaching 5.17 OP/cycle. This MACU utilization of 64% is a consequence of the short execution time of the vmacc instructions, which take two cycles to process a matrix row of eight elements. As a result, Snitch must issue a new vmacc every two cycles to keep Spatz’ pipelines full. However, bookkeeping scalar instructions limit the vmacc issue rate to once every three cycles. This limitation translates into a diagonal maximum performance boundary on the roofline plot [6].

The roofline shows that a Spatz-based PE can reach high performance and functional unit utilization even for very small kernels. Moreover, Spatz achieves this without needing a superscalar or out-of-order core. The vector abstraction allows a pseudo-double-issue behavior, with the VAU, VLSU, and VSLDU working in parallel, without the scalar core issuing more than one instruction per cycle. Section 4 will analyze how Spatz performs in a many-core system, with several instances competing for L1 memory bandwidth.

3.2 Synthesis results

We used Synopsys’ Fusion Compiler 2022.03 to synthesize the Spatz- and Snitch-based small-sized shared-L1 clusters of Figure 1 using GlobalFoundries’ 22FDX FD-SOI technology. We target 500 MHz in worst-case conditions (SS/0.72 V/125 °C). Figure 4 shows the post-synthesis area distribution of the Spatz2 and Spatz4 CCs.

The Spatz2-based CC is 193 kGE large, or 97 kGE/MACU. Snitch occupies 12% of it, 23 kGE, while Spatz2 occupies the remaining
Spatz: A Compact Vector Processing Unit for High-Performance and Energy-Efficient Shared-L1 Clusters

ICCAD’22, 30 October–3 November, 2022, San Diego, CA, USA

170 kGE. Spatz’s 1 KiB-large latch-based VRF occupies most of its footprint, 101 kGE. The MACUs are the next largest component of Spatz, occupying a total of 47 kGE. All remaining components have a very small footprint. Notably, Spatz’ controller and associated scoreboard logic occupy only 6 kGE. The Spatz-based CC is 355 kGE large, or 89 kGE/MACU. This normalized footprint is 8% smaller than Spatz’s. Most of Spatz’s footprint is occupied by the 2 KiB-large VRF, which uses 201 kGE. This footprint is twice the footprint of Spatz’s VRF, evidence of the scalability of our architecture. Spatz amortizes the footprint overhead of Spatz’ controller and Snitch, which contributes to the lower normalized footprint of this CC when compared to the Spatz-based CC.

We used Synopsys’ PrimePower 2022.03 to estimate the post-synthesis energy consumption per elementary operation of the Spatz-based cluster in typical conditions (TT/0.80 V/25 °C), using switching activities extracted from a gate-level simulation. Figure 5 shows this energy breakdown when running vload, vadd, vmul, or vmacc instructions, with a vector length of 32 elements of 32 bits.

Figure 5: Breakdown of the Spatz-based cluster’s energy consumption per elementary operation in the vector instruction.

Snitch only consumes 0.12 pJ per elementary operation while issuing instructions to the vector unit. The low energy requirement is because Snitch only needs to issue an instruction every four cycles to keep Spatz’s four MACUs fully utilized. Also of note is the energy efficiency gained from merging the vector-multiply vmul and vector-add vadd instructions into the vector-multiply-accumulate vmacc instruction. Successive vmul and vadd instructions require 13.9 pJ per elementary multiply-accumulate operation, whereas vmacc requires 36% less energy or 7.9 pJ on Spatz. Spatz operates on data stored in its VRF, responsible for most of Spatz’s energy consumption. For example, vmacc reads three operands and writes one result in the VRF per vector operation; the VRF requires 2.9 pJ, 36% of the cluster’s total energy consumption. The VAU is the second major energy consumer, with 2.8 pJ or 35% of the overall consumption. The remaining energy is consumed by several smaller blocks, SRAM banks and interconnect.

Both Spatz-based and Spatz-based clusters are more efficient than the scalar Snitch-based cluster. Figure 6 compares the energy consumption per elementary operation of those clusters. For example, the Spatz-based cluster consumes 5.2 pJ less energy than the Snitch-based cluster with four scalar cores to run a multiply-accumulate instruction. This 40% reduction in energy consumption highlights the feasibility of embedded vector engines to mitigate the VNB in small shared-L1 clusters. Even for very simple arithmetic instructions, such as an addition, the Spatz-based cluster requires 14% less energy than the equivalent Snitch-based cluster.

14% less energy than the equivalent Snitch-based cluster.

Figure 6: Energy consumption per elementary operation of Spatz-based, Spatz-based, and Snitch-based clusters running common instructions. All clusters instantiate 4 MACUs.

The Spatz-based and Spatz-based MemPool tiles have similar energy consumption for the considered instructions. However, the Spatz-based tile has a footprint 8% larger, which might impact its integration and replication at a higher hierarchy level.

4 SPATZ-BASED MEMPOOL CLUSTER

We used Spatz as the PE used to build up the MemPool many-core system. In this section, we analyze this system’s performance, in OP/cycle, on key data-parallel kernels.

4.1 MemPool configurations

MemPool [5] is a highly-parametric design. Its smallest unit, the tile (Figure 1), contains four Snitch cores, 2 KiB of L1 I$ storage divided into 16 SRAM banks, and a fully-connected logarithmic crossbar between the cores and memories. This tile can be replicated to build systems with as low as 16 cores (the "mempool" configuration) to as high as 256 cores (the "mempool" configuration) [5, 16]. We analyze Spatz impact on the PPA of several MemPool configurations, representing a wide range of shared-L1 cluster sizes.

We name a specific MemPool configuration as MemPool, where c is the number of Snitch + Spatz cores in the system, and i is the number of MACUs that each Spatz controls. A MemPool configuration with scalar cores only is called MemPool, where c is the number of Snitches in the system, each controlling a single...
MACU. First, we define a few small \textit{minpool} configurations, all with a peak performance of 32 OP/cycle:

- \textbf{MemPool}_{16} Configuration with 16 Snitch cores;
- \textbf{MemPool}_{4}Spatz\textsubscript{2} Configuration with 8 Snitch + Spatz\textsubscript{2} cores;
- \textbf{MemPool}_{4}Spatz\textsubscript{4} Configuration with 4 Snitch + Spatz\textsubscript{4} cores.

Each Spatz instance has a VRF with a vector length of 128 bit/MACU. In total, all VRFs amount to 8 KiB of L0 storage.

We also define larger \textit{mempool} configurations with the Snitch-only version corresponding to the largest MemPool instance reported by Cavalcante et al. [5]. All larger instances have a peak performance of 512 OP/cycle:

- \textbf{MemPool}_{256} Configuration with 256 Snitch cores;
- \textbf{MemPool}_{128}Spatz\textsubscript{2} Configuration with 128 Snitch + Spatz\textsubscript{2} cores;
- \textbf{MemPool}_{64}Spatz\textsubscript{4} Configuration with 64 Snitch + Spatz\textsubscript{4} cores.

Each Spatz instance has a VRF with a vector length of 128 bit/MACU. In total, all VRFs amount to 128 KiB of L0 storage.

### 4.2 Benchmarks

We benchmark the MemPool instances with the \textit{matmul} and \textit{conv2d} compute-bound signal processing kernels. Our analysis is performed assuming matrices stored in MemPool’s low-latency L1 memory, which is 64 KiB large for the small \textit{minpool} configurations, and 1 MiB for the larger \textit{mempool} configurations. Figure 7 shows the rooflines of the considered MemPool configurations. The Spatz-based MemPool systems reach equal or higher performance than the Snitch-based MemPool systems for both the \textit{mempool} and \textit{minpool} configurations and with all benchmarks.

![Roofline plot for MemPool instances running the matmul and conv2d benchmarks.](image)

Figure 7: Roofline plot for MemPool instances running the \textit{matmul} and \textit{conv2d} benchmarks. The subscript numbers besides the benchmark names indicate the matrix size \(n\) for \textit{matmul} and the kernel size \(f\) for \textit{conv2d}.

Spatz’ high performance and efficiency is fully confirmed in the small MemPool configurations. The MemPools\textsubscript{Spatz\textsubscript{2}} instance reaches 30.6 OP/cycle (95.6%) on \textit{matmul}_{64}. This performance is much higher than MemPool\textsubscript{16}’s, 18.6 OP/cycle (58.1%). Spatz’ performance degrades slightly for small matrices. MemPool\textsubscript{8}Spatz\textsubscript{2} achieves 22.0 OP/cycle (68.8%) on the \textit{matmul}_{16} kernel, with the performance being limited by Snitch’s issue rate. Despite reaching similar performance for large problems, MemPool\textsubscript{8}Spatz\textsubscript{4} performs slightly worse than MemPool\textsubscript{8}Spatz\textsubscript{2} on \textit{matmul}_{16}, reaching 20.0 OP/cycle (62.4%) due to a different \textit{matmul} tiling. The convolution also performs well on Spatz, with MemPool\textsubscript{8}Spatz\textsubscript{2} reaching 29.5 OP/cycle (92.2%) on \textit{conv2d}. MemPool\textsubscript{16}’s performance is competitive with Spatz’ performance, thanks to a handwritten implementation of the \textit{conv2d} kernel.

The advantage of a vector PE grows with large MemPool configurations. On MemPool\textsubscript{256}, for example, the \textit{matmul}_{256} kernel reaches 284 OP/cycle (55.4%). Performance is limited by the data reuse and the \textit{matmul} tiling, which is bounded by Snitch’s scalar register file. The VRF allows for increased data reuse on Spatz, which significantly improves Spatz’ performance. Moreover, vector chaining allows both the VLSU and the VAU to work concurrently, in a pseudo-double-issue behavior. Thanks to that, MemPool\textsubscript{4}Spatz\textsubscript{4} reaches 480.2 OP/cycle (93.1%) when running \textit{matmul}_{256}. While there is some performance degradation for smaller matrices—the MemPool\textsubscript{128}Spatz\textsubscript{2} instance reaches 258.3 OP/cycle (50.4%) on \textit{matmul}_{64}—this is still much higher than MemPool\textsubscript{256}’s performance on the same kernel, which reaches 85.2 OP/cycle (16.6%). With the convolution kernel, MemPool\textsubscript{128}Spatz\textsubscript{2} reaches 332.8 OP/cycle (65.0%) on \textit{conv2d}, higher than MemPool\textsubscript{256}’s 229 OP/cycle (44.7%).

### 5 PHYSICAL IMPLEMENTATION

This section analyzes the post-place-and-route PPA metrics of MemPool group instances that use either Snitch or Spatz as their PEs. We use the mempool group configurations. On the MemPool system, a \textit{group} contains a fourth of the cores and MACUs [5]. Four identical groups form the complete MemPool system, which only contains point-to-point connections between four groups. The group is MemPool’s most timing-critical design, where most of the power is consumed [5]. In the following, we focus on the group alone.

![Placed-and-routed MemPool group instances of MemPool\textsubscript{4}Spatz\textsubscript{4} and MemPool\textsubscript{256}. Images to scale.](image)

Figure 8: Placed-and-routed MemPool group instances of MemPool\textsubscript{4}Spatz\textsubscript{4} and MemPool\textsubscript{256}. Images to scale.
The MemPool4Spatz2 group is 27% larger than the MemPool256 group. As discussed in Section 3.2, Spatz’ extra footprint is due to its VRF. Figure 8 shows the placed-and-routed MemPool4Spatz4 and MemPool256 groups. The MemPool4Spatz2 group of Figure 8a was implemented as a 1.87 mm × 1.87 mm macro, and the MemPool256 group of Figure 8b is a 1.66 mm × 1.66 mm macro. The larger footprint has a small impact on MemPool’s maximum operating frequency, which drops from 485 MHz for MemPool256 to 471 MHz for MemPool4Spatz128. In typical conditions, the three analyzed groups achieve the same operating frequency of around 590 MHz. The critical path of MemPool4Spatz4 is 53 gates long, going from a register in the VLSU boundary, through the VRF’s read interface, and through the VAU, until reaching a register at the VRF’s write port. Overall, Spatz reaches similar frequencies to the rest of the MemPool group despite the length of its critical path and does not limit MemPool’s frequency. Moreover, it is possible to pipeline Spatz’ critical path by adding a pipeline stage at the VRF read interface. MemPool128Spatz2 and MemPool4Spatz4 perform similarly in terms of footprint. Due to the reduced size of the Spatz4 PEs, MemPool4Spatz4’s area is 5% smaller than MemPool128Spatz2’s.

Thanks to the comparable operating frequencies and much-improved MACU utilization, the Spatz-based MemPool systems achieve a peak performance much higher than the Snitch-based MemPool. In particular, MemPool4Spatz4 reaches the highest performance, 285 GOPS, when running a matmul256, 71% higher than MemPool256’s performance, 167 GOPS. Even considering the larger footprint of the Spatz-based groups, MemPool4Spatz4 reaches an area efficiency of 14.2 GOPS/mm², which is 33% higher than MemPool256’s 10.6 GOPS/mm². Concerning the Spatz-based MemPool instances, MemPool128Spatz2 design reaches a slightly lower area efficiency, 12.0 GOPS/mm², due to its lower matmul256 performance and larger footprint compared to MemPool4Spatz4.

5.2 Power and Energy Efficiency

We used Synopsys’ PrimePower 2022.03 to extract post-place-and-route power results of the MemPool group in typical operating conditions (TT/0.80 V/25°C), using switching activities extracted from a gate-level simulation of matmul256. Table 2 summarizes the power results for the considered MemPool instances.

MemPool256 consumes 1.30 W, which is higher than the consumption of both MemPool128Spatz2 and MemPool4Spatz4. Figure 9 shows a power breakdown of the three considered instances.

Snitch is a major contributor to the power consumption of MemPool256, consuming 375 mW, 29% of the system’s overall power consumption. More than half (198 mW, 53%) of the power is consumed by the register file alone. On the other hand, MemPool256’s MACUs consume only 127 mW, comparable to the power consumption of its instruction cache, 81 mW. This shows how the VNB translates into a large energy overhead for dispatching instructions. The unbalance in the power consumption breakdown is even more striking because of the low power consumption of the MACUs, which consume only 10% of MemPool256’s overall energy consumption. Finally, Snitch’s data reuse is limited by the size of its scalar register file. The largest matrix blocks we could fit in the register file is 4 × 4, i.e., the kernel loads eight elements from L1 for every 16 multiply-accumulate operations. Due to this high L1 memory traffic, the interconnects and L1 SPM SRAM banks are responsible for most of MemPool256’s power consumption, 793 mW (61%).

Vector processing amortizes much of the power overheads spotted on MemPool256. Snitch’s power consumption is 92 mW on MemPool128Spatz2 and 44 mW on MemPool4Spatz4, 8% and 4% of their overall power consumption. Spatz’ VRF consumes a large portion of the total power. On MemPool128Spatz2, the VRF consumes 343 mW, 30% of the overall power consumption. That number increases to 367 mW on MemPool4Spatz4, 34% of its total power consumption. Although Spatz’ VRF consumes 85% more power than Snitch’s register files, its capacity is also four times larger. Therefore, the largest matrix blocks we could fit in the VRF are 8 × 8, i.e., the kernel loads 16 elements from L1 for every 64 multiply-accumulate operations. As a result, the VRF acts as an L0 memory level, improving the locality and reducing the rate at which the PEs do expensive memory accesses into the L1 SRAM banks. In turn, this decreases the power consumed by the interconnects and L1 SPM banks, which consume 497 mW (46%) on MemPool4Spatz4.

In terms of energy efficiency, Spatz is an highly viable PE option to build a shared-L1 cluster. It more than doubled the energy efficiency of MemPool256, with MemPool128Spatz2 reaching 234 GOPS/W and MemPool4Spatz4 reaching 266 GOPS/W. Even considering Spatz’ increased footprint, for an area increase of 27% (mostly due to the VRF), compared to MemPool256, we increased the peak performance by 70% and the energy efficiency by 107%.

6 RELATED WORK

To the best of our knowledge, the tightly-coupled cluster of vector processors architecture has not been explored in past literature. Many vector processing units have been proposed in recent years, thanks to new vector ISAs such as Arm’s Scalable Vector Extension (SVE) [2] and RISC-V’s RVV [17]. Examples of such large-scale vector architectures based on the RVV ISA include BSC’s Vitruvius [11], PULP Platform’s Ara [6], and SiFive’s P270 [20] and X280 [19] cores. However, most of those units are large 64-bit vector processors supporting double-precision floating-point operations, attached to high-performance application-class scalar processors; hence they achieve comparatively low efficiency due to the complex micro-architecture of their supporting scalar cores [24].
Small-scale vector units have been proposed for Field-Programmable Gate Arrays (FPGAs), where the leanness of the vector processor is a constraint due to limited FPGA resources. Vicuna [15] is a timing-predictable vector processor compliant with RVV version 0.10, synthesized on a Xilinx Series 7 FPGA. Its VRF was implemented as a multi-ported Random-Access Memory (RAM) due to concerns with timing anomalies with a multi-banked VRF. Vicuna’s largest configuration, comparable to MemPool\textsubscript{128}, achieves up to 117 OP/cycle on an 8-bit \(1024 \times 1024\) \texttt{matmul} kernel. Vicuna’s multi-ported VRF is similar to Spatz’ VRF. To the best of our knowledge, there is no study about Vicuna’s scaling nor an Application-Specific Integrated Circuit (ASIC) implementation of this architecture, making a power or energy efficiency comparison with Spatz difficult. The same can be said about other small-scale RVV vector units demonstrated on FPGAs, e.g., Arrow [1] and AVA [9].

Arm also started exploring embedded vector machines with its Helium MVE, an optional extension proposed as part of the Armv8.1-M architecture [2]. The Arm Cortex-M55 [3] is the first processor to ship with support to MVE. However, to the best of our knowledge, no quantitative assessment of the performance and efficiency of a Cortex-M55 silicon implementation has been reported so far in the open literature; hence a quantitative comparison with Spatz is not possible. For what concerns a qualitative comparison, we observe that the Helium MVE defines eight 128-bit wide vector registers as aliases to the floating-point register file. On the M55 processor, the 64-bit datapath means Helium operates on a “dual-beat regime,” i.e., vector instructions execute in two cycles. This is enough to overlap the execution of successive vector instructions in different processing units without a superscalar core. However, the scalar core needs to frequently issue instructions to the Helium-capable processing unit to keep its pipeline busy. In contrast, Spatz’ longer vector registers and RVV’s LMUL register grouping allow for a maximum vector length of 4096 bits, keeping Spatz\textsubscript{4} busy for 32 cycles. This long execution, as shown by our results, massively amortizes the energy overhead of the scalar core, which is a considerable part of the overall energy consumption even on extremely data-parallel kernels such as the matrix multiplication.

7 CONCLUSION

In this paper, we explored for the first time vector processing as an option to build small and efficient PEs for large-scale clusters with tightly-coupled shared-L1 memory. We proposed Spatz, a compact vector processing unit based on the \(2\text{e}32\times\) embedded integer subset of RISC-V’s RVV extension version 1.0. Spatz is designed as a co-processor compliant with CORE-V’s X-Interface generic accelerator interface. In our case, Spatz was coupled with the Snitch core. The most efficient Spatz configuration, Spatz\textsubscript{4}, has four MACUs, and a centralized latch-based VRF with 2 KiB.

We implemented Spatz\textsubscript{4} with GlobalFoundries’ 22FDX FD-SOI technology and measured its energy consumption when running simple arithmetic and memory operations. Spatz amortizes much of Snitch’s energy consumption on instruction fetching and decoding thanks to the vector processing induced instruction fetch reduction, i.e., by mitigating the VNB. While a small Spatz\textsubscript{4} based cluster needs 7.9 pJ to execute a multiply-accumulate elementary operation, a Snitch-based cluster requires 13.1 pJ, 66% more energy for the same elementary operation, the difference mainly due to the scalar core.

We also explored Spatz’ PE when it is used as a PE on MemPool, a large-scale shared-L1 cluster with 256 MACUs and 1 MiB of L1. On a multi-core Spatz\textsubscript{4} environment, MemPool\textsubscript{64} reaches up to 480 OP/cycle, a MACU utilization of 94%. This performance is much higher than the performance achieved by the Snitch-based MemPool\textsubscript{256}, cluster, \(284 \text{OP/cycle},\) i.e., a MACU utilization of 55%. On the same kernel, MemPool\textsubscript{64} consumes 1.07 W, 18% less than the 1.30 W consumed by MemPool\textsubscript{256} running the same kernel and operating conditions. Spatz amortizes Snitch’s power requirements, responsible for 29% of MemPool\textsubscript{256}’s consumption. Moreover, its VRF improves locality and reduces accesses to the L1 SPM.

In terms of energy efficiency, MemPool\textsubscript{64} reaches up to 266 GOPS/W, more than twice the energy efficiency reached by MemPool\textsubscript{256}, 128 GOPS/W. Even considering Spatz’ impact on the design’s footprint, for an area increase of 27% (mostly attributed to the VRF), compared to MemPool\textsubscript{256}, we increased performance by 70% and energy efficiency by 116%. Spatz’ agile vector architecture allows a highly efficient PE, which improves the energy efficiency of a vast array of architectures and ensures that it is computation and not instruction fetch and decode to consume most of the power.

### Table 2: Post-place-and-route PPA results of MemPool\textsubscript{256}, MemPool\textsubscript{128}, and MemPool\textsubscript{64}.

|                 | MemPool\textsubscript{256} | MemPool\textsubscript{128} | MemPool\textsubscript{64} |
|-----------------|----------------------------|-----------------------------|-----------------------------|
| Area \([\text{mm}^2]\) | 15.8                       | 21.0                        | 20.1                        |
| Area (MemPool group) \([\text{mm}^2]\) | 2.75                       | 3.65                        | 3.50                        |
| Cell Area Utilization (MemPool group) \([\%]\) | 68%                        | 67%                         | 66%                         |
| Operating Frequency (worst-case) \([\text{MHz}]\) | 485                        | 471                         | 472                         |
| Operating Frequency (typical) \([\text{MHz}]\) | 587                        | 591                         | 594                         |
| Peak performance \([\text{GOPS}]\) | 167                        | 270                         | 285                         |
| Area efficiency \([\text{GOPS/mm}^2}]\) | 10.6                       | 12.0                        | 14.2                        |
| Energy efficiency \([\text{GOPS/W}]\) | 1.30                       | 1.15                        | 1.07                        |

(a) Extracted running the \texttt{matmul256} kernel at typical operating conditions.
