An improved frequency meter for atomic magnetometer based on accurate time measurement

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Abstract An improved frequency measurement method using FPGA and TDC (time-to-digital converter) is proposed, and its error analysis is carried out. Instead of measuring more precise counting values of equal-precision frequency measurement, this method obtains the converted frequency indirectly by accurately measuring the time of multiple measured signal cycles. It significantly improves the accuracy of the frequency meter in atomic magnetometer. The method is capable of eliminating the ±1 error of reference signal counting of equal precision frequency measurement method, as well as avoiding the limitation that the measurement range of TDC cannot reach 0. With this method, a prototype of the frequency meter is implemented with very small size. Tests show that the prototype achieved 0.0042 Hz precision and 0.00056 Hz standard deviation in the frequency range of 70 kHz to 350 kHz at the output rate of 10 Hz.

Key words: Larmor precession frequency, frequency measurement, FPGA, TDC (time-to-digital converter), error analysis

Classification: Circuits and modules for electronic instrumentation

1. Introduction

In recent years, high sensitivity magnetometers have attracted more and more attention [1, 2]. It transforms the requirement of magnetic intensity measurement accuracy into the requirement of Larmor precession frequency measurement accuracy. The magnetic field measurement accuracy of the required high-sensitivity magnetometer is supposed to be better than 0.002 nT in the range of 20 000 nT – 100 000 nT while the output rate of the frequency meter is not less than 10 Hz. That is to say, in the frequency range of 70 kHz – 350 kHz, the accuracy of frequency measurement should be less than 0.007 Hz in the high output rate (For cesium atom magnetometer, the corresponding Larmor coefficients between magnetic field signal and frequency signal are about 3.5 Hz/nT) [3, 4].

Many methods can be performed in frequency measurement. But not all methods can be applied in magnetometers. Some methods such as Newton-type technique, adaptive-based algorithm, time-frequency distributions based on the adaptive fractional spectrogram, autocorrelation factor-based algorithm and estimation method using Kronecker’s theorem are still in the theoretical stage [5, 6, 7, 8, 9]. Some methods such as the optical frequency comb technique rely on a huge test system [10]. Some methods such as four-wave mixing and six-port technology have limited range [11, 12]. Some methods such as the all-phase fast Fourier transform (FFT) cymometer are not accurate enough [13, 14]. Comparing comprehensively, frequency counter is one of the most common and basic digital measurement method, which is suitable for frequency measurement in magnetometer. Common methods of frequency counter include direct frequency measurement, direct period measurement and equal precision frequency measurement. Direct frequency measurement method counts the pulse number N within time T and is only suitable for high-frequency signal. Direct period measurement method use the standard high-frequency signal to measures the period T of the measured signal and is only suitable for low-frequency signal. Both of them will produce ±1 period error and have limitations in practical applications. The equal precision frequency measurement method can achieve the equal precision in the entire frequency range, independent of signal frequency. Based on it, several (n) identical equal precision frequency measurement units are implemented on FPGA to improve the accuracy of frequency measurement to 1/n of the original method [15]. A method using FPGA and TDC for high precision frequency measurement was first proposed in [16] which further improve the accuracy of frequency measurement by several orders of magnitude.

This paper presents a novel method of frequency measurement using FPGA and TDC. Instead of measuring more precise counting values of equal-precision frequency measurement [16], this method obtains the converted frequency indirectly by accurately measuring the time of multiple measured signal cycles. It has better accuracy performance than previous works.
according to the error analysis. We have made a frequency meter using this method, and the test proves that its accuracy and output rate meet the requirements.

In this paper, section 2 describes the existing frequency measurement method. Section 3 introduces the improved frequency measurement method proposed in this paper. Section 4 shows the frequency meter with the proposed method. In section 5, the prototype is tested and the test results are analyzed. In section 6, we summarize the work.

2. Equal precision frequency measurement method

The equal precision frequency measurement method is also known as multi-cycle synchronous frequency measurement method [17, 18]. The schematic diagram of equal precision measurement is shown in Figure 1. Two counters start counting the rising edge of the measured signal and the standard signal respectively at the rising edge of the real gate, and stop counting at the falling edge of the real gate. The real gate’s open and close are completely synchronized with the measured signal and the time interval between them is T. In Eq.(1), $N_s$ is the number of the rising edge of the measured signal and $N_0$ the number of the rising edge of the standard signal within the time interval T. Then, the frequency of the measured signal can be obtained:

$$T = \frac{N_s}{f_s} \approx \frac{N_0}{f_0} \quad (1)$$

The equal precision frequency measurement can achieve equal precision in the entire frequency range and have nothing to do with the measured signal frequency. The real gate time is not a fixed value but synchronized with the measured signal, which eliminates the ±1 period error of the measured signal but will produce ±1 period error of the standard signal. The measurement error is expressed as formula (2) [17].

$$\frac{df_5}{f_5} = \frac{df_0}{f_0} \pm \frac{1}{N_0} \quad (2)$$

The error only relates with the gate time and frequency of standard signals. The longer the gate time is, the higher the standard frequency is, and the smaller the relative error of the measured frequency is. However, the frequency of crystal oscillator cannot be infinitely high. One period of the standard signals is also the maximum possible value of $\Delta t_1$ and $\Delta t_2$ in Figure 1(a). The actual value of T can be calculated accurately from Eq. (3).

$$T = \frac{N_0}{f_0} + \Delta t_1 - \Delta t_2 \quad (3)$$

If $\Delta t_1$ and $\Delta t_2$ can be accurately measured, the measurement result of T will be more accurate.

3. Proposed frequency measurement method

Time-to-digital converter (TDC) is a device used to measure time interval, which converts the time interval into the digital output. Digital TDCs use internal propagation delays of signals through gates to measure time intervals with very high resolution [19]. A start pulse propagates through the delay line, and its statuses along the delay line will be recorded by flip-flops triggered upon the arrival of a stop pulse. Then, the time interval between the start and stop pulse is obtained by decoding the statuses [20]. In view of this, the proposed method uses FPGA and TDC to accurately measure the time of multiple cycles of the measured signal.

As shown in Figure 2, after the preset gate open, the real gate is open when the first rising edge of measured signal arrives. At this moment, TDC is given the first start signal and the rising edge of the measured signal begins to be counted. Then, after $k + 1$ rising edge of standard signal arrives, TDC is given the first stop signal and the rising edge of the standard signal begins to be counted. Then, the first TDC measurement result $t_a$ is read. Similarly, after the preset gate stop, the real gate is closed when the first rising edge of measured signal arrives. At this moment, TDC is given the second start signal and the counter for the measured signal is stopped. The count value $N_s$ for measured signal is obtained. Then, after $k + 1$ rising edge of standard signal arrives, TDC is given the second stop signal and the counter for the standard signal is stopped. The count value $N_0$ for standard signal is obtained. Then, the second TDC measurement result $t_b$ is read. There are $k$ standard signal cycles between the start signal and the stop signal.
in these two TDC measurements to avoid the problem of TDC dead time.

The frequency of the measured signal $f_S$ can be obtained from Eq. (4).

$$N_S \times T_S = N_o \times T_o + t_a - t_b$$

Where

$$T_S = \frac{1}{f_S}$$

$$T_o = \frac{1}{f_o}$$

After deformation, we obtain:

$$f_S = \frac{1}{T_S} = \frac{N_S}{N_o + t_a - t_b}$$

Differentiating to the above equation, obtain:

$$\frac{df_S}{f_S} = -\frac{N_o}{f_o} \left(\frac{t_a - t_b + N_o}{f_o} \right)^2$$

$$+ \frac{dN_s}{N_s} \frac{t_a - t_b + N_o}{f_o}$$

For $dN_s = 0$, $dN_o = 0$, $dt_a = dt_b = \pm 45$ ps, thus:

$$\frac{df_S}{f_S} = \frac{N_o}{N_o + t_a - t_b} \times \frac{dN_o}{f_0} - \frac{dt_a}{T_o} - \frac{dt_b}{T_o}$$

Where

$$\frac{dt_a}{T_o} - \frac{dt_b}{T_o} \leq 1$$

$$-1 \leq \frac{t_a}{T_o} - \frac{t_b}{T_o} \leq 1$$

Therefore, comparing formula (9) with formula (2), we can find that the error of the improved method is better than the existing method. The measurement error of the improved method mainly related with the precision of TDC.

We use TDC-GP22 of ACAM company to measure time interval and make it work under measurement mode 1 whose range is 3.5 ns to 2.5 μs (between start signal and stop signal) and channel double resolution is typical 45 ps. The delay of $k$ standard signal cycle time after the start signal ensures that the time between stop signal and start signal is not beyond the measurement range of TDC (no less than 3.5 ns). As shown in Figure 3, $k$ is set to 4.

The principle of the method using FPGA and TDC proposed in [16] is shown in Fig. 1(b). The measured signal $f_S$ of this method is expressed as:

$$f_S = \frac{N_S}{N_o - \left(\frac{t_{b_2} - t_{a_2}}{t_{b_1} - t_{a_2}}\right) f_o}$$

For $dN_s = 0$, $dN_o = 0$, $dt_{a_1} = dt_{b_1} = dt_{a_2} = dt_{b_2} = \pm 45$ ps, the error can be expressed as:

$$\Delta f_S = \frac{\Delta f_0}{f_0} = \frac{\frac{dt_{a_1}}{t_{a_2}} - \frac{dt_{a_2}}{t_{b_2}} - \frac{dt_{b_1}}{t_{b_2}} + \frac{dt_{b_1}}{t_{b_2}}}{N_o + \frac{t_{a_1} - t_{b_1}}{t_{b_2}} - \frac{t_{a_2} - t_{b_2}}{t_{b_2}}}$$

Where

$$t_{a_2} \approx t_{b_2} \approx T_0$$

$$1 \leq \frac{t_{a_1}}{t_{a_2}} \leq 2$$

$$1 \leq \frac{t_{a_1}}{t_{b_2}} \leq 2$$

$$-1 \leq \frac{t_{a_1} - t_{b_1}}{t_{b_2}} \leq 1$$

Comparing formula (13) with formula (9), two extra TDC measurements introduce greater measurement errors. The method proposed in this paper has better performance on accuracy.

4. Frequency meter design

According to our proposed method, a frequency meter is
developed. It mainly includes voltage conversion unit, input signal conditioning circuit, 40 MHz high precision temperature compensate X’tal (crystal) oscillator (TCXO) whose frequency accuracy is 0.1 ppm, FPGA, STM32, TDC and RS485 level conversion units, as shown in Figure 3.

Because the frequency meter must be integrated with the magnetometer probe, thus, the frequency meter into a circular sheet was designed with a diameter of 7 cm and a thickness of 2 cm. This design makes the devices compact and occupies little space for the whole PCB to fit inside the cylindrical probe. A finished frequency meter is shown in Figure 4.

The core of the frequency meter is the FPGA. The internal structure block diagram of FPGA is shown in Figure 5. FPGA realized rising edge counter, TDC configuration unit, SPI communication unit, FIFO, universal asynchronous receiver / transmitter (UART) unit [21] and some other sequential logic circuits or combinational logic circuits. After power-on, the FPGA first configures the mode and parameters of TDC, and then begins to repeat the measurement process. After every measurement, the intermediate results $N_0$, $N_S$, $t_a$ and $t_b$ are sent to STM32. The frequency value is then calculated from the intermediate result and returned to the user by RS485 (RS485 is selected according to the distance of transmission required). Considering the flexibility of the system, users can configure some parameters such as the output rate of the frequency meter or the format of the data output results through RS485. STM32 translates the instructions (such as translating the output rate into threshold time) and sends control signals to the FPGA through the UART. The design of state machine is needed in many modules of FPGA. The measurement process is mainly accomplished by the state transition driven by standard signal and the state transition driven by the measured signal. Therefore, the signal to be measured should enter the FPGA through the clock-specific IO after passing through the conditioning circuit. Meanwhile, the standard signal also drives the

![Fig. 3 Structure block diagram of frequency meter.](image1)

![Fig. 4 Top view and side view of frequency meter.](image2)

![Fig. 5 Internal structure block diagram of FPGA](image3)
state machine of the UART unit, TDC configuration unit and SPI communication unit.

5. Measurements and experimental results

In order to prove its performance in practice, several representative frequency points are selected to measure in the frequency range of 70 kHz – 350 kHz. The signal is obtained by dividing the output of 10 MHz oven controlled X’tal (crystal) oscillator (OCXO) whose frequency accuracy is 0.02 ppm. The 312500 Hz signal after 32-frequency division, 156250 Hz signal after 64-frequency division and 78125 Hz signal after 128-frequency division are measured. We set the output rate of the frequency meter to 10 Hz, and then record 6000 (10 minutes) output results. According to Eq. (9), the theoretical measurement error should be less than $10^{-7}$ of the measured signal. The test results are shown in Figure 6 and the statistical results are shown in Table I.

| True value (Hz) | 78125 | 156250 | 312500 |
|----------------|-------|--------|--------|
| Mean (Hz)      | 78125.000479 | 156250.001056 | 312500.002027 |
| Maximum (Hz)   | 78125.009300 | 156250.002158 | 312500.004148 |
| Minimum (Hz)   | 78124.999796 | 156250.000095 | 312499.999738 |
| Range (Hz)     | 0.000954   | 0.002063 | 0.004410 |
| Standard deviation (Hz) | 0.000134367 | 0.000282395 | 0.000560797 |

Table I The measurement results.

Table I shows that the maximum frequency error is less than 0.0042 Hz (Maximum, Measured at 312500 Hz), which corresponds to the error of magnetic field value 0.0012 nT. It can be estimated that the standard deviation is less than 0.00056 Hz (Measured at 312500 Hz), which corresponds to the error of the magnetic field value 0.00016 nT. It can be seen that the design meets the requirements.

| Precision (Hz) | [15] > 0.0576 | [16] < 0.080 | This work < 0.0042 |
|----------------|---------------|--------------|-------------------|
| Standard deviation (Hz) | < 0.023       | < 0.00056    |

Table II Comparison to previous works.

Table II gives a brief comparison of several reported works. Because time and frequency are inversely proportional, the resolution of frequency measurement is not linear in the whole frequency range to be measured, but related to many parameters. The results in this table are in the case of 10 MHz standard signal, 10 Hz output rate and 70 kHz ~ 350 kHz measured signal. We have selected the high performance TCXO and optimized the conditioning circuit. The test results show that this work has a great improvement on precision.

6. Conclusions

We have designed an improved frequency meter for atomic magnetometer using FPGA and TDC based on accurate time measurement. Compared with the current method, this frequency measurement method achieves smaller error and a great improvement on precision. We have implemented this design in limited space, and it has high flexibility and integration. The test results show that the measurement accuracy meets the requirement in the full measurement range.

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