Development of a sub-nanosecond time-to-digital converter based on a field-programmable gate array

Y. Sano, a,1 M. Tomoto, a Y. Horii, a O. Sasaki, b T. Uchida b and M. Ikeno b

a Nagoya University, Nagoya, Japan
b High Energy Accelerator Research Organization (KEK), Tsukuba, Japan

E-mail: yuta@hepl.phys.nagoya-u.ac.jp

ABSTRACT: The present time-to-digital converter (TDC) chips for the monitored drift tube (MDT) chambers at the ATLAS experiment will be replaced with new ones for the High-Luminosity LHC, expected to begin operation in 2026. The design and the performance of a 24 channel TDC with a variable time binning of down to 0.28 nsec based on a Xilinx Kintex-7 field programmable gate array are reported. The time measurement is provided by a multisampling scheme with quad phase clocks synchronized with an external reference clock. The differential and integral nonlinearities have been measured to be less than half of the time binning. The temperature dependence on the performance is observed to be small. In conclusion the obtained performance of the time measurement is sufficiently high for the use with MDT chambers.

KEYWORDS: Front-end electronics for detector readout; Particle tracking detectors (Gaseous detectors)

1 Corresponding author.

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1 Introduction

The High-Luminosity LHC (HL-LHC) is expected to begin operation in 2026, with a nominal leveled instantaneous luminosity of $5 \times 10^{34}$ cm$^{-2}$sec$^{-1}$. The present time-to-digital converter (TDC) chips for the monitored drift tube (MDT) chambers at the ATLAS experiment [1] will be replaced with new ones to fully exploit the hit rate capabilities of the chambers with a new trigger and readout scheme [2]. The proposed new readout system fulfils not only the full detector readout rate at 1 MHz but also a new MDT hardware trigger at Level-0. A TDC based on a field-programmable gate array (FPGA) is proposed as a candidate for the HL-LHC. The advantages of developing a TDC with an FPGA are the flexibility of modifying the logic and the simplicity of handling high-frequency clocks and high-speed data transfer based on pre-implemented circuits. Figure 1 shows a simplified schematic of the readout system for the MDT chambers proposed for the HL-LHC. The TDC works in synchronization with a 40 MHz reference clock taken from the system of the LHC accelerator. There are two types of TDCs to be implemented. The TDC for the Level-0 trigger is a counter based TDC whose time binning is 12.5 nsec. On the other hand, the TDC for readout is based on a multisampling scheme using quad phase clocks, whose time binning is 0.78 nsec. There are 24 channels for both TDCs.

In this study, a demonstrator of the TDC for MDT chambers at the HL-LHC is developed using Xilinx Kintex-7 FPGA [3]. The performance of the time measurement is evaluated for the TDC for readout. The study is provided not only for the designed time binning of 0.78 nsec but also for a time binning down to 0.28 nsec, which provides useful information about TDC development using FPGAs. The study is provided also with temperature from $-10^\circ$C to $60^\circ$C.
Figure 1. A simplified schematic of the readout system of the MDT chambers at the ATLAS experiment for the HL-LHC.

2 Schematic of TDC

Figure 2 shows a schematic of the TDC for readout. The internal clocks of 320 MHz and 160 MHz synchronized with 40 MHz reference clock are generated with a phase-locked loop circuit provided in the FPGA. In this design, a multisampling scheme using quad phase clocks with frequency of 320 MHz is employed to make time binning of $1/(320 \text{ MHz} \times 4) = 0.78$ nsec. Time measurement is provided in a time window of 6.25 nsec and transferred with 160 MHz clock. The dynamic range of $(1/160 \text{ MHz}) \times 2^{14} = 100 \mu \text{sec}$ is fulfilled by adding the information of 14 bit counter with 160 MHz clock. The time binning of the TDC is variable depending on the reference clock frequency. A reference clock frequency can be set up to 110 MHz, which corresponds to the time binning of 0.28 nsec and the dynamic range of 37 $\mu$sec.

The performance of the time measurement could generally be affected by the variation of the delays between different signal paths in the core of the TDC. The locations of the D flip flops in the core of the TDC are constrained to minimize the difference between signal path lengths. The signal path difference obtained from a simulation is between 0.1 and 0.2 nsec depending on the channels.
3 Demonstrator and test setup

Figure 3 shows a picture of the demonstrator used for the evaluation of the TDC performance. The performance is evaluated for 8 out of 24 channels. The reference clock and the signals are provided from a pulse generator (Agilent 81150A [4]). The standard deviation of time difference between the two leading edges of the pulses is measured to be 30 psec. The data output from the TDC is read out using Ethernet.

![Figure 3. A demonstrator used for performance evaluations.](image)

4 Performance evaluation

4.1 Measurement of the linearity depending on time binning

The differential nonlinearity (DNL) and the integral nonlinearity (INL) have been measured. The DNL is defined for each bin as

\[
DNL_i = \frac{T_i - T_{\text{BIN}}}{T_{\text{BIN}}},
\]

where \(T_{\text{BIN}}\) is the ideal time binning and \(T_i\) is the time difference between the specific bins \(i\) and \(i + 1\). For the measurement of DNL, the output from the core of the TDC is read out for the time difference of the leading edges between the signal clock and the reference clock. By scanning the time difference between signal and reference clocks, the width of a typical time bin can be focused on. The scan is performed with a step size of 100 psec for the time binning of 0.78 nsec and 33 psec for 0.28 nsec.

The results of the measurement of the DNL are shown in figure 4 for the two cases. The measured DNL is less than half of the time binning in both cases. The nonlinearity is dominated by the time difference between signal paths in FPGA. We observe a periodic structure with a cycle of four bins, where the four bins correspond to the four divided signal paths illustrated in figure 2. The nonlinearity for the time binning of 0.28 nsec is larger than the one for 0.78 nsec since signal
path difference with respect to the time binning is larger for the former. The obtained nonlinearity is consistent with the time difference between signal paths obtained from simulations, which is described in section 2. As a measure of the nonlinearity, the deviation $\sigma$ is defined by

$$\sigma^2 = \frac{1}{N} \sum_{i=0}^{N} (DNL_i)^2.$$  \hfill (4.2)

The obtained value of $\sigma$ for the time binning of 0.78 nsec (0.28 nsec) is $0.104 \pm 0.004 (0.28 \pm 0.01)$, respectively.

INL is parameterized in this study by

$$INL = \frac{\langle T_{\text{measured}} \rangle - T_{\text{input}}}{T_{\text{BIN}}},$$  \hfill (4.3)

where $T_{\text{input}}$ is the time difference between the leading edges of input signal clocks and $\langle T_{\text{measured}} \rangle$ is the mean of the time difference measured by the TDC. The time difference is scanned up to 100 $\mu$sec.

The results of the measurement of the INL are shown in figure 5 for the two cases. The measured INL is consistent with zero up to 100 $\mu$sec. Table 1 shows the result of a linear fit using the parameterization $INL = AT_{\text{ideal}} + B$. The uncertainty for the parameter $A$ corresponds to 25 psec over 100 $\mu$sec range.

![Figure 4](image)

**Figure 4.** Results of the measurement of DNL for time binning of 0.78 nsec with a reference clock frequency of 40 MHz (a) and for time binning of 0.28 nsec with a reference clock frequency of 110 MHz (b).

| ref. clock | Time binning | $A$               | $B$               |
|------------|--------------|-------------------|-------------------|
| 40 MHz     | 0.78 ns      | $(0.7 \pm 2.5) \times 10^{-8}$ | $(-3.5 \pm 7.5) \times 10^{-4}$ |
| 110 MHz    | 0.28 ns      | $(-6.9 \pm 7.3) \times 10^{-8}$ | $(-1.6 \pm 0.9) \times 10^{-3}$ |

**4.2 Measurement of the linearity depending on temperature**

The temperature dependence of DNL and INL is evaluated using thermostat chamber ESPEC SH-641 [5]. Figure 6(a) shows the relation between the deviation $\sigma$ of DNL and temperature.
Figure 5. Results of the measurement of INL for time binning of 0.78 nsec with a reference clock frequency of 40 MHz (a) and time binning of 0.28 nsec with a reference clock frequency of 110 MHz (b). Red lines show the results of a linear fit by INL = AT_{ideal} + B. Parameters A and B are shown in table 1.

Figure 6(b) shows the relation between the slope of the linear fit to INL and temperature in the case of a reference clock of 110 MHz, corresponding to a time binning of 0.28 nsec. Temperature dependence is obtained to be small for both DNL and INL in a range from −10 °C to 60 °C.

5 Conclusion

A sub-nanosecond TDC has been developed using Xilinx Kintex-7 FPGA. The time measurement is provided with a multisampling scheme with quad phase clocks synchronized with a reference clock. The time binning is variable depending on the reference clock frequency. The performance is evaluated for the reference clock frequency of 40–110 MHz, which corresponds to a time binning of 0.78–0.28 nsec. The number of implemented channels is 24, eight of which are employed for the measurements. The differential nonlinearity is measured to be less than half of the time binning. The integral nonlinearity is consistent with zero up to the dynamic range of 100 µsec. Temperature dependence on the differential and integral nonlinearity is small in a range from −10 °C to 60 °C. No significant difference is observed between different channels. The obtained performance of the
time measurement is sufficiently high for the drift time measurement of the MDT chambers at the ATLAS experiment. For the actual use of the FPGA-based TDC at the ATLAS experiment, the radiation tolerance needs to be tested.

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