Data acquisition system in Run-0a for the J-PARC E16 experiment

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Abstract—J-PARC E16 is an experiment to examine the origin of hadron mass through a systematic measurement of spectral changes of vector mesons in nuclei. The measurement of $e^+e^−$ pairs from the decay of vector mesons will provide the information of the partial restoration of the chiral symmetry in a normal nuclear density. To resolve a pulse pile-up and achieve good discrimination of $e^\pm$ from the background of a reaction rate of an order of 10 MHz, the data acquisition (DAQ) system uses waveform sampling chips of APV25 and DRS4. The trigger rate and data rate are expected to be 1 kHz and 130–330 MiB/s, respectively.

The DAQ system for readout of APV25 and DRS4 were developed, where events were synchronized by common trigger and tag data. The first commissioning in beam, called Run-0a, was performed in June 2020 with about 1/4 of the designed setup. The DAQ worked with a trigger rate of 300 Hz in the Run-0a and the main bottleneck was a large data size of APV25. Further optimization of the DAQ system will improve the performance.

Index Terms—Data acquisition systems, FPGAs, Front-end electronics, Readout electronics

I. INTRODUCTION

J-PARC E16 experiment aims to investigate the origin of hadron mass through a systematic measurement of spectral changes of vector mesons in nuclei. The measurement will be performed at the high-momentum beam line, which is a newly constructed beam line, at J-PARC Hadron Experimental Facility with a new spectrometer. A 30 GeV proton beam with an intensity of $1 \times 10^{10}$ protons per spill (2-seconds spill per 5.2 seconds cycle) irradiates thin targets. Proton-nucleus ($pA$) reaction occurs at an order of 10 MHz and produces vector mesons ($\rho/\omega/\phi$). If the vector mesons decay outside the nuclei, the measured mass shows the same value in the vacuum. On the other hand, if the vector mesons decay inside the nuclei (i.e. in medium), the mass spectra are expected to be modified due to an effect of the partial restoration of chiral symmetry with a finite baryon density.

E16 focuses on the detection of the $e^+e^−$ pairs from the decay of $\rho/\omega/\phi$ mesons to avoid the final state interactions. Therefore, the detector system was designed to measure $e^\pm$ precisely in a high-rate environment. The spectrometer is composed of silicon strip detectors (SSD) and GEM trackers (GTR) for momentum reconstruction of charged particles, and hadron blind detectors (HBD) and leadglass calorimeters (LG) for electron identification. Fig.1 shows the schematic view of the spectrometer, which is placed inside a dipole magnet. The detector components are modularized so that each module covers $30°$ of horizontal and vertical angles. One module contains SSD (768 channels), three different sizes of GTR (GTR1: $100 \times 100$ mm$^2$, 432 channels, GTR2: $200 \times 200$ mm$^2$, 720 channels, GTR3: $200 \times 200$ mm$^2$, 1,080 channels, ). HBD
TABLE I
E16 DETECTORS, READOUT DEVICES AND NUMBER CHANNELS

| Detector   | Num. of channels | readout chip | digitizer      | Num. of trigger ch. |
|------------|------------------|--------------|----------------|---------------------|
| SSD        | 19,968           | APV25        | APVDAQ         |                     |
| GTR1       | 11,232           | APV25        | SRS-ATCA       |                     |
| GTR2       | 18,720           | APV25        | SRS-ATCA       |                     |
| GTR3       | 28,080           | APV25        | SRS-ATCA       | 624                 |
| HBD        | 39,936           | APV25        | SRS-ATCA       | 936                 |
| LG         | 1,060            | DRS4         | DRS4QDC        | 1,060               |

(1,538 channels), and LG (38 or 42 channels). Table I shows the individual number of readout channels for each detector and there are more than 110,000 in total.

II. DAQ DESIGN

An overview of our data acquisition (DAQ) system is shown in Fig. 2. To resolve the pulse pile-up and to achieve the good discrimination of the background in the offline analysis, waveforms of the readout channels are recorded by using analog memory ASICs of APV25 [2] for SSD, GTR and HBD, and DRS4 [3] for LG, respectively. The sampling speed of APV25 and DRS4 are ~40 MS/s and ~1 GS/s, respectively. In E16 DAQ, there are two types of front-end module for APV25. The first one is APVDAQ [5], which is used for SSD. The second one is SRS-ATCA [6] for GTR and HBD. The front-end module for LG is called DRS4QDC. SRS-ATCA and DRS4QDC will be described in the following sections.

These ASICs have neither a trigger output capability nor a continuous readout feature. To generate a trigger signal, LG and the last amplification layer of GEM foil of GTR3 and HBD are used as the source of the trigger primitive signals [4]. The read out is triggered at 1 kHz and the data rate of ~600 MiB/spill (330 MiB/s in the 2 s beam duration, and an averaged value is 130 MiB/s over 5.2 s beam cycle) is expected when zero-suppression in FPGA is applied.

III. TRIGGER SYSTEM AND EVENT SYNCHRONIZATION

The trigger primitive signals from GTR3, HBD and LG are digitized and merged by Trigger Merger boards (TRG-MRG [8]), and afterwards sent to the trigger decision module (Belle2-UT3 [9]) via high speed optical links. The number of trigger primitive channels are listed in Table I. UT3 generates several types of trigger data: L1 trigger (physics trigger), notification of spill-start or spill-stop, calibration trigger, sampling of hit-number counts and single event upset (SEU) counts, which are encoded in 4 bits. The trigger data and associated tag data are distributed over standard CAT-7 LAN cables and repeater modules, Belle-2 FTSW [10]. The busy signals from the front-end modules are transferred by the same LAN cable and collected. Although the serial data are encoded in B2TT protocol, the distributed clock frequency and line rate are not same as the Belle-2 DAQ, which uses a 127 MHz clock. It is derived from the RF frequency of the SuperKEKB and there is no advantage in using it in the other site. Instead, a 125 MHz clock and 250 Mbps line rate are adopted. The unique tag data consists of 48-bit timestamp (LSB=8 ns), 16-bit spill ID and 32-bit event ID. The received tag data are checked to detect any event synchronization error.

Only SRS-ATCA can be directly connected to FTSW. RPV-260 [11] was designed to play as an interface bridge between RJ45 and KEK-VME backplane bus [12]. For APVDAQ, a trigger interface module (TIM) was developed. TIM is also used as the clock fan-out module to synchronize APVDAQ.

IV. FRONT-END MODULE FOR GTR AND HBD

SRS-ATCA, a variant of CERN-RD51 [13]’s Scalable Readout System [14], was adopted as the front-end module for GTR and HBD. A photo of SRS-ATCA is shown in Fig. 4. The SRS-ATCA hardware was designed by a German company etcSys. The module consists of an ATCA blade (EATCA-101), two mezzanine cards (EAD-M1) and one RTM (ERTM-101). Two main FPAGs of Xilinx Virtex-6 LXT240 on the
blade read the ADC data and manage each mezzanine card and APV25 chips, and one sub FPGA of Xilinx Spartan-6 LX16 configures the main FGAs. Front-end hybrid cards of APV25 and the mezzanine cards are connected by HDMI cables. Each mezzanine card has three 12-bit 8-channel ADCs (Texas Instruments ADS5281) to cope with 24 APV25 chips. Therefore, one SRS-ATCA module can handle $128 \times 24 \times 2 = 6,144$ channels in total. The trigger and tag data, which are encoded in B2TT protocol, are received via the RTM. The data of main FGAs are transferred to PC by UDP.

The firmware of SRS-ATCA has been extended for E16 as follows. Front-end modules are located near the spectrometer, where radiation level is not negligible. Therefore, soft error mitigation (SEM) core was implemented by using Xilinx IP to reduce the SEU failure. In addition, a watchdog timer is implemented to watch the loss of heartbeat from the SEM core. When the heartbeat from the SEM core is lost or the detected error is uncorrectable, the SEM core takes a control of internal configuration access port (ICAP) and reload the firmware from the on-board SPI-ROM to reboot the FPGA. The number of samples per event was chosen to be 24 because the GTR has a long drift time to obtain good position resolution. The APV25 and ADC are synchronized at 41.67 MHz which is derived clock from the global clock of 125 MHz. TDC (LSB=2 ns) is implemented to measure the time difference between the global clock of 125 MHz and the sampling clock of 41.67 MHz. The TDC uses a simple counter running at 500 MHz clock.

### V. Front-end module for LG

A waveform digitizer with DRS4, DRS4QDC, was developed for the LG readout. The board has 16 analog input channels. The input signals are split and fed into DRS4 chips and comparators. The former capture the waveform at 960 MS/s and the latter generate trigger primitives. The board has four DRS4 chips, where a pair of capacitor arrays of DRS4 are cascaded to extend the Level-1 trigger latency up to 2\(\mu\)s. To reduce the data size, only 200 samples in the region of interest (ROI) for each trigger are captured. DRS4 output is digitized by 12-bit 8-channel ADC. Analog Devices AD9367, which is used with a 30 MHz sampling frequency. These chips are managed by a Xilinx Spartan-6 LX150 FPGA. A FPGA-based TCP/IP processor, SiTCP [15], where 100 BASE-T is used for the data transfer. Although 100 BASE-T is enough to send event frames at the data rate of 6.4 MB/s, corresponding to the 1 kHz L1 trigger without zero-suppression (200 sample points $\times 2$ Bytes $\times 16$ channels $\times 1$ kHz), the functionalities of the waveform correction and data size reduction are implemented in the FPGA. First, the offset variation of raw waveform data is corrected with a block-RAM based lookup table. Next, the sequential order of the cascaded-pair data is sorted into a correct order. Then, so-called a symmetric spike noise, which appears around the last capacitor cell in the RoI of the previous trigger, is removed by linear interpolation using the values of neighbor cells of the spike. Next, the sum of the waveform within a specified length is calculated and compared with a threshold to decide whether the channel has a hit or not. Finally, the waveform data of the hit channel is further reduced by a delta-compression. It is a loss-less compression and the difference of the amplitude between the next sample point is calculated and classified to determine the bit width of the packed data structure.

DRS4QDC receives the trigger and tag data via the KEK-VME J0 backplane bus. The KEK-VME J0 bus has 7 differential lines to share the trigger and tag data [12]. The original J0-protocol uses the bus as an asynchronous parallel data bus and doesn’t send more than 5-bit data. However, DRS4QDC uses it as a source-synchronous bus to convey 4-bit trigger data and 96-bit tag data, whereas a backward compatibility is kept. The SEM is also implemented in the same way as SRS-ATCA except for the difference of the FPGA family.

### VI. Beam commissioning

E16 takes a staging approach in the spectrometer construction. Following stages are planned. The first commissioning of detectors and DAQ with beam, called Run-0a, was carried out in June 2020, where about 1/4 of full detectors (namely, 6 SSD, 6 GTR, 4 HBD, and 6 LG) were installed. The second commissioning (Run-0b), is scheduled in January 2021, where 6 SSD, 8 GTR, 6 HBD, and 6 LG will be used. The first physics run with 8 modules is planned in 2022 (Run-1), whereas the experiment with the full-equipped spectrometer will be performed within a few years (Run-2). Schematic views of Run-1 and Run-2 are shown in Fig. 6 and Fig. 11 respectively.
In Run-0a, an online event building software was not ready. Thus, data of the front-end modules were collected by separate processes for each module and written into the hard disks, while the trigger and tag were common to them. One PC with two Intel Xeon E5-2630 v4 10-core processors, DDR4 256 GB RAM, a network card of Intel X710D4 (10 Gbps×4, only 22 ports were enabled), and CentOS 7 operating system was used for the data collection of 4 SRS-ATCA and 18 DRS4QDC. For readout of 12 APVDAQ, the J-PARC hadron DAQ software [12] was used, where two single-board computers (SBCs), XVB601 and XVB602, were installed and each SBC passed data of 6 APVDAQ to the recorder PC. A data merger software based on ZeroMQ (FairMQ [16]) was developed and used for TRG-MRG and UT3.

The measured DAQ rate was approximately 300 Hz. The main bottleneck was that a long dead time of ∼3 ms in SRS-ATCA, where no zero-suppression was applied in the FPGA.

VII. SUMMARY AND OUTLOOK

J-PARC E16 experiment has successfully commissioned in June 2020 to investigate the origin of the hadron mass. The DAQ system adopted waveform sampling with analog memory chips of APV25 and DRS4. The front-end module and/or the readout firmware of those chips were developed. During the first beam commissioning, about 1/4 of full-equipped setup was installed. The DAQ worked with a trigger rate of approximately 300 Hz, which was 1/3 of the design goal. It was caused by the long data transfer time of 3 ms in SRS-ATCA.

Further developments are in progress. To improve the trigger accept rate, development of the zero suppression firmware as well as an FIR filter to compensate the signal distortion by a long transmission line are ongoing for SRS-ATCA. We also test parallel readout of APVDAQ by using MOCO [17] and an upgraded module. Moreover, the development of the DAQ online software for event-building and monitoring is to be done.

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