A note on load balancing in DC microgrids

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Abstract—A problem of load balancing in isolated DC microgrids is considered in this paper. Here, a DC load is fed by multiple heterogeneous DC sources, each of which is connected to the load via a boost converter. The gains of the DC Converters (DCC’s) provide for a means to control the division of load current amongst the DC sources. The primary objective of the control scheme is to minimise the total losses in the network, while maintaining the output voltage within a desired range, serving the load current demand and adhering to VI-characteristics of the power sources. Under assumptions of concavity/monotonicity/piece-wise-linearity of the VI-characteristics, the problem is solved using a convex relaxation. It is shown that the solution to the relaxed problem is tight. Thus, the resulting algorithm is guaranteed to reach global optimality in a numerically efficient manner [1]. Simulations are provided for corroboration.

Index Terms—Convex Optimization, DC-DC power converters, Load Balancing

I. INTRODUCTION

Consider the circuit shown in Figure 1. The heterogeneous VI-characteristic curves (output voltage vs current drawn) beside represent the power sources. It is assumed that all these curves are positive, piece-wise linear (PWL), concave and non-increasing (A1). This assumption aids analysis and isn’t impractical since several power sources exhibit concave/non-increasing VI-characteristics [2]. Moreover, any concave curve can be well-approximated as a PWL curve [1]. The internal resistances of these sources, $R_{s1}, R_{s2}, \ldots, R_{sk}$ are considered separately. Each source is connected to the load via a DC-DC converter (DCC). Large capacitive filters at the input of the DCC’s reduce current ripple in the power sources (A2). It is assumed that the DCC’s belong to the boost class (A3). The DCC outputs connect to the load via cables which have resistances, $R_1, R_2, \ldots, R_k$. The load is assumed to be resistive (A4), and the load voltage must be in a desired range. It is assumed that the minimum of range is greater than the open circuit voltages of all power sources (A5). The objective here is to set the DCC gains (control inputs) so as to minimize the total steady state (when current-sec and volt-sec balances hold) losses in the system. The resistive losses in the cables and the internal resistances, and those in the DCC’s are considered. It is required that the DCC’s are operated in the Continuous Conduction Mode (CCM) for its ease of analysis (A6).

Such scenarios arise in systems fed by multiple renewable sources, such as solar panels, fuel cells, lithium-ion/lead-acid batteries and windmills [3]. The variations in the power inputs change the VI-characteristic curves. Thus, an appropriate control strategy is needed to balance the load current and regulate the load voltage. Out of the several possibilities of load balancing it is advantageous (for example, efficient thermal management in DCC’s) to choose one which minimizes the total losses. The losses in the DCC’s are due to conduction and switching. It is also assumed that the conduction losses due to current ripples and the capacitors are negligible (A7).

There exists prior research work in this field. The authors of [4] consider a similar problem in an isolated DC microgrid and propose a metric termed as droop index, which measures the performance of the network. The performance is a function of the current difference between branches and the cable losses at the output side of the DCC’s. The authors of [5] propose a decentralized control scheme to regulate the load voltage. The scheme depends only on the output voltage and output current of a branch, thereby not requiring a communication between the DCC’s and a central controller. The authors of [6] present an optimization methodology for determining droop resistances, chosen from a discrete set of resistance, for the generation units in network so as to minimize the resistive losses in the network. The focus of all the references mentioned here is to introduce a virtual resistance (called droop resistance) to improve current sharing amongst the loads, while regulating voltage. To the best of the authors’ knowledge, an approach similar to the one presented in this paper for load balancing in DC microgrids which considers (i) arbitrary concave non-increasing PWL VI-characteristic curves, (ii) the losses in DCC’s, the internal resistances and the cables, (iii) maintains an output voltage within a desired range and (iv) caters to a current demand, has not been discussed in literature.
II. THE OPTIMIZATION PROBLEM
The following notations describe the variables in a network with N branches (see 5).
- \( \{V_{s1}, V_{s2}, \ldots, V_{sN}\} \) - average source voltages.
- \( \{I_{s1}, I_{s2}, \ldots, I_{sN}\} \) - average source currents.
- \( \{i_{s1}(t), i_{s2}(t), \ldots, i_{sN}(t)\} \) - instantaneous source currents.
- \( \{V'_{1}, V'_{2}, \ldots, V'_{N}\} \) - average input voltages.
- \( \{V''_{1}, V''_{2}, \ldots, V''_{N}\} \) - average output voltages.
- \( \{I_{1}, I_{2}, \ldots, I_{N}\} \) - average output currents.
- \( \{id_{1}(t), id_{2}(t), \ldots, id_{N}(t)\} \) - diode currents.
- \( \{im_{1}(t), im_{2}(t), \ldots, im_{N}(t)\} \) - MOSFET currents.
- \( \{vd_{1}(t), vd_{2}(t), \ldots, vd_{N}(t)\} \) - diode-anode voltage.

The following are known parameters of the circuit.
- \( f_k(x) = \min_{i \in \{1, \ldots, P_k\}} \{\beta_{k,i}x + \gamma_{k,i}\}, \beta_{k,i} < 0 \forall k, i \) (see A1).
- \( \{R_{s1}, R_{s2}, \ldots, R_{sN}\} \) and \( \{R_{1}, R_{2}, \ldots, R_{N}\} \) - source resistances and cable resistances, respectively.
- \( R_{\text{load}} \) - the load resistance.
- \( \{R_{L,1}, R_{L,2}, \ldots, R_{L,N}\} \) - DC resistances of inductors.
- \( \{V_{\text{load,min}}, V_{\text{load,max}}\} \) - load voltage range.
- \( \{I_{s1,\text{min}}, I_{s2,\text{min}}, \ldots, I_{sN,\text{min}}\} \) - minimum average input currents to ensure CCM.
- \( \{I_{1,\text{min}}, I_{2,\text{min}}, \ldots, I_{N,\text{min}}\} \) - minimum average output currents to ensure CCM.
- \( \{g_{1,\text{max}}, g_{2,\text{max}}, \ldots, g_{N,\text{max}}\} \) - maximum DCC gains.
- \( \{\lambda_1, \lambda_2, \ldots, \lambda_N\} \) and \( \{\mu_1, \mu_2, \ldots, \mu_N\} \) - weights.
- \( \{R_{M,1}, R_{M,2}, \ldots, R_{M,N}\} \) - DS resistances of MOSFETs.
- \( \{V_{D,1}, V_{D,2}, \ldots, V_{D,N}\} \) - FB voltages of diodes.
- \( \{R_{D,1}, R_{D,2}, \ldots, R_{D,N}\} \) - diode resistances.
- \( \{\alpha_1, \alpha_2, \ldots, \alpha_N\} \) - multiplicative constants for switching losses.

From here, \( (t) \) will be dropped for brevity and bold letters will denote optimal values.

A. The Construct

Consider the optimization problem mentioned below:

\[
\min_{k=1}^{N} \sum_{k=1}^{N} \lambda_k \left\{ I_{s,\text{rm}}^2 (R_{s,k} + R_{L,k}) + (im_k)^2 R_{M,k} \right\},
\]

\[
\cdots + (id_k)^2 R_{D,k} + V_{D,k}I_k + \alpha_k (vd_k im_k)_{\text{peak}} \right\} \] (1)

subject to

\[
V'_{k} = V_{s,k} - I_{s,k} R_{s,k}, \quad V''_{k} = V_{\text{load}} + I_{k} R_{\text{load}}, \quad \forall k,
\]

\[
\sum_{k=0}^{N} I_k = \frac{V_{\text{load}}}{R_{\text{load}}}, \quad V_{\text{load,min}} \leq V_{\text{load}} \leq V_{\text{load,max}}.
\] (2)

\[
V'_{k} \leq V''_{k} \leq g_{k,\text{max}} V'_{k}, \quad V_{s,k} = f_k(I_{s,k}), \quad \forall k,
\] (3)

\[
V_{s,k} R_{s,k} = \left\{ I_{s,\text{rm}}^2 (R_{s,k} + R_{L,k}) + (im_k)^2 R_{M,k} \right\}, \cdots + (id_k)^2 R_{D,k} + V_{D,k}I_k + \alpha_k (vd_k im_k)_{\text{peak}} + V_{\text{load}}I_k \right\}, \quad \forall k,
\] (4)

\[
I_{s,k} \geq I_{s,k,\text{min}}, \quad V_{s,k}, I_{s,k}, V'_{k}, V''_{k} \geq 0, \quad \forall k.
\] (5)

Modifications to this problem leads to the main algorithm shown in Figure 2.

1) The Cost Function: The objective function is the weighted sum of losses in the network. The weight of a branch can be interpreted as its per unit energy cost. Due to the large input and output capacitors (see A2), the losses in the cables and the internal resistances of the kth branch is

\[
I_{s,k}^2 R_{L,k} + \frac{1}{4} \sum_{k=0}^{N} \lambda_k \left( I_{s,k}^2 (R_{M,k} - R_{D,k}) \right) \cdots + (I_k + I_{s,k})^2 \frac{R_k}{2} + (I_{s,k} - I_k)^2 \frac{R_{D,k}}{2} \cdots + \alpha_k (V_{\text{load}} - I_{s,k} R_{\text{load}}) + I_{D,k} + \alpha_k (vd_k im_k)_{\text{peak}} + \frac{1}{4} \sum_{k=0}^{N} \lambda_k \left( I_{s,k}^2 (R_{M,k} - R_{D,k}) \right) \] (6)

This approximation is valid since the RMS of a waveform with a linear deviation of 40% of its average value is [2]

\[
\frac{\text{rms}(is_k)}{2} = \frac{1}{2} + \frac{0.4^2}{12} \approx \frac{1}{2} \] (9)

Therefore, the cost function is

\[
\sum_{k=0}^{N} \lambda_k \left\{ I_{s,\text{rm}}^2 (R_{s,k} + R_{L,k} + R_{M,k} + \alpha_k R_{D,k}) \right\},
\]

\[
\cdots + I_{s,k} I_k \left( \alpha_k R_{s,k} - (R_{M,k} - R_{D,k}) \right) \cdots + \alpha_k (V_{\text{load}} + V_{D,k}) \left( I_k + \alpha_k I_{s,k} \right) \right\} \]

The above can be modified further as

\[
\sum_{k=0}^{N} \lambda_k Q_k = \sum_{k=0}^{N} \lambda_k \left\{ I_{s,\text{rm}}^2 (R_{e1} - R_{e2}) \right\},
\]

\[
\cdots + (I_k + I_{s,k} \alpha_k)^2 \frac{R_k}{2} + \sum_{k=0}^{N} \lambda_k \left( I_{s,k}^2 (R_{M,k} - R_{D,k}) \right) \cdots + \alpha_k (V_{\text{load}} + V_{D,k}) \left( I_k + \alpha_k I_{s,k} \right) + I_{D,k}^2 R_{e3} \right\},
\] (16)
where \( s = \text{sign} (R_{M,k} - R_{D,k}) \),
\[
R_{ef1} = (R_{Sk} + R_{L,k} + R_{M,k} + \alpha_k R_{D,k}) ,
\]
(17)
\[
R_{ef2} = \left( \frac{|R_{M,k} - R_{D,k}|}{2} + \frac{\alpha_k^2 R_k}{2} \right) ,
\]
(18)
\[
R_{ef3} = \left( \frac{R_k - |R_{M,k} - R_{D,k}|}{2} \right) .
\]
(19)
The expression for cost is convex iff
\[ R_{ef1} \geq R_{ef2} \text{ and } R_{ef3} \geq 0. \]
(20)
These are not impractical for the following reason. From [2],
\[
\alpha_k \approx \frac{1}{2} (\tau_{ON} + \tau_{OFF}) f_s ,
\]
(21)
where \( \tau_{ON} \) and \( \tau_{OFF} \) are ON and OFF transition times for a MOSFET. Typically, \( f_s = 100 \) KHz, and \( \tau_{ON} + \tau_{OFF} = 100 \) ns, which imply that \( \alpha_k \approx 0.005 \). With an inductor DCR of \( \Omega \), a source resistance of \( 500\Omega \), MOSFET DSR of \( 200\Omega \), diode resistance of \( 30\Omega \) and a cable resistance of \( 1\Omega \) the bounds read
\[
1.7 \geq 0.115 \text{ and } 1 \geq 0.115 .
\]
(22)
Thus, the two conditions are satisfied with healthy margins. In some cases, a weighted combination of the absolute circulating currents (arising due to DCC output voltage differences) in the network is added to the cost. Mathematically, the additional cost is [4]
\[
\sum_{k=1}^{N} \mu_k |I_{ck}| = \sum_{k=1}^{N} \mu_k \sum_{j \neq k} \left| V_{k}'' - V_{j}'' \right| .
\]
(23)
It will be shown the qualitative aspects of the solution remain unchanged, even with this additional cost.

2) The Constraints: The first set of constraints are the Kirchoff’s Voltage Laws (KVL) applied to the input and the output side of the DCC’s. The second constraint is the Kirchoff’s Current Law (KCL) applied to load node. The third constraint bounds the output voltage within the desired range. The fourth set of constraints bounds the gains of the DCC’s. The following expression gives an upper bound on the the gain of the \( k \)th DCC [2],
\[
(1 - D) \frac{V_{D,k}}{V_{in}} D' (R_k + R_{load}) (D')^2 (R_k + R_{load}) + D'R_{D,k} + DR_{M,k} + RL_k ,
\]
(24)
where \( D' = 1 - D \). To get rid of its dependence on the input voltage, suppose that
\[
V_{k}' \geq 20V_{D,k} .
\]
(25)
Then a conservative upper bound would be
\[
\max_{D} \left\{ \frac{0.95D' (R_k + R_{load}) (D')^2 (R_k + R_{load}) + D'R_{D,k} + DR_{M,k} + RL_k}{(D')^2 (R_k + R_{load}) + D'R_{D,k} + DR_{M,k} + RL_k} \right\} .
\]
(26)
The fifth set give the power sources their VI-characteristics (see A1). The sixth set ensures that the input power to the DCC is equal its output power plus the losses [2]. To derive the functional form of this constraint, note that
\[
V_{k}' Is_{k} = V_{k}'' I_{k} + Q_k
\]
\[
\Rightarrow (V_{s_k} - I_{s_k} R_{s_k}) I_{s_k} = (V_{load} + I_{k} R_{k}) I_{k} + Q_k
\]
\[
\Rightarrow V_{s_k} I_{s_k} = I_{s_k}'' R_{s_k} + Q_k + I_{k}'' R_{k} + V_{load} I_{k}.
\]
(27)
Substituting for \( Q_k \), one obtains the seventh set. The last set constraining voltages and currents to be non-negative, ensures that power is only drawn from sources. Now, suppose that the following lower bounds hold
\[
I_{s_k} \geq \frac{\min \{V_{s_k}\}}{f_{s} L_{k}} , \forall k .
\]
(28)
B. The Convex Relaxation
In a series of steps, it shall be shown that the a convex relaxation of the problem can be used to obtain the globally optimal solution to the original non-convex problem. As the first step, let \( V_{load} \) be fixed to a value \( V_{load} \) within the desired range. Let the solution be \( P = \{ V_{s1}, \ldots, V_{sm}, V_{1}', \ldots, V_{m}', V_{1}'', \ldots, V_{m}'', I_{s1}, \ldots, I_{sm}, I_{1}, \ldots, I_{m} \} \). Let the optimal cost be \( C \). Now, suppose for some \( \delta > 0, V_{load} - \delta \) is also within the range. Then the point \( P_{\delta} = \{ V_{s1}, \ldots, V_{sm}, V_{1}', \ldots, V_{m}', V_{1}'', \ldots, V_{m}'', I_{s1}, \ldots, I_{sm}, I_{1}, \ldots, I_{m} \} \) is a feasible point for the opt-problem with the load voltage being \( V_{load} - \delta \), the cost of which is also \( C \). Note that the assumption \( A5 \) is necessary to prove feasibility of \( P_{\delta} \). Thus, the optimal cost with the load voltage being \( V_{load} - \delta \) cannot be more than \( C \). These arguments also hold good with the addition cost term given in (23), since the difference between the output voltages of the DCC’s in \( P_{\delta} \) remain unchanged. Thus, the optimum occurs when the load voltage is set to the range-minimum. This fact shall be used later.

For the second step, note that the sixth set of constraints are non-convex, as the functions \( f_{k} \)’s need not be affine. Since \( f_{k}(\cdot) \)’s are concave, a standard convex relaxation would be the following change
\[
V_{s_k} = f_{k}(I_{s_k}) \rightarrow V_{s_k} \leq f_{k}(I_{s_k})
\]
(29)
The seventh set of constraints are also non-convex [1]. A convex relaxation is achieved in the following way. With the assumption that the \( f_{k}(\cdot) \) is a PWL concave decreasing function (see A1), note that
\[
V_{s_k} I_{s_k} = f_{k}(I_{s_k}) I_{s_k} = \min_{j \in [1, P_k]} \left\{ \beta_{k,j} I_{s_k}^2 + \gamma_{k,j} I_{s_k} \right\} .
\]
(30)
1) Set $V_{\text{load}}$ to $V_{\text{load,min}}$. Ensure that circuit parameters adhere to all assumptions.

2) Solve the following:

$$\min_{k=0}^{N} \left\{ I_s^2 (R_{e1} - R_{e2}) + (I_k + I_{sk, \alpha})^2 \frac{R_k}{2} + (I_k - sI_k)^2 \frac{|R_{M,k} - R_{D,k}|}{2} + \alpha_k V_{\text{load}} I_k + V_{D,k} I_k + I_k^2 R_{e3} \right\}$$

subject to

$$V_k' = V_{sk} - I_{sk} R_{sk}, \quad V_k'' = V_{\text{load}} + I_k R_k, \quad \sum_{k=1}^{m} I_k = \frac{V_{\text{load}}}{R_{\text{load}}}, \quad V_k' \leq V_k'' \leq g_{k,\max} V_k', \quad V_{sk} \leq f_k (I_{sk}) \quad \forall k,$$

$$\min_{j \in [1, p_k]} \left\{ \beta_{k,j} I_s^2 + \gamma_{k,j} I_{sk} \right\} \geq I_s^2 (R_{e1} - R_{e2}) (I_k + I_{sk, \alpha})^2 \frac{R_k}{2} + (I_k - sI_k)^2 \frac{|R_{M,k} - R_{D,k}|}{2} \cdots$$

$$\cdots + \alpha_k V_{\text{load}} I_k + V_{D,k} I_k + I_k^2 R_{e3} + V_{\text{load}} I_k \quad \forall k,$$

$$I_k \geq I_{k,\min} \forall k, \quad I_k, I_{sk}, V_{sk}', V_{sk}'' \geq 0 \forall k, \quad V_k' \geq 20 V_{D,k}, \quad \forall k \quad \forall k,$$

$$3) \text{If feasible, and for some } k, \quad V_{sk} < f_k (I_{sk}), \quad \text{then set } V_{sk} \text{ to } f_k (I_{sk}), \quad \text{set } V_k' \text{ to } V_k' + f_k (I_{sk}) - V_{sk}.$$
given by the smaller positive root of the following equation
\[
\min_{j \in [1,P_k]} \{ \beta_{k,j} I_{s,k}^2 + \gamma_{k,j} I_{s,k} \} = Q_k + V_{load} I_{k,min}.
\] (33)

If such a root does not exist, there is no feasible solution to the optimization problem. However, the equivalence holds under the assumption that
\[
\frac{\partial (Q_k + V_{load} I_k)}{\partial I_k} \geq I_{s,k} (R_{M,k} - R_{D,k}) + V_{load} \geq 0, \quad \forall I_{s,k}.
\] (34)

To see the reason, note that for fixed output currents, the curve of the LHS is concave, while the RHS is convex quadratic. Assume that the curves meet at two points. Naturally, only the point corresponding to the lower source current can be optimal. Now, suppose that the output branch current increases. If (34) holds, then the source current has to increase to support the larger output requirement. Typically, the term \(|I_{s,k} (R_{M,k} - R_{D,k})| \ll 1\), while \(V_{load} \gg 1\), which makes the assumption valid in practice. With all the aforementioned modifications, the main optimization problem given in Figure 2 is obtained.

As the third step it will be shown that, at optimality (if it exists), the convex relaxations are tight. To begin with, consider the constraint in (31) previously mentioned. Suppose on the contrary, for some \(k\), at the optimal point \(P = \{V_{s1}, \ldots, V_{sm}, V_{1'}, \ldots, V_{m'}, I_{1'}, \ldots, I_{m'}\}\),
\[
\min_{j \in [1,P_k]} \{ \beta_{k,j} I_{s,k}^2 + \gamma_{k,j} I_{s,k} \} > Q_k + V_{load} I_k
\] (35)

Then, due to the continuity of the functions on either side of the constraint, there exists a \(\delta > 0\) such that the point \(P_\delta = \{V_{s1}, \ldots, V_{sm}, (V_{1'} + \delta R_{s,k}) \ldots, (V_{m'} + \delta R_{s,k}) \ldots (I_{s,k} - \delta) \ldots I_1 \ldots I_m\}\) is a feasible point. It is feasible because a (i) reduction in \(I_{s,k}\) only increases the range for possible \(V_{s,k}\) (see A1), and (ii) an increase in \(V_{k}\) only requires a reduction in gain of the \(k^{th}\) converter, which cannot go below 1 due to A5. The point \(P_\delta\) also has a lower cost, since a sufficiently small reduction in \(I_{s,k}\) reduces all terms in the cost function - \((I_{s,k} - I_k) \frac{R_{M,k}}{2}\) also reduces since in a lossy boost converter \(I_{s,k} > I_k\). Thus, at optimality, the power constraint is tight. Since in the arguments of \(P_\delta\) the DCC output voltages remain unchanged, the result holds with an additional cost of (23).

Lastly, suppose at optimality, for the \(k^{th}\) converter,
\[
V_{s,k} < f_k (I_{s,k} ).
\] (36)

![Fig. 3: Case (i): An equivalent circuit for case (i). The nonlinear voltage sources is realized using the circuit shown in Fig. 4](image)

![Fig. 4: Case (i): Schematic of nonlinear power source.](image)

III. COMPUTATIONS AND SIMULATIONS

This section presents computations in CVXPY [8] and simulations on LTSpice. Three cases are presented: (case i) sources have non-linear VI-characteristics, (case ii) sources are constant voltage sources with internal resistances and MOSFET/diode characteristics are same across DCCs, and (iii) sources are constant voltage sources with internal resistances and the MOSFET/diode characteristics are different across DCCs. The optimal gains for all the cases are calculated using CVXPY and LTSpice simulations are carried out with those optimal duty ratios. The simulations for case (i) and (iii) consider an equivalent circuit which emulates the optimization model. In the equivalent circuit, the terms with squared of the source currents manifest as resistances on the primary side of the MOSFET. The terms with squared of the output currents manifest on the secondary side. The MOSFET is modeled as an ideal switch with its DSR. To model the switching loss, a voltage controlled voltage source is included; essentially to emulate the product term of the source current and the output current.

The LTSpice simulations for (case ii) comprise two types: (case ii, a) simulation of a circuit with commercially available semiconductor component models, and (case ii, b) simulation...
of an equivalent circuit, as for the other cases. In all cases, the parameters of the circuit are assumed to be constant over the period of simulation and satisfy all the assumptions. Table I presents the parameters pertaining to the power sources for case (i), and Figure 3 & 4 present the circuits used for simulation. Table II presents the circuit parameters and numerical results from CVXPY & LTSpice. The circuits for cases (ii, a) and (ii, b) are presented in Figure 5 and Figure 6, respectively. Table III and VI presents circuit parameters and results for case (ii,a). The results for case (ii, b) are presented in Table IV. The circuit parameters and results from CVXPY for case (iii) are presented in Table V.

The diode’s forward bias and resistance are estimated using the LHS circuit in Figure 7. It is subjected to a slow voltage ramp, up to its rated voltage, instantaneous current & power are recorded and the form $P(I) = V_D I + I^2 R_D$ is fitted using least squares. The multiplicative constant for switching loss is estimated using the RHS circuit in Figure 7. The voltage source is set to $V_{load} + V_{D,k} + I_{k, min} (R_k + R_D,k)$, since this a lower bound on the MOSFET drain voltage in a DCC. The current source is set to $V_{load}/3 R_{load}$, since the current in a branch isn’t known prior to optimization. The circuit is simulated for several cycles with a duty ratio of 0.5. The average MOSFET power loss $P_{loss}$ and its rms-current $I_{rms}$ are recorded. Since the drain-to-source resistance of the MOSFET $R_{M,k}$ is known from its data-sheet, the multiplicative constant is

$$\alpha_k = \frac{P_{loss} - 0.5 \left( \frac{V_{load}}{3 R_{load}} \right)^2 R_{M,k}} {\left( V_{load} + V_{D,k} + \frac{V_{load}}{3 R_{load}} (R_k + R_D,k) \right) \frac{V_{load}}{3 R_{load}}}. \quad (38)$$

As expected, in all cases, the constraints are all tight at optimality. The voltages and currents obtained from LTSpice are in close correspondence with those obtained from CVXPY. However, for case (ii, a) the difference between the two sets of numbers is marginally more as compared to other cases, which can be attributed to modeling error of MOSFET/diode. The difference also shows up in power loss numbers reported in VI.

IV. FUTURE WORK

The problem of load balancing to minimize the total power losses in a DC microgrid with multiple heterogeneous sources supplying a load was considered. Under mild assumptions, it was shown that the non-convex problem has a tight convex relaxation. Computations and simulations were provided for corroboration. Some future directions of work: (i) solving the problem when (20) and (27) are relaxed, (ii) incorporating inductor-core losses, reverse recovery losses & capacitive losses, (iii) stability analysis (although simulations are indicative of it) (iv) decentralized control schemes, (v) extensions with other converter classes, and (vi) hardware realization.

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