High-Performance and Energy-Efficient Memory Scheduler Design for Heterogeneous Systems

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This paper summarizes the idea of the Staged Memory Scheduler (SMS), which was published at ISCA 2012 [14], and examines the work’s significance and future potential. When multiple processor cores (CPUs) and a GPU integrated together on the same chip share the off-chip DRAM, requests from the GPU can heavily interfere with requests from the CPUs, leading to low system performance and starvation of cores. Unfortunately, state-of-the-art memory scheduling algorithms are ineffective at solving this problem due to the very large amount of GPU memory traffic, unless a very large and costly request buffer is employed to provide these algorithms with enough visibility across the global request stream.

Previously-proposed memory controller (MC) designs use a single monolithic structure to perform three main tasks. First, the MC attempts to schedule together requests to the same DRAM row to increase row buffer hit rates. Second, the MC arbitrates among the requesters (CPUs and GPU) to optimize for overall system throughput, average response time, fairness and quality of service. Third, the MC manages the low-level DRAM command scheduling to complete requests while ensuring compliance with all DRAM timing and power constraints.

This paper proposes a fundamentally new approach, called the Staged Memory Scheduler (SMS), which decouples the three primary MC tasks into three significantly simpler structures that together improve system performance and fairness. Our three-stage MC first groups requests based on row buffer locality. This grouping allows the second stage to focus only on inter-application scheduling decisions. These two stages enforce high-level policies regarding performance and fairness, and therefore the last stage can use simple per-bank FIFO queues (i.e., there is no need for further command reordering within each bank) and straightforward logic that deals only with the low-level DRAM commands and timing.

We evaluated the design trade-offs involved and compared it against four state-of-the-art MC designs. Our evaluation shows that SMS provides 41.2% performance improvement and 4.8x fairness improvement compared to the best previous state-of-the-art technique, while enabling a design that is significantly less complex and more power-efficient to implement.

Our analysis and proposed scheduler have inspired significant research on (1) predictable and/or deadline-aware memory scheduling [91, 92, 194, 195, 197, 201, 202, 216] and (2) memory scheduling for heterogeneous systems [161, 201, 202, 207].

1. Introduction

As the number of cores continues to increase in modern chip multiprocessor (CMP) systems, the DRAM memory system has become a critical shared resource [139, 145]. Memory requests from multiple cores interfere with each other, and this inter-application interference is a significant impediment to individual application and overall system performance. Various works on application-aware memory scheduling [98, 99, 141, 142] address the problem by making the memory controller aware of application characteristics and appropriately prioritizing memory requests to improve system performance and fairness.

Recent heterogeneous CPU-GPU systems [1, 27, 28, 37, 76, 77, 78, 133, 152, 153, 167, 209] present an additional challenge by introducing integrated graphics processing units (GPUs) on the same die with CPU cores. GPU applications typically demand significantly more memory bandwidth than CPU applications due to the GPU’s capability of executing a large number of concurrent threads [1, 2, 3, 4, 13, 23, 27, 37, 38, 40, 62, 68, 77, 78, 133, 149, 150, 151, 152, 153, 154, 167, 176, 178, 179, 188, 189, 199, 200, 206, 209]. GPUs use single-instruction multiple-data (SIMD) pipelines to concurrently execute multiple threads [53]. In a GPU, a group of threads executing the same instruction is called a wavefront or warp, and threads in a warp are executed in lockstep. When a wavefront stalls on a memory instruction, the GPU core hides this memory access latency by switching to another wavefront to avoid stalling the pipeline. Therefore, there can be thousands of outstanding memory requests from across all of the wavefronts. This is fundamentally more memory intensive than CPU memory traffic, where each CPU application has a much smaller number of outstanding requests due to the sequential execution model of CPUs.

Figure 1 (a) shows the memory request rates for a representative subset of our GPU applications and the most memory-intensive SPEC2006 (CPU) applications, as measured by memory requests per thousand cycles when each application runs alone on the system. The raw bandwidth demands (i.e., memory request rates) of the GPU applications are often multiple times higher than the SPEC benchmarks. Figure 1 (b) shows the row buffer hit rates (also called row buffer locality or RBL [134]). The GPU applications show consistently high levels of RBL, whereas the SPEC benchmarks exhibit more variability. The GPU programs have high levels of spatial variability.
locality, often due to access patterns related to large sequential memory accesses (e.g., frame buffer updates). Figure 1(c) shows the bank-level parallelism (BLP) [109, 142], which is the average number of parallel memory requests that can be issued to different DRAM banks, for each application, with the GPU programs consistently making use of four banks at the same time.

In addition to the high-intensity memory traffic of GPU applications, there are other properties that distinguish GPU applications from CPU applications. Prior work [99] observed that CPU applications with streaming access patterns typically exhibit high RBL but low BLP, while applications with less uniform access patterns typically have low RBL but high BLP.

In contrast, GPU applications have both high RBL and high BLP. The combination of high memory intensity, high RBL and high BLP means that the GPU will cause significant interference to other applications across all banks, especially when using a memory scheduling algorithm that preferentially favors requests that result in row buffer hits (e.g., [173, 220]).

Recent memory scheduling research has focused on memory interference between applications in CPU-only scenarios. These past proposals are built around a single centralized request buffer at each memory controller (MC). The scheduling algorithm implemented in the memory controller analyzes the stream of requests in the centralized request buffer to determine application memory characteristics, decides on a priority for each core, and then enforces these priorities. Observable memory characteristics may include the number of requests that result in row buffer hits, the bank-level parallelism of each core, memory request rates, overall fairness metrics, and other information. Figure 2(a) shows the CPU-only scenario where the request buffer only holds requests from the CPUs. In this case, the memory controller sees a number of requests from the CPUs and has visibility into their memory behavior. On the other hand, when the request buffer is shared between the CPUs and the GPU, as shown in Figure 2(b), the large volume of requests from the GPU occupies a significant fraction of the memory controller’s request buffer, thereby limiting the memory controller’s visibility of the CPU applications’ memory characteristics.

One approach to increasing the memory controller’s visibility across a larger window of memory requests is to increase the size of its request buffer. This allows the memory controller to observe more requests from the CPUs to better characterize their memory behavior, as shown in Figure 2(c). For instance, with a large request buffer, the memory controller can identify and service multiple requests from one CPU core to the same row such that they become row buffer hits, however, with a small request buffer as shown in Figure 2(b), the memory controller may not even see these requests at the same time because the GPU’s requests have occupied the majority of the entries.

Unfortunately, very large request buffers impose significant implementation challenges, including the die area for the larger structures and the additional circuit complexity for analyzing so many requests, along with the logic needed for assignment and enforcement of priorities [194, 195]. Therefore, while building a very large, centralized memory controller request buffer could perhaps lead to reasonable memory scheduling decisions, the approach is unattractive due to the resulting area, power, timing and complexity costs.

In this work, we propose the Staged Memory Scheduler (SMS), a decentralized architecture for memory scheduling in the context of integrated multi-core CPU-GPU systems. The key idea in SMS is to decouple the various functional tasks of memory controllers and partition these tasks across several simpler hardware structures which operate in a staged fash-
2. Staged Memory Scheduler Design

Overview: Our proposed Staged Memory Scheduler [14] architecture introduces a new memory controller (MC) design that provides 1) scalability and simpler implementation by decoupling the primary functions of an application-aware MC into a simpler multi-stage MC, and 2) performance and fairness improvement by reducing the interference caused by very bandwidth-intensive applications. SMS provides these benefits by introducing a three-stage design. The first stage is the per-core batch formation stage, which groups requests from the same application that access the same row to improve row buffer locality. The second stage is the batch scheduler, which schedules batches of requests from across different applications. The last stage is the DRAM command scheduler, which sends requests to DRAM while satisfying all DRAM constraints.

The staged organization of SMS lends directly to a low-complexity hardware implementation. Figure 3 illustrates the overall hardware organization of the SMS. We briefly discuss each stage below. Section 4 of our ISCA 2012 paper [14] includes a detailed description of each stage.

Stage 1 - Batch Formation. The goal of this stage is to combine individual memory requests from each source into batches of requests that are to the same row buffer entry. It consists of several simple FIFO structures, one per source (i.e., a CPU core or the GPU). Each request from a given source

is initially inserted into its respective FIFO upon arrival at the MC. A batch is simply one or more memory requests from the same source that access the same DRAM row. That is, all requests within a batch, except perhaps for the first one, would be row buffer hits if scheduled consecutively. A batch is deemed complete or ready when an incoming request accesses a different row, when the oldest request in the batch has exceeded a threshold age, or when the FIFO is full. Only ready batches are considered for future scheduling by the second stage of SMS.

Stage 2 - Batch Scheduler. The batch scheduler deals directly with batches, and therefore does not need to worry about optimizing for row buffer locality. Instead, the batch scheduler focuses on higher-level policies regarding inter-application interference and fairness. The goal of this stage is to prioritize batches from applications that are latency critical, while making sure that bandwidth-intensive applications (e.g., those running on the GPU) still make good progress.

The batch scheduler considers every source FIFO (from stage 1) that contains a ready batch. It picks one ready batch based on either a shortest job first (SJF) or a round-robin policy. Using the SJF policy, the batch scheduler chooses the oldest ready batch from the source with the fewest total in-flight memory requests across all three stages of SMS. SJF prioritization reduces average request service latency, and it tends to favor latency-sensitive applications, which tend to have fewer total requests [98, 99, 109, 142]. Using the round-robin policy, the batch scheduler simply picks the next ready batch in a round-robin manner across the source FIFOs. This ensures that memory-intensive applications receive adequate service. The batch scheduler uses the SJF policy with probability $p$ and the round-robin policy with probability $1 - p$. The value of $p$ determines whether the CPU or the GPU

1 We refer the reader to our prior works [32, 33, 34, 35, 36, 66, 67, 93, 96, 97, 98, 99, 100, 112, 113, 114, 115, 116, 120, 121, 158, 183, 184] for a detailed background on DRAM.
receives higher priority. When $p$ is high, the SJF policy is applied more often and applications with fewer outstanding requests are prioritized. Hence, the batches of the likely less memory-intensive CPU applications are prioritized over the batches of the GPU application. On the other hand, when $p$ is low, request batches are scheduled in a round-robin fashion more often. Hence, the memory-intensive GPU application’s naturally-large request batches are likely scheduled more frequently, and the GPU is thus prioritized over the CPU.

After picking a batch, the batch scheduler enters a drain state where it forwards the requests from the selected batch to the final stage of the SMS. The batch scheduler dequeues one request per cycle until all requests from the batch have been removed from the selected FIFO.

**Stage 3 - DRAM Command Scheduler (DCS).** DCS consists of one FIFO queue per DRAM bank. The drain state of the batch scheduler places the memory requests directly into these FIFOs. Note that because batches are moved into DCS FIFOs one batch at a time, row buffer locality within a batch is preserved within a DCS FIFO. At this point, higher-level policy decisions have already been made by the batch scheduler. Therefore, the DCS simply issues low-level DRAM commands, ensuring DRAM protocol compliance.

In any given cycle, DCS considers only the requests at the head of each of the per-bank FIFOs. For each request, DCS determines whether that request can issue a command based on the request’s current row buffer state (e.g., is the row buffer already open with the requested row?) and the current DRAM state (e.g., time elapsed since a row was opened in a bank, and data bus availability). If more than one request is eligible to issue a command in any given cycle, the DCS arbitrates between DRAM banks in a round-robin fashion.

### 3. Qualitative Comparison with Previous Scheduling Algorithms

In this section, we compare SMS qualitatively to previously proposed scheduling policies and analyze the basic differences between SMS and these policies. The fundamental difference between SMS and previously-proposed memory scheduling policies for CPU-only scenarios is that the latter are designed around a single, centralized request buffer which has poor scalability and complex scheduling logic, while SMS is built around a decentralized, scalable framework.

**First-Ready FCFS (FR-FCFS).** FR-FCFS [173, 220] is a commonly used scheduling policy in commodity DRAM systems. An FR-FCFS scheduler prioritizes requests that result in row buffer hits over row buffer misses and otherwise prioritizes older requests. Since FR-FCFS unfairly prioritizes applications with high row buffer locality to maximize DRAM throughput, prior works [42, 45, 98, 99, 134, 137, 141, 142, 194, 195] have observed that it has low system performance and high unfairness.

**Parallelism-Aware Batch Scheduling (PAR-BS).** PAR-BS [142, 143] aims to improve both fairness and system performance. In order to prevent unfairness, it forms batches of outstanding memory requests and prioritizes the oldest batch, to avoid request starvation. To improve system throughput, it prioritizes applications with smaller number of outstanding memory requests within a batch. However, PAR-BS has two major shortcomings. First, batching could cause older GPU requests and requests of other memory-intensive CPU applications to be prioritized over latency-sensitive CPU applications. Second, as previous work [98] has also observed, PAR-BS does not take into account an application’s long term memory-intensity characteristics when it assigns application priorities within a batch. This could cause memory-intensive applications’ requests to be prioritized over latency-sensitive applications’ requests within a batch, due to the application-agnostic nature of batching.

**Adaptive Per-Thread Least-Attained-Serviced Memory Scheduling (ATLAS).** ATLAS [98] aims to improve system performance by prioritizing requests of applications with lower attained memory service. This improves the performance of low memory-intensity applications as they tend to have low attained service. However, ATLAS has the disadvantage of not preserving fairness. Previous works [98, 99] have shown that simply prioritizing applications based on attained service leads to significant slowdown of memory-intensive applications.

**Thread Cluster Memory Scheduling (TCM).** TCM [99] is a state-of-the-art application-aware cluster memory scheduler providing both high system throughput and high fairness. It groups an application into either a latency-sensitive or a bandwidth-sensitive cluster based on the application memory intensity. In order to achieve high system throughput and low unfairness, TCM employs a different prioritization policy for each cluster. To improve system throughput, a fraction of total memory bandwidth is dedicated to the latency-sensitive cluster and applications within the cluster are then ranked based on memory intensity with the least memory-intensive application receiving the highest priority. On the other hand, TCM minimizes unfairness by periodically shuffling applications within the bandwidth-sensitive cluster to avoid starvation. This approach provides both high system performance and fairness in CPU-only systems. In an integrated CPU-GPU system, the GPU generates a significantly larger number of memory requests compared to the CPUs and fills up the centralized request buffer. As a result, the memory controller lacks the visibility into CPU memory requests to accurately determine each application’s memory access characteristics. Without such visibility, TCM makes incorrect and non-robust clustering decisions, which classify some applications with high memory intensity into the latency-sensitive cluster and vice versa. Such misclassified applications cause interference not only to low memory intensity applications, but also to each other. Therefore, TCM cannot always provide high system performance and high fairness in an integrated CPU-GPU system. Increasing the request buffer size is a practical way
to gain more visibility into CPU applications’ memory access characteristics. However, this approach is not scalable as we show in our evaluations [14]. In contrast, SMS provides much better system performance and fairness than TCM with the same number of request buffer entries and lower hardware cost, as we show in Section 5.

4. Evaluation Methodology

We use an in-house cycle-accurate simulator to perform our evaluations. For our performance evaluations, we model a system with sixteen x86 CPU cores and a GPU. For the CPUs, we model three-wide out-of-order processors with a cache hierarchy including per-core L1 caches and a shared, distributed L2 cache. The GPU does not share the CPU caches. In order to prevent the GPU from taking the majority of request buffer entries, we reserve half of the request buffer entries for the CPUs. To model the memory bandwidth of the GPU accurately, we perform coalescing on GPU memory requests before they are sent to the memory controller [119].

We evaluate our system with a set of 105 multiprogrammed workloads simulated for 500 million cycles. Each workload consists of sixteen SPEC CPU2006 benchmarks and one GPU application selected from a mix of video games and graphics performance benchmarks. We classify CPU benchmarks into three categories (Low, Medium, and High) based on their memory intensities, measured as last-level cache misses per thousand instructions (MPKI). Based on these three categories, we randomly choose sixteen CPU benchmarks from these three categories and one randomly selected GPU benchmark to form workloads consisting of seven intensity mixes: L (All low), ML (Low/Medium), M (All medium), HL (High/Low), HML (High/Medium/Low), HM (High/Medium) and H (All high). For each CPU benchmark, we use Pin [125, 172] with PinPoints [159] to select the representative phase. For the GPU applications, we use an industrial GPU simulator to collect memory requests with detailed timing information. These requests are collected after having first been filtered through the GPU’s internal cache hierarchy, therefore we do not further model any caches for the GPU in our final hybrid CPU-GPU simulation framework. More detail on our experimental methodology is in Section 5 of our ISCA 2012 paper [14].

5. Experimental Results

We present the performance of five memory scheduler configurations: FR-FCFS [173, 220], ATLAS [98], PAR-BS [142], TCM [99], and SMS [14] on the 16-CPU/1-GPU four-memory-controller system. All memory schedulers use 300 request buffer entries per memory controller. This size was chosen based on empirical results, which showed that performance does not appreciably increase for larger request buffer sizes.

Results are presented in the workload categories, with workload memory intensities increasing from left to right. Figure 4 shows the system performance (measured as weighted speedup [50, 51]) and fairness (measured as maximum slowdown [43, 98, 99, 194, 195, 203]) of the previously proposed algorithms and SMS. Compared to TCM, which is the previous state-of-the-art algorithm for both system performance and fairness, SMS provides 41.2% system performance improvement and 4.8× fairness improvement. Therefore, we conclude that SMS provides better system performance and fairness than all previously proposed scheduling policies, while incurring much lower hardware cost and simpler scheduling logic, as we show in Section 5.2.

We study the performance of the CPU system and the GPU system separately and provide two major observations in Figure 5. First, SMS gains 1.76× improvement in CPU system performance over TCM. Second, SMS achieves this
1.76 × CPU performance improvement while delivering similar GPU performance improvement. The results show that TCM (and the other algorithms) end up allocating far more bandwidth to the GPU, at significant performance and fairness cost to the CPU applications. SMS appropriately deprioritizes the memory bandwidth intensive GPU application in order to enable higher CPU performance and overall system performance, while preserving fairness. Previously proposed scheduling algorithms, on the other hand, allow the GPU to hog memory bandwidth and therefore significantly degrade system performance and fairness.

We provide a more detailed analysis in Sections 6.1 and 6.2 of our ISCA 2012 paper [14].

5.1. Scalability with Cores and Memory Controllers

Figure 6 compares the performance and fairness of SMS against TCM (averaged over 75 workloads) with the same number of request buffers, as the number of cores is varied. We make the following observations: First, SMS continues to provide better system performance and fairness than TCM. Second, the system performance gains and fairness gains increase significantly as the number of cores and hence, memory pressure is increased. SMS’s performance and fairness benefits are likely to become more significant as core counts in future technology nodes increase.

Figure 7 shows the system performance and fairness of SMS compared against TCM as the number of memory channels is varied. For this, and all subsequent results, we perform our evaluations on 60 workloads from categories that contain high memory-intensity applications (HL, HML, HM and H workload categories). We observe that SMS scales better as the number of memory channels increases. As the performance gain of TCM diminishes when the number of memory channels increases from 4 to 8 channels, SMS continues to provide performance improvement for both CPU and GPU. We provide a detailed scalability analysis in Section 6.3 of our ISCA 2012 paper [14].

5.2. Power and Area

We present the power and area of FR-FCFS and SMS. We find that SMS consumes 66.7% less leakage power than FR-FCFS, which is the simplest of all of the prior memory schedulers that we evaluate. In terms of die area, SMS requires 46.3% less area than FR-FCFS. The majority of the power and area savings of SMS over FR-FCFS come from the decentralized request buffer queues and simpler scheduling logic in SMS. In comparison, FR-FCFS requires centralized request buffer queues, content-addressable memory (CAMs), and complex scheduling logic. Because ATLAS and TCM require more complex ranking and scheduling logic than FR-FCFS, we expect that SMS also provides power and area reductions over ATLAS and TCM.

We provide the following additional results in our ISCA 2012 paper [14]:

- Combined performance of CPU-GPU heterogeneous systems for different SMS configurations with different Shortest Job First (SJF) probability.
- Sensitivity analysis to SMS’s configuration parameters.
- Performance of SMS in CPU-only systems.

6. Related Work

To our knowledge, our ISCA 2012 paper is the first to provide a fundamentally new memory controller design for heterogeneous CPU-GPU systems in order to reduce interference at the shared off-chip main memory. There are several

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3We use 75 randomly selected workloads per core count. We could not use the same workloads/categorizations as specified in Section 4 because those were for 16-core systems, whereas we are now varying the number of cores.
prior works that reduce interference at the shared off-chip main memory in other systems. We provide a brief discussion of these works.

6.1. Memory Partitioning Techniques

Instead of mitigating the interference problem between applications by scheduling requests at the memory controller, Awasthi et al. [18] propose a mechanism that spreads data in the same working set across memory channels in order to increase memory level parallelism. Memory channel partitioning (MCP) [137] maps applications to different memory channels based on their memory intensities and row buffer locality, to reduce inter-application interference. Mao et al. [128] propose to partition GPU channels and allow only a subset of threads to access each memory channel. In addition to channel partitioning, several works [74, 122, 210] also propose to partition DRAM banks to improve performance. These partitioning techniques are orthogonal to our proposals, and can be combined with SMS to improve the performance of heterogeneous CPU-GPU systems.

6.2. Memory Scheduling Techniques

Memory Scheduling on CPUs. Numerous prior works propose memory scheduling algorithms for CPUs that improve system performance. The first-ready, first-come-first-serve (FR-FCFS) scheduler [173, 220] prioritizes requests that hit in the row buffer over requests that miss in the row buffer, with the aim of reducing the number of times rows must be activated (as row activation incurs a high latency). Several memory schedulers improve performance beyond FR-FCFS by identifying critical threads in multithreaded applications [47], using reinforcement learning to identify long-term memory behavior [79, 136], prioritizing memory requests based on the criticality (i.e., latency sensitivity) of each memory request [57, 123, 211], distinguishing prefetch requests from demand requests [109, 111], or improving the scheduling of memory writeback requests [110, 182, 193]. While all of these schedulers increase DRAM performance and/or throughput, many of them introduce fairness problems by under-serving applications that only infrequently issue memory requests. To remedy fairness problems, several application-aware memory scheduling algorithms [98, 99, 135, 141, 142, 194, 195, 197] use information on the memory intensity of each application to balance both performance and fairness. Unlike SMS, none of these schedulers consider the different needs of CPU memory requests and GPU memory requests in a heterogeneous system.

Memory Scheduling on GPUs. Since GPU applications are bandwidth intensive, often with streaming access patterns, a policy that maximizes the number of row buffer hits is effective for GPUs to maximize overall throughput. As a result, FR-FCFS with a large request buffer tends to perform well for GPUs [22]. In view of this, prior work [213] proposes mechanisms to reduce the complexity of FR-FCFS scheduling for GPUs. Ausavarungnirun et al. [15] propose MeDiC, which is a cache and memory management scheme to improve the performance of GPGPU applications. Jeong et al. [80] propose a QoS-aware memory scheduler that guarantees the performance of GPU applications by prioritizing memory requests from graphics applications over those from CPU applications until the system can guarantee that a frame can be rendered within a given deadline, after which it prioritizes requests from CPU applications. Jog et al. [83] propose CLAM, a memory scheduler that identifies critical memory requests and prioritizes them in the main memory. Ausavarungnirun et al. [17] propose a scheduling algorithm that identifies and prioritizes TLB-related memory requests in GPU-based systems, to reduce the overhead of memory virtualization. Unlike SMS, none of these works holistically optimize the performance and fairness of requests when a memory controller is shared by a CPU and a GPU.

Memory Scheduling on Emerging Systems. Recent proposals investigate memory scheduling on emerging platforms. Usui et al. [201, 202] propose accelerator-aware memory controller designs that improve the performance of systems that contain both CPUs and hardware accelerators. Zhao et al. [216] decouple the design of a memory controller for persistent memory into multiple stages. These works build upon principles for heterogeneous system memory scheduling that were first proposed in SMS.

6.3. Other Related Works

DRAM Designs. Aside from memory scheduling and memory partitioning techniques, previous works propose new DRAM designs that are capable of reducing memory latency in conventional DRAM [9, 10, 31, 32, 33, 34, 36, 63, 69, 72, 90, 100, 112, 113, 114, 115, 116, 126, 132, 155, 166, 177, 187, 190, 208, 218] and non-volatile memory [102, 105, 106, 107, 130, 131, 170, 171, 212]. Previous works on bulk data transfer [30, 34, 59, 60, 75, 81, 86, 124, 180, 183, 215, 217] and in-memory computation [7, 8, 11, 19, 25, 26, 44, 52, 54, 55, 56, 58, 61, 70, 71, 87, 94, 101, 127, 157, 160, 161, 168, 181, 184, 185, 192, 198, 214] can be used to improve DRAM bandwidth. Techniques to reduce the overhead of DRAM refresh [5, 6, 20, 24, 95, 118, 121, 146, 156, 169, 204] can be applied to improve the performance of GPU-based systems. Data compression techniques [162, 163, 164, 165, 205] can also be used on the main memory to increase the effective available DRAM bandwidth. All of these techniques can mitigate the performance impact of memory interference and improve the performance of GPU-based systems. They are orthogonal to, and can be combined with, SMS to further improve the performance of heterogeneous CPU-GPU systems.

Previous works on data prefetching [12, 21, 29, 39, 41, 46, 48, 49, 64, 65, 73, 84, 85, 104, 108, 109, 111, 138, 140, 144, 148, 186, 191] can also be used to mitigate high DRAM latency. However, these techniques generally increase DRAM bandwidth utilization, which can lead to lower GPU performance.
Other Ways to Improve Performance on Systems with GPUs. Other works have proposed various methods of decreasing memory divergence. These methods range from thread throttling [88, 89, 103, 174] to warp scheduling [117, 129, 147, 174, 175, 219]. While these methods share our goal of reducing memory divergence, none of them exploit inter-warp heterogeneity and, as a result, are orthogonal or complementary to our proposal. Our work also makes new observations about memory divergence that are not covered by these works.

7. Significance and Long-Term Impact

SMS exposes the need to redesign components of the memory subsystem to better serve integrated CPU-GPU systems. Systems-on-chip (SoCs) that integrate CPUs and GPUs on the same die are growing rapidly in popularity (e.g., [37, 133, 152, 153]), due to their high energy efficiency and lower costs compared to discrete CPUs and GPUs. As a result, SoCs are commonly used in mobile devices such as smartphones, tablets, and laptops, and are being used in many servers and data centers. We expect that as more powerful CPUs and GPUs are integrated in SoCs, and as the workloads running on the CPUs/GPUs become more memory-intensive, SMS will become even more essential to alleviate the shared memory subsystem bottleneck.

The observations and mechanisms in our ISCA 2012 paper [14] expose several future research problems. We briefly discuss two future research areas below.

Interference Management in Emerging Heterogeneous Systems. Our ISCA 2012 paper [14] considers heterogeneous systems where a CPU executes various general-purpose applications while the GPU executes graphics workloads. Modern heterogeneous systems contain an increasingly diverse set of workloads. For example, programmers can use the GPU in an integrated CPU-GPU system to execute general-purpose applications (known as GPGPU applications). GPGPU applications can have significantly different access patterns from graphics applications, requiring different memory scheduling policies (e.g., [15, 17, 83]). Future work can adapt the mechanisms of SMS to optimize the performance of GPGPU applications.

Many heterogeneous systems are being deployed in mobile or embedded environments, and must ensure that memory requests from some or all of the components of the heterogeneous system meet real-time deadlines [91, 92, 201, 202]. Traditionally, applications with real-time deadlines are executed using embedded cores or fixed-function accelerators, which are often integrated into modern SoCs. We believe that the observations and mechanisms in our ISCA 2012 paper [14] can be used and extended to ensure that these deadlines are met. Recent works [201, 202] have shown that the principles of SMS can be extended to provide deadline-aware memory scheduling for accelerators within heterogeneous systems.

Even though the mechanisms proposed in our ISCA 2012 paper [14] aim to minimize the slowdown caused by interference, they do not provide actual performance guarantees. However, we believe it is possible to combine principles from SMS with prediction mechanisms for memory access latency (e.g., [91,92,196,197]) to provide hard performance guarantees for real-time applications, while still ensuring fairness for all applications executing on the heterogeneous system.

Memory Scheduling for Concurrent GPGPU Applications. While SMS allows CPU applications and graphics applications to share DRAM more efficiently, we assume that there is only a single GPU application running at any given point in time. Recent works [16, 82] propose methods to efficiently share the same GPU across multiple concurrently-executing GPGPU applications. We believe that the techniques and observations provided in our ISCA 2012 paper [14] can be applied to reduce the memory interference induced by additional GPGPU applications. Furthermore, as concurrent GPGPU application execution becomes more widespread, the concepts of SMS can be extended to provide prioritization and fairness across multiple GPGPU applications.

Our analysis of memory interference in heterogeneous systems, and our new Staged Memory Scheduler, have inspired a number of subsequent works. These works include significant research on predictable and/or deadline-aware memory scheduling [91, 92, 194, 195, 197, 201, 202, 216], and on other memory scheduling algorithms for heterogeneous systems [161, 201, 202, 207].

8. Conclusion

While many advancements in memory scheduling policies have been made to deal with multi-core processors, the integration of GPUs on the same chip as the CPUs has created new system design challenges. Our ISCA 2012 paper [14] demonstrates how the inclusion of GPU memory traffic can cause severe difficulties for existing memory controller designs in terms of performance and especially fairness. We propose a new approach, Staged Memory Scheduler, which delivers superior performance and fairness for integrated CPU-GPU systems compared to state-of-the-art memory schedulers, while providing a design that is significantly simpler to implement (thus improving the scalability of the memory controller). The key insight behind simplifying the implementation of SMS is that the primary functions of sophisticated memory controller algorithms can be decoupled. As a result, SMS proposes a multi-stage memory controller architecture. We show that SMS significantly improves the performance and fairness in integrated CPU-GPU systems. We hope and expect that our observations and mechanisms can inspire future work in memory system design for existing and emerging heterogeneous systems.
Acknowledgments

We thank Saugata Ghose for his dedicated effort in the preparation of this article. We thank Stephen Somogyi and Fritz Kruger at AMD for their assistance with the modeling of the GPU applications. We also thank Antonio Gonzalez, anonymous reviewers and members of the SAFARI group at CMU for their feedback. We acknowledge the generous support of AMD, Intel, Oracle, and Samsung. This research was also partially supported by grants from the NSF (CAREER Award CCF-0953246 and CCF-1147397), GSRC, and Intel ARO Memory Hierarchy Program.

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