Logic Shrinkage: Learned FPGA Netlist Sparsity for Efficient Neural Network Inference

Erwei Wang  
Imperial College London  
London, United Kingdom  
erwei.wang13@imperial.ac.uk

James J. Davis  
Imperial College London  
London, United Kingdom  
james.davis@imperial.ac.uk

Georgios-Ilias Stavrou  
Imperial College London  
London, United Kingdom  
georgios-ilias.stavrou18@imperial.ac.uk

Peter Y. K. Cheung  
Imperial College London  
London, United Kingdom  
p.cheung@imperial.ac.uk

George A. Constantinides  
Imperial College London  
London, United Kingdom  
g.constantinides@imperial.ac.uk

Mohamed S. Abdelfattah  
Cornell University  
New York, NY, United States  
mohamed@cornell.edu

ABSTRACT

FPGA-specific DNN architectures using the native LUTs as independently trainable inference operators have been shown to achieve favorable area-accuracy and energy-accuracy tradeoffs. The first work in this area, LUTNet, exhibited state-of-the-art performance for standard DNN benchmarks. In this paper, we propose the learned optimization of such LUT-based topologies, resulting in higher-efficiency designs than via the direct use of off-the-shelf, hand-designed networks. Existing implementations of this class of architecture require the manual specification of the number of inputs per LUT, \( K \). Choosing appropriate \( K \) a priori is challenging, and doing so at even high granularity, e.g. per layer, is a time-consuming and error-prone process that leaves FPGAs’ spatial flexibility underexploited. Furthermore, prior works see LUT inputs connected randomly, which does not guarantee a good choice of network topology. To address these issues, we propose logic shrinkage, a fine-grained netlist pruning methodology enabling \( K \) to be automatically learned for every LUT in a neural network targeted for FPGA inference. By removing LUT inputs determined to be of low importance, our method increases the efficiency of the resultant accelerators. Our GPU-friendly solution to LUT input removal is capable of processing large topologies during their training with negligible slowdown. With logic shrinkage, we better the area and energy efficiency of the best-performing LUTNet implementation of the CNV network classifying CIFAR-10 by 1.54× and 1.31×, respectively, while matching its accuracy. This implementation also reaches 2.71× the area efficiency of an equally accurate, heavily pruned BNN. On ImageNet with the Bi-Real Net architecture, employment of logic shrinkage results in a post-synthesis area reduction of 2.67× vs LUTNet, allowing for implementation that was previously impossible on today’s largest FPGAs.

KEYWORDS

LUT-based neural networks, binary neural networks, pruning.

1 INTRODUCTION

Deep neural network (DNN) inference is particularly well suited to custom hardware acceleration due to the application’s inherent parallelism. In order to exploit this in the quest for ever-greater performance within given area and power budgets, researchers and industrial practitioners alike are increasingly turning to low-precision data types \([1, 17, 22]\). Binary neural networks (BNNs), in which weights and activations assume one of just two values, see this concept taken to the extreme. Figure 1a shows a generic BNN implementation of the quantized linear dot product operation central to DNN inference, wherein XNOR gates perform multiplication. Here, output \( y = \phi(\mathbf{x}^\top \mathbf{w}) \), with inputs \( \mathbf{x} \in \{-1, 1\}^N \), weights \( \mathbf{w} \in \{-1, 1\}^N \) and activation function \( \phi : \mathbb{N} \rightarrow \{-1, 1\} \). Such structures are compact and eminently parallelizable. When deployed on field-programmable gate arrays (FPGAs), however, their simplicity tends to lead to underuse of the rich compute and routing resources that the target device provides.

We previously posited that more complex networks—netlists of small lookup tables (LUTs)—would ideally suit FPGA implementation due to their architectural similarity to the target fabric \([20]\). In that work, LUTNet, a BNN is first sparsified before its remaining XNORs are replaced with trainable \( K : 1 \) Boolean operators: a process we termed logic expansion. Each of these, directly implementable as a \( K \)-LUT, has \( K \times \) more inputs than its XNOR predecessor, enabling recovery of the accuracy lost due to pruning. Formally, LUT \( n \) takes \( x^{(n)} \sim x, i \in \{1, \cdots, K\} \) as input. The weights are hardened within the LUT masks and so no longer appear externally. The result of this transformation is a fast and efficient task-specific inference accelerator. This is exemplified in Figure 1b, in which \( N \) \( K \)-LUTs (here, 3-LUTs) have been substituted for \( N \) XNOR gates. Since \( N \ll N \), compaction of the adder tree more than compensates for the marginal area penalty attributable to the \( K \)-LUTs. With LUTNet, we reported area efficiency improvements of around 2× over ReBNet \([3]\), the state-of-the-art BNN at the time, for problems.
of widely varying scale. More recent tools, including NullaNet [12] and LogicNets [18], also generate small LUTs as core components, but LUTNet remains unique in directly exposing a netlist’s LUTs as differentiable functions trainable via stochastic gradient descent.

In such a LUT-based network, fixed $K$ will inevitably be sub-optimal. For example, while it may be the case that 6-LUTs map particularly well to a given device, $K = 6$ may be too many (or too few) inputs for a given node to suit the training data. We therefore propose that the size of each LUT be learned during training. Starting from a netlist of $K$-LUTs, we achieve this by removing input connections determined to be unimportant, resulting in a new netlist in which $K'_n \leq K$ for all $n$. Where $K'_n = 0$, LUT $n$ can be removed entirely. This results in $N \leq \tilde{N}$.

We take inspiration from the field of neural architecture search (NAS), in which a sparse and efficient topology is typically found by cutting away parts of a dense network [15]. While our end goal is similar, the netlist-level NAS we propose presents unique challenges. In particular, unlike standard topologies with a single weight per node, each node in a network of $K$-LUTs has $K$ inputs sharing $2^K$ trainable parameters. Severance of one LUT input requires the manipulation of all $2^K$ entries within the respective truth table. Given that modern DNNs contain hundreds of thousands or even millions of nodes, naïve operation on all of these would quickly become intractable. We thus present a vectorized implementation of our input pruning proposal ideally suited to GPU acceleration.

In this paper, we present logic shrinkage: the automated search for, and construction of, DNN inference topologies featuring learned netlist sparsity. We make the following novel contributions.

- We propose a method for the evaluation of input connection salience within a netlist of LUTs used for DNN inference.
- We cast LUT input removal as a matrix-vector operation, enabling us to take advantage of GPUs for its realization.
- We present a TensorFlow-based implementation of logic shrinkage, in which DNNs composed of LUTs of fixed size are automatically transformed into sparser, heterogeneous networks more efficiently mappable onto FPGAs.
- We empirically explore the effects of logic shrinkage on area efficiency and accuracy via comparison with LUTNet [20], our state-of-the-art FPGA-specific DNN inference topology, across a broad range of standard network models and datasets. We also experimentally determine logic shrinkage’s impact on energy and training efficiency. Against LUTNet with fixed $K = 4$, ordinarily the best-performing choice of constant $K$, we achieve area compression of 1.54× and an energy saving of 1.31× for the CNV network [19] classifying the CIFAR-10 dataset [5] while reaching comparable accuracy. Finally, we report positive results at scale, with our logic-shrunk Bi-Real Net [9] design classifying ImageNet [2] demanding 2.67× lower post-synthesis area than LUTNet.
- We provide an open-source release¹ of our work for the community to use and build upon.

2 RELATED WORK

2.1 FPGA-Tailed DNN Architectures

LUT-based DNN inference accelerators have been shown to achieve remarkable performance when deployed on FPGAs. NullaNet [12] and LogicNets [18] were conceived with small-scale classification tasks in mind, for which they reached latency in the tens of nanoseconds and throughput in the hundreds of millions of samples per second. Going beyond FPGA-tailed network design, our previously proposed LUTNet topologies can be trained via stochastic gradient descent [20]. LUTNet’s trainable netlists are compatible with common machine learning optimization strategies such as pruning.

¹https://github.com/awai54st/Logic-Shrinkage
thereby affording opportunities for increased performance and efficiency. Furthermore, the LUTNet approach suits tasks spanning a broad range of scales, including ImageNet classification.

LUTNet netlists tend to be large due to the one-to-one mapping between DNN nodes and LUTs. Consequently, in typical deployments, only a subset of network layers are logic-expanded: the remainder are kept as standard BNN structures. We have also proposed a time-multiplexed version of the LUTNet architecture, which negates the need for each LUT to be specific to a single node by reintroducing runtime-variable weights [21]. This increases LUTNet’s scalability, but also reduces its potential area and energy efficiency gains over BNNs due to the lost freedom in LUT specialization.

We use LUTNet netlists as a starting point for logic shrinkage, and demonstrate that the resultant designs are more area and energy efficient. Our automated design flow maintains the deployment flexibility, scalability and ease of use of LUTNet’s. To evaluate the potential of logic shrinkage in the most generic setting, we assume the use of hardened weights, in line with vanilla LUTNet. Our approach could be applied to time-multiplexed architectures, however we would similarly expect lower gains from doing so.

2.2 Activation Pruning

Activations within a DNN commonly contribute to its output to varying degrees. Activation pruning exploits this by assigning coarser-grained search, decomposing convolutions into combinations of ‘atomic blocks’ and greatly increasing the number of possible output architectures vs DARTS [10]. This richness in flexibility resulted in the production of state-of-the-art ImageNet classifiers.

We propose a network topology search approach analogous to prior works on NAS. We start with an overprovisioned K-LUT-based architecture—a supernet—and selectively remove its redundancy at ultra-fine granularity via LUT input pruning.

3 BACKGROUND: LOGIC EXPANSION

To enable post-logic expansion retraining for LUTNet, we defined an interpolating extension to the complete set of K : 1 Boolean operations as our training function [20]:

\[ f(\tilde{x}^{(n)}) = \sum_{d \in \{-1,1\}^K} (\hat{c}_d \prod_{k=1}^K (1 - d_k x_k^{(n)})) \quad \text{if } K = 1 \]

\[ f(\tilde{x}^{(n)}) = \hat{c}_{(-1,-1)} (1 + \tilde{x}_1^{(n)}) (1 + \tilde{x}_2^{(n)}) \]  
\[ + \hat{c}_{(-1,1)} (1 + \tilde{x}_1^{(n)}) (1 - \tilde{x}_2^{(n)}) \]  
\[ + \hat{c}_{(1,-1)} (1 - \tilde{x}_1^{(n)}) (1 + \tilde{x}_2^{(n)}) \]  
\[ + \hat{c}_{(1,1)} (1 - \tilde{x}_1^{(n)}) (1 - \tilde{x}_2^{(n)}) \]  
\[ \ldots \]  
for \( K \in \mathbb{N}_{>0} \), with each polynomial comprised of \( 2^K \) trainable parameters. We use a logic-expanded, retrained network as the starting point for logic shrinkage.

4 MECHANICS OF LOGIC SHRINKAGE

4.1 LUT Input Salience

The activation gradient-based salience criteria commonly used with standard neural networks are not directly applicable to netlist pruning due to the interdependence of LUT inputs. However, their fundamental concept—gauging an activation’s importance by the impact on the network’s outputs with respect to a change in that activation—remains relevant, thus we adopt it for the purpose of establishing LUT input salience.

Consider a K-binary-input LUT with truth table entries encoded as \( \{0,1\} \mapsto \{-1,1\} \). Each entry represents the output with respect to a unique combination of inputs; changing one or more input values will alter the selection of LUT entries used as output. We define a particular LUT input’s salience to be the sum of such changes across all combinations of the remaining inputs. If the flipping of a given input never leads to a change in LUT output, that input can clearly be removed without having any impact on the functionality of the network. Such an input therefore has zero salience. If toggling an input sometimes—but rarely—results in output change, we consider that input to be of low salience, while the opposite holds for an input whose toggling often causes the LUT’s output to change.

LUTNet-style Lagrangian interpolation, which we introduced to make LUTs differentiable [20], presents us with an opportunity to more precisely quantify LUT input salience. Since LUT entries
in this scenario are real-valued, output changes are typically less coarse than when operating in the binary domain.

To exemplify our approach, Table 1 contains possible real-valued LUT entries \( \hat{c} \) of a 2-LUT, where \( x_1 \) and \( x_2 \) are its inputs. The LUT's entries will be binarized prior to synthesis; once this is done, this LUT will function as an AND gate.

In Table 1, the salience of input \( x_1, s_1 \), is defined as the total disturbance to the LUT output across both \( x_2 = 1 \) and \( x_2 = -1 \) when \( x_1 \) experiences a change in sign, i.e. the sum of column \( |\Delta x_1| \).

Similarly, the salience of \( x_2, s_2 \), is defined as the sum of row \( |\Delta x_2| \).

In general, we define the salience of K-LUT input \( i \) as

\[
s_i = \sum_{d_1 \in \{-1,1\}^{i-1}} \sum_{d_2 \in \{-1,1\}^{K-i}} \left| \hat{c}(d_1,1,d_2) - \hat{c}(d_1,-1,d_2) \right|
\]

From Table 1, since \( s_1 > s_2 \), we can conclude that toggles of input \( x_1 \) lead to greater impact on the LUT output than toggles of \( x_2 \). This is therefore less important than \( x_1 \) and so should be prioritized for disconnection. Once the less-salient inputs of a network's LUTs have been identified, we can turn to their removal.

We experimented with other candidate salience criteria—-including weight gradient- [7] and Taylor expansion-based [11] methods— before settling on the aforedescribed approach. While these were shown to work well for conventional DNN node pruning, we did not observe positive results in their use for LUT input removal.

4.2 Pruning

In a similar vein to the establishment of salience, LUT input pruning also requires a nonstandard approach. With a conventional neural network node, an activation can be removed by setting its corresponding weight to zero. The removal of an input from a K-LUT, on the other hand, requires the manipulation of all of the \( 2^K \) \( \hat{c} \) parameters that define the contents of the LUT.

Here we demonstrate the process of removing LUT inputs using the 2-LUT in (2) as an example. In order to remove input \( \hat{x}_1 \), the LUT mask \( \hat{c} \) should be transformed into \( \hat{c}' \) such that \( \hat{c}'_{(-1,-1)} = \hat{c}'_{(1,1)} \) and \( \hat{c}'_{(-1,1)} = \hat{c}'_{(1,-1)} \). Countless functions can be used to achieve this. Of them, we chose the computationally cheapest: assignment using the means of their pre-shrinkage values. The removal of input \( \hat{x}_1 \) is thus achieved by performing

\[
\begin{align*}
\hat{c}'_{(-1,-1)} &= \frac{1}{2} \left( \hat{c}_{(-1,-1)} + \hat{c}_{(1,1)} \right) \\
\hat{c}'_{(-1,1)} &= \frac{1}{2} \left( \hat{c}_{(-1,1)} + \hat{c}_{(1,-1)} \right) \\
\hat{c}'_{(1,-1)} &= \frac{1}{2} \left( \hat{c}_{(1,-1)} + \hat{c}_{(-1,1)} \right) \\
\hat{c}'_{(1,1)} &= \frac{1}{2} \left( \hat{c}_{(1,1)} + \hat{c}_{(-1,-1)} \right)
\end{align*}
\]

Similarly, the removal of LUT input \( \hat{x}_2 \) is achieved as

\[
\begin{align*}
\hat{c}'_{(-1,-1)} &= \frac{1}{2} \left( \hat{c}_{(-1,-1)} + \hat{c}_{(1,1)} \right) \\
\hat{c}'_{(-1,1)} &= \frac{1}{2} \left( \hat{c}_{(-1,1)} + \hat{c}_{(1,-1)} \right) \\
\hat{c}'_{(1,-1)} &= \frac{1}{2} \left( \hat{c}_{(1,-1)} + \hat{c}_{(-1,1)} \right) \\
\hat{c}'_{(1,1)} &= \frac{1}{2} \left( \hat{c}_{(1,1)} + \hat{c}_{(-1,-1)} \right)
\end{align*}
\]

Referring back to the 2-LUT example in Table 1, removal of less-salient input \( x_2 \) requires the application of (5) to the LUT mask, \( \hat{c} \). This results in new parameters \( \hat{c}'_{(-1,-1)} = \hat{c}'_{(1,1)} = -0.88 \) and \( \hat{c}'_{(-1,1)} = \hat{c}'_{(1,-1)} = 0.02 \). Once \( \hat{c}' \) is binarized, the 2-LUT performs the single-input function \( y = x_1 \), i.e. it is transformed into a wire.

4.3 Pruning at Scale

While pruning when \( K = 2 \), as exemplified in (4) and (5), is straightforward, the complexity of these operations increases exponentially with \( K \). Logic shrinkage of one K-LUT involves the transformation of \( 2^K \) parameters, and the assignments are unique for each of the \( \sum_{K=1}^{K=2} 2^K = 1 \) possible LUT input combinations. This complexity further scales with the number of LUTs being trained. To ensure scalability, the implementation of our pruning method must therefore take advantage of the high-performance linear algebraic capabilities of modern GPUs and DNN training frameworks.

We implement functions such as (4) and (5) as matrix-vector multiplications \( \hat{c}' = U \hat{c} \) with a transformation matrix \( U \in \mathbb{R}^{2^K \times 2^K} \). Continuing with those examples, the removal of input \( \hat{x}_1 \) (in (4) and of input \( \hat{x}_2 \) (in (5) are performed as

\[
\begin{pmatrix}
\hat{c}'_{(-1,-1)} \\
\hat{c}'_{(-1,1)} \\
\hat{c}'_{(1,-1)} \\
\hat{c}'_{(1,1)}
\end{pmatrix}
= \begin{pmatrix}
1 & 1 & 0 & 0 \\
1 & 1 & 0 & 0 \\
0 & 0 & 1 & 1 \\
0 & 0 & 1 & 1
\end{pmatrix}
\begin{pmatrix}
\hat{c}_{(-1,-1)} \\
\hat{c}_{(-1,1)} \\
\hat{c}_{(1,-1)} \\
\hat{c}_{(1,1)}
\end{pmatrix},
\]

i.e. \( U_1 = \frac{1}{2} I^{2 \times 2} \otimes I^{2 \times 2} \)

and

\[
\begin{pmatrix}
\hat{c}'_{(-1,-1)} \\
\hat{c}'_{(-1,1)} \\
\hat{c}'_{(1,-1)} \\
\hat{c}'_{(1,1)}
\end{pmatrix}
= \begin{pmatrix}
1 & 0 & 1 & 0 \\
1 & 0 & 1 & 0 \\
0 & 1 & 0 & 1 \\
0 & 1 & 0 & 1
\end{pmatrix}
\begin{pmatrix}
\hat{c}_{(-1,-1)} \\
\hat{c}_{(-1,1)} \\
\hat{c}_{(1,-1)} \\
\hat{c}_{(1,1)}
\end{pmatrix},
\]

i.e. \( U_2 = \frac{1}{2} I^{2 \times 2} \otimes I^{2 \times 2} \)

respectively, where \( \otimes \) is the Kronecker product and use of \( U_i \) causes the removal of LUT input \( i \).

The removal of a single input can be conceptualized as the merging of LUT parameter pairs followed by the forking of their means back to their original locations. This is achieved by \( I^{2 \times 2} \) in the aforementioned examples. The Kronecker product with the identity matrix permutes the merges and forks as required. In general,

\[
U_i = \frac{1}{2} I^{2^{K-1} \times 2^{K-1}} \otimes I^{2^{K-2} \times 2^{K-2}} \otimes \ldots \otimes I^{2 \times 2} \otimes I^{2^{K-K-1}}.
\]

Where removal of multiple LUT inputs is desired, \( U_i \) for each input \( i \) can simply be multiplied together to form a single transformation matrix, \( U \), before application.

The construction of \( U \), although computationally expensive, is a one-time process that we have found to never exceed 10 s. During
Algorithm 1: Logic shrinkage retraining process.

Inputs:

K ∈ \mathbb{N}, \quad \triangleright \text{# pre-shrinkage inputs per LUT}
N \in \mathbb{N}, \quad \triangleright \text{# pre-shrinkage LUTs}
δ ∈ [0, 1], \quad \triangleright \text{Target sparsity}
T ∈ \mathbb{N}, \quad \triangleright \text{# shrinkage iterations}
P ∈ \mathbb{N}, \quad \triangleright \text{# epochs per shrinkage iteration}
\hat{C} \in \mathbb{R}^{2^K \times \hat{N}} \quad \triangleright \text{Pre-shrinkage LUT masks}

Output:

\hat{C}' \in \mathbb{R}^{2^K \times \hat{N}} \quad \triangleright \text{Post-shrinkage LUT masks}

1: procedure LOGICSHRINK
2: \hat{C}' \leftarrow \hat{C}
3: for t \in \{1, \ldots, T\} do
4: S \leftarrow \text{getSaliency}(\hat{C}') \quad \triangleright \text{Per (3); } S \in \mathbb{R}^{\hat{N} \times K}
5: r \leftarrow \text{getRankOrder}(\text{vec}(S))
6: \delta_t \leftarrow \delta \times i/T
7: M \leftarrow \text{vec}_r(\hat{N} \times K, 1 \leq r \leq \delta_t \hat{N}K) \quad \triangleright M \in \{0, 1\}^{\hat{N} \times K}
8: V \leftarrow 0^{\hat{N} \times 2^K \times 2^K}
9: for n \in \{1, \ldots, \hat{N}\} do
10: V_n \leftarrow I_{2^K \times 2^K}
11: for i \in \{1, \ldots, K\} do
12: if \text{mask}_i = 1 \text{ then}
13: V_n \leftarrow V_n U_i \quad \triangleright \text{Per (6); } V_n \in \mathbb{R}^{2^K \times 2^K}
14: \hat{C}' \leftarrow \text{retrain}(\hat{C}', V, \text{epochs} = P)
15: return \hat{C}'

retraining, logic shrinkage is implemented as one instance of matrix-vector multiplication, which is ideally suited to GPU acceleration.

Although a post-shrinkage LUT mask \( \hat{c}' \) will always represent a simpler function, dependent on fewer inputs, than its predecessor \( \hat{c} \), \( \hat{c}' \) will retain \( 2^K \) parameters. While this means that a post-shrinkage netlist will contain redundancy, a benefit of this is that such a netlist will remain compatible with the existing LUTNet implementation flow. Our experiments revealed that Vivado effectively recognizes and removes this redundancy during synthesis with no noticeable overhead. Representation of sparse input connections in a dense format, as we propose, also simplifies our training software.

4.4 Iterative Pruning

The authors of many network pruning works, including Han et al. [4] and See et al. [16], proposed pruning across multiple iterations, with each including a post-pruning retraining phase. In keeping with this approach, we separate our LUT input pruning process into multiple iterations, each greedier than the last, with retraining following each. In early experiments, we confirmed that this approach outperforms one-shot pruning, and found that \( T = 3 \) iterations with \( P = 20 \) retraining epochs following each performed favorably. As exemplified in Figure 3, this setup results in training stability being reached quickly in each iteration.

Algorithm 1 details the iterative logic shrinkage training process. In each of the \( T \) total iterations, salience scores of all LUT inputs in the subset of the network subject to logic shrinkage are evaluated using (3) and then ranked. The input sparsity for iteration \( t, \delta_t \), increases with \( t \) until the target sparsity \( \delta \) has been reached. Binary mask \( M \) indicates the low-salience LUT inputs to be pruned. Finally, logic shrinkage transformation matrices \( U \) are constructed based on \( M \), and the network is retrained with input connections sparsified for \( P \) epochs. When retraining, we consistently apply all \( U \)s formed in order to ensure that inputs previously severed by logic shrinkage remain so from then on. The topology of the portion of the network not subject to logic shrinkage is preserved throughout this process, but its parameters remain trainable.

5 EVALUATION

5.1 Implementation

For ease of development and evaluation, we engineered logic shrinkage as a bolt-on addition to the existing LUTNet training and hardware implementation flow [20]. A high-level view of the augmented flow, with the logic shrinkage stage annotated in red, can be found in Figure 2. Now, in addition to the network model, training dataset, input precision and node pruning level that LUTNet takes as input, the user provides their desired LUT input pruning level as well. The back-end FPGA implementation steps remain unchanged.

In common with LUTNet, employment of logic shrinkage necessitates no FPGA knowledge. Parameterized Keras layers and C++ templates are provided for training and implementation, respectively, enabling low-effort construction of dataflow DNN engines.

5.2 Benchmarks

We evaluated our approach using the DNN model and dataset combinations detailed in Table 2. Hardware implementations for all datasets other than ImageNet targeted the Xilinx Kintex UltraScale XCKU115. For ImageNet, we targeted the largest FPGA available to us: the Virtex UltraScale+ XCVU9P. All implementations met timing at 200 MHz. Our primary comparison point was LUTNet, trained as we described in its original publication [20]. Where possible, we also maintained the BNN baseline, ReBNet [3], used as the starting point for LUTNet’s logic expansion, and considered its test accuracy to be a performance floor.

For fairness of comparison to vanilla LUTNet (and ReBNet), we used identical experimental settings to those employed for its evaluation with MNIST, SVHN and CIFAR-10 [20]. Implementations for these datasets included all layers: those selected for logic expansion (and subsequent shrinkage) were unrolled, with the remainder left identical to the BNN starting point. For ImageNet, our design
Table 2: Network architectures for evaluated benchmarks. Conv$_{x,y,z}$ denotes a convolutional layer with $x$ outputs, kernel size $y \times y$ and stride $z$. FConn$_x$ is a fully connected layer with $x$ outputs. MaxPool$_{x,y}$ is an $x \times x$ maximum-pooling layer with stride $y$, and BatchNorm and SoftMax are batch normalization and normalized exponential layers, respectively. ResBlk$_{x,y,z}$ denotes a residual block with two Conv$_{x,y,z}$ layers, each followed by a BatchNorm. Layers in bold were unrolled and targeted for logic expansion (and shrinkage). For ImageNet, the residual block in bold had its first convolutional layer unrolled and targeted.

| Dataset | Model | Network architecture |
|---------|-------|----------------------|
| MNIST [6] | LFC [19] | FConn$_{256}$, BatchNorm, FConn$_{256}$, BatchNorm, FConn$_{256}$, BatchNorm, FConn$_{256}$, BatchNorm, FConn$_{10}$, BatchNorm, SoftMax |
| SVHN [13] & CIFAR-10 [5] | CNV [19] | Conv$_{64, 3, 1}$, BatchNorm, Conv$_{64, 3, 1}$, BatchNorm, MaxPool$_2$, 2, Conv$_{128, 3, 1}$, BatchNorm, Conv$_{128, 3, 1}$, BatchNorm, FConn$_{256}$, 3, 1, BatchNorm, FConn$_{512}$, BatchNorm, FConn$_{10}$, BatchNorm, SoftMax |
| ImageNet [2] | Bi-Real-18 [9] | Conv$_{64, 7, 2}$, BatchNorm, MaxPool$_3$, 2, ResBlk$_{64, 3, 1}$, ResBlk$_{64, 3, 1}$, ResBlk$_{128, 3, 2}$, ResBlk$_{128, 3, 2}$, ResBlk$_{256, 3, 2}$, ResBlk$_{512, 3, 2}$, ResBlk$_{512, 3, 2}$, FConn$_{10}$, SoftMax |

5.3 Training Specifics

5.3.1 Small-Scale Datasets. For our experiments with MNIST [6], SVHN [13] and CIFAR-10, pretrained ReBNet BNNs were first node-pruned and logic-expanded following the LUTNet approach (described in Section 3) before being logic-shrunk (Section 4). We inserted four new retraining phases between the post-node pruning (---) and post-logic expansion (----) phases performed for LUTNet shown in Figure 3a. These are reflected in Figure 3b. After logic expansion, we performed 50 epochs of retraining with high-precision forward propagation (---), with a further 20 (----) performed following each of three logic shrinkage iterations. Finally, 200 epochs with binarized forward propagation (---) were performed, matching the final phase of LUTNet training. We chose these numbers of epochs and logic-shrinkage iterations since, as exemplified in Figure 3, training accuracy saturation was achieved at or before the end of each phase. All training phases were executed in TensorFlow and accelerated using Nvidia RTX 3090 GPUs.

5.3.2 ImageNet. We also experimented with the ImageNet dataset. For this task, we prepared a pretrained Bi-Real Net model [9], Bi-Real-18, as our starting point, and then performed the retraining process outlined in Section 5.3.1. Here, we ran post-logic expansion retraining for 32 epochs (rather than 50), post-logic shrinkage retraining for eight epochs per iteration (rather than 20) and final, binarized retraining for 64 epochs (rather than 200). These numbers were again chosen due to our observance of accuracy stability.

5.4 Area Efficiency

In line with the prior FPGA-tailed DNN works detailed in Section 2.1, our primary objective was to maximize the area efficiency of our implementations. We define this as the number of device LUTs required to construct a network able to achieve a particular test accuracy for a given dataset while operating at a given classification rate. In all of our experiments, throughput remained fixed, thus we need only consider area vs accuracy.

5.4.1 Pruning Sparsity Tuning. We began by seeking to understand the interplay between the sparsity afforded to us through BNN node sparsification (by tuning $\theta$) and LUT input pruning ($\delta$). To this end, Figure 4 shows the achieved whole-network area vs top-1 test accuracy for LUTNet and logic-shrunk implementations of the CNN network trained to classify the CIFAR-10 dataset. Each point marks the mean of five differently seeded training runs, with an error bar indicating its range. For reference, the mean test error rate of encompassed the target layer only due to the complexity of implementing the remaining layers. In all cases, layers selected for logic expansion and shrinkage are marked in bold in Table 2.
Figure 4: Area-accuracy tradeoff for LUTNet (● ▲ ▼ ▶) and logic-shrunk (○ △ ◀ ▽) implementations of the CNV network classifying the CIFAR-10 dataset with (initial) LUT size \( K = 2 \) (a), \( K = 4 \) (b) and \( K = 5 \) (c). Each color/shape reflects a distinct node sparsity \( \theta \). Along a given curve, each logic-shrunk point is representative of a different LUT input sparsity \( \delta \). The reference accuracy—that for unpruned ReBNet—is annotated on each \( y \)-axis (<>).

ReBNet without pruning—again averaged over five training runs—is also shown (<>). Filled markers (● ▲ ▼ ▶) reflect results for LUTNet, split into those with LUT size \( K = 2 \) (Figure 5a), \( K = 4 \) (5b) and \( K = 5 \) (5c). Each color/shape represents a distinct node sparsity \( \theta \). Unfilled markers (○ △ ◀ ▽) capture area vs accuracy for logic-shrunk implementations with varying LUT input sparsity \( \delta \). Along each colored line, implementations all had the same \( K \) and \( \theta \), varying only in \( \delta \). Logic-shrunk designs used the respective fixed-\( K \) LUTNet architecture as the starting point for logic shrinkage, after which they contained LUTs up to size \( K \).

By comparing across data points of different shapes/colors, one can clearly observe that the error rate increases as more aggressive node pruning is applied. This trend is consistent across both the LUTNet and logic-shrunk implementations. Figure 4 also reveals relatively consistent area-accuracy tradeoffs exposed through the variance of LUT input sparsity \( \delta \) for each combination of \( K \) and \( \theta \). As \( \delta \) increases, connection pruning becomes more aggressive, pushing data points to the left. The error rate decreases at first due to the removal of redundant logic from the netlist. Beyond each curve’s inflection point, the pruning becomes too harsh; we thus begin to see the error rate rise. Also notice that, in some cases, \( K \)-LUT-based implementations outperform unpruned ReBNet (660196 LUTs) despite occupying as little as a quarter of its area. This speaks to the increased expressiveness of these architectures over BNNs.

Inspection of Figures 5a and 5b reveals that, in some cases, logic-shrunk implementations consume more area than the LUTNet architectures they were shrunk from. This is counterintuitive since logic shrinkage reduces netlist complexity by severing LUT connections; it never adds them. We attribute this effect, which is more pronounced in denser networks (higher \( \theta \)) of smaller LUTs (lower \( K \)), to Vivado’s heuristic-based placement and routing algorithms.

These experiments suggest that the performance of logic-shrunk networks is more sensitive to the tuning of node sparsity \( \theta \) than LUT input sparsity \( \delta \). Figure 4 contains design points with \( \theta \) ranging from 91.0 to 98.0% and \( \delta \) in the range 0.0–87.5%. We can see that a 7 pp change in \( \theta \) has a larger impact on area-accuracy behavior than a change in \( \delta \) more than 10× in magnitude. We thus recommend that \( \theta \) be fine-tuned with \( \delta = 0 \) prior to increasing \( \delta \) with fixed \( \theta \). We have found \( \delta = 75\% \) to be a reasonable starting point.
5.4.2 Pareto-Optimality Analysis. Figures 4a–4c feature the data points taken from Figures 5a–5c with the addition of Pareto-optimal frontiers for the LUTNet (•••••) and logic-shrunk (△) implementations with identical (initial) LUT size $K$. For reference, points for the pruned ReBNet implementations used as starting points for logic expansion are also included (□ □ □ □ □). From these plots, we can quickly establish that logic shrinkage facilitates a significant area improvement—savings of up to 1.76X while remaining bounded within ±0.3 pp of the unpruned ReBNet accuracy—over LUTNet. As $K$ increases, the area gap between LUTNet and logic-shrunk designs increases, indicating that netlists of fixed-$K$-LUTs with higher $K$ are more redundant. Since logic shrinkage removes this redundancy, we would expect implementations with differing initial $K$ reaching comparable accuracy to be similar in size. We explore this hypothesis in Figure 6, in which the pairs of Pareto-optimal LUTNet and logic-shrunk implementations that resulted in the savings marked by dashed lines in Figure 5 are featured. As expected, the area of the logic-shrunk designs is relatively stable.

In Figure 4d, we overlay the frontiers across all $K$ taken from Figures 4a–4c. The LUTNet frontier (•••••) in Figure 4d captures all Pareto-optimal LUTNet points from the preceding subfigures. In comparison to that for pruned ReBNet (△ △ △ △ △), its placement demonstrates the significant area efficiency gain when moving from XNOR- to LUT-based networks for deployment on FPGAs. However, with logic shrinkage, we go further: all three logic-shrunk frontiers reflect improvement over LUTNet, with that using $K = 4$ as the starting point (—) performing the most favorably. While logic-shrunk implementations with initial $K = 5$ exhibit the greatest area savings over LUTNet, those with $K = 4$ have the best area-accuracy tradeoff. The superiority of designs with initial $K = 4$ can be attributed to the presence of 5-LUTs within those logic-shrunk implementations. The LUTs physically present in the target device are 6-LUTs, each capable of implementing either a single six-input function or two $k$-input functions with at least five (for $k = 5$), three (for $k = 4$) or one (for $k = 3$) shared inputs. There is less opportunity for packing of pairs of 5-LUTs than with 6-LUTs taking four inputs or fewer; hence the lower area efficiency of designs logic-shrunk from the starting point with $K = 5$. We thus recommend $K = 4$ as the starting point for exploration with new benchmarks.

5.4.3 Comparison to Random Pruning. To verify that logic shrinkage is an efficient sparsification method, we compared it against random LUT input pruning as a sanity check. The process for this was identical to that for logic shrinkage, but LUT inputs were removed at random. Our results for this set of experiments are shown in Figure 7. As evidenced by their Pareto fronts, logic-shrunk (△) implementations consistently outperformed those with random pruning (—), the former achieving a 1.50X area saving vs the latter at the unpruned ReBNet accuracy (□).
Two key features are apparent from the data in Table 3. Firstly, there are large gaps between pre-and post-synthesis LUT counts, with this phenomenon becoming more pronounced as δ increases. This is attributable to the logic optimization central to synthesis, opportunities for which increase as LUT size falls. The effects of optimization are particularly marked for 1-LUTs, the majority of which were optimized away. Three of the four possible functions performable by a 1-LUT (\( y = 0, y = 1, y = x \)) are free to implement. Only \( y = \bar{x} \) requires device resources, but in most cases can be absorbed by the downstream logic. Consequently, we see increasing LUT removal as the average LUT size decreases. Overall, we can conclude that logic shrinkage successfully promotes sparsity in such a way as to suit the optimizations performed during synthesis, resulting in highly area-efficient implementations.

### 5.4.5 Other Benchmarks.
We also benchmarked logic shrinkage using other popular datasets and models: MNIST (with LFC), SVHN (with CNV) and ImageNet (with Bi-Real-18). Table 4 shows the post-synthesis and post-implementation LUT requirements of each of these model-dataset combinations when implemented with LUTNet and logic-shrunk architectures with (initial) LUT size \( K = 4 \). The same layers for all pairs of designs were unrolled and pruned, with the node sparsity (and LUT input sparsity) tuned in an effort to keep their accuracy as close as possible.

For CNV classifying CIFAR-10, our use of logic shrinkage saw an area reduction of 1.54×. With the smaller datasets, the gains realized via logic shrinkage were less pronounced. The SVHN-CNV and MNIST-LFC combinations are more tolerant of sparsity, thus the majority of nodes in these networks were able to be removed prior to logic expansion. This left relatively little room for further improvement by logic shrinkage. Despite this, we still achieved area reductions of around 10% for these simpler tasks. For ImageNet on Bi-Real-18, the LUTNet layer was too large to fit our target FPGA, the XCVU9P (1182240 LUTs). Logic shrinkage with node and LUT input sparsity of 30% and 75%, respectively, saw its post-synthesis area reduced by 2.67×, thus leading to success in implementation.

### Table 3: Pre-and post-synthesis LUT size distributions for the LUTNet (●) and logic-shrunk (○) implementations with (initial) LUT size \( K = 4 \) and node sparsity \( \theta = 94\% \) reported in Figure 5b. Shaded cells mark the post-synthesis LUT size in the majority.

| LUT input sparsity \( \delta \) (%) | Top-1 test error rate (%) | Pre LUTs | Post LUTs | Pre 4-LUTs | Post 4-LUTs | Pre 3-LUTs | Post 3-LUTs | Pre 2-LUTs | Post 2-LUTs | Pre 1-LUTs | Post 1-LUTs |
|-----------------------------------|--------------------------|----------|-----------|------------|-------------|------------|-------------|------------|-------------|------------|-------------|
| 0.0                               | 15.89                    | 70778    | 53430     | 70778      | 49541       | 0          | 3654        | 0          | 233         | 0          | 2           |
| 25.0                              | 15.49                    | 70778    | 40209     | 29758      | 24405       | 29098      | 13629       | 10466      | 1852        | 9646       | 323         |
| 50.0                              | 15.18                    | 70778    | 21451     | 2642       | 2293        | 18130      | 12289       | 26592      | 6375        | 23414      | 494         |
| 75.0                              | 15.26                    | 62518    | 3212      | 0          | 0           | 998        | 816         | 6264       | 1708        | 55256      | 688         |
| 87.5                              | 16.00                    | 35262    | 945       | 0          | 0           | 6          | 2           | 116        | 32          | 35140      | 911         |

Figure 7: Area-accuracy tradeoff for randomly pruned (●) and logic-shrunk (○) CNV implementations trained to classify CIFAR-10 with initial LUT size \( K = 4 \). Each point reflects a distinct LUT input sparsity \( \delta \). Pareto frontiers for logic-shrunk (—one) and randomly pruned (—) designs are overlaid for comparison. The annotated arrow indicates the area saving between the best-performing implementations with accuracy ±0.3 pp from unpruned ReBNet’s (■).
Table 4: Top-1 test error rate and area—post-synthesis and post-implementation—for LUTNet and logic-shrunk designs with various models classifying various datasets. (Initial) LUT size $K$ was 4 in all cases.

| Dataset (network) | Architecture          | Node sparsity $\theta$ (%) | LUT input sparsity $\delta$ (%) | Error rate $\%$ | Area (post-synth.) | Area (post-impl.) |
|-------------------|------------------------|-----------------------------|---------------------------------|-----------------|--------------------|-------------------|
| MNIST (LFC)       | LUTNet                 | 99.9                        | 75.0                            | 2.13            | 62 919             | 58 192            |
|                   | Logic-shrunk           | 75.0                        | 75.0                            | 2.53            | 63 928             | 54 647            |
| SVHN (CNV)        | LUTNet                 | 95.0                        | 75.0                            | 3.80            | 201 644            | 154 814           |
|                   | Logic-shrunk           | 75.0                        | 75.0                            | 3.75            | 179 236            | 137 610           |
| CIFAR-10 (CNV)    | LUTNet                 | 91.0                        | 75.0                            | 15.42           | 339 479            | 291 349           |
|                   | Logic-shrunk           | 75.0                        | 75.0                            | 15.26           | 220 060            | 188 765           |
| ImageNet (Bi-Real-18) | LUTNet            | 30.0                        | 75.0                            | 45.13           | 1 840 666          | 2 -2 -2           |
|                   | Logic-shrunk           | 75.0                        | 75.0                            | 46.60           | 690 357            | 665 720           |

1 Target layer only. Designs for other datasets included all network layers.
2 Design could not fit onto target device.

5.5 Energy Efficiency

We also sought to quantify the energy efficiency impact attributable to logic shrinkage. To do so, we obtained power consumption estimates of both LUTNet and logic-shrunk implementations using the Xilinx Power Analyzer (XPA) tool with default settings: vectorless mode and 12.5% primary input switching probability. The resultant power estimates, for the same designs as captured in Figure 6, are shown in Figure 8. All were obtained post-placement and -routing. Power consumption is equivalent to energy efficiency here since all implementations have identical throughput.

Since dynamic power consumption is directly related to area occupancy, Figures 6 and 8 show similar trends. The static power remains consistent across all implementations. Overall, it can be concluded that the significant area reductions of logic shrinkage also result in energy efficiency improvements.

5.6 Training Efficiency

Logic shrinkage introduces additional matrix-vector multiplications for every forward propagation during retraining in order to ensure that pruned inputs remain severed. Thanks to the highly optimized linear algebra routines provided by GPUs, the slowdown in training speed with logic shrinkage is minor. This is evident in Figure 9, in which we capture per-epoch logic shrinkage overheads.

6 CONCLUSION

In this paper, we introduced logic shrinkage: the automated search for, and implementation of, LUT-based neural network inference accelerators in which LUT sizes and inputs are learned during training. We showed our realization of logic shrinkage to be lightweight and to result in the production of netlists that well suit the logic optimizations performed by FPGA synthesis tools. We analyzed hundreds of experimental results, finding significant area-accuracy tradeoff improvement over homogeneous LUT-based networks.

The authors of prior NAS works pursued a top-down approach, learning an intermediate representation—a network topology—while leaving its hardware mapping as a separate task. In contrast, we propose a bottom-up, hardware-aware alternative: directly learning a netlist as the topology, with the flexibility of the target platform exposed to the training process. We chose to focus on
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