Millimetre-wave high–low IMPATT source development: First on-chip experimental verification

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This paper reports design and development of high–low type Si/SiC-based Impact Ionisation Avalanche Transit Time device and its on-chip characterisation. The design has been performed with indigenously developed strain engineered non-linear self-consistent large-signal simulator. On-chip fabrication of Sc-MQTDD simulator is done successfully. The newly developed in-house strain-corrected mixed quantum tunnelling drift diffusion simulator is done successfully.

Introduction: Millimetre-wave frequency range of EM spectrum has immense application possibilities in the field of security sector for non-invasive imaging and improvised explosive device detection [1–3]. Amongst all two terminal millimetre-wave devices, Impact Ionisation Avalanche Transit Time (IMPATT) diodes have already proven their efficiency as high-power source in millimetre-/sub-millimetre-wave region [4–6]. Throughout the last decade, IMPATT diodes and oscillators have been steadily gaining significance in the field of high-power RF generation. However, most of the available IMPATT oscillators are fabricated with conventional Si or GaAs. But both Si and GaAs have intrinsic limitation of material parameters [7]. The capacity to deliver high power for an IMPATT oscillator depends on carrier saturation velocity, mobility, impact ionisation rate and breakdown electric field. Researchers are therefore searching for suitable semiconductor materials that exhibit such favourable material properties, for developing high-power, high-frequency IMPATT devices. Wide-band gap SiC and its hetero-structures are quite promising for high-frequency applications owing to superior material parameters, that is, 2× carrier saturation velocity, 5× mobility and 10× breakdown electric field than conventional Si [8]. Therefore, the current research has chosen SiC as a base material for the development of IMPATT oscillator chip [9, 10].

Design of the device has been done through an indigenously developed strain-corrected mixed quantum tunnelling drift diffusion (Sc-MQTDD) simulator. The simulation has taken into account the effects of parasitic series resistance, quantum effects, junction temperature enhancement effects, lattice phonon interaction effects, generation–recombination of charge carriers, field- and temperature-dependent carrier saturation velocity, mobility and ionisation rates and both substrate- and process-induced strains. Recent research has shown that the impact of process-induced strain on device characteristics is extremely significant [11–16]. Therefore, the previously used in-house simulator [17, 18] has been modified by incorporating strain effects and the validity of the same has already been established [6]. The non-linear DC and large-signal properties of the device under test (DUT) are obtained for W-band operation. The fabrication of the device has been started with a high-resistivity Si substrate (1×1023 m–3 concentrations). The epilayer of SiC (n-type on substrate, 3.5×1021 m–3 doping) has been developed through metal organic chemical vapour deposition technique. A buffer layer of n+ (6×1023 m–3 doping) was grown between the substrate and n-epilayer. The detailed of grown high–low structure is shown in Figure 1a.

To the best of authors’ knowledge, this is the first report on high–low IMPATT development and verification of the in-house simulator.

Theoretical model: This paper designs and analyses the 2D vertical and asymmetrically doped Si/SiC-ATT (p++-n-n+-p++ doping profile) device. Schematic representation of the designed diode is shown in Figure 1a. Throughout the current paper, in-plane means yz-plane and out-of-plane implies z-direction. Physical properties of Si/SiC material along the symmetric axis of the device are obtained from published literature [8]. At each instant of time the physical properties such as electric field, electron and hole current components, recombination current are obtained by solving the non-linear field and carrier transport equations, that is, Poisson’s equation and combined current continuity equations for various large-signal modulation factors at the edges of active region, subject to satisfaction of appropriate modified boundary conditions [19]. The authors have considered the effect of introducing an n-bump layer of appropriate doping concentration in between the substrate and epi-layer. The space- and time-dependent transport equations are described elsewhere [20, 21]. The carrier generation rates due to avalanche multiplication are given by equations 1–4 for electrons and holes.

\[
E_{\text{Effective}}(z) = -q\left(\Phi_{2D}(z) + G_{\text{OM}}\right) + \frac{E_{G}}{2} + \kappa T \ln \left(\frac{N_{c}}{N_{e}} + \Phi_{\text{Deformation}}\right),
\]

where \(G_{\text{OM}}\) is the Bohm quantum potential and is given as follows for electrons/holes:

\[
G_{\text{OM}}(z) = k_{B}T \left(\nabla \cdot \left(\frac{\mathbf{j}_{\text{neff}}}{\sqrt{N_{t}}}\right)\right),
\]

\(c_{e/p}\) denotes electron/hole density:

\[
G_{\text{OM}}(z) = k_{B}T \left(\nabla \cdot \left(\frac{\mathbf{j}_{\text{neff}}}{\sqrt{N_{t}}}\right)\right),
\]

\(c_{e/p}\) denotes electron/hole density:

\[
\frac{1}{q} \frac{\partial}{\partial z} C_{e/p}(z, t) = F_{e/p}(z, t) + G_{\text{Gain}}(z, t) + G_{\text{Loss}}(z, t),
\]

where \(F_{e/p}(z, t)\) is the generation rate and \(G_{\text{Gain}}(z, t)\) and \(G_{\text{Loss}}(z, t)\) are the gain and loss rate respectively.

Fig. 1 (a) Schematic diagram of DUT; (b) Si/SiC mesa diode with 50 μm diameter and (c) on-chip W-band IMPATT source (top view)
where $G_{A,TT}(z, t)$ and $G_{P,TT}(z, t)$ are the avalanche and tunnelling generation rates, respectively. The details have been explained elsewhere [6]. In Equations (2), $\Phi_{2D}(z)$ is the potential due to reverse bias, for which the Poisson equation is as follows, with symbols having their usual meanings:

$$
\frac{\partial^2 \Phi}{\partial z^2} (z, t) = -\frac{q}{\varepsilon} \left( N_D - N_A + \varepsilon_{sp} \right) (z, t),
$$

(6)

and $\Phi_{\text{Deformation}}$ is the strain-induced deformation potential:

$$
\Phi_{\text{Deformation}} = -2d_i \varepsilon_{i,j} \left( \frac{C_{ij} - C_{ii}}{C_{ii}} \right),
$$

(7)

where $\varepsilon_{i,j}$ is the induced strain due to doping, lattice and thermal mismatch. $d_i$, $C_{ii}$ and $C_{ij}$ are relevant deformation and elastic constants, $i, j \in x, y, z$. Finally, the current density equation is written as

$$
J_{SP}(z, t) = -q \mu_p \frac{\partial}{\partial z} \left( \frac{\partial V}{\partial z} + G^{0D}_{p,TT}(z, t) \right) \pm \frac{KT}{q} \frac{\partial}{\partial z} \left( \frac{\partial \Phi}{\partial z} - \varepsilon_{sp} \right) (z, t)
$$

(8)

The coupled Schrodinger–Poisson equations along with the current density and continuity equations have been solved simultaneously. Details of the approach that has been used for such purpose have been explained elsewhere [6]. Finally, the conductance and susceptance for the ATT diode are expressed as follows:

$$
G_{ATT} (\omega) = \frac{\Gamma_{ATT} (\omega)}{\left( \Gamma_{ATT} (\omega) \right)^2 + \left( x_{ATT} (\omega) \right)^2},
$$

(9)

$$
B_{ATT} (\omega) = \frac{-x_{ATT} (\omega)}{\left( \Gamma_{ATT} (\omega) \right)^2 + \left( x_{ATT} (\omega) \right)^2},
$$

(10)

where $\Gamma_{ATT} (\omega)$ and $x_{ATT} (\omega)$ are the resistance and reactance, respectively.

The Poisson and current continuity equations are solved at each space-steps for each phase of time cycle ranging from $T = 0$ to $2\pi$ for different modulation index. At present, the authors have considered 50% modulation above the breakdown voltage. Through this double iterative, self-consistent, voltage exited model/technique quasi-2D space–time analysis of the DUT has been done. The present extensive model/simulation takes into account the mobile space-charge effect, carrier diffusion effect, charge carrier generation–recombination effects in the central region and involves double iteration over the magnitude and location of field maximum for obtaining electric field and current density profiles. The modified boundary conditions for electric field (E(x, t)) and normalised current density (P(x, t)), in Se-MQTTD model are described elsewhere [20, 21]. The large-signal impedance and admittance plots are obtained through the in-house simulator as described earlier [21].

**Experimental procedure:** A suitable 3C-SiC epi layer has been grown on Si(1 0 0) 1–10 Ω cm substrates with 100 mm diameter. A heteroepitaxial Si/3C-SiC layers are grown by mixing together a C-based precursor with an Si-based gas chemical vapour deposition (CVD) reactor. This is done at a high temperature (>1250°C), and this requires controlling high temperature. It is to some extent difficult to control two separate precursors; Si and C and the use of a separate precursor could improve the surface morphology. Thus, to improve the crystal quality and to reduce the high-leakage currents, the experiment is carried out with the growth of 3C-SiC p–n junctions on a Ge-modified Si (1 0 0) substrate. Trapped charges are found to generate at the interface of substrate and epilayer. Oxidation process is done to rectify the issue. The defects at the semiconductor interface produced leakage current during reverses bias operation. Thermal oxidation has been done at the height of the first state of mesa. Low-resistance ohmic contacts are formed using E-beam evaporation techniques and photo-lithography, and mesa etching, following standard techniques, are performed sequentially to obtain on-chip diode dots. This is followed by on-chip I–V characterisations.

**Results and discussions:** The schematic diagram of the fabricated device is shown in Figure 1a. Figure 1b shows the mesa diode with 50 μm diameter. The on-chip device is shown in Figure 1c. The reverse and forward characterstics are shown in Figure 2a and b, respectively. The simulated device is found to break down at 188 V. The large-signal simulation study depicts the variation of peak electric E(x) field profile with different phase angle for $T = 0–2\pi$. The RF power output from the simulated device is ~10 W for a 3 × 3 array of diodes at a peak operating frequency of 94.3 GHz. Further experimental results show that the device breaks down at 185 V, close to the simulated data with the corresponding breakdown current ~12.5 mA. Incorporation of Ge layer reduces the surface roughness significantly and thus the leakage current reduces. This in turn has increased the output power. If the diode chip is mounted properly with W-band waveguide and is expected to generate ~2 W of RF power from a single diode at W-band window frequency (~94.0 GHz). Variation of breakdown voltage and efficiency with the DC operating current density, under experimental and simulation conditions, are plotted in Figure 3. It is interesting to observe that within the range of operating current density (15 × 10^7 A/m^2 to 25 × 10^7 A/m^2), the

![Fig. 2 (a) Reverse characteristics of on-chip device and (b) forward characteristics of on-chip device](image)

![Fig. 3 Comparison of experimental and simulation results](image)
agreement between theory and experiment is quite satisfactory. However, further increment of DC-operating current density results in the degradation of breakdown voltage in experimental observation. This is due to the fact that excessive junction temperature/oule heating in turn increases the parasitic effects and that degrades the overall device performance. Moreover, increasing bias current density increases the device efficiency up to $25 \times 10^7$ A/m$^2$. It starts degrading with further increase in bias current density. The efficiency graph shows a tendency of saturation within the current density range of $20 \times 10^7$ A/m$^2$ to $30 \times 10^7$ A/m$^2$. This may be explained in terms of enhancing undepleted epilayer with increasing current density as a result of mobile space-charge effect. This leads to the decrease in the voltage across avalanche region and the subsequent saturation of efficiency level.

Conclusion: For the first time, Si/SiC high–low type IMPATT source is developed and on-chip characterisation is reported. The potential of heterostructure IMPATT source at W-band frequency in terms of high power generation is reported. The experimental validation of the newly proposed Sc-MQTDD simulator is established.

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