Optimization of spacer and source/channel junction to improve TFET characteristics

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Abstract As the electrical characteristics of tunnel field-effect transistors (TFETs) are greatly influenced by the source junction and the gate spacer, the effects of these parameters are analyzed by technology computer-aided design simulation. As a result, it is found that an ON-state current of TFETs can be improved by +161.8% through the high-κ spacer of an appropriate length when the source junction does not overlap the edge of the spacer. In addition, it is confirmed that an intrinsic delay time which determines the high frequency characteristics is also reduced by ~65.9% because an increase of entire gate capacitance, a side effect of the high-κ spacer, is negligible.

Keywords: tunnel field-effect transistor (TFET), source/channel junction, high-κ spacer

Classification: Electron devices, circuits and modules (silicon, compound semiconductor, organic and novel materials)

1. Introduction

Recently, the demands for low power semiconductor chips are increasing in various fields such as mobile products, data centric computation and internet of things (IoT). When a supply voltage ($V_{dd}$) is lowered for the low power applications, it is essential to lower a subthreshold swing ($S$) to maintain a high ON-state current ($I_{on}$) and a low OFF-state current ($I_{off}$). However, as the metal-oxide-semiconductor field-effect transistors (MOSFETs) cannot reduce $S$ below 60 mV/dec at room temperature due to its fundamental limitations [1, 2], several new devices such as positive feedback FETs [3, 4], negative capacitance FETs (NCFETs) [5, 6, 7], nano-electro mechanical FETs (NEMFETs) [8, 9] and tunnel FETs (TFETs) [10, 11, 12, 13, 14, 15] are being explored as alternatives. Among them, TFETs are devices using band-to-band tunneling between source and channel as a current driving mechanism, and have received much attention because of those high compatibility with conventional complementary MOS (CMOS) processes [16, 17]. In order to improve $S$ and $I_{on}$ of TFETs, the width of the tunneling barrier should be narrowed by making abrupt energy band bending at the source junction when the tunneling current flows. To implement this, the electric field of the gate edge applied to the source junction should be precisely adjusted. In the structure of TFETs, the location of the source junction and the spacer located on the sidewall of the gate are important factors influencing this electric field. Therefore, various researches have been conducted to analyze the effect of the source junction and the spacer on the electrical characteristics of TFETs [18, 19, 20]. However, the source junction and the spacer do not independently affect the electrical characteristics of TFETs, but are closely related to each other. Therefore, in this study, we optimize the high-κ spacer length and the source junction location considering the interactions between the two parameters precisely by using technology computer-aided design (TCAD) simulations to maximize $I_{on}$ of TFETs. In addition, even though $I_{on}$ is improved by applying a high-κ spacer in a specific case, gate capacitance ($C_{gs}$) is increased by using high-κ material in general, and as a result, transient characteristics can be deteriorated. Therefore, we also analyzed the intrinsic delay time considering the change of $C_{gs}$.

2. Device structure and simulation method

Fig. 1 shows the device structure and the definitions of major parameters used in this research. All of the simulations are performed based on the double gate TFET structure. The values of design parameters are summarized in Table 1. A Ge is adopted as a body material to improve $I_{on}$ and $S$ by using narrow bandgap and direct tunneling components [21, 22, 23, 24, 25, 26, 27]. The relative permittivity and thickness of a gate insulator are 3.9 and 2 nm, respectively. As a result, an equivalent oxide thickness (EOT) of the gate insulator is set to 2 nm. And, a channel thickness ($T_B$) between the gates is 10 nm for a high gate controllability. The source is set as a 10$^{18}$cm$^{-3}$-doped p-type while the channel is undoped. Although the use of Ge in the channel could improve $I_{on}$ of TFETs [27], it delivers large $I_{off}$ and the ambipolar effect. It is known that lowering the drain doping concentration can suppress $I_{off}$ of Ge TFET effectively [28]. Therefore, in this research, the drain is composed of a 10$^{18}$cm$^{-3}$-doped n-type region to minimize $I_{off}$ and the ambipolar effect. The relative permittivity of inter-layer dielectric (ILD) region is set to 3.9 corresponding to SiO$_2$. Since the electrical characteristics of TFETs are determined by an electric field applied to the junction between the source and the channel, the material and the length of the spacer have a significant impact on the performance of TFETs. In order to analyze this effect of the spacer,

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the relative permittivity of the spacer is set to 22.0 corresponding to HfO$_2$ [29], and the change in the characteristics of the TFET according to the length of high-$\kappa$ spacer ($L_{SP}$) is examined. When using the high-$\kappa$ spacer, the Ge region under the high-$\kappa$ spacer can also be regarded as a channel due to the high influence of the gate voltage ($V_g$). Therefore, the channel length ($L_{CH}$) is defined as the sum of the $L_{SP}$ and the gate length ($L_g$), and is fixed at 50 nm. Since the position of the source junction, as well as the spacer, is an important factor in the performance of TFETs, the change of the electrical characteristics is examined while changing the length of the source/drain underlap ($L_{UL}$) from the channel edge (i.e., spacer edge).

Fig. 1  Basic schematic and major parameter definitions of double gate Ge TFET in this research.

| Table 1 Parameters used for TCAD simulation. |
| Parameter | Value |
| --- | --- |
| Gate work function | 4.05 eV |
| Equivalent oxide thickness (EOT) | 2 nm |
| Channel thickness ($T_e$) | 10 nm |
| p-type source doping concentration | $10^{16}$ cm$^{-3}$ |
| n-type drain doping concentration | $10^{16}$ cm$^{-3}$ |
| Permittivity of the ILD | 3.9 |
| Permittivity of the spacer | 22.0 |
| Channel length ($L_{CH}$) = $L_{SP}$ + $L_g$ | 50 nm |

To analyze the electrical characteristics of the device, TCAD simulation is performed using Synopsys Sentaurus$^\text{TM}$ [30]. For accurate extraction of the electrical characteristics, modified local density approximation (MLDA), Fermi–Dirac statistics, doping concentration dependent mobility, dynamic nonlocal band-to-band tunneling, and Schockley-Read-Hall (SRH) recombination models are used for the simulation. Since this research is conducted based on two-dimensional (2-D) simulation, all drain current characteristics are normalized by 1 $\mu$m-width.

3. Result and discussion

At first, to check the effect of the source junction location on the TFET characteristics, the change in $I_{on}$ is examined while changing $L_{UL}$ without the high-$\kappa$ spacer ($L_{SP}$ = 0 nm) as shown in Fig. 2(a). The $I_{on}$ is defined as the drain current when the drain voltage ($V_D$) is 0.95 V and the $V_g$ is threshold voltage ($V_{th}$) + 0.5 V. The $V_{th}$ is defined as the gate voltage when the drain current is 1 nA/$\mu$m. The $I_{on}$ of the TFET is the highest when $L_{UL}$ is 0 nm when the source junction is exactly aligned at the channel boundary, and gradually decreases when $L_{UL}$ is far apart or overlapped. In order to analyze the reason, the energy band at the source junction is examined as shown in Fig. 2(b). When $L_{UL}$ is 0 nm, the electric field by the gate is effectively concentrated at the junction, resulting in steep band bending and narrow tunneling width. On the other hand, when $L_{UL}$ < 0 nm, the electric field pulls down the energy band of the source region together. And, in the case of $L_{UL}$ > 0 nm, the electric field does not sufficiently pull down the energy band of the channel. As a result, in all cases where the $L_{UL}$ is not 0 nm, $I_{on}$ decreases as the tunneling width increases.

Next, the effect of the $L_{SP}$ on the characteristics of the TFET is examined. In order to consider the effect of the location of the source junction at the same time, the analysis is performed for each case of $L_{UL}$ is -7 nm and 2.3 nm, respectively. As will be discussed at the end of this chapter, when the overlap between the source junction and gate edge is large ($L_{UL}$ ≪ 0 nm), the electrical characteristics of the TFET are deteriorated by applying the high-$\kappa$ spacer. Therefore, as a representative case, the analysis is performed when $L_{UL}$ = -2 nm, which is the smallest value in this research. In contrast, when the source junction and the gate edge are underlapped, using the high-$\kappa$ spacer with optimized length improves the electrical characteristics of the TFET. Therefore, the case where $L_{UL}$ = 2.3 nm, which shows the most
improved electrical characteristics, is also analyzed.

At first, Fig. 3(a) shows the change of $I_{on}$ according to $L_{SP}$ when $L_{UL}$ is $7$ nm. As $L_{SP}$ increases, $I_{on}$ decreases gradually, and at $L_{SP} = 4.7$ nm, $I_{on}$ decreases by $12.8\%$ compared to the absence of the high-$k$ spacer. The reason why $I_{on}$ decreases as the $L_{SP}$ increases when the source junction overlaps the high-$k$ spacer ($L_{UL} < 0$ nm) can be confirmed by the energy band of the source junction in Fig. 3(b). As high electric field is transmitted through the high-$k$ spacer to the source region below the spacer, unnecessary energy band bending occurs to this region, which increases the tunneling width and decreases $I_{on}$.

Contrary to the above, the change of $I_{on}$ according to the change of $L_{SP}$ when the source junction is located away from the high-$k$ spacer ($L_{UL} = 2.3$ nm) is shown in Fig. 4(a). Initially, as $I_{on}$ increases with increasing $L_{SP}$, $I_{on}$ increases to $+157.2\%$ when $L_{SP} = 2.3$ nm compared to the absence of the high-$k$ spacer. However, as $L_{SP}$ becomes larger than $2.3$ nm, $I_{on}$ tends to decrease as $L_{SP}$ increases. As shown in Fig. 4(b), during the initial increase of $L_{SP}$ at $L_{UL} > 0$ nm, the high-$k$ material increases the electric field applied to the source junction, resulting in abrupt energy band bending and reduced tunneling width. However, if $L_{SP}$ increases over a certain level, the physical distance between the gate and the source junction becomes too far and the electric field decreases. As a result, the change of the energy band by the gate bias decreases and the tunneling width increases.

Summarizing the previous results with the change in $L_{UL}$ and $L_{SP}$, the highest $I_{on}$ (10.5 $\mu$A/um) can be obtained when both $L_{UL}$ and $L_{SP}$ are 2.3 nm. However, in order to optimize the device’s performance in high frequency (HF) range, not only $I_{on}$ but also changes in capacitance must be considered. Fig. 5 shows the change in the entire gate capacitance ($C_{gg}$) with increasing $L_{SP}$ when $L_{UL} = 2.3$ nm. $L_{SP}$ of the appropriate length helps improve $I_{on}$ as in the previous analysis, but the use of high-$k$ materials increases $C_{gg}$ as shown in Fig. 5. Although $C_{gg}$ increases due to the use of high-$k$ material, the amount of increase is only $+2.4\%$ when $L_{SP} = 2.3$ nm, which is very small value compared to the increase in $I_{on}$ (+157.2%). The length of the spacer is short compared to the total length of the gate that determines capacitance with the source, channel, and drain. Therefore, the use of high-$k$ spacer does not significantly increase $C_{gg}$.

In order to analyze switching characteristics of the TFET in HF range by considering the change of $I_{on}$ and $C_{gg}$ simultaneously, intrinsic delay time ($\tau$) which is define as $C_{gg} \cdot V_{dd}/I_{on}$ is extracted [31]. A 0.95 $V$-$V_{dd}$ is used as $V_{dd}$ in
this research. Fig. 6 shows extracted $\tau$ with the change of $L_{SP}$ when $L_{UL} = 2.3$ nm. Since the increase of $I_{on}$ by $L_{SP}$ is much larger than the increase of $C_{gg}$, $\tau$ becomes the smallest at $L_{SP} = 2.3$ nm where $I_{on}$ is most improved.

Finally, the changes of $I_{on}$ and $\tau$ due to the changes of $L_{UL}$ and $L_{SP}$ are summarized in Fig. 7 and Fig. 8, respectively. The highest $I_{on}$ (10.7 A/μm) is obtained when both $L_{UL}$ and $L_{SP}$ are 2.3 nm, which is +161.8% higher than when $L_{UL}$ and $L_{SP}$ are 0 nm. Since $\tau$ is determined by the change in $I_{on}$ rather than the change in $C_{gg}$, $\tau$ also becomes the smallest (24.7 ps) under the same condition, which is −65.9% smaller than when $L_{UL}$ and $L_{SP}$ are 0 nm.

4. Conclusion

Through TCAD simulation, the effects of source junction location and high-κ spacer length on the electrical characteristics of TFETs are investigated. In the absence of a high-κ spacer, the highest $I_{on}$ can be obtained when the $L_{UL}$ is 0 nm. At $L_{UL} < 0$ nm, $I_{on}$ decreases when the high-κ spacer is applied. On the other hand, when $L_{UL} > 0$ nm, $I_{on}$ can be improved by using appropriate length of the high-κ spacer. In this case, $C_{gg}$ increases due to the high-κ spacer, but the intrinsic delay time is reduced by the improvement of the $I_{on}$ as the change of $C_{gg}$ is small compared to the increase of $I_{on}$.

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