On-the-fly Vertex Reuse for Massively-Parallel Software Geometry Processing

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Figure 1: Reducing the number of shader invocation during rendering is essential to guarantee high performance. Traditionally, redundant vertex shading can be bypassed using a post-transform cache, but its poor scalability makes the vertex cache a poor choice in massively parallel environments. (a) The batch-based approaches we explore in this work show good reuse characteristics on modern GPUs (green vertices are shaded only once, dark red six times). (b, c) We evaluate static and dynamic batching in a variety of applications, e.g., rasterization of captured game scenes and computation of mesh simplification envelopes. The Witcher 3: Wild Hunt screenshot courtesy of CD PROJEKT S.A.; used with permission.

ABSTRACT

Compute-mode rendering is becoming more and more attractive for non-standard rendering applications, due to the high flexibility of compute-mode execution. These newly designed pipelines often include streaming vertex and geometry processing stages. In typical triangle meshes, the same transformed vertex is on average required six times during rendering. To avoid redundant computation, a post-transform cache is traditionally suggested to enable reuse of vertex processing results. However, traditional caching neither scales well as the hardware becomes more parallel, nor can be efficiently implemented in a software design. We investigate alternative strategies to reusing vertex shading results on-the-fly for massively parallel software geometry processing. Forming static and dynamic batching on the data input stream, we analyze the effectiveness of identifying potential local reuse based on sorting, hashing, and efficient intra-thread-group communication. Altogether, we present four vertex reuse strategies, tailored to modern parallel architectures. Our simulations showcase that our batch-based strategies significantly outperform parallel caches in terms of reuse. On actual GPU hardware, our evaluation shows that our strategies not only lead to good reuse of processing results, but also boost performance by $2 - 3 \times$ compared to naively ignoring reuse in a variety of practical applications.

CCS CONCEPTS

• Computing methodologies → Rasterization; Massively parallel algorithms;

KEYWORDS

Vertex Processing, GPU

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1 INTRODUCTION

Although hardware-supported, real-time rendering of 3D scenes is highly efficient, the standard rendering pipeline implemented in hardware lacks flexibility in certain aspects. With modern graphics processing units (GPU) inexorably rising in compute power, implementing (parts of) custom pipelines in compute-mode, i.e.,
in software, becomes an interesting alternative. Although certain features—like rasterization—will likely always be multiple orders of magnitude faster in hardware, others may efficiently be realized also in software. Primitive transformations, i.e., vertex shading, is one of those applications. While implementing vertex shading stages in software for execution on GPU compute units becomes more and more common, vertex reuse, i.e., reusing the result of the vertex shader when it is referenced more than once, is usually ignored. This is in part due to vertex reuse being realized in hardware in the conventional pipeline—a feature that is not exposed for custom use in software.

However, vertex reuse should not be neglected, as it offers several benefits for high-performance rendering. In addition to a significant reduction of required memory for storing input geometry data, effective vertex reuse can greatly reduce the number of shader invocations. A vertex in a mesh is, on average, referenced up to six times. The traditional solution to enable vertex reuse is the employment of a post-transform cache. The post-transform cache stores shaded vertex information, which can then be retrieved instead of computing the same information multiple times [Sheaffer et al. 2004, Wang et al. 2011]. The significance of this assumption is underlined by the wide body of research aiming at improving the ordering of vertices in meshes to yield better cache behavior. Unfortunately, there is little publicly available information on the implementation specifics used in current GPUs. The lack of mention of the post-transform cache in more recent articles [Kubisch 2015, Purcell 2010] also raises the question, to which degree the widely accepted preconceptions about vertex reuse still hold.

The adequacy of a central vertex cache in contemporary graphics pipelines and its use in a software pipeline should be questioned, and justifiably so: with the increasing degree of parallelism usually present in modern GPUs, the costs of a post-transform cache can be expected to rise drastically. Alternative design choices tailored towards massively parallel devices may circumvent this bottleneck while achieving similar or even better reuse characteristics. In this light, we see large potential benefits by revisiting the problem of efficient vertex reuse with an additional focus on software rendering pipelines. In search of methods capable of scaling with the massively parallel architecture of current and future GPUs, we make the following contributions:

(1) We investigate batch-based vertex uniquization as an alternative to post-transform caching for achieving reuse.

(2) Next to a naïve processing scheme, we discuss four batch-based approaches to identify unique vertices on massively parallel devices.

(3) We evaluate all approaches with respect to their theoretical and practical vertex reuse effectiveness in a variety of computer graphics applications.

2 RELATED WORK

It has been realized early on that there is significant potential for optimization by minimizing redundancy in an input stream describing mesh geometry. The pioneering work by Deering [1995], Evans et al. [1996], and Chow [1997] considered the problem from a data compression point of view. However, due to this angle of approach, these methods required input geometry to always first be encoded according to some compression scheme which would then be decompressed during processing.

Hoppe et al. [Hoppe 1999] were the first to explore the use of a k-FIFO post-transform vertex cache to reduce redundant vertex processing on-the-fly during rendering of triangle meshes. They furthermore presented a set of algorithms that automatically optimize the rendering sequence for a given mesh to maximize utilization of their proposed cache architecture. The downside of their optimization approach is that it requires exact knowledge of the properties of the underlying hardware which are subject to change. However, their work inspired a long line of followup research improving upon their results. [Chhugani and Kumar 2007; Lin and Yu 2006; Sander et al. 2007] Arguably one of the most impactful works is the architecture-agnostic approach by Forsyth [Forsyth 2006].

A more current area of research where we encounter the problem of massively parallel vertex processing is software rendering on the modern GPU. Noteworthy examples of GPU software rendering pipelines include Freepipe [Liu et al. 2010], CUDARaster [Laine and Karras 2011], and Piko [Patney et al. 2015]. They all use the compute mode of the GPU (typically on top of the CUDA [NVIDIA 2016] ecosystem) to implement rasterization and fragment shading, but lack mechanisms for vertex reuse. Freepipe simply executes the vertex shader every time an index is fetched. CUDARaster and Piko run the vertex shader in a preprocessing step on the entire vertex buffer and store the results in global memory. This strategy is wasteful if a substantial portion of the vertices is never referenced or used during rendering, which is a rather common case in practice, e.g., with methods such as level-of-detail or occlusion culling. The need for buffering the entire intermediate output of the geometry stage also leads to excessive memory requirements.

In order to avoid ambiguity in the following sections, we will employ the nomenclature for parallel execution and hardware concepts according to CUDA [NVIDIA 2016]. Hence, wave fronts of single-instruction-multiple-data (SIMD) width will be referred to as warp. Warp divergence indicates the case where threads follow redundant execution paths, since warps advance in lockstep. Logical groups of warps that run on the same multiprocessor share a portion of fast local shared memory and can easily synchronize will be addressed as blocks.

3 VERTEX REUSE STRATEGIES

A major goal of this work is a characterization of vertex reuse in a software-based, massively parallel context, and heightening the understanding of its influence on graphics workload. To this aim, we formulate the following assumptions: We only consider indexed triangles as primitives, for which the index buffer can be used to identify recurring vertices (Figure 2). The routine (or shader) for processing a vertex is invoked based on an index buffer, where groups of threads are assigned to consecutive primitives in the index buffer. In the ideal case, the vertex shader should be executed only once for each vertex that is referenced by the index buffer. To ensure high performance, shading must happen in parallel, without any need for expensive synchronization or communication across GPU multiprocessors. In order to support maximum performance in streaming pipelines, preprocessing of the vertex or index buffer should be kept at a minimum, or avoided altogether.
An obvious challenge in the parallel generation of this many-to-one mapping is that the input-to-output ratio is not known in advance. Ideally, we would like to choose a batch size such that the number of unique vertices stays constant size $N_u$. For this reason, we use a common multiple of the block size and the primitive size as batch size, e.g., for triangles and thread block size 32, we could use any multiple of $3 \times 32 = 96$. Since the batch size is fixed, static batching requires no preprocessing of the index buffer and can be applied directly to the input of a streaming pipeline.

Statically batched warp voting. For this strategy, we aim to fill up warps with triangles so that every thread receives a unique vertex to process. As a guideline for efficient processing, we use a common multiple of the block size and the primitive size as batch size, e.g., for triangles and thread block size 32, we could use any multiple of $3 \times 32 = 96$. Since the batch size is fixed, static batching requires no preprocessing of the index buffer and can be applied directly to the input of a streaming pipeline.



3.2 Batch-based vertex reuse

To avoid the issues raised by the use of a central cache, we propose the concept of batch-based vertex processing, which naturally lends itself to execution on massively parallel architectures. A batch is defined by us as a bounded region in the index buffer, that is assigned to a single warp or block for processing. The thread block is responsible for executing the shader once for each referenced vertex within its batch and assembling the output triangles. Each thread must analyze its batch, assign vertices uniquely to threads for shader invocation and finally distribute shading results for assembling the output triangles. This implies that duplicate indices in the batch need to be identified before executing the vertex shader.

An obvious challenge in the parallel generation of this many-to-one mapping is that the input-to-output ratio is not known in advance. Ideally, we would like to choose a batch size such that the number of unique vertices equals the block size, and one thread can run exactly one instance of the vertex shader. If that is not the case, under-utilization will arise, as threads that receive no unique vertex to process will simply idle. With larger batch sizes, it may be possible to identify a larger number of duplicate indices, at the cost of requiring multiple rounds of shader invocations to finish a whole batch. These considerations lead to the proposal of two strategies outlined in Figure 3: static batching and dynamic batching.

3.3 Static batching

For static batching, each thread block simply fetches a fixed number of indices from the input buffer to process. As a guideline for efficient processing, we use a common multiple of the block size and the primitive size as batch size, e.g., for triangles and thread block size 32, we could use any multiple of $3 \times 32 = 96$. Since the batch size is fixed, static batching requires no preprocessing of the index buffer and can be applied directly to the input of a streaming pipeline.

Statically batched naive. As a baseline, we implement a naive strategy that does not attempt any vertex reuse. Instead, every thread is directly assigned to a primitive, and invokes the vertex shader for all its indices. As thread blocks always fetch the same number of indices, the static batch size is implicitly given. Notice that, while this strategy leads to duplicate vertex shader execution, it avoids all communication overhead. Thus, for very simple vertex shaders, this naive approach may in fact show very good performance.

Statically batched warp voting. For this strategy, we aim to fill up warps with triangles so that every thread receives a unique vertex to work on, as outlined in Figure 4. For this purpose, we use fast, warp-level communication mechanisms, as detailed in Algorithm 1. Every thread first loads an index from the buffer and subsequently publishes it via register shuffle instructions to all other threads in the warp. Each thread then informs its peers via warp voting whether a duplicate index has been found. We track the number of unique indices observed so far and assign each new index to the available thread with the lowest ID. We also maintain an inverse lookup-table in shared memory for fast reassembly after shading.

We keep fetching indices until either all threads were assigned a unique vertex, or the batch boundary is hit. Next, all identified
unique vertices are shaded and output assembly is carried out. This process is repeated iteratively, until all indices in the batch have been processed. Note that starting a new iteration can lead to duplicate shader invocation inside a batch, since shading results are not carried over from the previous iteration. To distribute the shaded vertices within the warp, we again use shuffle instructions.

3.4 Dynamic batching

We assess the potential for optimizing vertex processing by allowing for a fast, low-impact preprocessing step to retrieve analytical data from the submitted index buffer. Specifically, we investigate the performance of several dynamic batching strategies, which rely on a load-time analysis of the input to derive optimal batch sizes. This routine splits the buffer into batches of variable length, with the goal of maximizing thread occupancy at runtime for the loading and processing of vertices.

To achieve this, we define \( N \) to be a multiple of the block size and scan the triangles in the index buffer front to back, counting unique indices until we reach \( N \), or a maximum allowed number of primitives has been added to the batch. As soon as either of these conditions is met, we start a new batch and continue scanning the index buffer until all indices have been assigned to their respective batches. The batch starting positions, stored in an auxiliary buffer, allow us to feed a close-to-ideal amount of data to each thread block.

Note that we do not require the buffer to forward information about the unique vertices, and leave their identification to be conducted by threads at runtime. Hence, no information other than the splitting of the index buffer into optimally processable portions is output at this point. Therefore, we can abstract our preprocessing procedure to an elaborate work scheduling routine, that could very well be realized by dedicated hardware. We propose three distinct strategies for the dynamic approach: dynamically batched sorting, dynamically batched hashing, dynamically batched parallel hashing.

**Algorithm 1: Statically batched warp voting.**

```plaintext
1 shared map[ ]
2 cStart ← BatchBegin
3 while cStart < BatchEnd do
4 fill ← 0, done ← 0, my_id ← −1, offset ← cStart
5 while offset < BatchEnd and fill < WarpSize do
6 incoming ← −1, outgoing ← −1
7 if offset + laneld < BatchEnd then
8 incoming ← indexBuffer[offset + laneld]
9 for i ∈ WarpSize do
10 current ← shfl(incoming, i)
11 match ← ballot(current = my_id)
12 if match = 0 then
13 if fill = laneld then
14 my_id = current
15 match ← BitShift(1, fill)
16 fill ← fill + 1
17 if i = laneld then
18 outgoing ← match
19 map[done + laneld] ← ffs(outgoing)−1
20 firstmask ← ballot(outgoing = 0 or incoming = −1)
21 additional ← min(WarpSize, ffs(firstmask)
22 done ← done + additional
23 offset ← offset + WarpSize
24 triangles ← [done/3]
25 if laneld < fill then
26 v ← shade(vertexBuffer[my_id])
27 v0 ← shfl(v, map[3 − laneld])
28 v1 ← shfl(v, map[3 − laneld + 1])
29 v2 ← shfl(v, map[3 − laneld + 2])
30 if laneld < triangles then
31 output(v0, v1, v2)
32 cStart ← 3 · triangles
```
Algorithm 2: Dynamically batched sorting.

```plaintext
shared ids[], linIds[], map[], marks[], uniquelds[], v[]
for i ∈ size(Batch) do in parallel
    ids[i] ← indexBuffer[BatchBegin + i]
    linIds[i] ← i
RadixSort (ids, linIds)
for i ∈ size(Batch) do in parallel
    marks[i] ← 1 if ids[i] ≠ ids[i + 1] else 0
numVertices ← PrefixSum (marks)
for i ∈ size(Batch) do in parallel
    map[linIds[i]] ← marks[i]
    uniquelds[marks[i]] ← id[i]
for j ∈ numVertices do in parallel
    v[j] ← shade (vertexBuffer[uniquelds[j]])
for i ∈ size(Batch)/3 do in parallel
    output (v[map[3i]], v[map[3i + 1]], v[map[3i + 2]])
```

Dynamically batched hashing. In this strategy, we employ a hash map in shared memory to remove duplicate vertex indices. As hash function, we use multiplicative hashing with linear probing. We choose the size of the hash map to match the thread block size. Ideally, the hash map is fully filled after loading a batch due to the size restrictions applied in our preprocessing step. Consequently, filling the hash map allows us to uniquely assign vertices to threads. Upon entering an index into the hash map, the loading thread records the value of the hash function, to be identify the required vertex after shading. Since the hash map is filled in parallel, we use atomic operations for insertion, as outlined in Algorithm 3 and Figure 6.

Algorithm 3: Dynamically batched hashing.

```plaintext
shared hashtable[], map[], v[]
for i ∈ BatchSize do in parallel
    hashtable[i] ← -1
for i ∈ size(Batch) do in parallel
    id ← indexBuffer[BatchBegin + i]
    p ← hash (id)
while not inserted do
    prev ← atomicCAS (hashtable[i], -1, id)
    if prev = -1 or prev = id then
        loc ← p
    else
        p ← probing (p)
    map[i] = loc;
for j ∈ BatchSize do in parallel
    if hashtable[j] ≠ -1 then
        v[j] ← shade (vertexBuffer[hashtable[j]])
for i ∈ size(Batch)/3 do in parallel
    output (v[map[3i]], v[map[3i + 1]], v[map[3i + 2]])
```

Dynamically batched parallel hashing. One issue with the simple hashing approach above is, that a fully occupied hash map will likely lead to excessive linear probing. In some cases, this may lead to pathological warp divergence, as a single thread repeatedly tries to find the last free entry, and the remaining peers in the warp have to join in the effort. As a remedy, we propose to perform hashing as a two-tiered approach. First, every thread executes up to a fixed number of linear probing attempts. Second, all threads within a warp collaboratively collaborate to find available spots until all indices have been inserted. This fast-path/slow-path strategy effectively repurposes otherwise idle threads in order to speed up the
We first determine the ideal reuse rate as the ratio of duplicate vertex multi-processors, where each multi-processor runs 1024 vertex of our main evaluation GPU, the NVIDIA GTX 1080Ti, we simulate the cache for that vertex just after, it may still result in a cache miss, completes a vertex shader invocation and another threads queries e.g. potential of being utilized. The problem gets even worse considering threads may execute in parallel, precluding an immense vertex reuse, shader execution, all threads that concurrently receive the same non-cached index to execute, will not be captured by the cache. Furthermore, as cache entries can only be generated after vertex processing stage of a real-time 3D rendering pipeline. To test our approaches throughout the evaluation of use-case scenarios.

4.2 Rasterization
The major motivation and use case for vertex reuse is the geometry processing stage of a real-time 3D rendering pipeline. To test our batch-based reuse techniques, we have implemented a configurable

4 EVALUATION
For performance evaluation, we use a set of commonly processed models, as well as content captured from five recent video games and an NVIDIA technical demo: Age of Mythology (abbreviated am), Assassin’s Creed: Black Flag (as), Deus Ex: Human Revolution (dx), Stone Giant animation (sg), Total War: Shogun 2 (sh), Rise of the Tomb Raider (tr), and The Witcher 3 (tw). A representative rendering from our 19 different scenes is shown in Figure 1b.

Obviously, evaluating the effectiveness of different vertex reuse methods is meaningful only if the processed data actually allows for detecting reuse. As this is usually not considered in the generation, formatting or conversion of mesh data, the order in which vertices are referenced in input models can be at best arbitrary, or, at worst, biased. Popular mesh processing algorithms have been presented previously, with the aim of reordering indices in a given mesh to increase vertex locality. As shown by Figures 7 and 8, applying such algorithms to popular models can remove unusual discontinuities, and significantly improve reuse potential in the OpenGL streaming pipeline. Incidentally, this is also true for our own techniques, which appear to exhibit similar behavior to OpenGL. In order to generate a fair ordering and enable vertex reuse even in unstructured models, we preprocess all meshes with the optimization algorithm by Forsyth (2006).

For comparison, we simulate a parallel caching scheme with different cache sizes and compare performance to our static and dynamic batching approaches. Furthermore, we investigate performance of our techniques when using them in a software streaming rendering pipeline and compare to a non-streaming, multi-kernel setup.

4.1 Caching vs batching and OpenGL
We first determine the ideal reuse rate as the ratio of duplicate vertex indices over the total length of the index buffer. Theoretically, a very large, global post-transform cache with instant reusability could yield the reported ideal figures. Unfortunately, such a global vertex cache does not seem practical for massively parallel devices, like modern GPUs. Storing and retrieving data from device-wide caches introduces an order of magnitude higher latency than caches on multi-processors, effectively reducing performance significantly. Furthermore, as cache entries can only be generated after vertex shader execution, all threads that concurrently receive the same non-cached index to execute, will not be captured by the cache. On a massively parallel device, like the GPU, tens of thousands of threads may execute in parallel, precluding an immense vertex reuse potential of being utilized. The problem gets even worse considering the long latency of a device-wide cache, e.g., even if one thread completes a vertex shader invocation and another threads queries the cache for that vertex just after, it may still result in a cache miss, as the latency for storing the shading result has not yet elapsed.

In order to compare to a more realistic cache-based approach, we simulate a per-multi-processor cache setup. Based on the design of our main evaluation GPU, the NVIDIA GTX 1080Ti, we simulate 28 multi-processors, where each multi-processor runs 1024 vertex shader invocations in parallel and stores the results in its dedicated least-recently-used (LRU) cache of size 16, 32, or 64KB. As mentioned before, a cache hit cannot occur for duplicate vertices being concurrently processed, but only if the result was already produced in an earlier shading cycle. For our statically batched warp voting, we use a batch size of 96, which fits the warp size of 32. For all dynamic batching approaches, we use a maximum batch size of 1023 indices and 256 unique vertices, and assign 256 threads to each batch. Test scene statistics and achieved reuse for each technique are listed in Table 1.

The recorded reuse rates of these cache-based techniques is always below \( \frac{1}{4} \) of the ideal reuse rate. In contrast, our dynamic batching usually falls within 5% of the ideal reuse, and statically batched warp voting within 10–20%. In general, both static and dynamic batching seem to be highly effective for all kinds of scenes.

The sum of these observations strengthens our assumption that the herein presented approaches may be better suited for modern architectures than a post transformation cache. Furthermore, our tests with implementing a post-transform cache, quickly lead us to believe that there is no efficient way of implementing such a cache in software. Thus, we solely focus on the presented batch-based approaches throughout the evaluation of use-case scenarios.

4.2 Rasterization
The major motivation and use case for vertex reuse is the geometry processing stage of a real-time 3D rendering pipeline. To test our batch-based reuse techniques, we have implemented a configurable
geometry stage in CUDA, that can be included into a streaming pipeline design. The geometry processing stage is simply given an input stream of indices and a vertex buffer. Based on the respective batching approach, indices are fetched from the index buffer and vertex reuse is evaluated. As a final step, one thread per triangle is used to write the output primitive with its vertices into a queue. This output queue could—when integrated into a full streaming pipeline—be consumed by the next stage in the rendering pipeline.

For a traditional real-time rendering pipeline, this queue would form the natural point for a sort middle approach.

The runtime results for the vertex processing for selected tested techniques on an NVIDIA GTX 1080 Ti are shown in Table 2. To simulate different vertex shader loads, we used a simple matrix multiplication (simple), a load of 256, 512 and 1024 cycles; for comparison, a cached access to L1 takes about 20 cycles, to L2 about 200. We also include a non-streaming, multi-staged processing implementation for reference. With this approach, all vertices in the vertex buffer are processed only once by separate kernel. The output vertex data can then be directly loaded from global memory in a separate kernel for assembling the output primitives. This approach is employed, e.g., by Laine and Karras (2011) for rasterization of 3D scenes. Since vertices need to be shaded exactly once, this technique can achieve ideal reuse, but only at the cost of sacrificing the advantages of a streaming architecture. For instance, unreferenced vertices are shaded in this approach regardless of their relevance to the scene. This can exact a significant performance penalty if, e.g., one large vertex buffer is used in combination with multiple index buffers to draw relevant portions on demand. Although this is not the case in our test scenes, our vertex reuse techniques can even outperform multi-staged geometry processing on several accounts. The full data set we produced for evaluating reuse in our software renderer can be found in the accompanying supplemental material for this paper.

As can be seen, for a very simple vertex shader, the naïve, no-reuse approach is the fastest, as it has no communication overhead. However, warp voting and sorting are on average only about 1.5× slower, and both hashing approaches are about 2.0× behind. The
Table 2: Processing times achieved with different vertex reuse techniques for rendering of geometry on a GTX 1080 Ti. We also include a non-streaming, multi-kernel technique (multi) for comparison.

|                  | sph | tree | dra | bud | as01 | dx33 | sg14 | sh11 | tr04 | tw03 |
|------------------|-----|------|-----|-----|------|------|------|------|------|------|
| naïve            | 0.07| 0.34 | 4.59| 0.81| 0.14| 0.05| 0.19| 0.83| 0.21| 0.35 |
| warp             | 0.13| 0.40 | 10.38| 1.69| 0.24| 0.11| 0.34| 1.39| 0.36| 0.61 |
| hash             | 0.16| 0.42 | 12.89| 2.05| 0.27| 0.12| 0.46| 1.47| 0.40| 0.74 |
| phash            | 0.13| 0.41 | 11.00| 1.82| 0.23| 0.10| 0.39| 1.32| 0.35| 0.65 |
| sort             | 0.20| 0.51 | 6.36 | 1.21| 0.31| 0.13| 0.41| 1.18| 0.34| 0.61 |
| multi            | 0.10| 0.38 | 6.24 | 1.02| 0.19| 0.08| 0.26| 1.09| 0.30| 0.47 |

Table 3: Runtimes for parallel Loop subdivision, executing on three of our input models, with different reuse methods, given in ms. Our techniques achieve up to %22 speed-up for happy_buddha over naïve streaming.

|                  | naïve | warp | hash | p.hash | sort |
|------------------|-------|------|------|--------|------|
| bunny            | 0.70  | 0.58 | 0.58 | 0.59   | 0.57 |
| sphere           | 0.79  | 0.68 | 0.68 | 0.69   | 0.64 |
| happy_buddha     | 11.10 | 8.50 | 8.15 | 8.17   | 8.61 |

This result indicates to us that, among the techniques capable of vertex reuse, warp voting has the lowest overhead.

As the vertex shader load increases, the naïve approach quickly falls behind, indicating that the proposed approaches can efficiently detect vertex reuse. For a 256 cycle load, warp-voting achieves the best performance, followed by parallel-hashing and hashing. For this load, the lower overhead of warp-voting still outweighs its lower vertex reuse rate. However, for larger loads the two hashing approaches catch up, and performance is overall tied between the our three techniques, while sorting eventually trails behind. We attribute the high performance of both hashing approaches and their marginal difference to the efficient implementation of shared memory atomics on recent GPUs.

To assess the performance of the proposed approach across multiple GPU generations, we also tested an NVIDIA GTX 780 Ti, 980 Ti and report the relative execution time compared to naïve, averaged over the entire test body in Figure 9. As can be seen, there is a significant difference across GPU generations, which is mostly due to more efficient shared memory operations. While for a simple shader, all vertex reuse approaches reduce performance in comparison to naïve, the more complex shaders again benefit greatly from reuse. Although statically batched warp voting again slightly loses ground in comparison to the other approaches on the GTX 1080 Ti in the complex case, it outperforms the other approaches on average over all GPUs. Additionally, statically batched warp voting does not require analysis of the index buffer and thus can be used in a full streaming approach.

5 SOFTWARE APPLICATIONS

In addition to their respective impact to rendering performance, we also evaluate our techniques for its potential in context of general, software-based processing tasks that allow for reuse. Specifically, we consider them for mesh subdivision and morphological transformation for inner and outer envelopes on 2-manifold models. Furthermore, we run a random walk simulation based on probabilistic input parameters. All applications were implemented in CUDA and executed on an NVIDIA GTX 1080 Ti.

5.1 Mesh Subdivision

Subdivision of low-detail meshes can be achieved by adding primitives to mesh, based on the adjacency information of its vertices. The particular steps to take, as well as orientations of the newly introduced triangles are determined by analyzing their topological neighborhood. An easily parallelizable subdivision algorithm has been presented in [Loop 1987]. Loop subdivision produces a piece-wise linear approximation of smooth surfaces based on B-spline and multivariate spline theory. For each edge and vertex, vertices are added in each subdivision iteration. The position of new vertices is computed from a convex combination of the adjacent primitives. Considering vertex reuse, allows the merging of these memory accesses. Figure 10 shows results for subdividing a simplified version of the original buddha statue in this way. We ran one iteration of the Loop subdivision with different vertex reuse strategies on the bunny, sphere, and happy_buddha models.

We evaluated a wide variety of different parameters for batch and thread block size, and chose those producing the best results for our final consideration. For naïve and warp, a batch size of 96 was used, with a block size of precisely one and two warps, respectively. For both hash and p.hash, we chose batches containing up to 192 indices and 64 threads per block. Note that, for the dynamic methods, the thread block size also equals the maximum allowed number of unique indices allowed in a batch. For sort, best results were achieved at a batch size of 768, with a block size of 256 threads. The Loop subdivision algorithm is arguably quite simple, and hence the cost of re-shading vertices comparatively inexpensive. However, the reduction in runtime with our vertex reuse techniques can still be as high as 26%. Without exception, all vertex reuse techniques outperform the naïve approach for the tested scenes (see Table 3).
Figure 9: Reported runtimes of the vertex processing stage in our software renderer, averaged over the entire test body (19 original scenes) and plotted relative to naïve. Different GPU architectures behave quite diversely: note the poor performance of hash, compared to our optimization p.hash on older architectures (GTX 780 Ti). Overall, statically batched warp voting seems to be the most reliable approach.

Figure 10: Running Loop subdivision on a simplified buddha with vertex streaming. The smoother, subdivided output is shown in the lower right.

5.2 Simplification Envelopes

The inner/outer envelopes of a mesh are defined to occupy a strict spatial sub-/superset of the input. Resulting meshes can be used, e.g., as input to a variety of simplification algorithms, manipulation of subdivision or for conservative intersection/collision testing with tolerance [Cohen et al. 1996; Zhou et al. 2007]. An envelope is obtained by moving vertices along their vertex normal towards the inside or the outside of the model. Provided that the original mesh does not contain self-intersections, an inner or outer envelope must also retain this property. Hence, before moving each vertex, we need to determine a safe distance  \( \epsilon \) to ensure that no intersections will occur as a result of its transformation. We have implemented the analytical approach presented by Cohen et al. and ported it for parallel execution in CUDA (1996). Potential intersections are identified and resolved efficiently by providing an octree representation of the scene as auxiliary input. Inner and outer envelopes for the bunny model are shown in Figure 1c.

We configured our routine to generate outer envelopes with a target  \( \epsilon \) equal to 2% of the mesh’s bounding box diagonal. We again report results with the best configuration found for each technique to yield consistently good results. As with subdivision, batch/block sizes for naïve and warp were chosen as 96/32 and 96/64, respectively. For all dynamic methods, we found that a block size of 128 works best. For hash, we picked a batch size of 576.

|       | naïve | warp | hash  | p.hash | sort  |
|-------|-------|------|-------|--------|-------|
| bunny | 71.73 | 29.41| 22.21 | 21.74  | 21.85 |
| sphere| 15.08 | 5.55 | 4.02  | 4.03   | 4.03  |
| buddha| 5021.80| 2112.45| 1595.31| 1516.15| 1509.76|

Table 4: Runtimes for parallel envelope creation, given in ms. Due to the particularly high shader cost, models with good vertex reuse (sphere) can achieve 3× the performance obtained with naïve streaming alternatives.
indices, and used 768 indices for both p.hash and sort. The envelope creation routine is comparably complex, and the incurred cost for each "shaded" vertex in the creation of envelopes is high: computing an intersection-free offset for a vertex to move by requires traversing a spatial data structure, which has to be stored in global memory. Similarly to our experiments for rendering with high shader loads, a speed-up of more than 3x can be achieved over naive streaming. Table 4 lists reported runtimes in milliseconds for processing 2-manifold models.

5.3 Parallel Random Walk

A random walk [Pearson 1905] describes a stochastic or random process, where a path is chosen on top of a graph structure or given domain, based on successive randomized steps. Random walks are used, e.g., to simulate the paths of molecules traveling through liquids, the random search path of animals, or messages traversing through a social network.

To evaluate whether on-the-fly reuse computations can increase the performance of such random processes, we implemented a parallel walk on a discrete domain that follows a Levy flight [Kleinberg 2000]. We use a grid size of 256 × 256 and place 300,000 agents on this grid. To simulate their activity, we overlay multiple Gaussian functions on this domain. The likelihood for agents to move a certain distance is then computed based on the activity input to the Fokker–Planck equation. To evaluate the movements, we run through all potential moves with a maximum distance of 16 and keep only those 8 with the highest likelihood. Then, every agent draws a random number to choose one of the stored options, whereas each is chosen with a probability proportional to their relative likelihood.

Reuse can be implemented in this scenario as follows. We encode the current agent location as a combined integer, using half of the bits for each dimension, yielding a single 32-bit word. This number serves as a virtual “index” for the reuse computations, combining agents that are currently placed on the same grid location. Given that the movement probability only depends on the current position, all agents with combined “indices” will see identical movement likelihoods, which can be computed only once. The final step, which involves drawing a random number and choosing the most likely move, has to be carried out separately.

Initializing all 300,000 agents randomly and running 10 simulation steps on the 256 × 256 showed that our reuse strategies can significantly increase the performance of the parallel random walk. Naive, warp, hash, p.hash, and sort, respectively, took 0.30 ms, 0.10 ms, 0.09 ms, 0.13 ms and 0.10 ms for one time step in their best configurations. The batch sizes that achieved the best performance were rather large (1536 for dynamic batching and 576 for static batching). At first glance, the great performance of reuse is not surprising, as the likelihood computations are rather time complex, and a high benefit can be expected for expensive vertex shaders. However, note that the agents are also likely to significantly diverge throughout the random walk. A further analysis revealed that a small amount of reuse already entails a significant performance gain, as the large batch sizes can still reduce the computations.

6 CONCLUSION

While the traditional solution to vertex reuse is represented by the post-transform vertex cache, caching seems to be less applicable for modern, massively parallel devices. Our simulations have shown that, even under ideal conditions, cache miss rates in a distributed environment commonly exceed 90%. We have presented four inheritently parallel, batch-based approaches, providing a suitable alternative to conventional caching. Our methods are straightforward to realize in software or hardware, and operate directly on the input buffers for indexed triangle meshes, with little to no pre-processing required. Especially for complex shading routines, we showed that batching can achieve high reuse and increase performance by up to 3x over non-reuse approaches. We have evaluated both static and dynamic batching methods on a variety of applications and test cases. Due to its use of fast, warp-level communication, our static warp-voting technique is well-suited for basic shading tasks, while a dynamic, hashing-based batching approach usually performs best at high shader complexity. Considering that vertex shaders often exhibit low-to-medium complexity and absence of a required preprocessing step, warp-voting appears to be the recommended choice for streaming pipelines written in a compute language.

Our results are obtained from simulations and applications in CUDA, but similar approaches are straightforward to implement in hardware, where communication primitives can be set up even more efficiently. As vertex reuse needs to interface with vertex shading, batch sizes and efficiency considerations for warp-based execution are certainly transferable into a hardware design. Furthermore, data reuse considerations are not only applicable to rendering, but also to general mesh processing and parallel graph traversal problems, where node dependencies require a similar treatment. We hope that our implementation will help other researchers kick off the conception of novel software rendering pipelines. Our source code is publicly available at [link removed for review].

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