Performance Evaluation of Epitaxial Layer Based Gate Modulated TFET (GM-TFET)

Rajesh Saha (rajeshsaha93@gmail.com)
Malaviya National Institute of Technology Jaipur  https://orcid.org/0000-0003-3108-6081

Rupam Goswami
Tezpur University

Brinda Bhowmick
National Institute of Technology Silchar

Srimanta Baishya
National Institute of Technology Silchar

Research Article

Keywords: Electrical Characteristics, Epitaxial layer, Gate Modulated TFET, TFET, TCAD.

Posted Date: July 27th, 2021

DOI: https://doi.org/10.21203/rs.rs-732664/v1

License: This work is licensed under a Creative Commons Attribution 4.0 International License.
Read Full License
Performance Evaluation of Epitaxial Layer Based Gate Modulated TFET (GM-TFET)

Rajesh Saha\textsuperscript{1*}, Rupam Goswami\textsuperscript{2}, Brinda Bhowmick\textsuperscript{3}, Srimanta Baishya\textsuperscript{4}

\textsuperscript{1}\textsuperscript{*}Department of ECE, Malaviya National Institute of Technology Jaipur, Jaipur 302017, Rajasthan, India.
\textsuperscript{2}School of Electronics, Tezpur University, Napaam, Tezpur 784028, Assam India.
\textsuperscript{3,4}Department of ECE, National Institute of Technology Silchar, Silchar 788010, Assam, India.
\textsuperscript{1}\textsuperscript{*}rajeshsaha93@gmail.com, \textsuperscript{2}rup.gos@gmail.com, \textsuperscript{3}brindabhowmick@gmail.com, \textsuperscript{4}s.baishya@yahoo.co.in

Abstract: This paper reports the performance of an epitaxial layer (ETL) based gate modulated (GM-TFET) through 3D Technology Computer Aided Design (TCAD) simulations. The architecture utilizes effects of both vertical tunneling and lateral tunneling phenomena to improve the device performance. Attributes of the ETL, its thickness \((t_{\text{epi}})\) and doping concentration \((N_{\text{epi}})\) are varied and their impact on device electrical parameters such as transfer characteristic, output performance, subthreshold swing (SS), and threshold voltage \((V_{T})\) is highlighted. It is observed that both \(t_{\text{epi}}\) and \(N_{\text{epi}}\) significantly influence the different electrical parameters of the ETL based TFET architecture.

Keywords— Electrical Characteristics, Epitaxial layer, Gate Modulated TFET, TFET, TCAD.

1. Introduction

Over the year, extensive research is carried out to control the various restrictions of short channel effects (SCEs) of MOSFET [1]. In this aspect, novel devices with different operation mechanism is proposed in the literature. Tunnel Field Effect Transistor (TFET) which operates on band to band tunneling (BTBT) mechanism instead of thermionic emission and it has subthreshold swing (SS) below 60 mV/dec. at 300 K [2-3]. One of the foremost disadvantage of TFET is its low ON state current [4-5]. Various research have been presented through structural engineering to enhanced the ON current of TFET like silicon on insulator (SOI) TFET [6], heterojunction TFET (HJ-TFET) [7], circular gate TFET (CG-TFET) [8], double gate (DG) TFET [9], dual material gate (DMG) TFET [10] and many more. Also, epitaxial layer (ETL) based TFET architecture is proposed to make TFET suitable for low power applications [11-12]. The gate overlapped on the source and drain regions is one popular approach to enhance the performance of TFETs with high tunneling at ON state [13]. Furthermore, source pocket doped with line tunneling TFET has been highlighted to improve the conduction of TFET [14]. The ETL based TFET provide the vertical tunneling along with lateral tunneling, which improves the tunneling probability and enhanced the ON current [15]. Such ETL based TFET is a potential candidate to boost the performance of TFET. A gate modulated (GM)-TFET having ETL with improved ON current for the variation in gate and drain bias is reported [16]. The source/drain lateral straggle \((\sigma)\) influence on analog and high frequency performance of GM-TFET is investigated in literature
Also, the linearity performance of GM-TFET for the variation of σ parameter is highlighted [16]. However, the performance of GM-TFET is not evaluated for various ETL thickness and doping concentration of the ETL.

In this work, the effect of ETL thickness (tepi) on transfer characteristic, output characteristic, SS and threshold voltage (VT) of GM-TFET is reported at fixed value of doping concentration of the ETL (Nepi) through Technology Computer Aided Design (TCAD) device simulator. We also highlighted the effect of Nepi on these electrical parameters of GM-TFET at fixed value of tepi.

The organization of the paper is as follows: Section II describes the device architecture along with simulation methodology. Section III provides the simulation results obtained from simulator and the same is discussed here. This work is summarized in Section IV.

2. Device structure and Simulation descriptions

The 2D representation of the GM-TFET with ETL is shown in Fig. 1. The epitaxial layer of the ETL GM-TFET is placed over the source and channel portions i.e. under the gate dielectric layer. In conventional TFET structure only lateral tunneling is present at tunnel junction perpendicular to gate field. In ETL GM-TFET, the vertical tunneling along with lateral tunneling improves the conduction mechanism of TFET [14]. Here, source, drain, channel as well as the epitaxial layer (ETL) is made of Silicon. SiO$_2$ having dielectric constant of 3.9 is taken as buried oxide, whereas, HfO$_2$ having dielectric constant of 22 is considered as gate dielectric. Metal having work function ($\phi_M$) = 4.02 eV is taken as gate material. The uniform doping concentration is considered for all regions. The $p^+$ source doping concentration of ($N_S$) = $10^{20}$ cm$^{-3}$ is considered as greater than $n^+$ drain doping concentration ($N_D$) = $5\times10^{18}$ cm$^{-3}$ to minimize the ambipolar
current [18]. The intrinsic channel has doping concentration \( N_{\text{ch}} = 10^{15} \text{ cm}^{-3} \), whereas, doping of epitaxial layer \( N_{\text{epi}} \) is varied, otherwise mentioned. The various dimensions of the parameters as shown in Fig. 1 are listed in Table 1.

### TABLE I

| Parameter                  | Value (nm) |
|----------------------------|------------|
| Length of source region (\( L_{S1} \)) | 75         |
| Length of intrinsic region (\( L_{\text{int}} \)) | 25         |
| Length of drain region (\( L_{D} \)) | 30         |
| Length of gate region (\( L_{G} \)) | 100        |
| Silicon layer thickness (\( t_{\text{Si}} \)) | 20         |
| Height of BOX (\( t_{\text{box}} \)) | 145        |
| Height of bulk (\( t_{\text{bulk}} \)) | 10         |
| Oxide thickness (\( t_{\text{ox}} \)) | 3          |
| Epitaxial layer thickness (\( t_{\text{epi}} \)) | varies    |

Sentaurus TCAD tool is used for the simulation of the device [20]. Masetti mobility model is considered to study impact of doping concentration on charge carriers and Fermi Dirac distribution is enabled due to presence of degenerate source/drain regions. As tunneling probability is dependent on energy bandgap and thus bandgap narrowing model is adopted. The recombination of the carriers is considered by enabling SRH model in simulator. The transport of the carriers in simulator is activated by considering non-local BTBT Kane’s model in simulator, which captures BTBT at the required junction. The experimentally calibrated fitting parameters of BTBT is chosen in simulator are: \( A_{\text{path}} = 1.63 \times 10^{14} \text{ cm}^{-3} \text{ s}^{-1} \), \( B_{\text{path}} = 1.47 \times 10^{7} \text{ V cm}^{-1} \), \( P_{\text{path1}} = 0.0567 \text{ eV} \) [21].

### 3. Results and Discussion

This section described the influence of epitaxial layer thickness \( t_{\text{epi}} \) and doping concentration of ETL \( N_{\text{epi}} \) on transfer characteristic, output characteristic, SS, and \( V_T \) of ETL based GM-TFET through device simulator. The drain to source bias \( V_{\text{DS}} \) = 0.5 V is taken. The threshold voltage reading is taken from simulator through maximum transconductance method.

#### 3.1 Influence of Epitaxial Layer Thickness \( t_{\text{epi}} \)

Here, the analysis is presented for \( t_{\text{epi}} = 4, 6, 8, \) and 10 nm at fixed \( N_{\text{epi}} = 10^{15} \text{ cm}^{-3} \).

The effect of \( t_{\text{epi}} \) on transfer characteristic by varying \( t_{\text{epi}} \) from 4 to 10 nm with step of 2 nm, while keeping all other dimensions fixed, in linear and log scale are presented in Figs. 2 (a) and
It is seen that ON current increases significantly, whereas, OFF current degrades insignificantly, with the decrease in $t_{\text{epi}}$. This improvement in ON current can be better explained from Fig. 3, where we have plotted eBTBT rate at source-channel junction for $V_G = 1.5$ V and $V_{DS} = 0.5$ V, taking $t_{\text{epi}}$ as parameter. It is perceived from Fig. 3 that the BTBT rate increases for lower value of $t_{\text{epi}}$ which signifies improvement on ON current of the device as summarized in Fig. 2(a).

The effect of $t_{\text{epi}}$ on output characteristic for $V_G = 0.5$ V, of ETL based GM-TFET is portrayed in Fig. 4. It is perceived (Fig. 3) that eBTBT rate rises with reduction in $t_{\text{epi}}$, which indicates carrier can easily flow from source to drain as $t_{\text{epi}}$ changed from 10 to 4 nm. Thus, the drain current saturation occurs at large $V_{DS}$ for high value of $t_{\text{epi}}$, whereas, for low value of $t_{\text{epi}}$ saturation occurs at low value $V_{DS}$.

The variation in SS and $V_T$ taking $t_{\text{epi}}$ as parameter is shown in Fig. 5. As the subthreshold characteristic improves with rise in $t_{\text{epi}}$, which leads to improvement in switching performance.
and accordingly, SS value decreases. The reduction in $t_{\text{epi}}$ increases ON current, which in turn reduces the threshold voltage to turn on the device.

![Graph showing the effect of $t_{\text{epi}}$ on output characteristic.](image)

Fig. 4. Effect of $t_{\text{epi}}$ on output characteristic.

![Graph showing the effect of $t_{\text{epi}}$ on SS and $V_T$.](image)

Fig. 5. Effect of $t_{\text{epi}}$ on SS and $V_T$.

### 3.2 Influence of Epitaxial Layer Doping Concentration ($N_{\text{epi}}$)

This section discussed the electrical parameters by changing $N_{\text{epi}}$ from $10^{15}$ to $10^{18}$ cm$^{-3}$ while keeping other design parameter constant at fixed $t_{\text{epi}} = 8$ nm.

![Graph showing the effect of $N_{\text{epi}}$ on transfer characteristic in gate voltage.](image)

(a)

![Graph showing the effect of $N_{\text{epi}}$ on transfer characteristic in drain current.](image)

(b)

Fig. 6. Effect of $N_{\text{epi}}$ on transfer characteristic in...
The influence of $N_{\text{epi}}$ on input characteristic in linear and log scale are presented in Figs. 6(a) and (b), respectively. It is seen that with increased $N_{\text{epi}}$, there is improvement in ON current as well as minute degradation in OFF current. As concentration of epitaxial layer increases, which enhanced the BTBT rate at tunnel junction and accordingly, improves the ON current.

The output performance as a function of $N_{\text{epi}}$ is portrayed in Fig. 7. It can be summarized that electrons can travel fast from source to drain regions with increased in $N_{\text{epi}}$, which indicates the drain current saturates at large drain bias as $N_{\text{epi}}$ is changed from $10^{15}$ to $10^{18}$ cm$^{-3}$.

$$\text{SS of MOSFET can be expressed as [22]:}$$

$$\text{SS} = \ln_{10} 10\left(\frac{\partial V_{GS}}{\partial \ln(n_m)}\right)$$  \hspace{1cm} (1)

The minimum concentration is expressed as

$$n_m = n_i^2/N_{\text{epi}} \exp\left(\frac{\phi_{S,\text{min}}}{\phi_i}\right)$$  \hspace{1cm} (2)

The inversion charge carriers $Q_{\text{inv}}$ of MOSFET is given by [23].
\[ Q_{\text{inv}} = \int_0^w \left( \frac{(qn_i)}{(N_{\text{epi}})} \right) \exp \left( \frac{\phi_{\text{s, min}}}{\phi_t} \right) dy \]  

where, \( n_i \) is the intrinsic concentration, \( q \) is the electronic charge, \( \phi_{\text{s, min}} \) is the minimum potential, and \( \phi_t \) is the thermal voltage. This \( Q_{\text{inv}} \) is related charge is directly related with the threshold voltage.

The influence of \( N_{\text{epi}} \) on both SS and \( V_T \) is summarized in Fig. 8. As OFF current of ETL based GM-TFET increases with rise in \( N_{\text{epi}} \), which degrade the corresponding SS value. It is examined also from (1) and (2), the SS is inversely related with \( N_{\text{epi}} \), which leads to degradation in SS value with increased \( N_{\text{epi}} \).

Also, less \( V_T \) is needed to make the device on with increased \( N_{\text{epi}} \) and this is primarily due to enhanced ON current with rise in \( N_{\text{epi}} \). It is also observed from (3) that \( Q_{\text{inv}} \) reduces with the increased in \( N_{\text{epi}} \) and this decreases the required gate bias to activate the channel.

### 4. Conclusion

We have elaborated the performance of ETL based GM-TFET for the variation of ETL thickness \( (t_{\text{epi}}) \) and doping concentration of ETL \( (N_{\text{epi}}) \). Simulation results reported that the increased in \( t_{\text{epi}} \) degrades the ON current and improves SS of GM-TFET. The roll-off in threshold voltage \( (V_T) \) is observed when \( t_{\text{epi}} \) decreases from 10 to 4 nm. Furthermore, the increase in \( N_{\text{epi}} \), enhanced the ON current, whereas, degrade the SS of GM-TFET. It is also analyzed that upto \( N_{\text{epi}} = 10^{17} \text{ cm}^{-3} \) the roll-off of \( V_T \) is lesser and when \( N_{\text{epi}} \) increases to \( 10^{18} \text{ cm}^{-3} \) the \( V_T \) falls by significant amount. The output current improves for low (high) values of \( t_{\text{epi}} \) \((N_{\text{epi}}) \) in GM-TFET. Therefore, lower value of \( t_{\text{epi}} \) with heavily doped ETL \( (N_{\text{epi}}) \) can boost the performance of GM-TFET.

**Ethics approval and Consent for Participate:** Not applicable as the manuscript does not contain any data from individual.

**Competing interests:** The authors declare that there is no conflict of interest.

**Funding:** This work is funded by Science & Engineering Research Board, Govt. of India (Sanction Reference. No. SRG/2019/000628).

**Author contributions:** The work and manuscript is written by Rajesh Saha and Rupam Goswami. The grammatical corrections and Figures in this paper have done by Brinda Bhowmick and Srimanta Baishya.
Acknowledgements: The authors acknowledge the funding by Science & Engineering Research Board, Govt. of India (Sanction Reference. No. SRG/2019/000628).

Compliance with ethical standards:

Disclosure of potential conflicts of interest: The authors declare that he has no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Research involving Human Participants and/or Animals: Not applicable

Informed consent: Not applicable

Consent for publication: Not Applicable

Availability of data and material: There is no any other data and material associated with this manuscript.

REFERENCES

[1] S. Chakraborty, A. Mallik, C. K. Sarkar and V. Ramgopal Rao, “Impact of Halo Doping on the Subthreshold Performance of Deep-Submicrometer CMOS Devices and Circuits for Ultralow Power Analog/Mixed-Signal Applications,” IEEE Trans. on Electron Devices 54 (2), 2007, pp. 241-248.

[2] W. Y. Choi, B.-G. Park, J.-D. Lee, and T.-J. K. Liu, “Tunneling field effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec,” IEEE Electron Device Lett. 28 (8), 2007, pp. 743–745.

[3] K. K. Bhuwalka, J. Schulze, and I. Eisele, “Scaling the vertical tunnel FET with tunnel bandgap modulation and gate workfunction engineering,” IEEE Trans. on Electron Devices 52 (5), 2005, pp. 909-917.

[4] K. Boucart and A. M. Ionescu, “Double-Gate Tunnel FET With High-κ Gate Dielectric,” IEEE Trans. on Electron Devices, 54 (7), 2007, pp. 1725-1733.

[5] S. O. Koswatta and M. S. Lundstrom, “Performance comparison between p-i-n tunneling transistors and conventional MOSFETs,” IEEE Trans. Electron Devices, 56 (3), 2009, pp. 456-465.

[6] S. Chander, B. Bhowmick, and S. Baishya, “Heterojunction fully depleted SOI-TFET with oxide/source overlap,” Superlattices and Microstructures 86, 2015, pp. 43–50.

[7] M. Fan, V.P. Hu, Y. Chen, C. Hsu, P. Su, and C. Chuang, “Investigation of Back gate-Biasing Effect for Ultrathin-Body III-V Heterojunction Tunnel FET,” IEEE Trans. Electron Devices 62, 2015, pp. 107-113.

[8] R. Goswami, B. Bhowmick, and S. Baishya, “Electrical noise in Circular Gate Tunnel FET in presence of interface traps,” Superlattices and Microstructures 86, 2015, pp. 342-354.

[9] L. Liu, D. Mohata, and S. Datta, “Scaling Length Theory of Double-Gate Interband Tunnel Field-Effect Transistors,” IEEE Trans. Electron Devices 59 (4), 2012, pp. 902–908.

[10] Sanjay Kumar, Ekta Goel, Kunal Singh, Balraj Singh, Prince Kumar Singh, Kamalaksha Baral, and Satyabrata Jit, “2-D Analytical Modeling of the Electrical Characteristics of Dual-Material Double-Gate TFETs With a SiO2/HfO2 Stacked Gate-Oxide Structure”, IEEE Trans. on Electron Devices 64, 2017, pp. 960-968.

[11] P. Y. Wang and B. Y. Tsui, “Epitaxial tunnel layer structure for P-channel tunnel FET improvement,” IEEE Trans. Electron Devices 60 (12), 2013, pp. 4098–4104.
[12] P. Y. Wang and B. Y. Tsui, “Epitaxial Tunnel Layer Structure for Complementary Tunnel FETs Enhancement,” In Proc. Int. Conf. SSDM, no. 1001, pp. 72-73, Sep. 2015. DOI: 10.7567/ssdm.

[13] S. Sant and A. Schenk, “Methods to Enhance the Performance of InGaAs/InP Heterojunction Tunnel FETs,” IEEE Trans. Electron Devices, vol. 63, no. 5, pp. 2169–2175, 2016. https://doi.org/10.1109/TED.2015.2489844.

[14] S. Blaeser, S. Glass, C. Schulte-Braucks, K. Narimani, NV. Driesch, S. Wirths, AT. Tiedemann, S. Trenlenkamp, D. Buca, QT. Zhao, S. Mantl, “Novel SiGe / Si line tunneling TFET with high I on at low V DD and constant SS,” IEEE Int. Electron Devices Meet., vol. 9, no. 2, pp. 22.3.1-22.3.4, Dec. 2015. https://doi.org/10.1109/IEDM.2015.7409757.

[15] P. Y. Wang and B. Y. Tsui, “Investigation into gate-to-source capacitance induced by highly efficient band-to-band tunneling in p-channel Ge epitaxial tunnel layer tunnel FET,” IEEE Trans. Electron Devices 63 (4), 2016, pp. 1788–1790.

[16] L. De Michielis, L. Lattanzio, P. Palestri, L. Selmi and A. M. Ionescu, “Tunnel-FET architecture with improved performance due to enhanced gate modulation of the tunneling barrier,” 69th Device Research Conference, Santa Barbara, CA, 2011, pp. 111-112. DOI: 10.1109/DRC.2011.5994440

[17] R. Saha, K Vanlalawmpuia, B. Bhowmick, and S. Baishya,"Deep Insight into DC, RF/Analog, and Digital Inverter Performance Due to Variation in Straggle Parameter for Gate Modulated TFET", Materials Science in Semiconductor Processing 91, 2019, pp. 102-107.

[18] R. Saha, B. Bhowmick, and S. Baishya, “Impact of lateral straggle on linearity performance in gate-modulated (GM) TFET”, Applied Physics A: Material Science and Processing, 126, 2020, pp. 201.

[19] N. N. Mojumder and K. Roy, “Band-to-Band Tunneling Ballistic Nanowire FET: Circuit-Compatible Device Modeling and Design of Ultra-Low-Power Digital Circuits and Memories,” IEEE Transactions on Electron Devices, 56 (10), 2009, pp. 2193-2201.

[20] TCAD Sentaurus User Guide, Synopsys Inc., Mountain View, CA, USA 2013.

[21] A Biswas, S. S. Dan, C. L. Royer, W. Grabinski, and A. M. Ionescu, “TCAD simulation of SOI TFETs and calibration of non-local band-to-band tunneling model,” Microelectronic Engineering 98, 2012, pp. 334–337.

[22] A. Tsormpatzoglou, C. A. Dimitriadis, R. Clerc, Q. Rafhay, G. Pananakakis, and G. Ghibaudo, “Semianalytical Modeling of Short-Channel Effects in Si and Ge Symmetrical double gate MOSFETs”, IEEE Trans. Electron Devices 54, 2007, pp. 1943-1951.

[23] H. A. E. Hamid, J. R. Guitart, and B. Iniguez, “Two dimensional Analytical threshold voltage and subthreshold swing Models of undoped symmetric Double-Gate MOSFETs,” IEEE Trans. Electron Devices 54, 2007, pp. 1402–1408.