An ultra-low power robust CMOS temperature sensor with an inaccuracy of ±0.7°C from −40°C to 85°C

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Abstract An ultra-low power robust CMOS temperature sensor is presented for RFID. The BJT-based sensor employs a calibrated hybrid ADC, which combines a coarse 5-bit SAR conversion with a fine 9-bit delta-sigma conversion. For the purpose of being robust, an error correction method is proposed in this paper, which can calibrate the SAR errors caused by power supply and mismatch. A smart clock generator is also proposed to adapt the change of PTAT bias current, which provides the integrators more settling time in low temperature with low bias current and makes the delta-sigma ADC faster in high temperature to reduce the error caused by leakage. The sensor has been implemented in a 130 nm CMOS process. After a one-point temperature trimming, the sensor has a resolution of 0.015 from −40°C to 85°C, and only consumes 10 µA from 1.5 V supply.

Keywords: ultra-low power, temperature sensor, smart clock generator, calibration

Classification: Integrated circuits

1. Introduction

Radio frequency identification (RFID) technology becomes popular in industrial control and internet of things in the last few years. And its market is still growing fast by integrating not only the circuit of identification and tracking, but also some smart sensors, [1, 2, 3, 4, 5].

For example, millions of voltage transformers used in power grid need to be equipped with temperature sensor with accuracy of ±1°C to protect itself from overload and overheating damages. The transformers always work in high temperature which may reduce battery life rapidly. With the advantage of small size and easy positioning, non-line-of-sight wireless operation, passive RFID tag with temperature sensor is a promising technology. To be cost-effective, these sensors should be fully CMOS circuit. Complex calibration process, i.e. multi-temperature calibration and trimming which need take several tens of seconds to do thermal calibration, must to be prevented. In addition, the power of temperature sensor should be as low as possible to make the communication distance longer.

In this work, a robust, low power, one-point trimming temperature sensor is presented. The system consists of a bipolar-based sensor, a calibrated hybrid analog to digital converter and its digital backend. With a low cost one-point trimming, it can achieve high accuracy. A redundancy algorithm and a smart clock generator circuit is proposed to improve the accuracy and reduce the power further. The circuit diagram of the temperature sensor is shown in Fig. 1. In the following sections, the detailed working principle and the test results will be discussed.

Fig. 1. The circuit diagram of the temperature sensor

2. BJT temperature sensor

It has been long recognized that the base-emitter voltage (VBE) has a negative temperature coefficient (TC), and the base-emitter voltage difference of two transistors biased at different current densities (ΔVBE) has a PTAT difference [6, 7, 8].

\[ V_{BE1} = \eta \cdot \left( \frac{kT}{q} \right) \cdot \ln \left( \frac{I_C}{I_S} \right) \quad (1) \]

where \( \eta \) is a process-dependent non-ideality factor (\( \eta \approx 1 \)); \( k \) is the Boltzmann constant; \( q \) is the electron charge; \( T \) is the temperature in Kelvin; \( I_C \) is the collector current and \( I_S \) is the PNP transistor saturation current.

If the current ratio is \( 1:p \), the difference of the base-emitter is

\[ \Delta V_{BE} = V_{BE2} - V_{BE1} = \eta \cdot \left( \frac{kT}{q} \right) \cdot \ln(p) \quad (2) \]

\( \Delta V_{BE} \) is more linear than \( V_{BE} \). Also \( \Delta V_{BE} \) is almost independent on process parameters.

\[ \mu = \frac{V_{PTAT}}{V_{REF}} = \frac{a \cdot \Delta V_{BE}}{V_{BE} + a \cdot \Delta V_{BE}} = \frac{a}{X + a} \quad (3) \]

\[ X = \frac{V_{BE}}{\Delta V_{BE}} \quad (4) \]

where \( a \) is factor which makes \( V_{REF} \) in Eq. (5) a lowest temperature coefficient.
\[ V_{\text{REF}} = V_{BE} + \alpha \cdot \Delta V_{BE} \]  

The ADC only needs to digitize the ratio \( X \) rather than generate a zero TC \( V_{\text{REF}} \) in analog domain. \( \mu \) can be computed in digital domain which is more robust than generating the \( V_{\text{REF}} \) in analog domain.

In practice, the non-linearity of \( V_{BE} \) may cause error up to 0.5°C. Increasing the value of \( \alpha \) can compensate the curvature of \( V_{BE} \), which makes the error function from parabolic curve to cubic curve and reduce the residual non-linearity [9]. The simulation result is shown in Fig. 2. \( \alpha 1 \) makes \( V_{\text{REF}} \) in Eq. (5) have the lowest 1st order temperature coefficient, \( \alpha 2 \) is larger than \( \alpha 1 \), which makes \( V_{\text{REF}} \) have a slight positive temperature coefficient. The error of \( \mu \) in Eq. (3) is decreased to 0.2°C by increasing \( \alpha \).

In CMOS process, the bias current only can be fed into the emitter rather than the collector of the bipolar because the collector must be connected to the ground. And the PNP bipolar in CMOS process shows low current gain \( \beta \) [10, 11, 12, 13].

The PTAT bias current makes the current gain \( \beta \) varies with changes of temperature which will impact on the accuracy of \( V_{BE} \).

\[ V_{BE} = \frac{kT}{q} \ln \left( \frac{I_c}{I_s} \right) = \frac{kT}{q} \ln \left( \frac{I_{\text{Bias}}}{I_s} \beta_E + 1 \right) \]  

The technique \( \beta \)-compensation mitigates this problem by generating a \( \beta \)-dependent current from a resistor of \( R/5 \) at the base terminal of QBR [6, 14] as shown in Fig. 3.

Chopper amplifier is used to eliminate the impact of offset. [15] The \( R_b \_\text{dummy} \) is added to make the layout of chopper amplifier unify [16]. Dynamic element matching is used for eliminate the mismatch of the current sources [17].

3. ADC design

3.1 Architecture design

\( X \) is a non-linear function of temperature as described in Fig. 4, implying a temperature-dependent resolution requirement [14]. At 125°C, the ADC requires the highest resolution, namely 13 bit, to make the target sensor resolution to be \( \pm 0.05^\circ \text{C} \).

A zoom ADC in [14] achieves advantages of high precision and high conversion speed by combining the strengths of both SAR ADC and \( \Delta \Sigma \) ADC, Fig. 5. The zoom ADC achieves similar accuracy while using 7x less energy than traditional temperature sensor based on \( \Delta \Sigma \) ADC [12, 14, 18, 19, 20]. However, the mismatch of feedback DAC, the noise in comparator and rapid temperature changing may result in incorrect coarse conversion value and overload in fine conversion, which produce a wrong temperature result. To make the sensor more robust, a self-calibrated hybrid ADC is presented, which relaxes the required accuracy of the coarse ADC by implementing a redundancy calibration algorithm. In this architecture, the result of fine ADC is used to check the coarse ADC, ensures that the zoom region is correct.

In the calibrated hybrid ADC, a SAR ADC digitizes the integer part of \( X \) first and the \( \Delta \Sigma \) converts the fractional one. SAR ADC is a coarse conversion, thus small CDAC is sufficient. And it can also decrease the resolution requirement of \( \Delta \Sigma \) ADC. Therefore, the oversampling rate can be reduced, and less energy is dissipated [14]. \( X \) ranges from 5.5 to 20 from \(-40^\circ \text{C} \) to \(125^\circ \text{C} \) in this design, Fig. 6, so a 5-bit SAR ADC makes the integer part conversion, a 9-bit \( \Delta \Sigma \) is implemented to make fine conversion and one bit for redundancy which is always necessary in hybrid ADCs. A sinc\(^2\) decimation filter is implemented to filter out the high-frequency noise of delta-sigma ADC and convert the bit stream to 9 bit data.

The 5-bit SAR ADC has big quantization errors and noise as well as DAC mismatch, which could result in incorrect \( n \) values. Then the \( \Delta \Sigma \) ADC will be set into a wrong region and overload. The calibrated hybrid ADC

![Fig. 2. Curvature of VBE simulated with different α](image)

![Fig. 3. Circuit of BIAS and sensor](image)

![Fig. 4. X and μ as a function of temperature](image)

![Fig. 5. Block diagram of the zoom-ADC](image)

![Fig. 6. Temperature dependence of X = n + m](image)
will have up to 1LSB of the coarse SAR ADC which may lead to a huge temperature error.

To avoid the error, an overlap technology named guard banding [14, 21, 22] is implemented by setting the full scale of the ΔΣ ADC to 2ΔVBE. Following the SAR ADC, VBE is compared to be changed from \( \text{contrast, if the } \frac{n}{C_1VBE} \) full range of \( \Delta \) scale of the \( \Delta \) banding \( \text{[14, 21, 22]} \) is implemented by setting the full lead to a huge temperature error. will have up to 1LSB of the coarse SAR ADC which may be chosen, but if it still touches the high alarm threshold, \( \Delta \) low alarm threshold and a high threshold. If the CIC output which makes the sensor more robust.

\[
\begin{align*}
&\text{Algorithm of guard banding} \\
&\text{In practice, the SAR ADC may still generate a wrong value of } n, \text{ caused by power noise, spikes in the circuit and rapid temperature changing. In the proposed design, a redundancy algorithm is implemented in digital backend, which makes the sensor more robust.}
\end{align*}
\]

\[
\begin{align*}
&\text{The proposed redundancy algorithm} \\
&\text{The idea is to compare the output of the CIC filter to a low alarm threshold and a high threshold. If the CIC output is greater than high threshold, then the } \Delta \Sigma \text{ ADC will convert again by setting the full scale from } (n - 1) \cdot \Delta VBE \sim (n + 1) \cdot \Delta VBE \text{ to } n \cdot \Delta VBE \sim (n + 2) \cdot \Delta VBE \text{ or from } n \cdot \Delta VBE \sim (n + 2) \cdot \Delta VBE \text{ to } (n + 1) \cdot \Delta VBE \sim (n + 3) \cdot \Delta VBE. \text{ If the output of the second conversion doesn’t touch any alarm threshold, the second result will be chosen, but if it still touches the high alarm threshold, the reference of } \Delta \Sigma \text{ ADC will be improved further, and if the low alarm is touched, the first result will be chosen. In contrast, if the first CIC output is smaller than the low alarm threshold, the feedback reference of } \Delta \Sigma \text{ ADC will be changed from } (n - 1) \cdot \Delta VBE \sim (n + 1) \cdot \Delta VBE \text{ to } (n - 2) \cdot \Delta VBE \sim (n - 1) \cdot \Delta VBE \text{ or from } n \cdot \Delta VBE \sim (n + 2) \cdot \Delta VBE \text{ to } (n - 1) \cdot \Delta VBE \sim (n + 1) \cdot \Delta VBE, \text{ as shown in Fig. 8.}
\end{align*}
\]

3.2 Circuit design
Fig. 9 shows the diagram of the 2nd-order \( \Delta \Sigma \) ADC. As the input signal of the ADC in \( \Delta \Sigma \) may be near full scale, a 2nd order \( \Delta \Sigma \) modulator is used to avoid overloading. The circuit level diagram of the zoom-ADC is described in Fig. 10. An array with 22, 260 fF unit capacitances acts as sampling capacitance and feedback DAC both in SAR period and \( \Delta \Sigma \) period. Each capacitor unit can samples \( \text{VBE} (\text{ck1d on first and ck2d.A on second, the positive one as example), } \Delta \text{VBE (ck1d on first and ck2d.B on second) or none (all switches are kept off) of which depends on the thermometer code generated by the logic.}

\[
\begin{align*}
&\text{The timing diagram of the calibrated hybrid ADC is shown in Fig. 11. During the SAR period, switch Sbp bypasses the second integrator and the first integrator works as a summing module and an amplifier. The first integrator sums VBE and } -n\Delta VBE \text{ together. One DAC cell is selected for sampling VBE and } n \text{ cells are selected to sample } \Delta VBE, \text{ thus, the voltage of the first integrator’s output is } (\text{VBE } - n\Delta VBE). \text{ The comparator will then judge whether the voltage is greater than zero or not.}
\end{align*}
\]

\[
\begin{align*}
&\text{Then the SAR logic makes the value approach to zero.}
&\text{DEC } = 16 + \sum_{i=0}^{5} \text{Di} \cdot 16 \div 2^i
\end{align*}
\]

\[
\begin{align*}
&\text{Di } = 1, \text{ if } bs = 1; \text{ Di } = 0, \text{ if } bs = 0;
&\text{Following the 5 SAR steps, } m \text{ which controls a half capacitor jump from 0 to 1 to test if the VBE is greater than } (n + 0.5) \cdot \Delta VBE \text{ or not. Based on the result of comparator, the full range of } \Delta \Sigma \text{ ADC is set to be } (n - 1) \cdot \Delta VBE \text{ to } (n + 1) \cdot \Delta VBE \text{ or } n \cdot \Delta VBE \text{ to } (n + 2) \cdot \Delta VBE. \text{ And the integer part } n \text{ is ready. Before the sigma-delta period, the smart clock generator circuit will tune its frequency based on the SAR result, which will be discussed in next section.}
&\text{During } \Delta \Sigma \text{ period, if the full range is } (n - 1) \cdot \Delta VBE \text{ to } (n + 1) \cdot \Delta VBE, \text{ one unit samples VBE, } (n - 2) \text{ units always sample } \Delta VBE \text{ and two units samples } \Delta VBE \text{ or 0 depends on bs. Sbp is always switched off.}
\end{align*}
\]
Both integrators are built with fully differential folded cascade OTA as shown in Fig. 12. The gain of the OTA is larger than 80 dB. The OTA used in the first integrator costs more area and power (5 µA) due to its critical noise and bandwidth constrain. The one in the second integrator uses the same architecture with less area and power (2 µA). SC-CMFB circuit is built in the OTA to prevent the differential gain from being decreased due to load effect.

![Schematic of the OTA used in integrator](image)

A sinc² digital filter [23] is implemented to convert the bit stream to a 9 bit data. The oversampling ratio is 1024, 2048 data need to be fed into the filter to produce m. Another digital circuit is implemented to calculate the final data [14].

\[
X = \frac{V_{BE}}{\Delta V_{BE}} = n + 2 \cdot m \\
\mu = \frac{\alpha}{X + \alpha}
\]  

(8)  

(9)

3.3 Smart clock generator

In the prototype in [14], the opamp in the integrators is the most power-hungry block in the ADC. To avoid noise leakage, the slew rate and gain-bandwidth (GBW) of the opamp in the switch-capacitor integrators should be large enough for setting accuracy. In the proposed architecture, a smart clock tuning circuit is implemented to relax the speed requirement of the opamps.

The opamps shares the bias circuit of the sensor in Fig. 2, so the bias current is a PTAT current. From −40°C to 85°C, the current has increased by 80%, as shown in Fig. 13.

When the SC integrator is switched, the opamp works in slew rate mode first. For a cascade opamp, the slew rate is show in Eq. (10) [24], \( I_{tail} \) is the current of tail current source of the input pair in Fig. 12. Thus in low temperature the slew rate is much slower.

\[
SR = \frac{I_{tail}}{C}
\]  

(10)

Then the opamp will work in GBW mode, for a one-pole opamp, the output voltage for a step input \( V_{in} \) is [25]

\[
V = V_{in}(1 - e^{-2\pi f GBW t})
\]

(11)

\[
GBW = \frac{g_m}{2\pi C}
\]

(12)

Where \( C \) is the load capacitor of the opamp, \( g_m \) is the transconductance of the input pair.

The sample capacitor of the first integrator is driven by the diode-connected bipolar QL and QR in the sensor shown in Fig. 3. When the voltage is sampled on a capacitor, the setting transient will be non-exponential [9]. The time constant is

\[
\tau = \frac{kT C}{I}
\]

(13)

Where \( C \) is the sample capacitor of the integrator in Fig. 10 and I is the bias current of the bipolar in Fig. 3.

The simulation result of the required time for opamp and diode-connected bipolar to settle on its own load within 60 µV to its final value is shown in Fig. 14.

![IBIAS and X as a function of temperature (orange line: X; blue line IBIAS)](image)

In other words, to guarantee the sigma-delta ADC accurate enough in the whole temperature range, the setting time requirement is temperature dependent, with a maximum value in −40°C. If the bias current is improved to meet the requirement in −40°C, the integrator has too much margin in 85°C, which wastes much power and can’t be acceptable in RFID whose power is very critical. Another way is to slow down the clock, however, in high temperature, most of the sample switches in Fig. 10 is open (X is small, so most switch is unused, discussed in section 3.2). If the clock period is too long, the leakage will cause large error, even make the sigma-delta ADC overload. Simulation result shows that the leakage of the switch in 85°C is 300x higher than that in −40°C. Which will be integrate by the integrator and lead to temperature error.

In this design, a smart clock generator (SCG) based on the SAR result is proposed. The smart clock tunes the frequency of the clock based on the coarse result of SAR ADC before the sigma-delta ADC begin. The architecture of the SCG circuit is shown in Fig. 15. A low power RC oscillator [26] provide the clock to the temperature sensor and ADC. The frequency of the clock is

\[
f = \frac{1}{2\pi \cdot RC}
\]

(14)

The capacitor in the OSC consists of an always on capacitor and a tunable capacitor. The clock period is shown in Fig. 14. If the temperature works in low temperature environment, the SAR ADC has a high value, the tunable capacitor will be added in the circuit to slow down the...
clock to leave more time for the integrator with low bias current. In contrast, if it works in high temperature, the result of the SAR ADC will be lower, the integrators have enough current for setting. The tunable capacitor will be removed and the clock will be speed up to reduce the effect of leakage.

4. Calibration

$\Delta V_{BE}$ is independent on process corner. The error caused by current source mismatch can be averaged out by applying DEM. However $V_{BE}$ has a PTAT process spread, which is related to doping concentration and junction depth [9].

\[ V_{BE} = \frac{kT}{q} \ln \left( \frac{I_C}{I_S + \Delta I_S} \right) \approx V_{BE,\Delta I_S=0} - \frac{kT}{q} \frac{\Delta I_S}{I_S} \]  
\[ (\Delta I_S \ll I_S) \]  
\[ (15) \]

\[ \mu = \frac{\alpha \cdot \Delta V_{BE}}{V_{BE,\text{ideal}} + \varepsilon + \alpha \cdot \Delta V_{BE}} \]  
\[ \varepsilon = \frac{-\Delta I_S}{I_S} \]  
\[ (16) \]

\[ \mu_{\text{ideal}} = \frac{\alpha \cdot \Delta V_{BE}}{V_{BE,\text{ideal}} + \alpha \cdot \Delta V_{BE}} \]  
\[ (17) \]

\[ \frac{1}{\mu} - \frac{1}{\mu_{\text{ideal}}} = \frac{q}{\alpha \cdot V_{BE,\text{ideal}}} = \gamma_D \]  
\[ (18) \]

The difference of the output is a temperature-independent variable $\gamma_D$. $\gamma_D$ can be selected as the trimming parameter.

A one point trimming method can be made in digital domain. $\gamma_D$ can be examined in production testing.

Where $u_{\text{ideal}}$ is the desired ratio at a well-defined calibration temperature, and $\mu$ is the test result of chip under testing at the same temperature.

This one-point trim method can decrease the cost of the chip my reducing the thermal trimming time.

\[ D_{\text{out}} = \Lambda \cdot \frac{\mu}{1 - \gamma_D \mu} - B \]  
\[ (19) \]

\[ \gamma_D = \frac{1}{\mu} - \frac{1}{\mu_{\text{ideal}}} \]  
\[ (20) \]

5. Measurement results

The temperature sensor was realized in a standard 0.13 µm CMOS process. The key parameters of the circuit is shown in Table I. The chip has an active area of 370 µm x 1800 µm, as shown in Fig. 16. 30 packaged chips with SOP14 were tested over the temperature from $-40°C$ to $85°C$. Fig. 17. A one-point trim at 25°C was done to compensate the $V_{BE}$ mismatch. At 8 samples/s, 2048 delta-sigma cycles, the sensor achieve inaccuracy of $\pm 0.7°C$. Supply current of the sensor consisting of digital back-end, control logic and CIC filter is 10 µA.

6. Conclusion

An ultra-low power CMOS temperature sensor with zoom ADC for RFID was proposed in this paper. The error correction is proposed to make the sensor robust. A smart clock generator is also intended to make the sensor has better performance by leaving more settling headroom in low temperature. The chip area of the sensor is 370 µm x 1800 µm. The measurement error over $-45°C$ to $85°C$ for total 30 test chips in plastic packaging is within $\pm 0.7°C$ after calibration in 25°C. The comparison among recent smart temperature sensors is summarized in Table II. With the same resolution and power level, the proposed circuit is more robust.

Acknowledgments

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Table II: Comparison of inaccuracy between references and this work

| Parameter       | Reference [27] | Reference [28] | Reference [29] | Reference [30] | Reference [14] | This work |
|-----------------|----------------|----------------|----------------|----------------|----------------|-----------|
| Inaccuracy      | ±0.1°C         | 1°C            | −1.4°C to +1.3°C | ±0.5°C         | ±0.25°C        | ±0.7°C    |
| Range           | 20°C to 50°C   | 25°C to 100°C  | 0°C to 100°C   | −40°C to 85°C  | −40°C to 125°C | −45°C to 85°C |
| Condition       | 15 samples     | 12 samples     | 6 samples      | 16 samples     | 19 samples     | 30 samples |
| Process         | 0.18 µm CMOS   | 65 nm 2P4M CMOS | 0.18 µm CMOS   | 65 nm CMOS     | 0.16 µm CMOS   | 0.13 µm CMOS |
| Power and current | 1.8–5.5 V, 16 µA | 1.1 V, 220 µA | 1.2 V, 54 nA  | 0.85–1.05 V, 68 µA | 1.5–2 V, 6 µA | 1.5 V, 10 µA |
| Calibration     | Packaging 1 points | 1 points    | 2 points       | 2 point        | 1 points       | Packaging 1 point |

Fig. 17. Measured temperature error of 30 chips after one-point trim