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PAPER

Electronic design automation for increased robustness in inkjet-printed electronics

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Abstract

Printed electronics is of great interest for low-cost, large-area fabrication due to fast and scalable processes with low material consumption. However, notable resources are currently required for fine-tuning layout designs and process parameters to prevent unintended fabrication artifacts. This study proposes the use of electronic design automation to mitigate such artifacts by segmenting input layouts and arranging the resulting objects in separate conflict-free layers. To this end, two exemplary conflicts with relevance for inkjet printing are defined. The first addresses heterogeneous structures composed of low- and high-resolution features. The second is concerned with layouts requiring a high feature density. Experimental data is used to derive constraints for layer arrangement. Finally, mixed-integer-linear programming is used to formally model the problem and minimize the total number of layers under the aforementioned constraints. The results of printing test layouts with and without algorithmic treatment are characterized in terms of film morphology, device functionality, and fabrication yield. The data demonstrates a more consistent fabrication outcome and significantly increased yields for optimized fabrication batches compared to non-optimized ones. The final processing of the layouts requires no human intervention and can readily be transferred to a variety of ink-substrate systems.

1. Introduction

Over the past decades, printing-based manufacturing has received growing interest as an additive fabrication approach for electronic devices. The key advantages of printed electronics are fast processes for rapid and local prototyping, scalability, the use of low-cost substrates, and an increased compatibility with flexible and stretchable materials compared to classical fabrication approaches [1–3]. In this context, numerous examples of fundamental electronic components such as passive elements, diodes, transistors, memories, batteries, as well as gas and biosensors have been realized [1]. Furthermore, in order to combine these elements into more complex circuits, printed vias, simple integrated circuits, or active-matrix backplanes for the use in display technology have been demonstrated [4, 5]. Solution-based printing techniques show an inherently increased compatibility with polymer materials when compared to the harsh physico-chemical conditions commonly needed in classical fabrication. At the same time, polymer materials exhibit great promise for applications requiring low-cost and large-area flexible electronics such as e.g. polymer LED displays or printed solar cells [6–9]. The possibility of fabricating low-Young’s modulus electronics, which is difficult in classical fabrication, is another advantage of printing technologies. Such soft sensor and actuator fields have recently sparked interest as a means to mitigate inflammatory or foreign-body responses to on-skin or implanted devices or as artificial skin for soft robotics [10–15]. Lastly, apart from these potential benefits, the low-cost aspect of printed electronics renders them attractive...
for a variety of internet-of-things or smart-packaging applications. Here, significant efforts have been devoted to realizing sensors, transistors, and other electronic components on cheap substrates such as paper [16–18].

As a consequence of the rising interest in printing technology, much progress in advancing the limits of printing-based fabrication was made over the past decade or two. Natively, most printing-based technologies do not offer as high a fidelity as classical fabrication approaches. In particular inkjet printing, which—due to its digital nature—holds great promise in research and development settings, is commonly limited to feature sizes in the range of tens of micrometers. Nonetheless, precise tuning of the process parameters or local surface functionalization have been shown to enable printed components with feature sizes below 1 μm [19–22]. Similarly, advances in the materials available for printing-based fabrication have enabled examples of printed RFID tags specifically tuned to the needs of item-level tracking [23]. Following these technological advances, a growing number of sensing applications has been demonstrated using printed devices. Here, examples include printed flexible biosensors, microelectromechanical systems, or microfluidics [24–30]. Nonetheless, applications requiring a high spatial resolution or soft materials, such as in vitro extracellular recordings have proven challenging with regards to process stability and fabrication yield [31–34].

These challenges illustrate a need for automation and generalization in printed-electronics processes. In classical microfabrication, electronic design automation (EDA) has allowed an enormous increase in the complexity of electronic devices after initial applications arose in the 1970s. Currently, the transistor count in one single chip has reached up to 50 billion. EDA approaches ensure the functional correctness of the designs by performing automatic circuit synthesis at different abstraction levels and optimize the yield as well as manufacturing and operating cost considering different types of process variations [35–41]. On a more general level, the concept of design automation has spread to other aspects of engineering including various rapidly emerging fields such as artificial intelligence, internet of things, quantum computing/computers, microfluidics, synthetic biology, and organic electronics [42–52]. These examples illustrate the versatility and generality of design automation techniques.

The present study aims at demonstrating the applicability and benefits of EDA techniques to inkjet-based manufacturing processes. Commonly, artifacts or undesired print outcomes are accounted for by manual adaptation of the print layouts or parameters combined with iterative fabrication tests to achieve a print outcome without height variations and undesired merging of features (compare figure 1 top row). Here, we propose to automate this time-intensive step using EDA as shown schematically in the bottom row of figure 1. Our approach is to analyze and define specific layout features that are prone to fabrication artifacts. We then use an automated process to generate a printing strategy that counteracts these artifacts. Previous examples of algorithmic optimization in inkjet printing exist e.g. for establishing design rules to be used in process design kits or varying drop spacing to optimize pattern reproduction [53, 54]. Our study follows a complementary approach by proposing an optimized print layer arrangement instead of restricting layout design or requiring anisotropic drop spacing.

In the following, we will refer to the above-mentioned sites of likely failure as conflicts. Individually, each of the conflicts discussed herein could be resolved using methods and algorithms similar to those applied e.g. for layer assignment in PCB routing or for multiple patterning [55–57]. In our case, however, the conflict relations can overlap, i.e. an object can have one conflict with a given set of objects and another conflict with a different (potentially overlapping) set of objects. Consequently, existing models and algorithms do not apply to the present example and we use a formal approach to model layer arrangement. Specifically, our aim is to obtain individual layers that can be printed and dried separately without exhibiting artifacts. To this end, we first decompose each object in an input layout into separate polygons. We then detect possible conflicts and ultimately optimize the layer assignment via mixed-integer-linear programming (MILP) to achieve conflict-free output layers. In order to demonstrate the viability of our approach, the following sections will define two exemplary conflicts commonly observed in inkjet printing. Here, we have focused on two conflicts that are of particular relevance for dense layouts composed of heterogeneously sized structures. After defining these conflicts, we lay out an algorithmic structure that allows us to address these conflicts by applying MILP and lastly use experimental data to derive the necessary constraints for optimizing a conflict-free layer assignment. We assess the impact of our optimization by printing exemplary layouts and characterizing their morphology, functionality, and comparing the fabrication yield for optimized and non-optimized fabrication batches.

2. Experimental section

2.1. Algorithmic processing of print layouts

All print layouts were designed in the intended size as pdf files. These .pdf files were then processed by a custom algorithm as briefly described in the following (supporting information is available online at stacks.iop.org/FPE/4/045002/mmedia providing a more detailed description). In the first step, each individual object of a given input layout was extracted. Next, each object was decomposed into strictly convex polygonal segments and the Laplace and proximity conflicts between each pair of polygons were detected based on thresholds in terms of area and dimensions as well as...
distance, respectively. In order to reduce the computational burden during subsequent steps, contacting but conflict-free pairs of polygons were recombined and all remaining contact lines between pairs of polygons were shifted to generate an overlap between individually printed polygons. All polygons were then grouped into print layers under the above discussed constraints using Gurobi® (Gurobi Optimization Inc., Beaverton, Oregon, USA). The resulting print layers were then output as .pdf files, converted to .dxf using Inkscape 0.92 (The Inkscape Project), and prepared for printing using the print parameters described below.

2.2. Print parameters
All prints were performed using an ink composed of 30–35 wt% silver nanoparticles in triethylene glycol monomethyl ether (Silverjet DGP-40LT-15C, Merck KGaA, Darmstadt, Germany). Prior to printing, the ink was sonicated for 30–45 min, filtered through a 0.45 μm polyvinylidene fluoride filter (Whatman, VWR International, Ismaning, Germany), and degassed at –0.8 bar for 5 min. The ink was loaded into a 1 μL cartridge (Dimatix Materials Cartridge, Fujifilm, Tokyo, Japan) and mounted into a commercially available inkjet printer (F-Series, Ceradrop, Limoges, France). During all prints, droplets were ejected at a nozzle plate temperature of 50 °C and a frequency of 2 kHz using a custom waveform resulting in a drop volume of 7.0 ± 0.6 μL ($n = 10$) ejected at approx. 30 m s$^{-1}$. A substrate temperature of 50 °C was used in all experiments and all samples were left to dry completely on the chuck for approx. 10 min after the completion of an individual layer.

In order to illustrate and analyze the Laplace conflict, a planarized 125 μm polyethylene naphthalate foil (Teonex® PQA1M, DuPont Teijin Films, Tokyo, Japan) was used as a substrate and droplets were ejected at a spacing of 20 μm in both x- and y-direction. Two 1 × 1 mm$^2$ contact pads connected by a single row of droplets with a length of 0.5, 1.0, 1.5, 2.0, and 2.5 mm served as test layouts and each wire was processed individually by our algorithm. For each layer arrangement, a total of 75 structures was printed by repeating each wire five times and printing three individual batches. After completion of the printing and prior to electrical characterization, all samples were sintered in a box oven at 150 °C for 1 h.

For the analysis of the proximity conflict, oxidized Si wafers (MEMC Electronic Materials S.p.A., Novara, Italy) were used as substrates and droplets were ejected at a spacing of 60 μm in both x- and y-direction. The test layouts were comprised of IDEs of twenty fingers made of individual rows of droplets at a length of approx. 1.6 mm positioned with a pitch of 68 μm. For each layer arrangement, a total of 150 structures was printed by repeating each structure 50 times and printing three individual batches. After print completion...
2.4. Electrical characterization

For electrical characterization of the printed wires, the samples’ approximate resistance was determined using a multimeter (VC275TRMS, Conrad Electronics SE, Wernberg-Köblitz, Germany) and samples with a resistance over 60 MΩ were regarded as non-functional and excluded from further analysis. The remaining samples were contacted in a four-point configuration using a multichannel potentiostat (VSP-300, Bio-Logic SAS, Seyssinet-Pariset, France). A sequence of currents (2, 4, 6, 8, and 10 μA for samples >100 Ω and 2, 4, 6, 8, and 10 mA for samples <100 Ω) was applied for five seconds each. The resulting voltage drop was recorded at 5 Hz sampling rate and the data was imported into MATLAB® to extract the samples’ resistance by fitting a first-order polynomial. Using the average wire width and nominal wire length, the resistance values of each sample were then converted to sheet resistances.

3. Results

3.1. Conflict definition

As described above, our study focusses on two exemplary conflicts that layouts for printed electronics can exhibit. These conflicts can be observed when an object features a transition between a large and a small (on the order of individual droplets) feature or when two features in a layout are close together and printed such that both are wet at the same time.

3.1.1. Laplace conflict

The first conflict is illustrated in figures 2(a) and (b). The data shows the intersection between a 1 × 1 mm² contact pad on the left and an approx. 40 μm wide line on the right. Both the microscopic and the profilometric data indicate a strong difference in layer height. While the contact pad exhibits layer heights of
≥600 nm, measurements of the line’s film thickness in the outlined region give a value of 37.7 ± 0.9 nm (n = 9). In general, such artifacts can be observed when small (on the order of individual droplets) and large features are printed within the same object. In this case, the shape of the smaller feature is mainly governed by surface tension and therefore rounded. The larger feature on the other hand will exhibit a lower average surface curvature. According to the Young–Laplace equation

$$\Delta p = \gamma \left( \frac{1}{R_1} + \frac{1}{R_2} \right),$$

with Δp as pressure difference between the liquid and the surrounding gas phase, γ as the liquid’s surface tension, and R₁ and R₂ as the surface’s local principal radii, this difference in curvature will result in a local increase in pressure in the smaller feature. The consequent redistribution of the ink leads to a thinning of the final dried film in smaller features that can negatively impact the final device’s functionality and behavior by locally increasing the sheet resistance of the final structure. We refer to this phenomenon as the Laplace conflict. While this is less of a concern for macroscopic layouts, high-density and high-resolution applications of printed electronics commonly exhibit such transitions between e.g. contacts and feedlines or denser and less dense parts of the layout.

3.1.2. Proximity conflict
The second conflict discussed in our study is illustrated in figure 2(c). Here, the schematic shows an interdigitated electrode (IDE). When printing the closely spaced electrode fingers within a single layer, a notable amount of merging and consequent short-cuts of the device can be observed as shown in an exemplary micrograph on the right. This phenomenon can pose severe limitations with respect to device layouts that require a tight spacing of elements for functionality as well as a general increase in integration density in printed electronics. Previous studies on this effect have shown that print parameters ensuring the full drying of one of the features before printing the next can be beneficial to reliably produce small gaps between features [22]. However, this approach can strongly limit the overall fabrication throughput. In particular if the ink or substrate system at hand allows only moderate temperatures and thus evaporation rates are expected to be low. We will refer to this phenomenon as a proximity conflict.

3.2. Algorithmic approach
The conflicts described above can occur both between two objects and within a given object itself. As such, our approach first uses a decomposition step to transform all internal conflicts in the input layout into inter-object conflicts. Generally speaking, the likelihood of an internal conflict scales with the size of the object. Thus, aggressive decomposition can be used to ensure the elimination of all conflicts. However, the computational burden of the following layer assignment increases drastically with the number of objects. As such, the final number of objects should be reduced as much as possible.

In order to achieve this trade-off, our proposed algorithm processes each object in a given input layout in two steps. The first step is to decompose the object into polygons that cannot contain an internal conflict. By analyzing the prerequisites of both the Laplace and the proximity conflict, it can be found that an internal conflict can only appear if the respective polygon is convex, i.e. encompasses internal angles >180° (compare figure 3(a)). As such, our algorithm decomposes each object such that all internal angles are ≤ 180°. To this end internal angles >180° are split by extending the adjacent edges of the polygon and selecting the shorter option for decomposition (compare figure 3(b)). Next, the Laplace and proximity conflicts between each pair of objects are detected based on thresholds in terms of area and

Figure 3. Object decomposition and recombination. (a) Both the Laplace and an internal proximity conflict can only be observed in concave polygons. (b) At each vertex with an internal angle >180°, two cut options are generated by extending the respective edges (dashed and dotted lines). Our algorithm introduces a cut along the shorter of the two options (dashed lines). (c) After decomposition, the individual polygons are recomposed to minimize the total number of objects, but ensure successful transformation of all internal conflicts to inter-object conflicts. (d) In order to ensure proper contact between conflicting polygons, an overlap is introduced.
dimensions as well as distance, respectively. At this stage, the original object is decomposed into a set of strictly convex polygons and all conflict relations are defined. To compensate for redundant decomposition, we recombine all contacting but conflict-free pairs of objects (see figure 3(c)). Further, an overlap between contacting and conflicting objects is introduced in order to ensure a proper contact when printed in separate layers (compare figure 3(d)). This procedure allows us to separate each object in the input layout into a set of conflicting objects without introducing redundant decomposition. After processing all objects of the input layout as described above, we have thus transformed all internal conflicts of the layout into conflicts between different objects. In order to resolve these conflicts by layer assignment, the following sections will derive the necessary constraints for layer optimization from experimental data.

3.3. Constraint definition

3.3.1. Laplace conflict

The structure with different feature sizes shown in figure 2(a) should not be printed within a single layer due to the Laplace effect. After decomposition, the contact pad and the wire are separated into two different objects $P_i$ and $P_j$, respectively, which now can be printed in separate layers. As such, either the large object ($P_i$) or the small object ($P_j$) can be printed first. Figure 4 shows experimental data for both of these options. In comparison to figure 2, the optical and profilometric data in figures 4(a) and (b) illustrate the result of printing and drying the contact pad first. In this arrangement, the contact pad acts as a wick resulting in a reduction of ink in the line similar to the original Laplace conflict. Consequently, the average film height in the line amounts to $40 \pm 1 \text{ nm} (n = 9)$. In addition, strong artifacts in the film morphology can be observed due to the flow of ink from the wire to the pad. Figures 4(c) and (d) illustrate equivalent data for printing the wire first and the pad second. In this configuration, the morphological artifacts are notably reduced and—importantly—the layer height in the wire is increased to an average film thickness of $251 \pm 1 \text{ nm} (n = 9)$. Comparing the amount of ink deposited per area in both regions results in one drop of ink per $20 \times 20 \mu \text{m}^2$ for the contact pad and one drop every $20 \mu \text{m}$ for the line spread over an average line width of $39.99 \pm 0.08 \mu \text{m} (n = 9)$. As such, a difference of a factor of two in terms of film thickness is expected between the pad and the line, which is in reasonable agreement with the profilometric data in figure 4(d).

Overall, printing both features in the same layer as well as printing the contact pad first and the wire second results in strong artifacts and a more than sixfold reduced layer thickness in the small feature posing a risk to device functionality. As a consequence, we introduce the following constraint

$$I_j + 1 \leq I_i,$$

where $I_i$ and $I_j$ refer to the larger and smaller feature’s layer, respectively. In this way, we ensure a relative printing order that successfully prevents unfavorable redistribution of ink caused by the Laplace conflict.

In order to evaluate the effect of the above described procedure on device functionality, we characterized a total of 225 wires of varying length printed in all three configurations. Figure 5 shows the resulting sheet resistance data as a function of wire length.

![Figure 4](image-url)
Printing both features in the same layer or printing the large feature first and the small feature second (blue triangles and orange squares, respectively) yields sheet resistances in the range of $10^1$–$10^2$ $\Omega \cdot \square^{-1}$. The sheet resistance of samples printed in line with equation (3) is in the range of $10^5$ $\Omega \cdot \square^{-1}$. On average, the first two print configurations yield 116- and 50-fold higher sheet resistances than the configuration used by our algorithm. Further, the sheet resistances of the samples printed in the first two configurations exhibit a significantly larger spread and vary as a function of wire length. Specifically, the average sheet resistances for the three configurations are $100 \pm 60$, $44 \pm 4$, and $0.89 \pm 0.04$ $\Omega \cdot \square^{-1}$ ($n = 30, 46, \text{and} 75$, respectively). This corresponds to a relative uncertainty of 60%, 9%, and 4%, respectively. In comparison, our algorithm results in samples that display a higher reproducibility and a linear relation between the resistance and the wire length. In terms of yield, only 40% of the samples printed in a single layer and 61% of the samples with the large feature printed first were functional. In contrast, the configuration used by our algorithm resulted in 100% of functional wires.

Overall, these results illustrate that in print layouts containing transitions between large and small features, a surface-tension-driven redistribution of the
ink can notably decrease the layer thickness of the small feature. Due to the nonlinear relation between layer thickness and sheet resistances observed in thin films, the effect is amplified in the electrical properties of the samples [58–60]. By decomposing the respective objects into separate polygons and imposing a constraint on their relative print order, we are able to avoid unfavorable ink redistribution through the layout, which prevents parasitic contributions to the samples’ resistance and ensures consistent sample behavior and a high fabrication yield.

3.3.2. Proximity conflict
As illustrated in figure 2(c), two polygons $P_i$ and $P_j$ are prone to undesired merging when they are closely spaced and printed in the same layer. Consequently, we do not allow printing two such polygons in the same layer by defining the constraint

$$l_i \geq l_j,$$  \hspace{1cm} (3)

where $l_i$ and $l_j$ refer to $P_i$’s and $P_j$’s print layer, respectively. Figure 6(a) illustrates the result of printing an IDE analogous to the one shown in figure 2(c), but under consideration of equation (3). Here, the electrode fingers are printed before the larger contacts to prevent a Laplace conflict. In addition, the odd and even electrode fingers are printed and dried separately in order to prevent proximity-related merging artifacts. An exemplary micrograph shows that this approach successfully prevents merging of the electrode fingers. In order to quantify the effect of this strategy, we printed a total of 300 IDEs in six batches where three batches were printed considering only the Laplace conflict and three considering both the Laplace and the proximity conflict. Figure 6(b) displays the percentage of functional devices observed throughout these batches. In the batches printed considering only the Laplace conflict 15 out of 150 devices were functional. On average, the per-batch yield in this case was 10% ± 17% ($n = 3$). In particular, two out of three batches resulted in no functional devices at all. In contrast, 120 of 150 devices in the batches considering both the Laplace and the proximity conflict were functional. Here, an average yield of 81% ± 12% ($n = 3$) with a maximum of 94% was observed. These results clearly demonstrate that constraining the layer arrangement as given in equation (3) effectively counteracts fabrication artifacts related to the proximity conflict.

In order to be able to apply equation (3) in MILP as proposed initially, we need to transform it into a linear representation. To this end, we first restate equation (3) as

$$l_i + 1 \leq l_j \lor l_j + 1 \leq l_i,$$  \hspace{1cm} (4)

i.e. for $P_i$ not to be printed in the same layer as $P_j$ either $P_i$ or $P_j$ has to be printed first. Next, we apply the ‘big M’ method

$$l_i + 1 \leq l_j + M \cdot (1 - q),$$  \hspace{1cm} (5)

where $M$ and $q$ represent a large constant and an auxiliary variable, respectively [61]. In this way, when setting $q = 1$ equation (5) is always fulfilled and equation (6) reduces to $l_i + 1 \leq l_j$. On the other hand, setting $q = 0$ reduces equation (5) to $l_i + 1 \leq l_j$ and causes equation (6) to be always fulfilled. In combination with the decomposition described above, we are thus able to resolve both proximity conflicts within a given objects and between different objects of the original layout by ensuring the layer assignment meets equations (5) and (6).

3.4. Layer assignment
The previous sections have demonstrated how separating individual features of a print layout into different layers can be used to successfully mitigate inkjet-specific fabrication artifacts. However, arbitrarily assigning objects to print layers can result in layer arrangements that will not cause fabrication artifacts, but involve an excess number of layers (see supporting information for a more detailed description). Here, we refer to the total number of layers as $l_{tot}$, which is bounded by 1 and N with N being the number of polygons after decomposition of the input layout.

In order to minimize fabrication time, we introduce

$$l_i \leq l_{tot}$$  \hspace{1cm} (7)

as a last constraint and model the overall problem as minimize $l_{tot}$

Subject to: (2) and (5)–(7).

In this way, we combine as many conflict-free features as possible into one layer to prevent excess layers. After decomposition, all layouts considered in this study consisted of less than 25 objects and were optimized in less than a second. As such, we expect the runtimes of larger layouts to remain moderate.

4. Conclusion and outlook
In this study, we presented the application of EDA techniques to the inkjet-based fabrication of printed electronics. To this end, we defined two exemplary layout features—the Laplace and the proximity conflict—that can cause fabrication artifacts leading to undesired device behavior or even failure. We developed an algorithm that is capable of automatically detecting these features in a given layout and outputs a modified version of the layout that effectively prevents fabrication artifacts. Specifically, the algorithm detects large-to-small-feature transitions in the layout, separates the respective objects, and places them into separate print layers. In this way, surface-tension-driven redistribution of ink and consequential layer thinning and parasitic resistances are successfully counteracted. Similarly, closely spaced layout features are detected and placed into separate layers to prevent unintended merging of features that can short-cut different circuit elements. We ensure a high fabrication throughput by
minimizing the total layer count in order to combine as many conflict-free features as possible into one layer. In particular in the case of low-evaporation systems, this strategy makes use of excessive drying periods by printing other conflict-free features of the layout. We illustrate our algorithm’s capabilities by comparing test layouts fabricated with and without algorithmic treatment. Our results show more reliable device properties, less variation, and a significantly higher yield for layouts printed in line with the algorithm’s recommendation. The whole process is automatically conducted by the computer and no human intervention is required. Lastly, our approach is system-independent and can readily be transferred to other ink–substrate combinations and printing platforms. To this end, appropriate conflict definitions have to be made and constraints to resolve these have to be defined. In particular with regards to unidirectional printing techniques such as roll-to-roll printing, we believe that our algorithm poses notable potential. In this context, additional layers require additional printheads or multiple passes of the roll. Using our method, the minimum number of required layers to ensure the artifact-free fabrication of a given layout can be ensured.

In addition to the exemplary fabrication artifacts discussed in this study, our approach can easily be extended by including further conflict definitions. In particular, aspects of multilayered printing with different materials could be addressed in future studies. I.e. similar to the application of EDA in photomask development, the algorithm could adapt the layout of a given layer to compensate potential differences in wetting behavior on the substrate and a previous layer. The conflicts discussed herein apply solely to systems that display negligible or slow absorption or drying. As such, they are usually not observed when printing on absorbing substrates (e.g. uncoated paper or fabric) or with low-boiling-point inks. Nonetheless, our methodology can be applied to such systems, too, by establishing appropriate conflict definitions and constraint to resolve these conflicts. Further, rasterization artifacts could be addressed by segmenting off-grid parts of a layout into separate layers. The inclusion of constraints to optimize the layer arrangement in terms of drying time could also be used to increase the benefits of our approach.

In most current printing processes, the adaptations and countermeasures described above are performed manually and in an iterative fashion by either adjusting print parameters or layout features. Despite the short development cycles in printing-based fabrication, this approach can demand notable time and experience to be completed successfully. We believe that our strategy can replace significant portions of the manual and iterative aspects of process development in printing-based fabrication. In this way, scientists and engineers can allocate more resources to developing new materials and sensor concepts to help fully exploit the potential of printed electronics.

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