Towards low-dimensional hole systems in Be-doped GaAs nanowires

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Abstract

GaAs was central to the development of quantum devices but is rarely used for nanowire-based quantum devices with InAs, InSb and SiGe instead taking the leading role. p-type GaAs nanowires offer a path to studying strongly confined 0D and 1D hole systems with strong spin–orbit effects, motivating our development of nanowire transistors featuring Be-doped p-type GaAs nanowires, AuBe alloy contacts and patterned local gate electrodes towards making nanowire-based quantum hole devices. We report on nanowire transistors with traditional substrate back-gates and EBL-defined metal/oxide top-gates produced using GaAs nanowires with three different Be-doping densities and various AuBe contact processing recipes. We show that contact annealing only brings small improvements for the moderately doped devices under conditions of lower anneal temperature and short anneal time. We only obtain good transistor performance for moderate doping, with conduction freezing out at low temperature for lowly doped nanowires and inability to reach a clear off-state under gating for the highly doped nanowires. Our best devices give on-state conductivity 95 nS, off-state conductivity 2 pS, on-off ratio ~10⁴, and sub-threshold slope 50 mV/dec at T = 4 K. Lastly, we made a device featuring a moderately doped nanowire with annealed contacts and multiple top-gates. Top-gate sweeps show a plateau in the sub-threshold region that is reproducible in separate cool-downs and indicative of possible conductance quantisation highlighting the potential for future quantum device studies in this material system.

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(Some figures may appear in colour only in the online journal)

1. Introduction

GaAs has played a vital role in the development of quantum nanoelectronic devices over the past 30 years. The modulation-doped AlGaAs/GaAs heterostructure supports a quasi-two-dimensional electron gas with remarkably high electron mobility >10⁵ cm²V⁻¹s⁻¹ [1]. This made AlGaAs/GaAs the system of choice for quantum Hall effect research [2]; thereafter it was central to work on 1D transport in quantum point contacts and quantum wires [3, 4], Coulomb blockade and quantum interference in quantum dots [5], and emerging designs for spin-based quantum information devices [6, 7]. The semiconductor nanowire is another major advance in nanoelectronics. Born from the development of catalyst-assisted semiconductor growth methods in the 1960s [8], nanowires are being developed for applications from electronics and photonics to energy harvesting and biosensing [9].

Nanowire-based quantum devices have primarily been developed using InAs/InP [10–13, 54], InSb [14–16] or SiGe nanowires [17–19], despite GaAs being one of the first materials grown in nanowire form [20]. Surface-states and their influence on carrier accumulation and contact ohmicity
are largely responsible. Surface-states in InAs pin the surface Fermi energy above the conduction band minimum [21]. This results in electron accumulation at the nanowire surface enabling effective ohmic contact with negligible Schottky barrier via patterned deposition of metal contacts. Similar behaviour occurs for InSb nanowires [14]. In SiGe nanowires, the valence band offset causes hole accumulation in the Ge core without intentional doping; the holes can be accessed via annealed Ni contacts [17]. In each case, normally on transistors are readily achieved without intentional doping using relatively simple contact formulations.

Surface-states in GaAs pin the surface Fermi energy mid-gap giving metal-semiconductor interfaces with a substantial Schottky barrier, typically $\sim$0.5 eV, and a lack of intrinsic carrier accumulation [22]. Ohmic contacts to GaAs are normally achieved using annealed alloys, e.g., NiGeAu for n-type contacts and PdZn or AuBe for p-type contacts [23]. Contact formation involves two key actions of the thermal annealing process. The first is diffusion of dopant species, i.e., Ge, Zn or Be, into the semiconductor. This degenerately dopes the adjacent semiconductor, producing a sufficiently narrow depletion region where tunnelling provides contact ohmicity [24]. The second is strong spiking/penetration of Au into the semiconductor. This can be detrimental for contacts to bulk GaAs [25, 26] but vital in heterostructure devices where contact access to buried conduction layers is required [27]. Functional annealed contacts can be extremely difficult to obtain and optimise in nanowires due to their tiny volume and high aspect ratio; in many instances buckling and breakage of the nanowire and contact interfaces occurs. Additionally, GaAs nanowires have to be doped during growth for sufficient carrier density to conduct current. Doping nanowires is also complicated because there are numerous routes for dopant incorporation [28] and common III–V dopants are amphoteric depending on incorporation site [29]. The incorporation site is in turn dependent on growth mechanism (axial versus radial), conditions and the exposed facets—the nanowire geometry invariably means numerous facets are exposed during growth.

GaAs nanowires are of significant interest for quantum device research [30] despite these challenges to making functional high-quality devices. A particular area of opportunity is the study of strongly confined 0D and 1D hole systems [31, 32]. Holes in GaAs exhibit strong spin–orbit effects, behaving like spin-$\frac{1}{2}$ particles, by virtue of the $p$-like nature of GaAs valence band states [33]. This led to the observation of highly anisotropic Zeeman spin-splitting in 1D hole systems [34–36] and correspondingly anisotropic Kondo physics in hole quantum dots [37] made using conventional planar p-type AlGaAs/GaAs heterostructures. A major difficulty in these devices is the ability to achieve strong confinement and access the few-electron limit [38]. The unique geometry offered by GaAs nanowires may overcome these difficulties. In this paper we report on the development of FET devices based on Be-doped p-type GaAs nanowires grown by molecular beam epitaxy (MBE). Our devices feature both doped silicon back-gates [39] and oxide-insulated top-gate structures [40], the latter with strong potential for realising functional quantum devices. Figure 1(a) shows a band diagram of a p-doped GaAs top-gated transistor. We focus here mostly on electrical transistor performance relative to dopant concentration and contact preparation, but also present preliminary data indicative of possible 1D conductance plateaus in our nanowire devices.

### 2. Fabrication and Measurement

Our homostructure core–shell GaAs nanowires were grown by MBE on (111) Si [41] using the self-catalysed Ga-assisted method [42, 43]. The undoped core was grown at 630 °C using an As$_x$ source and V/III flux ratio of 60 or 30 for 45 min. A Be-doped shell was then grown at 465 °C using As$_x$ and a V/III ratio of 150 for 30 min, giving final structures
with diameter 120–200 nm and length 6–10 μm. We studied nanowires with three different shell doping densities $n_{Be} = 1 \times 10^{18} \text{ cm}^{-3}$, $5 \times 10^{18} \text{ cm}^{-3}$ and $1.5 \times 10^{19} \text{ cm}^{-3}$, which we will refer to as low $n_{Be}$, moderate $n_{Be}$ and high $n_{Be}$, respectively. $n_{Be}$ was estimated using four-terminal measurements on grown nanowires [41].

Device fabrication was performed on a degenerately doped Si wafer capped with a bilayer oxide consisting of 100 nm thermally grown SiO$_2$ and 10 nm HfO$_2$ deposited by atomic layer deposition (ALD). The bilayer oxide is not essential and is an artefact of our other nanowire device projects [44]. The wafer was pre-patterned with alignment markers for electron-beam lithography (EBL) and Ti/Au interconnects. Nanowires were randomly deposited by dry transfer and then located by darkfield optical microscopy to facilitate deposition of contacts and gating structures direct to a selected nanowire. In this study, two different types of devices were made. The simplest devices feature a pair of source and drain contacts made with 200 nm of 99:1 Au:Be alloy (ACI alloys) defined by EBL and vacuum thermal evaporation. In some instances the AuBe contacts were annealed using an Ulvac-Riko Mila 4000 rapid thermal annealer with carbon susceptor at temperatures between 250 °C and 350 °C for times up to 120 s. The anneal temperature was deliberately kept below 350 °C to avoid the onset of strong Au penetration/spiking [25] from destroying the nanowire, although mild Au penetration into GaAs still occurs well below 350 °C [45]. Gating in these devices was achieved using the degenerately doped Si substrate [39]. Our more complex devices also feature a top-gate, which is produced in two steps following fabrication of the AuBe contacts. The first step was deposition of an EBL-defined 10 nm HfO$_2$ top-gate insulator by ALD. The second step was deposition of an EBL-defined 20/180nm Ti/Au gate electrode. Figure 1(b) shows a scanning electron micrograph of a completed top-gate device with the HfO$_2$ insulator highlighted by the dashed line. More complete details of the fabrication process are provided in the supplementary information, available online at stacks.iop.org/NANO/28/134005/mmedia. Figure 1(c) shows a cross section through the top-gated section of the device.

Device measurements were performed using either a probe station (Signatone) in a Faraday cage in ambient conditions, a home-built dipstick loaded into a He dewar or an Attocube attoDry 2100 variable-temperature system with base temperature $T = 1.5$ K. DC measurements were used to characterise the devices. In section 3, a source-drain bias $V_{sd}$ was applied using a Keithley K236 source-measure unit, which simultaneously measures the source current $I_s$. The drain current $I_d$ is measured using a Keithley K6517A electrometer. Unless mentioned explicitly, $I_s = I_d$, which we refer to as the source–drain current $I_{sd}$ hereafter. In section 4, a Yokogawa GS200 was used to set $V_{sd}$ and a Keithley K6517A was used to measure $I_{sd}$. The back-gate voltage $V_{bg}$ and top-gate voltage $V_{tg}$ were applied using Keithley K2401 source-measure units to enable continuous monitoring of gate leakage current $I_g$.

![Figure 2. Plot of source-drain current $I_{sd}$ versus source–drain bias $V_{sd}$ at $V_{bg} = 0$ V for doping densities (a) $n_{Be} = 1 \times 10^{15}$ cm$^{-3}$, (b) $n_{Be} = 5 \times 10^{18}$ cm$^{-3}$, and (c) $n_{Be} = 1.5 \times 10^{19}$ cm$^{-3}$. The contacts are unannealed in all three cases.](image)

3. AuBe as a contact metal for Be-doped nanowires

The AuBe ohmic contacts are one of the key contributors to the stability and performance of the devices in [34–37]. These contacts give reliable linear $I$–$V$ with relatively high yield in these devices subject to appropriate optimisation of anneal conditions [46]. This made AuBe an interesting contact metal to try with Be-doped GaAs NWs, with the intention that the contacts could be annealed to supplement the Be density local to the contact and facilitate ohmic p-type contact to GaAs nanowires as the shell doping density is reduced. Thus we now focus on our simple back-gated samples to look at contact efficacy versus $n_{Be}$ and anneal conditions. We begin by looking at unannealed AuBe contacts and then move on to discuss how annealing alters contact performance.

Figure 2 shows typical $I_{sd}$ versus $V_{sd}$ characteristics for the three different nanowire doping densities investigated with unannealed AuBe contacts. The main feature indicating good contact performance is that $I_{sd}$ increases linearly rather than exponentially as $|V_{sd}|$ is increased from zero—the former is characteristic of ohmic contacts whereas the latter is characteristic of diode-like Schottky contacts. The $I_{sd}$ versus $V_{sd}$ characteristic for low $n_{Be}$ in figure 2(a) is nonlinear but with the opposite curvature to Schottky contact behaviour—the curvature here arises due to saturation and is normal for field-effect transistors (FETs). This form is observed in 85% of our low $n_{Be}$ devices, with around 5% showing rectifying contacts instead. The comparative linearity for figures 2(b) and (c) where $n_{Be}$ is much higher is expected because saturation
voltage is proportional to doping density in FETs [47], pushing saturation outside the ±2.5 V measurement range. The increased $n_{Be}$ also reduces the Schottky barrier depletion width [41] enabling tunnelling to contribute strongly to the contact conduction process [24]. Correspondingly, the conductance $G$ increases from 48 ± 23 nS for low $n_{Be}$ to 1.5 ± 0.9 μS for moderate $n_{Be}$ and 9.4 ± 2.9 μS at high $n_{Be}$, respectively. We also examined the symmetry of the $I_d$ versus $V_{sd}$ characteristics as an additional indicator of contact quality. We defined an $I_d$ versus $V_{sd}$ characteristic as ‘symmetric’ if both: (a) the $I_d$ at $V_{sd} = ±2.5$ V, and (b) the integrals $\int I_d dV_{sd}$ for $−2.5 < V_{sd} < 0$ V and $0 < V_{sd} < 2.5$ V differ by less than 25%. Across the 30–35 devices measured at each $n_{Be}$, we found 17% gave symmetric $I_d$ versus $V_{sd}$ characteristics at low $n_{Be}$, 44% at moderate $n_{Be}$, and 100% at high $n_{Be}$. We conclude that the high $n_{Be}$ nanowires give the best contact performance.

We measured a sufficient number of devices with unannealed contacts that we can also assess resistance $R$ versus channel length $L$ for the three different $n_{Be}$; the data is plotted in figure 3. The resistance shows no clear trend with length for low and moderate $n_{Be}$, as expected if the contact resistance dominates the channel conductivity. We estimate the contact resistance for the low and moderate $n_{Be}$ devices to be 10 MΩ and 200 kΩ, respectively, by extrapolating to $L = 0$ μm. There is a clear relationship between $R$ and $L$ for high $n_{Be}$, as expected when the contact resistance is no longer dominant. We estimate the contact resistance for high $n_{Be}$ to be 29 ± 15 kΩ.

We now turn our attention to annealed AuBe contacts. The typical anneal for AuBe contacts to planar p-type AlGaAs/GaAs heterostructures is 450 °C–550 °C for 60–120 s [46]. However, in that instance, strong diffusion of ohmic spikes to a significant depth ~100 nm is required to access the 2D hole layer. Such an anneal is too aggressive for our nanowires. We instead focus in the 250 °C–350 °C range where Au penetration is not so aggressive [25] for times of 30–120 s to obtain Be diffusion without severely detrimental effects, e.g., buckling and nanowire breakage. These anneal conditions are not too dissimilar to those used for NiGeAu contacts to n-type GaAs/AlGaAs core–shell nanowires by Morkötter et al. [30]. For each set of anneal conditions, we measure the source–drain characteristics immediately prior to annealing and immediately thereafter, with $V_{be} = 0$ V. Annealing generally produces one of two effects—either the contact is improved, becoming more linear with higher $I_d$ at fixed $V_{sd}$, or it is deteriorated, giving lower $I_d$ at fixed $V_{sd}$ and/or reduced symmetry. Figures 4(a) and (b) show typical examples of improved and deteriorated contacts, respectively.

Figure 5 shows the evolution of $I_d$ versus $V_{sd}$ with annealing time for three different anneal temperatures at each of the three doping densities. The logarithmic scale for $I_d$ is used to better highlight changes in $I_d$ with asymmetry evident as different saturation levels at high positive/negative $V_{sd}$. The corresponding data plotted on a linear scale is presented in the supplementary information. Before elaborating on specifics, our overall finding is that while improvement in contact quality can be obtained in some circumstances, annealing generally proves detrimental. The best outcome occurs for moderate $n_{Be}$ at $T = 300$ °C (figure 5(e)) where significant improvement can be achieved for minimal anneal time. A similar outcome is attained for moderate $n_{Be}$ at $T = 250$ °C (figure 5(f)). Otherwise annealing generally provides little improvement, e.g., high $n_{Be}$ at $T = 250$ °C (figure 5(g)), or makes the contacts drastically worse (all other panels). The anneal is uniformly detrimental for low $n_{Be}$, which unfortunately is where improved contacts are most needed. Given this result, we performed a more extended study of anneal efficacy at moderate $n_{Be}$. Table 1 presents the yield of improved contacts versus anneal temperature and
time, with the optimum outcome being an 83% yield for annealing at 250 °C for 60 s.

We can explain our data in figure 5 on the basis that the diffusion of grown-in Be dopants within the nanowire is much faster than the diffusion of Be from the AuBe contacts into the nanowire. We are unable to find data for Be out-diffusion rate from AuBe alloy on GaAs but Be is well-known for its high diffusion rate as a dopant species in GaAs [48–50]. Under this scenario, for the low $n_{\text{Be}}$ samples, loss of Be from shell to core should both deteriorate the contacts, due to a rise in surface depletion width [41], and reduce the overall nanowire conductivity. For moderate and high $n_{\text{Be}}$, small amounts of dopant diffusion consistent with short anneals at relatively low temperature should not significantly deteriorate the contacts, and might well improve them slightly, as observed in figures 5(d) and (e). That said, higher temperatures and longer anneal times should tip the balance toward worse contact performance, as in the low $n_{\text{Be}}$ case, due to net diffusion of Be out of the shell.

### Table 1. This table shows the yield of improved contacts by annealing for the $n_{\text{Be}} = 5 \times 10^{18}$ cm$^{-3}$ (moderately doped) nanowires.

| $T$(°C) | Annealing time |
|--------|----------------|
|        | 30 s | 60 s | 90 s | 120 s |
| 250    | 75%  | 83%  | 75%  |
| 300    | 73%  | 45%  | 36%  | 36%  |
| 350    | 18%  | 18%  | 10%  | 10%  |

4. Top-gated Be-doped GaAs nanowire transistors

We now turn our attention to obtaining local gating for our Be-doped GaAs nanowires. Local gating requires patterned gate electrodes, which are most readily obtained by depositing an oxide layer by ALD to insulate the nanowire followed by EBL to define metal top-gate electrodes. The oxide can either be a conformal coating applied to the nanowires while standing vertically on the growth substrate, or a patterned oxide over the partially complete device structure. The InAs native oxide has been used to insulate local gate electrodes previously [40] but these gates only perform well, i.e., without strong current leakage, for small gate biases. Ultimately, the need for a gate oxide in In-based nanowires is driven by the small Schottky barrier arising from surface-state pinning [21]. In contrast the oxide should, in principle, be optional for GaAs nanowires because the mid-gap surface pinning induces a stronger Schottky barrier. Although this is true for AlGaAs/GaAs heterostructure devices, it does not work so well for our GaAs nanowire transistors, presumably due to the shell doping. After fabricating such a device with low $n_{\text{Be}}$ nanowires, we found that the gate leakage current $I_g \sim 400$ pA at the peak $I_{sd}$ of 1 nA. In contrast, our gate leakage current is always below 10 pA for top-gates featuring a HfO$\text{2}$ insulator.

Since our objective is quantum transport studies, we made top-gate transistors for each $n_{\text{Be}}$ and examined their performance as the temperature $T$ was reduced to 4 K. The aim was to find the lowest $n_{\text{Be}}$ giving the following desirable properties at low $T$: (1) reasonably symmetric and linear $I_{sd}$ versus $V_{sd}$ characteristics; (2) on-state conductance of order 100 nS or more; and (3) off-state conductance below 10 nS.
(i.e., on–off ratio better than $10^3$). The desire for the lowest $n_{Be}$ possible is to minimise dopant scattering and thereby maximise ballistic transport length.

Figure 6 shows $I_{sd}$ versus $V_{sd}$ for devices with different $n_{Be}$. At low $n_{Be}$ the room temperature on-state conductivity $G \sim 8$ nS is low, and as we reduce $T$ conduction freezes out (figure 6(a)). By $T = 155$ K we no longer see distinct on- and off-states. Thus, combined with the poor $I_{sd}$–$V_{sd}$ characteristics shown earlier, these nanowires are unsuitable for quantum transport studies. The high $n_{Be}$ nanowires are also unsuitable. Figure 6(c) shows data for a high $n_{Be}$ device at $T = 4$ K. While the on-state conductivity is high, and the $I_{sd}$ versus $V_{sd}$ characteristics are good, the on-off ratio is poor at $\sim 1.1$ with a high off-state current, i.e., we cannot properly deplete the high $n_{Be}$ nanowires with a metal top-gate. In contrast, the moderate $n_{Be}$ devices show considerable promise for low $T$ quantum transport applications. Figure 6(b) shows data obtained at $T = 4$ K for three different back-gate voltages $V_{bg}$ in a device annealed at $T = 250$ °C for 60 s. These devices show good on-state and off-state conductivity, 95 ns and 2 pS respectively, and high on-off ratio $\sim 10^4$. The top-gate sub-threshold slope is 50 mV/decade at $V_{bg} = 0$ V at $T = 4$ K. We found the top-gate subthreshold slope to be an order of magnitude better than is typical using the back-gate.

We also found scope for tuning the top-gate threshold voltage using the back-gate (figure 6(b)). We obtain a typical field-effect mobility of only $\sim 2$ cm$^2$/Vs at $T = 4$ K but note that this will be severely contact-limited for our devices and is unlikely to be a reliable measure of the true channel performance. The moderate $n_{Be}$ devices also give decent contact performance at $T = 4$ K. As figure 7 shows, $I_{sd}$ versus $V_{sd}$ is somewhat nonlinear but at least symmetric, and with sufficient conductance at reasonable $V_{sd}$ to viably use for further studies.

We made the device shown in figure 8(a) to demonstrate the potential for quantum transport studies using the moderate $n_{Be}$ nanowires with contacts annealed at $T = 300$ °C for 30 s. The device architecture features three narrow top-gates, each designed to define a short constriction in the nanowire, and together form a tunable quantum dot. Figure 8(b) shows $I_{sd}$ versus $V_{tg}$ obtained at $T = 1.5$ K for the two gates RG and CG—unfortunately the third gate LG functions poorly (see online supplementary figure S4) and was not considered further for this work. The characteristics for RG and CG show clear on- and off-states, strong sub-threshold behaviour, and curiously, a clear plateau at a common intermediate conductance for both gates. Figure 8(c) shows the same measurement obtained on a separate cooldown. The reduced on-state $I_{sd}$ is due to aging of the sample between the two cooldowns, which were separated in time by several weeks. The plateau structure appears similarly in both cooldowns. This suggests the plateau’s origin is not a quantum interference resonance arising from the ionised doping potential, since this should reconfigure [51] upon warming to room temperature given Be is a shallow acceptor in GaAs [52].

Figure 9 shows data obtained to further investigate the plateau structures in figure 8. The data in figure 9(a) is obtained in two stages. We start with CG and RG in a strong on-state by setting $V_{CG} = V_{RG} = -2$ V. First we sweep RG to
just below the plateau, i.e., $V_{RG} = +2.2$ V. Assuming the plateau indicates quantised conductance, this would mean that just a single 1D mode is transmitted through the region under RG. Second, we sweep CG from $V_{CG} = -2$ V to pinch-off ($I_{sd} = 0$). Interestingly, the plateau in the CG trace disappears in this case (see data in figure 8(c)). In figure 9(b) we repeat this measurement with the gates reversed—sweep CG to just below the plateau, then sweep RG to pinch-off. Here also the plateau disappears for the RG trace. This behaviour is consistent with that observed in a pair of QPCs separated by less than the ballistic length [53], where conservation of 1D subband index in transport means the series resistance is determined by whichever QPC passes the fewest 1D sub-bands.

This has also recently been observed in InAs nanowire devices [54]. In the context of figure 9(a), for example, it means that once we drive RG to below the first plateau, then only a single 1D subband can pass under CG. This single 1D subband remaining in transport at $V_{CG} = +2.2$ V is pinched-off as a single step as $V_{RG}$ is driven positive. The same holds on reversing the gates. The behaviour we observe here lends further support for the plateau we observe being caused by 1D conductance quantisation.

Future work will focus more closely on quantum transport effects in these p-GaAs nanowire devices. This will include studies of larger diameter nanowires seeking to obtain more than the single plateau we observe in the structures reported here as well as Coulomb-blockaded quantum dot devices for studying spin–orbit effects in the single-hole limit.

5. Conclusion

We reported on the development of nanowire transistors featuring Be-doped p-type GaAs nanowires and AuBe alloy contacts towards making nanowire-based hole quantum devices. Devices with traditional doped-substrate back-gates and EBL-defined metal/oxide top-gates were produced for three different Be-doping densities $n_{Be}$ and a range of AuBe contact processing recipes. A key focus was the comparison of unannealed contacts with those annealed at 250 °C–350 °C.

Figure 8. (a) Scanning electron micrograph of a three-gate nanowire transistor made using a moderate $n_{Be}$ GaAs nanowire and AuBe contacts annealed at 300 °C for 30 s. The source (S), drain (D), insulator (I), left-gate (LG)—shaded orange, centre-gate (CG)—shaded blue, and right-gate (RG)—shaded red, are indicated. The three gate electrodes are 200 nm wide with 200–300 nm spacing and insulated from the nanowire by 10 nm of HfO2. The scale bar represents 5 μm. (b) $I_{sd}$ versus $V_{tg}$ for CG (solid blue) and RG (dashed red) for the device in (a). Measurements were obtained at $T = 1.5$ K with $V_{sd} = 500$ mV (rms), $V_{bg} = 0$ V and no magnetic field applied. (c) $I_{sd}$ versus $V_{tg}$ for CG (solid blue) and RG (dashed red) obtained on a separate cooldown. The dashed red traces in both (b) and (c) are horizontally offset by $-0.5$ V for clarity. Any top-gate not being actively swept is held at $V_{tg} = -2$ V (strong on-state) to prevent them adversely influencing the measurements.

Figure 9. Plots of $I_{sd}$ versus $V_{tg}$ for (a) RG taken first to just below first plateau $V_{RG} = +2.2$ V with $V_{CG} = -2$ V (solid red) followed by a sweep of CG to pinch-off with $V_{CG} = +2.2$ V (dashed blue), and (b) CG taken first to just below first plateau $V_{CG} = +2.2$ V with $V_{RG} = -2$ V (solid blue) followed by a sweep of RG with $V_{CG} = +2.2$ V (dashed red). Measurements were obtained at $T = 300$ mK with $V_{sd} = 500$ mV (rms), $V_{bg} = 0$ V and no magnetic field applied.
for up to 120 s using a rapid thermal annealer. Annealing only brings small improvements for the moderately doped devices under conditions of lower anneal temperature and short anneal time. Otherwise, annealing generally proves detrimental. We attribute this to the diffusion of Be dopants from the shell being much faster than the out-diffusion of Be from the AuBe alloy into the GaAs. The performance of the top-gate transistors is also \(n_{\text{Be}}\)-dependent. Conduction in the lowest \(n_{\text{Be}} = 1 \times 10^{18} \text{ cm}^{-3}\) nanowires freezes out below \(\sim 100\) K making these devices unsuitable for quantum device applications. The highest \(n_{\text{Be}} = 1.5 \times 10^{19} \text{ cm}^{-3}\) devices cannot be fully depleted by our top-gates and give poor on-off ratio \(\sim 1.1\) making them also unsuitable. The moderate \(n_{\text{Be}} = 5 \times 10^{18} \text{ cm}^{-3}\) devices with contacts annealed \(T = 250\) °C for 60 s give good on-state conductivity 95 nS, off-state conductivity 2 pS, on-off ratio \(\sim 10^4\), and sub-threshold slope 50 mV/dec at \(T = 4\) K, making them well suited for quantum device studies. Lastly, we made a device featuring a moderate \(n_{\text{Be}}\) nanowire with annealed contacts and multiple top-gates. Top-gate sweeps show a plateau in the sub-threshold region indicative of possible conductance quantisation that is reproducible in separate cool-downs, demonstrating the potential of our device structures for future quantum transport studies.

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**References**

[1] Stöhrer H L, Gossard A C, Wiegmann W and Baldwin K 1981 Dependence of electron mobility in modulation doped GaAs (AlGa)As heterojunction interfaces on electron density and \(Al\) concentration *Appl. Phys. Lett.* 29 912–4

[2] Stöhrer H L 1999 Nobel lecture: the fractional quantum hall effect *Rev. Mod. Phys.* 71 875–89

[3] Beenakker C W J and van Houten H 1991 *Quantum Transport in Semiconductor Nanostructures* ( Solid State Physics vol 44) ed H Ehrenreich and D Turnbull (New York: Academic) pp 1–228

[4] Micloch A P 2011 What lurks below the last plateau: experimental studies of the 0.7 \(\times 2e^2/h\) conductance anomaly in one-dimensional systems *J. Phys.: Condens. Matter* 23 443201

[5] Kouwenhoven L P, Marcus C M, McEuen P L, Tarucha S, Westervelt R M and Wingreen N S 1997 *Electron Transport in Quantum Dots* (Mesoscopic Electron Transport vol 345) ed L L Sohn et al (Dordrecht: Kluwer Academic) pp 105–214

[6] van der Wiel W G, de Francheschi S, Elzerman J M, Fujisawa T, Tarucha S and Kouwenhoven L P 2003 Electron transport through double quantum dots *Rev. Mod. Phys.* 75 1–22

[7] Hanson R, Kouwenhoven L P, Petta J R, Tarucha S and Vandersypen L M K 2007 Spins in few-electron quantum dots *Rev. Mod. Phys.* 79 1217–65

[8] Wagner R S and Ellis W C 1964 Vapor–liquid–solid mechanism of single crystal growth *Appl. Phys. Lett.* 4 89–90

[9] Dasgupta N P, Sun J, Liu C, Brittan S, Andrews S C, Lim J, Gao H, Yan R and Yang P 2014 Semiconductor nanowires —synthesis, characterization and applications *Adv. Mater.* 26 2137–84

[10] Björk M T, Thelander C, Hansen A E, Jensen L E, Larsson M W, Wallenberg L R and Samuelson L 2004 Few-electron quantum dots in nanowires *Nano Lett.* 4 1621–5

[11] Fasth C, Fuhrer A, Björk M T and Samuelson L 2005 Tunable double quantum dots in InAs nanowires defined by local gate electrodes *Nano Lett.* 5 1487–90

[12] Nadj-Perge S, Frolov S M, Bakkers E P A M and Kouwenhoven L P 2010 Spin–orbit qubit in a semiconductor nanowire *Nature* 468 1084–7

[13] Heedt S, Prost W, Schubert J, Grützmacher D and Schäpers T 2016 Ballistic transport and exchange interaction in InAs nanowire quantum point contacts *Nano Lett.* 16 3116–23

[14] Nilsson H A, Caroff P, Thelander C, Larsson M W, Wagner J B, Wernersson L-E, Samuelson L and Xu H Q 2009 Giant, level-dependent \(g\) factors in InSb nanowire quantum dots *Nano Lett.* 9 3151–6

[15] Mourik V, Zuo K, Frolow S M, Plissard S R, Bakkers E P A M and Kouwenhoven L P 2012 Signatures of Majorana fermions in hybrid superconductor-semiconductor nanowire devices *Science* 336 1003–7

[16] van Weperen I, Plissard S R, Bakkers E P A M, Frolow S M and Kouwenhoven L P 2013 Quantized conductance in an InSb nanowire *Nano Lett.* 13 887–91

[17] Lu W, Xiang J, Timko B P, Wu Y and Lieber C M 2005 One-dimensional hole gas in germanium/silicon nanowire heterostructures *Proc. Natl. Acad. Sci. USA* 102 10046–51

[18] Hu Y, Churchill H O H, Reilly D J, Xiang J, Lieber C M and Marcus C M 2007 A Ge/Si heterostructure-based nanowire double quantum dot with integrated charge sensor *Nat. Nanotechnol.* 2 622–5

[19] Roddar S, Fuhrer A, Brusheim P, Fasth C, Xu H Q, Samuelson L, Xiang J and Lieber C M 2008 Spin states of holes in Ge/Si nanowire quantum dots *Phys. Rev. Lett.* 101 106802

[20] Hiruma K, Yazawa M, Katsuyama T, Ogawa K, Haraguchi K, Koguchi M and Kakibayashi H 1995 Growth and optical properties of nanometer-scale GaAs and InAs whiskers *J. Appl. Phys.* 77 447–62

[21] Noguchi M, Hirakawa K and Ikoma T 1991 Intrinsinc electron accumulation layers on reconstructed clean InAs(100) surfaces *Phys. Rev. Lett.* 66 2243–6

[22] Walldrop J R 1984 Schottky-barrier height of ideal metal contacts to GaAs *Appl. Phys. Lett.* 44 1002–4

[23] Baca A G, Ren F, Zolper J C, Briggs R D and Pearton S J 1997 A survey of ohmic contacts to III–V compound semiconductors *Thin Solid Films* 308–309 599–606

[24] Braslav N 1981 Alloyed ohmic contacts to GaAs *J. Vac. Sci. Technol.* 19 803–7

[25] Gyalui J, Mayer J W, Rodriguez V, Yu A Y C and Gopen H J 1971 Alloying Behavior of Au and Au–Ge on GaAs *J. Appl. Phys.* 42 3578–85

[26] Kuan T S, Batson P E, Jackson T N, Rupprecht H and Wilkie E L 1983 Electron microscope studies of an alloyed Au/Ni–Au–Ge ohmic contact to GaAs *J. Appl. Phys.* 54 6952–7

[27] Taylor R P, Coleridge P T, Davies M, Feng Y, McCaffrey J P and Marshall P A 1994 Physical and
electrical investigation of ohmic contacts to AlGaAs/GaAs heterostructures J. Appl. Phys. 76 7966–72

[28] Gutsche C, Regolin I, Bleker K, Lysov A, Prost W and Tegude F J 2009 Controllable p-type doping of GaAs nanowires during vapor–liquid–solid growth J. Appl. Phys. 105 024305

[29] Dufouleur J, Colombo C, Garma T, Ketterer B, Uccelli E, Nicolot M and Fontcuberta I Morral A 2010 p-doping mechanisms in catalyst-free gallium arsenide nanowires Nano Lett. 10 1734–40

[30] Morkötter S et al 2015 Demonstration of confined electron gas and steep-slope behaviour in delta-doped GaAs–AlGaAs core–shell nanowire transistors Nano Lett. 15 3295–302

[31] Csontos D, Züllicke U, Brusheim P and Xu H Q 2008 Lande-like formula for the g factors of hole-nanowire subband edges Phys. Rev. B 78 033307

[32] Csontos D, Züllicke U, Brusheim P and Xu H Q 2009 Spin-3/2 physics of semiconductor hole nanowires: valence band mixing and tunable interplay between bulk-material and orbital bound-state spin splittings Phys. Rev. B 79 155323

[33] Winkler R 2003 Spin–Orbit Coupling Effects in Two-Dimensional Electron and Hole Systems (Berlin: Springer)

[34] Klochan O, Micolich A P, Ho L H, Hamilton A R, Muraki K and Hirayama Y 2009 The interplay between one-dimensional confinement and two-dimensional crystallographic anisotropy effects in ballistic hole quantum wires New J. Phys. 11 043018

[35] Chen J C H, Klochan O, Micolich A P, Hamilton A R, Martin T P, Ho L H, Züllicke U, Reuter D and Wieck A D 2010 Observation of orientation- and k-dependent Zeeman spin-splitting in hole quantum wires on (100)-oriented AlGaAs/GaAs heterostructures New J. Phys. 12 033043

[36] Srinivasan A, Yeeh L A, Klochan O, Martin T P, Chen J C H, Micolich A P, Hamilton A R, Reuter D and Wieck A D 2013 Using a tunable quantum wire to measure the large out-of-plane spin splitting of quasi two-dimensional holes in a GaAs nanostructure Nano Lett. 13 148–52

[37] Klochan O, Micolich A P, Hamilton A R, Trunov K, Reuter D and Wieck A D 2011 Observation of the Kondo effect in a spin-3/2 hole quantum dot Phys. Rev. Lett. 107 076805

[38] Klochan O, Chen J C H, Micolich A P, Hamilton A R, Muraki K and Hirayama Y 2010 Fabrication and characterization of an induced GaAs single hole transistor Appl. Phys. Lett. 96 092103

[39] Daun X, Huang Y, Cui Y, Wang J and Lieber C M 2001 Indium phosphate nanowires as building blocks for nanoscale electronic and optoelectronic devices Nature 409 66–9

[40] Pfünd A, Shorubalko I, Letcuq R and Ensslin K 2006 Top-gate defined double quantum dots in InAs nanowires Appl. Phys. Lett. 89 252106

[41] Casadei A, Krosgstrup P, Heiss M, Rühr J A, Colombo C, Ruelle T, Upadhyay S, Sørensen C B, Nygård J and Fontcuberta I Morral A 2013 Doping incorporation paths in catalyst-free Be-doped GaAs nanowires Appl. Phys. Lett. 102 013117

[42] Fontcuberta i Morral A, Colombo C, Abstreiter G, Arbiol J and Morante J R 2008 Nucleation mechanism of gallium-assisted molecular beam epitaxy growth of gallium arsenide nanowires Appl. Phys. Lett. 92 063112

[43] Colombo C, Spirkoska D, Frimmer M, Abstreiter G and Fontcuberta i Morral A 2008 Ga-assisted catalyst-free growth mechanism of GaAs nanowires by molecular beam epitaxy Phys. Rev. B 77 155326

[44] Storm K, Nylund G, Samuelson L and Micolich A P 2012 Realizing lateral wrap-gated nanowire FETs: controlling gate length with chemistry rather than lithography Nano Lett. 12 1–6

[45] Yoshie T, Bauer C L and Milnes A G 1984 Preparation and characterization of interfacial reactions between gold thin films and GaAs substrates Thin Solid Films 111 149–66

[46] Clarke W R, Micolich A P, Hamilton A R, Simmons M Y, Muraki K and Hirayama Y 2006 Fabrication of induced two-dimensional hole systems on (311)A GaAs J. Appl. Phys. 99 023707

[47] Sze S M and Ng K K 2006 The Physics of Semiconductor Devices 3rd edn (New York: Wiley)

[48] Manfra M J, Peeflter L N, West K W, de Picciotto R and Baldwin K W 2005 High mobility two-dimensional hole system in GaAs/AlGaAs quantum wells grown on (100) GaAs substrates Appl. Phys. Lett. 86 162106

[49] Masu K, Konagai M and Takahashi K 1983 Diffusion of beryllium into GaAs during liquid phase epitaxial growth of p-Ga0.2 Al0.8 As J. Appl. Phys. 54 1574–8

[50] Ilegems M 1977 Beryllium doping and diffusion in molecular-beam epitaxy of GaAs and AlGaAs J. Appl. Phys. 48 1278–87

[51] See A M et al 2012 Impact of small-angle scattering on ballistic transport in quantum dots Phys. Rev. Lett. 108 196807

[52] Lewis R A, Cheng T S, Henini M and Chamberlain J M 1996 Energy states of Be in GaAs Phys. Rev. B 53 12829–34

[53] Wharam D A, Pepper M, Ahmed H, Frost J E F, Hasko D G, Peacock D C, Ritchie D A and Jones G A C 1988 Addition of the one-dimensional quantised ballistic resistance J. Phys. C: Solid State Phys. 21 L887–91

[54] Heede S, Manolescu A, Nennes G A, Prost W, Schubert J, Grutzmacher D and Schapers T 2016 Adiabatic edge channel transport in a nanowire quantum point contact register Nano Lett. 16 4569–75