An FPGA-Based Fully Pipelined Bilateral Grid for Real-Time Image Denoising

Nobuho Hashimoto*, Shinya Takamaeda-Yamazaki†

The University of Tokyo

*hashimoto-nobuho949@g.ecc.u-tokyo.ac.jp, †shinya@is.s.u-tokyo.ac.jp

Abstract—The bilateral filter (BF) is widely used in image processing because it can perform denoising while preserving edges. It has disadvantages in that it is nonlinear, and its computational complexity and hardware resources are directly proportional to its window size. Thus far, several approximation methods and hardware implementations have been proposed to solve these problems. However, processing large-scale and high-resolution images in real time under severe hardware resource constraints remains a challenge.

This paper proposes a real-time image denoising system that uses an FPGA based on the bilateral grid (BG). In the BG, a 2D image consisting of x- and y-axes is projected onto a 3D space called a “grid,” which consists of axes that correlate to the x-component, y-component, and intensity value of the input image. This grid is then blurred using the Gaussian filter, and the output image is generated by interpolating the grid. Although it is possible to change the window size in the BF, it is impossible to change it on the input image in the BG. This makes it difficult to associate the BG with the BF and to obtain the property of suppressing the increase in hardware resources when the window radius is enlarged.

This study demonstrates that a BG with a variable-sized window can be realized by introducing the window radius parameter wherein the window radius on the grid is always 1. We then implement this BG on an FPGA in a fully pipelined manner. Further, we verify that our design suppresses the increase in hardware resources even when the window size is enlarged and outperforms the existing designs in terms of computation speed and hardware resources.

Index Terms—Image Processing, Denoising Filter, Bilateral Filter, Bilateral Grid.

I. INTRODUCTION

The bilateral filter (BF) is popularly used as an edge-preserving smoother in many image processing applications such as tone mapping [1], stylization [2], upsampling [3], and optical-flow estimation [4]. One of the most important applications is medical image denoising [5], [6] demonstrated that the quality of medical images such as X-Ray and CT significantly improved after they were processed using the BF. Although this procedure demands real-time responses for interactive operations, real-time processing is still difficult under the severe constraints of hardware resources for large-scale and high-resolution images.

Considering a two-dimensional 8-bit grayscale image $f : \Omega \rightarrow \mathbb{I}$ where $\Omega \subset \mathbb{N}^2$ is the domain of the image and $\mathbb{I} = \{i \mid i = 0, 1, \ldots, 255\}$ is the intensity range, the BF output

\[ f_{BF} : \Omega \rightarrow \mathbb{I} \] is given by

\[ f_{BF}(i) = \frac{1}{k_{BF}(i)} \sum_{j \in W(r,2)} g_{\sigma_s}(j) g_{\sigma_r}(f(i) - f(i-j)) f(i-j), \]  

(1)

where $k_{BF} : \Omega \rightarrow \mathbb{R}$ represents the normalization term

\[ k_{BF}(i) = \sum_{j \in W(r,2)} g_{\sigma_r}(j) g_{\sigma_r}(f(i) - f(i-j)), \]

$W(r, d) = [-r, r]^d$ represents a hypercube around the pixel of interest; $r \in \mathbb{N}$ and $d \in \mathbb{N}$ denote the window radius and dimension, respectively; and $g_{\sigma_s} : \mathbb{I}^2 \rightarrow \mathbb{R}$ and $g_{\sigma_r} : \mathbb{I} \rightarrow \mathbb{R}$ represent the Gaussian spatial and range kernels, respectively. Hereafter, $g_{\sigma}$ denotes the Gaussian function, where $\sigma$ is the standard deviation.

The range kernel provides edge-preserving characteristics; however, it makes the BF nonlinear, which causes difficulty in acceleration. If the BF is linear, we can easily apply the methods presented in [7], [8]. Therefore, some approaches have attempted to remove nonlinearity by quantizing the range space [9], [11], and by approximating the range kernel using trigonometric functions [12], [13], the Taylor polynomials [14], [15], and the DFT (Discrete Fourier Transform) [16]. Other approaches to acceleration also exist, wherein input images are projected onto the other smaller space such as the histogram [17], bilateral grid (BG) [18], and adaptive manifolds [19]. These approaches are often implemented on a GPU, but they are not as small-scale and energy-efficient as FPGA implementations [20]. Therefore, brute force FPGA implementations are proposed [21], [23]. The aforementioned approaches [12], [15], [17] have also been implemented on an FPGA [24], [26]. However, these implementations still have at least one of the following unsolved problems: low throughput, large memory footprint, and an increase in hardware resources depending on the window radius.

To solve these problems, this paper proposes a novel method for the BG [18] and its fast and small FPGA implementation for the BF on grayscale images. Here, the BG can suppress the increase in hardware resources, and an FPGA can achieve fast and small-scale implementation. Therefore, we realized a high throughput, low latency accelerator with a low memory footprint using noniterative and sequential processing. The major contributions of this study are summarized as follows.

1) The BG is enhanced so that the window size of input images can be varied.
2) The fully pipelined FPGA implementation is proposed for the proposed BG so that it can suppress the increase in the hardware resources.

3) The proposed design is implemented on an actual FPGA board, and it outperforms the other existing designs in terms of computation speed and hardware resources.

II. FPGA-based Bilateral Grid with a Variable-Sized Window

A. Bilateral Grid with a Variable-Sized Window

First, we attempt to change the BG window radius on an input image. The existing BG \[ \text{BG} \] does not consider the window radius on the input image, but on the grid. This makes it difficult to associate the BG with the BF, and to suppress the increase in hardware resources when the window radius is enlarged, because if the radius on the grid increases, the resources will increase in the same way as the original BF. By following the derivation of the existing BG, the output of the BG with a variable-sized window \( f_{BG} : \Omega \to \mathbb{R} \) is obtained by rewriting (1) as

\[
\begin{align*}
    f_{BG}(i) &= \frac{1}{k_{BF}(i)} \sum_{j \in W(i-2)} g_{\sigma}(j_{g}) grid([f_{v}(i) - j_{g}])[1], \\
    k_{BF}(i) &= \sum_{j \in W(1,3)} g_{\sigma}(j_{g}) grid([f_{v}(i) - j_{g}])[1],
\end{align*}
\]

where \( \sigma_{g} = \sigma_{s}/r \) denotes the standard deviation, \( k_{BG} : \Omega \to \mathbb{R} \) denotes the normalization term

\[
k_{BG}(i) = \sum_{j_{g} \in W(1,3)} g_{\sigma_{s}}(j_{g}) grid([f_{v}(i) - j_{g}])[0],
\]

\( f_{v} : \Omega \to \Delta(\subset \mathbb{R}^{3}) \) represents the feature vector

\[
f_{v}(i) = \left( \frac{i}{r}, \frac{j}{r}, \frac{k}{r} \right),
\]

and \( grid : \Gamma \to \mathbb{N}^{2} \) expresses the grid space; \( \Gamma \subset \mathbb{N}^{3} \) represents the set of lattice points in the grid, the second term of \( grid \) is the sum of the intensity values in the elements, and the first term is the number of pixels present. Here, the window radius in the last line in (2) is fixed at 1 to make the computation of the filtering easier and faster. To achieve this, while the output is maintained to be similar to the BF, all pixels in the BF window need to be included in the window of the proposed BG. Thus, we introduce \( r \), as shown in the second line in (2).

Then, the algorithm of the proposed BG (the last line in (2)) is described as

1) Initialization: \( \forall v \in \Gamma, grid(v) = (0, 0) \)
2) Grid Creation (GC): \( \forall i \in \Omega, grid([f_{v}(i)]) += (1, f_{v}(i)) \)
3) Gaussian Filter (GF): \( \forall v \in \Gamma, grid_{f}(v) = f_{GF}(v) \)
4) Trilinear Interpolation (TI): \( \forall i \in \Omega, f_{BG}(i) = f_{TI}(f_{v}(i)) \)

where \( f_{GF} : \Gamma \to \mathbb{R} \) represents the GF around the element of interest in the grid, \( grid_{f} : \Gamma \to \mathbb{R} \) denotes the grid after the GF, and \( f_{TI} : \Delta \to \mathbb{R} \) denotes the TI for the elements on \( grid_{f} \). Here, the function \( f_{GF} : \Gamma \to \mathbb{R} \) is given by

\[
f_{GF}(v) = \begin{cases} 0 & (k_{GF}(v) = 0) \\ \frac{1}{k_{GF}(v)} \sum_{w \in W(1,3)} g_{\sigma_{g}}(w) grid(v - w)[1] & \text{otherwise} \end{cases},
\]

Then, the function \( f_{TI} : \Delta \to \mathbb{R} \) is given by

\[
f_{TI}(p) = \left[ \sum_{i,j,k \in \{0,1\}} x_{i}y_{j}z_{k} \cdot grid_{f}([p] + (i, j, k)) \right],
\]

where \( x_{i}, y_{j}, z_{k} \) denote the coefficients

\[
(x_{i}, y_{j}, z_{k}) = [p] - [p] - (i, j, k).
\]

B. Overall Accelerator Architecture

The overall architecture of the FPGA-based BG with a variable-sized window is shown in Fig. 1. First, the input image pixels \((x, y)\) are read one by one from the DRAM using the AXI bus and DMA. The GC then converts the input image into the grid when each input pixel is read; therefore, the grid elements \((x, y, z)\) are filled in line by line. The output values of this operation are stored in BRAMs (Block RAMs) \text{grid}. Here, the values in \text{grid} must be read for the GC because the operation \( grid([f_{v}(i)]) += (1, f_{v}(i)) \) is performed. The GF then blurs the grid after a bare minimum of elements (3×3×3 cube around the element of interest) are prepared. Thus, it blurs one plane in the \( r \) lines of the input image. The output values of this operation are stored in BRAMs \text{grid} \_ \text{f}. Because the input of the TI is a feature vector \((3)\) of the pixel of interest, the input image must be stored in BRAMs \text{lb} (line buffer). Finally, the TI is executed after a bare minimum of elements (eight nearest elements around the point of interest) are blurred by the GF. Therefore, \( r \) lines of the output image are obtained per \( r \) lines of the input image.

C. Hardware Optimization

Here, we focus on a \( w \times h \) 8-bit grayscale image. For the sake of simplicity, this paper does not explain corner cases in detail, such as the leftmost and rightmost lines; however,
Fig. 2: Illustration of read-modify-write removal and bit expression of $grid^{2D}(x, y)$.

in essence, these can be implemented similarly to the other cases.

As derived from (3) and (5), the domain of the grid is defined as

$\{ (x, y, z) \mid x = 0, 1, \ldots, gx-1, y = 0, 1, \ldots, gy-1, z = 0, 1, \ldots, gz-1 \}$,

where the constants $gx$, $gy$, and $gz$ denote

$\left( \left\lfloor \frac{h}{r} \right\rfloor + 2, \left\lfloor \frac{w}{r} \right\rfloor + 2, \left\lfloor \frac{255}{r\sigma_f / \sigma_s} \right\rfloor + 2 \right)$.

To separate the input image, we define $gg$ and $gi$ as

$gg(x, y) = \left\{ (ix, iy) \mid \left( \left\lfloor \frac{ix}{r} \right\rfloor, \left\lfloor \frac{iy}{r} \right\rfloor \right) = (x, y) \right\}$

$gi(x, y) = \left\{ (ix, iy) \mid \left( \left\lfloor \frac{ix}{r} \right\rfloor, \left\lfloor \frac{iy}{r} \right\rfloor \right) = (x, y) \right\}$,

so that all pixels in $gg(x, y)$ are projected onto the grid elements with the same x- and y-components $grid(x, y, *)$ and all pixels in $gi(x, y)$ require the $gridi$ elements with the same x- and y-components $grid_i(x, y, *)$ for the TI. Hereafter, the notation asterisk * is used as a wildcard; for example, $grid(x, y, *)$ denotes $\{grid(x, y, z) \mid z = 0, 1, \ldots, gz-1 \}$.

The overall pseudo code is shown in Algorithm 1 where $L_1$, $L_2$, and $L_3$ are LUTs. We note that Algorithm 1 expects (6), which will be defined later in section II-C2 is satisfied for II = 1 implementation.

1) Read-Modify-Write Removal on BRAM: For real-time processing, an FPGA design whose II (Initiation Interval) is 1 is desired. However, because $grid$ is stored in BRAMs, the read-modify-write operation $grid([fv(i)]) += (1, f(i))$ in the GC cannot be achieved in II = 1. Here, by exploiting the characteristics that the accesses to $grid$ are not random but regular and local to some extent, this operation can be accelerated. The x- and y-components of $fv(i)$ change regularly as input values are read, and therefore, they can be expressed by counters ($\ell$. 36 to 45 in Algorithm 1). However, the z-component of $fv(i)$ remains unknown until $f(i)$ is read. Therefore, as shown in Fig. 2 to update the elements $grid(x, y, *)$, the best solution would be to load $grid(x, y, *)$ onto registers $grid_z$ when processing the first pixel of each row in $gg(x, y)$ ($\ell$. 12 to 15 in Algorithm 1), update them on registers $grid_z$ ($\ell$. 16 in Algorithm 1), and store them back to BRAMs after processing the last pixel of the row in $gg(x, y)$ ($\ell$. 17 to 18 in Algorithm 1). We note that the update operation on registers can be achieved in II = 1. In this manner, the read-modify-write operation is removed.

Algorithm 1 Calculation of the BG on an FPGA.

Input: $f$: input image
Output: $f_{BG}$: output image filtered by the BG

1: // Initialization
2: $cx, py, cy \leftarrow r - \lfloor r/2 \rfloor - 1, 0, r - \lfloor r/2 \rfloor - 1$
3: $grid^{2D}[\ast][\ast] \leftarrow 0$
4: for $x \leftarrow 0$ to $(h-1)+2r+\lfloor r/2 \rfloor$ do
5:    for $y \leftarrow 0$ to $w-1$ do
6:        // GC (while there are still input pixels)
7:        if $x < h$ then
8:            $l \leftarrow f(x, y)$
9:            $pz \leftarrow L_1[\ell]$
10:        $gl \leftarrow (1, l)$
11:        $lb.enqueue(l)$
12:        if $(x, y)$ is the upper left corner of any $gg$ then
13:            $grid_z \leftarrow 0$
14:        else if $(x, y)$ is the left end of any $gg$ then
15:            $grid_z \leftarrow grid^{2D}[\[2][py]$  
16:        $grid_z[pz] \leftarrow grid_z[pz] + gl$
17:        if $(x, y)$ is the right end of any $gg$ then
18:            $grid^{2D}[\[2][py] \leftarrow grid_z$
19:        // GF ($gy \times gz$ times for each plane
20:        // after necessary data is prepared)
21:        if $grid^{2D}[\[1]$ completed then
22:            $cnt_y, cnt_z \leftarrow 0, 0$
23:        if $cnt_y >= gy \land cnt_z >= 0$ then
24:            $gf[\text{cnt}_z] \leftarrow \text{fgf}(2, cnt_y, cnt_z)$
25:        if $cnt_z >= gz-1$ then
26:            $grid_{f^{2D}}[\{\text{cnt}_z] \leftarrow gf$
27:            Shift $grid^{2D}[\ast][\text{cnt}_y + 2$ and regGF
28:        $cnt_y, cnt_z \leftarrow cnt_y + 1, 0$
29:        else
30:            $cnt_z \leftarrow cnt_z + 1$
31:        // TI (after two planes of $grid^{2D}$ completed)
32:        if $x >= 2r + \lfloor r/2 \rfloor$ then
33:            $f_{BG}(x-2r-[r/2], y) \leftarrow f_{TI}(L_2[\text{cx}], L_3[\text{cy}], lb.dequeue())$
35:        Load or Shift $grid^{2D}$ and regTI if necessary
36:        // Update counters
37:        if $y >= w-1$ then
38:            if $cx = r-1$ then
39:                $cx, py, cy \leftarrow cx + 1, 0, r-\lfloor r/2 \rfloor - 1$
40:            else
41:                $cx, py, cy \leftarrow 0, 0, r-\lfloor r/2 \rfloor - 1$
42:        else if $cy = r-1$ then
43:            $py, cy \leftarrow py + 1, 0$
44:        else
45:            $cy \leftarrow cy + 1$
Fig. 3: Data layout of $gridD^2$, $gridD^2$, and $lb$. The arrows represent data dependencies. The boxes surrounded by solid lines indicate the memory usage required for the proposed design.

![Diagram](image)

(a) GF is sufficiently short.

(b) GF is sufficiently long.

Fig. 4: Possible pipeline cases when $r = 3$. $GC(x)$ expresses the GC to generate $gridD^2(x, *); GF(x)$ expresses the GF to generate $gridD^2(x, *); TI(x)$ expresses the TI to generate $gi(x, *)$ in the output. 1) indicates that 0 and 1 are loaded onto $regGF$ directly from $gridD^2$. 2) indicates that 1 can be loaded one clock after 0 because the first pixel can be interpolated by only 0.

The suitable data structure for the grid is a 2D space $gridD^2$ with x- and y-axes, because all elements in the z-axis direction with a certain x- and y-components must be loaded and stored together. We note that each $(x, y)$ element in $gridD^2$ expresses $grid(x, y, *)$, which means the value in $gridD^2(x, y)$ is expressed as a bit combination of

\[
grid(x, y, gz - 1)[0], grid(x, y, gz - 1)[1],
grid(x, y, gz - 2)[0], grid(x, y, gz - 2)[1],
\ldots, grid(x, y, 0)[0], \text{ and } grid(x, y, 0)[1]
\]

in this order (see Fig. 2). Hereafter, the notation $gridD^2(x, y)$ is used instead of $grid(x, y, *)$ to simplify the explanations and improve ease of understanding.

2) Pipeline: For further performance improvement, three for loops of the GC, GF, and TI are pipelined together, which means they are unified into one for loop. Because the GF is executed for each grid element and the GC and TI are executed for each input image pixel, the number of executions of the GF $gz \times gy \times gz$, is different from that of the GC and TI, $w \times h$. Moreover, these processes are dependent on each other.

![Diagram](image)

Fig. 5: Accesses to grid by the GC and GF. The direction of the arrows indicates where the data are loaded and stored. The numbers in $gridD^2$ correspond to those in registers $regGF$. The dashed boxes (1, 2, and 3) no longer exist in $gridD^2$. The GC does not access 12 in this situation.

Therefore, hardware-level pipeline of such heterogeneous processes is challenging. Fig. 3 shows the data dependencies and memory usage, which is much smaller than one whole image. $gridD^2$ is defined in the same way as $gridD^2$, and hereafter, $gridD^2(x, y)$ is used instead of $gridD^2(x, y, *)$. Here, we focus on the GF of the plane $gridD^2(x, *)$ in the grid. The nine lines around the line of interest should be loaded onto registers from BRAMs before the line is processed. Thus, this operation can start after the generation of the second line $gridD^2(x + 1, 1)$. Furthermore, this operation should be completed before the last line $gridD^2(x, gy - 1)$ is loaded, which is required for the TI. Therefore, if

\[
gy \times gz < 2w - \left\lfloor \frac{r}{2} \right\rfloor - r - (w \mod r),
\]

holds, the GF can finish in time, as shown in Fig. 4a. Otherwise, as shown in Fig. 4b, the GC is delayed by suspending the input until it can restart. The TI is then processed $(r + \left\lfloor \frac{r}{2} \right\rfloor)$ lines behind the GC. In this manner, the pipeline between the set of processes ($GC(x)$, $GF(x - 1)$, and $TI(x - 2)$) are designed, which is called macro pipeline, and at the same time, the pipeline within the set of processes are also performed, which is called micro pipeline. This nested pipeline structure greatly accelerates our design.

3) Other Optimizations: We also partition the BRAMs to remove structural hazards. At most two load and / or store operations are allowed in one BRAM in one clock. The accesses to grid and gridf are shown in Figs. 5 and 6 respectively. Therefore, grid and gridf should be partitioned into three and two by plane such that each partition is not accessed more than twice. In terms of $lb$, because the input pixels are directly stored and the stored data are loaded for the TI in the same order, $lb$ is implemented as FIFO without causing structural hazards. Therefore, all structural hazards are removed, and II = 1 implementation is achieved in the proposed design.
Finally, the arithmetic units are minimized. To remove floating-point arithmetic, we utilize a simple approach to multiply each value by a power of two, which can be implemented as shift operations. Then, the GF (1) and TI (2) can be calculated as shown in Figs. 7 and 8, respectively. We note that the numerator and denominator in the GF can be calculated as shown in Figs. 7 and 8, respectively. We use the criterion MSSIM (Mean Structural SIMilarity index) proposed by [27]. The MSSIM corresponds to human visual perception to a higher degree than the other criteria, such as the PSNR (Peak Signal-to-Noise Ratio). The hyperparameters $C_1$ and $C_2$ are fixed as $(0.01×255)^2$ and $(0.03×255)^2$, respectively, and $7×7$ square window is used (see [27] for more details).

The denoising quality is better if the MSSIM value is larger, and the maximum value is 1.0. If the value is 1.0, the two pictures are identical.

First, from the original picture (Fig. 9a), the noised picture (Fig. 9b) is created by adding Gaussian noise with a standard deviation of 30. Then, the noised picture is processed using the two filters to obtain denoised pictures (Fig. 10). Finally, we calculate the MSSIM values between the denoised pictures and the original picture. The results are obtained by changing $r$, $\sigma_r$, and $\sigma_s$.

As shown in Fig. 12, the MSSIM values obtained from the
BF are larger than those obtained from the BG. However, by selecting proper parameters, the BG shows equivalent denoising quality in terms of the MSSIM. Moreover, Fig. 11 indicates that the BG shows equal or better denoising quality compared to the BF.

\section{Computation Speed and Hardware Resources}

First, the computation speed and hardware resources of the proposed design are evaluated as shown in Table I where $f_{clk}$ and $fps$ denote the maximum clock frequency and actual maximum frame rate, respectively. The maximum clock frequency $f_{clk}$ is obtained by measuring the execution time per frame $T_f$ by $\frac{1}{fps}$ on the ZCU 104 board. The $fps$ values are almost the same as the theoretical values. The rest of the items are obtained from the actual implementation results in the Vivado.

In the proposed design, as shown in Table I, the computation speed is sufficiently high in full HD images, and the speed is almost the same and independent of $r$. However, when $r$ is 4, the design runs slightly slowly because it does not hold, and extra clocks are required to finish the GF. Further, it is inferred that the consumption of hardware resources remains almost the same when $r$ increases.

Next, we compare the speed and resources of our design, a GPU implementation of the BF, and other existing implementations: (1) ICCEE 2008 [22], (2) TIE 2014 [23], and (3) TIE 2018 [25]. Our design and (3) have the characteristics wherein the consumption of hardware resources does not increase when $r$ is enlarged; however, (1) and (2) do not have the characteristics.

The results are shown in Table II where $f_{clk}$ and $T_p$ denote the maximum clock frequency and elapsed time per pixel, respectively. Here, we use estimated values for the frame rates of (1) to (3) (refer to the original papers for more details), because the actual values are not shown. As for the GPU implementation, we use one of the highest performance GPUs: A100 PCIe from NVIDIA. We also use the cv::cuda::bilateralFilter function in OpenCV 4.5.1 for C++ implementation and g++ 9.3.0 as a compiler.

As most of the filters are implemented on different FPGA boards, parameters, and sizes of images, the comparison of the speed of these implementations may be less significant. However, several insights can be obtained from these results. The elapsed time per pixel suggests that our design is the fastest of the five implementations, at least in this scenario, and ours is reasonably fast for real-time processing of large-scale and high-resolution images. In contrast, (1) can also process images relatively fast, but the resources increase in proportion to the square of $r$; (2) and (3) are much slower than our design.

As there are N/A cells in the table, the comparison of hardware resources may be incomplete. However, the results suggest that our design consumes a small number of BRAMs and DSPs, even though $r$ is large. In contrast, slice, LUT, and FF usage are not small compared with (3), but considering that our design runs sufficiently fast for real-time processing, it is acceptable because our design consumes a small percentage of resources on the ZCU 104 board, which is a relatively small-scale board. These outstanding characteristics are the result of highly parallelized and deeply pipelined implementation.

\section{Conclusion}

In this paper, we provide a detailed explanation of the BG with a variable-sized window and its fully pipelined FPGA implementation. The advantages of the proposed design are summarized as follows.

1) The BG is enhanced so that the window size of input images can be varied.
2) The fully pipelined FPGA implementation is proposed for the proposed BG so that it can suppress the increase in the hardware resources.

3) The proposed design is implemented on an actual FPGA board, and it outperforms the other existing designs in terms of computation speed and hardware resources.

Moreover, there is some room for improvement in the proposed design, especially in terms of the sensitivity of its output to the variations in the parameters used and its application to higher memory bandwidth. This sensitivity can be reduced by further enhancing the BG algorithm with a variable-sized window. Furthermore, the adverse effects caused by sensitivity can be alleviated by selecting the best parameters in terms of their MSSIM values. Here, a higher memory bandwidth implies that more than one pixel is read and processed together. Therefore, the implementation requires some changes, although the basic theory remains the same.

ACKNOWLEDGMENT
This work is supported in part by JSPS KAKENHI 19H04075 and 18H05288, and JST PRESTO JPMJPR18M9.

REFERENCES
[1] F. Durand and J. Dorsey, “Fast bilateral filtering for the display of high-dynamic-range images,” in Annual Conference on Computer Graphics and Interactive Techniques (SIGGRAPH). Association for Computing Machinery, 2002, p. 257–266.
[2] H. Winnemöller, S. C. Olsen, and B. Gooch, “Real-time video abstraction,” ACM Transactions on Graphics (TOG), vol. 25, no. 3, p. 1221–1226, 2006.
[3] J. Kopf, M. Uyttendaele, O. Deussen, and M. F. Cohen, “Capturing and viewing gigapixel images,” ACM Transactions on Graphics (TOG), vol. 26, no. 3, p. 93–es, 2007.
[4] J. Xiao, H. Cheng, H. Sawhney, C. Rao, and M. Isard, “Bilateral filtering-based optical flow estimation with occlusion detection,” in European Conference on Computer Vision (ECCV). Springer Berlin Heidelberg, 2006, pp. 211–224.
[5] F. Hannig, M. Schmid, J. Teich, and H. Hornegger, “A deeply pipelined and parallel architecture for denoising medical images,” in IEEE International Conference on Field-Programmable Technology (FPT), 2010, pp. 485–490.
[6] J. C. R. Giraldo, Z. S. Kelm, L. S. Guimaraes, L. Yu, J. G. Fletcher, B. J. Erickson, and C. H. McCollough, “Comparative study of two image space noise reduction methods for computed tomography: Bilateral filter and nonlocal means,” in Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBS), 2009, pp. 3529–3532.
[7] I. T. Young and L. J. van Vliet, “Recursive implementation of the Gaussian filter,” Signal Processing, vol. 44, no. 2, pp. 139–151, 1995.
[8] R. Deriche, “Recursively implementing the Gaussian and its derivatives,” INRIA Research Report RR-1893, 1993.
[9] Q. Yang, K. Tan, and N. Ahuja, “Real-time O(1) bilateral filtering,” in IEEE Conference on Computer Vision and Pattern Recognition (CVPR), 2009, pp. 557–564.
[10] Q. Yang, N. Ahuja, and K.-H. Tan, “Constant time median and bilateral filtering,” International Journal of Computer Vision (IJCV), vol. 112, no. 3, pp. 307–318, 2015.
[11] P. Nair and K. N. Chaudhury, “Fast high-dimensional filtering using clustering,” in IEEE International Conference on Image Processing (ICIP), 2017, pp. 240–244.
[12] K. N. Chaudhury, D. Sage, and M. Unser, “Fast O(1) bilateral filtering using trigonometric range kernels,” IEEE Transactions on Image Processing (TIP), vol. 20, no. 12, pp. 3376–3382, 2011.
[13] K. N. Chaudhury, “Acceleration of the shiftable O(1) algorithm for bilateral filtering and nonlocal means,” IEEE Transactions on Image Processing (TIP), vol. 22, no. 4, pp. 1291–1300, 2013.
[14] F. Porikli, “Constant time O(1) bilateral filtering,” in IEEE Conference on Computer Vision and Pattern Recognition (CVPR), 2008, pp. 1–8.
[15] K. N. Chaudhury and S. D. Dabhade, “Fast and provably accurate bilateral filtering,” IEEE Transactions on Image Processing (TIP), vol. 25, no. 6, pp. 2519–2528, 2016.
[16] P. Nair, A. Popli, and K. N. Chaudhury, “A fast approximation of the bilateral filter using the discrete fourier transform,” Image Processing On Line (IPOL), vol. 7, pp. 115–130, 2017.
[17] B. Weiss, “Fast median and bilateral filtering,” ACM Transactions on Graphics (TOG), vol. 25, no. 3, p. 519–526, 2006.
[18] J. Chen, S. Paris, and F. Durand, “Real-time edge-aware image processing with the bilateral grid,” ACM Transactions on Graphics (TOG), vol. 26, no. 3, p. 103–es, 2007.
[19] E. S. L. Gastal and M. M. Oliveira, “Adaptive manifolds for real-time high-dimensional filtering,” ACM Transactions on Graphics (TOG), vol. 31, no. 4, pp. 33:1–33:13, 2012.
[20] F. Hannig, M. Schmid, J. Teich, and H. Hornegger, “A deeply pipelined and parallel architecture for denoising medical images,” in IEEE International Conference on Field-Programmable Technology (FPT), 2010, pp. 485–490.
[21] H. Dutta, F. Hannig, J. Teich, B. Heigl, and H. Hornegger, “A design methodology for hardware acceleration of adaptive filter algorithms in image processing,” in IEEE International Conference on Applications-Specific Systems, Architectures and Processors (ASAP), 2006, pp. 331–340.
[22] T. Q. Vinh, J. H. Park, Y. Kim, and S. H. Hong, “FPGA implementation of real-time edge-preserving filter for video noise reduction,” in International Conference on Computer and Electrical Engineering (ICCEE), 2008, pp. 611–614.
[23] A. Gabiger-Rose, M. Kube, R. Weigel, and R. Rose, “An FPGA-based fully synchronized design of a bilateral filter for real-time image denoising,” IEEE Transactions on Industrial Electronics (TIE), vol. 61, no. 8, pp. 4093–4104, 2014.
[24] C. Pal, K. N. Chaudhury, A. Samanta, A. Chakrabarti, and R. Ghosh, “Hardware software co-design of a fast bilateral filter in FPGA,” in Annual IEEE India Conference (INDICON), 2013, pp. 1–6.
[25] S. D. Dabhade, G. N. Rathna, and K. N. Chaudhury, “A reconfigurable and scalable FPGA architecture for bilateral filtering,” IEEE Transactions on Industrial Electronics (TIE), vol. 65, no. 2, pp. 1459–1469, 2018.
[26] M. Igarashi, M. Ikebe, S. Shimoyama, K. Yamano, and J. Motohisa, “O(1) bilateral filtering with low memory usage,” in IEEE International Conference on Image Processing (ICIP), 2010, pp. 3301–3304.
[27] Zhou Wang, A. C. Bovik, H. R. Sheikh, and E. P. Simoncelli, “Image quality assessment: from error visibility to structural similarity,” IEEE Transactions on Image Processing (TIP), vol. 13, no. 4, pp. 600–612, 2004.