A D-Band Dual-Mode Dynamic Frequency Divider in 130-nm SiGe Technology

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Abstract—In this work, a dual-mode (divide-by-2 and divide-by-3) dynamic frequency divider is presented. A tunable delay gated ring oscillator (TDGRO) topology is proposed for dual-mode operation and bandwidth extension. It uses a 130-nm gate length SiGe BiCMOS technology with the \( f_t \) and \( f_{max} \) of 250 and 370 GHz, respectively. Verification shows that it works at W-band from 70 to 114 GHz (47.8% bandwidth) for divide-by-2 and works at D-band from 105 to 160 GHz (41.5% bandwidth) for divide-by-3. This divider can be used in integrated phase-locked loops (PLLs) at millimeter-wave frequencies.

Index Terms—BiCMOS, D-band, dual-mode, dynamic, frequency divider, millimeter-wave, SiGe, W-band.

I. INTRODUCTION

MILLIMETER-WAVE and terahertz bands offer wide bandwidth for high-speed communication systems. In a millimeter-wave communication system, high-frequency synthesizer (e.g., phase-locked loop) and carrier recovery blocks are essential parts at the receiver side. The frequency divider, voltage-controlled oscillators, and phase detectors are critical components of a millimeter-wave frequency synthesizer.

A dual-mode divider that can divide the input frequency either by-2 or by-3 can offer flexibility for millimeter-waveband synthesizer as the first divider stage. It allows a wide input frequency range to be converted into the same output frequency band, so it is less demanding on the bandwidth of the subsequent divider stage. Dual-mode operation is often implemented with tunable capacitors included in the injection-locked frequency divider circuit. In letter [1], a pair of switched capacitors is used as a capacitive load. When the switched capacitor is by-passed, the divider is in the divide-by-2 mode. When the switch is on, the capacitor shifts the resonator frequency of the tank, so the divider is switched to the divide-by-3 mode. The dual-mode operation can also be made by changing varactors [2]–[4] and active inductance [5].

For previously reported dual-modulus dividers, their locking range is often narrow (several gigahertz) and their input frequencies are relatively low (below 20 GHz). For divide-by-3-only dividers, the highest input frequency reaches D-band; however, the operational bandwidth is smaller than 20 GHz.

In this letter, a tunable delay gated ring oscillator (TDGRO) topology is proposed for dual-mode operation and bandwidth extension. A TDGRO dynamic frequency divider is designed and implemented for both divide-by-2 and divide-by-3, with a wide input frequency range of 70–160 GHz. For input frequency between 70 and 114 GHz, the divider operates as divide-by-2, and therefore, the output is in 35–57 GHz. For input frequency between 105 and 160 GHz, the divider operates as divide-by-3 and the output is in 35–53.3 GHz. By toggling between operation modes, the output frequency lies in the same frequency band for a wide input frequency range.

Previously published relevant works [1]–[10], [12]–[14] are summarized in Table I, and the proposed frequency divider demonstrates the highest input frequency (160 GHz) among the dividers that have dual-modulus, divide-by-2 and divide-by-3, with a state-of-the-art operational bandwidth (41.5%) among divide-by-3 dividers.

II. TDGRO DYNAMIC FREQUENCY DIVIDER

A TDGRO dynamic frequency divider topology is proposed in this work. A simplified functional diagram of the proposed TDGRO dynamic frequency divider is shown in Fig. 1. A TDGRO comprises two gated differential amplifiers (denoted as Amp1 and Amp2) with feedback connections to form a ring oscillator configuration. The delays between amplifiers, denoted as \( \tau \), are tunable with current in order to switch the division modes. The two amplifiers are gated by...
an input clock voltage and Amp1 and Amp2 are turned on at high/low voltage. A similar structure has been used in a divide-by-2 frequency divider [11].

To explain the operation principle of the proposed divider, four nodes A, B, C, and D are marked in Fig. 1, which can be either at a high voltage state or a low voltage state. Assume low-voltage states at nodes A, B, C, and D as an initial state. With a high clock voltage, Amp1 operates and makes node B as an opposite state of that at node A with a delay $\tau_{AB}$. This state is passed to node C with a delay $\tau_{BC}$. When a low clock voltage occurs, Amp2 passes this state to node D with a delay $\tau_{CD}$, and the state is further passed back to node A with another delay $\tau_{DA}$. There is a restriction: the state can only be passed to nodes B and D within the positive and negative clock periods, respectively. Considering the circuit symmetry, assume $\tau_{AB} + \tau_{BC} = \tau_{CD} + \tau_{DA} = \tau$, $\tau_{AB} = \tau_{CD} \ll \tau_{BC} = \tau_{DA}$.

When divide-by-2, the voltage waveform at input and output nodes (A, B, C, and D) of Amp1 and Amp2 is depicted in Fig. 2(a). Every two periods of input clock is divided into four time slots for a clear explanation. To achieve a divide-by-2 function, the state of node A needs to rise and fall within two clock periods (four time slots), which means the falling edge is in slot ④, and the rising edge is in slot ②. The minimum time for node A to change a state is $\tau_{AB} + \tau_{BC} + \tau_{CD} + \tau_{DA} = 2\tau$. The timing constraints can be expressed as $4\tau \leq 2T$. As long as $\tau \leq T/2$, nodes B and D can always change status during the positive and negative clock periods, respectively. The maximum divide-by-2 operation frequency is

$$f_{\text{div}2} \leq \frac{0.5}{\tau}. \quad (1)$$

For divide-by-3 operation, the voltage waveforms are illustrated in Fig. 2(b). Every three periods of input clock is divided into six time slots for a clear explanation. Assume again low voltage at nodes A, B, C, and D as an initial state. To achieve divide-by-3 function, the state of node A needs to rise and fall within three clock periods, which means the falling edge needs to be in the time slot ⑧, and the rising edge needs to be in the time slot ③. These timing constraints can be expressed as $4\tau \leq 3T$. Also, $\tau$ is bigger than $T/2$; otherwise, the divider operates divide-by-2. As a result, $0.5T \leq \tau \leq 0.75T$.

The falling edge of node A is in slot ⑧, so the falling edge of node C must be before slot ⑧. The state of node C can only be passed to node D during a negative clock period. In this case, the falling edge of node D is in slot ⑧, and the rising edge of node D is in slot ③. The timing constraints can be expressed as

$$\begin{cases} 1.5T \leq 3\tau \leq 2T \\ 2.5T \leq 4\tau \leq 3T. \end{cases} \quad (2)$$

As a result, $0.625T \leq \tau \leq 0.67T$. The divide-by-3 frequency range can be written as

$$0.625/\tau < f_{\text{div}3} < 0.67/\tau. \quad (3)$$

From (1) and (3), it can be seen that for a given delay $\tau$, the maximum working frequency can be improved by a third with the same $\tau$. The delay $\tau$ is limited by the semiconductor process and the layout.

Fig. 3 shows the schematic of the proposed frequency divider. Q1 and Q2 formed Amp 1, gated by Q9. Q3 and Q4 formed Amp 2, gated by Q10. Q11–Q13 are the clock input stages, with Q14–Q16 being the complimentary stages. Q5–Q8 are emitter followers for interamplifier buffer with Q17–Q20 are their current mirrors.

For a bipolar junction transistor, when the current $I_C$ changes, the delay $\tau_{bc}$ between the base and the emitter and $\tau_{pc}$ between the base and the collector are changed accordingly. In this case, the delay between the two latches is tunable. The total delay $\tau$ consists of a tunable delay from transistors and a fixed delay from the inevitable transmission line in layout. The electric delay of the transmission line is 0.4 ps, which is...
calculated by using the HFSS simulation. The tunable delay is estimated by observing the time delay between the signals at the input of the first latch (base of Q1) and the input of the second latch (base of Q4) when the divider is free running. The simulated tunable delay with different bias conditions is shown in Fig. 4. The total delay \( \tau \) can be tuned from 3.6 to 5.4 ps.

By using different bias voltages of \( V_{ee} \), the working frequency of the proposed divider is shifted. With a fixed bias point, the output frequency locking range is fixed, which means the input frequency is selected by bias point. With different input frequencies, the division modulus can be chosen by using different bias voltages of \( V_{ee} \). The circuit has only two biases, \( V_{ee} \) and \( V_b \), supplied at −3 and −1.8 V, respectively. A photograph of the circuit is shown in Fig. 5. The chip size is 530 \( \mu \)m \( \times \) 460 \( \mu \)m, including probing pads.

### III. Measurement Results

The circuit is characterized on-wafer using a Cascade MPS150 probe station. The frequency-domain measurement was performed using a Keysight network analyzer (N5247A PNA-X) and Virginia Diodes, Inc. (VDI) millimeter-wave extenders. Single-ended ground-signal-ground (GSG) and dc probes with 100-\( \mu \)m pitch were used for RF and dc connection, respectively. Three parameters are measured: output power, output spectrum, and input sensitivity.

In Fig. 6, the output power over different input frequencies is represented. The input power is constant −1 dBm. The working frequency range for the proposed frequency divider is 70–160 GHz. By sweeping the bias voltage, the emitter current is changed accordingly. The wide locking bandwidth is covered for both divide-by-2 and divide-by-3 function modes. The bias voltages and currents of the corresponding working frequency are also shown in Fig. 6. For a single bias point, the widest locking range for divide-by-2 is 17.2 GHz, from 97.4 to 114.6 GHz, when \( V_{ee} \) is −3.05 V, and \( I_{ee} \) is 50 mA. The widest locking range for divide-by-3 is 7.2 GHz, from 132 to 139.2 GHz, when \( V_{ee} \) = −2.73 V, and \( I_{ee} \) = 20 mA.

DC power consumption varies from 26 to 180 mW. When the \( V_{ee} \) is −2.6 V, and \( I_{ee} \) is only 10 mA, the proposed divider gives a low output frequency. For the divide-by-3 setting, the divider works from 107.4 to 110 GHz. For the divide-by-2 setting, the divider works from 70 to 76.2 GHz.

Fig. 7 shows the measured single-ended output spectrum of the divider in divide-by-3 and divide-by-2 mode when the input signal frequency was set at 159 and 111 GHz, respectively. The corresponding input power is −1 and −2.3 dBm. The output spectrum is shown with the frequency spans of 5 MHz and 70 GHz. The input power sensitivity curve of the proposed divider is shown in Fig. 8. The solid red curve represents the input sensitivity of the divide-by-2 mode, while the blue dashed curve represents the input sensitivity in the divide-by-3 mode.

### IV. Conclusion

A TDGRO dynamic frequency divider is demonstrated in this letter. The proposed divider can operate in a divide-by-2 or a divide-by-3 mode. The operating frequency ranges are from 70 to 114 GHz and from 105 to 160 GHz for the two modes. Compared with the recently published frequency dividers given in Table I, the proposed frequency divider demonstrates the highest frequency among the dividers that divide both by-2 and by-3. The proposed divider in the divide-by-3 mode has also the widest bandwidth of 55 GHz.
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