GRIP: A Graph Neural Network Accelerator Architecture

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Abstract—We present GRIP, a graph neural network accelerator architecture designed for low-latency inference. Accelerating GNNs is challenging because they combine two distinct types of computation: arithmetic-intensive vertex-centric operations and memory-intensive edge-centric operations. GRIP splits GNN inference into a fixed set of edge- and vertex-centric execution phases that can be implemented in hardware. We then specialize each unit for the unique computational structure found in each phase. For vertex-centric phases, GRIP uses a high performance matrix multiply engine coupled with a dedicated memory subsystem for weights to improve reuse. For edge-centric phases, GRIP uses multiple parallel prefetch and reduction engines to alleviate the irregularity in memory accesses. Finally, GRIP supports several GNN optimizations, including a novel optimization called vertex-irregularity in memory accesses. GRIP is efficient across a wide range of models and has numerous hardware optimizations to improve circuit testability for EDA [32]. Evaluated across several benchmark graphs, it reduces 99th percentile latency by a geometric mean of $17 \times$ and $23 \times$ compared to a CPU and GPU baseline, respectively, while drawing only $5 \text{W}$.

Index Terms—Deep Learning; Hardware Acceleration; Algorithm-Hardware co-Design; ASIC;

I. INTRODUCTION

Traditional deep neural networks (DNNs) rely on regularly structured inputs (e.g. vectors, images, or sequences) making them difficult to use in domains where data is naturally irregular (e.g. user connections on social media). Graph neural networks (GNNs) tackle this limitation by extending DNNs to allow arbitrarily structured graph-valued inputs, where feature vectors are associated with the edges and vertices of a graph. GNNs have found significant success in a range of practical tasks, including surfacing related content on social media [46], recommending meals on delivery platforms [24], and improving circuit testability for EDA [32].

GNNs combine two distinct types of operations [17], [31]: vertex-centric, which are associated with graph vertices, and edge-centric, which are associated with edges. Vertex-centric operations are computationally regular and primarily consist of multiplying vertex feature vectors by large weight matrices. These weights are shared across all vertices, leading to significant opportunities for data reuse. Edge-centric operations are similar to those found in graph analytics (e.g. neighborhood reduction [42]). Their computational structure depends on the often sparse and irregular structure of the input graph. This results in many random memory accesses and limited data reuse, but also requires relatively little computation.

The combination of these two types of computation makes GNN inference inefficient on existing architectures. As a result, GNNs have much higher inference latency than other neural networks, limiting them to applications where inference can be pre-computed offline [46]. Most DNN accelerators (e.g. the TPU [25]) are optimized for dense, regular computation, making edge operations hard to implement efficiently [3]. Graph analytics accelerators (e.g Graphicionado [20]) are designed for workloads that require little computation per-vertex and have difficulty exploiting data reuse in vertex-centric operations. Prior work has demonstrated inference on CPUs and GPUs is limited by architectural issues, such as cache and memory bandwidth bottlenecks [19], [45].

This paper proposes GRIP (GRaph Inference Processor), an accelerator architecture designed for low-latency GNN inference. GRIP’s programming model is inspired by GReTA [27], a decomposition of GNN inference into a fixed set of edge- and vertex-centric phases. GRIP implements each phase with separate specialized on-chip memory and execution units. For example, GRIP alleviates irregularity in the edge-accumulate phase by using multiple parallel prefetch engines to load data. This allows GRIP to support a broader class of GNNs than prior work, including emerging models that perform complex computation per-edge. Finally, GRIP includes hardware support for several optimizations: caching partitions of feature data, inter-phase pipelining, and preloading weights between layers. We also introduce a novel GNN optimization called vertex-irregularity that substantially improves latency by increasing the reuse of weight values during inference.

A. Contributions

This paper makes the following contributions:

1) GRIP, an accelerator architecture for low-latency GNN inference. GRIP is efficient across a wide range of models and has numerous hardware optimizations to improve inference latency.

2) A novel optimization for GNN inference called vertex-irregularity, which improves performance by increasing reuse of weights.

3) A detailed description of a $28 \text{nm}$ implementation of GRIP capable of executing four representative GNNs (GCN, GraphSAGE, G-GCN, and GIN). Evaluated across

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1 Following the convention in prior work [21], for clarity we call a GNN’s input a graph and the GNN itself a network.
1. Send
The layer takes as input a graph \( G \) consisting of a set of vertices \( V \) and edges \( E \). Each vertex and edge is assigned a feature vector \( h_v \) and \( h_{(u,v)} \) respectively. Computation is split into three operations:

- **Send** computes a message vector \( m_{u,v} \) for each edge.
- **Aggregate** reduces incoming messages for each vertex to a vector \( a_v \). The neighborhood function \( N(v) \) determines which messages are considered, typically using a fixed size random sample.
- **Update** combines each vertex’s current value with the output of aggregation to produce an updated vector \( z_v \).

By iteratively applying \( K \) of these layers, the final state for each vertex captures information about the structure of its \( K \)-hop neighborhood.

**Pooling and Readout.** Two other layer types are also used in some GNNs. **Pooling** defines a method of coarsening a graph by combining the features of clusters of vertices. **Readout** is a special case of pooling which uses a single graph-wide cluster to produce a representation for an entire graph (e.g. for graph classification). In this paper, we treat both layers as slightly modified versions of message-passing, where edges connect vertices to clusters rather than other vertices.

**Nodeflow.** A nodeflow [22] is a bipartite data structure that describes how features are propagated during message-passing. It is typically generated during a preprocessing step before inference, but can also be created on-demand (e.g. for dynamic graphs). The nodeflow is most useful when performing inference on a subset of the graph since it makes it easy to determine which edges and vertices are required to update a specific vertex. It can also be used to separate sampling from inference by precomputing the neighborhood function and encoding the result directly in the nodeflow.

In this paper, we denote the nodeflow for a particular layer as the three-tuple \((U, V, E)\), where \( U \) is the set of vertices read during inference, \( V \) is the set of vertices updated, and \( E \) is a set of edges connecting vertices in \( U \) to \( V \). Fig. 1 shows an example of using the nodeflow to compute inference in a two layer GNN.

**GCN.** We use the Graph Convolutional Network [28] (GCN) as a concrete running example of a GNN model. GCN uses multiple message-passing layers with the following send, aggregate, and update operations

\[
\begin{align*}
  m_{u,v} &\leftarrow h_u \\
a_v &\leftarrow \text{mean} \{m_{u,v} \mid u \in N(v)\} \\
z_v &\leftarrow \text{ReLU}(W a_v)
\end{align*}
\]

where \( W \) is a trainable weight matrix. We can rewrite this to use sparse-dense matrix multiplication (SpMM)

\[
Z \leftarrow \text{ReLU}(AHW)
\]
where \( \hat{A} \) is a sparse matrix derived from the nodeflow and \( H \)
and \( Z \) are dense matrices formed from the set of input and
output features respectively. This allows GCN inference to be
implemented using operations from highly optimized sparse
matrix libraries, such as Intel MKL [23] or cuSPARSE [35].

B. Performance Challenges of GNNs

To demonstrate the performance challenges of GNNs in
practice, we implement 2-layer GCN using the SpMM form
in Eq. 1. Our implementation uses TensorFlow compiled with
Intel MKL run on a single socket of an Intel Xeon E5-2690v4.
In Fig. 2, we plot measured performance versus arithmetic
intensity for each vertex in the Pokec dataset. Arithmetic
intensity depends on the number of unique neighbors that
must be read during inference, which is determined by the
local graph structure of each vertex.

![Graph Analytics Accelerators. Specialized accelerators
have also been proposed for graph analytics workloads [34],
[36], [37]. However, these workloads require relatively little
computation per-vertex and typically use scalars rather than
large feature vectors. Thus, the computation and memory access
patterns are very different. In Sec. VIII-F, we estimate GRIP to be
8.1x faster than the approach of Graphicionado [20].

GNN Optimizations. Many optimizations have been pro-
posed to improve GNN performance. Common techniques
include scheduling computation to reducing the impact of
sparsity [3], [11], [31], improved sampling [7], or eliminating
redundant computation [48]. These techniques are compatible
with GRIP and can be used for additional performance.

IV. PROGRAMMING MODEL

GRIP’s programming model is based on GReTA [27], a
graph-processing abstraction specialized for implementing
GNNs. GReTA decomposes GNN layers into four stateless user-
declared functions (UDFs): gather, reduce, transform, and activate. GRIP invokes each UDF in one of three
evolution phases: edge-accumulate, vertex-accumulate, and vertex-update. GRIP also allows programs to be composed by
using the result of one program as the features or accumulator
in another. This flexibility allows a wide range of GNN models
to be implemented.

Data Model. UDFs are restricted in the types of data they
can access to in order to simplify hardware implementation.

Fig. 2: CPU performance of GCN inference for vertices in
the Pokec [29] dataset. Bottlenecks in cache bandwidth result in
a significant gap between measured performance and the
roofline upper bound.

In this dataset, inference performance is theoretically bottle-
necked by off-chip memory bandwidth for all vertices. However,
there is a significant gap between the theoretical upper bound
and the actual measured performance at higher levels of
arithmetic intensity. Profiling shows the primary bottleneck
is last level cache bandwidth, a result consistent with prior
analysis of GPU performance [19]. In our experiment, the
highest arithmetic intensities occur when a vertex appears
in multiple neighborhoods and its feature vector can be
reused. However, if multiple cores are reading or writing a
vertex in parallel, this also results in higher utilization of
cache bandwidth. Additionally, features must compete with
large weight values that also occupy the cache and consume
bandwidth during the vertex-centric Update operation.

Opportunities for Acceleration. While GNN inference per-
formance may be limited on existing hardware, the difficulties
described in this section can be overcome with a custom
architecture. In particular, we propose using separate specialized
memory and execution units for each edge- and vertex-centric
operation. To specialize for vertex-centric operations, we use a
dedicated high performance matrix-multiplication unit. Weights
are stored on-chip in dedicated memory with a level of caching
to improve reuse. For edge-centric operations, we prefetch data
for multiple edges in parallel and specialize the on-chip feature
memory to enable fast gather and reduction operations. Finally,
since the nodeflow is known statically, we can also improve off-
chip access efficiency by scheduling bulk transfers of feature
data rather than loading on demand during execution. Taken
together, this gives a significant opportunity for improving
GNN inference performance.

III. RELATED WORK

DNN Accelerators. A significant number of custom neural
network accelerators have been developed, mostly focused on
dense operations [8], [9], [10], [13], [14], [15], [16], [25],
[30], [41], [49]. However, edge-centric operations are difficult
to implement efficiently on these architectures [3], which are
much more computationally irregular than traditional DNNs.
GRIP natively supports edge-centric operations by using a
graph-processing based programming model (Sec. IV) and by
a combination of specialized memory for edge accesses and
software techniques. In Sec. VIII-F we estimate GRIP to be
2.4x faster than a comparable TPU-like accelerator modified
specifically to improve GNN inference performance.

GNN Accelerators. HyGCN [45] and GraphACT [48]
are two accelerators designed for for graph convolutional
networks, a subclass of graph neural networks. Like GRIP,
these accelerators use separate edge- and vertex-centric units for
GNN computation. GRIP builds on these designs by handling
a much more general set of GNNs that includes models that
use computation associated with edges. This is important for
many emerging state-of-the-art GNNs, such as Graph Attention
Networks [40]. Additionally, GRIP’s support for vertex-tiling
reduces the amount of weight bandwidth required during vertex-
oriented operations. In Sec. VIII-F we estimate this improves
performance by 4.5x compared to HyGCN.

Graph Analytics Accelerators. Specialized accelerators
have also been proposed for graph analytics workloads [34],
[36], [37]. However, these workloads require relatively little
computation per-vertex and typically use scalars rather than
large feature vectors. Thus, the computation and memory access
patterns are very different. In Sec. VIII-F, we estimate GRIP to be
8.1x faster than the approach of Graphicionado [20].
Algorithm 2 GRIP Program Execution Semantics

Input: Layer nodeflow \((U, V, E)\); Vertex data \(h_u\) and \(h_v\); 
Edge data \(h_{(u,v)}\); Accumulators \(e_v\) and \(a_v\); Weights and 
bias \(W\)

Output: Updated vertex data \(z_v\)

1: /* Edge-Accumulate Phase */
2: for \((u, v) \in E\) do
3: \(e_v = \text{reduce}(e_v, \text{gather}(h_u, h_v, h_{(u,v)}))\)
4: /* Vertex-Accumulate Phase */
5: for \(v \in V\) do
6: \(a_v = \text{transform}(a_v, e_v, W)\)
7: /* Vertex-Update Phase */
8: for \(v \in V\) do
9: \(z_v = \text{activate}(a_v)\)

GRIP programs use four types of data: (1) A nodeflow \(NF = (U, V, E)\) encodes computational structure by defining the vertices and edges to read and update. (2) Feature vectors \(h_u\), \(h_v\), and \(h_{(u,v)}\) associated with nodeflow input vertices, output vertices, and edges respectively. (3) A set of constant layer weights \(W\). (4) Edge-accumulator \(e_v\) and vertex-accumulator \(a_v\) associated with each output vertex.

**Execution Semantics.** UDFs are executed in three phases:

1) **Edge-accumulate** iterates over nodeflow edges and invokes \(\text{gather}\) and \(\text{reduce}\). \(\text{Gather}\) reads features associated with an edge to produce a message value. \(\text{Reduce}\) accumulates messages sharing an output vertex into \(e_v\). This results in a single value per output vertex.

2) **Vertex-accumulate** iterates over each output vertex and combines \(e_v\) with the previous accumulator state \(a_v\) using \(\text{transform}\). \(\text{Transform}\) is the only UDF with access to layer weights and is usually the most computationally expensive operation in a layer (e.g. matrix multiplication).

3) **Vertex-update** again iterates over each output vertex and applies \(\text{activate}\) to \(a_v\). The \(\text{activate}\) UDF typically implements the non-linear operations required in a layer (e.g. the activation function). This produces a final updated value for each vertex \(z_v\).

Alg. 2 shows the full execution semantics of a GRIP program.

**A. Layer Implementation**

The decomposition used by GRIP is expressive enough to allow implementing a wide variety of GNNs. Implementing a particular layer is typically straightforward since each phase naturally maps to the operations of the massage-passing layer introduced in Sec. II. However, some complex models may require a layer to be split into multiple programs. This is especially true for models that require significant computation per-edge. For example, consider the following modified GCN Send operation

\[ m_{u,v} \leftarrow W_0 h_u \]  

This cannot be mapped directly to \(\text{gather}\) and \(\text{reduce}\) since they do not have access to the layer weights. Instead, we implement this layer by splitting it into two GRIP programs as shown in Fig. 3. Note that splitting a layer may result in each program iterating over a different nodeflow. For example, the program in Fig. 3a iterates over an identity nodeflow where all vertices are only self-connected. In Fig. 4, we demonstrate the flexibility of this approach by showing the implementation of a variety of different GNN models.

**V. THE GRIP ARCHITECTURE**

GRIP is an accelerator architecture for low-latency GNN inference. Rather than designing around a specific GNN, GRIP allows users to customize the architecture by implementing four processing elements (PEs) corresponding to each UDF of GReTA. This allows GRIP to be used to accelerate a wide variety of models. In this section, we describe an overview of GRIP and the microarchitecture of each execution unit. A high level overview of GRIP is shown in Fig. 5.

**A. Overview**

**Control.** GRIP is controlled by a host system that sends commands to execute different operations or transfer data. The control unit dequeues each command in-order and issues them asynchronously to individual execution units or the memory controller. Additionally, almost all buffers use double-buffering to allow overlapping the execution of different operations with moving data between buffers or loading from off-chip. A barrier command is used to enforce dependencies by preventing new
commands from being issued until all previous commands have completed. Each command also updates a global status register on completion, which can be queried by the host to monitor execution.

**Execution Units.** GRIP has three core execution units: the edge unit, the vertex unit, and the update unit. The edge unit performs the edge-accumulate phase by iterating over the edges of the nodeflow, which is stored in the nodeflow buffer. The edge unit then reads the associated features, executes gather, and finally accumulates the result into the edge accumulator using reduce.

The vertex unit performs the vertex-accumulate phase by iterating over the output vertices corresponding to the accumulated edge values. It then executes transform, accumulating the result into the vertex accumulator. The vertex unit also reads weight values from the tile buffer, which caches tiles of weight values from the global weight buffer. To synchronize the tile buffer and the vertex unit, the weight sequencer controls iterating over the tiles as described in Section VI-B. Since weight values are shared across all nodeflow output vertices, the global weight buffer is only required to be loaded once at the beginning of a GRIP program.

Finally, the update unit performs the vertex-update phase by reading the accumulated values for each vertex and passing the values to the activate PE. The result is written to the nodeflow buffer as an updated feature, or to the edge or vertex accumulator. This allows efficiently passing values between different GRIP programs when they are executed in sequence.

**PE Implementation.** GRIP allows users to customize four PEs corresponding to the UDFs introduced in Sec. IV. These can be implemented in multiple ways depending on the user’s needs. For example, they could be implemented using a reconfigurable fabric (e.g. an FPGA) for maximum flexibility. Alternatively, they could be implemented using a model specific circuit to optimize for area or performance.

Our implementation uses a programmable ALU based approach. Since most common GNNs only require a small number of operations in practice, this allows us to support a range of models on the same hardware while remaining reasonably efficient in practice. Specifically, we allow gather to be identity (e.g. \( h_u \) or \( h_v \)), element-wise sum, product, or scale by constant; reduce to be element-wise sum, max, or mean; transform to be matrix multiplication followed by element-wise sum; and activate to be either ReLU or a LUT operation which we describe in Sec. V-D. While these cover most GNN models we investigated, expanding the set of supported operations may be required for other GNNs. We leave exploring other possible implementations for future work.

**Memory Controller.** The memory controller is responsible for moving data on- and off-chip. Instead of each execution unit issuing requests to the memory controller directly, the host is required to statically schedule memory transfers before execution. This is possible since the set of features required for inference can be easily determined from the nodeflow. This also prevents individual units from stalling on external memory accesses, but requires scheduling commands such that loading data fully overlaps with execution (Sec. VI-A).

**B. Edge Unit**

The edge unit pipeline is split into source-oriented (P0-P2) and destination-oriented (R0-R4) sections called lanes that can be independently replicated. Stage R0 is only used for models that require reading source features.

The edge unit pipeline is split into two distinct halves (Fig. 6). Stages P0-P2 implement fetch, which iterates over the edges of the nodeflow and reads the features corresponding to the source vertex. The result is passed to reduce (stages R0-R4), which reads the corresponding destination feature and then applies gather and reduce, accumulating the result into the edge accumulator. GRIP allows optionally disabling stage R0 since most models do not require reading source features.

**Parallelization.** The edge-accumulator value for each output vertex can be computed independently. This means there is a significant amount of parallelism that can be exploited to improve the performance of the edge unit. A simple method to...
parallelize execution is to duplicate the elements of the edge unit into $N$ identical copies. Each copy can then be assigned a subset of output vertices to process in parallel (e.g. by a random hash of the vertex ID). However, since the nodeflow buffer is read every cycle by each lane, this approach requires adding $2N$ ports to the nodeflow buffer.

Instead, GRIP duplicates prefetch and reduce into $N$ and $M$ copies called lanes. Each lane is statically assigned a partition of input vertices (for prefetch) or output vertices (for reduce). Similarly, edges are assigned to a prefetch lane based on the edge’s source vertex. During execution, each prefetch lane iterates over its assigned edges and reads each edge’s corresponding feature. It then sends the feature data through an $N \times M$ crossbar to the reduce lane assigned to the destination vertex. This design restricts each lane to accessing only its assigned subset of features and edges, allowing GRIP to partition the nodeflow buffer into $N + M$ separate SRAMs. As a result, GRIP scales to a much larger number of lanes than the simpler design. Additionally, our implementation of GRIP extends this scheme to include off-chip memory by storing feature data pre-partitioned and setting the number of prefetch lanes equal to the number of DRAM channels.

C. Vertex Unit

The vertex unit implements the vertex-accumulate phase by iterating over the output vertexes and applying transform. Our implementation restricts transform to a matrix multiplication, which we implement using a $16 \times 32$ weight stationary PE array [9]. Each PE contains a 16-bit multiplier, as well as a local double buffered weight register. The PE array is broken into two $16 \times 16$ blocks. Blocks can be configured to use one of two modes: cooperative, where both blocks operate on the same vertex, or parallel, where blocks operate on different vertices in parallel. Parallel mode broadcasts weight values to both blocks, allowing for slightly lower energy consumption at the expense of higher latency when there is only a single output vertex.

Unlike many other neural network accelerators, GRIP does not use a systolic array structure. Instead, GRIP broadcasts inputs across the rows of the array and accumulates results down columns using a reduction tree. The entire operation is pipelined to allow multiple matrix operations to occur without stalling, even as weights are transferred in and out of the array. This results in a significant savings in latency for a single matrix-vector operations; instead of requiring $16 + 32 = 48$ cycles, our implementation requires just six (three to distribute values, one for multiplication, and two for reduction). This also eliminates the buffers required for input skewing in a systolic design.

D. Update Unit

The update unit iterates over each vector in the vertex accumulator and applies activate. Our activate PE allows two possible operations: element-wise ReLU and a two-level configurable lookup-table (LUT) that can be used to approximate many activation functions. Each LUT level is implemented as a separate table with 33 and 9 entries, respectively. Both cover overlapping ranges of input: the first level from $-2^a$ to $2^a$, and the second level from $-2^b$ to $2^b$, where $a$ and $b$ are user configurable values. The LUT entries linearly partition the range, e.g. entry 0 of level 1 corresponds to $-2^a$, entry 1 corresponds to $-2^a + 2^{a+1}/3$, etc. To perform an activation computation, the input is first converted to a 16-bit fixed point representation with 4-bits of integer precision. Each level is then checked in series to see if the input falls in its range. If so, the closest two LUT values are linearly interpolated to produce an output. If the values overflow the range for both levels, the input is either clamped to the closest value in the second level, or a user configured linear function is used. Additionally, the overflow behavior can be configured for both positive and negative inputs independently, allowing the implementation of non-symmetric activation functions. This simple approximation covers a large number of activation functions, including sigmoid, which is required for models such as G-GCN.

VI. OPTIMIZATIONS

GRIP implements two major GNN optimizations: execution partitioning and vertex-tiling. Execution partitioning describes a method to split a GRIP program to operate on partitions of a nodeflow, reducing the amount of on-chip memory required. GRIP supports pipelining operations on different partitions, improving performance. Vertex-tiling improves the locality of weights the vertex-accumulate phase, reducing the memory bandwidth required by the vertex unit. Collectively, these optimizations reduce inference latency for GRIP by a significant factor.

A. Execution Partitioning

A common GNN optimization is to split the graph into partitions that can be computed on separately [27], [31], [45]. This reduces the peak amount of on-chip memory required to compute inference since only a portion of the graph must be loaded at once. GRIP supports a similar optimization we refer to as execution partitioning, shown in Fig. 7. First, the user partitions the nodeflow offline by splitting the input and output vertices into fixed chunks of size $N$ and $M$. Likewise, the edges are partitioned into blocks of size $N \times M$, where block $NFi_{i,j}$ stores the edges connecting input vertices in chunk $U_i$ to output vertices in chunk $V_j$. During inference, GRIP executes

Fig. 7: An example of a nodeflow (a) and corresponding partitions (b) which are processed column-wise. GRIP also pipelines transferring feature data with execution (c).
edge-accumulate for each partition in a column, skipping blocks that are empty. Then, GRIP executes the vertex-accumulate and vertex-update phases once, updating values in the corresponding partition of output vertices. This ensures every incoming edge for each output vertex is processed before vertex-accumulate.

Another advantage of execution partitioning is that operations can be pipelined between partitions. GRIP implements two kinds of pipelining related to partitioning. First, GRIP pipelines loading data from off-chip with the edge-accumulate phase. This allows overlapping execution with bulk loading feature data for an entire partition. If enough space is available in the nodeflow buffer, GRIP also optionally caches partition feature data loaded during the processing of the first column to avoid reload data while processing later columns. Second, transferring weights from the global buffer can be pipelined with processing an entire column. GRIP performs inter-layer pipelining by loading the weights of the next layer while processing the last column, and preloads the tile buffer before processing the first column.

### B. Vertex-Tiling

The bandwidth required to load layer weights can be a significant bottleneck. For example, consider a GCN layer with a feature size of 256. Since our implementation of transform cannot hold the entire 1 MB weight matrix locally, new weight values must be loaded every cycle. At an operating frequency of 1 GHz, this requires a maximum of 2 TB/s of tile buffer bandwidth, which we found difficult to implement physically. While this could be resolved by increasing the number of weights stored within the multiplier array, this increases energy usage and lacks flexibility since a model with a larger feature size would still run into the same limitation.

GRIP’s approach is to instead use an optimization we call vertex-tiling. The key insight of vertex-tiling is that in almost all cases transform is affine, which allows us to perform an optimization similar to tiling matrix multiplication. Fig. 8 shows a graphical representation of this strategy. Here, edge-accumulate produces \( f \) elements for \( m \) output vertices. This requires storing \( f \times m \) elements in the edge accumulator instead of the full \( F \times M \) matrix. Then, we run vertex-accumulate (in this case matrix multiplication), which loads each \( f \times o \) tile from the tile buffer. We then repeat this process, first for all vertex tiles and then for all weight slices, maximizing the locality of the weights. This reduces the bandwidth between the tile buffer and the matrix unit by a factor of \( 1/m \). Thus, by tuning \( f \) and \( m \) we can trade-off the required bandwidth with the amount of storage required for tiles and edge-accumulate values.

### VII. EXPERIMENTAL METHODOLOGY

#### Datasets

| Dataset       | Nodes   | Edges     | 2-Hop |
|---------------|---------|-----------|-------|
| Youtube (YT)  | 1,134,890 | 2,987,624 | 25    |
| Livejournal (LJ) | 3,997,962 | 34,681,189 | 65    |
| Pokec (PO)    | 1,632,803 | 30,622,564 | 167   |
| Reddit (RD)   | 232,283  | 47,396,905 | 239   |

#### Models

We implemented four GNNs which cover a broad range of different model types: GCN [28], the max variant of GraphSage [21], GIN [44], and G-GCN [2], [5], [33]. For our neighborhood function, we use the same sampling procedure as described by the authors of GraphSAGE. Specifically, we deterministically map a given vertex to a fixed-sized, uniform sample of its neighbors. For all models, we use two layers with sample sizes 25 and 10 for the first and second layer, respectively. Samples between layers are independent. Additionally, we use a feature size of 602 (the feature size of the Reddit dataset), a hidden dimension of 512, and an output dimension of 256 for all layers.

#### Baseline

Our CPU baseline was a dual socket server containing two, 14-core 2.60 GHz Intel Xeon E5-2690 v4 CPUs, each with four channels of DDR4-2400 memory. We restricted our experiments to a single socket to adhere to Tensorflow performance guidelines [18] and to avoid latency variation resulting from NUMA. In this configuration, we measured a sustained 1.084 TFlop/s in a matrix multiply benchmark (93% of 1.164 TFlop/s theoretical peak) and 64.5 GiB/s of off-chip memory bandwidth (84% of 76.8 GiB/s theoretical peak).

We implemented both the baseline and our optimized inference algorithm in Tensorflow v2.0 [1] with eager mode enabled and compiled with the Intel Math Kernel Library [23]. To discount the overhead of the Tensorflow library for each model, we measured the time to evaluate an equivalent model with all tensor dimensions set to zero and subtract it from the latency measurement. We also perform a warm-up inference before all measurements to allow Tensorflow to compile and optimize the network.
We also measure the impact of each GNN optimization we with prior evaluations of inference performance [38]. With a variety of models and datasets. Table III shows GRIP’s (GCN, Pokec) and 10
The implementation uses 16-bit fixed point, which maintains smaller speedup on models that perform a larger portion of their
TABLE II: Architectural characteristics of baseline and GRIP.

|                | CPU          | GRIP         |
|----------------|--------------|--------------|
| Compute        | 1.164 TOP/s  | 1.088 TOP/s  |
| @ 2.6 GHz      | @ 1.0 GHz    |              |
| On-chip memory | L1: 14 × 32 KIB |  Nodelow: 4 × 20 KIB |
|                | L2: 14 × 256 KIB | Tile: 2 × 64 KIB |
|                | LLC: 35 MiB   | Weight: 2 MiB |
| Off-chip memory| 4× DDR4-2400 | 4× DDR4-2400 |
|                | 76.8 GiB/s    | 76.8 GiB/s   |
| Total Area     | 306.18 mm²   | 11.27 mm²   |
| Power          | 135 W        | 4.9 W       |

ASIC Synthesis: We implemented GRIP in SystemVerilog, choosing the architectural parameters to have similar compute and memory bandwidth as our CPU baseline (Table II). The implementation uses 16-bit fixed point, which maintains suitable inference accuracy in the models we evaluate. We then performed synthesis and place and route in a 28 nm CMOS process, targeting a 1 GHz operating frequency and worst case PVT corner. The critical path of GRIP was determined to be 0.93 ns, inside the weight SRAMs. Power estimates of each unit was produced by generating activity factors from a cycle accurate simulation of our implementation and applying them to our synthesized design. We used Cacti v6.5 [39] to estimate the area and power of the SRAM memories. We also integrated Ramulator [26] into our simulator to estimate DRAM timings and produce a command trace. These traces were fed to DRAMPower [6] to estimate DRAM power.

TABLE III: 99%-ile inference latency for GRIP, CPU, and GPU

| Model | Dataset    | GRIP µs | CPU µs | GPU µs |
|-------|------------|---------|--------|--------|
| GCN   | youtube    | 15.4    | 309.2  | 1082.4 |
|       | livejournal| 15.8    | 466.8  | 1313.6 |
|       | pokec      | 16.0    | 477.1  | 1085.6 |
|       | reddit     | 16.3    | 407.1  | 813.2  |
| G-GCN | youtube    | 134.1   | 2315.9 | 1332.5 |
|       | livejournal| 146.3   | 2493.2 | 1837.6 |
|       | pokec      | 146.7   | 2637.9 | 1409.2 |
|       | reddit     | 147.0   | 2864.2 | 1133.9 |
| GS    | youtube    | 113.7   | 1545.1 | 1309.0 |
|       | livejournal| 124.4   | 1947.4 | 2193.8 |
|       | pokec      | 124.9   | 2075.7 | 1759.1 |
|       | reddit     | 125.3   | 2099.0 | 1252.8 |
| GIN   | youtube    | 30.5    | 344.7  | 1387.6 |
|       | livejournal| 30.9    | 416.1  | 1221.5 |
|       | pokec      | 31.1    | 340.7  | 855.5  |
|       | reddit     | 31.4    | 354.8  | 1009.4 |

A. Overall Performance
To evaluate GRIP’s overall performance, we measured the total end-to-end execution time (latency) to compute inference with a variety of models and datasets. Table III shows GRIP’s inference latency and speedup versus our CPU and GPU implementation. We use 99th percentile latency for consistency with prior evaluations of inference performance [38].

Performance vs. CPU. Compared to our CPU implementation, GRIP achieves a latency improvement of between 29.8× (GCN, Pokec) and 10.9× (GIN, Pokec) with a geometric mean of 17.0× across all datasets and models. GRIP tends to give a smaller speedup on models that perform a larger portion of their computation during the Update step of the message-passing layer. For example, GIN’s Update uses a two-layer MLP that requires roughly double the computation of GCN’s single matrix multiplication. However, the additional computation results in similar overall CPU inference latency since our implementation is largely bottlenecked by non-computational factors (Sec. II-B). This results in GRIP achieving a smaller performance improvement of 10.9-13.5× compared to an improvement of more than 13.6× for all other models.

Performance vs. GPU. Practical deployments of online GNN inference most often use CPUs due to the large memory requirements for graph features and low utilization at small batch sizes. However, for completeness we also benchmark GRIP against an Nvidia P100 GPU implementation for each model. GRIP’s speedup on GPU ranges from 83.1× (Livejournal, GCN) to 7.7× (Reddit, G-GCN) with a geometric mean of 23.4×. For models with relatively low overall latency (GCN, GIN) we see a significantly higher speedup than with our CPU implementation. This is largely due to the overhead of transferring embeddings from host to GPU memory (roughly 200-500 µs, depending on the neighborhood size) which comprises a large portion of the overall execution time for models like GCN (25%-50% of total latency). GRIP does not incur this penalty since features and weights are already stored in device DRAM and do not have to be transferred from the host. On models with a higher total execution time (e.g. G-GCN), GRIP still achieves a significant speedup due to low GPU utilization. With a batch size of 1, there is not sufficient computation during each layer to fully utilize the computational resources of the GPU and overhead of launching each kernel tends to dominate.
B. Breakdown of Performance

In this subsection, we breakdown the performance impact of each architectural feature of GRIP. Specifically, we modify our cycle-accurate simulator to match the bottlenecks exhibited by our CPU implementation and then progressively remove each modification to measure the impact of different units. As a performance benchmark, we use the geometric mean speedup of GCN for the largest neighborhood in each dataset.

Baseline Configuration. Our baseline configuration emulates each core being assigned independent vertices and performing all GReTA phases, with weights and partition data being first loaded into L3 cache and intermediate values accumulated directly in L2. This results in the following simulator modifications. First, we modify our vertex unit to use 14, $8 \times 2$ matrix multiply units, with each unit assigned independent vertices within a partition. This emulates the effect of each CPU core using two 8-element SIMD units. Second, we increase the number of fetch and gather units to 14 and the crossbar width to 32 bytes, matching the number of cores and L2 cache bandwidth, respectively. We also disable pipelining between the edge and vertex units to emulate a single core performing both functions. Third, we merge the weight and nodeflow buffers into a single SRAM and limit the maximum read bandwidth to 16 bytes per cycle per fetch unit, matching the bandwidth of the L3 cache. Finally, we disable pipelining between the vertex and update unit to model both operations being performed by the same core. This configuration overestimates the performance of the CPU in practice since it models ideal performance and no additional computation required for auxiliary operations, such as indexing calculations. In particular, with a 2.6 GHz clock and an element width of 4-bytes, our model is $2.07 \times$ faster than the measured CPU latency.

Breakdown. In Fig. 9a, we show the impact of different units in GRIP by progressively removing each modification from our baseline in reverse order. First, we split the weight and nodeflow memories into separate SRAMs. This results in a $2.8 \times$ speedup due to removing contention between fetching features and weights from the same SRAM ($2.0 \times$), as well doubling the bandwidth available to load weight values into the vertex unit ($1.4 \times$). Second, we add the edge unit, resulting in an additional improvement of $3.4 \times$. While this is partially due to increased crossbar bandwidth after adjusting the number of fetch and gather units ($1.14 \times$), the majority of the speedup is due to allowing loading data, edge-accumulate, and vertex-accumulate phases to overlap by using a dedicated unit for each phase (2.97$\times$). Third, we enable the vertex unit and revert to using a single $16 \times 32$ matrix multiply unit, resulting in an additional $1.87 \times$ speedup. This is due to increased overall TOP/s ($1.63 \times$) and using a single unit rather than multiple units, which allows units to not be wasted when the overall number of output vertices is small ($1.15 \times$). Finally, separating and pipelining the update unit produces a small speedup of $1.02 \times$.

C. Architectural Parameters

Here, we discuss the impact of several high level architectural parameters on inference performance.

Number of DRAM Channels. The number of DRAM channels determines the overall memory bandwidth available to transfer data on- and off-chip. In Fig. 10a, we observe that GRIP’s performance is strongly related to the number of channels until around 8 channels ($\sim 150 \text{GiB/s}$). This indicates that GRIP’s performance is primarily limited by off-chip memory bandwidth.

Weight Bandwidth. The weight bandwidth determines how many values can be read from the global weight buffer each cycle. If this is set too low, loading weight values can become a bottleneck during vertex-accumulate. We observe this effect in Fig. 10b below 128 GiB/s, which corresponds to loading 64 weight values each cycle.

Crossbar Port Width. The crossbar port width determines the number of elements accumulated by each gather unit in a single cycle. In our experiments, the average number of edges per vertex is fairly small (sampled to be less than 25). Since edge-accumulate typically takes much less time than vertex-accumulate or loading data from DRAM, increasing the width has a limited impact on performance (Fig. 10c). However, it is preferable to over-allocate the crossbar width in order to ensure high performance even on dense nodeflows.

Matrix Multiply TOP/s. The total number of TOP/s GRIP can achieve is determined primarily by the size of the matrix multiply unit. In Fig. 10d we see that performance is strongly related to the size of this unit, until reaching around 2 TOP/s at which point GRIP is limited by memory bandwidth. Thus, our
implementation of GRIP would see a relatively small benefit from a substantially larger matrix unit (1.14× for a 4× larger unit).

**D. Model Parameters**

A key aspect GRIP’s design is balancing the performance between GReTA’s edge and vertex-centric phases. Here, we evaluate how this balance changes as the parameters of the GNN model are altered.

**Feature Dimensions.** In Fig. 11a, we evaluate how varying the number of the input and output features impacts the percent of time spent in matrix multiplication. The proportion is initially low (∼8%) for small features and increases linearly until 32 features. This is due to the fact that when the feature size is smaller than the native width of the DRAM interface, DRAM bandwidth is poorly utilized due to many random accesses. In our implementation, we use two dual-channel DRAM controllers, which each have an interface of 64 2-byte elements. Above this point, the proportion of time spent performing vertex-accumulation stays flat, reflecting the fact that each additional feature results in a constant amount of additional computation during inference. However, this analysis does not hold for the output features, which can be increased without needing to increase the number of values loaded from DRAM. We see that increasing the output feature size always increases the percent of time performing vertex-accumulate. Thus, models with large output feature sizes are likely to be limited by compute rather than memory.

**Sampled Edges.** Another important model parameter is the number of sampled edges per output vertex. In Fig. 11b, we evaluate how the number of edges impacts the percent of total time spent performing edge-accumulate. For less than 8 edges per vertex, GRIP’s performance is mostly limited by computation and overhead related to accessing data from DRAM. Above this threshold, the memory and crossbar bandwidth becomes a bottleneck, and GRIP spends an increasing portion of execution loading data.

**Neighborhood Size.** The neighborhood size heavily impacts GRIP’s overall latency and is influenced by local graph structure. To demonstrate the impact of the neighborhood size on performance, we plot GRIP’s minimum, median, and 99th percentile inference latency for GCN across different neighborhoods of the LiveJournal dataset in Fig. 12a. The result is a strong linear relationship between the neighborhood size and latency across the entire distribution. Each vertex added to the neighborhood results in a roughly constant increase in the amount of work during inference. Additionally, we observe that as the neighborhood size increases, the median latency moves closer to the 99th percentile. This is the result of larger neighborhoods being more likely to be densely connected, leading to a larger number of reductions that must be computed.

In Fig. 12, we evaluate the latency speedup compared to the CPU baseline across different neighborhood sizes. Below a neighborhood size of 95, we see a roughly constant speedup of between 12× and 18×. For these neighborhood sizes, all intermediate values fit into the L1 and L2 cache of a single CPU core. After this point, some feature values must be stored in the L3 cache and inference performance becomes limited by the cache bandwidth (Sec. II-B).

**E. Optimizations**

In this subsection, we evaluate the impact of each optimization used by GRIP.

**Partitioning and pipelining.** In Fig. 13a we show the cumulative speedups of each optimization enabled by partitioning.
We compare to an unoptimized baseline, where feature values are loaded from off-chip on demand and no pipelining exists between stages. First, by caching feature data on-chip, GRIP achieves a 1.3× speedup. This is due to the decreased memory traffic required to reload data between partition columns and by the improved throughput from bulk loading data for an entire partition. Second, pipelining operations between different partitions results in an additional 1.3× speedup due to overlapping execution with memory transfers. Finally, we can also pipeline the transfer of weights from the global weight buffer into the vertex-update unit. This increases the overall speed-up to a total of 2.5×.

**Vertex-Tiling.** In Fig. 13b, we show the speedup compared to no tiling as we alter the two tiling parameters $M$ (the number of vertices in a tile) and $F$ (the number of elements per vertex). We see that performance generally reaches a maximum around $F = 64$ elements. Above $F = 64$, increasing $F$ causes the vertex unit to stall more often while waiting for a tile to be produced by the edge unit. The performance degradation is not linear because the time taken to accumulate a tile depends on the connectedness of the node flow. We also see degraded performance below $F = 64$. This is because $F$ features are loaded from memory for each vertex. As $F$ decreases, more random DRAM accesses are required to load features, degrading DRAM throughput. Increasing $M$ also increases performance until around 12 vertices. The maximum number of output vertices in our model is 11. Increasing $M$ beyond this only adds additional latency associated with processing empty dummy vertices.

**F. Comparisons to Prior Work**

Several other approaches have been proposed to accelerate neural networks and graph algorithms. Here, we analyze the bottlenecks present in each approach and compare performance with GRIP.

**HyGCN.** HyGCN [45] is an accelerator designed for graph convolutional networks, a subset of GNNs that do not have computation associated with edges. HyGCN and GRIP take a similar approach of using separate units for edge- and vertex-centric operations. However, GRIP addresses two major bottlenecks present in the HyGCN design.

First, HyGCN uses 32 8-lane SIMD units to perform edge-oriented operations, but can only issue a single edge at a time. This means the throughput of edge operations will be limited when the number of features is smaller than the total number of SIMD lanes. In contrast, GRIP allows for multiple edges to be issued in parallel.

Second, HyGCN requires an entire feature vector to be computed and stored before performing vertex-oriented operations. In order to process multiple vertices in parallel, this requires a large buffer to store accumulated values (16 MB in the HyGCN implementation). The size of this buffer is also reported by the HyGCN authors to have a significant impact on their overall performance (1.3 - 4× worse performance for a 16× smaller buffer.) In contrast, GRIP uses vertex-tiling to only store a small number of elements from multiple feature vectors. This allows GRIP to use a roughly 10,000× smaller buffer (1.5 KiB) while achieving comparable performance.

We demonstrate these limitations by modifying our simulator to emulate the HyGCN approach. Specifically, we set the number of gather and fetch units to 1 and the crossbar width to 256 to match the number of SIMD lanes. We disable all tiling and force feature vectors to be fully accumulated before vertex-accumulate. We then set all other parameters to be the same as GRIP, including the same partitioning used in our evaluation of GRIP.

This configuration results in a speedup of 4.4× the baseline, shown in Fig. 9b. However, it performs 4.5× slower than GRIP due to limits in the available on-chip memory bandwidth for weights. Incorporating vertex tiling would allow for a much smaller edge accumulate buffer and reduce the required bandwidth by increasing the reuse of the weights.

**Modified TPU.** The TPU [25] is a DNN accelerator designed around a large 2-D systolic array. Unfortunately, GNNs are difficult to implement efficiently for the TPU due to a lack of support for edge-oriented operations [3]. Instead, we compare GRIP to a modified version of the TPU architecture that addresses this limitation by incorporating features from GRIP. We refer to this modified design as the TPU+.

Specifically, the TPU+ has an additional unit similar to GRIP’s edge-unit between the TPU’s unified buffer and the systolic data setup. This allows the TPU+ to natively support the GReTA programming model by mapping edge-accumulate onto the new edge-unit, vertex-accumulate onto TPU’s systolic array, and vertex-update onto the activation pipeline. This design also supports both the execution partitioning and vertex-tiling optimizations described in Sec. VI.

We estimate the performance of the TPU+ by modifying our cycle-accurate model to use a single fetch and gather unit. We also replace the vertex-unit with an identically sized 16×32 systolic array. As in the original TPU design, weights are stored off-chip and the dedicated weight bandwidth is limited to 30 GiB/s. All other parameters remain unchanged compared to our evaluation of GRIP, including the use of 4× DDR4-2400 for off-chip memory and the same partitioning and vertex-tiling optimizations.

This configuration achieves a 11.3× speedup (Fig. 9b) compared to our baseline in Sec. VIII-B. The main bottleneck in this approach is the limited bandwidth dedicated to weights. Moving weights on-chip as in GRIP results in a 1.72× speedup. Higher performance memory for weights (e.g. HBM as used by later versions of the TPU) could also address this bottleneck. However, we leave a fuller exploration for future work.

**Graphicionado.** Graphicionado [20] is an accelerator architecture designed for graph analytics. Like GRIP, Graphicionado allows several units to be specialized for a particular algorithms, such as GCN inference. However, it is designed for algorithms that use a small amount of state per-vertex. As a result, it suffers from two bottlenecks. First, like HyGCN, it cannot perform vertex-tiling since it requires full feature vectors to be accumulated. This results in a bottleneck similar to HyGCN since weight data cannot be easily reused between different
vertices. Second, each lane has independent vertex units instead of using a single shared unit, increasing the required weight bandwidth by an amount proportional to the number of lanes.

We estimate the impact of these bottlenecks by modifying our simulator by disabling tiling and splitting the vertex unit into two units lanes that share a single tile buffer port. We also use the same partitioning scheme used for GRIP. This configuration results in a speedup of $2.4 \times$ over the baseline, shown in Fig. 9b. However, this is $8.1 \times$ slower than GRIP due to significant bottlenecks in weight bandwidth.

G. Energy

Table IV shows the power consumption for each of GRIP’s core top level modules during GCN inference. The single most energy intensive during inference is loading embeddings from DRAM, consuming more than the rest of the accelerator combined (53.7%). This is due to the fact that both the number of vertices and the feature size is the largest at the input of GCN, leading to more data being initially loaded in the first layer. Additionally, GRIP optimizes for latency with four high performance DRAM channels, requiring a large amount of energy per transfer. The rest of the energy is mostly used by loading weights from the global weight and nodelow buffers. Both are fairly large, leading to a high energy cost per read and write. In total, GRIP uses just 4.9 W, a significant improvement over the 135 W TDP of the baseline CPU.

| TABLE IV: Breakdown of power for GCN inference. |
|-----------------------------------------------|
| Module             | mW | (%)|
|--------------------|----|----|
| **Execution Units**|    |    |
| Edge               | 4.1| 0.1|
| Vertex             | 656.6| 12.6|
| Update             | 0.4| < 0.1|
| **SRAM**           |    |    |
| Weight             | 1476.7| 28.3|
| Nodelow            | 269.5| 5.1|
| **DRAM**           |    |    |
|                    | 2794.7| 53.7|
| **Total**          | 4932.4| 100|

IX. CONCLUSION

GNNs represent a promising new method in machine learning to learn directly from graph-structured data. However, the computational costs of GNNs represent a significant barrier for deployment in many applications, especially in the scenario of online inference.

This paper presents GRIP, an accelerator architecture designed for low latency GNN inference. GRIP splits GNN operations into a series of edge- and vertex-centric phases. Each phase is implemented independently in hardware, allowing for specialization of both the memory subsystem and execution units to improve performance. Additionally, GRIP has hardware support for several optimizations that further reduce latency, including pipelining operations between nodelow partitions and vertex-tiling. We then implement GRIP as 28 nm ASIC capable of executing a range of different GNNs. On a variety of real graphs, our implementation improves 99th percentile latency by a geometric mean of $17 \times$ and $23 \times$ compared to a CPU and GPU baseline, respectively, while drawing only 5 W.

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