Efficient Design of Exclusive-Or Gate using 5-Input Majority Gate in QCA

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Abstract: Quantum dot cellular automata (QCA) is one of the emerging technology that has the capability of replacing the CMOS based technology at nano scale level. Majority gates and inverter are the principle elements in QCA to design any circuit. In this work, we propose a new 5-input majority gate. The new proposed gate reduces number of required cell, area and power consumption. The study of power dissipation is also explained using power estimator tool QCAPro. QCA designer 2.0.3 is used to validate the majority gate layout and their functionality. Furthermore, an XOR gate based on QCA are designed using proposed majority gate. Layout and simulation results show the improvement of proposed circuit over previous designed circuits.

Keywords: CMOS, Clocking, Majority gate, QCA, XOR gate.

I. INTRODUCTION

In last few decades, the increase in processing speed and exponential scaling in feature size have been successfully attained using lithography based VLSI technology. But this trend faces some serious challenges because of basic limits of CMOS technology such as short channel effects, ultra thin gate oxide, doping fluctuations and expensive lithography at nano scale level [1].

QCA is one of the emerging technology that has ability to replace the transistor based devices at nano scale level. QCA technology can overcome the limitation of conventional transistor based technology. QCA has some advanced features like faster speed, smaller size and lower power consumption in comparison to transistor based technology [2],[3]. QCA technology uses a QCA cell as a basic building block to construct gate and wire [4]. This cell consist of two electrons which give possible logic values of ‘0’ and ‘1’. QCA technology not only provide the solution at nano scale level but also gives the new method of information transformation and computation. In transistor based system some circuits (logic gates) perform computation and wires are used for signal transfer and communication. In contrast QCA technology is able to perform computation and communication simultaneously.

Many digital circuits based on QCA have been presented in last few decades eg: 5-input majority gate structures [5]-[14], exclusive-OR (XOR) gate structures [15]-[20], one bit full adders, one bit full subtractors, reversible alu [21], flipflops, registers etc. Many of the circuits are not robust and vulnerable to fabrication defects because of mutilayer wire crossing. Many of the 5-input majority gates are not efficient in terms of no. of cells and area. The proposed
5-input majority gate requires less no. of cells and area as compared to previous designed gates. Further efficient XOR gate is proposed using single layer coplanar wire crossing.

The rest of the paper is organised as follows. Section II gives the brief review about QCA technology. Section III explained about previous designed 5-input majority gates and proposed 5-input majority gate with power dissipation analysis. An optimal XOR gate is proposed in section IV. Section V consist of simulation result of proposed circuits and comparison to previous works. Finally section VI gives the conclusion of paper.

II. QCA REVIEW

A. QCA Cell

To implement any boolean logic function using QCA we use arrays of paired quantum dots. QCA does not use the transport of electrons like in conventional transistor based technology, rather than it uses the adjustment of coupled electrons in a small squared nano area. There are four potential wells located at the four corner of this nano squared area called QCA cell [3]. These potential wells are connected by four electron tunnel junctions. In these QCA cells two electrons are locked in. These two electrons are allowed to move in four quantum wells through tunnel junctions under the control of clock signal as shown in Fig. 1(a). Due to the coulombic interaction the two electrons will try to reside far from each other. So there will be two positions because of two diagonal, one position can be represented by logic ‘1’ and other by logic ‘0’.

Fig. 1. QCA (a) Logic ‘0’ and ‘1’ representation of QCA cell, (b) QCA wire, (c,d) QCA inverter representation, (e) Two different types of 3-input Majority gate.

B. QCA Wire

If we put two QCA cells adjacent to each other, then the position of electron in one cell will be transferred to other cell. Due to the coulombic interaction the next cell’s state will become same as the previous cell’s state [3]. Thus the signal will be transferred from one cell to another and the array of cell will act as a QCA wire as shown in Fig. 1(b).

C. Basic QCA Elements and Gates

The basic QCA gate is 3-input majority gate. In it QCA cell is used as a basic building block. The 3-input majority gate can be made by using 5 QCA cells arranged in two different ways as shown in Fig.1(e). In 3 input majority gate 3 cell will work as input cells, now the centre cell will be affected by the sum of the coulomb forces of 3 input cells, so the centre cell’s electrons adjustment will be the majority of the adjustment of 3 input cells. Finally the 5th cell will give
the output according to centre cell adjustment [3],[22]. So expression of three input majority gate can be given by (1).

\[ M_3(A, B, C) = AB + BC + CA \]  

(1)

By using three input majority gate we can make AND & OR gate by taking one input as ‘0’ or ‘1’ as in (2) and (3).

\[ A \cdot B = M_3(A, B, 0) \]  

(2)

\[ A + B = M_3(A, B, 1) \]  

(3)

A NOT gate can also be made by QCA cells by inverting the position of electrons in QCA cell [3], so that input logic ‘0’ will result as output ‘1’ and input logic ‘1’ will result as output ‘0’ as shown in Fig.1(c,d).

**D. QCA Clocking**

There are four clock phases in a QCA cell, these are Switch, Hold, Release and Relax. Each clock phase has 90° phase shift to its previous phase as shown in Fig. 2(a) [23],[24]. In the high state of clock signal electron tunnel junctions are opened and electrons are allowed to move between potential wells. High to low is a switch stage and at this time tunneling energy is decreasing so potential barrier is increasing. At low state QCA cell attains a fixed polarized state of electrons. Low to high section of clock signal is release stage in which tunneling energy increases so potential barrier decreases. Finally at high state the QCA cell is relaxed to an unpolarized state as shown in Fig. 2(b).

![Fig. 2](image.png)

(a) (b)

Fig. 2. (a) Four phase clocking, (b) QCA operation during one clock phase.

**E. Crossover**

In designing of QCA circuit sometime it requires to crossover a wire for interconnection of components. Mainly two types of crossover are available, one is multilayer and other is coplanar. In multilayer crossover, multiple layer are used for the interconnection of component as shown in Fig. 3(a). In coplanar crossover method, wire crossing is performed by two different types of cell [14]. One wire has cells with 90° orientation and other wire has cells with 45° orientation, as depicted in Fig. 3(b).
III. FIVE INPUT MAJORITY GATE

Earlier research show the efficacy of 3-input majority gate by incorporating it in most of the QCA designs, but with the essence of more optimal circuits, researchers have designed 5-input majority gate based QCA circuits. These are more efficient in terms of area and faster than the previous designs. Some of the 5-input majority gate structures have been presented in [5]-[14]. The logic function of 5-input majority voter can be expressed as in (4).

\[ M(A, B, C, D, E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE \]

(4)

The new proposed 5-input majority gate structure is shown in Fig. 4(a). Where A, B, C, D, E are 5 inputs and output cell is indicated by ‘OUT’. Remaining medium cells are device cells which aggregate the coulombic forces of all input cells and drive it to the output cell. The comparison table of proposed 5-input majority gate structure with previous designed structures are shown in Table 3.

A. Power Dissipation Analysis

The equation for instantaneous total power of a QCA cell [25],[26] can be expressed by (5).

\[ P_{\text{total}} = \frac{d}{dt}E = \frac{\hbar}{2} \left( \frac{d}{dt} \vec{\Gamma} \right) \cdot \vec{\lambda} + \frac{\hbar}{2} \left( \frac{d}{dt} \vec{\Gamma} \right) = P_1 + P_2 \]

(5)

Where \( \vec{\Gamma} \) = 3D energy vector, \( \vec{\lambda} \) = coherence vector, \( \hbar \) = reduced plank constant. \( P_1 \) represents the clock signal to cell power transfer & difference between input and output signal power. The 2nd term \( P_2 \) indicates the dissipated power (P_diss). The total power dissipation can be calculated by adding the power dissipation by individual cell.
Using above concept a power estimator tool QCAPro is developed by [27]. Using this tool we can compute total power dissipation as the sum of leakage and switching power dissipation, where leakage power is power losses during clock change and the switching power means the power loss at every clock cycle for every individual cell. Three tunneling energy levels are taken as input parameter: $0.5E_k$, $1.0E_k$ and $1.5E_k$ at the temperature of 2K to evaluate power dissipation of all designs. The power dissipation analysis of proposed 5-input majority gate is done using QCAPro and compared with previous designed gates as shown in Table 1. From the table it is clear that the proposed gate has lesser total power dissipation than previous designed gates for all three tunneling energy levels.

The thermal layout of average energy dissipation for $0.5E_k$ at 2K in every individual cell of proposed 5-input majority gate is shown in Fig. 4(b). QCA cells with dark color represent more energy dissipation as compared to QCA cells with light color.

**Table 1:** Power dissipation analysis of 5-input majority gates

| Designs | Avg. leakage energy dissipation (meV) | Avg. switching energy dissipation (meV) | Total energy dissipation (meV) |
|---------|--------------------------------------|--------------------------------------|-----------------------------|
|         | $0.5E_k$  | $1E_k$   | $1.5E_k$   | $0.5E_k$  | $1E_k$   | $1.5E_k$   | $0.5E_k$  | $1E_k$   | $1.5E_k$   |
| [5]     | 1.35      | 4.25     | 7.8        | 10.94     | 9.84     | 8.7        | 12.29     | 14.09     | 16.5       |
| [6]     | 1.28      | 4.14     | 7.69       | 11.53     | 10.37    | 9.16       | 12.81     | 14.51     | 16.85      |
| [7]     | 3.44      | 10.67    | 19.52      | 32.66     | 29.89    | 27.01      | 36.1      | 40.56     | 46.53      |
| [12]    | 3.69      | 11.38    | 20.96      | 27.61     | 25.25    | 22.69      | 31.30     | 36.63     | 43.65      |
| [8]     | 3.38      | 8.95     | 15.03      | 9.23      | 7.7      | 6.41       | 12.61     | 16.65     | 21.44      |
| [10]    | 4.41      | 13.55    | 24.73      | 31.24     | 28.31    | 25.21      | 35.66     | 41.85     | 49.94      |
| [9]     | 4.44      | 14.25    | 26.61      | 45.51     | 41.59    | 37.29      | 49.96     | 55.84     | 63.90      |
| [13]    | 2.99      | 7.73     | 12.35      | 3.69      | 2.77     | 2.15       | 6.68      | 10.5      | 14.5       |
| Proposed| 2.56      | 6.34     | 10.21      | 3.09      | 2.31     | 1.79       | 5.65      | 8.65      | 12.00      |

The thermal layout of average energy dissipation for $0.5E_k$ at 2K in every individual cell of proposed 5-input majority gate is shown in Fig. 4(b). QCA cells with dark color represent more energy dissipation as compared to QCA cells with light color.

**IV. EXCLUSIVE-OR GATE DESIGN**

To design any digital circuit we can use basic logic gates OR, AND, NOT and also universal gates NOR and NAND. In addition of these we can also use exclusive-OR (XOR) gate which is useful to design any complex circuit.

In literature many QCA based XOR gates have been presented [15]-[20]. Some of these designs are single layer and some are multilayer designs. A new QCA based XOR gate is designed in this paper. If ‘A’ and ‘B’ are two inputs of XOR gate then to implement it using QCA, the equation can be expressed as in (6).

$$A \oplus B = M_\gamma (A, B, X', X', 0)$$

(6)

Where equation for $X$ can be given by (7).

$$X = M_\gamma (A, B, 0)$$

(7)
Where $M_3$ denotes the 3-input majority gate and $M_5$ denotes the 5-input majority gate. The QCA layout of proposed XOR gate is shown in Fig. 5(a).

![QCA layout of proposed XOR gate](image)

Fig. 5. (a) Proposed XOR gate (b) A thermal layout energy dissipation map of proposed 5-input majority gate

V. SIMULATION RESULTS AND DISCUSSION

This section includes simulation results of proposed 5-input majority gate structure and XOR gate to validate the proposed circuit. All circuits are simulated using QCADesigner 2.0.3 simulator [28] and QCAPro tool is used for power dissipation analysis. Coherence vector is taken as simulation engine setup with parameter given in Table 2. The proposed gate and circuits are also compared with previous existing circuits.

| Parameter          | Value          |
|--------------------|----------------|
| Cell size          | 18*18 nm²      |
| Dot diameter       | 5 nm           |
| Relaxation time    | 1.000000e-015s |
| Time step          | 1.000000e-016s |
| Layer separation   | 11.5000 nm     |
| Clock low          | 3.8e-23 J      |
| Clock high         | 9.8e-22 J      |
| Relative permittivity | 12.9          |
| Clock amplitude factor | 2.000000    |
| Radius of effect   | 80 nm          |
| Clock shift        | 0.000000e+000 |
| Total simulation time | 7.000000e-011s |

The Table 3 shows the comparison of proposed 5-input majority gate with previous existing structures. From Table 3, we can see that only gate design in [5] has lesser area than proposed gate but it has not single layer accessibility to output. The gate design in [6] required equal number of cells and area as in proposed gate, but in this design input cells are very close, creating undesired effects. So the proposed 5-input majority gate is better than previous gates in terms of required number of cell and area occupied with single layer accessibility to input and output.

| 5 input maj gate structure | No. of cells | Area occupied (nm²) | Single layer accessibility to input and output cells |
|----------------------------|--------------|---------------------|-----------------------------------------------------|
| [9]                        | 23           | 24564               | Yes                                                 |
| [10]                       | 20           | 19084               | Yes                                                 |
A comparison of proposed XOR gate with previous existing XOR gate designs over some performance parameter is shown in Table 4. It can be seen from Table 4 that only the gate design in [19] required 29 cell which is same as in proposed gate but the required area and delay is more in [19]. So the proposed QCA based XOR gate is better than the previous XOR gates in terms of area occupied, complexity and input-output delay. Table 5 shows the comparison results of power dissipation analysis for proposed XOR gate with existing XOR gate. It is clear from this table that the proposed gate has lesser total power consumption than existing XOR circuits. The thermal layout of average energy dissipation for $0.5E_k$ at 2K in every individual
cell of proposed XOR gate design is shown in Fig. 5(b). QCA cells with dark color represent more energy dissipation as compared to QCA cells with light color.

| XOR gate designs | No. of cells | Area in µm² | Delay (Clock cycles) | Layer type |
|------------------|--------------|-------------|----------------------|------------|
| [15]             | 32           | 0.04        | 1                    | Single layer |
| [16]             | 42           | 0.05        | 0.50                 | Single layer |
| [17]             | 51           | 0.06        | 1.25                 | Single layer |
| [17]             | 30           | 0.03        | 1                    | Single layer |
| [18]             | 36           | 0.03        | 0.75                 | Single layer |
| [19]             | 29           | 0.03        | 0.75                 | Single layer |
| Proposed         | 29           | 0.02        | 0.5                  | Single layer |

Table 5: Power dissipation analysis of XOR gate designs

| XOR gate Designs | Avg. leakage energy dissipation (meV) | Avg. switching energy dissipation (meV) | Total energy dissipation (meV) |
|------------------|--------------------------------------|----------------------------------------|-------------------------------|
|                  | Avg. 0.5 Eₖ                         | Avg. 1.0 Eₖ                            | Avg. 1.5 Eₖ                  |
|                  | 9.73                                 | 29.7                                   | 52.78                        |
|                  | 11.20                                | 36.21                                  | 66.30                        |
|                  | 11.04                                | 30.50                                  | 51.97                        |
|                  | 11.80                                | 34.01                                  | 59.42                        |
|                  | 9.75                                 | 27.12                                  | 47.04                        |
|                  | 13.32                                | 33.00                                  | 53.64                        |
|                  | 40.08                                | 43.66                                  | 59.42                        |
|                  | 70.61                                | 18.49                                  | 37.40                        |
|                  | 22.21                                | 43.66                                  | 30.43                        |
|                  | 50.32                                | 35.29                                  | 12.80                        |
|                  | 40.44                                | 35.29                                  |                               |
|                  | 19.39                                | 15.73                                  | 12.80                        |
|                  | 12.80                                | 30.43                                  |                               |
|                  | 19.39                                | 35.29                                  |                               |
|                  | 12.80                                | 30.43                                  |                               |
|                  | 19.39                                | 35.29                                  |                               |
|                  | 12.80                                | 30.43                                  |                               |
| Proposed         | 50.01                                | 62.12                                  | 66.44                        |
|                  | 81.81                                | 50.19                                  |                               |
|                  | 33.25                                | 32.91                                  |                               |
|                  | 62.12                                | 48.73                                  |                               |
|                  | 77.47                                | 66.44                                  |                               |

The simulation result of proposed 5-input majority gate is shown in Fig. 6, where A, B, C, D and E indicate the 5 inputs and ‘Out’ gives the majority of all inputs. This shows the right operation of proposed 5-input majority gate. The simulation result of proposed XOR gate is shown in Fig. 7, where A & B indicate the 2 inputs and Out’ gives the output of the XOR gate. If we find the truth table of XOR gate then we can see that simulation result shows the right operation of proposed XOR gate and giving a valid output after delay of 0.5 clock cycles.

VI. CONCLUSION

In this paper, an optimal 5-input majority gate has been designed with power dissipation analysis, which is better than the previous designed gates over the performance parameter of required no. of cell, area occupation and total power consumption with single layer accessibility. We have also designed an efficient exclusive-OR gate. The proposed design for XOR gate is better than previous existing single layer designs in terms of area occupation, complexity, power consumption and input to output delay.

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