A FPGA Software based GPS Receiver Implementation with Signal blocker through Simulink

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Abstract

Background/Objectives: Field-Programmable Gate Array (FPGA) software based Global Positioning System (GPS) receiver has been designed and developed using the C language interface environment. GPS Receivers are used for tracking a signal and calculates the current position of the signal in real time. GPS Receiver is a real time application used for tracking purpose. Methods/Analysis: A GPS Receiver works on specially coded GPS satellite signals. The signal is processed in a GPS receiver for computing position, velocity and time. A GPS uses minimum four satellite signals for computing positions in three dimensions using the real time receiver clock. Findings: In this paper, it is planned to build a FPGA-based software GPS receiver using a high level Matlab design Simulink tool. This GPS Receiver is used to design such components that require huge computation like baseband signal processing correlator, C/A code generator, Discriminator Code Loop (DCL) are designed by the Xilinx FPGA block and implemented in Matlab/Simulink. Novelty: The “GPS Receiver Processing Captured Satellite data” model of GPS system without jammer, the signal level display shows the value 0.1779; but in case of a jammer, the signal level is reduced to 0.1447 which is 81% of the initial signal level. So, jammer reduces the signal strength and makes the signal weaker.

Keywords: C/A Code, Field-Programmable Gate Array, Global Positioning System, Matlab, Satellite, Signal blocker

1. Introduction

The Global Positioning System (GPS) is space based satellite navigation system which requires minimum four satellite to operate it. The GPS receivers are used to determine the current location at real transmission time, velocity and signal speed which depend on speed of light (3 x 10^8 meters/second) in all weather conditions. To detect the location at least four or more satellite signals are used. GPS Receiver is maintained by the United States government. It is easily reached to anyone and freely accessible for tracking location and calculates a real time user position. The GPS satellite signals are used for broadcasting on the equivalent frequencies but it works on diverse ranging codes having low cross correlation. The satellites signal are having a Code Division Multiple Access (CDMA) for ranging codes to estimate the propagation as well as navigation time which is used to calculate the exact position of the satellite and real transmission time.

The different ranging codes as well as navigation data should be modulated with the help of a carrier signal using a modulator such as Binary Phase Shift Keying (BPSK) in which we can use any modulator suited to research. These types of ranging codes which are used in GPS Satellite broadcasted by P(Y) code (military code) and C/A codes (coarse acquisition code). The signal frequency of C/A code is 1.023 MHz and the carrier frequency of L1 signal is 1575.42 MHz and GPS Receiver are used for the purpose of the navigation in civilian and military application, here we are considering C/A codes and P(Y) codes respectively with a different ranging codes.
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Figure 1. Basic Functional Block diagram of GPS Receiver.

Generally, GPS receiver is composed of two chips or three chips. The GPS receiver is composed of RF chip which is used to convert Radio Frequency (RF) signal to Intermediate Frequency (IF) signal, second one is correlation between RF signal to IF signal which processes the baseband signal and third and last one is Digital Signal Processor (DSP) which calculates the navigation solution and tracking loop for current user position. In this paper, It is implemented a correlated receiver with Field-Programmable Gate Array (FPGA) and tracking loop and navigation solution is completely calculated using PC processor on Matlab Simulink. In [Figure 1] presents the basic block diagram of GPS receiver. RF front end should be used to convert two frequencies such as the signal frequency and intermediate frequency and that frequency will use in FPGA to display the signal. The IF is used to sample a frequency by using Analog to Digital Converter (ADC). Here are some of the following requirements that are essential to comprehend the GPS receiver procedure by using FPGA.

The another programming software approach named as “averaging correlation” for block level GPS C/A attitude acquisition and tracking in the frequency domain by using the whole of smaller FFT blocks. The way of doing thing retains same but the chat ratio is observed in a superior way by using expensive correlator. Frequency dwelling software processing will add more sensibility and will become favorite if this way of doing things is implemented in national GPS headsets.

A GPS receiver reproduce the Pseudo Random noise (PRN) that is transmitted all SV over assimilated separately receiver; When cross-correlating communicated PRN with the incoming signal code with same or clone code generated at the receiver the same interconnecting properties come out as of mathematical autocorrelation of PRN code. When code of the clone code matches with the incoming signal of satellite the correlation is maximum, and if phase of the clone code is different by one chip on either side, the correlation is called minimum. Thus it is said that GPS signal acquisition and tracking is made up of two important processes, one is code replication and another being carrier replication. Now most receivers are digital; SDR’s are mostly developed because they do not need digital components. The digital signals by all SV are received by an antenna. These RF signals are amplified and then sent to preamplifier filter to minimize noise. After amplification and desired operation signals from SV are down converted IF using local oscillator (LO). The mixing of LO produces both upper and lower sideband of signal. Finally thermal noise is taken care.

A GPS wire in such embodiment includes an antenna which receives GPS signals at an RF frequency from noticeable satellites; a down-converter is joined to the projection for reducing the RF frequency of the conventional GPS signals to an In-between frequency (IF); a digitizer joined to the down-converter for sampling the IF GPS signals at a predetermined price; a memory is coupled to the digitizer for storing the sampled IF GPS signals (a micro film of GPS signals). A digital all hail processor is coupled to the flash from the past and engaged under simultaneous instructions and thereby a radio Fast Fourier Transform (FFT) operation is performed on the sampled IF GPS signals to lay at one feet pseudo range information.

Although originally developed for the armed forces, the GPS has proven steep for a common people of public applications. Each public opinion research demands tenacious show from the GPS wire and the associated requirements often vary widely. This handout describes the architectures and functions of settler GPS receivers and by the time mentioned focuses on performance considerations. The fundamental wire measurements are described and the cases of these measurements are thick to the aforementioned receiver architectures.

A GPS is a constellation of 24 satellites that provides users by all of round-the-clock, worldwide positioning capability by the agency of the front page new transmitted in the GPS navigation message. The bird snapper use to bring a screeching Delay Lock Loops (DLLs) to be a part with incoming small amount sequences with identical sequences generated every receiver. The pitance sequences are Gold codes formed as a produce of pseudo-random chat sequences. By aligning the approved and locally generated codes, the aerial determines the undisclosed range to each pumpkin. When the drop is firm, the aerial clock foreshadow is compared to the satellite
predate of copy to verify the undisclosed range. The satellite predate of electronic message is encoded onto the drop in the bucket sequence by the agency of the navigation data.

There are six orbital planes, spaced 60° individually and each containing four satellites. The eyes for of the orbital plane mutually respect to the celestial is 55° in sending up the river to give global coverage. At ridge of 20,200 km, an equatorial orbit would not extend coverage after 72° indifference. Earlier Block I satellites were planned at 63°; nonetheless this was lowered to 55° for the futuristic Block II satellites. This was done particularly because the deep space ship was subsequent as the begin vehicle for GPS satellites.

2. Simulation Stage C/A Code

The C/A is provided by the GPS satellites signal and it should be generated by a sequence having a chip size of 1023 chips. The code of C/A is repetitive every mille second with chipping rate size of 1.023 MHz and this code is only modulated in L1 frequency.

Here, used a method of simulation environment such as (MATLAB or Simulink) to verify each block of C/A code which is used in GPS receiver shown in [Figure 2]. A complete C/A code was built in simulation using received PRN code, initial code phase and loaded code phase, these all are required in the C/A code generation and correlation.

The Pseudo Random Noise (PRN) code is abbreviated which is determined for 29 satellites in our case and these codes are called the C/A code having the different 1023 chips. These chip codes are compared with the different different satellite code with the help of correlation.

3. Simulation Stage of DSP

This Simulation stages and implementation of the complete functionality of RF input, acquisition, tracking and navigation of GPS receiver on a DSP environment with the help of graphical programming language, C/C++. This makes every part in the GPS receiver structural design very easier to understand, the DSP environment is used with approach simulation as well as implementation stages. The implementation stages are easy as compared to the developing stages of most of the designers who have used to enhance new ideas or given algorithm. It has a new look for designing, simulating, implementing and developing the most difficult parts of a representative GPS receiver. Using the DSP environment, have been designed or implemented a digital filter, code loop filter, control logic and carrier recovery phase block to complete a GPS receiver as shown in [Figure 3].

Figure 2. Simulink Block diagram of C/A code generation and correlator.

Figure 3. Simulink block diagram of DSP.
4. Simulation Stage FPGA Partition

The Simulation Stage of FPGA Partition used the MATLAB or Simulink to simulate and validate each phase of the GPS receiver which are working or providing a good output. It is used to implement and designed for acquisition and tracking phase’s complete diagram by symbols, and a DSP environment is also used for implementation of navigation solution phase block. This algorithm codes are written in the C or C++ programming language. In this paper we are introducing the concept of the Matlab simulation as well as implementation of all the phases of the GPS receiver with the SPS service. Matlab Simulink are used to design the block of the every phase of the GPS receiver and also called graphical programming language. FPGA Partition is utilizing an environment which is suited to simulation as well as implementation stages. These stages have made the designer and developer’s mind enthusiastic every time in enhancing and developing the given algorithm. We consumed less time on the programming. It has made FPGA partition on same GPS specification one is without jammer as shown in [Figure 4] and second one with the jammer as shown in [Figure 5]. In this block it is used timing control unit, farrow variable delay and C/A code generation and correlator all these block makes a complete FPGA GPS receiver.

Figure 4. Simulink Block diagram of FPGA without jammer.

Figure 5. Simulink Block diagram of FPGA with a jammer.

Figure 6. Simulink block diagram of GPS receiver processing captured satellite data.

A GPS receiver channel was implemented on Simulink based on the functional block diagram of the GPS with combined timing control unit and farrow variable delay. An addition of a jammer block, the signal capacity and signal display power is reduced. This jammer is also
designed by Simulink having data type conversion and variable fractional delay block. Jammer has two input block in Simulink one is variable fractional delay block output and second one is same GPS input signal passes through the jammer. This jammer is using same GPS input signal but power of the signal is 10 times of the signal strength.

5. Implementation Result

A complete “GPS receiver processing captured satellite data” is having main three Simulink model as: GPS input signal, FPGA partition and DSP portion; all these three blocks make this model complete as shown in [Figure 6]. In which an error - Doppler Effect occurs when the frequency of Doppler shift occurs by the radioactive motion of GPS transmitter and receiver signal and this signal affects both acquisition and tracking command.

In the model with Jammer of FPGA partition, the “GPS Receiver Processing Captured Satellite data” model of GPS system, without jammer, the signal level display shows the value 0.1779. But in case if it uses a jammer, the signal level is reduced to 0.1447 which is 81% of the initial signal level. So Jammer blocks are used to reduce the signal strength and makes the signal weaker.

6. Conclusion

In this paper we have measured the performance of GPS receiver with and without jammer using 29 satellites, after the calculation and simulation we have concluded that after introducing jammer the signal level reduced to 81% initial level. Thus the jammer block has performed very well to reduce the signal strength.

7. References

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