Low temperature (<200°C) solution processed tunable flash memory device without tunneling and blocking layer

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Intrinsic charge trap capacitive non-volatile flash memories take a significant share of the semiconductor electronics market today. It is a challenge to create intrinsic traps in the dielectric layer without high temperature processing steps\textsuperscript{[1]}. While low temperature processed memory devices fabricated from polymers have been demonstrated as an alternative\textsuperscript{[2–7]}, their performance degrades rapidly after a few cycles of operation\textsuperscript{[8–14]}. Moreover conventional memory devices need the support of tunneling and blocking layers since the memory dielectric or polymer is incapable of preventing memory leakage\textsuperscript{[15–17]}. The main issue in designing a memory device is to optimize the leakage current and intrinsic trap density simultaneously\textsuperscript{[18]}. Here we report a tunable flash memory device without tunneling and blocking layer by combining the discovery of high intrinsic charge traps (>10\textsuperscript{15} cm\textsuperscript{−2}) together with low leakage current (<10\textsuperscript{−7} A.cm\textsuperscript{−2}) in solution derived, inorganic, spin-coated dielectric films which were heated at 200°C or below. In addition, the memory storage is tuned systematically up to 96\% by controlling the trap density with increasing heating temperature.

Today’s semiconductor memory technology is dominated by silicon-oxide-nitride-oxide-silicon (SONOS) non-volatile flash memory which is based on intrinsic charge traps in silicon-rich silicon nitride films deposited by high temperature (~780°C) compatible chemical vapor deposition\textsuperscript{[19, 20]}. The intrinsic charge traps in silicon-rich silicon nitride films were first reported in 1967\textsuperscript{[21]} and the first flash memory device incorporating silicon nitride charge storage was demonstrated in 1980’s\textsuperscript{[22]}. However the trap density and distribution are difficult to control in such material\textsuperscript{[23]}. Traps can be increased by ion bombardment and plasma-passivation\textsuperscript{[24]}, but the leakage current increases. Alternate high-k dielectrics such as TiO\textsubscript{2}, HfO\textsubscript{2}, ZrO\textsubscript{2}, etc. are excellent insulators for transistor applications\textsuperscript{[21, 27]}; but do not have the intrinsic charge trapping properties as silicon nitride. Although solution processed HfO\textsubscript{2} has been used to fabricate SONOS type flash memory\textsuperscript{[1]}, the devices required the support of additional dielectric layers which were deposited by sophisticated ultrahigh vacuum techniques with high temperature processing steps to improve the memory leakage. For most dielectrics, precursor solutions with organic solvents result in poor leakage current which can be improved to some extent by high heating temperature\textsuperscript{[25]}. However the high temperature heating process lowers leakage current but reduces trap density. Hence, the main challenge is to simultaneously achieve deep intrinsic charge traps together with very low leakage current at low processing temperatures. There are a few reports on solution processed flash memory by using polymer materials\textsuperscript{[29, 30]} but these devices degrade after only a few cycles of operation in normal environmental conditions and they are not capable of working at higher temperatures.

In the last few years, a novel inorganic, completely carbon free, water soluble dielectric Aluminium Oxide Phosphate (ALPO), has been successfully employed as gate dielectric in high performance TFTs that are competitive with a-Si TFTs\textsuperscript{[31]}. Due to its very low leakage current density, it was used recently as tunneling and blocking layer to fabricate fully solution processed two terminal capacitive flash memory devices\textsuperscript{[32]} with CdTe-NP as the charge storage center. Nevertheless a fully spin-coated low temperature processed (below 200°C) high-performance flash memory device without tunneling and blocking layers has not been reported so far.

Here we report the discovery of ultra-high number of intrinsic charge traps (>10\textsuperscript{12} cm\textsuperscript{−2}) in low temperature solution processed inorganic ALPO dielectric. At the same time, the leakage current is sufficiently low (<10\textsuperscript{−7} A.cm\textsuperscript{−2}) for flash memory operation without incorporating tunneling or blocking layers. In addition, the number of traps can be varied with heating temperature, which is strongly correlated with the oxygen vacancy concentration in the film. Furthermore, we demonstrate optimized robust high performance fully solution processed inorganic oxide precursor based flash memory devices without tunneling and blocking layer, where the processing temperature does not exceed 200°C. Our devices outperform other similar memory devices reported earlier\textsuperscript{[2–7]}.

A schematic of typical device architecture is depicted in Fig. 1a. ALPO is deposited by spin-coating a completely inorganic, carbon free and aqueous precursor solution on low-doped p-silicon substrate (p ≈ 4×10\textsuperscript{15} cm\textsuperscript{−3}). After deposition various substrates are heated at different temperatures including at low temperature such as 200°C. The inset of Fig. 1a shows a schematic of molecular structure of the low temperature (200°C) processed ALPO. The thickness of the deposited film is measured by ellipsometry (see Section I, Supporting Information) and verified by cross-sectional scanning electron microscope (SEM) image (Fig. 1b). Such prepared films are found to be atomically smooth showing surface roughness to be
FIG. 1. Device and deep level charge trapping response: (a) Schematic of device architecture. (b) Cross-sectional SEM image of a typical device (thickness ~139 nm). (c)(top-panel) AFM topography of the surface of the devices. (bottom-panel) Optical image of an array of devices. (d) C−V traces of as prepared (AP), heated at 200°C and 600°C respectively (also see Section II, Supporting Information). The heating was done for 1 hr for each sample. C−V was measured with the up-down DC sweep of ±20 V at a rate of 2V min⁻¹ on the gate (Gate Bias) of the MIS while imposing a small AC with amplitude and frequency of 100 mV and 100 kHz respectively. (e) Variation of hysteresis window (ΔVFB) as a function of heating temperature. (inset) variation of trap density as a function of heating temperature.

∼0.08 nm[28, 33] which is determined by the atomic force microscopy (AFM) with an areal scan over 50µm×50µm (top-panel, Fig. 1c). An aluminum contact is deposited thereafter by thermal evaporation for the purpose of electrical measurement. The deep level charge storage in the deposited ALPO is characterized via capacitance-voltage (CV) measurement. An optical image of device on chip has been shown in the bottom-panel of Fig. 1c.

Intrinsic trap levels in ALPO cause a hysteretic output of the CV traces highlighting the memory-like behavior of the devices (Fig. 1d). Further, the trap density can be varied by heating the samples at different temperatures which alters the hysteresis-window. For example, an as-prepared sample shows a memory window of ∼12.9 V (left-panel) which corresponds to a trap density of n ~5.65×10¹² cm⁻², where as, an ALPO-film heated at 200°C for one hour shows a hysteresis window of ∼17.5 V which corresponds to the trap density of n ~ 6.37×10¹² cm⁻². When the film is heated at 600°C, the trap density drastically reduces (n ~ 10¹¹ cm⁻²) causing a significantly low hysteresis window (~ 2.2 V, right-panel). A similar variation of electronic traps with heating temperature is also observed from the devices which are made with lower thickness ALPO film, however, there is no affect due to change in device dimension (see Section III, Supporting Information). From the sweep direction of the CV curve it is inferred that gate injection of carriers controls the memory operation. Although conventional flash memory architecture follows channel injection of carriers[20], the interface degrades fast in such devices[34]. Thus, compared to channel injected devices, gate-injected devices show higher endurance which is one of the key requirements of memory operation[35]. Because of such advantages, the quest for efficient gate-injected flash memory devices is ongoing[34–37]. A systematic change in the hysteresis window as a function of heating temperature is presented in Fig. 1e, where, solid squares are the experimental data, shaded region is guide to the eye and the width of the shaded region indicate the standard deviation around their mean vertical position estimated from similar results. Use of higher heating temperature (> 600°C) causes a dramatic reduction in trap density, thus reducing the hysteresis window. A 96% reduction in trap density (n ~ 2.19×10¹¹ cm⁻²) is observed at an heating temperature of ~800°C resulting a memory window of 0.7 V only. In addition, a negligible degradation in CV hysteresis is obtained from as prepared devices even after 5 years of storage in ambient conditions (see Section IV, Supporting Information). This demonstrates that the devices are very stable for long term application, in spite of the water absorbing property of ALPO[38, 39].
In order to investigate the robustness of intrinsic charge storage property of ALPO, we demonstrate a series of memory operations on the metal-insulator-semiconductor structured (MIS) two terminal capacitive devices which were heated at 200°C. The memory characterization focuses upon the flat band voltage shift ($\Delta V_{FB}$) due to the voltage sweep operation (i.e. erasing (E) or programming (P) operation) on the gate terminal of the devices. A device is programmed (P) or erased (E) by sweeping the gate voltage at a slow rate [32]. Sequential P and E cycles set and reset the flat band voltage reversibly and is confirmed from the nearly constant $V_{FB}$ values obtained from multiple E-P cycles (Fig. 2a). Two of the C-V traces corresponding to the 1st and 20th E-P traces are shown in the inset of Fig. 2a. Nearly constant values of $V_{FB}$ in E and P states indicate that E-P cycles have negligible effect on the memory state thus indicating high reliability of the devices.

Frequency and gate bias dependent $\Delta V_{FB}$ changes are shown in Fig. 2b. Flatband voltage window shows insignificant change within the range of 10-1000 kHz frequency of excitation voltage. Such behavior is attributed to the slow trapping-de-trapping phenomena which thus indicates that the states can be probed by deploying high speed CV measurement. With different gate bias voltages $\Delta V_{FB}$ increases first and then shows a decrease. Such behavior appears because of the competition between the trap filling and charge losses. Initially (∼5-20 V) as the sweep voltage is increased, larger electric field causes more charge injection into the traps, hence, the hysteresis width increases. Beyond 20 V, which corresponds to an electric field of ∼1.2 MV.cm⁻¹, the high leakage current (see Section V, Supporting Information) leads to increased charge loss, thus a reduction in hysteresis window is observed (Fig. 2b). A hysteresis window of 15 V is obtained for a sweep voltage range of ±15 V which corresponds to an optimum memory window of 50% of the total sweep-range. The result of 50% window for intrinsic traps in ALPO exceeds previously reported values [41] for other dielectrics. It is known from literature that the high performance operation of flash memory stack should not have leakage current density more than $10^{-6}$ A.cm⁻² when operated with an electric field of 1 MV.cm⁻¹ [41]. The ALPO devices show a leakage current density of ∼4.5×$10^{-8}$ A.cm⁻² only at -1 MV.cm⁻¹ electric field. Such low leakage current not only meets the criteria for the application of high-performance flash memory devices, but also outperforms other solution processed inorganic dielectrics namely Al₂O₃ [24], HfO₂ [25], ZrO₂ [26], and TiO₂ [27], which show typical leakage currents ∼$10^{-5}$ A.cm⁻², ∼$10^{-7}$ A.cm⁻², ∼$10^{-2}$ A.cm⁻² and ∼$10^{-5}$ A.cm⁻² respectively at 1 MV.cm⁻¹. This observation for ALPO also ensures that high quality flash memory devices can be fabricated without the need of blocking or tunneling layers.

True program (P) and erase (E) operations are realized by application of positive and negative square pulses respectively. Whereas the read operation is performed by using triangular pulses having shorter time periods (T ∼4 µs). Since high speed voltage sweep does not alter the memory state (Fig. 2b), shorter triangular pulses are expected to probe the E and P states without disturbing them. By varying the width of the square-pulses, various memory-windows ($V_{FB}|_P - V_{FB}|_E$) are obtained and shown in Fig. 2c. While using a single pulse to program or erase, a pulse width of 500 ms can set the memory window to be as large as ∼9 V. The program/erase speed of these devices is found to be ∼200 ms which is significantly faster compared to other solution processed flash memory devices [19, 22, 43]. During programming and erasing, a maximum charge capturing efficiency of 7.46 % is estimated while operating with a gate electric field of 2.37 MV/cm (see Section VI, Supporting Information). This capturing efficiency is higher than the reported values obtained from other dielectrics [46].
FIG. 3. Robust flash memory operation: (a) Program-disturb (PD) verification with high-speed $C−V$ measurement system. (Inset) $C−V$ traces from low speed (gray-traces) and high speed (red and green traces) measurements. Red colored lines indicate back-and-forth sweeps at high speed (time period $(T)=4\,\mu s$) while the sample is in programmed state. Green colored lines indicate back-and-forth sweeps at high speed (time period $(T)=4\,\mu s$) while the sample is in erased state. (b) Endurance characteristics of the device. (Inset) Shape of the pulses used in program $(P)$, erase $(E)$ and read operations. (c) Retention characteristics of the flash memory device. Programming of the state was done with a square pulse of height $\pm 33\,V$ and having a duration of 500 ms. (d) Retention characteristics of the flash memory device after endurance test of 10k cycles. (e) $P/E$ test of the flash memory devices at various temperatures. Lines are the guide to eye. (f) The statistical distribution of flash memory window for 47 devices. For this test applied $P/E$ voltage is $\pm 33\,V$ for 300 ms.

To check for any disturbance of the program/erase state during the read operation, the device is set to $E$ or $P$ states first with a single long square pulse ($T\sim 0.5\,s$, see Fig. 2c) and then multiple high-frequency triangular ($T\sim 4\,\mu s$) pulses were applied representing multiple read operations. Figure 3a shows the statistical distribution of $V_{FB}$ values obtained from such multiple read operations for both the $E$ and $P$ states. Narrow distributions of $V_{FB}$ indicate low read-disturb for both the states. Inset of Fig. 3a shows typical $C-V$ traces for $E$, $P$ and read operations. Here two red and two green lines indicate back-and-forth sweep of the voltage $(V_G)$ using the high speed triangular read pulse probing the $P$ and $E$ states respectively.

Erase-program operation over 10 k cycles shows no degradation in memory window thus demonstrates high endurance (Fig. 3b). In fact, with the increasing operation cycle memory window increases which may be attributed to the generation of additional trap states because of electrical stress. Data retention was tested by programming a fresh device at room temperature with pulses of amplitude 33 V and duration 500 ms. The device shows almost no change in memory window within $\sim 10^4$s which was the limit of experimental time scale. This is the highest reported retention time for any memory device without additional tunneling and blocking layers. Even after 10 k $P/E$ cycles devices show a degradation of only 9% memory window after $\sim 10^4$s (Fig. 3d). Temperature dependent data retention was also tested and presented in Fig. 2e. After $10^4$s of operation a memory window loss of 25% and 50% are observed at $60^\circ C$ and $80^\circ C$ respectively. The reliability is also tested on the device made with lower thickness of ALPO film (91 nm) which shows equivalent performance as obtained from the other devices (see Section VII, Supporting Information).

To examine the scalability of these low temperatures processed memory devices, we prepared and characterized more than 40 devices. Statistical distribution of memory window for all these devices are shown in Fig. 3f. 80% of devices lie within the expected memory window (3−4V) when programmed with $\pm 33\,V$ pulse height and 300 ms duration. The remaining 20% devices show a memory window of less than 3V. These preliminary results show sufficiently high yield for large scale production needed for practical applications.

Microscopic origin of memory operation is understood from the temperature controlled trap density variation which is confirmed from photo-emission spectroscopy (XPS). Multiple samples were prepared at different heating temperatures and studied with XPS. The shape of the
FIG. 4. Temperature dependent changes in trap states: (a) Core level O 1s spectra from different temperature heated film. Thick arrow indicate movement of the peaks obtained from samples heated with different temperatures. (b)-(d) Core level oxygen peaks from as−prepared, 200°C and 400°C heated ALPO films respectively. The oxygen peak(red) in each case is de-convoluted into three components corresponding to oxygen vacancies (M-O\text{vac}) ∼ green, lattice oxygen (M-O) ∼ blue and metal hydroxide (M-OH) ∼ cyan. (e) Atomic composition ratios of oxygen in ALPO thin films as a function of temperature. (inset) increment of traps O\text{vac} at 200°C with respect to AP ALPO film. (f) Schematics showing condensation mechanism of oxide precursors by heating. The first block denotes the individual molecules, second and third are low and high temperature processed ALPO films respectively. All molecular models were constructed using MolView(http://molview.org/). Escape of water molecules (black circle) shown in third block leads to the decrease in the trap states as well as the decrease of the thickness of the film.

Temperature dependent changes in trap states: oxygen peak changes systematically with respect to heating temperature (Fig. 4a). De-convolution of XPS signal into respective peaks of oxygen vacancies(M-O\text{vac}), metal hydroxide(M-OH) and lattice oxygen(M-O) helps understanding the contributions of respective states (Fig. 4b-d). The ALPO film which was heated at 200°C has similar ratio (atomic %) of aluminum (Al), oxygen (O) and phosphorous (P) as that of the mother solution (see Section VIII, Supporting Information). Due to addition of HCl in the ALPO precursor, a small percentage of chlorine is observed (see Section IX, Supporting Information) in low temperature processed ALPO film. It is observed that M-O\text{vac} intensity sharply decreases with increase in heating where temperature reaches above 200°C (Fig. 4b-d and Section X of Supporting Information). As the heating temperature increases, hydrogen is lost as water vapor and the film becomes denser. The M-O peaks increase with higher heating temperature (Fig. 4e-f). This is consistent with the reduction in the number of oxygen vacancies and consequently lower trap density in samples heated at higher temperature. A quantitative comparison between the peak intensity and the trap density of the heated film reveals a strong correlation between the oxygen vacancies and trap densities (see Section X, Supporting Information), thus indicating that the oxygen vacancies are the responsible entities for memory states.

In conclusion we have shown fabrication and high quality performance of low temperature processed (<200°C) inorganic flash memory devices which do not require tunneling or blocking layers. Simple sample fabrication technique involving spin-coating of solution is another advantage. Narrow distribution of memory window obtained from more than 40 samples indicates the scalability of the fabrication method. In spite of having no tunneling and blocking layers, these devices show extremely low leakage current which is one of the key features of memory operation, and demonstrate high endurance, high retention, thus, outperforming other solution processed memory devices reported so far. Temperature dependent control on trap density also helps optimizing the memory window.
ALPO based devices pave the way for designing a new class of scalable two terminal flash memory devices for practical applications.

METHODS

Material growth: Precursor solution of Aluminium Oxide Phosphorate, ALPO [Al2O3−x (PO4)2x] in water (18 MΩ cm) was prepared with Al(OH)3 (99%, Alfa Aesar, USA) and an appropriate amount of H3PO4 (ExcelaR Grade, Thermo Fisher Scientific, USA) and an appropriate amount of HCl (AR Grade, Thermo Fisher Scientific, USA) was added to obtain P/Al = 0.5 with concentration of 0.5 M. The solution was stirred under heat of 90°C in a water bath for 24 hours.

Device fabrication: Two terminal MIS structures were fabricated on piranha cleaned [H2SO4:H2O2 = 3:1] lightly doped silicon substrate (p−Si). The ALPO solution was spin-coated at 3000 rpm for 30s to form the gate dielectric. The films were then heated at 150°C for 1 min. This process was repeated for 2-3 times to achieve the desired thickness. The sample was exposed to oxygen plasma for 5 to 10 mins at 0.5 mbar pressure before deposition of each layer. Such fabrication process may help generation of stable traps in ALPO below 200°C. Typically, ALPO based devices are treated at high temperature (>350°C) to achieve better dielectric performance, thus, most of the reported devices do not show any memory effect[3]. For control devices the film was further heated at 800°C for one hour in ambient to achieve the trap free oxide. A 200 nm aluminium gate was deposited by thermal evaporation at ~ 10−6 mbar pressure. Before deposition of the top aluminium gate, the ALPO films were heated at different temperature in a preheated furnace for one hour. All devices were stored under ambient conditions and no degradation of CV curves was found even after three years.

Characterization: ALPO precursor solutions prepared with different concentrations and P/Al ratios were optically characterized using a UV-Visible spectrophotometer. They are all transparent in visible wavelength range with the main absorption peak in the ultra-violet range at 235 nm. After spin coating and heating, the film shows a refractive index 1.5 (see Section I, Supporting Information) with negligible absorption at 550 nm as measured by ellipsometry (M-2000, J.A. Woollam Co. Inc., USA). The thickness of ALPO film on silicon substrate extracted from ellipsometry is 139 nm and verified with cross-sectional SEM (Ultra 55, Carl Zeiss). The surface of the ALPO film is atomically smooth with a roughness of 0.08 nm as measured by AFM (ND—MDT, Russia). The CV curve was measured with HIOKI 3532 LCR meter and Keithley 2400 source meter. Agilent Device Analyzer B1500A was used to measure the IV characteristics in ambient environment. The leakage current and CV measurements were performed on more than 50 devices. The entire measurement was done in continuous mode of the instrument. The high speed CV measurement was performed with home made CV measurement system[2]. The XPS measurements were carried out by AXIS 165 with Al Kα radiation (9mA, 13keV, 1486.6 eV) in ultra—high vacuum. The XPS spectra were calibrated with C 1s peak (284.6 eV).

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**AUTHOR CONTRIBUTIONS**

S.M., V.V. conceived the project. S.M. designed and performed the experiments, completed characterization of the fully solution processed flash memory device. S.M. analyzed results and wrote the paper.

**ADDITIONAL INFORMATION**

Supplementary information is available in the online version of the paper. Correspondence and requests for materials should be addressed to S.M.