State-of-the-Art $β$-Ga$_2$O$_3$ Field-Effect Transistors for Power Electronics

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ABSTRACT: Due to the emergence of electric vehicles, power electronics have become the new focal point of research. Compared to commercialized semiconductors, such as Si, GaN, and SiC, power devices based on $β$-Ga$_2$O$_3$ are capable of handling high voltages in smaller dimensions and with higher efficiencies, because of the ultrawide bandgap (4.9 eV) and large breakdown electric field (8 MV cm$^{-1}$). Furthermore, the $β$-Ga$_2$O$_3$ bulk crystals can be synthesized by the relatively low-cost melt growth methods, making the single-crystal substrates and epitaxial layers readily accessible for fabricating high-performance power devices. In this article, we first provide a comprehensive review on the material properties, crystal growth, and deposition methods of Ga$_2$O$_3$, and then focus on the state-of-the-art depletion mode, enhancement mode, and nanomembrane field-effect transistors (FETs) based on $β$-Ga$_2$O$_3$, for high-power switching and high-frequency amplification applications. In the meantime, device-level approaches to cope with the two main issues of $β$-Ga$_2$O$_3$ namely, the lack of p-type doping and the relatively low thermal conductivity, will be discussed and compared.

INTRODUCTION

Gallium oxide, as a type of semiconducting sesquioxide, has been known for decades.$^{1−3}$ In recent years, owing to the tremendous progress in crystal growth and epitaxy techniques,$^{4−8}$ gallium oxide, particularly $β$-Ga$_2$O$_3$, has attracted renewed attention as one of the fourth-generation ultra-wide-bandgap (UWBG) semiconductors, in addition to AlGaN, diamond, and cubic boron nitride.$^9$ In comparison to the well-established SiC and GaN technologies, $β$-Ga$_2$O$_3$ with a larger energy bandgap (4.9 eV) exhibits higher breakdown electric field (8 MV cm$^{-1}$) and better Baliga’s figure of merit (BFOM) (Table 1), suggesting much less power loss incurred in the power devices based on $β$-Ga$_2$O$_3$. $^{10−14}$ The first single-crystal field-effect transistors (FETs) based on $β$-Ga$_2$O$_3$ homoepitaxial layers were demonstrated in 2012.$^{15}$ Furthermore, since the $β$-Ga$_2$O$_3$ crystals can be synthesized by various melt growth methods at atmospheric pressure, such as the floating zone (FZ), Czochralski (CZ), and edge-defined film-fed growth (EFG) methods, the cost for producing large-area, uniform, single-crystal substrates can be greatly reduced.$^{16−18}$ In contrast, the bulk crystals of SiC and GaN can only be manufactured by the less efficient vapor growth methods, such as the sublimation method for SiC crystals and the sodium flux and ammonothermal methods for GaN crystals.$^{16−18}$ So far, $β$-Ga$_2$O$_3$ wafers with diameters up to 4 in. have already been demonstrated or commercialized by companies, such as Tamura, Koha, and Novel Crystal Technology.$^9$ Due to its UWBG nature, $β$-Ga$_2$O$_3$ has found various optoelectronic applications, including solar-blind deep ultraviolet (DUV) photodetectors and transparent conductive oxide (TCO) electrodes for the light emitting diodes (LEDs).$^{19,20}$ Furthermore, the $β$-Ga$_2$O$_3$ nanowires and thin films with extraordinary chemical and thermal stabilities have been explored as highly sensitive gas sensors,$^{21}$ and the amorphous and stoichiometric Ga$_2$O$_3$, thin films deposited on GaAs (001) substrates can potentially serve as the GaAs gate dielectrics.$^{22}$

As electric vehicles revolutionize the automotive market, power electronics, a vital component of electric powertrains alongside batteries and traction motors, have emerged as a new research focus. The power electronics in electric vehicles mainly include the AC-to-DC rectifiers for charging the batteries, the DC-to-DC converters between high- and low-voltage batteries, and most importantly, the DC-to-AC...
inveters for powering the traction motors. Any performance enhancement in the power devices, particularly high-power
inveters, can considerably extend the vehicle driving range with the same battery capacity. Nowadays, the vast majority of
electronic systems are built upon Si, and thanks to the modern semiconductor manufacturing technologies, the performance
of Si-based devices has improved dramatically over the past few decades. On the other hand, for the power electronics, it was
demonstrated that with the same breakdown voltage and semiconductor manufacturing technologies, the performance
of Si-based devices has improved dramatically over the past few decades. As early as 1952, various polymorphs of Ga
mobility.


Table 1. Material Properties, BFOMs, JFOMs, and HCAFOMs of Different Semiconductors, Including Si, GaAs, 4H-SiC, GaN,
β-Ga2O3, and Diamond

| Crystal Type | Crystal Structure | Energy Bandgap (eV) | Dielectric Constant ($\varepsilon_r$) | RT Electron Mobility ($\mu_0$, cm² V⁻¹ s⁻¹) | Breakdown Electric Field ($E_{BR}$, MV cm⁻¹) | Electron Saturation Velocity ($v_{sat}$, $\times 10^7$ cm s⁻¹) | Thermal Conductivity ($\kappa$, W m⁻¹ K⁻¹) | BFOM ($\epsilon_r$) | JFOM ($\varepsilon'_r$) | HCAFOM ($\varepsilon''_r$) |
|--------------|------------------|---------------------|-------------------------------|--------------------------------|--------------------------------|--------------------------------|------------------|------------------|------------------|------------------|
| Si           | Face-Centered Cubic | 1.1                | 11.8                          | 1400                          | 0.3                           | 1                             | 150              | 1               | 1               | 1               |
| GaAs         | Zinc Blende       | 1.4                | 12.9                          | 8000                          | 0.4                           | 1.2                           | 55               | 15              | 2               | 5               |
| 4H-SiC       | Cubic and Hexagonal | 3.3                | 9.7                           | 1000                          | 2.5                           | 2                             | 270              | 340             | 17              | 48              |
| GaN          | Wurtzite          | 3.4                | 9.0                           | 1200                          | 3.3                           | 2.5                           | 210              | 870             | 28              | 85              |
| β-Ga2O3      | Monoclinic        | 4.9                | 10                            | 300                           | 8                             | 2                             | 13 [100]         | 3444            | 53              | 279             |
| Diamond      | Face-Centered Cubic | 5.5                | 5.5                           | 2000                          | 10                            | 1                             | 1000             | 24644           | 33              | 619             |

The BFOM, JFOM, and HCAFOM of Si are normalized to 1.

As early as 1952, various polymorphs of Ga2O3 and phase equilibria of the Al2O3-Ga2O3-H2O systems were determined.1 The five polymorphs are α, β, γ, δ, and ε, where the α-phase is corundum, β-phase monoclinic, γ-phase defective spinel, ε-phase orthorhombic, and δ-phase most likely orthorhombic.1,2,4 In general, the theoretical formation energies of the five polymorphs follow the tendency of $\beta < \varepsilon < \alpha < \delta < \gamma$.25 As a result, the monoclinic β-Ga2O3 is the most stable structure, while the remaining polymorphs are metastable. Furthermore, due to its high melting point of ~1793 °C, β-Ga2O3 is the only polymorph whose bulk crystal can be grown by using the melt growth methods.26 In comparison, the metastable ε-Ga2O3 and α-Ga2O3 can only withstand temperatures up to 870 and 600 °C, respectively. In fact, all phases ofGa2O3 can transition to other phases by annealing and would eventually end up transforming to the most stable β-phase.4 Therefore, until now the great majority of research on gallium oxide has been devoted to β-Ga2O3. On the other hand, the heteroepitaxy of α-Ga2O3 and ε-Ga2O3 on sapphire substrates has also attracted much attention, because compared to the monoclinic β-Ga2O3, the corundum α-Ga2O3 and the orthorhombic ε-Ga2O3 have a better symmetry match with the hexagonal c-plane sapphire substrates.27–30

The β-Ga2O3 has a monoclinic crystal structure with the space group of C2/m and the lattice constants of $a = 12.2 \text{ Å}$, $b = 3.0 \text{ Å}$, and $c = 5.8 \text{ Å}$, and $β = 104°$ (Figure 1).24 The β-Ga2O3 crystal is composed of sixfold coordinated Ga–O octahedra and fourfold coordinated Ga–O tetrahedra. The different arrangements of Ga and O atoms along different directions lead to anisotropic physical properties. For example, the thermal conductivity along the [010] direction is 21 W m⁻¹ K⁻¹, while it is 13 W m⁻¹ K⁻¹ along the [100] direction.31–33 The static dielectric constants of β-Ga2O3 perpendicular to the (100), (010), and (001) planes are also slightly different from each other.34 The β-Ga2O3 crystal structure has two cleavage planes, namely, (100) and (001), and since the lattice parameter along the [100] direction is higher than the [010] and [001] directions, it is easy to exfoliate ultrathin films along the (100) plane direction.13 After washing with organic solvents and annealing in oxygen ambient, the typical β-Ga2O3 wafer surface should exhibit a regular step-and-terrace morphology. The terrace width is a function of the substrate disorientation; the smaller the miscut angle, the larger the
terrace width of the substrate. The typical atomic force microscopy (AFM) image reveals that the (100) plane of a β-Ga2O3 substrate with a miscut angle of ~0.2° has the terrace width of 70 to 100 nm. During homoepitaxy, the adhesion energy on the terraces of the (100) plane is weaker than at the steps and kinks, therefore promoting the step-flow growth.65

The energy bandgap of pure β-Ga2O3 has been determined to be 4.7–4.9 eV.66,67 Therefore, β-Ga2O3 should be transparent from the UV to visible range, as evidenced by the clear crystal, 2-in.-diameter Ga2O3 wafer synthesized by the EFG method.68,69 The intrinsic electron mobility in the drift layers is typically n-type with carrier concentrations in low 1017–1018 cm−3. The electrical conductivity could be further enhanced by intentionally doping with shallow dopants, such as Si, Ge, and Sn. On the contrary, Mg and Fe are often used as the compensating acceptors for obtaining semi-insulating (UID) β-Ga2O3. For evaluating different semiconductors for the power device application, in addition to the BFOM, which only accounts for the DC conduction loss, the Johnson figure of merit (JFOM, power-frequency product) and the Huang’s chip area manufacturing (HCAFOM, manufacturability and expense) are also commonly considered. Thanks to the high breakdown electric field (8 MV cm−1), the JFOM and HCAFOM of β-Ga2O3 obviously stand out in comparison to Si, GaAs, SiC, and GaN (Table 1).

## CRYSTAL GROWTH OF GALLIUM OXIDE

Being able to grow bulk single crystals by using the relatively low-cost melt growth methods is one significant advantage of β-Ga2O3. In 1964, the first melt-grown β-Ga2O3 crystals were obtained with the use of the Verneuil method.72 However, not so many relevant research activities had been reported in the following years until 1996, when the FZ method was used to grow β-Ga2O3 single-crystal boules with diameters up to 8 mm were successfully synthesized by the FZ method.73,74,75 The starting material of the FZ method is SN-grade β-Ga2O3 powder, which is pressed into rods by a cold isostatic press process (50 to 300 MPa). Then, the rods are sintered at ~1500 °C in air for 10 h. During the crystal growth, the sintered rod is positioned on the upper shaft, slowly rotating in an opposite direction to a β-Ga2O3 seed crystal positioned on the lower shaft. Four high-power (1.5 kW) halogen lamps and the corresponding ellipsoidal mirrors are used as the heating system. The growth rate is 1 to 20 mm h−1 under dry air or synthetic air (21 vol % O2 + 79 vol % N2) flow. The crystal growth process is illustrated in Figure 2A. The major concerns of the FZ method are the collapse of the liquid melt which is barely held by the surface tension and the crack formation in the grown crystal due to high thermal gradients.

The feasibility of using the CZ method with Ir crucibles for growing β-Ga2O3 single crystals was demonstrated in 2000,76 and major improvements have been made since 2010.77–79 The starting material, SN-grade β-Ga2O3 powder, is first placed in the Ir crucible, which is heated by the surrounding radiofrequency (RF) inductor to form the β-Ga2O3 melt. A seed crystal is introduced into the melt and then slowly pulled up (1 to 2 mm h−1) while rotating (5 to 10 rpm). The crystal growth process is illustrated in Figure 2B. The β-Ga2O3 cylindrical boules with diameters up to 50 mm can be obtained using this method.80 The major concern of the CZ method is the decomposition of Ga2O3 into volatile species, such as Ga3, GaO, and Ga2O, in an oxygen-deficient atmosphere. On the contrary, the Ir crucible and other Ir parts are prone to oxidation in an oxygen-rich atmosphere. It was found that an appropriate growth atmosphere comprising CO2, Ar, and O2 along with overpressure, can effectively suppress the decomposition of Ga2O3 without harming the Ir crucible.81 The influence of other parameters on the grown crystal quality, such as furnace design, crucible aspect ratio, crystal-to-crucible diameter ratio, heating and cooling rates, growth and rotation rates, seed preparation, and crystallization ratio, have also been investigated.82

The EFG method, featuring high growth speed and precise control of crystal size and shape via the use of a die, has been applied to the growth of β-Ga2O3 since 2008.83 Similar to the FZ and CZ methods, the starting material of the EFG method is SN-grade β-Ga2O3 powder, which is placed in an Ir crucible along with an Ir die in the middle. The heating of the crucible is carried out by using an RF induction coil. Once the melting point is reached, the β-Ga2O3 melt moves up through the slit of the Ir die by capillary force, and a β-Ga2O3 seed crystal is positioned in contact with the melt on top of the die to initiate the crystal growth process, as illustrated in Figure 2C.84 The shape of the grown crystal is determined by the shape of the top surface of the die. The growth rate can reach 15 mm h−1 under the growth atmosphere comprising 2 vol % O2 + 98 vol
Table 2. Homoepitaxy of $\beta$-Ga$_2$O$_3$ Layers on (100) and (010) $\beta$-Ga$_2$O$_3$ Substrates, by Various Epitaxy Techniques, Including MOCVD, LPCVD, HVPE, and PA-MBE$^a$

| Epitaxial Layers | Substrates | Conditions | Homoepitaxy | Crystal Characteristics |
|-----------------|------------|------------|-------------|-------------------------|
| (A) $\beta$-Ga$_2$O$_3$ | (100) $\beta$-Ga$_2$O$_3$ | MOCVD: TMGa and O$_2$ or H$_2$O; 750−850 °C; 5−100 mBar | Nanocrystals of Ga$_2$O$_3$ were formed with O$_2$ as oxidant, while smooth epitaxial layers of Ga$_2$O$_3$ were formed with H$_2$O as oxidant. | 7 |
| (B) Sn-doped $\beta$-Ga$_2$O$_3$ | (100) $\beta$-Ga$_2$O$_3$ | MOCVD: TEGa, O$_2$, and TESn; 850 °C; 5 mBar | RMS surface roughness of ~0.6 nm was achieved. The maximum electron mobility of 41 cm$^2$ V$^{-1}$ s$^{-1}$ was obtained with the carrier concentration equal to $1 \times 10^{18}$ cm$^{-3}$. | 61 |
| (C) $\beta$-Ga$_2$O$_3$ | (100) $\beta$-Ga$_2$O$_3$ | MOCVD: TEGa and O$_2$; 850 °C; 5 mBar | The Ga$_2$O$_3$ layer grown on a substrate with 0.1° miscut angle exhibited high twin lamella (stacking fault) density, while the layer grown with 6° miscut angle exhibited nearly zero twin lamella. | 62 |
| (D) Sn- and Si-doped $\beta$-Ga$_2$O$_3$ | (010) $\beta$-Ga$_2$O$_3$ | MOCVD: TEGa, O$_2$, TEOS, and TESn; 850 °C; 5 mBar | A RMS surface roughness about 0.6 nm was achieved. No dislocations or planar defects were observed. The maximum electron mobility of about 130 cm$^2$ V$^{-1}$ s$^{-1}$ was obtained with the carrier concentration equal to $1 \times 10^{17}$ cm$^{-3}$ regardless of the dopant type. | 64 |
| (E) $\beta$-Ga$_2$O$_3$ | (010) $\beta$-Ga$_2$O$_3$ | LPCVD: Ga pellets and O$_2$; 780−950 °C | A maximum growth rate of 1.3 μm h$^{-1}$ was obtained at 850 °C, while a RMS surface roughness about 7 nm was obtained at 950 °C. | 65 |
| (F) $\beta$-Ga$_2$O$_3$ | Sn-doped (001) $\beta$-Ga$_2$O$_3$ | HVPE: GaCl and O$_2$; 800−1050 °C; 0.5 mBar for GaCl and 2.5 mBar for O$_2$ | A growth rate approximately 5 μm h$^{-1}$ was obtained at 900 °C and above. The thick layers of $\beta$-Ga$_2$O$_3$ grown at 1000 °C were smoother at the surface and had higher crystalline perfection than those grown at 800 °C. | 66 |
| (G) $\beta$-Ga$_2$O$_3$ | (001) $\beta$-Ga$_2$O$_3$ | PA-MBE: evaporated Ga and O$_2$ plasma; 800 or 900 °C; Ga beam equivalent pressure (BEP) 1.1 $\times$ 10$^{-7}$ or 2.4 $\times$ 10$^{-7}$ Torr | Ga BEP = 1.5 $\times$ 10$^{-7}$ mBar and 800 °C was the optimal growth condition. A RMS surface roughness of ~0.5 nm was achieved. The grown films were easily cleaved at the (100) and (001) planes. The easy cleavability of (100) planes facilitates the step-flow growth and terrace formation. | 35 |
| (H) $\beta$-Ga$_2$O$_3$ | (001) $\beta$-Ga$_2$O$_3$ | PA-MBE: evaporated Ga and O$_2$ plasma; 700−800 °C; Ga beam equivalent pressure (BEP) 1.7 $\times$ 10$^{-8}$ or 9.5 $\times$ 10$^{-8}$ Torr | The growth rate increased with increasing Ga BEP, reaching a plateau of 56 nm h$^{-1}$, and then decreased at higher Ga BEP. The growth rate decreased with the substrate temperature increasing from 750 to 800 °C. The growth rate became negative (i.e., etching) when only Ga flux was supplied. | 79 |

$^a$Characteristics of the grown crystals are summarized. TMGa represents trimethylgallium, TEGa triethylgallium, TESn tetraethyltin, and TEOS tetraethylorthosilicate.
Table 3. Heteroepitaxy of $\beta$-Ga$_2$O$_3$, $\varepsilon$-Ga$_2$O$_3$, and $\alpha$-Ga$_2$O$_3$ Layers on c-Plane and a-Plane Sapphire, 6H-SiC, c-Plane GaN, and c-Plane AlN/SiC Substrates, by Various Epitaxy Techniques, Including MOCVD, PA-MBE, HVPE, and Mist-CVD

| Epitaxial Layers | Substrates | Conditions | Crystal Characteristics | ref |
|-----------------|------------|------------|-------------------------|-----|
| (A) $\beta$-Ga$_2$O$_3$ | a- and c-plane sapphire | MOCVD: TMGa and $O_2$, 600–800 °C; 66 mBar | The Ga$_2$O$_3$ films grown on c-plane sapphire substrates were (021)-oriented, while the Ga$_2$O$_3$ films grown on a-plane substrates were less oriented and contained $\alpha$-phase. The film density (5.6 g cm$^{-3}$) was lower than the theoretical value (6.4 g cm$^{-3}$), indicating the presence of gallium or oxygen vacancies. | 67 |
| (B) Sn-doped $\beta$-Ga$_2$O$_3$ | c-plane sapphire | MOCVD: TMGa, $H_2$O and TESn, 775–850 °C; 5–50 mBar | The Ga$_2$O$_3$ films grown on c-plane sapphire substrates were (021)-oriented with the Sn-doping concentration $10^{17}$–$10^{18}$ cm$^{-3}$. The growth condition 850 °C and 50 mBar led to better crystal quality than 800 °C and 5 mBar. Ga vacancy-related defects and carbon-related complexes act as acceptors. | 68 |
| (C) Si-doped $\beta$-Ga$_2$O$_3$ | c-plane sapphire | MOCVD: TMGa, $H_2$O and TEOS, 800 °C; 5 and 10 mBar | The Ga$_2$O$_3$ films grown on c-plane sapphire substrates were (−201)-oriented. The Si-doping concentration in the range $10^{17}$–$10^{18}$ cm$^{-3}$ did not degrade the crystal quality. | 8 |
| (D) $\beta$-Ga$_2$O$_3$ | c-plane sapphire | MOCVD: TMGa and $H_2$O, 800 °C; 5–50 mBar | A 3-ML-thick layer of $\alpha$-Ga$_2$O$_3$ was observed at the interface between the $\beta$-Ga$_2$O$_3$ layer and c-plane sapphire substrate. The $\beta$-Ga$_2$O$_3$ layer was composed of rotational domains due to symmetry mismatch between the monoclinic $\beta$-Ga$_2$O$_3$ and trigonal $\alpha$-Ga$_2$O$_3$. | 69 |
| (E) $\varepsilon$-Ga$_2$O$_3$ | c-plane Sapphire | MOCVD: TMGa and $H_2$O, 550, 650, and 715 °C; 100 mBar | The Ga$_2$O$_3$ films grown on the c-plane sapphire substrates were polycrystalline. If the growth temperature was above 535 °C, pure (021)-oriented $\beta$-Ga$_2$O$_3$ was obtained. If the growth temperature was 505 °C, a mixture of $\beta$-Ga$_2$O$_3$ and $\varepsilon$-Ga$_2$O$_3$ was obtained. | 70 |
| (F) $\beta$-Ga$_2$O$_3$ | c-plane Sapphire | MOCVD: TEGa and $O_2$, 450–570 °C; 12.1 mBar | If the growth temperature was 550 °C, the deposited films were amorphous. If the growth temperature was increased to 715 °C, (−201)-oriented $\beta$-Ga$_2$O$_3$ with poor crystalline quality was obtained. Only when the growth temperature was controlled at 650 °C was high quality $\varepsilon$-Ga$_2$O$_3$ obtained. | 71 |
| (G) $\varepsilon$-Ga$_2$O$_3$ | 6H-SiC | MOCVD: TEGa and $O_2$, 500 °C; 35 mBar | The Ga$_2$O$_3$ films grown on 6H-SiC substrates were $\varepsilon$-phase pure and in high crystal quality. If annealed at 850 °C, transition to (021)-oriented $\beta$-Ga$_2$O$_3$ started to occur. If annealed at 900 °C, all $\varepsilon$-Ga$_2$O$_3$ was converted to $\beta$-Ga$_2$O$_3$. | 72 |
| (H) $\beta$-Ga$_2$O$_3$ | c-plane sapphire | PA-MBE: evaporated Ga and $O_2$ plasma; 600–750 °C; Ga beam equivalent pressure (BEP) $5 \times 10^{-9}$ to $2 \times 10^{-7}$ Torr | The Ga$_2$O$_3$ films grown on c-plane sapphire substrates were (−201)-oriented and $\beta$-phase pure. With the low Ga flux (high growth rate), three-dimensional columnar structures were observed. With the high Ga flux (low growth rate), a typical terrace surface morphology was obtained. | 73 |
| (I) $\beta$-Ga$_2$O$_3$ | a- and c-plane sapphire | PA-MBE: evaporated Ga and $O_2$ plasma; 600–800 °C; $5 \times 10^{-4}$ Torr | The Ga$_2$O$_3$ films grown on c-plane and a-plane substrates were both (021)-oriented, with no $\alpha$-phase diffraction peak observed. Six types of $\beta$-Ga$_2$O$_3$ grains on the c-plane substrate, with the orientation rotated every 60° from the Al$_2$O$_3$ [110] direction, were observed. | 74 |
| (J) $\varepsilon$-Ga$_2$O$_3$ | c-plane GaN, c-plane AlN/SiC | HVPE: Ga, HCl and $O_2$, 550 °C; 2.5 mBar for HCl and 10 mBar for $O_2$ | A growth rate of approximately 20 nm h$^{-1}$ was achieved for $\varepsilon$-Ga$_2$O$_3$ on c-plane AlN/SiC substrates. The as-grown films on GaN and AlN/SiC substrates were (0001)-oriented $\varepsilon$-phase pure. The $\varepsilon$-Ga$_2$O$_3$ film was thermally stable up to 700 °C and exhibited an optical bandgap equal to 4.9 eV. | 75 |
| (K) $\alpha$-Ga$_2$O$_3$ | c-plane sapphire | Mist-CVD: Gallium acetylacetonate Ga(C$_5$H$_7$O$_2$)$_3$ in deionized water with slight addition of HCl, 470 °C | The as-grown $\alpha$-Ga$_2$O$_3$ was phase pure and remained so after annealing at 550 °C. However, if the annealing temperature increased to 600 °C, $\alpha$- to $\beta$-phase transition started to occur. The $\alpha$-phase completely disappeared at 700 °C. | 76 |

*Characteristics of the grown crystals are summarized. TMGa represents trimethylgallium; TEGa, triethylgallium; TESn, tetraethyltin; and TEOS, tetraethylorthosilicate.*
% N. Later, the pulling rate and die geometry of the EFG method were further optimized to improve the grown crystal quality and shape. It is worth mentioning that for the FZ, CZ, and EFG methods discussed above, the doping of the β-Ga2O3 crystals is usually accomplished by mixing the dopants, such as SnO2 and SiO2, with the starting materials, β-Ga2O3 powder, before the crystal growth process.

### DEPOSITION OF GALLIUM OXIDE

**Homoeptaxy by MOCVD.** Among various deposition methods, metal–organic chemical vapor deposition (MOCVD) has drawn much attention, because it is most suitable for large-scale production and has precise control of growth rate and doping. For the homoeptaxy of β-Ga2O3 by MOCVD, (100)- and (010)-oriented wafers are generally used. In 2014, Wagner et al. demonstrated homoeptaxy of β-Ga2O3 on a (100) substrate by using trimethylgallium (TMGa) as the gallium precursor and oxygen gas or water as the oxygen precursor (Table 2A). When using pure oxygen gas, the formation energy of oxygen vacancies is greatly increased, and the byproduct Ga2O3(CO)3 may act as deposition masks, resulting in Ga2O3 nanocrystals instead of coherent films. In contrast, when using water as the oxygen source, since the oxygen part is fully consumed by the reaction with gallium, the formation of carbon-related byproducts is prevented and the remaining hydrogen part may form Ga–H passivation, which can reduce the surface state density and promote the layer-by-layer growth. In 2016, Baldini et al. demonstrated homoeptaxy of n-type β-Ga2O3 on a (100) substrate by using triethylgallium (TEGa), oxygen gas, and tetraethyltin (TETSn) as the precursors (Table 2B). Despite the ultraflat surface with the root-mean-square (RMS) surface roughness of only ~0.6 nm, the transmission electron microscopy (TEM) analysis reveals stacking faults in the form of twin lamellae, which may act as the compensation and scattering centers of electrons, limiting the electron mobility. To resolve this issue, it was found that using substrates with relatively large miscut angles can effectively avoid the formation of twin lamellae (Table 2C). For example, the β-Ga2O3 layer homoeptaxially grown on a 0.1° miscut (100) substrate has an estimated twin lamella density as high as 1 × 1017 cm⁻³. However, the growth rate of Ga2O3 films is sensitive to the substrate miscut angle. For example, the 0.1° miscut (100) β-Ga2O3 substrate exhibits a wide terrace, and the as-grown epitaxial layer has elongated islands on the surface and contains a high density of twin lamellae. In contrast, the 4° miscut substrate yields a narrow terrace, few two-dimensional islands, and sporadic twin lamellae. Finally, quantitative calculations using Read’s model of charged dislocations confirm the reduction of electron mobility caused by the twin lamellae.

In general, the β-Ga2O3 films grown on the (010) β-Ga2O3 substrates have higher crystalline perfection than on the (100) β-Ga2O3 substrates. Besides, the maximum electron mobility achieved by the (100) β-Ga2O3 films so far is only ~40 cm² V⁻¹ s⁻¹, while the electron mobility of the (010) β-Ga2O3 films grown by molecular-beam epitaxy (MBE) can be >100 cm² V⁻¹ s⁻¹. Furthermore, the heat transfer along the [010] direction (21 W m⁻¹ K⁻¹) is more efficient than along the [100] direction (13 W m⁻¹ K⁻¹), making the (010) β-Ga2O3 films more advantageous for the power device application due to the faster heat dissipation. Therefore, in this paragraph we focus on the homoeptaxial growth of β-Ga2O3 on the (010) substrates by MOCVD. In 2017, Baldini et al. demonstrated homoeptaxy of Si- and Sn-doped β-Ga2O3 on Fe-doped (010) substrates (Table 2D). The as-grown layers are ultraflat with the RMS surface roughness only ~0.6 nm and are exempt of dislocations or planar defects. Furthermore, due to the very high crystalline perfection, there is no distinguishable interface between the epitaxial layer and the (010) substrate. Compared to Sn, Si is the better dopant because it has higher doping efficiency and no memory effect. The maximum electron mobility equal to ~130 cm² V⁻¹ s⁻¹ can be achieved with the carrier concentration equal to 1 × 10¹⁷ cm⁻³ regardless of the dopant type.

**Homoeptaxy by Other Techniques.** In 2016, Rafique et al. demonstrated homoeptaxy of (010) β-Ga2O3 films by low pressure CVD (LPCVD) and investigated the influence of growth temperature on the crystal quality (Table 2E). With sufficiently high growth temperatures, the deposited crystals achieve high crystalline perfection, i.e., undifferentiable interface between the epitaxial layer and substrate, and the surface morphology exhibits a terrace-like structure, which basically reproduces the substrate’s terrace morphology. The RMS surface roughness is ~40 nm with the growth temperature equal to 780 °C but only ~7 nm if the growth temperature increases to 950 °C. In 2015, Murakami et al. demonstrated that thick layers of β-Ga2O3 can be homoeptaxially grown on (001)-oriented Sn-doped β-Ga2O3 substrates by halide vapor phase epitaxy (HVPE) with gaseous GaCl and O₂ as the precursors, and the influence of growth temperature on the crystal quality was investigated (Table 2F). Compared to those grown at 800 °C, the β-Ga2O3 layers grown at 1000 °C are much smoother at the surface and have higher crystalline perfection, as revealed by the narrower X-ray rocking curves. In 2008, Oshima et al. demonstrated homoeptaxy of β-Ga2O3 layers on (100) β-Ga2O3 substrates by plasma-assisted MBE (PA-MBE) using evaporated Ga and O₂ plasma (Table 2G). The deposited films and the substrate exhibit the same β-Ga2O3 (020) X-ray diffraction (XRD) peaks, and the film surface morphology features a duplicate of the substrate terrace with the RMS surface roughness only ~0.5 nm. The grown films can be easily cleaved at the (100) and (001) planes. The excellent cleavability of the (100) planes facilitates the stepped-flow growth and terrace formation. In 2018, Oshima et al. studied how the Ga-flux and the substrate temperature affect the PA-MBE growth rate (Table 2H). The growth rate of β-Ga2O3 increases with higher Ga-flux, reaching a plateau of 56 nm h⁻¹. Further increase of Ga-flux decreases the growth rate. The growth rate also declines with the substrate temperature elevating from 750 to 800 °C. Notably, the growth rate becomes negative, i.e., net etching, when only Ga-flux is supplied.

**Heteroeptaxy by MOCVD.** For the heteroeptaxy of β-Ga2O3 by MOCVD, c-plane sapphire substrates are most commonly used. The sapphire substrates are relatively cheap and able to provide electrical isolation for the power FETs. In 2016, Tadjer et al. compared the a-plane and c-plane sapphire substrates for the heteroeptaxy of β-Ga2O3 (Table 3A). Based on the XRD analysis, the β-Ga2O3 layer grown on the c-plane substrate reveals clear β-phase diffraction peaks attributed to the (−201) plane, while the β-Ga2O3 layer...
grown on the α-plane substrate exhibits an obvious α-phase diffraction peak along with some other β-phase diffraction peaks, suggesting a less crystalline and less oriented crystal structure.65 Besides, the deposited film density (5.6 g cm⁻³) is significantly lower than the theoretical value (6.4 g cm⁻³), indicating the presence of gallium or oxygen vacancies.66

Another study of heteroepitaxy of Sn-doped β-Ga₂O₃ on c-plane sapphire substrates also suggested that the grown films are clearly monoclinic and (−201)-oriented with the Sn doping concentration 10⁷−10¹⁰ cm⁻³ (Table 3B).67 However, the Ga vacancy-related defects and the residual carbon complexes from the TMGa precursors may act as acceptors which compensate the Sn donors.68 Similarly, the Si-doped β-Ga₂O₃ epitaxial layers on c-plane sapphire substrates were also (−201)-oriented, and no deterioration of crystal quality was observed in the doping range 10⁷−10¹⁸ cm⁻³ (Table 3C).65

However, when the Si doping concentration is up to 5 × 10¹⁸ cm⁻³, amorphization of the films occurs and only very low conductivity is obtained.8 On the other hand, different grains or domains have been observed in the heteroepitaxially grown β-Ga₂O₃. In 2015, Schewski et al. found a 3-ML-thick layer of crystalline α-Ga₂O₃ sandwiched between the β-Ga₂O₃ epitaxial layer and c-plane sapphire substrate (Table 3D).69 Besides, the β-Ga₂O₃ layer on top of the α-Ga₂O₃ layer is composed of rotational domains, which can be attributed to the symmetry mismatch between the monoclinic β-Ga₂O₃ and trigonal α-Ga₂O₃.69 Furthermore, despite the pure β-phase XRD pattern shown, the TEM investigation reveals that the β-Ga₂O₃ epitaxial layer actually contains in-plane grains rotated 120° to each other.70 Moreover, the actual lattice constants a and c are estimated to be smaller and the lattice constant b and angle β are estimated to be larger, compared to the standard values of single-crystal β-Ga₂O₃.70 In summary, while the (−201)-oriented β-Ga₂O₃ can indeed grow on the c-plane sapphire substrate epitaxially, the grown films can hardly be single-crystal due to the symmetry mismatch between the monoclinic β-Ga₂O₃ and hexagonal Al₂O₃.

Compared to the monoclinic β-Ga₂O₃, the crystallographic symmetry of orthorhombic ε-Ga₂O₃ is better matched to the sapphire substrates.71 Besides, the ε-Ga₂O₃ also possesses the wide bandgap nature of the β-Ga₂O₃ and can be grown in a relatively mild condition. In 2016, Boschi et al. found that the growth temperature plays a critical role in deciding the crystal form (Table 3E).72 For example, the films deposited at 550 °C are basically amorphous. If the growth temperature elevates to 715 °C, only weak and broad XRD peaks related to the (−201)-oriented β-Ga₂O₃ are observed, as the crystalline β-Ga₂O₃ are usually obtained at higher temperatures. However, when the growth temperature is controlled at 650 °C, intense and narrow XRD peaks corresponding to the ε-Ga₂O₃ are shown.72 Furthermore, although the SEM images showed hexagonal nucleation islands at the film surface and the large-area electron diffraction patterns suggested pseudohexagonal symmetry with the P6₃/mmc space group,72 the actual structure of ε-Ga₂O₃ is composed of ordered 120°-rotational twin domains, each of which has diameters of 5 to 10 nm and orthorhombic symmetry with the Pna2₁ space group.72 The high-resolution cross-section TEM image indicates that the ε-Ga₂O₃ film grown at 650 °C possesses a columnar structure and ε-Ga₂O₃ epitaxial islands are present at the interface between the ε-Ga₂O₃ film and c-plane sapphire substrate.72 Based on the photon energy for the onset of photocconductivity and band-to-band absorption, the optical bandgap of the ε-Ga₂O₃ films is between 4.6 and 4.7 eV, which is close to that of β-Ga₂O₃, and the cathodoluminescence spectroscopy indicates a group of deep donors located at ~0.7 eV below the conduction band and three defect states below the midgap.74 Lastly, the thermal stability of the ε-Ga₂O₃ films grown on c-plane sapphire substrates was investigated via differential scanning calorimetry (DSC), TEM, and XRD (Table 3F).75,76 After heteroepitaxy at 650 °C, the film was placed inside a tubular furnace for the heat treatment. The film can withstand prolonged heat treatment up to 700 °C. However, if the annealing temperature is higher than 900 °C, a complete transition to the β-phase occurs.73 Similarly thermally induced transition was observed for the ε-Ga₂O₃ films grown on 6H-SiC substrates by MOCVD (Table 3G).77 The as-grown films are ε-phase pure and in high crystal quality. However, the diffraction peaks corresponding to the (−201)-oriented β-Ga₂O₃ start to appear if the annealing temperature increases to 850 °C, and the ε-Ga₂O₃ is completely converted to β-Ga₂O₃ if annealed at 900 °C.77

**Heteroepitaxy by Other Techniques.** In 2010, Tsai et al. demonstrate that by using PA-MBE, phase pure, (−201)-oriented β-Ga₂O₃ films were successfully deposited on c-plane sapphire substrates (Table 3H).78 With the low gallium flux which leads to high growth rate, the as-grown film is composed of three-dimensional columnar structures. On the contrary, with the high gallium flux and thus low growth rate, a typical terrace surface morphology is obtained.78 The decreasing growth rate with increasing gallium flux is likely due to the formation and desorption of gallium suboxides and was also observed in another PA-MBE work (Table 2H).79 In 2012, Nakagomi et al. compared the (−201)-oriented β-Ga₂O₃ films heteroepitaxially grown on c-plane and a-plane sapphire substrates by PA-MBE (Table 3I).80 Both types of the sapphire substrates can lead to strong (−201)-oriented β-Ga₂O₃ XRD patterns.80 In contrast, the β-Ga₂O₃ film grown on the a-plane sapphire substrate by MOCVD includes certain α-Ga₂O₃.80 Moreover, the β-Ga₂O₃ film on the c-plane sapphire substrate contains six types of grains, with the orientation rotated every 60° from the Al₂O₃ [110] direction.80 Similar results have also been observed for other β-Ga₂O₃ films grown by MOCVD.68,69 In 2015, Oshima et al. demonstrated heteroepitaxy of ε-Ga₂O₃ and β-Ga₂O₃ on various substrates, including sapphire, GaN, and AlN/SiC, by using HVPE (Table 3J).79,81 Compared to MOCVD, the major advantage of HVPE is the relatively high growth rate (approximately 20 μm h⁻¹ for ε-Ga₂O₃ grown on c-plane AlN/SiC substrates and 250 μm h⁻¹ for β-Ga₂O₃ quasi-epitaxially grown on off-angled c-plane sapphire substrates), and the crystal qualities of the as-grown films are comparable to those grown by MOCVD.29,81 In 2013, Lee et al. demonstrated that mist-CVD can be a low-energy-consumption alternative to grow α-Ga₂O₃ films on c-plane sapphire substrates (Table 3K).77,82 Compared to the monoclinic β-Ga₂O₃, the corundum α-Ga₂O₃ is better matched to the hexagonal sapphire substrates, resulting in epitaxial layers with fewer defects. After growth at 470 °C with optimal flow rates, the α-Ga₂O₃ films were annealed at different temperatures step-by-step. The α-phase can be maintained for the annealing temperature up to 550 °C but gradually converted to β-phase if the annealing temperature higher than 600 °C.82

### DEPLETION-MODE β-GA₂O₃ FETS

Given the difficulty of p-type doping in β-Ga₂O₃, recent device performance milestones have been mainly achieved by the...
depletion-mode FETs based on epitaxial layers grown on single-crystal $\beta$-Ga$_2$O$_3$ substrates. For the power switching application, the essential parameter for evaluating the device performance is the power figure of merit (PFOM) = $V_{br}^2 / R_{on,sp}$, where $V_{br}$ is the on-state breakdown voltage and $R_{on,sp}$ is the on-resistance normalized by the device area. To exploit the full potential of $\beta$-Ga$_2$O$_3$ as predicted by the BFOM, many device-level approaches have been developed to increase $V_{br}$ while decreasing $R_{on,sp}$, as discussed below.

**Gate-Connected Field-Plates.** For metal-oxide-semiconductor FETs (MOSFETs), the gate-connected field-plate is a useful design to manage the electric field distribution between the gate and drain, so that the peak electric field in the channel region will not exceed the breakdown electric field of $\beta$-Ga$_2$O$_3$ (8 MV cm$^{-1}$). In 2016, Wong et al. demonstrated depletion-mode $\beta$-Ga$_2$O$_3$ MOSFETs with gate-connected field-plates for the first time (Figure 3A). An area-selective Si-ion implantation technique was employed to fabricate the channel and the source/drain (S/D) regions on an UID epitaxial layer grown on a Fe-doped (010) $\beta$-Ga$_2$O$_3$ substrate by ozone assisted (OA)-MBE. By using Silvaco two-dimensional device simulations, the most favorable field-plate geometry, which balances the peak electric fields among the drain, gate, and field-plate, can be obtained. The $\beta$-Ga$_2$O$_3$ MOSFET with the optimized field-plate design can achieve $V_{br} = 755$ V, $R_{on,sp} \approx 55$ mΩ cm$^2$, and PFOM $\sim 10.4$ MW cm$^{-2}$ (Table 4B). In comparison, without the gate-connected field-plate, a similar depletion-mode $\beta$-Ga$_2$O$_3$ MOSFET can only achieve $V_{br} = 370$ V, $R_{on,sp} \sim 69$ mΩ cm$^2$, and PFOM $\sim 2$ MW cm$^{-2}$ (Table 4A). Another major difference between the two devices is the incorporation of an UID layer below the channel region. The highly resistive UID buffer layer can protect the channel against charge compensation due to the outdiffusion of Fe deep acceptors from the Fe-doped (010) $\beta$-Ga$_2$O$_3$ substrate, while providing effective device isolation without the need of mesa etching.

**Ge-Doped Channels and Fluorinert Immersion.** In 2017, Moser et al. demonstrated two-finger depletion-mode $\beta$-Ga$_2$O$_3$ MOSFETs with the channel regions doped with Ge ($6.1 \times 10^{17}$ cm$^{-3}$) and mesa etching for device isolation. Compared to other $\beta$-Ga$_2$O$_3$ MOSFETs having similar device structures but with the channel regions doped with Sn ($1.7 \times 10^{19}$ cm$^{-3}$), the two devices can achieve comparable PFOMs of $\sim$11 MW cm$^{-2}$, but the device with Ge doping exhibits significantly higher channel electron mobility ($111$ cm$^2$ V$^{-1}$ s$^{-1}$) than the device with Sn doping ($19.7$ cm$^2$ V$^{-1}$ s$^{-1}$) (Table 4C and D), suggesting Ge might be a better dopant kind than the commonly used Si or Sn. In 2018, Zheng et al. demonstrated depletion-mode $\beta$-Ga$_2$O$_3$ MOSFETs with not only gate-connected field-plates but also Fluorinert FC-770 immersion. It was reported that the breakdown through air, which has the dielectric strength of $\sim$3 kV mm$^{-1}$, might be the primary premature breakdown mechanism limiting the $V_{br}$ in $\beta$-Ga$_2$O$_3$ MOSFETs with relatively low $V_{br}$ of 300–400 V. Therefore, by replacing air with Fluorinert FC-770, which has the dielectric strength of $\sim$15 kV mm$^{-1}$, the $V_{br}$ of the gate-field-plated MOSFETs can be significantly improved from 440 V in air to 1850 V in Fluorinert. However, due to the relatively long channel length (28 μm), the $R_{on,sp}$ of the device is $\sim$2000 mΩ cm$^2$, resulting in a relatively low PFOM of $\sim$1.7 MW cm$^{-2}$ (Table 4F).

**Source-Connected Field-Plates.** In 2019, Lv et al. demonstrated depletion-mode $\beta$-Ga$_2$O$_3$ MOSFETs with source-connected field-plates as an improvement to gate-connected field-plates (Figure 3B). The Si-doped channel layer and the UID buffer layer were homoepitaxially grown on...
Table 4. Representative Depletion-Mode $\beta$-Ga$_2$O$_3$ FETs with Various Device Structures and Fabricated by Different Deposition Techniques$^{a}$

| Features | Substrates/Gates Dielectric | Epitaxial Layers | Donor Concentrations | $V_{th}$ (V) | $R_{on}$ (m$\Omega$ cm$^2$) | $V_{th}^2/R_{on}$ (MW cm$^{-2}$) | $I_{sd,sat}$ (mA mm$^{-1}$) | $I_m/I_{off}$ | ref |
|----------|-----------------------------|-----------------|----------------------|-------------|-----------------|-----------------|-----------------|-------------|-----|
| (A)      | • Circular MOSFET           | Fe-doped (010) $\beta$-Ga$_2$O$_3$/20 nm Al$_2$O$_3$ | MBE | Channel: Sn, $7 \times 10^{17}$ cm$^{-3}$ | $370$ ($V_{GS} = -20$ V) | $\sim 69$ ($V_{GS} = 4$ V) | $\sim 2.0$ | $39$ ($V_{GS} = 4$ V) | $>10^{10}$ | 2013$^{53}$ |
|          | • Annealed Ti/Au for ohmic contacts | | | | | | | | |
|          | • Si implantation for S/D | | | | | | | | |
|          | • Lateral MOSFET Gatefield-plate | Fe-doped (010) $\beta$-Ga$_2$O$_3$/20 nm Al$_2$O$_3$ | OA-MBE | Channel: Si, $3 \times 10^{17}$ cm$^{-3}$ | $755$ ($V_{GS} = -55$ V) | $\sim 55$ ($V_{GS} = 4$ V) | $\sim 10.4$ | $78$ ($V_{GS} = 4$ V) | $>10^{9}$ | 2016$^{94}$ |
|          | • Si implantation for channel and S/D | | | | | | | | |
|          | • UID layer for device isolation | | | | | | | | |
| (B)      | • Two-finger MOSFET         | Mg-doped (100) $\beta$-Ga$_2$O$_3$/20 nm Al$_2$O$_3$ | MOCVD | Channel: Sn, $1.7 \times 10^{18}$ cm$^{-3}$ | $230$ ($V_{GS} = 0$ V) | $4.9$ ($V_{GS} = 0$ V) | $11$ | $\sim 60$ ($V_{GS} = 0$ V) | $<10^7$ | 2016$^{96}$ |
|          | • Channel $\mu_h$ = 197 cm$^2$ V$^{-1}$ s$^{-1}$ (by Hall effect) | | | | | | | | |
|          | • Mesa etching for device isolation | | | | | | | | |
| (C)      | • Lateral MOSFET Gatefield-plate | Fe-doped (010) $\beta$-Ga$_2$O$_3$/20 nm SiO$_2$ | OA-MBE | Channel: Sn, $1 \times 10^{16}$ cm$^{-3}$ | $382$ ($V_{GS} = -25$ V) | $\sim 171$ ($V_{GS} = 14$ V) | $0.9$ | $35$ ($V_{GS} = 14$ V) | $<10^6$ | 2017$^{101}$ |
|          | • SOG doping for S/D | | | | | | | | |
|          | • Specific contact resistance = $2.1 \times 10^{-5}$ $\Omega$ cm$^{-2}$ | | | | | | | | |
|          | • UID layer for device isolation | | | | | | | | |
| (D)      | • Lateral MOSFET Gatefield-plate | Fe-doped (010) $\beta$-Ga$_2$O$_3$/20 nm SiO$_2$ | MBE | Channel: Ge, $6.1 \times 10^{17}$ cm$^{-3}$ | $479$ ($V_{GS} = -20$ V) | $\sim 20$ ($V_{GS} = 0$ V) | $\sim 11.5$ | $80$ ($V_{GS} = 0$ V) | $>10^{8}$ | 2017$^{97}$ |
|          | • Channel $\mu_h$ = $111$ cm$^2$ V$^{-1}$ s$^{-1}$ (by Hall effect) | | | | | | | | |
|          | • Mesa etching for device isolation | | | | | | | | |
| (E)      | • Lateral MOSFET Gatefield-plate | Fe-doped (010) $\beta$-Ga$_2$O$_3$/20 nm SiO$_2$ | OA-MBE | Channel: Sn, $2 \times 10^{17}$ cm$^{-3}$ | $1850$ in Fluorinert | $460$ in air ($V_{GS} = -32$ V) | $\sim 2000$ in Fluorinert ($V_{GS} = 12$ V) | $1.7$ | $1.5$ ($V_{GS} = 12$ V) | $<10^9$ | 2018$^{99}$ |
|          | • Source field-plate | | | | | | | | |
|          | • Gatefield-plate | | | | | | | | |
|          | • SOG doping for S/D | | | | | | | | |
|          | • Fluorinert Immersion | | | | | | | | |
|          | • UID layer for device isolation | | | | | | | | |
| (F)      | • Lateral MOSFET Gatefield-plate | Fe-doped (010) $\beta$-Ga$_2$O$_3$/20 nm SiO$_2$ | MBE | Channel: Sn, $2 \times 10^{17}$ cm$^{-3}$ | $1850$ in Fluorinert | $460$ in air ($V_{GS} = -32$ V) | $\sim 2000$ in Fluorinert ($V_{GS} = 12$ V) | $1.7$ | $1.5$ ($V_{GS} = 12$ V) | $<10^9$ | 2018$^{99}$ |
|          | • Source field-plate | | | | | | | | |
|          | • Gatefield-plate | | | | | | | | |
|          | • SOG doping for S/D | | | | | | | | |
|          | • Fluorinert Immersion | | | | | | | | |
|          | • UID layer for device isolation | | | | | | | | |
| (G)      | • Lateral MOSFET Gatefield-plate | Fe-doped (010) $\beta$-Ga$_2$O$_3$/25 nm Al$_2$O$_3$ | MOCVD | Channel: Si, $8 \times 10^{17}$ cm$^{-3}$ | $480$ with $L_{SD} = 11 \mu m$ | $4.58$ with $L_{SD} = 11 \mu m$ | $50.4$ with $L_{SD} = 11 \mu m$ | $267$ with $L_{SD} = 11 \mu m$ | $<10^9$ | 2019$^{92}$ |
|          | • Source field-plate | | | | | | | | |
|          | • Gatefield-plate | | | | | | | | |
|          | • Si implantation for S/D | | | | | | | | |
|          | • Si$_n$ internal passivation | | | | | | | | |
|          | • Mesa etching for device isolation | | | | | | | | |
| (H)      | • Lateral MOSFET Gatefield-plate | Fe-doped (010) $\beta$-Ga$_2$O$_3$/20 nm Al$_2$O$_3$ | OA-MBE | Channel: Sn, $1.5 \times 10^{18}$ cm$^{-3}$ | $2321$ in Fluorinert ($V_{GS} = -10$ V) | $959$ ($V_{GS} = 1$ V) | $5.6$ | $\sim 6.5$ ($V_{GS} = 1$ V) | $<10^8$ | 2019$^{93}$ |
Table 4. continued

| Features | Substrates/Gates Dielectric | Epitaxial Layers | Donor Concentrations | $V_{br}$ (V) | $R_{on,sp}$ (mΩ cm$^2$) | $V_{br}^2/R_{on,sp}$ (MW cm$^{-2}$) | $I_{ds,sat}$ (mA mm$^{-1}$) | $I_{on}/I_{off}$ ratio | ref |
|----------|-----------------------------|------------------|----------------------|--------------|-----------------|-------------------------------|-----------------|----------------------|-----|
| (I)      | • Thin and heavily doped channel | MOCVD | Channel: $2.3 \times 10^{17}$ cm$^{-3}$ (charge carrier) | 1830 ($V_{GS} = -20$ V) | 21.6 ($V_{GS} = 10$ V) | 155 | 120 ($V_{GS} = 10$ V) | $>10^{10}$ | 2019$^{94}$ |
|          | • Mesa etching for device isolation | Mg-doped (100) $\beta$-Ga$_2$O$_3$ with 6° miscut/25 nm Al$_2$O$_3$ |  |  |  |  |  |  |  |
|          | • 0.7-μm-long and recessed gate | 0.20 μm Si-doped channel |  | 1 |  |  |  |  |  |
|          | • $\beta$-Ga$_2$O$_3$ epitaxial layer on sapphire substrate | Channel: $2.3 \times 10^{16}$ cm$^{-3}$ at 5–10 nm deep from the surface |  |  |  |  |  |  |  |
|          | • SiN$_x$ internal passivation | HVPE | Channel: F, $2.3 \times 10^{16}$ cm$^{-3}$ at 5–10 nm deep from the surface |  |  |  |  |  |  |
| (J)      | • Lateral MOSFET | c-plane Sapphire/40 nm Al$_2$O$_3$ | Channel: F, $2.3 \times 10^{16}$ cm$^{-3}$ at 5–10 nm deep from the surface |  |  |  |  |  |  |
|          | • $\beta$-Ga$_2$O$_3$ epitaxial layer on sapphire substrate | 0.15 μm Si-doped channel |  |  |  |  |  |  |  |
|          | • CF$_4$ plasma treatment for n-type doping | 0.15 μm Si-doped channel |  |  |  |  |  |  |  |
| (K)      | • Modulation-doped heterostructured FET | Fe-doped (010) $\beta$-Ga$_2$O$_3$/Pt/Ag Schottky gate contact | Channel (2DEG): $1.85 \times 10^{12}$ cm$^{-2}$ | 1365 ($V_{GS} = -5$ V) | 1201 ($V_{GS} = 0$ V) | 15.5 | 41 ($V_{GS} = 2$ V) | $>10^7$ | 2019$^{97}$ |
|          | • Gate field plate | $\beta$ (Al$_{0.22}$Ga$_{0.78}$)$_2$O$_3$ 5 nm spacer and 25 nm barrier |  |  |  |  |  |  |  |
|          | • Patterned regrowth of n$^+$ $\beta$-Ga$_2$O$_3$ for S/D | $\beta$ (Al$_{0.22}$Ga$_{0.78}$)$_2$O$_3$ 5 nm spacer and 25 nm barrier |  |  |  |  |  |  |  |
|          | • Patterned regrowth of n$^+$ $\beta$-Ga$_2$O$_3$ for S/D | 0.10 μm UID buffer layer |  |  |  |  |  |  |  |
|          | • SiN$_x$ internal passivation | 0.10 μm UID buffer layer |  |  |  |  |  |  |  |
|          | • Mesa etching for device isolation | 0.10 μm UID buffer layer |  |  |  |  |  |  |  |

*For each power device, the parameters for evaluating the power switching performance are summarized, including the three-terminal off-state breakdown voltage ($V_{br}$), on-resistance normalized by the device area ($R_{on,sp}$), power figure of merit (PFOM = $V_{br}^2/R_{on,sp}$), maximum saturation drain current ($I_{ds,sat}$) and $I_{on}/I_{off}$ ratio.*
a Fe-doped (010) β-Ga₂O₃ substrate by MOCVD, and then the S/D regions were formed by area-selective Si-implantation. The MOSFET with the optimized field-plate design and the channel length (L_SD) = 11 μm can achieve V_P = 480 V, R_on,sp = 4.58 mΩ cm², and PFOM = 50.4 MW cm⁻². When the L_SD was extended to 18 μm, although the V_P increased to 680 V, the R_on,sp increased to 11.7 mΩ cm² accordingly, making the PFOM slightly decreased to 39.5 MW cm⁻² (Table 4G). In 2019, Mun et al. further improved the source-connected field-plate design by adopting a thin and heavily doped channel. Besides, the deposition conditions for the Al₂O₃ gate dielectric and SiO₂ internal passivation were optimized, leading to record high V_P. The channel of the β-Ga₂O₃ MOSFET is composed a 150-nm-thick Si-doped (1.5 × 10²⁷ cm⁻³) β-Ga₂O₃ epitaxial layer grown on a Fe-doped (010) β-Ga₂O₃ substrate by MBE. Since the channel doping concentration is high enough, there is no need for the area-selective Si-implantation at the S/D regions. Such a design has also been seen in other β-Ga₂O₃ MOSFETs. The MOSFET with the optimized field-plate design (L_GF = 3 μm and L_SD = 25 μm) can achieve V_P = 2231 V in Fluorinert, but relatively large R_on,sp = 959 mΩ cm² and thus relatively low PFOM = 5.6 MW cm⁻² (Table 4H).

Recessed Gates and Heterostructure FETs. To further decrease R_on,sp while maintaining high V_P in 2019, Tetzner et al. demonstrated depletion-mode β-Ga₂O₃ MOSFETs featuring sub-μm gate length and gate recess for low R_on,sp and SiN internal passivation for high V_P (Figure 3C). The channel region is composed of a 200-nm-thick Si-doped β-Ga₂O₃ layer homoepitaxially grown on an Mg-doped (100) β-Ga₂O₃ substrate with a 6° miscut toward the [001] direction. The miscut angle was for avoiding the formation of twin lamellae. The 100-nm-deep recessed gate was lithographically structured by using BCl₃ reactive ion etching (RIE), followed by atomic layer deposition (ALD) of 25-nm-thick Al₂O₃ gate dielectric. The device isolation was carried out by a multiple energy N⁺-ion implantation. The β-Ga₂O₃ MOSFET with the L_SD = 10 μm can achieve V_P = 1830 V, R_on,sp = 21.6 mΩ cm², and record high PFOM = 155 MW cm⁻² (Table 4I). Despite the high breakdown electric field of β-Ga₂O₃ (8 MV cm⁻¹) which enables high V_P, most β-Ga₂O₃ MOSFETs suffer from large R_on,sp especially when the gate-drain distance needs to be long for reducing the peak electric field. Considering the relatively low intrinsic electron mobility of β-Ga₂O₃ (estimated 100–300 cm² V⁻¹ s⁻¹) compared to SiC and GaN (Table 1), the heterostructure FETs with two-dimensional electron gas (2DEG) channels can achieve high channel mobility due to the absence of impurity scattering.

In 2019, Joishi et al. demonstrated β-(Al₂₀₂·Ga₇·₈)O₃/Ga₂O₃ modulation-doped FETs with gate-connected field-plates and SiN passivation layers (Figure 3D). The device epitaxial layers comprise a 100 nm UID β-Ga₂O₃ buffer layer, a 5 nm β-(Al₂₀₂·Ga₇·₈)O₃ spacer, a delta sheet of Si dopants, and a 25 nm β-(Al₂₀₂·Ga₇·₈)O₃ barrier, all grown on a Fe-doped (010) β-Ga₂O₃ substrate by PA-MBE. The temperature dependent Hall measurements indicated that the charge density of the conducting channel, mainly composed of the 2DEG, is 3.4 × 10¹⁰ cm⁻² with the electron mobility equal to 101 cm² V⁻¹ s⁻¹, which is comparable to the electron mobility achieved by the Ge-doped β-Ga₂O₃ channels (111 cm² V⁻¹ s⁻¹). It is worth mentioning that similar β-(Al₂₀₂·Ga₇·₈)O₃/β-Ga₂O₃ modulation-doped heterostructure FETs with a delta sheet of Ge dopants has also been demonstrated. The field-plate design with SiN internal passivation is expected to yield higher V_P because the SiN exhibits a (dielectric constant, κ) × (dielectric strength, kV mm⁻¹) product of 75 MW cm⁻², which is higher than SiO₂ (39 MW cm⁻²) and Al₂O₃ (64.9 MW cm⁻²). The β-(Al₂₀₂·Ga₇·₈)O₃/Ga₂O₃ modulation-doped heterostructure FET with the L_SD = 16 μm can achieve V_P = 1365 V, R_on,sp = 120.1 mΩ cm², and PFOM = 15.5 MW cm⁻² (Table 4K).

Ohmic Contact Formation. On the aspect of reducing R_on,sp one primary task is to form high-quality ohmic contacts at the S/D regions. The commonly used metallization schemes on the β-Ga₂O₃ epitaxial layers include Ti/Au and Ti/Al/Ni/Au, followed by post-metallization annealing at 400–500 °C in nitrogen. The physical mechanisms for the ohmic contact formation between Ti/Au and Sn-doped β-Ga₂O₃ were investigated. It was found that at the junction between Ti and β-Ga₂O₃, a thin layer of Ti-TiOₓ which is partially lattice matched to the β-Ga₂O₃ can facilitate electron transport. Furthermore, the interdiffusion between Au and Ti can narrow the distance between the low-resistance Au and heavily doped β-Ga₂O₃. In addition to the metallization and annealing, high doping concentrations at the S/D regions are also critical to reduce the contact resistance. The commonly used doping methods include Si-implantation and Sn-doped spin-on-glass (SOG). After Si-implantation with the concentration 10¹⁹–10²⁰ cm⁻³, the implanted β-Ga₂O₃ substrates were annealed at 900–1000 °C in nitrogen to achieve a high activation efficiency of more than 60%. With the annealed Ti/Au electrodes, the specific contact resistance can be as low as 4.6 × 10⁻⁶ Ω cm². In another MOSFET work, the Ti/Au contacts (annealed at 470 °C in nitrogen for 1 min after metallization) on top of a Si-implanted S/D regions (Si = 5 × 10¹⁹ cm⁻³, annealed at 925 °C in nitrogen for 30 min after implantation) can achieve a similar specific contact resistance of 8.1 × 10⁻⁶ Ω cm². On the other hand, for the SOG doping, the S/D regions were first spin-coated with a 170-nm-thick layer of SOG (Sn = 4 × 10²¹ cm⁻³), followed by a 5 min and 1100 °C annealing process in nitrogen for the Sn ions to diffuse into the β-Ga₂O₃ layer. Lastly, the SOG layer was removed by a pH-buffered HF treatment. The Sn doping concentration is 4 × 10²¹ cm⁻³ at the surface and decays exponentially with the depth into the β-Ga₂O₃ layer. Combined with the annealed Ti/Au electrodes, the specific contact resistance is 2.1 × 10⁻⁵ Ω cm², which is much higher than the contact resistance achieved by the Si-implantation method. This could be part of the reason why the β-Ga₂O₃ MOSFETs with the SOG S/D contacts have relatively high R_on,sp and relatively low PFOM (Table 4E and F).

Recently, Jeong et al. demonstrated that by using CF₄ plasma treatment, an ohmic contact can be formed between the Ti/Al/Ti electrode and the Si-doped β-Ga₂O₃ epitaxial layer grown on a c-plane sapphire substrate by HVPE (Table 4J). The CF₄ plasma treatment was performed by using a reactive ion etcher with the RF power of 150 W and the slow introduction of CF₄ and O₂ gases into the chamber filled with nitrogen. Then, the Ti/Al/Ti metal stacks at the S/D regions were formed by evaporation, and the deposited electrodes are ohmic even without post-metallization annealing. However, the resulting specific contact resistance (2 × 10⁻³ Ω cm²) remains relatively high.

Recessed Gates and Self-Aligned Gates for RF Operation. So far, the high-breakdown electric field of β-Ga₂O₃ (8 MV cm⁻¹) has been mainly applied toward the
power switching application, for which the power device performance is evaluated by the PFOM = \( V_{DS}^2/R_{on,p} \) (Table 4). On the other hand, the high breakdown electric field of \( \beta\)-Ga\(_3\)O\(_5\) is also advantageous in the JFOM = (breakdown electric field) \times (electron saturation velocity), which describes the power-frequency product for the RF applications, such as RF amplifiers, RF switches, and power switching at GHz speed. Based on the combination of ab initio calculations and full band Monte Carlo simulations, a peak electron saturation velocity of \( 2 \times 10^7 \) cm s\(^{-1} \) is estimated at an electric field of 200 kV cm\(^{-1} \) (Table 1). Therefore, the JFOM of \( \beta\)-Ga\(_3\)O\(_5\) can be higher than GaN and SiC (Table 1). In light of this, in 2017, Green et al. demonstrated depletion-mode \( \beta\)-Ga\(_3\)O\(_5\) MOSFETs with recessed gates for small- and large-signal RF operations (Figure 3E). The epitaxial layers, including a 180-nm-thick Si-doped channel layer \( (1 \times 10^{18} \text{ cm}^{-3}) \) and a 25-mm-thick Si-doped ohmic layer \( (1 \times 10^{19} \text{ cm}^{-3}) \), were grown on a \( (100) \) \( \beta\)-Ga\(_3\)O\(_5\) substrate with a \( 6^\circ \) miscut by MOCVD, followed by multiple steps of lithographic RIE for the mesa device isolation and the formation of S/D regions and recessed gate. For the DC operation, the \( \beta\)-Ga\(_3\)O\(_5\) MOSFET exhibits maximum current density \( = 150 \text{ mA mm}^{-1} \) and maximum transconductance \( g_m \) of 21.2 mS mm\(^{-1} \) at \( V_{GS} = -3.5 \text{ V} \) and \( V_{DS} = 40 \text{ V} \). For the small-signal RF operation, the device exhibits cutoff frequency \( f_c \) and maximum oscillating frequency \( f_{\text{MAX}} \) equal to 2.7 and 12.9 GHz, respectively, at the DC biasing condition of maximum \( g_m \). For the large-signal CW RF operation, the device achieves output power \( P_{\text{OUT}} \) of 0.23 W mm\(^{-1} \) with power added efficiency (PAE) of 6.3\% at 800 MHz using passive source and load tuning. In 2019, Liddy et al. demonstrated depletion-mode \( \beta\)-Ga\(_3\)O\(_5\) MOSFETs with self-aligned refractory metal gates (SAGs) for eliminating the source access resistance (Figure 3F). The device fabrication started with the deposition of a 22-nm-thick Si-doped \( \beta\)-Ga\(_3\)O\(_5\) epitaxial layer on a Fe-doped \( (010) \) \( \beta\)-Ga\(_3\)O\(_5\) substrate by MOCVD and then a 30-nm-thick Al\(_2\)O\(_3\) gate dielectric by ALD, which can also serve as the implant cap. Next, the W/Cr gate electrode was formed by sputtering and lithographic RIE, followed by Si-implantation to define the S/D regions. Lastly, after removing the Al\(_2\)O\(_3\) implant cap, the annealed Ti/Al/Ni/Au metal stacks formed ohmic contacts to the implanted regions. Due to the negligible source access resistance and the short channel length \( (2.5 \mu\text{m}) \), the \( \beta\)-Ga\(_3\)O\(_5\) MOSFET achieves maximum \( g_m \) of 35 mS mm\(^{-1} \) at \( V_{GS} = 4 \text{ V} \) and \( V_{DS} = 10 \text{ V} \).

**Delta-Doped Channels and Oxygen Annealed UID Layers for RF Operation.** For the power devices operating at high frequencies, the gate length usually needs to be scaled into the sub-\( \mu \text{m} \) regime. However, such a small-sized gate would not be able to effectively control the channel if the channel thickness is higher than 200 nm. Therefore, approaches like recessed gates and thin channels with heavy doping have been adopted to alleviate this issue. In 2019, Xia et al. demonstrated \( \beta\)-Ga\(_3\)O\(_5\) metal–semiconductor FETs (MESFETs) with delta-doped channels for RF operations (Figure 3G). A monolayer of Si-ions dopants was implanted between two UID buffer layers, which were sequentially grown on a Fe-doped \( (010) \) \( \beta\)-Ga\(_3\)O\(_5\) substrate by PA-MBE. Based on Hall measurements on an isolated van der Pauw structure, the delta-doped channel has a sheet electron density of \( 1.13 \times 10^{18} \text{ cm}^{-2} \) with the electron mobility equal to \( 70 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1} \). The \( \beta\)-Ga\(_3\)O\(_5\) MOSFET can achieve maximum \( g_m \) of 44 mS mm\(^{-1} \) at \( V_{GS} = 2 \text{ V} \) and \( V_{DS} = 12 \text{ V} \), and record high \( f_c \) of 27 GHz and \( f_{\text{MAX}} \) of 16 GHz. In order to further improve the large-signal RF performance, it is critical to avoid current collapse at high
Table 5. Representative Enhancement-Mode $\beta$-Ga$_2$O$_3$ FETs with Various Device Structures and Fabricated by Different Deposition Techniques$^a$

| Features | Substrates/Gates | Dielectric | Epitaxial Layers | Carrier Concentrations | $V_{th}$ (V) | $R_{on}$ (mΩ cm$^2$) | $V_{gs}/R_{on}$ (MW cm$^{-2}$) | $I_{on}$/sp | $I_{on}$/sp ref |
|----------|-----------------|------------|------------------|------------------------|--------------|------------------|-----------------------------|---------|----------------|
| (A)      | Lateral finFET  | Mg-doped (100) $\beta$-Ga$_2$O$_3$/20 nm Al$_2$O$_3$ | MOCVD  | Fin-array: $2.3 \times 10^{17}$ cm$^{-3}$ | $612$ ($V_{gs} = 0$ V) ($L_{sd} = 21$ μm ($W_cc = 19$ μm) | $\sim 1.6$ ($V_{gs} = 4$ V) ($L_{sd} = 4$ μm) ($W_cc = 19$ μm) | NR | $> 0.18$ mA mm$^{-1}$ ($V_{gs} = 4$ V) ($L_{sd} = 4$ μm) ($W_cc = 19$ μm) | 2016$^{11,2}$ |
| (B)      | Lateral MOSFET  | Fe-doped (010) $\beta$-Ga$_2$O$_3$/50 nm Al$_2$O$_3$ | OA-MBE | Channel: $< 4 \times 10^{14}$ cm$^{-3}$ | $40$ ($V_{gs} = 0$ V) ($L_{sd} = 4$ μm) | $22.5$ ($V_{gs} = 17$ V) ($L_{sd} = 4$ μm) | $\sim 7.1 \times 10^{-3}$ | $1.4$ mA mm$^{-1}$ ($V_{gs} = 38$ V) ($L_{sd} = 4$ μm) | 2017$^{11,3}$ |
| (C)      | Lateral MOSFET  | Fe-doped (010) $\beta$-Ga$_2$O$_3$/50 nm Al$_2$O$_3$ | MOCVD  | Channel (without oxygen annealing): $2 \times 10^{14}$ cm$^{-3}$ | $3000$ ($V_{gs} = 0$ V) ($L_{sd} = 17$ μm) | $163$ ($V_{gs} = 9$ V) ($L_{sd} = 17$ μm) | $5.52$ | $6.4$ mA mm$^{-1}$ ($V_{gs} = 9$ V) | 2020$^{11,4}$ |
| (D)      | Lateral MOSFET  | Fe-doped (010) $\beta$-Ga$_2$O$_3$/20 nm SiO$_2$ | OA-MBE | Channel: $> 5.5 \times 10^{17}$ cm$^{-3}$ | $505$ ($V_{gs} = 0$ V) ($L_{sd} = 8$ μm) | $172$ ($V_{gs} = 8$ V) ($L_{sd} = 8$ μm) | $14.8$ | $> 40$ mA mm$^{-1}$ ($V_{gs} = 8$ V) ($L_{sd} = 8$ μm) | 2018$^{11,5}$ |
| (E)      | Lateral MOSFET  | Si+/300 nm SiO$_2$ | RF sputtering $\rightarrow$ 900 °C for 1 h in open air $\rightarrow$ SOG doping | Channel: $\approx 1.7 \times 10^{11}$ cm$^{-3}$ | $224$ ($V_{gs} = V_{th} = -70$ V) | $1.8 \times 10^{-7}$ ($V_{gs} = V_{th} = 90$ V) | $2.8 \times 10^{-10}$ | $< 15$ mA mm$^{-1}$ ($V_{gs} = -70$ V) | 2021$^{11,6}$ |
| (F)      | Vertical MOSFET | n-type (001) $\beta$-Ga$_2$O$_3$/30 nm Al$_2$O$_3$ | HVPE  | Source region: $5 \times 10^{19}$ cm$^{-3}$ | $105$ ($V_{gs} = 0$ V) | $18$ ($V_{gs} = 3$ V) | $< 62.1$ | $< 300$ A cm$^{-2}$ ($V_{gs} = 3$ V) | 2018$^{11,7}$ |
| (G)      | Vertical MOSFET | Sn-doped (001) $\beta$-Ga$_2$O$_3$/50 nm Al$_2$O$_3$ | HVPE  | Source region: $5 \times 10^{19}$ cm$^{-3}$ | $263$ ($V_{gs} = 0$ V) | $135$ ($V_{gs} = 6$ V) | $0.5$ | 26 A cm$^{-2}$ ($V_{gs} = 6$ V) | 2020$^{11,8}$ |
| (H)      | Lateral MOSFET  | Fe-doped (010) $\beta$-Ga$_2$O$_3$/20 nm Al$_2$O$_3$ | PA-MBE | Channel: $1 \times 10^{18}$ cm$^{-3}$ | NR | NR | NR | $1.2$ mA mm$^{-1}$ ($V_{gs} = 8$ V) ($L_{sd} = 4$ μm) | 2019$^{11,9}$ |

$^a$For each power device, the parameters for evaluating the power switching performance are summarized, including the three-terminal off-state breakdown voltage ($V_{br}$), on-resistance normalized by the device area ($R_{on}$), power figure of merit ($PFOM = V_{br}/R_{on}$), maximum saturation drain current ($I_{on}$/sp) and $I_{on}$/sp ratio.
drain bias ($V_{GD}$). Therefore, a UID buffer layer is always needed to keep the channel away from the Fe- or Mg-doped insulating substrate. However, background donors, such as Si or hydrogen or oxygen vacancies due to imperfect epitaxy, may lead to a background electron concentration $10^{15} – 10^{16}$ cm$^{-3}$. To resolve the issue of conductive UID layers, in 2020, Lv et al. applied an oxygen annealing process for compensating and neutralizing the donors in the UID layer (Figure 3H). Following the epitaxial growth of a 0.2-μm-thick Si-doped channel and a 0.5-μm-thick UID buffer layer and the formation of ohmic contacts at the S/D regions, the channel region was deposited with a 0.2-μm-thick SiN passivation layer by plasma-enhanced CVD (PECVD), followed by lithographic etching to expose the gate foot region for the oxygen annealing process (500 °C for 5 min in oxygen atmosphere). The $\beta$-Ga$_2$O$_3$ MOSFET with the oxygen annealing treatment can achieve maximum $I_{on}$ of 11 mS mm$^{-1}$ at $V_{GS} = 10$ V and $V_{DS} = 20$ V, and $f_T = 1.8$ GHz, $f_{MAX} = 4.2$ GHz, $P_{OUT} = 0.4$ W cm$^{-2}$, and PAE = 10% for the large-signal CW RF operation at 1 GHz.

**ENHANCEMENT-MODE $\beta$-Ga$_2$O$_3$ FETS**

For mitigating off-state power loss and ensuring safe operation at high voltages, normally off enhancement-mode transistors are usually preferable to depletion-mode transistors, which can be as large as 612 V at $V_{DS} = 0$ V (Table 5A). Following this concept, in 2016, Chabak et al. demonstrated $\beta$-Ga$_2$O$_3$ wrap-gate FinFETs capable of normally off operation with the $V_{TH}$ between 0 and 1 V (Figure 4A). The fabrication of the $\beta$-Ga$_2$O$_3$ FinFET array started on a 300-nm-thick Sn-doped $\beta$-Ga$_2$O$_3$ epitaxial layer grown on a Mg-doped (100) $\beta$-Ga$_2$O$_3$ substrate by MOCVD, and then Cr hard mask arrays of ~300-nm-wide fin channels separated with ~900 nm pitch were formed on the $\beta$-Ga$_2$O$_3$ epitaxial layer by electron beam lithography (EBL) and metal evaporation. Subsequently, a RIE step using BCl$_3$ chemistry, with the etching selectivity Ga$_2$O$_3$/Cr ≈ 2:1, removed the entire Cr mask while creating triangular-shaped fins. The $\beta$-Ga$_2$O$_3$ wrap-gate FinFET with the $L_{GD} = 4$ μm and $L_{C} = 2$ μm can achieve an $I_{on}/I_{off}$ ratio larger than 10$^5$ but only a very limited $I_{DSS}$ of ~0.18 mA mm$^{-1}$. With the $L_{GD}$ increased to 21 μm, the $V_{BS}$ can be as large as 612 V at $V_{GS} = 0$ V (Table 5A).

**UID or Oxygen Annealed Channels**

Compared to the complex fin-shaped channels, in 2017, Wong et al. demonstrated that by using a relatively simple, 4-μm-long UID channel defined by Si-ion implantation, enhancement-mode $\beta$-Ga$_2$O$_3$ MOSFETs with positive $V_{TH}$ can be realigned (Figure 4B). Following the deposition of a 1.2-μm-thick UID buffer layer on a Fe-doped (001) $\beta$-Ga$_2$O$_3$ substrate by OA-MBE, the S/D regions as well as the access regions were formed by Si-ion implantation ($5 \times 10^{19}$ cm$^{-3}$), leaving a 4 μm undoped gap as the channel region. The background electron concentration was estimated to be less than $4 \times 10^{14}$ cm$^{-3}$ by C–V analysis on a Schottky barrier diode (SBD) comprising Pt/$\beta$-Ga$_2$O$_3$/UID. The $\beta$-Ga$_2$O$_3$ MOSFET can achieve an $I_{on}/I_{off}$ ratio nearly 10$^6$ and a decent $I_{DSS}$ = 1.4 mA mm$^{-1}$. However, the $V_{th}$ is only ~40 V, which is attributed to premature breakdown through the Al$_2$O$_3$ dielectric layer between the gate and drain (Table 5B). Previously, an oxygen annealing process was applied for compensating and neutralizing the background donors in the UID layer, in order to improve the MOSFET’s large-signal RF performance (Figure 3H). Following the same concept, in 2020, Lv et al. demonstrated that the oxygen annealing treatment under the gate region can exhaust the electron concentration in the channel, leading to normally off operation (Figure 4C). A 0.6-μm-thick UID buffer layer and a 0.2-μm-thick Si-doped (2 × 10$^{17}$ cm$^{-3}$) channel layer were epitaxially grown on a Fe-doped (010) $\beta$-Ga$_2$O$_3$ substrate by MOCVD. After the formation of ohmic contacts at the S/D regions, a 0.2-μm-thick SiN was deposited via PECVD, followed by lithographic etching to expose the gate foot region for the oxygen annealing process (500 °C for 5 min in oxygen atmosphere). The $\beta$-Ga$_2$O$_3$ MOSFET with the double source-connected field-plates and $L_{GD} = 17$ μm can achieve record high $V_{br} > 3000$ V in Fluorinert FC-770, $R_{on,sp} = 163$ mΩ cm$^{-2}$, and PFOM = 55.2 MW cm$^{-2}$ (Table 5C).

**Recessed Gates or Ultrathin Channels.** As described previously, small-sized and recessed gates are useful in rapidly controlling the channels for RF operations. In 2018, Chabak et al. demonstrated that if the active channel thickness, decreased by the recessed gate, is small enough, the gated region of the channel can be fully depleted at $V_{GS} = 0$ V (Figure 4D). The channel, a 0.2-μm-thick Si-doped $\beta$-Ga$_2$O$_3$ epitaxial layer, was grown on a Fe-doped (010) $\beta$-Ga$_2$O$_3$ substrate, followed by a similar recessed gate formation process as described previously. The recess depth was ~140 nm, leaving the active channel thickness of ~60 nm in the gated region. Based on Hall measurements on several unetched van der Pauw structures, the undepleted channel layer has an average minimum free carrier concentration of 5.5 × 10$^{12}$ cm$^{-3}$ and an average sheet electron mobility of 106 cm$^2$ V$^{-1}$ s$^{-1}$. The enhancement-mode $\beta$-Ga$_2$O$_3$ MOSFET, with the recessed gate design, $L_C = 1$ μm and $L_SD = 8$ μm, can achieve $V_{th}$ = 505 V, $R_{on,sp} = 17.2$ mΩ cm$^{-2}$, and PFOM = 14.8 MW cm$^{-2}$ (Table 5D). Following the concept of applying an ultrathin, fully depleted channel for enhancement-mode FETs, in 2021, Yoon et al. demonstrated that 8-nm-thick Sn-doped polycrystalline $\beta$-Ga$_2$O$_3$ thin films can serve as the channels of bottom-gate MOSFETs capable of normally off-high voltage operation (Figure 4E). The device fabrication started with the deposition of an amorphous 8 nm thin Ga$_2$O$_3$ thin film on a SiO$_2$/p+ Si substrate by RF sputtering, followed by annealing at 900 °C for 1 h in an open atmosphere for crystallization into monoclinic $\beta$-Ga$_2$O$_3$. The n-type doping of the $\beta$-Ga$_2$O$_3$ thin film was accomplished by a similar SOG method as described previously. Finally, the S/D electrodes were formed by the deposition of Ti/TiN metal stacks by RF sputtering. The optical bandgap of the 8-nm-thin Sn-doped polycrystalline $\beta$-Ga$_2$O$_3$ thin film (5.77 eV) is higher than that of a 100-nm-thick $\beta$-Ga$_2$O$_3$ thin film (4.7 eV) due to the quantum confinement effect. The back-gate MOSFET with the nanomembrane channel can achieve high $V_{th}$ = 224 V, but the $R_{on,sp}$ and $I_{DSS}$ are unsatisfactory compared to conventional $\beta$-Ga$_2$O$_3$ FETs fabricated by epitaxy (Table 5E).

**Vertical Fins or Current Apertures.** In 2018, Hu et al. demonstrated high-voltage, vertical $\beta$-Ga$_2$O$_3$ MOSFETs which can remain in the off-state with $V_{GS} = 0$ V under $V_{DS} > 1$ kV (Figure 4F). A 10-μm-thick Si-doped ($N_d < 2 \times 10^{16}$ cm$^{-3}$) n-drift layer was grown on an n-type (001) $\beta$-Ga$_2$O$_3$ substrate by HVPE, followed by Si-ion implantation ($N_d = 5 \times 10^{15}$ cm$^{-3}$) on the epitaxial layer to form the source region. Then,
the vertical channel was formed by RIE with the patterned Pt metal mask which defines the position and area of the source. A 30-nm-thick Al₂O₃ was deposited by ALD as the gate dielectric, followed by sputtering a 50-nm-thick Cr as the gate electrode. The vertical β-Ga₂O₃ MOSFET with the source area equal to 0.33 μm × 80 μm can achieve V_{br} = 1057 V at V_{GS} = 0 V and R_{on,sp} ∼ 18 mΩ cm², resulting in PFOM ∼ 62.1 MW cm⁻² (Table 5F).

Following the concept of vertical fin channel, in 2020, Wong et al. used N-ion implanted current blocking layers (CBLs) to form vertical current apertures connecting between drain and source (Figure 4G). A 9-μm-thick Si-doped (1.5 × 10¹⁶ cm⁻³) n-drift layer was formed on a Sn-doped (001) β-Ga₂O₃ substrate by HVPE, followed by chemical mechanical polishing. The 0.8-μm-thick CBLs were formed in the epitaxial layer by N-ion implantation (1.5 × 10¹⁹ cm⁻³), followed by annealing at 1100 °C for 30 min in nitrogen to remove implantation damage and activate the implanted N as compensating acceptors. Subsequently, Si-ion implantation was conducted to form the channel regions, source access regions, and source contact layers, with the doping concentrations equal to 5 × 10¹⁷ cm⁻³, 2 × 10¹⁸ cm⁻³, and 5 × 10¹⁹ cm⁻³, respectively, followed by annealing at 950 or 800 °C for 30 min in nitrogen for the donor activation. The vertical β-Ga₂O₃ MOSFET with the CBL formed vertical current aperture can achieve V_{br} = 263 V at V_{GS} = 0 V and R_{on,sp} = 135 mΩ cm², resulting in PFOM = 0.5 MW cm⁻² (Table 5G).

N-Doped p-Type Channel. Theoretically, N can act as deep acceptors in β-Ga₂O₃, while Si has been experimentally confirmed as shallow donors. In 2019, Kamimura et al. demonstrated that by controlling the doping concentration ratio between N and Si, the β-Ga₂O₃ UID layer can behave as a p-type channel, based on which an enhancement-mode β-Ga₂O₃ MOSFET can be obtained (Figure 4H).

For each β-Ga₂O₃ nanomembrane FET, the parameters for evaluating the device performance are summarized, including the threshold voltage (V_{TH}), maximum drain current (I_{d,max}), I_{on}/I_{off} ratio, subthreshold slope (SS), maximum transconductance (g_m_{max}), and breakdown voltage (V_{br}).
higher than the Si concentration (2 × 10^{17} \text{ cm}^{-3}), making the UID channel p-type. The enhancement-mode $\beta$-Ga$_2$O$_3$ MOSFET with the p-type UID channel and the $V_{TH} > +8$ V can achieve a $I_{on}/I_{off}$ ratio larger than 10$^5$, but the $I_{dssat}$ remained low at 1.2 $\mu$A mm$^{-1}$, since the $V_{GS}$ swing was limited up to +8 V by the Al$_2$O$_3$ gate leakage (Table S1).$^{122}$

\section{$\beta$-Ga$_2$O$_3$ NANOMEMBRANE FETS}

Despite its UWBG (4.9 eV) and high breakdown electric field (8 MV cm$^{-1}$), one obvious drawback of $\beta$-Ga$_2$O$_3$ is the relatively low thermal conductivity (21 W m$^{-1}$ K$^{-1}$ in [010]), compared to Si (150 W m$^{-1}$ K$^{-1}$), SiC (270 W m$^{-1}$ K$^{-1}$), and GaN (210 W m$^{-1}$ K$^{-1}$) (Table 1). In 2014, Hwang et al. found that $\beta$-Ga$_2$O$_3$ nanomembranes can be easily synthesized by an exfoliation process similar to that of graphene and transferred to a different semiconductor platform.$^{123}$ Although $\beta$-Ga$_2$O$_3$ is not a layered material like graphene, the ease of exfoliation is likely attributed to the monoclinic structure and the higher lattice parameter along the [010] direction than the [001] directions. The integration scheme is beneficial for on-chip power management and enables the formation of heterojunctions, which may open the possibilities of new (opto) electronic applications. Particularly, in contrast to the low power switching applications demonstrated by other nanomaterials, such as graphene, MoS$_2$, and WSe$_2$, $\beta$-Ga$_2$O$_3$ nanomembrane FETs aim at achieving high-power switching in low dimensions.

**Shifting from Depletion- to Enhancement-Mode.** As mentioned previously, the enhancement-mode power devices enable fail-safe operation and simplify circuit designs at the system level. For the $\beta$-Ga$_2$O$_3$ nanomembrane FETs, the $V_{TH}$ can be shifted from negative to positive via various approaches. In 2017, Zhou et al. showed that the $V_{TH}$ of bottom-gate MOSFETs ($\beta$-Ga$_2$O$_3$/SiO$_2$/p$^+$ Si) can be increased from $-120$ V to $\sim 80$ V, when the thickness of the $\beta$-Ga$_2$O$_3$ nanomembrane channel was shrunken from 110 to 50 nm.$^{127}$ In 2019, Kim et al. found that by applying remote CF$_2$ plasma on part of the $\beta$-Ga$_2$O$_3$ nanomembrane, the $V_{TH}$ of the bottom-gate MOSFETs can be increased from $-7.5$ V without the treatment to $\sim 2$ V with the treatment.$^{128}$ In 2022, Wang et al. demonstrated that by forming a heterojunction between the p-type SnO and n-type $\beta$-Ga$_2$O$_3$ nanomembrane, the $V_{TH}$ of the bottom-gate MOSFETs (SnO/$\beta$-Ga$_2$O$_3$/SiO$_2$/p$^+$ Si) can be increased from $-40$ V without SnO to $\sim 5$ V with 12 nm SnO.$^{129}$

**Bottom-Gate MOSFETs.** To effectively control the channels of the $\beta$-Ga$_2$O$_3$ nanomembrane MOSFETs, i.e., to decrease the subthreshold slope ($SS$, mV/dec) of the MOSFET, various gating schemes have been investigated. The most widely used scheme is the bottom-gate MOSFETs,$^{123,127,130}$ in which a $\beta$-Ga$_2$O$_3$ membrane (as the channel), exfoliated from a (−201) bulk $\beta$-Ga$_2$O$_3$ crystal, is transferred to the surface of a SiO$_2$ dielectric layer (as the gate dielectric) deposited on a heavily doped Si substrate (as the bottom-gate). The $\beta$-Ga$_2$O$_3$ nanomembrane firmly adheres to the SiO$_2$ surface through the bond-free van der Waals force. Subsequently, the S/D regions are defined by EBL, followed by Ti/Al/Au or Ti/Au metallization and a lift-off process. Two representative bottom-gate $\beta$-Ga$_2$O$_3$ nanomembrane FETs and their electrical characteristics are shown in Figure 5A and B.$^{123,127}$ It is worth mentioning that an Ar plasma bombardment process prior to the S/D metallization step can effectively reduce the contact resistance. Without the Ar bombardment, the contacts may show Schottky-like behaviors.$^{127}$ Furthermore, to achieve high drain currents, the $\beta$-Ga$_2$O$_3$ nanomembrane channels need to have adequate electron concentrations. Therefore, heavily doped crystals (2.7 × 10^{18} \text{ cm}^{-3}), from which the nanomembranes are exfoliated, are desirable.$^{127}$ The bottom-gate $\beta$-Ga$_2$O$_3$ nanomembrane FETs also exhibit much better temperature and air stabilities, compared to devices based on conventional 2D transition metal dichalcogenides. No degradation of electrical characteristics was observed when the operating temperature was elevated to 250 °C or after a month-long storage in ambient condition.$^{130}$ Moreover, the electrical properties of the bottom-gate $\beta$-Ga$_2$O$_3$ nanomembrane FETs can be improved by Al$_2$O$_3$ surface passivation, which reduces surface states and absorbates at the nanomembrane surface.$^{31}$

**Dual-Gate FETS.** To further enhance the channel control, dual-gate $\beta$-Ga$_2$O$_3$ nanomembrane FETs have been developed recently.$^{132,133}$ In 2019, Ma et al. demonstrated a dual-gate $\beta$-Ga$_2$O$_3$ nanomembrane FET, comprising a top-gate MESFET and a bottom-gate MOSFET, as shown in Figure SC.$^{132}$ Upon the bottom-gate MOSFET ($\beta$-Ga$_2$O$_3$/SiO$_2$/p$^+$ Si), the top-gate electrode (Ni/Au) was deposited over a part of the $\beta$-Ga$_2$O$_3$ channel by EBL and lift-off processes. A Schottky contact is formed at the Ni/$\beta$-Ga$_2$O$_3$ interface. Therefore, when a negative potential is applied to the top-gate, the depletion width of the Schottky junction expands, reducing the effective channel thickness. Compared to the bottom-gating mode, the $\beta$-Ga$_2$O$_3$ nanomembrane FET operating in the dual-gating mode exhibited a positively shifted $V_{TH}$, a much higher $g_{m_{max}}$, and a much lower $SS$.$^{132}$ In 2020, Kim et al. demonstrated double graphene-nanomembrane $\beta$-Ga$_2$O$_3$ nanomembrane MESFETs (graphene/$\beta$-Ga$_2$O$_3$/graphene), as shown in Figure SD.$^{133}$ The graphene and $\beta$-Ga$_2$O$_3$ nanomembranes were mechanically exfoliated from the pyrolytic graphite and ($−201$) $\beta$-Ga$_2$O$_3$ crystals, respectively, and subsequently integrated into the multilayered architecture via van der Waals heterojunctions on a SiO$_2$/p$^+$ Si substrate. The S/D electrodes were formed by EBL and lift-off processes, followed by a rapid thermal annealing step (1 min in Ar at 480 °C) to form ohmic contacts with the $\beta$-Ga$_2$O$_3$ channel. Compared to the single graphene-gate device with a negative $V_{TH} (−0.96 \text{ V})$, the double graphene-gate $\beta$-Ga$_2$O$_3$ MESFET operated with a positive $V_{TH} (+0.25 \text{ V})$ and achieved a low $SS$ (68.9 mV/dec). The excellent electrical properties are attributed to the high crystallinity of each exfoliated nanomembrane and the high-quality interface between graphene and $\beta$-Ga$_2$O$_3$.$^{133}$

**Bottom-Gate MESFETs.** In addition to the Schottky junctions described previously (Ni/$\beta$-Ga$_2$O$_3$ and graphene/$\beta$-Ga$_2$O$_3$),$^{132,133}$ in 2021, Kim et al. demonstrated bottom-gate nanomembrane MESFETs based on the Schottky junctions of Nb(or Ta)S$_2$/β-Ga$_2$O$_3$, as shown in Figure SE.$^{134}$ The exfoliated Nb(or Ta)S$_2$ nanoflake as the bottom-gate was dry-transferred onto an Al$_2$O$_3$-coated glass substrate by polydimethylsiloxane (PDMS) stamping. Then the $\beta$-Ga$_2$O$_3$ nanomembrane channel was precisely aligned and electrostatically transferred onto the Nb(or Ta)S$_2$ nanoflake. The S/D and gate electrodes (Ti/Pt) were defined by photolithography, sputtering deposition, and lift-off processes. Note that after the UV exposure and development, plasma treatment to the $\beta$-Ga$_2$O$_3$ was performed for improving the ohmic contacts. Due to $\beta$-S$_2$’s larger work function ($5.6$ eV) than usual novel metals, the TaS$_2$ bottom-gate $\beta$-Ga$_2$O$_3$ nanomembrane MESFET achieved a record low (61 mV/dec) with a negative
Waals bonding, as shown in Figure 5G. and n-type nanomembranes, as shown in Figure 5F. nanomaterials, junction FETs (JFETs) of various forms have nanomembranes and other two-dimensional semiconductor V

The 4H-SiC can...melting methods, such as the FZ,...recently. Compared to the commercialized semiconductors, such as Si, GaN, and SiC, power devices based on β-Ga2O3 are capable of handling high voltages in smaller dimensions and with higher efficiencies. Furthermore, the β-Ga2O3 bulk crystals can be synthesized by the relatively low-cost melt growth methods, such as the FZ, CZ, and EFG methods, making the single-crystal substrates and epitaxial layers readily accessible. Several epitaxy fabrication started with the homoepitaxial growth of a p-type 4H-SiC layer (1 μm thick and doping concentration equal to 2 × 10^{17} \text{ cm}^{-3}). Then, two hydrogen silsesquioxane (HSQ) covered regions, for insulating the S/D electrodes from the conductive 4H-SiC layer, were formed by EBL, followed by developing using 25% tetramethylammonium hydroxide. An exfoliated β-Ga2O3 nanomembrane was dry-transferred onto the HSQ and 4H-SiC to form the channel. Lastly, the S/D electrodes were fabricated by EBL, metallization, and lift-off, followed by rapid thermal annealing for creating ohmic contacts with the β-Ga2O3 channel. When applied with a negative VGS, the depletion width of the heterojunction between the p-type 4H-SiC and n-type β-Ga2O3 increases, narrowing the effective channel thickness. The 4H-SiC bottom-gate β-Ga2O3 nanomembrane JFET operated in the depletion-mode with the VTH = −7.4 V and SS = 114 mV/dec. Most importantly, for the same input power of 160 W m⁻¹, the JFET based on the 4H-SiC substrate exhibited a peak temperature at least 100 °C lower than based on a sapphire substrate, manifesting the stronger heat dissipation of the 4H-SiC substrate. Interestingly, in 2021, Choi et al. demonstrated ambipolar JFETs based on van der Waals heterojunctions formed between exfoliated p-type MoTe2 flakes and exfoliated n-type β-Ga2O3 nanomembranes, either of which can function as the channel, as shown in Figure 5H. With the MoTe2 as the bottom-gate and the β-Ga2O3 as the channel, the JFET operated in the depletion-mode with the VTH × −4 V and Ion/Ioff ratio ∼10^4.

**CONCLUSION**

Due to its UWBG (4.9 eV) and large breakdown electric field (8 MV cm⁻¹), β-Ga2O3 has attracted renewed attention as one of the next-generation semiconductors recently. Compared to the commercialized semiconductors, such as Si, GaN, and SiC, power devices based on β-Ga2O3 are capable of handling high voltages in smaller dimensions and with higher efficiencies. Furthermore, the β-Ga2O3 bulk crystals can be synthesized by the relatively low-cost melt growth methods, such as the FZ, CZ, and EFG methods, making the single-crystal substrates and epitaxial layers readily accessible. Several epitaxy

Figure 6. (A) Representative depletion-mode β-Ga2O3 FETs with the Vbr and Rnmax listed in Table 4 (red circles). (B) Representative enhancement-mode β-Ga2O3 FETs with the Vbr and Rnmax listed in Table 5 (green circles). The black and blue dashed lines represent the Baliga’s theoretical limits for Si and β-Ga2O3, respectively.
techniques have been investigated for the depositions of α, ε-, and β-phase Ga2O3, including MOCVD, LPCVD, PA-MBE, HVPE, and mist-CVD, among which MOCVD is most widely used while HVPE offers relatively high growth rates. For the homoepitaxy on the (100) β-Ga2O3 substrates, despite ultraflat surfaces obtained, stacking faults in the form of twin lamellae are usually observed in the epitaxial layers, which however can be avoided by using substrates with relatively large miscut angles. In contrast, the epitaxial layers based on the (010) β-Ga2O3 substrates possess better crystal qualities, and the heat transfer along the [010] direction is more efficient than along the [100] direction. Therefore, Fe-doped semi-insulating (010) β-Ga2O3 substrates are widely used for fabricating high-performance β-Ga2O3 MOSFETs. On the other hand, the β-Ga2O3 epitaxial layers grown on c-plane sapphire substrates, although showing clear (−201)-oriented XRD patterns, are not thoroughly single-crystal, because of the symmetry mismatch between the monoclinic β-Ga2O3 and hexagonal Al2O3. The orthorhombic ε-Ga2O3 can be better matched to the sapphire substrates, but tends to transform into β-Ga2O3 upon high-temperature annealing. Therefore, so far the great majority of the β-Ga2O3 FETs have been built on the homoepitaxial layers, although heteroepitaxy on the sapphire substrates in the long term should be the more cost-effective solution.

For the power switching application, to exploit the full potential of β-Ga2O3, many device-level approaches have been developed to increase $V_{th}$ and decrease $R_{on,p}$ for maximizing PFOM. The depletion-mode β-Ga2O3 FETs with gate- or source-connected field-plates, Fluorinert immersion, and SiN$_x$ passivation can effectively avoid premature breakdown through the β-Ga2O3 channel and air, resulting in $V_{th}$ higher than 1000 V. On the aspect of reducing $R_{on,p}$, the Ge-doped β-Ga2O3 channels possess higher electron mobility than the Sn-doped channels, and the 2DEG channels of the heterostructure FETs also exhibit high electron mobility (>100 cm$^2$/V·s) due to the absence of impurity scattering. In addition, ohmic contacts with the channels can be formed via Ti/Au metallization followed by annealing, and the heavily doped S/D regions can be obtained by Si-ion implantation or SOG. As shown in Figure 6A, although some depletion-mode β-Ga2O3 FETs have already achieved $V_{th}$ higher than 1000 V, further reduction of $R_{on,p}$ is necessary, so that the β-Ga2O3 FETs’ PFOMs can advance closer to the Baliga’s theoretical limit. For the RF amplification application, it is desirable for the power devices to have large transconductance gain (gm) and wide bandwidth ($f_T$ and $f_{MAX}$). To better control the channels, which leads to high gm, recessed gates and delta-doped channels have been applied for the depletion-mode β-Ga2O3 FETs, resulting in gm higher than 20 mS·mm$^{-1}$. For increasing the bandwidth, parasitic capacitance and resistance of the β-Ga2O3 FETs needs to be minimized. In light of this, the SAGs have been adopted for eliminating the source access resistance.

For mitigating off-state power loss and ensuring safe operation at high voltages, enhancement-mode FETs are usually preferable to depletion-mode ones. Despite the lack of p-type doping, several device-level approaches have been developed to shift the $V_{TH}$ of the β-Ga2O3 FETs from negative to positive. The main idea is to deplete the gated region of the channel. For example, the metal wrap-gates of the finFETs can partly or fully deplete the narrow fin channels with enhanced electrostatics. Following the same idea, the enhancement-mode β-Ga2O3 FETs with ultrathin channels, recessed gates, vertical fin channels and vertical current apertures have been demonstrated. In addition, the electron concentrations of the channels can be exhausted by using oxygen annealing or by simply adopting an UID channel. It is worth mentioning that p-type UID channels have been demonstrated by using N-ion implantation. However, the drain currents of such devices remained low. Despite the tremendous progress recently, as shown in Figure 6B, the performance of the enhancement-mode β-Ga2O3 FETs in general is still lagging the depletion-mode ones in terms of $V_{th}$ and $R_{on,p}$. Lastly, to resolve the low-temperature conductivity issue of β-Ga2O3, exfoliated nanomembranes of β-Ga2O3 are integrated into multilayered structures on various semiconductor platforms for better heat dissipation. Based on the strain-free van der Waals heterojunctions which can control the effective channel thickness, the electrical characteristics of the β-Ga2O3 nanomembrane FETs can be easily modulated. Depending on the gating schemes, a great variety of β-Ga2O3 nanomembrane FETs have been explored, such as bottom-gate MOSFETs (β-Ga2O3/SiO2/p+ Si), top-gate MESFETs (Ni/β-Ga2O3), dual-gate MESFETs (graphene/β-Ga2O3/graphene), bottom-gate MESFET (β-Ga2O3/TaS2), top-gate JFETs (p-type WSe2/n-type β-Ga2O3 and p-type BP/n-type β-Ga2O3), and bottom-gate JFETs (n-type β-Ga2O3/p-type SiC and n-type β-Ga2O3/p-type MoTe2). In general, the β-Ga2O3 nanomembrane FETs possess strong channel control capability, with the SS lower than 200 mV/dec, which is favorable for the high-frequency power switching application. However, the $V_{th}$ and gm of the β-Ga2O3 nanomembrane FETs are lower than the epitaxial β-Ga2O3 FETs.

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