Long-term electrical characteristics
of a poly-3-hexylthiophene water-gated thin-film transistor

Axel Luukkonen, Amit Tewari, Kim Björkström, Amir Mohammad Ghafari, and Ronald Österbacka∗

Physics, Faculty of Science and Engineering, Åbo Akademi University, Henriksgatan 2, 20500 Turku, Finland

Eleonora Macchia

Physics, Faculty of Science and Engineering, Åbo Akademi University, Henriksgatan 2, 20500 Turku, Finland

Dipartimento di Farmacia - Università degli Studi di Bari Aldo Moro, Via Orabona 4, 70125 Bari, Italy

Fabrizio Torricelli

Department of Information Engineering, University of Brescia, Via Branze 38, 25123 Brescia, Italy

Luisa Torsi

Dipartimento di Chimica - Università degli Studi di Bari Aldo Moro, Via Orabona 4, 70125 Bari, Italy

(Dated: August 25, 2022)

Organic water-gated thin-film transistors (WG-TFTs) are of great interest in developing low-cost and high-performance biosensors. The device’s sensitivity to changes in measurement conditions can impair long-term operation, and care must be taken to ensure that the WG-TFT sensor response is due to an actual biorecognition event occurring on the sensing electrode. This work aims to clarify the long-term stability of a poly-3-hexylthiophene (P3HT) WG-TFT operated intermittently over two months during 5750 measurement cycles. We have evaluated the device figures of merit (FOM), such as threshold voltage, mobility, and trap density, during the whole measurement period. Short-term changes in the FOM are mainly attributed to work function changes on the gate electrode, whereas long-term changes are consistent with an increase in the semiconductor trap density. The shift in threshold voltage and decrease in mobility are found to be linear as a function of measurement cycles and caused by electrical stress, with time immersed in water having a negligible effect on the device. The trap density-of-states estimated using the subthreshold slope is similar to earlier reported values for P3HT OFETs and exhibits a gradual increase during device use and a partial recovery after rest, indicating the formation of shorter- and longer-lived traps.

I. INTRODUCTION

Water-gated thin-film transistors (WG-TFTs) employ water as a gate dielectric as opposed to the solid dielectric, typically SiO₂, used in conventional organic field-effect transistors (OFETs).

The WG-TFT, illustrated in Fig. 1, is made up of three parts: (i) the semiconductor deposited on the substrate and contacted with the source and drain electrodes, (ii) the aqueous gate dielectric, and (iii) the gate electrode, usually metallic. Due to the formation of electrical double layers at the gate electrode and semiconductor surface upon applying a gate voltage, the gating capacitance is considerably higher than in conventional OFETs. This enables low-voltage (< 1 V) operation and makes the device highly sensitive to electrical or capacitive changes at the gate-electrolyte and semiconductor-electrolyte interfaces, making the WG-TFT attractive for use in biosensors. While WG-TFTs have demonstrated high performance in a biosensor setting, the device stability can still be improved to shorten measurement times and lengthen the usable device lifetime. The device should also be as stable as possible to avoid incorrect readings during sensing measurements.

Device degradation in conventional organic field-effect transistors (OFETs) typically manifests as decreased source-drain current, increased hysteresis, a shift in threshold voltage, and increased gate leakage. An increase in trap density is the main cause of these effects. Electrical degradation in WG-TFTs is expressed similarly. However, the degradation mechanisms in WG-TFTs are challenging to pinpoint and model due to the complexity of the double layers. Furthermore, operation in aqueous environments

FIG. 1. A simple schematic of a WG-TFT with interdigitated source and drain (S-D) electrodes.
can lead to unwanted electrochemical effects, causing increased doping and oxidation of the semiconductor and rapid degradation of the WG-TFT. These effects can be largely mitigated by operating the device within the proper voltage window and by using a hydrophobic semiconductor.\cite{17, 18}

Here the difference between an increase in trap density and trap filling needs to be noted. The trap density is described by the trap density-of-states function (trap DOS) and is usually modeled as a gaussian or exponential tail extending into the bandgap.\cite{19, 20} Trap states, i.e. localized states inside the bandgap, are intrinsically present in all organic semiconductors, but the trap density can be further increased by exposure to light, moisture or oxygen, by electrical stress or by a combination of these.\cite{11, 13, 15, 21, 25} Trap states closer to the band edge are considered shallow, with trap states further inside the bandgap being considered deep traps.

Trap states can be either permanent or transient irrespective of their depth, as their lifetime depends not on the depth of the state inside the bandgap but on the formation energy of the defect acting as a trap state.\cite{24} Trap filling occurs in an OFET as the applied gate voltage moves the charge carrier quasi-Fermi level from deep inside the bandgap towards the band edge. Upon removal of the gate voltage, a trapped charge will be released after a period determined by the depth of the trap. During a transfer measurement, the gate voltage sweep rate needs to be slow enough that trap filling and release has time to occur, reaching a quasi-equilibrium.\cite{20, 26} A too fast sweep rate will lead to an increase in hysteresis, as charges being trapped (released) will retrack from (add to) the source-drain current during the on (off) sweep. In this work, trapping and de-trapping times are shown to be short, and thus we only concern ourselves with changes in the trap density in the analysis.

Poly-3-hexylthiophene (P3HT) is a benchmark semiconducting polymer, and its highly hydrophobic nature lends it well to water-gated applications. P3HT WG-TFTs have demonstrated good environmental stability, with only minor surface changes due to water exposure and a long shelf-life when protected from light and oxygen exposure.\cite{10} In the biosensor configuration, the device is operated with a gate covered by a self-assembled monolayer (SAM). Typically, the SAM contains biorecognition elements selective to the biomolecule of interest. When the specific biomolecule reaches the biorecognition element, there will be a change in the gate potential and/or its capacitance, leading to a measurable change in the source-drain voltage and the device figures of merit (FOM) - mainly the threshold voltage.\cite{3, 8, 9} Care needs to be taken during sensing measurements, as similar current changes can also be caused by changes in the semiconductor bulk or surface, by contamination of the water or by any combination of these. To ensure that the measured current change is due to the biorecognition element, intermittent measurements using a bulk gold gate without surface treatment, henceforth called the reference gate, are performed to ensure all other factors remain stable.\cite{6, 9}

In this work, we monitor a P3HT-based WG-TFT over two months and 5750 transfer cycles. Biosensing experiments are performed throughout this time, and the channel stability is continuously probed using reference gate measurements. Assessing the long-term changes in device figures of merit during normal device usage, we show that device degradation is caused mainly by electrical stress and progresses at a constant rate throughout the measurements. The shift in threshold voltage and decrease in mobility throughout the device lifetime is consistent with an increase in trap density, which we also observe using estimations from the subthreshold slope. In addition to a steady increase in trap density, we observe a steep rise in trap density during heavy usage and a partial recovery during rest, indicating the formation of two different trap species.

II. EXPERIMENT

A. Fabrication of the P3HT WG-TFT

Devices were manufactured using P3HT acquired from TCI, which at the time had the highest regioregularity commercially available ($RR > 99$% and $M_n = 27000 – 45000$). P3HT was dissolved in chlorobenzene under ambient conditions at a concentration of $4\text{ mg ml}^{-1}$. The solution was sonicated for 20 min before filtering through a $0.2\mu m$ PTFE filter. Patterned substrates were acquired from the Technical Research Centre of Finland. They consist of silicon covered by a layer of thermally grown SiO$_2$. A 5 nm thick chromium adhesion layer followed by 50 nm of gold forms interdigitated electrodes on top, illustrated in Fig. 2a along with the measurement setup in Fig. 2b. The channel is $80\mu m$ wide and $5\mu m$ long, for a $W/L$ ratio of $16160$. Substrates were ultrasonically cleaned in acetone and IPA, 10 min in each, before rinsing with DI-water. 100 µl of the semiconductor solution was deposited using spin coating in ambient air, at 2000 rpm for 30 s. Samples were annealed at 90°C for 60 min in darkness. Resistors were stored in darkness in a vacuum before measurements. In preparation for electrical measurements, 3D printed polymer water wells were fitted to the resistor using PDMS. The well can hold approximately 1 ml and was filled with HPLC-grade water for use as the gate dielectric. It is connected to a larger external reservoir to keep the water level constant during measurements. A rectangular piece of gold was used as the reference gate electrode and held vertically with a clamp.

The studied WG-TFT was one of several used for biosensing experiments. It was chosen for analysis due to mostly identical experiments being conducted throughout the device lifetime, offering the most consistency in measurement conditions.
connected and left in the well. Then, 20 transfer cycles are
alized gate is inserted into the water well next to the
After initial stabilization has been achieved, a function-
cycles until the change in current is below 2 % per hour.
more in detail, the device is stabilized using
The lack of hysteresis also indicates that
The measurements can be divided into low and high duty
The duty cycle, D, is the fraction of time an electrical
measurements. The insets in Fig. 3c and 3d show
The device lifetime. When the same measurements are
Fig. 3a shows the change in device transfer character-
A. Long-term stability analysis of a single
Fig. 3a shows the change in device transfer character-
The maximum S-D current decreases from around 45 µA to 15 µA during this time. The hysteresis in the transfer curve remains negligible throughout the measurements, and the source-drain current is three orders of magnitude larger than the gate current, both of which indicate a device operating in a proper voltage region without incurring any significant electrochemical degradation. The lack of hysteresis also indicates that trapping and de-trapping times are significantly shorter than the transfer measurement time, meaning the measurements take place in a quasi-equilibrium. The measurement protocol for sensing measurements is depicted in Fig. 3b. More in detail, the device is stabilized using the bulk gold gate and a long delay between measurement cycles until the change in current is below 2 % per hour. After initial stabilization has been achieved, a function-
alized gate is inserted into the water well next to the
reference gate. The reference gate is electrically discon-
nected and left in the well. Then, 20 transfer cycles are
recorded with a delay of 30 seconds between each mea-
surement using the functionalized gate. The functional-
ized gate is subsequently removed from the device and
incubated in the analyte for 10 min, during which time the electrical connection to the reference gate is restored and five transfer cycles are recorded with a delay of 30 seconds. This way, the stability of the channel and electrolyte can be continuously probed, ensuring that any significant change observed in device characteristics during sensing measurements is caused purely by changes to the surface of the functionalized gate. This method also enables the analysis of long-term changes in device FOM such as the threshold voltage, hole mobility, and effective trap density, as the same gold gate is used for stabilization and reference measurements throughout the device’s lifetime. Here we introduce a helpful metric to investiga-gate the effect of electrical stress on device degradation. The duty cycle, D, is the fraction of time an electrical bias is applied and is defined as
\[
D = \frac{\text{time under bias}}{\text{time under bias} + \text{time resting}}
\]
The measurements can be divided into low and high duty cycle measurements (low D and high D). The duration of a single transfer measurement is 46 seconds. During stabilization, the delay time is 30 min and gives low D ≈ 3 %. During sensing and reference measurements, the delay time is 30 s which gives a high duty cycle of D ≈ 61 %.

FIG. 2. (a) Drawing of the interdigitated source and drain electrodes with W/L = 16160. (b) Measurement setup inside the probe station showing source and drain contact probe needles, solid gold reference gate and resistor / well assembly. The external reservoir is not shown in the picture.

III. RESULTS & DISCUSSION

A. Long-term stability analysis of a single WG-TFT

The device is operated - is given by the following equation,
\[
I_D = \frac{W}{L} C_i \mu \frac{(V_G - V_{TH})^2}{2}
\]
where W and L are the width and length of the channel. The channel capacitance in similar devices has been measured to be on the order of 3 - 10 µF cm². [1] [27] [28]
Using C_i = 5 µF cm², we arrive at a mobility of around

B. Electrical measurements

Measurements were conducted under ambient condi-
tions (20 % relative humidity at 23 °C) in the dark. A Keithley 4200A SCS Parameter Analyzer and a probe station were used for all electrical measurements. A drain voltage (V_{DS}) of -0.4 V was applied while sweeping the gate voltage (V_{GS}) from +0.1 V to -0.4 V and back at a rate of 20 mV s⁻¹.
FIG. 3. (a) Evolution of the transfer and gate current over 5750 cycles from two months of biosensing measurements. The measurement protocol (b) describes a typical session of sensing measurements. The stabilization and reference measurements are performed with the same solid gold reference gate throughout the device lifetime, while sensing is performed with a single-session use gate with a functionalized gold surface. The maximum drain current measured during each stabilization (low duty, see Eq. 1) cycle and reference cycle (high duty) is presented in (c) and (d) as a function of cycle index and time, respectively. The insets show the first sensing measurement session after the initial stabilization of the device.

FIG. 4. (a) Threshold voltage $V_{TH}$ as a function of cycle index, showing a nearly linear shift over the long term. The effect of gate exposure to air manifests as faster shifting during some low $D$ measurements. (b) $C_{th}$ as a function of cycle index showing a nearly linear shift but no difference between low and high $D$ measurements. (c) $[N_{eff}/C_t]$ as a function of cycle index. The stars indicate measurements conducted after the device has been resting for at least two days. The inset highlights an example of net increase in trap states during high $D$ and a net decrease during the following low $D$ measurements.
\[ N_{\text{eff}} \approx \frac{C_i |\Delta V_{TH}|}{q} \] (4)

As we found a decrease in trap density during low \( D \) measurements, and an increase during high \( D \) measurements, there would be some delay time at which the change in trap density would be minimal. By fitting the data displayed in the inset of Fig. 4 with linear fits, assuming a bias-induced increase and time-dependent decrease in trap density, the ideal delay time for low \( D \) measurements was found to be around 5 minutes. Using this delay time, the trap density should remain stable during low \( D \) measurements, shortening the stabilization time needed when switching to high \( D \) measurements. This could improve device stability during long measurements and improve consistency between measurement days. However, the ideal delay time may vary between devices and geometries. The increase in trap density can also be approximated utilizing the shift in threshold voltage:

\[ S = \frac{k_B T \ln 10}{q} \left[ 1 + \frac{N_{\text{eff}} q^2}{C_i} \right] \] (3)

where \( N_{\text{eff}} \) is the effective trap density per unit energy and unit area, \( k_B \) is the Boltzmann constant, \( T \) is the temperature, \( q \) is the elementary charge. Using literature values for the capacitance, the trap density is on the order of \( 5 \times 10^{13} \text{eV}^{-1} \text{cm}^{-2} \), which is on the higher side of earlier reported values using the method. It is not possible to decouple the effect of any change in the capacitive coupling between the gate, electrolyte, or electrolyte-semiconductor surface from that of an increase in trap density, so we consider \( [N_{\text{eff}} C_i] \) instead. The evolution of \( [N_{\text{eff}} C_i] \) as a function of cycle index is shown in Fig. 4. The trap DOS can be determined in conventional OFETs utilizing temperature series measurements, but this is not feasible with a WG-TFT. The effective trap density used here assumes a constant trap DOS and can be considered a rough but useful estimate.

The trap density is represented by \( [N_{\text{eff}} C_i] \) in Fig. 4 and is indeed observed to increase. The increase during high \( D \) is linear with cycle index and very consistent throughout the device lifetime. This indicates gate biasing as a driver of the increasing trap density, as opposed to source-drain current; the S-D current decreases significantly towards later cycles, but the rate of increasing trap density remains the same.

During low \( D \), a net decrease in trap density is observed when high \( D \) measurements have been performed beforehand. However, when measurements are initiated after a rest period, marked with * in Fig. 3e, the trap density increases similarly to that during high \( D \) measurements. This can be explained as generation of two different trap species during operation. Shorter-lived trap states will disappear during rest periods while longer-lived ones will remain, leading to the long-term increase in trap density observed in Fig. 4 as well as the partial recovery observed during low \( D \) and rest. Generation of such metastable traps in OFETs has previously been reported by Iqbal, et al. and attributed to the formation of radical complexes involving water. By fitting an exponential decay to the instances of net de-trapping under low \( D \), the lifetime of the shorter-lived trap species was estimated to be 437 ± 225 minutes.
FIG. 6. Gate voltage shift observed after letting the device rest for 15 minutes with the gate electrode either submerged in the well or exposed to air. After exposing the gate to air, the device exhibits a significant threshold voltage shift before returning to the preceding level.

B. Short-term shift in the threshold voltage upon exposing the gate to air

A brief investigation of gate exposure to air was conducted on an identically prepared WG-TFT. The device underwent initial stabilization by cycling with a delay of 30 minutes over two days before the measurement was started. Transfer measurements were conducted before and after resting the device for 15 minutes with the gate either submerged in the well or removed and kept in air. The shift in threshold voltage as a function of time is shown in Fig. 6. After resting the device with the gate submerged in water, a negligible shift in threshold voltage can be observed, with the device remaining stable afterward. However, after the gate was exposed to air, a larger shift in threshold voltage can be observed, with a subsequent return towards the initial level. This behavior is like that observed in the previously used device when resuming measurements after storage. During storage, the gate is kept submerged in water to suppress this effect, however during reassembly of the device the gate is dried and thus exposed to air before reinsertion into the WG-TFT well. The exact mechanism of the gate potential shift upon exposure to air warrants more research but can likely be attributed to adsorption or (partial) oxidation giving rise to a shift in work function.35

IV. CONCLUSIONS

The long-term stability of a P3HT WG-TFT was analyzed over two months, during which the device was in intermittent usage, following a protocol for biosensing measurements. It was shown that the change in device figures of merit was caused by electrical stress, with time spent submerged in water having a negligible effect on the device. We show that hysteresis and gate leakage remained low throughout the measurements, with degradation manifesting as a decrease in overall current. The decrease in current was attributed to a linear shift in the threshold voltage and a linear decrease in mobility with cycle number, both of which are consistent with an increase in trap density in the semiconductor. The trap density was approximated using the subthreshold slope, showing that a net increase occurred during periods of high duty cycle measurements, with a decrease occurring during low duty cycle measurements and rest. Generated trap states consisted of a near-permanent species and a species with a lifetime of several hours. The long usable lifetime utilizing a simple geometry and commercially available semiconductor further support WG-TFTs in biosensing applications. Our investigations provide new insights into the degradation mechanisms dominating the device’s short- and long-term behavior. However, more specialized long-term measurements in conjunction with robust modeling are still needed to decouple the effects of the different device parts and fully understand the stability issues.

V. ACKNOWLEDGMENTS

Financial support from the Academy of Finland through projects #316881, #316883, and #270010; H2020 – Electronic Smart Systems – SiMBiT: Single-molecule bio-electronic smart system array for clinical testing (Grant agreement ID: 824946), and Åbo Akademi University CoE ”Bioelectronic activation of cell functions” are acknowledged.

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