Cryogenic Analysis of Junctionless Nanowire MOSFET during Underlap in Lower Technology Nodes

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1. Abstract:
This paper presents a cryogenic analysis of Junction less Underlapped Nanowire MOSFETs in lower technology nodes. The temperature dependent analysis is carried out to extract the DC figure of merits (FOMs) of the proposed nanowire MOSFET. The analysis is carried out to investigate the drain current associated with the device at different temperature. Further the analysis is extended with underlap length variation from source, drain and both sides. As the trans conductance plays a vital role in device performance estimation, so the analysis is further extended to calculate the transconductance for all the temperature variation and underlap length variation. With the introduction of gate metal under lapping, the sub-threshold behaviour of the proposed structure under different temperature is carried out extensively.

Keywords: Nano, MOSFET, Cryogenic, Underlap, Sub-threshold

2. Introduction
With an increase in the demand for portable electronic gadgets, semiconductor industry is thinking about more than Moore. Device miniaturization is no more an effective solution to bring the device into next lower technology nodes. As a result of which, different engineering techniques have introduced to bring down the scaling of the device into different level. As the device size is shrinking down to sub nanometre
regime, few unavoidable effects are affecting the device performances badly [1-4]. Although the device
dimension is scaled down using some gate engineering or channel engineering techniques, but the effect
of temperature on device performance is also an important topic of discussion. In spite of efficient
characteristics in room temperature, the semiconductor devices need a thorough analysis in higher and
lower temperature condition. Cryogenic analysis is the process of analyzing the behavior of a particular
device at very low temperature [5-8]. Ultra low temperature changes the properties of material that
instead changes the device also, which provides an interesting area for the researchers to do research.
Multi-gate devices are considered as one of the best immune to reduce short channel effects [9].
Improved electrostatic controllability with multiple gates surrounding in different axis makes the device
state of the art in semiconductor industry. Among different multi-gate devices, GAA MOSFET is
considered as the leader in multi-gate MOSFET family in lower technology nodes [10-13]. The GAA
MOSFET may be a rectangular type or cylindrical type (Nanowire), but the channel should be controlled
by the gate from all the direction. GAA MOSFET with rectangular gate or channel is less efficient than
cylindrical because of corner effect that reduces the mobility of the electron. At the same time, the
potential developed on the device is a surface phenomenon and the electric field at the centre is zero, so
the geometrical shape of the channel also affects the device performances significantly [14-16]. In case
of conventional MOSFET, the source, drain and channel are having different doping concentration [17].
As a result of which, concentration barriers will be formed and junction will be created. Fabricating
semiconductor devices with junction reduces the electron mobility and dissipates more heat as electron
or hole has to overcome the doping concentration difference barrier. Apart from this miniaturization in
MOSFET with junction takes more time and it’s more expensive as the process involves scale down of
each and every component. However in case of junctionless devices, scaling down of device in to
different technology node is easy and cost effective compared to their counter parts [18,19].
3. Device Design and Simulation:

The simulation is carried out using Sentaurus TCAD (Synopsys) [20, 21]. The simulator includes various physics based transport model for semiconductor devices in different technology nodes. Along with drift diffusion model, quantum potential based models are also there to investigate the device performance in quantum level also. In order to investigate the temperature analysis for the device in higher as well as lower temperature, thermodynamic models are also there. Apart from these, this simulator also allows some gate engineering and channel engineering techniques to study the insights of various effects associated with semiconductor devices. In this work a junctionless Nanowire MOSFET is introduced in order to analyze the effect of the temperature in various FOMs of the device if some gate engineering technique is performed. The gate metal is under lapped from source side, drain side and both side to study the device behavior. The doping concentration of the junctionless device s kept as 1e18 with a metal work function of 4.3 eV. Apart from that the dioxide used is having a thickness of 2nm which is SiO$_2$. The underlap length variation is denoted as $L_u$ and symbolized as $L_u(S)$ and $L_u(D)$ for source and drain respectively. The device dimensions of the proposed structure are given in table 1. The variation in underlap length and temperature is used to calculate the drain current at different conditions as shown in figure. Apart from this, the cryogenic analysis is carried out for a low temperature around 80K in order to have a clear insight into device performance at cryogenic.

Table 1. Device dimensions of the proposed structures
### Device Dimensions

Nano Wire MOSFET (Junction less)

|                          |                        |
|--------------------------|------------------------|
| Channel Length \((L_g/10-60)\) nm |                        |
| Doping Concentration \((N_d/N_A)\) Phosphorus \((1e+18)\)  |
| Doping Concentration \((N_d/N_A)\) Boron \((1e+18)\)          |
| Oxide Thickness \((t_{ox})\) \((2\text{nm SiO}_2)\)           |
| Channel Thickness \((t_{ch})\) \(10\text{ nm}\)                |
| Source/Drain Extensions \((L_s/L_d)\) \(20\text{ nm}\)         |
| Source/Drain Underlap \((L_{u(S)}, L_{u(D)})\) \((2,5,7)\text{ nm}\) |

4. Results and Discussion:

The analysis of the proposed device in terms of electrostatic potential and electric field distribution at a low gate bias of 0.2 V is illustrated in figure 2.

![Figure 2. Cut section of the proposed structure in no underlap condition for (a) Electrostatic potential distribution (b) Electric field distribution at a low bias of 0.2V](image)

The electrostatic potential and electric field are surface phenomenon. This can be observed from the cut section of the device shown in figure 2. From the figure, the distribution from source to drain and from outer metal gate to inner channel can be easily identified. The potential is developed at the interface of the channel and dielectric; whereas the electric field at the centre is assumed to be zero. However, the effect of drain bias can be seen near the drain side as the gate bias is very low. Figure 3(a) shows the transfer characteristics of the proposed model with source side underlap with various underlap length. With increase in underlap length, the transfer characteristic is bending down and moving away from...
saturation as a very low temperature around 100K is applied to the system. The device transfer characteristics with temperature variation are illustrated in figure 3(b). From the figure it can be observed the shape change in transfer characteristic curve at different temperature can be observed. With the increase in temperature 80K to 200K, the bending of the curve it getting more straighter and moving towards saturation.

![Figure 3. Transfer characteristics of the proposed structure (a) with source underlap (2nm, 5nm, 7nm) at a temperature of 100K (b) with different temperature (cryogenic temperature)](image)

![Figure 4. Transfer characteristics of the proposed structure (a) with drain underlap at a temperature of 100K (b) with different temperature (cryogenic temperature)](image)

The transfer characteristics for drain side underlap with different underlap length and temperature is illustrated in figure 4(a) and (b) respectively. It is observed that in case of drain side underlap the characteristics are almost same for low underlap length up to 5nm. Once the underlap length is increasing, the change in the shape of the graph is well observed as shown in figure 4(a). Similarly, the transfer characteristics with the variation of temperature from 80K to 200K are shown in figure 4(b)
which looks similar to the source side underlap. As cryogenic analysis is the temperature analysis below 135K, so the device characteristics below this temperature is having different shape as shown in figure. The analysis is further extended to both side underlap. The characteristic curve thus obtained is similar to source and drain side underlap but it is more prominent while increasing the underlap length from 2nm to 7nm as shown in figure 5(a). Similarly the transfer characteristics at different temperature for both side underlaps are illustrated in figure 5(b). From the figure, the temperature dependency of the proposed structure can be easily identified from the figure. The temperature dependent mobility of the electron defines the characteristics shape when a gate bias is applied and with low temperature, its mobility will also get affected.

Figure 5. Transfer characteristics of the proposed structure (a) with both side underlaps at a temperature of 100K (b) with different temperature (cryogenic temperature)

The work is further extended to the transconductance extraction of the proposed model with source, drain and both side underlap. The transconductance extraction for all the three cases are illustrated in figure 6,7,8 respectively. The maximum trans conductance for all the above three cases are higher in no underlap condition while reduces gradually with underlap.
Figure 6. Transconductance of the proposed structure (a) with source underlap at a temperature of 100K (b) with different temperature (cryogenic temperature)

Figure 7. Transconductance of the proposed structure (a) with drain underlap at a temperature of 100K (b) with different temperature (cryogenic temperature)
5. Conclusion:

The cryogenic analysis was carried out for the proposed junctionless nanowire MOSFET and the temperature dependency characteristics in terms of drain current and transconductance were investigated extensively. The analysis is carried out for a temperature of 80K to 200K with the underlap length variation of 2nm, 5nm and 7nm. The gate metal is under lapped for these underlap lengths and the corresponding FOMs with underlap also investigated for clear cryogenic analysis.

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