A Design of Peak to Average Power Ratio Based SWIPT System in 180 nm CMOS Process for IoT Sensor Applications

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This work was supported by the National Research and Development Program through the National Research Foundation of Korea (NRF) funded by Ministry of Science and ICT under Grant 2020M3H2A1076786.

ABSTRACT In this paper, we propose a peak-to-average-ratio (PAPR) based simultaneous wireless information and power transfer (SWIPT) system for Internet-of-Things (IoT) sensor applications. Conventional SWIPT system is based on power-hungry transmitter and receiver modules. The presence of such blocks directly impact the power consumption in IoT devices. This problem can be solved by proposing an ultra-low-power communication mechanism. Recently SWIPT with multi-tone is under consideration because of its increased power conversion efficiency (PCE). We proposed a PAPR based SWIPT receiver that utilizes the multi-tone waveform for information decoding in SWIPT system. An adaptive power splitter (APS) smartly regulates the distribution of received radio frequency (RF) signals between the energy harvesting (EH) path and the information decoding (ID) path. A digital controller was designed to control the demodulation of the PAPR based modulated signal and retrieves the digital information. Back-scattering modulation has been opted for up-link data transfer. For the EH path we design an RF-DC converter with an adaptive matching to increase the dynamic range of input power. The propose SWIPT system based on the PAPR demodulator is implemented on the 180 nm CMOS process. The digital clock frequency at the SWIPT receiver is 64 kHz, which can provide a data rate of 8 kbps with power consumption of 7.3 \( \mu \)W with area utilization of 0.4 mm\(^2\).

INDEX TERMS Energy harvesting, information decoding, multi-tone, peak to average power ratio, simultaneous wireless information and power transfer.

I. INTRODUCTION

The rapid development of 5G communication and modern devices have highly eased our lives and improved the quality-of-service (QoS). The demand of devices is increasing exponentially with advancement of the technology. But the uninterrupted and prolonged power supply is a major concern of billions of these battery-operated, low-powered Internet-of-Things (IoT) devices and sensors nodes [1], [2]. Sometimes, these sensor devices are installed at critical locations, such as the inside of any living body, or in the sensitive and hazardous environment, where recharging with conventional methods is not a viable solution [3]–[5]. These devices require an alternate source of energy instead of traditional methods like solar [6] or vibration [7]. Energy harvesting (EH) from radio frequency (RF) has emerged as a strong choice for power-limited or even battery-less nodes, without affecting data transmission. Hence wireless power transfer (WPT) has emerged as a potential solution due to its wireless power handling feature for sensors and IoT devices [8]–[11]. However, WPT has several constraints like distance, safety, high frequency needed for transmission, and initial setup cost [12]. In [13] it
is revealed that not only power but information can also be transmitted on a single waveform, which is termed as simultaneous wireless information and power transfer (SWIPT). Having a power efficient SWIPT system is challenging due to the usage of power-hungry RF and communication blocks. A non-linear circuit for efficient power distribution between information decoding (ID) path and EH path is proposed in [14], [15]. In many cases, planning SWIPT waveforms on custom communication modules is still a challenging assignment. In particular, it is vital to plan transmit waveforms such that IoT devices can handle remote data without utilizing active devices [16]. An efficient SWIPT system depends on an efficient antenna design also. Recently a hybrid coupler based antenna design was proposed in [17], [18], as well as a dual-band, dual-mode and dual-polarized wearable antenna designs are proposed in [19], [20] respectively. But our focus will be on receiver side specially information modulation and demodulation.

Recent development in efficient waveform design proposes the use of multi-tone waveforms in the EH path that is very handy in terms of power conversion, compared to the single-tone waveform [21], [22]. The sum of multi-tone waveforms generates a high peak-to-average ratio (PAPR) [23], which results in improved power conversion efficiency (PCE) at the receiver end. In the literature variety of SWIPT receiver architectures are proposed, like power splitting (PS) [25], time switching [26], and antenna switching and integrated receivers. In the TS scheme, the receiver toggles between ID and EH path based on the time period and works well when simultaneous operation is not possible due to an insufficient amount of harvested energy. On the contrary, in the PS scheme, the received RF signal is divided into two separate paths, the EH path, and ID path, with a certain splitting ratio, in order to process the received RF signal simultaneously.

SWIPT with multi-tone is created by summing frequency, amplitude, and varying the number of tones [27]. Among all proposed approaches, number of tones based modulation technique is in practice. In this method, the PAPR value of the transmitting signal is controlled by changing the tone number for summation [23], [24]. Literature shows that a higher number of tones results in higher PAPR of RF signal which results in increased rectifier’s output voltage. But, it also degrades the bit rate. It is a matter of fact that more the number of tones in limited bandwidth will eventually result in shortening of channel spacing. Having more number of tones means lower frequency spacing, and lower frequency spacing directly affects the bit rate, thus it degrades the communication quality [29]. On the contrary, lower the number of tones means higher the frequency spacing but poor will be PCE performance. Thus achieving high PCE and communication performance with the same conventional receiver hardware is quite challenging. A dual-mode SWIPT was proposed in [25], to control the communication mode and energy status of IoT devices for energy-neutral operations, which supports the dual-mode operation. Dual-mode includes single-tone and multi-tone methods for energy harvesting and communication. This is implemented on PCB having commercial devices that are not reliable for optimal operation. RFID works quite similarly to SWIPT in terms for information communication and RF energy harvesting. But the energy source in RFID is a dedicated transmitter unlike the ambient environment in SWIPT [32]–[35].

In this paper, we designed a PAPR based receiver for SWIPT system that uses multi-tone waveform for information decoding. The PAPR estimator estimates the ratio of Powerpeak and Poweravg. After recovering the data bits, a synchronization pattern is detected, which results in successful information decoding. The key contributions of this work are given as:

- A design of the SWIPT system, which utilizes the PAPR modulated multi-tone waveform, was presented.
- A PAPR based demodulator was implemented at the chip level to recover the data and validated the proposed idea through simulation and experiments.
- A digital controller was designed to control the SWIPT system operations. We verified the smooth operation of digital controller.

The rest of the paper is structured as, in section II, PAPR based SWIPT system is presented, section III presents the proposed model. Simulations and experimental results are given in section IV, and the paper is concluded in section V.

## II. PAPR BASED SWIPT SYSTEM

The concept of (SWIPT) is presented in Fig. 1. From the base station, an energy signal $x(t)$ is transmitted carrying the modulated information. The channel fading is taken ideal at the moment as ideal adaptive matching is considered. The receiver receives the signal $y(t)$ having channel and system noise $\eta(t)$. This received signal is used for both EH and ID blocks. In the SWIPT system, the transmitter’s power and modulation waveform is generated as per the requirement of the receiver. Transmitter and receiver are designed for multi-tone transmission for PAPR modulation and demodulation respectively. The PAPR maps to fine constellation points associated with every energy level. Because of the non-linear rectification process, the PCE is optimized using multi-tone waveforms. Moreover, PAPR based information transmission facilitates low-power ID using simple PAPR measurement [23]. The receiver architecture has two primary paths, the EH and ID path as shown in Fig. 1. In order to harvest energy and decode information from the same RF signal at the receiver with self-powering, an adaptive power splitter splits the RF signal with the ratio of $\theta$, where $0 \leq \theta \leq 1$. Initially, the EH path is selected to charge the super capacitor. Once enough energy is harvested for self-power up and also for energy-neutral operation, the PAPR (ID) path is selected. To meet the minimum signal-to-noise ratio (SNR) for receiver operation, it is assumed that even a small $\theta$ is sufficient. Then the EH circuit can harvest maximum signal power [25]. The received EH signal after splitting mathematically can be
The power splitter (APS) distributes the received power between the EH and PAPR (ID) blocks as the input RF signal is not fixed and received power from RF signal changes over time. The distribution of received RF power to EH and PAPR (ID) path with a splitting ratio of \( \theta \) and \( (1 - \theta) \) respectively. This adaptive logic allows the SWIPT system to cover a wide range of input power, with high PCE efficiency and decodes the information in parallel. The algorithm-1 describes the overall operation of APS.

**Algorithm 1 Adaptive Power Splitter Operation**

1: Input: \( EH, Eth, PS_{ratio}, min\_limit, max\_limit \)
2: Select max(\( PS_{ratio} \)) for maximum energy harvesting
3: if \( EH > Eth \) then
4: reduce the \( PS_{ratio} \) for information decoding
5: if \( EH < Eth \) then
6: check PS minimum limit
7: if \( PS_{ratio} = min\_limit \) then
8: maintain min\_limit and continue operation
9: else
10: return to step no. 4
11: end if
12: else
13: check the PS maximum limit
14: if \( PS_{ratio} = max\_limit \) then
15: maintain the max\_limit and continue operation
16: else
17: increase the \( PS_{ratio} \)
18: end if
19: end if
20: end if
21: return

Recent research [22] into optimal signal design for energy harvesting has found that employing a multi-toned modulation waveform can result in significant PCE gain instead of the single-tone waveform. This gain comes from the non-linear behavior of RF rectifiers which results in higher DC output with a signal of higher PAPR. However, the modulation technique used for the single-tone waveform cannot be used for multi-tone waveform [21], [22]. To address this issue, a PAPR demodulator is proposed in the SWIPT system to yield high PCE and low power consumption in the ID path. Initially, maximum power is harvested and stored in a super capacitor by the EH path. When sufficient power is accumulated in the super capacitor, then it is supplied to the PAPR (ID) path. At the low input power, a multi-tone signal results in increased PCE performance when the input power is low. While multi-tone operation, the EH path harvests energy. The PAPR path demodulates the multi-tone waveform.

### III. PROPOSED MODEL

#### A. SYSTEM ARCHITECTURE

Fig. 2 shows the block diagram of the proposed PAPR demodulator-based SWIPT system. The proposed architecture has two parts: the EH and the PAPR (ID) path. An antenna gathers information from the surrounding environment in the form of an RF signal. Antenna matching is performed with the help of a network analyzer to ensure the maximum possible power transfer from the antenna to the power splitter as the signal strength of the incoming signal varies greatly.

Based on the input power level, the designed adaptive power splitter (APS) distributes the received power between the EH and PAPR (ID) blocks as the input RF signal is not fixed and received power from RF signal changes over time. The distribution of received RF power to EH and PAPR (ID) path with a splitting ratio of \( \theta \) and \( (1 - \theta) \) respectively. This adaptive logic allows the SWIPT system to cover a wide range of input power, with high PCE efficiency and decodes the information in parallel. The algorithm-1 describes the overall operation of APS.

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An efficient design of reconfigurable RF-DC converter is given in [32]. Fig. 4 represents circuit description of one of the rectifier blocks. The rectifier circuit employs internal threshold voltage cancellation (IVC) technique for threshold voltage ($V_{th}$) compensation of the transistor used as rectifying devices. The main rectification body is composed of one NMOS transistor and two PMOS transistors. An auxiliary block is made-up of two PMOS transistors. Fig. 3(a) shows the positive phase of input power. The back compensated transistor reduces $V_{th}$ of the forward-biased transistors and increase harvested power in the main rectification chain. Fig. 3(b) shows the negative phase of input power, the rectifying devices are reversed-biased. This reduces source-gate voltages to zero, consequently minimizes the leakage current in the rectification chain. The output of DC-DC boost converter is given to LDO in order to keep constant output voltage. A super capacitor is connected at the output of the LDO to store energy and provides power for the ID path. Self-power and energy-neutral operations in the SWIPT system is very essential to provide power to the ID transceiver through the EH receiver but this task is very challenging. Energy harvested through the EH path is small as compared to the energy required for the continuous operations of the device, especially in battery-less applications. To overcome this situation, two modes of device operation was designed: energy harvesting mode and active mode. In the harvested energy mode, the SWIPT system will continue its normal communication operation, and when the store energy drops below the operation threshold voltage, the ID path is disabled and SWIPT system is switched to the harvesting mode.
these two modes. A higher ambient energy from the RF signal indicates a faster charging of the super-capacitor, thus allows more energy harvest in active mode. This will shorten the time taken by the SWIPT system in energy harvesting mode, when the voltage across the super capacitor falls below the operation threshold voltage. As a result, the device’s total switching frequency between two modes is reduced.

In order to reduce mode-switching, the quantity of energy required for device operation is also crucial. When the necessary energy rises, the super capacitor is quickly discharged, causing the SWIPT system to switch to the harvesting mode. Devices that require a very small amount of energy to operate take relatively small energy from the super capacitor. The device can function continuously without switching to the harvesting mode if the quantity of energy required for device operation is less than or equal to the amount of energy harvested. The sensitivity of proposed system is $-5$ dBm, and the measured peak power efficiency of the energy harvesting system is 69%.

C. PAPR (ID) PATH

The current research still lacks in achieving higher harvesting efficiency while using RF signal of higher PAPR. There have been attempts to design modulation specific schemes, particularly multi-tone based excitation and nonlinear signal amplification in order to enhance the SWIPT efficiency [28]–[32]. Conventional communication design is being used to transfer the information in SWIPT system like OFDM, QAM, QPSK, etc., and such communication designs are not optimized for higher energy harvesting in the SWIPT system. PAPR based SWIPT system provides a simple and efficient way to transmit/receive information. Digital information is modulated on a multi-tone waveform having different PAPR values. At the receiver end PAPR values are calculated for each symbol and digital information is retrieved using the lookup table.

Fig. 4 depicts the proposed PAPR demodulator. The peak power ($Power_{peak}$) and average power ($Power_{avg}$) must be calculated to obtain the PAPR, for which two dedicated modules were designed. The switching between $Power_{peak}$ calculation and $Power_{avg}$ calculation is controlled through a mux. Initially, $Power_{peak}$ is selected by default. The PAPR values of the symbol can be calculated as:

$$PAPR_{symbol} = \frac{PeakPower_{symbol}}{AveragePower_{symbol}}$$

The finite-state machine-based digital controller controls the overall operation of the SWIPT receiver. The selection of analog-to-digital converter (ADC) reference voltage for both peak selection and average selections are adaptive. The digital controller controls the switching of mux logic to ADC control. Different PAPR values can be produced for a given number of tones and the variation in each tone yields a specific PAPR value. Estimation is done for modulation order that is required to obtain to communication rate. In order to communicate, the SWIPT transmitter and receiver need to be synchronized. A synchronization sequence frame (SSF) is initiated from the SWIP transmitter to receiver. SSF consists of a preamble, SYNC, data frame (byte1, byte 2), and cyclic redundancy check (CRC). The frame format is given in Fig. 5. The overall flow of the PAPR demodulator is given in algorithm 2. As the RF signal arrives from APS to ID path,
the PAPR demodulator calculates the Peak value and average value respectively, and switching is done through mux logic controller, once peak and average values are determined from RF signal, PAPR estimator ratio is calculated from the peak and average values. Estimated value is provided to corresponding PAPR symbol. Digital symbol values are extracted based on the PAPR lookup table, and then the algorithm checks that whether bits are recovered, if not the algorithm again starts form selecting peak and average values. If bits are recovered than SYNC is detected, after successfully detection of SYNC, data frames are extracted and final information is recovered.

Algorithm 2 Data Extraction From Received RF Signal

1: Input: RF Signal
2: Acquire $P_{\text{peak}}$ & $P_{\text{avg}}$ signals value from ADC and mux configuring
3: Estimate $P_{\text{APPR}}$
4: Map $P_{\text{APPR}}$ → data symbol through LUT
5: Convert data symbol → bit stream
6: if no. of bits > frame size then
7: search preamble pattern
8: if valid preamble pattern then
9: detect SYNC pattern
10: if valid SYNC then
11: extract data frame
12: return to step no. 2
13: end if
14: else
15: return to step no. 2
16: end if
17: else
18: return to step no. 2
19: end if

D. BACK-SCATTERING MODULATION

The uplink communication between transmitter and receiver is handled using back-scattering modulation. In case of limited power for transceiver operations, a back-scatter modulated signal is sent to the receiver. The power management and digital controller modules control the switching operation which diverts the antenna output to carry out modulation. Since back-scattering modulation doesn’t involve any oscillator hence power consumption is comparatively very low.

IV. SIMULATION AND EXPERIMENTAL RESULTS

The chip micro-photograph of the proposed PAPR based SWIPT system is shown in Fig. 6. The chip is implemented and fabricated in 180 nm CMOS technology with a die area of 675 $\mu$m × 600 $\mu$m. It consists of a DC-DC boost converter, an RF boost converter, an RF switch, LDO,
power management unit (PMU), serial peripheral interface (SPI), PAPR estimator, decoder, digital controller, and back-scattering blocks. The PAPR based SWIPT system consumes 7.3 µW. Fig. 7 presents the measurement environment created for measuring the actual design unit. The PAPR modulated RF signal is generated through a vector signal generator. In which multiple tones can be combined to generate the required PAPR waveform. A network analyzer is used for impedance matching between antenna and chip input. PAPR decoded information and SWIPT system control registers can be accessed by PC through the SPI interface. The RF signal is received by both EH and PAPR (ID) paths through APS. The harvested energy is stored on the super capacitor, which is used to power up the PAPR (ID) path.

Fig. 8 shows the performance measurement of RF-DC converter at different number of tones. It shows that PCE measured against the RF input power with respect to number of tones. For low power, all tones performs almost similarly in terms of PCE. As the input power increases the multi-tone performance increases. The breakeven point is observed at -3 dBm input power level among all tones. The achieved throughput of our proposed design is 2 bit/sec/Hz as compared to [31] for 4 number of tones is 50 bit/s/Hz. However the rectifier output voltage in [31] at 0 dBm is 0.57 V as compared to 0.68 V which is achieved in our proposed design.

The simulated result of PAPR based modulate data frame and its counter demodulated data at receiver end is shown Fig. 9. Fig. 10 shows the relation between the multi-tone and harvested DC power. The higher the number of tones, the more the harvested DC power. The communication pattern is implemented and verified in Verilog HDL. Fig. 11 show the PCE and data rate versus PS ratio at different input power levels power.
TABLE 1. Performance comparison summary with SWIPT system.

| Parameters          | TIE2016[34] | Sensors2019[25] | TIE2020[29] | Sensors2021[30] | This Paper |
|---------------------|-------------|----------------|-------------|----------------|------------|
| Technology (nm)     | 180         | PCB            | 180         | 180            | 180        |
| Architecture        | RFID        | SWIPT          | RFID        | SWIPT          | SWIPT      |
| Energy Source       | RF/Battery  | RF             | RF/VL       | Ambient RF     | RF         |
| Power uW            | 66.3        | NA             | 64          | 123@2MHz       | 7.3        |
| Area mm²            | 1.1         | NA             | 2.4         | 0.067          | 0.4        |
| Data Rate (kbps)    | NA          | 1000-4000      | 40          | 8-500          | 8          |
| Clock Frequency (MHz)| 0.032      | NA             | 1.92        | 0.032-2        | 0.064      |
| RF Frequency (MHz)  | 560-930     | 900            | 902-928     | 5800           | 900        |
| Downlink Modulation | ASK         | ASK/BPSK/PAPR  | ASK         | ASK            | PAPR       |
| Uplink Modulation   | Back-Scattering | Back-Scattering | Back-Scattering | Back-Scattering | Back-Scattering |

V. CONCLUSION

In this paper, a PAPR based SWIPT system is presented for sensor applications. Since the SWIPT system is different
REFERENCES

[1] I. Tomkos, D. Klonidis, E. Pikasis, and S. Theodoridis, “Toward the 6G network era: Opportunities and challenges,” IT Prof., vol. 22, no. 1, pp. 34–38, Jan. 2020, doi: 10.1109/MITP.2019.2963491.

[2] M. Z. Chaari and S. Al-maadeed, “Wireless power transmission for the Internet of Things (IoT),” in Proc. IEEE Int. Conf. Infor., IoT, Enabling Technol. (ICIoT), Feb. 2020, pp. 549–554, doi: 10.1109/ICITAE69969.2020.9089547.

[3] L. Hou and S. Tan, “A preliminary study of thermal energy harvesting for industrial wireless sensor networks,” in Proc. 10th Int. Conf. Sens. Technol. (ICST), Nov. 2016, pp. 1–5, doi: 10.1109/ICST-SMT.2016.7796283.

[4] E. Boshkovska, D. W. K. Ng, N. Zlatanov, and R. Schober, “Practical peak-to-average power ratios for SWIPT,” in Proc. IEEE 33rd Annu. IEEE Power Electron. Spec. Conf., Jun. 2021, pp. 6322–6323, doi: 10.1109/PESC.2021.6021284.

[5] D. I. Kim, J. H. Moon, and J. J. Park, “New SWIPT using PAPR: How it works,” IEEE Wireless Commun., Vol. 5, no. 6, pp. 672–675, Dec. 2016, doi: 10.1109/LWC.2016.2614665.

[6] J. J. Park, J. H. Moon, K.-Y. Lee, and D. I. Kim, “Dual mode SWIPT: Waveform design and transceiver architecture with adaptive mode switch- ing,” in Proc. IEEE Veh. Technol. Conf. (VTC Spring), Jun. 2018, pp. 1–5, doi: 10.1109/VTCSpring.2018.8417661.

[7] H. Abbasizadeh, S. Y. Kim, B. S. Rikan, A. Hejazi, D. Khan, Y. G. Pu, K. C. Hwang, Y. Yang, D. I. Kim, and K.-Y. Lee, “Design of a 900 MHz dual-mode SWIPT for low-power IoT devices,” Sensors, vol. 19, no. 21, pp. 4676, Oct. 2019.

[8] M. Wagih, G. S. Hilton, A. S. Weddell, and S. Beeby, “Dual-polarized wearable antenna/rectenna for full-duplex and MIMO simultaneous wireless information and power transfer (SWIPT),” IEEE Trans. Antennas Propag., vol. 69, no. 10, pp. 6322–6332, Oct. 2021, doi: 10.1109/TAP.2020.3070230.

[9] Y. Qiu, C. Van Liempd, B. O. het Veld, P. G. Blanken, and C. Van Hoof, “Micropower energy harvesting,” in Proc. IEEE Int. Symp. Ind. Electron. Spec. Conf., Aug. 2012, pp. 684–689, doi: 10.1109/ISIE.2012.6329510.

[10] S. Claessens, N. Pan, D. Schreurs, and S. Pollin, “Enhanced biased ASK modulation performance for SWIPT with AWGN channel and dual-purpose hardware,” IEEE Trans. Microw. Theory Tech., vol. 66, no. 7, pp. 3478–3486, Jul. 2018, doi: 10.1109/TMTT.2018.2829515.

[11] L. Liu, R. Zhang, and K.-C. Chua, “Wireless information and power transfer: Architecture design and rate-energy tradeoff,” IEEE Trans. Commun., vol. 61, no. 9, pp. 3990–4001, Sep. 2013, doi: 10.1109/TCOMM.2013.071813.130105.

[12] X. Zhou, R. Zhang, and C. K. Ho, “Wireless information and power transfer: Architecture design and rate-energy tradeoff,” IEEE Trans. Microw. Theory Tech., vol. 61, no. 11, pp. 4754–4767, Nov. 2013, doi: 10.1109/TMTT.2013.1280855.

[13] C. Im, J.-W. Lee, and C. Lee, “A multi-tone amplitude modulation scheme for wireless information and power transfer,” IEEE Trans. Veh. Technol., vol. 69, no. 1, pp. 1147–1151, Jan. 2020, doi: 10.1109/TVT.2019.2954860.

[14] M. R. U. Rehman, I. Ali, D. Khan, M. Asif, P. Kumar, S. J. Oh, Y. G. Pu, S. J. Oh, K. C. Hwang, Y. Yang, D. I. Kim, and K.-Y. Lee, “A design of adaptive control and communication protocol for SWIPT system in 180 nm CMOS process for sensor applications,” Sensors, vol. 21, no. 3, p. 848, Jan. 2021.

[15] S. Claessens, N. Pan, D. Schreurs, and S. Pollin, “Multitone FSK modulation for SWIPT,” IEEE Trans. Microw. Theory Tech., vol. 67, no. 5, pp. 1665–1674, May 2019, doi: 10.1109/TMTT.2019.2908645.

[16] S. K. Oh, S. J. Oh, K. Shehroz, M. Basim, D. Lee, Y. G. Pu, M. Lee, K. C. Hwang, Y. Yang, and K.-Y. Lee, “An efficient reconfigurable RF-DC converter with wide input power range for RF energy harvesting,” IEEE Access, vol. 8, pp. 79310–79318, 2020, doi: 10.1109/ACCESS.2020.2990662.

[17] A. U. Din, J. H. Lee, N. X. Hieu, and J. W. Lee, “Dual-mode RFID tag IC supporting gen-2 and visible RFID modes using a process-compensating self-calibrating clock generator,” IEEE Trans. Ind. Electron., vol. 67, no. 1, pp. 569–580, Jan. 2020, doi: 10.1109/TIE.2019.2989678.
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