Structure and electrical behavior of silicon nanowires prepared by MACE process

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Abstract

We report on the structure and electrical characteristics of silicon nanowire arrays prepared by metal assisted chemical etching (MACE) method, investigated by cross-sectional scanning electron microscopy (SEM) and high resolution X-ray diffraction (HR-XRD) methods. SEM micrographs show arrays of merged parallel nanowires, with lengths of 700 nm and 1000 nm, resulted after 1.5 min and 5 min etching time, respectively. X-ray reciprocal space maps (RSMs) around Si (004) reciprocal lattice point indicate the presence of 0D structural defects rather than of extended defects. The photoluminescence spectra exhibit emission bands at 1.70 eV and 1.61 eV, with intensity significantly higher in the case of longer wires and associated with the more defected surface. The transient photoluminescence spectroscopy reveals average lifetime of 60 µs and 111 µs for the two SiNW arrays, which correlate with a larger density of defects states in the latest case. The I-V characteristics of the nanowires, show a memristive behavior with the applied voltage sweep rate in the range 5V/s - 0.32V/s. We attribute this behavior to trap states which control the carrier concentration, and model this effect using an equivalent circuit. Photogeneration processes under excitation wavelengths in visible domain, 405 nm - 650 nm, and under light intensity in the range 20 - 100 mW/cm² provided a further insight into the trap states.

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I. INTRODUCTION

Silicon nanowire (SiNW) arrays with controlled morphology (porosity, length, orientation) have been efficiently prepared by metal assisted chemical etching (MACE) processing [1][2], aiming to widen their applicability to performant light emitting devices, photodetectors, energy storage and conversion, or sensors [4][5]. Yet, defective surfaces of SiNWs resulting from chemical-assisted preparation processes can affect the electric parameters of the devices [7][8].

The dynamic hysteresis of the electrical characteristics of a nano-electronic device when the applied voltage changes in time is one of the first indications of the presence of a charge trapping mechanism inside the devices with a relaxation time comparable to the time of the voltage variation. This phenomenon is used in memristive device, often based on metallic nanowires [9], but also on silicon nanowires [10][11]. Sensing devices based on SiNWs have also been proposed, where the dynamic occupation of the nanowire surface states created by the external charges from the adsorbed biomolecules modify the hysteresis loop [12]. Or field effect transistors where the nanowires are in contact with a dielectric, or polymer [13].

The electrical hysteresis is also present in solar cells based on perovskite materials, and associated to the degradation of the cell, due to ionic migration, charge accumulation at interfaces, and their influence on the photogenerated current [14][15][16]. Apart of the possible hysteretic effects, the surface states of SiNWs are also important for the characteristics of nanostructured solar cells, where the electrons trapped by surface states can act as a gate bias that enhances the photoconductivity [17][19].

In this work we report on the electrical response of Al/SiNWs/Al device structures with pristine SiNW arrays prepared by the MACE method. The nanowires are highly imperfect and in lateral contact to each other, forming a system of inter-connected wires rather than independent wires. The current-voltage (I-V) and capacitance-voltage (C-V) curves, measured in dark and under various illumination conditions in terms of wavelengths and intensity, are analyzed using an equivalent circuit with lump elements. The model, although simplistic, is able to reproduce satisfactorily the normal and inverted hysteresis observed in the I-V curves. We suggest that the intimate mechanism accounting for the hysteresis may be related to the effect of charge carrier trapping and detrapping at the surface states present in the pristine SiNW arrays. We show that traps filling by tuning the light wavelength may be used as a method to determine their origin and electronic properties.

II. EXPERIMENTAL

Inter-connected silicon nanowire arrays have been fabricated via metal-assisted chemical etching (MACE) as shown in the flow chart presented in Fig. 1. Single-sided polished samples (1 × 1 cm²) cut from (100) oriented silicon wafers (p-type, with resistivity of 1 – 10 Ω·cm and thickness of 625 µm) were used in the process. The samples were cleaned with acetone, methanol, isopropanol, and deionized water followed by drying in N² gas flow, then treated with HF:H₂O (1:3) solution for 3 min to remove the native oxide. To obtain the SiNW arrays, the polished side of the samples were coated with Ag nanoparticles by immersing them in HF [3 M]:AgNO₃ [1.5 mM] solution for 1 min. The coated samples were then cleaned with DI-water to remove the excess of Ag nanoparticles. The samples subsequently underwent etching process by immersing them in an etching solution of HF [5 M]:H₂O₂[0.4 M] for 1.5 min and 5 min, respectively, followed by immersion in H₂O:HNO₃ (3:1) to remove residual
FIG. 1: Schematic illustration of the MACE steps for SiNWs preparation and Al/SiNWs/Al structures fabrication.

Ag nanoparticles. Finally, the samples were cleaned with DI-water, then dried with N₂ gas. For electrical measurements, two coplanar Al contacts, 2×10 mm² each, with the thickness of 150 nm were deposited on the surface of the samples via a hard mask. The distance between the two contacts is 6 mm. Contacts deposition was made by using an electron beam evaporator (Polyteknik Cryofox Explorer 600 LT).

Micrographs of the SiNWs were recorded on the top and at a tilt angle to observe the in-depths of the structures, by using a field emission scanning electron microscope (FE-SEM), FEI NovaTM NanoSEM 630. The structural characteristics of the SiNW arrays were investigated by using a SmartLab X-ray diffraction system from Rigaku Corp. (Osaka, Japan). X-ray reciprocal space maps (RSMs) around Si (004) reciprocal lattice point were recorded in triple-axis configuration (ultra-high resolution) with a four-bounce Ge monochromator with two reflections at incidence and a two-bounce Ge monochromator with two reflections in the front of detector. Bending profiles were obtained using grazing-incidence XRD in asymmetric skew geometry on (111) reflection. In this configuration, the incidence angle of the source was varied from 0.5° to 4° to obtain different X-ray penetration depth.

The photoluminescence (PL) emission spectra of the SiNW arrays were recorded with an Edinburgh FL920 fluorescence spectrophotometer equipped with microsecond flashlamp as an excitation source. Time-correlated single photon counting (TCSPC) technique was used to determine the photoluminescence lifetime, using excitation at 300 nm and recording the emission at 770 nm wavelength. FAST Version 3.4.2. Edinburgh Instruments Ltd software was used for experimental fit.

The I-V and C-V characteristics were measured using a Keithley 2400 and SCS 4200 Keithley system, in dark and under light illumination with various wavelengths, as well as under white light using a solar simulation lamp, with intensities in the range 20-100 mW/cm². The curves were recorded by forward and reverse sweeping the applied voltage in the range -10V to +10V.
FIG. 2: SEM micrographs of the SiNWs arrays prepared by a MACE process. The etching time was: (a), (b) 1.5 min and (c), (d) 5 min.

III. RESULTS

A. Structure and PL properties of silicon nanowires

The top and cross-sectional SEM micrographs of the SiNW arrays obtained at 1.5 min and 5 min etching time, are shown in Fig. 2a-d. The length of the NWs is about 700 nm after 1.5 min etching (see Figs. 2a-b) and 1000 nm after 5 min etching (Figs. 2c-d). In the following we refer to these two samples as SiNW$_{short}$ and SiNW$_{long}$, respectively. There is a saturation value so that the lengths of the wires are limited with the respect of the concentrations of the oxidizing agent H$_2$O$_2$, AgNO$_3$ concentration, and specific resistivity ($\rho$) of bulk Si [20]. As seen, the wires are laterally interconnected and form continuous structures of walls in both arrays. According to ImageJ analysis, the coverage area is 36% and 32% for SiNW$_{short}$ and SiNW$_{long}$, respectively, which suggests that the longer etching time leads to a higher porosity. Note that the coverage area means the surface occupied by tips of SiNWs observed in SEM top view image and by longer etching time the diameter of SiNWs decreases and as result the coverage area decreases. In order to investigate the microstructural features of the nanowire arrays, we performed X-ray diffraction in high resolution setup. X-ray reciprocal space maps (RSMs) around Si (004) reciprocal lattice point give information regarding the out-of-plane lattice value, relative lattice strain and the crystal imperfections. X-ray RSMs along ($q_z$, $q_x$) coordinates for SiNW$_{short}$ and SiNW$_{long}$ arrays are presented in Figs. 3a,b. The reciprocal space coordinates $q_x$ and $q_z$ are projections of the scattering vector along
FIG. 3: X-ray reciprocal space maps (RSMs) recorded near Si (004) reciprocal lattice point on the nanowire arrays with length of (a) 700 nm and (b) 1000 nm SiNWs.

[100] and [001] directions, respectively, and are related with the angular coordinates as:

\[ q_x = \frac{2 \sin (\omega - \theta)}{\lambda} \] and \[ q_z = \frac{2 \sin \theta}{\lambda}. \]

The X-ray reciprocal space maps present an intense peak located around \( q_z \in (0.7360 - 0.7365) \, \text{Å}^{-1} \). Using the crystallographic relations for cubic crystals, the lattice constant \( a \) can be expressed as \( \frac{4}{q_z} \) \cite{21}, giving a lattice constant equal to 5.43 Å, which corresponds to the lattice parameter of bulk Si. This is an indication that the MACE process does not affect the value of the lattice parameter of the samples. Further, it can be observed that the spot broadening increases with increasing the nanowire length in both \( q_z \) and \( q_x \) direction. The broadening of the RSM spot can be ascribed to the occurrence of bending and torsion of nanowire array, which is more pronounced for the longer (1000 nm) SiNWs, due to a higher surface energy. At the same time, the X-ray scattering in the reciprocal space looks different. For instance, the area elongated along \( q_x \), which is related to the diffuse scattering, could be determined by crystal imperfections (e.g. point defects, extended defects, or stacking faults), and broader angular dispersion is observed for the longer nanowires. The cross section of intensity distribution of our RSM along \( q_x \) is presented below in Fig. 4a.

The X-ray rocking curves indicate two types of scattering: (1) the narrow peak is related to the specular scattering (\( I_{\text{spec}} \)), also called Bragg scattering, where the X-ray scattering has taken place on the atomic planes; (2) the broad feature indicates the presence of the
FIG. 4: Cross section of intensity distribution along $q_x$ direction for short and long nanowire arrays (a) and (b) bending profiles.

X-ray diffuse scattering (XDRS), further denoted as $I_{\text{diff}}$. This scattering is determined by the structural imperfections in the Si lattice. To have a qualitative description of the X-ray scattering, we obtain the ratio between $I_{\text{diff}}/(I_{\text{diff}} + I_{\text{spec}})$. For instance, the shorter SiNWs exhibit a ratio of 0.31, whereas the longer SiNWs exhibit ratio of 0.94. Clearly, this ratio can be viewed as a measure of the structural defect density in our samples. It is reasonable to assume that the longer SiNWs possesses a higher density of the structural defects, being promoted by the strain relaxation processes due to the bending and torsion phenomena [22].

To prove the existence or absence of the strain relaxation processes, we obtained bending profiles of our samples, which correspond to the average tilt of the arrays - Figure 4b. These profiles were obtained in the framework of grazing-incidence X-ray diffraction on highly-asymmetric (111) reflection, which allowed us to attain different X-ray penetration depths, varying the incidence angles of the X-ray source. Further details regarding the grazing-incidence X-ray diffraction technique on (111) in nanowires, as well as for the bending profiles can be found in [23].

The evolution of the FWHM of the X-ray spectra with the incidence angle gives the tilt of nanowire array at different penetration depths. One may observe that the shorter nanowires determine a smaller tilt, e.g. $0.028^\circ$, comparing to the longer ones which have an average tilt of $0.037^\circ$. It is clear that the higher tilt for the longer nanowires is determined by a higher surface energy of the nanowire array. However, for both samples the bending profiles do not present dips, whose occurrence can be assigned to a quasi-local manifestation of some relaxation mechanisms in the nanowires. The absence of the strain relaxation processes can be further attributed to the absence of the extended structural defects, such as edge and screw threading dislocations. This is possible by taking into account the small length of our arrays. Also, previous investigations in highly dense nanowire arrays prepared by MACE showed the occurrence of edge and screw threading dislocations only for wires longer than 9 µm [23]. At the same time, we must consider the previous findings from the rocking curves profiles, indicating a relationship between the array length and the XRDS intensity, which was attributed to the presence of the structural defects.

The XRD findings indicate that the MACE process has determined the formation of 0D
FIG. 5: PL spectra of SiNWs arrays under excitation with Xe lamp at wavelength of 350 nm and 450 W power.

defects, nanocrystals or nanopores on the surface of SiNWs, rather than extended structural defects. The nature of structural defects is analyzed by recording the photoluminescence (PL) emission from SiNWs arrays. The PL spectra are shown in Fig. 5.

The SiNW_short presents a rather weak PL intensity, about 1/15 of the PL for the SiNW_long. The spectrum is centered at 730 nm (1.70 eV). Sample SiNW_long shows an intense and broad PL emission spectra in the VIS-NIR region, centered at 770 nm (1.61 eV). The red-shift in energy of 80 meV of the PL maximum position, observed for the longer NWs, could be related to the structure of interconnected skeletons and increased porosity, as resulted during the MACE process with a longer duration [20]. The observed red-shift with longer etching time is in agreement with our previous results [20]. It has however worth noting that others researchers [24], have observed blue-shift upon increasing etching time and correlated that with the presence of SiO_x. It appears that in our case, the SiO_x fraction is not increasing with the etching time and consequently has a low contribution to the PL emission which strongly shifts towards NIR spectral range. A slow (S) band in the red-yellow spectral range with long microsecond decay times is reported and analyzed in porous silicon nanostructures PL spectra and attributed to phonon-assisted exciton recombination within the silicon nanostructure [25]. It was also reported that TEM images of the luminescent SiNWs prepared by MACE technique reveal that the surfaces of the SiNWs are very rough, with a few nano-sized silicon particles being attached to the SiNWs. The PL spectrum of such SiNWs was peaked at 700 nm for an excitation wavelength of 400 nm [26].

Lin et al. [27] reported that SiNWs synthesized via MACE exhibit a nanoporous structure. The PL emission band in the red region, at 730 nm was attributed to the excitons captured by the interface states between the Si nanostructures and the native oxide layer. The PL intensity increases with the porosity [27]. It was also reported that longer etching time, or higher H_2O_2 concentration could facilitate the diffusion and nucleation of Ag
ions and effectively enhance the porosity of the nanowires \[28\]. Recently, it was shown that MACE-produced SiNW arrays are covered with porous structures, silicon nanocrystals, which result from the lateral etching of NWs sidewalls. The broad PL spectrum centered at 695 nm (1.78 eV) is attributed to radiative recombination of excitons in these nanocrystals \[29\]. In our experiment, even if the length of the NWs does not differ very much, the PL intensity is substantially higher in the case of long wires which suggests the formation of a larger number of luminescence centers.

The enhancement of the PL intensity and the wavelength red-shift could be attributed to enhanced porous structure of the SiNWs surface and also of a porous Si layer formed at the base of SiNWs, resulting after a longer MACE process \[30, 31\]. Previous studies reported that HF post etching treatments of SiNWs are mandatory in order to obtain light emission \[32\]. Other experiments demonstrated that H\(_2\)O\(_2\) could favor PL emission, which is attributed to SiO\(_2\) layer formation on the NWs surface \[24\]. However, in this work a different etching process in terms of reagents concentration leads to a significant intensity of the PL emission, without any post-treatment, as also observed by reference \[33\]. This result underlines the essential role of the etching solution concentration on the formation of various light emitting centers, such as Si nanostructures, SiO\(_2\) layer, other specific Si bonding structure. The PL lifetime of the SiNWs arrays was measured by transient photoluminescence spectroscopy (TCSPC) method.

Fig. 6 shows PL emission decay curves of the SiNWs arrays obtained by using the excitation wavelength 300 nm and the emission wavelength 770 nm. The monoexponential lifetime decreases sharply for shorter SiNWs, indicating a smaller contribution of the surface disorder. Long lifetime observed for the longer SiNWs should be mostly dictated by nonradiative processes involving surface defects, in agreement with the results of XRD-RSM maps presented in Figure 3. The average lifetime obtained by fitting the experimental values
is 60 µs for the short SiNWs and 111 µs for long SiNWs. By increasing the etching time, the number of both radiative and non-radiative centers increases, however their ratio remains relatively unchanged and that determines longer luminescence lifetime coupled with stronger radiative emission.
B. Electrical characteristics of Silicon nanowires

FIG. 7: Current-voltage characteristics of Al/SiNWs/Al structures: (a)-(e) short SiNWs and (f)-(j) long SiNWs, measured at various voltage sweep rates. In dark and under illumination measurements.
The I-V curves of the Al/SiNWs/Al structures, measured at various voltage sweep rates in dark and under illumination, are presented in Figures 7 a-j. The plots are non-linear, characteristic to two diodes in antiparallel configuration, due to the Al-Si Schottky contacts. The current intensities under illumination are slightly higher compared to those measured in dark. The hysteresis observed in the I-V curves of both samples suggests that a process of trapping and de-trapping of minority (e) charge carriers, with different time constants, may take place. A dependence of the hysteresis area (in VA units) as a function of the voltage sweep rate may also be observed, see Fig. 8a,b.

In the case of the SiNW short sample the hysteresis area in quadrant 1, defined as area of the “down” curve minus the area of the “up” curve, shows a continuous decrease as the voltage sweep-rate increases, see Fig. 8a, but remains in the positive range of values. A different behavior may be observed in the case of SiNW long, as the hysteresis area takes negative values at small V rates and positive values for rates beyond 1.38 V/s, see Fig. 8b. Also, the data reveal that the hysteresis area increases under illumination for short NWs, see Fig. 8a, but exhibits an interesting evolution at sweep rates below 4 V/s in the case of long NWs, Fig. 8b. Additional results obtained on SiNW arrays with lengths larger than 1000 nm and exhibiting different morphologies are shown in the Supplementary Material, Fig. A2, where it has been observed that post-treated SiNWs with HF shows minimum hysteresis and confirm that surface defect-free nanowires can be prepared by MACE using an HF post-treatment. This result is in good agreement with Choi et al [34]. It is worth noting that the untreated bulk Si shows no hysteresis and confirms the larger defective surface area of SiNWs is associated with charge trapping and hysteresis effect. The corresponding plot is shown in Supplementary Material, Fig. A3. As apparent, the extend of the hysteresis is not related with etching time in the range tested (2-10 min).

IV. MODELING THE I-V CHARACTERISTICS

We consider an equivalent electrical circuit of the Si/SiNWs/Al structures to model the observed memristive behavior of measured I-V curves. The memristive effect consists in the dependence of the I-V curve, and consequently of the electrical resistance of the device, on the history of the applied voltage, i.e. increasing or decreasing [9]. I-V hysteresis loops for
FIG. 9: A simple circuit model for the I-V characteristic with hysteresis. The direction of the current depends on the polarity of the main voltage $V(t)$.

Multiple cycles are shown in the Supplementary Material, Fig. A1. The I-V experimental data show exponential-like dependencies, and a difference between the current “up”, $I_{\text{up}}$, i.e. when the voltage increases, and the current “down” $I_{\text{down}}$, i.e. when the voltage decreases. A simple model to account for this behavior should combine a resistor, two diodes, and one or two capacitors, as illustrated in Figure 9. The role of the diodes is to give the exponential-like current as a function of voltage, and the role of the $R-C$ block is to generate a voltage drop $u$ which controls the number of charge carriers passing through the circuit. The voltage $u$ corresponds to an electric field internal to the diodes, such that the currents through each diode $D_j$, ($j = 1, 2$) can be written as:

$$I_{D_j}(t) = I_j \left[ e^{\frac{q(V(t) - u(t))}{nkT}} - e^{-\frac{qu(t)}{nkT}} \right],$$ (1)

where $I_j$ and $n_j$ are diode parameters (saturation current and ideality factor, respectively), $q$ is the elementary electric charge, $k$ is Boltzmann’s constant, and $T$ the temperature. We begin by considering only one capacitor, $C_1$, and ignore the second one, i.e. $C_2 = 0$. The total current in the circuit is then:

$$I = I_{D_1} + I_{D_2} = I_R + I_{C_1},$$ (2)

where $I_R = u/R$, and $I_{C_1}$ is discussed below.

The order of magnitude of the charge associated with the capacitance $C_1$ needed to explain the experimental data can be inferred from the observed hysteresis effect. The total charge going through the circuit corresponds to the area of the current versus time, which can easily be evaluated since the voltage has a constant rate in time. For example, for the SiNW$_{\text{short}}$ sample, at a voltage rate of 0.63 V/s in dark (Figure 7d), the hysteresis area between the positive voltages 4 V and 5 V, corresponding to a time interval of 1.6 s, is 0.15 mVA, or 0.24 mAs or 0.24 mC of electric charge. This gives an estimated $C_1 \approx 0.24$ mF, which is obviously a very large value for such a small sample. A more realistic assumption is to assume a much smaller capacitance, and associate the capacitor with a trapping mechanism, which temporarily stores a relatively small amount of charge, $Q_1$, but contributes significantly to the voltage $u$, which in turn has a much larger effect on the current than the stored charge.
The capacitance is associated to a temporary polarization effect, likely due to interface states in the Schottky diodes \[35\] and/or surface states \[11, 12\]. Therefore, we assume that the current controlled by the capacitor is

\[
I_{C_1} = b \frac{dQ_1}{dt}
\]  

(3)

where \(b\) is a coefficient describing the amplification factor of the number of carriers controlled by the polarization effects associated with the charge \(Q_1\). Here Equation (3) is a simplified version of Equation (5) of Reference \[12\], where both acceptor-like and donor-like traps are considered.

Next, we denote by \(\tau_1\) the time constant associated to the relaxation of this electric or trapping charge. This relaxation process may depend on more complex phenomena, like ion displacement, diffusion, etc., which we cannot describe in detail. Instead, we define the relaxation time \(\tau_1\) via the equation

\[
\frac{dQ_1}{dt} = -\frac{Q_1(t) - C_1 u(t)}{\tau_1}
\]  

(4)

which leads to an exponentially asymptotic charging or discharging with a time factor \(e^{-t/\tau_1}\). A similar assumption has been used to explain the hysteresis phenomenon in perovskite based solar cells \[36\].

In Fig. 10 we show the calculated I-V characteristic using empirical parameters inspired by the experimental results, but also adjusted for the convenience of the numerical calculations: \(I_1 = 0.04\) mA, \(I_2 = 0.03\) mA, \(n_1 = -n_2 = 30\), \(\tau_1 = 6\) s, \(C_1 = 1.5\) nF, \(b = 10^6\), \(R = 1600\) \(\Omega\). The voltage is swept from -5 V to 5 V and back to -5 V in 50 seconds, i.e. with a rate of 0.4 V/s. The current was calculated numerically using Equations (1)-(4), by discretizing the time in small steps, with initial conditions \(Q_1 = 0\). (The current in the two diodes was obtained using the Lambert function, since the voltage \(u(t)\) implicitly depends on the current.)

The intersection of the “up” and “down” curves at negative voltages occurs because of the initial and final state of the capacitor (uncharged vs. charged). However, one feature of the hysteresis loop shown in Fig. 10 differs from the experiment. For positive voltage, the “up” curve is always above the down curve, i.e. opposite to the experimental data obtained for the sample A (700 nm). The reason is that after the voltage reached the maximum and begins to decrease, the capacitor \(C_1\) pushes current against the main current of the source, i.e. decreasing the current compared to the “up” values. This effect does not depend on the magnitude of the coefficient \(b\), but on its sign, which is positive. To match the experimental data with this simple model we need to assume a negative sign of this coefficient \(b\) for the “up” segment of the I-V characteristic, i.e. in that phase the trapping mechanism releases current with the same orientation as of the total current. The resulting I-V curves are shown in Fig. 11.

The I-V characteristic looks now qualitatively similar to the experimental data shown in Figures 7a-e. This similarity suggests a negative intrinsic polarization mechanism of the sample, during the measurements, with a relaxation time of the order of seconds. Such a situation can also be obtained in perovskite based solar cells, where the “up” and “down” currents in the hysteresis loops can be inverted, depending on the sign of the polarization of the cell \[16, 36\]. It is also seen in Fig. 7 that in presence of light the magnitude of the current increases, due to increased number of photogenerated charge carriers.
FIG. 10: The I-V characteristic with a normal current $I_{C_1}$. When the voltage $V$ decreases (along the “down” curves) $I_{C_1}$ is oriented against the source, if it is released by a normal capacitor, and consequently the total current is smaller than it was when $V$ increased (the “up” curves).

FIG. 11: The calculated I-V curves with the same parameters as in Figure 9, but negative coefficient $b$. In this case the current for positive voltage is smaller when the voltage decreases, as observed for the samples of 700 nm.

An additional feature may be observed in the I-V curves of the sample SiNW$_{long}$, where the hysteresis for positive voltage reverses with decreasing the voltage rate, see Figs. 7-f-j. An initial shoulder is visible at high rates on the “up” curve, below the “down” curve, which then moves above the “down” curves at lower voltage rates, below 1.38 V/s. For lower voltage rates the hysteresis loop becomes twisted. A possible interpretation is that in this situation another capacitor, $C_2$, is activated at a certain positive voltage, acting now in the regular manner, i.e. pumping current against the source, $I_{C_2} = b \, \frac{dQ_2}{dt}$ with the $b$ coefficient always positive. In Fig. 12 we show the results with $C_2 = 0.6$ nF. Such an example looks qualitatively similar with the data for the sample SiNW$_{long}$ shown in Figs. 7-f-j. Such a twisted hysteresis loop has been shown by Thissandier et al. [37], for an array of disconnected SiNWs, when the voltage was increased above a certain threshold.
FIG. 12: The calculated I-V curves with the same parameters as in Figure 3, plus second capacitor $C_2 = 0.6$ nF which is activated gradually between voltages 0.5 - 1 V. The current created by the second capacitor has always a positive coefficient $b$.

We emphasize that the model used for explaining the I-V curves is primitive, and only qualitative. The magnitude of the $b$ coefficient and of the capacitances have somehow a complementary character: we could increase one by decreasing the other one. However, for a small $b$ value the capacitances would be unrealistic, and for this reason we believe their role is more like a trigger for activation of more charge carriers, typical for a small polarization field inside a Schottky or a p-n diode, or for a gate inside a transistor. Since the NWs are formed in p-type Si, with resistivity of the order of 1-10 $\Omega \cdot$ cm, then shunt resistors should be included for a more realistic circuit model. Still, the development of a more complex equivalent circuit is beyond the scope of this study.

A. Capacitance behavior under illumination

The C-V characteristics of the SiNW arrays measured at various frequencies are shown in Figure 13a,b. Both structures exhibit reduced capacitance by increasing the frequency in the range 5-100 kHz, with maximum value of 9.9 nF, Figure 14a, and 3.7 nF, Figure 14b, at 5 kHz. However, the SiNW arrays with long NWs exhibit asymmetric behavior in the region of positive voltages, 0 to +10V, where large and switching hysteresis loops appear under the forward and reverse polarization. The presence of a positive or negative sign of the current due to traps, or equivalently, negative or positive capacitance, as proposed in the equivalent circuit, could explain the observed behavior.

Next we show the C-V characteristics measured under illumination with various wavelengths, in Fig. 14a,b. The capacitance of the structure with short NWs slightly increased when the structure is illuminated at 650 nm and 532 nm wavelength, Fig. 14a, while the structure with long NWs exhibits a significantly reduced capacitance under illumination at these wavelengths, Fig. 14b, likely due to the effect of photogenerated carries trapped at the surface states, lowering the value of the capacitive reactance. Fig. 14b also shows the capacitance changing slightly under illumination with 450 nm or 405 nm wavelength. In this case the photogenerated carriers behave like free carriers and determine the increase of the current intensity, see I-V characteristics in Fig. 7.
Fig. 13 shows the C-V characteristics under illumination with white light, with various intensities. Both structures exhibit higher capacitance when the light intensity increases, reaching 26 nF for the structure with short NWs, Fig. 15a, and 1.6 nF for SiNWs with long NWs, Fig. 15b, under illumination with 100 mW/cm². All the C-V curves present hysteresis, noticeable under positive applied voltage, 0/+10 V. The structure with long NWs shows also a supplementary capacitance peak at positive applied voltage, that increases with the intensity of light. Also, the occurrence voltage shifts towards higher values, from 1.82 V to 2.16 V with increased light intensity.
V. DISCUSSION AND CONCLUSIONS

The analysis of hysteresis exhibited by the I-V characteristics shown in Figs. 7a-e, reveals that charge carriers are trapped on the surface states in sample SiNW\textsubscript{short}, with PL average lifetime of 60 $\mu$s, when the voltage sweep rate varies from 5 V/s to 0.32 V/s. The hysteresis area linearly increases by lowering the sweep rate, see Fig. 8a, which suggests that the slow traps are involved in the process. The situation changes for the SiNW\textsubscript{long} sample, with PL average lifetime of 111 $\mu$s, where larger hysteresis areas appear at faster voltage sweep rates, Figs. 7f-j. In fact, as the variation of the hysteresis area vs voltage sweep rate presented in Fig. 8a,b suggests, at slow V rates, of 0.32 V/s and 0.63 V/s, the slow traps act in the both structures. Also, since faster voltage sweeps are required to activate the fast surface states, the evolution of the hysteresis area in Figure 8b indicates the presence of fast surface traps in the SiNW\textsubscript{long} sample. The I-V hysteresis in SiNWs prepared by MACE has also been obtained in Ref. [6], but the dependence on the voltage rate has not been reported. The presence of the traps in the SiNWs can also be inferred from the non-ideal diode characteristic of the Schottky contacts, observed in the I-V characteristic [38].

The C-V response of this structure to excitation with various wavelengths suggests the presence of electron traps active at energy below 2.4 eV (observed in C-V responses at 1.9 eV and 2.33 eV irradiation), which are within the band gap of porous silicon [39–41]. Although these band gap values are also within the (broad) emission band limits observed in Fig. 5, they are different than the values derived from the maxima in the PL emission spectra, centered at 1.70 eV for SiNW\textsubscript{short} and 1.61 eV for SiNW\textsubscript{long}, suggesting that different trap centers are involved in the PL emission and photogeneration processes.

In summary, the evolution of I-V hysteresis vs applied voltage rates was used to assess the effect of surface traps on transport properties of the pristine SiNWs arrays. The transition from an inverted to a direct hysteresis is demonstrated considering the effect of a capacitance associated with the surface traps which controls the charge current through the structure. The I-V and C-V characteristics measured under illumination with various wavelengths in the visible domain indicate that traps filling can be detected by tuning the photons energy. Using this method we assessed the energy range of the surface trap states energy of a SiNWs array.
However, the characterization methods used in this work, including PL, I-V and CV, bring evidence on effects due to the presence of surface states, but hardly allow an accurate assignment of their energy to a specific defect or complex. First, taking into account that different techniques may give specific energy values to the same defect type, and second, the fact that we deal with a highly irregular surface which allows a variety of local environments and therefore prevents an accurate identification of the defect type, then a schematic representation of the associated energy levels may be misleading.
Appendix: Supplementary Material

Successive measurements of I-V characteristics, displayed in Figures A1 a,b, show that the hysteretic behavior is reproducible. A remanent charge localized on the surface state traps could determine a slight shift of the hysteresis curves, as observed in the case of long SiNWs. The current intensity slightly increases, correlated with this initial trapping effect. Another possible explanation may be the heating of the sample during the measurements.

FIG. A1: Successive measurements of I-V characteristics for short (700 nm) (a), and long (1000 nm), (b), SiNWs.
I-V curves measured on a third series of samples with 2 µm NW length are shown in Figures A2 a,b. The two SiNW arrays were processed with the same etching time, 10 minutes. Sample (a) oxidized at room temperature prior to contacts deposition. Sample (b) was treated in HF prior to contacts deposition, in order to remove any oxide layer from the surface of SiNWs. Sample (b) shows a smaller hysteresis area than that of sample (a), also twisted hysteresis in I-V characteristics, with 3 orders of magnitude smaller resistance. These results relate the hysteresis to the presence of trapping states at the Si-SiO$_2$ interfaces and underline their contribution to the conduction mechanism.

FIG. A2: I-V characteristics of oxidized (a), and HF cleaned (b), SiNWs.
The I-V curves of bulk silicon, plotted in the Figures A3, show no hysteresis. The measurement has been done as a reference and supports that the hysteresis observed in the corresponding plots of SiNW arrays are related to the much larger and more defective surface area of SiNWs.

![I-V characteristic of untreated bulk Si](image)

FIG. A3: I-V characteristics of untreated bulk Si.

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CREDIT AUTHOR STATEMENT

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DECLARATION OF COMPETING INTEREST

All authors have read and agreed to the published version of the manuscript. The authors declare no conflict of interest.

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