Chip Layout Optimization of SiC Power Modules
Based on Multiobjective Electro-Thermal Design Strategy

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(Manuscript received May 17, 2021, revised July 20, 2021)

Electro-thermal co-design of power modules is required to maximize the capabilities of promising power semiconductor devices. The chip layout on the substrate, which is restricted by the size of the power module substrate, determines the electrical and thermal characteristics of the power module. This paper proposes a chip layout optimization strategy for power modules based on a multiobjective electro-thermal design algorithm. The parasitic inductance and thermal resistance of the SiC power module are evaluated using the unified simulation model based on the multiphysics solver of the finite element method. The proposed multiobjective optimal design approach uses non-dominated sorting genetic algorithm II (NSGA-II) and the developed simulation model to obtain a Pareto front for the parasitic inductance and thermal resistance of the power module. Module samples with the obtained Pareto front parameters are experimentally characterized and validated with numerical simulation results.

Keywords: Power electronics, layout, optimization method, design automation, power module, finite element method

1. Introduction

High density power conversion systems are expected for various applications in modern society. The innovation of device structure has improved the performance of conventional silicon (Si) power semiconductor devices. In addition, wide bandgap semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) have the superior electrical and mechanical characteristics of high breakdown electric field, high mobility, and high thermal conductivity to conventional Si semiconductors (1). High switching frequency operation using these promising power semiconductor devices enables to miniaturize passive components (2), and increases power density of power conversion circuits. However, high di/dt in fast switching operation induces switching surge voltage across the parasitic inductance in the wiring of power modules or power conversion circuits (3) (4). It causes the anomalous self turn-on phenomenon of power MOSFET (5) or electromagnetic interference (EMI) noise emission to other equipment (6). The wiring design of the power module substrate enables to reduce the parasitic inductance. For example, a multi-layered power module substrate helps to lower the parasitic inductance in the module (7). In addition, the directly mounted snubber capacitor on the substrate reduces the parasitic inductance by minimizing the current loop path, which suppresses the switching surge voltage (8). Miniaturization of power modules and power conversion circuits also reduces the parasitic inductance in the wiring of circuits.

Miniaturization, however, increases not only mutual coupling among the wiring and passive components but also deteriorates heat dissipation per unit area/volume. The forward coupling of the mutual parasitic inductance in the wiring induces the switching surge voltage. The latter leads to the larger thermal resistance from the junction to heatsink on the mutual interference of proximately located power devices, which makes thermal management difficult. Wide bandgap power semiconductor devices are expected to increase the current density of power modules, which requires the more sophisticated design of wiring pattern and power device placement in power module compared to the conventional Si power semiconductor devices. Thus miniaturization of power modules has the difficulty of multidisciplinary improvement aspect in electrical and thermal characteristics. Maximizing the capability of promising power semiconductor devices requires a multiobjective optimal electrical and thermal characteristics design of the power module.

Power module design requires an accurate numerical model to estimate its actual electrical and thermal behaviors. Numerical simulation using finite element method (FEM) or finite volume method (FVM) enables to provide the high precision evaluation for these characteristics of power modules or power conversion circuits (9) (10) (11). Partial element equivalent circuit (PEEC) method or method of momentum (MoM) have also been utilized to extract the parasitic inductance and capacitance in power modules or power conversion circuits (12) (13). These numerical simulations have been applied to the design optimization for power modules. Reference (14) optimized the power module substrate for long-term reliability of a Si IGBT power module in terms of the thermal resistance and thermal stress using FEM simulation. References (15) and (16) optimized a forced air-cooled heatsink design for a multi-chip power module using the genetic algorithm.

A multiobjective optimization method is another key technology in the simultaneous electrical and thermal design of power modules (17). For example, the chip layout on the power module substrate affects not only electrical parasitic compo-
nents but also thermal resistance, especially in thermal interference. In general, the specification and manufacturing process restricts the size of power module substrate, which becomes the constraints for optimization. Then, there is a limitation in the size of the power module substrate for the optimization of the chip layout, whose size is determined in the manufacturing process. Though a chip layout was optimized to lower the junction temperature of chips in the power module based on particle swarm optimization algorithm in (18), the electrical characteristic such as the parasitic inductance is not considered. Some research groups developed a multiobjective optimization algorithm to design the power module substrate for minimizing the parasitic inductance and thermal resistance (19) (20) (21). However, these tools require the individual compact simulation model to analyze electrical parasitic components and the thermal resistance. Miniaturization increases the electrical and thermal coupling effect in the power module. A unified simulation model based on a multiphysics simulation tool, which uses the same solver, is suitable for the integrated design of the electrical and thermal characteristics.

This paper aims to propose a chip layout optimization strategy in power modules based on a multiobjective optimal design algorithm to achieve the best electrical and thermal characteristics with low computational cost. Both the parasitic inductance and the thermal resistance are numerically analyzed with the same FEM based multiphysics simulation model. A multiobjective optimization algorithm is developed based on the developed multiphysics FEM model and non-dominated sorting genetic algorithm II (NSGA-II). This paper demonstrates the chip layout optimization for the multi-layered ceramic substrate of a SiC power module to reduce the parasitic inductance in the module and the thermal resistance from the junction to ambient considering thermal interference between chips. The obtained Pareto front parameters in the multiobjective optimization are experimentally validated for the implemented SiC power module samples.

2. Proposed Modeling Method and Multiobjective Optimization Procedure

2.1 Multiobjective Optimization Based on NSGA-II

A multiobjective optimization problem consists of two or more objective functions that are in competition with each other, satisfying constraints such as specifications, manufacturing process, and cost. It provides a Pareto front or non-inferior solution depending on the weight of each objective function on the obtained solutions. The designers may choose the practical optimized design in the obtained Pareto front. A number of multiobjective optimization algorithms using the evolutionary algorithm have been suggested to obtain a Pareto-front (22) (23) (24) (25). These multiobjective optimization methods can lower the calculation cost without the convergence at the local minimum.

NSGA-II (25) is a well-known multiobjective optimization algorithm that expands the conventional genetic algorithm (GA) for the multiobjective optimization problem. NSGA-II introduces the crowded tournament selection operator and crowding distance to obtain a variety of solutions. Fig. 1 shows a schematic diagram of the NSGA-II procedure at a generation t. Here, P_t is the parent population of size N, and Q_t is the offspring population of size N after tournament selection, recombination, and mutation. The combined population of size 2N is non-dominated sorted. Solutions belonging to the best non-dominated set F_1 are the best solutions in the combined population and chosen for the new population P_{t+1}. This process is repeated until the size of the new population P_{t+1} exceeds N. When the size of l-th best solution F_l exceeds the size N, the crowding distance sorting is adopted to obtain the diversity in P_{t+1}.

The simulated binary crossover and the polynomial parameter mutation are adopted in this paper. The crossover rate and mutation rate are 0.8 and 0.25, respectively.

2.2 Electrical and Thermal Modeling of Power Module with FEM

Both the electrical and thermal characteristics of power modules are analyzed using the same FEM solver. Multiphysics FEM software Femtet (Murata software) can treat electromagnetic analysis, heat conduction analysis, stress analysis, etc., and their coupled analysis. This paper focuses on the modeling of the parasitic inductance and the thermal resistance for power modules. They are solved with harmonic electromagnetic analysis and heat conduction analysis, respectively.

Electromagnetic analysis of the solver gives the S parameter at a port of the analyzed model. S_{11} of S parameter gives the frequency characteristic of impedance Z at a port. Z is calculated by the following equation using S_{11} and the reference impedance Z_0=50 Ω.

\[
Z = \frac{1 + S_{11}}{1 - S_{11}}Z_0. \quad \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdOTS
\]

**Fig. 1.** Schematic diagram of the NSGA-II procedure.

Electrical parasitic components are identified from this frequency characteristic of impedance. Heat conduction analysis of the solver gives the temperature distribution in the simulated model by solving the heat diffusion equation. The transient thermal characteristics of the power module Z_{th}(t) is calculated as follow:

\[
Z_{th}(t) = \frac{T_j(t) - T_{amb}}{P_m}. \quad \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdOTS
\]

Here, \( T_j(t) \) is the temperature at the junction and is represented with space averaged value. \( T_{amb} \) is the ambient temperature, and \( P_m \) is the input power of heat.

2.3 Proposed Multiobjective Optimization Procedure

A flow chart of the proposed optimization algorithm for a multiobjective optimal design of power modules is shown in Fig. 2. This program is coded based on Python. NSGA-II for the multiobjective optimization is implemented in DEAP library on Python. The objective functions are extracted from the results by multiphysics FEM solver Femtet, which is run.
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Fig. 2. Flow chart of the developed algorithm for multi-objective optimization of power module.

by the macro based on Python.

The desired objective functions are minimized through NSGA-II. First, main program generates initial variables at random within the constraints. Next, the main program runs the subprogram to evaluate the fitness value. The subprogram generates a macro that contains the analyzed model dimensions and physical properties based on each individual, and runs Femtet to perform electromagnetic and heat conduction analysis to the given model. The fitness value is extracted from the returned FEM simulation results. After that, the main program progresses the evaluation for initial individuals, and generates next individuals. The generation exceeds after selection, crossover, mutation, and evaluation of offspring until it reaches the desired generation. The Pareto front will be obtained in the final generation.

3. Verification of Proposed Multiobjective Optimization Design Strategy

The proposed chip layout optimization strategy of power modules based on a multiobjective optimal design algorithm is validated in this section. This paper optimizes the chip location for both side arm in the SiC half-bridge power module with the multi-layered ceramic substrate using the developed algorithm. Here, the size of the power module substrate is used as a constraint.

3.1 Specification of Developed Power Module and Its Numerical Model

Figure 3 illustrates the structure of the studied SiC half-bridge power module using the multi-layered ceramic substrate, which is used as the reference power module substrate in this paper. The insulation layer is composed of silicon nitride (Si₃N₄) ceramic with 320 µm thickness. The Cu plate is brazed on ceramic with active metal as a conduction layer on both sides of the insulation layers. Two double side substrate is stacked and brazed to constitute a multi-layered substrate. The top and middle layer conductors are electrically connected at terminal M and N through four φ1.8 mm vias filled with Cu cores to flow a large current. There is the parasitic inductance in the current power loop for a half-bridge and dc bus. This undesired inductance causes switching surge voltage in switching transient. The developed structure reduces the area of the power loop in power conversion circuits, resulting in low parasitic inductance. Moreover, the middle copper layer of this developed multi-layered power module substrate spreads heat in the horizontal direction. This results in the lower thermal resistance from junction to case (26).

SiC MOSFET CPM2-1200-0080B (1200 V/40 A, 3.1 mm/3.36 mm/180 µm, CREE) die is attached with t = 120 µm Sn-Ag-Cu solder (Senju Metal Industry Co.) on the top layer Cu pattern for both side arm. The chip locations (x_HS, y_HS, x_LS, y_LS) as illustrated in Fig. 3(a) are (2.0, 2.0, 2.0, 2.0). Here, “HS” and “LS” denote the high-side and low-side arm of the half-bridge module, respectively.

The numerical simulation model overview for the electrical and thermal simulation with Femtet is shown in Fig. 4. This model consists of a die, a die-attach, a multi-layered ceramic substrate, 100 µm thermal grease, and an aluminum heatsink. The heat dissipating active area of SiC MOSFET is modeled on 2.6 mm/2.4 mm/20 µm at the surface of MOSFET to simulate the heat generation in the MOSFET channel. The cross-section of the bonding wire is approximated as rectangular based on geometrical mean distance (GMD) with 261 µm square for φ300 µm wire. The analysis port is set at the terminal P and N in the electromagnetic analysis. The fixed ambient temperature is given uniformly across the backside of a heatsink, and other model surfaces are thermally insulated. The physical parameters of each material at room temperature are listed in Table 1. Here, λ, c, ρ, σ, ε_r, and μ_r denote the heat conductivity, the specific heat, the density, the electrical conductivity, the relative permittivity, and the magnetic permeability in a vacuum, respectively. The
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Fig. 4. Numerical simulation model on Femtet.

Table 1. Physical parameters of materials for simulation.

| Material      | 1 [W/(m·K)] | c [J/(kg·K)] | ρ [kg/m³] | σ [S/m] | εr | μ0 |
|---------------|-------------|--------------|-----------|---------|----|----|
| SiC           | 495         | 680          | 3250      | 1.96×10¹⁰ | 1.0 | 1.0 |
| Sn-Ag-Cu      | 54          | 231          | 7400      | 6.67×10⁹  | 1.0 | 1.0 |
| Cu            | 402         | 385          | 8960      | 5.98×10⁹  | 1.0 | 1.0 |
| Al            | 58          | 630          | 3500      | 0         | 8.6 | 1.0 |
| Si grease     | 0.84        | 800          | 2340      | 0         | 1.0 | 1.0 |
| Air           | 237         | 902          | 2698      | 3.77×10⁷  | 1.0 | 1.0 |

Table 2. The obtained objective function in simulations and experiments.

| Layout | Simulation | Experiment |
|--------|------------|------------|
| A      | 7.51       | 7.44       |
| B      | 7.66       | 7.46       |
| A      | 1.54       | 1.55       |
| B      | 1.55       | 1.56       |
| A      | 1.44       | 1.46       |
| B      | 1.42       | 1.44       |

3.2 Multiobjective Optimization Setup

This paper demonstrates the electro-thermal optimization of SiC power module to the chip layout. The objectives functions in this study are given as follow:

\[
\begin{align*}
\text{min. } L_{PN} &= f_1(x_{HS}, x_{LS}, y_{HS}, y_{LS}), \quad \cdots \cdots \cdot \quad (3) \\
\text{min. } R_{HS} &= f_2(x_{HS}, x_{LS}, y_{HS}, y_{LS}), \quad \cdots \cdots \cdot \quad (4) \\
\text{min. } R_{LS} &= f_3(x_{HS}, x_{LS}, y_{HS}, y_{LS}), \quad \cdots \cdots \cdot \quad (5)
\end{align*}
\]

here \( L_{PN} \) is the parasitic inductance in the wiring of the power module between the terminal P and N in the unit (H), \( R_{HS} \) and \( R_{LS} \) are the steady-state thermal resistance from the junction of MOSFET to ambient temperature for high-side and low-side arm in the unit (K/W). Variables \( (x_{HS}, x_{LS}, y_{HS}, y_{LS}) \) give the location of the power devices as illustrated in Fig. 3(a), whose constraints are dependent on the physical structure of the package and chips. The location and length of the bonding wires are also changed associated with chip locations. The optimization process of NSGA-II is performed for 200 genes and ten generations.

3.3 Chip Layout Optimization Example

The obtained optimized objective function values using the developed algorithm through NSGA-II are shown in Fig. 5. Here, each axis is described in Eqs. (3) to (5), respectively. The blue markers are for initial genes, and the red markers are for final genes in Fig. 5(a). Fig. 5(b) shows the two dimensional mapping of the obtained Pareto front at final genes. The parasitic inductance and thermal resistance have a trade-off relationship, while the thermal resistance at each side arm does not have. The Pareto front surface in Fig. 5(a) is obtained as advancing generation, and convergence to a local solution is not found. Overall, the difference between the maximum and minimum value in the inductance and the thermal resistance is 6.3 nH and 0.20 K/W, respectively, on the obtained Pareto front. The multiphysics FEM simulation model enables the multiobjective optimal design of power modules. All the processing time from start to end is 266,343 sec for Core i9-8700K, DDR4-128GB memory, and 64-bit system. The average calculation time for each gene is 130 sec, and reducing the calculation time for electromagnetic analysis is a future task.

A Pareto front gives the users the layout which satisfies the desired constraints. The parasitic inductance and transient thermal characteristics for two layout configurations in the Pareto front are experimentally examined to verify the developed model for multiobjective optimization. The designed parameters of \( (x_{HS}, x_{LS}, y_{HS}, y_{LS}) \) for Layout A and B are (0.1, 8.8, 0.1, 5.4) and (4.2, 8.7, 8.2, 9.2), respectively, as indicated in Fig. 5. The simulated and experimental results are summarized in Table 2.

3.4 Electrical Characteristic Verification

Figure 6 shows the frequency characteristics of the parasitic inductance between terminal P and N for Layout A and B. Here, the blue and red lines are Layout A and B, respectively. The solid and dashed lines are the measured and calculated results, respectively. The measured result is experimentally obtained by impedance analyzer 4294A (Agilent Technology) with conducting MOSFET by applying \( V_{gs} = 18 \text{ V} \) across the...
gate to source terminals for both arm devices. The measured frequency characteristics of the parasitic inductance coincide with the simulation result for the optimized layout. The developed simulation model indeed characterizes the electrical characteristic of the module.

3.5 Thermal Characteristic Verification

The transient thermal network models called as structure function from junction to heatsink and ambient for each side arm of Layout A and B are shown in Fig. 7. The blue and red lines are experimentally obtained from the time response of junction temperature based on static test method using T3Ster (MentorGraphics), respectively, for high-side and low-side arm. Here, the time response of junction temperature is measured using the temperature dependency of a forward voltage drop in the body diode of the MOSFET for a fixed small measurement current. $V_{gs}=-18 \text{ V}$ is applied across gate and source terminal with the battery during the measurement, which is proposed by the authors in Ref. (28) to alleviate the difficulty in the junction temperature estimation of SiC MOSFETs. The green and magenta lines are the structure functions obtained from the simulated time response of junction temperature with FEM analysis, respectively, for high-side and low-side arms. Here, the averaged temperature on the surface of the active area is used as junction temperature. The obtained transient thermal network models of the measured results coincide with the simulation results for the optimized layouts, except for at the heatsink. The heatsink is simply modeled by a block whose backside is clamped with the ambient temperature, while a temperature-controlled water-cooled heatsink is used in the experiment. The difference of thermal capacitance at heatsink in Fig. 7 stems from the ideal ambient set in the simulation and actual thermal interface with thermal grease. Transient thermal characterization of power modules accurately simulates the thermal characteristics of power modules.

Figures 8 and 9 are the temperature distribution on the surface of each power module, which are simulated using FEM and measured by thermal image camera TG165 (FLIR), respectively. Here, the temperature gauge is not shown in the figure because the measured module surface is encapsulated with resin for passivation and the measuring spot of the camera is wider than the chip size. Thus, the absolute temperature does not coincide with the simulation result, but relative temperature distribution are useful for the comparison. The measured temperature distribution coincides with the simulated result well. The average junction temperature of Layout B 50.9 °C is lower than Layout A 52.3 °C in the simulation, which is in agreement with the optimal design here.

4. Conclusion

This paper proposed a chip layout optimization method for the coupled design on electrical and thermal characteristics of power modules based on a multiobjective optimization algorithm. The developed unified simulation model based on a multiphysics FEM solver and the developed multiobjective algorithm using NSGA-II enables to perform the multiobjective design of power modules. This paper optimized the chip location in SiC half-bridge module by the developed algorithm. The developed design strategy enables to evaluate the trade-off between the parasitic inductance and thermal coupling effect, and obtain the optimized layout for each charac-
teristic. The multiobjective optimization for an actual multi-chip power module and the design of a multi-layered power module substrate are under investigation.

Acknowledgment

This work was partially supported by JSPS KAKENHI Grant Number 20J10227, JAPAN. This work is partially supported by JST Open Innovation with Enterprises, Research Institute and Academia (OPERA) Program Grant Number JPMJOP1841, JAPAN. The author would like to thank Waseda University Graduate Program for Power Energy Professionals (PEP) for their scholarship to visit the University of Arkansas, Fayetteville, AR, USA, as a visiting student. The authors of this paper would like to acknowledge Prof. Alan Mantooth and his research team at the University of Arkansas, Fayetteville, AR, USA, for their invicing us to this work.

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