Hardware-aware mobile building block evaluation for computer vision

MAXIM BONNAERENS, IDLab-AIRO, Ghent University - imec, Belgium
MATTHIAS FREIBERGER, IDLab-AIRO, Ghent University - imec, Belgium
MARIAN VERHELST, MICAS-ESAT, KU Leuven, Belgium
JONI DAMBRE, IDLab-AIRO, Ghent University - imec, Belgium

In this work we propose a methodology to accurately evaluate and compare the performance of efficient neural network building blocks for computer vision in a hardware-aware manner. Our comparison uses pareto fronts based on randomly sampled networks from a design space to capture the underlying accuracy/complexity trade-offs. We show that our approach allows to match the information obtained by previous comparison paradigms, but provides more insights in the relationship between hardware cost and accuracy. We use our methodology to analyze different building blocks and evaluate their performance on a range of embedded hardware platforms. This highlights the importance of benchmarking building blocks as a preselection step in the design process of a neural network. We show that choosing the right building block can speed up inference by up to a factor of $2 \times$ on specific hardware ML accelerators.

1 INTRODUCTION

In recent years, machine learning models have seen a wide adoption in edge devices. Bringing these models to resource-constrained hardware has accelerated the research in the design of both, computationally efficient neural network models and specialized hardware accelerators that are optimized to execute these neural networks. Many compact neural networks for mobile deployment have been designed over the years, but optimal performance for a given hardware platform can only be achieved when the network is co-designed for it: not every model design choice that aims to improve efficiency does so on every hardware platform.

However, designing neural networks than can run on a certain target platform with a target latency is a complex task as they have many design choices, ranging from the type of layers used to the spatial resolution and the channel width of each block. Early work was done by manually designing efficient networks. MobileNetV1 [12] and its introduction of depthwise separable convolutions sparked the beginning of a research field focused on the design of efficient vision models that can be deployed on embedded and mobile platforms. Over the years, improved model architectures were released: MobileNetV2 [22] adds inverted residuals and inverted bottlenecks and MobileNetV3 [11] expands this further by adding the squeeze-and-excitation module [13] to the bottleneck structure. Another family of efficient models based on group convolutions and a shuffle operator are the ShuffleNets [17, 33]. All these models use multi-layer building blocks that are repeated multiple times in the network. Their design process focused mainly on optimising the layer structure of these building blocks in order to make them hardware efficient. Different variations of a network are typically manually designed [10, 17, 24], or scaled using a single complexity parameter to trade-off between task performance (e.g., accuracy) and computational cost, e.g., input resolution or channel width [12, 17]. In order to compare such efficient models, most works use curve estimates that show the trade-off between accuracy and a model complexity metric, such as FLOPs or latency, for predefined model variants of a model family. These curves allow practitioners to gain insight in these trade-offs and make the best choices for their design constraints.

Authors’ addresses: Maxim Bonnaerens, maxim.bonnaerens@ugent.be, IDLab-AIRO, Ghent University - imec, Belgium; Matthias Freiberger, IDLab-AIRO, Ghent University - imec, Belgium; Marian Verhelst, MICAS-ESAT, KU Leuven, Belgium; Joni Dambre, IDLab-AIRO, Ghent University - imec, Belgium.
The problem with curve based comparisons is that they only use a handful of model variants, while each model type still has a very large number of hyperparameters. Once the initial mobile building blocks had been established, the design process therefore shifted towards neural architecture search to find new state-of-the-art efficient models. Networks optimised with NAS have repeatedly shown to outperform manually designed networks [2, 14, 16, 18, 21]. As efficient models are targeted towards mobile and embedded platforms, they are often resource constrained. Hardware-aware NAS incorporates these constraints into the search, which allows finding optimal models for specific target platforms [8, 25, 26, 29]. However, the effectiveness of NAS comes with the very large computational cost of training and evaluating many candidate networks. A truly wide search is only feasible when large budgets can be spent on computing resources. For this reason, in practice, the search space of current NAS methods is usually constrained, using techniques such as parameter sharing [18]. These so called one-shot NAS approaches amortize the training cost of all networks in the search space by training all possible architectures together in a large supernet, reducing the cost of NAS by several orders of magnitude [4]. As a result most approaches in NAS now use a search space with a single, fixed building block while searching for other important parameters such as network depth and width or kernel filter size. The choice of the layer structure within the building block itself is mostly based on literature, common practice or previous experience.

As we will show, the relative efficiency of network families that use different building blocks depends, both, on the architecture of the targeted hardware platform and on the desired accuracy range. This means that a true hardware-aware network design approach requires a hardware-aware building block selection method as a front-end before finalizing the full network architecture either through NAS or manual design. To provide a more systematic approach to designing design spaces, [19] introduce a comparison paradigm based on empirically sampled distribution estimates. While the authors show in their follow up work [20] that it can be used to optimize a design space, it does not consider the trade off between complexity within a model family and hardware cost. As we will confirm in this paper, this trade-off offers crucial information, since the best choice can change, depending on the desired accuracy level, or when choosing a more powerful version of a given embedded platform type.

In this work we propose a methodology to evaluate and compare the performance of efficient network building blocks for computer vision in a hardware-aware manner. As in [20] which up until now was the main paradigm to compare design spaces, we use a sampled approach to pre-estimate how well a model family will perform. However, instead focusing only on the accuracy of a model family, we propose an extension based on a sampled estimate of the pareto front, highlighting the trade-off between complexity and accuracy. In Section 2, we revisit the work of [20]. Our approach is presented in Section 3, where we also demonstrate why information about the accuracy-complexity trade-off is necessary to make the best choices. We show that our extension allows to match the information obtained by [20], but is better suited to analyze the relationship between hardware cost and accuracy.

Finally, in Section 4 we use our methodology to analyze and compare some of the most common building block choices on various hardware platforms. Our analysis shows that while certain building blocks constructed with depthwise separable convolutions, inverted bottlenecks and Squeeze-and-Excitation modules may be more efficient FLOPs-wise, they are often not optimal for embedded ML hardware platforms when measuring the actual latency. As such, our approach can be used as a truly hardware-aware efficient building block selection step for the construction of mobile design spaces.
2 EMPIRICAL DISTRIBUTION FUNCTIONS

The work of [19] uses the concepts of design spaces and model families. A model family is a collection of related neural network models that share some set of high-level architectural design principles. These can range from very high level principles, such as the convolutional neural networks versus the vision transformer families, to very specific principles such as which specific layers to use and the relation between their depth, width and input resolution in EfficientNets.

A design space is a concrete set of architectures that can be instantiated from a model family. A design space consists of two components: a parameterization of a model family, such that specifying a set of model hyperparameters fully defines a network instantiation, and a set of allowable values for each hyperparameter.

To make a robust analysis of a model family over a wide range of network hyperparameters, Radosavovic et al. [20] introduced a new methodology: comparing model families using empirical distribution estimates. Instead of comparing handpicked variants of a network, they sample from a design space that parameterizes a network family over a wide range of network parameters and train them to collect accuracy metrics, which can be compared using empirical distribution functions (EDF). The normalized error EDF of a design space with $n$ models with errors $e_i$ is given by:

$$\hat{F}(e) = \frac{1}{n} \sum_{i=1}^{n} w_i [e_i < e]$$

(1)

$\hat{F}(e)$ gives the fraction of models with error less than $e$, with normalizing factor $w$ to control for model complexity.

While this approach allows to compare entire model families and has shown to be a valuable tool to create better design spaces [20], the metric it uses does not capture differences in accuracy/complexity trade-offs between different model families. This makes EDFs a useful tool when designing model architectures around a certain predefined complexity target.

3 CAPTURING TRADE-OFFS AND SEARCH SPACE DIFFICULTY

3.1 Random sampling versus Best models

The aim of hardware-aware network design is to optimally use the available computing budget to find solutions that are as close as possible to the accuracy/complexity pareto front for the targeted hardware platform. Since, in practice, there is a bound on the total number of network variants that can be evaluated within a reasonable time, it is beneficial to start from a family with similar best networks but a higher density of good networks.

In [19], Radosavovic et al. demonstrated their paradigm of comparing EDFs on different model families by generating the NDS dataset which consists of 5000 models from each corresponding design space. In Figure 1 we show 5000 trained models from two of the network families in this dataset, the NASNet [34] and the PNAS [15] model families, and highlight the best of those models on an accuracy/complexity curve.

Comparing only the best models from these larger sampling spaces as depicted in Figure 1a indicates that both families are capable of achieving similar results. However when we look at all the models in the scatter plots and the corresponding EDF in Figure 1c, we can see that, when randomly sampled, the PNAS family produces more models with good accuracy than the NASNet family. This means that, for a model designer or NAS-method, it is easier to find a well performing model for PNAS than for NASNet.

Instead of trying to estimate the true pareto front, we propose to use a random sampling accuracy/complexity curve based on a much lower number of samples (only 130). As can be seen in Figure 1b, the quality of this approximation decreases more rapidly for the NASNet family. This
means that, like the approach in [19], it implicitly captures the underlying difficulty of finding good solutions, but as an added value, this approach maintains the trade-off information.

![Fig. 1](image)

(a) Comparing the best performing models out of 5000 generated ones for the PNAS and NASNet families shows that they can achieve similar accuracies, but in general PNAS will provide good models much faster as can be seen in the normalized error EDF (c), which is also implicitly captured when creating accuracy/complexity curves (b) through random sampling with only 130 samples.

In essence our methodology to evaluate model families is done by executing the following steps: 1) create a design space for the model family to be evaluated 2) randomly sample ±130 models from this design space and train them in a low epoch regime 3) collect hardware costs such as latency from the target hardware platforms 4) create a pareto curve based on the optimal accuracy/complexity points from the sampled models.

### 3.2 Sample size

Training multiple neural networks to evaluate a model family is an expensive step in the process of designing a new model. While it is not necessary to train every sampled model until convergence as a low-epoch regime suffices to gather insights [20], we still aim to minimize the required number of samples.

We therefore analyzed the effect of the sampling size on the complexity/accuracy curve. To quantify this, we measured the average standard deviation across the accuracy/complexity curve over a 100 repetitions of a certain sample size. To determine the best point in this cost-benefit trade-off we use the Kneedle algorithm [23] to find the elbow point where the cost to train extra networks is no longer worth the expected decrease in noise on the pareto curve. Figure 2 shows the trendlines of the average standard deviation for increasing sample sizes as well as the elbow points. For all families in the NDS dataset this elbow point occurs for a sample size between 80 and 180 with a mean of 128. We therefore recommend a sample size of ±130 when using random sampling pareto curves.

### 3.3 Comparison to empirical distribution functions

In this section we illustrate why it is beneficial to keep information about the accuracy/complexity trade-off.

We first revisit the results from [19] for the DARTS [16] and ResNeXt [30] families to compare them to our approach. The corresponding normalized EDFs can be seen in Figure 3 (top row). To make a fair comparison we only use 130 sampled models for both approaches ([19] have also shown that any sample size above 100 provides a reasonable estimation). Using their approach, Radosavovic et al. concluded that DARTS and ResNeXt models are similar when normalized by the total number of trainable parameters and that the DARTS family is a better choice than ResNeXt
models when normalized by flops (top left and middle plots). The main insight obtained from these EDFs is that it shows which family provides more higher performing models. However it cannot show how this is related to the complexity of the models.

In the bottom plots of Figure 3, we show our random sampling accuracy/complexity curves. We can see that the ResNeXt and DARTS families perform similarly in the FLOPs domain until 150M FLOPs, where DARTS models start to outperform ResNeXt models. In the parameter domain we can see that the ResNeXt family produces slightly more efficient models in the low parameter setting but the DARTS family can reduce the error with larger models. Using EDFs becomes less insightful as the difference in the complexity distribution between model families becomes larger. When comparing the same ResNeXt and DARTS models based on their number of activations, which is a better proxy than FLOPs or parameters for certain memory-bound hardware accelerators such as GPUs and TPUs [2], the corresponding EDF still shows that ResNeXt and DARTS models perform similar, while our performance curve shows that the ResNeXt family outperforms DARTS in the lower complexity domain by a significant margin.

4 HARDWARE-AWARE MOBILE BUILDING BLOCKS EVALUATION

In this section we show the results of our evaluation of mobile building blocks for convolutional neural networks on various hardware platforms.

4.1 Mobile convolutional building blocks

Our focus is on comparing model families that are defined only by their convolutional building block, i.e. all models in the family have a structure that consists of a sequence of repeated blocks which can have different structural parameters such as input resolution and output channels but share the same layer structure. The different model families that we compare use the same design space and only differ in the used building block.

In recent years, one building block has been dominant in hardware-aware designed neural networks [9, 11, 26, 27]: the mobile inverted bottleneck convolution (MBConv). The structure of the building block is illustrated in Figure 4, it consists of a depthwise separable convolution used in an inverse bottleneck structure and in many cases a Squeeze-and-Excitation unit.
Fig. 3. (top) The normalized error EDFs highlight that DARTS models produce more highly accurate models. (bottom) Random sampling accuracy/complexity curves show that in the low complexity domain, ResNeXt actually outperforms DARTs.

Fig. 4. Structure of the MBConv building block, consisting of a depthwise separable convolution with an inverse bottleneck and Squeeze-and-Excitation unit.

While it has been shown to be a computationally efficient building block, recent work has shown that the large variation within layers of edge models due to the use of various diverse compression techniques results in throughput and energy efficiency shortcomings [3].

In the remainder of this work we evaluate alternative building blocks which differ in the convolutional layer type, the bottleneck structure and the inclusion of a Squeeze-and-Excitation unit.
4.2 Setup

We evaluate building blocks for mobile vision models based on the RegNet design space [20]. This is defined by 4 parameters: depth $d$, initial width $w_0$, slope $w_a$ and quantization $w_m$. Instead of making the width of every block in the neural network a hyperparameter, the RegNet design space parameterizes the block widths as $w_j = w_0 + w_a \cdot j$ for $0 \leq j < d$. This block width is additionally quantized through the hyperparameter $w_m$ such that the network only increases width at each of the 4 stages, where each stage consists of a sequence of identical blocks (see [20] for more details).

For all evaluations we sampled 130 models (as described in Section 3.2) from the design spaces created by the evaluated building block, and train each model for 10 epochs. The models are trained using SGD and a cosine learning rate schedule with initial learning rate 0.05 a weight decay of $10^{-4}$ and a batch size of 128 on an RTX 3090.

All evaluated networks are trained on the Visual Wake Words dataset [5]. This is specifically designed for vision models in embedded applications. It represents the vision use-case of identifying whether a person is present in an image or not. The dataset is derived from the publicly available COCO dataset, and provides a realistic benchmark for tiny vision models.

4.3 Hardware platforms

We evaluated the different mobile building block choices on a range of hardware platforms. The platforms evaluated are: a CPU and GPU found in modern mobile phones such as the Pixel 4, a dedicated hardware accelerator for edge devices (i.e. Intel Movidius Myriad X Vision Processing Unit (VPU)) and an embedded GPU from NVIDIA found on the Jetson Nano. We also include a benchmark on a server-grade GPU to highlight the difference between choices for mobile deployment versus cloud deployment. Table 1 gives an overview of the hardware platforms and also includes the inference framework used as it also influences the inference speed.

The latencies from the mobile CPU, mobile GPU and VPU are obtained using nn-Meter [32], a highly accurate latency prediction library.

| Device                | Processor           | Framework     |
|-----------------------|---------------------|---------------|
| mobile CPU            | Pixel4              | CortexA76 CPU | TFLite        |
| mobile GPU            | Pixel4              | Adreno 640 GPU| TFLite        |
| VPU                   | Intel NCS2          | MyriadX VPU   | OpenVINO      |
| embedded GPU          | Jetson Nano         | NVIDIA Maxwell GPU | TensorRT |
| server GPU            | Server              | NVIDIA RTX 3090 GPU | PyTorch   |

Table 1. Evaluated hardware platforms

4.4 Depthwise separable convolutions versus standard convolutions

Since its introduction in MobileNet [12], depthwise separable convolutions have been the de facto building block for efficient vision models. A depthwise separable convolution factorizes a standard convolution into a depthwise convolution and a $1 \times 1$ convolution called a pointwise convolution. This factorisation reduces the computations by a factor of $\frac{1}{C_{out}} + \frac{1}{K^2}$, where $C_{out}$ is the number of output channels of the convolution and $K$ the kernel size. For the commonly used $3 \times 3$ kernel size this means a reduction by a factor 8 to 9. While depthwise separable convolutions were initially introduced for small vision models, they became standard in vision models across all complexity ranges, e.g. the very large vision model EfficientNet-L2 with 480M parameters and 585B FLOPS also uses them.
Although standard convolutions may be more computationally expensive, they can, in certain cases, utilize the hardware resources better. Hardware accelerators for DL commonly use wide single-instruction multiple-data (SIMD) processing units to achieve a high FLOP/S throughput. However, high throughput can only be achieved if there is enough data re-use to fully utilize the processing units. In depthwise convolutions the data re-use is much lower than in standard convolutions as each input feature map is only used in the computation of its corresponding output feature map. During training, the resource utilization can be improved by using large batch sizes, obtaining data re-use with the convolutional kernel weights. However, during inference where typically batch sizes of 1 are used, this puts a memory bottleneck on the hardware accelerator. As a result, fused versions of the MobileNetV2 building block (Fused-MBCConv) where the first pointwise and depthwise convolution are fused into a standard convolution have recently been included in some hardware-aware neural architecture searches [9, 28, 31] and shown to be part of the best models on certain hardware platforms.

Figure 5 compares the randomly sampled pareto front of the design spaces based on depthwise separable convolution with the standard convolution. It can be seen that depthwise separable convolutions indeed outperform standard convolutions when comparing FLOPs. The performance curves for the mobile CPU and mobile GPU have similar trend lines and also favour the depthwise separable convolutions. For the Jetson Nano embedded GPU, however, we see that the theoretical advantage of standard convolutions no longer translates into faster latency. Instead, standard convolutions outperform depthwise convolutions as the complexity grows. On the VPU and server-grade GPU the initial order is reversed and standard convolution executes faster than the depthwise separable convolution.

To quantify the difference, we selected models with equal FLOPs from both families and compared the latencies on the different hardware platforms. On the mobile CPU, models from both families with equal FLOPs also have about equal latencies but on the VPU the inference time of the depthwise separable convolution models is $2 \times$ longer than the standard convolution models. A similar trend was seen on the embedded GPU where the latencies of those models were a factor $1.85 \times$ longer.

![Fig. 5. Depthwise separable convolutions are efficient when evaluated by FLOPS (upper left) but this does not translate to faster inference on all embedded hardware platforms.](image)
4.5 Grouped convolutions

In grouped convolutions the input channels are divided in multiple groups over which a normal convolution is performed, which puts their cost in FLOPS between those of depthwise separable and standard convolutions. This is confirmed in Figure 6 (top left). In fact, depthwise convolutions can be considered as a special case of grouped convolutions, where the number of groups equals the number of input and output channels. Similarly, standard convolutions are the special case where there is only 1 group.

In theory, grouped convolutions should be able to improve hardware utilization through their improved data reuse while still using significantly fewer FLOPs than standard convolutions. However, current implementations in most deep learning frameworks fail to leverage these advantages, which in practice makes grouped convolutions slower than their standard convolution counterpart [6]. Figure 6 shows that, indeed, grouped convolutions are never the most promising solution on any of the tested hardware platforms. This means that, for most target latency ranges and platforms using the much larger search space offered by grouped convolutions will rarely be beneficial. Instead, it is more efficient to narrow down the model design space to either depthwise separable convolutions or standard convolutions, based on their relative performance in trade-off plots like Figure 6.

![Fig. 6. While grouped convolutions should in theory be able to combine advantages from depthwise and standard convolutions, current implementation across various hardware accelerators and inference platforms fail to leverage these advantages making grouped convolutions not an optimal choice.](image_url)

4.6 Bottleneck versus inverted bottleneck

Bottlenecks were introduced together with residual connections in ResNets [10]. The main idea behind this is to lower the computational cost of each building block by performing the convolutions at a lower dimension, such that more building blocks can be stacked and deeper networks can be created without significantly increasing the computational cost.

A standard bottleneck structure consists of three convolutional layers: a $1 \times 1$ pointwise convolution to reduce the channel size, a standard convolution to improve the features, and a final $1 \times 1$ pointwise convolution to restore the channel dimensions. A parallel residual path connects
the input and output of this block. In MobileNetV2 [22] the inverted bottleneck was introduced where the residual connection is moved to connect the bottlenecks. In practice, this means that an inverted bottleneck consists of a pointwise convolution to expand instead of reduce the channel dimension, a (depthwise) convolution and a final pointwise convolution to restore the original channel dimension. The motivation for this design was that it is more hardware efficient as only the bottleneck lower dimension tensors need to be fully saved to memory as the intermediate higher channel dimension tensors are only used in depthwise convolutions. This means the tensor can be split into smaller ones.

A third possibility is to use no bottleneck, since the RegNet paper found that their best models used a bottleneck expansion/reduction factor of 1.0 [20]. When using no bottleneck we also drop the final pointwise convolution present in bottleneck structures since it is no longer required to make channel sizes match. All our building blocks in this comparison make use of depthwise convolutions.

![Fig. 7. The bottleneck structure has little influence on the latency across all tested hardware platforms. The accuracy of inverted bottlenecks significantly lacks behind building blocks with standard or no bottleneck.](image)

The results, as shown in Figure 7, indicate that using inverted bottlenecks degrades performance and fails to deliver the promised expected inference speedup. In general, across all hardware platforms, the blocks without a bottleneck and with a regular bottleneck show very similar performance. It can be observed that the VPU and server-grade GPU slightly favour the building block without bottleneck as it executes faster compared to bottleneck blocks. These are the same hardware platforms where the standard convolution outperformed the depthwise separable convolution, indicating that pointwise convolutions underperform on these platforms.

4.7 Squeeze-and-Excitation unit

A Squeeze-and-Excitation (SE) [13] block is an architectural unit for convolutional neural networks that performs dynamic channel-wise feature recalibration in order to improve the representation power of a convolutional building block. Given input \( X \) the SE unit first squeezes the spatial...
information using global average pooling:

\[
z_c = \frac{1}{H \times W} \sum_{i=1}^{H} \sum_{j=1}^{W} x_c(i, j),
\]

(2)

This step is followed by an excitation step that recalibrates the channels:

\[
s = \sigma(W_2(\text{ReLU}(W_1(z)))).
\]

(3)

Where \(W_1\) and \(W_2\) are two learned linear transformations and \(\sigma\) refers to the sigmoid activation function. The final output \(Y\) of the SE unit is obtained by scaling the original inputs \(X\): \(Y = X \cdot s\), where \(\cdot\) refers to the channel-wise multiplication.

MnasNet [26] brought the SE unit to mobile vision networks, as they were shown to improve model performance compared to previous state-of-the-art models with similar latency. More recently, however, Squeeze-and-Excitation modules have been removed from mobile vision architectures when they are deployed on embedded ML accelerators. EfficientNet-lite [7] and MobileNet-EdgeTPUv2 [1], for example, remove the SE unit as they claim it is not well supported for mobile accelerators such as the Google EdgeTPU.

We evaluated the SE block by comparing design spaces with the depthwise separable building block, with and without an SE unit extension. Figure 8 shows that the SE block is indeed a favorable addition for certain mobile platforms as it is very FLOPS-efficient. This also translates to its being more optimal for mobile CPU and GPU. However, for the embedded Jetson Nano GPU it is no longer a clear benefit to include the SE unit as it fails to exploit the optimizations for convolutional kernels and adds a significant delay. Comparing models with and without the SE unit, and with equal execution time on a mobile CPU, we found that those same models without the SE unit have a running time that is up to a factor 1.9× longer on the embedded Jetson Nano GPU.

Fig. 8. Adding a Squeeze-and-Excitation block improves performance on most hardware platforms but all. The Jetson Nano GPU for example executes them significantly slower, making them not always the optimal choice.
5 CONCLUSION
Developing a new model for a targeted hardware platform and with given design constraints requires careful consideration of the building block. An evaluation based on FLOPs often often leads to misleading conclusions w.r.t. the relative benefits of the components in the standard MBConv block on specific hardware platforms. We developed a methodology that can be used to select building blocks and constrain the design spaces for network design (e.g. as an input to NAS) in a hardware-aware manner, while maintaining the freedom to trade off between task performance and execution efficiency.

We used our approach to evaluate the hardware-efficiency of different convolutional building blocks on various hardware platforms. Our results show that execution of building blocks with components that are theoretical efficient such as the SE unit take a factor $1.9\times$ longer to execute than their non-optimized counterparts due to better hardware utilization on platforms with specific embedded ML accelerators such as the intel NCS2 or the Nvidia Jetson Nano.

In essence, our gained insights highlight the importance of benchmarking the building blocks used in mobile vision neural networks, which has been overlooked in the past. We believe that our methodology will be key to the develop hardware-aware neural networks for deployment on edge devices.

ACKNOWLEDGMENTS
This research received funding through the Research Foundation Flanders (FWO-Vlaanderen) under Grant G006718N and 1S47820N.

REFERENCES
[1] Berkin Akin, Suyog Gupta, Yun Long, Anton Spiridonov, Zhuo Wang, Marie White, Hao Xu, Ping Zhou, and Yanqi Zhou. 2022. Searching for Efficient Neural Architectures for On-Device ML on Edge TPUs. In Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition. 2667–2676.
[2] Bowen Baker, Otkrist Gupta, Nikhil Naik, and Ramesh Raskar. 2016. Designing neural network architectures using reinforcement learning. arXiv preprint arXiv:1611.02167 (2016).
[3] Amirali Boroumand, Saugata Ghose, Berkin Akin, Ravi Narayanaswami, Geraldo F Oliveira, Xiaoyu Ma, Eric Shiu, and Onur Mutlu. 2021. Google neural network models for edge devices: Analyzing and mitigating machine learning inference bottlenecks. In 2021 30th International Conference on Parallel Architectures and Compilation Techniques (PACT). IEEE, 159–172.
[4] Han Cai, Chuang Gan, Tianzhe Wang, Zhekai Zhang, and Song Han. 2019. Once-for-all: Train one network and specialize it for efficient deployment. arXiv preprint arXiv:1908.09791 (2019).
[5] Aakanksha Chowdhery, Pete Warden, Jonathon Shlens, Andrew Howard, and Rocky Rhodes. 2019. Visual wake words dataset. arXiv preprint arXiv:1906.05721 (2019).
[6] Perry Gibson, José Cano, Jack Turner, Elliot J Crowley, Michael O’Boyle, and Amos Storkey. 2020. Optimizing grouped convolutions on edge devices. In 2020 IEEE 31st International Conference on Application-specific Systems, Architectures and Processors (ASAP). IEEE, 189–196.
[7] Google. [n. d.]. EfficientNet-lite. https://github.com/tensorflow/tpu/blob/master/models/official/efficientnet/lite/README.md.
[8] Zichao Guo, Xiangyu Zhang, Haoyuan Mu, Wen Heng, Zechun Liu, Yichen Wei, and Jian Sun. 2020. Single path one-shot neural architecture search with uniform sampling. In European conference on computer vision. Springer, 544–560.
[9] Suyog Gupta and Berkin Akin. 2020. Accelerator-aware neural network design using automl. arXiv preprint arXiv:2003.02838 (2020).
[10] Kaiming He, Xiangyu Zhang, Shaoqing Ren, and Jian Sun. 2016. Deep residual learning for image recognition. In Proceedings of the IEEE conference on computer vision and pattern recognition. 770–778.
[11] Andrew Howard, Mark Sandler, Grace Chu, Liang-Chieh Chen, Bo Chen, Mingxing Tan, Weijun Wang, Yukun Zhu, Ruoming Pang, Vijay Vasudevan, et al. 2019. Searching for mobilenetv3. In Proceedings of the IEEE/CVF international conference on computer vision. 1314–1324.
Hardware-aware mobile building block evaluation for computer vision

[12] Andrew G Howard, Menglong Zhu, Bo Chen, Dmitry Kalenichenko, Weijun Wang, Tobias Weyand, Marco Andreetto, and Hartwig Adam. 2017. Mobilenets: Efficient convolutional neural networks for mobile vision applications. arXiv preprint arXiv:1704.04861 (2017).

[13] Jie Hu, Li Shen, and Gang Sun. 2018. Squeeze-and-excitation networks. In Proceedings of the IEEE conference on computer vision and pattern recognition. 7132–7141.

[14] Chenxi Liu, Barret Zoph, Maxim Neumann, Jonathon Shlens, Wei Hua, Li-Jia Li, Li Fei-Fei, Alan Yuille, Jonathan Huang, and Kevin Murphy. 2018. Progressive neural architecture search. In Proceedings of the European conference on computer vision (ECCV). 19–34.

[15] Chenxi Liu, Barret Zoph, Maxim Neumann, Jonathon Shlens, Wei Hua, Li-Jia Li, Li Fei-Fei, Alan Yuille, Jonathan Huang, and Kevin Murphy. 2018. Progressive neural architecture search. In Proceedings of the European conference on computer vision (ECCV). 19–34.

[16] Hanxiao Liu, Karen Simonyan, and Yiming Yang. 2018. Darts: Differentiable architecture search. arXiv preprint arXiv:1806.09055 (2018).

[17] Ningning Ma, Xiangyu Zhang, Hai-Tao Zheng, and Jian Sun. 2018. ShuffleNet v2: Practical guidelines for efficient cnn architecture design. In Proceedings of the European conference on computer vision (ECCV). 116–131.

[18] Hieu Pham, Melody Guan, Barret Zoph, Quoc Le, and Jeff Dean. 2018. Efficient neural architecture search via parameters sharing. In International conference on machine learning. PMLR, 4095–4104.

[19] Ilija Radosavovic, Justin Johnson, Saining Xie, Wan-Yen Lo, and Piotr Dollár. 2019. On network design spaces for visual recognition. In Proceedings of the IEEE/CVF international conference on computer vision. 1882–1890.

[20] Ilija Radosavovic, Raj Prateek Kosaraju, Ross Girshick, Kaiming He, and Piotr Dollár. 2020. Designing network design spaces. In Proceedings of the IEEE/CVF conference on computer vision and pattern recognition. 10428–10436.

[21] Esteban Real, Alok Aggarwal, Yanping Huang, and Quoc V Le. 2019. Regularized evolution for image classifier architecture search. In Proceedings of the aaai conference on artificial intelligence, Vol. 33. 4780–4789.

[22] Mark Sandler, Andrew Howard, Menglong Zhu, Andrey Zhmoginov, and Liang-Chieh Chen. 2018. Mobilenetv2: Inverted residuals and linear bottlenecks. In Proceedings of the IEEE conference on computer vision and pattern recognition. 4510–4520.

[23] Ville Satopaa, Jeannie Albrecht, David Irwin, and Barath Raghavan. 2011. Finding a”kneedle” in a haystack: Detecting knee points in system behavior. In 2011 31st international conference on distributed computing systems workshops. IEEE, 166–171.

[24] Karen Simonyan and Andrew Zisserman. 2014. Very deep convolutional networks for large-scale image recognition. arXiv preprint arXiv:1409.1556 (2014).

[25] Dimitrios Stamoulis, Ruizhou Ding, Di Wang, Dimitrios Lymberopoulos, Bodhi Priyantha, Jie Liu, and Diana Marculescu. 2019. Single-path nas: Designing hardware-efficient convnets in less than 4 hours. In Joint European Conference on Machine Learning and Knowledge Discovery in Databases. Springer, 481–497.

[26] Mingxing Tan, Bo Chen, Ruoming Pang, Vijay Vasudevan, Mark Sandler, Andrew Howard, and Quoc V Le. 2019. MnasNet: Platform-aware neural architecture search for mobile. In Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition. 2820–2828.

[27] Mingxing Tan and Quoc Le. 2019. EfficientNet: Rethinking model scaling for convolutional neural networks. In International conference on machine learning. PMLR, 6105–6114.

[28] Mingxing Tan and Quoc Le. 2021. EfficientNetv2: Smaller models and faster training. In International Conference on Machine Learning. PMLR, 10096–10106.

[29] Bichen Wu, Xiaoliang Dai, Peizhao Zhang, Yanghan Wang, Fei Sun, Yiming Wu, Yuandong Tian, Peter Vajda, Yangqing Jia, and Kurt Keutzer. 2019. FbNet: Hardware-aware efficient convnet design via differentiable neural architecture search. In Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition. 10734–10742.

[30] Saining Xie, Ross Girshick, Piotr Dollár, Zhuowen Tu, and Kaiming He. 2017. Aggregated residual transformations for deep neural networks. In Proceedings of the IEEE conference on computer vision and pattern recognition. 1492–1500.

[31] Yunyang Xiong, Hanxiao Liu, Suyog Gupta, Berkin Akin, Gabriel Bender, Yongzhe Wang, Pieter-Jan Kindermans, Mingxing Tan, Vikas Singh, and Bo Chen. 2021. Mobiledets: Searching for object detection architectures for mobile accelerators. In Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition. 3825–3834.

[32] Li Lyna Zhang, Shihao Han, Jianyu Wei, Ningxin Zheng, Ting Cao, Yuqing Yang, and Yunxin Liu. 2021. nn-Meter: Towards Accurate Latency Prediction of Deep-Learning Model Inference on Diverse Edge Devices. In Proceedings of the 19th Annual International Conference on Mobile Systems, Applications, and Services. ACM, New York, NY, USA, 81–93. https://doi.org/10.1145/3458864.3467882

[33] Xiangyu Zhang, Xinyu Zhou, Mengxiao Lin, and Jian Sun. 2018. ShuffleNet: An extremely efficient convolutional neural network for mobile devices. In Proceedings of the IEEE conference on computer vision and pattern recognition. 6848–6856.
[34] Barret Zoph, Vijay Vasudevan, Jonathon Shlens, and Quoc V Le. 2018. Learning transferable architectures for scalable image recognition. In Proceedings of the IEEE conference on computer vision and pattern recognition. 8697–8710.