Three-dimensional integration technology of magnetic tunnel junctions for magnetoresistive random access memory application

Kay Yakushiji*, Hideki Takagi, Naoyo Watanabe, Akio Fukushima, Katsuya Kikuchi, Yuuichi Kurashima, Atsushi Sugihara, Hitoshi Kubota, and Shinji Yuasa

National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba, Ibaraki 305-8568, Japan

*E-mail: k-yakushiji@aist.go.jp

Received March 31, 2017; accepted April 16, 2017; published online May 15, 2017

Three-dimensional integration processes (based on direct wafer bonding and back-surface silicon removal) for magnetic tunnel junctions with perpendicular magnetization (p-MTJs) were developed. Perfect wafer bonding, namely, bonding without interfacial voids, and damageless silicon removal were successfully demonstrated by using very flat tantalum cap layers. Moreover, p-MTJ nanopillars subjected to these processes exhibited no degradation in magnetoresistance or spin-transfer-torque (STT) switching. Magnetoresistive random access memory (MRAM) technology incorporating these processes (direct wafer bonding and back-surface silicon removal) will make it possible to integrate epitaxial MTJs (with a single-crystal tunnel barrier) and ferromagnetic electrode layers (based on new materials). © 2017 The Japan Society of Applied Physics

Three-dimensional (3D) integration technology based on direct wafer bonding and back-surface silicon removal processes is a key technology for developing next-generation ultrahigh-density nonvolatile memory such as spin-transfer-torque switching magnetoresistive random access memory (STT-MRAM)1–3 and novel voltage-torque MRAM.1,5 However, it is a great technological challenge to apply 3D integration technology to magnetic tunnel junctions (MTJs) because the magnesium oxide (MgO) tunnel barrier, which is only about 1 nm thick, is fragile and very sensitive to mechanical stresses. That is, even a single crack or a slight deformation of the tunnel barrier layer would seriously degrade the magnetoresistance (MR) and switching properties of the MTJs. For that reason, 3D integration technologies for MTJs have not been demonstrated so far.

Direct wafer bonding and back-surface silicon removal are important processes not only for the 3D stacking of MTJ cells for ultrahigh-density MRAMs but also for integrating epitaxial MTJs with a single-crystal tunnel barrier and a novel magnetic material in MRAM chips during the back-end-of-line (BEOL) process. Historically, the first high-performance MTJs with a MgO(001) tunnel barrier were epitaxially grown on single-crystal MgO(001) substrates.9 However, such epitaxial MgO-based MTJs were of little practical use because epitaxial MTJs could not be grown on polycrystalline metal lines (e.g., copper lines) of CMOS circuits in the BEOL. After that, (001)-oriented (textured) cobalt–iron–boron (CoFeB)/MgO/CoFeB MTJs, which can be fabricated on any kind of underlayer by the solid-phase epitaxial growth of amorphous CoFeB,10 were developed and applied to magnetic sensors and STT-MRAMs. Perpendicularly magnetized CoFeB/MgO/CoFeB MTJs11 are expected to be applicable to high-density STT-MRAMs with about 30-nm-sized MTJ cells. For ultrahigh-density MRAMs with an MTJ size of <20 nm, however, novel MTJs based on new tunnel barrier and magnetic materials will be needed to achieve enhanced MTJ properties such as lower write current, higher perpendicular magnetic anisotropy (PMA), and smaller saturation magnetization.13 New tunnel-barrier materials, such as spinel Mg−Al−O(001), and new ferromagnetic materials, such as Heusler alloys,12–17 may outperform the MgO barrier and CoFeB electrodes in the near future. For an MTJ composed of such new materials to exhibit high performance, it must be epitaxially grown on a single-crystal substrate. We therefore aimed to develop 3D integration technology for MTJs that will enable epitaxial MTJs to be integrated in MRAMs and other practical applications. Moreover, such epitaxial MTJs are effective for suppressing variations in MTJ properties owing to polycrystallinity, which will be a serious problem for <1X-nm generation, because the tunnel barrier and ferromagnetic layers of the epitaxial MTJs are both single crystals.

In this study, we used textured CoFeB/MgO-based MTJs with perpendicular magnetization (p-MTJs). It should be noted that a polycrystalline MgO tunnel barrier is more fragile than a single-crystal MgO barrier. The textured p-MTJ is therefore more suited to damageless 3D integration processes. Once the 3D integration processes are established with textured p-MTJs, they will surely be applicable to epitaxial MTJs (with a more robust single-crystal tunnel barrier). p-MTJ films were fabricated on 6-in. bare Si wafers by sputtering (with a Canon-Anelva C-7100 system) at room temperature. The films had a top-free-type stacking structure, as schematically shown in Fig. 1(a), consisting of (from the bottom up) a Si substrate/tantalum (Ta) seed layer/Ru/p-SAF/MgO tunnel barrier/CoFeB free layer/MgO cap/Ru/Ta cap layer.18,19 Here, p-SAF is a perpendicularly magnetized synthetic antiferromagnetic reference layer. The MR ratio and resistance–area (RA) product after annealing at 350 °C, as evaluated by the current-in-plane tunneling (CIPT) technique, were 120% and 5.3 Ω µm², respectively. On an 8-in. counter wafer, a lead electrode layer (based on low-resistance CuN layers) was stacked. Note that the counter wafer corresponds to a CMOS wafer with copper lines on top in an MRAM application. Tantalum was used for the cap layer both in the p-MTJ and counter wafers [Fig. 1(a)]. The Ta cap layers must be almost perfectly flat to avoid the formation of voids when they are bonded to each other. The criterion for avoiding void formation was found to be an RMS roughness of <0.2 nm. Figures 1(b) and 1(c) are schematic illustrations of the products obtained after direct wafer bonding and back-surface silicon removal, respectively. The details will be described later.

The 6-in.-p-MTJ and 8-in.-electrode wafers were bonded in a room-temperature bonding apparatus (Mitsubishi Heavy Industries MBW-12ST). The outline of a bonded product is shown schematically in Fig. 2(a). First, surface oxide layers on the Ta cap layers were sputter-etched in situ using an argon ion beam, then the wafers were immediately bonded in
a high vacuum. This bonding method is called “surface-activated bonding” (SAB).20-22 The argon ion beam energy was 1.5 keV, and the etching depth was 5 nm. A bonding load of about 3 MPa was applied for 60 s. The total thickness variation (TTV) of the bonded wafers was 2.3 µm. Defects at the bonding interface were evaluated by scanning acoustic microscopy (PVA TePla SAM 300). As shown in Fig. 2(b), most of the wafer area was successfully bonded. Only a few small white spots, which correspond to bonding defects due to small particles, are observed. A cross-sectional transmission electron microscopy (TEM) image of the bonded wafers is shown in Fig. 2(c). Except for the bonding defects due to particles, the two Ta cap layers are bonded almost perfectly. Note that it is very difficult to identify the bonding interface in the TEM image because the Ta cap layers are bonded uniformly without interfacial voids.

The back-surface Si in the 6-in.-p-MTJ wafer was removed by a high-speed (yet damageless) process. First, coarse and fine grindings were performed using 320- and 8000-grit wheels, respectively. The total grinding time ranged from 10 to 15 min. The average thickness of the remaining silicon was approximately 12.9 µm, and TTV was 1.2 µm. Next, the residual Si was selectively removed by wet etching with alkaline solution. To remove the Si layer, tetramethylammonium hydroxide (TMAH)-based solution, which exhibited a high etching selectivity to the Ta layer, was used. The TMAH concentration was 5%, and the etching temperature was 70 °C. The etching process and photographs of the ground and etched wafers are shown schematically in Fig. 3(a). Because the back-surface Si is completely removed, the surface of the wafer is a Ta layer, which was originally the seed layer of the MTJ film. Cross-sectional TEM images of the bonded wafers after the Si was removed are shown in Fig. 3(b). The surface is covered with a thin native tantalum oxide layer, which is easily removed during the subsequent microfabrication process.
After wafer bonding and silicon removal, additional annealing at 350 °C for 1 h was performed, and the p-MTJ film was then formed into nanopillars to evaluate the STT switching properties. Diameters (ϕ) of the p-MTJ pillars were varied from 28 to 65 nm by electron-beam lithography and argon ion etching. To compare the switching properties obtained before and after wafer bonding and silicon removal, p-MTJ nanopillars were also fabricated from p-MTJ films prepared by basically the same methods under the same conditions (i.e., without wafer bonding or silicon removal).

A typical magnetoresistance curve (electric resistance R vs magnetic field H) and STT switching properties of the p-MTJs (ϕ = 32 nm) formed without wafer bonding or silicon removal are shown in Figs. 4(a) and 4(b), respectively. The magnetoresistance curve shows an MR ratio of 114% with sharp reversals of the free-layer magnetization. On the other hand, the magnetization of the p-SAF reference layer was highly stable in the magnetic field range between −4 and +4 kOe. The STT switching properties for AP-to-P and P-to-AP switchings (where AP and P respectively denote antiparallel and parallel magnetic configurations) for a current-pulse duration of 2 µs are shown in Fig. 4(b). By fitting the experimental data (open circles) to the theory of thermally assisted STT switching (solid curves),23) average critical switching current (I_c0_avg) and thermal stability factor (Δ ≡ K_uV/k_B T) were evaluated to be 53 µA and 110, respectively. The switching efficiency (Δ/I_c0_avg) was about 2.

The typical magnetoresistance and STT switching properties of the p-MTJ (ϕ = 35 nm) obtained after wafer bonding...
and silicon removal are shown in Figs. 4(c) and 4(d), respectively. It is clear that a slightly higher MR ratio (143%) is obtained when wafer bonding and silicon removal are applied. We consider that the enhanced MR ratio is mainly due to the etching process used in nanopillar fabrication, because the blanket film exhibited a p-SAF field of about 4 kOe. Note that the p-MTJ has a top-pinned and bottom-free structure during nanopillar fabrication. STT switching properties after wafer bonding and silicon removal [shown in Fig. 4(d)] change only slightly. The p-MTJ showed \( I_{c0,\text{avg}} \) of 62 \( \mu \text{A} \) and \( \Delta \) of 98 (i.e., a switching efficiency of 1.6).

The dependences of \( I_{c0,\text{avg}}, \Delta \), and average critical switching voltage \( (V_{c0,\text{avg}}) \) on the diameter of p-MTJs are plotted in Figs. 5(a)–5(c), respectively. According to these figures, \( I_{c0,\text{avg}} \) reasonably scales with MTJ diameter. Moreover, \( \Delta \) is basically independent of MTJ diameter, while \( V_{c0,\text{avg}} \) slightly increases as MTJ diameter decreases. The trends of \( I_{c0,\text{avg}} \) and \( \Delta \) reasonably agree with those recently reported for pillar sizes below 50 nm.\(^{24-27}\) It can thus be concluded from the above-described results that the p-MTJ nanopillars exhibited favorable STT switching properties and no serious degradation after wafer bonding and silicon removal.

In summary, for the first time in the field of spintronics and magnetics, MTJs based on 3D integration technology (i.e., direct wafer bonding and back-surface-silicon removal) were successfully developed and tested. p-MTJ nanopillars after wafer bonding and silicon removal exhibited no degradation in magnetoresistance or STT switching. STT-MRAM technology incorporating direct wafer bonding and back-surface silicon removal will make it possible to integrate epitaxial MTJs with a single-crystal tunnel barrier and novel materials.

Acknowledgment
This work was supported by the ImPACT Program of the Council for Science, Technology and Innovation.

Fig. 5. Dependences of (a) average critical switching current \( (I_{c0,\text{avg}}) \), (b) thermal stability factor \( (\Delta) \), and (c) average critical switching voltage \( (V_{c0,\text{avg}}) \) on size \( (\phi) \) of magnetic tunnel junctions with p-MTJs after wafer bonding and silicon removal.