Pseudo-Differential Transconductor Circuit for a Low Supply Voltage Application

Nur Diyana Izni bt Mohd Sabari, Faizah bt Abu Bakar, Anishaziela bt Azizan, Sohiful Anuar Zainol Murad

Faculty of Electronic Engineering Technology, Universiti Malaysia Perlis, 02600 Arau, Perlis.

Email: diyanaizni@studentmail.unimap.edu.my, faizah@unimap.edu.my, anishaziela@unimap.edu.my, sohiful@unimap.edu.my

Abstract. This paper presents a pseudo-differential transconductor circuit. Operational Transconductance Amplifier (OTA) is a standout amongst the most functional and major circuit elements within the analog and mixed-signal circuit style. It is additionally one of the more intricate cells to plan. Due to the rising performance of new generation MOS transistors, the complexity of integrated circuit is continuously increasing with time. The reduction in component sizing is one of the main reasons for integrating millions of transistors into a single chip. There is a great demand for battery powered equipment like a laptop, wireless communication, and implantable devices. In all these devices, it is essential to maintain low power dissipation to achieve good battery life and weight. The main feature of the research is to design a pseudodifferential transconductor circuit for a low supply voltage application with the targeted gain greater than 20 dB using Mentor Graphics software. The designs are done in Pyxis Schematic and Pyxis Layout using eldo platform for simulation to simulate the functionality of the transconductor circuit. From the postlayout simulation, with supply voltage of 1.2V, the gain of 30 dB with cut-off frequency of 398 kHz has been achieved.

Keywords: Current mirror, Low supply voltage application, Op-amp, OTA, Pseudo-differential transconductor

1. Introduction

The transconductor is a fundamental construction piece of numerous simple circuits [1]-[2]. Because of process resilience, the principle parameters of voltage-controlled oscillators, variable gain amplifiers, or filters are required to control some level of programmability [3]-[5]. A few reviews have tended to the plan of low-distortion transconductors, applying dissimilar strategies that linearize the voltage-to-current (V-I) transformation within the input level. These strategies basically consist of cross-coupling, signal attenuation, pseudodifferential stages, source degeneration, and adaptive biasing [6].

Pseudo-differential (PD) structure is most preferred, as it maintains a strategic distance from the voltage drop over the tail current source [7]-[8]. There are many sorts of operation amplifier, however OTA is not the same as others since it is a voltage control current source device [9]. A few methodologies have been suggested to configure low-voltage OTA utilizing pseudo-differential (PD) setups. PD design needs an extra common mode feedback (CMFB) circuit which fulfills two reasons; first to settle the common mode voltage at high impedance nodes and the second to suppress the common-mode signal part [10].
Nonetheless, small supply voltages cause a few performance degradations such as degraded intrinsic gain, limited voltage swing and less dynamic range \[11\]. The objectives of this work is to design a transconductor circuit to achieve expected gain more than 20dB which has taken into account the process and temperature variation (PVT) with low power consumption using Mentor Graphic.

Current mirror is used as a fundamental building block which normally utilized as a part in linear IC design like transconductors, Current Conveyors, CFOAs (current feedback operational amplifiers), filters and others \[12\]-\[13\]. Current mirrors are utilized to give bias currents and active loads to circuits \[14\]. By using appropriate current mirrors with high output impedance, a good gain can be accomplished.

The important parameters that help in the designing of transconductor are gain, slew rate, common mode rejection ratio, power dissipation, gain bandwidth, power supply rejection ratio, and phase margin. A transconductor or generally called Operational Transconductor Amplifier (OTA) is basically an op-amp without any output buffer, preventing it from driving resistive or large capacitive loads. They are preferred over op-amps mainly because of their smaller size and simplicity. OTA essentially comprises of differential pair and current mirrors.

In this paper, the transconductor circuit is aimed to accomplish output gain greater than 20dB. The transconductor circuit is developed by several schematics such as two core transistors in pseudo-differential topology, common-mode feedback circuit, and common-mode feedforward circuit.

This paper is organized as follows. The proposed transconductor design is explained more detail in Section 2. Section 3 discusses the postlayout simulation results. Finally, the conclusion is given in Section 4.

2. Circuit Design

Figure 1 shows a conceptual block diagram of the pseudo-differential transconductor circuit designed. The structures of pseudo-differential, current mirror, common-mode feed forward, and common-mode feedback circuit are considered in order to complete the design.

![Figure 1. Conceptual block diagram of the designed transconductor circuit](image)

The topology of a general pseudo-differential transconductor is shown in Figure 2 which acts as core circuit for the circuit design.
In low power application, the lack of cascade and tail transistors prevent a large voltage drop across the tail current source and subsequently required a larger voltage source. The transconductor is power efficient because the bias current is reused by top (PMOS) and bottom (NMOS) parts of the structure. There are no obvious internal poles exist in the structure making it an advantage in a high bandwidth filter design. In addition, pseudo-differential transconductor also allows wider input and output voltage range and reduce the noise from the transistors at the load. Furthermore, NMOS input pairs are used such that the parasitic input capacitance is reduced compared to PMOS transistors.

The schematic of the proposed transconductor is shown in Figure 3. The core circuit of the pseudo-differential transconductor circuit above is presented by transistors M1 and M2. M1 and M2 are known as feedforward transconductor while M7 and M8 are known as feedback transconductor since the inputs for each core circuit depends on the outputs of the other core circuit, consequently giving a precise common-mode signal.

There are two common-mode feedforward (CMFF) circuits planned in each block of transconductor circuit. A common-mode feedforward (CMFF) circuit composed in the transconductor helps to control the effect caused by the variation in the input common-mode signals and to acquire the input common-mode rejection. The common-mode current is imitated by the M3 transistors and subtracted by the M4 transistor from the transconductor output. Despite that, the output common-mode voltage of the transconductor cannot be controlled by the CMFF. Consequently, a common-mode feedback (CMFB) circuit is also involved in the transconductor circuit.

In Figure 2, the pseudo-differential transconductor core circuit is shown. The circuit consists of transistors M1 and M2, which are part of the feedforward transconductor, and M7 and M8, which are part of the feedback transconductor. The schematic diagram in Figure 3 illustrates the entire transconductor circuit, including the CMFF and CMFB circuits.

Figure 2. Pseudo-Differential Transconductor Core Circuit

Figure 3. Pseudo-Differential Transconductor Circuit
The CMFF of the next transconductor (M9 and M10 transistors) generates the common-mode signal which is reused by the CMFB circuit. The M5 transistor has a fixed common-mode gate bias voltage which infuses the common-mode reference signal for the circuit. The M6 transistor then feeds back the output common-mode signal detected and it compares with the fixed reference current from the M5 transistor. With this topology, the accuracy of the PMOS current mirror restraints the DC common-mode rejection. Furthermore, the transconductor’s bias generation must be exact since the gain of the CMFB is very low. Hence, a mirror-error compensation circuit is executed to neutralize the error generated by the PMOS current mirror.

The size of transistors used in the whole transconductor circuit is shown in Table 1. The length (L) of the transistor is designed almost twice of 130 nm to take into account the impact of channel length modulation in the transistor during fabrication.

### Table 1. Transistors size

| Transistor | Size (W/L) μm |
|------------|--------------|
| M1         | (2.56/0.25)  |
| M2         | (15.2/0.25)  |
| M3         | (2.56/0.25)  |
| M4         | (30.4/0.25)  |
| M5         | (5.12/0.25)  |
| M6         | (30.4/0.25)  |
| M7         | (2.56/0.25)  |
| M8         | (15.2/0.25)  |
| M9         | (2.56/0.25)  |
| M10        | (30.4/0.25)  |

A systematical error exists in the PMOS current mirror of the transconductors [15]. The error of the mirror circuit can be demonstrated as a small common-mode current that is infused into the transconductor output, thereby urging to a shift in the output common-mode voltage of the transconductor. Since the transconductance of the pseudo-differential transconductors relies upon the input common-mode level, precise biasing is necessary in this design. For integrated circuit, resistor biasing of transistor circuits is not used since they occupy a larger area region than transistors.

A mirror-error compensation circuit which adds the error in the common-mode with an inverse polarity to the reference signal of the common-mode was outlined as shown in Figure 4. Transistors M1-M2 are the duplicate of the core of the transconductor, while transistors M3-M4 are the copy of CMFF circuit. Hence, the transistors’ sizes are the same as the ones in transconductor circuit. The common-mode level errors in the transconductors are wiped out by injecting the reverse-polarity common-mode reference signal to the VERROR gate at the CMFB circuit of the transconductor.
There are two op-amp circuits in the mirror-error compensation circuit, the schematic is designed as shown in Figure 5. From the op-amp circuit, transistors M6, M7 and the capacitor with 5.648fF act as a buffer in order to lower the output resistance.

The feedforward transconductor and feedback transconductor are design separately as shown in Fig.6 and Fig.7 respectively.
The supply voltage, VDD is connected to a DC voltage source with 1.2V to fulfil the low supply voltage for this circuit. Two AC voltage sources are required to perform AC analysis with magnitude of
0.5V in opposite orientation. The common-mode voltage is set to half the VDD which is 0.6V. AC analysis is performed in order to get the simulated circuit gain.

Figure 8 shows the layout of the proposed transconductor. The designing process of the layout is done after the simulation of the transconductor circuit. The work is done using Mentor Graphics Pyxis schematic driven layout.

3. Postlayout Simulation
The proposed transconductor was simulated using Mentor Graphics Pyxis employing 130 nm technology. The postlayout simulation result of the transconductor circuit is shown in Figure 9.
From the figure, it is shown that the measured gain is 30.5dB. The -3dB point is the frequency that the gain has reduced to 0.707 of its peak value. From the figure, the -3 dB or the cut-off frequency of the transconductor is shown to be 398 kHz.

4. Conclusion
In this paper, a pseudo-differential transconductor circuit is presented. Pseudo-differential transconductor circuit is suitable for low voltage application since it avoids voltage drop across the tail current. There are two transconductor core circuits with two common-mode feedforward circuits and a common-mode feedback circuit to fix the common-mode signals. A new transconductor circuit based on pseudo-differential topology is designed and functioned well with the DC gain of 30.5 dB which has taken into account the process and temperature variations (PVT) using Mentor Graphics.

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