Recent Development in Analog Computation

– A Brief Overview

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Abstract – The recent development in analog computation is reviewed in this paper. Analog computation was used in many applications where power and energy efficiency is of paramount importance. It is shown that by using innovative architecture and circuit design, analog computation systems can achieve much higher energy efficiency than their digital counterparts, as they are able to exploit the computational power inherent to the devices and physics. However, these systems do suffer from some disadvantages, such as lower accuracy and speed, and designers have come up with novel approaches to overcome them. The paper provides an overview of analog computation systems, from basic components such as memory and arithmetic elements, to architecture and system design.

I. INTRODUCTION

There are more and more application cases where the energy efficiency of computational elements is of paramount importance. One of such example is portable devices where the volume and weight of the battery is limited, and the power consumption needs to be minimized to extend the battery life. A more extreme case is the autonomous sensors where all the operation power is scavenged from environment [1]. In implantable biomedical devices, the power consumption has
to be minimized so that the heat generated does not affect the nearby tissue, and battery life is maximized.

In order to accommodate this ever-increasing need for efficiency, researchers have designed the analog frontend of these systems with great performance and efficiency. For example, [2] [3] [4] discussed low-power high-performance frontend amplifiers and filters for implantable systems. Analog to digital converters (ADCs) [5] [6] [7] [8] [9] are usually an important and power-hungry part in these systems, and [10] [11] proposed comparator designs that can greatly improve the accuracy and efficiency of these ADCs. Computational units (processors) are another essential part, as they provide autonomous decision making, compression of sensory data, and other functions. These computational unit are usually implemented with digital processors, which can be too inefficient for ultra-low-power applications.

To explore the approaches that could lead to efficiency beyond digital processors, it is meaningful to compare the energy efficiency between the human brain and the digital processor. The human brain has an energy efficiency of about $10^{15}$ operation per joule [12]. Today’s super computer’s energy efficiency is about $8.3 \times 10^9$ operation per joule [13], more than 6 orders of magnitude lower than the human brain. The huge energy efficiency gap suggests that the ways they do computation are fundamentally different. One notable difference is how the information is presented. Digital computer uses binary system, that is, systems using only 0 and 1 to achieve better immunity to noise. Whereas the neurons are using a continuous presentation of information, more like analog circuits. For example the firing rates and the membrane potential in a neuron are continuous variables. These analog signaling implies that a single wire can carry multi-bit information, as a result, the wiring and signaling overhead can be largely reduced. In addition, neurological system cleverly exploits the physical phenomena as the bases for
computation. Aggregation and integration are carried out in charge domain, using the conservation of charge. Summing is implemented by observing Kirchhoff’s current law (KCL). Amplification and non-linear functions are realized by modulation of energy barriers to ions in thermal equilibrium and therefore whose energies are Boltzmann distributed [14]. All these principle of operation is actually found and available in integrated circuits [15]. However, by using only on and off states of active devices, digital computers lose a factor of $10^4$ in efficiency [14]. Analog circuits have principles that are much more similar to neurological systems and have the potential to get back the lost efficiency. However, the analog computation is for the same reason more sensitive to noise and offset when compared to digital computers. It is found in [16] that the cost for precision for analog system increases exponentially, while that for digital increases polynomially. Therefore, analog computation is more preferable at low accuracy. Interestingly, the brain is also known to be of low accuracy, with a typical signal-noise ratio (SNR) in the range of 1-10 [17], [18], [19]. This in turn suggests that very high energy efficiency can be achieved if the system is built to tolerate the relative inaccuracy of analog computation.

In this paper, we will discuss different aspects of analog computation system, starting from basic components such as memory and arithmetic elements, to the entire architecture design of an analog deep learning engine.

II. ANALOG MEMORY

Memory is one of the indispensable components in a computation system. Most of modern digital memories are volatile, either requiring constant refreshing, or a minimum VDD for state retention [20]. Non-volatile digital memories including flash memory [21], FRAM (Ferroelectric RAM) [22], [23], ReRAM (Resistive RAM) [24], and MRAM (Magnetoresistive
RAM) [25] require special process and add to fabrication cost. In analog computation systems, digital memory has inherent difficulty in integration because they require analog-digital conversion to interface with other circuits in analog domain. Recently, researchers have proposed different designs of Floating gate (FG) memories to realize analog non-volatile storage of information.

A floating gate device has gate that is electrically isolated from outside (floating), and the charge trapped on this isolated gate is used to store analog or digital values. To modify the charge on the floating gate, two mechanisms can be used. When a high voltage is applied across the gate oxide, the oxide barrier becomes more triangular and its effective thickness is reduced, making it easier for the quantum tunneling of electrons from the gate to the channel to happen. This is called Fowler–Nordheim (FN) tunneling and is a major cause of gate leakage current in modern deep-sub-micron process and can be measured and characterized with specially designed circuits [26]. As the reverse process of FN tunneling, hot electron injection can be exploited to add electron to the FG. When the source-to-drain voltage of a PFET is sufficiently large, the energy of holes near the drain side is large enough to generate hot electron-hole pairs. The liberated hot electrons are able to overcome the oxide barrier and be attracted to the floating gate, which is at positive potential.

In contrast to people’s perception that FG devices can only be used to build digital memories such as EEPROM of Flash memories, they are actually more of an analog device, as the amount of charge on the FG is change in a continuous way. In the literature, FG devices are extensively used to implement analog systems [27], [28], [29], [30], [31], [32].
One of the important design difficulties of FG analog memories is to achieve tunneling control. Because FN tunneling requires high voltage, it is relative more difficult to control as the high voltage needs to be applied on or removed from the gate selectively. Therefore, many works [30], [31] choose not to have individual control of tunneling, instead, they use tunneling as global erase, and injection to program individual memory to its target, making it difficult to be used in adaptive systems. Selective tunneling is proposed in [33], by simultaneous control of the tunneling and control gate voltages. This requires a large number of pins and therefore not suitable for large-scale systems. In [27], a high-voltage switch is proposed to control the tunneling voltage individually, which is not compatible with standard process and consumes power. A charge pump is used to generate a local HV for the selected memory [32].

The update rules describe how the memory output changes with the update command. Single-transistor memory [33] tends to have exponential update rules, which are not desirable for the stability of algorithm [32]. By keeping the FG voltage constant during update, a more linear update rule can be realized [27] [32].

Paper [34] presents floating-gate analog memory with current mode output. It uses a novel approach to realize random access of individual memory in an array, as well as updates at both direction (tunneling and injection), without the use of charge pump or high voltage switch. The

| Parameter                      | Value                      |
|-------------------------------|----------------------------|
| Technology                    | 1P8M 0.13-μm CMOS          |
| Area                          | 35×14 μm²                  |
| Power supply                  | 3 V                        |
| Power consumption             | 45 nW                      |
| Output range                  | 0 - 10 nA                  |
| Programming resolution        | 7 bits                     |
| Dynamic range                 | 53.8 dB                    |
| Programming isolation         | 86.5 dB                    |
interconnection and pin count is minimized, facilitate scaling. And the memory has a pseudo-linear sigmoid update rule, which is more preferable than exponential rules. The memory design is compatible with standard digital processes and was implemented in a 0.13μm digital CMOS process, achieving small area and low power consumption. The performance of the analog memory in [34] is summarized in Table I.

III. ANALOG NON-LINEAR OPERATOR

One of the advantages of analog computation is that some non-linear functions can be realized directly, while in digital processor, they require lots of computational resources. One family of important non-linear functions is radial-basis functions. These bell-shaped functions are extensive utilized, because they are a good metric of similarity in artificial neural network and machine learning systems [30], [35], [36], [37]. A bump circuit [38] provides arguably the simplest way to generate this kind of function, although this implementation does not have tunable width of the transfer function. In [30], a floating gate input stage is added to scale the input to get a variable width. Researchers use a digital-to-analog converter (DAC) to for similar purpose [36], both of these two approaches increases area and power consumption. Paper [35], [39] propose to switch the number of transistors connected in the circuit to vary the bump width, which leads to limited number of achievable transfer functions. A direct synthesis method is presented in [40], where the squared difference is exponentiated to yield a Gaussian function; however, the circuit design is relative complex and occupies large area.
By combining the current correlator discussed in [38] and a tunable transconductor, paper [41] achieve both variable width and height of the bump function. In [41], the design of linear transconductors in sub-threshold CMOS is discussed. Such design is challenging because the linear range of differential pair becomes smaller as the device enters weak inversion [42]. Linearization techniques have been proposed for strong inversion [42], [43], [44] [45], but none of these is adequate with biasing current down to nA. In [41], the output resistance of saturated transistor is exploited to implement a tunable resistance with very large value, which is used as the degeneration resistor for the trans-conductor. A novel pseudo-differential structure is also

![Figure 1: The measured 2-D bump output with different width on x and y dimensions [41].](image)

| Table II. Performance Summary and Comparison of the Bump Circuits |
|---------------------------------------------------------------|
| **Parameter** | [41] | [30] | [39] | [40]* |
| Technology | 0.13 μm | 0.5 μm | 0.13 μm | 0.18 μm |
| Supply voltage | 3 V | 3.3 V | 1.2 V | 0.7 V |
| Power | 18.9 nW | 90 μW | 10.5 μW | 485 nW |
| Area | 988 μm² | 3444 μm² | 1050 μm² | - |
| Response time | 45 μs | 10 μs | - | 9.6 μs |

*: simulation results
proposed to allow operation with supply voltage as low as 0.5V. In Figure 1, the measured 2-D bump output is plotted by cascading two identical bump circuits, with each dimension's parameters individually tunable. Table II summarizes and compares the performances of recently reported tunable bump circuits.

IV. ANALOG ONLINE CLUSTERING ENGINE

K-means clustering algorithm finds the underlying regularity in multi-dimensional data by capturing the spatial density patterns, and is used in many applications such as feature extraction and pattern recognition [46]. The algorithm is relative resource-intensive in digital domain, as it requires the parallel operation of multi-dimensional matrices. Analog computation has potential to improve upon digital processors in energy efficiency when implementing this algorithm [16].

Previous works have proposed analog vector quantizers (VQ), a simplified clustering engine, which search a set of pre-programmed templates and find the one that closest to the input [47], [48]. The clustering engine is one step further than VQ as it is able to adapt the templates according to the input statistics and therefore is more flexible in the face of changing environment. Analog clustering engines are relatively less reported due to their difficulty of design. The two designs in [49] and [36] have the template stored in volatile memories, precluding their use in applications with intermittent power. The use of digital memory in [36] requires analog to digital conversions for interfacing and adds to headroom. A novel analog online clustering engine is presented in [50]. Apart from the real-time online clustering capability, it is also capable of providing a measure of similarity between the input and each template based on simplified Mahalanobis distances, which greatly facilitates its integration to a more complex system. The learned templates are stored in a non-volatile fashion, enabling reuse after black-out. The prototype design with 8 by 4 dimensions was fabricated in a 0.13 μm digital CMOS process.
Figure 2: Clustering test result.

| Parameter                  | Value                              |
|----------------------------|-----------------------------------|
| Technology                 | 1P8M 0.13 μm CMOS                 |
| Total Area                 | $0.9 \times 0.2 \text{ mm}^2$ (8 × 4 array) |
| MDC Cell Area              | $90 \times 30 \mu\text{m}^2$      |
| Power consumption          | $15 \mu\text{W} @ 3\text{V}$     |
| Classification Speed       | 16 kHz                            |
| Clustering Speed           | 4 kHz                             |

Figure 2 shows the clustering test results of the prototype [50]. The green dots are input vectors with 4 underlying clusters, each with different mean and sigma. The magenta lines show the evolution of template during clustering. Clearly the prototype was able to find the centroids and variances of the input data clusters accurately, demonstrating a robust learning performance. The measured performance is summarized in Table III.
V. Analog Machine Learning Engine

The era of big data witnesses the extensive research and application of machine-learning [51]. Among the various subjects of machine learning, deep machine learning (DML) architectures mimic the information representation in the human brain, with the objective to achieve robust automated feature extraction, and provides a solution to the “curse of dimensionality” [52].

DML systems require massive parallel computation, which researchers have been realized with GPU-based platforms [53]. However these implementations are usually power hungry, making it hard to incorporate them to portable or wireless devices, and restrict their potential of scaling-up. Analog computation provides the potential to overcome this limit by achieving much higher energy efficiency compared to their digital counterpart.

Analog computation has been employed in machine learning systems and their building blocks [47] [36] [35] [30] [49] [41]. However, the ability to learn is what lacks in many of these designs. As a result, parameters have to be pre-programmed in order for the systems to function properly [47], [35], [30]. This places serious limitation on the application of these systems. A machine learning system with supervised learning capability is discussed in [36], but it still relies on the label provided during the training.

In these systems, memories are usually implemented in digital domain, which requires analog-digital conversions in order to interface with other analog circuitries. These additional conversions consume unnecessary area and power headroom, and require the memory to be centralized instead of distributed [54], [55], [56], [36]. In [49], analog values are stored on capacitors, this storage technique is inherently analog, but due to the leakage, it requires frequent refreshing, and the values drift over long term. These volatile storages are disadvantage because
they will lose their states in the event of blackout, which can be common in battery-less applications where the power is harvested from the environment. [1].

In [37] [57], an analog deep learning engine is presented. It learns by unsupervised training, which is more preferable compared to supervised ones in that it does not require external assistant and therefore achieves fully autonomous operation. The learned parameters are stored in analog floating gate memories, which is non-volatile and compatible to standard digital processes. For easy scaling, the architecture adapts an array-based structure, which provides future possibility of large-scale implementation. The energy efficiency is the paramount design

![Figure 3: Measured classification accuracy using the feature extracted by the chip [57].](image)

| TABLE IV. COMPARISON OF ANALOG PROCESSORS |
|-----------------------------------------|
| Process | JSSC’15 [57] | JSSC’13 [54] | ISSCC’13 [55] | JSSC’10 [56] |
| Purpose | DML Feature Extraction | Neural-Fuzzy Processor | Object Recognition | Object Recognition |
| Non-volatile Memory | Floating Gate | NA | NA | NA |
| Power (W) | 11.4u | 57m | 260m | 496m |
| Peak Energy Efficiency | 1.04TOPS/W | 655GOPs/W | 646GOPs/W | 290GOPs/W |
goal of this work and the authors uses several innovative design strategies to maximize the efficiency including parallel computation, deep sub-threshold biasing, algorithmic feedback to mitigate analog non-ideality \cite{58}, current mode arithmetic, distributed memory and flexible power domain partition. In Figure 3, image feature extraction is demonstrated, which reduces the input dimension from 32 to 4. The measured peak energy efficiency is over 1 Terra-OPS per Watt, and it is shown that the accuracy achieved is comparable to emulations in floating-point software environment, also shown in Figure 3. The performances of recent state-of-art parallel processors which employ bio-inspired analog computation are listed and compared in Table IV.

VI. CONCLUSIONS

This paper provides a brief survey of recent development in analog computation. Although analog computation has been around for a long time, researchers have recently focused on this topic as it shows the potential of energy efficiency improvement over digital processors. However, as analog systems require custom design and are sensitive to circuit non-idealities, innovative design and careful considerations on circuit, algorithm and architecture levels are important to achieve good performance.
REFERENCES

[1] Y. Zhang, F. Zhang, Y. Shakhsheer, J. Silver, A. Klinefelter, M. Nagaraju, J. Boley, J. Pandey, A. Shrivastava, E. Carlson, A. Wood, B. Calhoun and B. Otis, "A batteryless 19 uW MICS/ISM-band energy harvesting body sensor node SoC for ExG applications," IEEE J. Solid-State Circuits, vol. 48, no. 1, pp. 199-213, Jan. 2013.

[2] T. Yang, J. Lu and J. Holleman, "A high input impedance low-noise instrumentation amplifier with JFET input," in Proc. 56th IEEE Int. Midwest Symp. Circuits and Syst. (MWSCAS), Aug. 2013, pp. 173-176.

[3] T. Yang, J. Lu, N. Poore and J. Holleman, "A current-reuse complementary-input chopper-stabilized amplifier for neural recording," in Proc. IEEE Int. New Circuits and Syst. Conf. (NEWCAS), Jun. 2014, pp. 85-88.

[4] J. Lu, T. Yang, M. S. Jahan and J. Holleman, "A low-power 84-dB dynamic-range tunable Gm-C filter for bio-signal acquisition," in Proc. 57th IEEE Midwest Symp. Circuits Syst. (MWSCAS), Aug. 2014, pp. 1029-1032.

[5] H.-C. Hong and G.-M. Lee, "A 65-fJ/Conversion-Step 0.9-V 200-kS/s Rail-to-Rail 8-bit Successive Approximation ADC," IEEE J. Solid-State Circuits, vol. 42, no. 10, pp. 2161-2168, Oct. Oct. 2007.

[6] S.-K. Lee, S.-J. Park, H.-J. Park and J.-Y. Sim, "A 21 fJ/conversion-step 100 kS/s 10-bit ADC with a low-noise time-domain comparator for low-power sensor interface," IEEE J. Solid-State Circuits, vol. 46, no. 3, pp. 651-659, Mar. 2011.

[7] N. Verma and A. Chandrakasan, "An ultra low energy 12-bit rate-resolution scalable SAR ADC for wireless sensor nodes," IEEE J. Solid-State Circuits, vol. 42, no. 6, pp. 1196-1205, Jun. 2007.
[8] M. Yoshioka, K. Ishikawa, T. Takayama and S. Tsukamoto, "A 10 b 50 MS/s 820uW SAR ADC with on-chip digital calibration," in IEEE ISSCC Dig. Tech. Papers, Feb. 2010, pp. 384-385.

[9] J. Yuan and C. Svensson, "A 10-bit 5-MS/s successive approximation ADC cell used in a 70-MS/s ADC array in 1.2-um CMOS," IEEE J. Solid-State Circuits, vol. 29, no. 8, pp. 866-872, Aug. 1994.

[10] J. Lu and J. Holleman, "A low-power dynamic comparator with time-domain bulk-driven offset cancellation," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 2012, pp. 2493-2496.

[11] J. Lu and J. Holleman, "A low-power high-precision comparator with time-domain bulk-tuned offset cancellation," IEEE Trans. Circuits and Syst. I, Reg. Papers, vol. 60, no. 5, pp. 1158-1167, May. 2013.

[12] R. C. Merkle, "Brain, Energy Limits to the Computational Power of the Human," [Online]. Available: http://www.merkle.com/brainLimits.html.

[13] M. Fischetti, "Computers versus Brains," Scientific American, 25 Oct. 2011. [Online]. Available: http://www.scientificamerican.com/article.cfm?id=computers-vs-brains.

[14] C. Mead, "Neuromorphic electronic systems," Proc. IEEE, vol. 78, no. 10, pp. 1629-1636, Oct. 1990.

[15] J. Lu, "An analog VLSI deep machine learning implementation," Ph. D. Dissertation, University of Tennessee, Mar. 2014.

[16] R. Sarpeshkar, "Analog versus digital: extrapolating from electronics to neurobiology," Neural Comput., vol. 10, pp. 1601-1638, Oct. 1998.

[17] W. Bialek, et al., "Reading a neural code," Science, vol. 252, pp. 1854-1857, June 1991.

[18] R. R. de Ruyter van Steveninck, et al., "Reproducibility and variability in neural spike
trains," *Science*, vol. 275, pp. 2406-2419, 1997.

[19] M. van Rossum, "Effects of noise on the spike timing precision of retinal ganglion cells," *J. Neurophysiology*, vol. 89, pp. 2406-2419, 2003.

[20] J. Chang, et al., "A 20nm 112Mb SRAM in high-κ metal-gate with assist circuitry for low-leakage and low-VMin applications," *ISSCC Dig. Tech. Papers*, pp. 316-317, Feb. 2013.

[21] P. Pavan, et al., "Flash memory cells—an overview," *Proc. of IEEE*, vol. 85, no. 8, pp. 1248-1271, Aug. 1997.

[22] H. P. McAdams, et al., "A 64-Mb embedded FRAM utilizing a 130-nm 5LM Cu/FSG logic process," *IEEE J. Solid-State Circuits*, vol. 39, no. 4, pp. 667-677, Apr. 2004.

[23] "Overview for FRAM Series MCU," TI, [Online]. Available: http://www.ti.com/litds/ti/microcontroller/16-bit_msp430/fram/overview.page. [Accessed Sep. 2013].

[24] T-Y. Liu, et al., "A 130.7mm² 2-layer 32Gb ReRAM memory device in 24nm technology," *ISSCC Dig. Tech. Papers*, pp. 210-211, Feb. 2013.

[25] M. Jefremow, et al., "Time-differential sense amplifier for sub-80mV bitline voltage embedded STT-MRAM in 40nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 216-217, Feb. 2013.

[26] J. Lu and J. Holleman, "A wideband ultra-low-current on-chip ammeter," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sept. 2012, pp. 1-4.

[27] R. R. Harrison, J. A. Bragg, P. Hasler, B. A. Minch and S. P. Deweerth, "A CMOS programmable analog memory-cell array using floating-gate circuits," *IEEE Trans. Circuits Syst.II, Analog Digit. Signal Process.*, vol. 48, no. 1, pp. 4-11, Jan. 2001.

[28] B. K. Ahuja, et al., "A very high precision 500-nA CMOS floating-gate analog voltage reference," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2364-2372, Dec. 2005.
[29] L. R. Carley, "Trimming analog circuits using floating-gate analog MOS memory," *IEEE J. Solid-State Circuits*, vol. 24, no. 6, pp. 1569-1575, Dec. 1986.

[30] S. Peng, P. Hasler and D. V. Anderson, "An Analog programmable multidimensional radial basis function based classifier," *IEEE Trans Circuits and Syst. I, Reg Papers*, vol. 54, no. 10, pp. 2148-2158, Oct. 2007.

[31] P. Hasler and J. Dugger, "An analog floating-gate node for Supervised learning," *IEEE Trans Circuits and Syst. I, Reg Papers*, vol. 52, no. 5, pp. 834-845, May 2005.

[32] M. Figueroa, S. Bridges, D. Hsu and C. Diorio, "A 19.2 GOPS mixed-signal filter with floating-gate adaptation," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1196-1201, July 2004.

[33] C. Diorio, "A p-channel MOS synapse transistor with self-convergent memory writes," *IEEE Trans. Electron Dev.*, vol. 47, no. 2, pp. 464-472, Feb. 2000.

[34] J. Lu and J. Holleman, "A floating-gate analog memory with bidirectional sigmoid updates in a standard digital process," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2013, vol. 2, pp. 1600-1603.

[35] T. Yamasaki and T. Shibata, "Analog soft-pattern-matching classifier using floating-gate MOS technology," *Neural Networks, IEEE Transactions on*, vol. 14, no. 5, pp. 1257-1265, Sept. 2003.

[36] K. Kang and T. Shibata, “An on-chip-trainable Gaussian-kernel analog support vector machine,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 7, pp. 1513-1524, Jul. 2010.

[37] J. Lu, S. Young, I. Arel and J. Holleman, "A 1TOPS/W analog deep machine-learning engine with floating-gate storage in 0.13μm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 504-505.

[38] T. Delbruck, "'Bump' circuits for computing similarity and dissimilarity of analog
voltages," in *Proc. Int. Joint Conf. on Neural Networks*, Jul. 1991, pp. 475-479.

[39] K. Lee, J. Park, G. Kim, I. Hong and H.-J. Yoo, "A multi-modal and tunable Radial-Basis-Function circuit with supply and temperature compensation," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2013, pp.1608-0611.

[40] F. Li, C.-H. Chang and L. Siek, "A very low power 0.7 V subthreshold fully programmable Gaussian function generator," in *Proc. Asia Pacific Conf. on Postgraduate Research in Microelectronics and Electron.*, Sept. 2010, pp. 198-201.

[41] J. Lu, T. Yang, M. Jahan and J. Holleman, "Nano-power tunable bump circuit using wide-input-range pseudo-differential transconductor," *Electron. Lett.*, vol. 50, no. 13, pp. 921-923, 2014.

[42] P. Furth and A. Andreou, "Linearised differential transconductors in subthreshold CMOS," *Electron. Lett.*, vol. 31, no. 7, pp. 545-547, Mar. 1995.

[43] Z. Wang and W. Guggenbuhl, "A voltage-controllable linear MOS transconductor using bias offset technique," *IEEE J. Solid-State Circuits*, vol. 25, no. 1, pp. 315-317, Feb. 1990.

[44] A. Nedungadi and T. R. Viswanathan, "Design of linear CMOS transconductance elements," *IEEE Trans. Circuits Syst.*, vol. 31, no. 10, pp. 891-894, Oct. 1984.

[45] J. Pennock, "CMOS triode transconductor for continuous-time active integrated filters," *Electron. Lett.*, vol. 21, no. 18, pp. 817-818, Aug. 1985.

[46] D. J. C. MacKay, Information Theory, Inference and Learning Algorithms, New York, NY, USA: Cambridge University Press, 2003.

[47] S. Chakrabartty and G. Cauwenberghs, "Sub-microwatt analog VLSI trainable pattern classifier," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1169-1179, May 2007.

[48] R. Chawla, A. Bandyopadhyay, V. Srinivasan and P. Hasler, "A 531nW/MHz, 128x32 current-mode programmable analog vector-matrix multiplier with over two decades of
linearity," in Proc. IEEE Custom Integr. Circuits Conf. (CICC), Oct. 2004.

[49] J. Lubkin and G. Cauwenberghs, "A micropower learning vector quantizer for parallel analog-to-digital data compression," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 1998, pp. 58-61.

[50] J. Lu, S. Young, I. Arel and J. Holleman, "An analog online clustering circuit in 130nm CMOS," in Proc. IEEE Asian Solid-State Circuits Conference (A-SSCC), Nov. 2013, pp. 177-180.

[51] "Machine Learning Surveys," [Online]. Available: http://www.mlsurveys.com/.

[52] I. Arel, D. Rose and T. Karnowski, "Deep machine learning - a new frontier in artificial intelligence research," Computational Intelligence Magazine, IEEE, vol. 5, no. 4, pp. 13-18, 2010.

[53] J. Bergstra, F. Bastien, O. Breuleux, P. Lamblin, R. Pascanu, O. Delalleau, G. Desjardins, D. Warde-Farley, I. Goodfellow, A. Bergeron and Y. Bengio, "Theano: deep learning on GPUs with Python," in Big Learning Workshop, NIPS'11, 2011.

[54] J. Oh, G. Kim, B.-G. Nam and H.-J. Yoo, "A 57 mW 12.5 µJ/Epoch embedded mixed-mode neuro-fuzzy processor for mobile real-time object recognition," IEEE J. Solid-State Circuits, vol. 48, no. 11, pp. 2894-2907, Nov. 2013.

[55] J. Park, I. Hong, G. Kim, Y. Kim, K. Lee, S. Park, K. Bong and H.-J. Yoo, "A 646GOPS/W multi-classifier many-core processor with cortex-like architecture for super-resolution recognition," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2013, pp. 17-21.

[56] J.-Y. Kim, M. Kim, S. Lee, J. Oh, K. Kim and H.-J. Yoo, "A 201.4 GOPS 496 mW real-time multi-object recognition processor with bio-inspired neural perception engine," IEEE J. Solid-State Circuits, vol. 45, no. 1, pp. 32-45, Jan. 2010.

[57] J. Lu, S. Young, I. Arel and J. Holleman, "A 1 TOPS/W analog deep machine-learning...
engine with floating-gate storage in 0.13 μm CMOS," IEEE J. Solid-State Circuits, vol. 50, no. 1, pp. 270-281, Jan. 2015.

[58] S. Young, J. Lu, J. Holleman and I. Arel, "On the impact of approximate computation in an analog DeSTIN architecture," IEEE Trans. Neural Netw. Learn. Syst., vol. 25, no. 5, pp. 934-946, May. 2014.