GrateTile: Efficient Sparse Tensor Tiling for CNN Processing

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Abstract—We propose GrateTile, an efficient, hardware-friendly data storage scheme for sparse CNN feature maps (activations). It divides data into uneven-sized subtensors and, with small indexing overhead, stores them in a compressed yet randomly accessible format. This design enables modern CNN accelerators to fetch and decompressed sub-tensors on-the-fly in a tiled processing manner. GrateTile is suitable for architectures that favor aligned, coalesced data access, and only requires minimal changes to the overall architectural design. We simulate GrateTile with state-of-the-art CNNs and show an average of 55% DRAM bandwidth reduction while using only 0.6% of feature map size for indexing storage.

Index Terms—Neural Network Hardware, Data Compression, Sparse Matrix.

I. INTRODUCTION

Convolutional neural networks (CNNs) are now considered one of the most widely used machine learning techniques in computer vision and image processing [1]–[5]. Its primary operation is the convolution between kernels (weights) and feature maps (activations), which can consume lots of power through MAC operations and memory accesses. To alleviate this problem, one can take advantage of the redundancies in the feature maps and skip unnecessary processing with sparse computation. For example, neural networks using the ReLU activation function may have highly sparse feature maps with up to 80% zero values clipped from negative values. It is also possible to fine-tune the network to generate kernels with higher sparsity [6], [7], so that CNN accelerators can reduce operation waste by gating the processing elements (PEs) and avoid scheduling zero operations [6], [8], [9].

Compared with the energy wasted through redundant operations, data access power is arguably more critical for future accelerator designs because memory bandwidth has been growing slower than the speed of PEs [10]. That is, an algorithm can become increasingly memory bound for future architectures. Newer networks tend to adopt smaller convolution kernels with deeper layers, which further reduces operation count at the cost of increased memory usage. In Fig. 1 we calculate the power consumption breakdown according to [11] by simulating several popular CNNs with SCALE-sim on a 16 × 16 systolic array [12]–[14]. Notice that the percentage of MAC power decreases from 35% in 2012 to 15% in 2016, while the DRAM feature read consistently consumes over half of the remaining power. Modern CNN accelerators have already utilized on-chip SRAM to effectively reduce data access power (Fig. 2a). To push the envelope further, we could compress the feature maps, but the compression scheme may not be compatible with the tiled processing nature of modern CNN accelerators (Fig. 2b). A better approach is to divide the feature maps into independently compressed subtensors to make them randomly-accessible for tiled processing (Fig. 2c). This design principle allows the memory controller to fetch only the required subtensors and assemble them into tiles on-the-fly, without wasting bandwidth on over-fetching data outside of the tiles.

After analyzing how CNN architectures divide, compress, and store the feature maps [15], [16], we observe that the division and storage process has an equally if not more substantial impact on the overall DRAM bandwidth when compared with the compression algorithms for individual subtensors. Fig. 3 illustrates the trade-off between using a larger subtensor size, which causes wasted fetch (Fig. 3a), and a smaller subtensor size which causes data fragmentation (Fig. 3b). To break free from this trade-off, we propose GrateTile, which divides the feature maps into uneven sizes for optimal CNN processing (Fig. 3c). By inserting smaller subtensors between larger tensors, GrateTile combines the storage efficiency of larger subtensors without the over-fetching waste. By adding GrateTile functionality to existing CNN accelerators, we can gain approximately 55% bandwidth improvement over the uncompressed baseline, and 6-27% bandwidth improvement over compressed tiles according to our simulation. In summary, our contributions are:

- A bandwidth-efficient storage scheme for sparse feature
maps with CNN accelerator-friendly memory access patterns,
- A universal methodology to convert a sparse tensor into the GrateTile packing given CNN layer and accelerator configurations, and
- A method for integrating GrateTile into existing accelerators with small hardware modification and overhead.

II. RELATED WORKS

While GrateTile focuses on exploiting feature map sparsity that tends to be dynamic, kernel sparsity tends to be more static. Researchers have gained great success exploiting this attribute to reduce DRAM bandwidth and power consumption for CNNs. These methods operate by dropping small kernel values followed by retraining to compensate for accuracy loss. Many of these works also focus on designing PEs that can skip unnecessary MAC or math operations to save power. EIE [6] is a fully-connected layer accelerator, which uses two indices for the next non-zero values in the feature maps and kernels so that it only performs operations with non-zero operands. Several CNN accelerators also apply similar methods to skip unnecessary operations [8], [17]. This processing flow forces serialization of operation for different kernel values and therefore limits the parallelism. SCNN decomposes a matrix multiplication or a CNN into several outer product operations [9] and is thus an outer product PE array. Since the outer product is zero when either kernel or feature map is zero, it compacts the input to ensure there is no wasted operation. However, since the output address from each PE is different, this causes irregular address calculation and results in a distribution unit that is three times larger than the PE array.

The methods above assume the zero values can appear randomly. On the other hand, some researchers believe the sparsity can be structural, and subtensors of kernel tensors may repeatedly appear in different positions. CirCNN and PermDNN assume any row in the kernel tensor is a rotation of its neighboring row [18], [19]. These repeating structure of kernel tensors enable many methods for reducing operation count, such as replacing the multiplication by table lookup. Wu et al. use the vector quantization to cluster kernels by k-means and replace them by their cluster center indices to save memory [20].

III. GrateTile FOR SPARSE FEATURE MAPS

A. The Need for Hardware Aligned Storage

As discussed before in Fig. 3 to support tiled CNN processing, we need to divide the feature maps into subtensors and
compress them independently. Many architectures adopt simple compression algorithms such as bitmask or zero run-length coding (ZRLC) \[8\], \[15\]–\[17\] with uniform division scheme for the tensors (Fig. 4). While suitable for hardware implementation, this can lead to a waste of memory bandwidth. Even though the convolution operation only requires data from surrounding pixels (\textit{i.e.}, halo), we may end up fetching the entire neighboring subtensors because the compressed blocks are not randomly accessible (Fig. 3a). Furthermore, modern memory hierarchies, like DRAM or cache, favor aligned and coalesced access, and the variable size of compressed data can result in fragmentation and wasted bandwidth. We can reduce fragmentation with index memory (Fig. 5b), but this pointer index can be too big for the on-chip SRAM, or contribute to additional latency and bandwidth if stored in the DRAM.

Fig. 6a shows how GrateTile can eliminate both the aforementioned problems. By unevenly dividing the subtensors, we have fewer subtensors and smaller index memory sizes, while ensuring proper boundary alignment for tiled processing. Next, we explain the methodology for finding an optimal division given a CNN and the hardware configuration.

### B. Computing GrateTile Configuration

Consider a CNN architecture processing a $3 \times 3$ convolution on 4 input channels, using an $8 \times 8$ tile size for the output feature map (Fig. 3a). Our goal is to create a feature map division that (1) avoids accessing partially compressed subtensors, and (2) minimizes the number of subtensors to reduce data fragmentation. In this example, to compute the first output tile, we need to fetch a $10 \times 10 \times 4$ input tile (Fig. 4a). When processing the next output tile, we would step toward the right by 8 elements on the feature map (Fig. 5b) to fetch the next input tile. Since the step size is constant within one layer of CNN processing, the left (orange) and right (cyan) access boundaries form two arithmetic progressions, denoted as $B_L = \{-1, 7, 15 \cdots\}$ and $B_R = \{9, 17, 25 \cdots\}$. The GrateTile configuration is simply the divisions formed by both boundaries, namely the union $G = B_L \cup B_R$, or simply $G = \{1, 7\} \mod 8$, as shown in Fig. 5c. Because $7 - 1 = 6$ and $1 - 7 = 2 \mod 8$, each spatial dimension of the feature map is divided into two uneven sizes of 2 and 6, which results in four subtensor shapes—$6 \times 6$, $2 \times 6$, $6 \times 2$, and $2 \times 2$. A $10 \times 10$ window is then composed of one $6 \times 6$, two $2 \times 6$ and $6 \times 2$, and four $2 \times 2$ subtensors. Also, since the halo only appears in the spatial dimension, this division process is not necessary along the channel dimension.

We now generalize this example for all modern CNN layers, whose computations can be defined by the following three parameters:

- **Kernel size**—denoted as $2k + 1$ since kernel sizes tend to be odd integers.
- **Two output elements** convolving two windows with a stride of $s$. When $s > 1$, it means a smaller output feature map and thus less computation cost.
- **Dilated CNN** \[21\] convolves strided input elements for one output element to enlarge the equivalent window size, and we denote this stride as $d$.

Besides, we denote the output tile size as $t_h \times t_w$. Fig. 6a shows a CNN with $d = 1$. To compute the leftmost output element, we fetch from the feature map a window starting at the left boundary of $-k$ and right boundary of $(t_w - 1)s + k + 1$. Since the offset between two neighboring subtensors is $st_w$, we can define the GrateTile configuration as follows

$$G = \{-k, (t_w - 1)s + k + 1\} \mod st_w$$

$$= \{-k, k - s + 1\} \mod st_w \quad \text{(1)}$$

For dilated CNN shown in (Fig. 6b), a similar process yields

$$G = \{-kd, kd - s + 1\} \mod st_w.$$ 

An interesting property for GrateTile is that any configuration for mod $N$ is also valid for mod $N'$ if $N' | N$. For example, consider an AlexNet CONV1 whose $(k, s, t_w) = (5, 4, 8)$, its GrateTile configuration is $G = \{27, 2\} \mod 32$, but $G = \{3, 2\} \mod 8$ is also a valid GrateTile configuration. In the extreme case, the GrateTile degenerates to Fig. 2c when $N' = 1$. It is thus possible to use a single $N$ across all CNN layers to keep the hardware implementation simple.
and we show that $N = 8$ can be a suitable choice for most purposes in Section IV.

### C. Memory Layout for Compressed Subtensors

Given a GrateTile configuration, we need to store these subtensors in a data structure that complies with the memory alignment requirement to maximize the benefits of compression. Since subtensors can have different compressed sizes, we have to store the extra metadata (e.g., pointers in Fig. 3) separately from the compressed subtensors. Such metadata are usually too large to fit into the SRAM. For example, the size of metadata would be 72 kB for AlexNet CONV2 if each subtensor contains 8 words and requires a 32-bit pointer. Therefore, a more reasonable choice for metadata storage would be in the DRAM. However, we must be careful since fetching them would cause extra bandwidth and access latency.

Fig. 7(a) shows how we store the subtensors and metadata. Since GrateTile is a near-uniform subtensor division methodology, it is relatively straightforward to extend the data structure from uniform division (Fig. 7a) for our purposes. For example, a GrateTile configuration $G = \{1, 7\} \pmod{8}$ is equal to dividing every $8 \times 8$ subtensors further into four small subtensors, and therefore its metadata would extend from the uniform division structure for size 8. With uniform division, every subtensor has a pointer to the starting address of the subtensor. We extend this structure by adding the compressed sizes of the four smaller neighboring subtensors. Thus, accessing these subtensors is a two-step procedure, where we first locate the starting address from the pointer and then add the subtensor sizes to get the actual offset for each subtensor.

We now calculate the size of the metadata as follows. As shown in Fig. 7a in a uniform subtensor division, we need a pointer for each $8 \times 8 \times 8 = 512$ words. Since GrateTile only stores these subtensors in aligned addresses, given a 32-bit addressing space with a 16-byte cache alignment, the size of the pointer is $32 - \log_2 16 = 28$. We now extend this to the GrateTile division and represent the sizes of the four neighboring subtensors by the number of 16-byte cache lines it used. For this purpose, different GrateTile configurations yield different subtensor sizes, which may require different numbers of bits. To this end, we select the maximum number among the GrateTile configurations supporting popular CNN kernel sizes. For kernel sizes 3, 7 and 11, we have $G = \{1, 7\} \pmod{8}$, and a 512-word uniform subtensor divides into four subtensors of sizes 64, 192, 192, and 576 bytes, requiring $3 + 4 + 4 + 6 = 17$ bits of metadata. For kernel sizes 5 and 9, we have $G = \{2, 6\} \pmod{8}$, which requires $5 + 5 + 5 + 5 = 20$ bits of metadata. Therefore, for every 512 words of feature map stored in GrateTile format, we need $28 + 20 = 48$ bits of metadata, which represents only 0.6% of overhead.

### IV. Evaluations

In this section, we discuss the bandwidth reduction with GrateTile in sparse CNN processing compared with several uniform division methods used by other CNN accelerators [15], [16]. We simulate memory fetch patterns of representative layers from popular CNN networks [11–4]:

- **AlexNet**: All layers, except for the first input layer since it takes dense input images.
- **VGG 16**: The layers right before the pooling layers.
- **ResNet 18**: The layers right after the pooling layers.
- **ResNet 50**: The downsampling CNN layers and the layers before them.
- **VDSR**: Every four layers of VDSR, since it consists of 18 layers of the same shape.

Fig. 8 illustrates the geometric mean of bandwidth savings from these benchmarks. We use the bitmask compression and the mod 8 GrateTile configuration for this experiment; we shall discuss the logic behind the selection of this number later. Note that GrateTile saves an average of 55% feature map accessing bandwidth, which represents 6-27% more savings than uniform subtensor division. We discuss the details of how we arrive at these results in the remainder of this section, as well as insights from our experiments.

#### A. Experiment Setup

We perform our simulation on two types of hardware platforms that are characteristics of CNN architectures, namely, an NVIDIA GPU and the Eyeriss architecture. We assume the memory alignment size is 8 words (128 bits), which is in line with the AXI bus width of [15]. NVIDIA GPUs also adopt a similar alignment configuration, which is 8 floating numbers (256 bits) per one L1-cache line. To determine the
maximum processing tile size, we must consider both double buffering (prefetching) and convolutional kernels, and assume a reasonable processing tile of less than one-fourth of the buffer size. Therefore in the following experiments, for an NVIDIA Volta architecture with 64 KB shared memory in one of its processor array, we define the small tile (NVIDIA) configuration to hold a 4K-word feature map subtensor. For Eyeriss with a 108 KB global buffer, we define the large tile (Eyeriss) configuration to hold 16K words.

Fig. 9 illustrates a bandwidth reduction breakdown of Fig. 8 for individual network layers. Table I shows the processing tile size and GrateTile configuration for various CNN layers. We compare GrateTile with uniform subtensor division schemes ranging from 1 × 1 × 8 to 8 × 8 × 8, under both the small and large tile configurations. All subtensors are aligned with the cache lines except for the 1 × 1 × 8 division, where we compactly the subtensors because each subtensor is too small to fill up one cache line. Table II and III show the bandwidth overhead caused by fetching the metadata.

**B. Discussions**

From these experiments, we can obtain several useful insights:

(1) **Tile size and bandwidth reduction.** For uniform tensor division, an optimal division size does not exist because it is a trade-off between the partial tensor accesses and the data indexing overhead. For example, the larger uniform 8 × 8 × 8 division can derive the most benefits by going with larger processing tiles, resulting in a bandwidth improvement of 13% (40.9% - 27.9%). In comparison, a smaller uniform division like 2 × 2 × 8 does not derive similar benefit with larger processing tile (40.2%-40.1% = 0.1%); it also consumes much more metadata than the 8 × 8 × 8 division. Since GrateTile uses a small number of subtensors to prevent partial tensor accesses, it outperforms the best uniform division methods (4 × 4 × 8) according to Fig. 8 and Table III.

(2) **Metadata overhead.** In Table II we calculate the metadata required for every 8 × 8 × 8 = 512-word feature map and extrapolate the results to different division methods. In Table III we show the results with and without the bandwidth overhead caused by accessing the metadata. Observe that without the overhead, the bandwidth saving generally becomes better as the uniform subtensor sizes get smaller. The only exception is 2 × 2 × 8 for large tile configuration due to its cache fragmentation (Fig. 3c). The compacted 1 × 1 × 8 division can be considered as a performance upper-bound since there is neither partial cache or partial cache accesses, and GrateTile mod 8 is only 1.8% worse than this upper-bound. However, the 1 × 1 × 8 division adds 24.4% metadata fetching overhead, making it performs the worst compared with other division methods.

(3) **Limitations and GrateTile configuration.** Because GrateTile is best suited for tile-based CNN processing, adopting GrateTile may need to bandwidth overhead by creating unnecessary subtensor division, for example, if an accelerator processes a whole channel before the next channel. In this scenario, a tile and a feature map have the same sizes at the spatial dimensions, which happens in layers like AlexNet CONV5 or VGG 16 CONV5_3 where a uniform division subtensor (16 × 16) can contain the whole input feature map (14 × 14). For these layers, using GrateTile requires 4% more bandwidth than not dividing the subtensor at all. It also explains why the mod 16 GrateTile has slightly better performance (56.0%-54.1% = 1.9%) than mod 8 in Table III. However, this subtensor division does not work in the smaller tile hardware configuration, which implies a large workspace requirement to compress the subtensors. Therefore, we claim that the mod 8 GrateTile is a reasonable choice for most network layers and hardware configurations.

**V. Conclusions**

We propose GrateTile, a hardware-friendly methodology for storing and accessing compressed, sparse feature maps. GrateTile divides feature maps into uneven subtensors, and in the process, avoids wasteful fetches of partial subtensors and partial cache lines. Furthermore, it only requires a small metadata indexing overhead to keep track of the
locations of the compressed subtensors. It can be a simple-yet-effective modification for existing CNN accelerators since it is mostly independent of the compression algorithms and requires changes only to the existing feature map division methods. Our experiments show that GrateTile can save up to 55% more bandwidth than the baseline and 6-27% compared with uniform subtensor division methods.

For hardware compression and decompression, our preliminary SystemVerilog implementation shows promising area efficiency compared to ZRLC, bitmask, and dictionary-based algorithms, with better scalability and less serialization. We will continue to investigate in this front and share our findings with the community.

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