An accurate and flexible analog emulation of AdEx neuron dynamics in silicon

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Abstract—Analog neuromorphic hardware promises fast brain emulation on the one hand and an efficient implementation of novel, brain-inspired computing paradigms on the other. Bridging this spectrum requires flexibly configurable circuits with reliable and reproducible dynamics fostered by an accurate implementation of the targeted neuron and synapse models. This manuscript presents the analog neuron circuits of the mixed-signal accelerated neuromorphic system BrainScaleS-2. They are capable of accurately reproducing the original model dynamics and can be configured for a wide range of parameterizations.

Index Terms—analog neuromorphic, AdEx, silicon neuron

I. INTRODUCTION

SPIKING neuron models attempt to replicate the time-continuous dynamics and the event-based, asynchronous communication scheme of their archetype. Building on the simpler leaky integrate-and-fire (LIF) equation, the AdEx model captures these fundamental properties and can reproduce many of the dynamics and firing patterns found in electrophysiological recordings of biological neurons [1]. It describes the dynamics of the membrane potential $V$ as

$$ C \frac{dV}{dt} = -g_l (V - E_l) + g_d \Delta_T e^{\frac{V - V_T}{\alpha_T}} - w + I, \quad (1) $$

with membrane capacitance $C$, leak potential $E_l$, leak conductance $g_l$, soft threshold $V_T$, and exponential slope $\Delta_T$. The dynamics of the adaptation current $w$ are governed by

$$ \tau_w \frac{dw}{dt} = a (V - E_l) - w, \quad (2) $$

with time constant $\tau_w$ and subthreshold adaptation strength $a$. The time-continuous dynamics are accompanied by spike-triggered jump conditions $V \rightarrow V_r$ and $w \rightarrow w + b$.

Synaptic interaction is typically modeled by weighting and accumulating the presynaptic spike trains of each synapse $i$, $S_i(t) = \sum_j \delta(t - t_j)$, and by convolving them with an interaction kernel, typically an exponential decay $s(t) = \sum_i w_i S_i(t) \exp(t/\tau_{syn})$. This integrator trace is then translated into a current onto the membrane either directly (current-based) or by modulating a conductance pulling the membrane towards a synaptic reversal potential (conductance-based):

$$ I_{cuba} = I \cdot s(t), \quad \text{or} \quad I_{coba} = g \cdot s(t) \cdot [E_{syn} - V]. \quad (3) $$

The AdEx equations and other complex neuron models have inspired a plethora of analog neuromorphic implementations [2]–[6] and also lay the foundation for the silicon neuron presented in this manuscript. The discussed silicon neuron can accurately reproduce the original model dynamics and can be configured for a wide range of parameterizations.

The neuron circuits represent one of the central components of the analog core of BrainScaleS-2 (Fig. 1 A), a mixed-signal neuromorphic system emulating neuronal and synaptic dynamics on 1000-fold accelerated time scales compared to the biological nervous system. The silicon neurons are embedded into the rich infrastructure provided by the neuromorphic ASIC (Fig. 1 B). They receive weighted stimuli via the synapse array and relay their output spikes to the chip-internal event routing fabric. While partially controlled and interfaced through full-custom digital backend logic (Fig. 1 C), the neuronal dynamics are realized by analog circuits.

II. SILICON IMPLEMENTATION

The design can be separated into multiple functional blocks mainly corresponding to the individual terms of the model equations. The circuit is implemented in a 65 nm bulk comple-

![Fig. 1. (A) Photograph of a BrainScaleS-2 ASIC. (B) Block-level schematic of the neuromorphic system. (C) Block-level schematic of the silicon neuron.](image-url)
mentary metal-oxide-semiconductor (CMOS) technology and occupies an active silicon area of approximately 2575 µm².

A. Bulk-driven OTA as a building block

The mostly linear nature of the differential equations behind the model dynamics emphasizes the need for an area- and energy-efficient, widely linear component, mainly to translate voltages into proportional currents. For that purpose, preceding silicon neurons have often already relied on operational transconductance amplifiers (OTAs) [6], [7]. Saturation effects and the limited linear range of standard OTA designs, however, can dramatically distort the underlying dynamics when compared to the original model equations. The presented circuits address this issue by relying on a bulk-driven differential pair (M1, M2) to linearize the characteristics of the OTA (Fig. 2 A). Bulk-driven circuits exploit the body effect to modulate a transistor’s drain current [8]. In the present case, we make use of the reduced transconductance $g_{mb} \ll g_m$ to increase the linear input range of the OTA (Fig. 2 B), lifting the requirement for more complex and less area- or energy-efficient linearization techniques but requiring careful biasing and verification to always maintain reverse biased body diodes. Depending on the exact, application-specific dimensioning, the discussed circuit exhibits a footprint down to less than $10 \times 10 \mu m^2$, despite the requirement for isolated and thus spatially separated n-wells for the two transistors of the differential pair. It serves with only slight modifications to the specific instantiation as a common building block for the silicon neuron, e.g. realizing the leak conductance of the membrane dynamics (Equation (1)).

B. Adaptation

The adaptation state variable $w$ (Equation (2)) also resembles leaky integrator dynamics. While taking the form of a current in the model equations, it is in our silicon neuron represented as a voltage $V_w$. The core dynamics are, hence, implemented through a low-pass filter, directly relying on a capacitor and the bulk-driven OTA as a pseudo-conductance (Fig. 3 A), allowing to tune the adaptation time constant through its bias (Fig. 3 B). We fitted OTA2 with a second, approximately twelve-fold stronger output stage to repurpose the circuit to also generate the adaptation current $I_w = \frac{g_w}{g_m} (V_{ref} - V_w)$ directed onto the membrane.

The adaptation state is driven by the membrane-dependent subthreshold contributions on one hand and spike-triggered increments on the other. The former are realized through

\[
\tau_w \frac{dI_w}{dt} = -\tau_w \frac{dV_w}{dt} = \pm g_w \frac{g_m}{g_a} \cdot \left( V_m - E_1^{\text{adapt}} \right) - I_w , \quad (4)
\]

with $\tau_w (I^*_b) \equiv C_w/g_a (I^*_b)$. These dynamics are augmented by spike-triggered in- or decrements of $V_w$ resulting from short current pulses $I_b$ with configurable width and amplitude.

C. Exponential feedback current

The exponential term is in its core implemented through the characteristics of a single metal-oxide-semiconductor field-effect transistor (MOSFET) biased in weak inversion (Fig. 4 A, M4). Its gate-to-source voltage is derived from the membrane via an OTA and a subsequent current-to-voltage conversion implemented straight-forwardly through a long-channeled transistor (M3) biased to operate in its linear region and thus acting as a resistor with on-resistance $r_{conv}$. This compact conversion circuit allows tuning the exponential current’s onset and slope (Fig. 4 B, 4 C):

\[
I_{\text{exp}}(V_m) = I_0 \cdot \exp \left( \frac{8 \cdot g_{ota} \cdot \left| V_m - V_{\text{exp}} \right|}{n \cdot V_T / r_{\text{conv}}} \right) . \quad (5)
\]

This current is mirrored onto the membrane and can be gated either to disable the whole circuit or to “pause” the strong exponential feedback during the neuron’s refractory period. The current mirror formed by M1 and M2 rectifies the output current of OTA1 and, hence, effectively powers down the second half of the circuit for membrane potentials significantly below $V_T$.

D. Emulating current- and conductance-based synapses

The synaptic integrator circuits (Fig. 5 A) represent the interface between the synapse array and the neuron’s membrane circuits. They integrate current pulses from their associated

Fig. 2. (A) Bulk-driven OTA serving as a building block for the silicon neuron (simplified schematic). (B) Small signal transconductance measured for different bias currents.

Fig. 3. (A) Schematic of the adaptation circuit. (B) Trajectory of the adaptation voltage after clamping and releasing from a fixed potential, measured for different bias currents. (C) Transient response of a membrane to a step current measured for different subthreshold adaptation strengths.
column of synapses [9] and modulate the membrane in analogy to Equation (3). Here, the low-pass filter directly exploits the synaptic line’s capacitance, which can optionally be augmented with a dedicated capacitor. The conductance (in Fig. 5A schematically drawn as a variable resistor) is realized through multiple series-connected p-channel MOSFETs. They are biased in weak inversion to a constant gate-to-source voltage, similar to the predecessor circuit [6].

OTA1 derives a current $I_{\text{syn}} = g_1 \cdot \Delta V_{\text{syn}}$ based on the deflection of the integrator voltage, directly implementing a current-based output. In that process, offsets can be compensated by tuning the voltage drop of the two source followers (M1, M2) via their bias currents. Conductance-based synapses (Fig. 5B) are realized via an additional feedback path: OTA2 can modulate the bias current of OTA1 based on the membrane potential such that

$$g_1 \propto g_2 \cdot \left( \frac{E_{\text{syn}} + I_{\text{syn}}/g_2}{E_{\text{syn}}} - V_m \right),$$  

where $g_1$ is assumed to be approximately proportional to the applied bias current. Mixing the static bias current with an additional, modulated component allows to create a “virtual” reversal potential $E_{\text{syn}}$. In the excitatory case, the latter usually extends far beyond the threshold voltage and thus falls outside the membrane’s dynamic range. Our design decouples the true zero crossing — and with it the linear range — of OTA2 from that normally never reached reversal potential.

III. RESULTS

The neuron circuit’s dynamics can be tuned via 16 analog bias currents and 8 voltages individually provided for each neuron instance and a set of digital controls (40 bit of local static random-access memory (SRAM)) to enable or disable parts of the circuit. This large configuration space allows the flexible emulation of a wide range of model dynamics. Table I summarizes the parameter ranges achieved by the neuron design, measured across 128 neurons. The effective parameter ranges can in many cases be further extended by selecting a reduced membrane capacitance, here configured for its maximum value of approximately 2.47 pF.

With each neuron instance receiving an individual set of analog references generated by the on-chip parameter storage [10], one may not only precisely tune the operating points to certain target dynamics but can also compensate for process corner effects as well as mismatch-induced fixed-pattern variability across neurons, a process we refer to as calibration. The flexible parameterization and calibration allows to configure the neuron circuits for a wide range of operating points. In the following, we will demonstrate the reliability and accuracy of the silicon neuron and for that purpose, in each case, discuss the dynamics of a population of 128 calibrated neurons.

A. LIF neuron dynamics

Calibrating the neuron circuits to a leak-over-threshold regime exhibits well-matching dynamics (Fig. 6A) and narrow inter-spike interval (ISI) distributions (Fig. 6B). The ISIs furthermore closely correspond to those predicted by evaluating the original model equations based on the calibration targets, here measured for membrane time constants spanning two full orders of magnitude (Fig. 6C).

A calibration of the synaptic input circuits, namely of $\tau_{\text{syn}}$, their effective amplitudes, and offsets, yields similarly well-

![Fig. 4. (A) Exponential term. (B) & (C) The exponential current is correctly reproduced across three orders of magnitude and can be parameterized via the reference potential and the OTA’s bias. Saturation of the OTA, the current-to-voltage conversion, and the output stage limits $I_{\text{exp}}$ but – due to the overall fast transients – does not significantly impact spike timing.](image)

![Fig. 5. (A) Simplified synaptic input circuit. (B) Postsynaptic potentials measured for various membrane potentials, implementing conductance-based synaptic interaction.](image)

| Parameter | Minimum | Maximum | Unit |
|-----------|---------|---------|------|
| membrane time constant $\tau_m$ | 0.6 ± 0.2 | 915 ± 140 | µs |
| leak potential $E_l$ | 0.0 | 1.0 | V |
| firing threshold $V_l$ | 0.2 | 1.2 | V |
| stimulus current $I_{\text{stim}}$ | 0.0 | 121 ± 14 | nA |
| synaptic time constant $\tau_{\text{syn}}$ | 0.29 ± 0.03 | 538 ± 98 | µs |
| synaptic peak current $I_{\text{syn}}$ | 0.033 ± 0.003 | 1.15 ± 0.03 | µA |
| adaptation time constant $\tau_w$ | 22 ± 3 | 853 ± 117 | µs |
| subthreshold adaptation $|a|$ | 30 ± 4 | 1065 ± 114 | µS |
| spike-triggered adapt. $|b|$ | 0 | $\infty$ | µA |
| exponential slope $\Delta_T$ | 13 ± 2 | >91 ± 46 | mV |
matching postsynaptic currents. This results in homogeneous postsynaptic potential (PSP) trajectories (Fig. 6 D), leaving the membrane’s resting potential mostly unaffected (Fig. 6 E) and yielding closely matching amplitudes (Fig. 6 F).

B. AdEx firing patterns

We benchmarked the full AdEx circuits by seeking to reproduce the different firing patterns discussed by Naud, Marcille, Clopath, et al. [1]. With only few exceptions, we relied on the originally published parameter sets and employed fully automated calibration routines to find suitable circuit configurations corresponding to those target dynamics. Figure 7 shows measured membrane and adaptation state traces for the first of 128 neurons. These rich dynamics all emerge as a response to a constant step current and differentiate themselves only in the neurons’ parameterizations. All calibrated 128 neurons could – with only slight deviations in the exact spike times and counts – reproduce the desired firing patterns.

IV. Discussion

The circuits discussed in this manuscript faithfully emulate the AdEx model equations and synaptic interaction. They can be precisely calibrated to a wide range of operating points and capture the model dynamics with unprecedented accuracy. Being part of the mixed-signal accelerated neuromorphic system BrainScaleS-2, they have proven themselves in a wide range of experimental studies ranging from the emulation of structured neurons to the machine-learning inspired training of spiking neural networks [11], [12].

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