Research on Topology and Modulation Control Method of a Novel Three-Level Current-Fed DCDC Converter

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Abstract. Multilevel current source converter has the benefits of high output capacity, low current switching stress and low harmonic or ripple content. This paper presents a new topology of three-level current-fed DC/DC converter for superconducting magnetic energy storage application. In this topology, a superconducting inductance acting as a constant current source and a shunt inductance acts as current divider ensure current flows through the power switch components equally to generate immediate level of current. A novel kind of pulse width modulation (PWM) switching strategy for the current instantaneous control of the current source converter was proposed. The modulation switching strategy proposed is able to effectively control the DC current output of the converter. Also, due to the both of proposed topology and control method are quite a simple, it can be easily realized in the practice. Simulation results prove the feasibility and validity of the proposed topology and modulation strategy

1. Introduction

According to the difference of DC side energy storage elements, the multilevel converter can be divided into two categories: voltage source converter (VSC) and current source converter (CSC). Capacitors act as the energy storage component in VSCs, while the inductor is the energy storage component of CSCs.

The VSCs have been studied extensively in the past years. Since A. Nabae et al. propose a three-level neutral-point-clam converter (3L-NPC) [1], many people devote themselves to the research of this field. Until now, a series of ripe theories have been established. As a basis of the converter, the topology of converters has been studied deeply. There are mainly several types of topological structures, such as neutral-point-clamped (NPC), flying capacitor, and active NPC and modular multilevel converters. The control strategy of VSCs also forms a systematic theory.

Multilevel CSCs have a lot of advantages in high output capacity, low current switching stress and low harmonic or ripple content, compared with multilevel voltage source converter. It is especially suitable for low voltage and high current situations, such as superconducting magnetic energy storage and electric vehicle applications [2]. It can simplify the topology structure of converters and improve the charging-discharging efficiency and safety.

In fact, multilevel CSCs have not been developed well yet so far. In the past several decades, researchers pay less attention to multilevel CSCs, unlike VSCs. There are mainly two reasons. On the one hand, the commonly used energy storage sources such as capacitances, ultra-capacitors, and
batteries are all voltage sources components, on the other hand, the energy storage components of voltage-source converters are more efficient than the energy storage inductors of CSCs. In addition, VSCs shows advantages in volume and cost of energy storage device, compared with CSCs. However, with the development and application of superconducting technology, this situation will change soon. In recent years, the breakthrough development of superconducting technology will address the issue of inductor efficiency on energy storage in CSCs. At the same time, the energy storage coil of the power superconducting magnetic energy storage system owns current source characteristics, so multilevel CSCs will appear significant development prospects in superconducting electric power systems. So, it is worthwhile to work on the research of a three-level current-fed DC/DC converter.

2. Proposed CSC Topology
Various topologies are proposed by researchers in the past. There are two main types of circuit topology on the current multilevel converter. A single-phase combined current multilevel converter is introduced. Two single-phase switched current-source converters with independent current sources are connected in parallel at the AC output port to form a combined type of single-phase current-source multilevel converter. A single-phase direct type is introduced in [3], this converter can directly produce the output current of different levels, by means of controlling switches reasonably, which is different from the multilevel current by superimposing current in the output side. A simplified direct type five-level current-fed inverter was proposed in the literature [4].

As shown in Fig. 1, a novel topology on three-level current-fed DC/DC converter is proposed for superconducting magnetic energy storage application. This topology can directly produce an output current of three-level by means of reasonable switch combinations, without external control or closed-loop control. Superconducting coil acts as a constant current source, which passes I current. Inductor $L_1$ acts as a current divider, carry $I/2$ current. Two power switch components connected with the same point of shunt inductance working in the complementary state. By choosing the appropriate combinations of switches, the level of output current can be up to three. In order to get output current with low harmonics, ideal three-level current waveforms, the shunt inductor $L_1$ should always carry $m_e/2$ current as far as possible, which requires switches should have the same internal resistance and the resistance of shunt inductor should be as small as possible. It puts forward a challenge to the performance of switches and sharing-inductor in practical applications. However, in experimental situations, these devices can be considered ideal, so the typical structure of topology will impel circuit to equalize the inductor currents, if a reasonable switch combination is selected. Only a slightly unbalance will appear and a relatively ideal three-level output current can be obtained based on the simulation environment.

![Figure 1. Topology of three-level DC/DC current-fed converter proposed](image)

One of the most important problems in VSCs is the balance of the sharing-capacitor voltage, which directly influences the performance of the converter. Corresponding to the self-balancing problem of capacitor voltage, multilevel CSC should pay attention to the balance of the shunt inductor current [2]. The topology proposed can balance the inductor current no matter what the initial value of shunt...
inductance current is. The current at all levels can be stabilized by the current-equalizing regulation of the converter itself, without the need for additional control or auxiliary circuit.

2.1. Operation of the Converter

In order to explain the operation of the proposed converter, the input current is considered constant, equal to $I$. The power switches such as insulated gate bipolar transistors (IGBTs), which connected to the both ends point of inductors are complementary. So, topology proposed has four possible switch combinations, as shown in Fig. 2.

![Sub circuits of the topology proposed](image)

**Figure 2.** Sub circuits of the topology proposed

From Fig. 2, it can be seen that when a first level output current is generated, the shunt inductor $L_1$ is series with the load, shown in Fig. 2(b), on the contrary, in Fig. 2(c), the shunt inductor $L_1$ is series with power switch $S_4$, then parallel with the load. In Fig. 2(b), the current flow through the shunt inductor $L_1$ is smaller than the current flow through power switch $S_3$. This happens because the inductor $L_1$ ends in negative voltage in steady states, and the current decreases gradually because the inductor and load are discharged in the reverse voltage. While in Fig. 2(c), inductance and load are in the same branch, the inductance ends in positive voltage when the system enters steady states, so the current increases gradually because the inductor and load are charged by the forward voltage. If we do anything to it, the system may not work properly. However, so long as to keep the actual duration of these two switches combination the same, which required by outputting $I/2$ current, topology proposed can generate the three-level output current. This control strategy is called redundant switch combination control [5].

According to Fig. 2, the working process of this converter is as follows:

1) Power switch $S_3$ and $S_4$ are turned on, $S_1$, $S_2$ are turned off (the equivalent sub circuit is shown in Fig. 2(a)), and then, a zero current is injected.

2) Power switch $S_2$ and $S_3$ are turned on, $S_1$, $S_4$ are turned off, (the equivalent sub circuit is shown in Fig. 2(b)), and then, a first level current is delivered, which is also obtained by $S_1$, $S_3$ are on, $S_2$, $S_4$ are turned off, (the equivalent sub circuit is shown in Fig. 2(c)).

3) Power switch $S_1$, $S_2$, are turned on, $S_3$, $S_4$ are turned off, and then, the second level current is injected to the load. (The equivalent sub circuit is shown in Fig. 2(d)).

Table 1. Shows the link between switch combinations and the level of output current.
Table 1. Switch stats and output current level

| S1 | S2 | 0       | 1          |
|----|----|---------|------------|
| 0  | 1  | Zero-level | First-level|
| 1  |    | First-level | Second-level|

2.2. Modulation of the Converter

In multilevel converters, pulse width modulation (PWM) is a very important control mode, which plays an important role in the waveform, harmonic control, and power. Various PWM control strategies have been widely used in voltage source inverter in the past years [6]. According to the conversion frequency of power devices, there are two kinds: linear frequency conversion modulation and high frequency conversion modulation. There are two kinds of high-frequency conversion modulation: space vector modulation and mobile carrier harmonic component modulation. Space vector modulation is generally used in converters that the level of output current is less than five, and it is difficult to implement in five-level converters or more levels.

In this paper, the control strategy is of course based on PWM, but just use one carrier. The main concept is to use the same triangular waveform to compare with the reference and reference operated in the whole modulation. In fact, to some extent, the operation is similar to the traditional phase opposition disposition PWM and sinusoidal PWM [7].

The modulation index is defined as

\[ M = \frac{V_p}{V_t} \]  

Where \( V_p \) is the reference amplitude, \( V_t \) is the peak of the carrier signal.

Fig. 3 shows the useful waveforms in the whole working process of the converter. Fig. 3(1) shows the reference \( R \), the carrier \( C \), and the rectified reference \( |R| \). The carrier amplitude is set at one, the modulation index is 0.9. \( |R| \) is the absolute value of signal \( R \). \( R_s \) is the rectified reference \( |R| \) limited by signal 1/2, half of the carrier amplitude. \( R_f \) is produced by Formula (2). When \( R_f \) compared with the carrier \( C \), signal \( P \) is achieved; when \( |R| \) compared with 1/2 logic, signal \( K \) is achieved, as shown in Fig. 3.

\[ R_f = 4 \times R_s - 2|R| \]  

(2)
Figure 3. Waveforms of the proposed PWM (x-axis: \( t \) (s), y-axis: \( C, R \) (pu), \( P, K \) (0/1))

The symmetrical control of redundant switch combination is employing to generate three-level output current in topological circuits [5]. The main idea of this control strategy is signal \( K, P, P_a \) sharing the control of gate signals of switches. The signal \( K \) and \( P \) establish the current level together; while \( P_a \) plays a role in alternating the two switches combinations that make circuits generate \( I/2 \) output current. \( P_a \) is an auxiliary signal to balance the current of sharing-inductor. Fig. 4 elaborates the generating process of the \( P_a \) signal. In1 is the \( P \) signal, Out1 is the \( P_a \) signal, and In2 is the value of inductor \( L_1 \) current. D latch1 and D latch 2, logical operator 1 form a falling edge trigger.

Figure 4. The generation of Signal \( P_a \)
According to the value of signal $P_a$, the circuit alternates two switch combinations required by the $I/2$ output current. In Fig. 1, if the inductor current exceeds $I/2$ current, signal $P_a$ will impel the circuit changes the states into another state, shown in Fig. 2(b), when the next $I/2$ output current level appears; otherwise, the circuit will change into the states of $S_1$ is on, $S_2$ is off. When signal $K$ is low, the zero or $I/2$ output current can be achieved, depending on the signal $P$ is high or low. When the signal $P$ is high, zero output current will appear, otherwise, the $I/2$ output current can be obtained. When signal $K$ is high, $I$ or $I/2$ output current can be achieved, also depending on the value of signal $P$. When the signal $P$ is high, $I$ output current will appear, otherwise, the $I/2$ output current can be obtained. The logic equations for each control signal are presented by Formula. (3) and Formula. (4). the map for gate signals is shown in Table 2, $(0, 1)$ means the $S_1$ is off and $S_2$ is on.

$$S_1 = L \otimes P \oplus P' \otimes P_a$$  \hspace{1cm} (3)

$$S_2 = L \otimes P \oplus P' \otimes P'_a$$  \hspace{1cm} (4)

| $P$ | $P_a$ | $K$ | $S_1$ | $S_2$ |
|-----|------|-----|-----|-----|
| 0   | 0    | 0   | 0   | 0   |
|     | 0    | 1   | 0   | 0   |
|     | 1    |     |     |     |
| 1   | 0    | 0   | 1   | 0   |
|     | 1    | 1   | 0   | 1   |

1) When signal $K$ is low, a zero current or $I/2$ current will be produced, depending on the level of signal $P$. When signal $P$ is high, $S_1$, $S_2$ is on, a zero current must be generated; when signal $P$ is low, $I/2$ output current must be produced. In this condition, depending on the value of $P_a$, the circuit change the switch combination from $S_1$ is on, $S_2$ is off to $S_1$ is off, $S_2$ is off, which can ensure the inductor current almost carrying $I/2$ current in the whole modulation.

2) When signal $K$ is high, $I$ current or $I/2$ current will be obtained, also depending on the value of signal $P$. When signal $P$ is high, $S_3$ and $S_4$ are on, $I$ current must be generated; when signal $P$ is low, $I/2$ output current must be produced. In this condition, it keeps the same in switch states, as mentioned in the previous paragraph.

3. Simulation and Discussion

In this part, the feasibility and validity of the topology proposed have been verified by the simulation result achieved in Matlab/Simulink surroundings. The constant current source is set to 1A, the inductance is 150 mH, the load is 10 ohm resistance, the modulation index is 0.9.

Fig. 5(a) shows the performance of the topology, including the output current and current of shunt inductor, Fig. 5(b) shows gate signals of $S_1$ and $S_2$. For this case, it can be observed that the inductor current is fluctuating around 0.5A approximately in the steady state, which is half of the value of the constant current source. From the waveforms of the inductor current, we can clearly see that the simple feedback controller regulates inductor current effectively, as it expected. Moreover, the output current is a three-level wave.

The simulation results also show the output current does not be affected by the changes of load, the inductor current still always fluctuating around half of the main current in the steady states. Fig. 6 shows output current and inductor current, when the load is 10-ohm resistance series with 0.1 H inductance.
Figure 5. Output current and inductor current, gate signals of $S_1$ and $S_2$ ($x$-axis: $t$ (s))

Figure 6. Waveforms of the output current and inductor current with resistance and inductance load ($x$-axis: $t$ (s), $y$-axis: $I$ (A))

4. Conclusion
This paper has presented a new topology of current-fed DC/DC converter for superconducting magnetic energy storage, using four power switches and only one inductor. Its structure is quite simple, but owns
a good output performance. The control method adopted in this paper is similar to the multi-carrier method, but different in some ways. The control signals of switches is obtained by comparing a single carrier with various reference signals processed.

Because of the typical structure of topology and a novel kind of PWM utilization, topology proposed can self-balance the sharing inductor current, even under the condition of changing load. Furthermore, a simple feedback control strategy is applied to ensure a better balance process of the inductor current. In simulations, the waveforms of output current and inductor current are satisfactory, just show a slight unbalance.

The operation, analysis, modulation of this topology proposed have been exposed in this paper, and finally, the feasibility and validity of topological structure has been verified in simulation.

The proposed three-level current-fed DC/DC converter is very suitable for the superconducting magnetic energy storage system application, because of the inherent benefits, such as low switching current stress, high output capacity and low ripple content.

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