ORIGINAL RESEARCH PAPER

Design of a 128-channel transceiver hardware for medical ultrasound imaging systems

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Funding information
Ministry of Electronics and Information technology

Abstract
In this work, the design and development of a 128-channel transceiver hardware for medical ultrasound imaging systems and research is presented. The proposed hardware solution integrates the analog front-end (AFE) sections, high voltage transmit pulser sections, field programmable gate array (FPGA)-based transmit beamforming and control logic, time gain compensation (TGC) and continuous (CW) Doppler functional circuits, and the necessary power supplies (high voltage (HV) and low voltage (LV)) into a single board. In addition, it integrates pervasive segments like power, clock tree sections, and power management and debugger logic. The developed transceiver solution helps to advance the research in medical ultrasound imaging techniques and technologies. To prototype an ultrasound imaging system, the developed hardware can be interfaced with a 128-channel ultrasound transducer array and an FPGA-based signal processing module. As the transceiver hardware is designed with commercially available chipsets, it provides the flexibility to programme the ultrasound AFE signal chain, transmit beamforming and the arbitrary transmit wave pattern. Besides, compared to the commercial open ultrasound research scanners, the flexibility to interface FPGA-based signal processing module helps to investigate the performance of hardware realisation of various ultrasound signal processing algorithms. Moreover, the work realises a single-board transceiver solution for multichannel ultrasound system fulfilment.

1 | INTRODUCTION

Ultrasound imaging is a very popular and ubiquitous diagnostic technique [1]. A medical ultrasound imaging system transmits focussed beams of sound wave energy into the medium of interest, that is, the human body and reconstructs the biological tissue image onto a display [2]. The basic building blocks of an ultrasound imaging system are the transmitter module, receiver module, control and display modules, and the power supply module [3]. An ultrasound imaging system needs high voltage (HV) power supplies for the transmitter section and low voltage (LV) power supplies for the receiver sections.

Figure 1 depicts an ultrasound imaging system block diagram [2]. As illustrated in Figure 1, the transmit section has a transmit beamformer, transmit pulser and transmit/receive (T/R) switch. The receiver section has an analog front-end (AFE) processor for signal conditioning followed by a receive (Rx) beamformer. In addition, the receiver section has the time gain compensation (TGC) control and the continuous wave (CW)/pulsed wave (PW) Doppler processing modules. The control logic performs the necessary pulse repetition frequency (PRF) generation, synchronisation among the transmitter and the receiver sections, the T/R switch control etc. Since the transmitter section operates at high voltages, the receiver section is isolated by the T/R switch during transmission. On reception, the T/R switch is on, and the analog signal conditioned, and the receive beamformed/Doppler processed data is streamed to the back-end processing module for further processing, image formation, and display. The control and display interface provides proper control and addressing mechanism to various modules like the T/R switch, AFE, Tx/Rx beamformer, the Doppler processor etc. for adequate configuration and synchronisation.

Due to advancements in technology, ultrasound imaging systems have succeeded in real-time 3D/4D imaging, high
frame rate imaging etc. [4, 5]. As described (Figure 1), except for the ultrasound transducer array (probe) the other parts of an ultrasound imaging system build on electronics technology. Hence, the advancement in electronics technology such as integrated circuit (IC) development, field programmable gate array (FPGA)-based signal processing hardware development etc. enable ultrafast imaging. The advancement in FPGA technology [6] enabled the employment of signal processing hardware along with communication controllers like peripheral component interconnect express (PCIe), high-speed serialiser-deserialiser (SerDes), Gigabit Ethernet etc. on a single device. The FPGA technology also enables the hardware acceleration of ultrasound imaging algorithms with reduced power consumption.

Even though the advancement in technology enables the miniaturisation of ultrasound machines, (both cart-based and portable) commercial scanners do not provide control over transmit and receive hardware modules for researchers. Hence, for research purposes, many open platforms that provide access to ultrasound transmit and receive signal chains were developed [3, 5, 7]. The review article [3] compares the existing ultrasound open platforms for research in terms of hardware processing capability and input-output (IO) throughput. Most of the ultrasound system architectures discussed [3] follow the FPGA-based front-end and mid-end processing, and a PC-based back-end processing. The open ultrasound system architectures discussed [3] employ multiple boards for the fulfilment of multichannel systems, and the researchers cannot access/configure the FPGA logic.

In this work, we present the design and development of a single-board multichannel ultrasound transceiver solution. The transceiver hardware is based on an FPGA and supports up to 128 channels. The transceiver hardware can be interfaced with an ultrasound probe, as well as an FPGA-based processing board, for the investigation of ultrasound system/imaging algorithm performance. The rest of the work is organised as follows: Section 2 reviews the related works, and section 3 presents the ultrasound transceiver’s hardware design. The transceiver’s board testing methodologies are presented in section 4. Section 5 details the results and discussions, and finally, section 6 concludes the development work.

2 | LITERATURE REVIEW

Since the early stages of development, medical ultrasound imaging technology has continuously evolved towards patient diagnosis and treatment [4, 5]. The use of the ultrasonic wave as a medical diagnostic tool started in the 1940s [2]. Since then the medical ultrasound industry has had rapid growth. In the early stages of development, the systems were based on analog technology and later evolved to digital technology [8]. Initially, the systems were developed using digital signal processors (DSPs) and microprocessors. Once the programmable logic devices were introduced, the systems evolved based on FPGAs [9–11].

Though the ultrasound technology evolved significantly, the ultrasound researchers did not have access to hardware and raw ultrasound radio frequency (RF) data. For most commercial ultrasound machines, hardware is proprietary and raw sensor data for investigating new imaging algorithms is not available. The work presented in [12, 13] provided a research interface for commercial scanners to collect raw ultrasound receive data to examine the imaging algorithms. Further, the open ultrasound platforms like SARUS, ULA-OP 256, Sonix Touch, Verasonics etc. were developed [3].

The existing works related to this development are classified into the development of research/open platform (OP) ultrasound systems, FPGA-based ultrasound imaging systems, ultrasound data acquisition systems, platforms for ultrasound signal processing algorithm implementations on FPGA etc. In addition, the development work also can be referred for the development of commercial ultrasound imaging systems. The development of open platforms is necessary to foster the development of new ultrasound diagnostic methods like synthetic aperture, plane wave, shear wave elastography, vector flow imaging etc [3]. In addition, the development of custom hardware for ultrasound systems can enable hardware configuration and control over system design. Moreover, it can to
validate the ultrasound signal processing chain and to investigate the architectural performance [10].

As described in [3] the architectures for the open platforms are classified into hardware-based and software-based platforms. In hardware-based platforms, data processing is performed onboard computing hardware like FPGAs, DSPs, SoCs etc. Since complex computations are handled by onboard electronics, hardware-based OPs need not send the enormous digitised raw channel data to the back-end processor/PC, that is, in hardware OPs, complex signal processing operations like digital receive beamforming, Doppler processing, scan conversion etc. can be performed on computing devices like FPGA, SoCs etc. This helps in the reduction of the data rate while streaming the front-end processed data to the back-end processor/PC. Hence, such systems can be designed with low-cost serial links like universal serial bus (USB) 3.0, Gigabit Ethernet etc. and can be easily interfaced with a PC. However, for preliminary testing of new algorithms developed on real data, the hardware OPs require an excessive amount of memory to store large volumes of raw channel data that can be streamed on demand to the back-end PC in an offline basis [4].

In software-based platforms, the raw data are acquired on a PC, and further, the processing algorithms are implemented on CPU/GPU-based high-level languages. Furthermore, to handle high data rate requirements, the software OPs require high-speed serial links like PCIe 3.0. Compared to hardware OPs, software OPs provide the flexibility to evaluate newly developed ultrasound signal/image processing algorithms in real time. However, due to the necessity of high data rate, limitations in processing etc., the software OP architecture can not be accustomed to build commercial ultrasound systems.

Most of the research scanners discussed followed FPGA-based data acquisition and processing. In hardware OPs, the FPGAs were used to realise the receive beamformer, transmit sequencer, and high-speed communication controllers like USB 3.0, Gigabit Ethernet, SerDes etc. In software OPs the FPGAs were used to deserialize the high-speed data and to stream to back-end PC via a high-speed PCIe/Gigabit Ethernet link. Hence, in the open architectures discussed, the FPGAs played a vital role as transmit sequencer, data packet controller (High-speed SerDes, PCIe, Gigabit Ethernet etc.), receive digital beamformer etc. Further to realise multichannel systems, multiple FPGA boards were integrated.

The significance of employing FPGAs in ultrasound data acquisition and processing is described in [9, 14, 15]. The works [9, 14, 15] demonstrated a scaled-down version of (8 channels) ultrasound data acquisition and processing systems. In [9] the Xilinx®-Kintex-7 FPGA KC705 evaluation kit was used as the FPGA-based receive signal chain processor, and the Opal Kelly® XEM3001 FPGA module was used as the transmit sequencer and controller. The work presented in [9] can be used as a hardware OP and can be used to validate ultrasound receive signal processing algorithm architecture implementations on FPGA. In [14] the FPGA-based TSW1400 evaluation kit was used to acquire and stream offline ultrasound raw channel data to a PC. Once the raw channel data is acquired, the ultrasound receive signal chain can be validated either via MATLAB or C/C++ programs. The work presented in [15] demonstrates a transmitter solution for research purposes.

Analysis of some of the existing designs of FPGA-based ultrasound imaging systems is presented in [11]. The first design discussed [10] is an FPGA-based 16-channel portable system, and its complete transmit, receive mid-end, backend, and control were integrated on FPGA. In the second design, FPGA-based timing control and high speed and a digital IO interface were implemented. The timing control synchronised the front-end modules, and the high-speed digital IO interface transfers the digitised the ultrasound's raw sensor data to a PC for further processing and image formation. The imaging system architecture discussed in the third design has FPGA-based transmit and receive beamforming, and the prototype was developed by utilising existing evaluation boards. Again, the systems were demonstrated with scaled-down versions (16/8 channels).

A 128-channel ultrasound imaging beamformer based on FPGA is discussed in [16]. However, this system is cumbersome as eight16-channel FPGA-based boards were integrated to form the beamformer. The system can be connected by a USB 2.0 port to stream beamformed ultrasound data to a PC, and the PC can perform back-end processing and image formation. Hence, tests and investigation of new imaging algorithms can be achieved. The ultrasound imaging system for the development and test of new ultrasound investigation methods presented in [17] also exercises FPGA-based hardware to stream raw RF data to a PC via a high-speed interface. A flexible multichannel system demonstrated in [18] used eight 16-channel FPGA-based front-end boards to realise a 128-channel system. The importance of leveraging FPGAs for medical imaging is discussed in [19–21]. The work presented in [22] demonstrated a pixel-level reconfigurable digital beamforming core for ultrasound imaging. To validate similar kinds of algorithm implementations on FPGA, a multichannel ultrasound front-end hardware with the capability to stream a higher number of channel data to FPGA-based processing hardware is vital.

From the literature review of related works, it is evident that the multichannel systems were realised with multiple hardware modules. Therefore, to design compact systems (cart-based as well as portable) a single-board transceiver solution that integrates the transmitter, receiver, power supply, and pervasive segments like the clock tree, power tree, power monitoring, and management etc. with necessary interfaces (ultrasound transducer array/probe, FPGA mezzanine/board to board connector) is required. This motivated us to develop an FPGA-based 128-channel ultrasound transceiver hardware that could be exercised to promote research as well as commercial ultrasound system development. Also, the transceiver hardware needs to be interfaced with a custom-designed high-end FPGA-based processing board or commercial high-end FPGA-based evaluation boards for the development of hardware OPs/commercial systems.

The following section discusses the ultrasound transceiver hardware architecture design in detail.
3 | ULTRASOUND TRANSCEIVER HARDWARE ARCHITECTURE

The block diagram of the proposed ultrasound transceiver hardware architecture is shown in Figure 2. The architecture is based on Xilinx® Kintex-7 FPGA (XC7K160 T) and MAXIM® MAX14808 transmit pulsar cum transmit/receive switch chip and Texas Instruments® AFE 5818 chip. The architecture employs eight AFE5818 chips and 16 MAX14808 chips along with the FPGA and other pervasive sections (power supplies, power tree, clock tree, power management etc.) to realise a 128-channel ultrasound transceiver solution. In addition, the analog TGC and CWD circuits are also integrated with the hardware system. The selection of the hardware components for the transceiver hardware was carried out based on the front-end design considerations discussed in [23, 24]. The datasheets and the reference designs [25, 26, 27, 28] provided by TI® were also referred to perform the design.

To store the FPGA boot bit-file configuration as well as the transmit beamformer delay tables, a non-volatile flash memory is interfaced with the FPGA. The HV, LV power supplies and the Power Management Bus™ (PMBUS) chip UCD90320 are also accommodated with the system architecture. For reliable operation of any digital hardware, jitter cleaned and the deskewed clock is imperative. Therefore, a clock jitter cleaner and deskew circuitry based on TI® LMK™ series ICs are designed. The transmit beamformer logic implemented on FPGA excites the ultrasound probe via the transmit pulser and T/R switch in a delay-controlled manner to focus the transmitted ultrasound beam/wavefront at a particular focal point. The transmit beamformer outputs are delay sequenced LV pulses, and the needed HV pulses to excite the sensors are generated by the pulser. To protect the low voltage AFE section, the T/R switch is kept in an off state during transmission.

As detailed in Figure 2 the transceiver hardware provides the interface provisions such as USB/JTAG (JTAG SMT2), USB/UART (CP2103 chip), ultrasound probe, board to board, or FPGA mezzanine connector (FMC) etc. The JTAG/USB (JTAG SMT2 module) interface is provided to establish the FPGA connectivity with the PC via the Xilinx Vivado tool. The joint test action group (JTAG) SMT2 module is the JTAG to USB and vice versa protocol converter. Similarly, the CP2103 chip is the universal asynchronous receiver transmitter (UART) to USB/USB to UART protocol converter bridge. The UART interface is necessary for any hardware system to build the system test routines on any FPGA/processor. The ultrasound probe and the FMC connector are attached with the

**Figure 2** Ultrasound transceiver hardware block diagram
hardware architecture to provide an ultrasound sensor array and an external digital signal processor module interface. The following subsections explain various subblocks in the ultrasound front-end transceiver architecture.

### 3.1 FPGA

The 128-channel transmit beamformer, the control logic for CWD, TGC, clock tree, AFE, serial peripheral interface (SPI) flash etc. are proposed to be implemented on the FPGA selected, that is, Xilinx® Kintex™ –7 XC7K160T FPGA. Figure 3 details the interface modules connected to FPGA, and Figure 4 illustrates the digital hardware logic effectuated in FPGA. The proposed FPGA is selected based on the gate count, memory, IO bandwidth, and timing performance requirements of the hardware logic. The selected FPGA that has nearly 162,240 logic cells along with distributed RAM of 2188 Kb and 144GMACS operations can be performed with available 600 DSP slices. The FPGA core can operate at a very low voltage of 1.0 V or 0.9 V to ensure lower power consumption with lower cooling required.

The digital hardware implemented in the FPGA (Figure 4) has mainly the transmit beamformer and control logic to configure the various peripheral controller ICs. The transmit beamformer generates the delayed pulse control signals to energise the ultrasound transducer array for focussed beam transmissions. Based on the transmission control parameters, the transmit beamformer can be configured for the required focal point, type of transmission etc. The peripheral controller ICs like AFE, CWD ADC, TGC DAC etc. can be configured via the serial interfaces like SPI/I2C. The TGC interface logic is designed to support up to six TGC sliders, and based on the maximum depth, the sliders are equally divided. A UART interface-based PC GUI is developed and used to pass the front-end control parameters to the FPGA control logic. A master controller FSM is designed to maintain the synchronisation among the various interface controllers implemented in the FPGA. The Quad serial peripheral interface (QSPI) flash interface logic performs QSPI Flash read/write logic. The transmit beamformer delay tables are stored in Flash sectors, and on bootup, and the delay values are loaded into the internal delay registers of the FPGA.

### 3.2 AFE processor

An analog front-end (AFE) or AFE processor has a set of signal conditioning circuitry, such as a low noise amplifier (LNA), a programmable gain amplifier (PGA), voltage controlled attenuator (VCAT), filters followed by an analog to digital converter (ADC). In the proposed architecture, the AFE5818 chip from TI® is selected as the analog front-end processor [25]. It accepts analog echo and converts it into a digital low voltage differential
signaling (LVDS) format. The chip also can be configured via the SPI interface.

The AFE5818 AFE processor supports up to 16 channels, along with a CW mixer and a beamformer. The integrated LNA supports programmable gain (12, 18 and 24 dB), 250 mVPP to 1VPP input dynamic range, and a programmable active termination. The VCAT provides digital and analog attenuation control up to 40 dB and improves the overall low-gain signal to noise ratio (SNR), which benefits harmonic and near-field imaging. The PGA supports 24 or 30 dB programmable gain. The anti-aliasing filter can be configured in the range of 10 to 35 MHz in steps of 5 MHz. The on-chip CWD beamformer can be configured up to 16 selectable phase delays. Furthermore, a unique third- and fifth-order harmonic suppression filter is implemented to enhance CW sensitivity. The integrated ADC supports up to 75 dB SNR and up to 65 MHz sampling frequency.

Figure 5 details the AFE5818 interface diagram with various peripherals. It has a T/R switch interface that accepts analog low voltage echo signals for signal conditioning. The signal-conditioned and digital-converted LVDS signals are transferred via the board to board connector to other processor boards for beamforming and further processing. The TGC interface section provides analog control of the TGC gain of the AFE. For CW processing, a CW interface section is designed and integrated with an AFE 5818 chip. The SPI signals are interfaced with the FPGA for configuring the AFE for various modes. To set a particular AFE, the particular AFE needs to be selected and programmed via SPI.

3.3 | Transmit receive switch and transmit pulser

The MAX14808 high voltage pulser generates high-frequency high voltage pulses up to ±105V for driving ultrasound piezoelectric transducers. The device supports two operating modes, octal three-level/quad five-level pulser modes. The octal three-level mode can run on eight independent channels, and each channel can generate three-level pulses. The quad five-level mode can operate on four independent channels, and each channel can generate five-level pulses. A grass-clipping diode and active damp circuit are integrated to provide more protection by fully discharging the pulser output node as soon as the transmit burst is over. The thermal protection output THP gets automatically set when the temperature exceeds 150°C, and the device gets shut down. Regular operation resumes when the temperature falls below 130°C and the THP
gets reset. Each channel has a low power T/R switch recovery time after the transmission is less than 1.2 µs, but it is recommended to turn off the T/R switch for a period of 3 µs after transmission burst.

3.4 | Power management and Debug bus (PMBus).

The UCD90320 device from TI® is employed as PMBus™ in the proposed design (Figure 6). The selected PMBus™ module supports up to 32 power rails for sequencing and managing. In addition to power sequencing and managing, it is integrated with 24 ADCs to monitor the supply current, voltage, and temperature. In the proposed and designed architecture, the FPGA, AFEs etc. require specific power on and off sequencing for proper functioning of the devices. The PMBus™ UCD90320 can be configured for proper power on and off sequencing in the devices via the power enabling pins. For example, the power on and off sequencing of the FPGA is critical, as the core voltage needs to be powered on initially before any IO supplies. If the IO supply is powered on initially, it may cause the current to sink into the core, and this, in turn, may damage the device.

The designed transceiver hardware architecture requires low voltage (LV) supplies for the FPGA, AFEs, UCD90320, clock tree section etc., and high voltage (HV) for the pulser section. Hence, a power tree that employs the DC to DC converters and low drop out regulators (LDOs) is designed. For critical noise circuits, a DC to DC converter followed by an LDO regulator or an LDO regulator alone is applied. Since all the power supplies required are also integrated on the 128-channel transceiver hardware itself, in addition to power sequencing, monitoring of rail voltages, currents, fault conditions etc. is also critical for reliable operation of the circuits. The device can be configured for a particular current, voltage, and temperature tolerance. The moment the power rails break the tolerance levels, the specific rail can be cut off, and the information can be read via the PMBus™ controller interface.

3.5 | Clock tree and clock jitter cleaner

The clock routing and jitter cleaning are crucial in any of the hardware circuit designs. The LMK04610 device from TI is employed as the clock management and jitter cleaner. Figure 7 illustrates the clock management design for the proposed hardware. The clock jitter cleaner IC has two i/p clocks and 10 o/p differential clocks. The device accepts a 125 MHz LVDS clock from the programmable oscillator LMK61E2 device, and the FPGA logic can programme the same. Initially, the LMK04610 device operates at the 100 MHz clock from the CVHD-950 oscillator and generates 100 MHz OSCOUT, which is available for the FPGA to programme the LMK61E2 oscillator chip.

Further, the LMK04610 chip can be programmed by the FPGA via the SPI interface to generate the required clock outputs. The LMK00308 clock buffer provides proper driving strength to various clocks required for the devices, like AFE, pulser etc SPI, serial peripheral interface.

3.6 | Flash memory

A serial NOR flash memory of size 256Mb (MT25QL256ABA8ESF) is selected to interface with the FPGA to boot bit file and store the transmit beamformer delay configurations. The device is the first high-performance multiple input/output
serial Flash memory manufactured based on 65 nm NOR technology. It features execute-in-place (XIP) functionality, advanced write protection mechanisms, and a high-speed SPI-compatible bus interface. The innovative, high-performance, dual, and quad input/output instructions enable the transfer bandwidth to be double or quadruple for READ and PROGRAMme operations.

### 3.7 Interfaces

The transceiver hardware needs to be interfaced with the ultrasound transducer array to transmit high-voltage pulses and to receive low-voltage analog echoes. The signal-conditioned and digitised analog echo signal needs to be transferred to further hardware for processing and image formation. Therefore, to accomplish the IO data handling, an ultrasound probe connector and a board-to-board connector are employed. The control interfaces are mainly based on SPI, I2C, and UART protocols. Table 1 illustrates the interfaces used in the design, along with the required descriptions.

| Sl. No | Interface | Description |
|--------|-----------|-------------|
| 1.     | SPI flash | The interface between FPGA and flash. Supports up to 4 lines (QSPI). To boot the FPGA from flash as well as flash Read/Write. |
| 2.     | SPI       | To Configure AFE, LMK04610, UCD90320 etc. devices via. FPGA |
| 3.     | I²C       | The interface between the FPGA and programmable oscillator (FPGA user clock) |
| 4.     | UART      | The interface between the FPGA and PC. Used USB to UART converter (CP2103) to access the serial port via the USB connector. |
| 5.     | JTAG      | The FPGA bitstream configuration and debugging interface via the Xilinx VIVADO tool installed on PC. |
| 6.     | Ultrasound probe connector | To interface the ultrasound transducer array with the TR switch and AFE. |
| 7.     | Board to board connector | To transfer signal-conditioned and digitised LVDS data to the processor board for further processing. |

**TABLE 1** BOARD interfaces

Abbreviations: AFE, analog front-end; FPGA, field programmable gate array; JTAG, joint test action group; LVDS, low voltage differential signaling; QSPI, Quad serial peripheral interface; SPI, serial peripheral interface; UART, universal asynchronous receiver transmitter; USB, universal serial bus.

![Clock management interface](image.png)

**FIGURE 7** Clock management interface

### 3.8 AC and DC analysis

Once the components are selected and the architecture design is completed, the component to component interconnection compatibility, i.e., the drive strength and voltage compatibility needs to be verified by performing AC and DC analysis. The AC analysis checks the required drive strength by calculating the total drive capacitance required, that is, the load capacitance should be higher than all the other drive input capacitances. In DC analysis, the voltage compatibility among the pins is checked by considering high- and low logic levels. The drive strength issues are resolved by adding proper buffers, and the voltage compatibility issues are resolved by adding level translators.

### 4 ULTRASOUND TRANSCEIVER HARDWARE TESTING

Once the schematic capture is completed, the placement of components and the PCB design are completed. We performed signal integrity, power, and thermal analysis of the designed PCB, and the designed PCB passed all the examinations. Figure 8 shows the fabricated and component-populated ultrasound transceiver hardware along with the test setup. To test the interfaces and the signal chain, we developed a PC-based automated test software. The FPGA and the PC are interfaced via the universal asynchronous receiver transmitter, and the serial port-based test control mechanism is followed. The various interfaces and signal chains can be tested via the test GUI developed.

To bring up the hardware, we used AFE 5818 EVM and TSW1400 EVM from Texas Instruments and the high-speed Data Capture Pro™ software. An adapter card to transfer our designed hardware AFE LVDS data to TSW1400 EVM is designed and developed. The transceiver hardware and the TSW1400 EVM are connected via the adapter. An ultrasound
The probe is connected and energised by the transmit pulser. Plane wave excitation is carried out to test phantoms (the kidney and resolution), and the received echo at each sensor output or AFE input is measured along with the noise levels. Further, the signal chain and SNR analysis are carried out. The AFE output's signal and noise analysis are performed, and the SNR degradation at the signal conditioned output is analysed. The received echo is signal conditioned, digitised, streamed to the PC and captured by the high-speed Data Capture Pro™ software (Figure 9).

To determine the system receiver's sensitivity and noise performance, the signal chain and SNR analysis of the front-end signal conditioning hardware are performed. We analysed various ultrasound array geometries and frequencies (2.5 MHz phased array, 3.5 MHz convex array, 7.5 MHz linear array etc.) at a dynamic range of 0.9 µV (−120 dB) to 1 V (0 dB). Figure 10, Figure 11, and Figure 12 summarise the ultrasound probe output (AFE input) to ADC input (AFE output) signal and noise levels. Based on the sensor source impedance and bandwidth, the calculated thermal noise at the probe output is 1.42 µV (−116.98 dB).

**FIGURE 8** Ultrasound transceiver hardware and test setup

**FIGURE 9** Captured ultrasound echo
medical ultrasound imaging systems, the echoes are in µV to mV levels. Accordingly, based on the signal chain and SNR analysis, the proposed and designed hardware can process the ultrasound echo dynamic range. The study also shows that due to the signal chain, there is an SNR degradation from the probe output to the ADC input.

The developed ultrasound front-end hardware is integrated with the ultrasound system prototype and the receiver signal chain analysis from the sensor to display is carried out. Figure 13 shows the system prototype developed. The signal-conditioned and digitised analog RF data is streamed into an FPGA-based digital beamformer board through the board-to-board connector (Figure 3). The data received from the transceiver hardware is streamed to the PC by a high-speed Gigabit Ethernet link. A further MATLAB-based raw data analysis is performed to analyse the signal and noise performance of the front-end hardware. Initially, we used the vector signal generator (VSG) to generate the test echo signal with the required dynamic range and fed it to the ultrasound probe output or the AFE input path. The signal-conditioned and digitised test signal is captured in the PC. The MATLAB-based signal and FFT analysis are performed to analyse the noise floor. Figure 14 depicts the captured signal and the corresponding FFT. A 1Hz signal in the mV range is generated using a VSG and fed to the AFE input. The signal is conditioned and captured in the PC and the corresponding FFT analysis is carried out to analyse the noise floor. The plane wave transmission is performed, and the analog echoes are captured up to 15 cm range from a cyst phantom. Noise floor analysis is performed, and it is observed that the noise floor is below 10 µV. Figure 15 depicts the ultrasound echo captured in the PC and the corresponding FFT plot.

5 | RESULTS AND DISCUSSIONS

Most of the development work in ultrasound hardware [3, 5, 7] is related to open ultrasound platforms for research. The designs are oriented towards the three technical attributes [3] required for open ultrasound platforms, that is, programmable per-channel basis TX operations, significant memory and access of pre-beamformed data, abundant computational resources, and high throughput IO for real-time processing. We analysed the various hardware-based open platforms and investigated the hardware components integrated into the systems. The systems employ separate power modules (HV and LV), TRX solutions, and either an FPGA or a PC/GPU-based backend processing. In most of the designs, due to colossal data bandwidth requirements, an FPGA-based receive digital beamforming is performed.

Our development work is compared with previous works in the literature and concluded in Table 2. The existing works used up to 32-channel TRX hardware [5] to integrate a multichannel system. The work reported in [7, 16] used 16-channel TRX hardware and [9, 15] integrated existing evaluation modules. The analysis of existing designs for FPGA-based ultrasound imaging systems [11] also discusses the evaluation board-based designs. Our design provides a 128-channel transmit-receive solution.
with integrated power supplies along with sequencing and management compared to the existing reported works. Our work also integrates analog CWD and TGC hardware. The pulser adopted supports the generation of both five-level as well as three-level pulses. The hardware developed also has on board the 256 Mb QSPI flash. The external interface connectors (ultrasound probe and FMC/board to board) enable the interface of the hardware developed with ultrasound array and digital hardware for processing. The power tree is designed in such a way that the entire power supply requirements can be generated from a single 12 V power supply. The estimated power requirement for the developed hardware is approximately 22 W.
TABLE 2  Comparison with previous works in the literature

|               | This work                                      | [5]                          | [7]                          | [9]                          | [15]                         | [16]                         |
|---------------|------------------------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|
| **Hardware**  | Custom designed using commercially available ICs | Custom                       | Custom                       | Evaluation modules           | Evaluation modules           | Custom                       |
| **Channels**  | 128 Tx/Rx                                      | 32 Tx/Rx                     | 16 Tx/Rx                     | 8 Tx/Rx                      | 8 Tx/Rx                      | 16 Tx/Rx                     |
| **Tx voltage**| Up to 210 V pp                                 | Up to 200 V pp               | Up to 200 V pp               | Up to 210 V pp               | Up to 100 V pp               | -                            |
| **Tx frequency**| Programmable up to 20 MHz                      | Programmable up to 20 MHz    | Programmable up to 20 MHz    | Programmable up to 20 MHz    | Programmable up to 0.5 to 20 MHz | -                            |
| **Tx type**   | 5-Level 64 channels, 3-level 128 channels      | Linear                       | Linear                       | 3-Level                      | 3-Level                      | -                            |
| **ADC**       | 12/14 bit, programmable up to 62.5 MHz sampling, | 12 bit at 78 MHz sampling, programmable down sampling | 12 bit at 78 MHz sampling, programmable down sampling | 12/14 bit, programmable up to 62.5 MHz sampling, | 12/14 bit, programmable up to 62.5 MHz sampling, | 12 bit at 50 MHz |
| **Transmit sequencing and control** | FPGA (Xilinx Kintex-7 160T) | FPGA                         | FPGA                         | Opel Kelli XEM3001 FPGA module. | Spartan 3E FPGA starter kit. | FPGA (EP3C16Q240) |
| **Analog CW and TGC** | Analog CW and TGC integrated on board | -                            | -                            | Not supported                | Not supported                | Analog TGC                  |
| **Onboard memory** | 256 Mb QSPI flash                              | Nil                          | Nil                          | -                            | -                            | Nil                          |
| **Interfaces** | Ultrasound probe connector, high-speed board to board connector for LVDS interface. | Custom Backplane bus         | Custom Backplane bus         | SMA connectors               | Custom wiring                | Custom Backplane bus         |
| **Power supplies** | Integrated LV and programmable HV on board. Derived all supplies from a single 12V power supply. | External power module        | External power module        | External power supplies      | External power supplies      | External power module        |

**Abbreviations:** ADC, analog to digital converter; CW, continuous; FPGA, field programmable gate array; HV, high voltage; IC, integrated circuit; LV, low voltage; LVDS, low voltage differential signaling; QSPI, Quad serial peripheral interface; SMA, SubMiniature version A; TGC, time gain compensation.
under peak operation of the circuits. We developed test routines and PC-based tests for automation control. Also, the transmit-receive experiments are conducted, and the noise floor of the ADC and SNR of the complete signal chain is investigated.

6 CONCLUSION

An integrated TRX solution for 128-channel ultrasound front-end hardware is designed and developed. The signal chain and SNR analysis of the hardware intended are computed, the TRX solution is tested, and the noise floor and SNR at the front-end receive signal chain are measured. The developed hardware provides a noise floor of $-110$ dB, and the SNR achieved is up to $61$ dB. Even though the SNR obtained is acceptable for ultrasound imaging and diagnosis, the SNR can be further improved to form a vivid ultrasound image. We also discussed the testing methodology of the hardware developed.

Compared to the existing reported works, we conclude that our development work is the complete 128-channel TRX solution with the required external interfaces. The peak power consumption of the hardware developed is 22 W, which is well within the ultrasound system’s requirements. We also developed a digital beamformer processor board to integrate with the transceiver board, which provides a complete 128-channel ultrasound prototype solution. Sensor-to-display signal chain analysis is carried out in prototype systems to conclude that the developed ultrasound front-end hardware is superior in its noise performance and system integrity.

ACKNOWLEDGMENT

This work was supported by the Medical Electronics and Health Informatics (ME & HI) Division of Ministry of Electronics and Information Technology, Government of India, as per order No.1 (5)/2015-ME&HI dated 18/11/2015 under the ICDU Project and the microelectronics division of the Ministry of Electronics and Information Technology, Government of India, as per order No.9 (1)/2014-MDD dated 15-12-2014 under the SMDP-C2SD Project.

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How to cite this article: Kidar, J., et al.: Design of a 128-channel transceiver hardware for medical ultrasound imaging systems. IET Circuits Devices Syst. 1–13 (2021). https://doi.org/10.1049/cds.2020.0753