A fully differential switched-capacitor integrator based programmable resolution hybrid ADC architecture for biomedical applications

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1 | INTRODUCTION

The 21st century is marked as digital era by electronic industries which brought revolution in signal processing. Modern electronic systems employ sophisticated functional blocks which impact power consumption, cost, performance and reliability of the system. Digital signal processor (DSP) is able to implement complex algorithms and functions with high computational accuracy and power. Along with this, improved noise margin, error detection and correction codes made the transmission and storage of digital signals less prone to noise. Hence the analog circuit techniques in many applications were replaced by reliable, cost-effective, fast and flexible digital technologies. Thus, there is an extensive need for analog to digital converters (ADCs) and digital to analog converters (DACs) to avail benefits of digital signal processing as the real-world signals are analogue. Of late, design of ADCs has become critical, especially with technology scaling because the circuit noise is not decreasing as much as the technology/supply voltage does.

The advancements in healthcare system make humans life better day by day. Biomedical devices [1] help to monitor the patient's body and provide support systems round the clock without causing much inconvenience on their day-to-day life. It not only reduces the length of hospital stay for post-operative care but also offers superior monitoring and reporting process. Moreover, the pre-diagnosis of functional disorders and deadly diseases by these devices might save the life and also reduces the cost of medical care to a greater extent. In many cases, to monitor the biological signals, a wireless body sensor network (WBSN) [2] with multiple nodes is used. To extend battery life, the power consumed by these nodes should be as low as possible. In each sensor node, ADC is a critical block that interfaces physical world with DSP block. Literature study suggests that successive approximation register (SAR) ADC is the most suitable one by virtue of its characteristics like conversion accuracy, ultra-low-power consumption, simple design and technology scaling amenability [3,4]. Typically, SAR ADC [5] is implemented with a binary-weighted capacitor DAC, dynamic comparator and digital logic. The number of
capacitors used in the binary-weighted DAC is exponentially proportional to the resolution (N bits). The area, energy consumption and distortion due to mismatch are directly related to the number of capacitors used in DAC. Therefore, there are numerous switching techniques reported in literature to reduce the number of capacitors used in DAC circuit. Biomedical signals such as the electroencephalogram (EEG), electrocardiogram (ECG), breathing quality, measures of blood parameters such as oxygenation, glucose, cholesterol, c-reactive protein (CRP), erythrocyte sedimentation rate (ESR), platelet count, etc. have varying dynamic range and bandwidth. In addition, within a given application like ECG, to accomplish low- and high-resolution tasks at different intervals as shown in Figure 1, a variable-resolution ADC may be optimal. Hence, a power-efficient and fully programmable resolution ADC can substantially reduce the size and cost of the WBSN. In [7–16], adaptive-resolution ADC architectures are presented for implantable sensors. In all these papers, SAR ADC is designed with binary-weighted capacitive DAC using different switching methods.

The switched-capacitor integrator SAR ADC [7] is implemented using operational transconductance amplifier (OTA) with programmable unity gain bandwidth (UGB) and slew rate, dynamic comparator, capacitors, switches and control logic. The advantages of switched-capacitor integrator based SAR ADC over conventional SAR ADC are summarized as follows: the number of unit capacitors used in the binary-weighted DAC is exponentially proportional to the resolution (N bits). The area and energy consumption are directly related to the number of capacitors and the value of unit capacitor used in the DAC. One way to reduce the energy consumption is by reducing the unit capacitance. The large number of unit capacitors with the smaller unit capacitance makes the effect of capacitor mismatch more severe. Also, the binary-weighted capacitive SAR requires large number of switches which introduce more distortion. Whereas the differential switched-capacitor integrator based SAR ADC requires 6 capacitors and 16 switches only. Also, the resolution of ADC can be programmable without much modifications to the architecture.

**FIGURE 1** Segment depiction of an electrocardiogram signal [6]

![Segment depiction of an electrocardiogram signal](image)

**FIGURE 2** (a) Successive approximation register analog to digital converter (SAR ADC) block diagram. (b) SAR ADC with feedback integrator digital to analog converter. SIPO, serial-in–parallel-out

![Successive approximation register analog to digital converter (SAR ADC) block diagram](image)

**FIGURE 3** (a) First-order multi-bit delta-sigma modulator (DSM) block diagram. (b) First-order DSM with successive approximation register (SAR) quantizer. (c) Reduced block of first-order DSM with SAR quantizer. DAC, digital to analog converter. SIPO, serial-in–parallel-out

![First-order multi-bit delta-sigma modulator (DSM) block diagram](image)
Another advantage of switched-capacitor integrator based SAR ADC is that the reference voltages are sampled on the capacitors $C_3$ and $C_4$ in Figure 4a at the beginning of conversion. This makes the switched-capacitor integrator based SAR ADC less prone to any signal-dependent inaccuracies associated with the reference voltage compared to binary-weighted SAR ADC.

This paper presents a hybrid ADC with programmable resolution from 8 to 15 bits for biomedical applications. This proposed ADC operates in two modes of operation: (1) SAR ADC mode for lower resolution of 8–11 bits, and (2) delta-sigma modulator (DSM) with multi-bit quantizer for higher resolution of 12–15 bits. The organization of this paper is as follows. Section 2 explains the working principle and techniques used in the proposed programmable resolution ADC. Section 3 discusses the impact of circuit non-idealities on proposed ADC. Section 4 presents the design of building blocks such as OTA with programmable slew rate and UGB, dynamic comparator and digital control logic. Section 5 summarizes the performance parameters and compares with state-of-the-art designs. The paper is concluded with Section 6.

2 | OPERATING PRINCIPLE OF PROPOSED HYBRID ADC

The conventional SAR ADC is implemented using a sample and hold (S/H), comparator, serial-in-parallel-out (SIPO) register and N-bit feedback DAC blocks as shown in Figure 2a. Here, $f_s$ is the sampling frequency and $N$ is the resolution of ADC. The feedback DAC is implemented with a 1-bit DAC and discrete-time integrator as shown in Figure 2b. The discrete-time integrator accumulates the scaled reference voltage after every comparison cycle from 1-bit DAC and refreshes in each sampling phase. Thus, it fulfills the functionality of an equivalent $N$-bit DAC.
Figure 3a shows the block diagram of first-order multi-bit DSM ADC which can achieve high resolutions with oversampling and noise-shaping technique. The multi-bit ADC in the loop can be realized with a SAR quantizer which is shown in Figure 2b. In the block diagram shown in Figure 3b, there are two DACs, one operates at frequency $Nf_s$ used for SAR operation and another is an $N$-bit DAC which operates at a frequency of $f_s$ and used for noise-shaping purpose. This $N$-bit DAC can be implemented with a discrete-time integrator and 1-bit DAC as shown in Figure 2b. Since both the paths are using the same DAC structure, they can be reduced to one path. Further, by shifting the summing point towards the comparator, the integrator block operated at frequency $f_s$ added into both forward and feedback paths. The series connection of the integrator block and reset@$f_s$ blocks cancel with each other in the feedback path. Therefore, the reduced block diagram of first-order DSM with SAR quantizer can be redrawn as shown in Figure 3c. Hence the only difference between SAR quantizer of Figure 2b and the first-order DSM with SAR quantizer of Figure 3c is the reset@$f_s$ block. Therefore, it is possible to switch between SAR quantizer and first-order multi-bit DSM by controlling this reset@$f_s$ block. Further, the resolution of SAR quantizer is programmable by controlling the $N$ value, and the DSM resolution is controlled with an oversampling ratio (OSR).

Figure 4a shows circuit level implementation of the proposed 8-bit to 15-bit programmable resolution hybrid ADC which is controlled by a 3-bit input bus res[2 : 0]. The discrete-time integrator is implemented with a switched-capacitor integrator with fully differential OTA; capacitors $C_1$, $C_2$, $C_3$, $C_6$; and switches $S_{3,8}$. The reset@$f_s$ block is implemented with two switches $S_i$ and $S_s$. The feedback 1-bit DAC is implemented using capacitors $C_1$, $C_2$, $C_3$, $C_4$ and switches $S_{11:16}$. Figure 4b shows the timing waveform of the proposed hybrid ADC in the first-order DSM with SAR quantizer mode. The nodes $v_1$ and $v_2$ are connected to the left of capacitors $C_1$ and $C_2$, respectively. Conversion procedure is depicted with a flow chart as shown in Figure 5. The proposed hybrid ADC configured as a switched-capacitor integrator based SAR ADC from 8-bit to 11-bit resolutions and a first-order multi-bit DSM from 12-bit to 15-bit resolutions. The control bus res[2 : 0] is used to select the resolution of ADC. The signal-to-noise ratio (SNR) for first-order DSM with multi-bit quantizer is given by

$$SNR_{dB} = 6.02N + 1.76 + 30\log_{10}(OSR) - 10\log_{10}\left(\frac{\pi^3}{3}\right)$$

The resolution ($N$) for multi-bit DSM and OSR is chosen to target the corresponding SNR for each resolution from 12-bit to 15-bit. For example, res[2 : 0] = ‘100’ configures the proposed ADC as the first-order DSM with 7-bit SAR quantizer and an OSR of 16 which targets 75 dB SNR. The sampling and clock frequency, targeted SNR, SAR quantizer resolution, and OSR for all modes are calculated according to the resolution mode chosen by res[2 : 0].

The conversion process starts when reset is ‘high’. The total conversion can be divided into four phases as follows:

**Sampling phase:** In this phase, switches $S_{5}$, $S_{6}$, $S_{8}$, $S_{10}$, $S_{11}$ and $S_{12}$ are ‘ON’. Capacitors $C_1$ and $C_2$ sample the differential input signals $V_{ip}$ and $V_{in}$, through $S_{10}$, $S_5$ and $S_{11}$, $S_6$ switches, respectively. Also, capacitor $C_3$ samples the supply
voltage $V_{dd}$ through switch $S_{11}$ and capacitor $C_4$ discharges to ground through switch $S_{12}$. In 8-bit to 11-bit resolution modes, switches $S_1$ and $S_2$ are ‘ON’ thereby resetting the capacitors $C_5$ and $C_6$. This phase exists for a positive half cycle of the clock after the end of conversion (EoC). Further, to avoid the distortion due to charge injection, bootstrapped switches with bottom plate sampling are used.

**Charge accumulation phase**: This phase comes up during every negative half of clock cycle. In this phase, $S_3$, $S_4$, $S_5$, and $S_6$ switches are ‘ON’ and the remaining switches are ‘OFF’. Therefore, the capacitors $C_1$ and $C_2$ are connected between $V_{cm}$ and virtual short node. This forces the charge on capacitors $C_1$ and $C_2$ to transfer and accumulate on capacitors $C_5$ and $C_6$, respectively.

**Comparison phase**: This phase exists for a small interval which starts at the positive edge if EoC signal is low. In this phase, the differential outputs of OTA are compared and the decision bit is stored in SIPO register.

**Passive charge sharing phase**: This phase starts after the comparison phase in positive half cycle, in which the capacitors $C_1$, $C_2$, $C_3$ and $C_4$ involve in passive charge sharing through switches $S_9$, $S_{10}$, $S_{13}$, $S_{14}$, $S_{15}$ and $S_{16}$ based on the comparator output. As shown in Figure 5, if the comparator output is high, capacitors $C_1$, $C_4$ and $C_2$, $C_3$ share the charge, otherwise capacitors $C_1$, $C_3$ and $C_2$, $C_4$ share the charge, respectively. This allows to decide the comparison level for the next cycle.

The conversion starts with sampling phase and then followed by accumulation, comparison and passive charge sharing phases for $N$ cycles. At the EoC, the capacitors $C_5$ and $C_6$ are discharged by closing switches $S_1$ and $S_2$, when the proposed ADC is configured in SAR mode. In the first-order DSM mode, at the EoC of SAR quantizer, the capacitors $C_5$ and $C_6$ are left with the quantization error. Hence, the integration property allows noise shaping with an OSR. This characteristic allowed to obtain high resolutions.

### 3 | DISTORTION ANALYSIS

The ADC characteristics deviate from ideal due to non-idealities of OTA, capacitors’ mismatch and switches. This non-linearity reflects as a distortion in the output and degrades the effective number of bits (ENOB). The estimation of distortion shows the effect of each sub circuit and the specifications needed to achieve the required resolution.

#### 3.1 | Capacitor mismatch

The accuracy of SAR ADC depends on the matching of feedback capacitors. The physical design and manufacturing process control the variation of mismatch between capacitors. This kind of mismatch cannot be removed entirely but this can be viewed as a random statistical process and the variation in system characteristics can be estimated [17]. In fully differential circuits and charge sharing circuits, the relative values of capacitors are more important than absolute values. Therefore, the deviation or mismatch between the components is calculated as the normalized deviation from their mean value.

It is assumed that the capacitors $C_1$–$C_4$ are matched well and $\alpha_1$, $\alpha_2$, $\alpha_3$ and $\alpha_4$ are the normalized deviations of capacitors $C_1$–$C_4$ from their mean value, respectively.

\[
\alpha_i = \frac{\Delta C_i}{C_m} = \frac{C_i - C_m}{C_m}
\]

\[
C_{m1} = \frac{C_1 + C_2 + C_3 + C_4}{4}
\]

\[
\sum_{i=1}^{4} \alpha_i = \alpha_1 + \alpha_2 + \alpha_3 + \alpha_4 = \frac{C_1 + C_2 + C_3 + C_4 - 4C_{m1}}{C_{m1}} = 0
\]

Similarly, $\alpha_5$ and $\alpha_6$ are the normal deviations of $C_5$ and $C_6$, respectively.

\[
C_{m2} = \frac{C_5 + C_6}{2}
\]

\[
\alpha_5 = \frac{C_5 - C_{m2}}{C_{m2}}
\]

\[
\alpha_6 = \frac{C_6 - C_{m2}}{C_{m2}}
\]

\[
\therefore \alpha_5 + \alpha_6 = \frac{C_5 + C_6 - 2C_{m2}}{C_{m2}} = 0
\]

Therefore, from a statistical point of view, it can be assumed that the sum of normalized deviations is zero. Accordingly,

\[
\sum_{i=1}^{4} \alpha_i = \alpha_1 + \alpha_2 + \alpha_3 + \alpha_4 = 0
\]

\[
\alpha_5 + \alpha_6 = 0
\]
output is ‘1’ in all cycles. The standard deviation ($\sigma$) of this INL$_{\text{max}}$ relates to the standard deviation of capacitor ($\sigma_{\text{AC}}$) as shown in Equation (5).

$$|\text{INL}|_{\text{max}} = (a_1 + a_2)2^{N-2} \sum_{k=1}^{N-1} \frac{k}{2^k}$$

$$= (a_1 + a_2)2^{N-2}\left(2 - \frac{N + 1}{2^{N-1}}\right) \quad (4)$$

$$\sigma_{\text{INL}}_{\text{max}} = 2^{N - N - 1} \frac{\sigma_{\text{AC}}}{\sqrt{2C}} \quad (5)$$

### 3.2 OTA non-idealities

In Section 2, operation of the proposed ADC is demonstrated by assuming infinite gain, bandwidth for OTA and also instant charge transfer between capacitors. In reality, due to the finite gain of OTA, during charge sharing, some charge will be left behind in capacitors $C_1$ and $C_2$, which is known as static error voltage. Similarly, the finite UGB and slew rate of amplifier causes settling time error, which is known as dynamic error. These errors depend on the input signal, which causes harmonics at the output.

#### 3.2.1 Finite gain of OTA

The switched-capacitor integrator transfer function is derived as follows [18] by analysing the finite gain effect of OTA. During sampling phase ($\phi_1$), $C_1$ charges to the input voltage ($v_{\text{in}}[n]$), while $C_3$ holds the charge ($q_3[n - 1]$) held in previous cycle. Owing to the finite gain ($A$) of OTA, the voltage on the left side of $C_3$ is $-v_{\text{op}}[n - 1]/A$. Thus, the charge on $C_3$ ($q_3[n - 1]/A$) can be written as

$$q_3[n - 1] = C_3 \left(1 + \frac{1}{A}\right)v_{\text{op}}[n - 1] \quad (6)$$

In charge integration phase, it is assumed that the charge $q$ flows out from $C_1$ to $C_3$ and the charge on $C_1$ becomes

$$q_1[n] - q = C_1 \left(\frac{v_{\text{op}}[n]}{A}\right) \quad (7)$$

From Equation (7), the transferred charge $q$ can be written as

$$q = q_1[n] - C_1 \left(\frac{v_{\text{op}}[n]}{A}\right) \quad (8)$$

After, charge ($q$) transfer takes place, the charge on capacitor $C_3$ becomes

$$q_3[n] = q_3[n - 1] + q$$

$$q_3[n] = q_3[n - 1] + q_1[n] - C_1 \left(\frac{v_{\text{op}}[n]}{A}\right) \quad (9)$$

$$v_{\text{op}}[n] = \frac{q_3[n] + q_1[n]}{C_3 \left(1 + \frac{1}{A} + \frac{C_1}{C_3A}\right)}$$

$$v_{\text{sim}}[n] = \frac{q_3[n] + q_1[n]}{C_3 \left(1 + \frac{1}{A} + \frac{C_2}{C_3A}\right)} \quad (10)$$

#### TABLE 1 SAR ADC voltage reference levels due to capacitors’ mismatch

| Cycle | Voltage reference level | Error in Voltage reference level ($V_o$) |
|-------|-------------------------|----------------------------------------|
| 1     | 0                       | 0                                      |
| 2     | $(-1)^{n-1} \left(1 - \frac{n+1}{2^k}\right) V_{dd}$ | $(-1)^{n-1} (a_1 + a_2) \frac{V_{dd}}{2}$ |
| 3     | $(-1)^{n-1} \left(1 - \frac{n+2}{2^k}\right) V_{dd} + (-1)^{n-1} \left(1 - \frac{2n+3}{2^k}\right) V_{dd}$ | $(-1)^{n-1} (a_1 + a_2) \frac{V_{dd}}{2} + 2(-1)^{n-1} (a_1 + a_2) \frac{V_{dd}}{4}$ |
| 4     | $(-1)^{n-1} \left(1 - \frac{n+3}{2^k}\right) V_{dd} + (-1)^{n-1} \left(1 - \frac{2n+5}{2^k}\right) V_{dd}$ | $(-1)^{n-1} (a_1 + a_2) \frac{V_{dd}}{2} + 2(-1)^{n-1} (a_1 + a_2) \frac{V_{dd}}{4}$ |

Abbreviation: SAR ADC, successive approximation register analog to digital converter.
Voltage reference levels deviate from the ideal voltage references because of this repetitive gain error which results in non-linearity in ADC transfer characteristics. Equation (11) shows the voltage reference error due to the finite gain of OTA in the $n$th cycle of SAR ADC operation:

$$V_e = -\frac{C_1 V_{dd}}{C_5 A} \sum_{k=1}^{N-1} (-1)^{k-1} \frac{k}{2(k+1)}$$

The maximum integrated non-linearity can be calculated as

$$|\text{INL}|_{\text{max}} = \left| \frac{C_1}{C_5 A} (2^N - N) \right|$$

From Equation (12), the OTA gain needs to satisfy the following relation to achieve INL less than 0.5 LSB:

$$A > \frac{C_1}{C_5} (2^{N+1} - 2N - 2)$$

In DSM operation, the variation in integrator transfer function alters the signal transfer function (STF) and noise transfer function (NTF). By substituting Equation (6) and $q_1[n] = C_1v_{ip}[n]$ in Equation (9) and applying $z$ transform results in

$$V_{op}(z) = \frac{C_1/C_5}{(1 + 1/z)} \frac{V_{ip}(z)}{(1 - z^{-1} / (1 + \epsilon))}$$

Similarly,

$$V_{om}(z) = \frac{C_2/C_6}{(1 + 1/z)} \frac{V_{im}(z)}{(1 - z^{-1} / (1 + \epsilon))}$$

where

$$\epsilon = \frac{C_1}{C_5(A + 1)} = \frac{C_2}{C_6(A + 1)}$$

Since $C_1 = C_2$ and $C_5 = C_6$, the loop filter transfer function of DSM can be written as

$$L(z) = \frac{V_{op}(z) - V_{am}(z)}{V_{ip}(z) - V_{im}(z)} = \frac{g\cdot p}{1 - p z^{-1}}$$

where $g = \frac{C_1}{C_5 A} (A + 1)$ and $p = \frac{1}{1 + \tau}$ are integrator gain and pole, respectively.

![FIGURE 6 Pole-zero mapping: (a) signal transfer function and (b) noise transfer function for different operational transconductance amplifier gains](image)

Therefore, the STF and NTF become

$$STF(z) = \frac{L(z)}{1 + L(z)} = \frac{g\cdot p}{1 - p(1 - g)z^{-1}}$$

$$NTF(z) = \frac{1}{1 + L(z)} = \frac{1 - p z^{-1}}{1 - p(1 - g)z^{-1}}$$

From Equation (17), it can be observed that the finite amplifier gain has two effects: a small reduction in the integrator’s gain constant and an inward shift of the integrator’s pole ($z - 1$). The change in integrator’s gain constant is equivalent to a coefficient error ($\epsilon$) and also causes the extra poles of both STF and NTF move away from the origin. Thus, this
change in integrator gain has a negligible impact on the in-band SNR degradation. In contrast to this, the second effect, the shift in pole location of loop filter is more problematic because the loop filter pole becomes an NTF zero. This movement of an NTF zero affects the attenuation of noise in pass band.

This phenomenon is modelled in MATLAB for an integrator gain ($C_1/C_3$) of 0.3. The pole-zero movement in STF and NTF with OTA gain ($A$) is observed and plotted in Figure 6. One can observe that the pole of STF is moving away from $z = 0.7$ as OTA gain ($A$) decreases and zero stays at the origin. This results in the gain reduction in the signal path, as shown in frequency response of STF in Figure 7. In the pole-zero plot of NTF, shown in Figure 6, as OTA gain ($A$) decreases, the NTF zero moves from $z = 1$ towards $z = 0$ and pole moves away from $z = 0.7$ which is similar to STF pole movement. The movement of NTF zero causes reduction of attenuation as can be observed in Figure 7. From all of the discussions above, it can be concluded that the finite dc gain of OTA is one of the limiting factors for modulator to achieve maximum SNR.

Further, a low-order modulator is susceptible to the nonlinear phenomenon of dead bands. A dead band is a range of inputs that yields the same periodic output sequence and hence the same post-decimation output. Therefore, in dead band, a dc input with a small magnitude appears as a zero input. The reason behind this is the shift in NTF’s zero from $z = 1$ to $z = p$, which limits the NTF’s DC gain to $(1 - p)/(1 - p + gp) = 1/(1 + A)$ instead of zero. Thus, the modulator loses its ability to achieve infinite precision with dc signals. To register small dc input values ($u$), the following expression [18] should satisfy

$$A > \frac{1}{2|u|} \quad (20)$$

It is assumed that the OTA gain is constant over output swing in all the above discussions. In practice, OTA gain is a function of input voltage, which causes harmonic distortion. Since the magnitude of the associated input-referred error signal is no more than $v_{\text{out max}}/A$, the maximum output of OTA ($v_{\text{out max}}$) is $(C_1/C_3) v_{\text{in max}}$. Therefore, upper limit on the total harmonic distortion (THD) of the signal is

$$THD = \frac{C_1}{C_3} \frac{1}{A} \quad (21)$$
Even if there is no explicit distortion limit for the ADC, it is needed to ensure that the loop filter is sufficiently linear so that the distorted out-of-band quantization noise does not fall in the noise notch. Based on these considerations, the amplifier is designed for a particular gain, followed by modulator simulations to verify that the amplifier's linearity is adequate.

Further, the programmable resolution ADC with finite OTA gain is modelled in MATLAB. The ADC is simulated with a sinusoidal signal of frequency 123 Hz for resolutions from 8-bit to 15-bit. As the OTA gain is varied from 0 to 80 dB, SNR, THD and signal to noise and distortion ratio (SNDR) are observed as shown in Figure 8. It can be seen that the SNR improves with the OTA gain. It is observed that, the gain around 80 dB ensures the THD below −90 dBc, which is needed in case of 15-bit resolution. From this result it is concluded that, OTA with 80 dB gain serves our purpose of designing an ADC that is programmable from 8-bit to 15-bit.

3.2.2 | Settling time considerations

In charge integration phase it is assumed that every conversion is given sufficient time for charge transfer to settle completely within the required resolution. This settling time must be less than half the clock period [19]. Typically, at large inputs, the OTA saturates and the charge transfer is limited by the bias current. This is known as slewing and the rate at which the

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**TABLE 2** Computation of capacitor size \( C_1 \), slew rate and UGB requirements of PADC for various resolutions

| Target resolution | OSR | SNR (dB) | \( \frac{C_{\text{ref}}}{C_1} \geq \) | \( f_{\text{clk}} \) (kHz) | Slew rate (V/μs) | UGB (MHz) | I (μA) |
|-------------------|-----|---------|----------------------|----------------|----------------|-----------|-------|
| 8                 | 1   | 50      | 4.05 (μV)\(^2\)     | 8              | 18             | 0.08      | 0.43  |
| 9                 | 1   | 56      | 1.02 (μV)\(^2\)     | 9              | 20             | 0.09      | 0.47  |
| 10                | 1   | 62      | 0.26 (μV)\(^2\)     | 10             | 22             | 0.1       | 0.51  |
| 11                | 1   | 68      | 64.2 (μV)\(^2\)     | 11             | 24             | 0.11      | 0.55  |
| 12                | 16  | 75      | 12.8 (μV)\(^2\)     | 7              | 256            | 1.2       | 4.9   |
| 13                | 16  | 81      | 3.2 (μV)\(^2\)      | 8              | 288            | 1.3       | 5.4   |
| 14                | 32  | 86      | 1.02 (μV)\(^2\)     | 8              | 576            | 2.7       | 10    |
| 15                | 128 | 92      | 0.26 (μV)\(^2\)     | 6              | 1792           | 9         | 27    |

Abbreviations: OSR, oversampling ratio; SNR, signal-to-noise ratio; UGB, unity gain bandwidth.

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**FIGURE 9** Folded cascode operational transconductance amplifier with programmable bias circuit
charge transfer happens is called slew rate. Once the OTA input voltage falls under the input range of OTA, the transconductance \( g_{m} \) decides the minimum time needed to settle within the required accuracy. This is known as linear settling phase. It is assumed here that, slewing phase exists for \( x \) part of \( T_{clk}/2 \) and rest of \( T_{clk}/2 \) is allocated for linear settling phase. The boundary conditions for bias current and the transconductance can be derived as follows. The maximum charge that needs to be transferred from capacitor \( C_{1} \) to \( C_{5} \) is \( C_{1} V_{dd} \) in \( x T_{clk}/2 \) time and therefore, the bias current should follow the relation as shown in Equation (22).

\[
I > \frac{C_{1} V_{dd}}{x T_{clk}/2} \tag{22}
\]

In linear settling phase, the time constant can be written [18] as

\[
\tau = \frac{C_{1} + C_{L} + C_{1} C_{L}/C_{S}}{g_{m} g_{m}} \approx \frac{C_{1}}{g_{m}} \tag{23}
\]

The settling time required to keep normalized error voltage below \(-100 \text{ dB}\) is

\[
\left(1 - x\right) \frac{T_{clk}}{2} = \ln\left(10^{5}\right) \approx 12\tau \tag{24}
\]

The required \( g_{m} \) can be computed as
From Equations (22) and (25), the $g_m/I$ ratio can be written as

$$g_m \approx \frac{C_1}{(1 - x)T_{clk}/24}$$

(25)

From Equations (22) and (25), the $g_m/I$ ratio can be written as

$$\frac{g_m}{I} = \frac{12}{V_{dd}} \frac{x}{1 - x}$$

(26)

4 | REALIZATION OF PROGRAMMABLE RESOLUTION ADC

The ADC works as SAR ADC for 8-bit to 11-bit resolution and a multi-bit quantizer DSM for 12-bit to 15-bit. Here, the SAR ADC works as a multi-bit quantizer. The proposed programmable resolution ADC is built with OTA, comparator, digital control logic, bootstrapped switch, capacitors and switches. This section discusses the design of each of these blocks. The total input-referred noise power for a switched-capacitor integrator [20] is given as

$$v_{n,\text{diff}}^2 \approx 4 \cdot \frac{2kT}{C_1}$$

(27)

By considering the in-band mean-square noise, the value of capacitor $C_1$ is calculated and tabulated as shown in Table 2 using Equation (28) for a required SNR. Therefore, the capacitor $C_1$ is determined as 1 pF subject to the noise for 15-bit resolution. The value of capacitor $C_5$ is determined as 3.3 pF from the integrator gain which is 0.3:

$$C_1 \geq \frac{64kT}{V_{dd}^2 \text{OSR}^{10 \text{SNR/10}}}$$

(28)

4.1 | OTA

The folded cascode (FC) OTA [21] is used to implement the switched-capacitor integrator as shown in Figure 9. In the previous section, it is discussed that a DC gain of 80 dB is sufficient to keep the third harmonic distortion below -90 dBc. The slew rate and UGB requirements of OTA depend on the clock frequency used for a particular resolution from 8-bit to 15-bit. The designed ADC operates as SAR ADC from 8-bit to 11-bit resolutions and first-order multi-bit SAR quantizer DSM from 12-bit to 15-bit resolutions. Therefore, a first-order N-bit quantizer DSM requires $(N + 1)$ OSR clock cycles for conversion. The Nyquist sampling frequency is 2 kHz. Table 2 lists the quantizer resolution, OSR and frequency ($f_{clk}$) of the clock. The required slew rate and UGB of OTA are determined from clock frequency using Equations (22) and (23) and are tabulated. The bias current of FC OTA and clock frequency are chosen according to ADC resolution.

The FC OTA is designed such that it operates in weak inversion region for all bias currents. The transistors are sized in such a way that, the ficker noise as well as the effect of transistor mismatch [22] are less. Figure 10 shows AC response of FC OTA for all bias currents. It is observed that, the DC gain of OTA is greater than 80 dB in all these cases and also the required slew...
rate and UGB have been achieved. Also, the phase margin is above 60° for all cases which can be seen from Figure 10. Further, the DC analysis is carried out by varying the input voltage. Figure 11 shows the DC gain variation over output swing. It confirms the variation in DC gain is less than 1 dB over ±0.54 V output swing, which helps to reduce the harmonics.

4.2 Switches

The proposed programmable resolution ADC consists of a total of 16 switches. It is required to consider the effects like charge injection, clock feed-through and gate voltage dependent resistance while implementing switches, to reduce harmonic distortion. The NMOS transistor can switch ‘ON’ for voltages below \( V_{\text{dd}} - V_{\text{thn}} \) and the PMOS transistor can switch ‘ON’ for voltages above \( |V_{\text{thp}}| \) without distortion. In other cases, transmission gate is used as a switch when node voltages swing between 0 and \( V_{\text{dd}} \). Sampling switches \( S_9, S_{10} \) and \( S_3, S_4 \) are implemented using bootstrapped switch [23] to reduce the input dependent non-linearity. Switches \( S_1, S_2, S_5, S_6, S_7, S_8, S_{12}, S_{13} \) and \( S_{16} \) are implemented with NMOS transistors and \( S_{15} \) are implemented using PMOS transistors. Figure 12 shows the output spectrum of bootstrapped circuit, which ensures that all harmonics are less than –100 dBc.

4.3 StrongARM dynamic comparator

The schematic diagram of a strongARM comparator [24] is shown in Figure 13, which is generally used in ADCs because of its positive feedback, high input impedance, rail-to-rail output swing and negligible static power consumption. In reset phase, the \( \text{clk} \) signal is low, thus the transistor M3 is in ‘cut-off’

| Target resolution | OSR | SAR | \( f_{\text{clk}} \) | ENoB (bits) | SFDR (dB) | Power (μW) |
|-------------------|-----|-----|----------------|------------|----------|------------|
| 8                 | 1   | 8   | 18             | 7.17       | 58.37    | 0.856      |
| 9                 | 1   | 9   | 20             | 8.2        | 63.5     | 1.02       |
| 10                | 1   | 10  | 22             | 9.18       | 69.14    | 1.17       |
| 11                | 1   | 11  | 24             | 10.14      | 66.3     | 1.287      |
| 12                | 16  | 7   | 256            | 11.22      | 76.4     | 12.47      |
| 13                | 16  | 8   | 288            | 11.73      | 77.8     | 14.95      |
| 14                | 32  | 8   | 576            | 12.9       | 83.7     | 33.06      |
| 15                | 128 | 6   | 1792           | 13.97      | 91.63    | 98.35      |

Abbreviations: ENoB, effective number of bits; OSR, oversampling ratio; SAR, successive approximation register; SFDR, spurious-free dynamic range.
region and the output nodes \(outp, outm\) charged to \(V_{dd}\) through the transistors M8 and M9, respectively. When \(clk\) signal goes high, the decision phase starts and output nodes start discharging at different rates depending upon the input voltages \(V_{ip}\) and \(V_{im}\). Meanwhile, when one of the output nodes reaches \(V_{dd} - |V_{tip}|\), corresponding transistor M6 or M7 switches ‘ON’ and the positive feedback between back-to-back connected inverters (M4, M6 and M5, M7), also known as latch, enables and pulls one of the output nodes to \(V_{dd}\) and other to \(gnd\). This charge and discharge process takes some time to make decision which is known as a comparator delay. This delay can be classified into two parts: \(t_{on}\) is the time required to discharge one of the output nodes to \(V_{dd} - |V_{tip}|\) and \(t_{latch}\) is the time needed for latch decision.

### 4.4 Digital control logic unit

The block level diagram of digital control logic circuit is shown in Figure 4a. It is designed using Verilog-A and then synthesized. The resolution of ADC is programmable using a 3-bit select bus \(res[2:0]\). The SAR resolution controller programs the counter as per the chosen resolution. The counter starts counting on every positive edge of clock and generates \(EoC\) signal when it reaches the upper limit. Meanwhile, the comparator output \((D_{out})\), \(EoC\) and \(clk\) as input signals and generates the control signals for all switches \((S_{1:16})\) in every clock cycle.

### 5 RESULTS

The proposed programmable resolution ADC is laid out in UMC 180 nm 1P6M CMOS technology as shown in Figure 14 and occupies an area of 725 \(\mu m \times 315 \mu m\). The capacitors \(C_1 = C_2 = C_3 = C_4 = 1\) \(pF\) and \(C_5 = C_6 = 3.3\) \(pF\) are implemented using metal-insulator-metal capacitors and dummy capacitors are placed around this capacitor bank to minimize the interference as well as mismatch. Also, the analog and digital layouts are separated by guard rings and distinct supply voltages are used to reduce cross talk. Further, the post layout simulations are carried out with an ADC full scale range of 1.8 V differential with a Nyquist sampling frequency of 2 \(kS/s\). Figures 15 and 16 show the ADC output spectrum for resolutions from 8-bit to 15-bit, respectively. The first-order noise shaping (20 \(dB/decade\)) can be observed in the resolution modes 12-bit to 15-bit. The number of fast fourier transform (FFT) points used for ADC simulations from 8-bit to 11-bit is 256. Twelve-bit and thirteen-bit ADC simulations used 4096 FFT points. Fourteen-bit ADC simulations used 8192 FFT points and 15-bit ADC simulations used 32,768 FFT points. The results of ADC simulations for various resolution modes (8-bit to 15-bit) are summarized in Table 3. The proposed ADC offers adequate ENOB for each resolution mode.

Figure 17 shows the plot of SNDR of the proposed ADC over a normalized input with respect to full signal swing for all resolution modes (8-bit to 15-bit). Also, Figure 18 depicts a consistent SNDR over an input signal frequency for all target resolutions. Figure 19 shows the stacking diagram of power consumption by OTA, digital control logic, DAC and comparator. Table 4 shows the comparison of the performance of proposed ADC with similar type ADCs. It can be seen that the proposed ADC is on par with many designs found in state-of-the-art and demonstrated a new approach to implement programmable resolution ADC.
the capacitors’ mismatch is also calculated. The proposed ADC is designed and laid out in UMC 180 nm 1P6M CMOS technolog. Further, the non-as finite v alues of gain, UGB and slew rate on ADC characterized with tuneable UGB and slew rate is used in the design be operated in both SAR mode and DSM mode. A FC OTA is presented in this paper. The proposed ADC is implemented An 8

6  |  CONCLUSION

An 8-bit to 15-bit programmable resolution ADC has been presented in this paper. The proposed ADC is implemented with a fully differential switched-capacitor integrator and it can be operated in both SAR mode and DSM mode. A FC OTA is designed with tuneable UGB and slew rate in the design of proposed ADC. The effects of non-idealities of OTA, such as finite values of gain, UGB and slew rate on ADC characteristics are modelled and studied through behavioural simulations. Further, the non-linearity in ADC characteristics due to the capacitors' mismatch is also calculated. The proposed ADC is designed and laid out in UMC 180 nm 1P6M CMOS technology and occupies an area of 0.228 mm². Post layout simulations show that the proposed ADC achieves an adequate SNDR in all resolution modes (8-bit to 15-bit). The total design consumes 0.86 to 98 μW in 8-bit to 15-bit resolutions, respectively, from a supply voltage of 1.8 V.

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