Single Dual-X Current Conveyor based BASK/BPSK Modulators

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Abstract. Two voltage mode digital modulators have been proposed i.e. Binary Amplitude Shift Keying (BASK) modulator and Binary Phase Shift Keying (BPSK) modulator. Both circuits use Dual-X Second Generation Current Conveyor (DXCCII) as the active building block and have the advantages of proper input impedances and use of grounded resistor. Detailed mathematical analysis of both circuits are given. The circuits have been simulated with SPICE using 0.35µm CMOS technology parameters. The supply voltage of ±1.8 V is used. Much satisfactory results have been obtained with the proposed circuits.

Keywords: BASK; BPSK; DXCCII; modulators.

1. Introduction

Modulation is a process where one of the parameters of the carrier signal, which can be amplitude, phase or frequency, is varied linearly according to the variations in the message signal or modulating signal. With the modulation, the information contained in the message signal is transferred to the carrier signal. When modulation is done for the digital signals then it is known as the digital modulation. The device that performs this modulation is known as the digital modulator. The digital signal is a basically a binary signal in the form of 0s and 1s and it is a low pass signal and can’t be transmitted through the wireless medium, so in order to transmit the digital signal through wireless medium, modulation is required. In Binary Amplitude Shift Keying (BASK), the binary 1 is represented by the presence of carrier signal while binary 0 is represented by the absence of carrier signal whereas in Binary Phase Shift Keying (BPSK), the binary 1 is represented by the presence of in phase carrier signal while binary 0 is represented by the presence of 180° out of phase carrier signal. Infrared (IR) remote controls, transmitter and receiver in optical fiber communication employ BASK, and broadband modems, satellite communication, mobile phones employ BPSK.

Many new active building blocks have been introduced in recent past to explore above mentioned applications and one such trendy block is second generation current conveyor (CCII) [1] and inverting CCII [2]. Literature survey shows that one another most trending block that can be explored to implement modulation process is dual X second generation current conveyor (DXCCII) [3,4]. As per literature survey, two EXCCII based voltage mode digital modulator circuits are reported in [5] and [6] which provide simultaneous ASK and BPSK modulation processes. A current mode BASK modulator circuit has been reported in [7] making use of two MO-CCCCTA. A voltage mode BASK
modulator using only one CC III+ has been reported in [8]. Voltage mode memristor based BASK and BPSK modulators are presented in [9]. DPCCII based BASK modulator is reported in [10]. Further voltage mode MO-CCCCC, digitally programmable CDTA and MO-OTA based BASK and BPSK modulator circuits are reported in [11], [12] and [13] respectively. A DXCCII based modulator topology has also been presented in [6] which performs BPSK modulations but unexplored and unanalyzed.

The newly proposed BASK modulator circuit employs single DXCCII, one NMOS transistor and one grounded resistor while BPSK modulator circuit uses single DXCCII, one NMOS and one PMOS transistor and one grounded resistor. This article includes total of six sections including introduction in Section-1. DXCCII block description is given in Section-2 followed by proposed BASK and BPSK modulators in Section-3 & 4 respectively. Proposals simulation verification is reported in Section-5 and concluded in Section-6.

2. DXCCII Description

The DXCCII, conceptually, is a combination of CCII [1] and ICCII [2]. It is therefore more versatile building block as it has the features of both the current conveyors i.e. CCII and ICCII. The block diagram of DXCCII [3] is shown below in Fig. 1. It has 5 terminals named as Y, Xp, Xn, Zp and Zn. Xp is called as the non-inverting X terminal while Xn is called as the inverting X terminal. Y is an input terminal with high impedance. Xp and Xn are terminals with low impedance while Zp and Zn are terminals with high impedance.

Figure 1. Block diagram of DXCCII [3].

Table 1. (W/L) Ratio of CMOS for DXCCII [3].

| Transistor | W(µm) | L(µm) |
|------------|-------|-------|
| M1, M2    | 1.4   | 0.7   |
| M3, M7, M8| 2.8   | 0.7   |
| M4, M5    | 2.4   | 0.7   |
| M6, M9, M10| 4.8 | 0.7   |
| M11 to M20| 9.6   | 0.7   |

Ideally, the voltages and currents relationships of various terminals can be described by the following matrix [3] mentioned below in (1).

\[
\begin{bmatrix}
 I_Y \\
 V_{Xp} \\
 V_{Xn} \\
 I_{Zp} \\
 I_{Zn}
\end{bmatrix} =
\begin{bmatrix}
 0 & 0 & 0 & 0 & 0 \\
 1 & 0 & 0 & 0 & 0 \\
 -1 & 0 & 0 & 0 & 0 \\
 0 & 1 & 0 & 0 & 0 \\
 0 & 0 & 1 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
 V_Y \\
 I_{Xp} \\
 I_{Xn} \\
 I_{Zp} \\
 I_{Zn}
\end{bmatrix}
\] (1)
The CMOS implementation of the DXCCII used in the proposed circuits is shown in Fig. 2. The aspect ratio of transistors used in the implementation of DXCCII are given in Table 1 [3].

3. Proposed BASK Modulator

The proposed BASK modulator is shown in Fig. 3 below.

3.1 Operation of the proposed BASK modulator

$V_c$ is the sinusoidal carrier signal. It carries the modulating signal $V_m$. Voltage $V_c$ is applied at the high input impedance terminal Y of the DXCCII. Voltage $V_c$ is given as

$$V_c = A_c \sin(2\pi f_c t)$$

Where

- $A_c$ is the amplitude of the carrier signal voltage $V_c$,
- $t$ is the time period and $f_c$ is the frequency in hertz (Hz) or cycles/second.

This carrier signal voltage $V_c$ is copied at the Xp terminal of the DXCCII, that is

$$V_{Zp} = V_{Xp} = V_c$$

voltage $V_m$ is the bipolar modulating signal.

voltage $V_{ASK}$ is the BASK modulated output voltage signal.

The $M_{T1}$ is used as a switch. The modulating signal $V_m$ is applied at the high impedance gate terminal of this transistor. When voltage $V_m$ is positive, the $M_{T1}$ turns on and works as a closed switch, and when voltage $V_m$ is negative, the $M_{T1}$ turns off and works as an open switch. The gate voltage of $M_{T1}$ depends on the amplitude of the modulating signal $V_m$. And the drain voltage of $M_{T1}$ depends on the amplitude of the carrier signal $V_c$, which is very small as voltage $V_c$ is much smaller in magnitude than voltage $V_m$. The source voltage of $M_{T1}$ depends on the voltage $V_{ASK}$ developed across the resistor R.
Therefore, whenever $M_{T1}$ is on, it always works in the non-saturation region or the ohmic region as it always holds the condition of working in ohmic region which is given as

$$V_{DSn} < V_{GSn} - V_{THn} \quad (4)$$

where $V_{DSn}$ is the drain to source voltage of $M_{T1}$, $V_{GSn}$ is the gate to source voltage of $M_{T1}$, and $V_{THn}$ is the threshold voltage of $M_{T1}$. $V_{THn}$ for NMOS is positive.

The on resistance of this $M_{T1}$ used as a switch is denoted by $R_{on,n}$. From [6], for the ohmic region, the resistance $R_{on,n}$ is therefore expressed as

$$R_{on,n} = \frac{1}{(W/L_n) \mu_n C_{ox,n}(V_{GSn} - V_{THn} - V_{DSn})} \quad (5)$$

Where $(W/L)_n$ is the aspect ratio of $M_{T1}$, $\mu_n$ is the mobility of electron, and $C_{ox,n}$ is the gate oxide capacitance per unit area, of $M_{T1}$. It can be seen from the equation (5) that the $R_{on,n}$ varies with voltage $V_{GSn}$ and voltage $V_{DSn}$. But, since the on resistance $R_{on,n}$ is much smaller in magnitude than the magnitude of the external resistor $R$, therefore the effect of variation of $R_{on,n}$ on the BASK modulated output voltage $V_{ASK}$ is negligible. Mathematically, it can be expressed by the following equations written below

$$R_{on,n} \ll R \quad (6)$$

The BASK modulated output voltage is given as

$$V_{ASK} = I_{out} \times R \quad (7)$$

The voltage $V_A$ at node A is equal to the voltage $V_{Xp}$, that is

$$V_A = V_{Xp} \quad (8)$$

Also, when the $M_{T1}$ is on, then the total resistance $R_{total,n}$ between node A and ground is equal to the sum of the on resistance $R_{on,n}$ of the $M_{T1}$ and the external resistance $R$, i.e.

$$R_{total,n} = R_{on,n} + R \quad (9)$$

The output current $I_{out}$ is given as

$$I_{out} = \frac{V_A}{R_{total,n}} \quad (10)$$

From equations (8), (9) and (10)

$$I_{out} = \frac{V_{Xp}}{R_{on,n} + R} \quad (11)$$

From equations (6) and (9)

$$R_{total,n} = R_{on,n} + R \cong R \quad (12)$$

Therefore from equations (11) and (12), $I_{out}$ is given as

$$I_{out} \cong \frac{V_{Xp}}{R} \quad (13)$$

Thus from the equations (7) and (13), it can be concluded that the variation in the output current $I_{out}$ because of $R_{on,n}$ is negligible and therefore, the effect on the output voltage $V_{ASK}$ because of the variations in $R_{on,n}$ is also negligible. When the $M_{T1}$ working as a switch is in off condition than the associated resistance is denoted by $R_{off,n}$. $R_{off,n}$ is ideally infinite as the $M_{T1}$ is in non-conducting state. Now when the voltage of the modulating signal $V_m$ is positive (logic high), $M_{T1}$ turns on and the equal amount of the currents developed at $Xp$ and $Zp$ terminals of the DXCCII flow towards the node A, which then get added up at the node A as no current goes to the gate terminal of $M_{T1}$ and then the
net current flows through the transistor MT1 and then flows through the resistor R and then goes to the ground. The two currents developed at Xp and Zp terminals of the DXCCII linearly depend on the voltage $V_{XP}$ as can be observed from the equation (13). As the voltage $V_{XP}$ is AC in nature therefore the currents developed because of it are also AC in nature and since these two currents add up at the node A and therefore the resultant current is also AC in nature which flows through the resistor R developing an AC voltage $V_{ASK}$ in return across it which is in phase with the carrier signal voltage $V_c$. When the voltage of the modulating signal $V_m$ is negative (logic low), MT1 turns off and therefore no current flows through the resistor R and the voltage $V_{ASK}$ developed across it is zero. This way, the ASK modulated output voltage $V_{ASK}$ is thus obtained across the resistor R.

The overall operation of the proposed BASK modulator can therefore be summarized by these two equations as mentioned below

$$V_{ASK} = I_{out} \times R \cong V_c$$

when $V_m$ is positive or logic high (NMOS MT1 is on)

$$V_{ASK} = 0;$$

when $V_m$ is negative or logic low (NMOS MT1 is off)

### 4. Proposed BPSK Modulator

The proposed BPSK modulator is shown in Fig. 4.

4.1 Operation of the proposed BPSK modulator

$V_c$ is the sinusoidal carrier signal. It carries the modulating signal $V_m$. $V_c$ is applied at the high input impedance terminal Y of the DXCCII. $V_c$ is given as

$$V_c = A_c \sin(2\pi f_c t)$$

Where

$A_c$ is the amplitude of the carrier signal voltage $V_c$, t is the time period and $f_c$ is the frequency in hertz (Hz) or cycles/second. This carrier voltage $V_c$ is copied at the Xp terminal of the DXCCII, that is

$$V_{zp} = V_{xp} = V_c = A_c \sin(2\pi f_c t)$$

And the voltage developed at the Xn terminal of DXCCII is the inverted carrier voltage $V_c$, that is

$$V_{zn} = V_{xn} = -V_c = A_c \sin(2\pi f_c t)$$

$V_m$ is the bipolar modulating signal. $V_{PSK}$ is the BPSK modulated output voltage signal.

The MT1 and MT2 are used as the two switches. The modulating signal $V_m$ is applied at the high impedance gate terminals of these transistors, MT1 and MT2. When voltage $V_m$ is positive MT1 turns on and works as a closed switch while MT2 turns off and works as an open switch. And when voltage $V_m$ is negative MT1 turns off and works as an open switch while MT2 turns on and works as a closed switch. The gate voltages of MT1 and MT2 depend on the amplitude of the modulating signal $V_m$. And the drain voltage of MT1 and the source voltage of MT2 depend on the amplitude of the carrier signal $V_c$, which are very small as voltage $V_c$ is much smaller in magnitude than voltage $V_m$. The source voltage of MT1 and the drain voltage of MT2 depend on the voltage developed across the resistor R. Therefore, whenever MT1 and MT2 are on, they always work in the non-saturation region or the ohmic region as they always hold the condition of working in the ohmic region. The conditions for operation in the ohmic region for MT1 and MT2 are given below in equations (17) and (18) respectively.

For MT1

$$V_{DSn} < V_{GSn} - V_{THn}$$

For MT2

$$V_{DSn} < V_{GSn} - V_{THn}$$
\[ V_{DSP} > V_{GSP} - |V_{THp}| \]  

where

\( V_{DSn} \) is the drain to source voltage of \( M_{T1} \), \( V_{GSp} \) is the gate to source voltage of \( M_{T1} \).

\( V_{THn} \) is the threshold voltage of the \( M_{T1} \). \( V_{THn} \) for NMOS is positive,

\( V_{DSP} \) is the drain to source voltage of \( M_{T2} \), \( V_{GSp} \) is the gate to source voltage of \( M_{T2} \), and

\( V_{THp} \) is the threshold voltage of the \( M_{T2} \). \( V_{THp} \) for PMOS is negative.

The on resistances of the transistors \( M_{T1} \) and \( M_{T2} \) used as switches are denoted by \( R_{on,n} \) and \( R_{on,p} \) respectively. From [6], for the ohmic region, the resistances \( R_{on,n} \) and \( R_{on,p} \) can be expressed as

\[ R_{on,n} = \frac{1}{(W/L)_n \mu_n C_{ox,n} (V_{GSp} - V_{THn} - V_{DSn})} \]  

and

\[ R_{on,p} = \frac{1}{(W/L)_p \mu_p C_{ox,p} (V_{GSp} - V_{THp} - V_{DSP})} \]  

where

\( (W/L)_n \) is the aspect ratio of the \( M_{T1} \), \( \mu_n \) is the mobility of electron, \( C_{ox,n} \) is the gate oxide capacitance per unit area, of \( M_{T1} \), \( (W/L)_p \) is the aspect ratio of \( M_{T2} \), \( \mu_p \) is the mobility of hole, \( C_{ox,p} \) is the gate oxide capacitance per unit area, of \( M_{T2} \).

It can be seen from the above equations (19) and (20), that \( R_{on,n} \) varies with the \( V_{GSp} \) and \( V_{DSn} \), while \( R_{on,p} \) varies with the \( V_{GSp} \) and \( V_{DSP} \). But, since both of these on resistances i.e. \( R_{on,n} \) and \( R_{on,p} \) are much smaller in magnitude than the magnitude of the external resistor \( R \) therefore the effect of variations of \( R_{on,n} \) and \( R_{on,p} \) on the BPSK modulated output voltage \( V_{PSK} \) is negligible. Mathematically, it can be expressed by the following two equations written below

\[ R_{on,n} \ll R \]  

\[ R_{on,p} \ll R \]  

The BPSK modulated output voltage is given as

\[ V_{PSK} = I_{out} \times R \]  

The voltage \( V_A \) at node A is equal to the voltage \( V_{XP} \), that is

\[ V_A = V_{XP} \]  

The voltage \( V_B \) at node B is equal to the voltage \( V_{XN} \), that is

\[ V_B = V_{XN} \]  

Also, only of the transistors is on at a time i.e. either \( M_{T1} \) or \( M_{T2} \). When \( M_{T1} \) is on, then the total resistance \( R_{total,n} \) between node A and ground is equal to the sum of the on resistance \( R_{on,n} \) of the \( M_{T1} \) and the external resistance \( R \). And when the \( M_{T2} \) is on, then the total resistance \( R_{total,p} \) between node B and ground is equal to the sum of the on resistance \( R_{on,p} \) of \( M_{T2} \) and the external resistance \( R \). Mathematically \( R_{total,n} \) and \( R_{total,p} \) are given as

\[ R_{total,n} = R_{on,n} + R \]  

\[ R_{total,p} = R_{on,p} + R \]  

When only \( M_{T1} \) is on, then the output current \( I_{out} \) is

\[ I_{out} = \frac{V_A}{R_{total,n}} = \frac{V_{XP}}{R_{on,n} + R} \]  

From equations (21) and (26)

\[ R_{total,n} = R_{on,n} + R \approx R \]
Therefore, from equations (28) and (29)

\[ I_{\text{out}} = \frac{V_{Xp}}{R} \]  

(30)

Now when only \( M_{T2} \) is on, then the output current \( I_{\text{out}} \) is

\[ I_{\text{out}} = \frac{V_B}{R_{\text{total,p}}} = \frac{V_{Xn}}{R_{\text{on,p}} + R} \]  

(31)

From equations (22) and (27)

\[ R_{\text{total,p}} = R_{\text{on,p}} + R \approx R \]  

(32)

Therefore from equations (31) and (32), \( I_{\text{out}} \) is given as

\[ I_{\text{out}} = \frac{V_{Xn}}{R} \]  

(33)

Thus from the equations (30) and (33), it can be concluded that the variation in the output current \( I_{\text{out}} \) due of \( R_{\text{on,n}} \) and \( R_{\text{on,p}} \) is negligible and therefore, the effect on the output voltage \( V_{\text{PSK}} \) because of the variations in \( R_{\text{on,n}} \) and \( R_{\text{on,p}} \) is also negligible.

When \( M_{T1} \) and \( M_{T2} \) working as the switches are in off condition than the associated resistances are denoted by \( R_{\text{off,n}} \) and \( R_{\text{off,p}} \) respectively. \( R_{\text{off,n}} \) and \( R_{\text{off,p}} \) are infinite ideally as the \( M_{T1} \) and \( M_{T2} \) transistors are in non-conducting state or off state. Now when the voltage of the modulating signal \( V_m \) is positive (logic high), \( M_{T1} \) turns on and \( M_{T2} \) turns off and the currents developed at \( Xp \) and \( Zp \) terminals of DXCCII flow towards node \( A \), which then get added up at node \( A \) as no current goes in to the gate terminal of \( M_{T1} \) and then the net current flows through the transistor \( M_{T1} \) and then through the resistor \( R \) and then goes to the ground. The two currents developed at \( Xp \) and \( Zp \) terminals of DXCCII linearly depend on the voltage \( V_{Xp} \) as can be seen in equation (30). As the voltage \( V_{Xp} \) is AC in nature therefore the currents developed because of it are also AC in nature and since these two currents add up at the node \( A \) and therefore the resultant current is also AC in nature which flows through the resistor \( R \) developing an AC voltage \( V_{\text{PSK}} \) in return across it which is in phase with the carrier signal voltage \( V_c \). And when the voltage of the modulating signal \( V_m \) is negative (logic low), \( M_{T1} \) turns off and \( M_{T2} \) turns on and the currents developed at \( Xn \) and \( Zn \) terminals of DXCCII flow towards node \( B \), which then get added up at node \( B \) as no current goes in to the gate terminal of \( M_{T2} \) and then the net current flows through the \( M_{T2} \) and then through the resistor \( R \) and then goes to the ground. The two currents developed at \( Xn \) and \( Zn \) terminals of DXCCII linearly depend on the voltage \( V_{Xn} \) and it can be seen in equation (33). As the voltage \( V_{Xn} \) is AC in nature therefore the currents developed because of it are also AC in nature and since these two currents add up at the node \( A \) and therefore the resultant current is also AC in nature which flows through the resistor \( R \) developing an AC voltage \( V_{\text{PSK}} \) in return across it which is 180° out of phase with the carrier signal voltage \( V_c \).

The operation can be summarized by these two equations as mentioned below

\[ V_{\text{out}} = I_{\text{out}} \times R \equiv V_c = A_c \sin(2\pi f_c t); \quad \text{when } V_m \text{ is positive or logic high} \]

\[ V_{\text{out}} = I_{\text{out}} \times R \equiv -V_c = -A_c \sin(2\pi f_c t); \quad \text{when } V_m \text{ is negative or logic low} \]

In conclusion, the output voltage \( V_{\text{ASK}} \) of the proposed BASK modulator and the output voltage \( V_{\text{PSK}} \) of the proposed BPSK modulator can mathematically be written in the tabulated form as shown below in the Table 2.

| Modulating signal \( V_m \) | BASK output \( (V_{\text{ASK}}) \) | BPSK output \( (V_{\text{PSK}}) \) |
|-----------------------------|---------------------------------|---------------------------------|
| Logic HIGH \((1V)\)        | \( A_c \sin(2\pi f_c t) \)       | \( A_c \sin(2\pi f_c t) \)       |
| Logic LOW \((-1V)\)        | 0                               | \(-A_c \sin(2\pi f_c t) \)      |

Table 2. Summary of outputs of the proposed BASK and BPSK modulators.
5. Simulation results of the proposed BASK and BPSK modulator

The BASK & BPSK modulators are simulated with SPICE using CMOS implementation of the active block DXCCII [35] and 0.35µm CMOS technology parameters. The supply voltage for the active block DXCCII is taken as ±1.8V and the voltage $V_{bias}$ is set to 1.05V. The aspect ratios ($W/L$) of the transistors $M_{T1}$ and $M_{T2}$ used as the switches are same i.e. 30µm/0.7µm. The value of external resistor $R$ is selected as 5KΩ. The waveform of the input carrier voltage signal $V_c$ is shown in Fig. 5. The carrier signal $V_c$ is having a peak amplitude $A_c$ of 100mV and frequency $f_c$ of 20MHz. The waveform for the modulating signal $V_m$ is shown in Fig. 6. The waveforms for the ASK modulated output voltage $V_{ASK}$ and PSK modulated output voltage $V_{PSK}$ are shown above in Fig. 7 and Fig. 8 respectively.

The logic high and logic low levels of the modulating signal $V_m$ are defined as follows

$$V_m = 1V;$$  \hspace{1cm} \text{for logic high or logic 1 or bit 1}

$$V_m = -1V;$$  \hspace{1cm} \text{for logic low or logic 0 or bit 0}

\begin{figure}[h]
  \centering
  \includegraphics[width=\textwidth]{carrier_signal}
  \caption{Waveform of the carrier signal $V_c$}
\end{figure}

\begin{figure}[h]
  \centering
  \includegraphics[width=\textwidth]{modulating_signal}
  \caption{Waveform of the modulating signal $V_m$}
\end{figure}
Figure 7. ASK modulated output voltage $V_{\text{ASK}}$

Figure 8. PSK modulated output voltage $V_{\text{PSK}}$

Table 3. Comparison of the various Modulators

| Ref. no. | Active elements | No. of floating/grounded resistors | No. of capacitors | No. of MOS | BASK/ BPSK | Max. carrier frequency (Hz) | Supply voltage |
|----------|-----------------|-----------------------------------|-------------------|------------|------------|-----------------------------|----------------|
| [5]      | 1 EXCCII        | 1/0                               | 0                 | 23+1       | Both       | 20M                         | ±1.25          |
|          | 1 MOS           |                                   |                   |            |            |                             |                |
| [6]      | 1 EXCCII        | 0/3                               | 0                 | 21+2       | Both       | 20M                         | ±1.25          |
|          | 2 MOS           |                                   |                   |            |            |                             |                |
| [7]      | 2 MO-CCCCCTA    | 0/0                               | 3                 | 2×26       | ASK        | 2.11M                       | ±0.9           |
| [8]      | 1 CCCII+        | 0/1                               | 2                 | NA         | ASK        | 20.78M                      | ±1.5           |
| [9]      | 1 VCCS Memristors | 0/1                       | 1                 | NA         | Both       | 1K                          | NA             |
| [10]     | 1 DPCCII        | 0/2                               | 0                 | 18         | ASK        | 125K                        | ±0.75          |
| [11]     | 1 MO-CCCCC      | 1/2                               | 3                 | NA         | Both       | 1.5M                        | NA             |
| [12]     | 1 Digitally programmable CDTA | 0/2                       | 2                 | 67         | Both       | 34.39M                      | ±0.8           |
| [13]     | 2 MO-OTA        | 0/1                               | 3                 | NA         | Both       | NA                          | NA             |
| Proposed | 1 DXCCII, 1 MOS | 0/1                               | 0                 | 20+1       | ASK        | 20M                         | ±1.8           |
| Proposed | 1 DXCCII, 2 MOS | 0/1                               | 0                 | 20+2       | PSK        | 20M                         | ±1.8           |
6. Conclusion

Two voltage mode digital modulators have been proposed namely BASK and BPSK. BASK employs one DXCCII, one grounded resistor and one NMOS transistor while BPSK employs one DXCCII, one grounded resistor, one NMOS and one PMOS transistor. Both the above proposed circuits provide the advantage of having proper input impedances and use of grounded resistor. A comparative study table of various digital modulators available in the open literature is given in table 3. All the proposed circuits have been simulated with SPICE using 0.35µm CMOS technology parameters. The supply voltage of ±1.8V is used. Convincing results have been obtained with all the proposed circuits.

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