Etching rate of silicon nanowires with highly doped silicon during metal-assisted chemical etching

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Abstract
The fabrication of silicon nanowires (SiNWs) by metal-assisted chemical etching (MACE) has been widely studied in a variety of fields. SiNWs by high-doped silicon are potential materials to be applied in thermoelectric, lithium-ion batteries and sensors. However, existing studies on the etching characteristics of high-doped silicon are limited and misunderstandings are existing. In this study, through the comparison of three types of silicon with different concentrations, it was found that the loss of SiNWs by low-doped and medium-doped was little but the loss for high-doped silicon was significant. Contrary to existing reports, we clarify that the etching rate of high-doped silicon was the highest among them through measurements and calculations, although the observed length was the smallest. The differences between supposed generated SiNWs and measured SiNWs can be assumed as the lateral etching of high-doped silicon. In addition, the cluster morphology of high-doped silicon also suggested severe lateral etching. Therefore, the etching characteristics of high-doped silicon and the mechanism need to be re-understood to control reactions and obtain expected SiNWs.

1. Introduction
As a simple process allowing large-area fabrication, metal-assisted chemical etching to fabricate SiNWs has been widely applied in the field of solar cells [1–5], thermoelectric [6–10], biology [11–15], and sensors [16–20]. To understand the etching characteristics of silicon with different doped concentration is significant for controlling the fabrication for various applications. Studies show that compared to SiNWs by low-doped and medium-doped silicon, SiNWs by high-doped silicon tend to be difficult to form long and vertical SiNWs [21], leading to a seemingly losing motivation in related research of high-doped silicon. Yet high-doped silicon can be widely used in the fields of electrically conductive [22], optically active [22], and thermoelectric [23], owing to its high electrical conductivity. In previous studies, the etching rate of SiNWs during MACE process was generally understood by the observed length of SiNWs and the etching time [15, 21, 24]. However, we find that the actual etching rate of the SiNWs by high-doped silicon greatly differs from previous understanding, as the loss of generated SiNWs during the etching process was verified. In this work, SiNWs fabricated by MACE using silicon of low, medium, and high doping concentration (10^{15} cm^{-2}, 10^{19} cm^{-2} and 10^{20} cm^{-2}) were compared. The results show the SiNWs loss of medium-doped and low-doped silicon during etching process was little, but the SiNWs loss of high-doped silicon was severe. Due to the great loss of SiNWs by high-doped silicon, the increase in etching time is unlikely to increase the length of SiNWs like low-doped silicon, therefore the existing fabrication concept acquired from the relatively abundant experience based on low-doped silicon cannot be fully applied to high-doped silicon. Moreover, the calculation of etching rate using the remained length of SiNWs divided by etching time became inapplicable because the lost part of high-doped silicon can be even longer than the observed part. Contrary to the report in previous studies that believed the etching rate of SiNWs of high-doped silicon was smaller than medium-doped and low-doped silicon [15, 21], we verified that the etching rate of high-doped silicon was the largest among the three types of silicon. The etching characteristics of
high, medium, low-doped silicon in length and morphology clarified the dynamic changes of SiNWs during the MACE, which can result in new understanding of the fundamental mechanism of high-doped silicon. This result indicates that compared to the increase in etching time, controlling the etching conditions is crucial for fabricating expected SiNWs using high-doped silicon. The study contributes to the MACE of high-doped silicon and more application possibilities of SiNWs by high-doped silicon.

2. Experimental methods

Silicon substrates with three different resistivities were selected for the fabrication of SiNWs, comprising n-type silicon of low-doped wafer of 1–2 Ω cm (204 μm thick), medium-doped wafer of 0.0114–0.0118 Ω cm (622 μm thick), and high-doped wafer of 0.0007 Ω cm (598 μm thick) with a (100) crystal orientation. The doped concentrations are roughly 10^{15} cm^{-3}, 10^{18} cm^{-3} and 10^{20} cm^{-3}. The same experimental processes and solution under same temperature (300K) were used for the samples. Before the experiment, the silicon substrates were cut into 2*2 cm. Then the wafers were cleaned with HF for 1 min to remove the native oxide, and the substrates were immersed in a solution of 4.8 M HF and 0.015 M AgNO_3 for electroless silver plating (ESP) 1 min in order to plate silver particles. With the silver particles plated on the Si substrate, the samples were immersed in the 4.8 M HF solution and 0.15 M H_2O_2 for MACE from 1 h to 5 h respectively. After the experiment, the length of SiNWs, the thickness of sandwich-structured composites (SSCs), and the thickness of silicon substrate were measured by scanning electron microscope (SEM).

3. Result and discussion

A silicon substrate was continuously converted to SiNWs during etching progress. Figure 1 shows an example of SEM image of SiNWs/Si/SiNWs sandwich-structured composites (SSCs), which include SiNWs on both sides and silicon substrate in the middle. As the SSCs have upside-down symmetry, SiNWs on two sides have the same length. The thickness of the SSCs equal to the length of SiNWs on both sides plus the thickness of remained silicon substrate in the middle.

Table 1 shows the fabrication conditions, length of SiNWs, thickness of SSCs and supposed length of converted SiNWs. The length of SiNWs, thickness of silicon substrate and thickness of SSCs were measured by SEM. The supposed length of converted SiNWs is calculated based on the value of the initial thickness of silicon wafer substrate and the remained thickness of the silicon substrate at one side, indicating the total amount of silicon that should have been converted to SiNWs during the MACE. The loss of SiNWs is the difference value between the supposed length of converted SiNWs and the measured length of SiNWs. The results in table 1 are analyzed in figure 2.

Figure 2(a) shows the length changes of SiNWs with the etching time. The SiNWs length of all the three types of silicon increased during 1 h to 5 h respectively. For each hour, the SiNWs by middle-doped silicon was the largest, followed by low-doped silicon. Notably, the length of SiNWs by high-doped silicon in each hour was the smallest among the three types, which seems to be in contradiction with the conventional wisdom that the etching rate should increase with increasing doped concentration [21]. When the similar phenomenon was observed in previous studies, the reason was explained as vertical etching rate of high-doped silicon decreased as the silver particles spread into the solution or the top of SiNWs and the silver particles remained at the bottom decreased [15, 21]. However, this recognition towards the etching characteristics of high-doped silicon is incorrect, which will be proved and detailed explained in the following figures.

Figure 2(b) shows the thickness changes of SSCs with the etching time. According to the differences between the initial thickness of silicon substrate and the measured thickness of SSCs, the changed values imply the
Figure 2. (a) Length of measured SiNWs with different resistivity as a function of MACE time. (b) Thickness of remained SSCs with different resistivity as a function of MACE time. (c) Loss rate of SiNWs with different resistivity as a function of MACE time, using the loss of SiNWs divided by the supposed length of converted SiNWs. (d) Supposed length of converted SiNWs and measured length of SiNWs (0.0007 Ω cm) as a function of MACE time.

Table 1. Length of SiNWs, thickness of SSCs, thickness of silicon substrate, and supposed length of converted SiNWs fabricated by MACE using different resistivity of silicon wafer.

| No. | Resistivity /Ω cm | Etching time /h | Length of SiNWs /μm (One side) | Thickness of SSCs /μm | Thickness of silicon substrate /μm | Supposed length of converted SiNWs (One side) |
|-----|-------------------|----------------|---------------------------------|----------------------|-------------------------------|---------------------------------------------|
| (1) | 1–2               | 1              | 22                              | 190                  | 145                           | 29.5                                        |
| (2) | 1–2               | 2              | 38                              | 190                  | 114                           | 45                                          |
| (3) | 1–2               | 3              | 51                              | 186                  | 80                            | 62                                          |
| (4) | 1–2               | 4              | 65                              | 186                  | 52                            | 76                                          |
| (5) | 1–2               | 5              | 78                              | 181                  | 22                            | 80                                          |
| (6) | 0.0114            | 1              | 29                              | 590                  | 530                           | 46                                          |
| (7) | 0.0114            | 2              | 46                              | 590                  | 500                           | 61                                          |
| (8) | 0.0114            | 3              | 65                              | 585                  | 455                           | 83.5                                        |
| (9) | 0.0114            | 4              | 74                              | 580                  | 429                           | 86.5                                        |
| (10)| 0.0114            | 5              | 91                              | 580                  | 403                           | 109.5                                       |
| (11)| 0.0007            | 1              | 19                              | 550                  | 510                           | 44                                          |
| (12)| 0.0007            | 2              | 22                              | 497                  | 455                           | 71.5                                        |
| (13)| 0.0007            | 3              | 40                              | 487                  | 413                           | 92.5                                        |
| (14)| 0.0007            | 4              | 43                              | 464                  | 371                           | 113.5                                       |
| (15)| 0.0007            | 5              | 54                              | 460                  | 353                           | 122.5                                       |
amount of silicon that lose in the form of SiNWs. It can be seen that for low-doped and medium-doped silicon, the major changes of SSCs thickness happened during the first hour and there were almost no changes with the etching time increase afterwards. However, high-doped silicon shows a very different tendency with the above two types of silicon, as the loss of SiNWs continuously increased from 0 h to 5 h. It can be understood that at the beginning most of the silver ions are gathered at the top of SiNWs for each type of silicon, leading to the severe lateral etching \[21, 22\] and caused the loss of SiNWs. But with the etching time increase, the loss of SiNWs for low-doped and medium-doped silicon did not increase and maintained at a constant level of 14–23 μm and 23–42 μm respectively. Whereas for the high-doped silicon, the loss of SiNWs was occurring during the whole process, with a great increase from 48 μm to 138 μm. Figure 2(c) shows the specific loss rate of SiNWs which is calculated by the loss of SiNWs divided by the supposed length of converted SiNWs, indicating the length of lost SiNWs as a percentage of converted SiNWs. As we indicated above, the loss of SiNWs fabricated with low-doped and medium-doped silicon almost did not change after 1 h, therefore the loss rate is low and continuously decreased with the etching time. The fifth hour of medium-doped silicon is considered an experimental error. On the other hand, the loss rate of high-doped silicon was maintained at a high level above 50% at each hour, which means more than half the length of converted silicon nanowires have been lost in the etching process and the amount cannot be ignored. The loss of high-doped silicon is further analyzed in figure 2(d), which shows the supposed length of converted SiNWs and the measured length of SiNWs. The differences of which reflect the SiNWs loss during the etching process. When etching time was 1 h, the length of remaining SiNWs was 19 μm, but the SiNWs loss was 23 μm; when etching time was 5 h, the length of remaining SiNWs was 54.5 μm, but the SiNWs loss was up to 68.5 μm. Considerable loss of SiNWs for high-doped silicon kept occurring in the whole etching process, the length of which was more than the remained part of SiNWs for each hour.

Therefore, we clarify that the loss of SiNWs of high-doped silicon is significant and the actual etching rate of high-doped silicon is the highest among the three types of silicon (figure 3). This result suggests that the etching rate on high-doped silicon was misunderstood so far, therefore the explanation of the mechanism why the etching rate of high-doped silicon was lower than low-doped silicon was incorrect understanding. The major reason is the loss of high-doped silicon was not fully observed and was ignored in the analysis. The observed SiNWs by high-doped silicon were the shortest among the three types of silicon not because of the vertical etching rate decreases; on the contrary, the vertical etching of high-doped silicon was continuously going on and the length of generated SiNWs was the largest. However, the high-doped concentration resulted in severe lateral etching and a large amount of the generated SiNWs disappeared in the solution during the etching process.

The overall generated length of SiNWs can indicate the vertical etching of silicon, while the loss of SiNWs indicates the severe degree of lateral etching. Compared to the low generated length (table 1) and little loss of SiNWs of low-doped and medium-doped silicon (figure 2(b)), the large dopant concentration of high-doped silicon increases the crystal defects that can provide more contact sites for silver ions, resulting in a high H₂O₂ oxidation rate whether vertically or laterally. Moreover, the more defect sites on the surface of high-doped silicon can absorb more silver ions, which resulted in the formation of higher porous SiNWs \[25\]. With the
increasing loss of SiNWs, the silver particles absorbed by the high porosity of high-doped silicon would dissolve into the solution, which could further intensify the lateral etching.

Hence, the high etching rate by high-doped silicon is critical when considering the etching characteristics and controlling the fabrication process. As SiNWs fabricated by high-doped silicon has the characteristics of higher initial conductivity and higher porosity, it is potentially to be used in the energy fields like thermoelectric. Therefore, it is necessary to re-understand the etching characteristics of high-doped silicon and the mechanism to control reactions and obtain expected SiNWs. For example, by adjusting the experimental conditions to reduce the loss of SiNWs, fabrication of longer vertical SiNWs or rapid large-area preparation is potential.

In terms of morphology, the SiNWs fabricated by high-doped silicon show distinct morphological characteristics compared to the SiNWs fabricated by low-doped and medium-doped silicon. Figure 4 shows the morphology of SiNWs fabricated with silicon of the three different concentrations. When using low-doped silicon (figures 4(a)–(e)) and medium-doped silicon (figures 4(f)–(j)), the SiNWs grow vertically during the etching process from 1h to 5h. However, the SiNWs fabricated by high-doped silicon (figures 4(k)–(o)) were clustered, and the clusters even became two layers during the etching time of 3–5 h. The reason for the clustering phenomenon can be attributed to the severe lateral etching of high-doped silicon. During the etching process, some diffused silver ions in the etching solution may start to nucleate on the sidewall near certain weak defective sites after reaching a certain threshold, forming a new etching pathway along the lateral direction of the nanowires [21]. This lateral etching of high-doped silicon thus caused the loss of the top part of SiNWs and resulted in the clustering of SiNWs. In other words, the top of SiNWs is likely to form the clusters then dissolve gradually, and this process might have repeated since the thickness of the SSCs was continuously decreasing. Therefore, in order to fabricate longer SiNWs, the reduction of lateral etching needs to be considered by controlling the etching conditions, which can also be reflected in the reduction of the thickness of SSCs.

4. Conclusion

This study compared the etching characteristics of SiNWs fabricated with low-doped, medium-doped, and high-doped concentrations of silicon by MACE. Little loss of SiNWs during the etching process was found in low-doped and medium-doped silicon, but the loss of SiNWs for high-doped silicon was significant. Previous studies believed the etching rate for high-doped silicon was slower than low-doped silicon; however, this study proved that the etching rate of high-doped silicon was the largest among the three doped concentrations of silicon although the observed length of high-doped silicon was the smallest. This is because a large amount of SiNWs loss exists during the etching process when using high-doped silicon to fabricate the SiNWs due to the severe lateral etching. In terms of morphology, the clusters and multilayer structures of SiNWs by high-doped silicon were observed due to the lateral etching. Therefore, this study pointed out the incorrect understanding and clarified the etching rate of high-doped silicon. It is necessary to include the loss of SiNWs by high-doped silicon when examining the actual etching rate or seeking proper control for experimental conditions based on the etching characteristics.
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Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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