A radiation detector design mitigating problems related to sawed edges

A. Aurola, V. Marochkin and T. Tuuva

Pixpolar, Tekniikantie 1, 02150, Finland
Lappeenranta University of Technology, P.O. Box 20, 53851, Finland
E-mail: Vladislav.Marochkin@pixpolar.com

ABSTRACT: In pixelated silicon radiation detectors that are utilized for the detection of UV, visible, and in particular Near Infra-Red (NIR) light it is desirable to utilize a relatively thick fully depleted Back-Side Illuminated (BSI) detector design providing 100% Fill Factor (FF), low Cross-Talk (CT), and high Quantum Efficiency (QE).

The optimal thickness of such detectors is typically less than 300 µm and above 40 µm and thus it is more or less mandatory to thin the detector wafer from the backside after the front side of the detector has been processed and before a conductive layer is formed on the backside. A TAIKO thinning process is optimal for such a thickness range since neither a support substrate on the front side nor lithographic steps on the backside are required. The conductive backside layer should, however, be homogenous throughout the wafer and it should be biased from the front side of the detector.

In order to provide good QE for blue and UV light the conductive backside layer should be of opposite doping type than the substrate. The problem with a homogeneous backside layer being of opposite doping type than the substrate is that a lot of leakage current is typically generated at the sawed chip edges, which may increase the dark noise and the power consumption. These problems are substantially mitigated with a proposed detector edge arrangement which 2D simulation results are presented in this paper.

KEYWORDS: Solid state detectors; X-ray detectors; Photon detectors for UV, visible and IR photons (solid-state) (PIN diodes, APDs, Si-PMTs, G-APDs, CCDs, EBCCDs, EMCCDs etc); Detector modelling and simulations II (electric fields, charge transport, multiplication and induction, pulse formation, electron emission, etc)

1Corresponding author.
1 Introduction

In pixelated silicon radiation detectors that are utilized for the detection of UV, visible, and Near Infra-Red (NIR) light it is desirable to utilize a relatively thick fully depleted Back-Side Illuminated (BSI) detector design. The benefit of the BSI configuration is that structures on the front side such as conductors do not absorb light thus enabling 100% Fill Factor (FF). The advantages of the fully depleted configuration are considerably reduced Cross-Talk (CT) due to lack of diffusion and improved Quantum Efficiency (QE) due to lack of recombination.

The thicker the fully depleted detector the better is the QE for NIR light. However, the thicker the fully depleted detector the more dark current is generated in the depleted bulk (which can be, however, mitigated by cooling), the bigger bias at a conductive backside layer is required to fully deplete the bulk, and the bigger is the CT particularly at the boundary of the pixel matrix. Thus there is an optimal detector thickness depending mainly on the optics, the magnitude of the bias on the conductive backside layer, and the pixel size.

In case the detectors should be thinner than 300 µm thick it is more or less mandatory to thin the detector wafer from the backside after the front side of the detector has been processed and before the conductive layer is formed on the backside. One option is to bond the front side of the detector wafer to a support wafer. The problem is, however, that it is not trivial to reach the contact pads located on the front side of the detector wafer especially if the detector is thicker than 40 µm. This problem can be avoided in TAIKO thinning process since no support wafer is required but the detector thickness must be at least 40 µm. The TAIKO process is a wafer back grinding method developed by DISCO. The difference to conventional back grinding is that the TAIKO process leaves an edge (approximately 3 mm) on the outer most circumference of the wafer and thin grinds only the inner circumference. The TAIKO process has, however, the problem that lithographic steps cannot be performed on the backside of the detector wafer. This means that the conductive backside layer must be homogenous throughout the wafer and that the contact to the conducting backside layer needs to be placed on the front side of the detector.

In order to provide good QE for blue and UV light the conductive backside layer should be as thin as possible and it should be of opposite doping type than the substrate (an inversion layer
Figure 1. A schematic drawing of the proposed detector edge structure (the potential values correspond to simulations). The floating neutral area next to the edge minimizes the depleted edge area. The outermost $p^+$ ring (at $V_1$) is used for punch-through biasing of the backside $p^+$ layer and for depleting the detector bulk. The $n^+$ ring at $V_2$ is used for the collection of edge-generated electrons in particular. The $p^+$ ring at $V_3$ is used to isolate the active detector area (at $V_4$) from the $n^+$ ring at $V_2$ and from edge generated electrons.

is generally not an option due to the relatively thick fully depleted substrate). Beside the use of TAIKO process it is hereby assumed that the detector chips are separated from the wafer by sawing which is a standard procedure in chip manufacturing. The problem with afore described arrangement is that it is difficult to bias the conductive backside layer from the front side. Another problem is typically that a lot of leakage current is generated at the sawed chip edge, which may increase the dark noise and the power consumption.

In this paper we present 2D simulation results of a thick fully depleted BSI detector chip arrangement that is obtained with the TAIKO thinning procedure, that has a conductive backside layer on an oppositely doped wafer and that has less problems related to the sawed edges. The key aspect of the detector edge design is to maximise the neutral area on the chip edges.

2 Concept

A cross-section of the simulated edge arrangement of the thinned detector is presented in figure 1 wherein the detector arrangement surrounded by the proposed edge area corresponds to a standard diode detector. The front view of the detector of figure 1 is presented in figure 2. The processing of a thinned detector structure that is not bonded to a support wafer necessitates that no lithographic steps can be performed after thinning. Therefore a maskless $p^+$ implant is deployed on the backside of the detector’s $n$ type high resistivity substrate. The combination of oppositely doped substrate and conductive backside layer is utilised in order to achieve high QE for blue light. This complicates, however, the design since the biasing of the backside layer needs to be performed from the front side and one cannot simply bias the backside through a neutral substrate of opposite doping type (if the backside layer and the substrate were of the same doping type one could bias the back-
side layer through a neutral substrate). A preferable way to achieve the biasing of the conductive backside layer is to use punch-through biasing as explained in [1].

The punch-through biasing is achieved with the outermost p⁺ ring (at potential $V_1$) — when a large enough reverse bias is applied to this p⁺ ring the depletion region in the n⁻ bulk around the p⁺ ring will extend to the backside p⁺ layer. At even larger reverse bias values the potential of the p⁺ backside layer will follow the p⁺ layer resulting in punch-through biasing of the p⁺ backside layer. When the potential of the p⁺ backside layer starts to follow the potential of the outermost p⁺ ring the junction between the p⁺ backside layer and the n⁻ substrate starts to be reverse biased everywhere else than beneath the outermost p⁺ ring. Consequently a sufficiently large reverse bias applied to afore said p⁺ ring will deplete the whole bulk between the p⁺ backside layer and the large area n⁺ doping (at potential $V_4$) as already explained in [1].

Since there is no biased contact at the edge of the detector a floating neutral area will be formed next to the edge as depicted in figure 1. The potential of this neutral area will follow closely the potential of the p⁺ backside layer [1]. The benefit of the neutral area next to the sawed edge is that it minimises the depleted area at the sawed edge and thereby the edge generated leakage current.

The excess electrons (including edge generated electrons) collected by the neutral area flow horizontally in a channel located in the proximity of the backside p⁺ layer and beneath the outermost p⁺ ring after which these electrons flow through the substrate and are collected by an n⁺ ring (at potential $V_2$) as is depicted by the red arrow in figure 1. Excess holes collected by the p⁺ backside layer flow vertically to the outermost p⁺ ring as is depicted by the vertical grey arrow. An additional p⁺ ring (at potential $V_3$) prevents excess electrons originating from the edge area from entering into the large area n⁺ doping collecting the radiation-induced electrons.

It is important to note that in reality the substrate doping will differ at least slightly at different parts of the detector chip. The location where the excess electrons from the neutral area flow to the n⁺ ring (at $V_2$) corresponds to the location wherein the substrate has the highest doping underneath the outermost p⁺ ring. The location of the punch-through biasing of the backside layer corresponds, on the other hand, to the location having the smallest substrate doping underneath the outermost p⁺

---

Figure 2. Top view of the detector presented in figure 1 comprising the proposed edge structure.
Electrostatic potential distribution in the simulated detector edge structure. The border of the neutral area situated next to the detector edge is depicted by a white line. The detector is fully depleted beneath the anode.

These separate locations have been also drawn to figure 2. The higher the doping fluctuations underneath the outermost p⁺ ring the larger the potential difference between the backside p⁺ layer and the neutral area located next to the edge and thus the larger the edge generated leakage current. An efficient way to mitigate this problem is to use neutron trans-mutated Silicon (or Germanium) wafers.

3 TCAD simulation study

In this section 2D simulation results are presented and discussed. The simulated device comprises an n⁻ type 100 µm thick silicon substrate having a resistivity of 2 kΩ cm. The effect of the fixed charge at the Si/SiO₂ interface is taken into account by setting the positive oxide charge concentration to 1e11 cm⁻³. The bias voltages at $V_1 = -20$ V, $V_2 = +15$ V, $V_3 = 0$ V, and $V_4 = +15$ V presented in figure 1 have been used in the 2D simulations corresponding to figures 3–7. The value of around 1 V at the backside p⁺ layer and the neutral area in figure 1 corresponds to the 2D simulation results. One should note, however, that in reality the potential at the backside p⁺ layer and at the neutral area would differ more as it is explained in conjunction with figure 2.

The electrostatic potential distribution of the simulated structure is presented in figure 3. The border of the neutral area situated next to the detector edge is depicted by a white line — elsewhere the detector is fully depleted excluding the n⁺ and p⁺ areas. It can be deduced from figure 3 that the proposed detector edge structure functions as desired; there is a neutral area next to the detector edge, the depleted edge area is minimized, and beneath the anode the detector is fully depleted.

The electron current distribution in the simulated detector edge structure is presented in figure 4. Electrons generated at the depleted edge and flowing from the neutral area through the depleted bulk are represented by the yellow arc located beneath the outermost p⁺ ring and extend-
Figure 4. Electron current distribution in the simulated detector edge structure. Electrons flowing from the neutral edge area through the depleted bulk are represented by the yellow arc located beneath the $p^+$ ring and reaching to the $n^+$ ring. No edge generated electrons reach the $n^+$ doped anode.

Figure 5. Electron density distribution in the simulated detector edge structure. The neutral area is next to the detector edge and the flow of electrons from the neutral area to the $n^+$ ring is represented by the arc located beneath the larger left hand side $p^+$ ring.

The electron density distribution in the simulated structure is presented in figure 5. The neutral area is next to the detector edge and the flow of electrons from the neutral area to the $n^+$ ring (at $V_2$) can be easily identified. Thus one can deduce that the detector edge structure works as desired.

The hole current distribution in the simulated structure is presented in figure 6. A large reverse bias potential at the left hand side outermost $p^+$ ring provides punch-through biasing of the backside $p^+$ layer depleting thereby also the bulk. The punch-through hole current is represented by the
Figure 6. Hole current distribution in the simulated detector edge structure. A large reverse bias potential at the left hand side outermost p$^+$ ring provides punch-through biasing of the p$^+$ backside layer depleting thereby also the bulk. The punch-through hole current is represented by the yellow column beneath the left hand side p$^+$ ring.

Figure 7. Hole density distribution in the simulated edge structure. The punch-trough hole current from the p$^+$ backside layer to the left hand side p$^+$ ring is represented by the green column beneath the left hand side p$^+$ ring.

yellow column beneath the left hand side p$^+$ ring. In other words, it can be clearly seen that the punch through biasing effect is established as intended.

The hole density distribution in the simulated structure is presented in figure 7. The punch-through hole current from the p$^+$ backside layer to the left hand side p$^+$ ring is represented by the green column beneath the left hand side p$^+$ ring. This feature manifests also that the detector edge structure is working as designed.
Figure 8. A top view of a pixelated detector comprising the suggested edge structure.

Figure 9. A cross-section of the edge of the pixelated detector shown in figure 8. The detector comprises the proposed edge structure.

4 Examples of other detectors incorporating the proposed edge structure

The proposed edge arrangement can be used with various types of radiation detectors having a homogeneous backside conductive layer of opposite doping type than the substrate or incorporating an inversion layer on the backside. One example is a pixelated detector which top view is shown in figure 8. A cross-section of the same pixelated detector is shown in figure 9. In this structure there is on the backside a negatively charged insulator layer [2] (formed e.g. of Hafnium oxide) providing an inversion layer of holes underneath the interface. In order to insure that the inversion layer is
Figure 10. A top view of an SDD comprising the proposed edge structure.

Figure 11. A cross-section view of a SDD comprising the proposed detector edge structure. The electrodes of the detector are biased such that the semiconductor body below the SDD rings is completely depleted and that a necessary horizontal potential gradient is created transporting radiation induced electrons underneath the SDD rings towards the anode.

electrons generated beneath the SDD rings are collected by the SDD structure’s n⁺ and p⁺ rings meaning that the SDD of figure 11 does not suffer from interface generated dark noise. The proposed detector edge arrangement enables the biasing of the backside.
p\textsuperscript{+} layer, minimises the amount of edge generated leakage current, and prevents edge generated electrons from entering into the active SDD area, i.e., the SDD does not suffer from edge generated dark noise.

5 Conclusions

The proposed detector edge structure enables thinned detectors with good QE for blue and NIR light, low CT, low dark noise, simple manufacturing without the need for a support wafer or back-side processing, as well as low edge generated leakage current. In order to maximise the benefits of the proposed detector edge structure neutron trans-mutated Silicon (or Germanium) wafers should be used.

References

[1] J. Kemmer and G. Lutz, Large-area, low capacitance semiconductor arrangement, U.S. patent no. 4837607 (1989).
[2] A. Aurola and J. Kallipuska, Puolijohdelaite, Finnish patent application no. 20050502 (2006).