In-Memory Computing using Memristor Arrays with Ultrathin 2D PdSeO$_x$/PdSe$_2$ Heterostructure

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1. Introduction

Traditional computing systems are designed based on von Neumann architecture, which relies on the physical separation of storage and computation. This inevitably requires the data to be shuttled back and forth between the memory and processor units frequently, which impose a limitation of speed in modern computers, known as the “memory wall.”[1] More intriguingly, a significant amount of energy is wasted in transferring the data between the two subsystems. To push the envelope for speed and energy efficiency, a radically different computing paradigm that allows in situ computation within the memory, or in-memory computing (IMC), is revolutionary to address the issues associated with abundant data movement.[2,3] In particular, IMC based on analog memristors holds promise to provide a low latency and energy-efficient approach to implement data-centric applications such as image processing by means of neural network training.[3,4] Thus far, the development of convolutional neural network (CNN), an important model for image recognition, has been experimented using memristor devices, which are plagued with fundamental scientific issues related to interdevice variability, nonlinearity, and sneak path current.[5–7] Such a two-terminal memristor is typically integrated with metal oxide as a switching medium, which relies on the formation and rupture of filaments in the amorphous medium for resistive switching (RS).[5,6,8–12] However, the stochasticity of the ions’ movement is difficult to control and thus results in poor spatial and temporal variations in the RS performance.[11–15] The variation has a significant influence on the computing accuracy loss, as most reported high computing accuracies were only realized with small cycle-to-cycle variation.[7,13,16] Compared with single-layered oxide, switching medium made of double-layered oxide offers better...
control of the stochastic filament formation.\textsuperscript{[9,17–22]} However, such double-layered structure usually requires two different oxide materials to be deposited via multistep processing, such as physical sputtering and atomic layer deposition (ALD) at the expense of a thick RS layer, low on/off ratio, and/or large forming voltage.\textsuperscript{[9,20–23]} By far, double-layered RS medium based on oxides has been limited to a thickness above 6 nm, placing a constraint on its scalability limit for further performance enhancement.\textsuperscript{[23]} New materials and device concepts are therefore desired to circumvent the switching variability issue and push the scalability limit.

2D materials (2DMs) with an atomically thin body and unique physical/electronic/optical/mechanical properties have received tremendous interest as emerging materials to realize highly scalable memristive devices and enable multifunctional neuromorphic computing platforms.\textsuperscript{[24–27]} Furthermore, the inherent ability to form intrinsic native oxide renders it promising to achieve an ultrathin heterostructure made of oxide(s) on 2DM.\textsuperscript{[28–31]} So far, the reported oxide/2DM-based memristors were primarily fabricated by introducing a layer of binary oxide (e.g., ZrO\textsubscript{2} and ZnO) on spin-coated or sputtered polycrystalline 2DM film, with a thick switching medium of up to 220 nm.\textsuperscript{[30–33]} Furthermore, the absence of dangling bonds on 2DM further hinders the deposition of ultrathin oxides, thereby imposing a scalability bottleneck.\textsuperscript{[28,34]}

Among the semiconducting transition metal dichalcogenides (TMDs), palladium selenide (PdSe\textsubscript{2}) with an uncommon pentagonal structure has attracted tremendous attention recently due to its extraordinary high carrier mobility, large bandgap tunability, and high photosensitivity, which are desirable for electronic and photoelectronic applications.\textsuperscript{[35,36]} The low symmetric pentagonal structure renders it sensitive to defects. It was reported that Se vacancy at the surface of PdSe\textsubscript{2} has a low diffusion barrier and can be manipulated by scanning tunneling microscope (STM).\textsuperscript{[37,38]} Moreover, by leveraging on the vacancy-induced phase transition, we have demonstrated heterophase grain boundary-based memristors showing excellent resistive uniformity and synaptic plasticity.\textsuperscript{[27]} Other defect engineering-related applications were also reported, such as modulators and nociceptors.\textsuperscript{[19–41]} Furthermore, PdSe\textsubscript{2} has excellent air stability and can be oxidized by layer under oxygen plasma,\textsuperscript{[35,42]} making it promising to construct ultrathin bilayer 2D/oxide heterostructure through a controllable oxidation process to overcome the scalability bottleneck. These preliminary physical characteristics and prototype devices manifest the potential of PdSe\textsubscript{2} for realizing high-performance neuromorphic devices.

Here, we demonstrate an analog memristor crossbar array based on ultrathin 2D PdSeO\textsubscript{x}/PdSe\textsubscript{2} heterostructure switching medium for enabling the implementation of a neural network hardware accelerator. This is realized by means of a controllable low-temperature ultraviolet (UV)–ozone treatment, in which transition metal oxides are formed via in situ oxidation of the PdSe\textsubscript{2} nanosheet, leading to an ultrathin PdSeO\textsubscript{x}/PdSe\textsubscript{2} heterostructure with a thickness of ≈1 nm in each layer. More intriguingly, density functional theory (DFT) calculations and kinetic Monte Carlo (kMC) simulations show that the ions’ transport properties are distinctly different between the two layers, which can serve to confine the formation of filaments, thus resulting in minimal performance variations. Notably, low device variability values of 4.8% and −3.6% are achieved for set and reset voltages, respectively. Moreover, sub-pJ switching energy is obtained in the PdSeO\textsubscript{x}/PdSe\textsubscript{2} memristor, showing promise for enabling low-power programming of multiple analog states. Moreover, the high linearity and symmetric analog weight update coupled with tuneable conductance states result in image recognition with high accuracy. Leveraging on this crossbar array architecture, various kernels that are common to neural network training are implemented for multiple image-processing tasks, manifesting the potential of this new analog memory concept for the development of non-von Neumann hardware accelerator.

2. Results and Discussion

2.1. Uniform Resistive Switching in Memristors with Ultrathin Heterostructure

PdSe\textsubscript{2} is a rarely explored group-X 2D TMD with an uncommon puckered pentagonal structure,\textsuperscript{[35]} as shown in Figure S1 (Supporting Information). The mechanically exfoliated few-layer PdSe\textsubscript{2} nanosheet is used as the starting material for the fabrication of vertical two-terminal memristors. By means of UV–ozone treatment (100 °C, 15 min), we transform the pristine PdSe\textsubscript{2} into a heterostructure by oxidizing the surface to form transition metal oxide, i.e., PdSeO\textsubscript{x}, as shown in Figure 1a,b. This method allows the PdSeO\textsubscript{x}/PdSe\textsubscript{2} heterostructure to be aggressively scaled down to a thickness of 1 nm each, as verified by the cross-sectional transmission electron microscopy (TEM) image. It is worth noting that the treatment not only forms an amorphous PdSeO\textsubscript{x} layer, but also decorates defects and results in an underlying distorted PdSe\textsubscript{2} layer, as depicted in Figure 1c. Such a unique heterostructure is approaching the scaling limit for forming ultrathin oxide (≈1 nm) on TMD, which is, by far, not realizable using standard ALD due to the absence of dangling bonds needed for growth nucleation.\textsuperscript{[28,34]}

When the PdSeO\textsubscript{x}/PdSe\textsubscript{2} heterostructure is integrated as a switching medium, the memristor exhibits reproducible bipolar nonvolatile RS behavior with remarkable uniformity, achieving coefficients of variation (CVs) of 4.8% and −3.6% for set and reset voltages, respectively (Figure 1d,e). Notably, such low variability cannot be achieved when shortening (10 min) or increasing (40 min) the ozone treatment time, as shown in Figure 1f. It is found that a short ozone treatment time would result in defective crystalline PdSe\textsubscript{2}, and a long treatment time would lead to a complete amorphous structure. Moreover, both high-resistance state (HRS) and low-resistance state (LRS) are exhibiting good cycle-to-cycle or temporal uniformity (Figure S2, Supporting Information). Notably, apart from low variability, the operating voltage and on/off ratio are demonstrating good cyclical and environment endurance, in which the RS parameters are retained over 700 switching cycles and after 6 months of storage under ambient condition (Figure IF, Figures S3 and S4, Supporting Information). In addition, the operating voltage also experiences good spatial uniformity between devices (see Figure S5 in the Supporting Information) down to a dimension...
of 100 × 100 nm² (Figure S6, Supporting Information). A performance benchmarking (Figure S7 and Table S1, Supporting Information) shows that the low variation in a memristor with PdSeO\textsubscript{x}/PdSe\textsubscript{2} heterostructure is superior to other memristors with switching medium made of 2DM, oxide/oxide, 2DM/oxide, and 2DM/2DM hybrid structures. Furthermore, the PdSeO\textsubscript{x}/PdSe\textsubscript{2} heterostructure has been the thinnest among other resistive switching media based on bilayer heterostructure (Table S1, Supporting Information), which possesses a narrow variation of operating voltages as compared to other memristors in the sub 1 V regime (Figure 1g). The remarkable RS uniformity and stability over time and/or environment are critical for the implementation of neuromorphic hardware accelerator with high accuracy.

Additionally, more than 28 discrete LRS and 9 discrete HRS with small fluctuation are obtained by using different compliance currents (CCs) and reset voltages, respectively (Figure 1h; Figure S8a, Supporting Information). Concurrently, the memristor also exhibits a superior retention performance of longer than 24 h without obvious degradation (Figure S8b, Supporting Information). The achievement of multiple resistance states with good retention is a key performance metric for building artificial neural networks (ANNs) with multistates/weights for various applications.
2.2. Structure Evolution under Ozone Treatment

To understand the mechanism responsible for the uniform RS behavior in memristors with an ultrathin heterostructure, a high-resolution TEM (HR-TEM) is first employed to study the structural evolution as a function of ozone-treatment time and the thickness of PdSe₂ nanosheet (the temperature is set to 100 °C). The exfoliated PdSe₂ nanosheet shows clear lattice fringes without obvious defects (Figure 2a,e), in which the lattice spacings of 0.387, 0.286, and 0.291 nm are corresponding to (002), (200), and (020) crystal planes of orthorhombic PdSe₂, respectively. Meanwhile, the selected-area electron diffraction (SAED) reveals two principal planes (020) and (200) (inset image in Figure 2e), confirming the orthorhombic structure.

Figure 2. Structure evolution under ozone treatment. a–d) Cross-sectional HR-TEM images of PdSe₂ nanosheet treated with different times: a) pristine, b) 10 min, c) 15 min, and d) 40 min. e–h) Their corresponding top view HR-TEM and SAED images: e) pristine, f) 10 min, g) 15 min, and h) 40 min. The inset images are the corresponding SAED images. The temperature is fixed at 100 °C. The scale bars of HR-TEM images in (a)–(h) are 5 nm and those for the SAED images in (e)–(h) are 10 nm. i) XPS spectra of Pd 3d and j) Se 3d of pristine and ozone-treated PdSe₂ nanosheet with different ozone treatment times.
and the fine single-crystal feature. It was reported that both Se vacancies ($V_{\text{Se}}$) and Pd vacancies ($V_{\text{Pd}}$) exist in few-layer PdSe$_2$ based on the STM results.[37,38] Notably, no obvious defects were observed in our HR-TEM images, which may be attributed to the negligible defect density and different characterization methods. However, when subjected to 10 min ozone treatment, the PdSe$_2$ nanosheet experiences slight lattice disorders as evidenced by the symmetric SAED spots, revealing a sparsely defective single-crystalline PdSe$_2$ structure (Figure 2b,f). When ozone treatment is extended to 15 min, a bilayer heterostructure is formed with an amorphous transition metal oxide overlying the defective PdSe$_2$, as shown in Figure 2c. This can be evident from the weaker diffraction points and diffused rings in the SAED spectrum, as well as the disordered lattice fringes observed in the top view HR-TEM images (Figure 2g). The appearance of amorphous structure and diffused rings indicates a more severely damaged crystal structure as compared to that of a 10 min treatment. When the time is extended to 40 min, the PdSe$_2$ nanosheet is completely transformed into an amorphous structure without distinct lattice fringes and SAED spots (Figure 2d,h). In addition, the effect of PdSe$_2$ thickness on the structure evolution under ozone treatment is also investigated, as shown in Figure S9 (Supporting Information). A similar phenomenon is observed, in which thick nanosheet (≈3.8 nm) retains its single-crystalline structure with some defects (Figure S9a, Supporting Information), while the thin one (≈1.3 nm) completely transforms into amorphous structure (Figure S9c, Supporting Information). The composition of the ozone-treated samples with different structures is characterized by energy-dispersive X-ray spectroscopy (EDS), as shown in Figure S10 (Supporting Information). All these samples show the existence of O, and the ratio is qualitatively increasing from defective PdSe$_2$ to PdSeO$_x$/PdSe$_2$, followed by amorphous PdSeO$_x$.

To further verify the structure evolution, X-ray photoelectron spectroscopy (XPS) is used to confirm the observation (Figure 2i,j). Compared to the pristine PdSe$_2$, the peaks of Pd 3d$_{3/2}$ (=336.9 eV), Pd 3d$_{5/2}$ (=342.2 eV), Se 3d$_{3/2}$ (=54.9 eV), and Se 3d$_{5/2}$ (=55.8 eV) show no obvious change after 10 min treatment, but apparent shift toward lower binding energies is observed when the time is extended to 15 and 40 min.[44] The variations of the abovementioned peaks are summarized in Figure S11a (Supporting Information), in which an evident change in binding energy corresponds to a remarkable change of the crystal structure, i.e., the appearance of an amorphous layer. This is evidenced by the new distinct peaks at higher binding energies (orange lines in Figure 2i,j) in all ozone-treated samples, indicating the formation of PdO$_x$ and SeO$_x$ (i.e., PdSeO$_x$).[42,44] With prolonged treatment time, the areas under the XPS peaks that are associated with these oxides are shown to increase (Figure S11b, Supporting Information). This can also be confirmed by the diminishing Raman peaks, as shown in Figure S11c (Supporting Information).[45] In a nutshell, through increasing ozone treatment time, the PdSe$_2$ nanosheet is postulated to experience structure evolution from pristine PdSe$_2$ with single crystallinity to defective PdSe$_2$, followed by a transition to PdSeO$_x$/PdSe$_2$ heterostructure, and finally completely transformed into PdSeO$_x$ amorphous layer.

### 2.3. Resistive Switching Mechanism

First, the relationship between the structure evolution and RS behavior is plotted in Figure 3a to investigate the uniform RS mechanism in PdSeO$_x$/PdSe$_2$ heterostructure memristors. As shown in Figure 3a-1, there is no RS phenomenon when pristine single-crystalline PdSe$_2$ nanosheet is used as a switching medium. After being treated for 10 min, the memristor with defective single-crystalline PdSe$_2$ shows RS behavior but with a small on/off ratio (≈10, Figure 3a-II). The most uniform RS behavior can be demonstrated in a memristor with heterostructure, which achieves the lowest set and reset voltage variations of 4.8% and –3.6%, respectively, as well as much higher on/off ratio (≈300, Figure 3a-III). This is in contrast to other oxide/oxide memristors, where uniformity is improved but at the expense of a significantly reduced on/off ratio.[20,21] Huge randomness similar to the traditional metal-oxide-based memristor is found when amorphous PdSeO$_x$ is used as the switching medium (24% and –15.5% for set and reset voltage variations, respectively), as shown in Figure 3a-IV.[8–10] The impact of ozone treatment time on the switching behavior is further investigated, as shown in Figure S12 (Supporting Information). It is found that the variations in set and reset voltages are increased with longer treatment after the PdSeO$_x$/PdSe$_2$ heterostructure is formed, showing a strong dependence on the treatment duration. However, other pertinent switching parameters are experiencing less dependence on the treatment time, which indicates that the bilayer heterostructure is effective in improving RS uniformity. A similar relationship between the RS behavior and the crystal structure is also found in memristors with different thicknesses (Figure S13, Supporting Information). Moreover, uniform RS behavior can also be obtained by reducing the temperature to 60 °C with optimal time (Figure S14, Supporting Information). This leads to a high on/off ratio in memristors with PdSeO$_x$/PdSe$_2$ heterostructure as compared to single amorphous PdSeO$_x$ or defective crystalline PdSe$_2$, indicating the importance of heterostructure in achieving low variability.

It is noted that the LRS shows inconspicuous change whereas the HRS decreases slightly with increasing device size (Figure S15, Supporting Information); thus, the pure electronic or interface-dominant mechanism can be excluded in the ozone-treated memristor.[46,67] Conductive atomic force microscopy (CAFM) is employed to further unveil the RS mechanism of the ozone-treated memristor (Figure S16, Supporting Information). CAFM images in Figure S16a–d (Supporting Information) reveal that the amorphous PdSeO$_x$ contains a much higher defect density than that in the defective crystalline PdSe$_2$, unraveling the abundant percolation channels. By increasing voltage stress, conductive filaments are formed as evidenced by the higher currents measured across the active layer (Figure S16f, Supporting Information). When active Ti is replaced by inert platinum (Pt) as the top electrode (Figure S17, Supporting Information), no RS behavior is observed, suggesting that the formation of conductive filaments is attributed to the migration of Ti ions (i.e., electrochemical metallization mechanism, ECM). This can be further confirmed by EDS and electron energy loss spectroscopy (EELS), in which obvious Ti penetration into the switching layer is observed when the
memristor is switched on (Figures S18 and S19, Supporting Information).

We observe that the Ti$^{x+}$ transport is influenced by the distinct defect densities between the defective PdSe$_2$ and amorphous PdSeO$_x$. DFT calculations are performed to unveil the Ti$^{x+}$ transport property in the ozone-oxidized PdSe$_2$. In perfect PdSe$_2$, a large Ti$^{x+}$ diffusion barrier across the layer ($H_1$: 1.5875 eV, across the layer) and along the interlayer spacing ($L_1$: 1.3414 eV, through the interlayer spacing) are presented, as illustrated in Figure S20a,e (Supporting Information).
Moreover, when the PdSe₂ presents point defects (Pd and Se vacancies), the diffusion barrier will be lower but remains relatively high (0.9746 and 0.8735 eV for H₂ and L₂, respectively), as shown in Figure S20b,e (Supporting Information). Such high diffusion barriers are not feasible to result in RS behavior, which is consistent with our experimental result. Defect cluster with one Pd vacancy and two Se vacancies would be created during ozone treatment, leading to a significant diffusion barrier (0.007 eV for H₃ and 0.9657 eV for L₃), as shown in Figure S20c,e (Supporting Information). This makes the diffusion of Ti⁺⁺ more favorable through the defect channels. It is reasonable and postulate that increasing defects and thus diffusion channels would result in a higher ion transport rate. Therefore, the amorphous structure with abundant diffusion channels has higher ion mobility than that in the defective crystalline PdSe₂ with limited diffusion channels, as illustrated in Figure S20f (Supporting Information).

This can be further verified by kMC simulation, as shown in Figure 3b–g and Figure S21 (Supporting Information). It is found that the diffusion time is markedly reduced for Ti⁺⁺ diffusing through the defective PdSe₂, PdSeOₓ/PdSe₂, and amorphous PdSeOₓ (Figure 3b–d), in which Ti⁺⁺ shows the highest ion transport rate through the amorphous structure. Despite using different sets of random numbers, the Ti⁺⁺ diffuses toward the bottom layer along a similar path in the defective PdSe₂ and PdSeOₓ/PdSe₂, showing a confined diffusion path (see Figure 3e,f). However, when the random number varies, the diffusion pathway will change in the amorphous PdSeOₓ (Figure 3g), which results in uncontrollable ion transport and thus a random RS behavior. Compared to the other two structures, there are limited defects/diffusion channels in the defective PdSe₂, especially in the third and fourth layers; thus, the ion diffusion path is constricted. Nevertheless, it largely retains the property of pristine single-crystalline PdSe₂ with low resistance in HRS (>10⁶ Ω), causing an on/off ratio of lower than 10. This would inevitably limit the number of distinctive conductive states needed to perform efficient neural network training. By introducing an amorphous oxide layer PdSe₂ to form a PdSeOₓ/PdSe₂ heterostructure, the HRS can be significantly increased to achieve a higher on/off ratio (Figure 3a). Moreover, there are abundant transport paths in the overlapping amorphous layer for Ti⁺⁺ migration, which are confined in the underlying defective crystalline layer. This implies that the PdSeOₓ/PdSe₂ heterostructure is capable of confining the ion transport paths and leads to an enhanced switching uniformity and a high on-off ratio.

2.4. Synaptic Plasticity and Image-Recognition Simulation

Synaptic plasticity including short-term plasticity (STPL) and long-term plasticity (LTPL) forms the foundation of bioinspired neuromorphic computing.[48] Long-term potentiation (LTP) and long-term depression (LTD) are two essentials LTPL, which can be mimicked by the PdSeOₓ/PdSe₂ memristor. The profiles of LTD and LTP can be flexibly tuned by applying different pulse schemes, as shown in Figure 4a–c. When applying 200 pulses with a width of 0.12 ms, the postsynaptic current increases progressively with positive pulses but decreases swiftly with negative pulses, resulting in asymmetric LTP and LTD (Figure 4a). However, the symmetry and linearity of the analog conductance switching can be improved by reducing the pulse width to 0.05 ms (Figure 4b). Further improvement can be achieved by using nonidentical pulse scheme, in which the LTP and LTD processes show near-ideal linearity and symmetry (Figure 4c). The linearity and symmetry of LTP and LTD under different pulse schemes are further quantified using a device behavioral model[49] (Figure 4d). LTP and LTD with incremental modulation of device conductance, and reasonable linearity and symmetry, are the basic requirements for the implementation of ANN. Other synaptic plasticities including paired-pulse facilitation (PPF), spike-timing-dependent plasticity (STDP), and spike-amplitude-dependent-plasticity (SADP) also can be emulated by the PdSeOₓ/PdSe₂ memristor, as shown in Figure S22 (Supporting Information). Moreover, low energy consumption of around 0.9 pJ per spike is achieved with a short pulse of 20 ns in our device, which is comparable to that of biosynapse (see Figure S23 in the Supporting Information).[50]

Based on the measured LTD and LTP results, a fully connected ANN based on the PdSeOₓ/PdSe₂ memristor is simulated with NeuroSim+ platform to perform image recognition using the Modified National Institute of Standard and Technology (MNIST) database.[49] The ANN network is constructed by 400 input neurons, 100 hidden neurons, and 10 output neurons with a passive crossbar array hardware architecture, as illustrated in Figure 4e. The 400 input neurons correspond to the input image with a size of 20 × 20 pixels, and the 10 output neurons correspond to 10 classes of digits (0–9). In each training epoch, 10 000 images are randomly selected from the MNIST training dataset of 60 000 handwritten digit images and sent to the ANN for training. Subsequently, the recognition accuracy of the ANN is estimated using a separate testing dataset of 10 000 images. As shown in Figure 4f,g, recognition accuracy of about 82.86% is obtained by using identical pulses with long pulse width, while a better recognition accuracy of 88.16% can be obtained by using shorter pulses to improve the linearity and symmetry. When subjected to nonidentical pulses, the recognition accuracy can be significantly enhanced to 93.40%, which is comparable to that of ideal devices (93.95%). Furthermore, our device shows small cycle-to-cycle variations of 1.3% and 2.6% for nonidentical pulses and identical pulses, leading to recognition accuracies of 93.19% and 86.83%, respectively.

2.5. Convolutional Image Processing

Convolutional image processing is further demonstrated with our PdSeOₓ/PdSe₂ memristor crossbar array. The National University of Singapore (NUS) building is used as the input image, in which the image intensity is converted into voltages and applied across the rows of the crossbar array, as illustrated in Figure 5a. Each pixel in the processed image is generated by convoluting the input voltage (Vᵢ) and conductance (Gᵢ) vectors as mapped from a 3 × 3 input subimage and conductance matrix, respectively. Here, two memristors are used as a differential pair to represent both positive and negative weight values, and a 3 × 3 × 2 crossbar array is used to construct the target convolution kernel.[51] The product and summation of
Vij and Gij involved in the convolutional operation, i.e., \( I' = \sum Vij \times Gij \), can be implemented using the crossbar array by Ohm’s law and Kirchhoff’s current law. This can be verified by Figure 5b,c, in which the output current shows a perfect match between the total current (\( I_1 \)) and the summation of the individual current of three memristors (\( I_{11}, I_{21}, \) and \( I_{31} \)). The output currents of each column are accumulated as \( I_{out} \), and then the \( I_{out} \) is converted to the pixel (\( P_{out} \)) by software. After performing the convolution operation of the whole image, the complete extraction results are achieved.
First, we experimentally demonstrated convolutional vertical and horizontal edge detection, and average softening based on the hardware-measured (HWM) dataset. The HWM dataset is built by physically implementing the dot product and summation in the PdSeO$_x$/PdSe$_2$ memristor crossbar array, in which the memristors with two states (LRS and HRS) are used to construct the target convolution kernel. The detailed information about the image processing with HWM dataset is described in Figures S25–S28 (Supporting Information). As shown in Figure 5d,e and Figure S29 (Supporting Information), fine vertical and horizontal

**Figure 5.** Convolutional image processing implemented using PdSeO$_x$/PdSe$_2$ memristor crossbar array. a) The overall process of the convolutional image processing with the memristor crossbar array. b,c) Comparison between directly measured total current and the summation of the individual current of the memristors: b) the memristors in a column are all in HRS and c) the memristors in a column are all in LRS. d,e) Hardware- and software-processed vertical and horizontal edge extractions. For the hardware-processed image processing, the output current of each column $(I_i^+ - I_i^-) + (I_j^+ - I_j^-) + (I_k^+ - I_k^-)$ can be searched in the HWM dataset. The searched output currents are postaccumulated and converted to $I_{out}$ by the software. The Prewitt kernels are for horizontal and vertical edge detections. f) Five states are achieved by adjusting the compliance current; thus, weights of $[-4 \text{ to } 4]$ can be mapped. g) Image-processing results with five states.
edge features are successfully extracted, and softening of the image is realized with the HWM dataset. We show that comparable results are obtained between the software- and hardware-implemented convolution operations. Furthermore, we confirm that nine memristors in the $3 \times 3$ crossbar array are capable of achieving uniform and consistent five states by adjusting the compliance current, as shown in Figure S5f and in Figure S30 and Table S2 (Supporting Information). With these states, the weights of $[-4 \text{ to } 4]$ can be mapped to construct complex convolution kernels, such as Laplacian and Gaussian soft kernels (Figure S30b, Supporting Information). Thus, a plethora of image-processing results such as Gaussian soften, sharpen, embossment, arbitrary edge detection, and motion blur are successfully achieved, as shown in Figure 5g and Figure S31 (Supporting Information). Moreover, any one of the four LRS states (LRS1–LRS4) is sufficient to construct the convolution kernel with the HRS state for $45^\circ$ and $135^\circ$ edge extractions (Figure S31e–h, Supporting Information). The edge extractions described here are among the most frequently used operations, which are computationally expensive in CNNs,$^{[5,6,53]}$ manifesting the potential of a PdSeO$_x$/PdSe$_2$ memristor crossbar array as the building block for CNNs.

3. Conclusion

A low-voltage memristor concept based on ultrathin PdSeO$_x$/PdSe$_2$ heterostructure switching medium is demonstrated for the development of neural network hardware accelerator. The heterostructure, in which each layer is scaled down to 1 nm, is realized using in situ oxidation by UV–ozone to form an amorphous transition metal oxide on the defective PdSe$_2$ nanosheet. Low variability in set and reset voltages is achieved, which is attributed to the confinement of conductive filaments in the heterostructure as confirmed by the DFT calculations and kMC simulations. Furthermore, with high linearity and symmetric analog weight update coupled with tuneable conductance states, image recognition with high accuracy and multiple convolutional image processing tasks are successfully implemented. The circumstance of switching variability issue using our ultrathin PdSeO$_x$/PdSe$_2$ heterostructure design underscores its potential for the practical implementation of 2DM-based in-memory computing hardware.

4. Experimental Section

Device Fabrication: First, the bottom electrode made of Ti/Au (5 nm/20 nm) was deposited onto a 285 nm silicon dioxide using an e-beam evaporator. Next, mechanically exfoliated PdSe$_2$ nanosheet was transferred onto the bottom electrode. Then the PdSe$_2$ nanosheet was treated by UV–ozone with different times or temperatures. The fabrication was completed by depositing Ti/Au (20 nm/80 nm) as the top electrode. The top and bottom electrodes were patterned by the electron beam lithography (EBL, JBX-6300FS) using poly(methyl methacrylate) (PMMA) as the photoresist and isopropyl alcohol/methyl isobutyl ketone (IPA/MIBK) (1:3) as the developer.

Device Measurement: I–V characteristics were measured in ambient condition at room temperature using an Agilent 4155B semiconductor parameter analyzer and a probe station. The pulse measurements were carried out using a Cascade probe station connected to a 4200-SCS Keithley semiconductor analyzer.

Material Characterization: Cross-sectional HR-TEM and EDS were conducted in a Talos F200X TEM. Before TEM characterization, thin lamellae were prepared using a focused ion beam (FBI, FEI, Helios NanoLab). The top view HR-TEM and the corresponding EDS and cross-sectional EELS were conducted in JEM-ARM200F. The TEM samples were made by transferring the ozone-treated PdSe$_2$ nanosheets onto the TEM holder. XPS characterizations were performed using a Quantera PHI II system with a monochromated Al anode. The source was operated at 15 kV with an emission current of 7 mA. The CAFM was performed using Bruker Multimode V, which operates in contact mode using a Pt tip with a radius of 25 nm and a spring constant of 1 N m$^{-1}$. The vertical memristor was fabricated using ozone-treated PdSe$_2$ nanosheet as the active switching layer, sandwiched by Pt top electrode and Ti bottom electrode. The current map was collected under a constant bias of 100 mV before and after electrical stress.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

This project was supervised and directed by K.-W.A. Y.L. and K.-W.A. conceived this work. Y.L. and K.-W.A. designed the experiments. Z.Y. and Y.-W.Z. performed the DFT calculations, S.C. and Y.-W.Z. performed the kMC simulation. S.L. and Y.X. wrote the code for image processing. Y.L. conducted the electrical measurements. Y.L. and M.E.P. performed the material characterization. All authors contributed to the discussion and result analysis. Y.L. and K.-W.A. wrote the manuscript.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

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