Defect control in advanced high-mobility substrates
(invited)

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Abstract. This paper discusses the use of so-called high mobility substrates in association with defect generation and its impact on the electrical device parameters. The global or local strain engineering has to be optimized in order to avoid the harmful effects of stress-induced misfit and threading dislocations.

1. Introduction
The ITRS roadmap requires a downscaling of the minimum feature size and currently 45 nm and below technology nodes are under development. The scaling of the gate length goes hand in hand with a scaling of the vertical dimensions, requiring ultra thin gate dielectrics. However, in order to restrict the off-state power consumption the gate tunnel current has to be controlled. The latter can be obtained by using so-called high-\(k\) gate dielectrics. Essential for high-performing devices is a good control of the carrier mobility in the channel. Scaling has in general a negative impact on the channel mobility due to the highly-doped channel profiles. In addition, the quality of present-day high-\(k\) dielectrics also degrades the channel mobility caused by enhanced phonon and remote Coulomb scattering. An improvement in carrier mobility can be achieved by the use of fully silicided (FUSI) or metal gates, as clearly illustrated in figure 1. However, there is extensive research to develop substrates to further boost up the carrier mobility. There are several ways to fabricate these high-mobility substrates.

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{figure1.png}
\caption{Surface phonon limited mobility component at room temperature for devices using conventional poly-Si gate, high-\(k\) gate dielectric with poly-Si gate and high-\(k\) gate dielectric with midgap TiN metal gate, respectively [1].}
\end{figure}

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For classical CMOS, the heavily doped HALO and channel regions needed to suppress the leakage current and short channel effects degrade the low-field mobility [2]. In addition, the statistical dopant fluctuations lead to undesired threshold voltage variations. This can be overcome by the use of ultra-thin body Silicon-on-Insulator (SOI) devices. For a too low film thickness mobility degradation can be observed due to the impact of the surface roughness [3].

Another approach to boost up the low-field carrier mobility is to rely on strain engineering, whereby the changes in the lattice structure cause a splitting in the valence and conduction bands. The suppression of the intervalley scattering associated with the band splitting and/or the reduction of the in-plane effective mass may lead to an enhanced mobility [4-5]. The carrier mobility enhancement is different for holes than for electrons and depends on the value and the direction of the uniaxial or biaxial stress and on the channel orientation. Biaxial and uniaxial strains have a similar impact on the conduction band, but uniaxial strain significantly warps the valence band thereby resulting in a larger hole mobility enhancement compared to biaxial strain [6]. An example of biaxial strain in a device is a channel region with strained silicon on a relaxed buffer layer, whereas uniaxial strain can e.g. be obtained by SiGe recessed source/drain regions.

The strain engineering can be divided into two main fields, i.e., the global and the local strain approach. For the first, there is a strong interest in using epitaxial SiGe layers, whereby the stress in the film will increase the electron and hole mobility in the devices. As an alternative one can use a strained Si on a relaxed SiGe buffer layer or even directly on a buried oxide. Whether or not a strain-relaxed buffer layer is used underneath will have an impact on the density of both misfit and threading dislocations (TDs). As will be discussed further, TDs can enhance the diode leakage current, degrade the carrier lifetime and increase the low frequency noise.

A local strain can be achieved by dedicated processing steps and/or modules such as e.g. shallow trench isolation, the use of liners and capping layers, full silicidation and/or metal gate electrodes, dry etch processes, and source/drain engineering. In the latter case the source/drain regions may be formed in strained Si or SiGe recessed areas which are created by selective epitaxial growth. The stress modeling in a strained layer can be rather complex as for fully processed devices one has to take into account the different stress sources, i.e. the possible global stress and the different processing-induced local stresses. In some cases uniaxial mechanical stress is even applied after complete device processing in order to improve the device characteristics [7].

For sub 32 nm technology nodes there also exists strong interest in exploring the use of Ge substrates instead of silicon, mainly because of the enhanced carrier mobility and the overall lower thermal budget required for processing. This implies that some of the fundamental defect work performed on Si will have to be repeated for Ge. There is still uncertainty whether or not a real push forward will be achieved with Ge substrates or with Germanium-on-Insulator (GeOI).

The aim of the present paper is to review from a defect viewpoint the status of the use of several high-mobility substrates and to outline the impact of defects on the electrical device performance such as leakage current, carrier lifetime and noise characteristics.

2. Stress-induced dislocation nucleation
It is well known that for stress fields above the silicon yield stress, which depends on the concentration of intrinsic point defects like self-interstitials and vacancies, dislocation nucleation and multiplication occurs [8]. Film stresses and defect generation related to film-edge induced stress have recently been reviewed by the authors [9]. Theoretical models are available for the planar stress components, enabling to determine for a variety of substrate and film orientations the glide and climb components of the stress-induced dislocations in the silicon [10]. Dependent on the experimental conditions, 60° dislocations, dislocation half loops or Hu-loops, triangular half loops, and/or Frank-Read dislocation sources may be generated [11].

Isolation-stress-induced dislocations can be the source of so-called pipeline defects, which drastically enhance the transistor off-state leakage current [12-13]. Such defects have been observed in
LOCOS [12-13] and STI [14] isolated CMOS. A similar type of defects has also been revealed in Silicon-on-Insulator (SOI) technologies [15-16]. The origin of the higher leakage current is illustrated in figure 2 [16]: enhanced dopant diffusion along the dislocation lines or in the strained sidewall regions generates a short between source and drain, causing increased conduction via the isolation edges.

Residual stress at the interface between different layers, such as strained Si on a SiGe layer, will also lead to stress-induced dislocations. In this case one speaks about misfit and threading dislocations. As mentioned in the introduction, such layers are used for mobility enhancement. Figure 3a illustrates the process sequence of a strained Si (8 nm) layer on a stress relaxed SiGe buffer layer. The use of a SiGe:C layer has an impact on the density of both misfit and threading dislocations. A XTEM micrograph of the sandwich structure is shown in figure 3b.

### Figure 2
Cross-sectional TEM micrograph of the active Si region between source and drain, showing dislocation defects (W/L=0.875/0.35 μm) [16].

### Figure 3
(a) Schematic view of the strained Si and SiGe virtual substrates after the first growth steps (left) and after the complete fabrication cycle (right). (b) XTEM micrograph of the strained Si and the buffer layers with a SiGe:C region in-between.

### 3. Stress-induced dislocations and device performance
Stress-induced dislocations have a strong influence on a variety of electrical device parameters such as leakage current, carrier lifetime and low frequency noise. Figure 4 shows the impact of the substrate type on the leakage current of n+p diodes [17]. EMMI analyses pointed out that there is a direct agreement between the presence of threading and misfit dislocations and the leakage current. The
direct correlation between the threading dislocation density and the leakage current has been reported by Giovani et al. [18], and is illustrated in figure 5.

Figure 4. Current density vs. voltage characteristics of n+p diodes on different substrate types (T=300 K) [17].

Figure 5. Leakage current density versus threading dislocation density [18].

The impact of stress-induced dislocations present in the active device regions (depletion region) on the leakage current depends on their electrical activity. It should be remarked that there is still some controversy about the electrical activity of dislocations, whereby there exists a School claiming that dislocations are only electrically active if decorated by impurities. From that viewpoint it is important to remark that stress fields enhance the trapping of impurities. Some gettering techniques are relying on stress-field induced trapping effects, as e.g. in the case of Fe gettering by SiO₂ precipitates [19]. This implies that the local stress field may compete with the on purpose introduced gettering sites [20]. Strain relaxation will dominate the Cu precipitation process, while for Co and Ni it is of less importance [21]. In the latter case bounding dislocations enhance the metal precipitation process. This implies that the Frank partial dislocation of a stacking fault can lead to internal gettering of Ni. The recombination activity of the observed misfit and threading dislocations in the SRB structures has been studied by EBIC [22]. The dislocations can also be revealed by defect etching, as illustrated in figure 6. Clear difference is seen between the different types of dislocations.

A direct consequence of the electrical activity of the dislocations is their impact on the minority carrier lifetime. This parameter was determined by the MicroWave Absorption (MWA) technique, which also allows to determine the lifetime of the near-surface virtual substrate and strained layer, by using different excitation wavelengths [22]. For the studied samples a bulk (Si substrate) recombination lifetime $\tau \geq 100 \text{ µs}$ and a surface recombination velocity $s \geq 100 \text{ cm/s}$ were derived. It was also noticed that p-well samples have a higher effective recombination lifetime value than n-well samples and that a thick SRB layer (~350 nm) degrades the lifetime compared to the thin SRB layers (~250 nm).

It is important to remark that strain engineering has to take into account the interaction between the intentional introduced strain field (global or local) and the possible presence of defects associated with high dose implanted source/drain, halo and pocket regions. This may lead to stress relaxation, not only resulting in dislocation generation but also leading to reduced impact on the mobility [23]. In addition, the thermal stability of the strain during thermal processing has to be considered.
A last parameter that is discussed is the low frequency noise, which has been investigated in detail [24]. The presence of misfit or threading dislocations gives rise to an excess generation-recombination noise, as illustrated in figure 7 for devices in strained Si on a thin SRB layer. An increased LF noise can also be caused by an indiffusion of Ge into the gate dielectric [25-26]. However, in the absence of Ge diffusion and/or dislocation generation the LF noise is generally lower than in the reference Si devices, as shown in figure 8. This observation can be explained by the impact of the strain on the quality of the gate dielectric. Tensile stress during oxidation improves the interface quality and reduces the presence of border traps [27].

Figure 6. Defect etching used to delineate the different type of dislocations that can be observed.

Figure 7. Normalized current noise spectral density versus drain current for a 10 μm x 5 μm n-MOSFET with and without a threading dislocation.

Figure 8. Input-referred noise spectral density versus gate voltage overdrive for 10 μm x 1 μm n-MOSFETs fabricated on a silicon reference or an SRB wafer.

4. Conclusion
The variety of available high-mobility substrates is strongly improving the electrical device performance when the defect generation can be controlled. This is, however, not always
straightforward. For some of these materials the manufacturability has already been demonstrated for deep submicron technology nodes.

5. References
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