A novel structure of all-optical optimised NAND, NOR and XNOR logic gates employing a Y-shaped plasmonic waveguide for better performance and high-speed computations

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Abstract
All-optical devices have demonstrated a broad range of applications in the communication field. These devices serve as the fundamental building blocks of sophisticated integrated circuits. By integrating these devices into fields such as signal processing, chip design, and network computations, it is possible to achieve a much more efficient device. This paper describes the design of all-optical logic gates such as NAND, NOR, and XNOR using a plasmonic-based Y-shaped power combiner. The combiner employs the concept of linear interference to generate the desired logic gates. The work is simulated and analysed using MATLAB and finite-difference time domain method. The current work is framed within a 60 µm² area which is less than the size of the existing structures. The parameters characterising insertion loss, transmission efficiency, and extinction ratio are calculated and compared to those of a variety of other designs.

Keywords All-optical devices · Y-combiner · Universal logic gates · FDTD · Linear interference · Plasmonic

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1 Introduction

The demand for faster communication is surging at an unexpected rate. While the researchers are carrying several experiments to meet the needs of high-speed transmission, a new offspring called plasmonic evolved from its predecessors (Gibbs 1985; Hu et al. 2008). In the earlier days, semiconductor-based transistors served the need of electronics. It often sits back due to limitations like low speed, high power consumption and heat dissipation (Cotter et al. 1999; Priya et al. 2021). Having eliminated these, photonic evolved with high-speed communication by replacing electrons with photons (Tang et al. 2010; Holmgaaard and Bozhevolnyi 2007; Wu 2004). However, it is limited by diffraction when the order of design is close to the operating wavelength (Kumar et al. 2017). Also, the optical sources are bulk and are difficult to fabricate, making the devices larger. Plasmonics solved these limitations by combining the advantages of electronics and photonics (Hayashi and Okamoto 2012). The surface plasmon polaritons evolved as a result of surface plasmon resonance phenomenon confining at nanoscale level thereby eliminating the diffraction limit (Barnes et al. 2003; Zhang et al. 2009; Talebi et al. 2008; Gramotnev and Bozhevolnyi 2010). Various configurations of plasmonic waveguides like MIM, IMI, DLSPPW etc., are used to design the plasmonic structures (Feng et al. 2007; Zia et al. 2006; Pile et al. 2005; Charbonneau et al. 2005; Jung 2010). All optical logic gates are being proposed by many researchers around the world using several design techniques like electro-optic (EO), semiconductor optical amplifier based mach–zehnder interferometer (SOA-MZI), photonic crystals (PhC) and plasmonic (Rao et al. 2021; Fakhruldeen and Mansour 2018; Pal et al. 2020; Birr et al. 2015; Gogoi and Sahu 2015). Using these techniques, all the basic gates like NOT, AND, XNOR, OR, XOR and universal gates like NAND and NOR are realized (Taflove and Hagness 2000; Anguluri et al. 2021; Kumar et al. 2015; Kim et al. 2006; Nozhat et al. 2017). These can be used to create a variety of other combinational and sequential circuits (Singh et al. 2019; Rao et al. 2020; Isfahani et al. 2009; Nozhat et al. 2015; Singh et al. 2014). Using a Y-shaped power combiner, all optical universal logic gates such as NAND and NOR, as well as all-optical XNOR gates are presented and proven using the FDTD method (Kotb and Guo 2020; Moradi et al. 2019; Fu et al. 2012; Moniem 2017; Swarnakar et al. 2021). Surface plasmons can be seen in noble metals like silver and gold at visible and near-infrared wavelengths. Because of their absorption, scattering, and coupling properties, which are reliant on basic factors such as nanoparticle geometry, size, and position; plasmonic nanoparticles are appealing candidates for application in optical systems. In sub-wavelength plasmonic MIM waveguides with slot cavity resonators for telecommunication wavelengths, the usage of all-optical NAND, NOR and XNOR (NNX) gates is demonstrated. Because of their simple configuration and capacity to enable light confinement at the nanoscale, low crosstalk, and suitable propagation distances, two-dimensional (2D) MIM waveguides were chosen for the proposed logic device, among other reasons. It is feasible to conduct a range of logic functions with the MIM logic device without changing the phase of the input signals in subsequent implementations. The present work is categorized into several sections. The design and operation of NNX gate utilize the same structure covered in Sect. 2. Section 3, and 4 gives the simulation results and assessment of all-optical NNX respectively. Section 5 gives the conclusion of the present work.
2 Design and operation of all-optical NAND, NOR and XNOR logic gates

All-optical NNX logic gate is built using a Y-shaped plasmonic waveguide. The schematic consists of two Y-shaped power combiners which are cascaded such that the output of one Y-combiner is given as input to the second Y-combiner. The two inputs of the first combiner are considered as the ports for input signals (A and B) while third input signal is considered as the reference signal (R). The second combiner’s output serves as the output port of the designed structure. The layout of the design is depicted in Fig. 1.

The plasmonic waveguide structure is designed with a refractive index of 2.01 with a metal material of Silicon Oxynitride (Swarnakar et. al 2021). The linear interference principle governs how the Y-combiner works. A linear waveguide of length (L) 2.9 µm connects the two Y-combiners. The phase shift of the input is controlled by an external phase shifter. The entire schematic is designed under the footprint of 12 µm × 5 µm. The two inputs to logic gates are applied to the first and second ports of first Y-combiner and the output is given to the second combiner. The second Y-combiner’s second input is connected to R, which is always high. The phase of R is adjusted in accordance with the desired output of the logic gate. The principle of constructive and destructive interference occurs at the junction of each combiner. According to linear interference, if the input’s path difference is zero and phase is in the order of even multiples of π, constructive interference will occur, resulting in modulation of the optical signal, and vice versa. Similarly, if the path difference is zero and phase is in odd multiples of π, the destructive interference will occur there by cancelling the optical signal. The design specifications of the structure are shown in below Table 1.

3 Simulation results and discussion

The FDTD method employs the device analysis. A continuous transverse electric (TE) optical wave with perfectly matched boundary conditions is considered as the input. In this design, low intensity signals have an optical intensity of 1e9 W/m, while high intensity signals have an optical intensity of 3e9 W/m are used to excite the input ports with 1550 nm wavelength (Anguluri et al. 2021). All the input states of two-input NNX logic gates are considered as the input. The output states are considered as output. The simulation results are shown in Fig. 2. The output signals are compared with the expected outputs to verify the correctness of the design.

![Fig. 1 Schematic of NAND, NOR and XNOR using Y-combiner](image-url)
gate is provided with the change in phase of the inputs with either $0^0$ or $180^0$ to satisfy the gate’s output. The parameter specifications for designing NNX gate are shown in Table 2.

### 3.1 NAND logic gate

The nand gate works like, when both inputs are high, the output is low; otherwise, it is high. To improve the feasibility of constructing complicated digital circuits, universal gates must be used. The simulation and analysis of NAND gate is carried using FDTD approach. The practical outcomes are then compared to the theoretical outcomes derived using MATLAB. The NAND schematic’s simulation parameters are shown in Table 2. For 2-input NAND gate, four combinations of inputs are applied to the designed waveguide. The output of NAND gate is obtained from the output port of second combiner. The output normalized power ($P_{\text{out}}$) along with the input phase of each input combination is shown in Table 3.

From Table 3, it is clear that the output behaviour of NAND gate is satisfied. The high and low intensity output signal powers are noted. Transmission efficiency is calculated by

| Sl. no. | Simulation Parameters | NAND | NOR | XNOR |
|---------|----------------------|------|-----|------|
| 1       | Mesh size            | X ($\mu$m) | Z ($\mu$m) | X ($\mu$m) | Z ($\mu$m) | X ($\mu$m) | Z ($\mu$m) |
|         |                      | 0.0480 | 0.0438 | 0.0370 | 0.0346 | 0.0738 | 0.0738 |
| 2       | No. of mesh cells    | X     | Z     | X     | Z     | 295    | 67    |
|         |                      | 103   | 273   | 124    | 162    |
| 3       | Input field transverse | Gaussian | Gaussian | Gaussian |
| 4       | Low intensity signal | 1e9 W/m | 1e9 W/m | 3e9 W/m |
| 5       | High intensity signal | 3e9 W/m | 3e9 W/m | 3e9 W/m |
| 6       | Reference signal     | 3.3e9 W/m | 3.3e9 W/m | 3.3e9 W/m |

| Sl. no. | Input signals | A | $\phi_A$ | B | $\phi_B$ | Output signal | Transmission efficiency (%) |
|---------|---------------|---|----------|---|----------|----------------|-----------------------------|
| 1       |               | 0 | 0$^0$    | 0 | 0$^0$    | 1.0983 $\equiv$ 1 | 109                         |
| 2       |               | 0 | 0$^0$    | 1 | 180$^0$  | 1.4147 $\equiv$ 1 | 141                         |
| 3       |               | 1 | 0$^0$    | 0 | 180$^0$  | 1.4734 $\equiv$ 1 | 147                         |
| 4       |               | 1 | 0$^0$    | 1 | 0$^0$    | 0.1137 $\equiv$ 0 | 11.3                        |
multiplying the highest output power with 100 as represented in Table 3. Figure 2 displays the timing diagram of a NAND gate verified using MATLAB. Figure 3 shows the light propagation across NAND gate for all input signal combinations.

3.1.1 Case (i)

Here, a low-intensity signal of 1e9 W/m is applied as input to both of the first Y-combiner ports. A phase of 0° is applied to input A and 180° is applied to the input B. The intensity of 3.3e9 W/m with a phase of 180° is applied as input to R. The first combiner receives inputs that are out of phase and have the same intensity, there exists destructive interference at the output and the input to the next Y-combiner is assumed to be low. The other port receives R as high intensity signal and the same is driven towards the output, thereby receiving the high signal at the output as represented in Fig. 3a.

3.1.2 Case (ii)

Here, the first input port is given the signal intensity of 1e9 W/m with phase of 0° and the second input port is given the intensity of 3e9 W/m with a phase of 180°. Due to the out-of-phase nature of these signals, destructive interference occurs at the output of the first combiner, resulting in a low signal at the next input. The R being high signal as the other input causes constructive interference at the output leading to high signal as represented in Fig. 3b.

3.1.3 Case (iii)

Similar to the above case, the first and second input ports are given high and low intensity signals of intensity 3e9 W/m and 1e9 W/m respectively. The phase shift of the input ports remains same as 0° and 180° for first and second ports respectively. Due to destructive interference, the low signal reaches the next combiner and the R will reach the output port as a result of constructive interference i.e., logic ‘1’ as shown in Fig. 3c.
Fig. 3 Light propagation across NAND gate for all input signal combinations
3.1.4 Case (iv)

In this case, the two input ports are given high intensity signal of intensity 3e9 W/m. The phase shift of two inputs ports is made 0. Then according to constructive interference, the output signal will be high and of more intensity as the input signal. The R of intensity 3.3 W/m is given as the compensating signal to cancel the previous output so as to obtain the logic ‘0’ at the output. The low intensity output is observed due to occurrence of destructive interference at the output junction as shown in Fig. 3d.

3.2 NOR logic gate

The output of NOR gate is examined with the same structure as depicted in Fig. 1. The output of NOR gate goes low when any of the input is high and high when both inputs are low. The FDTD approach is used to simulate and analyse the NOR gate. The obtained practical results are then compared with the theoretical results obtained from MATLAB. The simulation specifications of NOR schematic is given in Table 2. The $P_{out}$ and input phase for all-optical NOR gate is shown in Table 4. From Table 4, it is clear that the output behaviour of NOR gate is satisfied. The transmission efficiency is also

| Sl. no. | Input signals | Output signal |
|---------|---------------|---------------|
| A  $\phi_A$ | B  $\phi_B$ | $P_{out}$ | Transmission efficiency |
| 1 | 0 0$^0$ | 0 0$^0$ | 1.3361 $\equiv$ 1 | 134 |
| 2 | 0 0$^0$ | 1 0$^0$ | 0.0136 $\equiv$ 0 | 1.36 |
| 3 | 1 0$^0$ | 0 0$^0$ | 0.0087 $\equiv$ 0 | 0.87 |
| 4 | 1 0$^0$ | 1 0$^0$ | 0.0237 $\equiv$ 0 | 2.37 |
formulated and provided in Table 4. The timing diagram of NOR gate is verified using MATLAB and is shown in Fig. 4.

3.2.1 Case (i)

In this case, the low intensity signal of 1e9 W/m with phase shift of 0° is applied as input to both the input ports of first Y-combiner. The R of intensity 3.3e9 W/m is applied as input with a phase shift of 180°. Since the first combiner takes inputs having same intensity and in phase, constructive interference will occur at the output and the input to the next Y-combiner is assumed to be low. The other port receives R as high intensity signal and the same is driven towards the output, thereby receiving the high signal at the output i.e., logic ‘1’ as shown in Fig. 5a.

3.2.2 Case (ii)

In this combination, the first input port is given the low signal of intensity 1e9 W/m and the second input port is given high signal of intensity 3e9 W/m with a phase of 0° for both ports. A high signal is obtained at the output of the first combiner as a result of constructive interference. The R being high and is out of phase with the output from first combiner causes destructive interference at the output leading to low signal as shown in Fig. 5b.

3.2.3 Case (iii)

The first and second input ports are provided with intensity of 3e9 W/m and 1e9 W/m respectively with 0° phase shift. Due to the constructive interference, the high signal reaches the next combiner and the R with high intensity which is out of phase caused destructive interference and low signal will reach the output port as in Fig. 5c.

3.2.4 Case (iv)

In this case, the two input ports are given high intensity of 3e9 W/m with a phase shift of 0°. The combiners output gives logic high signal as a result of constructive interference. This high signal is combined with R of opposite phase. Due to destructive interference at the output junction, the low signal is received at the output as shown in Fig. 5d.

3.3 XNOR logic gate

The same structure as depicted in Fig. 1 can be used to get the output of XNOR gate. The output goes low when inputs are different and high when inputs are same. The simulation and analysis of XNOR gate is carried using FDTD method. The practical findings are compared to the theoretical results generated using the MATLAB simulink tool. The simulation parameters of XNOR schematic are given in Table 2. For 2-input XNOR gate, four combinations of input values are applied as input to the design. The normalized $P_{out}$ along with the input phase is shown in Table 5 for all-optical XNOR gate.

From Table 5, it is clear that the output of XNOR gate is determined. The high and low intensity output signal powers are noted. The transmission efficiency is also formulated and provided in Table 5. The NAND gate timing diagram is presented in Fig. 6, which was simulated using MATLAB.
Fig. 5  Light propagation across NOR gate for all input signal combinations
The simulation results of the XNOR gate are shown in Fig. 7. The input combinations are applied based on the truth table of XNOR gate.

### 3.3.1 Case (i)

In this combination, the low optical signal of intensity 1e9 W/m is applied as input to both the input ports of first Y-combiner. Phase of 0° and 180° is applied to first and second input ports. The R of intensity 3.3e9 W/m is applied as input to the reference. The output of first combiner will be XOR of A and B and is given to second combiner. The other port receives R as high intensity signal and the same is driven towards the output, thereby receiving the high signal at the output as shown in Fig. 7a.

### 3.3.2 Case (ii)

Here, the first port is given the low signal of intensity 1e9 W/m with 0° phase shift and the second input port is given high signal of intensity 3e9 W/m with a phase of 180° for both ports. Due to constructive interference, high signal is obtained at the output of first combiner. The R being high signal and is out of phase with the output from first combiner causes destructive interference at the output leading to low output as shown in Fig. 7b.

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**Table 5 Simulation results of all-optical XNOR gate**

| Sl. no. | Input signals | Output signal | Transmission efficiency (%) |
|---------|---------------|---------------|-----------------------------|
| A  | ɸA  | B  | ɸB  | P<sub>out</sub>  |
| 1  | 0  | 0°  | 0  | 180°  | 1.4294 ≡ 1  | 143  |
| 2  | 0  | 0°  | 1  | 180°  | 0.0094 ≡ 0  | 1  |
| 3  | 1  | 0°  | 0  | 180°  | 0.0138 ≡ 0  | 1.3  |
| 4  | 1  | 0°  | 1  | 180°  | 0.5448 ≡ 1  | 55  |

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**Fig. 6** Timing diagram of all-optical XNOR gate using MATLAB
3.3.3 Case (iii)

Similar to the above case, the first and second input ports are given high and low intensity signals of intensity $3e9$ W/m and $1e9$ W/m respectively with $0^0$ and $180^0$ phase shift. Due to constructive interference, the high signal reaches the next combiner and
Table 6  Comparison of all-optical NAND/NOR/XNOR gate with the existing structures

| Sl. no | Ref. no       | Designed logic gate | Components          | Wavelength (nm) | Size             | Channel profile | Low intensity optical signal | High intensity optical Signal | Insertion loss (dB) | Extinction ratio (dB) | Transmission efficiency (%) |
|--------|----------------|---------------------|---------------------|----------------|------------------|----------------|----------------------------|----------------------------|----------------------|------------------------|----------------------------|
| 1      | Kumar et al. 2017) | NAND                | 4 MZIs              | 1550           | 38 × 10 µm²     | n.r.³          | 0.026e6 W/m                | 0.026e6 W/m              | n.r.³               | n.r.³                  | n.r.³                      |
|        |                 | NOR                 | 3 MZIs              | 1550           | 45 × 8 µm²      | n.r.³          | 0.026e6 W/m                | 0.026e6 W/m              | n.r.³               | n.r.³                  | n.r.³                      |
| 2      | Kumar et al. 2015) | NAND                | 3 EO-MZIs           | 1330           | ~ 70 mm         | n.r.³          | 0 V                        | 6.75 V                   | n.r.³               | n.r.³                  | n.r.³                      |
|        |                 | NOR                 | 2 EO-MZIs           | 1330           | ~ 70 mm         | n.r.³          | 0 V                        | 6.75 V                   | n.r.³               | n.r.³                  | n.r.³                      |
| 3      | Kim et al. 2006) | NAND                | 2 SOA-MZI Structures | 1539.45       | n.r.³           | n.r.³          | n.r.³                      | n.r.³                   | > 15                 | n.r.³                  |                           |
| 4      | Nozhat et al. 2017) | NAND                | 5 × 5 array of gold disk particles | 445.5 | 520 × 520 nm² | 1.5            | n.r.³                      | n.r.³                   | n.r.³               | 24                     | ~ 90                      |
| 5      | Singh et al. 2019) | NAND                | 2 MZIs              | 1550           | 40 × 7.5 µm²    | 1.65           | 0.7e9 W/m                 | 3e9 W/m                 | 0.756               | 10.25                  | n.r.³                      |
| 6      | Rao et al. 2020) | NAND                | 12×9 grid of photonic crystals | 1550 | 7.2 × 5.4 µm² | 3.46           | 0 W/m                    | 1 mW/m                  | n.r.³               | 17.59                  | n.r.³                      |
|        |                 | NOR                 | 12×9 grid of photonic crystals | 1550 | 7.2 × 5.4 µm² | 3.46           | 0 W/m                    | 1 mW/m                  | n.r.³               | 14.3 dB                | n.r.³                      |
|        |                 | XOR                 | 12×9 grid of photonic crystals | 1550 | 7.2 × 5.4 µm² | 3.46           | 0 mW                     | 1 mW                    | n.r.³               | 10.52                  | n.r.³                      |
| 7      | Isfahani et al. 1097) | NOR                 | 2 micro ring resonators | 1550 | n.r.³         | 3.1            | n.r.³                     | n.r.³                   | n.r.³               | n.r.³                  | 81%                       |
| Sl. no | Ref. no                | Designed logic gate | Components                                                                 | Wavelength (nm) | Size               | Channel profile | Low intensity optical signal | High intensity optical Signal | Insertion loss (dB) | Extinction ratio (dB) | Transmission efficiency (%) |
|-------|------------------------|---------------------|----------------------------------------------------------------------------|-----------------|--------------------|------------------|-----------------------------|------------------------|----------------------|------------------------|
| 8     | Nozhat and Granpayeh   | NOR                 | 2 square ring resonators and 3 linear wave-guides                         | 1535            | n.r.²              | 1.47             | 0.004e6 W/m                | 0.007e6 W/m            | n.r.²                | n.r.²                 | 70%                    |
| 9     | Singh et al. (2014)    | NOR                 | Two 3 dB couplers and 2 SOA amplifiers                                   | 1555            | 500 × 0.15 μm²     | n.r.²            | n.r.²                      | n.r.²                  | n.r.²                | 15.67 dB              | n.r.²                 |
| 10    | Kotb and Guo (2020)    | XOR                 | 3 SOAs and One Delayed Interferometer                                   | 1540            | n.r.²              | n.r.²            | n.r.²                      | n.r.²                  | n.r.²                | n.r.²                  |
| 11    | Morad et al. (2019)    | XOR                 | 1 square ring resonator and 3 linear wave-guides                           | 1628            | n.r.²              | 1.47             | n.r.²                      | n.r.²                  | n.r.²                | 22.66                 | n.r.²                 |
| 12    | Fu et al. (2012)       | XOR                 | Gold coated plasmonic slot wave-guide                                     | 830             | 11 μm × 100 nm     | 1.5              | n.r.²                      | n.r.²                  | n.r.²                | 24                    | 219.3                 |
| 13    | Moniem (2017)          | XOR                 | 18 × 15 array of silicon rods                                             | 1550            | 35 × 21 μm²        | 3.39             | 0 mW                       | 100 mW                 | n.r.²                | n.r.²                 | 87                    |
Table 6 (continued)

| Sl. no. | Ref. no | Designed logic gate | Components | Wavelength (nm) | Size | Channel profile | Low intensity optical signal | High intensity optical Signal | Insertion loss (dB) | Extinction ratio (dB) | Transmission efficiency (%) |
|---------|---------|---------------------|------------|----------------|------|----------------|------------------------------|----------------------------|----------------|------------------|--------------------------|
| 14      | This work | NAND                | 2 Y-combiners | 1550 | 12 × 5 µm² | 2.01 | 1e9 W/m     | 3e9 W/m                 | 0.407 | 11.13       | 147                     |
|         | NOR     | 2 Y-combiners      | 1550       | 12 × 5 µm² | 2.01 | 1e9 W/m     | 3e9 W/m                 | 1.25         | 24.29       | 134                     |
|         | XNOR    | 2 Y-combiners      | 1550       | 12 × 5 µm² | 2.01 | 1e9 W/m     | 3e9 W/m                 | 1.55         | 21.82       | 143                     |

n.r.* Not reported
the R which is out of phase causes destructive interference and low signal will reach the output port i.e., logic ‘0’ as shown in Fig. 7c.

3.3.4 Case (iv)

In this case, the two input ports are given high intensity signal of 3e9 W/m with 0° and 180° phase shift. The combiner output gives low signal as a result of destructive interference. This signal is combined with the R of opposite phase difference. Due to constructive interference at the output junction, the high signal is received at the output as shown in Fig. 7d.

4 Performance analysis of NAND/NOR/XNOR gate

The performance analysis of NAND/NOR/XNOR gate is analyzed by calculating extinction ratio (ER), insertion loss (IL) and transmission efficiency. The $P_{out}$ matches the theoretical truth table of NAND/NOR/XNOR gate and the efficiency of the transmission is as high for NAND as 147% in case of ‘10’ condition, NOR gate as high as 134% in case of ‘00’ condition, XNOR gate as high as 143% in case of ‘00’ condition.

On the basis of the output data, performance measures such as IL and ER are determined. The IL is given by

$$IL = 10\log_{10}\left(\frac{P_{out}}{P_{in}}\right)$$

(1)

where $P_{out}$ is the peak output power and $P_{in}$ is the peak input power ($P_{in}$). The ER is the proportion of peak $P_{out}$ in the ON state ($P_{out \mid ON}$) to peak $P_{out}$ in the OFF state ($P_{out \mid OFF}$). It is given by

$$ER = 10\log_{10}\left(\frac{P_{out \mid ON}}{P_{out \mid OFF}}\right)$$

(2)

The IL and ER of the all-optical NAND gate are found to be 0.407 dB and 11.13 dB respectively. The IL and ER of the all-optical NOR gate are observed to be 1.25 dB and 24.29 dB respectively. The IL and ER of the all-optical XNOR gate are found to be 1.55 dB and 21.82 dB. The comparison of present work with the existing work is shown in Table 6.

5 Conclusion

The present work proposes a miniaturised design of all-optical logic gates such as NAND, NOR, and XNOR using a Y-shaped plasmonic combiner. The work is designed, simulated, and analysed using the FDTD method. The design of this work fits within a 60 µm² area, which is smaller than the area currently occupied by existing structures. Numerous performance-related parameters such as IL, transmission efficiency, and ER are calculated from the output results. NAND, NOR, and XNOR gates have an ER of 11.13 dB, 24.29 dB, and 21.82 dB, respectively. Due to its compact structure, the size of digital circuits will be significantly reduced, resulting in improved performance in optical computing.
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Declaration

Conflicts of interest The authors declare that there are no conflicts of interest related to this article.

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