Proving LTL Properties of Bitvector Programs and Decompiled Binaries (Extended)

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Abstract. There is increasing interest in applying verification tools to programs that have bitvector operations. SMT solvers, which serve as a foundation for these tools, have thus increased support for bitvector reasoning through bit-blasting and linear arithmetic approximations. In this paper we show that similar linear arithmetic approximation of bitvector operations can be done at the source level through transformations. Specifically, we introduce new paths that over-approximate bitvector operations with linear conditions/constraints, increasing branching but allowing us to better exploit the well-developed integer reasoning and interpolation of verification tools. We show that, for reachability of bitvector programs, increased branching incurs negligible overhead yet, when combined with integer interpolation optimizations, enables more programs to be verified. We further show this exploitation of integer interpolation in the common case also enables competitive termination verification of bitvector programs and leads to the first effective technique for LTL verification of bitvector programs. Finally, we provide an in-depth case study of decompiled ("lifted") binary programs, which emulate X86 execution through frequent use of bitvector operations. We present a new tool DarkSea, the first tool capable of verifying reachability, termination, and LTL of lifted binaries.

1 Introduction

There is increasing interest in using today’s verification tools in domains where bitvector operations are commonplace. Toward this end, there has been a variety of efforts to enable bitvector reasoning in Satisfiability Modulo Theory (SMT) solvers, which serve as a foundation for program analysis tools. One common strategy employed by these SMT solvers is bit-blasting, which translates the input bitvector formula to an equi-satisfiable propositional formula and utilizes Boolean Satisfiability (SAT) solvers to discharge it. Another strategy is to approximate bitvector operations with integer linear arithmetic \cite{14}. CVC4 now employs a new approach called int-blasting \cite{58}, which reasons about bitvector formulas via integer nonlinear arithmetic.

Inspired by these SMT strategies, this paper explores the use of linear approximations of bitvector operations through source-level transformations, toward enabling Termination/LTL verification of bitvector programs. Our bitwise branching introduces new conditional, linear arithmetic paths that over-approximate
many but not all bitvector behaviors. These paths cover the common cases and, in the remaining cases, other paths fall back on the exact bitvector behavior. As a result, in the common case, the reasoning burden is shifted to linear arithmetic conditions/constraints, a domain more suitable to today’s automated Termination/LTL techniques. Bitwise branching can be combined with various tools, making it an appealing general strategy. We at first chose to implement bitwise branching within ULTIMATE \[33\] source code (during the C-to-Boogie \[12\] translation) so that we could compare against unmodified Ultimate, which is already one of the more effective Termination/LTL verifiers. Furthermore, to our knowledge other tools don’t allow one to flip a switch to enable their own bit-precise analysis (i.e., CBMC’s Bitblasting or CPAchecker’s FixedSizeBitVectors theory) or disable that analysis, abstracting with integers. We needed such a switch to evaluate bitwise branching. Other tools that employ non-bit-precise techniques simply report "Unknown" as soon as they encounter bit operations. We created rules for expressions and assignment statements, and implemented them as a source translation, it is incorporated into ULTIMATE.

We first examine the impact of bitwise branching on reachability and experimentally demonstrate that the translation imposes negligible overhead (from introducing additional paths to verify), yet allows existing tools to verifying more bitvector programs. Specifically, we first prepared 26 new bit vector reachability benchmarks, including examples drawn from Sean Anderson’s “BitHacks” repository\[1\], which use bitvector operations for various purposes. Without bitwise branching, ULTIMATE’s default setting (Z3 and SMTInterpol) is only able to verify 2 of the 26 benchmarks. We show that bitwise branching allows us to verify these benchmarks with comparable performance with existing tools across a variety of back-end SMT solvers (MathSAT, Z3, CVC4, SMTInterpol). We also show that bitwise branching is comparable in performance (both time and problems solved) with Z3.

The ability to use integer interpolation in the common case has far-reaching consequences, which we explore in the remainder of the paper. In Sec.6 we show that, for bitwise termination benchmarks, bitwise branching improves ULTIMATE and is competitive with other tools that support termination of bitvector programs (e.g., AProVE, KITTEL, CPAchecker). SV-COMP has a collection of benchmarks for various verification tasks, however, most SV-COMP benchmarks require little or no bitvector reasoning and they have no bitvector operations in them whatsoever. Others have bitvector operations, but those operations are not relevant to the property and existing tools abstract them away. Since the SV-COMP benchmarks do not include examples targeted to bitvector termination or bitvector LTL, we created new benchmarks by extending examples from the SV-COMP termination category \[7\] and submitted our benchmarks to SV-COMP repository, as well as the the AProVE bitvector benchmarks \[11\].

More notably, our work leads to one of the first tools for verifying temporal logic (LTL) properties of bitvector programs. To our knowledge, the only existing tool is ULTIMATE, and we show that bitwise branching improves Ulti-

\[1\] https://graphics.stanford.edu/~seander/bithacks.html
MATE’s ability to verify LTL from merely 3 examples to a total of 59 new LTL benchmarks (out of a total of 67 benchmarks), adapted from ULTIMATE’s LTL repository \( \text{[8]} \) and the BitHacks repository.

**Case study: temporal verification of lifted binaries.** In Sec. 7 we explore how bitwise branching can be used as part of a novel strategy for verifying decompiled (“lifted”) binaries. Lifted binaries have lost their source data-types and instead emulate the behavior of the architecture with extensive use of bitvector operations. We developed a new tool called DARKSEA, built on top of our ULTIMATE-based bitwise branching, as well as IDA PRO and McSEMA. Although these decompilation tools generate IR/C programs and today’s verification tools do parse C programs, we also describe some critical translations that were needed to make the output of McSEMA suitable for verification (rather than re-compilation).

We experimentally validated our work and show that DARKSEA is the first tool for verifying temporal properties of lifted binaries. DARKSEA is able to prove or disprove LTL properties of 8 lifted binaries. The most comparable alternative is ULTIMATE, which cannot prove any of them without DARKSEA’s translations, and can only verify 6 of them without bitwise branching.

**Contributions.** In summary, our contributions are:

- (Sec. 4) Bitwise branching for introducing paths with linear approximations.
- (Sec. 5) An evaluation showing that it allows one to prove reachability of more bitvector programs, with negligible overhead.
- (Sec. 6) An evaluation showing competitive performance on termination, and the first effective technique for LTL of bitvector programs.
- (Sec. 7) A case study and new tool called DARKSEA, the first temporal verification technique for decompiled (lifted) binaries.
- New suites of bitvector benchmarks for reachability (23), termination (31), LTL (41) and lifted binaries (8).

We conclude with related work (Sec. 8). All code, proofs and benchmarks are available online \( \text{[2]} \).

## 2 Motivating Examples

| (1) Reachability | (2) Termination | (3) LTL \( \varphi = \square (\Diamond (n < 0)) \) |
|-------------------|----------------|----------------------------------|
| `int r, s, x;` | `a = *; assume(a>0);` | `while(1) {` |
| `while (x>0){` | `while (x>0){` | `n = *; x = *; y = x-1;` |
| `z = x >> 31;` | `a--;` | `while (x>0 && n>0) {` |
| `x--;` | `x = x & a;` | `n++;` |
| `r = x + (s&(1-s));` | `y = x \| n;` | `y = x - y;` |
| `if (r<0) error();` | `x = x - y;` | `n = -1;` |
| `}` | `}` | `}` |
| `}` | `}` | `}` |
| `and_reach1.c` | `or_loop3.c` | `or_loop3.c` |

\( \text{[2]} \) github.com/cyruliu/darksea
We will refer to the above bitvector programs throughout the paper. To prove error unreachable in the Example (1), a verifier must be able to reason about the bitvector \( \gg \) and \& operations. Specifically, it must be able to conclude that expression \( s\& (1-s) \) is always positive (so \( r \) cannot be negative) which also depends on the earlier \( x\gg 31 \) expression. We will use this example to explain our work in Sec. 4, and compare performance of ULTIMATE using state-of-the-art SMT solvers, with and without bitwise branching.

We will see that the key benefits of bitwise branching arise when concerned with termination and LTL. Example (2) involves a simple loop, in which \( a \) is decremented, but the loop condition is on variable \( x \), whose value is a bitvector expression over \( a \). Today’s tools for Termination of bitvector programs struggle with this example: AProVE, CPAchecker and ULTIMATE report unknown and KITTeL and 2LS timeout after 900s (Apx. E). Critical to verifying termination of this program are (1) proving the invariant \( x > 0 \land a > 0 \) on Line 3 within the body of the loop and (2) synthesizing a rank function. To prove the invariant, tools must show that it holds after a step of the loop’s transition relation \( T = x > 0 \land a’ = a - 1 \land x’ = x\& a’ \), which requires reasoning about the bitwise-\& operation because if we simply treat the \& as an uninterpreted function, \( I \land T’ \land x’ > 0 \not\Rightarrow I’ \).

The bitwise branching strategy we describe in this paper helps the verifier infer these invariants (and later synthesize rank functions) by transforming the bitvector assignment to \( x \) into linear constraint \( x \leq a \), but only under the condition that \( x \geq 0 \) and \( a \geq 0 \). That is, bitwise branching translates the loop in Example (2) as depicted in the gray box to the right. This transformation changes the transition relation of the loop body from \( T \) (the original program) to \( T’ \):

\[
T’ = x > 0 \land a’ = a - 1 \land ((x \geq 0 \land a’ \geq 0 \land x’ \leq a’) \lor \neg (x \geq 0 \land a’ \geq 0) \land x’ = x\& a’)
\]

Importantly, when \( I \) holds, the else branch with the \& is infeasible, and thus we can treat the \& as an uninterpreted function and yet still prove that \( I \land T’ \land x’ > 0 \not\Rightarrow I’ \). With the proof of \( I \) a tool can then move to the next step and synthesizing a ranking function \( R(x, a) \) that satisfies \( I \land T’ \Rightarrow R(x, a) \geq 0 \land R(x, a) > R(x’, a’) \), namely, \( R(x, a) = a \).

Bitwise branching also enables LTL verification of bitvector programs. We examine the behavior of programs such as Example (3) above, with LTL property \( \Box (\Diamond (n < 0)) \). The state of the art program verifier for LTL is ULTIMATE, but ULTIMATE cannot verify this program due to the bitvector operations. (ULTIMATE’s internal overapproximation is too imprecise so it returns Unknown.) In Sec. 6 we show that with bitwise branching, our implementation can prove this property of this program in 8.04s.

**Case study: Decompiled binary programs.** In recent years many tools have been developed for decompiling (or “lifting”) binaries into a source code format \[\text{\cite{15,49,10,27,55}}\]. The resulting code, however, has long lost the original
source abstractions and instead emulates the hardware, making frequent use of
bitvector operations. These challenging programs are beyond the capabilities of
existing tools for LTL verification, making them an interesting case study.

Consider the (source) program shown to the right. This program, which does
not contain any bitvector operations, is taken from the Ultimate
repository\(^3\).

```c
while(1) {
    y = 1; x = *;
    while (x>0) {
        x--; 
        if (x <= 1) y = 0; }
} }
```

Some existing techniques and tools (e.g., [21,8]) can
prove that the LTL property $$\square(x > 0 \Rightarrow \diamond(y = 0))$$ holds. However, after the program is compiled
(with gcc) and then disassembled and lifted (with
IDPro and McSema), the resulting code has many
bitvector operations. The resulting lifted code is
quite non-trivial (full version in Apx. A) and re-
quired substantial engineering efforts just to parse and analyze with existing
verifiers (see Sec. 7). Let’s first focus on the bitvector complexities; here is a
fragment of the lifted IR (in C for readability):

```c
while(true) {
    tmp_x = load i32, i32* bitcast (% x_type* $x to i32*)
    ... 
    if ( ((tmp_x >> 31) == 0) & ((tmp_x == 0) ^ true) ) {
        tmp_40 = add i32 tmp_x , -1
        store i32 tmp_40 , i32* bitcast (% x_type* $x to i32*)
    tmp_xp = load i32, i32* bitcast (% x_type* $x to i32*)
    tmp_42 = tmp_xp + -1; tmp_45 = tmp_42 >> 31;
    tmp_43 = tmp_xp + -2; tmp_46 = tmp_42 >> 31;
    if ((((((tmp_42 != 0u)&1)) & ((((((tmp_44 == 0u)&1)) ^ ((((((tmp_44 ^
    tmp_45 )) == 2u)&1)))&1)))&1))) {
        store i32 0, i32* bitcast (% y_type* $y to i32*)
    } else { break; }
}
```

Roughly, Line 4 corresponds to the $$x>0$$ comparison, and Line 10 corresponds
to the $$x<=1$$ comparison. These bitvector operations, introduced to emulate the
behavior of the binary, make it challenging for existing verification tools.

We describe a new tool DARKSEA that uses bitwise branching in the context
of a decompilation toolchain involving IDA Pro, McSema and Ultimate. The
lifting performed by tools like McSema is geared toward recompilation rather
than verification, thus foiling existing tools. In Sec. 7.2 we describe translations
performed by DARKSEA to tailor lifted binaries for verification. In Sec. 7.3 our
experimental results show that DARKSEA is the first tool capable of proving
reachability, termination and LTL of lifted binaries.

### 3 Preliminaries

Our formalization is based on Boogie programs\(^3\), denoted $$P$$. Our implemen-
tations parse input source C programs (or binaries recompiled to C) that may
have bitvector operations. These programs are then translated into Boogie pro-
go, in which bitvector operations are represented as uninterpreted functions.

\(^3\)http://github.com/ultimate-pa/ultimate/blob/dev/trunk/examples/LTL/simple/
PotentialMinimizeSEVPABug.c
Below is an abbreviated expression syntax of $P$:

$$
e ::= \text{Lit} \mid \text{Id} \mid \ldots \mid \text{UninterpFn}$$

$$\text{BinOp} ::= \ast \mid \div \mid \% \mid \&\& \mid || \mid ==> \mid <==> \mid \ldots$$

$$\text{UnOp} ::= - \mid ! \ldots$$

$$\text{UninterpFn} ::= \text{bwAnd} \mid \text{bwOr} \mid \text{bwXor} \mid \text{bwShL} \mid \text{bwShR} \mid \text{bwCompl}$$

Ultimate is an automaton based program analysis framework \[35\], it’s internal representation is boogie program with customized syntax. Figure 1 shows boogie statement syntax implemented in Ultimate, automatic abstraction techniques (such as predicate analysis \[20\] and interpolation \[45\]) are employed on building control-flow automata.

**Definition 1 (Control-flow automaton).** A (deterministic) control flow automaton (CFA) \[39\] is a tuple $A = (Q, q_0, X, s, \rightarrow)$ where $Q$ is a finite set of control locations and $q_0$ is the initial control location, $X$ is a finite sets of typed variables, $s$ is the loop/branch-free statement language (as defined earlier) and $\rightarrow \subseteq Q \times s \times Q$ is a finite set of labeled edges.

We assume conditional branching has been transformed to non-deterministic branching: $\text{if } \ast \text{ then } \{ \text{assume}(b); s_1 \} \text{ else } \{ \text{assume}(\neg b); s_2 \}$. As discussed later, Ultimate (used in our implementation) has two modes: “bitvector mode,” in which these uninterpreted expressions are translated into SMT bitvector sorts and “integer mode,” in which they remain uninterpreted.

For the semantics, we assume a state space $\Sigma : \text{Var} \rightarrow \text{Val}$, mapping variables to values. We let $[e] : \Sigma \rightarrow \text{Val}$ and $[s] : \Sigma \rightarrow \mathcal{P}(\Sigma)$ be the semantics of expressions and statements, respectively, and $[P]$ denotes traces of $P$.

4 Bitwise-branching

We build our bitwise-branching technique on the known strategy of transforming bitvector operations into integer approximations \[14,58\] but explore a new

\[https://github.com/ultimate-pa/ultimate/wiki/Boogie\]
direction: source-level transformations to introduce new conditional paths that approximate many (but not all) behaviors of a bitvector program. These new paths through the program have linear input conditions and linear output constraints and frequently cover all of the program’s behavior (with respect to the goal property), but otherwise fall back on the original bitvector behavior when none of the input conditions hold. We provide two sets of bitwise-branching rules:

1. **Rewriting rules** of the form $C \vdash_E e_{bv} \leadsto e_{int}$ in Fig. 2a. These rules are applied to bitwise arithmetic expressions $e_{bv}$ and specify a condition $C$ for which one can use integer approximate behavior $e_{int}$ if $e_{bv}$. In other words, rewriting rule $C \vdash_E e_{bv} \leadsto e_{int}$ can be applied only when $C$ holds and a bitwise arithmetic expression $e$ in the input conditions is matched to an expression $e_{bv}$ with a substitution $\delta$. Then, $e$ will be transformed into a conditional approximation: $C \delta \vdash e_{int} \delta : e_{bv}$. Note that, although modulo-2 is computationally more expensive, it is often more amenable to integer reasoning strategies. For conciseness, we omitted variants that arise from commutative re-ordering of the rules (in both Figs. 2a and 2b).
For example, consider the bitvector arithmetic expression \( s \& (1 - s) \) in Example (1) of Sec. 2. If we apply the rewriting rule 
\[
E_1 \geq 0 \land E_2 = 1 \vdash E_1 \& E_2 
\]
with the substitution \( s/e_1, 1-s/e_2 \) then the expression is transformed into \( s \gg 0 \land \text{if } (1-s)=1 ? s \% 2 : (s \& (1-s)) \). Since \( s \) reflects the sign bit of the positive variable \( x \), it is always 0 and the if condition is feasible. In general, we can further replace the remaining bitwise operation in the else expression with other applicable rules. There may still be executions that fall into the final catch-all case where the bitwise operation is performed. However, as we see in the subsequent sections of this paper, these case splits are nonetheless practically significant because often the final else is infeasible.

2. Weakening rules of the form 
\[
C \vdash S \ s_{bv} \leadsto s_{int}
\]
are in Fig. 2b. These rules are applied to relational condition expressions (e.g., from assumptions) and assignment statements \( s_{bv} \), specifying an integer condition \( C \) and overapproximation transition constraint \( s_{int} \). When the rule is applied to a statement (as opposed to a conditional), replacement \( s_{int} \) can be implemented as \( \text{assume}(s_{int}) \). When a weakening rule \( C \vdash S \ s_{bv} \leadsto s_{int} \) is applied to an assignment \( s \) with substitution \( \delta \), the transformed statement is \( \text{if } C \delta \text{ assume}(s_{int}\delta) \text{ else } s_{bv} \). In addition, when \( s_{bv} \) of a weakening rule can be matched to the condition \( c \) in an \( \text{assume}(c) \) of the original program via a substitution \( \delta \), then the \( \text{assume}(c) \) statement is transformed to \( \text{if } C \delta \text{ then } \text{assume}(s_{int}\delta) \text{ else } \text{assume}(c) \). Following up Example (2) of Sec. 2 consider the set of statements of given program as alphabet set in CFA, Fig. 3 shows this rule application for \( x = x \& a \) in automaton level, the top is the original automaton, the bottom is the transformed automaton after bitwise branching rule applied.

**Lemma 1 (Rule correctness).** For every rule \( C \vdash E \ e \leadsto e' \), \( \forall \sigma. \ C(\sigma) \Rightarrow [e]\sigma = [e']\sigma \). For every \( C \vdash S \ s \leadsto s' \), \( \forall \sigma. \ C(\sigma) \Rightarrow [s]\sigma \subseteq [s']\sigma \).

We encode each rule in Z3 script, proof details are in Appendix D. The rules in Fig. 2a and Fig. 2b were developed empirically, from the reachability/termination/LTL benchmarks in the next sections and, especially, based on patterns found in decompiled binaries (Sec. 7). We then generalized these rules to expand coverage.

**Translation algorithm.** We implemented bitwise branching via a translation algorithm, in a fork of Ultimate. We denote our version as UltimateBW, and will be releasing it publicly shortly. Our translation acts on the AST of the program, with one method \( T_E : \text{exp} \rightarrow \text{exp} \) to translate expressions and another method \( T_S : \text{stmt} \rightarrow \text{stmt} \) to translate assignment statements, each according to the set of available rules, algorithms of \( T_E \) and \( T_S \) see Apx. C.

In brief, when we reach a node with a bitwise operator, we recursively translate the operands, match the current operator against our collection of rules, and apply all matching rules to construct nested if-then-else expressions/statements. We found that, when multiple rules matched, the order did not matter much.

Let \( T_E(e) : e \) denote the result of applying substitutions to \( e \), and similar for \( T_S(s) : s \). We lift this to a translation on a Boogie program \( P \) with \( T_E(P) : P \) and \( T_S(P) : P \), referring to all expressions and statements in \( P \), respectively.
Theorem 1 (Soundness). For every $P, T_E, T_S$, $[P] \subseteq [T_S\{T_E\{P\}\}]$.

Proof. Induction on traces, showing equality on expression translation $T_E$ via induction on expressions/statements and then inclusion on statement translations $T_S$. First show that $T_E$ preserves traces equivalence. Structural induction on $e$, with base cases being constants, variables, etc. In the inductive case, for a bitvector operation $e_1 \otimes e_2$, assume $e_1, e_2$ has been (potentially) transformed to $e'_1, e'_2$ (resp.) and that Lemma 1 holds for each $i \in \{1, 2\}$: $\forall \sigma. [e_i] \sigma = [e'_i] \sigma$. Since $\otimes$ is deterministic, $[e'_1 \otimes e'_2] \sigma = [e_1 \otimes e_2] \sigma$. Finally, applying the transformation to $\otimes$, we show that $[T_E\{e'_1 \otimes e'_2\]}] = [e'_1 \otimes e'_2] \sigma$ again by Lemma 1.

Next, for each statement $s$ or relational condition $c$ step, we prove $T_S$ preserves trace inclusion: that $[s] \subseteq [T_S\{s\}]$ or that $[c] \subseteq [T_S\{c\}]$. We do not recursively weaken conditional boolean expressions, which would require alternating strengthening/weakening. Thus, inclusion holds directly from Lemma 1.

5 Reachability of Bitvector Programs

We now evaluate the effectiveness of bitwise branching (BwB), as implemented in our UltimateBwB, toward reachability verification over our new suite of 28 bitvector programs, including those adapted from existing code snippets like the “BitHacks” programs, which use bitwise operations for various tasks.

We ran our experiments with BenchExec [13] on a machine with an AMD Ryzen 3970X 32 Core CPU with 3.7GHz and 256GB RAM running Linux 5.4.65. We limited CPU time to 5 minutes, memory to 8GB, and restricted each run to two cores. We built Ultimate 0.2.1 from source and used it as baseline.

The results are summarized in Table 1. Labels are ✓ for satisfied properties, ✗ for violated properties with counterexamples, and ? for the unknown results where the tools could not decide. We also report timeouts (T), out-of-memory (M), crashes (✓), and highlight false positive (✓) and false negative (✗) results in gray, if any. Ultimate has two modes: integer and bitvector, each specialized to the corresponding kind of programs. In Ultimate’s integer mode, overflow/underflow is accounted for with assume statements. In its bitvector mode, Ultimate can utilize a variety of back-end SMT solvers with internal bitvector reasoning strategies, such as CVC4, Z3 and MathSAT (MS). By contrast, UltimateBwB does not use bitvector mode but instead transforms bitvector programs (through bitwise branching) and verifies them in Ultimate’s integer mode using the same set of back-end SMT solvers. Table 1 shows that...

github.com/ultimate-pa/ultimate b4afca67, dev
the performance of the integer verification with bitwise branching is comparable to the bitvector verification, despite the fact that the bitwise branching transformation may introduce many new paths.

Because ULTIMATE’s verification algorithms heavily utilize interpolation for optimizations, we also ran the experiment with interpolation enabled when possible, using MathSAT’s interpolation (MS Itp, in both modes) and SMTINTERPOL (SItp, only in the integer mode because SMTINTERPOL does not support bitvectors). Notably, without bitwise branching, ULTIMATE can only verify 2 of 28 programs using the default setting (SItp+Z3) in its integer mode while ULTIMATEBWB can verify all 28 programs in the same settings. Moreover, while interpolation is less effective in the bitvector mode (see MS Itp vs. MS), when combined with bitwise branching in the integer mode, it improves over those solvers (about 1.2x speedup, the total time for all benchmarks at the bottom row of Table I e.g. see total time, BwB MS Itp vs BwB SItp+Z3) and has the best results (BwB SItp+Z3 column).

6 Termination and LTL of Bitvector Programs

We now evaluate bitwise branching on the main target: liveness properties of bitvector programs. There are few comparable tools that support bitvector
reasoning and these properties; the most comparable (and mature) tools are listed to the right, along with their limitations.

**Termination.** We compare bitwise branching with the termination provers in the table to the right. We applied these tools to two benchmarks suites: (i) We first used 18 bitvector terminating programs selected from AProVE’s bitvector benchmarks [33]. Notably, those benchmarks were designed with general bitvector arithmetic in mind so that there is only a small portion of bitvector programs in it (i.e. 18/118 or 15%). (ii) We therefore built a second set of 31 termination benchmarks, including 18 terminating programs (✔) and 13 non-terminating programs (✗), called TermBitBench with bitvector operations including bitwise |, &, ~, <<, >>.

**Results.** To the right is a table summarizing our results (details see Apx. [E]). For the AProVE benchmarks, our tool can correctly prove the termination or non-termination of 2 programs, which is less than the number of programs that can be proved by CPAchecker (3), KITTeL (3), and 2LS (14). However, for TermBitBench, while UltimateBWB can prove all 31 programs, CPAchecker, KITTeL, and 2LS can only prove at most 16 programs. Moreover, while our tool was built on top of Ultimate, it outperforms Ultimate in proving termination and non-termination of bitvector programs. This is because Ultimate’s algorithms for synthesizing termination [30] and non-termination proofs [43] are not applicable to SMT formulas containing bitvectors. As a consequence, Ultimate relies on integer-based encodings of source programs together with overapproximations of bitwise operations. These results confirm that bitwise branching provides an effective means for termination of bitvector programs. Note that there are 6 false results in AproveBench for termination, they are spurious counterexamples that arise due to Ultimate’s overapproximation for unsigned integers, they do not involve branches created by our bitwise branching strategy.

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| Tool            | BitVec | Term | LTL |
|-----------------|--------|------|-----|
| ULTIMATE        | Limited | Yes  | Yes |
| AProVE          | ✔      | Yes  | No  |
| KITTeL          | ✔      | Yes  | No  |
| CPAchecker      | ✔      | Yes  | No  |
| 2LS             | ✔      | Yes  | No  |
| UltimateBwb     | Yes    | Yes  | Yes |

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6 [github.com/aprove-developers/aprove-releases/releases](https://github.com/aprove-developers/aprove-releases/releases), master, 2019-09-03
7 [github.com/s-falke/kittel-koat](https://github.com/s-falke/kittel-koat), c00d21f, master
8 [github.com/sosy-lab/cpachecker](https://github.com/sosy-lab/cpachecker), c2f1d8cce6, master
9 [github.com/diffblue/2ls](https://github.com/diffblue/2ls), d35ccf73, master
Linear temporal logic. We compared our tool against Ultimate, which is the state-of-the-art LTL prover and the only mature LTL verifier that supports bitvector programs. To our knowledge, there are no available bitwise benchmarks with LTL properties so we create new benchmarks for this purpose: (iii) New hand-crafted benchmarks called LTLBitBench of 42 C programs with LTL properties, in which bitwise operations are heavily used in assignments, loop conditions, and branching conditions. There are 22 programs in which the provided LTL properties are satisfied (✔) and 20 programs in which the LTL properties are violated (✗). (iv) Benchmarks adapted from the “BitHacks” programs, consisting of 26 programs with LTL properties (18 satisfied and 8 violated).

The table to the right summarizes the result of applying Ultimate and UltimateBwB on these two bitvector benchmarks (see Apx. [1] for details). UltimateBwB outperforms Ultimate: UltimateBwB can successfully verify 41 of 42 programs in LTLBitBench and 18 of 26 BitHacks programs while Ultimate can only handle a few of them. Note that we have more out-of-memory results in BitHacks Benchmarks, perhaps due to memory consumption reasoning about the introduced paths. In conclusion, bitwise branching appears to be the first effective technique for verifying LTL properties of bitvector programs.

| (iv) BitHacks | (iii) LTLBitBench |
|---------------|-------------------|
| ✔️ Ultimate w. BwB | ✔️ Ultimate w. BwB |
| 3 | 10 |
| ✗ | ✗ |
| ? | 21 |
| T | 1 |
| M | 1 |

7 Case Study: LTL of Decompiled Binaries

Decompiled binary executables are rife with bitvector operations, making them an interesting domain for a case study. Many tools [27, 53, 29, 30, 40, 25] have been developed for decompilation. Similar to compilation, the decompilation process consists of multiple phases, beginning with disassembly. Some techniques have emerged for verifying low-level aspects of decompiled binaries such as architectural semantics [52, 24, 11], decomposition into logic [47, 48, 49, 55], and translation validation [23] (discussed in Sec. 8).

Further along the decompilation process, other tools aim to represent a binary at a higher level of abstraction through a process called lifting. A lifted binary can be represented in IR or source code, but includes only some of the source-level abstractions of the original program. Instead, a lifted “program” emulates the machine itself, with data structures that mimic the hardware (e.g., registers, flags, stack, heap, etc.) and control that mimics the behavior of the binary.

While some of the above mentioned works involve manual or semi-automated proofs of safety properties, we have not yet seen many automated techniques for verifying reachability, termination and temporal properties of those lifted binaries. To a large extent today’s automated verification techniques have relied on source abstractions (e.g., invariants and rank functions over loop variables, structured control flow, procedure boundaries, etc.).
7.1 Bitvector operations in lifted binaries

Lifted binaries frequently use bitvector operations, e.g., to reflect signed/unsigned comparison of variables whose type was lost in compilation. As we show in Sec. 7.3, lifted programs are beyond the capabilities of termination verification tools such as Ultimate, CPAchecker, AProVE or KITTeL.

Returning to Example (3), while the source code for the inner loop of PotentialMinimizeSEVPABug.c is straight-forward (decrementing \( x \) and assigning 0 to \( y \) if \( x \leq 1 \)), the corresponding expressions in the lifted binaries involve multiple bitvector operations:

\[
(((\text{tmp}_42 \neq 0u) \& 1) \& \\
(((\text{tmp}_44 == 0u) \& 1) ^ (((\text{tmp}_44 \oplus \text{tmp}_45) + \text{tmp}_45) == 2u) \& 1))) \& 1
\]

This expression simulates branch comparisons that the machine would perform on values whose type was discarded during compilation. The source code variable \( x \) is a signed integer, but compilation has stripped its type. During decompilation, to approximate, lifting procedures consider these \( \text{tmp} \) variables (and all integer variables) to be unsigned. Meanwhile, in the binary, the condition \( x \leq 0 \) is compiled to be a signed comparison. Therefore, lifting recreates a signed comparison using the unsigned \( \text{tmp} \) variables. Lifted binaries are good candidates for bitwise branching. For the above example, we can use three rules: R-RightShift-Pos, R-And-1, R-And-Log (rule labels see Apx. B).

7.2 DarkSea: A toolchain for temporal verification of lifted binaries

Bitvector operations are not the only issue: lifted binaries have several other wrinkles that preclude them from being verified with today’s tools. We briefly discuss these issues and how we address them in a new toolchain called DarkSea, the first tool capable of verifying reachability, termination and LTL properties of lifted binaries. DarkSea is comprised of several components:

DarkSea takes as input a lifted binary (obtained from IDA Pro and McSema) in LLVM IR format, which then can be converted to C via llvm-cbe.

Lifting tools like McSema \cite{10, 27} are often designed with the goal of re-compilation rather than verification. Consequently, the McSema IR, even if converted to C, cannot be analyzed by existing tools (see Sec. 7.3) which either crash, timeout, memout, or fail during parsing. We therefore perform a series of translations discussed below to re-target the lifted binaries into a format more amenable to verification, which we then input to UltimateBwB. The translations below work with LLVM-8.0 and consist of around 500 lines of C++ and 200 lines of bash. We also identified and fixed several defects in McSema \cite{11, 0, 5}. 
1. **Run-time environment.** For re-compilation, lifting yields code that switches context between the run-time environments and the simulated code, akin to how a loader moves environment variables onto the stack. A first pass of DarkSea analyzes lifted output to discover the original program’s main, decouples the surrounding context-switch code, and removes it.

2. **Passing emulation state through procedures.** McSema generates lifted programs in which function arguments pass emulation state that is used for re-compilation. We found this to make it difficult for verifiers to track state. We thus eliminate these arguments from every function call, creating a single global pointer to the emulation state struct and replacing all uses of the first argument in the function body with a use of our new pointer.

3. **Nested structures.** Lifted binaries simulate hardware features (e.g., registers, arithmetic flags, FPU status flags) and, for cache efficiency, represent them as nested structures, e.g., `state->general_registers.register13.union.uint64cell`. DarkSea flattens these nested data structures, creating individual variables for all the innermost and separable fields, and then translates accesses to these nested structures.

4. **Property-directed slicing.** Not all the instructions are relevant to the properties we aim to verify, so we further slice the program to keep only property-dependent code, using DG [17] in termination-sensitive mode. For LTL properties, we use the atomic propositions’ variables to seed our slicing criteria.

More detail about these translations (and an example) can be found in Apx. H.

### 7.3 Experiments

We evaluated whether our translations (Sec. 7.2) and bitwise branching (Sec. 4) enabled tools to verify termination and LTL properties of decompiled binaries.

**Table 2: Termination of Lifted Binaries, with and without DarkSea translations.**

| Raw McSema | DarkSea transl. |
|------------|-----------------|
| APROVE     | APROVE          |
| CPAchecker| CPAchecker     |
| KITTeL     | KITTeL         |
| 2LS        | 2LS            |
| ULTIMATEBwB| ULTIMATEBwB    |
| ✔️         | ✔️              |
| -          | -               |
| -          | -               |
| -          | -               |
| -          | -               |
| T          | T               |
| -          | -               |
| -          | -               |
| ?          | ?               |
| 18         | 18              |
| -          | -               |
| 18         | 18              |
| -          | -               |
| 18         | 18              |
| -          | -               |
| 18         | 18              |
| -          | -               |

As discussed in Sec. 6, there are several termination provers that support bitvector programs. We thus applied those termination provers to today’s lifting results on both the raw output of McSema and then on the output of our translation. We used a standard termination benchmark (i.e., 18 small, but challenging programs in literature selected from the SV-COMP termination-crafted benchmark). As discussed in Sec. 7.2, lifted code is more complicated than its corresponding source (e.g., >10k vs 533 LOC in total). Although today’s termination
provers can verify the source of these programs, they struggle to analyze the corresponding code lifted from the programs’ binaries, as seen in the **Raw McSema** columns in Table 2 (Details are given in Tables 8 and 9 in Apx. [H].) We devoted genuine effort to overcome small hurdles but, fundamentally, without the **DarkSea** translations, tools struggled for the following reasons:

- **AProVE**: Errors in conversion from LLVM IR to internal representation.
- **KITTeL**: Parsing (from C to KITTeL’s format via LLVM bitcode with LLVM2KITTeL) succeeded, but then KITTeL silently hung until timeout.
- **CPAchecker**: Crashes on all benchmarks, while parsing system headers.
- **ULTIMATE**: Crashes on 3 benchmarks, due to inconsistent type exceptions.

Table 2 also shows the verification results of those termination provers when applied to **DarkSea**’s translated output (second set of columns).

In sum, the results show that our translations benefit both CPAchecker and ULTIMATE (which already have sophisticated parsers), reducing crashes in analyzing lifted code. As highlighted in green, **DarkSea** translations enabled ULTIMATE to prove termination on all of the 18 lifted programs, as compared to ULTIMATE timing out on 15 of the programs without **DarkSea**’s translations.

**LTL of lifted binaries.** We finally evaluate the effectiveness of **DarkSea** in proving LTL properties of 8 lifted binaries. In Table 3 we report the LTL property and expected verification result of each benchmark, as well as the verification time and result of ULTIMATE and **DarkSea** on them (details in Apx. [I]). Green cells use slightly different settings (enabled SBE, there are various setting strategies in ULTIMATE framework [33]). **DarkSea**’s translations eliminate unsoundness results that come from applying ULTIMATE directly to McSema IR (detailed table in Apx. [I]).

**Table 3: ULTIMATE vs. **DarkSea** on lifted programs with LTL properties.**

| Benchmark         | Property         | Exp. | Ultimate | DarkSea |
|-------------------|------------------|------|----------|---------|
| 01-exsec2.s.c.c   | ♦]**(x = 1)**    | ✔    | 4.45s    | 11.23s  |
| 01-exsec2.s.f.c.c | ♦)**(x ≠ 1)**    | ✗    | 6.31s    | 10.36s  |
| SEVPA_gccO0.s.c   | □**(x > 0 ⇒ y = 0)** | ✔    | 6.31s    | 22.92s  |
| SEVPA_gccO0.s.f.c | □**(x > 0 ⇒ y = 2)** | ✗    | 5.16s    | 14.92s  |
| acqrel.simplify.s.c | □**(x = 0 ⇒ y = 0)** | ✔    | 5.17s    | 9.00s   |
| acqrel.simplify.s.f.c.c | □**(x = 0 ⇒ y = 1)** | ✗    | 6.06s    | 17.60s  |
| exsec2.simplify.s.c | □**(x = 1)**    | ✔    | 4.92s    | 5.60s   |
| exsec2.simplify.s.f.c.c | □**(x ≠ 1)**    | ✗    | 4.55s    | 6.28s   |

In summary, we have shown that **DarkSea** can verify reachability, termination and LTL properties of lifted binaries. To our knowledge, **DarkSea** is the first to do so.
8 Related Work

Bitvector reasoning. Many works support bitvector reasoning in SMT solvers (e.g., [56]). Kroening et al. [42] perform predicate image over-approximation. Niemetz et al. [50] propose a translation from bitvector formulas with parametric bit-width to formulas in a logic supported by SMT solvers, making SMT-based procedures available for variant-size bitvector formulas.

He and Rakamarić [32] build on spurious counterexamples from overapproximations of bitvector operations. Mattsen et al. [44] use a BDD-based abstract domain for indirect jump reasoning. Bryant et al. [16] iterative construct an abstraction of a bit vector formula.

Other works have targeted reasoning about termination of bitvector programs. Cook et al. [22] use Presburger arithmetic for representing rank functions. Chen et al. [19] employ lexicographic rank function synthesis for bit precision and rely on the bit-precision of an underlying SMT solver. Falke et al. [28] propose an approach, implemented in KITTeL, which derives linear approximations of bitvector operations using some rules similar to our bitwise-branching rules for expressions. However, Falke et al. create a large disjunction of cases which puts a large burden on the solver. By contrast, our bitwise-branching creates multiple verification paths, but solver queries for most of them can be avoided through integer interpolation. As we show in Sec. 6 our UltimateBwB was able to solve 33/49 benchmarks, whereas KITTeL solved only 10. Moreover, KITTeL does not support LTL properties and crashes on lifted binaries.

Tools for disassembly and decompilation. Jakstab [41] focuses on accurate control flow reconstruction in the disassembly process. BAP [15] performs static disassembly of stripped binaries. Angr [54] includes symbolic execution and value-set analysis used especially for control flow reconstruction. IDA Pro [53] (used in DarkSea) demonstrated high accuracy and uses value-set-analysis. Hex-Rays Decompiler [3], Ghidra [9], and Snowman [25] further de-compile disassembled output to higher level representations such as LLVM IR or C code.

Verifying binaries. Some works focus on the low-level aspects of the binary and aim at precise de-compilation. Roessle et al. [52] de-compile x86-64 into a big step semantics. Earlier, others performed “decompilation-into-logic” (DiL) [47,48,49], translating assembly code into logic. While DiL provides a rich environment for precise reasoning about fine-grained instruction-level details, it incurs high complexity for reasoning about more coarse-grained properties such as reachability, termination, and temporal logic. In more recent work, Verbeek et al. [55] use the semantics of Roessle et al. [52] and describe techniques to decompile into re-compilable code.

Others focus on verifying the decompilation/lifting process itself. Dasgupta et al. [23] describe a translation validation on x86-64 instructions that employs their semantics for x86-64 (Dasgupta et al. [24]). Metere et al. [46] use HOL4 to verify a translation from ARMv8 to BAP. Hendrix et al. [37] discuss their ongoing work on verifying the translation performed by their lifting tool reopt. Numerous other works (e.g., Sail [11]) provide formal semantics of ISAs.
9 Conclusion

We have shown that a source-level translation to approximate bitvector operations leads to tools that are competitive to the state-of-the-art in reachability and termination of bitvector programs. We show that bitwise branching incurs negligible overhead, yet enables more programs to be verified. Notably, we showed that this approach leads to the first effective technique for verifying LTL of bitvector programs and, to our knowledge, the first technique for verifying reachability, termination and LTL of lifted binary programs.

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A Full Lifted Code for PotentialMinimizeSEVPABug (Sec. 2)

```c
//@ ltl invariant positive: ([] ( AP(x > 0) ===> <>AP(y==0)));
/*@*/
/* Provide Declarations */
#include <stdarg.h>
#include <setjmp.h>
#include <limits.h>
#include <stdint.h>
#include <math.h>

/*@ */
/* Global Declarations */

/*@ */
/* Types Declarations */
struct Istruct_A_type;
struct Istruct_O_type;
struct Istruct_f_type;
struct Istruct_union_OC_anon;
struct Istruct_struct_OC_ArchState;
struct Istruct_struct_OC_ArithFlags;
struct Istruct_union_OC_ArithFlagsSelector;
struct Istruct_struct_OC_AddressSpace;
struct Istruct_struct_OC_ArithFlags;
struct Istruct_union_OC_ArithFlags;
struct Istruct_union_OC_float80_t;
struct Istruct_union_OC_anon_OC_3;
struct Istruct_struct_OC_x87Stack;
struct Istruct_struct_OC_uint64_t;
struct Istruct_union_OC_vec64_t;
struct Istruct_union_OC_anon_OC_4;
struct Istruct_struct_OC_MMX;
struct Istruct_struct_OC_FPUStatusFlags;
struct Istruct_union_OC_FPUStackStatus;
struct Istruct_union_OC_FPUControlStatus;
struct Istruct_struct_OC_float80_t;
struct Istruct_union_OC_anon_OC_11;
struct Istruct_struct_OC_u8int;
struct Istruct_struct_OC_vec128_t;
struct Istruct_struct_OC_FpuFXSAVE;

/*@ */
/* Types Definitions */
struct Iarray_u6replace_u8int {
  int array[4];
};
struct Iarray_u4replace_u8int {
  int array[4];
};
struct Iarray_u8replace_u8int {
  int array[8];
};
struct Iarray_u8replace_u64int {
  int array[8];
}
```
struct l_struct struct OC_uint64v8_t {
    struct l_array 8 ureplace u64 int field0;
};

struct l_struct union OC_vec512_t {
    struct l_struct struct OC_uint64v8_t field0;
};

struct l_struct union OC_VectorReg {
    struct l_struct union OC_vec512_t field0;
};

struct l_array 32 struct AC l struct union OC_VectorReg {
    struct l_struct union OC_VectorReg array[32];
};

struct l_struct struct OC_ArithFlags {
    int field0;
    int field1;
    int field2;
    int field3;
    int field4;
    int field5;
    int field6;
    int field7;
    int field8;
    int field9;
    int field10;
    int field11;
    int field12;
    int field13;
    int field14;
    int field15;
};

struct l_struct union OC_SegmentSelector {
    short field0;
};

struct l_struct struct OC_Segments {
    short field0;
    short field1;
    short field2;
    short field3;
    short field4;
    short field5;
    short field6;
    short field7;
    short field8;
    short field9;
    short field10;
    short field11;
};

struct l_struct struct OC_Reg {
    struct l_struct union OC_anon field0;
};

struct l_struct struct OC_AddressSpace {
    int field0;
    int field1;
    int field2;
    int field3;
    int field4;
    int field5;
    int field6;
    int field7;
    int field8;
    int field9;
    int field10;
    int field11;
};

struct l_struct struct OC_GPR {
    int field0;
    int field1;
    int field2;
struct _struct_OC_Reg field3;
int field4;
struct _struct_OC_Reg field5;
int field6;
struct _struct_OC_Reg field7;
int field8;
struct _struct_OC_Reg field9;
int field10;
struct _struct_OC_Reg field11;
int field12;
struct _struct_OC_Reg field13;
int field14;
struct _struct_OC_Reg field15;
int field16;
struct _struct_OC_Reg field17;
int field18;
struct _struct_OC_Reg field19;
int field20;
struct _struct_OC_Reg field21;
int field22;
struct _struct_OC_Reg field23;
int field24;
struct _struct_OC_Reg field25;
int field26;
struct _struct_OC_Reg field27;
int field28;
struct _struct_OC_Reg field29;
int field30;
struct _struct_OC_Reg field31;
int field32;
struct _struct_OC_Reg field33;
};
struct _struct_OCanon_OC3 {
  int field0;
  int field1;
};
struct _array8_struct_OC_anon_OC3 {
  _struct_OCanon_OC3 array[8];
};
struct _struct_OCX87Stack {
  _array8_struct_OC_anon_OC3 field0;
};
struct _array1_uureplace_u64int {
  int array[1];
};
struct _struct_OC_uint64v1_t {
  _array1_uureplace_u64int field0;
};
struct _struct_union_OC_vec64_t {
  _struct_OC_uint64v1_t field0;
};
struct _struct_OCanon_OC4 {
  int field0;
  struct _struct_union_OC_vec64_t field1;
};
struct _array8_struct_AC_l_struct_OC_anon_OC4 {
  _struct_OC_anon_OC4 array[8];
};
struct _struct_OC_MMX {
  _array8_struct_AC_l_struct_OC_anon_OC4 field0;
};
struct _struct_OC_FPUStructFlags {
  int field0;
  int field1;
  int field2;
  int field3;
  int field4;
  int field5;
Bitwise Branching for Bitvector Programs (Extended)

202 int field6;
203 int field7;
204 int field8;
205 int field9;
206 int field10;
207 int field11;
208 int field12;
209 int field13;
210 int field14;
211 int field15;
212 int field16;
213 int field17;
214 int field18;
215 int field19;
216 struct _array_4_ureplace_u8int field20;
217);
218 struct lstruct_union_OC_FPUAbridgedTagWord {
219 int field0;
220};
221 struct lstruct_union_OC_FPUControlStatus {
222 int field0;
223};
224 struct _array_10_ureplace_u8int {
225 int array[10];
226};
227 struct lstruct_struct_OC_float80_t {
228 struct _array_10_ureplace_u8int field0;
229};
230 struct lstruct_union_OCanon_OC_l1 {
231 struct lstruct_struct_OC_float80_t field0;
232};
233 struct _array_6_ureplace_u8int {
234 int array[6];
235};
236 struct lstruct_struct_OC_FPUStackElem {
237 struct lstruct_union_OCanon_OC_l1 field0;
238 struct _array_6_ureplace_u8int field1;
239};
240 struct _array_8struct_ACstruct_struct_OC_FPUStackElem {
241 struct lstruct_struct_OC_FPUStackElem array[8];
242};
243 struct _array_96_ureplace_u8int {
244 int array[96];
245};
246 struct lstruct_struct_OC_SegmentShadow {
247 struct lstruct_union_OCanon field0;
248 int field1;
249 int field2;
250};
251 struct lstruct_struct_OC_SegmentCaches {
252 struct lstruct_struct_OC_SegmentShadow field0;
253 struct lstruct_struct_OC_SegmentShadow field1;
254 struct lstruct_struct_OC_SegmentShadow field2;
255 struct lstruct_struct_OC_SegmentShadow field3;
256 struct lstruct_struct_OC_SegmentShadow field4;
257 struct lstruct_struct_OC_SegmentShadow field5;
258};
259 struct lstruct_struct_OC_State {
260 struct lstruct_struct_OC_ArchState field0;
261 struct _array_32struct_AC_lstruct_union_OC_VectorReg field1;
262 struct lstruct_struct_OC_ArithFlags field2;
263 struct lstruct_union_OCanon field3;
264 struct lstruct_struct_OC_Segments field4;
265 struct lstruct_struct_OC_AddressSpace field5;
266 struct lstruct_struct_OC_GPR field6;
267 struct lstruct_struct_OC_X87Stack field7;
268 struct lstruct_struct_OC_MMX field8;
269 struct lstruct_struct_OC_FPUStatusFlags field9;
struct l struct union OC anon field10;
struct l struct struct OC SegmentCaches field12;
};

// External Global Variable Declarations */
extern struct l struct struct OC State* globalState;

// Function Declarations */
sub_401106 foo(struct l struct struct OC State* tmp14, int tmp15, void* tmp16);
void* sub_401106 VERIFIER nondet int(struct l struct struct OC State* tmp39, int tmp40, void* tmp41);
extern void _VERIFIER_nondet unsigned() __attribute__((__noreturn__));

// Global Variable Definitions and Initialization */
int x;
int y;
int STATE REG RAX ;

// LLVM Intrinsic Built-In Function Bodies */
static int llvm_add_u32(int a, int b) {
  int r = a + b;
  return r;
}
static int llvm_lshr_u32(int a, int b) {
  int r = a >> b;
  return r;
}
static int llvm_and_u8(int a, int b) {
  int r = a & b;
  return r;
}
static int llvm_xor_u8(int a, int b) {
  int r = a ^ b;
  return r;
}

// Function Bodies */
void* main(struct l struct struct OC State* tmp1, int tmp2, void* tmp3) {
  struct l struct struct OC State* tmp4;
  int* tmp5;
  int* tmp6;
  int* tmp7;
  int* tmp8;
  int* tmp9;
  void* tmp11;
  int tmp12;
  int tmp13;
  int tmp14;
  int tmp15;
  int tmp16;
  int tmp17;
  int tmp18;
  int _2e lessa3;
  int _2e lessa3 PHI TEMPORARY;
  int _2e lessa2;
  int _2e lessa2 PHI TEMPORARY;
  int _2e lessa1;
  int _2e lessa1 PHI TEMPORARY;
  int tmp19;
tmp_4 = globalState;
tmp_5 = (tmp_4->field2.field1);
tmp_6 = (tmp_4->field2.field3);
tmp_7 = (tmp_4->field2.field7);
tmp_8 = (tmp_4->field2.field9);
tmp_9 = (tmp_4->field2.field13);
tmp_10 = (tmp_4->field2.field5);
goto block_401119;
do {
    \* Syntactic loop 'block_401119' to make GCC happy */
block_401119:
    STATE_REG RAX = __VERIFIER_nondet_int();
tmp_11 = /* tail */ sub_401106__VERIFIER_nondet_int(/\*UNDEF*/
            struct struct struct OC_State*/eUNDEF*/;
            /\*UNDEF*/(0UL), tmp_3) :
tmp_12 = STATE_REG RAX;
x = tmp_12;
y = 1;
tmp_13 = tmp_12 >> 31;
if ((((((tmp_13 == 0u)&&1) & (((((tmp_12 == 0u)&&1)))&&1)) )
    } */
if ((((tmp_13 == 0u)&&1)) & (tmp_12 != 0u)&&1) {
    goto block_401135;
} else {
    2e_less1_PHI_TEMPORARY = tmp_12; /* for PHI node */
    2e_less2_PHI_TEMPORARY = ((((tmp_12 == 0u)&&1)); /* for PHI node */
    2e_less3_PHI_TEMPORARY = tmp_12; /* for PHI node */
    goto block_401163;
}
do {
    /* Syntactic loop 'block_401135' to make GCC happy */
block_401135:
tmp_14 = tmp_14_PHI_TEMPORARY;
tmp_15 = tmp_14 - 1;
tmp_16 = tmp_14 - 2;
tmp_17 = tmp_16 >> 31;
tmp_18 = tmp_15 >> 31;
if ((((((tmp_16 != 0u)&&1)) & (((((tmp_17 == 0u)&&1))) - ((((llvm_add_u32((tmp_17 + tmp_18)) == 2u)&&(1)))))&&1))
    } */
if ( (tmp_16 != 0u)&&1) & (tmp_17 == 0u) {
    goto block_401159_2e_backedge;
} else {
    goto block_40114f;
}
}
block_40114f:
y = 0;
goto block_401159_2e_backedge;
block_401159_2e_backedge:
if ((((((tmp_18 == 0u)&&1)) & (((((tmp_15 == 0u)&&1)))&&1))
    } */
if ((((((tmp_18 == 0u)&&1)) && (tmp_15 != 0u))&&1)) {
    tmp_14_PHI_TEMPORARY = tmp_15; /* for PHI node */
goto block_401135;
} else {
    goto block_401159_2e_block_401163_crit_edge;
} while (1); /* end of syntactic loop `block_401135` */
block_401159:
  x = tmp_15;
  \_2e\_lcssa3\_PHI\_TEMPORARY = tmp_15; /* for PHI node */
  \_2e\_lcssa2\_PHI\_TEMPORARY = (((tmp_15 == 0u)&1)); /* for PHI node */
  \_2e\_lcssa1\_PHI\_TEMPORARY = tmp_18; /* for PHI node */
goto block_401163;
block_401163:
  \_2e\_lcssa3 = \_2e\_lcssa3\_PHI\_TEMPORARY;
  \_2e\_lcssa2 = (((\_2e\_lcssa2\_PHI\_TEMPORARY)&1));
  \_2e\_lcssa1 = \_2e\_lcssa1\_PHI\_TEMPORARY;
  llvm_\_ctpop\_i32((\_2e\_lcssa3 & 255));
  *tmp_5 = 0;
  *tmp_6 = (((((int)tmp_19))& 1)); 1 ;
  *tmp_7 = ((( (int)\_2e\_lcssa2));
  *tmp_8 = ((( (int)\_2e\_lcssa1));
  *tmp_9 = 0;
  *tmp_10 = 0;
goto block_401119;
} while (1); /* end of syntactic loop `block_401119` */
B  Bitwise Branching Rules with Labels

The rules from Section 4 are reproduced here, now with labels.

\[ e_1 = 0 \Rightarrow e_1 \land e_2 \Rightarrow 0 \]
\[ (e_1 = 0 \lor e_1 = 1) \land (e_2 = 0 \lor e_2 = 1) \Rightarrow e_1 \land e_2 \Rightarrow e_1 \lor e_2 \]
\[ e_1 \geq 0 \land e_2 \geq 0 \Rightarrow r \oplus e_1 \land r \oplus e_2 \]
\[ e_1 \leq 0 \land e_2 \leq 0 \Rightarrow r \ominus e_1 \land r \ominus e_2 \]

C  Bitwise Branching Algorithm

```
1 type rule_exp = (exp -> exp -> exp) * (exp -> exp -> exp)
2 let rec T_E (e:exp) : exp = s
3 match e with
4 | BinOp(\(\oplus\), e1, e2) -> s
5 | e1' = T_E e1 in
6 | e2' = T_E e2 in
7 let rules = Rules.find_exp(\(\oplus\)) in
8 fold_left (fun acc (cond, repl) -> ITE(cond e1' e2', repl e1' e2', acc)
9 | (BinOp(\(\ominus\), e1, e2)) rules
10 | _ -> e
```

```
1 type rule_stmt = (exp -> exp -> exp) * (lhs -> exp -> exp)
2 let rec T_S (s:stmt) : stmt = t
3 match s with
4 | Assign(lhs, BinOp(\(\oplus\), e1, e2)) ->
5 | let e1' = T_E e1 in
6 | let e2' = T_E e2 in
7 let rules = Rules.find_stmt(\(\oplus\)) in
8 fold_left (fun acc (cond, repl) -> IfElseStmt(cond e1' e2', repl lhs e1' e2', acc)
9 | (Assign(1, BinOp(\(\ominus\), e1, e2)) rules
10 | _ -> s
```
from z3 import *

def prove(r, f):
    s = Solver()
    s.add(Not(f))
    if s.check() == unsat:
        print("proved rule: " + r)
    else:
        print("failed to prove rule: " + r)
        print(s.model())

def vec2bool(v):
    if v != 0:
        return True
    else:
        return False

def bool2vec(b):
    if (b==True):
        return BitVecVal (1 , 1)
    else:
        return BitVecVal (0 , 1)

# prove RS-POS rule
rule_1 = "RS-POS: check((n>>31)==0) <====> n==0"
A_1 = (n>>31)==0
B_1 = (n==0)
constraints_1=And (Implies (A_1 , B_1) , Implies (B_1 , A_1))
prove (rule_1, constraints_1)

# prove RS-NEG rule
# 32 bit 2's complement
rule_2 = "RS-NEG: check((n>>31)==-1) <====> n<0"
A_2 = (n>>31)==-1
B_2 = (n<0)
constraints_2=And (Implies (A_2 , B_2) , Implies (B_2 , A_2))
prove (rule_2, constraints_2)

# prove AND-1 rule
rule_3="AND-1: check(n&1) <====> n"
A_3 = (n&1)==n
B_3 = Or (n==0, n==1)
constraints_3=And (Implies (A_3 , B_3) , Implies (B_3 , A_3))
prove (rule_3, constraints_3)

# prove AND-0 rule
rule_4 = "AND-0: check(n&0) <====> 0"
A_4 = ((n&0)==0)
prove (rule_4, A_4)

# print("AND-0 rule: check(n&0)==0," + str(s4.check ()))

# prove XOR-0 rule
rule_5="XOR-0: check(n^0) <====> n"
A_5 = ((n^0)==n)
prove (rule_5, A_5)

# prove XOR-EQ rule
rule_6="XOR-EQ: check(n=1 or 0, e = 1 or 0, n==e ) ==0 "
n_6_1 = ((n==0) & (e==1)) == 0
A_6_1 = BitVecs (n_6_1 , e_6_1) == 0
B_6_1 = And (Or(n_6_1 ==1, n_6_1 == 0) , Or(e_6_1 ==1, e_6_1 == 0) , n_6_1 == e_6_1)
prove (rule_6, A_6_1)
# prove XOR rule

## rule 6.2

\[
A_{6.2} = "XOR-NEQ: check(n=1 or 0, e = 1 or 0, n!=e) \implies 1"
\]

\[
B_{6.2} = \text{And}(\text{Or}(n_{6.2} = 1, \ n_{6.2} = 0), \ \text{Or}(e_{6.2} = 1, \ e_{6.2} = 0)), \ \text{Or}(n_{6.2} = e_{6.2})
\]

\[
\text{prove}(\text{rule } 6.2, \implies (B_{6.2}, \ A_{6.2}))
\]

### rule 7

\[
\text{rule } 7 = "\text{NOT-SWITCH}: check(\neg (n=b) \iff n\neq b)"
\]

\[
\text{B}_7 = \text{BitVec}(\it{n}_7, 32)
\]

\[
\text{A}_7 = (\text{Not}(\it{n}_7=\it{b}))
\]

\[
\text{B}_7 = \text{And}(\text{Implies}(\text{A}_7, \ \text{B}_7))
\]

### rule 8

\[
\text{rule } 8 = "\text{OR-1 rule } \ n_1 \iff 1"
\]

\[
\text{n}_8 = \text{BitVec}(\it{n}_8, 32)
\]

\[
\text{A}_8 = (\{\it{n}_8[1]=1\})
\]

\[
\text{B}_8 = \text{Or}(\it{n}_8 ==1, \ \it{n}_8==0)
\]

\[
\text{prove}(\text{rule } 8, \And(\text{Implies}(\text{B}_8, \ \text{A}_8), \ \text{Implies}(\text{A}_8, \ \text{B}_8)))
\]

### rule 9

\[
\text{rule } 9 = "\text{OR-0 rule } \ n_0 \iff \text{n }"
\]

\[
\text{n}_9 = \text{BitVec}(\it{n}_9, 32)
\]

\[
\text{A}_9 = (\{\it{n}_9[0]==\it{n}_9\})
\]

\[
\text{prove}(\text{rule } 9, \ \text{A}_9)
\]

### rule 10

\[
\text{rule } 10 = "\text{BOOL-TRUE rule } \ n!=0 \implies \text{True}"
\]

\[
\text{n}_10 = \text{BitVec}(\it{n}_10, 32)
\]

\[
\text{A}_{10} = \text{Implies}(\text{n}_10!=0, \text{True})
\]

\[
\text{prove}(\text{rule } 10, \ \text{A}_{10})
\]

## General rules & operators are mutual exclusive negative

### rule and xneg

\[
\text{rule and xneg } = "\text{r=acb exclusive negative: } r = \text{acb}, \ a>0, \ b<0 \implies r<=-a, \ r>=-b"
\]

\[
\text{and a3, and b3, and r3= BitVecs('\text{and a3 and b3 and r3'}, 32)}
\]

\[
\text{constr and xneg } = \text{Implies}(\text{And}(\text{and a3} >0, \ \text{and b3}<0, \ \text{and r3}=(\text{and a3 } \ \text{and b3}), \ \text{And}(\text{and r3} !=\text{and a3}, \ \text{and r3}>=0))
\]

\[
\text{prove}(\text{rule and xneg, constr and xneg})
\]

## General rules & both operators are non-negative

### rule and d4

\[
\text{rule and d4 } = "r<\text{acb} \text{ less than: } r < \text{acb}, \ a>0, \ b>0 \implies r<\text{a}, \ r<\text{b}"
\]

\[
\text{and a4, and b4, and r4= BitVecs('\text{and a4 and b4 and r4'}, 32)}
\]

\[
\text{constr and d4 } = \text{Implies}(\text{And}(\text{and a4} >0, \ \text{and b4} >= 0, \ \text{and r4} <= (\text{and a4 } \ \text{and b4})), \ \text{And}(\text{and r4} <\text{and a4}, \ \text{and r4} <\text{and b4}))
\]

\[
\text{prove}(\text{rule and d4, constr and d4})
\]

## General rules & both operators are negative

### rule and neg5

\[
\text{rule and neg5 } = "\text{r=acb both negative: } r < \text{acb}, \ a<0, \ b<0 \implies r<\text{-a}, \ r<\text{-b, } r<0"
\]

\[
\text{and a5, and b5, and r5= BitVecs('\text{and a5 and b5 and r5'}, 32)}
\]

\[
\text{constr and neg5 } = \text{Implies}(\text{And}(\text{and a5} < 0, \ \text{and b5}<0, \ \text{and r5}=(\text{and a5 } \ \text{and b5})), \ \text{And}(\text{and r5} < \text{and a5}, \ \text{and r5} > \text{and b5}, \ \text{and r5} < 0))
\]

\[
\text{prove}(\text{rule and neg5, constr and neg5})
\]

## And logic rules & both operators are one bit size

### rule and neg6

\[
\text{rule and neg6 } = "\text{acb both one bit: a<cb } \Rightarrow \text{acb}"
\]

\[
\text{and a6, and b6 = BitVecs('\text{and a6 and b6'}, 1)}
\]

\[
\text{constr and neg6 } = \text{Implies}((\text{and a6} \text{ and b6})==1, \ \text{And}(\text{and a6} ==1, \ \text{and b6} ==1))
\]

\[
\text{prove}(\text{rule and neg6, constr and neg6})
\]

## General rules or, both operators are non-negative

### rule or

\[
\text{rule or } = "r=a \text{ or general: } r := a|b, \ a>=0, \ b>=0 \iff r>=a, \ r>=b"
\]
or\_a1, or\_b1, or\_r1 = BitVecs('or\_a1 or\_b1 or\_r1', 32)
constr\_or = Implies(And(or\_a1 >= 0, or\_b1>=0, or\_r1)=(or\_a1|or\_b1)), And(
or\_a1 >= or\_a1, or\_a1 >= or\_b1))
prove(rule\_or, constr\_or)

# General rules or, both operators are negative (two's complement)
rule\_or\_neg = "r=a\_b genral both negative: r = a\_b, a<0, b<0 \Rightarrow r>=a, r
>=b" or\_a2, or\_b2, or\_r2 = BitVecs('or\_a2 or\_b2 or\_r2', 32)
constr\_or\_neg = Implies(And(or\_a2 < 0, or\_b2 < 0, or\_r2=(or\_a2|or\_b2)), And(or\_a2 >= or\_a2, or\_r2 >= or\_b2, or\_r2<0))
prove(rule\_or\_neg, constr\_or\_neg)

# General rules or, both operators are mutual exclusive negative (two's complement)
rule\_or\_log = "a\_b 0 to logic: (a\_b) 0 \Rightarrow a==0 & & b==0 \Rightarrow r>=a, r
>=b" or\_a4, or\_b4 = BitVecs('or\_a4 or\_b4', 1)
constr\_or\_log = Implies((or\_a4|or\_b4 = 0), And(or\_a4==0,or\_b4 = 0))
prove(rule\_or\_log, constr\_or\_log)

# General rules xor, both operators are non-negative
rule\_xor\_neg = "r=a\_b genral, both non-negative: r = a\_b, a<0, b<0 \Rightarrow r
>=0" xor\_a, xor\_b, xor\_r = BitVecs('xor\_a xor\_b xor\_r', 32)
constr\_xor\_neg = Implies(And(xor\_a >= 0, xor\_b>=0, xor\_r:=(xor\_a xor\_b)), And(xor\_r >= 0))
prove(rule\_xor, constr\_xor)

# General rules xor, both operators are negative (two's complement)
rule\_xor\_neg = "r=a\_b genral both negative: r = a\_b, a<0, b<0 \Rightarrow r<0" xor\_a1, xor\_b1, xor\_r1 = BitVecs('xor\_a1 xor\_b1 xor\_r1', 32)
constr\_xor\_neg = Implies(And(xor\_a1 < 0, xor\_b1 < 0, xor\_r1=(xor\_a1 xor\_b1)), And(xor\_r1>=0))
prove(rule\_xor\_neg, constr\_xor\_neg)

# General rules xor, operators are mutual exclusive non-negative (two's complement)
rule\_xor\_xneg = "r<=a\_b genral mutual exclusive non-negative: r <= a\_b, a<0, b<0 \Rightarrow r<0" xor\_a2, xor\_b2, xor\_r2 = BitVecs('xor\_a2 xor\_b2 xor\_r2', 32)
constr\_xor\_xneg = Implies(And(xor\_a2 < 0, xor\_b2 >= 0, xor\_r2:=(xor\_a2 xor\_b2)), And(xor\_r2<0))
prove(rule\_xor\_xneg, constr\_xor\_xneg)

# xor to logic rule, operators are one bit
rule\_xor\_log = "a\_b one bit \Rightarrow (a==0 & & b==1 a==1 & & b==0)" xor\_a3, xor\_b3 = BitVecs('xor\_a3 xor\_b3', 1)
constr\_xor\_log = Implies(1=(xor\_a3 xor\_b3), Or(And(xor\_a3==0, xor\_b3
==1), And(xor\_a3==1,xor\_b3 ==0)))
prove(rule\_xor\_log, constr\_xor\_log)

# General rules complement
rule\_com = "CPL-POS k CPL-NEG. = "a genral"
com\_a, com\_b = BitVecs('com\_a com\_b', 32)
constr\_com\_1 = Implies(And(com\_a >= 0, com\_r:="com\_a"), com\_r >=0)
constr\_com\_2 = Implies(And(com\_a < 0, com\_r:="com\_a"), com\_r>=0)
constr\_com = And(constr\_com\_1, constr\_com\_2)
prove(rule\_com, constr\_com)
### E Detailed Results for Termination and LTL

Table 4 shows the details running results of 26 bithacks benchmarks on LTL verification task, Table 5 and Table 6 show the details of LTL and Termination running results on our hand-crafted benchmarks, table 7 shows the details of termination running results on 18 bitwise benchmarks from APROVE, they are corresponding to section 6.

| Benchmark              | Property                                      | Expected | Ultimate Time | Ultimate Result | DarkSea Time | DarkSea Result |
|------------------------|-----------------------------------------------|----------|---------------|-----------------|--------------|----------------|
| counting-bits-BK1false.c | □(y >= 0)                                     | ✔️       | 8.80s         | ✔️              | 10.75s       | ✗              |
| consecutive-zero-bits-trailingfalse.c | y = 1                                      | ✗️       | 5.91s         | ✔️              | 7.24s        | ?              |
| counting-bits-BKfalse.c    | □(y <= 1)                                     | ✗️       | 6.93s         | ✔️              | 8.15s        | ✗              |
| display-bitfalse.c         | y > 1                                         | ✗️       | 24.55s        | ✔️              | 59.18s       | ✗              |
| parityfalse.c              | y >= 1                                        | ✗️       | 23.81s        | ✔️              | 9.09s        | ✗              |
| display-bitfalse.c         | y < 0                                         | ✗️       | 27.20s        | ✗              | 64.63s       | ✗              |
| counting-bits-setfalse.c   | y >= 1                                        | ✗️       | 8.88s         | ✔️              | 7.77s        | ✗              |
| reverse-bits1false.c       | n < 0                                         | ✗️       | 8.11s         | ✔️              | 10.21s       | ✗              |
| logbase2.c                 | y >= 1                                        | ✔️       | 7.60s         | ✔️              | 7.49s        | ✔️              |
| base64.ltl.c                | □(\text{start} = 1)                          | ✔️       | 124.37s       | ✔️              | 602.61s      | M              |
| modulus-division.c         | y > 1                                         | ✔️       | 6.67s         | ✔️              | 17.25s       | ✗              |
| consecutive-zero-bits-trailing.c | y >= 1                                     | ✔️       | 6.07s         | ✔️              | 7.51s        | ✔️              |
| interleave-bits.c          | y >= 1                                        | ✔️       | 11.40s        | ✔️              | 300.66s      | ✗              |
| logbase2-N-bit1.c          | y >= 1                                        | ✔️       | 12.39s        | ✔️              | 547.43s      | M              |
| reverse-N-bit.c            | n > 1                                         | ✔️       | 6.91s         | ✔️              | 13.09s       | ✔️              |
| counting-bits-set.c        | y >= 1                                        | ✔️       | 9.23s         | ✔️              | 8.52s        | ✔️              |
| consecutive-zero-bits.c    | y >= 1                                        | ✔️       | 5.29s         | ✔️              | 5.85s        | ✔️              |
| counting-bits-BK.c         | □(y <= 1)                                     | ✔️       | 6.63s         | ✔️              | 8.46s        | ✔️              |
| dropbf.ltl.c                | □(A! = 1 ∨ RELEASE = 0)                      | ✔️       | 8.42s         | ✔️              | 13.47s       | ✔️              |
| reverse-bits.c             | y >= 1                                        | ✔️       | 7.21s         | ✔️              | 10.81s       | ✗              |
| counting-bits-lookup.c     | y >= 1                                        | ✔️       | 900.41s       | ✔️              | 900.41s      | ✔️              |
| display-bit.c              | y >= 32                                       | ✔️       | 24.99s        | ✔️              | 705.44s      | M              |
| counting-bits-BK1.c        | □(y >= 0)                                     | ✔️       | 7.51s         | ✔️              | 8.59s        | ✔️              |
| display-bit1.c             | n < 0                                         | ✔️       | 20.46s        | ✔️              | 7.29s        | ✗              |
| reverse-bits1.c            | n > 1                                         | ✔️       | 6.33s         | ✔️              | 12.55s       | ✔️              |
| parity.c                   | y >= 1                                        | ✔️       | 19.67s        | ✔️              | 6.93s        | ✔️              |
Table 5: Details for LTLBitBench.

| Benchmark       | Property | Expected | Ultimate Time | DarkSea Time |
|-----------------|----------|----------|---------------|--------------|
| and.guard2.false.c | \(z \geq 100\) | ✗ | 7.54s | 7.65s | ✗ |
| xor.stem1.false.c | \(n < 0\) | ✗ | 5.78s | 6.41s | ✗ |
| and.guard2.false.c | \(y > 0\) | ✗ | 7.11s | 5.52s | ✗ |
| xor.stem.false.c | \(n < 0\) | ✗ | 6.34s | 5.86s | ✗ |
| xor.guard.false.c | \(n > 0\) | ✗ | 6.40s | 6.24s | ✗ |
| or.loop1.false.c | \(\Diamond (\n < 0)\) | ✗ | 6.98s | 6.76s | ✗ |
| and.guard.false.c | \(n < 0\) | ✗ | 6.34s | 5.81s | ✗ |
| xor.stem.false.c | \(n < 0\) | ✗ | 5.67s | 6.33s | ✗ |
| xor.guard.false.c | \(n > 0\) | ✗ | 5.82s | 5.96s | ✗ |
| and.guard1.false.c | \(n > 0\) | ✗ | 7.82s | 6.04s | ✗ |
| com.loop.false.c | \(y < 0\) | ✗ | 5.70s | 6.81s | ✗ |
| or.stem.false.c | \(n < 0\) | ✗ | 7.11s | 5.81s | ✗ |
| and.guard4.false.c | \(n > 0\) | ✗ | 8.62s | 5.55s | ✗ |
| and.stem2.false.c | \(n > 0\) | ✗ | 7.69s | 6.35s | ✗ |
| or.loop2.false.c | \(n > 0\) | ✗ | 6.47s | 8.89s | ✗ |
| and.loop1.false.c | \(z < 0\) | ✔ | 9.22s | 7.60s | ✔ |
| com.stem.false.c | \(\Box (y < 0)\) | ✔ | 8.89s | 9.52s | ✔ |
| or.loop.false.c | \(\Diamond (\n < 0)\) | ✔ | 7.60s | 7.82s | ✔ |
| and.stem2.c | \(n > 0\) | ✔ | 5.81s | 5.36s | ✔ |
| xor.stem1.c | \(n < 0\) | ✔ | 7.05s | 5.76s | ✔ |
| xor.guard.c | \(n < 0\) | ✔ | 6.41s | 5.67s | ✔ |
| and.guard4.c | \(n > 0\) | ✔ | 10.25s | 6.00s | ✔ |
| or.stem.c | \(n < 0\) | ✔ | 5.38s | 7.38s | ✔ |
| com.stem.c | \(\Box (y = 1)\) | ✔ | 6.50s | 5.59s | ✔ |
| xor.stem.c | \(n < 0\) | ✔ | 5.40s | 5.41s | ✔ |
| xor.loop.c | \(n < 0\) | ✔ | 6.14s | 7.97s | ✔ |
| and.stem1.c | \(n < 0\) | ✔ | 7.05s | 5.32s | ✔ |
| and.guard.c | \(n < 0\) | ✔ | 6.43s | 901.21s | ✗ |
| and.loop1.c | \(z < 0\) | ✔ | 7.63s | 5.46s | ✔ |
| com.loop.c | \(y < 0\) | ✔ | 6.44s | 5.39s | ✔ |
| or.loop.c | \(\Box (\n < 0)\) | ✔ | 7.55s | 10.05s | ✔ |
| and.guard2.c | \(z \geq 100\) | ✔ | 9.58s | 17.04s | ✔ |
| or.loop2.c | \(n < 0\) | ✔ | 6.17s | 6.33s | ✔ |
| and.stem.c | \(n < 0\) | ✔ | 5.49s | 5.57s | ✔ |
| or.ZERO.int.c | \(p = 1\) | ✔ | 67.11s | 9.38s | ✔ |
| and.loop.c | \(y \geq 1\) | ✔ | 6.15s | 5.92s | ✔ |
| and.guard1.c | \(n > 0\) | ✔ | 7.81s | 8.04s | ✔ |
| or.loop1.c | \(\Diamond (\n < 0)\) | ✔ | 8.44s | 6.58s | ✔ |
| or.loop3.c | \(\Diamond (\n < 0)\) | ✔ | 7.47s | 6.11s | ✔ |
| or.guard.c | \(n < 0\) | ✔ | 5.92s | 4.52s | ✔ |
Table 6: Details for TermBitBench.

| Benchmark                  | Expected | AProVE | CPAchecker | KITTEL | 2LS | ULTIMATE | DARKSEA |
|----------------------------|----------|--------|------------|--------|-----|----------|---------|
|                            |          | Time   | Result     | Time   | Result | Time     | Result  |
| xor-01-false.c             | ?        | 18.41s | ✔          | 900.24s | T    | 900.53s  | T       |
| xor-04-false.c             | ✗        | 185.04s | ✗          | 900.24s | T    | 900.15s  | ✗       |
| not-04-false.c             | ✗        | 4.18s  | ?          | 900.24s | T    | 900.14s  | ✗       |
| not-05-false.c             | ✗        | 3.03s  | ✗          | 900.24s | T    | 900.13s  | ✗       |
| and-05-false.c             | ✗        | 10.11s | ✗          | 900.24s | T    | 900.16s  | ✗       |
| or-02-false.c              | ✗        | 4.83s  | ✗          | 900.24s | T    | 900.16s  | ✗       |
| not-03-false.c             | ✗        | 2.95s  | ✗          | 900.24s | T    | 900.16s  | ✗       |
| and-03-false.c             | ✗        | 4.65s  | ✗          | 900.24s | T    | 900.18s  | ✗       |
| not-02-false.c             | ✗        | 1.90s  | ✗          | 900.24s | T    | 900.18s  | ✗       |
| and-05-false.c             | ✗        | 6.29s  | ✗          | 900.24s | T    | 900.18s  | ✗       |
| or-01-false.c              | ✗        | 5.76s  | ✗          | 900.24s | T    | 900.18s  | ✗       |
| and-02-false.c             | ✗        | 6.30s  | ✗          | 900.24s | T    | 900.18s  | ✗       |
| not-01.c                   | T         | 902.06s | ✔          | 900.24s | T    | 900.18s  | ✔       |
| and-02.c                   | T         | 901.23s | ✔          | 900.24s | T    | 900.18s  | ✔       |
| or-01.c                    | T         | 23.72s | ✔          | 900.24s | T    | 900.18s  | ✔       |
| xor-01.c                   | T         | 4.14s  | ✔          | 900.24s | T    | 900.18s  | ✔       |
| and-03.c                   | T         | 12.83s | ✔          | 900.24s | T    | 900.18s  | ✔       |
| not-02.c                   | T         | 3.11s  | ✔          | 900.24s | T    | 900.18s  | ✔       |
| and-01.c                   | T         | 5.74s  | ✔          | 900.24s | T    | 900.18s  | ✔       |
| or-02.c                    | T         | 10.16s | ✔          | 900.24s | T    | 900.18s  | ✔       |
| or-03.c                    | T         | 5.27s  | ✔          | 900.24s | T    | 900.18s  | ✔       |
| not-03.c                   | T         | 3.95s  | ✔          | 900.24s | T    | 900.18s  | ✔       |
| and-04.c                   | T         | 901.56s | ✔          | 900.24s | T    | 900.18s  | ✔       |
| or-06.c                    | T         | 7.48s  | ✔          | 900.24s | T    | 900.18s  | ✔       |
| and-05.c                   | T         | 4.40s  | ✔          | 900.24s | T    | 900.18s  | ✔       |
| or-04.c                    | T         | 2.39s  | ✔          | 900.24s | T    | 900.18s  | ✔       |
| or-05.c                    | T         | 17.17s | ✔          | 900.24s | T    | 900.18s  | ✔       |
| and-06.c                   | T         | 10.12s | ✔          | 900.24s | T    | 900.18s  | ✔       |
| not-05.c                   | T         | 3.21s  | ✔          | 900.24s | T    | 900.18s  | ✔       |

Table 7: Details for AProVE termination benchmarks.

| Benchmark                  | Expected | AProVE | CPAchecker | KITTEL | 2LS | ULTIMATE | DARKSEA |
|----------------------------|----------|--------|------------|--------|-----|----------|---------|
|                            |          | Time   | Result     | Time   | Result | Time     | Result  |
| sigred/xor-01-overflow/spec2.c | ✔        | 2.03s  | ✗          | 900.24s | T    | 900.17s  | ✗       |
| sigred/xor-02-overflow/common.c | ✔        | 2.12s  | ✗          | 900.24s | T    | 900.17s  | ✗       |
| sigred/pagination-paper/a  | ✔        | 2.37s  | ✗          | 900.24s | T    | 900.17s  | ✗       |
| sigred/pagination-paper/b  | ✔        | 2.09s  | ✗          | 900.24s | T    | 900.17s  | ✗       |
| sigred/pagination-paper/c  | ✔        | 4.30s  | ✗          | 900.24s | T    | 900.17s  | ✗       |
| sigred/pagination-paper/d  | ✔        | 3.90s  | ✗          | 900.24s | T    | 900.17s  | ✗       |
| sigred/pagination-paper/e  | ✔        | 5.60s  | ✗          | 900.24s | T    | 900.17s  | ✗       |
| sigred/pagination-paper/f  | ✔        | 6.71s  | ✗          | 900.24s | T    | 900.17s  | ✗       |
| sigred/pagination-paper/g  | ✔        | 4.18s  | ✗          | 900.24s | T    | 900.17s  | ✗       |
| sigred/pagination-paper/h  | ✔        | 5.56s  | ✗          | 900.24s | T    | 900.17s  | ✗       |
| sigred/pagination-paper/i  | ✔        | 2.39s  | ✗          | 900.24s | T    | 900.17s  | ✗       |
| sigred/pagination-paper/j  | ✔        | 3.82s  | ✗          | 900.24s | T    | 900.17s  | ✗       |
| sigred/pagination-paper/k  | ✔        | 900.26s | ✔          | 900.24s | T    | 900.17s  | ✔       |
| sigred/pagination-paper/l  | ✔        | 2.33s  | ✗          | 900.24s | T    | 900.17s  | ✗       |
F  Bug in GCC

Example 1 (A reported bug in gcc [7]).

```c
static uint64_t div(uint64_t ui1, uint64_t ui2){
    return (ui2 == 0) ? ui1 : (ui1 / ui2); }
static int8_t mod(int8_t si1, int8_t si2){
    return (si2==0) || ((si1==128) && (si2==-1)) ? si1 : (si1 % si2); }
static int32_t g_5 = 0, g_11 = 0;
int main (){
    uint64_t l_7 = 0x509CB0BEFCDF11BBLL;
    g_11 ^= l_7 && ((div((mod(g_5, 0)), -1L)) != 1L);
    if (!g_11) return __VERIFIER_error();
    return 0;
}
```

From the source semantics of this example, variable \texttt{g\_11} would have value 1 at Line 9 and \texttt{VERIFIER\_error} is un-reachable. However, a defect [2] in gcc folds \((\text{div}((\text{mod}(\text{g\_5}, 0)), -1L)) \neq 1L\) to 0. This makes \texttt{g\_11} become 0 at Line 9, introducing a new error behavior.

G  \texttt{DarkSea} translations through an example lifted binary

We here explain via an example the need for the translations perform by DarkSea, discussed in Sec. 7. Figure 4 shows an (condensed) example of the result of lifting a GCC-compiled binary version of \texttt{PotentialMinimizeSEVPABug.c} (using McSema). In the following, we describe how decompilation tools (e.g., McSema) target re-compilation and the challenges this poses for existing verification techniques and tools. We then describe translations performed by DarkSea to make lifted binaries more amenable to verification. As discussed in Sec. 7, the translations below were implemented as passes on the lifted LLVM IR.

Run-time environment. Binary lifting de-compiles into a program that mimics the binary behavior. To ensure that a new re-compiled binary would run correctly, lifting yields code that switches the contexts between the run-time environments and the simulated code, somewhat akin to how a loader first moves environment variables onto the stack. This context-switch code wraps around the simulated program and is indispensable for execution of re-compiled code. Context-switch code can be fairly complex. For example, it frequently uses assembly code to move values between the physical environment (e.g., environment variables like \texttt{PATH}) and the simulated constructs (e.g., registers and the stack). The initial state of the registers is also loaded from the runtime, as seen by the instructions in callout 1 in Fig. 4. Tracing back the origins of these values, which stem from the runtime code, poses a nearly impossible, yet unnecessary task for verification tools. For most verification tasks, it does not matter where the initial
Fig. 4: Challenges involved in reasoning about the lifted binary of PotentialMinimizeSEVPABug.c.
values of registers or environment variables such as \$PATH come from; we can just treat them as nondeterministic input values on the stack.

**Translation: Removing verification-unrelated code and data.** We implemented a pass to analyze lifted output and decouple context-switch code from the code that simulates the original program. We first locate the original main function in the simulated code and then follow the control flow to statically extract and trim code that can reach main. Further, the context-switch code also includes program-dependent functions that are registered to be executed before the main or after the exit. To avoid missing such functions in verification, we allocate calls to them at the begin or the end of the main function, following the order these functions are registered to run in the original binary.

**Passing emulation state through procedures.** Binary lifting for recompilation generates programs in which function calls are used to pass emulation state. This can be seen, for example, in callout 2 in Fig. 4 where struct.State is passed as the first argument to sub_401111_main. These arguments are not part of the original program. Rather, lifting introduces these additional arguments to simulate the possibility of context-switches within function calls. Further, when the lifted code is recompiled, code simulating the callee can access the contexts through these struct.State arguments, which is typically more efficient than directly accessing the global data structure. Interprocedural reasoning is known to make verification more challenging and requires more sophisticated algorithms such as procedure summaries \[57,20\] and nested interpolants \[34\], especially when context sensitivity is required. When machine emulation involves expanding use of arguments, we found this complicates analysis and hampers verification.

**Translation: Simplifying function arguments.** Adding arguments to user procedures (as done by McSema) complicates verification. Fortunately, a translation is possible: the arguments in a McSema-generated function point to the same global data structure. As such, we eliminate these arguments from every function call. We then create a pointer pointing to the global data struct and replace all uses of the first argument in the function body with uses of our new pointer.

**Nested structures for emulation.** Lifted binaries encode complicated structures that simulate hardware features such as registers, arithmetic flags, FPU status flags, the stack, and instruction pointers. These are represented as nested structures, e.g., state->general_registers.register13.union.uint64cell. This can be seen, for example, in callout 3 in Fig. 4 where the field tmp__1->field6.field13.field0.field0 is accessed. The use of nesting in these structures provides efficiency: constructs that are commonly used together (e.g., general purpose registers) can be artificially grouped to the same cache line, avoiding cache evictions. However, reasoning about these nested data-structures is difficult because verification tools cannot make any assumptions about where these data-structures come from, how they are used and, most importantly, how they may be aliased. Consequently, verification tools have to carefully track heap references to infer non-aliasing, even though the lifting process ensures that they will not.
Translation: Flattening the emulation state. Many of the data structures for the emulated state are functionally independent and hence the complex nesting is not necessary to maintain the original semantics. We implemented a pass to flatten the data structures. We create individual variables for all the innermost and separable fields. We then translate accesses to these nested structures, with use-define reasoning to identify all the accesses to a flattened field. For the aforementioned `state->general_registers.register13.union.uint64cell`, we allocate a new global variable `register13` with the same type of `uint64cell` and re-locate all the original accesses to `register13`.

H Detailed Results for DARKSEA Translation

Table 8 and Table 9 show the details of applying termination verifiers to MC-Sema output and the output after DARKSEA’s translations, respectively.

| Benchmark | Expected | AProVE | CPAchecker | KITTeL | 2LS | ULTIMATE | DARKSEA |
|-----------|----------|-------|-------------|--------|-----|----------|---------|
|            | Time     | Time   | Time        | Time   | Time| Time     | Time    |
| Singapore-2_gccO0.mcsema.cbe.c | 8.28s | 2.04s | 0.06s | 0.17s | 900.43s | T | 900.36s |
| aaron2_gccO0.mcsema.cbe.c | 5.48s | 2.13s | 0.06s | 0.17s | 900.45s | T | 900.43s |
| Singapore_gccO0.mcsema.cbe.c | 4.13s | 2.06s | 0.06s | 0.17s | 900.35s | T | 900.39s |
| Mysore_gccO0.mcsema.cbe.c | 3.77s | 1.98s | 0.05s | 0.16s | 900.35s | T | 900.35s |
| Parallel_gccO0.mcsema.cbe.c | 3.01s | 2.12s | 0.06s | 0.15s | 900.36s | T | 900.36s |
| Pure2Phase-1_gccO0.mcsema.cbe.c | 8.61s | 2.56s | 0.05s | 0.16s | 900.38s | T | 900.41s |
| Thun-1_gccO0.mcsema.cbe.c | 3.55s | 2.41s | 0.05s | 0.15s | 900.44s | T | 900.42s |
| easy2_gccO0.mcsema.cbe.c | 2.72s | 2.22s | 0.05s | 0.16s | 589.64s | M | 765.56s |
| aaron3_gccO0.mcsema.cbe.c | 9.82s | 2.44s | 0.06s | 0.20s | 900.41s | T | 900.47s |
| Pure3Phase-2_gccO0.mcsema.cbe.c | 5.85s | 2.54s | 0.06s | 0.22s | 900.48s | T | 900.43s |
| easy2debug_gccO0.mcsema.cbe.c | 3.65s | 2.28s | 0.06s | 0.19s | 900.48s | T | 902.27s |
| Mysore_gccO0.mcsema.cbe.c | 7.78s | 2.03s | 0.06s | 0.17s | 900.49s | T | 900.49s |
| easy1_gccO0.mcsema.cbe.c | 2.92s | 2.24s | 0.05s | 0.16s | 785.05s | M | 802.15s |
| aaron2_gccO0.mcsema.cbe.c | 9.27s | 2.15s | 0.05s | 0.16s | 900.35s | T | 900.37s |
| easy1_gccO0.mcsema.cbe.c | 2.68s | 1.83s | 0.02s | 0.11s | 566.99s | M | 879.64s |
| Thun-2_gccO0.mcsema.cbe.c | 5.91s | 2.41s | 0.03s | 0.16s | 900.36s | T | 900.45s |
| Pure2Phase-2_gccO0.mcsema.cbe.c | 4.57s | 1.90s | 0.02s | 0.13s | 900.38s | T | 900.35s |
| aaron3_gccO0.mcsema.cbe.c | 46.87s | 1.91s | 0.03s | 0.11s | 900.43s | T | 900.44s |
Table 9: Details for termination verification of DarkSea translated lifted binaries.

| Benchmark                | AProVE | CPAchecker | KITTeL | 2LS | Ultimate | DarkSea |
|--------------------------|--------|------------|--------|-----|----------|---------|
| g0.c.execute            | 1.85s  | 0.01s      | 0.01s  | 0.12s | 7.51s    | 9.64s   |
| aaron2-g0.c.execute     | 1.34s  | 0.02s      | 0.12s  | 7.91s | 7.27s    | 8.14s   |
| aaron3-2-g0.c.execute   | 1.58s  | 0.02s      | 0.12s  | 7.18s | 8.00s    | 8.90s   |
| easy-g0.c.execute       | 1.65s  | 0.02s      | 0.12s  | 7.18s | 10.32s   | 10.25s  |
| Mysore-2-g0.c.execute   | 1.54s  | 0.02s      | 0.12s  | 7.91s | 9.44s    | 9.44s   |
| easy-g0.c.execute       | 1.63s  | 0.02s      | 0.12s  | 7.79s | 7.79s    | 8.00s   |
| aaron2-1-g0.c.execute   | 1.40s  | 0.02s      | 0.15s  | 7.03s | 10.25s   | 8.90s   |
| Pure3Phase-1-g0.c.execute | 1.86s | 0.02s      | 0.12s  | 7.18s | 9.44s    | 9.44s   |
| aaron3-2-g0.c.execute   | 1.88s  | 0.02s      | 0.12s  | 7.79s | 7.79s    | 8.00s   |
| easy2-1-g0.c.execute    | 1.46s  | 0.02s      | 0.14s  | 8.00s | 12.30s   | 12.30s  |
| aaron3-1-g0.c.execute   | 1.46s  | 0.02s      | 0.14s  | 8.00s | 12.30s   | 12.30s  |
| easy1-g0.c.execute      | 1.52s  | 0.02s      | 0.10s  | 7.51s | 8.14s    | 8.14s   |
| aaron3-1-g0.c.execute   | 1.52s  | 0.02s      | 0.10s  | 7.51s | 8.14s    | 8.14s   |
| easy2-2-g0.c.execute    | 1.52s  | 0.02s      | 0.10s  | 7.51s | 8.14s    | 8.14s   |
| aaron3-2-g0.c.execute   | 1.48s  | 0.01s      | 0.15s  | 7.91s | 7.91s    | 8.90s   |
| easy2-1-g0.c.execute    | 1.52s  | 0.02s      | 0.10s  | 7.51s | 8.14s    | 8.14s   |
| Singapore-g0.c.execute  | 1.83s  | 0.02s      | 0.15s  | 6.96s | 6.96s    | 6.96s   |
| Singapore-2-g0.c.execute | 1.45s | 0.02s      | 0.10s  | 7.03s | 7.03s    | 7.03s   |

I Detailed Results for LTL of Lifted Binaries

Table 10 is a more detailed version of the table from Sec. 7, this time comparing the performance of Ultimate versus DarkSea, when applied first to vanilla McSema IR, and then applied to DarkSea’s translated IR. The experimental result shows that our translations significantly eliminates all crashes and possibly unsound results occurring in the verification of the original lifted code. The unsoundness came from the fact that Ultimate detected possible memory errors in the code snippet setting run-time environment up in those programs, thus considering the programs to be infeasible with respect to the LTL properties and assuming that they always hold. DarkSea inherits such behavior from Ultimate. Moreover, the results on the simplified lifted code These results highlights the effectiveness of our bitwise branching technique which helps DarkSea to prove the LTL properties of all 17 benchmark correctly while Ultimate can only prove 6 of them. The possible memory errors were eliminated when our translation flattened the emulation state.
Table 10: Details for LTL lifted binary benchmarks, using vanilla McSema versus DarkSea’s translated IR and vanilla Ultimate versus DarkSea’s bitwise-branching (Section 4). Gray cells are unsound, green cells use slightly different settings (enabled SBE).

| Benchmark          | Property | Exp. | Vanilla McSema IR | DarkSea’s translated IR |
|--------------------|----------|------|-------------------|-------------------------|
|                    |          |      | Ultimate          | DarkSea                  |
|                    |          |      | Time Result       | Time Result              |
|                    |          |      |                   |                         |
| 01-exec2.s.c       | $\square x = 1$ | ✓    | 4.45s             | 4.56s                   |
|                    |          |      |                   |                         |
| 01-exec2.s.f.c     | $\square x \neq 1$ | x    | 6.31s             | 5.79s                   |
|                    |          |      |                   |                         |
| SEVPA gccO0.s.c    | $\square (x > 0 \Rightarrow \diamond y = 0)$ | ✓    | 6.31s             | 5.93s                   |
|                    |          |      |                   |                         |
| SEVPA gccO0.s.f.c  | $\square (x > 0 \Rightarrow \diamond y = 2)$ | x    | 5.16s             | 5.25s                   |
|                    |          |      |                   |                         |
| acqrel.simplify.s.c | $\square (x = 0 \Rightarrow \diamond y = 0)$ | ✓    | 5.17s             | 5.38s                   |
|                    |          |      |                   |                         |
| acqrel.simplify.s.f.c | $\square (x = 0 \Rightarrow \diamond y = 1)$ | x    | 6.06s             | 5.48s                   |
|                    |          |      |                   |                         |
| example1.fea.s.c   | $\Box error = 0$ | x    | 13.06s            | 13.14s                  |
|                    |          |      |                   |                         |
| example2.fea.s.c   | $\Box error = 0$ | ✓    | 11.22s            | 11.11s                  |
|                    |          |      |                   |                         |
| example3.fea.s.c   | $\Box error = 0$ | ✓    | 14.24s            | 14.15s                  |
|                    |          |      |                   |                         |
| example4.fea.s.c   | $\Box error = 0$ | ✓    | 10.47s            | 12.02s                  |
|                    |          |      |                   |                         |
| example5.fea.s.c   | $\Box error = 0$ | ✓    | 11.13s            | 11.36s                  |
|                    |          |      |                   |                         |
| example6.fea.s.c   | $\Box error = 0$ | ✓    | 4.92s             | 4.96s                   |
|                    |          |      |                   |                         |
| example7.fea.s.c   | $\Box x = 1$ | ✓    | 4.95s             | 5.22s                   |
|                    |          |      |                   |                         |
| example8.fea.s.c   | $\Box x \neq 1$ | x    | 4.57s             | 4.92s                   |
|                    |          |      |                   |                         |
| nondet gccO0.s.c  | $\Box x > 0$ | x    | 5.06s             | 4.78s                   |
|                    |          |      |                   |                         |
| example1.fea.s.c   | $\Box p = 1$ | ✓    | 4.97s             | 5.82s                   |
|                    |          |      |                   |                         |
| example2.fea.s.c   | $\Box p = 2$ | x    | 4.96s             | 4.87s                   |
|                    |          |      |                   |                         |