Via Interconnections for Half-Inch Packaging of Electronic Devices Using Minimal Fab Process Tools

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Reliability of a laser-via formation process for Fan-Out Wafer Level Packaging (FOWLP) technology was evaluated using Minimal Fab (MF) that is cleanroom-less and uses a half inch wafer. After a die-bonding and a compression molding process of a half-inch Si wafer, the laser-vias were formed with a diameter of 150 µm by irradiation of an ultra-violet (UV) pulsed laser beam. The measured thickness of the epoxy mold compound (EMC) was 93.9 µm of average with 1.9% of the variation at 1 σ in the half-inch wafer. The bottom diameter of the vias was 51.8 µm and 9.0% of the variation at 1 σ. In order to evaluate the contact-resistance of the vias, Cross-Bridge Kelvin Resistor (CBKR) test-structures were fabricated by the die-bonding the Si wafer with Al or Cu/Ti pads to a 42 alloy substrate, the compression molding, the laser-via, and the redistribution layer (RDL) formation. In case of the Al pads, the via conduction was obtained only in the outer peripheral area. On the other hand, in case of the Cu/Ti pad, all via conductions were obtained. The high-yield via-interconnections were achieved by using Cu/Ti pads.

Keywords: Via interconnections, Laser-via, Half-inch wafer, Minimal fab, FOWLP

1. Introduction

Fan-Out Wafer Level Packaging (FOWLP) technology has been widely researched and developed for miniaturization, high-performance, and high-functionality of electronic devices [1-3]. Its applications have been demonstrated by smartphones [4,5], automotive electronics [6], Internet of Things (IoT) sensor devices [7], wireless communications [8-10], healthcare [11,12], and wearable devices [13]. The underlying fabrication process technology of the FOWLP such as vias, redistribution layers (RDL), and solder joints have been developed to obtain high-reliability interconnections between the electrode pads on Si chips and solder balls mounted to the external terminals on a package [14, 15]. A laser-via process, which is able to open the vias by irradiation of a laser beam to an epoxy mold compound (EMC) on the pads, has often been applied to the fabrication technology of the vias [16-21]. Typically, in the EMC used for protecting the Si chip, spherical particles of SiO2 known as silica fillers are contained in the epoxy resin to reduce the mismatch in coefficient of thermal expansion (CTE) between the Si chip and the EMC [22,23]. During laser ablation process, SiO2 which has a higher melting point than epoxy resin is difficult to ablate. The non-ablated silica fillers greatly affect the via-interconnections since it redeposits around the vias and remains on the bottom of the vias [20,21]. This is a common issue in the general packaging technology, not only the FOWLP technology. The FOWLP processes without the laser-via process have been developed to avoid the filler problem [24-26]. The process without using the filler begins with a formation of Cu pillars on a wafer. After dicing, the chips are attached face-up on the carrier substrate with adhesive tape, followed by compression molding. After polishing, the top of the Cu pillars is revealed and the RDL is formed on the polished surface as shown in Fig. 1 (a) [24-26]. The aforementioned fabrication process is currently in mass production. This is because that the Cu pillar technology needs
300 mm wafer process technology including photolithography with a huge investment. Due to the mass production, it is unreasonable for on-demand manufacturing with a small order.

In on-demand applications except mass production devices like smartphones, chips are often connected with each other with a small number of electrode pads [6-8,12]. Thus, a pad pitch becomes wider, where laser via technology is still valuable. But, one has to solve the residual filler problem.

The process development of the laser-via introduced by Minimal Fab (MF) [27-30] is suitable for a low-volume production as shown in Fig. 1 (b) [31]. Since the MF performs half-inch wafer process one by one as a single chip, the device and packaging process is low cost and high throughput [28]. Material of the electrode pads, via configuration, and laser-via process for MF have been evaluated for further reduction of the via contact-resistance [31].

In this paper, we report the reliability evaluation and improvement to achieve electrically stable via-interconnections of FOWLP fabricated using the MF.

2. Experimental

2.1. The shape of the vias

In order to evaluate the via shape, the following process was performed using MF processing tools. A bare Si wafer with a diameter of 12.5 mm (nominally called "half-inch"), and thickness of 250 µm was attached using Ag paste to an alloy substrate with a diameter of 13.5 mm and thickness of 200 µm. The die-bonding tool was used to dispense Ag-paste to the alloy substrate. The bonding force of 10 N and the bonding temperature at 180 °C was applied to the wafer for 60 s. After that, the die-bonded Si wafer was covered with the EMC by compression molding tool. The liquid EMC was dispensed on the surface of die-bonded Si wafer. The compression molding force of 1.8 kN for 180 s was applied. The vias with a diameter of 150 µm, and 1 mm-pitch were formed by irradiation of the pulsed ultra-violet (UV) laser beam, which has the wavelength of 355 nm (Nd: YVO₄ laser). The focused spot diameter (1/e² of maximum fluence with Gaussian profile) was around φ20 µm. FWHM (Full Width at Half Maximum) of the pulse was around 9 ns. The average energy per one pulse of the laser beam was 0.8 µJ. The pulsed UV laser beam was scanned over the molded wafer using an X-Y Galvano scanner. During the raster scanning of the laser, laser beam was switched on only for the locations of the vias specified by CAD (Computer Aided Design).

The depth and bottom geometries of the 89 fabricated vias in the half-inch wafer area were measured using an optical microscope.

2.2. The contact-resistance of the vias

For measurement of the via contact-resistance, the Cross-Bridge Kelvin Resistor (CBKR) test-structures with three vias were fabricated by the following process using MF tools [31]. After the piranha and RCA cleaning of the half-inch Si wafer, a TEOS (Tetraethylorthosilicate) film of 100 nm thickness was deposited on the Si wafer by a plasma CVD (Chemical Vapor Deposition) as an electrical isolation. Al-1%Si (later referred to Al) film of 1.0 µm thickness was deposited by a plasma sputtering tool. The Al pads were formed by a photolithography process (photoresist coating, maskless-exposure, and photoresist developing), following by a wet-etching, and a photoresist removal by acetone and IPA cleaning.

The Al pads formed on the Si wafer was used as a die to carry out a die-bonding and a compression molding process. Prior to the laser-via process, a photoresist (AZP4620) was coated on the mold compound surface by the spin coating to prevent the re-deposition of the silica fillers. The photoresist thickness was approximately 9 µm. The laser-via process was performed under the above-mentioned condition. The photoresist with deposited silica fillers was then removed by acetone and IPA cleaning. Ar plasma cleaning was performed using a CCP (Capacitively Coupled Plasma) dry-etcher to eliminate the surface oxide of the Al pads at the bottom of the vias. The
applied RF power of the CCP dry-etcher was 20 W for the upper electrode (40 MHz) and 30 W for the substrate electrode (2 MHz). The chamber pressure was 3 Pa and Ar flow-rate was 3.0 sccm. The Ar plasma cleaning was applied for 180 s. The Cu film of the RDL was deposited to the cleaned EMC surface by the Cu sputtering following by Cu electroplating with a DC current density of 50 mA/cm² for 270 s. The Cu electrode pads were fabricated by photolithography, Cu wet-etching, and photoresist removal. The photoresist (AZP4620) of 9 μm thick was again formed for protecting the Cu film inside the vias. Finally the 85 CBKR test-structures placed with 1.0 mm pitch were realized where the total number of vias formed in the package was 255 (= 85 × 3 electrodes).

Cu/Ti pads were formed on another Si wafer in the same manner as the Al pad process. Ti sputtered film of 50 nm thick was deposited as an adhesion layer before a Cu sputter of 1.0 μm-thick film.

The via contact-resistance was measured from Cu electrode pads on the mold surface using a prober. A current of ±10 mA was applied to single via and the voltage difference at interface between bottom of the via and the Al (or Cu/Ti) pad on the wafer was measured. The via contact-resistance was determined from the slope of obtained I-V characteristics.

The cross-section of the via was observed by a Scanning Electron Microscope (SEM).

3. Results and discussion

Figure 2 shows the cross-sectional SEM images of the via with the Cu/Ti pad. The measured top of the via diameter was 152 μm, which was approximately the same as the designed value of φ150 μm. The sidewall of the via had a tapered shape with the slope of 58°. The Cu film was formed conformally from the via top through the via sidewall until the via bottom. The film thickness of Cu at the bottom of the via was thinner than that of the top of the via because the chemical reactivity of at the via bottom seems to be slower than that of the via top, which would be attributed to a steric hindrance to cause a slower transportation of chemical spices at the via bottom. At the via sidewall surface, an interface roughness of 3.7 μm was observed between the Cu RDL layer and the EMC layer as shown in Fig. 2 (b). The interface roughness is completely buried in the Cu RDL layer with the thickness of 10.8 μm. The resultant Cu overlayer on the interface layer of 7.1 μm is comparable to 7 μm of Cu RDL layer on the EMC flat surface around the via. Although the 4 μm at the bottom of the via is less than 7 μm, 4 μm is enough to make an electric contact. Thus, in a tapered via structure full embedding of a via by a metal material is not necessarily needed, but conformal deposition of a metal layer is enough.

In the tapered via structure, there are three geometrical factors to form a flat bottom area to make an electrical contact: (1) EMC thickness, (2) taper angle of the sidewall, and (3) EMC tail toward the inner direction at the periphery of the via bottom. Since the three factors have fabrication variations, a via bottom diameter should be designed with a margin to exceed the three variations. Figure 3 shows histograms of the depth and the via bottom diameter of the 89 fabricated vias formed with 1.0 mm pitch after the laser-via process. Figure 3 (a) shows a histogram of measured via depth, i.e., the EMC thickness. The average thickness was 93.9 μm with three standard deviations (3σ) of 5.4 μm. Since the tapered angle is 58°, the height variation of 5.4 μm is converted to be 3.4 μm as a lateral variation at the via bottom.

![Fig. 2. SEM cross-sectional images of the interface between the bottom of the via and Cu/Ti pad on Si wafer.](image-url)
In Fig. 3 (b), the average via bottom diameter was 51.8 \( \mu m \) with three standard deviations of 14.1 \( \mu m \). This value is \(~4 \) times as the 3.4 \( \mu m \). This suggests that there are other factors to generate the variation. Other factors would be a variation of the tapered angle and a variation of the tail length. An important point of view here is that the total variation of the diameter at the via bottom is around 14.1 \( \mu m \). For example, if a demand for the contact diameter is 30 \( \mu m \), every via makes an electrical contact for a designed bottom diameter over 30 \( \mu m \) + 14.1 \( \mu m \). Since in the present experiment the average diameter is 51.8 \( \mu m \), contact areas over 37.7 \( \mu m \) (= 51.8 – 14.1) are obtained for all vias. In other words, all vias should have enough contact areas.

Next, we have actually measured the electrical contacts for the vias. Figure 4 shows the distribution map of the measured via contact-resistances. Only 44 out of the 85 CBKR test-structures were electrically conducted in case of the Al pads as shown in Fig. 4 (a). The measured via contact-resistances had an average of 10.2 \( \Omega \), with a variation of 70.3% for one standard deviation. It is noted that the vias in the outer periphery of the wafer were conducted. The vias in the central area of the wafer were almost non-conducted.

In the case of the Cu/Ti pad, all the 255 vias were conducted, thus all the 85 via contact-resistances were able to be measured as shown in Fig. 4 (b). The contact-resistances had an average of 16.1 m\( \Omega \) with a variation of 29.8% as one standard deviation. The via contact-resistance of the Cu/Ti pads were drastically reduced by three orders of magnitude than that of the Al pads. Furthermore, the yield and variation of the via-interconnections were improved.

It is considered that there are two possible causes for the failure of the Al pad conduction. The first one is the ablation of the Al layer. The epoxy resin evaporates at approximately 350 °C [32,33].
Therefore, the laser irradiation heated the surface temperature more than 350 °C on the spot of the laser beam. In a previous work, surface roughness on the Al pad was observed by an optical microscope [31]. It is considered that the Al pad surface was ablated by the laser irradiation because Al has a relatively low melting point of 660 °C. Since Cu has the melting point of 1085 ºC, Cu pad has high-tolerance for the laser ablation as compared with that of the Al pad.

The second cause is the oxidation of the Al pad surface. Al is easily oxidized compared with Cu. It is considered that the oxide film on the Al pad surface was remained. Figure 2 (b) shows a magnified SEM image of the via bottom, where the Cu/Ti pad was connected directly with the Cu film of the RDL without any intermediate layer.

In this work, we have demonstrated the via formation process that contributes to reliable via-interconnections by forming the taper-shaped vias. With a diameter of 150 μm and a pitch of 500 μm, around 300 vias were formed within the area of half-inch wafer. The diameter and density of the vias are sufficient for a system in package developed within the half-inch size in case without the requirement of the large number of external Input and Output (I/O) terminals. If the system can be mounted completely within the half-inch sized package, it is unnecessary to extract more than 100 external terminals of solder balls.

4. Conclusion

We evaluated the reliability of the laser-via process to achieve electrically stabilized via-interconnections using MF. The depth and bottom diameter of the vias were measured after the laser-via process. The variation of the EMC thickness was 1.9% in the half-inch area. The uniformity of the diameter of via bottom was suppressed to be 9.0%. Thus, it ensures that the electrode pads at the bottom of the vias can certainly make contacts with the conductive metal layer. The reliability of the via-interconnection was improved by replacement of the pad material from Al to Cu. It was found that the developed laser-via process is able to be used as a practical process in FOWLP technology for a small number of vias.

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