Current mirror with charge dissipation transistor for analogue single-event transient mitigation in space application

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Abstract
Current mirror utilizing an extra transistor for single-event-induced charge dissipation is proposed. This technique involves two inverters and a dissipation transistor. The inverters are employed as a sensor that turns on the dissipation transistor when heavy ion hits the sensitive node, and the dissipation transistor helps to attenuate the single-event transient (SET)-induced perturbation. During normal operation, inverters are in static state, and the dissipation transistor is off, which has no effect on circuit performance, and contributes to negligible power consumption. Once heavy ion strikes the sensitive node and the fault is detected, the dissipation transistor is triggered to self-correct the SET disturbance. Simulation results indicate that the proposed technique reduces the SET pulse duration by at least 48.4% with linear energy transfers of 30 MeV cm²/mg. This paper provides a novel hardening method for analogue single-event transient mitigation in current mirror circuits.

\[ I_{\text{out}} = \frac{(W/L)_R}{(W/L)_g} I_{\text{ref}} \] (1)

The key point of current mirrors is the translation from reference current \( I_{\text{ref}} \) to \( I_{\text{out}} \) through the gate potential \( V_g \) which is also the drain potential of the root transistor \( M_R \) and apparently to be the most sensitive node in this topology. Any variation on \( V_g \) would distort all the leaf branches in circuit, causing degradation to all the subsequent blocks. Therefore, we focus on ASET mitigation on the case where \( M_R \) is hit by particle.

In this paper, two inverters as a sensor and a dissipation transistor for extra charge cancellation are proposed as a radiation-hardened-by-design (RHBBD) technique for ASET mitigation on node \( V_g \). The design is modelled in 28-nm bulk CMOS process, and technology computer-aided design (TCAD) simulation tool is used to evaluate the radiation performance. Compared with the normal topology, simulation results indicate that the current mirror with dissipation transistor significantly alleviates the single-event transient (SET) pulse width \( W_{\text{SET}} \) with negligible penalty.
2 | RHBD CURRENT MIRROR CIRCUITS

The root node of current mirror DC-biases all subsequent leaf branches and tend to be particularly sensitive to SETs. If $M_{R}$ is hit by energetic particle and the SET glitch occurs at $V_g$, all the output currents will undergo perturbations until the SE deposited charges are dissipated. Previous studies have reported several techniques to increase the charge dissipation rate at the struck node. By enlarging the transistor size, the drive capability is increased, and heavy-ion-induced charges can be dissipated more rapidly [7]. A similar technique is forward biasing the bulk of vulnerable transistor, which decreases the threshold voltage and increases the device drivability [8,9]. Another mitigation technique is lowering impedance at critical nodes, which enhances the escape speed of the excess ionization charges toward supply rails [10,11]. However, adopting those techniques affects circuit’s normal operation, and the relevant circuit parameters need to be precisely adjusted according to the design specifications.

As shown in Figure 2a, when heavy ion strikes $M_{R}$, the PN junction between the drain node and N-well collapses, and drain potential tends to collapse to N-well potential, which results in a positive SET pulse observed at $V_g$. This positive current can only be removed through load current source, and SET pulse width ($W_{SET}$) is determined by the amount of charge collection ($Q_D$) and the rate of the charge restorability ($I_{ref}$) [12]:

$$W_{SET} \propto Q_D \times \ln \left( \frac{1}{I_{ref}} \right).$$

(2)

To solve this problem, another pull-down NMOS transistor is deliberately added at $V_g$ to help dissipating excess charges and reducing SET perturbation. The RHBD technique ideally has no impact on circuit normal operation, and the following conditions shall be met:

1. The dissipation transistor is only triggered once, and a positive SET glitch occurs at $V_g$, otherwise remains switching off.

2. The size of dissipation transistor should be small in order to reduce the possibility of being hit by particles and decrease the area penalty.

As shown in Figure 2b, a dissipation transistor $M_d$ and two inverters are added as an RHBD technique in circuit. The threshold of the inv1 is tuned to be higher than the nominal voltage level of node $V_g$. This ensures that during normal operation, the node $V_g$ is logic low (‘0’) seen by inv1’s input, which results in a low output at the gate of $M_d$. Therefore, $M_d$ is off and has no impact on circuit performance during normal operation. However, once a heavy ion strikes $M_R$ and SET pulse occurs at $V_g$, this positive glitch would produce a ‘0-1-0’ pulse at inverter’s output and temporarily turn on the pull-down transistor $M_d$, which helps to speed up the discharging of the heavy-ion-deposited charges.

Heavy-ion-induced positive shift of potential $V_g$ is the trigger signal to open the dissipation transistor, which helps to pull down $V_g$ to its original level. In this case, two current paths are provided for ionization charge dissipation. One is through the load current source, and the other is through the dissipation transistor $M_d$. As a result, the SET pulse width is modified as follows, which is alleviated attributed to the dissipation current ($I_d$) through the pull-down transistor $M_d$:

$$W_{SET} \propto Q_D \times \ln \left( \frac{1}{I_{ref} + I_d} \right).$$

(3)
3 | SIMULATION DETAILS AND RESULTS

To verify the effectiveness of the proposed technique, 3D TCAD simulation tool is adopted in this work. TCAD has been proven to be a useful tool for SET investigation, which provides insight into the physical mechanisms of SEEs [13,14].

In order to simplify our simulation and analysis process, only one root node and one leaf node \( M_R \) and \( M_{1,1} \) sharing the same device size \( \frac{W}{L} = 12.5 \mu m/300 n \) are included in this study. \( M_R \) with minimum feature size \( \frac{W}{L} = 100 n/30 n \) is added in RHBD circuit. Comparing with mirror devices, \( M_d \) attributes to negligible area penalty and has trivial probability being directly hit by particles. 50 \( \mu A \) is chosen as the reference current \( I_{ref} \) to DC-bias leaf branches, which is widely applied in practical applications. During normal operation, output currents are the same as the reference one \( I_{out1} = I_{out2} = \ldots = I_{ref} \). \( M_R \) is the struck transistor and \( I_{out} \) is the output node for observation.

Device simulations are used to obtain the shape, amplitude, and duration of transient pulse generated by the interaction of incident particle and the sensitive transistor in circuits. In our simulations, all MOS transistors are modelled as TCAD numerical device model to provide a more accurate result compared with the SPICE and TCAD mixed-mode simulation. The root transistor \( M_R \) is struck by a heavy ion, and the initial SET appears at the node \( V_g \) and finally propagates to the output terminal \( I_{out1} \).

Typical bulk CMOS technology is used in our investigation. The structural and doping profiles of the devices are calibrated to that of the 28-nm commercial SPICE models for DC and AC (transient) calibrations [15]. Transistor size, spacing, and well configuration are satisfied with layout design rules.

In the TCAD simulation process, heavy-ion strike is simulated as an electron–hole pair column with the track as its axis. Ion used in simulations has linear energy transfers (LETs) of 30 MeV cm\(^2\)/mg. The LET value is kept constant along the heavy-ion track. The length and radius of ion track are 10 and 0.025 \( \mu m \), respectively. We simulated ion strike at the centre of drain of the struck transistor normally. Same as our previous works [16-18], the included physical models are (a) Fermi–Dirac statistics; (b) the doping-dependent carrier mobility model with high electric field saturation, carrier–carrier scattering, as well as interface scattering; (c) carrier recombination model: doping-dependent SRH and Auger recombination; (d) the effect of band-gap narrowing; (e) hydrodynamic carrier transport model; (f) other models are configured with default models and parameters.

Ideally, current mirrors should be invariant over operating conditions. In order to prove the circuits’ robustness, SPICE simulations are carried out for process, voltage supply, and temperature (PVT) analysis at the bias point of 50 \( \mu A \). Simulation results indicate that the PVT variations are 1.73% for both normal and RHBD circuits. The power consumption is 89.46 \( \mu W \) for both cases. Since dissipation transistor is off during normal operation, only negligible static power dissipation would be introduced by extra inverters.

Figure 3 illustrates the transient current pulses obtained from current mirror with or without \( M_d \) as an SET dissipation transistor. Consisting with our expectations, negative perturbations are observed at outputs due to the positive peak on their gates. After \( M_R \) struck by an ion, the PN junction between P+ drain and N-well collapse, and a positive SET pulse occurs at \( M_R \) drain node, which mirrors to transistors’ gate nodes. Therefore, all devices in leaf nodes tend to turn ‘off’, and output currents decrease accordingly. In the radiation-hardened topology, \( M_d \) with minimum feature size is added for SET mitigation. Simulation results indicate that the proposed technique effectively reduces the SET pulse duration. In this paper, we choose 40 \( \mu A \) as the threshold level to represent the SET outputs for comparison. For normal circuit without any hardening technique, the SET pulse width is 4.392 ns, while it is 2.264 ns for the RHBD circuit. In other words, the proposed technique reduces SET pulse width from the normal configuration by 48.4%.

4 | DISCUSSION

4.1 | Dissipation transistor optimization

The device size of the pull-down transistor \( M_d \) needs to be carefully considered for the reasons below: in order to reduce the probability of \( M_d \) being hit in real-life application, the dimension of \( M_d \) should be minimized; however, in order to speed up the charge dissipation process and lowering SET duration, \( M_d \) should be large enough. Therefore, the SET pulse width \( W_{SET} \) versus \( M_d \) device size is studied to find an optimal radiation-hardening strategy.

Figure 4 gains insight into the SET pulse width caused by ion striking with various LET values. As shown in Figure 4a, \( W_{SET} \) increases almost linearly with the increases of LET, which indicates that higher energy deposition results in larger SET duration. As the device size of dissipation transistor \( M_d \)
increases, $W_{SET}$ decreases accordingly, which is consistent with our previous analysis that larger pull-down transistor is more conducive to discharging additional charges. Device with large $W/L$ ratio has a higher drive capability, which helps to speed up the charge dissipation process and reduce SET pulse width. Pulse-width reduction ratio (PWRR) is adopted in this work to represent SET hardening performance with various $M_d$ dimensions, which is defined as

$$\text{PWRR} = \frac{W_{SET}(\text{without } M_d) - W_{SET}(\text{with } M_d)}{W_{SET}(\text{without } M_d)}.$$  \hspace{1cm} (4)

As plotted in Figure 4b, effective SET mitigation performance is achieved when a minimum feature size $M_d$ transistor ($W/L = 100/30 \text{ nm}$) is added in circuit. However, as $M_d$ becomes larger, extra benefits obtained from transistor enlarging become lower. Taking LET of 30 MeV·cm$^2$/mg as an example, 48.4% SET PWRR is achieved with $M_d$ device size of $W/L = 100/30 \text{ nm}$. Extra 10.2% and 16.8% PWRR can be gained when $M_d$ enlarges to $W/L = 150/30 \text{ nm}$ and $W/L = 200/30 \text{ nm}$, respectively. However, when the gate width of $M_d$ transistor is higher than 200 nm, trivial benefit can be obtained

**FIGURE 4**  (a) Single-event transient pulse widths, (b) pulse-width reduction ratio (PWRR) versus linear energy transfer (LET) values with various $M_d$ dimensions

for SET pulse attenuation, whereas the probability of $M_d$ being hit is boosted. In this paper, the minimum feature size $M_d$ transistor is preferred in circuit to balance the trade-off between the SET pulse mitigation performance and the cross section of the RHBD circuit.

### 4.2 Threshold-level shift of Inv1

The key point for this RHBD technique working properly is that the threshold voltage of Inv1 is tuned to be higher than the normal level of node $V_g$, which ensures that the output of inverter chain is ‘0’, and dissipation transistor is ‘off’ during normal operation. Potential disturbance caused by PVT variations and ageing effects should be taken into account. Total ionizing dose (TID) effects also degrade devices’ electrical characteristics, but CMOS scaling helps to improve the TID effects tolerance [19]. In this paper, the Inv1’s threshold level is set to be 100 mV higher than node $V_g$, which exceeds the noise floor of typical circuits.

As shown in Figure 5, a common method to shift inverters' threshold level is adjustment of transistors' $W/L$ ratio. Through enlarging the gate width of PMOS and the gate length of NMOS, the threshold voltage is shifted to right. In this case, the cross section of Inv1 would not be increased as the following reasons:

Since a relative low voltage is seen by inverter’s input, the drain of NMOS device with reverse-biased junction is the most sensitive region in circuit [20]. Only heavy-ion hitting on this node can cause error in inverter chain. As shown in Figure 6, with the increasing of gate length, the sensitive area would not

**FIGURE 5** Input and output characteristics of an inverter with modulation of $W/L$ ratio

**FIGURE 6** Schematic of a transistor with gate length increasing
be added accordingly, which mitigates the boost up of circuit’s cross-section. Still, in order to reduce the probability of being hit by particle and remain a low cross-section of RHBD circuit, minimum size should be adopted in inverters.

5 | CONCLUSION

In this paper, a novel RHBD technique is proposed for SET mitigation in current mirror circuits. Two inverters as a sensor used to trigger a dissipation transistor for excess charge compensation are applied at the bias node of current mirror, which is one of the most vulnerable nodes in the circuit. Simulation results indicate that minimum feature size dissipation transistor helps to reduce the SET pulse width by 48.4% with an LET of 30 MeV·cm²/mg. Larger dissipation transistor can be exploited to further reduce the pulse duration, but the cross section of the RHBD circuit would increase accordingly. This paper presents an inspiring radiation-hardening technique for analogue IC designers.

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