An effective nano design of demultiplexer architecture based on coplanar quantum-dot cellular automata

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Abstract
Quantum-dot cellular automata (QCA) are prospective nanotechnology with striking performance to tackle the shortcomings of complementary metal-oxide-semiconductor (CMOS) transistor-based technology such as fabrication dimensions and switching speed. The demultiplexer, as a crucial component for the design of many logic circuits, comprises a circuit for separating the multiplex data into the component data. The demultiplexer is highly utilised in the communication system for building serial data lines to parallel ones. So, its efficient schematisation has turned to an issue that has captured the concentration of the investigation group. Therefore, a novel structure of QCA-based one to two demultiplexers is proposed, and it is employed to design one to four demultiplexers. QCAdesigner software, as a powerful layout and tool for simulation, is utilised for evaluating the validity and practicality of the proposed structures. The detailed evaluation of proposed layouts shows excellent performance than prior operations, and notable developments regarding the occupied area, cell count, and latency.

Therefore, based on the importance of this component, efficient QCA-based demultiplexer design has brought the widespread concentration of the investigators’ community.

Here principal attention is given to introduce simple and optimised one to two demultiplexer based on QCA technology. The proposed one to two demultiplexer has been used as a basic module to implement one to four demultiplexer. The proposed design is widely compared to the other priorly suggested ones with regard to various characteristics. Presented layouts have impacts on total circuit performance with a view to area possession, number of cells, and latency. The main aim of this study is briefly explained below:

- Presenting an optimal structure of a single-layer one to two demultiplexer based on QCA to reduce cell counts and consumption area.
- Comparing and evaluating the introduced schematisation with other modern schematisations.
- Analysing and demonstrating the validity of the suggested schematisation with the utilization of the QCAdesigner tool.

Section 2 provides a review of the previous QCA-dependent demultiplexer layouts. The suggested layout for one to two demultiplexer depending on QCA is explained in Section 3.
Also, a new implementation of one to four demultiplexer is presented in this section. Section 4 expresses QCA-based layout and the execution outcomes of the suggested architectures, which are obtained from QCA designer tool along with corresponding comparative studies. In the end, in Section 5, the conclusion and future work are drawn.

2 | RELATED WORK

Different architectures and implementations for QCA-dependent demultiplexers have been discussed in this section.

Iqbal et al. [25] have introduced a new modular procedure for the design of 1–2
n
demultiplexer. This approach provides a quick procedure for designing high order demultiplexers. At first, a one to two QCA demultiplexer structures are provided as a building block, and then one to four and one to eight QCA-based demultiplexers are designed. Any 1–2
n
demultiplexer schematised with the suggested procedure may be simply enhanced to a larger 1–2
n
+ 1
n
demultiplexer. This design methodology consists of less number of cells and the occupation of a smaller area. The presented design has superior performance in terms of circuit stability and power consumption.

Sardinha et al. [22] have proposed QCA one to four demultiplexer as an essential part of building a nano-router circuit based on QCA. This component is implemented with the utilization of a significant number of gates. An architecture with numerous layers without interference by cells among each other has been utilised to address the issues of lines crossing. This component helps to have higher speed communication in the nano-router.

Also, a novel concept of 1–2
n
demultiplexer with the utilization of QCA technology has been introduced by Ahmad [21]. The proposed one to two demultiplexer design has been created for the rotation of two 2-input AND gates. The primary concentration of the current execution is an efficiency enhancement and circuit complexity decrement. Using this structure, an efficient one to four demultiplexer has been presented in which two inverters and four 3-input AND gates were needed. Introduced layouts have developments regarding area occupation and intricacy.

A one to two demultiplexers have been designed with the utilisation of three-dot QCA architecture by Das et al. [26]. In this work, the primary gates' schematisation with three-dot QCA is shown and used for schematising the demultiplexer circuit. The design of this structure has been conducted with no overlapping by utilization of minimum gates. In the suggested architecture, a significant decrement in the number of cells and fields was attained. But, the utilization of the area of the suggested architecture has been notably high.

A simple and optimised QCA-based single layered demultiplexer has been presented by Khan and Arya [27]. This design uses only two majority gates where both of them act as AND gates and one NOT gate. In the one to two demultiplexer, the input signal is applied to both of the majority gates which perform AND operation using the select line and produce two outputs. The proposed design is coplanar and uses less number of cells. The energy dissipation of this structure is very minute and has a small latency, but it is negligible.

Chakrabarty et al. [28] have designed a one to four demultiplexers to manufacture a QCA-based Nano-calculator. This demultiplexer is used to integrate adder, subtractor, multiplexer and divider circuits into a single circuit to simulate the calculator circuit. The presented demultiplexer is designed based on a multilayer crossover approach, and three clock zones are used to complete a full cycle. Offered layout suffers from higher total area and QCA cell count.

Mallaia et al. [29] have presented a new approach to multiplexer and demultiplexer layouts using QCA logic gates along with power dissipation analysis. In this design, one to two demultiplexers involve two majority gates, and one to four demultiplexers is composed of eight majority gates. The proposed configurations avoided the multilayer crossover. The outcomes guarantee the predominance of presented plans according to the power dissipation and time deferral.

Finally, Ganesh et al. [30] have proposed some basic algorithms based on majority voting logic for combinational circuits like QCA demultiplexer. One to four demultiplexer is developed with the equation by the majority voting scheme equation. In this implementation, one input and two select lines arrive at the majority gates using coplanar crossover approach to produce four outputs. In this circuit, eight majority gates are required that increased the delay and complexity in the circuit. Some related QCA-based demultiplexer designs are surveyed in Table 1.

3 | PROPOSED DESIGN

The demultiplexer as a data distributor is a combinational circuit that receives an input data and chooses an n number of output lines based on the value of the select lines. 1–2
n
demultiplexers are made up of m AND gates; one for 2
n
possible integrations of the n select inputs, with the single line input, fed to the whole of the mentioned gates. Since just one AND gate will remain active, it determines which input will be required to direct to which output [25, 31]. One to two demultiplexer has two outputs and a unit data input line using one selection line. According to the logic diagram shown in Figure 1, an inverter and n number two AND gates are needed for building the suggested one to two demultiplexer with the main objective to improve efficiency and reduce complexity. The output logic function for one to two demultiplexer can be expressed via Eq. (1).

\[
\text{Output } Y_0 = \bar{I}S, \text{ Output } Y_1 = IS \tag{1}
\]

QCA layout of the suggested single layer one to two demultiplexer is given in Figure 2, aiming to attain huge device density, low layout area, and top calculation velocity, where I is
### TABLE 1 An overview of the reviewed previous works in the field of quantum-dot cellular automata (QCA)-based demultiplexer

| Article | Main opinion | Advantages | Limitations |
|---------|--------------|------------|-------------|
| Ganesh et al. [30] | Designing a one to four demultiplexer as one of the combinational circuits based on majority voting logic in QCA | • useful for building QCA circuit | • increasing area |
| Sardinha et al. [22] | Designing multilayer one to four demultiplexer as a part of the nano-router building blocks | • area improving | • increasing cell count |
| Iqbal et al. [25] | Introducing a novel and efficient design of modular 1–2\(^n\) demultiplexer using QCA | • cell count improving | • increasing clock phases |
| Chakrabarty et al. [28] | Proposing a new one to four demultiplexer to integrate the four circuits into a calculator circuit in QCA technology | • less cell count | • high clocking cycle |
| Ahmad [21] | Proposing an optimised design of 1–2\(^n\) demultiplexer using QCA | • less latency | • increasing area |
| Das et al. [26] | Offering a three-dot QCA based one to two demultiplexer without any overlapping using minimum gates | • less power consumption | • high power consumption |
| Khan and Arya [27] | Proposing a simple and optimised QCA-based single-layered demultiplexer and analysing energy dissipation | • fast response | • high power consumption |

### FIGURE 1 Logic diagram of one to two demultiplexer

![Logic diagram of one to two demultiplexer](image)

The demultiplexer signal input, \(S\) refers to the selector input, and \(Y_0\) and \(Y_1\) are the demultiplexer output signals. The proposed demultiplexer has been constructed using the 90\(^\circ\) QCA cells and there is no need for any crossover. It is clear from Figure 2 that the proposed layout is implemented using only 21 QCA cells and occupies 0.02 \(\mu\text{m}^2\) area. Also, it makes the utilization of two phases of the clock for producing valid output. Different coloured cells demonstrate four periodic stages of QCA clocking that make all the inputs reach a particular logic gate at the same time.

Higher regular demultiplexer circuit can be executed with the utilization of the suggested QCA one to two demultiplexer as elementary building blocks. The schematic diagram of the one to four demultiplexer has been indicated in Figure 3 that is implemented by applying three one to two demultiplexer and used as a module. In the logic implementation, one to four demultiplexer, four AND gates, and two inverters are used. Each output of the first demultiplexer is entered into one of the other two demultiplexers as an input. As can be seen in Figure 3, \(S_0\) and \(S_1\) are the choosing lines utilised for routing the input to the determined output line. The truth table of one to four demultiplexer is presented in Table 2. By using this table, the logic expression of demultiplexer can be given as Equation (2).

\[
\text{Output } Y_0 = IS_1\overline{S_0}, \text{ Output } Y_1 = I\overline{S_1}S_0, \text{ Output } Y_2 = IS_1\overline{S_0}, \text{ Output } Y_3 = IS_1S_0
\]
Figure 2 refers to the ultimate QCA design of suggested one to four demultiplexer, which is made up of quite similar blocks, as presented in the one to two demultiplexer. Different combinations of the select lines ($S_1$ $S_0$) determine one single input data that is switched to the output lines. The layout of the proposed one to four demultiplexer is used in coplanar crossover wiring with normal and 45 rotated QCA cells in a single layer. The proposed QCA structure consists of 92 QCA cells covering 0.12 $\mu m^2$ layout area. As can be seen, the output signals of this structure are delayed by one clock cycle.

4 | SIMULATION OUTCOMES

The current part introduces the tool used for simulation and the outcomes obtained from the simulation along with precision assessment. Also, the comparison to modern schematizations has been determined.

4.1 | Simulation tool

QCA designer is an accurate tool for simulation to validate the QCA circuits. This tool is developed by the University of Calgary and gives subscribers the potency to approve and scheme any QCA systems [32]. To validate and evaluate the design of the suggested schematizations, QCA designer 2.0.3 is used. Also, the simulation engine has been regulated to link simulation parameters and vector sort by default.

4.2 | Accuracy analysis

The simulation results for the proposed QCA-based one to two demultiplexer is illustrated in Figure 5, whose functions are
validated. According to this result, two waveforms along with various frequencies have been imported to $S$ and $I$. Input $I$ is revealed in output $Y_0$ when selection $S$ is down, and when the $S$ is high, input $I$ appears in output $Y_1$. Therefore, selection lines $S$ varies to select outputs $Y_0$ and $Y_1$. The outputs $Y_0$ and $Y_1$ are generated properly after a delay of 0.5 clock cycles.

Figure 6 illustrates the simulation results for the presented one to four demultiplexer along with three different waveforms that are imported to inputs $S_0$, $S_1$, and $I$. When the select line $S_0$ is 00, the input $I$ is transferred at the output $Y_0$. If $S_0$ is equal to 01, the input $I$ emerges at the output $Y_1$. Also, for ‘10’ and ‘11’ combination of the select line, outputs $Y_2$ and $Y_3$ represent the input $I$, respectively. Depending on this result, the propagation postponement from input cells to each the output cell is identical and is one clock cycle where the input signal shows up at 0 of the first clock cycle, and the output is transferred at clock three from the same cycle.

### 4.3 Comparisons

A comparative analysis has been conducted between the offered demultiplexers and the designs in terms of QCA cells. The density of the circuits and clocking zone amounts utilised to schematised the circuits are illustrated in Table 3. The main focus of the proposed one to two demultiplexer implementation with a simple structure is achieved by decreasing the intricacy of the circuit and enhancing the yield as is evident from Table 3, the suggested structures consist of less area occupation and reduced clock delays in comparison through to other designs. Reduction in the total area covered by proposed one to two demultiplexer is notable. This design has not significantly improved in cell count and delay. In contrast, implemented one to four demultiplexer by applying three modules of one to two demultiplexer has an influence on total circuit performance with a view to cell numbers and effective area as compared to the already reported ones. Also, this QCA architecture includes less latency compared to the existing structures except for the proposed one to four demultiplexer in [28]. For better analyses, the multiplexer’s structures of comparison part includes the QCA cost parameter. The QCA cost function in [34] is used to evaluate these circuits and is expressed as follows:

$$\text{Cost}_{QCA} = \left( M^k + I + C^l \right) \times T^p, 1 \leq k, l, p \quad (3)$$

It is found that the parameter QCA cost includes important metrics like the number of minority gates, inverters, wire crossings, and delay as shown by $M$, $I$, $C$, and $L$ respectively. Due to the achieved results, the suggested one to four demultiplexer layout is reduced in terms of quantum cost compared to the existing design. In contrast, the QCA cost of one to two demultiplexer is the same as the designs in References [21,27,29].

### 5 CONCLUSION AND FUTURE WORK

The present article encompassed a new and simplest layout of one to two demultiplexer that highlights approximately all features of the QCA technology. The basic benefit of the suggested construct is that it has a clear schematisation and modular method with partial area occupation. The proposed structure can be used as a fundamental building block to implement any higher order demultiplexer. Therefore, using this structure, an optimal coplanar one to four demultiplexer has been suggested. Using the QCAdesigner simulator, the functionality of the proposed architectures was demonstrated and performance evaluations were provided. Analysis of the
construct is conducted in diverse dimensions to affirm that the suggested layouts generate an acceptable result. Considering the provided comparison, the provided architectures reach better performances in terms of cell count and improvement in the occupation area. In addition, offered one to four demultiplexer shows improvement in QCA cost compared to its
counterparts. Suggested optimal structures can further be used to design higher order demultiplexer to solve the problem of delay using the same concept. Also, in the future, it may lead to the development of demultiplexer-based circuits, especially in nano-communication areas.

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