A comparative TCAD assessment of III-V channel materials for future high speed and low power logic applications

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Abstract. In this work, by means physics based drift-diffusion simulations, three different narrow band gap semiconductors; InAs, InSb and In$_{0.53}$Ga$_{0.47}$As, and their associated heterostructures have been studied for future high speed and low power logic applications. It is observed that In$_{0.53}$Ga$_{0.47}$As has higher immunity towards short channel effects with low DIBL and sub-threshold slope than InSb and InAs. Also it is observed that for the same device geometry InSb has the highest drive current and lower intrinsic delay but its $I_{ON}/I_{OFF}$ figure of merit is deteriorated due to excess leakage current.

1. Introduction
The narrow bandgap III–V semiconductors (InAs, InSb and In$_{0.53}$Ga$_{0.47}$As) have attracted considerable attention as alternative channel materials for beyond silicon logic applications due to their very high electron mobility and saturation velocity. The superior electronic properties of III-V materials translate to favorable logic figure of merits for ultra high-speed and low-power logic applications. This paper endeavors to predict the logic performance of these next-generation digital III-V family materials and present a comparative analysis using physics based two-dimensional drift-diffusion simulator. For the first time in order to investigate the potential of these materials for digital applications they are introduced into the channel of their associated heterostructure devices of similar geometry.

2. Device Structure and Model
Reliability of device modelling is based on accurate physical models and material parameters which are not completely available in the simulator database. As a prerequisite for simulation of devices based on III-V compound semiconductors, material parameters have been obtained through bibliographic review. The physical material parameters for the ternary alloys are obtained from experimental data and vegard’s interpolation schemes from generally accepted values for the binary compounds. Figure 1 shows the vertical band profile of the devices under study. These structures are designed to evaluate the digital performance of specific channel materials and to bring forward an effective comparison. Therefore for the first time the transistors with different channels are modeled with same device geometry. In order to rationale that gate leakage is mostly due to material properties the heterojunctions have type I configuration which confines the holes in the channel and minimizes leakage current [1]. The structures consist of a 10 nm narrow bandgap channel sandwiched between a 4 nm, high bandgap barrier layer and a 0.16 μm thick buffer layer. The device that employs InAs as the primary channel is inserted between In$_{0.53}$Ga$_{0.47}$As sub-channels to realize the lattice-match criteria. Channel charge is supplied through a delta-doped layer at a concentration of $3 \times 10^{12}$ cm$^{-2}$ located in the barrier just below the gate and a spacer layer of 5 nm separates the channel from the barrier to prevent scattering of electrons. The gate length of the devices is 40 nm and gate-source/drain...
separation of 50 nm respectively. The drain is biased at 0.5 V in all simulations unless otherwise stated to reduce overall dc power consumption. The simulation temperature is maintained at 300 K. In order to have a fair analysis, the schottky gate work-function is adjusted for a near e-mode threshold voltage of -0.04 V in all the three devices.

The simulation models are tuned by benchmarking the drain and transfer characteristics with experimental data from [2][3][4]. All the simulations have been performed in SILVACO/BLAZE simulator using physical models accounting for the electric-field-dependent and concentration-dependent carrier mobilities, Shockley–Read–Hall recombination/generation, Selberherr’s impact ionization and the schottky thermionic emission models. The experimental uncertainties were incorporated using interface charge models and S/D resistances. The effect of compressive biaxial strain on InAs and InSb channels due to lattice mismatched heteroepitaxial growth is also incorporated through quantitative bandgap corrections [5] [6].

![Figure 1. Schrodinger-Poisson solutions for conduction band profile of III-V heterostructures](image)

3. Results And Discussion

The drain characteristics plot shows that the extraordinarily high mobility and saturation velocity of InSb translates to remarkable drive current.

![Figure 2. I-V, transconductance and cutoff frequency characteristics](image)

Transconductance measurements show a peak transconductance of 2800 mS/mm for InSb HEMT while InGaAs has maxima at 1336 mS/mm. Although the transconductance of the device is a suitable measure of the device speed, it is more convenient to use the intrinsic delay as the figure of merit. We have investigated the intrinsic delay of the device by measuring the cutoff frequencies through S-parameter simulation. InSb reports the highest cutoff frequency (0.89 THz) and therefore the least delay time of 0.179 ps. This simulation results suggests that THz frequency response may be possible with nanoscale InSb HEMTs. Therefore InSb turns out to be a capable candidate for ultra high-speed logic devices [7].
Furthermore, a typical curve of drain current versus gate voltage ($V_G$) in logarithmic scale is plotted in figure 3 to present the various device metrics. The inset in the figure shows the evaluation methodology undertaken in the study proposed by R.Chau et.al and successfully demonstrated in various III-V logic devices. The sub-threshold slopes are relatively similar for the three devices with InSb showing the highest sub-threshold slope confirming poor short channel effects. As shown in Figure 3, InAs and InSb FETs exhibit DIBL=108 mV/V and 204 mV/V respectively, whereas, for InGaAs FETs DIBL=55 mV/V, thereby showing immunity to logic degradation. The increase in DIBL and SS of InSb is due to their high channel dielectric constant and low effective mass that enhances potential barrier lowering. However, InSb exhibits the highest ON-current (324 mA/mm) due to relatively high electron velocity $v_{sat}=5 \times 10^5$ m/s and mobility of 78000 cm/Vs.

![Figure 3. Sub-threshold and DIBL characteristics of the three devices](image)

Although the three devices have shown high ON state current and intrinsic delay, the device performance is dictated by the leakage current behavior. The parameters that determine gate leakage are the schottky barrier height, bandgap, conduction band offset, dielectric constant of the barrier and channel dielectric constant. In InAs HEMT, the InGaAs sub-channel forms an additional barrier for the tunneling electrons and holes in InAs channel reducing the leakage current. The leakage and SCE analysis is carried out by measuring the electric field in the gate and channel regions. A large channel dielectric constant results in the electric field penetrating the channel that causes severe performance degradation [8]. The electric field profile along the channel of the three devices is represented in figure 4. InSb shows the highest peak electric field. Because of the strong variation of the electric field along the heterojunction interface impact ionization occurs near the drain end causing additional leakage current and SCEs [9]. Also the increased electric field at the gate edges decreases the tunneling barrier width and increases the gate leakage current [10]. The fringing field distribution profile is obtained using a cutline at few angstroms distance below the gate. This needle-shaped electric field is a function of the dielectric constant of the barrier which is highest for AlInSb (16.6).

The chart in figure 5 shows the gate leakage current, the sub-threshold OFF current and the total leakage current. Although the ON current of InSb is the highest among the III-V digital materials, the excess leakage current degrades the $I_{ON}/I_{OFF}$ figure of merit as shown in figure 4. This high leakage current in InSb is attributed due to low confinement in the channel, low bandgap, reduced barrier height and high dielectric constant of the channel and barrier materials causing high field effects as shown in figure 4. The author is aware that the resulting leakage current does not include a complete current leakage assessment, and therefore the OFF state current predictions should be considered as lower limit estimate. The effects of band-to-band tunneling (function of bandgap) are not activated in the simulation which can further magnify the leakage current.
4. Conclusion
As a concluding note, the various figure of merits of the three devices are summarized in table 1.

Table 1. Summary of figure of merits

| Channel      | SS (mV/dec) | DIBL (mV/V) | $I_{on}/I_{off}$ ($\times 10^4$) | $f_t$ (GHz) | T (ps) | V$_{cc}$ (V) |
|--------------|-------------|-------------|---------------------------------|-------------|--------|--------------|
| In$_{0.53}$Ga$_{0.47}$As | 84          | 55          | 2.0                             | 422         | 0.377  | 0.5          |
| InAs         | 88          | 108         | 3.1                             | 640         | 0.248  | 0.5          |
| InSb         | 94          | 204         | 0.5                             | 890         | 0.179  | 0.5          |

References
[1] Desplanque L, Vignaud D, Godey S, Cadio E, Plissard S, Wallart X, Liu P and Sellier H 2010 J. Appl. Phys. 108 043704
[2] Kim D H, del Alamo J A, IEEE IEDM 2007 629
[3] Ashley T, Barnes A R, Buckle L, Datta S, Dean A B, Emery M T, Fearn M, Hayes D G, Hilton K P, Jefferies R, Martin T, Nash K J, Phillips T J, Wilding P J and Chau R, ICSICT 2004 3 2253
[4] Vasallo B G, Wichmann N, Bollaert S, Roelens Y, Cappy A, Gonzalez T, Pardo D and Mateos J, IEEE Transactions on Electron Devices 2007 54 2815
[5] Luisier M, Neophytou N, Kharche N and Klimeck G, IEEE IEDM 2008 1
[6] Kasturiarachchi T, Brown F, Dai N, Khodaparast G A, Doezema R E, Chung S J and Santos M B, Applied Physics Letters 2006 88 171901
[7] Serge Oktyabrsyky, Peide Ye, “Fundamentals of III-V Semiconductor MOSFETs,” Springer, 2010 and references therein.
[8] Oh Saeroonter, Ph.D dissertation, 2010
[9] Christian H, Buchali F, Prost W, Brockerhoff V, Fritzsche D, Niskel H, Losch R, Schlapp W, Tegude F J IEEE Transactions On Electron Devices 1994 41 1685
[10] Sathaiya D M and Karmalkar S IEEE Transactions On Electron Devices 2007 54 2614