A self-adaptive blanking time circuit for fast IGBT De-saturation Short-circuit protection

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Abstract This paper proposed a self-adaptive blanking time (SABT) circuit for fast IGBT de-saturation short-circuit detection. When IGBT normally turns on or experiences fault under load (FUL), the blanking time is determined by detecting gate voltage \( V_{GE} \). While when IGBT is under hard switching failure (HSF), the blanking time is determined by detecting gate voltage \( V_{GE} \). The simulation with the UMC 0.6 \( \mu m \) 700 V technology indicates that the proposed SABT circuit can quickly detect FUL and HSF. Compared to the conventional blanking time circuit, the SABT circuit can shorten the fault detection time of FUL from 1.3 \( \mu s \) to 35.5 ns, while the fault detection time of HSF condition is reduced from 2.329 \( \mu s \) to 294 ns.

key words: blanking time, IGBT, de-saturation short-circuit protection

Classification: Power devices and circuits

1. Introduction

Insulate gate bipolar transistor (IGBT) is the key component in the power system, which could be used in a range of several hundred volts to several thousand volts. Power devices are considered as the most fragile components in the power system, and will experience extreme conditions during the long-term wear-out [1, 2]. Therefore, monitoring and predicting failure are always carried out to effectively improve reliability and prolong the life span of IGBTs [3].

Short-circuit protection is one of the most concerns in IGBT applications where IGBTs withstand high current, high voltage and overheat [4]. In previous works, numerous short-circuit detection methods have been reported, such as gate voltage pattern, \( \frac{di}{dt} \) detection, collector current detection and de-saturation detection. The first method is based on gate voltage pattern detection. This method could be divided into two categories: Miller plateau analysis and \( V_{GE} \) monitoring.

Miller plateau analysis can detect short-circuit condition according to the relationship of Miller plateau voltage and collector current [5, 6]. For \( V_{GE} \) monitoring [7-10], when IGBT turns on under hard switching failure (HSF), the Miller plateau would not exist in gate voltage turn-on transient. While fault under load (FUL) occurs, the gate voltage of IGBT can suddenly increase higher than the power supply voltage. These methods can detect short-circuit conditions very fast.

The second one is based on \( \frac{di}{dt} \) detection [11-14]. Kelvin emitter (\( E' \)) is introduced to reduce the power loop oscillation effect on the drive circuit. There is a stray inductance \( L_{EE'} \) between the power emitter (\( E \)) and Kelvin emitter (\( E' \)). When the collector current suddenly changes, \( \frac{di}{dt} \) will induce a voltage drop \( V_{EE} \) across \( L_{EE'} \). The collector current slope under short-circuit is greater than that under normal operation. Thus, when \( V_{EE} \) is larger than the reference voltage, the IGBT is regarded as in short-circuit condition.

The third one is based on collector current detection. The collector current could be measured by shunt resistors [15], current sense-IGBT [16], the parasitic inductance of IGBT [17, 18], Hall sensor, Rogowski coil [19], and current transducer [20]. Shunt resistors are only suitable for low power applications due to the additional power loss, and its accuracy would be affected by parasitic inductance and temperature. Current mirror sense-IGBT is co-packaged with the main IGBT module, which released by Fuji Electrical. Hall sensor, Rogowski coil and current transducer are based on electromagnetic principle. They are usually in large size and hard to assemble in the planar bus-bar. In [21] and [22], printed circuit board Rogowski coil has been proposed to detect collector current.

The last one is de-saturation detection [23-27], which has been used in many commercial products. It is regarded as a highly reliable method. This method compares collector-to-emitter saturation voltage \( V_{CE,sat} \) with a reference voltage during IGBT on-state. However, during the IGBT’s turn-on transient, the collector-emitter voltage \( V_{CE} \) falls down from bus-bar voltage \( V_{bus} \) to \( V_{CE,sat} \). Therefore, blanking time is needed to avoid false triggering. M. Chen group proposed a self-adaptive blanking circuit for IGBT short-circuit protection based
on $V_{CE}$ monitoring where a fixed delay time unit still exists to cope with the hard switching failure [24, 25].

This paper introduces an improved self-adaptive blanking time circuit. When IGBT normally turns on, the blanking time is determined by detecting the variation of $V_{CE}$. While when IGBT is under HSF condition, the blanking time is determined by detecting $V_{GE}$. After the blanking time, a transmission gate is opened to enable short-circuit detection by comparing $V_{DESAT}$ with a reference voltage.

In section 2, the required blanking time and the conventional method are introduced. In section 3, the operational mechanism of the proposed circuit is discussed. In section 4, the simulation results are shown and discussed. Conclusions are given in section 5.

2. The blanking time analysis and $V_{CE}$ short-circuit detection method

The IGBT turn-on transient is shown in Fig. 1. The minimum blanking time is supposed to be the sum of $t_1$, $t_2$, and $t_3$ [24]. In the following, each period of the blanking time and relevant factors will be discussed.

![Fig. 1. IGBT turn-on transient and the minimum blanking time.](image)

1. In $t_1$ region, IGBT doesn’t conduct current. The gate current $I_G$ charges input capacitances $C_{GE}$ and $C_{GC}$, and $V_{GE}$ rises to threshold voltage $V_{GE,th}$ at a constant rate [28].

$$t_1 = R_G \times (C_{GC} + C_{GE}) \times \ln \left( \frac{V_{CC}}{V_{CC} - V_{GE,th}} \right)$$  \hspace{1cm} (1)

Where $R_G$ is the gate resistor, and $V_{CC}$ is the power supply voltage.

2. In $t_2$ region, as $V_{GE}$ raising over $V_{GE,th}$, the collector current begins to conduct. The collector current finally increases to the correspondent Miller plateau voltage when the collector current $I_C$ equals to $I_L$.

$$I_C = \frac{I_D}{1 - \alpha_{pnp}} = \frac{\mu_n C_{ox} W}{2 \times (1 - \alpha_{pnp})} \left( V_{GE} - V_{th} \right)^2$$  \hspace{1cm} (2)

$$V_{GE,L} = \sqrt{\frac{2I_L (1 - \alpha_{pnp})}{\mu_n C_{ox} W}} + V_{th}$$  \hspace{1cm} (3)

$$t_2 = R_G \times (C_{GC} + C_{GE}) \times \ln \left( \frac{V_{CC} - V_{GE,th}}{V_{CC} - V_{GE,L}} \right)$$  \hspace{1cm} (4)

Where $V_{th}$ is the threshold voltage of the MOS transistor, $\alpha_{pnp}$ is the common-base current gain, $\mu_n$ is the electron mobility, $C_{ox}$ is the gate oxide capacitance of the MOS transistor, $V_{GE,L}$ is the gate voltage when $I_C$ equals to load current. Combining Eq. (2) and Eq. (3), $t_2$ could be given by Eq. (4).

3. In $t_3$ region, $V_{CE}$ decreases to saturation voltage $V_{CE, sat}$ rapidly. The displacement current caused by $V_{CE}$ variation cancels out the gate charging current. $V_{GE}$ remains constant during $t_3$, which is called Miller plateau voltage $V_{GE, MP}$. The period $t_3$ is given by following,

$$t_3 = R_G \times \frac{C_{GC}}{V_{GE, MP}} \times \frac{V_{CC} - V_{DESAT}}{V_{CC} - V_{CE, sat}}$$  \hspace{1cm} (5)

According to the above analysis, the blanking time is related to the gate resistor $R_G$, the input capacitance of IGBT modules $C_{ox}$, load current $I_L$, bus-bar voltage $V_{bus}$, temperature, etc. Fig. 3 shows the required minimum blanking times of two IGBT modules under different

![Fig. 2. The equivalent circuit of an IGBT module.](image)

![Fig. 3. The required minimum blanking time in different situations.](image)
situations. The input capacitances of CM400DY-12 and IXXN110N65C4H1 are 40 nF and 5.5 nF, respectively. Therefore, the minimum blanking time of CM400DY-12 is longer than that of IXXN110N65C4H1. As shown in Fig. 3 (a), the minimum blanking time increases with the increased bus-bar voltage. In Fig. 3 (b), the minimum blanking time becomes longer as $R_G$ increasing. The results agree with the above analysis.

The conventional blanking time is implemented by using a constant current $I_{ons}$ to charge an external capacitor $C_b$ when IGBT turns on [29], but the fixed blanking time is not suitable for all situations. Besides, the slope of the detection voltage is limited by the charging speed of the external capacitor $C_b$. Therefore, the detection voltage can’t quickly follow the variation of $V_{CE}$ when $V_{CE}$ changes fast under FUL condition.

The blanking time is critical for short-circuit detection. If blanking time is longer than expected, the IGBT needs to withstand high current for more time under HSF or FUL. In contrast, if blanking time is shorter than the expected, $V_{CE}$ doesn’t reduce under the reference voltage within the blanking time, then false triggering will occur.

3. The proposed self-adaptive blanking time circuit

Hard switching fault (HSF) and fault under load (FUL) are two frequently happened short-circuits in power systems. All protection circuits should consider both two short-circuit conditions. HSF means short-circuit happens before the IGBT turns on. When IGBT turns on, collector current rapidly increases to a large value. The Miller plateau doesn’t exist in $V_{GE}$ turn-on transient. Besides, $V_{CE}$ remains near the bus voltage. FUL happens during the on-state where IGBT normally turns on first, then short-circuit occurs, $V_{CE}$ rapidly increases from $V_{CE\text{,sat}}$ to $V_{bus}$, and $V_{GE}$ raised above the $V_{CC}$ [30].

![Fig. 4. IGBT fault behavior under two types of short-circuit: (a) are waveforms under HSF, (b) are waveforms under FUL [30].](image)

Fig. 5 is the block diagram of the proposed circuit. The proposed circuit is divided into two modules by function: the blanking time generation module and short-circuit detection module. The blanking time generation circuit can facilitate a self-adaptive blanking time and generate a signal to enable the short-circuit detection after the blanking time. When IGBT normally turns on, the blanking time is determined by detecting the variation of $V_{CE}$. While when IGBT is under HSF condition, the blanking time is determined by detecting $V_{GE}$.

The short-circuit detection module is used to detect the short-circuit condition by using U3 to compare $V_{DESAT}$ with a reference voltage $V_{REF3}$. The $V_{DESAT}$ is connected to the collector of IGBT through a transmission gate TG2 and a high voltage diode $D_i$. After the blanking time, TG2 is opened to enable short-circuit detection.

In the following, the operational mechanism of the proposed circuit for different failure conditions will be discussed in detail.

3.1 Operational mechanism for normal operation and FUL condition

For normal operation and FUL, IGBT normally turns on first. A self-adaptive blanking time is implemented by detecting the variation of $V_{CE}$. The waveforms of the proposed circuit under FUL are shown in Fig. 6.

Initially, TG1 is open, $V_{BE}$ is larger than $V_{CC}$, and $V_{CE\text{,sat}}$ maintains at $V_{CC} + V_{FED1}$. During the turn-on transient, $V_{CE}$ reduces from $V_{bus}$ to smaller than $V_{CC} – V_{FED1}$, $V_{CE\text{,sat}}$ equals to $V_{CC} + V_{FED1}$. $V_{CE\text{,sat}}$ follows the variation of $V_{CE}$. $R_1$, $R_2$, and $C_1$ consist of an RC filter. The output of the RC filter $V_{RC}$ is the time derivative of $V_{CE\text{,sat}}$. $V_{RC}$ is a pulse during the $V_{CE}$ variation period. Comparator U1 is used to reshape the pulse $V_{RC}$. When the rising edge of $V_{O1}$ arrives, D flip flop sets $V_Q$ to high, which means $V_{CE\text{,sat}}$ already reduced to $V_{CE\text{,sat}}$. TG1 is closed while TG2 is opened so that short-circuit detection is enabled. When the input control pulse $V_{E\text{,q}}$ returns to a low level, D flip flop is reset. TG1 is opened, TG2 is closed again, and the short-circuit detection is disabled.

3.2 Operational mechanism for HSF condition

For the HSF condition or short-circuit during turn-on transient, the variation of $V_{CE}$ cannot be useful because $V_{CE}$ remains near bus-bar voltage and $V_{CE\text{,sat}}$ maintains at $V_{CC} + V_{FED2}$. Therefore, $V_{O1}$ remains high, the blanking time automatically switches to be implemented by detecting $V_{GE}$. A complementary comparator U2 is used to compare the gate voltage $V_{GE}$ with the reference voltage $V_{REF2}$, where $V_{REF2}$ is equal to $V_{CC} – V_{thp}$, and $V_{thp}$
is the threshold voltage of PMOS in the UMC fabrication process. The $V_{CE}$ is supposed to less than short-circuit threshold voltage $V_{REF3}$ when $V_{GE}$ raises to $V_{CC} - V_{th}$ during normally turn-on transient. Thus, it’s regarded as short-circuit if $V_{DESAT}$ is larger than $V_{REF3}$ when TG2 opens at $V_{GE} > V_{REF2}$. As shown in Fig. 7, when the short-circuit detection module is enabled, $V_{DESAT}$ immediately changes to $V_{CC} + V_{F,DS}$, and short-circuit signal $V_{SC}$ is set to high.

4. Simulation verification

The proposed circuit was built on the UMC 0.6 μm 700 V BCD process. Simulation is carried out in Cadence Spectre to verify the feasibility. A double pulse test bench is build up to test the proposed circuit. A gate driver with the conventional blanking time circuit is also simulated for comparison.

4.1 Simulation results under FUL condition

In Fig. 8, a short-circuit condition is added to the circuit under test by connecting the collector of the IGBT to the bus-bar directly at 70 μs. In Fig. 8 (a), when $R_G$ changes from 10 Ω to 50 Ω, the blanking time $t_b$ changes from 382.7 ns to 938.5 ns. When short-circuit happens, $V_{DESAT}$ raises to power supply voltage $V_{CC}$ immediately, and $V_{SC}$ is set to high within 35.5 ns. Fig. 8 (b) shows the waveforms of the conventional circuit for comparison. When FUL occurs, $V_{DESAT}$ gradually increases because the slope is limited by charging the external capacitor. The detection time of the conventional circuit is 1.3 μs.

4.2 Simulation results under HSF condition

Fig. 9 shows simulation waveforms under the HSF condition. Short-circuit exists from the beginning, and IGBT turns on under the short-circuit condition at 56 μs. When $R_G$ changes from 10 Ω to 50 Ω, the blanking time $t_b$ of the proposed circuit changes from 294 ns to 870.4 ns in Fig. 9 (a). The short-circuit condition is detected after the required minimum blanking time. For the conventional circuit, the blanking time is constant. Therefore, IGBT modules have to withstand high current for 2.329 μs in Fig. 9 (b).
Fig. 8. Simulation waveforms under FUL with different \( R_G \): (a) and (b) are the waveforms when IGBT normally turns on given by the proposed circuit and conventional circuit, respectively. (c) and (d) are the waveforms when short-circuit happens given by the proposed circuit and conventional circuit, respectively.

Fig. 9. Simulation waveforms under HSF with different \( R_G \): (a) is the waveforms of the proposed circuit, (b) is the waveforms of the conventional circuit.

5. Conclusion

This paper introduced a self-adaptive blanking time generation circuit. It’s implemented by detecting \( V_{CE} \) variation and gate voltage \( V_{GE} \). This blanking time circuit will be useful to effectively reduce the withstand time when IGBT suffers short-circuit, and improve the reliability of the de-saturation short-circuit detection. The simulation is carried out under a 0.6 \( \mu m \) 700V BCD process. The simulation results indicate the proposed SABT circuit can reduce detection time from 2.329 \( \mu s \) to 0.294 \( \mu s \) under HSF condition, while detection time reduces from 1.3 \( \mu s \) to 35.5 ns under FUL condition.

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