Low Stray Inductance Busbar Design and Optimization for SiC-Based Three-Level Device

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Abstract. In this paper, the sensitivity of switching-off voltage spikes of SiC MOSFET and Si IGBT to stray inductance at the same voltage and current levels is compared and analyzed. The influence of the geometric structure of simple stacked busbar on its stray inductance is analyzed and the general guiding principle of busbar design is given. Aimed at the three-level circuit topology involved in this project, based on the analysis of its working principle and commutation circuit, the stray inductance network of stacked busbar is successfully extracted with the help of finite element simulation software ANSYS Q3D, and the idea of optimizing stray inductance of maximum commutation circuit is putted forward. A set of three-level AC-DC-AC power electronic device is designed, and a series of iterative optimization design and optimization results analysis of the busbar of the device are made.

1. Introduction

With the development of power electronic technology towards high frequency and high energy density, many shortcomings of traditional power electronic devices represented by silicon devices are gradually exposed, which can not meet the development needs of the industry. At the same time, new power electronic devices represented by silicon carbide devices have attracted more and more attention due to their advantages of low loss, high temperature resistance, high switching speed etc. Literature[1-2] systematically compares and analyzes the device characteristics of the two materials under the same voltage and current levels. The advantages of silicon carbide MOSFET in high frequency and high power are analyzed and verified. The disadvantages of large conduction voltage drop, serious oscillation of switching voltage and current waveforms and sensitivity to stray parameters of the circuit are pointed out.

In order to reduce the adverse effects of parasitic inductance on silicon carbide devices, the busbar design of the device is particularly important. Many achievements have been made in the study of busbar at home and abroad. Literature [3] shows that the position of vias on the busbar has a great influence on the stray inductance. If vias change the current direction or the vias are near the edge of the busbar, they will have a great influence on the inductance. Literature [4] explains the busbar design and inductance analysis of an H bridge in detail. Literature [5] analyzes the current distribution in different current flows of the three-layer busbar and gives a design scheme of the three-level device and the selection principle of the device, which has very good guiding significance. Document [6] proposes a concept of layer reduction busbar. Although this scheme can reduce the busbar stray inductance, it will make the whole
device more difficult to manufacture. Document [7] proposes that the busbar can be divided into internal inductance $L_i$ and external inductance $L_e$ according to its stray inductance generation mechanism, in which the internal inductance is generated by flux linkage and is related to frequency. The external inductance is determined by the geometry of the busbar and is independent of frequency. Document [8] gives the design process and general design principles of inverter busbar, which has high reference value.

2. Comparison of SiC and Si Devices

2.1 Double pulse test Circuit

The double pulse test circuit is shown in the following fig.1. The upper tube Q2 is turned off, and the gate drive of the lower tube Q1 is added with double pulses. At time $t_0$, the gate of the lower tube sends out the first pulse, and the tested tube is saturated and turned on. The DC voltage $U$ is applied to the load inductance $L_1$. According to the following expression, the inductance current rises linearly. When the two quantities $U$ and $L$ are determined, we can control the load current at times $t_1$, $t_2$ and $t_3$ by controlling the time length $\Delta t$.

$$I = \frac{U \times \Delta t}{L_1} \quad (1)$$

At time $t_3$, the switching tube Q1 is turned off again. At this time, the load current is already large. Due to the presence of the stray inductance $L_s$ of the busbar, a voltage spike is generated across Q1, which may cause the tube to be damaged.

![Figure 1. Schematic diagram of double pulse test.](image1)

![Figure 2. Waveform of double pulse test.](image2)

2.2 Comparison of experimental results

In order to compare the sensitivity of SiC MOSFET and Si IGBT to stray inductance, the SiC MOSFET half-bridge module CAS300M17BM2 (CREE) and the silicon half-bridge module FF300R17KE4 (Infineon) are selected in this paper. Double-pulse test of the two modules are built on the Simplorer software platform under ANSYS. The commutation loop stray inductance $L_s$ takes 100nH; Load inductance $L_{load}$ takes 30nH.

| Voltage and current level | FF300R17KE4 (Si) | CAS300M17BM2 (SiC) |
|---------------------------|------------------|--------------------|
| 600V/200A                | 155V             | 198V               |
| 600V/300A                | 246V             | 300V               |
| 800V/200A                | 165V             | 210V               |
| 800V/300A                | 252V             | 303V               |

From the experimental results, we can see that under the same voltage and current level, the overshoot voltage at both ends of SiC MOSFET is significantly larger than that of Si IGBT and increases with the DC voltage level and turn-off current getting larger, which brings great challenges to the application of SiC devices. In the actual device design process, when the selected tube type, capacitance, inductance and other devices are determined, the stray inductance value brought by them cannot be changed. At this time, the only part that we can optimize is the connection busbar, which puts forward urgent requirements for the design of low stray inductance busbar.
3. **Optimal Design Principles for Simple BusBar**

As shown in the following figure, two laminated busbars with a length of 200mm and a width of 100mm were built in ANSYS Q3D, and the upper and lower conductive layers were connected with copper bars to simulate connection terminals. The red end is the positive electrode, and the distance from the left side of the positive busbar is $Y_1$; The green end is negative and the distance from the left side of the negative busbar is $Y_2$. Parameter scans on $Y_1$ and $Y_2$ are set in Q3D to observe the trend of the stray inductance of the busbar changing with the position of the terminals.

![Figure 3. Simple representation of the busbar.](image1)

From the scanning results, when the upper and lower terminals overlap and are centered, the stray inductance is the smallest. This is because the current flows in the upper and lower conductive layers are opposite, and the generated magnetic fields cancel each other out, thus reducing the external comprehensive stray inductance. It is concluded that when designing the busbar, the overlap ratio of the upper and lower currents in the converter circuit should be increased as much as possible, and the length of the converter circuit should be reduced. As shown in the figure5, when the terminals are placed in the center, the actual effective current flow path is the shortest and the stray inductance is the smallest. The following figure establishes a busbar structure with $L$ length, $W$ width and $h$ spacing between the upper and lower insulating layers. Document [9] gives an analytical expression for the length and width of a simple laminated busbar.

![Figure 4. Parameters Scan Results.](image2)

![Figure 5. Surface current distribution.](image3)

![Figure 6. Physical representation of busbar.](image4)

![Figure 7. Main circuit configuration of three-level topology.](image5)
\[ L_{\text{planar}} = \mu_0 \mu_r \frac{Lxh}{W} \]  
(2)

\( \mu_0 \): Permeability of Insulating Medium in Vacuum.
\( \mu_r \): relative permeability of Insulating Medium.

It can be seen that the stray inductance of the laminated busbar is equivalent to countless tiny inductors connected in series in length and parallel in width. As the thickness of the insulating layer decreases, the more the magnetic fields cancel each other out, and thus the smaller the stray inductance. The paper also shows that the best aspect ratio of the busbar is between 1 and 2, which is beneficial to reduce inductance and also takes the manufacturing cost of the busbar into account.

3.1 Analysis of converter circuit

Figure 6 is the main circuit configuration of three-level topology. Take DC-AC terminal as an example. When T51 and T52 are turned on and T81 and T82 are turned off, the voltage between point A and point O is \( \frac{U_{dc}}{2} \); When T51 and T52 are turned off and T81 and T82 are turned on, the voltage is \( -\frac{U_{dc}}{2} \); when T51 and T62 are turned off, the voltage is 0. In the third case, T52 and T61 cannot be turned on or off at the same time, and which tube is turned on is determined by the current direction of the load, thus realizing the three levels of point A (\( \frac{U_{dc}}{2} \)、\( -\frac{U_{dc}}{2} \)、0).

3.2 Analysis of basic Commutation loop

![Diagram](image)

3.1 Analysis of converter circuit

![Diagram](image)

4. Design and Optimization of Three-level Busbar

4.1 The specification of the device is as follows:
- Rated input voltage: 1200V rms
- Rated input current: 150A rms
- Switching frequency: 1KHz
- MOSFET module rating: 1700V, 325A
Dimensions: 850×475×150mm (L×W×H)

Water Cooling

Figure 12. Overall view of the device.

Figure 13. Details of busbar (a) and (b)

As shown in the figure 14, Loop1 is the maximum commutation loop of the three-level circuit. So loop1 is the most concerned and it's the direction of busbar optimization. Figure 15 shows the actual current flow path of the device. Current flows between different layers and is connected by capacitors and modules of the circuit to form the whole circuit. In Q3D software, the current source and current sink are sequentially set at each interface terminal of the loop1 as shown in figure 15 to extract the busbar stray inductance. Figure 16 shows the current distribution of the busbar on its surface and the simulation results are shown in the table 2.
Table 2. Simulation results of stray inductance of busbar.

| Freq:100(MHz) | S1     | S2     | S3     | S4     |
|--------------|--------|--------|--------|--------|
| S1           | 28.065 | -6.2085| -6.1062| -1.7621|
| S2           | -6.2085| 19.039 | 4.5822 | -12.529|
| S3           | -6.1062| 4.5822 | 29.671 | -24.41 |
| S4           | -1.7621| -12.529| -24.41 | 58.241 |

From simulation results: the elements on the main diagonal are the self-inductance of each part of the busbar, the other elements are mutual inductance, the self-inductance is positive, the mutual inductance is mostly negative, only a few are positive but the value is not large. The effect of laminated busbar greatly reduces the total inductance value.

4.2 Optimized Busbar 1st Edition:

Analyzed from the converter circuit, the maximum commutation loop is between the positive layer and the zero layer, while the laminated busbar of the device places the two layers of busbar in the outermost layer, thus increasing the insulation thickness. According to the formula(2), it is essential to reduce the insulation thickness, so the zero layer and the negative layer are interchanged.

4.3 Optimized Busbar 2nd Edition:

In order to reduce the self-inductance 58.241nH(table2) of the path of I4 (figure15), it is necessary to reduce the length of the path as much as possible, which is limited to the determination of module selection and the heat dissipation of the whole device. The distance between modules cannot be simply shortened, otherwise the module will be damaged due to unsatisfactory heat dissipation. We must find another way to restructure the placement of the modules. The modules with drive plates are placed in both sides and the modules without drive plates are placed in the middle. In this way, the width W of the busbar can be reduced. Although the length of the busbar is increased, it has little influence on the stray inductance of the circuit.

4.4 Optimized Busbar 3rd Edition:

In order to reduce the inductance of the path of I4, the capacitor is inverted on the busbar, which is conducive to reducing the length of the maximum stray inductance path without changing the placement of the module on the water cooling plate to prevent other parts from being affected. In addition, in order to minimize the stray inductance of the whole commutation loop, the small busbars cannot be ignored. Judging from the above simulation results, the proportion of this part in the whole circuit is not small, so the three small busbars are widened to the greatest extent without changing the structure of the module, which has no effect on the heat dissipation of the system. The results of all the above iterative designs is summarized in table3.
Table 3. Simulation result of the four version busbar.

| Busbar Version      | Stray inductance (nH) |
|---------------------|-----------------------|
| Original edition    | 42.13                 |
| Optimized 1st Edition | 42.10             |
| Optimized 2nd Edition | 57.70             |
| Optimized 3rd Edition | 37.79             |

Compared with the original version, the Optimized 1st edition didn’t reduce the stray inductance significantly after reducing the insulation distance between the two layers of the converter circuit. The reason is that the overlapping degree of converter path I2, I3 and path I4 is very low, and the magnetic field formed is not obviously offset, so it didn’t been optimized after reducing the insulation distance. For the Optimized 2nd edition, although the width W of the mother row is reduced and the stray inductance of the path I4 is obviously optimized, the small busbars must be changed after the placement position of the modules is changed, so that the stray inductance contribution rate of the small busbar in the whole circulation loop is obviously increased, which leads to the increase of the overall stray inductance and the failure of the scheme. For the Optimized 3rd edition, after absorbing the experience of the second and third editions, it is decided to widen the small busbars to the greatest extent to reduce its contribution rate in the commutation loop while keeping the placement position of the module unchanged. Secondly, the capacitor is closed to the module and inverted on the upper layer of the busbar, which is conducive to fully reducing the commutation loop length from the capacitor terminal to the module terminal, thus achieving the purpose of overall stray inductance optimization.

5. Conclusion
Firstly, after comparing the performances of SiC devices and Si devices, it is found that the SiC devices are more sensitive to the stray inductance of the commutation loop. It is in this way that higher requirements are put forward for special buses for SiC devices. Secondly, the design of general busbar is fully analyzed, and on the basis of previous research results on busbar, the general guiding principles of busbar design are given. Then, aimed at the three-level neutral point clamped topology involved in this project, the basic working principle of the circuit and the commutation loop are analyzed, which provides a theoretical basis for the next busbar optimization. At last, the iterative optimization process of the whole device in this project is given. For the two failed version, the reasons are analyzed, and the optimization is successfully carried out with full consideration of the mechanical, geometric, heat dissipation and other limitations of the actual power electronic device design. The whole analysis and design process of this article can provide a good reference for peers.

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