Two-phase low-power analogue CMOS peak detector with high dynamic range

E Malankin
National Research Nuclear University MEPhI (Moscow Engineering Physics Institute), Kashirskoe highway 31, Moscow, 115409, Russia
ezmalankin@mephi.ru

Abstract. A low-power two-phase peak detector with wide dynamic range was developed. The PD was designed on the basis of the CMOS UMC 180 nm process. This block is considered as a part of the read-out electronics of the CBM experiment at upcoming FAIR accelerator (Germany). Peak detector has the following advantages: wide dynamic range of 5 – 1000 mV, low power consumption of 500 µW. The designed PD meets the requirements to the muon chamber read-out electronics of the CBM experiment. Due to the area efficiency (100x90 µm²) and low power consumption it can be used in different applications for high-energy physics read-out electronics.

1. Introduction
The conventional analog peak detector (PD) architecture [1] is built basically on the operational amplifier (figure 1). The OpAmp charges the hold capacitance, when the input voltage is higher than the output voltage. However, when the input voltage becomes lower, the hold capacitance is not discharged, because the feedback diode is reverse-biased. In the CMOS peak detectors current source on a MOS transistor is used as a rectifying element instead of the diode in the high gain OpAmp feedback loop a [2].

Figure 1. Conventional peak detector.
Figure 2. Two-phase peak detector.
In the multi-channel detector read-out systems the two-phase configuration (figure 2) is usually applicable. In this configuration the drawbacks of the classical PD structure are eliminated [3]. In particular, the two-phase configuration has the following advantages:

- absence of the input offset voltage (i.e. the accuracy is not limited by the input offset voltage of the OpAmp);
- common-mode errors have no influence on the accuracy;
- the influence of the input transistors process mismatch is decreased.

An additional requirement set to the peak detector in the muon read-out system in the CBM experiment is the low power consumption (no more than 1 mW), area size of $100 \times 150 \mu m^2$, dynamic range of $5 - 500 mV$ with negative polarity and regular occupancy no less than 0.3 MHz[4].

2. Peak detector schematic and layout

2.1. Peak Detector schematic and simulation
The design was carried out on the basis of the UMC technological libraries with 180 nm design rules. Cadence company software packages were used for schematic development and simulations.

The main block of the two-phase PD is the OTA (figure 3). That amplifier corresponds to the requirements on power consumption and dynamic range. The OTA is optimized for the operation with negative polarity signals with amplitudes in the range of $5 - 500 \ mV$. This range corresponds to the output signals of the shaper in the channel of the muon chambers readout.

![Figure 3. Transconductance operational amplifier.](image)

In figure 4 the schematic of the designed two-phase peak detector is given. This schematic consists of the OTA, rectifying current mirror, hold capacitor, reset scheme, «Peak Find» signal scheme, and analog gates to switch between the “read” and “write” phases.
During the simulation the main parameters of the two-phase peak-detector were obtained. In figure 5 the functional diagram of the designed peak detector is shown.

Figure 4. Two-phase peak detector schematic.

Figure 5. PD functional diagram.
The transfer function is linear all over the input signals range. The whole dynamic range of the peak detector is $5 - 1000$ mV (figure 6). As to the Monte-Carlo analysis the distribution of the PD output peak value due to the process variations is no more than 0.3% at 100mV input signal (figure 7).

2.2. Peak detector layout
PD layout (figure 8) was designed according to the UMC 180 nm process rules. The area of the Peak Detector is $100 \times 90 \ \mu m^2$. Here the 100 µm – is the height of the peak detector, which is in correspondence to the analog channel height standard in the read-out electronics for the muon system of the CBM experiment.

Figure 6. PD transfer function.

Figure 7. Distribution of the output peak value.

Figure 8. Two-phase peak detector layout.
As a result of the development there was designed the low-power peak detector which could be used as a part of the readout electronics for the muon chambers. The obtained parameters are listed in table 1.

| Parameter                      | Specification | Simulation |
|--------------------------------|---------------|------------|
| Input signal dynamic range, mV | 5–500         | 5–1000     |
| Die size, µm²                  | 100x150       | 100x90     |
| Regular occupancy, MHz         | 0.3           | 0.4        |
| Power consumption, mW          | 1             | 0.55       |

Table 1. Parameters of the peak detector.

3. Conclusion
The low-power analog peak detector with a wide dynamic range for readout electronics for the muon chambers of the CBM experiment was designed. It was developed on the basis of the UMC 180 nm MMRF CMOS process. The peak detector meets the requirements to the readout electronics for the muon chambers of the CBM experiment.

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