Modeling and design of a Mott selector for a ReRAM-based non-volatile memory cell in a crossbar architecture

Mohammadreza Farjadian1 · Majid Shalchian1

Received: 2 July 2021 / Accepted: 17 January 2022 / Published online: 14 February 2022
© The Author(s), under exclusive licence to Springer Science+Business Media, LLC, part of Springer Nature 2022

Abstract
In this work, we developed a model for a nonvolatile memory cell based on the electrical model for a TiOx/HfOx ReRAM cell and the hybrid electrothermal model of a VO2 Mott selector developed recently by our team. Both models have been calibrated and validated with experimental data, and the operating characteristics of a one-selector-one-ReRAM (1S1R) memory cell has been studied. The length of the selector layer was varied as a design parameter to meet the design requirements for proper read, write, and erase operations. Simulation results suggest that the modified selector cell with 60 nm length of the VO2 layer meets all the requirements for proper operation, with a cell write voltage of 1.6 V and erase voltage of 2.5 V. The access time for this structure was studied by benchmarking with experimental data. Write access time of 10.5 ns and erase access time of 16 ns have been obtained from simulations.

Keywords Nonvolatile memory (NVM) · Modeling · Memory selector · Insulator-to-metal transition (IMT) · Vanadium oxide · Resistive random access memory (ReRAM)

1 Introduction
Resistive random access memory (ReRAM) is a competitive candidate for the next generation of nonvolatile memory (NVM) devices due to its excellent scalability, fast switching speed, simple device fabrication, and two-terminal structure. This device has the potential for use in a three-dimensional (3D)-stacked memory architecture [1–5]. It has also received significant attention for neurocomputing hardware due to nonlinear characteristics which can emulate the spike signal communicated between neurons [6–8]. Conversely, the crossbar architecture provides great potential for high-density ReRAM array implementation, in which the cell size could be as small as 4F3 (F is the minimum feature size) [9]. However, the crossbar architecture has a significant drawback with pure passive ReRAM cells. Parasitic current paths through neighboring cells, which are referred to as sneak paths, may cause leakage and may alter unselected memory cells during read or write operations [10]. A selector device connected in series with the memory element is used to solve the sneak path issue. Various types of selector devices have been proposed, including diodes (one-diode–one-resistor [1D1R]), CMOS transistors (one-transistor–one-resistor, [1T1R]) [11], bipolar junction transistors (1BJT1R), or even a second ReRAM cell [12]. Among those methods, 1T1R and 1BJT1R involve complex fabrication processes [13] and require a three-terminal device which is not fully compatible with the crossbar structure. Mott devices based on transition metal oxides exhibiting conductivity switching or insulator-to-metal transition (IMT) at room temperature are a promising candidate for selector devices in crossbar architecture, with a switching time on the order of a few nanoseconds. Several studies have investigated the selector properties of vanadium dioxide (VO2) and niobium dioxide (NbO2) as Mott selector devices [14–17]. A Mott selector connected in series with a ReRAM forms a one-selector–one-ReRAM (1S1R) memory cell structure. The device modeling community has tried to develop comprehensive models to accelerate the analysis, design, and development of NVM devices. The ReRAM models have usually aimed to simplify the complex process of ion and vacancy migration and the formation of a single dominant conductive filamentary path [18–22]. Among those, the Stanford-PKU compact Verilog-A model [18]...
is a viable choice to simulate the ReRAM along with other circuit elements [18]. For Mott selector modeling, there are two main mechanisms proposed in the literature to explain the IMT: (i) structural changes induced by Joule heating (thermal) [23] and (ii) field-assisted carrier generation (electrical) [24]. We recently proposed an analytical hybrid model which takes into account the interaction of both Joule heating and field-assisted transition [25]. In this model, the contribution of electric field, temperature, and carrier concentration as main parameters affecting the transition is considered [25]. The main advantage of the proposed model is that it can estimate the device characteristics from pure thermal transition to pure electrical transition as the design parameter varies, which is crucial feature for a design-oriented model.

In this paper, we used the proposed model [25] calibrated with an experimental device [26] along with the Stanford-PKU ReRAM model [18] calibrated with experimental data [19] to design a 1S1R NVM cell for crossbar structure. Then we used the proposed model to check the design requirements and make the cell more robust against sneak path leakage.

This paper is arranged as follows: In Section 2, device structures, modeling approaches, and model calibrations for ReRAM and the Mott selector are presented, and design requirements for proper read, write, and erase operations are discussed. Section 3 illustrates simulation results and discusses the improvement of the selector by adjusting the VO2 layer length to meet the design requirements. Finally, Section 4 concludes the paper.

2 Device structure and modeling

2.1 ReRAM element

Figure 1a shows the schematic cross-section of the ReRAM element, obtained from an experimental report [18], which consists of TiN/TiOx(~5 nm)/HfOx(3.3 nm)/Pt. The HfOx is the active ReRAM layer sandwiched between TiOx and the bottom electrode.

The operation of the ReRAM is described by conductive filament (CF) formation as a result of oxygen ion movement, vacancy generation, and recombination events [6]. In the Stanford-PKU model [18], a single dominant filament is assumed, and the core variable is the gap size (g) between the filament and the bottom electrode which controls the resistance of the cell. The time derivative of g is related to the oxygen ion activation energy barrier and the applied voltage obtained from the original theory of filament formation as a result of oxygen ion movement and vacancy generation [27]:

$$\frac{dg}{dt} = -v_0 \times \exp\left(-\frac{E_a}{kT}\right) \times \sinh\left(r \times \frac{a_0}{t_{ox}} \times \frac{qV}{kT}\right)$$  \hspace{1cm} (1)

where V is applied voltage, $E_a$ is activation energy for vacancy generation, $a_0$ is the hopping site distance, $t_{ox}$ is the oxide thickness, $k$ is the Boltzmann constant, $T$ is ambient temperature, and $v_0$ is a fitting parameter. According to the proposed model [27], in the absence of an electric field, the probability per second that a particle with the escape rate of $v$ may overcome the barrier of $E_a$ is proportional to $v \exp(-E_a/kT)$. In the presence of an electric field ($F$), the height of potential barriers is changed by the amount of $+qFa_0/2$ toward the field and by $-qFa_0/2$ in the reverse direction, where $a_0$ is the distance between adjacent lattice positions (hopping distance). So the probability that ions move in the direction of the field becomes:

$v \exp(-E_a/kT) + v \exp(-(E_a + qa_0F/2)/kT)$.

Formulating the drift current proportional to a sinh function similar to Eq. (1).

Similar physics leads to Eq. (1), where the gap size between the tip of the filament and the opposite electrode is controlled by the electric field ($F = Vt_{ox}$), and a field enhancement factor ($r$) takes into account the polarizability of the material. Besides, as the current flows, the temperature is updated due to the self-heating effect, and the electric field in the gap region is increased as the gap size decreases. As a result, nonlinear and hysteresis $I$–$V$ characteristics are observed. Details of model equations are presented in [18]. We implemented this model in MATLAB and calibrated it with the experimental device [19] using parameters and constants listed in Table 1.

Figure 2a compares the $I$–$V$ characteristic for the “Set” (write) operation obtained from the model with the experiments. This result confirms that the model fits very well with the experimental report. Assuming that there is no filament in the structure initially, and the ReRAM is in
the insulator phase, the electrical potential applied to the device is increased from 0 to 2.0 V to perform the write operation. The model suggests that the filament is formed entirely around 1.6 V, and a jump in current is observed. In the backward path, the electrical conductivity remains high, which confirms the nonvolatile storage characteristics demonstrated by the model. Figure 2b shows I−V characteristics of the ReRAM during “Reset” (erase) operation obtained by the model and compared with experiments [18]. The sweep begins with the device in the “Set” state; the filament is removed entirely at −2.5 V, and the electrical resistance jumped to 1 MΩ. A noticeable decrease in electrical current is observed during the backward sweep from 2.5 V to 0. Again, the model shows perfect agreement with experimental data. The slight difference is attributed to the current limiter used in the experimental report.

3 VO₂ Mott selector

Figure 1b demonstrates the schematic cross-section of the VO₂ Mott layer sandwiched between two electrodes. Experimental implementation of this structure as a Mott selector is reported in [26]. We proposed an electrothermal hybrid model in [25], which captures two main mechanisms responsible for Mott transition, (i) Joule heating and (ii) field-assisted carrier generation, in the form of the Poole–Frankel effect. The transport of carriers at the insulating phase of the VO₂ layer is modeled based on the drift–diffusion framework, current continuity equations coupled to the heat transfer equation [28]:

\[
J = J_n + J_p = \left( qn\mu_n E + qD_n \frac{dn}{dx} \right) + \left( qn\mu_p E - qD_p \frac{dp}{dx} \right)
\]

\[
\frac{dn}{dr} = \frac{1}{q} (\nabla \cdot J_n) - r_n + g_n
\]

\[
\frac{dp}{dr} = \frac{1}{q} (\nabla \cdot J_p) - r_p + g_p
\]

\[
\nabla^2 V = -\frac{\rho}{\varepsilon}
\]

\[
\rho \frac{dT}{dt} = \nabla \cdot (K \nabla T) - \frac{J \cdot J}{\sigma(T)}
\]

where \( J \) is the current density, \( \mu \) is mobility, \( E \) is the electric field, \( D \) is the diffusion coefficient, \( r \) is the recombination rate, \( g \) is the generation rate, \( V \) is the electrical potential, \( \rho \) is the charge density, \( \varepsilon \) is the electric permittivity, \( c \) is the heat capacity, \( K \) is the thermal conductivity, \( T \) is the temperature, and \( \sigma(T) \) is the temperature-dependent electrical conductivity. Karda et. al [28] proposed using this model along with empirical temperature-dependent bandgap collapse to prepare a semiclassical electrothermal model for the IMT. However, the proposed model does not take into account the Poole–Frankel effect, which occurs only in an electric field beyond 10⁷ to 10⁹ V/cm, which is unattainable in normal planar structures but is the dominant effect in a Mott memory selector device with VO₂ layer length of sub-100 nm. Another issue is that the model requires a finite element solution of the transport equation based on a commercial device simulator. Using few assumptions, the transport equations can be simplified under normal operating conditions. Miller et al. [30] reported minority carrier lifetime in a range of 4–15 μs for VO₂ from a photocurrent decay experiment. The long minority carrier lifetime indicates that the electron–hole recombination is a slow process. Moreover, [29] and [30] demonstrated minority carrier diffusion length of a few microns. Since the length of the device under consideration (Mott selector) is very short (20–80 nm) compared to the minority carrier diffusion length (few microns), the diffusion is not the dominant transport mechanism, and we may ignore the diffusion term in Eq. (2). We also assume that the current flow is only in the x-direction: \( J(x) = \sigma(T) \times E(x) \). Therefore, ignoring the recombination, generation, and diffusion terms, a simplified electrothermal model is obtained.

\[
\frac{dT}{dt} = \nabla \cdot (K \nabla T)
\]

\[
\frac{dn}{dt} = \frac{1}{q} (\nabla \cdot J_n - r_n + g_n)
\]

\[
\frac{dp}{dt} = \frac{1}{q} (\nabla \cdot J_p - r_p + g_p)
\]
for the transient update of device temperature as a function of applied voltage.

$$c \frac{dT}{dt} = \frac{\partial}{\partial x} (K \frac{dT}{dx}) + \frac{\partial}{\partial y} (K \frac{dT}{dy}) + \frac{\partial}{\partial z} (K \frac{dT}{dz}) + \sigma(T) \left( \frac{\partial V}{\partial x} \right)^2$$  \hfill (7)  

For field-assisted transition, the model is based on the Poole–Frenkel phenomenon, which relates carrier density to the applied electric field and other device parameters as below:

![Fig. 2 I–V characteristics of the ReRAM obtained by the model compared with experimental results.](image-url)
where \( N_0 \) is the reference value of carrier concentration, \( \omega \) is the activation energy, \( \beta \) is the Poole–Frenkel constant, and \( E \) is the applied electric field. In this mechanism, transition takes place when carrier density reaches the Mott criterion.

The proposed model divides the VO\(_2\) layer into 100 segments in the \( x \)-direction and three segments in the \( y \)-direction, and we prepared a two-dimensional matrix of variables accordingly. At each simulation step, each segment is either in the metallic phase or in the insulating phase, which affects its parameters (including the mobility and resistivity), and using the finite difference method, Eqs. (2) to (6) are solved to obtain, voltage, current, and temperature at each segment. When the electric field is not close to the critical field, the barrier lowering due to the electric field effect (Poole–Frenkel effect) can be neglected, and we only check the critical temperature \( T_c \) for the transition. However, when the electric field increases, the field-assisted mechanism based on Eq. (8) turns "ON," and the transition takes place when carrier density reaches a critical value (Mott criterion): \( n_c = (0.25/\alpha_H)^3 \approx 3 \times 10^{18} \text{ cm}^{-3} \), where \( \alpha_H \) is the effective Bohr radius. At the end of each simulation step, based on the applied electric field and temperature, criteria for both thermal and electrical transition are checked with logical "OR," and after the transition, the cell parameters are updated. Details of the model derivation were published in our recent paper [25].

In our analysis, we considered a uniform VO\(_2\) layer, and each segment is in either the metallic or insulating phase. Therefore, there is not a considerable concentration gradient that leads to the diffusion before or after the transition, although the drift and diffusion are balanced in the equilibrium. Moreover, there is not any carrier concentration gradient within a segment during the transition. This is similar to the operation of a unipolar junction-less field effect transistor (JL-FET) in the accumulation mode. By ignoring the diffusion term, our model does not capture the effect of local diffusion fluctuations between two neighboring segments, if one is in the metallic phase and the other one is in the insulating phase, but this only affects the accuracy of transition time calculation. However, as we will discuss later in the transient analysis part, the extrinsic characteristics of the devices under test (including parasitic resistance and capacitance) are usually the dominant factors affecting the measured transition time results; therefore, the accuracy of the proposed model depends on comparison with \( I-V \) characteristics, and we proposed a simple complementary model to quantify the transition time.

The VO\(_2\) layer length \( (L_{\text{VO2}}) \) is a key parameter affecting the switching dynamics. Details of the model were presented in [25].

We calibrated the proposed model with the experimental device [26], and the device parameters and model calibration parameters are listed in Table 2. The reported VO\(_2\) has length of 20 nm, and the transition voltage is about 0.35 V. Under these conditions, the applied electric field is more than \( 10^5 \text{ V/cm} \), and the dominant switching phenomenon is Poole–Frenkel. Figure 3 shows the \( I-V \) characteristics of this VO\(_2\) layer obtained by the model compared with the experiment, which indicates excellent agreement.

The VO\(_2\) bulk is in the insulator state at the beginning \( (V=0) \). During forward sweep, IMT switching is observed at 0.35 V. This means that the selector device turns “ON” at this voltage. In the backward path, the switching is observed at 0.19 V. This shows that the model predicts volatile characteristics of the Mott device. The proposed selector device has high current drive capability; therefore, in the series combination of selector and ReRAM, the ReRAM limits the cell current. Figure 3 indicates that the VO\(_2\) layer has bipolar and symmetric \( I-V \) characteristics with respect to the applied voltage, which is an important selector feature for both set and reset operations.

### 4 Design requirement for crossbar operation

A 1S1R memory cell in crossbar architecture is illustrated in Fig. 4a. Each cell is addressed for read and write operations by applying a voltage between the selected bit line on the top and the word line on the bottom. For selection of

| Parameters | Description | Value |
|------------|-------------|-------|
| \( L_{\text{VO2}} \) | VO\(_2\) layer length | 20 nm |
| \( L_{\text{TE}} \) | Electrode length | 100 nm |
| \( A \) | Active area | \( 5 \times 10^6 \text{ nm}^2 \) |
| \( W \) | VO\(_2\) layer width | 250 nm |
| \( \omega \) | Activation energy | 0.5 eV |
| \( \beta \) | Poole–Frenkel constant | \( 1.2135 \times 10^{-24} \) |
| \( T_A \) | Ambient temperature | 300 K |
| \( T_{\text{IMT}} \) | IMT temperature | 326 K |
| \( T_{\text{MT}} \) | MIT temperature | 322 K |
| \( n_c \) | Mott critical concentration | \( 3 \times 10^{18} \text{ cm}^{-3} \) |
| \( K \) | Thermal conductivity | \( [4, 6] \text{ W/K m} \) |
| \( R_{\text{ON}} \) | Metallic phase resistivity | 110 \( \Omega \) |
| \( R_{\text{OFF}} \) | Insulator phase resistivity | 60K \( \Omega \) |
| \( R_S \) | Series resistor | 250 \( \Omega \) |
the proper cell, the main concern is the status of unselected neighboring cells. To avoid sneak path leakage during read, write, and erase operations, the selector of the unselected cells should be in the insulator or OFF state. Consequently, it is necessary to apply limited voltages to word lines and bit lines of unselected cells. Kim et al. [31] proposed \( V/2 \) and \( V/3 \) schemes for the correct operation of the crossbar architecture.

The \( V/2 \) scheme is demonstrated in Fig. 4b. During read or write operation, full voltage (\( V_{\text{Apply}} \)) is applied to the selected cell, and the \( V_{\text{Apply}}/2 \) is delivered to all other unselected word lines and bit lines. Maximum voltage applied to unselected cells that share either the word line or the bit line with the selected cell would be \( V_{\text{Apply}}/2 \) which is called disturb voltage. Therefore, a significant requirement for correct operation is that the disturb voltage should be lower than the threshold voltage for IMT of the selector to avoid sneak path leakage. Similarly, Fig. 4c illustrates the \( V/3 \) scheme in which \( V_{\text{Apply}} \) and 0 are applied to selected word line and bit line respectively, while \( V_{\text{Apply}}/3 \) and \( 2 \times V_{\text{Apply}}/3 \) are delivered to unselected word lines and bit lines, respectively. In this scheme, the disturb voltage in the worst case is reduced to \( V_{\text{Apply}}/3 \). The main requirement is to ensure that the unselected cell’s selector is not turned ON by the disturb voltage, even if its ReRAM is in a low-resistance state (LRS), while the selected cell’s selector is switched ON, even if its ReRAM is in a high-resistance state (HRS). In general, the \( V/3 \) scheme is more flexible and provides a better margin; however, it requires three supply voltages and is more complicated. Another critical design consideration is to limit the maximum current flow of the selected word line to avoid electromigration phenomena. Therefore, the maximum suitable current is limited to 135 μA, assuming a line area of 30×30 nm² for a Cu metal line. Table 3 summarizes...
the requirements for the correct operation of the 1S1R cell for both $V_{\text{Apply}}/2$ and $V_{\text{Apply}}/3$ schemes.

## 5 Simulation results and discussion

### 5.1 Results and analysis of 1S1R memory

The simulation results for the 1S1R cell presented in Fig. 4a based on the specifications of the VO$_2$ selector [26] and ReRAM [18] are shown for “write (set)” and “erase (reset)” operations in Figs. 5 and 6, respectively. Figure 5a shows the $I$–$V$ characteristics of the selector and the ReRAM elements separately, and Fig. 5b shows the $I$–$V$ characteristics of the complete 1S1R cell during SET operation. We assumed that the ReRAM is in HRS initially (at $V = 0$ V). Based on simulation results, the selector turns “ON” at 0.39 V instead of 0.34 V while the “Set” voltage for the ReRAM does not change from 1.63 V; this is because the voltage drop over the selector is obtained from the resistance division between the two components. The memory cell selector turns “OFF” during the backward sweep at 0.125 V, which is called the holding voltage.

Figure 6a shows the $I$–$V$ characteristics of the selector and the Mott elements separately during “Reset,” and Fig. 6b shows the $I$–$V$ characteristics of the 1S1R cell obtained from simulation. The “Reset” operation is performed when the ReRAM is in LRS. A current jump observed at $V = −0.39$ V during forward sweep is the signature of the selector turning “ON” (IMT). This jump is small because of the selector’s high drive capability. The complete erase operation is performed when the voltage reaches $−2.5$ V. Therefore, a low current level is observed during backward sweep in Fig. 6b.

The design requirements for the integrated 1S1R structure are summarized in Table 4. Design requirements are met for the read operation in both $V/2$ and $V/3$ schemes. However, the write and erase requirements are not met. For a correct write operation, the selector should be OFF in the worst case for the applied $V_{\text{write}}/2$ or $V_{\text{write}}/3$. But since $V_{\text{write}} = 1.63$ V, this condition cannot be met by the proposed selector because it turns on at 0.39 V, which leads to the formation of the sneak paths. For erase operation, the situation is even worse because $V_{\text{erase}} = −2.5$ V. Consequently, the proposed structure does not work correctly in a crossbar structure, and a modification is required.

### 6 Modified 1S1R cell characteristics

To meet the design requirements for write and erase operations, we propose a modification of the selector cell based on our electrothermal model [25] briefly described in Sect. 2.2. The key idea is to increase the threshold for undesirable turn “ON” of the neighboring cell’s selectors. To achieve this, we increase the length of the VO$_2$ layer ($L_{\text{VO2}}$). This reduces the electric field over the selector for the same applied voltage. Other parameters are kept unchanged to ensure minimum deviation from the reference structure. The length of the VO$_2$ layer is increased from 20 to 40 nm, 60 nm, and 80 nm. $I$–$V$ characteristics of the modified selectors are illustrated in Fig. 7. The IMT threshold voltage is increased from 0.34 V to 0.68 V, 1.01 V, and 1.35 V for the samples with $L_{\text{VO2}}$ (nm) = (40, 60, and 80), respectively. Furthermore, the MIT switching threshold and the width of the hysteresis loop are also increased with the VO$_2$ layer length. These results provide a degree of freedom to design the 1S1R cell according to the specified requirements.

The “Set” (write) operation and “Reset” (erase) operation of the modified 1S1R cell for the abovementioned selector lengths are illustrated in Fig. 8. For a write operation, the ReRAM element is in the HRS at the beginning, and the applied voltage is increased from 0 to 2 V. The selector turns on at $V_{\text{th-IMT}} (V) = (0.39, 0.73, 1.06, 1.37)$ for the cells with $L_{\text{VO2}}$ (nm) = (20, 40, 60, 80), respectively. After selector switching, the cells are almost the same because the conductance of VO$_2$ layers in the metallic phase is negligible compared to the ReRAM cell, therefore $V_{\text{write}} = 1.63$ V for all cells. In the backward sweep and when the ReRAM is in LRS, the MIT threshold voltages are increased monotonically, $V_{\text{hold}} (V) = (0.125, 0.30, 0.46, 0.61)$ for the samples with $L_{\text{VO2}}$ (nm) = (20, 40, 60, 80), respectively, as shown in Fig. 8a.

Figure 8b demonstrates the erase operation when the ReRAM is in LRS. The selector’s absolute turn-on threshold voltage is increased from 0.39 V for the original sample with $L_{\text{VO2}} = 20$ nm to 0.73 V, 1.06 V, and 1.37 V for the

| Scheme | Operation | Condition I | Condition II | Condition III |
|--------|-----------|-------------|--------------|--------------|
| V/2    | Read      | $V_{\text{read}} > V_{\text{IMT}}$ | $V_{\text{IMT}} > V_{\text{read}}/2$ | Maximum acceptable current $\leq 135$ µA |
|        | Write     | $V_{\text{write}} > V_{\text{SET-RERAM}}$ | $V_{\text{IMT}} > V_{\text{write}}/2$ |              |
|        | Erase     | $|V_{\text{erase}}| > |V_{\text{RESET-RERAM}}|$ | $V_{\text{IMT}} > |V_{\text{erase}}|/2$ |              |
| V/3    | Read      | $V_{\text{read}} > V_{\text{IMT}}$ | $V_{\text{IMT}} > V_{\text{read}}/3$ |              |
|        | Write     | $V_{\text{write}} > V_{\text{SET-RERAM}}$ | $V_{\text{IMT}} > V_{\text{write}}/3$ |              |
|        | Erase     | $|V_{\text{erase}}| > |V_{\text{RESET-RERAM}}|$ | $V_{\text{IMT}} > |V_{\text{erase}}|/3$ |              |
samples with $L_{VO_2}$ (nm) = (40, 60, and 80), respectively, while the erase voltage remains −2.5 V. The reason is that the voltage drop over the Mott selector in metallic phase is negligible compared to the ReRAM during erase operation.

Table 5 summarizes the design requirements for proper read, write, and erase operation in all modified 1S1R structures.

Given the $V_{\text{write}} = 1.63$ V and $V_{\text{erase}} = −2.5$ V, the selector with 40 nm oxide length does not meet the requirements.
for proper write and erase operations in the V/2 scheme, and the erase condition is not satisfied even in V/3 schemes. The 80 nm selector requires a very large read voltage ($V_{\text{read}} = 1.4 \text{ V}$), which means that the margin between read and write is very small, and it is not acceptable because of the device-to-device variability and the noise; however, write and erase requirements are met for this device. The best design option for the selector is the device with a 60 nm VO$_2$ layer. This device meets all the requirements for the V/3 scheme as specified in Table 5. The margin between read
Table 4: Design requirement analysis for read, write, and erase operations of the 1S1R cell with $V/2$ and $V/3$ schemes

| Scheme | Operation | Condition I      | Condition II   | Condition III | Operating voltage range |
|--------|-----------|------------------|----------------|---------------|-------------------------|
| $V/2$  | Read      | $V_{read} > 0.39$ V | $0.39$ V > $V_{read}/2$ | Maximum acceptable current ≤ 135 µA | 0.4–0.65 V |
|        | Write     | $V_{write} > 1.63$ V | $0.39$ V > $V_{write}/2$ | Not met       |                         |
|        | Erase     | $|V_{erase}| > 2.5$ V | $0.39$ V > $|V_{erase}|/2$ | Not met       |                         |
| $V/3$  | Read      | $V_{read} > 0.39$ V | $0.39$ V > $V_{read}/3$ | Not met       | 0.4–1 V                |
|        | Write     | $V_{write} > 1.63$ V | $0.39$ V > $V_{write}/3$ | Not met       |                         |
|        | Erase     | $|V_{erase}| > 2.5$ V | $0.39$ V > $|V_{erase}|/3$ | Not met       |                         |

Fig. 7 $I$–$V$ characteristic of an experimental 20 nm VO$_2$ selector [26] compared to the simulation results based on the electrothermal model [25] for the selector with a VO$_2$ length of 20 nm, 40 nm, 60 nm, and 80 nm

7 Transient analysis of the cell access time

The access time of memory cells is an important design parameter. Here we neglect the delay related to the interconnects and only take into account the intrinsic delay for set and reset operations of ReRAM along with the response time for IMT/MIT operations. The turn-on time for the selector determines the read access time, and the write/erase time is the sum of selector turn-on time and ReRAM write/erase time. Consequently, for the transient analysis, the characteristics of ReRAM and selector are studied separately.

Figure 9 shows the simulated transient characteristics for “Set” and “Reset” operations of the ReRAM cell [18]. The applied voltage for the “Set”/“Reset” operations is 2 V/−2.5 V respectively. The voltage is applied in the form of a pulse with the rise time of 10 ns, as illustrated in the insets of Fig. 9. The “Set” operation is high-speed ($t_{set} = 1.2$ ns; we supposed the difference between the time that the applied voltage reached 2 V and the time when the current reached its maximum value as the “Set time”). The “Reset” operation requires more time as indicated in Fig. 9b; the time scale for the reset operation is about 6.6 ns (~7 ns) (the time difference between application of $V_{applied} = −2.5$ V and when the current reaches 50% of its final value is considered the “Reset time”).
Several studies have reported the transient behavior and IMT/MIT switching for the VO$_2$ structure [32–37], showing that transition time in VO$_2$ depends on the length and cross-section of the active layer [34, 35]. In addition, in [35], the dependency of the transition time on the voltage amplitude and the input pulse width is discussed. The transient response of the selector is studied based on experimental data because, first, the proposed model only captures the
DC characteristics, and second, we would like our analysis to be based on experimental evidence. The 20 nm selector in [26] has a cross-section of 5 × 10^4 nm^2. A similar structure has been reported in [35], with a length of 100 nm and a cross-section of 3 × 10^4 nm^2, and the switching time of 800 ps has been reported for IMT and MIT. Another study suggests a transition time of 2 ns in VO_2 with length of 100 nm and 1 × 10^4 nm^2 cross-sectional area [36]. Consequently, we expect the IMT and MIT switching time for the selector to be in the range of 1 to 2 ns. A simple RC model is proposed in [33] to approximate the time constant for the transition. After the transition to the metallic phase, the electrical resistance of the selector decreases by several orders, whereas the dielectric constant of VO_2 increases [39]. For example, the relative permittivity of VO_2 increases from 36 in the insulator phase to 6 × 10^4 (real part) in the metallic phase at 100 °C [39]. This indicates that the time constants for IMT and MIT are in the same order [33].

Based on the above discussion, there are two scenarios to estimate transition time for the selector. In the optimistic scenario, the resistance of the selector in the insulating phase increases proportionally with the length of the VO_2 layer, while the dominant capacitance is considered the lateral capacitance between the selector and surrounding area, which decreases by increasing L_{VO_2}, and the RC model suggests that the time constant remains unchanged; experimental evidence for this scenario is presented in [38]. In this case, we keep the IMT switching time in a range of 1 ns for all selectors from 20 to 80 nm VO_2 lengths. In the pessimistic scenario, the dominant capacitance is the intrinsic layer capacitance between the two electrodes and increases with the VO_2 length. Therefore, the RC time constant is proportional to the square of the oxide length (t_{RC} \propto L_{VO_2}^2); experimental evidence for this scenario is reported in [39]. Taking the switching time of 1 ns for the 20 nm selector, we obtain switching time of 4, 9, and 16 ns for selectors with length of 40, 60, and 80 nm, respectively, based on the pessimistic scenario.

Table 6 represents the range of the access times expected for the read, write, and erase operations based on the above-mentioned scenarios. This result is especially interesting for the 1S1R cell with 60 nm selector length, which meets the design requirements for valid operations, and suggests that the read access time is between 1 and 9 ns, write access time is in the range of 2.5 to 10.5 ns, and the erase access time is between 8 and 16 ns, which are practical values for fast NVM.

### 8 Conclusion

We studied the design of 1S1R memory cells based on the VO_2 Mott selector and TiO_2/HfO_2 ReRAM element. The previously developed electrothermal model for a Mott selector and the Stanford-PKU model for ReRAM has been used...
to analyze and study the design requirements of the 1S1R cell. Simulation results suggest that the model follows the current–voltage characteristics of experimental devices during read, write, and erase operations. We studied the variation of the selector VO₂ length as the design parameter to achieve the design requirements, and simulation results suggest that the selector with the VO₂ layer length of 60 nm can meet all design requirements. We further studied the access time for the memory cell based on experimental results and the first-order RC model, and we obtained the worst-case access time on the order of 9, 10.5, and 16 ns for read, write, and erase operations, respectively. These results

Fig. 9 Transient characteristics of the ReRAM device reported in [18]. a The “Set” operation with the response time of 1.2 ns (inset shows the applied voltage pulse); b the “Reset” operation with the time constant of 6.6 ns (inset shows the applied voltage)
suggest that the proposed IMT model can be used for the design of selector-based NVM cells.

References

1. Akerman, J.: Toward a universal memory. Science (2005). https://doi.org/10.1126/science.1110549
2. Park, J.H., et al.: Enhancement of data retention and write current scaling for sub-20 nm STT-MRAM by utilizing dual interfaces for perpendicular magnetic anisotropy. In: Symposium on VLSI Technology (2012). https://doi.org/10.1109/VLSIT.2012.6242459.
3. Zhu, J.: Magnetoresistive random access memory: the path to competitiveness and scalability. Proc. IEEE (2008). https://doi.org/10.1109/JPROC.2008.2004313
4. Pirovano, A., et al.: Scaling analysis of phase-change memory technology. In: IEEE International Electron Devices Meeting (2003). https://doi.org/10.1109/IEDM.2003.1269376
5. Qazi, M., et al.: A low-voltage 1 Mb FRAM in 130 μm CMOS featuring time-to-digital sensing for expanded operating margin. IEEE J. Solid State Circuits (2012). https://doi.org/10.1109/JSSC.2011.2164732
6. Wong, H.P., et al.: Metal-oxide RRAM. Proc. IEEE (2012). https://doi.org/10.1109/JPROC.2012.2190369
7. Guan, X., Yu, S., Wong, H.S.P.: On the switching parameter variation of metal-oxide RRAM—part I: physical modeling and simulation methodology. IEEE Trans. Electron Devices (2012). https://doi.org/10.1109/TED.2012.2184544
8. Yu, S., Guan, X., Wong, P.: On the switching parameter variation of metal oxide RRAM—part II: model corroboration and device design strategy. IEEE Trans. Electron Devices (2012). https://doi.org/10.1109/TED.2012.2184544
9. Huang, Y., et al.: A new dynamic selector based on the bipolar RRAM for the crossbar array application. IEEE Trans. Electron Devices (2012). https://doi.org/10.1109/TED.2012.2201158
10. Linn, E., et al.: Incorporating variability of resistive RAM in circuit simulations using the Stanford–PKU model. IEEE Trans. Nanotechnol. (2020). https://doi.org/10.1109/TNANO.2020.3004666
11. Li, H., et al.: Resistive RAM-centric computing: design and modeling methodology. IEEE Trans. Circuits Syst. I Regul. Pap. (2017). https://doi.org/10.1109/TCIL.2017.2709812
12. Belyaev, M., et al.: Switching channel development dynamics in planar structures on the basis of vanadium dioxide. Phys. Solid State (2018). https://doi.org/10.1134/S1063784418030046
13. Pergament, A.L., et al.: Switching effect and the metal–insulator transition in VO2 thin films. IEEE Trans. Nanotechnol. (2019). https://doi.org/10.1109/TNANO.2019.2922838
14. Reuben, J., et al.: Incorporating variability of resistive RAM in circuit simulations using the Stanford–PKU model. IEEE Trans. Nanotechnol. (2020). https://doi.org/10.1109/TNANO.2020.3004666
15. Liu, X., et al.: Reduced threshold current in NbO2 selector by engineering device structure. IEEE Electron Device Lett. (2014). https://doi.org/10.1109/LED.2014.2344105
16. Martens, K., et al.: The VO2 interface, the metal-insulator transition tunnel junction, and the metal-insulator transition switch-on/off resistance. J. Appl. Phys. (2012). https://doi.org/10.1063/1.4767473
17. Son, M., et al.: Self-selective characteristics of nanoscale VOx devices for high-density ReRAM applications. IEEE Electron Device Lett. (2012). https://doi.org/10.1109/LED.2012.2188989
18. Jiang, Z., et al.: A compact model for metal-oxide resistive random access memory with experiment verification. IEEE Trans. Electron Devices (2016). https://doi.org/10.1109/TED.2016.2545412
19. Jiang, Z., et al.: Verilog-A compact model for oxide-based resistive random access memory (RRAM). In: International Conference on Simulation of Semiconductor Processes and Devices (2014). https://doi.org/10.1109/SISPAD.2014.6931558
20. Pergament, A.L., et al.: Switching effect and the metal–insulator transition in VO2 thin films. IEEE Trans. Nanotechnol. (2019). https://doi.org/10.1109/TNANO.2019.2922838
21. Reuben, J., et al.: Incorporating variability of resistive RAM in circuit simulations using the Stanford–PKU model. IEEE Trans. Nanotechnol. (2020). https://doi.org/10.1109/TNANO.2020.3004666
22. Belyaev, M., et al.: Switching channel development dynamics in planar structures on the basis of vanadium dioxide. Phys. Solid State (2018). https://doi.org/10.1134/S1063784418030046
23. Pergament, A.L., et al.: Switching effect and the metal–insulator transition in VO2 thin films. IEEE Trans. Nanotechnol. (2019). https://doi.org/10.1109/TNANO.2019.2922838
24. Farjadian, M., Shalchian, M.: Hybrid electrothermal model for resistive RAM-centric computing: design and modeling methodology. IEEE Trans. Electron Devices (2012). https://doi.org/10.1109/TED.2012.2184544
25. Shin, J., et al.: TiO2-based metal-insulator-metal selection device for bipolar resistive random access memory cross-point application. J. Appl. Phys. (2011). https://doi.org/10.1063/1.3544205
26. Huang, J., et al.: One selector-one resistor (1S1R) crossbar array for high-density flexible memory applications. In: International Electron Devices Meeting (2011). https://doi.org/10.1109/JIEDM.2011.6131653
27. Lee, M.J., et al.: Two series oxide resistors applicable to high speed and high density nonvolatile memory. Adv. Mater. (2007). https://doi.org/10.1002/adma.200700251
28. Karda, K., et al.: Self-consistent, semiclassical electrothermal model for mott devices. IEEE Trans. Electron Device Lett. (2011). https://doi.org/10.1109/LED.2011.2163697
29. Mott, N.F., Gurney, R.W.: Electronic Processes in Ionic Crystals. Dover, New York (1948)
30. Karda, K., et al.: A self-consistent, semiclassical electrothermal modeling framework for mott devices. IEEE Trans. Electron Devices (2018). https://doi.org/10.1109/TED.2018.2817604
31. Zhou, Y., Ramanathan, S.: GaN/VO2 heteroeptaxial p–n junctions: Band offset and minority carrier dynamics. J. Appl. Phys. (2013). https://doi.org/10.1063/1.4807922
32. Miller, C., et al.: Unusually long free carrier lifetime and metal-insulator band offset in vanadium dioxide. Phys. Rev. B (2012). https://doi.org/10.1103/PhysRevB.85.085111
33. Kim, S., et al.: Crossbar RRAM arrays: selector device requirements during write operation. IEEE Trans. Electron Device (2014). https://doi.org/10.1109/TED.2014.2327514

Table 6 Range of expected access times for read, write, and erase operations of a 1S1R memory cell based on two scenarios

| Oxide length | Read access time (ns) | Selector turn OFF (ns) | Erase access time (ns) | Write access time (ns) |
|--------------|----------------------|------------------------|------------------------|------------------------|
| 20 nm        | $t_{\text{on}} \leq 1$ | $t_{\text{off}} \leq 1$ | $t_{\text{erase}} \leq 8$ | $t_{\text{write}} \leq 2.2$ |
| 40 nm        | $1 \leq t_{\text{on}} \leq 4$ | $1 \leq t_{\text{off}} \leq 4$ | $8 \leq t_{\text{erase}} \leq 11$ | $2.2 \leq t_{\text{write}} \leq 5.5$ |
| 60 nm        | $1 \leq t_{\text{on}} \leq 9$ | $1 \leq t_{\text{off}} \leq 9$ | $8 \leq t_{\text{erase}} \leq 16$ | $2.2 \leq t_{\text{write}} \leq 10.5$ |
| 80 nm        | $1 \leq t_{\text{on}} \leq 16$ | $1 \leq t_{\text{off}} \leq 16$ | $8 \leq t_{\text{erase}} \leq 23$ | $2.2 \leq t_{\text{write}} \leq 17.5$ |
32. Pergament, A.L., et al.: Electrical switching and oscillations in vanadium dioxide. Physica B (2018). https://doi.org/10.1016/j.physb.2017.10.123
33. Nikitin, A.A., et al.: Metal–insulator switching of vanadium dioxide for controlling spin-wave dynamics in magnonic crystals. J. Appl. Phys. (2020). https://doi.org/10.1063/5.0027792
34. Kar, A., et al.: Intrinsic electronic switching time in ultrathin epitaxial vanadium dioxide thin film. Appl. Phys. Lett. (2013). https://doi.org/10.1063/1.4793557
35. Jerry, M., et al.: Dynamics of electrically driven sub-nanosecond switching in vanadium dioxide. IEEE Silicon Nanoelectron. Workshop (2016). https://doi.org/10.1109/SNW.2016.7577968
36. Zhou, Y., et al.: Voltage-triggered ultrafast phase transition in vanadium dioxide switches. IEEE Electron Device Lett. (2013). https://doi.org/10.1109/LED.2012.2229457
37. Radu, I.P., et al.: Switching mechanism in two-terminal vanadium dioxide devices. Nanotechnology (2015). https://doi.org/10.1088/0957-4484/26/16/165202
38. Pergament, A.L., et al.: Metal-insulator transition, electrical switching and oscillations. A review of state of the art and recent progress. arXiv:1601.06246 [cond-mat.mtrl-sci] (2016)
39. Yang, Z., et al.: Dielectric and carrier transport properties of vanadium dioxide thin films across the phase transition utilizing gated capacitor devices. Phys. Rev. B (2010). https://doi.org/10.1103/PhysRevB.82.205101

Publisher’s Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.