Edge plating for building large arrays and low-inductance board-to-board connection

Junho Park$^1$ and Dong Gun Kam$^{2a)$}

$^1$Department of Electrical Engineering, Pohang University of Science and Technology, 77 Cheongam-ro, Nam-gu, Pohang 16499, Republic of Korea
$^2$Department of Electrical and Computer Engineering, Ajou University, 206 Worldcup-ro, Yeongtong-gu, Suwon 16499, Republic of Korea

a) kamdong@gmail.com

Abstract: This paper proposed the use of edge plating for direct board-to-board connection. Edge plating offers a contiguous reference plane for array antenna applications and can significantly reduce the loop inductance of power distribution networks.

Keywords: edge plating, board-to-board connection, power distribution network (PDN), contiguous plane, low inductance

Classification: Microwave and millimeter-wave devices, circuits, and modules

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1 Introduction

Edge plating has become a well-developed technology, enabling low manufacturing costs for plated edges. Most manufacturers of printed circuit boards (PCBs) have a galvanic production line and a milling facility. Thus, additional investment in machines or the invention of a new process is unnecessary. Initially, the motivation for developing edge plating (Fig. 1) was the need to control electromagnetic compatibility behavior [1]. It soon became evident that the cooling function of a PCB is also improved significantly. Edge plating offers an advantage for signal integrity at the point of signal transfer from device to periphery. For high-speed links, the interface from device to cable is vulnerable. For a few millimeters on the path from the PCB edge to the cable, the shielding or the continuous reliable ground reference for signal transmission is unavailable. This can result in noticeable disturbances in signal quality. Signal quality can be secured if the PCB, the plug, and the cable form a single entity. This is achieved with plugs that are

Fig. 1. Round edge plating.

Fig. 2. Plated half holes.
mounted on the plated edge of the PCB. Plated half holes or castellated holes (Fig. 2) are now more commonly used. These holes are used for mounting a PCB to another PCB by means of solder, or for the insertion of specially designed edge connectors.

Although edge plating has been available for some time, its usage has been limited to electromagnetic shielding. In the previous report [1], edge plating provides continuous shielding to reduce radiated emission from PCB structures. In the previous report [2], edge plating shields a patch electrode in a high-sensitivity electric probe. While all the other layers of a PCB are well utilized, the third dimension of a PCB, the edge, has been neglected. Our research investigates the possibilities of using the PCB edge as another routing layer.

In this paper, we propose the use of edge plating for providing a continuous ground plane to massive antenna arrays and low-inductance board-to-board connection. In Section II, the concept and thought process regarding providing a continuous ground plane to large arrays is introduced. The edge plating for low-inductance board-to-board connection is analyzed using an equivalent circuit model in Section III. The time and frequency domain properties of the proposed packaging method is discussed and analyzed in Section IV. Section V concludes the paper.

## 2 Package tiling for building large arrays

Massive antenna arrays are required for millimeter-wave communication, radar or imaging system to achieve higher gain, beam coverage and channel capacity [3]. In many case, the required phased-array antennas need to be divided into multiple sub-arrays, each built on a different package and then assembled at the board level [4, 5]. Besides, when a faulty antenna is found in a package, this approach allows us to replace that package instead of rebuilding the entire board.

The spacing between antenna elements is typically set to be around half a wavelength to achieve a wide beam steering angle while suppressing grating lobes. For example, in a 94-GHz imaging system, antenna elements are arranged at 1.6-

![Fig. 3. Conventional approach of package tiling.](image1)

![Fig. 4. Proposed approach.](image2)
mm intervals assuming free space. To maintain this spacing, some antenna elements should be placed extremely close to the edge of a package (see the red dotted circles in Fig. 3). Recently, it is also ascertained that the properties of antenna element vary significantly depending on its location on a finite ground plane in millimeter-wave sub-array systems [6]. Since those antennas see only a part of the ground plane, their characteristics get detuned. Alternatively, the antenna ground of each package can be directly connected through the edge plating [7], as shown in Fig. 4. This provides a contiguous ground plane for the entire array.

Fig. 5 shows three methods of building a $4 \times 4$ array antenna: the whole array in a single package; (b) $4 \times 4$ array antenna split: four $2 \times 2$ sub-arrays are connected through another PCB at the bottom; (c) $4 \times 4$ array antenna edge plating: four $2 \times 2$ sub-arrays are directly connected by edge plating (proposed method).

![Fig. 5.](image)

Fig. 6. Radiation patterns of the three methods.

3 Low-inductance connection of power distribution networks

A transient current injected in power distribution network (PDN) can cause a significant amount of simultaneous switching noise (SSN) which is a major source of jitter, skew and radiated emission problems [8]. The amount of the SSN is linearly proportional to the total loop inductance of the entire PDN. Therefore, it is most important to minimize the loop inductance of the PDN to satisfy the noise margin.

Edge plating can be used for low-inductance board-to-board connection (cf. conventional castellations are used for board-on-board connection). The hierarchical PDN consists of a package and PCB level PDNs (see Fig. 7). The PDNs of
packages are usually connected at the board level using vertical interconnect structures such as plated through hole vias and solder balls. On the other hand, edge plating can directly connect the PDNs of the packages (see Fig. 8). Plated edges can be directly soldered to each other during the board assembly. This edge plating can add a new current path between two packages.

Fig. 9 and Fig. 10 compare signal current paths in the two approaches. To facilitate understanding, solder balls and vias are omitted in the models. When no decoupling capacitor is used, the total loop inductance of the conventional PDN is the sum of Package 1, PCB and Package 2 inductances in series (Fig. 9). On the other hand, in the proposed PDN, total loop inductance is the sum of the original
loop inductance (red solid line) and the new loop inductance (blue dotted line) of edge plating, in parallel (Fig. 10). When there are decoupling capacitors, the total loop inductance can be calculated in a similar way, as summarized in Table I. In either case, it is clear that the total inductance is significantly reduced by the edge plating.

### Table I. Comparison of total loop inductance

| Case                              | Conventional PDN                                                                 | Proposed PDN                                                                 |
|-----------------------------------|---------------------------------------------------------------------------------|------------------------------------------------------------------------------|
| w/o decoupling capacitors         | $L_C = L_{PKG1} + L_{PCB} + L_{PKG2}$                                         | $L_P = (L_{PKG1} + L_{EDGE} + L_{PKG2}) \parallel (L_{PKG1} + L_{PCB} + L_{PKG2})$ |
| w/ decoupling capacitors          | $L_C = L_{PKG1} + L_{DE-PCB} \parallel (L_{PCB} + (L_{PKG2} \parallel L_{DE-PCB}))$ | $L_P = (L_{PKG1} + L_{EDGE} + L_{PKG2}) \parallel (L_{PKG1} + L_{DE-PCB} \parallel (L_{PCB} + (L_{PKG2} \parallel L_{DE-PCB})))$ |

$L_{PCB}$ = loop inductance of PCB, $L_{PKG}$ = loop inductance of package
$L_{EDGE}$ = loop inductance of edge plating (solder)
$L_{DE-PCB}$ = equivalent series inductance of on-PCB decoupling capacitor

Fig. 11. Test vehicle of the conventional PDN

Fig. 12. Test vehicle of the proposed PDN
We designed test vehicles to verify the proposed idea. In the conventional approach shown in Fig. 11, two 30 mm x 30 mm packages are connected to a 75 mm x 35 mm board through a pair of power and ground balls (diameter = 0.6 mm). In the proposed approach shown in Fig. 12, the two 30 mm x 30 mm packages are directly connected through edge plating and six solder bridges; three solder balls for the power planes and the other three for the ground planes. Plated half hole

4 Time and frequency domain verification

We designed test vehicles to verify the proposed idea. In the conventional approach shown in Fig. 11, two 30 mm x 30 mm packages are connected to a 75 mm x 35 mm board through a pair of power and ground balls (diameter = 0.6 mm). In the proposed approach shown in Fig. 12, the two 30 mm x 30 mm packages are directly connected through edge plating and six solder bridges; three solder balls for the power planes and the other three for the ground planes. Plated half hole
arrays consisting of an oblong via are used to form the edge plating and illustrated in Fig. 13. The oblong vias feature length ($W_E$) of 3 mm and height ($H_E$) of 1 mm, and the spacing between adjacent vias ($S_v$) is 5.4 mm. These vias are aligned on the outer edge of the package and the cutting is performed to expose the plated contour over the complete thickness of the packages.

The self-impedance ($Z_{11}$) at one probing pad (Port 1) was measured while the other pad (Port 2) remained open. Measurement result shows good correlation with 3-D fullwave simulation (HFSS) result [9], and the latter is adopted in this paper in
order to include the effect of decoupling capacitors and to compare SSN. Fig. 14 shows that the total capacitances of the two structures do not differ significantly.

The self-impedance was simulated again with the other pad being short terminated. Fig. 15 shows that the total inductance of the proposed approach (blue dotted line) is much lower than that of the conventional approach (red solid line). All the resonances of odd-numbered modes are considerably suppressed by positioning the probing pad at the center of the power/ground plane. Parallel resonance points a, b, and c correspond to even-numbered cavity modes; (2,0), (2,2), and (4,0), respectively.

Even when several decoupling capacitors (0402 size, 22 nF each with equivalent series inductance of 348 pH) are included in the test vehicles, the proposed structure shows a clear advantage, as shown in Fig. 16.

The test vehicles were then modelled using the balanced transmission line model (TLM) method [10] to evaluate power supply fluctuation in the two structures. The equivalent circuit model for the conventional PDN consists of one PCB-level PDN, two package-level PDNs, as shown in Fig. 17. An inter-level PDN is added in parallel between the PCB- and the package-level PDN to reflect

Fig. 19. Comparison of the conventional PDN impedance between the TLM modeling and 3-D EM solver

Fig. 20. Comparison of the proposed PDN impedance between the TLM modeling and 3-D EM solver
the coupling effect [11]. The vias and solder balls are modeled using a π-type equivalent circuit model. The ports for excitation are placed in the center of the package-level PDNs, and the equivalent circuit model for the proposed PDN includes the modeled edge plating, as shown in Fig. 18.

Fig. 19 and Fig. 20 compare the equivalent circuit model (TLM) and 3-D full-wave simulation results. Self-impedances (Z11) were extracted at the probing pad (Port 1) while the other pad (Port 2) remained open. After confirming good correlation, we proceeded to transient simulations using the TLM models.

Fig. 21. Voltage Fluctuation Simulation Setup: The VRM is connected at the PCB level PDN and the IC is mounted at the probing port 1.

Fig. 22. Simulated power supply voltage fluctuation for the test vehicle of the conventional structure.

Fig. 23. Simulated power supply voltage fluctuation for the test vehicle of the proposed structure.
Fig. 21 shows the simulation setup, where the voltage regulator module (VRM) of 1.5 V with 70 nH is mounted on the PCB and the “IC” (100-mA current source) at Port 1. Fig. 22 and Fig. 23 show the SSN of the two test vehicles. The amplitude of the simulated voltage fluctuation of the proposed structure is only 180 mV, while that of the conventional structure is 680 mV.

5 Conclusion
We introduced edge plating for both building a large array and board-to-board connection. The proposed idea offers a contiguous reference plane for a large array. It also reduces the loop inductance of PDNs, which in turn reduces SSN. The proposed packaging tiling method is expected to be used for millimeter-wave 5G massive MIMO systems, phased radar arrays and sub-terahertz imaging systems due to its clear advantages and low fabrication costs.

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