Frequency-Response Analysis and Design Rules for Capacitive Feedback Transimpedance Amplifier

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Abstract—Precision instrumentation systems, such as optical receivers and other current-output measurement systems, often contain a transimpedance amplifier (TIA). The commonly used resistive feedback TIA (RF-TIA) has a drawback in its practical implementation; the system bandwidth is limited by the feedback resistor and its parasitic capacitance in high-speed applications. To overcome this drawback, a capacitive feedback TIA (CF-TIA) can be used. The gain and bandwidth performance of the CF-TIA are theoretically equivalent to those of the RF-TIA. Although CF-TIA has been introduced in previous studies for reducing thermal noise and addressing the difficulty in integrating a high resistance with the CMOS technology, past analyses have not been in sufficient depth. The ultimate goal of this study is providing designers in this field with helpful design rules and analytical tools. In particular, a transfer function model, the critical design parameters, and a stability analysis are presented. Furthermore, a new CF-TIA configuration involving a simplified integrator dc-feedback loop is introduced, which can be deployed as a single stage rather than the conventional two-stage topology. While the applications considered in this study were high-speed sensor measurements and devices with a high input capacitance, such as a laser position detector, the analytical results obtained herein are also applicable to a variety of other applications such as emerging biosensors and optical communication systems.

Index Terms—Capacitive feedback, dc-feedback loop, stability, transfer function, transimpedance amplifiers (TIAs).

I. INTRODUCTION

TRANSMIPEANCE amplifiers (TIAs) are used to convert the low-current signals into a proportional output voltage that is more suitable for further analog-signal processing and for removing the noise at the input stage. They are widely used in not only optical communications [1], electrical sensors [2]–[5], and photodetectors [6]–[8] but also emerging biosensors [9], [10]. An operational amplifier (op-amp) with negative feedback is commonly used in the TIAs. The most typical TIA topology is the topology of a resistive feedback TIA (RF-TIA). It is simple and easy to analyze, because the feedback resistor value directly matches the transimpedance gain.

Unfortunately, in the high-speed measurement applications, as the value of the feedback resistor is increased to satisfy the requirement of high sensitivity, the system bandwidth, set by the feedback resistor and its parasitic capacitance, is reduced [11], [12]. The parasitic capacitance is typically about hundreds of femtofarads and varies from case to case depending on the circuit layout, and it is almost impossible to predict its value [13]. Depending on the desired bandwidth and gain, the parasitic capacitance could cause a significant difference between the expected and the actual behavior of the TIA. Thus, in general, the value of the feedback resistor is conservatively limited against the worst case scenario in which the feedback resistor has a maximum parasitic capacitance. Even in this worst case scenario, the actual system bandwidth limited by the self-resonant frequency of the feedback resistor must be greater than or equal to the desired bandwidth.

A capacitive feedback TIA (CF-TIA) can be employed to overcome the problems associated with the parasitic capacitance of the feedback resistor. The basic topology consists of an integrator with a low-value feedback capacitor and a cascaded differentiator circuit. The transimpedance gain is controlled by the ratio between the integrator’s feedback capacitor and the differentiator’s input capacitor and the relatively quite small feedback resistor of the differentiator compared with the RF-TIA’s feedback resistor. Thus, it can eliminate the aforementioned problem arising from the parasitic capacitance of the large resistance.

Although parasitic inductance is also present in the real-world capacitors, its effect on the TIA system is generally negligible, because the self-resonant frequency of the capacitor is very high. If it is assumed that general multilayer ceramic capacitors are used, the parasitic inductance is typically less than 1 nH [14]. Unlike the RF-TIA’s feedback resistor, the CF-TIA system does not require a high value of the capacitor such that the self-resonant frequency created by the capacitor’s parasitic inductance of 1 nH is close to the system frequency.

The CF-TIA was initially proposed for reducing the thermal noise generated by the RF-TIA’s feedback resistor and for overcoming the difficulty in integrating a high resistance in the CMOS chips [3]–[5], [9], [10], [15]–[17]. Applications of the CF-TIA that have been considered the most in the literature are biosensors with a narrow bandwidth and circuits with a small input capacitance in which thermal noise is dominant. However, the CF-TIA can be used for eliminating the parasitic capacitance problem even in the applications requiring high bandwidth and a high input capacitance, without compromising the system performance.

A disadvantage of the CF-TIA is that the integrator is easily saturated by the dc input signal. Two types of approaches can be used to address this issue. One is the discrete-time (DT)
To the best of our knowledge, this work is the first attempt ever to develop the general frequency-response model of the CF-TIA with a dc-feedback loop as well as to compare the theoretical performance of the CF-TIA and the RF-TIA. This work provides useful analysis tools and design guidance for the CF-TIA with a dc-feedback loop for a variety of applications. The research and evaluation presented in this article are not limited to specific applications. Accordingly, they are expected to help designers choose the best performance architecture for their purpose.

II. Basic Performance and Design of CF-TIA

This section presents the general characteristics of a CF-TIA model and explains the essential design criteria. A typical CF-TIA is shown in Fig. 1. The integrator serves as the first stage, and it is followed by the second stage (differentiator) for achieving an overall flat gain within the desired signal bandwidth.

The discussion in this section is based on the assumption of a very high \( R_f \), this being the simplest way to provide a dc path for preventing the saturation of the integrator’s capacitance and for simultaneously biasing the amplifier. However, the output of the op-amp can be easily saturated, even with an infinitesimal dc input. In addition, in some applications, the dc input can be quite large. For an optical sensor, for example, the dc input generated by ambient light is significant. Thus, dc rejection is essential to prevent the saturation of the CF-TIA. An alternative method involving an integrator dc-feedback loop that can offset the substantial dc input is presented in the subsequent sections.

The feedback capacitance of the first-stage integrator, \( C_f \), could be a parasitic capacitance or the capacitance of a capacitor introduced intentionally. The influence of the pole generated by \( C_f \) and \( R_f \) could be compensated by placing a resistor in parallel with \( C_d \) to generate a zero at \( 1/(R_f C_f) \), as mentioned in [4]. However, it is assumed that the pole created by \( C_f \) and \( R_f \) is negligibly small compared with the system bandwidth.

The achievable bandwidth of the CF-TIA, \( f_{\text{max}} \), is limited by the gain-bandwidth product of the op-amp, \( f_{\text{GBWP}} \), and the ratio between \( C_f \) and \( C_{\text{in}} \), as follows [5], [9]:

\[
f_{\text{max}} \leq f_{\text{GBWP}} \cdot \frac{C_f}{C_{\text{in}} + C_f}
\]

where \( C_{\text{in}} = C_s + C_{i,\text{op}} \) is the total capacitance, with \( C_s \) and \( C_{i,\text{op}} \) denoting the sensor capacitance and the input capacitance of the op-amp (comprising the differential and common-mode capacitances) at the amplifier’s input, respectively. It is to be noted that (1) provides the default limit for the TIA, irrespective of whether the feedback is capacitive or resistive.

To obtain the maximum attainable CF-TIA gain \( G_{\text{max}} \), we first note that the overall gain of a generic CF-TIA is

\[
\frac{v_o}{i_{\text{in}}} = \frac{C_d R_d}{C_f}
\]

where \( C_d \) and \( R_d \) are the components of the second-stage differentiator, \( i_{\text{in}} \) is the input current, and \( v_o \) is the output voltage of the CF-TIA. The gain of the differentiator increases.
with the frequency until it is rolled off by the open-loop gain of the op-amp. It is to be noted that $C_c$ is introduced to stabilize the differentiator and is given by $C_c = 1/(2\pi R_d f_H)$. Since the intersection point of the differentiator gain and the op-amp’s open-loop gain curves should be higher than the required bandwidth or the upper cutoff frequency $f_H$, the following condition can be obtained:

$$R_d C_d \leq \frac{f_{GBWP}}{2\pi f_H^2}. \quad (3)$$

When $f_H$ for the target application is provided, $G_{\text{max}}$ can be expressed as follows by using (2) and (3):

$$G_{\text{max}} = \frac{f_{GBWP}}{2\pi C_f f_H^2}. \quad (4)$$

which is similar in form to the expression for the transimpedance limit in [18].

$G_{\text{max}}$ is equivalent to the maximum attainable gain of the two-stage RF-TIA, in which the maximum gain of the first-stage TIA, $1/(2\pi f_H C_f)$, is amplified by the second-stage voltage amplifier with a maximum gain of $f_{GBWP}/f_H$. We can conclude that the CF-TIA does not degrade the fundamental system performance limits in terms of the maximum achievable bandwidth and gain.

The next step is to set the values of the circuit components. First, $C_f$ should be chosen to have the minimum value to maximize the gain, and the impact of $C_d$ should then be evaluated. The value of $C_d$ is limited by its loading effect. The low but nonzero op-amp output resistance $r_o$ and $C_d$ create an additional pole in the open-loop transfer function of the op-amp, which limits the bandwidth of the CF-TIA. To avoid the loading effect of $C_d$, we should select the value of $C_d$ by using the criterion

$$C_d \leq \frac{1}{2\pi f_H r_o}. \quad (5)$$

In general, $r_o$ is not constant in most op-amps. The output resistance or the capacitive loading effect on the op-amp for different frequencies is usually provided in the op-amp’s datasheet. Given the value of $C_d$, the value of $R_d$ is set using (3).

A noise performance analysis is now presented. An input-referred noise model is commonly used in noise analysis for comparing the input signals with noise levels at the input. The power spectral density (PSD) of the input-referred noise current is given by

$$S_N = i_n^2 + \frac{4kT}{R_f} + \left(\frac{e_n C_{\text{in}}}{2\pi f_c}\right)^2. \quad (6)$$

where $i_n$ is the inverting-input current noise of the op-amp, $e_n$ is the differential voltage noise of the op-amp, $k$ is Boltzmann’s constant, and $T$ is the absolute temperature.

All noise sources are expressed in amperes or volts per root hertz. It is important to understand the effect of each term in (6). The current noise $i_n$ and the thermal noise current of $R_f$ are directly seen at the input node. The thermal noise voltage $(=4kTR_f)^{1/2}$ is divided by $R_f$ to be the thermal noise current form as the second term of (6). The third term of (6) is expressed by dividing the output noise of the integrator for $e_n$ by the integrator gain; $e_n$ is amplified by the noise gain $C_{\text{in}}/C_f$ at the integrator output, and the input-referred expression for $e_n$ contribution is then obtained by dividing $e_n C_{\text{in}}/C_f$ with the integrator gain $1/(2\pi f_c C_f)$.

By integrating the PSD in (6) up to $f_H$, dividing by $f_H$, and then taking the square root, we obtain the root-mean-square (rms) value of the input-referred noise

$$i_{N,\text{rms}} = \sqrt{i_n^2 + \frac{4kT}{R_f} + \left(\frac{e_n 2\pi f_c C_{\text{in}}}{3}\right)^2}. \quad (7)$$

This expression is identical to that for the rms input-referred noise of the RF-TIA. It is to be noted that increasing $R_f$ does not limit the bandwidth, nor is $R_f$ related to the gain of the CF-TIA, unlike the RF-TIA. When $R_f$ is increased sufficiently to render the thermal noise term negligible, significant improvements can be made in the noise performance compared with the RF-TIA.

However, the significant improvement occurs when thermal noise is dominant only, namely, when $f_{\text{in}}$ is limited to tens of kilohertz and $C_{\text{in}}$ is negligibly small. In the high-speed optical sensor applications requiring a large bandwidth and a large sensor capacitance, typically, the $e_n$ term is dominant; hence, the significant improvements become ineffective. It is to be noted that $i_n$ can be neglected by using an op-amp with a field-effect-transistor input stage, which is often preferred to TIAs.

Even if the improvement is marginal, the input-referred noise of the CF-TIA is still upper bounded by that of the RF-TIA for a sufficiently large $R_f$. Therefore, deploying the CF-TIA does not add any noise but only reduces the thermal noise to a lower level in comparison with the RF-TIA. It was observed that while the noise, gain, and bandwidth performance of the CF-TIA were equivalent to those of the RF-TIA, the effects of the variation of the parasitic capacitance seen in the RF-TIA were eliminated.

III. CF-TIA WITH INTEGRATOR DC-FEEDBACK LOOP

A. Frequency-Response Analysis

In [5], [9], [10], and [15]–[17], CF-TIAs were used with an integrator dc-feedback loop instead of a very high single $R_f$, as shown in Fig. 2. The dc-feedback loop comprises an inverting integrator, namely, a feedback-integrator, followed
Rewriting (9) in the standard form of the transfer function of a second-order bandpass filter with a center frequency $\omega_0$ and $\alpha (=1/Q)$ yields

$$H_i(s) = -R_{dc}A_{ol}\frac{\alpha\omega_0s}{s^2 + \alpha\omega_0s + \omega_0^2}$$ (10)

where $\omega_0 = 2\pi f_0$

$$f_0 = \frac{1}{2\pi \sqrt{C_1R_1C_fR_{dc}}}, \quad \alpha = \frac{\sqrt{C_1R_1}}{\sqrt{C_fR_{dc}}A_{ol}}$$ (11)

and $A(s)$ is approximated by $A_{ol}$, the low-frequency open-loop gain of the op-amp. This approximation is valid for most of the cases when the poles of $A(s)$ occur at frequencies higher than $f_0$. The parameter $f_0$ should be as low as possible to minimize the frequencies at which the dc-canceling feedback loop is active. If a wide passband is assumed along with $\alpha \gg 1$, the upper and lower cutoff frequencies, $f_{i,H}$ and $f_{i,L}$, can be expressed as

$$f_{i,H} = \frac{1}{2\pi C_fR_{dc}A_{ol}}$$ and $$f_{i,L} = \frac{A_{ol}}{2\pi C_1R_1}$$ (12)

where the subscript $i$ implies that $f_{i,H}$ and $f_{i,L}$ are the first-stage integrator's cutoff frequencies.

With the second-stage differentiator, cascaded to the first-stage integrator, the overall transfer function of the CF-TIA, $H(s)$, is derived by multiplying $H_i(s)$ by the transfer function of the differentiator

$$H_d(s) = \frac{v_{in}}{v_{i,o}} = \frac{sC_dR_d}{1 + sC_dR_d}$$ (13)

where $C_d = 1/(2\pi R_df_{i,H})$. The resulting $H(s)$ is a bandpass filter transfer function, with the lower cutoff frequency of $H(s)$, $f_L$, being equal to $f_{i,H}$ when $H_i(s)$ has a wide passband. For a narrow passband of $H_i(s)$, we have

$$f_L = f_0 \approx \frac{1}{2\pi C_fR_{dc}A_{ol}\sqrt{2}}$$ (14)

where $\alpha = \sqrt{2}$ from (11) for obtaining a maximally flat response (Butterworth response) of $H(s)$. Note that the upper cutoff frequency of $H(s)$ is $f_{i,H}$ regardless of $H_i(s)$.

From (14), it is apparent that the higher the value of $R_{dc}$, the lower the value of $f_L$. With a high $R_{dc}$, the passband of $H(s)$ extends to low frequencies, thereby preventing unnecessary signal attenuation in low frequencies. If a signal with high power in low frequencies, such as the Gaussian beam commonly used for laser detection, is used as the input signal, owing to the attenuation of signals in low frequencies of the TIA, either the peak power of the input signal is reduced or the shape of the input signal is distorted, resulting in the detection performance being degraded. Therefore, a high $R_{dc}$ is beneficial to preventing unnecessary signal attenuation and suppressing thermal noise. However, a very high $R_{dc}$ limits the capability to remove the unwanted dc components. The relation between the allowable dc component $I_{dc}$ and $R_{dc}$ is

$$R_{dc} \leq \frac{V_{max,o}}{I_{dc}}$$ (15)

where $V_{max,o}$ is the maximum allowable output voltage of the op-amp. For the determination of the value of $R_{dc}$, the level of
thermal noise, the passband width of the CF-TIA with the integrator dc-feedback loop for three cases: when the system is stable with a fairly large $R_1 (= 632 \, \text{kΩ})$, when the gain peaks at a reduced $R_1 (= 632 \, \text{kΩ})$, and when the gain peaking is avoided by setting $C_2 = 560 \, \text{pF}$. The parameter values for all the cases are as follows: $A_{\text{ol}} = 75 \, \text{dB}$, $R_{\text{dc}} = 5 \, \text{MΩ}$, $C_f = 0.2 \, \text{pF}$, $C_d = 1 \, \text{nF}$, $C_1 = 100 \, \text{nF}$, and $C_e = 16 \, \text{pF}$.

**B. Adding Additional Capacitor $C_2$**

When the values of $C_f$, $R_{\text{dc}}$, and $A_{\text{ol}}$ are known, the stability of the system can be ensured by adjusting the product of $C_1$ and $R_1$ such that $\alpha \geq \sqrt{2}$ in (11). With this adjustment, the frequency response is free of gain peaking. The adjustment can be expressed as

$$C_1 R_1 \geq 2 C_f R_{\text{dc}} A_{\text{ol}}^2. \quad (16)$$

From (16), it is apparent that the product $C_1 R_1$ for ensuring stability is significantly large, because $A_{\text{ol}}^2$ is generally exceedingly large.

On the other hand, $C_1 R_1$ is the time constant $\tau$ for the steady state of the system, and having a large $\tau$ is undesirable. When $\tau$ is too large, it takes an extremely long time to remove the dc input. The magnitudes of the transfer functions $H_1(s)$, $H_f(s)$, and $H(s)$ are plotted in Fig. 3. In the figure, the relationship between $\tau$ and the stability of the system is brought out by the switching of $R_1$ from 632 kΩ to 623 kΩ. Other parts are the same for both cases, with $R_{\text{dc}} = 5 \, \text{MΩ}$, $C_f = 0.2 \, \text{pF}$, and $C_1 = 100 \, \text{nF}$. When $\tau$ is exceedingly large, namely, 63.2 s, with $R_1 = 632 \, \text{MΩ}$, the system is stable, and the value of $\alpha$ is $\sqrt{2}$. However, when $\tau$ is reduced significantly to 63.2 ms with $R_1 = 632 \, \text{kΩ}$, gain peaking occurs, and the value of $\alpha$ is 0.0446.

Introducing an additional capacitance $C_2$ in parallel with $R_1$ can prevent gain peaking, even when $\tau$ is significantly reduced. This allows the dc-feedback loop to have a zero, resulting in a sufficiently large phase margin without a large value of $\tau$. When $C_2$ is introduced, following the approaches mentioned in Section III-A yields the following equation:

$$i_{\text{in}} = s C_f (v_{\text{in}} - v_{i,o}) + s C_m v_{\text{in}} + \left( v_{\text{in}} - \frac{1 + s C_2 R_1}{s C_1 R_1} v_{i,o} \right) \frac{1}{R_{\text{dc}}}. \quad (17)$$

$H_1(s)$ is then obtained as

$$H_1(s) = \frac{v_{i,o}}{i_{\text{in}}} \approx \frac{1}{s C_f} \left( \frac{1}{s C_1 R_1} \right) \left( \frac{1}{s C_f R_{\text{dc}} A_{\text{ol}}} \right) \left( \frac{C_2}{C_1 C_f R_{\text{dc}}} \right) \left( 1 + \frac{R_1}{C_1 C_f R_{\text{dc}}} \right) \left( \frac{1}{C_1 C_f R_{\text{dc}}} \right) \left( \frac{R_1}{C_1 C_f R_{\text{dc}}} \right) \left( \frac{C_2}{A_{\text{ol}}} \right) \left( \frac{1}{A_{\text{ol}}} \right). \quad (18)$$

When (18) is rewritten in the standard form of the transfer function, similar to (10), $\alpha$ is given by

$$\alpha = \sqrt{\frac{C_1 R_1}{C_f R_{\text{dc}} A_{\text{ol}}}} \left( \frac{1}{\sqrt{C_1 C_f R_{\text{dc}}}} \right) \left( \frac{C_2}{A_{\text{ol}}} \right). \quad (19)$$

where approximation (a) is obtained by assuming $\alpha \approx 0$ in (11). This approximation is valid if $\tau$ is significantly reduced and gain peaking occurs in the absence of $C_2$. The parameter $f_0$ continues to be given by (11). The value of $C_2$ can then be set using the formula

$$C_2 = \sqrt{\frac{C_1 C_f R_{\text{dc}}}{R_1}} \alpha. \quad (20)$$

where $\alpha \geq \sqrt{2}$.

Fig. 3 shows that introducing $C_2 (= 560 \, \text{pF})$ in parallel with $R_1 (= 632 \, \text{kΩ})$ for $\alpha = \sqrt{2}$ renders the system stable. In the absence of $C_2$, gain peaking occurs at 638 Hz. It is to be noted that a small value of $C_2$ is preferred because of its loading effect on the output of the integrator’s op-amp, as discussed earlier. For the same reason, given a value of $C_1$, $R_1$, a high value of $R_1$, and a low value of $C_1$ are preferred.

Introducing $C_2$ is also useful when $A_{\text{ol}}$ is highly unstable, since it can eliminate the dependence of $A_{\text{ol}}$ on $\alpha$. The parameter $A_{\text{ol}}$ can vary widely from one device to another, even among devices of the same type, depending on the temperature, component aging, manufacturing process variations, and so on.

**IV. CF-TIA With Simplified Integrator DC-Feedback Loop**

In this section, a new configuration of the CF-TIA involving a simplified integrator dc-feedback loop is introduced. The dc-feedback path of a CF-TIA can be simplified by using a single noninverting integrator, as shown in Fig. 4. With this simplification, the inverting buffer is not required and the first-stage integrator can be solely used as an excellent CF-TIA with a sufficiently broad passband.

The method discussed in Section III-A can be used to obtain the following equation:

$$i_{\text{in}} = s C_f (v_{\text{in}} - v_{i,o}) + s C_m v_{\text{in}} + \left( v_{\text{in}} - \frac{1 + s C_1 R_1}{s C_1 R_1} v_{i,o} \right) \frac{1}{R_{\text{dc}}}. \quad (21)$$
It is noteworthy that (21) is identical to (17) for $C_2 = C_1$. This implies that using a simplified integrator dc-feedback loop not only simplifies the circuit but also has an effect identical to that of adding $C_2$ (discussed in Section III-B), resulting in a sufficiently large phase margin without a significantly large value of $\tau$.

$H_i(s)$ for the new configuration of the CF-TIA is obtained as

$$H_i(s) = \frac{v_{i,o}}{i_{in}} \approx \frac{-1}{C_f s^2 + \frac{1}{C_f R_{dc}} s + \frac{1}{C_1 R_1 C_f R_{dc}}}.$$  \hspace{1cm} (22)

From (22), the design parameters for the first-stage integrator of the proposed CF-TIA topology are

$$a = \sqrt{\frac{C_1 R_1}{C_f R_{dc}}}, \quad f_{i,H} = \frac{1}{2\pi C_f R_{dc}}, \quad \text{and} \quad f_{i,L} = \frac{1}{2\pi C_1 R_1}.$$  \hspace{1cm} (23)

The expression for $f_0$ is the same as that in (11). Compared with (12), the dependence of the upper and lower cutoff frequencies on $A_{ol}$ has been eliminated in (23), which is obtained by multiplying and dividing $f_{i,H}$ and $f_{i,L}$ in (12) by $A_{ol}$, respectively. The elimination of the dependence on $A_{ol}$ is one of the merits of the simplified dc-feedback loop.

Furthermore, the overall flat gain region of $H_i(s)$ is considerably expanded by shifting each of the lower and higher cutoff frequencies from (12) to (23) by an amount equal to $A_{ol}$. Therefore, the first-stage integrator can act as a wideband TIA with the flat gain $R_{dc}$, the upper cutoff frequency $f_{i,H}$, and the lower cutoff frequency $f_{i,L}$. The upper cutoff frequency is limited only by the intersection of the noise gain and the op-amp's open-loop gain curves, and this can be expressed as $f_{i,H} < f_{\text{GBWP}} C_f / C_{in}$. When $f_{i,H}$ satisfies the desired system bandwidth, the second stage would become the postamplifier multiplying gain only, and it is not part of the CF-TIA.

$R_{dc}$ must be reduced to increase $f_{i,H}$ to achieve a wide passband in $H_i(s)$. However, with a decrease in $R_{dc}$, the overall noise increases when the resistive noise is dominant. Then, instead of having a high $f_{i,H}$ with a low $R_{dc}$, the bandwidth can be expanded by using a second-stage differentiator. An additional resistor $R_2$ is introduced in parallel to $C_0$ to extend the bandwidth of $H_i(s)$. The insertion of $R_2$, such that $C_f R_{dc} = C_d R_2$, leads to a zero being introduced in $H_d(s)$ at $f_{i,H}$, and $H_d(s)$ is then given as

$$H_d(s) = \frac{R_d}{R_2} \left(1 + \frac{s C_d R_2}{1 + s C_c R_d}\right).$$  \hspace{1cm} (24)

The flat gain of $H_i(s) (= R_{dc})$ is multiplied by $R_d/R_2$, and the decrease in $H_i(s)$ beyond $f_{i,H}$ is compensated by the increase in $H_d(s)$ beyond the zero that was introduced. The resulting $H(s)$ of the bandwidth-extended system becomes the bandpass filter transfer function with a flat gain of $C_d R_d / C_f$, a lower cutoff frequency $f_L$ equal to $f_{i,L}$, and an upper cutoff frequency $f_H$ of $1/(2\pi C_d R_2)$. In Fig. 5, $|H_i(s)|$, $|H_d(s)|$, and $|H(s)|$ are depicted for two cases: $R_1 = 632$ and 80 kΩ.

Moreover, compared with the conventional configuration, the attenuation of signals at low frequencies is reduced in this proposed configuration. For the given values of discrete components, $f_L (= f_{i,L}$ in (23)) of this configuration is lower than $f_L (= f_0$ in (11)) of the conventional configuration. This can be proved as follows. From (23), under the assumption of a wide passband for $H_i(s)$, we have

$$\frac{1}{2\pi C_1 R_1} (= f_{i,L}) \ll \frac{1}{2\pi C_f R_{dc}} (= f_{i,H}).$$  \hspace{1cm} (25)

By dividing (25) by $2\pi C_1 R_1$ and taking the square root, we obtain

$$\frac{1}{2\pi C_1 R_1} (= f_{i,L} \text{ in (23)}) \ll \frac{1}{2\pi \sqrt{C_f R_{dc} C_1 R_1}} (= f_0 \text{ in (11)}).$$  \hspace{1cm} (26)
the circuit was verified by performing experimental measurements on a hardware implementation. A photograph of the realized circuit is presented in Fig. 6. Since the target application required high-capacitance components, for which the single-chip design was infeasible, the circuit was implemented with discrete components. However, the presented frequency-response model and stability analysis have been generalized to be applicable to all CF-TIA applications, including the CMOS chip design.

All the circuits were built with the same op-amp, OPA657 (Texas Instruments). OPA657 has wideband and low-noise characteristics, and its GBWP, \( A_{\text{ol}} \) at room temperature, and \( e_{n} \) are 1.6 GHz, 75 dB, and 4 nV/\( \sqrt{Hz} \), respectively. It is to be noted that GBWP is not a trimmed parameter and can vary up to \( \pm \)40\% because of the process variations for any op-amp [19]. Consequently, although the datasheet specifies the GBWP to be 1.6 GHz, the value was considered to be 1.28 GHz in this study, about 80\% of the typical value, in order to account for process variations. In the simulation and experiment, if it were to be assumed that the circuits were to be used in the optical sensors such as the laser position sensor QP154-Q (First Sensor), \( C_{f} \) would be expected to be 20 pF. The addition of the sum of the common-mode and differential-mode input capacitances, \( C_{\text{in}, \text{op}} = (0.7 + 4.5 \text{ pF}) \), of OPA657 to \( C_{f} \) yields a \( C_{\text{in}} \) value of 25.2 pF. \( C_{f} \) was set to 0.2 pF by choosing the one of the low-valued practical discrete capacitors. For hardware implementation, the PCB was designed with care to minimize the parasitic capacitance on the board. For example, to make the PCB trace length as short as possible, a feedback element such as \( C_{f} \) was placed just below the op-amp package on the opposite side of the board between the output and inverting input pins of the op-amp.

Under the above assumption, the maximum achievable bandwidth was calculated to be 10 MHz from (1), and the required bandwidth or \( f_{H} \) was assumed to be the maximum value considering the high-speed application. The discrete components were set as \( R_{d} = 1 \text{ k} \Omega, C_{d} = 1 \text{ nF}, C_{e} = 16 \text{ pF}, C_{1} = 100 \text{ nF}, \) and \( R_{\text{dc}} = 5 \text{ M} \Omega \). These values correspond to a gain of 5 M\( \Omega \) from (2). The other components were allowed to vary from case to case.

Simulations were performed for five different cases investigated in this study. The frequency responses for these cases are shown in Fig. 7. Case 1 represents a CF-TIA with a conventional integrator dc-feedback loop topology with \( R_{1} = 632 \text{ M} \Omega \) for \( f_{L} = 20 \text{ Hz} \), \( \alpha = \sqrt{2} \), and \( \tau = 63.2 \text{ s} \). Case 2 shows that gain peaking occurs at \( f_{L} = 638 \text{ Hz} \) with \( \alpha = 0.0446 \) when \( \tau \) and \( R_{1} \) are reduced significantly to 63.2 ms and 632 k\( \Omega \), respectively, from the value for case 1. The stabilized overall gain is shown in case 3 for \( a = \sqrt{2} \), when \( C_{2} = (560 \text{ pF}) \) is introduced in parallel with \( R_{1} \). Note that \( R_{1}, f_{L}, \) and \( \tau \) of case 3 are the same as the value of case 2. The simplified dc-feedback-loop cases are shown in cases 4 and 5 with \( R_{1} = (80 \text{ k} \Omega) \) for \( f_{L} = 20 \text{ Hz} \) and \( \tau = 8 \text{ ms} \). Case 4 represents the single-stage CF-TIA with a wide passband. In particular, case 5 shows that the passband of the single-stage CF-TIA is considerably extended by a differentiator with \( R_{2} = 1 \text{ k} \Omega \). Cases 4 and 5 also

As discussed earlier, \( C_{1}R_{1} \) is the time constant \( \tau \) for the steady state of the system; it is the time required to remove the dc input in the initial state. In (26), \( \tau \) has an inverse relationship with \( f_{L} \). In the conventional configuration, the inverse ratio is significantly large. Under the assumption that \( \alpha = \sqrt{2} \) in (11), \( f_{L} \) of the conventional configuration can be expressed in terms of \( \tau \)

\[
f_{L} = \frac{A_{\text{ol}}}{\sqrt{2\pi \tau}}
\]

where \( A_{\text{ol}} \) is typically extremely large. Thus, if \( f_{L} \) is limited to a low value by the system requirements, \( \tau \) becomes considerably large, resulting in the time taken for dc input removal being extremely long. Conversely, if \( \tau \) is limited to a lower value, \( f_{L} \) becomes significantly large, resulting in the unnecessary attenuation of the low-frequency component of the input signal. The proposed configuration, however, has a considerably lower inverse ratio. Therefore, it can have a considerably lower \( f_{L} \) \( (= 1/(2\pi \tau)) \) for a given value of \( \tau \). Consequently, the proposed configuration allows a larger margin of reduction for \( \tau \), and the gain in the low-frequency band need not be sacrificed. Thus, it is possible to reduce \( \tau \) while achieving an \( f_{L} \) identical to or lower than that of the conventional configuration.

The above discussion was verified by comparing \( f_{L} \) between the conventional and proposed configurations, with \( C_{1} = 100 \text{ nF} \). As shown in Figs. 3 and 5, \( f_{L} \) \( (= 2.5 \text{ Hz}) \) of the proposed configuration in Fig. 5 is ten decades lower than \( f_{L} \) \( (= 638 \text{ Hz}) \) of the conventional configuration in Fig. 3, when \( \tau = 63.2 \text{ ms} \) and \( R_{1} = 632 \text{ k} \Omega \) for both cases. Furthermore, in the proposed configuration, even if \( \tau = 8 \text{ ms} \) with \( R_{1} = 80 \text{ k} \Omega \), we can set \( f_{L} \) \( (= 20 \text{ Hz}) \) as small as that for \( \tau = 63.2 \text{ s} \) and \( R_{1} = 632 \text{ M} \Omega \) in the conventional configuration.

V. SIMULATION AND EXPERIMENT

The presented circuits were implemented and simulated using PSpice to verify the analyses of the transfer functions, design parameters, and performance limits presented in the preceding sections. For the new configuration, namely, the CF-TIA involving a simplified integrator dc-feedback loop,
show that the proposed CF-TIA configuration with a simplified dc-feedback loop can achieve an $f_L (= 20 \text{ Hz})$ as small as that of the conventional configuration with $\tau = 63.2 \text{ s} (R_1 = 632 \text{ M} \Omega)$ in case 1, even if $\tau$ is reduced significantly to 8 ms ($R_1 = 80 \text{ k} \Omega$). The descriptions, features, and parameters of these simulation cases are given in Table I. The analytical results for all these cases are shown in Figs. 3 and 5. The simulation results are in excellent agreement with the analytical results.

In Fig. 8, the experimental results for the newly proposed CF-TIA are compared with the corresponding simulation results. The implemented circuit pertained to cases 4 and 5 of Fig. 7. Measurement results were obtained as follows. The function generator Tektronix-AFG3252 generates an input voltage of the swept-sine wave in a frequency range from 1 Hz to 20 MHz. Then, an input series resistor between the circuit and the function generator converts the input voltage into the input current $i_n$. The CF-TIA amplifies and converts $i_n$ into the output voltage $v_o$, and the digital oscilloscope Keysight-DSOX4104A records $v_o$. Note that the swept-sine wave steps through a range of frequencies, so only one frequency at a given time stimulates the circuit under test. Therefore, it is necessary to capture and hold the peak of the fast Fourier transform (FFT) results to get the frequency-response plot. This is done using the oscilloscope’s internal maximum function after FFT. The voltage level of the function generator or input resistor value can be adjusted depending on whether $v_o$ is within the proper voltage range that can be measured by the oscilloscope.

Evidently, the measurement results are highly consistent with the simulation results up to 10 MHz. Beyond this frequency, the measurement results for the integrator and the bandwidth-extended system start to roll-off by 40 dB/decade, whereas the roll-off frequency is at about 12.6 MHz in the simulation result. At this frequency, the open-loop gain of the op-amp intersects the feedback factor or noise gain ($\approx C_{in}/C_f$). From this frequency, the integrator gain is subject to the open-loop gain of the op-amp, and a slope of $-20 \text{ dB/decade}$ is added to the gain curve.

There are several possible reasons for the roll-off frequency in the measurement results being lower than that in the simulation results, and they include the additional input capacitances in the PCB layout and variations in the parameters of the circuit components. The main reason appears to be that $f_{\text{GPWP}}$ of the op-amp used in the actual implementation is less than the values specified in the datasheet or the simulation model.
parameters because of process variations. This is also likely to be the reason for the experimentally obtained gain curve of the differentiator showing a roll-off of 20 dB/decade around about 10 MHz, which is lower than the frequency expected from the simulation results.

VI. CONCLUSION

In this article, the fundamental performance limits and a detailed analysis of the CF-TIA are presented. Specifically, guidelines are provided for the design of the CF-TIAs, which involves an analysis of the overall transfer functions, an appropriate choice of the critical design parameters, and the consideration of practical aspects for their implementation. Furthermore, a CF-TIA with a simplified integrator dc-feedback loop is introduced. The newly proposed CF-TIA configuration not only simplifies the CF-TIA structure but also has the advantage of having a better tradeoff relationship (small inverse ratio) between the low cutoff frequency and the time constant for the steady state. All the analyses and the new configuration were validated by the excellent agreement among the analysis, simulation, and experimental results. Although high-speed optical sensor applications requiring a wide bandwidth and a high sensor capacitance, such as laser position detectors, were the target applications considered in this study, the analyses presented are also applicable to various measurement sensors, such as emerging biosensors, nuclear science instrumentation, and optical communication systems.

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