Impact of CT saturation on overcurrent relays

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Abstract: An overcurrent relay analyses and processes the secondary currents from a set of current transformers (CTs) and if the currents exceed the operating threshold initiates the tripping of a circuit breaker after an appropriate time. An important issue for a protection relay is how it responds when the steel core of the CT is saturated. The exact behaviour of a CT depends on various factors such as core size, CT ratio, primary current magnitude, DC offset, secondary phasing, remnant flux and the operation of an upstream relay. It is important to ensure that the relay operating times, obtained under similar fault conditions using both the test bench and the test set, will then be compared. The results obtained will then be used to determine how different levels of CT saturation affect different generations of an inverse time overcurrent relays. The final section of this study will explain how CT saturation affects an overcurrent grading study involving a mixture of electromechanical, static and numerical relays.

1 Introduction

A power system generates electricity energy and transports it over overhead lines, transformers and cables to the consumers. The whole system must achieve high levels of reliability and deliver economically affordable electricity to all sections of society at an environmentally acceptable cost. It is inevitable that short-circuit faults will occasionally occur, especially on overhead lines, and the impact of these on the overall network must be minimised by the correct and co-ordinated operation of protection relays. Relay mal-operation, either failure to trip correctly or false operation, causes unnecessary power outages and financial losses.

From the perspective of a radial high-voltage (HV) distribution feeder, the downstream inverse definite minimum time (IDMT) overcurrent relay must minimise the damage caused by a short-circuit fault on the downstream HV feeder or the associated HV: low-voltage (LV) transformers. In addition, the downstream IDMT relay must grade correctly with the protection on the LV feeders and ensure all LV faults are cleared by the LV protection (normally fuses). The exception to this rule is when the LV protection failed to clear the fault and the fault can only be cleared by the downstream HV protection. However, the operation of backup protection normally results in the disconnection of numerous consumers and the majority is connected to un-faulted LV feeders. Similarly, the settings applied to the upstream IDMT relay must ensure it grades correctly with the downstream protection, i.e. it only operates when a fault occurs up-stream of the downstream relay or downstream of this relay, if it failed to clear the fault.

A protection system always consists of current transformers (CTs) and one or more relays and circuit breakers, but it may also include communications with adjacent relays or supervisory control and data acquisition systems. Ideally, CTs convert the primary currents flowing through each pole of the circuit breaker into low-level ‘directly proportional’ secondary currents with the same wave shape. However, once the CT saturates, the secondary current waveform is distorted, which means the CT no longer provides the correct input signals to the relay. This can cause a delay in the relay operating time and in extreme cases might result in the failure of a downstream relay to clear a fault, which increases the risk of damage to the protected plant and/or results in the operation of an upstream relay.

CT saturation is affected by factors related to the ferromagnetic material used in its core. The maximum flux density in the core of a protection CT is typically 1.8 T, which for a given CT size, turn ratio and power frequency are proportional to the voltage across the secondary terminals of the CT. Consequently, when the primary fault current is high and the secondary burden resistance is significant, the likelihood of saturation increases, especially if the fault occurs near a current zero and the X/R ratio of the primary system is high. The resulting DC offset in the primary current will then continue for a few power frequency cycles as shown in Fig. 1. The rate of the DC transient decay is determined by the X/R ratio of the primary network [1]. In addition, the behaviour of a CT also depends on the magnetic state of the core prior to the occurrence of the fault, i.e. it is related to the remnant flux in the CT core.

Various experiments on the physical relay test bench and the power systems computer-aided design (PSCAD) simulation operating with the OMICRON CMC 256–6 test set are discussed in Sections 2 and 3.

2 Experimental setup

2.1 Experiment on the physical relay test bench

The test bench is a three-phase system, consisting of a 415 V voltage source supplied by a 6.6 kV:415 V dedicated transformer, an R–L source impedance, two sets of 1 and 5 A CTs and an R–L model of a transmission line. The magnitude and phase of the source and line impedances are all adjustable, and the turns ratio of the CTs can be set to appropriate values for testing protection relays. In all cases, the tests involving energising a faulted network, with the fault involving one or more phases located at the end of the line. A disadvantage of the test bench is the point-of-wave of fault application is not controllable and consequently cannot adequately test the influence of remnant flux on CT saturation. The circuit diagram is shown in Fig. 2.

2.2 Experiment using PSCAD simulation with OMICRON CMC 256–6

The CTs are represented by a mathematical model based on the ‘Jiles Atherton’ theory in PSCAD [2]. The secondary current signals are then converted into common format for transient data exchange file and replayed using an OMICRON CMC 256–6 test set connected to an overcurrent relay for testing. Compared to using the physical test bench, the PSCAD simulation can control the point-of-wave at which the fault occurs and is removed, and
this allows the effect of remnant flux to be investigated. The connection of the test system is shown in Fig. 3. Fig. 4 below shows the CT model used in PSCAD for simulation. The AC system shown in Fig. 5 consists of a 415 V, 50 Hz voltage source. A single-phase-to-ground fault is applied to end the transmission line.

2.3 Overcurrent relays

As defined by IEC60255, the relay has three IDMT characteristic curves. Each inverse type can be discriminated by current and time relationship illustrated below:

standard inverse (SI) = \( t = \text{TMS} \times \frac{0.14}{(I_{S})^{0.2}} - 1 \)

very inverse = \( t = \text{TMS} \times \frac{13.5}{(I_{S})} - 1 \)

extremely inverse = \( t = \text{TMS} \times \frac{80}{(I_{S})^2} - 1 \)

where TMS is the time multiplier setting, \( I \) is the fault current (CT secondary current) and \( I_s \) is the setting current.

Overcurrent relays are often classified into three types, i.e. electromechanical, static and numerical. In this project, the CDG-36 (electromechanical relay), MCGG-22 (static relay) and MICOM P122 (numerical relay) are tested.

3 Experimental results

3.1 Factors of CT saturation

3.1.1 Effect of DC offset in the primary fault current: When the fault occurs, the primary current may contain an exponential DC transient which affects the build up of the residual core flux [3].

The increase in the flux caused by the primary current may be above the knee point of the CT, which will result in saturation and the distortion of the secondary current. As shown in Fig. 6, the large magnitude waveform is the primary fault current and the small magnitude waveform is the secondary current. Especially, when the fault happens at or near a current zero, the DC offset is maximum and the distortion of the secondary current waveform becomes more severe. The test results of the hysteresis loop, primary fault current and secondary current results from the PSCAD simulation are shown in Figs. 7 and 8 below.

According to Fig. 7, when \( V_{\text{peak}} = 0.339 \text{kV} \) and \( t = 0.465 \text{s} \), there is a minimum DC offset in the primary fault current. However, when \( V_{\text{min}} = 0 \text{kV} \) and \( t = 0.470 \text{s} \), there is a maximum DC offset in the primary current.

3.1.2 Effect of CT secondary burden resistance: Fig. 9 shows that as the burden resistance increases, the CT saturation becomes more severe and distortion of the CT secondary current waveform increases. This is because the higher secondary burden resistance requires more voltage from the CT and the flux density B of the CT core is proportional to \( \frac{V_{\text{burden}}}{t} \). Once the CT is saturated, a large current will flow into the magnetising branch, leading to a reduced secondary current, i.e. distortion of the CT secondary current occurs [4].

3.1.3 Effect of X/R ratio: The X/R ratio of the system represents the duration of the DC offset seen in the primary fault current. Fig. 10 indicates a higher X/R ratio and will produce a larger DC offset under the same condition. In addition, when the X/R ratio...
becomes higher, the secondary current going through the relay is lower during the first cycle. As a result, the waveform of the secondary current is distorted.

3.1.4 Effect of CT ratio: The CT ratio and the CT turns ratio have a reciprocal relationship, Fig. 11 shows that as the CT ratio is lowered, the distortion in the secondary current becomes more significant. For a given primary current and core cross-section area, the excitation voltage varies with the turns ratio and the flux density. Increasing the CT turns ratio leads to a higher excitation voltage, which is more likely to exceed the knee point of the CT excitation curve.

3.1.5 Effect of remnant flux: The presence of remnant flux mainly depends on the point on a wave, where the fault current was interrupted, the magnitude of the primary fault current and the value of the core flux before the interruption [5–7]. The flux magnitude is affected by the secondary impedance, the DC offset and the magnitude of the primary current [6, 7]. When the fault is applied under the CT saturation condition, the remnant flux will reach its maximum. The solution to reduce the remnant flux is to include an air gap in the core [8].

The test results shown in Figs. 12 and 13 are obtained when the first fault occurred at $t = 0.47\, \text{s}$ and the fault duration is $0.5\, \text{s}$ and the second fault: occurred at $t = 0.47 + 0.5 + 0.02\times10 = 1.17\, \text{s}$; i.e. the second fault is applied after ten cycles with the same DC offset as the first fault.
According to Fig. 13, when the first fault is applied, the CT saturation occurs after \( \approx 1.5 \) cycles (non-saturated time: \( \Delta t = 0.5 - 0.471 = 0.029 \) s). Whilst for the second fault, CT saturation takes place after <1 cycle (non-saturated time: \( \Delta t = 1.181 - 1.17 = 0.011 \) s). Thus, remnant flux results in earlier CT saturation.

3.2 Comparison between the test bench and PSCAD simulation

Case 1: TMS = 0.1 s, turn ratio: 36/60, \( X_s = j2.8 \), \( R_b = 0.1 \) Ω, time to apply fault: 0.2776 s. The test results are shown in Figs. 14 and 15.

Case 2: TMS = 0.1, turn ratio: 36/60, \( X_s = 11.2 \), \( R_b = 5.5 \) Ω, time to apply fault: 0.296 s. The test results are shown in Figs. 16 and 17.

3.3 Results obtained when testing overcurrent relays using the physical relay test bench

Scenario 1: The MCGG-22 relay and MICOM P122 relay are connected in series. The circuit diagram is shown in Fig. 18. The CT of the MICOM P122 relay is forced into deep saturation by increasing its burden resistance to 5.3 Ω, the source impedance \( X_s \) is \( j11.2 \) and the setting currents of each relay are set to 1 A. According to the grading study, the TMS of the upstream relay is 0.2 and the TMS of the downstream relay is 0.1, where \( R_{lead} \) is the lead resistance and \( R_b \) is the burden resistance.

The test results are shown in Table 1 and the characteristic curve is shown in Fig. 19.
Fig. 19 shows that when the fault current is small, the effect of CT saturation on the downstream MICOM P122 relay is not obvious, i.e. the grading between the relays is correct. However, when the fault current is large, the CT of the MICOM P122 relay is deeply saturated, i.e. the dashed line shows the tripping time of the saturated relay is significantly delayed. The tripping time of the two relays is similar at high values of current; this leads to incorrect co-ordination.

Scenario 2: the CDG-36 is the upstream relay and the MCGG-22 and MICOM P122 relays are the downstream relays connected in series, see Fig. 20. According to the grading study, the TMS of the upstream relay is 0.2 and the TMSs of the downstream relays are 0.1. If the source impedance $X_s$ is $j11.2$, all the setting currents are 1 A and the CTs of the MCGG-22 and MICOM P122 relays are deeply saturated by increasing the burden resistance to 5.3 $\Omega$, then the test results are shown in Table 2 and the characteristic curve shown in Fig. 21 are obtained.

According to Table 2 and Fig. 21, the operating time of the CDG-36 electromechanical relay is slightly delayed when the fault current becomes large due to the internal high burden resistance of the electromechanical relay. However, the delays are not very significant and do not affect the grading time of upstream and downstream relays. Therefore, CT saturation does not significantly affect the static and the numerical relays; however, it does have an obvious effect on the electromechanical relay (see Fig. 22).

**Table 1** Tripping time with two relays in series

| Turn ratios l and 2 | MCGG-22 (upstream, $R_b = 0.1 \, \Omega$, IEC SI) | MICOM P122 (downstream, $R_b = 5.3 \, \Omega$, IEC SI) |
|---------------------|--------------------------------------------------|--------------------------------------------------|
| $I/I_s$ | Tripping time, s | TMS = 0.2 | $I/I_s$ | Tripping time, s | TMS = 0.1 |
| 6/60 | 2.295 | 1.761 | 2.064 | 1.117 |
| 12/60 | 4.483 | 0.952 | 4.229 | 0.563 |
| 24/60 | 8.407 | 0.658 | 7.653 | 0.466 |
| 36/60 | 12.671 | 0.572 | 9.867 | 0.44 |
| 48/60 | 15.74 | 0.514 | 11.278 | 0.424 |
| 60/60 | 20.549 | 0.486 | 12.083 | 0.422 |

Fig. 18 Network diagram with two relays in series

Fig. 19 $t$–$I$ characteristic curve for scenario 1

Fig. 20 Circuit diagram of three relays in series
3.4 Results obtained when testing overcurrent relays by using PSCAD simulation and the OMICRON CMC 256-6

As shown in Table 3 and Fig. 23, the tripping time of the CDG-36 electromechanical relay is easily delayed when the CT is saturated. For the MCGG-22 and the MICOM P122 relays, the time difference under the two conditions is very small.

4 Conclusion

This paper investigated the impact of DC offset, secondary burden resistance, \( \frac{X}{R} \) ratio, CT ratio and remnant flux on CT saturation. The tests were performed using the physical relay test bench and the PSCAD simulation. The results from these two systems are identical. If the duration of the DC offset is significant and the magnitude of the fault current is high, a high risk exists of incorrect time grading of overcurrent relays, and this would result in the mal-operation of relays. This is especially a problem when the fault current has a high magnitude. By testing CT saturation on different types of overcurrent relays, we can conclude that CT saturation has less influence on the static and the numerical relays as compared with the electromechanical relay.

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### Table 2  Tripping time with an upstream CDG-36 and two downstream relays

| Turn ratios I and 2 | CDG-36 (upstream, \( R_b = 0.1 \Omega \), IEC SI) | Downstream, \( R_b = 5.3 \Omega \) | MCGG-22 (IEC SI) | MICOM P122 (IEC SI) |
|---------------------|---------------------------------------------|---------------------------------|------------------|------------------|
| \( I/I_s \)          | Tripping time, s                              | \( I/I_s \)                      | Tripping time, s | Tripping time, s |
| 6/60                | 2.188                                        | 2.017                           | 2.242            | 1.07             | 1.049             |
| 12/60               | 4.136                                        | 1.007                           | 4.589            | 0.53             | 0.545             |
| 24/60               | 9.603                                        | 0.725                           | 8.004            | 0.375            | 0.382             |
| 36/60               | 12.806                                       | 0.613                           | 10.006           | 0.336            | 0.348             |
| 48/60               | 17.077                                       | 0.549                           | 12.141           | 0.32             | 0.339             |
| 60/60               | 21.348                                       | 0.526                           | 13.477           | 0.306            | 0.334             |

Fig. 21  \( t-I \) characteristic curve for scenario 2

Fig. 22  Screenshot of test interface
| $I_{Is}/I_s$ | CT saturation (maximum DC offset), t/s | No CT saturation (no DC offset), t/s | Calculation value/s (IEC SI) |
|-----------|------------------------------------|-------------------------------------|-------------------------------|
| 2.079     | 1.033 1.148 0.9558 0.9396          | 0.9848 0.7913 0.949               |
| 4.151     | 0.5106 0.5863 0.5403 0.4819        | 0.5031 0.4523 0.485               |
| 8.294     | 0.339 0.3925 0.4215 0.3322         | 0.3402 0.3389 0.324               |
| 12.438    | 0.2895 0.3603 0.4749 0.2722        | 0.2856 0.2938 0.271               |
| 16.575    | 0.2608 0.3456 0.4922 0.243          | 0.2579 0.2691 0.242               |
| 20.718    | 0.2489 0.343 0.5114 0.2332         | 0.2375 0.2616 0.224               |

Table 3 Relay characteristics under CT saturation and no CT saturation

Fig. 23 $t-I$ characteristic curve for three types of relays under different conditions

6 References

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