Modular Reciprocating HVDC Circuit Breaker with Current-limiting and Bi-directional Series-parallel Branch Switching Capability

Jianzhong Xu, Moke Feng, and Chengyong Zhao

Abstract—The high-voltage direct current (HVDC) circuit breaker is becoming popular with the rapid development of the flexible HVDC grid for efficient DC fault ride-through purposes. This paper proposes a novel module for reciprocating HVDC circuit breaker topology, whose branch connections are able to switch between series and parallel modes to limit the rising rate and interrupt the DC fault currents. Diode-bridge sub-modules (DBSMs) are used to compose the main branch for current interruption. Besides fault clearance, the proposed topology has the advantageous function of DC fault current limiting by employing DBSMs with bi-directional conduction capability. The topology can easily switch among branch connection modes through the assembled trans-valves, and their resistance and reactance are very small in the normal state when branches are in parallel and the values become promptly large in the transient state when the branches are series connected. With the modular design, it is easy to change the number of branches or sub-modules and the types of sub-modules to adapt to more specific needs. A 6-terminal modular multi-level converter (MMC) based HVDC grid is established in PSCAD/EMTDC, and various simulation scenarios are carried out to validate the proposed topology.

Index Terms—Reciprocating current limiting, direct current circuit breaker (DCCB), diode-bridge sub-module (DBSM), series and parallel branches, DC fault clearance.

I. INTRODUCTION

With the large-scale application of fully-controlled power electronic devices represented by the insulated gate bipolar transistor (IGBT), high-voltage direct current (HVDC) technology with good controllability and scalability has developed rapidly [1]-[5]. In recent years, research focus has gradually changed from the past point-to-point HVDC transmission to the flexible DC grid. Combined with future potential energy storage facilities, the flexible DC grid can maximize the integration of various renewable energy sources and loads [6]-[8]. However, the DC grid has characteristics of low inertia and low impedance. Thus, after a DC-side short-circuit fault occurs, the fault current will rise sharply in a very short time and will affect the safety and stability of the DC grid [9]-[12].

One of the most reliable fault isolation methods in DC grid is to employ direct current circuit breaker (DCCB). The protection scheme based on DCCB can realize fast fault clearance and system recovery [13]-[16]. Therefore, DCCB is of great significance for stable operation. There are various types of DCCBs according to the main switching type of device, which can be divided into mechanical DCCBs, solid-state DCCBs and hybrid DCCBs [17]. Among them, the hybrid DCCB combines the economy of mechanical DCCB and the response speed of solid-state DCCB, hence has broader application prospects in the DC grid [18].

Figure 1 shows the classical hybrid DCCB proposed by ABB [19], [20], where UFD stands for ultra-fast disconnector and MCB stands for main circuit breaker. Its detailed structure and operation principle are documented very well. Hence a description of those aspects will not be repeated here. This type of hybrid DCCB relies mainly on fully controlled power electronic devices to break a fault current. At present, the use of fully controlled devices such as IGBT is limited by the rated voltage and current of a single device. In the case of a large-scale DC grid, a large number of IGBTs is required to connect in series or parallel to withstand the high voltages and large currents. However, the series-parallel technologies of IGBTs are still facing great challenges [21], [22]. The consistency of the switching action is difficult to guarantee. Moreover, the cost of IGBTs is high, and the wide use of IGBTs will increase the capital costs.

![Fig. 1. Hybrid DCCB from ABB.](image-url)
In order to reduce the fault current interrupting capability and the energy dissipations of DCCBs, current-limiting reactors are usually installed. The current-limiting reactors can help suppress the peak value of the DC fault current. However, for a DC grid at high voltage level, if the steady-state resistance of current-limiting reactors and the on-state resistance of power electronic devices are large, the steady-state performance of the DC grid will be affected. To address this issue, a switchable current-limiting DCCB (CL-DCCB) based on series-parallel connection mode is proposed in [23]. CL-DCCB employs reactors to limit the fault currents for the interruption, as shown in Fig. 2, where MOA stands for metal oxide arrester.

![Fig. 2. Topology of CL-DCCB.](image)

The MCB includes a low loss branch, a power electronic branch and an absorption branch. The branch circuit breakers (BCBs) 1 and 2 have similar structures to MCB, and the branch 2 of BCB is substituted by a capacitor. The BCBs are used for switching the connection mode. When BCBs are connected, current-limiting reactors \( L_1 \), \( L_2 \) and \( L_3 \) are in series, and CL-DCCB has low steady-state resistance. When BCBs are disconnected, \( L_1 \), \( L_2 \) and \( L_3 \) are in parallel, and CL-DCCB has high transient impedance to limit the fault current.

Nevertheless, there are some shortcomings of CL-DCCB. Firstly, when the connection mode switches from parallel to series, the current direction of the \( L_2 \) branch will reverse sharply, and therefore \( L_2 \) will induce a large spike voltage. Secondly, BCBs cut off the branch by first turning off \( T_1 \) and \( T_2 \). Then, the fault current is transferred from branch 1 to branch 2, and the capacitors in Fig. 2 are charged. When the current flowing through branch 1 is approaching 0, the UFD opens and the capacitors are further charged. When the capacitors are fully charged, the BCB will be completely disconnected. The capacitors in CL-DCCB are designed as fault current transfer and circuit breaking components. As the fault current grows fast, BCBs need to break the circuit in a short time. As a result, it is hard to determine a suitable capacitance to balance the fault current transfer and the cooperation with UFD. The demands of fast disconnection is hard to be satisfied too.

To solve the above problems, this paper proposes a modular reciprocating DCCB (MR-DCCB) with diode-bridge submodule (DBSM) as the main working unit. Firstly, the MR-DCCB employs a bridge structure for the reactor \( L_p \) in even number branches. This bridge maintains the current direction of reactor \( L_p \) to avoid abnormal peak voltage. Secondly, the MR-DCCB employs a diode-T-bridge (DTB) in trans-valves (TVs) in replacement of BCB in CL-DCCB. Although DTBs use relatively more IGBTs and diodes, IGBTs in DTB are faster and more stable to break the circuit and change the connection mode than capacitors.

With DBSM, the proposed circuit breaker can be quickly switched between the normal working mode and the current-limiting mode to realize reciprocating current limiting. The topology has a modular nature, and therefore the number of DBSMs and the types of sub-modules can be adjusted if needed.

The remainder of this paper is organized as follows. The topology and working mechanism of MR-DCCB are introduced in Section II, and the analytical expression of the fault current is also derived. Section III validates the correctness of the proposed MR-DCCB and compares it to CL-DCCB proposed in [23]. The overall performance of MR-DCCB in a DC grid is further validated in Section IV. Section V concludes this paper.

II. MR-DCCB

A. Topology

The topological structure of MR-DCCB is shown in Fig. 3(a). The number of branches can be any odd number. It is determined by the voltage level and capacity. The main design principle is to ensure that both the maximum current and its rate of increase do not exceed the allowed value of the DC grid. Figure 3(a) is illustrated by taking three branches as an example. Under this circumstance, the reactance value in the current-limiting mode is 9 times the value in the normal operation mode. This is sufficient to limit fault current if the reactance value is properly designed. In Fig. 3(a), diodes \( D_1 \), \( D_2 \), \( D_3 \), and \( D_4 \) make up a bridge circuit to maintain the direction of current flowing through the reactor \( L_{DCCB} \); \( R_s \) is a discharging resistance for \( L_{DCCB} \); and \( T_i \) is a combination of several IGBTs in series to bypass \( R_s \). The anti-parallel diodes of \( T_i \) are not shown in Fig. 3.
B. Working Mechanism

DBSM is the main working unit of the proposed MR-DCCB, and two of its working states are used, i.e., the blocking state and the bypass state. In the blocking state, T is turned off. D₁, D₄ (with positive current), D₂, D₃ (with negative current), and D₅ will conduct and the current flows through capacitor C. In the bypass state, T is turned on. D₁, D₄ (with positive current), D₂, D₃ (with negative current), and T will conduct so that the current will not flow through C. A similar mechanism also exists in the DTBs of TV, but the current will be cut off if T in DTB is turned off. The entire current paths are shown in Fig. 4.

In order to show the working mechanism of the MR-DCCB is better, a two-terminal HVDC system is simplified to two voltage sources with the same voltage level but slightly different voltage values, as shown in Fig. 5. L₁ and L₂ are the smoothing reactors of the converters at both ends; R₁ and R₂ are the equivalent resistances of the transmission line (including steady-state resistance of smoothing reactors); U₁ and U₂ are the DC voltages of the converters at both ends; iₚ is the total current flowing through the system.

The limiting and breaking process of fault current of MR-DCCB in abnormal operation will be analyzed below. In MR-DCCB, all DBSMs or DTBs in the same branch are controlled in the same way. For simplicity, we use “a branch is blocked/bypassed” to refer to the unified control state of all DBSMs or DTBs in the branch.

When a DC fault occurs, the working processes of MR-DCCB are divided into four successive phases: ① phase 1,
steady-state operation phase; ② phase 2, fault detection and TV delay phase; ③ phase 3, connection mode switching (CMS) and current-limiting phase; ④ phase 4, fault clearing phase. The MR-DCCB is initially involved in the fault ride-through process in phase 3, and the fault current is ultimately cleared in phase 4, as shown in Fig. 6.

Fig. 6. Diagram of working process of MR-DCCB.

The specific analysis of the four phases is as follows.

1) Phase 1 ($t_s$-$t_1$)

In this phase, three BV branches of MR-DCCB are connected in parallel. In BVs and TVs, branch 2 is blocked, and branch 1 is bypassed.

The equivalent circuit of phase 1 is shown in Fig. 7, where $R_{a1}$ is the equivalent resistance of the power electronic devices in branch 1; $L_e$ is the current-limiting reactor; and $R_p$ is the steady-state resistance of $L_e$.

The analytical expression of fault current in phase 2 is:

$$i_a(t) = \frac{U_1}{R_{a1}} + \left( I_1 - \frac{U_1}{R_{a1}} \right) e^{-\frac{t-t_1}{\tau_p}} \quad t_1 < t \leq t_2$$ (2)

where $R_{a1} = R_{a1} + (R_{a1} + R_p)/3$; $\tau_p = L_{a1}/R_{a1}$; $L_{a1} + L_p/3$; and $I_1 = i_a(t_1)$.

Fault current increases exponentially in this phase, and its time constant is determined by the equivalent reactance and resistance from fault point to DC-side outlet of the converter. The values of fault current can increase largely within a few milliseconds.

2) Phase 2 ($t_1$-$t_2$)

One of the challenges of DCCB is fault detection. Because of the high voltage and low impedance of DC grids, the DC fault current increases with an increasing rate of several kilo amperes per millisecond. Most fault detection strategies can only be used as backup protection because of considerable time delay. A feasible scheme is the measured rate of change of voltage (ROCOV) [24], which can be used to confirm the occurrence of a DC fault in a very short time and will be used in this paper. When a DC fault near the MR-DCCB occurs, ROCOV detector detects the fault in a short time [23], and after detection, the MR-DCCB begins to operate. Then, the TV branches receive a break signal. The action processes of TVs are as follows:

1) After receiving the fault signal, branch 2 in TVs is bypassed and branch 1 is blocked. The fault current is transferred from branch 1 to branch 2.

2) When the instantaneous fault current in branch 1 is lower than the allowed breaking value of UFD, UFD begins to break, which usually takes several milliseconds.

Before UFD is disconnected, no current-limiting operations are implemented. Hence, the fault current will develop freely through branch 1 in BVs and branch 2 in TVs. The equivalent circuit in phase 2 is shown in Fig. 8.

Fig. 7. Equivalent circuit of phase 1.

The steady-state current can be calculated by:

$$i_a(t) = \frac{U_1}{R_{a1} + R_p + \frac{2}{3}(R_{a1} + R_p)} \quad t \leq t_1$$ (1)

The steady-state current is mainly affected by the voltage difference and transmission line resistance of the converter stations at both ends.

3) Phase 3 ($t_2$-$t_3$)

During time $t_2$-$t_3$, after UFD is fully disconnected, branch 2 in TVs is blocked to break the TV branches, and the connection mode changes from parallel to series.

At the same time, branch 1 in BVs is blocked. Capacitors in branch 1 are inserted into the circuit to be charged, which is also the preparation for current transfer.

The equivalent circuit is shown in Fig. 9. MR-DCCB2, $R_{a2}$, $L_{a2}$ and $U_{a2}$, which have no influence on MR-DCCB1 during the fault, are intentionally omitted.

In phase 3, the equivalent circuit of the MR-DCCB1 changes suddenly at $t_2$. Therefore, the Laplace transformation is used to solve the circuit in the frequency domain.

The number of series capacitors in branch 1 of BV is much smaller than that in branch 2, thus the majority of the short-circuit current still flows through branch 1 when both branches 1 and 2 are blocked.
The operation circuit of Fig. 9 is shown in Fig. 10, where $s$ is the Laplacian; $I_2$ is the fault current value at time $t_2$; $R_{eq}$ is the equivalent resistance; and $u_{C}(t_2)$ is the capacitor voltage at time $t_2$.

The analytical expression of the fault current in the CMS process is calculated as:

$$i_m(t) = \frac{A}{L_{eq}} e^{-\frac{s}{\tau_2}} (\cos \omega_s (t-t_2) + \frac{k_3}{s} \sin \omega_s (t-t_2)) \quad t_2 < t \leq t_3 \quad (3)$$

where $A=L_{eq} I_2 + L_2 I_2$; $L_{eq}=L_{eq} + 3L_p$; $R_{eq}=R_{eq} + 3(R_{on} + R_p)$; $\omega_s = \sqrt{3N_c/(L_{eq} C) - 1/t_\tau^2}$; $\tau_2 = 2L_{eq}/R_{eq}$, and $k_3 = (U_i \tau_2 - A)/(AR, \omega_s)$.

The DBSM capacitors will be charged to the rated voltage in a very short time. After capacitors are fully charged at time $t_3$, branch 2 is bypassed to transfer the current from branch 1 to branch 2. MR-DCCB works in current-limiting mode during time $t_2$-$t_4$. The fault current transfer process is illustrated in Fig. 11.

Before time $t_4$, if the fault has been cleared, the fault current will not continue to increase. The DBSMs and TVs can be re-triggered to bypass branch 1 and block branch 2 to return to normal operation. Otherwise, a breaking operation is required.

After the protection device determines that a breaking operation is required, the current of branch 1 is detected. When it is less than the allowed breaking value of UFD, the opening signal is given. In general, the breaking of UFD needs approximately a delay of 2 ms. During the delay phase, the fault current is still free to develop because the transfer branch is still in the bypass state.

The equivalent circuit of the current-limiting process is shown in Fig. 12. $R_{eq}$ is the equivalent resistance of the power electronic devices that are inserted into branch 2. The analytical expression of fault current in phase 3 is:

$$i_m(t) = \frac{U_i}{R_{eq}} + \left[ I_3 - \frac{U_i}{R_{eq}} \right] e^{-\frac{s}{\tau_2}} t_3 < t \leq t_4 \quad (4)$$

where $I_3 = i_m(t_1)$; $\tau_2 = L_{eq}/R_{eq}$.

The fault current in phase 4 is calculated as:

$$i_m(t) = Ce^{-\frac{s}{\tau_5}} \left[ \frac{K_1}{\tau_5} + K_2 \omega_s \cos \omega_s (t-t_4) + \frac{K_3}{\tau_4} - K_4 \omega_s \sin \omega_s (t-t_4) \right] t_4 < t \leq t_5 \quad (5)$$

where $\tau_5 = [2(L_{on} + 3L_p)]/[\{9(R_{on} + R_p)\}^2]$; $\omega_s = \sqrt{12N_c(L_{on} + 3L_p) - 9(R_{on} + R_p)^2 C^2/2}^+$; $I_4 = i_m(t_4)$; $K_1 = -U_i/(3N_c)$; and $K_3 = [(I_4/C) - (K_4/\omega_s)]/\omega_s$.

After fault clearance, $T_i$ is turned off to input discharging resistance of $L_{on}$ into the circuit to dissipate the energy in $L_{on}$.

The above analytical expressions will be validated in the following subsections by comparing the results with those obtained from the detailed electromagnetic transient (EMT)
III. VALIDATION OF MR-DCCB

A. Topology Validation in Test System

A test system is set up as shown in Fig. 5. The system parameters are given in Table I. DC short-circuit fault occurs at \( t_i = 4 \) s.

| Item                        | Value     |
|-----------------------------|-----------|
| Rated voltage of station \( U_1 \) | 500 kV    |
| Rated voltage of station \( U_2 \) | 499 kV    |
| Smoothing reactance \( L_s \) | 100 mH    |
| Current-limiting reactance \( L_p \) | 90 mH     |
| Steady-state resistance of current-limiting reactor \( R_p \) | 0.1 Ω   |
| Line equivalent resistance \( R_e \) | 0.25 Ω   |
| Sub-module capacitance \( C \) | 200 μF   |

The total current flowing through the MR-DCCB \( (I_{\text{DCCB}}) \) and the current of the branches in BV \( (I_{\text{branch1}}) \) for branch 1, \( I_{\text{branch2}} \) for branch 2, and \( I_{\text{MOA}} \) for branch 3) are shown in Fig. 14.

Fig. 14. Fault current waveforms of MR-DCCB during short-circuit fault.

Following Section II-B, the waveforms are also divided into the following phases.

1) Time \( t_1-t_2 \) phase 1. The fault occurs at time \( t_1 \).
2) Time \( t_2-t_3 \) phase 2. In this phase, the fault current rapidly develops from a steady-state value of 1.87 kA to 9.25 kA.
3) Time \( t_3-t_4 \) phase 3. Before \( t_3 \), TV branches are blocked to change the connection mode from parallel to series. In this process, the reactance of the topology increases by 9 times the steady-state value. Shortly the fault current is transferred from branch 1 to branch 2. After \( t_3 \), fault current develops at a lower rate to wait for the disconnection of the UFD in branch 1.
4) Time \( t_4-t_5 \) phase 4. After the UFD is fully disconnected, branch 2 in BV is blocked, the fault current charges the DBSMs, and then discharges through the arrester. The TV is responsible for changing the structure of the circuit. Figure 15 shows the voltage across TV during the operation of MR-DCCB.

![Fig. 15. Voltage stress of TV.](image)

When the circuit structure changes suddenly, the voltage across it will be interrupted, and thus a certain number of DBTs are required to be connected in series to prevent device damage.

B. Performance Comparison

In this section, MR-DCCB is compared with CL-DCCB proposed by [23]. The test system is the same as that in Section III-A. A short-circuit fault occurs at \( t = 4 \) s. The total current flowing through the two topologies is shown in Fig. 16.

![Fig. 16. Total current comparison between CL-DCCB and MR-DCCB.](image)

As shown in Fig. 16, MR-DCCB is almost three times faster than CL-DCCB in completely cutting off the fault current. Also, the total period of large fault current is much shorter. Due to the existence of a capacitor in Fig. 2, the equivalent circuit of CL-DCCB is an RLC oscillating circuit, and the fault current will oscillate while decreasing. This would prolong the process of current decrease. The DBSM structure in MR-DCCB prevents the oscillation and makes the whole cut-off process of current controllable. Thus, MR-DCCB has an advantage of stability and rapidity over CL-DCCB.

C. Validation of Analytical Results

The accuracy of the analytical calculation results is checked by comparing with the simulation results from PSCAD/EMTDC. The test system built in Section III-A is used and the fault current waveforms of all phases are plotted in Fig. 17.
It can be seen that the two curves fit very well from phase 1 to phase 5 before the arrester operates. It is also observed that in the nonlinear region of the arrester, the analytical results of MR-DCCB do not agree with the detailed simulations. This is because the transient characteristics of MR-DCCB can only be described by the analytical equations in Section II-B before the arrester operates. When the arrester operates, it is very difficult to perform accurate analytical analysis.

D. Economic Analysis

In this section, we give detailed comparisons between the proposed MR-DCCB, DCCB from ABB, DCCB from the Global Energy Interconnection Research Institute (GEIRI) of the State Grid Cooperation of China and CL-DCCB.

IGBT 5SNA 2000K450300 is adopted to analyze economic performance. The rated parameter of the IGBT is 4.5 kV/2 kA [25], the nominal voltage is 3 kV considering the security margin, and the peak interrupting current is 9 kA when applied to DCCB [19]. The diode model 5SDD 36K5000 is selected and its nominal parameter is 5 kV/3.6 kA.

Considering a ±500 kV two-terminal HVDC system, the peak breaking value for DCCB is 1.5 times the rated voltage [13]. Considering the allowed safety value and the characteristic of arresters, the DCCB should tolerate a voltage of 800 kV. Under this condition, both the ABB and GEIRI schemes need 1072 IGBT modules for bi-directional fault current breaking, and the CL-DCCB needs 540 IGBT modules, 1068 standalone diodes and 356 capacitors.

As for the MR-DCCB in this paper, in each DBSM, T bears the voltage of the sub-module capacitor. The rated voltage of one DBSM is set to be 4.5 kV, and the peak interrupting current is 9 kA. Therefore, to break the fault current with a maximum value of 9.25 kA (3.08 kA for each BV in parallel) and voltage of 800 kV, 267 DBSMs in total are needed in branch 2 for BV. Since the TV needs to break 2/3 of the current and voltage, 356 DTBs in total are needed in branch 2 of the TV. In addition, there are 15 DBSMs in branch 1 in BV and 2 IGBTs in branch 1 in TV. The total number of required IGBTs is 642, the total number of required standalone diodes is 2834, and the total number of required capacitors is 282.

Table II gives the device comparison of four schemes. For the application of high voltage and large current, the price of IGBT is about 10 to 20 times that of diodes and capacitors. To compare the total cost of DCCBs, the cost of diodes and capacitor are set to unit 1, and the cost of IGBT are set to the average value of 15. As the number of UFD is very small and the cost is low, the price of UFDs is ignored. IGBT module is defined as an IGBT/diode pair.

### Table II Comparison of Four Schemes

| Scheme    | IGBT module | Standalone diode | Capacitor | UFD | Total cost |
|-----------|-------------|------------------|-----------|-----|------------|
| ABB       | 1072        | 0                | 0         | 1   | 17152      |
| GEIRI     | 1128        | 0                | 282       | 1   | 18330      |
| CL-DCCB   | 540         | 1068             | 356       | 3   | 10064      |
| MR-DCCB   | 642         | 2834             | 282       | 5   | 13388      |

The total cost of the MR-DCCB is 21.94% less than the ABB scheme and 26.96% less than the GEIRI scheme. It will save more than 1/5 of the DCCB cost. Although MR-DCCB costs 24.83% more than CL-DCCB, it has more advantages such as stability and rapidity over CL-DCCB, as shown in Fig. 16, which is also its main innovation. The significantly improved current limiting and breaking performance of MR-DCCB can well compensate for the larger cost, and is potential for the application in a future DC grid.

IV. TOPOLOGY VALIDATION IN DC GRID

The performance of MR-DCCB in an actual DC grid is verified in this section. The diagram of the 6-terminal HVDC system and the system parameters are shown in Fig. 18 and Table III.
The start-up process of the DC grid is not simulated in this paper, and we assume that the DC grid has already reached steady state before the fault. At $t_f = 1.5$ s, a pole-to-pole short-circuit fault occurs at the fault point shown in Fig. 18. The total current flowing through the circuit breaker during the fault and the current flowing through branch 1 and branch 2 in BV are shown in Fig. 19.

In Fig. 19, it can be seen that the proposed MR-DCCB has shown its capability in fault current limiting and clearing. However, the DC fault in the power grid leads to a rapid drop of the DC voltage of the converter, which will cause the grid voltage to be unbalanced. Therefore, it is necessary to reconstruct the system voltage during the fast power recovery stage. After using the MR-DCCB for current limiting and braking, the capacitor discharging process of the modular multi-level converters (MMCs) can be slowed and the DC voltage of MMC can be maintained, as shown in Fig. 20. In Fig. 20, when the MR-DCCB is not activated, the DC voltage of the converter continues to decrease after the fault; and if the MR-DCCB is activated, the DC voltage of the converter can be maintained.

Based on the above analysis, before $t = 1.504$ s (period $t_p - t_f$), the fault current flows over the MR-DCCB and the MR-DCCB is not fully disconnected. The DC voltage of the converter continues to decrease. The rate of decrease is the same as the situation where there is no MR-DCCB. After $t = 1.504$ s, the MR-DCCB is fully disconnected, and the fault will no longer affect the DC voltage. Therefore, the DC voltage is kept near a certain value (310 kV in Fig. 20) and would not decrease further. About 62% of the rated DC voltage remains.

A larger residual DC voltage is conducive to power recovery after a severe DC short-circuit fault of the DC grid. Therefore, the MR-DCCB is beneficial in maintaining the DC voltage after a fault.

V. CONCLUSION

An MR-DCCB with current-limiting and bi-directional series-parallel branch switching capability is proposed in this paper. The current-limiting and breaking processes of the MR-DCCB are analyzed, and each working phase is mathematically calculated. The calculation results are verified by simulation and the conclusions are as follows.

1) Multiple branches are connected in parallel in steady state so that the system is almost not influenced by the MR-DCCB. The loss of the MR-DCCB is relatively low, and it can effectively dissipate the energies in the current-limiting inductors. During the transient state, branches are connected in series, so the impedance is high, and the fault current can be quickly cleared.

2) The DBSM are employed in MR-DCCB as the main device. Each branch can interrupt bi-directional DC fault current. The modular nature of the new topology can easily change the number of paralleled branches, the number of series DBSMs and the sub-module types.

3) The MR-DCCB is validated by detailed simulations on PSCAD/EMTDC. It is capable of limiting the fault current and clearing the fault within 7 ms, thus it has a good application prospect in future DC grid.

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