An abstract semantics of speculative execution for reasoning about security vulnerabilities

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Abstract. Reasoning about correctness and security of software is increasingly difficult due to the complexity of modern microarchitectural features such as out-of-order execution. A class of security vulnerabilities termed Spectre that exploits side effects of speculative, out-of-order execution was announced in 2018 and has since drawn much attention. In this paper we formalise speculative execution and its side effects with the intention of allowing speculation to be reasoned about abstractly at the program level, limiting the exposure to processor-specific or low-level semantics. To this end we encode and expose speculative execution explicitly in the programming language, rather than solely in the operational semantics; as a result the effects of speculative execution are captured by redefining the meaning of a conditional statement, and introducing novel language constructs that model transient execution of an alternative branch. We add an abstract cache to the global state of the system, and derive some general refinement rules that expose cache side effects due to speculative loads. Underlying this extension is a semantic model that is based on instruction-level parallelism. The rules are encoded in a simulation tool, which we use to analyse an abstract specification of a Spectre attack and vulnerable code fragments.

1 Introduction

Modern multicore architectures exhibit several features to speed up execution: commands may appear to occur out of order, allowing computation to proceed past some bottleneck (e.g., loading a value from memory), several levels of faster intermediate memory (caches) to speed up repeated accesses, and in particular, speculative execution, where a branch is optimistically executed, even though local computation may not yet have determined if it is the correct branch. Such features are difficult to reason about, though there has been significant work in understanding weak memory models [37,2,36,1,15,23] and also detailed formal microarchitectural models (e.g., [4]).

Recently several significant security vulnerabilities have been found related to out-of-order execution, e.g., Meltdown [28], Foreshadow [5], and Spoiler [22]. In this paper we focus on the recently published Spectre class of attacks [25,24]. Spectre differs in that the attack may target the victim’s code to retrieve private
information, while other attacks exploit processor features only. While complex
to exploit, Spectre is a vulnerability present in almost all modern architectures.
It allows malicious code to access the memory of a victim process, potentially
reading private data, without sharing the virtual memory space. The attack
works by detecting footprints in the cache left by speculative execution; for
instance, a branch that includes a bounds check on an index $i$ into an array $A$
may speculatively load the element at $A[i]$, before it knows for certain that $i$
is within the bounds of $A$. Though the speculative computations leading up to
the point where the mis-speculation is detected are discarded, depending on the
subsequent access patterns there may still be an effect on the cache, which is not
discarded, and which can be used to infer the value in memory at out-of-bounds
address $A[i]$. In earlier work we have proposed a semantic framework to support reasoning
about weak memory models [12] which is implemented in a simulation/model
checking tool based on Maude [8]. In this paper we extend this framework with
a model of cache behaviour and speculative execution. Although Spectre may
occur in memory models that provide sequential consistency, a weak memory
model framework is a natural fit for speculative execution as speculated instruc-
tions may begin out of order, i.e., before the relevant branch is reached. This
enables not only a close inspection of Spectre-like attacks but also the analysis
of other related potential vulnerabilities that may arise in modern hardware ar-
chitectures. Our intention for the semantics is to allow analysis of vulnerability
to Spectre-like attacks to be integrated within a more general, software-level
reasoning framework; we do not aim to precisely model the implementation of
speculative execution or caches for a particular architecture.

Speculative execution presents several challenges. Firstly, it requires a model
of the cache which, for our concerns, needs to be modelled at a level that presents
enough details to realistically capture the effects of speculative execution, but is
abstract enough to not over-complicate reasoning. Secondly, speculative execution
should allow side effects to take effect before the relevant branch is reached.
Thirdly, speculation can be nested, and the target of future branches may depend
on speculatively executed computations, necessitating the creation of transient
state that can be easily discarded. Finally, we want to be able to model and
explore possible mitigations, e.g., memory barriers to halt speculation, such as
Intel’s LFENCE instruction [21, Sect. 11.4.4.3].

The paper is structured as follows: in Sect. 2 we summarise a wide-spectrum
language and its semantics for reasoning about weak memory models. In Sect. 3
we extend this with new constructs for reasoning about speculative execution,
and give its semantics. We formalise some attacker and victim patterns, in par-
ticular those of Spectre, in Sect. 4. Related work is discussed in Sect. 5.

2 Background: IMP-ro

A wide-spectrum language for reasoning about weak memory models, IMP-ro, is
introduced in [12,11]. It is essentially an imperative language with assignments,
conditionals and loops, with the difference that instead of sequential composition
\( (c_1 ; c_2 \text{ for } c_i \text{ a command}) \) it has prefixing, \( \alpha ; c \), where \( \alpha \) is an instruction (as in process algebras such as CSP \([20]\) and CCS \([31]\)). The semantics of prefixing is defined so that either \( \alpha \) may be executed, or some instruction \( \beta \) from within \( c \) may be executed, provided that \( \beta \) can be reordered before \( \alpha \) according to the rules of the memory model. To instantiate \( \text{IMP-ro} \) for a particular memory model a “reordering relation” \( \trianglerighteq \) on instructions is defined, stating when instructions can occur out of order; in addition, different models may also have different instruction types, for instance, memory barriers for enforcing order.

We recap \( \text{IMP-ro} \) below, before extending it to include speculative execution in later sections. We ground our work in a weak memory framework because speculation can occur before preceding instructions are executed, even when speculative execution is implemented on architectures which enforce sequential consistency. In addition, it appears that increasingly security vulnerabilities will be found due to instruction reordering on modern architectures, e.g., \([22]\). However, the particular reordering relation is not important for the analysis in this paper, and to avoid distraction we mostly assume sequential consistency.

The elements of \( \text{IMP-ro} \) are actions (instructions) \( \alpha \), commands (programs) \( c \), processes (local state and a command) \( p \), and the top level system \( s \), encompassing a shared state and all processes. We assume a set of variables \( \text{Var} \), divided into locals (registers) and globals. By convention we use \( r, r_1, r_2, \) etc., to name local variables, and unless otherwise stated, \( x, y, z \) for global variables. A state \( \sigma \) is a mapping from \( \text{Var} \) to values, with the notation \( \sigma[x:=v] \) representing an update of \( \sigma \) to map \( x \) to \( v \). Below \( x \) is a variable (shared or local) and \( e \) an expression.

\[
\begin{align*}
\alpha &::= x := e \mid [e] \\
c &::= \text{nil} \mid \alpha \cdot c \mid \alpha \sqcap c \mid c_1 \sqcap c_2 \mid \text{while } b \text{ do } c \\
p &::= (\text{local } \sigma \cdot c) \\
s &::= (\text{global } \sigma \cdot p_1 \parallel p_2 \parallel \ldots)
\end{align*}
\]

An action may be an update \( x := e \) or a guard \([e]\). For weak memory models the set of actions may also include fences (memory barriers); we introduce an abstract barrier in later sections. Commands include the terminated command \( \text{nil} \), prefixing, choice, and iteration. We also include the abstract command type for “true prefixing”, \( \alpha \cdot c \), where reordering is forbidden, i.e., \( \cdot \) is prefixing in the usual CSP \([20]\) and CCS \([31]\) sense. For brevity, for a command \( \alpha ; \beta ; \text{nil} \) we omit the trailing \( \text{nil} \) and just write \( \alpha ; \beta \). A process encapsulates a command within a local state \( \sigma \) (total on local variables), representing registers. A system is structured as the parallel composition of processes sharing a global state, each with their own values for local variables.

A relevant subset of the operational rules are given in Fig. 1. Transitions are labelled with the syntax of the transition, i.e., assignments and guards, with the addition of the silent label \( \tau \), modelling an internal step of a process with no effect on the context. For brevity and ease of explanation we tend to focus on rules involving guards of a particular form, \([x = v]\), which represents a load of \( x \)
Rule 1 (Prefix)

\[(\alpha; c) \xrightarrow{\alpha} c \quad (a)\]

\[c \xrightarrow{\beta \; c'} \xrightarrow{\beta_{(\alpha)}} (\alpha; c') \quad (b)\]

Rule 2 (Choice)

\[c \ominus d \xrightarrow{\tau} c\]

\[c \ominus d \xrightarrow{\tau} d\]

Rule 3 (While)

\[\text{while } b \text{ do } c \xrightarrow{\tau}\]

if \(b\) then \((c; \text{ while } b \text{ do } c)\) else nil

Rule 4 (Locals)

\[c \xrightarrow{\tau} \]

Rule 5 (Locals/store)

\[c \xrightarrow{\tau} \]

Rule 6 (Locals/load)

\[c \xrightarrow{\tau} \]

Rule 7 (Locals/guard)

\[c \xrightarrow{\tau} \]

Rule 8 (Parallel)

\[p_1 \xrightarrow{\alpha} p_1' \]

\[p_2 \xrightarrow{\alpha} p_2' \]

\[p_1 \parallel p_2 \xrightarrow{\alpha} p_1' \parallel p_2' \]

Rule 9 (Globals/store)

\[p \xrightarrow{\tau} \]

Rule 10 (Globals/load)

\[p \xrightarrow{\tau} \]

when \(x = v\). The more general rules are given in [12]. We omit some rules, such as terminating rules like \((\text{local } \sigma \bullet \text{nil}) \xrightarrow{\tau} \text{nil}\).

Rule 1 is the key rule that allows later instructions to happen earlier, according to an architecture-specific reordering relation \(\prec\). For instance, for TSO, the main part of the reordering relation is that loads can come before stores, i.e., \(x := 1 \xrightarrow{\text{TSO}} r := y\), while \(\alpha \not\prec \beta\) for all other instruction types. Relations for TSO, ARM and POWER are given in [12]. To avoid distraction in this paper we assume sequential consistency, i.e., \(\alpha \not\prec \beta\) for the basic instruction types, with the exception that \(\tau\) steps can be reordered (allowing future local calculations to be executed ahead of time). In Rule 1 the notation \(\beta_{(\alpha)}\) accounts for forwarding, where in a case such as \(x := 1; r := x\) the instruction \(r := x\) can take effect before \(x := 1\) provided the value 1 is forwarded to \(r\), meaning that \(r := 1\) is executed (rather than \(r := x\), which it would not be sensible to execute before \(x := 1\) from a sequential semantics perspective). Forwarding is defined straightforwardly in
and we do not repeat it here. The semantics for true prefixing, \( \alpha \cdot c \), is given by an equivalent version of Rule 1(a).

Rule 2 is straightforward for nondeterministic choice. In Rule 3 we unfold a loop into a conditional; the definition of conditional in a speculative context is crucial and is deferred until Sect. 3.2. Rule 4 covers the case of some change to the local registers. This is an internal step of the process and is a silent \( \tau \) step at the global level. Rule 5 applies when a store \( x := r \) is executed by a process; the local value \( v \) for \( r \) is substituted so that the label \( x := v \) is promoted to the global state (this rule can be generalised to cover any assignment of the form \( x := e \) (10)). Rule 6 states that when a load \( r := x \) instruction is executed internally it becomes a load of \( x \), i.e., a guard \([x = v]\), for any value \( v \). Although there is a transition \([x = v]\) for every possible \( v \), only the guard with the correct value for \( x \) will be possible at the system level (via Rule 10). The loaded value becomes the new value for \( r \) in the local state. Rule 7 states that a guard is evaluated with respect to the registers, and is promoted for evaluation with respect to the global state. Rule 8 gives the usual interleaving model of concurrency. Rules 9 and 10 straightforwardly update and access the global store via promoted stores (Rule 5) and loads (Rule 6).

Refinement \((\sqsubseteq)\) is defined so that \( c \sqsubseteq d \) iff all terminating traces of \( d \) are also traces of \( c \), ignoring subsequences of internal \((\tau)\) steps. Terminating traces are those retrieved from the operational semantics where eventually \textit{nil} is reached. (For simplicity we ignore non-terminating behaviours, that is, for this paper we consider only partial correctness, which is sufficient for detecting Spectre-like attacks.) Note that if a behaviour is blocked (no rules are applicable, e.g., a false guard) it is not considered terminating. This eliminates behaviours where the wrong branch is incorrectly taken (as opposed to incorrectly speculated), as discussed in more detail in [12].

We lift reasoning from the operational to refinement level via Law 11 which allows us to straightforwardly derive Law 13. More specific laws may also be straightforwardly derived, such as resolving nondeterminism via Law 12, and Law 14 that hides local effects, exposing a process’s global effect; this helps later to abstract from the details of transient speculative contexts.

\[
c \xrightarrow{\text{c}} c' \Rightarrow c \sqsubseteq \alpha \cdot c' \quad (11)
\]
\[
c_1 \cap c_2 \subseteq c_1 \quad (12) 
\]
\[
\alpha ; c \sqsubseteq \alpha \cdot c \quad (13)
\]
\[
(\text{local } \{r \mapsto 1\} \bullet x := r) \sqsubseteq x := 1 \quad (14)
\]

3 Caches in weak memory models: IMP-ro-spec

From the perspective of functional correctness, speculative execution may be ignored; in the case where a process speculates along the branch that is eventually taken (after the conditional is evaluated) implementations ensure that speculated instructions are committed in a consistent order; and when speculation was

\footnote{In this paper we assume a multicycle atomic storage system; for memory models which lack this (e.g., POWER) the storage system described in [12] may be used.}
down the incorrect branch any speculative computation is discarded. However, as revealed by Spectre and other vulnerabilities, incorrect speculation can have side effects, and in this section we extend IMP-ro to expose them.

For convenience we call the extended language IMP-ro-spec, which defines conditionals to expose (incorrect) speculative execution, and records operations on the cache in a global variable. Speculation occurs within a transient context, which is discarded if speculation is found to be incorrect.

3.1 Syntax of IMP-ro-spec

Speculative execution. We introduce three new commands to capture speculative execution in IMP-ro.

\[
\alpha ::= \ldots | \text{SPECFENCE} \tag{15}
\]

\[
c ::= \ldots | \text{spec}(c) | c_1 \triangle c_2 | (\text{buf } \sigma \bullet c) \tag{16}
\]

\[
\tilde{c} \equiv (\text{buf } \emptyset \bullet (\text{local } \sigma \bullet c)) \tag{17}
\]

\[
\text{if } b \text{ then } c_1 \text{ else } c_2 \equiv \text{spec}(\tilde{c}_2) \triangle ([b] ; c_1) \cap \text{spec}(\tilde{c}_1) \triangle ([\neg b] ; c_2) \tag{18}
\]

The instruction type SPECFENCE blocks load speculation; this is an abstract command type that may correspond to, for instance, the LFENCE command of Intel architectures \[21\]. We include it to demonstrate the relevance of reordering relations and how mitigation techniques can be considered in our framework. A speculation command \text{spec}(c) gives the effect of executing command \(c\) speculatively, that is, no effects on the global or local state can be seen, however, there can be cache side effects based on the steps of \(c\). A partial pre-execution command \(c_1 \triangle c_2\) partially executes \(c_1\) before \(c_2\) begins. The initial command \(c_1\) may not execute at all, execute to completion, or partially execute. It is the well-known CSP “interrupt” operator, but we rename it in this context to avoid confusion with hardware interrupts. The transient buffer command \((\text{buf } \sigma \bullet c)\) is used to keep track of modifications to globals executed speculatively.

We also introduce the abbreviation \(\tilde{c}\) which creates the transient context for a speculative execution of \(c\), that is, a (temporary) mapping of (all) registers, and an initially empty transient buffer [17]. The values for the speculative copy of registers \(\sigma\) created here is left unconstrained and may differ to the actual local state in the outer context; this accounts for different strategies that different architectures may take. Because the specifics of the local state are not relevant for reasoning about Spectre we do not model a specific strategy, which could be given by adding an explicit transition that sets up the local state according to the current context. A speculative execution of code \(c\) is of the form \text{spec}(\text{buf } \sigma_y \bullet (\text{local } \sigma_l \bullet c))\), where a copy of the locals is encapsulated in \(\sigma_l\), stores to globals are encapsulated in \(\sigma_y\), and the outer speculative command generates the cache side effects. An example of how they interact is given in Sect. 3.3.

Speculation is evident at branch points, and hence we model conditionals differently. Whereas in [12] a conditional \text{if } b \text{ then } c_1 \text{ else } c_2\ was defined in the standard way as \(([b]; c_1) \cap ([\neg b]; c_2)\) here we extend the definition to potentially pre-execute speculation down the alternative branches as given in (18). This says
there are two possibilities: speculatively execute the second branch (ignoring the guard) up until the point where the first branch is chosen, or speculatively execute the first branch until the point the second branch is chosen. These two possibilities cover all behaviours relevant in the context of Spectre; as far as is known speculation down the eventually correct branch has no impact on the security of the system that is not already visible through other analysis techniques, e.g., information flow \cite{33}. However, speculation down the correct branch is straightforward to capture, as discussed in Appendix A.

To explain the relevance of the transient context (initialised in (17)) consider the execution of $\text{spec}(x := 1; \ r := x; \ldots)$. The effect of $x := 1$ must not be seen globally (as it is difficult to unwind), however during speculation $r$ must use the value 1. If instead $r$ was to use a value of $x$ loaded from main memory this would violate local consistency (see \cite{1}). This detail is especially important if $r$ is used in later (speculated) calculations, including future branches. In our approach it emerges from the semantics that $x$ is not loaded nor drawn into the cache during speculation of the above code. A purely syntactic approach to determining the effect of speculative execution might conclude that $x$ is added to the cache, and hence could be overly pessimistic from a security analysis perspective.

Nested speculation, which may arise from nested conditionals or a speculated loop, is straightforward in our framework; a new, nested, transient context is created, and if an inner speculation attempts to load a global which the outer speculation has buffered then the cache effect is removed (see Rule 24(e)).

The cache. The cache is modelled as a single global variable \texttt{CACHE}, kept in the shared state, which holds a set of type $\texttt{Addr}$, representing addresses (for this work we do not care what values are in the cache; however it is straightforward to modify the type of \texttt{CACHE}). We assume an uninterpreted function $\&: \texttt{Var} \rightarrow \texttt{Addr}$ such that $\&x$ returns the address of the (global) variable $x$. We introduce three operations on \texttt{CACHE} to model cache side channels abstractly: cache fetching (adding something to the cache), cache clearing (clearing the (entire) cache), and cache querying (checking if an address is in the cache). Other explicit cache operations could be added, but these are sufficient for modelling the attack patterns utilised to instrument Spectre attacks \cite{25}.

\begin{align*}
\texttt{CACHE} := x & \equiv \texttt{CACHE} := \texttt{CACHE} \cup \{ \&x \} \quad (19) \\
\texttt{cclear} & \equiv \texttt{CACHE} := \emptyset \quad (20) \\
x \in \texttt{CACHE} & \iff \&x \in \texttt{CACHE} \quad (21)
\end{align*}

As these are abbreviations for updates to and guards on a global variable they fit in with the framework introduced in Sect.\ref{sec:framework}. A cache fetch represents the side effect of a speculated load. The instruction \texttt{cclear} captures abstractly flushing as well as eviction of particular cache lines as it ensures that a certain address is not present in the cache any more.

The variable \texttt{CACHE} is kept in the global state and hence is shared between all processes. An alternative would be to explicitly model it as a separate construct,
e.g., \((cch\ C \bullet c)\) where \(C\) is a set of addresses. This approach would allow more fine-grained control over cache levels, e.g., each process could have its own L1 cache, with some subset sharing an L2 cache, with the L3 cache at the top level.

\[
(cch\ L3 \bullet (cch\ L2_a \bullet (cch\ L1_1 \bullet p_1) \parallel (cch\ L1_2 \bullet p_2)) \parallel (cch\ L2_b \bullet \ldots))
\]

We are interested in the worst case behaviour of the cache, where it leaks private information, and are not concerned with the specifics of how that may happen. However details of the cache, such as its update policy, may also be captured with extra machinery. In that sense our model of the cache is an abstraction of the underlying microarchitecture implementation, which could be verified using data and action refinement techniques [19,32,3].

### 3.2 Semantics of IMP-ro-spec

**Partial pre-execution.** The semantics of a partial pre-execution process is based on that of the interrupt operator from CSP [20].

**Rule 22 (Partial pre-execution)**

\[
\begin{align*}
(c_1 \alpha \rightarrow c'_1) & \quad (a) \\
(c_1 \triangle c_2 \alpha \rightarrow c'_1 \triangle c_2) & \quad (b)
\end{align*}
\]

For commands of the form \(\text{spec}(c)\triangle d\) the speculation of \(c\) occurs for some period of time (Rule 22(a)) before discarding the computation and starting down the \(d\) branch (Rule 22(b)). The arbitrariness of when \(c_2\) starts captures the unknown time at which speculation may be found to be incorrect. We make use of the following law that covers the interruption occurring after a single action.

\[
(\alpha \cdot c_1) \triangle c_2 \sqsubseteq \alpha \cdot c_2 \quad (23)
\]

**Transient buffers.** Transient buffers catch stores and record them in a state; recorded values may be used for speculative computations.

**Rule 24 (Buffer)**

\[
\begin{align*}
(c \xrightarrow{x:=v} c') & \quad (a) \\
(\text{buf} \sigma \bullet c) \xrightarrow{\tau} (\text{buf} \sigma_{[x:=v]} \bullet c') & \quad (b) \\
(\text{buf} \sigma \bullet c) \xrightarrow{x \mapsto v} (\text{buf} \sigma \bullet c') & \quad (c) \\
(\text{buf} \sigma \bullet c) \xrightarrow{\text{CACHE} + x} c' \quad x \notin \text{dom}(\sigma) & \quad (d) \\
(\text{buf} \sigma \bullet c) \xrightarrow{\text{CACHE} + x} c' \quad x \notin \text{dom}(\sigma) & \quad (e)
\end{align*}
\]

Rule 24(a) states that (speculated) stores are recorded in the transient buffer;
Rule 24(b) states that (speculated) loads are serviced by the buffer (similar to forwarding [12]) if a value is available; Rule 24(c) states that otherwise the load is promoted (to be handled by the global state via Rule 10). In cases where nested speculation has resulted in a cache fetch, Rule 24(d), similarly to Rule 24(b), hides a fetch of $x$ if a store of $x$ is in the buffer already; Rule 24(e) states that otherwise the cache fetch is promoted. In addition a transient buffer command promotes other instruction types not covered above (e.g., $\tau$, specfence), and the rules do not need to cover registers since the transient buffer encloses a local state [17].

Speculation (down an incorrect path). Speculation should have no observable effect on registers or globals (the “CPU state”), however in reality it may leave a footprint in the cache. The main concept is to make explicit a cache fetch with each speculated load.

\[
\begin{align*}
\text{Rule 25 (Speculative context)} & \quad \frac{c \left[ x=v \right]}{\text{spec}(c)} \quad \text{CACHE} \leftarrow x \quad \frac{c' \quad (x \neq v \lor \text{spec}(c'))}{(a) & \quad \frac{c \rightarrow c'}{\text{spec}(c) \rightarrow \text{spec}(c')}} \\
& \quad \text{spec}(c) \quad \frac{\text{CACHE} \leftarrow x}{c'} \quad (b) & \quad \text{spec}(c) \quad \frac{\text{CACHE} \leftarrow x}{c'} \quad \text{spec}(c') \quad (c) \\
& \quad \text{spec}(c) \quad \frac{\text{CACHE} \leftarrow x}{\text{spec}(c')} \quad \text{spec}(c) \quad \frac{\text{CACHE} \leftarrow x}{\text{spec}(c')} \quad \text{spec}(c') \quad \text{spec}(c) \quad \frac{\text{CACHE} \leftarrow x}{\text{spec}(c')} \quad (d)
\end{align*}
\]

Rule 25(a) states that speculated loads of global variables have an initial side effect on the cache. The load is delayed until after the cache fetch. Rule 25(b) states that speculative execution can perform local computation. Rule 25(c) states that cache fetches are promoted (from nested speculation). Rule 25(d) states that speculation may silently complete. By omission, i.e., since there is no corresponding rule, speculation is blocked if $c$ executes a specfence command. We do not need to consider further action types, since speculation always encompasses a transient context out of which only loads and cache fetches are exposed.

Reordering of cache instructions. The semantics of IMP-ro is instantiated for a particular memory model by defining the relation $\equiv$, as used in Rule 1(b). We must therefore define the cases under which the new (cache-based) instruction types can be reordered. The concept of speculative execution is that loads can be initiated ahead of time, though they must still (appear to) conform to the particular memory model. However the cache fetches are not so constrained. We therefore allow cache fetch instructions to be reordered before the majority of instruction types.

\[
\begin{align*}
y & \leftarrow e \quad \text{CACHE} \leftarrow x \quad \text{iff} \quad x, y \quad \text{distinct} \quad (26) \\
\text{specfence} \neq r & \leftarrow x \quad \text{specfence} \neq \text{CACHE} \leftarrow x \quad (27)
\end{align*}
\]
Equation (26) states that a cache fetch of \( x \) may occur earlier than loads, and stores of other variables (note that \( x := 1 \iff \text{CACHE} \leftarrow x \) as the assignment will service the corresponding load, rather than memory). Equation (27) states that specfence instructions block loads and cache fetches. A potential mitigation for the Spectre vulnerability (short of turning off speculation entirely) is to insert (concrete) specfence instructions at the start of each potentially affected branch. However, this would have too great an impact on processor speed to be seriously considered as a blanket fix [30].

As an example of out-of-order execution with cache side effects consider a command of the following form, where \( l_i \) are loads and \( s_i \) are store instructions to distinct locations.

\[
l_1 ; l_2 ; (\text{if } b \text{ then } l_3 ; s_1 \text{ else } s_2 ; l_4)
\]

Speculation allows cache fetches to come earlier (out-of-order), although whether the loads themselves can come earlier than preceding loads depends on the architecture: ARM and POWER allow loads to be reordered, whereas TSO doesn’t [37]. Let \( c_3 \) be the cache fetch corresponding to load \( l_3 \). One possible behaviour, where the true branch is speculated before the false branch is executed, is given by the following sequence, which exposes the cache fetch for \( l_3 \).

\[
c_3 \cdot l_1 \cdot l_2 \cdot [\neg b] \cdot s_2 \cdot l_4
\]

The cache fetch for \( l_3 \) occurs before the earlier loads, which, for some execution- and architecture-specific reason, have taken longer to resolve. Note \( l_3 \) itself occurs in an order consistent with the memory model.

For simplicity we enforce ordering on cache operations, though the framework is flexible (for instance, on Intel architectures cache flush instructions do not necessarily prevent pre-fetching [21]).

\[
\alpha \not\iff \text{CCLEAR} \quad \text{CCLEAR} \iff \alpha \quad x \in \text{CACHE} \iff \alpha \quad \alpha \not\iff x \in \text{CACHE}
\]

We do not intend for these to be definitive, but rather develop a framework that is flexible enough to cope with different models.

3.3 Example of cache side effects due to speculation

In this section we show the particular behaviour of a conditional statement, where the true branch is (partly) speculated before the false branch begins. We construct the true branch, \( \text{branch}_T \), so that it modifies some global \( x \) and a register \( r_1 \), before loading \( z \) into register \( r_2 \) and proceeding as \( \text{branch}'_T \). A (partial) behaviour of \( \text{branch}_T \) is given by (28).

\[
\begin{align*}
\text{branch}_T &
\equiv x := 1 ; \ r_1 := 2 ; \ r_2 := z ; \ \text{branch}'_T \\
\text{branch}'_T &
\equiv x := 1 ; \ r_1 := 2 ; \ r_2 := z \rightarrow \text{branch}'_T
\end{align*}
\]

The trace ends with a load of \( z \). We will take the case where globally \( z \) has the value 42. Now consider speculating \( \text{branch}_T \).
\[\text{spec}(\text{branch}_T)\]
\[= \text{Set up new transient context (17)}\]
\[\text{spec}(\text{buf} \varnothing \bullet (\text{local } \sigma \bullet \text{branch}_T))\]
\[\tau^* \text{ From (28), locally update } x \text{ by Rule 24(a) and } r_1 \text{ by Rule 1} \]
\[\text{spec}(\text{buf} \{x \mapsto 1\} \bullet (\text{local } \sigma_{[r_1 := 2]} \bullet r_2 := z ; \text{branch}_T))\]
\[\text{CACHE} \leftarrow z \text{ Fetch (Rule 24(a)); arbitrarily assume } z \text{ is 42} \]
\[\begin{align*}
\{z = 42\} ; \text{spec}(\text{buf} \{x \mapsto 1\} \bullet (\text{local } \sigma_{[r_1 := 2]}\cdot r_2 := 42 \bullet \text{branch}_T))
\end{align*}\]

The cache fetch has been exposed in the trace (the corresponding load \(z = 42\) is pending). We abbreviate the remaining code as \(\text{branch}'_T\), and may derive (29) by the above calculation and Law 11.

\[\begin{align*}
\text{branch}'_T & \equiv \{z = 42\} ; \text{spec}(\text{buf} \{x \mapsto 1\} \bullet (\text{local } \sigma_{[r_1 := 2]}\cdot r_2 := 42 \bullet \text{branch}_T)) \\
\text{spec}(\text{branch}_T) & \subseteq \text{CACHE} \leftarrow z \bullet \text{branch}'_T
\end{align*}\]

Now we show how the cache fetch in the \(\text{true}\) branch may be seen in behaviours where the \(\text{false}\) branch is taken.

\[\begin{align*}
\text{if } b \text{ then } \text{branch}_T \text{ else } \text{branch}_F \\
\equiv & \text{ Definition 18} \\
\text{spec}(\text{branch}_T) & \triangleq \{b\} ; \text{branch}_T \triangleq \text{spec}(\text{branch}_T) \triangleq \{\neg b\} ; \text{branch}_F \\
\equiv & \text{ Arbitrarily choose } \text{false} \text{ branch by Law 12} \\
\text{spec}(\text{branch}_T) & \triangleq \{\neg b\} ; \text{branch}_F \\
\equiv & \text{ by (29)} \\
\text{CACHE} & \leftarrow z \bullet \text{branch}'_T \triangleq \{\neg b\} ; \text{branch}_F \\
\equiv & \text{ by Law 24} \\
\text{CACHE} & \leftarrow z \bullet \{\neg b\} ; \text{branch}_F
\end{align*}\]

From the system’s perspective the speculation has had no effect: the assignment to \(x\) was caught in the transient buffer, and then discarded, and the computations involving registers \(r_1\) and \(r_2\) became silent steps that did not affect the outer state. However, the cache has (potentially) been modified.

At the system level this gives the following behaviour, assuming global state \(\sigma_g\) satisfies \(\sigma_g(z) = 42\) and assuming \(\sigma_g(\text{CACHE}) = C\) (the value for \(x\) is irrelevant), and \(\sigma_l\) is the local state (mapping \(r_1\) and \(r_2\)).

\[\begin{align*}
\text{if } b \text{ then } \text{branch}_T \text{ else } \text{branch}_F \\
\equiv & \text{ By the above derivation (note that neither } \sigma_g \text{ nor } \sigma_l \text{ are affected)} \\
\text{spec}(\text{branch}_T) & \triangleq \{b\} ; \text{branch}_T \triangleq \text{spec}(\text{branch}_T) \triangleq \{\neg b\} ; \text{branch}_F \\
\equiv & \text{ Execute instruction (Rule 1(a)), 19, Rule 9} \\
\text{spec}(\text{buf} \{\text{CACHE} := C \cup \{z\}\} \bullet (\text{local } \sigma_l \bullet \{\neg b\} ; \text{branch}_F)) & \parallel \ldots
\end{align*}\]

The processes in ‘…’ could include a malicious attacker that may be able to exploit the existence of \(z\) in the cache. We give an example of this in the next section.

---

Note that \(\text{branch}_T\) does not depend on any of the values it buffers/loads, and hence we may choose an arbitrary local \(\sigma_l\); for other cases the choice of \(\sigma_l\) may be important.
The derivations above cover the situation where a single speculated load is promoted to a cache fetch. The variant of the Spectre attack we consider in the next section contains two speculated loads; using similar reasoning to the above we can straightforwardly show the following.

\[ \text{spec}(r_1 := x; r_2 := y) \]
\[ \subseteq \text{CACHE} \leftarrow x \cdot [x = v_1]; \text{spec}(r_2 := y) \]
\[ \subseteq \text{CACHE} \leftarrow x \cdot \text{CACHE} \leftarrow y \cdot [x = v_1]; [y = v_2]; \text{spec}(\text{nil}) \]

And hence by generalising Law 23 we may deduce the following.

\[ \text{spec}(r_1 := x; r_2 := y) \triangle c \subseteq \text{CACHE} \leftarrow x \cdot \text{CACHE} \leftarrow y \cdot c \quad (30) \]
\[ \text{if } b \text{ then } r_1 := x \quad ; \quad r_2 := y \quad \text{else } c \subseteq \text{CACHE} \leftarrow x \cdot \text{CACHE} \leftarrow y \cdot [\neg b] \quad ; \quad c \quad (31) \]

4 Security vulnerabilities

4.1 Attack patterns

Cache-based timing attacks often utilise certain attack strategies to set up the cache as a covert or side channel to expose secret information. Generally, an attacker that shares a cache with a victim can observe through the variation in access time whether a particular memory address resides in the cache (a cache hit) and hence has been accessed previously, or not (a cache miss). To reduce noise on this covert channel, the attacker first “clears” the cache to make sure the memory address in question does not reside in the cache. This can be achieved by either flushing the cache line in question (some Intel architectures offer an instruction \texttt{clflush}), or by filling the cache with other content (by accessing physically congruent addresses in a large array [17]), so that due to the contention the memory addresses in question (if present) will be evicted. Both these options are captured in our model through the instruction \texttt{cclear} (as emptying the cache and filling the cache with other content amounts to the same desired effect).

For example consider the following code that iterates over the elements of an array \( B \) to determine which of \( B[i] \) is in the cache.

\[ \text{Atk} \equiv i := 0; \quad \text{while } i < 256 \text{ do (if } B[i] \in \text{CACHE then } r := i); \quad i += 1 \] \quad (32)

If the attacker is trying to determine the value of some byte of data \( D \), then under the assumption \( B[D] \in \text{CACHE} \) and for all \( i \neq D \) we have \( B[i] \notin \text{CACHE} \) then we have \( r = D \).

The guard \( B[i] \in \text{CACHE} \) is an abstraction of a timing attack that loads \( B[i] \) and checks the amount of time against an architecture-specific threshold. For our level of analysis we do not need to explicitly model such detail, we care only that it is possible.

\texttt{Flush+Reload [46]} and also \texttt{Evict+Reload [17]}, two examples that follow the above pattern, can be used to target the last level cache (LLC), which is
shared between cores, and hence works on any cross-core as well as cross-VM settings \[27\]. In cases where a flush instruction is not available evicting is used to “clear” the cache. The following fundamental concepts of micro-architectures are exploited in these attack patterns \[17\]: 1) the LLC is shared amongst all CPUs; 2) the LLC is inclusive (i.e., contains all data that is stored in the L1 and L2 caches, hence modifications on the LLC influence caches on all other cores); 3) single cache lines are shared amongst processes on the same core; and 4) programs can map any other program binary/library into their address space.

4.2 The Spectre attack

Spectre attacks typically use an attack pattern based on those described above. Additionally to setting up the cache as a channel, the attacker (mis)trains the branch predictor to speculate down the desired branch. Depending on the processor-specific branch prediction mechanism used, the training can occur by repeatedly running the code with “correct” input. When unexpectedly supplied with an “incorrect” input, the processor will (incorrectly) speculate the desired branch, in which secret information is loaded from memory (e.g., execute a memory access at an address that is chosen by the attacker), or in other variants the attacker may leverage its own code to access the secret from the same process, for instance, a webpage script run from within a browser process. In a third phase of the attack the timing difference between a cache hit and a cache miss is observed by the attacker, as in \(32\), allowing it to deduce the secret value.

An example of victim’s code that is susceptible to a Spectre attack is given below (following \[24\]). Assume that the attacker wishes to know the value of some data \(d\), held at some address in the private space of the victim process \(V\) and which can be retrieved via variable \(k\), i.e., \(d\) is at address \&\(k\). The attacker knows/calculates the address of \(k\) relative to the victim array \(A\), which we will call \(\chi\), loading the value into \(r_2\) via an out-of-bounds index into \(A\). That is, \(A[\chi] = d\). This private data is then used as an index into another array \(B\).

\[
V \equiv r_1 := \chi; \quad n := \#A; \quad \text{if } r_1 < n \text{ then } (r_2 := A[r_1]; r_3 := B[r_2])
\]

We apply Law \(31\) to observe the potential effects of speculation.

\[
V \subseteq r_1 := \chi; \quad n := \#A; \quad \text{CACHE} \leftarrow A[\chi]; \quad \text{CACHE} \leftarrow B[d]; \quad [r_1 \not< n]
\]

(We let \&\(A[i]\) return a unique address for the array \(A\) at index \(i\).) Let \(\sigma_l\) be the local state for \(V\) \((A, n, r_1, r_2, r_3 \in \text{dom}(\sigma_l))\), and \(\sigma_g\) the global state \((B \in \text{dom}(\sigma_g), \sigma_g(\text{CACHE}) = C)\); then we can derive the following refinement.

\[
(\text{global } \sigma_g \cdot (\text{local } \sigma_l \cdot V) \parallel p) \sqsubseteq (\text{global } \sigma_g[\text{CACHE} := C \cup \{\&k, \&B[d]\}] \cdot (\text{local } \sigma_l' \cdot \text{nil}) \parallel p)
\]

The data \(d\) does not appear explicitly in the shared state, but indirectly through a cache fetch. Note that the values of the variables whose addresses are in the cache are not accessible.
To infer $d$ the attacker may perform an attack as given by $Atk$ in (32). For simplicity here we assume $Atk$ and $V$ share $B$, for instance if $B$ is a read-only array of data shared by processes in a system; alternatively $Atk$ does not need to share $B$, but rather know where $B$ maps to in a shared cache, and map an array $B_{Atk}$ of its own so that the addresses in the cache line up. At this level of abstraction we do not distinguish these alternatives. To establish the precondition that all elements of $B$ are not in the cache the attacker sets up the context to ensure that it executes a `cclear` before the victim’s code is run. For instance, if the vulnerable code is in a function call provided by the server $V$, with the initial value of $r_1$ passed as an argument,

$$(\text{global } \{ \text{CACHE} \mapsto \ldots \}) \bullet \text{cclear} ; \ V(\chi) ; \ Atk)$$

This pattern can be repeated; in fact $\chi$ need not be a specific address, as data from $V$’s private space can be read consecutively byte-by-byte by incrementing $\chi$ on each attack.

**Model checking.** We validated the semantics by encoding the refinement laws as an extension to the simulation tool described in [12], which is written in the Maude rewriting engine [8,42]. The refinement laws and auxiliary definitions (such as $r \Leftarrow$ for cache fetches) were encoded straightforwardly. We then encoded the Spectre attacker and victim processes, extending the array $A$ so that its contents went beyond its stated length to model an out-of-bounds index into private memory; the simulation runs showed that $r = d$ is established in the attacker in the cases where speculation is not interrupted in the victim until after the two cache fetches.

5 Related work

Cache side channels have been studied in the past decade (see [47,16] for an overview), and a number of tools have been developed to support the detection of vulnerabilities (e.g., [14,44,6,39]). However, these developments predate the publication of the Spectre vulnerability [25,24] and hence do not consider the effects of speculative execution. Since the effects of speculation do not affect the functional correctness of an implementation (the results of incorrect speculation are thrown away), they could be safely ignored in earlier work on the semantics of weak memory models (e.g., [12]). Detailed formal models of microarchitecture describe the interaction of the cache with processors [4], but are not readily integrated with language-level analysis techniques.

A model of speculative execution to study vulnerabilities and support the evaluation of software mitigations is presented in [30]. That work assumes a uniprocessor system and is not integrated with a weak memory model, and is designed to give a precise description of the behaviour of the microarchitecture. The work of [13] gives a model of execution that highlights speculative behaviours by explicitly modelling executions down false branches within a partially-ordered
multiset graph-based model. In contrast to our framework, they don’t consider nested speculation, nor reorder speculated instructions.

A number of tools have been developed for detecting Spectre-vulnerable code and injecting fences to mitigate the danger\cite{43,26,45} as well as information flow approaches to ensuring security in the presence of speculative execution\cite{18,7}. The operational semantics underlying these approaches is less abstract than that presented in this paper, and the analysis is performed at the semantic level. The key difference of our work is that we encode speculative execution at the command level, and hence our framework supports algebraic, or refinement-based reasoning.

The CheckMate tool\cite{40} integrates a model of speculative execution into a weak memory model framework\cite{29}. Since the work aims at the verification of microarchitectures, their model is set at that level and does not provide high-level properties such as Law\cite{31} to support reasoning on the program level. Their tool is used to synthesise Spectre-style attacks and generate assembler test programs that can be used to determine if a particular processor is susceptible. We can potentially use these test programs to investigate the security implications within our more abstract framework. We have focused on cache effects from speculative loads, however two variants of Meltdown and Spectre discovered by the CheckMate tool\cite{40,41} work from speculative stores. On architectures where speculatively executed stores affect the cache we can adapt our semantics such that Rule\cite{24}\(\alpha\) emits the appropriate cache-modifying action (rather than being a purely internal step).

6 Conclusion

We have captured the side effects of speculative execution down the wrong path with a relatively small extension to an existing framework for reasoning about weak memory models (out-of-order execution). To calculate speculated computations (beyond loads) we introduced a transient context, which is discarded in the case of incorrect speculation. In our semantic framework, in contrast to Plotkin-style semantics where states appear in the configuration of the operational rules\cite{35}, we expose the effect of a transition in its label. This simplifies semantic issues concerning redeclaration of variables (see\cite{9,10} for a further discussion); operations on variables in the inner (transient) scope become silent τ steps that do not effect the variables in the outer scope, despite sharing the same names. Allowing early execution of speculated instructions was straightforward to specify in the reordering relation of IMP-\(\text{ro}\)\cite{12}.

Our intention is to allow abstract functional analysis techniques to be used alongside security analysis techniques, reusing existing tools. In particular, the information flow analysis framework in\cite{34,33} has been extended to weak memory models\cite{38} based on the reordering semantics of IMP-\(\text{ro}\)\cite{12}. We envisage a further extension of that work based on IMP-\(\text{ro-spec}\) to find information leaks resulting from speculative execution. (information flow approaches to speculative execution are also considered in\cite{18,7}). We have aimed to provide just enough
detail so that cache effects can be modelled, but not so much that the ability to derive generic algebraic laws (such as Law 31) is lost.

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A Speculation down the correct branch; parallel speculation

As far as is currently known correct speculation has no security implications, and therefore we do not model such behaviours explicitly. However if needed we can capture this in several ways. For instance, a cache fetch can be associated with every load, whether inside or outside a speculation, similarly to Rule 25(a). Such semantics can be given by annotating each load that may exhibit this side effect.

\[
(r := x)_{\text{CACHE}} \xrightarrow{\text{CACHE}+} r := x
\]

Alternatively we could add the possibility of speculation down the eventually chosen branch as a choice.

\[
\text{spec}(c_2 \cap c_1) \triangle ([b] ; c_1) \sqcap \text{spec}(c_1 \cap c_2) \triangle ([\neg b] ; c_2)
\]

A more precise model that commits the transient context when correct speculation is found is possible, though significantly more complicated.

The concept of speculation down either branch can be extended straightforwardly to parallel speculation down multiple branches, for instance,

\[
(\text{spec}(c_1) \parallel \text{spec}(c_2)) \triangle ([b] ; c_1)
\]