HALCONE : A Hardware-Level Timestamp-based Cache Coherence Scheme for Multi-GPU systems

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ABSTRACT

While multi-GPU (MGPU) systems are extremely popular for compute-intensive workloads, several inefficiencies in the memory hierarchy and data movement result in a waste of GPU resources and difficulties in programming MGPU systems. First, due to the lack of hardware-level coherence, the MGPU programming model requires the programmer to replicate and repeatedly transfer data between the GPU's main memory. This leads to inefficient use of precious GPU memory. Second, to maintain coherency across an MGPU system, transferring data using low-bandwidth and high-latency off-chip links leads to degradation in system performance. Third, since the programmer needs to manually maintain data coherence, the programming of an MGPU system to maximize its throughput is extremely challenging. To address the above issues, we propose a novel lightweight timestamp-based coherence protocol, HALCONE, for MGPU systems and modify the memory hierarchy of the GPUs to support physically shared memory. HALCONE replaces the Compute Unit (CU) level logical time counters with cache level logical time counters to reduce coherence traffic. Furthermore, HALCONE introduces a novel timestamp storage unit (TSU) with no additional performance overhead in the main memory to perform coherence actions. Our proposed HALCONE protocol maintains the data coherence in the memory hierarchy of the MGPU with minimal performance overhead (less than 1%). Using a set of standard MGPU benchmarks, we observe that a 4-GPU MGPU system with shared memory and HALCONE performs, on average, 4.6× and 3× better than a 4-GPU MGPU system with existing RDMA and with the recently proposed HMG coherence protocol, respectively. We demonstrate the scalability of HALCONE using different GPU counts (2, 4, 8, and 16) and different CU counts (32, 48, and 64 CUs per GPU) for 11 standard benchmarks. Broadly, HALCONE scales well with both GPU count and CU count. Furthermore, we stress test our HALCONE protocol using a custom synthetic benchmark suite to evaluate its impact on the overall performance. When running our synthetic benchmark suite, the HALCONE protocol slows down the execution time by only 16.8% in the worst case.

1. INTRODUCTION

Multi-GPU (MGPU) systems have become an integral part of cloud services such as Amazon Web Services (AWS) [7], Microsoft Azure [8], and Google Cloud [1]. In particular, many deep learning frameworks running on these cloud services provide support for MGPU execution to significantly accelerate the long and compute-intensive process of training deep neural networks. For instance, Goyal et al. [12] trained ResNet-50 in only 1 hour using 256 GPUs, which would have otherwise taken more than a week using a single GPU. MGPU systems are also commonly used for parallelizing irregular graph applications [5, 28, 36, 37] and facilitating large-scale simulations in different domains including physics [41], computational algebra [38], surface metrology [40] and medicine [13].

GPU applications are evolving to support ever-larger datasets and demand data communications not only within a GPU but also across multiple GPUs in the system. As a result, the underlying programming model is evolving, and major vendors such as NVIDIA and AMD have introduced software abstractions such as shared and global memory spaces that enable sharing of data among different threads within a GPU. Furthermore, GPU-to-GPU Remote Direct Memory Access (RDMA) [22] was introduced so that a GPU can transfer data directly to/from another GPU, without involving the CPU, through off-chip links such as NVLink or PCIe as shown in Figure 1. However, despite continuous advances in inter-GPU networking technologies, the off-chip link bandwidth is roughly 3-10× lower than local main memory (MM) bandwidth. Thus, data accesses to/from remote GPU memories, which are essential for MGPU applications, can lead to severe performance degradation due to the NUMA effect [19, 20].

To highlight the large impact on performance when relying on state-of-the-art RDMA technology for GPU-to-GPU communication, we perform an experiment with a SGEMM kernel from the cuBLAS library [23] that is executed on an
NVIDIA DGX-1 [14] MGPU system. More specifically, we aim to compare the impact of RDMA on kernel execution time considering two Volta GPUs (i.e., GPU0 and GPU1), which are connected by NVLinks that support 50 GB/s per direction. We first place the matrices in GPU0’s memory and execute $\text{SGEMM}$. Then, we enable $P2P$ direct access to leverage RDMA and run the same $\text{SGEMM}$ kernel on GPU1 while the matrices reside in GPU0’s memory (we refer to this as remote). Figure 2 shows the results of the experiment with different matrix sizes. The kernel using local memory is $12.4 \times$ (for a matrix size of $32768 \times 32768$) to $2895 \times$ (for a matrix size of $512 \times 512$) faster than the kernel using remote memory. These results clearly show that RDMA is expensive, and motivate the pressing need for an alternate path to reduce the significant cost of remote accesses in MGPU systems.

Programming a GPU system also has several challenges. In particular, a program written to run on a single GPU cannot be easily ported to run on multiple GPUs. The programmer must be aware of any data sharing, both within a single GPU and across multiple GPUs. As there is no hardware support for cache coherency in current MGPU systems, the programmer must explicitly maintain coherency while developing a GPU program. This requires manually transferring duplicated data when needed to different GPUS’ memory, using explicit barriers if previously read data is modified, or in the worst case, using atomic operations. All of these approaches require significant effort by the programmer. Moreover, contemporary GPUs only support weak data-race-free (DRF) memory consistency [15, 30], so the programmer has to ensure there are no data races during program execution.

To leverage the true capability of MGPU systems and ease MGPU programming, we need efficient hardware-level inter-GPU coherency. Extending well-known directory-based or snooping-based CPU coherence protocols such as MESI, MOESI, etc. is not suitable for an MGPU system [42]. This is because the MGPU system with its thousands of parallel threads per GPU produces a much larger number of simultaneous memory requests than CPUs, which translates into a prohibitively high degree of coherency traffic in these traditional protocols [31]. A promising solution to alleviate coherency traffic is to use self-invalidation by relying on temporal coherence [31]. Previous timestamp based solutions targeting a single GPU used global time (the TC protocol) [31] or logical time (the G-TSC protocol) [35] to maintain coherency across the L1Ss and L2Ss of a GPU. However, none of the previous timestamp based work has addressed coherency issues in an MGPU system.

To provide support for efficient intra-GPU and inter-GPU coherency, in this paper we propose HALCONE - a new timestamp-based hardware-level cache coherency scheme for tightly-coupled MGPU systems with physically shared main memory (named MGPU-SM for short).HALCONE

1An MGPU system can be designed by cabling together a collection of MGPU nodes, and leveraging a message passing layer, such as MPI [18] to work collectively on a single application. An alternate approach is to consider an MGPU system that is more tightly-coupled and uses shared memory (i.e., MGPU-SM) [21]. The former involves more programmer effort to support MGPU execution, while the latter relies on the hardware and runtime system to support a version of shared memory. In this paper, we focus on improving the performance and scalability of an MGPU-SM system.

2Request traffic is reduced by up to 41.7% and the response traffic is reduced by up to 3.1% in the memory hierarchy.
show that HALCONE can result in up to 16.8% performance degradation for extreme cases, but it lowers programmer burden. We also show that an MGPU system with HALCONE scales well with GPU count and CU count per GPU.

2. BACKGROUND

2.1 Communication and Data Sharing

To share data across GPUs in MGPU systems, a variety of communication mechanisms are available. A GPU can use P2P memcpy to copy data to and from the memory of a remote GPU. This P2P memcpy approach essentially replicates the data in different memory modules [42]. To avoid this data replication, P2P direct access (called RDMA in this paper) can be used where a GPU can access data from a remote GPU memory without copying it to its MM. However, P2P direct access leads to high latency remote data accesses, which causes performance degradation [39].

Current NVIDIA GPUs provide a page fault mechanism in a virtually unified address space called unified memory (UM)3. Under UM, the data is initially allocated on the CPU. When a GPU tries to access this data, it triggers a page fault and the GPU driver serves the page fault by fetching the required page from another device. However, this page fault mechanism is known to introduce serialization in accessing pages and can hurt GPU performance [4, 16].

2.2 Timestamp Based Coherency

In this section, we briefly explain the operation of G-TSC protocol [35], which was designed for intra-GPU coherence that share the MM. HALCONE builds on top of the G-TSC protocol and also our proposed HALCONE protocol.

Read Operation: A read request from a CU contains the warpedt and the address. Each block in the L1S 4 has a read timestamp (rts) and write timestamp (wts). If the block is present and the warpedt falls within the range between wts and rts (i.e. the lease), it is a cache hit. Otherwise, the read request is treated as an L1S miss and is forwarded to the L2S. This read request to L2S contains the address, the wts of the block and the warpedt. If the wts value for the request is set to 0, it means a compulsory miss occurred at L1S, and L2S must respond with the data and the timestamps. A non-zero value for wts implies the block exists in L1S, but the timestamp expired.

Upon receiving a read request, the L2S checks if the block exists in the L2S. If it does not exist, L2S sends a read request to the MM. If the warpedt of the request from L1S is within the lease for that block in the L2S, the L2S also compares the wts from the L1S request and the wts of the block in the L2S. If both wts values are the same, it means that the data was not modified by another CU and simply that the lease expired in the L1S. In that case, the L2S extends the lease by increasing the rts and sends the new rts and wts values to the L1S. If the wts values do not match, it implies that the data was modified by a different CU. Hence, L2S sends both data and new timestamps to the L1S.

Write Operation: Write requests are handled using a write-thru policy from L1S to L2S, and L1S adopts a no-write-allocate policy. To result in a write hit in a cache, the warpedt needs to be within the lease of the requested cache block. Otherwise, it is considered a write miss. When there is a write hit in the L1S, the data is written in the L1S, but the access to the data is locked until L2S is updated and L2S sends the updated timestamps for the data. It is necessary to lock access to the block to ensure that the warpedt is updated correctly using the wts value for the L1S receive from the L2S. Any discrepancy in updating warpedt may result in an incorrect ordering of memory access requests. If there is an L1S write miss, the data is directly sent to the L2S to complete the write operation. For an L2S write miss, the L2S sends a write request to the MM. If we get a write hit at L2S, the L2S writes the data to the block in the L2S and updates the timestamps for that block. L2S then sends the updated rts and wts values to the L1S.

On both read and write operations, the responses from L1S to CU contain the wts value from the most recent memory operation. Based on this wts value, CU updates its warpedt.

3. HALCONE IN MGPU-SM SYSTEMS

We present the working fundamentals of our proposed HALCONE using an example MGPU system with 4 GPUs that share the MM. HALCONE builds on top of the G-TSC protocol [35], which was designed for intra-GPU coherence but cannot be readily applicable to MGPU systems. Maintaining coherency across multiple GPUs is more challenging as the L1Ss of a GPU can only interact with their own L2S. We need to maintain coherence across multiple L2S across different GPUs. A straightforward extension of G-TSC would be to add timestamps to each block in the MM leading to significant area overhead as we would need space to store the timestamps of each block of data in the MM. G-TSC also needs to maintain a logical time counter at the compute unit level, which needs to send timestamps i.e. warpedt back and forth between CUs and L1Ss leading to additional traffic overhead. As we show later in the paper (Section 3.2), to

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3UM provides the abstraction of a virtually unified memory combining the CPU’s and GPUs’ physical memories.

4Throughout this paper, we use L1S to refer to L1S vector cache unless specified otherwise.

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| Table 1: Terminologies and definitions | Term | Definition |
|----------------------------------------|------|------------|
|                                        | physical time | The wall clock time of an operation. |
|                                        | logical time  | The logical counter maintained by a component (e.g., CU and cache). |
|                                        | warpts | The current logical time of a CU. In the G-TSC protocol, the memory operations are ordered based on the warpedts. |
|                                        | cts | The current logical times of a cache. Each cache has a cts that is updated based on the last memory operation. |
|                                        | memts | The memory time stamp that represents the logical read access. When a GPU tries to access this data, it triggers a page fault. |
|                                        | lease | An entry containing address, data, and associated timestamps in the caches. |
|                                        | wts | The write timestamp of a cache block. It represents the logical time when a write operation is visible to the processors. |
|                                        | rts | The read timestamp of a cache block. It represents the logical time until which reading the cache block is valid. |
|                                        | RdLease | Lease assigned to a block after a read operation is executed. |
|                                        | WtLease | Lease assigned to a block after a write operation is executed. |
|                                        | memts | The memory time stamp that represents the logical read timestamp that the memory assigns to a cache block. |

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maintain coherence in MGPU systems we do not need to maintain a logical time counter in the CU level, but instead, each L1$ and L2$ can maintain the individual counters. This helps reduce request traffic. In addition, while G-TSC simply provides the same lease for both reads and writes, we provide different lease values for reads and writes. By doing so, as we will see in Section 5.4, this benefits the exploitation of temporal locality. To elaborate, each write operation moves the logical time counter ahead by the write lease value. If we use the same lease for read as for write, each write operation will lead to self-invalidation of the previously read block.

3.1 An MGPU System with Shared Memory

Figure 3 shows the logical organization of our target MGPU-SM system. In this configuration, each CU has a private L1$ and each GPU has 8 distributed shared L2 banks. Each L2 bank has a corresponding cache controller (CC). We use High Bandwidth Memory (HBM) as the MM because HBM is power and area efficient, capable of providing high bandwidth required for GPUs [24]. A network provides connectivity between the CC in the L2$ and the MM controller (MMC) in the HBM. More details about the network are provided in Section 4. We assume a 4 GB memory per HBM stack in this example. Each L2 CC handles 2 GB (the size depends on the number of CCs and the HBM size) of the entire address space in the HBM. Thus, all the GPUs are connected to all the HBM stacks, making the memory space physically shared across all GPUs. We use a TSU in each HBM to keep track of the timestamps for the blocks being accessed by the different L2$s. We provide the detailed operation of the TSU later in this section.

3.2 HALCONE Protocol

We define the HALCONE protocol using a single-writer-multiple-reader (SWMR) invariant. Our HALCONE protocol is based on the G-TSC [35] protocol designed for a single GPU. The terms used to explain the HALCONE protocol are defined in Table 1. Unlike the G-TSC protocol, we do not have a warpTSUs but assign a timestamp cts to each of the L1$s and L2$s. Each CU has a private L1$, hence the cts for an L1$ is equivalent to the warpTSUs in the G-TSC protocol. Managing timestamps at the caches allows us to reduce timestamp traffic between the L1$ and CU, as well as between the L1$ and L2$ by eliminating the need for sending cts with requests and responses to maintain coherence as compared to G-TSC protocol which sends warpTSUs with every request. The memory operations are ordered based on the logical time, in particular, cts. If two requests have the same cts value, the cache uses physical time to order them. The key idea is that the block is only valid in the cache if the cts is within the valid lease period. Figure 4 shows the transactions between CUs, L1$s, L2$s, and MM for read and write operations. We explain these transactions with the help of Algorithms 1–5.

3.2.1 Read Operations

L1$: Figure 4(a) shows the transactions between a CU and the L1$ for read operations. As shown in Algorithm 1, a cache hit at L1$ occurs only when there is an address (tag) match and the current timestamp, cts, is within the lease period of the cache block. If there is a tag hit, but the cts is not within the lease period, we fetch the cache block from L2$ with new rts and wts values. For an L1$ miss, we fetch the cache block with its rts and wts values from L2$.

L2$: Algorithm 2 shows how read requests are handled by the L2$. The L2$ hit or miss is similar to that of L1$. Figure 4(b) shows the transactions between the L1$ and the L2$ for read requests. If there is a cache hit and the lease is valid, the L2$ sends the cache block, rts, and wts to the L1$. If there is a cache miss in the L2$, then the L2$ sends a request to the MM. After fetching the cache block from MM, the L2$ responds to the L1$ with the cache block, rts, and wts. If there is a tag match, but cts is not within the lease period in L2$, we re-fetch the data with new timestamps from the MM. This re-fetching of data ensures coherency in case another GPU modified the data in the MM. Note that G-TSC protocol only fetches renewed timestamps from L2$ if data has not been modified by another CU. However, such re-fetching requires to send the warpTSUs with each request (which we eliminated to reduce traffic) and adds more complexity as HALCONE has a deeper memory hierarchy.

MM: Figure 4(c) shows the transactions to and from the
Algorithm 1: Read Request to L1

Initialization: cts = 0;
Fetch RdReqFromCU{Addr};
if Block(Addr) == nil or cts > rts(Block) then
  Send RdReqToL2{Addr};
else
  Fetch RspFromL2{Data, rts, wts};
  Bwts = max[cts, wts];
  Brts = max[wts + 1, rts];
  cts = max[cts, Bwts];
  UnlockAccessToBlock;
  Send RspToL1{Block{Data}};
end if

Algorithm 2: Read Request to L2

Initialization: cts = 0;
Fetch RdReqFromL1{Addr};
if Block(Addr) == nil or cts > rts(Block) then
  Send RdReqToMM{Addr};
else
  Fetch RspFromMM{Data, Mrts, Mwts};
  Bwts = max[cts, Mwts];
  Brts = max[wts + 1, Mrts];
  Send RspToL1{Block{Data, Brts, Bwts}};
end if

Algorithm 3: Read or Write Request to MM

Initialization: Mmts = 0;
Fetch RdReqFromL1{Addr};
if TSU(Addr) == nil then
  AddEntryToTSU{BlockAddr};
else if Req==ReadReq then
  MemtsEntry = mmts + RdLease;
  Mrts = MemtsEntry;
  Mwts = Mrts - RdLease;
else if Req==WriteReq then
  MemtsEntry = mmts + WrLease;
  Mwts = Mrts - WrLease;
  Send RspToL2{Block{Data, rts, wts}};
end if

Algorithm 4: Write Request to L1

Initialization: cts = 0;
Fetch WrReqFromCU{Addr};
if cts <= rts(Block) then
  WriteToBlock;
  LockAccessToBlock;
  Send WrReqToL2{Addr};
else
  Send WrReqToL2{Addr};
  Fetch RspFromL2{Block, rts, wts};
  Bwts = max[cts, wts];
  Brts = max[wts + 1, rts];
  cts = max[cts, Brts];
  UnlockAccessToBlock;
  Send RspToL1{Block{Data}};
end if

Algorithm 5: Write Request to L2

Initialization: cts = 0;
Fetch WrReqFromL1{Addr};
if cts <= rts(Block) then
  WriteToBlock;
  LockAccessToBlock;
  Send WrReqToMM{Addr};
else
  Send WrReqToMM{Addr};
  Fetch RspFromMM{Block, rts, wts};
  Bwts = max[cts, wts];
  Brts = max[wts + 1, rts];
  cts = max[cts, Brts];
  UnlockAccessToBlock;
  Send RspToL1{Block{Data, Brts, Bwts}};
end if

MM for read requests from the L2$. Algorithm 3 explains how a read request from the L2$ is handled by the MMC. The MM tracks the timestamp of each block accessed by the L2$ of all the GPUs using the TSU. The TSU stores the read address and the timestamp (memts) of the block, but not data itself. memts is used to keep track of the lease of a block sent to the L2$. If there is no entry for the requested address in the TSU (i.e., the block has never been requested by the L2$), it adds the address and then updates the memts of the block using the Mrts allocated for the read operation. If there is already an entry in the TSU for the requested address, the TSU extends the memts of the entry using the Mrts for the read operation.

3.2.2 Write Operations

L1$: Figure 4(d) shows the transactions that take place for write requests to the L1$. We adopt a write-through (WT) cache policy for both the L1$s and L2$s. Algorithm 4 illustrates how write requests to L1$s are handled. Due to the WT policy, a write request to L1$ triggers a write request from L1$ to L2$, irrespective of a cache hit or miss. If the cts is within the 1ease, it is a write hit. In case of a write hit, the data is written immediately to the cache block in the L1$ and a write request is sent to the L2$. Access to the block is locked until the L1$ receives a write response, along with the new timestamps, from the L2$. The access is locked by adding an entry to the miss-status-holding-register (MSHR). In the case of a write miss in the L1$, the L1$ sends the request to the L2$. Once the L2$ returns both the block and its timestamps to the L1$, the L1$ writes data to the appropriate location and updates its cts.

L2$: Figure 4(e) shows the transactions that take place for write requests to the L2$. Algorithm 5 demonstrates how a write request to the L2$ is serviced. As we are using a WT policy for the L2$, a write request to the L2$ triggers a write request from the L2$ to the MM, irrespective of whether the access is a cache hit or miss. Again, the cache hit and miss conditions are the same as in the case of the L1$. If the access is a cache hit, the data is written to the block in the L2$ and a write request is sent to the MM. The L2$ updates the timestamp of the cache block using the response that it receives from the MM. The access to the block is locked until the write response and the timestamps are received from the MM. If the L2$ access results in a cache miss, L2$ sends a write request to the MM. The write request includes the data and address. The MM sends a response with the block and updated timestamps. Next, the L2$ issues a write to the block and updates its timestamps using the response from the MM.

MM: Figure 4(f) shows the transactions to and from the MM for a write request from the L2$. Algorithm 3 explains how a write request from the L2$ is serviced by the MMC. If there is no matching entry for the requested address in the TSU, then the TSU adds the address and updates the timestamp of the block using the 1ease for the write operation. If there is an entry present in the TSU for the requested address, the MM increases the memts of the entry using the 1ease for a write operation.

3.2.3 Intra-GPU Coherency

We use instructions identical to those described by Tabakb et al. [35] to explain both intra-GPU and inter-GPU coherency. Here, we first present how intra-GPU coherency is maintained using our HALCONE protocol. Figure 5(a) shows the instructions and the sequence of steps for maintaining intra-GPU coherency. In this example, we have two compute units, CU0 and CU1. Both CU0 and CU1 belong to GPU0. Each CU has a private L1$, but the L2$ is shared between the two CUs. In Figure 5(a), we show two L2$s for the sake of explanation, but both L2$s are the same L2$. CU0 executes 3 instructions, I0-1, I0-2, and I0-3, which read location [X], write to location [Y], and read location [X], respectively. Similarly, CU1 executes 3 instructions, I1-1, I1-2, and I1-3, which are: read location [Y], write location [X], and read location [Y], respectively. Both L1$s and L2$s have initial cts values of 0. 1 to 44 correspond to different memory events that occur during the execution of the three
the write request in L2$. As the request misses in L2$ as well, the L2$ sends a read request to the MM at 5. At 6, the MM sends the response to the L2$ with rts and a wts values of 10 and 0, respectively (we choose these values of the timestamps for this example). Our protocol works correctly for any values of rts and wts. Based on the cache block and the timestamps received from MM, at 7 L2$ updates its cts, the block’s rts and wts, and responds to L1$ with the updated rts and wts values, along with the cache block. Similarly, the L1$ updates its cts, and rts and wts values for the cache block at 8. The CU finally receives the data from L1$ at 9.

Instruction I1-1 from CU1 issues a read from location [Y] and follows the same steps as I0-1. The CU1 receives the data through steps 10 to 13. We assume a different lease (wts = 0, rts = 7) for location [Y] for this example.

CU0 requests to write to location [Y] at 15. The write request from a CU is served by the MM, regardless of whether it is a cache hit at L1$ or L2$. At 16, the L1$ of CU0 sends a write request to L2$. This results in a cache hit at L2$ as the location [Y] was previously read by CU1 and cts ≤ rts. At 17, the L2$ sends a write request to the MM for location [Y]. The MM updates the value and timestamps for location [Y]. We assume a lease of 5 for write operations in this example. At 18, the MM sends the response with rts = 12 and wts = 8 for the block containing [Y] to the L2$. Then the L2$ updates the timestamps for [Y] and sets cts(= 8) at 19 and sends the updated timestamps to the L1$ of CU0. At 20, the L1$ updates the timestamps for the block containing [Y] and the associated cts(= 8). Note that we do not show the actions to lock and unlock a block in the diagram for clarity. Every write request to a block in the cache must lock access to the block until receiving a response from the MM. At step 21, there is a write request (I1-2) from the CU1 at location [X]. This follows the same steps followed by I0-2. The response to the write request is executed in steps 22 to 26. Now, both L1$ and L2$ of CU1 have a cts value of 11 after completing the write request to location [Y]. At 27, there is a read request for location [X] from CUO. At 28, the cts value is 8 and the block for location [X] has a rts value of 10. Hence, it is a cache hit in L1$. Note that the advantage of using a logical timestamp is that it allows the scheduling of a memory operation in the future by assigning a larger rts value. Hence, the previous write on [X] by CU1 will be visible later to L1$ of CU0 as it has a cts value lower than the assigned wts value to the block for the write request by CU1 at 24. Since the cts of the L1$ of CU0 is smaller than the cts value of the L1$ of CU1 at this point, the read by CU0 of the L1$ happens before the write by the L1$ of CU1. The data is sent to CU0 by L1$ at 29. At 30, CU1 sends a request to read location [Y]. This request creates a coherency miss in L1$. This is because the cts is 11, but the block for location [Y] has a rts of 7. At 31, L1$ sends a read request to L2$. This request results in a cache hit at L2$, since L2$ has a cts value of 11 and the block for [Y] has rts = 12 and wts = 8. The execution order of the instructions in this example is I0-1 → I1-1 → I0-2 → I0-3 → I1-2 → I1-3.

### 3.2.4 Inter-GPU Coherency

In this example, we use the same instructions as in the previous example for intra-GPU coherency. CU0 of GPU0 executes instructions I0-1, I0-2, and I0-3. However, instructions I1-1, I1-2, and I1-3 are executed by the CU0 of GPU1 in this example. Thus, we have two different L2$s, one connected to GPU0 and one connected to GPU1. Figure 5(b) shows the instructions and the sequence of execution for explaining inter-GPU coherency. The read request from CU0 of GPU0 to read location [X] and read request from CU0 of GPU1 to read location [Y] follow the exact same steps (steps 1 - 14) as in the case of intra-GPU coherency. The write

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**Figure 5:** The timeline for (a) the intra- and (b) inter-GPU coherency. [] represents response traffic in [Data, rts, wts] or [Data] format, {} represents the updated cts of a cache. In (a), the two L2$ instances refer to the same physical L2$.
request from CU0 of GPU0 at \( t_1 \) and the write request from CU0 of GPU1 at \( t_1 \) are also handled in the same manner as in the case of intra-GPU coherency. The only difference is that the data for the write of \([X]\) and for the write of \([Y]\) reside in different L2$s. The read request (I0-3) by CU0 of GPU0 at \( t_1 \) still produces a cache hit in L1$. The read, there is no eviction of L2$ entries. When there is an eviction from the TSU, it is due to the eviction of L2$ entries. The eviction of TSU entries is related to the eviction of L2$ entries. When there is an eviction from the TSU, it is due to the eviction of L2$ entries. The eviction of TSU entries is related to the eviction of L2$ entries. Figure 6 shows the operation of the TSU. A request from the memory controller is sent to the TSU and the DRAM layer in parallel. The TSU responds with the timestamp for the cache block, and in parallel with the DRAM layer, responds with the cache block. Thus, the TSU never impacts the critical path of the DRAM access, and does not add any performance overhead. The eviction of TSU entries is related to the eviction of L2$ entries. When there is an eviction from the L2$ of a GPU, the TSU also evicts the timestamp for that cache block if it is not shared with other GPUs. The TSU logic determines the block sharers using the timestamp value. Assuming 64B cache block size, 4B for ACK, 4B for metadata and 8B address, HALCONE increases the network traffic by 5% and 5.26% for read and write transactions, respectively. This increases the read and write timestamps. It is assumed that the data for \([X]\) and \([Y]\) was lying in different L2$s. The read request issued by CU0 of GPU1 (I1-3) results in a different set of execution steps. This is because at \( t_2 \), there is no longer an L2$ hit, as the lease (\( \text{rts} = 7 \), \( \text{wts} = 0 \)) expired for a \( \text{cts} = 11 \). Hence the data for \([Y]\) has to be fetched from the MM. The MM has the updated value written by CU0 of GPU0. This value is received by CU0 of GPU1, and thus it becomes coherent with CU0 of GPU0. The execution order for both the instructions in this example is again I0-1→I1-1→I0-2→I0-3→I1-2→I1-3.

### 3.2.5 TSU Implementation

The TSU is physically placed inside the logic layer of the HBM stack. We could have chosen to place the TSU in the DRAM layer, but this would increase memory access latency. We designed the TSU as an 8-way set associative cache. The TSU needs to store the \( \text{mmts} \) for all of the blocks in all the L2$s in the MGPU system. We use 16 bits for each \( \text{mmts} \). Since we have 8 distributed L2$s modules in each GPU, each way of the TSU keeps track of the timestamps of the cache blocks in one of the L2$s modules. For example, for an MGPU with a 2MB L2$ per GPU, we need 64KB of space for the timestamps in the TSU for each GPU. As TSU logic only searches for the presence of the timestamp of a block and generates or updates timestamps, the latency for accessing the TSU is identical to a L3$ hit time of 40 cycles [17]. We conservatively assume a 50 cycles access latency for TSU.

Figure 6 shows the operation of the TSU. A request from the memory controller is sent to the TSU and the DRAM layer in parallel. The TSU responds with the timestamp for the cache block, and in parallel with the DRAM layer, responds with the cache block. Thus, the TSU never impacts the critical path of the DRAM access, and does not add any performance overhead. The eviction of TSU entries is related to the eviction of L2$ entries. When there is an eviction from the L2$ of a GPU, the TSU also evicts the timestamp for that cache block if it is not shared with other GPUs. The TSU logic determines the block sharers using the timestamp value. Assuming 64B cache block size, 4B for ACK, 4B for metadata and 8B address, HALCONE increases the network traffic by 5% and 5.26% for read and write transactions, respectively. If the timestamp value overflows, instead of flushing the cache, we simply re-initialize the timestamps to 0. This re-initialization results in a cache miss for one of the cache blocks. However, given we are using a write-through policy for writes in both L1$ and L2$, there is no chance of losing data belonging to the cache block experiencing the overflow. We just need to do an extra MM access. We need 1KB of storage per L1$ of size 256 KB and 128 KB of storage per L2$ of size 2 MB for holding the read and write timestamps. For each cache timestamp (\( \text{cts} \)), we use 64 bits. For an example GPU with 32 CUs, the GPU requires a total of 40 \( \text{cts} \) entries (32 for the 32 private L1$s belonging to each CU and 8 for the L2$s). Hence, we need a total of 320 bytes to represent all the \( \text{cts} \) values for the entire GPU.

### 4. Evaluation Methodology

In this section, we describe the MGPU system configurations, the simulator, standard application benchmarks, and the custom synthetic benchmarks (for stress testing HALCONE) that are used to evaluate different MGPU configurations.

#### 4.1 MGPU System Configurations

Table 2 shows the architecture of each GPU in our MGPU system. To complete a comprehensive evaluation, we evaluate five different MGPU configurations:

1. **MGPU system with RDMA (RDMA-WB-NC)**
2. **MGPU system with RDMA and HMG coherency (RDMA-WB-C-HMG)**
3. **MGPU-SM system, L2$ with WB and no coherency (SM-WB-NC)**
4. **MGPU-SM system, L2$ with WT and no coherency (SM-WT-NC)**
5. **MGPU-SM system, L2$ with WT and HALCONE (SM-WT-C-HALCONE)**

Figure 1 shows the RDMA configuration for a typical MGPU system. In this configuration, each GPU’s L1$ is connected to a switch (SW) that connects to another GPU’s L2$ for RDMA. Each switch forwards 16 bits per transfer. Switches run at 16 GTransfers/s. Thus, each switch can support a throughput of 32 GB/s (unidirectional link bandwidth between L2 and MM), which is the peak unidirectional bandwidth for PCIe 4.0 [11]. In the case of HMG, to maintain coherency, each GPU’s L2$ is connected to the switch (SW) and the protocol uses RDMA via L2$. For RDMA connections between L2$...
and MM, we use PCIe 4.0 links. For both baseline and HMG configurations, the MGPUSim simulator faithfully models the PCIe interconnects. For our MGPU-SM system, we group together the switches to form a switch complex. Both the L2$s and the MM are connected to the switch complex. The overall L2-to-MM bidirectional bandwidth is 256 GB/s, though each HBM supports an effective communication bandwidth of 341 GB/s [6]. Hence, in our MGPU-SM evaluation, the total L2-to-MM bandwidth is limited to 1 TB/s. We carefully model the queuing latency on the L2-to-MM network, as well as a fixed 100-cycle latency at the memory controllers (the number is calibrated using a real GPU with HBM memory). For our evaluation, we allocate memory by interleaving 4 KB pages across all the memory modules in the MGPU system.

Our evaluation of the RDMA-WB-NC and SM-WB-NC configurations is aimed at exposing the need for our proposed MGPU-SM cache coherent systems (more details in Section 5). The SM-WB-NC and SM-WT-NC configurations are used to compare L2$ write-back (WB) policy with L2$ write-through (WT) policy in a MGPU-SM system. This comparison helps us learn which write policy is more suitable for L2$ in a MGPU-SM system. The SM-WT-NC and SM-WT-C-HALCONE configurations are then compared to determine the overhead of coherence (we use a WT policy as it provides better performance than WB, as reported in our experiments in Section 5). The comparison between configuration RDMA-WB-C-HMG and SM-WT-C-HALCONE demonstrates the improvements achieved by our proposed solution over the most optimized hardware coherence support for MGPU systems (HMG protocol). Except for HMG which leverages scope based memory consistency model, we adopt existing weak memory consistency model for our evaluation. Nonetheless, our HALCONE protocol can work as a building block for more strict memory consistency models.

4.2 Simulation Platform

We use the MGPUSim [32] simulator to model MGPU systems. MGPUSim has been validated against real AMD MGPU systems. We modified the simulator and its memory hierarchy to support HALCONE. After implementing the HALCONE protocol, we verify the implementation using unit, integration, and acceptance tests provided with the simulator. We also modified the simulator to support the HMG protocol by implementing a hash function that assigns a home node for a given address, directory support for tracking sharers and invalidation support for sending messages to the sharers as needed.

4.3 Benchmarks

We use standard application GPU benchmarks as well as synthetic benchmarks to evaluate our HALCONE protocol in an MGPU-SM system.

4.3.1 Standard Benchmarks

We use a mix of memory-bound and compute-bound benchmarks, 11 in total (see Table 3), from the Hetero-Mark [34], PolyBench [26], SHOC [9], and DNNMark [10] benchmark suites to examine the impact of our HALCONE protocol on the MGPU-SM system. In addition, these workloads have large memory footprints and represent a variety of data sharing patterns across different GPUs. More details about the benchmarks can be found in [32, 33].

### Table 3: Standard benchmarks used in this work. Memory represents the footprint in the GPU memory.

| Benchmark (abbr) | Suite | Type | Memory |
|-----------------|-------|------|--------|
| Advanced Encryption Standard (aes) | Hetero-Mark | Compute | 71 MB |
| Matrix Transpose and Vector Multiplication (atx) | PolyBench | Memory | 64 MB |
| Breadth First Search (bs) | SHOC | Memory | 574 MB |
| BiCGStab Linear Solver (bicg) | PolyBench | Compute | 64 MB |
| Bitonic Sort (bs) | AMDAPPSDK | Memory | 67 MB |
| Finite Impulse Response (fir) | Hetero-Mark | Memory | 67 MB |
| Floyd Warshall (fws) | AMDAPPSDK | Memory | 32 MB |
| Matrix Multiplication (mm) | AMDAPPSDK | Memory | 192 MB |
| Maxpooling (mp) | DNNMark | Compute | 64 MB |
| Rectified Linear Unit (rl) | DNNMark | Memory | 67 MB |
| Simple Convolution (conv) | AMDAPPSDK | Memory | 145 MB |

#### 4.3.2 Synthetic Benchmarks

The publicly available benchmark suites mentioned in Section 4.3.1 have been developed considering the lack of hardware-level coherency support in GPUs. Hence, these benchmarks cannot necessarily harness the potential benefit of the hardware-support for coherency in our MGPU-SM system. To stress test our HALCONE protocol, we develop a synthetic benchmark suite called **Xtreme**. There are three benchmarks in the Xtreme suite9. All the benchmarks in the Xtreme suite perform a basic vector operation: \( C = A + B \), where \( A \) and \( B \) are floating point vectors. We describe the basic operation of the Xtreme benchmarks with a simple example. For each example, we assume the following:

1. There are two GPUs: GPU\(_X\) and GPU\(_Y\).
2. Both GPU\(_X\) and GPU\(_Y\) are equipped with two CUs each: CU\(_X0\), CU\(_X1\), and CU\(_Y0\) and CU\(_Y1\), respectively.
3. There are three vectors \( A, B \) and \( C \) that are used to compute \( C = A + B \) using both GPU\(_X\) and GPU\(_Y\).
4. Each of the three vectors, \( A, B \) and \( C \), are split into 4 slices: \( A_0, A_1, A_2 \) and \( A_3 \); \( B_0, B_1, B_2 \) and \( B_3 \); and \( C_0, C_1, C_2 \) and \( C_3 \).
5. At the beginning of the program, CU\(_X0\) reads \( A_0, B_0 \), and \( C_0 \); CU\(_X1\) reads \( A_1, B_1 \), and \( C_1 \); CU\(_Y0\) reads \( A_2, B_2 \), and \( C_2 \); and CU\(_Y1\) reads \( A_3, B_3 \), and \( C_3 \).

The three Xtreme benchmarks work as follows:

**Xtreme1:**

1. CU\(_X0\) performs \( C_0 = A_0 + B_0 \); Similarly, CU\(_X1\) operates on \( A_1, B_1 \) and \( C_1 \); CU\(_Y0\) operates on \( A_2, B_2 \) and \( C_2 \); and CU\(_Y1\) operates on \( A_3, B_3 \) and \( C_3 \).
2. Repeat step 1 10 times.
3. CU\(_X0\) performs \( A_0 = C_0 + B_0 \); Similarly, CU\(_X1\) operates on \( A_1, B_1 \) and \( C_1 \); CU\(_Y0\) operates on \( A_2, B_2 \) and \( C_2 \); and CU\(_Y1\) operates on \( A_3, B_3 \) and \( C_3 \).
4. Repeat step 3 10 times.

With Xtreme1, we evaluate the impact of consecutive writes to the same location by a CU. There is no data sharing between the CUs or the GPUs. When there is a write to any location, the corresponding entry of the L1$ and L2$ sets are updated and generate read misses. Steps 2 and 4 force coherency misses in the caches.

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9All the benchmarks in the Xtreme suite perform repeated writes to and reads from the same location. This extreme behavior is typically uncommon in regular GPU benchmarks, and so the name Xtreme.
Xtreme2:  
1. CU X0 performs C0 = A0 + B0; Similarly, CU Y1 operates on A1, B1 and C1; CU Y0 operates on A2, B2 and C2; and CU Y1 operates on A3, B3 and C3.  
2. CU X0 performs A1 = C1 + B1;  
3. Repeat step 2 10 times.  
4. Repeat step 1

With Xtreme2, we stress test HALCONE for intra-GPU coherency. There is a SWMR invariant dependency between CU X0 and CU Y1 at 2. CU X0 writes to a location that was previously read by CU Y1. Step 3 forces coherency misses.

Xtreme3:  
1. CU X0 performs C0 = A0 + B0; Similarly, CU Y1 operates on A1, B1 and C1; CU Y0 operates on A2, B2 and C2; and CU Y1 operates on A3, B3 and C3.  
2. CU X0 performs A1 = C1 + B1;  
3. Repeat step 2 10 times.  
4. Repeat step 1

With Xtreme3, we stress test HALCONE for inter-GPU coherency. The difference between Xtreme2 and Xtreme3 is that at 2, CU X0 writes to a location that was previously read by CU Y1 and CU Y1, respectively.

In our evaluation, we vary vector sizes from 192 KB to 96 MB for A, B and C so that we can examine the impact of capacity misses at different levels of the memory hierarchy.

5. EVALUATION

In this section, we present our evaluation of the HALCONE protocol for both existing standard benchmarks and synthetic benchmarks. The standard benchmarks have been developed in accordance with the current MPGU programming model that assumes no hardware support for coherency and places the burden of maintaining coherency on the programmer. Hence, we evaluate these traditional GPU benchmarks to ensure our HALCONE protocol does not introduce extra overhead for these legacy cases, where coherency has been maintained by the GPU programmer. Next, we evaluate the Xtreme benchmarks, a set of three synthetic benchmarks that leverage hardware support for coherency to ensure the correctness of their computations.

5.1 Standard Benchmarks

We compare 5 different MPGU configurations: RDMA-WB-NC as our baseline, RDMA-WB-C-HMG, SM-WB-NC, SM-WT-NC and SM-WT-C-HALCONE assuming a 4-GPU system. We use a WrLease of 5 and a RdLease of 10 for this evaluation. Please refer to Section 5.4 for details on why we choose these lease values.

Figure 7(a) shows the speed-up for different MPGU configurations, as compared to RDMA-WB-NC. Our evaluation shows that the RDMA-WB-C-HMG, SM-WB-NC, SM-WT-NC, and SM-WT-C-HALCONE configurations achieve, on average, a 1.5 ×, 3.9 ×, 4.6 ×, and 4.6 × speed-up, respectively, versus RDMA-WB-NC. There are two reasons why all 3 shared memory configurations are faster than using RDMA-WB-NC alone.

First, RDMA-WB-NC requires data copy operations between the CPU and GPUs. Shared memory eliminates this traffic since the CPU and GPUs share the same memory. Second, during kernel execution, all of the GPUs are required to use RDMA to access data residing on other GPUs’ memory for the baseline. The shared main memory allows sharing of data across GPUs with no RDMA overhead.

For the compute-bound benchmarks (i.e., aes, atax, bicg, and mpi), all the MPGU-SM configurations achieve lower (1.2 × to 2.0 ×) speed-up as compared to the speed-up achieved for the memory-bound benchmarks (3 × to 27 ×). This is due to the memory-bound benchmarks’ higher reliance on the high overhead RDMA for shared data access than the compute-bound benchmarks. Even though RDMA-WB-C-HMG uses RDMA, this configuration brings the cache blocks from a remote GPU in its L2$ instead of its L1$ as in the case of RDMA-WB-NC. Hence, workloads that exploit temporal and spatial locality (i.e., mm and conv) achieve speed-up up to 18 × for RDMA-WB-C-HMG configuration.

If we compare the speed-up of SM-WB-NC and SM-WT-NC, for all the compute-bound benchmarks, the difference between a WB L2$ and a WT L2$ is less than 1%. But for the memory-bound benchmarks, we observe up to 3 × better performance when employing a WT cache. This lower performance of WB cache can be explained by inspecting the L1$ and L2$ transactions. Figures 7(b) and 7(c) show the normalized L2$ and L1$ traffic in terms of number of L2$ to MM and L1$ to L2$ transactions and responses, respectively, for both read and write operations. As we observe in Figures 7(b), as expected, when using WB there are, on average, 22.7% less transactions than WT from L2$ to MM for all the benchmarks. However, it is counter-intuitive that even with fewer L2$ to MM transactions, SM-WB-NC performs worse than SM-WT-NC. For a read or write miss in the L2$ with a WB policy, first, the L2$ performs a write to MM to generate a cache eviction if there is either a conflict or capacity miss. Only then the L2$ can service the pending read or write transactions. The L2$ generating the WB becomes a bottleneck when there are frequent cache evictions.

Note that the benchmarks in our evaluation use large memory footprints to generate frequent capacity and conflict misses in the L2$. Additionally, the benchmarks are streaming in nature. Hence, the benchmarks have frequent cache evictions, which perform worse with WB than with WT. With a WT L2$, we do not need to write the data to the MM in case of an eviction as the updated copy of the data is always available in the MM. The transactions from L1$ to L2$ remain the same for both SM-WB-NC and SM-WT-NC across all benchmarks.

Figure 7(a) also shows that our proposed SM-WT-C-HALCONE suffers, on average, a 1% performance degradation as compared to the SM-WT-NC configuration. This slight performance degradation is due to more L1$ transactions being generated for SM-WT-C-HALCONE as compared to SM-WT-NC, as seen in Figure 7(c). As explained earlier, the standard benchmarks do not require any support for coherency and due to their streaming nature (which means these benchmarks continuously read and write to different cache blocks) they suffer capacity and conflict misses instead of coherency misses. For more details on this, refer to Section 5.3. We conclude that our HALCONE protocol is efficient as it causes, on average, 1% performance degradation for standard MPGU benchmarks when compared to an MPGU system with SM-WT-NC configuration. Moreover, compared to RDMA-WB-NC,

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10 We use normalized values here due to the wide variations in the number of L2$ to MM as well as L1$ to L2$, transactions across the different benchmarks.
Figure 7: (a) Speed-up for different MGPU systems, normalized versus RDMA-WB-NC. (b) Number of L2$ to MM transactions for SM-WT-NC and SM-WT-C-HALCONE normalized versus the number of transactions for the SM-WB-NC configuration in an MGPU system. (c) Number of L1$ to L2$ transactions for SM-WT-NC and SM-WT-C-HALCONE normalized versus the number of transactions for the SM-WB-NC configuration in an MGPU system. Mean refers to geometric mean.

an MGPU system with the SM-WT-C-HALCONE configuration has, on average, 4.6× better performance. Besides, the SM-WT-C-HALCONE configuration, on average, outperforms RDMA-WB-C-HMG configuration by 3×.

5.2 Scalability Study

We use strong scaling to explore the scalability of the MGPU-SM system with HALCONE protocol, by varying both the GPU count and CU count while keeping the size of the workloads constant.

5.2.1 GPU Count Scalability Study

For this study, we use 32 CUs per GPU as the baseline comparison point. Figure 8(a) shows the speed-up for GPU counts of 1, 2, 4, 8 and 16. Here, runtimes are normalized to that of a single GPU. On average, we achieve a 1.76×, 2.74×, 4.05×, and 5.43× speed-up in comparison to a single coherent GPU for 2, 4, 8, and 16 GPUs, respectively. Some of the workloads (i.e., atax, bicg, mp and relu), do not scale well beyond 4 GPUs due to lesser computations available for each GPU and so do not benefit from a larger GPU count. Nonetheless, the comparison shown in Figure 8(a) confirms that our proposed HALCONE protocol is scalable and does not limit the scalability of an MGPU-SM system.

5.2.2 CU Count Scalability Study

For this study, we use a 4-GPU system and consider 32, 48 and 64 CUs per GPU (see Figure 8(b) and Figure 8(c)). The atax, bicg, mp, and relu benchmarks do not scale with CU count as they do not have sufficient compute intensity. The bfs and bs benchmarks do not scale as we increase the CU count because of a L2$ bottleneck. For these benchmarks, the number of transactions from L2$ to MM for 32 CUs is the same as the number of transactions for 48 and 64 CUs. Hence, L2$ queuing and serialization latencies dominate the runtime, irrespective of the number of CUs. In Figure 7(b) and Figure 7(c), we have already demonstrated that our HALCONE protocol, on average, introduces only 1% additional traffic from L2$ to MM and from L1S to L2$. The bfs and bs benchmarks suffer from the L2$ bottleneck, even when the MGPU system lacks coherency. Hence, the HALCONE protocol itself is not a bottleneck in terms of CU scalability. The aes, fir, mm and conv benchmarks, do not stress the L2$ even if the number of transactions from L2$ to MM increases with the increased CU count and have sufficient compute intensity to take advantage of higher CU count. Hence, these benchmarks benefit from a larger number of CUs. On an average we see 1.12× and 1.24× speed-up as we increase the CU count from 32 to 48 and 64, respectively.

5.3 Xtreme Benchmarks

As discussed before, the standard MGPU benchmarks have been developed in accordance with the assumption that there is no hardware support for coherency and no weak-consistency programming model assumed for the GPUs. Hence, we use our synthetic benchmark suite, Xtreme, to evaluate the impact of our proposed HALCONE protocol for some of the extreme cases of applications, where we need coherency to ensure the correctness of the computation. With Xtreme benchmarks, we evaluate three different scenarios:

1. The data size is small, so there are neither L1$ nor L2$ capacity or conflict misses.
2. The data size is large enough to cause L1$ capacity and conflict misses, but not large enough to cause L2$ capacity or conflict misses.
3. The data size is large enough to cause both L1$ and L2$ capacity and conflict misses.

We use MGPU-SM with 4 GPUs for this evaluation. Figure 9 shows the comparison of speed-up for SM-WT-NC and SM-WT-C-HALCONE for all three Xtreme benchmarks. The repeated writes to the same cache location in Xtreme1 cause the cts of both the L1$ and L2$ to step ahead in logical time, leading to coherency misses for the data that was read before. For a vector size of 192 KB, we observe a performance degradation of 14.3% for SM-WT-C-HALCONE. As the vector size increases, there are more capacity and conflict misses, and eventually capacity and conflict misses far outnumber coherency misses. The coherency misses can occur if the lease expires for a cache block. However, if there are frequent cache evictions because of conflict or capacity misses, the cache blocks are evicted based on an LRU policy, even if the lease is valid. Thus, for a vector size of 98304 KB, we observe only a 0.6% performance degradation for SM-WT-C-HALCONE in comparison to SM-WT-NC. The Xtreme2 benchmark exploits intra-GPU coherency. Xtreme3 requires inter-GPU coherency among the MGPUs for correctness. The data dependency in Xtreme2 and Xtreme3 results in coherency misses when repeated writes are performed. We observe a performance degradation of up to 12.1% and 16.8% for Xtreme2 and Xtreme3, respectively. This degradation decreases as the data size increases due to the corresponding increase in capacity and conflict misses in L1$ and L2$.

5.4 Sensitivity to Timestamps

We used (RdRelease, WrRelease) = (5, 10) for our evaluations. We examined the impact of using different (RdRelease, WrRelease) values of (2, 10), (10, 2), (5, 10), (10, 5), (20, 10),
Figure 8: (a) GPU scalability: Speed-up for the SM-WT-C-HALCONE with different #GPUs normalized to that of a single coherent GPU. (b) and (c) CU scalability: Speed-up and #L2$ transactions for the SM-WT-C-HALCONE with different #CUs normalized to that of the SM-WT-C-HALCONE with 32 CUs. Mean stands for geometric mean.

Figure 9: Speed-up for the Xtreme benchmarks running on an MGPU system with SM-WT-C-HALCONE w.r.t. an MGPU system with SM-WT-NC for different vector sizes: (a) Xtreme1, (b) Xtreme2 and (c) Xtreme3 and (10, 20) using the coherence-aware Xtreme benchmarks. We found that if the difference between the WrLease and RdLease and the RdLease is increased to 10 from 5, then the benchmark performance degrades by up to 3% for the Xtreme. So we need to maintain a smaller difference between RdLease and WrLease. In terms of absolute values of RdLease and WrLease, a large value of the RdLease can help an application that performs significantly smaller number of writes than number of reads. On the other hand, a smaller RdLease results in more coherency misses. We choose a smaller WrLease value than RdLease value based on the assumption that if a CU or a GPU writes to a cache block, it may write to the same cache block in the future. This, in turn, prevents consecutive writes to the same block and avoids making cts too large, potentially causing many coherency misses.

6. RELATED WORK

MGPU systems have been recently adopted as the computing platform of choice by variety of data-intensive applications. Today there is growing interest in developing optimized MGPU system architectures and efficient hardware coherence support to reduce programming complexity.

MGPU System Design: Milic et al. propose a NUMA-aware multi-socket GPU solution to resolve performance bottlenecks related to NUMA memory placement in multi-socket GPUs [19]. The proposed system dynamically adapts inter-socket link bandwidth and caching policies to avoid NUMA effects. Our CC-MGPU system completely avoids the impact of NUMA on performance. Arunkumar et al. [27] and Ren et al. [27] propose a MCM-GPU, where multiple GPU modules are integrated in a package to improve energy efficiency. As in MCM-GPU, our CC-MGPU can take advantage of novel integration technologies to improve energy efficiency and performance. Arunkumar et al. [3] also argue the need to improve inter-GPU communication. We plan to explore high-bandwidth network architectures for CC-MGPU systems in the future.

MGPU Coherence: NUMA-Aware multi-socket GPU [19] maintains inter-GPU coherency by extending SW-based coherence for L1$s to the L2$s. The resulting coherency traffic lowers application performance. Similarly, MCM-GPU [2] leverages the software-based L1$s coherence protocol for its L1.5$s. The flushing of the caches and coherence traffic hurt system scalability. Young et al. [39] propose CARVE method, where part of a GPU’s memory is used as a cache for shared remote data and the GPU-VI protocol is used for coherency. This protocol does not scale well with an increase in the amount of read-write transactions and false sharing. Also, the CARVE method can cause performance degradation for workloads with large memory footprint as it reduces effective GPU memory space. To reduce coherency traffic, Singh et al. propose timestamp-based coherence (TC) protocol for intra-GPU coherency [31]. As this protocol relies on a globally synchronized clock across all CUs, maintaining clock synchronization is a challenging task for large MGPU systems. To address this, Tabakh et al. [35] propose a logical timestamp based coherence protocol (G-TSC). However, as discussed in Section 2.2, the G-TSC protocol is designed for single GPU systems and does not scale well for MGPU systems. HMG [27] is a recent hardware-managed cache coherence protocol for distributed L2$s in MCM-GPUs using a scoped memory model consistency. HMG proposes to extend a simple VI-like protocol to track sharers in a hierarchical way that is tailored to the MCM-GPU architecture, and achieves a cost-effective solution in terms of on-chip area overhead, inter-GPU coherence traffic reduction and high performance. This protocol, however, relies on error-prone scoped memory consistency model that increases programming complexity. In contrast, our new timestamp-based coherence HALCONE protocol operates assuming weak consistency model, which is currently adopted by modern GPU products, and is able to outperform HMG by $3 \times$ on average (see Section 5.1).

7. CONCLUSION

In this work, we propose a novel MGPU system, where GPUs physically share the MM. This system eliminates the programmer’s burden of unnecessary data replication and expensive remote memory accesses. To ensure seamless sharing of data across and within multiple GPUs, we propose HALCONE, a novel timestamp-based coherence protocol. For standard benchmarks, a MGPU-SM system (that has 4 GPUs and uses HALCONE) performs on average, 4.66× faster than the non-coherent conventional MGPU system with same number of GPUs. In addition, compared to a coherent MGPU
system using the state-of-the-art HMG coherence protocol, an MGPU system that uses HALCONE reports 3× higher performance. Our scalability study shows that our coherence protocol scales well in terms of both GPU count and CU count. We develop synthetic benchmarks that leverage data sharing to examine the impact of our HALCONE protocol on performance. For the worst case scenario in our synthetic benchmarks, the proposed MGPU-SM with HALCONE suffers from only a 16.8% performance overhead.

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