Memristive Computing for Efficient Inference on Resource Constrained Devices

Venkatesh Rammamoorthy
University of Central Florida
Florida, USA

Geng Zhao
University of Central Florida
Florida, USA

Bharathi Reddy
Sundrape Inc.
Bangalore, India

Ming-Yang Lin
Nanjing University
Nanjing, China

Abstract—The advent of deep learning has resulted in a number of applications which have transformed the landscape of the research area in which it has been applied. However, with an increase in popularity, the complexity of classical deep neural networks has increased over the years. As a result, this has leads to considerable problems during deployment on devices with space and time constraints. In this work, we perform a review of the present advancements in non-volatile memory and how the use of resistive RAM memory, particularly memristors, can help to progress the state of research in deep learning. In other words, we wish to present an ideology that advances in the field of memristive technology can greatly influence and impact deep learning inference on edge devices.

I. INTRODUCTION

Memristors were first proposed by Leon Chua [1] as the missing element of the circuit, which can be used to change its resistance based on the amount of current passing through it. This spurred an interesting line of research on using the concept of spike-timing-dependent-plasticity (STDP) to program the resistance of the memristor [2]–[4]. This enabled several methods to use the properties of a memristor to emulate an artificial biological synapse. Fig. 1 shows the resistive memory model for a memristor, in which the resistance of the model is coupled with the voltage across it. Interestingly, there have been previous papers which have supported the positive impact of advancement in resistive memory on deep learning, particularly computer vision [5], further proposing the impact in medical and sport sciences as well [6]–[8].

Interesting, a few papers have employed memristors to realize highly sparse and efficient convolutional neural networks which can easily be deployed on devices with significant time and space constraints. Some approaches have designed a memristor-based sparse compact convolutional neural network (MSC CNN) to reduce the number of memristors [9]. An average pooling and $1 \times 1$ convolutional layer are used in order to replace fully connected layers. Meanwhile, depthwise separation convolution is utilized to replace traditional convolution to further reduce the number of parameters. Furthermore, a network pruning method is adopted to remove the redundant memristor crossbars for depthwise separation convolutional layers. Therefore, a more compact network structure is obtained while the recognition accuracy remaining unchanged.

Another approach uses memristors to perform pruning as well as quantization in deep neural networks by incorporating alternating direction method of multipliers (ADMM) while training the deep neural network.

Interesting, a few papers have employed memristors to realize highly sparse and efficient convolutional neural networks which can easily be deployed on devices with significant time and space constraints. This paper aims to design a memristor-based sparse compact convolutional neural network (MSC-CNN) to reduce the number of memristors [9]. An average pooling and $1 \times 1$ convolutional layer are used in order to replace fully connected layers. Meanwhile, depthwise separation convolution is utilized to replace traditional convolution to further reduce the number of parameters. Furthermore, a network pruning method is adopted to remove the redundant memristor crossbars for depthwise separation convolutional layers. Therefore, a more compact network structure is obtained while the recognition accuracy remaining unchanged.

The framework primarily consists of three main steps:

- Memristor-based ADMM regularized optimization
- Masked mapping
- Retraining

The above method was able to achieve an impressive compression rate of over $20\times$ with respect to the weight compression rate and a compression of $24\times$ with regard to the weight quantization of the deep learning models. Table I shows the results of the model on CIFAR-10 and MNIST datasets for deep learning models such as LeNet-5, ResNet-18 and VGG-16. While several papers have explored more complicated methods of pruning such as pruning during training [11], pruning after training (in which the model is pruned after it is completely trained, followed by a fine-tuning procedure to ensure convergence of the pruned model), pruning before training [13], hardware-based methods have gone for more conventional methods of pruning. These methods have mostly adhered to iterative pruning strategies in which the model is either trained and pruned multiple times, or the model is pruned after the corresponding reference model achieves convergence on the dataset. For instance, in [3], an
Fig. 1: The IV characteristic of a memristor - shown as the missing element of the circuit. Additionally, the memristor has also been shown in terms of a programmable resistance based on the amount of doping in the memristor.

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Another related field in which memristors have found a lot of impact has been neuromorphics [15]–[19]. Computation using memristive systems provide an interesting and compelling solution to increase the overall efficiency of the neuromorphic system. While some papers have identified some gaps in the behavior-level dynamics of memristive computing systems during simulation and proposed solutions, other have used different fabrication techniques to apply memristors for more machine learning based applications. Some of these applications include implementing well-known machine learning algorithms such as a multilayer perceptron network, K Nearest Neighbors and Independent Component Analysis [20], [21].

Memristor-based computation provides a promising solution to boost the power efficiency of the neuromorphic computing system.

II. Conclusion

In this study, we examine the state of research in resistive RAM technology, particularly in the field of memristors. We found that a majority of approaches have used the analog properties of memristors to emulate the learning capabilities of a biological synapse. A number of studies have shown that Memristor-based matrix-vector multiplication platform provides fast computation, high accuracy and low design cost. However, as the development of memristor technology is still maturing, device defects and fabrication yield may be a significant concern. Specifically, the single-bit failure (SBF) denotes a device that freezes in a high conductance state (“stuck-on”) or a low conductance state (“stuck-off”). Although neural networks usually can tolerate a certain number of imperfect synaptic weights, high SBF rate degrades the computation accuracy significantly. For example, we tested a feed-forward neural network for MNIST database: as the SBF rate increases to 20%, the average recognition accuracy rapidly dropped from 92.64% to 39.4%, which is far below an acceptable range. Redundancy schemes have been widely adopted in memory designs. But it is not efficient for the memristor-based analog computations with high precision requirement.

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| Method               | Original Accuracy | Pruned Accuracy | Crossbar Area Saved | Compression Ratio | 7-bit | 6-bit | 5-bit |
|----------------------|-------------------|-----------------|---------------------|------------------|-------|-------|-------|
| **MNIST**            |                   |                 |                     |                  |       |       |       |
| Group Scissor [23]   | 99.15%            | 99.14%          | 75.94%              | 4.16×            | -     | -     | -     |
| our LeNet-5          | 99.17%            | 99.15%          | 94.34%              | 17.69×           | 99.07%| 99.03%| 99.03%|
|                     |                   |                 |                     |                  |       |       |       |
| **CIFAR-10**         |                   |                 |                     |                  |       |       |       |
| Group Scissor [23]   | 82.01%            | 82.09%          | 57.43%              | 2.35×            | -     | -     | -     |
| our ConvNet          | 84.41%            | 84.55%          | 57.45%              | 2.35×            | 84.18%| 83.50%| 80.81%|
| our VGG-16           | 93.70%            | 93.76%          | 89.26%              | 9.31×            | 93.67%| 93.64%| 93.26%|
| our ResNet-18        | 94.14%            | 93.79%          | 91.49%              | 11.75×           | 93.68%| 93.25%| 92.92%|

\*Numbers of parameter reduced: 8.65K

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| **CIFAR-10**         |                   |                 |                     |                  |       |       |       |
| Group Scissor [23]   | 82.01%            | 82.09%          | 57.43%              | 2.35×            | -     | -     | -     |
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| our VGG-16           | 93.70%            | 93.36%          | 89.26%              | 9.31×            | 93.67%| 93.64%| 93.26%|
| our ResNet-18        | 94.14%            | 93.20%          | 91.49%              | 11.75×           | 93.68%| 93.25%| 92.92%|

\*Numbers of parameter reduced: 102.30K, VGG-16: 13.98M, ResNet-18: 10.46M

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