Specializing Coherence, Consistency, and Push/Pull for GPU Graph Analytics

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Abstract—This work provides the first study to explore the interaction of update propagation with and without fine-grained synchronization (push vs. pull), emerging coherence protocols (GPU vs. DeNovo coherence), and software-centric consistency models (DRF0, DRF1, and DRFrlx) for graph workloads on emerging integrated GPU-CPU systems with native unified shared memory. We study 6 graph applications with 6 graph inputs for a total of 36 workloads running on 12 system (hardware-software) configurations reflecting the above design space of update propagation, coherence, and memory consistency. We make three key contributions. First, we show that there is no single best system configuration for all workloads, motivating systems with flexible coherence and consistency support. Second, we develop a model to accurately predict the best system configuration – this model can be used by software designers to decide on push vs. pull and the consistency model and by flexible hardware to invoke the appropriate coherence and consistency configuration for the given workload. Third, we show that the design dimensions explored here are inter-dependent, reinforcing the need for software-hardware co-design in the above design dimensions. For example, software designers deciding on push vs. pull must consider the consistency model supported by hardware – in some cases, push maybe better if hardware supports DRFrlx while pull may be better if hardware does not support DRFrlx.

I. INTRODUCTION

As technology scaling slows down, architects are increasingly relying on alternative designs that can provide continued performance scaling with the available transistors [1]. Specialization is one such approach where a processing element is designed to perform a specific task. These specialized processors make more efficient use of transistors in terms of area and performance, but are harder to program and less widely applicable than general purpose processors. To get around these limitations, system designers also leverage heterogeneity of processing elements by providing many different kinds of processing elements, each suited to different uses. The graphics processing unit (GPU) is an example of a specialized processor which is both being integrated on-chip with central processing units (CPUs) and becoming more general purpose. This allows application developers to accelerate parallel portions of their applications with a GPU architecture that is designed for large-scale parallelism and memory throughput.

The domain of graph analytics is one that has been shown to benefit from increasingly specialized processors and software stacks. Many frameworks exist that generalize and provide abstractions for programming and optimizing graph workloads [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14]. While numerous frameworks focused on distributed and shared memory multi-core CPU systems, some have been implemented for the GPU with the goal of providing better performance and scalability than the more traditional CPU graph frameworks. Topology-driven, vertex-centric implementations [13], [15], [16] of graph algorithms are commonly used because they are easy to implement and can achieve high throughput on GPUs via their asynchronous thread structure. A significant algorithmic design choice affecting these implementations is that of update propagation in terms of push vs. pull [17]. For kernels of graph algorithms that need to perform edge-propagated updates, a source vertex can either pull changes from its neighbors or push changes to its neighbors. For a given algorithm, both choices preserve the direction of the edge-propagated updates through the edge, but can change the control-flow and memory access behavior of the implementation. More importantly, pull does not require fine-grained synchronization while push does.

Traditional GPU architectures suffer from unique challenges which cause fine-grained synchronization to be performance prohibitive. Recently, however, with CPU-GPU integration and native support for a global (shared) address space, new coherence protocols and software-centric memory consistency models have been proposed and/or commercially implemented which make fine-grained synchronization more efficient on GPUs. For example, in contrast to conventional GPU coherence protocols (referred to as GPU coherence [18]), the DeNovo protocol [18] uses ownership to exploit synchronization locality in L1 caches. Similarly, in contrast to the simple DRF0 consistency model, the DRF1 model avoids heavyweight invalidation and dirty data flushing at unpaired synchronization points and the DRFrlx model further allows reordering relaxed synchronization operations [19].

This work provides the first study that explores the interaction of update propagation with and without fine-grained synchronization (push vs. pull), emerging coherence
protocols (GPU vs. DeNovo coherence), and software-centric consistency models (DRF0, DRF1, and DRFRlx) for graph workloads on emerging integrated GPU-CPU systems with native unified shared memory. The paper makes the following contributions.

**Need for flexibility – one size does not fit all:** We evaluate the impact of graph algorithm and graph input on the hardware+software design decisions for update-propagation (push or pull), coherence protocol (GPU or DeNovo), and consistency model (DRF0, DRF1, or DRFRlx). We study 6 graph algorithms and 6 graph inputs for a total of 36 workloads on the 12 possible configurations of hardware+software (referred to as system below). We find that there is no one configuration that is optimal for all cases. The configuration with push, GPU coherence, and DRFRlx consistency model performs the best for 24 (majority) of the workloads, but for the remaining 12, different configurations perform significantly better (reducing execution time by up to 87%, average of 44%). This motivates systems with flexible consistency models and flexible coherence protocols such as Spandex [20] which can adapt to the different needs of different graph workloads.

**A model to predict the best design choice:** We develop a simple model to predict the best performing system configuration (of the 12 choices for update propagation, coherence, and consistency combinations) for a given graph algorithm and input. The model uses only 6 simple parameters to represent the graph algorithm and input, which drive a decision tree to choose the optimal system configuration. For each of the 36 workloads, the model picks a configuration that performs within 3.5% of the best one. For 28 of the 36 cases, it picks exactly the optimal configuration. This model can be used by software developers to determine the appropriate software configuration and by system designers to drive configuration selection for an adaptive system such as Spandex [20].

**Inter-dependent design dimensions:** Our evaluation also shows that the three design dimensions (update propagation, coherence, and consistency) are interdependent; choosing one without consideration of the support for others can lead to significantly sub-optimal designs. For example, the choice of push vs. pull depends, in general, on whether the system supports DRFRlx. Specifically, for graphs with high load imbalance, assuming the system supports DRFRlx leads to a choice of push. However, running push on a system that supports only DRF1 instead of DRFRlx can perform up to 80% worse than a pull based implementation. Thus, design decisions for pull vs. push that ignore consistency support can lead to significantly sub-optimal decisions. Recognizing such interdependencies, we also show how to extend our model to determine the optimal configuration assuming only partial support for the design space considered.

**Summary:** Overall, this work is the first to systematically consider the impact of emerging coherence and consistency options on graph algorithms running on integrated GPUs. Our results motivate support for flexible coherence and consistency, we show a model to predict the best configuration for a graph algorithm + input and to drive flexible systems, and we demonstrate the interdependence of the design decisions of push vs. pull, consistency, and coherence supported.

### II. DESIGN SPACE

To study the interaction of irregular workloads with the underlying communication fabric, we first describe an implementation design space comprised of three dimensions: push vs. pull, cache coherence protocols, and memory consistency models. Table I summarizes this design space and the salient trade-off considerations for each implementation. Each implementation represents a design specialization that can be made for the irregular graph workloads that we explore. The salient features of these implementations are used by our specialization model in Section IV.

#### A. Push vs. Pull

We define push vs. pull as the dimension where updates may be to shared remote vertex properties or unshared local vertex properties, respectively.

Figure 1 shows pseudocode for two representative kernels: one using push updates and another using pull updates. Interest in this dimension is motivated by considerations for fine-grained synchronization overhead, as well as the elision of redundant work (described in depth in Sections III).

Although push updates incur additional overheads via the use of atomics, optimizations for atomics in the coherence and consistency dimensions are available to maintain or even

### TABLE I: Summary of the implementation design space and the salient features explored by the model described in this work. Salient features are introduced in Section II and then discussed in the context of specialization in Section IV.

| Implementation | Description | Salient Features |
|----------------|-------------|------------------|
| **Push vs. Pull Dimension** | | |
| Pull | Target in outer loop; Sparse remote reads; Elide work at sources; | |
| Push | Source in outer loop; Dense local reads; Sparse remote atomics; Elide work at targets; | |
| Push+Pull | Non-deterministic source/target direction; Remote reads and updates; | |
| **Coherence Dimension** | | |
| GPU | Write-through at L1 on sync.; Self-inval. at L1 on sync.; Atomics at L2 (bypass L1); Good when low update reuse; | |
| DeNovo | Registration (ownership) at L1 on sync.; Atomics at L1; Good when high update reuse; | |
| **Consistency Dimension** | | |
| DRF0 | Data to data reordering; Seq. consistency for acquires&releases; Overlapping data accesses w/ data updates; Programmability; | |
| DRF1 | Data to data reordering; Data to atomics reordering; Overlapping data accesses w/ atomics; Programmability; | |
| DRFRlx | Data-data reordering; Data-atomic reordering; Atomic-atomic reordering; Overlapping atomics; Overlapping atomics; Mitigate imbalance via MLP; | |
We consider a commonly used protocol, referred to as workload’s properties. The vprop, update, and atomicUpdate functions influence the algorithmic information of the workload. The iteration variable therefore do not consider HRF here. We also note that DRFrlx provides efficiency than GPU coherence+HRF and with easier programmability. We programmability cost since coherence protocols such as DeNovo \cite{18} and model and discussed below.

1 is data-race-free, also referred to as the DRF0 consistency sequentially consistent (SC) execution for any program that at the LLC and in program order (normal data accesses are synchronization (also referred to as atomic) accesses execute happens infrequently and at a coarse granularity. Protocols that rely on data-race-freedom and assume synchronization. This scenario presents a third implementation option together, requiring both reads and updates to use synchronization. This scenario presents a third implementation option of push+pull, which is dependent upon the construction of the algorithm.

\textbf{B. Coherence}

GPUs typically use simple, software-driven coherence protocols that rely on data-race-freedom and assume synchronization happens infrequently and at a coarse granularity. We consider a commonly used protocol, referred to as GPU coherence, as follows \cite{18}. At synchronization reads, GPU coherence self-invalidates the entire L1 cache, and at synchronization writes, it invokes write throughs (flushes) of all dirty data to the shared last level cache (LLC). All synchronization (also referred to as atomic) accesses execute at the LLC and in program order (normal data accesses are still performed at the L1). This coherence protocol enables sequentially consistent (SC) execution for any program that is data-race-free, also referred to as the DRF0 consistency model and discussed below.\footnote{Recent systems provide for the heterogeneous-race-free (HRF) \cite{21} consistency model which adds lower-overhead locally scoped synchronization. However, later work \cite{18}, \cite{22} showed that HRF comes at an unnecessary programmability cost since coherence protocols such as DeNovo \cite{18} and the llRc variant \cite{22} support DRF with similar (and sometimes better) efficiency than GPU coherence+HRF and with easier programmability. We therefore do not consider HRF here. We also note that DRFrxx provides similar performance benefits as HRF with GPU coherence, thereby providing representative coverage of the coherence+consistency design space.}

While GPU coherence is simple and performs well for traditional GPU workloads, it can be inefficient for workloads with frequent synchronization. The DeNovo coherence protocol seeks to address these inefficiencies and has been shown to provide high performance for a wide variety of applications in heterogeneous systems \cite{18}, \cite{20}. DeNovo obtains exclusive ownership for written data and atomic accesses. Owned data does not have to be invalidated or flushed at synchronization, and synchronization/atomics for owned locations can execute at the local L1. This significantly reduces the overhead of synchronization accesses and improves reuse of written data and atomic, while still avoiding the overheads of writer-initiated invalidations (as present in standard CPU MESI-style protocols).

However, for workloads where L1 cache utilization or reuse is poor, DeNovo can add overhead relative to GPU coherence by unnecessarily requiring ownership registration and unnecessarily bringing in data for atomic updates into the L1 and replacing other useful data. Thus, there is a workload dependent tradeoff between GPU coherence and DeNovo. In the design dimension of coherence protocols, we consider both GPU and DeNovo coherence.

\textbf{C. Consistency}

Most programming languages (and GPUs) support the data-race-free family of consistency models. DRF0 (data-race-free 0) is the simplest to program of these models, providing sequential consistency (SC) to data-race-free programs. With GPUs, DRF0 incurs data invalidation and flush overhead on all synchronization accesses as described above (only for non-owned data with DeNovo). To partly mitigate this overhead, DRF1 recognizes that some synchronization accesses (distinguished as unpaired synchronization) are never used to order data accesses, and so can be overlapped (reordered) with data accesses \cite{19}, \cite{23}. For such synchronizations, the only overhead is that they need to appear SC relative to other synchronization accesses; therefore, they are executed in program order relative to each other (and at the LLC for GPU coherence). The programmer still gets SC for DRF programs, but the definition of a DRF program is enhanced to accommodate unpaired synchronizations. Thus, DRF1 offers

\begin{figure}[h]
\centering
\begin{lstlisting}
1: procedure PushKernel(V, E_int, E_out, op, vprop, i)
2: for s ∈ V do
3: if spred(s) then
4:     ps ← vprop(s, i)
5: for e ∈ E_out(s) do
6:     t ← dest(e)
7:     if tspred(t) then
8:         atomicUpdate(op, t, p, i + 1)
9:
10:
\end{lstlisting}
\caption{Vertex-centric push and pull kernels with static algorithmic traversal. The spred and tspred functions influence the algorithmic control of the workload. The vprop, update, and atomicUpdate functions influence the algorithmic information of the workload. The iteration variable i is used to track the state of the double-buffered vertex properties between kernel invocations, such that the previous iteration’s values are read-only.}
\end{figure}

\begin{figure}[h]
\centering
\begin{lstlisting}
1: procedure PullKernel(V, E_int, E_out, op, vprop, i)
2: for t ∈ V do
3: if tspred(t) then
4:     pt ← init()
5: for e ∈ E_in(t) do
6:     s ← src(e)
7: if spred(s) then
8:     pt ← vprop(s, t)
9:     pt ← op(pt, ps)
10: update(t, p, i + 1)
\end{lstlisting}
\end{figure}
better performance than DRF0 (by allowing reordering of data accesses relative to unpaired synchronizations), but with slightly more complex programmability.

Finally, data-race-free-relaxed (DRFrlx) \[19\] recognizes that some synchronizations do not need to be ordered even with respect to each other. Thus, DRFrlx potentially improves performance by exploiting intra-thread memory level parallelism (MLP) among such relaxed synchronizations (popularly known as relaxed atomics). While several GPUs support relaxed atomics, they are known to be hard to reason about and not all systems provide efficient support for them \[18\].

In the memory consistency models design dimension, we study DRF0, DRF1 and DRFrlx.

III. TAXONOMY FOR GRAPH ANALYTICS

In this section, we describe workload properties that determine the computation performed by each workload, and subsequently, the required communication. These properties form the taxonomy used by our work in the context of traditional vertex-centric graph analytics applications. For our taxonomy, we first define each \textit{workload} as an input graph and algorithm pair. We then describe two salient features of graph workloads affecting communication: \textit{graph structure}, and \textit{algorithmic properties}.

A. Graph Structure

Graph structure is the connectivity of the input graph and influences both the working-set size and the data access patterns of a workload. In addition to the effect of algorithmic properties, the overall amount of communication performed by a workload depends on graph size, vertex connectivity, and the degree distribution across vertices. Thus, we highlight three primary components of graph structure that influence communication: \textit{volume}, \textit{reuse}, and \textit{imbalance}.

1) Volume: The volume of data that is accessed is considered the working set size of the application, and is thus a function of the vertices and edges in the graph. For some algorithms, auxiliary structures which scale with the number of vertices and edges add to the size of the working set (e.g., a color array for graph coloring). Although volume can also depend on the frontier size of a given iteration, the frontier size is dependent on dynamic behavior of the workload, which is difficult to compute statically.

As a \textit{proxy} for the working set size of a core, we compute the volume per core as an average distribution of the graph over all cores:

\[
Volume(G) = \frac{|V(G)| + |E(G)|}{|SM|}.
\]  

In Equation 1, \( G \) is the input graph, \( V \) and \( E \) are the vertex and edge sets respectively, and \( |SM| \) is the number of GPU cores available. The \textit{Volume} metric thus gives a value proportional to the average working set size to be touched by each GPU core. To anticipate whether this volume is high or low, we compare the volume of data to the available L1 and L2 resources that can be dedicated to each core during full utilization of the GPU. If the volume can roughly fit in each core’s dedicated L1 data cache, then the volume is low. If the volume can fit within a core’s allocation of the L2 cache (assuming an even partitioning across cores), then the volume is medium. Otherwise, the volume is high.

These three discretized values of volume act as inputs to our specialization model (Section IV).

2) Reuse: To drive our specialization model, we need to anticipate how much intra-thread-block data reuse can be exploited in our graph workloads based on vertex connectivity. Figure 2 depicts connectivity attributes we use that describe the potential for reuse. Our heuristics assume directed, symmetric graphs to match the universal input format we have for our workloads; however, they could be extended to express reuse for directed, non-symmetric graphs.

Figure 2a depicts the simplest case where neighbors in the graph are in the same thread block (\textit{local neighbors}, see Equation 4). Such vertices are scheduled concurrently (by thread block), and may exploit data reuse on reads and updates...
We make no assumptions about the ordering of our graphs (i.e., we do not assume a highest degree vertex ordering) so this computation must be performed for all warps. The computed value of imbalance is provided as an input to our specialization model (Section IV).

B. Algorithmic Properties

We analyze these properties of graph applications to anticipate the algorithmic influence on data access patterns, and thus use them for specialization of communication. We identify three salient components of algorithmic properties in this regard: algorithmic traversal, algorithmic control, and algorithmic information. After introducing these components in this section, we describe how we model them for use for specialization in Section IV.

1) Algorithmic Traversal: Algorithmic traversal is the pattern in which each work item propagates changes through the input graph; i.e., algorithmic traversal describes where in the graph information is propagated. An algorithm’s traversal can be either static or dynamic.

A static traversal is one in which the connectivity of the input graph is directly used to define the source and target nodes. That is, in a static traversal, the source and target nodes of an update are always neighbors in the input graph.

In algorithms with a dynamic traversal, the source and target nodes are data-dependent and dynamically computed such that they may not be neighboring nodes in the input graph. An example of dynamic traversal is when updates propagate over the edges defined by the transitive closure of the input graph; i.e., edges that are not present in the source graph.

We analyze each application to determine its traversal type, static or dynamic, and use it in our specialization model (IV).

2) Algorithmic Control: Algorithmic control is the control flow that dictates whether information is propagated or not. For vertex-centric algorithms, control flow is affected when the algorithm necessitates that information should only be propagated for a vertices in the active set of the graph; i.e., the frontier [3]. Algorithmic control manifests in code as predicates that are functions of properties of the vertices on an edge.

Figure 1 shows pseudocode for both a push and pull graph kernel, with predicates for source and target vertices denoted by spred and tpred, respectively. The position of each predicate in the control flow changes from the outer loop (line 3) to the inner loop (line 7), or vice versa, when the algorithm is changed between push and pull, respectively. Therefore, based on whether the implementation is push or pull, and if one predicate is more likely to be true than the other, more updates and their computations can be elided in the outer loop.

Therefore, algorithmic control is specified as source if push elides more computations and updates, target if pull elides more computations and updates, and symmetric if both push and pull elide an equal amount of work. The value that algorithmic control takes on for a particular application is used by our specialization model (Section IV).

Finally, there are some algorithms which perform both racy push and pull updates in the same dynamic traversal (see Section III-B1). These algorithms do not have a design space
which can leverage asymmetry in algorithmic control between push and pull implementations.

3) Algorithmic Information: Algorithmic information is the data that is used to compute control flow and the updated value of a vertex; i.e., algorithmic information describes what information is propagated, and influences the working set of the workload. In Figure 1, algorithmic information is shown as accesses to source vertex properties through the function vprop, and implicitly for the target vertex properties through the functions update and atomicUpdate.

As with control, the position of each property access changes from the outer loop to the inner loop, or vice versa, between push and pull algorithms, respectively. As a consequence, an algorithm that performs either push or pull may have better expected performance due to hoisting redundant data accesses and computations into the outer loop.

Therefore, algorithmic information is specified as source if push hoists more computations and updates, target if pull hoists more computations and updates, and symmetric if both push and pull hoist an equal amount of work. The value that algorithmic information takes on for a particular application is used by our specialization model (Section IV).

Finally, algorithms which perform both racy push and pull updates in the same traversal (see Section III-B1) cannot leverage asymmetry in information between push and pull implementations, because both pull and push updates are present throughout the loop body.

IV. WORKLOAD-DRIVEN SPECIALIZATION

This section introduces a model that establishes how to specialize the update-propagation of the algorithm and the coherence and consistency of the memory system based on the application and input-dependent features introduced in our taxonomy (see Section III).

A. Full Design Space Optimization

This section elaborates on how and why our taxonomy properties described in Sections III-A and III-B interact with each other. Figure 4 contains a decision tree that streamlines these choices resulting in a well-optimized configuration.

1) Push and Pull: As stated in Sections III-B2 and III-B3, both algorithmic control and algorithmic information make decisions with respect to actions on either the source or target. Eliding work or hoisting loads at source is sufficient for recommending a push algorithm, regardless of what the input graph is. However, eliding work or hoisting loads at the target to recommend a pull algorithm is not sufficient. This raises the question, why is push more preferred over pull? Simply, a push algorithm makes dense reads (on the critical path) and then issues sparse writes (off the critical path). In a pull algorithm, there are blocking sparse reads. These are likely to not perform as well as a push algorithm unless the input has particular properties.

Even with considering a pull implementation, it is sufficient for the input graph to have medium or low reuse, or medium or high imbalance, or high volume to favor a push implementation instead. If the input does not maximize data reuse there is limited benefit to bringing it into the local cache, mitigating one of the main reasons to select pull. Similarly, a high volume input will hinder any possible reuse by thrashing the cache. A medium or high imbalance value signals that push performance can be improved by allowing data and/or atomic reordering with respect to atomics. This choice (DRF1 vs. DRFRlx) will be discussed further in Section IV-A3, but is sufficient for us to recommend push.

If the criteria is met to recommend a pull configuration, we pair it with GPU coherence and DRF0. The non-atomic reads and updates of a pull implementation interface well with GPU coherence (as described in Section II-C). Similarly, non-atomic reads and updates mean there is no need for atomic relaxation and DRF0 will perform just as well.

2) Coherence: Assuming a push implementation was selected, the next design space dimension to select is coherence. If the graph input has medium or low reuse, or high volume, we recommend GPU coherence. Given a push implementation, the key difference between DeNovo and GPU coherence is that DeNovo performs owned (i.e., L1) atomics. If there is medium or low reuse, there is little anticipated benefit to bringing data into the L1 for atomics. Similarly, no matter how much reuse we observe, if there is high volume we are unlikely to be able to leverage it as we anticipate cache thrashing. If neither of these conditions are met, we can expect that DeNovo will have a performance benefit.

3) Consistency: Regardless of the coherence protocol selected, we must reason about the optimal consistency model. It is sufficient for the input graph to have high imbalance, or high or medium volume to recommend DRFRlx. A high imbalance characteristic means that we have several long-running warps that are underutilizing GPU hardware and increasing application run-time. Given our imbalance metric (described in Section III-A3) and that at this point in the model-flow we know we are utilizing a push implementation, we know there are atomics proportional to vertex degree that need to be processed. Using DRFRlx we can utilize MLP and overlap these atomics, improving the performance of imbalanced threads and increasing the overall performance and hardware utilization of the workload. With high or medium volume we anticipate that cache thrashing will increase the number of outstanding atomics, which would be similarly susceptible to the MLP improvements provided by DRFRlx. Without either of these characteristics we conservatively recommend DRF1, saving the programmer the effort of reasoning about relaxed atomics.

4) Algorithmic Traversal: The model as described above is predicated on the decision that AT is static. If AT is dynamic, by definition we cannot chose a push or pull implementation as traversal is determined at run-time via synchronization accesses, so instead we describe this as a dynamic push+pull implementation. For dynamic traversal workloads, the amount
of racy accesses over the lifetime of the workload change over time. Some of these algorithms have a traversal which constricts the number of possible racing accesses over time. In these scenarios, we can anticipate that a reduction in likelihood of racy accesses competing for the same data. This paired with a reduction in data volume leads us to anticipate data reuse. Therefore, we specialize for reuse by using DeNovo coherence, allowing racy accesses to receive ownership at the L1.

Other dynamic traversal algorithms can exist where the number of racy accesses to the same data does not constrict. We argue that in such a case DeNovo is still preferable. As the dataset converges, each atomic access bringing data into the L1 will serve an increasing number of requests from threads in that SM. We believe that this more than offsets the cost of ping-ponging. This is compared to GPU coherence which will serialize requests at the L2. L2 atomic requests to the same address must be serialized to account for ordering requirements; there is no distinction made between atomic requests from the same thread or different different threads within a warp as it would be infeasible to include something like threadID in the MSHR \(^2\).

As mentioned, dynamic traversal workloads require extensive use of fine-grained synchronization. Moreover, these algorithms require the values returned by these racy accesses in order to determine the traversal’s control flow. Since the values for these racy accesses are being read, diligent reasoning by the programmer should be used to determine whether these racy accesses can be relaxed using DRFRlx according to the specification described in [19]. Additionally, a consequence of reading the values returned by racy accesses for control flow is that a thread must wait for the values to proceed computation, limiting the impact of atomic relaxation on performance. Therefore, specialize for a consistency model that offers ease of programmability (DRF1) without considerable loss in performance.

B. Partial Design Space Optimization

The model described above is not sufficient to reason about the optimal design given design space restrictions. Namely, if DRFRlx is not available on the target GPU, the design choice between push and pull becomes more complicated. If DRFRlx is not available, there is naturally no longer a choice in the consistency dimension. Furthermore, we always recommend GPU coherence if pull is selected, and the coherence decision is made independently of the consistency decision. It follows that the only decision to be reconsidered is when to push or pull.

Similar to the full model, if AC elides more work at source we opt for a push implementation. Because the amount of loads that can be hoisted via AI is generally less than the

\(^2\)Such a distinction is not needed when working with in-order networks, but that solution will not scale as GPUs increase core-counts, and is therefore not modeled in our simulator as a result.

V. METHODOLOGY

A. Graph Inputs

We select six representative input graphs from the SuiteSparse matrix collection [24] with a variety of connectivity features. Where applicable, each graph has been slightly modified to remove self-edges, and has been converted to a directed, symmetric graph to support push and pull kernels using the same input. Table II lists the name, number of vertices and edges, and other basic properties of these graphs.

For each graph, we compute the volume, reuse, and imbalance metrics described in Sections III-A1, III-A2 and III-A3, as shown in Table II. For each graph, the graph structure profile is subsequently used in our workload-driven methodology to predict the optimal design to specialize to for a given workload.

The various thresholds we choose are: (a) low volume - less than 1.5 times the L1 data cache size, high volume - greater than the L2 cache size divided by the number of GPU SMs, (b) low reuse - less than 0.15, high reuse - larger than 0.40 (for the Reuse formula), (c) low imbalance - less than 0.05, high imbalance - larger than 0.25 (for the Imbalance metric) and (d) k-means clustering threshold (Section III-A3) for the max degree centroid differential is 10. These thresholds were
TABLE II: Input graph statistics and their taxonomy classifications. H indicates a high value, M for medium, and L for low. Blue and red classifications indicated favorable and negative characteristics respectively.

| Graph | Vertices | Edges | Max Deg | Avg Deg | Std Dev | Def | Volume (KB) | AN_L | AN_H | Reuse | Imbalance |
|-------|----------|-------|---------|---------|---------|-----|-------------|------|------|--------|-----------|
| AMZ   | 410236   | 671368 | 2770    | 16.265  | 16.298  | 1855.178 (H) | 2.616 | 13.749 | 0.160 (M) | 0.000 (L) |
| DCT   | 52652    | 178076 | 38      | 3.382   | 4.475   | 60.078 (M) | 1.215 | 2.167 | 0.359 (M) | 0.083 (M) |
| EML   | 265214   | 837912 | 7636    | 3.159   | 42.490  | 287.272 (H) | 0.167 | 2.992 | 0.053 (L) | 1.000 (H) |
| OLS   | 88263    | 683186 | 10      | 7.740   | 2.411   | 200.898 (M) | 3.446 | 4.295 | 0.445 (H) | 0.000 (L) |
| RAJ   | 410236   | 163178 | 3469    | 7.906   | 32.954  | 47.869 (L) | 4.697 | 3.209 | 0.594 (H) | 0.617 (H) |
| WNG   | 61032    | 243088 | 4       | 3.919   | 0.278   | 79.458 (M) | 0.020 | 3.899 | 0.594 (L) | 0.000 (L) |

TABLE III: Algorithmic properties for each application. The ‘—’ markers for the CC application indicate where properties are dependent on the dynamic behavior of the workload, and thus not used for specialization.

| App | Traversal | Control | Information |
|-----|-----------|---------|-------------|
| PR  | Static    | Symmetric | Source      |
| SSSP| Static    | Source   | Source      |
| MIS | Static    | Symmetric | Symmetric   |
| CLR | Static    | Symmetric | Target      |
| BC  | Static    | Source   | Symmetric   |
| CC  | Dynamic   | —        | —           |

TABLE IV: Simulated heterogeneous system parameters.

| CPU Parameters |
|----------------|
| Frequency: 2 GHz |
| Cores: 1 |

| GPU Parameters |
|----------------|
| Frequency: 700 MHz |
| CUs: 15 |

| Memory Hierarchy Parameters |
|-----------------------------|
| L1 Size (8 banks, 8-way assoc.) | 32 KB |
| L2 Size (16 banks, NUCA) | 4 MB |
| Store Buffer Size | 128 entries |
| L1 MSHRs | 128 entries |
| L1 hit latency | 1 cycle |
| Remote L1 hit latency | 35–83 cycles |
| L2 hit latency | 29–61 cycles |
| Memory latency | 197–261 cycles |

We evaluate six applications (for each of the graph inputs from the previous section). Five of them are adapted from the Pannotia benchmark suite [25] and exhibit a wide range of algorithmic control and information. These are PageRank (PR), Single-Source Shortest Path (SSSP), Maximal Independent Set (MIS), Graph Coloring (CLR), and Betweenness Centrality (BC). We have developed new implementations where either a push or pull version of the application did not exist. Furthermore, we have modified the kernels by unrolling inner loops and inlining hand-written assembly code to show the benefits of relaxing the ordering of atomic operations within a thread [19]. A sixth application, Connected Components (CC), is adapted from [26] to represent the design space for workloads with dynamic algorithmic traversal. We find that these applications are similar to those found in contemporary works on graph processing and irregular memory accesses on GPUs [27], [28]. The algorithmic properties described in Section III, used to characterize each application, are summarized in Table III; their values having been determined by manual inspection of application code.

C. Simulation Infrastructure

We simulate a tightly-integrated, coherent CPU-GPU system using the same simulator as prior work, obtained from the authors [19]. This simulator uses GEMS [29] to model a coherent memory system, Garnet [30] to model a 4x4 mesh network, Simics [31] to model the CPU, and GPGPU-Sim [32] to model the GPU. This work must be simulated (as opposed to studied on a real machine) since there are no means to change the coherence and memory consistency of conventional CPU-GPU systems to capture the design space range covered here. Each core has a private L1 cache, and all cores shared a banked L2 cache. We summarize the key hardware parameters in Table IV.

We measure the execution time of each graph workload using a stall classification methodology similar to that described by Alsop et al. [33]. Busy represents time spent doing useful work (cycles where 1 or more instructions were able to issue). Comp represents time spent waiting for an occupied computation unit or the result of a computation. Data represents time spent waiting for an occupied LD/ST unit, or waiting for the result of a non-atomic memory operation. Sync represents time spent waiting for the result of an atomic memory operation, or waiting at a thread barrier. Idle represents idle time spent by a GPU core as it waits for other cores to complete a kernel.

D. Configurations

We evaluate each workload across the full suite of possible optimizations. In each configuration, from left to right: T and S denote Target and Source updates, respectively, in static traversal, and D denotes Dynamic traversal; G and D denote GPU and DeNovo coherence, respectively; 0, 1, and R denote DRF0, DRF1, and DRFrlx, respectively.

VI. Evaluation

Figure 5 shows the results for the 6 graph applications with 6 inputs per application. For all but the CC application,
Fig. 5: GPU execution time breakdown for six different graph applications, each with six different input graphs. All bars of a particular input are normalized to the leftmost configuration — DG1 for CC, TG0 for all other applications. Each application also has two bars shown for the geometric mean performance of designs across inputs: BEST for empirically found optimal designs, and PRED for designs predicted by our methodology. In each configuration, from left to right: T and S denote Target and Source updates, respectively, in static traversal, and D denotes Dynamic traversal; G and D denote GPU and DeNovo coherence, respectively; 0, 1, and R denote DRF0, DRF1, and DRFrlx, respectively.

for each input, we show execution times for 5 design configurations, normalized to the Pull configuration, TG0
TABLE V: Each entry in the table is the design predicted as best by our model for a given workload (the column gives the algorithm and the row gives the input). The entries in gray are mispredicted but perform within 3.5% of the actual best design.

|        | PR  | SSSP | MIS  | CLR  | BC   | CC   |
|--------|-----|------|------|------|------|------|
| AMZ    | SGR | SGR  | SGR  | SGR  | SGR  | DDR1 |
| DCT    | SGR | SGR  | SGR  | SGR  | SGR  | DDR1 |
| EML    | SGR | SGR  | SGR  | SGR  | SGR  | DDR1 |
| OLS    | SDR | SDR  | TG0  | TG0  | SDR  | DDR1 |
| RAJ    | SDR | SDR  | SDR  | SDR  | SDR  | DDR1 |
| WNG    | SGR | SGR  | SGR  | SGR  | SGR  | DDR1 |

Fig. 6: Normalized execution time comparison of SGR (DGR where applicable) to the empirical best and predicted designs (for target, GPU, and DRF0). Since Pull does not use fine-grained atomicism, it does not show performance variation with the consistency models or coherence protocols. We therefore show only one Pull configuration (the simplest one, TG0).

Our results have three key takeaways.

Need for flexibility – **one size does not fit all**: A primary takeaway from our results is that there is no single hardware/software configuration that works best for all workloads. While SGR works best for many of these workloads, there are 12 cases where it does not, summarized in Figure 6. In these cases we see that relative to SGR, the best configuration reduces execution time ranging from 7% to 87%, averaging a 44% reduction. Also note that while we say BEST for clarity, the best configuration varies workload to workload.

These results motivate the need for flexible hardware mechanisms that support flexible coherence and consistency models. Recent work such as Spandex [20] that shows how to efficiently integrate different coherence protocols in heterogeneous systems provides a path to such flexibility while preserving the simplicity and efficiency desired by such systems.

The model is accurate: Another key takeaway is that our predictive model (as described in Section IV-A) accurately predicts the optimal HW/SW configuration in 28 out of 36 workloads. All 8 mispredictions perform within 3.5% of the empirical best, and average 1.3% difference. Five of these workloads ((AMZ,CC), (DCT,CC), (EML,CC), (OLS,CC), (RAJ,CC)) had predictions that were expected to be sub-optimal and chosen to relieve burden on the programmer in exchange for a minimal reduction of performance (average 1.3%) as described in our model. The other three workloads ((EML,SSSP), (OLS,BC), (WNG,SSSP)) mispredict as the result of known limitations of our metrics. We will consider (EML,SSSP) as an example, but similar reasoning can be applied to the other workloads as well.

EML is a graph that is categorized as high volume, low reuse, and high imbalance. SSSP is an application that elides more work at source and hoists more information at source.

Following our decision flow, the optimal configuration for this should be SGR; however, empirically, the optimal is SG1 (albeit with a very small difference from SGR). The reason for the (small) difference is that we are limited by our static metrics. The static volume and imbalance calculations do not consider the run time affects the application will have on these attributes. The first kernel of SSSP is a breadth first search. EML’s power-law distribution of edges means the working set size (approximated by our volume calculation) is actually quite small, despite the large size of the graph. Similarly, if one of the high degree nodes is not on the frontier, the imbalance for this workload will be quite low. A decision flow similar to our model that used runtime information could consider this and choose the correct configuration.

Inter-dependent design dimensions: Finally, the results show that the design dimensions considered in this work are inter-dependent. For example, consider MIS and RAJ. If the system does not support DRFrlx, then the best configuration is Pull (TG0). If the system supports DRFrlx, then the best configuration is Push with SDR. This shows that the decision of Pull vs. Push cannot be made independent of the knowledge of the consistency model supported by the system. Overall, there are seven workloads where without efficient support for DRFrlx, we would recommend a pull implementation over a push one. Applying the extension of the model to the partial design space (Section IV-B), we find that we are able to accurately predict these decisions for four of the seven cases. For the other three cases, we need finer grain distinctions in the volume and AI input parameters – we omit these extensions here for lack of space.

VII. RELATED WORK

A. Graph Analytics Frameworks

There exist many programmable frameworks for implementing graph analytics workloads [2], [3], [4], [5], [6], [7],
works identify that existing systems perform poorly for graph analytics applications on the processing sub-systems, including data structure representations, scheduling and compute-to-data mapping, structural transformations of data, and data access type annotations to improve locality and performance and to reduce communication overheads. However, there are several limitations of these works as they relate to the design space explored in our work. Most of the works on graph processing frameworks focus on CMP systems using commodity hardware, some focusing on distributed systems, while others on shared memory. Our work explores the implications of future heterogeneous systems with unified, coherent shared memory and flexible coherence and consistency. For works that have explored GPU implementations, none have considered GPUs with fully coherent memory systems on a tightly-coupled CPU-GPU system with unified, shared memory. Moreover, none of these works have considered nor characterized the design space of coherence and consistency for GPUs, especially in the context of data-dependent and algorithmic-dependent behavior of graph workloads.

B. Synchronization

As the field of graph analytics develops, more works have explored the implications of racy (push-style) updates and their relationship with synchronization. Many works only consider either push- or pull-style implementations or do not have comprehensive comparison for several algorithms [6], [14]. Some explore both pushing and pulling, and even the idea of choosing the best implementation at runtime as the state of the graph processing progresses [3], [4], [9], [17], but do not consider trade-offs of racy and non-racy updates in the presence of coherence and consistency specialization. Some works identify that existing systems perform poorly for graph analytics workloads due to the fine-grained synchronization overheads using atomic operations [6], [34], [35], [36], [37], but do not consider architectures with efficient coherence and consistency support for atomic operations. Previous works that explore the design space of coherence and consistency for heterogeneous CMPs [18], [20], [22], [38] do not consider how these trade-offs change with respect to pushing and pulling. Finally, works on programmable architectures for graph analytics [39], [40] have more rigid memory systems with little to no fine-grained synchronization support, and do not implement coherence because the accelerators do not operate in a unified, global address space.

C. Input Sensitivity and Concurrency

Several works have explored the relationship of data movement, input sensitivity, and concurrency on the performance of both CPU and GPU systems [5], [17], [41], [42], [43], [44], [45], [46], [47], [48]. However, these works do not consider either the role of the compute-to-data mapping or coherence and consistency on data- and algorithmic-dependent performance scaling. [46] does explore the interplay of coherence and data-dependence, but does not explore consistency models.

VIII. Conclusion

Our taxonimization and evaluation of graph analytics in relation to update propagation, consistency, and coherence has shown that the design space for these workloads leads to non-trivial and inter-dependent design decisions that are input- and algorithm-dependent. The optimal configurations and the performance of each configuration vary widely by workload. Based on our insights, we have proposed a specialization model that accurately predicts the optimal software-hardware configuration in 28 out of 36 workloads, and predicts a configuration that is within 3.5% in the remaining 8 workloads. We also show that we can extend the model to apply our taxonomy to a restricted design space. Using our model, software developers can make hardware-aware design choices and hardware designers can leverage the flexibility and reconfigurability of upcoming memory systems (e.g., [20]) to specialize for diverse irregular graph workloads on configurable processor architectures. Looking forward, we aim to target our analysis to implement runtime methods that leverage flexible memory systems to achieve optimal performance, and to extend our taxonomy to other classes of algorithms and graph datasets.

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