A 190.3-dBC/Hz FoM 16-GHz rotary travelling-wave oscillator with reliable direction control

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This letter presents a rotary travelling-wave oscillator (RTWO) with reliable direction control in a standard 130 nm complementary metal-oxide-semiconductor (CMOS) technology. To achieve low phase noise (PN), and low power consumption, 16-stages customised transmission line segments are designed and simulated on electromagnetic tools. The PN is investigated through modelling the RTWO as multiple standing-wave oscillators. The proposed oscillator achieves 11.2% tuning range, 190.3 dBc/Hz figure-of-merit (FoM) at 1 MHz offset and 192.3 dBc/Hz FoM at 10 MHz offset with 5.8-mW power consumption from 16-GHz carrier.

Introduction: Voltage-controlled oscillators, dominating the noise and power consumption, are the core of phase-locked loop (PLL). Ring oscillators suffer from poor phase noise (PN) and less energy efficient compared to LC oscillators [1] due to the unavoidable noise injection in each stage and charging and discharging process in every clock cycle. Wave-based oscillators recently have gained interest because of its superior PN performance. Rotary travelling-wave oscillators (RTWO) utilising TL to form a Möbius loop naturally provide multiphases with high-resolution rail-to-rail outputs, enabling RTWO to be an excellent potential candidate for beam-forming integrated-circuits (ICs) in 5G modem applications [2]. The RTWO was first presented by Wood [3], where RTWO arrays were utilised in a large chip to generate gigahertz clock. The authors in [4] demonstrated a 15 GHz RTWO in a 0.18 μm process with PN of ~112 dBc/Hz at 1 MHz offset. A design achieved 15 GHz with 182 dBc/Hz FoM in 90 nm CMOS [5]. A more recent work from Shehata et. al. [6] demonstrated a low flicker noise corner RTWO in a 22 nm fully-depleted-silicon-on-Insulator (FDSOI) technology. Mutilphase square-like outputs suggest that RTWO can be employed in an all-digital PLL (ADPLL) to replace the power-hungry component, time-to-digital converter and digitally controlled oscillator (DCO). The deployment of RTWO in ADPLL was discussed in [7] in which a variable look-up table was created to adapt to the undetermined direction of the rotary wave. The authors in [8] proposed a phase-offset technique to force the direction of the wave while the reliability of the direction control scheme was not proved, the same as [9]. Motivated by the need for a power efficient and a reliable direction control RTWO, this letter presents a process-voltage-temperature (PVT) resilience direction control with tunable power consumption while maintaining low PN, achieving 190.3 dBc/Hz FoM.

Circuit topology: The proposed RTWO shown in Figure 1 is composed of a differential TL with a cross-connection to form a Möbius loop, requiring no termination and no matching. Consequently, the limitations on the load impedance mismatch and signal bandwidth are greatly alleviated. Unlike LC oscillator, the signal generated from RTWO not only keeps the fundamental harmonic but also maintains the odd harmonic components. Similar to the basic RTWO, gain stages are implemented by complementary latches, to compensate the loss of the resonator, sharpening the transition of the signal while keeping symmetric waveform to further decrease 1/f noise up-conversion degrading the close-in PN. To achieve multiple phases, low PN and low flicker noise corner frequency, the TL is divided into N segments (N = 16). PN is primarily dominated by the differential TL stages [10]. On the other hand, the increased number of amplifiers affects total power consumption. To balance the power consumption and the PN, two mechanisms are introduced: (i) The amplifiers are inserted at every other TL segments. (ii) The gated pair is tuned through binary-weighted switches. Junction varactors are inserted at every TL segment to widen tuning range. Attributed to the symmetric structure, the rotary wave can propagate to both clockwise (CW) and counterclockwise (CCW) direction. In the proposed design, static inverter-based buffers are intentionally inserted between each TL bank, formed by four consecutive TL segments, to introduce delay such that the travelling wave propagation is intervened by the in-balanced termination impedance of the TL during start-up. The delay is set sufficiently large to overcome PVT variations, thus ensuring robust propagation direction control.

Modeling of RTWO: Coplanar TLs can be modelled as lumped LC ladder assuming no loss from the TL. Considering differential inductance and capacitance per unit length, $L_0$ and $C_0$, the phase velocity of the rotary wave is given by $v_p = \frac{c}{\sqrt{L_0C_0}}$, leading to the free-running frequency as $f_0 = \frac{1}{2\pi c} \sqrt{\frac{1}{L_0C_0}}$, where $N$ is the number of segment of the TL. The factor of 2 accounts for two complete waves travelling around the loop to force one cycle. It is noticed that the total differential inductance and capacitance are $N(L_0 + L_{diff})$ and $N(C_0 + C_{diff})$, respectively [11].

Circuit design: To maximise the quality factor (Q) of the resonator, the top metal with a thickness of 4 μm is used to design the Möbius loop. Negligible sheet resistance benefits the energy stored in the TL. The cross-connections are implemented in metal 7 with 3 μm thickness. To keep inner and outer loops symmetry, metal 7 is also used in corners. The loop is designed and simulated based on electromagnetic tools. A 3-D view is presented in Figure 2(a). The simulated Q-factor and inductance at 16 GHz are shown in Figure 2(b). Several design iterations are required to adjust and optimise TLs spacing and width. Each four
adjacent TL segments are conserved as a TL bank, including two gain stages and four tuning capacitor stages. Direction and power control signals are applied to the TL banks.

Figure 3 shows two TL segments. The length for all transistors herein is selected to be the minimum length. The gain stages control rotation directions and adjust power consumption. The direction control bit ‘dir’ with an enable signal ‘en’, determine the direction of the travelling wave during the start-up. In each of direction control module, either the CW control or the CCW control is delayed by approximately 1 ns through a set of inverters. Combined with 4-bits power control signals, the direction control signal sequentially sets n-channel/p-channel mos transistors. Combined with 4-bits power control signals, the direction control or the CCW control is delayed by approximately 1 ns through a set of inverters.

Figure 4(a) Simulated phase noise (PN) at 16 GHz in five corners, (b) frequency versus $V_{\text{tun}}$ versus power control setting

where $Q = \pi^2 R_p/8L_{\text{0on}}$, and $V_0 = 4/\pi I_D R_p$, attributed to the differential property. $I_D$ is the summation of drain currents with $V_{\text{GS}} = V_{\text{DD}}$, and $V_{\text{DS}} = V_{\text{DD}}/2$.

The noise current injected from differential pairs becomes strongest at which the drain voltage of two NMOS transistors are the same. This results in two strongest noise injection period, that is in every cycle of the clock. In the presence of this periodical noise injection, the thermally induced noise from the differential pair is cyclostationary. Its spectral density is scaled by a ratio of total injection time and the time period.

The total injection time is $4\Delta t$ in one cycle, $T_0$, if each side of the noise conduction time at the zero-crossing point is denoted by $\Delta t$, which is given by $\Delta t = \frac{V_{\text{DD}}}{2 + 0.56/R_p}$, where $T_0$ is the injection time when the differential pair is in equilibrium. Since the current noise of the differential pair is given by $I_N = 4kT \sqrt{\gamma/\Delta t}$, where $g_m = 4kT \gamma$ is the noise coefficient. Assuming $g_m = g_m, \ k = \gamma, \ p = 1/2g_m$, the total noise current is

$$\frac{I_N}{I_D} = \frac{4kT\gamma}{4\pi R_p} \left(\frac{1}{\sqrt{2T_0}}\right).$$

In analogous to Equation (1), PN due to the differential pair is derived as

$$L(\Delta f)_{\text{diff}} = \frac{|g_m|}{2} \left(1 + \frac{\sqrt{2}}{\gamma/\Delta f}\right)^2.$$  

Underestimating $\Delta t$ due to approximating transition smoothly will not affect the PN estimation as injected noise strength is overestimated. Equations (1) and (3) yield the total PN given by

$$L(\Delta f)_{\text{total}} = 4kT R_p \left(1 + \sqrt{\frac{1}{2\gamma}}\right)^2 \left(\frac{f_0}{2\beta \Delta f}\right)^2.$$  

Equation (4) is the total PN in a $\lambda/4$ SWO. The RTWO is modelled as a superposition of multiple $\lambda/2$ SWOs [11]. It is necessary to modify the Q-factor in a $\lambda/4$ SWO by replacing $L$ with $L/4$, resulting in $Q^2 = \pi^2 R_p/2L_{\text{on}}$. The amplitude of RTWO is also reduced by a factor of $2$, giving rise to total noise as

$$L(\Delta f)_{\text{total}} = 2kT R_p \left(1 + \sqrt{\frac{\lambda}{2\gamma}}\right)^2 \left(\frac{f_0}{2Q \Delta f}\right)^2.$$  

Simulation results: The proposed RTWO was implemented in a standard 0.13 $\mu$m CMOS process from a 1.2 V supply. The S-parameter file of the TL segments was extracted in EM tools. The simulated tuning range is from 15.1 to 16.9 GHz. At 1 MHz offset, the maximum power consumption is 5.8 mW with FoM of 190.3 dBc/Hz; the minimum power consumption is 3 mW with FoM of 185.5 dBc/Hz. The PN at 1 MHz offset increases by 7 dB due to the small signal swing at the minimum power setting. Figure 4(a) shows the simulated PNs from 16 GHz carrier with 5.8 mW setting under five corners. The temperature for ‘ss’, ‘ft’, ‘nt’, ‘fs’, and ‘sf’ process corners were set as 120, 0, 27, 0 and 120 degrees, respectively. Figure 4(b) depicts the frequency varying according to the tuning voltage and the power control setting. The most-significant
bit (MSB) of the power setting was set to 1 to keep the minimum current for oscillation. The $1/f^\alpha$ corner frequency is approximated to 400 kHz.

Figure 5 summarises simulated PN versus tuned frequency in process corners when the maximum power setting is set. The difference in PN in two direction propagation is negligible. Figures 5(a) to (c) show the simulated PN at 100, 1 and 10 MHz versus tuned frequency while keeping 5.8 mW power consumption. Figure 5(d) is the FoM at 1 MHz versus tuned frequency.

To verify the direction control, two signals, for example, 157.5 and 168.75 degrees (Figure 1), were measured by the phase difference. For the CW and CCW wave propagation, the ideal phase difference is 11.15 and $-11.15$ degrees, respectively. Monte Carlo simulation, including the process spreading and device mismatch, is shown in Figure 6, demonstrating the robust direction control. The majority is falling into one $\sigma$.

**Conclusion:** An RTWO with reliable direction and power-saving control is proposed. The oscillator is operating at 16 GHz with 11.2% tuning range, drawing power from 5.8 to 3 mW. Table 1 summarises the performance of the proposed RTWO and compares it with previous arts. FoM defined as

$$ \text{FoM} (\Delta f) = -\text{PN} (\Delta f) + 20 \log_{10} \left( \frac{f_0}{\Delta f} \right) - 10 \log_{10} \left( \frac{P_{DC}}{1 \text{ mW}} \right) $$

showing 190.3 and 192.3 dBc/Hz at 1 and 10 MHz offset.

**Table 1. Comparison with state-of-the-art rotary travelling-wave oscillator design**

| References | This work | [6] | [12] | [13] | [14] |
|------------|-----------|-----|-----|-----|-----|
| Technology (nm) | 130 | 22 | 28 | 130 | 28 |
| Supply voltage (V) | 1.2 | 0.8 | 1.3 | 1.2 | – |
| Power (mW) | 5.8 | 21 | 75 | 28.4 | 16.2 |
| Frequency (GHz) | 16.2 | 30 | 19.8 | 2 | 37.7 |
| Tuning (%) | 11.2 | 13.5 | 20.6 | 16 | 12 |
| Phase noise (PN) @ 1 MHz (dBc/Hz) | $-113.7$ | $-107$ | $-101.2$ | $-141$ | – |
| PN @ 10 MHz (dBc/Hz) | $-135.7$ | $-128.1$ | $-131.2$ | $-121.2$ | – |
| FoM @ 1 MHz (dBc/Hz) | 190.3 | 183.5 | 168.4 | 190 | – |
| FoM @ 10 MHz (dBc/Hz) | 192.3 | 184.6 | 178.4 | – | 180.6 |

**Fig 6** Two hundred Monte Carlo simulations for both direction control. (a) Clockwise control, and (b) counterclockwise control

**Acknowledgments:** This work was financially supported by the Natural Science and Engineering Research Council of Canada. Computer-aided design tools were provided by CMC Microsystems, ON, Canada.

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Received: 15 November 2020 Accepted: 7 January 2021
doi: 10.1049/el.12089

**References**

1. Guo, H., et al.: A 0.083-mm$^2$ 25.2-to-29.5 GHz multi-LC-tank class-F234 VCO with a 189.6-dBc/Hz FOM. *IEEE Solid-State Circuits Lett.* 1(4), 86–89 (2018)
2. Kibaroglu, K., Sayginer, M., Rebeiz, G. M.: A low-cost scalable 32-element 28-GHz phased array transceiver for 5G communication links based on a 2×2 beamformer flip-chip unit cell. *IEEE J. Solid-State Circuits.* 53(5), 1260–1274 (2018)
3. Wood, J., Edwards, T. C., Lipa, S.: Rotary traveling-wave oscillator arrays: a new clock technology. *IEEE J. Solid-State Circuits.* 36(11), 1654–1665 (2001)
4. Hsieh, H., Hsu, Y., Lu, L.: A 15/30-GHz dual-band multphase voltage-controlled oscillator in 0.18-μm CMOS. *IEEE Trans. Microwave Theory Tech.* 55(3), 474–483 (2007)
5. Zhang, C., et al.: A 15 GHz, $-182$ dBc/Hz/mW FOM, rotary traveling wave VCO in 90 nm CMOS. *IEEE Microwave Wireless Compon. Lett.* 22(4), 206–208 (2012)
6. Shehata, M. A., Keaveney, M., Staszewski, R. B.: A 184.6-dBc/Hz FoM 100-kHz flicker phase noise corner 30-GHz rotary traveling-wave oscillator using distributed stubs in 22-nm FD-SOI. *IEEE J. Solid-State Circuits Lett.* 2(9), 103–106 (2019)
7. Takinami, K., et al.: A distributed oscillator based all-digital PLL with a 32-phase embedded phase-to-digital converter. *IEEE J. Solid-State Circuits.* 46(11), 2650–2660 (2011)
8. Aidoo, M., et al.: Direction control of wave propagation in rotary traveling wave oscillator (RTWO) using phase offset technique. *SoutheastCon 55,* 1–5 (2017)
9. Zhuo, C., et al.: Modeling, optimization and control of rotary traveling-wave oscillator. In: IEEE/ACM International Conference on Computer-Aided Design, San Jose, California pp. 476–480 (2007)
10. Chen, Y., Pedrotti, K.: Rotary traveling-wave oscillators, analysis and simulation. *IEEE Trans. Circuits Syst. I Regul. Pap.* 58(1), 77–87 (2011)
11. Takinami, K., et al.: Phase-noise analysis in rotary traveling-wave oscillators using simple physical model. *IEEE Trans. Microwave Theory Tech.* 58(6), 1465–1474 (2010)
12. Vigilante, M., Reynaert, P.: A coupled-RTWO-based subharmonic receiver front end for 5G E-band backhaul links in 28-nm bulk CMOS. *IEEE J. Solid-State Circuits.* 53(10), 2927–2938 (2018)
13. Bai, Z., et al.: A 2-GHz pulse injection-locked rotary traveling-wave oscillator, *IEEE Trans. Microwave Theory Tech.* 64(6), 1854–1866 (2016)
14. Galeone, S., et al.: An eight-phase 40GHz RTWO in 28nm CMOS with phase noise reduction via head and tail filtering. In: IEEE International Conference on Electronics, Circuits and Systems (ICECS), Genoa, Italy, pp. 306–309 (2019)