Demystifying the Performance of HPC Scientific Applications on NVM-based Memory Systems

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Abstract—The emergence of high-density byte-addressable non-volatile memory (NVM) is promising to accelerate data- and compute-intensive applications. Current NVM technologies have lower performance than DRAM and, thus, are often paired with DRAM in a heterogeneous main memory. Recently, byte-addressable NVM hardware becomes available. This work provides a timely evaluation of representative HPC applications from the “Seven Dwarfs” on NVM-based main memory. Our results quantify the effectiveness of DRAM-cached-NVM for accelerating HPC applications and enabling large problems beyond the DRAM capacity. On uncached-NVM, HPC applications exhibit three tiers of performance sensitivity, i.e., insensitive, scaled, and bottlenecked. We identify write throttling and concurrency control as the priorities in optimizing applications. We highlight that concurrency change may have a diverging effect on read and write accesses in applications. Based on these findings, we explore two optimization approaches. First, we provide a prediction model that uses datasets from a small set of configurations to estimate performance at various concurrency and data sizes to avoid exhaustive search in the configuration space. Second, we demonstrate that write-aware data placement on uncached-NVM could achieve $2\times$ performance improvement with a 60% reduction in DRAM usage.

Keywords—Non-volatile memory; Optane; heterogeneous memory; persistent memory; byte-addressable NVM; HPC;

I. INTRODUCTION

Byte-addressable non-volatile memories, such as STT-RAM, ReRAM, and PCM [11], [15], [24], [25], are promising to accelerate data- and compute-intensive HPC applications [16]. High-density NVM enables larger memory capacity than DRAM under the same area constraints. Data stored in NVM can persist through power failures as if in storage. Recently, some NVM technologies may even provide comparable bandwidth and latency to that of DRAM, enabling much higher performance than block devices. Altogether, these characteristics start blurring the boundary between memory and storage when NVM is used in the main memory. However, NVM technologies are still under active development and not ready for replacing DRAM. For instance, the write bandwidth of the Intel Optane DC persistent memory is only one third that of DRAM [21]. Consequently, NVM is often paired with DRAM, building a heterogeneous memory system.

The recent release of the Intel Optane DC persistent memory module (named Optane in the rest of the paper) marks the first mass production of byte-addressable NVM. The Optane provides a realistic and accessible hardware platform for evaluating the impact of new main memory designs on HPC scientific applications. The future Exascale system is reported to be based on an NVM technology like Optane [14]. Therefore, the performance of HPC applications on this new hardware requires a timely and comprehensive evaluation. Several works have provided system evaluation and performance of specific applications [9], [12], [21], [32]. Still, the landscape of HPC scientific applications requires a systematic approach to identify bottlenecks and opportunities. Does an NVM-based main memory change the priority in optimization? How to effectively leverage the heterogeneity in DRAM/NVM systems for the best performance? Answering these questions not only helps to exploit NVM on the next generation supercomputers but also influences the design of runtime and system software to accommodate this emerging memory technology.

In this work, we follow the well-known Seven Dwarfs [1] and choose flagship libraries and applications, such as ScALAPACK [4], SuperLU [17], and Hypre [34] to cover the landscape of scientific applications. Our study provides a comprehensive evaluation of the domains of dense and sparse linear algebra, spectral methods, N-body methods, structured and unstructured grids, and Monte Carlo-based algorithms. We find that scientific applications exhibit three tiers of sensitivity on the uncached-NVM, i.e., insensitive, scaled, and bottlenecked. Leveraging DRAM as a cache
to NVM could effectively improve application performance even when the input problems have a memory footprint three to five times the DRAM capacity. Furthermore, we reveal two bottlenecks arising from the asymmetric bandwidth and scaling limitation in NVM, i.e., write-throttling and concurrency contention. These characteristics may change the critical computation phases in applications and, thus, require different priorities in optimization. Also, we identify that concurrency changes have a diverging effect on read and write accesses in applications, which requires different strategies like the write-aware placement. We believe that this work provides insights and feedbacks that are critical for applications to leverage future systems with NVM-based main memory.

We explore two optimization directions. We develop a model to predict application performance in cached-NVM at different concurrency and problem sizes to help design space exploration and identify optimal configurations. On uncached-NVM, we demonstrate in ScaLAPACK that explicitly managing write-aware placement can significantly improve performance and reduce DRAM usage. We summarize our contributions as follows.

• A comprehensive performance study of HPC workloads from common computation domains (the Seven Dwarfs) on cached and uncached NVM-based main memory;
• Highlight that write throttling and concurrency contention change the priority of optimizing computation in scientific applications;
• Identify the diverging effect of concurrency change on read and write in applications, and demonstrate the effectiveness of write-aware data placement;
• Develop a prediction model to estimate performance at various concurrency and data sizes to select optimal configurations.

II. BACKGROUND

In this section, we introduce NVM-based memory systems and the Seven Dwarfs in scientific applications.

A. NVM-based Heterogeneous Memory

Extensive research has proposed using NVM for implementing the main memory to exploit its high density, persistence, and power efficiency [15], [24]. Still, the current NVM technologies have lower performance than DRAM, and thus, main memory designs often pair NVM with DRAM, either as a cache or placed side-by-side to NVM. Previous works mostly use simulations and small problems for evaluation due to the lack of large-scale hardware. Recently, the first mass production of byte-addressable NVM arrives in the format of the Intel Optane DC Persistent Memory Module (PMM). In this work, we use this new hardware to evaluate realistic problems on promising memory designs.

The work of [21] has provided detailed system evaluation, and we briefly summarize the system architecture (Figure 1) in this section. The memory subsystem consists of DRAM DIMMs and NVDIMMs that share integrated memory controllers (iMC). Each NVDIMM has a small internal controller for address translation and a data buffer. The internal data granularity in the Optane media is 256 bytes, while the data granularity between the processor and memory subsystem is 64 bytes. System evaluation has quantified that sequential and random read accesses to NVM have a latency of 174 ns and 304 ns, respectively [21]. Write latency to NVM depends on store instructions and data sizes. For instance, 64- to 256-byte non-temporal data store has 180 – 200 ns latency [12]. On one socket, the read bandwidth to NVM can reach 39 GB/s while the peak write bandwidth is only 13 GB/s [12], [21]. Thus, the NVM exhibits about three times asymmetry in read and write bandwidth.

The NVDIMMs can be configured in Memory or AppDirect mode. In Memory mode, DRAM becomes a hardware-managed direct-mapped write-back cache to NVM and is transparent to applications. Note that DRAM on one socket cannot cache accesses to NVM on another socket [9]. In AppDirect mode, the NVM becomes a byte-addressable persistent memory. A dax-aware file system would transparently convert file read and write operations into 64-byte load and store instructions in this mode to access NVM. Also, in this mode, the NVM on each socket can be exposed as a non-uniform memory access (NUMA) node to the CPUs. Standard NUMA management routines like numactl can be used to control data placement in this configuration.

B. Seven Dwarfs of HPC scientific applications

The work of [1] summarizes seven domains of numerical algorithms in major HPC science and engineering applications, known as “Seven Dwarfs”. For a comprehensive evaluation of the HPC landscape, we select one application from each Dwarf as well as Laghos [7], a proxy application of the BLAST hydrodynamics application, for the experiments. We introduce each Dwarf and application as follows.

• Dense Linear Algebra features dense array data structures. They exhibit strided memory access to all the elements of the data structures. Classic vector and ma-
trix operations fall into this category. We select matrix multiplication (level 3) from ScALAPACK [4] for the experiment.

- **Sparse Linear Algebra** methods store data in compressed formats and access data elements through indirect memory accesses. We choose SuperLU [17] that adopts the BAR method for implementing sparse LU factorization.

- **Spectral Methods** often use fast Fourier transforms (FFT) to solve differential equations. Data permutation in this method often requires matrix transpose. We evaluate the FT benchmark that performs discrete 3D FFT from the NPB [2] suite.

- **N-Body Methods** have a high computation complexity of $O(N^2)$ for simulating a dynamical system of $N$ particles. We use hardware accelerated cosmology code (HACC) [10] that simulates the formation of structure in collisionless fluids under the influence of gravity in an expanding universe.

- **Structured Grids** feature regular grid structures. Stencil operations on the grids often have high spatial locality in data accesses. We choose Hypre [34], a high-performance pre-conditioners library for solving linear systems in our evaluation.

- **Unstructured Grids** feature irregular grid structures. Data accesses and updates often involve multiple levels of memory reference indirection. We use a general block-structured AMR framework, BoxLib [3], for the test.

- **Monte Carlo** methods rely on repeated random data accesses to calculate numerical results. We use XSBench [27], which implements a Monte Carlo neutron transport algorithm, as a representative of such workloads.

### III. METHODOLOGY

In this section, we describe the experimental setup, benchmarks, and methodologies. We use the Intel Purley platform that consists of two 2nd Gen Intel® Xeon® Scalable processors as the testbed. The memory subsystem consists of four iMacs, 12 memory channels, a total of 192 GB DRAM (12 DIMMs), and 1.5 TB NVM (12 NVDIMMs). The memory channels run at 2400 GT/s, supporting 230.4 GB/s peak system bandwidth. We override the EFI memory map to expose NVM on each socket as a separate NUMA node. The configuration of the system is summarized in Table I.

The platform runs the Fedora 29 operating system with GNU/Linux 5.1.0. When the Optane DC PPM is configured in AppDirect mode and exposed as NUMA nodes, we use `numactl` to control the data placement onto different memories. Table II summarizes the applications and their input problems. Table II summarizes the applications and their input problems. Table II summarizes the applications and their input problems. Table II summarizes the applications and their input problems. We compile all applications with GCC 8.3.1. For each application, we report the application-defined figure of merit (FoM) if available. Otherwise, we report the run time of the main computation kernels.

We develop profiling routines that sample memory bandwidth on each NVDIMM and DRAM DIMM. We use the Intel Processor Counter Monitor (PCM) tool [26] to monitor hardware counters to collect core activities and offcore events. The profiling routines are integrated into applications to exclude the initialization and finalization stages. We only report the profiling results of the main computation phases. When the Optane is configured in Memory mode, we report the memory traffic as measured to DRAM DIMMs because it is accessed before NVDIMMs. When the Optane is in AppDirect mode, we report the memory traffic as the sum of traffic to NVDIMMs and DRAM DIMMs.

### IV. PERFORMANCE ANALYSIS

This section evaluates the impact of NVM-based main memory on HPC scientific applications from three aspects – (1) the performance sensitivity in cached-and uncached-NVM (2) the write throttling effect on critical phases (3) the diverging effect of concurrency changes on read and write accesses. We also quantify the performance impact of checkpointing on NVM.

#### A. Overall Performance

We start the evaluation with an overview of the performance sensitivity of HPC applications on two NVM-based main memory, i.e., cached and uncached. All the experiments use the local socket to eliminate the severe NUMA effects reported in [9], [12], [21]. Input problems have a memory footprint fit in DRAM capacity (50%-85%) so that we can use the performance on DRAM-only main memory as the reference. Figure 2 reports application performance on DRAM-only, cached-NVM, and uncached-NVM main memory. Note that SuperLU, XSBench, and FFT use application-defined metrics, i.e., the higher, the better, while the other applications report the run time, i.e., the lower, the better.

### Table I: Platform Specifications

| Processor       | 2nd Gen Intel® Xeon® Scalable processor |
|-----------------|----------------------------------------|
| Cores           | 2.4 GHz (3.9 GHz Turbo frequency × 24 cores (48 HT) × 2 sockets |
| L1-dcache       | private, 32 KB, 8-way set associative, write-back |
| L1-icache       | private, 32 KB, 8-way set associative, write-back |
| L2-cache        | private, 1MB, 16-way set associative, write-back |
| L3-Cache        | shared, 32 MB, 11-way set associative, non-inclusive write-back |
| DRAM            | six 16-GB DDR4 DIMMs × 2 sockets |
| NVM             | six 128-GB Optane DC NVDIMMs × 2 sockets |
| Interconnect    | Intel® UPI at 10.4 GT/s, 10.4GT/s, and 9.6 GT/s |

### Table II: Evaluated benchmarks.

| Benchmark  | Input Problems                                      |
|------------|-----------------------------------------------------|
| Hypre [34] | a 3D electromagnetic diffusion problem              |
| Laghos [7] | the Sedov blast wave Q3-Q2 3D computation            |
| ScALAPACK [4] | the distributed matrix multiplication of dimension NxN |
| NPB [2] - FT | a discrete 3D fast Fourier Transform of class D       |
| HACC [10]  | a 252 simulation box using 384 grids in CORAL benchmark suite |
| BoxLib (AMReX) [3] | the spherical chemical wave propagation |
| XSBench [27] | the unorganized grid of XL problem with 34 million lookups |
| SuperLU [17] | a distributed PGDSSVX routine with real datasets from [6] |
Table III: An overall characterization of application sensitivity to the uncached-NVM. The last column indicates the performance compared to that on DRAM. Highlighted cells classify applications into three tiers.

| N-body          | Application | Memory BW (MB/s) | Read BW (MB/s) | Write BW (MB/s) | Write Ratio(%) | Slowdown(x) |
|-----------------|-------------|------------------|----------------|-----------------|----------------|--------------|
| Structured Grid | XSBench     | 4,135            | 3,114          | 1,021           | 25             | 1.27         |
| Dense Linear Algebra | Scalapack   | 11,984           | 10,104         | 1,880           | 16             | 2.99         |
| Monte Carlo     | XSBench     | 16,134           | 16,130         | 4               | 0              | 4.16         |
| Structured Grid | Hypre       | 11,413           | 10,519         | 894             | 8              | 4.67         |
| Sparse Linear Algebra | SuperLU    | 8,342            | 6,208          | 2,134           | 25             | 4.94         |
| Unstructured Grids | BoxLib      | 10,336           | 8,248          | 2,088           | 21             | 8.94         |
| Spectral Methods | FFT         | 5,983            | 3,633          | 2,350           | 39             | 14.92        |

All applications on the cached-NVM manage to achieve performance comparable to that on the DRAM. The performance gap between DRAM and the cached-NVM is less than 10% except for ScaLAPACK, Hyre, and BoxLib. These three applications have more performance loss, with a maximum loss of 28% in Hypre (to be analyzed in Section IV-B). Note that cached-NVM requires no porting efforts from the application developer, which would likely be the first deployment choice.

On the uncached NVM, applications exhibit three tiers of performance sensitivity, i.e., insensitive, scaled, and bottlenecked performance compared to the DRAM baseline. We report the profiling results of average memory traffic, in read and write, respectively, in Table III. In the first tier, HACC and Laghos show little performance change when the main memory changes from DRAM-based to NVM-based. The performance loss is much lower than the latency and bandwidth difference between NVMe and DRAM. This class of applications features low memory bandwidth (in green). Scientific applications that share similar computations as HACC (N-body) and Laghos (unstructured finite element) may sustain performance when directly ported to systems with NVM-based main memory.

Four applications (in gray cells) exhibit scaled performance on the uncached NVM, as compared to their DRAM baseline. These applications exhibit 2.99 to 4.94 times slowdown, which approximates the three times performance gap between DRAM and NVM, as benchmarked on the testbed [21]. ScaLAPACK, XSBench, and Hypre have a high memory bandwidth but a low write ratio. The total memory bandwidth ranges between 11 and 16 GB/s while their write accesses only take up 0.03% to 16% total memory traffic. SuperLU falls between the scaled and bottlenecked tier because its main computation phase, “factor”, consists of two dramatically different stages. The first phase slows down more than ten times, but the second phase has no performance loss. Section IV-C provides in-depth analysis.

The third tier of performance sensitivity, including BoxLib and FFT, shows a severe performance bottleneck on the uncached NVM. They slow down more than the performance gap between DRAM and NVM. This group of applications has a total memory bandwidth lower than applications in the second tier but high write traffic. In particular, their memory traffic has read/write ratios as low as 1.5 so that the write traffic could even reach 36% total memory traffic. We notice that the hardware supports up to 12 GB/s write bandwidth on the testbed, indicating that bandwidth saturation is not the cause of the bottleneck. We identify the write throttling effect and concurrency contention as the primary causes of the slowdown in Section IV-D.

**Insight I:** N-body and structured grids applications may have negligible performance loss on NVM-based main memory.

B. Cache Efficiency

We use two metrics to quantify the effectiveness of using DRAM as a cached to NVM. First, for input problems with memory footprint smaller than the DRAM capacity, we define cache efficiency as the relative performance to that on DRAM directly. The expectation is that low hardware overhead for managing DRAM as a cache should bring...
the performance to match using DRAM natively. Second, when the input problems require memory size larger than the DRAM capacity, we defined cached speedup as the performance improvement from non-cached NVM. The expectation is that the cached-NVM can enable larger problems than DRAM and also higher performance than uncached-NVM.

Overall, the cached NVM delivers high cache efficiency. Hypre is the application with the most performance loss in the cached-NVM, i.e., 28%. We identify the cause by collecting samples of read and write traffic throughout the execution. In the cached-NVM, DRAM acts as the last level cache before the NVM main memory. Thus, we collect traffic to both DRAM and NVM. In DRAM-only main memory, we only collect traffic to DRAM DIMMs. Figure 4 reports the reconstructed trace of memory traffic. We notice that the 59.5 GB/s read bandwidth in cached-NVM (green line) is precisely 28% reduction of the 82.5 GB/s read bandwidth in DRAM (blue line). Since Hypre is a read-dominant workload, the read bandwidth directly affects the performance. Interestingly, the write bandwidth in cached-NVM (yellow line) reaches 9.3 GB/s, which is significantly higher than the 5.7 GB/s write bandwidth in DRAM (orange line). We attribute this increased write traffic to DRAM cache to the cache line replacement, i.e., load misses in the DRAM cache need to read from NVM (black line) and then save data into the DRAM cache.

We scale up the input problems in three MPI applications, i.e., SuperLU, BoxLib, and Hypre, which typically require multiple compute nodes on supercomputers for realistic simulations. For SuperLU, we use five real datasets (kim2, offshore, Ge87H76, nlplkt80, and nlplkt120) from [6]. The largest input requires 490 GB memory. For BoxLib and Hypre, we scale up their simulation domains to reach 300 GB memory footprint. Figure 3 reports the performance on the cached-NVM. SuperLU sustains similar performance (factor mflops) even when the input problems scale up to five times DRAM capacity. When BoxLib and Hypre have the memory footprint 4.4 and 2.9 times the DRAM capacity, the cached-NVM still manages to double the performance compared to the uncached-NVM.

Insight II: sparse linear algebra and structured/unstructured grids applications can benefit from the cached-NVM to enable substantially large problems at reasonable performance.

C. Write Throttling

Uncached-NVM exposes the characteristics of NVM directly to the application without interference from the DRAM cache. We analyze application performance in this mode to provide feedback and insights for future NVM-based designs. Asymmetric read and write performance is a common characteristic of NVM technologies. For instance, the testbed in this study has 39 GB/s read bandwidth and 13 GB/s write bandwidth [21]. Our analysis reveals a write-throttling effect that could change the critical computation phase of an HPC application when moved from DRAM-based to NVM-based main memory.

SuperLU and Laghos both have two distinct phases in the execution, as shown in the trace of memory traffic in Figure 5. These phases, however, exhibit different sensitivity to the write throttling effect. The first phase in Laghos always takes about 20% the execution time when running on DRAM (Figure 5a) and uncached-NVM (Figure 5b). In contrast, on DRAM, the first phase in SuperLU only takes 20% the execution time (Figure 5c), but significantly extends to 70% execution time on uncached-NVM (Figure 5d).
We find that there exists a threshold value of the write bandwidth (2 GB/s on the testbed), above which a computation phase will significantly prolong the execution. For instance, the first phase in Laghos has a moving average of 1.3 GB/s write bandwidth with its peak remaining lower than 2 GB/s on DRAM. The read/write ratio remains at 3 in this stage. These characteristics remain unchanged when Laghos runs on the uncached NVM. On the other hand, the first phase in SuperLU exhibits high write traffic, and low read/write ratio when running on DRAM, resulting in an average of 33 GB/s and a peak at 40 GB/s. When running on the uncached NVM, the write bandwidth of this phase reduced by about 14 times, reaching only 2.3 GB/s. The dramatically reduced write performance throttles the read performance due to data dependency and coupling effects in shared units [20]. Consequently, the read performance is also reduced significantly from 54 GB/s to 4 GB/s. It is a high priority to address this change of behavior in critical phases when optimizing applications on NVM-based main memory.

We identify low read/write ratio and high write bandwidth as the indicator to detect applications that are susceptible to the write throttling effect. Comparing the two phases in SuperLU, we find that the second phase with a high read/write ratio and low write traffic has only a moderate slowdown, which is expected due to the performance gap between DRAM and NVM hardware. In Laghos, read and write bandwidth on DRAM in the two phases is lower than the peak bandwidth of NVM, so the changes in application performance are insignificant (27%). We highlight that phase-specific characteristics become crucial for determining the bottleneck of HPC applications on NVM because the throttling effect could dramatically change the profile of execution.

**Insight III:** HPC applications with computation phases susceptible to the write throttling effect on uncached-NVM require different priorities in optimization.

**D. Concurrency Contention**

HPC applications on supercomputers exploit the high parallelism from multicore processors to accelerate simulations. However, multiple threads may contend on shared buffers or units in the memory, creating a performance bottleneck. For instance, re-ordering and merging write to NVM is a common technique to mitigate the high energy cost and low write bandwidth of NVM technologies. On the testbed, write pending queues (WPQ) in NVM are used to combine...
multiple write requests into one transaction to the Optane media. When the concurrency is high, contention may arise on a fully occupied WPQ, where new requests have to wait for the WPQ to drain before being inserted into the queue [32]. Also, high concurrency would decrease the opportunity of combinable requests in WPQ, similar to the well-known fact that high concurrency reduces the locality in the row buffer.

We identify concurrency contention on NVM by comparing the performance changes at different concurrency across memory configurations. We run each application using two levels of concurrency on DRAM, cached-NVM, and uncached-NVM, respectively. The contention ratio on a memory configuration is measured as the performance at the high concurrency level normalized to that at the low concurrency level. Figure 6 reports the ratios in the eight applications. Applications with a ratio larger than one (the red dotted line) have performance improvement at increased concurrency. For instance, HACC and XSBench have more than 30% performance improvement when their concurrency increases. A ratio below one (the red line) indicates performance loss at high concurrency. However, the loss may not necessarily be a result of contention on memory. Some algorithmic properties of low scalability could also cause performance loss. Therefore, we propose to compare ratios on NVM to that on DRAM to identify the concurrency contention. For instance, FFT has a ratio of 0.61 on DRAM but only 0.37 on uncached-NVM, indicating that the contention from NVM is the main cause for performance loss. Similarly, Boxlib has a notable gap between the two ratios. Interestingly, ScaLAPACK has higher contention on cached-NVM than uncached-NVM.

We reconstruct the trace of memory traffic of FT and ScaLAPACK at two concurrency levels in Figure 7 and 8. FT consists of iterative phases. In each phase, the write bandwidth at the lower concurrency can reach 3 GB/s (7a) while at the high concurrency it is below 2.6 GB/s. The increased concurrency, however, has an opposite effect on read bandwidth, which increases from 3.8 GB/s to 4.5 GB/s. Overall, increased concurrency increases the divergence between the read and write bandwidth. This diverging effect could also change the composition of computation phases. In ScaLAPACK, the first stage extends from 10% execution time in Figure 8a to 30% in Figure 8b. Note that read bandwidth in the second stage increases from 12 GB/s to 17 GB/s, resulting in reduced execution time. Since the execution time of the first stage remains unchanged, it now becomes a more important phase in the computation.

Insight IV: Concurrency changes may have a diverging effect on read and write access. Phase-specific optimization or write-aware data placement may be more effective than a global adjustment of concurrency.
E. Leveraging the memory persistence

Large-scale HPC simulations rely on I/O intensive visualization and checkpointing to detect anomaly at an early stage for long-running jobs. Thus, HPC applications may directly benefit from high bandwidth and persistence on Optane memory for I/O. We configure Optane in App Direct mode and evaluate the overhead of visualization in Laghos on four tiers of storage, from tmpfs on DRAM, a DAX-aware ext4 file system on the Optane, an ext4 file system on the local RAID, to a Lustre file system on network interconnected disk. Note that tmpfs is not persistent but provides the upper bound of performance. The results are consistent with the memory/storage hierarchy, as shown in Figure 9a. The Optane memory only imposes 2%-5% overhead, achieving four times reduction in overhead on other persistent storages. We further analyze the interaction between NVM and DRAM traffic in Figure 9b. The write-only traffic to NVM is periodic (red triangles) at about 2 GB/s and shows no interference to the traffic to DRAM during the execution.

V. PERFORMANCE OPTIMIZATION

In this section, we propose two optimization techniques for cached- and uncached-NVM main memory, respectively. We develop a prediction model to estimate performance in cached-NVM when the concurrency or data size changes. On uncached-NVM, we employ write-aware data placement to avoid the diverging effect.

A. Model-based Prediction

The performance analysis on cached-NVM in Section IV-B and IV-D shows that both concurrency change and data size can impact the effectiveness of execution. Naturally, if a performance model can predict application performance at various configurations, it helps the application developer select an optimal setup without exhaustively search the configuration space. Suppose a general configuration consists of multiple dimensions of freedom. Our empirical observation indicates that when sweeping the configuration in one dimension, performance impact may change from positive to negative, which will reflect in a similar trend on some hardware events. These events are defined as critical events and used as predictors [5].

A set of critical events mutually indicate the overall trend in the performance of an application at a specific configuration. This behavior is modeled analytically in a multivariate function (Eq. 1). Here, each variant $N_{e_i}$ represents the count of one critical event $e_i$, $\beta_i$, the coefficient, indicates either a positive or negative impact on the derivative of performance. Our selection of critical events combines empirical observation and a statistical procedure. First, from the classification of performance sensitivity to NVM main memory, we identify several critical indicators, such as the computation intensity, memory traffic, read and write ratios. These metrics could be reflected in a range of hardware events. Second, we test a set of relevant hardware events into the regression model to prune highly correlated events, i.e., high p-values. Table IV summarize the events selected for deriving the prediction model.

$$IPC_p = \sum_{n=1}^{N} \beta_i \cdot (N_{e_i} \cdot IPC_s) + \sigma \quad (1)$$

Table IV: The events selected for performance prediction.

| Feature | Activities                                      |
|---------|-------------------------------------------------|
| $p_0$   | Instruction Retired                             |
| $p_1$   | Cycles Active                                   |
| $p_2$   | Cycles stalled due to Resource Related reason    |
| $p_3$   | Cycles in waiting for outstanding offcore requests |
| $p_4$   | Count of the number of reads issued to memory controllers. |
| $p_5$   | Counts of Writes Issued to the iMC by the HA.   |

We use two data collection strategies to collect training data sets for the models of concurrency and data size, separately. When deriving the model for predicting performance at different concurrency, we collect hardware events from application executions at the middle point concurrency. For instance, for hardware with $HT$ hardware concurrency, we collect data sets from executions using $0.75HT$. When deriving the model for predicting performance at a different data size, we fix the concurrency and collect events from configurations at a small data size. Next, the measurement for each hard event is first scaled by the sampled IPC ($IPC_s$ in Eq. 1) and then normalized by calculating their zero scores. The normalized features are used as the training data set to derive the coefficients of Eq. 1 using multivariate linear regression.

We evaluate the accuracy of the prediction by comparing the estimated IPC with the observed IPC. In the first experiment, we predict the application performance at different concurrency. We collect training data sets from running applications in the configuration of $ht = 36$ only. The prediction model is derived from this training data set to estimate the performance at other concurrency levels. The estimation error $E_{est}$ is calculated as the absolute difference
of prediction and observed divided by the observed IPC. In Figure 10, we report the accuracy as $1 - E_{est}$ for XSBench and FT, respectively. The average prediction errors in the two applications are 5% and 8%. All concurrency levels except the lowest and highest level have accuracy above 90%. In the second experiment, we derive the prediction for various data sizes at concurrency $ht = 36$. We collect the training data set from each application execution using a small input problem. The derived model then predicts the application performance at larger input problems. Figure 11 reports the prediction accuracy when the data size (x-axis) increases in XSBench and ScaLAPACK. While all data sizes in ScaLAPACK have accuracy over 97%, XSBench has lower accuracy at the largest data size.

![Figure 10: The model accuracy of concurrency change.](image)

![Figure 11: The model accuracy of data size change.](image)

### B. Write-aware Data Placement

We target uncached-NVM in heterogeneous memory in the second optimization strategy. Performance analysis in Section IV-D has revealed that some applications, such as ScaLAPACK and FT, are sensitive to the diverging effect on read and write access from concurrency changes. Instead of adjusting the global concurrency level, we explore write-aware data placement in applications to circumvent this effect. This approach keeps data structures with substantial write traffic in DRAM and places other data structures in NVM. Therefore, when concurrency increases, the read bandwidth from NVM could scale up and write to DRRAM avoids the contention on NVDIMMs.

We use a hardware sampling-based implementation of the data-centric profiling tool [22] to identify write-intensive data structures. Then, the source code is modified accordingly to place the data structures onto DRAM using APIs in [21]. Figure 12 presents the result after applying this optimization in ScaLAPACK, as compared to that on DRAM-only, cached-NVM, and uncached-NVM. The results show that this approach manages to achieve DRAM-like performance at different problem sizes. Note that the used DRAM size in this optimization is only 30% of the DRAM and cached-NVM modes. As a validation, we also placed other read-intensive data structures onto DRAM, which results in little difference compared to that on uncached-NVM.

![Figure 12: Compare the optimized Scalapack with the original on DRAM, cached-NVM and uncached-NVM.](image)

## VI. RELATED WORK

Before the hardware of byte-addressable NVM becomes available, most previous works use emulators and simulators for evaluating their approaches on NVM [8], [13], [19], [20], [23], [29]–[31], [33]. Although simulations and emulations can provide valuable insights into the performance trend, they either lack the performance details or are constraint by small problems due to the long simulation time. In [12] and [32], the authors prove that using software emulation or hardware emulation does not capture all the features of real hardware like the Intel Optane. Therefore, the system software for NVM proposed in the previous studies requires re-evaluation. Different from these works, the findings and insights in this work are derived from representative HPC applications on real NVM hardware.

Since the release of real hardware, several works have provided preliminary evaluations of the Intel Optane DC PMM [12], [21]. Some works have also ported selected applications in commercial database, scientific and graph workloads onto Optane [9], [18], [28], [32]. For instance, [9] optimizes the graph workload Galois to mitigate the NUMA effect when Optane is in the Memory mode. Still, a comprehensive evaluation that covers the landscape of HPC applications as in our work is missing.

Prior works have proposed various approaches for utilizing NVM-based heterogeneous memory systems [8], [20], [30], [31]. Unimem [30] uses a sample-based approach to collect memory access information to decide data placement on NVM-DRAM systems. Siena [20] explores different organizations and configurations of DRAM and NVM in a memory system to decide optimal system designs for HPC applications. NVStream [8] utilizes the byte-addressability in NVM to remove expensive system calls and uses non-temporary storage and delta compression to reduce overhead due to ensuring crash consistency on NVM. In this work,
we identify new optimization priorities and insights that will also benefit these approaches and techniques.

VII. Conclusion
In this work, we analyze the performance of the Seven Dwarfs on NVM-based heterogeneous main memory. Our results quantify the effectiveness of using DRAM as a cache to NVM to enable large problems at reasonable performance. For uncached NVM, we identify that the write throttling effect and concurrency contention requires a high priority in optimizations. We highlight that changing concurrency may have a diverging effect on read and write access in some applications. Therefore, a global adjustment of the concurrency may be insufficient. For the cached-NVM, we develop a prediction model based on hardware events collected from a small set of application runs to predict the performance at various concurrency and data size. For uncached-NVM, we demonstrate the effectiveness of write-aware data placement. Overall, our study provides insights and feedback for designing and exploiting NVM-based main memory on future supercomputers.

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