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Assessing the Potential of Inversion Layer Solar Cells Based on Highly Charged Dielectric Nanolayers

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The production and performance of p-type inversion layer (IL) Si solar cells, manufactured with an ion-injection technique that produces a highly charged dielectric nanolayer, are investigated. It is demonstrated that the field-induced electron layer underneath the dielectric can reach a dark sheet resistance of 0.95 kΩ sq⁻¹ on a 1 Ω cm n-type substrate, lower than any previously reported. In addition, it is shown that the implied open-circuit voltage of a p-type IL cell precursor with a highly charged dielectric is equivalent to that of a cell with a phosphorous emitter. In the cell precursor, light-beam-induced current measurements are performed, and the uniformity and performance of the IL is demonstrated. Finally, simulations are used to explain the physical characteristics of the interface leading to extremely low sheet resistances, and to assess the efficiency potential of IL cells. IL cells are predicted to reach an efficiency of 24.5%, and 24.8% on 5/10 Ω cm substrates, by replacing the phosphorous emitter with a simpler manufacturing process. This requires a charge density of beyond 2 × 10¹³ cm⁻², as is demonstrated here. Moreover, IL cells perform even better at higher charge densities and when negative charge is optimized at the rear dielectric.

1. Introduction

The continuous improvement of solar photovoltaic (PV) technology requires processing and device architectures that minimize charge carrier losses.¹–³ Passivated emitter and rear cells (PERCs) have become the industrial standard due to the developed Al₂O₃/SiNx passivating stack, which in combination with a reduced metal–silicon contact area have led to lower recombination losses in the rear of the cell. In addition, fabrication compatibility with the previous dominating technology—Al-BSF (full-area back surface field)—ensured a smooth transition to PERC with minimal processing additions or changes.⁴–⁶ Despite their advantages, the classical PERC design and its unavoidable losses limit commercial efficiency to just above 24%.⁷ The strongest contenders to supersede PERC are designs using passivating contacts to minimize silicon–metal contact losses and enhance the Si/dielectric interface passivation. Out of several passivating contacts recently proposed, the tunneling oxide/poly-Si passivated contacts (TOPCon)⁸–⁹ as well as the c-Si/a-Si heterojunction (HJT) structures¹⁰ have gained the most attraction since they allow for both excellent contact passivation and low contact resistance. The TOPCon designs require more processing steps than PERC cells, lack a passivating contact at the front, and are therefore limited by Auger recombination in the front boron emitter. HJT cells perform well because they have a passivating contact at both the front and rear surface but are limited by parasitic absorption in the front a-Si layer.

Therefore, we investigate an advanced inversion layer (IL) junction design that can be manufactured at low temperatures, and avoids parasitic absorption and Auger losses in the emitter. IL cells have been investigated in the past decades.¹¹–¹³ In IL cells, the pn junction is formed by introducing positive charges into a front dielectric layer, such that an n-type IL is formed in the underlying p-type base. The charge density must be sufficiently high so that the induced emitter is conductive enough to be comparable to the phosphorous emitter. Previously, fixed charge in titanium oxide, silicon oxide, tantalum oxide, and aluminum oxide thin films has been used to induce ILs in silicon.¹¹–¹³ Silicon nitride was first used in IL cells in the 1980s and has since been widely studied due to its high charge density and good
charge stability.\textsuperscript{[14]} Introducing cesium before nitride deposition was found to boost the charge density to nearly 10\textsuperscript{13} cm\textsuperscript{-2}.\textsuperscript{[15]} However, this concentration was not high enough to induce a sufficient conductivity to compete with phosphorous emitters at the time. The first challenge in developing IL cells is therefore to produce high enough charge densities in the dielectric layer, to reduce lateral resistive losses.\textsuperscript{[13,16–19]} Since the IL is interrupted at regions beneath the metal contacts, the second challenge is to produce local doping that ensures the continuity of the IL. Laser doping is a fast and cost-effective way to achieve this, and it has been recently used for this purpose in a prototype IL cell.\textsuperscript{[13]} Recent progress in metallization technologies shows that metal fingers between 20 and 25 μm wide are possible using screen printing,\textsuperscript{[20]} or a combination of laser doping and electroplating.\textsuperscript{[21,22]} This development allows more fingers per wafer without excessive shading losses, and therefore to use emitters with significantly higher sheet resistance values while avoiding significantly increased series resistance losses. Taking these developments in metallization into account, we investigate both the production and modeled operation of p-type IL Si solar cells on the basis of new findings about interface charge and passivation.

Herein, we first report the process of maximizing positive charge inside the dielectric layer, which produces a highly conductive electron-rich layer induced via field effect. We then explain the interface parameters of such ultracharged dielectric layer when in contact with Si, with help of Sentaurus TCAD (TCAD = technology computer aided design). Finally, we will assess the efficiency potential of p-type IL cells at maximized dielectric charge density.

2. Sample Preparation and Characterization

Two sets of silicon specimens were used here. The first set was used to optimize the dielectric charge and understand the properties of a SiO\textsubscript{2}/Si interface, whereas the second set was used to manufacture IL cell precursors and test the characteristics of the cell. Set 1 starts with a 200 μm thick, 1 Ω cm, phosphorus-doped n-type float zone silicon substrate. The planar wafers have a 100 nm thermal oxide grown on both sides at 1050 °C in a dry atmosphere. These were subsequently annealed in 5% hydrogen ambient at 425 °C for 30 min for enhanced chemical passivation. To maximize the charge density inside a SiO\textsubscript{2} surface layer, a field- and temperature-assisted technique was used to drive positive ions into the dielectric.\textsuperscript{[23]} This technique was originally developed for field-effect passivation\textsuperscript{[24–26]} since it enables control of charge inside passivating dielectrics. Charge densities above 5 × 10\textsuperscript{12} cm\textsuperscript{-2} were obtained and controlled with this technique in previous work. Here, this technique was leveraged and applied to IL cells with the aim to maximize charge. Figure 1 shows the processing of the ion migration technique, which involves delivery of ion precursors, application of an electric field, and an anneal at elevated temperature. The delivery of the ion precursor was conducted by spin-coating wafers with a solution of 10\textsuperscript{-3} mol L\textsuperscript{-1} KCl, in a deionized (DI) water:isopropyl alcohol (IPA) 30:70 solvent, at 3000 rpm for 30 s. The ions were driven into the dielectric layer by corona discharge (30 kV, 30 s), which generates an electric field across the dielectric, followed by an anneal at 430 °C for 10 s, to migrate the ions into the dielectric. The corona discharge rig used is the same as in the study by Bonilla et al.\textsuperscript{[27]} Herein, we first generate an electron accumulation layer on 1 Ω cm n-type wafers to demonstrate the potential of this technique.

The sheet resistance of Set 1 specimens was monitored using the Van der Pauw (VdP) method,\textsuperscript{[28,29]} with the sample structure shown in Figure 2a. The sample was first diced into 1 cm × 1 cm squares, before the surface dielectric at the corners removed by a diamond scribe. Then, 100 nm thick aluminum contacts were deposited at the corners by masked thermal evaporation. VdP measures the sheet resistance of the whole specimen, across the entire thickness. Figure 2b shows the structure of a sample with/without charge applied. To extract sheet resistance of the accumulation layer, an approximation is performed using the following calculations. The sheet resistance of the accumulation layer is given by

\begin{equation}
\frac{1}{R_{\text{sheet}}} = \frac{1}{R_{\text{accum}}} - \frac{1}{R_{\text{Si}}}
\end{equation}

Figure 1. Processing method for field- and temperature-assisted migration of ions into surface dielectrics: delivery of ion precursor, applying a polarization electric field, and annealing.
In Equation (1), $\sigma$ is conductivity, $t$ is thickness, and the regions A and B are labeled in Figure 2b. $R_S(A_0 + B_0) = \int \sigma(A_0 + B_0)dt^{-1}$ and $R_S(A + B) = \int \sigma(A + B)dt^{-1}$ are the measurable sheet resistances of the whole wafer, prior to and after charge application. Considering there is no illumination, $\sigma(B)dt$ is close to $\int \sigma(B_0)dt$, and $\int \sigma(A_0)dt \ll \int \sigma(A)dt$, so an approximation is made to calculate the accumulation layer sheet resistance, from the two measurable quantities as follows

$$R_S(\text{acc}) \approx \frac{1}{\int \sigma(A + B)dt - \int \sigma(A_0 + B_0)dt} = \frac{1}{R_S(A + B)^{-1} - R_S(A_0 + B_0)^{-1}} \tag{2}$$

All measured $R_S(\text{acc})$ values reported herein use this approximation. Sentaurus device simulations were conducted for this sample geometry to assess the inaccuracy of using the approximation in Equation (2). The simulations showed that, for a charge density of $2 \times 10^{13} \text{ cm}^{-2}$, this approximated $R_s$ (Equation (2)) is 4.7% higher than that calculated using Equation (1) with the simulated conductivity and carrier density across the specimen. A full analysis of such simulation is discussed in the Supporting Information for completeness.

To obtain the wafer sheet resistance, two resistance measurements are taken and computed using the following VdP relations:

$$R_S = \frac{\sigma}{d} = \frac{\pi \left( R_{AB,CD} + R_{BC,DA} \right)}{2} \tag{3}$$

$$R_{AB,CD} = \frac{V_{DC}}{I_{AB}} \tag{4}$$

where $V_{DC}$ is the voltage difference between contact C and contact D, whereas a current of $I_{AB}$ is forced through contact A and contact B. The contacts are labeled in Figure 2a. When there is fourfold rotational symmetry of the sample structure, $R_{AB,CD}$ can be assumed equivalent to $R_{BC,DA}$. One measurement of the resistance is therefore proportional to the wafer sheet resistance, and is used as a parameter, referred to as intermediate resistance, to reflect the change of wafer sheet resistance in Section 3.

Understanding the properties of the Si–SiO$_2$ interface and the formation of the field-induced electron layer has been conducted via VdP $R_s$ measurements as a function of dielectric charge, on specimens from Set 1. To avoid error in monitoring the exact concentration of dielectric charge, a subset of specimens was only charged via corona discharge, without the presence of alkali ions or any annealing steps. This set was used to establish the dependence of resistivity and charge carrier density on the amount of dielectric charge. A Kelvin probe (KP) was used to record the surface potential of these specimens, and the charge was extracted using the formalism in the study by Bonilla et al. assuming that charge stays at the surface of the dielectric during the measurement period, which has been previously shown to be reasonable. A KP020 KP kit from KP technologies and the same corona charging kit were used for this purpose.

The second set of the samples (Set 2) used the structure shown in Figure 3, and was produced with the purpose of fabricating IL cell precursors. These 180 µm thick, 1 Ω cm, p-type Cz Si solar grade wafers were RCA cleaned (RCA = Radio Corporation of America), textured in a KOH solution, and had a 100 nm thermal oxide grown on both sides. Rear openings were produced using a laser scriber prior to rear screen printing of aluminum paste. The wafers were then fired at ≈825 °C set temperature, for 3 s in a SCHMID (previously Sierratherm) belt furnace. A localized emitter was formed across the front surface by laser doping. An 85% H$_3$PO$_4$ solution was spin coated at 8000 rpm for 50 s onto the sample as a phosphorus source. A continuous wave, 532 nm, 20 W laser was scanned across the surface twice at a speed of 2 m s$^{-1}$ to both ablate the dielectric material and melt the silicon beneath to allow diffusion of P atoms and dope the molten
region. The laser was scanned across the same region twice to ensure sufficient incorporation of dopants. Further details of this laser doping process can be found in the studies by Davidsen et al. and Hallam et al. \[22,31\] The fingers were spaced apart by 0.7 mm, with a single 1 mm wide bus bar produced in the middle of the cell, as shown in Figure 3b. The active region of the precursors is 20 mm × 20 mm at the center of the 40 mm × 40 mm specimen. The samples were then rinsed in DI water for 15 min to remove the phosphorous solution. It is noted that these samples did not have the benefits of phosphorous gettering during emitter formation, nor any hydrogenation effects since no fired silicon nitride was used in this case. The purpose of this experiment was to study charge origin arising only from the extrinsic ions in the oxide film. An ion precursor solution of KCl (0.05 mol L\(^{-1}\)) KCl, DI water:IPA = 30:70) was used here to provide a source of K\(^{+}\) ions to be migrated into the oxide surface film. The ions were later driven into the dielectric layer by corona-annex cycles, as described earlier. Implied \(V_{oc}\) (\(iV_{oc}\)) was measured in between corona-annex cycles by a Sinton Suns-\(V_{oc}\) instrument, to monitor the appearance of the charge-induced emitter. Light-beam-induced current (LBIC) maps were also obtained for precursors with or without the IL being produced by the charged ions. The contrast in an LBIC map comes from variation in collection efficiency. The technique has therefore been used to visualize the induced pn junction and check its uniformity and electrical connection between the induced emitter and the laser-doped bus bar. We used a 405 nm wavelength blue laser in our LBIC setup. Further details about this set up can be found in the study by Shi et al.\[32\]

### 3. Field-Induced Electron Layers

Specimens in Set 1 had an ionic precursor delivered by means of spin coating, followed by electrostatic charging and migration of the ions into the dielectric at elevated temperature. This was repeated in cycles until the sheet resistance of the wafer plateaued, which was monitored using VdP measurements after each discharge and anneal cycle. The recorded field-induced sheet resistance from two samples is shown in Figure 4, with each point taken after a corona discharge (30 kV, 30 s) and anneal (430 °C, 10 s) cycle, and each color representing measurements taken after the ion precursor had been replenished via spin coating. The lowest accumulation layer sheet resistance values of the two samples were 1.19 and 1.12 kΩ sq\(^{-1}\), which were found to have reduced to 0.95 and 0.96 kΩ sq\(^{-1}\), respectively, when measured 30 days later. This implies that an even higher net charge density is present within the thin oxide, than that produced immediately after processing.

From the decrease in accumulation layer sheet resistance in Figure 4, it is evident that the first measurement immediately after each spin coating resulted in a higher resistance than the previously recorded one. This increase can be explained by the adsorption of molecules with negative charge at the oxide surface during spin coating, which would compensate the positive charge in the dielectrics, therefore the measured sheet resistance would appear higher than that prior to the spin coating. The anions would then be driven off the surface during the anneal, which would produce a concentration of only positive K\(^{+}\) ions in the oxide. Another aspect worth noticing is the unexpected reduction observed 30 days after processing, with an even lower value of \(R_s\) measured after a short anneal (430 °C, 20 s). We propose that this is due to the change of charge distribution at the Si–SiO\(_2\) interface: the high voltage applied during corona discharge produces an additional space charge that allows electrons from Si to be trapped at the interface states, partially compensating the positive charge. This is often referred to as hot-electron injection, and its net effect would be to increase sheet resistance of the electron layer. These electrons will decay to ground states gradually afterward and bring the net charge concentration up, and thus the sheet resistance down. The sheet resistance drop observed at the points that are noted with “overnight” and “1 h later” in Figure 4 can be explained by the same effect. The further reduction by an anneal can be explained by the drive off of negative molecules adsorbed at the surface, since the specimens were left in a noncontrolled laboratory atmosphere. To study these effects in detail, additional measurements were conducted on specimens from Set 1.

The effects of the short anneal (430 °C, 20 s) and voltage application were explored since these are unavoidable processes...
during the ion migration. Monitoring of the charge distribution at the dielectric–silicon interface due to the processing was conducted via KP and VdP. Figure 5a shows the KP-monitored contact potential difference (CPD) between the silicon bulk and a gold probe after a short anneal on two specimens: one fresh specimen, and one where ionic charge was applied 10 months earlier in the same manner as in Figure 4. CPD reflects a change in the amount of charge both at the surface and within the dielectric layer. The CPD of the fresh sample sees an increase upon the short anneal and decays back gradually in hours. This is assumed to be due to the injection of electrons from the Si bulk to the dielectric layer. Such electrons then decay to ground states and bring the CPD back to the original level. For the previously ionic-charged sample, the CPD drop upon annealing is due to the drive off of surface-adsorbed negative molecules, which could have occurred in the 10 month period. VdP measurements were used to both alter and monitor the charge distribution to show the effect of voltage application. Standard VdP measurements require two equivalent resistance measurements for each calculated sheet resistance, as described in Section 2. An average of the two resistance measurements is shown to be proportional to the calculated wafer sheet resistance. To be able to record resistance continuously, here we use only one measurement, referred to as intermediate resistance, which is indicative of the change of specimen resistivity. Current from –10 to 10 mA was scanned between two adjacent contacts on a fresh Set 1 sample, producing the maximum voltage difference of ≈1 V. The measurements were taken as groups of 20 with 1/5/15 s intervals between each measurement. Three consecutive sets were taken for each measurement interval, with a 10 min gap in between to allow excited electrons to decay. Figure 5b shows the change of intermediate resistance for each measurement. The increase in intermediate resistance for each measurement indicates the effect of the measurement itself, meaning that the voltage applied drives electrons from the Si bulk toward the dielectric, with the effect more prominent at a shorter measurement interval. The decrease in intermediate resistance toward the initial value after a 10 min gap shows an almost complete decay. This same experiment was repeated three times on each sample to confirm the physical phenomenon. Since the samples are periodically exposed to a corona discharge with a voltage of 30 kV, it is therefore expected that the rise in potential across the dielectric will have an impact on the measurement of accumulation layer sheet resistance. We were able to eliminate this impact by taking an additional measurement long enough after the ion migration process has been done, and in this way, we evaluate the final steady state of the samples. Such values are reported as the 30 day measurement in Figure 4.

4. Electrical Properties of the Interface and Field-Induced Layer

Both the sheet resistance of the electron layer and the density of positive charge in the dielectric are essential parameters to understand the properties of IL cells. Accumulation layer sheet resistance can be obtained using VdP measurements as described earlier, whereas charge density can be acquired using KP provided that the centroid of the ions is known with respect to the Si–SiO₂ interface, as detailed in the study by Bonilla et al.[30] In Section 3, the electron layer was induced by K⁺ ions driven into the dielectric layer in which case the distribution of the ions is unknown, and cumbersome to obtain via KP. In this section, the charge is instead generated using only a corona discharge. Such charges stay at the surface of the dielectric layer and are therefore easily measurable using KP.[27] The accumulation layer sheet resistance and wafer sheet resistance were obtained for a Set 1 specimen, as a function of corona charge density as is shown in squares in Figure 6. A model was developed in Sentaurus TCAD to understand the properties of and account for all physical phenomena involved in the formation of the field-induced electron layers. The model comprises a 200 μm thick, 1 Ω cm n-Si specimen, with an oxide layer on both sides. Positive dielectric charge was defined at the front Si–SiO₂ interface. Interface state density (Dit) of 5 × 10¹⁰ eV⁻¹ cm⁻² was set at midgap, 2 × 10¹⁵ eV⁻¹ cm⁻² at the conduction band tail, and 8 × 10¹⁴ eV⁻¹ cm⁻² at the valence band tail, as has been recently reported.[31] A schematic of the structure and a band diagram at the interface is shown in the inset in Figure 6a. Klaassen’s parameterization was used to model the mobility throughout the sample bulk and in the space charge layer.[34] A density
gradient quantum-mechanical model (DGM) was used to account for the confined carrier distributions occurring near semiconductor–insulator interfaces \[^{[35,36]}\]. Including these carrier density and mobility effect was critical to achieve a model that reflected the measurements. The equilibrium state was calculated, and the carrier density and mobility were extracted as a function of the distance from the Si–SiO\(_2\) interface. These were integrated over the entire sample depth to calculate the wafer sheet resistance. Wafer sheet resistance of the model with no charge specified was simulated to work out the accumulation layer sheet resistance using the method described in Section 2. Further details of the model can be found in the Supporting Information, and a full description of the physical phenomena is reported in the study by Yu et al. \[^{[37]}\]. The simulated accumulation layer sheet resistance and specimen sheet resistance as a function of charge density are shown in Figure 6. The simulated curves show good agreement with the experimental data. The model can then be explored to predict the behavior of the electron layer in a complete device architecture.

Both accumulation layer (on n-type wafers) and IL (on p-type wafers) were simulated using this model, including positive charge densities up to \(4 \times 10^{13} \text{ cm}^{-2}\) on 1, 5, and 10 \(\Omega\) cm wafers. Here, the thickness of an induced layer was defined by the location at which the electron density stops changing with depth, defined by where \(dn/dt < 10^{16} \text{ cm}^{-4}\) for the accumulation layer, and the location where the hole density exceeds that of electrons for the IL. The sheet resistance was calculated by equating the reciprocal of integrated carrier density times mobility, over the specified thickness, as previously described in Equation (1). This gives a slightly lower value than that approximated by Equation (2), as described in Section 2. A list of \(R_s(\text{acc})\) calculated by the two methods can be found in the Supporting Information.

Figure 7 shows the sheet resistance of the induced layers. For an IL in a p-type base, the induced electrons initially deplete the surface region, before they are in sufficient concentration to drive the surface into an inversion n-type layer. This explains the higher resistance observed for 1 \(\Omega\) cm versus 10 \(\Omega\) cm material for IL in Figure 7a, as opposed to the accumulation layer sheet resistance in Figure 7b. For clarity, Table 1 lists the sheet resistance of accumulation and IL at charge densities above \(1.6 \times 10^{13} \text{ cm}^{-2}\). Here, it is predicted that a charge density of \(4 \times 10^{13} \text{ cm}^{-2}\) can produce an IL sheet resistance as low as 182 \(\Omega\) sq \(^{-1}\) on a 1 \(\Omega\) cm wafer, and 180 \(\Omega\) sq \(^{-1}\) on a 5 \(\Omega\) cm wafer, which is close to that of a P-diffused emitter. \[^{[38]}\] This of course relies on the ability to produce a dipole with sufficient electric field strength to support this concentration of charge. The lowest accumulation layer sheet resistance acquired in Section 3 is 0.95 k\(\Omega\) sq \(^{-1}\), indicating the charge density is \(\approx 2 \times 10^{13} \text{ cm}^{-2}\) according to Table 1.
The simulation results also show that a 1500 1499 1946 1734 1 2 5 cm base 1 www.pss-rapid.com sqΩ2 2 DΩ2 2 RΩD cm base 1 interface to reduce probe at Ω10 C, 10 s) cycles. After the last spin of KCl solution, (midgap) has a minor effect on local carrier eV can be obtained with a charge eV band-tail states concentrations. It is clear from 10 cm 2 843 841 968 911 this suggests that and (midgap) below 10 cm 2, assuming a well-passivated interface with Dν = 5 10МОeV cm2 at midgap, and 1035/1014eV cm2 at conduction/valence band tail.[33] In addition, it is important to note that, since the emitter resistance decreases with light injection, IL solar cells do not have the same requirement for emitter conductivity as PERC. This is explored in Section 6.

5. Field-Induced IL on p-Type Cell Precursors

Ionic charge was applied on Set 2 specimens to generate an induced emitter and fabricate precursor IL cells. Figure 9a shows a schematic of a Set 2 sample with positive charge applied at the dielectric surface. It is noted that laser damage occurs at the boundary between the doped opening and the SiO2 film during the laser doping process as noted in Figure 9a. A number of mechanisms can be involved in damaging this boundary, e.g., thermal mismatch between Si and SiO2 during cooling after lasering, the amorphous to crystalline Si interface formed after the laser-melted region freezes, or the doping efficiency through the amorphous–crystalline interface. When the SiO2 film is charged immediately after laser doping, there is a gap in the induced n-type layer underneath the laser damage, which hinders the extraction of electrons collected by the IL pn junction. Therefore, before the application of K+ ion precursors, the samples were annealed at 430 °C, from 30 min to 1 h, with the aim to: 1) improve doping efficiency at the boundary between the p-type bulk Si and laser-doped n-type; 2) allow regeneration of bonds at the Si–SiO2 interface to reduce Dν; and 3) distinguish the effect of annealing on repairing the boundary from the effect of annealing on ion migration when performed after charge deposition. An IL was then induced by spin coating of the KCl solution and conducting corona–anneal cycles as described in Section 2. Both processes were monitored by Suns–Voc and shown in Figure 9b,c. Each color change represents a replenishment of the ion precursor using a spin coating of solution. Each point was taken after two corona discharge (30 kV, 30 s) and anneal (430 °C, 10 s) cycles. After the last spin of KCl solution, measurements were taken by placing the Suns-Voc probe at

Table 1. Sheet resistance of accumulation an IL at positive charge densities of 1.6 × 1013, 2 × 1013, 2.5 × 1013, and 4 × 1013 cm−2 on 1, 5 Ωcm n/p-type Si wafers by simulation.

| Q [cm−2] | Racc (Ω sq−1) | Rinv (Ω sq−1) |
|----------|---------------|---------------|
|          | 1 Ωcm base    | 5 Ωcm base    | 1 Ωcm base | 5 Ωcm base |
| 1.6 × 1013 | 1500          | 1499          | 1946       | 1734       |
| 2 × 1013   | 843           | 841           | 968        | 911        |
| 2.5 × 1013 | 436           | 436           | 467        | 453        |
| 4 × 1013   | 178           | 178           | 182        | 180        |

Figure 8. a) Simulated wafer sheet resistance of a 200 μm thick, 1 Ωcm, n-Si specimen as a function of dielectric charge density for various Dν values at midgap and b) various Dν, band-tail states concentrations.

To our knowledge, this value is the highest achieved in any reported IL cell to date.[39] The simulation results also show that it is possible to obtain a sheet resistance nearing that of standard diffused emitter, when sufficient charge is provided to induce the emitters.

Low emitter conductivity has been considered as one of the major concerns for IL cells. Density of interface states at both midgap and at the band tail are key factors limiting the IL emitter conductivity. Here, we explore the possibility of increasing induced emitter conductivity by passivating the states. Figure 8 shows the simulated wafer sheet resistance as a function of charge density with various Dν values. It is clear from Figure 8a that the shift of wafer sheet resistance is less than 0.1 Ω sq−1 for Dν (midgap) below 1012 eV cm−2. Since this is the case for most passivated wafers,[40,41] this suggests that the variation of Dν (midgap) has a minor effect on local carrier distribution, and therefore on the conductivity of the space charge layer. The effect of Dν at tail states is shown in Figure 8b. It is evident that there are large changes in: 1) wafer sheet resistance and 2) the dependence of resistance on surface charge density. These simulation results demonstrate that passivating band-tail interface states is key to improve conductivity of an induced emitter, since more charge would be directly mirrored in the induced layer rather than in the interface states. Despite the high electron layer sheet resistance obtained (0.95 kΩ sq−1), it can be further reduced by optimizing dielectric charge density and Dν (tail). An emitter sheet resistance of 0.35 kΩ sq−1 can be obtained with a charge density of 2 × 1013 cm−2, and 0.25/0.14 kΩ sq−1 at 2.5 × 1013/4 × 1013 cm−2, assuming a well-passivated interface with Dν = 5 × 1010 eV cm−2 at midgap, and 1013/1012 eV cm−2 at conduction/valence band tail.[33]
different positions of the bus bar to evaluate the measurement variability. This variability is indicated by the error bars in the last measurements in Figure 9b,c. The $iV_{oc}$ increased by 150–160 mV during the first 30 min of anneal and plateaued. Ionic charge then boosted the $iV_{oc}$ by ≈30 mV to a final $iV_{oc}$ of ≈604 mV, indicating the appearance and the continuity of the n-type IL. At an $iV_{oc}$ of ≈600 mV, it appears the precursor cell is no longer limited by charge carrier collection at the IL junction. Although 604 mV may seem low, it is actually a high $V_{oc}$ considering the dimensions and geometry of the sample, as well as the lack of gettering or hydrogenation processes in the bulk. In Figure 9c, a higher $iV_{oc}$ was taken 4 months after drive-in of the K$^+$ ions, with a further increase recorded after a short anneal, which agrees with the increased accumulation layer conductivity found 1 month after processing described in Section 3.

Figure 10 shows an LBIC map of a 1.25 mm $^2$ area of the IL precursor cell with 125 × 125 pixels, which is indicative of the photocurrent collected while a blue laser is scanned across the front surface. It is important to note that no metallization has been applied to this cell precursor, so the LBIC current is only indicative for this particular structure. The low-current regions represent the laser-doped fingers as expected. The uniform high-current region between the fingers indicates that the pn junction is formed uniformly across the whole of the sample, and that the electrical contact between the induced emitter and the laser-doped bus bar is no longer affected by the laser damage. Figure 10b shows the LBIC image of a control sample where no ionic charge was incorporated but underwent the initial anneal at 430 °C for 30 min. The large low-current regions in between fingers indicate the clear absence of an emitter. The high-current stripes right adjacent to the laser-doped lines comes from the pn junction formed between the laser-doped P-rich region and the p-type bulk. These results prove the uniform formation of the induced emitter and the continuity of a full-area n-type layer underneath the dielectric. The potential of the IL cell with optimized parameters is explored in Section 6.

6. Device Simulations of IL Cell Performance

The performance of IL cells at various finger spacings and charge densities was simulated on 1 and 5 Ω cm p-type substrates using Sentaurus TCAD. The finger width was set to 25 μm since recent progress in metallization technologies shows that such thin metal fingers are possible using screen printing, or a
combination of laser doping and electroplating. The bulk lifetime was set to $\tau_p = 10$, $\tau_n = 3.7$ ms for 1 $\Omega$ cm, as may be reached in Ga-doped wafers if Fe concentration is sufficiently small, and $\tau_p = 10$, $\tau_n = 15$ ms for 5 $\Omega$ cm, $\tau_p = 131$ ms, $\tau_n = 1.14$ ms for 10 $\Omega$ cm wafers as referred from the studies by Min et al. and Altermatt et al. The rear of the cell is set to be the same dielectric-silicon interface as the front dielectric but passivated with a typical, negatively charged dielectric with density of $5 \times 10^{13}$ cm$^{-2}$, which is a reasonable fixed charge at a c-Si/Al$_2$O$_3$ interface. A modified local-density approximation (MLDA) quantum-mechanical model rather than DGM is used here to accelerate the simulations. The difference in simulated sheet resistance for the two models is negligible and their comparison is included in the Supporting Information. In these simulations, we first focus on a cell in which the phosphorus emitter of a PERC architecture is directly replaced by the IL emitter. We then address the optimization of negative charge at the rear dielectric to create the best industrially possible IL cell.

Figure 11 shows the performance of the simulated IL cells, with the dashed lines being internal efficiencies, and the solid lines considering grid resistance and shading losses. For Figure 11a, $D_n$ at tail states is $2 \times 10^{15}$ eV$^{-1}$ cm$^{-2}$ at the conduction band, and $8 \times 10^{14}$ eV$^{-1}$ cm$^{-2}$ at the valence band, the same as used in the model in Section 4, without SiN$_x$ hydrogen passivation. For cells with a 1 $\Omega$ cm base, the performance is predicted to be higher at higher charge densities, and at $2 \times 10^{15}$ cm$^{-2}$, the performance would peak at the finger spacing of 800 $\mu$m, with the tendency of shifting to a larger finger spacing at a higher charge density. The peak occurs when the performance gain due to reduced shading losses is outweighed by the increased resistive losses, its shift toward larger finger spacing therefore implies a more conductive emitter. Switching to a higher base resistivity produces a more conductive emitter, which alleviates the effect of increased resistive losses while allowing larger finger spacing, with the additional benefit of less sensitivity to bulk recombination, and therefore reduced requirement for gettering and hydrogenation. By switching to 5 $\Omega$ cm, the best cells’ performance increased by 0.35–0.62% absolute to 23.8–24%, and further by 0.52–0.87% absolute to 24–24.2% on a 10 $\Omega$ cm base. A combination of SiN$_x$/SiO$_2$ stack and extra hydrogen passivation is estimated to bring the band-tail interface states down to a density of $10^{15}$/10$^{14}$ eV$^{-1}$ cm$^{-2}$ at the conduction/valence band. Figure 11b shows the performance of the cell when surface passivation is enhanced, thus reducing the band-tail states. The improvement in cell performance by the passivation is noted, with the maximum efficiency at various charge densities increased by 0.27–0.5% absolute, to 23.7–23.9% on 1 $\Omega$ cm substrates. The 5 $\Omega$ cm substrates see yet better cell performances, with the best cell reaching 24.5–24.6% efficiency, and 24.8–24.9% on 10 $\Omega$ cm substrates. Low emitter conductivity has been considered as one of the major concerns for IL cells. With the plateaus only appearing at finger pitches of 1400 $\mu$m for the

![Figure 11](Image)
charge density of $2 \times 10^{13} \text{cm}^{-2}$ on 5 $\Omega$ cm substrates, it is clear that the emitter resistivity is no longer limiting the efficiency potential of IL cells.

The ultimate potential of an IL cell incorporating negative charge in the rear dielectric is now explored. A negative charge density of above $1 \times 10^{13} \text{cm}^{-2}$ has been proven possible at a c-Si/$\text{Al}_2\text{O}_3$ interface,\cite{24} but there still remains huge potential for increasing and optimizing such charge, especially when combined with a nitride capping layer. Figure 11c shows the potential of the cells when both positive/negative charge density at the front and the rear are set to be the same. $D_n$ was set to be $5 \times 10^{10} \text{eV}^{-1} \text{cm}^{-2}$ at midgap and $10^{15}/10^{14} \text{eV}^{-1} \text{cm}^{-2}$ at conduction/valence band tail. The increased conductivity near the rear dielectric by the addition of negative charge is shown to improve the cell performance to beyond 24.6% and 24.9% on a 5/10 $\Omega$ cm substrate, at a charge density of $2 \times 10^{13} \text{cm}^{-2}$ at both front and rear dielectric, with a further improvement possible at larger pitches or charge densities. The top efficiency in the fabrication line is 24.3% for 5 $\Omega$ cm, and 24.6% for 10 $\Omega$ cm substrates, and is equivalent to what is expected for PERC.\cite{25} For these simulations, recombination at the rear contact is found to be the limiting loss. Considering that the IL model has a same cell design at the rear as PERC, the field-induced emitter is predicted to perform as good as a diffused one. These simulation results demonstrate the following: 1) the potential of IL as a competitive cell type in PV industry, especially with negative charge incorporated at rear dielectric; 2) the benefit of switching to 5 $\Omega$ cm substrates is clear and could be taken advantage of; and 3) the significance of passivating $D_n$ at tail states at the Si–dielectric interface.

### 7. Conclusions

This work studies the fabrication and potential of p-type IL Si solar cell based on highly charged dielectric nanolayers. A field- and temperature-assisted method has been developed to manipulate ionic charge to achieve an extremely high charge density inside a dielectric layer. With this ion-charged dielectric, we managed to induce an electron layer in dark on a 1 $\Omega$ cm, n-type Si wafer, with its sheet resistance being as low as 955 $\Omega$ sq$^{-1}$—the lowest value reported in the literature to the authors’ knowledge. The ionic charge was applied to a p-type substrate with laser-doped selective emitters to fabricate a precursor cell, with its implied $V_{oc}$ exceeding 600 mV after induction of the IL. This is regarded as a substantial step forward in the manufacture of IL cells, considering the dimension, geometry, and lack of gettering and hydrogenation of these cells. Sentaurus TCAD simulations were conducted to evaluate the potential of IL cells on 1, 5, and 10 $\Omega$ cm substrates. The results show that IL cells can present an efficiency of 24.5%, and 24.8%, on 5 and 10 $\Omega$ cm substrates provided that the charge density exceed $2 \times 10^{13} \text{cm}^{-2}$, and the interface is improved by the SiN$_x$/SiO$_2$ passivation stack and extra hydrogen passivation. Here, a charge density of $2 \times 10^{13} \text{cm}^{-2}$ has been attained in the laboratory. Better performance is predicted provided higher charge densities, or incorporation of negative charge at rear dielectric. In addition, it is found that switching from to more resistive substrates can lead to an efficiency boost of 0.65–0.79% (5 $\Omega$ cm) and 0.94–1.11% (10 $\Omega$ cm) absolute, for charge densities above $2 \times 10^{13} \text{cm}^{-2}$, pointing out the benefit on using higher-resistivity wafers. The simulation results also demonstrate the prominent effect of passivating $D_n$ at tail states in terms of improving induced emitter conductivity. By increasing the temperature to 500 °C and the corona discharge rate, this ion migration process can be done in seconds, at moderate temperatures, and using inexpensive and fast corona processing. IL cells can potentially have very low capital expenditure if adopted industrially.

### Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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### Conflict of Interest

The authors declare no conflict of interest.

### Data Availability Statement

The data that support the findings of this study are openly available in the Oxford University Research Archive at https://ora.ox.ac.uk, reference number 2de97cf5-d000-4b67-973d-78f9fc9f2bf2.
