Utilization of Si atomic steps for Cu nanowire fabrication

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Abstract

Techniques for controlling atomic step position at low-temperature and selective growth of Cu nanowires along the atomic step edges have been studied. By immersing the Si(111) substrates with well-defined step/terrace surfaces in the Cu-contained water with the dissolved oxygen content of less than 1 ppb, selective growth of Cu nanowires along the step edges was successfully achieved. Total reflection X-ray fluorescence spectroscopy (TXRF) revealed that the fabricated nanowires were composed of mono-atomic Cu rows. For step position control, the characteristics of step-flow pinning effect of SiO\textsubscript{2} films were investigated. Fine SiO\textsubscript{2} line patterns drawn by anodic oxidation using AFM probes enable us to obtain the step-free Si areas predetermined by the patterns.

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1. Introduction

Nanoscale devices have high potential for pioneering future electronics. To utilize various kinds of developed nanodevices, it is one of the most useful applications to combine them with ultra-large scale integrated circuits (ULSI). In addition, Si single crystal is one of the important and hopeful materials to realize future nanotechnologies, because of its high purity and significant surface controllability. Therefore, it is important to establish fabrication technologies of various kinds of nanostructures on the single crystal Si surfaces\cite{1–3}.

To achieve fabrication of nanodevices, self-assembled or self-organized technologies are most useful because of its cost advantage compared with the conventional lithography. It is very appropriate to utilize the Si surface from this point of view. Atomic steps of Si surfaces are expected as the simplest and finest controllable structures. Selective growth of metallic nanowires along the atomic steps will give us some possibilities of realizing nanodevices. Until now, a lot of nanowiring technologies have been proposed. Some methods for controlling the step/terrace structures have been also reported. It was reported that the step/terrace structures in the predetermined area by forming holes or trenches could be constructed on the vicinal Si(111) surface by high temperature annealing in ultrahigh vacuum\cite{4,5}. A method of flattening the Si surface on mesas with Si epitaxial growth was also proposed\cite{6}. However, it is difficult to apply these high temperature processes to flattening the Si surface after oxide isolation to combine with the fine pattern of ULSI. Low temperature processes will be a key concept in manufacturing nanodevices.

In this study, we report technologies for controlling atomic steps at low temperature and selectively growing Cu nanowires along the atomic step edges in Cu-contained solution at room temperature. In addition, the possibility of the step controllability will be also discussed.

2. Experimental

The samples used in this experiment were p-type Si(111) wafers with miscut angles varied from 0 to 0.2\degree in the (112) direction. All the samples were etched in ultralow-dissolved-oxygen water (LOW) with the dissolved oxygen
content of less than 1 ppb to form well-defined step/terrace structures on the surfaces. LOW is an aqueous solution of ammonium sulfite monohydrates \[7,8\]. For Cu nanowire formation, the samples were subsequently immersed for 10 s at room temperature in solutions containing 10 ppm Cu ions, where the dissolved oxygen content was controlled. The solutions were water dilution of Cu standard solution (10,000 ppm Cu in 5 wt% HCl). The surface topography was observed by atomic force microscopy (AFM) before and after the immersion. The quantitative analysis on the Cu adsorption was performed by total reflection X-ray fluorescence spectroscopy (TXRF). An incident angle, a tube voltage and current of X-ray generator in the TXRF measurements were 0.05, 40 kV and 40 mA, respectively.

The key idea for the step control is combination of step etching and pinning. The samples with step/terrace structure obtained in the LOW were transferred into an AFM equipment. Formation of the pinning sites for the step flow was done by fabricating fine SiO\(_2\) line patterns. The patterns were drawn by anodic oxidation using an AFM probe \[8\]. The samples were then etched again in LOW. Morphologies of the all surfaces were observed by AFM in the cyclic mode in air.

3. Results and discussion

3.1. Cu nanowire formation

Fig. 1 shows 200 nm×200 nm AFM images of the Si(111) surfaces (a) before and (b) after immersion in the Cu-contained solution. The content of dissolved oxygen in the Cu-contained solution was controlled as less than 1 ppb. The surface after LOW treatment clearly reveals atomically flat step/terrace structure, as seen in Fig. 1(a), which was achieved due to considerably higher etching rate at step edges than on terraces in the solution. After immersion in the Cu-contained solution, nanoscale wire was apparently formed at the step edge, as indicated with an arrow in Fig. 1(b). The average width and height of the nanowire were estimated as 10 and 0.5 nm, respectively \[9\], although these values could involve overestimation due to curvature radius of AFM probes. To identify the material of the nanowire, the amount of adsorbed Cu atoms was investigated by TXRF on the Si substrates with various miscut angles. The result is shown in Fig. 2. The average step density of each Si surface with different miscut angle was estimated from AFM images of five areas of the same Si substrate. In this figure, it can be seen that there exits a strong linear relationship between the amount of Cu atoms and average step density \[10\]. It clearly indicates that the constituent material of the nanowire fabricated at step edges is Cu atoms. In addition, the area density of the Cu atoms, \(A_{\text{Cu}}\) (atoms/cm\(^2\)), was found as

\[
A_{\text{Cu}} = 2.8 \times 10^7 \times L + B
\]

where \(L\) (cm\(^{-1}\)) is the total length of the bi-atomic step edges in 1 cm\(^2\) area on the Si(111) surfaces. In Eq. (1), the proportionality factor, \(2.8 \times 10^7\) cm\(^{-1}\), and the second term, \(B\), correspond to the amount of Cu atoms adsorbed at unit length of the step and on unit terrace area, respectively. The amount of Si atoms at step edge per unit step length is calculated to be \(2.6 \times 10^7\) cm\(^{-1}\) from the lattice constant of crystalline Si. This result reveals that the nanowires formed along the atomic step edges consist of approximately monoatomic Cu rows. The Cu atom density on terrace region was found from \(B\) as the order of \(10^{11}\) atoms/cm\(^2\), which is only one in 10,000 of the Si atoms on the terraces. The results demonstrate the high potential of the present nanowire.
fabrication method to achieve significant growth selectivity on atomic steps.

We consider the selective growth mechanism of Cu nanowires along the step edges as follows. At step edges, etching reaction of Si with $\text{OH}^-$ ions generates electrons, which reduce the $\text{Cu}^{2+}$ ions to Cu atoms. Since the etching rate at step edges is much higher than on terrace surfaces, the reduced Cu atoms can selectively adhere along the step edges. To achieve the selective reaction at step edges, dissolved oxygen in the solution must be eliminated, since the dissolved oxygen attacks the atomically flat terrace surface and makes the start points of etching, which enlarges to triangle pits by the following OH$^-$ attack [11]. Further, a large amount of dissolved oxygen enhances growth of chemical oxide, which suppresses the Cu adhesion because of low adhesion rate on SiO$_2$ [12]. In addition, it is known that the dissolved oxygen is reduced to a superoxide anion radical, $\text{O}_2^-$ [11]. One electron is transferred from Cu$^{1+}$, which appear as intermediate state in the reduction process quoted above, to $\text{O}_2^-$ with the abstraction of two protons from water molecules to form hydrogen peroxide [13]. Oxidation of Cu ions prevents Cu adsorption on Si substrates. Actually, no Cu wire was formed in the solution with saturated amount of dissolved oxygen [14].

3.2. Step control

To apply the selective growth characteristics of Cu atoms at atomic step edges to the industrial electronic devices, configuration and position of the steps should be controlled before Cu nanowire fabrication. However, in the method described above, the step position and configuration cannot be controlled. As each unit device is surrounded with SiO$_2$ isolation, information of whether SiO$_2$ pattern can control positions of the atomic step very useful. SiO$_2$ fine line patterns can be drawn by anodic oxidation using AFM probes [8]. It is reported that the step/terrace structures can be also formed by immersion of the Si(111) wafers in the NH$_4$F solution [15]. However, it is difficult to apply the NH$_4$F solution to formation of the well-defined step/terrace Si surface surrounded by the SiO$_2$ isolation because of its high etching-rate for the SiO$_2$ films. On the other hand, the LOW treatment is appropriate to flattening of the Si surface surrounded by the SiO$_2$ isolation, since the SiO$_2$ etching rate is quite low in the solution.

To investigate step flow aspect during Si etching, the well-defined step/terrace structure was used before drawing SiO$_2$ line pattern. The step/terrace surface was obtained by LOW treatment. Then the surface was modified with SiO$_2$ pattern, followed by LOW treatment again. Fig. 3 shows a 1 $\mu$m $\times$ 1 $\mu$m AFM image obtained after Si etching in the LOW with existence of a square SiO$_2$ pattern. The white square line is the SiO$_2$ pattern drawn by anodic oxidation with an AFM probe.

Fig. 2. The amount of Cu atoms on the Si(111) surfaces obtained by TXRF after immersion in the Cu-contained solution as a function of the step density. The correlation factor between the amount and step density is approximately 1.

Fig. 3. A 1 $\mu$m $\times$ 1 $\mu$m AFM image obtained after Si etching in the LOW with existence of a square SiO$_2$ pattern. The white square line is the SiO$_2$ pattern drawn by anodic oxidation with an AFM probe.
rotated from the others. This direction shift was occurred probably because the step flow was interfered by SiO₂ region at certain points on the steps. These results indicate that SiO₂ patterns are useful to control positions of the Si atomic steps during step-flow etching in the LOW. With combination of the SiO₂ fence pattern, which rejects invasion of the outside steps, and the pattern for step-flow pinning, achievement of completely artificial step configurations in the area is expected.

4. Summary

In summary, the Si(111) surface with the well-defined step/terrace structures can be easily obtained with high temperature oxidation and immersion in the LOW. It is indicated that nanowires, which consist of mono-atomic Cu rows, selectively grow along atomic step edges on the Si(111) surface. Possibility that positions of the atomic steps are controlled using the fence effect of the SiO₂ patterns is shown. The technique for precise step control has been studied. These two technologies will be important to realize future nanodevices.

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