A New Approach to the PWM Modulation for the Multiphase Matrix Converters Supplying Loads with Open-End Winding

Pawel Szczepankowski 1*, Natalia Strzelecka 2 and Enrique Romero-Cadaval 3

Abstract: This article presents three variants of the Pulse Width Modulation (PWM) for the Double Square Multiphase type Conventional Matrix Converters (DSM-CMC) supplying loads with the open-end winding. The first variant of PWM offers the ability to obtain zero value of the common-mode voltage at the load’s terminals and applies only six switches within the modulation period. The second proposal archives for less Total Harmonic Distortion (THD) of the generated load voltage. The third variant of modulation concerns maximizing the voltage transfer ratio, minimizing the number of switching, and the common-mode voltage cancellation. The discussed modulations are based on the concept of sinusoidal voltage quadrature signals, which can be an effective alternative to the classic space-vector approach. In the proposed approach, the geometrical arrangement of basic vectors needed to synthesize output voltages is built from the less number of vectors, which is equal to the number of the matrix converter’s terminals. The PWM duty cycle computation is performed using only a second-order determinant of the voltages coordinate matrix without using trigonometric functions. A new approach to the PWM duty cycles computing and the load voltage synthesis by 5 × 5 and 12 × 12 topologies has been verified using the PSIM simulation software.

Keywords: square-type matrix converters; pulse width modulation; multiphase systems

1. Introduction

A fully controlled bidirectional semiconductor switch is an element of the Conventional Matrix Converter (CMC) which offers a direct AC–AC voltages conversion with additional input power factor control functionality. This type of converter, in comparison with the more established Voltage Source Inverter (VSI), has certain individual features that determine the innovation of such a solution [1–3]. It does not contain a bulk dc-link capacitor, thus is far more promising in terms of power density with the inherent four-quadrant operation [4,5]. Compared to traditional variable speed drives with CMC, the multi-phase electric motor drive gives some fundamental advantages. These configurations have greater system redundancy because it can operate during some fault conditions, is characterized by the lower torque ripple and lower per-leg converter rating [6]. Furthermore, the operation of multiphase motors is quieter, allowing for the independent control of two or more series/parallel connected motors [7]. Multiphase electric machines can be fed also by the conventional matrix converter with three inputs [8–11]. The matrix topology is also presented as a unit, which control the power flow between the power generator and the electrical grid [12–16]. Multiphase generators have also been used in systems generating electricity such as offshore installations and wind farms [17,18]. Another application of the multiphase matrix converter in straight forward energy conversion is described in [19], where the 6 × 6 CMC and multi-winding transformer have been used to supply variable...
reactive power flow to the power system. A modulation approach based on the model of the $5 \times 5$ matrix converter with fictitious DC-link was shown in conference paper [20].

Multi-phase electric machines, including three-phase and five-phase variants, can be designed as a machine with open stator winding. Such a solution, especially in combination with a CMC, offers some important features. First, the possibility of direct power supply to both ends of the stator phase winding increases the maximum voltage amplitude within the linear range of the PWM modulator [21]. It should be noted here that the output voltage of the CMC cannot exceed the input voltages envelope. A quite frequency discussed problem in drives controlled by power converters, is the common voltage, which can be understood as a voltage measured between the ground potential and a virtually created star point connected with the stator terminals. The common-mode voltage in terminals of AC drives resulting in bearing currents harmful for the motor drive. The use of certain voltage modulation techniques in a matrix converter allows eliminating this problem [5,22–24].

As indicated in the brief introduction multi-phase drives with CMCs are rather niche applications. However, PWM algorithms are the subject of numerous studies, and almost all of the presented algorithms assume ideal sinusoidal input voltage and are designed for machines with the symmetric construction. The application of these methods without consideration of an input voltage asymmetry or the source harmonics in the calculation results in inaccurate load voltage generation. The approach to voltage synthesis proposed in the article takes this aspect into account and allows for the generation of the appropriate load voltage.

Due to a large number of input and output phases, the complexity of PWM algorithms based on the space-vector approach increases significantly. For a single matrix converter with three inputs and three outputs, the number of switch states is $3^3$ (27). In the case of five input, five output converter, it gives $5^5$ (3125) and analogically in drive with the open-end stator winding, the number of states is equal to $5^{10}$. Therefore, the graphical presentation of voltage vectors corresponding to all switch states, at a given moment of time, becomes very unreadable, which makes it problematic to design and elaborate the dedicated PWM algorithms. The works [3,25] show that the synthesis of output voltages in multi-phase systems can be successfully simplified. These methods can be classified to the direct method of modulation. Compared to the transformation proposed by Clarke, the use of the Hilbert transform leads to the reduction of the number of required vectors. Therefore, for the CMC $5 \times 5$ the PWM algorithm can be developed using only 10 vectors. Apart from the modulation methods based on the space-vector approach, a group of methods of direct modulation can be indicated, such as the Venturini solution [1,26,27], while the general Venturini formulas for PWM duty cycles for several multi-phase converters, including square-type matrix converters are presented in [28]. The work in [25] proposes Wachspress formulas, which can be theoretically applied for any number of inputs. The use of either the Venturini solution or the Wachspress functions forces the commutation all switches of the given output cell (shown in the drawing later in the article). This can be explained by the fact that the switch modulating function is continuous, thus results in higher switching losses. All the PWM modulation methods discussed in the article are characterized by a lower number of switching cycles of at most 6 during the modulation period.

The paper is organized as follows. Definitions and principles of the proposed an output voltage synthesis using the DSM-CMC converter are presented in Section 2. This section also presents the method of generating quadrature signals using the Discrete Second-Order Generalized Integrator (DSOGI) structure. Then, the next three sections demonstrate variants of the proposed modulation. Abilities of the input displacement angle control have been also discussed. Results are summarized and discussed in the conclusion section. Due to a huge number of switching elements, the realization of the experimental setup is very expensive. Therefore, the conclusions presented in the article are the result of circuit simulation in PSIM11 software and analytical research only. However, the proposed solution has been verified partially by an experiment and published in [3,25,29].
2. The Principle of an Output Voltage Synthesis in DSM-CMC Converter

The DSM-CMC converter consists of two square-type matrix converters, \( \text{CMC}_P \) and \( \text{CMC}_N \), connected to load terminals as shown in Figure 1, where the simplified diagram of the circuit is depicted. If the number of load phases is equal to \( n \), the total number of bidirectional power electronic switches is equal to \( 2n^2 \). Both converter are connected with the \( n \)-phase AC voltage source \( v_{i1}, v_{i2}, \ldots, v_{in} \). The voltage of the phase \( x \) of the load

\[
v_{ox}(t) = v_{Px}(t) - v_{Nx}(t)
\]

measured at the load terminals, are synthesized by these converters by using the switch group \( h_{11}, h_{21}, \ldots, h_{n1} \).

![Figure 1. Simplified diagram of the square-type double conventional matrix converter.](image)

As can be seen in Figure 2, switches on both sides of one phase of the load make the single commutation cell with two voltage multiplexers, \( s_P \) and \( s_N \), respectively.

![Figure 2. The single commutation cell for DSM-CMC 5 × 5.](image)
2.1. Case of 5 Phases

The number of multiplexer switches is equal to the number of input voltages, and in this case, takes 5. For a better understanding of the proposal, let the further consideration will be focused on $5 \times 5$ topology.

According to the proposed concept of the voltage synthesis described in [3], all input voltages with pulsation $\omega_i$ can be represented as a collection of five rotating vectors:

$$
\mathbf{v}_i = \begin{bmatrix}
v_{i1x} & v_{i1y} \\
v_{i2x} & v_{i2y} \\
v_{i3x} & v_{i3y} \\
v_{i4x} & v_{i4y} \\
v_{i5x} & v_{i5y}
\end{bmatrix}
$$

(2)

with the real

$$
\begin{align*}
v_{i1x} &= V_{i1} \cos(\omega_i t) \\
v_{i2x} &= V_{i2} \cos(\omega_i t - 2\pi/5) \\
v_{i3x} &= V_{i3} \cos(\omega_i t - 4\pi/5) \\
v_{i4x} &= V_{i4} \cos(\omega_i t - 6\pi/5) \\
v_{i5x} &= V_{i5} \cos(\omega_i t - 8\pi/5)
\end{align*}
$$

(3)

and the imaginary parts of coordinates

$$
\begin{align*}
v_{i1y} &= V_{i1} \sin(\omega_i t) \\
v_{i2y} &= V_{i2} \sin(\omega_i t - 2\pi/5) \\
v_{i3y} &= V_{i3} \sin(\omega_i t - 4\pi/5) \\
v_{i4y} &= V_{i4} \sin(\omega_i t - 6\pi/5) \\
v_{i5y} &= V_{i5} \sin(\omega_i t - 8\pi/5)
\end{align*}
$$

(4)

where $V_{i1}, \ldots, V_{i5}$ are the amplitudes of these voltages. Due to the analytic signal concept based on the Hilbert transform, for the pure sinusoidal input waveforms, the imaginary coordinates are just quadrature components and an input voltage vectors collection can be presented as shown in Figure 3 as the symmetric system.

![Figure 3. The collection of five the rotating input vectors.](image)

These coordinates can be determined using the Hilbert filter or obtained through FFT/DFT based operation [30–32]. However, the Hilbert filter and algorithms based on DFT, although are quite accurate, are not the simple solution from code developing point of view. Moreover, error signals in the form of DC offsets, glitches, and momentary voltage sags may occur in measurements. Therefore, the input vector coordinates can be calculated in a different manner. A compromise solution, between accuracy and not complicated
solution, maybe the use of the Double Second-Order Generalized Integrator with loop feedback extension functioned as Orthogonal Signal Generator (DSOGI-OSG), which in the OSG part prevents unexpected resonance and variables overflow. DSOGI-OSG structure in continuous time-domain is presented in Figure 4.

![Figure 4](image)

Figure 4. Double Second-Order Generalized Integrator with loop feedback extension functioned as Orthogonal Signal Generator (DSOGI-OSG) structure in continuous time-domain [33–35]: $V_i$—the input sinusoidal signal, $V_{ix}$—in-phase component of the input signal, $V_{iy}$—the quadrature component of the input signal, $E_i$ the error signal, $k$—the gain block, $\omega_i$—reference pulsation of the input signal, and $\int$ is an integrator block.

The transfer function takes the form of (5) for in-phase output and (6) for orthogonal output, while (7) represents the notch filter equation

\[
\frac{V_{ix}(s)}{V_i(s)} = \frac{k \cdot \omega_i \cdot s}{s^2 + k \cdot \omega_i \cdot s + \omega_i^2} \quad (5)
\]

\[
\frac{V_{iy}(s)}{V_i(s)} = \frac{k \cdot \omega_i^2}{s^2 + k \cdot \omega_i \cdot s + \omega_i^2} \quad (6)
\]

\[
\frac{E_i(s)}{V_i(s)} = \frac{\omega_i^2}{s^2 + k \cdot \omega_i \cdot s + \omega_i^2} \quad (7)
\]

where the parameter $k$ is a value less than unity ($k$ is taken the value of $1/\sqrt{2}$ here), $E_i(s)$ is the error signal, while $\omega_i$ is an input voltage nominal pulsation. If processed signal frequency does not have an exact value, another extension of SOGI structure, called Frequency-Locked Loop (FLL), may be applied [36–38].

The load voltage $v_o$ produced by the single commutation cell, shown in Figure 2, can be analogous represented by two rotating vectors, $v_P$ and $v_N$, as is depicted in Figure 5. Only the geometrical distance of real (indicated by subscript x) coordinates of these vectors produce the load voltage. While the imaginary coordinate (indicated by subscript y) can generate the reactive power flow at the converter input. In general, there exists some degree of freedom for selecting the instantaneous value of this component because it does not influence on the load currents. The article is focused on the cases, which locus of each output vector is straight a circle. This means that a rotating output voltage vector moves along a circular trajectory and this movement can be clockwise or counterclockwise. Four variants of the PWM modulation scheme are shown in Figure 5.

A vector arrangement in Figure 6a, for the given commutation cell, can be presented as the rotating polygon as illustrated in Figure 6b. The polygon surface is named here as the output voltage synthesis field. All the points, which represent output voltage vectors, have to be located inside the synthesis field. Such a geometric arrangement allows for direct application the Wachspress function for the PWM duty cycles calculation [25,28]. However, the number of switching within the modulation period should be minimal, and for this reason, Venturini and Wachpress solution is not suitable. Decreasing the number of switching can be realized by applying the Nearest Three Vectors (NTV) modulation technique, which relays on the selection of a proper triangle in the synthesis field. Figure 6c shows two selected triangles for the voltages generated by CMC_P and CMC_N converters. Note that both points, representing these voltages, are located in their triangular local
synthesis fields. This is the required condition of output voltage synthesizability. The selection of the optimal triangle may consist in finding the appropriate vertex of the synthesis field, which clearly indicates the input vector closest to the output vector. In the case of using NTV technique, this solution is sufficient, because the other two required vectors are adjacent to the selected one. As can be seen, vector \( v_P \) is closest to the vertex number 2, while vector \( v_N \) is closest to vertex 4. All six required PWM duty cycles can be calculated using the smooth interpolation technique, which is, in the discussed case, nothing more than an appropriate triangle area relation for the NTV modulation [3]. An area of the triangle can be computed using the second-order matrix determinant. Thus, an application of that solution only needs coordinates of the triangle vertices. As mentioned earlier, these coordinates can be computed using the DSOGI-OSG block shown in Figure 4.

Figure 5. Four variants of output vectors rotation: (a) CCV-CCV, (b) CV-CV, (c) CCV-CV, and (d) CV-CCV.

Figure 6. The principle of operation: (a) vectors arrangement, (b) synthesis field, and (c) selected triangles.
2.2. Case of 12 Phases

In the case of more input voltages, for example, when the number of inputs is equal to 12, the choice of the optimal triangle is not so obvious. Now, let us consider the graphical vector arrangements for 12 × 12 topology expressed as regular polygon shown in Figure 7a.

![Figure 7. Synthesis field of the 12 × 12 matrix topology (a), the input voltage vectors, and an example reference output voltage \( \vec{v}_{01} \) (b).](image)

One of 12 presented input vectors is referred here as the base vector. It means that the distance—defined as \( r_1 \cdots r_{12} \) and shown in Figure 7b—between this vector and the reference vector \( \vec{v}_{01} \) is the smallest. There are three triangles with a common upper vertex of \( \vec{v}_{01} \) and shown in Figure 7b—between this vector and the input voltage vectors, and an example reference output voltage \( \vec{v}_{01} \).

When the value of transfer voltage ratio \( q = V_o / V_i \) of the 12 × 12 topology, e.g., for CMCp or CMCN, is in the range

\[
\frac{\cos \left( \frac{\pi}{12} \right)}{\cos \left( \frac{\pi}{17} \right)} \leq q \leq \cos \left( \frac{\pi}{12} \right)
\]

a large number of output phases allows generating the output voltage with lower THD, therefore the cost of passive elements can be decreasing. Corresponding simulation results are presented in the further part of the text. PWM duty cycles calculation for CMCp and
CMC_N are explained in two separate subsections. While the two concepts of gating signals generation have been presented in the third subsection.

2.3. PWM Duty Cycles Calculation for CMC_P and Topology 5 × 5

Referred to the triangle \( \Delta_{[1,2,3]} \) in Figure 6, the reference output voltage \( v_P \) is synthesized using 3 switches: \( h_{11}, h_{21}, \) and \( h_{31}. \) Taking into account previous considerations, the following formulas can be proposed for the calculation of PWM duty cycles,

\[
d_{1P} = \xi_P \cdot \left| \begin{array}{ccc} v_{i2x} - v_{1x} & v_{i2y} - v_{1y} \\ v_{12x} - v_{1x} & v_{12y} - v_{1y} \\ \end{array} \right| = \frac{\Delta_{[2,3,3]}}{\Delta_{[1,2,3]}} \tag{12}
\]

\[
d_{3P} = \xi_P \cdot \left| \begin{array}{ccc} v_{i4x} - v_{3x} & v_{i4y} - v_{3y} \\ v_{14x} - v_{3x} & v_{14y} - v_{3y} \\ \end{array} \right| = \frac{\Delta_{[2,3,3]}}{\Delta_{[1,2,3]}} \tag{13}
\]

\[
d_{2P} = 1 - d_{1P} - d_{3P} = \frac{\Delta_{[3,1,1]}}{\Delta_{[1,2,3]}} \tag{14}
\]

where \( \xi_P \) is the scaling factor, which is equal to the triangle \( \Delta_{[1,2,3]} \) surface. Thus, the average value of the CMC_P output voltage can be expressed by the following formula.

\[
\overline{v}_P = d_{1P} \cdot v_{i1} + d_{2P} \cdot v_{i2} + d_{3P} \cdot v_{i3} \tag{16}
\]

2.4. PWM Duty Cycles Calculation for CMC_N and Topology 5 × 5

Referred to the triangle \( \Delta_{[3,4,5]} \) in Figure 6, the reference output voltage \( v_N \) is synthesized by 3 switches: \( h_{31}, h_{41}, \) and \( h_{51}. \) The corresponded duty cycles can be calculate using the following formulas,

\[
d_{3N} = \xi_N \cdot \left| \begin{array}{ccc} v_{i4x} - v_{3x} & v_{i4y} - v_{3y} \\ v_{i5x} - v_{3x} & v_{i5y} - v_{3y} \\ \end{array} \right| = \frac{\Delta_{[4,5,5]}}{\Delta_{[3,4,5]}} \tag{17}
\]

\[
d_{4N} = \xi_N \cdot \left| \begin{array}{ccc} v_{i5x} - v_{4x} & v_{i5y} - v_{4y} \\ v_{i3x} - v_{4x} & v_{i3y} - v_{4y} \\ \end{array} \right| = \frac{\Delta_{[5,5,3]}}{\Delta_{[3,4,5]}} \tag{18}
\]

\[
d_{5N} = 1 - d_{3N} - d_{4N} = \frac{\Delta_{[3,4,4]}}{\Delta_{[3,4,5]}} \tag{19}
\]

where \( \xi_N \) is the scaling factor, which is equal to the triangle \( \Delta_{[3,4,5]} \) surface. The average value of the CMC_N output voltage can be expressed by the following formula.

\[
\overline{v}_N = d_{3N} \cdot v_{i3} + d_{4N} \cdot v_{i4} + d_{5N} \cdot v_{i5} \tag{21}
\]

2.5. The Concept of Gating Signals Generation

The gate signals can be controlled according to different strategies. Apap et al. [39] compared and presented several PWM signal gating methods. Among them, the cyclic Venturini and Min-Mid-Max (MMM) schemes of modulation are proposed. Two approaches have been applied to the gates signal generation: basic and mentioned MMM scheme.
In the case of the basic solution, the sequences of the switch states always depend on the selected triangle in which the synthesis of the output voltage is realized. Therefore, these sequences can be placed in a lookup table. An overview of the basic sequences is shown in Figure 8, where the value of $\varphi \approx 1.618$, which is so-called the golden ratio exists in the pentagon.

![Switch state sequences](image)

(a) sequences type I for $q \in \langle 1/(1 + \varphi), \cos(\pi/5) \rangle$

(b) sequences type II for $q \in (0, 1/(1 + \varphi))$

**Figure 8.** The switch state sequences in the basic solution of the gating signals for both converter cells $CMC_P$ and $CMC_N$.

The MMM method is used to improve the quality of the voltage generated by the converter in terms of THD. The switch states sequences for the $CMC_P$ and $CMC_N$ converters are characterized in Figure 9. Note that these sequences correspond to the case illustrated in Figure 6b.
3. The PWM Variant 1—An Output Voltage Synthesis with Zero Value of the Common-Mode Voltage

The common-mode voltage, defined as

$$v_{cm}(t) = \frac{(v_{o1}(t) + v_{o2}(t) + v_{o3}(t) + v_{o4}(t) + v_{o5}(t))}{5},$$  \hspace{1cm} (22)$$
can lead to the degradation of rolling bearings in electric machines powered by PWM inverters. As indicated in the introduction an open-end windings stator fed by the double matrix converter allows for the PWM modulation without the common-mode voltage generation. The proposed approach to the load voltage synthesis with conjunction with the basic solution of the gating signals control (shown in Figure 8) gives the same desired result. Elimination of the common-mode voltage can be performed by all PWM modulation schemes: CV-CV, CCV-CCV, CV-CCV, and CCV-CV. The use of the first two cases allows obtaining an input displacement angle, which is dependent on the load parameters like in the Venturini methods [1,26].

The referenced $k$-output voltage vectors of the CCV-CCV modulation scheme can be expressed by following equations.

$$v_{P_{dk}} = q \cdot \cos(\omega_o t - ((k - 1) \cdot 2\pi/5))$$  \hspace{1cm} (23)$$

$$v_{P_{yk}} = -q \cdot \sin(\omega_o t - ((k - 1) \cdot 2\pi/5))$$  \hspace{1cm} (24)$$

$$v_{N_{dk}} = -q \cdot \cos(\omega_o t - ((k - 1) \cdot 2\pi/5))$$  \hspace{1cm} (25)$$

$$v_{N_{yk}} = q \cdot \sin(\omega_o t - ((k - 1) \cdot 2\pi/5))$$  \hspace{1cm} (26)$$

Above equation are proposed for the first commutation cell. Equations for the rest of the rotating vectors pairs can be represented by analogous elaboration. The referenced output voltages in CV-CV scheme can be represented by following equations.

$$v_{P_{dk}} = q \cdot \cos(\omega_o t - ((k - 1) \cdot 2\pi/5))$$  \hspace{1cm} (27)$$

**Figure 9.** The MMM type of sequences of the gating signals for both converter cells CMC$_P$ and CMC$_N$ for the case depicted in Figure 6c.
\( v_{Pyk} = q \cdot \sin(\omega_o \cdot t - ((k - 1) \cdot 2\pi / 5)) \) (28)
\( v_{Nxk} = -q \cdot \cos(\omega_o \cdot t - ((k - 1) \cdot 2\pi / 5)) \) (29)
\( v_{Nyk} = -q \cdot \sin(\omega_o \cdot t - ((k - 1) \cdot 2\pi / 5)) \) (30)

The possibility to change the rotation of the given output vector by changing the sign of the imaginary component allows realizing the PWM modulation, in which the resultant imaginary component of the \( v_{oiy} \) takes the zero value. If vectors \( \vec{i}_P \) and \( \vec{i}_N \) rotate in opposite directions, as is typical for last two presented schemes of modulation CV-CCV and CCV-CV, the passive input current component is not generated. Simulation results of the PWM variant 1 for DSM-CMC 5 × 5 and four modulation schemes are shown in Figure 10. Simulation parameters are listed in Table A1, which can be found in an appendix.

Figure 10. Simulation of the PWM variant 1 for DSM-CMC 5 × 5 and four modulation schemes—RL load case.

Analogous simulation tests have been realized for the proposed converter connected to a 12-phase symmetrical power supply. Figure 11 shows the load voltage generated by DSM-CMC 12 × 12 for an output frequency equal to 10 Hz, while results obtained for 300 Hz are presented in Figure 12.

Simulation parameters for this case are available in Table A2 in Appendix A. The selection of different sets of simulation parameters did not subserve a specific purpose. The simulation tests were carried out with the use of two independent simulation files. However, in the case of the DSM-CMC 12 × 12 simulation, a small calculation step was chosen due to the high modulation frequency. It was set to 100 kHz to get a good PWM resolution at 300 Hz of the fundamental frequency.
Properties of this type of matrix converter, compared with counterpart $5 \times 5$, remains the same. In particular, the common-mode voltage is also eliminated by using the basic type of switches state sequences. The voltages shown in these figures are characterized by a low THD, which is about 12%. Comparing to the $5 \times 5$ topology, the resulted voltage gain for DSM-CMC is higher and takes optimally the value of 1.93.

4. The PWM Variant 2—An Output Voltage Synthesis with Less Harmonic Distortion

The basic solution of the switch states sequence has been applied in the PWM modulation with eliminating the common-mode voltage. If a lower THD of the load voltage waveform is desired, a more advanced gating signal generation mechanism can be proposed, such as MMM scheme shown in Figure 9. With regard to variant 1, this is the only change. However, the MMM method is more complicated because the input voltage vector collection should be arranged in a specific order $\{\text{min} - \text{mid} - \text{max} - \text{mid} - \text{min}\}$ within the selected triangular synthesis field. Simulation results are presented in Figure 13.
A lower THD of the load voltage $v_o$ is obtained but the common-mode voltage $v_{cm}$ is also generated, as marked in the presented drawings.

Figure 13. Simulation of the PWM variant 2 for DSM-CMC 5 × 5 and four modulation schemes: $f_o = 250$ Hz, $q = 2 \times 0.8$.

5. The PWM Variant 3—An Output Voltage Synthesis with Maximum Voltage Transfer Ratio and Minimum Number of Switching

A synthesis field for multi-phase and symmetrical AC voltage sources can be represented by a regular polygon as shown in Figures 6b and 7a. A radius of a circle inscribed of this polygon limits an output voltage amplitude in the linear range of modulation. The maximum voltage transfer ratio for CMC$_N$ and CMC$_P$, related to the input voltage amplitude and number of inputs equal to $n$, can be expressed as follows,

$$q_{P_{\text{max}}} = q_{N_{\text{max}}} = \cos\left(\frac{\pi}{n}\right)$$  \hspace{1cm} (31)$$

Therefore, the maximum load voltage for DSM-CMC 5 × 5 in p.u. is equal to

$$v_{o_{\text{max}}} = 2 \cdot \cos\left(\frac{\pi}{5}\right) = 1.618$$  \hspace{1cm} (32)$$

The value (32) can be increased by modifying the position of the $v_P$ and $v_N$ vectors. In contrast to the methods described in the previous sections, trajectories of these vectors are not a circle. The locus of each vector is not changing smoothly and contains discontinuities. This type of modulation belongs to the discontinuous group of PWM modulations. Both reference vectors $v_P$ and $v_N$ take exactly five positions, in which they lie on one of five input vectors. An algorithm flowchart for DSM-CMC 5 × 5 is presented in Figure 14.
Figure 14. An algorithm flowchart of the variant 3 PWM modulation: (a) Step 1: generation of synthesis field and reference voltage vectors $v_P$ and $v_N$. (b) Step 2: calculation of the set of distances between the N point and vertices of the synthesis field. (c) Step 3: calculation of the set of distances between the P point and vertices of the synthesis field. (d) Step 4: shortest distance selection, setting the origin vertex, and the vector’s offset $\{v_{sx}, v_{sy}\}$ calculation. (e) Step 5: the reference vector $v_o$ shift resulting in the new coordinates of $P$ and $N$ points. (f) Step 6: calculation of four areas of the triangle and PWM duty cycles.

The output voltage synthesis field is generated using the DSOGI blocks at the first step of the proposed algorithm. The reference output voltage vectors coordinates, $\{v_{Nx}, v_{Ny}\}$ and $\{v_{Px}, v_{Py}\}$, are also calculated at this step. The vectors can rotate clockwise (CV-CV scheme) or counterclockwise (CCV-CCV scheme), as shown in Figure 15.

Figure 15. An example rotation of the reference output vector.
Based on the analysis of the vector arrangement in Figure 15, it can be written that the maximum length of the voltage vector, in a linear range of modulation, is equal to the following expression.

\[ v_{o \text{max}} (\text{variant3}) = 1 + \cos\left(\frac{\pi}{5}\right) = 1.809 \]  \hspace{1cm} (33)

However, a vector of this length has to be accordingly shifted inside the synthesis field as shown in Figure 14d,e. Therefore, new coordinates of the reference output vector for the given commutation cell can be calculated as follows.

\[ v_{osx} = v_{ox} + v_{sx} \] \hspace{1cm} (34)

\[ v_{osy} = v_{oy} + v_{sy} \] \hspace{1cm} (35)

Distances between N-point and all the synthesis field vertices are calculated in Step 2. The same procedure is applied for the point P in Step 3. Next, the shortest calculated distance in a N-collection \( \{ r_{N1}, r_{N2}, r_{N3}, r_{N4}, r_{N5} \} \) is compared with the shortest calculated distance in a P-collection \( \{ r_{P1}, r_{P2}, r_{P3}, r_{P4}, r_{P5} \} \). Finally, the less value is selected, which correctly indicates the optimal vertex of the synthesis field. The shift coordinates are calculated in Step 4. As can be seen in Figure 14d, vertex number 4 has been chosen. Thus, the PWM duty cycles, for the case illustrated in Figure 14f can be calculated using the following formulas.

\[ d_{1Ps} = \frac{\Delta[2,Ps,4]}{\Delta[1,2,4]} \] \hspace{1cm} (36)

\[ d_{2Ps} = \frac{\Delta[4,Ps,1]}{\Delta[1,2,4]} \] \hspace{1cm} (37)

\[ d_{4Ps} = \frac{\Delta[1,Ps,2]}{\Delta[1,2,4]} \] \hspace{1cm} (38)

and

\[ d_{4Ns} \equiv 1 \] \hspace{1cm} (39)

Formula (39) refers to the case where the end of the \( v_N \) vector coincides with the \( v_{i4} \) vector. It means the permanent connection of the input voltage \( v_{i4} \) with one side of the load phase during the PWM modulation period. Figure 15 shows a case, which in the one side of the load is permanently connected to an input voltage \( v_{i1} \) during PWM modulation. Sequences of the switch states shown in Figure 16 correspond to the case, which in the \( s_N \) switch is connected permanently to the input phase 4. The zero load voltage is generated by using the same switch in both CMC\( P \) and CMC\( N \) matrix converters. Simulation results for maximal voltage transfer ratio (33) are shown in Figure 17. The common-mode voltage \( v_{cm} \) is eliminated. An application of the CV-CV and CCV-CCV scheme of modulation resulting in the non-zero input displacement angle.

![Figure 16](image_url)

**Figure 16.** Sequences of the switch states in one commutation cell for the case presented in Figure 14.
Having half the number of switching operations during the PWM modulation period is an advantage of variant 3. In order to obtain the unity power factor at the system input, the sequence types have to be toggled continuously in the order CV-CV, CCV-CCV, ..., etc. However, this mode of operation may require to redesign of an input filter. Example simulation results of the PWM variant 3 with toggling mode for DSM-CMC 5 × 5 have been presented in Figure 18.

![Simulation of the PWM variant 3 for DSM-CMC 5 × 5 and two modulation schemes: \( f_o = 250 \text{ Hz}, q = 1.8 \).](image)

**Figure 17.** Simulation of the PWM variant 3 for DSM-CMC 5 × 5 and two modulation schemes: \( f_o = 250 \text{ Hz}, q = 1.8 \).

**Figure 18.** Simulation of the PWM variant 3 with toggling mode for DSM-CMC 5 × 5.

### 6. Summary and Conclusions

This paper presents a new approach to the PWM modulation for the multi-phase matrix converters supplying loads with open-end winding. The proposed approach is an alternative for the methods based on the space-vector modulation. Three variants of PWM modulation were presented. Animations for the first two of them are available at IEEE DataPort data set [40]. The first variant allows for eliminating the common-mode voltage, which is a desired feature from a practical point of view. The second variant based on a specific rearranging switches state sequences can offer quasi-multilevel waveforms with low THD. However, a common-mode voltage level can be unaccepted due to influence on the bearings lifetime. Variant 3 of the PWM modulation described in a paper offer over 12% greater voltage transfer gain. Comparison of an input angle value for the proposed variants of PWM modulation is presented in Table 1.
Table 1. Comparison of an input angle value for the proposed variants of PWM modulation.

| PWM Variant | Modulation Scheme | $\phi_i = \phi_o$ | $\phi_i = -\phi_o$ | $\phi_i = 0$ |
|-------------|-------------------|-------------------|-------------------|--------------|
| variant 1   | CCV-CCV           | CV-CV             | CV-CCV or CCV-CV   |              |
| variant 2   | CCV-CCV           | CV-CV             | CV-CCV or CCV-CV   |              |
| variant 3   | CCV-CCV           | CV-CV             | toggling           |              |

The multi-phase matrix converters, with an equal number of input and outputs, belong to the niche solution. Recently, we can observe an increasing interest in multi-phase systems. Furthermore, the complexity of the modulation algorithms grows up. The described proposal is a research result of analytic signal and an application of the smooth interpolation method in PWM duty cycle computing. Some selected features and properties have been compared with the space-vector method. Table 2 presents such a comparison. The PWM duty cycle computation represented by equations, from (12) to (14), is performed using only a second-order determinant of the voltages coordinate matrix without trigonometry usage. Therefore, the proposed method also naturally extends the applicability of the formulas to unbalanced and distorted AC voltage sources. Moreover, all computation can be realized in the FPGA structure using the simple multipliers and adders. The important contribution of the presented article is a presentation of the novel algorithm, which is much easier than algorithms based on the space-vector approach. This property is essential in multi-phase systems because the number of vectors is very high. The proposed solution uses only vectors that represent the Hilbert analytic signal pair calculated for the input and the reference vectors. The number of vectors needed to realize the output voltage synthesis is equal to only the sum of input and output phases.

Table 2. The comparison of the proposed modulation with the space-vector approach.

| Proposed Modulation | Space Vector Modulation |
|---------------------|-------------------------|
| how the vector map is generated | using the analytic signal concept, which is based on the Hilbert transform | using the Clark transform for multi-phase systems |
| the difficulty of the vector map generator | comparable with SVPWM, using several methods: triple Clarke, or DSOGI, or DFT | comparable with the proposed, using the Clarke rotation operator |
| degree of difficulty with more phases | the number of vectors is equal to the number of converter’s terminals | the number of vectors is equal to $2^{2P}$, where $P$ is the number of the load phase |
| the common-mode voltage elimination in the multi-phase systems | yes | requires the modification of the modulation using the rotating vectors collection |
| minimization of the number of switching | possible for variant no. 3, in the general case a sorted and optimized the switch states sequence should be used | the minimization of the number of switching is a natural feature for the space-vector modulation, which is based on the nearest three vectors, however—for that selection can be an additional issue of computation |
| is it applicable for unbalanced and asymmetrical loads with the open-winding | yes | no applicable, space-vector methods assumed the symmetric loads with the open-winding |
| the load phase failure | ready for that failure, each load phase is controlled by an individual and independence the cell controller | in the event of the sudden change in the number of load phases, the algorithm (switches’ state sequences table) must be thoroughly rebuilt, it is not possible in a real-time system, the modification can only be implemented offline |
| application of trigonometric functions for PWM duty cycle computing | no (it speeds up the algorithm) | yes |
Author Contributions: The concept, algorithmization, simulation studies, P.S.; simulation results verification and presubmission editing, E.R.-C. and N.S. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the LINTE^2 Laboratory, Gdansk University of Technology.

Conflicts of Interest: All authors declare no conflict of interest.

Appendix A. Simulation Parameters

Table A1. Simulation parameters for DSM-CMC 5 × 5.

| Parameter                                      | Value                                      |
|------------------------------------------------|--------------------------------------------|
| Number of input voltages                       | 5                                          |
| Number of output voltages                      | 10                                         |
| Number of an ideal bidirectional switches      | 50                                         |
| Source phase voltage amplitude                  | $V_i = 100$ V                              |
| Input frequency                                 | $f_i = 50$ Hz                              |
| Output frequencies                              | $f_o = 10$ Hz, 250 Hz                      |
| Voltage gain of CMC_P                          | $q = 0.8$                                  |
| Voltage gain of CMC_N                          | $q = 0.8$                                  |
| The load parameters                            | $R_o = 0.5$ Ω, $L_o = 1$ mH                |
| An algorithm frequency                         | $f_s = 10$ kHz                             |
| Simulation step                                 | 250 ns                                     |
| Simulation software                             | PSIM 64-bit Version 11.0.3                 |

Table A2. Simulation parameters for DSM-CMC 12 × 12.

| Parameter                                      | Value                                      |
|------------------------------------------------|--------------------------------------------|
| Number of input voltages                       | 12                                         |
| Number of output voltages                      | 24                                         |
| Number of an ideal bidirectional switches      | 288                                        |
| Source phase voltage amplitude                  | $V_i = 100$ V                              |
| Input frequency                                 | $f_i = 50$ Hz                              |
| Output frequencies                              | $f_o = 10$ Hz, 300 Hz                      |
| Voltage gain of CMC_P                          | $q = 0.95$                                 |
| Voltage gain of CMC_N                          | $q = 0.95$                                 |
| The load parameters                            | $R_o = 10$ Ω, $L_o = 0.1$ mH               |
| An algorithm frequency                         | $f_s = 100$ kHz                            |
| Simulation step                                 | 100 ns                                     |
| Simulation software                             | PSIM 64-bit Version 11.0.3                 |

Simulation research has been performed for symmetric and balanced source and load. Obtained currents and voltages have been presented as p.u. values referred to the base voltage $V_{base} = V_i$ and the base current equal to $I_{base} = V_i/Z_o$, where $Z_o$ was a load impedance.

References

1. Rodriguez, J.; Rivera, M.; Kolar, J.W.; Wheeler, P.W. A Review of Control and Modulation Methods for Matrix Converters. *IEEE Trans. Ind. Electron.* 2012, 59, 58–70. [CrossRef]
2. Friedli, T.; Kolar, J.W. Milestones in Matrix Converter Research. *IEEE J. Ind. Appl.* 2012, 1, 2–14. [CrossRef]
3. Szczepankowski, P.; Wheeler, P.; Bajdecki, T. Application of Analytic Signal and Smooth Interpolation in Pulsewidth Modulation for Conventional Matrix Converters. *IEEE Trans. Ind. Electron.* 2020, 67, 10011–10023. [CrossRef]
4. Helle, L.; Larsen, K.B.; Jorgensen, A.H.; Munk-Nielsen, S.; Blaabjerg, F. Evaluation of modulation schemes for three-phase to three-phase matrix converters. *IEEE Trans. Ind. Electron.* 2004, 51, 158–171. [CrossRef]
5. Ahmed, S.M.; Abu-Rub, H.; Salam, Z. Common-Mode Voltage Elimination in a Three-to-Five-Phase Dual Matrix Converter Feeding a Five-Phase Open-End Drive Using Space-Vector Modulation Technique. *IEEE Trans. Ind. Electron.* **2015**, *62*, 6051–6063. [CrossRef]

6. Levi, E.; Bojoi, R.; Profumo, F.; Toliyat, H.; Williamson, S. Multi-phase induction motor drives-A technology status review. *IET Elect. Power Appl.* **2007**, *1*, 489–516. [CrossRef]

7. Levi, E. Multi-phase Machines for Variable speed applications. *IEEE Trans. Ind. Electron.* **2008**, *55*, 1893–1909. [CrossRef]

8. Nguyen, T.D.; Lee, H. Development of a Three-to-Five-Phase Indirect Matrix Converter With Carrier-Based PWM Based on Space-Vector Modulation Analysis. *IEEE Trans. Ind. Electron.* **2016**, *63*, 13–24. [CrossRef]

9. Ahmed, S.M.; Salam, Z.; Abu-Rub, H. An Improved Space Vector Modulation for a Three-to-Seven-Phase Matrix Converter With Reduced Number of Switching Vectors. *IEEE Trans. Ind. Electron.* **2015**, *62*, 3327–3337. [CrossRef]

10. Ahmed, S.M.; Iqbal, A.; Abu-Rub, H.; Rodriguez, J.; Rojas, C.; Saleh, M. Simple carrier-based PWM technique for a three-to-nine phase direct AC-AC converter. *IEEE Trans. Ind. Electron.* **2011**, *58*, 5014–5023. [CrossRef]

11. Ahmed, S.M.; Iqbal, A.; Abu-Rub, H. Generalized Duty-Ratio-Based Pulselithth Modulation Technique for a Three-to-k Phase Matrix Converter. *IEEE Trans. Ind. Electron.* **2011**, *58*, 3925–3937. [CrossRef]

12. El-Khoury, C.N.; Kanaan, H.Y.; Mouhtarbel, I.; Al-Haddad, K. A review of matrix converters applied to PMSG based wind energy conversion systems. In *Proceedings of the IECON 2013—39th Annual Conference of the IEEE Industrial Electronics Society*, Vienna, Austria, 10–13 November 2013; pp. 7784–7789. [CrossRef]

13. Liu, X.; Wang, P.; Loh, P.; Blaabjerg, F. A Three-Phase Dual-Input Matrix Converter for Grid Integration of Two AC Type Energy Resources. *IEEE Trans. Ind. Electron.* **2013**, *60*, 20–29. [CrossRef]

14. Pena, R.; Cardenas, R.; Reyes, E.; Clare, J.; Wheeler, P. Control of a Doubly Fed Induction Generator via an Indirect Matrix Converter With Changing DC Voltage. *IEEE Trans. Ind. Electron.* **2011**, *58*, 20–29. [CrossRef]

15. Garces, A.; Molinas, M. A Study of Efficiency in a Reduced Matrix Converter for Offshore Wind Farms. *IEEE Trans. Ind. Electron.* **2012**, *59*, 184–193. [CrossRef]

16. Abdel-Rahim, O.; Funato, H.; Abu-Rub, H.; Ellabban, O. Multiphase Wind Energy generation with direct matrix converter. In *Proceedings of the 2014 IEEE International Conference on Industrial Technology (ICIT)*, Busan, Korea, 26 February–1 March 2014; pp. 519–523. [CrossRef]

17. Yaramasu, V.; Wu, B.; Sen, P.C.; Kouro, S.; Narimani, M. High-power wind energy conversion systems: State-of-the-art and emerging technologies. *Proc. IEEE* **2015**, *103*, 740–788. [CrossRef]

18. Zoric, I.; Jones, M.; Levi, E. Arbitrary Power Sharing Among Three-Phase Winding Sets of Multiphase Machines. *IEEE Trans. Ind. Electron.* **2018**, *65*, 1128–1139. [CrossRef]

19. Sienko, T.; Szczepaniak, J.; Martis, C. Reactive Power Transfer via Matrix Converter Controlled by the “One Periodical” Algorithm. *Energies* **2020**, *13*, 665. [CrossRef]

20. Rezaoui, M.M. Study of output voltages of a matrix converter feeding an five AC-induction machine using the strategy calculated modulation PMW. In *Proceedings of the 2010 Modern Electric Power Systems*, Wroclaw, Poland, 20–22 September 2010; pp. 1–4.

21. Rahman, K.; Iqbal, A.; Al-Hitmi, M.A.; Dordevic, O.; Ahmad, S. Performance Analysis of a Three-to-Five Phase Dual Matrix Converter Based on Space Vector Pulse Width Modulation. *IEEE Access* **2019**, *7*, 12307–12318. [CrossRef]

22. Baranwal, R.; Basu, K.; Mohan, N. Carrier-Based Implementation of SVPWM for Dual Two-Level VSI and Dual Matrix Converter With Zero Common-Mode Voltage. *IEEE Trans. Power Electron.* **2015**, *30*, 1471–1487. [CrossRef]

23. Tewari, S.; Mohan, N. Matrix Converter Based Open-End Winding Drives With Common-Mode Elimination: Topologies, Analysis, and Comparison. *IEEE Trans. Power Electron.* **2018**, *33*, 8578–8595. [CrossRef]

24. Raza, J.; Sztajnec, E. Elimination of Common Mode Voltage in the Three-To-Nine-Phase Matrix Converter. *Energies* **2020**, *13*, 631. [CrossRef]

25. Szczepanowski, P.; Bajdecki, T.; Strzelecki, R. Direct Modulation for Conventional Matrix Converters Using Analytical Signals and Barycentric Coordinates. *IEEE Access* **2020**, *8*, 22592–22616. [CrossRef]

26. Malekjamshidi, Z.; Jafari, M.; Zhu, J. Analysis and comparison of direct matrix converters controlled by space vector and Venturini modulations. In *Proceedings of the 2015 IEEE 11th International Conference on Power Electronics and Drive Systems*, Sydney, Australia, 9–12 June 2015; pp. 635–639. [CrossRef]

27. Dey, A.K.; Mohapatra, G.; Mohapatra, T.K.; Sharma, R. A Modified Venturini PWM scheme for Matrix converters. In *Proceedings of the 2019 IEEE International Conference on Emerging Energy Technologies and Systems (ICSETS)*, Bhubaneswar, India, 6–9 March 2019; pp. 467–471. [CrossRef]

28. Ali, M.; Iqbal, A.; Khan, M.R.; Ayyub, M.; Anees, M.A. Generalized Theory and Analysis of Scalar Modulation Techniques for a m × n Matrix Converter. *IEEE Trans. Power Electron.* **2017**, *32*, 4864–4877. [CrossRef]

29. Szczepanowski, P.; Nieznanowski, J. Application of Barycentric Coordinates in Space Vector PWM Computations. *IEEE Access* **2019**, *7*, 91499–91508. [CrossRef]

30. Reilly, A.; Frazier, G.; Boashash, B. Analytic signal generation-Tips and traps. *IEEE Trans. Signal Process.* **1994**, *42*, 3241–3245. [CrossRef]

31. Marple, L. Computing the discrete-time “analytic” signal via FFT. *IEEE Trans. Signal Process.* **1999**, *47*, 2600–2603. [CrossRef]
33. Yan, Q.; Zhao, R.; Yuan, X.; Ma, W.; He, J. A DSOGI-FLL-Based Dead-Time Elimination PWM for Three-Phase Power Converters. *IEEE Trans. Power Electron.* 2019, 34, 2805–2818. [CrossRef]

34. Xin, Z.; Zhao, R.; Blaabjerg, F.; Zhang, L.; Loh, P.C. An Improved Flux Observer for Field-Oriented Control of Induction Motors Based on Dual Second-Order Generalized Integrator Frequency-Locked Loop. *IEEE J. Emerg. Sel. Top. Power Electron.* 2017, 5, 513–525. [CrossRef]

35. Hoffmann, N.; Lohde, R.; Fischer, M.; Fuchs, F.W.; Asiminoaei, L.; Thøgersen, P.B. A review on fundamental grid-voltage detection methods under highly distorted conditions in distributed power-generation networks. In Proceedings of the 2011 IEEE Energy Conversion Congress and Exposition, Phoenix, AZ, USA, 17–22 September 2011; pp. 3045–3052.

36. Rodriguez, P.; Luna, A.; Ciobotaru, M.; Teodorescu, R.; Blaabjerg, F. Advanced Grid Synchronization System for Power Converters under Unbalanced and Distorted Operating Conditions. In Proceedings of the IECON 2006—32nd Annual Conference on IEEE Industrial Electronics, Paris, France, 6–10 November 2006; pp. 5173–5178.

37. Patil, K.R.; Patel, H.H. Modified dual second-order generalised integrator FLL for synchronization of a distributed generator to a weak grid. In Proceedings of the 2016 IEEE 16th International Conference on Environment and Electrical Engineering (EEEIC), Florence, Italy, 7–10 June 2016; pp. 1–5.

38. He, X.; Geng, H.; Yang, G. A Generalized Design Framework of Notch Filter Based Frequency-Locked Loop for Three-Phase Grid Voltage. *IEEE Trans. Ind. Electron.* 2018, 65, 7072–7084. [CrossRef]

39. Apap, M.; Clare, J.; Wheeler, P.; Bradley, K. Analysis and comparison of AC-AC matrix converter control strategies. In Proceedings of the IEEE 34th Annual Conference on Power Electronics Specialist, Acapulco, Mexico, 15–19 June 2003; pp. 1287–1292. [CrossRef]

40. Szczepankowski, P. A new approach to the PWM modulation for the double, square-type, conventional matrix converters supplying loads with open-end winding. *IEEE Dataport* 2020. [CrossRef]