DIVE INTO BIG MODEL TRAINING

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ABSTRACT

The increasing scale of model size and continuous improvement of performance herald the arrival of the Big Model era. In this report, we explore what and how the big model training works by diving into training objectives and training methodologies. Specifically, training objectives describe how to leverage web-scale data to develop extremely capable and incredibly large models based on self-supervised learning, and training methodologies which are based on distributed training describe how to make big model training a reality. We summarize the existing training methodologies into three main categories: training parallelism, memory-saving technologies, and model sparsity design. Training parallelism can be categorized into data, pipeline, and tensor parallelism according to the dimension of parallelism that takes place. Memory-saving technologies are orthogonal and complementary to training parallelism. And model sparsity design further scales up the model size with a constant computational cost. A continuously updated paper list of big model training is provided\textsuperscript{1}.

Index Terms: Deep Learning, Distributed Training, Training Parallelism

1. INTRODUCTION

The past several years have witnessed the scale of the model increase as datasets become larger and large-scale computation becomes more available. The rise of self-supervised learning algorithms has enabled models to unleash the power of extensive unlabeled datasets and become the carriers of intelligence. The pros- perous training methodologies, including training parallelism and memory-saving technologies, make it possible to train outrageously large neural networks on many GPUs in an efficient manner. The term Big Model refers to a big data-driven and multi-domain capable model with a large number of parameters. And the training objective describes how to leverage broad data to transform deep neural network architecture into a big model with the help of large-scale computing power.

1.1. Development of Big Model Scale

The number of parameters of deep neural networks has been growing rapidly in recent years. As shown in Table 1, the model size grows over time. Since the advent of the GPT series, the era of Big Model has begun.

According to [4], Megatron-LM uses 32 DGX-2H servers (a total of 512 Tesla V100 GPUs) to scale transformer-based models up to 8.3 billion parameters based on tensor parallelism (Sec 4.3). ZeRO (Sec 5.3) proposed by Rajbhandari et al. in [5] could fit

\begin{table}[h]
\centering
\begin{tabular}{|l|c|c|}
\hline
Name & \#Param & Date \\
\hline
GPT [1] & 110 million & Jun 2018 \\
BERT [2] & 340 million & Oct 2018 \\
GPT-2 [3] & 1.5 billion & Feb 2019 \\
Megatron-LM [4] & 8.3 billion & Sep 2019 \\
Switch Transformer [7] & 1.6 trillion & Jan 2021 \\
BaGuaLu [8] & 174 trillion & April 2021 \\
Megatron-Turing NLG [9] & 530 billion & Jan 2022 \\
PaLM [10] & 540 billion & April 2022 \\
\hline
\end{tabular}
\caption{Large-scale models released in recent years.}
\end{table}

than 1 trillion parameters on 1024 GPUs with model and data parallelism. However, it is only on a theoretical level and due to resource constraints, they actually train a 17B language model with state-of-the-art performance and the largest model size by that time. The first Trillion-scale parameter model Switch Transformer [7] which is based on the mixture-of-experts algorithm (Sec 6) has come out in 2021. In the same year, the number of parameters in Bagualu [8] reached a record-breaking 174 trillion, which even rivals the number of synapses in a human brain.

1.2. Why Big Model Prospers

The upper limit of the parameter scale has been broken over the past few years along with the state-of-the-art performance. The reasons for the continued interest in Big Model include the following:

\textbf{Big Model performs better.} Intuitively, the best performers on the standard dataset are basically pre-trained Big Models. By scaling up the model size, big models benefit from significant performance improvements across a wide range of machine learning problems [11, 12, 3, 4]. Kaplan et al. [13] from OpenAI demonstrate exhaustively that model performance depends strongly on scale and has a power-law relationship with the number of parameters, size of the dataset, and amount of computing. This study further suggests that larger models will continue to perform better.

\textbf{Big Model is more capable.} The Big Model shows the ability to adapt to multiple downstream tasks after being pretrained on a large amount of data. The multiple downstream tasks and data requirements are trivial and long-tailed distribution. Standard pre-training and fine-tuning paradigm [14] generally require updating the entire model weight. As we scale the parameter size from GPT-2 (1.5B) to GPT-3 (175B), GPT-3 becomes a few-shot learner which can better achieve downstream task adaptation without fine-tuning. In particular, it can be adapted via natural language prompts to do a passable job on a wide range of tasks despite not being trained explicitly to do many of those tasks.
1.3. Challenges in Big Model training

| Name     | #Param | Dataset Size | Time     |
|----------|--------|--------------|----------|
| GPT [1]  | 110M   | 4GB          | 3 days   |
| BERT [2] | 340M   | 16GB         | 50 days  |
| GPT-2 [3]| 1.5B   | 40GB         | 200 days |
| GPT-3 [6]| 175B   | 560GB        | 90 years |

The significant performance improvement by bigger models comes with many practical challenges. The bottleneck restricting our efficient training of big models mainly lies in computing resources and network communication. Big Model training is challenging for the following reasons:

1. as shown in Table 2, the number of computing operations required results in unrealistically long training time;
2. it is no longer possible to fit the entire model on a single accelerator (mainly GPU and TPU) due to limited memory capacity;
3. computational scalability is not linear due to the communication cost and memory redundancy, for example, the training time may not be reduced by a factor of two if we use twice the number of GPUs.

1.4. Overview of this report

This report is organized as follows. In Section 2, we review training algorithms for Big Model based on self-supervised learning. In Section 3, we introduce distributed training needed for Big Model training. In Section 4, we introduce three kinds of training parallelism methods including DP (Data Parallelism), PP (Pipeline Parallelism) and TP (Tensor Parallelism). In Section 5, we introduce some widely used memory-saving technologies. In Section 6, we introduce the sparsely gated mixture-of-experts approach which greatly enlarges model size with the same amount of computing resources. Finally, in Section 7 and 8, we bring up a discussion on Big Model and conclude the report.

2. TRAINING OBJECTIVES

Before diving into big model training methodologies, this section first introduces training objectives [15] of transforming a model architecture and a large amount of data into a Big Model based on self-supervised learning (SSL).

The traditional paradigm for training deep neural networks is supervised learning, and the performance of the model grows roughly logarithmically with the size of the annotated dataset [16]. However, rare and expensive data with annotation quickly becomes a scalability bottleneck for continuous improvement of state-of-the-art model performance. Hence, it stimulates research on self-supervised learning in academia. Over the past few years, SSL has achieved great success in the fields of natural language processing [1, 2], computer vision [17, 18] and speech processing [19, 20]. It leverages large amounts of data to learn universal representations, which can benefit almost all downstream tasks.

The term “self-supervised learning” was first introduced in robotics. Then the machine learning community further develops this idea and describes it as “the machine predicts any part of its input for any observed part” [21]. Current SSL methods can be categorized into generative, contrastive, and generative-contrastive according to their objectives [22]. We enumerate below their respective definitions and notable works that use the corresponding algorithms:

1. **Generative**: train an encoder to encode input into an explicit vector and a decoder to reconstruct the input from the vector, either continuous or discrete. SSL methods based on generative models include autoregressive models (GPT [1], Pixel-RNN [23], WaveNet [24]), auto-encoding models (BERT [2], MAE [25], VQ-VAE [26]) and hybrid generative models (XLNet [27]).

2. **Contrastive**: train an encoder to encode input into an explicit vector to measure similarity. The well-known works include CPC [28] which uses the contrastive InfoNCE loss to discriminate the correlated positive samples from negative context samples, and MoCo [29] which leverages instance discrimination via momentum contrast.

3. **Generative-Contrastive**: train an encoder-decoder to generate fake samples and a discriminator to distinguish them from real samples. It leverages the discriminative loss function as the objective. The most influential work is Generative Adversarial Networks (GAN) [30] and there are many of its variants [31, 32, 33].

The pre-training and fine-tuning paradigm [14] is the most widely adopted pipeline for the SSL method to transfer to the downstream task. Specifically, researchers firstly design elaborate pretext tasks (e.g. Next Sentence Prediction task in BERT [23]) to help models learn critical features from a large number of unlabeled datasets. Then they can fine-tune the pretrained model on a variety of target labeled datasets without training from scratch. Moreover, the recent GPT-3 [6] has shown that large-scale SSL models can achieve competitive performance via few-shot adaptation instead of full fine-tuning, which stimulates researchers’ desire to explore the potential of bigger models. However, Big Model always brings expensive training costs and unbearable training time. The following parts will introduce some relevant system designs and software platforms to democratize Big Model training.

3. DISTRIBUTED TRAINING

Although Big Model brings better performance and more capabilities, the training of Big Model is not just an algorithmic challenge but a systemic challenge. A GPT-3 with 175B parameters can never be fit into one GPU’s memory even with the most powerful GPU. Distributed computing can’t be avoided in Big Model training.

If the Big Model is like a vehicle, the distributed training is the highway that makes the model run faster. As the cornerstone of parallel processing of big data and big model training, distributed training consists of two parts: the training framework and the distributed system. Distributed training makes large models go from untrainable to trainable, from unacceptable training time and money consumption to convergent cost consumption. Distributed training based on backward pass usually has the following main processes: slice data loading, forward pass, backward pass, set communication, and parameter update.

3.1. Training Framework

The main process of large model training is usually built through the training framework. Based on the framework, researchers build the model layer, combined the layer to forward process, load training
data and pre-processing, construct the loss function and validation process.

The most famous early training framework is Caffe [34], which requires users to write backward propagation code in addition to forward code. Moreover, the original Caffe does not support multi-node distributed training. After subsequent development, it supports multi-machine training based on the MPI [35] communication framework. However, there are few users of distributed training based on Caffe. The current mainstream distributed training frameworks are affected by more than 90% of developers from two modern frameworks, namely Pytorch [36] and Tensorflow [37]. These modern frameworks allow researchers to focus on the forward process, optimizer efficiency, and loss design while using automatic differentiation techniques to implicitly express the computation of the gradient compute and backward process. The most important feature of the modern training framework for Big Model is the multi-node multi-gpu setting which reduces the time to configure distributed GPUs with less expert knowledge.

3.2. Distributed system

There are two main categories of distributed training architectures: Parameter Server (PS) [38] and All-reduce [39] as is shown in Fig 1.

The PS architecture typically contains workers and PS. Worker usually run on GPUs to perform forward and backward pass and push the gradients to PS on CPUs to update the parameters. Then workers pull the latest parameters from PS and start the next iteration. However, communication workload and network congestion become the performance bottleneck when scaling PS to larger clusters.

In all-reduce, only GPU machines are involved. GPUs compute the gradients of the model parameters independently and then aggregate gradients based on collective communication method. Specifically, a Ring all-reduce operation can be divided into a reduce-scatter and an all-gather operation. Reduce-scatter partitions $M$ bytes gradients into $n$ parts and each node send $\frac{(n-1)M}{n}$ traffic to other nodes. Then all-gather requires each node to broadcast its reduced part to all other $(n-1)$ nodes to obtain the result in an iteration. As a decentralized and homogeneous architecture, all-reduce achieves higher performance than PS in most distributed training tasks. However, it can’t utilize extra non-worker nodes and further research has shown that it is no longer optimal with additional CPU machines [40].

As a more general system for distributed training, BytePS [40] can leverage spare CPU and bandwidth resources in the cluster to accelerate DNN training. It offers a framework for communication that is demonstrated to be optimal in heterogeneous GPU/CPU clusters, and current all-reduce and PS can be regarded as two specific cases of BytePS.

4. TRAINING PARALLELISM

As the scale of the model and dataset increases, it becomes hard to deploy training tasks on an individual GPU machine. Even if we could fit the entire model on one GPU, the training time would become a nightmare. Thus, it is natural to employ distributed training methods and multi-processes to reduce the training burden. The training algorithms can be categorized into several popular types, such as synchronous vs asynchronous, cross-iteration vs intra-iteration, and data parallel vs model parallel [41].

In this report, we categorize these techniques according to the dimension of parallelism that takes place, including data (batch size), model (forward and backward pass), and tensor (matrix operations) [42].

4.1. Data Parallelism

As the simplest and most common way to scale training, Data Parallelism replicates the same model weights to multiple devices and distributes a portion of the data to each device for simultaneous processing, which is equivalent to parallelizing the training process along the batch dimension. In particular, each process performs forward and backward propagation on different subsets of data samples and synchronizes either gradients or updated parameters depending on the algorithm. There are three main synchronization approaches:

1. **Bulk Synchronous Parallel (BSP) [43]**: Workers wait for each other to synchronize at the end of every iteration, which reduces the staleness of weights used to compute gradients and ensures good statistical efficiency. However, waiting for gradients from other workers significantly decreases hardware efficiency and shifts the training bottleneck to communication when the model scales.

2. **Asynchronous Parallel (ASP) [44]**: Each worker proceeds with the computation for the next iteration without waiting for gradients from other workers, which reduces idle time but may lead to gradients being computed on stale weights and lowers statistical efficiency. Experimental studies demonstrate that ASP does not reduce training time [45].

3. **Stale Synchronous Parallel (SSP) [46]**: When a worker asks for updated parameter $\theta$, the model will give it a stale version that excludes recent gradient updates $\delta$. Specifically, a worker reading $\theta$ at iteration $c$ gets all $\theta$ accumulated from iteration $0$ to $c-1$, where $s \geq 0$ is a user-controlled threshold. In the SSP model, workers can perform more computations instead of waiting for other workers to finish.

Training frameworks (Sec 3.1) provide native distributed Data Parallelism APIs for developers. For example, PyTorch offers DataParallel (DP) for single-process multi-thread data parallel training using multiple GPUs on the same machine, and DistributedDataParallel (DDP) [41] for multi-process data parallel training across GPUs and machines. DDP has provided several techniques to accelerate training since PyTorch v1.5, including bucketing gradients (which buckets multiple gradients into one AllReduce operation instead of launching an AllReduce immediately when each gradient tensor becomes available), overlapping computation with communication (which starts an AllReduce operation on gradients before the local backward pass finishes), and gradient accumulation (which conducts $n$ local training iterations before synchronizing gradients globally instead of launching AllReduce in every iteration).
4.2. Pipeline Parallelism

When a model gets too big to fit on an individual GPU, it feels straightforward to partition the model across multiple GPUs, with each GPU responsible for only a portion of the model. However, a naive implementation of model parallelism results in severe underutilization of GPU resources, as illustrated in Figure 2. For each minibatch, there is only one active stage. When one device starts the processing stage, all other devices get stuck in a bubble of idle time.

Fig. 2. Model parallel training with 4 devices. Numbers indicate minibatch ID.

Pipeline Parallelism is a method to speed up neural network training by combining model parallelism with data pipelining. The main idea is that we split one minibatch into multiple microbatches to enable devices to process several microbatches simultaneously. During the forward pass, each device sends intermediate activations to the next stage. During the backward pass, each device sends the gradients of the input tensor back to the previous pipeline stage.

There are several possible ways of scheduling forward and backward microbatches across devices, either in a synchronous way such as GPipe [47] or in an asynchronous way such as PipeDream [48].

GPipe proposes a schedule where the forward passes for all microbatches in a batch are first executed, followed by backward passes for all microbatches as illustrated in Figure 3. Following [49], here we refer to the idle time introduced by partitioning as pipeline bubble $t_{pb}$, the number of microbatches in a batch as $m$, and the number of devices used for pipeline parallelism as pipeline stages $p$. The total amount of time spent in the pipeline bubble is $t_{pb} = (p-1)(t_f + t_b)$, where $t_f$ and $t_b$ denote the time to execute a single microbatch’s forward and backward pass. And the ideal processing time for a batch is $t_{ideal} = m(t_f + t_b)$. Therefore, the bubble time fraction is $t_{pb} / t_{ideal} = m-1 / m$.

To make the fraction as small as possible, we need $m \gg p$. The experiments in [47] demonstrate that the bubble overhead is negligible under the condition that $m \geq 4 \times p$ when activation checkpointing (Sec 5.1) is applied.

PipeDream schedules each worker to alternatively perform the forward and backward passes (1F1B for short), which is more memory-efficient than GPipe. In this schedule, the devices first enter a startup state where they perform a different number of forward passes. As soon as the output stage completes the forward pass for the first minibatch, it performs the backward pass for the same batch and then starts alternating between forward and backward passes in the following minibatches. After the startup state, each device then enters a steady state where no GPU is idle.

As we can see, a naive implementation of pipelining may lead to weight version mismatches between forward and backward passes. In GPipe (Figure 3), weight gradients are accumulated and updated at the end of the minibatch. It maintains a single weight version but requires periodic sync semantics. However, in PipeDream (Figure 4) which does not have end-of-batch gradient synchronization, it’s likely that the naive 1F1B schedule would cause serious weight version mismatches. Specifically, when weight updates are immediately applied to the latest weight version, gradient computations may be incorrect for the forward and backward of one microbatch using a different version of weights. PipeDream, therefore, adopts a weight stashing scheme to tackle this issue. The total number of weight versions stashed is $p$ in the worst case, which is expensive for big models. PipeDream-flush [50] introduces a periodical global synchronization scheme that reduces the memory footprint by sacrificing a little throughput. The number of outstanding forward passes is at most the number of pipeline stages for this schedule, but the time spent in the bubble stays the same.

To further reduce the pipeline bubble, in the interleaved 1F1B schedule [49], each device is assigned multiple pipeline stages and performs computations on model chunks as shown in Figure 5. The number of microbatches $m$ must be an integer multiple of the pipeline stages $p$ in this schedule. If each device has $c$ model chunks, the forward and backward time for a microbatch for each chunk reduces to $t_f / c$ and $t_b / c$. The bubble time fraction is then $t_{pb} / t_{ideal} = \frac{m-1}{m} \frac{1}{c}$, indicating that the bubble time is reduced by $c$. However, the bubble time reduction comes along with an extra amount of communication by $c$ times.

4.3. Tensor Parallelism

Tensor Parallelism refers to partitioning a tensor into several parts along a specific dimension and computing them separately on different devices. It is orthogonal and complementary to Data Paral-
For the first part of the block layer perceptron (MLP), which consist of a self-attention block followed by a two-layer multi-layered (Sec 4.1) and Pipeline Parallelism (Sec 4.2).

Firstly, this report introduces the implementation of 1D Tensor Parallelism used by Megatron-LM [4] for transformer [51] layers, which consist of a self-attention block followed by a two-layer multi-layer perceptron (MLP).

Typically, the MLP block consists of two GEMMs and a GeLU non-linearity layer. For the first part of the block $Y = \text{GeLU}(XA)$, if we split the weight matrix $A$ along its rows and input $X$ along its columns as $A = \begin{bmatrix} A_1 \\ A_2 \end{bmatrix}$ and $X = [X_1, X_2]$. This partitioning will result in $Y = \text{GeLU}(X_1A_1 + X_2A_2)$. It will require an extra synchronization process before GeLU since the nonlinearity of GeLU in that $\text{GeLU}(X_1A_1 + X_2A_2) \neq \text{GeLU}(X_1A_1) + \text{GeLU}(X_2A_2)$.

Instead, if we split $A$ along its columns $A = [A_1, A_2]$, it removes the need for synchronization since GeLU can be independently applied to the output of each partitioned GEMM: $[Y_1, Y_2] = \begin{bmatrix} \text{GeLU}(XA_1), \text{GeLU}(XA_2) \end{bmatrix}$. It is called column-wise parallelism as shown in Figure 6.

For the second part of the block $Z = \text{Dropout}(YB)$, we split the second GEMM along its rows $B = \begin{bmatrix} B_1 \\ B_2 \end{bmatrix}$ so it can take the output of the GeLU layer directly: $Z = \text{Dropout}([Y_1, Y_2] B_1 B_2)$. The output of the second GEMM is required to be reduced across devices before the dropout layer since we obtain $Y_1B_1$ and $Y_2B_2$ on two separate devices.

As shown in Figure 7, we partition the GEMMs associated with $Q, K, V$ in a column-wise manner such that we can split per attention head parameters and workload across the devices without extra synchronization. Similar to the above, the subsequent linear layer is in parallel along its rows and takes the output of the attention layer directly. There are 4 total All-Reduce operations in the forward and backward pass of a single tensor parallel transformer layer (2 in MLP and 2 in attention block). The open-source implementation is available at Megatron-LM [2].

However, in Megatron-LM, each device has to accommodate the whole activations and it could easily become a memory bottleneck when the model scale is large. To further reduce memory cost, Colossal-AI [52] proposes 2D [53], 2.5D [54] and 3D [55] Tensor Parallelism based on Scalable Universal Matrix Multiplication Algorithm (SUMMA) [56]. The open-source implementation is available at Colossal-AI [3].

Take a linear layer $Y = XA$ in 2D Tensor Parallelism for instance [57], we split both the input $X$ and weight $A$ into $[X_{10}, X_{11}, X_{00}, X_{01}]$ and $[A_{10} A_{11}, A_{00}, A_{01}]$ (given $P = q \times q$ devices and $q = 2$). The process includes $q$ steps.

In step 1, $X_{10}$ is broadcasted in its row and $A_{00}$ is broadcasted in its column. Then we multiply $X_{10}$ and $A_{00}$ on each device as $X_{10}A_{00}$. In step 2, $X_{10}$ is broadcasted in its row, $A_{10}$ is broadcasted in its column, and we multiply them as $X_{10}A_{10}$. Finally, we add the above two products to get $Y = \begin{bmatrix} X_{10}A_{00} + X_{11}A_{10}, X_{10}A_{01} + X_{11}A_{11}, X_{00}A_{00} + X_{01}A_{10}, X_{00}A_{01} + X_{01}A_{11} \end{bmatrix}$.

### 5. MEMORY-SAVING TECHNOLOGIES

#### 5.1. Activation Checkpointing

During the forward pass, training frameworks such as PyTorch and TensorFlow store all activations by default. During the backward pass, gradients are backpropagated from the loss node. Activation is then freed after its gradient has been calculated.

Activation Checkpointing (also known as "activation recomputation", "gradient checkpointing" or "re-materialization") is a technique to alleviate memory pressure during the backward pass by storing only a subset of activations. This is especially useful in large-scale models where activations can become a significant memory overhead.

For instance, if a model computes $Y = XA$, where $X$ is the input and $A$ is the weight matrix, instead of storing the intermediate activations $X$, $XA$, and $Y$, only the final output $Y$ is stored. During the backward pass, the activations required to compute gradients are reconstructed from the stored intermediate activations.

In Megatron-LM, activation checkpointing is implemented using 2D, 2.5D, and 3D tensor parallelism. The open-source implementation is available at Colossal-AI [3].
method to trade computation for memory. In general, gradient computation in the backward pass depends on the intermediate results of the forward pass and we need $O(n)$ memory for intermediate results to train a $n$ layer neural network with a sequence of length $n$. To reduce the memory consumption, it is feasible to drop some of the intermediate results during the forward pass and re-compute them by running forward from the closest recorded results.

The idea of the checkpointing technique can be traced back to the automatic differentiation literature [58]. Chen et al. [59] bring this idea to neural network computation graph construction. Specifically, the neural network is divided into several segments and only stores the output of each segment. Assume we divide $n$ layer network into $k$ segments, then the memory cost is:

$$
\text{cost}_{\text{total}} = \max_{i=1,...,k} \text{cost}_{\text{segment}}(i) + O(k) = O\left(\frac{n}{k}\right) + O(k)
$$

(1)

The first part of the equation is the memory of back-propagation on $i$-th segment, and the second part is the cost of storing the intermediate outputs between segments. The minimum cost is $O(\sqrt{n})$ at $k = \sqrt{n}$, which reduces the memory cost to be sub-linear.

However, the assumption that networks have linear graphs limits its applicability. It may lead to inefficiency and oversimplification regarding architectures like ResNet50 [60] and U-Net [61]. To seek a more general solution, Checkmate [62] formulates the checkpointing problem as a mixed-integer linear program with more flexible search space and uses off-the-shelf numerical solvers to discover optimal checkpointing strategies.

5.2. Mix Precision Training

In Mixed Precision Training [63, 64], both the forward and backward passes are performed using IEEE half-precision format (FP16) weights and activations. This has the effect of speeding up training while reducing memory costs.

The value range of FP16 is $5.96 \times 10^{-8}$ to 65504, while that of FP32 is $1.4 \times 10^{-38}$ to $3.4 \times 10^{38}$. Since the FP16 format has a narrower dynamic range than FP32, the biggest challenge towards replacing the original FP32 neural network calculation with FP16 is the accuracy loss. Three techniques are proposed to avoid suffering from degradation at half-precision as follows [63].

**FP32 master copy of weights.** The mixed-precision optimizer maintains a FP32 master copy of weights and updates the weight gradient during the optimizer step. The motivation is that the updates might become too small to be represented in FP16. Even if the weight update is representable in FP16, it might still become zero when the ratio of the weight value to the weight update appears too large.

**Loss scaling.** To avoid gradient underflow in FP16, we can scale up the loss value computed in the forward pass. This requires no extra operations during the backward pass by the chain rule. Note that gradients need to be unscaled before the weight update.

**Arithmetic precision.** For some models, in the process of FP16 vector dot-product, it is necessary to use the FP32 value to perform the accumulation operation and then convert the value of FP32 to FP16 for storage. Without this accumulation in FP32, some FP16 models would suffer from accuracy loss compared with baseline models. Therefore, in mix precision training, it is required to use NVIDIA Volta GPUs which introduce Tensor Cores to multiply FP16 input matrices and accumulate products into either FP16 or FP32 outputs [65] whereas previous GPUs supported only FP16 operation.

In particular, NVIDIA provides a PyTorch Extension (Apex) [66] to streamline mixed precision and has been included in the upstream PyTorch library for convenient implementation. There are 4 optimization levels as follows:

1. **O0:** FP32 training.
2. **O1:** Mixed Precision. Use FP16 in certain operators such as GEMM and convolution. Model weights remain FP32.
3. **O2:** “Almost FP16” Mixed Precision. Cast weights and data to FP16 and maintain an FP32 master weights.
4. **O3:** FP16 training.

Typically, training at O1 and O2 levels can converge to the same loss as O0 for regular models on NVIDIA GPUs.

5.3. Zero Redundancy Optimizer

Let’s get started by checking the memory consumption of the current training system.

During model training, most of the memory is consumed by model states (e.g. Adam [67] momentum and variances), gradients, and parameters. For a model with a parameter size of $\Psi$ using Adam and mixed precision training (Sec 5.2), it requires $2\Psi$ bytes of memory to store parameters and weights in fp16 format respectively. In addition, it needs to hold optimizer states ($FP32$ copy of the parameters, momentum, and variance) with memory requirements of $4\Psi$, $4\Psi$, and $4\Psi$ bytes, respectively. As a result, at least it requires $16\Psi$ bytes memory for model states.

The rest is taken up by residual states such as activations, temporary buffers, and fragmented memory. Residual memory consumption changes dynamically based on the configuration of the training task, such as batch size. Residual memory and model state memory compete with each other for computation resources.

The Zero Redundancy Optimizer (ZeRO) [5] provides two sets of optimizations (ZeRO-DP and ZeRO-R) to optimize memory usage during training.

ZeRO-DP aims at reducing the memory footprint of the model states with three main optimization stages as shown in Figure 8. It uses a dynamic communication schedule to distribute optimizer state ($P_{\text{opt}}$), gradient ($P_g$), and parameters ($P_p$) across multiple data-parallel processes. It retains the training efficiency of Data Parallelism while achieving the memory efficiency of Model Parallelism. ZeRO-DP requires no additional communication when using $P_{\text{opt}}$ and $P_g$, allowing for up to an 8x memory reduction. When using $P_p$ in addition to $P_{\text{opt}}$ and $P_g$, ZeRO-DP incurs a maximum of 1.5x communication while reducing the memory footprint by $N_d$ times, where $N_d$ denotes Data Parallelism degree.

ZeRO-R aims at reducing the residual memory consumption by partitioned activation recomputation, constant buffer size, and on-the-fly memory defragmentation. In particular, ZeRO-R optimizes activation checkpointing (Sec 5.1) by identifying and removing activation replication in existing Model Parallelism approaches.

Based on ZeRO, ZeRO-Offload [68] enables big model training by offloading data and computation from the GPU to the host CPU. Furthermore, ZeRO-Infinitiy [69] provides a more general heterogeneous system technology that leverages GPU, CPU, and NVMe (Non-Volatile Memory express) for scaling model training. The open-source implementation of ZeRO techniques is available at DeepSpeed.

https://github.com/microsoft/DeepSpeed
6. MODEL SPARSITY DESIGN

In this section, we introduce the Mixture-of-Expert (MoE) algorithm, a type of model sparsity design. Unlike the methods mentioned above, in which distribute training burdens are loaded to different devices, MoE introduces a sparsely-activated model with an outrageous number of parameters but a constant computational cost.

The MoE layer consists of a number of experts (each a feed-forward neural network) and a trainable gating network to decide which expert to activate as shown in Figure 9. The gating network is critical to the MoE layer, which is modeled by a softmax activation function to indicate the weights of each expert in processing each incoming example. The output of the MoE layer can be written as: \( y = \sum_{i=1}^{n} G(x)_i E_i(x) \), where \( G(x) \) denotes the output of the gating network and \( E_i(x) \) denotes the output of the \( i \)-th expert.

**Softmax Gating** \([71]\) is a simple choice of non-sparse gating function which multiplies the input with a trainable weight matrix \( W_g \) before the Softmax function.

\[
G(x) = \text{Softmax}(x \cdot W_g)
\]

**Noisy Top-K Gating** \([70]\) adds sparsity and noise to the Softmax Gating network by introducing tunable Gaussian noise and top \( k \) values selection before the softmax function.

\[
G(x) = \text{Softmax}(\text{KeepTopK}(H(x), k);
H(x)_i = (x \cdot W_g)_i + \epsilon \cdot \text{Softplus}((x \cdot W_{noise})_i)); \quad (3)
\]

where trainable weight matrix \( W_{noise} \) denotes the amount of noise per component. If \( v_i \) is in the top \( k \) elements of \( v \), then \( \text{KeepTopK}(v, k)_i = v_i \) and the rest are setting to \(-\infty\). Ramachandran and Le \([72]\) further demonstrate that higher \( k \) values in lower layers are important for models.

**GShard** \([73]\) sparsely scales Transformer by replacing every other feed-forward layer with a position-wise MoE layer. **Group-level Top2 Gating** is introduced to satisfy the need for balanced load and efficiency at scale by the following mechanisms:

1. **Expert capacity.** The number of tokens each expert computes is set to be below some uniform threshold. And a token would be degenerated into a zero vector if experts elected by the token exceed their capacity.
2. **Local group dispatching.** The gating network evenly partitions all tokens in a training batch into multiple local groups.
3. **Auxiliary loss.** Add an auxiliary loss to minimize the mean square of the fraction of input routed to each expert in case the gating network keeps selecting the same few experts.
4. **Random routing.** The gating network patches to the 2nd-best expert with the probability proportional to its weight.

**Switch Transformer** \([7]\) uses a more simplified strategy that only routes to a single expert as shown in Figure 10. This \( k = 1 \) routing strategy is referred to as **Switch Routing**.

**Fig. 8.** Comparison between baseline and three stages of ZeRO-DP optimizations. \( \Psi \) denotes model size, \( K \) denotes the memory multiplier of optimizer states, and \( N_d \) denotes DP degree. We assume the model uses Adam optimizer with mix precision training. Image based on: [5].

**Fig. 9.** Illustration of a MoE layer. Image based on: [70].

**Fig. 10.** Illustration of token routing dynamics. Expert capacity is calculated as \((\text{tokens}_\text{per batch}/\text{num experts}) \times \text{capacity factor})\). If experts overflow (denoted by dotted red lines), the tokens will not be processed by this layer. Image based on: [7].

Experiments show that Switch Routing reduces routing computation while performing better \([7]\). To achieve stable and scalable training, Switch Transformer incorporates selective precision, smaller parameter initialization, and higher expert dropout. And for the first time, it scales model size up to \textit{trillion} parameters.
7. DISCUSSION

In this section, we will discuss several issues with big models and briefly touch on some topics that are not covered in this report.

Towards Big Model. While big models continue to break records on technical benchmarks, they are becoming more likely to reflect bias from training data [74]. In natural language processing, toxicity is a primary measure of the bias. And detoxification methods like domain-adaptive pretraining [75] help to mitigate toxicity but degrade the model performance at the same time.

More about Big Model training. We can see that resource requirements for Big Model have grown far more than hardware improvements over the past generations. To facilitate the next major leap in model capacity and performance, it will become increasingly important to co-design training algorithms, models, software, and hardware [15]. In addition to the technologies introduced in this report, methods for training Big Model include specially architected hardware training platform [76, 77], efficient optimizers [78, 79], and so on.

Extremely Big or Small Models. While we investigate scaling up model size, there are numerous efforts underway to create lightweight models in order to alleviate deployment constraints [82, 83, 84, 85]. The two share the adaptation of low-bit-width representation, which is used in big model training to save memory consumption, while in lightweight model design to decrease model storage and increase inference speed. And they all complete the corresponding tasks in a sharing manner, specifically in big model training it means to distribute computation to different nodes, while in lightweight model design it means to model inter or intra group relationship to decrease model size.

Big Model Deployment. When it comes to deployment, model compression techniques like parameter pruning [86, 87, 88], knowledge distillation [89, 90, 91] and quantization [92, 93, 94] could alleviate the demanding requirements. For example, trillion parameter model Switch Transformer [7] can be distilled into small dense versions with up to 100x compression rate while preserving 30% of the sparse model quality gain. Pipeline and tensor parallelism in Sec 4 could also be used to provide additional memory capacity in inference stage.

8. CONCLUSION

This report comprehensively reviews the existing large scale model training methodologies and categorize them into: parallelism, memory-saving technologies and mixture-of-expert algorithms. Moreover, we provide brief introduction to self-supervised learning and distributing training algorithm. To democratize billion even trillion scale model training, it is critical to develop training algorithm (Sec 2), software system (Sec 4, 5, 6) based on distributed training (Sec 3).

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