Temperature-dependent power-law model for submicron CMOS circuits
EOS breakdown study

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Abstract: A temperature-dependent power-law model to simulate the pulsing EOS breakdown in CMOS integrated circuits (ICs) was proposed and evaluated in this study. It is a logarithm form of power-law model inversely related to the temperature. Fitting the results from the stressing of different commercial ICs with the grounded-gate NMOS (GGNMOS) ESD circuits by the electrical pulses indicated that the new model displayed comparable accuracy to the traditional E model/thermochemical model at constant/room temperature. When temperature changed, however, the new model had a better relationship in regression. The temperature-dependent power-law model could be used to evaluate the EOS window design of integrated circuits and be implemented into the components classification for the assembly line’s quality control.

Keywords: pulse stressing, EOS, grounded-gate NMOS (GGNMOS), E model, regression analysis

Classification: Electron devices, circuits, and systems

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1 Introduction

Electrical overstress (EOS) generates massive damage to CMOS process integrated circuits. Damage from EOS was induced by the high stressing voltage or current. By simulation of pulse voltage, the failure mechanisms of the circuit’s breakdown could be investigated. Regarding the voltage pulse causing the damage in CMOS process, the major failures modes include burnt metal, junction damage, and dielectric breakdown [1, 2]. The burnt metal failure is resulted from the overloading of metal route current. On the other hand, the junction damage refers to the destruction of the p–n junction from joule-heating. Dielectric breakdown occurs as the voltage across the dielectric layer exceeds the breakdown voltage of the dielectric. In the integrated circuit’s design, the electrostatic discharge (ESD) protection circuit is typically applied to dissipate the unexpected pulsing energy. For the ESD protection device, grounded-gate NMOS device is the most common structures for ESD/EOS protection in CMOS technology.

To simulate the EOS behaviors, pulsing stress is the common method which generates different durations of voltage pulses into the device [3, 4, 5]. The models of the pulsing stress breakdown events were proposed by characterizing the dielectric and junction breakdown. For the dielectric breakdown, the models of long-term stressing duration were studied in Time Dependent Dielectric Breakdown (TDDB) model. The dielectric time-to-failure (TF) in TDDB model developed in the late 1970s was found and described by the relation (1) [6, 7, 8, 9, 10]:

\[
\ln(TF) \propto \frac{\Delta H_0}{k_b T} - \gamma E_{OX}
\]

where \(\Delta H_0\) is the enthalpy of activation for oxide breakdown, \(E_{OX}\) is the electric field in the oxide proportional to the stressing voltage, \(\gamma\) is the acceleration...
parameter, $k_b$ is Boltzmann’s constant, and $T$ is the temperature. Equation (1) is commonly referred as the “E model” applied to low-field/low current stressing. A later study [11] proposes a thermochemical model by treating $\gamma$ in to $a/k_bT$ for the acceleration parameter with an inverse temperature dependence and rewrites E model in equation (2):

$$\ln(TF) = \frac{\Delta H_0 - aE_{OX}}{k_bT} + c$$

where $c$ is a constant.

For the voltage dependence of time to failure in CMOS circuits, the voltage was directly proportional to the stressed electric field $E_{OX}$. The electric field in equation (1) and (2) could thus be simplified to stressed voltage. Another empirical model, known as power-law model [12, 13, 14], that concerns the voltage dependence of oxide breakdown and the junction breakdown is shown in equation (3):

$$TF = c \times V_{stress}^{-n}$$

where $V_{stress}$ is the stress voltage. A study has presented the experimental evidence of the power-law model for voltage dependence of the ultrathin oxide breakdown [12]. Although power-law model is a simple and convenient model for the applied voltage can be easily measured, it does not have a temperature variable and thus only works well at constant temperature. In CMOS circuit, the junction temperature rises rapidly under device operation which decreases the junction mobility and induces the degradation of the device’s performance. Temperature factor is becoming important in the advanced CMOS process.

Hence we proposed a new “temperature-dependent power-law model” to predict the EOS breakdown from the pulsing stress method in submicron CMOS circuits in this study. It was logarithm form of power-law model inversely related to the temperature. For the breakdown models (1)–(3) had never been studied in the commercial ICs to verify their applicability, the new model and the traditional models were validated by stressing voltage pulses to CMOS at constant different temperatures. Our results clearly demonstrated that the new temperature-dependent power-law model showed comparable results to E model at the room temperature and better results at different temperatures. The failure models were also investigated by deprocessing analysis and cross-section inspection.

2 Model and experimental method

We reconsidered the three models (i.e., relation (1) and equations (2) and (3)) describing the EOS breakdown. The E model and thermochemical model shown in equation (1) and (2), respectively, is different description of the effect of temperature on $TF$. These two models would obviously show better correlations when the temperature changes. As the electric field term $E_{ox}$ in equation (1) and (2) can be presented by $V_{ox}/d$, in which $d$ is the distance of the plate, power-law model shown in equation (3) was to replace $E_{ox}$ in relation (1) and equation (2) by an easily measured voltage term and more convenient to predict the $TF$ at constant temperature. However, power-law model would thus be not applied well in the conditions
when temperature changes with electrical heating, especially in CMOS when heating dissipating is not readily. Accordingly, we proposed a new “temperature-dependent power-law model” inspired from the ideas of relation (1) and equation (2) by transforming equation (3) into a logarithm form and adding a temperature variable as shown in equation (4):

\[
\ln(TF) = \frac{\alpha - \beta \times \ln(V_{\text{stress}})}{T} + c
\]

where \(\alpha, \beta, c\) are constants obtained from experiments.

To validate the new model as shown in equation (4), four sets of ICs (IC-A, IC-B, IC-C, and IC-D) of different brands, using the GGNMOS ESD circuits and fabricated in 65 nm complementary metal oxide semiconductor (CMOS) process with 3.3 V I/O and ESD protection circuits were examined. The specification of ICs was shown in Table I. The square pulse waveform shown in Fig. 1 was generated to provide voltage pulses with different durations and amplitudes. During the test, the supply pin (V_{dd}) and the ground pin (GND) were well connected yet the other pins were left floating.

The ICs were stressed with electrical pulses started from 3.3 V with the pulse width (stress time, t_{stress}) from \(10^{-3}\) to \(10^0\) sec at room temperature (298 K). After each pulse, a voltage of 3.3 V (V_{dd}) was applied to the ICs and the leakage current (I_{dd}) was measured. The failure criteria were set to I_{dd} exceeding 1.0 mA. If the circuit was normal, a 0.1 V increment in the voltage of same pulse width was applied to the circuit until the electrical failure was observed. Each condition of pulse width was tested in 5 samples in each set of the ICs. Based on the breakdown tests, time-to-failure (TF) could be applied with stress time (t_{stress}). The failure modes were investigated by deprocessing analysis of each tested set of ICs by scanning electron microscope (SEM). The cross-section of the IC was further inspected by transmission electron microscope (TEM).

| sets of ICs | IC-A | IC-B | IC-C | IC-D |
|-------------|------|------|------|------|
| Process Technology | 65 nm CMOS Process |
| ESD circuit type | grounded-gate NMOS |
| HBM pass voltage (V) | 8000 | 6000 | 6000 | 6000 |
| I/O circuit voltage (V) | 3.3 | 3.3 | 3.3 | 3.3 |
| core device voltage (V) | 1.2 | 1.2 | 1.2 | 1.2 |

The influences of temperatures on TF were investigated on the tested ICs at 298, 323, 348, 373, and 398 K. The breakdown voltage–stress time was also recorded. Each temperature condition was tested on 3 samples in each set of ICs and the stress time was discussed as a function of the breakdown voltage and the temperature. For the analysis of the experimental data, multiple linear regression was used to model the relationship between the variables. The models were simplified to the multiple linear regression models and fit the regression line with
the least-squares method. For the breakdown models had never been studied in the commercial ICs, we would first study the applicability of the models at room temperature for commercial ICs and then evaluate their conformities when temperature changed. The failure models were also investigated.

3 Results and discussion

At room temperature (298 K), the $TF$ (pulse stressing time) to the breakdown voltage of four different sets of ICs described by E model (1) and power-law model (2) was shown in Fig. 2(a) and 2(b), respectively. The electric field term in E model and thermochemical model, which is hardly to be measured for different layout structures and dielectric materials, was simplified to $V$. As expected, the breakdown voltages showed negative correlation to the stress time. The slopes varied with different ICs nevertheless their breakdown voltages were close in the longer stress time ($10^6$ sec). In the short pulsing stress time, the failed voltages showed greater variation, possibly due to the different ESD circuit layouts (i.e., the area and geometry) and designs of the ICs. To realize the applicability of the two models, the obtained data were employed and calculated as shown in Table II. The R-squared is applied to indicate how well the experimental data fit the models. At

![Fig. 1. Waveforms of pulsing voltage used in the experiments](image)

| Table II. Data fitting of stress time and breakdown voltage for the ICs in E model and the proposed model at room temperature. The R-square values of the two models are provided. |
|-----------------|-------|-------|-------|-------|
|                | IC-A  | IC-B  | IC-C  | IC-D  |
| E model: $\ln(t_{stress}) \approx c_1 - c_2 \times V_{stress}$ | $c_1 = 14.81$ | $c_1 = 13.55$ | $c_1 = 27.22$ | $c_1 = 28.26$ |
|                | $c_2 = 2.21$ | $c_2 = 2.12$ | $c_2 = 4.16$ | $c_2 = 4.71$ |
| proposed model: $\ln(t_{stress}) \approx \frac{\alpha - \beta \ln(V_{stress})}{\beta \ln(V_{stress})}$ | $\alpha = 10438.94$ | $\alpha = 9452.56$ | $\alpha = 17173.74$ | $\alpha = 17003.88$ |
|                | $\beta = 5444.46$ | $\beta = 5060.04$ | $\beta = 9121.78$ | $\beta = 9464.48$ |
| $R^2$ of E model | 0.990 | 0.980 | 0.987 | 0.954 |
| $R^2$ of proposed model | 0.994 | 0.983 | 0.987 | 0.955 |
room temperature, the E model and the thermochemical model can be simplified to the same equation for single-variable regression and the proposed model also can be simplified as the power-law model in the same way. In the comparison of regression analysis, the proposed model fit better than E model in R-squared in the tested ICs.

To realize the breakdowns caused by voltage pulses, we analyzed the different layouts of the four failure tested ICs at stress time of $10^{-3}$ sec by layer-by-layer as junction punch-through. These damages were mainly resulted from molten silicon. To provide more evidence of the failure mode, the cross-section of IC-D’s emission spot was inspected by TEM as shown in Fig. 4. The results clearly showed the gate oxide damage taking place in the event. TEM image also provided the thickness of gate oxide (51.2 Å). These analyses verified the breakdown model’s applicability and the failure cause in gate oxide breakdown. The deprocessing results shown in Fig. 3 demonstrated the damage occurring at the GGNMOS protection circuit and MOS gate oxide as well as junction punch-through. These damages were mainly resulted from molten silicon. The analysis verified the breakdown model’s applicability and the failure cause in gate oxide breakdown.

Fig. 2. The relationship of breakdown voltages with stress time of IC-A, IC-B, IC-C, and IC-D at 298 K: (a) $V_{\text{stress}}$ plotted against $\log(t_{\text{stress}})$ for E model, (b) $\log(V_{\text{stress}})$ plotted against $\log(t_{\text{stress}})$ for power-law model.
Fig. 3. Deprocessing analysis of the tested samples (pulse width: \(10^{-3}\) sec) in IC-A, IC-B, IC-C, and IC-D. The gate damage was observed in all samples.

Fig. 4. Cross-section inspection of IC-D by TEM. The gate oxide damage was observed: (a) low magnification TEM image, (b) high magnification TEM observation.
We then investigated the effects of temperature on the \( TF \) and breakdown voltage by selecting the most fragile IC-D with lower breakdown voltage at room temperature as the model. The IC was stressed at 298, 323, 348, 373, and 398 K and the breakdown voltage against temperature at different stress time \( (TF) \) was depicted in Fig. 5. As expected, the breakdown voltage decreased with the elevating temperature at the same stressing time. The effect of temperature was more significant at longer stress time than shorter stress time as indicated by the slope. The results clearly demonstrated the importance of temperature on the breakdown of commercial IC. Changes in the MOSFET mobility, leakage current, and property of energy band gap with the temperatures would contribute to the different breakdown voltages in ICs [15].

Fig. 5. The breakdown voltage of IC-D was plotted against temperature with different stress time.

To realize the applicability of the four models, the \( TF \) and breakdown voltages at different temperatures for IC-D as plotted in Fig. 5 were input into relation (1) and equations (2)–(4) and their coefficients as well as the R-square values were determined by multiple regression analysis (Table III). For E model and thermochemical model, the electric field (E) term was also simplified to voltage (V). As shown in of Table III (entries 1 and 2), thermochemical model showed better linear relationship than E model \( (R = 0.976 \text{ vs } R = 0.973) \) at different temperatures despite the difference was not large. Both the models showed better linear relationship than power-law model \( (entry \ 3, \ R = 0.948) \) that does not use the temperature as a variable. The R-square value was 0.978 for the proposed model and was best among the four models \( (entry \ 4) \). Despite the fact that the difference was small for the proposed model \( (4) \), E model \( (1) \), and thermochemical model \( (2) \), the temperature-dependent power-law model \( (4) \) had the advantages of using an easily measured voltage. In model \( (1) \) and \( (2) \), the electric field should only be determined by specific and costly instruments. Simulation of the proposed model by various breakdown voltages, stress time, and temperatures was depicted in Fig. 6. The slopes for different temperatures changed by \( \log(V_{stress}) \) plotting against \( \log(t_{stress}) \). Our study clearly demonstrated that the new temperature-dependent power-law model showed comparable or better applicability to describe the breakdown in real ICs.
4 Conclusion

A temperature-dependent power-law model for EOS breakdown was proposed and verified in commercial ICs. The model showed comparable linear relationship to E model at constant/room temperature and better correlation than E model, thermochemical model, and power-law model at different temperature. The new model used the easily measured voltages at the coefficient and could be used to described the EOS breakdown in commercial ICs. For the breakdown is never investigated in commercial ICs, we also used deprocessing analysis and cross-section inspection to analyzed the failed ICs and the gate damages are observed in all samples.

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