A single-stage bridgeless ZVS AC/DC converter for power-factor-correction applications

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Abstract: A novel single-stage bridgeless AC/DC power-factor-correction (PFC) converter with galvanic isolation is proposed in this paper. An auxiliary switch and a clamp capacitor are connected in parallel with primary side of the transformer to reduce the voltage stress of main and auxiliary switches. The resonant inductance and the resonant capacitor are resonant to achieve zero-voltage-switching (ZVS) for both main and auxiliary switches. The main switches share the same driver signal, and the converter does not need to sense the positive or negative ac input voltage, so it could be easily implemented with available average current model control IC. The detailed ZVS operation principle of the system is presented. The proposed converter has the advantages of minimum component count, galvanic isolation and higher efficiency. Simulation and experimental results are presented for a 3000W prototype circuit at 85kHz switching frequency to demonstrate the effectiveness of the proposed converter.

Keywords: power-factor-correction, zero-voltage-switching, bridgeless

Classification: Power devices and circuits

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1 Introduction

Nowadays, isolated AC/DC PFC converters are becoming necessary for many types of electronic equipment to meet harmonic regulations and standards [1,2,3,4,5,6]. Generally, isolated PFC converters are divided into two-stage type and single-stage type according to their topologies[1,2,7]. For the two-stage type of PFC converter, the first stage is designed for rectification and power factor correction, and the second stage is designed for isolation and output voltage regulation. These topologies have good performance of high power factor, low harmonic distortion and constant output voltage, but they have the drawbacks of high components count, low efficiency and complex control. Unlike the two-stage type, the single-stage converters processed the power conversion in one stage, they have the features such as simple structure, few components and high efficiency. The flyback and forward converters are widely used in single-stage converter[3,7], but these topologies are limited for low power applications.

A resonant DC-DC converter with galvanic isolation which is suitable for single-stage high application is proposed in[8], an passive-clamp circuit is used to limit the switch voltage stress and realize the soft-switch for power switch, but it use too many passive components. A single-stage AC/DC isolated converter based on active-clamp technique is proposed in[9], it can realize the ZVS for both main and auxiliary switches, but it still needs a diode bridge rectifier and high conduction loss problem still remains. In an effort to maximize the power supply efficiency, considerable research efforts have been directed toward designing bridgeless PFC circuits. In [10], a bridgeless single-stage PFC topology is proposed, and a high conversion efficiency can be achieved, but the main switch suffers a high voltage spike during the turn-off the main switch.
In this paper, a novel single-stage bridgeless isolated AC/DC PFC converter is proposed for high power application, unlike the traditional bridge or bridgeless boost converters, the proposed converter can realize ZVS for all main and auxiliary switches, and higher conversion efficiency, lower THD current, nearly unit power factor can be achieved. The operating principles of the converter are described in detail. Finally, simulation and experimental results based on a 3000W prototype are provided to verify the effectiveness of the proposed converter.

2 Circuit topology

Fig. 1. Proposed single-stage bridgeless AC/DC PFC converter

Fig. 1 shows the single-stage bridgeless AC/DC PFC topology. The proposed topology consists of the main switches S1 and S2 which can be driven with the same pulse width modulation(PWM) signal, and it is not necessary to sense the positive or negative ac line cycle. The auxiliary S3 and clamp capacitor Cc is composed of active-clamp circuit, and it could limit the voltage spike of main switches when the turn-off of the main switches. The converter operates in the resonant mode when S1 and S2 are on, utilizing the resonance between capacitance Cp and inductance Lr. L is input inductor, and if the turns ration of isolation transformer is one, the proposed converter provides an output voltage which is greater than the input voltage. The main switch S1, S2 and auxiliary S3 all could turn on at ZVS based on the resonance during the commutation interval, so the converter can operate with higher switching frequency and reduction in the size of the passive components.

Fig. 2. Key waveforms of the proposed converter
3 Operating principle

The key waveforms of the proposed bridgeless PFC converter are provided in Fig.2. The resonant frequency of inductor $L_r$ and capacitor $C_p$ has a significant impact on the operation of the converter, it can be higher, lower or equal to the switching frequency. For simplicity, assuming that the switch frequency is higher than resonant frequency, as it can be easily implemented by using a standard average current model control IC. The following assumptions are made: i) All elements are ideal. ii) The energy stored in resonant inductor $L_r$ is sufficient to completely discharge the parasitic capacitor $C_i$ and turns on the main switch’s body diode.

For simplicity, the discussion that follows refers only to the positive ac line cycle operation, and the equivalent circuits of six operation stages are provided in Fig.3 over one switching period.

Stage 1 ($t_0-t_1$)

Stage 2 ($t_1-t_2$)

Stage 3 ($t_2-t_3$)

Stage 4 ($t_3-t_4$)
Stage 5 ($t_4 - t_5$)

![Diagram](image)

Stage 6 ($t_5 - t_6$)

![Diagram](image)

**Fig. 3.** Operation stages of proposed isolated converter

Stage 1 ($t_0 < t < t_1$)

This interval starts when switches $S_1$ and $S_2$ are turned on, the switch $S_3$ is turned off. The input inductor $L$ is being linearly charged, and the resonant inductor $i_{Lr}$ charges the resonant capacitor $C_p$ until time $t_1$ when the resonant inductor current becomes zero. The value of transformer’s second side current $i_{sec}$ is negative and it discharges the capacitor $C_s$. The diode $D_1$ and $D_6$ are turned on. This stage ends when resonant current becomes zero at time $t_1$.

There are two circuit loops in the primary side of the transformer as shown in Fig. 3(a). One circuit loop is composed of power supply $U_{in}$, inductor $L$, switch $S_1$, capacitor $C_p$, resonant inductor $L_r$ and diode $D_2$. Another circuit loop is composed of switch $S_1$, resonant capacitor $C_p$, resonant inductor $L_r$ and switch $S_2$.

Stage 2 ($t_1 < t < t_2$)

At time $t_1$, the main switch $S_1$ and $S_2$ keep conducting, the input inductor current $i_s$ still increasing linearly. The value of resonant inductor current $i_{Lr}$ changed from negative to positive, and it discharges the resonant capacitor $U_{cp}$. The value of second side current $i_{sec}$ also becomes positive, and the diode $D_4$ and $D_5$ are turned on.

There are two circuit loops in the primary side of the transformer as shown in Fig. 3(b). One circuit loop is composed of power supply $U_{in}$, inductor $L$, switch $S_2$ and diode $D_2$. Another circuit loop is composed of switch $S_1$, resonant capacitor $C_p$, resonant inductor $L_r$ and switch $S_2$.

Stage 3 ($t_2 < t < t_3$)

At time $t_2$, main switches $S_1$ and $S_2$ are turned off, and the auxiliary switch $S_3$ is off. The input inductor current $i_s$ decreases and it charges the parasitic capacitor $C_{r2}$. The resonant inductor current $i_{Lr}$ also decreases, but the value is still positive. The diode $D_4$ and $D_5$ keep conducting, and capacitor $C_o$ is charged by the current $i_{sec}$. The paralleled diode of auxiliary $S_3$ starts conduction. The interval time is very
short and the input inductor current \( i_s \) is almost constant.

There are three circuit loops in the primary side of the transformer as shown in Fig.3(c). The first is composed of power supply \( U_s \), inductor \( L \), switch \( S_2 \) and diode \( D_2 \), the second is composed of power supply \( U_s \), inductor \( L \), switch \( S_1 \), switch \( S_3 \), clamp capacitor \( C_c \) and diode \( D_2 \), the last circuit loop is composed of \( S_3 \), clamp capacitor \( C_c \), resonant inductor \( L_r \) and resonant Capacitor \( C_p \).

Stage 4 \((t_4<t_5)\)

At time \( t_4 \), the main switches \( S_1 \) and \( S_2 \) are off, as the antiparalled diode of auxiliary switch \( S_3 \) turns on, the auxiliary switch \( S_3 \) should be turned on to achieve ZVS. The input inductor current \( i_s \) decreases linearly. The resonant inductor \( i_{Lr} \) decreases to zero at time \( t_4 \). The secondary side diode \( D_4 \) and \( D_5 \) are still on, and the current \( i_{sec} \) charges capacitor \( C_s \).

There are two circuit loops in the primary side of the transformer as shown in Fig.3(d). One circuit loop is composed of power supply \( U_s \), inductor \( L \), switch \( S_1 \), switch \( S_3 \), clamp \( C_c \) and diode \( D_2 \). Another circuit loop is composed of switch \( S_3 \), clamp capacitor \( C_c \), resonant capacitor \( C_p \), and resonant inductor \( L_r \).

Stage 5 \((t_5<t_6)\)

At time \( t_5 \), auxiliary switch \( S_3 \) is on, the resonant inductor current \( i_{Lr} \) increases from zero to a positive value. The clamp capacitor \( C_c \) discharges. The secondary side diode \( D_3 \) and \( D_6 \) turns to conduction.

There are two circuit loops in the primary side of the transformer as shown in Fig.3(e). One circuit loop is composed of power supply \( U_s \), inductor \( L \), resonant capacitor \( C_p \), resonant inductor \( L_r \), and diode \( D_2 \). Another circuit loop is composed of switch \( S_3 \), clamp capacitor \( C_c \), resonant capacitor \( C_p \), and resonant inductor \( L_r \).

Stage 6 \((t_6<t_7)\)

At time \( t_6 \), the auxiliary switch \( S_3 \) turns off. The resonant inductor current \( i_{Lr} \) decreases and the value is negative. The negative inductor current \( i_{Lr} \) discharges capacitor \( C_{c2} \) from \( U_c \) to zero in this stage, and the antiparalled diode of switch \( S_2 \) starts to conduct, hence the energy stored in the resonant inductor \( L_r \) must be greater than the energy stored in the resonant capacitor \( C_r \). The main switch \( S_2 \) be turned on the ZVS operation, as the antiparalled diode of switch \( S_1 \) also conducts, the main switch \( S_1 \) and \( S_2 \) are turned on for ZVS operation. Another switch cycle starts again, and the situation is similar when the ac line is in the negative cycle.

There are two circuit loops in the primary side of the transformer as shown in Fig.3(b). One circuit loop is composed of power supply \( U_s \), inductor \( L \), switch \( S_1 \), resonant capacitor \( C_p \), resonant inductor \( L_r \), and diode \( D_2 \). Another circuit loop is composed of switch \( S_1 \), resonant capacitor \( C_p \), resonant inductor \( L_r \), and switch \( S_2 \).

### 4 Simulation and experimental result

Simulation and experimental prototypes of the proposed ZVS bridgeless converter and the ZVS converter proposed in [9] were built to verify and compare the feasibility of the converter. The key components of the proposed converter are specified in Table I. Standard average current mode with the IC UC3854 is used.
The PSIM software is also used to illustrate the operation waveform of the converter.

**Table I.** System parameters of the proposed bridgeless converter

| Parameter                        | Value               | Parameter                        | Value   |
|----------------------------------|---------------------|----------------------------------|---------|
| Input AC voltage                 | 220V/50Hz           | Turn ratio for primary side winding and secondary side winding | 8:9     |
| Output DC voltage                | 400V                | SiC switch                       | C3M0065090J |
| P0 max                           | 3000W               | Resonant inductor Lr              | 5uH     |
| Switching frequency(KHz)         | 85K                 | Input inductor L                  | 220uH   |
| Output filter capacitance C0     | 2200uF              | capacitance Cp                    | 6.6uF   |
| Clamp capacitance C              | 100uF               | capacitance Cs                    | 2.2uF   |

**Fig. 4.** Simulation and experimental waveform of input voltage, input current and output voltage in [9]

**Fig. 5.** Simulation and experimental waveform of input voltage, input current and output voltage of the proposed converter
Fig. 6. Simulation and experimental waveform of input current, primary capacitor $C_p$ and secondary capacitor $C_s$.

Fig. 7. Experimental waveform of gate voltage and drain-source voltage for switch devices $S_2$ and $S_3$.

Fig. 8. Power Factor Curve.
Fig. 9. Comparison of measured Efficiency Curve

Fig.4 and Fig.5 show the simulation and experimental waveforms of input voltage, input current and output voltage at the rated output power of 3000W of two different topologies proposed in [9] and in this paper separately. The input current is in phase with the input voltage and its shape is a sinusoidal waveform. It can be observed that the measured current THD value of the proposed bridgeless converter is only 2.93% and it is lower than the converter in [9], the output voltage keeps at 400V.

Waveforms of primary capacitor \( u_{cp} \), secondary capacitor voltage \( u_{cs} \) and input current \( i_s \) for the proposed converter are provided in Fig.6. The results of simulation and experiment are basically the same.

Waveforms for ZVS transition during turn-on for \( S_2 \) and \( S_3 \) are provided in Fig.7 for positive line cycle operation. It can be observed from Fig.7 that zero voltage switching (ZVS) could be achieved for \( S_2 \) and \( S_3 \) SiC MOSFETs.

The power factor curve of the proposed bridgeless PFC topology is shown in Fig.8, and a nearly 0.995 of the PF value could be achieved at full load.

Curves of the measured converter efficiency at 220V/50Hz input are provided in Fig.9. It can be observed that the proposed converter maintains greater efficiency across the entire load range than the converter proposed in [9], and the improvement efficiency at full load is nearly 1 percentage point, and a peak efficiency of 95.6% can be achieved.

5 Conclusion

A new ZVS bridgeless AC-DC converter topology has been presented in this paper. The proposed converter reduces switching losses by realizing soft-switching operation for the two main MOSFETS and one auxiliary MOSFET. The proposed converter has many advantages for practical implementation. It can be easily implemented with available control IC, the main switches can be driven with the same PWM signal and it does not need to sense the positive or negative ac input voltage, and it has higher conversion efficiency than the traditional boost PFC converter. The theoretical analysis is verified by a 3000W simulation and experimental prototype. A nearly unity power factor, a peak efficiency of 95.6%, and lower than 3.2% THD current could be achieved.

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