Design of PLL based Frequency Synthesizer using Harmonic Extraction Techniques

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Abstract

Objectives: This paper introduces a design of PLL based Frequency Synthesizer using Harmonic Extraction Technique. Different parameters of PLL and Frequency Synthesizer are analyzed. Methods: The Harmonic Extraction technique includes VCO with common gate amplifier, cascode amplifier and Differential output Buffer. The LC tank circuit used in this paper is a current mirror VCO. In order to extract the harmonics, Band pass filter is used. After that dual loop PLL is introduced which consists of proportional path and integral path. Furthermore Phase and Frequency Detector (PFD) is implemented using Gate Diffusion input (GDI) method. The proposed design is implemented using 90nm Cadence Virtuoso Analog Design Environment tool. Findings: As a result of using this technique, VCO achieves tuning range of 23.17% and phase noise of -85dBc/Hz @1MHz and -93dBc/Hz@10MHz with a small power dissipation of 50uW and Frequency Synthesizer achieves power dissipation of 4.8mW. Improvements/Applications: The performance analysis has shown that the designed Frequency Synthesizer has better tuning range, low power and low Phase noise which makes it suitable to operate in high frequency applications.

Keywords: Band Pass Filter (BPF), Dual Loop PLL, Frequency Synthesizer, GDI, Harmonic Extraction, PFD, PLL, VCO

1. Introduction

An electronic system that generates a large number of frequencies from a stable crystal oscillator is known as Frequency Synthesizer. Frequency Synthesizer is used in many modern devices such as radio receivers, mobile telephones and many communication devices. The low Phase noise and wide tuning range are difficult to obtain in high frequency Synthesizer. Push - Push VCOs has been implemented but it produces low amplitude output1,2,3. So, Linearized Trans Conductance VCO (LITVCO) is used4,5 but the power dissipation is high in that configuration. A new technique of VCO has been utilized known as LC VCO with current mirror which improves the VCO phase noise performance, wide tuning range as well as attains low power dissipation. In addition to VCO, a dual loop PLL is introduced in which the control loop is spitted into separate integrating and proportional paths6. The basic block diagram of Frequency synthesizer is shown in the figure1. It consists of Voltage Controlled Oscillator (VCO), Dual loop PLL, Phase and Frequency detector, Frequency Divider. This paper is organized as follows: Section II shows the design of frequency synthesizer. Section III explains the design of blocks of frequency synthesizer. Section IV shows the simulation results and discussion. Section V shows the performance analysis of frequency synthesizer. Finally, Section VI is the conclusion of this paper.

2. Design of Frequency Synthesizer

Figure 2 shows the schematic of Frequency synthesizer. Apart from the blocks in frequency synthesizer, Band Pass Filter (BPF) is used to extract the signal from all the harmonics produced by VCO. The harmonics produced by VCO are lower in amplitude. Therefore, common gate
amplifier at supply node and cascode amplifier at tail node of VCO is used. Differential output buffer is used to produce doubler output.

![Figure 1. Block diagram of frequency synthesizer.](image1)

![Figure 2. Schematic of frequency synthesizer.](image2)

### 3. Design of Blocks of Frequency Synthesizer

#### 3.1.1 LC Tank Circuit

The LC tank circuit used in this work is a current mirror VCO. The presence of negative resistance in cross coupled configuration compensate all the losses due to the resistance and capacitance but the full potential of LC tank circuit is not utilized and in balanced configuration, many components are required to produce a balanced circuit to consume less current. Therefore a new topology is demonstrated in Figure 3 where both cross coupled and balanced configuration are used. The frequency of oscillation of LC Tank circuit is

\[
f_{\text{osc}} = \frac{1}{2\pi \sqrt{LC}}
\]

Where \( L \) is the effective tank inductance, and \( C \) is the total effective tank capacitance. The \( Q \) factor of an inductor can be determined by following formula.

\[
Q = \frac{W_L}{R}
\]

![Figure 3. Schematic of LC tank circuit.](image3)

#### 3.1.2 Differential Output Buffer

Figure 4 shows the schematic of Differential Output Buffer. Differential output Buffer consists of four NMOS transistors. It produces the difference of two signal and the output voltage is amplified. The inputs of Differential Output Buffer is connected to the common Gate Amplifier and Cascade Amplifier. The advantages of this configuration is that it achieves large output oscillation amplitude and hence making the waveform less sensitive to noise.

![Figure 4. Schematic of differential output buffer.](image4)
3.1.3 Common Gate Amplifier

A common Gate amplifier is also known as current buffer or voltage amplifier. In this circuit the source terminal of the transistor acts as input and the drain acts as output and the gate is common. The gain of common gate stage is positive. Common gate configuration provides a low input impedance while offering a high output impedance. The input and output of this configuration are in phase. Figure 5 indicates the schematic of common gate amplifier.

- Current gain, \( A_i = 1 \)  
- Voltage gain, \( A_v = g_m R_L \)  
- Input resistance, \( R_{in} = \frac{1}{g_m} \)  
- Output resistance, \( R_{out} = r_o \)

3.1.4 Cascade Amplifier

The cascade is a two-stage amplifier composed of common gate and common Emitter. This configuration has many advantages such as higher input-output isolation, higher input impedance, high output impedance, higher gain or higher bandwidth. Common gate is known for wider bandwidth than common emitter configuration but common gate is having low impedance. So, the solution is to precede the common gate stage by a low gain common-emitter stage which has moderately high input impedance. This configuration also eliminates the Miller effect and thus contributes to a much higher bandwidth. Figure 6 shows the schematic of cascade amplifier.

3.1.5 Band Pass Filter (BPF)

Figure 7 shows the implementation of Band Pass Filter (BPF) with a unity gain amplifier. A simple differential amplifier can be used as a unity gain amplifier in band pass filter. The filter consists of NMO and NM1 as a differential pair with a current source NM3 and NM4. PM0 and PM1 are connected as diodes with active load. NM2 acts as a uniform distributed line. The gate of NM2 is connected to the output of the differential pair. The BPF is used to extract the harmonics of VCO and fed to the common gate amplifier and cascade amplifier which will help to increase amplitude and bandwidth of the signal.
3.1.6 Dual Loop PLL

The PLL in this work was implemented in a dual-path configuration. This architecture requires two charge pumps before the signal is applied to the VCO. The charge pump consists of two current sources. One source is connected to the positive rail while the other is connected to the negative supply rail and the output of the charge pump drives the loop filter. The charge pump either charges or discharges a capacitor according to the condition of controlled voltage. The output of phase detector provides two signals UP and DOWN. Loop filter then extracts the low frequency of the phase error signal which is fed to the voltage controlled oscillator. Figure 8 illustrates Charge pump Circuit. Figure 9 and Figure 10 demonstrates the schematic of Proportional Path and Integral Path respectively. Proportional path consists of a charge pump circuit resistor and a capacitor. Integral path consists of a charge pump circuit and a capacitor. Figure 11 illustrates the schematic of Dual loop PLL which is a combination of Proportional path and integral path. The output of Phase and frequency detector is provided to the input of Dual loop PLL. The Charge pump and loop filter in PLL converts the phase or frequency error into voltage. The output of PLL is fed to VCO. Phase and Frequency Detector (PFD) compares the phase of feedback signal coming from VCO and reference signal. The output of PFD is produced in the form of error voltage as two signals UP and DOWN. The two signals are fed to the charge pump. The PFD is constructed using Gate Diffusion Input (GDI) in which only four transistors are used. This technique reduces power dissipation, propagation delay, and area. Figure 12 shows schematic of PFD. Figure 13 shows the schematic of Frequency divider. Frequency divider is implemented using D flip-flop. D flip-flop is known as frequency divider circuit. It receives signal of frequency fin from VCO and produces signal of frequency fout. D flip flop is implemented using transmission gate.

Figure 8. Charge pump circuit.

Figure 9. Schematic of proportional path circuit.

Figure 10. Schematic of integral path circuit.

Figure 11. Schematic of dual loop PLL.

4. Simulation Results and Discussion

The schematics of blocks of Frequency Synthesizer is simulated using 90nm CMOS technology in CADENCE Virtuoso Analog Design Environmental Tool (ADE).

4.1.1. Transient Analysis

Transient analysis is obtained by varying the controlled voltage and corresponding frequencies are measured.
By varying controlled voltage, transient waveforms are obtained with different frequencies. Figure 14 shows transient waveform of VCO. Table 1 lists the tuning range of VCO by varying the controlled voltage from 900mV to 5V Figure 15 illustrates the transfer characteristics of VCO.

Table 1. Variation of frequency with controlled voltage.

| S.NO | Controlled Voltage(V) | Frequency(GHz) |
|------|------------------------|----------------|
| 1    | 0.9                    | 2.06           |
| 2    | 1                      | 4              |
| 3    | 1.5                    | 7.8            |
| 4    | 2                      | 9.715          |
| 5    | 2.5                    | 10.8           |
| 6    | 3                      | 12.792         |
| 7    | 3.3                    | 14.4           |
| 8    | 4                      | 16.8           |
| 9    | 4.5                    | 17.5           |
| 10   | 4.8                    | 18.1           |
| 11   | 5                      | 19.75          |

**Figure 12.** Schematic of phase and frequency detector (PFD).

**Figure 13.** Schematic of frequency divider.

**Figure 14.** Transient response of VCO.

**Figure 15.** Transfer characteristics of VCO.

### 4.1.2 Periodic steady state analysis

Periodic steady state analysis determine the periodic steady state response of a circuit at a specified fundamental frequency. It also analyze the circuit’s operating point. It is mandatory to obtain periodic steady state analysis for the determination of phase noise. The periodic steady state analysis of VCO has been determined in Figure 16. As frequencies are increasing, the magnitude of signals are decreasing. So, the third harmonic signal at 4.9Ghz is extracted using Band pass filter. Figure 10 portrays the periodic steady state analysis.
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4.1.3 Phase Noise
Phase noise is the frequency domain representation of fluctuations in the phase of waveform. Phase noise is one of the parameters that limits the performance of systems.

Phase noise depend on two factors:
1. High quality factor – Higher the quality factor of a oscillator circuit, better is the phase noise.
2. Selection of oscillator device – Bipolar transistor has a lower input impedance while the field effect transistor has a high input impedance. High impedance of FET results in optimum phase noise.

The Phase noise of VCO is determined in Figure 17. The Phase noise is calculated as -85dBc/Hz @ 1 MHz and -93dBc/Hz @10Mhz.

4.1.4 Transient Analysis of Dual Loop PLL
The Transient analysis of Dual loop PLL is shown in Figure 18. According to the condition of the controlled voltage which is given by the inputs UP and DOWN, the capacitor goes on charging and discharging.

4.1.5 Transient Analysis of Phase and Frequency Detector(PFD)
Figure 19 depicts the transient analysis of Phase and frequency detector (PFD) .PFD compares the phase of reference signal and the signal coming from VCO through frequency divider. Dead zone is one of the main features in PFD phase characteristic as it introduces jitter to the PLL system. Dead zone is due to the small phase error. When there is a phase difference between the PFD input signals, the output of PFD is not proportional to this error. The reason of this problem is due to the delay time of the flip flop is varying. So, PFD using GDI cells eliminates the problem of dead zone property and hence it generates signal having no phase error.
**4.1.6 Transient Analysis of Frequency Divider**

Figure 20 shows the transient analysis of frequency divider. Frequency divider divides the signal coming from VCO by N times. The frequency divider used here dividing the input pulse by a factor of two. So, it can be used as a divide by two counters.

![Figure 20. Transient analysis of frequency divider.](image)

**5. Performance Analysis of Frequency Synthesizer**

Table 2 shows the comparison with published paper given in. The comparison is done in phase noise, tuning range, total power dissipation of VCO.

**Table 2. Comparison with reference.**

| Parameters                      | Reference paper[4]       | Current Work |
|---------------------------------|---------------------------|--------------|
| Phase noise(dBc/Hz)             | -89@1Mhz -110@10Mhz      | -85@1Mhz -93@10Mhz |
| Tuning range                    | 11.7%                     | 23.17%       |
| Power dissipation (total frequency synthesizer) | 66mW                      | 4.8mW        |
| Power dissipation (VCO)         | 54mW                      | 50uW         |

**6. Conclusion**

Frequency synthesizer is designed in 90nm technology using CADENCE Virtuoso Analogue Design Environmental tool (ADE). Current mirror VCO is used which attains wide tuning range, lower power dissipation and low phase noise. Transient analyses of different voltages has been determined and corresponding frequency has been measured. Periodic steady state of VCO has been analyzed and phase noise of VCO has been determined. Dual loop PLL is used and PFD is implemented using GDI (Gate Diffusion Input) cells.

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**8. References**

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