Analog circuit design methodology utilizing a structure of thin BOX FDSOI

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Abstract: This paper proposes to utilize a structure of thin BOX FDSOI in analog circuit design. The thin BOX layer is utilized to create area efficient capacitors. The design experiment shows that the combination of the thin BOX layer capacitor and a metal fringe capacitor improves the capacitance by 92\% in comparison with the metal fringe capacitor only. Another advantage of the thin BOX FDSOI technology is the high controllability of the threshold voltages of transistors. As a demonstration of utilizing the advantage in analog circuit design, we designed a PMOS-type Dickson charge pump with dynamic threshold voltage control. The designed charge pump achieves 5.7 times larger output current and 3.5 times higher energy efficiency than a conventional charge pump.

Keywords: body bias control, thin BOX FDSOI, charge pump

Classification: Integrated circuits

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1 Introduction

Thin buried oxide (BOX) fully depleted silicon on insulator (FDSOI) transistor is one of the candidates for the next generation MOS transistor [1, 2]. FDSOI technology achieves both faster operation speed at lower supply voltage and less process variation than conventional bulk technology. One of the advantages of the thin BOX FDSOI transistor is the high controllability of the threshold voltage and it has been utilized only in digital circuit design [3, 4, 5]. This paper discusses the utilization of the advantages of thin BOX FDSOI technology in analog circuit design. We propose to use the thin BOX layer to create area efficient capacitors. The area efficiency can be further increased if the transistors and capacitors with the same well voltage were put in the same well to share a well-tap. As a demonstration, we designed a Dickson type charge pump (DCP) [6] in a 65 nm thin BOX FDSOI process. In the designed DCP, capacitors are created using the thin BOX layer, and the threshold voltages of diode-connected PMOS transistors are dynamically controlled so that the threshold voltages are lowered for on-mode transistors and raised for off-mode transistors to improve the voltage pump efficiency and achieve large output current.

2 Thin BOX layer capacitor and dynamic threshold voltage control

2.1 Thin BOX layer capacitor

In a thin BOX FDSOI process, a diffusion is insulated from a well by a thin BOX layer. Fig. 1(a) shows a cross section of a PMOS transistor on a thin BOX layer. The very thin BOX layer achieves high body bias effect, and it also results in a large diffusion-to-body capacitance [2, 7]. From another viewpoint, as shown in Fig. 1(b), this large diffusion region can be utilized as a large capacitor. Since the P-diffusion and the N-well are isolated by a thin BOX layer, no current flows whatever high voltage is applied to the P-diffusion. A diode is formed between the N-well and the P-substrate, thus little leakage current flows when the N-well voltage is higher than the P-substrate voltage. Hence, the structure in Fig. 1(b) is used as a capacitor (named thin BOX capacitor) with terminals A and B. This thin BOX capacitor needs a well-tap to control the N-well voltage. The P-N junction causes a parasitic capacitance between the N-well and the P-substrate. When driving the voltage of terminal A, an energy loss occurs in charging/discharging the parasitic capacitance.

Since thin BOX capacitors do not use any metal layer, a metal fringe capacitor [8] can be constructed over a thin BOX capacitor in the same silicon area. By
connecting the thin BOX capacitor and the metal fringe capacitor in parallel, a large capacitance can be achieved with high area efficiency.

### 2.2 Area reduction by N-well sharing

Body bias control is used to control the threshold voltage of transistors to improve circuit operation [5, 9]. The body bias control requires several different potential wells to divide the potentials of back gates. Spacing between different potential wells, spacing between well edge to diffusion, and additional well-taps increase circuit area. When transistors and thin BOX capacitances are placed in a same potential well, the area overhead of well-taps is mitigated. Fig. 2 shows the area reduction by N-well sharing.

![Fig. 2. Area reduction by N-well sharing.](image)

### 2.3 Dynamic threshold voltage control

We implemented a PMOS-type DCP [6] as a demonstration of utilizing the advantages of thin BOX FDSOI technology in a 65 nm process. A DCP is a voltage boost circuit which pumps up charges with diode-connected transistors, capacitors, and complementary clock signals [6]. Fig. 3(a) shows a conventional 3-stage DCP with diode-connected NMOS transistors. Let CP_N denote this type of DCP. The voltage-amplified gain per stage, \( V_{ga} \), is roughly expressed as follows [6, 10]

\[
V_{ga} = V_{DD} - V_{drop} - \frac{I_{load}}{C_f}
\]  

(1)
where $V_{DD}$ is a supply voltage, $V_{\text{drop}}$ is the drop voltage of the diode-connected transistor, $I_{\text{load}}$ is the average output current which flows to a load, $C$ is a clock coupling capacitance of each node, and $f$ is a clock frequency. As $V_{DD}$ decreases, $V_{ga}$ decreases. Since $V_{\text{drop}}$ is not only dependent on but close to the threshold voltage of the transistor, lowering the threshold voltage increases $V_{ga}$. The threshold voltage of a diode-connected transistor $V_t$ can be modeled as

$$V_t = V_{t0} + \gamma(\sqrt{\phi_s + V_{SB}} - \sqrt{\phi_s})$$

where $V_{t0}$ is the threshold voltage when the source is at the body potential, $\phi_s$ is the surface potential at threshold, and $\gamma$ is the body effect coefficient.

Fig. 3(b) shows the DCP with diode-connected PMOS transistors. Let CP$_{P,\text{wBB}}$ denote this type of DCP. In contrast to CP$_N$, forward bias effect decreases $V_t$ of a PMOS transistor. $V_t$ decreases by 22\% when $V_{SB}$ is $-0.40$ V. It decreases $V_{\text{drop}}$, and $V_{ga}$ increases. Therefore, CP$_{P,\text{wBB}}$ can generate a higher output voltage than CP$_N$.

In order to achieve a further high output voltage, we propose another PMOS-type DCP, denoted by CP$_{P,\text{wBB}}$, where the body voltages of the diode-connected PMOS transistors are driven by clock signals as shown in Fig. 3(c). When the diode-connected PMOS transistor is ON, the body voltage is driven to 0 V and $V_{SB}$ is equal to $-V_{\text{source}}$, where $V_{\text{source}}$ is the source voltage of the transistor. Strong forward body bias is applied thus $V_t$ decreases further. The diode-connected transistor $M_0$ of CP$_{P,\text{wBB}}$ achieves 22\% lower $V_t$ than that of CP$_{P,\text{wBB}}$ when $V_{SB}$ is equal to $-0.40$ V. On the other hand, when the diode-connected PMOS transistor is OFF, the body voltage is driven to $V_{DD}$ and $V_{SB}$ is equal to $(V_{DD} - V_{\text{source}})$. No enhanced body bias is applied and the $V_t$ returns to the nominal, thereby the amount of backward current flowing through off-mode transistors is the same as CP$_{P,\text{wBB}}$'s. Consequently, CP$_{P,\text{wBB}}$ achieves lower $V_{\text{drop}}$ and generates a higher output voltage than CP$_N$ and CP$_{P,\text{wBB}}$.

![Fig. 3. Dickson Charge pumps (a) CP$_N$ (b) CP$_{P,\text{wBB}}$ (c) CP$_{P,\text{wBB}}$.](image)

The area reduction mentioned in Sect. 2.2 can be applied to CP$_{P,\text{wBB}}$ if the capacitor mentioned in Sect. 2.1 is used as the clock coupling capacitors. Transistors $M_0$, $M_2$ and capacitors $C_1$, $C_3$ can share an N-well, and $M_1$, $M_3$ and $C_2$ can
share another N-well. Therefore, the area overhead of well-taps to drive the bodies are mitigated.

3 Experimental results

3.1 Evaluation setup
Thin BOX capacitors and charge pump circuits were designed in a commercial 65-nm FDSOI process with eight metal layers. In this work, we assume the charge pumps are used to generate a reverse bias voltage to suppress leak current in digital circuits, as illustrated in Fig. 4. The same supply voltage is used for the charge pump and the digital circuit. A 1 MHz clock signal is assumed for charge pump operation. The nominal supply voltage of the process is 0.75 V, however we use a 0.40 V supply voltage for both the charge pump and the digital circuits. These charge pumps are designed to output 1.2 V to apply a strong reverse bias voltage to the digital circuits. In the following sections, first the evaluation result of the capacitance of the thin BOX capacitor is discussed. Next, the effect of dynamic threshold voltage control on the charge pump characteristics is discussed.

3.2 Capacitance design comparison
Three types of capacitors were designed and compared for the capacitance per area. The first is a metal fringe capacitor using a metal to metal capacitance formed in routing layers. In this design, the metal fringe capacitor occupies six metal layers of metal 1 layer to metal 6 layer. The second is a thin BOX capacitor with the thin BOX layer in the FDSOI process. Note that a thin BOX capacitor is formed using no metal layer, metal layers can be used for signal routings and/or metal fringe capacitors. Hence, the last is a capacitor with the combination of the metal fringe and thin BOX capacitors. All the capacitors are designed respectively in a 17.6 µm by 8.2 µm footprint. The capacitance is evaluated by an RC extraction tool. We also evaluate the P-N junction parasitic capacitance between the N-well and the P-substrate for the thin BOX capacitor.

Table I shows the evaluation results of the capacitors. The capacitance of the thin BOX capacitor achieves 92% of the metal fringe capacitor. The P-N junction parasitic capacitance is 64% of the thin BOX capacitor. The combination of both the metal fringe capacitor and the thin BOX capacitor achieves 92% larger capacitance compared with the metal fringe capacitor only. The P-N junction parasitic capacitance is 31% of the combination of the metal fringe and thin BOX capacitors.
3.3 Evaluation of dynamic threshold control on charge pump performance

To show the effects of changing the types of the diode connected transistors and using the dynamic threshold voltage control, three DCP circuits, CPN, CP_{P,woBB}, and CP_{P,wBB}, were designed. The same 3-stage structure as shown in Fig. 3 is used. The channel length and width of the diode-connected transistors are identical. All the capacitors are created as the combination of the thin BOX and the metal fringe capacitors. The capacitances of these capacitors are all the same value. The area of CP_{P,wBB} is minimized by N-well sharing. Transistors M_0, M_2 and capacitors C_1, C_3 share an N-well, and M_1, M_3 and C_2 share another N-well. All of circuits are extracted from the layouts and evaluated via circuit simulation. Fig. 5 shows the layout image of CP_{P,wBB}.

The terminal As of the thin BOX capacitors are tied to the outputs of the drive inverters. Driving the voltages of the terminal As loses energy to charge/discharge the P-N junction parasitic capacitances. Since these parasitic capacitances do not contribute to pumping up current, the energy efficiency of the thin BOX capacitor is worse than the metal fringe capacitor only.

Fig. 6(a) shows the output characteristics of the designed DCPs. In the simulation, ideal constant current load is connected to the output of charge pumps and the output voltages are evaluated. When the load current is zero, all the charge pumps successfully output 1.2 V. However, as the load current increases, the output voltages decrease. The result shows that CP_{P,wBB} outputs the highest output voltage. CP_{P,wBB} achieves 5.7 times larger output current than CP_{P,woBB} when the output voltage is degraded to 1.1 V (8.3% degradation). Energy efficiency is evaluated by comparing the average power of load current $P_{load}$ per the average power of the charge pump circuit $P_{CP}$. Fig. 6(b) shows $P_{load}/P_{CP}$ vs. output voltage. CP_{P,wBB} achieves 3.5 times higher energy efficiency than CP_{P,woBB} when the output voltage is degraded to 1.1 V. Table II shows the performance comparison of the designed charge pump circuits. In CP_{P,wBB}, transistors and thin BOX capacitors can be placed adjacently thus the area overhead of CP_{P,wBB} is small.

### Table 1. Normalized capacitance under the same area conditions.

| Capacitor Configuration                                      | Normalized Capacitance |
|--------------------------------------------------------------|-------------------------|
| Metal fringe capacitor (M1-M6)                              | 1                       |
| Thin BOX capacitor                                          | 0.92                    |
| Metal fringe capacitor (M1-M6) + Thin BOX capacitor          | 1.92                    |
| Diode capacitance between N-well and P-sub                  | 0.59                    |

Fig. 5. CP_{P,wBB} layout image.
Conclusion

This paper proposed to utilize the characteristics of thin BOX FDSOI for analog circuit design. The design experiment in a 65 nm FDSOI process shows that the combination of the thin BOX capacitor and the metal fringe capacitor improves the capacitance by 92% in comparison with a metal fringe capacitor of the same footprint. With the area efficient capacitors, the charge pump circuit with dynamic threshold voltage control is designed in a small circuit area. When the output voltage degradation is 8.3%, it achieves 5.7 times larger output current and 3.5 times higher energy efficiency than the conventional charge pump.

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Table II. Performance comparison (VDD 0.40 V, clock frequency 1 MHz, output voltage 1.1 V).

| Circuit Area [um²] | Area overhead [-] | Load current [nA] | $P_{CP}$ [nW] | $P_{load}$ [nW] |
|-------------------|------------------|-------------------|--------------|----------------|
| $C_N$             |                  |                   |              |                |
| 508               | -                | -                 | -            |                |
| $C_{P,woBB}$      | 518              | 2.0%              | 7            | 98             | 8              |
| $C_{P,wBB}$       | 509              | 0.2%              | 40           | 148            | 41             |

Fig. 6. Experimental Results (a) Relation between load current and output voltage (b) $P_{load}/P_{CP}$ vs. output voltage.