Improving Dependability of Neuromorphic Computing With Non-Volatile Memory

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Abstract—As process technology continues to scale aggressively, circuit aging in a neuromorphic hardware due to negative bias temperature instability (NBTI) and time-dependent dielectric breakdown (TDDB) is becoming a critical reliability issue and is expected to proliferate when using non-volatile memory (NVM) for synaptic storage. This is because an NVM requires high voltage and current to access its synaptic weight, which further accelerates the circuit aging in a neuromorphic hardware. Current methods for qualifying reliability are overly conservative, since they estimate circuit aging considering worst-case operating conditions and unnecessarily constrain performance. This paper proposes RENEU, a reliability-oriented approach to map machine learning applications to neuromorphic hardware, with the aim of improving system-wide reliability without compromising key performance metrics such as execution time of these applications on the hardware. Fundamental to RENEU is a novel formulation of the aging of CMOS-based circuits in a neuromorphic hardware considering different failure mechanisms. Using this formulation, RENEU develops a system-wide reliability model which can be used inside a design-space exploration framework involving the mapping of neurons and synapses to the hardware. To this end, RENEU uses an instance of Particle Swarm Optimization (PSO) to generate mappings that are Pareto-optimal in terms of performance and reliability. We evaluate RENEU using different machine learning applications on a state-of-the-art neuromorphic hardware with NVM synapses. Our results demonstrate an average 38% reduction in circuit aging, leading to an average 18% improvement in the lifetime of the hardware compared to current practices. RENEU only introduces a marginal performance overhead of 5% compared to a performance-oriented state-of-the-art.

I. INTRODUCTION

Machine learning models built with spike-based computations and bio-inspired learning algorithms, e.g., Spiking Neural Network (SNN) [1] lower the energy consumption of machine learning tasks when they are executed on event-driven neuromorphic hardware such as DYNA-P-SE [2], TrueNorth [3], and Loihi [4]. A typical neuromorphic hardware consists of computation units called neurosynaptic cores, communicating spikes via a shared interconnect. A neurosynaptic core is essentially a crossbar, which is a \( n \times n \) organization of input and output neurons and synaptic weight storage at each crosspoint.

Recently, Non-Volatile Memory (NVM) such as Phase Change Memory (PCM), Oxide-based RAM (OxRAM), and Spin-Transfer Torque Magnetic RAM (STT-MRAM) are used for synapses in neuromorphic architectures [5], beyond their use as memory for conventional von-Neumann computing [6–8]. NVMs bring certain advantages such as high integration density, multi-bit synapse, CMOS compatibility, and above all, non-volatility, which can further lower the energy consumption of neuromorphic hardware. However, NVMs also introduce reliability issues such as endurance, aging, and read disturbances (see Table I) [9]–[11]. These issues are triggered when propagating current through an NVM synapse. In this work, we focus on one specific reliability issue — that of aging of circuit components in a neuromorphic hardware leading to hard failures, and propose an intelligent solution to mitigate this problem (Section IV).

Although reliability issues of NVMs have been addressed at the system-level for von-Neumann computing with NVM-based main memory, e.g., [6], [12], these approaches do not apply to neuromorphic computing. Recent system-level works on mapping SNN-based applications to neuromorphic hardware, such as [13]–[19], target performance improvement only. They do not consider reliability issues of neuromorphic computing. Our recent work [20] demonstrates the significant reliability degradation introduced using these SNN mapping approaches. In fact, this motivating work has also shown the change in reliability profile for different neuron and synapse mapping strategies. This is because with change in mapping, computation units in the hardware are stressed differently when processing a machine learning task, resulting in different reliability behavior of the hardware.

Contributions: This paper addresses reliability issues, specifically, circuit aging in neuromorphic computing with NVM using an intelligent neuron and synapse mapping technique. Following are our key contributions.

- We formulate the detailed aging of CMOS-based circuits in a neuromorphic hardware.
- We incorporate and integrate different failure mechanisms such as Time-Dependent Dielectric Breakdown (TDDB), Negative-Bias Temperature Instability (NBTI), and Hot Carrier Injection (HCI).
- We use this low-level circuit aging formulation to develop a system-wide reliability model, which allows to estimate the aging of computation units in a neuromorphic hardware when processing a spike train from a machine learning application.
- We propose a meta-heuristic approach based on Particle Swarm Optimization (PSO) [21] to map neurons and
synapses to a neuromorphic hardware. We apply Pareto Optimization to retain only those mappings that are optimal in terms of reliability and performance.

We evaluate our approach, which we call RENEU (REliability-aware NEUromorphic Computing), with state-of-the-art machine learning applications built using multi-layer perceptron (MLP), convolutional neural network (CNN), and recurrent neural network (RNN) models on a state-of-the-art neuromorphic hardware with OxRAM synapses. Results demonstrate an average of 38% reduction in circuit aging, leading to an average of 18% improvement in the lifetime of the hardware compared to current practices. RENEU only introduces a marginal performance overhead of 5% compared to a performance-oriented state-of-the-art mapping approach.

To the best of our knowledge, this is the first work that formulates the detailed aging of a neuromorphic hardware when executing a machine learning application and proposes a novel neuron and synapse mapping technique to reduce the overall aging of the hardware, improving dependability of neuromorphic computing.

II. BACKGROUND

A. Spiking Neural Networks

Spiking neural networks (SNNs) are computation models with spiking neurons and synapses [1]. Neurons are typically implemented using Leaky Integrate-and-Fire (LIF) model [22]. Information is represented using short impulses of infinitesimally small duration, called spikes. Spiking LIF neurons can be organized into feedforward layers, e.g., multi-layer perceptron (MLP) and convolutional neural network (CNN) or in a recurrent topologies, e.g., recurrent neural network (RNN). In this work, we evaluate MLP, CNN, and RNN-based machine learning applications (Section V). SNNs can implement both supervised and unsupervised learning. For supervised learning, a model is trained with examples from the field, without being exclusively programmed with any task-specific rules. A trained SNN model is then deployed on a neuromorphic hardware to perform inference from in-field data. For unsupervised learning, a machine learning model is trained in real-time using bio-inspired learning algorithms such as spike-timing dependent plasticity (STDP) [23]. Without loss of generality, we focus on supervised machine learning approaches.

Recently, machine learning applications using analog computation models have achieved significant breakthroughs in computer vision and image processing domains [24]. Many research centers around the world now use analog models of CNNs for diverse applications. Section V discusses how RENEU applies to analog CNNs.

B. Neuromorphic Hardware

Figure 1 shows a representative tile-based neuromorphic hardware similar in structure to the DYNAP-SE, Loihi, and TrueNorth architectures. DYNAP-SE has four tiles per chip where each tile consists of a crossbar (C) and communicates with other tiles using the interconnect. Routing of spikes on the interconnect is facilitated using a switch (S).

A crossbar is an \( n \times n \)-organization (in 3D) of \( n \) rows (top electrodes) and \( n \) columns (bottom electrodes), and storage elements, e.g., NVM at their crosspoints. In DYNAP-SE, \( n = 128 \), while in TrueNorth, \( n = 256 \). When mapping an SNN to a neuromorphic hardware, synaptic weights are programmed as conductivity of these NVMs. The figure also illustrates a small example of mapping an SNN to the crossbar. Synaptic weights \( w_1 \) and \( w_2 \) are programmed into NVM cells P1 and P2, respectively. The output spike voltages, \( v_1 \) from N1 and \( v_2 \) from N2, inject current into the crossbar, which is obtained by multiplying a pre-synaptic neuron’s output spike voltage with the NVM cell’s conductance at the cross-point of the pre- and post-synaptic neurons (following Ohm’s law). Current summations along columns are performed in parallel using Kirchhoff’s current law, and implement the sums \( \sum_j w_i v_j \), needed for forward propagation of neuron excitation.

A crossbar introduces the following constraints when mapping SNNs to a neuromorphic hardware.

- Each crossbar has \( n \) input ports and \( n \) output ports, i.e., \( n \) input neurons, one at each row, inject current into the crossbar, and \( n \) output neurons, one at each column, act as current sink to propagate neuron computations.
- Each crossbar can accommodate a maximum of \( n \) pre-synaptic connections per output neuron.

C. Non-volatile Memory

Emerging NVM technologies such as phase-change memory (PCM), oxide-based memory (OxRAM), spin-based magnetic memory (STT-MRAM), and Flash have recently been used as synaptic storage elements within crossbars. NVMs are non-volatile, have high CMOS compatibility, and can achieve high integration density. Each NVM device can implement both a single-bit and multi-bit synapse. Because of these properties, an NVM-based neuromorphic hardware typically consumes energy that is magnitudes lower than using SRAMs [5]. [25]–[27]. However, NVMs also introduce reliability issues and Table II summarizes the sources of reliability concerns.

In this work, we focus on PCM-based neuromorphic computing [5]. Figure 2 illustrates how a chalcogenide semiconductor alloy is used to build a PCM cell. The amorphous phase (RESET) in this alloy has higher resistance than the crystalline phase (SET). \( \text{Ge}_2\text{Sb}_2\text{Te}_5 \) (GST) is the most commonly used alloy for PCM. To compute \( \left( x_i \cdot w_i \right) \), a current is injected into the resistor-chalcogenide junction via the heater element. The current is controlled to ensure that the phase
TABLE I: Reliability issues in NVMs.

| Reliability Issues                  | NVMs          |
|-------------------------------------|---------------|
| High-voltage related circuit aging  | PCM, Flash    |
| High-current related circuit aging  | OxRAM, STT-MRAM |
| Read disturbance                    | All           |
| Limited endurance                   | All           |

III. RELIABILITY FORMULATION

There are many sources of reliability issues in a neuromorphic hardware with PCM synapses, as listed in Table I. We focus on the aging of CMOS-based circuits due to high voltage PCM operations. Figure 3 shows the internal circuitry of a neuron which injects current into a crossbar [28]. We observe that the CMOS transistors are operated at elevated voltages (1.8V and 3V for 1D-1R PCM, and 1.2V and 1.8V for 1T-1R PCM) during the execution of a machine learning application. These elevated voltages accelerate CMOS aging, leading to hard or soft faults in the neuromorphic hardware. It is important to note that continuous device scaling and elevated operating temperatures can make these errors manifest sooner than endurance-related failures, making CMOS aging a critical dependability issue.

A. High-Voltage Related Circuit Aging

In this section we formulate CMOS aging considering Time-Dependent Dielectric Breakdown (TDBD), Negative-Bias Temperature Instability (NBTI), and Hot-Carrier Injection (HCI) failure mechanisms. These are the dominant ones in scaled technology nodes (45nm and below). In older nodes, Electromigration (EM) plays a key role [29]–[32]. Nevertheless, our aging formulation can be easily extended to also consider EM and any other failure mechanisms.

CMOS aging is accelerated when the device is stressed, i.e., exposed to high overdrive voltages[3]. With this understanding, we provide a brief background of these failure mechanisms.

- **TDBD:** This is a failure mechanism in a CMOS device, when the gate oxide breaks down as a result of long-time application of relatively low electric field (as opposed to immediate breakdown, which is caused by strong electric field) [33]. The lifetime of a CMOS device is measured in terms of its mean time to failure (MTTF) as

  \[ \text{MTTF} = A e^{-\gamma V^\alpha} \]

  (1)

1 Overdrive voltage is defined as the voltage between transistor gate and source (Vgs) in excess of the threshold voltage (Vth), where Vth is the minimum voltage required between gate and source to turn the transistor on.
where $A$ and $\gamma$ are material-related constants, and $V$ is the overdrive gate voltage of the CMOS device.

- **NBTI:** This is a failure mechanism in a CMOS device in which positive charges are trapped at the oxide-semiconductor boundary underneath the gate[33]. NBTI manifests as 1) decrease in drain current and transconductance, and 2) increase in off current and threshold voltage. The NBTI lifetime of a CMOS device is

$$MTTF_{NBTI} = \frac{A}{V_0} e^{E_0/KT};$$

where $A$ and $\gamma$ are material-related constants, $E_0$ is the activation energy, $K$ is the Boltzmann constant, $T$ is the temperature, and $V$ is the overdrive gate voltage of the CMOS device.

- **HCI:** This is a failure mechanism in a CMOS device, when a carrier (electron or hole) gains sufficient kinetic energy to overcome the potential barrier of the conducting channel and gets trapped in the gate dielectric, permanently changing the switching characteristics of the device[33].

Unlike the TDDB and NBTI failure mechanisms, for which silicon-characterized reliability models are available from foundries, characterized models for HCI failure mechanism are still in development for scaled nodes.

1) **TDDB Aging of a Single Neuron in a Tile:** We illustrate our aging formulation for TDDB failure mechanism first, and then show how to extend this formulation to consider other failure mechanisms such as NBTI and HCI.

TDDB failures can also be modeled using the Weibull distribution[30] with a scale parameter $\alpha$ and a slope parameter $\beta$. Reliability at time $t$ can be written as

$$R(t) = e^{-\left(\frac{V(t)}{\alpha}\right)^\beta},$$

with the corresponding MTTF computed as

$$MTTF = \int_0^\infty R(t)dt = \alpha(V)^\beta \left(1 + \frac{1}{\beta}\right),$$

where $\Gamma$ is the Gamma function. Using the expressions for MTTF from Equations [1] and [3] and rearranging, we obtain the expression for the scale parameter $\alpha$ as

$$\alpha(V) = \frac{A e^{-\gamma V}}{\Gamma \left(1 + \frac{1}{\beta}\right)}.$$  

(5)

Figure[4] illustrates a spike train and the change in operating voltage of a neuron circuit to inject current into the crossbar for each spike in the spike train. To estimate the aging in this time duration, we let $[t_i, t_{i+1}]$ be the $(i+1)^{th}$ time interval with $\Delta t_i = t_{i+1} - t_i$ and $V_i$ as the neuron’s voltage.

Reliability of a CMOS device at the start of execution is

$$R(t)|_{t=t_0} = 1.$$  

(6)

At the end of the first interval, the reliability is

$$R(t_1) = e^{-\left(\frac{V_i}{\alpha}\right)^\beta}.$$  

(7)

Using the term $\theta$ to represent reliability degradation during this interval $[t_0, t_1]$, the reliability at the beginning of the second interval (i.e., right after the start of the first idle period) is

$$R(t_1^+) = e^{-\left(\frac{V_i+\Delta t_i}{\alpha}\right)^\beta}.$$  

(8)

Due to the continuity of the reliability function, we can equate Equations [7] & [8] to compute $\theta$ as

$$\theta = \left(\frac{\alpha(V_i)}{\alpha(V_{i+1})} - 1\right) \theta.$$  

(9)

Substituting Eq. [9] in Eq. [8] reliability at time $t_2$ is

$$R(t_2) = e^{-\left(\sum_{i=1}^n \frac{\Delta t_i}{\alpha(V_{i+1})}\right)^\beta}.$$  

(10)

We can extend this equation to compute the reliability of a CMOS device in the neuron circuit at the end of the spike train as

$$R(t_\text{end}) = e^{-\left(\sum_{i=1}^n \frac{\Delta t_i}{\alpha(V_{i+1})}\right)^\beta}.$$  

(11)

We define the TDDB aging of the neuron $i$, $\mathcal{A}_{TDDB}(i)$, as

$$\mathcal{A}_{TDDB}(i) = \sum_{i=1}^n \frac{\Delta t_i}{\alpha(V_{i+1})}, \text{ such that } R(t_{\text{end}}) = e^{-\left(\mathcal{A}_{TDDB}(i)\right)^\beta},$$

(12)

where the scaling factor $\alpha(V_i)$ can be calculated using Eq. [5].

2) **TDDB Aging of a Tile:** The aging of Eq. [12] can be extended to incorporate the aging of other neurons in the tile (i.e., all input to a crossbar in the tile). To this end, we consider a tile to be faulty if any input neuron fails due to TDDB.

Using this series failure model, the TDDB aging of tile $j$ is

$$\mathcal{A}_{TDDB}^j = \max\{\mathcal{A}_{TDDB}(i), \forall i \in 1,\ldots,n\}.$$  

(13)

where $n$ is the number of input ports of the tile, i.e., the number of input neurons and $\mathcal{A}_{TDDB}(i)$ is the TDDB aging of the $i^{th}$ neuron in the $j^{th}$ tile, computed using Eq. [12].

3) **TDDB Aging of a Neuromorphic Hardware:** To compute the TDDB aging of the neuromorphic hardware with $N$ tiles, we similarly use a series failure model, where a single faulty tile leads to the failure of the neuromorphic hardware. The TDDB aging of the neuromorphic hardware is

$$\mathcal{A}_{TDDB} = \max\{\mathcal{A}_{TDDB}^i, \forall j \in 1,\ldots,N\}.$$  

(14)

Formulating TDDB as a series failure model allows our mapping framework to minimize the maximum aging, i.e., solving a minmax problem (see Section IV).

2In our future work, we consider a single faulty neuron to reduce the capacity of the crossbar in a tile, rather than treating the entire tile to be faulty. Nonetheless, considering this capacity reduction is a reactive solution. The proposed work, on the other hand is an orthogonal proactive approach.
B. Combining Aging due to other Failure Mechanisms

Next, we consider NBTI, which is manifested as threshold voltage shift in a CMOS device. Recent works such as [34] suggest that NBTI is the collective response of two independent mechanisms: the as-grown hole traps (AHTs) and generated defects (GDs). AHTs and a small proportion of GDs can be recovered by annealing at high temperatures if the NBTI stress voltage is removed.

Using the spike train of Fig. 4, NBTI aging is given by

\[ A_{NBTI} = \sum_{i=0}^{m-1} g_i \cdot (V_{c} - V_{NBTI})^{m} \cdot (t_{i+1} - t_{i})^{n}, \]

such that \( R(T) = e^{-A_{NBTI}}, \) where \( \beta, g, m, n \) are material-dependent constants [34].

To combine the aging from different failure mechanisms such as TDDDB, NBTI and HCI, we use the Sum-of-Failure-Rates (SOFR) model, which is used extensively in the industry [32]. SOFR assumes an exponential lifetime distribution for each failure mechanism, allowing us to compute the overall aging of the neuron as the combined effect of aging due to each failure mechanism individually.

Using Equations 15 & 17, the failure rate for TDDDB is

\[ \lambda_{TDDDB} = \frac{1}{MTTF_{TDDDB}} = \int_{0}^{\infty} e^{(-A_{TDDDB})^{\beta}}. \]

Using SOFR, the overall failure rate is computed as

\[ \lambda_{overall} = \frac{1}{MTTF_{overall}} = \lambda_{TDDDB} + \lambda_{NBTI} + \lambda_{HCI}. \]

The overall aging of the neuromorphic hardware is therefore

\[ A_{overall} = \ln \left( e^{(-A_{TDDDB})^{\beta}} + e^{(-A_{NBTI})^{\beta}} + e^{(-A_{HCI})^{\beta}} \right)^{\frac{1}{\beta}}. \]

Equation 18 can be extended to consider other failure mechanisms, as well as other models to compute the aging.

C. Lifetime Computation

The lifetime of a neuromorphic hardware is usually much longer than the execution time of a machine learning workload. To estimate how much a neuron circuit’s lifetime changes due to the mapping of neurons and synapses to the hardware, we estimate the aging over the time duration of a workload, and then use it to extrapolate the lifetime, considering the same workload being executed repeatedly until one of the hardware components fails due to one of the failure mechanism. The lifetime measured as MTTF is

\[ MTTF = \int_{0}^{\infty} e^{(-A_{overall})^{\beta}}. \]

To compute MTTF, the slope parameter of Weibull distribution is set to \( \beta = 2 \), and the operating temperature is set to 300K. Other fitting parameters are adjusted to achieve an MTTF of 2 years in the baseline system. This is the typical lifetime of neuromorphic products.

IV. PROPOSED SOLUTION

A. High-Level Overview

Figure 6 shows a high-level overview of the workflow of RENEU, which can either directly input an SNN-based machine learning application or an artificial neural network (ANN)-based one after converting its ANN operations to SNN using the N2D2 tool [33], [35]. The SNN model is then partitioned into clusters, where each cluster accommodates a fixed number of neurons and synapses, and can fit on its entirety to a crossbar in the hardware. We use the clustering technique of the DFSynthesizer tool [14]. The clustered SNN model is then used by RENEU to find the mapping of the clusters to the crossbars using an instance of the PSO. We now describe in details the PSO step of RENEU.

B. PSO-based Cluster Mapping

We consider the mapping of a clustered SNN \( G(C, E) \) with a set \( C \) of clusters and a set \( E \) of edges, to the neuromorphic hardware \( H(T, I) \), where \( T \) is the set of tiles in the hardware and \( I \) is the set of connections of these tiles.

Mapping \( M : G(C, E) \rightarrow H(T, I) \) is specified by a logical matrix \((m_{ij}) \in \{0, 1\}^{\mid C \mid \times \mid T \}\), where \( m_{ij} \) is defined as

\[ m_{ij} = \begin{cases} 1 & \text{if cluster } c_i \in C \text{ is mapped to tile } t_j \in T \\ 0 & \text{otherwise} \end{cases} \]

The mapping constraints are the following:

1. A cluster can be mapped to only one crossbar, i.e.,

\[ \sum_{j} m_{ij} = 1 \quad \forall i \]

2. A crossbar can accommodate at most one cluster, i.e.,

\[ \sum_{i} m_{ij} \leq 1 \quad \forall j \]

We use an instance of Particle Swarm Optimization (PSO) [21] to obtain this mapping. The fitness function of
the PSO is a joint metric $\lambda$ defined as the product of aging and execution time. This metric $\lambda$ is computed as follows.

- $\tau_M$ = Execution time of mapping $M$, computed using the DFSynthesizer tool \[13\].
- $A_M$ = Aging of mapping $M$, computed using [18] with spike trains obtained from the SNN model.
- $\lambda_M = \tau_M \cdot A_M$. This is the fitness function.

The PSO finds the optimum mapping with the minimum value of the fitness function, i.e.,

$$\lambda_{M_{opt}} = \min_{{\lambda}_M \mid i \in 1, 2, \cdots},$$ (23)

We instantiate $n_p$ swarm particles. The position of these particles are solutions to the fitness function, and they represent cluster mappings, i.e., $M$’s in Equation (23). Each particle also has a velocity with which it moves in the search space to find the optimum solution. During the movement, a particle updates its position and velocity according to its own experience (closeness to the optimum) and also experience of its neighbors. We introduce the following notations.

$$D = |C| \times |V| = \text{dimensions of the search space}$$ (24)

$$\Theta = \{\theta_l \in \mathbb{R} \}_{l=0}^{n_l-1} = \text{positions of particles in the swarm}$$

$$\mathbf{V} = \{v_l \in \mathbb{R}^D \}_{l=0}^{n_l-1} = \text{velocity of particles in the swarm}$$

Position and velocity of swarm particles are updated, and the fitness function is computed as

$$\Theta(t+1) = \Theta(t) + \mathbf{V}(t+1)$$

$$\mathbf{V}(t+1) = \mathbf{V}(t) + \varphi_1 \cdot (P_{best} - \Theta(t)) + \varphi_2 \cdot (G_{best} - \Theta(t))$$

$$F(\theta_l) = \lambda_{\theta_l} = \tau_{\theta_l} \cdot A_{\theta_l}$$

where $t$ is the iteration number, $\varphi_1, \varphi_2$ are constants and $P_{best}$ (and $G_{best}$) is the particles own (and neighbors) experience. Finally, local and global bests are updated as

$$P_{best}^l = F(\theta_l)$$ if $F(\theta_l) < F(P_{best}^l)$

$$G_{best} = \min_{l=0, \ldots, n_p-1} P_{best}^l$$ (26)

Due to the binary formulation of the mapping problem (see Equation (20)), we need to binarize the velocity and position of Equation (24) which we illustrate below.

$$\mathbf{V} = \text{sigmoid}(\mathbf{V}) = \frac{1}{1 + e^{-\mathbf{V}}}$$

$$\Theta = \begin{cases} 0 & \text{if rand(1)} < \mathbf{V} \\ 1 & \text{otherwise} \end{cases}$$ (27)

In finding a new position of a PSO particle, we use the two constraints (21) and (22).

C. Pareto-Optimization

We record all mappings generated using the PSO. In the final step, we perform Pareto-optimization to select a mapping that maximizes aging without compromising performance. Figure 7 shows the Pareto front of LeNet-CIFAR application and selection of the final mapping.

V. RESULTS AND DISCUSSIONS

We conduct all simulations on a system with 8 CPUs, 32GB RAM, and NVIDIA Tesla GPU, running Ubuntu 16.04. We model the DYNAP-SE neuromorphic hardware \[2\] with four tiles. Each tile has one $128 \times 128$ crossbar with PCM synapses. We evaluate 10 standard machine learning applications obtained from [13] that are summarized in Table II.

![Figure 7: Pareto optimization.](image)

**TABLE II: Applications used to evaluate our approach.**

| Class      | Applications      | Synapses | Neurons | Topology             |
|------------|-------------------|----------|---------|----------------------|
| MLP        | EdgelDet          | 3,936    | 136,14  | FeedForward (690, 1024, 1024) |
| MLP        | Inception         | 5,904    | 980     | FeedForward (690, 1024) |
| MLP-MNIST  | CNN-MNIST         | 159,553  | 5,576   | CNN                  |
| CNN        | LeNet-MNIST       | 1,029,286| 4,634   | CNN                  |
| CNN        | LeNet-CIFAR       | 2,136,560| 18,472  | CNN                  |
| CNN        | HeartClass        | 1,396,521| 24,732  | CNN                  |
| CNN        | HeartEstm         | 636,578  | 6,952   | Recurrent Reservoir  |
| CNN        | SpeechReco        | 636,578  | 6,952   | Recurrent Reservoir  |
| CNN        | VisualPursuit     | 636,578  | 6,952   | Recurrent Reservoir  |
| RNN        | EFISynthesizer    | 636,578  | 6,952   | Recurrent Reservoir  |

- \(^a\) Input(24x24) - [Conv, Pool]*16 - FC*150 - FC*10
- \(^b\) Input(32x32) - [Conv, Pool]*16 - Conv*120 - FC*84 - FC*10
- \(^c\) Input(32x32x3) - [Conv, Pool]*16 - Conv*120 - FC*84 - FC*10
- \(^d\) Input(8x8x2) - [Conv, Pool]*16 - Conv*120 - FC*256 - FC*6

We evaluate the following state-of-the-art approaches.

- **PYCARL**: A performance-oriented approach to map neurons and synapses to a neuromorphic hardware \[13\].
- **Reliability Qualification**: A conservative reliability qualification technique, which estimates aging assuming worst-case operating conditions \[20\].
- **RENEU** (proposed): We use a detailed circuit aging model and use it to map neurons and synapses to a neuromorphic hardware improving reliability without compromising performance.

A. Lifetime Improvement

Figure 8 reports the MTTF of RENEU normalized to PYCARL for each of our machine learning applications. We observe that the MTTF of RENEU is better than PYCARL by an average of 18%. This improvement is because RENEU allocates clusters to tiles, minimizing the circuit aging of its crossbars. Lower aging leads to higher MTTF. We observe no noticeable improvement of MTTF for MLP-MNIST because this is a very small application to begin with.

B. Aging Reduction

Figure 9 reports the circuit aging caused by RENEU normalized to PYCARL for each of our machine learning...
applications. We observe that the aging of RENEU is lower than PYCARL by an average of 38%. This improvement is because RENEU formulates the detailed circuit aging of a neuromorphic hardware and allocates the neurons and synapses of a machine learning application to minimize it.

C. Temperature Dependency

Figure 10 illustrates the temperature dependency of circuit aging in a neuromorphic hardware. We report the aging results of RENEU at two elevated temperatures, 325K and 350K, for each of our machine learning applications. Aging results are normalized to RENEU at 300K. We observe that aging increases with an increase in temperature. Aging observed at 325K and 350K is higher than that observed at 300K by an average of 7% and 26%, respectively. These results follow from our aging formulation, which incorporates temperature using the scaling parameter $\alpha$ in (5) for TDDB and the parameter $g_0$ in (15) for NBTI. These parameters grow exponentially with temperature, resulting in a corresponding exponential increase in the aging. Higher aging leads to lower lifetime.

D. Diode vs. Transistor-based PCM

Figure 11 reports the circuit aging in a neuromorphic hardware with transistor-based PCM normalized to RENEU which uses diode-based PCM. We report results for each of our machine learning applications. We observe that the aging of a neuromorphic hardware with transistor-based PCM is on average 10% lower than diode-based PCM. This is because the operating voltages of a neuromorphic hardware are comparatively lower for transistor-based PCM, which reduces the circuit aging. However, a diode-based PCM cell is 33% smaller than a transistor-based PCM cell, which means that diode-based PCM cells can implement neuromorphic hardware with high integration density. Nevertheless, our approach RENEU can be applied to improve reliability of neuromorphic hardware with both diode and transistor-based PCM.

E. Performance Impact

Figure 12 reports the performance of RENEU measured as the execution time normalized to PYCARL for each of our machine learning applications. We also report the results of a conservative reliability qualification technique, which periodically de-stresses a neuron circuit to achieve similar MTTF as RENEU [20]. We make the following two observations. First, the execution time of a machine learning application using RENEU is within 5% of the execution time of PYCARL. This is because RENEU incorporates both performance and reliability when finding a suitable mapping of neurons and synapses to the neuromorphic hardware. Second, to achieve a similar MTTF as RENEU, existing conservative flavor of PYCARL periodically de-stresses the neuron circuit, which introduces an average performance overhead of 35%.
F. Circuit Aging with More Crossbars

Figure [3] reports the circuit aging as the amount of hardware resources are increased. We report the aging results of RENEU with 9 and 16 crossbars for each of our machine learning applications. Aging results are normalized to RENEU with 4 crossbars. We make the following two observations. First, aging reduces with increasing number of crossbars. This is because with more crossbars in the system, the average load on each crossbar reduces, which in turn reduces the stress on its CMOS devices. Lower stress reduces the circuit aging. With 9 and 16 crossbars, the average circuit aging is respectively, 24% and 29% lower than RENEU with 4 crossbars. Second, for MLP-MNIST, there is no noticeable improvement. This is because MLP-MNIST is a small application to begin with.

Fig. 13: Circuit aging of RENEU with 9 and 16 crossbars normalized to RENEU with 4-crossbars (lower is better).

G. Optimization Time

Table [III] reports the optimization time (measured as wall clock time) of RENEU in finding a mapping using the proposed PSO. The optimization time depends on the size of the application. The MLP-MNIST, which is a small application requires 4.6s, while LeNet-CIFAR requires 98.2s.

TABLE III: Optimization time of RENEU.

| Application     | Time (s) | Application     | Time (s) |
|-----------------|---------|-----------------|---------|
| EdgeDet         | 53.1    | ImgSmooth       | 47.2    |
| MLP-MNIST       | 4.6     | CNN-MNIST       | 84.4    |
| LeNet-MNIST     | 70.12   | LeNet-CIFAR     | 98.2    |
| HeartClass      | 14.6    | HeartEstm       | 59.93   |
| SpeechRecog     | 82.0    | Visual Pursuit  | 90.8    |

VI. CONCLUSION

We present RENEU, a reliability-oriented approach for mapping neurons and synapses to the hardware resources of a Non-volatile Memory (NVM)-based neuromorphic hardware. Prior efforts in mapping neurons and synapses have mostly considered performance. RENEU is built on two key contributions. RENEU formulates the detailed circuit aging in a neuromorphic hardware considering different failure mechanisms such as Time Dependent Dielectric Breakdown (TDDDB), Negative Bias Temperature Instability (NBTI), and Hot Carrier Injection (HCI). Using this formulation RENEU places the neurons and synapses to the hardware using an instance of Particle Swarm Optimization (PSO), exploring the performance and reliability trade-offs. We evaluate RENEU using machine learning applications on a state-of-the-art neuromorphic hardware with PCM synapses. Results demonstrate a significant improvement in reliability of neuromorphic computing with marginal impact on performance.

ACKNOWLEDGMENT

This work is supported by the National Science Foundation Faculty Early Career Development Award CCF-1942697 (CA- REER: Facilitating Dependable Neuromorphic Computing: Vision, Architecture, and Impact on Programmability).

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