RESEARCH ARTICLE

TUNABLE MIXED DECIMATION MULTIPATH DELAY FEEDBACK FOR RADIX $2^k$ FFT.

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Abstract

The Decimation Multipath Delay Feedback (M²DF) is a technique for the radix $2^k$ FFT, which eliminates the standby time of arithmetic modules in computing units. In this paper tunable M²DF architecture is proposed. In this, tunable arithmetic units are utilized in place of conventional arithmetic units to overcome the under utilization of arithmetic units in conventional M²DF architecture. The results show that, the tunable M²DF technique utilizes the lesser number of LUTs and slice registers than the conventional M²DF technique. In addition, the proposed technique having advantage of high throughput with reduced delay and area compared with conventional M²DF.

Introduction:

Fast Fourier Transform (FFT) is mostly used algorithm for Discrete Fourier Transform computation in the field of signal processing. The area efficient and high performance FFT implementation throws a challenge on the designers. Hardware designers are putting effort to design effectual architectures for the computation of the FFT to meet required specifications and real-time fulfillment of present applications. Various techniques have proposed over the years to tradeoff the area and performance of the FFT. Pipelined architectures [1] are extensively used because they will achieve more throughputs and small latencies relevant for today’s applications to achieve small area and to dissipate less power. The single path delay commutator (SDC) [2] is the most popular technique in the serial input and serial output scenarios. Single path delay feedback (SDF) architecture is proposed to reduce the memory banks in the pipelines [3]. The SDF concept extended to radix 2 to radix $2^k$ [4-6]. The high throughput requirements of communication services encouraged to multipath delay commutators [7] and multipath delay feedback (MDF) [8].

The MDF structures are formed using multiple interconnected SDFs. The MDF scheme is utilized in various applications due to its efficient memory usage, but suffers from arithmetic resource utilization and it is rectified in M²DF architecture [9], which utilizes the folding transformation technique for the significant reduction of arithmetic resources.

In this work, tunable M²DF architecture is proposed to further reduce the arithmetic operations in terms of number of LUTs and registers.

Construction of M²DF Architecture:

Design of parallel radix-$2^k$ FFT processor based on folding transformations to derive the folding matrices of DIF and DIT of SDF structures. The pipelined structure is rescheduled by incorporating DIF blocks into DIT blocks to form M²DF architecture from the SDF architecture. The M²DF mainly focus on horizontal processing in relevant to the hardware implantations and is shown in Fig.1

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**Arithmetic Unit:**
The M^2DF architecture mainly consists of control circuit and arithmetic unit and mathematics unit. Among them arithmetic unit plays an important role.

Fig. 1: M^2DF Architecture

Fig. 2: (a) Type I structure, complex adders are shared only
Conventionally two different structures are used. One is Type-I, In this adders are shared by means of streams and is shown in Fig. 2(a). Another type of arithmetic unit is Type – II, In this type adders and multipliers are reused to pick up the equipment effectiveness and is shown in Fig. 2(b).

**Proposed M²DF Architecture using the tunable Arithmetic Unit:-**
In the modified M²DF architecture the conventional arithmetic units are modified using tunable arithmetic units, while maintaining the feedback structure of conventional architecture.

**Tunable Arithmetic unit:-**
Fig. 3 shows the tunable arithmetic unit. In this 4-stage pipelined technique is adopted. This unit consists of 6 butterfly units and 3 complex multipliers. Compared to type I and type II AU’s the proposed AU having high throughput and consumes less area. Due to the tunable arithmetic unit, the inexact multiplier configurations have much higher sensitivities than the most of the inexact adder configurations and the pipelined technique is effectively utilized. Due to these advantages tunable arithmetic unit has a double impact on the quality of solutions.
Simulation Results:
The simulation of the proposed M^2DF architecture and the conventional M^2DF architectures are carried out using Xilinx ISE 14.5. The simulation results are shown in Fig.4. (These Two parallel 512 point FFT designed using proposed tunable arithmetic unit).

| Name            | Value                                                                 |
|-----------------|------------------------------------------------------------------------|
| data_out[31:0]  | 00000000000000000000000000000000...                                  |
| clk             | 1                                                                     |
| data_in[a][511:0]| 00000000000000000000000000000000...                                  |
| data_in[b][511:0]| 00000000000000000000000000000000...                                  |
| data_out[a][511:0]| 00000000000000000000000000000000...                                  |
| data_out[b][511:0]| 00000000000000000000000000000000...                                  |
| [32:0]          | 00000000000000000000000000000000...                                  |

Fig. 4: Simulation results for Tunable M^2DF Architecture for radix-2 512 point FFT.

Here data_in_a and data_in_b are inputs indicates the iteration loops and data_out is the required output. The corresponding RTL schematic of radix-2 two parallel 512 point FFT architecture is shown in Fig. 5.

Fig. 5: RTL Schematic for tunable M^2DF of radix-2 for 512 point FFT.

Similarly, the two parallel 1024 point FFT, two parallel 2048 point FFT and their RTL schematics are shown in Fig. 6 to Fig. 9.

Fig. 6: Simulation results for tunable M^2DF Architecture for radix-2 1024 point FFT.
Fig. 7: RTL Schematic for tunable M’DF of radix-2 for 1024 point FFT.

Fig. 8: Simulation results for tunable M’DF Architecture for radix-2 2048 point FFT.

Fig. 9: RTL Schematic for M’DF of radix-2 2048 point Fast Fourier Transform.

Table 1: Comparison of proposed structure with existing structures

| Configuration | Structures               | Slice LUTs | Slice registers | DSP48E1s | latency | throughput |
|---------------|--------------------------|------------|----------------|----------|---------|------------|
| Radix-2, 2/512| M’DF FFT Architecture    | 2417       | 2077           | 24       | 524     | 612        |
|               | Tunable M’DF FFT Architecture | 1140       | 1219           | 20       | 516     | 618        |
| Radix-2, 4/1024| M’DF FFT Architecture     | 3154       | 3881           | 36       | 533     | 1196       |
|               | Tunable M’DF FFT Architecture | 2060       | 2139           | 30       | 523     | 1238       |
Radix-2, 8/2048  M^2DF FFT Architecture  6833  8860  84  542  2368  
Tunable M^2DF FFT Architecture  4012  4678  70  530  2463  
Radix-2^2, 2/512  M^2DF FFT Architecture  3345  2790  24  524  612  
Tunable M^2DF FFT Architecture  1565  1780  24  513  613  
Radix-2^3, 4/1024  M^2DF FFT Architecture  3885  3112  36  533  1196  
Tunable M^2DF FFT Architecture  2451  2696  32  519  1224  
Radix-2^3, 8/2048  M^2DF FFT Architecture  8753  5631  84  540  2368  
Tunable M^2DF FFT Architecture  11207  14836  176  531  2398  
Radix-2^4, 2/512  M^2DF FFT Architecture  3436  3033  24  526  596  
Tunable M^2DF FFT Architecture  1682  1717  24  518  613  
Radix-2^3, 4/1024  M^2DF FFT Architecture  5112  4225  48  536  1186  
Tunable M^2DF FFT Architecture  3505  3992  44  528  1224  
Radix-2^3, 8/2048  M^2DF FFT Architecture  9062  10265  286  540  2372  
Tunable M^2DF FFT Architecture  8446  8542  280  532  2398  

Conclusion:
The Radix-2 M^2DF based Fast Fourier Transform is most significant architecture in the DSP and various Communication systems. The FFT architecture used in the mixed decimation Multipath Delay feedback (M^2DF) eliminates the stand by time of arithmetic modules in FB architectures by integrating Discrete In Time process into the Discrete In Frequency operated computing units. Still arithmetic resources are under utilization in order to overcome this problem uses the tunable FFT is used in the place of type I and type II of arithmetic units (AUs).
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