Bit Error Rates of Flip-Flop Operations with AND Gate Functionality using a 1.55-µm Polarization Bistable VCSEL

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Abstract: Bit error rates (BERs) of all-optical flip-flop operations with AND-gate functionality using a 1.55-µm polarization bistable vertical-cavity surface-emitting laser (VCSEL) were measured. Optical data pulses of a 500-Mb/s return-to-zero pseudo-random bit-sequence were used. The best BER we obtained was 5.00×10⁻⁹ and the eye diagram was clearly open. Input-pulse power was about 17 dB lower than VCSEL output power. From the BER variation for the set-pulse power under fixed data-pulse power, we found that fluctuations in the switching threshold and power of AND pulse (combination of data and set pulses) affect the BER. We also evaluated the BER of memory operations.

Keywords: All-optical signal processing, bit error rate (BER), optical memory, optical flip-flop, polarization bistability, vertical-cavity surface-emitting laser (VCSEL)

Classification: Optoelectronics, Lasers and quantum electronics, Ultrafast optics, Silicon photonics, Planar lightwave circuits

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1 Introduction

All-optical flip-flops with set and reset signals can be used to perform many optical signal processing functions in future networks. Examples of such applications are: as regenerate memory elements, as storage of the header information of a packet, as basic building blocks of optical shift registers and optical counters, and in threshold function and self-routing. All-optical flip-flop having AND gate functionality with three optical inputs of data, set, and reset signals have more sophisticated functions, because only the data bit, whose timing is adjusted to the set pulse, is memorized. Thus, it can be used as optical sampling memory for optical drop and insert [1], for optical buffer memory [2, 3, 4], and for storage of the header information of a packet [5, 6, 7].

A polarization bistable vertical-cavity surface-emitting laser (VCSEL) is promising as a suitable bistable device for developing small, low-power-consumption systems because it can be easily constructed in an array of VCSELs and has a small operation current. The VCSEL has two lasing modes with polarization directions orthogonal to each other, and it exhibits bistable characteristics in regard to these two polarization states. The polarization direction can be switched by injecting an optical pulse. A polarization bistable VCSEL can thus be operated as a 1-bit optical flip-flop memory. An optical buffer memory with a shift-register function, consisting of a two-dimensional array of polarization bistable VCSELs, was previously proposed [2]. The memory operation was based on a flip-flop operation with AND-gate functionality. After that, a 4-bit optical buffer memory using four 1.55-μm VCSELs, in which two sets of shift-register
memories were connected in parallel, was demonstrated [3]. Next, fast memory operations using a 980-nm VCSEL, in which one bit was arbitrarily selected from 20-Gb/s RZ data signals and 40-Gb/s non-return-to-zero (NRZ) data signals and then stored, were reported [4]. This memory operation was applied to all-optical header recognition for optical packet switching at 1.55 µm. Payloads with 500-Mb/s RZ pseudo-random bit-sequence (PRBS) [5] and 40-Gb/s NRZ PRBS [6] formats were switched to two designated ports according to the state of one bit in a 4-bit header with the 500-Mb/s RZ format. Recently, a 2-bit header recognition and packet switching have been demonstrated using two 1.55-µm polarization bistable VCSELs [7].

Stability of operation is one of the most important features in all-optical signal processing. Thus, the bit error rates (BERs) have been evaluated for many kinds of all-optical flip-flop operations such as a two-section bistable laser diode including a saturable absorber [1], a semiconductor ring laser [8], an optical static random access memory cell based on a semiconductor optical amplifier–Mach-Zehnder interferometer [9], a contention resolution circuit that employs cascaded wavelength converters connected to both ports of single integrated optical flip-flop [10], and an optical 3R flip-flop using a single mode Fabry-Pérot laser diode [11]. We measured the BER of all-optical flip-flop operations using a 1.55-µm VCSEL and obtained a good BER of $1.56 \times 10^{-10}$ at 1 Gb/s using set and reset pulses with lower power than VCSEL output power [12]. Regarding all-optical flip-flops having AND gate functionality, the BER have not been evaluated except the work in Ref. [1]. In optical flip-flops with AND gate functionality, the range of optical input power for proper operation becomes narrow because of the AND gate operation. Therefore, we need to evaluate the BER apart from flip-flops without AND-gate functionality.

In this study, the BER of the flip-flop operation with AND-gate functionality and that of an optical memory operation using a 1.55-µm polarization bistable VCSEL were measured. After the best BER and the corresponding eye diagram were obtained, the BER variation for the set-pulse power under fixed data-pulse power was investigated and compared with the calculated BER variation to clarify the origin of the BER deterioration. In optical memory operation, the BER of the operation in which one bit was selected from RZ PRBS data signals and stored for various bit rates was measured.

2 BER measurement of flip-flop with AND-gate functionality

2.1 Best BER and eye diagram
Flip-flop operation with AND-gate functionality is achieved using the implementation shown in Fig. 1(a). The input powers of both the data and set pulses are set to less than the threshold of the polarization bistable switching of the VCSEL. If a set pulse with 0° polarization is injected simultaneously with a “1” data pulse, and the total input power of the data and set pulses exceeds the switching threshold, and the polarization state of the VCSEL switches from 90° to 0°. A polarizer placed after the VCSEL converts the polarization bistable switching of the VCSEL output into on/off switching.
The timing chart of input pulses and corresponding VCSEL output signals is shown in Fig. 1(b). Input pulses with 1-ns duration were used. The data pulses had a format of $2^{11}-1$ PRBS, and the set and reset pulses had a repetitive pattern. The reset-pulse pattern was delayed from the data-pulse pattern by a half cycle. The duty ratio of the data and reset pulses was 1/8. The period of the set pulses was set to twice that of the data pulses to examine the four situations in which the data and set pulses are “0,0”, “1,0”, “0,1”, and “1,1”.

The experimental setup for measuring the BER is shown in Fig. 2. To obtain operations with small input-pulse power, two tunable laser diodes and three lithium-niobate modulators were used to adjust the wavelengths of the data/set pulses and reset pulse independently [12]. After the data and set pulses (with 0° polarization) were combined using a 3-dB coupler, the reset pulse (with 90° polarization) was combined through a polarization beam combiner. The polarization angles of the input pulses were aligned toward 0° or 90° by using a polarization controller, and they were maintained until the pulses were injected into the VCSEL through a circulator. At the combination of the data and set pulses,
a proportional-integral-derivative (PID) control system was used to minimize the drift of the phase differences between them. The clock signal from a pulse-pattern generator, whose frequency was reduced into a quarter by a prescaler, was fed into an error detector because the duration of the VCSEL 0° output was four times longer than that of the input pulses. The bias current of the VCSEL was set to 7.99 mA in the bistable region at 20°C. The VCSEL output power was −3.0 dBm, and the lasing wavelengths were 1550.480 and 1550.375 nm for 0° and 90° polarization lasing, respectively.

The power and wavelengths of the input pulses were adjusted to obtain as good a BER as possible for the flip-flop operation with AND-gate functionality. As a result, the best BER of 5.00×10⁻⁹ was obtained and the eye diagram was clearly opened (Fig. 3). The input-pulse powers were −19.8, −19.7, and −20.0 dBm for data, set, and reset pulses, respectively. These powers were 16.6-17.0 dB lower than VCSEL output power; thus, this flip-flop operation had a large optical gain. Moreover, the data-pulse power was almost the same as the set-pulse power. Multiple peaks were observed when the data and set pulses were injected. They are considered to represent the relaxation oscillation of the VCSEL output [12, 13, 14, 15].

2.2 BER variation for set-pulse power
The data-pulse power was fixed to −19.8 dBm, at which the best BER (5.00×10⁻⁹) was obtained. The BER variation was investigated by changing the set-pulse power. The experimental results are shown in Fig. 4. The BER deteriorated when the set-pulse power was increased or decreased from −19.7 dBm. The BER deterioration with increasing set-pulse power was more noticeable than that with decreasing set-pulse power. Therefore, BER variation depicts a right-left asymmetric “V” shape.

To clarify the main factors that affected BER variation, it was numerically calculated by changing the set-pulse power. For this calculation, the following two assumptions were made.

Assumption 1: The BER of flip-flop operation with AND-gate functionality can be calculated from the sum of the following two probabilities: the probability that the data- or set-pulse power is above the switching threshold, and the probability that the power of the AND pulse (made by the combination of the data and set pulses) is below the switching threshold.

![Fig. 3. Eye diagram of optical flip-flop operation with AND-gate](image-url)
Assumption 2: The switching threshold fluctuates, and the probability density of the switching threshold $f_{th}$ for power $p$ can be expressed by a Gaussian function having a peak at $P_{th}$, i.e.,

$$f_{th}(p) = \frac{1}{\sqrt{2\pi} \sigma_{th}} \exp\left(-\frac{(p-P_{th})^2}{2 \sigma_{th}^2}\right), \quad (1)$$

where $\sigma_{th}$ is the standard deviation of the switching threshold. Fluctuations in the data-, set-, and AND-pulse powers were assumed to be negligible.

Under Assumptions 1 and 2, the BER was calculated. The AND-pulse power $P_A$ can be calculated as

$$P_A = \left(\sqrt{P_D} + \sqrt{P_S}\right)^2, \quad (2)$$

where $P_D$ and $P_S$ are the data- and set-pulse powers, respectively. Since there are four combinations of data and set pulses “0, 0”, “1, 0”, “0, 1”, and “1, 1”, and each occurs with the same probability, the BER is calculated as [16],

$$\begin{align*}
\text{BER} &= \frac{1}{4} \int_{-\infty}^{P_D} \frac{1}{\sqrt{2\pi} \sigma_{th}} \exp\left(-\frac{(p-P_{th})^2}{2 \sigma_{th}^2}\right) dp + \frac{1}{4} \int_{-\infty}^{P_S} \frac{1}{\sqrt{2\pi} \sigma_{th}} \exp\left(-\frac{(p-P_{th})^2}{2 \sigma_{th}^2}\right) dp \\
&\quad + \frac{1}{4} \int_{P_A}^{\infty} \frac{1}{\sqrt{2\pi} \sigma_{th}} \exp\left(-\frac{(p-P_{th})^2}{2 \sigma_{th}^2}\right) dp \\
&\quad + \frac{1}{8} \left[ \text{erfc}\left(\frac{P_{th}-P_D}{\sqrt{2} \sigma_{th}}\right) + \text{erfc}\left(\frac{P_{th}-P_S}{\sqrt{2} \sigma_{th}}\right) + \text{erfc}\left(\frac{P_A-P_{th}}{\sqrt{2} \sigma_{th}}\right) \right]. \quad (3)
\end{align*}$$

The first (second) term corresponds to “1, 0” (“0, 1”) and means the probability that the data (set)-pulse power is above the switching threshold. The third term corresponds to “1, 1” and means the probability that the AND-pulse power is below the switching threshold. Note that “0, 0” does not increase the BER. And “erfc” stands for the error function, defined as

$$\text{erfc}(x) = \frac{2}{\sqrt{\pi}} \int_x^{\infty} \exp(-y^2) \, dy. \quad (4)$$

After a certain value for parameter $P_{th}$ was assumed, $\sigma_{th}$ was determined in such a way that the experimentally measured BER at the smallest set-pulse power (BER=$4.36 \times 10^{-3}$ at $-27.2$ dBm) was reproduced. The BER variation for the
set-pulse power was calculated from Eq. (3). In this calculation, the $P_{th}$ values of 17.5, 18.0, 18.5, and 19.0 $\mu$W were adopted, and the corresponding $\sigma_{th}$ values were 1.88, 1.64, 1.41, and 1.17 $\mu$W, respectively. The calculation results are shown in Fig. 4(a). The calculated BERs as set-pulse power increased from $-19.7$ dBm agreed well with those of the experiment. The BERs calculated using $P_{th}=18.5$ or 19.0 $\mu$W particularly well reproduced the measured BERs. However, the calculated BERs as set-pulse power decreased from $-19.7$ dBm disagreed with those of the experiment. Whatever value of $P_{th}$ was adopted, the disagreement with the experiment at weak set-pulse power did not disappear.

The main origin of BER deterioration with increasing set-pulse power from $-19.7$ dBm is considered to be the increase in the probability of the set-pulse power exceeding the switching threshold, and this probability is described considering switching-threshold fluctuation. On the other hand, the main origin of BER deterioration with decreasing set-pulse power from $-19.7$ dBm is considered to be the increase in the probability of the AND-pulse power falling below the switching threshold, and it is insufficient to consider only the switching-threshold fluctuation to describe this probability. In Assumption 2, the fluctuations in the data-, set-, and AND-pulse powers were ignored. Among these pulses, the AND pulse might have a larger power fluctuation than the other two pulses because of the interference between the data and set pulses, although the PID control system minimized the phase difference. Assumption 2 was therefore changed as follows.

Assumption 2': In addition to the switching threshold considered in Eq. (1), the AND-pulse power also fluctuated, and the probability density of the AND-pulse power $f_A$ can be expressed by a Gaussian function having a peak at $P_A$, i.e.

$$f_A(p) = \frac{1}{\sqrt{2\pi}\sigma_A} \exp\left(-\frac{(p-P_A)^2}{2\sigma_A^2}\right),$$

(5)

where $P_A$ is the AND-pulse power derived from Eq. (2), and $\sigma_A$ is its standard deviation assumed to be written using the relative error $\varepsilon_A$ as

$$\sigma_A = \varepsilon_A P_A.$$  

(6)

The BER was calculated under Assumptions 1 and 2'. The probability that the data (set)-pulse power is above the switching threshold is the same as the first (second) term of Eq. (3). However, the probability that the AND-pulse power is below the switching threshold is different from the third term of Eq. (3). Thus, the BER is given as

$$\text{BER} = \frac{1}{8} \left[ \text{erfc}\left(\frac{P_{th}-P_D}{\sqrt{2}\sigma_{th}}\right) + \text{erfc}\left(\frac{P_{th}-P_S}{\sqrt{2}\sigma_{th}}\right) \right]$$

$$+ \frac{1}{4} \int_{-\infty}^{\infty} \frac{1}{\sqrt{2\pi}\sigma_A} \exp\left(-\frac{(p-P_A)^2}{2\sigma_A^2}\right) \frac{1}{\sqrt{2\pi}\sigma_A} \exp\left(-\frac{(p-P_{th})^2}{2\sigma_{th}^2}\right) dp.$$  

(7)

Note that $P_A$ derived from Eq. (2) is the power on condition that the data and set pulses are combined in the same phase. If it is assumed that the origin in the fluctuation of $P_A$ is the fluctuation in the phase difference between the data and set pulses, the assumption including the $p > P_A$ element in $f_A(p)$ is not rigorously accurate. However, the contribution to the BER from the overlap of the $p > P_A$ element in $f_A(p)$ and $f_{th}(p)$ in Eq. (7) was considered to be small enough, and the conventional Gaussian form of Eq. (5) was used.
The parameters $P_{th}=19.0 \mu W$ and $\sigma_{th}=1.17 \mu W$ were adopted because the BERs calculated using these parameters under Assumptions 1 and 2 agreed best with the measured BERs. After a certain value of $\varepsilon_A$ was assumed, the BER variation for the set-pulse power was calculated from Eq. (7). The BERs when $\varepsilon_A$ was 0.08, 0.09, 0.10, and 0.11 are shown in Fig. 4(b). The BERs with both increasing and decreasing set-pulse power from $-19.7 \text{ dBm}$ agreed well with the measured ones. The BERs calculated using $\varepsilon_A=0.09$ particularly well reproduced the measurement.

These BER calculations clearly show that the measured BER variation for the set-pulse power is described well by considering switching-threshold fluctuation and AND-pulse-power fluctuation. The calculation adopting the parameters $P_{th}=19.0 \mu W$, $\sigma_{th}=1.17 \mu W$, and $\varepsilon_A=0.09$ particularly well reproduced the measured BER variation. Namely, the BER variation is well described by considering that the switching threshold fluctuates by about $\pm6\%$ and the AND-pulse power fluctuates by about $\pm9\%$ due to the phase difference between the data and set pulses. A $9\%$ reduction in the AND-pulse power corresponds to about a $\pm35\degree$ difference in the phase angles for $P_D = P_S$.

### 3 BER measurements of optical memory operations

The BER of optical memory operation, in which one bit was selected from data-bit sequences then stored, was measured by using the same experimental setup shown in Fig. 2. A timing chart of optical memory operation is shown in Fig. 5. The difference between this optical memory operation and the flip-flop operation described in section 2 is that some data bits are injected until the injection of reset pulse. One data bit is sampled using the AND gate functionality and is memorized. To evaluate the BER difference due to the pattern effect of the VCSEL, two cases were evaluated: the case in which the set pulse was injected with the first data bit (referred to as the “first-bit AND” case), and the case in which the set pulse was injected with the last data bit (referred to as the “last-bit AND” case). Because the 4-ns interval was longer than the duration of relaxation oscillations, the effect of

![Fig. 5. Timing chart of optical memory operation. This chart shows case in which first bit is memorized for 500 Mb/s. Data pulse had format of RZ 2^11–1 PRBS. Data-bit sequence was decomposed into packets of 4-ns in length with intervals of 4 ns. Set pulses with same duration as data pulses and with 8-ns period were injected simultaneously with one bit of data-bit sequence. Reset pulses with same duration as data pulses and with 8-ns period were delayed from first data bit by 6 ns.](image-url)
the last data bit of the previous packet to the VCSEL could almost be negligible when the first data bit of the next packet was injected. The chart shown in Fig. 5 represents the optical memory operation in the first-bit AND case. The reset pulses with the same duration as the data pulses and with an 8-ns period were delayed from the first data bit by 6 ns to ensure that the switched state was stored for more than 2 ns until the next switching. When the bit rate of the data pulses was changed, the duration of the set and reset pulses was set to the same value as that of the data pulse, but the packet length (4 ns), interval (4 ns), and period of set and reset pulses (8 ns) were all fixed.

Eye diagrams and BERs of the optical memory operations for bit rates of 500 Mb/s ~ 3 Gb/s are shown in Fig. 6. The power and wavelengths of the input pulses were adjusted to obtain the best BER. Open eye diagrams and BERs better than $1.00 \times 10^{-7}$ were obtained in both the first- and last-bit AND cases at 500 Mb/s. As bit rate increased, the eye diagrams became closed and BER deteriorated. At 3 Gb/s, the eyes were hardly open, and BERs were worse than $1.00 \times 10^{-2}$. For each bit rate, the BER in the last-bit AND case was better than that in the first-bit AND case. This may be because in the first-bit AND case, the VCSEL output signals fluctuated when the data pulses with 0° polarization were injected after the polarization of the VCSEL was switched to 0°.

As bit rate increased, the pulsewidths of the data and set pulses became shorter, and larger pulse power was required for polarization bistable switching. When the number of data bits increases, the accumulated pulses in the cavity changes the number of carriers in the active region of the VCSEL; consequently, undesired polarization bistable switching occurs even when the set pulse and “1” data bit are not simultaneously injected. As a result, the range of input-pulse power for proper AND-gate operation becomes narrow. An example of narrowing the range of input-pulse power for proper AND-gate operations is shown in Fig. 7. An input waveform and output waveform in the 3-Gb/s last-bit AND case are shown in Fig. 7(a). The set pulse was injected when the data bit was “0” in the left half of the

![Fig. 6. Eye diagrams and BERs of optical memory operations for bit rate of 500 Mb/s ~ 3 Gb/s. Upper (lower) panels show results for first (last)-bit AND case.](image)
figure, and the set pulse was injected simultaneously with the fourth “1” data bit in the right half. In the left half, although switching to 0° polarization should not occur, a precursor of undesirable switching was observed after eight data bits were injected. On the other hand, in the right half, although switching to 0° polarization occurred, the switched state was not fully stored. Waveforms in which the set (data)-pulse power was increased by 1 dB to fully store the switched polarization state in the right half are shown in Fig. 7(b) (Fig. 7(c)). In both figures, the storage times of the switched state became longer, but the precursor of undesirable switching became larger in the left half.

The input-pulse powers were set to −24.4 ~ −17.2 dBm to obtain the eye diagrams shown in Fig. 6. These powers were much smaller than the VCSEL output power (−3.0 dBm). This means that the optical memory operations had large optical gain in the range of 21.4 ~ 14.2 dB. The set-pulse power became larger than the data-pulse power as bit rate increased because the data-pulse power was suppressed to avoid undesirable switching due to the data-pulse accumulation. The magnitudes of frequency detuning were 2.1 ~ 3.9 GHz for the data and set pulses and 0.2 ~ 3.5 GHz for the reset pulses. Here, the frequency detuning of the data and set (reset) pulses is defined as the frequency difference relative to the VCSEL lasing frequency in the 0° (90°) polarization state.

One solution to avoid the problem due to the data-pulse accumulation and to obtain good BERs for higher bit rates is to increase the amount of frequency detuning of the data and set pulses. By doing this, the photon lifetime in the cavity is reduced and the pulse accumulation is suppressed [17]. As shown in Fig. 5 of Ref. [12], a larger amount of frequency detuning requires larger optical power of the input pulse for polarization bistable switching. To amplify the data and set pulses, an erbium-doped fiber amplifier and a band-pass filter before the PBC were added to the experimental setup shown Fig. 2, and the BER of optical memory operations was then measured in the case in which pulses with large amount of

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**Fig. 7.** Effect of data pulses accumulation. (a) Waveform for 3 Gb/s last-bit AND case in which BER of $1.43 \times 10^{-2}$ was obtained. (b) ((c)) Waveform in which the set (data)-pulse power was increased by 1 dB.
frequency detuning were injected. The obtained eye diagrams and BERs are shown in Fig. 8. In both the first- and last-bit AND cases at 3 Gb/s, the eye diagrams clearly opened, and the BERs improved by about two orders of magnitude compared to those at 3 Gb/s in the small-detuning cases. The BERs for bit rates higher than 3 Gb/s could be measured, and open eyes were obtained. The transients of the VCSEL output from 90° to 0° in the large-detuning cases were slower than those in the small-detuning cases. This may be because the power of the input pulses was not sufficient for fast switching. However, when pulses with larger power were injected, proper AND-gate operations were not obtained, and BER deteriorated.

The relation between measured BER and bit rate is summarized in Fig. 9 for BERs in both the small- and large-detuning cases shown in Figs. 6 and 8. The pulse powers and magnitudes of frequency detuning of input pulses in which the best BERs were obtained are shown in Fig. 10. The input-pulse powers were $-13.4 \sim -5.9$ dBm in the large-detuning cases. The optical gains were $10.3 \sim 2.8$ dB, which were smaller than those in the small-detuning cases instead of BER improvements. The magnitudes of frequency detuning were $8.6 \sim 10.0$ GHz for the data and set pulses and $1.7 \sim 3.5$ GHz for the reset pulses in the large-detuning cases. The

![Fig. 8. Eye diagrams and BERs of optical memory operations using optical pulses with large amount of frequency detuning for bit rate of 3 ~ 6 Gb/s. Upper (lower) panels show results for first (last)-bit AND case.](image)

![Fig. 9. Bit rate dependence of BER of optical memory operations. Circles (triangles) are for first (last)-bit AND case. Solid (broken) eye guides are for case using pulses with small (large) amount of frequency detuning.](image)
The BERs of flip-flop operations with AND-gate functionality and optical memory operations using a 1.55-μm polarization bistable VCSEL were measured. In the flip-flop operations with AND-gate functionality using 500-Mb/s RZ input pulses, the best BER \(5.00 \times 10^{-9}\) was obtained when the data-pulse power was almost the same as the set-pulse power. The BER variation for the set-pulse power under fixed data-pulse power was investigated and showed that fluctuations in switching threshold and AND-pulse power affect the deterioration of BER.

In the case of optical memory operations at which the magnitudes of frequency detuning of data and set pulses were less than 4 GHz, proper memory operations at 500 Mb/s ~ 3 Gb/s were obtained. However, the eye diagram of VCSEL output closed, and BER deteriorated with increasing bit rate. To avoid difficulty due to data-pulse accumulation in the VCSEL, input pulses with a large amount of frequency detuning of about 10 GHz were used. Although the optical gain was reduced, BERs at 6 Gb/s were better than those at 3 Gb/s in the small-detuning case.

These results suggest that polarization bistable VCSELS are applicable to all-optical flip-flops with AND gate functionality and all-optical memories having optical gain and will provide stable operations with good BER.

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