Performance Reproduction and Prediction of Selected Dynamic Loop Scheduling Experiments

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Abstract

Scientific applications are complex, large, and often exhibit irregular and stochastic behavior. The use of efficient loop scheduling techniques, from static to fully dynamic, in computationally-intensive applications characterized by large data-parallel loops, is crucial for improving their performance, often degraded by load imbalance, on high-performance computing (HPC) platforms. A number of dynamic loop scheduling (DLS) techniques has been proposed between the late 1980's and early 2000's and efficiently used in scientific applications. In most cases, the computing systems on which they have been tested and validated are no longer available. The use of DLS for the purpose of improving the performance of computationally-intensive scientific applications executing on modern HPC platforms is of increased significance today as system-induced load imbalance is exacerbated due to systems diversity, complexity, increased size, increased heterogeneity, and massively parallel nature. This work is concerned with the minimization of the sources of uncertainty in the implementation of DLS techniques to avoid unnecessary influences on the performance of scientific applications. Therefore, it is important to ensure that the DLS techniques employed in scientific applications today adhere to their original design goals and specifications. The goal of this work is to attain and increase the trust in the implementation of DLS techniques in today's studies. To achieve this goal, the performance of a selection of scheduling experiments from the 1992 original work that introduced factoring, an efficient DLS technique proposed for shared-memory systems, is reproduced and predicted both, via simulative and native experimentation. The scientific challenge is the reproduction of the performance of the past experiments with incomplete information, such as the computing system characteristics and the implementation details. The selected scheduling experiments involve two computational kernels and four loop scheduling techniques. The experiments show that the simulation reproduces the performance achieved on the past computing platform and accurately predicts the performance achieved on the present computing platform. The performance reproduction and prediction confirms that the present implementation of these DLS techniques considered both, in simulation and natively, adheres to their original description. Moreover, the simulative and native experiments follow the expected performance behavior for the considered scheduling scenarios. The results confirm the hypothesis that reproducing experiments of identical scheduling scenarios on past
and modern hardware leads to an entirely different behavior from expected. This work paves the way towards additional simulative and native experimentation using further DLS techniques in the future.

**Keywords.** Dynamic loop scheduling; performance reproduction; performance prediction; simulation; native experimentation; shared-memory; many-core architecture.

1 Introduction

Dynamic loop scheduling (DLS) is an effective scheduling approach employed in computationally-intensive scientific applications for the purpose of optimizing their performance in the presence of load imbalance caused by problem, algorithmic, and systemic characteristics. The DLS techniques dynamically schedule the work contained in the parallel loop iterations among the parallel processing units whenever they become available and request work. Over the years, DLS techniques have successfully been used in scientific applications, such as, N-body simulations, computational fluid dynamics, radar signal processing [1], and computer vision application [2].

One of the well-known and efficient DLS techniques is factoring, introduced by Hummel et al. [3] in 1992. Therein, the performance of the IBM Research Parallel Processor Prototype (hereafter, the RP3) system [4] was compared for the execution of three computational kernels: matrix multiplication, adjoint convolution, and Gauss-Jordan elimination, using four scheduling techniques: straightforward parallelization (or static chunking, STATIC), self-scheduling (SS) [5], guided self-scheduling (GSS), and factoring (FAC) [3]. In the present work, the scheduling behavior of the first two computational kernels using the above four scheduling techniques is reproduced to confirm that the implementations of the DLS techniques both, in simulation and in native codes, adhere to their original goals and specifications [3].

Confirming the adherence of the DLS implementation to their original design goals minimizes the sources of uncertainty in their implementation and helps avoiding unnecessary influences on the performance of scientific applications. For instance, a DLS that has been implemented to intensively use shared memory locks will cause unnecessary scheduling overhead. Therefore, adversely influencing performance. Another example would be that SS in
present implementations performs differently than in the past for the particular implementation of MM considered in the past and in this work, leading to uncertainty whether the present SS implementation adheres to the original one. It was found that SS is properly implemented in the present and that the source of the discrepancy is due to the fact that MM in the past was compute-bound while in the present it is memory-bound. The achieved trust in the implementation of DLS techniques for shared-memory systems has already been transferred to their implementation for distributed-memory systems [7]. Confirming the adherence of the STATIC, SS, GSS, and FAC implementations to their original design goals lays the foundation for confirming the implementation of further DLS techniques that aim to better balance the increase in load balancing with the increase in scheduling overhead, such as, weighted factoring [8], adaptive weighted factoring [9], and adaptive factoring [10].

Reproducibility is a key aspect of the scientific method [11]. The reproduction of scientific experiments contributes to the validation of those experiments and to establish that the conclusions drawn from these experiments are of scientific relevance [12]. In the present work, reproduction [11] is defined as revisiting a certain scientific problem, namely, the performance of DLS techniques [3], without the original artifacts or the possibility to execute the artifacts on the original computing system [4]. Reproduction is employed in this work as a means to attain and increase the trust in native and simulative implementations of DLS.

The scheduling experiments selected from the work of Flynn Hummel et al. [3] were reproduced earlier [13], using simulative as well as native execution with DLS techniques implemented employing a centralized process coordination approach. This work extends the reproduction of the experiments selected from the work of Flynn Hummel et al. [3] by investigating the implementation of the DLS techniques using decentralized process coordination. In the authors best understanding, DLS techniques were implemented originally using decentralized process coordination. For completeness both implementations, centralized and decentralized process coordination, are compared in this work. The simulative experiments were conducted with a simulator developed based on the SimGrid-SimDag (hereafter, SG-SD) interface that employs individual representations of the two HPC platforms considered: IBM RP3 (past) and Intel Knights Landing (present). The reproduction of the selected scheduling experiments is a means for the experimental verification of the implementation of STATIC, SS, GSS, and FAC using SG-SD.
Moreover, the selected scheduling experiments were performed natively on an Intel Knights Landing (hereafter, the KNL) architecture, whose characteristics are captured in a platform file representation required by the simulator. SG-SD is then used to predict the performance of the execution on the KNL. The results of the native and simulative executions were compared and found in close agreement, which increases the confidence in the simulation-based prediction of the performance of DLS experiments.

The present work makes the following contributions: (1) Employs reproduction as a means to experimentally verify the SG-SD implementation of STATIC, SS, GSS, and FAC by comparing the present simulation results with the corresponding results on the RP3 from the work of Flynn Hummel et al. [3]. (2) Repeats the selected scheduling experiments [3] on the KNL 7210 processor to explore whether conclusions of the past experiments hold on a modern computing system. (3) Introduces a SG-SD-based simulator to simulate and predict the behavior of two computational kernels using four loop scheduling techniques [3] that employ the decentralized process coordination approach. Experimentally verified implementations of DLS techniques can be useful for studying the relation between their use at different levels of scheduling [14]. Moreover, the present work enables future studies on the scheduling behavior under various scheduling scenarios and in the presence of variable application and system properties.

The remainder of this work is structured as follows: The background on DLS techniques, the simulation toolkit, as well as an overview of relevant reproducibility studies are reviewed in Section 2. The proposed methodology for performance reproduction and prediction of DLS is described in Section 3. The reproduction of the selected experiments on the RP3 is presented in Section 4. The reproduction of the selected scheduling experiments on the KNL architecture is detailed in Section 5. The performance of the KNL-based experiments predicted with SG-SD is compared against the performance of the native experiments on the KNL and discussed in Section 6. The conclusion and insights into future work are outlined in Section 7.

2 Background and Related Work

This section reviews the dynamic loop scheduling techniques and the SimGrid simulation toolkit. A number of relevant reproducibility studies are also discussed.
**Dynamic loop scheduling.** The loop scheduling techniques considered in this work can be classified into static and dynamic. Using straightforward parallelization (denoted STATIC), the parallel loop iterations are divided into equally-sized chunks. A processor is assigned *exactly one chunk* of iterations equal to the overall number of loop iterations ($N$) divided by the number of available processing elements ($P$). STATIC has a very low scheduling overhead ($h$), bounded above by $P$. Application performance may be degraded due to load imbalance if the execution of the loop iterations is characterized by high variability. Self-scheduling [5] (SS), is a dynamic loop scheduling technique, at the other scheduling extreme, whereby a processing element obtains a chunk consisting of *exactly one loop iteration* whenever it becomes available and requests work. When all loop iterations have been self-scheduled, the processors finish their execution at virtually the same time due to the fine-grain self-balancing of the workload. Scheduling a single loop iteration at a time leads to increased scheduling overhead over STATIC and potentially to an overall completion time greater than the optimal time.

A number of other DLS techniques provide a trade-off between minimizing scheduling overhead and maximizing the load balancing. Two such techniques are guided self-scheduling (GSS) [6] and factoring (FAC) [3]. GSS assigns a chunk of loop iterations to an available and requesting processor that is equal to the number of the remaining unscheduled loop iterations ($R$) divided by the number of the processors $P$. Therefore, chunks are of decreasing sizes, and workload can be balanced among the processors also in the case of uneven processor start times. Even though GSS offers a good compromise between load balancing and scheduling overhead, it assigns a very large chunk to the first available worker. The execution of this chunk can dominate the application performance leading to load imbalance. FAC [3] is designed to balance the execution of loop iterations with variable execution times. It assigns chunks of loop iterations to available and requesting workers in batches vs. single loop iterations at a time, therefore, reducing the scheduling overhead $h$. The number of the loop iterations in a chunk depends on the remaining number of loop iterations $R$ and on the coefficient of variation (c.o.v.) of the loop iterations execution times.

**Loop scheduling in simulation.** SimGrid [15] is a scientific simulation framework for the study of the behavior of large-scale distributed computing systems, such as, the Grid, the Cloud, and peer-to-peer (P2P) systems. It provides ready-to-use models and application programming interfaces (APIs) to simulate various distributed computing systems. SimGrid (hereafter,
SG) provides four different APIs for different simulation purposes. The MetaSimGrid (MSG) and SimDag (SD) provide APIs for the simulation of computational problems expressed as parallel independent tasks or as parallel task graphs, respectively. The SMPI interface provides the functionality for the simulation of programs written using the message passing interface (MPI) and targets developers interested in the simulation and debugging of their parallel MPI codes. The newly introduced S4U interface currently supports most of the functionality of the MSG interface with the purpose of also incorporating the functionality of the SD interface over time. This work considers the SG-SD interface.

Related work. DLS techniques have previously been implemented in the SG-MSG interface with the purpose of studying their scalability [16] and robustness against load imbalance [17]. Moreover, a number of DLS techniques were also implemented in SG-MSG to study their resilience in a heterogeneous computing system [18]. Another closely related study performed simulation-based reproduction (using SG-MSG) to confirm and validate the implementation of several DLS techniques in simulation [19].

Two approaches can be employed to implement process coordination in the DLS techniques natively or in simulation: (1) Centralized process coordination, using a master-worker execution model; and (2) Decentralized process coordination, wherein each “worker thread” calculates and executes a chunk of work whenever it becomes available. A first effort to reproduce a selection of experiments from [3] using simulation considered the DLS techniques implemented using the master-worker execution model [13].

The present work extends and complements previous work [13] by investigating the reproduction of a selection of experiments [3] with the DLS techniques employing a decentralized process coordination approach using only “worker threads” without a “master thread”. In this approach, threads (or processes) are responsible for obtaining work on their own from the central work queue shared via memory, eliminating the master-side contention that characterizes the centralized process coordination model. The goal of this work is the use of performance reproduction and performance prediction as a means of experimental verification of the adherence of the DLS techniques implementation in SG-SD to the original design goals and specifications.
3  Reproduction and Prediction Methodology

In this work, four scheduling techniques: STATIC, SS, GSS, and FAC are implemented in SG-SD. To confirm the implementation of these scheduling techniques, selected scheduling experiments from the original publication are reproduced using simulation. As mentioned earlier in Section 2, the DLS techniques under study can be implemented in one of two approaches: (1) Centralized process coordination; (2) Decentralized process coordination. In this work, the DLS techniques implemented using the decentralized process coordination approach are investigated. In a centralized process coordination approach, the master calculates and assigns chunks of iterations to available and requesting workers. Also, the master can be dedicated or act as a worker as well when there are no requests to serve from workers. The decentralized approach studied in the present work is close to the implementation described in the original work, where each thread calculates and obtains a chunk of work when it becomes available. Atomic operations are used instead of locks to optimize the implementation as proposed in the original publication. The results of simulating and executing the scheduling experiments using centralized (from previous work) and decentralized (from the present work) process coordination approaches are compared in Sections 4 and 5.

The reproduction and prediction approach consists of three steps as illustrated in Figure 1. Step 1 of the reproduction process is described in Section 4. The results of the simulated experiments are compared with the results from the original publication to confirm the present implementation of the DLS techniques in the SG-SD simulator. The results of the original paper were extracted from the figures using web plot digitizer. Comparing the reproduced results with the original results ensures that the DLS techniques are delivering the same performance as in the original publication, and hence the verification of their implementation. The poor implementation of the DLS techniques may lead to load imbalances that should have been avoided using the DLS techniques.

The selected DLS experiments are reproduced on the state-of-the-art many-core processor architecture, the KNL, as shown in Step 2 in Figure 1. The KNL is representative of modern manycore architectures that exhibit a high degree of parallelism, rendering it, therefore, an interesting architecture for

1https://apps.automeris.io/wpd/
the study of DLS. The details of the implementation and the reproduction of the DLS experiments on the KNL are presented in Section 5. This allows to examine whether the conclusions drawn from the DLS experiments described in the original work [3] are influenced by the underlying system. One can also examine whether the advancements in computer systems over three decades alter the conclusions of publications of the past.

The SG-SD simulator is configured (cf. Section 6) to predict the performance of the selected experiments on the KNL architecture instead of the RP3 system denoted by Step 3 in Figure 1. The native execution results from Section 5 are compared with the results of the simulated execution from Section 6 to attain trustworthiness in the SG-SD-based prediction of the performance of the selected DLS experiments. The proposed reproduction methodology in Figure 1 can be used in other scheduling studies to confirm the implementation of scheduling techniques (Step 1) and confirm the correctness of the simulation (Step 2).

![Figure 1: Proposed reproduction and prediction methodology.](image-url)
Selection of the DLS Experiments  The original paper [3] compared the performance of executing three different computational kernels: matrix multiplication, adjoint convolution, and Gauss-Jordan method on the RP3 system using four different scheduling techniques STATIC, SS, GSS, and FAC. Two matrix sizes were used as input for each of the three kernels. Two variations of the adjoint convolution kernel were considered: with increasing task sizes and with decreasing task size. All scheduling experiments in [3] were performed on the RP3\textsuperscript{2} system [4].

Algorithm 1: Parallel matrix multiplication (MM)

\begin{algorithm}
\textbf{Input:} Matrices $A$ and $B$ each of size $n \times n$

\textbf{Output:} Matrix $C$ of size $n \times n$

\textbf{Data:} $A$, $B$, $n$

\textbf{Result:} $C \leftarrow A \times B$

\begin{algorithmic}
\State \textbf{for} $k = 1 : n \times n$ \textbf{do} in parallel
\State $i \leftarrow k/n$
\State $j \leftarrow k - n \times (k - 1)/n$
\State $C[i,j] \leftarrow 0$
\State \textbf{for} $l = 1 : n$ \textbf{do}
\State \quad $C[i,j] \leftarrow C[i,j] + A[i,l] \times B[l,j]$
\State \textbf{end}
\State \textbf{end}
\end{algorithmic}
\end{algorithm}

The matrix multiplication (MM) and adjoint convolution with decreasing task sizes (AC-d) kernels are selected for reproduction and prediction in this work, with matrix sizes of $300 \times 300$ and $75 \times 75$, respectively. The computational kernels are described in Algorithms 1 and 2. Larger matrices are used in the scheduling experiments on the KNL to arrive at an execution cost on the KNL close to that of the experiments on the RP3 system. Using large matrices results in a longer program execution time. Errors in the execution time measurements and in the overhead are small compared to the measurement of the program execution. These timings are negligible, i.e., the time measurement function calls require 16.15 microseconds for a program execution time of 329 seconds. The matrix sizes of $5500 \times 5500$ and $600 \times 600$

\footnotetext{Each processor had its own local memory, configured in a shared address space. Every processor-memory element was connected to other elements using the Omega network [4].}
Algorithm 2: Parallel adjoint convolution (AC-d)

**Input:** Two matrices $A$ and $B$ each of size $n \times n$

**Output:** Matrix $C$ of size $n \times n$, where $C$ the adjoint convolution of $A$ and $B$

**Data:** $A$, $B$, $C$, $n$, $const$

1. for $k = 1 : n \times n$ do in parallel
2. $C[k] \leftarrow 0$
3. for $l = k : n \times n$ do
4. $C[k] \leftarrow C[k] + const \times A[l] \times B[l - k]$
5. end
6. end

are used for the MM and the AC-d kernels on the KNL, respectively. The selected experiments details are summarized in Table 1.

Table 1: Selected scheduling experiments

| Computational kernel                                      | Matrix size | Scheduling method | Number of processors |
|-----------------------------------------------------------|-------------|-------------------|----------------------|
| Matrix multiplication (MM)                                | $300 \times 300$ | STATIC, SS         | 4, 8, 16, 24, 32, 40, 48, 56 |
| Adjoint convolution with decreasing task sizes (AC-d)    | $75 \times 75$   | GSS, FAC           | 32, 40, 48, 56       |

The two kernels represent two different task granularities: equal task sizes and decreasing task sizes. Each iteration of a kernel’s for loop was considered a task to be scheduled.

The open-source simulator and the raw results obtained from simulated and native executions for this work are available online [20]. An Easybuild\(^3\) configuration file is also provided to ensure the creation of an experimental environment that is similar to the one used for this work.

\(^3\)http://easybuild.readthedocs.io
4 Reproduction of Selected Experiments via Simulation

To confirm the implementation of the four scheduling techniques in SG-SD, the selected scheduling experiments on the RP3 system [3] are reproduced and compared with those obtained using SG-SD [15]. Every iteration of a kernel’s outer loop is modeled as a SG-SD sequential computation task. The amount of work contained in each computational task is specified in number of floating point operations (FLOP) in the simulator. For both MM and AC-d, the FLOP count in each iteration is inferred from their pseudocodes. This number is used in the simulator as the amount of work in each sequential computation task. The DLS techniques are implemented using decentralized process coordination. The pseudocode of the SG-SD simulator of the parallel execution of the two kernels with DLS techniques is listed in Algorithm 3.

**Algorithm 3**: SG-SD pseudocode — decentralized process coordination

**Input:** platformFile, numThreads, kType, pSize, method  
**Output:** simulatedTime  
**Data:** schedulingStep, scheduledTasks, chunkSize, hosts, tasks, numTasks, dummyTask, dummyComm, changedTasks

1. numTasks ← pSize × pSize  
2. tasks ← CreateTasks(kType, pSize)  
3. foreach i ∈ numTasks do  
   4. SD_task_watch(tasks[i], SD_DONE)  
4. end  
/* Create a computational task to represent create threads overhead */  
6. dummyTask ← SD_task_create_comp_seq(“createThreads”, thread creation overhead according to numThreads in FLOPs)  
7. SD_task_schedule(dummyTask, hosts[0])
/* Run the simulation until a task is completed */
while !(is_empty(changedTasks=SD_simulate(-1))) do
  for i = 0 : numThreads do
    if (scheduledTasks < numTasks) and is_free(hosts[i]) then
      chunkSize ← calculate_chunk_size(numTasks, numThreads, schedulingStep, method)
      /* Create a scheduling overhead task according to the scheduling method */
      dummyTask ← SD_task_create_comp_seq(“scheduling overhead”, scheduling overhead in FLOPs corresponding to method)
      dummyComm ← SD_task_create_end_end_comm(“assigning chunk”, chunkSize × pSize × 8)
      /* Add dependencies between calculating chunk overhead, assigning overhead and the start of the execution of the chunk of tasks */
      SD_task_schedule(dummyTask, hosts[i])
      Schedule_comm_A_to_B(dummyTask, hosts[0], hosts[i])
      /* Schedule the chunk of tasks */
      for j = 0 : chunkSize do
        SD_task_schedule(tasks[scheduledTasks], hosts[i])
      end
      Increment schedulingStep
    end
  end
end
Print the simulated time
Terminate the program

A SG-SD sequential computation task is created to represent the scheduling overhead of each DLS technique. This task is scheduled on the available thread in each simulated scheduling round. The amount of work performed by each of these scheduling tasks varies and depends on the selected scheduling technique. The values for the amount of work performed by each of these scheduling overhead tasks are obtained empirically, to match the simulation
results to the results in the original publication [3]. Specifically, they are found to be 75, 400, 750, and 750 FLOP for STATIC, SS, GSS, and FAC techniques, respectively. A SG-SD end-to-end communication task is also created in each scheduling round to simulate the time taken to send the assigned chunk of tasks from process 0, to the available process that needs work. It is assumed that, initially, process 0 stores all the data, and other processes transfer one column of the matrix from process 0 for every task they obtain. This data strategy is referred to as pool of tasks and data.

The amounts for computation (FLOP) and communication (Byte) in each loop iteration for the two selected computational kernels are presented in Table 2. Two factors, $g_1$ and $g_2$, are used to capture the unknown effects in the execution of the computational kernels on the RP3 system. These factors cover all software- and hardware-related aspects that may influence program execution on RP3, e.g., memory system and operating system interference. These factors are presented in Table 2 are unitless and are experimentally determined to be 35 and 60, respectively.

To provide the SimGrid simulation engine with the specifications of the simulated system, it requires an XML file as a platform file. Each processor in the RP3 system is represented as a host in the SimGrid platform file used in the reproduction experiments. All hosts (processors) are interconnected by creating a communication link between every host and all others. Additional details about the RP3 system are extracted from the work that introduced the RP3 system [4], such as processor speed (1.562 MFLOP/s), network bandwidth (50 Mbit/s), and latency (2 µs).

All simulations are performed using SG-SD 3.16 on a manycore compute node with an Intel KNL processor (7210) running at 1.3 GHz, using CentOS operating system, version 7.2.1511. The GNU C compiler, version 6.3.0, is used for the compilation of the simulator with `-g -Wall` as compilation flags.

Table 2: Computational kernels parameters for their simulation on the RP3 system.

| Computational kernel | Task size (FLOP)                      | Communication size (Byte) |
|----------------------|--------------------------------------|---------------------------|
| MM                   | $g_1 \times (5 + 2 \times \text{rowLength})$ | $\text{chunkSize} \times \text{rowLength}$ |
| AC-d                 | $g_2 \times 3 \times (\text{matrixSize} - \text{iterationID})$ | $\text{chunkSize} \times \text{rowLength}$ |
Figure 2: Simulation results for the selected DLS experiments on the RP3 system using a decentralized process coordination (SG-SD-D) obtained with SG-SD (red bars) compared with the simulation results for the selected DLS experiments on the RP3 system using a centralized process coordination (SG-SD-C) (blue bars) and the original publication results (black bars). Parallel cost = parallel program execution time \times number of threads.
Results of Reproduction  The selection of parallel cost as a performance metric (over the parallel execution time) is due to the fact that the parallel cost was used in the original publication [3] that this work compares against. The parallel cost reflects the sum of the time that each processing element spends solving the problem [21]. The simulative performance for executing MM and AC-d using a decentralized coordination approach with SG-SD (SG-SD-D) compared against the original native performance results [3] is illustrated in Figure 2. These results show that the simulation performance is close to the native performance in the original publication. The simulative performance of the same experiments using a centralized process coordination [13] (SG-SD-C) is also compared against the original native performance results [3] in Figure 2. The percent error (%E) between the simulative execution time in this work (T_{sim}) and the original native execution time (T_{nat}) [3] is calculated as: \[ %E = \left(1 - \frac{T_{sim}}{T_{nat}}\right) \times 100. \]

A positive percent error %E indicates that the simulator underestimates the original execution time, while a negative %E signifies overestimation. The minimum absolute %E between SG-SD-D and the native execution is 0.073%, for GSS — AC-d and 56 threads, as can be observed from Figure 2(g). The maximum absolute %E is 45.89% in the case of SS — MM and 4 threads, as can be observed from Figure 2(b). The average of the absolute %E is 10.89% in all the scheduling experiments on the RP3 system and the SG-SD simulation results shown in the present work. For the results centralized process coordination [13], the minimum and the maximum absolute %E are 0.49%, and 30.94%, respectively, in the case of GSS — AC-d and 24 threads (see Figure 2(g)) and SS — AC-d and 56 threads (see Figure 2(f)). The average of the absolute %E is 7.44% between the simulative results [13] (SG-SD-C) and the native execution results [3]. The simulative results follow a similar trend to the original native experiments, which is of high relevance for the comparison of different scheduling techniques. These results confirm that the implementation of the considered DLS techniques in SG-SD adheres to their implementation used in the original publication [3].

5  Reproduction of Selected Experiments via Native Execution
For the purpose of reproducing the selected experiments [3] via native execution in the present work, the two computational kernels were implemented in C. Their parallelization considers the scheduling techniques STATIC, SS, GSS, and FAC using Pthreads [22]. The Pthreads threading library is chosen due to its lightweight threading and its efficiency in communication and data exchange on shared memory computing systems.

A decentralized process coordination is used in parallelizing the computational kernels with the DLS techniques. The main thread, thread 0, creates a number of threads equal to the number of cores in the current experiment minus one (the main thread). All threads, including the main thread, execute the code described in Algorithm 4. Each thread obtains work using the obtain work function described in Algorithm 5. The program holds two global variables that represent the current state of the program: schedulingStep and currentIndex. The currentIndex represents the loop index of the outer loop that is parallelized of the computational kernels and indicates the program progress. The obtain work function updates these two variables after each work assignment to advance the program state. Updates to these global variables (Lines 1 and 3 in Algorithm 5) are performed using atomic operations to avoid data races between parallel threads. The size of the allocated chunk of work is calculated by the selected loop scheduling technique. All threads are pinned on the cores of the experiments platform using the scatter strategy, to ensure better and more stable performance among execution runs.

The parallel cost is reported for each experiment. This cost is calculated as the product of the program’s parallel execution time and the number of threads. A script to run the experiments and calculate the confidence interval is used to execute each experiment for a minimum number of 20 times and maximum of 100. For all the experiments, the script stops after 20 times yielding a confidence interval of less than 5% and a confidence level of 95%.

**Reproduction Results**  The performance results in terms of parallel cost of the native execution of the DLS techniques implemented using decentralized process coordination are compared to the performance results of the native execution using the centralized approach [13] in Figure 3. As can be observed from Figure 3, the parallel cost of the centralized process coordination increases as the number of threads increases. This can be attributed to the effect of multiple threads competing to lock and unlock the work queue.
Algorithm 4: Decentralized DLS — thread execution

Input: threadID
Output: void
Global data: method, schedulingStep, currentIndex
Local data: start, chunkSize

1 while True do
2     if obtain_work(start, chunkSize) then
3         execute_kernel(start, chunkSize)
4     else
5         break
6     end
7 end
8 /* Exit thread */
9 return NULL

Algorithm 5: Decentralized DLS — obtain work

Input: method, schedulingStep, currentIndex
Output: start, chunkSize
Global data: method, schedulingStep, currentIndex, numTasks
Local data: myStep

1 myStep ← fetch_and_add(schedulingStep, 1)
2 chunkSize ← calculate_chunk(numThreads, numTasks, myStep)
3 start ← fetch_and_add(currentIndex, chunkSize)
4 if start < numTasks then
5     if start + chunkSize >= numTasks then
6         chunkSize ← numTasks - start
7         return True
8 else
9     return False
10 end

and the master serving work requests and update the same data structure concurrently. In the present decentralized implementation, threads obtain work on their own from a pool of tasks (accessed via a shared loop index) whenever they become available. The updates of the shared variables between threads are performed using atomic operations. Therefore, the decen-
Centralized DLS implementation does not exhibit the same parallel cost increase as the centralized implementation [13] as the number of threads increases. The performance behavior of the four loop scheduling techniques is compared in the execution of the selected experiments on the KNL processor, illustrated in Figure 3 and the execution on the RP3 system, illustrated in Figure 2. The performance trend of the scheduling techniques in Figure 3 is comparable to that in Figure 2 for the AC-d kernel, as can be observed by comparing sub-figures (e,f,g,h) in both Figure 2 and Figure 3, yet the absolute performance is different. However, for the MM kernel, the performance trend and absolute values of the scheduling techniques in the past and in the present differs significantly. The original results, in Figure 2(b) and (d), suggest that SS and FAC yield almost similar performance. Examining the results in Figure 3(b) and (d), one can notice a significantly different performance from the one in Figure 2(b) for the same computational kernel. In the present results, STATIC, GSS, and FAC outperform SS, which exhibits the poorest performance for the MM kernel. The poor performance of SS is due to its large scheduling overhead and the fine granularity of the MM loop iteration for the matrix size under study. The achieved trust in the implementation of DLS techniques for shared-memory systems has already been transferred to their implementation for distributed-memory systems [7]. These experiments are performed on a single KNL processor running CentOS operating system version 3.10.0-327.el7.x86_64, with a single 64-core Intel Xeon Phi standalone processor, version 7210. The computational kernels codes are compiled using GNU C compiler version 6.3.0, with the -O3 -mavx512f -mavx512cd -mavx512er -mavx512pf optimization flags. The KNL processor is booted in the memory mode [23]. As the computational kernels under study are not memory intensive and the main focus of this work is on studying the effect of scheduling on the execution time, the MCDRAM is, however, not used. All memory allocations being performed on the regular DDR4 memory. To make the results in this work reproducible, the GNU C compiler is used instead of the Intel C compiler. Certain compilation lags (see above) are used to optimize the generated code for the KNL processor and obtain the best possible performance using the GNU C compiler.
Figure 3: Parallel cost of the native execution of selected DLS experiments on the KNL processor with DLS implemented using a decentralized process coordination (dark blue bars) compared with the native execution results with DLS implemented using a centralized (master-worker) process coordination (green bars). Parallel cost = parallel program execution time × number of threads.
6 Prediction of DLS Performance via Simulation

The SG-SD simulator from Section 4 is used to predict the performance of the DLS experiments of interest on the KNL processor using simulation. A close agreement between the performance prediction using simulation and the native execution represents an experimental validation of the simulation. The experimental validation of the simulation is essential to attain trustworthiness in the prediction results of the simulation in future experiments. Accurate parameters that describe the execution on the KNL processor are required as input to the simulator. In this work, three such parameters have been identified: (1) Pthreads library: Creation of threads; (2) Scheduling overhead; and (3) Task execution time.

Timers are inserted in the source code of the computational kernels around the functions that represent these parameters. For instance, timers are inserted before and after Line 2 in Algorithm 4 to measure the scheduling overhead and before and after Line 3 in Algorithm 4 to measure the task execution time. The measurement procedure described in Section 5 is used to ensure the accuracy of the time measurements. These time overheads (in the microsecond range), are multiplied by the nominal computing speed of a KNL core of 41,600 MFLOP/s to obtain the computational effort as FLOP. The scheduling overheads and tasks execution times are read during simulation from a file. This way, the simulator can account for these overheads and make more accurate predictions of the execution time. As all threads on KNL share the available memory, there is no over the network inter-thread communication. Therefore, the communication size is set to 0 Byte in the SG-SD simulator for both computational kernels.
Figure 4: Parallel cost of the execution of selected DLS experiments obtained with SG-SD (red bars) compared with the cost of the native execution results on the KNL processor (dark blue bars). Parallel cost = parallel program execution time × number of threads.
The theoretical speed of a single core of the KNL is calculated using information from the publication that introduced it \[23\]. The single core speed of the KNL is found to be 41.6 GFLOP/s. Even though the SG-SD simulator, in this experiment, simulates a shared memory system and the network is unused, the parameters for describing the network are still required in the platform file. The values that describe the processor speed, network bandwidth, and network latency of the KNL system used in these experiments are 41,600 MFLOP/s, 100 Gbit/s, and 100 ns, respectively. SimGrid is a multithreaded simulator. To reduce the simulation time of SimGrid-based experiments, it is executed in parallel on the KNL hyperthreaded processor, with 256 hardware threads.

**Performance Prediction Results** The results of the execution of the selected DLS experiments on the KNL are compared to the simulation-based prediction results obtained with SG-SD-D in Figure 4. The results show that the simulated execution behavior is in agreement with the native execution for the four different DLS techniques in executing the two computational kernels under test.

The percent error \(E\) between the results of the simulation of KNL execution and the results of KNL execution is calculated as described in Section 4. The minimum absolute \(E\) is 0.00948\%, for FAC — MM with 4 threads as can be observed from Figure 4(d). The maximum absolute \(E\) is 21.42\%, for STATIC — MM with 40 threads as can be observed from Figure 4(a). The average of the absolute \(E\) is 1.94\% between all the scheduling experiments on the KNL and their corresponding SG-SD simulation presented in this work. The average percent error values correspond to acceptable differences. More importantly, the performance trends of the studied DLS techniques are similar between the native and simulative executions. Therefore, it can be stated that the simulator predicts the performance of the two computational kernels with the four implemented scheduling techniques on the present computing system.

7 Conclusion and Future Work

In this work, the reproduction of the behavior of two computational kernels \[3\] has been used to confirm the adherence of the present implementation of four scheduling techniques to the original specification \[3\]. The
achieved trust in the implementation of DLS techniques for shared-memory systems has also been transferred to their implementation for distributed-memory systems \[7\]. Moreover, the reproduction, in the present, of previous scheduling experiments on modern hardware, is used to evaluate the hypothesis that the results and conclusions from past experiments are influenced by the modern software stack and hardware systems used in the present work. In contrast to the earlier results of Flynn Hummel et al. \[3\] which indicate that both FAC and SS perform comparably, this work shows that it is significantly inefficient to use the SS technique for the particular form of the MM kernel considered herein. This behavior can be attributed to the massive increase in the hardware computing speed since 1992 \[3\], and to the fact that the MM loop iterations that were considered of large granularity in earlier work, are now shown to be of small granularity. Consequently, the overhead of allocating work in SS is larger than the time to execute an MM loop iteration. Hence, the performance of the SS technique is presently dominated by the scheduling overhead. The main contribution of this work is a confirmation of the hypothesis that reproducing experiments of identical scheduling scenarios on past and modern hardware may lead to an entirely different behavior from what is expected.

A comprehensive study of the performance behavior of dynamic loop scheduling techniques for various applications and on several architectures is envisioned as part of future work. This work lays the foundation and motivates the reproduction and experimental verification of other DLS techniques and their implementations in other simulators. The study of the performance of scientific applications with various DLS techniques under perturbations and failures in the computing system is envisioned as future work.

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