Analysis and Design of Series-LC-Switch Capacitor Multistage High Gain DC-DC Boost Converter for Electric Vehicle Applications

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Abstract: Research into modern transportation systems is currently in progress in order to fully replace the traditional inter-combustible engine with a noiseless, fast, energy-efficient, and environmentally friendly electric vehicle. Electric vehicles depend on an electric motor and require highly efficient converter drive circuits. Among these converters, DC-DC boost converters play a major role in charging not only the battery banks but also in providing the DC-link excitation voltage in transformerless applications. However, the development of these converters, which have higher voltage and current gain with minimum components, minimum voltage, and current stress, is quite challenging. Therefore, this research work aims to address these issues and also to improve overall system performance. These aims are achieved by developing a series LC-based single-stage boost converter, and extending its gain through a multi-stage boost converter using switch capacitor phenomena. This article also presents a complete operating model in continuous conduction mode. The proposed converter is tested under various testing conditions, such as output loading, input voltage levels, and duty cycle ratio for a 50 W resistive load. The results are compared with existing models. The proposed converter is stated to have achieved the highest efficiency, i.e., 96.5%, along with extendable voltage gain with reduced voltage and current stresses, which is a major contribution to this research field.

Keywords: DC-DC converters; electric vehicle; energy saving; extendable high gain; switch capacitors converter; switch voltage stress; switch current stress

1. Introduction

The report “Riding the Energy Transition: Oil Beyond 2040”, regarding energy transition for the oil market, was published by the International Monetary Fund (IMF) in May 2017, and showed their concern for adopting electric vehicles in the upcoming future. The discussion concluded that the future of transportation will see around 290 million people (93% of the population) travel via electric vehicles (EV) in the USA [1]. However, EV performance as compared to the conventional engine is a real concern. The ideal development of the electric vehicle was compared with the outperformance of combustible cars, which would create a Kodak moment for combustion-based automakers who fail to transition to EVs.

The adoption of EV as an emerging technology solely depends on how fast EV can outperform the inter-combustible engine (ICE). Travel does not always require a top speed
and maximum torque bearing capacity, but the cost of mileage per fuel is a major concern. Due to this reason, many automakers, such as BMW, Ford, Chinese OEM, Honda, Renault-Nissan, Tesla, Volvo, and many other EV-developing companies, have set out plans for 2025 and 20,230 to manufacture millions of environment friendly EVs [2]. The development of EV technology falls into the following three categories: battery packs, electromechanical systems, and power electronic units. The power electronics converters inside the EVs mainly consist of DC-DC or AC converters, and, as such, there is a significant need for a high gain DC-DC converter. In the inverter section, due to reliability issues, most of the existing EVs utilize the two-level voltage source inverter (VSI), with or without using DC boost converter stages [3]. Often, a directly coupled battery to an inverter-based application is not sufficient to reach the required voltage level, and often requires several battery packs in series to provide a sufficient DC link voltage level [4]. One way to push the VSI limit is by developing a strong DC link voltage by connecting several battery packs in series or by using a high gain DC-DC converter. However, it takes several hours to charge several battery banks and, additionally, maintaining several battery packs is very difficult. This type of configuration was only experienced by Tesla (75–100 kWh) [5].

Therefore, the utilization of a high gain DC-DC converter is a suitable option. Moreover, DC-DC boost converters also have applications in E-scooters and power train EVs, as reported in [4,6,7]. Since future transportation will be mostly made by EVs, the major advantage of using these EVs in the future is that they will drastically reduce our dependency on fossil fuels. Additionally, carbon emitted from combustible engines, and the greenhouse effect, will be reduced. These small advancements in technology will help to create a sustainable environment that will benefit both the human and animal races.

A vast majority of researchers are devising methods to energize EVs using dynamic wireless power transfer EV charging (DWPT-EV). The development of high gain boost converters plays a vital role in both battery charging and EV driving. As the EV moves over one charging pad to another, several problems occur between the primary and secondary charging pads. Some of these issues include power fluctuation, misalignment factors, and voltage stabilization requirements for battery charging, which are mentioned in-depth in [8]. These DC-DC high gain boost converters with a closed-loop control strategy can easily reduce battery charging and power fluctuation issues. The development of these DC converters, along with bidirectional DC-DC converters, can make DWPT-EV serve as a vehicle to grid (V2G) application, as discussed in [9–12].

There are also several issues associated with traditional DC-DC boost converters. Such converters use high power-rating switches to overcome voltage stress issues. This is because the output voltage and the voltage across the switches are equal. Additionally, the high on-state resistance $R_{DS_{on}}$ and the duty cycle approaching unity causes high conduction losses, which limit the output voltage gain of a converter [13,14]. The equivalent series resistance (ESR) of the inductor and other elements is yet another limitation to boosting voltage gain [15]. An alternative solution is to adjust the turn ratio of the inductors in interleaved converters, such as push-pull, flyback, full-bridge, and half-bridge circuits. Making their special arrangements, such as in isolated multipport converters, also helps in providing bidirectional power flow and reduced fault current chances, as well as a high gain voltage, as in [16]. However, there are drawbacks, such as leakage inductance, the system’s increased weight, high costs, and high voltage spikes [17]. Additional problems include poor voltage regulation and lack of flexible switching [18]. To overcome these issues requires special arrangements, such as the use of half-bridge flyback converters, a passive snubber, active clamping methods, and the switched capacitor method with coupled inductors, as suggested in [19].

Non-isolated DC-DC converters, on the other hand, eliminate many of the above-mentioned issues. There are many ways to enhance voltage gain for these converters by using capacitors, inductors, and diodes, as discussed in [20,21]. In the following literature review, either of these elements is switched alone, or sometimes both have been switched. In [20], multiple capacitors with inductors were connected in the boost stage.
This worked on the principle of single inductor stored cell-based SC (SIESC-SC), with only two operating modes. However, this converter, as compared to other converters, was not suitable for lighter loads, and its efficiency was less than 90% [22]. Behdad Faridpak in [14] and Javed Ahmad et al. in [23] developed a high gain DC-DC converter using a switch inductor/capacitor mode and operated them as voltage multiplier cells (VMC). However, the developed model used multiple inductors, capacitors, and switches to form VMCs in a single-stage boost converter and still requires additional elements in boost stages. This not only increases the cost, but it also means that the offered stress is still higher than the proposed model. A similar effort with a reduced number of components, but using coupled inductors, was presented in [19]. However, calculating turn ratios is yet another job which must be performed. The obtained output voltage gain was similar to that obtained from the active network converter (SC-ANC) [24]. However, the desired number of reactive and active switches was very high. Similarly, Z-source and quasi-Z-source (QZS) in [25] serves the same purpose, although it is limited by the duty cycle \( D \leq 0.5 \), and the voltage gain is also slightly less than presented in [23]. The active switch along with the switch inductor and capacitor proposed in [26] and [27] offered a high gain with an extendable option, but nonetheless, it required multiple inductors and switches to operate.

It is desirable to have a maximum converter gain at around 50% of duty cycle, a fast converter response, minimum number of converter boost side elements, a minimum voltage and current stress, maximum efficiency, minimum losses, fewest operating modes, zero current switching (ZCS), and ease of control. These types of DC-DC boost converters often have limited duty cycle variations. Some converters are limited to 30%, while the rest can be adjusted between 50 and 90%.

In this paper, an easily-adjustable voltage gain non-isolated DC-DC boost converter is proposed using an LC series single stage with switch capacitors (SC). The proposed converter is capable of handling all the stated problems in [14,19,26]. This converter has only one auxiliary switch connected in series to the capacitor and inductor. The proposed converter operates using the minimum number of elements needed to produce a very high voltage gain DC-DC converter. The normalized voltage stress concerning output across the auxiliary switch linearly rises as the duty cycle approached unity, instead of rising or staying constant, such as in all existing non-isolated boost converters. The operating principle and steady-state analysis at multiple varying loads is presented in detail in the following sections. These facts are verified by using both simulation and experimental setup analysis.

The paper is organized as follows: Section 2 presents the modelling and operation of the proposed converter, Section 3 presents the analysis of the proposed converter, and Section 4 presents the results along with a discussion. Section 5 concludes the discussion.

**Contribution**

- The overall number of inductors, capacitors, and switches have been largely reduced. Now, only one inductor, capacitor, and switch are required for use in the single-stage boost converter. This reduces the overall size and cost of the system.
- The multiple-stage boost converters are easily extendable and gain can be easily adjusted according to requirements. The PWM signal is used to control only one switch, which controls the single-stage overall gain.
- The proposed design aims to reduce both device voltage and current stress in order to reduce device size. In this way, device power capacity is utilized to its maximum.
- The proposed DC-DC converter serves as a good option for use in both EV driving and battery charging systems.

**2. Modelling and Operation of the Proposed Converter**

Figure 1 shows the basic structure of an active network derived from the concept of capacitor \( (C_A) \) and connected inductor \( (L_1) \). It is switched by using an auxiliary switch. When the switch \( (S_1) \) is ON, the inductor is charged through the source, and when the
switch turns OFF, the voltage across the switch \((V_{SW})\) becomes twice the input. Both \(C_A\) and \(L_1\) share the same amount of voltage from the input source.

![Schematic diagram](image)

**Figure 1.** Boosting side the proposed converter using LC network.

Multiple capacitors and diodes on the output of the auxiliary switch form the switched-capacitor three-stage boost converter, with a series or parallel combination of capacitors as shown in Figure 2. The diodes \(D_1, D_2, D_3, D_4, D_5\), and capacitors \(C_1, C_2, C_3, C_4, C_5,\) and \(C_6\), form the complete unit of the three-stage switched capacitor boost converter. Figure 3 shows the typical waveforms obtained during continuous conduction mode (CCM). In CCM operation, the current through the inductor never falls to zero. The operating modes of the proposed converter in the steady-state are presented in detail as follows.

![Schematic diagram](image)

**Figure 2.** Three-stage DC-DC boost converter.

### 2.1. CCM Operation

There are only two further operating modes in the CCM condition. These are mode 1, when the auxiliary switch \((S_1)\) is turned ON, and mode 2, when the switch \((S_2)\) turns OFF. The timing diagram for the two-stage boost converter is as in Figure 3. We will be using the timing diagram to understand the operation of this converter circuit by dividing it into intervals.
2.2. Mode 1 \( (t_0, t_1) \)

During this time interval, a positive signal is applied at the gate of \( S_1 \) and it turns ON. The capacitor \( (C_A) \), and inductor \( (L_1) \), start to store the energy. The equivalent circuit is shown in Figure 4a. Since all the components are assumed as an ideal, their internal parasitic resistances are, therefore, ignored for the sake of simplicity. Initially, at this stage, it is also assumed that the circuit initial conditions are set to zero. Thus, the voltage induced by the inductor and the voltage stored by the capacitor is given by Equation (1). It can be seen that the DC source, \( C_A \), and \( L_1 \) are parallel to each other. The inductor charging current in this mode is given by Equation (2).

\[
V_{in} = V_{C_A} = V_{L_1} \quad (1)
\]
\[
i_{L_1} = i_{in} - i_{C_A} \quad (2)
\]

2.3. Mode 2 \( (t_1, t_2) \)

During this time interval, the configuration as shown in Figure 4b, the switch turns off. The capacitor \( (C_A) \) maintains its constant voltage level, and the inductor discharges its energy. The voltage across the switch \( V_{SW} \) can be easily evaluated by applying KVL in this loop. Therefore, the loop equation is given by Equation (3). From Equation (1) as a result of the initial condition, the voltage across the switch is given by Equation (4).

\[
V_{C_A} + V_{L_1} = V_{SW} \quad (3)
\]
\[
V_{SW} = 2V_{in} \quad (4)
\]

During the inductor discharging state i.e., within the same interval, the current will flow through the diode \( (D_1) \) and make it forward-biased, while the diode \( (D_2) \) becomes reverse-biased. This capacitor \( (C_2) \) becomes parallel to the switch and attains the voltage level using KVL is given by Equation (5). The equivalent circuit is shown in
Figure 4c. Thus, the connection formed is a series, and its current in this mode is given by Equation (6).

\[ V_{C2} = V_{SW} = 2V_{in} = V_{L1} + V_{C_A} \]  \hspace{1cm} (5)

\[ i_{C2} = C_2 \frac{dV_{C2}}{dt} = i_{L1} \]  \hspace{1cm} (6)

![Figure 4c](image)

**Figure 4.** Charging and discharging of LC network in (a) Mode 1, (b) Mode 2 operation, (c) Output capacitors charging and (d) Output capacitors charging.

2.4. **Mode 1** \((t_2, t_3)\)

During this interval, the converter again enters mode 1, when the \((S_1)\) turns ON. However, this time the inductor and capacitors hold the previous states and become charged again as well, while \(C_2\) maintain its charge. At this position, the voltage across the switch sets to zero, and the diode \(D_1\) becomes reverse-biased. At this stage, the capacitor \(C_2\) that was previously charged to the switch voltage level will now start to discharge through diode \((D_2)\) to charge capacitor \((C_1)\) at the same potential level. Using KVL, the steady-state voltage across \(C_1\) is given by Equation (7), and the equivalent circuit is shown in Figure 4d.

\[ V_{C2} = V_{C1} = 2V_{in} \]  \hspace{1cm} (7)

Each capacitor in this three-stage boost converter follows the same charging principle, and shares the equivalent switch voltage. In each operating mode, if \(C_2, C_4, C_6\ldots\) are charging then \(C_1, C_3, C_5\ldots\) will be discharging to charge the other side, and vice versa.

2.5. **Converter Gain**

For the sake of simplicity, it is assumed that the output load is connected across \(C_2\). The voltage across the inductor is given by Equation (8). In CCM the inductor current is evaluated by considering both modes, i.e., one complete cycle. During the ON state i.e. mode 1, the inductor current, given that all initial conditions are zero and using the inductor voltage from Equation (1) in mode 1, is given by Equation (9), respectively. Similarly, during
mode 2 which is the OFF stage, the inductor current is computed by Equation (10). In this state \( V_L = -(V_{in} - V_o) \). If the converter is operating in a steady-state condition, the average current through the inductor will remain the same in both on and off conditions. Therefore, from Equations (9) and (10) we can determine the gain of the converter when the load is connected at the first stage i.e., across \( C_2 \) as in Equation (12).

\[
V_{L1} = \frac{L_1 di}{dt}
\]  

\[
I_{on} = \int_{0}^{T_{on}} V_L dt = \frac{V_{in}DT}{L_1}
\]

\[
I_{off} = \int_{T_{on}}^{T} V_L dt = -(V_{in} - V_o)(1 - DT)
\]

\[
I_{on} + I_{off} = \frac{V_{in}DT}{L_1} - \frac{(V_{in} - V_o)(1 - D)T}{L_1} = 0
\]

\[
G_{CCMC2} = \frac{V_{oC2}}{V_{in}} = \frac{1}{1 - D}
\]

If the load is connected to \( C_4 \), then the gain of the converter at the second stage is given by Equation (13). The equivalent circuit for this type of configuration is shown in Figure 5. For the \( j^{th} \) stage of the boost converter, the converter gain is given by Equation (12), and the output voltage \( (V_o) \) for the extendable converter is given by Equation (15).

\[
G_{CCMC2} = \frac{V_{oC4}}{V_{in}} = \frac{2}{1 - D}
\]

\[
G_{stage} = \frac{V_o}{V_{in}} = \frac{j}{1 - D} \text{ where, } j \text{ is any stage from 1, 2, 3, \ldots n}
\]

\[
V_o = V_{C2} + V_{C4} + V_{C6} + \ldots + V_{C_{j^{th} stage}}
\]

![Figure 5. Equivalent circuit in mode 2 when the load is connected to C4.](image)

According to KCL, the average input current and the average inductor currents for this converter are given by Equations (16) and (17) respectively. Based on the input to output power balance. We can write inductor current from Equation (17) in terms of gain for any \( (j) \) stage and the input to output current gain is mentioned by Equation (19).

\[
I_{in} = I_L - I_o
\]

\[
I_L = I_{in} + I_o
\]

\[
I_L = I_o \left( 1 + G_{stage} \right)
\]
The proposed converter works on the principle of zero switch current (ZSC). If the converter fails to follow the current, the diodes $D_1, D_2, D_3, D_4,$ and $D_5$ will undergo the reverse recovery problem during the OFF condition.

2.6. Voltage Stress

The switches in the proposed converter undergo stress when they are in the off state. For the converter shown in Figure 2, the switch voltage stress is three lower than the output voltage. The net conclusion is that in this proposed converter, the switch stress across MOSFET, diodes and, capacitor will be $j^{-1}V_o$. This is a major contribution of this research, as the element voltage stress within this converter will not be affected by converter gain extension. Additionally, as in Equation (20), it is the contribution of this research that the switch stress from sources other than conventional converters is significantly reduced by increasing the duty cycle ratio.

\[ V_{C_1}, V_{C_2}, \ldots, V_{C_j} = V_{D_1}, V_{D_2}, \ldots, V_{D_n} = V_{SW} = \frac{V_o}{j} = \frac{2}{j}V_o(1-D) \]  

The normalized voltage stress across the power switch \( \left( \frac{V_{SW, stress}}{V_{in}} \right) \) or \( \left( \frac{V_{SW, stress}}{V_o} \right) \) in terms of CCM gain and that of the diodes \( \left( \frac{V_{D_{stress, (1-n)}}}{V_{in}} \right) \) is given by Equation (21).

\[ \frac{V_{SW, stress}}{V_{in}} = \frac{V_{D_{stress, (1-n)}}}{V_{in}} = \frac{1}{1-D} \quad \text{or} \quad \frac{V_{SW, stress}}{V_o} = \frac{2}{j}(1-D) \]  

2.7. Current Stress

The normalized inductor current stress \( \left( \frac{I_L}{I_{in}} \right) \) can be obtained by modifying Equations (16) and (18) to obtain Equation (22).

\[ \frac{I_L}{I_{in}} = \frac{G_{stage} + 1}{G_{stage}} \]  

3. Analysis of the Proposed Converter

In this section, we have analyzed our proposed converter in terms of current and voltage gain, and have compared the results with the existing boost as shown in Figures 6–12. The proposed converter is also analyzed by relating the impacts of extending boosting stages and output voltage as a function of duty cycle variation. This section will also relate voltage and current stress levels by comparing the proposed converter with existing models. The steady-state analysis and loss analysis model for the proposed converter is also presented in its sub-section. At the end of this section, a complete design method based on the required inductor and capacitor selection is presented in detail.
Figure 6. DC–DC five stage boost converter.

Figure 7. Voltage gain of the proposed converter at various stages.

Figure 8. Voltage gain comparison for the varying duty cycle.
Figure 9. Current gain as a function of duty cycle for the proposed converter.

Figure 10. Inductor to output current as a function of duty cycle.

Figure 11. Inductor Normalized current gain as a function of voltage gain.
PEER (SL-DS-DC) [27] and switch inductor switch capacitor (SL-SC) [14] in Figure 8 have a
function that is in the converter, when increasing the duty cycle of the converter, its gain linearly increases. As the D approaches unity, the system gain suddenly begins to rise in a nonlinear way. The proposed converter is also compared with the existing voltage gain models as in Figure 8. The switched inductor double switch DC converter (SL-DS-DC) [27] and switch inductor switch capacitor (SL-SC) [14] in Figure 8 have a good range of voltage gain but, nonetheless, are limited by voltage gain adjustment i.e., \(D = \leq 0.4\). Additionally, these converters do not offer a high degree of freedom to adjust a smooth output voltage. Their system also becomes unstable/discontinued above this limit. However, switch capacitor active switch LC network (SC-AS-LC) [26], coupled inductor switch capacitor (CL-SC) [19], switch capacitor active network converter (SC-ANC) [24], and the proposed converter not only provide high voltage gains, but are also controllable for the entire range of varying \(D \leq 0.9\). However, these converters are not preferred due to the high current stress level.

According to the input-output power balance, the current gain of the proposed converter significantly decreases as the duty cycle ratio is increased, as in Figure 9. This also justifies that, as the number of stages increases, the current gain for the same connected load will decrease, while the output voltage will increase. Hence, the results obtained from Equation (19) are justifiable, and the voltage gain will rise significantly. This causes a considerably higher inductor current to pass through it, which is why the inductor current to the output current ratio for each stage will be raised, as in Figure 10. Therefore, the proposed converter requires a high current inductor and MOSFET to support such a value of inrush current. However, if the input voltage level is enhanced for the same output side load, the requirement of inductor current will gradually decrease. Based on the inductor to output current gain analysis as shown in Figure 10, to support a large number of stages an inductor current support and input voltage rating must be specified first.

The number of the boost stage \(j\) depends on the amount of gain demanded, as in Equations (14) and (19). The second factor is the selection of LC and switch parameters, as demonstrated in the next sections. The number of boost stages for the same input voltage can be theoretically extended up to the \(jth\) level for higher voltage gain and, for the fixed duty cycle, as shown in Figure 10. However, as demonstrated practically in the next section, the gain starts to saturate for each \(jth\) stage as the D approaches unity. This is mainly because at a higher value of D, the input switch side current becomes high, which causes conduction losses and, secondly, at each higher stage of \(j\) the inductor current becomes

![Figure 12. Normalized diode voltage stress as a function of voltage gain.](image-url)
very high which causes significant inductor power loss. Therefore, the best way for the proposed design to overcome this issue is to raise the level of input voltage level to extend the gain stages.

The inductor current to the output current gain for the five stages of the proposed converter is also compared with the normalized inductor current gain of the existing topologies [14,19,24,26,27] in Figure 11. It can be seen that the proposed converter inductor current gain is very high among all the other types of converters. This is mainly because when the switch is opened, the capacitor, together with the input source currents, becomes higher in magnitude in order to charge the capacitors in the boost stage. This is shown by Equation (22). Its higher current is the main thrust to support a large number of finite multiple boost stage capacitor charges. The inductor current gain for the SL-SC and SL-DS-DC converter is the same, and also offers limited gain. However, the SL-SC type converter is among the lowest to offer inductor current gain and, thus, offers the limited extending option. This comparison also suggests that the proposed converter can step up a very low voltage (i.e., $V_{in} = 1$ V) to around several times higher than its input voltage. In this regard, the proposed converter requires a high current rating inductor to handle this gain. The comparison analysis also reveals that the proposed converter is also well suited for high power applications, especially in DWPT battery charging systems.

Figure 12 relates the normalized voltage stress (NVS) across the diodes for the presented converter under varying voltage gain ($G_v$) and is compared with the existing models as presented in the literature section. The NVS gain to the voltage gain for diodes in SC-ANC, SC-AS-LC, and SL-DS-DC are almost equal, while $\frac{NVS}{G_v} \approx 1$. The diode voltage stress of the existing models, when compared to the proposed design, is still higher. On the other hand, the proposed converter model and CL-SC converter diode voltage stress is the same, and is, in fact, quite low at almost 1 : 8 times that of SC-ANC, SC-AS-LC, and SL-DS-DC. The proposed designed converter $\frac{NVS}{G_v}$ is almost 1/75 part of the NVS level of the existing models i.e., SC-ANC, SC-AS-LC, and SL-DS-DC, which is the major contribution of the proposed design.

Similarly, Figure 13 relates the normalized switch voltage stress with the voltage gain of the converters. Here, for most of the schemes, the stress level for the switch is different as compared to diodes. The switch voltage stress ($NVS/G_v$) for the proposed and CL-SC converter is the same i.e., (1:5). The SC-ANC and SL-SC, on the other hands, are the same but higher than our proposed converter i.e., (7:30). However, among all of these, SL-DS-DC appears to undergo the highest $NVS/G_v$ stress ratio i.e., (7:15). It is to be noted that all the results obtained and compared are valid for CCM, and are justifiable for mathematical forms obtained from Equations (19)–(22).

![Figure 13. Normalized switch voltage stress as a function of voltage gain.](image-url)
The comparison of the proposed design in terms of minimum component requirement with common gain, switch voltage and current stress, and maximum achieved efficiency is presented in the next section.

3.2. Steady-State Analysis

By fixing the duty cycle at around 50% and setting input voltage to 7 volts, the circuit as shown in Figure 9 achieves the steady-state in almost 200 ms. The steady-state output voltage and current waveform of the 5th stage DC-DC boost converter is shown in Figure 14. The system rise time is 23 ms, while the system percentage overshoot is 34.9%. Since the response of the system is underdamped, the oscillations completely die out around 180 ms.

Figure 14. Output voltage and current for the fifth stage boost converter.

3.3. Loss Analysis

Various types of losses are affiliated with the DC-DC converter. The majority of the commonly associated losses are with diodes, the MOSFETs/IGBTs capacitor, and inductor losses. In Equations (23)–(31), the efficiency of the proposed converter is calculated for the fifth stage boost converter. It is assumed that the converter is ripple-free in current and voltage.

The losses affiliated with any IGBT or MOSFET include conduction losses, switching power losses and, if the output side capacitance is considered linear, side capacitance loss. The conduction loss for MOSFET and IGBT is given by Equations (23) and (24), while the output side capacitance loss is given by Equations (25) and (26).

\[
P_{\text{IGBT}} = V_{\text{CE(on)}} I_{\text{on}} \tag{23}
\]

\[
P_{\text{CMOSFET}} = V_{\text{DS(on)}} I_{\text{on}} \tag{24}
\]

\[
P_{\text{SW,IGBT}} = \left( E_{\text{on}} + E_{\text{off}} \right) f_{\text{SW}} \tag{25}
\]

\[
P_{\text{SW,MOSFET}} = 0.5 C_{\text{disc}} V_{\text{DC}}^2 f_{\text{SW}} \tag{26}
\]

The power loss associated with diodes in any converter during conduction is related by Equations (27)–(29). The inductor loss due to ESR is given by Equation (30). The efficiency of the system is given by Equation (31), where, \( P_{\text{loss}} \) is the sum of power loss across MOSFET/IGBT, diodes, and the inductor from Equations (23)–(30).

\[
P_{D_{\text{r}}} = r_D I_{\text{rms}}^2 \tag{27}
\]

\[
P_{D_{\text{f}}} = V_f I_{D_{\text{f}}} \tag{28}
\]

\[
P_{D_{\text{tot}}} = P_{D_{\text{r}}} + P_{D_{\text{f}}} \tag{29}
\]

\[
P_{L} = r_{L_{\text{DC}}} I_{\text{rms}}^2 \tag{30}
\]
In this section, we will analyze the minimum size requirement of the inductor, capacitor, and diodes based on their voltage stress, current stress, and ripple factors. For this purpose, it is necessary to have information regarding average current in case of inductance selection and voltage rating while selecting the capacitor size. This is because the capacitance and switching frequency play a major role in reducing the ripples in output voltage. Indeed, frequency and inductance selection reduce the ripples in current.

The capacity of a plate to store a charge on any plate is given by Equation (32), and the current through any conductor is given by Equation (34). After substituting Equation (32) in Equation (33), the minimum capacitance to reduce the ripple in output voltage for the proposed converter is given by Equation (34).

\[ \Delta Q = C \Delta V \]  
\[ I = \frac{\Delta Q}{\Delta t} \]  
\[ C_{min}(f_{sw}) = \frac{D V_o}{R_f \Delta V f_{sw}} \] 

The average current passing through the inductor when the switch is turned on is equivalent to the input current, and the voltage induced around it is given by Equation (35). When we substitute Equation (14) in Equation (34), we can obtain the minimum inductance requirement for the proposed converter in Equation (36). From Equation (36), we can design an inductor for any stage output voltage and with the desired ripple current \( \Delta i \).

\[ V_L = \frac{L \Delta i}{\Delta t} \]  
\[ L_{min} = \frac{V_o (1 - D) D}{f_{sw} \Delta t} \] 

The selection of MOSFET and switches can be easily carried out based on the required gain from Table 1. The proposed converter is designed to step up a minimum of five volts input to 50 volts output by using only the 5th stage boost converter. It can be easily extended up to the 10th stage but, due to input current limitations, the prototype is designed for only the 50 W test.

Table 1. Required components for the experiment.

| Components | Device Specifications | Quantity | Parameter |
|------------|----------------------|----------|-----------|
| Regulatable DC power supply \( (V_{in}) \) | 600 V, 20 A | 1 | 5–10 V |
| Resistive Load | Variable | 2 | 150 \( \Omega \), 1 A |
| Output DC voltage | 5 ports | | 13–75 V |
| Adjustable output power \( (P_o) \) | PWM | | 2–50 W |
| Switching frequency \( (f_s) \) | | | 20–50 kHz |
| Inductor | 3 mH, 10 A | | 3 mH, 10 A |
| Capacitors | Electrolytic | 9 | \( C_A = 2 \mu F, 100 V \), \( C_1 . . . C_{an} = 3000 \mu F, 50 V \) |
| Power Switch \( (S) \) | Infineon IPW60R045P | 1 | 650 V, 60 A, 45 m\( \Omega \) |
| Diodes | VS-15TQ060-M3 | 8 | \( V_{BR} = 1000, 15 A \) |
| Microcontroller | Arduini UNO | 1 | - |
| Oscilloscope | Lecroy waveRunner | 1 | - |
4. Experimental Results and Discussion

This section discusses the performance of the proposed converter. The following experiments are conducted to test the voltage regulation, system gain, output power delivered, inductor current to output current, and system efficiency by changing the duty cycle ratio. The proposed system can take any value of input voltage between 1–11 V. The maximum boosted voltage achieved at 10 V input is approximately 70 volts, and the maximum achieved power from this system is 50 W at a 100 Ω resistive load. A 50 kHz and a 15 V peak pulse voltage is applied to the gate of the Infineon IPW60R045CP. The experimental results are summarized from Figures 15–24. The required set of equipment and components used during the experiment is summarized in Table 1. For comparison, the different levels between 5–10 V are applied at the input side of the converter.

![Figure 15. Voltage gain analysis at different voltage levels.](image)

![Figure 16. Inductor to output current gain analysis for different voltages.](image)
Figure 17. Power analysis of the proposed system for different input voltages.

Figure 18. Voltage gain regulation as a function of load resistance.

Figure 19. Efficiency analysis of the proposed system.
Figure 20. Switch ZCS condition analysis.

Figure 21. Output voltage and current steady state analysis and a zoomed version (lower window).
Figure 22. Switching voltage and current waveforms at $D = 50\%$.

Figure 23. Diode current switching as a function of MOSFET switching voltage.
Figure 24. (a) Experimental test bench overview, (b) gate control and single stage boost converter and (c) multiple boost stage.
In Figure 15, the voltage gain analysis for varying duty cycles at three different input voltage levels (5 V, 7 V & 10 V) is summarized. The system voltage gain for any input voltage is the same but, it must be noted that it linearly rises as $D$ increases. These results align to Equation (14), and the system gain remains almost linear till it crosses 50%. Following this, the system tends to become nonlinear, and practically no further gain enhancement is achieved typically after $D = 60\%$. The inductor current to output current ratio as a function of the duty cycle at three input voltage levels is presented in Figure 16. As the duty cycle increases, the $I_L/I_o$ ratio gradually tends to decrease. The decrement in inductor current gain is more pronounced at higher voltage levels. This is because of the input to output power balance, as discussed in the previous section.

In Figure 17, power regulation at different input voltage levels as a function of $D$ is presented. As the input voltage level is increased, the output power also shows a significant increase. This demonstrates that, for a large duty cycle ratio or turn-on time, both output voltage and current increase the higher the power level goes. The output power level difference also shows that for high input voltage levels, the output power rise will be significantly higher. This means that for a low voltage, such as a 5 V input, there is a slight power loss across semiconducting devices.

We also tested the system against load variation. Since the proposed system is designed for a minimum of 100 $\Omega$ (section 3D), it is not recommended to use it with resistances lower than the designed value, otherwise the system gain will drastically drop. However, for any value of load the design procedure, as discussed in the previous section, must be considered. The experimental results to validate this fact are performed for the 7 volt input, as shown in Figure 18. In this experiment, the duty cycle is fixed at $D = 50\%$, while the resistive load is decreased in steps from 40 $\Omega$ to 100 $\Omega$. The output current increases with it, while the power drops from 15 W to 10 W, respectively. The overall gain decreases by 33%. This means that the voltage gain is dependent over load resistance.

To justify the proposed design, overall performance analysis is justified based on the power transfer efficiency from input to the output side of the system. The system input voltage is fixed at 10 volts while the duty cycle ratio is changed between 10–70 $\%$, and is calculated based on the calculations presented in section (3D). However, the overall result is presented in Figure 19 against various levels of output power, and is completely tabulated in Table 2.

Table 2. Efficiency analysis of the proposed converter.

| Loss Types | D = 10% | D = 20% | D = 30% | D = 40% | D = 50% | D = 60% | D = 70% |
|------------|---------|---------|---------|---------|---------|---------|---------|
| $P_{con}$ (mW) | 37      | 110     | 205     | 390     | 950     | 1300    | 2500    |
| $P_{osc}$ (mW) | 2      | 1.5     | 1.5     | 1.8     | 2.3     | 2.3     | 2.3     |
| $P_D$ (mW) | 240     | 240     | 320     | 360     | 280     | 250     | 260     |
| $P_L$ (mW) | 760     | 380     | 400     | 260     | 260     | 260     | 360     |
| Output power | 7.8    | 16.5    | 21      | 28.6    | 40.9    | 46.2    | 50.4    |
| $\eta$ (%) | 88      | 95.7    | 95.77   | 96.5    | 96.4    | 96.2    | 94.2    |

The experimental result of our proposed converter is presented for voltages and current in Figures 20–23. The control signal, which ensures zero switching currents (ZSC) for the proposed converter, is presented in Figure 20. It can be seen that as the switch turns off, boost voltage appears across its drain terminal, while the inductor current begins to fall to zero at the same time. The inverse happens when the switch turns on. The switching current and output (voltage, current) waveforms are presented in Figure 21. The ripples in the output current and voltage are measured to be less than 5% of the rated values. The average current flowing through boost stage one diode as a demo, as a function of switching voltage, is shown in Figure 23. The current switching is all according to the phenomena already explained in Section 2.1.

The experimental gate voltage, drain to source voltage, and current waveforms for 5 V input voltage and at $D = 50\%$ is shown in Figure 20. It shows that as the gate voltage
transit to zero, the \( V_{DS} \) peaks and, at the same instant, the drain current switches to zero, which ensures the zero current switchings (ZCS) condition. The output current and voltage waveforms at this condition are presented in Figure 21. Additionally, the zoomed-in version for this value of current and voltage waveforms is also shown in the lower side window of Figure 23. The ripples in current and voltage are very low, i.e., 4 mA and 1 V respectively. These values make around a 0.7% and 2% ripple factor of the output levels. This output voltage is also compared with the waveforms of switching voltage and current in Figure 23. The average diode current waveform connected to the load side is a current waveform in comparison to gate switching voltage is shown in Figure 22.

The performance analysis of the proposed converter in terms of voltage gain and current gain, along with maximum achieved efficiency and a minimum number of elements required in a single-stage boost converter, is presented in Table 3. Among these converters, SC-ANC, SC-AS-LC, and SL-DS-DC require at least two MOSFET switches to perform the analysis, while our proposed converter performs its work using only one MOSFET. Similarly, SC-AN, CL-SC, and SC-AS-LC-based topology require two minimum inductors to perform the single-stage boost converter. However, our converter performs its operation with only one inductor. The other components, such as diodes and capacitors, are variable, as they can be adjusted to achieve desired boost voltage level. The proposed converter not only reduces the overall size, but it also improves efficiency. Additionally, it also reduces control complexity and the number of single-stage boosting elements, which is the major contribution of the proposed work. The output voltage is almost smooth, and contains almost negligible ripples in current and voltage. The overall lab prototype of the proposed system is demonstrated in Figure 24.

### Table 3. DC-DC boost converter analysis.

| Topology     | \( G_V \) | \( I_L/I_o \) | \( V_{SW}/V_{in} \) | \( V_{D}/V_{in} \) | Max Efficiency | Minimum Elements |
|--------------|-----------|--------------|---------------------|---------------------|----------------|------------------|
| SL-SC [14]   | \( \frac{5D_L-D_T+3}{1-D_L-D_T} \) | \( \frac{G_L+1}{4} \) | \( \frac{G_V-1}{2} \) | 93                | 3              | 3                | 4                | 10              |
| CL-SC [19]   | \( \frac{2G_V}{1+G_V} \) | \( \frac{G_V}{2} \) | \( \frac{G_V}{2} \) | 93                | 1              | 3                | 2                | 3               |
| SC-ANC [24]  | \( \frac{1+D-D_T}{(1-D)^2} \) | \( \frac{1}{2} \) | \( \frac{1}{2} \) | \( 1+G_V \)       | 97             | 2                | 3                | 2               |
| SC-AS-LC [26] | \( \frac{1+D-D_T}{1-(1-D)^2} \) | \( \frac{1}{2} \) | \( \frac{1}{2} \) | \( 1+G_V \)       | 95             | 2                | 2                | 1               |
| SL-DS-DC [27] | \( \frac{3-D_T}{1-D} \) | \( \frac{G_V-1}{2} \) | \( \frac{G_V}{2} \) | \( G_V-1 \)       | 92.5           | 2                | 3                | 2               |
| Proposed Work | \( \frac{1}{1-G_T} \) | \( 1+G_V \) | \( \frac{G_V}{2} \) | \( \frac{G_V}{2} \) | 96.5           | 1                | 3                | 1               |

### 5. Conclusions

This paper proposes a high gain DC-DC boost converter with multiple boost stages. The overall size of the system has become more compact in comparison to other designs, with minimum reactive and switching elements. This is mainly because the single boost stage relies on one switch, capacitor, and inductor. The multiple-stage boost side requires a minimum of only two diodes and capacitors. As shown through experimental analysis, a single battery can be easily charged with a minimum of 5 volts, and its regulation is easily obtained by controlling the single switch using the PWM control technique. It is a single-stage boost converter along with multiple charging ports with stepped regulatable output voltage. With the reduced voltage and current stress, the device heating is also reduced and, as such, any extra heat sink requirements are lowered. The proposed design performance is verified by using both SPICE and an experimental setup and attains more than 90% efficiency throughout variable loads. The reliability of the proposed converter mainly relies on the LC selection and proper selection of the switching frequency. Improper selection will lead to the declination of output gain due to conduction losses. Since the multiple boost stages consist of diodes with large blocking voltage capacity, in case of fault the capacitor will not discharge back-stage and damage the main circuit. Instead,
will discharge through the load to the ground. It is also recommended not to operate the proposed converter without connecting the output load.

6. Future Challenges

The proposed converter has applications not only in high-power EV charging systems, but also in driving DC/AC electromechanical systems. The major challenge in using the proposed converter is as a bidirectional DC-DC converter mode. This is because the diodes used in the multiple boost stage are unidirectional and uncontrolled rectifiers. Secondly, if the diodes are replaced with active MOSFETs, then additional control strategies will be required in order to synchronously control the multiple boost stages. With this limitation, the proposed converter cannot be used in V2G applications.

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Nomenclature

| Symbol | Meaning |
|--------|---------|
| Δi     | incremental current |
| ΔQ     | incremental charge |
| ΔV     | incremental voltage |
| CCM    | continues conduction mode |
| CL-SC  | coupled inductor switch capacitor |
| Cn     | nth capacitor |
| Cosc   | output capacitor |
| D      | duty cycle ratio |
| ESR    | equivalent series resistor |
| EV     | electric vehicle |
| fsw    | switching frequency |
| Gv     | voltage gain |
| I0     | output current |
| ICE    | inter combustible engine |
| In     | input current |
| IMF    | International Monetary Fund |
| Ln     | nth inductor |
| NVS    | normalized voltage stress |
| Pc     | conduction power loss |
| PD     | diode power loss |
| PL     | inductor power loss |
| Ploss  | total power loss |
Symbol Meaning
QZS Z-source & quasi Z source
RL load resistance
SC switch capacitor
SC-ANC switch capacitor active netowrk converter
SL switch inductor
SL-DS-DC switch inductor double switch DC convertor
Sn nth switch
VL voltage across inductor
VMC voltage multiplier circuit
VSI voltage source inverter
Vsw Switch voltage
ZCS zero current switching
ZVS zero voltage switching

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