SHE-PWM LOW COST MULTI LEVEL INVERTER FOR PV BASED WATER PUMPING APPLICATIONS

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Abstract: In this article different multi-level inverter (MLI) configuration is introduced by a decreased quantity of power elements. At the output side the MLI topology generates the seven level voltage waveform with minimum number of components. The said topology configuration requires less dc voltage and power semiconductor switches. It also reduces the voltage block on switches, which reduces the inverter topology complexity and costs. Such capabilities were discovered by contrasting the topology to traditional topologies from the above perspectives. Testing were carried out to demonstrate the efficacy of the generalized MLI topology in both simulation and hardware, and the findings are presented for better understanding.

Keywords: Multi level Inverter, Photovoltaic, Pulse width Modulation, Selective Harmonic Elimination, Water pumping system, Total Harmonic system.

1. Introduction

Inverters based on high power semiconductor devices i.e. multilevel inverters (MLI) have become an essential component of extreme advanced world. They've been used in a variety of applications, including versatile AC transmission systems and electric vehicles [1, 2, 3, 4]. MLIs with higher voltage of output than any other traditional inverter has a credible sinusoidal occurrence. The high frequency of switching, low output harmonics make them a very effective solution [5,6,7].

The standard MLIs are divided into three types. They are multi-level inverters based on Flying Capacitor (FC), Neutral Point Clamped (NPC) and Cascaded H-Bridge (CHB). The multi-level CHB is mainly used in commercial processes for a great deal of power [8]–[11]. So many configurations with different switching techniques for cascading multi-level inverters [11]–[18] have been addressed in recent years. Various symmetrical MLIs were submitted in [8] and [19]–[23]. The major gain of these frameworks is the small voltage dc sources, one of the vital characteristics of the inverter cost determination. But at the other side, since most of them use many bidirectional power switches, isolated bipolar transistors (IGBTs) which is considered as key shortcoming of these configurations.

A new configuration of cascaded multilevel inverters is considered in this article, to increase the level voltage & decreases amount of various components and overall value of inverter. It should be noted that the unidirectional switches have been used in the considered topology. So a new SHE process is proposed to calculate magnitude of source. Because the output voltage is easy to synthesise and developing the switching circuitry, SHE-PWM was chosen for generating switching pulses. In the method, the required switching angles and its values determine the number with harmonic distortion to be removed from of the waveform output [24-25].
2. Block Diagram

The block diagram of the MLI for PV based pumping system is shown in figure 1. It consists of two PV Array’s connected to DC-DC Converter and MPPT controller to abstract extreme power from the source. The number of modules in PV array-2 is selected in that way it produce the double the power that PV Array-1 produce to maintain \( V_2 = 2 \times V_1 \). The PV arrays are connected to the multilevel inverter through DC-DC converter and these converters are controlled by MPPT controllers to abstract the extreme output from the available PV supply at different environmental conditions. Multilevel inverter with minimum switch is considered from the literature and analyzed in the next section.

![Figure 1: Block of the MLI for PV based pumping applications](image)

2.1. Circuit diagram

The minimum switch count based MLI is represented in figure 3 which consists of five switches with antiparallel diodes, the switch may be IGBT/MOSFET. The switching process of the circuit is evidently given in the Table I. the instantaneous switch ON of the switches in the same leg that is S1, S2 and S3, S4 causes voltage sources to short circuit. In the same switches S5 and S6 should not switch ON simultaneously.

![Figure 2: Topology framework of the considered MLI](image)

| Level No. | \( S_1 \) | \( S_2 \) | \( S_3 \) | \( S_4 \) | \( S_5 \) | \( S_6 \) | \( V_0 \) |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 1         | 1         | 0         | 0         | 1         | 0         | 1         | \( +V_{dc} \) |
| 2         | 0         | 1         | 1         | 0         | 0         | 1         | \( +2V_{dc} \) |
| 3         | 1         | 0         | 1         | 0         | 0         | 1         | \( +3V_{dc} \) |
| 4         | 1         | 0         | 1         | 0         | 1         | 0         | 0         |
|           | 0         | 1         | 0         | 1         | 0         | 1         | 0         |
| 5         | 0         | 1         | 1         | 0         | 1         | 0         | \( -V_{dc} \) |
| 6         | 1         | 0         | 0         | 1         | 1         | 0         | \( -2V_{dc} \) |
| 7         | 0         | 1         | 0         | 1         | 1         | 0         | \( -3V_{dc} \) |

Table 1: Output voltages of the considered topology
In table 1, 1 and 0 represents the ON and OFF of the power semiconductor switches correspondingly. The voltage sources considered in the above circuit is asymmetrical therefore there is a leeway of obtaining more number of voltage stages. If the DC voltage sources considered is symmetrical then we will get only three voltage levels.

2.2. Switching Technique
Typically, the output voltage from the inverter is attained by proper switching of available switches. Higher the THD at the output cause unwanted heating and generates less efficiency characteristics. Therefore, here selective harmonic elimination method considered in this article and total harmonics in circuit is reduced at the maximum extent.

![Figure 3: Seven level voltage waveform of the Inverter.](image)

Figure 3 displays the output waveform of required levels for calculating switching angles to reduce the THD.

\[ V_{\text{out}} = \frac{4V_{dc}}{\pi} \left[ \cos \alpha_1 - \cos \alpha_2 + \cos \alpha_3 + \cos \alpha_4 - \cos \alpha_5 + \cos \alpha_6 - \cos \alpha_7 + \cos \alpha_8 \right] \]

\[ V_{1_{\text{max}}} = \frac{4V_{dc}}{\pi} \text{ (c), by putting } \alpha_1, \alpha_2, ..., \alpha_9 = 0 \]

Modulating index: \( m = \frac{V_i}{V_{1_{\text{max}}}} \)

\[ mV_{1_{\text{max}}} = V_i \]

\[ 3m - \frac{4V_{dc}}{V_i} \]

At the angle of \( \alpha_4 \) the \( 3mV_{dc} \sin \omega t \) (required sine wave) is touching the \( V_{dc} \) level so the amplitude of sine wave is equal to \( V_{dc} \).

\[ 3mV_{dc} \sin \alpha_4 = V_{dc} \]

\[ \alpha_4 = \sin^{-1} \left( \frac{1}{3m} \right) \]

Where \( m = \text{modulating index} = 1 \)

\[ \int_0^{\alpha_2} 3mV_{dc} \sin \omega t \, dt + \int_{\alpha_2}^{\alpha_4} V_{dc} \, dt + 3mV_{dc} \sin \omega t \, dt = 0 \]

\[ -3V_{dc}(-\cos \alpha_3 + \cos 0) + V_{dc}(\alpha_4 - \alpha_5) - 3V_{dc}(-\cos \alpha_4 + \cos \alpha_5) = 0 \]

\[ -3 + \alpha_4 - \alpha_5 + 3V_{dc} \cos \alpha_6 = 0 \]

Substitute \( "\alpha_4" \) value in above equation to get \( "\alpha_2" \)

In the similar way, the required switching angles is calculated and switching technique is executed to produce the minimized THD.
3. Simulation and Experimental Results:
To maintain adequate quality in all output voltages of the considered MLI a seven level inverter exposed in figure 2 has been considered. The simulation is done using MATLAB/Simulink and experimental setup is made by using CT60 IGBT’s and microcontroller. The switching pulses is derived and given the switches to get required output voltage and it is revealed in the figure 3.

![Figure 4: Output voltage of the considered topology of MLI for Nine level Experimental setup is exposed in figure 4 and the yield voltage waveform is shown in figure 5. Topology produces a %THD of 3.4% which is acceptable for all commercial applications.](image)

4. Conclusion
In this paper the topology considered is simulated and validated by experimental setup. The 7-step output is attained with a %THD of 3.4% which is acceptable by the IEEE standard. The same topology can also be used for PV applications and irrigation applications as a future research work. As the topology is having lesser number of components, size and price of topology is very less with comparing of other recent and traditional H-bridge based MLI’s.

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