Depth-Optimal Quantum Circuit Placement for Arbitrary Topologies

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Received: date / Accepted: date

Abstract A significant hurdle towards realization of practical and scalable quantum computing is to protect the quantum states from inherent noises during the computation. In physical implementation of quantum circuits, a long-distance interaction between two qubits is undesirable since, it can be interpreted as a noise. Therefore, multiple quantum technologies and quantum error correcting codes strongly require the interacting qubits to be arranged in a nearest neighbor (NN) fashion. The current literature on converting a given quantum circuit to an NN-arranged one mainly considered chained qubit topologies or Linear Nearest Neighbor (LNN) topology. However, practical quantum circuit realizations, such as Nuclear Magnetic Resonance (NMR), may not have an LNN topology. To address this gap, we consider an arbitrary qubit topology. We present an Integer Linear Programming (ILP) formulation for achieving minimal logical depth while guaranteeing the nearest neighbor arrangement between the interacting qubits. We substantiate our claim with studies on diverse network topologies and prominent quantum circuit benchmarks.

1 Introduction

Quantum computation [1] promises to expand the reach of computing beyond classical — both theoretically and practically. In quantum computing, the operations take place on so called Qubits, which is a linear combination of the conventional Boolean states in the two dimensional complex Hilbert space. Each operation on these qubits...
can be defined by a unitary matrix $U$ which is represented by means of quantum gates. A quantum gate over the inputs $X = \{x_1, \ldots, x_n\}$ consists of a single target line $t \in X$ and, one or more control line(s) $c \in X$ with $t \neq c$. The following gates define the commonly used quantum gate library.

- **NOT gate**: The qubit on the target line $t$ is inverted.
- **Controlled NOT gate (CNOT)**: The target qubit $t$ is inverted if the control qubit $c$ is 1. This gate belongs to the general class of Toffoli gates, when accommodating larger number of control qubits.
- **Controlled $V$ gate**: The $V$ operation is performed on the target qubit $t$ if the control qubit $c$ is 1. The $V$ operation is also known as the square root of NOT, since two consecutive $V$ operations are equivalent to an inversion.
- **Controlled $V^\dagger$ gate**: The $V^\dagger$ gate performs the inverse operation of the $V$ gate, i.e. $V^\dagger = V^{-1}$.
- **SWAP gate**: The SWAP gate, as the name suggests, exchanges two qubits. This gate belongs to the general class of Fredkin gates, when accommodating control qubits.

A major challenge towards the realization of practical and scalable quantum computing is to achieve quantum error correction. Long-distance interacting Qubits is particularly susceptible to the noise. Therefore, prominent quantum technologies and quantum error correction codes, e.g. surface codes, require that the quantum gates must be formed with a nearest neighbour interaction. In the resulting circuits, the interacting Qubits may form a chain, as in a 1D Qubit layout, and therefore, these circuits are referred to as Linear Nearest Neighbor (LNN) circuits. Conversion of a quantum circuit to an LNN one can be achieved by using SWAP gates.

These SWAP gates allow for making all control lines and target lines adjacent and, by this, help to convert a given quantum circuit to a nearest neighbor one. More precisely, a cascade of adjacent SWAP gates can be inserted in front of each gate $g$ with non-adjacent circuit lines in order to shift the control line of $g$ towards the target line, or vice versa, until they are adjacent. This is shown using the following example.

**Example 1** Consider the circuit depicted in Fig. 1. As can be seen, gates $g_1$, $g_4$, and $g_5$ are non-adjacent. Thus, in order to make this circuit nearest neighbor compliant, SWAP gates in front and after all these gates are inserted as shown in Fig. 2.

Quite a few works have been done in recent past to convert a quantum circuit to an LNN one by introducing additional swap gates, which, naturally impact the circuit performance by increasing the logical depth and gate count. To that effect, heuristic and exact solutions are proposed, which balance the LNN conversion with other performance metrics. It is pointed out in that the problem of nearest
neighbour quantum circuit construction is equivalent to an NP-complete problem. Hence, it is unlikely that this problem can be solved optimally for large instances.

In parallel to the previous works, efficient LNN circuit construction has been studied for important quantum benchmarks, such as, quantum error correction [11] for Clifford+T gates [12]. In this work, we are primarily interested in the automated flow and for generic quantum circuits.

1.1 Qubit Topology

As noted in [9], the qubit topologies, on which the quantum circuit is to be mapped, are not necessarily of LNN structure. We provide a few examples here.

Recently, quantum error detection code is demonstrated on a square lattice [13]. It also highlights the fact that for a classical bit-flip, linear array of qubits suffices, while for general fault detection, extending to higher-dimensional lattice structures is needed.

Nuclear Magnetic Resonance (NMR) quantum computing achieved early success with realization of Shor’s factorization algorithm [14]. Liquid state NMR quantum computing utilizes the atomic spin states to realize the qubit and hence, has the molecular structures as qubit topologies. Solid state NMR has been also demonstrated [15] using crystal of NaNO₃, essentially leading to molecular topologies.

A recent proposition for scalable quantum computer indicates that multiple, parallel quantum gates can be formed between distant qubits by controlling the lasers on Trapped Atomic Ions [16].

Harnessing atomic spins in endohedral fullerene molecules as qubits have also been reported [17]. It has been further argued that molecular structures serve as a natural candidate for quantum technology by holding superpositions for longer period and ability to scaffold multiple molecules in a larger array.

Hence, an automated algorithm for achieving nearest neighbour interactions for a given quantum circuit while mapping on diverse qubit topologies are of significant practical interest. This is the main focus of current paper.

1.2 Related Works

To the best of our knowledge, [9] and [18] were the first to look into arbitrary topologies for quantum circuits with nearest neighbour constraints. So far, most of the other works in this domain have concentrated on 1D qubit layout or 2D qubit lattice structures [4, 6].

The work presented in [18] focuses on identifying the qubit topology best suited for a given quantum circuit placement. In contrast, our focus is towards evaluating a given qubit topology and performing mapping on it. This particular problem has been dealt with in [9] with examples taken from liquid state NMR molecules as the topologies. There, a graph partitioning-based approach is proposed and it is claimed to be asymptotically optimal for the case of chain nearest neighbour architecture. We address the same problem, by formulating it as an instance of ILP and show
that optimal results are achievable for a wide variety of benchmarks and different topologies.

Independently, efficient qubit topology identification and the mapping flows for specific interaction graphs have been done in [19, 20]. For example, it is proved that for cyclic butterfly topology, the depth overhead for mapping a given quantum gate to a nearest neighbour one is $6 \log n$. Subsequently, the mapping algorithm is also derived.

Communication and computation over networks is of major interest in quantum networks [21] as well as for classical telecommunication networks. The problem of permutation routing on variety of graphs has been studied in the past [22–24].

1.3 Motivation and Contribution

Despite the presence of diverse qubit topologies and need for an automated mapping flow of quantum circuits to such topologies, the current literature focuses mostly on 1D chain qubit and 2D lattice structures.

– In order to address this gap, we present an ILP-based algorithm to realize depth-optimal nearest neighbour quantum circuits. Our algorithm is also applicable, naturally, to simpler structures.

– We benchmark the algorithm for diverse topologies and quantum circuits and compare the scalability and performance against previous exact NN optimization approaches.

2 Preliminaries and problem statement

In this section, we introduce the notations and terminologies for formally defining the nearest-neighbor optimization problem of quantum computing. Thereafter, we present three variants of the problem.

Definition 1 A quantum circuit, defined over $n$-qubits $q_1, q_2, \ldots, q_n$ is a series of levels $L_i$, where each level $L_i$ consists of a set of quantum gates $G_{i1}^1, G_{i2}^2, \ldots, G_{ik}^k$ with each gate $G_{ij}^i$ operating on one or more qubits. Any two pair of gates $G_{ij}^i$ and $G_{ik}^k$ in a level $L_i$ do not operate on any common qubit and therefore can be executed in parallel. We assume that each level $L_i$ takes one cycle to execute. A quantum circuit with $k$ levels has a delay of $k$ cycles.

Given a quantum gate with $m$-control lines $l_1, \ldots, l_m$ and target line $l_t$, qubits $q_l$ and $q_t$ have to be nearest-neighbors, $1 \leq l \leq m$. For level $L_i$, we define interaction $I_i$ as the set of nearest neighbors for the all the gates in $L_i$. The levels and corresponding interactions of a quantum circuit is determined using Algorithm [1].

Example 2 Fig. [3] shows a quantum circuit with 5 two-input Toffoli gates and 2 CNOT gates. The circuit has 5 levels and hence has a delay of 5.

\[\text{xor5_254.real file from RevLib}\]
Fig. 3: A quantum circuit with delay 5

Fig. 4: Interactions for block size b = 2

\[ L_1 : [t_2 \times 2 f_0, t_1 \times 1, t_1 \times 3] \]
\[ L_2 : [t_2 \times 4 f_0] \]
\[ L_3 : [t_2 \times 0 f_0] \]
\[ L_4 : [t_2 \times 3 f_0] \]
\[ L_5 : [t_2 \times 1 f_0] \]

Corresponding to level \( L_1 \), interaction \( I_1 \) is \([ (x_2, f_0), (x_1), (x_3) ]\). Similarly, \( I_2, I_3, I_4 \) and \( I_5 \) is \([ (x_4, f_0) ], [ (x_0, f_0) ], [ (x_3, f_0) ] \) and \([ (x_1, f_0) ] \) respectively.

**Algorithm 1: Level Computation Algorithm**

```
Procedure ComputeLevel(devUseTable)
    levelList = [];
    processedGate = set();
    L = set();
    Lvar = set();
    for G_i \in QCkt do
        if G_i \notin processedGate then
            if G_i.var \cap Lvar == \phi then
                L.add(G_i);
                Lvar.add(G_i.var);
                processedGate.add(G_i);
                for G_j \in QCkt do
                    if G_j.var \cap Lvar == \phi then
                        L.add(G_j);
                        Lvar.add(G_j.var);
                        processedGate.add(G_j);
            levelList.add(L);
            L = set();
            Lvar = set();
    return reassignMap;
```

Physically, qubits can be arranged in various topologies, as discussed in the subsection 1.1. Such topologies allow interaction between only between some pairs of qubit positions. We introduce this constraint in the form of a topology graph.
Table 1: Minimum number of nodes in the smallest graph of each topology

| Topology     | Min. #Nodes |
|--------------|-------------|
| 1D           | 2           |
| Cycle        | 3           |
| 2D-Mesh      | 9           |
| Torus        | 9           |
| 3D-Grid      | 8           |
| Cyclic butterfly | 24         |

**Definition 2** A topology graph is an ordered pair \( T=(T_V, T_E) \). \( T_V \) is the vertex set, where each vertex \( v \in T_V \) represents a physical location where one qubit can reside. \( T_E \) is the edge-set, which contains a set of edges. An edge \( e_{vw} \in T_E \) indicates that qubit at location/vertex \( v \) and \( w \) can interact. In other words, qubits at location \( v \) and \( w \) are nearest-neighbors (NN).

Fig. 5 presents various topologies. The minimum number of nodes for the smallest graph of each topology is presented in Table 1. Given a quantum circuit with \( n \)-qubits, and a specific topology, we use the smallest topology graph \( T \) such that \( T_V \geq n \) for realizing the quantum circuit.

**Definition 3** A configuration \( C_t \) is the set of ordered tuples \((q_i, v)\), which indicates that in cycle \( t \), qubit \( q_i \), is at location \( v \), \( 1 \leq i \leq n \) and \( v \in T_V \). Configuration \( C_0 \) represents the initial configuration.

Fig. 5: Topology (a) 1D-nearest neighbor (b) Cycle (c) 2D-Mesh (d) Torus (e) Fully connected graph (f) 3D-Grid (g) Cyclic butterfly network
Table 2: Depth $D$ and Space $S$ complexity of realizing arbitrary permutations using a given topology.

| Topology                      | Degree | $D$       | $S$       |
|-------------------------------|--------|-----------|-----------|
| Fully Connected Graph         | $n-1$  | 1         | 1         |
| 1D nearest-neighbor [13]      | 2      | $2n - 3$  | 1         |
| 2D nearest-neighbor [19]      | 4      | $O(\sqrt{n})$ | 1         |
| Cyclic butterfly network [20] | 4      | $6\log n$ | 2         |
| Hypercube [19]                | $\log n$ | $O(\log^2 n)$ | 1         |

2.1 Problem statement

We now define three variants the nearest-neighbor optimization problem of quantum circuits for arbitrary topologies and also present the relation between the variants.

**Problem $P_1$:** Given an initial configuration $C$ of $n$-inputs, an interaction $I$ and a topology graph $T$, the objective is to determine the series of swap gates needed to transform the location of the qubits from configuration $C$ such that all qubit pairs in interaction $I$ are nearest-neighbors and the delay due to insertion of swap gates is minimum.

**Problem $P_2$:** Given an initial configuration $C$ of $n$-inputs, a series of interactions $I_1, I_2, \ldots, I_k$ and a topology graph $T$, the objective is to determine the series of swap gates needed to transform the location of the qubits from configuration $C$ such that all qubits pairs in interaction $I_1$ are nearest-neighbor, and then again location of qubits are transformed to be nearest neighbors for $I_2$ and so on, till interaction $I_k$ is met and the delay due to insertion of swap gates is minimum for the overall problem.

**Problem $P_3$:** Given an initial configuration $C$ of $n$-inputs, a series of levels $L_1, L_2, \ldots, L_k$ and a topology graph $T$, the objective is to determine the series of swap gates needed to transform the location of the qubits from configuration $C$ such that all qubits pairs in interaction $I_1$ (corresponding on level $L_1$) are nearest-neighbor, and then again location of qubits are transformed to be nearest neighbors for $I_2$ (corresponding on level $L_2$) and so on, till interaction $I_k$ (corresponding on level $L_k$) is met and the combined delay of swap gates and gates present in the actual circuit is minimum.

The Problem formulation $P_1$ has been popularly used for showing effectiveness of various topologies to realize arbitrary permutations. Table 2 shows the depth and space requirements for realization of arbitrary permutations on various topologies.

Problem $P_2$ with $k = 1$ is equivalent to Problem $P_1$. Therefore, finding an optimal solution for $P_2$ with $k = 1$ is equivalent to solving $P_1$. Problem $P_2$ does not consider the scheduling of the swap gates in parallel to quantum gates present in the original circuit, if possible. $P_3$ transforms the qubit locations on the topology graph such that the interactions needed to execute a level in quantum circuit is met. Problem $P_3$ addresses this issue and considers the quantum gates as well and can find the optimal solution with minimum delay.
### Table 3: Parameters/constants used in ILP

| Param/const. | Description                  |
|--------------|------------------------------|
| $G$          | Topology graph               |
| $C$          | Input/start configuration    |
| $n$          | Number of inputs             |
| $k + 1$      | Number of levels             |
| $L_i$        | Number of qubit interaction pairs in level $i$ |
| $T$          | Maximum number of cycles used for the problem |

**Theorem 1**  
For a topology graph $T$ and a quantum circuit $C$ with $k + 1$ levels, the delay $d_I$ of solution $S_I$ obtained by optimally solving problem $P_2$ is at most $k$-cycles more than the delay $d_O$ of optimal solution $S_O$ of problem $P_3$ i.e. $d_I - d_O \leq k$.

**Proof.** Consider an initial configuration and a quantum circuit two levels. Let us assume that the delay of solution be $d_I$ and $d_O$ be the optimal solution. Optimal solution for $P_3$ would have been able to insert additional gates at only one level $L_0$, which was not considered by $P_2$. If $d_I - d_O > 1$, this would imply that $d_I$ is not the optimal solution for $P_2$, since there exists a solution to solve $P_2$ with $d_O + 1$ delay which is a contradiction. This idea can be extended for any number of gates to derive Theorem 1. 

It is possible to split the circuits into equal size blocks, with $b$-levels in each block, except the last block which might have less than $b$ levels. Fig. 4 shows the blocks with size $b=2$, with the last block having a single interaction. Each block can solved using $P_2$ or $P_3$ to make the qubits nearest-neighbors and the output configuration of the solution is used as input configuration for the next block. For a quantum circuit with $k + 1$-levels and $b \geq k$, 

- Optimal solution with minimum delay $d_O$ can be determined using $P_3$.
- A bounded delay solution with delay $d_I$ can be determined using $P_2$ such that $d_I - d_O \leq k$.

Various suboptimal solutions can be obtained using $b < k$, using both $P_2$ and $P_3$. Choosing a small block size $b$ makes it easier to solve each sub-problem and therefore it becomes feasible to solve the nearest neighbor technology mapping problem for circuits with large number of gates. Corresponding to circuit in Fig. 3 the 1D-nearest neighbor compliant circuit, obtained using problem formulation $P_2$ and $P_3$ for block size $b = 4$, is shown in Fig. 6(a) and Fig. 6(b) respectively.

### 3 Methodology

In this section, we initially present an ILP formulation for the problem $P_2$. Description of the variables used in the formulation is presented summarily in Table 4. Thereafter, we present the modified ILP for problem $P_3$. 

Table 4: Variable description used in ILP

| Var. | Description | Var. | Description |
|------|-------------|------|-------------|
| delay | Delay due to insertion of swap gates | \( c_{v,q,t} \) | 1 indicates qubit \( q \) will move to new location \( v \) in cycle \( t \) |
| \( m_{x,t} \) | 0 indicates Interaction \( i \) met in cycle \( t \) | \( a_{x,t} \) | 1 indicates gates in Level \( i \) are scheduled in cycle \( t \) |
| \( \alpha_{p,q,t} \) | 1 indicates qubit \( p \) and \( q \) are NN in cycle \( t \) | \( e_{b_{x,t}} \) | 1 indicates interaction \( I_i \) has been met in cycle \( t \) and gates of level \( i \) can be placed in the current or following cycles. |
| \( P(p,v),(q,w),t \) | 1 indicates qubit \( p \) is in location \( v \) and \( q \) is in location \( w \) in cycle \( t \) | \( b_{q,t} \) | 1 indicates qubit \( q \) cannot be involved in a swap in cycle \( t \) |
| \( x_{v,p,t} \) | 1 indicates qubit \( p \) is in location \( v \) in cycle \( t \) | \( b_{v,q,t} \) | 1 indicates qubit \( q \) in location \( v \) cannot be involved in a swap in cycle \( t \) |
| \( u_{v,q,t} \) | 1 indicates qubit \( q \) will remain in location \( v \) in cycle \( t \) | \( s_{b_{m,n,t}} \) | 1 indicates swap is not permitted between locations \( m \) and \( n \) in cycle \( t \) |

3.1 ILP formulation for \( P_2 \)

Objective function:

\[
\text{Minimize } \text{delay} \quad \text{(1)}
\]

\[
\sum_{t=0}^{T} m_{k,t} - \text{delay} = 0 \quad \text{(2)}
\]
Chronological interaction constraints: If an interaction is met in cycle \( t \), then the status should not change to not met after that cycle. In addition, interaction \( i \) must be met before \( i - 1 \)th interaction is met.

\[
\begin{align*}
m_{i,t+1} - m_{i,t} & \geq 0 \quad 0 \leq t \leq T - 1, 0 \leq i \leq k \quad (3) \\
m_{i+1,t} - m_{i,t} & \geq 0 \quad 0 \leq t \leq T, 0 \leq i \leq k - 1 \quad (4)
\end{align*}
\]

Successful interaction constraints: An interaction is met if all the qubit pairs in the interaction are nearest neighbors. If an interaction has been met in cycle \( t \), then in all cycles \( t' > t \), the qubit positions do not matter any longer.

\[
L_{i,t} + \left( \sum_{(p,q) \in I_{i}} n_{p,q,t} \right) + \left( \sum_{t'=0}^{t-1} L_{i,1} - m_{i,t'} \right) \geq L_{i,1} \quad 0 \leq t \leq T \quad (5)
\]

Nearest neighbor constraints: Two qubits \( p \) and \( q \) are nearest neighbors if the qubits are in two locations \( v \) and \( w \) respectively or in \( w \) and \( v \) respectively, such that \((v, w) \in G_{E}\).

\[
\begin{align*}
p_{(p,v),(q,v),t} & = x_{v,p,t} \land x_{w,q,t} & (p, q) & \in I, (v, w) & \in G_{E} \quad (6) \\
p_{(p,w),(q,v),t} & = x_{w,p,t} \land x_{v,q,t} & (p, q) & \in I, (v, w) & \in G_{E} \quad (7) \\
n_{p,q,t} & = \bigvee_{(v,w) \in G_{E}} (p_{(p,v),(q,v),t} \lor p_{(p,w),(q,v),t}) & (p, q) & \in I \quad (8)
\end{align*}
\]

Qubit position update constraints: A qubit \( q \) is at location \( v \) in cycle \( t+1 \) if it was in location \( v \) in cycle \( t \) and there were no swaps performed involving the location \( v \) or if \( q \) was in a location \( w \) which is nearest neighbor with \( v \) and a swap was performed between \( v \) and \( w \).

\[
\begin{align*}
u_{v,q,t+1} & = (\land_{(v,w) \in G_{E}} (1 - s_{v,w,t})) \land x_{v,q,t} \quad (9) \\
c_{v,q,t+1} & = \lor_{(v,w) \in G_{E}} s_{v,w,t} \land x_{w,q,t} \quad (10) \\
x_{v,q,t+1} & = u_{v,q,t+1} \lor c_{v,q,t+1} \quad (11)
\end{align*}
\]

Qubit location and swap constraints: A qubit \( q \) can be at exactly one position in any given cycle. In a given cycle, a location can be involved in atmost one swap.

\[
\begin{align*}
\sum_{v \in G_{V}} x_{v,q,t} & = 1; \quad 0 \leq t \leq T, q \in Q \quad (12) \\
\sum_{(v,w) \in G_{E}} s_{v,w,t} & \leq 1; \quad 0 \leq t \leq T, v \in G_{V} \quad (13)
\end{align*}
\]

Initialization constraints: A qubit \( q \) is at location \( v \) in cycle 0, based on input configuration \( C \).

\[
x_{v,q,0} = 1; \quad (v, q) \in C \quad (14)
\]

This concludes the description of the ILP formulation for problem \( P_2 \). The following subsection presents the modifications needed in the ILP for optimally solving \( P_3 \).
3.2 ILP formulation for $P_3$

Objective function:

$$\text{Minimize } \sum_{i=0}^{k} \sum_{t=0}^{T} t a_{i,t} \quad (15)$$

Level scheduling constraints: Each level can be scheduled/activated exactly once.

$$\sum_{t=0}^{T} a_{i,t} = 1; \quad 0 \leq i \leq k \quad (16)$$

Only one level can be activated per time step.

$$\sum_{i=0}^{k} a_{i,t} = 1; \quad 0 \leq t \leq T \quad (17)$$

Activation for a level $i$ can happen only if corresponding interaction $i$ is met.

$$a_{i,t} + m_{i,t} \leq 1; \quad 0 \leq t \leq T, 0 \leq i \leq k \quad (18)$$

Swap blocking constraints: If an interaction $i'$ is met and all the gates in any Level $i$ such that ($i < i'$) have been scheduled, then swaps involving the qubits in interaction $i$ cannot be performed and interaction $i'$ is blocked till Level $i$ has been scheduled. Qubit involved in an interaction $i$ cannot be swapped in the cycle, when the Level $i$ is scheduled.

$$eb_{i',t} = a_{i,t} \land (1 - m_{i',t}); \quad 0 \leq i \leq k - 1, i + 1 \leq i' \leq k, 0 \leq t \leq T \quad (19)$$

$$b_{q,t} = \lor_i (a_{i,t} \lor eb_{i,t}); \quad \forall i, \exists q \in I_i, 0 \leq t \leq T \quad (20)$$

$$b_{v,q,t} = b_{q,t} \land x_{v,q,t}; \quad 0 \leq t \leq T \quad (21)$$

$$sb_{m,n,t} = \lor_q (b_{m,q,t} \lor b_{n,q,t}); \quad \forall q \in Q, 0 \leq t \leq T \quad (22)$$

In addition to these constraints, Chronological interaction constraints, Successful interaction constraints, Nearest neighbor constraints, Qubit position update constraints, Qubit location and swap constraints and Initialization constraints presented in ILP formulation for $P_2$ are applicable to $P_3$. This completes the description of the ILP formulation of $P_3$.

4 Experimental Results

In this section, we present the benchmarking results for multiple quantum circuits from [26] for various topologies. We used Gurobi [27] as ILP solver. For all the block sizes, we set TIME\_LIMIT parameter of Gurobi to 600 seconds to limit the time of execution of the solver, except for solving full circuit optimization for which we set TIME\_LIMIT to 7200. We set the number of threads parameter in Gurobi to 8. For the experiments, we used 64-bit Ubuntu 14.04 running on Intel(R) Xeon(R) CPU E5-1650 v2@3.50GHz with 15.6 GB RAM.
Table 5: Realisation of all configurations of 4-qubits for 1D-topology

| Config. | #S | D | Config. | #S | D | Config. | #S | D |
|---------|----|---|---------|----|---|---------|----|---|
| a b c d | 0 0 | b c a d | 2 2 | c d a b | 2 1 |
| a b d c | 1 1 | b c d a | 3 3 | c d b a | 1 1 |
| a c b d | 1 1 | b d a c | 3 2 | d a b c | 3 3 |
| a c d b | 2 2 | b d c a | 2 2 | d a c b | 2 2 |
| a d b c | 2 2 | c a b d | 2 2 | d b a c | 2 2 |
| a d c b | 3 3 | c a d b | 3 2 | d b c a | 1 1 |
| b a c d | 1 1 | c b a d | 3 3 | d c a b | 1 1 |
| b a d c | 2 1 | c b d a | 2 2 | d c b a | 0 0 |

Table 5 demonstrates realization of all possible configurations of 4-variables for 1D topology. The initial configuration is assumed to be [a,b,c,d]. #S and D is the number of swap gates required and the corresponding delay to realise the target configuration respectively. This table has been obtained using Problem formulation $P_2$ with $k=1$. We would like to highlight that configuration [a b c d] and [d c b a] are identical since for both the configuration the pair of nearest-neighbor variables is same.

Table 6 presents the results of 1D-Nearest neighbors for multiple block size $b = \{1, 2, 4, 8, 16\}$. The column Tech. indicates whether the solution for a benchmark is obtained using the problem formulations $P_2$ or $P_3$. Using a large block size is expected to reduce overall circuit delay, since the optimization solver can search a larger solution space to obtain optimal solution in that space instead of hitting a locally optimal solution. For circuit xor5_254, the delay for block side $b = 1$ is 9 while that with block size $b = 4$ is 7. On the other hand, by using a smaller block, it is possible to obtain a feasible solution within the time limits specified for the solver, since the solver has to solve a smaller instance of the formulated ILP. For example, solutions could not be obtained for $b \geq 4$ within the specified time limits for circuit alu-bdd_288. It should be noted that for all block sizes $b < L$, where $L$ is the number of levels in the circuit, the overall circuit is not guaranteed to have least delay, even when using formulation $P_3$ since combining the optimal solutions of the subproblems does not guarantee globally optimal solution.

We demonstrate the impact of topology on feasibility of nearest neighbor mapping for a given circuit. For this purpose, we used the circuit 4gt10 – v1.81 shown in Fig. 7. The circuit has a Toffoli gate with 3-control lines. This cannot be mapped using 1D-NN or cycle topology because a qubit can have at most two-neighbors in 1D or cycle topology. However, for other topologies, the mapping is feasible and the results using formulation $P_3$ are presented in Table 7. In order to make the nearest neighbor mapping feasible, the Toffoli gate with $n$-controls can be decomposed into a sequence of 2-control Toffoli gates $[28, 29]$. We used the RC-Viewer+ tool $[30]$ to decompose the circuit as shown in Fig. 8, followed by problem formulation $P_3$ to solve the nearest neighbor mapping problem for the same. As evident from the results, the decomposed circuit is now feasible to be mapped to 1D-NN and cycle topologies. For the other topologies, the mapping of the decomposed circuit has worse delay compared to the mapping of the original circuit, due the higher number of levels in the decomposed circuit.
Table 6: Benchmarking results for various block size for 1D-topology

| Benchmark          | #Var | #Gates | #L Tech. | b=1  | b=2  | b=4  | b=8  | b=16 |
|--------------------|------|--------|----------|------|------|------|------|------|
|                    |      |        |          | #S D | #S D | #S D | #S D | #S D |
| 3,17,14            | 3    | 6      | P_2      | 3    | 9    | 3    | 8    | 3    | 8    |
| 4gt11-v1,85        | 5    | 4      | P_2      | 3    | 9    | 3    | 8    | 3    | 8    |
| alu-bdd,288        | 7    | 9      | P_2      | 22   | 19   | 19   | 17   | —    | —    |
| ex-1,166           | 3    | 4      | P_2      | 1    | 5    | 1    | 5    | 1    | 5    |
|    ex1,226         | 6    | 7      | P_2      | 7    | 9    | 7    | 9    | 8    | 9    |
|    fredkin,7       | 3    | 1      | P_2      | 0    | 1    | 0    | 1    | 0    | 1    |
|    grayscale6,48    | 6    | 5      | P_2      | 0    | 5    | 0    | 5    | 0    | 5    |
|    ham3,103        | 3    | 4      | P_2      | 4    | 7    | 3    | 6    | 3    | 6    |
|    mod5d2,70       | 5    | 8      | P_2      | 6    | 12   | 6    | 12   | 9    | 10   |
|    one-two-three-v3,101 | 5 | 8 | P_2 | 11 | 13 | 11 | 13 | 10 | 13 |
|    peres,9         | 3    | 2      | P_2      | 2    | 4    | 2    | 4    | 2    | 4    |
|    rd32,272        | 5    | 6      | P_2      | 12   | 11   | 9    | 11   | 9    | 11   |
|    toffoli_double,4 | 4  | 2      | P_2      | 3    | 4    | 3    | 4    | 3    | 4    |
|    xor5,254        | 6    | 7      | P_2      | 7    | 9    | 7    | 9    | 6    | 9    |

Table 7: Benchmarking results for 4gt10-v1,81 using $P_3$ formulation, $w = 1$

|          | #G  | D  | ID  | Cycle | 2D-Mesh | Torus | 3D-Grid | CBN |
|----------|-----|----|-----|-------|---------|-------|---------|-----|
| Original | 6   | 6  | NF  | NF    | 11      | 11    | 5       | 7   |
| Decomposed | 12 | 12 | 25  | 26    | 14      | 21    | 6       | 15  |

For the first time, we report results for multiple topologies for various standard benchmark quantum circuits in Table 8. For each circuit, we consider the smallest topology graph with number of nodes greater than or equal to number of variables in the circuit. We have considered an arbitrary initial placement of the qubits on the topology graph. As expected, topologies with greater number of edges have lower delay. For example, the delay obtained for cycle topology is less than that for 1D topology. Multiple benchmarks for the 3D-Grid and cyclic butterfly network (CBN) did not complete execution within the specified time limit, due to the relatively large size of the topology graphs.
Direct comparison of our method to obtain nearest-neighbor compliant circuits with existing works could not be performed for primarily three reasons. The existing works [31–34] focus on determining linear nearest neighbors (LNN), with the objective of reducing number of swap gates. Our proposed method is for obtaining the LNN circuits with minimal depth which is contrary to the goal of reducing swap gate count. Secondly, the initial placement of the qubit is assumed to be given as input to the problem, but other works consider this as part of the optimization. Finally, most of the existing works decompose the gates into two qubit gates [4, 32, 34, 35]. In our work, we used unmodified circuits from RevLib [26]. For reference of the readers, we provide a brief summary of the existing results in terms of number of swap gates against the solution of our proposed methodology using problem formulation $P_3$ with block size $b = 4$, for the decomposed circuits in Table 8. Due to non-availability of

| Benchmark          | #Var | #Gates | #L Tech. | 1D | Cycle | 2D-Mesh | Torus | 3D-Grid | CBN |
|--------------------|------|--------|----------|----|-------|---------|-------|---------|-----|
| 3D_Cycle           | 3    | 6      | P_5      | 3  | 7     | 0       | 6     | 10      | 7   | 0     | 6   | 0   |
| 4gt11_v1_85.real   | 5    | 4      | P_5      | 3  | 7     | 0       | 6     | 14      | 7   | 0     | 6   | 0   |
| 4mod5_v1_25.real   | 5    | 4      | P_5      | 3  | 7     | 0       | 6     | 14      | 7   | 0     | 6   | 0   |
| alu_bdd_288.real   | 7    | 9      | P_5      | 3  | 7     | 0       | 6     | 14      | 7   | 0     | 6   | 0   |
| ex_1_166.real      | 3    | 4      | P_5      | 3  | 7     | 0       | 6     | 14      | 7   | 0     | 6   | 0   |
| ex1_226.real       | 6    | 7      | P_5      | 3  | 7     | 0       | 6     | 14      | 7   | 0     | 6   | 0   |
| fredi_kin_7.real   | 3    | 1      | P_5      | 3  | 7     | 0       | 6     | 14      | 7   | 0     | 6   | 0   |
| graycode6_48.real  | 6    | 5      | P_5      | 3  | 7     | 0       | 6     | 14      | 7   | 0     | 6   | 0   |
| ham3_103.real      | 3    | 4      | P_5      | 3  | 7     | 0       | 6     | 14      | 7   | 0     | 6   | 0   |
| mod5mils_71.real   | 5    | 5      | P_5      | 3  | 7     | 0       | 6     | 14      | 7   | 0     | 6   | 0   |
| one-two-three-v3_101.real | 5 | 8 | P_5 | 3 | 7 | 0 | 6 | 14 | 7 | 0 | 6 | 0 | 0 |
| peres_9.real       | 3    | 2      | P_5      | 3  | 7     | 0       | 6     | 14      | 7   | 0     | 6   | 0   |
| rd32_272.real      | 5    | 6      | P_5      | 3  | 7     | 0       | 6     | 14      | 7   | 0     | 6   | 0   |
| toffoli_double_4.real | 4  | 2 | P_5 | 3 | 7 | 0 | 6 | 14 | 7 | 0 | 6 | 0 | 0 |
Table 9: Comparison with existing works on LNN

| Benchmark  | #Var | #Gates | $P_{\text{opt}}(b = 4)$ | N=32 | N=34 | N=33 |
|------------|------|--------|--------------------------|------|------|------|
| 3_2,13     | 3    | 14     | 7                        | 6    | 6    | 4    |
| 4_49,17    | 7    | 32     | 15                       | 15   | 20   | 12   |
| 4gt10-v1,81| 5    | 36     | 33                       | 22   | 30   | 20   |
| 4gt11,84   | 5    | 7      | 5                        | 5    | 3    | 1    |
| 4gt13-v1,93| 5    | 17     | 18                       | 10   | 11   | 6    |
| 4gt5,75    | 5    | 22     | 25                       | 15   | 17   | 12   |
| 4mod5-v1,23| 5    | 24     | 22                       | 13   | 16   | 9    |
| alu-v4,36  | 5    | 32     | 26                       | 22   | 23   | 18   |
| hwb4,52    | 4    | 23     | 13                       | 9    | 14   | 10   |
| ham7,104   | 7    | 87     | 140                      | 83   | 84   | 68   |
| mod5adder,128 | 6 | 87 | 94                       | 65   | 85   | 51   |

the depth of the transformed circuits, we cannot compare the performance of our method against the existing works.

5 Conclusion

In this paper, we addressed the problem of nearest-neighbor optimization for a given quantum circuit, an arbitrary topology graph and an initial configuration specifying the location of qubits in the topology graph. We formulated the problem using two ILP variants — one of the variant for obtaining the optimal solution and a simpler variant that can obtain a bounded solution. In addition, our problem formulation allows the optimization to be performed as a large set of small optimizations or a smaller set of larger optimization problems, by setting appropriate block sizes. We demonstrated the effectiveness of our approach by running it on a set of benchmark circuits. Further research can be undertaken to solve the same problem for arbitrary topologies by heuristic based approaches that would allow scaling for larger circuits.

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