Design of a full-bridge type fault current limiter

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Abstract. Compared to AC system, DC power system is more likely to be damaged by short current, because in DC system the fault current increases faster and doesn’t have zero crossing point. The DC current limiter (FCL) can limit the rise of the current, thus it is efficient to use FCL to improve the reliability of the power system. Based on the previous research, we proposed an improved topology, established its mathematical model and analyzed its working processes. Besides, parameter design methods of solid-state DC current limiter are proposed by combining modeling and image analysis. And the control strategy of DC transformer short circuit fault crossing and recovery is put forward. Simulation and experiment results proved the effectiveness of topology and control strategy we proposed.

1. Introduction

With the development of economy and the continuous improvement of people's living standard, the electricity load is constantly increasing, which makes the complexity of the power system gradually increase. Meanwhile, ensuring the reliability of power supply is still the top priority of power grid operation [1]. In addition, with more and more medical and precision instruments with higher requirements for power quality are connected, requirements for the power system are new and higher.

Compared to the protection measures of traditional AC power distribution system, the research on the protection and fault treatment of DC system is still not so mature. Once the fault occurs, the short-circuit current of the DC system rises faster. Unlike the AC system, which has zero crossing point that could facilitate the circuit breaker's operation, the circuit breaker of the DC system faces a worse operating environment. And compared with AC circuit breaker, the cost for DC circuit breaker to improve its capacity is higher, so the research of DC current limiter to cooperate with circuit breaker is a new hot spot [2-3].

Although superconducting current limiter devices account for more than half of the project applications that have been put into operation, considering the technological breakthrough brought by the development of semiconductor technology these days, solid-state FCL is the future mainstream. The development of solid-state current limiter is largely due to the early promotion of American Electric Power Academy (EPRI). After several decades of efforts, prototype test of serial switching solid-state current limiter designed by EPRI topology was completed in 2004. In 2004, Tsinghua University proposed a two-times current-transfer short circuit current limiter used in DC system and proposed the theoretical analysis [4]. After that, topologies of current-limiting hybrid DC circuit breaker and some practical topologies of FCL were proposed, making DC FCL developed rapidly. [5-6]
2. Topology and Working Processes of DC FCL

Our research is based on the analysis and improvement of the previous topology in Fig.1. The fundamental principle of this kind of DC FCL is to make the direction of current in inductance alternates periodically by setting some specific switching law, so as to limit the current using the “passing low frequency and blocking high frequency” principle of inductance.

But the question is, in the topology in Fig.1 (a), voltage on the inductance can be really large, which is far large more than an IGBT can bear. So in Fig.1 (b), a resistance and capacitance are parallel with the inductance, which will play an important role in declining the voltage on inductance, thus the voltage that the switches need to bear is much lower. Simulation results also shows that this topology has good performance in decreasing voltage on switches.

![Topology in previous research](image1)

**Fig.1** previous topology and the improved topology we propose

In addition to the improvement in topology, the practical problems in engineering application of DC FCL also contains the design of movement law. Situation that all switch tubes are shut off at the same time should be avoided, otherwise the short-circuit current in main circuit will loss pathways, and the instantaneous change of current will cause a large voltage in inductance, which is harmful.

Therefore, it is necessary to reserve a dead zone, in other words, a certain transition time, during which all switch tubes are on. Switching law can be seen in Fig.2.

![Switching law of DC FCL considering dead zone](image2)

**Fig.2.** Switching law of DC FCL considering dead zone

When the DC FCL works, it has several different working conditions, and for each of the condition we can list several equations. For example, when S1 and S4 is off while S2 and S3 is on, equations are as follows.
\[
U = R (i_1 + i_c) + L_1 \frac{di}{dt} + L_0 \frac{d(i_1 + i_c)}{dt}
\]

But there is no analytical solution to the equations, so in order to prove its correctness, we use MATLAB to find the numerical solution to the equations, and then compare numerical solution with the simulation results. The comparison shows that the numerical solution corresponds to the simulation well, so we can use the calculation procedure in MATLAB to carry out the following analysis.

3. Parameter Design of DC FCL

3.1. Equivalent System of DC FCL

For the equivalent system in Fig.3, parameters of each component in the circuit need to be designed. The main objectives of our design are: (1) to control the peak value of the fault current within 300A; (2) to minimize the value of the reactance that occupies the largest volume in the current limiter, so as to reduce the volume of the current limiter device. And the initial value of the circuit parameters we use is in Table.1.

![Fig.3. Solid-state DC FCL equivalent system structure](image)

| Parameters | value | Parameters | value |
|------------|-------|------------|-------|
| $U_s$      | 750V  | $L_0$      | 0.004H |
| $R$        | 2Ω    | $L_1$      | 0.0004H|
| $C$        | 40μF  | $R_s$      | 0.01Ω  |
| $f$        | 3000Hz| Dead time ratio | 0.03 |

3.2. Parameter Design of Resistance and Capacitance

After some calculation and analysis, we set the switching frequency to 2000Hz, and the dead time is set
to 3%. There are several key parameters affecting the operating characteristics of DC FCL: inductance L1, inductance L0, resistance R and capacitance C, whose influences on fault current are relatively complex.

Our strategy is to find the combination of R and C that can make fault current smallest, then pick the smallest inductance combination that meet the design requirement, so as to make device volume smaller.

Fig.4. Three-dimensional fitting image of RC and fault current

Fig.4 shows the case that while other parameters remain unchanged, the value range of resistance is set as $[2\Omega, 5\Omega]$, and capacitance varies between $10\mu F$ and $60\mu F$. Then, the peak values of fault current corresponding to discrete points of different R and C combinations are calculated. A three-dimensional image using curve fitting toolbox is drawn in MATLAB. Through the graph above, we choose the resistance and capacitance combination, which is $R = 2.3\Omega$ and $C = 15.7\mu F$.

(a). Three-dimensional fitting image of inductance and fault current
(b). Equal peak current image

Fig.5. Three-dimensional fitting image and equal peak current image

After determining the values of R and C, we need to design the numerical values of inductance L1 and L0 using the same methods above, while the value range of L1 is set as $[0.0002H, 0.0006H]$ and L0 varies between $0.0004H$ and $0.004H$. After drawing the three-dimensional image using curve fitting toolbox, we also use it to obtain the "equal peak current" image made of the same peak current line, which can be the basis of choosing the combination of inductance.

As we can see in Fig.5 (b), the curve indicated by the labeled arrow is approximately the equal peak current line of 300A, on which we can pick the combination of inductance. In order to make the volume of current limiter smaller, the inductance should be as small as possible, we choose $L1=0.00028H$ and $L0=0.001H$. 
4. Simulation and Test Results
According to Fig.4, simulation model is established in PSCAD/EMTDC, which contains DC power supply, bridge current limiter structure, load and other auxiliary circuits. Parameter values are set according to our calculation and analysis above, which is also shown in Table.1. And experimental platform is shown in Fig.6.

![Experimental platform of DC FCL](image)

After using the experimental platform to carry out the test, we get the results of the current and voltage in different conditions, which contains both normal and fault conditions. Results show that the DC FCL we designed can limit the fault current to about 300A, while the voltage on IGBTs can be limited to about 850V, as shown in Fig.8, which can avoid the device being struck by the impulse voltage. And a series of other simulation and test with different parameter are also carried out, which are helpful in proving the effectiveness of the limiter we proposed.

![Waves of fault current in different working conditions](image)

![Voltage on IGBTs in different working conditions](image)
5. Conclusion
Based on the results and discussions presented above, the conclusions are obtained as below:

1. The designed current limiter can keep the voltage stress in a small range while having a good current limiting effect, and make the voltage at the inlet side of the current limiter drop within acceptable limits.

2. It is also indicated in the tests that under different input voltages the relationship between the peak fault current and the input voltage is approximately linear, which can provide a reference for the parameter design of the current limiter under different voltage levels.

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