GENERALIZED TAPPED INDUCTOR SWITCHER (GTIS) APPROACH TO MODELLING OF HIGH-ORDER CONVERTERS

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Abstract
A generalized modelling technique suited to integrated and high order Pulse-Width-Modulation (PWM) topologies is studied and proposed here. Most integrated converters have their switches shared by more than one inductive element. The proposed generalised tapped inductor switcher model takes full account of the properties of the shared switcher assembly and so extends the capabilities of the earlier tapped inductor switcher model. The proposed generalised tapped inductor switcher can accommodate both voltage and current switched inputs and thus can model a wide range of high-order PWM topologies. The topology of the GTIS block is proposed and its static and small-signal models are derived. The proposed approach is illustrated by analysing a tapped inductor Single Ended Primary Inductor converter. The validity of the proposed approach is verified by comparison of the theoretical, simulated and experimental results.

1 INTRODUCTION

Over the years, several modelling approaches were proposed for dynamic modelling of the pulse width modulated switching converters. These methodologies can mainly be classified into either analytical or equivalent circuit techniques. Potentially, each approach can yield the same results, however, differs by the required computational burden.

Analytical modelling aims to investigate the dynamics of switched circuits applying specialised mathematical tools and considering the particular topological properties of a given converter [1–8]. Perhaps the most popular approach is the state-space averaging (SSA) [1, 2]. Others include generalised SSA [3, 9], frequency-dependent averaging [4], averaging via KBM (Krylov-Bogoliubov-Mitropolsky) algorithm [5], discrete-time/sampled-data modelling [6–8] etc.

The equivalent circuit methods [10–16] are hinged on the idea of finding a continuous circuit model of the original switching circuit. The equivalent circuit retains the physical meaning of topology under study and can be conveniently applied to complex power stages. Also, it is suggested in [1] that any switching DC-to-DC converter can be reduced to a fixed canonical equivalent circuit. The idea of a canonical equivalent circuit was short-lived, however. The equivalent circuit approach was scrutinised and revisited by several authors who rather model the non-linear part of switching converter, that is, the switch, by a particular averaged circuit. Such an average circuit model can be substituted point by point to replace the switched network. Thus, the averaged circuit removes the switching frequency components while retaining the low-frequency characteristics of the system [10–17]. This provides an easy way to derive a dynamic model of a given converter and simplifies the analysis task.

The switching network can be defined in several alternative ways. A widely accepted model of a complementary switching block in Figure 1(a) is the three-terminal PWM switch model [12]. This model is characterised by a common node between PWM switches. This feature may pose difficulties applying it to some topologies such as Cuk, SEPIC or isolated converters, which have splits switches.

A split switch arrangement is shown in Figure 1(b), which can be treated with the two-port PWM model [13]. This module is quite flexible and can accommodate a wider diversity of PWM converters. However, the current and voltage characteristics of the block mainly depend on the peripheral circuit. As a result, the universal model of the block differs from the types of converter [13]. The switched inductor model [14, 15] shown in Figure 1(c) incorporates the inductor connected at the common node of PWM switches. Such equivalent circuit generates...
terminal currents in response to the terminal’s voltages and the duty cycle. While being quite an effective modelling tool this circuit is inconvenient to be used in topologies comprising tapped inductors or split switch arrangement.

The recently proposed tapped inductor switcher (TIS) model [17] is portrayed in Figure 1(d). TIS applies SSA, yet, is formulated using the flow graph technique [18–21]. TIS offers a generalised methodology to model various tapped inductor converters with different winding configurations. The regular switched inductor block in Figure 1(c), often encountered in PWM converters, can be regarded as a trivial case of the switched tapped inductor with unity winding ratio, \( a = 1 \) [17]. Thus, TIS can be used to model PWM converters with either regular or tapped inductors in which the switcher is excited by external voltage sources. Although possible, application of TIS to the modelling of the high-order and/or integrated topologies is inconvenient for the following reasons.

Many high-order topologies, such as SEPIC, Cuk, Zeta including their isolated versions, and tapped inductor derivatives, as well as many other converters found in alternative energy generation systems, may include two or more inductors connected to the junction point in between the PWM switches; see Figures 4 and 6. Thus, the switches appear to be shared by more than one inductive element. The key challenge in the modelling of such converters is modelling the shared switcher assembly. Earlier research showed that the modelling of high-order converters, comprising multiple switched inductive elements, can be accomplished using several three-terminal TIS blocks [22]. However, to identify the TIS blocks and establish their orientation within the circuit a preliminary circuit manipulation may be required. Such manipulation may not be immediately obvious and may require deeper consideration [23].

A modelling technique is derived here to accommodate a wider range of PWM topologies including the integrated and high-order converters in a straightforward manner. The proposed generalised taped inductor switcher (GTIS) model is developed with a particular aim to take full account of the properties of the shared switcher assembly and so extend the capabilities of the earlier TIS model. The proposed approach is hinged on considering the extra ‘hidden’ inputs and outputs introduced by the shared switcher. The resulting GTIS equivalent circuit can be applied without preliminary manipulation and, therefore, is ‘user friendly’ and better suited to modelling the high-order converters.

The static and small-signal models of the GTIS block is presented. And its application to the analysis of switching converters is elaborated. For example, the proposed modelling approach is applied to obtain the complete dynamic characteristics of a kind of a tapped inductor SEPIC (TI-SEPIC) converter. First, the steady-state model and DC solutions of the problem circuit are derived by the GTIS-SFG (Switching-Flow-Graph) method. Next, the small-signal model for the given converter specifications is obtained. The control-to-output and the line-to-output transfer functions are found, and their low-frequency gain coefficients are obtained.

To validate the theoretical predictions, PSIM simulation software was employed to acquire the frequency response data. The theoretical transfer functions of the TI-SEPIC example circuit were evaluated by SIMULINK software and compared to PSIM simulation results. To further confirm the proposed theory an experimental prototype of TI-SEPIC converter was built. Key waveforms of the converter and comparison plot of the theoretical versus the measured small-signal control-to-output frequency response are reported.

2 | MODELLING THE GENERALISED TAPPED INDUCTOR SWITCHER

2.1 | Derivation of the GTIS-SFG models

Compared to the original three-terminal TIS block, see Figure 1(d) [17], the GTIS block in Figure 2 has two additional terminals, designated as ‘3’ and ‘4’ at the primary and secondary windings of the tapped inductor, respectively. GTIS, same as earlier TIS, uses the equivalent winding ratio parameter defined as \( a = \frac{N_{10}}{N_{20}} \). Calculation rules of the equivalent turn \( N_{10}, N_{20} \) of various coupled inductor structures are given in [17].
As shown in Figure 2, while GTIS terminals 1 and 2 connect to the external circuit via a series switch, the switches appear in parallel to terminals 3 and 4. For this reason, terminals 0, 1 and 2 are voltage inputs, whereas terminals 3 and 4 can accept currents from external input sources. As a response to the external excitation terminals 0, 1 and 2 can output switched currents, $i_0$, $i_1$, $i_2$, whereas terminal 3 and 4 output switched voltages, $v_3$, $v_4$, to the external circuit.

The equations of the non-linear model of the GTIS operating in the continuous conduction mode (CCM) can be written off Figure 2 as

\[ i_1 = K(d) \left( i_{Lm} - i_3 - \frac{i_4}{a} \right) \]  
\[ i_2 = aK'(d') \left( i_{Lm} - i_3 - \frac{i_4}{a} \right) \]  
\[ i_i = i_1 + i_2 + i_3 + i_4 \]  
\[ v_3 = v_{Lm} + v_0 \]  
\[ v_4 = \frac{v_{Lm}}{a} + v_0. \]

Here, $K(d)$ is the switching function of the duty cycle variable, $d$, and the switching period, $T_s$, defined by

\[ K(d) = \begin{cases} 
1 & 0 \leq t < dT_s \\
0 & dT_s \leq t < T_s 
\end{cases} \]  

$K'(d')$ is defined similarly concerning the complementary duty cycle, $d'$:

\[ K'(d') = \begin{cases} 
0 & 0 \leq t < dT_s \\
1 & dT_s \leq t < T_s 
\end{cases} \]

Equations (1)–(7) allow construction of the non-linear GTIS flow graph model shown in Figure 3(a), which includes switched branches governed by the switching functions $K(d)$ and $K'(d')$. The model in Figure 3(a) is based on the earlier three-terminal TIS model [17] also introducing an intermediate variable (node)

\[ i'_{Lm} = i_{Lm} - i_3 - i_4/a. \]

Thus, GTIS includes a few additional branches to incorporate the input variables, $i_3$, $i_4$, and the corresponding output variables $v_3$, $v_4$ into the earlier three-terminal TIS model. Note that the branches to and from $i_3$, $i_4$, $v_3$, $v_4$, are linear, that is, independent of either $K(d)$ or $K'(d')$ switching functions, and do not introduce any additional dependence on the duty cycle variables, $d$ and $d'$.

Applying the procedure for modelling the non-linear switched branches [18] to the signal flow graph in Figure 3(a), the steady-state and the average small-signal models of the GTIS can be obtained as shown in Figure 3(b) and (c), respectively. Here, the details of derivation are omitted for brevity. The resulting average small-signal model in Figure 3(c) is linear and, therefore, is conveniently formulated in the Laplace domain.

Henceforth the following notation is adopted to denote the voltages, the currents and the duty cycle variables: $x = X + \hat{x}$, where $X$ is the steady-state (operating point) value, and $\hat{x}$ is the small-signal perturbation of a particular variable $x$.

### 2.2 Brief summary of high-order converters

GTIS can be identified as a primary building block of many hybrid converters including the recently proposed topologies
for alternative energy generating systems. For instance, GTIS block can be recognised as central to the three basic high-order converters Cuk, SEPIC and Zeta and their tapped inductor and transformer isolated versions illustrated in Figures 4–6.

Depending on the topologies at hand, GTIS's current input terminals '3' and '4' may or may not be in use. For instance, see Figure 4, Cuk-derived converters use both third and fourth GTIS inputs, whereas the SEPIC-derived converters in Figure 5 use only the third input and the Zeta-derived converters employ only the fourth terminal; see Figure 6. Thus, exploiting particular topological properties of a given converter allows simplifying its GTIS-based model.

Note that to model the isolated variants in Figures 4(b), 5(b) and 6(b), a virtual short is provided between the primary and the secondary sides of the transformer. The short helps to identify the GTIS orientation within the converter, but otherwise bears no impact on the converter’s performance so that the converter’s small-signal model and its transfer functions remain unaffected.

The complexity of high-order switching converters and the formidable analytical difficulties one encounters taking on the challenge of their small-signal modelling are reflected by the complexity of GTIS model in Figure 3. For instance, the isolated Cuk converter in Figure 4(b) is a six-order system and its exact analysis is far from being a trivial task. Yet, application of GTIS constitutes a more technically straightforward approach to modelling of this class of converters than the earlier intuitive-manipulation approach suggested in [22].
2.3 | Application guidelines

GTIS analysis of a given converter can be performed following the procedure described next. The procedure is adapted from [17] and repeated here for the sake of clarity.

1. Manipulate the circuit and identify the orientation and interconnect of GTIS block within the problem converter, determine the winding ratio \( a \) and dismiss the unused terminals and their associated branches.
2. Note the key \( v-i \) relationships at the GTIS terminals and construct the general GTIS-SFG model of the problem converter.
3. To obtain the steady-state model of the converter, substitute the steady-state GTIS-SFG model in Figure 3(b). Then solve to obtain the DC solution.
4. To obtain the small-signal SFG model of the given converter, substitute the small-signal GTIS-SFG model in Figure 3(c). Compute and plot the desired small-signal transfer functions if necessary.

In contrast, traditional SSA modelling method (SSA) needs more efforts:

1. steady-state analysis of the problem circuit;
2. derive the state variable equations of the circuit under each operation subintervals;
3. neglecting the ripple and doing averaging;
4. derive the steady-state model and obtain the steady-state solution;
5. introduce small-signal perturbation, derive the small-signal model;
6. derive the transfer function.

By comparison, steps 1–3 in SSA method which are time-consuming and tedious are not needed by GTIS method. Moreover, although steps 4–6 in SSA method are also needed by GTIS method, the implementation is much easier since the GTIS model has already been derived and only needs to be substituted into the problem circuit.

3 | APPLICATION EXAMPLE

The following application example of GTIS modelling methodology considers the high gain non-isolated TI-SEPIC DC–DC converter (TI-SEPIC) in Figure 7. The converter is a simplified version of [28]. The operation of the TI-SEPIC in Figure 7 is similar to that of a traditional SEPIC, however, the traditional SEPIC has a grounded inductor, whereas the converter in Figure 7 has its tapped inductor floating atop the capacitor \( C_1 \). This modification allows increasing the DC gain by unity.

The analysis will be carried out based on the assumptions of (a) CCM mode, (b) ideal (lossless) components and (c) negligible leakage inductances. The modelling procedure follows the application guidelines in Section 2.3.

3.1 | Identify the GTIS module in the non-isolated high gain tapped inductor SEPIC converter

As can be seen, the high gain TI-SEPIC converter employs GTIS’s terminal 3 to sink the current, \( i_3 \), whereas there is no current flowing into GTIS’s terminal 4. Therefore, in the analysis to follow, the associated pair of variables \( i_4 \) and \( v_4 \) are accounted for but, \( i_4 \) and \( v_4 \) are dismissed and their associated branches removed.

The winding ratio \( a \) in GTIS can be obtained considering

\[
N_{20} = \frac{N_2 + N_1}{N_1} \quad N_1 \quad n = \frac{N_2}{N_1},
\]

which result in

\[
a = \frac{N_{20}}{N_{20}} = \frac{1}{1 + n^2}, \quad (9)
\]

3.2 | Note the key \( v-i \) relationships and construct the general GTIS-SFG model of the TI-SEPIC

The small-signal \( v-i \) relationships at the GTIS terminals can be established examining Figure 7 and recalling that the switching part of the converter (represented by the dashed GTIS block) is to be replaced by its linearised model. The equations of the linear network external to GTIS can be written as

\[
\begin{align*}
\hat{v}_0(t) &= \hat{i}_1(t) = Z_{C_1}(s)\hat{i}_1(t) \\
\hat{v}_1(t) &= 0 \\
\hat{v}_2(t) &= \hat{v}_{out}(t) = Z_{out}(s)\hat{i}_2(t) = -Z_{out}(s)\hat{i}_2(t). \\
\hat{i}_3(t) &= \hat{Z}_L(s)\hat{i}_3(t) = \frac{\hat{v}_3(t) - \hat{i}_3(t)}{Z_L(i)}
\end{align*}
\]

Here \( Z_C(s) = r_L + s \), \( Z_{C_1}(s) = r_{C_1} + \frac{1}{\frac{r_{C_1}}{r_L} + s} \) and \( Z_{out}(s) = \frac{R}{1 + \frac{r_L + r_C}{r_{out}}} \) are the equivalent impedance of the input inductor, the capacitor \( C_1 \) and the filter capacitor \( C_0 \) and load, respectively. Also, \( r_L \) and \( r_C \) are the direct current resistance of the input inductor, \( L_0 \) and the magnetising inductance, \( L_{mag} \) respectively; and \( r_{C_1} \) and \( r_{C_2} \) are the ESRs of the capacitor \( C_1 \) and output capacitor \( C_0 \), respectively.
GTIS general model of TI-SEPIC converter can be constructed by applying (10), as shown in Figure 8. Here, the GTIS block is depicted as a black box.

### 3.3 GTIS steady-state model of TI-SEPIC

By substituting GTIS steady-state model Figure 3(b) into Figure 8 the steady-state SFG model of TI-SEPIC can be derived as illustrated in Figure 9. Here, it is understood that all the variables assume their steady-state values. Furthermore, for the steady-state analysis the impedances of the linear network are reduced to their DC values as follows:

\[
Z_{L}(s) = r_{L} + sL \rightarrow s \rightarrow 0 r_{L},
\]

\[
Z_{out}(s) = R \left( \frac{s}{rC_{0}} + \frac{1}{R} \right) \rightarrow s \rightarrow 0 R.
\]

At first glance it may seem problematic having a branch \((I_{0}–V_{0})\) with an infinite gain; see Figure 9. This, however, simply implies that the physical solution must fulfill \(I_{0} = 0\) for any \(V_{0}\). Following the same reasoning, one can conclude that \(V_{Lm} \rightarrow 0\) and \(V_{L} \rightarrow 0\).

The steady-state solution is obtained by solving the SFG in Figure 9:

\[
V_{out} = V_2 = \frac{1 + nD}{1 - D} V_{g}
\]

\[
V_{C1} = V_0 = V_{g}
\]

\[
\langle I_{L} \rangle = -\frac{V_{out}}{R} \frac{1 + nD}{1 - D} \tag{13}
\]

\[
\langle I_{Lm} \rangle = I_{Lm} - I_3 = \frac{(n + 1)}{1 - d} \frac{V_{out}}{R}. \tag{14}
\]

The relationships (11)–(14) appear as gain constants of the small-signal model derived in the next section.

### 3.4 GTIS small-signal model of TI-SEPIC

The small-signal model of the TI-SEPIC converter can be derived by substituting the GTIS small-signal model Figure 3(c) into Figure 8 (while keeping \(a = 1/(1 + n)\)). The resulting flow graph model of TI-SEPIC is shown in Figure 10. The numerical values of the gain coefficients are obtained from the DC solutions (11)–(14).

The small-signal GTIS-SFG model in Figure 10 allows deriving any desirable transfer function of the problem converter. For instance, applying the familiar flow graph analysis rules the desired control-to-output transfer function can be obtained from Figure 10 as

\[
\hat{\frac{v_{out}}{d}}(s) = K_d \frac{1 + b_1 s + b_2 s^2 + b_3 s^3}{1 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4}, \tag{15}
\]

whereas the line-to-output transfer function is

\[
\hat{\frac{v_{out}}{v_{g}}}(s) = K_L \frac{1 + b_1 s + b_2 s^2}{1 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4}. \tag{16}
\]

Here, the low-frequency gain constants are

\[
K_d = \frac{V_2(1 + d)}{(1 - d)^2}, \quad K_L = \frac{(1 + ad)}{(1 - d)^2},
\]

respectively, and the \(s\)-terms coefficients are

\[
a_1 = \frac{L_d(1 + nd)^2}{R(1 - d)^2} + \frac{L_{mn}r^2}{R},
\]

\[
a_2 = \frac{L_d(n + 1)(1 + nd)^2}{R(1 - d)^2} + \frac{L_{mn}r^2}{R},
\]

\[
a_3 = \frac{L_d(n + 1)^2(1 + nd)^2}{R(1 - d)^2} + \frac{L_{mn}r^2}{R},
\]

\[
a_4 = \frac{L_d(n + 1)^3(1 + nd)^2}{R(1 - d)^2} + \frac{L_{mn}r^2}{R}.
\]
\[ a_2 = L_1 C_4 + \frac{L_4 C_n (1 + nd)^2}{(1 - d)^2} + (C_1 + n^2 C_n) L_m. \]

\[ a_3 = \frac{L_4 C_1 L_m (1 + n)^2}{R(1 - d)^2}, \quad a_4 = \frac{L_1 L_m C_1 (1 + n)^2}{(1 - d)^2}, \]

\[ b_1 = \frac{-L_4 (1 + nd)^2}{R(1 - d)^2}, \quad b_2 = (L_4 + L_m) C_1, \]

\[ b_3 = \frac{-L_4 C_1 L_m (1 + n) (1 + nd)}{R(1 - d)^2}, \quad p_1 = 0, \quad p_2 = \frac{L_m C_1 (1 + n)}{1 + nd}. \]

### 4 SIMULATION AND EXPERIMENTAL VERIFICATION

Theoretical predictions were evaluated first by simulation. PSIM version 9.1.4 simulation program was used.

For simulation purposes, an ideal power stage was considered, that is, ideal switch models were used. The benchmark converter had the following set of parameters (in CCM mode): \( D = 0.44, n = N_2/N_1 = 3.4, R = 350 \, \Omega, V_o = 48 \, V, \quad V_{out} = 214 \, V, \quad L_m = 75 \, \mu H, \quad L = 200 \, \mu H, \quad C_1 = 22 \, \mu F, \quad C_m = 10 \, \mu F \) and \( f_s = 50 \, kHz \). Using PSIM AC-analysis option frequency responses of the benchmark converter in Figure 7 were obtained. Using the parameters above, theoretical transfer functions (15) and (16) were computed. Comparison plots of the simulated versus calculated responses of the benchmark converter are shown in Figure 11. Due to the rapid gain and phase variations at the vicinity of the high-resonant frequency PSIM has some difficulties in acquiring the precise response. Nevertheless, in all cases, the theoretical results stay in good agreement with the simulation.

A laboratory prototype of TI-SEPIC in Figure 7 was designed, built and tested. The parameters of the experimental converter are listed in Table 1. The key waveforms of the converter are shown in Figure 12.

For the listed set of parameters, the ideal theoretical control-to-output transfer function was derived from (15) as

\[ \frac{\ddot{v}_{out}}{\ddot{d}} = \frac{313.78 (1 - 0.946 \times 10^{-5} s^3 + 5.72 \times 10^{-9} s^2 - 2.814 \times 10^{-14} s^3)}{1 + 0.116 \times 10^{-4} s + 4.565 \times 10^{-8} s^2 + 4.88 \times 10^{-14} s^3 + 1.674 \times 10^{-16} s^4}. \] (17)

In Figure 13, the calculated response (17) of the ideal converter versus the measured small-signal control-to-output, \( \ddot{v}_d/\ddot{d} \), frequency response of the experimental TI-SEPIC with Venable 8805 frequency response analyser. The predicted and the measured responses stand in good agreement. The parasitic resistances of the components introduce additional damping and flatten the practical converter’s response.

The prototype converter and its experimental platform are shown in Figure 14.

### 5 DISCUSSION

The earlier TIS-SFG model represents a voltage-driven TIS, which generated terminal currents as a response to the applied voltages and the duty cycle. However, some complex integrated converters may also feed current into the switched coupled magnetic device. Analysis of such converters calls for an extended model that can correctly consider both voltage and current excitation applied to the switcher. This prompted the development of the GTIS as an extension to the earlier TIS switched flow graph modelling approach. GTIS includes a pair of direct current inputs that offer greater modelling flexibility than the original TIS. The employment of GTIS current inputs is optional and depends on the topological properties of the given converter.
FIGURE 12  Typical waveforms of the TI-SEPIC converter: (a) the switch gating voltage, $v_{gs}$, the input current, $i_g$, and the switch voltage, $v_{ds}$; (b) switch gating voltage, $v_{gs}$, switch voltage, $v_{ds}$ and the output rectifier current, $i_{out}$; horizontal scale: $5 \mu S$

FIGURE 13  Comparison of the ideal calculated, ideal simulated versus the measured small-signal control-to-output frequency response, $\frac{\delta v_o}{\delta d}$, of the experimental TI-SEPIC converter

TABLE 1  Prototype specifications

| Components                        | Specification |
|-----------------------------------|---------------|
| Rated power                       | 30 W          |
| Duty cycle                        | 0.44          |
| Input voltage (RMS)               | 24 V          |
| Output voltage                    | 102.7 V       |
| Load                              | 343 Ω         |
| MOSFET, $Q$                       | IRFB4321      |
| Output diode, $D_s$               | DPG151300     |
| Switching frequency               | 50 kHz        |
| Magnetising inductance, $L_m$     | 78 $\mu$H     |
| Turns ratio                       | $n = \frac{N_2}{N_1} = 3.1$ |
| Input inductance                  | 182 $\mu$H    |
| Output capacitor, $C_{o}$         | 10 $\mu$F     |
| Capacitor, $C_1$                  | 22 $\mu$F     |
| Snubber Resistor, $R_C$           | 25 kΩ         |
| Snubber capacitors, $C_{Cc}$      | 22 $\mu$F     |
| Snubber diode, $D_C$              | MBR40250      |

FIGURE 14  The experimental platform for testing the TI-SEPIC benchmark converter

The GTIS, having both voltage and current inputs, can be conveniently adjusted to model a wider class of PWM converters. Having six input and five output variables, GTIS represents a quite complex sub-system. This, however, justly reflects the fact of life that complex systems have complex models. Although the GTIS model in Figure 3(c) may seem intimidating, it is still a first-order sub-graph, same as the earlier TIS. This means that applying either GTIS or TIS eventually leads to the same system order, the same differential equations and the results are expected to be identical too.

The proposed GTIS contains the full information about the switched inductor cell which can be trimmed to the original TIS but not vice versa. A small-signal model of TI-SEPIC was obtained with the original three-terminal TIS model earlier [23]. The modelling procedure required preliminary manipulation of an equivalent circuit to identify the orientation of the two TIS
blocks to model such a converter. Such a drill is a preroga-
tive of an experienced specialist and may seem like a brain-
racking task for a novice. The proposed GTIS method is aimed
at bypassing this difficulty. As shown above, GTIS is straight-
forward to apply as it is strictly technical and involves no cir-
cuit manipulation. Both approaches yield identical theoretical
results.

The benefit of employing GTIS is at the initial stage of con-
verter modelling during the formulation of the preliminary flow
graph model. Applying GTIS requires little or no circuit manip-
ulation and, thus, suggests a more direct way to model the high-
order converters. GTIS is intended to be ‘dropped’ into a par-
ticular topology to model a switcher shared by two or more in-
ductive components. The increased number of inputs and outputs
allows GTIS to accommodate a wider range of topological sce-
narios, encountered in high-order converters while reducing the
circuit manipulation effort to the minimum. Depending on the
topological properties of the converter at hand, a few inputs
and outputs could be expected to remain unemployed or left
out of no interest. Therefore, upon the construction of the ini-
tial model, the associated branches can be removed yielding a
simplified flow graph model.

Yet, even with GTIS providing a shortcut to obtain the
desired model, the calculation of the converter’s high- or low-
transfer functions remains challenging. Application of sym-
bolic computation tools such as MAPLE, MATLAB, MA-
TH-EMATICA etc. is recommended to alleviate the calculation
burden.

6 | CONCLUSION

The paper proposes the steady-state and the average small-
signal models of GTIS and formulates to comply with the signal
flow graph analysis approach. The proposed GTIS-SFG model
can be applied to study the steady-state and dynamic properties
of converters comprised of a variety of interconnected inductive
deVICES, both regular and coupled, operating in the continuous
conduction mode.

A designer armed with the GTIS is relieved from the task
of deriving from scratch the state–space average equations of a
switcher circuit. Instead, the average model of a converter can
be obtained by point-to-point substitution of GTIS equivalent
CIRCUITS and subsequently by GTIS-SFG sub-graph. This simpli-
fies the modelling effort of complicated converters.

As an application example, the analysis of a kind of high
gain TI-SEPIC converter is presented. The given example first
derives the small-signal GTIS-SFG dynamic model from which
the key small-signal characteristics of the converter such as
control-to-output and line-to-output transfer functions were
obtained.

The evaluation of the theoretically predicted results was
done by comparison to PSIM simulation results and measure-
ments obtained from the experimental prototype. A good match
was found in all cases and supports the proposed modelling
approach.

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