Structural, Electronics and Optical Properties of CaO

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Abstract. The carrier effective masses of CaO in the cubic phase are estimated by ab initio calculations, which are used for the simulation of Si/CaO metal-oxide-semiconductor (MOS) devices by solving Schrödinger and Poisson equations self consistently. It is shown that higher switching speed, longer lifetimes, and higher endurance can be obtained replacing SiO₂ by CaO as gate dielectric, suggesting promising biomedical applications for Si/CaO-based MOS devices due to the CaO bio-compatibility.

Concerns with reliability and gate leakage currents through ultrathin SiO₂ dielectrics in metal-oxide-semiconductor field-effect transistors (MOSFET’s) are driving research efforts to find appropriate high dielectric constant (high–κ) materials for SiO₂ replacement. CaO may be considered as an interesting candidate for SiO₂ replacement as a dielectric gate material. It exhibits high mechanical and radiation resistance, and its wide band gap energy (7.1 eV) combined with a reasonably high dielectric constant (11.8) indicates a typical insulator behavior [1]. Concerning bio-compatibility, CaO incorporation in TiN–based films [2] and diamond-like carbon [3] is improving biological acceptance of these materials for bio-medical applications. The formation of a Ca–O–Si heterobridging bond favors Si–Ca–O interfacing, which points to a feasible development of improved bio-compatible Si-based biosensors through growth of CaO films in silicon surfaces [4].

In this work we perform a first-principles study of the electronic properties of the CaO cubic phase, estimating its band gap energy and carrier effective masses, which are fundamental for device simulation. To demonstrate the possibility of CaO for MOS device applications, we calculate the low frequency capacitance and the electrostatic potential drop within the oxide of both Si/CaO and Si/SiO₂ MOS devices, which allows a direct comparison of the role of CaO and SiO₂ as gate dielectrics. The calculations were performed with the ABINIT code, which is based on self-consistent plane-wave expansion combined with ultrasoft pseudopotentials [5]. For the sake of comparison, many-body effects were described in the local density approximation (LDA), using the Perdew-Zunger exchange term [6] with the Ceperley-Alder parametrization [7], and in the generalized gradient approximation (GGA), within the framework of the Density Functional Theory (DFT). The 3s²−, 3p⁶−, and 4s²-Ca; 2s²−, and 2p⁶−O electron states were treated as part of the valence-band states. In the CaO cubic phase, the cations Ca and anions O are located at...
(0,0,0) and (0.5,0.5,0.5), defining a fcc unit cell. Through a total energy minimization process with a cut-off energy of 700 eV, the lattice constants $a = 4.712$ Å (LDA) and $a = 4.819$ Å (GGA) were obtained. These values are in very good agreement with the measured value $a = 4.81$ Å [8].

Figure 1. CaO band structure along high-symmetry axis of the cubic Brillouin zone calculated using both GGA (solid line) and LDA (dashed) approximations.

Figure 1 exhibits the calculated band structure of cubic CaO along the main high-symmetry directions in the Brillouin zone (BZ) for both LDA and GGA approximations (relativistic contributions were disregarded). CaO presents an indirect band gap with conduction band minimum located at the X-point. In addition, there is a secondary energy valley at the Γ-point giving rise to a direct band gap. For the indirect band gap, we obtained $E_{G(\Gamma \rightarrow X)} = 3.44$ eV (LDA) and $E_{G(\Gamma \rightarrow X)} = 3.67$ eV (GGA), while for the direct one we obtained $E_{G(\Gamma \rightarrow \Gamma)} = 5.07$ eV (LDA) and $E_{G(\Gamma \rightarrow \Gamma)} = 4.79$ eV (GGA). All theoretical values for the band gap energy are smaller than the experimental gap of 7.1 eV [1], which is due to the well-known underestimation of the energy values of conduction band states in ab initio calculations within the density functional theory. There are several others first-principles calculations of the CaO electronic properties [9, 10], in which $E_{G(\Gamma \rightarrow X)}$ and $E_{G(\Gamma \rightarrow \Gamma)}$ were estimated to be in the 2.91−14.96 eV and 5.02−9.71 eV range, respectively. However, no data concerning the carrier effective masses were published previously.

The CaO carriers effective masses for the main directions in the Brillouin zone are shown in Table 1. They were obtained by fitting to a parabola, the curves of energy versus $\vec{k}$ along the $\Gamma \rightarrow X$ and $\Gamma \rightarrow \Gamma$ lines. We observe that the carriers effective masses are highly anisotropic in both conduction and valence bands, and that there is a large discrepancy between results obtained with the LDA and GGA approximations. Since experimental results on the effective masses in cubic CaO are still lacking, a direct evaluation of our theoretical estimates is not possible.

The primary requirement for a gate dielectric to be used in MOS devices is to efficiently block the charge carriers between the channel and the gate. Thus, energy barriers for both electrons and holes in the semiconductor substrate have to be high enough in order to prevent thermally stimulated injection. Unfortunately, recent results reveal that the energy gap is inversely proportional to the dielectric constant for several candidate oxides [11]. In the case of CaO, its reasonably wide band gap makes it a feasible option for this task. However, the energy barriers are not known because the Si/CaO band offset has not been measured yet. Here, we
Table 1. CaO carrier effective masses (e ≡ electron; hh ≡ heavy hole; lh ≡ light hole) in terms of the free electron mass $m_0$, estimated from the band structure for both LDA and GGA approximations.

|     | LDA               | GGA               |
|-----|-------------------|-------------------|
|     | k-direction       |                   |
|     | e             | hh           | 1.68 | 6.42 | 4.47 |
|     | lh           | 0.29 | 1.73 | 1.47 |
|     | m_ΓX/m_0       | 1.02 | 5.24 | 1.77 |
|     | m_ΓK/m_0       | 0.73 | 6.17 | 1.43 |
|     | m_ΓL/m_0       | 0.71 | 1.62 | 0.97 |
|     | m_ΓT/m_0       | 0.55 | 3.22 | 1.05 |

anticipate the electric characteristics of a Si/CaO MOS. In order to simulate a MOS capacitor, some CaO parameters are necessary, namely its carriers effective masses and the energy barriers at Si/CaO interfaces. The former parameters were extracted from our *ab initio* calculations, while the latter were estimated from the difference of electron affinities ($\chi_{Si} = 4.05$ eV and $\chi_{CaO} = 0.7$ eV) of both materials, which yield $\Delta E_{C(Si/CaO)} = 3.35$ eV and $\Delta E_{V(Si/CaO)} = 2.65$ eV for electrons and holes, respectively. We remark that these values are similar to those of the Si/SiO$_2$ interface, namely $\Delta E_{C(Si/SiO_2)} = 3.2$ eV and $\Delta E_{V(Si/SiO_2)} = 4.6$ eV.

The devices modeled in this work are basically MOS capacitors with metallic gate, having a silicon substrate doped with p-type impurities ($N_A = 10^{17}$ cm$^{-3}$) and CaO as the gate dielectrics. For the sake of comparison, we also simulate Si/SiO$_2$ MOS devices. For a realistic simulation, self-consistent calculations of the Schrödinger and Poisson equations are employed. This method is widely used in device simulations and it is discussed elsewhere [12, 13]. As for gate leakage currents, our model relies on the WKB approximation to calculate the tunneling probability of electrons in the channel through the gate dielectrics [13, 14].

The ratio of the total capacitance at low frequencies ($C_{TOT}$) and the oxide layer capacitance ($C_{OX} = \varepsilon_0 A/T_{OX}$) is depicted in Fig. 2a, where $\varepsilon_0$ is the dielectric permeability, $T_{OX}$ is the oxide layer thickness, and $A$ is the capacitor area under inversion bias for SiO$_2$- and CaO-based MOS devices. The CaO-based device exhibits a reasonably smaller capacitance in comparison to the SiO$_2$-based capacitor, which is a direct consequence of the higher CaO dielectric constant.
This difference becomes larger for ultrathin oxide thicknesses. Through the relaxation time constant of a $RC$ circuit given by $\tau = RC$, where $R$ and $C$ are the resistance and capacitance of the $RC$ circuit, respectively, one concludes that the charging/discharging times is smaller for Si/CaO MOS capacitors. This indicates the possibility of higher switching speeds during device operation. By comparing devices with the same capacitance (see the horizontal lines in Fig. 2a), we conclude that CaO dielectrics exhibits an equivalent oxide thickness a third smaller than SiO$_2$, which is confirmed by the dielectric constant ratios $\epsilon_{\text{CaO}} / \epsilon_{\text{SiO}_2} \approx 3$. Moreover, by comparing the gate leakage current through the equivalent 3 nm thick CaO layer and a 1 nm thick SiO$_2$ dielectrics, the current in the former case is nearly six orders of magnitude smaller for gate voltages ($V_G$) above 1.0 V. In respect to the device electrostatics, our MOS device simulations indicate that the electric field within the oxide layer is weaker for CaO layers. For a 3 nm thick oxide, this difference can be as high as 20%. Therefore, considering the role of the dielectric breakdown, CaO oxide layers also offer the advantage of longer lifetimes and higher endurance in comparison to SiO$_2$. These results are depicted in Fig. 2b, which displays the electrostatic potential drop within the oxide and substrate as function of the gate voltage. The electric field in the oxide is uniform due to the absence of charges and can be estimated by $E_{\text{OX}} = \Delta V_{\text{OX}} / T_{\text{OX}}$. As for the potential drop in the substrate, the figure shows that the band bending is higher in Si/CaO than in Si/SiO$_2$ MOS devices. Consequently, the amount of charge stored for inversion biases is also higher with CaO as dielectric gate material.

In conclusion, we have calculated the cubic CaO band structure to obtain its carrier effective masses along $\Gamma - X$ and $\Gamma - \Gamma$ lines and have estimated the Si-CaO band offset, which allowed us to simulate Si/CaO MOS devices. Our results indicate that CaO might represent an alternative material candidate for SiO$_2$ replacement as gate dielectrics in certain applications. Despite a higher switching speed, longer lifetimes, and higher endurance of Si/CaO MOS devices in comparison to Si/SiO$_2$ MOS devices, it is important to remark that problems related with the CaO reactivity with water and unperfect Si–Ca–O interfacing should restrict the use of CaO for MOS biodevice applications.

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