The influence of the deep level type on a switching time delay of GaAs avalanche S-diodes

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Abstract. In this work, the influence of the deep level type on a switching time delay of GaAs avalanche S-diodes is investigated. It is shown that the dependence of time delay on voltage can be approximated by an exponential function. The 1.5 times increase of voltage leads to significant decrease of time delay (up to 1000 times). The avalanche S-diodes doped with Fe and Cr/Fe impurities exhibit better stability than diodes doped with Cr. The switching time instability (jitter) for the S-diodes based on GaAs doped Fe or Cr/Fe was 14 times less than for the S-diodes based on GaAs doped with Cr at the same switching conditions.

1. Introduction
Transition metals, such as manganese, chromium, iron, and copper create deep acceptor levels in GaAs energy band gap. Iron and chromium impurities are used for production of semi-insulating material with resistivity of $10^5$ and $10^9$ $\Omega \cdot cm$, respectively. It makes possible to produce $\pi$-$\nu$-$n$ structures, with hole- and electron- conductivity layers of high resistance. Semiconductor structures based on GaAs with deep levels are used for production of avalanche $S$-diodes [1,2]. The reverse current-voltage characteristics ($I$-$V$-curves) of the $S$-diodes have a region with negative differential resistance (NDR). For the first time, this device was described in [3], where GaAs structures doped with iron were used. The authors of different works explained the $S$-type $I$-$V$-curve using the mechanism of recharge of deep levels [1,2,4]. Recent results allow to associate the NDR with the generation of collapsing Gunn domains in the avalanche regime [5,6].

Traditionally, in solid-state pulsed power technology, the field-effect transistors and insulated-gate bipolar transistors are used. As a rule, the switching times of this devices are relatively large (more than 5-10 ns). For the switching in subnanosecond range, another pulsed power devices are used: drift step recovery diodes [7], or avalanche devices, such as sharper diodes [8] and high-gain photoconductive switches [9,10]. The $S$-diode is an avalanche device which have typical switching times of 0.05-2 ns, and the threshold voltages of 50-2000 V. This makes possible to use it in pulse power suppliers for high power semiconductor lasers [11]. Another promising applications are pulse power suppliers for ultrawideband radars and lidars or electrooptical modulators with Pockels cells.

It is well known, that all avalanche devices suffer from poor switching stability which is caused by random nature of switching. According to statistics, to increase the stability (to decrease the deviation of the time delay) the time delay of switching should be decreased. In this study we investigate the influence of deep level impurities on a time delay and stability (jitter) of switching of the avalanche S-diodes.
2. Experimental conditions

The GaAs (100) wafers were grown by vertical gradient freeze (VGF) method. The three types of structures were made from this material. The first structure (GaAs:Cr) was made in the process of diffusion of chromium into the \( n \)-GaAs wafer. The second structure (GaAs:Fe) were made by diffusion of iron into \( n \)-GaAs, and the third one (GaAs:Cr, Fe) was made by diffusion of chromium and iron into \( n \)-GaAs. Initial concentration of donor impurity in GaAs was \( 5 \times 10^{16} \text{ cm}^{-3} \). The avalanche S-diodes were made by the planar mesa-technology. The diffusion was performed using the techniques which are described in [12, 13]. The thickness of the \( \pi \)-layer (doped with iron) was \( d_{\pi} \approx 36 \mu \text{m} \) (the average resistivity \( \rho_{\pi} \approx 2 \times 10^{5} \Omega \cdot \text{cm} \)), the thickness of the \( \nu \)-layer (doped with chromium) \( d_{\nu} \approx 51 \mu \text{m} \) (\( \rho_{\nu} \approx 2 \times 10^{9} \Omega \cdot \text{cm} \)).

After process of diffusion, substrates were cut to chips of square form with 800 \( \mu \text{m} \times 800 \mu \text{m} \) size. Each chip was placed into microwave metal/ceramic package. Contacts were made from the Pb (6\%)-Sn (91\%)-Ag (3\%) alloy. The contacts were formed at \( T = 580^\circ \text{C} \) in hydrogen atmosphere. The schematic view of the S-diode structure is shown in the Figure 1.

![Figure 1. Schematic view of the S-diode structure.](image)

The time delay characteristics were measured in sharper circuit with a load of 51 \( \Omega \) (figure 2). The rising edge of a triggering voltage pulse was 5 ns. Pulse frequency was 10 Hz. In the measurements, the LeCroy WaveSurfer 104 Xs oscilloscope (1 GHz bandwidth) was used. We measured the time delay of S-diodes as a function of applied pulse voltage. A time delay was considered as a time between a 0.5-level rising edge of a triggering pulse and a 0.5-level rising edge of the pulse after S-diode switch-on.

![Figure 2. Schematic view of the measurement setup: 1 – triggering generator; 2 – S-diode holder and load resistance \( R_n \approx 51 \Omega \); 3 - (Ch1, Ch2) first and second channels of the oscilloscope, \( U_0 \) and \( U_n \) – amplitudes of voltage for triggering pulse and pulse at the load, respectively.](image)
3. Experimental results

Figure 3(a) shows the time delay ($t_d$) dependence on a triggering pulse voltage. These curves are well approximated by equation $\lg t_d = A - B \cdot U^{-1}$ (where $A$ and $B$ are the constants). These data indicate that time delay decreases when voltage increases. It should be noted, when voltage increases in 1.5 times, the time delay changes from 30 $\mu$s to 50 ns. It is known from the literature that for S-diodes based on $\pi$-$\nu$-$n$ structures, the most probable mechanism of time delay dependence on voltage is the process of recharging of deep centers during the microplasma avalanche breakdown in $\pi$-$\nu$ junction [1]. The slopes of the curves depicted in figure 3 are different for different types of structures. As illustrated in figure 3(a), the slope of the curve for GaAs:Fe structure less than for structure with chromium impurities (GaAs:Cr and GaAs:Cr, Fe).

Figure 3(b) shows jitter dependence on voltage ($U^{-1}$). Here the jitter was measured for 600 switching events and it represented the total range of measured time instability. Thus, jitter equals to $6 \cdot \sigma$ ($\sigma$ - standard deviation of time delay). As we can see, jitter decreases when the pulse voltage increases. For 100 ns time delay the S-diodes based on GaAs:Fe and GaAs:Cr, Fe structures have 1.4 ns and 2 ns jitter, respectively. The diodes based on GaAs:Cr structures have 20 ns jitter at the same time delay.

Figure 3(a, b). (a) Dependences of the time delay on voltage; (b) Dependences of the jitter on voltage

Figure 4 shows dependence of jitter to time delay ratio ($j/d$ ratio) on triggering pulse voltage. The ratio characterizes relative switching stability and it can be used as a critical parameter for comparative analysis of different types of S-diodes. Obviously, to increase the stability, the time delay of switching should be decreased and the $j/d$ ratio should be a constant. However, in experiment the $j/d$ ratio decreases at low voltages and saturates. This fact can be explained by a change of switching delay mechanism: under saturation at high voltages we have single mechanism with constant $j/d$ ratio.

Figure 4. Dependences of $j/d$ ratio on triggering pulse voltage.
For application it is important to provide a lower $j/d$ ratio. The experiment shows that switching instability of S-diodes doped with iron is less by 14 times in comparison with diodes doped with Cr. Assuming a constant $j/t$ ratio we can estimate the jitter for different time delays. For example, at time delays of 1-10 ns the jitter should be 100-1000 ps for S-diodes doped with Cr (about 10 % of time delay). This values correspond to 17-170 ps standard deviation which are very close to rms jitter of GaAs:Fe high-gain photoconductive switches (14-96 ps [14-17]). In this regard, S-diode structures doped with iron (GaAs:Fe and GaAs:Fe, Cr) looks more promising because of lower jitter (about 1 % of time delay).

4. Conclusion
The experimental results of study of deep level type influence on switching time delay and jitter for S-diodes were presented. It was found that the switching time delay and jitter depend on triggering pulse voltage. As a critical parameter for comparative analysis of switching stability the jitter to time delay ratio ($j/d$ ratio) was proposed. In experiment, the $j/d$ ratio decreasing and saturation were found under triggering pulse voltage increase. Avalanche S-diodes doped with Fe and Cr/Fe impurities exhibit much better stability than diodes with Cr. Thus, S-diode structures doped with iron are more promising because of lower jitter which riches about 1% of time delay. Our future experimental work will be aimed at the study of $j/d$ ratio for a shorter time delays. Also, the physical mechanisms responsible for switching delay and stability of S-diodes doped with different deep levels will be investigated in our further work.

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