Development Status of Equipment Testability Verification Technology

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Abstract. Testability verification of equipment refers to the test and evaluation for testing whether the testability of equipment given by design and manufacture meets the specified testability requirements. Testability verification can lay a theoretical and technical foundation for the testability and maintainability transformation of active equipment, and provide a development platform for the development of equipment maintenance support equipment and system of grass-roots units. Its research work has very important military and economic significance for improving the overall level of information and intelligence of equipment and the security of use. This paper summarizes the development status of testability test and verification technology at home and abroad, analyses the key technologies of testability verification, and points out the key and difficult problems to be solved urgently at present. Finally, based on the comprehensive analysis of the current testability physical verification and non-physical verification technology schemes, some suggestions are given for further research and development of testability verification technology schemes.

1. Introduction
Testability refers to a design characteristic that equipment can determine its state (working, non-working or performance degradation) in time and accurately, and effectively isolate its internal faults [1]. With the application of various new technologies in weapons and equipment, the integration degree of equipment is getting higher and higher. The quality of testability level directly affects the support ability and combat effectiveness of equipment. Higher testability level can reduce equipment life cycle cost.

Testability verification refers to "the work for testing and developing products to meet the testability requirements stipulated in the contract"[2]. Testability verification test refers to the artificial injection of a certain number of faults into the equipment, fault detection and fault isolation through internal self-inspection or external testing equipment, and the conclusion of testability evaluation[3]. The tester evaluates the testability level of the unit under test according to the testability evaluation results, and decides whether to receive the developed equipment or not. As the key technology of testability verification test stage, fault injection technology has attracted the attention of researchers. In testability verification test[4], it is an important step before fault injection whether representative and cost-effective fault samples can be extracted. After selecting the fault samples, which method to distribute the samples can make the fault injection efficient and economical. It is necessary to study the fault injection methods of different units under test.

According to the requirement of testability verification, a certain number of faults need to be injected into the system under test, mainly in two ways: hardware injection and software injection. Hardware injection mainly involves injecting faults into the system through additional hardware
devices. Software injection mainly simulates the occurrence of hardware or software faults by changing the instruction system and data of software execution or modifying memory contents by presupposing fault programs in software.

2. Research Status of Testability Verification Test

From the point of view of life cycle, testability verification can be divided into three stages: testability design verification test in R&D stage, testability verification test based on fault injection in finalization stage, and testability field statistical verification test in use (trial) stage.

2.1. Testability Design Verification Test in R&D Stage

Testability verification test is a continuous analysis and evaluation work carried out by the contractor throughout the whole development process in order to achieve the testability requirements of equipment, and it is a part of equipment development test[5]. The purpose of testability verification is to identify design defects and take corrective measures through inspection, test and analysis and evaluation, and ultimately meet the requirements of testability design. The method of testability verification is flexible, and the data and basis of fault detection/isolation obtained from various analysis, simulation and test during the development process should be used to verify the testability design and analysis. At present, a lot of research on testability design verification test has been carried out at home and abroad. Shi Junyou[6] proposed an evaluation and verification method based on the data of the development stage. Shen Shenmu[7] proposed a method of estimating the system testability index based on the testability block diagram from the testability data of replaceable units. Qiu Jing[8] put forward the technical framework of testability virtual verification based on virtual prototype, pointed out the key technology and process of developing testability virtual verification, and pointed out that the related technology research of testability virtual verification is at the initial stage, which is an important direction of testability verification test development.

2.2. Testability Verification Test Based on Fault Injection in Finalization Stage

Testability verification test based on fault injection refers to "when equipment design is finalized, production is finalized or major design changes are made, that is, when equipment is injected with a certain number of faults in the laboratory or in the actual use environment, fault detection and isolation are carried out by the method prescribed by the testability design, the testability level of equipment is estimated according to the results, and whether the equipment meets the specified testability requirements is judged or not." Request, decide to accept or reject "[9]. The validation test in this stage is a very important link in the whole life cycle of equipment. The test data are used to verify the degree to which the equipment meets the requirements of testability design. In foreign literatures[10-12], whether for in-machine test (BIT) validation or automatic test equipment (ATE) validation, fault injection-based validation test method is mostly used. There have been many successful cases in testability verification test of weapon equipment abroad. For example, 1248 faults were injected into APG-66 radar system[13] for preliminary evaluation of effectiveness, and 150 faults were injected into formal test. APG-65 radar system[14] injects 302 faults in the initial evaluation of effectiveness, and at least 95 faults are required in the formal test. Testability verification of weaponry and equipment in China started relatively late. Only a few research institutes have carried out in-depth testability verification research systematically. The main target of this research is electronic products[15-18].

2.3. Testability Statistical Verification Test Based on Use Data in Outfield Use Stage

As a part of the weapon system series test, the testability field statistical verification of weapon equipment is attached great importance to by the US military because of the objective authenticity of its data[19]. C-17 is a new main transport aircraft developed by the U.S. Air Force. According to the requirements of the aircraft development contract, the U.S. Air Force conducted a 30-day reliability, maintainability and testability evaluation test. A total of 12 aircraft participated in the flight, flying for nearly 2200 hours. The design index value of the aircraft's Fault Detection Rate (FDR) is 0.95, the design index value of the Fault Isolation Rate (FIR) is 0.90, and the design index value of the false alarm rate is 0.05. The FDR test value obtained from the evaluation test is 0.99, the FIR test value is
0.95 and the false alarm rate test value is 0.60. The test results show that FDR and FIR are qualified, but the false alarm rate index does not meet the contract requirements. Because of military confidentiality, domestic experts have not collected any reports about the procedure and method of statistical verification of testable outfield.

3. Research Status of Fault Sample Selection Technology

The research results of fault sample selection technology are scattered, and the research at home and abroad is mainly carried out in the form of mathematical statistics. American and French scientific research institutes use normal distribution to determine confidence intervals, and use Bernoulli law of large numbers and central limit theorem to do early research on fault sample selection. Domestic researchers, including Tian Zhong and Zhou Yufen, have studied fault sample selection methods based on binomial distribution, which take into account FIR/FDR and other indicators. Other sample selection methods, including fault feature based method and adequacy criterion based method, are also preliminarily discussed. Xu Ping et al. proposed the corresponding sample selection method considering the fault feature model, Shi Junyou et al. proposed the test coverage adequacy criterion, and studied the method of determining the fault sample size [20].

In the process of sample selection, because of the correlation between samples, the correlation model can be used to model the fault propagation behavior to describe the relationship between fault samples. The correlation model uses directed graph to represent the direction of signal flow and the composition and connection relationship of each module[21]. Researchers generally use multi-signal flow graph model to study fault sample selection[22]. Researchers of National Defense University of Science and Technology combined multi-signal flow graph modeling with fuzzy probability to study fault propagation characteristics[23]; Li Guo and others studied system fault propagation model based on small world network[24]; Hunan University used cloud theory and potential function to obtain data potential field distribution map of fault propagation network, which accurately expressed fault propagation characteristics[25].

When analyzing circuit faults, it is necessary to conduct in-depth analysis of fault propagation. The common method is to construct fault propagation directed graph and establish correlation matrix by multi-signal flow graph method. However, it mainly focuses on static reasoning, because fault propagation in circuits is often a dynamic process, so it is necessary to study the dynamic propagation behavior of circuit faults. Using infectious disease model to study fault propagation behavior has become a new idea. Cellular automata (CA) models are widely used in the construction of epidemic transmission models and the prediction of epidemic trends. Yu Lei et al. used this model to simulate the transmission process of infectious diseases[26], and studied the transmission behavior of SARS virus; You Aili et al.[27] used cellular automata model to study infectious diseases in medicine. Wu Jimei, Bai Hui and Shao Shihuang proposed a functional fault propagation model for complex circuits. Cellular automata model was applied to circuit analysis to analyze the propagation behavior of circuit faults with added disturbances. However, this method did not fully consider the relationship between principal cells and neighbours [28].

When fault samples are selected, fault points need to be analyzed for sample allocation, and more stratified sampling based on fault rate is adopted. Although this method is scientific, the accuracy of fault rate information cannot be guaranteed. Li Tianmei[29] and others of National Defense University of Science and Technology proposed that prior information could be used to enhance the scientificity of the sampling method based on failure rate, and discussed the Gamma distribution fitting estimation method of failure rate based on prior expert data; Zhao Jianyang[30] and others proposed the sample allocation method adding the damage degree of failure mode, which is an improvement of the existing method; Deng Lu[31] and others proposed the basis. For testability verification test sample allocation method of fault attributes, this method is practical and integrates many factors to describe the fault. However, the above methods are still inaccurate in describing the characteristics of fault points.

In summary, the application of fault sample selection method has the following problems:

(1) When the test index or the evaluation precision are required to be high, the above-mentioned methods lead to a large number of fault samples. Because of encapsulation and other characteristics,
injection failures cannot be successfully carried out in many locations, so the test will not be carried out.

(2) Because of the inaccuracy of failure rate information in some equipment, the sample selection method based on failure rate needs to be improved. The phenomenon of fault propagation may lead to the failure of other units after injecting fault into the unit under test, which may affect other functions of the equipment under test. Therefore, it is necessary to study the fault propagation behavior.

(3) The randomness of sample selection leads to the difference of fault sample set. The method of sample allocation considering only fault rate information is not scientific, so the evaluation system of fault sample set should be improved. At the same time, the current situation of the project should be fully considered and the effectiveness of fault injection should be studied.

4. Research Status of Fault Injection Methods and Tools
The concept of fault injection was first proposed abroad in the 1970s, and has been used to study fault-tolerant systems. Since the mid-1980s, some research institutes have used fault injection technology to evaluate the fault-tolerant mechanism in the system[32]. With the passage of time, more and more researchers of measurement and control begin to pay attention to fault injection technology, and gradually develop the theory of fault injection. The International Year for Fault Tolerance has a panel devoted to the theory of fault injection, which has also been discussed and studied in various academic seminars. Internationally, whether BIT verification or ATE verification, the test verification method based on fault injection is mainly used[33]. With the deepening of fault injection theory, fault injection methods have been widely studied. Fault injection tools that meet the requirements of various tasks have been gradually put into scientific research. And good results have been achieved in the experiment.

4.1. Research Status Abroad
Gros used stratified sampling method to select fault models [34]; Alouani proposed the test method of maximum accelerated failure[35]; University of California, NASA and LAAS-CNRS of France and other universities and research departments of the United States studied fault injection more comprehensively[36]; Germany, Britain, Italy and other countries engaged in theoretical research work of fault injection more fully[37-38].

In summary, the related achievements of fault injection technology in various countries are summarized as follows: In terms of hardware fault injection tools, Messaline and RIFLE in France can inject pin-level faults based on probes and sockets for fixed faults, open-circuit faults and other logical faults[39], which has strong reference value; FIST tools in Sweden can inject faults into chips by generating signal flip. [40]; MARS can realize particle radiation fault and pin level fault injection [41].

4.2. Domestic Research Status
Domestic research on fault injection began in the 1980s. The Fault-Tolerant Computer Laboratory of Harbin University of Technology first studied fault injection[42]. Tsinghua University, Beijing University of Aeronautics and Astronautics, National Defense University of Science and Technology, various weapons research institutes and other departments have begun to study this field[43]. Fault syringes designed by Beihang and other institutions have been put into use, and some research results have been achieved[44]. In the existing application research, there are many fault injection methods in hardware implementation, which are mainly used for hardware fault injection through pin-level probe method, and software fault injection is mainly realized by modifying the contents of memory or registers[45].

In terms of fault injection tools, many explorations have been made in China. In the early stage, Harbin University of Technology developed a compulsory fault injection tool HFI-2[46], and connected the fixture to the injected chip to change the injection point current or voltage value, similar to today's post-drive fault injection. In recent years, some universities, such as National Defense University of Science and Technology, have begun to study fault injection tools[47]. The SWIFIARDS software developed by Chongqing University can inject various common faults such as memory faults[48]. Harbin University of Technology has developed a fault injection software for
evaluating the reliability of spaceborne systems: SFID is injected into the information data set by setting the fault location and other faults to achieve fault injection[49]. Gao Fengqi and others from the Ordnance Engineering College proposed a hardware-in-the-loop simulation fault injection system[50]. The system uses the TMS320C5416 series of DSP devices as the core device to control the fault injection[51]. Xuping designed a hardware-based fault injection system, which can realize bus-level fault injection and equipotential injection. Zhang Xiaojie designed a fault injection system which can realize short circuit and open circuit. Although there are few kinds of fault, it provides a design idea for later research[52]. Shi Junyou realized the hardware fault injection into the electronic equipment connection[53]. Engineer Huang Yongfei designed a device that can inject eight kinds of faults into J30 electrical connector[54]. Based on fault injection theory, Anglong Lee established a framework of fault injection assessment tool system, and accelerated the process of fault injection based on observation points and parallel methods. A RTL level fault injection tool is developed to enable it to be applied to the design of large scale integrated circuits[55].

In terms of fault injection methods, the implementation of fault injection based on physical implementation and simulation can be divided into two categories. The method based on simulation provides convenience for testing, but there are some drawbacks such as inaccurate model establishment, partial idealization of fault injection and low reliability of test results. In the physical implementation based fault injection method, the hardware fault injection method has strong controllability, high reliability, and is convenient for specific and instantaneous fault injection. Although the cost of software fault injection is low, the depth of fault injection is determined only according to the location of software arrival, and the final fault performance is mostly hardware fault.

5. Concluding Remarks
This paper summarizes the development status of equipment test and verification technology at home and abroad, and analyses the key technology of test and verification. The key and difficult problems that need to be solved urgently are pointed out in order to further promote the development of equipment testing and testing technology. Improve the technical level of equipment test and verification test, and provide reference support.

6. References
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