Loop stability analysis of boost circuit under globally dynamic compensation strategy

Xiaofan Wang1,2, Yingna Guo1,2, Weibin Cheng1,2, Mingquan Leng1,2
1 Shaanxi Key Laboratory of Measurement and Control Technology for Oil and Gas Wells, Xi’an, People’s Republic of China
2 MOE Key Laboratory of Photoelectricity Gas & Oil Logging and Detecting, Xi’an, People’s Republic of China
E-mail: 15114985248@163.com

Abstract: The PFC Boost converter controlled by the mode of CCM has strong non-linearity due to the use of non-linear elements such as power switch and multipliers. Here, a globally optimised control strategy of dynamic slope compensation is proposed to eliminate bifurcation, chaos behaviours. Time-varying adjustment of control efforts can achieve the optimal compensation intensity can be adjusted in real time in the whole power frequency cycle, so that the compensation voltage \( V_m = V_0 - V_i \) and ensure that the system has the strongest control efforts at any time. Finally, small-signal model of the peak current AC–DC Boost converter is derived and analysed to obtain the new equivalent power-level transfer function including the current loop. In order to compensate the current inner loop, the transfer function of the voltage outer loop is obtained, and the circuit simulation and experimental verification are carried out. The results show that globally dynamic compensation has good frequency domain response and application prospect (Table 1).

1 Introduction

The non-linear switchers and multipliers of AC-DC boost converters result in strong non-linear behaviours, such as fast time-scale bifurcation and chaos [1, 2]. Therefore, the fixed slope compensation strategy is proposed, the compensation voltage \( V_m > 0.5V_0 - V_i \) can ensure the stability of the circuit [3], although the fixed slope compensation expand the scope of the duty cycle, it results in the inductor current dead zone due to its constant compensation, which reduces the power factor and decreases the input power [4]. Aiming at the above insufficiency, a method of dynamic slope compensation control mode have been derived and the stability of the system is analysed from the frequency domain at the same time. The voltage outer loop is used to compensate the worst-stability zero-crossing time, which ensures that the circuit meets the frequency domain stability requirements throughout the whole cycle. Finally, the experimental circuit has been built to verify the theory, it can be found that the theory has good prospects in practical application and promotion through comparison between the simulation and the measured circuit waveforms.

2 Analysis of fixed slope compensation and globally dynamic compensation

2.1 Analysis of fixed slope compensation

Fig. 1 is AC–DC Boost circuit of peak current mode structure: The principle of fixed slope compensation strategy is to add a small ramp signal based on the reference current, so that the circuit can eliminate the fast time-scale bifurcation and other behaviours. From the diagram, we can see that the control loop is composed of current inner loop and voltage outer loop. The current inner loop is obtained by multiplying the gain of the voltage outer loop with the input voltage and multiplying a certain ratio coefficient. In this way, the peak value of inductance current tracks the input voltage waveform, and the control signal of MOSFET is generated by comparing the peak value of inductance current with the reference current. In order to eliminate the sub-harmonics oscillation of inductance current in the circuit, most scholars adopt the control strategy of fixed slope compensation. Fig. 2 is the curve of inductance current of fixed slope compensation:

\[
\begin{align*}
G_{o1} & = \frac{V_0}{D'} + \left( 2F_aV_0/D'R \right) + \left( F_aF_iV_0/D' \right) \\
\omega_L & = \frac{D'}{D'C} \left[ 1 + \frac{2F_aV_i}{D'R} + \frac{F_aF_iV_0}{D'} \right] \\
Q & = \frac{1}{D'C} \left[ 1 + \left( 2F_aV_0/D'R \right) + \left( F_aF_iV_0/D' \right) \right]
\end{align*}
\]

Table 1 Relevant parameters of equivalent power-level transfer function

| Parameter | Expression |
|-----------|------------|
| \( G_{o1} \) | \( \frac{V_0}{D'} + \left( 2F_aV_0/D'R \right) + \left( F_aF_iV_0/D' \right) \) |
| \( \omega_L \) | \( \frac{D'}{D'C} \left[ 1 + \frac{2F_aV_i}{D'R} + \frac{F_aF_iV_0}{D'} \right] \) |
| \( Q \) | \( \frac{1}{D'C} \left[ 1 + \left( 2F_aV_0/D'R \right) + \left( F_aF_iV_0/D' \right) \right] \) |

Fig. 1 AC–DC Boost circuit of PCM structure diagram

Fig. 2 Curve of inductance current of fixed slope compensation
The inductance current diagram of globally dynamic compensation can be expressed as:

\[ i_{\text{ref}}(t) - f_i \int^t_0 m_i \, dt \]

The average inductance current for each switching period may be expressed as:

\[ i_{av} = i_n + \frac{1}{2} m_c D_n T = \frac{\sqrt{2} I_r \sin 2 \pi t}{T_0} - mD_n T \]

It is easy to see that the fixed slope compensation strategy reduces the average value of inductance current \( i_{av} \), the input current deviates from the input voltage waveform and occurs the dead zone from the above formula. At the same time, the input power is reduced to a certain extent.

2.2 Analysis of globally dynamic compensation

When \( V_m > 0.5 V_o - V_i \) and \( V_m \neq V_o - V_i \), the disturbance of the current can be eliminated after several periods; when \( V_m = V_o - V_i \), the disturbance error of the current can be eliminated in a switching period, the slope of compensation voltage is equal to that of inductance current, and the system has the strongest control efforts [5, 6].

In order to overcome the shortcoming of fixed slope compensation, the reference current \( i_{\text{ref}} \) is considered as the disturbance object, the average value of inductance current is equal to the rated input current, the value of the reference current \( i_{\text{ref}} \) is calculated by reverse derivation; at the same time, it is in the real-time adjustment of the slope compensation voltage during the whole frequency period, which makes the compensation voltage \( V_m = V_o - V_i \), the circuit can eliminate the disturbance error of inductor current in a switching cycle. Fig. 3 is the working curve of inductor current for dynamic optimisation slope compensation:

The relation between two adjacent sampling points of current from the inductor current diagram can be expressed as:

\[ \begin{align*}
  i_n &= IR_o - \int^t_0 m_i(t) \, dt - \int^t_0 m_c(t) \, dt \\
  i_{n+1} &= IR_o - \int^t_0 m_i(t) \, dt - \int^t_0 m_c(t) \, dt + \int^{t+D_T}_t m_d(t) \, dt
\end{align*} \]

In order to realise sinusoidal input current and ensure the circuit can work stably, the average inductance current is simplified as follows:

\[ i_{L(\text{ref})} = i_n + \frac{1}{T} \int^{t+D_T}_t i_i(t) \, dt \]

\[ = IR_o - \int^t_0 m_i(t) \, dt - \int^t_0 m_c(t) \, dt + \frac{1}{T} \int^{t+D_T}_0 i_i(t) \, dt \]

The Formula (5) can be concluded after linearisation of the inductance current rise and fall:

\[ i_{\text{ref}} = \sqrt{2} I_r \cdot \frac{\sin 2 \pi t}{T_0} \]

\[ = \frac{1}{T} \int^{t+D_T}_t \left( m_o(t) + \frac{V_o - 0.5 V_o(t)}{L} \cdot \frac{V_o - V_i(t)}{V_o} \cdot T \right) \, dt \]

Compared with the reference current expressions of global dynamic optimisation compensation and the fixed slope compensation, it is easy to find that the average of the reference current and the inductive current of the dynamic slope compensation are raised, which overcomes the shortcoming that the input current of the fixed slope compensation is reduced [7]. Most importantly, the compensation voltage adjusts the control efforts in real time according to input voltage (Fig. 4). The slope of compensation voltage is equal to the slope of inductance current drop in each switching cycle, which can eliminate the disturbance error in one switching cycle. The stability of the system is improved.

3 Small signal modelling analysis and loop design

The current inner loop of PCM is stable after adding the slope signal, the new equivalent power level circuit is formed, which is constituted by the current inner loop and Boost main power circuit. The reasonable voltage outer loop is designed to meet the requirement of restraining output voltage fluctuation, transient response and output resistance. The block diagram of AC-DC Boost circuit of PCM is as follows:

The establishment of AC small-signal model is the basis of the design of outer loop voltage [8]. The influence of inductance current ripple and slope compensation should be taken into account in the derivation of the transfer function of current inner loop. The

![Fig. 3 Inductor current diagram of globally dynamic compensation](http://creativecommons.org/licenses/by/3.0/)

![Fig. 4 AC-DC Boost circuit system block diagram of PCM](http://creativecommons.org/licenses/by/3.0/)
average inductance current $i_{s\omega}$ and omitting high-order terms, then the $d(t)$ can be simplified as:

$$
\hat{d}(t) = \frac{1}{m_cF_1}\left[\hat{i}_{r\omega}(t) - \dot{i}_L(t) - \frac{D^2T_s}{2}\dot{m_c}(t) - \frac{D^2T_s}{2}\dot{m}_d(t)\right]
$$

Considering the expressions of charging slope $\dot{m}_c$ and discharging slope $\dot{m}_d$ and $\dot{m}_n$, the above formula can be simplified as:

$$
\hat{d}(t) = F_m[-\ddot{t}(t) - F\dot{v}(t) - F\ddot{v}]
$$

The parameters in the formula are expressed as $F_m = (1/M_cT_s)$, $F = ((4D - 1)T_s)/2L$, $F_m = ((D^2 - 2D)T_s)/2L$.

The expression between the duty cycle perturbation expression and other disturbances is obtained, and then combining the duty cycle perturbation expression with the traditional power Boost circuit transfer function, finally, the new expression of equivalent power level can be obtained. The frequency domain transfer function of traditional equivalent power level circuit is as follows:

$$
\dot{i}_L(s) = G_{ad}(s)\dot{d}(s) + G_{vd}(s)
$$

$$
\tilde{v}_e(s) = G_{ad}(s)d(s) + G_{vd}(s)
$$

The four parameters $G_{ad}G_{vd}G_{vd}G_{vd}$ are given in [9] and they are no longer listed in detail here.

The new equivalent power-level transfer function based on $\dot{d}(t)$ and the traditional power-level transfer function. The expression is as follows:

$$
G_{nt} = \frac{\hat{v}}{\dot{d}} = \frac{F_mG_{ad}}{1 + F_mG_{ad} + F_mF_Gd} = G_m\left(1 - \frac{s(1/D^2R)}{1 + (s/L\omega_n^2) + (s/\omega_n)}\right)
$$

Where the parameters are expressed in the Table 1.

The transfer function of the equivalent power level has been concluded, the design of the voltage outer loop is connected with circuit parameters and the Boost circuit is designed. The main parameters in the circuit are as follows (Table 2).

The input voltage of AC–DC Boost circuit rises from zero to peak value and then decreases to zero after the rectifier bridge. The voltage changes periodically. Finally, the transfer function of the voltage outer loop is designed to compensate the current inner loop, and the experimental circuit is guided theoretically.

The expression can be obtained by simplifying it with the substitution value:

$$
P = 1 + F_mG_d + F_mF_Gd
$$

$$
Q_e = D^2R^2\sqrt{\frac{C}{L}}\left(1 + (RCP_mV_o/4L) - (F_m/F_mV_o/4D^2)\right)
$$

The functional image of $Q_e$ changing with the duty cycle during the entire cycle was given as shown in the following figure (Fig. 6):

**Table 2** Circuit design parameters

| Parameters | Value |
|------------|-------|
| input voltage | AC220V |
| output voltage | DC400V |
| switching frequency | 50 kHz |
| inductance | 2 mH |
| resistive load | 400 Ω |
| capacitance | 470 µF |
| output power | 400 W |
It is easily found that the value of $Q_c$ over the entire range of the duty cycle variation is about 0.01. In the reference [10], it is proposed that the equivalent power-level transfer function can be written in the following form when $Q_c \ll 0.5$ and the calculation method of zero pole is given:

$$G_c(s) = \frac{G_{vc}(1 - s/\omega_z)}{(1 + s/\omega_p_c)(1 + s/\omega_p)}$$  \hspace{1cm} (16)

The function relation between zero pole and duty cycle was derived, the curve of zero pole with duty cycle is drawn (Fig. 7).

It is found that the of the high-frequency pole and the zero point of right plane decreases gradually during the input voltage from peak to zero, and the difference between the two frequency values is decreasing. The phase delay of the system is very large, and the phase margin is too small when the input voltage is close to zero, which can induce unstable phenomenon. The worst stability of the system must be compensated so that the whole duty cycle can meet the requirements of frequency domain response.

It can be calculated that $f_{p_1} = 1.5 \text{ Hz}$, $f_{p_2} = 8.5 \text{ kHz}$, $f_{c} = 80 \text{ Hz}$, $G_{vc} = 11$ when the input voltage is close to zero. So the outer loop voltage should be designed to offset the right half plane zero point, a single pole compensation network is designed:

$$G_V = K_V\left(\frac{1}{(1 + (s/\omega_v))}\right)$$  \hspace{1cm} (20)

The open loop transfer function of the circuit is described as:

$$T_{bf} = G_c(jf)G_V(jf) = \frac{K_V G_{vc}(1 - j(1/f_c))}{(1 + j(f/f_{p_1}))(1 + j(f/f_{p_2}))(1 + j(f/f_{p_3}))}$$  \hspace{1cm} (21)

Phase margin

$$\varphi_m = 180^\circ - \arctan\frac{f}{f_{p_1}} - 2\arctan\frac{f}{f_{c}} - \arctan\frac{f}{f_{p_2}}$$  \hspace{1cm} (22)

Then, the location of the crossing frequency need to be determined, in order to ensure the stability of the system, the following two conditions need to be satisfied when $f = f_c$:

$$\varphi_m = 80^\circ - \arctan\frac{f}{f_{p_1}} - 2\arctan\frac{f}{f_{c}} - \arctan\frac{f}{f_{p_2}} \geq 45^\circ$$  \hspace{1cm} (23)

Finally, the crossing frequency $f_c$ and the gain $K_V$ can be calculated as $f_c = 35 \text{ Hz}$, $K_V = 2.12$. The compensated system transfer function is simulated by Mathcad software. The simulation results are as follows:

Measuring the Bode diagram, the phase margin is $46^\circ$ and the amplitude gain is equal to 1 at the crossing frequency. It meets the frequency response requirement, because the duty cycle is 0.95, which is the time of maximum phase delay of the system. Therefore, the response bandwidth is lost. So the other values of duty cycle are verified, the amplitude margin, gain and frequency response bandwidth are greatly improved, so the voltage outer loop compensation design can meet the requirements of frequency response (Fig. 8).

### 4 Simulation and experimental verification

#### 4.1 Simulation verification

In order to verify the stability of the globally dynamic compensation theory under the voltage outer loop compensation, a simulation circuit is built in Matlab software. The following are the simulation results:

It is found that the zero current dead zone is eliminated and the power factor is improved under globally dynamic compensation.
strategy. At the same time, the compensation voltage is adjusted in real time with the input voltage and the compensation voltage slope is consistent with the inductor current discharging slope in each switching period, which ensures the elimination of error disturbance in a switching period (Fig. 9).

5 Conclusion

The experimental results show that the dynamic compensation adjusts the compensation intensity in real time to raise the reference current and eliminate the zero-current dead zone and improve the power factor compared with fixed slope compensation, the circuit compensated by the voltage outer loop has strong stability and anti-interference ability in frequency domain and the boost circuit has strong stability in time domain and frequency domain. Therefore, the compensation method for boost converters has good application prospects in the future.

6 Acknowledgments

[1] Natural Science Basic Research Plan in Shaanxi Province of China (2016GY-059).
[2] Research Project of key Laboratory of Education Department of Shaanxi Province (15JS083).
[3] Postgraduate Innovation Fund Project (YCS17112032).

7 References

[1] Orabi, M., Ninomiya, T.: ‘Nonlinear dynamics and stability analysis of boost power factor correction converter’, IEEE Trans. Ind. Electron., 2003, 50, (6), pp. 1116–1125
[2] Tse, C.K.: ‘Flip bifurcation and chaos in three-state boost switching regulators’, IEEE Trans. Circuits Syst., 1994, 41, (1), pp. 16–23
[3] Yidi, Y., Lu, W., Lu, H.H.C., et al.: ‘Stabilization of fast-scale instabilities in PCM boost PFC converter with dynamic slope compensation’. IEEE Int. Symp. on Circuits and Systems, Lisbon, Portugal, July 2005, pp. 2481–2484
[4] Lu, W., Lang, S., Zhou, L.: ‘Improvement of stability and power factor in PCM controlled boost PFC converter with hybrid dynamic compensation’, IEEE Trans. Circuits Syst., 2015, 62, (1), pp. 320–328
[5] Cheng, W., Song, J., Li, H., et al.: ‘Time-varying compensation for peak current control PFC boost converter’, IEEE Trans. Power Electron., 2015, 30, (6), pp. 3431–3437
[6] Prakash, K.S., Barai, M.: ‘Time-variant slope compensation for peak current mode control of boost converter with point-of-load applications’. 2016 IEEE 6th Int. Conf. on Power Systems, New Delhi, India, October 2016
[7] Weinbin, C., Guo, Y., Tang, N.: ‘Parameter sine perturbation adjustment and stabilization of wide input boost circuits’, Acta Phys. Sin., 2012, 59, (5), pp. 3035–3042
[8] Song, B.-M., Abedi, M.R.: ‘Dynamic modeling and performance of a current-mode controlled boost DC-DC converter with slope compensation’. IEEE Transportation Electrification Conf. and Expo, ITEC, Pearborn, USA, 2012
[9] Zhang, W.: ‘Modeling and control of switching converter’ (China Power Press, Beijing, 2006, 1st edn.), pp. 190–220
[10] Xu, D.: ‘Modeling and control of power electronics system’ (Machine Press, Beijing, 2006, 1st edn.), pp. 67–94