Development of timing synchronization system for Hyper-Kamiokande

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Abstract. Hyper-Kamiokande (HK) is a next generation neutrino detector, planned to start operation in 2027. Its main physics goals include precise measurements of neutrino oscillation parameters and investigations of the Grand Unified Theories. HK is an underground water Cherenkov detector, with a 68 m diameter and 71 m height cylindrical tank –approximately 8 times larger fiducial volume than Super-Kamiokande. It will be equipped with about 53,000 photo-sensors. Its front-end electronics is required to be synchronized with sub-ns precision, in order to ensure accurate timing measurements of the Cherenkov photons. We have developed a prototype system to distribute the synchronization clock with auxiliary information via optical fibers. In this paper, the design of the system, the descriptions of the developed prototype and finally the performance of the system are presented.

1. Introduction

Hyper-Kamiokande (HK) [1] is a next generation neutrino and a nucleon decay detector following Super-Kamiokande (SK) [2], operating from 1996, and aims at precise measurements of neutrino oscillation parameters and investigations of the Grand Unified Theories, which predict nucleon decay. It is a large underground water-Cherenkov detector, with a 68 m diameter and 71 m height cylindrical tank –approximately 8 times larger fiducial volume than SK, and equipped with about 53,000 photo-sensors. We plan to start construction of HK in 2020 and operation in 2027 and now are under the R&D phase of each the detector component.

We are newly developing many electronics components for HK. PMTs with 50 cm-diameter are improved from SK. The Water Cherenkov detectors use only the Cherenkov photons information from the surrounding PMTs on the wall, and the performances of the PMT, such as quantum efficiency and timing resolution, affect the performance of the detector. The new PMTs have about two times better quantum efficiency and timing resolution than that of SK, especially the time resolution is about 1 ns. Therefore, it is required for the electronics to maintain the new PMT’s properties in order to achieve better performance of HK. We are developing a timing synchronization system for HK. In this report, we show status of the developments of the timing system. First, we summarize requirements for the system and the design, and then show the performance of a prototype of the system implemented on a field programmable gate array (FPGA).
Figure 1. Left: the schematic design of the HK electronics, right: the conceptual design of the timing synchronization system. Blue (green) arrows show the flows of the MCLK (the serialized data) and brown arrows show the flows of the status of the FEs. The distributors also merge the status.

Table 1. Format of serialized information: A data of 0 bytes, 0 bits is sent first. MCNT:32 bit counter, ADDR:address of FE, ST:status of MCLK Gen., CMD:command, EXDATA:extension data, HEAD:length of the extension data ($n \leq 135$).

| BYTE  | 0   | 1 - 4 | 5 - 6 | 7 | 8 | 9 - $n$ | $n + 1$ |
|-------|-----|-------|-------|---|---|---------|--------|
|       | START | MCNT[31:0] | ADDR[15:0] | ST & CMD | HEAD | EXDATA | STOP |

2. Electronics of HK and requirements
Left of figure 1 shows the schematic design of the HK electronics, which consists of three parts: about 2,000 front-end electronics (FEs), a data acquisition system (DAQ) and the timing synchronization system. We plan to put all the FEs, which digitize PMT signals and supply high voltages to the PMTs, in the water tank in order to avoid attenuation and deterioration of the PMT signals due to the long length of the cable. The timing synchronization system distributes timing signals to the whole electronics and synchronizes them with the GPS clock. To preserve the timing resolution of the PMTs itself, timing resolution of the electronics should be less than 0.25 ns and it means the electronics should be synchronized with sub-ns. In addition, all the electronics in the water tank have to be reliable enough and free from failures. It is necessary to have high redundancy and is required to run over 10 years because we cannot replace them easily.

3. Schematic design
The timing system synchronizes all the FEs, about 2000 modules, with sub-ns precision to meet the requirements. The system generates the master timing signals and distributes it to all FEs. All the modules are synchronized to the reference and the relative phases between the boards do not change even after the reset or the power cycle of one of the boards. A conceptual design is based on that of SK and shown in right of figure 1. It consists of GPS receivers, an atomic clock, a master clock (MCLK) generator, distributors and its receivers in the FEs. The GPS and the atomic clock give an accurate and stable clock synchronized with the GPS time to the system. This is necessary for T2HK experiment, using HK as the far detector of T2K experiment [3], for neutrino oscillation physics.
The timing system uses two signal channels to transmit the timing information from the MCLK generator to the FEs. The UTP cables used in SK have a capability of maximal length of about 100 m, while optical fibers can communicate over 1 km. Therefore, we use optical fibers as signal lines because 100 m cable is not long enough for the large HK. We plan to install two fibers for the timing system. One fiber is used for the MCLK and another is used for a serialized counter, commands and other auxiliary data, whose contents are not fixed yet. There are a veto command for the calibration and a reset command for the digitizer. The MCLK generator serializes this information except for the MCLK into one signal channel as shown in table 1.

The MCLK generator (MCLKGen.) generates the 125 MHz MCLK from the atomic clock. The digitizer of HK will multiply the MCLK, run with a 4 GHz clock and achieve 0.25 ns timing resolution. The timing receiver block decodes the serialized counter etc. and delivers them to other blocks in the FE. It is required to run continuously without the MCLK even if supply of the MCLK is cut for remote maintenance, for example, during the shutdowns of the FEs.

4. Performance
We implemented a prototype of the master clock generator and the timing receiver in a FPGA on KC705, a commercially available FPGA evaluation board. Then, we confirmed the delivery of the MCLK and the serialized information and that the system works well and the prototype kept running for about two weeks. We also developed optical transceiver boards to evaluate optical modules which converts an electric signal to an optical signal and vice versa. Since the timing jitter of the MCLK affects the timing resolution of the whole system, we evaluated the jitter of the MCLK generated by the prototype and the jitter deterioration caused by the optical modules.

The prototype of KC705 outputs the MCLK through a SMA port as an electric clock signal. In the results of the evaluation, the period jitter of this SMA output was about $\Delta T_{RMS} \approx 8 \pm 10$ ps (RMS). When the MCLK was converted to the optical signal and re-converted to the electric signal again by the external board, the period jitter became about $\Delta T_{RMS} \approx 15 \pm 10$ ps. This is good enough for the requirement of sub-ns synchronization.

5. Summary and prospect
HK is now under the R&D phase of each the detector component towards the operation in 2027. New timing synchronization system is necessary for the HK electronics and the requirement for HK is tighter than SK especially in durability coming from the fact that the FEs are put in the water tank where we cannot access easily. We designed a prototype of the timing synchronization system and implemented to evaluate the conceptual design. We confirmed our design works as expected and has a capability to synchronize with sub-ns precision.

The system we implemented in this paper is a conceptual design and needs further developments, for example interfaces between the timing system and the digitization block and the redundancy and so on. We plan to connect the timing system with the digitization block of the FE and check that the timing resolution of the PMTs does not change due to the timing system. In addition, we are planning to add some functions, like monitoring the number of hit PMTs and the FE’s status and configurations of the FEs etc.

References
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