Tensor Network Quantum Simulator With Step-Dependent Parallelization

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Abstract—In this work, we present a new large-scale quantum circuit simulator. It is based on the tensor network contraction technique to represent quantum circuits. We propose a novel parallelization algorithm based on step-dependent slicing. In this paper, we push the requirement on the size of a quantum computer that will be needed to demonstrate the advantage of quantum computation with Quantum Approximate Optimization Algorithm (QAOA). We computed a single amplitude of QAOA ansatz state on 210 qubits. The simulation involved 1,785 gates on 1,024 nodes of the Cray XC 40 supercomputer Theta. To the best of our knowledge, this constitutes the largest simulation of QAOA ansatz simulations reported to this date.

Keywords: Quantum computing, quantum simulator, tensor network simulator, tensor slicing, high performance computing

I. INTRODUCTION

Simulations of quantum circuits on classical computers are essential for better understanding of how quantum computers operate, the optimization of their work, and the development of quantum algorithms. For example, simulators allow researchers to evaluate the complexity of new quantum algorithms and to develop and validate the design of new quantum circuits [1].

Many approaches have been proposed to simulate quantum circuits on classical computers. The major types of simulation techniques are full amplitude-vector evolution [2]–[5], the Feynman paths approach [6], linear algebra open system simulation [7], decision diagrams [8], and tensor network contractions [9]–[11].

Tensor network contraction simulators are exceptionally well suited for simulating short quantum circuits. The simulation of Quantum Approximate Optimization Algorithm (QAOA) [12] circuits is exceptionally efficient with this approach given how short the circuits are.

In this work, we used our tensor network simulator QTensor, which is an open-source project developed in Argonne National Laboratory. The source code and documentation are available at github:danlkv/QTensor. It is a quantum circuits simulator capable of simulating arbitrary quantum circuits. It also supports automatic differentiation with respect to gate parameters which is useful in the Quantum Machine Learning applications [13] and QAOA parameter optimization [14].

One major milestone in quantum computing science is Google’s simulations of random large quantum circuits [15]. The research interest of the community is now focused on providing an advantage of using quantum computers to solve real-world problems. QAOA is considered as a prime candidate to demonstrate such advantage. QAOA can be used to solve a wide range of hard combinatorial problems with a plethora of real-life applications, like the MaxCut problem, which is NP-complete. In this paper, we explored the limits of classical computing using a supercomputer to simulate large QAOA circuits, which in turn helps to define the requirements for a quantum computer to beat existing classical computers.

Our main contribution is the development of a novel tensor network parallelization algorithm, which interleaves tensor slicing and tensor contraction steps. Such approach was never described in previous work. This allowed us to increase the size of simulated circuits from 120 qubits to 210 qubits on a distributed computing system, while maintaining the same time-to-solution.

In Section II we start the paper by discussing related work. In Section IV we describe tensor networks and the bucket elimination algorithm. Simulations of a single amplitude of QAOA ansatz state are described in Section V. We introduce a novel approach step-dependent slicing to finding the slicing variables, inspired by the tensor network structure. Our algorithm allows simulating several amplitudes with little cost overhead, which is described in Section VII.

We then show the experimental results of our algorithm running on 64-1,024 nodes of Theta supercomputer located in Argonne National Laboratory. All these results are described in Section VIII. In Section IX we summarize our results and draw conclusions.

II. RELATED WORK

In recent years, much progress has been made in parallelizing state vector [3]–[5] and linear algebra simulators [7]. Very large quantum circuit simulations were performed on the most
powerful supercomputers in the world, such as Summit [16], Cori [4], Theta [5], and Sunway TaihuLight [17]. All these simulators have various advantages and disadvantages. Some of them are general-purpose simulators, while others are more geared toward short-depth circuits.

One of the most promising types of simulators is based on the tensor network contraction technique. This idea was introduced by Markov and Shi [9] and was later developed by Boixo et al. [18] and other authors [19]. Our simulator is based on representing quantum circuits as tensor networks.

Boixo et al. [18] proposed using the line graphs of the classical tensor networks, an approach that has multiple benefits. First, it establishes the connection of quantum circuits with probabilistic graphical models, allowing knowledge transfer between the fields. Second, these graphical models avoid the overhead of traditional diagrams for diagonal tensors. Third, the treewidth is shown to be a universal measure of complexity for these models. It links the complexity of quantum states to the well-studied problems in graph theory, a topic we hope to explore in future works. Fourth, straightforward parallelization of the simulator is possible, as demonstrated in the work of Schutzki et al. [19]. The approach has been studied in numerous efficient parallel simulations relevant to this work [10], [17], [19], [20].

III. METHODOLOGY

A. QAOA introduction

The combinatorial optimization algorithms aim at solving a number of important problems. The solution is represented by an $N$-bit binary string $z = z_1...z_N$. The goal is to determine a string that maximizes a given classical objective function $C(z) : \{+1, -1\}^N$. The QAOA goal is to find a string $z$ that achieves the desired approximation ratio:

$$\frac{C(z)}{C_{\text{max}}} \geq r$$

where $C_{\text{max}} = \max_{x \in \mathbb{Z}} C(z)$.

To solve such problems, QAOA was originally developed by Farhi et al. [21] in 2014. In this paper, QAOA has been applied to solve MaxCut problem. It was done by reformulating the classical objective function to quantum problem with replacing binary variables $z$ by quantum spin $\sigma^z$ resulting in the problem Hamiltonian $H_C$:

$$H_C = C(\sigma^z_1, \sigma^z_2, ... , \sigma^z_N)$$

After initialization of a quantum state $|\psi_0\rangle$, the $H_C$ and a mixing Hamiltonian $H_B$:

$$H_B = \sum_{j=1}^{N} \sigma^z_j$$

is then used as to evolve the initial state $p$ times. It results in the variational wavefunction, which is parametrized by $2p$ variational parameters $\beta$ and $\gamma$. The ansatz state obtained after $p$ layers of the QAOA is:

$$|\psi_p(\beta, \gamma)\rangle = \prod_{k=1}^{p} e^{-i\beta_k H_B} e^{-i\gamma_k H_C} |\psi_0\rangle$$

To compute the best possible QAOA solution corresponding to the best objective function value, we need to sample the probability distribution of $2^N$ measurement outcomes in state $|\gamma, \beta\rangle$. The noise in actual quantum computers hinders the accuracy of sampling, resulting in the need of even a larger number of measurements. At the same time, sampling is an expensive process that needs to be controlled. Only a targeted subset of amplitudes need to be computed because sampling all amplitudes will be very computationally expensive and memory footprint prohibitive. As a result, the ability of a simulator like QTensor to effectively sample certain amplitudes is a key advantage over other simulators.

The important conclusion Farhi et al. [21] paper was that to compute an expectation value, the complexity of the problem depends on the number of iterations $p$ rather than the size of the graph. This is a result of what is known as lightcone optimization. It has a major implication to the speed of a quantum simulator computing QAOA energy [22], but this type of optimization is not applicable for simulating ansatz state, which is the type of simulation we focus in this paper. A more detailed MaxCut formulation for QAOA was provided by Wang et al. [23]. It is worth mentioning that there is a direct relationship between QAOA and adiabatic quantum computing, meaning that QAOA is a Trotterized adiabatic quantum algorithm. As a result, for large $p$ both approaches are the same.
B. Description of quantum circuits

A classical application of QAOA for benchmarking and code development is to apply it to Max-Cut problem for random 3-regular graph. A representative circuit for a single-depth QAOA circuit for a fully connected graph with 4 nodes, is shown in Fig. 1. The generated circuit were converted to tensor networks as described in Section IV-A. The resulting tensor network for the circuit in 1 is shown in Fig. 3. Every vertex corresponds to an index of a tensor of the quantum gate. Indices are labeled right to left: 0 - 3 are indices of output statevector, and 32 - 25 are indices of output statevector. Self-loop edges are not shown (in particular $Z^{2^7}$, which is diagonal). We simulated one amplitude of state $|\gamma, \beta\rangle$ from the QAOA algorithm with depth $p = 1$, which is used to compute the energy function. The full energy function is defined by $\langle \gamma, \beta | C | \gamma, \beta \rangle$ and is essentially a duplicated tensor expression with a few additional gates from $C$. The full energy computation corresponds to the simulation of a single amplitude of such duplicated tensor expression.

IV. OVERVIEW OF SIMULATION ALGORITHM

In this section, we briefly introduce the reader to the tensor network contraction algorithm. It is described in much more detail in the paper by Boixo et al. [18], and the interested reader can refer to work by Detcher et al. [24] and Marsland et al. [25] to gain an understanding of this algorithm in the original context of probabilistic models.

A. Quantum circuit as tensor expression

A quantum circuit is a set of gates that operate on qubits. Each gate acts as a linear operator that is usually applied to a small subspace of the full space of states of the system. State vector $|\psi\rangle$ of a system contains probability amplitudes for every possible configuration of the system. A system that consists of $2^n$ two-state systems will have $2^n$ possible states and is usually represented by a vector from $C^{2^n}$.

However, when simulating action of local operators on large systems, it is more useful to represent state as a tensor from $(C^2)^{\otimes n}$. In tensor notation, an operator is represented as a tensor with input and output indices for each qubit it acts upon. The input indices are equated with output indices of previous operator. The resulting state is computed by summation over all joined indices. The comparison between Tensor Network notation and Dirac notation is shown in Table I.

Following tensor notations we drop the summation sign over any repeated indices, that is, $a_i b_j = \sum_i a_i b_j$. For more details on tensor expressions, see [26].

|                | Dirac notation | Tensor notation |
|----------------|----------------|----------------|
| general        | $|\psi\rangle = X_{i} \otimes I_{i} |\psi\rangle$ | $\phi_{i,j} = X_{i} |\psi\rangle$ |
| product state  | $|\psi\rangle = |a\rangle |b\rangle$ | $\psi_{i,j} = a_i b_j$ |
| with Bell state| $|\psi\rangle = X_{i} \otimes I_{i} (|00\rangle + |11\rangle)$ | $\phi_{i,j} = X_{i} |\delta_{i,j}$ |

TABLE I: Comparison between different notations of quantum circuits

Fig. 2: Correspondence of quantum gates and graphical representation.

Fig. 3: Graph representation of tensor expression of the circuit in Fig. 1. Every vertex corresponds to a tensor index of a quantum gate. Indices are labeled right to left: 0-3 are indices of output statevector, and 32-25 are indices of input statevector. Self-loop edges are not shown (in particular $Z^{2^7}$, which is diagonal).

B. Graph model of tensor expression

Evaluation of a tensor expression depends heavily on the order in which one picks indices to sum over [9], [27]. The most widely used representation of a tensor expression is a “tensor network,” where vertices stand for tensors and tensor indices stand for edges. For finding the best order of contraction for the expression, we use a line graph representation of a tensor network. In this notation, we use vertices to denote unique indices, and we denote tensors by cliques (fully connected subgraphs). Note that tensors, which are diagonal along some of the axes and hence can be indexed with fewer indices, are depicted by cliques that are smaller than the dimension of the corresponding tensor. This results in a substantial simplification of the tensor network as described in detail in [28]. For a special case of vectors or diagonal matrices, self-loop edges are used. Figure 2 shows the notation for the gates...
used in this work. For a more detailed description of graph representation, see [27].

Having built this representation, one has to determine the index elimination order. The tensor network is contracted by sequential elimination of its indices. The tensor after each index elimination will be indexed by a union of sets of indices of tensors in the contraction operation. In the line graph representation, the index contraction removes the corresponding vertices from the graph. Adding the intermediate tensor afterwards corresponds to adding a clique to all neighbors of index $i$. We call this step elimination of vertex (index) $i$. An interactive demo of this process can be found at https://lykov.tech/qg (works for cZ\_v2 circuits from “Files to use”— link).

The memory and time required for the new tensor after elimination of a vertex $v$ from $G$ depends exponentially on the number of its neighbors $N_G(v)$. Figure 4 shows the dependence of the elimination cost with respect to the number of vertices (steps) of a typical QAOA quantum circuit. The inset also shows for comparison the number of neighbors for every vertex at the elimination step.

Note that the majority of contraction is very cheap, which corresponds to the low-degree nodes from Figure 3. This observation serves as a basis for our step-dependent slicing algorithm.

The main factor that determines the computation cost is the maximum $N_G(v)$ throughout the process of sequential elimination of vertices. In other words, for the computation cost $C$ the following is true:

$$C \propto 2^c; c \equiv \max_{i=1\ldots N} N_G(v_i),$$

where $G_i$ is obtained by contracting $i-1$ vertices and $c$ is referred to as the contraction width. We later use shorter notation for the number of neighbors $N_i(v) \equiv N_G(v_i)$.

The problem of finding a path of graph vertex elimination that minimizes $c$ is connected to finding the tree decomposition. In fact, the treewidth of the expression graph is equal to $c - 1$. Tree decomposition is NP-hard for general graphs [29], and a similar hardness result is known for the optimal tensor contraction problem [30]. However, several exact and approximate algorithms for tree decomposition were developed in graph theory literature; for references, see [29], [31]–[34].

V. SIMULATION OF A SINGLE AMPLITUDE

The simulation of a single amplitude is a simple benchmark to use to evaluate the complexity of quantum circuits and simulation performance. We start with $N$-qubit zero state $|0^\otimes N\rangle$ and calculate a probability to measure the same state.

$$\sigma = \langle 0^\otimes N | \hat{U} | 0^\otimes N \rangle = \langle \vec{\gamma}, \vec{\beta} | 0^\otimes N \rangle$$

A. Ordering algorithm

The ordering algorithm is a dominating part of efficient tensor network contraction. Linear improvement in contraction width results in an exponential speedup of contraction.

There are several ordering algorithms that we use in our simulations. The major criterion to choose one is to maintain a balance between ordering improvement and run time of the algorithm itself.

1) Greedy algorithm: The greedy algorithm contracts the lowest-degree vertex in the graph. This algorithm is commonly used as a baseline since it provides a reasonable result given a short run-time budget.

2) Randomized greedy algorithm: The contraction width is very sensitive to small changes in the contraction order. Gray and Kourtis [35] used this fact in a randomized ordering algorithm, which provided contraction width improvement without prolonging the run time. We use a similar approach in the rgreedy algorithm. Instead of choosing the smallest-
degree vertex, \( r\text{greedy} \) assigns probabilities for each vertex using Boltzmann’s distribution:

\[
p(v) = e^{\exp(-\frac{1}{\tau}N_G(v))}
\]

The contraction is then repeated \( q \) times, and the best ordering is selected. The \( \tau \) and \( q \) parameters are specified after the name of the \( r\text{greedy} \) algorithm.

3) Heuristic solvers: The attempt to use some global information in the ordering problem gives rise to several heuristic algorithms.

Tamaki’s heuristic solver [36] is a dynamic programming approach that provides great results. This is also an “anytime” algorithm, meaning that it provides a solution after it is stopped at any time. The improvements from this algorithm are noticeable when it runs from tens of seconds to minutes. We denote time (in seconds) allocated to this ordering algorithm after its name.

VI. PARALLELIZATION ALGORITHM

We use a two-level parallelization architecture to couple the simulation structure and hardware constraints. Our approach is shown at Fig. 6. Multinode-level parallelization uses MPI to share tasks. We slice the partially contracted full expression over \( n \) indexes and distribute the slices to \( 2^n \) MPI ranks. We use a novel algorithm for determining the slice vertex and step at which to perform slicing, which results in massive expression simplification. This is described in Section VI-C. A high-level picture of our algorithm is shown in Fig. 7.

Node-level parallelisation over CPU cores uses system threads. For every tensor multiplication and summation we slice the input and output tensors over \( t \) indices. Contraction is then performed by \( 2^t \) threads writing results to a shared result tensor. This process is described in Section VI-B.

To illustrate the two approaches used, we consider a simple expression \( C_i = A_{ij}B_j \). There are two obvious ways of parallelization:

1) Parallelization over elements of sum, index \( j \). Every worker computes its version of \( C_i \) for some value of \( j \), and the results then are summed.
2) Parallelization over the indices of the result, \( i \). Every worker computes part of the result, \( C_i \), for some value of \( i \).

These two options are intrinsically similar: every worker is assigned a simplified version of the expression, which is obtained by applying a slicing operation over some indices to every tensor. The difference between the two is that while performing computation using the first option, one must store copies of the result for every worker, which results in higher memory usage that scales linearly with the number of workers. This is not an issue in the second option, where different workers write to different parts of the shared result. The second option is less flexible, however. Usually one has a complex expression on the right-hand side, and the result has a smaller number of dimensions. The crucial part is that one can reduce treewidth of a complex expression using parallelization, which is discussed in Section VI-C.

A. Description of hardware and software

The benchmarks reported in this paper were performed on the Intel Xeon Phi HPC systems in the Joint Laboratory for System Evaluation (JLSE) and the Theta supercomputer at the Argonne Leadership Computing Facility (ALCF) [37]. Theta is an 12-petaflop Cray XC40 supercomputer consisting of 4,392 Intel Xeon Phi 7230 processors. Hardware details for the JLSE and Theta HPC systems are shown in Table II.

The Intel Xeon Phi processors used in this work have 64 cores. The cores operate at 1.3 GHz frequency. Besides the L1 and L2 caches, all the cores in the Intel Xeon Phi processors share 16 GB of MCDRAM (another name is High Bandwidth Memory) and 192 GB of DDR4 memory. The bandwidth of MCDRAM is approximately 400 GBytes/s, while the bandwidth of DDR4 is approximately 100 GBytes/s.

The memory on Xeon Phi processors can be configured in the following modes: flat mode, cache mode, and hybrid mode. In the flat mode, the two levels of memory are treated as separate entities. One can run entirely in MCDRAM or entirely in DDR4 memory. In the cache mode, the MCDRAM is treated as a direct-mapped L3 cache to the DDR4 layer. In the hybrid mode, a part of the MCDRAM is L3 cache and the rest is directly addressable fast MCDRAM, but it does not become part of the (lower bandwidth) DDR4 memory.

Besides memory modes, the Intel Xeon Phi processors support five cluster modes: all-to-all, quadrant/hemisphere, and sub-NUMA cluster SNC-4/SNC-2 modes of cache operation. The main idea behind these modes is how to optimally maintain cache coherency depending on data locality.

For the types of problems we are computing here, there is not much difference between various memory configurations [38]. In the calculations presented in this paper, we used the quadrant clustering mode for all quantum circuit simulations on Intel Xeon Phi nodes. We explored the use of different

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### TABLE II: Hardware and software specifications

| Intel Xeon Phi node characteristics |  
|------------------------------------|---|
| Intel Xeon Phi models              | 7210 and 7230 (64 cores, 1.3 GHz, 2.622 GFLOPs) |
| Memory per node                    | 16 GB MCDRAM, 192 GB DDR4 RAM |

| JLSE Xeon Phi cluster (26.2 TFLOPS peak) |  
|-----------------------------------------|---|
| # of Intel Xeon Phi nodes              | 10 |
| Interconnect type                      | Intel Omni-Path™ |

| Theta supercomputer (11.69 TFLOPS peak) |
|----------------------------------------|
| # of Intel Xeon Phi nodes              | 4,392 |
| Interconnect type                      | Aries interconnect with Dragonfly topology |
| Cray environment loaded modules        | PrgEnv-intel/ 6.0.5, intel/ 19.0.5.281, cray-mppich/ 7.7.10 |
affinity modes and found that there is not much difference in performance between them. For our benchmarks, we used the default affinity, which is set to scatter.

B. Single-node parallelization

Simulation of quantum circuits is an example of a memory-bound task: the main bottleneck of simulation is the storage of intermediate results of a simulation. In a simplistic approach called the state-vector evolution scheme, the full vector of size $2^n$ is stored in memory. Thus a circuit containing only 300 qubits will require more memory than there are atoms in the universe. A much more efficient algorithm is the tensor network contraction algorithm described here. But as we show below, it requires use of a complicated parallelization scheme compared with the straightforward linear algebra parallelization scheme used in the state-vector simulators.

Modern high-performance computing (HPC) systems have nodes with a large number of CPU cores. An efficient calculation has to utilize all available CPU cores, using many threads to execute code. The major problem in using MPI-only code is that all of the data structures are replicated across MPI ranks, which results in increased memory usage linearly with respect to the number of MPI ranks. The largest data object in our simulation is the tensor, which is a result of the contraction step. Memory requirements to store such tensor are exponential with respect to its size.

Moreover, every code will inevitably have a part that can be executed only serially. As the number of OpenMP threads or MPI increases, the parallelization becomes less efficient according to Amdahl’s law. Thus, following this logic, smaller computations require less time, and the portion of the program that benefits from parallelization will be smaller for small tensors. As a result, according to Amdahl’s law, this means that for small tensors, we need to use fewer threads.

To address these problems, we share the resulting tensor between $2^t$ threads. We also use an adaptive thread count determined from task size (Eq. 1). A usual approach of splitting matrices in the code is to split into $2^t$ rows, or columns. This approach is not applicable in our case since tensors have size 2 over each dimension, and it would require reshaping the tensor, so it would be indexed with a multi-index. We choose a similar but more elegant approach. To slice into $2^t$ parts, we first choose indices that will be our slice dimensions. The slicing operation fixes the value of the index and reduces the number of dimensions by one. We then use a binary form of the thread index (the id of the thread) as a point in space $\{0, 1\}^{2^t}$ that defines the slice index values.

Every contraction in the bucket elimination step can be represented by the permutation of indices as

$$C_{ijk} = A_{ij} B_{ik}$$

where index $i$ contains indices that $A$ and $B$ have in common and $j, k$ contain indices specific to $A, B$, respectively. For our simulation, we slice the tensor over the first $t$ indexes of the resulting tensor because this approach results in consistent blocks of resulting tensors assigned to each thread, thereby reducing the memory access time. This part of the algorithm is shown in green in Fig 7.

To determine an optimal number of threads to use, we run a series of experiments to estimate the overhead time. We use these experimental results as the basis for an empirical formula for optimal thread count:

$$t = \max(\lfloor \frac{r - 22}{2}\rfloor, 1),$$

where $r$ is rank of the resulting tensor.

C. Multinode parallelization

Every computational node has RAM and a pool of CPU cores. Parallelization over nodes (compared with threads) increases the size of aggregated distributed memory. Thus storing duplicates of tensors is not an issue. For this reason, we use every node to compute a version of a tensor expression evaluated at some values of the tensor indices.

In graph representation, the contraction of the full expression is done by consecutive elimination of graph vertices. The elimination of a vertex removes it from the graph and connects all neighbors. An interactive demo of this process can be found at https://lykov.tech/qg (works for $cZ_2$ circuits from “Files to use”— link).

The slice of a tensor over an index can be viewed as the function of many variables evaluated at some value of one variable

$$f(x_1, x_2, \ldots, x_n)|_{x_1=a} = \tilde{f}(x_2, \ldots, x_n),$$

where variables can have integer values $v_i \in [0, d-1]$. Slicing reduces the number of indices of the tensor by one. Moreover, in graph representation, this operation results in the removal of the corresponding vertex from the expression graph. Since all sizes of indices we use are equal to 2, removal of $n$ vertices allows us to split the expression into $2^n$ parts.

This operation is equivalent to decomposition of the full expression into the following form:

$$\sum_{m_1 \ldots m_n} \left( \sum_{V \setminus \{m_i\}} T^1 T^2 \ldots T^N \right),$$

where $m_i$ are indices that we slice over and the parts of the expression correspond to the expression in parentheses.

Each part is represented by a graph with lower connectivity than the original one. This dramatically affects the often sub-optimal elimination path and, respectively, the cost of contraction. Depending on the expression, we observed that using only two computational nodes can allow for speedups of an order of $2^t$.

D. Step-dependent slicing

The QAOA circuit tensor expression results in a graph that has many low-degree vertices, as demonstrated in Fig. 3 for a small circuit. As can be seen in Fig. 4, most contraction steps
are computationally cheap, and the connectivity of a graph is low.

Each partially-contracted tensor network is a perfectly valid tensor network and can be sliced as well. From a line graph representation perspective, vertices can be removed at any step of contraction, giving rise to a completely new problem of finding an optimal step for slicing the expression. We propose a step-dependent slicing algorithm that uses this fact and determines the best index to perform slicing operation, shown in Fig. 8.

We start with finding the ordering for the full graph. Our algorithm then selects consideration only those steps that come before the peak. For every such contraction step \( s \), we remove \( r \) vertices with the biggest number of neighbors from the graph and re-run the ordering algorithm to determine the contraction after slicing. The distribution of contraction width is shown on Fig. 11.

The step \( s \) at which slicing produces best contraction width and contraction order before that is then added to a contraction schedule. This process can be repeated several times until \( n \) indices in total are selected - each \( r \) of them having their optimal step \( s \). This algorithm requires \( \frac{n}{r}N \) runs of an ordering algorithm, where \( N \) is the number of nodes in the graph, which is usually of the order of 1000. Only greedy algorithms are used in this procedure due to its short run time.

The value of \( r \) can be used to slightly tweak the quality of the results. If \( r = n \), all the \( n \) variables are sliced at a single step. If \( r = 1 \), each slice variable can have its own slice step \( s \), which gives better results for larger \( n \).

We observed that using \( n = 1 \) already provides contraction width reduction by 3, which converts to 8x speedup in simulation.

To the best of our knowledge, this approach of step-dependent parallelization was never described in previous work of this field.

In the first part of the full simulation, labeled (a) in Figure 7, we read the circuit, create the expression graph, find the elimination order, and form buckets. We also find the best parallelization step \( s \) and the corresponding index used in the parallel bucket elimination. The simulation starts with contracting the first \( s \) buckets, which is computationally cheap. After this we have some other tensor expression network, which also is represented by a partially contracted graph. This expression is conceptually no different from the one we started with; however, its graph representation has much higher connectivity.
1. Generate circuit graph
2. Find elimination order
3. Find optimal parallelization index s
4. Form buckets

(a) Simulate first s buckets
1. Find optimal parallelization vertices
2. Remove vertices
3. Find new elimination order
4. Slice remaining buckets

(b) For every remaining bucket B
   - R = B[0]
   - For every tensor T in B[1:]
     - rank r higher than 22?
       - Yes: Q = shared_tensor()
         - t = (r-22)/2 threads
         - Slice(Q) = Slice(R)*Slice(T)
       - No: R = R*T
   - Finished bucket?

No buckets left

Fig. 7: Sketch of the parallel bucket elimination algorithm. Part (a) and steps b2–b4 depend only on the structure of a task and can be executed only once for the QAOA algorithm. Steps b1 and b5 are performed serially. The outer loop of the blue region performs the elimination of the remaining buckets; the inner loop corresponds to processing a single bucket. The summation operation at the end of the bucket processing is omitted for simplicity.

VII. SIMULATION OF SEVERAL AMPLITUDES

The QAOA algorithm in its quantum part requires sampling of bit-strings that are potential solutions to a Max-Cut problem. It is possible to emulate sampling on a classical computer without calculating all the probability amplitudes. To obtain such samples, one can use frugal rejection sampling [39] which requires calculating several amplitudes.

Our tensor network approach can be extended to simulate a batch of variables. If we contract all indices of a tensor network, the result will be scalar - a probability amplitude. If we decide to leave out some indices, the result will be a tensor indexed by those indices.

This tensor corresponds to a clique on left-out indices. If a graph contains a clique of size a, its treewidth is not smaller...
than \( a \). And if we found a contraction order with contraction width \( c \), during the contraction procedure we will have a clique of size \( c \). If \( a < c \) then adding a clique to the original graph does not increase contraction width. This opens a possibility to simulate a batch of \( 2^a \) amplitudes for the same cost as a single amplitude. This is discussed in great detail in [19].

Figure 9 shows contraction width for simulation of batch of amplitudes for different values of \( a \), ordering algorithms and graph sizes.

VIII. RESULTS

We used the Argonne’s Cray XC40 supercomputer called Theta that consists of 4,392 computational nodes. Each node has 64 Intel Xeon Phi cores and 208 GB of RAM. The combined computational power of this supercomputer is about 12 PFLOP/sec. The aggregated amount of RAM across nodes is approximately 900,000 GB.

For our main test case, a circuit with 210 qubits, the initial contraction was calculated using a greedy algorithm and resulted in contraction width 44. This means that the cost of simulation would be \( \geq 70 \) TFLOPS and 281 TB, respectively. Using our step-dependent slicing algorithm with \( r = n \) on 64 computational nodes allows us to remove 6 vertices and split the expression into smaller parts that have a contraction width of 32, which easily fits into RAM of one node. The whole simulation, in this case, uses 60% of 13 TB cumulative memory of 64 nodes, more than 35x less than a serial approach uses.

Figure 11 shows how the contraction width \( c \) of the sliced tensor expression depends on step \( s \) for several values of numbers of sliced indices \( n \). The notable feature is the high variance of \( c \) with respect to \( s \)—the difference between the smallest and the largest values goes up to 9, which translates to a 512x cost difference. However, the general pattern for different QAOA circuits remains similar: increasing \( n \) by one reduces \( \min_s(c(s)) \) by one.

Computational speedup provided by 64 nodes is on the order of \( 4096 = 2^{12} \) which is more than the theoretical limit of 64x for any kind of straightforward parallelization. Using 512 nodes drops the contraction width to 29 and reduces the simulation time 3x compared with that when using 64 nodes.

The experimental results for 64–1,024 nodes are shown in Fig. 10. Simulation time includes serial simulation of the first small steps before step \( s \), which takes 40 s for a 210-qubit circuit, or 25–50% of total simulation time, depending on the number of nodes.

IX. CONCLUSIONS

We have presented a novel approach for simulating large-scale quantum circuits represented by tensor network expressions. It allowed us to simulate large QAOA quantum circuits up to 210 qubit circuits with a depth of 1,785 gates on 1,024 nodes and 213 TB of memory on the Theta supercomputer.
Algorithm 1 Parallel bucket elimination

Input: Ordered buckets $B_i$ containing tensors, parallelization step $s$, number of parallel vertices $n$ vertex ordering $\pi : V \rightarrow \mathcal{N}$, $\pi = \{(v_i, i)\}_{i=1}^{|V|}$

Output:

1: contract_first($s, B_i$) $\triangleright$ Serial part: contract first $s$ buckets
2: for $i = 0, n$ do $\triangleright$ Find best index to slice along
3: \hspace{0.5cm} $p_i = \max_{G, \pi} \text{degree}_v(G)$
4: \hspace{0.5cm} remove_vertex($G, p_i$)
5: end for
6: $\emptyset \leftarrow \text{binary_repr}(\text{mpi}_\text{get}_\text{rank}())$ $\triangleright$ Find best index to slice along
7: for $j = 0, n$ do $\triangleright$ Slice the expression
8: \hspace{0.5cm} $B_i \leftarrow B_i[p_j = v_j]$ $\triangleright$ Process next bucket
9: end for
10: for $i = s, |V|$ do $\triangleright$ Process next bucket
11: \hspace{0.5cm} $v \leftarrow \pi^{-1}(i)$ $\triangleright$ Process next bucket
12: \hspace{0.5cm} $R \leftarrow B_i[0]$ $\triangleright$ Process next bucket
13: for $T \in B_i[1 : ]$ do $\triangleright$ Process next bucket
14: \hspace{0.5cm} $r \leftarrow [T \text{indexes} \cup R \text{indexes}]$ $\triangleright$ Result size
15: \hspace{0.5cm} $t \leftarrow \lfloor \frac{|r| - 2}{2} \rfloor$ $\triangleright$ Contract in thread pool
16: if $t > 0$ then $\triangleright$ Contract in thread pool
17: \hspace{0.5cm} $Q \leftarrow \text{shared}\_\text{tensor}(r)$ $\triangleright$ Contract in thread pool
18: \hspace{0.5cm} $\vec{w} \leftarrow \text{binary}_\text{repr}(\text{get}\_\text{thread}_\text{num}())$ $\triangleright$ Contract in thread pool
19: \hspace{0.5cm} $k \leftarrow \text{indices}_v(Q); t]$ $\triangleright$ Contract in thread pool
20: \hspace{0.5cm} $Q_w, Q_{w_j} = (Q_v, T_v)[k_j = w_j]$ $\triangleright$ Contract in thread pool
21: \hspace{0.5cm} $R \leftarrow Q$ $\triangleright$ $R$ now points to shared memory tensor
22: else
23: \hspace{0.5cm} $R \leftarrow RT$ $\triangleright$ Parallel sum can be implemented in the same fashion as the contraction above
24: end if
25: end for
26: $R \leftarrow \sum_i R$ $\triangleright$ Parallel sum can be implemented in the same fashion as the contraction above
27: if $R$ is scalar then
28: \hspace{0.5cm} result $\leftarrow \text{result} \cdot R$ $\triangleright$ Parallel sum can be implemented in the same fashion as the contraction above
29: else
30: \hspace{0.5cm} $k = \pi(w)$, $w$ is the earliest index of $R$ w.r.t $\pi$ $\triangleright$ Parallel sum can be implemented in the same fashion as the contraction above
31: \hspace{0.5cm} $B_k \leftarrow B_k \cup R$ $\triangleright$ Parallel sum can be implemented in the same fashion as the contraction above
32: end if
33: end for
34: result $\leftarrow \text{mpi}_\text{reduce}_\text{sum}($result$)$ $\triangleright$ Gather the results
35: return result

As a demonstration, we applied our algorithm to simulate quantum circuits for QAOA ansatz state with $p = 1$, but our algorithm also works for higher $p$ also. To reduce memory footprint, we developed a step-dependent slicing algorithm that contracts part of an expression in advance and reduces the expensive task of finding an elimination order. Using this approach, we found an ordering that produces speedups up to 512x, when compared with other parallelization steps $s$ for the same expression.

The unmodified tensor network contraction algorithm is able to simulate 120-140 qubit circuits, depending on the problem graph. By using a randomized greedy ordering algorithm, we were able to raise this number to 175 qubits. Furthermore, using a parallelization based on step-dependent slicing allows us to simulate 210 qubits on the supercomputer Theta. Another way to obtain samples from the QAOA ansatz state is to use density matrix simulation, but it is prohibitively computationally expensive and memory demanding. The largest density matrix simulators known to us can compute 100 qubit problems [40] and 120 qubit problems [41] using high-performance computing.

The important feature of our algorithm is applicability to the QAOA algorithm: the contraction order has to be generated only once and then can be reused for additional simulations with different circuit parameters. As a result, it can be used to simulate a large variety of QAOA circuits, which is used to study QAOA angles transferability between graphs [42], optimality of angles [14], and the behaviour of QAOA under symmetry [43].

We conclude that this work presents a significant development in the field of quantum simulators. To the best of our knowledge, the presented results are the largest QAOA quantum circuit simulations reported to date.

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Fig. 11: Distribution of the contraction width (maximum number of neighbors) \( c \) for different numbers of parallel indices \( n \). While variance of \( c \) is present, showing that it is sensible to the parallelization index \( s \), we are interested in the minimal value of \( s \), which, in turn, generally gets smaller for bigger \( n \).
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