Designs of Branch-Line Couplers by Considering the Parasitic Effects of P-I-N Diodes

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ABSTRACT Branch-line couplers (BLCs) are commonly used in the wireless systems. To achieve reconfigurable applications, switchable BLCs with p-i-n diodes can be used. Several studies have used diode parasitic reverse-biased capacitor and forward-biased inductor to approach off and on states. Although the capacitance and inductance are usually low, the parasitic effect may degrade predicted switching responses. This study proposes five reconfigurable switching microstrip BLCs. Each of the first two presented BLCs uses shunt to ground diodes for realizing two switching modes. The first mode with reverse-biased capacitors for perfect matching design is equivalent to a conventional branch-line coupler (BLC). The second mode uses low forward-biased inductances to approach shunt to ground, which transfers most signal power from Port 1 to Port 2/4; however, parasitic inductors produce some mismatches. To improve this problem, the proposed third or fourth BLC achieves two perfect matching modes by using shunt stub-loaded diodes. Specifically, by using four stub-loaded diodes, the proposed final BLC exhibits three perfect matching modes and one perfect isolation mode under a lossless ideal circuit condition.

INDEX TERMS Branch-line, coupler, diode, matching, parasitic effect, reconfigurable, stub-loaded, switchable.

I. INTRODUCTION

In wireless communication system, antenna usually requires power splitting devices such as power divider [1] and conventional branch-line coupler (BLC) [1] which can achieve 90° phase difference between two transmission paths and equal power delivery. Reconfigurable components [2]–[31] were popular research topics because each of them provided a different desired responses by using one device. [2], [4]–[6], [9]–[11], [13], [14], [18], [19], [24], and [28]–[31] have used varactors/active inductors to adjust their phases, operating frequencies, or power splitting ratios. [3], [7], [8], [23], [25], and [26] have used p-i-n diodes to provide switching couplers and dividers.

For a switchable circuit, achieving one of its different mode perfect matching conditions may not be difficult; however, simultaneously meeting all mode perfect matching designs are usually challenging. Furthermore, control changing response components, such as p-i-n diode, usually cannot prevent unwanted parasitic effects (reverse-biased capacitor and forward-biased inductor), which may highly degrade different mode matching performances of a reconfigurable device. For example, [7] and [8] used p-i-n diodes to approach off and on states. In practical design, approaching p-i-n diode on and off states exhibit parasitic inductance and capacitance. The parasitic inductance and capacitance could affect the predicted lengths of transmission lines and short/open circuit quality. Although [7] mentioned the parasitic effects of p-i-n diodes have to be compensated by additional tuning networks, there is no clear systematic design process to discuss this issue. Therefore, time-consuming optimization processes might be required after completing the initial circuit design. [12] added extra shunt capacitances to compensate p-i-n diode inductances; however, its parasitic capacitances were not solved.

This study proposes five microstrip 4-port switchable BLCs, namely BLC A, BLC B, BLC C, BLC D, and BLC E. BLC A and BLC B are exactly equivalent to a
conventional BLC when p-i-n diodes are reverse biased, and most signal power is transferred from Port 1 to Port 4 or Port 1 to Port 2 when diodes are forward biased. However, non-zero parasitic inductances are not avoided in BLC A and BLC B for forward-biased diodes, which degrade predicted performances. BLC C and BLC D substantially improve the performance by using shunt stub-loaded diodes. Finally, BLC E demonstrates perfect responses for three matching modes and one blocking mode from Port 1 to each of the other three ports by using four shunt stub-loaded diodes. Compared with [7]/[8] has two operation modes, BLC B and BLC D provides detailed designs for solving one and both of the two mode parasitic effects, respectively.

II. DESIGN OF PROPOSED BLC A

Fig. 1 illustrates the conventional BLC composed of six lines $X_i$, $i = 1–6$, where electrical lengths are $\theta_1 = 90^{\circ}$ and $\theta_2 = 90^{\circ}$; characteristic impedances are $Z_1 = 35.36$ $\Omega$ and $Z_2 = 50$ $\Omega$ when system impedance is $Z_0 = 50$ $\Omega$. Figs. 2(a) and 2(b) are even- and odd-mode equivalent half circuits of BLC presented in Fig. 1, respectively, wherein $Z_{\text{in1}}$, $Z_{\text{in2}}$, $Z_{\text{in01}}$, and $Z_{\text{in02}}$ are input impedances. Fig. 3 illustrates BLC A with four transmission lines $X_1^{(A)}–X_4^{(A)}$, wherein $\phi_i^{(A)}$ and $Z_i^{(A)}$, $i = 1$ or 2, represent electrical length and characteristic impedance, respectively; two diodes ($D_1^{(A)}$ and $D_2^{(A)}$); and two capacitors of $C_1^{(A)}$ and $C_2^{(A)}$ capacitances. BLC A exhibits two operation modes Mode 1$^A$ and Mode 2$^A$, in which all diodes are operated by using reverse- and forward-biased states, respectively. Mode 1$^A$ is equivalent to the conventional BLC. Most signal power is transferred from Port 1 to Port 4 in Mode 2$^A$. Infineon’s BAR65-02 V p-i-n diode is used to design each switching circuit of proposed couplers. Fig. 4 illustrates the diode model, in which the forward-biased state is a series resistor of $R_D$ resistance and an inductor of $L_D$ inductance, and the reverse-biased state is a capacitor of $C_D$ capacitance, with $L_D = 0.7$ nH and $C_D = 0.34$ pF. The practical value of $R_D$ is small and slightly affects performances of proposed BLCs, wherein $R_D = 1$ $\Omega$ is extracted for each diode of the proposed circuits. To simplify the analysis, $R_D$ is considered $0 \Omega$ for all proposed BLC ideal circuit models. Fig. 5(a) and Fig. 5(b) present Mode 1$^A$ and Mode 2$^A$ circuits of BLC A, respectively. In Fig. 5(a), the four capacitances $C_1^{(AF)}$, $C_2^{(AF)}$, $C_1^{(AR)}$, and $C_2^{(AR)}$ are equal ($C_1^{(AF)} = C_2^{(AF)} = C_1^{(AR)} = C_2^{(AR)} = C_A$). $X_2^{(A)}$ with two parallel capacitors of $C_A$ capacitance is equivalent to series two lines $X_2$ and $X_4$ of conventional BLC (Fig. 1). They can be derived to form the following equations by using their $ABCD$ matrices.

$$
\cos \theta_2 - 2\pi f_0 C_A Z_2^{(A)} \sin \theta_2^{(A)} = 0
$$

$$
Z_2^{(A)} \sin \theta_2^{(A)} = 50 \Omega
$$

![FIGURE 4. Diode circuit model.](image)

where $f_0$ is the operating center frequency. The line parameters of $X_1^{(A)}$ or $X_4^{(A)}$ presented in Fig. 5(a) are equal to those of $X_1$ or $X_6$ presented in Fig. 1; Fig. 5(a) exhibits the bilateral symmetry. Therefore, Mode 1$^A$ of BLC A is equivalent to the BLC of Fig. 1. Fig. 5(b) presents the Mode 2$^A$ circuit of BLC A, where $L_{D1}^{(AF)}$ and $L_{D2}^{(AF)}$ are equal inductances ($L_{D1}^{(AF)} = L_{D2}^{(AF)} = L_A$). All design parameters are determined and fixed except for two inductances ($L_{D1}^{(AF)}$ and $L_{D2}^{(AF)}$). Each of the proposed circuits exhibits microstrip line form and is realized using RO4003C substrate with a thickness of 0.508 mm, dielectric constant of 3.65, and loss tangent of 0.0065. The proposed BLC A requires a via hole for inductances is approximately 0.3 nH; the total equivalent capacitance value

![FIGURE 5. (a) Mode 1$^A$ and (b) Mode 2$^A$ equivalent circuits of proposed BLC A.](image)
of one via hole and diode reverse-biased state capacitance is approximately 0.345 pF, i.e., the total equivalent capacitance of series $C_D$ and $L_h$ is approximately 0.345 pF. Thus, $C_A = 0.345$ pF and $L_A = L_D + L_h = 1$ nH are used to design Mode 1$^A$ and Mode 2$^A$ responses of BLC A, respectively. $\theta_1^{(A)} = 78.77^\circ$ and $Z_2^{(A)} = 51\Omega$ are obtained by substituting $C_A = 0.345$ pF and designed center frequency $f_0 = 1.8$ GHz in (1) and (2). By using the BLC A design, Mode 1$^A$ response is perfectly match with the conventional BLC (Fig. 1), i.e., $|S_{21}| = |S_{31}| = -3$dB, and the phase difference of $S_{21}$ to $S_{31}$ is $90^\circ$ at center frequency. For Mode 2$^A$, $L_A = 1$ nH and the input impedance of the inductance are low. Therefore, Port 2 and Port 3 approach short circuits. Because $\theta_1^{(A)} = 90^\circ$, the input impedance from Port 1 to Port 2 or Port 4 to Port 3 is large. In other words, from Port 1 to Port 2 and Port 4 to Port 3 direction loading effects are negligible. $X_2^{(A)}$ with its two end shunt capacitors is equivalent to series two lines $X_2$ and $X_4$ of the conventional BLC (Fig. 1). Consequently, $|S_{21}|$ and $|S_{31}|$ are small and $|S_{41}|$ is approximately 100(kΩ) because each of Port 1/Port 4 load impedance and characteristic impedance of $X_2/X_4$ is $50\Omega$, i.e., signal approaches the impedance match at Port 1 or Port 4. Fig. 6 presents the layout and photograph of BLC A. Fig. 6(a) indicates that the signal and biasing circuit are nearly isolated by a resistor of $R = 5.6k\Omega$, which is also used for all other proposed circuits. Fig. 6(b) illustrates two biasing lines BL$^{-1}$A and BL$^{2}$A, which are sourced by $V_{1A}$ and $V_{2A}$ voltages, and BL$^{2}$A is an electronic line connected to backside ground plane. For Mode 1$^A$ and Mode 2$^A$, $V_{2A} - V_{1A} = 7.5$ V and $V_{1A} - V_{2A} = 7.5$ V, respectively. Layout of Fig. 6(a) uses the shunt open stub to realize each capacitance of $C_1^{(A)}$ and $C_2^{(A)}$ of BLC A.

Figs. 7 and 8 present the magnitude and phase responses of $S$ parameters, and each ideal circuit simulation of Mode 2$^A$ is for diode loss $R_D = 0\Omega$ or $R_D = 1\Omega$ because this mode has forward-biased state diodes. However, Mode 1$^A$ doesn’t discuss diode losses since it has reverse-biased state diodes which don’t consider the losses such as the diode model of Fig. 4. Furthermore, each port 50-$\Omega$ extension line and connector are calibrated using the Thru-Reflect Line (TRL) method to obtain the results of all proposed circuits; each port 50-$\Omega$ line is de-embedded for full-wave simulations of all proposed circuits. Minor affections between ideal circuit simulations of $R_D = 0\Omega$ and $R_D = 1\Omega$ are observed for supporting the $R_D$ neglect in the ideal circuit design. The small $R_D$ and minor affections are also included in corresponding responses of all other ideal circuits. Consequently, $R_D = 0\Omega$ is used to facilitate all designs of the proposed ideal circuits. For Mode 1$^A$, the measured insertion losses of both $-20\log|S_{21}|$ and $-20\log|S_{41}|$ are approximately 3.19 dB at 1.8 GHz; and the measured $-15$-dB bandwidth ranges of $|S_{11}|$, $|S_{32}|$, and $|S_{41}|$ are approximately 1.636–1.928, 1.595–1.925, and 1.683–2.053 GHz, respectively. For Mode 2$^A$, the measured insertion losses of $-20\log|S_{21}|$, $-20\log|S_{31}|$, and $-20\log|S_{41}|$ are approximately 10.7, 10.25, and 1.38 dB at 1.8 GHz, respectively; the measured $-15$-dB bandwidth range of $|S_{11}|$ is approximately 1.67–1.95 GHz, $|S_{32}|$ is $< -20$ dB near the operating band. In Mode 1$^A$, the measured phases of $S_{21}$ and $S_{31}$ are approximately $-89.13^\circ$ and $-178.15^\circ$ at 1.8 GHz, respectively, whereas in Mode 2$^A$, that of $S_{41}$ is approximately $-137.4^\circ$. In BLC A design, Mode 1$^A$ ideal circuit simulation achieves perfectly match at $f_0$, as illustrated in Fig. 7(a) and its $S_{21}$ to $S_{31}$ phase difference is $90^\circ$, as illustrated in Fig. 8(a). However, Mode 2$^A$ ideal circuit responses exhibits some mismatches such as $|S_{21}| \approx |S_{31}| \approx -11$dB and $|S_{41}| \approx -0.75$dB at $f_0$. Although Mode 2$^A$ can transfer most signal energy from Port 1 to Port 4, some applications may not be accepted by these level mismatches. This problem is occurred because $L_A \neq 0$ at $f_0$, i.e., Port 2 or Port 3 are not exactly equivalent to a short circuit at $f_0$. Moreover, when the $L_A$ value is zero, phase of

![FIGURE 6. (a) Layout and (b) photograph of BLC A.](image-url)

![FIGURE 7. Ideal circuit simulation, full-wave simulation, and measurement magnitude responses of $S$ parameters for (a) Mode 1$^A$ and (b) Mode 2$^A$.](image-url)

![FIGURE 8. Ideal circuit simulation, full-wave simulation, and measurement phase responses of $S$ parameters for (a) Mode 1$^A$ and (b) Mode 2$^A$.](image-url)
$S_{41}$ is $-90^\circ$. The third proposed circuit BLC C can solve these parasitic effect problems of non-zero $L_A$ value.

III. DESIGN OF PROPOSED BLC B

$S$ parameters $S_{11}, S_{21}, S_{31},$ and $S_{41}$ of four-port symmetric circuit, such as locations of ports in Fig. 1, can be obtained using following equations.

\[
\begin{align*}
S_{11} & = 1/2(S_{11e} + S_{11o}) \\
S_{21} & = 1/2(S_{21e} + S_{21o}) \\
S_{31} & = 1/2(S_{21e} - S_{21o}) \\
S_{41} & = 1/2(S_{11e} - S_{11o})
\end{align*}
\]

where $S_{11e/o}$ and $S_{21e/o}$ are the even- and odd-mode circuit $S$ parameters of the four-port symmetric circuit, respectively. $S_{11e/o}$ and $S_{21e/o}$ for Fig. 2 are calculated as follows:

\[
\begin{align*}
S_{11e} & = 0 \quad (7) \\
S_{21e} & = -1/\sqrt{2}(1 + j) \quad (8) \\
S_{11o} & = 0 \quad (9) \\
S_{21o} & = 1/\sqrt{2}(1 - j). \quad (10)
\end{align*}
\]

In the traditional BLC (Fig. 1), Points $A_1$ and $A_2$ are connected to ground, as illustrated in Fig. 9. The even-mode or odd-mode circuit presented in Fig. 9 is equivalent to the odd-mode circuit presented in Fig. 2(b); i.e., $S_{21e} = S_{21o} = 1/\sqrt{2}(1 - j)$ and $S_{11e} = S_{11o} = 0$ for Fig. 9.

By using (3)–(6), $S_{11}, S_{21}, S_{31},$ and $S_{41}$ of Fig. 9 are obtained as follows:

\[
\begin{align*}
S_{11} & = 0 \quad (11) \\
S_{21} & = 1/\sqrt{2}(1 - j) \quad (12) \\
S_{31} & = 0 \quad (13) \\
S_{41} & = 0. \quad (14)
\end{align*}
\]

All signal power is transferred from Port 1 to Port 2 and the phase of $S_{21}$ is $-45^\circ$. Although Fig. 9 was proposed in [7]–[8], the parasitic effects of switches were not provided a detailed discussion or solution. The related parasitic effects of switches are included in BLC B (Fig. 10) composed of six transmission lines $X_{11}^{(B)} - X_{10}^{(B)}$, wherein $\theta_i^{(B)}$ and $Z_i^{(B)}$, $i = 1$ or 2, represent electrical length and characteristic impedance, respectively; two diodes $D_1^{(B)}$ and $D_2^{(B)}$ exhibits reverse-biased capacitances $C_1^{(BR)}$ and $C_2^{(BR)}$; forward-biased inductances $L_1^{(BF)}$ and $L_2^{(BF)}$. BLC B exhibits two operation modes Mode 1$^B$ and Mode 2$^B$, in which all diodes are operated by reverse- and forward-biased states, respectively. Mode 1$^B$ is exactly equivalent to the conventional BLC (Fig. 1), and Mode 2$^B$ is nearly equivalent to the BLC of Fig. 9. Capacitance is $C_1^{(BR)} = C_2^{(BR)} = C_B$ in Mode 1$^B$ and inductance is $L_1^{(BF)} = L_2^{(BF)} = L_B$ in Mode 2$^B$. Fig. 11(a) and 11(b) illustrate the even- and odd-mode top half equivalent circuits of Mode 1$^B$, respectively, wherein $Z_{1e}^{(BR)}, Z_{2e}^{(BR)}, Z_{1o}^{(BR)},$ and $Z_{2o}^{(BR)}$ are input impedances. The design conditions are as follows:

\[
\begin{align*}
\theta_1^{(B)} & = 90^\circ \quad (15) \\
Z_1^{(B)} & = 35.36 \Omega \quad (16) \\
Z_{1e}^{(BR)} & = Z_{1o}^{(BR)} = Z_{1e}^{(BF)} = Z_{1o}^{(BF)} \quad (17) \\
Z_{2e}^{(BR)} & = Z_{2o}^{(BR)} = Z_{2e}^{(BF)} = Z_{2o}^{(BF)} \quad (18)
\end{align*}
\]

where $Z_{1e1}, Z_{1e2}, Z_{1o1},$ and $Z_{1o2}$ of (17) and (18) are the input impedances of Fig. 2. From the design conditions (15)–(18), Fig. 2(a) and 2(b) are equivalent to Fig. 11(a) and 11(b), respectively. By using (17) and (18), the following design equations are derived.

\[
\begin{align*}
\frac{\pi f_0 Z_2^{(B)} C_B + \tan \theta_2^{(B)}}{Z_2^{(B)} (Z_2^{(B)})^2 \tan \theta_2^{(B)} \pi f_0 C_B} & = \frac{1}{Z_0} \quad (19) \\
Z_2^{(B)} \tan \theta_2^{(B)} & = Z_0 \quad (20)
\end{align*}
\]

All the determined parameters of transmission lines in Mode 2$^B$ are same as those in Mode 1$^B$. Therefore, the odd-mode circuit of Mode 2$^B$ is same as that of Mode 1$^B$. \par

\[\text{P. -H. Deng et al.: Designs of Branch-Line Couplers by Considering the Parasitic Effects of P-I-N Diodes}\]
which is equivalent to that of the conventional BLC [Fig. 2(b)] or the even-mode/odd-mode circuit of Fig. 9. When the inductance $L_B$ is low, i.e., Points $A_1(B)$ and $A_2(B)$ approach short circuits at $f_0$, the even-mode circuit of Mode 2B approaches the odd-mode circuit of Mode 1B. Thus, Mode 2B is nearly equivalent to Fig. 9 and approaches the $S$ parameters of (11)–(14). Each of the diodes $D_1(B)$ and $D_2(B)$ in microstrip BLC B requires the via hole for connecting with ground. As described in BLC A, the total reverse-biased capacitance and forward-biased inductance of each diode with a via hole in this work are 0.345 pF (i.e., $C_B = 0.345$ pF) and 1 nH (i.e., $L_B = 1$ nH), respectively. $\theta_2^{(B)} = 41.9^\circ$ and $Z_2^{(B)} = 55.72 \Omega$ are solved by substituting $C_B = 0.345$ pF, $Z_0 = 50 \Omega$, and $f_0 = 1.8$ GHz in (19) and (20).

Fig. 12 presents the layout and photograph of BLC B. In Fig. 12(b), two biasing lines BL1B and BL2B are sourced by $V_{IB}$ and $V_{2B}$ voltages, respectively, and BL2B is an electronic line connected to the backside ground plane. For Mode 1B and Mode 2B, $V_{2B} - V_{IB} = 7.5$ V and $V_{1B} - V_{2B} = 7.5$ V, respectively. Figs. 13 and 14 present the magnitude and phase responses of $S$ parameters, where each ideal circuit simulation of Mode 2B is for diode loss $R_D = 0 \Omega$ or $R_D = 1 \Omega$. In Mode 1B, the measured insertion losses for $-20\log |S_{21}|$ and $-20\log |S_{31}|$ are approximately 3.3 dB and 3.1 dB at 1.8 GHz, respectively, and the measured $-15$-dB bandwidth ranges of $|S_{11}|$, $|S_{32}|$, and $|S_{41}|$ are approximately 1.63–1.906, 1.608–1.939, and 1.606–1.939 GHz, respectively. In Mode 2B, the measured insertion losses of $-20\log |S_{21}|$, $-20\log |S_{31}|$, $-20\log |S_{32}|$, and $-20\log |S_{41}|$ are approximately 0.93, 12.4, 17, and $-17.2$ dB at 1.8 GHz, respectively, and measured $|S_{11}|$ is approximately $-11.54$ dB at 1.8 GHz. The measured phases of $S_{21}$ and $S_{31}$ are approximately $-91.7^\circ$ and $-182.15^\circ$ at 1.8 GHz in Mode 1B, respectively; the measured phase of $S_{21}$ is approximately $-61.29^\circ$ in Mode 2B. In BLC B design, Mode 1B ideal circuit simulation achieves perfectly match at $f_0$, as illustrated in Fig. 13(a) and its $S_{21}$ to $S_{31}$ phase difference is $90^\circ$, as illustrated in Fig. 14(a). However, Mode 2B ideal circuit responses exhibit some mismatches such as $|S_{11}|$ is approximately $-17.25$ dB, $|S_{21}|$ is approximately $-0.43$ dB, $|S_{31}|$ is approximately $-12.56$ dB, and $|S_{41}|$ is approximately $-17.24$ dB at $f_0$; the frequency of minimal $|S_{21}|$ near the operating frequency $f_0$ shifted to 1.678 GHz. Although Mode 2B can transfer most signal energy from Port 1 to Port 2 at $f_0$, there exist mismatches and those degrade the center frequency several response performances. This problem is similar to that of BLC A and is caused by $L_g \neq 0$ at $f_0$, i.e., Points $A_1(B)$ and $A_2(B)$ are not equivalent to short circuits at $f_0$. The fourth proposed circuit BLC D solve these parasitic effect problems of the non-zero $L_B$ value. Moreover, when $L_B$ value is zero, phase of $S_{21}$ is $-45^\circ$.

Type A of [7] is an equal power splitting conventional BLC (Fig. 1) which can connect shunt to ground p-i-n diode to each of Points $A_1$ and $A_2$. Type A of [7] used ideal open and short to design each diode switching model. However, the model deviates from the practical design situation. Figs. 15 and 16 show ideal circuit simulations of BLC B and Type A of [7] wherein each diode uses the proposed model of Fig. 4 ($C_D = 0.34$ pF, $L_D = 0.7$ nH, and $R_D = 0 \Omega$), i.e., each diode in Type A of [7] replaces ideal open and short with $C_D = 0.34$ pF and $L_D = 0.7$ nH for representing reverse- and forward-biased states, respectively. Fig. 15(a) shows perfect match and equal power split ($|S_{21}| = |S_{31}| = -3$ dB) in Mode 1B of BLC B, however, when the two diodes are operated in reverse-biased states, the responses for Type A of [7] have mismatches resulting in unbalanced power splitting levels ($|S_{21}| = -4.174$ dB and $|S_{31}| = -2.192$ dB). Furthermore, the center frequency phase responses of Fig. 16(a) are $\angle S_{21} = -90^\circ$ and $\angle S_{31} = -180^\circ$ for BLC B and $\angle S_{21} = -95.983^\circ$ and $\angle S_{31} = -186.812^\circ$ for

![FIGURE 12. (a) Layout and (b) photograph of BLC B.](image)

![FIGURE 13. Ideal circuit simulation, full-wave simulation, and measurement magnitude responses of $S$ parameters for (a) Mode 1B and (b) Mode 2B.](image)

![FIGURE 14. Ideal circuit simulation, full-wave simulation, and measurement phase responses of $S$ parameters for (a) Mode 1B and (b) Mode 2B.](image)
IV. DESIGN OF PROPOSED BLC C

Fig. 17 presents BLC C, which can solve the undesired parasitic effects of non-zero inductances presented in BLC A. BLC C consists of four transmission lines $X_1^{(C)} \sim X_4^{(C)}$, wherein $\theta_1^{(C)}$ and $Z_1^{(C)}$, $i = 1$ or $2$, represent electrical length and characteristic impedance, respectively; two open stubs $X_S$ and $X_{C}$, wherein $\theta_S^{(C)}$ and $Z_S^{(C)}$ represent electrical length and characteristic impedance, respectively; shunt capacitors of $C_1^{(C)}$ and $C_2^{(C)}$ capacitances, wherein $C_1^{(C)} = C_2^{(C)} = C_C$, and two diodes $D_1^{(C)}$ and $D_2^{(C)}$, wherein reverse-biased capacitances are $C_D^{(CR)}$ and $C_D^{(CR)}$, respectively; forward-biased inductances are $L_{D1}^{(CF)}$ and $L_{D2}^{(CF)}$, respectively. $Z_{in1}^{(C)}$, and $Z_{in2}^{(C)}$ are input impedances. BLC C has two operation modes Mode 1$^C$ and Mode 2$^C$ wherein all diodes are operated by reverse- and forward-biased states, respectively. Mode 1$^C$ is equivalent to a conventional BLC (Fig. 1). All signal power is perfectly transferred from Port 1 to Port 4 and phase of $S_{41}$ is $-90^\circ$ in Mode 2$^C$. The capacitance is $C_{D1}^{(C)} + C_{D2}^{(C)} = C_D$ in Mode 1$^C$ and the inductance is $L_{D1}^{(CF)} = L_{D2}^{(CF)} = L_D$ in Mode 2$^C$. The first step is to design Mode 2$^C$. $Z_{in1}^{(C)} = Z_{in2}^{(C)} = 0$ in Mode 2$^C$ can derive the following equation:

$$j2\pi f_0 L_D + \frac{Z_S^{(C)}}{\tan \theta_S^{(C)}} = 0. \tag{21}$$

In (21), $f_0$ is the operating center frequency and $L_D$ is determined when the diode is selected. One of $Z_S^{(C)}$ and $\theta_S^{(C)}$ can be arbitrarily designed and the other one can be solved using (21). The second step is Mode 1$^C$ design. In Mode 1$^C$, each of $Z_{in1}^{(C)}$ and $Z_{in2}^{(C)}$ designs to equal the input impedance of shunt capacitor at each of Port 1 and Port 4, i.e., the design equation can be written as follows:

$$\frac{1}{j2\pi f_0 C_C} = \frac{1}{j2\pi f_0 C_D} + \frac{Z_S^{(C)}}{\tan \theta_S^{(C)}}. \tag{22}$$

In (22), $Z_S^{(C)}$ and $\theta_S^{(C)}$ are determined for Mode 2$^C$, and $C_D$ is a well-known parameter when the diode is used in Mode 2$^C$. Thus, $C_C$ is determined. $\theta_1^{(C)} = 90^\circ$ and $Z_1^{(C)} = 35.36\Omega$. In (1) and (2), $C_A = C_C$, $\theta_2^{(A)} = \theta_2^{(C)}$, and $Z_2^{(A)} = Z_2^{(C)}$. $\theta_1^{(C)}$ and $Z_1^{(C)}$ are solved using (1) and (2) because $f_0$ and $C_D$ has been determined. Therefore, Mode 1$^C$ is equivalent to Mode 1$^A$ as the conventional BLC of Fig. 1 at the center frequency $f_0$, i.e., $X_1^{(C)}$ with shunt $C_1^{(C)}$ and $C_2^{(C)}$ capacitors is equivalent to a $50\Omega$ and $90^\circ$ transmission line between Port 1 and Port 4, as presented in Fig. 1. In Mode 2$^C$, $Z_{in1}^{(C)} = Z_{in2}^{(C)} = 0$ and $\theta_1^{(C)} = 90^\circ$, which can cause $Z_{in1}^{(C)} = Z_{in2}^{(C)} = \infty$. Therefore, the signal is perfectly transferred from Port 1 to Port 4 by using the equivalent $50\Omega$ and $90^\circ$ transmission line when each port impedance is $Z_0 = 50\Omega$ and the phase
of $S_{41}$ is $-90^\circ$ in Mode $2^C$. The center frequency $f_0 = 1.8$ GHz is operated for BLC C. The forward-biased state inductance and reverse-biased state capacitance of the diode are $L_D = 0.7$ nH and $C_D = 0.34$ pF, respectively. The related parameters $Z_S^{(C)} = 29.55\Omega$, $\theta_S^{(C)} = 75^\circ$, $Z_L^{(C)} = 50.92\Omega$, $\theta_L^{(C)} = 79.25^\circ$, and $C_C = 0.33$ pF are obtained using the BLC C design. Fig. 18 presents the layout and photograph of BLC C. The three biasing lines BL1C, BL2C, and BL3C presented in Fig. 18(b), are sourced by $V_{1C}$, $V_{2C}$, and $V_{3C}$ voltages. $V_{1C} - V_{2C} = V_{3C} - V_{1C} = 7.5$ V and $V_{2C} - V_{1C} = V_{1C} - V_{3C} = 7.5$ V are for Mode $1^C$ and Mode $2^C$, respectively. The implemented circuit presented in Fig. 18 uses the shunt open stub to realize each capacitance of $C_1^{(C)}$ and $C_2^{(C)}$ presented in Fig. 17. Figs. 19 and 20 present the magnitude and phase responses of $S$ parameters, where each ideal circuit simulation of Mode $2^C$ is for diode loss $R_D = 0$ or $R_D = 1$ Ω. For Mode $1^C$, the measured insertion losses of $-20\log|S_{21}|$ and $-20\log|S_{31}|$ are approximately 3.11 and 3.29 dB at 1.8 GHz, respectively, and the measured $-15$-dB bandwidth ranges of $|S_{11}|$, $|S_{21}|$, and $|S_{41}|$ are approximately 1.63–1.942, 1.606–1.945, and 1.627–1.975 GHz, respectively. For Mode $2^C$, the measured insertion loss of $-20\log|S_{41}|$ is approximately 0.655 dB at 1.8 GHz, and the measured $-15$-dB bandwidth ranges of $|S_{11}|$, $|S_{21}|$, $|S_{31}|$, and $|S_{32}|$ are approximately 1.552–2.02, 1.608–2.018, 1.6112.139, and 1.337–2.322 GHz, respectively. The measured phases of $S_{21}$ and $S_{31}$ are approximately $-93.22^\circ$ and $-184^\circ$ at 1.8 GHz in Mode $1^C$, respectively; the measured phase of $S_{41}$ is approximately $-94.86^\circ$ in Mode $2^C$. Ideal circuit simulations of Figs. 19(a) and 19(b) demonstrate perfect matches in Mode $1^C$ and Mode $2^C$.

V. DESIGN OF PROPOSED BLC D

Fig. 21 illustrates BLC D, which can solve the undesired parasitic effects of non-zero inductances in BLC B. BLC D consists of six transmission lines $X_{D_i}^{(D)} - X_{B_i}^{(D)}$, wherein $\theta_i^{(D)}$ and $Z_i^{(D)}$, $i = 1$ or 2, represent electrical length and characteristic impedance, respectively; two open stubs $X_{S1}^{(D)}$ and $X_{S2}^{(D)}$, wherein $\theta_S^{(D)}$ and $Z_S^{(D)}$ represent electrical length and characteristic impedance, respectively; and two diodes $D_1^{(D)}$ and $D_2^{(D)}$, in which reverse-biased capacitances are $C_{DS1}^{(D)}$ and $C_{DS2}^{(D)}$, respectively, and forward-biased inductances are $L_{D1}^{(D)}$ and $L_{D2}^{(D)}$, respectively. $Z_{inD1}^{(D)}$ and $Z_{inD2}^{(D)}$ are input impedances. BLC D exhibits two operation modes Mode $1^D$ and Mode $2^D$, in which all diodes are operated through reverse- and forward-biased states, respectively. Capacitance is $C_D = 0.34$ pF in Mode $1^D$ and inductance is $L_{D1}^{(D)} = L_{D2}^{(D)} = L_D = 0.7$ nH in Mode $2^D$. The first step is to design Mode $2^D$. In Mode $2^D$, the line parameters of $X_{S1}^{(D)}$ and $X_{S2}^{(D)}$ can be determined when $Z_{inD1} = Z_{inD2} = 0$. In Mode $1^D$, $Z_{inD1}^{(D)}$ or $Z_{inD2}^{(D)}$ is equivalent to the input impedance of a shunt to ground capacitor with $C_{DS}$ capacitance. Mode $1^D$ is equivalent to Mode $1^B$ of BLC B. The line parameters of $X_{1}^{(D)} - X_{6}^{(D)}$ and $C_{DS}$ can be designed using the Mode $1^B$ design. The designs of $Z_{inD1} = Z_{inD2} = 0$ by

![FIGURE 18. (a) Layout and (b) photograph of BLC C.](image1)

![FIGURE 19. Ideal circuit simulation, full-wave simulation, and measurement magnitude responses of S parameters for (a) Mode $1^C$ and (b) Mode $2^C$.](image2)

![FIGURE 20. Ideal circuit simulation, full-wave simulation, and measurement phase responses of S parameters for (a) Mode $1^C$ and (b) Mode $2^C$.](image3)

![FIGURE 21. Proposed BLC D structure.](image4)
in Mode 2D and $C_{DS}$ in Mode 1D are similar to the designs of $X_{S1}^{(C)}$ and $X_{S2}^{(C)}$ with diodes $D_1^{(C)}$ and $D_2^{(C)}$ in BLC C. Because Mode 1D is equivalent to Mode 1B, Mode 1D is equivalent to a conventional BLC (Fig. 1). In Mode 2D, $Z_{inD1}^{(D)} = Z_{inD2}^{(D)} = 0$, i.e., Points $A_1^{(D)}$ and $A_2^{(D)}$ are short circuits. The even- and odd-mode circuits of Mode 2D are same and equivalent to the Mode 1B odd-mode circuit of BLC B, which is equivalent to the conventional BLC odd-mode circuit of Fig. 2(b). Based on the analysis presented in Section III, the $S$ parameters of (11)–(14) are successfully achieved in Mode 2D, i.e., all signal power is perfectly transferred from Port 1 to Port 2 and the phase of $S_{21}$ is $-45^\circ$ in Mode 2D. The center frequency $f_0 = 1.8$ GHz is operated for BLC D. The related parameters $Z_{S}^{(D)} = 29.55 \Omega$, $\theta_1^{(D)} = 75^\circ$, $\theta_2^{(D)} = 35.36 \Omega$, $\theta_1^{(D)} = 90^\circ$, $Z_2^{(D)} = 55.4 \Omega$, and $\theta_2^{(D)} = 42^\circ$ are obtained using the BLC D design. Fig. 22 presents the layout and photograph of BLC D. The three biasing lines BL-1D, BL-2D, and BL-3D presented in Fig. 22(b) are sourced by $V_{1D}$, $V_{2D}$, and $V_{3D}$ voltages. $V_{1D} - V_{2D} = V_{2D} - V_{1D} = 7.5$ V and $V_{2D} - V_{1D} = V_{1D} - V_{3D} = 7.5$ V are for Mode 1D and Mode 2D, respectively. Figs. 23 and 24 present the magnitude and phase responses of $S$ parameters, wherein each ideal circuit simulation of Mode 2D is for diode loss $R_D = 0 \Omega$ or $R_D = 1 \Omega$. For Mode 1D, the measured insertion losses of $-20 \log |S_{21}|$ and $-20 \log |S_{31}|$ are approximately 3.23 and 3.08 dB at 1.8 GHz, respectively, and the measured −15-dB bandwidth ranges of $|S_{11}|$, $|S_{32}|$, and $|S_{41}|$ are approximately 1.616–1.981, 1.606–1.991, and 1.602–1.966 GHz, respectively. For Mode 2D, the measured insertion loss of $-20 \log |S_{21}|$ is approximately 0.494 dB at 1.8 GHz, and the measured −15-dB bandwidth ranges of $|S_{11}|$, $|S_{32}|$, and $|S_{41}|$ are approximately 1.724–1.941, 1.652–2.612, 1.63–2.755, and 1.627–2.784 GHz, respectively. The measured phases of $S_{S1}$ and $S_{S3}$ are approximately $-91.935^\circ$ and $-182.975^\circ$ at 1.8 GHz in Mode 1D, respectively; the measured phase of $S_{21}$ is approximately $-47.5^\circ$ in Mode 2D. Ideal circuit simulations presented in Figs. 23(a) and 23(b) demonstrate perfect matches in Mode 1D and Mode 2D.

**FIGURE 22.** (a) Layout and (b) photograph of BLC D.

**VI. DESIGN OF PROPOSED BLC E**

Fig. 25 presents BLC E consisting of six transmission lines $X_1^{(E)}$–$X_6^{(E)}$, wherein $\theta_i^{(E)}$ and $Z_i^{(E)}$, $i = 1$ or 2, represented electrical length and characteristic impedance, respectively; shunt to ground capacitors of $C_1^{(E)}$ and $C_2^{(E)}$ capacitances with equal values ($C_1^{(E)} = C_2^{(E)} = C_E$); four open stubs $X_1^{(E)}$–$X_4^{(E)}$, wherein $\theta_i^{(E)}$ and $Z_i^{(E)}$ represented electrical length and characteristic impedance, respectively; and four diodes $D_1^{(E)}$–$D_4^{(E)}$ with each reverse-biased capacitance and forward-biased inductance of $C_D = 0.34$ pF and $L_D = 0.7$ nH, respectively. $Z_{in1}^{(E)}$, $Z_{in2}^{(E)}$, and $Z_{inD1}^{(E)}$–$Z_{inD4}^{(E)}$ are input impedances. BLC E exhibits four operation modes, Mode 1E, in which $D_1^{(E)}/D_2^{(E)}$ is the forward-biased state and $D_3^{(E)}$/$D_4^{(E)}$ is the reverse-biased

**FIGURE 23.** Ideal circuit simulation, full-wave simulation, and measurement magnitude responses of $S$ parameters for (a) Mode 1D and (b) Mode 2D.

**FIGURE 24.** Ideal circuit simulation, full-wave simulation, and measurement phase responses of $S$ parameters for (a) Mode 1D and (b) Mode 2D.

**FIGURE 25.** Proposed BLC E structure.
state; Mode 2\(^E\), in which \(D_1^{(E)}/D_3^{(E)}\) is the reverse-biased state and \(D_2^{(E)}/D_4^{(E)}\) is the forward-biased state; Mode 3\(^E\), in which all of \(D_1^{(E)}/D_3^{(E)}\) are reverse-biased states; and Mode 4\(^E\), in which all of \(D_1^{(E)}/D_3^{(E)}\) are forward-biased states.

Designs of \(X_1^{(E)}, X_6^{(E)}, X_{17}^{(E)}, X_{21}^{(E)}, X_1^{(C)}\), and \(C_2^{(E)}\) in BLC E (Fig. 25) are the same as those of \(X_1^{(C)}, X_4^{(C)}, X_{21}^{(C)}, X_{22}^{(C)}, C_1^{(C)}\), and \(C_2^{(C)}\) in BLC C (Fig. 17), respectively. \(E\) is operated forward- and reverse-biased states, respectively, wherein \(C_{SE} = C_E\) is a capacitance of equivalent shunt to ground capacitor and \(i = 1, 2, 3,\) or 4. The design equations between Part E\(_i\) and Part E\(_2\) of BLC E are equivalent to \(X_2^{(C)}\) and \(X_3^{(C)}\) of BLC C, respectively. \(Z_{inD1}^{(E)} = 0\) and \(Z_{inD2}^{(E)} = \frac{1}{j2\pi f C_E}\), when \(D_1^{(E)}\) is operated forward- and reverse-biased states, respectively, wherein \(C_{SE} = C_E\) is a capacitance of equivalent shunt to ground capacitor and \(i = 1, 2, 3,\) or 4. The design equations between Part E\(_i\) and Part E\(_2\) of BLC E can be derived as follows.

\[
\frac{\pi f_0 Z_{2}^{(E)} C_E + \tan \theta_2^{(E)}}{Z_{2}^{(E)} - (Z_{2}^{(E)})^2 \tan \theta_2^{(E)} \pi f_0 C_E} = \frac{\tan \left(\frac{\theta_2^{(C)}}{2}\right)}{Z_{2}^{(C)} - \tan \theta_2^{(C)}} \quad (23)
\]

\[
Z_{2}^{(E)} \tan \theta_2^{(E)} = Z_{2}^{(C)} \tan \left(\frac{\theta_2^{(C)}}{2}\right) \quad (24)
\]

By substituting \(\theta_2^{(C)} = 79.25^\circ\) and \(Z_2^{(C)} = 50.9\Omega\) of BLC C; \(C_{SE} = C_E = C_C = 0.33\ pF\) and \(f_0 = 1.8\ GHz\) into (23) and (24), \(\theta_2^{(E)} = 36.64^\circ\) and \(Z_2^{(E)} = 56.66\Omega\) are solved. In Mode \(1^E\), \(Z_{inD1}^{(E)} = Z_{inD2}^{(E)} = \infty\) because \(Z_{inD1}^{(E)} = Z_{inD2}^{(E)} = 0\) and \(\theta_1^{(E)} = 90^\circ\), i.e., the loading effect at Port 1 from \(Z_{in1}^{(E)}\) or at Port 4 from \(Z_{in2}^{(E)}\) can be ignored. Part E\(_1\) is equivalent to the \(X_2^{(C)}\) of BLC C and \(C_E = C_C\). Therefore, Mode \(1^E\) is equivalent to Mode \(2^C\) of BLC C, in which all signal power perfectly transfers from Port 1 to Port 4 and the phase of \(S_{41}\) is \(-90^\circ\).

In Mode \(2^E\), \(Z_{inD3}^{(E)} = Z_{inD4}^{(E)} = 0\) (short circuit at Point \(A_1^{(E)}\) or Point \(A_3^{(E)}\)) and \(Z_{inD1}^{(E)} = Z_{inD2}^{(E)}\) are equivalent to the input impedance of a shunt to ground capacitor with \(C_{SE} = C_E = C_C\), and the even- or odd-mode circuit of Mode \(2^E\) is equivalent to the odd-mode circuit of Mode \(1^C\) in BLC C. Because Mode \(1^C\) is equivalent to the conventional BLC, even- and odd-mode circuits of Mode \(2^E\) are equivalent to the odd-mode circuit of the conventional BLC. Therefore, the \(S\) parameters of (11)–(14) can be achieved in Mode \(2^E\). After above BLC E design, all parameters of BLC E have been determined and Mode \(3^E\) is equivalent to Mode \(1^C\) of BLC C, i.e., Mode \(3^E\) is equivalent to the conventional BLC. In Mode \(4^E\), \(Z_{inD1}^{(E)} = 0, i = 1–4\), (short circuits at Point \(A_1^{(E)}\)–Point \(A_4^{(E)}\)), i.e., signals are not transferred between adjacent ports because they are blocked by these short circuits.

Fig. 26 presents the layout and photograph of BLC E. The five biasing lines BL\(_{1E}\), BL\(_{2E}\), BL\(_{3E}\), BL\(_{4E}\), and BL\(_{5E}\) are excited by \(V_{1E}, V_{2E}, V_{3E}, V_{4E}\), and \(V_{5E}\), respectively.

\[
V_{2E} - V_{1E} = V_{1E} - V_{SE} = V_{3E} - V_{4E} = V_{4E} - V_{1E} = 7.5V, \quad V_{1E} - V_{2E} = V_{3E} - V_{1E} = V_{SE} - V_{1E} = V_{1E} - V_{4E} = 7.5V, \quad V_{1E} - V_{2E} = V_{3E} - V_{1E} = V_{1E} - V_{4E} = V_{5E} - V_{1E} = V_{SE} = 7.5V, \quad \text{are for Mode 1}\_E, \text{Mode 2}\_E, \text{Mode 3}\_E, \text{and Mode 4}\_E, \text{respectively. Figs. 27 and 28 present the magnitude and phase responses of 5 parameters, wherein each ideal circuit simulation of Mode 1}\_E, \text{Mode 2}\_E, \text{and Mode 4}\_E \text{is for diode loss} R_D = 0\Omega \text{ or } R_D = 1\Omega. \text{For Mode 1}\_E, \text{the measured insertion loss of } -20\log|S_{41}| \text{is approximately 0.686 dB at 1.8 GHz, and the measured } -15\text{-dB bandwidth ranges of } |S_{11}|, |S_{31}|, |S_{32}|, \text{and } |S_{41}| \text{are approximately 1.631–1.984, 1.678–2.048, 1.617–2.078, and 1.359–2.306 GHz, respectively. In Mode 2}\_E, \text{the measured insertion loss of } -20\log|S_{21}| \text{is approximately 0.66 dB at 1.8 GHz, and the measured } -15\text{-dB bandwidth ranges of } |S_{11}|, |S_{31}|, |S_{32}|, \text{and } |S_{41}| \text{are approximately 1.745–1.919, 1.7–2.34, 1.677–2.577, and 1.68–2.66 GHz, respectively. For Mode 3}\_E, \text{the measured insertion losses of } -20\log|S_{21}| \text{and } -20\log|S_{31}| \text{are approximately 3.27 and 3.13 dB at 1.8 GHz, respectively, and the measured } -15\text{-dB bandwidth ranges of } |S_{11}|, |S_{31}|, |S_{32}|, \text{and } |S_{41}| \text{are approximately 1.638–1.972, 1.614–1.97, and 1.62–1.998 GHz, respectively. For Mode 4}\_E, \text{the measured return loss of } -20\log|S_{11}| \text{is approximately 1.089 dB at 1.8 GHz, and the measured } -15\text{-dB bandwidth ranges of } |S_{21}|, |S_{31}|, |S_{32}|, \text{and } |S_{41}| \text{are approximately 1.586–1.927, 1.434–2.914, 1.475–2.811, and 1.556–1.898 GHz, respectively. The measured phase of } S_{31} \text{is approximately } -87.87^\circ \text{in Mode 1}\_E, \text{the measured phase of } S_{21} \text{is approximately } -49.43^\circ \text{in Mode 2}\_E; \text{the measured phases of } S_{21} \text{and } S_{31} \text{are approximately } -95.7^\circ \text{and } -183.8^\circ \text{at 1.8 GHz in Mode 3}\_E, \text{respectively. Ideal circuit simulations presented in Figs. 27(a)–27(d) demonstrate perfect matches without considering losses of diodes in Mode 1}\_E. \text{Mode 3}\_E \text{and perfect isolation from Port 1 to all other ports in Mode 4}\_E.}

**VII. COMPARISON BETWEEN PROPOSED AND PREVIOUS SWITCHABLE COUPLERS BY USING P-I-N DIODES**

Table 1 presents a comparison between the proposed and previous switchable couplers with p-i-n diodes. The perfect matching and perfect blocking modes are under lossless condition for transmission lines, via holes, and diodes. [7]/[8] and [25] used reverse- and forward-biased states of each
diode to approach off and on states, respectively; however, the reverse-biased capacitance and forward-biased inductance that might degrade the predicted performances were not given a detailed discussion or solution. [12] used an extra capacitor in parallel with p-i-n diode to compensate the undesired inductance; however, the extra capacitor and reverse-biased capacitance of each diode were not considered in the circuit, which could affect the predicted line lengths. Although [26] included the reverse-biased capacitance and forward-biased inductance of each diode in simulation, the capacitance and inductance did not in the design equations, i.e., each diode circuit model was added after following proposed design equations. This design procedure could require time-consuming optimization. Compared with BLC A/B, BLC C/D provided two perfect similar matching design modes; however, they require extra open stubs. The size of BLC C/D is larger than that of BLC A/B. Therefore, a trade-off selection may be required between BLC A/B and BLC C/D. BLC E achieves three perfect matching modes and one perfect blocking mode, which successfully includes complicated diode parasitic effects in the multifunction circuit design. However, compared with BLC C/D, BLC E requires extra two stubs and two diodes, i.e., BLC E needs additional circuit size and costs of elements. There still exists a trade-off selection value between BLC E and BLC C/D. This study including the five circuits in one paper can demonstrate several switching designs of similar BLCs by considering parasitic effects of p-i-n diodes and trade-off designs between the BLCs. Compared with [7], this study gives the detailed design discussion in parasitic resistor, inductor, and capacitor of p-i-n diode for affections of switching BLCs. Besides, systematic and trade-off designs considering parasitic effects are included in the manuscript.

VIII. SWITCHING EXAMPLES USING PROPOSED BLCs

This section demonstrates switching examples using proposed BLCs with signal source at Port 1 of each BLC. BLC C can connect a vertical polarization dipole antenna at each of Ports 2, 3, and 4. For Mode 1^C, the antenna beam pattern can be indicated a certain direction because |S_{21}| = |S_{31}| and the phase difference between S_{21} and S_{31} of BLC C are 3 dB and 90°, respectively, i.e., this mode is a 1 × 2 antenna array. Mode 2^C is an omni-directional antenna at Port 2 and no antenna radiation at Port 2 because |S_{21}| = 1 and |S_{31}| = 0. BLC D can connect a vertical polarization dipole antenna at each of Ports 2 and 3. Mode 1^D is an 1 × 2 antenna array which is similar to Mode 1^C of BLC C switching example. Mode 2^D is an omni-directional antenna at Port 2 and no antenna radiation at Port 2 because |S_{21}| = 1 and |S_{31}| = 0. For BLC E, a horizontal polarization dipole antenna can be connected at Port 4 and a vertical polarization dipole antenna can be connected at each of

|    | BLC A/B | BLC C/D | BLC E |
|----|---------|---------|-------|
| 1^* | 0       | 0       | 0     |
| 2^* | 0       | 0       | 0     |
| 3^* | 0       | 0       | 0     |
| 4^* | 0       | 0       | 0     |
| 5^* | 1       | 2       | 4     |

1*: number of operation modes; 2*: number of perfect matching modes; 3*: number of perfect blocking modes from Port 1 to each other ports; 4*: number of included diode reverse-biased capacitance and forward-biased inductance mode designs; 5*: number of diode; 6*: responses: S for single band and D for dual band.

TABLE 1. Comparison between proposed and previous switchable couplers by using P-i-n Diodes.
Ports 2 and 3. Mode 1E (|S41| = 1 and |S21| = |S31| = 0) is a horizontal polarization omni-directional antenna at Port 4 and no antenna radiations at Ports 2 and 3. Mode 2E (|S21| = 1 and |S31| = |S41| = 0) is a vertical polarization omni-directional antenna at Port 2 and no antenna radiations at Ports 3 and 4. Mode 3E (|S21| = |S31| = 3dB, |S41| = 0, and 90° phase difference between S21 and S31) is an 1 × 2 antenna array and no antenna radiation at Port 4. Mode 4E (|S21| = |S31| = |S41| = 0) has no antenna radiations at Ports 2–4. In other words, two different polarization omni-directional antennas, one 1 × 2 antenna array, and no power for all antennas can be selected for the BLC E switching example. Switching examples of BLC A and BLC B can be similar to those of BLC C and BLC D, respectively, however, the parasitic effects could affect antenna performances.

IX. CONCLUSION
This paper presents five reconfigurable switching BLCs (BLC A to E). BLC A and BLC B use shunt to ground diodes to realize two operation modes. One mode is equivalent to a conventional BLC and the other mode can transfer most signal power from Port 1 to Port 2/4. However, BLC A and BLC B present one mode mismatch problem caused by the forward-biased state non-zero inductances of diodes. To overcome this problem, BLC C and BLC D with sub-loaded diodes successfully exhibit two perfect matching modes in ideal circuit. By using design concepts of BLC C and BLC D, the final coupler proposed is BLC E, which exhibits three perfect matching modes and one perfect blocking mode from Port 1 to the other three ports. All the proposed BLCs are carefully verified for measured and simulated results.

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