CMS Phase-1 pixel detector refurbishment during LS2 and readiness towards the LHC Run 3

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ABSTRACT: The CMS Phase-1 pixel detector was extracted from the underground cavern after the end of the LHC Run 2 in 2019 and has been kept cold to protect the silicon sensors during the long shutdown period (LS2) in 2019–2021. The LHC is now preparing for the next period of data taking, Run 3, which is scheduled to start in spring 2022. The Phase-1 pixel detector was going through a series of refurbishment and repairs this year to improve the quality of the collected data and enhance the detector performance. The innermost barrel pixel layer has been replaced with new modules and features improved front-end readout chips (PROC600v4), token bit manager chips (TBM10d), and circuit boards to rectify the issues discovered in Run 2. The forward pixel detector has been equipped with new cooling inlets for safe handling and features a revised high-voltage power distribution scheme to better match the low-voltage granularity. All the DC-DC converter modules have been replaced with new modules featuring an improved FEAST2.3 ASIC, which is considerably more robust against the Total Ionizing Dose effect and thus prevents them from breaking during operation. Overall, this article will summarize the refurbishment work of the pixel detector during LS2, and highlight the readiness towards the LHC Run 3 after installation and commissioning.

KEYWORDS: Particle tracking detectors, Particle tracking detectors (Solid-state detectors), Large detector systems for particle and astroparticle physics

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1 Introduction

The CMS pixel detector is the innermost sub-detector of the CMS experiment [1]. The pixel detector was upgraded in so-called Phase-1 upgrade, which took place during the long shutdown 1 (LS1) in 2016–2017, and it successfully took data over the period of 2017–2018 during the CERN Large Hadron Collider (LHC) Run 2 [2]. At the time of writing, LHC is in the second long shutdown LS2 (2019–2021). CMS uses this time for maintenance of the detector. To extend its lifetime in the harsh radiation environment of the LHC, the LS2 was used to refurbish the Phase-1 pixel detector.

1.1 CMS Phase-1 pixel detector

The CMS Phase-1 pixel detector is closest to the collision point of the sub-detectors in CMS. It provides excellent spatial particle track information for the CMS detector. The Phase-1 pixel detector has over 124 million readout channels. These channels are distributed over four barrel layers (BPix), and three forward disks (FPix) on each end [2]. The pixel modules have a hybrid design with a silicon sensor connected to 16 front-end readout chips (ROCs). The outgoing data stream is routed on a high density interconnect (HDI) and managed by an ASIC called token bit manager (TBM). The entire readout of a module in the innermost layer (L1) is designed to cope with a particle hit rate of up to 600 MHz/cm².

2 Refurbishments and testing

In BPix, L1 experiences the most radiation damage of all pixel layers. During LHC Run 2 the Phase-1 pixel detector collected data for a recorded integrated luminosity of almost 120 fb⁻¹. Expecting to take twice as much data during the upcoming Run 3 (2022–2025) [3], the fluence in the first pixel layer would exceed the operational limits. The ROCs are designed to withstand a dose of 120 Mrad, but have been tested beyond that [4]. A new L1 was manufactured and installed in the BPix. For this endeavor, the Phase-1 pixel detector was extracted from CMS in 2019 and stored in a cold and dry environment in a clean room. The new installed modules feature improved ROCs called PROC600v4 [4] and TBM ASICs called TBM10d [4], rectifying issues discovered during Run 2. The improved ROCs have better shielding of the calibration pulse injection circuit leading to reduced pixel cross-talk and noise. Moreover, they have an improved time-stamp buffer logic, which
in the past caused timing errors and thus loss of data synchronization. The old TBM suffered from a vulnerability for a specific single event upset (SEU) which required a power cycle of the TBM to recover. The new TBM is guarded against this SEU phenomena. In addition, L1 is equipped with new high voltage cables with better insulation. With the new cables and upgraded power supplies, the reverse bias voltage can be ramped up to over 800 V, compared to 450 V in Run 2. A greater range for the high voltage in combination with a lower noise level helps to operate the modules at a very high efficiency [5] through Run 3. Prior to the L1 installation, the inner modules of the second layer (L2) were easily accessible. Thus, defect inner L2 modules were replaced. Figure 1 shows one half of BPix prepared for the installation of the new first pixel layer.

![Figure 1](image.png)

Figure 1. This picture shows one half of BPix just before the first pixel layer was installed. L1 rests ready for installation in front of layers 2 through 4.

Some of the CO\textsubscript{2} cooling pipes of the FPix were noted to be broken at the connection to the end flanges. Thus, all inlet connections were replaced with a more robust connection system. For FPix it was also possible to harmonize the low and high voltage supply lines. For both BPix and FPix, the controller ASIC on the DC-DC converter boards suffered during Run 2 from radiation induced leakage current in a transistor. This caused charge build-up, damaging the connected chips. All DC-DC converters were replaced with new DC-DC converters featuring an improved and more radiation hard ASIC called FEAST2.3 [4]. Concurrently everything was examined for faulty connections and fixed if needed. A more detailed description of the improvements of the Phase-1 pixel detector can be found in Ref. [4].

All modules were tested after reassembling the BPix in the clean room. The testing procedure involved checking all power connections as well as electrical and optical data streams. After synchronization of the configuration signals with the ROCs was achieved, the ROCs were tested up to a functioning pixel level. These tests were performed first at room temperature and later at around –20°C. As a result of refurbishing, and testing, and resolving issues in the clean room, the fraction of working pixels is again higher than 99.1 % for BPix and 98.5 % for FPix, compared to 93.5 % for BPix and 96.7 % for FPix at the end of Run 2.
3 Installation and checkout

After BPix and FPix were tested in the clean room and ready to be installed, BPix and FPix were moved to the cavern of the CMS experiment located 100 m underground. By design BPix had to be installed as two half barrels, since the beam pipe was already installed at the center of the experiment. The two halves were guided on rails to carefully slide in place without touching the beam pipe or other components of the detector. The reinsertion went without major difficulties and BPix was centered around the beam pipe. All power and high voltage cables, as well as all optical fibers, were connected and BPix was made ready for testing.

After BPix was completely installed a quick checkout was performed. Faulty power supplies had to be exchanged and optical fibers were examined, and cleaned, and non-functional ones replaced with spares. Module testing after facilitating all the connections between BPix and the service cavern showed that the detector did not have any faults due to the moving and installation. After the first checkout of BPix, FPix was installed and commissioned. After commissioning at room temperature was finished, the detector volume was sealed and cooled down to about \(-20^\circ C\). After extensive testing up to the functioning pixel level, the fraction of working pixels stayed to be larger than 99.1% for BPix and 98.5% for FPix. Soon after the first calibrations at cold temperature, large amount of data with over 3.5 million cosmic particle tracks was recorded with the refurbished detector.

In the second half of October 2021, the pixel detector successfully measured the first collision data at the LHC injection energy after extensive calibration of thresholds and other pixel operation parameters.

References

[1] CMS collaboration, *The CMS experiment at the CERN LHC*, 2008 JINST 3 S08004.

[2] CMS collaboration, *CMS technical design report for the pixel detector upgrade*, Tech. Rep., CERN-LHCC-2012-016, CERN, Geneva, Switzerland (2012) [CMS-TDR-11].

[3] CERN, *Long term LHC schedule*, https://lhc-commissioning.web.cern.ch/schedule/LHC-long-term.htm, last update: Jan. 2022, accessed: Mar. 2022.

[4] The Tracker Group of the CMS collaboration, *The CMS Phase-1 pixel detector upgrade*, 2021 JINST 16 P02027.

[5] T. Rohe et al., *Fluence dependence of charge collection of irradiated pixel sensors*, Nucl. Instrum. Meth. A 552 HRPPUI RSR [physics/0411214]