Theory and design of phase-inverted balanced coupled-line DC-blocker

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Abstract: A planar DC-blocker suitable for differential mode signalling applications is designed and fabricated. The theory of this component is explained in a new form which utilises the wave scattering transfer matrix. The proposed interpretation of the transfer matrix is most suitable for series (cascade) elements like DC-blockers. In addition to the theoretical enhancement, design of a compressed balanced DC-blocker inserted through a shielded broadside coupled stripline (SBCSL) transmission line (TL) is presented. The return loss of better than 10 dB is obtained at 50-ohm differential-mode input ports of the fabricated DC-blocker in the entire frequency range of 5.6–8.4 GHz. The other achievement of this paper is design and fabrication of a wideband substrate-integrated waveguide (SIW)-mediated balun structure for single-ended measurement of a balanced SBCSL component. The fabricated balun exhibits a nearly perfect coaxial-mode to coupled-stripline differential-mode conversion in the full range of 5–9 GHz. The presented balun is successfully utilised to derive the scattering parameters (S-parameters) of the fabricated balanced SBCSL DC-blocker.

1 Introduction

Theory of planar multi-conductor transmission lines (TLs) and coupled-line circuit elements are well established for the decades [1–3]. So far, various realisations for filters, directional couplers, baluns etc. based on coupled-line elements have been proposed [4]. The series DC-blocking is a task well suited for coupled-line structures since the structure is wideband due to the intrinsic travelling wave effect of coupled lines [4]. Beside the coupled-line realisation, there exist other DC-blocking solutions: like discrete lumped capacitors for printed circuit boards (PCBs) and metal finger capacitors or metal-insulator-metal (MIM) capacitors for ICs [5–7]. At low frequencies, the lumped capacitors are used due to their small size. However, at higher frequencies, the coupled-line DC-blockers exhibit lower losses, thus they are preferable [4]. In addition, for applications like transformer coupling of cascaded IC circuit stages [8–9], one can modify coupled-line DC-blockers in order to provide extra functionalities such as phase inversion, impedance matching, and so on. Successful demonstration of transformer coupled active ICs for millimeter-wave applications can be found in the recent papers [10–13]. In this sense, a modified phase-inverted DC-blocker can be approximately seen as a unit-ratio transformer which can be utilised as an interface of two cascaded active stages with the same characteristic impedances (Fig. 1).

Previously, theory of design and operation of conventional coupled-line DC-blockers have been explained in terms of even and odd modes characteristic impedances [2, 4]. Here, using the TL capacitance and inductance matrices, we present an alternative derivation based on the wave scattering transfer matrices. This derivation is mostly fit for cascaded circuits where the wave scattering transfer matrix of the whole circuit is simply obtained by successive multiplication of wave scattering transfer matrices of all stages. The derivation of overall wave scattering transfer matrix of a multi-step DC-blocker is covered in section 2. In the next section, we present a phase-inverted DC-blocker for SBCSL structure. Since aspect ratios (AR) of the metallic tracks in a PCB are normally very low [14], obtaining high values of couplings between adjacent metallic traces in a PCB is a difficult task and generally results in extremely close-coupled traces. Our proposed design is a single-layer PCB structure in 5–10 GHz frequency range in which the loose coupling problem is properly solved by use of auxiliary couplings between metallic traces.

The other remarkable contribution of this work is the design of a novel coaxial line-to-SBCSL wideband balun, which we use as an interface for the measurement of the DC-blocker S-parameters. In our proposed balun, we have used a SIW-based interface to solve the problems, which usually appear in the connection of a shielded balanced TL to an unbalanced TL. These problems are namely the undesired radiation (single-frequency or wideband) (Fig. 2a), and the excitation of unwanted resonant modes within the balun structure (Fig. 2b). The former appears if the conductor shielding is truncated, while the latter is normally a consequence of short-end termination of the conductor shielding. In addition, the mentioned SIW interface facilitates the correction of balun phase and amplitude imbalance. This problem exists in balun transitions, which have been designed based on lumped element [14–17] or coupled-line Marchand balun dividers [18–20]. Also, our proposed balun does not require high values of even to odd mode impedances ratio which is necessary in the solution proposed by [21]. The design procedure of the explained balun is also discussed in Section 3. The fabrication and measurement processes are presented in Section 4.

2 Theory improvement

Fig. 3a shows a pair of typical common-ground-coupled traces. The depicted structure if is seen as a four-port network like that of Fig. 3b can be represented by a wave scattering transfer matrix (M_total), using the procedure rigorously explained in Appendix. The input and output power waves are related to each other through M_total by:

$$\begin{align*}
\begin{bmatrix}
\text{Input Amp.} \\
\text{Input Mag.}
\end{bmatrix}
\begin{bmatrix}
\text{Output Amp.} \\
\text{Output Mag.}
\end{bmatrix}
\end{align*}
$$

Fig. 1 Equivalence of a phase inverted DC-blocker to a 1:1 transformer
According to the derivation given in Appendix, $M_{\text{Total}}$ is equivalent to an exponential matrix of the form:

$$M_{\text{Total}} = e^{i\theta[D']^{-1}}$$

where $\theta$ is the coupled-line electrical length and $[D']$ is an involutory matrix (that means $[D'] = [D']^{-1}$) defined by (A12) and (A15) in Appendix, respectively. Now, suppose we left ports (2) and (3) of Fig. 3a open to derive an expression for a wave scattering transfer matrix for a two-port network of Fig. 3c, which is a simple circuit model for a one-stage DC-blocker. After some mathematical manipulation one can find that:

$$\begin{pmatrix} a_i \\ b_i \end{pmatrix} = M_{\text{DC-blocker}} \begin{pmatrix} a_i \\ b_i \end{pmatrix}$$

where

$$M_{\text{DC-blocker}} = \frac{-1/2}{M_{11} + M_{12}} \begin{bmatrix} M_{11} + M_{13} \\ M_{12} + M_{13} \end{bmatrix}_{2 \times 1} \times \begin{bmatrix} M_{22} - M_{42} \\ M_{21} - M_{41} \end{bmatrix}_{2 \times 2} + \begin{bmatrix} M_{12} \\ M_{13} \end{bmatrix}_{2 \times 1}$$

In (4), $(M_{ij})$s are the elements of the $4 \times 4$ matrix $M_{\text{Total}}$. According to (4) and (31), (34) and (39) given in Appendix, $M_{\text{DC-blocker}}$ depends on the operating frequency $(\omega)$, coupled-line section length $(l)$, electromagnetic (EM) wave velocity $(v_{TE})$, the reference impedance $(Z_0)$, and the capacitance per unit length matrix of the coupled-line structure $(C_{\text{cpl}})$. The advantage of using wave scattering transfer matrix as proposed above over conventional impedance matrix notations used in classic references [1,3] is its compatibility with cascaded circuit architecture. For instance, overall $(4 \times 4)$ wave scattering transfer matrix for a multi-step (n-step) DC-blocker is equal to:

$$M_{\text{cascaded}} = M_{\text{Total}}^1 M_{\text{Total}}^2 \cdots M_{\text{Total}}^n$$

or

$$M_{\text{cascaded}} = e^{i\theta[D'_1]} \times e^{i\theta[D'_2]} \cdots e^{i\theta[D'_n]}$$

which can be simply written as

$$M_{\text{cascaded}} = \prod_{k=1}^{n} \left( \cos \theta_k \times I_{4	imes4} + j \sin \theta_k \times [D'_k] \right)$$

Then, the wave scattering transfer matrix of the n-step DC-blocker is simply calculated using (4). It is obvious that all other network parameters (like Z-parameters or S-parameters) can be directly calculated from the derived $M_{\text{DC-blocker}}$. No other network representation, namely the conventional Z-parameters representation, has a simple form of (7) for cascaded circuit architecture when the port number is greater than 2.

### 3 Designs and simulations

#### 3.1 DC-blocker

The simplest equivalent circuit for our proposed SBCSL DC-blocker is shown in Fig. 4a. It consists of two separate similar paths of open-ended cascaded coupled-line sections ($M_{\text{cascaded}}$ s) each connects an input SBCSL conductor trace to an output SBCSL trace. It is seen in the figure that each path comprised of a cascaded connection of five separate four-port networks, where the first, third, and last networks (namely cpl1, cpl2 and cpl3) are coupled-line sections and delay1 and delay2 are isolated delay lines. Since the figure implies that cpl3 and delay2 are rotated copies of cpl1 and delay1, respectively, their corresponding scattering transfer matrices are equal to:

$$M_{\text{Total}}^1 = E_4(M_{\text{Total}}^1)^{-1} E_4$$

$$M_{\text{delay}} = E_4(M_{\text{delay}})^{-1} E_4$$

where

$$E_4 = \begin{bmatrix} 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix}$$

So $4 \times 4$ scattering transfer matrix of the cascaded coupled-line sections is derived as

$$M_{\text{cascaded}} = M_{\text{Total}}^1 \times M_{\text{delay}} \times M_{\text{Total}}^1 \times E_4(M_{\text{delay}})^{-1} E_4$$

In (11), $M_{\text{Total}}^1$ and $M_{\text{Total}}$ are calculated by (2) and $M_{\text{delay}}$ is simply equivalent to
\[ M_{\text{delay}} = \begin{bmatrix} e^{j\theta_1} & 0 & 0 & 0 \\ 0 & e^{j\theta_2} & 0 & 0 \\ 0 & 0 & e^{-j\theta_1} & 0 \\ 0 & 0 & 0 & e^{-j\theta_2} \end{bmatrix} \] (12)

where \( \theta_1 \) and \( \theta_2 \) are the electrical lengths of the depicted delay lines.

The differential mode and common mode equivalent circuits of the DC-blocker are shown in Fig. 4b. It is seen in the figure that in the differential mode, the DC-blocker is approximately equivalent to the series connection of two \( M_{\text{cascaded}} \) networks and a phase-inverter block. \( M_{\text{cascaded}} \) can be derived from \( M_{\text{DC-blocker}} \) using the same procedure that we calculated \( M_{\text{DC-blocker}} \) from \( M_{\text{Total}} \) (look (3) and (4)). Also Fig. 4b illustrates that in the common mode, the DC-blocker is approximately equivalent to the parallel connection of two \( M_{\text{cascaded}} \) networks.

According to (39)–(42) of Appendix cpl1, cpl2 and cpl3 sections are characterised by their electrical lengths (\( \theta_{\text{cpl}} \)), coupling ratios (CRs), matched impedance of the coupled-line sections (\( Z_{\text{cl}} \)), and the reference impedance (\( Z_0 \)). As we later show, the depicted delay lines are added to the structure only for practical issues and they are assumed matched to \( Z_0 \) in our primary design.

Now, we consider the case of unoptimised DC-blocker with design parameters listed in Table 1 (see Fig. 5). According to Fig. 6a (port numbering as Fig. 4b has been applied) such a DC-blocker shows a wideband behaviour around the centre frequency of \( f_0 \) (about 66% of relative bandwidth with return losses of better than 15 dB). The cross-section of a typical realisation of cpl1 and cpl2 with specifications replaced by values in Table 1 for a single-layer PCB is shown in Fig. 6b. As shown in Fig. 6b, the metallic traces should be very close to each other (0.03 mm). This tight spacing of metallic traces is not practically realisable. Even if one can realise this narrow gap, there is a high risk of dielectric breakdown in the case of unequal DC voltages of the traces. Also, the unnecessary 1.1-mm traces widths and low 0.7-mm distances from top and bottom shielding are the other disadvantages of this realisation. It should be noted that these constraints are due to the fact that in contrast to the IC realisation which is practically feasible, the PCB realisation has some limitations due to the quasi-TEM wave propagation, which does not have any analytical solution. The even and odd modes of a single-layer PCB coupled-line structure have different effective permittivities and so experience different phase velocities [22].

To avoid the mentioned restrictions, we have designed our DC-blocker in the form illustrated in Fig. 7a. This figure shows a half of the DC-blocker which is a path between the input SBCSL (+) trace and the output SBCSL (-) trace following Fig. 4a definitions. The other half has the same but rotated structure. The figure shows that cpl1 and cpl3 are top-layer and bottom-layer edge-coupled coupled-line structures, respectively. cpl2 is a top-bottom broadside-coupled coupled-line structure which allows the coupling ratio (CR_{cpl2}) to be increased to the desired value. In addition, delay1 consists of two separate delay sections: a top-layer...
trace \( (\theta_d) \), and a connection of a metallised via and a bottom-layer trace \( (\theta_d) \). It is obvious from the figure that this configuration already features the phase inversion property. The design values of the optimised DC-blocker with the configuration of Fig. 7a is listed in Table 2 (see Fig. 5). These values are obtained for the best return loss and common mode rejection performance. It is worth mentioning that a big restriction in our design is the values of \( \theta_d \) which for the sake of feasibility and fabrication limitations cannot be decreased very much. Table 2 shows that the total electrical length of the proposed DC-blocker is approximately 80 degree which is 10 degree smaller than that of a simple quadrature-length structure. Fig. 7b shows the scattering parameters of the optimised design. It is shown that better than 10 dB of return loss is obtained in a 50% of relative bandwidth. Also the common mode rejection level is better than 5 dB in the same frequency band.

The optimised DC-blocker configuration is simulated in Ansoft HFSS (Fig. 8a). It is connected to the input and output SBCSL structures at both sides. The final structure is finely tuned in Ansoft HFSS for the best possible performance. The shown metalised vias complete the outer metallic shield inside the Taconic-30mil-RF35 laminate. The cross-section of the input/output SBCSLs (as illustrated in Fig. 8b) are composed of two broadside-coupled 2.2-mm \( \times \) 70-\( \mu \)m copper traces spaced 2.5 mm from the top and bottom aluminium shields. In this structure, \( Z_0 = 50\, \Omega \) for differential mode propagation. The thorough depiction of the structure in Fig. 8c (compare to the model of Fig. 6b) shows that there is a 0.35-mm air gap between the coupled traces. This is a noticeable modification to the mentioned 0.03 mm. The traces have 0.7 mm widths and spaced 0.5 mm from the auxiliary grounds. Fig. 8c shows that the top and bottom layers are symmetric but mirrored with respect to each other. The shown 1-mm ground vias and 0.7-mm traces vias are both easy to fabricate. There is not any air gap smaller than 0.35 mm in the shown structure. The connecting SBCSL conductor traces of 2.2-mm width are also shown in the figure. The simulated S-parameters of the transition at the input and output 50-ohm SBCSL ports are shown in Fig. 8d. Assuming \( f_s = 7.2 \, \text{GHz} \), the parameters are plotted in the same scale as that of Fig. 7b. The figure implies that the simulated structure shows frequency responses very close to that of the ideal structure. A return loss of better than 15 dB for a bandwidth of 2.8 GHz (39%) and 10 dB for a bandwidth of 3.2 GHz (45%) have been achieved. Also, the common mode rejection level is better than 4 dB in the same 50% of relative bandwidth. The overall length of the transition is 5 mm, which is equal to \( \lambda_g/5 \) at 7.2 GHz.

![Fig. 7 Single-layer PCB realisation of the DC-blocker of Fig. 7a](image)

(a) Our proposed optimised design, (b) Scattering parameters of the optimised design for values listed in Table 2

| \( Z_{CL1} \) | \( Z_{CL2} \) | \( CR_{p1} \) | \( CR_{p2} \) | \( \theta_{p1} \) | \( \theta_{p2} \) | \( \theta_c \) | \( \theta_d \) |
|---|---|---|---|---|---|---|---|
| 100 \( \Omega \) | 65 \( \Omega \) | 0.3 | 0.75 | — | 12° | 22.4° |

![Fig. 8 Optimised DC-blocker](image)

(a) Single-layer PCB realisation of the component for SBCSL structure, (b) Input and output SBCSL structures cross sections, (c) Detailed specifications of the transition, (d) Scattering parameters based on the ports definition of Fig. 7b

**IET Microw. Antennas Propag., 2019, Vol. 13 Iss. 8, pp. 1188-1197**

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Means of balun transitions and coax-to-SIW connectors

For the measurement of the balanced DC-blocker

3.2 SIW-mediated balun

For the measurement of the balanced DC-blocker S-parameters, we have designed a wideband SIW-mediated balun. This component is expected to properly transform the unbalanced coaxial TEM single-ended mode into the balanced SBCSL quasi-TEM differential mode. The proposed balun configuration is illustrated in Fig. 5a. It simply consists of a coaxial-to-SIW and SIW-to-SBCSL transitions. The main role of the intermediate SIW section is to electrically connect all SBCSL conductors together, namely (+), (−) and the shielding. The SBCSL structure is composed of two copper traces printed on the top and bottom layers of a Taconic RF-35-30 mil laminate (with εr = 3.5 and tanδ = 0.0018), while the whole PCB is surrounded by two aluminium lids (Fig. 5b). The transition contains of two slots on the top and bottom layers, which gradually transforms the SIW guiding mode into the differential mode of the SBCSL. Since the slots are entirely covered by the aluminium plates air cavities, there will be no chance for any radiation loss mechanisms. Also, due to the very small height of the cavities, no resonant modes are excited and probable reflections or total power reflections are all entirely eliminated. It is worth to mention that, the top and the bottom copper layers of the PCB have identical patterns. The dimensions of the SBCSL TL are chosen similar to those of the DC-blocker of Fig. 8a. Also, the dimensions of the SIW (like SIW width ≈ 18 mm) are chosen in such a way that in the entire frequency range of 5.6–8.8 GHz (which is our desired transition band), it operates in its single-mode condition. The detailed dimensions of the transition (PCB and aluminium lids) are found in Fig. 5a. In this figure, it is seen that the transition slots are placed inside 0.4 mm × 6 mm × 23.2 mm top and bottom cavities. The total length of the transition is about 13 mm. The S-parameters of the transition between the SIW and the SBCSL ports (highlighted in Fig. 5b) are plotted in Fig. 9a which is designed and simulated in Ansoft HFSS. As can be seen from slightly above the SIW cut-off frequency (4.7 GHz), the return loss exceeds 20 dB and remains above this value in the entire SIW single-mode band. The S21 and S11 figures show no signs of radiation losses or total power reflections or resonant-like behaviour. A completely flat response for S21 is achieved above 5 GHz which is definitely novel in the literature. The E-field intensity distribution is plotted in the same figure, which shows proper transition of the EM wave inside the structure. Also, the E-field vector distribution at the symmetry plane shows that the transition has properly excited the propagating differential mode of the SBCSL structure. The simulation results of the proposed balun when is used as divider are depicted in Fig. 9b. More than 40 dB of common mode rejection ratio (CMRR) is achieved above 5 GHz. Also, the phase and amplitude imbalance are both less than 0.5% above 5 GHz. The simulations show that the balun has an excellent behaviour as a 180-degree divider, too.

4 Fabrication and measurement

The scattering parameters of the coax-to-SIW transition of Fig. 5a is shown in Fig. 10. The design and optimisation of this transition is based on the CPW-to-SIW transition proposed in [23]. The figure shows that the return loss of better than 28 dB is obtained for this transition in the frequency range of 5.2–8.4 GHz. More to say, |S21| shows a smooth and non-radiative behaviour in the frequency region of interest. Next, for the sake of measurement, the designed coaxial-to-SIW transition, SIW-to-SBCSL balun transition and the SBCSL DC-blocker are all attached together in a series and back-to-back fashion as shown in Fig. 11.

The fabricated circuit is shown in Fig. 12. It consists of a Taconic RF-35 30 mil laminate, which is patterned on both sides. The circuit is assembled on a machined aluminium plate (Bottom plate). Another machined aluminium plate (lid) is placed on top of the PCB and is firmly attached to the PCB and the bottom plate. Also, the bottom side of the PCB and the total assembled structure are shown in the figure. The top lid and the bottom plate construct the required closed cavities for the SBCSL structure, DC-blocker, and the balun transitions. For each S-parameters measurement process, the high-frequency SMA connectors will be attached to the assembly from sidewalls.

Fig. 13a shows the fabricated sample of the structure of Fig. 11. The SIW connecting section length is about 8.5 mm, which is about λ/4 at 6.7 GHz. The top aluminium lid is removed in Fig. 13a for a better illustration. The S-parameters are measured at
the depicted coaxial ports. The measured and simulated results are shown in Fig. 13b. It is seen that the measurement and simulation results have similar behaviour in the entire frequency band. The cut-off frequency and the nulls of $S_{11}$ are excellently predicted in the simulations. Even the upper band frequency responses of both simulation and measurement are approximately similar. Except for a very narrow frequency band around 6.5 GHz, $S_{11}$ is better than 10 dB in 5.6-8.4 GHz for the simulations and measurements. This means the relative bandwidth is 40% for the centre frequency of 7 GHz. Also, the measured insertion loss is <1.6 dB in 5.7-8.4 GHz frequency band in which its difference with that of simulation is <0.4 dB in the entire 5.9-8.4 GHz band.

Since both the DC-blocker and the SIW-based balun transition contribute the results shown in Fig. 13b, we have fabricated an auxiliary calibration kit to separately extract $S$-parameters of each component. This kit (as shown in Fig. 14a) consists of line and through circuits, which are almost identical except for the length of the SBCSL connecting section. Before advancing with the calibration, it is worth looking at the depicted coaxial ports. The measured and simulated results are shown in Fig. 13a. It is seen that the measurement and simulation $S$-parameters are similar. As seen, $S_{11}$ is <0.45 dB in the entire frequency range of 5.2–9.4 GHz. Corresponding to the increase in $S_{11}$ to about ~15 dB, the insertion loss increases to about 0.8 dB around 6.5 GHz. It seems that the fabrication tolerances (specifically within the tapered slot transition area) are responsible for this little difference between the simulation and measurement results.

In the next step, if we call the scattering transfer matrix of the circuit of Fig. 13a $T_{\text{Test}}$, we can easily find that

$$T_{\text{Test}} = T_y T_{\text{blocker}} T_x$$

Since $T_y$ and $T_x$ networks are identical but mirrored, we have

$$T_y = (E_T E_y)^{-1}$$

where

$$E_z = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$$

So, the scattering transfer matrix of the transition is calculated as

$$T_{\text{blocker}} = T^{-1}_x T_{\text{Test}} E_z T_x E_z$$

The corresponding curves ($S_{\text{blocker}}$) are depicted in Figs. 16a and b. The overall behaviours of simulation and measurement $S$-parameters are similar. As seen, $S_{11}$ is <−10 dB in the whole region of 5.6–8.4 GHz (40% of equivalent relative bandwidth). Also, the insertion loss is better than 1.5 dB in the same frequency band and better than 1 dB in 5.9–8.4 GHz (about 1/3 of relative bandwidth). The difference between $S_{11}$ of simulated and that of measured is <0.5 dB in 5.6–8.4 GHz. The small increase in the difference of the simulated and measured insertion losses are due to the fact that the attenuation constant which is derived from the applied calibration method is extremely sensitive to the precision of the measurement process. So, even very small errors in the measured values have noticeable effects on the calculated attenuation constant. Actually, for this error to be significantly
suppressed, we need to use several different length line circuits and implement the procedure presented in [25], which is out of the scope of this paper. Summarily, the fabricated DC-blocker presents an acceptable performance in 5.6–8.2 GHz which is approximately a 1/3 octave frequency region. Since according to Fig. 8c, its total length is only 5 mm or approximately λg/5 @ 7 GHz (λg ≈ 2.5 cm @ 7 GHz for the SBCSL differential mode) this component can be easily used where a compressed phase-inverted differential mode DC-blocker is required. A short comparison of the proposed component to some other DC blocking solutions is presented in Table 3. It is seen that the phase inversion functionality is only present in this work. Also, none of the other solutions have been designed for balanced TLs. Except for the ATC capacitor, the smallest feature size of our DC-blocker is much bigger than those of other solutions. In terms of the operational bandwidth, the ATC capacitor and the quarter-wave coupled-line have the best performance, but in the expense of cost and requirement of separate mounting phase in the former and very narrow gap size and feature size in the latter. In addition, the overall dimensions of the presented solutions are approximately in a same order of magnitude. Finally, the ATC capacitor has the best performance in terms of its insertion loss.

5 Conclusion
Here, we first proposed a wave transfer matrix representation for a coupled-line configuration. We expressed the superiority of this method over other solutions for cascade circuit architecture. Then using the mentioned matrix representation, we proposed a compact coupled-line DC-blocker with built-in phase inversion capability for 5–10 GHz applications. However, our fabricated microwave DC-blocker can be redesigned for example for multi hundreds gigahertz IC applications, using the idea of spiral-form-coupled structures, which has been previously reported by authors [29, 30]. In addition to the mentioned DC-blocker, a very wideband SIW-based coax-to-SBCSL balun transition was proposed which was successfully used for the measurement of the fabricated DC-blocker. Our measurement results show that both the DC-blocker
Table 3: Comparison of our proposed DC-blocker with some other available solutions

| DC-blocker type               | Dimensions | Smallest feature size | 10 dB return loss bandwidth | Insertion loss | Single-phase fabrication | Balanced configuration | Phase inversion |
|------------------------------|------------|-----------------------|-----------------------------|----------------|--------------------------|------------------------|------------------|
| quarter-wave coupled-line     | λg/5 × λg/4 | 70                    | 100%                        | 0.5 dB         | yes                      | no                     | no               |
| interdigital capacitor       | λg/5 × λg/4 | 200                   | 33%                         | 0.5 dB         | yes                      | no                     | no               |
| ATC 800b capacitor            | λg/9 × λg/6 | —                     | 100%                        | 0.4 dB         | no                       | no                     | no               |

This work λg/5 × λg/4 35% 1 dB yes yes yes

and the balun transition can be used for differential signalling applications.

6 Acknowledgments
The authors would like to thank Iran National Scientific Foundation (INSF) for financial supporting this research work. The authors also would like to thank Mr. Al}
\[
\begin{bmatrix}
\alpha_i \\
\beta_i \\
\gamma_i \\
\delta_i
\end{bmatrix} = M_{\text{element}} \begin{bmatrix}
\alpha_i \\
\beta_i \\
\gamma_i \\
\delta_i
\end{bmatrix}
\]  
(26)

Equation (20) to (26) result in the following relation for \( M_{\text{element}} \):

\[
\begin{aligned}
M_{\text{element}} &= I_{x \times 4} - \frac{a_0}{2} \left[ I_{x \times 2} \right] \left[ C_a \right] \left[ I_{x \times 2} \right] \\
&\quad + \frac{j \omega}{2} \left[ Z_0 \left[ I_{x \times 2} \right] \left[ C_a \right] \left[ I_{x \times 2} \right] \right] + \frac{1}{a_0} \left[ I_{x \times 2} \right] \left[ L_a \right] \left[ I_{x \times 2} \right] - v_{TL}
\end{aligned}
\]  
(27)

In (27) \( I_{x \times 4} \) represents a 4 \( \times \) 4 identity matrix. (A8) can be simplified since we have assumed an ideal TEM wave transmission along the coupled-line structure. This assumption (which is a good approximation for the case of PCB and IC transmission line structures) has an important outcome: Both the scalar electric potential and longitudinal part of the vector magnetic potential satisfy Laplace's equation. It means that if we define a capacitance per unit length matrix \( \left[ C_a \right] \) and an inductance per unit length matrix \( \left[ L_a \right] \) for the coupled-line structure, these two matrices are related to each other by

\[
\left[ L_a \right] = \frac{1}{v_{TL}^2} \left[ C_a \right]^{-1}
\]  
(28)

where \( v_{TL} \) is the velocity of EM wave propagation along our transmission line. These matrices are related to \( \left[ C_a \right] \) and \( \left[ L_a \right] \) by

\[
\left[ C_a \right] = \frac{\left[ C_a \right]}{l}
\]  
(29)

\[
\left[ L_a \right] = \frac{\left[ L_a \right]}{l}
\]  
(30)

where \( l \) is the total length of the coupled-line section and \( \frac{l}{n} \) is the infinitesimal length associated with the coupled-line element of Fig. 17a. Using (28)–(30) and by defining the electrical length parameter \( \theta \) as

\[
\theta = \frac{a_0 l}{v_{TL}}
\]  
(31)

Equation (27) can be rewritten as:

\[
M_{\text{element}} = I_{x \times 4} - \left( \frac{\theta}{n} \right) [D'] + \left( \frac{\theta}{n} \right) \| [D']\|
\]  
(32)

where

\[
[D'] = \left[ \begin{array}{cc}
I_{x \times 2} & I_{x \times 2}
\end{array} \right]
\]  
(33)

We consider the circuit of Fig. 17a as a four-port network of Fig. 17b and assign a four-dimensional wave scattering transfer matrix \( M_{\text{element}} \) to it, as

\[
\begin{bmatrix}
\alpha_i \\
\beta_i \\
\gamma_i \\
\delta_i
\end{bmatrix} = M_{\text{element}} \begin{bmatrix}
\alpha_i \\
\beta_i \\
\gamma_i \\
\delta_i
\end{bmatrix}
\]  
(26)

We can look at the coupled-line section as a \( \| [C_a] \| \) or \( \| [L_a] \| \) in the style depicted in Fig. 18. This characteristic is useful in Taylor series representation of \( M_{\text{Total}} \):
where $Z_{0o}$ and $Z_{0e}$ are odd and even impedances of the coupled-line structure and $C_1$ and $C_M$ are related to $\{C_o\}$ by (23) and (29) and CR is the coupling ratio of the quarter-wavelength couple-line structure if used as a directional coupler in the configuration of Fig. 19. By some mathematical manipulation, we obtain:

$$\left[D\right] = \frac{1}{2\sqrt{1-\text{CR}}} \times \left( \begin{array}{cc} \{Z_o\} & \{I_{x2}\} \\ \{Z_{CL}\} & \{I_{x2}\} \end{array} \right) \left( \begin{array}{cc} 1 & -\text{CR} \\ -\text{CR} & 1 \end{array} \right) \left( \begin{array}{cc} \{I_{x2}\} & \{I_{2x2}\} \\ \{I_{x2}\} & \{-I_{2x2}\} \end{array} \right)$$

By this interpretation $M_{\text{Total}}$ can be directly expressed in terms of $\theta$, CR and $Z_0/Z_{CL}$ using (39).

Fig. 19  Pair of quarter-wavelength couple-line as a directional coupler