Adaptive-Latency DRAM: Reducing DRAM Latency by Exploiting Timing Margins

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This paper summarizes the idea of Adaptive-Latency DRAM (AL-DRAM), which was published in HPCA 2015 \cite{90}, and examines the work’s significance and future potential. AL-DRAM is a mechanism that optimizes DRAM latency based on the DRAM module and the operating temperature, by exploiting the extra margin that is built into the DRAM timing parameters. DRAM manufacturers provide a large margin for the timing parameters as a provision against two worst-case scenarios. First, due to process variation, some outlier DRAM chips are much slower than others. Second, chips become slower at higher temperatures. The timing parameter margin ensures that the slow outlier chips operate reliably at the worst-case temperature, and hence leads to a high access latency.

Using an FPGA-based DRAM testing platform, our work first characterizes the extra margin for 115 DRAM modules from three major manufacturers. The experimental results demonstrate that it is possible to reduce four of the most critical timing parameters by a minimum/maximum of 17.3%/54.8% at 55\textdegree C while maintaining reliable operation. AL-DRAM uses these observations to adaptively select reliable DRAM timing parameters for each DRAM module based on the module’s current operating conditions. AL-DRAM does not require any changes to the DRAM chip or its interface; it only requires multiple different timing parameters to be specified and supported by the memory controller. Our real system evaluations show that AL-DRAM improves the performance of memory-intensive workloads by an average of 14\% without introducing any errors.

Our characterization and proposed techniques have inspired several other works on analyzing and/or exploiting different sources of latency and performance variation within DRAM chips \cite{30,34,51,71,73,75,76,77,78,88,89,90,92,93,97,98,127,146,147}.

1. Problem: High DRAM Latency

A DRAM chip is made of capacitor-based cells that represent data in the form of electrical charge. To store data in a cell, charge is injected, whereas to retrieve data from a cell, charge is extracted. Such movement of charge happens through a wire called bitline. Due to the large resistance and the large capacitance of the bitline, it takes a long time to access DRAM cells. To guarantee correct operation for every module sold, DRAM manufacturers impose a set of minimum latency restrictions on DRAM accesses, called timing parameters \cite{60}. Ideally, timing parameters should provide just enough time for a DRAM chip to operate correctly. In practice, however, there is a very large margin in the timing parameters to ensure correct operation under worst-case conditions with respect to two aspects. First, due to process variation, some outlier cells suffer from a larger RC-delay than other cells \cite{64,94}, and require more time to be accessed. Second, due to temperature dependence, DRAM cells lose more charge at high temperature \cite{97,171}, and therefore require more time to be accessed. Due to the worst-case provisioning of the fixed timing parameters, which ensure reliable operation up to a temperature of 85\textdegree C, it takes a longer time to access most of DRAM under most operating conditions than is actually necessary for correct operation.

2. Key Observations and Our Goal

First, we observe that most DRAM chips do not contain the worst-case cells that require the largest access latency. Using an FPGA-based testing platform \cite{52}, we profile 115 real DRAM modules and observe that the slowest cell (i.e., the cell that stores the smallest amount of charge) for a typical chip is still significantly faster than the slowest cell of the worst-case chip. Our profiling exposes the large margin built into DRAM timing parameters. In particular, we identify four timing parameters that are the most critical during a DRAM access: tRCD, tRAS, tWR, and tRP.\textsuperscript{1} At 55\textdegree C, we demonstrate that the parameters can be reduced by an average of 17.3\%, 37.7\%, 54.8\%, and 35.2\%, respectively, while still maintaining correctness.

Second, we observe that most DRAM chips are not exposed to the worst-case temperature of 85\textdegree C. We measure the DRAM ambient temperature in a server cluster running a very memory-intensive benchmark, and find that the temperature never exceeds 34\textdegree C, and never changes by more than 0.1\textdegree C per second. Other works \cite{48,99} also observe that worst-case DRAM temperatures are not common, and that servers typically operate at much lower temperatures \cite{48,99}.

Based on these two observations, we show that typical DRAM chips operating at typical temperatures (e.g., 55\textdegree C) are capable of operating correctly when accessed with a much smaller access latency, but are nevertheless forced to operate

\textsuperscript{1}For a detailed background on the operation of DRAM, and an explanation of each timing parameter, we refer the reader to our prior works \cite{30,31,32,34,51,52,67,68,69,70,71,73,75,76,77,78,88,89,90,92,93,97,98,127,146,147}.
at the largest latency of the worst-case module and operating conditions. Modules in existing systems use these worst-case latencies because existing memory controllers are equipped with only a single set of timing parameters that are dictated by the worst case.

Our goal in our HPCA 2015 paper [90] is to exploit the extra margin that is built into the DRAM timing parameters to reduce DRAM latency, and thus improve performance as well as energy consumption. To this end, we first provide a detailed analysis of why we can reduce DRAM timing parameters without sacrificing reliability.

3. Charge & Latency Interdependence

The operation of a DRAM cell is governed by two important parameters: i) the quantity of charge and ii) the latency it takes to move charge. These two parameters are closely related to each other. Based on SPICE simulations with a detailed DRAM model, we identify the quantitative relationship between charge and latency [90]. We briefly summarize our three key observations from these analyses here. Section 7 of our HPCA 2015 paper [90] provides a detailed analysis of our observations.

First, having more charge in a DRAM cell accelerates the sensing operation in the cell, especially at the beginning of sensing, enabling the opportunity to shorten the timing parameters that correspond to sensing (tRCD and tRAS). Second, when restoring the charge in a DRAM cell, a large amount of the time is spent on injecting the final small amount of charge into the cell. If there is already enough charge in the cell for the next access, the cell does not need to be fully restored. In this case, it is possible to shorten the latter part of the restoration time, creating the opportunity to shorten the timing parameters that correspond to restoration (tRAS and tWR). Third, at the end of precharging, i.e., setting the bitline into the initial voltage level (before accessing a cell) for the next access, a large amount of the time is spent on precharging the final small amount of bitline voltage difference from the initial level. When there is already enough charge in the cell to overcome the voltage difference in the bitline, the bitline does not need to be fully precharged. Thus, it is possible to shorten the final part of the precharge time, creating the opportunity to shorten the timing parameter that corresponds to precharge (tRP). Based on these three observations, we conclude that timing parameters can be shortened if DRAM cells have enough charge.

4. Adaptive-Latency DRAM

As explained in Section 3, the amount of charge in the cell right before an access to it plays a critical role in how long it takes to retrieve the correct data from the cell. In Figure 1, we illustrate the impact of process variation using two different cells: one is a typical cell (left column) and the other is the worst-case cell that deviates the most from the typical (right column). The worst-case cell initially contains less charge than the typical cell for two reasons. First, due to its large resistance, the worst-case cell cannot allow charge to flow inside quickly. Second, due to its small capacitance, the worst-case cell cannot store much charge even when it is fully charged. To accommodate such a worst-case cell, existing timing parameters are conservatively set to large values.

In Figure 1, we also illustrate the impact of temperature dependence using two cells at two different operating temperatures: i) a typical temperature (55°C, bottom row), and ii) the worst-case temperature (85°C, top row) supported by DRAM standards. Both typical and worst-case cells leak charge at a faster rate at the worst-case temperature. Therefore, not only does the worst-case cell have less charge to begin with, but it is left with even less charge at the worst temperature because it leaks charge at a faster rate (top-right in Figure 1). To accommodate the combined effect of process variation and temperature dependence, existing timing parameters are set to very large values. That is why the worst-case condition for correctness is specified by the top-right of Figure 1, which shows the least amount of charge stored in the worst-case cell at the worst-case temperature in its initial state. On top of this, DRAM manufacturers add an extra latency margin to the access time under worst-case conditions. In other words, the amount of charge in a cell under worst-case conditions is still greater than the minimum amount of charge required for correctness.

If we were to reduce the timing parameters, we would also reduce the amount of charge stored in the cells. It is important to note, however, that we are proposing to exploit only the additional slack (in terms of charge) compared to the worst case. This allows us to provide as strong of a reliability guarantee as manufacturers currently do for worst-case cells and operating conditions. In Figure 1, we illustrate the impact of reducing the timing parameters. The lightened portions inside the cells represent the amount of charge that we are giving up by using reduced timing parameters. Note that we are not giving up any charge for the worst-case cell at the worst-case temperature. Although the other three cells are not fully charged in their initial state, we propose to give up just enough charge from them such that they are left.
with a similar amount of charge as the worst case (top-right). This is because these cells are capable of either holding more charge to begin with (typical cell, left column) or holding their charge for longer (typical temperature, bottom row). Therefore, optimizing the timing parameters (based on the amount of existing charge slack) provides the opportunity to reduce overall DRAM latency while still maintaining the same reliability guarantees provided by DRAM manufacturers.

Based on these observations, we propose Adaptive-Latency DRAM (AL-DRAM), a mechanism that dynamically optimizes the timing parameters for different modules at different temperatures. AL-DRAM exploits the additional charge slack present in the common-case compared to the worst-case, thereby preserving the level of reliability (at least as high as the worst-case) provided by DRAM manufacturers.

5. DRAM Latency Profiling: Experimental Analysis of 115 Modules

We present and analyze the results of our DRAM profiling experiments, performed on our FPGA-based DRAM testing infrastructure, SoftMC [52], which is also used in our various past works analyzing various DRAM characteristics [30,34,68,69,75,89,90,97,136]. In total, we analyze 115 DRAM modules from three major manufacturers, comprising 920 total DRAM chips. Our full methodology is explained in Section 6 of our HPCA 2015 paper [90].

5.1. Analysis of a Representative DRAM Module

We study the possible timing parameter reductions of a DRAM module while still maintaining correctness. To guarantee reliable DRAM operation, DRAM manufacturers provide a built-in safety margin in retention time, also referred to as a guardband [2, 68, 97, 127, 166]. This way, DRAM manufacturers are able to guarantee that even the weakest cell is insured against various other modes of failure. We first measure the safety margin of a DRAM module by sweeping the refresh interval at the worst-case operating temperature (85 °C), using the standard timing parameters. Figure 2a plots the maximum refresh intervals of each bank and each chip in a DRAM module for both read and write operations. We make several observations. First, the maximum error-free refresh intervals of both read and write operations are much larger than the DRAM standard (208 ms for the read and 160 ms for the write operations vs. the 64 ms standard). Second, for the smaller architectural units (banks and chips in the DRAM module), some of them operate without incurring errors even at much higher refresh intervals than others (as high as 352 ms for the read operations and 256 ms for the write operations). This is because the error-free retention time is determined by the worst single cell in each architectural component (i.e., bank/chip/module).

Based on this experiment, we define the safe refresh interval for a DRAM module as the maximum refresh interval that leads to no errors, minus an additional margin of 8 ms, which is the increment at which we sweep the refresh interval. The safe refresh interval for the read and write operations are 200 ms and 152 ms, respectively. We then use the safe refresh intervals to run the tests with all possible combinations of timing parameters. For each combination, we run our tests at two temperatures: 85 °C and 55 °C.

Figure 2b plots the error-free timing parameter combinations (tRCD, tRAS, and tRP) in the read operation test. For each combination, there are two stacked bars — the left bar for the test at 55 °C and the right bar for the test at 85 °C. Missing bars indicate that the test (with that timing parameter combination at that temperature) causes errors. Figure 2c plots same data for the write operation test (tRCD, tWR, and tRP).

We make two observations. First, even at the highest temperature of 85 °C, the DRAM module reliably operates with reduced timing parameters (24% reduction for read, and 35% reduction for write operations). Second, at the lower temperature of 55 °C, the potential latency reduction is even higher (36% for read, and 47% for write operations). These latency reductions are possible while maintaining the safety margin of the DRAM module. From these two observations, we conclude that there is significant opportunity to reduce DRAM timing parameters without compromising reliability.

5.2. Analysis of 115 DRAM Modules

We have studied the effect of temperature and the potential to reduce various timing parameters at different temperatures for a single DRAM module. The same trends and observations...
also hold true for all of the other modules we studied. In this section, we analyze the effect of process variation by studying the results of our profiling experiments on 115 DIMMs. We also present results for intra-chip process variation by studying the process variation across different banks within each DIMM.

Figure 3a (solid line) plots the highest refresh interval that leads to correct operation across all cells at 85°C within each DIMM for the read operation test. The red dots on top show the highest refresh interval that leads to correct operation across all cells within each bank for all 8 banks. Figure 3b plots the same data for the write operation test.

Figure 3: Analysis of 115 modules. Reproduced from [90].

We draw two conclusions. First, although there exist a few modules which just meet the timing parameters (with a low safety margin), a vast majority of the modules very comfortably meet the standard timing parameters (with a high safety margin). This indicates that a majority of the DIMMs have significantly higher safety margins than the worst-case module even at the highest-acceptable operating temperature of 85°C. Second, the effect of process variation is even higher for banks within the same DIMM, explained by the large spread in the red dots for each DIMM. Since banks within a DIMM can be accessed independently with different timing parameters, one can potentially imagine a mechanism that more aggressively reduces timing parameters at a bank granularity and not just the DIMM granularity. We leave this for future work.2

To study the potential of reducing timing parameters for each DIMM, we sweep all possible combinations of timing parameters (tRCD/tRAS/tWR/tRP) for all the DIMMs at both the highest acceptable operating temperature (85°C) and a more typical operating temperature (55°C). We then determine the acceptable DRAM timing parameters for each DIMM for both temperatures while maintaining its safety margin.

Figures 3c and 3d show the results of this experiment for the DRAM read and DRAM write, respectively. The y-axis plots the sum of the relevant timing parameters (tRCD, tRAS, and tRP for the DRAM read and tRCD, tWR, and tRP for the DRAM write). The solid black line shows the latency sum of the standard timing parameters (DDR3 DRAM specification). The dotted red line and the dotted blue line show the most acceptable latency parameters for each DIMM at 85°C and 55°C, respectively. The solid red line and blue line show the average acceptable latency across all DIMMs.

We make two observations. First, even at the highest temperature of 85°C, DIMMs can reliably operate at reduced access latencies: 21.1% on average for read, and 34.4% on average for write operations. This is a direct result of the possible reductions in timing parameters tRCD/tRAS/tWR/tRP = 15.6%/20.4%/20.6%/28.5% on average across all the DIMMs.3 As a result, we conclude that process variation and lower temperatures enable a significant potential to reduce DRAM access latencies. Second, we observe that at lower temperatures (e.g., 55°C) the potential for latency reduction is even greater (32.7% on average for read, and 55.1% on average for write operations), where the corresponding reduction in timing parameters tRCD/tRAS/tWR/ tRP are 17.3%/37.7%/54.8%/35.2% on average across all the DIMMs.

We conclude that existing DRAM modules can be accessed reliably with lower access latencies, especially at lower temperatures than the worst-case temperature specified by DRAM manufacturers.

6. Real-System Evaluation

We evaluate AL-DRAM on a real system that offers dynamic software-based control over DRAM timing parameters at runtime [10, 11]. We use the minimum values of the timing parameters that do not introduce any errors at 55°C for any module to determine the latency reduction at 55°C. Thus, the latency is reduced by 27%/32%/33%/18% for tRCD/tRAS/tWR/tRP, respectively. Our full methodology is described in Section 8 of our HPCA 2015 paper [90].

Figure 4 shows the performance improvement of reducing the timing parameters in the evaluated memory system with one rank and one memory channel at a 55°C operating temperature. We run a variety of different applications in two different configurations. The first one (single-core) runs only one thread, and the second one (multi-core) runs multiple

2Note that our future works [30, 33, 34, 87, 89] explain this observation of latency heterogeneity within a DRAM chip.

3Due to space constraints, we present only the average potential reduction for each timing parameter. However, detailed characterization of each DIMM can be found online at the SAFARI Research Group website [91].
applications/threads. We run each configuration 30 times (only SPEC benchmarks are executed 3 times due to their large execution times), and present the average performance improvement across all the runs and their standard deviation as an error bar. Based on the last-level cache misses per kilo instructions (MPKI), we categorize our applications into memory-intensive or non-intensive groups, and report the geometric mean performance improvement across all applications from each group.

We draw three key conclusions from Figure 4. First, AL-DRAM provides significant performance improvement over the baseline (as high as 20.5% for the very memory-bandwidth-intensive STREAM applications [109]). Second, when the memory system is under higher pressure with multi-core/multi-threaded applications, we observe significantly higher performance (than in the single-core case) across all applications from our workload pool. Third, as expected, memory-intensive applications benefit more in performance than non-memory-intensive workloads (14.0% vs. 2.9% on average). We conclude that by reducing the DRAM timing parameters using AL-DRAM, we can speed up a real system by 10.5% (on average across all 35 workloads on the multi-core/multi-thread configuration).

We also conducted reliability stress tests for our mechanism. We ran our workloads for 33 days without interruption of the lower latencies. We observed no errors and correct results.

7. Other Results and Analyses in Our Paper

Our HPCA 2015 paper [90] includes significant amount of DRAM latency analyses and system performance evaluations. We refer the reader to [90] for detailed evaluations and analyses.

- **Effect of Changing the Refresh Interval on DRAM Latency.** We evaluate DRAM latency at different refresh intervals. We observe that refreshing DRAM cells more frequently enables more DRAM latency reduction (Section 7.1 of our HPCA 2015 paper [90]).

- **Effect of Reducing Multiple Timing Parameters.** We study the potential for reducing multiple timing parameters simultaneously. Our key observation is that reducing one timing parameter leads to decreasing the opportunity to reduce another timing parameter simultaneously (Section 7.2 of our HPCA 2015 paper [90]).

- **Analysis of the Repeatability of Cell Failures.** We perform tests for five different scenarios to determine that a cell failure due to reduced latency is repeatable: i) same test, ii) test with different data patterns, iii) test with timing-parameter combinations, iv) test with different temperatures, and v) DRAM read/write. Most of these scenarios show that a very high fraction (more than 95%) of the erroneous cells consistently experience an error over multiple iterations of the same test (Section 7.6 of our HPCA 2015 paper [90]).

- **Performance Sensitivity Analyses.** We analyze the impact of increasing the number of ranks and channels, executing heterogeneous workloads, using different row buffer policies. We show that AL-DRAM effectively improves performance in all cases (Section 8.4 of our HPCA 2015 paper [90]).

- **Power Consumption Analysis.** We show that AL-DRAM reduces DRAM power consumption by 5.8%. This reduced power consumption is due to the reduced DRAM latencies (Section 8.4 of our HPCA 2015 paper [90]).

8. Related Work

To our knowledge, our HPCA 2015 paper is the first work to i) provide a detailed qualitative and empirical analysis of the relationship between process variation and temperature dependence of modern DRAM devices on the one side, and DRAM access latency on the other side (we directly attribute the relationship between the two to the amount of charge in cells), ii) experimentally characterize a large number of existing DIMMs to understand the potential of reducing DRAM timing constraints, iii) provide a practical mechanism that can take advantage of this potential, and iv) evaluate the performance benefits of this mechanism by dynamically optimizing DRAM timing parameters on a real system using a variety of real workloads.

Several works investigated the possibility of reducing DRAM latency by either exploiting DRAM latency variation or changing the DRAM architecture. We discuss these below.

**DRAM Latency Variation.** Chandrasekar et al. [29] evaluate the potential of relaxing some DRAM timing parameters to reduce DRAM latency. This work observes latency variations across DIMMs as well as for a DIMM at different operating temperatures. However, there is no explanation as to why this phenomenon exists. In contrast, our HPCA 2015 paper [90] (i) identifies and analyzes the root cause of latency variation in detail, (ii) provides a practical mechanism that can relax timing parameters, and (iii) provides a real system evaluation of this new mechanism, using real workloads, showing improved performance and preserved reliability.
NUAT [153] and ChargeCache [51] show that recently-refreshed rows contain more charge, and propose mechanisms to access recently-refreshed rows with reduced latency. Even though some of the observations in these works are similar to ours, the approaches to leverage them are different. AL-DRAM exploits temperature dependence in a DIMM and process variations across DIMMs, while NUAT and ChargeCache use the time difference between a row refresh and an access to the row (hence its benefits are dependent on when the row is accessed after it is refreshed). Therefore, NUAT and ChargeCache are complementary to AL-DRAM, and can potentially be combined for better performance.

Voltron [34] uses an experimental characterization of real DRAM modules to identify the relationship between the DRAM supply voltage and access latency variation. Voltron uses this relationship to identify the combination of voltage and access latency that minimizes system-level energy consumption without exceeding a user-specified threshold for the maximum acceptable performance loss.

Flexible-Latency DRAM (FLY-DRAM) [30] uses an experimental characterization of real DRAM modules to capture access latency variation across DRAM cells within a single DRAM chip due to manufacturing process variation. FLY-DRAM identifies that there is spatial locality in the slower cells, resulting in fast regions (i.e., regions where all DRAM cells can operate at significantly-reduced access latency without experiencing errors) and slow regions (i.e., regions where some of the DRAM cells cannot operate at significantly-reduced access latency without experiencing errors) within each chip. To take advantage of this heterogeneity in the reliable access latency of DRAM cells within a chip, FLY-DRAM (1) categorizes the cells into fast and slow regions; and (2) lowers the overall DRAM latency by accessing fast regions with a lower latency.

Design-Induced Variation-Aware DRAM (DIVA-DRAM) [89] uses an experimental characterization of real DRAM modules to identify the latency variation within a single DRAM chip that occurs due to the architectural design of the chip. For example, a cell that is further away from the row decoder requires a longer access time than a cell that is close to the row decoder. Similarly, a cell that is farther away from the wordline driver requires a larger access time than a cell that is close to the wordline driver. DIVA-DRAM uses design-induced variation to reduce the access latency to different parts of the chip.

Low-Latency DRAM Architectures. Various works [31, 32, 33, 53, 78, 92, 108, 116, 142, 146, 154, 176] propose new DRAM architectures that provide lower latency. Many of these works improve DRAM latency at the cost of either significant additional DRAM chip area (i.e., extra sense amplifiers [108, 142, 154], an additional SRAM cache [53, 176]), specialized protocols [31, 78, 92, 146] or a combination of these. Our proposed mechanism requires no changes to the DRAM chip and the DRAM interface, and hence has almost negligible overhead. Furthermore, AL-DRAM is largely orthogonal to these proposed designs, and can be applied in conjunction with them, providing greater cumulative reduction in latency.

Binning or Overclocking DRAM. AL-DRAM has multiple sets of DRAM timing parameters for different temperatures and dynamically optimizes the timing parameters at runtime. Therefore, AL-DRAM is different from simple binning (performed by manufacturers) or overclocking (performed by end-users; e.g., [58, 126]) that are used to figure out the highest static frequency or lowest static timing parameters for DIMMs.

Other Methods for Lowering Memory Latency. There are many works that reduce overall memory access latency by modifying DRAM, the DRAM-controller interface, and DRAM controllers. These works enable more parallelism and bandwidth [3, 4, 31, 32, 78, 88, 93, 145, 146, 147, 167, 174, 178], reduce refresh counts [66, 68, 70, 97, 98, 136, 164], accelerate bulk operations [32, 145, 146, 147, 148], accelerate computation in the logic layer of 3D-stacked DRAM [5, 6, 14, 15, 50, 54, 55, 72, 100, 129, 173], enable better communication between the CPU and other devices through DRAM [93], leverage DRAM access patterns [51, 153], reduce write-related latencies by better designing DRAM and DRAM control policies [35, 83, 144], reduce overall queuing latencies in DRAM by better scheduling memory requests [12, 13, 38, 46, 49, 56, 59, 61, 65, 76, 77, 84, 85, 86, 96, 109, 110, 111, 112, 120, 121, 125, 129, 141, 152, 159, 160, 161, 162, 163, 177], employ prefetching [9, 28, 36, 37, 42, 44, 45, 47, 84, 113, 114, 115, 119, 122, 124, 128, 158], perform memory/cache compression [1, 7, 8, 39, 41, 43, 130, 131, 132, 133, 134, 151, 165, 168, 175], or perform better caching [67, 137, 138, 149, 150]. Our proposal is orthogonal to all of these approaches and can be applied in conjunction with them to achieve higher latency and energy benefits.

Experimental Studies of DRAM Chips. There are several studies that characterize various errors in DRAM. Many of these works observe how specific factors affect DRAM errors, analyzing the impact of temperature [48] and hard errors [57]. Other works have conducted studies of DRAM error rates in the field, studying failures across a large sample size [95, 106, 143, 155, 156, 157]. There are also works that have studied errors through controlled experiments, usually using FPGA-based DRAM testing infrastructures like SoftMC [52], to investigate errors due to retention time [52, 66, 68, 69, 70, 97, 98, 127, 136], disturbance from neighboring DRAM cells [62, 74, 75, 118], latency variation across/within DRAM chips [29, 30, 33, 87, 89], and supply voltage [33, 34]. None of these works extensively study latency variation across DRAM modules, which we characterize in our work.

9. Significance

Our work on AL-DRAM is the first to extensively characterize and exploit the large access latency variation that exists in modern DRAM devices. In this section, we discuss
the novelty of AL-DRAM and its expected future impact on the community.

9.1. Novelty

We make the following major contributions in our HPCA 2015 paper [90]:

**Addressing a Critical Real Problem, High DRAM Latency, with Low Cost.** High DRAM latency is a critical bottleneck for overall system performance in a variety of modern computing systems [117,123], especially in real large-scale server systems [63,101]. Considering the significant difficulties in DRAM scaling [64,117,118,123], the DRAM latency problem is getting worse in future systems due to process variation. Our HPCA 2015 work [90] leverages the heterogeneity created by DRAM process variation across DRAM chips and system operating conditions to mitigate the DRAM latency problem. We propose a practical mechanism, *Adaptive-Latency DRAM*, which mitigates DRAM latency with very modest hardware cost, and with no changes to the DRAM chip itself.

**Large-Scale Latency Profiling of Modern DRAM Chips.** Using our FPGA-based DRAM testing infrastructure [30,33,34,52,68,69,75,87,89,90,97,127,136], we profile 115 DRAM modules (920 DRAM chips in total) and show that there is significant timing variation between different DIMMs at different temperatures. We believe that our results are statistically significant to validate our hypothesis that the DRAM timing parameters strongly depend on the amount of cell charge. We provide a detailed characterization of each DIMM online at the SAFARI Research Group website [91]. Furthermore, we introduce our FPGA-based DRAM infrastructure and experimental methodology for DRAM profiling, which are carefully constructed to represent the worst-case conditions in power noise, bitline/wordline coupling, data patterns, and access patterns. Such information will hopefully be useful for future DRAM research.

**Extensive Real System Evaluation of DRAM Latency.** We evaluate our mechanism on a real system [10,11] and show that our mechanism provides significant performance improvements. Reducing the timing parameters strips the excessive margin in the electrical charge stored within a DRAM cell. We show that the remaining margin is enough for DRAM to operate reliably. To verify the correctness of our experiments, we ran our workloads for 33 days nonstop, and examined their and the system’s correctness with reduced timing parameters. Using the reduced timing parameters over the course of 33 days, our real system was able to execute 35 different workloads in both single-core and multi-core configurations while preserving correctness and being error-free. Note that these results do not absolutely guarantee that no errors can be introduced by reducing the timing parameters. However, we believe that we have demonstrated a proof-of-concept which shows that DRAM latency can be reduced at no impact on DRAM reliability. Ultimately, DRAM manufacturers can provide the reliable timing parameters for different operating conditions and modules.

9.2. Potential Long-Term Impact

**Tolerating High DRAM Latency by Exploiting DRAM Intrinsic Characteristics.** Today, there is a large latency cliff between the on-chip last level cache and off-chip DRAM, leading to a large performance fall-off when applications start missing in the last level cache. By enabling lower DRAM latency, our mechanism, Adaptive-Latency DRAM, smoothens this latency cliff without adding another layer into the memory hierarchy.

**Applicability to Future Memory Devices.** We show the benefits of the common-case timing optimization in modern DRAM devices by taking advantage of intrinsic characteristics of DRAM. Considering that most memory devices adopt a unified specification that is dictated by the worst-case operating condition, our approach that optimizes device latency for the common case can be applicable to other memory devices by leveraging the intrinsic characteristics of the technology they are built with. We believe there is significant potential for approaches that could reduce the latency of Phase Change Memory (PCM) [40, 80, 81, 105, 139, 140, 170, 172], STT-MRAM [79, 105], RRAM [169], and NAND flash memory [16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 102, 103, 104, 107].

**New Research Opportunities.** Adaptive-Latency DRAM creates new opportunities by enabling mechanisms that can leverage the heterogeneous latency offered by our mechanism. We describe a few of these briefly.

- **Optimizing the operating conditions for faster DRAM access:** Adaptive-Latency DRAM provides different access latencies for different operating conditions. Future works can explore how the operating conditions themselves can be optimized, which can be used in conjunction with AL-DRAM to further improve the DRAM access latency. For instance, balancing DRAM accesses over multiple DRAM channels and ranks can potentially reduce the DRAM operating temperature, maximizing the benefits provided by AL-DRAM. At the system level, operating the system at a constant low temperature can enable the use of lower DRAM latencies more frequently.

- **Optimizing data placement to reduce overall DRAM access latency:** We characterize the latency variation in different DIMMs due to process variation. Placing data based on this information and the latency criticality of data maximizes the benefits of lowering DRAM latency, by placing the data that is most sensitive to latency in the fastest DRAM chips (and, thus, providing lookups to the data with the fastest access latency).

- **Error correction mechanisms to further reduce DRAM latency:** Error correction mechanisms allow us to lower DRAM latency even further, by correcting bit errors that occur when a small number of the DRAM operations end before the minimum charge is stored in the DRAM cell. Such mechanisms can rely on error correction to compensate for the reduced reliability.
of read and write operations at even lower latencies, leading to a further reduction in DRAM latency without errors. Future research that uses error correction to enable even lower latency DRAM is therefore promising as it opens a new set of trade-offs. Note that our recent work, DIVA-DRAM [89], explores this direction and finds very promising benefits.

Inspired by our characterization and proposed techniques, several recent works [30, 34, 51, 71, 89, 127] have explored many of these new research opportunities, by (1) analyzing different sources of latency and performance variation within DRAM chips, and (2) exploiting these sources of latency and performance variation to reduce access latency and/or energy consumption.

10. Conclusion

This paper summarizes our HPCA 2015 work on Adaptive-Latency DRAM (AL-DRAM), a simple and effective mechanism for dynamically tailoring the DRAM timing parameters for the current operating condition without introducing any errors. AL-DRAM takes advantage of the large latency margin available in the DRAM timing parameters for common-case operation, by dynamically the operating temperature of each DRAM module and employing timing constraints optimized for a particular module at the current temperature. AL-DRAM provides an average 14% improvement in overall system performance across a wide variety of memory-intensive applications run on a real multi-core system. We conclude that AL-DRAM is a simple and effective mechanism to reduce DRAM latency. We hope that our experimental exposure of the large margin present in the standard DRAM timing constraints will inspire other approaches to optimize DRAM chips, latencies, and parameters at low cost.

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References

[1] B. Abali, H. Franko, D. Poff, R. Saccone, C. Schulz, L. Herger, and T. Smith, "Memory Expansion Technology (MXT): Software support and performance," in IBM JRD, 2001.
[2] J.-H. Ahn et al., "Adaptive Self Refresh Scheme for Battery Operated High-Density Mobile DRAM Applications," in ASSCC, 2006.
[3] J. H. Ahn, N. P. Jouppi, C. Koryakos, J. Leverich, and R. S. Schreiber, "Improving System Energy Efficiency with Memory Bank Subsetting," in ACM TACO, 2012.
[4] J. H. Ahn, J. Leverich, R. Schreiber, and N. P. Jouppi, "Multicore DIMM: an Energy Efficient Memory Module with Independently Controlled DRAMs," in IEEE CAL, 2009.
[5] J. Ahn, S. Hong, S. Yoo, O. Mutlu, and K. Choi, "A Scalable Processing-in-Memory Accelerator for Parallel Graph Processing," in ISCA, 2015.
[6] J. Ahn, S. Yoo, O. Mutlu, and K. Choi, "DIM-Enabled Instructions: A Low-Overhead, Locality-Aware Processing-in-Memory Architecture," in ISCA, 2015.
[7] A. R. Alamledeen and D. A. Wood, "Adaptive Cache Compression for High-Performance Processors," in ISCA, 2004.
[8] A. R. Alamledeen and D. A. Wood, "Frequent Pattern Compression: A Significance-Based Compression Scheme for L2 Caches," Univ. of Wisconsin-Madison, Computer Sciences Dept., Tech. Rep. 1500, 2004.
[9] A. Alamledeen and D. Wood, "Interactions Between Compression and Prefetching in Chip Multiprocessors," in HPCA, 2007.
[10] AMD, AMD Opteron 4300 Series processors, http://www.amd.com/en-us/products/server/4000/4300.
[11] AMD, "BBRD for AMD Family 16h Models 06h-0Fh Processors," 2013.
[12] R. Ausavarungnirun, K. Chang, L. Subramanian, G. H. Loh, and O. Mutlu, "Staged memory scheduling: achieving high performance and scalability in heterogeneous systems," in ISCA, 2012.
[13] R. Ausavarungnirun, S. Ghose, O. Kayiran, G. H. Loh, C. R. Das, M. T. Kandemir, and O. Mutlu, "Exploiting Inter-Warp Heterogeneity to Improve GPGPU Performance," in PACT, 2015.
[14] A. Boroumand et al., "Google Workloads for Consumer Devices: Mitigating Data Movement Bottlenecks," in ASPLOS, 2018.
[15] A. Boroumand, S. Ghose, B. Lucia, K. Hsieh, K. Malladi, H. Zheng, and O. Mutlu, "LazyPIM: An Efficient Cache Coherence Mechanism for Processing-in-Memory," in IEEE CAL, 2016.
[16] Y. Cai, S. Ghose, E. F. Haratsch, Y. Luo, and O. Mutlu, "Error Characterization, Mitigation, and Recovery in Flash Memory-Based Solid-State Drives," in Proceedings of the IEEE, 2017.
[17] Y. Cai, S. Ghose, E. F. Haratsch, Y. Luo, and O. Mutlu, "Error Characterization, Mitigation, and Recovery in Flash Memory Based Solid-State Drives," arXiv:1706.08642 [cs.AR], 2017.
[18] Y. Cai, S. Ghose, E. F. Haratsch, Y. Luo, and O. Mutlu, "Errors in Flash-Memory-Based Solid-State Drives: Analysis, Mitigation, and Recovery," arXiv:1711.11427 [cs.AR], 2017.
[19] Y. Cai, S. Ghose, Y. Luo, K. Mai, O. Mutlu, and E. F. Haratsch, "Vulnerabilities in MLC NAND Flash Memory Programming: Experimental Analysis, Exploits, and Mitigation Techniques," in HPCA, 2017.
[20] Y. Cai, E. F. Haratsch, O. Mutlu, and K. Mai, "Error Patterns in MLC NAND Flash Memory: Measurement, Characterization, and Analysis," in DATE, 2012.
[21] Y. Cai, E. F. Haratsch, O. Mutlu, and K. Mai, "Threshold voltage distribution in MLC NAND flash memory: Characterization, analysis, and modeling," in DATE, 2013.
[22] Y. Cai, Y. Luo, S. Ghose, and O. Mutlu, "Read Disturb Errors in MLC NAND Flash Memory: Characterization, Mitigation, and Recovery," in ISDN, 2015.
[23] Y. Cai, Y. Luo, E. Haratsch, K. Mai, and O. Mutlu, "Data retention in MLC NAND flash memory: Characterization, optimization, and recovery," in HPCA, 2015.
[24] Y. Cai, O. Mutlu, E. F. Haratsch, and K. Mai, "Program Interference in MLC NAND Flash Memory: Characterization, Modeling, and Mitigation," in ICCD, 2013.
[25] Y. Cai, G. Yalcin, O. Mutlu, E. Haratsch, A. Cristal, O. Unsal, and K. Mai, "Flash correct-and-reflash: Retention-aware error management for increased flash memory lifetime," in ICCD, 2012.
[26] Y. Cai, G. Yalcin, O. Mutlu, E. F. Haratsch, A. Cristal, O. Unsal, and K. Mai, "Error Analysis and Retention-Aware Error Management for NAND Flash Memory," in IIT, 2013.
[27] Y. Cai, G. Yalcin, O. Mutlu, E. F. Haratsch, O. Unsal, A. Cristal, and K. Mai, "Neighbor-cell Assisted Error Correction for MLC NAND Flash Memories," in SIGMETRICS, 2014.
[28] P. Cao, E. W. Felten, A. R. Karlin, and K. Li, "A Study of Integrated Prefetching and Caching Strategies," in SIGMETRICS, 1995.
[29] K. Chandrasekhar, S. Goossens, C. Weiss, M. Koedam, B. Akesson, N. Wehn, and K. Goossens, "Exploiting Expendable Process-margin in DRAMs for Run-time Performance Optimization," in DATE, 2014.
[30] K. Chang, A. Kashyap, H. Hassan, S. Khan, K. Hsieh, D. Lee, S. Ghose, P. Gkelmanen, T. Li, and O. Mutlu, "Understanding Latency Variation in Modern DRAM Chips: Experimental Characterization, Analysis, and Optimization," in SIGMETRICS, 2016.
[31] K. Chang, D. Lee, Z. Chihi, A. Alamledeen, C. Wilkerson, Y. Kim, and O. Mutlu, "Improving DRAM performance by parallelizing refreshes with accesses," in HPCA, 2014.
[32] K. Chang, P. J. Nair, S. Ghose, D. Lee, M. K. Qureshi, and O. Mutlu, "Low-Cost Inter-Linked Subarrays (LLS): Enabling Fast Inter-Subarray Data Movement in DRAM," in HPCA, 2016.
[33] K. K. Chang, "Understanding and Improving Latency of DRAM-Based Memory Systems," Ph.D. dissertation, Carnegie Mellon University, 2017.
[34] K. K. Chang, A. G. Yaglckci, A. Agrawal, N. Chatterjee, S. Ghose, A. Kashyap, H. Hassan, D. Lee, M. O'Connor, and O. Mutlu, "Understanding Reduced-Voltage Operation in Modern DRAM Devices: Experimental Characterization, Analysis, and Mechanisms," in SIGMETRICS, 2017.
[35] N. Chatterjee, N. Muralimanohar, R. Balasubramonian, A. Davis, and N. P. Jouppi, "Staged Reads: Mitigating the Impact of DRAM Writes on DRAM Reads," in HPCA, 2012.
[36] R. Cooksey, S. Jourdan, and D. Grunwald, "A Stateless, Content-directed Data Prefetching Mechanism," in ASPLOS, 2002.
[37] F. Dahlgren, M. Dubois, and P. Stenstrom, "Sequential Hardware Prefetching in Shared-Memory Multiprocessors," in IEEE TPDS, 1995.

[38] R. Das, R. A. Mangharam, O. Mutlu, A. Kumar, and M. Azimi, "Application-to-core mapping policies to reduce memory system interference in multi-core systems," in HPCA, 2013.

[39] R. de Castro, A. Lago, and M. Silva, "Adaptive compressed caching: design and implementation," in SRAC-PAD, 2003.

[40] G. Dhiman, R. Ayoub, and T. Rosing, "PDRAM: A hybrid PRAM and DRAM main memory system," in DAC, 2009.

[41] F. Dougall, "The Compression Cache: Using On-Line Compression to Extend Physical Memory," in Winter USENIX Conference, 1993.

[42] J. Dudas and T. Mudge, "Improving Data Cache Performance by Pre-executing Instructions Under a Cache Miss," in ICS, 1997.

[43] J. Dusser, T. Piquet, and A. Seneviratne, "Zero-content Augmented Caches," in ICS, 2009.

[44] E. Ebrahimi, O. Mutlu, and Y. Patt, "Techniques for bandwidth-efficient prefetching of linked data structures in hybrid prefetching systems," in HPCA, 2009.

[45] E. Ebrahimi, C. J. Lee, O. Mutlu, and Y. N. Patt, "Prefetch-aware Shared Resource Management for Multi-core Systems," in ISCA, 2011.

[46] E. Ebrahimi, R. Chakraborty, C. Fallin, C. J. Lee, A. Joan, O. Mutlu, and Y. N. Patt, "Parallel application memory scheduling," in MICRO, 2011.

[47] E. Ebrahimi, O. Mutlu, C. J. Lee, and Y. N. Patt, "Coordinated Control of Multiple Prefetchers in Multi-core Systems," in MICRO, 2009.

[48] N. El-Sayed, I. A. Stefanovici, G. Amvrosiadis, A. A. Hwang, and B. Schroeder, "Temperature Management in Data Centers: Why Some (Maybe Like It Hot)," in SIGMETRICS, 2012.

[49] S. Ghose, H. Lee, and J. F. Martinez, "Improving Memory Scheduling via Load-based Criticality Information," in ISCA, 2013.

[50] Q. Guo, N. Alachiotis, B. Akin, F. Sadi, G. Xu, T. M. Low, L. Pileggi, J. C. Hoe, and F. Franchetti, "3D-Stacked Memory-Side Accelerator: Accelerator and System Design," in WAND, 2014.

[51] H. Hassan, G. Pekhimenko, N. Vijaykumar, V. Seshadri, D. Lee, O. Ergin, and O. Mutlu, "Charge-Cache: Reducing DRAM Latency by Exploiting Row Access Locality," in HPCA, 2016.

[52] H. Hassan, N. Vijaykumar, S. Khan, S. Ghose, K. Chang, G. Pekhimenko, D. Lee, O. Ergin, and O. Mutlu, "SoftMC: A Flexible and Practical Open-Source Infrastructure for Enabling Experimental DRAM Studies," in HPCA, 2017.

[53] H. Hidaka, Y. Matuda, M. Asakura, and K. Fujishima, "The Cache DRAM Architecture: A DRAM with an On-Chip Cache Memory," in MICRO, 1990.

[54] K. Hsieh, S. Khan, N. Vijaykumar, K. K. Chang, A. Boroumand, S. Ghose, and O. Mutlu, "Accelerating Pointer Chasing in 3-D Stacked Memory: Challenges, Mechanisms, Evaluation," in ICD, 2016.

[55] K. Hsieh, E. Ebrahimi, G. Kim, N. Chatterjee, M. O’Connor, N. Vijaykumar, O. Mutlu, and S. W. Keckler, "Transparent Offloading and Mapping (TOM): Enabling Programmer-Transparent Near-Data Processing in GPU Systems," in ASPLOS, 2016.

[56] J Hur and C. Lin, “Adaptive History-Based Memory Schedulers,” in MICRO, 2004.

[57] A. A. Hwang, I. A. Stefanovici, and B. Schroeder, “Cosmic Rays Don’t Strike K. Hsieh, V. F. Seshadri, D. Lee, L. Zheng, J. Halbert, K. Bains, S. Jang, and J. Choi, “A Case for Exploiting Read-Write Disparity,” in HPCA, 2014.

[58] S. Khan, A. R. Alameldeen, C. Wilkerson, O. Mutlu, and D. A. Jimenez, “Improving Cache Performance by Exploiting Read-Write Disparity,” in HPCA, 2014.

[59] D. Kaseridis, J. Stuecheli, and L. K. John, “Minimalist Open-Page: A DRAM Page-Structure for Enabling Experimental DRAM Studies,” in MICRO, 2016.

[60] D. Lo, L. Cheng, R. Govindaraju, P. Ranganathan, and C. Kozyrakis, “Heracles: Phase-Change Technology and the Future of Main Memory,” in HPCA, 2010.

[61] B. Lee, P. Zhou, Y. Yang, B. Zhao, E. Ipek, O. Mutlu, and D. Burger, “Detecting and Mitigating Data-Dependent DRAM Failures by Prefetch-Aware Shared Resource Management for Multi-core Systems,” in ISCA, 2012.

[62] E. Ebrahimi, A. A. Hwang, I. A. Stefanovici, and B. Schroeder, “Improving Memory Scheduling via Pre-executing Instructions Under a Cache Miss,” in ICS, 1997.

[63] J. Dusser, T. Piquet, and A. Seneviratne, "Zero-content Augmented Caches," in ICS, 2009.

[64] S. Ghose, H. Lee, and J. F. Martinez, "Improving Memory Scheduling via Load-based Criticality Information," in ISCA, 2013.

[65] Q. Guo, N. Alachiotis, B. Akin, F. Sadi, G. Xu, T. M. Low, L. Pileggi, J. C. Hoe, and F. Franchetti, "3D-Stacked Memory-Side Accelerator: Accelerator and System Design," in WAND, 2014.

[66] H. Hassan, G. Pekhimenko, N. Vijaykumar, V. Seshadri, D. Lee, O. Ergin, and O. Mutlu, "Charge-Cache: Reducing DRAM Latency by Exploiting Row Access Locality," in HPCA, 2016.

[67] H. Hassan, N. Vijaykumar, S. Khan, S. Ghose, K. Chang, G. Pekhimenko, D. Lee, O. Ergin, and O. Mutlu, "SoftMC: A Flexible and Practical Open-Source Infrastructure for Enabling Experimental DRAM Studies," in HPCA, 2017.

[68] H. Hidaka, Y. Matuda, M. Asakura, and K. Fujishima, "The Cache DRAM Architecture: A DRAM with an On-Chip Cache Memory," in MICRO, 1990.

[69] K. Hsieh, S. Khan, N. Vijaykumar, K. K. Chang, A. Boroumand, S. Ghose, and O. Mutlu, "Accelerating Pointer Chasing in 3-D Stacked Memory: Challenges, Mechanisms, Evaluation," in ICD, 2016.

[70] K. Hsieh, E. Ebrahimi, G. Kim, N. Chatterjee, M. O’Connor, N. Vijaykumar, O. Mutlu, and S. W. Keckler, "Transparent Offloading and Mapping (TOM): Enabling Programmer-Transparent Near-Data Processing in GPU Systems," in ASPLOS, 2016.

[71] J Hur and C. Lin, “Adaptive History-Based Memory Schedulers,” in MICRO, 2004.

[72] A. A. Hwang, I. A. Stefanovici, and B. Schroeder, “Cosmic Rays Don’t Strike K. Hsieh, V. F. Seshadri, D. Lee, L. Zheng, J. Halbert, K. Bains, S. Jang, and J. Choi, “A Case for Exploiting Read-Write Disparity,” in HPCA, 2014.

[73] D. Kaseridis, J. Stuecheli, and L. K. John, “Minimalist Open-Page: A DRAM Page-Structure for Enabling Experimental DRAM Studies,” in MICRO, 2016.

[74] D. Lo, L. Cheng, R. Govindaraju, P. Ranganathan, and C. Kozyrakis, “Heracles: Phase-Change Technology and the Future of Main Memory,” in HPCA, 2010.

[75] B. Lee, P. Zhou, Y. Yang, B. Zhao, E. Ipek, O. Mutlu, and D. Burger, “Detecting and Mitigating Data-Dependent DRAM Failures by Prefetch-Aware Shared Resource Management for Multi-core Systems,” in ISCA, 2012.

[76] E. Ebrahimi, A. A. Hwang, I. A. Stefanovici, and B. Schroeder, “Improving Memory Scheduling via Pre-executing Instructions Under a Cache Miss,” in ICS, 1997.

[77] J. Dusser, T. Piquet, and A. Seneviratne, "Zero-content Augmented Caches," in ICS, 2009.

[78] S. Ghose, H. Lee, and J. F. Martinez, “Improving Memory Scheduling via Load-based Criticality Information,” in ISCA, 2013.

[79] Q. Guo, N. Alachiotis, B. Akin, F. Sadi, G. Xu, T. M. Low, L. Pileggi, J. C. Hoe, and F. Franchetti, "3D-Stacked Memory-Side Accelerator: Accelerator and System Design," in WAND, 2014.
[177] J. Zhao, O. Mutlu, and Y. Xie, "FIRM: Fair and High-Performance Memory Control for Persistent Memory Systems," in MICRO, 2014.

[178] H. Zheng, J. Lin, Z. Zhang, E. Gorbatov, H. David, and Z. Zhu, "Mini-rank: Adaptive DRAM architecture for improving memory power efficiency," in MICRO, 2008.