**Research Article**

**Temperature-Dependent Physical and Memory Characteristics of Atomic-Layer-Deposited RuO$_x$ Metal Nanocrystal Capacitors**

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1. Introduction

Memory devices with a low program/erase voltage operation and a better scalability with excellent endurance/retention are required for future nanoscale high-performance flash memory applications. According to the International Technology Roadmap for Semiconductors (ITRS) on a 20 nm technology node [1], the scaling of tunneling oxide thickness is one of the key issues for conventional floating gate memory devices. Recently, many nanocrystals with the advantages of many energy levels as well as high charge-trapping probability, high-speed with a low program/erase voltage operation, high scalability potential, excellent endurance, and data retention, and so forth, have been reported [2–10]. Due to higher density of states around the Fermi level, discrete charge storage in the nanocrystals and stronger coupling with conduction channel, the thickness of tunneling oxide can be reduced for metal or metal oxide nanocrystal memory devices. To solve the scaling problems, high-κ tunneling barriers such as HfO$_2$, Al$_2$O$_3$ are also reported by many researchers. The metal nanocrystals embedded in high-κ tunneling barriers with high thermal stability (~1000°C) are needed in future nanoscale nonvolatile memory applications, that can follow the conventional complementary-metal-oxide-semiconductor (CMOS) process line. Recently, the TiN nanocrystal memory devices were reported with process temperatures of 1000°C [7] and ~1050°C [10]. Due to the high melting point (~1200°C [11]) and high work function (Φ$_m$ > 4.7 eV) of ruthenium oxide (RuO$_x$) materials, this nanocrystal can be also used as a charge-storage node in nanoscale flash memory device applications. Furthermore, the RuO$_x$ material can be deposited...
by atomic-layer-deposition (ALD), which will be useful in future applications. In this study, annealing dependence of the atomic-layer-deposited RuO$_x$ nanocrystals embedded in the high-$\kappa$ HfO$_2$/Al$_2$O$_3$ layers in an n–Si/SiO$_2$/HfO$_2$/RuO$_x$/Al$_2$O$_3$/Pt memory structure has been investigated. After post-deposition annealing (PDA) temperature ranges from 850–1000°C, the Hf-silicate layer at the SiO$_2$/HfO$_2$ interface is formed. The memory devices with a low voltage operation (<5 V) and good memory characteristics are obtained after a high PDA of 1000°C.

2. Experimental and Methods

n-Type Si (100) substrate with a doping of $1 \times 10^{17}$/cm$^3$ was cleaned by an RCA process. To remove native oxide from the Si surface, the wafer was dipped in HF solution. After cleaning Si wafers, the tunneling oxide (SiO$_2$) with a nominal thickness of 3 nm was grown by a rapid thermal oxidation (RTO) process at a substrate temperature of 1000°C for 15 s. The oxygen gas (O$_2$) was used for oxidation. The high-$\kappa$ HfO$_2$ film with an as-deposited thickness of 2 nm was grown for a wetting layer by ALD. The high-$\kappa$ HfO$_2$ film can be used as a part of tunneling oxide. The stack tunneling oxide layers are SiO$_2$ and HfO$_2$ films, which can also improve memory performance. Then, the RuO$_x$ metal layer with an as-deposited thickness of ∼2 nm was grown by ALD using a diethyl-cyclopentadienyl ruthenium [Ru(EtCp)$_2$] precursor at a substrate temperature of 350°C. The precursor temperature was 100°C. The high-$\kappa$ Al$_2$O$_3$ film with a thickness of 20 nm was deposited in situ for a blocking oxide by ALD. The H$_2$O precursor was used for oxygen content. The description of the deposition of high-$\kappa$ and metal oxide films by ALD can be found in our previous study [12]. To form the RuO$_x$ nanocrystals from a RuO$_x$ nanolayer, a PDA process with the temperature ranges from 850 to 1000°C for 1 min in N$_2$ (90%) + O$_2$ (10%) gas mixtures by a rapid thermal annealing (RTA) process was performed. To maintain the quality of the high-$\kappa$ Al$_2$O$_3$ film during the RTA process, a small amount (10%) of oxygen gas was used during the annealing process. For comparison, the pure Al$_2$O$_3$ film as a charge-trapping layer was also deposited on a SiO$_2$/Si substrate. The thickness of the Al$_2$O$_3$ film was 20 nm. The Al$_2$O$_3$ charge-trapping layer was annealed at 900°C for 1 min. in N$_2$ ambient by the RTA process. A platinum (Pt) metal gate electrode with a gate area of $1.12 \times 10^{-4}$ cm$^2$ was fabricated by using a shadow mask. A schematic view of the RuO$_x$ metal nanocrystal capacitors is shown in Figure 1. The RuO$_x$ metal nanocrystals are embedded in the high-$\kappa$ HfO$_2$/Al$_2$O$_3$ films. Table 1 shows the thickness and electrical characteristics of the RuO$_x$ nanocrystal memory capacitors. To confirm the size and microstructure of the RuO$_x$ nanocrystals, high-resolution transmission electron microscopy (HRTEM) with an operating voltage of 300 kV and a resolution of 0.17 nm was carried out. To investigate the chemical bonds of Si–O, Hf–O, Ru–O, and Al–O signals, X-ray photo-electron spectroscopy (XPS) was performed. Memory characteristics such as capacitance-voltage (C−V) hysteresis, current density-voltage (J−V), retention, and endurance, and so forth, were investigated using an HP 4284A LCR meter and HP 4156C semiconductor measurement analyzer.

3. Results and Discussion

The thicknesses of the as-deposited dielectric layers are verified by cross-sectional HRTEM images, as shown in Figure 2(a). The as-deposited film is investigated for comparison. The thicknesses of SiO$_2$, HfO$_2$, RuO$_x$, and Al$_2$O$_3$ layers are 3, 2, 2, and 20 nm, respectively, for the as-deposited film. The RuO$_x$ metal layer shows crystalline, while both high-$\kappa$ HfO$_2$ and Al$_2$O$_3$ films appear amorphous in nature. The elemental compositions of all layers are observed by energy dispersive X-ray spectroscopy (EDS) with a spot size of 0.5 nm in a diameter and a spacial resolution of ∼1 nm (Figure 2(b)). The numbers indicated on the EDS spectra correspond to the numbers on the TEM image. The peak elemental compositions of hafnium (Hf), ruthenium (Ru), oxygen (O) and aluminum (Al) atoms are 23.6, 3.5, 60.3, and 37.5 at %, respectively. It is estimated that the SiO$_2$, HfO$_2$ and Al$_2$O$_3$ films are closely stoichiometric for the as-deposited one. After annealing at 850°C (sample: S1), the RuO$_x$ nanolayer displayed the nanocrystals (Figure 2(c)). The peak elemental compositions of the Hf, Ru, O, and Al atoms are 24.5, 17.7, 59.5 and 39.9 at %, respectively (Figure 2(d)). The atomic concentration of Ru is increased from 3.5 at % to 17.7 at % after the annealing process. It is speculated that this higher atomic concentration of Ru after the annealing process may be due to both Ru-rich nanocrystal formation, and higher thickness from 2-3 nm. Furthermore, the atomic concentrations of Si and Hf atoms at a beam position of 4 are 33.2 and 13.5 at %, respectively, for the annealed memory capacitors, and those values are 29.9 and 6 at % for the as-deposited capacitor. Enhanced Si and Hf atoms at the SiO$_2$/HfO$_2$ interface can be explained by diffusion of Hf and Si atoms after the annealing process. This is due to the Hf-silicate (HfSiO$_x$, or simply HfSiO) formation at the SiO$_2$/HfO$_2$ interface, which has been also confirmed by subsequent XPS measurement later. The atomic concentrations of Al and Hf at a beam position of 6 are 8.1 and 24.7, respectively, for the annealed memory capacitors, while those values are 6.1 and 24 for the as-deposited capacitors. The atomic concentrations are enhanced (slightly) after the annealing process. It indicates
that the Hf and Al atoms are also diffused after the annealing process which can also form HfAlOₓ at the HfO₂/Al₂O₃ interface or in the vicinity of the RuOₓ nanocrystals. The thicknesses of SiO₂, HfO₂, and Al₂O₃ layers are found to be 3.5, 1, and 17 nm, respectively (Figure 3(a)). The thickness of RuOₓ nanocrystal is approximately 3 nm. Total physical thickness of the stack tunneling oxides including SiO₂, HfSiOₓ, and HfO₂ layers is 4.5 nm, which is one of the important key areas to improve the memory characteristics. The thickness of SiO₂ layer is slightly (0.5 nm) increased

Figure 2: (a) HRTEM image of RuOₓ nanolayer; (b) atomic concentration profiles by EDX from TEM image (a); (c) HRTEM image of RuOₓ nanocrystals at PDA 850°C; (d) atomic concentration profiles by EDX from TEM image (c) in an n–Si/SiO₂/HfO₂/RuOₓ/Al₂O₃/Pt structure. The beam positions are indicated as shown in the HRTEM images.
Figure 3: HRTEM images with different post-deposition annealing temperatures from (a) 850°C; (b) 900°C; (c) 950°C; (d) 1000°C in an n-Si/SiO₂/HfO₂/RuOₓ/Al₂O₃/Pt capacitor.

Table 1: Thickness and characteristics of all memory capacitors after the annealing process.

| Memory capacitors | PDA (°C) | SiO₂ (nm) | HfO₂ (nm) | RuOₓ (nm) | Al₂O₃ (nm) | Memory window at ±5 V | Memory window at ±7 V | Breakdown voltage (V) |
|-------------------|----------|-----------|-----------|-----------|------------|-----------------------|-----------------------|----------------------|
| S1                | 850      | 3.5       | 1         | 3         | 17         | 1.8 V                 | 4.0 V                 | −15                  |
| S2                | 900      | 3.5       | 1         | 3         | 17         | 8.0 V                 | 11.1 V                | −14                  |
| S3                | 950      | 3.5       | 1         | 4         | 17         | 7.5 V                 | 10.8 V                | −14                  |
| S4                | 1000     | 4.0       | 1         | 4         | 17         | 5.2 V                 | 8.6 V                 | −13.4                |

compared to that of the as-deposited one. The thicknesses of HfO₂ and Al₂O₃ films are reduced (2-1 nm and 20–17 nm) compared to that of the as-deposited one, due to both the nanocrystal formation and densification of the films. All of the films including HfO₂, RuOₓ, and Al₂O₃ show crystalline after the annealing process. The thickness of SiO₂ is increased (3.5–4 nm) by increasing the annealing temperatures from 850°C to 1000°C (Figure 3 and Table 1), due to both the oxygen diffusion and HfSiO formation at the SiO₂/HfO₂ interface. The thickness of SiO₂ layer including HfSiO film
is approximately 4 nm at a PDA of 1000°C. The thickness of stack tunneling oxide including SiO₂, HfSiO, and HfO₂ layers nm is approximately 5 nm. It is expected that the thickness of the HfSiO layer is about 0.5–1.0 nm. The thickness (∼3 nm at 850°C to ∼4 nm at 1000°C) and average diameter (∼7 nm at 850°C to ∼11.5 nm at 1000°C) of the RuOₓ metal nanocrystals are also increased with an increasing in the annealing temperature up to 1000°C (sample: S4), due to the agglomeration or nanotwin formation after high temperature process. The Si and metal nanotwin formations after the annealing process were also reported by Wang et al. [13]. Figure 4 shows a plane-view TEM image of the RuOₓ nanocrystals in an n–Si/SiO₂/HfO₂/RuOₓ/Al₂O₃/Pt memory structure at a PDA of 850°C (sample: S1). The RuOₓ nanocrystals are observed clearly. The average diameter is approximately 7 nm, which is larger than that of the cross-sectional TEM image in Figure 2(c) (diameter: ∼4 nm) due to the different crystal orientations or image captured at different positions. The nanocrystals are like a circular disk and the diameters are varied from 4–10 nm. Figure 5 shows the diameter and density of the RuOₓ metal nanocrystals with different annealing temperature ranges from 850°C–1000°C. The density of the RuOₓ nanocrystals is calculated from the plane-view TEM images. The density of the RuOₓ metal nanocrystals is high: 1.5 × 10¹²/cm² at a PDA of 850°C; 0.7 × 10¹²/cm² at a PDA of 1000°C. A single RuOₓ nanocrystal with different annealing temperatures is also shown in the inset of Figure 5. At a PDA of 1000°C, the nanocrystals are difficult to observe clearly on a plane-view TEM image because of crystalline Al₂O₃ film. It suggests that the density of the RuOₓ metal nanocrystals decreases (slightly) with increasing the annealing temperatures due to the agglomeration of multiple nanocrystals. The nanocrystal sizes are varied from 4–10 nm, 4–12 nm, 4–17 nm, and 5–18 nm for the PDAs of 850°C, 900°C, 950°C, and 1000°C, respectively (data not shown). The average diameters are from 7–11.5 nm for the annealing temperatures at 850°C to 1000°C. The nanocrystal size distribution is broad with increasing the annealing temperature. However, the memory characteristics are very promising for future nanoscale nonvolatile memory applications. Furthermore, the compositions of the RuOₓ metal nanocrystals are explained by XPS below.

Figure 6(a) shows the Ru3d spectra with different annealing temperatures. The RuOₓ metal nanocrystals show the Ru3d5/2 and Ru3d3/2 doublets. At a PDA of 850°C (sample: S1), the peak binding energies of the Ru3d5/2 and Ru3d3/2 electrons are 281.7 eV and 285.9 eV, respectively. The peak binding energies are quite similar 281.7–281.5 eV for the Ru3d5/2 electrons, and 285.9–285.7 eV for the Ru3d3/2 electrons, with increasing annealing temperatures from 850–1000°C. The peak fittings of the Ru3d5/2 core level electrons are performed by Shirley background subtraction and Gaussian/Lorentzian functions at a PDA of 1000°C (Figure 6(b)). The RuOₓ peak is located at 281.5 eV. A negligible intensity of the RuO₂ and RuO peak is observed. The binding energy peak positions and the separation between the doublets (4.0–4.2 eV) indicate the presence of the RuO₂ nanocrystals. Zhang et al. [14] reported that the peak binding energies of the Ru3d5/2 electrons for Ru and RuO₂ elements were 280.6 eV and 281.6 eV, respectively. Kaga et al. [15] reported that the peak binding energies of the Ru3d5/2 electrons are 280 eV for the Ru, and 280.8 eV for the RuO₂ films. Basically, the RuO₃ element is almost unchanged up to an annealing temperature of 1000°C due to the high thermal stability of the RuOₓ nanocrystals in the memory capacitors.

Figure 7(a) shows the Hf4f peaks with different annealing temperatures. The peaks are located at the Hf4f7/2 and Hf4f5/2. These Hf4f doublet peaks originate from the pure HFO₂ or Hf-silicate film. The peak binding energies are 17–16.7 eV for the Hf4f7/2 electrons, and 18.6–18.4 for the Hf4f5/2 electrons with different annealing temperatures from 850–1000°C (samples: S1–S4). The shift of the Hf peak toward higher binding energy is attributed to both the formation of the Hf-silicate and Hf-aluminate films, which...
Figure 6: (a) XPS spectra of the Ru3d electrons with different annealing temperatures from 850–1000°C; (b) Ru3d electrons at a PDA of 1000°C is deconvoluted.

Figure 7: (a) XPS spectra of the Hf4f electrons with different annealing temperatures from 850–1000°C; (b) XPS spectra of the Si2p electrons at the PDA of 850°C and 1000°C.

is ∼0.3 eV higher than that of pure HfO2 film (16.7 eV [16]). Figure 7(b) shows the Si2p core-level electrons with different annealing temperatures (samples: S1 & S4). An additional peak shift with respect to the Si2p core-level spectra (99.2 eV) at the interfacial layer of the HfO2/SiO2 structures is ∼3.45 eV with different annealing temperatures of 850°C and 1000°C. A lower Si2p binding energy shift with respect to SiO2 (∼4.2 eV) indicates that the interfacial layer is composed with the Hf atoms or formed Hf-silicate compound. It is believed that this Hf-silicate layer is at the SiO2/HfO2 interface or HfO2 layer itself a HfSiO layer. Furthermore, the SiO2 peak (∼102.65 eV)
versus sweeping gate voltages with different annealing temperatures from 850–1000°C. A high-κ Al2O3 charge-trapping layer is also shown for comparison.

Figure 8: (a) C-V hysteresis characteristics with different sweeping gate voltages at a PDA of 950°C; (b) a C-V hysteresis memory window versus sweeping gate voltages with different annealing temperatures from 850–1000°C. A high-κ Al2O3 charge-trapping layer is also shown for comparison.
region of the nanocrystals should be larger than the core area of the nanocrystals. It is believed that the holes will be trapped in the annular region while the electrons will be trapped in the core region of the nanocrystals. Considering the nanocrystal density of $0.8 \times 10^{12} \text{cm}^{-2}$ at a PDA of 950°C, one RuO$_2$ nanocrystal can trap 23 electrons and 33 holes under the gate voltages of +7 V and −7 V, respectively. The hysteresis memory windows as well as electron- (or hole-) trapping density can be varied with sweeping gate voltages and different annealing temperatures, as shown in Figure 8(b). A large hysteresis memory window of the RuO$_2$ metal nanocrystal memory capacitors at different annealing temperatures is observed compared to that of the pure Al$_2$O$_3$ charge-trapping layers in a Pt/Al$_2$O$_3$ (20 nm)/SiO$_2$ (3 nm)/Si structure, due to charge-trapping in the RuO$_2$ nanocrystals. The memory capacitors with an as-deposited RuO$_2$ metal layer in an n–Si/SiO$_2$/HfO$_2$/RuO$_2$/Al$_2$O$_3$/Pt structure have been also fabricated for comparison. According to our capacitor design, the metal gate electrode (Pt) is deposited by using shadow mask. It indicates that the device-to-device isolation is observed by metal gate electrode only but the RuO$_2$ metal layer is continuous. For the as-deposited RuO$_2$ film, the C–V characteristics could not be observed from our CV measurement system and the system shows OVERLOAD. Then the capacitors have been annealed from 600–1000°C. The C–V characteristics are observed from the PDAs of 800–1000°C. At PDA of <800°C, the C–V characteristics could not be measured. It suggests that the electric field could not pass inside the RuO$_2$ metal layer, resulting in no C–V characteristics. At the PDA of >800°C, the RuO$_2$ nanocrystals have been formed and the metal layer becomes discrete, resulting in the electric field pass through the RuO$_2$ nanocrystal boundary. In this case, the CV system could measure C–V characteristics. On this point, the temperature of the metal nanocrystal formation can be monitored, which is also important for other metal nanocrystal formation process. The nanocrystal formation temperature depends on the thickness of the metal nanolayer, deposition process, and material itself. A memory window of the pure Al$_2$O$_3$ charge-trapping layer is increased (slightly) after sweeping gate voltages of ±7 V. After the annealing process, the Al$_2$O$_3$ grain boundaries can be formed and the charges can be trapped on the grain boundary sites. The thickness of tunneling oxide (SiO$_2$) is increased (3 nm to 4 nm) at the SiO$_2$/Al$_2$O$_3$ interface after the high-temperature annealing process. Due to both the thicker tunneling oxide and the higher temperature, the charge-trapping can be only observed in the RuO$_2$ nanocrystals. If the operation voltage is higher than ±7 V then the charge-trapping can be observed in both of the RuO$_2$ nanocrystals and Al$_2$O$_3$ charge-trapping layers. Under a sweeping gate voltage of ±5 V, the hysteresis memory windows are 1.8, 8.0, 7.5, and 5.2 V for the PDA of 850°C, 900°C, 950°C, and 1000°C, respectively. Those values are 4.0, 11.1, 10.8, and 8.6 V under a sweeping gate voltage of ±7 V (Figure 8(b)).

Even though the high-density RuO$_2$ nanocrystals are observed at a PDA of 850°C but the smallest memory window is observed as compared to that observed for other high temperature annealing processes. It may be due to both the higher equivalent oxide thickness (EOT = 8.9 ± 0.5 nm), as shown in Figure 9, and the unwanted defects remained in the RuO$_2$ nanocrystals at low annealing temperature (850°C).

The EOT decreases (slightly) with increasing PDA up to 950°C, due to densification of the layers. But the EOT is increased at a PDA of 1000°C due to a thicker stack tunneling oxide (~5 nm). A minimum EOT of 7.9 ± 0.5 nm is observed at a PDA of 950°C. The memory window at 1000°C is also lower as compared to that of both annealing temperatures of 900°C and 950°C due to the higher EOT, the lower density of the RuO$_2$ nanocrystals and higher leakage current, which will be discussed below. At a PDA of 900°C and 950°C, a large hysteresis memory window of >14.0 V is observed under a sweeping gate voltage of ±10 V due to both the lower EOT (7.9 ± 0.5 nm) and the RuO$_2$ nanocrystals composed with RuO$_2$ and RuO$_3$ elements (data not shown). A memory window of 0.9 V is also observed under a small sweeping gate voltage of ±1 V. The large memory window and high electron- (or hole-) trapping density of the memory devices under a low voltage operation can be used in future multi-level-charge (MLC)-trapping flash memory device applications, which has been explained below.

The C–V hysteresis indicates that the charge can be trapped in the RuO$_2$ nanocrystals under a small positive gate voltage and the trapped charges can be erased under a small negative gate voltage. The electric fields across layer-by-layer under the external gate voltages ($V_g$) can be explained below. Considering the memory device under programming mode, the stack voltage, $V_{stack}(=V_g - V_{FBN} - \psi_s)$ across the memory structure can be written by

$$V_{stack} = V_{SiO_{2}} + V_{HfO_{2}} + V_{RuO_{2}} + V_{Al_{2}O_{3}},$$

where $\psi_s$ is the surface potential at the SiO$_2$/Si interface, $V_{SiO_{2}}$ is the voltage across the SiO$_2$ tunneling layer (i.e., SiO$_2$ and HfSiO$_3$), $V_{HfO_{2}}$ is the voltage across the HfO$_2$ layer, $V_{RuO_{2}}$ is the voltage across the RuO$_2$ nanocrystal layer, and $V_{Al_{2}O_{3}}$ is the voltage across the blocking oxide (Al$_2$O$_3$). The $V_{FBN}$ is about +0.5 V for our device. The surface potential can be written as

$$\psi_s = kT q \ln \frac{N_D}{n_i},$$

where $k$ (=1.38 × 10$^{-23}$ J/K) is the Boltzmann’s constant, $T$ (=300 K) is the absolute temperature, $N_D$ (1 × 10$^{17}$ cm$^{-3}$) is
Figure 9: Equivalent oxide thickness (EOT) versus different annealing temperatures.

Figure 10: Electric fields across different layers versus different annealing temperatures and different gate voltages.

Figure 11: Leakage current with different annealing temperatures.

The doping density in n-type Si, \( n_i = 1.45 \times 10^{10} \text{ cm}^{-3} \) is the intrinsic carrier concentration of Si. Using those above values, the \( \psi_s \) is 0.41 V. From Gauss’s law of electrostatics on layer-by-layer structure, the boundary condition can be written as follows:

\[
\varepsilon_{\text{SiO}_2} \cdot E_{\text{SiO}_2} = \varepsilon_{\text{HfO}_2} \cdot E_{\text{HfO}_2} = \varepsilon_{\text{RuO}_x} \cdot E_{\text{RuO}_x} = \varepsilon_{\text{Al}_2\text{O}_3} \cdot E_{\text{Al}_2\text{O}_3},
\]

(4)

The \( \varepsilon_{\text{SiO}_2}, \varepsilon_{\text{HfO}_2}, \varepsilon_{\text{RuO}_x}, \) and \( \varepsilon_{\text{Al}_2\text{O}_3} \) are the relative permittivities of the SiO\(_2\), HfO\(_2\), RuO\(_x\) nanocrystal, and Al\(_2\)O\(_3\) layers, respectively. The \( E_{\text{SiO}_2}, E_{\text{HfO}_2}, E_{\text{RuO}_x}, \) and \( E_{\text{Al}_2\text{O}_3} \) are the electric fields across the SiO\(_2\), HfO\(_2\), RuO\(_x\) nanocrystal, and Al\(_2\)O\(_3\) layers, respectively. The electric fields across the SiO\(_2\), HfO\(_2\), and Al\(_2\)O\(_3\) layers can be obtained from (2) and (4),

\[
E_{\text{SiO}_2} = \frac{V_{\text{SiO}_2}}{t_{\text{SiO}_2}}
= \left[ t_{\text{SiO}_2} + \varepsilon_{\text{SiO}_2} \cdot \left( \frac{t_{\text{HfO}_2}}{\varepsilon_{\text{HfO}_2}} + \frac{t_{\text{RuO}_x}}{\varepsilon_{\text{RuO}_x}} + \frac{t_{\text{Al}_2\text{O}_3}}{\varepsilon_{\text{Al}_2\text{O}_3}} \right) \right]^{-1} \cdot V_{\text{stack}},
\]

(5)

\[
E_{\text{HfO}_2} = \frac{V_{\text{HfO}_2}}{t_{\text{HfO}_2}}
= \left[ t_{\text{HfO}_2} + \varepsilon_{\text{HfO}_2} \cdot \left( \frac{t_{\text{SiO}_2}}{\varepsilon_{\text{SiO}_2}} + \frac{t_{\text{RuO}_x}}{\varepsilon_{\text{RuO}_x}} + \frac{t_{\text{Al}_2\text{O}_3}}{\varepsilon_{\text{Al}_2\text{O}_3}} \right) \right]^{-1} \cdot V_{\text{stack}},
\]

(6)

\[
E_{\text{Al}_2\text{O}_3} = \frac{V_{\text{Al}_2\text{O}_3}}{t_{\text{Al}_2\text{O}_3}}
= \left[ t_{\text{Al}_2\text{O}_3} + \varepsilon_{\text{Al}_2\text{O}_3} \cdot \left( \frac{t_{\text{SiO}_2}}{\varepsilon_{\text{SiO}_2}} + \frac{t_{\text{HfO}_2}}{\varepsilon_{\text{HfO}_2}} + \frac{t_{\text{RuO}_x}}{\varepsilon_{\text{RuO}_x}} \right) \right]^{-1} \cdot V_{\text{stack}},
\]

(7)

where the \( t_{\text{SiO}_2}, t_{\text{HfO}_2}, t_{\text{RuO}_x}, \) and \( t_{\text{Al}_2\text{O}_3} \) are the thicknesses of the SiO\(_2\), HfO\(_2\), RuO\(_x\) nanocrystal, and Al\(_2\)O\(_3\) layers, respectively. Total series capacitance \( (C_{\text{total}}) \) at accumulation region can be written as

\[
\frac{1}{C_{\text{total}}} = \frac{t_{\text{SiO}_2}}{\varepsilon_{\text{SiO}_2} \cdot \varepsilon_0 \cdot A} + \frac{t_{\text{HfO}_2}}{\varepsilon_{\text{HfO}_2} \cdot \varepsilon_0 \cdot A} + \frac{t_{\text{RuO}_x}}{\varepsilon_{\text{RuO}_x} \cdot \varepsilon_0 \cdot A} + \frac{t_{\text{Al}_2\text{O}_3}}{\varepsilon_{\text{Al}_2\text{O}_3} \cdot \varepsilon_0 \cdot A}.
\]

(8)
where $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm is the free space permittivity. The values of $C_{\text{total}}$ are 43.43, 45.2, 48.72, and 43.92 pF for the PDA of 850°C, 900°C, 950°C, 1000°C, respectively. Considering the series capacitances using (8) and thicknesses (Table 1) of layer by layer for all annealing temperatures, the relative permittivity values of the Al$_2$O$_3$, HfO$_2$, and Ru$_x$ layers are 13, 17, and 40, respectively [18–21]. The higher relative permittivity of the Al$_2$O$_3$ film is due to the crystallization or Ru$_x$ diffusion into the Al$_2$O$_3$ film during a high-temperature annealing process. The different crystal orientation including metal-doped Al$_2$O$_3$ film or nanograin formation of the high-κ Al$_2$O$_3$ films may also cause higher permittivity of the film. The values of effective permittivity of the SiO$_2$ layer are found to be 4.15, 4.65, 6.15, and 5.1 for the PDA of 850°C, 900°C, 950°C, 1000°C, respectively. The effective permittivity of the tunneling oxide (SiO$_2$) is higher than that of a pure SiO$_2$ layer ($\varepsilon_{\text{SiO}_2} = 3.9$). It suggests that the Hf-silicate layer at the HfO$_2$/SiO$_2$ interface is formed after the annealing process, due to the Hf and Si atom diffusion which is also explained by EDX and XPS analyses. Using those relative permittivity values in (5), (6), and (7), the electric fields have been calculated under positive gate voltages of $V_g = +10$ V or +5 V on the Pt gate electrode. The electric fields versus PDA temperatures are plotted as shown in Figure 10. The electric field across the SiO$_2$ layer ($E_{\text{SiO}_2}$) is higher than 8 MV/cm under an operation voltage of +10 V for all annealing temperatures. Under a gate voltage of +5 V, the $E_{\text{SiO}_2}$ is $\sim$4 MV/cm. It indicates that the modified Fowler-Nordheim (F-N) tunneling mechanism plays a role to trap electron in the RuO$_x$ nanocrystals. The electric field across the HfO$_2$ layer is smaller $\sim2$ MV/cm but the conduction band offset $|\Delta E| = (E_F)_\text{Si} - (E_F)_{\text{HfO}_2} = 4.05\text{ eV} - 2.35\text{ eV} = 1.7\text{ eV}$ between the Si and HfO$_2$ conduction layers is also smaller. The electrons can be tunneled easily through the HfO$_2$ layer. The electric field is decreased (slightly) with increasing the PDA temperature, due to the higher thickness and permittivity of the SiO$_2$ layer. It is noted that the electric field across the high-κ Al$_2$O$_3$ layers is much smaller than the electric field across the SiO$_2$ layer. In this case, the electrons are tunneled through the tunneling oxide layer and the charges are trapped in the RuO$_x$ metal nanocrystals under a low voltage operation. When we apply the negative gate voltage on Pt gate electrode then the electric field across the tunneling oxide layer ($E_{\text{SiO}_2}$) is also higher than that of the blocking oxide layer ($E_{\text{Al}_2\text{O}_3}$). First, the trapped electrons will be tunneled back from the RuO$_x$ nanocrystals to the Si conduction layer. Second, the holes will be tunneled from the Si valence band to the RuO$_x$ nanocrystals. So, the large memory window is observed due to the electron and hole traps under positive and negative gate voltages, respectively, on the gate electrode.

Figure 11 shows the variation of leakage current density with different annealing temperatures. The leakage current density of the RuO$_x$ nanocrystal memory capacitors is higher than that of the pure Al$_2$O$_3$ charge-trapping layers due to the RuO$_x$ nanocrystal formation. The leakage current increases with increasing the PDA temperatures, due to the nanocrystal formation and outdiffusion of RuO$_x$ metal into the high-κ Al$_2$O$_3$ blocking oxide. Furthermore, the crystallization of the Al$_2$O$_3$ film can also play a role to increase leakage current. The formation of crystallites may result in increased leakage currents along grain boundaries of the Al$_2$O$_3$ films after high temperature annealing process. The breakdown voltage of the RuO$_x$ nanocrystal memory capacitors decreases with increasing the PDA temperatures, due to higher leakage current. It is also believed that the hysteresis memory window at a PDA of 1000°C is lower as compared to that of 950°C, due to a higher leakage current. It implies that the hysteresis memory window can be limited by gate leakage or backtunneling current, and also by design of memory structure.

Figure 12(a) shows the excellent program/erase endurance characteristics under a small program/erase voltage of $\pm5$ V and a pulse width of 200 ms for a PDA of 1000°C.
An initial memory window is 5.6 V and it is 5.5 V after extrapolation of $10^4$ cycles. A small memory window loss of $\sim 2\%$ is observed after $10^6$ cycles. Figure 12(b) shows the variation of the flat-band voltage with retention time at a PDA of 1000 $^\circ$C. The program/erase voltage is $\pm 5$ V and pulse width is 200 ms. To read the data (i.e., $V_{FB}$) with elapsed time under programming/erasing conditions, the capacitance is measured at a read voltage of 0.1 V and the capacitance transferred to the $V_{FB}$. An initial memory window is 5.6 V and it is 5.5 V after 10 years of data retention. A small charge loss of $\sim 14\%$ at RT ($\sim 23\%$ at 85 $^\circ$C) is observed after 10 years of retention time. A small charge loss and large memory window of the RuO$_x$ nanocrystal memory capacitors under a small program/erase voltage of $\pm 5$ V are due to both the deep-level charge trap in the RuO$_x$ nanocrystals and the thicker ($\sim 5$ nm) tunneling oxide layer at a PDA of 1000 $^\circ$C, which is very useful for future nanoscale nonvolatile memory applications.

4. Conclusions

The RuO$_x$ metal nanocrystals in n–Si/SiO$_2$/Hf-silicate/HfO$_2$/RuO$_x$/Al$_2$O$_3$/Pt capacitors with different annealing temperatures from 850–1000 $^\circ$C have been investigated by using HRTEM, EDX, and XPS measurements. An average diameter of the RuO$_x$ metal nanocrystals increases from 7–11.5 nm and the density decreases from 1.5 – $0.7 \times 10^{12}$ cm$^{-2}$ with increasing PDA temperatures from 850 $^\circ$C to 1000 $^\circ$C, due to agglomeration of multiple nanocrystals. The isolated nanocrystals are observed by plane-view TEM due to the diffusion of the Si and Hf atoms at the HfO$_2$/SiO$_2$ interface during the annealing process, the Hf-silicate layer is confirmed by both XPS and electrical measurements. The RuO$_x$ metal nanocrystals with a high-density (>1 $\times 10^{12}$/cm$^2$), large memory window (>5 V) at a small gate voltage operation (<5 V), and a small EOT (<9.0 nm) are obtained. A good endurance of $10^6$ cycles and a large memory window of $\sim 4.3$ V with a small charge loss of $\sim 23\%$ at 85 $^\circ$C after extrapolation of 10-year data retention are obtained, which can be useful in future low voltage operated nanoscale nonvolatile memories.

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