Fabrication and Characterization of Controllable Grain Boundary Arrays in Solution Processed Small Molecule Organic Semiconductor Films

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We have produced solution-processed thin films of 6,13-bis(triisopropyl-silyl ethynyl) pentacene with grain sizes from a few micrometers up to millimeter scale by lateral crystallization from a rectangular stylus. Grains are oriented along the crystallization direction, and the grain size transverse to the crystallization direction depends inversely on the writing speed, hence forming a regular array of oriented grain boundaries with controllable spacing. We utilize these controllable arrays to systematically study the role of large-angle grain boundaries in carrier transport and charge trapping in thin film transistors. The effective mobility scales with the grain size, leading to an estimate of the potential drop at individual large-angle grain boundaries of more than one volt. This result indicates that the structure of grain boundaries is not molecularly abrupt, which may be a general feature of solution processed small molecule organic semiconductor thin films where relatively high energy grain boundaries are typically formed. This may be due to the crystal Transient measurements after switching from positive to negative gate bias or between large and small negative gate bias reveal reversible charge trapping with time constants on the order of 10 s, and trap densities that are correlated with grain boundary density. We suggest that charge diffusion along grain boundaries and other defects is the rate determining mechanism of the reversible trapping.

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I. INTRODUCTION

Conjugated polymers and organic small molecules such as polythiophenenes and pentacenes are of current interest because of their potential for low cost large area fabrication of various electronic devices such as solar cells, light-emitting diodes and thin film transistors. Organic semiconductor devices have advanced rapidly in terms of overall performance since mobilities exceeding 1 cm$^2$/V·s$^{-1}$ were first demonstrated in pentacene thin film transistors. In addition, an understanding of the fundamental mechanisms related to bias stress and other charge trapping effects is emerging. There has also been continuing progress in producing materials and processing methods with better overall uniformity and lifetime. Research on new methods for solution processing remains a key area, as well as understanding how such processes produce desirable thin film properties.

Laterally directed film deposition from liquid solutions can produce highly oriented films. Drop casting with controllable drying can also produce films with a high degree of local orientation, but with circular symmetry on a mesoscopic scale. A number of other methods have also been devised which give some degree of orientation and control of grain structure. Our method utilizes directed deposition from a hollow stylus composed of a rectangular glass capillary, and is based on a process that has been previously shown to produce oriented films with large grain size. We have recently developed the method further in order to vary the grain size through variation in the writing speed and substrate temperature. In this paper, we demonstrate the control of grain structure, the effect of grain boundaries on carrier transport, and reversible charge trapping for organic field-effect transistors fabricated with 6,13-bis(triisopropyl-silyl ethynyl)(TIPS) pentacene as the semiconductor material.

In Sec. III we describe results that show that semi-periodic arrays of parallel grain boundaries can be obtained, typically with just two dominant grain orientations in a twin configuration leading to a well-defined grain boundary since the orientation of the grain on each side of the boundary as well as the orientation of the boundaries themselves are aligned with the writing direction. These structures make it possible to systematically characterize the effect of the grain boundaries on thin film transistor carrier mobility, which we discuss in Sec. IV. Small numbers, as few as four grain boundaries oriented so that they maximally impede the carrier flow are found to reduce the measured field effect mobility by a significant factor. This effect is shown to be highly reproducible over arrays of transistors with channels oriented parallel and perpendicular to the film writing direction, and the effect also depends on the orientation of the boundaries.

Studies of transient phenomena in organic thin film transistors have previously found that effects can be divided into reversible and irreversible mechanisms, i.e. mechanisms with time scales of $\sim$10 s vs. mechanisms with time scales that can reach many hours. The slow mechanism is often referred to as the bias stress effect, and has been studied for a number of organic semicon-
from reversible transient currents on switching between two different negative gate voltages, where electron traps are assumed to be mainly empty in both conditions.\textsuperscript{23}

In Sec. VI, our measurements are discussed in terms of other work in the literature. These studies generally support our observation of reversible trapping of positive charge but they also clearly show that the charge does not necessarily only reside at grain boundaries.\textsuperscript{34} This is consistent with our results, since we also observe measurable trap density for films with no large-angle grain boundaries (although there can be small angle grain boundaries or other defects such as dislocations), but at a significantly lower level than the films with large-angle grain boundaries. Shallow trap states at grain boundaries appear to play a role in producing a current bottleneck, thus reducing the effective mobility.

II. EXPERIMENTAL METHODS

TIPS-pentacene is synthesized as previously reported.\textsuperscript{16} The deposition technique used in this study is a direct-write method using a hollow rectangular capillary with size of 0.5 × 5.0 mm\textsuperscript{2} I.D. (Wale apparatus Co.\#4905-100) as depicted in Fig. 1 (a). A solution with a concentration of 0.2 - 5.0 wt\% in toluene is held in the capillary by capillary forces. The capillary is bent at 1 cm from the end to form an "L" shape so that a gravity feed at constant pressure corresponding to the height of the vertical part is maintained. The capillary can hold enough solution in the horizontal part to coat a one inch long substrate, eliminating the need for solution pumping. Filling and cleaning of the capillary is straightforward since the narrow cross section causes it to draw in solution by capillary action. A substrate is mounted on a computer-controlled linear translation stage (Newport, M-VP-25XA) equipped with a thermoelectric module for temperature control. Film deposition is accomplished by allowing the microdroplet of solution on the end of the capillary to make contact with the surface and then laterally translating the substrate at a controlled rate, typically 0.02-25 mm/s.

A heavily doped n-type Si substrate with a 300 nm thermally grown SiO\textsubscript{2} layer is degreased in acetone and methanol, and rinsed with hot acetone and hot isopropyl. To make thin film transistors, the semiconductor layer is deposited on top of the SiO\textsubscript{2} with thickness of 30 - 50 nm. Gold is evaporated through a shadow mask to form source and drain electrodes with a 100 \(\mu\)m channel length and 900 \(\mu\)m channel width, creating a "bottom gate, top-contact" transistor geometry in which the substrate serves as the gate contact.

Polarized optical microscopy (Olympus, BXFM) is used to produce images of the thin films. We can identify the fast axis (low refractive index axis) of the grain using a full wave plate (gypsum, \(\Delta = 530\) nm) thereby determining the grain orientation. Movies of the growth process can also be produced with the same microscope,
as shown in Fig. 2.

The electrical measurements are carried out on a microprobe stage (Cascade M150) with Keithley 2636 dual source meter units in the dark with N\textsubscript{2} protection. The field-effect mobility is measured at both saturation and linear regime by transfer characteristic measurement. For the saturation regime, the gate bias is swept from \(-60\) V to \(60\) V and back to \(-60\) V when drain-source voltage fixed at \(-60\) V. The drain current is:

\[
I_{d,\text{sat}} = \frac{W}{2L} \mu_{\text{sat}} C_i (V_g - V_t)^2, \tag{1}
\]

where \(I_{d,\text{sat}}\), \(W\), \(L\), \(V_g\), \(V_t\), \(C_i\) are the drain current, channel width, channel length, gate voltage, threshold voltage and capacitance per unit area (here we use \(C_i\)=10.0 \(nF/cm^2\)). So \(\mu_{\text{sat}}\) can be extracted from the plot \(I_{d,\text{sat}}^{1/2}\) vs. \(V_g\). In the linear regime, the \(V_d\) is fixed at \(-10\) V and drain current is:

\[
I_{d,\text{lin}} = \frac{W}{L} \mu_{\text{lin}} C_i (V_g - V_t)V_d, \tag{2}
\]

so \(\mu_{\text{lin}}\) can be extracted from \(I_{d,\text{lin}}\) vs. \(V_g\).

Charge trapping/detraping is studied by transient effect measurements which as mentioned above, are done in two ways: (i) Drain source current is measured under \(V_g\) biased at \(60\) V for \(300\) s and abruptly switched to \(-20\) V with fixed \(V_d = -20\) V. (ii) \(V_g\) was biased at \(-50\) V for \(300\) s and switched to \(-20\) V when \(V_d = -20\) V. The trap density can be estimated from the transient current based on the model that we discuss in Sec.V.

III. GRAIN STRUCTURE AND TWIN BOUNDARY

Fig. 1 (b) is the schematic of the well defined twin boundary. When the thin film is deposited, the [001] direction is perpendicular to the substrate. Fig. 1 (b) shows the top view of the molecular structure. Note that there are grains with two different orientations. They are separated by a twin boundary which runs parallel to the writing direction. The grain orientation is such that the direction of highest mobility is closely aligned along the writing direction. The Fresnel ellipsoid is depicted, illustrating that the molecular long axis is aligned with the optical slow axis. Assuming the bulk crystal structure,\textsuperscript{25} the angle between the molecular long axis and [100] is \(28^\circ\). So by using polarized microscopy, the reflected light intensity is expected to become extinct upon rotating the sample by \(\pm 28^\circ\) relative to the writing direction. The direction of the rotation depends on whether the grains are in the twinned orientation or not. Fig. 1(c, d) shows that thin films made from 5 wt% solution at a speed of 0.1 mm/s with large grain size are in fact rotated by \(\pm 28^\circ\). The trap density of the two images are complementary indicating a well defined growth orientation along the [100] crystallographic axis with alternating twin grain orientations. The average grain size perpendicular to the writing direction is \(L_g \approx 200\) \(\mu\)m.

When the writing speed is increased, grain nucleation occurs more frequently and the grain size is reduced laterally but the growth orientation and twin grain boundary orientations stay the same. Fig. 3 shows a thin film made at a coating speed of 0.2 mm/s. As shown in Fig. 3 (b) and (c), the extinction in the two
images are exactly complementary.

When the writing speed is further increased above a critical value, the dynamic meniscus become much larger as the solution is pulled out of the capillary by viscous forces leaving a wet film; then the crystallization no longer occurs at a well defined contact line. Instead, nucleation occurs randomly to form a spherulitic grain structure as shown in Fig. 4. A video of the crystallization process is also included in Fig. 2 (online only). Images (c) and (d) are from the region within the black rectangle in image (b), but rotated by ±28°; a particle near the center of this region serves as a mark. When the sample is rotated 28° clockwise, the grain under the particle is dark while the two grains next to it are bright. When it is rotated 28° counterclockwise, the contrast reverses completely showing that the grain orientation of each "stripe" is also along the [100] and the grain boundary is the same twin grain boundary observed at the lower speeds.

FIG. 4. Grain structure of a 35 nm thick film made from a 5 wt% solution at 2.0 mm/s. (a,b) Thin film is placed at 0° with the writing direction with 5× and 20× objective lenses (c) The zoom in image of the region inside the black rectangle of (b), with the sample rotated 28° clockwise. There is a particle serving as a mark, the grain it sitting on extinct, the other two next to it is bright (d) The zoom in image of the black box of (b) by rotating sample 28° counter-clockwise. The grain under the particle reverses the contrast as well the other two next to it which imply the same type grain boundary observed at the lower speeds.

IV. EFFECT OF GRAIN BOUNDARIES ON MOBILITY

A. Electrical measurement and mobility anisotropy

A forty gold pad "quad" structure is utilized for the anisotropy measurement depicted in Fig. 5. Each film drawn from the TIPS-pentacene organic solution covers an array of 58 devices including 38 of them in parallel with the writing direction and 20 in the perpendicular direction. This structure allows us to measure the mobility on both orthogonal directions rapidly over arrays of transistors so that a statistical analysis can be carried out. The I-V output and transfer characteristics of a device with mobility 0.8 cm²V⁻¹s⁻¹ are depicted in Fig. 5 (c) and (d) respectively. Fig. 5 (d) shows a positive threshold and noticeable hysteresis implying a large number of trap states which we will discuss in detail.

Fig. 6 shows that by varying the substrate speed, thin film transistors with different well controlled grain structures can be made. The transistors are made of 5 wt% solution with speed of (a) 0.06 mm/s, (b) 0.2 mm/s, (c) 1.0 mm/s, (d) 2.0 mm/s respectively. The difference of the grain structure is striking. At low speed, because of the well defined contact line of the meniscus, large grains are formed as shown in Fig. 6 (a). When the writing speed is increased, grain nucleation occurs more frequently and the grain size is reduced especially in the direction perpendicular to the writing direction as shown in Fig. 6 (b). Because the grains are long enough to bridge to the channel in the parallel direction the mobility remains at a high value, but the mobility in the direction perpendicular to the writing direction is reduced by a factor of 2.4. When the writing speed is increased above 1.0 mm/s, as shown in Fig. 6 (c) the grain size is further reduced in both directions, and the mobility is correspondingly reduced in both directions. At 2.0 mm/s, the spherulitic grain structure shown in Fig. 6 (d) exhibits the very special "stripe" structure described above. The mobility is the same in both direction because the orientation of the grains in the channel is nearly random. Comparing the grain structure and mobilities at 0.06 mm/s and 0.2 mm/s (Fig. 6 (a) and (b)), μ∥ is almost unchanged, while
μ4 is reduced by a factor more than 2 due to the presence of four grain boundaries across the channel, on average. This effect illustrates convincingly that the grain boundaries are a bottleneck for carrier transport. In order to estimate the potential drop on each grain boundary we adopt a series resistance model with the transistor working in the linear regime:

\[ V_d = \Delta V_{\text{grain}} + N \Delta V_{\text{GB}}, \]  

(3)

where \( \Delta V_{\text{grain}}, \Delta V_{\text{GB}}, N \) are the potential drop on all the grains and potential drop on each grain boundary. Eq. (3) can also be rewritten in terms of effective mobility \( \mu_{\text{eff}}, \) intragrain mobility \( \mu_0, \) and grain boundary resistance \( R_{\text{GB}}. \) Using \( qe n_0 = C_i V_g \) inserted into Eq (2) for \( I_{d,\text{lin}}, \) where \( n_0 \) is the mobile carrier density per unit area induced by gate and \( \Delta V_{\text{GB}} = I_{d,\text{lin}} R_{\text{GB}}, \) we predict a linear relationship between \( 1/\mu_{\text{eff}} \) and the number of grain boundaries \( N \):

\[ \frac{1}{\mu_{\text{eff}}} = \frac{1}{\mu_0} (1 + N f), \]  

(4)

where \( f = \mu_0 R_{\text{GB}} g_e n_0 W/L. \) Thus, it is expected that the mobility will scale with the grain size. To test this idea, linear mobility is measured with \( V_d = -10 \) V for the four samples of Fig. 6 and the estimated grain boundary number \( N \) and the linear mobility of the perpendicularly oriented channel are listed in Table I. It confirms that the linear mobility scales inversely with the number of grain boundaries blocking the channel. A value \( f = 0.33 \pm 0.05 \) is estimated from the data in Table I.

For the case of four grain boundaries, \( N = 4, \) given \( \mu_0 = 0.1, \mu_{\text{eff}} = 0.04 \) and \( V_d = -10 \) V, we can estimate that \( R_{\text{GB}} \approx 10^6 \Omega \) and \( \Delta V_{\text{GB}} \approx 1.3 \) V. This large voltage drop on the grain boundary cannot occur within a 1 nm distance because it would lead to an electric field on the order of \( 10^9 \) V/m, i.e. larger than the breakdown field for most materials. This surprising result suggests that the effective grain boundary thickness is on the scale of 10 nm or more. We note that Teague et al. found a potential drop across a grain boundary of about 1 V by surface potential imaging. Therefore, such a finding is not unprecedented. However it is significant that we conclude that this is the typical behavior of grain boundaries in this materials system when deposited from solution. Given that there are a great many studies of carrier transport in vapor deposited films that show high mobility even for very small grain size, even at the nanometer scale, we speculate that there is a fundamental difference between grain boundaries in solution processed films vs. vapor deposited films, i.e. grain boundaries in small molecule solution processed films appear to present a larger barrier to carrier transport.

### Table I. Mobility measurement for individual transistors with different grain structures, as depicted in Fig. 6

| Sample | Speed (mm/s) | N | \( \mu_{\perp,\text{linear}} \) (cm\(^2\)/V-s) | \( f \) | \( \mu_{\parallel,\text{sat}} \) (cm\(^2\)/V-s) | \( \mu_{\perp,\text{sat}} \) (cm\(^2\)/V-s) |
|--------|-------------|---|---------------------------------|------|-----------------|-----------------|
| a      | 0.06        | 0.1| 0.29                           | 0.04 | 0.29            | 0.17            |
| b      | 0.2         | 0.04| 0.08                           | 0.38 | 0.38            | 0.07            |
| c      | 1.0         | 0.02| 0.05                           | 0.33 | 0.058           | 0.037           |
| d      | 2.0         | 0.01| 0.07                           | 0.28 | 0.015           | 0.015           |

In the saturation regime Eq.(4) should still be valid aside from the numerical value of \( f \). Therefore, we also examine the correlation between the saturation mobility and the grain size. Fig. 7 shows a clear linear relationship between \( 1/\mu_{\text{eff}} \) and grain boundary number \( N \), again implying the validity of the series resistance model.

### B. Transistor array measurements

Saturation mobility of the parallel and perpendicular channel on arrays of devices is shown in Fig. 8. Each data point is a statistical collection of 38 mobility measurements for \( \mu_{\parallel,\text{sat}} \) and 20 for \( \mu_{\perp,\text{sat}} \). Note that at 0.02 mm/s a relatively large error bar for the mobility is found because the grain orientation has a significant variation. Since a single grain dominates each transistor, the angle variation is translated to a variation in the measured mobility due to the intrinsic mobility anisotropy of the material. All other data exhibit small variations, showing that the thin film fabrication method is highly repeatable. Thus, the difference of the mobility as the speed is varied is predominantly...
V. TRANSIENT EFFECT MEASUREMENT

In subsection V A, the transient effect of the devices are measured while switching from the off state ($V_g = +60$ V for 300 s, to ensure that the electron traps are maximally filled) to the on state ($V_g = -20$ V). We observe two different effect: (i) “slow” bias stress effect, with time constant $\sim 10^4$ s. Here we adapt the model recently proposed by Lee et. al, that is, the decay of the current is caused by holes drifting into the insulator that is believed to be mainly responsible for the hysteresis in transfer curves. This effect is correlated with the grain boundary density with time constant $\approx 40$ s.

In subsection V B the transient effect of the devices are characterized while switching from $V_g = 0$ to $-50$ V and then from $V_g = -50$ V to $-20$ V with $V_{ds} = -20$ V. This measurement is designed to be sensitive to hole traps, since when switching between two different negative gate voltages, the electron traps should be mainly depopulated in both states. A reversible effect is observed with time constant $\approx 10$ s, possibly due to holes diffusing into traps at the grain boundaries and other defects.

A. Bias stress effect and electron trapping at grain boundaries

Transient phenomena were studied to understand the relationship between the trap states and grain structure. First we describe a simple model that we use to separate the slow bias stress from the reversible effects. The key feature of the model is that the density of mobile carriers $n_{mob}(t)$ change with time when the device is turned on. In general, this can be either due to electron traps discharging or hole traps charging. The density of charged electron traps as a function of time is represented as $n_{et}(t)$, and these trapped electrons induce an equal density of mobile holes $n_{hi}(t) = n_{et}(t)$ thereby adding to the drain current. Conversely, charged hole traps represented as $n_{ht}(t)$ remove carriers from participating in current flow. Combining these terms with the total gate charge density $n_0$, which depends only on the gate voltage and capacitance, we have:

$$n_{mob}(t) = n_0 - n_{ht}(t) + n_{hi}(t).$$

In order to model the slow bias stress effect, we follow...
Table II. Fitting parameter for the transient current when \( V_g \) was switched from +60 V to -20 V with \( V_d = -20 \) V. Heated samples were heated to 60° during TIPS-pentacene deposition. Note the abbreviated subscripts: \( sat \) = saturation, \( lin \) = linear, \( dr \) = drift, \( hi \) = induced holes, \( et \) = electron trap.

| Sample orient. | Temp (°C) | speed (mm/s) | conc. (wt%) | \( \mu_{sat} \) (cm² V⁻¹ s⁻¹) | \( \mu_{lin} \) (cm² V⁻¹ s⁻¹) | \( \tau_{dr} \) (s) | \( \beta_{dr} \) | \( n_{hi}(0) \) (10¹¹ cm⁻²) | \( \tau_{et} \) (s) | \( \beta_{et} \) |
|----------------|-----------|--------------|-------------|-----------------------------|-----------------------------|----------------|-------------|---------------------|----------------|-------------|
| A              | 25        | 2            | 5           | 0.02                        | 0.02                        | 8000          | 0.51        | 3.30                | 40             | 0.50        |
| B              | 25        | 2            | 5           | 0.015                       | 0.013                       | 8000          | 0.51        | 3.55                | 40             | 0.50        |
| D              | 25        | 2            | 5           | 0.013                       | 0.011                       | 20000         | 0.55        | 4.68                | 30             | 0.55        |
| E*             | 25        | 2            | 5           | 0.0048                      | 0.0024                      | 15000         | 0.50        | 10.27               | 40             | 0.54        |
| C              | 25        | 0.2          | 5           | 0.28                        | 0.129                       | 35000         | 0.55        | 1.24                | 15             | 0.55        |
| C*             | 25        | 0.2          | 5           | 0.07                        | 0.029                       | 8000          | 0.54        | 2.24                | 50             | 0.50        |
| H              | 25        | 0.08         | 5           | 0.31                        | 0.127                       | 26000         | 0.55        | 1.19                | 22             | 0.53        |
| N              | 60        | 0.1          | 0.3         | 0.80                        | 0.19                        | 8000          | 0.51        | 1.50                | 22             | 0.55        |
| L*             | 60        | 0.1          | 0.3         | 0.13                        | 0.048                       | 35000         | 0.55        | 1.77                | 28             | 0.55        |

By fitting the transient current curve with Eq. (6), the trap density can be extracted and is listed in Table II for representative samples. In order to model the drain current, the expression for \( n_{mob}(t) \) above is inserted into Eq. (2) with \( C_t V_g \rightarrow q_e n_{mob}(t) \). Eq. (6) also requires the linear mobility, which was measured from transfer curves with \( V_d = -6 \) V for each sample. Table II also lists extracted parameters for selected samples, including the stretching exponents, which were found to be in the typical range for similar processes.\(^{19}\) The extracted values of \( n_{hi}(0) \) show devices with smaller mobility values have larger trap state densities, suggesting a correlation with the presence of grain boundaries.

In Fig. 2 we present detailed results for samples C and E*. Fig. 2(a) and (b) show how the current decays after the gate bias is switched from 60 V (off state) to -20 V (on state) for sample C. When the gate is biased at 60 V, the electron trap states are filled and thus induce mobile holes. Once the gate bias is switched to -20V, the trapped electrons depopulate, resulting in a decay of the induced hole density and hence of the drain current, with a time constant of 15 s (see Table II). The lower curve in (b) shows the curve corresponding to only the bias stress component (time constant 35000 s). The full fit, including both terms of Eq. (6) is seen to match the data almost perfectly, thus demonstrating the utility of the model in separating the two transient components. A relatively small effect of the reversible component is observed, corresponding to an electron trap density, when fully filled, of \( \approx 10^{11} \) cm⁻². We consider sample C, which has one of the lowest trap densities of all of the samples that we measured, to be characteristic of samples with a nearly single crystal semiconductor layer. Fig. 3(c) and (d) show results for the extreme opposite case, sample E*, which has a very small grain size and a grain morphology similar to the one shown in Fig. 3(d). We extract an electron trap density of \( \approx 10^{12} \) cm⁻². In this case, we interpret the time constant \( \tau_{et} \) as being characteristic of electron detrapping. If we assume that most of the extra traps are associated with the presence of grain boundaries, then the density of traps per grain boundary, with \( N \approx 30 \) for sample E*, is on the order of \( 10^{10} \) cm⁻². This is a remarkably large density in the sense that, taking into account geometric factors such as the area of the transistor channel and the thickness of the semiconductor film (35 nm), the density of trap states on each grain boundary is calculated to be \( > 10^{13} \) cm⁻². Based on electrostatic considerations, this density is probably too high to be present at a planar boundary. However, since traps are spatially localized on grain boundaries rather than being randomly distributed over the channel, they can form a bottleneck at a lower overall average density. Therefore, the calculation above may be an overestimate. This possibility is discussed below in Sec. VI.

Table II also lists results for heated substrates. Due to the increased evaporation rate of the solvent at elevated temperatures we can produce large grain size and high mobility at higher speed when the substrate is heated. Surprisingly the carrier mobility is more than double the highest value that we have measured previously. However, the trap density deduced from transient measurement is not reduced compared to lower mobility large grain samples prepared at room temperature. This indicates that the difference in mobility is not correlated with a reduction in trap states. Note that we are compar-
FIG. 9. Transient effect measurement with switching gate bias from 60 V to −20 V. (a) Large grain size ($L > 200 \mu m$) with mobility of 0.28 cm$^2 V^{-1} s^{-1}$. (b) The later 900 s measurement of (a) when gate bias is −20 V after bias with 60 V for 300 s, long dashed line below the data points is a single stretched hyperbola function with $\tau_{dr} = 35000$ s and $\beta_{dr} = 0.55$, solid line is the sum of the stretched hyperbola function and stretched exponential function. (c) Small grain size ($L = 1 \sim 2 \mu m$) with mobility 0.0048 cm$^2 V^{-1} s^{-1}$. (d) The later 900 s measurement of (b) when gate bias is −20 V after bias with 60 V for 300 s, long dashed line below the data points is a single stretched hyperbola function with $\tau_{dr} = 15000$ s and $\beta_{dr} = 0.55$, solid line is the sum of the stretched hyperbola function and stretched exponential function.

FIG. 10. Transient measurement with switching gate bias from −50 V to −20 V. (a) Large grain size ($L > 200 \mu m$) with mobility of 0.28 cm$^2 V^{-1} s^{-1}$. (b) The first 300 s measurement of (a) when gate bias is −50 V, long dashed line crossing the data points is a single stretched hyperbola function with $\tau_{dr} = 5500$ s and $\beta_{dr} = 0.6$, the dashed line is for $\beta_{dr} = 0.5$ and the solid line is for $\beta_{dr} = 0.7$. (c) Small grain size ($L = 1 \sim 2 \mu m$) with mobility 0.0048 cm$^2 V^{-1} s^{-1}$. (d) The first 300 s measurement of (b) when gate bias is −50 V, solid line is the sum of the stretched hyperbola function and stretched exponential function. The long dashed line is the stretched hyperbola function only. The inset shows the stretched exponential component of the fit, along with the data minus the bias stress component.

B. Reversible hole trapping/detrapping

Another variation of the transient effect measurement is carried out with switching between two negative gate voltages. In Fig. 11 data for samples C and E* is presented. Compared to Fig. 9 this measurement brings the Fermi level closer to the valence band maximum, where hole traps are more likely to be found. The drain current is measured starting when the gate bias is switched from 0 V to −50 V (on state). After 300 s the gate is switched to −20 V for 900 s. Fig. 11(a) and (b) show the results for sample C. A gradual decrease in drain current is observed when the device is first turned on. After switching to the smaller gate voltage, a small increase is observed over the first ≈ 60 s, followed by stable operation. Fig. 11(c) and (d) show the same measurement for sample E*. The data shows a much larger relative change over the first minute compared to sample C. It is clear from inspection of (d) that the trapping/detrapping process is reversible with the same time constant in each direction. Furthermore, the similar magnitude of the effect in each direction suggests that most of the trap states exist at energies relative to the valence band maximum that are accessible between the two negative gate voltages. Therefore, it is plausible that the transient effect observed at negative gate voltages correspond mainly to filling and emptying of hole trap states.

We use the same model developed in Sec. VA to fit this data. A minor difference is the assumption that hole traps are being filled, as discussed above. Therefore, after switching to −50 V (t = 0 in the figure) $n_{ht}$ ($ht$ = holes trapped) is extracted from the fitting rather than $n_{hi}$ ($hi$ = holes induced). Taking the hole trap density to be $n_{ht}(\infty)$ and assuming that $\tau_{dr} \gg \tau_{diff}$,
of Fig. 11 (a) with Fig. 7, a simple linear relationship between the 1/µeff and the number of grain boundaries in the channel. Combining the results of Fig. 11 (a) with Fig. 4, a simple linear relation between neF and number of grain boundaries is deduced as shown in the Fig. 11 (b). Note that since this is a combination of results from two data sets, we omit the data points and simply show a plot of the correlation. The trap density per grain boundary is estimated to be 1.0 × 10^{10} cm^{-2}, and the intercept value, 1.2 × 10^{11} cm^{-2}, is the electron trap density due to the defects not associated with grain boundaries. The dashed line in Fig. 11(b) is the same plot for hole traps. In this case, the density is 2 × 10^{9} cm^{-2} per grain boundary. Since the traps are thought to be inhomogeneously distributed in the channel because they are associated with grain boundaries, a more natural unit is per grain boundary length. Multiplying by the channel length (100 µm), the hole trap line density is λh ≈ 2 nm^{-1} along a grain boundary. However, this latter value probably overestimates the local trap density as we discuss below.

\[ n_{\text{mob}} \approx \frac{n_0 - n_{\text{ht}}(\infty)}{1 + (t/\tau_{\text{dr}})^{\beta_{\text{dr}}}} + n_{\text{ht}}(\infty) \exp(-t/(\tau_{\text{diff}})^{\beta_{\text{diff}}}) \]

(7)

Note that this expression is for the time interval with V_g switch from −50 V to −20 V with V_d = −20 V.

TABLE III. Fitting parameter for the transient current when V_g switch from −50 V to −20 V with V_d = −20 V.

| Sample | Speed (mm/s) | Concentration (wt%) | µ_{sat} (cm^{2}V^{-1}s^{-1}) | µ_{lin} (cm^{2}V^{-1}s^{-1}) | n_0 - n_{ht}(\infty) (10^{11}cm^{-2}) | \tau_{\text{dr}} (s) | \beta_{\text{dr}} | n_{\text{ht}}(\infty) (10^{11}cm^{-2}) | \tau_{\text{diff}} (s) | \beta_{\text{diff}} |
|--------|--------------|---------------------|-----------------|-----------------|-------------------------|--------|--------|-------------------------|--------|--------|
| C      | 0.2          | 5                   | 0.28            | 0.129           | 32.1                    | 5500   | 0.60   | NA                      | NA     | NA     |
| E*     | 2            | 5                   | 0.0048          | 0.0024          | 30.8                    | 7000   | 0.60   | 2.30                    | 13     | 0.55   |

*devices are measured at perpendicular channel.

In order to fit the data in Fig. 10(d), a second component corresponding to the reversible process is deduced. The time constant is 13 s, which we suggest to be characteristic of hole diffusion into grain boundaries. Note that the recovery after switching the gate to −20 V is also consistent with this picture since detrapping of holes with a nearly identical time constant neatly explains the observed increase in the drain current. A similar model based on hole detrapping has been proposed to explain transient measurements of vapor deposited pentacene field-effect transistors.\(^{40}\)

C. Correlation of trap states with grain boundaries

Fig. 11 (a) shows the electron trap density (n_{et}) extracted from transient current data as described above, and plotted versus the inverse of the saturation mobility. A linear relationship is observed, suggesting that the traps are correlated with the mobility. This is not believed to be a causal relationship, and instead both are believed to be directly determined by the grain boundary density. In Fig. 7 we found the linear relationship between 1/µ_{eff} and the number of grain boundaries in the channel N. Combining the results of Fig. 11 (a) with Fig. 4 a simple linear relation between n_{et} and number of grain boundaries is deduced as shown in the Fig. 11 (b). Note that since this is a combination of results from two data sets, we omit the

VI. DISCUSSION

In this section we discuss the results in terms of possible models for the grain boundary structure. First, we note that the large grain boundary resistance deduced in Sec. IV A is consistent with conducting probe atomic force microscopy results on vapor deposited sexithiophene single grain boundary.\(^{\text{41,42}}\) Several previous studies have noted a correlation between grain size and mobility\(^{24,42}\) or have deduced the effect of grain boundaries by vary-
ing the transistor channel length in organic field effect transistors. Such effects have been particularly prevalent, and problematic, in solution deposited films. Therefore, we suggest that high grain boundary resistance is a typical feature of solution processed organic semiconductor films, although this may be more closely related to the crystal packing than to the processing conditions *per se*, as we explain below. Conversely, there are many examples of vapor deposited films where grains size appears to be of secondary importance, pointing to the possibility that vapor deposited films are less susceptible to such effects.

It has been suggested by Rivnay et al. that high grain boundary resistance can be related to crystal packing since herringbone-type molecular films can readily have low molecular misorientation across large-angle boundaries. On the other hand, π-stacked crystal structures, of which TIPS-Pentacene is an example, are thought to be most susceptible to having only large molecular misorientation across grain boundaries, leading to high grain boundary resistance. We can extend this idea by pointing out that many vapor-deposited organic semiconductors have a herringbone arrangement, which accounts for the general trends alluded to above.

Our data is relevant to this discussion because in order to hold the large voltage drop that we observe, the boundary cannot be molecularly abrupt as generally assumed. Following the crystal packing arguments of Rivnay et al, we assume that the dominant grain boundary that we depict in Fig. 1 (b) is a relatively high energy structure because of the large (56°) misorientation of the molecules across the interface. In this case a high degree of disorder near the boundary follows logically from these arguments, since the molecules near the boundary may become rotated or displaced in order to reach a more favorable local configuration. While there may well be other effects that influence the grain boundary resistance, e.g. related to the processing conditions, this simple model appears to be consistent with our results, as well as a large body of the existing literature.

Hole traps at grain boundaries have been reported by several groups in which spatial maps of trapped positive charge has been observed. Our observation of hole traps correlated with grain boundaries is consistent with these studies. However, our estimates of trap densities appear to overestimate the trap densities after accounting for the localization of the traps in the region of the grain boundaries. Since the grain boundaries are a bottleneck to current flow, the drain current should be very sensitive to trap densities that alter the mobile carrier concentration in the grain boundary. But, given that the transient effects that we observe in Figs. 9 and 10 only modulate the drain current by a small amount, the density of trapped charge producing the transient effect must be small compared to total density of mobile carriers, i.e. \( \lambda_n < 0.1 \) nm\(^{-1} \), which is considerably lower than the value estimated above.

Note that this effect can also be recast in terms of a barrier model since it produces a local reduction in mobile carriers by electrostatic repulsion from fixed charge, which is the essential mechanism of the grain boundary barrier model. However, we reiterate that since the transient effects are weak, barriers cannot be the primary cause of the large grain boundary resistance. Therefore, a simple trap model without significant barrier effects is the most natural way to explain the drastically reduced mobility when grain boundaries are present. This is plausible because a high density of shallow traps is likely to accompany the relatively deep traps that are responsible for the reversible transient currents. This model can be implemented by assuming two different mobilities, one for the grains \((\mu_0)\) and the other for the disordered region within the grain boundaries \((\mu_{GB})\). With this model, we can extend the discussion of Sec. IV A, and find a complementary form for the \( f \) factor in Eq. 3 from which we can estimate the grain boundary mobility,

\[
f = \frac{L_{GB}}{L} \left( \frac{\mu_0}{\mu_{GB}} - 1 \right). \tag{8}
\]

A similar expression has been derived by Chen et al. We take the grain boundary thickness \( L_{GB} \) to be about 10 nm. With \( f = 0.33 \) and \( \mu_0 = 0.1 \) cm\(^2\) V\(^{-1}\)s\(^{-1}\), we estimate the mobility within the grain boundaries to be \( \mu_{GB} = 3 \times 10^{-5} \) cm\(^2\) V\(^{-1}\)s\(^{-1}\). This value is in line with typical values obtained for disordered organic semiconductor materials.

VII. CONCLUSIONS

Solution-processed TIPS-pentacene thin films are fabricated by a rectangular stylus. The grain size of the thin films can be varied over a wide range, from a few micrometers up to millimeter depending on the substrate speed and temperature, with the [100] crystallographic axis of the grains aligned with the writing direction for speeds \( \leq 1 \) mm/s, and randomly oriented for higher speeds. Measurements of anisotropic mobility reveal that grain boundaries are a bottleneck for carrier transport. A potential drop at individual grain boundaries of more than a volt is deduced. Transient measurements reveal a reversible charge trapping associated with grain boundaries. Straightforward analysis of the data suggests that shallow traps within disordered grain boundaries with a grain boundary thickness of at least 10 nm can explain the results, although transient currents are evidence for modest barrier effects.
VIII. ACKNOWLEDGEMENT

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