Design and Implementation of an Asymmetric Cascaded H-bridge Fifteen Level Inverter with Minimum Number of Switches for Smart Grid Applications

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ABSTRACT. Multilevel inverters are nowadays getting more and more attention in the industrial world due to the attractive features offered by the multilevel inverters. However, usage of more semiconductor switches in the higher levels of these inverters poses a restriction to its wider applications in the industries. Therefore, a novel fifteen level inverter of cascaded H-bridge topology is being designed and implemented, that incorporates the minimum number of switches, thus confirms the reduction in size, minimum switching losses and further reduction in overall cost of the multilevel inverter. The foremost concern of the suggested work is to improve the efficiency and quality of the desired voltage waveform of the multilevel inverter using the effective controlling strategies keeping harmonics at a lower level. The control methods are applied to the fifteen level inverter for further improvement in the voltage regulation and thereby lead to the better efficiency, reliability and economic improvement. The performance assessment of the implemented fifteen level inverter has been done in respect of the total harmonic distortion and switching losses and is compared with the other existing topologies. The implemented inverter is well suited for drive, renewable energy and smart grid applications.

Keywords: Multilevel Inverter (MLI), Harmonics, Cascaded H-Bridge (CHB) Inverter, Pulse Width Modulation (PWM), Space Vector Modulation (SVM)

1. Introduction

Role of the smart grids are very prominent in the modern era. For reliable source of power, smart grids provide the technologies that improve the any fault detection and self heal the power network without interrupting the supplied electricity. Smart grid technology can sustain a huge number of fluctuations caused due to weather conditions [1]. Multilevel Inverters (MLIs) are playing a very vital role in the smart grid technology. Due to the benefits offered by the MLIs for e.g. harmonics reduction, reduced switching and conduction losses, increased voltage stability and better quality of power, smart grid technology becomes more and more reliable and flexible nowadays [2]. Because of improved flexibility of the MLI based smart grid, the transmission from the solar power and wind power, which are Renewable Energy Sources (RESs) is permissible now. In fact, MLIs are emerging as an attractive solution for the smart grid applications in comparison with the conventional inverters [3]. Due to rise in the levels of the MLIs, more and more semiconductor devices are required, which ultimately causes an increase in complexity and overall system cost. Therefore, there is a need to decrease the complexity by reducing the components and number of switches used in the MLIs. This is possible with the hybrid topologies of the MLIs and also there is considerable reduction in the overall system cost using these hybrid topologies of the MLIs.
The three common structures of the MLIs are Neutral Point Clamped (NPC), Flying Capacitor (FC) and Cascaded H-bridge (CHB) structures that are most widely used. These structures are very popular nowadays due to their modular structure and the ability of generating staircase sinusoidal output waveform with lower Total Harmonic Distortion (THD) [4, 5]. Some of the key features of the MLIs are better output waveform with lower THD and lesser harmonics, efficient working of the system at fundamental and higher switching frequency and different switching redundant states etc. However, one of the disadvantages of these MLIs structures is the need of higher number of switching appliances. To reduce the components and semiconductor switches, optimal use of semiconductor devices and reduction in overall loss have been a topic of investigation in the area of power electronics. Different hybrid topologies of the MLIs used for numerous applications have been demonstrated in the literature [6-7]. Main aim of these hybrid topologies is to minimize the components and switching devices keeping the harmonics at a lower level. Figure 1 depicts the possible energy sources connected with the reduced number of switches based MLI and its applications.

![Multilevel Inverter with Reduced Switches and its Applications](image)

**Figure 1 MLIs with Minimum Number of Switches and its Applications**

With the development in the MLI topologies, some issues have been raised related to the modulation and controlling of these inverters [8]. Lower order harmonics appear in the desired staircase voltage waveform of the MLI. These harmonics affect badly the voltage quality and power quality of the MLI output waveform. Using the appropriate and optimized control and modulation strategy, these aforesaid challenges can be well addressed. In this research article, design and implementation of a MLI system with reduced number of switches has been proposed. A CHB fifteen level inverter topology with viable controlling strategies has been implemented here. The proposed system makes use of Level shifted Pulse Width Modulation (LS-PWM) and In phase and Quadrature

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Space Vector Modulation (SVM) strategies. System is being implemented at three different frequencies i.e. 50 Hz, 100 Hz and 200 Hz. Finally, the implemented system is compared with the some existing systems in terms of required number of switches and the obtained THD.

2. Proposed Multilevel Inverter System

Level shifted pulse width modulation and space vector modulation is being used for the implementation of the proposed inverter system. Phase Disposition (PD), Phase Opposition Disposition (POD) and Alternate Phase Opposition Disposition (APOD) are the three control strategies used for the designed system. The implemented MLI system is represented in figure 2.

A cascaded multilevel inverter system makes use of series of H-bridges. Direct current sources used in MLI system are various DC batteries and renewable sources such as PV etc. A hybrid topology is being used for the designing of the proposed fifteen level inverter system, which ensures the smooth and efficient working of the MLI system.
2.1 Switching pattern scheme for the proposed fifteen level inverter system

The switching sequences of power switches $S_{11}$, $S_{12}$, $S_{13}$, $S_{14}$, $S_{15}$, $S_{16}$ and $S_{17}$ are shown in table 1. Operational mode 1 represents that the power switches $S_{11}$, $S_{12}$, $S_{13}$ & $S_{14}$, $S_{15}$ are in ON (1) position, the maximum obtained voltage across the load is $+V_{dc}$. Operational mode 2 shows that the switches $S_{12}$, $S_{13}$ & $S_{14}$, $S_{15}$ are in the ON position, the obtained voltage is $+5V_{dc}/7$. Operational mode 3 represents that the switches $S_{11}$, $S_{13}$ & $S_{14}$, $S_{15}$ are in 1 position i.e. ON and the obtained voltage is $+3V_{dc}/7$. Operational mode 4 depicts that the switches $S_{13}$ & $S_{14}$, $S_{15}$ are in 1 position and the obtained voltage is $+4V_{dc}/7$. Mode 5 shows that the switches $S_{11}$, $S_{12}$ & $S_{14}$, $S_{15}$ are ON and the obtained voltage is $+3V_{dc}/7$. Similarly, for different modes some of the power switches are ON condition and some switches are in OFF condition. Table 1 summarizes the switching pattern of semiconductor switches of fifteen level inverter.

| Output Voltage | Switching Pattern |
|----------------|--------------------|
|                | $S_{11}$ | $S_{12}$ | $S_{13}$ | $S_{14}$ | $S_{15}$ | $S_{16}$ | $S_{17}$ |
| $+7V_{dc}$     | 1       | 1       | 1       | 1       | 1       | 0       | 0       |
| $+6V_{dc}$     | 0       | 1       | 1       | 1       | 1       | 0       | 0       |
| $+5V_{dc}$     | 1       | 0       | 1       | 1       | 1       | 0       | 0       |
| $+4V_{dc}$     | 0       | 0       | 1       | 1       | 1       | 0       | 0       |
| $+3V_{dc}$     | 1       | 1       | 0       | 1       | 1       | 0       | 0       |
| $+2V_{dc}$     | 0       | 1       | 0       | 1       | 1       | 0       | 0       |
| $+1V_{dc}$     | 1       | 0       | 0       | 1       | 1       | 0       | 0       |
| $0V_{dc}$      | 0       | 0       | 0       | 1       | 0       | 1       | 0       |
| $0V_{dc}$      | 0       | 0       | 0       | 0       | 1       | 0       | 1       |
| $-1V_{dc}$     | 1       | 0       | 0       | 0       | 0       | 1       | 1       |
| $-2V_{dc}$     | 0       | 1       | 0       | 0       | 0       | 1       | 1       |
| $-3V_{dc}$     | 1       | 1       | 0       | 0       | 0       | 1       | 1       |
| $-4V_{dc}$     | 0       | 0       | 1       | 0       | 0       | 1       | 1       |
| $-5V_{dc}$     | 1       | 0       | 1       | 0       | 0       | 1       | 1       |
| $-6V_{dc}$     | 0       | 1       | 1       | 0       | 0       | 1       | 1       |
| $-7V_{dc}$     | 1       | 1       | 1       | 0       | 0       | 1       | 1       |

2.2 Proposed Control Strategies for Multilevel Inverter System

Level shifted pulse width modulation and in phase and quadrature space vector pulse width modulation strategies are being applied for the proposed multilevel inverter system. In level shifted pulse width modulation strategy, numerous carrier signals are used. These carrier signals are arranged in various levels and every carrier signal is having same frequency and amplitude. This control strategy is categorized into three forms i.e. phase disposition, phase opposition disposition and alternate phase opposition disposition. Amplitude modulated (AM) signals which are sinusoidal in nature are termed as in phase quadrature signals. Voltage and current signals are in quadrature form in this particular type of control strategy. This implies that these two waveforms are symmetrical i.e. the obtained output voltage is under control. As the proposed system makes use of these two techniques so the voltage obtained at the output section is controlled.
3. Simulation Results

The implemented system makes use of seven switches for the designing of fifteen level inverter. Therefore, there is considerable reduction in the power switches required for fifteen level CHB inverter. Figure 3 depicts the Simulink model for the proposed asymmetric CHB MLI. The power semiconductor switches used are MOSFET. Specification parameters of the designed MLI system are shown in table 2.

Table 2 Parameters of the Implemented fifteen level CHB MLI System

| Parameter                      | Specification |
|--------------------------------|---------------|
| Input Voltage (volt)           | 50, 100, 200  |
| Reduced Number of Switches     | 7             |
| Resistive Load (ohms)          | 10            |
| Frequency (Hz)                 | 50, 100       |
| Total Number of Levels         | 15            |

The implemented fifteen level CHB inverter makes use of three unequal DC sources. The DC source magnitudes are designed with the voltages such as 50Vdc, 100Vdc, 200Vdc respectively and the fifteen levels inverter is designed with seven switches. Figure 3 depicts the Simulink model for the proposed MLI system. Despite of growing importance and advantageous of MLI based systems, one of the major drawback is the presence of significant amount of unwanted harmonics in its output voltage and current. Generally, harmonics tend to exhibit severe effects on electrical and mechanical components such as increase in losses in the system, reduction in overall system performance and life span of the system reduces. To overcome these problems, research has been carried out to control or mitigate the effects of harmonics in inverters. The most fundamental aspect is to select the proper switching scheme for the semiconductor devices to reduce the Total Harmonic Distortion (THD). Term THD is used to indicate the quantity of harmonics contents and is defined in terms of the amplitudes of the harmonics \( H_n \), at frequency \( n\omega_0 \), where \( \omega_0 \) is frequency of the fundamental component having amplitude \( H_1 \) and \( n \) is integer. The THD is mathematically given by:

\[
THD = \sqrt{\frac{\sum_{n=2}^{\infty} H_n^2}{H_1^2}}
\]  

To minimize the THD in the output waveform of MLI based systems, there is a strong requirement to select the proper switching strategy for the firing of switching devices in the MLI system. Therefore, the switching strategies are important to study and investigate for reliable and efficient working of MLI based systems. There are many issues of concern in the designing of a MLI system such as maintaining the harmonics at a lower level, to ensure better voltage quality, reduction in switching losses and minimization of number of switching devices used to further reduce the overall cost of the system. Asymmetrical MLIs are alternative to minimize the THD of the obtained output voltage without an increase in the power semiconductor devices used. Usage of different values of DC
voltages promotes the use of hybrid topologies of the MLI system, which employ different modulation strategies and optimization techniques and the ultimate aim is to optimize the voltage quality of the overall system.

Figure 3 Simulation Model for the 15 level MLI
THD analysis for the proposed system has been done and is compared with the already existing traditional inverters, which is shown in figure 4.

![Proposed System vs Existing System at 50 Hz, 100 Hz, and 200 Hz frequency](image)

**Figure 4** Proposed and Existing Systems at 50 Hz, 100 Hz, and 200 Hz frequency

THD obtained at 50 Hz frequency in the proposed system is 5.23%, which is very low in comparison with the existing systems as depicted in figure 5. The proposed system results in the minimum THD i.e. 5.23 % at the frequency of 50 Hz. Table 3 indicates the performance of the proposed system in terms of THD and power factor and is compared with the existing traditional systems [9, 10].
Table 3 Proposed system and conventional systems

| Method                                      | THD (%) | Power Factor |
|---------------------------------------------|---------|--------------|
| System designed by Madhusudhana et al. [9]  | 6.67    | 0.669        |
| System designed by Meenakshi et al. [10]   | 5.78    | 0.776        |
| Proposed System                             | 5.23    | 0.887        |

4. Conclusion

One of the essential requirements in today’s industrial world is reduction in cost of power electronics devices. Multilevel inverters with minimum number of switches are preferable over the conventional inverters. An adaptive fifteen level CHB multilevel inverter system with minimum switches has been introduced and implemented with the aid of modified level move and in stage quadrature space vector pulse width modulation controlling strategies. The THD for the proposed multilevel inverter is 5.23% at the fundamental frequency 50 Hz. As compared to other existing multilevel inverter systems, THD is less. Also, the designed fifteen level inverter system provides the higher output voltage quality with relatively minimum power losses and harmonics. The proposed multilevel inverter system is capable for drive and smart grid applications.

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