An optimization method of clock synchronization for large-scale regional power network based on IEEE 1588

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Abstract—At present, mobile devices generally use GPS, Beidou and other satellite time service methods to obtain time, but the clock synchronization based on IEEE 1588 protocol still has deviation. To solve this problem, a clock synchronization method is proposed to improve IEEE 1588 protocol. Based on the analysis of IEEE 1588 protocol, the clock deviation and frequency deviation which affect the synchronization accuracy are modeled. The second-order Kalman filtering algorithm is used to recursively deduce the clock deviation and frequency deviation, and the Allan variance is used to verify the noise characteristics and constantly correct the clock deviation. Finally, the improved effect is verified by relevant experiments. The results show that the improved system can improve the synchronization accuracy.

1. Introduction.

As the research on Beidou satellite navigation technology started late in China, and the relevant technologies are not mature enough at present, the navigation chips in China are purchased through domestic agents of foreign manufacturers, and the core technology has not been formed for a long time, which also limits the development of China's navigation system[1]. At this stage, China's power enterprises mainly rely on GPS time synchronization technology, and satellite time service products are mainly single products, with only a small number of dual system products, Beidou three system products and single Beidou products[2]. However, limited by the United States and free of charge, it has low reliability and poor autonomy[3]. With the development and improvement of Beidou satellite navigation system in China, and in order to avoid the incalculable serious consequences to the power industry, many domestic enterprises and scholars have carried out the research on Beidou satellite navigation technology and its related products.

The accuracy of clock synchronization largely determines the performance of distributed network measurement and control system, so clock synchronization is very important for distributed network measurement and control system. IEEE 1588 clock synchronization protocol is based on network clock synchronization[4]. Assuming that the network line between master and slave clock modules has equal delay, the synchronization deviation correction of slave clock relative to master clock is completed by calculating clock deviation. In many network environments, the assumption of peer delay of master-slave clock lines can not be established, which leads to large deviation of synchronization accuracy[5]. The root cause of clock deviation is frequency deviation. The protocol only compensates the clock deviation of master-slave clock, but not the frequency deviation.

The time service function of Beidou system is to broadcast the time service information regularly by the ground central control system to provide the time service user with the time delay correction
value. According to the time delay correction value, the time service user continuously adjusts the local clock to align it with Beidou standard time, or control the time difference within a certain range. Beidou user machine provides two time service modes: vehicle direction time service and two-way time service.

Based on the deep analysis of IEEE 1588 protocol, this paper models the clock deviation and frequency deviation which affect the synchronization accuracy. Second order Kalman filtering algorithm is used to recursively deduce the clock deviation and frequency deviation, and Allan variance is used to verify the noise characteristics and constantly correct the clock deviation. The clock synchronization accuracy of the improved method is tested through experiments to verify the effectiveness of the improved method.

2. IEEE 1588 protocol.

IEEE1588 protocol is also called precise synchronization clock protocol, that is, PTP (Precision Time Protocol). PTP system is a distributed network structure, and the logical range of protocol operation is called a domain. PTP system consists of one or more PTP subdomains. In a PTP system, the grandmaster clock provides the time source of the whole system. The implementation protocol only needs to add time synchronization messages to the original network, which only takes up a small amount of network resources. By calculating the network transmission delay accurately, the time deviation from the clock to the master clock is calculated, and then the local time is adjusted to match the time of the clock source.

IEEE1588 synchronization system is a system composed of publisher and receiver. During the operation of the system, the master clock acts as the time publisher, publishes the local time to the network every other period of time, and the slave clock receives the time according to its own domain and priority. At the same time, the line delay is calculated from time to time to ensure accurate synchronization according to the network situation.

![Fig.1. Schematic diagram of IEEE1588 synchronization](image)

The process of IEEE 1588 clock synchronization is as follows: (1) the master clock sends a sync message to the slave clock every certain time (sync interval). The master node records the sending time stamp TM1, but TM1 is not sent with sync. The slave clock records the time stamp TS1 when it receives sync. (2) The master sends a follow up message containing the TM1 timestamp mark recorded the previous time sync was sent (3) Send delay from node to master_ The request message and the timestamp TS2 at the time of the message are recorded. The time stamp TMS2 is recorded after the master node receives the message. (4) The master node returns a delay-response to the slave node. This message contains the TM2 mark of the previous record. After the
slave node receives this message, it uses the TM1, TS1, TS2, TM2 to calculate the time delay between it and the master node. The specific synchronization process is shown in Fig.1.

The synchronization calculation process includes delay value calculation and offset value calculation. The delay value is the average value of message transmission delay between slave nodes, and the offset value is the time deviation between slave nodes. The calculation formula is as follows:

\[
\text{Delay} = \frac{\text{delayMS} + \text{delaySM}}{2} = \frac{T_{s1} - T_{m1} + T_{m2} - T_{s2}}{2} \quad (1)
\]

\[
\text{offset} = \theta(k) = T_{s1} - T_{m1} - \text{Delay} = \frac{T_{s1} - T_{m1} + T_{m2} - T_{s2}}{2} \quad (2)
\]

When the clock offset value between master clock and slave clock is obtained, the time or frequency can be further adjusted by servo control system, and finally the adjusted slave clock and master clock are nearly synchronized.

3. Improved clock synchronization method.

Aiming at the problem that IEEE 1588 only compensates the clock deviation of master-slave clock, this paper establishes the state equation and measurement equation of clock deviation and frequency deviation, and uses Kalman filtering method to recursively correct the clock deviation, so as to reduce the deviation statistics and improve the synchronization accuracy. Kalman filtering algorithm is suitable for the situation that process noise and measurement noise are white noise. Therefore, Allan variance is used to test the noise characteristics according to the experimental data.

Kalman filtering algorithm was proposed by Kalman in 1960, and its discrete filtering and prediction process is shown in Fig.2.

3.1 State transition equation model of crystal oscillator clock

Rewrite the ground cabinet expression of the crystal oscillator clock mathematical model in the second-order state into the following form:

\[
\theta(k + 1) = \theta(k) + \gamma(k) r_\xi + \omega_\gamma(k) \quad (3)
\]

\[
\gamma(k + 1) = p \cdot \gamma(k) + \omega_\gamma(k) \quad (4)
\]

where \( K \) represents the \( k \)-th update of the oscillator clock, which \( \theta(k) \) is actually to correspond to the continuous update of the offset, that is, to correspond to the clock offset rate. When the physical clock is continuously updated from the \( k \)-th time to the \( K+1 \)st time, the time interval of the clock \( r_\xi \) is updated to the corresponding number of times. It can be seen from the above formula that in an asymmetric sensor network environment, the time value of the clock, that is, the state of the crystal oscillator clock, can be described by the clock skew and offset. In other words, the parameter variables in the state model of the crystal oscillator clock can be regarded as the clock offset or offset rate.
Equations (3) and (4) can be changed into vector form to express the clock of the oscillator. Therefore, the basic state transition equation in the process of clock change can be obtained, which is described by the above vector equation.

3.2 Observation equation model of PTP time synchronization protocol

The true value of clock offset at the nth time synchronization is:

$$\theta(n) = \frac{[t_s(n) - t_r(n)] - [t_s(n) - t_f(n)]}{2} + \frac{d_m(n) - d_m(n-1)}{2}$$  \hspace{1cm} (5)

In the asymmetric wireless network environment, there are serious differences between the actual wireless network and the theory, so the propagation delay obtained according to PTP is different from that in reality. The clock calculation value of PTP is only an observation value of the clock offset in the real environment, not a synchronization value. In order to more conveniently describe the difference between the calculated value of the clock offset and the real value $0$, the calculated value of PTP can be measured in the research and regarded as an observation value of clock synchronization.

Therefore, in the nth update of time synchronization, the calculated value of clock offset is as follows:

$$\theta(n) = \frac{[t_s(n) - t_r(n)] - [t_s(n) - t_f(n)]}{2}$$  \hspace{1cm} (6)

Comparing the above two formulas, it is not difficult to find that $\theta$ is equal to 0 only when $d_m$ is equal to $d_m$. Because a variety of factors affect the clock synchronization, these factors mainly include the asymmetric delay of the clock, the processing factors to obtain the clock delay parameters and so on. Then the real value of time offset $0$ and the estimated value of clock offset are different in the real environment. There is a difference between them.

$$\Delta d(n) = \frac{d_m(n) - d_m(n-1)}{2}$$  \hspace{1cm} (7)

Therefore, from the essence of clock synchronization, the calculated value of clock offset actually has an observation error of $\theta(n)$, which is an observation error corresponding to the deviation of the real value.

3) Optimal modeling of time synchronization based on Kalman filter

Vector $\mu(n) = [\mu_s(n) \mu_f(n)]^T$ is introduced to correct the clock. The clock correction process can be described by mathematical formula as follows:

$$\begin{cases}
\theta(n) = \theta(n-1) - \mu_s(n-1) \\
\gamma(n) = \gamma(n-1) - \mu_f(n-1)
\end{cases}$$ \hspace{1cm} (8)

Therefore, the new clock state transition equation with clock correction output is:

$$x(n) = Ax(n-1) + B\mu(n-1) + \omega(n)$$ \hspace{1cm} (9)

Therefore, the Kalman filter iterative algorithm is described as:

$$\hat{x}(n|n-1) = A\hat{x}(n-1|n-1) + B\mu(n-1)$$ \hspace{1cm} (10)

4. Analysis of clock synchronization test results

Through the back-to-back test, the synchronization accuracy is analyzed, and the advantages of IEEE 1588 protocol clock synchronization method after the improved algorithm are verified.

The clock synchronization test process starts to record data 2 minutes after the system is powered on. At this time, the clock synchronization system enters a basically stable state, and its waveform data has reference value. The clock synchronization error is updated once every second, and the waveform data of 2 h is selected for recording time. The clock deviation recorder is used to record the synchronization deviation waveform and generate the deviation curve and deviation distribution histogram.

The waveform data of back-to-back test of the improved algorithm is shown in Fig.3 and Fig.4. The clock deviation at any time is about 79 ns. The deviation curve is shown in Fig.3, and the
deviation distribution histogram is shown in Fig. 4. From the deviation distribution histogram, it can be seen that the main deviation distribution is in the range of (-20 ns, 20 ns).

Fig. 3. Deviation curve  Fig. 4. Deviation distribution

5. Conclusion.
Aiming at the problem that IEEE 1588 protocol's equal delay assumption is easy to cause large synchronization error in complex network environment, this paper analyzes the factors that affect the synchronization accuracy, establishes the second-order Kalman state estimation model of relative frequency deviation and frequency drift, and estimates the noise characteristics of the state estimator by using Allan variance. The hardware design of the clock synchronization module is implemented. The synchronization precision of the improved synchronization protocol meets the requirements of high precision clock synchronization.

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