Hardware Architecture for Inplace Compute of Burrows-Wheeler Transform in a Single Iteration

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Abstract—The Burrows-Wheeler transform (BWT) is used by the bzip2 family of compressors. In this paper, we present a hardware architecture that implements an inplace algorithm to compute the BWT. Our design does not have explicit storage for the suffix array, or output array. The performance of our implementation is fixed, and does not depend on the input string content. We use a register based character buffer in a scanchain configuration, such that the BWT is computed from right to left, as characters are loaded. Loading new characters is done every six cycles, producing a new output character from the previously computed block at the same rate. Our FGPA implementation does not use block ram instances, and achieves throughput of 66, 35, 18, and 15 MB/s for block sizes of 128 B, 1 kB, 4 kB, and 8 kB. We also report results for an ASIC implementation in 65 nm technology, which can also be adjacent to similar strings in \( S \). Therefore, if the context of a character is a good predictor for the character, \( L \) is likely to exhibit repeated characters, forming a string that is easier to compress.

Interest in hardware implementations of the BWT has risen in the recent years [8], [9], [12]. Most techniques that implement BWT in hardware explore the fact that characters in \( L \) are prefix to the first character of the corresponding rotated string. Therefore, finding the first column \( F \), of the sorted suffix array (shifted strings) leads to the transformed output. If there are no repeated characters in \( S \), the string \( F \) is a sorted version of \( S \). In the case of repeated characters in \( S \), multiple sorting iterations are required where repeated characters are replaced by their suffix. While this approach reduces memory requirements, it makes performance dependent on the input data, since the occurrence of repeated characters will trigger additional sorting iterations.

In [4], authors introduced an algorithm to compute the BWT without explicit storage for the suffix array, or output array. The algorithm is shown in Listing 1. It relies on combinatorial properties of the BWT, and runs in \( O(n^2) \) using \( O(1) \) extra memory cells, apart from the memory required to store the \( N \) characters of the input string. In this paper, we present a hardware architecture that implements such an algorithm in a single iteration, within a fixed number of clock cycles. The performance of our architecture is constant, and does not depend on the input string content. FPGA implementation results shown that our design achieves throughput of 66, 35, 18, and 15 MB/s for block sizes of 128 B, 1 kB, 4 kB, and 8 kB. The source code is publicly available in [11].

This paper is organized as follows. In the next section, we discuss relevant works in the literature, highlighting their strengths and key differences from our work. Software implementations of the BWT are discussed next, with performance numbers on the bzip2 implementation, and the inplace BWT algorithm in [4]. A description of the hardware architecture for inplace compute of BWT is detailed next. The experimental results section reports area and performance numbers obtained from our architecture. This section also offers a comparison with prior works. Finally, this work ends with a conclusion, which also highlights possible points of improvements of the proposed hardware implementation.

I. INTRODUCTION

The Burrows-Wheeler transform (BWT) was introduced in [2], and it is used by the bzip2 family of compressors [10]. The BWT processes a block of text as a single unit, producing a new block of text that contains the same characters, but is easier to compress. The transform tends to group same characters together in the output, generating data that is easy to compress with locally-adaptive algorithms. First, the BWT algorithm performs \( N \) rotations (cyclic-shifts) of the input string \( S \) with length \( N \). The rotated strings are then sorted lexicographically, and the transformed output \( L \) is formed from the last character of each rotated string after sorting, as shown in Table I. Since the first and last characters of each rotated string are adjacent in the string \( S \), consecutive characters in \( L \) will also be adjacent to similar strings in \( S \). Therefore, if the context of a character is a good predictor for the character, \( L \) is likely to exhibit repeated characters, forming a string that is easier to compress.

Interest in hardware implementations of the BWT has risen in the recent years [8], [9], [12]. Most techniques that implement BWT in hardware explore the fact that characters in \( L \) are prefix to the first character of the corresponding rotated string. Therefore, finding the first column \( F \), of the sorted suffix array (shifted strings) leads to the transformed output. If there are no repeated characters in \( S \), the string \( F \) is a sorted version of \( S \). In the case of repeated characters in \( S \), multiple sorting iterations are required where repeated characters are replaced by their suffix. While this approach reduces memory requirements, it makes performance dependent on the input data, since the occurrence of repeated characters will trigger additional sorting iterations.

The algorithm is shown in Listing 1. It relies on combinatorial properties of the BWT, and runs in \( O(n^2) \) using \( O(1) \) extra memory cells, apart from the memory required to store the \( N \) characters of the input string. In this paper, we present a hardware architecture that implements such an algorithm in a single iteration, within a fixed number of clock cycles. The performance of our architecture is constant, and does not depend on the input string content. FPGA implementation results shown that our design achieves throughput of 66, 35, 18, and 15 MB/s for block sizes of 128 B, 1 kB, 4 kB, and 8 kB. The source code is publicly available in [11].

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II. RELATED WORKS

The first attempt to implement BWT in hardware was done in [7], where the input string is right shifted and compared at each step. The sorted string is obtained by left shifting the stored data. This method is known as Weavesorter, and it requires software replacement of repeated values in the
### TABLE II

| Block size | 100 kB | 200 kB | 300 kB | 400 kB | 500 kB | 600 kB | 700 kB | 800 kB | 900 kB |
|------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| Bits per char | 2.31 bits | 2.18 bits | 2.11 bits | 2.07 bits | 2.05 bits | 2.02 bits | 2.01 bits | 1.98 bits | 1.98 bits |
| BWT Percent. | 60.1% | 64.1% | 62.2% | 70.0% | 66.2% | 67.4% | 73.4% | 70.0% | 69.7% |
| Throughput | 12 MB/s | 12 MB/s | 14 MB/s | 12 MB/s | 11 MB/s | 12 MB/s | 11 MB/s | 12 MB/s | 12 MB/s |
| Alloc. memory | 0.78 MB | 1.56 MB | 2.34 MB | 3.12 MB | 3.90 MB | 4.68 MB | 5.47 MB | 6.25 MB | 7.03 MB |

Notes: Average values from corpus E.coli.txt, bible.txt, book1.txt, book2.txt, and world192.txt. Allocated memory is 8x the block size, and it is used for both BWT and compression.

### TABLE III

| Block size | book1.txt Hector |
|------------|------------------|
| 1 kB       | 4.34             |
| 4 kB       | 3.86             |
| 16 kB      | 3.43             |
| 64 kB      | 3.00             |
| 256 kB     | 2.68             |
| 750 kB     | 2.49             |
| 1 MB       | 2.43             |
| 4 MB       | 2.26             |
| 16 MB      | 2.13             |
| 64 MB      | 2.04             |
| 103 MB     | 2.01             |

Notes: book1.txt from Calgary compression corpus, and the Hector corpus [5]. Compression uses move-to-front algorithm and a modified Huffman coding [2].

### III. BURROWS-WHEELER TRANSFORM

The Burrows-Wheeler transform (BWT) reorganizes the characters in a text block such that the transformed text tend to have same characters grouped together, which enables more efficient data compression [2].

#### A. Software Implementation

A naive software implementation of the BWT algorithm takes $O(N^2 \log N)$ time and requires $O(N^2)$ space. We profiled the reference implementation of bzip2, available in [10], with various corpus and different block sizes. Results are listed in Table II, including values for compression ratio (bits per character), percentage of time spent in BWT over the total execution time, BWT routine throughput, and allocated memory for the entire operation. Compression results for smaller text block sizes are listed in Table III, which was extracted from the original BWT publication [2].

The variation in compression rate reported in Table II in the 100 kB to 900 kB block size range is 14%. Alternatively, Table III shows less effective compression rates, most likely due to different compression algorithms used. The average improvement in compression rate for the 1 kB to 4 kB range is 11%. Another 11% improvement in compression rate is obtained when block size is increased from 4 kB to 16 kB.

The importance of BWT performance is also noticeable from results in Table II. The BWT routine takes more than 60% of bzip2 execution time for all text block sizes. The

```c
void inplaceBWT( unsigned char S[], int n ){
    int i, p, r, s;
    unsigned char c;
    for ( s = n-3; s >= 0; s-- ){
        c = S[ s ];
        /* steps 1 and 2 */
        r = s;
        for ( i = s+1; S[ i ] != END_MARKER; i++ )
            if ( S[ i ] <= c ) r++;
        p = i;
        while ( i < n )
            if ( S[ i++ ] < c ) r++;
        /* step 3 */
        S[ p ] = c;
        /* step 4 */
        for ( i = s; i < r; i++ )
            S[ i ] = S[ i+1 ];
        S[ r ] = END_MARKER;
    }
}
```

Listing 1. Inplace algorithm to compute BWT, introduced in [4].
TABLE IV
PERFORMANCE RESULTS FOR SOFTWARE IMPLEMENTATION OF INPLACE ALGORITHM TO COMPUTE BWT [4].

| Block size | 1 kB | 2 kB | 4 kB | 8 kB | 16 kB | 32 kB | 64 kB | 128 kB | 256 kB |
|------------|------|------|------|------|-------|-------|-------|--------|--------|
| Number of blocks | 3953 | 1977 | 989  | 495  | 248   | 124   | 62    | 31     | 16     |
| Compression time   | 1.4 s | 2.5 s | 4.9 s | 9.6 s | 19 s  | 38 s  | 76 s  | 152 s  | 300 s  |
| Throughput         | 2.8 MB/s | 1.5 MB/s | 0.78 MB/s | 0.40 MB/s | 0.20 MB/s | 0.10 MB/s | 0.05 MB/s | 0.02 MB/s | 0.01 MB/s |

Notes: corpus bible.txt, with 4047392 bytes.

measured throughput is nearly constant at 12 MB/s, while the allocated memory for the whole operations was 8x the block size used.

B. Inplace Algorithm with Single Iteration

The algorithm in Listing 1 was introduced in [4] to compute the BWT without explicit storage for the suffix array, or the output array. It computes the BWT from right to left, in $O(N^2)$ steps, using $O(1)$ extra memory cells, apart from the cells storing the input text block. Table III shows performance information of our CPU implementation. Throughput quickly degrades for large block sizes, following the expected quadratic time complexity. In the next sections, we show that careful implementation of the algorithm in hardware leads to a substantial increase in throughput.

IV. HARDWARE IMPLEMENTATION

Our hardware architecture for inplace compute of BWT is shown in Fig. 1. The transformed output is computed in a fixed number of steps, independent of the input string content. Every 6 cycles a new character is loaded, and another character from the previous block is made available at the output. The character buffer is implemented with registers in a scanchain configuration, such that it fits a complete text block. The algorithm proceeds from right to left, performing the BWT of a gradually increasing text block size, until the transform of the entire block is computed. The comparison signals necessary for sorting characters are generated in parallel for all characters in the buffer. An encoder finds the end marker position in the character buffer, which is then used to define the ranges to compute $\varepsilon$ (steps 1 and 2 in the algorithm).

Every iteration of the outer loop in Listing 1 takes 6 cycles, as shown in Fig. 2. Cycle 1 simply loads the new character and shifts the scanchain; as a side effect, a new output character from the previously computed block is produced. Cycle 2 uses the equality comparators to find the end marker position, which is used in cycle 3 to perform a population count over the ($\leq$) comparison results. Similarly to cycle 3, cycle 4 also performs a population count, but on the ($<$) comparison results. Cycles 5 and 6 perform repositioning of the newly added character and the end marker in the buffer.

Timing analysis revealed that the population count in cycles 3 and 4 has substantial impact on the maximum frequency. Therefore, we split the addition over two cycles by computing the result in two partial sums that are added together in the coming cycle. This change increased the maximum frequency up to 48%, depending on block size.

V. EXPERIMENTAL RESULTS

Our hardware implementation is publicly available in [11]. This section presents area and performance results for FPGA and 65 nm CMOS targets.

A. FPGA Implementation

Our FPGA implementation was synthesized using Synopsys Synplify tool. Our target device was an FPGA with part
**TABLE V**

**Experimental results and comparison with other Burrows-Wheeler hardware architectures.**

|                      | This work | FCCM’19 [9] | ICFPT’17 [12] | IPDPSW’16 [8] | ReConFig’13 [3] |
|----------------------|-----------|-------------|---------------|---------------|-----------------|
| **Device**           | XCVU9P*   | XCVU9P*     | XCVU9P*       | XCVU9P*       | XCVU9P*         |
| **Technology**       | 20 nm     | 20 nm       | 20 nm         | 20 nm         | 20 nm           |
| **Block size**       | 128       | 1 kB        | 4 kB          | 8 kB          | 18 MB/s         |
| **BRAMs**            | 0%        | 0%          | 0%            | 0%            | 8 kB            |
| **Registers**        | 1.1 k (0.05%) | 8.7 k (0.36%) | 34 k (1.4%)  | 67 k (2.8%)  | 64 kB           |
| **Max Freq.**        | 345 MHz   | 186 MHz     | 95 MHz        | 69 MHz        | 371 MB/s        |
| **Throughput**       | 66 MB/s   | 35 MB/s     | 18 MB/s       | 15 MB/s       | 62 MB/s         |
| **Has Parallel.**    | No        | No          | No            | No            | 0%              |
| **# of Cycles**      | 768       | 6144        | 24576         | 49152         | 2048            |
| **Iterations**       | Single    | Single      | Single        | Single        | Input Dep.      |
| **Open-source**      | Yes       | Yes         | Yes           | Yes           | Input Dep.      |

Notes: (*) Complete part number XCVU9P-L2FSGD2104E. (†) Complete part number EP1S10B672C6. (‡) Imposes restrictions to input string content. (††) Multiple blocks are computed in parallel.

Fig. 3. ASIC implementation of inplace BWT accelerator in 65 nm CMOS.

number XCVU9P-L2FSGD2104E. Placement and routing was done using standard Xilinx tools. Results for various block sizes are reported in Table V, including a comparison with other recent works.

As shown in Table V, our architecture uses no block rams (BRAMs). Our storage requirements are simply the registers necessary to store the input text block. This is only matched by the work in [8], however, our design not only reaches almost twice the throughput, but does so in a single iteration. Moreover, compared to [8], we support much larger text block sizes. The best results in terms of throughput were reported by [12], however, it is important to notice that authors used several instances to compute multiple blocks simultaneously, which is equally applicable to our design.

**B. ASIC Implementation**

Our ASIC implementation uses a 128 B block size and targets a 65 nm CMOS process. The synthesis and physical implementation were done using the Genus and Innovus. The accelerator layout is shown in Fig. 3. It uses a square layout with 380 \( \mu m \) side length, while the actual design area uses 19260 instances and 92680 \( \mu m^2 \). The maximum frequency 843 MHz, which is capable of 161 MB/s.

**VI. CONCLUSION**

We presented a hardware implementation for inplace compute of the BWT. Our design does not have explicit storage for the suffix array, or output array. We do not use any block ram memory. The performance is fixed, and does not depend on the input string content. Our area and performance results are very competitive for small block sizes like 128 B, and 1 kB. Future work could potentially increase throughput by computing multiple blocks in parallel. Moreover, improvements to the performance for large block sizes are likely possible by redesigning the comparators to generate results over multiple cycles.

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