**Nanospike electrodes and charge nanoribbons: A new design for nanoscale thin-film transistors**

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To scale down thin-film transistor (TFT) channel lengths for accessing higher levels of speed and performance, a redesign of the basic device structure is necessary. With nanospike-shaped electrodes, field-emission effects can be used to assist charge injection from the electrodes in sub-200-nm channel length amorphous oxide and organic TFTs. These designs result in the formation of charge nanoribbons at low gate biases that greatly improve sub-threshold and turn-off characteristics. A design paradigm in which the gate electric field can be less than the source-drain field is proposed and demonstrated. By combining small channel lengths and thick gate dielectrics, this approach is also shown to be a promising solution for boosting TFT performance through charge focusing and charge nanoribbon formation in flexible/printed electronics applications.

**INTRODUCTION**

In more demanding applications of thin-film transistors (TFTs), such as in back-end-of-line (BEOL) applications, scaling down the channel length \((L, 2)\) is problematic because of increasing contact resistance and short-channel effects \((3–5)\). When contact resistance is high, it can dominate TFT performance at short channel lengths. Contact resistance and short-channel effects can both be seen in amorphous oxide semiconductors, organic/polymer semiconductors, and two-dimensional (2D) semiconductors such as MoS\(_2\) \((6–8)\), and various approaches have been tried to overcome these problems \((8, 9)\).

The new device design proposed and demonstrated in this letter addresses both contact resistance and short-channel effect problems in multiple classes of semiconductors with channel lengths below 200 nm. Charge injection is facilitated because of a combination of field-emission and enhanced charge carrier density near the source electrode. Simultaneously, subthreshold swings are much steeper, and off currents are kept low at short channel lengths. A new mode of TFT operation is described in which the spatial distribution of charges in the channel changes, such that charges are expected to form one or more narrow channels in subthreshold and near turn-off conditions (we designate these narrow regions of charge as “charge nanoribbons”). A TFT design for printed electronics is also proposed in which the maximum gate electric field is less than the maximum source-drain field. In these TFTs, charge nanoribbons persist well above threshold and can continue to enhance TFT performance. Data from indium gallium zinc oxide (IGZO) TFTs and the organic semiconductor (pentacene) TFTs are used to demonstrate the effects, showing that they are not confined to a single material system and can benefit many materials systems.

**RESULTS**

The basic device design of a nanospike TFT with IGZO is shown in Fig. 1, where both the source and drain electrodes are nanospike-shaped. These electrodes are analogous to field-emission tips used in vacuum electronics and in conducting scanning probe microscopes, both of which take advantage of shaping metal tips to sharp points to achieve local field enhancement for facile emission of electrons into the vacuum energy level \((10)\). In TFTs, nanospike-shaped tips similarly focus high electric fields at the source and/or drain contact tips, lowering the Schottky barriers for carrier injection from the metal to the semiconductor. For comparison, conventional flat edge electrodes (or flat TFTs) are also fabricated alongside with the same channel length. For accurate channel current measurements and to avoid collecting spreading currents, separate side guard electrodes are used, and they are biased to the same potential as the drain.

Figure 1 (E and F) shows the measured characteristics of a 50-nm channel length single-nanospike IGZO TFT. The characteristics show excellent drain current modulation with gate voltage despite the physical gate dielectric thickness being almost twice the channel length. At low gate voltages in the subthreshold region, drain currents do not change notably with increasing drain voltage. This is different from what is typically observed in short-channel TFTs. When the source-drain field exceeds the gate field, there is greater field focusing of the electrons onto a narrower channel. The output characteristics in Fig. 1F show linear and saturation behavior in the expected voltage regions. The gate leakage current, which flows from the drain contact through the insulator, was subtracted from these characteristics to arrive at more accurate drain currents. The procedure used and original raw data are shown in the Supplementary Materials.

To increase drive current in a spike electrode TFT, a line array of nanospikes can be used. Three different spacings between individual nanospikes were studied. Output characteristics are shown in Fig. 2A for TFTs with spike width to spike spacing ratios of 1:0 (in which the spikes are all coalesced), 1:1, and 1:3. The currents approximately scale with the overall device width. This is because the wider spacings between spikes correspond to a greater gate area and hence a greater number of channel electrons. Electrostatic electric field simulations in Fig. 2C were performed with COMSOL. The magnitude of the enhancement of the electric field at the tips and the distribution of the field within the device channel are shown. As the spacing between individual nanospikes increases, so does the enhancement of the electric field at the nanospike tips and on the carriers within the channel. Given a tip radius of 20 nm for all devices, the maximum electric field of a 1:3 electrode is \(2.58 \times 10^6\) V/cm, of...
1:1 electrode is $2.53 \times 10^6$ V/cm, and of a 1:0 electrode is $2.45 \times 10^6$ V/cm. Increasing spike spacing also initiates the formation of individual charge conduction paths. The transfer characteristics in Fig. 2B also show greatly improved subthreshold characteristics with increased spacing between the nanospikes. This is again due to efficient charge focusing into nanoribbons in subthreshold conditions. At low gate voltages, when the source-drain electric field is greater in magnitude than the gate field, gate control can be considered quasi-3D. In several respects, the enhancement in gate control by the nanospike electrode TFTs makes them the planar analog to silicon fin field effect transistor (FinFET).

Figure 3 depicts the contrast between subthreshold operation of multispike TFTs and flat-electrode TFTs with the same channel length (100 nm) and width (1.8 μm). Subthreshold swings are much better for the nanospike TFTs compared to flat TFTs, and the off current is much lower for the nanospike TFTs. Threshold conditions are reached at smaller gate voltages, and the difference in drain current with respect to flat-electrode TFTs near threshold is substantial, as shown in Fig. 3C. The nanospike TFT has better injection through field-emission effects and increased volume carrier density at the source electrode because of charge nanoribbon formation, despite having a much smaller injection perimeter. The total number of charges induced by the gate is approximately the same for the nanospike TFT and the flat TFT (because the channel width, channel length, and gate area are the same). In the nanospike TFT, the high source-drain electric field in the IGZO relative to the gate field causes charge nanoribbons to persist even in the on-state. Thus, the total channel charge is confined in a smaller surface area in the nanospike TFT compared to the flat TFT. The Fermi level is raised in the nanospike TFT resulting in increased volume carrier densities and lower contact resistance per unit channel width at the source. In IGZO and many other disordered semiconductors, multiple trap and release has been shown to be a dominant charge transport mechanism (6), and a higher carrier density generally translates to a higher mobility and carrier velocity. In Fig. 3D, it can be noticed that the currents are nearly identical in TFTs with multiple channel lengths, suggesting that the carrier velocity is saturated. Saturation velocities, estimated from measured drain currents and the device geometry, are more than $1.5 \times 10^6$ cm/s and are reduced in value from the theoretical saturation velocity of crystalline IGZO, which is $>8 \times 10^6$ cm/s. Such reduction in velocity from ideal values is due to trapping and has been described in detail in a theoretical study that was recently reported (6).

To reduce the gate leakage current further, a wet etch was performed to isolate individual IGZO TFT devices. Figure 4 shows the transfer and output characteristic of an isolated 100-nm channel five-spike electrode TFT with a 5:1 spacing. With the isolation of individual devices, the gate leakage current is greatly reduced by more than a factor of $10^5$. These devices are measured in air, and the data presented are raw data with no leakage current processing.
Moving beyond IGZO to a very different material system, data from pentacene TFTs with a channel length of ~20 nm are shown in Fig. 5. Similar TFTs were previously reported by our group in the context of short-channel organic TFTs and chemical sensors (11). However, many unique aspects of the characteristics of these TFTs were never mentioned in previous work. The maximum gate-source and gate-drain electric fields are lower than the maximum source-drain fields. The gate insulator is 100 nm thick, which is more than five times the channel length. This is contrary to the design principle of all TFTs and even silicon field-effect transistors, in which the gate insulator is always designed to be much thinner than the channel length value.

Data in Figs. 2 and 3 show that thick gate dielectrics relative to the channel length value can also result in good TFT characteristics, provided that charge focusing is used, and the source electrode is shaped like nanospikes or nanospike arrays. Such an electrode design results in quasi-3D gate control of the channel, which is highly beneficial for the turn-off and subthreshold performance (12). Drain-induced barrier lowering (DIBL)–like effects, almost always present in short-channel TFTs, are greatly mitigated or eliminated in nanospike TFTs. Charge nanoribbon formation will, in turn, help charge injection by raising the Fermi level in the semiconductor. This effect is independent of the benefits to charge injection because of field-emission effects described above. In other words, these two separate effects combine to help reduce contact resistance per unit in these TFTs, while improving subthreshold and retaining good turn-off characteristics.

**DISCUSSION**

Nanospike electrodes can be very useful in realizing high-performance TFTs with thick gate insulators deposited by printing and other fabrication methods compatible with flexible electronics. When combined with the high-resolution, high-throughput nanoimprint lithography for defining the source-drain nanospikes, it is possible to achieve good characteristics both above and below threshold. Channel lengths on the order of a few hundreds of nanometers defined by nanoimprint lithography have been reported in TFTs (13). Using thicker gate dielectrics will avoid pinhole problems and
improve reliability of the gate dielectric and device. Charge focusing into nanoribbon arrays will enhance local carrier densities and will help achieve higher mobilities and velocities for a given operating voltage, notwithstanding the thicker gate insulator. The design of such a TFT is shown schematically in Fig. 5C. Compared to flat-electrode TFTs, the proposed design will result in better contacts and better device characteristics. The design will also improve speed by reducing overlap capacitance by increasing dielectric thickness while retaining the drive current and operating voltage. The overlap area and hence the capacitance are also reduced because of the spike geometry of the source and drain with gaps between spikes compared to continuous flat electrodes.

The TFT structures proposed in this work have some additional advantages and possible future uses. Some of these possibilities are mentioned below. It is possible to reduce the DIBL-like variation of subthreshold drain current with drain voltage. This has been hitherto difficult to achieve in short-channel TFTs. The slope of the subthreshold region can be controlled by changing the spike width to spacing ratio. With a smaller spacing, or wider spikes, the TFTs will have subthreshold behavior more similar to those of conventional TFTs with the same channel length. A very small DIBL-like effect means that the current gain in subthreshold can be quite high, leading to subthreshold circuits with high current gain and very low power dissipation. Further electric field tailoring of the charge distribution in the channel (for example, by using two asymmetric gates) can lead to possible high-density quasi-1D–gated conductors.

The frequency response implications of this new TFT geometry need to be explored. The reduced overlap capacitance (between gate drain and gate source) will likely improve speed while also providing greater tolerance to mismatches and alignment errors in fabrication. The reduced threshold will enable lower-voltage (and lower-power) operation. The combination of small channel lengths and relatively thick gate insulators (without short-channel effects) will help the field of flexible/printable electronics in which thicker gate dielectrics are more common.

**MATERIALS AND METHODS**

**IGZO thin-film fabrication and measurement**

The IGZO TFTs were fabricated as bottom-gate, top-contact transistors. The substrate used is a silicon wafer with 90 nm of thermally grown SiO₂, where the highly doped silicon wafer acted as a global bottom gate and the SiO₂ as the gate dielectric. IGZO (20 nm) was then sputtered on the sample using a 1:1:1 target for In:Ga:Zn, respectively, and at a radio frequency power of 150 W, at a pressure of 5 mTorr, and at 7% O₂ in Ar. The IGZO film was annealed at 450°C for 1 hour in air to complete the film formation. For the TFT data shown in Fig. 4, the IGZO material was sputtered using a target with a composition of Ga₂O₃:In₂O₃:ZnO at a ratio of 1:2:2, respectively. The sputtering conditions were the same as previously stated.

All devices reported in this paper were fabricated in this manner. For the 200-nm short-channel devices, JEOL electron beam patterning was used for the metal contact patterning to prototype various source drain designs and geometries, processing details listed below. For long-channel devices, all layers up to and including IGZO were the same as the short-channel devices. To deposit the contact metals, 500 nm of Al was deposited through a shadow mask. Device dimensions of the long-channel devices include channel lengths ranging from 50 to 150 μm with all W/L = 20. The sputtered IGZO material is very uniform and consistent with previous reports of low variation of film quality (14). Both long- and short-channel devices were tested and analyzed under vacuum, unless otherwise noted, in a probe station at pressures <1 × 10⁻⁷ torr and at room temperature.

**E-beam lithography of nanospike contacts**

The nanospike pattern was fabricated using a JEOL 6000 FSE Electron Beam (e-beam) lithography tool. A solution of ZEP-520A:Anisole::1:2 was used as the e-beam resist. The resist was deposited onto the prepared IGZO samples with a plastic syringe through a 0.2-μm Polytetrafluoroethylene (PTFE) filter and spin-coated for 2000 rpm for 60 s and annealed at 180°C for 2 min. The resulting film is ~140 nm thick, as measured using an Ellipsometer J.A. Woollam M-2000 DI.

The writing of the pattern was done at 50 keV with an exposure current of 100 pA using exposure mode 7, the fine feature aperture, and fifth lens of the JEOL 6000 system. Development was done using a bath of amyl acetate for 15 s followed by a rinse in deionized (DI) water.

The resulting patterned resist was used as a mask to create metal contacts through a metal deposition and lift-off process. Aluminum (30 nm) and 30 nm of silver were deposited onto the resist using a Kurt J. Lesker Thermal Evaporator tool. Aluminum was used as the contact layer, while silver is primarily used to help with scanning.

**Fig. 5. Pentacene nanospike TFTs.** (A) SEM image of the ~20-nm channel length pentacene TFT with side guard electrodes. WD, working distance. (B) Output characteristics at lower VDS for VGS as large as -30 V. Output characteristics show minimum contact effects at low VDS. (C) Schematic demonstrating the formation of charge nanoribbons in the channel that focuses a larger area of gate electric field to a smaller channel area, allowing for better gate control and enhanced carrier concentrations in channel.
electron microscopy (SEM) imaging of the metal features. Liftoff was conducted by soaking the sample in a 4-hour bath of Remover PG at 80°C followed by 2 s of ultrasonication and then a rinse using DI water.

**TFT isolation method and measurement**

To isolate individual devices, the IGZO film was etched into islands where the etch pattern is conformal to the devices. The etch areas were patterned using Raith eLine e-beam lithography tool. The e-beam resist consisted of 4 weight % poly(methyl methacrylate) (PMMA) in anisole and was spun onto the IGZO samples at 3000 rpm for 60 s. The substrate was then annealed at 180°C for 2 min. The writing of the pattern was done with 20-kV electron high tension (EHT) and a 120-μm aperture. The sample was developed with a solution consisting of 10 ml of methyl isobutyl ketone and 15 ml of isopropanol alcohol (IPA) for 10 s followed by a rinse in IPA. The patterned devices were then wet-etched in an HCl solution diluted in water (1:6, respectively), followed by a water rinse. After the etch, the remaining PMMA was lifted off in acetone. The measurement of these isolated TFTs were taken in air at atmosphere and at room temperature.

**SUPPLEMENTARY MATERIALS**

Supplemental material for this article is available at https://science.org/doi/10.1126/sciadv.abm1154.

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