Graphene-Silicon Schottky diodes for photodetection*
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Abstract— We present the optoelectronic characterization of two graphene/silicon Schottky junctions, fabricated by transferring CVD-graphene on flat and nanotip-patterned n-Si substrates, respectively. We demonstrate record photo responsivity, exceeding 2.5 A/W under white light, which we attribute to the contribution of charges photogenerated in the surrounding region of the flat junction or to the internal gain by impact ionization caused by the enhanced field on the nanotips.

I. INTRODUCTION

The graphene/silicon (Gr/Si) junction has been the subject of an intense research activity both for the easy fabrication and for the variety of phenomena that it allows to study. It offers the opportunity to investigate new fundamental physics at the interface between a 2D semimetal and a 3D semiconductor, and holds promises for a new generation of graphene-based devices such as photodetectors, solar cells and chemical-biological sensors [1].

II. FEATURES OF THE GR/SI JUNCTION

A Gr/Si junction with defect-free interface exhibits rectifying current-voltage (I-V) characteristics, which are the result of the formation of a Schottky barrier, as in traditional metal-semiconductor (M/S) Schottky diodes. Moreover, a Gr/Si junction presents features that are absent in M/S diodes. The vanishing density of states at the graphene Dirac point enables Fermi level tuning and hence Schottky barrier height modulation by a single anode-cathode bias [1,2]. Fig. 1 shows the energy bands alignment in a Gr/n-Si junction and the modulation of the Schottky barrier height, $\Phi_B$, which is decreased (increased) by the reverse (forward) bias; graphene is assumed p-type, such being the common doping of air-exposed samples [3].

When the Gr/Si junction is used as a photodiode, graphene acts not only as anti-reflecting and transparent conductive layer for charge transport to the external circuit, but it functions also as active material for light absorption and electron-hole generation and separation. Graphene absorbs about 2.3% of the incident light, independently of the wavelength, from near ultraviolet to near infrared [4]. Although most of the incident light is converted to photocharge into Si, the absorbance in graphene enables detection of photons with Si sub-bandgap energy through internal photoemission over the Schottky barrier [5]. Photocharges injected over the Schottky barrier (Fig. 2 (a)), under high reverse bias, can be accelerated by the electric field in the depletion region of the diode and cause avalanche multiplication by scattering with the Si lattice, thus enabling internal gain.

(a) Zero bias (b) Reverse bias (c) Forward bias

Figure 1. Gr/Si junction energy bands alignment at (a) zero, (b) reverse and (c) forward bias. Due to the low density of states of graphene, the Schottky barrier height, $\Phi_B$, is modulated by the applied bias. $\Phi_B$ and $V$ are the built-in potential and the external bias of the junction; $E_F$ and $E_g$ are the Fermi energies of graphene and Si, while $E_c$ and $E_v$ are the lowest and highest levels of the Si conduction and valence band, respectively.

Successful application of the Gr/Si junction for photodetection at Si sub-bandgap energies, for instance at 1550 nm which is of interests for optical communication, has been reported, with responsivity up to 0.37 A/W in reverse bias [6].

The Gr/Si junction forms the ultimate ultra-shallow junction, which is ideal to detect light absorbed very close to the Si surface, such as near- and mid-ultraviolet, which generates charges in a less than 20 nm deep layer. The location of the Gr/Si junction reduces the diffusion path and prevents the severe surface recombination that occurs in traditional pn junctions. Indeed, detection with high responsivity of 1.14 A/W has been demonstrated for the wavelength range from 200 to 400 nm [7].

(a) Photodetection in a Gr/Si junction. Photons with energy lower than the Si bandgap, $E_g = E_c - E_v$, but higher than the Schottky barrier $\Phi_B$ ($\Phi_B < h \nu < E_g$) can be absorbed in graphene. Emitted over the Schottky barrier, such electrons can originate avalanche multiplication through impact ionization. (b) Graphene on flat Si substrate (“flat Gr/Si” junction) and (c) graphene on patterned Si (“Gr/Si-tips” junction).

In this paper, we report the electrical characterization and the photoresponse of two types of Gr/Si devices, shown in Figs

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by transferring CVD-graphene on flat and nanotip-patterned n-Si substrates, respectively. We demonstrate record photo responsivity, exceeding 2.5 A/W under white light, which we attribute to the contribution of charges photogenerated in the surrounding region of the flat junction or to the internal gain by impact ionization caused by the enhanced field on the nanotips.
2 (b) and 2 (c), which are fabricated on flat and nanotips terminated Si surfaces. In the following, we will refer to them as the “flat Gr/Si” [8,9] and the “Gr/Si-tips” [10] device, respectively.

III. DEVICE FABRICATION AND MEASUREMENTS

The fabrication involves the patterning of the substrate and the transfer of a monolayer CVD-graphene from Cu foils by a wet etch method [11]. For the flat Gr/Si device [8], the substrate preparation implies the opening of a 10 µm wide slit in the capping SiO₂ layer by reactive ion etching (RIE), followed by buffered HF cleaning, immediately prior to graphene transfer. The size of the transferred graphene foil is about 1 × 0.4 cm², implying that most of the graphene sheet extends over the 60 nm thick SiO₂ layer. Fig. 3 (a) shows graphene both on Si and SiO₂: the micro-Raman spectra of Fig. 3 (b) confirm high-quality monolayer graphene everywhere.

The fabrication of the Gr/Si-tips devices [10, 12] starts with RIE etching of the Si-tips followed by a two-step dielectric deposition (USG and BPSG films), the chemical mechanical polishing (CMP) process to uncover the tips up to the desired diameter, and the transfer of graphene (Fig. 3 (c) and 3 (d)).

The electrical measurements are performed by a Keithley 4200 SCs using graphene (contacted with a Ti/Au layer [13]) as the anode and the Si substrate as the cathode, in a Janis ST500 cryogenic probe station under controlled pressure (typically 50 mbar) and temperature. Photoconductance is investigated under white light from a LED array with adjustable intensity up to 5 mW/cm² and spectrum ranging from 420 to 720 nm.

IV. FLAT GR/SI JUNCTION: RESULTS AND DISCUSSION

The I-V characteristic (Fig. 4 (a)) of the flat Gr/Si junction, at room temperature, shows a rectifying behavior typical of a Schottky diode that can be fitted by the equation:

\[
I = I_0 \exp \left( \frac{q(V + R_s I)}{nkT} \right) - 1
\]

with

\[
I_0 = A A' T^2 \exp \left( -\frac{q\Phi_0}{kT} \right)
\]

where \(I_0\) is the reverse saturation current, \(n\) the ideality factor, \(A\) the area of the Gr/Si junction, \(A' = 112\ Acm^{-2}K^{-2}\) is the effective Richardson constant for n-Si, \(T\) is the temperature and \(\Phi_0\) is the Schottky barrier height at zero bias. A more realistic model (Fig. 4 (c)) includes a series resistance, \(R_s\), cumulative of all the resistive paths in the device and the measuring circuit, and a shunt resistance \(R_{sh}\), to take into account possible leakages, as those due to defect that could locally lower the Schottky barrier. Hence, eq. (1) becomes:

\[
I = \frac{R_p}{R_s + R_p} \left( I_0 \exp \left( \frac{q(V + R_s I)}{nkT} \right) - 1 \right) - \frac{V}{R_p}
\]

Eq. (3) provides an excellent fit to the forward current, but underestimates the reverse saturation current, which results about an order of magnitude higher than expected (Fig. 4 (a); the overall fit improves at lower temperatures (Figs 4 (b)).

The behavior of the junction under white LEDs illumination is shown in Fig. 4 (d): The forward characteristic remains unaffected (apart the appearance of an open circuit voltage of ~0.2 eV due to photovoltaic effect), while the reverse current dramatically increases reaching values higher than the forward current. This unexpected behavior, together with the anomalous dark leakage, indicates that other components add to the reverse current of the Gr/Si junction.
The responsivity of the device, defined as the ratio of the photocurrent \( I_{ph} \) to the incident power, results \( R = \frac{I_{ph}}{P_{opt}} = 2.5 \times 10^4 \) at -3 mW/cm². This value exceeds the performance of solid-state photodetectors on the market or of similar Gr/Si devices [14]. Furthermore, Figs 4 (e) and 4 (f) show a photocurrent proportional to the incident power and a good transient behavior of the device.

To explain the experimental findings, we propose the model illustrated in Fig. 5 (a), in which both the part covered by SiO₂ and the junction region contribute to the observed optoelectronic behavior of the flat Gr/Si device. A large area Gr/SiO₂/Si MOS (Metal-Oxide-Semiconductor) capacitor surrounds the Gr/Si junction. In reverse bias, thermally or optically generated holes (minority carriers) are attracted to the SiO₂/Si side of the MOS capacitor. By diffusion, they reach the junction region and are swept by the electric field of the reverse biased junction, thus contributing to the reverse current. We point out that the band bending on the Si surface (Fig. 5 (b)), due to the gating effect of graphene [15], favors the drift of holes from the MOS to the junction region (where, as we will demonstrate, there is an inadvertent ultrathin dielectric layer).

The model is supported by the high frequency (10 kHz) capacitance-voltage (C-V) measurements shown in Fig. 6. The C-V curve of an Ag/SiO₂/Si MOS test structure (Fig. 6 (c)) is compared with the C-V characteristic of flat Gr/Si device (Fig. 6 (d)), composed of the mentioned Gr/SiO₂/Si MOS and the Gr/Si diode (Fig. 6 (e)). As shown in Fig. 6 (a), the MOS test structure exhibits the typical accumulation region, with higher capacitance, in forward bias and the depletion region, with lower capacitance, in reverse bias. By contrast, for the Gr/Si device, the Gr/SiO₂/Si MOS component, which is dominant at positive voltage, is overcome by the capacitance of the depletion layer of the Gr/Si diode in reverse bias. This originates, for negative bias, the shoulder highlighted in the plot of Fig. 6 (a). The depletion layer capacitance of a diode, when an ultrathin interfacial oxide layer is considered, is expressed by [8,16]:

\[
\frac{1}{C^2} = \frac{2n [N_d q (\Phi_{ho} - N_c \Phi) - qV]}{\varepsilon_0 \varepsilon_r A^2 q N_d}
\]

\( \Phi_{ho} = \frac{V_m}{n} + kT \ln \frac{N_c}{N_d} + kT \approx 0.54 \text{ eV} \)

where \( n = 3.9 \) is extracted from the fit of Fig. 4 (a), \( N_d = 4.5 \times 10^{14} \text{ cm}^{-3} \) is the doping density of Si, \( \varepsilon_r = 11.7 \varepsilon_0 \) is the Si permittivity, and \( \Phi_n = kT \ln \frac{N_c}{N_d} \) with \( N_c \) the effective density of states in the conduction band (= 2.9 \times 10^{19} \text{ cm}^{-3} at T = 300K). The x-intercept, \( V_m \), of the straight-line fitting the 1/C² - V curve, shown in Fig. 6 (b), is used to evaluate the barrier height as

\[
\Phi_{ho} = \frac{V_m}{n} + kT \ln \frac{N_c}{N_d} + kT \approx 0.54 \text{ eV}
\]

a value in good agreement with the barrier height of 0.52 eV extracted with the Richardson method, based on I-V measurements shown in Fig. 7. The forward part of the I-V curves at different temperatures is used to extract the reverse current at zero bias, \( I_0(T) \), which, according to eq. (2), is plotted as \( \ln \frac{I_0}{T^2} \) vs \( \frac{1}{T} \) to extract the barrier height [19,10]. The y-intercept of the Richardson plot, which is shown in Fig. 7 (b), yields a Richardson constant of 3.9 \times 10^{-5} \text{ Acm}^{-2} \text{K}^{-2} that is several orders of magnitude lower than the theoretical value. We attribute the discrepancy to the inadvertent presence of a native oxide layer at Gr/Si interface. Such insulating layer modifies eq. (2) by a tunneling factor [8]:

\[
I_0 = A \Phi^{\chi/2} \exp(-\chi^2/2) \exp\left(-\frac{\Phi_{ho}}{kT}\right)
\]

where \( \chi = 3\text{eV} \) is the mean barrier height and \( \delta [\text{Å}] \) is the thickness of the layer.
Hence, a modified effective Richardson constant, $\Lambda^* = \Lambda^\prime \exp(-\chi^{1/2} \Phi)$, where $\Lambda^\prime$ is the measured value and $\Lambda^\prime$ the theoretical one, can be used to estimate the oxide thickness as ~8 Å. Indeed, the presence of a sub-oxide SiO$_2$ layer below graphene with thickness ~1 nm is confirmed by the X-ray photoelectron spectra (inset of Fig. 7 (b)).

V. Gr/Si-TIPS JUNCTION: RESULTS AND DISCUSSION

We fabricated the device with graphene on patterned Si to further improve the photoresponse. The nanotips patterning has three major advantages: 1. The textured substrate favors light absorption through multiple reflections; 2. The reduced area favors barrier uniformity by reducing the probability of including defects; 3. More importantly, the field amplification at the top of the tips (Fig. 8 (a)), that is at the Gr/Si junction, enhances photocharge separation and can enable internal gain by avalanche multiplication.

A remarkable feature of the Gr/Si-tips junction is the linear dependence of the Schottky barrier height on the applied voltage, extracted from the I-V characteristics at different temperatures, as shown in Fig. 8 (c) [10]. The barrier increases (decreases) in forward (reverse) bias, related to the properties of graphene as explained previously, and expressed as

$$\Phi_B(V) = \Phi_{B0} + \gamma q(V - R_s I) ,$$

(7)

where $\gamma$ is the slope of the fitting straight line.

We notice that the slightly lower value of the Schottky barrier at zero bias (0.36 eV vs 0.52 eV) with respect to the previous device can be attributed to the image force barrier lowering, which is more pronounced here, being proportional to the fourth root of substrate doping concentration ($N_d$~$10^{18}$ cm$^{-3}$ for the Gr/Si-tips device).

The bias-modulation of the barrier can be considered in the diode equation by redefining the ideality factor as [10,16]:

$$\frac{1}{m} = \frac{1}{n} \frac{\partial \Phi_B}{q \partial(V - R_s I)} = \frac{1}{n} - \gamma .$$

(8)

Including eq. (8) in eq. (1) leads to the expression:

$$I = I_0 \left[ e^{\varphi(V - R_s I)/m kT} - 1 \right] - I_0 \left[ e^{-q(V - R_s I)/kT} - 1 \right]$$

(9)

that corresponds to the parallel of two opposite diodes, with $m$ and $\gamma$ ideal factors respectively, in series with the resistance $R_s$, as shown in the inset of Fig. 8 (c). Eq. (9) provides an excellent fit to the experimental data, as shown in Fig. 8 (c).

From a physical viewpoint, the eq. (9) model considers both the injection of electrons from graphene to Si due to the lowering Schottky barrier in reverse barrier (Fig. 8 (d)) and the injection of electrons from Si to graphene due to the lowering of the Si depletion layer barrier in forward bias (Fig. 8 (e)).

Since the Gr/Si-tips device consists of more than 3 millions tips (corresponding to a total junction area of 6.079 x $10^{-5}$cm$^2$), the homogeneity of the Schottky barrier is an important parameter to check [17]. Assuming that the spatial distribution of the barrier follows a Gaussian distribution, with average value $\Phi_{Bm}$ and standard deviation $\sigma_B$, $P(\Phi_B) = \frac{1}{\sqrt{2\pi}\sigma_B} \exp\left(-\frac{(\Phi_B - \Phi_{Bm})^2}{2\sigma_B^2}\right)$, as shown in Fig. 9 (a), then the dependence of the barrier height on temperature is [18]:

$$\Phi_B = \Phi_{Bm} - \frac{\sigma_B^2}{2kT} .$$

(10)

The experimental data, reported in Fig. 9 (b), follow this model and yield a $\sigma_B = 74$ meV lower than typical values obtained for flat Gr/Si junctions and comparable to the barrier inhomogeneity of industrial M/S Schottky diodes.

The photoresponse of the device was measured under the same conditions of the flat Gr/Si device. Figs 9 (c) and 9 (d) show the response to the white LED light: Taking into account the effective junction area, this photocurrent corresponds to a responsivity $\geq 3$ A/W at 3 mW/cm$^2$. For this device the graphene gating effect is negligible, since the SiO$_2$ layer is too thick (400-450 nm). The record responsivity is due to the field amplification on the top of the nanotips, i.e. in the junction area, which facilitates photocharge separation and likely causes internal gain through impact ionization [10].

Figure 8. (a) Simulated electric field in the space around a Si-tip at V=1V; the field arrows are in logarithmic scale (simulation by COMSOL software). (b) Schottky barrier height as a function of the applied bias; the inset shows the measured I-V characteristics at temperatures stepping from 120 K to 390 K. (c) Fitting of a two-diode model to the I-V curve at room temperature and equivalent circuit (inset). Electron injection due to the modulation (d) of the Schottky barrier height in reverse bias and (e) of the depletion layer barrier in forward bias.

Figure 9. (a) Spatial inhomogeneity of a Schottky barrier. (b) Measured Schottky barrier height as function of the temperature. Photoresponse of the device to white LED light: (c) I-V characteristics and (d) transient response to on/off light switching.
VI. CONCLUSION

We have reviewed key electrical features of the Gr/Si junction and focused on two specific devices. Although caused by different mechanisms, on both devices we have reported a responsibility exceeding that of present solid-state devices. This work unveils new physical phenomena occurring in Gr/Si photodiodes and demonstrates the high potential of such devices as next-generation photodetectors.

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