Ratatoskr: An open-source framework for in-depth power, performance and area analysis in 3D NoCs

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We introduce ratatoskr, an open-source framework for in-depth power, performance and area (PPA) analysis in NoCs for 3D-integrated and heterogeneous System-on-Chips (SoCs). It covers all layers of abstraction by providing a NoC hardware implementation on RT level, a NoC simulator on cycle-accurate level and an application model on transaction level. By this comprehensive approach, ratatoskr can provide the following specific PPA analyses: Dynamic power of links can be measured within 2.4% accuracy of bit-level simulations while maintaining cycle-accurate simulation speed. Router power is determined from RT level synthesis combined with cycle-accurate simulations. The performance of the whole NoC can be measured both via cycle-accurate and RT level simulations. The performance of individual routers is obtained from RT level including gate-level verification. The NoC area is calculated from RT level. Despite these manifold features, ratatoskr offers easy two-step user interaction: First, a single point-of-entry that allows to set design parameters and second, PPA reports are generated automatically. For both the input and the output, different levels of abstraction can be chosen for high-level rapid network analysis or low-level improvement of architectural details. The synthesize NoC model reduces up to 32% total router power and 3% router area in comparison to a conventional standard router. As a forward-thinking and unique feature not found in other NoC PPA-measurement tools, ratatoskr supports heterogeneous 3D integration that is one of the most promising integration paradigms for upcoming SoCs. Thereby, ratatoskr lies the groundwork to design their communication architectures.

Additional Key Words and Phrases: 3D integrated circuits, Network on chip

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1 INTRODUCTION
Networks-on-Chips (NoCs), in which on-chip routers connect components (e.g., processing elements) and transmit data using packets, are one of the most promising communication architectures for state-of-the-art chip designs. NoCs have advantages over conventional approaches such as bus systems: Since the number of components per chip increases constantly, buses become a bottleneck as more and more participants fight for arbitration. NoCs tackle this issue and offer better latency and throughput because of their decentralized nature. This increases system efficiency and thus power consumption. Therefore, integration of NoCs into whole systems has become a vital research topic. Recently, NoCs are found in both the academic designs, e.g., in the Eyeriss CNN-accelerator [10] or in the bio-inspired visual attention engine [26], and the industrial designs, e.g., in the 260-core ShenWei processor Sunway SW26010 processor [11] or AMD’s infinity fabric [29].

In addition to the prevalent trend towards higher core counts, the performance of systems can be increased using novel integration methods. One very promising option is 3D and heterogeneous integration: Vertical 3D interconnects are rather short and therefore the interconnect length and, thus, delay and power consumption of the system are reduced. Plus, the footprint shrinks through stacking because components are divided among layers. Beside these incremental advances, 3D integration allows for one game-changing paradigm: Integration of heterogeneous technologies. This is a fundamental advantage that is efficiently only available using 3D integration.\(^1\) In heterogeneous 3D ICs, dies with varying electrical characteristics and technologies (analog, mixed-signal, logic and memory) are stacked and closely interconnected. The key benefit lies in the possibility to optimize the silicon technology node for the components of each die. Therefore, heterogeneous 3D integration boosts performance, energy efficiency and robustness, and it allows building truly innovative novel architectures for various applications such as high-performance computing, e.g., performance enhancements by interleaving stacking of memory and processing dies [31]. This paradigm is as also applied in Intel’s new Lakefield architecture using Foveros 3D technology [1].

To build fast and efficient communication architectures for these systems, it is essential to design NoCs specifically targeting 3D-integrated and heterogeneous chips.

As for all components integrated into a chip, an in-depth analysis of power, performance and area (PPA) of the NoC is imperative to judge its properties. The PPA figures must take heterogeneous 3D integration into account because heterogeneity changes power models (e.g., [4]) and area and performance vary with technology. Here, we propose ratatoskr: An open-source framework for PPA analysis of 3D NoCs. It is the first comprehensive framework to precisely determine PPA for NoCs from gate level to transaction level, i.e., including a router hardware implementation, a cycle-accurate router model and a transaction-level application model. Furthermore, it supports heterogeneous 3D integration. Such a comprehensive framework cannot be found in the literature so far. While individual tools exist, neither are these integrated into one single tool flow nor are these able to cope with heterogeneous 3D integration: Simulators such as Noxim [14] and Booksim 2.0 [17] allow for performance evaluation of general-purpose NoCs, but do not include router models for heterogeneous 3D integration. Plus, both simulators do not offer an application model on transaction level to inject real-world based traffic pattern out-of-the-box. There exist models for power consumption of routers, such as ORION [23], but these do not model heterogeneity and do not provide a model for dynamic power consumption of links [22, Sec. 2]. Hardware models of routers enable precise area results, but the existing implementations such as OpenSoC Fabric [13] or OpenSmart [27] are not shipped with a simulator for performance comparison and do not

\(^{1}\)2.5D integration allows for heterogeneous integration, as well, but is limited by the rather poor performance of the interconnects though the interposer layer in comparison to a true 3D approach.
reflect the special properties of heterogeneous 3D integration. Thus, ratatoskr addresses these shortcomings by providing the following specific features:

- **Power estimation:**
  - Static and dynamic power estimation of routers and links on a cycle-accurate level.
  - Accuracy of dynamic link energy is within 1% of bit-level accurate simulations.

- **Performance models:**
  - Network performance for millions of clock cycles on a cycle-accurate (CA) level using the NoC simulator.
  - Network performance for thousands of clock cycles on a register-transfer level (RTL).
  - Timing of routers from synthesis on the gate level.

- **Area analysis:** NoC area from synthesis on gate-level for any standard cell technology.

- **Verification:** Gate-level model of NoC enables verification on gate-level against design rule checks (DRCs).

- **Benchmarks:**
  - Support for realistic application model on transaction-level.
  - Conventional synthetic traffic patterns.

- **Heterogeneous 3D Integration:**
  - Heterogeneity yields non-purely synchronous systems, since the same circuit in mixed-signal and digital achieve different maximum clock speeds. Therefore, the NoC simulation and router hardware model implement a pseudo-mesochronous router (cf. Ref. [18]).
  - Heterogeneity yields different number of routers per layers, since (identical) circuits in mixed-signal and digital have different area. Therefore, the NoC simulation allows for any non-regular network topology via XML configuration files.
  - With the same approach, NoCs in active interposers can be modeled, as well.

- **Usability:** Single point-of-entry to set design parameters. The design parameters allow for rapid testing of different designs.

- **Reporting:** Automatic generation of detailed reports from network-scale performance to buffer utilization.

- **Open-source:** The source code of the framework is available from https://github.com/jmjos/ratatoskr.

The remainder of this paper is structured as follows: In Section 2 we give a detailed discussion of related approaches. In Section 3, we introduce the ratatoskr framework by starting from a user perspective and highlight the design parameters that can be set. Next, we dig into the technical details: We explain our models in Section 4 and our implementation of the core components (RTL NoC model, CA NoC model, link model) in Section 5. After these rather technical sections, we shift the focus again to the user perspective and show the generated reports, which the framework provides for PPA analysis in Section 6. In Section 7, we show the results of our framework focusing on properties of the NoC provides as well as the simulation performance; in Section 8 a discussion follows. Finally, we conclude the paper in Section 9.

## 2 RELATED WORK

As already argued, the ratatoskr framework is the only comprehensive framework for modeling, simulation and design of 3D NoCs that provides in-depth PPA results. Nonetheless, individual tools already exist for some of ratatoskr’s features, from which we discuss differentiating features here.

For the cycle-accurate performance models of NoCs, many simulators have been published. An extensive overview is given in Ref. [9, Table II, p. 3]. Three of them are currently state-of-the-art and used in many publications:
- **Noxim** [9] is a NoC simulator implemented in C++ using the class library SystemC. It provides the capability to model conventional 2D and homogeneous 3D NoCs. Furthermore, optical links are included. The simulator measures performance (i.e. network, packet and flit latency).

- **Booksim 2.0** [16] is a NoC simulator implemented in C++. Similar to Noxim, it also provides the capability to model conventional 2D and homogeneous 3D NoCs. It measures performance similar to Noxim.

- **Garnet 2.0** [2] targets a different level of abstraction. It is integrated into the Gem5 full-system simulator and therefore offers very high precision to assess different architectures under real loads. However, Garnet 2.0 does not allow for a fast evaluation of millions of clock cycles due to the naturally slow simulation performance of Gem5.

Both the Noxim and the Booksim 2.0 simulator are limited to be applied in heterogeneous 3D integration because the provided cycle-accurate router models do not specifically target their unique features, specifically non-purely synchronous clocked routers and non-regular topologies. Plus, it is not possible to model routers with varying parameters per layer within the same NoC without extensive source code modifications. Therefore, the existing tools cannot be used for performance analysis in NoCs for heterogeneous 3D systems. **Ratatoskr** addresses these shortcomings.

Regarding **power estimation** in NoCs, **ORION 3.0** [23] is the state-of-the-art tool for modeling power consumption of router’s components. The results can either be used to characterize single routers or they can be included in NoC simulators for high-level (i.e. cycle-accurate) power estimation. While Booksim does not include power-modeling capability, Noxim counts energy-relevant events during simulation [9, Sec. 5.1]. The figures from ORION can be used as input to compute the dynamic router power during a simulation run. Since this is currently the best available option for high-level router power consumption in NoCs, we use the same approach and include Noxim’s power model. ORION 3.0 also has a basic link energy model (cf. Ref. [23, Eqs. 10, 11]) but it does not account for the pattern-dependent coupling switching effects. Since none of the current NoC simulators include power models for links, those within **Ratatoskr** therefore extend state-of-the-art, as published in [22]. Please note, that the effects of pattern-dependent coupling switching are not modeled in any power model of NoC routers and this is, to the best of the authors’ knowledge, still an open research issue. The **Ratatoskr** framework also allows for power estimation at RTL by using the provided NoC implementation for gate-level simulation. This generates the most precise numbers including the effects of pattern-dependent coupling switching activities; however, it is very slow and can only be used for thousands of clock cycles while the NoC simulator within our framework can handle millions of clock cycles. Thereby, **Ratatoskr** covers the full stack of power estimations and can generate results at different accuracy levels and speeds.

For **area analysis** a hardware implementation of a NoC is required. Among the popular open-source implementations, Stanford university [3] provides the implementation of the router architecture from [7]. As another example, the OpenSoCFabric project [13] is quite popular. It allows for 2D mesh and 2D flattened butterfly topology with wormhole routing and virtual channels. The implementation is written in Chisel and enables a run-through ASIC flow. While the provided router is very advanced and rich of features, it does not provide support for 3D integration. OpenSMART implements a "single-cycle multi-hop asynchronous repeated traversal router" [28, p. 1], which is state-of-the-art in terms of performance. It allows for non-regular network topologies, but it does not feature 3D integration. Due to their shortcomings, none of the popular NoC implementations can be used for our framework.

In general, when building a **NoC for heterogeneous 3D integration**, routers must be able to provide two features: First, non-purely synchronous communication must be possible. In Ref. [18], we discuss this topic in detail and propose a pseudo-mesochronous router architecture that enhances
throughput by 2x, latency by 2.26x and dynamic power consumption by 41% with a small hardware overhead of 2.01% for synthetic and real-world-based benchmarks using 15nm digital and 45nm mixed-signal technology nodes compared to a conventional NoC design with homogeneous routers, i.e. the same routers regardless of the layer’s technology node. Second, reductions of area costs in the routers in mixed-signal layers are essential. This can be achieved by moving resources from this layer into faster and more area-efficient layers. We assess this for buffer re-ordering in Ref. [20] and achieve area reduction of 28% and power savings of 15% at a small 4.6% performance loss for 130nm and 65nm nodes; for routing algorithms, we show up to 6.5x latency improvements in Ref. [18] for different technology scenarios. These two main previous works form the foundation, on which we develop the router model within the ratatoskr framework. The ratatoskr framework was used to generate results for many publications, e.g. the aforementioned and Ref. [4–6].

3 THE RATATOSKR FRAMEWORK

Here, we introduce the ratatoskr framework from the user perspective before we gradually go into technical details in the subsequent sections. In this section, we explain the framework’s parts and their functionality to generate an in-depth PPA analysis and introduce the process to set design parameters.

3.1 Parts and functionality of the framework

The parts and functionality of ratatoskr is shown in Fig. 1. Seen from the most abstract perspective, the tool flow of the framework is tailored towards in-depth PPA generation for the user: Design parameters are set and the framework generates PPA reports. Using these results, the user can modify the parameters until design constraints are met.

There are two sets of design parameters, separated by their target: Network properties and application properties, as shown on top of Fig. 1 on top in green boxes. The network properties include the network topology and floorplan, the number of virtual channels (VCs), the buffer depths, used routing algorithm and the link dimensions; the application properties define either a synthetic traffic pattern or an instance of the application model (cf. Sec. 4.1). Setting the parameters is simple, as only a single-point of entry file bin/config.ini is modified and a Python script
bin/configure.py is executed. They set up the whole framework. The detailed options for parameters are introduced in Sec. 3.2. The Python script bin/plot_network.py opens a GUI and displays the network with a floorplan.

The actual execution of the framework starts after setting the design parameters using the aforementioned Python script. In general, there are three parts in ratatoskr, which reflect the different levels of abstract present. The parts are depicted in Fig. 1 in blue boxes; they are

- **RTL NoC**: The box on the left-hand side shows the hardware model of the NoC: On RT level, a NoC is generated using Python scripts for meta-programming of VHDL code from the network properties. The implemented router is the novel pseudo-mesochronous vertical high-throughput router as published in our previous work [18]. The properties of this router are discussed in detail in Sec. 4.2.

  Having a RTL NoC, has two advantages: First, it is is converted to gate level and thus it can be verified to conduct DRCs. Second, the RT level NoC can be synthesized for standard cell libraries. This generates precise data for NoC power, NoC area and router timing. Plus, it is possible to get results for heterogeneous 3D integration with different technology nodes.

  As a comfortable area-saving feature, our scripts removes unused parts of the crossbar automatically based on information about the routing algorithm. This allows increasing area efficiency by up to 30% over conventional routers, as synthesis for a commercial digital technology demonstrates.

  The whole RTL NoC can be simulated using VHDL simulators. We provide processing elements that inject uniform random traffic as well as a trace-file based traffic generator for real-world application traffic. While RTL simulation is very precise, it is also very slow and only a few thousand clock cycles can be simulated realistically. Therefore, we provide a higher simulation performance of the NoC on CA level.

- **CA NoC Model**: The aforementioned NoC simulator on CA level is shown on the blue box in the middle of Fig. 1. It actually takes both the network and the application parameters as input. The latter are required to load realistic traffic patterns into the network. The CA router model copes with the non-purely synchronous transmission of data, which is typical for heterogeneous 3D systems. This is a novel feature not to be found in the competing simulators. The simulator can be run using the Python scripts bin/run_simulations.py or by directly running the executable. Since the simulator is a complex software and the core of the framework, Sec. 5.1 is dedicated to the technical details.

  The simulator generates results for the network performance (e.g. flit latencies) and the dynamic router power. We use the power model of Noxim, in which power-relevant events are counted, cf. [14, Sec. 5.1]). As an innovative feature, the simulator stores transmission matrices. In short, these report the transition probabilities between idle and non-idle states and the data types transmitted (i.e. modeled by the colors in the application model) of all links in the network. This feature allows for precise dynamic and pattern-dependent link energy, as explained in the next paragraph.

- **Link model**: To generate precise power results for the links, we use our power models for single (vertical and horizontal) links [4, 6] and integrate them into our framework. This requires using the aforementioned transmission matrices. It enables precision within 1% of much slower bit-level simulations and also allows for post-simulation assessment of different hop-to-hop data codings without a second simulation execution. The power models are implemented in Python can be found in the power folder.

After finishing the execution of the framework, PPA results are generated as shown in the bottom-most part of Fig. 1. Beside the individual results of the framework’s parts, which already
Table 1. A description of software and hardware configurations using the configuration ini file.

| Property          | Section       | Field                                      | Description                                                                 |
|-------------------|---------------|--------------------------------------------|-----------------------------------------------------------------------------|
| Application       | Config        | simulationTime                             | length of simulation in ns                                                  |
| Properties        |               | flitsPerPacket                             | maximum length of packets                                                  |
|                   |               | benchmark                                  | ["synthetic", "task"] to select application model                        |
|                   | Task          | libDir                                     | folder path for configuration data                                         |
|                   | Synthetic     | simDir                                     | folder path for temporary data                                             |
|                   |               | restarts                                   | number of simulations                                                      |
|                   |               | warmupStart, warmupDuration, warmupRate    | length and injection rate in warmup phase                                  |
|                   |               | runRateMin, runRateMax, runRateStep        | injection rates for the simulation                                         |
|                   |               | runStartAfterWarmup, runDuration           | timing of main run phase                                                   |
|                   |               | numCores                                   | number of cores used                                                       |
|                   | Report        | bufferReportRouters                        | list of routers’ ids to be reported                                        |
|                   |               | bufferDepthType                            | ["single", perVC"] single or VC-wise buffer depth                        |
|                   |               | bufferDepth                                | value for buffer depth                                                     |
|                   |               | buffersDepths                              | list of buffers depths (one for each VC)                                  |
|                   |               | vcCount                                    | list of VCs per router port                                               |
|                   |               | topologyFile                               | file with network topology                                                |
|                   |               | flitSize                                   | bit-width of flits                                                        |

have been described before, ratatoskr also encapsulates the most relevant ones into reports. This maintains high usability and is in-line with our approach to a rapid design space exploration by iterating design parameters and testing them against constraints.

### 3.2 Setting design parameters

The design parameters that can be set using the config.ini file are shown in Table 1. As already introduced, network and application properties are configured separately.

The application configuration has four sections. In Config, the general parameters of the simulation are given: The simulation time and the maximum length of packets are set for the network; the selection between synthetic or application model and a directory for application model files are set for the benchmark. In Task, the folder holding the two files for the application model is given. These are xml descriptions of the task graph and of the mapping of tasks to processing elements (cf. Section 4.1). In Synthetic, synthetic traffic patterns are configured: The number of simulation runs, used CPU cores and the temporary directory are given. Synthetic patterns have multiple phases and the duration of warm-up and run phases can be set. Furthermore, in Report, the reports can be configured. A list of routers can be defined that are included in the generation of statistics which allows excluding edge-cases such as routers at the borders of the network.

The network configuration has no sections. Here, all parameters of NoC and routers are set. This includes the number of layers in a 3D chip as well as the router count per dimension for conventional 3D mesh topologies. Note that the dimensions are a list to implement floorplans with different router counts per layer as found in heterogeneous integration. If other topologies than
mesh are desired, a configuration must be done via separate Python scripts. Plus, the clock delay is set by a list, because of varying clock frequencies in heterogeneous 3D systems. Furthermore, the VC count and buffer depths are configured; this is possible per router or per individual VC. Next, a file path to the network topology is given. Finally, we set the bit-width of flits.

It is possible to configure the network and the application for the simulator in further extend by modifying the intermediate xml, which the configuration Python scripts generate as input for the next stage of the framework, especially the simulator. The xml files are described in Section 5.1.

4 ARCHITECTURES AND MODELS

4.1 Application model

We start the description of the architecture and models on the top-most abstraction level: The application model on transaction level. It must be abstract yet accurate and at the same time account for all properties of typical application executed on system-level. Since we especially target heterogeneous 3D chips, the relevant application areas must be covered; This includes a broad spectrum of use cases: Many platforms have been proposed from high-performance processors [25] to Vision SoCs for image processing [32] and wireless sensors for IoT (Internet of Things) [15]. Therefore, the application model must account for (1) the timing of processing, which may change depending on input data and implementation technology, (2) the dynamic effects of varying input data (i.e. the statistical expected behavior) and (3) the data types transmitted for precise power modeling (for pattern-dependent switching coupling activities). We discussed models for applications in heterogeneous 3D SoCs in [19]. There, we argue in detail that colored statistical Petri nets with retention time on places are able to model all effects required. The colors are used to differentiate varying data streams with respect to pattern-dependent coupling switching.

In general, a Petri net is an application model using graphs, in which data flows along edges are abstracted by tokens transmitted between places (vertexes). Our Petri nets model property (1) by retention times, which delay sending tokens; property (2) is modeled using a statistical net, in which sending tokens is associated with probabilities; property (3) is modeled by annotating tokens with colors that reflect the activities along the data flows. An example for such a Petri net is shown in Fig. 2. There are two places $p_1$ and $p_2$ modeling tasks in the application. The processing time on that places is in the given intervals: $[4, 7]$ and $[2, 3]$, respectively. With probability $\hat{p}$, the application sends tokens from $p_1$ to itself and with probability $1 -\hat{p}$ to $p_2$. The tokens are colored, here depicted with red squares and purple circles (the shape is used for better accessibility). In that very figure, we also show an exemplary layer of a NoC with $2\times3$ mesh topology in green. Each rectangle represents a tile comprising router, network interface (NI) and processing element (PE). The Petri-net is mapped on this network topology. The implementation of our application model and an introduction on its configuration is described in Section 5.1.

Fig. 2. Example for mapping of application model to NoC.
4.2 Router hardware architecture

We use a lightweight router architecture both on RT and CA level that suits the needs of heterogeneous 3D interconnects. By configuration interfaces, we also enable rapid prototyping. The technical details of the router are the following: We use wormhole packet switching to reduce buffer depths, which are rather expensive especially in mixed-signal nodes. Flow-control is realized with credit counters. Number of ports is flexible in this design; therefore, it can be used in networks with different topologies. This is highly relevant for applications in heterogeneous 3D SoCs since irregular topologies are to be expected. Both simulator and router support varying flit widths. The router architecture is shown in Fig. 3. It is split into three major parts: In the input ports, the flits are stored in buffers. The model implements VCs and the number of VCs and the buffer depth per VC can be set individually per router and per port. Thereby, smaller routers for instance in mixed-signal layers can be realized by e.g. by smaller buffers depths or less VCs. The central control unit uses the architecture proposed by [8], building the most light-weight router possible, which allows to use the router in expensive technology nodes as well (such as mixed-signal layers). Requests from the input ports will be processed and acknowledgments will be generated if a path is free. The central control unit has a modular design and consists of routing calculation, VC allocation, port allocation and switch allocation units. The VC arbiter prioritizes VCs with lower number, i.e. the first free VC with the lowest number is chosen. The allocation is done in input-first-manner; thus, one VC per input port requests and output port per clock cycle. The next VC may send a request after the previous VC received an acknowledgment, following round robin. The output port assigns acknowledgments also using round robin. The switch allocation does not perform maximum matching due to its large costs. Rather, a separable-input-first allocation is used for the switch allocation. It offers lower costs, but saturation rate is higher; this issue for saturation is actually negligible for the networks with few VCs [8]. Routing decisions are made in routing computation unit. The crossbar connects input ports and output ports. It has MUX-based architecture to minimize the control signals. We do not connect inputs and outputs, which are not possible based on the routing algorithm (cf. implementation details in Sec. 5.2). Thereby, the size of the crossbar may be reduced by a significant portion, as explained in the results in Sec. 7.2. To summarize, our router supports rapid testing of different design by means simple setting of the following design parameters, as shown in Fig. 3:

a) the input port count,
b) the VC count per port,
c) the buffer depth per port and VC and
d) the turns forbidden by the routing algorithm for automatic area-reduction of the crossbar
4.3 Power model

The power models comprise the dynamic energy of the router and of the links in the network. We take both into consideration, since related work showed that links cause between 17% in the Teraflop router [23] and up to 53.9% in the NOSTRUM 8×8-NoC [30, Table 1, p. 4] of the overall energy consumption of the network. Extensive work on the power consumption of routers has already been conducted: ORION 3.0 [24] provides the most detailed models for energy consumption of the individual router’s components. The framework abstracts the power consumption for different technology nodes. ORION 3.0 is not directly linked to a NoC simulator. The Noxim simulator includes power models into NoC simulations, as introduced in [9, Sec. 5.1, pp. 14-15]. In essence, Noxim counts power-relevant events in the router such as buffer write and buffer read, routing calculation etc. The values for each event are gathered from other sources (e.g. bit-level simulations or models such as ORION). Because of these extensive related works, we do use the same power models as Noxim within our simulator; the implementation in C++ is briefly introduced in Section 5.3. We do not include a further description of the models here and kindly refer to [9, Sec. 5.1, pp. 14-15].

There has been some research on the power consumption of links. While ORION includes a basic power model, as introduced in Eqs. 10 and 11 in Ref. [24], the effects of pattern-dependent coupling switching are not accounted for. However, we showed in [6] that this can lead up to 79.77% modeling error. One option to leverage this error would be bit-level accurate link simulations; this, however, is too slow for a simulation of a complete NoC. Another option is to characterize data flows by their typical switching activities, modeled using the colors, such that flows with similar coupling switching properties are annotated with the same color in the application model. This can be used to calculate the pattern-dependent coupling switching in links. Therefore, we introduce the concept of data-flow matrices $M$ for each link in NoC simulations. The entries of a data-flow matrix $M$ depend on the NoC hardware, i.e. VC count, arbitration, buffer depth, topology, and the application. For the latter, we use the colored Petri-net application model (cf. Section 4.1), in which each transmission between two tasks in an application is annotated with a color $\sigma_i$ from the set of all colors $\Sigma = \{\sigma_1, \ldots, \sigma_n\}$. A data-flow matrix therefore denotes the transitions between different colors on that link and also denotes, if a link was idle or used. For $n$ colors, each data-flow matrix $M$ has the size $[0,1]^{2n+3\times 2n+3}$. It has a row and column for each color both as active (data of that color have been sent) or idle (last time the link was active, data of that color have been sent), head flits (active/idle) and an initial state until data were sent the first time via this link. In Ref. [19], we introduced a toy example using a simulation of a router without VCs, which is passed by two data streams with different colors and different injection rates of 0.5625 flits/cycle and 0.1875 flits/cycle. This results in a transmission matrix such as:

\[
\begin{pmatrix}
\text{idle} & \text{(head, data)} & \text{(head, idle)} & \text{(\(\sigma_1\), data)} & \text{(\(\sigma_1\), idle)} & \text{(\(\sigma_2\), data)} & \text{(\(\sigma_2\), idle)} \\
\text{idle} & 0.010 & 0.000 & - & - & - & - \\
\text{(head, data)} & - & - & 0.019 & 0.042 & - & 0.014 & - \\
\text{(head, idle)} & - & - & 0.007 & 0.013 & - & 0.005 & - \\
\text{(\(\sigma_1\), data)} & - & 0.041 & - & 0.326 & 0.126 & - & - \\
\text{(\(\sigma_1\), idle)} & - & 0.013 & - & 0.113 & 0.039 & - & - \\
\text{(\(\sigma_2\), data)} & - & 0.014 & - & - & 0.114 & 0.045 & - \\
\text{(\(\sigma_2\), idle)} & - & 0.006 & - & - & - & 0.040 & 0.014 \\
\end{pmatrix}
\]

To highlight the expressiveness of the matrix, it shows this example that 32.6% of all transmissions of color $\sigma_1$ are followed by the same color (Matrix read row-wise). Based on these pieces of information, the power consumption of the network can be calculated: Different colors represent data with different coupling and switching activities. Thus, the power consumption for packets with the same color is similar. This abstraction allows for precise and fast power estimation. At this point, we do
not dig deeper into the details of the power model such as the physical formulae, as it has been published in Ref. [6]. However, the implementation of the power model in Python is discussed in Sec. 5.3. The performance and accuracy of our approach are introduced and discussed in Sec. 7.3.

5 IMPLEMENTATION

5.1 NoC simulator using C++ and SystemC

The NoC simulator inside the ratatoskr framework is implemented in C++14 using SystemC 2.3.3 class library, which provides a simulation kernel. All design parameters can be set without modifications to the code and therefore without recompiling. Only if novel functionality is required, the core will change; this is easy due to our clear class hierarchy. We start by explaining our software architecture. Next, we dig into implementation details of interesting components.

5.1.1 Software architecture. A component diagram of the main parts is depicted in (Fig. 4). The dotted arrows represent the dependency between two components (the component at the arrow’s source depends on the component at the arrows’ end). We did not draw all the components of the system for the sake of brevity. One can see that the NoC class reads the configuration of the simulation from the config.xml file and the configuration of the NoC from network.xml, both located in a configuration folder. The NoC class then hosts all components of the network: First, the RouterVC class implements the router model with VCs. Second, the NetworkInterface class interconnects PEs and routers. Third, the ProcessingElement class implements the PEs by providing a platform to simulate the application model and hosting tasks. All three components are connected by SystemC signals for data, flow control, etc. We abstract these in the SignalContainer class for easy use and maintenance.

The simulator inside ratatoskr provides two router models, a small standard router based on [8] and a vertical high-throughput link/router [18], as well as four routing algorithms. Furthermore, it is possible to extend the code by adding new classes (e.g. novel router models or other routing algorithms) that implement the abstract classes provided by our solution (see next paragraphs and Fig. 5). Therefore, one only has to write a C++ implementation, then register it in the constructor of Router base class and compile.

5.1.2 Implementation details. In this section we discuss the implementation details and the benefits of such design. In Fig. 5, we see the general software architecture of the ratatoskr framework. The top-level class is Noc. All NoC components are inheriting form the NetworkParticipant class. The NoC class is the top-level class in the simulator. It contains a vector with all NetworkParticipants.
Each NetworkParticipant provides two virtual functions: initialize that initializes components and bind that binds the signals of connections between components. This directly follows the SystemC-modeling style. The NoC simulator provides three types of network participants: Router, ProcessingElement and NetworkInterface. Each one of these classes is realized through a concrete class implementing the virtual functions of their base classes (namely initialize and bind). Furthermore, the behavioral model of the components is implemented in the concrete classes with the suffix VC. We use modern C++ (C++14) extensively within these models; this does not only enable reader-friendly code but also a more abstract modeling. For instance, within the router there are no further SystemC sub-modules; rather, the communication within the router between VC allocation, arbitration and switch, as introduced in Section 4.2, is realized via data structures from the standard library. For instance, request and acknowledgments are std::maps that constitute the router architecture in data. The advantage lies in the option to iterate these data structures. This flat hierarchy is advantageous both for better software maintenance and higher simulation performance, as SystemC modules and communication via ports result in context switches during simulation. The implementation of routing functions is also shown in Fig. 5, on the bottom-right part. There is a base class BaseRouting, which has a virtual function route; it takes the current node’s address and the destination’s address as input and calculates an output port. We provide a set of deterministic, low-overhead routing algorithms for heterogeneous 3D SoCs as published in [18]. To summarize, we used inheritance and polymorphism programming paradigms to achieve a highly maintainable and flexible architecture. The user can freely add implementations of new participants or routing algorithms without breaking or recompiling the code base.

5.1.3 Detailed configuration using XML files. Using xml files allows for a very fine-grained configuration of the NoC under test. We provide an example of the hardware description in Fig. 6. The file starts with the definition of routers and PE using the nodeTypes tag. Nodes are identified using unique ids. First, we show the definition of a router with VCs using dimension-ordered routing and 1 GHz clock frequency. Second, a PE is defined with VCs and 1 GHz clock frequency. Next, the nodes are instantiated in the nodes tag. Each node has a position in 3D space, is associated with one of the nodeTypes and has a unique id. Finally, connections between nodes are defined. Each connection has two ports. The end-points of the ports are connected using the unique node ids; furthermore, the VC count is defined and the buffer depth is set (either for all VCs or VC-wise). Via the connection’s data structure any topology for a heterogeneous 3D SoC can be defined. Since the xml files tend to be rather long, we provide Python classes for their functional definition.

We also provide an example for the application description using colored statistical Petri-nets with retention time on places in the code shown in Fig. 7. One exemplary task, which implements places, is defined there. Tasks have unique ids. In-going and out-going data connections are configured with the requires and generates tags. Application data are generated after all required data, from
the `requires` tag, are available. To model the stochastic property, data can be sent to different destinations, which are grouped into a `possibility` each that is selected following a given probability. The timing of tasks and the retention time on places is modeled using the tags `start`, `duration`, `repeat`, `interval` and `delay`. A task is only executed in between the `start` time and until its `duration` is finished. A task will also stop execution, if it was repeated for as many times as given by the tag `repeat`. For each repetition, one data send possibility is taken. If tokens are available, a task sends data to this destination. It will send data count times. There is a delay in-between sending data, in which the task is idle; this implements the retention time. The colored Petri net is realized by defining data types as shown in the lower part of the code in Fig. 7. We do not provide an exemplary mapping file because of its simple structure mapping task ids to PE node ids.

### 5.2 NoC router using VHDL

The implementation of the router in VHDL is straight-forward following the modular architecture introduced in Sec. 4.2. It can be configured for the aforementioned design parameters by using the python script `hardware/vhdl_writer.py`. These take the `config.ini` as an input and write VHDL sources, accordingly. The script also generates a directory as input for synthesis, e.g. with Synopsis design compiler. There are four network options:

1. A NoC using a conventional router as introduced in Sec. 4.2.
2. A NoC using the high-throughput router as introduced in [18].
3. A NoC with PEs injecting uniform random traffic using the conventional router.

```xml
<nodeTypes>
  <nodeType id="0">
    <model value="RouterVC" />
    <routing value="XYZ" />
    <clockDelay value="1" />
  </nodeType>
  <nodeType id="1">
    <model value="ProcessingElementVC" />
    <clockDelay value="1" />
  </nodeType>
</nodeTypes>

<nodes>
  <node id="0">
    <xPos value="0"/>
    <yPos value="0"/>
    <zPos value="0"/>
    <nodeType value="0"/>
    <idType value="0"/>
  </node>
...<nodes>
</connections>
<con id="0">
  <ports>
    <port id="0">
      <node value="0"/>
      <bufferDepth value="16"/>
      <vcCount value="3"/>
    </port>
    <port id="1">
      <node value="0"/>
      <buffersDepths value="10, 20, 30"/>
      <vcCount value="3"/>
    </port>
  </ports>
</con>
...<connections>

Fig. 6. Example for configuration of a NoC.

```xml
<task id="1">
  <start min="0" max="0"/>
  <duration min="100" max="100"/>
  <repeat min="2" max="2"/>
  <requires>
    <requirement id="0">
      <type value="1"/>
      <source value="0"/>
      <count min="1" max="1"/>
    </requirement>
  </requires>
  ...<requires>
  <generates>
    <possibility id="0">
      <probability value="1"/>
      <destinations>
        <destination id="0">
          <delay min="0" max="50"/>
          <interval min="10" max="10"/>
          <count min="3" max="3"/>
          <type value="1"/>
          <task value="3"/>
        </destination>
      </destinations>
    </possibility>
    ...<possibility>
  </generates>
</task>

```xml
<data>
  <dataTypes>
    <dataType id="0">
      <name value="image"/>
    </dataType>
    ...<dataTypes>
  </data>

Fig. 7. Example for a configuration of an application.

```
(4) A NoC with PEs injecting uniform random traffic using the high-throughput router.

The two latter options can be used for verification as well as VHDL simulation. Also, the NoC can be synthesized for FPGA-based prototyping [12], as well.

In addition to the configuration options, we also target low area overhead. Therefore, we remove turns from the crossbar that are impossible within the routing algorithm to reduce its size. We use a data structure, in which the possible and impossible turns are stored. Based hereupon, the crossbar either connects the input to the output port or both to ground. In the latter case, the synthesis tool optimizes the links and, automatically, the size of the crossbar is reduced without further user interaction.

We also provide a VHDL traffic generator and receiver based on trace files generated by Python scripts that are connected to our simulator (or any other high-level tool to generate traffic patterns). A so-called "Data Generate Unit" then injects the traffic based on the patterns information on the packet length and the injection time. Furthermore, we ship a "Data Converter Unit". It allows to convert the received data from the network to a end-user-friendly data format. Specifically, it allows to: (1) back/conversion of received data to the original data type and do further processing (like noise analysis); (2) comparison of the received data (from hardware simulation) and the generated data (from high-level simulation) for verification and error analysis; (3) reporting of system statistics just as generated from the high-level model. This hardware-level functionality gives the user an extended framework for verification, prototyping and emulation.

5.3 Power models using Python

The dynamic router energy is implemented just as in Noxim. Five events are tracked: A buffer write, a buffer read, popping the head element from a buffer, routing calculation and crossbar traversal. The occurrences of these events are counted using a power class, which is singleton.

The dynamic link energy is calculated using the aforementioned data-flow matrices during simulation, which then are fed into a Python implementation of the power model along with the correct parameters for link width and size, switch activities represented by colors in the application model and the used technology nodes. The data-flow matrices could be generated during data sending in the routers. Although this would slightly increase simulation performance, we implemented a separate Link class. This allows for better maintainability and readability of the code. The links are modeled cycle-accurate and add an entry to the correct entry in the data-flow matrices in each clock cycle. Links are modeled unidirectional, because of non-purely synchronous interaction between routers. When a simulation stops, the data-flow matrices are written into csv files that then are read by the aforementioned Python model. The Python scripts are given in the folder power. An interconnect package implements four classes: The class Driver implements the model for the driver of a link, and the class Interconnect implements the physical models for the link itself. The class DataStream and DataStreamProb implement the properties of data streams (i.e. colors in the application graph). An exemplary usage of the link power model is shown in Fig. 8. First, the properties of a 3D link are defined. Next, the parameters are passed to the link model. As additional features, the link model does not only calculate power but can also be used for other physical properties of the links. For instance, one can obtain the maximum length (in mm) based on target clock frequency (and vice versa); the link area including keep-out-zones is also provided for any link design. Finally, three data streams are defined. The first is based on samples and the second and third on expected behavior. Finally, the energy is calculated using these data streams and a data-flow matrix as given from the simulator.
from interconnect import Interconnect, Driver, DataStream, DataStreamProb

# define 3D link
phit_width = 16 # transmitted bits per link (incl. flow-control, ECC, etc.)
wire_spacing, wire_width = 0.6e-6, 0.3e-6
TSV_pitch, TSV_radius, TSV_length = 8e-6, 2e-6, 50e-6 # length is constant
metal_layer = 5
ground_ring = False # structure used to reduce TSV noise (affects power)
KOZ = 2 * TSV_pitch
driver_40nm_d4 = Driver.predefined('comm_45nm', 4) # comm. 40nm driver / or define own via Driver()

# set parameters of link
interconnect_3D_dig = Interconnect(B=phit_width, wire_spacing=wire_spacing, wire_width=wire_width,
metal_layer=metal_layer, Driver=driver_40nm_d4, TSVs=True, TSV_radius=TSV_radius,
TSV_pitch=TSV_pitch, TSV_length=TSV_length, KOZ=KOZ, ground_ring=ground_ring)

# get maximum length based on target clock frequency
f_clk_dig = 1e9
l_max_3D_dig = interconnect_3D_dig.ms.max_metal_wire_length(f_clk_dig)

# get area of link
TSV_area = interconnect_3D_dig.area_3D

# define three datastreams with different properties
ds1 = DataStream(ex_samp, B=16, is_signed=False) # 16b data stream from specific samples
ds2 = DataStream.from_stoch(N=1000, B=16, uniform=1, ro=0.4) # random dist. ro := correlation (1000 samples)
ds3 = DataStream.from_stoch(N=1000, B=16, uniform=0, ro=0.95, mu=2, log2_std=8) # gaussian

# calculate energy based on data flow matrix from matrix
E_mean = interconnect_2D_dig.E([ds1, ds2, ds3], data_flow_matrix)

Fig. 8. Exemplary usage of the link power model.

6 AVAILABLE PPA REPORTS

Our proposed tool provides the PPA measurements for the NoC in the whole chip. In short, the following is provided:

**Performance**
- Mean and median flit delay
- Mean and median packet delay
- Mean and median network delay

**Power**
- Dynamic router power (Noxim)
- Dynamic link energy

**Area**
- Router area for a given technology node
- Link area

After simulation, the *ratatoskr* framework generates several reports about the aforementioned measurements. First, there is a textual report (*report*.txt); it is the most general and basic information, namely the average flit, packet and network latencies. Furthermore, the clock count and delay per layer and all (normalized) data-flow matrices per link are included. Second, *report_Links.csv* contains flattened link data-flow matrices without normalization, for further automated processing. Third, *report_Routers_Power.csv* contains the dynamic power of each router. Forth, the usage of virtual channels is reported. The *VCUsage* folder contains VC usage per each router, with csv files named after router IDs. The rows of each file denote the ports of a router (in order: local, east, west, north, south, up and down) and the columns represents the count of VCs used, i.e. in the first row, all VCs are empty and in the last row all VCs are filled with at least one flit. Fifth and finally, the usage of buffers is reported, as well. The *BuffUsage* folder contains the buffer usage of the routers as csv files, named after router ID and direction. The rows of the file are equal to the buffer depth and the columns denote the VC numbers. Thereby, a usage count for each buffer element is given.

When executing the fully-automated tool flow using the Python scripts *run_simulation.py*, *ratatoskr* collects all necessary pieces of information from the previous files and generates a pdf file with a visual summary. It includes three types of plots: The network performance, i.e. the latency over injection rate; the average buffer usage per layer and direction as 3D histograms

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and the average VC usage per layer as histogram. The exemplary plots are given in Fig. 9. In Fig. 9a the network performance is given for different injection rates for an exemplary network configuration, namely a 4×4×4-NoC with three heterogeneous technologies. Our reports include the standard deviation as well as the mean of the relevant latencies. In Fig. 9b the VC usage is given for the lower layer (therefore, the downwards direction is never used). One can see, that higher VC numbers are less used, which is in line with the router model. Also the pressure on west and east is higher, which is a consequence of XYZ routing and round-robin VC arbitration. Finally, in Fig. 9c a histogram is given, which reports for one exemplary direction in a layer the number of times, a certain buffer usage and VC usage were given. These three reports available from ratatoskr give in-depth insight into the network dynamics and allow for router parameter optimization even on a micro-architectural level, e.g., for single buffer elements.

To summarize, the automatically generated reports available by our framework provide in-depth insight into the NoCs PPA. Especially the buffer usage and the VC usage that extend the related work, as this feature is new. It is tailored towards heterogeneous 3D integration, because we average the reports per layer. Thereby, routers can be optimized in each layer, an thus per technology node, to meet both the technological and application’s requirements.

\footnote{In this example, we use 130 nm, 65 nm and 32 nm technology nodes.}
Results

7.1 Simulation performance

The simulation time for different injection rates is shown in Fig. 10. We simulate a 4×4 NoC with 32 flits per packet, 4 flit deep buffer, 4 VCs and dimension order routing (XY-routing) with Booksim 2.0 (depicted as green rectangles), Noxim (orange circle) and our simulator inside ratatoskr (blue cross). Uniform random traffic is injected into the network. The injection rate is increased from 0.015 flits/cycle to 0.08 flits/cycle in steps of 0.05 flits/cycle. We run 10 simulations using Ubuntu 18.04 on a single core of an Intel i7-6700 at 4GHz. Fig. 10 reports the median and the standard deviation of the run time. Both Noxim and ratatoskr do not change their performance with larger injection rates, while Booksim 2.0 does. For low injection rates, Booksim 2.0 is faster than the other two competitors; this relation is reversed for injection rates higher than 0.035 flits/cycle. Ratatoskr is consistently slower than Noxim with approximately four to eight seconds.

The simulation time for different network sizes is shown in Fig. 11. We simulate a NoC of varying size with the same properties as in the last example. Uniform random traffic is injected into the network with an injection of 0.03 flits/cycle. The network size is increased from 4×4 to 10×10 in steps of 1. Again, we run 10 simulations on the aforementioned machine. Fig. 11 reports the median and the standard deviation of the run time. The performance relation between the programs remains the same for all network sizes: Booksim is slower than ratatoskr, which is slower than Noxim.
7.2 PPA of router hardware

We ship an automatically configured and synthesizable hardware implementation along with each simulation run. Here, we shortly showcase the PPA figures of the high-throughput router architecture:

The network performance is shown in Fig. 12: The average flit latency and packet latency for different injection rates from 1% to 8% in [flits/cycle] are shown using a 4×4×4 NoC with dimension-ordered routing, 4 VCs, 4-flit deep buffer and 1 GHz clock speed. We simulated 100,000 clock cycles injecting uniform random traffic pattern. Both the average and the standard deviation are reported in the figure.

To report area and power, we synthesize the same router for 45 nm technology at 250 MHz frequency. We compare three experimental setups, as shown in Tab. 2: First, we use a router with a fully connected crossbar as baseline. Next, we use conventional XYZ dimension-ordered routing, which removes turns from the crossbar. This router does not account for the possible and impossible turns from the routing algorithm. Finally, we use Z⁺(XY)Z⁻ routing algorithm from [18]. This routing algorithm shows very high performance for heterogeneous 3D SoCs and has less turns possible than conventional XYZ. We report the numbers for power in [µW] and area in [µm²] for both the complete router and its crossbar. One individual inner router has a total cell area of 37899 to 39168 µm² and a total power of 4.57e+03 to 5.4e+03 mW depending on the routing algorithm. We also highlight the advantages of our crossbar size reduction as well as power savings using information about the routing algorithms.

| Router | Crossbar | Router | Δ | Crossbar | Δ | Router | Δ | Crossbar | Δ |
|--------|----------|--------|----|----------|----|--------|----|----------|----|
| Power [µW] | 5.40e+03 | 183.588 | 4.49e+03 | -17% | 64.005 | -65% | 4.57e+03 | -15% | 71.162 | -61% |
| Area [µm²] | 39168 | 1288 | 37942 | -3% | 894 | -31% | 37899 | -3% | 880 | -32% |

Table 2. Router cost reduction by removing impossible turns of routing algorithm

7.3 Power modeling capabilities

To demonstrate the accuracy of our power models, we compare the estimated link power for a NoC with and without VCs against a bit-level accurate simulation. The results are based on the case study provided in [22, Sec. 8 and Fig. 7], in which a 3D Vision SoC is simulated that consists of one layer in mixed-signal technology and one in memory technology. Six analog-digital converters in the mixed-signal layer send their 512×512-pixel image data to a single memory in the adjacent layer via a NoC. The injection rate of image traffic is set to 20% per sensor. As shown in Tab. 3, the used models are always within 2.4% of the bit-accurate simulations, while conventional models that do not account for pattern-dependent switching coupling and virtual channels yield an error of up to 42.5%. For a NoC without VCs, both the conventional and ratatoskr’s power models yield a low error of <1%. Neither Booksim nor Noxim provide this power analysis feature; the accuracy for links is higher than ORION 3.0’s power estimation (which is not embedded into simulations).

8 DISCUSSION

The simulation performance is evaluated for varying injection rates and network sizes: First, concerning the simulation time for different injection rates, see Fig. 10. Booksim 2.0 has a very high performance for small injection rates (by disabling router without traffic). However, the simulation speed is reduced linearly with higher injection rates. For injection rates higher than 0.02 flits per
cycle, Noxim is faster than Booksim. For injection rates higher than 0.035 flits per cycle, ratatoskr’s simulator is faster than Booksim. In fact, for the highest injection rate evaluated (0.08 flits/cycle) Booksim 2.0 is 2.3× slower than ratatoskr. Both Noxim and ratatoskr have a constant simulation time independent from the injection rate, but ratatoskr is 2× slower than Noxim. This is not a result of less performing router or application model. The impact of the application model is very small, as we already evaluated in [21, p. 6], where it was 1/30 of the overall simulation time. Rather, the slower performance is a direct result of the added functionality of the power model for links and detailed buffer usage statistics as for every link in every clock cycle, large data structures are written. This can easily be shown using profiling (using gcc -pg). Thus, our simulator is slower than state-of-the-art but offers more features, but this is an acceptable compromise for the power model accuracy (see below). Second, concerning simulation time for different network sizes, shown in Figure 11, one can see that all three simulators are linearly slower for more routers. Furthermore, the performance difference is constant. This is expected since every router is simulated for each clock cycle. To summarize, our simulator has the same performance as state-of-the-art if one does not account for extended features; the new features reduce performance but allow for better quality of results, as we will discuss in the next paragraph.

The PPA of the router is evaluated by synthesis of the high-throughput router for 45 nm node. The results are shown in Table 2. We report the reduction in router power and area by removing the impossible turns of Z*(XY)Z− routing algorithm [18] and conventional XYZ routing algorithms. The power of the crossbar is reduced by 61% and 65%, respectively. This has a 15% to 17% positive effect of the total router power. The area of the crossbar is reduced by approx. 31%–32%; this reduces the total router area by approximately 3%. The power and area enhancements are not affecting the router’s performance, as the turns in the removed turns in the crossbar had not been taken.

Our used power models are more accurate than conventional models without considering pattern-dependent switching coupling and virtual channels as clearly shown in Tab. 3: The error of our models is 2.4% while conventional models yield up to 42.5% error for a given case study. These very good results are a consequence of the usage of data-flow matrices in the simulator. Therefore, the price of this low modeling error is reduced simulation performance in comparison to conventional models. The data-flow matrices contribute to the 2× reduced simulator performance in comparison to Noxim. However, we strongly advocate this feature. We are convinced that the reduced simulator performance is a price well-paid for the modeling error. The only other viable option to get such good results are bit-accurate simulations. However, those have much worse performance than our data-flow matrices. A trace file of the data transmissions along each link would need to be written. While our data flow matrices have a constant size and a memory complexity of $O(n^2)$, with $n$ colors, generation of bit-accurate trace file has a non-constant size linearly increasing with the simulation time $t$. Since usually the simulation time is much larger than the number of different data streams (i.e. colors) in the application graph ($t >> n$), the performance gain and memory reduction are significant.

|                  | Energy per transmitted flit [pJ] |
|------------------|----------------------------------|
|                  | without VCs ∆ | with four VCs ∆ |
| Baseline: bit-accurate simulations | 2.39 | 4.18 |
| Conventional model (without switching & coupling) | 2.40 | <1% | 2.40 | 42.5% |
| Used model [22]  | 2.40 | <1% | 4.28 | 2.4% |

Table 3. Accuracy of used power models, numbers based on case study from Ref. [22].
For the sake of completeness, we also briefly discuss the router architectures properties. As one can see in Fig. 12, the network saturates after 7% injection rate, which is expected for the chosen, light-weight architecture. Since the focus of this submission is not a novel router architecture but a simulation tool that ships a hardware implementation on top of the actual core simulator, we do not compare against other router implementations.

To summarize, the ratatoskr framework generates more accurate results than state-of-the-art competitors at the cost of slightly reduced simulation performance. Since accurate power results are key in heterogeneous 3D SoC due to layers in mixed-signal technology with a high base power consumption, ratatoskr tackle one of the most important issues. Furthermore, we ship a hardware implementation, which is automatically generated for each simulation run. Since the whole tool uses a single-point of entry and easy-to-use configuration interfaces it is very user friendly and allows for rapid prototyping. In addition, more detailed configuration interfaces are also provided if non-standard parameters are to be set and optimized. Thus, the proposed design and simulation tool allows to efficiently build NoC for heterogeneous 3D SoCs.

9 CONCLUSION

In this work, we introduce ratatoskr, an open-source framework for in-depth PPA analysis in 3D NoCs. We also support heterogeneous 3D integration as it has become one of the key innovations to build more efficient systems. The framework ratatoskr is implemented in C++, SystemC, Python and VHDL. It offers power estimation of routers and links on a cycle-accurate level. The accuracy of our models for the dynamic power of links is within 2.4% accuracy of bit-level simulations while maintaining cycle-accurate simulation speed. The performance of the NoC can be measured on CA level for long simulations using traffic injected from TL-modeled applications or synthetic patterns, on RTL for shorter simulations using synthetic patterns, and on gate-level for router timing. The hardware implementation of the routers can be synthesized for standard cell technologies and includes a power and area saving feature that removes unused turns in the crossbar based on information about the routing algorithm. This saves up to 32% total router power and 3% router area compared to a conventional router without these features. The whole framework evolves around a single configuration file that allows to set the most important design parameters easily, but more detailed and more complex configuration options are also available. The framework generates user reports to assess designs. With this wide range of features, ratatoskr is the first comprehensive framework for PPA-analysis in NoCs also comprising heterogeneous 3D integration. It will participate to tackle important issues for state-of-the-art chips due to the increasing relevance of heterogeneity and the prevalent challenges found in on-chip interconnection networks. You’ll find the source code and usage examples of ratatoskr at https://github.com/jmjos/ratatoskr.

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