ZIPPER: Exploiting Tile- and Operator-level Parallelism for General and Scalable Graph Neural Network Acceleration

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\section*{ABSTRACT}

Graph neural networks (GNNs) start to gain momentum after showing significant performance improvement in a variety of domains including molecular science, recommendation, and transportation. Turning such performance improvement of GNNs into practical applications relies on effective and efficient execution, especially for inference. However, neither CPU nor GPU can meet these needs if considering both performance and energy efficiency. That’s because accelerating GNNs is challenging due to their excessive memory usage and arbitrary interleaving of diverse operations. Besides, the semantics gap between the high-level GNN programming model and efficient hardware makes it difficult in accelerating general-domain GNNs.

To address the challenge, we propose ZIPPER, an efficient yet general acceleration system for GNNs. The keys to ZIPPER include a graph-native intermediate representation (IR) and the associated compiler. By capturing GNN primitive operations and representing with GNN IR, ZIPPER is able to fit GNN semantics into hardware structure for efficient execution. The IR also enables GNN-specific optimizations including sparse graph tiling and redundant operation elimination. We further present an hardware architecture design consisting of dedicated blocks for different primitive operations, along with a run-time scheduler to map an IR program to the hardware blocks. Our evaluation shows that ZIPPER achieves 93.6× speedup and 147× energy reduction over Intel Xeon CPU, and 1.56× speedup and 4.85× energy reduction over NVIDIA V100 GPU on averages.

\section{INTRODUCTION}

Graph neural networks (GNN) start to gain momentum since researchers involve graphs into DNN tasks. By leveraging the end-to-end and hierarchical learning capability of deep learning, as well as the rich structural information of graphs, GNNs achieve better performance in a variety of domains including molecular science \cite{16}, recommendation \cite{13,39}, and transportation \cite{7,8}.

To better unleash the power of GNNs via efficient inference execution, we first perform a thorough analysis of the general GNN design space. We find that GNNs consist of diverse primitive operations, including regular, compute-intensive general matrix multiplication operations from DNNs and irregular, memory-intensive graph operations, such as gather and scatter, from traditional graph processing. As such, systems optimize exclusively for DNNs or traditional graph processing are sub-optimal for GNNs. Meanwhile, the primitive operations can be freely interleaved in general GNN models. As a result, prior GNN accelerators that focus on a particular kind of GNN \cite{2,22,24,34,37} are not generally applicable.

Then we build ZIPPER, an efficient yet general acceleration system for GNNs. The fundamental challenge in accelerating the general domain of GNN is the semantics gap between the high-level GNN programming model and efficient hardware. Today’s GNN programming model \cite{36} is designed to define operations on an input graph as a whole by representing all vertices and edges as tensors. We refer to it as \textit{classic GNN programming model}. Such a programming model makes GNNs similar to conventional CNNs and thus friendly to algorithm designers. But it hides the performance-critical graph structures as well as the vertex- and edge-level operations from flexible execution, losing the opportunity of improving system efficiency.

To bridge the semantics gap, we propose a GNN-aware intermediate representation (IR) and the associated compiler, which together automatically extract the graph-specific semantics (e.g., vertex and edge computational graphs) from classic GNN programming model. The compiler takes a GNN model described in classic popular GNN frameworks (e.g., DGL \cite{36}) and generates an IR program that will later be mapped to the hardware. The IR captures primitive operations from GNNs into an IR program, with its semantics fitting into the hardware structure for efficient execution. More importantly, the informative IR program enables our compiler to perform GNN-specific optimizations such as sparse graph tiling and redundant operation elimination.

Coupled with the compiler, we propose a GNN accelerator architecture to execute GNN IR programs. The accelerator hardware consists of dedicated execution blocks for different primitive operations, along with a run-time scheduler to map an IR program to the hardware blocks. For better performance, the scheduler effectively exploits GNN-specific parallelisms while respecting the dependencies enforced in an IR program. For instance, the scheduler overlaps the execution of tiles (subgraphs) which exercise different hardware resources/blocks to improve hardware utilization.

In evaluation, we compare ZIPPER with Intel Xeon E5-2630 v4 CPU and NVIDIA V100 general-purpose GPU. The experiments results show that ZIPPER achieves 93.6× speedup and 147× energy reduction over the CPU on average. Compared to the GPU, ZIPPER achieves 1.56× speedup and 4.85× energy reductions.

We summarize the main contributions below:
- We perform a thorough characterization on general GNN models today. Our characterizations show that GNN workloads have a mixed set of compute-intensive and memory-intensive operators that do not simultaneously exist in either traditional graph analytics or DNNs.
- We present a GNN IR. It captures primitive operations in GNNs, which is friendly to hardware semantics. The associated compiler automatically converts a GNN model into an IR program while applying GNN-specific optimizations such as tiling and redundant computation elimination.
- We propose an efficient and flexible GNN accelerator architecture. The architecture exploits the parallelisms unique to GNN to maximize hardware utilization, thereby improving execution efficiency. The architecture is also applicable to a broad domain of GNNs.
- We evaluate ZIPPER with detailed experiments and demonstrate average 93.6× and 1.56× speedup with 147× and 4.85× energy reduction over CPU and GPU, respectively.

2. BACKGROUND

GNN models form a large design space, and prior work [15, 37] usually focus on only specific GNN models (e.g., GCN (or graph convolutional network) [25]) and, thus, lack general applicability. Since our work targets generic GNN models, this section describes the general design space of GNN models, emphasizing the common computation primitives.

GNNs extend traditional graph processing with the end-to-end learning capability of deep learning, which has led to better accuracies than the prior hand-crafted or intuition-based methods (e.g., DeepWalk [30] and node2vec [18]) in a wide variety of domains including molecular science [16], recommendation [13, 39], and transportation [7, 8].

Similar to conventional DNNs, GNNs are composed of layers, where a layer $l$ takes as input the vertex and edge embedding matrix along with the graph structure in the form of the adjacency matrix and outputs the new embedding matrix for the layer $l + 1$. Different from DNNs which may consist of a large number of layers, GNN models only have a few (usually less than five) GNN layers.

Capturing GNN Design Space. Owing to the end-to-end learning capability of GNNs, algorithm researchers have explored a wide variety of different GNN models, leading to an enormous model space for GNNs [40].

While the GNN design space is vast, computations in GNN can be abstracted as two main kinds of operations [36]: 1) graph operations (GOP) and 2) neural-network operations. The latter could be further classified into either general matrix multiplication (GEMM) or element-wise (ELW) operations. These three operations (GOP, GEMM, ELW) cover all forms of computation in GNNs. This abstraction is described in a widely-used GNN library DGL [36], and also shared by other libraries such as PyG [14] and NeuGraph [27].

We now briefly describe these three operations and show how they are used with concrete GNN models.

Graph Operations. There are two graph operations in GNNs: scatter and gather. Such two operations can be considered as vectorized graph propagation operations in traditional graph processing (c.f., GAS [17] for graph processing).
- The scatter operation distributes the embedding of each vertex to its outgoing (or incoming) edges.
- The gather operation collects and reduces the embeddings of all the incoming (or outgoing) edges of each vertex to a fixed-length vertex embedding. The specific reduction function is user-defined, and aligns vertices’ embedding for subsequent operations despite different edges.

General Matrix Multiplication Operations. GNNs use neural network (NN) operations such as MLP [28] and RNN [11] to transform vertex and edge embeddings. These NN-based operations are important to GNNs as they enable the learning ability on the graph. Since there is no dependency among vertices and edges, these NN operations can be performed in parallel, which is essentially general matrix multiplication.

Element-Wise Operations. GNNs also use element-wise (ELW) operations to transform vertex and edge embeddings. Common ELWs include add, exp, and RELU. ELW operations on different vertices and edges can also be executed in parallel. While an ELW operation is less compute-intensive than a GEMM, GNNs can spend a significant portion of time on ELWs owing to their quantity as we show later.

Examples. We take a layer from two popular GNN models, GCN [25] and GAT [35], respectively, as examples to illustrate how we can express GNNs with such primitive operations. Figure 1 shows each layer’s computation graph implemented in the DGL [36] library, where $F$, $V$, and $E$ represent the embedding size, vertex number, and edge number of the input graph, respectively. We annotate the three primitive operations in the figure. The GCN model in Figure 1a show is relatively simple. In contrast, the GAT model in Figure 1b shows much more complex computation patterns. The mixed operation types also show the complexity and operation diversity of GNNs.

3. MOTIVATION

A GNN model by nature is a flexible combination of DNNs and graph processing. Diverse characteristics of DNNs and graph processing introduce great expressiveness but also make it challenging for accelerating computation. In this section, we first study the characteristics of the GNN workloads against the well-studied DNN models and traditional graph processing algorithms on GPU architecture. We find that the existing solutions suffer from inefficiency problems due to GNN’s diverse characteristics. We then study the root cause at both architecture and software level, and propose a solution with co-design of software and hardware.
We compare and contrast GNNs against DNNs as well as traditional graph processing algorithms to understand GNNs’ common and unique properties. Specifically, we start our study from two representative GNN models, GAT [35] and GraphSAGE (SAGE) [20], two DNN models, VGG [33] and ResNet (RN) [21], and a traditional graph processing workload PageRank (PR) [5]. GNNs and traditional graph processing algorithm are evaluated on three datasets (Table 3): DNNs are evaluated on ImageNet [10] with batch size of 256.

We identify two opportunities for optimizing GNNs.

**Observation 1:** GNNs exhibit much higher memory usage than DNNs and traditional graph processing. As a result, it’s hard to efficiently scale GNNs to large graphs.

Specifically, Figure 2 compares the memory usage of different algorithms on a NVIDIA V100 GPU with 32 GB memory. On the dataset SL, the GNN GraphSAGE uses 16.3 GB of GPU memory, while PageRank on the same dataset uses only 3.7 GB and VGG16 with ImageNet under batch size of 256 uses 6.9 GB. We also observe a similar trend on dataset CP.

The excessive memory usage prevents GNN models from processing large graphs. Figure 2 shows that when using a large graph EO, which consists of 10.5× more vertices and 1.2× more edges than SL, both GNNs GAT and GraphSAGE run into the out-of-memory issue.

To understand the excessive memory usage, we further break down the memory usage into four components: the graph data, the weight matrices, the input/output feature embeddings, and the workspace, which refers to the intermediate data between operations. We observe that GNNs use a significant portion of memory for storing the intermediate data. This is fundamental because classic GNN systems operate on an entire graph within one operation.

**Observation 2:** Due to irregular nature of graph, similar to traditional graph processing, GNNs also show lower hardware utilization than CNNs. However, GNNs mix diverse primitive operations, which requires different types of hardware resources. It provides a unique optimization opportunity by redistributing the hardware resource while overlapping different operations.

**Primitive Operation Diversity** Figure 3 plots how the single-precision FLOP efficiency and the DRAM bandwidth utilization change over time for the four algorithms – all on a V100 GPU. These two metrics capture key computational and memory behaviors of an algorithm. The data is obtained from one iteration of PageRank and a layer in the GNN and DNN models. At the top of each figure, we annotate which primitives operation (i.e., GEMM, ELW, and GOP in Section 2) dominates an algorithm at a given moment in time.

GNNs exhibit a much more diverse mix of primitive operations than traditional graph processing and CNNs. GOP dominates the execution of PageRank, while GEMM and ELW dominate the execution of VGG. In contrast, all the three primitive operations exist in GNNs; the interleaving of the three operations varies by GNN model.

It is worth noting that prior GNN accelerators [15,22,24,37,41] target only one particular type of GNN called GCN (graph convolutional network), which has a fixed primitive operation interleaving of GOP-GEMM-ELW as shown in Figure 1a. A general GNN would be much more complex than GCN in model structure, as GAT shown in Figure 1b, which has a much more complicated primitive operation mixing and interleaving.

**Low Hardware Utilization** Because of the primitive operation diversity, GNNs tend to have lower hardware utilization than CNNs. As a result, accelerators built for CNNs are ill-suited for GNNs. We annotate in Figure 3 the average FLOP efficiency and DRAM bandwidth utilization for each algorithm. The FLOP efficiency on both GNNs is at least 35% lower than that of VGG; the DRAM bandwidth utilization of both GNNs is also lower than that of VGG.

A close examination of the GNN execution shows the reason. CNNs primarily rely on GEMM, which has high FLOP efficiency and high DRAM bandwidth utilization due to its regular compute and memory access patterns. GNNs mix regular GEMM kernels and irregular GOPs used in traditional graph processing (e.g., PR), which has low FLOP efficiency and DRAM bandwidth utilization due to its irregular compute and memory access patterns. As a result, GNNs tend to have lower hardware utilization than CNNs.

### 3.2 Inter-tile Pipelining

Our main idea is to exploit the operation diversity in GNNs and pipeline the operations to reduce memory footprint while improving hardware utilization. Figure 4 illustrates the idea of a simple GNN with three primitives operations.

Figure 4a illustrates how GNNs are executed on today’s system, where the three operations are sequentially executed as three serialized stages, each operating on the entire graph. The intermediate data between stages encodes information for the entire graph, leading to a large memory footprint. In addition, the serialized execution leads to long execution times with low hardware resource utilization.

A common strategy to reduce the memory footprint is graph tiling [42], which partitions a graph into smaller subgraphs, a.k.a., tiles, and operates on each tile separately. Figure 4b illustrates such an idea, where the entire graph is divided into three tiles. The three tiles are processed sequentially, which reduces the memory footprint since at any given moment only a small subgraph is resident in memory.

However, this strategy degrades performance due to the bookkeeping overhead such as setting up and switching tiles. In addition, it does not address the low hardware utilization, as at any given moment only one operation is executed.

We propose to pipeline across tiles, as illustrated in Figure 4c, which retains the advantage of low memory footprint while significantly improving the performance. By pipelining
across tiles, operations of different tiles are overlapped and executed at the same time. Overlapping operations exercise different resources, improving the overall resource utilization and therefore leads to better performance.

3.3 Challenges of Inter-tile Pipelining

Applying tile-level pipelining to GNNs is challenging for two reasons. First, there is a semantics gap between the classic GNN programming model and efficient hardware execution. In particular, tile-level pipelining requires us to identify the operations associated with each tile, including its vertices and edges. But classic GNN programming model is designed to define operations on a graph as a whole without exposing vertex- and edge-level operations. This is accomplished by representing all vertices and edges as tensors. This programming model thus expresses GNN execution as tensor computations, similar to conventional CNNs. Figure 5 shows such an example from the GNN library in PyTorch, where the bold boxes show how the vertices and edges are represented as tensors and the GNN execution is represented as tensor computation without exposing graph semantics.

While this programming model makes GNNs similar to conventional CNNs and is thus friendly to GNN algorithm designers, it also hides vertex and edge-level details that are vital for efficient hardware execution.

Second, GNNs adopt a wide variety of different operations. Therefore, one must flexibly schedule a GNN to the hardware. For instance, the GCN and the GAT in Figure 1 are drastically different. A static, fixed mapping from a GNN to the hardware is likely suboptimal in utilizing the hardware.

4. ZIPPER OVERVIEW

In this work, we propose a hardware and software co-designed system that exploits the tile- and operator-level parallelism to provide efficient and scalable support for generic GNN acceleration. ZIPPER overcomes the challenges of inter-tile pipelining in Section 3.3 through a combination of software GNN compiling and hardware GNN architecture. Figure 6 shows an overview of the ZIPPER system.

First, ZIPPER proposes a GNN intermediate representation (IR) and the associated compiler, which together automatically extract the graph-specific semantics (e.g., vertex and edge computation graphs) from classic GNN programming model. The IR is closer to the hardware, and enables an efficient hardware accelerator design and scheduling.

Second, ZIPPER proposes an accelerator architecture for executing GNN models represented as IR programs. The key to the hardware is to be flexible enough to accommodate different types and mixes of the primitive operations while being efficient by exploiting GNN-specific parallelisms and locality. The hardware achieves this by employing dedicated blocks for each primitive operation coupled with an efficient run-time scheduler, which maps GNN IR programs to the hardware substrate.

IR and Compiler The proposed IR is structured as multiple directed acyclic graphs (DAG) extracted from a GNN model. Each graph is labeled as a vertex segment or an edge segment, where the DAG nodes are the GNN operations for a single vertex or an edge while the DAG edges are the data of the vertex or edge. The IRs are meant to be used by the compiler, which compiles the GNN model into a low- and tile-level program consisting of three functions for the source vertices of tiles (sFunction), the edges of the tiles (eFunction), and the destination vertex of partitions (dFunction), respectively, under the tiling-based execution semantics to specifies the
tile data dimensions as well as the interactions between the vertices and edges. We refer to the three functions as SDE functions for simplicity.

**Hardware Architecture** The hardware consists of two main components: the building blocks to support various primitive operations execution and a scheduler that dispatches GNN tiles to the hardware blocks.

The hardware blocks consist of both generic matrix and vector units to support GEMM and ELM operations, respectively, as well as graph-specific structures that are optimized for GOP. The scheduler generates independent work units for source vertices and edges in tiles and destination vertices in partitions, which we call sStreams, eStreams and dStreams. The streams are then pipelined efficiently across the hardware blocks to achieve high utilization.

5. **GNN PARALLELIZATION**

In order to exploit the inter-tile pipelined execution opportunity, we first describe our graph tiling method and a generally applicable strategy to parallelize GNN models.

5.1 **Graph Tiling**

The fundamental building block in our proposed system is graph tiling (also called partition or sharding), which divides an input graph into smaller sub-graphs, a.k.a., tiles. The benefits of graph tiling are two-fold: easing the pressure of excessive memory footprint of GNN computation and exposing tile-level parallelism that ZIPPER leverages (Figure 4).

We adopt a tiling strategy called grid-based or regular tiling [24, 27, 42]. The idea is to divide the graph adjacency matrix into multiple smaller rectangles as tiles. Figure 7b illustrates the grid-based tiling example. Formally, we first split the vertices evenly into several destination partitions according to their vertex IDs. For each destination partition, we further split its vertices into several source partitions according to their vertex IDs. As a result, each tile corresponds to exactly one destination and one source partition and uniquely identifies a set of edges whose source and destination vertices are in the corresponding partitions.

Owing to the sparsity in the graph, the adjacency matrix for the tile that indicates connections between edges and vertices is stored in a sparse format such as edge list (COO) or compressed sparse column (CSC) for saving the storage [6]. While the tile metadata such as the edge and vertex numbers are usually stored in a dense array.

5.2 **Multi-streamed Execution**

Based on the above grid-based graph tiling, we propose a generally applicable parallel execution mechanism for GNN models which are combinations of GEMM, ELM, and GOPs.

We first need a multi-streamed parallel execution mechanism that supports fine-grained inter-stream synchronization via a signal-wait pair. The idea is to map the computation of concurrent tiles to different streams and insert proper synchronization instructions to maintain the dependency from the original GNN model.

The key for this mapping is the Gather operation. This operation is applied to all the tiles under the same partition to reduce the embeddings of all the edges and source vertices for each destination vertex. As such, all the operations that depend on the result of the Gather operation need to wait for all tiles in the same partition. In the meantime, the operations that do not depend on the Gather operation can be executed in parallel.

Following the above principle, we propose to use multiple streams for the concurrent tile computation and a single stream for the partition computation. We call the former as sStreams and eStreams, processing the source vertices and edges in tiles respectively, and the latter as dStream for the destination vertices in partitions. The reason that the number of s/eStreams is greater than the number of dStream is that there can be many tiles for the same partition.

Figure 6c-bottom shows an example of streams. The dStream first processes the embedding of a partition until it reaches the signal and wait instructions. The signal instruction wakes up two sStreams, which starts to load and process a tile under the partition. The sStream ends up with a signal to wake up an eStream and continue the tile process. When the eStream reaches the end, it fetches the metadata of the next tile and checks whether the destination partition is the current one. If true, the eStream starts a new round of s/eStreams through the signal and wait instruction; or it re-
Figure 7: Comparison of different graph tiling methods. The vertices in (c) are arranged in descending order of their in-degrees. The maximum of the source and destination vertices in a tile is 4 and 6 respectively.

5.3 Tile Parameter Optimization

Although the tiling-based pipelining reduces the memory footprint of the GNN computation, the large amount of tile vertex data loaded and computed without contributions to the final results because of the graph sparsity. Figure 7a illustrates this problem where the source vertex without an edge in a tile causes redundant memory access and computation. For example, in tile 1 (the top left one), vertex 3 is included in the tile and thus loaded to the on-chip memory. However, this vertex will be only computed as an edge source and the result will not be propagated to any edges or destination vertices because it does not have any associated edges. So the on-chip memory load, as well as the associated computation of such vertices, are unnecessary in this tile.

Sparse Tiling. We use the sparse graph tiling approach [27] that embraces the graph sparsity to remove the above unnecessary processing. As illustrated in Figure 7b, only the source vertices that have associated edges in the tile are kept. Usually, traditional graph processing systems, e.g., [31], prefer regular tiling to sparse tiling. It is because their vertex/edge features are scalars. Applying sparse tiling would turning efficient sequential off-chip memory access into much more expensive random access on small-size scalars, leading to lower overall performance even skipping unnecessary vertices. However, the vertex/edge features in GNN are high-dimensional embeddings, much larger than the scalars and each of them can be translated into multiple off-chip memory transactions, which can match the bandwidth of sequential access while avoiding unnecessary processing.

Graph Reordering. The improvement of the sparse tiling is limited yet because of the random vertex distribution. As shown in Figure 7b, we can observe that most source vertices only have a few (mostly one) edges to the destination partitions in a tile, which less than their out-degrees. As such, there is an opportunity to gather the out-edges of the source vertices into a few tiles to further reduce the redundancy and improve vertex data reuse.

We leverage graph reordering to fulfill such an opportunity, which makes minimal modifications to the existing system design. There are lines of sophisticated graph reordering in traditional graph processing, but only the lightweight methods are effective considering the limited performance improvement [4, 12]. In contrast, applying the reordering to GNN can lead to considerable performance improvement, because the data volume and computation for a vertex is much more than that in traditional graph processing. We use a heuristic Degree Sorting strategy that reorders the vertices according to their in-degrees as shown in Figure 7c to illustrate the effectiveness of reordering for GNN. The vertices with high in-degrees are arranged to the left side so there are more blank rows on the right side for the sparse tiling. As a result, the total source vertex load is reduced.

6. GNN IR AND COMPILING

ZIPPER automatically compiles a high-level GNN model expressed in classic GNN programming framework (e.g., DGL [36]) to the tile-level program that is scheduled and executed as streams on our hardware substrate. As we have explained earlier, the classic GNN programming model is centered around tensor computation and does not expose edge and vertex level operations. To bridge the semantics gap, we propose a graph-semantics-preserving IR that is used by the compiler to generate the SDE functions mentioned in Section 5. An end-to-end illustration of the compiling process is depicted in Figure 8, and we first introduce the IR with the corresponding compiling process, and then discuss performance optimizations based on the IR.

6.1 Graph-Native GNN IR

We propose Graph-Native GNN IR that contains multiple computational DAG segments. Each segment is labeled as an edge or vertex segment, and consists of IR operations as nodes that operate the data of a single edge or vertex. Figure 8b shows two examples.

Table 1 lists a subset of the IR operations in ZIPPER, which are designed to represent all three types of primitive operations (Section 2). In particular, the computational operations correspond to the GEMM and ELW operations in general DNNs, while the communicational operations correspond to the GOPa that exchange data between vertex and edge. All the IR operations target only one item (i.e., single edge or vertex) for graph semantic atomicity. The IR connects the high-level programming model by using compatible computational graphs and operations in the DNN, while it recovers the graph semantics by operating on a single edge and vertex with decoupled computational graphs.

Compiler. We build a compiler to automatically translate the existing GNNs expressed via the high-level programming model to our proposed IR. The compiler then uses the generated IR to produce the SDE functions, which are eventually mapped to the hardware streams to exploit tile-level pipelin-
ing. For a given GNN model, the compiler generates the functions in three steps, as illustrated in Figure 8.

**Step 1: Constructing the IR with graph semantics.** The compiler extracts a generalized GNN computational graph to capture the nature of the given GNN model. Specifically, it first acquires the raw computational graph from the standard DNN programming frameworks such as TensorFlow and PyTorch, then defuses and replaces the library-customized DOPs into atomic ones (i.e., Scatters, Gather). We achieve that by maintaining a list of operations according to the library implementations, for example the apply_edges / update_all in DGL and the Scatter in PyG.

Afterward, the compiler splits the computational graph into multiple segments as the graph-native IR to reveal the graph semantics. Because the tensor types (e.g., tensor for edge or vertex) are changed only by the DOPs, the compiler simply splits the model by replacing each DOP with a pair of IR computational operations send and recv as annotated by the red solid boxes in Figure 8. The output is multiple disconnected GNN model segments, and the compiler then labels the segments with graph semantics based on the computational operations. For example, a segment containing sendOutEdge will be labeled as \(IR_{v.x}\) where the \(x\) denotes the segment index. The compiler finally maps the rest computational operations to the corresponding single-item operations (i.e., operations for a single edge or vertex). It also inserts input and output markers for the whole IR as the entry and exit indicators to finish the IR construction.

**Step 2: Optimizing the structure of the IR.** The proposed graph-native GNN IR not only supports the existing optimizations in deep learning, but also enables the GNN-specific optimizations. The node and edge in our IR segments represent the operator and feature embedding, which is highly similar to the deep learning computational graph. So the existing optimizations in deep learning, e.g., subgraph substitution and operator fusion, are fully applicable to our IR. Besides, the supplementary of the graph semantics enables the space to explore the GNN-specific optimizations, which involves both the computational graph and the input graph. We further propose such an optimization based on our IR and we detail it in Section 6.2.

**Step 3: Generating SDE function code.** Before translating the optimized IR into functions of the instruction sequences, we first adapt the proposed general IR according to the low-level hardware execution model. In this paper, we target the tiling-based execution model (Section 5.2), so we need independent and separate sFunction and dFunction for the processing of source and destination vertices under a tile and a partition, respectively. We obtain the functions by further dividing the vertex segments into source and destination parts as illustrated in Figure 8c. The compiler first replicates the vertex segments, and then prunes the operations unrelated to the source or destination semantics from each replica.

Given the adapted IR, we generate the instruction SDE functions using the hardware ISA that we describe later. The source, destination, and edge segments target the sFunction, dFunction, and eFunction, respectively. For each segment, we sort it topologically from the input markers. The input and output markers are translated into data-transfer instructions; the computational and send operations corresponds to the computational instructions; the recv operations are regarded as barriers for the synchronization instructions to ensure the multi-stream execution semantics.

Since the proposed IR can be multiple disconnected segments as in Figure 8, the sorting can be deadlocked, which implicates the interaction between the segments. For the deadlock in a destination segment, the compiler inserts the update, signal, and wait instructions, and resumes the sorting by removing the recv operations in the next source or destination segment; for the deadlock at the end of a source segment, the compiler inserts the signal and wait instructions, and resumes the sorting by removing the recv in an edge segment; for the deadlock at the end of an edge segment, the compiler checks whether there are still unvisited segments: if true, it simply removes the recv in one unvisited segment and resumes the sorting, or it ends the IR translation to finish the function generation.

**Instruction Set Architecture (ISA).** We propose ZIPPER ISA with three types of instructions: computational, data-transfer, and synchronization instructions as shown in Table 2. The computational instructions are supposed to cover all the operations of GEMM, ELW and GSP appeared in the model computation. Each of the instructions is coarse-grained and operates on all the edges or vertices in a tile to improve the performance. The ELW instructions also have matrix and vector versions aiming at different use cases. The data-transfer instructions are designed for loading and storing the embed-
Table 2: The details of ISA for the ZIPPER architecture.

| Instruction Type | Examples                                                                 | Operands                          |
|------------------|--------------------------------------------------------------------------|-----------------------------------|
| ELW              | arithmetics (ADD, SUB, MUL, DIV), special functions (EXP, RELU), matrix-vector multiplication (GEMV) | data dimensions, source and destination addresses of embedding memory |
| GEMM             | general matrix multiplication (GEMM), index-guided batched matrix multiplication (BBM)   | tile id, data dimensions, source and destination addresses of embedding memory |
| GOP              | edge gather (GTHR. DST, SRC, GTHR. DST, MAX), vertex scatter (STL. OUTE, STL. INE) |                        |
| Data-Transfer    | off-chip memory load (LD. DST, LD. SRC, LD. EDGE), store (ST. DST)          | tile id, data dimensions, destination address of embedding memory         |
| Synchronization  | stream wakeup (STWAKUP. E), fetch new tile / partition ID (FCH. TILE, FCH. PTT), update (UPD. PTT), check (CHK. PTT) | stream ID |

ings of the edges and vertices. They are also coarse-grained in the tile level and can be further divided into multiple off-chip memory transactions according to the protocol. The synchronization instructions perform inter-stream synchronization and ensure the correct execution order.

6.2 IR-Based Compiling Optimization

The graph-native IR also provides a wide optimization space for GNN model in addition to generating the low-level code. Optimizations from both traditional deep learning and graph processing such as graph substitution and operation fusion, forming GNN-specific optimizations, can be automatically applied by compilers through the IR. We propose edge-to-vertex (E2V) optimization to demonstrate how the IR can be used for GNN model optimization.

The idea of E2V is to move an operation on edge to the vertex if the operation input only involves the source or destination of the edges. For example, we can move the two matrix-vector multiplications (MVs) to the vertex segment in Figure 8b as the edge-to-vertex optimization. Because the nature of one vertex relates to multiple edges, the data scattered to edges will be the same as the source or destination vertex data. If now an operation applied to the edges uses only the source or destination data, the results would also be the same. So this operation causes redundant computation.

To detect and eliminate such redundancy, we apply the operation before the data are scattered to the edges. We first detect the redundancy by traversing and examining the operations in the edge segment from the recv. Operations that use only the source or destination are enqueued. When an operation does not satisfy the condition, we move the operations in the queue ahead of the corresponding send in the vertex segment. Finally, we insert extra send-recv pairs for the moved operations whose results are still used in the edge segment, and restart to examine the next recv. In fact, the E2V optimization can be also applied to original computational graphs, but it may complicate the implementation and incur several unnecessary traversals on the whole graph.

7. HARDWARE ARCHITECTURE

To support the diverse primitive operations and inter-tile pipelining in GNN computation, we design a flexible hardware substrate, as shown in Figure 6. Generally, we deploy two types of computing units for the primitive operations and launch multiple streams concurrently for the inter-tile pipelining due to the interleaving nature of operations which uses different computation resources in GNN computation. The streams are created and maintained by a hardware scheduler, which feeds the instructions of the ready stream to the downstream dispatcher. The dispatcher decodes and issues the incoming instruction to the target components for the execution. We also design a tile hub and a unified memory for storing the edge list and embeddings of the tiles being processed by the streams.

7.1 Hardware Component

In the ZIPPER architecture, we deploy a set of computing units and various memory structures. We later perform a design space exploration (i.e., the number of computing units and memory structure parameters) for justifying our choices.

Computing Unit. Two types of computing units are deployed for different primitive operations (Section 3.1): Matrix Unit (MU) and Vector Unit (VU). The MU is a single systolic array including a weight buffer for the GEMMs. It executes with output stationary dataflow [9] where the input embeddings and weight are feed to the unit at the same time. The VU is a group of single-instruction-multiple-data (SIMD) cores for the ELWs and GOPs. The reason for offloading GOPs to the VU instead of another dedicated component is that the atomic operations in GOP are also element-wise with only the operands determined by the tile edge list. For executing the GOPs, each core is responsible for scattering or gathering one vertex in the tile at a time and fetches the corresponding part of the edge list. Both the MUs and VUs can be instantiated to have multiple instances to increase parallelism.

Memory. The on-chip memory consists of two parts: 1) a large unified embedding memory (UEM) for storing the input, intermediate and output embeddings of edges and vertices, and 2) a small tile hub (TH) for the graph tiles containing the edge list and other metadata such as the edge and vertex numbers of the tile. Owing to the large size of embeddings, we use eDRAM as the UEM. The eDRAM has multiple banks and connects directly with all the computing units to support the multi-streamed parallel execution. For the TH, we use a small dedicated on-chip SRAM, since the edge lists are accessed more frequently and randomly. The new data will be loaded to the TH when an eStream finishes tile. For the interaction between the on-chip and off-chip memory, we design a memory controller that responds to the data-transfer
instructions, where the vertex (tile) request is converted to the off-chip memory transactions according to the vertex ID and embedding size (the address and size of the previous tile).

7.2 Scheduling
The ZIPPER hardware uses a two-level scheduling, which exploits both the tile-level parallelism (TLP) and the operator-level parallelism (OLP) with streams. Recall that a stream executes the SDE functions generated from the GNN model on a tile. We implement it as a group of registers that represent its state.

The first scheduler creates and manages the streams for the pipelined execution. It adopts a simple first-ready-first-serve policy for scheduling different streams. When a stream is ready, the scheduler fetches and feeds the current instruction to the input queue of the next level dispatcher, and switches stream state to issued. If the dispatcher queue is full, the schedule will stall.

The second dispatcher is responsible for decoding and issuing the incoming instructions from the scheduler. It also bookkeeps the state of each computing unit. For a computational instruction, the dispatcher will find a target unit that is ready to issue the instruction. If all the target units are busy, the instruction will be added to an instruction queue until the previous instructions and a target unit finish. We set the queue size to the maximum stream number to avoid congestion. For a data-transfer and synchronization instruction, the dispatcher will issue the instruction back to the scheduler for state update and to the memory controller for transaction generation, respectively.

8. EVALUATION
In this section, we present the evaluation results for ZIPPER. We first explain the evaluation methodology and then present the detailed performance results.

8.1 Methodology
Benchmark Datasets and Models. The details of the selected datasets can be found in Table 3. We also select five popular and diverse GNN models for the evaluation.

- GCN [25] is the most famous but simplest GNN model that bridges the gap between spectral- and spatial-based approaches. It consists only of a pair of Scatter-Gather (also known as a SpMM) and a GEMM.
- GAT [35] extends the GCN with a multi-head attention mechanism, involving multiple ELWs and GOPs. We only use one head in our evaluation for simplicity.
- SAGE [20] generalizes GCN with different aggregator, from which we choose maxpool in our benchmark.
- GNN [26] employs a gated recurrent unit (GRU). We implement the GRU with separate ELWs and GEMMs on ZIPPER, but leverage the GRUCell kernel on GPU.
- R–GCN [32] introduces the GCN to the graph with multiple edge types, which correspond to different weights in the GEMM. We set the type number to 3 and randomly generate the edge type for each benchmark graph.

We run the forward pass of a single layer of each model under a typical 128 for the input and output embedding sizes in all experiments, but it is also straightforward for our accelerator to run different layers and embedding sizes.

System Configuration. Table 4 shows the system configuration, where the baseline is DGL 0.5 on one NVIDIA V100 GPU with 32GB memory and two Intel Xeon E5-2630 v4 with 256GB memory, respectively. For ZIPPER, we use a 32 × 128 systolic array as a MU, and eight 32-wide as a VU. Intuitively, we deploy one dStream, four sStreams and four eStreams on top of one MU and two VUs in ZIPPER. We explore the design space of the streams and computing units later in Section 8.3.

8.2 Detailed Results
Performance. Figure 9 shows the performance speedup over
the baselines. We observe that ZIPPER outperforms the CPU and GPU, achieve $93.6\times$ and $1.56\times$ speedup on average, respectively. In the meantime, ZIPPER is able to process the large graph datasets and achieves the highest speedup over CPU because of the application of graph tiling. In contrast, GPU processing the graph as a whole is limited to its off-chip memory size and issues the out-of-memory error. We also observe limited speedup and even slowdown for GAT. This is because DGL has their special operation support for the softmax attention in the GAT while we implement it with ordinary instructions. Besides, the dataset HW is much denser than others, so there is less sparsity to exploit and makes the sparse tiling strategy less effective. Nevertheless, ZIPPER still achieves considerable speedups on the other four models.

**Energy.** Figure 10 shows the total energy reduction of ZIPPER over the baseline CPU and GPU. We observe that the energy consumptions of the CPU and GPU are $147\times$ and $4.85\times$ that of ZIPPER on average, respectively. This is not surprising since we leverage multiple dedicated computing units for the different GNN primitives, while the GPU and CPU spend excessive hardware resources to flexibly support various workloads. Besides, the sparse tiling and reordering also reduce a large number of redundant accesses to both the on-chip and off-chip memory, which takes a large part of the energy consumption.

**Area.** Table 5 presents the area breakdown of the ZIPPER architecture except for HBM. The overall area of ZIPPER is 53.58 mm$^2$, which is down to 6.57% of the baseline GPU die size. The on-chip memory (including the unified embedding memory and the tile hub) consumes 97.91% area of the ZIPPER, and the computing units (including one MU and two VUs) consume about 2.09% area.

| One MU | One VU | Embedding Mem. | Tile Hub | Total |
|--------|--------|----------------|----------|-------|
| Area (mm$^2$) | 1.00 | 0.06 | 52.31 | 0.15 | 53.58 |
| Percentage | 1.86% | 0.12% | 97.63% | 0.28% | 100% |

### 8.3 Optimization Effectiveness

![Figure 10: ZIPPER energy reduction over the baselines.](image)

We analyze the effect of each optimization in ZIPPER.

**Sparse Tiling and Reordering.** We compare the off-chip memory read and execution latency with different tiling strategies: regular tiling, sparse tiling, and sparse tiling with reordering. Figure 11 shows the results on CP while the results also follow the same trend on other datasets. We can observe that the two sparse tiling methods provide $58\times$ and $123\times$ of memory access reduction on average. The lower reduction of GAT, SAGE and GGNN is because they also access the destination vertex embeddings, which cannot be reduced.

Besides, the tiling methods also achieve $48\times$ and $135\times$ speedup on average over the regular tiling. The reason for the low speedup of GGNN and RGCN is that the two models involve edge-type-guided batch matrix multiplication, which suffers from a long latency of on-chip memory access and dilutes the benefit of memory access and computation reduction. But in general, the sparse tiling with reordering can effectively reduce memory access and improve performance.

**Compiling Optimization.** We evaluate the compiling optimization effectiveness by comparing the optimized and the naive implementation of the same GNN models. Figure 12 shows the speedup results of GAT and SAGE, which we find the opportunities for the compiling optimization. But libraries have optimized the models manually because of their high popularity. So we just implement a naive but straightforward version of the same models using DGL. GAT and SAGE achieves $1.87\times$ and $1.03\times$ speedup, respectively. Our optimization also works on the baseline V100 GPU with DGL and achieves a speedup of $2.36\times$ and $1.62\times$.

**Multi-Stream on Hybrid Architecture.** We evaluate different design choices by changing the numbers of s/eStreams, MU, and VU. Figure 13 shows execution latencies normalized to the result of each model with two s/eStreams, one MU, and two VUs, where we make two observations. First, there is usually a sweet point of the s/eStream number. While we increase the s/eStream number, the performance first increases but then decreases with at most $1.72\times$ speedup. But the sweet points usually vary between models and architectures.
Second, models have different sensitivity to different computational units. For example, the speedup of GAT changes with both VU and MU, while that of SAGE only changes with MU. This is because of the different model definition, where the SAGE have much more dense GEMM requiring the MU.

8.4 Comparison with HyGCN

We also compare ZIPPER with the current state-of-the-art GCN accelerator HyGCN [37]. To ensure a fair comparison, we use four datasets: Cora, Citeseer, Pubmed and Reddit, and run a full two-layer GCN on ZIPPER as described in HyGCN. We also compare the baseline CPU and GPU with PyG [14] under the same configuration.

Figure 14 depicts the results. In the end-to-end comparison, ZIPPER outperforms HyGCN in both latency and energy for all the cases. We also disable the software reordering to only compare the hardware with HyGCN, and find that ZIPPER performs a bit worse than HyGCN but still better than PyG-GPU. The reason, in addition to the different technology node, is that HyGCN owns a two-stage pipeline specialized for the GCN model, while ZIPPER breaks it for better flexibility to support more general GNNs such as GAT and RGCN.

9. RELATED WORK

The growing scale of graph data and the wide use of GNNs have driven the development of GNN-specific hardware.

GNN Accelerator. Most GNN accelerators combine the different components with an efficient but fixed pipeline structure. HyGCN [37] is the first to design a hybrid architecture with two-stage pipeline for the irregular and regular computation in GNN. However, it only focuses on the GCN-like models, which are only a small portion of GNNs. GReTa [24] and GNNerator [34] extend the pipeline with one more component and bidirectional dataflow, respectively. GraphACT [41] and ReGraphX [2] also take CPU and 3D ReRAM techniques into consideration for accelerating the GNN training. However, those works are still built or optimized for only a specific class of the real-world GNN models since they do not change the nature of the fixed pipeline structure.

In contrast, Auten et al. [3] connect all the components with a crossbar switch in a hardware block to make it possible to support general GNN models from the hardware aspect, which is the closest work to ours. However, they miss the key information of how a GNN model as well as the input graph is mapped to and executed on the hardware. Besides, their distributed block topology potentially limits the DNN component and bandwidth to take their full advantage, and leads to poor performance on large datasets. Instead, our architecture supports arbitrary GNN models through the graph-native GNN IR compiler and flexible hardware scheduling. Meanwhile, our optimizations for the graph tiling and model compiling also improve the overall performance, which is a complete solution for the general GNN acceleration.

SpMM Architectures. EnGN [22] proposes a unified SIMD architecture where they adopt a ring-based dataflow for SpMM to improve hardware utilization. AWB-GCN [15] proposes three auto-tuning techniques based on a special SpMM unit to address the issue of workload imbalance in GNNs. In a word, these works focus on the irregularity issues in GAT operation, which are inherited from traditional graph processing. They are orthogonal to our work since we focus more on the inter-tile pipelining, and are applicable to our Vector Unit for executing the GOPs in the GNN models.

10. CONCLUSION

In this work, we propose ZIPPER, a general and scalable GNN acceleration system that implements the inter-tile pipelining to exploit the tile- and operation-level parallelism. We first characterize the GNN computation and identify two main problems: excessive memory footprint and GNN primitive operation interleaving. These two problems motivate the idea of the inter-tile pipelining. We first leverage the graph tiling to address the problem of the excessive memory footprint and then pipeline the resulted tiles through a tiling-based multi-stream execution model. However, because of the graph semantic unawareness of the high-level GNN programming model, which is inherited from the traditional DNN frameworks, it is non-trivial to do the GNN model conversion from the programming model into our execution model. So we further propose the GNN Intermediate Representation (IR) and the associated compiler to recover the graph semantics and generate the low-level programs automatically. Finally, we provide architectural support for the tiling-based multi-stream execution, which leads to the ZIPPER architecture. We also propose two optimizations based on graph tiling and compiling to improve the The proposed system achieves 93.6× speedup with 147× energy reduction and 1.56× speedup with 4.85× energy reduction over CPU and GPU solution on average.
[33] Karen Simonyan and Andrew Zisserman. Very deep convolutional networks for large-scale image recognition. In Yoshua Bengio and Yann LeCun, editors, 3rd International Conference on Learning Representations, ICLR 2015, San Diego, CA, USA, May 7-9, 2015, Conference Track Proceedings, 2015.

[34] Jacob R. Stevens, Dipankar Das, Sasikanth Avancha, Bharat Kaul, and Anand Raghunathan. Gnnerator: A hardware/software framework for accelerating graph neural networks. CoRR, abs/2103.10836, 2021.

[35] Petar Velickovic, Guillem Cucurull, Arantxa Casanova, Adriana Romero, Pietro Liò, and Yoshua Bengio. Graph attention networks. In 6th International Conference on Learning Representations, ICLR 2018, Vancouver, BC, Canada, April 30 - May 3, 2018, Conference Track Proceedings. OpenReview.net, 2018.

[36] Minjie Wang, Lingfan Yu, Quan Gan, Yu Gai, Zihao Ye, Mufei Li, Jinjing Zhou, Qiheng Guo, Hao Zhang, Haibin Lin, Junbo Zhao, Jinyang Li, Alexander Smola, and Zheng Zhang. Deep graph library: Towards efficient and scalable deep learning on graphs. CoRR, abs/1909.01315, 2019.

[37] Mingyu Yan, Lei Deng, Xing Hu, Ling Li, Yujing Feng, Xiaochun Ye, ZhiMIN Zhang, Dongrui Fan, and Yuan Xie. HyGCN: A GCN accelerator with hybrid architecture. In IEEE International Symposium on High Performance Computer Architecture, HPCA 2020, San Diego, CA, USA, February 22-26, 2020, pages 15–29. IEEE, 2020.

[38] Mingyu Yan, Xing Hu, Shuangchen Li, Abanti Basak, Han Li, Xin Ma, Itir Akgun, Yujing Feng, Peng Gu, Lei Deng, Xiaochun Ye, ZhiMIN Zhang, Dongrui Fan, and Yuan Xie. Alleviating irregularity in graph analytics acceleration: a hardware/software co-design approach. In Proceedings of the 52nd Annual IEEE/ACM International Symposium on Microarchitecture, MICRO 2019, Columbus, OH, USA, October 12-16, 2019, pages 615–628. ACM, 2019.

[39] Rex Ying, Ruining He, Kaifeng Chen, Peng Ekombatchai, William L. Hamilton, and Jure Leskovec. Graph convolutional neural networks for web-scale recommender systems. In Proceedings of the 24th ACM SIGKDD International Conference on Knowledge Discovery & Data Mining, KDD 2018, London, UK, August 19-23, 2018, pages 974–983, 2018.

[40] Jiaxuan You, Zhitao Ying, and Jure Leskovec. Design space for graph neural networks. In Hugo Larochelle, Marc’Aurelio Ranzato, Raia Hadsell, Maria-Florina Balcan, and Hsuan-Tien Lin, editors, Advances in Neural Information Processing Systems 33: Annual Conference on Neural Information Processing Systems 2020, NeurIPS 2020, December 6-12, 2020, virtual, 2020.

[41] Hanqing Zeng and Viktor K. Prasanna. Graphacht: Accelerating GCN training on CPU-FPGA heterogeneous platforms. In Stephen Neuendorffer and Lesley Shannon, editors, FPGA '20: The 2020 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, Seaside, CA, USA, February 23-25, 2020, pages 255–265. ACM, 2020.

[42] Xiaowei Zhu, Wentao Han, and Wenguang Chen. GridGraph: Large-scale graph processing on a single machine using 2-level hierarchical partitioning. In Shan Lu and Erik Riedel, editors, 2015 USENIX Annual Technical Conference, USENIX ATC’15, July 8-10, Santa Clara, CA, USA, pages 375–386. USENIX Association, 2015.