Algorithm to Compilation Co-design: An Integrated View of Neural Network Sparsity

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Abstract

Reducing computation cost, inference latency, and memory footprint of neural networks are frequently cited as research motivations for pruning and sparsity. However, operationalizing those benefits and understanding the end-to-end effect of algorithm design and regularization on the runtime execution is not often examined in depth.

Here we apply structured and unstructured pruning to attention weights of transformer blocks of the BERT language model, while also expanding block sparse representation (BSR) operations in the TVM compiler. Integration of BSR operations enables the TVM runtime execution to leverage structured pattern sparsity induced by model regularization.

This integrated view of pruning algorithms enables us to study relationships between modeling decisions and their direct impact on sparsity-enhanced execution. Our main findings are: 1) we validate that performance benefits of structured sparsity block regularization must be enabled by the BSR augmentations to TVM, with 4x speedup relative to vanilla PyTorch and 2.2x speedup relative to standard TVM compilation (without expanded BSR support). 2) for BERT attention weights, the end-to-end optimal block sparsity shape in this CPU inference context is not a square block (as in Gray et al. [2017]) but rather a linear 32x1 block 3) the relationship between performance and block size / shape is suggestive of how model regularization parameters interact with task scheduler optimizations resulting in the observed end-to-end performance.

1 Introduction

Capabilities of neural networks have accelerated in the last decade and that progress has been accompanied by a productive tension between two competing goals. One goal is to expand the boundaries of functionality and performance, which has been accompanied by increasing scale in data and compute. A second goal is for new capabilities to have broad impact and operationalization. This goal tends towards the opposite direction - shrinking down compute and data required to achieve a capability.

For example, expansion of data and compute has led to recent NLP advances showing how large language models have unprecedented generalization capabilities [Brown et al. 2020, Raffel et al. 2019]. These models should enable new realtime human-model interactions and entirely novel model development process where capabilities are instantiated at inference time, or can be rapidly adapted using lightweight methods such as prefix tuning [Li and Liang 2021]. However computational cost is an impediment to the impact and adoption of such models. How do we make these models accessible for both small and large scale research and deployment? Could such models be used in conjunction with privacy-preserving AI which requires model computation on edge devices? How can these
language models be embedded at low cost into human-in-the-loop interactions requiring realtime latency?

One proposed answer to these questions has been the literature around sparsification and pruning of neural networks. Since the 1980s, we have known that it is usually possible to prune most parameters from trained neural networks without affecting accuracy [LeCun et al., 1990]. Han et al. [2015] reduced number of parameters of AlexNet [Krizhevsky et al., 2012] by $9 \times$ and VGG [Simonyan and Zisserman, 2014] by $13 \times$ using connection pruning. The lottery ticket hypothesis was proposed by Frankle and Carbin [2018], which observes that a subnetwork of randomly-initialized network can replace the original network with the same performance. Chen et al. [2020, 2021] demonstrate the core LTH observations remain generally relevant in transformer models for both computer vision and natural language processing. Although current-generation CPUs and GPUs do not immediately benefit from sparsity, there is an active research area dedicated to writing libraries to accelerate sparse neural networks on these platforms [Elsen et al., 2020] and next generation hardware has native sparsity support (e.g., the NVIDIA A100, GraphCore IPU, and Cerebras Wafer-Scale Engine).

Although pruning is often motivated by performance, algorithms are often studied in isolation separate from their consequences with respect to compilation and execution. However, interactions between model regularization choices, model compilation, and inference execution can have subtle-yet-critical effects on performance.

In this research, we implement both unstructured and structured sparsification of the attention weights of BERT alongside BSR sparsity optimizations in the TVM compiler [Chen et al., 2018]. We show how algorithms and compiler optimizations interact at different levels of the abstraction stack to determine end-to-end performance.

2 Methods

2.1 Structured Sparsification

Following the conventional pruning formulation, we consider the following optimization problem [Han et al., 2015]:

$$\min_w \sum f(w) + \lambda \|w\|_p,$$

(1)

where $\|w\|$ denotes the parameters of a neural network model, $\|w\|_p$ denotes the $\ell_p$ norm of $w$ for $p \in \{0, 1\}$. Note that equation 1 can be interpreted as the Lagrangian form of the problem:

$$\min_{w \in \mathbb{R}^d} f_0(w)$$

subject to $\|w\|_p \leq \tau,$

(2)

where $f_0$ is the pruning loss, $p \in \{0, 1\}$, and $\tau$ is the tolerance of nonzero weights. To obtain models with structured sparsity, we calculate our norm $\|w\|_p$ in a structured group manner

$$\|w\|_p = \sum_{n=1}^{N} \sum_{b=1}^{B} \|w_{b,n}\|_p$$

(3)

A weight matrix or convolution kernel can be divided into blocks with sparsity determined by the outcome of the model optimization. Here $B$ is the block size and $N$ is the number of blocks that comprise the weight matrix or convolution kernel.

In contrast to the standard (unstructured) $\ell_1$ / lasso procedure, group sparsity regularizes towards sparsity within each block, leading to a smaller set of more common used intra-block patterns, at least in the regime where $B$ is sufficiently small.

2.2 TVM Compiler Integration

Gray et al. [2017], Gale et al. [2020] has shown the advantage of block sparsity in executing Transformer [Vaswani et al., 2017] models on GPU. Zhang et al. [2021], Gale et al. [2020] demonstrates that the compiler scheduling introduces tremendous inference speed up on neural network. We augmented the TVM compiler with the following additions to achieve inference speed up on sparse neural network:
• We expand support for Block Sparse Row (BSR) for use with attention kernels and fully connected layers. BSR reduces the sparse neural network memory footprint and speeds up inference. Acceleration of sparse neural networks depends on eliminating operations (e.g., element-wise matrix multiplication) on zeroed weights (through pruning) and reusing the sparsity structure-based operations.

• To eliminate the operation on zeroed-out weights, we implement the element-wise matrix multiplication for the BSR format. Specifically, we represent BSR matrices as data values, indices, and indptr (index pointer). Through indices and indptr, TVM picks only the non-zero weight in the sparse attention kernel and executes element-wise multiplication with input tensor. The BSR format and sparse multiplication operator implementation follow SciPy [Virtanen et al., 2020].

• The TVM task scheduler is able to reuse structure-based sparsity. The aforementioned indices and indptr of BSR representation intrinsically reflect the characteristics of sparse matrices. The BSR representations are stored in a task buffer together with corresponding operators in TVM. TVM analyzes the similarity of tasks in the buffer and optimize the execution of the tasks through an auto-scheduler. The analysis proceeds in the task searching stage, attending to different hardware specifications (e.g., number of cores, cache size, instruction set architecture (ISA), max memory per block, and max thread per block). If two tasks in the task buffer are the same, TVM treats them as identical and reuse them. If two tasks are similar, TVM schedules them adjacent in the execution path.

Figure 1: Overview of the augmented compiler: algorithm to compilation co-design

2.3 Experiments

The goal of our experiments was to implement both unstructured and structured sparsification and assess the relative end-to-end impact on performance when the algorithm interacts with the compiler implementation, while assessing accuracy at different levels of sparsification. Here we focus on a sparsity and compiler co-design approach to achieve inference speed up on CPU (Intel Core Processor Haswell). Haswell is not a high performance CPU, but rather a cost-effective contemporary standard and widely used in cloud computing environments.

We use the official BERT model from Google as the starting point. Following the notation from Devlin et al. [2019], we denote the number of layers (i.e., transformer blocks) as \(L\), the hidden size as \(H\), and the number of self-attention heads as \(A\). We prune the BERT model: BERT\_BASE \((L = 12, H = 768, A = 12, \text{total parameters} = 110M)\). As the parameters of these transformer blocks take up more than 90% weights of the entire BERT, the weights of these transformer blocks are our pruning target.

Data: In pre-training, we use the same pre-training corpora as Devlin et al. [2019]: BookCorpus (800M words) [Zhu et al., 2015] and English Wikipedia (2,500M words). Based on the same corpora,
we use the same preprocessing script to create the pre-training data. In fine-tuning, we report our results on the Stanford Question Answering Dataset (SQuAD) [Rajpurkar et al., 2016] and the General Language Understanding Evaluation (GLUE) benchmark [Wang et al., 2018]. The GLUE is a collection of datasets/tasks for evaluating natural language understanding systems.¹

**Input/Output representations:** We follow the input/output representation setting from Devlin et al. [2019] for both pre-training and fine-tuning. We use the WordPiece Wu et al. [2016] embeddings with a 30,000 token vocabulary. The first token of every sentence is always a special classification token ([CLS]). The sentences are differentiated with a special token ([SEP]).

**Evaluation:** In pre-training, BERT considers two objectives: masked language modeling (MLM) and next sentence prediction (NSP). For MLM, a random sample of the tokens in the input sequence is selected and replaced with the special token ([MASK]). The MLM objective is a cross-entropy loss on predicting the masked tokens. NSP is a binary classification loss for predicting whether two segments follow each other in the original text. In pre-training, we use MLM and NSP as training objectives to pre-train, retrain the BERT model, and as metrics to evaluate the BERT model. In fine-tuning, F1 scores are reported for SQuAD, QQP and MRPC. Matthew’s Corr and Pearson-Spearman Corr are reported for CoLA and SST2 respectively. Accuracy scores are reported for the other tasks.

## 3 Results

We first run standard dense computations to set baselines for uncompiled PyTorch / Tensorflow inference (Table[1]) without any model pruning or TVM compilation. We compare these baselines against sparse model variants using irregular sparse pruning and structured sparse pruning to BERT for a standard SQuAD QA task [Rajpurkar et al., 2016] and GLUE benchmark [Wang et al., 2018].

Next, with standard TVM compilation (i.e. prior to adding expanded BSR support) we observe an expected speedup, with inference time reduced to about 55% of the vanilla PyTorch inference time (from 1389ms to 764ms). Note we are less interested in the absolute inference times which will be specific to a hardware configuration, and more interested in relative reduction observed in this context of commodity CPU hardware. Table[1] shows inference times at an 80% sparsity ratio for a range of block sparsity optimizations.

As a negative control, we apply irregular sparse pruning and structured sparse pruning of various dimensions and assess the inference time using the standard (unmodified) TVM compiler and runtime. We observe that inference performance remains approximately the same with most deviations being within ~ 5% of dense inference in spite of the 80% sparsity ratio.

We then apply the same experiments for the augmented TVM compiler, expanding BSR support, labeled TVM⁺ in Table[1]. Here we observe notable performance improvements from the structured sparse pruning, with inferences times improving by as much as 55% (0.45 TVM⁺/Dense) in the case of 1 × 32 block sparsity.

There is a non-monotonic relationship between linear block size and computation time. Inference time improves for L1 block sparsity dimensions from 1 × 1 to 1 × 32, but becomes worse for larger sizes (Figure[2] Table[3]).

When transitioning from single-row linear blocks for structured sparsity to square blocks of 4x4, 8x8, 16x16, and 64x64 we see a marked decrease in performance, although inference is still more performant than the dense computation.

The performance of the models (Table[2]) is relatively consistent as the sparsity ratio varied from 50% to 80%. The largest drop was in SQuAD F1 scores while other tasks were within 1-3% for

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¹https://github.com/google-research/bert

²The datasets/tasks are: CoLA [Warstadt et al., 2018], Stanford Sentiment Treebank (SST) [Socher et al., 2013], Microsoft Research Paragraph Corpus (MRPC) [Dolan and Brockett, 2005], Semantic Textual Similarity Benchmark (STS) [Agirre and Soroa, 2007], Quora Question Pairs (QQP), Multi-Genre NLI (MNLI) [Williams et al., 2017], Question NLI (QNLI) [Rajpurkar et al., 2016], Recognizing Textual Entailment (RTE) and Winograd NLI (WNLI) [Levesque et al., 2012].
Table 1: Inference times in milliseconds on a commodity Haswell Intel Core Processor and improvement relative to the dense baseline (TVM+/Dense).

| Sparsity Ratio | Dense | Irregular Sparsity | Structured Sparsity |
|----------------|-------|--------------------|---------------------|
| block size     | 1389  | 1375               | 1 × 1               |
| PyTorch ms     | 1298  | 1281               | 1 × 4               |
| Tensorflow ms  | 764 (19) | 759 (14)         | 755 (11)           |
| TVM ms         | 772 (19) | 754 (6)            | 379 (8)            |
| mean std       | 1.000 (0.025) | 0.977 (0.008)     | 0.690 (0.003)      |
| TVM+/ms mean   |       |                    |                    |
| TVM+/ms std    |       |                    |                    |

2x-5x compression rates. Fine tuning and hyperparameters were not aggressively optimized and these values can likely be improved with more computationally intensive fine tuning assessments.

| Sparsity Ratio | SQuAD 1.1 | MNLI | MNLIM | MRPC | QNLI | QQP | RTE | SST-2 | CoLA |
|----------------|-----------|------|-------|------|------|-----|-----|-------|------|
| Dense          | 88.5      | 84.1 | 84.1  | 84.6 | 91.4 | 90.4| 69.7 | 93.2  | 81.5 |
| 50% Zeros      | 86.5      | 83.6 | 82.5  | 87.0 | 90.9 | 89.7| 68.6 | 92.1  | 81.9 |
| 80% Zeros      | 81.8      | 81.3 | 81.1  | 86.8 | 89.5 | 89.0| 64.6 | 91.5  | 80.4 |

Table 2: Task accuracy for dense, 50% sparsified, and 80% sparsified BERT variants.

4 Discussion

We have implemented pruning algorithms alongside compiler support for sparse inference. In doing so, we are able to assess sparsity regularization from an integrated perspective. We show how the performance implications of modeling decisions are dependent on compiler support for sparsity, and illustrate the interaction between regularization and scheduling algorithms embedded in the compiler and runtime.

An interesting observation was the non-monotonic relationship between inference time and block size. This could reflect how modeling choices interact with the runtime scheduler. For small sparse blocks, block computation improves performance while the sparsity pattern is also likely to be replicated, leading to computation reuse by the TVM scheduler. As block sizes increase, in spite of larger-scale parallel computation, the cardinality of repeated sparsity patterns drops, which reduces the compute savings available to the scheduler. Thus larger linear patterns such as 1 × 384 as well as larger N × N square blocks are likely to have this issue.

Some direct follow-ups to this work include 1) create instrumentation tools for introspection of task reuse by the scheduler to better quantify effects of regularization choices 2) examine whether the finding that 1 × 32 linear blocks are optimal relates to the sparsity patterns and structure of BERT’s attention weight matrices 3) examine algorithm-to-compiler performance relationships in other architectures such as convolution and graph neural networks and 4) generalize principles for
Designing structured sparsification algorithms that are likely to result in end-to-end performance improvements, accounting for compilation and runtime execution.

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