Power System Harmonic Elimination to Improve Power Quality

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Abstract- An improvised RLC interface filter for a Dynamic Voltage Restorer (DVR) is proposed. The RLC filter is connected in the front end between the IGBT based Voltage Source Inverter (VSI) and the injection transformer and is able to eliminate voltage harmonics in the system and also switching harmonics generated from VSI. The voltage at the sensitive load end is pure sinusoidal. In this method, the DVR produced Pulse Width Modulation (PWM) voltage with voltage harmonic canceling the voltage harmonic generated from the supply main. The VSI handles harmonic power. The low order switching harmonics generated by the IGBT based VSI is suppressed. The DVR has greater voltage injection capability. Good dynamic and transient results recorded and Total Harmonic Distortion (THD) at the sensitive load end is minimized. The voltage at the sensitive load is sinusoidal and at 1.0 pu. PSCAD/EMTDC is used to validate the performance of the interface filter and the DVR. Simulated results are presented.

Keywords: Series Active Power Filter (SAPF), Voltage harmonics, Passive filters, H-Bridge inverter

1. INTRODUCTION

Devices such as arc furnaces, adjustable speed drives, computer power supplies, switch-mode power supply etc. are some typical nonlinear characteristic loads used in most of the industrial applications and are increasing rapidly due to technical improvements of semiconductor devices, digital controller and flexibility in controlling the power usage. The alternate switching actions of these power devices and its non-linearity characteristics result in a distorted input current. The power converter will behave like a current source, injecting harmonic and the interaction with the main system impedance will result in voltage distortion. Voltage THD above 5 % is undesirable above limit IEEE Std. 519. Unwanted heat in generated in equipment connected to harmonic source. High level of voltage distortion will cause equipment mal-function and damage.

Power system rich in harmonics have poor operating power factor and low efficiency. Harmonics can damage power factor correcting capacitors at plant facility and at utility distribution points. Harmonics can initiate system resonance that can severely disrupt system operation. A method is proposed to reduce the voltage THD. Rectifier or dc supply connected with a large filter capacitor on its dc side is a voltage type harmonic source [1][2][3]. One of the problems of power system harmonics is the supply voltage distortion at the Point of Common Coupling (PCC). Generally, passive LC filter is used to attenuate the voltage ripple from inverter switching [4][5]. For specific harmonic elimination, banks of passive filters are connected parallel with the load at the load end [6][7][8]. This will suppress the specific harmonics such as 5th, 7th and 9th orders. This method is not cost effective. The output voltage on the LC filter capacitor is controlled by switching operation of the PWM inverter, where the LC filters will introduce a time delay and cause resonance in the output AC voltage. Publication [9][10] discusses the regulating technique done to control the output voltage across the LC filter capacitor. Various control techniques has been introduced to control harmonics in inverter such as digital control strategies based on repetitive control, dead-beat control, and discrete-time sliding-mode control [11]. The techniques have some drawbacks, such as complexity, sensitivity to parameter variations and loading conditions, and steady-state errors in distorting condition.
Current ripple of PWM inverter is reduced with large inductor however, the voltage drop across it is increased [12]. The disadvantages of large inductor are the cost, weight and also increase voltage stress on the inverter switches.

Several controller schemes were proposed to control the DVR such as PI controller and park's transformation [13], DVR with Sliding Mode Control [14], Indirect Control of Capacitor Supported DVR [15], instantaneous p-q theory [16], synchronous d-q theory [17] and fuzzy logic controller [18]. Majority of the proposed controller algorithms were based on the Synchronous Rotating Frame Theory (SRFT) or d-q theory while the remaining controllers were too complex to implement as significant computing time was required. It is observed that many researchers addressed the problems of power quality and special attention is given to the voltage sag/swell but few research papers are published on multilevel converters based DVR. The developed controllers are also complex to implement and required more number of components. The total harmonic distortion (THD) of the load side voltage obtained by some research papers is above IEEE-519 Standards. Also the results obtained for the RMS of the load side voltage of some researchers is shown to be lower than the desired level and as there is not much published literature on multilevel based DVR, it is necessary to establish the compensating performance of seven-level cascade multilevel based DVR by proposing new controlling techniques.

This paper proposes an improvised smoothing filter design method with minimum transient current overshoot problem without decreasing the active damping performance of inverter systems. The VSI model is a 7-level H-Bridge as shown in Figure 1. The number of H-bridge cells in a Cascaded H-Bridge (CHB inverter) is determined by the inverter operating voltage, harmonic requirements, and cost. A phase-shifted carrier-based modulation scheme is used for the multilevel inverter. The main advantage of PWM control based DVR control is including fast switching speed of the power switches beside PWM technique offers simplicity and good response and high switching frequencies can be used to improve on the efficiency of the converter without incurring significant switching losses [19]. The basic idea of PWM based multicarrier phase shift modulation technique is varying the ON or OFF switching periods of the IGBTs switches of multilevel converter at a constant frequency so that the ON periods are longest at the peak of the wave. The control of switch duty ratio adjusts the output voltage level. The multilevel inverter with s voltage levels requires (s – 1) triangular carriers. In the phase-shifted multicarrier modulation, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by \( \theta_{cr} = \frac{360^\circ}{s - 1} \).

Phase shifted multicarrier modulation model in PSCAD is shown in Figure 2. The three phase structure of seven level cascaded inverter is illustrated in Figure 1. Each dc source is connected to a three phase inverter. Each inverter level can generate three different voltage outputs, +Vdc, 0, and –Vdc by connecting the dc source to the ac output by different combinations of the four switches. The ac outputs of each of the different full bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs.
From Figure 2, when switch S15 is at 240°, the phase shift of S16 is at 60°. Similarly S13 at 120°, phase shift of S14 is at 300°, S11 is 0° and S12 is 180°.

![Figure 2. Phase-shifted multicarrier modulation model in PSCAD](image)

2. **RLC FILTER SYSTEM**

The single-phase one leg equivalent circuit of an inverter system is shown in Figure 3. From the Figure, $E_{inv}$ is the VSI output voltage, supply current is $i_x$, current through capacitor is $i_c$, load current is $i_L$ and $V_L$ is voltage across the load.

The dc supply voltage $V_{dc}$ is constant and the gate switch of VSI is ideal. The output voltage of the VSI is written as:

$$E_{inv} = V_L + R_{f}i_x + L_{f} \frac{di_x}{dt}$$

(1)

Separating both the capacitor voltage and the current through the inductor into average over a switching cycle and harmonics ripple component,

$$E_{inv} = \bar{V}_L + \bar{V}_L$$

(2)

$$i_c = \bar{i}_L + \bar{i}_L$$

(3)

Substituting eq. 2 and 3 in eq. 1 gives

$$E_{inv} = \bar{V}_L + \bar{V}_L + R_{f} (\bar{i}_L + \bar{i}_L) +$$
\[ L_f \frac{d}{dt} (\overline{i_x} + i_R) \]  

Considering \( P_L \) and \( R_L \), \( \overline{i_x} \) is small as compared to \( L_f \frac{d}{dt} \overline{i_x} \), then the ripple component of the filter inductor current is

\[ \overline{i_x} = \frac{1}{L_f} \int (E_{inv} - \overline{E_{inv}}) dt \]  

and the average value of output voltage is

\[ E_{inv} = \overline{V_L} + R_L \overline{i_x} + L_f \frac{d}{dt} \overline{i_x} \]  

The capacitor voltage harmonic, with reference to Figure 3;

\[ i_c = i_x - i_L \]  

Splitting the capacitor and inverter output currents into the average and harmonic components,

\[ i_c = \overline{i_c} + i_{ch} \]  

\[ i_x = \overline{i_x} + i_{xh} \]  

Substituting eq. (3) and eq. (8)-(9) into eqn. (7), the following equation is obtained

\[ \overline{i_c} + \overline{i_{ch}} = \overline{i_x} + \overline{i_{xh}} - i_L - \overline{i_L} \]  

Thus,

The average and harmonic components of the filter capacitor current can be obtained as

\[ \overline{i_c} = \overline{i_x} - \overline{i_L} \]  

\[ \overline{i_{ch}} = \overline{i_{xh}} - \overline{i_{Lh}} \]  

Considering, the filter capacitor is large, and all the inductor harmonic current flows through the capacitor. Thus,

\[ \overline{i_{ch}} = \overline{\overline{i_x}} \]  

The ripple component of the filter capacitor voltage is

\[ \overline{\overline{V_c}} = \frac{1}{C_f} \int \overline{i_{ch}} dt = \frac{1}{C_f} \overline{i_x} \overline{dt} \]  

3. LC FILTER VALUES

The reactive power of the LC filter is

\[ P_{rec} = \omega_s L_f \left( I_{xh}^2 + I_{ch}^2 \right) + \omega_s C_f \left( V_L^2 + V_{LV}^2 \right) \]

where,

\[ \omega_s = 2\pi f_s \]  

\( f_s \) is fundamental frequency, \( I_{xh} \) and \( V_L \) are rms value of the fundamental component of the inductor current and load voltage. The harmonic components is much smaller than the fundamental components and eq. 14 is simplified as

\[ P_{rec} = \omega_s L_f \left( I_{xh}^2 + I_{ch}^2 \right) + \omega_s C_f \left( V_L^2 \right) \]  

The rms value of the current through the inductor is

\[ P_{rec} = \omega_s L_f \left( I_{xh}^2 + I_{ch}^2 \right) + \omega_s C_f \left( V_L^2 \right) \]

\[ \omega_s C_f \left( V_L^2 \right) \]  

Splitting the current \( I_x \) in terms of real and imaginary, eq. 15 is rewritten as

\[ P_{rec} = \omega_s L_f \left( I_{xh}^2 + I_{ch}^2 \right) + \omega_s C_f \left( V_L^2 \right) \]

\[ \omega_s C_f \left( V_L^2 \right) \]

Capacitance is given as

\[ C_f = k \frac{V_{dc}}{f_s f_{av}} \]

Inductance is given as

\[ L_f = \frac{V_{dc}}{f_s f_{av}} \left( k \frac{V_{dc}}{V_{av}} \left( 1 + 4 \pi^2 \left( \frac{f_x}{f_{av}} \right)^2 \right)^{1/2} \right) \]

where,

\[ k \]  

is the modulation index.

From extensive simulation, the value of \( R_L \) is selected at 2.0 ohm giving good dynamic performance, actively damps the resonance oscillations, during voltage disturbances. The value of \( L \) and \( C \) component is determined to minimize the reactive power in these components. From eq. 17 and 18, the capacitance and inductance values are 75 \( \mu \)F and 0.09 mH, respectively for this model.

4. PROPOSED CONTROL SCHEME
In this proposed control strategy as shown in Figure 4, the synchronous angular frequency of the supply voltage is detected by using phase locked loop (PLL). The generated reference angular frequency is used to generate the zero sequence component of the system voltage based on eq. 19.

\[
\begin{bmatrix}
V_{\text{zero sequence}} \\
V_d \\
V_q
\end{bmatrix} = \sqrt{2} \begin{bmatrix}
1 & 0 & 0 \\
0 & \cos(\omega t) & \sin(\omega t) \\
0 & -\sin(\omega t) & \cos(\omega t)
\end{bmatrix} \begin{bmatrix}
1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\
1 & -1/2 & -1/2 \\
0 & \sqrt{3}/2 & -\sqrt{3}/2
\end{bmatrix} \begin{bmatrix}
V_a \\
V_b \\
V_c
\end{bmatrix}
\]  

(19)

By applying the inverse of the park transformation under consideration of \( V_d = 0, V_q = V_{\text{Smax}}, V_0 = V_{\text{zero sequence}} \), the desired system voltages are generated as shown in (20). Position of d-q vector is shown in Figure 5.

\[
\begin{bmatrix}
V_a \\
V_b \\
V_c
\end{bmatrix} = \sqrt{3} \begin{bmatrix}
1 & 0 & 0 \\
0 & \cos(\omega t) & -\sin(\omega t) \\
0 & \sin(\omega t) & \cos(\omega t)
\end{bmatrix} \begin{bmatrix}
1/\sqrt{2} & 1 \sqrt{3}/2 \\
1/\sqrt{2} & -1/2 \sqrt{3}/2 \\
1/\sqrt{2} & -1/2 \sqrt{3}/2
\end{bmatrix} \begin{bmatrix}
V_{\text{zero sequence}} \\
V_{\text{Smax}}
\end{bmatrix}
\]  

(20)

The reference compensation voltages to control DVR are generated by comparing the calculated desired system voltages in (20) and the measured load side voltages, and then the error signals are subjected to a phase shift multicarrier PWM controller in order to determine the desired switching pattern for the IGBTs of DVR.
5. RESULTS AND DISCUSSION

The model is connected to three-phase at 415 V, 50 Hz, power source, as shown in Figure 6. The sensitive load is three-phase R-L circuit rated at (R = 8.0 ohms, L = 0.05 mH) with a parallel connected 3-phase diode bridge rectifier series with a 0.9 mH reactance, as nonlinear load. Voltage harmonics distortion is introduced when a three-phase diode Bridge rectifier is connected at the main supply.

![Figure 5. D-Q vector representation](image)

![Figure 6. Power circuit of DVR model in PSCAD](image)
5.1 Compensation of voltage harmonics

Voltage harmonics is initiated at the source side between \( t = 0 \text{ms to 300ms} \), distorting both source and voltage at sensitive load as presented in Figure 7. THD level recorded at source side is 12.56 \%. Figure 7 also shows voltage at the sensitive load and the injected voltage by DVR.

As can be seen from Figure 7, the proposed DVR is able to inject the appropriate three-phase voltage component to correct the supply voltage anomalies due to three-phase harmonic distortion. Under normal operation the DVR is doing nothing. It quickly injects the necessary voltage components to smoothen the load voltage upon detecting voltage harmonics. The load voltage waveform is sinusoidal maintained at 1.0 pu. The source and load current waveform is shown in Figure 8. As seen from the figure, the load current is compensated and is sinusoidal.
When the DVR is connected, the voltage THD is considerably reduced from 12.56 % to 1.793 % at sensitive load end as shown in Figure 9. This is a significant improvement. The system parameters used in the model are shown in Table 1.

![Figure 8. Source and load current waveform](image)

To evaluate performance of the proposed DVR based Seven-level cascaded multilevel inverter against other published literature, a comparison matrix is shown in Table 2. The Table shows that the voltage THD level of the current model developed in PSCAD has the lowest value. The main contributions of this study are as follows: seven level cascade multilevel converter based DVR for power quality improvement of the distribution systems has been developed and simulated in PSACD/EMTDC. Improvement in system voltage transient. New simple

![Figure 9. Comparison of THD level.](image)

| Table 1 |
|-----------------|-----------------|
| Supply voltage  | 415 V           |
| $f_s$           | 50 Hz           |
| $f_{sw}$        | 10 kHz          |
| $f_{cut-off}$   | 650 Hz          |

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controller schemes based d-q theory to overcome the disadvantages of the existing controller schemes by reducing the complexity, number of signal measurements and computing time has been developed.

| Description | [20] | [21] | [22] | [23] | [8] | Current Study |
|-------------|------|------|------|------|----|---------------|
| Year        | 1995 | 2008 | 2009 | 2012 | 2012 | 2014          |
| Operating voltage and frequency | 480 V, 60 Hz | 2300 V, 50 Hz | 346 V, 50 Hz | 400 V, 50 Hz | 400 V, 50 Hz | 415 V, 50 Hz |
| Inverter type | Passive Clamped Resonant DC Link Inverter | Diode Clamped | 3-level | 3-level | 3-level | Cascade Multilevel |
| RMS of the load side voltage after compensation | 283 V | Not given | 210 V | 240 V | 240 V | 245 V |
| THD of the load side voltage after compensation | 3.39 % | 2.23 % | 3.31 % | 3.9 % | 4.35 % | 1.793 % |

6. CONCLUSION

This project presents a new model of DVR based Seven-level cased multilevel converter and, the controller. The simulation results show that voltage imperfection mitigation, and the enhancement of voltage stability has been achieved. The performance comparison of the proposed DVR and its controller with some previously reported DVR modules shows that it is more efficient in terms of cost, component, power consumption and losses. It is also found that the absolute beneficial of DVR can be achieved with connection of the distributed generation sources such as solar cells, wind generation system etc in the DC side of the proposed DVR model. The simulation results have demonstrated excellent suppression of voltage harmonic capabilities of DVR using the proposed new RLC filter carrier based PWM technique. The DVR is an attractive custom power device for power quality improvement specifically to suppress voltage harmonics and also to mitigate voltage sag and combination both as a hybrid unit.

7. REFERENCES

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