Efficient Floating Point Arithmetic for Quantum Computers

Raphael Seidel†, Nikolay Tcholtecv†, Sebastian Bock†, Colin Kai-Uwe Becker†, Manfred Hauswirth†∗
†Fraunhofer Institute for Open Communication Systems (FOKUS)
Berlin, Germany
{firstname.lastname}@fokus.fraunhofer.de
∗Technische Universität Berlin

Abstract—One of the major promises of quantum computing is the realization of SIMD (single instruction - multiple data) operations using the phenomenon of superposition. Since the dimension of the state space grows exponentially with the number of qubits, we can easily reach data point for data-processing instructions which would be rather expensive in classical computing. Formulating such instructions in terms of quantum gates, however, still remains a challenging task. Laying out the foundational functions for more advanced data-processing is therefore a subject of paramount importance for advancing the realm of quantum computing. In this paper, we introduce the formalism of encoding so-called-semi-boolean polynomials.

Index Terms—quantum computing, quantum arithmetic, floating point arithmetic

I. INTRODUCTION

It goes without doubt that the success of classical computers heavily relies on their ability to perform arithmetic evaluations. One might argue that the unique nature of quantum computers works better for fundamentally different approaches to information processing like the prominent variational quantum algorithms [1]. However, the following example shows that once reliable hardware is available, quantum computers can surpass classical computers regarding the FLOPS metric.

To elaborate on this claim, consider the situation that an arbitrary quantum algorithm requires the multiplication of two numbers. For this, we assume the following partition of quantum registers:

- Factor 1 register
- Factor 2 register
- Target register
- Miscellaneous register

The factor registers hold the information corresponding to each factor; the target register stores the multiplication results. The miscellaneous register is an m bit register which holds any other information that the algorithm produced so far.

We assume that before the multiplication, the quantum computer is in the state

\[ |\psi\rangle = \sum_{i=0}^{2^{m}-1} a_i |x_i\rangle |y_i\rangle |0\rangle |i\rangle. \]  

Applying the multiplication circuit to this state let us estimate how many multiplications we can execute simultaneously:

\[ U_{\text{mult}} |\psi\rangle = \sum_{i=0}^{2^{m}-1} a_i |x_i\rangle |y_i\rangle |x_i \cdot y_i\rangle |i\rangle. \]  

Since we evaluated one multiplication per index i, we are in the best case at 2\(^m\) multiplications! The resource requirements of the multiplication circuit do not grow with m, thus we conclude that this situation can easily lead to the case, where multiplications cost less than a single gate! This could be regarded as an "inverse curse of dimensionality."

Another interesting estimation we can make using this insight is to derive how many qubits are required to bring today’s exascale (10\(^{18}\) FLOPS) computing to the zettascale (10\(^{21}\) FLOPS). For this, we assume an entangling gate speed of \(\approx 10^{-7}\) s and a 32-bit multiplication circuit depth \(\approx 10^4\) (see fig. 1) yielding a processing time of \(\approx 10^{-2}\) s per multiplication circuit execution. This implies that we need a superposition of 10\(^{19}\) computational basis states, which is reached at \(m = 65\) qubits. Together with the 32 · 3 = 96 qubits from the factor and target registers and an additional \(\approx 32\) ancilla qubits (which are required to steeply increase multiplication evaluation speed), we arrive at \(\approx 200\) qubits. This is however highly dependent on how the quantum

\footnotesize{1}FLOPS stands for floating point operations per second, which is a measure for the speed of a computation device

\footnotesize{2}“Curse of dimensionality” is a term coined by mathematician Richard Bellman, which describes the exponential growth of computation and data resources for higher-dimensional data.

\footnotesize{3}To define the depth of a circuit C, we divide C into a sequence of timesteps. During each time step, each qubit can execute at most one elementary gate. The circuit depth is then defined as the total amount of time steps required to complete the circuit. Note that this definition is highly dependent on the set of elementary gates. For our benchmarks we used the gate set \{CX, RZ, SX\}.
We implement a full adder for every digit position of both workings of a computer but it also minimizes the complexity which are necessary to construct the semi-boolean polynomial (1). Addition techniques like this are often called carry-ripple (VII). After this, in section (V) we discuss several techniques to improve the performance of the semi-boolean polynomial encoder.

This paper is structured as follows: In what is left of section (I) we will give a short overview of the basics of classical arithmetic and how it translates to quantum computers. In section (II) we will define and discuss the fundamentals which are necessary to construct the semi-boolean polynomial encoder. Section (III) introduces arithmetic operations as applications of the previously constructed encoding circuit. The remainder of this section discusses how signed and non-integer values can be treated. The following section (IV) constructs several methods to perform in-place operations (ie. addition, multiplication, polynomial evaluations etc.). After this, in section (V) we discuss several techniques to improve the performance of the semi-boolean polynomial encoder followed by a complexity estimation. Finally, in section (VI) the developed methods are critically reviewed, followed by a summary of our results in section (VII).

A. Overview

This section aims to provide the reader with some basic information about how arithmetic operations are traditionally performed on classical computers and how these methods translate to quantum computers.

Most of today’s implementations of arithmetic are performed in the binary system. Not only does this suit the inner workings of a computer but it also minimizes the complexity of the elementary building blocks of arithmetic circuits. To perform an addition the most straightforward approach is to deploy a chain of so-called full adders which perform the basic operation of vertical addition in binary eg.:

\[
\begin{array}{cccc}
1 & 0 & 1 & 0 \\
+ & 1 & 1 & 1 \\
\hline
1 & 0 & 0 & 0 \\
\end{array}
\]

We implement a full adder for every digit position of both summands, which determines the sum digit and the next carry digit depending on both the summand digits and the carry digit. An algorithmic formulation can be found in algorithm 1. Addition techniques like this are often called carry-ripple because in this approach certain additions can create a ripple of carries that propagates to the most significant position. Note that for adding two \( n \)-bit integers \( N_1, N_2 \), we need to execute \( n \) full adders, implying a complexity of \( O(\log(N)) \).

In base 2 the full adder can be represented by a truth table:

| \( x_i \) | \( y_i \) | \( c_{in} \) | \( c_{out} \) | \( s_i \) |
|-----------|-----------|------------|------------|-------|
| 0         | 0         | 0          | 0          | 0     |
| 0         | 1         | 0          | 1          | 1     |
| 0         | 0         | 1          | 0          | 0     |
| 1         | 0         | 1          | 0          | 1     |
| 1         | 1         | 1          | 1          | 1     |
| 1         | 1         | 0          | 0          | 1     |
| 1         | 1         | 1          | 1          | 1     |

Note that we can’t infer the constellation of \( x_i \) and \( c_{in} \) in the case that we just know \( y_i = 1, c_{out} = 1, s_i = 0 \), implying \( |x_i \rangle |y_i \rangle |c_{in} \rangle \rightarrow |s_i \rangle |y_i \rangle |c_{out} \rangle \) is not reversible. From this, we conclude that there is no (ancilla free) quantum circuit that can perform this operation. This is a bit inconvenient because especially for multiplications (which will be covered shortly), having an in-place addition is vital. This problem was however successfully addressed by Cuccaro et al. in [3]. For their approach, they realized that for \( x, y \in \mathbb{N} \) the in-place addition \( |x \rangle |y \rangle |0 \rangle_{n+1} \rightarrow |x \rangle |x + y \rangle \) by itself is indeed reversible implying that the structure of successive full-adders might be the problem. Therefore their new approach consisted of calculating a set of intermediate truth values (with so-called MAJ gates) for each bit which are then again processed (in reversed order) by a sequence of so-called UMA gates resulting in a characteristic V-shape of the belonging circuits. Even though this circuit design is cheap in qubits and gates, the V-shape prevents parallel execution of most of the gates which results in sub-optimal circuit depth.

Evaluating multiplications is simple once we have access to in-place addition. This is because the product of any binary number \( y \) with another number \( y \) with just a single 1 (for

\[4\] Since every quantum gate can be represented by a unitary (and therefore invertible) operator, any sequence of such gates has to be invertible
instance $y = (100)_2$ is simply $x$ but bit shifted depending on where $y$ had it’s 1:

$$12 \cdot 4 = (1100)_2 \cdot (100)_2 = (1100)_2 \ll 2 = (110000)_2 = 48.$$  

(3)

If we now want to relax the restriction of the second factor $y$ having only a single 1, we can write $y$ as a sum of single-1-numbers

$$y = a_0 + a_1 + \ldots + a_k,$$

(4)

for instance $(1010)_2 = (1000)_2 + (10)_2$ and then calculate

$$x \cdot y = \sum_{i=0}^{k} x \cdot a_i.$$  

(5)

Here we can see why an in-place adder is so important: Without it, we would have to store (and uncompute) at least $k$ different numbers (one for each iteration of the sum). We rewrite eq. (5) in a more algorithmic manner

$$xy = \sum_{i=0}^{n} (x \ll i)y_i.$$  

(6)

Where $n$ is the bit size of $y$, $y_i \in \mathbb{F}$ is the truth value of the $i$-th digit of $y$ in binary. From this, we formulate algorithm 2.

**Algorithm 2 Multiplication 1**

**Input:** Binary strings of the factors $(x_i)_{i \leq n}, (y_i)_{i \leq n}$  
**Output:** Binary string of the product $x \cdot y$

1: $s = 0$
2: for $i$ in $(0, 1, 2, \ldots, n)$ do
3: \hspace{1em} if $y_i$ then:
4: \hspace{2em} $s += (x \ll i)$
5: \hspace{1em} end if
6: end for
7: return $s$

We see that for the multiplication of two $n$-bit integers $N_1, N_2$ the algorithm requires $O(n)$ additions, implying a complexity of $O(\log(N))^2$.

Furthermore, we note that for the case of quantum computers, the bit shift doesn’t have to be performed physically (ie. through swaps) - it is enough to rewire the in-place addition circuit. Regarding the conditional execution of the in-place addition, there are multiple possibilities: We could either turn every gate of the addition into its controlled version (for instance using 5) or only control certain key gates of the adder as demonstrated in 5. Even though much cheaper in gate overhead, this only works for certain kinds of addition circuits. A third possibility, which we used to make the multiplication performance of various adders comparable to our methods (see

5A bit shift is an operation which moves a string of bits into a certain direction. Left shifts are denoted using the operator $\ll$, whereas right shifts are written as $\gg$. The amount of the shift is determined by the second operand. So for instance $(1010)_2 \ll 3 = (1010000)_2$

fig. (2)), compromises the best of both worlds. For this, we use the well-known 5 identity

$$a - b = (\overline{a} + b)$$  

(7)

where the $\overline{a}$ is the bitwise negation of $a$. Since we can easily perform conditional bitwise negation using multiple CNOT gates, this allows for a versatile and efficient realization of carry-ripple adder-based multiplication circuits. To see how this can be used, we reformulate eq. (4):

$$xy = \sum_{i=0}^{n} (x \ll i)y_i$$

$$= \sum_{i=0}^{n} (x \ll i) \frac{1 - (-1)^{y_i}}{2}$$

$$= \sum_{i=0}^{n} (x \ll i) \frac{1 - \sum_{i=0}^{n} (x \ll i)(-1)^{y_i}}{2}$$

$$= \sum_{i=0}^{n} (x \ll i) \frac{1}{2} \left( \sum_{i=0}^{n} (x \ll i) - \sum_{i=0}^{n} (x \ll i)(-1)^{y_i} \right)$$

$$= \sum_{i=0}^{n} (x \ll i) \frac{1}{2} \left( x \sum_{i=0}^{n} 2^i - \sum_{i=0}^{n} (x \ll i)(-1)^{y_i} \right)$$

$$= \left( x \ll (n + 1) - x - \sum_{i=0}^{n} (x \ll i)(-1)^{y_i} \right) \gg 1$$

From this, we give the modified version of algorithm 2:

**Algorithm 3 Multiplication 2**

**Input:** Binary strings of the factors $(x_i)_{i \leq n}, (y_i)_{i \leq n}$  
**Output:** Binary string of the product $x \cdot y$

1: $s = x \ll (n + 1)$
2: $s = x$
3: for $i$ in $(0, 1, 2, \ldots, n)$ do
4: \hspace{1em} if $y_i$ then:
5: \hspace{2em} $s += (x \ll i)$
6: \hspace{1em} else:
7: \hspace{2em} $s -= (x \ll i)$
8: \hspace{1em} end if
9: end for
10: return $s \gg 1$

Even though far from complete, this concludes the short overview on standard methods for arithmetic evaluations. In the upcoming sections, we will see a very different approach, which has its own benefits and drawbacks compared to the methods we presented so far.

II. FUNDAMENTALS

In this section, we will define the concept of semi-boolean polynomials and lay out the necessary techniques to encode their evaluation into circuits.

A. Modular arithmetic

A central part of the methods that are described below is modular arithmetic, therefore we will provide a short coverage
of the belonging basics.

For \( x \in \mathbb{Z} \), \( y \in \mathbb{N} \), the modulo operator \( \text{mod} \) maps to the smallest positive number \( z \) such that
\[
z = x + jy,
\]
where \( j \in \mathbb{Z} \) is an integer. For instance, we have \( 7 \text{ mod } 3 = 1 \) (\( j \) would be equal to 2 in this case). Given an integer \( n \in \mathbb{N} \), we can construct a ring \( \mathbb{Z}/n\mathbb{Z} \) by applying the modulus function to the set of integers. This ring is denoted as follows:
\[
\mathbb{Z}/n\mathbb{Z} := \mathbb{Z} \text{ mod } n.
\]
For \( a, b \in \mathbb{Z}/n\mathbb{Z} \) the arithmetic operations in \( \mathbb{Z}/n\mathbb{Z} \) are realized by applying \( \text{mod } n \) after their respective \( \mathbb{Z} \)-operations. For example:
\[
\text{mul}_{\mathbb{Z}/n\mathbb{Z}}(a, b) = \text{mul}_{\mathbb{Z}}(a, b) \text{ mod } n,
\]
\[
\text{add}_{\mathbb{Z}/n\mathbb{Z}}(a, b) = \text{add}_{\mathbb{Z}}(a, b) \text{ mod } n.
\]

B. Semi-Boolean Polynomials

Semi-boolean polynomials will play an important role in the course of this paper. The basic idea is to use a technique described in \[6\] to encode a certain type of polynomial. Although being unnamed by the authors of \[6\], we will denote these polynomials as \emph{semi-boolean} to differentiate between polynomials with more general domains. A \emph{semi-Boolean polynomial} (from now on: \emph{SB-polynomial}) is a multivariate polynomial that has Boolean tuples as its domain but arbitrary real numbers as coefficients:
\[
\Omega : \mathbb{F}_2^n \to \mathbb{R}.
\]
Furthermore, we define an integer \emph{SB-polynomial} as an SB-polynomial which has only integer coefficients. An example would be given by \[14\] where \( x_0, x_1 \) and \( x_2 \) denote boolean variables:
\[
\Omega(x) = 4x_0x_2 - 3x_1.
\]
Integer SB-polynomial evaluations can be encoded into circuits i.e., for two registers (domain and image) of size \( n, m \in \mathbb{N} \) respectively and a given integer SB-polynomial \( \Omega \), this encoding acts as
\[
U_{\text{sbp}}(\Omega) |x\rangle |0\rangle = |x\rangle |\Omega(x) \text{ mod } 2^m\rangle.
\]
How does this work? The idea is to construct the QFT of the state \( |\Omega(x)\rangle \) followed by an inverse QFT. Encoding the Fourier-transform of \( |\Omega(x)\rangle \) is advantageous because of the additive nature of phase gates.
We will first lay out the procedure of constructing the Fourier transformed state without any domain register. The encoding circuit will then follow by turning some of the gates into controlled operations.

Suppose we want to encode the Fourier transform of the state \( |y\rangle \), where \( y \) is some integer. The first step is to initialize the image register into the state of uniform superposition by applying \( H \) gates on every qubit:
\[
|s\rangle = \frac{1}{\sqrt{2^n}} \sum_{k=0}^{2^n-1} |k\rangle
\]
We now define the gate
\[
U_{\Omega}(y) = \bigotimes_{i=0}^{m-1} P_i \left( \frac{2\pi i y 2^i}{2^n} \right),
\]
where \( P_i(\phi) \) is the parametrized phase gate, \( \text{diag}(1, \exp(i\phi)) \) applied on the \( i \)-th qubit of the register. Applying \( U_{\Omega}(y) \) to the uniform superposition state gives
\[
U_{\Omega}(y) |s\rangle
\]
\[
= \frac{1}{\sqrt{2^n}} \sum_{k=0}^{2^n-1} \left( \prod_{j=0}^{m-1} \exp \left( \frac{2\pi i y 2^i k_j}{2^m} \right) \right) |k\rangle
\]
\[
= \frac{1}{\sqrt{2^n}} \sum_{k=0}^{2^n-1} \exp \left( \frac{2\pi i y m \sum_{j=0}^{m-1} 2^j k_j}{2^m} \right) |k\rangle.
\]
Using the conventions from Nielsen & Chuang chapter 5.1 \[7\] this is the Fourier transform of \( |y\rangle \) implying:
\[
\text{QFT}^\dagger U_{\Omega}(y) |\Omega(0)\rangle |0\rangle = |y \text{ mod } 2^n\rangle.
\]
We inserted the modulus because if \( 2^m \leq y = (y \mod 2^m) + j 2^m \) in eq. \[18\], the phase corresponding to \( j 2^m \) results in an integer multiple of \( 2\pi \) and therefore vanishes. Note that \( U_{\Omega} \) is additive in the sense that
\[
U_{\Omega}(y_1) U_{\Omega}(y_2)
\]
\[
= \left( \bigotimes_{i=0}^{m-1} P_i \left( \frac{2\pi y_1 2^i}{2^m} \right) \right) \left( \bigotimes_{i=0}^{m-1} P_i \left( \frac{2\pi y_2 2^i}{2^m} \right) \right)
\]
\[
= \bigotimes_{i=0}^{m-1} P_i \left( \frac{2\pi y_1 2^i}{2^m} \right) P_i \left( \frac{2\pi y_2 2^i}{2^m} \right)
\]
\[
= \bigotimes_{i=0}^{m-1} P_i \left( \frac{2\pi y_1 2^i + y_2 2^i}{2^m} \right)
\]
Hence, we can conclude that:
\[
U_{\Omega}(y_1) U_{\Omega}(y_2) = U_{\Omega}(y_1 + y_2).
\]
The next step for encoding SB-polynomials is to turn \( U_{\Omega} \) into controlled gates. If we for instance, control \( U_{\Omega}(y) \) on the 0-th qubit of the domain register, we can abuse our notation and write \( U_{\Omega}(y x_0) \) because if \( x_0 = 0 \), the gate is not executed, which is equivalent to applying \( U_{\Omega}(0) \). If \( x_0 = 1 \), \( U_{\Omega}(y) \) is executed which is also equivalent to \( U_{\Omega}(y x_0) \). The same works with more factors of \( x_i \) by controlling \( U_{\Omega} \) on the corresponding qubits. We, therefore, are now able to encode SB-monomials.
For instance,
\[
\text{QFT}^\dagger U_{\Omega}(4x_0 x_1 x_2) |x\rangle |s\rangle = |x\rangle |(4x_0 x_1 x_2) \text{ mod } 2^m\rangle.
\]
The key insight in finding these circuits is that the evaluation of the binary representation of $x$ to its value is an SB-polynomial:

$$x = \sum_{k=0}^{n_1-1} 2^k x_k.$$  

We formalize this idea by defining the $n$-bit unsigned integer encoding SB-polynomial:

$$\Omega_{\text{us}}^n : \mathbb{F}_2^n \rightarrow \mathbb{N},$$

$$(x_0, x_1, \ldots, x_n) \rightarrow \sum_{k=0}^{2^n-1} 2^k x_k.$$  

The next step is to write the arithmetic evaluations in terms of these SB-polynomials. This is not hard: The SB-polynomial for the addition is simply the sum of the corresponding SB-polynomials. From this, we conclude that the conversion from the binary representations of $x$ and $y$ to the value of $x + y$ can also be written as a semi-Boolean polynomial:

$$x + y = \sum_{k=0}^{n_1-1} 2^k x_k + \sum_{k=0}^{n_2-1} 2^k y_k$$

$$= \Omega_{\text{us}}^{n_1}(x_0, x_1, \ldots, x_n) + \Omega_{\text{us}}^{n_2}(y_0, y_1, \ldots, y_n).$$  

Similarly, the difference and the product can also be written as the evaluation of SB polynomials. Our arithmetic circuits therefore simply arise from substituting the representation from eq. 30 into the arithmetic operation and afterward encoding the resulting semi-Boolean polynomial by using the encoding circuit we constructed in section II i.e.:

$$U_{\text{add}} = U_{\text{shp}}(\Omega_{\text{us}}^{n_1}(x) + \Omega_{\text{us}}^{n_2}(y)), \quad (33)$$

$$U_{\text{sub}} = U_{\text{shp}}(\Omega_{\text{us}}^{n_1}(x) - \Omega_{\text{us}}^{n_2}(y)), \quad (34)$$

$$U_{\text{mult}} = U_{\text{shp}}(\Omega_{\text{us}}^{n_1}(x)\Omega_{\text{us}}^{n_2}(y)). \quad (35)$$

The circuits that come out of this algorithm have been known as Fourier-arithmetic and have been studied in [8], [9].

For an arbitrary, multivariate, integer coefficient polynomial $p : \mathbb{R}^k \rightarrow \mathbb{R}$, we can use that $p(\Omega_{\text{us}}(x), \Omega_{\text{us}}(y), \Omega_{\text{us}}(z), \ldots)$ is again an SB-polynomial which can therefore be encoded using eq. 15:

$$U_{\text{poly}}(p) = U_{\text{shp}}(p(\Omega_{\text{us}}^{n_1}(x), \Omega_{\text{us}}^{n_2}(y), \Omega_{\text{us}}^{n_3}(z), \ldots)). \quad (36)$$

Note that this circuit evaluates $p$ without the computation of any intermediate values making it very light on the qubit count.

III. ARITHMETIC

With the mathematical fundamentals and the SB-polynomial encoder at hand, we can now start constructing arithmetic circuits.

A. Unsigned integer arithmetic

Consider now 3 quantum registers with size $n_1, n_2, m \in \mathbb{N}$ and the integers $x < 2^{n_1}$ and $y < 2^{n_2}$. The goal of this section is to construct circuits that perform the following operations:

$$U_{\text{add}} |x\rangle |y\rangle |0\rangle = |x\rangle |y\rangle |(x + y) \mod 2^m\rangle,$$  

$$U_{\text{sub}} |x\rangle |y\rangle |0\rangle = |x\rangle |y\rangle |(x - y) \mod 2^m\rangle,$$  

$$U_{\text{mult}} |x\rangle |y\rangle |0\rangle = |x\rangle |y\rangle |(xy) \mod 2^m\rangle.$$  

Additionally, we will construct a technique that can encode an arbitrary multivariate integer coefficient polynomial (not semi-boolean) $p(x, y, z, \ldots)$, such that

$$U_{\text{poly}}(p) |x\rangle |y\rangle |z\rangle |0\rangle = |x\rangle |y\rangle |z\rangle |p(x, y, z, \ldots) \mod 2^m\rangle.$$  

B. Signed Integer Arithmetic

The above discussions construct the simple case of executing basic arithmetic on unsigned integers. However, it cannot deal with signed integers and the belonging operations. To treat negative values, the first question which arises is how to represent them. The most basic approach would be to add a sign bit $x_s$ which then indicates the sign:

$$\text{sign}(x) = \begin{cases} 1 & \text{if } x_s = 0 \\ -1 & \text{if } x_s = 1 \end{cases}.$$  

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In principle this approach might be a suitable approach for our techniques, however, a more detailed analysis uncovers many disadvantages for implementation on a quantum computer. For the multiplication of two numbers, is be straightforward to determine the sign bit of the result. The sign bit of the product can be determined by applying CNOT gates controlled on the sign bits of the factors. For sums the situation is already much more complicated: Imagine adding two numbers $x$, $y$, where one is positive and the other is negative. The sign of the sum depends on whether the $|x| \geq |y|$. Even though a comparison like this would in principle be possible to implement on a quantum computer, it is still very unwieldy. Furthermore, evaluating polynomials like eq. (2) would not be possible anymore, because every single monomial needs to be computed separately to determine its absolute value.

Given the above considerations, we pick a different encoding for negative numbers, which makes use of the modular structure of the unsigned integer arithmetic. With this approach, there is no need to construct extra circuits for the signed integer arithmetic and every operation for the unsigned case, directly translates to the signed case. The one thing which does change is the de/encoding of the corresponding numbers. To see how this works, we begin by defining the $n$-bit signed integer encoding ring isomorphism

$[\cdot]_n : \mathbb{Z}/2^n \mathbb{Z} \cup \mathbb{Z}/2^n \mathbb{Z} \to \mathbb{Z}/2^{n+1} \mathbb{Z},$

$$x \rightarrow \begin{cases} x & \text{if } x \geq 0 \\ 2^{n+1} - |x| & \text{else} \end{cases} \quad \text{(38)}$$

An intuitive understanding of what this does can be gained from viewing $\mathbb{Z}/12\mathbb{Z}$ as a clock-face. In this context, the numbers from $-6$ to $6$ are being represented on the clock. Positive values like $3$ or $4$ are being represented by themselves, whereas negative values are being represented by moving the pointer counterclockwise. We give some examples:

$$[0]_3 = 0, \quad \text{(39)}$$
$$[3]_3 = 3, \quad \text{(40)}$$
$$[-4]_3 = 16 - 4 = 12. \quad \text{(41)}$$

If we now want to execute an arithmetic operation on a signed integer $x$, we encode $[x]_n$ and execute the unsigned operation. If at some point we want to extract the results, we measure and simply apply the inverse of eq. (38):

$$[y]_{n-1}^{-1} = \begin{cases} y & \text{if } y < 2^n \\ y - 2^n & \text{else} \end{cases} \quad \text{(42)}$$

for this formalism to recover the signed result. We will now provide proof of why this works for handling signs. What is required to show is, that for two $n$-bit signed integers $x$, $y$, regardless of the constellation of signs, the following identities hold:

$$[x + y]_n \mod 2^{n+1} = ([x]_n + [y]_n) \mod 2^{n+1}, \quad \text{(43)}$$
$$[x - y]_n \mod 2^{n+1} = ([x]_n - [y]_n) \mod 2^{n+1}, \quad \text{(44)}$$
$$[xy]_n \mod 2^{n+1} = [x]_n[y]_n \mod 2^{n+1}. \quad \text{(45)}$$

Let $x < 0$ and $y \geq 0$ such that the multiplication does not result in an overflow, i.e. $|xy|$ can still be represented by an $n$-bit integer - otherwise increase $n$:

$$[x]_n[y]_n \mod 2^{n+1} = (2^{n+1} - |x|)y \mod 2^{n+1}$$
$$= (2^{n+1} - |x|)[y]_n \mod 2^{n+1}$$
$$= (-|x|)[y]_n \mod 2^{n+1}$$
$$= (2^{n+1} - |x|)[y]_n \mod 2^{n+1}$$
$$= [xy]_n \mod 2^{n+1}. \quad \text{(46)}$$

Here, we used that $2^{n+1}y$ is either 0 or an integer multiple of $2^{n+1}$ and thus vanishes after applying the modulus. In the following step, we added $2^{n+1}$ knowing that it also vanishes because of the modulus. The case where both $x$ and $y$ are non-negative is trivial because this is just unsigned integer multiplication. What remains to be shown, is the case where both $x$ and $y$ are negative:

$$[x]_n[y]_n \mod 2^{n+1} = (2^{n+1} - |x|)(2^{n+1} - |y|) \mod 2^{n+1}$$
$$= (2^{2(n+1)} - 2^{n+1}(|x| + |y|) + |x||y|) \mod 2^{n+1}$$
$$= |x||y| \mod 2^{n+1}$$
$$= xy \mod 2^{n+1}$$
$$= [xy]_n \mod 2^{n+1}. \quad \text{(47)}$$

In some situations, the following formula comes in more handy than eq. (38):

$$[x]_n = x \mod 2^{n+1}. \quad \text{(48)}$$

One such situation is proving the addition-equivalent of the above identities. Let $x$, $y$ be arbitrary signed $n$-bit integers

$$[x + y]_n \mod 2^{n+1} = (x + y) \mod 2^{n+1}$$
$$= (x \mod 2^{n+1} + y \mod 2^{n+1}) \mod 2^{n+1}$$
$$= ([x]_n + [y]_n) \mod 2^{n+1}. \quad \text{(49)}$$

The case of subtraction works the same. With this at hand, we can describe the signed integer arithmetic circuits.

For this, we assume for now, that all participating registers have size $n$. We will shortly lift this restriction. Furthermore, let $x$, $y$, $z$ again be signed $n$-bit integers

$$U_{add} [x]_n [y]_n |0\rangle = ([x]_n + [y]_n) |0\rangle + ([x]_n + [y]_n) \mod 2^{n+1})$$
$$= |[x]_n + [y]_n \mod 2^{n+1}\rangle. \quad \text{(50)}$$

Similarly, for the multiplication, subtraction, and polynomial encoding we get

$$U_{mult} [x]_n [y]_n |0\rangle = ([x]_n)[y]_n |[x - y]_n \mod 2^{n+1}\rangle,$$

$$U_{poly}(p) [x]_n [y]_n |z]_n \ldots |p(x,y,z\ldots)\rangle \mod 2^{n+1}. \quad \text{(51)}$$

To provide an explicit example suppose we want to multiply the 3-bit signed integers $-3$ and $2$. Then we first encode
We now use the SB-polynomial from eq. (56) instead of eq. (31) to encode signed arithmetic on registers with size \( n_1, n_2, m \)

\[
\begin{align*}
U_{\text{add}}^{n_1, n_2, m} & = U_{\text{sbp}}(\Omega_{\text{IE}}^{n_1, m}(x) + \Omega_{\text{IE}}^{n_2, m}(y)), \\
U_{\text{sub}}^{n_1, n_2, m} & = U_{\text{sbp}}(\Omega_{\text{IE}}^{n_1, m}(x) - \Omega_{\text{IE}}^{n_2, m}(y)), \\
U_{\text{mult}}^{n_1, n_2, m} & = U_{\text{sbp}}(\Omega_{\text{IE}}^{n_1, m}(x) \Omega_{\text{IE}}^{n_2, m}(y)).
\end{align*}
\]

Applying the multiplication to the state \([x]_{n_1}, [y]_{n_2}, 0\) then yields

\[
\begin{align*}
[x]_{n_1}, [y]_{n_2}, 0 & \rightarrow [x]_{n_1} \Omega_{\text{IE}}^{n_1, m}(x) \Omega_{\text{IE}}^{n_2, m}(y) \mod 2^{m+1}), \\
[x]_{n_1}, [y]_{n_2}, 0 & \rightarrow [x]_{n_1} [y]_{n_2} \mod 2^{m+1}), \\
[x]_{n_1}, [y]_{n_2}, 0 & \rightarrow [x]_{n_1} [y]_{n_2} m \mod 2^{m+1}).
\end{align*}
\]

In the first equality, we used the functionality of the SB-polynomial encoder eq. (15). The second equality is eq. (57) and the last equality is eq. (45) and using the fact that we assume suited register sizes to prevent overflow for the given multiplication. Eq. (67) shows that the concept of the image extended SB-polynomial \( \Omega_{\text{IE}}^{n, m} \) yields the desired results for flexible register size arithmetic.

### D. Floating-Point Arithmetic

The last step for full floating-point arithmetic is encoding for the arithmetic of non-integers. For this, we will use the following representation: Let \( x \in \mathbb{Q} \) be a rational such that its binary representation is finite (ie. not something like 0.01). Then there exist integers \( k, l \in \mathbb{Z} \) such that

\[
x = \pm \sum_{i=k}^{l} 2^ix_i,
\]

where \( \forall k \leq i \leq l : x_i \in \mathbb{F}_2 \). We write this as

\[
x = \pm 2^k,
\]

where \( \pm \) is a signed \( n = k + l \) bit integer. We call \( k \) the exponent and \( \pm \) the mantissa of \( x \). Even though it would be straightforward to encode both mantissa and exponent as quantum variables, performing arithmetic operations on such a bi-quantum encoding does not turn out as simple. To perform the addition of two bi-quantum encoded floats, the mantissa would have to be bit shifted depending on the state of the exponent register. Such a circuit could in principle be constructed using Fredkin gates\(^8\) in combination with an incrementor gate\(^9\) however it would be very unwieldy. The data-format we are about to construct does not need such quantum-conditioned bit shifting because only the mantissa is quantum - the exponent is a classically known number. We call this property mono-quantum encoding.

We extend the \([\cdot]\) notation:

\[
[x]_n := [x]_n = [2^{-k}x]_n.
\]

\(^8\)A Fredkin gate is a controlled SWAP gate

\(^9\)An incrementor gate is a gate that when applied to an \( n \)-qubit register, performs the operation \(|x\rangle \rightarrow |x + 1 \mod 2^n\rangle\)
We will now prove an identity that is required later (in eq. (72)). Let $0 \leq j \in \mathbb{N}_0$ we then have

$$2^j [x]_n \mod 2^{n+1} = \begin{cases} 2^j x \mod 2^{n+1} & \text{if } x \geq 0 \\ (2^{j+n+1} - 2^j x) \mod 2^{n+1} & \text{else} \end{cases}$$

$$= \begin{cases} 2^j x \mod 2^{n+1} & \text{if } x \geq 0 \\ (2^{n+1} - 2^j x) \mod 2^{n+1} & \text{else} \end{cases}. \quad (65)$$

Simply plugging the SB-polynomials of the mantissa into the SB-polynomial encoder (as we did in the previous sections) however, does not suffice because we only defined the SB-polynomial encoder for integer coefficients. In order to still be able to encode non-integer values, our solution is to bit shift the polynomial (ie. multiply by a power of two) such that all its coefficients are integers. This bit shift will be reversed when decoding a measurement outcome. For this, we introduce a new notation for the SB-polynomial encoder. Consider an arithmetic operation writing into a target register with exponent $k_0$. The bit shifted SB-polynomial encoder is now defined as

$$U_{\text{sbp}}^{k_0} (\Omega) := U_{\text{sbp}} (2^{-k_0} \Omega). \quad (66)$$

This allows us to conveniently write down the encoding of the mantissa into the target register. Similarly, we extend the notation of the encoding SB-polynomial to account for the fact that they have to turn the boolean array of the mantissa $x$ into the actual value $x$. For this, consider a domain register $x$ with size $n_1$ and exponent $k_1$:

$$\Omega^{n_1,m,k_1} (x) := 2^{k_1} \Omega^{n_1,m} (x). \quad (67)$$

Using these definitions, it is once again possible to write down arithmetic circuits for floating-point operations. For this we assume that the relevant registers have sizes $n_0, n_1, n_2, \ldots$ and exponents $k_0, k_1, k_2, \ldots$. The resulting arithmetic circuits can be summarized as follows:

$$U_{\text{add}} = U_{\text{sbp}}^{k_0} (\Omega^{n_1,n_0,k_1} (x) + \Omega^{n_2,n_0,k_2} (y)), \quad (68)$$

$$U_{\text{sub}} = U_{\text{sbp}}^{k_0} (\Omega^{n_1,n_0,k_1} (x) - \Omega^{n_2,n_0,k_2} (y)), \quad (69)$$

$$U_{\text{mult}} = U_{\text{sbp}}^{k_0} (\Omega^{n_1,n_0,k_1} (x) \Omega^{n_2,n_0,k_2} (y)). \quad (70)$$

Note that the target registers have certain requirements regarding their exponents, in order to ensure that only integer SB-polynomials are handed to the non-bit shifted SB-polynomial encoder. For instance, if we want to multiply two numbers with exponents $k_1, k_2$, the smallest possible outcome is $2^{k_1+k_2}$. Hence, the target register needs to have an exponent of $k_0 \leq k_1 + k_2$. Anything above this threshold can not support the result of the $2^{k_1} \times 2^{k_2}$ multiplication.

To summarize, the following rules are valid for shape determination:

- Addition: $k_0 \leq \min(k_1, k_2)$
- Multiplication: $k_0 \leq k_1 + k_2$

These techniques also generalize to the arbitrary polynomial circuit eq. (64). Note that we can lift the restriction of integer coefficients as long as the bit shifted SB-polynomial

$$2^{-k_0} p((\Omega^{n_1,n_0,k_1} (x), \Omega^{n_2,n_0,k_2} (y), \Omega^{n_3,n_0,k_3} (z), \ldots)) \quad (71)$$

contains only integer coefficients.

The following is an example for a floating-point arithmetic circuit evaluation for the multiplication of two floats with different data shapes:

$$U_{\text{mult}} ([x]^{n_1}_2 | [y]^{n_2}_2 | 0) = U_{\text{mult}} ([2^{-k_1} x]_n | [2^{-k_2} y]_n | 0)$$

$$= ([2^{-k_1} x]_n | [2^{-k_2} y]_n | 0)$$

$$= ([2^{-k_0} \Omega^{n_1,n_0,k_1} (2^{-k_1} x)_n \Omega^{n_2,n_0,k_2} (2^{-k_2} y)_n] \mod 2^{n_0+1})$$

$$= ([x]^{n_1}_2 | [y]^{n_2}_2 | 2^{-k_0+k_1+k_2} [2^{-k_1} x]_n [2^{-k_2} y]_n) \mod 2^{n_0+1})$$

$$= ([x]^{n_1}_2 | [y]^{n_2}_2 | 2^{-k_0+k_1+k_2} [2^{-k_1+k_2} x y]_n) \mod 2^{n_0+1})$$

$$= ([x]^{n_1}_2 | [y]^{n_2}_2 | [x y]^{k_0}_n) \mod 2^{n_0+1}) \quad . \quad (72)$$

As usual, we assume that the register sizes are chosen that neither an overflow nor an underflow is happening. Let’s recapitulate what identities were used here

1. Application of definition of $[\cdot]$ for non-integers eq. (64)
2. The bit shifted SB-polynomial encoder eq. (65)
3. Evaluation of the image extended SB-polynomials eq. (66)
4. Multiplicative morphism property of $[\cdot]$ eq. (45)
5. Applying eq. (65) with $k_0 \leq k_1 + k_2 \iff -k_0 + k_1 + k_2 \geq 0$
6. Again eq. (64) (this time backward)

IV. IN-PLACE OPERATIONS

A significant disadvantage of the methods described in section III is that we always need a new register to store our results. This is the case for many quantum operations, in order to ensure the reversibility of the circuits. However, certain arithmetic operations are reversible by themselves and in principle it should be possible to implement them in-place i.e., operating only on the domain register and not requiring a target register. In order to reduce the complexity of the equations in this section, the presentation focuses on the unsigned integers and omits the variety of indices relating to the register sizes and exponents. However, all of the considerations in this section can also be performed with full floating-point arithmetic.

A. In-place Addition

Since modular addition is a reversible operation, implementing it in-place poses no major challenge. Indeed, it can be easily recognized that the initial $\textbf{H}$ gates of the SB-polynomial encoder can be interpreted as a streamlined\textsuperscript{10} version of a QFT that only acts on the $|0\rangle$ state

$$\textbf{H} |0\rangle = \frac{1}{\sqrt{2^n}} \sum_{k=0}^{2^n-1} |k\rangle$$

$$\frac{1}{\sqrt{2^n}} \sum_{k=0}^{2^n-1} \exp\left(\frac{2\pi i 0k}{2^n}\right) |k\rangle \quad (73)$$

$$= \text{QFT} |0\rangle .$$

\textsuperscript{10}“Streamlined” in this context means a more efficient version which is only valid if the input state is $|0\rangle$
We present an example calculation for the case if in-place multiplication is supposed to happen. Basically, with the general form of a QFT yields the desired result:

\[ U_{\text{in-place}}(\Omega(x)) = \text{QFT}^\dagger U_G(\Omega(x)) \text{QFT}. \]  

(74)

Here, the Fourier-transformations are applied onto the register, where the in-place operation is supposed to happen. Simply replacing \( H^n \) in the SB-polynomial encoder (eq. (25)) with the general form of a QFT yields the desired result:

\[ U_{\text{in-place}}(\Omega(x)) = \text{QFT}^\dagger U_G(\Omega(x)) \text{QFT}. \]  

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Simply replacing \( H^n \) in the SB-polynomial encoder (eq. (25)) with the general form of a QFT yields the desired result:

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(74)

Here, the Fourier-transformations are applied onto the register, where the in-place operation is supposed to happen. Basically, everything discussed before - regarding sign and exponent treatment - now directly translates to this setting:

\[ U_{\text{in-place}}(\Omega(x)) = \text{QFT}^\dagger U_G(\Omega(x)) \text{QFT}. \]  

(74)

We present an example calculation for the case if in-place additions on two registers in a computational basis state \(|x\rangle\langle y|\) with sizes \(n, m\) are performed:

\[ U_{\text{add}} = U_{\text{in-place}}(\Omega(x)) = \text{QFT}^\dagger U_G(\Omega(x)) \text{QFT}. \]  

(75)

Fig. 2: (a) The circuit for the regular QFT. (b) The circuit for QFT in-place multiplication with \(a = 3\).

B. In-place Multiplication

It is well known that every quantum operation has to be invertible - this is because all the elementary gates that are available to us are invertible, implying that every sequence of them is also invertible. For an arbitrary modular in-place multiplication this is however unfortunately not the case. For instance, we have:

\[ (2 \times 7) \mod 8 = 6 \mod 8 \]  

(79)

\[ (2 \times 3) \mod 8 = 6 \mod 8 \]  

(80)

If we are only given the result 6 and the fact that our operation was a 2-multiplication, we can’t infer which was the initial value. In fact, this is the reason why our modular arithmetic in \(\mathbb{Z}/2^n\mathbb{Z}\) is a ring and not a field because not all of its elements possess an inverse. The following theorem addresses the invertibility of elements in \(\mathbb{Z}/2^n\mathbb{Z}\).

**Theorem 1:** Let \(n \in \mathbb{N}\) and \(a \in \mathbb{Z}/2^n\mathbb{Z}\). We then have

\[ a \text{ invertible in } \mathbb{Z}/2^n\mathbb{Z} \iff a \mod 2 = 1 \]  

(81)

**Proof:** According to Bézout’s lemma [11], the condition of \(a\) being invertible is that

\[ \gcd(a, 2^n) = 1, \]  

(82)

where \(\gcd\) denotes the greatest common divisor function. In our case this is easily evaluated because the only prime factor of \(2^n\) is 2, implying \(a\) is invertible if 2 is not a prime factor of \(a\). This is equivalent to 2 being an odd number.

This implies that only circuits performing modular multiplications with odd numbers are reversible and can get executed in-place. Hence, the question emerges of how such circuits can be generated.
We conclude:

According to Nielsen & Chuang eq. (5.5-5.10) [7] we have

\[
\text{QFT} |ax\rangle = \frac{1}{\sqrt{2^n}} \bigotimes_{l=0}^{n-1} \left( |0\rangle + \exp \left( \frac{2\pi i a x}{2^{l+1}} \right) |1\rangle \right)
\]

Note that for index constellations where \( k > l \), the phase is an integer multiple of \( 2\pi \). Hence we can simplify

\[
\text{QFT} |ax\rangle = \frac{1}{\sqrt{2^n}} \bigotimes_{l=0}^{n-1} \left( |0\rangle + \exp \left( \frac{2\pi i a x}{2^{l+1}} \right) |1\rangle \right) \quad (83)
\]

Similar to the regular quantum Fourier-transform, this equation shows how the phases of the corresponding qubits are successively synthesized: The \( |1\rangle \) state of the \( l \)-th qubit receives a phase if the \( k \)-th qubit is also in the \( |1\rangle \) state because only then \( x_k = 1 \) (otherwise we have \( x_k = 0 \)). This is done by performing controlled phase gates on these qubits. To turn this into an in-place multiplication, we will therefore simply perform a QFT whilst substituting any occurring CP(\( \phi \)) gates with CP(\( a\phi \)) gates. For an example circuit check fig. [2]. There is however still one extra case left to be considered. If \( l = k \), the gate which would apply the phase \( x_k\pi \) in the regular QFT, is the H gate on the \( k \)-th qubit:

\[
H |x_k\rangle = \frac{1}{\sqrt{2}} (|0\rangle + \exp(i\pi x_k) |1\rangle). \quad (85)
\]

Since there is no such gate that would perform the same transformation but with a phase of \( \pi x_k \), this might cause problems. This is however easily resolved, because we assumed that \( a \) is invertible, implying \( a \) mod \( 2 = 1 \). Therefore

\[
(x_k a) \text{ mod } 2 = (x_k \text{ mod } 2) (a \text{ mod } 2) = x_k \text{ mod } 2. \quad (86)
\]

Implying \( x_k\pi \) and \( ax_k\pi \) correspond to the same phase shift. We conclude:

\[
\text{QFT} U^{\text{in-place}}_{\text{mul}} (a) = \frac{1}{\sqrt{2^n}} \text{SW} \prod_{l=0}^{n-1} \left( \prod_{k=0}^{l-1} \text{CP}_{x_k x_k} \left( \frac{2\pi i a 2^k}{2^{l+1}} \right) H_{x_k} \right), \quad (87)
\]

where SW denotes the swap gates, which are executed as usual. Note that even though this notation might suggest that \( U^{\text{in-place}}_{\text{mul}} (a) \) could in principle be a standalone circuit, this is not the case - the in-place multiplication can only happen during a QFT.

We choose this notation to capture its functionality, which is

\[
\text{QFT} U^{\text{in-place}}_{\text{mul}} (a) |x\rangle = \text{QFT} (ax \text{ mod } 2^n). \quad (88)
\]

For an example, see fig. [2].

C. Semi-in-place multiplication

The restriction of only being able to perform odd number in-place multiplication can be at least partially lifted. For this, we note that a \( 2^k \) multiplication is the same as a \( k \)-bit shift into the more significant direction. This can be achieved via a compiler pass for increasing the exponent of the float in question by \( k \). To perform in-place multiplication with an arbitrary (classically known) integer \( a \), we, therefore, follow the following protocol

- Factorize \( a \) (on the classical computer) such that \( a = b2^k \), where \( b \) is odd.
- Add \( k \) to the exponent of the quantum float in question.
- Perform in-place multiplication with \( b \) as discussed in section [IV-B].

Even though this method in principle allows arbitrary number multiplication, it comes with some drawbacks

- It is still not possible to perform in-place multiplication with a number encoded in another quantum register.
- The \( 2^k \) multiplication does not follow the modular arithmetic, while the \( b \) multiplication does, which results in a complicated overflow behavior.

To be more specific, consider the example \( a = 6 = 3 \cdot 2^1 \) which will be in-place multiplied on the state unsigned integer state \(|7\rangle_{\text{fr}} \). Since the register size is 4, the maximum number which can get represented is \( 2^4 - 1 = 15 \), implying the mantissa multiplication \( 3 \cdot 7 = 21 \) results in overflow. Following the above protocol we have

\[
U^{\text{semi-in-place}}_{\text{mul}} (6) |7\rangle_{\text{fr}} = |3 \cdot 7\rangle_{\text{fr}} \quad (89)
\]

If we now measure and decode, we get the result

\[
((3 \cdot 7) \text{ mod } 2^4) \cdot 2^1 = 10, \quad (90)
\]

which is rather uninformative. Note that this only causes problems, if the mantissa multiplication results in overflow: If we instead multiplied \( a = 6 \) on \(|3\rangle_{\text{fr}} \), the correct result would be to be 18, which is still more than 15. However the mantissa multiplication \( 3 \cdot 3 = 9 \) yields no overflow, so we still acquire the correct result

\[
((3 \cdot 3) \text{ mod } 2^4) \cdot 2^1 = 18. \quad (91)
\]

A CP gate is a controlled phase gate.
we want to encode the monomial (asymptotically)\[50%

The CNOT/RZ gate count for the (un)computation of the
truth value of the ancilla qubit can furthermore be reduced by
improvements obviously rapidly grows, once we have a target
register with more than three qubits.

Another important factor for circuit depth reduction is the
order, in which monomials are encoded. An example for why
this makes a difference is depicted in fig. (7). To understand
how much of an impact this can make, we note that the worst
order we could find, has roughly about 17 times the depth
of the best order we could find for a 32-bit unsigned integer
multiplication. Our general approach for determining a suited
order we could find, has roughly about

D. Monomial encoding order

Another important factor for circuit depth reduction is the
order, in which monomials are encoded. An example for why
this makes a difference is depicted in fig. (7). To understand
how much of an impact this can make, we note that the worst
order we could find, has roughly about 17 times the depth
of the best order we could find for a 32-bit unsigned integer
multiplication. Our general approach for determining a suited
order, is to evaluate a cost function \(C(\Omega_m)\) for each monomial
\(\Omega_m\) in each step and choose the monomial with the smallest
cost for that particular iteration. We evaluated several cost
functions and found that

\[C(\Omega_m) = \max\{d_x \mid x \in \text{Vars}(\Omega_m)\}\]  (92)
produces the best results. Here, \( \text{Vars}(\Omega_m) \) denotes the set of variables of \( \Omega_m \) (i.e., \( \text{Vars}(\{x_0, x_1, x_3\}) = \{x_0, x_1, x_3\} \)) and \( d_x \), the depth of the qubit[12] associated to \( x_i \).

E. Entanglement via Global Mølmer-Sørensen gates

One of the interesting perks of ion-trap architectures is that they are able to perform multiple two-qubit entangling operations within one laser pulse[13]. These operations are frequently called Global Mølmer-Sørensen gates. The unitary matrix describing a GMS gate on \( n \) qubits is determined by a symmetric \( n \times n \) matrix \( \chi \) indicating XX interactions:

\[
\text{GMS}(\chi) = \exp\left(-\frac{i}{2} \sum_{i=0}^{n-1} \sum_{j=i+1}^{n-1} \chi_{ij} X_i \otimes X_j \right) \tag{93}
\]

An important distinction that has to be made is whether the entries of \( \chi \) are uniform[10] or not. The uniform case has been demonstrated in[13] - the non-uniform case has not been realized on a physical backend to the best of our knowledge, however we still include it’s treatment in case of future progress on this field.

Using the techniques described in[14], we can perform every single entangling operation using GMS gates. We will see that the requirement of uniform GMS gates only increases the amount of entangling operations by a constant factor (compared to allowing arbitrary \( \chi \)). This is possible because many parameters can be inserted into the circuit via parametrized single qubit gates.

For this, we note that the SBP-encoder consists of three types of entangling operations:

1) (Un)computing the ancilla qubit in fig. 5
2) Performing the \( U_G \) gate controlled on the ancilla qubit
3) Entangling operations contained in the QFT

Regarding the first type, we refer to[14] which provides circuits for 2 and 3 controlled X gates. This obviously restricts the maximum degree of the SB-polynomials to 3, however we note that many important applications (such as multiplication, addition or subtraction) only require degree 2 or lower. Therefore, we leave the efficient synthesis of \( \geq 4 \) controlled X gates using only GMS entangling operations as an open research question.

For the second and third type we note that both are of the shape of multiple successive CP gates, where one knob is always on the same qubit but the others evenly distributed on the other qubits. We will denote circuits of this kind as ascending CP sequences - for an example check fig. 8. We will now construct a technique that can execute ascending CP sequences, but also any other CP sequence with only a single non-uniform GMS gate (+some single qubit gates).

For a single CP gate acting on the two-qubit computational basis state \( |xy\rangle \), where \( x, y \in \{0, 1\} \), the applied phase reads

\[
\text{CP}_{ab}(\phi) |xy\rangle = \exp(i\phi) |xy\rangle
\]

\[
= \exp\left(\frac{i\phi}{2}(x + y - (x \oplus y))\right) |xy\rangle
\]

\[
= \exp\left(\frac{i\phi x}{2}\right) \exp\left(\frac{i\phi y}{2}\right) \exp\left(i\frac{\phi(1 - (1)^{x+y})}{4}\right) |xy\rangle
\]

\[
= P_a \left(\frac{\phi}{2}\right) P_b \left(\frac{\phi}{2}\right) \exp\left(i\frac{\phi}{4} Z_a \otimes Z_b\right) \exp\left(i\frac{\phi}{4}\right) |xy\rangle, \tag{94}
\]

where we used

\[
2xy = x + y - (x \oplus y), \forall (x, y) \in \{0, 1\}^2 \tag{95}
\]

with the mod 2 addition denoted by \( \oplus \). Since we proved in eq. [10] for a complete base of \( (\mathbb{C}^2)^{\otimes 2} \), we have a valid operator identity:

\[
\text{CP}(\phi)_{ab} = P_a \left(\frac{\phi}{2}\right) P_b \left(\frac{\phi}{2}\right) \exp\left(i\frac{\phi}{4} Z_a \otimes Z_b\right) \exp\left(i\frac{\phi}{4}\right) \tag{96}
\]

Furthermore, since every operator in \[96\] commutes, we conclude that any sequence of CP gates \( \text{CP}_{a_0 b_0}(\phi_0), \ldots, \text{CP}_{a_m b_m}(\phi_m) \) on \( n \) qubits can be represented by the unitary

\[
\prod_{i=0}^{m} \text{CP}_{a_i b_i}(\phi_i)
\]

\[
= \exp(i\Omega) \prod_{i=0}^{n-1} P_i(\omega_i)
\]

\[
\cdot \exp\left(-\frac{i}{2} \sum_{i=0}^{n-1} \sum_{j=i+1}^{n-1} \chi_{ij} Z_i \otimes Z_j \right) \tag{97}
\]

\[
= \exp(i\Omega) \prod_{i=0}^{n-1} P_i(\omega_i)
\]

\[
\cdot \exp\left(-\frac{i}{2} \sum_{i=0}^{n-1} \sum_{j=i+1}^{n-1} \chi_{ij} H^{\otimes n}(X_i \otimes X_j)H^{\otimes n} \right)
\]

\[
= \exp(i\Omega) \prod_{i=0}^{n-1} P_i(\omega_i) H^{\otimes n} \text{GMS}(\chi) H^{\otimes n},
\]

where we used that for any linear operator \( A \)

\[
H \otimes^n \exp(iA)H^{\otimes n} = H \otimes^n \sum_{k=0}^{\infty} \frac{(iA)^k}{k!} H^{\otimes n}
\]

\[
= \sum_{k=0}^{\infty} \frac{(iH \otimes^n A H^{\otimes n})^k}{k!}
\]

\[
= \exp(iH \otimes^n A H^{\otimes n}) \tag{98}
\]

[12] To define the depth of a qubit \( q \), we divide the containing circuit \( C \) (as with usual depth definition) into a sequence of time steps. During each time step, each qubit can execute at most one gate. The depth of \( q \) is then defined as the amount of time steps until the final gate on \( q \) is executed. Therefore we have the following formula for the depth of the circuit: \( D_C = \max\{d_y/q \text{ is qubit in } C\} \).

[13] Uniform denotes that \( \forall i, j : \chi_{ij} = c \) for some constant \( c \).
Fig. 7: Two different orders of monomial encoding for the SB-polynomial \( \Omega(x) = x_0 + 2x_1x_2 + 3x_0x_1 \). We assume here that the techniques from section (V-C) are used to execute the controlled \( U_G \) gates in parallel. Note that (7a) allows faster execution because the ancillas for \( U_G(1) \) and \( U_G(2) \) can be computed in parallel. This is not the case for (7b). Here, the computation of the corresponding ancillas awaits the conclusion of the previous controlled \( U_G \) gate in every step.

\[
|0 \rangle^{\otimes 3} \rightarrow H |0 \rangle \rightarrow U_G(1) \rightarrow U_G(2) \rightarrow U_G(3) \rightarrow \text{QFT}^\dagger
\]

(a)

\[
|0 \rangle^{\otimes 3} \rightarrow H |0 \rangle \rightarrow U_G(1) \rightarrow U_G(2) \rightarrow U_G(3) \rightarrow \text{QFT}^\dagger
\]

(b)

Fig. 8: Apart from multi-controlled X gates, every entangling operation of the SBP-encoder is of this shape

The formulas for the parameters are

\[
\omega_i = \sum_{k \leq m} \frac{\phi_k}{2}, \quad \chi_{ij} = -\sum_{k \leq m} \frac{\phi_k}{2}, \quad \Omega = \sum_{k \leq m} \frac{\phi_k}{4}. \tag{99}
\]

In case the hardware only supports uniform GMS gates, arbitrary CP sequences are no longer easily encodable, however, ascending CP sequences still are. For this, we write out the decomposition of a CP gate into CNOT gates:

\[
P(\phi) = P \left( \frac{\phi}{2} \right) P \left( -\frac{\phi}{2} \right) P \left( \frac{\phi}{2} \right)
\]

Applying this to an ascending CP sequence yields

\[
P(\phi_1) P(\phi_2) P(\phi_3) P(\phi_4)
\]

\[
P \left( \sum_i \frac{\phi_i}{2} \right) P \left( -\frac{\phi_1}{2} \right) P \left( \frac{\phi_1}{2} \right)
\]

\[
P \left( -\frac{\phi_2}{2} \right) P \left( \frac{\phi_2}{2} \right)
\]

\[
P \left( -\frac{\phi_3}{2} \right) P \left( \frac{\phi_3}{2} \right)
\]

\[
P \left( -\frac{\phi_4}{2} \right) P \left( \frac{\phi_4}{2} \right)
\]

Such sequences of CNOT gates, with a single control and multiple targets are called \textit{fan-out} gates and can be realized with two uniform GMS gates according to [15]. Since we need two fan-out gates, we end up with 4 GMS gates per ascending CP sequence.
F. Complexity analysis

To estimate the performance of the processing of arithmetic operands of magnitude $N \in \mathbb{N}$, we separate the SBP-encoder into three steps

1) Initial H gates / Fourier transform (in the case of in-place operations)
2) (Controlled) $U_G$-application
3) Fourier transform

The initial H gates can be executed in constant time. The Fourier transform can be done in $O(\log(N)^2)$. If the hardware provides access to GMS gates, this reduces to $O(\log(N))$, as there is one ascending CP sequence per qubit.

In order to estimate the complexity of a single controlled $U_G$ gate, we note that (un-)computing the truth value of the ancilla qubit (see section (V-A)) can be done in constant time.

The next step is the application of an ascending CP sequence which has complexity $O(\log(N))$ for a CNOT based implementation and $O(1)$ for GMS based implementations. We now estimate how many controlled $U_G$ we have to apply. In the case of an addition the SB-polynomial is

$$\Omega_{\text{add}}(x, y) = \sum_{i=0}^{n_1-1} 2^i x_i + \sum_{j=0}^{n_2-1} 2^j y_j,$$

which implies $O(\log(N))$ monomials. For multiplications we have

$$\Omega_{\text{mult}}(x, y) = \left( \sum_{i=0}^{n_1-1} 2^i x_i \right) \times \left( \sum_{j=0}^{n_2-1} 2^j y_j \right).$$

This yields $O(\log(N)^2)$ monomials, as we have to iterate over every combination of $(i, j)$ $i < n_1, j < n_2$. From this, we conclude that in the case of addition, the controlled $U_G$-application step can be performed in $O(\log(N)^2)$ (GMS: $O(\log(N))$) and in the case of multiplication we have $O(\log(N)^3)$ (GMS: $O(\log(N)^2)$).

The final Fourier transform has the same complexity as the initial thus leaving the complexity valid without modification. We summarize the results of our estimations in table I.

| Operation | CNOT complexity | GMS complexity |
|-----------|-----------------|----------------|
| Addition  | $O(\log(N)^2)$  | $O(\log(N))$  |
| Multiplication | $O(\log(N)^3)$  | $O(\log(N)^2)$ |
| Deg. $k$ Polynomial | $O(\log(N)^{k+1})$ | $O(\log(N)^k)$ |

TABLE I: Gate-count complexity estimation of different arithmetic operations using either CNOT or global Mølmer-Sørensen gates as elementary entangling gates

VI. CRITICAL POINTS

A valid point of criticism is the fact that ripple-carry adder based implementations of arithmetic evaluations scale as $O(\log(N))$ for additions and $O(\log(N)^2)$ for multiplications (check section ([1-1])) and therewith better compared to our approach. Apart from the possibility to reduce the complexity using GMS gates, this can be addressed by noting that the determined complexities are only valid regarding the gate count and not the depth. As it turns out (see fig [14]), the depth (and with it the execution speed) is significantly lower than ripple-carry adder based implementations, since it can be reduced by one factor of $\log(N)$ for each operation type.

To see how this works, we assume that the target register has a size of the order of $n_{\text{target}} \approx \log(N)$. We then allocate $n_{\text{target}}$ ancilla qubits and apply the technique described in section ([V-C]). This allows parallel execution of $n_{\text{target}} \approx \log(N)$ controlled $U_G$ gates, implying an improvement in execution speed by this factor.

Another point of criticism is constituted by the fact that with growing factor size, the RZ gate phases in the $U_G$ and QFT gates become exponentially small. Assuming only finite physical RZ gate precision this implies an upper limit for the operand size. For multiplications, the speed of our methods can however still be harnessed by reducing the problem into smaller multiplications using Karatsuba’s divide-and-conquer algorithm [16]. This however comes at the cost of additional ancilla qubits for storing intermediate results.

VII. CONCLUSIONS

In this work, we presented the design and handling of various types of arithmetic operations. For unsigned integer arithmetic, we constructed our circuits based on the idea that such evaluations can be written as SB-polynomials. Our way of encoding signed integers allows for an efficient operation evaluation since it can be reduced to the unsigned integer arithmetic circuits. We furthermore extended our algorithm/encoding by the possibility to inter-operate between registers of different sizes. Regarding the representation of non-integers, it turns out that encoding both the mantissa and the exponent as quantum variables (bi-quantum encoding) is in principle possible but only at the cost of highly increased circuit complexity. Instead, we store the exponent as a classical value (mono-quantum encoding) which again enables us to profit from the efficient unsigned integer circuits. Values encoded by our method can also be processed using other types of algorithms which perform modular arithmetic since there is no other specific requirement than the modular overflow behavior. Subsequently, we demonstrate methods to perform in-place operations, which can both save on qubits and prevent the necessity of uncomputation operations.

Finally, we discuss several implementation improvements for the SB-polynomial encoder. Probably most outstanding is the possibility to perform every entangling operation using ion-trap native GMS gates. These gates allow the entanglement of more than two qubits within a single pulse, which enables a reduction in entangling gate count by a factor of $O(\log(N))$. We estimate our circuit complexity and find that CNOT based implementations of addition and multiplication circuits are asymptotically more expensive in gate count by one factor of $O(\log(N))$ compared to ripple-carry based approaches. This is however overshadowed by the fact that encoding SB-polynomials can be performed with many parallel gate executions. Using this we could show that regarding depth (and with that speed), our approach has no extra $O(\log(N))$ factor and furthermore provides a speed-up with a factor of more than 900% (compared to carry ripple approaches).
Fig. 9: Depth of the resulting circuits from an unsigned integer multiplication of our method compared to two other ripple-carry adder based multiplication approaches ([3], [17]). For implementation specifics check section (I-A). At 32 bit, the resulting depth of the SBP encoder is only 10.7% of the depth of the ripple-carry based approaches. Note that we chose the target register size as minimal as possible without risking overflow. The depths are calculated after transpiling the circuits into the gate set \{CX, RZ, SX\}. The circuit construction, transpilation (optimization level 2) and evaluation was performed using IBM’s Qiskit [18].

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