SpinAPS: A High-Performance Spintronic Accelerator for Probabilistic Spiking Neural Networks

Anakha V Babu\textsuperscript{a}, Osvaldo Simeone\textsuperscript{b}, Bipin Rajendran\textsuperscript{b,*}

\textsuperscript{a}Department of Electrical and Computer Engineering, New Jersey Institute of Technology, NJ, 07102 USA
\textsuperscript{b}Department of Engineering, Kings College London, Kings College London, WC2R 2LS, UK

Abstract

We discuss a high-performance and high-throughput hardware accelerator for probabilistic Spiking Neural Networks (SNNs) based on Generalized Linear Model (GLM) neurons, that uses binary STT-RAM devices as synapses and digital CMOS logic for neurons. The inference accelerator, termed “SpinAPS” for Spintronic Accelerator for Probabilistic SNNs, implements a principled direct learning rule for first-to-spike decoding without the need for conversion from pre-trained ANNs. The proposed solution is shown to achieve comparable performance with an equivalent ANN on handwritten digit and human activity recognition benchmarks. The inference engine, SpinAPS, is shown through software emulation tools to achieve 4× performance improvement in terms of GSOPS/W/mm\textsuperscript{2} when compared to an equivalent SRAM-based design. The architecture leverages probabilistic spiking neural networks that employ first-to-spike decoding rule to make inference decisions at low latencies, achieving 75% of the test performance in as few as 4 algorithmic time steps on the handwritten digit benchmark. The accelerator also exhibits competitive performance with other memristor-based DNN/SNN accelerators and state-of-the-art GPUs.

Keywords: Spiking Neural Network (SNN); Artificial Neural Networks (ANNs); Generalized Linear Model (GLM); Spin-Transfer-Torque Random

\textsuperscript{*}Corresponding author

Email address: bipin.rajendran@kcl.ac.uk (Bipin Rajendran)
1. Introduction

The explosive growth of processing requirements of data-driven applications has resulted in intensive research efforts for alternative computing architectures that are more energy-efficient than traditional von Neumann processors. Unlike the dominant Deep Neural Networks (DNNs) which rely on real-valued information encoding, Spiking Neural Networks (SNNs) communicate through discrete and sparse tokens in time called spikes, mimicking the operation of the brain and are hence projected to be ideal candidates for realizing energy-efficient hardware platforms for artificial intelligence applications. Moreover, SNNs are also ideal for real-time applications as they take advantage of the temporal dimension for data encoding and processing. However, SNNs lag behind DNNs in terms of computational capability demonstrations due to the current lack of efficient learning algorithms [1]. Backpropagation techniques are ubiquitously adopted to train DNNs, but the discontinuous nature of spikes makes it non-trivial to derive such gradient-based rules for SNNs [2]. Here we explore a probabilistic framework for SNNs, which defines the output of spiking neurons as jointly distributed binary random processes. Such definitions help in applying maximum likelihood criteria and then derive flexible learning rules without requiring backpropagation mechanisms, conversions or other approximations from pre-trained ANNs [3].

Conventional neural networks have millions of trainable parameters and are trained using von Neumann machines, where the memory and computation units are physically separated. The performance of these implementations is typically limited by the “von Neumann bottleneck” caused by the constant transfer of data between the processor and the memory. SNN implementations on these platforms becomes inherently slow due to the need to access data over time in order to carry out temporal processing. Hence, hardware accelerators are necessary to exploit the full potential of SNNs and also to develop efficient learning
algorithms. Here, we discuss a hardware accelerator designed for implementing probabilistic SNNs, that uses binary STT-RAM devices for realizing synapses and digital CMOS for neuronal computations. We also evaluate the performance of probabilistic SNNs against equivalent ANNs on standard benchmark datasets.

2. Related Work

In an effort to build large-scale neuromorphic computing systems that can emulate the energy efficiency of the human brain, several computing platforms have implemented SNNs. While Tijanic chip [4], Intel’s Loihi [5] and IBM’s TrueNorth [6] realize spiking neurons and make use of static random access memory (SRAM) to store the state of synapses and neurons, recent research efforts have proposed the use of tiled crossbar arrays of two terminal nanoscale devices for implementing large-scale DNN systems [7, 8, 9, 10]. Though analog memristor based neural network accelerators are estimated to provide higher throughput than GPUs, there are several challenges associated with these in-memory computing solutions [8, 10, 11, 12]. For instance, programming variability and stochasticity of device conductances as well as the need for accurate and area/power-hungry digital to analog converters (DAC) at the input and analog to digital converters (ADC) at the output, along with the additive noise contributed by these peripheral logic circuits pose significant challenges [9, 13, 14].

Among the emerging nanoscale memory devices, Spin Transfer Torque RAM (STT-RAM) has been explored for implementing synaptic weights for ANNs as well as SNNs owing to their fast read/write characteristics, high endurance, and scalability [15, 16] in several previous studies [14, 17, 18, 19]. The stochastic nature of the spintronic devices has been leveraged to model neural transfer functions in a crossbar architecture [20]. These designs for SNNs have shown over $20 \times$ energy improvements over conventional CMOS designs. Notably, an all-spin neuromorphic processor design for SNNs comprising of spintronic synapses and neurons with in-memory computing architecture has been pro-
jected to give $1000 \times$ higher energy efficiency and $200 \times$ speed up compared to equivalent CMOS implementations [17]. In contrast to these prior implementations using spintronic devices, we consider STT-RAM device as a binary storage unit, minimising the area/power and precision requirements of peripheral logic circuits consisting of ADCs/DACs. Thus, $n$-bit synaptic weight is represented by using $n$ binary STT-RAM devices. While the idea of using STT-RAM device as a binary storage unit has been discussed earlier in [14 18], a deterministic spiking neuron model was used for learning and inference based on a crossbar architecture. Instead, this work uses STT-RAM memory as a regular storage unit, similar to that of SRAM storage in conventional designs. To the best of our knowledge, this work presents the first design of a hardware accelerator based on STT-RAM devices to implement probabilistic SNNs based on a generalized linear model (GLM) for neurons.

2.1. Main Contributions

The main contributions of this paper are listed as follows.

- We propose a hardware accelerator for inference, Spintronic Accelerator for Probabilistic SNNs (SpinAPS) that integrates binary spintronic devices to store the synaptic states and digital CMOS neurons for computations. The potential of hardware implementations of Generalized Linear Model (GLM)-based probabilistic SNNs trained using the energy efficient first-to-spike rule are evaluated for the first time in this work.

- We evaluate the performance of probabilistic SNNs on two benchmarks - handwritten digit recognition and human activity recognition datasets, and show that SNN performance is comparable to that of equivalent ANNs.

- SpinAPS achieves $4 \times$ performance improvement in terms of GSOPS/W/mm$^2$ when compared to an equivalent design that uses SRAM to store the synaptic states.
This paper is organized as follows: In Section 3, we review the architecture of GLM-based probabilistic SNNs and also explain the first-to-spike rule for classification. The algorithm optimization strategies for an efficient hardware implementation for the first-to-spike rule is considered in Section 4. The architecture details of SpinAPS core and the mapping of the GLM kernels into the memory is discussed in Section 5. Section 6 details the relevant digital CMOS neuron logic blocks and memory design. We then evaluate the performance of our hardware accelerator for different bit precision choices in Section 7. Finally, we conclude the paper in Section 8.

3. Review of GLM neuron model for SNNs

The majority of the neuron models used in SNN computations are deterministic in nature, by which the neuron emits a spike when the membrane potential crosses the threshold value. The non-differentiable nature of the spikes in SNNs makes it non-trivial to use the standard approach of stochastic gradient descent (SGD) widely used for training ANNs. Therefore, several approaches have been used to realize deterministic SNNs such as converting pretrained ANNs, smoothing out the membrane potential to define the derivatives, and so on [21, 22, 23, 24]. In contrast to deterministic models, probabilistic models for neurons are based on a linear-nonlinear Poisson model that are widely studied in the field of computational neuroscience [25].

![Figure 1: The architecture of Generalized Linear Model (GLM) model used for SNN learning in this work [26]. N_X input neurons and one output neuron is shown for simplicity.](image)

Generalized Linear Models (GLM) yield a probabilistic framework for SNNs
that is flexible and computationally tractable [3, 25]. The basic architecture of GLM-based probabilistic SNNs used for SNN training is shown in Fig. 1. We focus on a 2-layer SNN, which has $N_X$ presynaptic neurons encoding the input and $N_Y$ output neurons corresponding to the output classes. Each of the input neurons receives a spike train having $T$ samples through rate encoding. The input is normalized and spikes are issued through a Bernoulli random process. For cases where the sign of the input is vital in achieving learning, the negative sign is absorbed in the sign bit of the corresponding weights. The membrane potential of $i^{th}$ output neuron at any instant $t$ can be expressed as,

$$u_{i,t} = \sum_{j=1}^{N_X} \alpha_{j,i}^{T} x_{j,t-\tau}^{t-1} + \beta_{i}^{T} y_{i,t-\tau}^{t-1} + \gamma_{i}$$

(1)

where $\alpha_{j,i}$ denotes the stimulus kernel; $x_{j,t-\tau}^{t-1}$ represents the input spike window having $\tau$ spike samples; $\beta_{i}$ denotes the feedback kernel; $y_{i,t-\tau}^{t-1}$ represents the output spike window with $\tau$ samples; and $\gamma_{i}$ is the bias parameter. Here $j$ refers to the index of the pre-synaptic neuron and $i$ refers to the index of the post-synaptic neuron. The stimulus and feedback kernels in GLM can be defined as the weighted sum of fixed basis functions with the learnable weights, and they are expressed as shown below.

$$\alpha_{i,j} = A w_{i,j}, \quad \beta_{i} = B v_{i}$$

(2)

The matrices $A$, $B$ are the basis vectors, defined as $A = [a_1, \ldots, a_{K_{\alpha}}]$ and $B = [b_1, \ldots, b_{K_{\beta}}]$. The prior work in GLM [26] uses real-valued raised cosine basis vectors for the stimulus and the feedback kernels. The vectors $w_{j,i} = [w_{j,i,1}, \ldots, w_{j,i,K_{\alpha}}]^T$ and $v_{i} = [v_{i,1}, \ldots, v_{i,K_{\beta}}]^T$ are the learnable weights in the network with $K_{\alpha}$, $K_{\beta}$ denoting the number of basis functions. The spiking probability of the output neuron is then decided based on the sigmoid non-linearity applied to the membrane potential. GLM neurons have reproduced a wide range of spiking neuronal behaviors observed in human brain by appropriately tuning the stimulus and feedback kernels [25]. Learning rules for a GLM SNN based on rate and first-to-spike decoding rules have been derived in a number of works reviewed in [3, 27, 28].
Two main decoding strategies have been considered for the given SNN architecture - rate decoding and first-to-spike decoding [26]. When using the rate decoding scheme for inference, the network decision is based on the neuron with the maximum spike count. For the first-to-spike scheme, a decision is made when one of the output neuron spikes. It has been shown in [26] that the first-to-spike rule exhibits a low inference complexity compared to rate decoding due to its ability to make decisions early. Hence, we choose the first-to-spike scheme for our hardware optimization studies.

3.1. First-to-Spike Decoding

The fundamental idea of first-to-spike scheme is illustrated in Figure 2. The kernels for the GLM based SNN are trained using the maximum likelihood criterion, which maximizes the probability of obtaining the first spike at the labeled neuron and no spikes for all other output neurons up to that time instant. This probability can be mathematically expressed as,

$$p_t(\theta) = \prod_{i=1, i \neq c}^{N_v} \prod_{t' = 1}^{t} g(u_{i,t'}) g(u_{c,t}) \prod_{t' = 1}^{t-1} \overline{g}(u_{c,t'})$$

(3)

where $c$ corresponds to the labeled neuron, $u$ denotes the membrane potential, and $g(u)$ denotes the sigmoid activation function applied to the membrane potential $u$. Also $\overline{g}(u) = 1 - g(u)$. The weight update rules are derived by maximizing the log probability in equation (3) and are discussed in detail in [26]. Note that the feedback kernels are not necessary for the first-to-spike rule as the network dynamics need not be calculated after the first spike is observed.

3.2. Datasets Used in This Study

Throughout this work, we evaluate the performance of Probabilistic SNNs on handwritten digit recognition and human activity recognition (HAR) datasets [29]. With 60,000 training and 10,000 test images, each of the input image in the handwritten digit database has 784 (28 × 28) pixels corresponding to the 10 (0, 1, ..., 9) digits. The HAR dataset has a collection of physical activities feature extracted from the time series inputs of the embedded sensors in a smart
phone. The database has roughly 7,000 training samples and 3,000 test samples corresponding to six types of physical activities.

4. Hardware-Software Co-optimization

In this section, we discuss the design choices that facilitate our hardware implementation. We start by observing the floating-point baseline accuracy of FtS in Fig. 3, where the kernels are trained using the techniques demonstrated in [26]. For the purpose of designing the inference engine, we assume that the kernels are fixed and binary basis vectors are used in the training instead of the cosine basis vectors. The usage of binary basis vectors helps in simplifying the kernel computations without requiring any multipliers in hardware. We first determine the floating baseline test accuracy as a function of the presentation times $T$ by training the SNN over 200 epochs.

It can be seen that the network performance improves with higher presentation times $T$ and spike integration windows $\tau$, reaching a maximum test accuracy for $T = 16$ and $\tau = 16$. Note that for the handwritten digit benchmark, the network accuracy of the GLM SNN trained using the FtS rule with ($T = 8$, $\tau = 8$)
Figure 3: The test accuracy of GLM on human activity recognition (HAR) and handwritten digit recognition. A comparable performance is achieved with respect to an ANN having the same architecture. Here presentation time $T$ is kept the same as the spike integration window $\tau$.

$\tau = 8$ is 93.5%, which is at par with the 93.1% accuracy of a 2-layer artificial neural network (ANN) with the same architecture. In the case of HAR dataset, GLM achieves a maximum test accuracy of 94.5% with $T = 16$, $\tau = 16$ which is comparable with ANN test accuracy of 96.3%. Hence, we chose $T = 8$, $\tau = 8$ for handwritten digit recognition and $T = 16$, $\tau = 16$ for HAR benchmarks as the baseline. We now discuss software optimization strategies for implementing the first-to-spike scheme in an energy efficient manner in hardware.

### 4.1. Sigmoid Activation Function

As shown in Fig. 1, the basic GLM neuron architecture uses a sigmoid activation function to determine the spike probability of the output neurons. The implementation of sigmoid functions in hardware is relatively complex as it involves division and exponentiation, incurring significant area and power [30]. Here we follow the piecewise linear approximation (PWL) demonstrated in [31] for implementing the sigmoid activation function. In the PWL approximation, the sigmoid is broken up into integer set of break points such that the resulting function can be expressed as powers of 2. Considering the negative axis alone,
the PWL approximation $y$ for input $x$ can be expressed as

$$y_{x<0} = \frac{1}{2} + \frac{\hat{x}}{2 \lfloor x \rfloor}$$

(4)

where $(x)$ is the integer part of $x$ and $\hat{x}$ is the fractional part of $x$. Using the symmetry of sigmoid function, the values in the positive $x$-axis can be obtained as $y_{x>0} = 1 - y_{x<0}$. The output of the PWL approximation is then compared with a pseudo-random number generated from the linear feedback shift register (LFSR) and a spike is generated if the PWL value is greater than the LFSR output. A 16-bit LFSR is used and is assumed to be shared among all the output neurons.

### 4.2. Quantization

We now aim at finding the minimum bit precision required for the learnt weights $w_{j,i}$ and biases $\gamma_i$ in order to maintain close to baseline floating-point accuracy during inference. Here we follow a post training quantization study to determine the minimum bit precision required for the learnable parameters. Starting with the baseline networks for the two datasets obtained using floating point parameters, we quantize them into discrete levels and study the inference accuracy with the PWL approximation for the sigmoid. With $b$-bit quantization, one bit is reserved for the sign to represent both positive and negative parameters. We use a uniform quantizer with quantization step given by the relation

$$w_q = \frac{w_{max} - w_{min}}{2^{b-1}}; \quad \gamma_q = \frac{\gamma_{max} - \gamma_{min}}{2^{b-1}},$$

(5)

respectively for weights and biases. We also quantize the membrane potential and the output of the PWL activation to $b$ bits. We summarize the inference performance of the GLM SNN as a function of bit precision in Fig. 4 (a). Network performance degrades with lower choices of $b$, but we note that 5 bit resolution is sufficient for maintaining close to baseline floating-point inference accuracy for the two benchmarks. Even though the input spike pattern lasts for $T$ algorithmic time steps, the first-to-spike learning rule allows a decision.
Figure 4: (a) Test performance of the GLM SNN after quantization of weights with PWL approximation and by using a 16-bit LFSR. (b) Cumulative distribution of the number of input samples classified as a function of decision time $t_d$. An early decision can be made in first 4 time steps for classifying 75% of the images in the handwritten digit benchmark.

to be made even before all the spikes are presented to the network. It can be observed for the handwritten digit benchmark, around 75% of the samples are classified in the first 4 algorithmic time steps. Thus GLM SNN can leverage the ability of first-to-spike rule in making decisions with reduced latency and memory accesses.

5. Overview of SpinAPS architecture

As illustrated in Fig. 5, the core architecture of SpinAPS consists of binary spintronic devices to store the synaptic states and digital CMOS neurons to perform the neuronal functionality. The SpinAPS core accepts input spike at every processor time step $t$, reads the synapses corresponding to the spike integration window $\tau$ from the memory to compute the membrane potential and applies the non-linear PWL activation function to determine the spike probability of the output neurons. A pseudo-random number generated from the LFSR is then used to actually determine whether a spike is issued or not as explained in Section 4. The word width, and hence the memory capacity of the banked STT-RAM memory used in the SpinAPS core can be designed based on the bit precision $b$ required for the synapses. SpinAPS co-locates the dense
Figure 5: The core architecture of SpinAPS having binary STT-RAM devices to store the synaptic states and digital CMOS neurons. Assuming a spike integration window of $\tau = 7$, the core can map 256 input and 256 output neurons.

STT-RAM memory array and digital CMOS computations in the same core, thereby avoiding the traditional von Neumann bottleneck. Following the principles demonstrated in IBM’s TrueNorth chip [6], a tiled architecture with 4096 SpinAPS cores, with each core having 256 neurons, can be used to realize a system with 1 million neurons as illustrated in Fig. 6. We next discuss the basic characteristics of the spintronic synapses and how we can map the parameters of probabilistic SNNs into the memory.

5.1. **STT-RAM as Synapse**

Synapses generally scale as $N^2$, where $N$ is the number of neurons in each layer. Recently, spintronic devices have been explored for its use as nanoscale synapses [15, 20, 16] mainly due to its high read and write bandwidths, low power consumption and excellent reliability [32, 33, 34]. These spintronic devices are compatible with CMOS technology and fast read/write has been demonstrated in sub 10 ns regime [35, 36]. Here we propose binary STT-RAM devices as the nanoscale electrical synapses for the SpinAPS core illustrated in Fig. 5. Structurally, STT-RAM uses a Magnetic Tunnel Junction (MTJ) with a pair
of ferromagnets separated by a thin insulating layer. These devices have the ability to store either '0' or '1' depending on the relative magnetic orientation of the two ferromagnetic layers as shown in Fig. 7. The memory array is typically configured based on the crossbar architecture with an access transistor connected in series with the memory device to selectively read and program it.

5.2. Synaptic Memory Architecture

Here we discuss the mapping of the learnable parameters, stimulus kernel ($\alpha$) and the bias parameters ($\gamma$) of GLM-based SNN into the spintronic memory to achieve accelerated hardware performance.
5.2.1. Kernel Mapping

Here we choose \((T = 8, \tau = 7)\) to describe the mapping of 8-bit synapses, hence the word width (vertical lines in Fig. 8) required for the memory is \(256 \times 8 = 2048\) bits. Each of the input neuron generates a bit pattern of length \(\tau\), hence unique kernel weights are provided for every neuron, requiring \(256 \times 7 = 1792\) word lines in the array. Thus, a network with 256 input and 256 output neurons can be mapped to a memory array with \(2048 \times 2048\) memory devices. For example if the bit pattern generated by the first input neuron is “1010010”, then the synaptic weights corresponding to 1\(^{st}\), 3\(^{rd}\), and 6\(^{th}\) word line will be read sequentially. The address corresponding to these word lines are stored in registers, indicated as address storage registers in Figure 5. These synaptic weights will be added at the output neuron to compute the membrane potential. One word line will be sufficient for mapping \(\gamma\) as \((256 \times 8)\) bits is equivalent to the word width of the core. As \(\gamma\) determines the baseline firing rate of the output neurons, the word line voltage corresponding to the \(\gamma\) line is kept high indicating an “always read” condition.

6. High-level Design

6.1. Neuron Implementation

We now describe the digital CMOS implementation of the relevant blocks. The baseline design assumes 8-bit precision and is synthesized using TSMC
45 nm logic process running at a clock frequency of 500 MHz.

6.1.1. Generation of spike window

As discussed in Section 3, normalized input spikes are transformed to generate spikes of length $T$ using a Bernoulli random process. At each time instant, $t = 1 \ldots T$, incoming spikes are latched at the input neuron (marked as ‘In. Reg’, a serial-in, parallel out shift register in Fig. 5) which is then translated into an activation pattern of length $\tau$, and applied as read enable signals to the word lines associated with each kernel weights. The spike window generator circuit uses a multiplexer for selecting the bit pattern of length $\tau$ from the input register and whose select lines are configured by the controller for every $t$. For example, when $t = 1$, the select line will be “000” and as no input spikes have arrived before, the output of the multiplexer would be “0000000”. When $t = 3$, the select line becomes “010”, and the multiplexer output will be $s_2s_1000000$, where $s_i = 1/0$ represents the presence/absence of a spike at $t = i$ and so on. As discussed in Section 5, the synapses associated with the input neurons are read sequentially and hence the logic circuit for the spike window generator can be shared among all the input neurons. The synaptic weights are stored in the registers and the sign bit of the weights can be optionally flipped depending on the sign of the input before computing the membrane potential ($u$).

6.1.2. Piecewise Linear Approximation (PWL) for sigmoid calculation

Our GLM neuron model uses a non-linear sigmoid activation function for generating the spike probabilities for the output neuron based on the value of $u$. Here we adopt the traditional piecewise linear approximation (shown in Equation 4) for the sigmoid using adders and shift registers as described in [31]. The 18-bit membrane potential $u$ is clipped to an 8-bit fixed point number in the range [-8,8] before applying to the Piecewise Linear Approximation (PWL) sigmoid generator which is shared among 16 output neurons. The clipped fixed point representation assumes 1 bit for the sign, 4 bits for the integer and 3 bits for the fractional part. The output of the sigmoid generator is an unsigned
8-bit number whose values lie in the range $[0, 255]$ and is compared with the
8-bit pattern from the 16-bit LFSR (Linear Feedback Shift Register) to generate
output spikes.

6.2. Design of the synaptic memory

We describe the memory organization for the baseline design with 8-bit pre-
precision and $(T = 8, \tau = 7)$ as discussed in Section 4. The required memory
capacity for any $b$-bit precision would become $2048 \times 256 \times b$ bits. We design
and analyze the STT-RAM based synaptic memory using DESTINY, a com-
prehensive tool for modeling emerging memory technologies \cite{37}. STT-RAM
cell architecture with 1T/1MTJ configuration is simulated using the parameters
mentioned in table 1 with the feature size $F = 70\text{ nm}$ \cite{38}. In table 1 $V_r$ is
the read voltage, $t_r$ is the read pulse width, $I_p$ is the programming current and
$t_w$ denotes the write pulse width. Representative values for read and write pulse
width is assumed based on experimentally reported chip-scale demonstrations
of STT-RAM \cite{35, 38}. The optimized solution of the memory mapping for 8-bit

\begin{table}[h]
\centering
\caption{Simulation parameters for STT-RAM array using DESTINY with the feature size $F = 70\text{ nm}$}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline
Parameter & Cell Area & $R_{on}$ & $R_{off}$ & $V_r$ & $t_r$ & $I_p$ & $t_w$ \\
 & $F^2$ & $\Omega$ & $\Omega$ & mV & ns & $\mu A$ & ns \\
\hline
Value & 24 & 2500 & 5000 & 80 & 5 & 150 & 10 \\
\hline
\end{tabular}
\end{table}

Figure 9: Banked STT-RAM organization for mapping the synapses of GLM SNN having 256
input and 256 output neurons with 8-b precision weights.
precision is shown in Figure 9. The read energy per word line for 8b is around 535 pJ with a latency of 7.34 ns. The simulated STT-RAM array running at 100 MHz has an area efficiency of 43% with a total synaptic area of 1.14 mm\(^2\) and power of 53.5 mW.

7. Performance evaluation

We use a commonly used performance metric to benchmark our accelerator design - the number of billions of synaptic operations that can be performed per second per watt (GSOPS/W) and per unit area (GSOPS/W/mm\(^2\)). A synaptic operation refers to reading one active word line (256 b-bit synapses), computing the spike probability and then issuing the output spike. We compare these performance metrics of SpinAPS with an equivalent SRAM-based design for different bit precisions (shown in table 2), with neuron logic implementation kept the same. The SRAM memory is simulated using DESTINY [37] and clocked at 250 MHz. Independent of bit precision, SpinAPS can perform 25.6 GSOPS while the SRAM-based design achieves 64 GSOPS due to its higher clock rate. For 8-bit precision, SpinAPS core is approximately 6× better in synaptic power and 3× in synaptic area when compared to SRAM. For the values reported in table 2, a 10% overhead is considered for the spike routing infrastructure between the cores and 20% overhead is added to consider the area and power of the core’s controller [6, 39, 40]. It can be noticed that the SpinAPS core can achieve a maximum performance improvement of 4× and a minimum of 3× in terms of

| Precision | GSOPS/W | GSOPS/W/mm\(^2\) |
|-----------|---------|-------------------|
|           | SRAM    | STT-RAM           | SRAM | STT-RAM |
| 5         | 353     | 474               | 177  | 559     |
| 6         | 283     | 412               | 119  | 415     |
| 7         | 230     | 366               | 83   | 322     |
| 8         | 193     | 311               | 61   | 239     |
GSOPS/W/mm² when compared to an equivalent SRAM-based design for 8b and 5b precision choices respectively. The average energy per algorithmic time step $t$ of the SpinAPS core and the total area for the design as a function of the bit precision is shown in Fig. 10.

Figure 10: (a) Average energy per processor time step ($t$) of SpinAPS for each of the bit choices for the handwritten digit benchmark. One processor time step corresponds to reading all the active word lines (on an average 365), compute the membrane potential and generating an output spike. (b) Area of the SpinAPS core as a function of bit precision.

We now compare the performance of SpinAPS with an inference accelerator design employing STT-RAM devices for SNNs, memristor-based inference engines for DNNs, and GPUs. The performance improvement projected for SpinAPS is comparable to what has been recently reported in [14], which uses STT-RAM devices in integrated crossbar arrays. Furthermore, the SpinAPS design presented here, when extrapolated to 32 nm [12] technology node achieves 850 GSOPS/W, which is also comparable with other recent memristor-based DNN inference engines achieving 800 GSOPS/W in [11] and 1060 GSOPS/W in [10]. Note that when compared to state-of-the-art GPUs like Tesla V100, SpinAPS can achieve approximately 20×, and 4× improvement in terms of GSOPS/W, and GSOPS/mm² [12]. While implementations employing analog phase change memory (PCM) devices in crossbar arrays have been projected to provide two orders of magnitude improvement in energy efficiency when compared to GPUs through extrapolated and aggressive assumptions [11], SpinAPS projections are based on more realistic design choices that are representative of
8. Conclusions

In this paper, we proposed a hardware accelerator SpinAPS using binary STT-RAM devices and digital CMOS neurons to perform inference for probabilistic SNNs. The probabilistic SNNs based on the GLM neuron model are trained using the novel first-to-spike rule and its performance is benchmarked on two standard datasets, exhibiting comparable performance with an equivalent ANN. We discussed the design of the basic elements in the SpinAPS core, considering different bit precision choices and the trade-off associated with the performance and hardware constraints. SpinAPS leverages the ability of first-to-spike rule in making decisions with low latency achieving approximately 4× performance improvement in terms of GSOPS/W/mm² compared to SRAM-based design.

Acknowledgment

This research was supported in part by the National Science Foundation grant #1710009, and the CAMPUSENSE project grant from CISCO Systems Inc. Resources of the High-Performance Computing facility at NJIT was used in this work.

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