Ultrahigh Speed Artificial Neuron Compatible with Standard Foundry Processes and SFQ Cells

M. Altay Karamuftuoglu1 and Ali Bozbey1

1 Department of Electrical and Electronics Engineering, TOBB Economy and Technology University, Ankara, Turkey
E-mail: bozbey@etu.edu.tr

Abstract

Neuromorphic computing methods and artificial neurons can enhance the possibilities of solving complex problems more efficiently. We propose a neuron circuit formed by a double-junction SQUID interfered with a resistor (threshold loop), a resistor – inductor structure (decaying loop), and mutual inductance between threshold loop and decaying loop. Designed artificial neuron has the following main properties: (i) ultra-high-speed operation with minimal power consumption, (ii) compatibility with standard foundry processes so that it can be fabricated with the available infrastructure, (iii) compatibility with conventional logic gates so that complicated networks can be designed and implemented. The proposed artificial neuron, fabricated with a commercial foundry service, with different activation functions, has been implemented and demonstrated experimentally. Operation speed of the neuron is about 50 GHz with about $5 \times 10^{-19}$ J/spike energy.

Keywords: Superconductor, Artificial Neuron, Neuron Circuit, Integrate and Fire Model Neuron, leaky IFN

1. Introduction

The current scientific community enthralled by understanding the general principles of human brain functions, as a further matter, on how to mimic the abilities by utilizing artificial neurons for more efficient computing. Neurons are considered as fundamental units of human brain due to the functions, receiving and sending electro-chemical signals to process the data and creating overall behavior [1]. Dendrites receive synaptic inputs from other neuron axons and they bring information to the cell body. Soma collects all signals from its dendrites and creates relative response that depends on received signals. The axon carries the electrical response to the connected neurons. Functionality comes from self-assembly of brain cells, known as nerve cells or neurons. Mathematical neuron models are created with relatively similar components of biological structure [2,3].

Artificial neural networks are considered as an alternative and effective way to deal with complex problems such as image recognition, decision making, forecasting while simulating the biological brain [4,5]. Implementation of the neuron behavior gives us opportunity to create neuromorphic computers that can learn events the way brain does. Computational software tools connect artificial neurons to each other to create Artificial Neural Network (ANN) to adopt biological neural network behavior. ANN software tools have gained extensive acceptance for neural network applications because of learning abilities, computational power and speed through parallel processing.

Even though there are hardware neuron design examples based on CMOS devices [6–9], CMOS technology is facing its fundamental limits as Moore’s law [10,11] reaches its end and this motivates the different technology investigations about artificial neuron applications [12] for implementing a neuromorphic computer. One of the strongest candidates for hardware neuron implementation technologies is single flux quantum (SFQ) technology [13,14]. Characteristic features of Josephson junctions which have ultra-high-speed switching behavior with low power consumption match the properties of biological neurons. The comparison of biological neuron [1] with CMOS IFN Model representations [6,8,9,15] and our
superconducting IFN Model features is shown in Table 1 which is adapted and extended from [16].

There are several neuron circuits that report to implement the characteristics of a brain cell by using SFQ technology [17–23]. However, these circuits have the problem of high complexity, usage of inefficient on-chip area, slow operation speed and/or incompatibility with standard SFQ digital library elements which enables convenient integration with conventional logic circuits. Our circuit is based on leaky IFN model and it demonstrates an effective and robust way of implementation of a biological brain cell operation. The neuron circuit can trigger the connected next neuron and/or digital SFQ circuit cells in the library since it has matching input/output without the need for another circuit. In addition, another main advantage of the proposed neuron circuit is that it is compatible with the established SFQ foundry processes [24–27].

2. Neuron circuit

2.1 Principle of operation

For biological neural networks, synaptic strengths define the function of the network and network provides the same operation if synapses are not changed. If the synapse values are preserved, biological memory function of network will be achieved [28]. If a person does the action repetitively, related synaptic weight values increase, and this provides recall function of network. Main body of neuron, soma, acts like a temporary storage of inputs to be able to do aggregation function. If sufficient number of input pulses arrive to soma from synapses, it fires an axonal (output) pulse and the operation is called somatic operation. However, if the number of inputs is not enough within a certain time, no output pulse will be released. These principles are inherently implemented in JJ based logic circuits, namely single flux quantum (SFQ) circuits [13,14] where the logic “1” and “0” is based on single flux quantum pulses. Hence, it is possible to implement the operation of a biological neuron by JJs and SFQ circuits in an intuitive way.

In this study, our circuit implements the mathematical model shown in Figure 1 which is mainly composed of a summation function and activation function. In the model, number of inputs and their individual weighs determine the function of the cell. Operation starts with individual multiplication of inputs with their weights as shown in equation (1). Then, all values arriving from inputs are added together on summation function. If the sum of multiplication results surpasses the threshold value, activation function provides an output and pulses are transmitted to the next neurons via synapses as reported in equation (2).

\[ X_0W_0 + X_1W_1 + X_2W_2 + X_3W_3 = u \]  \hspace{1cm} (1)
\[ f(u) = Y \]  \hspace{1cm} (2)

2.2 Implementation of the artificial neuron

The schematic of Josephson junction (JJ) based Artificial Neuron (JJ-AN) circuit is shown in Figure 2. The neuron cell is modelled by using Josephson junctions and passive elements. The circuit is mainly formed by a threshold loop, decaying loop, and mutual inductance between threshold loop and decaying loop. Each of the loops adjust the fading time of pulses that are held in threshold loop. Various combinations of parameter values can create different threshold values and decaying times on neuron circuit. In JJ-AN design, the activation function is set to desired number of pulses. Artificial neuron’s way of working principle matches the characteristic features of biological neuron somatic operation and similarities make JJ-AN a potential candidate for use in high performance and low power neural network implementations.
Table 1. The comparison of biological neuron [1] with CMOS IFN Model [6,8,9,15] representations and our superconducting IFN Model features. Table is adapted and extended from [16].

| Information Transfer | Biological Neuron | CMOS Neuron | SFQ Neuron |
|----------------------|------------------|-------------|------------|
| Long distance 'Lossless' Data Transmission | Electro-chemical Impulse [1,29] | Electrical Spike [6–9] | Single Flux Quantum (SFQ) Pulse [13] |
| 3D Architecture | Membrane, Nucleus, Mitochondria, Ribosomes [30] | Semiconducting Metal Layer Stack [31] | Superconducting Metal Layer Stack [32] |
| Threshold Tuner (Summation Operation) | Soma [1,29] | Spike Integrator Circuit [7–9] | Threshold & Decaying Loops of JJ-AN This Paper |
| Interconnection | Synapse [1,29] | Synapse Circuit [9] | Pulse Splitter and Merger Digital Circuits [13] |
| Fault tolerance | ✓ [30] | ✓ [6] | ✓ This Paper |
| Speed (Spike Fire Rate/Second) | $10^3$ [33,34] | $10^3$ [6,8,35] | $10^{10}$ This Paper |
| Energy per spike (Joule/Spike With/-w/o DC power) | N/A-10^{-12} [6,36] | $10^{-15}$-10^{-15} [6] | $10^{-17}$-10^{-19} This paper, [37] |

**Figure 2.** Artificial neuron circuit used in this study.

To match the impedance of a JJ-AN to an SFQ logic circuit or any desired circuits, $L_{IN1}$, $L_{IN2}$ and $L_{OUT}$ inductances are used. So, when a JJ-AN fires a pulse, it can be handled directly by the SFQ circuits or vice versa. $J_1$ and $J_2$-Josephson junctions determine the threshold value and quiescent point of these junctions is set by bias current. $R_{LOOP}$ resistor adjust the amount of current dissipation from threshold loop. By increasing this resistor, current dissipates faster, and more input pulses will be needed to reach to threshold value. Mutual coupling between $L_{LOOP}$ and $L_{TOP}$ inductances is another factor that adjust the decaying time of loop current. If we increase the mutual coupling value, amount of current that is transferred to decaying loop will increase and the circulating current in the threshold loop will dissipate faster. On the other hand, when $L_{LOOP}$ value is increased, the decay time will be increased, and the threshold loop current will remain in the loop longer. As a result of this, interval time between the input pulses can be higher. The effect of $R_{TOP1}$ and $R_{TOP2}$ resistors is same as $R_{LOOP}$ parameter. In addition, the quiescent point of neuron circuit can be adjusted easily by changing the DC bias current. In summary, by adjusting the circuit parameters and bias point of the JJ-AN, it is possible to adjust the memory duration and threshold values of the neuron.

There are many solutions to reach the desired neuron properties. Simulation assumes perfect parameters without any tolerance and no thermal noise. Unfortunately, when the circuits are fabricated, there are some fabrication tolerances in the JJ critical currents, inductances and resistors. In addition, during measurements thermal noise increases the gray zone of comparator-based circuits [38,39].

In this study, pulse energy calculation of JJ-AN shows that dissipation is extremely low even if DC power consumption of JJ-AN is included. During the generation of the SFQ pulse, Josephson junction switches to voltage state and generates a quantum accurate digital signal in the form of single flux quanta $\Phi_0 = 2.06 \times 10^{-15}$ Wb [37]. Energy per pulse is calculated by equation (3) where $I_C$ is the critical current of the Josephson junctions.

$$E_{SFQ} = \int_0^T I_C V dt = I_C \Phi_0$$ (3)

Critical current of the junctions in the neurons of this study are about 250 $\mu$A. So, energy per pulse is about $5 \times 10^{-19}$ Joule, excluding DC power. Bias voltage of the neuron cells is about 2.5 mV with a bias current of 350 $\mu$A. So, DC power consumption is 8.75 $\times 10^{-7}$ W. For 50 GHz operation, average energy per pulse is 1.75 $\times 10^{-17}$ Joule including DC Power.

2.3 Device operation

Every pulse that arrives to neuron circuit is held in threshold loop and the amount of current that is collected can be observed on $L_{LOAD}$ parameter. Threshold loop mimics the part of human brain cell called soma. Pulses may arrive to the circuit at arbitrary times and it may increase the stored current value that is in the threshold loop. In the meantime, the current dissipates as heat in certain periods of time. A series of single inductance ($L_{LOAD}$) and resistance ($R_{LOAD}$) is added to output...
port of neuron as load. Different input variations are provided to JJ-AN circuit in Figure 3. All simulations are done by using Josephson Simulator (JSIM) [40] and results are shown in Figure 4.

![Figure 3. JJ-AN Simulation Schematic. (L_{LOAD}=1 \text{ pH}, L_{LIN1}=0.3 \text{ pH}, L_{LIN2}=1.6 \text{ pH}, L_{LOOP}=9.6 \text{ pH}, L_{TOP}=9.6 \text{ pH}, R_{LOAD}=4 \Omega, R_{LOOP}=1.25 \Omega, R_{TOP1}=5 \Omega, R_{TOP2}=5 \Omega, K=0.5 \text{ pH}, J_1=243 \mu\text{A}, J_2=243 \mu\text{A}, I_b=0 \mu\text{A})]

![Figure 4. JJ-AN JSIM result with different input patterns. Voltage units are mV and current units are mA.]

In this test, input pattern contains spikes with different amplitudes, delays and durations. Even if negative amplitude inputs arrive, JJ-AN keeps its functionality. First, input spikes with 1 mV amplitude arrive to circuit (I). Due to insufficient number of spikes and large delay between spikes, neuron circuit is unable to fire an output. However, if the number of spikes is increased and the delay between neurons is decreased, neuron circuit can fire an output after reaching threshold value (II). Likewise, neuron circuit can work under any positive continuous signals (V). Neuron circuit is also put under test with the same input sets that have negative amplitudes and similar characteristics are observed (III, IV, VI). The last but not least, mixed input pattern is provided to show transition characteristics of the model (VII). Input and output voltage values are observed on \( V_{PULSE} \) and \( J_2 \).

### 2.4 Neuron-SFQ cell compatibility

JJ based artificial neuron and a biological neuron are analogous to each other and it is possible to implement most of the functionalities of a biological neuron with the proposed circuit. However, this property alone is not enough for practical applications. For implementing a complicated artificial neural network, many of these cells should be able to reliably fabricated, and neurons should be able to be interfaced with conventional logic circuits as well as other neurons for input and output signals. As the conventional logic interface we aimed to match the artificial neurons with SFQ logic circuits as the SFQ logic technology is already matured technology for implementations of highly complicated and high speed logic circuits [41–48]. In addition, SFQ circuits and proposed artificial neurons can be fabricated by using the same foundry process on the same chip. So, cost and reliability of fabrication and ability to use available design tools enable convenient scaling of the artificial neural networks with the proposed artificial neuron.

Fundamentally, a JJ-AN has one input and one output line each of which is compatible with SFQ logic circuits [13,49,50]. It is comprised of two loops: the threshold loop that holds the current and the decaying loop that sets the dissipation time. To trigger the neuron circuit and make it give an output, the number of pulses that provides sufficient current in the threshold loop should surpass the limit that is adjusted by the sensitivity parameters. In this research, first optimized circuit has a threshold of two and the second one has threshold of three SFQ pulses. For the first design, after obtaining a single input pulse, second pulse should arrive within 65 ps. If it arrives after 65 ps, there will not be enough current in the threshold loop due to the decay of stored current. For a neuron of threshold two, after every two pulses, neuron circuit provides a single pulse as an output and it is ready to obtain next pulse after releasing the output pulse. The neuron of threshold three provides an output after obtaining three pulses and the delay between pulses should be set to maximum 20 ps. SFQ test circuit schematics of the JJ-AN together with peripheral circuits and operation of neuron circuits with two/three pulse thresholds are shown in Figure 5 and Figure 6. Input patterns that arrive to the neuron are SFQ pulses from the previous Josephson transmission line (JTL) cell. With the arrival of an input pulse, circulating threshold loop current increases and stored current is observed on \( L_{LOOP} \). If the threshold limit of the loop is reached, \( J_2 \) switches and fires an output pulse to next stage.

![Figure 5. Test Schematic of JJ-AN. (L_{LIN1}=0.3 \text{ pH}, L_{LIN2}=1.11 \text{ pH}, L_{LOOP}=5.32 \text{ pH}, L_{OUT}=2.94 \text{ pH}, L_{TOP}=10.76 \text{ pH}, R_{LOOP}=0.34 \Omega, R_{TOP1}=0.31 \Omega, R_{TOP2}=0.3 \Omega, K=0.21 \text{ pH}, J_1=278 \mu\text{A}, J_2=272 \mu\text{A}, I_b=369 \mu\text{A}, Two pulse threshold) (L_{LIN1}=0.3 \text{ pH}, L_{LIN2}=1.57 \text{ pH}, L_{LOOP}=9.42 \text{ pH}, L_{OUT}=4.59 \text{ pH}, L_{TOP}=12.34 \text{ pH}, R_{LOOP}=0.53 \Omega, R_{TOP1}=7.23 \Omega, R_{TOP2}=3.86 \Omega, K=0.34 \text{ pH}, J_1=150 \mu\text{A}, J_2=243 \mu\text{A}, I_b=342 \mu\text{A}, Three pulse threshold)]
Figure 6. a) Simulation results of the neuron with two pulse threshold. This neuron is tested with four different input situations: 1 pulse, 2 pulses, 4 pulses, and 6 pulses. As expected, after each 2 SFQ pulses, JJ -AN fires an SFQ pulse. b) Simulation results of the neuron with three pulse threshold. This neuron is tested with three different input situations: 1 pulse, 3 pulses, and 3 pulses. As shown, when the number of pulses arriving with proper timing are equal to the threshold of the JJ-AN, it fires an SFQ pulse. Even if the number of pulses is equal to the threshold, the delay between pulses affect the result of neuron output since the trapped current is dissipated in the threshold loop. Voltage units are mV and current units are mA.

3. Optimization procedure

Optimization of neuron circuit is an important process that helps to obtain better results after the fabrication process of neuron circuit. To optimize circuit, Particle Swarm Optimization (PSO) is selected because it is one of the non-linear optimization methods and its algorithm depends on modelling of particles. Each particle that seeks for the maxima point in a given search-space determines the values based on the objective function of the application. Further information can be found in [41,51] that was used to develop SFQ logic cells [13,49,50] and vortex transitional memory [41].

Optimizer uses a reference of defined input pulse train to compare the output pulses that appears if the threshold is surpassed. In simulation, it obtains peak points for each of input and output pulses. Input pulse train comes from previous digital cell or neuron circuit and neuron circuit is optimized together with them because the circuit must ensure that its impedance matches with SFQ digital library. Reference input and output patterns are provided by the circuit that is already constructed in schematics and pattern format that we want to obtain and see in output is written on commercially available numerical computing environment. We have developed a function to integrate the pattern of neuron circuit and an optimization of any circuit with analog input and output patterns. This function checks the peak points of input and output lines and it compares the peak points that are found to create I/O relation. Optimizer sweeps each parameter with predefined step size to limit points. For this study, step size is set as 1% of parameters’ design values.

We have run the modified optimizer for two circuits defined with different patterns and these circuits are made for STP2 process technology [27] with \( J_c=2.5 \text{ kA/cm}^2 \). For each case, we have run the program about 48 hours in an Intel i7 3930K CPU @3.20GHz 6 core PC with 5 particles. Step size is set to 1% of parameter values and value of margin range have been discrete in 1% steps. We have obtained ±23% for two pulse threshold neuron circuit with 20 ps input pulse delay and ±7% for three pulse threshold neuron circuit with 20 ps delay between pulses. All individual parameter margin ranges are shown in Figure 7 and the chip photographs are shown in Figure 8.
4. Experimentation of JJ-AN

4.1 Individual input pattern generation

To be able to test the individual artificial neurons, we created an on-chip pulse generator circuit by using SFQ cells. For this purpose, we used splitter and merger cells as shown in Figure 9. The pulse generators generate 1, 2, and 3 pulses with proper timings by using a single external trigger signal. By adjusting the delay paths (A, B, C, D), we can create the certain input patterns for JJ-ANs. Number of pulses are determined by the number of merger and splitter cells. Splitter cell first converts a single SFQ pulse to 2 simultaneous pulses and then one of these pulses is delayed as required and merged to obtain an SFQ pulse train. By combining n splitter and n merger cells, n+1 path ways are created for SFQ pulses. Delay time of the paths are adjusted with Josephson transmission lines and different type of SFQ library circuits if necessary. Pulse path simulations are shown in Figure 10, and $\Delta t_k$ denotes the delay for the k$^{th}$ connection.

Figure 11. JJ-ANs’ test circuits with individual input pattern on chip. Bar = 100 µm.

4.2 Input test design for JJ-AN

To test JJ-AN circuits individually, JTL, SPL, and CBU circuits are placed on chip. Every JJ-AN circuit which is shown in Figure 11 has different input pattern. When there is an SFQ pulse at the input (top row), it triggers three different input test patterns for three independent neurons: For neuron 1 (red rectangle), it generates a single SFQ pulse, for neuron 2 (orange rectangle) it generates two SFQ pulses with 20ps interval, and for neuron 3 (green rectangle) it generates three SFQ pulses with 65ps interval time. Since the thresholds of the neurons 1, 2, 3 are two, then output1 is “0” while Output2 and Output3 are “1” after each input signal. JSIM simulation results of the neuron circuits with two pulse threshold are shown in Figure 12-a and Figure 12-b. The experimental result which is inline with the simulation is shown in Figure 12-c. When there is an SFQ pulse at the input (top row), it triggers two different input test patterns for two independent neurons: For neuron 4 (cyan rectangle), it generates two SFQ pulses and for neuron 5 (blue rectangle), it generates three
SFQ pulses with 20ps intervals. Since the thresholds of the neuron 4 and 5 are three, Output4 is “0” while Output5 is “1” after each input signal. JSIM simulation results of the neuron circuits with three pulse threshold are shown in Figure 13-a and Figure 13-b. The experimental result which is inline with the simulation is shown in Figure 13-c.

5. Conclusion

The circuits in this study, fabricated with AIST Standard Process (STP2) [27], cover 40 µm × 80 µm on-chip area and the size of the neuron circuits is adjusted for the peripheral SFQ library circuits. The maximum switching speed of the proposed neuron is about 50 GHz with an event energy per SFQ pulse of approximately 1.75×10⁻¹⁷ and 5×10⁻¹⁹ Joule/spike including and excluding DC power respectively as mentioned in Table 1. As we have used RSFQ technology, DC power consumption is much higher than the switching power consumption. However, it is possible to implement the circuits by using e-RSFQ where the bias resistors are replaced with Josephson junctions and inductors [52] and achieve zero static power consumption.

Emulating neuronal dynamics directly on chip will enable the creation of neural networks or hybrid circuits for robust/high performance operations and further enhance the development of neuromorphic computers with complex operations. A Josephson junction artificial neuron circuit (JJ-AN) has been proposed and implemented by using single flux quantum logic. JJ-AN is amenable to use in processing event-based sensory information and low-power perceptual decision making. The working principles of the circuit closely matches to that of a biological neuron in the sense that it operates based on pulsed logic. Activation threshold is determined by the pulse interval and number of pulses arriving at the artificial neuron. Proposed artificial neuron is analyzed by numerical simulations and correct operations are proven experimentally. JJ-ANs are optimized to compensate for non-modelled experimental factors and unwanted distortions on model parameters. In summary, JJ-AN has promising characteristics due to its size, I/O speed, compatibility with digital circuits, reliability on fabrication and power consumption to improve the performances of neuromorphic computing systems.

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Figure 13. a) JSIM simulation results of the neuron circuits with three pulse threshold. SFQ Representation. b) JSIM simulation results of the neuron circuits with three pulse threshold. DC Representation. c) Experimental results from neuron circuits with three pulse threshold. Voltage units are mV.

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