Proposal of Analog In-Memory Computing with Magnified Tunnel Magnetoresistance Ratio and Universal STT-MRAM Cell

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Abstract—In-memory computing (IMC) is an effective solution for energy-efficient artificial intelligence applications. Analog IMC amortizes the power consumption of multiple sensing amplifiers with analog-to-digital converter (ADC), and simultaneously completes the calculation of multi-line data with high parallelism degree. Based on a universal one-transistor one-magnetic tunnel junction (MTJ) spin transfer torque magnetic RAM (STT-MRAM) cell, this paper demonstrates a novel tunneling magnetoresistance (TMR) ratio magnifying method to realize analog IMC. Previous concerns include low TMR ratio and analog calculation nonlinearity are addressed using device-circuit interaction. Peripheral circuits are minimally modified to enable in-memory matrix-vector multiplication. A current mirror with analog calculation nonlinearity are addressed using device-circuit interaction. Previous circuits are modified to follow the computation requirement, meanwhile supports 1024 2-bit input and 1-bit weight multiply-and-accumulate (MAC) computations simultaneously. The 2-bit input is represented by the width of the input (IN) pulses, while the 1-bit weight is stored in STT-MRAM and the \( \times 7500 \) magnified TMR (m-TMR) ratio is obtained by latching. The proposal is simulated using 28-nm CMOS process and MTJ compact model. The integral nonlinearity is reduced by 57.6% compared with the conventional structure. 9.47-25.4 TOPS/W is realized with 2-bit input, 1-bit weight and 4-bit output convolution neural network (CNN).

Index Terms—STT-MRAM, tunneling magnetoresistance ratio, in-memory computing, analog computing, linearity.

I. INTRODUCTION

Merging nonvolatile memories (NVMs) accompany with better computing ways enable great potential for energy-efficient artificial intelligence applications [1]–[3]. Magnetic random access memory (MRAM) has demonstrated promising developments for in-memory computing (IMC) and near-memory computing (NMC) [4]–[6]. Compared with other resistive-type NVMs, IMC with MRAM (in-MRAM computing) shows potential with logic compatible supply voltage, relatively small variability issues and high endurance [6].

Previous in-MRAM computing realizations mainly rely on intrinsic computing ability of bit-cells [6]–[9] and circuit-level modification [10]–[13]. Circuit-level solutions e.g., Pinatubo, logic-in-memory and computing-in-memory provide Boolean logic computation and support binary neural networks (BNN). MRAM building blocks e.g., sensing amplifier (SA) and reference cells are modified to follow the computation requirement, which could result in deteriorated memory performance.

Compared with digital IMC, analog IMC shows great merit in terms of high on-chip bandwidth and computation-area efficiency [14]. One-transistor one-magnetic tunnel junction (MTJ) 1T-1M bit-cell using spin-transfer-torque (STT) switching mechanism is with foundry supported as the most universal cell structure [13]–[17]. Unlike other nonvolatile memories, e.g., flash [18], resistive-RAM (RRAM) [19], [20] and phase change memory (PCM) [21], the analogue memory devices behavior of STT-MRAM cannot directly apply to analog computing for energy and throughput constrained applications. The main reason is that 100%-200% regular tunnel magnetoresistance (TMR) ratio is overwhelmingly difficult to fulfill the requirement of high dimensional matrix-vector multiplication (MVM). Although TMR was enhanced to 249% [22], the discrimination of anti-parallel (AP) and parallel (P) resistance is not sufficient, which can be influenced by the process variations.

In terms of circuit-level, analog IMC meets obstacles in its development due to: (1) Limited TMR causes mismatch between the impact of external input data and internal stored data on the output. (2) The analog computation behavior is more vulnerable to transistor nonlinear effects than its digital counterpart [23]. (3) Multiple bit-lines are required to enable simultaneously for cost amortization. In order to avoid inconsistency operations, processing units must fulfill the calculation requirements of different loads [24].

In order to bring in-MRAM computing into silicon realization, recent work attempt to make breakthrough through different hierarchical levels. [23], [25] integrates MTJ and Schottky diode as a rectified tunnel MR (R-TMR) device. Device fabrication indicates that it is possible to achieve more than 10000% on/off ratio can be obtained through varying DC offset. [6] applies the next-generation spin-orbit torque (SOT) MRAM to realize analog IMC at DNN interface, with Ron equals to 6 MOhm. A STT-MRAM prototype with NMC was demonstrated in [5]. Shift and rotate operations can be realized close to bit-cell array.

In this paper, the proposed a novel device-circuit interacted design approach, as transfer normal TMR (in MTJ device) to magnified TMR (in computation circuits). Analog in-MRAM computing is firstly implemented based on universal 1T-1M
cell with STT switching mechanism. To realize an enlarged virtual TMR ratio for analog computing, additional peripheral circuits are implemented, including dynamic latch, current mirror with feedback, and a successive approximation (SAR) analog-to-digital converter (ADC). Nonlinear issues of analog calculation are carefully addressed. The proposal is with minimally modified peripheral circuits realization using 28-nm CMOS, and without modification of bit-cell structure.

The reminder of the paper is organized as follow: Section II explains the basic concept and reviews recent works. Section III presents proposed in-MRAM computing structure. Section IV illustrates simulation results. Finally, Section V compares the performance of this work to prior IMC schemes, and concludes this paper with future remarks.

II. PRELIMINARIES

A. Matrix Vector Multiplication

High-dimensional matrix-vector multiplication (MVM) is a dominant kernel in signal-processing and machine-learning computations [27]. Instead of accessing raw bits row by row, IMC accesses a computation result over multiple bits, thus amortizing the accessing costs. The structure of the storage array matches the computational form of MVM, so the power consumption can be amortized by implementing MVM with IMC. MVM in-memory realization can split as a combination of multiply accumulate (MAC) computations as:

\[ Y_{OUT} = \sum_{i=0}^{m-1} W_i \times X_{IN,i} \]

where \( W \) is the weights stored in memory array, \( X_{IN} \) is the activations from external input, and \( Y_{OUT} \) is the calculation results. There are \( m \) weights and \( m \) activations involved in the MAC calculation.

MVM needs to map the parallel input data to each row, map the parallel computation to the bit cells where the data is stored, and then reduce the output data by adding up. The mapping of weights in the storage array can be represented by:

\[
W = \begin{pmatrix}
W_{0,0} & W_{0,n-2} & \cdots & W_{0,n-1} \\
W_{1,0} & W_{1,n-2} & \cdots & W_{1,1} \\
\vdots & \vdots & \ddots & \vdots \\
W_{m-1,0} & W_{m-1,n-2} & \cdots & W_{m-1,1}
\end{pmatrix}
\]

where \( n \) means each weight is quantified to \( n \) bits.

B. Universal 1T-1M bit-cell

Foundry-support 1T-1M bit-cell structure shows high-density and access energy efficiency in MRAM array [15–17]. Fig. 1(a) illustrates the basic storage element of perpendicular magnetic anisotropy (PMA) MTJ. Compared with in-plane magnetic anisotropy (IMA), PMA MTJ fulfills the thermal stability requirement, but also has no restriction of cell aspect ratio, which shows the scaling advantages of high-density integration [28], [29]. MTJ consists of two ferromagnetic electrodes (CoFeB) with a tunnel barrier layer (MgO). The top magnet is the storage layer (referred as the free layer) and the bottom magnet is the reference (referred as the pinned layer). Nonvolatile data writing is performed by injecting a spin-polarized current from one of the ferromagnetic electrodes to change the magnetic orientation of the free layer. The effective resistance of MTJ is low (\( R_P \)) when two ferromagnetic electrodes are spin aligned, and high (\( R_{AP} \)) when the magnetic direction of two layers is in the antiparallel state. The resistance difference is represented as TMR ratio [22], [30], [31]:

\[ TMR = \frac{R_{AP} - R_P}{R_P} \]

Fig. 1 demonstrates the cross-sectional view, bit-cell structure and I-V characteristics of 1T-1M bit-cell. According to spin transfer torque mechanism, a bidirectional current can change the MTJ between states when it is higher than critical current \( I_{C0} \). During the write operation, the current flowing from bit line (BL) to source line (SL) can write the data stored in MTJ as ‘0’, while the current with opposite direction can write ‘1’. Fig. 1(d) shows the resistance state at different voltages and the transition of MTJ between P state and AP state.

C. Digital and analog realization of IMC

IMC is an effective way to achieve energy-efficiency emphasized non-von Neumann architecture. The principle operation of IMC is the MAC step. The few-updated weight data is stored within the memory array, and the data to be proceeded is the input from the outside. Completing part or all of the calculation in memory can reduce the power consumption caused by data transfer in the calculation. According to computation signal type and implementation approach, IMC can be classified as digital [32], [33] and analog [18–20], [34–36] computing. The framework of digital and analog IMC are illustrated in Fig. 2.

Digital IMC merges embedded memories and Boolean logic block to form processing element (PE) unit. The acceleration
array is composed of multiple PE units. Input buffer and accumulator are responsible for data input and output, respectively.

Analog IMC retains the structure of the memory array and read-write function. External activation signals are input to each word-line (WL) through digital-to-analog converter (DAC) or pulse width modulation (PWM), and multiple rows are accessed at once. The DAC converts a digital quantity of input into a WL voltage value or the PWM adjusts the bit-cell current. Within the bit-cell, the weight data stored in the memory and the external input data are completed the AND operation to achieve the multiplication operation. According to Kirchhoff current law, the current flowing through each bit-cell is summarized on the bit line (BL). The result of the accumulation operation is expressed as the BL voltage drop or the voltage value on the output capacitor. Finally, an ADC converts the voltage amplitude into the digital output of memory-computation integrated block. Depending on the trade-off between precision and energy consumption, 4-8 bit ADCs are usually used in analog computing [19], [21].

Table I lists a literature study of recent IMC, including various types of memory and calculation methods. Compared with analog IMC, the digital way has the advantage of computational flexibility and accuracy. But its approach of combining logical units with bit-cells requires a lot of area overhead. The advantage of analog IMC is with high parallelism degree, which can bring enhanced throughput and energy efficiency than the digital way. Nevertheless, the design challenge of analog IMC is the design trade-off among accuracy, additional layout area and power consumption of analog components [14].

The main advantages of using static RAM (SRAM) for analog IMC are mature technology and fast computing speed. The binary logic stored in SRAM can be easily distinguished, allowing for high margins and computational linearity when multiple lines are turned on. The enhanced 8T SRMA bit-cell can effectively reduce the interference of computing to the storage data [34], [35]. [34] uses the charge sharing of multiple lines to realize the addition operation, reducing the power consumption caused by the BL current and improving the energy efficiency. In [36], the columns of DRAM are configured as charge-sharing cells, and the dot product operation is accomplished by non-destructive weight reading, saving peripheral circuit area and power consumption.

NVMs, e.g., Flash, PCM and RRAM show potential for analog computing because of high resistance ratio. [19] stores multi-bit signed numbers in a 2T-2M bit-cell, and uses ADC with adjustable precision to meet different computing requirements. In [20], the multi-bit input is split and computed. Under the premise of ensuring accuracy, this method implements MAC with multi-bit I/O unit.

MRAM cannot be directly used for analog IMC due to limited TMR. [37] proposes a new analog computing structure with operational amplifier integrator circuit, which uses the difference of the current flowing through $R_P$ and $R_{LP}$ to complete the calculation. This method alleviates the problem of...
limited TMR, but it has a high requirement on the performance of operational amplifier.

III. PROPOSAL OF ANALOG IN-MRAM COMPUTING

This section aims to solve major analog IMC design challenges: limited device TMR ratio, circuit nonlinearity and multi-bit computation configuration. The proposal refers to minimally modified memory array circuits. That is, universal bit-cell is used and the majority of MRAM peripheral circuits is retained. The dual-mode bit-cell is configured to realize magnified TMR ratio (m-TMR) for analog computing. Integrating current mirror with feedback can enhance the linearity of the analog calculation.

![Diagram of dual-mode MRAM](image)

**Fig. 3.** Floorplan of proposed in-MRAM computing. Modified (additional) peripheral blocks mainly include: dynamic latch, current mirror with feedback and SAR-ADC.

A. The floorplan of dual-mode MRAM

Fig. 3 illustrates the block diagram of in-MRAM computing. The operation includes normal storage and IMC mode. A mode controller selects the dual-modes according to CEN (computing enable) signal. In the storage mode, the MRAM bit-cell array (BCA) executes the read-write operation as standard memory. Alternatively, computing mode is executed with analog MVM, which consists of 16 MAC operations in equation (1). As shown in Fig. 3 the MRAM BCA is divided into 16 local BCAs, each corresponding to 16 MAC operations. W is stored in the local BCA as shown in equation (2). And X_{IN} is the activations from external input, which is converted into pulse signal of corresponding width after passing the counter. The multiplication is completed in the BCA, the accumulation is completed in the integrating current mirror. Finally, Y_{OUT} is calculated using a SAR-ADC and shift adders.

B. The dual-mode bit-cell

As shown in Fig. 4(a), 1T-1M bit-cell is applied to normal storage mode. The pass-transistor (PT) switch N2 is allocated for in-MRAM computing mode. Compared with universal 1T-1M cell, a PT interface PL is included to initiate in-MRAM computing. The 1T-1M bit-cell structure with PT switch is regulated with BL, WL, SL, PR and CEN signals. The latch unit is consisted of two transistors and a reference resistance (R_{ref}), as shown in Fig. 4(b). The resistance value of R_{ref} is setup between R_P and R_{AP} of MTJ. This specific value is determined according to the simulation results of power consumption and latch yield, which will be elaborated in Section IV. In the local BCA, latch unit and 1T-1M cell with PT switch are connected by WL and PR. The CENs of two cells control the mode of local BCA.

Fig. 4(c) shows the working principle of the storage mode. The CENs of two units are both low levels. Transistor N2 and N4 are cut-off, the proposed 1T-1M bit-cell is identical to conventional 1T-1M. It can complete read and write operations. In storage mode, W is stored in the local BCA and is the preparation for the in-MRAM computing. Compared to other storage such as SRAM, non-volatile MRAM has no static power consumption while holding data.

When CEN[n], CEN, BL, BR are high and SL is low, two cross connected units are in the computing mode. As shown in Fig. 4(d), the CENs of two units are both high, and two units are connected to form a latch structure. According to the resistance value of MTJ, high and low levels are generated on WL and PR to complete the latching operation. The magnetic orientation of the pinned layer is away from the transistor N1. When the resistance of MTJ is higher than R_{ref}, PR is with low level and WL is high. The MTJ is in AP state, and the magnetic orientation of the free layer is the same as the current. The high voltage difference between the two ends of
the MTJ does not affect the data stored in the MTJ.

### C. Local bit-cell array

![Fig. 5. The block diagram of local BCA. It mainly includes memory array using universal 1T-1M bit-cells, as well as additional PT switch array, reference-latch column and buffer-compute column in MRAM computing.](image)

![Fig. 6. Timing diagram of local BCA.](image)

Fig. 5 shows the block diagram of local BCA, which consists of the proposed 1T-1M dual-mode cell, PT switch array, reference-latch column and buffer-compute column. The WL connects all columns in the local BCA, and the WL of 16 local BCAs are isolated by the buffer of the buffer-compute column. The PT switch array controls connection between each bit-cell and the latch unit. In the computing mode, each column of the 1T-1M bit-cell array is connected with the reference-latch column in turn to generate high and low levels on each WL using the latch structure, as shown in Fig. 6. The buffer-compute column can prevent the local BCA from interfering with each other in the computing mode. Meanwhile, the buffer-compute column can amplify the weight signal on the WL to node W using the first stage inverter of the buffer. MTJ resistance is converted into the gate voltage of transistor N1 by the latch structure. The TMR is ultimately amplified to the m-TMR:

$$m\text{-TMR} = \frac{R_{off} - R_{on}}{R_{on}}$$  \hspace{1cm} (4)

where $R_{on}/R_{off}$ is the on/off resistance of transistor.

N1 and N2 are connected in series to complete the multiplication of W and IN. IN is the input pulse generated by the activations from external $X_{IN}$. The voltage is provided in the computing line (CL) of buffer-compute column, and different current $I_{CL,i}$ is generated in each row, which are calculated through CL and subsequent modules. According to Kirchhoff current law, the CL current $I_{CL}$ is given by:

$$I_{CL} = \sum_{i=0}^{m-1} I_{CL,i}$$ \hspace{1cm} (5)

where $I_{CL,i} = I_{th}$ when W[i] and IN[i] are high, otherwise $I_{CL,i} = 0$. The computing port CL and the read-write port BL are decoupled, which can improve the computation stability and the amount of data that can be simultaneously accessed.

### D. The associated current mirror and ADC

A local BCA corresponds to an integrating current mirror and a SAR-ADC. Fig. 6 shows the operation waveform of these modules. CMEN the enabling signal of integrating current mirror. Sample is the sampling signal of SAR-ADC, which overlaps with the CMEN to improve the speed of in-MRAM computing. At the end of sampling, SAR-ADC converts the sampling voltage, while the array continues to calculate the next column. The operation mode of pipeline can greatly shorten the calculation delay. The calculation delay of one column is given by:

$$T = T_{CEN} + T_{ADC}$$ \hspace{1cm} (6)

where $T_{CEN}$ indicates the latch and compute time, and $T_{ADC}$ is the conversion time of ADC. The more columns that are calculated, the less the average delay per column. The average delay of n columns is given by:

$$T_{AVG} = T_{CEN} + \frac{1}{n} \times T_{ADC}.$$ \hspace{1cm} (7)

### E. Operations of Input and Output

Table II lists the multiplication of 2-bit input and 1-bit weight. $X_{IN}$ is the input via buffer, then the counter generates
a set of pulses whose width \( T_{IN} \) corresponds to the value of the activation signal. This set of pulse is connected to the \( IN \) of the buffer-compute column (see Fig. 4), and determines the calculated current conduction time for each row of the buffer-compute column. \( T_{CP} \) is the period of the \( CP \) pulse. \( V_a \) represents the output voltage corresponding to the output result of \( \cdot 1 \).

**TABLE II**

| MTJ | W | \( x_{IN} \) | \( T_{IN} \) | \( V_{OUT} \) |
|-----|---|---------|--------|-------|
| P   | 1 | 0       | 0      | 0     |
|     | 01 | \( 1 \times T_{CP} \) | \( 1 \times V_a \) |        |
|     | 10 | \( 2 \times T_{CP} \) | \( 2 \times V_a \) |        |
|     | 11 | \( 3 \times T_{CP} \) | \( 3 \times V_a \) |        |

*Fig. 7.* (a) Circuit of integrating current mirror with feedback (CMF) structure. (b) The timing control logic circuit. (c) Waveform of computation control signals. \( V_{OUT,0/1/2/3/4} \) is the output waveform of different \( X_{IN} \).

**F. SAR-ADC**

**Fig. 8.** (a) Schematic of 4-bit SAR-ADC. (b) Operation waveform of SAR-ADC, when \( ADC\_OUT \) is ‘1010’.

SAR-ADC is commonly used in analog IMC because of its low cost in layout area and power consumption for multi-bits conversion. In this work, we use a 4-bit SAR-ADC as the important peripheral circuit of the analog in-MRAM computing. Fig. 8(a) presents a schematic of the 4-bit SAR-ADC comprising five weighted capacitors (\( C4-C0 \)), five switches (\( S4-S0 \)), SA and SAR logic for binary search algorithm. The capacitance ratio of \( C4, C3, C2, C1, \) and \( C0 \) is 8:4:2:1:1. The top plates of the five capacitors are shorted to the node \( P \) of the SA, and the total parasitic load at node \( P \) is 16 times that of \( C0 \).
Fig. 8(b) illustrates an example of the readout operation of 4-bit SAR-ADC. At the beginning of the readout operation, the voltages at node P (V_P) and node N (V_N) are initially set to a common voltage V_{COM} (V_P = V_N = V_{COM}). After setting the input node to the analog input voltage V_{IN}, all five switches (S4-S0) are switched from V_{IN} to ground to decrease V_P by (16/16) × V_{IN} via ac coupling of C4-C0, such that V_P = V_{COM} − V_{IN}.

After the sampling is completed, it enters the conversion phase. In this phase, the SAR logic generates a control signal to switch S4 from ground to the reference voltage (V_{REF}), which supplied by the band gap reference, to increase V_P by (8/16) × V_{REF}. Thus, V_P = V_{COM} − V_{IN} + 1/2V_{REF}. V_P is compared with V_N to determine whether V_P is higher or lower than V_N, which is essentially the comparison of V_{IN} and 1/2V_{REF}. The output of the SA is sent to the SAR logic to determine the control of the capacitor switches in the next operation phase. When V_P>V_N, it means that V_{IN}<1/2V_{REF}, in the next operation phase, the SAR logic generates a control signal to switch S4 from V_{REF} to ground and switch S3 from ground to V_{REF} to decrease V_P by (4/16 − 8/16) × V_{REF}. Thus, V_P = V_{COM} − V_{IN} + 1/4V_{REF}. When V_P>V_N, the SAR logic generates a control signal to switch S3 from ground to V_{REF} to increase V_P by (4/16) × V_{REF}. Thus, V_P = V_{COM} − V_{IN} + 1/2V_{REF} + 1/4V_{REF}. After 4 operation phases, the SAR logic will determine 4-bit digital code to get the final readout of the SAR-ADC.

In summary, analog in-MRAM computing was realized based on the above-mentioned proposal, using modified MRAM peripheral circuits implementation and device-circuit interaction design methods. Limited device TMR ratio can be addressed peripheral circuit within 1T-1M bit-cell based MRAM macro. The m-TMR formed by latching structure can meet the requirements of analog calculation. Circuit nonlinearity can be alleviated by the proposed CMF, which adds two additional transistors outside the current mirror. Multi-bit computing configuration allows analog computation by splitting data, converting it to a digital signal and then producing the result by a shift adder.

### IV. EXPERIMENTAL RESULTS

The proposed m-TMR enlargement approach, analog in STT-MRAM computing circuits and system are verified and simulated with Spectre in Cadence Virtuoso front-end, using 28-nm CMOS process design kits and MTJ VerilogA compact model [39, 40]. The simulation conditions are typical-typical (TT) corner, 27°C, and the supply voltage (V_{dd}) is 900 mV. Table III lists fundamental MTJ parameters used in our analysis. MTJ physical parameter conforms to a commercial 40-nm critical dimension (CD) MTJ physical parameters. The effective low-resistance R_P of MTJ is 6 kΩ with spin aligned ferromagnetic electrodes. An initial 200% TMR ratio is configured.

#### A. Power consumption of latch structure

The reference resistance R_{ref} and the latching voltage (V_l) in latch structure affect the yield and power consumption. In order to reduce power consumption and improve latch variability performance, 5000 Monte-Carlo runs analysis is performed for R_{ref} and V_l under different TMR, and the 1-bit latch power consumption under different conditions is evaluated. Comprehensive analysis of the influence of R_{ref} and V_l on latching and selection of appropriate parameters can reduce power consumption and improve yield.

| Parameters | Description | Default Value |
|------------|-------------|---------------|
| ∆H_{0}    | Activation energy | 0.8 eV       |
| T          | Field acceleration | 1.5 cm/MV   |
| β          | Shape parameter   | 1.5          |
| k_{B}      | Boltzmann constant | 8.625 × 10^{-2} eV/K |
| T_{0}      | Ambient temperature | 300 K       |
| Variable   | Description     | Default Value |
| Oxide barrier thickness of | 0.85 nm  |
| Area       | MTJ surface     | 40 nm - 40 nm - 0.4 |
| t_{sl}     | Thickness of free layer | 1.3 nm      |
| V_{dd}     | Volume of free barrier | 5.5 nm       |

### TABLE III

Physical parameters of STT-MTJ for in-MRAM computing performance simulation

| Parameters | Description | Default Value |
|------------|-------------|---------------|
| R_{ref} (kΩ) | Reference resistance | 7.7 kΩ |
| V_l (mV)   | Latching voltage | 700 mV |
| Power (fJ) | Power consumption | 97.8 fJ |
| Yield (%)  | Yield (%) | 75.8 % |

#### TABLE IV

Simulated latch performance with different TMR ratio

| TMR (%) | R_{ref} (kΩ) | V_l (mV) | Power (fJ) | Yield (%) |
|---------|--------------|----------|------------|-----------|
| 50      | 7.7          | 700      | 97.8       | 75.8      |
| 100     | 8.5          | 600      | 78.4       | 86.8      |
| 150     | 9.0          | 600      | 74.3       | 93.8      |
| 200     | 9.5          | 600      | 70.8       | 95.2      |
| 250     | 9.5          | 600      | 68.8       | 97.5      |

Fig. 9(a) and 9(b) show the failure probability of latch ‘1’ and ‘0’ under different conditions. In order to estimate the latching yield of in-MRAM computing, the voltage of the node W greater than 750 mV is ‘1’, less than 150 mV is ‘0’, and all other voltages are latching faults. The yield is sensitive to the change of reference resistance R_{ref}, and the latch voltage V_{latch} has different effects on the yield under different reference resistance R_{ref}. To ensure the overall yield of the latch structure, the two cases need to be considered comprehensively, and the average failure rate is shown in Fig. 9(c). When the reference resistance R_{ref} is 8.5 kΩ, 9 kΩ and 9.5 kΩ, and the supply voltage V_l is 700 mV, 700 mV and 600 mV respectively, the failure rate maintains a low level. Considering the power consumption simulation results in Fig. 9(d), the reduction of latch voltage V_{latch} has a great impact on latch power consumption. Therefore, we select reference resistance 9.5 kΩ and supply voltage V_{latch} to obtain 95.2% accuracy and 70.8 fJ power consumption. Compared with the case of 900 mV power supply voltage as V_{latch}, the result of comprehensive analysis is that the failure rate is reduced by 56.4% and the power consumption is reduced by 66.7%.

The optimal R_{ref} and V_l are obtained after trading off yield and power consumption, as summarized in Table IV. The higher the TMR, the higher the yield and the lower the power consumption. After amplification by the inverter, the m-TMR is not related to the initial TMR ratio. TMR only affects the
the degree to which the actual curve deviates from the ideal transformation curve along the longitudinal axis, indicating difference between the transformation curve and the ideal of TCM and CMF. Integral nonlinearity (INL) refers to the results. Charging current increases of output voltage in Fig. 10(a). The ability of the CMF can be adjusted by the voltage of the input pulse, $\gamma$ of the CMF structure and the capacitance of capacitor C1.

yield. Simulation results show that the m-TMR is about 15000.

B. Enhanced INL

The contrast of waveforms between proposed CMF structure and traditional current mirror (TCM) is demonstrated in Fig. 10a). $V_{\text{BIAS}}$ of the TCM stays the same, thus the charging current $I_{\text{OUT}}$ of the output capacitor decreases with the increase of output voltage $V_{\text{OUT}}$. As a comparison, $V_{\text{BIAS}}$ of the CMF decreases 80mV with the increase of $V_{\text{OUT}}$, so $I_{\text{OUT}}$ can be kept constant to enhance the linearity of the results.

Fig. 10b) and 10c) show the $V_{\text{OUT}}$ versus the ideal output of TCM and CMF. Integral nonlinearity (INL) refers to the difference between the transformation curve and the ideal transformation curve along the longitudinal axis, indicating the degree to which the actual curve deviates from the ideal curve. Comparing the INL of the TCM and the CMF, it can be found that adding feedback structure significantly improves output linearity. In Fig. 10b), the maximum value of INL is 1.014 LSB; the maximum value of INL in Fig. 10c) is only 0.430 LSB. The INL can be reduced by 57.6% by using a feedback structure.

The output voltage range is highly depended on the calculation margin. However, the nonlinearity of the analog calculation increases as the output voltage $V_{\text{OUT}}$ approaches the supply voltage $V_{\text{dd}}$ of 900 mV. The ability of the CMF structure to enhance linearity is limited. The maximum $V_{\text{OUT}}$ should be limited to 650 mV for regular CMF operation. The maximum $V_{\text{out}}$ can be adjusted by the voltage of the input pulse, $\gamma$ of the CMF structure and the capacitance of capacitor C1.
C. Analog in-MRAM computing results

The computation task with 4 accumulations of 2-bit inputs and 1-bit weights (2bIN-1bW-4Acc) is executed. The transition simulation results of \( V_{OUT} \) is shown in Fig. 10(d). The waveform from bottom to top correspond to the calculated results 0 to 12 respectively. The charging time \( T_{CH} \) of each cycle is 800 ps. Around 4 ns, the difference between adjacent curves gradually decreases from bottom to top, and the minimum is 46 mV. This is due to the nonlinearity of the analog calculation. Before 4 ns, the SAR-ADC completes sampling of \( V_{OUT} \). After 4 ns cycle, the SAR-ADC performs analog-to-digital conversion, the output capacitor discharges, and the array latches the next column of weight data.

In order to reflect the influence of proposed 1T-1M on the calculation, the in-MRAM computing structure of 1T-1M is also simulated under the same simulation conditions. Fig. 10(e) shows the \( V_{OUT} \) of conventional 1T-1M array and proposed 1T-1M array under different TMR. For conventional 1T-1M array, as TMR increases, the influence curve of \( W \) is close to that of \( X_{TH} \). The difference between the two curves is too big to match together, and the analog calculation cannot be realized. On the contrary, the proposed 1T-1M uses latches to magnify the m-TMR by 7500 times when TMR equals 200%, and the two curves almost coincide. Different TMR only affects the yield of latched results, but has no effect on the the influence curve of \( W \). As shown in Fig. 10(f), digital output quantized by 4-bit SAR-ADC is close to the ideal output. The maximum INL is 1.25 LSB.

D. Analysis of overall energy efficiency

Fig. 11(b) shows the energy efficiency and in-MRAM computing latency versus conventional digital MRAM. As the number of open rows increases, the parallelism of in-MRAM computing increases, and the energy efficiency advantage becomes more obvious. When 64 rows open, the proposed structure achieves 25.4 TOPS/W which is 3.05 times more than conventional MRAM. The delay of in-MRAM computing cannot change as the amount of calculated data increases and is 83.8% of digital MRAM when 64 lines are turned on.

V. Conclusion

The performance of recent in-memory computing of NVMs is compared in Table V. Indeed, STT-MRAM based IMC shows little superiority of energy efficiency over the other NVMs. This is mainly due to its intrinsic low TMR ratio. The process of latching magnetoresistance difference to generate the amplified m-TMR requires at least one-third of the comprehensive analog in-MRAM computing power consumption. The advantages of STT-MRAM over other memory are low writing voltage and low process deviation. Logic compatible writing voltage (e.g., 0.9 V with 28nm CMOS) can be applied for ultra-low power operation. Device variability induced unreliable effects can be partially alleviated when using STT-MRAM for analog IMC.

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A favorable scenario of in-MRAM computing could be artificial intelligence applications on Internet of things (IoT) edge devices, as normally-off and instant-on storage and computing units, e.g., emphasized energy cost in sleep-mode [41]. In this paper, an analog in-MRAM computing structure is proposed and experimentally realized. On the basis of commercial 1T-1M bit-cell, modified 1T-1M bit-cell builds the latch structure through the peripheral circuit. The m-TMR obtained from simulation can reach a maximum of 15000, which meets the requirements of analog calculation. The proposed CMF adds feedback current stabilization on the basis of traditional current mirror, and the INL is reduced by 57.6%. The energy efficiency of the entire computing architecture reached 25.4 TOPS/W (2bIN-1bW-64Acc), which is 3.05 times that of the traditional digital MRAM.
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