BSC: Block-based Stochastic Computing to Enable Accurate and Efficient TinyML

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Abstract—Along with the progress of AI democratization, machine learning (ML) has been successfully applied to edge applications, such as smart phones and automated driving. Nowadays, more applications require ML on tiny devices with extremely limited resources, like implantable cardioverter defibrillator (ICD), which is known as TinyML. Unlike ML on the edge, TinyML with a limited energy supply has higher demands on low-power execution. Stochastic computing (SC) using bitstreams for data representation is promising for TinyML since it can perform the fundamental ML operations using simple logical gates, instead of the complicated binary adder and multiplier. However, SC commonly suffers from low accuracy for ML tasks due to low data precision and inaccuracy of arithmetic units. Increasing the length of the bitstream in the existing works can mitigate the precision issue but incur higher latency. In this work, we propose a novel SC architecture, namely Block-based Stochastic Computing (BSC). BSC divides inputs into blocks, such that the latency can be reduced by exploiting high data parallelism. Moreover, optimized arithmetic units and output revision (OUR) scheme are proposed to improve accuracy. On top of it, a global optimization approach is devised to determine the number of blocks, which can make a better latency-power trade-off. Experimental results show that BSC can outperform the existing designs in achieving over 10\% higher accuracy on ML tasks and over 6\times power reduction.

I. INTRODUCTION

With the rapid development of artificial intelligence (AI), deep neural networks (DNNs) as typical models of machine learning (ML) have been widely used on edge applications. Recently, there are growing demands on the implementation of DNNs to tiny devices \cite{1}, such as surveillance cameras in smart housing and implantable cardioverter defibrillator in intelligent healthcare, which is known as TinyML. However, the energy supply (e.g., battery) of tiny devices is extremely limited, impeding the implementation of DNNs. Although many compression technologies \cite{2-8} through compacting models can save energy to a certain extent, it falls into low accuracy when the compression rate becomes high. For TinyML, stochastic computing (SC) \cite{9-13} stands out to save energy by significantly simplifying computing circuits.

SC utilizes the probability of ‘1’s in the whole bitstream to represent data. For example, bitstream 0100 indicates 1/4 in unipolar format, but -2/4 (i.e., 2\times1/4-1) in bipolar format. Regarding the data representation in SC, basic arithmetic operations such as addition and multiplication can be implemented by one simple gate instead of the traditional binary implementations with tens of gates \cite{14}. For example, we can use an AND gate for unipolar and an XNOR gate for bipolar to approximate multiplication, and use an OR gate to approximate addition. In contrast to conventional binary circuits, an SC circuit can significantly simplify hardware complexity and save energy.

However, SC usually suffers from low accuracy on basic ML operations (e.g., multiply-accumulate (MAC) and general matrix multiplication (GEMM)) and long computing latency. The accuracy is affected by the design of arithmetic units and data precision. Specifically for arithmetic units, the accuracy issue is mainly from two aspects. One is the correlation among inputs, which causes that the results of logic operating cannot be consistent with probability computing. The other is the overflow problem, it is ubiquitous when the accurate results exceed -1 or 1. Besides, existing works \cite{15,16} increases the length of bitstreams to improve data precision, even using exponential bits to obtain accurate results. But, this will undoubtedly introduce long computing latency.

To deal with the long latency problem, in this work, we first divide bitstreams into blocks and execute them in parallel to reduce latency. In this way, arithmetic units inside every block are required to have high accuracy. The correlation and overflow may cause accuracy loss in every block. Meanwhile, block division also brings inter-block inaccuracy problem. To alleviate these accuracy problems, we propose optimized intra-block arithmetic units which can provide high computing accuracy. Moreover, we develop the inter-block output revision (OUR) scheme to address missing ‘1’s or redundancy ‘1’s problem among blocks. Finally, a novel strategy is devised to determine the number of block to make a better trade-off between latency and power.

The main contributions of this paper are listed as follows.

- We propose a novel architecture, namely BSC, where the inputs are divided into blocks and executed them in parallel using optimized intra-block arithmetic units.
- A new output revision (OUR) scheme is designed to solve the inter-block inaccuracy problem. Besides, we first propose a novel heuristic strategy to guide block division for better latency-power trade-off.
- Comprehensive experiments are conducted and the results show that our methods can achieve higher accuracy on ML tasks than existing methods with the reduced latency and pipeline stalls, as well as over 6\times power reduction compared with binary circuits.

The paper is organized as follows: In Section II, we present the background and motivations of this work. Section III presents our design. Evaluation results are reported in Section IV. Section V concludes this paper.

II. BACKGROUND AND MOTIVATION

A. Related Work

In order to obtain accurate results, long bitstreams are used to improve accuracy. Deterministic SC \cite{17} utilizes exponential bits to produce accurate results compared with floating point (FP). However, it brings unacceptable long latency.

In addition, arithmetic units also influence the accuracy of MAC and GEMM. On the one hand, for multiplier, work \cite{18}...
concluded that the inaccuracy is maximal when the multiplication result is zero using the XNOR gate. So it removes near-zero operands. However, it works only if we know the value of operands in advance. Work [19] proposed a new sign-magnitude data format to optimize multiplier, but its adder can only compute one input in one adder, which is unfriendly for computing pipeline and increases the latency. Therefore, we utilize the sign-magnitude data format to improve the accuracy of multiplier, and redesign the adder for this format.

On the other hand, for adder, many works [20, 21] lacked the bipolar non-scaled addition for MAC and GEMM in DNNs, without saying for sign-magnitude format. Work [13, 16] proposed a separated adder for the sign-magnitude format, but it is greatly influenced by overflow problem. Therefore, we design new adder to mitigate overflow problem.

B. Challenges and Motivation

**Challenge 1: High Data Precision Requires Long Computing Latency.** In SC, high data precision is often required to obtain high accuracy. Specifically, in deterministic SC [17], to process m n-bits inputs, $2^m \times \log_2 n$-bit bitstreams must be generated. Obviously, the computing time increases exponentially, leading to unacceptable latency. To shorten latency, we propose a block-based architecture, namely BSC, which divides inputs into blocks and executes blocks in parallel. In this way, to obtain high computing accuracy, the accuracy of arithmetic units in every block must be guaranteed.

**Challenge 2: Correlation Problem in Basic XNOR Multiplier and OR-tree Adder.** In SC, multiplier and adder are two critical arithmetic units. As the basic circuits, XNOR multiplier and OR-tree adder [22] cannot obtain high accuracy with bipolar because of strong correlation among inputs [22]. If inputs are all independent, those operations can get a high accuracy. However, there are often correlations among inputs. For example, the addition of two bipolar inputs $a + b = c$ can be computed correctly using OR gate if and only if their corresponding bitstreams A and B are exclusive.

To mitigate the correlation issue, the work [19] proposed ‘sign-magnitude’ format, which expresses data using absolute value with an additional sign bit in front, to optimize XNOR multiplier. However, their implementation in a sequential manner still faces long latency due to the single-input adder. To shorten the latency, the parallelism might be introduced but we may need to redesign the arithmetic units to adapt to this format and can handle multiple inputs for addition.

**Challenge 3: Separated Adder Suffers from Severe Overflow Problem.** For sign-magnitude data, we do multiplication using XNOR gate for sign bit, and AND gate for magnitude. For addition, if all the data have the same sign, they can be added using an unipolar adder, and the sign of the result can be obtained directly. In MAC and GEMM operations, multi-inputadders are needed. However, the existing studies face the overflow issue severely to implement multi-input adders. For example, in [13], inputs are divided into positive and negative parts according to sign bits. It performs an OR tree for the summation of $POS$ and $NEG$. Then it utilizes scaled addition to compute $\frac{POS - NEG}{2}$, which exactly is the expression of bipolar $POS - NEG$. However, the mean absolute error (MAE) of the separated adder is high (shown in Section IV-A). Because the results of $POS$ and $NEG$ are often overflow for multiple inputs, which lead to $POS = 1$ and $NEG = 1$. So

$$\begin{align*}
\text{POS} & = 1 \quad 1 \quad 1 \quad 1 \\
\text{NEG} & = 1 \quad 1 \quad 1 \quad 1
\end{align*}$$

Fig. 1: An example of multiple inputs addition with separated adder. There are total 5 inputs, 3 positive inputs and 2 negative inputs. $\text{POS} - \text{NEG} + 1 = 1/2$ (i.e., 0 in bipolar). We give an example in Figure 1 to explain this phenomenon clearly. So, parallel computation without input scaling will magnify the overflow problem, which leads to huge accuracy loss.

Therefore, we propose an optimized merged adder to mitigate the correlation and overflow problems to improve the computation accuracy for multi-input adders inside blocks.

III. DESIGN OF THE BSC ARCHITECTURE

A. Overview of BSC

In order to improve accuracy and reduce computing latency, we propose a block-based SC architecture, namely BSC, which divides inputs into blocks and executes multiplication and addition in parallel. In this way, the computing latency is obviously reduced. Moreover, we utilize the sign-magnitude format to mitigate correlation problem for multiplier. Meanwhile, we design accumulator-based adder to ensure intra-block addition accuracy (see Section II-B) and OUR scheme (see Section II-C) to solve inter-block inaccuracy problem. Besides, a heuristic strategy of block division (see Section II-D) is proposed to determine the number of block. This strategy takes all accuracy, latency and energy into consideration. Figure 2 illustrates the overview of our proposed BSC architecture. We introduce its details as follows.

B. Intra-Block: Accumulator-based adder

For multiplier, we directly apply XNOR+AND gates between inputs to mitigate correlation of bipolar computing. As indicated in Section II-B, traditional adders suffer from correlation problem in the OR adder and overflow problem in the separated adder. In order to address these problems, inside every block, we design a new accumulator-based adder for sign-magnitude format as demonstrated in Figure 3. The new adder takes advantage of uNSADD adder [24] to compare the real accumulated ‘1’s in inputs and output to determine the output bit. In every cycle, the accumulators of positive and negative parts are subtracted to calculate real accumulated ‘1’s so far. This merged accumulator mitigates the impacts of correlation and quick overflow problems. Meanwhile, the adder maintains the uniform of output, which decreases the effects of correlation for next computation.

Firstly, all inputs are entered into the parallel counter (PC). In every cycle, one bit of every input is accumulated into accumulators in parallel. The accumulation is processed separately for positive and negative parts to their own accumulators (marked as $A_p$ and $A_n$ in the figure). Secondly, subtract two accumulators. In this stage, we do not know the sign of output, so we use circuits to calculate $A_p - A_n$ and $A_n - A_p$, respectively. This step aims to get the number of accumulated ‘1’s of all inputs so far. Then, one bit of two temporal
Stage 1: Block Division

Stage 2: Intra-Block Computation

Stage 3: Inter-Block OUR Scheme

Fig. 2: Overview of BSC. There are 3 stages: (1) block division; (2) intra-block computation in parallel; (3) revise output.

Outputs \(S_{op}\) and \(S_{on}\) are obtained by comparison. Finally, after \(n\) cycles, we compute the sign bit and select the correct output result from \(S_{op}\) and \(S_{on}\) according to \(A_p\) and \(A_n\). The temporal \(S_{op}\) and \(S_{on}\) are computed based on the comparison of \(A_p - A_n / A_n - A_p\) and \(A_{op} / A_{on}\). If \(A_p - A_n\) is larger than \(A_{op}\), which accumulates the number of ‘1’s in the temporal output so far, then \(S_{op}[t] = 1\). Otherwise, \(S_{op}[t] = 0\), where \(t\) is the index of the temporal output. Then, \(A_{op} = A_{op} + S_{op}[t]\). Initially, \(A_{op} = 0\). The same is true for \(S_{on}\).

Now, we provide an example (shown in Figure 3) to explain the accumulator-based adder. In example, there are five inputs. \(A_p\) and \(A_n\) are accumulated based on the inputs in every cycle. For example, in Cycle 2, \(A_p = 4\) means the first two bits of positive inputs have total four bits. Then \(A_p - A_n\) and \(A_n - A_p\) are calculated respectively. \(A_{op}\) and \(A_{on}\) are set as 0 initially, and accumulate ‘1’s according to \(S_{op}\) and \(S_{on}\) in every cycle. Compared with \(A_{op}\) and \(A_{on}\), \(S_{op}\) and \(S_{on}\) are determined. Finally, we compare \(A_p\) and \(A_n\) in Cycle 5 to obtain sign bit 1 and select the corresponding output 1100. We find that in this case the error is eliminated by the adder compared with the separated adder. However, it will bring pipeline stalls because we can’t know the sign bit immediately. The pipeline stalls may be reduced with the number of block increasing.

C. Inter-Blocks: Output Revision (OUR) Scheme

Although the intra-block adder can alleviate correlation and overflow problems well, the block division brings new inter-block inaccuracy problem. For multiplier, it does not have this problem since its inputs are XNORed and ANDed. However, for adder, the number of ‘1’s in the output of each block may be more or less than the accurate result, which makes the errors among blocks are exacerbated. We give following two examples to explain the problem.

In Figure 5 we list two cases of block computing with errors. The accurate results of two cases are both 2/4. We omit detailed processes for more concise understanding. In CASE 1, most of ‘1’s in the greater part (i.e., positive part in the figure) appear at the end of bitstreams, and most of ‘1’s in the lower part (i.e., negative part in the figure) appear in the front of bitstreams. This case causes that the remained accumulated ‘1’s finally have no place to fill them, which induces the number of ‘1’s in this block is less than the accurate result. In CASE 2, the situation is exactly opposite. Most of ‘1’s in positive part appear in the front of bitstreams and most of ‘1’s in negative part appear at the end of bitstreams. In this case, there are more ‘1’ in this block than that of the accurate result. Without the block division, this problem occurs only once in the whole bitstreams. However, because of block division, these cases may occur in every block, which induces inaccuracy among blocks.

To solve this inter-block inaccuracy problem, we propose an OUR scheme to fill/remove ‘1’s after parallel intra-block computation without any additional latency cost. OUR scheme is shown in the Stage3 of Figure 2. First, we calculate the summation of \(A_p\), \(A_n\) and \(A_o\) from all blocks. \(A_p\), \(A_n\) and \(A_o\) identify the number of ‘1’s of positive data, negative data, and output in every block. \(\Psi\) and \(\Phi\) in Figure 2 refer to \(\sum A_p - \sum A_n\) and \(\sum A_o\). \(\Psi\) and temporal output, which consists of the output of every block, are compared and judged to execute ‘1’s filling/removing process. If \(\Psi\) is larger than \(\Phi\), that means the accurate number of ‘1’s is larger than the temporal output, so the filling process is launched. On the contrary, the removing process is executed.

Figure 6 is an example to demonstrate the filling process of OUR scheme, in which the input bit-length is \(n = 8\) and the number of block is \(k = 2\). The inputs of both two blocks are
from CASE 1 in Figure 5. In Figure 6, intra-block computation is executed in Cycle 1-4, and filling process is performed from Cycle 5-13. \( \Psi = 6 + 6 - (4 + 4) = 4 \), \( \Phi = 1 + 1 = 2 \) and the sign bit are computed in Cycle 5. In next two cycles, \( \Psi \) is larger than \( \Phi \) and temporal output \( t = 0 \), so we fill ‘1’s at these two positions. After Cycle 6 and 7, \( \Psi \) is equal to \( \Phi \), so the remaining bits can be output directly in every cycle. Without OUR, the computation based on blocks also needs 13 cycles until every bit is output, while OUR makes the addition deterministic. As the number of blocks increases, the total cycles of intra-block computation can be further decreased.

D. Heuristic Strategy for Block Division

Regarding the proposed BSC, how to determine parallelism is a critical question. Because we divide bitstreams into blocks, the parallelism refers to the number of blocks. Aiming to select a good number of blocks, we propose a novel heuristic strategy to balance among accuracy, latency, and power.

① On the accuracy side, the number of blocks impacts the accuracy of proposed intra-block adder. For our accumulator-based adder, the sign bit in every block is judged locally. If the local sign bit is inconsistent with the global sign bit, the output of this block may produce large errors (because it selects the opposite-sign result as output), which leads to even more overhead for the OUR scheme to fill/remove ‘1’s. Moreover, more ‘1’s filling/removing may break the uniform distribution of outputs when ‘1’s‘0’s become dense, which will exacerbate the correlation problem in later multiplication. To ensure the local sign bit has a high probability of being consistent with the global sign bit, we propose a heuristic strategy.

For every block, we utilize the average value to represent the size of positive and negative parts. In this way, the judgment of two parts can be simplified to the judgement of two average bitstreams. Next, we search for the minimal bit-length \( d \) of blocks to make the correct probability of local sign bit judgment larger than \( \theta \), which is an acceptable probability threshold. The more ‘1’s the bitstream has, the larger value this bitstream represents. If the average bitstream of positive and negative parts are represented as \( AVG_{POS} \) and \( AVG_{NEG} \), and the corresponding values are \( p \) and \( q \), the probability of \( p \geq q \) can be expressed as:

\[
P(p \geq q) = \sum_{i=0}^{d} C_d^i p^i (1-p)^{d-i} \sum_{j=0}^{i} C_d^j q^j (1-q)^{d-j},
\]

where \( i \) refers to the number of ‘1’s in \( AVG_{POS} \) and \( j \) refers to the number of ‘1’s in \( AVG_{NEG} \). From the equation, \( i \) is always greater or equal to \( j \). Therefore, the correct probability of two average values is:

\[
Probability = \begin{cases} 
P(p \geq q) & p \geq q \\ 1 - P(p \geq q) & p < q 
\end{cases}
\]

We enumerate all \( p \) and \( q \) range from 0 to 1 with step 0.1, and calculate the probability that the two average values can be correctly judged. Then, we can determine the minimal bit-length for every block where the correct probability is greater than \( \theta \). Results will be shown in Section IV-C.

② As we know, when the bitstreams are executed in parallel, the latency can be shorten multiple times according to the number of blocks. However, the hardware implementations become more complex. In order to trade-off between latency and hardware cost, a constraint is set. That is, the hardware power consumption of BSC must be lower than FP.

Therefore, combining above two factors, the number of block can be determined heuristically, which brings better accuracy, lower latency and saved power.

IV. EXPERIMENTS

A. MAE Evaluation of Adders

Adders as the dominant arithmetic circuits are first evaluated in this subsection. Note that all FP inputs are randomly generated and converted to bitstreams using Sobol generator.

Setup. We demonstrate the comparison of six types of adders, including OR-tree adder (ORADD), separated adder (SEPADD),adder in uGEMM [24] for bipolar (uNSADD), our proposed intra-block adder (ACCADD), block-based adders without OUR (BLKADD), and with OUR (RBLKADD). Experiments show the MAE of adders under different number of inputs. Every bitstream is represented using 64 bits, and the number of block for BLKADD and RBLKADD is set as 4. Results are shown in Figure 7.

Results. Figure 7 demonstrates that with the number of inputs increasing, MAE shows an upward trend among adders because of the overflow problem, which is inevitable when the number of inputs get large. However, we find that SEPADD can’t afford this overflow problem when the number of inputs is only 4, while its MAE is so low when executes 2-inputs addition. Even the MAE become higher than ORADD when the number of inputs is 16. For ORADD, correlation problem always keeps strong. Other 4 adders are much better than ORADD and SEPADD. Our proposed RBLKADD is the best
because it alleviates the correlation and overflow problems using sign-magnitude format and intra-block ACCADD. So it is better than uNSADD. Moreover, it utilizes OUR scheme to make up errors caused by ACCADD and inter-block inaccuracy problem, which brings errors in BLKADD.

B. MAE Evaluation of GEMM

This subsection evaluates the efficiency of proposed BSC architecture using GEMM operation. 

Setup. We compare XNOR-OR (XNOR multiplier and OR-tree adder for bipolar), AND-SEP (AND multiplier and separated adder for sign-magnitude), uGEMM (proposed by [24]), AND-ACC (AND multiplier and accumulator-based adder for sign-magnitude), BSC* (BSC without OUR) with our BSC. Experiments show GEMM results of two $16 \times 16$ matrices. We explore the impact of input bit-length on these methods. For BSC* and BSC, the bit-length $d$ in every block is set as 16. When the input bit-length is lower than $d$, the number of block is set as 1. Results are shown in Figure 8.

Results. For XNOR-OR and AND-SEP circuits, because their adders suffer from severe correlation and overflow problems when the number of input is 16 (see in Figure 7), the MAE can’t reduce with precision increasing. They always keep high MAE. For other 4 circuits, with the bit-length increasing, computation becomes more accurate. This is because these circuits can deal with multiple inputs well. As the same as Section IV-A, our proposed BSC obtains best results because of proposed intra-block adder and inter-block OUR scheme.

C. The Number of Block Exploration

In this section, the number of block is explored according to Section III-D. The number of block is determined heuristically from accuracy and latency-power aspects.

a) From the accuracy aspect, we search the minimal bit-length of every block through Equation 2. We enumerate $p$ and $q$ in range $[0, 1]$ with step 0.1, which includes total $11 \times 11 = 121$ combinations. Figure 9 show the correct probability of size judgment using 12 bits. For example, when $p = 0.2$, $q = 0.3$, $P(0.2 < 0.3) = 0.63$. The $d$ with an average probability greater than the threshold $\theta$ we set will be finally selected. In our experiments, $\theta$ is set as 90%. Through exhaustive search, the average probability becomes greater than $\theta$ when $d = 12$, that means there is more than 90% probability that the size of two 12 bits bitstreams can be judged correctly. This method can guarantee the addition accuracy inside every block, reduce the cost of OUR scheme and keep output relatively uniform.

b) From the latency-power aspect, a power constraint is set to find the adequate number of block. Table I shows computing cycles, pipeline stalls, MAE and power consumption for MAC operation of two 16 dimensions vectors under different number of blocks. We only choose the number of block that can be divided by input bit-length exactly. bitstreams are represented using 64 bits. SC circuits are implemented by Bluespec SystemVerilog, then compile to Verilog to evaluate power consumption on Vivado v2020.2.

The first column of Table I identifies different number/bit-length of blocks and methods. Results show that compared with BSC*, our BSC can improve the accuracy without any additional cycles. But the power grows greatly with the parallelism increasing. For FP computing, the power of MAC for two 16 dimensions vectors is 34.6W. So we select the number of block lower than 32 for 64-bits inputs.

Therefore, combine the results of a) and b), we choose $k = 4$ and $d = 16$ as the recommended number and bit-length of

| Design   | Cycles | Stalls | MAE   | Power (W) |
|----------|--------|--------|-------|-----------|
| 1/64 Ours BSC* | 130    | 64     | 0.314 | 2.17      |
| 2/32 Ours BSC* | 98     | 32     | 0.362 | 3.35      |
| 4/16 Ours BSC* | 82     | 16     | 0.305 | 5.74      |
| 8/8 Ours BSC* | 74     | 8      | 0.346 | 10.86     |
| 16/4 Ours BSC* | 70     | 4      | 0.508 | 21.02     |
| 32/2 Ours BSC* | 68     | 2      | 0.332 | 41.31     |
| 64/1 Ours BSC* | 67     | 1      | 0.352 | 81.02     |

TABLE I: Results of the number of block exploration on MAC under BSC and BSC* circuits.
block when data is represented as 64 bits. In this way, the computing latency can be reduced as much as possible. And we can achieve over $6 \times$ power saving than FP circuit. For other data precision, the process is similar.

### D. Evaluation of Latency

In this subsection, we compare the cycles, pipeline stalls and MAE of 6 circuits for MAC. Table II demonstrates the results of two 16 dimensions vectors with 64-bits, $k$ is set as 4 in method BSC* and our BSC.

From Table II, we see that our BSC will produce a little higher cycles and pipeline stalls than first 3 circuits. But we achieve $3.6 \times$, $3.1 \times$ and $1.2 \times$ accuracy improvement than them. The improvement can be larger in MLP implementation because errors will be accumulated among thousands of MAC. We also observe that BSC has similar MAE than AND-ACC, but BSC saves lots of cycles because of parallel computing. Therefore, in the next case study of MLP, we remove comparison with this method. Compared with BSC*, ours can improve accuracy without additional cycles. Besides, BSC implements deterministic adder because of OUR, its latency is much lower than deterministic circuits with $2^{16 \log_{16} 64} = 2^{96}$ cycles.

### E. MLP Implementation

Finally, we implement MLP as a study case to show the strength of our proposed BSC on ML.

We develop a custom SC simulator integrated with PyTorch to implement these circuits. The MLP is 3-layers perceptron with 32 and 64 hidden neurons. We first train the MLP model 30 epochs using FP, then implement MLP using above 5 circuits. The inference accuracy (shown in Table III) is evaluated on the MNIST dataset. Results show that our method can achieve the best inference accuracy. And there is only 0.7% accuracy gap compared with FP.

### V. CONCLUSION

This work present a block-based SC architecture, namely BSC, aiming at improving the accuracy of SC arithmetic circuits, reducing computing latency and saving energy. BSC divides inputs into blocks, then they are executed in parallel. We propose a novel intra-block accumulator-based adder and inter-block output revision (OUR) scheme to improve accuracy. Moreover, we propose a heuristic strategy to determine the number of block, which takes accuracy, latency and power consumption into consideration. Results show that our method achieves over 10% higher accuracy than existing methods, and saves over $6 \times$ power consumption.

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### TABLE II: Evaluation results of latency on MAC.

| Design | MAE | Cycles | Stalls |
|--------|-----|--------|--------|
| XNOR-OR | 1.097 | 65 | 0 |
| AND-SEP | 0.937 | 65 | 0 |
| uGEMM | 0.362 | 65 | 0 |
| AND-ACC | 0.315 | 130 | 64 |
| BSC* | 0.361 | 82 | 16 |
| Ours | 0.305 | 82 | 16 |

### TABLE III: The accuracy of 3-layers perceptron with 32 and 64 hidden neurons under FP circuit and different SC circuits.

| Design | FP | XNOR-OR | AND-SEP | uGEMM | BSC* | Ours |
|--------|----|---------|---------|-------|------|------|
| Accuracy | 96.1% | 10.0% | 21.7% | 85.1% | 93.4% | 95.4% |
| Acc.loss | - | 86.1% | 74.4% | 11.0% | 2.7% | 0.7% |

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