Reduction of Power Consumption in Norflash Memory Based Wearable Electronics with Improved LRU Algorithm

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Abstract. Norflash storage is a very important memory module for the practical application in the smart wearable electronics. For the versatility and complexity of its functional applications, it is highly demanded to build Norflash flash devices in the system. The Norflash memory devices have advantages in terms of the fast transmission speed, small volume, and good stability, when the algorithm calls the storage module to record the data and read user inquired storage data. Each startup of access in the storage module will cause a lot of power consumption. The improved Least Recently Used (LRU) algorithm is implemented to the Norflash memory device of the intelligent wearable electronics in order to reduce the power consumption in this work. The type M29F010B of ST’s chips is used for this investigation. The interface design method of the chip is analyzed in details. This approach reduces the number of accesses in the wearable electronics devices while reading from the recorded Norflash pages in the memory, comparing with the ordinary storage methods under the original operations. It shows that the improved LRU algorithm could effectively reduce the system power consumption and therefore to enhance the battery efficiency up to 8.8%.

1. Introduction

With the development of the embedded wearable products and the rise of semiconductor materials in the global market, major companies have adopted Norflash flash memory devices in succession. In smart wearable products, the algorithm will detect a certain state of the human body in walking, running, and cycling, etc., and send the movement status, such as steps, movement time and calories to the storage module for information preservation. Norflash guarantees data accuracy [1]. Because of writing and reading data frequently, there is additional power consuming in the smart wearable products. According to the related research, the storage system accounts for 40% of the total wearable device power consumption, and the predictable storage power consumption of the wearable products in the future will increase 50%, and power consumption is still one of the important indicators in smart wearable products.

Despite the continuous development of lithium battery technology, it could not meet the demands in the future smart wearable products. The current solution is to enhance the hardware design, but it does not solve the issue of power consumption fundamentally. This work aims to study the access method of the Norflash memory devices with the improved LRU algorithm to reduce system power consumption due to frequently operations about the motion data of writing and reading [2].

2. Norflash Hardware Configuration
In the smart wearable hardware design, the storage module mainly consists of the host USB, FPGA and Norflash. The Norflash chip M29F010B manufactured by the ST company is used in this work. It is a 1 Mbit non-volatile memory that can be frequently read, erased and programmed. It reads and writes data in 512-byte buffer mode according to page reads. The main device control signals of this chip are shown in Figure 1.

![Figure 1 Schematic pin layout in the Norflash M29F010B](image)

In the pin diagram, pin A represents a 1-bit address bus, which can directly access the bus read operation and control the interface to send the command[3]; DQ represents the 18-bit data bus, and outputs the address of the operation device read in the selected data bus; pin E represents the start function for activating the memory, and allowing the bus to read and write operations; pin G represents the output enable for triggering read function in the memory bus; pin W represents the write enable for controlling the memory interface; pin VCC uses to supply voltage in the operating system. Hardware architect is demonstrated in Figure 2:

![Figure 2 Connection diagram](image)

Norflash connects the pin A, W, G and E interfaces to the processor. When the system is powered on or reset, the MCU issues commands to perform the related operations. The FIFOs(First Input First Output) are configured by different endpoints to complete the instantaneous transmission between the data. DMA is a controller that connects memory and peripheral devices with DMA capabilities. The pin A as an address bus, serves as a writable control terminal for controlling the I/O port instruction FIFO(First Input First Output). For 'complete state' or 'empty state', Norflash storage uses synchronous read operation and synchronous write operation, while the smart wearable devices have more memory consumption for larger storage capacity. When the system error bit DQ5 is ‘1’, the correct data is written to memory, and the current data polling mode or data switching mode is selected[4]. If it is data polling mode, DQ7 data read to identify programming or erasing function, if the data switching mode DQ6 is used to identify whether the programming or erasure control has completed its operation. Figure 3 indicates Data polling and data switching process.
3. Software design of smart wearable storage

According to the functional requirements in the product, the smart wearable system performs modular allocation and module memory capacity allocation. The Norflash page of each module starts from 0. Different motion categories in the storage modules have different start timestamp and end time-stamp. When the page state is 0xFF, Norflash is in a writable state, and when the page state is 0X01, invalid data of the page are deleted. The smart wearable system synchronizes the internal storage data to the mobile phone APP through the Bluetooth connection. Because of the real-time motion detection in the smart wearable system, each motion detection needs to call the algorithm, and then the data is output to the Norflash, according to the user's requirements to search the data. The system calls the infrequently used data is LRU. The data type to be searched is loaded into memory. This design is based on the characteristics of LRU algorithm page replacement, through the improvement of the LRU algorithm, reducing the amount of external memory to read and the power consumed by memory.

Smart wearable devices are allocated to memory in the form of pages. When the system performs data search, only 45% of data are accessed and read collectively. This results in reading memory data frequently, increasing the power consumption of the system. According to the characteristics of the LRU algorithm, it pages different types of storage modules into modules such as S1, S2, and S3, etc., and the data is stored and searched in the form of a comprehensive module classification, which reduces the search for extra Norflash pages and increases the system access speed. The main work of the improved LRU algorithm are as follows, as presented in Figure 4.

![Figure 4 Schematic processing diagram of the improved LRU algorithm](image-url)
(1) The improved LRU algorithm divides the modules into block maintenance, to set each module in the name of A, B, C...N;
(2) It is connected by linked list, calculates the number of times of the user accesses in the storage module, and joins the access history list in accordance with certain rules;
(3) To prioritize by the number of visits in each module, if it is not the same as the original priority, then it reorder the storage module;

For different sports users, there will be frequently used and infrequently used motor function motor function, this article uses an improved LRU algorithm. To mark an access timestamp for each movement state store or query, recording the access time each time, the visit time is recorded as \{T_1, T_2, ..., T_n\}; Each time a movement type data is accessed, the number of times the number of activity in the array is self-increasing, recording the access time each times, The number of visits is denoted as \{1, 2, ..., n\}; The total visit time is recorded as:

(1) The longer the movement type, the higher the exercise priority, the shorter the time, the lower the priority. Motion storage modules are allocated through the priority of the movement. In the intelligent wearable system, a total storage allocation of movement data is recorded as M (unit is K), if the total access time is T (international unit / s), the total running time is T_1, the amount of memory stored for the running type of motion is recorded as N:

(2) To repeat the above steps, when the priority is changed, a new storage allocation; When priority doesn't change, maintaining existing storage modules; Flash storage is an unit with page, the storage volume per page is 512 bytes, The corresponding Flash storage page number:

(3) Among them 1 k is 1024 bytes; The main work of the software are as follows, as shown in Figure 5.

4. Experimental results and analyses
In summary, the advantages of applying the improved LRU algorithm to the Norflash storage are:

(1) The software program does not need to search and write the data every time as it visits the flash, only when the modular data is stored, and the data updates in the current module. Thus, it greatly reduces the number of accessing flash pages.
(2) This design greatly simplifies the logic design of the software and increases the reliability and efficiency of the system each time when the software is in writing mode [8].

(3) The improved LRU algorithm is used. It is easy to see the algorithm's time complexity and space complexity [19]. This is consistent with other existing LRU algorithms, but this part is based on the memory processing. Time consumption is negligible comparing with journaling, page transfer, and loading time [9].

In the various motion state records of the intelligent wearable system, a program to real-time detection step function. Comparison of experimental data, the power consumption of the step function is reduced to the maximum, among them, a single exercise of running and riding, when detecting that the human body is in running or riding, the current data is stored and queried. The maximum power consumption of the improved cycling single time was 0.036w, the sleep function does not need frequent the invocation of the data. Therefore, the reduced power consumption is the lowest, the improved single maximum power consumption was 0.026w.

Power consumption comparisons between the two methods are given in Figure 6:

Figure 6 (a) the power consumption comparison between two algorithms for the function of (a) stepping

Figure 6 (b) the power consumption comparison between two algorithms for the function of (a) riding

Figure 6 (c) the power consumption comparison between two algorithms for the function of (a) sleeping

Figure 6 (d) the power consumption comparison between two algorithms for the function of (a) running

To load different programs into smart wearable devices, user wears two smart wearable devices to do the same exercise. Types of the movement: walking, cycling, sleeping, running. To take one minute as the basic unit and record 30 minutes. Repeating the above experiment 10 times and recording the
average. Under the same condition, to record power consumption caused by motion, as shown in Table 1, Comparison of original storage and improved storage, in the first minute of the single movement, average power consumption drops to 4.425%. When single movement takes 30 minutes, average power consumption drops to 8.823%. For long periods of single motion, the use of improved storage type, it has the effect of significantly reduced power consumption, only for data storage and query against a motion module to reduce redundant flash page queries and time access. the record data is shown in table 1:

| Function | Origin Power/1m in mA | Improved LRU | Power Save | Origin Power/30min in mA | Improved LRU | Power Save |
|----------|-----------------------|--------------|------------|--------------------------|--------------|------------|
| Step     | 0.029                 | 0.026        | 7.79%      | 0.882                    | 0.798        | 9.48%      |
| Ride     | 0.033                 | 0.032        | 3.41%      | 1.037                    | 0.904        | 12.82%     |
| Sleep    | 0.025                 | 0.023        | 4.55%      | 1.132                    | 1.067        | 5.74%      |
| Run      | 0.034                 | 0.034        | 2.13%      | 1.079                    | 0.991        | 8.10%      |

5. Conclusions
In this article we have employed the improved LRU algorithm successfully to reduce the power consumption in wearable electronics with the Norflash memory. The origin algorithm regularly counts the number of storage visits for each module. Reasonable memory allocates the functions of walking, running, cycling and sleeping in smart wearable electronics. When the algorithm calls the storage module and the user queries data, it is only for target storage module to operation. In the case of basic functions, it has been demonstrated that the improved LRU algorithm enhances the performance of storage modules in the wearable ring devices verified experimentally in the same environment. This design reduces the number of additional flash pages and amount of access time. Comparing with the regular algorithm for the power consumption in various sports in the same time slot, the overall system power consumption decreases by nearly 8.8%. The original 24 hours of power can be extended to 28 hours. This approach reduces the power consumption of the memory module, therefore, improves the journey efficiency in the wearable devices.

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References
[1] Chang Yuanhao, Lin Jianhong, Hsieh J W, et al. A Strategy to Emulate NOR Flash with NAND Flash [J]. ACM Transactions on Storage, 2010, 6(2): 1-23.
[2] Yoo Y S, Lee H, Ryu Y, et al. Page Replacement Algorithms for NAND Flash Memory Storages[M]. Berlin, Germany: Springer, 2007.
[3] Barriga L, Ayani R. Lazy Update: An Efficient Implementation of LRU Stacks[J]. Information Processing Letters, 1995, 54(2):81-84.
[4] Servalli G, Brazzelli D, Camerlenghi E, et al. A 65 nm NOR flash technology with 0.042 ¹m2 cell size for high performance multilevel application. In: International Electron Device Meeting (IEDM), session 35-1, 2005. 869-872
[5] Tanaka H, Kido M, Yahashi K, et al. Bit cost scalable technology with punch and plug process for ultra high density flash memory. In: VLSI Symposia on Technology, 2007, 14-15
[6] Katsumata R, Kito M, Fukuzumi Y, et al. Pipe-shaped BiCS flash memory with 16 stacked layers and multi-level-cell operation for ultra high density storage devices. In: VLSI Symposia on - Technology, 2009. 136-137
[7] Hubert A, Nowak E, Tachi K, et al. A stacked SONOS technology, up to 4 levels and 6 nm crystalline nanowires with gate-all-around or independent gates (©-Flash), suitable for full 3D integration. In: International Electron Device Meeting (IEDM), 2009. 637-640

[8] Takashima D, Noguchi M, Shibata N, et al. An embedded DRAM technology for high-performance NAND flash memories. In: 2011 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC). San Francisco, CA, 2011. 536–546

[9] Yuasa S, Nagahama T, Fukushima A, et al. Giant room temperature magnetoresistance in single-crystal Fe/MgO/Fe magnetic tunnel junctions. Nat Mater, 2004, 3: 868-871

[10] Durlam M, Addie D, Akerman J, et al. A 0.18 µm 4 Mb toggling MRAM. In: International Electron Device Meeting (IEDM), session 34-6, 2003. 995-997