Research of low noise pHEMT transistors in equipment for microwave radiometry using numerical simulation

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Abstract. The numerical impact modeling of some external effects on devices based on AlGAs/InGaAs/GaAs heterostructures (pHEMT) was carried out. The mathematical model was created that allowed to predict the behavior of the drain current depending on condition changes on the heterostructure in the barrier region and to start the process of directed construction optimization of the devices based on AlGaAs/InGaAs/GaAs pHEMT with the aim of improving their noise characteristic.

1. Introduction
Amplifiers based on MMIC that are the part of microwave radiometry equipment have special requirements for noise characteristics. It should be noted that it includes not only the desire to minimize the noise of active MIC amplifying elements, in our case, heterostructured pHEMT, but also the stability of noise characteristics with the thermodynamic balance of the system “biological body - the radiometer input circuits” even in conditions of special antenna noise.

Optimization of such transistors production cycle is still a complicated and expensive procedure [1-3]. This paper presents the results of numerical simulation and calculation of the low noise features pHEMT for increasing efficiency when they are operating as a part of amplifiers for microwave radiometry equipment.

2. Simulation results
According by previous studies [4], the most important influence on the characteristics of heterostructured field-effect transistors is provided by the parameters of the gate region (thickness, composition and doping profile of individual layers, geometric dimensions and profile of the gate groove, topological dimensions and spatial location of the gate electrode). The choice of optimal parameters of the gate area was very important, for example, to obtain optimal noise characteristics at a given length of the gate electrode, providing the required level of the breakdown voltage, enhance the stability of device characteristics to possible fluctuations of technological process parameters.

The application of numerical modeling for prediction of the noise parameters of the developed transistors is very perspective task, since it allows to find out the distribution of physical fields, charges and flows of charged particles in an inhomogeneous structure that consists of different layers of semiconductor materials and dielectric layers located on the surface.
Additional calculations of the distribution dependence of local noise sources in the volume of the structure from the concentration of charges at the dielectric-semiconductor interface were performed for the most accurate prediction of the behavior of noise parameters. The developed software package was successfully applied in the work for this purpose [4].

According calculation results that are shown in figure 1 the value of the introduced charge \( q=1\times10^{12} \text{[cm}^{-2}\text{]} \) corresponds to the location of \( 1\times10^{12} \) electron charges on the cm\(^2\) of dielectric-semiconductor boundary surface.

![Figure 1](image1.png)

**Figure 1.** The image of the screen for a calculating of the local noise sources through the transistor in the state of normal depletion of the sub-gate region.

The detected dependencies allowed to offer design for a low-noise transistor, taking into account the distribution of noise sources in its cross-section. Figure 2 shows the results of numerical simulation of two variants of the top of the transistor.

![Figure 2](image2.png)

**Figure 2.** The image of the screen for a calculating of the potential distribution over the transistor cross section for two variants design options. Left – gate recess 0.8 \( \mu \text{m} \), on right - gate recess 1.6 \( \mu \text{m} \).

As shown by previous researches, the biggest influence on the characteristics of heterostructured field-effect transistors is provided by the parameters of the gate region (thickness, composition and doping...
profile of individual layers, geometric dimensions and profile of the gate groove, topological dimensions and spatial location of the gate electrode). The choice of the gate area parameters was extremely important for optimal characteristics for a given length of the gate electrode, providing the required coefficient of amplification, increasing the stability of device characteristics to possible fluctuations of process parameters.

The width of the gate groove remains an insufficiently studied parameter during developing its design, which can affect to the output characteristics of the device. In our case, we analyzed a heterostructured transistor of standard design described earlier in [6]. The developed numerical simulation procedures for the transistor showed a good agreement with the experimental data and allowed to start predicting of the noise characteristics of the device developed for microwave radiometry equipment.

Figure 3. The image of the screen. Minimum noise figure (dB) vs frequency (Hz) for two pHEMT topology. Solid line – gate recess 1.6µm, dash line – gate recess 0.8µm.

As a result of numerical analysis of the distribution of local noise sources across the cross section of this transistor it was detected a strong influence of charge states on transistor’s surface on the distribution of these sources. So we can suggest that changing the width of the sub-gate groove will affect the noise characteristics of the transistor. Figure 3 shows graphs of the dependence of the noise coefficient of the developed transistor from the frequency for two variants of its surface design. It can be seen that the design with a reduced width of the gate groove allows to reduce the noise coefficient of a heterostructured transistor, especially in the area of relatively high frequencies. So, in the area of frequency 8GHz, the noise coefficient of the transistor with a sub-gate groove width of 0.8 µm is 1.2 dB, and the noise coefficient of the transistor with a sub-gate groove width of 1.6 µm is 1.8 dB. It should be noted that the received two versions of the transistor design are competitive and do not lose to each other in the coefficient of amplification, saturation current density, uniformity of the flow characteristic (Gate-Drain) and other important output parameters. The results of the research allow us to conclude that the developed numerical modeling algorithms can be effectively used for analyzing
submicron structures of pHEMT transistors, taking into account the main physical phenomena and features of real device structures. Numerical analysis of the effect of the top part design of the transistor on noise parameters shows that the procedure of chemical etching of the gate groove should provide its required width for the developed design of the transistor heterostructure based on the AlGaAs-InGaAs-GaAs material system, as well as homogeneous etching of the gate groove with a good surface morphology.

3. Conclusion
Performed calculations of the distribution of local noise sources in the volume of the heterostructure from the concentration of charges at the dielectric-semiconductor interface show strong interconnection. The existence of an optimal charge at the heterostructure boundary for achievement of minimal noises in the device without taking into account self-heating were predicted by numerical modeling [5-7]. It is quite correct taking into account the modes of small displacements on the electrodes in the MMIC equipment for microwave radiometry.

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