A Radiation-Hardened Programmable Read Only Memory for Space Applications

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\textbf{Abstract:} A radiation-hardened 64-Kb Programmable Read Only Memory (PROM) fabricated by 0.18um commercial technology is proposed. The Radiation-Harden-By-Design (RHBD) technique is applied in the design of the PROM. At the cell level, memory cells consisting of two high reliable antifuse elements are used. At the circuit level, robust sense amplifiers are designed with Dual Interlocked Cell (DICE) latches added to the radiation sensitive nodes. Furthermore, the enclosed NMOS and guard rings are applied at the layout level. As the measurement showed, the PROM could operate at the temperature between -55 and +125°C with 55ns maximum address access time. The TID (Total Ionizing Dose) test showed that irradiation dose to 5M rad(Si) negligibly impacted standby current and access time. In the heavy ion test, no SEU (Single Event Upset) and no SEL (Single Event Latch-up) were observed up to LET (Linear Energy Transfer) of 64.4MeV·cm²/mg.

\textbf{Keywords:} PROM, radiation harden, RHBD

\textbf{Classification:} Integrated circuits

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1 Introduction
Programmable Read-Only Memory (PROM) is a kind of non-volatile memories. It has been widely applied in space fields where superior reliability is required, such as satellite communication and spacecraft electronics [1-3]. For space application, PROMs should be hardened against natural radiation in the space. Traditionally, the radiation tolerance for PROM is achieved by using specific manufacturing process, known as “Radiation Hardening by Processes” (RHBP), which has a drawback by entailing high costs. To address this issue, Radiation Hardened By Design (RHBD) techniques have been proposed [4]. The RHBD uses layout and circuit design techniques for radiation hardness and radiation-tolerant ICs can be fabricated by standard CMOS process. Then, its cost is much lower than RHBP.

Up to now, there are few reports on the application of the RHBD in PROM. To our knowledge, it might owe to the fact that highly-reliable memory elements such as fuse or antifuse in PROM are hardly fabricated by commercial process. In our previous work [5], a new antifuse structure compatible with commercial process was proposed, and the reliability of the antifuse has already been verified, which makes the application of the RHBD in PROM feasible.

This paper presents a radiation-hardened 64 Kb PROM prototype in which the independently developed antifuse cells and the RHBD technique are applied. The PROM prototype is characterized by its high performance under radiation condition. Its design and implementation are discussed in this paper.

2 Architecture design and measurement of the PROM without being radiation-hardened
The proposed PROM is an asynchronous, 8K×8 bits programmable memory device, which is featured by fully asynchronous operation and does not require external clocks. The PROM has three control inputs: CE, PE, and OE. CE is the
device enable input that controls chip selection. PE controls program operation and OE enables data output. The PROM also has thirteen address inputs A (12:0), and eight bidirectional data lines D (7:0). To program it, a high voltage (Vpp) is directly applied through the PE pin, and then switched to the bit-line (BL) to program memory cell selected by the word-line (WL). To read, eight memory cells (a word) are selected, and the sense amplifiers will detect the voltage state of the corresponding BLs. If the antifuses in the memory cell are ruptured, the BL is pulled-down to Grand. Logic ‘1’ will be detected. Otherwise, Logic ‘0’ will be detected. Then valid data will appear on data output, D (7:0) through I/O buffers.

![Architecture diagram of the PROM prototype.](image)

![Planar view of the PROM. (a) Layout. (b) Die Photograph.](image)

![Access time as a function of temperature.](image)

The PROM prototype is designed and fabricated by TSMC 0.18um process. The area is 4.2 mm×5.3 mm. The layout, real object and function test result of the PROM are shown in Fig. 2 and Fig. 3. The fabricated PROM can operate from -55 to+125 °C with 55 ns maximum address access time.
3 Radiation-hardened techniques and test results

PROMs need to be hardened against the natural radiation when they work in the space. The radiation effect mainly includes total-ionizing dose (TID) and single event effect (SEE). In order to reduce cost, the RHBD technique is applied instead of specialized radiation-hardened manufacturing processes.

The applied RHBD techniques can be divided into three levels. Firstly, at the memory cell level, the independently developed antifuse compatible with commercial technology is adopted in the memory cell. Antifuse is commonly used as memory element for highly-reliable PROMs due to its immunity to radiation. The antifuse consists of two electrodes and a thin dielectric as the insulation layer between them. To program an antifuse, a high voltage is applied between the two electrodes to break down the thin dielectric and generate a conductive filament. The virgin and the ruptured antifuse are used for storage of logic ‘0’ and ‘1’, respectively. In this work, the applied antifuse consists of an oxide-nitride (ON) dielectric layer, sandwiched between polysilicon and N-well layers (see Fig. 4(a)). The reliability of the antifuse has already been verified in our previous work [5]. The biggest challenge for antifuses is the suspect switch-off phenomenon when the ruptured antifuses are being hit by heavy ions. To solve this problem, memory cell consisting of two antifuses and two select transistors are applied (see Fig. 4(b)), which can provide double redundancy and improve the robustness.

![Fig. 4. Structure of (a) antifuse and (b) memory cell.](image_url)

![Fig. 5. Schematic of the DICE hardened sense amplifier.](image_url)
Secondly, according to [6, 7], traditional sense amplifier designed with current mirror are the most radiation-sensitive parts of antifuse PROMs, so it should be excluded. Inverter is used as the sense amplifier in this design due to its robustness. As is shown in Fig. 5, to read a memory bit, the bit-line (BL) is pulled-up weakly by the PMOS P1 (the NMOS N0 is for Vpp isolation and is always on during read cycle). If the antifuse in the memory cell is ruptured, the BL is pulled-down to Grand with the select transistors turning on. Logic ‘1’ will be read out by the inverters and then stored by the Dual Interlocked Cell (DICE). While the antifuses stay at virgin state, the BL is still pulled-up and logic ‘1’ would be read out. The DICE latch is placed behind the inverter to strengthen the robustness by providing storage redundancy to correct SEU errors [8].

Thirdly, at the layout level, edgeless gate NMOS transistors and guard rings are used. In the 0.18um process, TID primarily increases leakage currents, manifest as increased standby current in ICs. Guard rings and edgeless gates NMOS transistors (see Fig. 6) are able to effectively cut leakage paths [9-10]. Guard rings could also help mitigating single event latch-up (SEL) [11].

For TID test, three samples were fabricated and irradiated by Co-60 gamma-rays with a power supply voltage of 3.6V (the work power supply voltage is 3.3V) at room temperature. The dose rate was 83 rad (Si)/s. The inputs were asserted to read mode, and all outputs were opened during irradiation. Under these bias conditions, most gates were activated. The power supply currents and the access time of the samples were monitored during irradiation. After irradiation to dose of 5M rad(Si), the function of all samples was tested. All the samples passed the functional test after irradiation. The changes in the power supply current and the access time during irradiation are shown in Fig. 7. The current and the access time of the samples remain almost constant during irradiation up to total dose of 5M rad(Si).

Single Event Effects (SEE) tests were also conducted and the HI-13 Tandem Accelerator was utilized to generate the heavy ions. Then, two samples were exposed to heavy ion beams with a power supply voltage of 3.6V. Exposures were conducted with Br at LET (Linear Energy Transfer) 42 Mev·cm²/mg and I at LET 64.4 Mev·cm²/mg respectively.

The SEE tests were done under both static and dynamic conditions. For the static condition, the devices were statically biased with the supply currents monitored for latch-up. No latch-up was detected even though LET is up to 64.4
Mev·cm²/mg. Under the dynamic condition, SEU (Single Event Upset) test was conducted by dynamically reading out the data stored in PROM and detecting bit errors. No upset was observed up to LET of 64.4 Mev·cm²/mg. The test results are shown in Table I.

![Fig. 7. TID test result.](image)

### Table I. SEE test result

| SN | Ion | Energy (MeV) | LET (Mev·cm²/mg) | Latch-up | SEU |
|----|-----|--------------|------------------|----------|-----|
| 1# | Br  | 220          | 42               | 0        | 0   |
| 1# | I   | 260          | 64.4             | 0        | 0   |
| 2# | Br  | 220          | 42               | 0        | 0   |
| 2# | I   | 260          | 64.4             | 0        | 0   |

### 6 Conclusion

In this paper, a high-performance 64 K-bit Radiation-hardened PROM has been designed, fabricated by 0.18um commercial technology. The test results show that it can operate reliably from -55 to +125 °C under irradiation up to 5 M rad(Si) and LET up to 64.4 Mev·cm²/mg with 55 ns maximum address access time. The proposed PROM might be a good memory choice for space applications.

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