Effect of jitter on the settling time of mesochronous clock retiming circuits

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Abstract
It is well known that timing jitter can degrade the bit error rate of receivers that recover the clock from input data. However, timing jitter can also result in an indefinite increase in the settling time of clock recovery circuits, particularly in low swing mesochronous systems. Mesochronous clock retiming circuits are required in repeaterless low swing on-chip interconnects. We first discuss how timing jitter can result in a large increase in the settling time of the clock recovery circuit. Next, the circuit is modelled as a Markov chain with absorbing states. The mean time to absorption of the Markov chain, which represents the mean settling time of the circuit, is determined. The model is validated through behavioural simulations of the circuit, the results of which match well with the model predictions. We consider circuits with (1) data dependent jitter, (2) random jitter, and (3) combination of both of them. We show that a mismatch between the strengths of up and down corrections of the retiming can reduce the settling time. In particular, a 10% mismatch can reduce the mean settling time by up to 40%. We leverage this fact toward improving the settling time performance, and propose useful techniques based on biased training sequences and mismatched charge pumps. We also present a coarse+fine clock retiming circuit, which can operate in coarse first mode, to reduce the settling time substantially. These fast settling retiming circuits are verified with circuit simulations.

Keywords Settling time · Clock recovery · Metastability · Low swing interconnect · Absorbing Markov chains

1 Introduction
Timing jitter in the incoming data degrades the bit error rate (BER) of receivers that recover clock from the data itself, and this effect has been extensively studied (c.f., [1, 2]). However, it has been recently observed in [3] that, under certain conditions, timing jitter can also increase the settling time of clock retiming circuits. In this paper, we present a detailed analysis of the settling time of mesochronous clock retiming circuits in the presence of jitter.

Mesochronous clock retiming circuits are required in repeaterless low swing on-chip interconnects to sample the data correctly at the receiver [4, 5], and also in off-chip links that use a forwarded clock [6, 7]. In mesochronous receivers, a clock running at the correct frequency is available at the receiver and only the correct phase needs to be recovered. Hence, such clock retiming circuits use delay line [4, 5] or phase interpolators [8] to generate the required clock phase. Use of delay based retiming circuits is preferred over systems that use phase locked loops with a voltage controlled oscillator (VCO) per channel due to their better performance and lower complexity [9]. Delay based retiming circuits are preferred even in systems where the clock frequency is known only nominally and not exactly [8]. Fast locking clock data recovery (CDR) circuits (also known as burst mode CDRs [10]) offer very short settling times. These CDR circuits use gated VCOs [11], oversampling [10] or injection locking [12]. However, these CDR circuits have certain limitations. Gated VCOs have poor phase aligning and no input jitter.

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rejection. Oversampling CDRs come with high complexity and power consumption. Injection locked CDRs have quantization phase error and high cycle to cycle jitter. Hence, for source synchronous on-chip and chip to chip links, delay based retiming circuits are preferred. Hsieh and Sobelman in [13], provide a detailed discussion and comparison of different CDR circuit architectures.

Delay based clock retiming circuits are known to offer fast settling times as compared to PLL based synchronizers as they do not need a clock synthesis step [13]. Timing jitter can increase the settling time of such delay based clock retiming circuits indefinitely[3]. This occurs when the circuit wakes up with its clock in the horizontally closed region of the data eye. Typical systems implemented on-chip can have hundreds of long interconnects [14, 15], and a horizontal eye opening of about 85% is not pessimistic [16, 17]. If the initial clock position is assumed to be uniformly distributed, there is a 15% chance that the circuit wakes up with its initial clock phase in the closed region of the eye, making it important to study and understand this problem. To analyze the settling time, the clock retiming circuit can be modelled as a Markov chain with absorbing states [3]. Here the states correspond to the clock positions. The state transitions correspond to the phase corrections done by the clock recovery circuit. This model provides useful insights into the dynamics of the system. In particular, as shown in this work, the mean settling time of the circuit is predicted by the model.

In this paper, we investigate the settling time of mesochronous clock retiming circuits in detail. Section 2 presents a detailed discussion on the settling time of mesochronous clock retiming circuits, in particular, its dependence on timing jitter, which is the main focus of this work. We demonstrate the increase in settling time, caused due to jitter, using experiments performed on a chip and these experiments are described in Sect. 3. Next, toward analyzing different types of jitter, a Markov chain model of the mesochronous synchronizers is presented in Sect. 4. As the settling time is random, it cannot be determined exactly. However, using the Markov chain model we can determine bounds on the settling time. These are given in Sect. 5. Techniques for reducing the settling time, along with supporting circuit simulations, are given in Sect. 6. Finally, we make overall concluding remarks in Sect. 7.

2 Setting time of the clock retiming circuit

In order to analyze the settling time of a mesochronous system, we consider a repeaterless interconnect system as shown in Fig. 1. Here the delay of the interconnect is expressed as \((n + \lambda)T\), where \(n \in \mathbb{Z}^+, \lambda \in [0, 1)\) and \(T\) is the system clock period. \(\phi_{Ts}\) and \(\phi_{Rs}\) are the phases of the transmitter and receiver clocks respectively. The clock retiming circuit derives the sampling clock \(\phi_d\), which is positioned at the center of the input data eye, from the receiver clock phase. The settling time of the circuit is defined as the time it takes for the circuit to derive this sampling clock phase. This time depends on the initial phase error between the clock and the data. This initial phase error \(\Delta \phi\) is a continuous variable taking values in \([0, 2\pi)\). When the initial phase error is less than \(\pi\), the circuit achieves lock by decreasing the phase to 0. On the other hand, when \(\Delta \phi\) is greater than \(\pi\), the circuit achieves lock by increasing the phase difference to \(2\pi\), which is the same as 0 by phase wrapping (refer Fig. 2). The settling time of the clock recovery circuit depends on the gain of the system and the initial phase error. For mesochronous systems, this settling time can be expressed as

\[
t_s = \begin{cases} 
T \frac{C}{2K_{VC}K_{CP}} \Delta \phi & \text{when } \Delta \phi < \pi, \\
T \frac{C}{2K_{VC}K_{CP}} (2\pi - \Delta \phi) & \text{when } \Delta \phi > \pi.
\end{cases}
\]  

(1)

Here \(C\) is the loop filter capacitor, \(K_{VC}\) is the gain of the phase modulator, \(K_{CP}\) is the gain of the charge pump and \(z\) is the data activity factor. The expression in (1) is derived in “Appendix A”.

2.1 Lengthening of the settling time

When the initial phase difference is equal to \(\pi\), the circuit can settle at two discrete values of the phase difference: 0 or \(2\pi\) (which is same as 0 by phase wrapping), and both the solutions are acceptable. Since the initial phase difference
is a continuous variable, the above scenario represents a situation of taking a discrete decision on a continuous input. Theoretically, such decisions can take an infinite amount of time for certain initial conditions [18]. This happens when $\Delta\phi$ is exactly $\pi$ radians and the system has no reason to choose one solution over another. This is akin to metastability in flip-flops [19]. When $\Delta\phi$ is exactly $\pi$ radians, the flip-flops in the phase detector become metastable. In these conditions, the phase detector loop enters a state of indecision. However, for sustained indecision of the phase detector loop, the flip-flops in the phase detector must become metastable in every clock cycle. Practically, however, given the narrow widths of the metastability windows, the fast recovery times and the inherent jitter present in the clocks, sustained loop indecision due to flip-flop metastability is highly unlikely. Hence, metastability of the flip-flops in the phase detector is not discussed in this work.

2.2 Effect of timing jitter: the window of susceptibility

When the input data has timing jitter (due to inter-symbol-interference (ISI) in the data and/or random jitter in the clock) and the initial clock phase ($\phi_0^d$) is in the horizontally closed region of the data eye, the expression of settling time in (1) is not valid. Fig. 3 illustrates an eye diagram with timing jitter and when $\phi_0^d$ is in the horizontally closed region of the data eye. This region is called the window of susceptibility ($W$) henceforth. When the initial clock is in this window $W$, the output of the phase detector is randomized by the jitter in the data, and hence, the phase error information is lost. This increases the settling time $t_s$ indefinitely, till the system escapes this window $W$.

2.3 Working of phase detectors in the window of susceptibility

The timing diagram of the Alexander phase detector [20] is shown in Fig. 4(a). The phase detector takes 2 samples per bit period and takes a binary decision of shifting the clock to the right or to the left based on the last three samples (labelled as A, B and C in Fig. 4). When there is no jitter in the data, the phase detector consistently produces either up (UP) or down (DN) pulses. Thus, for a given data activity factor $x$, the settling time can be calculated using (1).

The phase detector’s decision to assert one of UP or DN signals depends on the value of the sample taken at time instant B. Fig. 4(b) shows the timing diagram of the Alexander phase detector when the data is corrupt with jitter [3]. Due to jitter the value of the sample at time instant B depends on the current data transition time and not on the average data arrival time. Hence, the phase detector produces UP and DN pulses randomly and the clock recovery circuit can remain stuck, with its clock in this region, indefinitely.

Linear phase detectors like the Hogge phase detector [21] behave similar to binary phase detectors in the window of susceptibility. The ideal characteristics of the
Alexander and Hogge phase detectors are shown in Fig. 5. The highlighted region shows the window $W$, and within this window the variation in the gain of the phase detector is negligible. Hence, the analysis of the system behaviour in the window $W$ is applicable to both these types of phase detectors. The width of the window ($T_W$) depends on the amount of timing jitter present in the system and the threshold of the sampling comparators. The effect of offset on $T_W$ is illustrated in Fig. 6. To understand the effect of the offset, let us consider the case when there is an offset and the initial clock position at $\phi_0^c$ as shown in Fig. 6. Here we consider the scenario when there is non-zero offset, and the initial clock position $\phi_0^c$ is outside the window of susceptibility $W$ as shown in Fig. 6. Here, for every $0 \rightarrow 1$ transition, the circuit makes a correction by shifting the clock to the left. Similarly, for every $1 \rightarrow 0$ transition, the circuit makes a correction by shifting the clock to the right. Since every $0 \rightarrow 1$ transition is followed by a $1 \rightarrow 0$ transition, the net result is that the clock remains stuck. Hence, as shown in Fig. 6, offsets can result in increasing the width of the window of susceptibility $W$. We will revisit this with the example of offset in the presence of 1-bit ISI in Sect. 4.1.1.

3 Experimental demonstration of the increase in settling time

We use the coarse+fine retiming circuit for on-chip interconnects reported in [5] for the analysis and experiments. Figure 7 shows the block diagram of this synchronizer.

In this circuit, a delay locked loop (DLL) is used to generate multiple phases of the clock. A controller picks one of the phases of the DLL and delays it to bring the output clock to the center of the eye using a voltage controlled delay line (VCDL). The controller comprises a phase detector which senses the phase difference between the clock and the data and integrates the error using a charge pump. This charge pump is called the weak charge pump. The integrated error voltage is used to control the delay of the VCDL. If the VCDL range is not sufficient to achieve lock (which is detected by the control voltage $V_c$ exceeding preset upper and lower voltage bounds $V_H$ and $V_L$), the controller automatically picks the next adjacent phase, resets the control voltage using a strong charge pump and re-attempts to lock. The process repeats till lock is achieved.

Most of the circuit blocks used in the clock retiming circuit in Fig. 7 are standard circuit elements, except for the charge pump circuit which consists of the weak and the strong charge pumps. Figure 8 shows the transistor level circuit diagram of the weak and strong charge pumps. When the control voltage is outside the bounds $V_H$ and $V_L$, the strong charge pump is activated which brings the control voltage within the bounds. During this period, when the strong charge pump is active, the weak charge pump is disabled by the transistors $M_2$ and $M_3$ as shown in Fig. 8.
We have measured the lengthening of the settling time on a prototype chip of this synchronizer. The chip has a circuit with a low swing transmitter and an interconnect which produces some ISI. Fig. 9 shows the simulated eye diagram at the receiver for a clock frequency of 2 GHz.

The chip was tested at a frequency of 2 GHz with Centellax TG1B1-A data generator [22] and Centellax TG1C1-A clock synthesizer [23]. In the clock synthesizer instrument, one of the clock outputs can be phase shifted with a resolution $2^\circ$, which is used for programming the initial phase error. Figure 10 shows the control voltage evolution when the circuit is stuck in the horizontally closed region of the eye at startup. Notice the abrupt change in the slope of the signal when the circuit escapes the window $W$, which happens after about 725 cycles in this example. When the circuit is initialized at the edge of this window, such a lengthening of settling time is not observed as shown in Fig. 11.

The lengthening of the settling time was observed with different data patterns like PRBS7, PRBS15 and PRBS31. In addition, the TG1B1-A data generator produces outputs with different Mark-to-Space ratios. The Mark-to-Space ratios can be chosen between 0.5, 0.25 and 0.125. Even with these different patterns, the increase in settling time occurs when the clock is initialized in the closed region of the data eye. Figure 12 shows the control voltage evolution when the circuit is stuck in the horizontally closed region of the eye with a data pattern with Mark-to-Space ratio of 0.125, in which case the circuit remains stuck with its clock in the window $W$ for about 1200 cycles. As expected the total settling time is higher for a lower data activity factor. It is worth noting that changing the Mark-to-Space ratio only changes the data activity factor. The minimum run length for logic 1 and logic 0 is still 1-bit. We will show in Sect. 6 that by changing the minimum run length for one of the logic levels, the settling time can be reduced considerably.

Fig. 9  Eye diagram at the receiver input along with the histogram of the zero crossing positions

Fig. 10  Measured lengthening (by about 725 cycles) of the settling time, with the clock initialized within the window $W$. The data is from a PRBS31 source with a Mark-to-Space ratio of 0.5. X-scale: 250 ns/div. Upper waveform is the reset (active low) signal

Fig. 11  Measured settling behaviour with the clock initialized at the edge of the window $W$. The data is from a PRBS31 source with a Mark-to-Space ratio of 0.5. X-scale: 250 ns/div. Upper waveform is the reset (active low) signal

Fig. 12  Measured lengthening of the settling time (about 1200 cycles), with the clock initialized within the window $W$. The data is from a PRBS31 source with a Mark-to-Space ratio of 0.125. X-scale: 1 ns/div. Upper waveform is the reset (active low) signal

Having demonstrated the problem of increased settling time, the next section will analyze the settling time of these circuits in the presence of different types of jitter.
4 Markov chain model of the clock recovery circuit

In order to analyze the settling time when the initial clock is in the window \( \mathcal{W} \), the circuit is modelled as a Markov chain with absorbing states [24]. The binary phase detector produces UP or DN pulses on every data transition, which are converted into an analog control voltage using a charge pump. The control voltage is used to delay the clock (either using a phase interpolator or a delay line). Since the input is binary, the output phase is quantized. Hence, the clock position can be discretized to the step size \( \gamma \) of the phase detector loop update. In order to keep the jitter in the recovered clock low, controllers typically use step sizes of less than 0.1% of the clock period (c.f., [5, 8, 25, 26]). The region where the input data eye is closed, i.e., the window \( \mathcal{W} \), is of particular interest. A Markov chain model of the system is constructed in which the states designate the clock positions and the phase corrections performed by the clock retiming circuit form its state transitions. The edges of the window \( \mathcal{W} \) are modelled as absorbing states.

The sources of timing jitter are data dependent jitter (ISI induced) in the data and noise induced random jitter in the clocks of the transmitter and receiver. The analysis for each type of jitter is done separately, followed by an analysis for data dependent and random jitter together. For analyzing the effect of data dependent jitter, an interconnect link with different bandwidths is considered. The interconnect is modelled as a 20 section RC network. For simulating different amounts of ISI, different values of RC time constants are chosen and the eye diagrams and timing jitter histograms for a few considered channel bandwidths are listed as cases 1 through 3 as follows:

Case 1 For benign channels the horizontal eye opening approaches 100% and the jitter histogram has a narrow distribution as shown in Fig. 13.

Case 2 As the bandwidth of the channel decreases, the jitter histogram splits and produces two distinct peaks [27]. This shows that the ISI due to the immediate previous bit is dominant (Fig. 14).

Case 3 Further reduction in the bandwidth shows that the jitter histogram splits into 4 regions as shown in Fig. 15. This shows that the ISI due to previous two bits is dominant.

Further reduction in the bandwidth of the channel results in the jitter histogram splitting to 8 peaks, 16 peaks and so on [27]. While the modeling presented in this paper can be used to analyze these scenarios, such channels are not usable due to the very high ISI present. Hence, our analysis considers ISI of 1 previous bit and 2 previous bits. For modeling effect of random jitter, the random jitter is assumed to have a Gaussian distribution [28]. Overall, the system is analyzed for the cases when the jitter is

1. induced by ISI due to 1 previous bit,
2. induced by ISI due to 2 previous bits,
3. random with a Gaussian distribution and
4. induced by random jitter and ISI due to 1 previous bit.

4.1 Markov chain model for jitter induced by 1 bit ISI

When the ISI due to the immediate previous bit is dominant, the zero crossings of the data are bunched into two narrow distributions as shown in Fig. 14. This is approximated to the data signal following one of two distinct traces. Figure 16 illustrates an eye diagram with ISI due to exactly 1 previous bit. Here \( t_i \) is the initial sampling instant of the clock, \( \gamma \) is the distance to the right edge of the window and \( V_{th} \) is the threshold of the samplers in the phase detector. \( A \) and \( B \) represent the two distinct zero crossing times of the data signal. For the eye diagram shown in Fig. 14, the size of the window \( \mathcal{W} \) is about 4% of the bit period. This means \( T_W \) is about 40\( \gamma \). Assuming that the source outputs 1 and 0 with equal probability, the bit

![Fig. 13](image1.png)
Fig. 13 Eye diagram and zero crossing histogram for a benign channel

![Fig. 14](image2.png)
Fig. 14 Eye diagram and zero crossing histogram for a channel for which the ISI due to the immediate previous bit is dominant
combinations that result in traces with zero crossing at \( A \) and \( B \), respectively, are listed in Table 1. Here \( b_0 \) is the current bit corrupt with ISI due to immediately previous bit \( b_{-1} \). A data transition occurs when \( b_0 \neq b_1 \). Table 1 lists all 3 bit combinations which cover all possible data traces.

Here \( LT \) and \( RT \) indicate that the clock is shifted to the left and to the right, respectively, by a step of size \( \tau \) while \( NA \) indicates no corrective action in that cycle. When all sequences are equally likely, the probabilities \( \Pr(\text{RT}) = 0.25 = \Pr(\text{LT}) \) and \( \Pr(\text{NA}) = 0.5 \). Note that the system escapes the window of susceptibility \( W \) when, for the first time, either \( (n_R - n_L)\tau \geq \gamma \) or \( (n_L - n_R)\tau \geq (T_W - \gamma) \). Here \( n_R \) and \( n_L \) are the total number of times the clock position has been shifted to the right and to the left, respectively, from start-up.

This system is modelled as a one dimensional Markov chain. The states of the Markov chain correspond to the positions of the sampling clock in the window \( W \). Once the clock escapes this window, the time taken to lock to the center of the eye can be calculated from (1). Thus, the edge positions of the window are modelled as absorbing states, thereby making this a Markov chain with absorbing states [24]. Figure 17 shows the state diagram of the Markov chain for this system. By knowing the state space and the transition probabilities of a Markov chain, one can calculate the mean time to absorption from any initial state [24]. The calculation of the mean time to absorption (and its variance) is presented in “Appendix B”.

The combined plots of the mean settling time for the 1 bit ISI case obtained from behavioural simulations of the circuit and its Markov chain model predictions via the mean absorption time are shown in Fig. 18. The behavioural simulations were done using a 20 section RC interconnect and a VerilogA behavioural description of the clock retiming circuit, while the model predictions were computed by solving for the mean absorption time of this Markov chain using a linear equation solver.

As one would expect, the settling time is maximum when the initial sampling phase is at the center of the window \( W \). It is worth noting that the variance of the absorption time is quite high. Figure 19 shows the standard deviation of the absorption time as predicted by the Markov chain model and as observed in the data obtained from behavioural simulations.

### 4.1.1 Modeling the effect of offset and 1-bit ISI

As was discussed in Sect. 2, offsets can increase the width of the window of susceptibility. Figure 20 illustrates an example of the effect of offset in the case when the ISI is limited to 1 previous bit. In this case, the circuit behaviour crucially depends on the clock position in the window. In particular, it differs when the clock is in \( A - A' \), \( A' - B' \) and in \( B' - B \). For instance, using a procedure similar to

| \( b_{-1} \) | \( b_0 \) | \( b_1 \) | Zero crossing time | Action |
|---|---|---|---|---|
| 0 | 0 | 0 | – | \( NA \) |
| 0 | 0 | 1 | \( B \) | \( LT \) |
| 0 | 1 | 0 | \( A \) | \( RT \) |
| 0 | 1 | 1 | – | \( NA \) |
| 1 | 0 | 0 | – | \( NA \) |
| 1 | 0 | 1 | \( A \) | \( RT \) |
| 1 | 1 | 0 | \( B \) | \( LT \) |
| 1 | 1 | 1 | – | \( NA \) |

### Table 1 Possible sequences and data traces for 1 bit ISI
the one described for analyzing 1-bit ISI, one can easily verify that the probabilities for left and right shifts are as follows.

| Window | Pr(LT) | Pr(RT) | Pr(NA) |
|--------|--------|--------|--------|
| $A - A'$ | 0.375  | 0.125  | 0.5    |
| $A' - B'$ | 0.25   | 0.25   | 0.5    |
| $B' - B$ | 0.125  | 0.375  | 0.5    |

By constructing the Markov chain with above transition probabilities, the settling time analysis can be extended to analyze the effect of any given offset in a straightforward manner.

### 4.2 Markov chain model for jitter induced by 2 bits ISI

When the ISI due to previous two bits is significant, the data transitions histogram has 4 peaks as shown in Fig. 15. This can be approximated to ISI of exactly two bits which results in 4 distinct data transition times. Figure 21 illustrates an eye diagram when ISI is limited to two bits and the four data transition times are labelled as $A$, $B$, $C$ and $D$. Thus, the window of susceptibility $\mathcal{W}$ can be divided into three sub-windows which are $\mathcal{W}_{A-B}$, $\mathcal{W}_{B-C}$ and $\mathcal{W}_{C-D}$. Unlike the 1 bit ISI case, the occurrences of the traces with zero crossing time at $A$, $B$, $C$ and $D$ are not independent of each other. Thus, the system is no longer memoryless, and hence, requires a second order Markov chain model. A second order Markov chain model is, in general, difficult to analyze. A technique to convert this second order Markov

| Window | Pr(LT) | Pr(RT) | Pr(NA) |
|--------|--------|--------|--------|
| $A - A'$ | 0.375  | 0.125  | 0.5    |
| $A' - B'$ | 0.25   | 0.25   | 0.5    |
| $B' - B$ | 0.125  | 0.375  | 0.5    |

Fig. 18 Mean absorption time as predicted from the Markov chain model and from behavioural simulations. Each data point in the behavioural simulation is an average of 100 runs

Fig. 19 Standard deviation of the absorption time as predicted from the Markov chain model and from behavioural simulations. Each data point in the behavioural simulation is an average of 100 runs

Fig. 20 Sketch of an eye diagram illustrating the effect of offset for the case when the ISI is limited to 1 previous bit

Fig. 21 Sketch of an eye diagram with ISI due to previous 2 bits, showing the four discrete data transition times

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chain to a first order Markov chain (with an enlarged state space) is described in the following. This greatly simplifies the analysis, as known results for first order Markov chains can be directly applied.

To construct the Markov chain model of the system, one needs to first consider the order of occurrences of the traces with zero crossing times at \( A, B, C \) and \( D \). Figure 22 shows the state diagram of the source data. The finite state machine (FSM) is limited to 3 bit combinations as the ISI for every bit is limited to previous two bits. The state transitions are labelled with the zero crossing locations of the data signal \( A \) through \( D \). \( X^{(i)} \), \( i = 1, 2 \), indicates a state transition without a data transition.

The second order Markov chain model for this system is shown in Fig. 23. To capture the memory of the system, six states are used for each clock position. Four of these states correspond to the previous data transition \( (T_{n−1}) \) occurring at \( A, B, C \) and \( D \). The remaining two states are i) \( X^{(1)} \) which indicates no data transition in the previous cycle, and ii) \( X^{(2)} \) which indicates no data transition in the previous two cycles.

For example, when \( T_{n−1} = A \), the source can be in either state \( S_2 \) or \( S_3 \) (refer Fig. 22) and the next cycle will either not have a data transition or have a data transition at position \( B \). When the initial clock is in the sub-window \( \mathcal{W}_{B,C} \), a data transition at \( B \) results in a clock shift to the right by \( 1\delta \). Thus, the transitions from state at \( T_{n−1} = A \) are either to state \( X^{(1)} \) at the same clock position or to state \( T_{n−1} = B \) of the next clock position to the right. Extending the analysis to the rest of the FSM in Fig. 22, the rest of the state transitions can be determined. In Fig. 23, the transitions are shown for only one clock position for brevity, in particular, for the clock positions in the sub-window \( \mathcal{W}_{B,C} \). Note that all the state transitions have a probability of 0.5 when the data source outputs 0 and 1 with equal probability.

Similar to the 1 bit ISI case, the mean time to absorption for the 2 bit ISI case was determined using the Markov chain model. Also, behavioural simulations were performed. For the eye diagram shown in Fig. 15, the window size is about 30% of the clock period. Here \( \mathcal{W}_{A-B} \sim 8\% \), \( \mathcal{W}_{B-C} \sim 15\% \), and \( \mathcal{W}_{C-D} \sim 7\% \). The mean time to absorption for each clock position was taken as the average of the mean times to absorption from each of the six states in the Markov chain that correspond to that position. For the behavioural simulations, a 20 section RC interconnect was used with a VerilogA behavioural description of the clock retiming circuit. In order to reduce the simulation time and the required sample size, a step size of \( 3.5\tau \) was used for this analysis. The combined plots of the mean time to absorption for 2 bit ISI case obtained from behavioural simulations and Markov chain model predictions are shown in Fig. 24. The behavioural simulations used an RC circuit for the interconnect, whereas the Markov chain model truncated the ISI to 2 bits. Note that the peak of the mean time to absorption, as predicted by the model, is about 1100 cycles when the step size is \( 3.5\tau \). This can be as high as 12,000 cycles when the step size is \( 1\tau \).
Thus, we can conclude that the predictions of the settling time of the clock retiming circuits by the Markov chain model have good accuracy. The Markov chain model predictions are presented for an equiprobable bit sequence as the data. As seen in Fig. 24, these predictions differ slightly from those given by the behavioural simulations, where the latter are performed for a bit sequence generated by the random number generator in VerilogA. The deviation is owing to the following: (1) the random bit sequence generated is not exactly equiprobable, (2) a finite number of simulations are used.

4.3 Markov chain model for Gaussian distributed random jitter

This section discusses the increase in the settling time due to random jitter in the clock. There are two sources of clock jitter in digital systems: inherent jitter in the clock generating oscillator and jitter introduced by the clock distribution network. The former can be modelled as a Gaussian distribution [28]. The latter, however, depends on several factors and can be random with arbitrary distribution [29]. The analysis in this section assumes that the jitter has a Gaussian distribution.

For ease of analysis, it is assumed that the receiver clock is noise free and all the jitter is in the transmitter clock. This assumption is valid as long as the channel response is constant over the spectrum of the noisy clock. The jitter histogram is assumed to be a Gaussian distribution with a standard deviation of $\sigma_{ck}$. The sampling clock position ($t_{ck}$) with respect to the mean data transition position can be represented as $m\tau$, where $m$ is an integer taking values from $-\infty$ to $\infty$. Hence, with respect to the sampling clock position, the mean of the data transition can be written as $-mt$. Unlike the analysis for ISI induced jitter where the window of susceptibility $W$ was bounded, random jitter may be unbounded, and hence, the size of the window $W$ may be arbitrarily large. For our analysis, a window size of $\pm 3\sigma$, i.e., $|mt| < 3\sigma_{ck}$, is assumed. This covers $> 99.999\%$ of the possible data transition positions.

When the clock transition is to the right of the mean data transition position ($m > 0$), the circuit shifts the clock to the right towards final lock ($m$ is incremented). However, even when $m > 0$, the random jitter in the data can cause the instantaneous data transition to occur to the right of the sampling clock position. This results in a clock shift in the wrong direction. Figure 25 shows the probability distribution of the clock transition time and the data transition position. The shaded area represents the probability that the data transition occurs to the right of the sampling clock position, when the mean of the data transition is to the left of the sampling clock transition ($m > 0$). This is the probability of a phase update in the wrong direction. This probability can be calculated as follows.

$$\Pr(\text{update is wrong}) = \int_{t_{ck}}^{\infty} \frac{e^{-\frac{(x-m\tau)^2}{2\sigma_{ck}^2}}}{\sqrt{2\pi}\sigma_{ck}} \, dx = \frac{1}{2} \text{erfc} \left( \frac{2m\tau}{\sqrt{2\sigma_{ck}}} \right),$$

where $\text{erfc}(x)$ is the standard complementary error function [24]. The probability of an update in the correct direction can then be calculated as

$$\Pr(\text{update is right}) = 1 - \Pr(\text{update is wrong}).$$

Note that these probability values will be scaled by a factor which equals the probability of transitions since the transitions occur independent of the clock jitter. For a source which outputs 1 and 0 with equal probability, the probability of transition is also $1/2$. This equation is then used to construct the probability transition matrix of the Markov chain to predict the mean time to absorption and the standard deviation of the time to absorption. As noted earlier, absorption in this case is defined as the phase difference between the mean of data position and sampling clock position being $> 3\sigma_{ck}$. Figure 26 shows the plots of...
the mean time to absorption and the standard deviation of the time to absorption with the initial clock position as estimated by the Markov chain model, when $r_{ck} = 20\, s$, i.e., standard deviation of the clock jitter is 2% of the clock period.

4.4 Modeling the effect of ISI and random jitter

The Markov chain model of the system can be easily extended to analyze the combined effect of data dependent and random jitter. An example case of jitter induced by 1 bit ISI and Gaussian distributed random jitter is shown in this section. When the jitter is solely due to 1 bit ISI, the data follows one of two distinct traces as discussed in Sect. 4.1. When random jitter is also present, the zero crossing of the data spreads around these two zero crossing positions. Since the random jitter is independent of the data, the probability distribution of the data zero crossing positions due to random jitter and due to 1 bit ISI is equal to the product of the probability distribution of the zero crossing positions due to random jitter and due to 1 bit ISI. For the purpose of analysis it is assumed that the receiver clock is jitter free and the transmitter clock has all the random jitter and the channel introduces data dependent jitter.

Figure 27 shows the distribution of the data zero crossing positions and the sampling clock position when the data signal has both random jitter and 1 bit ISI induced jitter. The window of susceptibility is now widened to $3\sigma_{ck} + W_{A-B} + 3\sigma_{ck}$.

The effect of the data jitter can be modelled as a shift in the mean of the Gaussian random jitter. Hence, for random jitter along with jitter due to 1 bit ISI, the jitter at any time can be considered to be Gaussian distributed, with a standard deviation of $\sigma_{ck}$ and mean at either $A$ or $B$. Consider an example clock position ($t_{ck}$) as shown in Fig. 27. Choosing $A$ as the reference position for calculations, the probability of a data transition occurring to the left of the clock is given by

$$ Pr(T_L) = Pr(A) \cdot \Phi\left(\frac{t_{ck} - 0}{\sigma_{ck}}\right) + Pr(B) \cdot \Phi\left(\frac{t_{ck} - W_{A-B}}{\sigma_{ck}}\right), $$

where $\Phi\left(\frac{x-\mu}{\sigma}\right)$ is the cumulative distribution function (CDF) of a general Gaussian distribution with mean $\mu$ and standard deviation $\sigma$. The probability of a data transition to the right of the clock can then be calculated as

$$ Pr(T_R) = 1 - Pr(T_N) - Pr(T_L), $$

where $Pr(T_N)$ is the probability of having no data transition in that clock cycle.

The Markov chain along with its transition probabilities was determined in this manner. Figure 28 shows the mean absorption time and the standard deviation of the absorption time obtained for data with timing jitter induced by 1 bit ISI in addition to Gaussian distributed random jitter with standard deviation of 1% of the clock period.
5 Bounds on the settling time

As the settling time is a random quantity, it is not possible to determine it exactly. However, in this section, we determine bounds on the settling time for a given value of probability of absorption, i.e., confidence level. Toward this we leverage the fact that the settling time of the circuit is maximum when the initial clock is at the center of the window of susceptibility (for a system without any programmed bias). In particular, the bound on the mean settling time will equal this maximum value of settling time.

Let \( l(0) \) be the row vector corresponding to the initial probability mass function on the states of the Markov chain. Here \( l(0) \) contains exactly one entry with value 1 which corresponds to the initial clock position (at the center of the window \( W \)), while the entries corresponding to the rest of positions are zeroes. Let the probability transition matrix of this Markov chain be denoted by \( P \). Using standard results for Markov chains [24], we know that given \( l(0) \), the probability mass function on the states of the Markov chain after \( n \) transitions is given by 

\[
\mu(n) = l(0) \cdot P^n.
\]

For a Markov chain with absorbing states, the probability of absorption after \( n \) transitions equals the sum of those entries of \( \mu(n) \) that correspond to the absorbing states. Hence, one can iteratively find the number of transitions required for absorption to occur for a given absorption confidence level (i.e., probability of absorption).

For illustrative purposes, we present results for a 1 bit ISI case with a window of susceptibility of size 40 steps. From the procedure described earlier to obtain a bound on the settling time, we now calculate the probability of absorption of the Markov chain as a function of the number of transitions. The results obtained are shown in Fig. 29. In fact, this plot corresponds to the cumulative distribution function of the absorption time. Hence, it directly follows that the probability of absorption in exactly \( n \) cycles corresponds to the slope of the above graph. This is shown in Fig. 30. Observe that the distribution of probability of absorption is skewed as one would expect. The probability of absorption is zero for \( n \) less than the distance to the nearest absorbing state. Also, for very large values of \( n \) this probability approaches zero.

As seen from Fig. 29, for absorption with \( > 99\% \) surety, the Markov chain needs about 3000 state transitions. This number depends on the gain of the system and increasing the gain reduces the window size (in terms of number of phase steps), and hence, the settling time. An analysis of the number of transitions needed for absorption with \( > 99\% \) confidence with the size of the window, in terms of number of steps, was done. Figure 31 shows the plot obtained from this analysis.

6 Techniques for reducing the settling time

6.1 The coarse first synchronizer

The settling time of the circuit depends on the loop gain or the step size of the phase correction circuit. A large step size will mean that the size of the window of susceptibility (in term of number of steps) is small. This results in quick settling, as was discussed in the previous section. However, a large step size results in high jitter in the clock after lock is achieved. The synchronizer proposed in [5] uses a coarse and a fine correction loop for accurate synchronization. The circuit designed there first tries to achieve lock using the
fine tuning loop. If lock cannot be achieved in the limited range of the fine tuning loop, a coarse correction is initiated. If the fine tuning loop is disabled during the initial settling period, it enables us to have a much larger step size, and hence, a much faster settling. For instance, when a 10 phase DLL is used, and even if a horizontal eye opening of 50% is available, the size of $W$ is only 5 steps.

Figure 32 shows the charge pump circuit for the synchronizer in Fig. 7, appropriately modified to have a coarse only mode. Here, during the initial period after startup, a switch disconnects the loop filter capacitor and another set of switches convert the charge pump to a combinational circuit [30], i.e., connecting the gate of the PMOS current source to GND and gate of the NMOS current sink to VDD. This converts the current sources in the fine charge pump to ON switches. This essentially increases the current injected at every fine correction step, and the control voltage overshoots the bounds set by $V_H$ and $V_L$ in every cycle. Hence, the circuit takes a coarse correction step at every cycle of the divided clock. This is equivalent to disabling the fine tuning loop and ensuring a coarse tuning step in every cycle of the divided clock that drives the coarse tuning loop. After lock is achieved, the loop filter capacitor is connected back to the charge pump, and the gates of the PMOS current source and NMOS current sink are connected to $V_{bp}$ and $V_{bn}$ respectively, to resume normal operation.

The amount of time for which the coarse tuning loop should be run before enabling the fine tuning loop depends on the size of $W$ and on the desired confidence level for achieving lock within this period. In this example given in Fig. 7, the coarse synchronizer used a 10 phase (DLL). Assuming an extreme condition that the horizontal eye opening is only 50%, it means that the window size is 5 steps. From the analysis presented in the previous section, an absorption with > 99% confidence level needs 32 cycles to be absorbed. This corresponds to 256 ns in absolute time if the coarse controller operates on a divide by 16 clock for a 2 GHz system clock.

The coarse first synchronizer was designed and simulated for a benign channel. The receiver input eye diagram for this test is shown in Fig. 33. For an initial clock phase at the center of $W$, the settling behaviour is shown in Fig. 34. As seen, the circuit escapes the window $W$ very fast and settles accurately once the fine tuning loop is enabled. The lower waveform is the select signal for switching from coarse mode to normal mode, which is run for 160 ns in coarse mode. This signal can be generated using a power on reset circuit.

This same synchronizer circuit was simulated with an input that had very high ISI. The receiver input eye diagram for this test is shown in Fig. 35. With such data input, the settling of the synchronizer is shown in Fig. 36. The clock was initialized to the center of the window $W$. Even...
for this input, the circuit escapes the window $\mathcal{W}$ within the coarse first operating period. The noise in the control voltage is primarily due to the high jitter in the incoming data.

### 6.2 Synchronizer with a bias towards one of the absorbing states

Reduction of settling time using the coarse first technique is specific to the coarse+fine type synchronizer in [5]. A different, though more general, technique of reducing the settling time is by introducing a mismatch in the relative strengths of the UP and DN updates in every cycle. Using the 1 bit ISI model for the purpose of illustration, we next discuss the settling time of this synchronizer.

Figure 37 shows the mean time to absorption as a function of initial sampling phase when the step sizes for the left and the right shifts are (1) equal, and (2) mismatched by 10%. The standard deviation for these cases is given in Fig. 38.

Note that a 10% mismatch in the step size of the left/ right shift reduces the mean absorption time by up to 40%. The effect of this mismatch is more pronounced in the standard deviation of the absorption time as a small mismatch is shown to result in a large reduction in the standard deviation as shown in Fig. 38. Hence to reduce the settling time of the circuit, one can deliberately introduce a mismatch in the UP/DN strengths of the charge pump in the circuit. Alternately, a training sequence can also induce a similar mismatch, by producing different amounts of ISI to the two logic levels 0 and 1. This inherently introduces a bias towards one side of the window $\mathcal{W}$ and reduces the settling time.

Fig. 34 Settling of the coarse first synchronizer with input having jitter from a benign channel. The lower waveform is the control signal for enabling the coarse mode.

Fig. 35 Receiver input eye diagram for a channel with high ISI.

Fig. 36 Settling of the coarse first synchronizer when the input signal has high ISI with only 50% horizontal eye opening. The lower waveform is the control signal for enabling the fine correction.

Fig. 37 Mean absorption time for a symmetric Markov chain and for a chain with a 10% bias to right shift.
6.2.1 Reduction in settling time with charge pump mismatch

Figure 39 shows the reduction in the settling time of the circuit with the introduction of a 10% mismatch in the UP and the DN currents of the charge pump. Under identical initial conditions, a simulation with 10% mismatch showed > 80% reduction in the time taken to exit the window \( W \).

Charge pump mismatch, however, can result in increased jitter once the circuit has locked. Simulations of the coarse-fine retiming circuit show that a 10% mismatch in the values of the UP and DN currents increases the peak-to-peak jitter of the recovered clock from 2.04 to 2.27 ps, which is approximately a 10% increase in the jitter. This is still only about 0.6% of the clock period of 400 ps which was used in this simulation. If such a performance degradation is not acceptable, the introduced mismatch can be switched off after lock has been achieved.

6.2.2 Reduction in settling time with training sequence

A training sequence that biases the system to either one of the directions can be used to reduce the settling time. For instance, one such training sequence is “...0010011100100111...”. This sequence has a minimum run length of 1 bit for a logic ‘1’ and 2 bits for logic ‘0’. Hence the ISI for logic ‘1’ is always more than that for logic ‘0’ and the phase detector’s output in the window \( W \) is biased towards the left. For instance, assuming the ISI is limited to 1 previous bit, we can use Table 1 to compute the probabilities of a corrective action to the left and to the right respectively. In the above bit pattern, we have the following 3 bit sequences: (a) “001”, (b) “010”, (c) “100”, (d) “001” (e) “011”, (f) “111”, (g) “110”, (h) “100”, which then repeat. Hence, referring to Table 1, we see that \( \Pr(NA) = 0.5 \), \( Pr(LT) = 3/8 \) and \( Pr(RT) = 1/8 \). Hence, this sequence implements a 25% bias to the left.

Figure 40 shows the control voltage as the circuit settles when (a) the above training sequence “...0010011100100111...” is used, and (b) a random equiprobable binary sequence is used. Notice the considerable reduction in the settling time when the deliberately biased training sequence is used. One could also use an alternating 1 and 0 training sequence which reduces the jitter due to ISI to zero. However, random uncorrelated jitter between the transmitter and receiver clocks may still result in a non-zero size of the window \( W \).

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**Fig. 38** Standard deviation of the for a symmetric Markov chain and for a chain with a 10% bias to right shift

**Fig. 39** Control voltage of the clock recovery circuit when \( \Delta \phi \sim \pi \) radians, showing the quick escape from the window \( W \) when the charge pump (CP) has a mismatch in the UP and DN currents

**Fig. 40** Control voltage of the clock recovery circuit when \( \Delta \phi \sim \pi \) radians, showing the quick escape from the window \( W \) when a biased training sequence is used
7 Conclusions

The effect of jitter on the settling time of mesochronous clock retiming circuits is discussed in detail. In particular, it is shown how ISI induced jitter and random jitter can increase the settling time of clock recovery circuits indefinitely. A model of the system as a Markov chain with absorbing states is developed. Using this model, the effect of different types of jitter is analyzed. The model predictions of the settling time in terms of the mean absorption time of the Markov chain match well with behavioural simulations. Using insights gained from the model, techniques for reducing the settling time are reported. A coarse first synchronizer that uses only coarse correction steps initially is proposed. This architecture achieves small settling times in the presence of substantial ISI. Another technique of reducing the settling time, by introducing a mismatch between the phase updates in either direction of the clock retiming circuit, is also discussed. This is applicable to phase interpolator based clock retiming circuits as well. This mismatch is achieved either by introducing a mismatch in the charge pump or through biased training data. All the suggested fast settling synchronizers are verified with circuit simulations.

Appendices

Appendix A: Derivation of the deterministic component of the settling time

For mesochronous systems, a clock running at the correct frequency is available and only the phase has to be corrected. Hence, the clock recovery circuit can be of the first order, i.e., the loop filter is a single capacitor \([5, 8]\). When a bang-bang phase detector is used, the capacitor voltage \((V_c)\) is quantized to a step size given by

\[
\delta V_c = \frac{\int_0^T I_{CP} \, dt}{C} = \frac{K_{CP}}{C}. \tag{51x302}
\]

Here \(K_{CP}\) is the gain of the charge pump, expressed in terms of the charge pump current \(I_{CP}\) and the clock period \(T\). Hence, the step size of the phase corrections is

\[
\delta \varphi = \delta V_c K_{VC} = \frac{K_{CP} K_{VC}}{C}. \tag{51x314}
\]

The number of phase correction steps \((M)\) needed for achieving lock can be written as

\[
M = \begin{cases} \frac{\Delta \phi}{\delta \varphi} & \text{when } \Delta \phi < \pi, \\ 2\pi - \frac{\Delta \phi}{\delta \varphi} & \text{when } \Delta \phi > \pi. \end{cases} \tag{51x326}
\]

The settling time can then be written as

\[
t_s = \frac{MT}{\alpha}, \tag{51x339}
\]

where \(\alpha\) is the data activity factor. From (2), (3) and (4), the settling time expression in (1) follows.

Appendix B: Mean time to absorption of a Markov chain

Knowing the probability transition matrix of a Markov chain, the mean time to absorption and its variance can be computed. We will outline an example computation in this “Appendix”. The state diagram of the Markov chain representation of the clock recovery circuit, for data with 1 bit ISI, is shown in Fig. 17. The states corresponding to \(-T_W/2\) and \(T_W/2\), which are at the edges of the window of susceptibility, are absorbing states. The probability transition matrix \(\tilde{P}\) for this Markov chain can be written as

\[
\tilde{P} = \begin{bmatrix}
1 & 0 & 0 & 0 & \cdots & 0 \\
1 & 1 & 1 & 0 & \cdots & 0 \\
\frac{1}{4} & \frac{1}{2} & \frac{1}{4} & 0 & \cdots & 0 \\
0 & 1 & 1 & \frac{1}{4} & \frac{1}{2} & \frac{1}{4} \\
\cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\
0 & \cdots & 0 & \frac{1}{4} & \frac{1}{2} & \frac{1}{4} \\
0 & \cdots & 0 & 0 & 0 & 1 \\
\end{bmatrix}.
\]

To calculate the mean time to absorption (and the variance of the time to absorption), \(P\) is first written in the canonical form [24]. This is obtained by reordering the entries in \(\tilde{P}\) to separately aggregate all the transient and absorbing states respectively. Hence, \(\tilde{P}\) can be written as

\[
\tilde{P} = \begin{bmatrix}
\mathbf{Q} & \mathbf{R} \\
\mathbf{0} & \mathbf{I} \\
\end{bmatrix}
\]

\[
= \begin{bmatrix}
\frac{1}{2} & \frac{1}{2} & 0 & 0 & \cdots & 0 & \frac{1}{2} & 0 \\
\frac{1}{2} & \frac{1}{2} & 0 & 0 & \cdots & 0 & 0 & 0 \\
\cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\
0 & \cdots & 0 & \frac{1}{2} & 0 & \frac{1}{2} & 0 & \frac{1}{2} \\
0 & \cdots & 0 & 0 & 1 & 0 & 0 & 0 \\
0 & \cdots & 0 & 0 & 0 & 1 & 0 & 0 \\
\end{bmatrix}
\]
Here $Q$ is a square matrix which captures the transitions from one transient state to another transient state, $R$ captures the transitions from transient states to absorbing states and $I$ is an identity matrix. The fundamental matrix $N$ can be computed using the equation

$$N = (I - Q)^{-1},$$

where $I$ is an identity matrix of the same dimensions as $Q$. Conditioned on the starting position, the mean time to absorption ($T_{\text{mean}}$), in terms of the number of steps, is given by

$$T_{\text{mean}} = NC^1,$$

where $C^1$ is a column vector with number of rows equal to the number of transient states, and with all entries as 1. The variance of the time to absorption (in terms of number of steps), conditioned on the starting position, is calculated as

$$T_{\text{var}} = (2N - I) \cdot T_{\text{mean}} - T_{\text{mean}}^2.$$

Here $T_{\text{mean}}^2$ is obtained by squaring the elements of $T_{\text{mean}}$.

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