Design of a low noise amplifier for L-band GPS applications

Mohammed J Alali¹, Ahmed S Tukkee², Mahmood K Zarkani³
¹Department of electrical and electronic engineering, University of Kerbala, 56001, Karbala, Iraq
²Department of petroleum engineering, University of Kerbala, 56001, Karbala, Iraq
³Department of biomedical engineering, University of Kerbala, 56001, Karbala, Iraq

Abstract: The low noise amplifier (LNA) is a key part of any receiving system to prevent signal degradation due to different types of noise and the need for long transmission. This paper describes the procedures to design an LNA using a commercial SiGe hetero-junction bipolar transistor (HBT), BFP640, from Infineon Technologies. The amplifier, which satisfies certain specifications, may then be used to strengthen the L2C second civilian GPS signal. The design process was carried out using a powerful microwave CAD package, Advanced Design System (ADS), by Keysight Technologies, which provides a complete RF circuit design facility. The LNA was designed to meet the desired specifications of a low noise figure less than 1 dB, power gain of greater than 20 dB, and output voltage standing ratio (VSWR) of less than 2. The centre frequency used was 1.227 GHz, with an operating bandwidth of 40 MHz. This work thus presents a prototype model that can be readily implemented based on the calculated components of matching networks, as the simulation results demonstrate that the amplifier circuit satisfies the desired requirements.

1. Introduction

The low noise amplifier (LNA) is an essential component in the receiving end of most communication systems [1], [2]. The design of an LNA includes trade-offs to achieve high power gain, a minimum noise figure, and low input/output VSWR, and this involves synthesising the necessary matching networks to set the minimum possible noise figure, maximum gain, proper impedance transformation, stability, and other performance factors correctly. These can be expressed either in terms of the two-port S-parameters of the RF device or the component values of an equivalent circuit model. Common applications of the LNA include increasing the received signal power without contributing any further noise [3-5]. In [2], a broadband LNA was proposed with power gain of 25 dB for operation in the 3 to 7 GHz frequency band. In [6], two transistors were used in a cascode structure to design an LNA based on their mutual effects on each other. In this paper, a low noise amplifier with 20 dB power gain, a noise figure of less than unity, and an output return loss of less than -10 dB at an operating frequency of 1.227 GHz is presented, with all the associated design calculations.

A typical amplifier block diagram is presented in Figure 1 below. The design process starts with the selection of a suitable RF low-noise device for the desired specifications. A stabilised bias circuit can thereafter be designed to keep the Q-point of the transistor constant against variations in temperature and the device internal parameters. The input matching circuit is then synthesised to present the optimum source reflection coefficient, Γ_s, in order to achieve the desired low noise figure at the input port of the active device. The output matching circuit is then designed to maximise the power gain by minimising the output VSWR by utilising the concept of conjugate matching [7]. The matching networks should then be properly isolated from the DC bias circuit by means of the addition of appropriate blocking capacitors and RF chokes to avoid oscillation or unstable operation.
2. Design of the Biasing Circuit
Investigating the data sheet for the ultra-low-noise RF transistor BFP640 with the SOT343 package [8] shows that the value of power gain is about 20 dB at a collector current, $I_C$, of 5 mA, with a typical noise figure of about 0.65 dB. The third order intercept point (IP3) also occurs around this value of collector current. The power gain has no significant impact on the increase in $I_C$, though to avoid overheating, the value of current is relatively small. The collector-to-emitter voltage, $V_{CE}$, is set to 2V to avoid driving the HBT into the breakdown region. Accordingly, the corresponding values of base current and base voltage are evaluated after locating the $Q$-point of transistor characteristics such that $I_B = 20\mu A$ and $V_{BE} = 0.776\, V$, respectively, as shown in Figure 2 below. These characteristics are obtained by using DC and simulating the schematic in ADS using the SPICE transistor model. The collector supply voltage $V_{CC}$ is selected as 2.5V, mimicking low power consumption inside portable devices yet slightly higher than $V_{CE}$. Several calculations are then performed to determine the resistors constituting the biasing circuit, as presented in Figure 3.

![Figure 3](image.png)

**Figure 3:** The collector feedback bias circuit is used in this design is presented in Figure 3, which shows the currents flowing in the resistors and the transistor.
Figure 3: The DC bias circuit of the amplifier.

The DC current flowing in the voltage-divider base resistor, $R_{B2}$, is usually 10 times larger than $I_B$ [7]. Therefore, the resistor values are calculated from the following relationships:

$$R_{B2} = \frac{V_{BE}}{10I_B} \quad (1)$$

$$R_{B1} = \frac{V_{CC} - V_{BE}}{11I_B} \quad (2)$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C + 11I_B} \quad (3)$$

Substituting $V_{CE} = 2V$, $V_{BE} = 0.776V$, $I_C = 5$ mA, and $I_B = 20$ µA gives $R_{B1} = 7.83$ kΩ, $R_{B2} = 3.88$ kΩ, and $R_C = 95.78$ Ω. These resistances are connected using real values imported from the ADS library such that $R_{B1} = 8.2$ kΩ, $R_{B2} = 3.9$ kΩ, and $R_C = 100$ Ω. Appropriate DC blocking capacitors of 100 pF with an RF choke of 100 nH are added to provide the required isolation between the DC and RF signals at 1.227 GHz.

3. Synthesis of the Matching Networks

The input and output matching networks are responsible for achieving optimum impedance transformation while ensuring low noise figures and stable operation [9], [10]. However, the optimum source reflection coefficient values required for both conjugate matching and minimum noise contribution rarely lie close to each other on the Smith chart. Furthermore, most microwave transistors are potentially unstable at frequencies beyond 1 GHz, and therefore the source and load reflection coefficients must be selected from outside the stability circles on the Smith chart.

A small signal transistor model, characterised by its measured $S$-parameters is first simulated across the desired band to test its stability factor, minimum noise figure, maximum stable gain, and other necessary performance parameters. Figure 4 presents the minimum noise figure, $NF_{min}$, and the stability factor across the frequency band from 1.1 GHz to 1.3 GHz. The plot shows that the stability factor, $K$, is less than 1 which implies that the transistor is potentially unstable at the specified frequency range. However, the minimum noise figure that can be achieved is seen to be around 0.62 dB, offering superior noise performance.
As the transistor is potentially unstable, conjugate matching at the input and output ports cannot be fully realised, and some gain mismatch must be tolerated to sustain stable operation. The maximum stable gain, MSG, and the forward transmission coefficient, $S_{21}$, are sketched together in Figure 5. This plot shows the roll-off in power gain with the increase of frequency due to the effect of the internal parasitic capacitances of the RF transistor that shunt its output port.

The input and output reflection coefficients are further sketched on the Smith chart in Figure 6 across the frequency band of concern. It is clear that these coefficients are relatively far away from the centre of the chart, suggesting that careful matching is required.
Figure 6: Input and output reflection coefficients of the RF transistor.

The design procedure of matching networks begins by selecting the appropriate source and load reflection coefficients to produce the desired noise figure and power gain while simultaneously ensuring stable operation. For this purpose, the source stability circle was sketched at the centre frequency 1.227 GHz on the Smith chart to exclude the unstable region. The noise circles and available gain ($G_A$) circles were plotted on the same chart to develop a compromise between power gain and noise figure when selecting the source reflection coefficient, $\Gamma_s$. These circles are displayed in Figure 7.
Figure 7: Stability, noise, and available gain circles at 1.227 GHz.

The optimum source impedance, $Z_{\text{opt}}$, for minimum noise figure, $NF_{\text{min}}$, lies at the centre of the noise circles and is equal to $86.2 + j36.35 \, \Omega$. However, the corresponding calculated load reflection coefficient, $\Gamma_L$, lies inside the output stability circle, which causes unstable operation in the circuit. Therefore, a trade-off is made by selecting $\Gamma_s$ at the intersection point between the $NF = 0.72 \, \text{dB}$ noise circle and the $G_A = 21.7 \, \text{dB}$ available gain circle, as depicted in Figure 7. In this case, $\Gamma_s = 0.364 - j0.1$ and $Z_s = 103.45 - j24.35 \, \Omega$. The equivalent value of the output reflection coefficient is thus evaluated from

$$\Gamma_{\text{out}} = S_{22} + \frac{S_{12}S_2\Gamma_s}{1-S_{11}\Gamma_s} \quad (4)$$

The load reflection coefficient is the complex conjugate of the output reflection coefficient to achieve minimum output VSWR; hence, $\Gamma_L = \Gamma_{\text{out}}^*$. In this case, $\Gamma_L = 0.1924 + j0.0233$ and $Z_L = 73.72 + j3.57 \, \Omega$. The calculated load reflection coefficient therefore lies outside the load stability circle, as shown in Figure 8.

Figure 8: Location of the load reflection coefficient with respect to the load stability circle.

Based on pre-calculation of $Z_s$ and $Z_L$, the input and output matching circuits were synthesized analytically using the Smith chart tool of the ADS simulator. Single L-section networks with parallel inductor and series capacitor were selected in this design for simplicity and compact structure. Figure 9 presents the AC schematic of the low noise amplifier showing the calculated values of the components in the input and output matching networks. Although, lumped components were used in the construction of the matching circuits in this case, transmission lines could also be utilised to reduce the parasitic elements associated with the realistic capacitors and inductors in this frequency. However, a high quality and low-loss dielectric substrate was needed in this case to implement the distributed elements as microstrip lines.
4. Simulation of the amplifier circuit
The amplifier circuit was thereafter defined in the microwave computer program ADS in order to test and optimise its performance at the specified frequency range. The component values of the matching networks were optimised for better response and then tuned for practical purposes. The final amplifier circuit, including the DC bias circuit, is presented schematically in Figure 10.

As shown from this schematic, all component values were equated to standardised ones in order to simplify the implementation process. The DC blocking and bypass capacitors may be of SMD or chip type to reduce parasitic effects. In addition to DC signal blocking, these are useful in terms of shunting the spurious noise signals to ground and thereby improving circuit stability [12]. The RF choke and matching inductors can either be wound on air cores with suitable size AWG enamelled wire or be implemented as standard chip inductors. Capacitors $C_1$ and $C_2$ of the matching circuits should be trimmer capacitors for tuning purposes to enable more practical adjustment of the circuit response.

The simulated noise figure and power gain of the amplifier are displayed in Figure 11 across a frequency range from 1.1 GHz to 1.3 GHz. The noise figure is about 0.64 dB at 1.227 GHz, but remains lower than 0.66 dB across the entire band. On the other hand, the power gain is 20.7 dB at 1.227 GHz with values greater than 20 dB in the full swept frequency range.
In Figure 12, the input and output VSWR are sketched against frequency. The output VSWR is equal to 1.7 at the nominated frequency of operation, while the input VSWR is relatively high, exceeding 10 at 1.227 GHz. The improvement in noise figure is thus achieved only at the expense of the degradation in the input VSWR. In addition, the fact that the device is potentially unstable at the operating frequency has compressed the available region for source impedance selection to avoid oscillation and instability. However, the latter problem can be solved by inserting a 50 Ω RF isolator (or circulator) at the input of the LNA to prevent any reflected power moving back into the receiving antenna. An alternative measure to improve the quality of matching is to balance input and output return losses, as depicted in Figure 13.
5. Conclusion
In this paper, a low noise amplifier was designed and simulated to operate at a GPS frequency of 1.227 GHz using an ultra-low noise hetero-junction bipolar transistor (HBT). This showed that a compromise between the noise figure, VSWR, and power gain was necessary in this design process. The simulation results further indicated, however, that the selected HBT device offers superior noise and gain performances at the frequency band of interest, and that the structure of the designed amplifier is very compact, allowing it to be implemented in both discrete and hybrid microwave integrated circuits.

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