Advanced field-effect transistors (FETs) with non-trivial gates (e.g., offset-gates, mid-gates, split-gates, or multi-gates) or hybrid integrations (e.g., with diodes, photodetectors, or field-emitters) have been extensively developed in pursuit for the “More-than-Moore” demand. But understanding their conduction mechanisms and predicting current–voltage relations is rather difficult due to countless combinations of materials and device factors. Here, it is shown that they could be understood within the same physical picture, i.e., charge transport from gated to nongated semiconductors. One proposes an indicator based on material and device factors for characterizing the transport and derives a unified and simplified solution for describing the current–voltage relations, current saturation, channel potentials, and drift field. It is verified by simulations and experiments of different types of devices with varied materials and device factors, employing organic, oxide, nanomaterial semiconductors in transistors or hybrid integrations. The concise and unified solution provides general rules for quick understanding and designing of these complex, innovative devices.

1. Introduction

Field-effect transistors (FETs) or thin-film transistors (TFTs) with non-trivial gate structures have been explored for superior functions in cutting-edge research, including the offset-gate structure, mid-gate structure, split-gate structure, light-emitting transistors, or other multigate or partial-gate structures. A significant feature is that gated and nongated semiconductor channels are coupled together. Such coupled channels are also critical to integrate sensing, memory, computing, or illumination by integrating transistors with photodiodes (PDs), light-emitting diodes (LEDs), field emitters, sensors, and etc. Some of them are illustrated in Figure 1a, which are made with a broad range of new semiconductors including organic small molecules or polymers, metal oxide, low dimensional semiconductors, perovskites, and etc. However, the countless possibilities of material combination and interface make it difficult to understand the relationship between material and device parameters and device characteristics. So far, these devices have been comprehended or explained case by case in experiments only through complex and special models and nonuniversal numerical simulation. Therefore, a concise physical picture and a general framework for understanding such new devices or predicting their characteristics are still blank.

A general physical framework would answer both fundamental and practical questions: Why and what material or device factors will affect the charge transport and current conduction mechanisms? How do these factors determine the current–voltage relations and the current saturation? How is the electric potential and field distributed in the channels? How to design the device structures? The framework should also be as concise and universal as possible, so that it can be applied to devices and semiconductors with various particularities. The target of this study is to understand the mechanisms and predict the performance of those new devices made of various materials.

Here, we focus on the key physical process, i.e., charge carriers drift from the gated-channel into a nongated channel (Figure 1b). First, we derive a basic theory framework with simple and universal equations for describing how charge transport occurs, how current–voltage relations behave, and how the electric potential and field evolve. Then, we verify the theory framework by simulating an offset-gate transistor as an example. Finally, we apply it to examine different experimental devices and briefly discuss
2. The Physical Picture

From Gauss law and continuity principle, the current on the boundary between the gated and nongated semiconductor is continuous (Figure 1b, the gray boundary). In gated semiconductors, the electric resistance \( R \) is related to the drain current \( I_D \) by using the gradual channel approximation\(^{[13]} \):

\[
\frac{dV}{dR} = \frac{I_D}{dV} = \frac{I_D}{dx} \frac{1}{W \mu C_i (V_G - V_{th} - V(x))}.
\]

Here, \( W \) is the channel width, \( C_i \) is the capacitance per unit area for the insulating dielectric layer, \( V_G \) is the gate voltage, \( V_{th} \) is the threshold voltage, and \( V(x) \) is the local potential. Denote \( V_S \) as the source potential as transistors with organic or low-dimensional semiconductors usually have injection barriers, unlike silicon MOSFETs. Denote \( V_1 \) as the potential at the end \( (|V_S| < |V_1| < |V_G - V_{th}|) \) and \( L \) as the gated channel length. Integrate \( dV \) from \( V_S \) to \( V_1 \) and \( dx \) from 0 to \( L \) and we have the \( I-V \) relation above the threshold:

\[
I_D = \frac{W}{L} C_i \mu \left( V_G - V_{th} - \frac{V_1 + V_S}{2} \right) (V_1 - V_S).
\]

Here, \( V_1 \) would not exceed the saturation voltage \( V_{DSAT} \) which is usually above \( V_{DSAT} = V_G - V_{th} \) of conventional MOSFETs due to the transport in the various non-gated semiconductors as discussed below.

In nongated semiconductors, the conduction mechanisms include: a) Fowler–Nordheim (F–N) tunneling via quantum mechanical tunneling or Poole–Frenkel (P–F) emission that occurs with rich structural defects\(^{[14,15]} \); b) Ohmic current or space charge limited current (SCLC) achieved by band-conduction or thermally activated transport among localized states (e.g., at grain boundaries)\(^{[16]} \); c) ballistic transport without scattering (e.g., in nanotubes)\(^{[17]} \). Among them, Ohmic current and SCLC are mainly dominant at high current density in various semiconductors\(^{[18,19]} \). At the beginning of the non-gated channel, the current density \( J \) depends on the local carrier density \( n \) and drift electric field \( \epsilon \):

\[
J = \left( n_0 + n_{sp} \right) q \mu \epsilon = \left( 1 + \eta \right) n_0 q \mu \epsilon
\]

The subscript “0” and “Sp” refer to the free carriers at thermal equilibrium and the rest carriers forming space charge regions, respectively; \( q \) is the elementary charge; \( \eta \) is the space-charge-to-equilibrium-carrier ratio; \( \eta = n_{sp}/n_0 \) (Figure 1b). The \( n_{sp} \) responsible for forming space charge regions will increase when increasing the dielectric relaxation time \( \tau_R \) within which carriers are relaxed toward a uniform distribution, decreasing the carrier transit time \( \tau_T \) within which carriers are swept out, or increasing

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Figure 1. From devices to transport in materials. a) Transistors and integration containing coupled channels. The lateral structures are on the first row and the vertical structures are in the lower row. b) The key physical process, i.e., charges from gated to non-gated semiconductors. Potentials, current, length, and thickness parameters are marked. c) Transport mechanisms in materials. The single-linear rows and double-linear rows indicate the transport in the gated and nongated semiconductors, respectively. In (c), the yellow and grey dots represent the movable and trapped carriers, respectively, and the number of them illustrates the density in the \( x \)-direction.
the injected carrier density \( n_{\text{inj}} \). Thus, the average \( \eta \) is characterized by (see Note S1, Supporting Information for details):

\[
\eta = \frac{n_{\text{SP}}}{n_{0}} = n_{\text{inj}} r_{T} = \frac{W C_{i} (V_{G} - V_{\text{th}}) V_{t} \epsilon_{sc} \mu_{1}}{L S d (q n_{0})^{2}}
\]

(3)

Here, \( r_{T} \approx d/\mu_{1} \Delta V \) with \( \Delta V = V_{2} - V_{1} \). \( r_{T} \) and \( \epsilon_{sc} \) are the permittivity, length, and current area of the nongated semiconductor; \( V_{t} \) is the potential at the end of the gated-channel (with the upper limit \( V_{G} \) or \( V_{\text{th}} \)); \( \mu_{1} \) and \( \mu_{2} \) are the carrier mobility in the gated and nongated semiconductors.

The impacts of materials and device factors on \( \eta \) are summarized in Equation (3). The \( \eta \) is also an indicator for how severe the charges injected from the gated semiconductors are limited by the transport in the nongated semiconductors: a) with weak injection and fast relaxation (\( \eta \ll 1 \)), most injected carriers kept unrelaxed, giving the non-Ohmic law for the currents injected from the gated semiconductors are limited (Figure 1c-I); b) with strong injection and slow relaxation (\( \eta \gg 1 \)), most injected carriers kept unrelaxed, giving the non-Ohmic law for the currents injected from the gated semiconductors are limited (Figure 1c-II); c) when the density of trap states \( n_{t} \) is comparable with that of mobile carriers, trap-limited SCLC (or “trap-fill limited,” TFL) dominates (Figure 1c-IV).

When estimating the average \( \eta \), \( V_{i} \approx (V_{G} - V_{\text{th}})/2 \) could be used. As \( \eta \) widely varies, a universal expression of the current density \( J \) is needed.

We simply assume \( J = n(n/n_{0})^{-1} q \mu_{1} \epsilon \epsilon_{0} / \mu_{0} = A_{1}^{n} q \mu_{1} \epsilon \epsilon_{0} \), where \( \mu_{1} \) is a characteristic mobility, \( \alpha = 1 \) and \( \gamma = 1 \) characterize the carrier-density\( (n)\)-dependent and field\( (\epsilon)\)-dependent mobility,[19,20] \( n_{0} \) and \( \epsilon_{0} \) are the characteristic trap density and electric field, and \( A_{1} \) is a constant. In particular, \( \delta = T_{c}/T \) if density of trap states is in exponential distribution with energy and \( T_{c} \) is the characteristic temperature (\( T_{c} > T_{i} \)). The general trap-limited (TFL) SCLC for disordered semiconductors is (see Note S2, Supporting Information):

\[
J_{\text{SCLC}} = A_{1}^{n} \frac{V_{n}}{d^{3/2}} \frac{\Delta V^{n}}{d^{n}} \propto \mu_{0} \Delta V^{n} d^{n}
\]

(4a)

where \( A_{1} = A_{1}^{n} \frac{v_{t}}{d^{3/2}} \mu_{0} \frac{\Delta V^{n}}{d^{n}} \propto \mu_{0} \).\( \frac{\Delta V^{n}}{d^{n}} \)

(5)

Here, \( C_{i} = \epsilon_{ox} / t_{ox} \) with \( \epsilon_{ox} \) as permittivity and \( t_{ox} \) as the thickness of the insulating layer below or above the gated semiconductor, and \( V_{\text{th}} \) is the onset voltage for the nongated channel (due to injection barriers or trap states). In the following, \( V_{\text{th}} \) is omitted for simplicity and could be included by replacing \( V_{\text{th}} \) with \( V_{\text{th}} - V_{\text{th}} \) whenever needed. For a drain-offset transistor, \( S = W t_{w} \) with \( t_{w} \) as the thickness of the nongated semiconductor. By defining the partial voltage coefficient \( \gamma = (L S Q_{\mu_{1}})/(W d^{2} C_{i} \mu_{2}) \) and assuming a small contact effect \( V_{c} \ll V_{i} \), Equation (5) becomes its voltage form:

\[
V_{i} = V_{G} - V_{th} - \frac{V_{i}}{2} = \gamma (V_{D} - V_{i})^{n}
\]

(6)

As \( V_{i} < V_{D} \), the second-order Taylor series is applied to the right and the accurate and approximated solutions are:

\[
V_{i} \approx \frac{\gamma (V_{C} - V_{th})^{n}}{2} - 2 \gamma V_{D}^{n}
\]

(7)

where \( a = 1 + \gamma \alpha (1 - 1) \gamma^{n} - 1 \), \( b = -2 (V_{C} - V_{th} + a \gamma V_{D}^{n}) \), and \( c = 2 p V_{C}^{n} \) (Note S4, Supporting Information). The accurate solution is used below and the approximated solution is for very small \( \gamma \) (e.g., when the nongated channel is with low conductance).

### 3. The Device Performance

#### 3.1. Current–Voltage Relations

How materials and device factors affect conduction mechanisms could be understood by combining Equations. (3) and (4). For example, the transport factor \( \alpha \) is very sensitive to \( n_{0} \) as \( \eta \approx 1/n_{0}^{2} \) and, thus, if the semiconductor become rich in carrier-generating states \( (\eta \ll 1) \), the SCLC-Ohmic transition could occur \( (\alpha \) decreases from 2 toward 1). Conversely, if the injection from the gated channel \( (C_{i} V_{C}) \) significantly increases or the nongated channel becomes rich in trapping states \( (\eta \gg 1) \), the Ohmic-SCLC transition may occur or even to the trap-limited SCLC \( (\alpha \) increases from 1 toward 2 and beyond).

Taking a drain-offset transistor, or similarly a transistor-diode hybrid integration, as an example (Figure 1b with \( V_{i} = V_{D} \)), the gated and nongated channel (Equations 1 and 4) are coupled and mutually limit each other:

\[
I_{D} = \frac{W}{L} \mu_{1} C_{i} \left( V_{C} - V_{th} \right) \left( V_{D} - V_{i} \right) / 2 = Q_{0} \mu_{2} \left( V_{D} - V_{i} \right)^{n}
\]

Here, \( C_{i} = \epsilon_{ox} / t_{ox} \) with \( \epsilon_{ox} \) as permittivity and \( t_{ox} \) as the thickness of the insulating layer below or above the gated semiconductor, and \( V_{\text{th}} \) is the onset voltage for the nongated channel (due to injection barriers or trap states). In the following, \( V_{\text{th}} \) is omitted for simplicity and could be included by replacing \( V_{\text{th}} \) with \( V_{\text{th}} - V_{\text{th}} \) whenever needed. For a drain-offset transistor, \( S = W t_{w} \) with \( t_{w} \) as the thickness of the nongated semiconductor. By defining the partial voltage coefficient \( \gamma = (L S Q_{\mu_{1}})/(W d^{2} C_{i} \mu_{2}) \) and assuming a small contact effect \( V_{c} \ll V_{i} \), Equation (5) becomes its voltage form:

\[
V_{i} = V_{G} - V_{th} - \frac{V_{i}}{2} = \gamma (V_{D} - V_{i})^{n}
\]

(6)

As \( V_{i} < V_{D} \), the second-order Taylor series is applied to the right and the accurate and approximated solutions are:

\[
V_{i} \approx \frac{\gamma (V_{C} - V_{th})^{n}}{2} - 2 \gamma V_{D}^{n}
\]

(7)

where \( \alpha = 1 + \gamma \alpha (1 - 1) \gamma^{n} - 1 \), \( b = -2 (V_{C} - V_{th} + a \gamma V_{D}^{n}) \), and \( c = 2 p V_{C}^{n} \) (Note S4, Supporting Information). The accurate solution is used below and the approximated solution is for very small \( \gamma \) (e.g., when the nongated channel is with low conductance).
The *I–V* relations described by Equations (5 and 7) with *V* <sub>q</sub> ≈ 0 are qualitatively illustrated in Figure 2. In output characteristics (Figure 2a), |I<sub>D</sub>| increases with |V<sub>D</sub> − V<sub>0</sub> <sub>D</sub>| (approximately with |V<sub>D</sub> − V<sub>0</sub> <sub>D</sub>|<sup>α</sup> as often |V<sub>D</sub>| ≪ |V<sub>0</sub>|) until *V* <sub>D</sub> reaches the saturated voltage *V* <sub>D, SAT</sub>, beyond which the current saturates due to pinch-off. In transfer characteristics (Figure 2b), |I<sub>D</sub>| increases with (V<sub>G</sub> − V<sub>0</sub>)<sup>2</sup> until |V<sub>D, SAT</sub>| > |V<sub>D</sub>|, beyond which the current is limited by the non gated channel. When the non gated channel has high conductance (large γ), the device behaves like a regular transistor; otherwise, the current is limited by the non gated channels (small γ) in the case of Ohmic current, SCLC, or trap-limited SCLC. Conduction mechanisms could change if changing materials or device factors according to Equation (3).

The impacts of material and device factors on the ratio *η*, charge transport factor *α*, and charge density factor *Q*<sub>0</sub> are summarized in Figure 3a. The original data are given in Figure S1 (Supporting Information). As an example, the impacts of donor-like and acceptor-like states on *I–V* characteristics are shown in Figure 3b–h, including the 2D-TCAD simulation (dots) and the fitting using Equations (5 and 7) (curves). The 2D-TCAD simulations were performed by solving Poisson equations and continuity formulas in fine grids and parameters are shown in Table S1 (Supporting Information). For donor-like states, the peak energy is fixed below the conduction band edge (CB, or lowest unoccupied molecular orbit LUMO) with the same characteristic width (*w<sub>D</sub>*) and the characteristic width (*w<sub>0</sub>*) is varied (Figure 3b). For acceptor-like states, the maximum of the exponentially distributed acceptor-like tail states (*N<sub>α</sub>*) is fixed as 10<sup>18</sup> cm<sup>-3</sup>, while the characteristic width (*w<sub>α</sub>*) is varied (Figure 3b). With more donor-like states, e.g., increasing *n<sub>D</sub>* = 10<sup>15</sup> cm<sup>-3</sup> to *n<sub>D</sub>* = 10<sup>16</sup> cm<sup>-3</sup>, the estimated ratio *η* by Equation (3) sharply decreases from 151 to 1.5 (using *V*<sub>1</sub> = *V*<sub>G</sub>/2 = 1.5 V), suggesting that *α* would change from 2 toward 1. Consistently, the transport factor *α* decreases from 2 to 1 as *N<sub>α</sub>* increases, as shown in Figure 3c,d. By contrary, *α* increases beyond 2 as the DOS of acceptor-like states broadens (*w<sub>α</sub>* increases). The evolution of output and transfer characteristics (Figure 3e–h) could all be understood by that: when *N<sub>α</sub>* increases, *Q*<sub>0</sub> (and thus γ) increases, leading to the increased *V*<sub>1</sub> (and thus *f<sub>β</sub>*) and decreased *V* <sub>D, SAT</sub>; the opposite occurs when *w<sub>α</sub>* increases. Using Equation (3) with a single set of *Q*<sub>0</sub> and *α* provides good fitting to both *I*<sub>D</sub>.
3.2. Potential and Field Evolution

The evolution of local channel potential $V(x)$ can be derived from Equation (5):

$$V(x) = (V_G - V_{th}) \left( 1 - \sqrt{1 - \frac{x}{L}} \right), \text{ for } 0 < x < L$$  \hspace{1cm} (8a)

and $V_i$ simultaneously for all the cases (Figure 3e–h), validating the simplified physical picture.

where $\theta$ is defined as the saturation degree, $\theta = 2V_i/(V_G - V_{th} - V_i/2)/(V_G - V_{th})^2$, and $0 < \theta \leq 1$. It quantifies the impacts of drain and gate voltages on the operational regime: when $\theta \ll 1$ or $\theta = 1$, the gated channel is in the linear or saturated regime, respectively. In general, distributions of $V(x)$ are characterized by $\theta$ and $\alpha$ (illustrated in Figure 4a) and will change when voltages or material properties significantly change.
The impacts of voltage scanning are exemplified in Figure 4b,c and 4d,e for an unsaturated, gated channel with the reasons for the transition (i.e., changing \( V_D \) or \( V_G \)). The impacts of materials are exemplified in Figure 4f,g by inducing donor-like states with Ohmic conduction (\( \alpha \approx 1 \)) in the nongated channel and in Figure 4h,i by inducing acceptor-like states with trap-limited SCLC (\( \alpha > 2 \)). At the meantime, the gated channel also changes to the saturated regime (Figure 4f, \( \theta = 1 \)) or the linear regime (Figure 4h, \( \theta < 1 \)) due to the increased or decreased partial voltage coefficient \( \gamma \) (and thus \( V_J \)), respectively. For all the cases, the calculations by Equation (8) curves agree well with the 2D TCAD simulation (dots). Also, we could obtain the drift electric field by \( E_D(x) = -dV/dx \), Joule heating power density by \( p(x) = |J|E_D(x) \), and carrier density by \( n(x) = J/(\mu E_D) \) using Equations (5) and (8) or probing \( V(x) \) in experiments for partially gated or even regular transistors.

3.3. Current Saturation

Current saturation occurs when carrier concentration becomes depleted near the end of the gated channel, with \( V_J \) reaching \( (V_G - V_{th}) \) and \( V_D \) reaching \( V_{D,SAT} \). As \( V_{D,SAT} \) is the turning point in \( I-V \) curves (Figure 2) and critical for stabilizing current and tolerating signal fluctuations, it is derived from Equation (7):

\[
V_{D,SAT} = (V_G - V_{th}) + \sqrt{(V_G - V_{th})^2/(2\gamma)}
\]

Here, \( \epsilon_{ox} \) and \( \kappa_{ox} \) are the permittivity and thickness of the dielectric layer and \( S = W_{th} \). The approximate equal sign holds when \( \gamma \) is small or, instead, \( V_{D,SAT} \) approaches the classic \( (V_G - V_{th}) \) when \( \gamma \) is large. Accordingly, \( V_{D,SAT} \) increases linearly with \( (V_G - V_{th})^2 \) or \( (V_G - V_{th}) \) with ideal Ohmic conduction or SCLC, respectively. We use a trap-free semiconductor in simulations to examine \( V_{D,SAT} \) of devices with varied parameters (\( V_{th}, \kappa_{ox}, d \), and \( L \), Figure 5a), which fall in the same line calculated by Equation (9) with \( \alpha = 2 \) (SCLC regime, Figure 5b and Figure S2, Supporting Information). The materials or device factors that lead to increased \( V_{D,SAT} \) are also indicated by the gray arrow.

Interestingly, the method helps to answer another longstanding problem: how to estimate the drain depletion-region length \( \Delta L \), Figure 5c) in a saturated TFT? As this region is depleted (\( n_{ox}/n_0 \gg 1 \)) and narrow (\( \tau_I/\tau_T \gg 1 \)), \( \Delta L \) could be estimated by using Equation (5) with \( V_J = V_G - V_{th}, V_2 = V_D, d = \Delta L \) and the SCLC limit:

\[
\Delta L = \sqrt[4]{\frac{2IQD_{th}C_1}{\mu_1} \left( \frac{V_D - V_{th}}{V_G - V_{th}} \right)^2} \approx \frac{9}{4} \left( \frac{V_D}{V_G - V_{th}} - 1 \right)^2 \cdot \sqrt{L^2}
\]
where \( \lambda = \sqrt{\frac{\varepsilon_{ox}}{t_{ox}L^2}} \) is the natural length. The \( \Delta L \) in accumulation-mode, thin-film based transistors is predicted to increase with \( \lambda^2 \), different from conventional inversion-mode, pn-junction based MOSFETs. This is consistent with the extracted \( \Delta L \) by varying \( t_{ox} \) or \( t_{sc} \) in TCAD simulation (Figure 5c and Figure S3, Supporting Information). The undesired channel length modulation characterized by \( \Delta L = t_{ox} \) would be intensified in short-channel TFETs, but could be weakened by decreasing \( \lambda \) (Note S5, Supporting Information). It also quantifies the advantages of using ultra-thin semiconducting films in short-channel FETs in terms of weakening the channel modulation.

4. Applications

4.1. Applications with Various Semiconductors

When using organic semiconductors in transistors or transistor–diode integrations, charge carriers are generally intrinsically low (\( n_0 < 10^{20} \text{ cm}^{-3} \)) and thus usually with \( \eta \gg 1 \) and \( \alpha \approx 2 \). But charge transport of polarons could be limited by structural disorders so that it takes the forms of trap-and-release, variable range hopping, charge transfer, nuclei tunneling, and etc. The macroscopic conductance as a function of temperature and gate-field could be described by the thermal activation of carriers near the exponentially distributed tail states. In these cases, \( \alpha = T_f/T > 1 \) is expected, especially in a disordered film with localized tail states or trapping states. We have shown that various transport mechanisms of organic semiconductors could be universally described by the generalized Einstein relation, so that the gate- and temperature-dependent mobility of organic semiconductors could be included in the current framework. In addition, organic FETs usually suffer from significant contact injection barriers that lower the on-current and cut-off frequencies and, thus, the contact potential \( V_S \) should be considered.

When using metal-oxide semiconductors as the nongated channels, the carrier density and field-dependent transport mechanisms include the trap-limited conduction, variable range hopping, and percolation. As the intrinsic carrier concentration is also usually low with abundant defects, \( \eta \gg 1 \), \( \alpha > 2 \), and a small value of \( Q_0 \) close to or below the SCLC limit would be expected. In contrast, when using semiconductors with high carrier densities as the nongated channels for light-emitting or detecting, e.g., perovskites and 2D narrow-bandgap materials, we expect \( \eta \ll 1 \), \( \alpha \approx 1 \), and \( Q_0 \approx qn_0 \). The mentioned materials will be studied in various devices in the following section.

4.2. Applications in Various Transistors and Hybrid Integration

As the first example, transistors in the drain-offset structure have been used to stabilize current or to make high-voltage TFETs for driving field-emitters, piezoelectric actuators, or integrated MEMS. Drain-offset transistors were fabricated based on amorphous N-doped InGaZnO\(_4\) semiconductor (\( t_{sc} = 60 \text{ nm} \)), which is chosen for its relatively large bandgap (\( \gtrsim 3 \text{ eV} \)) and low intrinsic carrier concentration to investigate the current limitation from the nongated channels. The methods of fabrications and measurements are the same as described elsewhere. The electrodes are Mo (\( L = 200 \text{ nm} \), \( d = 100 \text{ nm} \), and \( W = 40 \text{ nm} \)) and the dielectric layer is SiO\(_2\) (\( t_{ox} = 300 \text{ nm} \)). The measured output characteristics are shown in Figure 6b,c, with the dots and curves representing the experimental data and fitting, respectively. The estimated \( \eta \) as an indicator is about 192 due to low carrier density in the N\(_2\)-doped InGaZnO\(_4\).
(n₀ ≈ 10^{15} \text{ cm}^{-3}, V_C = 30 \text{ V}). The fitting results are calculated by the total resistance \( R_{\text{tot}} \) with the channel resistance \( R_{\text{CH}} \) and a back-channel resistance \( R_{\text{BACK}} \) in parallel. \( R_{\text{CH}} \) is calculated by Equations (5 and 7) using the same parameter \( \alpha \) (with \( \beta = 2\alpha - 1 \)) and a fitting parameter \( Q_0 \), while \( R_{\text{BACK}} \) is extracted by \( R_{\text{BACK}} = \partial V_D/\partial I_D \) beyond \( V_D,\text{SAT} \). The simple fittings agree well with the experimental data with \( \alpha = 2.3 \) (trap-limited SCLC), corresponding well with the disordered transport in amorphous InGaZnO₄. The values of \( V_{D,\text{SAT}} \) increase almost linearly with the \( V_C \) (Figure 6, top) and this is also consistent with the above theories. The charge density factor \( Q_0 \) changes slightly when varying \( V_C \) (Figure 6, bottom). Thus, the drain-offset, high-voltage TFTs could be understood by the above physical framework.

Transistor hybrid integration, e.g., with photo-diodes, light-emitting diodes, field emitters, or others for various functions, could also be effectively simplified by the above approach. As the first example, the transistor-photodiode integration was fabricated by integrating a vacuum-deposited InGaZnO₄ TFT and solution-processed a vertical photodiode based on perovskite-organics [ITO-SnO₂-(FASnI₃)₀.₆(MAPbI₃)₀.₄-poly(3-hexylthiophene)-Au, Figure 6e]. The perovskite semiconductor is chosen as a representative, light-sensitive semiconductor with relatively high carrier concentrations and Ohmic conduction in
Figure 7. Exemplary results of fast computing split-gate transistors. a) A schematic representation of the transistor structure. For transfer characteristics, b,d) the current $I_D$ and c,e) the potential drop $V_2-V_1$ at varied $V_{G1}$ and $V_{G2}$ with fixed $V_D = 6$ V, where (b, c) is obtained from the TCAD simulation (0.5 V step) and (d, e) are from calculations by Equation (11) (0.05 V step). The computing time on the same computer is about 50 min and 2 s, respectively. For output scanning, the data for varied $V_D$ and $V_{G2}$ with fixed $V_{G1} = 6$ V are shown in (f–i) in the same order.

a diode structure.\cite{39,40} The methods of fabrication and measurement are the same as described elsewhere.\cite{39} The parameters for experimental devices are: $W = 1600$ μm, $L = 40$ μm, $t_c = 60$ nm, $t_{ox} = 300$ nm (SiO$_2$), and $V_d = 0.1$ V. Due to the high carrier density in perovskite semiconductors, the photodiodes exhibit Ohmic conduction behaviors in $J$–$V$ characteristics\cite{39} so that $\eta \ll 1$ and $\alpha = 1$ is used here. The transfer curves are shown in the linear or semilog scale with the fitting curves (Figure 6h). These results are consistent with the above discussions and verify that $Q_0$ reflects the photogenerated carrier density in the non-gated channels (photodiodes). As the second example, the performance of MoS$_2$–TFT and OLED integration (Figure 6i) is predicted by using Equations (5 and 7) with the device and material parameters as reported in reference\cite{38} and with the ideal SCLC, giving the results ($\alpha = 2$, Figure 6i) close to the experimental data reported in reference.\cite{38} The 2D semiconductors are the extensively studied candidates for ultra-thin, fast logic devices.\cite{10} As the third example, Si-FET and ZnO–nanowire–emitter integration (Figure 6k) were fabricated as described elsewhere\cite{41} and the $I$–$V$ characteristics are shown in Figure 6k. The nanowire emitter is studied here as it could be used in the source of fast electron beams for microscope or nanolithography technologies.\cite{42} The $I$–$V$ characteristics could be fitted by using Equations (5 and 7) with $\alpha = 2.1$, supporting that the field-emission by F–N tunneling into vacuum at large anode bias $V_A$ could also be approximated by Equation (5). These results confirm the proposed physical framework could also be applied to understand and simplify transistor hybrid integration.

4.3. Applications in Fast Computing of Complex Transistors

The above theory provides opportunities for fast computing or design aid of complex transistors. As a demonstration, a compiled HTML file is provided to calculate drain-offset transistors, mid-gate transistors, solid-state vacuum triodes, split-gate transistors, and transistor hybrid integration according to the input parameters (see Figures S4 and S5, Supporting Information). The calculated results presented in this manuscript could be obtained by using this file. As an example, split-gate transistors have been made (e.g., with MoS$_2$ or WSe$_2$)\cite{8,43} for fast sensing and computing applications and could be regarded as the gated/nongated/gated structure. A typical device structure is illustrated in Figure 7a. Denote the gate voltages as $V_{G1}$ (near the source) and $V_{G2}$ (near the drain) and the current is:

$$I_D = \frac{W}{L_1} \mu_1 C_i \left( V_{G1} - V_{th1} - \frac{V_1 + V_2}{2} \right) (V_1 - V_S)$$

$$= S Q_0 \mu_2 \frac{(V_2 - V_1)^\beta}{d^\theta}$$
here, $V_1$ and $V_2$ are the potential at the end and beginning of the two gated channels. Calculation methods are given in Note S6 (Supporting Information). Exemplary results of calculated transfer characteristics with the same set of parameters are presented by plotting the contours of $I_D$ and the voltage drop across the nongated channel $V_2 - V_1$ in Figure 7d,e which agree well with the 2D-TCAD simulation shown in Figure 7b,c but consume about 1000 times less time. In particular, the asymmetric impacts of $V_{G1}$ and $V_{G2}$ on $I_D$ and $V_2 - V_1$ are clearly observed with details in Figure 7d,e, dashed ovals. Output characteristics are shown in Figure 7f–h. The results demonstrate that the simplified physical picture may provide a physical-meaningful platform for few-shot learning to train parameters and to model and predict the performance of complex transistors.

For computing other transistors or transistor integration in Figure 1a, similar approaches could be applied by modifying Equation (5). For example, mid-gate transistors and solid-state vacuum triodes (or so-called “static induction transistors”) (Figure 1a) could be treated by rewriting Equation (5) corresponding to the nongated/gated/nongated structure (Note S7, Supporting Information). In general, mid-gate transistors usually have Ohmic conduction in the non-gated channels to allow Ohmic injection (e.g., Ga$_2$O$_3$ transistors [45]), while static induction transistors usually have SCLC in the non-gated channels to keep the low off-current.

6. Experimental Section

Device Simulation: The 2D-TCAD simulations were performed by solving Poisson equations and continuity formula in fine grids. The device parameters are $W = 1000$ μm, $L = 8$ μm, $d = 2$ μm, $t_{ox} = 20$ nm, $\mu_i = \mu_s = 1$ cm$^2$V$^{-1}$s$^{-1}$, and $C_i = 1.1 \text{ nF cm}^{-2}$. More details of simulation and fitting parameters are given in Tables S1–S3 and Notes S5 and S6 in Supporting Information.

Device Fabrication: Drain-offset transistors were fabricated based on amorphous N$_2$-doped InGaZnO$_4$ semiconductor ($t_{ox} = 60$ nm). The methods of fabrications and measurements are similar to previous studies.[31] Bottom-gate, inverted staggered TFTs with an offset-gate were fabricated on glass substrates. The electrodes are Mo ($L = 200$ μm, $d = 100$ μm, and $W = 40$ μm) and the dielectric layer is SiO$_2$ ($t_{ox} = 300$ nm). Gate electrodes were formed by the deposition of a 200 nm thick Mo layer that was subsequently patterned with wet etching. The gate insulator was then deposited by plasma-enhanced chemical vapor deposition (PECVD). A 60 nm thick InGaZnO$_4$ film was sputtered on the gate insulator and etched to form an active layer. The InGaZnO$_4$ deposition was conducted under nitrogen gas to introduce nitrogen doping, which helped to improve the stability of InGaZnO$_4$. In sputtering, the gas flow was Ar/O$_2$/N$_2$ = 30:0.5:1 in the unit of sccm with the power of 900 W. The source and drain electrodes were formed by sputtering and lift-off processes. A passivation layer was deposited by PECVD and electrode holes were etched by reactive ion etching. Finally, the devices were annealed at 350 °C for 1 h in nitrogen atmosphere.

Transistor–photodiode integration was fabricated by integrating a vacuum-deposited InGaZnO$_4$ TFT and solution-processed a vertical photodiode based on perovskite–organics [ITO–SnO$_2$-(FASnI$_3$)$_{10.6}$ (MAPbI$_3$)$_{0.4}$]-poly(3-hexylthiophene)-Au. The methods of synthesis of (FASnI$_3$)$_{0.6}$ (MAPbI$_3$)$_{0.4}$, fabrication of photodiodes, and integration of photodiodes with TFTs are the same as described elsewhere.[39] The parameters for experimental devices are: $W = 1600$ μm, $L = 40$ μm, $d = 0.5$ μm, $t_{sc} = 60$ nm, $t_{ox} = 300$ nm (SiO$_2$), and $V_D = 0.1$ V. The area $S$ for a pixel of photodetector is 1925 μm $\times$ 1925 μm.

Si-FET/ZnO–nanowire–emitter integration was fabricated by growing ZnO nanowires on the drain electrode of a MOSFET, as described elsewhere.[41] N-channel enhancement MOSFET (Infineon: BSP 324) was used for the high maximum-rating drain–source voltage (400 V). The layers of Cr (200 nm) and Zn seed material (100 nm) were selectively deposited on the drain electrode of the MOSFET by sputtering. A solution was prepared by mixing zinc nitrate hexahydrate and hexamethylenetetramine (1:1) with the concentration of Zn$^{2+}$ 2 µmol L$^{-1}$. Then the substrates were suspended with top-side down in the solution at 80 °C for 18 h for growing ZnO nanowires.

Device Characterization and Analysis: Drain-offset transistors were measured for high-voltage test by using a high-voltage semiconductor test system (Keithley 2657A and Keithley 2450). In the drain-offset InGaZnO$_4$ transistors (Figure 6), the common parameters for fitting are: $\mu_i = 10$ cm$^2$V$^{-1}$s$^{-1}$, $\mu_s = 1$ cm$^2$V$^{-1}$s$^{-1}$, $V_D = 0.75$ V, and the charge transport factor $\alpha = 2.34$. The charge density factor $Q_D$ depending on $V_C$ are $Q_D = 1.3 \times 10^{-11}$, $1.1 \times 10^{-11}$, $9.9 \times 10^{-12}$, $8.2 \times 10^{-12}$, or $6.9 \times 10^{-12}$ C cm$^{-2}$, for $V_C = 30$, 26, 22, 18, or 14 V.

For transistor–photodiode integration with InGaZnO$_4$-TFT and a PSK-photodiode, the electrical characteristics were characterized in air by a semiconductor parameter analyzer (Agilent, B1500A) in the dark or under illumination with a LED (wavelength 850 nm). The common parameters for fitting are: $\mu_i = 8 \{1 - \exp \left(-\left(V_{G2}/17\right)^2\right)\} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, $\mu_s = 0.1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, $\alpha = 1$. The charge density factor $Q_D$ and threshold voltage $V_D$ depending on illumination power are $Q_D = 1.1 \times 10^{-7}$, $2.4 \times 10^{-7}$, $5.7 \times 10^{-8}$, $3.6 \times 10^{-9}$, and $2.9 \times 10^{-9}$ C cm$^{-2}$ and $V_{th} = -8.5$, -7.0, -6.8, or -6.5 V for $P = 1374$, 128.3, 302.0, or 276.0 W.

For MoS$_2$-TFT and OLED simulation the parameters for calculating the transistor–OLED integration are defined according to the reference:[18] $W = 300$ μm, $L = 4$ μm, $d = 0.1$ μm, $S = 0.09 \times 0.09 = 0.0081$ cm$^2$, $C_i = 1.6 \times 10^{-7}$ F cm$^{-2}$ (50 nm Al$_2$O$_3$ with $t_{ox} = 9$ nm), $\mu_i = 18$ cm$^2$V$^{-1}$s$^{-1}$ (MoS$_2$), $V_D = 4$ V, $\mu_s = 0.0005$ cm$^2$V$^{-1}$s$^{-1}$ (OLED), and $V_D = 3$ V. Then the $I$–$V$ characteristics are calculated by Equations (5) and (7) with the factors as

$$\frac{W}{L} \mu_i C_i \left( V_{G2} - V_{th2} - \frac{V_D + V_2}{2} \right) \left( V_D - V_2 \right) \quad (11)$$

5. Conclusion

The charge transport of semiconductors in transistors with non-trivial gates or hybrid integration could be simplified and understood in the same physical picture of “charge carriers from gated into nongated semiconductors.” The conduction in the nongated semiconductors is a synergetic result of charge transport in the gated semiconductors and carrier relaxation, transit, and transport in the non-gated semiconductors. A general theoretical framework is derived to describe $I$–$V$ relation, current saturation, evolution of potential and drift field for various transistors with nontrivial gates or transistor–diode integration. Within the framework, how materials and device factors determine the performance could be briefly understood by: a) the space-charge-to-free-carrier ratio $\eta$ as an indicator that characterizes how severely the charges injected from the gated semiconductor are limited by the transport in the nongated semiconductor; b) the charge transport factor $\alpha$ and charge density factor $Q_D$ that characterize the conduction mechanisms from Ohmic to SCLC and then to trap-limited SCLC; c) the partial voltage coefficient $\gamma$ that characterizes the voltage distribution between the coupled channels (an increased $\gamma$ leads to an increased $V_2$ across the gated channel). The understanding has been verified by numerical simulations and agrees well with device experiments and a device calculator is demonstrated. Having general applicability, the approach may be combined with specific properties of semiconductors and devices and provide a straightforward way to quickly understand, model, design, and analyze complex transistors or hybrid integrations and the semiconductors in them.
$\alpha = 2$ and $Q_0 = 3 \times 10^{-13}$ C cm$^{-3}$ (ideal SCLC and $e_{SC} = 3e_0$ for organic semiconductors).

For Si-MOSFET and ZnO-emitter integration, the field emission current of the ZnO nanowire in the integrated device was measured while they were being controlled by the Si-MOSFET. The integrated device was placed in a high-vacuum chamber ($5 \times 10^{-5}$ Pa). The anode current was probed by a monitored with a stainless-steel probe (1 mm diameter) and biased by a power supply picoammeter (Keithley 6487).

Device Calculation: A calculator for different devices is compiled in an open-source, HTML file with a user interface for demonstration and testing in the Supporting Information. Readers may open the "index" file to use it and read the "Manual" file for assistance. The calculator was tested by comparing some results with those obtained from TCAD simulations with varied device or material parameters. The calculations and fittings in this manuscript could be obtained by setting the corresponding parameters in this calculator. The calculator could be used to fit the experimental data or predict performance of some transistors. When calculating the split-gate transistors, the device has the dimension of $L_1 = 8 \mu m$, $d = 2 \mu m$, and $L_2 = 8 \mu m$ with other parameters as the same as those in the drain-offset transistors.

Supporting Information
Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements
The authors gratefully acknowledge the financial support of the project from the National Natural Science Foundation of China (61922090). C.L. derived theories, performed simulations, and analyzed the data. X.L., S.H., and Y.W. fabricated and measured devices. Y.L. wrote the HTML codes for device calculation. All authors contributed to discussions. SJC acknowledges the financial support from the Natural Science Foundation of Guangdong Province, China (2018B030311045).

Conflict of Interest
The authors declare no conflict of interest.

Data Availability Statement
The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords
charge transport, field-effect transistors, hybrid integration

Received: October 30, 2021
Revised: November 14, 2021
Published online: December 16, 2021

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