Simultaneous Boron Emitter Diffusion and Annealing of Tunnel Oxide Passivated Contacts Via Rapid Vapor-Phase Direct Doping

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Abstract—n-type silicon-based tunnel-oxide passivating contact (TOPCon) solar cells are a cell concept reaching highest power conversion efficiencies. In this article, we demonstrate a substantial simplification of processing such TOPCon solar cells by reducing the number of high temperature processes. To this end, rapid vapor-phase direct doping (RVD) processes are applied for emitter formation and simultaneous annealing of the TOPCon layers within one process. RVD emitters with sheet resistances of 200 Ω sq⁻¹ reach low emitter saturation current densities of 26 fA cm⁻² on textured surfaces. Thermal interface oxides of the TOPCon layers were adapted to withstand the increased thermal budget of the RVD process. Optimized layers exhibit a saturation current density of less than 1 fA cm⁻² and a contact resistance of 5 mΩ cm⁻². The best solar cell with the simultaneous emitter diffusion and TOPCon annealing during the RVD process reaches a confirmed efficiency of 23.3%, similar to a reference with sequential BBr₃ diffusion and subsequent TOPCon deposition and annealing reaching 23.1%.

Index Terms—Boron emitter, poly-si passivating contacts, rapid vapor-phase direct doping (RVD), tunnel-oxide passivating contact (TOPCon).

I. INTRODUCTION

Solar cells with tunnel-oxide passivating contacts (TOPCon) have been investigated for several years and when implemented on the rear of a both-side contacted n-type front emitter cell a very high efficiency of 25.8% has been demonstrated [1]. Typically, these poly-Si-based passivating contacts are deposited after the emitter was formed via BBr₃ diffusion [2]–[5] or ion implantation [6]. An alternative for this emitter formation process is the rapid vapor-phase direct doping (RVD) process [7]–[9]. In contrast to the conventional BBr₃ diffusion, RVD diffusion is not carried out in oxygen containing atmosphere but pure hydrogen and diborane (B₂H₆) is used as boron precursor. During the RVD process doping atoms are directly incorporated into the silicon wafer without forming a silicate glass. Thus, a removal step of the silicate glass is not necessary. Moreover, the profile can be tuned not only by temperature and time, but also by changing the B₂H₆ content in the gas atmosphere [10]. This property in principle enables an in-situ drive-in step simply by switching off the B₂H₆ gas.

n-type TOPCon cells with B-RVD emitters as schematically shown in Fig. 1 were already successfully realized using a sequential process with emitter diffusion on the front side prior to the TOPCon processes on the rear side [9]. These cells reached a high efficiency of up to 23.9% for a homogeneous emitter diffused at 1030 °C, which demonstrates the potential of RVD. However, in that study the RVD cells showed slightly reduced open circuit voltages (V_{OC}) and short-circuit current densities (J_{SC}) when compared to reference cells diffused with a conventional BBr₃ process. The reduced J_{SC} resulted from a slight flattening of the surface texture during RVD processes at 1030 °C. The reason for the V_{OC} reduction might be caused by an increased incorporation of impurities with increasing RVD process temperature in a not ideal furnace. Both limitations
might be circumvented by reducing the process temperature and the contamination of the silicon bulk during the RVD process.

A variation of RVD parameters with temperatures up to 1000 °C showed a wide variation of possible emitter profiles. The additional application of a diffusion barrier between samples and quartz holders protected the samples from incorporation of impurities from the quartz holders and led to an improved bulk lifetime. The optimized RVD process featured a process temperature of 950 °C. This process was applied for all experiments within this publication. It enabled a bulk lifetime of 3.5 ms for 1 Ω cm n-type FZ wafers [10].

This reduced thermal budget simplifies the consolidation of the two high temperature process steps during the fabrication of TOPCon cells: the emitter diffusion and the annealing of the TOPCon layers. In this case the deposition of the TOPCon layers (growth of the interfacial oxide and doped a-Si deposition) is done before the emitter diffusion process. A simultaneous process was already successfully demonstrated for p-type Si cells and POCl₃ diffusion and n-type Si cell precursors with the B-RVD process, both processes were performed at 900 °C [10], [11]. For the latter n-type TOPCon precursors, however, the corresponding emitter profile was too shallow and the series resistance too high for fabrication of a high efficiency solar cell.

This article builds upon these prior results to achieve the goal of excellent simultaneous annealing of poly-Si and diffusion of boron. The properties of the resulting optimized RVD emitter are discussed in detail. The thermal budget of this emitter process requires an adaption of the TOPCon layer, especially the interfacial oxide layer. Finally, results of first solar cells with the simultaneous emitter diffusion and TOPCon annealing process are shown.

II. EXPERIMENTAL PROCEDURE

For all experiments n-type FZ Si wafers (1 Ω cm, 200-μm thick, (100)-oriented, shiny etched) were used unless marked explicitly. The wafers were thermally oxidized to prevent recombination due to FZ bulk defects [12], [13]. Before further processing this oxide was removed wet-chemically if not stated differently.

A. Boron Emitter Formation

For the emitter diffusion via RVD a chemical vapor deposition (CVD) reactor called RTCVD160 build at Fraunhofer ISE for epitaxial deposition of silicon was used [14]. For emitter diffusion diborane (B₂H₆) serves as dopant precursor in H₂ ambient. With this furnace a prove of principle of the RVD process and the simultaneous TOPCon annealing is possible. However, the design is not optimized for diffusion processes regarding throughput and homogeneity. In contrast to conventional diffusion furnaces, in the RTCVD160 two samples are positioned parallel to the main gas flow on top of silicon-carbide-coated silicon dummies in a large quartz carrier standing in a quartz tube. The optically heated furnace covers only the middle part of the quartz tube where the samples are positioned. This leads to a temperature gradient from room temperature up to the process temperature for larger quartz parts during the process. On some of these parts boron atoms are deposited during B-RVD processing leading to autodoping in subsequent processes even if boron is not, or only at low concentration, provided within the process. Therefore, a constant, high background boron content above the inserted B₂H₆ concentration is assumed for the processes described in this article.

Based on previous experiments the most promising diffusion process was chosen with a process temperature of 950 °C for 30 min [10]. The afore mentioned 275-nm thick thermal oxide grown to prevent recombination due to FZ bulk defects was maintained on rear sides to prevent boron diffusion during RVD and removed afterwards. Front sides were planar or alkaline textured (random pyramids) as in the final cells. As a reference a typical BBr₃ diffusion process in a tube furnace at 890 °C for 60 min was conducted. Lifetime samples were prepared using Al₂O₃ deposited by atomic layer deposition (ALD) and subsequent forming gas anneal (FGA) at 425 °C for 25 min as surface passivation layer on both sides resulting in asymmetric RVD emitter samples with a passivated emitter on the front and the passivated bulk on the rear side and symmetric BBr₃ emitter references.

B. Tunnel Oxide Passivated Contact and Annealing

To investigate TOPCon properties after annealing conditions similar to the RVD process, symmetrically coated samples were fabricated. After RCA cleaning [15], different tunnel oxides where thermally grown. Four oxidation processes were carried out in a tube furnace resulting in different oxide layers: TO1 was grown at 600 °C in an O₂/N₂ mixture atmosphere, TO2 at 600 °C in O₂, TO3 at 600 °C in O₂ with longer oxidation time and TO4 at 750 °C in O₂. After deposition of 50 nm phosphorus-doped amorphous silicon on both sides by plasma-enhanced CVD (PECVD, cPlasma, and centrotherm) [16], the samples were annealed either under standard conditions (TO1; 900 °C for 10 min in N₂) or with the thermal budget of the RVD process (TO2, TO3, TO4; 950 °C, 30 min in N₂ or H₂ atmosphere). The annealing in H₂ atmosphere was done in the RTCVD160 and samples were covered with 400 nm SiO₂ by in-line PECVD (MAiA, Meyer-Burger) on both sides before annealing to protect the TOPCon layer from boron diffusion due to the autodoping effect already mentioned. The final hydrogenation was done by deposition of 10 nm Al₂O₃ by ALD followed by FGA for 25 min at 425 °C.

C. Solar Cell Process

To study the simultaneous high-temperature processing sequence of emitter formation and TOPCon annealing during the RVD process at the device level, we have fabricated lab type TOPCon solar cells with an aperture area of 2x2 cm². The front side of the solar cells features an alkaline textured (random-pyramids) surface. Prior to the RVD diffusion, the full-area TOPCon electron contact on the rear surface was deposited in form of the ultrathin thermally grown SiO₂ layer TO2 covered by an about 50-nm thick phosphorous-doped amorphous Si layer deposited with a tube furnace PECVD (cPlasma, centrotherm). The TOPCon layer was capped with a 400 nm thick PECVD
SiO$_x$ layer to protect it from boron diffusion. The RVD boron diffusion was performed at 950 °C for 30 min. As a reference (Ref) for this simultaneous high temperature processing sequence, solar cells were also fabricated using two separate high temperature processes. First, the boron emitter was diffused using a conventional BBr$_3$ tube furnace process. Afterwards, the TOPCon layer deposition took place using TO1 followed by the anneal at 900 °C for 10 min in a tube furnace in a second high temperature process. The process flow is visualized in Fig. 2 for the reference and the RVD route.

C. Characterization Methods

Boron emitter profiles and phosphorus profiles of $n^+$-poly-Si contacts were measured by electrochemical capacitance voltage profiling (ECV, WEP Wafer profiler CVP21). Sheet resistances $R_{SH}$ of the emitters were measured by four-point probing.

Saturation current densities of passivated emitters $J_{0e}$ and of the $n^+$-poly-Si contacts were evaluated from quasi-steady-state photoconductance (QSSPC) measurements conducted with a Sinton WCT-120 lifetime tester [17] like described by Steinhauser et al. [18] using the Auger model described by Niewelt et al. [19]. In order to evaluate the $J_{0e}$ of the asymmetrically diffused RVD samples, the $J_0$ value of the rear surface (without $p^+$ diffusion) passivated with Al$_2$O$_3$ was assumed to be 1 fA cm$^{-2}$ obtained from reference lifetime samples.

Contact resistivities $\rho_{C,C}$ of the $n^+$-poly-Si contacts were determined using vertical dark current-voltage ($I-V$) measurements contacting both sides of the samples. To this end, symmetric test structures received a full-area metallization using an electron-beam evaporated stack of Ti, Pd, and Ag on the rear and seven 2x2 cm$^2$ size windows at the front. The poly-Si/SiO$_x$/c-Si contact resistivity was determined by fitting the $I-V$ curve around $V = 0$ V and subtracting $\rho_{C,base}$ of the base material ($\rho_{C}$ between metal/poly-Si is negligible small).

The 1-sun $I-V$ parameters of the solar cells were measured under standard testing conditions (STC: AM1.5g, 100 mW cm$^{-2}$, 25 °C) using a sun-simulator with an incident current calibration based on certified $I-V$ measurements (Fraunhofer ISE CalLab).

For single cells confirmed measurements were conducted at Fraunhofer ISE CalLab. The pseudofill factor ($PFF$) was extracted from illumination intensity vs. $V_{OC}$ (Suns $V_{OC}$) measurements using the Suns $V_{OC}$ setup from Sinton Instruments. The spatial distribution of the implied open-circuit voltage $iV_{OC}$ was determined from photoluminescence (PL) images at 1 sun illumination calibrated with a modulated PL measurement [20]. The PL measurements were performed with the Fraunhofer ISE modulum tool.

III. RESULTS AND DISCUSSION

A. Boron Emitter Formation

With the RVD process a large variety of boron emitter profiles depending on temperature, time and precursor gas flow is possible in principle [10]. Based on these results the most promising RVD process for the application in high-efficiency solar cells was chosen for further investigations. The corresponding profiles on planar and textured surfaces and on different sample positions are shown in Fig. 3(a) in comparison to a conventional BBr$_3$ emitter profile without drive-in step.

As mentioned in Section II-A the furnace used for the emitter diffusion via RVD is not optimized for this process. The resulting emitters are not spatially homogeneous over the whole 4 inch wafer but have a gradient with increased diffusion in the upper front part of the wafer with respect to the position and gas flow in the RTCVD160 furnace and a reduced diffusion in the bottom rear part of the wafer as can be seen in the sheet resistance map in Fig. 3(b). On planar surface the emitter profile is measured in the upper front quarter [RVD (p,u), red stars in Fig. 3(a)] and in the bottom rear quarter [RVD (p,b), blue circles in Fig. 3(a)]. These two profiles differ both in surface concentration and depth resulting in an almost doubled sheet resistance value ($R_{SH}$) in the bottom rear part (see Table I). This gradient is expected to be avoidable with a special furnace with wafer positioning and gas flows optimized for RVD processes.

Final cells have a textured surface instead of the planar one discussed by now. Depending on the diffusion regime the increased surface area could lead to a different profile. For the reference BBr$_3$ diffusion the boron containing silicate glass acts as an inexhaustible source for which no difference between planar and textured surfaces is expected. For RVD processes there is

| Sample       | $R_{SH}$ (Ω sq$^{-1}$) | $J_{0e}$ @ 25 °C (fA cm$^{-2}$) |
|--------------|------------------------|----------------------------------|
| RVD, planar, top | 102                    | 28 ± 10                          |
| RVD, planar, bottom | 194                  | 21 ± 7                           |
| RVD, textured, bottom | 200               | 26 ± 9                           |
| BBr$_3$, planar | 94                     | 27 ± 10                          |

TABLE I

Sheet resistance values $R_{SH}$ measured by four-point probing and emitter saturation current densities $J_{0e}$ evaluated from QSSPC measurements of RVD emitters on planar and textured surfaces. In addition, for $J_{0e}$ the estimated systematic uncertainty is given. For the BBr$_3$ reference RSH is determined from the ECV profile shown in Fig. 3(a).
no glass acting as dopant source, but the dopant containing gas is flowing across the wafer surface. In this case the diffusion regime might depend on process conditions like dopant gas flow and furnace geometry affecting the transport of molecules to the surface and doping profiles might be different on planar and textured surfaces. However, profiles measured on the same area on samples with planar [RVD (p,b), blue circles in Fig. 3(a)] and textured [RVD (t,b), green triangles in Fig. 3(a)] are very similar. Therefore, the doping gas source is assumed to be inexhaustible resulting in similar profiles and sheet resistances on planar and textured surfaces.

For solar cells not only profile and sheet resistance of emitters, but also the electrical quality of the passivated emitter is relevant. The electrical quality in terms of the emitter saturation current density $J_{0e}$ of the RVD emitters passivated by Al$_2$O$_3$ layers as well as the respective sheet resistances are given in Table I. For comparison, the $J_{0e}$ of a BBr$_3$ emitter with a similar profile as the RVD emitter in the top wafer part [see black squares and red stars in Fig. 3(a)] is determined. Although all $J_{0e}$ values are very similar considering the uncertainty there are small trends. The gradient in sheet resistance leads to $J_{0e}$ values depending on the position on the wafer. The best $J_{0e}$ value of 21 fA cm$^{-2}$ is obtained in the bottom rear quarter of the planar wafer where the sheet resistance is highest. The increased diffusion in the upper front region is as expected accompanied with an increased $J_{0e}$ of 28 fA cm$^{-2}$. The larger surface area of the textured samples leads to an increase of the $J_{0e}$ value if same sample areas are compared.

Although there are slight differences, within the given errors all $J_{0e}$ values of the RVD emitters are in accordance with the value of the reference BBr$_3$ emitter. Therefore, no difference caused by the front side for devices with RVD emitters and BBr$_3$ emitters is expected at least for the upper part of the wafers where emitter profiles are similar.

### Table II

| Oxide thickness (nm) | Annealing condition | $J_{0e}$ at 25 °C (fA cm$^{-2}$) | Contact resistivity $\rho_c$ (mΩ cm$^2$) |
|----------------------|---------------------|-------------------------------|--------------------------------------|
| TO1* 1.2$^{[21]}$    | 900 °C, 10 min, N$_2$| 0.5 ± 0.2                     | 4.2 ± 0.1,4$^{[22]}$                 |
| TO2* 1.49 ± 0.03     | 950 °C, 30 min, H$_2$| 2.8 ± 1.0                     | Not measured                         |
| TO2 1.49 ± 0.03      | 950 °C, 30 min, N$_2$| 0.2 ± 0.2                     | 5 ± 2                               |
| TO3 1.54 ± 0.03      | 950 °C, 30 min, N$_2$| 0.8 ± 0.4                     | 111 ± 34                            |
| TO4 1.92 ± 0.02      | 950 °C, 30 min, N$_2$| 2.1 ± 0.8                     | 11265 ± 342                         |

B. Tunnel Oxide Passivated Contact and Annealing

For the simultaneous emitter diffusion and TOPCon annealing during the RVD process, the TOPCon process has to be adapted to withstand the increased thermal budget of the RVD process compared to standard annealing conditions. As described in Section II-B, TOPCon layers with ultra-thin thermally grown SiO$_x$ layers of different thicknesses were exposed to annealing conditions similar to those of the RVD process. Resulting saturation current densities $J_e$ after hydrogenation and contact resistivities $\rho_c$ are given in Table II. For comparison, 1.2 nm thick oxide TO1 is included which is optimized for the standard annealing conditions (900 °C, 10 min, N$_2$) as used for the reference sequentially processed BBr$_3$ cells described in Section III-C. n-type TOPCon contacts featuring TO1 reveal a very low saturation current density of 0.5 fA cm$^{-2}$. Previous studies showed that the passivation quality of TOPCon layers with this oxide degrades drastically for annealing temperatures of ≥950 °C due to enhanced pinhole formation and

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Fig. 3. (a) Boron emitter profiles obtained with the RVD process at 950 °C for 30 min and with the BBr$_3$ reference process at 890 °C for 60 min (taken from Richter et al. [21]) measured by ECV. On RVD samples profiles are measured on planar (p) and textured (t) surfaces and on top (u) and bottom (b) part of the planar sample with respect to the position in the RTCVD160 furnace. (b) Map of the sheet resistance $R_{SH}$ of the textured 4 inch sample measured by four-point probing.
dopant diffusion into the c-Si wafer. However, thicker and more stoichiometric interfacial oxides are a more effective diffusion barrier and therefore enhances the thermal stability of TOPCon structures [22]. The thermal oxide layers exposed to 950 °C processes (TO2 – TO4) therefore have increased thicknesses and stoichiometry.

Looking at the samples annealed at 950 °C in the same N2 atmosphere as the reference TO1, the \( J_0 \) values are still very low. The thinnest oxide TO2 has the lowest \( J_0 \) value with 0.2 fA cm\(^2\), which is even better than that of the reference TO1.

The inhomogeneity of the RVD sample is similar to that of the standard TOPCon layer TO1 annealed separately at 900 °C for 10 min in N2 as described in Section II-C. Resulting \( J_0 \) parameters of the best performance cell per variation as well as the average values of the seven fabricated cells per variation (resulting from in-house measurements) are given in Table III.

| \( J_0 \) Values for the Best PV and Reference Cells | \( V_{OC} \) | \( J_{SC} \) | \( FF \) | \( \eta \) |
|---|---|---|---|---|
| (mV) | (mA cm\(^2\)) | (%) | (%) |
| Ref, best\(^a\) | 685 | 41.5 | 81.6 | 23.1 |
| Ref, mean | 674 ± 4 | 41.3 ± 0.1 | 81.0 ± 0.4 | 22.6 ± 0.3 |
| RVD, best\(^b\) | 685 | 41.5 | 81.9 | 23.3 |
| RVD, mean | 678 ± 4 | 41.2 ± 0.1 | 80 ± 2 | 22.4 ± 0.6 |

C. Solar Cells

Finally, \( n \)-type TOPCon solar cells have been fabricated using the simultaneous emitter diffusion via RVD and TOPCon annealing as described in Section II-C. These cells are compared to reference (Ref) cells fabricated sequentially using BBBr3 diffusion for emitter formation with the profile shown in Fig. 3(a) and the standard TOPCon layer TO1 annealed separately at 900 °C to reference (Ref) cells fabricated sequentially using BBBr3 reference cell. This results in a quite high confirmed efficiency \( \eta \) of 23.3% which is even slightly higher than that of the reference with 23.1%. This result is expected from the results described in Sections III-A and 3.B as the best RVD cell has a similar emitter profile as the reference [top position of the wafer, see Fig. 3(a) and(b)]. Besides best cell parameters mean values are given for the seven cells on the corresponding wafers using in-house \( I–V \) measurements. The stated errors are standard deviations of the mean values indicating the homogeneity of the parameters over the wafer. Although confirmed and in-house measurements lead to slightly different parameters, references and RVD cells can be compared for both measurements. Again, reference and RVD cells have comparable results considering the uncertainties.

The inhomogeneity of the RVD sample is similar to that of the reference sample in terms of the standard deviation for most mean values given in Table III. However, there is a clear trend of the efficiency distribution within the wafer. In Fig. 5 the
i Voc image of the RVD wafer with the seven cells is shown and corresponding FF values are stated.

Best efficiencies are obtained for upper and worst for lower cells. While Voc and Jsc values are randomly distributed on the wafer there is a reduction of the FF from 81.4% in average for top to 77.8% for bottom two cells. To determine the reason for this reduction PFF were determined as the difference PFF – FF is related to series resistance Rs [24]. This difference PFF – FF increases from 1.9% for top to 4.9% for bottom cells indicating an increase of Rs for the bottom cells. This increased Rs is most probably caused by the increased sheet resistance Rsh measured in the bottom area [see Table I and Fig. 3(b)] and/or an increased contact resistivity ρc on the front side. The sheet resistance additionally varies between left and right part of the wafer leading to a further reduction of the FF of the bottom-left compared to the bottom-right cell. The bottom-left cell simultaneously has the lowest Voc which might be partly caused by a higher contact recombination due to the weaker doping profile but is most probably also influenced by local bulk contamination.

Compared to previous results with homogeneous RVD emitters [9] the short circuit current Jsc is increased as the process temperature is lowered, and reflection properties are not affected by flattened pyramids. However, previous cells had a higher open circuit voltage Voc of 703 mV and a FF of 82.8%. One significant difference is the emitter profile. Although the previously used temperature was higher (1030°C instead of 950°C) the surface concentration was significantly lower. This is most probably caused by the autodoping effect in the reactor. Directly before previous RVD processes for cells only very few diffusion processes were conducted resulting in a minor autodoping effect. First experiments with ex situ drive-in steps already showed very promising properties of resulting emitter and TOPCon layers adopted to the increased thermal budget [25].

Even better cell parameters are expected for a driven-in emitter with the additional advantage that the drive-in step can be done in situ in the same process as the diffusion and the TOPCon annealing simply by switching of the boron source (B2H6). However, this requires an optimized furnace design in which autodoping effects are avoided. First experiments with ex situ drive-in steps already showed very promising properties of resulting emitter and TOPCon layers adopted to the increased thermal budget [25].

IV. Conclusion

In this article, the alternative emitter formation process RVD on the front side of wafer is combined with the annealing of TOPCon layers on the rear side in order to simplify the fabrication process and to reduce the CO2 footprint of the TOPCon solar cell. The applied RVD process resulted in low emitter saturation current densities between 21 and 28 fA cm\(^{-2}\) on planar and down to 26 fA cm\(^{-2}\) on textured surface for emitters with sheet resistances between 100 and 200 Ω sq\(^{-1}\).

In a second step, the TOPCon layer is adapted to withstand the high thermal budget of the RVD process by varying the thermal interface oxide. Optimized TOPCon layers reached a saturation current density of 0.2 fA cm\(^{-2}\) and a contact resistivity of 5 mΩ cm\(^{-2}\) after annealing in N2.

Finally, the combination of TOPCon annealing and emitter diffusion during the RVD process is applied to solar cells. With a confirmed efficiency up to 23.3% the RVD cells reached even slightly better results than reference cells with BBr\(_3\) emitters and subsequent TOPCon deposition and annealing. However, there is still a gradient of the diffusion over the wafer surface leading to a gradient in sheet resistance, emitter saturation current density and FF of final solar cells.

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