TCAD and SPICE Models for Account of Radiation Effects in Nanoscale MOSFET Structures

K. O. Petrosyants¹,², D. A. Popov³, M. R. Ismail-Zade⁴, L. M. Sambursky¹,², B. Li³, Y. C. Wang³

¹National Research University Higher School of Economics
(Moscow Institute of Electronics and Mathematics), Moscow, Russia, kpetrosyants@hse.ru
²Institute for Design Problems in Microelectronics of Russian Academy of Sciences, Moscow, Russia
³Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China

Abstract — Two types of the MOSFET models available in commercial versions of TCAD and SPICE simulators are completed with additional equations taking into account radiation effects. The adequacy of the models is demonstrated on two examples 1) 0.2 um and 0.24 um SOI/DSOI MOSFETs considering TID effects and single heavy ion impact, and 2) 28 nm bulk MOSFET, 45 nm and 28 nm high-k gate SOI MOSFETs considering TID effects.

Keywords — decananometer MOSFETs, DSOI, TCAD, SPICE, total ionizing dose, single event upset.

I. INTRODUCTION

Deep submicron and nanometer FD SOI MOSFET- and FinFET-based CMOS technologies are becoming more widespread for several reasons (see e.g. 0, 0): 1) they allow to provide greater radiation hardness to certain types of radiation effects; 2) they allow to reduce the statistical variation of parameters and characteristics due to random dopant fluctuations (RDF). Multi-finger transistors are increasingly used in electronic circuits, which allow better control of short- and narrow-channel effects.

The behavior of FinFETs and, in particular, their radiation hardness significantly depends on the specific transistor body and gate configuration (triple-gate 0, II-gate 0, Ω-gate 0), and also on the width of a single finger 0.

A. Total Ionization Dose Effects

The behavior of FinFETs with wide fingers, both on an insulating substrate and on bulk silicon subjected to stationary radiation exposure, corresponds to conventional planar transistors.

In the presence of dose effects, the structure of such a transistor during modeling is traditionally approximated as a combination of three almost independent MOS structures with a 2-dimensional channel approximation: front (front gate), sidewall (shallow trench isolation) and bottom (buried oxide – for the case of SOI MOSFET) 0.

Many sources confirm (see e.g. 0–0) that in SOI FinFETs with narrow fingers, dose effects practically do not appear in typical space conditions, even with a dose of several megarads, regardless of the electrical regime during irradiation. In FinFETs on bulk silicon with decreasing finger widths, resistance to dose effects is reduced (see e.g. 0); the main dose effects are the effects associated with the accumulation of charge in the volume of relatively thick shallow trench isolation (STI) layer (N0) and at the interfaces between the STI and silicon (Nk). For both SOI and bulk FinFETs, the influence of typical methods of global or local mechanical stress introduction does not significantly affect dose effects manifestation 0.

B. Single Events

In nanometer MOSFETs with a small body volume, the radius of the particle’s track becomes comparable to the transistor’s body size (gate length, finger width). Therefore, the result of an ion strike significantly depends not only on traditional parameters: linear energy transfer (LET), particle fluence, but also on the angle of a particle incidence.

In addition, the effect significantly depends on the transistor structure and especially on the design of the gate stack (using different gate materials, high-k dielectrics) 0, in some cases, on the strike location 0, as well as on the orientation of the transistor with respect to the substrate crystallographic orientation 0.

The most common effects are single-event gate rupture (SEGR) 0, soft breakdown 0, radiation-induced leakage current (RILC) 0, microdose effects 0, long-term reliability degradation 0.

In our previous works, the universal methodology of taking into account the radiation effects in submicron MOSFET models available in commercial versions of TCAD 0 and SPICE 0. The special analytical functions were introduced into the standard TCAD and SPICE models in order to implement radiation dependence of model parameters. In this work this methodology was extended to the deep submicron and nanometer devices.

II. TCAD-RAD SUBSYSTEM

In this work, the universal TCAD-RAD subsystem 0 (see Fig. 1) is used to simulate the characteristics of deep submicron and nanometer MOSFET structure. It consists of two parts: the standard Sentaurus Synopsys software core 0 and the special library of radiation models for physical parameters and electrical characteristics of MOSFET structures taking into account neutron, gamma-rays and proton irradiation.

DOI: 10.31114/2078-7707-2020-4-2-8
Gamma radiation models are based on ionization effects. The adequate models of radiation-dependent parameters ($N_{ox}$, $N_{it}$, $S_0$, $\mu$) for novel deep submicron MOSFETs and nanometer MOSFETs with high-k gate oxide structures are implemented in Sentaurus Synopsys TCAD.

Neutron models are based on displacement effects. The adequate models of radiation-dependent parameters ($\tau$, $\mu$, n/p) are included.

Proton model is based on additive approach combined the ionization and displacement effects influence on device structure.

A. Double SOI MOSFET

The Double SOI (DSOI) structure is an experimental SOI structure with an additional silicon layer (SOI2) in the buried oxide (see Fig. 2). This kind of structure provides higher radiation hardness for total ionization dose (TID) 0 and single-event upset (SEU) 0 effects. In our colleagues calibrated the TCAD model for 0.2 um DSOI structure. $I_D-V_G$ characteristics for the DSOI structure with gate length 1 um and width 8 um were simulated before and after irradiation up to 1000 krad. The simulation results are in agreement with the measured experimental data on the order of magnitude (see Fig. 3).

In the following example, SEU sensitivity was considered for the 0.24 um temperature hardened CMOS technology with three different configurations of buried oxide: the bulk structure, the traditional SOI and the SOI with additional silicon layer (DSOI). TCAD-SPICE simulation of a SRAM cell based on these configurations was carried out.

For the three structures, simulation of the Argon ion strike at nine points was done: in the left source edge (1), in the middle of the source (2), in the source near the junction (3), in the source junction (4), in the middle of the gate (5), in the drain junction (6), in the drain near the junction (7), in the middle of the drain (8), in the right drain edge (9). The
LET of ion was 10.78 MeV·cm²/mg, the track radius was 0.02 μm and the length was 4 μm. Three discrete values of external temperature were considered for every combination of the structure and strike point: 300 K (room temperature), 423, 573 K.

The general result of SEU simulation is the following: at elevated temperature, the SEU sensitivity area increases (see Fig. 4,a–c). Here are the details:

- **for bulk configuration** (Fig. 4 a), upset occurs at room temperature in case when an ion strikes into drain or gate regions (points 4–9), while at temperatures above the room temperature, the cross-sectional area expands to the source (points 2, 3).

- **for SOI and DSOI configurations with zero bias applied to the SOI2 layer** ($V_{SOI2} = 0$) (Fig. 4 b), upset does not occur at room temperature but it can be observed after a strike into the drain junction (point 6) at 423 K and into the gate at 573 K (points 4, 5).

- **for DSOI configuration with large negative bias applied to the SOI2 layer** ($V_{SOI2} = −15$ V) (Fig. 4 c), upset does not occur at 300 and 423 K. Upset occurs only after a strike into the drain junction (point 6) and center of the gate (point 5) at 573 K.

As can be seen, the DSOI configuration with large negative bias applied to the SOI2 layer is the preferred variant with respect to the SEU sensitivity area, especially for the case of elevated external temperature.

**B. 45 nm MOSFET**

In conventional MOSFETs with nanometer thick (1–3 nm) gate oxide, the tunneling effect of high-energy carriers through this layer gives rise to the gate leakage current, which causes a substantial current loss and excessive heat dissipation. This effect is heavily suppressed in MOSFET structures with high-k gate oxide (see Fig. 5): the gate leakage current is eliminated and the electrical characteristics of the MOSFET are preserved.

Adequate modeling results of structures with high-k dielectric can only be obtained after choosing appropriate physical models. Firstly, the conventional drift-diffusion transport model cannot correctly describe the particles distribution in nanometer devices. In this case, the Hydrodynamic model was used. Secondly, the wave nature of electrons and holes can no longer be neglected. So the Density Gradient Quantization model was attached to the basic model. Thirdly, the physical effect of tunneling through a very thin oxide layer must be taken into account, therefore, Direct Tunneling model was used. Fourthly, the standard mobility model Enormol(Lombardi_high-k) for structures with high-k oxide was included.

Unfortunately, a very small number of publications are devoted to the experimental investigation of the radiation hardness of MOSFET structures with high-k gate oxide. Therefore, the calibration of our model was carried out 0 on the basis of experimental data for submicron MOSFETs with HfO₂ gate oxide. In 0 the I-V characteristics of 45 nm SOI

---

Fig. 4. Layout of MOSFET structures with the indication of ion strike points: a) bulk, b) SOI and DSOI with $V_{SOI2} = 0$ V, and c) DSOI with $V_{SOI2} = −15$ V, × transistor failure at 300 K, ⋄ at 423 K, ⋄ at 573 K, ○ no failure; d) drain voltage dependence on time after ion strike
MOSFET ($t_{SOX}=1.2$ nm) before and after gamma irradiation were measured. Noticeable degradation is observed only for radiation response of the backgate interface (see Fig. 6) with backgate voltage more than ~5 V.

![MOSFET structure with high-k gate insulator](image)

**Fig 5.** MOSFET structure with high-k gate insulator

![Measured (dash) 0 and simulated (line) $I_dV_g$ for 45 nm SOI MOSFET before and after gamma irradiation](image)

**Fig 6.** Measured (dash) 0 and simulated (line) $I_dV_g$ for 45 nm SOI MOSFET before and after gamma irradiation

Additionally, the influence of shallow trench isolation (STI) on the radiation-induced drain current change was investigated for 45 nm SOI MOSFET structure with high-k gate oxide ($t_{HIOX}=10$ nm) with account for gamma irradiation dose up to 1 Mrad. The noticeable effects on $I_d$-$V_g$ characteristic include the threshold voltage shift, mobility degradation, additional current hump in the subthreshold (Fig. 7).

![Simulated $I_dV_g$ characteristics for 45 nm high-k SOI MOSFET with $t_{HIOX}=10$ nm](image)

**Fig 7.** Simulated $I_dV_g$ characteristics for 45 nm high-k SOI MOSFET with $t_{HIOX}=10$ nm

III. 28 NM BULK MOSFET SPICE MODEL TAKING INTO ACCOUNT THE TID EFFECTS

A. Model Description

In this chapter, we present a compact SPICE model developed specifically for 28 nm bulk MOSFETs with account for total ionizing dose (TID) effects. The modified MOSFET compact SPICE model is based on the standard PSP model v103.1 (available in major SPICE-like simulators) that is described in terms of surface potential equations. This core model is better suited as a basis for a rad-hard model to cover the behavior of the present-day CMOS nanometer technology devices in extreme conditions without trading off accuracy for model continuity 0.

Measured $I_d$-$V_g$ curves demonstrate improved radiation tolerance in the open state, whereas the most evident effect in the irradiated bulk MOSFETs is the significant increase in the leakage current attributed to charge trapping in STI oxide. To characterize the mentioned effects, we involved several built-in model parameters that were assigned with dose-dependent saturated analytical functions.

The radiation-dependent model parameters of the PSP model are threshold voltage-related ($VFB$), carrier mobility-related ($BETN$, $MUE$, $THEMU$), subthreshold slope related ($CT$, $DPHB$), DIBL-effect related ($CF$), drain leakage current-related ($CJOSTI$).

Changes of all of the said parameters are dependent on total dose $D$ and are expressed in the form 0:

$$a_1 + a_2 \cdot \exp(-a_3 \cdot D),$$  

or in the form of a polynomial. In (1) $a_1$, $a_2$, $a_3$ are fitting factors related to ionization dose and electrical bias during irradiation. Fitting factors in these expressions constitute the set of static radiation parameters of the model.

B. Model Parameter Extraction Procedure

The model parameter extraction procedure with account for total dose effects is automated with industry extraction tool IC-CAP, which simplifies data exchange and processing.

The initial data are the sets of IV and CV-curves of standard semiconductor devices of different sizes, obtained as a result of measurements or process and device simulation for different values of total dose and transmitted to IC-CAP using an in-house software interface. The extraction procedure allows obtaining model parameters for intermediate total dose values and includes the following steps:

Step 1. Determination of the complete set of model parameters on the basis of measurement data for unirradiated devices. The method used to identify the parameters includes a combination of analytical and optimization procedures.

The analytical procedure includes the parameters calculation from measured data:

- to determine threshold voltage $V_{TH}$ and free carrier mobility $\mu$, $\sqrt{I_d-V_g}$ curves are extrapolated linearly at the maximum slope. The intercept at the $V_g$ axis is defined as $V_{TH}$. The slope of the linear extrapolation provides insights into $\mu$.

- DIBL-effect is calculated as $DIBL = -(V_{TH}^{high} - V_{TH}^{low})/(V_{DS}^{high} - V_{DS}^{low})$, where $V_{TH}^{high}$ and $V_{TH}^{low}$ are the
threshold voltage extracted at a high $V_{DS}^{\text{max}}$ and low $V_{GS}^{\text{low}}$ drain voltage.

- the on-current ($I_{D,\text{on}}$) is defined at $|V_{GS}|=V_{GS}^{\text{max}}$, and the off-current ($I_{D,\text{off}}$) at $V_{GS}=0$.

Step 2. From the complete set of model parameters, a list of the main radiation-dependent parameters is selected: $V_{FB}$, $BETN$, $CF$ and $CJOSTI$.

Step 3. For each total dose value from the list of discrete values, the corresponding values of the selected parameters (for threshold voltage, carrier mobility, etc.) are determined based on the measurement results. This procedure is repeated for all planned discrete total dose values $D_i$: $i = 1 \ldots n$.

Step 4. The radiation dependencies of the model parameters obtained in step 3 are approximated by analytical functions of the form (1). The coefficients of this function constitute a set of radiation parameters of the entire model. Precise adjustment of the values of the radiation parameters is made using global optimization, i.e. for all available experimental characteristics.

Step 5. The resulting analytical expressions together with the coefficients are built into the description of the MOSFET SPICE model, that is further included in the library of models.

C. Model Verification

As an example for MOSFET modeling with account for total dose effects, the PSP-based model parameters were identified for a 28 nm bulk CMOS $n$-MOSFET with $W/L = 3 \mu m/30 nm$ irradiated up to 1000 Mrad (SiO2) with steps of 0, 10, 50, 140, 340, 540, 940, and 1000 Mrad at a dose rate of 8.82 Mrad/(SiO2) 0. The structure parameters are: $L = 7 \mu m$, $t_{BOX} = 25 nm$, $t_{ox} = 1.55 nm$; the gate stack is HKMG (high-k metal gate). Fig. 8 shows measured and simulated transfer characteristics up to 1000 Mrad. Approximation of MOSFET model parameters ($V_{TO}$, $\mu$, DIBL, parameter, subthreshold slope, $I_{D,\text{leak}}$) versus TID is shown in Fig. 9; degradation of mobility is less than 4% and is not shown. The maximum modeling error is not more than 10%.

The next example demonstrates the capabilities of PSP-based model in application to the 28 nm FDSOI technology. In Fig. 10 the measured 0 and simulated transfer characteristics of unirradiated FDSOI $n$-MOSFETs with $W/L = 1 \mu m/28 nm$ fabricated by the STMicroelectronics manufacturer are shown.

IV. Conclusion

The universal approach was used to take into account radiation effects in the nanometer MOSFET models built into TCAD and SPICE simulators.

The special analytical functions were introduced into the TCAD-RAD software version to describe the dependence of the device structure electrical physical parameters $\mu$, $\tau$, $N_{\text{ac}}$, $N_0$, $S_0$, etc. on radiation dose/fluence. The approximation coefficients for these analytical functions were defined from the physical experiments and/or extracted from measured IV-characteristics after device irradiation.

The same approach was used to take into account radiation effects in the compact SPICE MOSFET models for circuit simulation. The basic device electrical parameters $V_{TO}$, $\mu_{eff}$, $SS$, etc. were assigned with radiation dose/fluence-dependent functions. The approximation coefficients of these dependences were extracted from the experimental IV-characteristics obtained after device irradiation and included in the device compact SPICE-RAD model descriptions.
The adequacy of the developed TCAD and SPICE MOSFET radiation models was illustrated by several practical examples with reasonable accuracy.

**SUPPORT**

The reported study was funded by The Russian Foundation for Basic Research (grant No. 18-07-00898), and The Russian Foundation for Basic Research and National Natural Science Foundation of China (grant No. 20-57-53004).

**REFERENCES**

[1] Fleetwood D. M. Evolution of total ionizing dose effects in MOS devices with Moore's law scaling // IEEE Transactions on Nuclear Science. – 2017. – Vol. 65. – №. 8. – P. 1465-1481

[2] Simoen E., et al. Radiation effects in advanced multiple gate and silicon-on-insulator transistors // IEEE Transactions on Nuclear Science. – 2013. – Vol. 60. – №. 3. – P. 1970-1991

[3] Song J.-J., et al. Fin width and bias dependence of the response of triple-gate MOSFETs to total dose irradiation // IEEE Trans. Nucl. Sci., vol. 58, no. 6, Dec. 2011, P. 2871–2875.

[4] Colinge J. P., et al. Radiation dose effects in trigate SOI MOS transistors // IEEE Trans. Nucl. Sci., vol. 53, no. 6, Dec. 2006, P. 3237–3241.

[5] Gaillardin M., et al. High tolerance to total ionizing dose of Ω-shaped gate field effect transistors // Appl. Phys. Lett., vol. 88, no. 22, Nov. 2006, P. 223511/1–223511/3.

[6] Gaillardin M., et al. Total ionizing dose effects on triple-gate FETs // IEEE Trans. Nucl. Sci., vol. 53, no. 6, Dec. 2006, P. 3158–3165.

[7] Petrosyants K. O., et al. SOI/SOS MOSFET universal compact SPICE model with account for radiation effects // EUROSOI-ULIS 2015: 2015 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon. – IEEE, 2015. – P. 305-308.

[8] Put S., et al. Influence of fin width on the total dose behavior of p-channel bulkMUGFETs // IEEE Electron Dev. Lett., vol. 31, no. 3, Mar. 2010, P. 243–245.

[9] Kobayashi D., et al. Proton-induced mobility degradation in FinFETs with stressor layers and strained SOI substrates // IEEE Trans. Nucl. Sci., vol. 58, no. 3, Jun. 2011, P. 800-807.

[10] Sexton F. W. Destructive single-event effects in semiconductor devices and ICs // IEEE Trans. Nucl. Sci., vol. 50, no. 3, Jun. 2003, P. 603–621.

[11] Ceschina M., et al. Heavy ion irradiation of thin oxides // IEEE Trans. Nucl. Sci., vol. 47, no. 6, Dec. 2000, P. 2648-2655.

[12] Scarpa A., et al. Ionizing radiation induced leakage current on ultrathin gate oxides // IEEE Trans. Nucl. Sci., vol. 44, no. 6, Dec. 1997, P. 1818–1825.

[13] Griffoni A., et al. Microdose and breakdown effects induced by heavy ions on sub-32 nm triple-gate SOI FETs // IEEE Trans. Nucl. Sci., vol. 55, no. 6, Dec. 2008, P. 3182–3188.

[14] Choi B. K., et al. Long-term reliability degradation of ultrathin dielectric films due to heavy-ion irradiation // IEEE Trans. Nucl. Sci., vol. 49, no. 6, Dec. 2002, P. 3045-3050.

[15] Griffoni A., et al. Effects of heavy-ion strikes on fully depleted SOI MOSFETs with ultra-thin gate oxide and different strain-inducing techniques // IEEE Trans. Nucl. Sci., vol. 54, no. 6, Dec. 2007, P. 2257–2263.

[16] Griffoni A., et al. A statistical approach to microdose induced degradation in FinFET devices // IEEE Trans. Nucl. Sci., vol. 56, no. 6, Dec. 2009, P. 3285-3292.

[17] Sun Y., et al. Physics of strain effects in semiconductors and metal-oxide-semiconductor field-effect transistors // J. Appl. Phys., vol. 101, no. 10, May 2007, P. 104503-1–104503-22.

[18] Petrosyants K. O. et al., Effective Radiation Damage Models for TCAD Simulation of Silicon Bipolar and MOS Transistor and Sensor Structures // Sensors and Transducers. 2018. Vol. 227. No. 11. P. 42-50.

[19] Petrosyants K. O. et al., Radiation-Induced Fault Simulation of SOI/SOS CMOS LSI’s Using Universal Rad-SPICE MOSFET Model // Journal of Electronic Testing, 33(1), 2017, P. 37-51.

[20] TCAD Sentaurus User Manual J-2014.09, Synopsys.

[21] Petrosyants K. O. et al., 45nm High-k MOSFETs on Bulk Silicon and SOI Substrates Modeling to Account for Total Dose Effects // in Proc. of in Proc. of 2017 IWRMN-EDHE 2017, P. 1-3.

[22] Huang Y. et al., An Effective Method to Compensate Total Ionizing Dose Induced Degradation on Double-SOI Structure // IEEE Transactions on Nuclear Science, Vol. 65, No. 8, August 2018, P. 1-8.

[23] Gao J. T. et al. // Back gate impact on SEU Characterization of a Double SOI 4k-bit SRAM //2018 IEEE Nuclear and Space Radiation Effects Conference (NSREC 2018), Hawaii, US, July, 16-20, 2018.

[24] Huang Y. et al. TCAD Simulation of Total Ionizing Dose Response on DSOI nMOSFET // 2019 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), Grenoble, France, 2019, P. 1-5.

[25] Petrosyants K. O. et al., Electrical characterization and reliability of submicron SOI CMOS technology in the extended temperature range (to 300°C) // Microelectronics and Reliability, 2017, Vol. 79, P. 416-425.

[26] Petrosyants K. O. et al., TCAD Simulation of Dose Radiation Effects in Sub-100 nm High-k MOSFET Structures // Russian Microelectronics. 2018. Vol. 47. No. 7. P. 487-493.

[27] Liu S. T., et al. Total dose radiation response of a 45nm SOI Technology // Proc of SOI Conf. (San Diego, USA), 2010, P. 1-2.

[28] Li X., et al. PSP 103.1 // PSP model is a joint development of Arizona, Univ. NXP Semicond. Res., Phoenix, AZ, USA, Tech. Note NXP-R-TN-2008/00299, Apr. 2009.

[29] Zhang C.-M., et al., GigaRad total ionizing dose and post-irradiation effects on 28 nm bulk MOSFETs // in Proc. IEEE Nucl. Sci. Symp. Conf. Rec., Nov. 2016, P. N43-N48.

[30] Beckers A. et al. Characterization and modeling of 28-nm FD-SOI CMOS technology down to cryogenic temperatures // Solid-State Electronics, 159, 2019, P. 106-115.
TCAD и SPICE-модели для описания радиационных эффектов в наноразмерных МОП-транзисторных структурах

К.О. Петросяниц, Д.А. Попов, М.Р. Исмаил-Заде, Л.М. Самбурик, Б. Ли, Ю. Ванг

1 Национально-исследовательский университет «Высшая школа экономики» (Московский институт электроники и математики), г. Москва, Россия, kpetrosyants@hse.ru
2 Институт проблем проектирования в микроэлектронике РАН, г. Москва, Россия
3 Институт микроэлектроники Китайской академии наук, г. Пекин, Китай

Аннотация — Два типа моделей МОПТ, имеющихся в коммерческих версиях TCAD и SPICE-симуляторов, дополняют уравнениями для учёта радиационных эффектов. Адекватность моделей иллюстрирована на двух примерах: 1) 0,2- и 0,24-мм КНИ/DSOI МОПТ с учётом дозовых эффектов и ОИЧ; 2) 28-нм МОПТ на объёмном кремнии, 45-нм и 28-нм КНИ МОПТ с high-k диэлектриком с учётом дозовых эффектов.

Ключевые слова — 45-нм МОПТ, 28-нм МОПТ, DSOI, TCAD, SPICE, поглощенная доза, однонаправленные сбои.

Литература
[1] Fleetwood D. M. Evolution of total ionizing dose effects in MOS devices with Moore’s law scaling // IEEE Transactions on Nuclear Science. – 2017. – Vol. 65, no. 8. – P. 1465-1481
[2] Simoen E., et al. Radiation effects in advanced multiple gate and silicon-on-insulator transistors // IEEE Transactions on Nuclear Science. – 2013. – Vol. 60, no. 3. – P. 1970-1991
[3] Song J.-J., et al. Fin width and bias dependence of the response of triple-gate MOSFETs to total dose irradiation // IEEE Trans. Nucl. Sci., vol. 58, no. 6, Dec. 2011, P. 2871–2875.
[4] Colinge J. P., et al. Radiation dose effects in trigate SOI MOS transistors // IEEE Trans. Nucl. Sci., vol. 53, no. 6, Dec. 2006, P. 3237–3241.
[5] Gaillardin M., et al. High tolerance to total ionizing dose of Ω-shaped gate field effect transistors // Appl. Phys. Lett., vol. 89, no. 22, Nov. 2006, P. 223511/1–223511/3.
[6] Gaillardin M., et al. Total ionizing dose effects on triple-gate FETs // IEEE Trans. Nucl. Sci., vol. 53, no. 6, Dec. 2006, P. 3158–3165.
[7] Petrosyants K. O., et al. SOI/SOS MOSFET universal compact SPICE model with account for radiation effects // EUROSOI-ULIS 2015: 2015 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon. – IEEE. – 2015. – P. 305-308.
[8] Put S., et al. Influence of fin width on the total dose behavior of p-channel bulkMOSFETs // IEEE Electron Dev. Lett., vol. 31, no. 3, Mar. 2010, P. 243–245.
[9] Kobayashi D., et al. Proton-induced mobility degradation in FinFETs with stressor layers and strained SOI substrates // IEEE Trans. Nucl. Sci., vol. 58, no. 3, Jun. 2011, P. 800–807.
[10] Sexton F. W. Destructive single-event effects in semiconductor devices and ICs // IEEE Trans. Nucl. Sci., vol. 50, no. 3, Jun. 2003, P. 603–621.
[11] Ceschia M., et al. Heavy ion irradiation of thin oxides // IEEE Trans. Nucl. Sci., vol. 47, no. 6, Dec. 2000, P. 2648-2655.
[12] Scarpa A., et al. Ionizing radiation induced leakage current on ultrathin gate oxides // IEEE Trans. Nucl. Sci., vol. 44, no. 6, Dec. 1997, P. 1818–1825.
[13] Griffon F., et al Microdose and breakdown effects induced by heavy ions on sub 32-nm triple-gate SOI FETs // IEEE Trans. Nucl. Sci., vol. 55, no. 6, Dec. 2008, P. 3182–3188.
[14] Choi B. K., et al. Long-term reliability degradation of ultrathin dielectric films due to heavy-ion irradiation // IEEE Trans. Nucl. Sci., vol. 49, no. 6, Dec. 2002, P. 3045-3050.
[15] Griffon F., et al. Effects of heavy-ion strikes on fully depleted SOI MOSFETs with ultra-thin gate oxide and different strain-inducing techniques // IEEE Trans. Nucl. Sci., vol. 54, no. 6, Dec. 2007, P. 2257–2263.
[16] Griffon F., et al. A statistical approach to microdose induced degradation in FinFET devices // IEEE Trans. Nucl. Sci., vol. 56, no. 4, Dec. 2009, P. 3285-3292.
[17] Sun Y., et al. Physics of strain effects in semiconductors and metal-oxide-semiconductor field-effect transistors // Int. J. Appl., vol. 101, no. 10, May 2007, P. 104503–1–104503–22.
[18] Petrosyants K. O., et al. Effective Radiation Damage Models for TCAD Simulation of Silicon Bipolar and MOS Transistor and Sensor Structures // Sensors and Transducers, 2018. Vol. 227. No. 11. P. 42-50.
[19] Petrosyants K. O. et al., Radiation-Induced Fault Simulation of SOI/SOS CMOS LSI’s Using Universal Rad-SPICE MOSFET Model // Journal of Electronic Testing, 33(1), 2017, P. 37-51.
[20] TCAD Sentaurus User Manual J-2014.09. Synopsys.
[21] Petrosyants K. O. et al., 45nm High-k MOSFETs on Bulk Silicon and SOI Substrates Modeling to Account for Total Dose Effects // in Proc. of in Proc. of 2017 IWRMN-EDHE 2017. P. 1-3.
[22] Huang Y. et al., An Effective Method to Compensate Total Ionizing Dose Induced Degradation on Double-SOI Structure // IEEE Transactions on Nuclear Science, Vol. 65, No. 8, August 2018, P. 1-8.
[23] Gao J. T. et al. // Back gate impact on SEU Characterization of a Double SOI 4k-bit SRAM // 2018 IEEE Nuclear and Space Radiation Effects Conference (NSREC 2018), Hawaii, US, July. 16-20, 2018.
[24] Huang Y. et al., TCAD Simulation of Total Ionizing Dose Response on DSOI nMOSFET // 2019 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), Grenoble, France, 2019, P. 1-5.
[25] Petrosyants K. O., et al., Electrical characterization and reliability of submicron SOI CMOS technology in the extended temperature range (to 300°C) // Microelectronics and Reliability, 2017, Vol. 79, P. 416-425.
[26] Petrosyants K. O. et al., TCAD Simulation of Dose Radiation Effects in Sub-100 nm High-k MOSFET Structures // Russian Microelectronics. 2018. Vol. 47. No. 7. P. 487-493.
[27] Liu S. T., et al. Total dose radiation response of a 45nm SOI Technology // Proc of SOI Conf. (San Diego, USA), 2010, P. 1-2.
[28] Li X., et al. PSP 103.1 // PSP model is a joint development of Arizona, National University, NXP Semicond. Res., Phoenix, AZ, USA, Tech. Note NXP-RT-TN2008/0799, Apr. 2009.
[29] Zhang C.-M., et al. GigaRad total ionizing dose and post-irradiation effects on 28 nm bulk MOSFETs // in Proc. IEEE Nucl. Sci. Symp. Conf. Rec., Nov. 2016, P. N43-N48.
[30] Beckers A. et al. Characterization and modeling of 28-nm FDSOI CMOS technology down to cryogenic temperatures // Solid-State Electronics, 159, 2019, P. 106-115.