OVERVIEW AND STUDY OF THE 3D-TSV INTERCONNECTS INDUCED COUPLING IN CMOS CIRCUITS

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September 7, 2022

ABSTRACT

The semiconductor industry’s rapid advancement pushes conventional two-dimensional technology to its utmost limitations in terms of scaling, performance, and cost factors. These challenges drive the usage of 3D technology in the production of various Integrated Circuits. One of the numerous features of 3D Integration is the use of Through Silicon Vias (TSVs) for the assembly of multilayers into a single stack. This process, which was initially developed for memory chips, has been used afterward in many applications in other areas of microelectronics. The purpose of this research is to assess the effect of 3D-TSV interconnection on the performance of MOS transistors and CMOS circuits. This is accomplished using numerical and analytical models capable of describing the substrate coupling induced by TSV at the circuit level. The analytical approach proposed enables the study and optimization of the performance, not only of MOS devices but also large CMOS circuits with 3D interconnects as a function of various technological and electrical parameters.

Keywords 3D-TSV · Analytical model · CMOS circuits · MOS transistors · TCAD simulations

1 Introduction

The functionality of computational systems has increased dramatically in the microelectronics industry over the last few decades. Many advancements (like speed, power, and integration level) have been driven by semiconductor device scaling, which has increased the number of transistors on a single chip in accordance with Moore’s Law [Pendse 2014]. Furthermore, as the semiconductor industry has evolved, the concept of "More Moore" has incorporated a variety of functionalities in the same technological node, allowing for an increase in integration density [Lau 2011], [Rousseau 2009]. The "More than Moore" approach, on the other hand, has focused on functional diversification, presenting a new category of devices with heterogeneous functionalities that do not scale in the same technological node. As a result, over the last decade, conventional 2D technology has been shown to have some issues, particularly with the increase in demand for device and interconnects capabilities in terms of chip size, density, minimum metal pitch, and the number of metal layers. Because of all of these constraints, the development of an alternative technology for designing and building microelectronic systems, such as 3D integration, became critical.

3D integration technology, which was first used in memory chips, has since found its use in other domains of microelectronics, like image sensors and MEMS [Benkechkache et al. 2017, et al. 2020, 2016a,b,c]. The use of Through Silicon Vias (TSVs), which are regarded as the enabling technology for multilayer Integrated Circuits (ICs) assembled into a single package, is one of the various approaches to such technology [Sun et al. 2014]. The chip packaging with 3D-TSV technology has resulted in numerous benefits and advantages [Papanikolaou et al. 2010, Dukovic et al. 2010]. It enabled, in particular, to reduce power dissipation, the number of long interconnects, and their overall length, thereby increasing the speed and performance of MOS devices [Lu and Srivastava 2015]. However, this

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type of interconnects shows some undesirable effects on the performance of ICs nearby, like the substrate coupling effect or phenomena [Rousseau et al. 2009, et al. 2016d,e]. Such a parasitic effect has been studied experimentally and analytically in traditional 2D circuits [Shreeve et al. 2004, et al. 2000]. This effect has been investigated experimentally and analytically in conventional 2D circuits, however, in 3D-ICs it still has yet to be investigated. Some studies concentrated on TSV electrical characterization [et al. 2007, 2013], Kim and Jung [2009], stress Jung et al. [2014], or thermal [Okoro et al. 2013], but the TSVs-induced coupling on CMOS circuits was rarely investigated. Despite the fact that the effect of TSVs interconnects on MOS devices was thoroughly studied in Benkechkache et al. [2014, et al. 2008, 2011], the TSVs-induced coupling on complex CMOS circuits was not taken into account.

This paper is structured as follows: Section II will first evaluate the impact of 3D-TSV interconnects on MOS devices using a numerical approach as well as an analytical model utilized to describe an equivalent circuit capable of evaluating the 3D-TSV interconnects. The analytical model will then be used in sections III and IV to investigate the effect of 3D-TSV technology in CMOS circuits, specifically a CMOS inverter and an oscillator, with the goal of optimizing their performance in terms of various technological and electrical parameters. Section V summarizes the main findings.

2 3D-TSV influence on MOS devices

One of the major concerns of the presence of TSV interconnects nearby MOS components and CMOS circuits is the induced parasitic effects known as "the substrate coupling" which affects their electrical performance. Therefore, in order to study and evaluate such an impact, a numerical approach is considered by testing MOS components placed close to a via using TCAD simulations first. However, once considering evaluating the 3D-TSV technology on CMOS circuits, numerical simulations are time-consuming. To this purpose, we are going to define an analytical approach to study the parasitic substrate coupling induced by the via on the electrical behavior of CMOS circuits. The main objective of both numerical and analytical approaches considered is to reduce the substrate coupling induced by the presence of this kind of vertical interconnections on electronic devices in 3D technology.

2.1 Numerical model

To study the impact of TSV interconnections on the performance of MOS devices, a numerical model is used in this case.

2.1.1 Device description and analysis method

The analysis method conducted is based on numerical simulations carried out using the Sentaurus-TCAD tool. A simplified two-dimensional structure of a MOS transistor placed next to a TSV was considered as demonstrated in Figure 1. However, since the dimensions of the TSV are much larger than those of the MOS transistor, the meshing of the assembly is difficult due to the limited number of mesh nodes. Therefore, the TSV is considered as a perfect conductor and is represented on the structure as an electrode applied on the entire left vertical boundary of the structure.

The study of the substrate coupling induced by the via was carried out with a transient simulation in order to evaluate the variations in the electrical characteristics of the MOS components. Therefore, it is important initially to put the MOS transistor used in a saturation regime \( V_{GS} = V_{DS} = 1.5 \text{ V} \), then apply a parasitic potential on the TSV with a square signal of \( f = 200 \text{ MHz} \) frequency and a maximum amplitude of 1.2 V. The induced variation in the drain current as a function of different technological and electrical parameters will be investigated. Figure 2-a shows the potential lines propagating in the silicon substrate when applying a voltage on the via nearby.

The influence of the induced coupling by the TSV on the electrical performance of the MOS transistor results in a significant variation observed in the drain current, as shown in Figure 2-b. These variations follow a capacitive behavior where each rising or falling edge of the potential applied to the TSV, a charging and a discharging phenomenon is noted in the behavior of the drain current. This methodology is applied to all the simulations described here. The objective of this approach is to test different geometries and configurations of the 3D architecture.

2.1.2 Parameter optimization

The optimization of different parameters concerning the substrate thickness, the separation distance from the TSV, the rising/falling time of signal applied to the TSV, and the insulation thickness of the via was performed using TCAD simulations.

- **Substrate thickness:** The thickness of the substrate, or in other words the length of the TSV, is one of the most important technological parameters with regard to 3D integration. This parameter directly imposes
the diameter of the vias according to the conditions of the possible form factors for the TSVs. In our case study, we have considered a range of values that corresponds to the real technological process considered for high-density 3D integration [8]. This range varies from 5 $\mu$m up to 20 $\mu$m thickness. This limiting value is imposed by the large number of meshes that would then be necessary. By considering the same transient study presented previously, the variations observed in the drain current of the MOS transistor are noted and presented in Figure 3. This MOS transistor is placed at a distance of 6 $\mu$m from the TSV. The impact of the oxide thickness of the TSV, $T_{ox,TSV}$, is also investigated. A minimum thickness of 0.05 $\mu$m was considered. It cannot be reduced further for technological reasons since too a thin layer could create insulation problems. A maximum thickness investigated was not considered beyond 0.5 $\mu$m since the oxide thickness of the TSV should not be much thicker, for technological recommendations, in order to avoid the increase in the diameter of the TSV. In the range of $T_{SUB}$ values considered, the thickness of the TSV insulation oxide also has a significant influence on nearby devices, hence the increase of such a parameter serves to reduce the coupling of the substrate.

- **The distance from the TSV:** The separation distance of the TSV from the MOS transistor is an important design parameter, its influence is modeled for a range of distances that varies from 2 to 10 $\mu$m. These distances are maintained in this range of values which are not less than 2 $\mu$m, in order to take into account the constraint.
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Figure 3: The overshoots observed on the drain current of the transistor versus the thickness of the substrate.

Figure 4: The overshoots observed on the drain current of the transistor versus the clearance distance from the via.

- The TSV signal rising/falling time: One of the electrical parameters investigated here is the rising and falling time of the signal applied to the TSV, $t_{rf}$. In this study, the MOS transistor is placed close to the TSV with a 6 µm separation distance and a substrate thickness of 10 µm. Two values of oxide thickness of the TSV are considered in this case, with a minimum value of 0.05 µm and an average thickness of 0.25 µm. The study of the influence of this $t_{rf}$ parameter on the electrical characteristics of MOS components is done considering a range of values from 20 to 300 ps. The variations observed in the drain current of the MOS transistor as a function of this parameter are described in Figure 5. One can note in this figure the influence of the rising/falling time of the signal applied to the TSV on the intensity of the coupling, it appears clearly that the short times generate a more consequent coupling compared to longer times.
2.2 Analytical model

When the accuracy of physics-based results is essential, numerical simulations would be the best solution to study the impact of 3D-TSV interconnects on the characteristics of CMOS ICs. However, when dealing with large circuits, the simulation is expected to take a long time. In this case, a SPICE-like circuit simulation is a viable option for obtaining quasi-instantaneous results [Jankovic and Pesic-Brdjanin, 2015]. This simulation requires the development of an analytical model which defines each element in the equivalent circuit to be investigated.

2.2.1 Device and analysis description

This analytical model is defined in detail here showing the impact of TSVs on MOS transistors, which will be useful to extend the work to see its influence on CMOS circuits. The equivalent circuit is made up of a set of capacitors and resistors for the substrate and a set of MOS capacitors representing the via’s insulation layer (an oxide layer). MOS transistors, on the other hand, will be modeled using a compact model (BSIM4).

- **Substrate network:**

  Silicon possesses dielectric and conductive properties, which can be translated into a capacitive and resistive effect, respectively. Therefore, the silicon substrate could be viewed and modeled whether as a purely resistive or capacitive and resistive network depending on the frequency used. Eq. 1 defines this crossover frequency $f_T$ as [Ali et al., 2010]:

  \[
  f_T = \frac{1}{2\pi T_s} = \frac{q(\mu_n + n\mu_p)}{2\pi \epsilon_0 \epsilon_{si}}
  \]  

  With $T_s$ the substrate dielectric relaxation time, $q$ the electron charge, $\mu_n$ and $\mu_p$ stand for the electron and hole mobilities, respectively, and $n$ and $p$ are the carrier densities, and $\epsilon_{si}$ the silicon permittivity.

  Therefore, the equivalent circuit proposed describing the coupling through the substrate is made up of two main vertical ($R_{ver}$ and $C_{ver}$) and lateral ($R_{Lateral}$ and $C_{Lateral}$) components as shown in Figure 6-a. These components present the substrate resistance and capacitance between the device’s contacts and the TSV outer edge contact at a specific distance, $D_{TSV}$. Since this model is going to be validated later on using a linear geometry with a 2D-TCAD simulation, the cross-sectional area is set by default as $1 \mu m$ so that a square geometry is considered in this case. The expressions of equivalent resistances and capacitances for evaluating the parasitic coupling in the silicon substrate could be found in the literature as [Ali et al., 2010], [Raskin et al., 1997]:

  \[
  R_{ver} = K_1 \frac{\sigma_{si} S_{pad}}{T_{sub}}
  \]  

  \[
  C_{ver} = K_1 \frac{\epsilon_0 \epsilon_{si} S_{pad}}{T_{sub}}
  \]
$R_{\text{Lateral}} = \left[ K_2 \frac{\pi \sigma_{\text{s}_i}}{4ln\left(\frac{\pi(D_{TSV}-W)}{W+t}+1\right)} W \right]^{-1}$  \hspace{1cm} (4)

$C_{\text{Lateral}} = K_2 \frac{\pi \varepsilon_{\text{s}_i}(\varepsilon_{\text{s}_i}+1)}{4ln\left(\frac{\pi(D_{TSV}-W)}{W+t}+1\right)} W$  \hspace{1cm} (5)

where $\sigma_{\text{s}_i}$ is the silicon conductivity, $S_{\text{pad}}=WxW$ is the pad surface, $t$ is the conductor thickness, $K_1$ and $K_2$ represent the fringing factors, that in turn can be defined as Rousseau [2009], Benkechkache et al. [2014]:

$$K_1 = C_e \frac{D_{TSV}}{\varepsilon_0 \varepsilon_{\text{s}_i} S_{\text{pad}}}$$  \hspace{1cm} (6)

$$K_2 = (C_o - C_e) \frac{2ln\left[\frac{\pi(D_{TSV}-W)}{W+t}+1\right]}{\varepsilon_0(\varepsilon_{\text{s}_i}+1)W}$$  \hspace{1cm} (7)

with $C_o$ and $C_e$ the equivalent capacitance of the even- and odd-modes for two open-end coupled microstrip lines expressed as:

$$C_{e,o} = \sqrt{\mu_0 \varepsilon_0 \varepsilon_{\text{eff}_{e,o}}} Z_{C_{e,o}} W + C_{f_{e,o}}$$  \hspace{1cm} (8)

with $\varepsilon_{\text{eff}_{e,o}}$ and $Z_{C_{e,o}}$ the effective permittivities and the characteristic impedances at the end of circuits, respectively, $C_{f_{e,o}}$ the fringing capacitances for both even and odd-modes. The effective permittivities and characteristic impedance expressions could be defined in terms of other circuit geometries (such as substrate thickness, $T_{\text{sub}}$ and distance between via and the device, $D_{TSV}$), which are used in the expressions illustrated in details in Kirschning and Jansen [1984]. The same idea is used to define the fringing capacitance expressions from Edwards [1981].

Since the substrate network elements of both resistances and capacitances have values that are directly related to the local doping of the structure, the doping concentration is not constant throughout the substrate, the highly doped surface region, called ‘active’, is modeled as equivalent resistance $R_{\text{active}}$ and equivalent capacitance $C_{\text{active}}$. Whereas, at the bottom of the structure, the doping is constant and is considered as a region called ‘bulk’ modeled with an equivalent resistance $R_{\text{bulk}}$ and capacitance $C_{\text{bulk}}$, as can be seen in Figure 6-a. In our case study, the bulk region is considered with a high resistivity of 3.4 Ohm.cm while the heavily doped region with a low resistivity of 0.072 Ohm.cm Rousseau [2009]. Such values are determined using an approximation of the average doping in both regions.

Values of the various components of the considered structure, with a TSV placed on the left edge, can be calculated using the analytical expressions expressed above as a function of different parameters like the substrate thickness and the distance between the TSV and the device contacts.
2.2.2 Device description and analysis method

A SPICE model was developed using the circuit analysis tool HSpice-Synopsys to investigate the effect of 3D-TSV interconnects on MOS transistors. This approach is best suited to perform comprehensive characterization, particularly when complicated circuits and several parameters involved are in question. The MOS transistors were modeled using a compact model BSIM4 with a 65 nm technology, a channel length of 50 nm, and a gate oxide layer of 3.2 nm thick. The effect of TSVs on MOS transistors is investigated against different technological and electrical parameters, including the thickness of the substrate (\(T_{\text{sub}}\)), the distance between the via and MOS transistors contacts (\(D_{\text{TSV}}\)), and the signal rising/falling time (\(t_{\text{rf}}\)). Figure 8 depicts the electrical model schematic considered made up of the various circuit components determined previously.

This proposed model is considered for both nMOS and pMOS transistors using specific compact models, where all quantities are complementary with equivalent bulk and active resistances. The signal applied to the TSV, defined as \(V_{T\text{TSV}}\), is considered with a 3.3 V amplitude of a square wave potential. The impact of the via on the characteristics of a single MOS transistor, regarding both bulk voltage and drain current, was investigated and is plotted in 9.
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Figure 8: Circuit schematic used to study the 3D-TSV technology impact on a single MOS transistor.

Figure 9: Simulated TSV interconnects influence on the electrical characteristics of a MOS transistor.

2.2.3 Parameter optimization

The different parameters optimized are the same ones investigated previously, and which were performed using the analytical model proposed.

- **The substrate thickness**: This first parameter, \( T_{\text{sub}} \), was investigated in a range of values from 5 \( \mu \text{m} \) up to 20 \( \mu \text{m} \). The overshoots percentage taken from the drain current of both nMOS and pMOS transistors versus the substrate thickness is presented in Figure 10-a. These MOS transistors are placed at a 6 \( \mu \text{m} \) distance from the via. The impact of the oxide thickness of the TSV, \( T_{\text{ox}} \), is shown also in this figure, with two different values. It can be seen that the substrate thickness has a clear impact on the performance of MOS transistors. The increase of the drain current depends on the threshold voltage, that in turn depends on the bulk voltage. This is explained by the increase in the vertical component of the bulk resistance network. Moreover, the induced negative coupling effects are higher in the case of a pMOS transistor in comparison to the nMOS transistor, because the Body effect is more pronounced. Within the interval of \( T_{\text{sub}} \) values up to 10 \( \mu \text{m} \), the oxide thickness of the TSV has a significant impact on transistors nearby, hence the increase of this parameter reduces the substrate coupling.

- **The distance from the TSV**: The separation distance of the TSV from the device contact, \( D_{\text{TSV}} \), was varied between 2-10 \( \mu \text{m} \) range. Its effect is seen clearly through Figure 10-b. This figure shows the overshoot percentage taken from the drain current of the nMOS and pMOS transistors. The substrate thickness of these MOS transistors is fixed to 10 \( \mu \text{m} \). From this figure, it is evident that the substrate coupling decreases with the
Figure 10: (a) The overshoots percentage taken from the drain current of MOS transistors versus the substrate thickness, and (b) the overshoots percentage taken from the drain current versus the separation distance of the TSV from the MOS transistors contacts, and (c) the overshoots percentage taken from the drain current versus the rising/falling time signal.

Comparing results obtained from the numerical simulation previously, the variation observed was in the range of 4 to 8%, whereas the analytical approach seems to overestimate the impact of TSV at small substrate thicknesses, however, this difference doesn’t exceed more than 2%. The good agreement with the obtained results from the analytical model proposed confirms the possibility to use the proposed analytical approach to evaluate the 3D-TSV interconnects impact on the performance of CMOS circuits.

3 3D-TSV influence on CMOS circuits

The use of the proposed analytical approach was extended to evaluate in this case the influence of TSVs on the characteristics of CMOS ICs, and particularly in this work the CMOS inverter and the ring oscillator.
3.1 CMOS inverter

The electric model for this analysis necessitates the use of both types of MOS transistors, as shown in Figure 11. In this model, because the N-well acts as a shield toward the TSV-induced coupling preventing it from reaching the active area of the pMOS transistor, only the nMOS transistor is connected to the substrate resistance network. The TSV’s influence is being investigated with respect to the same parameters considered previously. Applying a square wave signal on the TSV of a 3.3 V amplitude with a frequency of 200 MHz and a rise/fall time of 200 ps, the simulated plot is shown in Figure 12. In this analysis, the $V_{DD}$ of the CMOS inverter is set at 1.8 V while its input was biased with a square wave voltage of 1.8 V and a 72 MHz frequency [Rousseau 2009].

3.1.1 The substrate thickness

The influence of the 3D-TSV interconnect on the performance of the CMOS inverter is studied first with respect to the substrate thickness that was varied in a range of values from 5 $\mu$m up to 20 $\mu$m (see Figure 13-a). The CMOS inverter parameter investigated concerns the output voltage. Placing the TSV at a 6 $\mu$m distance from the inverter, the overshoots on its output voltage induced by the via increases as the thickness of the substrate increases as well, which is consistent with the effects observed on the nMOS transistor alone.

3.1.2 The distance from the TSV

Figure 13-b depicts the overshoots on the output voltage of the CMOS inverter versus the separation distance of the TSV from the inverter contact. This parameter was investigated from 2 $\mu$m up to 10 $\mu$m taking into account also different thickness values of the TSV’s oxide layer.

Figure 11: Schematic view of the SPICE circuit model for the study of the impact of TSV on a CMOS inverter circuit.

Figure 12: Impact of TSV on the CMOS inverter output current and output voltage.
Figure 13: (a) The overshoots on the inverter output voltage as a function of the substrate thickness, and (b) The overshoots on the inverter output voltage as a function of the distance from the TSV contact, and (c) The overshoots on the inverter output voltage versus the TSV signal rising/falling time.

It is noted through the simulation results that the effect of the TSV on the inverter output voltage is minimal once the separation distance is large, whereas it gets more significant the closer the via to the inverter circuit. This is explained by the fact that both lateral active region and bulk resistances value that increase with distance. On the other hand, it was observed that a thicker oxide layer of the TSV helps reduce the substrate coupling.

### 3.1.3 The TSV signal rising/falling time

Figure 13c depicts the overshoots on the output voltage of the inverter versus the via’s signal rising/falling time. This parameter was investigated with a range of 25-300 ps, considering an inverter circuit placed at a separation distance of 6 \( \mu \text{m} \) from the via and a substrate of 10 \( \mu \text{m} \) thick. From the simulation results, it is observed that the overshoots on the output voltage of the inverter circuit decrease as \( t_{rf} \) get higher. This is mainly due to the effect of charge and discharge of the oxide layer capacitance of the via.

Even though the simulation results show that the induced coupling by the 3D-TSV interconnects causes no logical errors in the inverter circuit performance, it is still not negligible at least regarding the induced power consumption on the nMOS transistor.

### 3.2 Ring oscillator

Based on the same approach considered to investigate the TSV-induced coupling in the inverter circuit, we have evaluated, in this section, the impact of the 3D-TSV technology on a Ring Oscillator. For this purpose, we have taken as a reference an 11-stage ring oscillator circuit without the presence of any via connections nearby (see 14). Then, the electrical model to study the parasitic coupling induced by the TSV interconnects was implemented. The output signal
of the 11-stage oscillator with a TSV contact nearby was simulated considering a TSV biasing with a square wave potential of 3.3 V amplitude, a frequency of 200 MHz, and a signal rise/fall time of 200 ps. The oscillator simulation results were plotted in Figure 15 where the 11 inverters were biased with $V_{DD}$ of 3 V.

As a figure of merit for the ring oscillator, the delay time per gate is considered, that is defined as:

$$\tau = \frac{T}{2n}$$

when T is the oscillator time period and n the number of its gates (n=11 in the considered example).

### 3.2.1 The substrate thickness

The time delay variation of the ring oscillator induced by the TSV was investigated versus the substrate thickness. This parameter was varied in a range of values from 5 $\mu$m up to 20 $\mu$m and the oscillator circuit is placed at 6 $\mu$m away from the TSV contact.

From the simulation results shown in Figure 16a, it is evident that increasing the thickness of the substrate has a strong contribution and influence on the time delay of the circuit. Such behavior is much evident once a thinner TSV oxide layer is considered, as already seen in previous studies.

### 3.2.2 The distance from the TSV

This technological parameter has a clear impact on the performance of the ring oscillator, as illustrated in Figure 16b. This influence is expressed by the variation in time delay simulated versus such separation distance ranging from 2 $\mu$m to 10 $\mu$m.
From the simulation results obtained, it is clear that the TSV-induced time delay of the oscillator circuit is considerable once the separation distance is a few micrometers, whereas it gets lower at large distances. This is still explained by the fact that the increase in both lateral bulk and active region resistances causes a decrease in the parasitic coupling from the via.

### 3.2.3 The TSV signal rising/falling time

Figure 16-c depicts the TSV signal rising/falling time influence on the ring oscillator. This parameter was varied in a range of 25-300 ps and simulation results show that it does not show a considerable influence on the time delay of the oscillator in comparison to the previous cases.

The TSV has a greater impact on ring oscillator performance than on inverter performance, causing significant variance in the performance of a simple structure of an 11-stage oscillator circuit. The observed impacts would be amplified in circuits with a higher number of stages.

### 4 Conclusion

In this work we reported on the evaluation of the impact of TSV interconnects on the electrical performance of MOS devices by means of numerical TCAD simulation and an analytical model once considering CMOS circuits. Both approaches were defined and implemented to describe the TSV behavior at the circuit level and other phenomena such as the substrate coupling, as a function of different technological and electrical parameters. The analytical model compared to the numerical approach has proved to be effective to perform rapid and reliable simulations of the substrate coupling induced by the TSV on two commonly used CMOS circuits, i.e., the CMOS inverter and the ring oscillator.
Range of values for which the impact of the considered parameters (i.e., the substrate thickness, the distance from the TSV, and the signal rising/falling time) on the circuit performance is limited can be easily appreciated from the simulations, thus yielding a useful design tool for use with even more complex CMOS circuits.

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