Peak current failure levels in ESD sensitive semiconductor devices and their application in evaluation of materials used in ESD protection. Part 1: Theoretical analysis

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Peak current failure levels in ESD sensitive semiconductor devices and their application in evaluation of materials used in ESD protection. Part 1: Theoretical analysis

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Abstract. This paper shows that theoretical analysis of the thermal model of damage to electrostatic discharge (ESD) energy susceptible devices combined with data from Human Body Model test on devices can be used to estimate an ESD pulse current threshold for damage to ESD energy susceptible semiconductor devices over a wide range of ESD duration and waveforms. The technique is intended for laboratory evaluation of ESD threats from equipment, materials and other ESD sources in the electronics assembly factory environment. In Part 2 of this paper the predicted ESD current damage threshold is experimentally demonstrated to give a useful boundary to a “safe” area of ESD current and duration.

1. Introduction

The evolution of electronics and semiconductor technology has led to ever smaller devices which are more susceptible to damage from ElectroStatic Discharges (ESD) during manufacture and handling. These devices must be handled in an ESD Protected Area (EPA). In order to effectively specify and design ESD control equipment and materials for use in the EPA it is necessary to understand and quantify the characteristics of ESD that cause damage. The ESD susceptibility of an electronic component is often quoted as an ESD withstand voltage experimentally determined using the Human Body Model (HBM) test [1]. The withstand voltage is the largest ESD source voltage that the device can stand without damage. This voltage, however, only indicates the risk of damage only under the particular set of test conditions with the HBM ESD test source. The risk of ESD damage due to charged conductors or insulators cannot be directly assessed by using the device HBM withstand voltage.

Most devices are susceptible to the discharge energy not voltage [1]. In this work we restrict our discussion to ESD energy susceptible devices and pn junctions in particular in which damage often occurs because a small internal region is intensely heated by the passage of the ESD current [1]. The power required to raise the damage region to fail temperature is a function of the pulse duration: the shorter the ESD pulse, the more power is required for a failure [2]. Discharge power and discharge energy are proportional to discharge current and so it has been suggested that ESD current might be a better parameter for evaluating ESD damage risks [2],[3],[4] and that a material or item can be
evaluated for ESD risk on the basis of the maximum ESD current that can be drawn from it when it is acting as an ESD source.

In Part 1 of this paper we have shown that the ESD damage current threshold may be estimated from HBM data which are routinely measured and often given on device data sheets and that the current threshold may be extrapolated over a range of pulse durations using simple derating rules. This theory is then generalized to cover waveforms other than HBM. In Part 2 of the paper we have evaluated the current threshold concept experimentally using exponentially decaying resistor-capacitor circuit pulse (RC) and rectangular transmission line pulse (TLP) simulated ESD waveforms by investigating damage to example devices. The goal is to bridge the gap in understanding between device physics and assessment of electronics assembly ESD risks.

2. ESD current threshold

2.1. Component damage due to internal energy dissipation

The victim device is modelled as a series resistance, $R_d$, simulating the bulk resistance of the device, and a battery, $V_{bd}$, simulating the forward or reverse junction voltage of the device [1],[2]. The damage region may be a metallization track, transistor junction or other conducting device part. The power $P_f$ dissipated by ESD current flow $I_{esd}$ through the device leading to failure, is

$$ P_f(t) = I_{esd}^2(t)R_d(t) + I_{esd}^2(t)V_{bd} $$

where $I_{esd}(t)$ and $R_d(t)$ are the discharge current and effective device resistance. The power dissipation causes a temperature rise in the region – damage is caused if the temperature exceeds a certain threshold (e.g. the material melting point). Modern devices have extremely small (sub micron) internal feature dimensions, and so only a small energy is required to raise the hot spot to the damage temperature. A model of this failure mode based on the general heat flow equation leads to $P_f$ being a function of the pulse duration

$$ P_f = \left( \frac{\rho C_p V}{t} + \frac{\sqrt{\pi KnC_p}}{\sqrt{t}} + C \right) \Delta T $$

where $V$ is the volume of the heat source, $S$ is the surface area of the heated region, $C$ is a constant and $\Delta T$ is the temperature rise required to damage the device, $\rho$ is the density of the device material, $C_p$ is the specific heat, $T$ the temperature of the material, $K$ is the thermal conductivity, and $q(t)$ is the rate of heating per unit volume of the heat source [1],[2]. For sufficiently short pulses the situation is adiabatic and follows $1/t$ dependence. A constant amount of energy $\rho C_p V \Delta T$ is required to raise the heated region to failure temperature, dependent only on its size, properties of the materials, and the temperature rise to failure. This forms an energy threshold that must be exceeded before damage can occur. In the regime of intermediate pulse lengths some heat diffuses away from the defect region. For very long pulses energy is lost to the surrounding material at a constant rate (dependent on device heat sinking) and the failure power is constant. In summary, the power required to reach the failure temperature decreases as $t$ is increased until a steady state is achieved. For very small damage regions the $t^{-0.5}$ adiabatic pulse region is likely to be at very short (nanosecond) pulse durations.

2.2. Derivation of the current threshold

For ESD damage to occur with intermediate or long ESD pulse durations, the internal power dissipation in the damage region must exceed a threshold value to overcome heat losses at some discharge current threshold for ESD damage($P_f=f(I)$). The middle term of Equation (2) can be combined with the device model, Equation (1) leading to

$$ P_f = I_{esd}^2 R_d + I_{esd} V_{bd} = S \left( \sqrt{\pi KnC_p} \right) \Delta T t^{-0.5} $$

2
All the device parameters $S$, $K$, $\rho$, $C_p$ and $\Delta T$, $R_d$, $V_{bd}$ are dependent on device construction and may, to a first approximation, be assumed to be constants for a given device and failure mechanism.

Equation (3) contains the information required for the calculation of the current threshold for damage and can be simplified if we take into account typical damage mechanisms of energy sensitive devices. In reverse biased junction burnout, $V_{bd}$ is typically much higher than $I_{esd}R_d$ and Equation (3) is simplified by approximating the term $I_{esd}^2R_d$ to be negligible. In metallization burnout, on the other hand, $I_{esd}R_d \gg V_{bd}$ and the second term in Equation (3), $I_{esd}V_{bd}$, is negligible. These simplifications lead to limits for the dependence of the failure current on the ESD duration. In one extreme we can assume that $V_{bd} \gg I_{esd}R_d$ and power dissipation is mainly across the device junction. This gives a failure current threshold $I_f$ of

$$I_f = G t^{-n}$$

(4)

where $G$ is approximately constant for a given device and failure mode and $n = 0.5$ [2]. If the ESD failure mode is such that $V_{bd} \ll I_{esd}R_d$ then $n = 0.25$. It is less severe a derating function than the $t^{-0.5}$ relation.

We can obtain the peak current threshold empirically at 150 ns pulse duration by using standard ESD test data from the HBM model [2]. In this test, if the voltage dropped across the device is small the discharge current is primarily governed by the series 1500 $\Omega$ resistance, $R_{HBM}$. The peak current in the HBM ESD event can directly give a reasonable measure of the ESD current threshold for damage of the device in HBM-like situations. We need know nothing about the internal structure of the device, except to confirm that it is subject to energy related failure rather than being a voltage sensitive type. Perhaps most usefully, the test is already performed on the majority of devices. The peak ESD current threshold $I_{HBM}$ can be calculated from

$$I_{HBM} = \frac{V_{HBM}}{R_{HBM}}$$

(5)

where $R_{HBM} = 1500 \Omega$. We can derate the current threshold to give safe working at other ESD pulse duration $t_{esd}$ as we know $I_f$ varies with $t^{-0.5}$ or $t^{-0.25}$ and we can calculate, for any arbitrary $t_{esd}$

$$I_f = I_{HBM} \left( \frac{t_{esd}}{t_{HBM}} \right)^{-n}$$

(6)

At shorter ESD durations than 150ns the $t^{-0.25}$ curve must be used to obtain safe current limits. At longer durations, the $t^{-0.5}$ curve provides the safe limit. The lower of the two possible current limits must be used as we do not know the precise failure mode of the device. Figure 1 shows in normalised form $I_f/I_{HBM}$ how these failure thresholds vary with pulse duration. The area below the two curves then forms a “safe area”, in which ESD is not expected to damage the component.
2.3. The effect of variation in ESD waveform on the current threshold

Many natural ESD events, including many discharges originating from charged insulating materials, have exponentially decaying waveforms. ESD from charged conductive parts may have unidirectional exponential or oscillatory forms. The normal oscillatory form has an exponentially decaying envelope. The oscillatory waveform must have lower dissipation in the device than a unidirectional discharge of the same amplitude and duration, as the current periodically returns to zero. An oscillatory discharge defined in terms of its peak current and envelope duration can safely be treated as for the unidirectional exponential discharge. Other more unusual waveforms may require careful assessment to determine their risk factor.

Perhaps the worst case is the rectangular transmission line pulse often used to investigate the performance of microelectronic protection networks. This can be expected to result in a greater device dissipation compared to the unidirectional exponential waveform of similar amplitude and duration, as the peak current is maintained for the entire duration.

We used the theoretical method of Lee et al [8] to estimate the peak current threshold for destruction due to TLP equivalent to the RC threshold. The power dissipation in the device is integrated over the duration of the waveforms. For the case \( P_f \approx I_{esd}^2 R_d \) the energy \( E \) in the pulse dissipated in the device resistance \( R_d \) is given by

\[
E = 0.5 I_{fRC}^2 R_d RC = I_{fTLP}^2 R_d I_{TLP}
\]

(7)

if the TLP duration \( t_{TLP} \) is set equal to the RC time, resulting in that \( I_{fTLP} = 0.71 I_{fRC} \). For the case \( P_f \approx I_{esd} V_{bd} \) the energy in the pulse is

\[
E = I_{fRC} V_{bd} RC = I_{fTLP} V_{bd} I_{TLP}
\]

(8)

This leads to \( I_{fTLP} = I_{fRC} \). Clearly the case \( P_f \approx I_{esd}^2 R_d \) is more severe and leads to the conclusion that setting the current threshold at 0.71 \( I_{fRC} \) should give a margin of safety to avoid damage by any pulse waveform.

3. Conclusions

For damage to occur it is necessary for the applied ESD pulse to exceed two parameters - an energy threshold, and a discharge peak current threshold that may be estimated from the HBM test data. In practice the energy threshold may be dominant only for pulses that are very short duration (nanosecond or less). The peak current threshold calculated from HBM data can be used to estimate the boundary of an “ESD safe area” in the peak current-duration curve over a wide range of ESD duration based on \( t^{0.25} \) and \( t^{0.25} \) derating factors. The procedure has been extended to cater for “worst case” rectangular TLP waveforms. This theory is experimentally tested in Part 2 of our paper.

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