A new family of bioSFQ logic/memory cells

Vasili K. Semenov, Evan B. Golden, and Sergey K. Tolpygo

1 Department of Physics and Astronomy, Stony Brook University, Stony Brook NY 11794
2 Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA 02421

Abstract—Superconductor electronics (SCE) is competing to become a platform for efficient implementations of neuromorphic computing and deep learning algorithms (DLAs) with projects mostly concentrating on searching for gates that would better mimic behavior of real neurons. In contrast, we believe that most of the required components have already been demonstrated during the long history of SCE, whereas the missing part is how to organize these components to efficiently implement DLAs. We propose a family of logic/memory cells in which stored multi-bit data are encoded by quasi-analog currents or magnetic flux in superconductor loops while transmitted data are encoded as the rate of SFQ pulses. We designed, fabricated, and tested some of the basic cells to demonstrate a proof of concept, e.g., a unipolar and bipolar multipliers based on Josephson junction comparators. We coined the term bioSFQ to clearly connote close but distinguishable relations between the conventional SFQ electronics and its new neuromorphic paradigm.

Index Terms—artificial neural networks, bipolar multiplier, electronic circuits, neuromorphic computing, superconductor electronics, superconducting integrated circuits, SFQ, RSFQ.

I. INTRODUCTION

SUPERCONDUCTOR electronics (SCE) has demonstrated the lowest energy dissipation per operation [1] and the highest clock rates (~770 GHz) [2] among existing electronics. It is more mature than other beyond-CMOS technologies for classical and quantum computing. A number of hardware technologies are competing to become a platform for energy-efficient artificial neural networks (ANNs), including conventional CMOS (see, e.g., [3]), more exotic memristor-based [4], and perhaps even more exotic superconductor-based technologies [5], [6].

Josephson junctions (JJ) can act as natural spiking neuron-like devices for neuromorphic computing [7]. Most of the existing projects on implementation of superconductor electronics for neuromorphic computing concentrate on searching for gates that would better mimic behavior of real neurons, e.g., using adiabatic quantum flux parametrons [8], flux qubits, phase slip junctions [9], magnetic JJs [10], single photon detectors [11], [12], etc. [13]. Many JJ-based suggestions are purely theoretical and only a few operational JJ-based ANNs have been reported [13]-[16].

We believe that most of the required components have already been invented (in particular, by our team members) for superconductor digital electronics, whereas the essential missing part is how to creatively utilize and organize (design and fabricate) these components in large-scale, fast, and energy-efficient artificial neural networks. In this work, we propose a family of logic/memory cells in which stored multi-bit data are encoded by quasi-analog currents or magnetic flux in superconductor loops while transmitted data are encoded as the rate of SFQ pulses. We coined the name “bioSFQ” to clearly connote a close but distinguishable relation between the conventional SFQ electronics and its new neuromorphic paradigm. In the proposed devices and circuits, information propagates with the speed of light and its quasi-stochastic processing naturally emulates electrical processes in the brain.

Unique features of SCE continue to keep it attractive for large-scale electronic systems. However, in all prior attempts to implement SCE for general-purpose or high-performance computing it mimicked well-developed CMOS approaches and, as a result, its powerful potential has not been unleashed. Neuromorphic computing could become the greatest exception.

II. BASIC COMPONENTS

A. Storage of Analog Bipolar Data

Closed superconductor loops are traditional devices for storage of quantized magnetic flux. Josephson junction circuits allow the control the flux with single flux quantum accuracy as discussed, for example, in [17], Fig. 4. We implement such storage component as relatively long, thin film strips placed over one or between two ground planes; see Fig. 1c. The edges of the strip are terminated by flux pumps or, if necessary, by another Josephson junction-based circuitry.

B. Reading of Analog Bipolar Data

The value of current can be measured by a Josephson current comparator; see, for example, [18]. However, in the case of a superconducting current in a loop, it is more natural to use a non-destructive comparator or C-SQUID [19] that does not affect the measured current, as shown in Fig. 1a.

This research is based upon work supported by the Under Secretary of Defense for Research and Engineering under Air Force Contract No. FA8702-15-D-0001. (Corresponding author: Vasili Semenov.)

V. K. Semenov is with the Department of Physics and Astronomy, Stony Brook University, Stony Brook, NY 11794-3800, USA (e-mail: Vasili.Semenov@StonyBrook.edu).

E. B. Golden and S. K. Tolpygo are with the Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA 02421, USA (e-mails: Evan.Golden@ll.mit.edu, Sergey.Tolpygo@ll.mit.edu). Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org. Digital Object Identifier will be inserted here upon acceptance.
The comparator converts the applied current, $I$, into the rate of SFQ pulses. The probability of an SFQ pulse passage through the comparator is given by the error function

$$p(X) = \frac{1}{2} \left( 1 + \text{erf}(\pi^{1/2}X) \right), \quad (1)$$

where $I_{th}$ is the (adjustable) threshold current of the comparator. If current $I$ is the comparator input current $I_1$ shown in Fig. 1a, then the width of the comparator gray zone $\Delta I$ is defined by the thermal and quantum noise in the comparator junctions \cite{18} – \cite{22}. If $I$ is the current in the primary of the C-SQUID transformer L10, then the effective gray zone $\Delta I$ is a custom-adjustable parameter defined by the transformer L5-L10 to the desired effective gray zone width, e.g., $-0.15$ mA to $0.15$ mA in Fig. 1b.

The black trace in the Fig. 1b shows the measured dependence of the probability of the SFQ pulse transmission on current flowing via inductor L10. The desired widening of the grey zone is achieved by the additional attenuation of the current induced in L5 by shunting inductor L4. As a result, the inductive divider composed of L5 and L4 reduces the feeding current $I_1$ injected between comparator junctions J3 and J4. The red trace in Fig. 1b shows the complementary probability of no SFQ response on the clock pulse. The complementary output in the circuit is calculated by passing the direct output through an RSFQ NOT cell, not shown in Fig. 1.

The comparator transmission function (1) is nonlinear and saturates at $|X| > 1$. This behavior closely resembles the sigmoid response function frequently used to describe behavior of neurons. In general, saturation of the response function with stimulus strength is typical for all biological systems. Hence, this feature of the comparator response (1) is highly beneficial for neuromorphic applications.

Near the threshold, $|X| < \Delta I$, expansion of (1) is very close to the linear response

$$p(X) = \frac{1}{2} + X, \quad (3)$$

shown as the black straight line in Fig. 1b. The linear mode of operation allows us to perform many useful operations in a very simple manner, see III below.

C. Other Components

Layout of a simple bioSFQ circuit comprising a few basic components is shown in Fig. 2. In fact, all basic components of bioSFQ were reviewed in \cite{23} and many later publications as components of SFQ digital circuits. After 30 years in existence, some of them were “reinvented” as neural network cells; for example, the splitter cell was reintroduced in \cite{24}.
III. BASIC FUNCTIONS

A. Copying of Bipolar Currents

Two inputs in Fig. 1a (inductor L10 and L11) are required to use the comparator for measuring a linear combination of currents I\textsubscript{10} and I\textsubscript{11} flowing in the corresponding inductors. In particular, if mutual inductances of L5 and L10, and of L5 and L11 are equal and have opposite signs $M_{L5,L10} = -M_{L5,L11}$, the comparator measures difference of the two input currents, as shown in Fig. 3. Trains of “positive” and “negative” SFQ pulses shown in the upper traces in Fig. 3b are continuously applied to opposite ends of inductor Y, as shown in Fig. 3a. As a result, the cell is trying to keep the difference between the signals (the middle trace in Fig. 3b) as low as possible. The lower traces show results of the simulation of the Copy operation: copying current $X$ (black trace) in one inductor to current $Y = X$ (blue trace) in another inductor.

B. Bipolar Multiplication

A bipolar multiplier requires three comparators operating in the proportional mode; see Fig. 4. The first (lower) comparator in Fig. 4a converts operand $X$ to positive and negative trains of SFQ pulses which serve as clock pulses for two upper $Y$ comparators. As a result, the rates of output SFQ pulses from $Y$ comparators are proportional to a product of $X$ and $Y$. Two mergers join the corresponding trains of pulses and inject them to an inductor with large inductance. Earlier we used superconductor loops that store data for an infinitely long time, even after interruption of all SFQ pulses. Here we demonstrate a solution for a temporal storage of data. A relaxation of current to
zero value is provided by a small resistor shown on top of Fig. 4a. The relaxation time is defined by $L/R$ constant. At nonzero $Z$, the rates of positive and negative pulses are unbalanced and the value of current is proportional to the difference of positive and negative rates of SFQ pulses applied to the opposite edges of line $Z$.

The middle traces in Fig. 4b show variations of input signals $X$ and $Y$ with time. $Y$ remains positive the entire time, while $X$ changes from a positive to a negative value. The lower traces in Fig. 4b show the idealized product $X^*Y$ (black color) and the actual (simulated) multiplication results produced by the circuit (blue color).

### C. Demonstration of Unipolar Multiplication

Demonstration of the bipolar multiplier is in progress. At this point in time, we present the measured properties of a unipolar counterpart. It requires just two comparators connected in series as shown in Fig. 5. The multiplier utilizes the fact that the probability of independent events equals the product of individual probabilities. The first comparator ($X$) is fed by SFQ pulses with frequency $f_{ct}$ (from the clock source) and converts them into a stream of output SFQ pulses with frequency $f_{X} = p_{X}f_{ct}$. The SFQ pulse transfer probability $p_{X}$ is given by (1), (2) and defined by the applied current $I_{X}$, the corresponding threshold current $I_{thX}$, and the width of the gray zone $\Delta I_{X}$. Similarly, the second comparator ($Y$) multiplies its input frequency $f_{X}$ by its transfer probability $p_{Y}$, which is defined by the measured current ($I_{Y}$) and the corresponding parameters $I_{thY}$ and $\Delta I_{Y}$ of the second comparator.

The output frequency of the two-comparator multiplier is given by

$$f_{out} = p_{X}p_{Y}f_{ct}. \quad (4)$$

The time-averaged output voltage of the device is given by the Josephson frequency to voltage relation $V_{out} = \Phi_{0}f_{out}$. In the linear regime of both comparators, (4) reduces to

$$f_{out} = f_{ct} \left( \frac{2}{2} + X \right) \left( \frac{2}{2} + Y \right). \quad (5)$$

The measurement results of the described two-operand unipolar multiplier are shown in Figs. 5 and 6. The circuit was fabricated in the 8-Nb layer planarized process SFQ5ee using Nb/Al-AlO$_x$/Nb junctions with Josephson critical current density of 100 $\mu$A/µm$^2$ and the minimum linewidth of 0.25 µm [25]. We have found that both comparators are very well described by (1), and the output of the multiplier is described by (4) at up to 35 GHz sampling frequency.

The full testing results are demonstrated in the three-dimensional color map in Fig. 6 showing the color-coded normalized output frequency as a function of both input currents $I_{X}$ and $I_{Y}$. One can see that the device is fully functioning and operates as expected. Obviously, the demonstrated device can be extended to unipolar multiplication of multiple operands by adding more comparators in series.

### IV. Conclusion

We presented quasi-analog Josephson junction circuits which can be useful for the implementation of deep learning.
algorithms and neuromorphic computing. The circuits could be easily modified for large fan-ins and fan-outs because long storage inductors could be coupled with many comparators and many trains of SFQ pulses could be split and merged if necessary. Although presented and demonstrated circuits are composed of known components, their parameters are highly original. More importantly, the circuits serve as demonstrations of the potential of other prospective quasi-analog superconductor circuits.

Our near-term goal is in scaling up the suggested bioSFQ approach to large-scale circuits utilizing the availability of a unique fabrication technology at MIT LL, sufficient to manufacture circuits with up to ten million Josephson junctions per chip [25], [26] as well as a recently demonstrated AC/SFQ biasing technique of SFQ circuits [27].

However, our dream project is beyond implementation of the known deep learning algorithms which, as far as we know, are quite disconnected from the known successful implementations of deep learning in nature, e.g., as humans. This is because human brains do not contain multi-bit adders and multipliers required for implementing machine learning algorithms. In this respect, our bioSFQ approach is not going to change this. We share the known opinion that the cortex effectiveness depends on the complexity of the circuit rather than on the details of neuron interconnections. It would be fantastic to create superconductor cortex-like circuitry so complex that it would start behaving as a real cortex.

ACKNOWLEDGMENT

We are grateful to Alex Wynn for his interest in and support of this work. The numerical simulations were performed using PSCAN2 software package developed by Pavel Shevchenko [28]. We thank to Coenrad Fourie for assistance with InductEx software [29] used for inductance extraction from circuit layouts. We are also grateful to Vlad Bolkhovsky and Ravi Rastogi for overseeing the wafer fabrication.

This material is based upon work supported by the Under Secretary of Defense for Research and Engineering under Air Force Contract No. FA8702-15-D-0001. Any opinions, findings, conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the Under Secretary of Defense for Research and Engineering. Delivered to the U.S. Government with Unlimited Rights, as defined in DFARS Part 252.227-7013 or 7014 (Feb 2004). Notwithstanding any copyright notice, U.S. Government rights in this work are defined by DFARS 252.227-7013 or DFARS 252.227-7014 as detailed above. Use of this work other than as specifically authorized by the U.S. Government may violate any copyrights that exist in this work.

REFERENCES

[1] J. Ren, and V. K. Semenov, “Progress with physically and logically reversible superconducting digital circuits,” IEEE Trans. Appl. Supercond., vol. 21, no. 3, pp. 780-786, Jun. 2011.

[2] W. Chen, A. V. Rylyakov, V. Patel et al., “Rapid Single Flux Quantum T-flip flop operating up to 770 GHz,” IEEE Trans. Appl. Supercond., vol. 9, no. 2, pp. 3212-3215, Jun. 1999.

[3] J. Hasler, and B. Marr, “Finding a roadmap to achieve large neuromorphic hardware systems,” Frontiers in Neuroscience, vol. 7, Sep. 2013, Art. no. 11.

[4] M. Prezioso, F. Merrikh-Bayat, B. D. Hoskins et al., “Training and operarion of an integrated neuromorphic network based on metal-oxide memristors,” Nature, vol. 521, no. 7550, pp. 61-64, May 2015.

[5] K. Berggren, Q. F. Xia, K. K. Likharev et al., “Roadmap on emerging hardware and technology for machine learning,” Nanotechnology, vol. 32, no. 1, Oct. 2020, Art. no. 012002.

[6] E. Toomey, K. Segall, and K. K. Berggren, “Design of a power efficient artificial neuron using superconducting nanowires,” Frontiers in Neuroscience, vol. 13, Sep, 2019, Art. no. 933.

[7] P. Crotty, D. Schultz, and K. Segall, “Josephson junction simulation of neurons,” Physical Review E, vol. 82, no. 1, Jul, 2010, Art. no. 011914.

[8] I.I. Soloviev, A. E. Schegolev, N. V. Klenov et al., “Adiabatic superconducting artificial neural network: Basic cells,” J. Appl. Phys., vol. 124, no. 15, Oct. 2018, Art. no. 152113.

[9] R. Cheng, U. S. Goteti, and M. C. Hamilton, “Spiking neuron circuits using superconducting quantum phase-slip junctions,” J. Appl. Phys., vol. 124, no. 15, Oct, 2018, Art. no. 152126.

[10] M. L. Schneider, C. A. Donnelly, S. E. Russell et al., “Ultralow power artificial synapses using nanotextured magnetic Josephson junctions,” Science Advances, vol. 4, no. 1, Jan, 2018, Art. no. e1701329.

[11] J. M. Shainline, S. M. Buckley, A. N. McCaughan et al., “Circuit designs for superconducting optoelectronic loop neurons,” J. Appl. Phys., vol. 124, no. 15, Oct. 2018, Art. no. 152130.

[12] J. M. Shainline, S. M. Buckley, A. N. McCaughan et al., “Superconducting optoelectronic loop neurons,” J. Appl. Phys., vol. 126, no. 4, Jul. 2019, Art. no. 044902.

[13] F. Chiarello, P. Carelli, M. G. Castellano et al., “Artificial neural network based on SQUDs: demonstration of network training and operation,” Supercond. Sci. Technol., vol. 26, no. 12, Dec. 2013, Art. no. 125009.

[14] K. Segall, M. LeGro, S. Kaplan et al., “Synchronization dynamics on the picosecond time scale in coupled Josephson junction neurons,” Phys. Rev. E, vol. 95, no. 3, Mar, 2017, Art. no. 032220.

[15] T. Onomi, and K. Nakajima, "An improved superconducting neural circuit and its application for a neural network solving a combinatorial optimization problem," J. Phys. Conf. Series, vol. 507, May 2014, Art. no. 04029.

[16] Y. Yamanashi, K. Umeda, and N. Yoshikawa, "Pseudo sigmoid function generator for a superconductive neural network," IEEE Trans. Appl. Supercond., vol. 23, no. 3, Jun. 2013, Art. no. 1701004.

[17] M. W. Johnson, P. Bunyk, F. Maibaum et al., "A scalable control system for a superconducting adiabatic quantum optimization processor," Supercond. Sci. Technol., vol. 23, no. 6, Jun. 2010, Art. no. 065004.

[18] T.V. Filipov, Y.A. Polyakov, V.K. Semenov, and K.K. Likharev, "Current resolution of RSFQ comparators," IEEE Trans. Appl. Supercond., vol. 5, no. 2, pp. 2240-2243, Jun. 1995.

[19] V. K. Semenov, "Digital SQUDs: New definitions and results," IEEE Trans. Appl. Supercond., vol. 13, no. 2, pp. 747-750, Jun. 2003.

[20] V. K. Semenov, T. V. Filipov, Y. A. Polyakov et al., “SFQ balanced comparators at a finite sampling rate,” IEEE Trans. on Appl. Supercond., vol. 7, no. 2, pp. 3617-3621, Jun. 1997.

[21] T.V. Filipov, A. Sahu, M. Erençelik, D. Edelsits, M. Habib and D. Gupta, "Gray zone and threshold current measurements of the Josephson balanced comparator," IEEE Trans. on Appl. Supercond., vol. 31, no. 5, pp. 1-7, Aug. 2021, Art no. 1101007.

[22] T.J. Walls, T.F. Filipov, and K.K. Likharev, "Quantum fluctuations in Josephson junction comparators," Phys. Rev. Lett., vol. 89, no.21, p. 217004, Nov. 2002.

[23] K.K. Likharev, and V. K. Semenov, "RSFQ Logic/Memory family: A new Josephson-junction technology for sub-tera赫ertz-clock-frequency digital systems," IEEE Trans. on Appl. Supercond., vol. 1, no. 1, pp. 3-28, Mar, 1991.

[24] M. L. Schneider, and K. Segall, “Fan-out and fan-in properties of superconducting neuromorphic circuits,” J. Appl. Phys., vol. 128, no. 21, Dec. 2020, Art. no. 214903.
[25] S.K. Tolpygo, V. Bolkhovsky, R. Rastogi et al., “Fabrication processes for superconductor electronics: Current status and new developments,” *IEEE Trans. Appl. Supercond.*, vol. 29, no. 5, Aug. 2019, Art. no. 1102513.

[26] S.K. Tolpygo S.K. Tolpygo, V. Bolkhovsky, R. Rastogi et al., “A 150-nm process node of an eight-Nb-layer fully planarized process for superconductor electronics,” *Applied Superconductivity Conference, ASC 2020 Virtual Conference*, 25 Oct. – 7 Nov. 2020, Invited presentation Wk1EOt3B-01. *Superconductivity New Forum (SNF)*, vol. 14, Issue No. 49, March 19, 2021, Art. no. STP669 Wk1EOt3B-01. [Online] Available: https://snf.ieeeesc.org/issues/snf-issue-no-49-march-2021

[27] V. K. Semenov, E. B. Golden and S. K. Tolpygo, “SFQ bias for SFQ digital circuits,” *IEEE Trans. Appl. Supercond.*, vol. 31, no. 5, Aug. 2021, Art. no. 1302207.

[28] P. Shevchenko, PSCAN2 Superconductor Circuit Simulator. [Online] Available: http://pscan2sim.org/documentation.html

[29] C. J. Fourie, InductEx, Stellenbosch Univ., Stellenbosch, South Africa, 2015. [Online]. Available: http://www.inductex.info