The Case for RISP:
A Reduced Instruction Spiking Processor

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Abstract—In this paper, we introduce RISP, a reduced instruction spiking processor. While most spiking neuroprocessors are based on the brain, or notions from the brain, we present the case for a spiking processor that simplifies rather than complicates. As such, it features discrete integration cycles, configurable leak, and little else. We present the computing model of RISP and highlight the benefits of its simplicity. We demonstrate how it aids in developing hand built neural networks for simple computational tasks, detail how it may be employed to simplify neural networks built with more complicated machine learning techniques, and demonstrate how it performs similarly to other spiking neuroprocessors.

I. INTRODUCTION

Since the 1960s, researchers have turned to the brain for inspiration on how to build novel computing devices. This has led to several waves of research on spiking neuroprocessors [28]. In our previous research, we have explored all facets of neuroprocessors, from fabrication and nanotechnology [2], [4], to circuits and systems [11], [29] to applications and simulations [9], [15], to data encoding and decoding [31], to machine learning [25], [30]. Informed especially by our development of several neuroprocessors [6], [8], [19], [20], we have been motivated to research what happens when we simplify, rather than complicate. The result is RISP, a Reduced Instruction Spiking Processor.

RISP features integrate-and fire-neurons with discrete integration cycles. Synaptic delays are also discrete, and synaptic weights and neuron thresholds may be configured as either discrete or analog. Besides the aforementioned parameters, the only other configurable feature of RISP is that neurons may either retain their activation potentials indefinitely, or they may leak away completely at each integration cycle. There are no other complicating features of RISP that are in many other neuroprocessors, such as plasticity, refractory periods, custom integration techniques, complicated leak models and learning rules. In this paper we define RISP and detail some of its attractive properties. Our goal is to demonstrate that a simple neuroprocessor like RISP is viable alternative to more complicated neuroprocessors.

II. RELATED WORK

There are several neuroprocessor models, typically implemented in simulation, that are commonly used in the literature to explore and evaluate spiking neural networks and neuromorphic-style computation. These tend to be focused on one particular domain at a time. For example, there are a set of simulators that target computational neuroscience simulations, including NEST [10], [12], NEURON [3], Brian [13], Brian2 [35], Nengo [3], GeNN [37] and Brian2GeNN [36]. Though these simulators tend to have significant flexibility in the types of computation that can be achieved, with large variation in the types of neuron and synapse models that can be implemented, that flexibility often comes at the price of slow simulation times for even simple networks, making it difficult to use those simulators to evaluate new types of algorithms [16]. There are also simulators that primarily target machine learning-style computation with spiking neural networks, including BindsNET [14] and NengoDL [27]. Because these simulation environments focus on the machine learning use case of spiking neural networks, their functionality is often restricted to accommodate that behavior. Finally, there are simulation frameworks that primarily target particular neuromorphic hardware implementations, including NEMO [22], which targets IBM’s TrueNorth [17], and NengoLoihi, which targets Intel’s Loihi [7]. These simulators are focused on capturing the functionality of the underlying hardware and can also restrict the types of evaluations that can occur on those systems or perform prohibitively slowly [16].

III. RISP SPECIFICATION

In RISP, each neuron has two configurable parameters: a threshold, and whether or not the neuron leaks. As with most spiking neuroprocessors, each neuron stores an action potential, whose value may be increased or decreased by spikes on incoming synapses. Processing works in discrete timesteps, where incoming spikes are integrated over the timestep, and it is the neuron’s action potential at the end of the timestep that determines whether or not the neuron fires. When a neuron is configured with leak enabled, then if a neuron does not fire at the end of the integration cycle, its action potential is reset to zero. Without leak, neurons retain their action potentials across time steps.

Because of the integration cycle of neurons, synapses only have unit delays. Like neurons, synapses may be configured to either have discrete weights or analog weights. There is no restriction on connectivity, or the number of synapses that may come into or go out of a neuron.

Certain neurons may be designated as input neurons that may receive spikes from the outside world. Similarly, neurons may be specified to be output neurons, whose spikes may be monitored by the outside world.
To be precise, a RISP network is defined by 8 sets:

1. **N Neurons:** \( V = \{ v_0, v_1, \ldots, v_{N-1} \} \)
2. **N Thresholds:** \( T = \{ t_0, t_1, \ldots, t_{N-1} \} \)
3. **N Leaks:** \( L = \{ l_0, l_1, \ldots, l_{N-1} \} \)
4. **M Synapses:** \( E = \{ e_{0}, e_{1}, \ldots, e_{M-1} \} \) \( e_{i} = (v_j \rightarrow v_k) \)
5. **M Weights:** \( W = \{ w_{0}, w_{1}, \ldots, w_{M-1} \} \)
6. **M Delays:** \( D = \{ d_{0}, d_{1}, \ldots, d_{M-1} \} \)
7. **Input neurons:** \( I \subseteq V \)
8. **Output neurons:** \( O \subseteq V \)

Figure 1 shows a very simple RISP network that computes the binary AND of two inputs \( A \) and \( B \). When spikes are applied to both input neurons at timestep 0, then the output neuron \( X \)'s action potential is increased to a value of two at timestep 1. As such, if fires. If a spike is applied to one of \( A \) or \( B \), but not to the other, then \( X \)'s action potential only reaches a value of one, and therefore it does not fire. Moreover, since it is configured with leak, its action potential is reset to zero, and the network is ready to compute a new AND at the next timestep.

**IV. ATTRACTIVENESS OF RISP**

RISP’s simplicity is attractive in many pragmatic respects. We detail them in the sections below.

**A. Hand Constructing Networks**

Because of its simplicity, it is a straightforward matter to construct RISP networks by hand, rather than by machine learning or other optimization techniques. This can be useful, either for solving simple problems, or for composing larger neural networks.

We present an example in Figure 2. This network calculates which input neuron, \( I_X \) or \( I_Y \), spikes more over an interval of \( t \) timesteps. If \( I_X \) spikes more, then \( O_X \) spikes exactly once, at timestep \( t + 1 \). If \( I_Y \) spikes more, then \( O_Y \) spikes exactly once, at timestep \( t + 1 \). If they spike equally, then neither spikes, although it is a straightforward matter to add an extra synapse to break ties in favor of \( I_X \) or \( I_Y \). There is a bias neuron that is required to spike once at timestep 0. The network clears itself, and may be reused for more inputs at timestep \( t + 1 \).

This type of network is useful for composing spiking neural networks, perhaps created by other methodologies (e.g., backpropagation [33], [34] or genetic algorithms [30]). For example, some neural networks, like the one we show later in section IV-B require their outputs to be interpreted by voting among two output neurons. The network in Figure 2 performs this interpretation, which can in turn be used as inputs to other spiking neural networks, or even as control signals for a physical device.

There have been other research projects that construct spiking neural networks that may be implemented by RISP, either by targeting RISP explicitly, or by targeting a neural network that conforms to the RISP specifications. For example, in our previous work, we have constructed RISP networks that perform binary operations on a variety of input/output encodings and decodings, and RISP networks that convert between encodings/decodings [25]. The Whetstone training methodology uses backpropagation and a “sharpening” activation function to train deep spiking neural networks that may be implemented on RISP [33], and to reduce the size of the resulting networks, we developed a convolutional “kernel” on RISP [25]. Monaco and Vidiola’s integer factorization sieve [21] may be implemented on RISP.

**B. Network Simplification**

RISP’s simplicity makes it straightforward to analyze network behavior to simplify and improve the networks. As an example, consider the spiking neural network in Figure 3. This network was trained by the genetic algorithm EONS [30] to solve the cart-pole problem. In this problem, there is a cart enclosed on a fixed-size road, and on the cart is a pole on a hinge that can fall left or right. The goal of the problem is to push the cart left and right at fixed power, and keep both the cart on the road and the pole balanced.

To solve this with RISP and EONS, we selected an input encoding technique where each input value corresponds to two input neurons, with negative values spiked into one neuron (e.g., \( I_X^- \)) and positive values spiked into another (e.g., \( I_X^+ \)). The magnitude of the value is converted into a number of spikes, from one to four, and the spikes all have unit weights.

There are two output neurons, \( O_L \) and \( O_R \), which correspond to pushing the cart left and right respectively. The spiking neural network “runs” the application by working in discrete simulated time intervals of 0.02 seconds. At the

![Fig. 1. An example RISP network that computes the binary AND of inputs A and B. The output neuron must be configured with leak, so that when one input spikes and the other doesn’t, the action potential is reset to zero for the next problem.](image1)

![Fig. 2. RISP network that computes which input, \( I_X \) or \( I_Y \), fires more over an interval of \( t \) timesteps. The synapses are colored to facilitate reading the elements of the sets \( E, W \) and \( D \).](image2)
we may deduce that whenever neuron 2 fires, neuron B of 0.65 and delay of 2, and neuron B is the only post-synapse to neuron fire one timestep later. Further, because the synapse B→8 has weights that exceed the neuron’s threshold of -0.21. Therefore, we may set the weights of all of these synapses equal to one, and set the threshold of neuron 8 to one as well.

By applying observations as these, we may simplify the network in Figure 3 into the one in Figure 4. This network has only one hidden neuron, a reduction of 75 percent, and 15 synapses, a reduction of 17 percent. Moreover, seven of the neuron thresholds (64 percent) and nine of the synapse weights (60 percent) have been set to one.

With EONS, we train the spiking neural network using ten random starting positions for the cart and pole, and run the genetic algorithm until a network has been trained to keep the cart on the road and the pole balanced for five simulated minutes in each of the ten starting positions. As shown in the figure, the network has four hidden neurons and 18 synapses. The neuron thresholds and synapse weights are floating point numbers whose values are rounded on the picture.

Because of the simplicity of RISP and of the input encoding, we can simplify this network with the goals being:

- Reduce the number of neurons and synapses.
- Set neuron thresholds and synapse weights to 1 or -1.

Both goals allow our networks to be implemented more simply, and to consume less power while executing. An example of this simplification is to consider the neurons 2, B and 8 in Figure 4. Since the synapse 2→B has a weight of 0.65 and delay of 2, and neuron B has a threshold of -0.66, we may deduce that whenever neuron 2 fires, neuron B will fire one timestep later. Further, because the synapse B→8 is the only post-synapse to neuron B, and its delay is two, we may simply delete neuron B, and replace its pre and post synapses with a synapse 2→8 whose delay is 3.

In a separate analysis, we observe that all four pre-synapses to neuron 8 have weights that exceed the neuron’s threshold of -0.21. Therefore, we may set the weights of all of these synapses equal to one, and set the threshold of neuron 8 to 0.9.

One of our current research projects is to implement these and similar observations to simplify RISP networks. We are also attempting stochastic and enumeration techniques to simplify the networks using empirical observations. These techniques are enabled by the fact that RISP is simple, and does not have features such as plasticity, complex learning rules and refractory periods, that complicate the analysis of the networks.

C. Genetic Training and Simulation Speed

Over the past seven years, the TENLab research group has performed many explorations of real-time control applications with spiking neuroprocessors [1], [18], [23], [51]. One of the easiest of these is the cart-pole application mentioned in section IV.B. In this section, we perform a small experiment using a genetic optimization of spiking neural networks on the cart-pole application, to see whether RISP trains similarly to other spiking processors. We use the same input encoding as in section IV-B. We perform six sets of optimizations using the EONS genetic algorithm and the TENLab neuromorphic computing framework [24], [30], [32]. These are listed in Table 1.

The first four processors listed are the four variants of RISP. The fourth is Caspian [20], developed at Oak Ridge National Laboratory and implemented on FPGAs, with a very fast simulator. The fifth is DANNA2, developed by TENLab and implemented on FPGAs, with a VLSI workflow [19]. We performed a simple genetic optimization composed of populations of 500 networks optimizing over 100 epochs, with 10 random starting positions of the cart and pole. For each
In this paper, we introduce RISP, a Reduced Instruction Spiking Processor, whose goal is to explore the effectiveness of simplifying spiking neuroprocessors. RISP features integrate-and-fire neurons, unit integration cycles and therefore unit synaptic delays, and either analog or discrete weights and thresholds. The only other feature is that neurons may leak their action potentials at each cycle, or they may retain them.

In this paper, we demonstrate how RISP’s simplicity enables the hand-construction of networks, and how it allows us to reason about pre-trained networks to simplify them. Finally, we perform a very simple experiment with genetic training on a control application to show that RISP trains on par with other neuroprocessors that contain more features.

Our near-future plan with RISP is to implement a network compiler that renders RISP networks on inexpensive micro-controllers like the RP2040 ($5) and FPGA’s like the UPduino ($25). We anticipate that RISP’s simplicity should lead to very clean implementations, featuring high density of neurons and synapses on these inexpensive devices. The devices may then be used in physical experiments such as the ones we performed with the robots NeoN and GRANT.

The bottom line is that simplicity in a spiking neuroprocessor has multiple advantages, and is worth exploring as an alternative to neuroprocessors with more complicated, albeit potentially bio-realistic features. Our goal with RISP is for it to be the “simple” option as a spiking neuroprocessor in applications and scenarios that desire to explore spiking neuroprocessors as their solutions.

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