Data-driven complementary recycling folded cascode OTA

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Abstract. A data-driven complementary recycling folded cascode (CRFC) OTA is demonstrated in this article. The proposed OTA introduces digital concept to analog world, establishing a data-driven scheme to control the current dynamically. Two comparators detect the state of virtual ground node of the amplifier in a closed loop. When the input differential signal exceeds the threshold of comparator, the biasing current of the OTA is augmented to achieve a higher slew rate and larger GBW, while for a small input, the OTA consumes relatively low power. The CRFC architecture improves the GBW and slew rate compared with the conventional RFC. A transient simulation on a capacitive feedback loop shows that the data-driven scheme improves the settling time of the circuit from 101.8 ns to 15.8 ns while the power only increases by 57%. The OTA is designed for capacitor sensing circuit in MEMS gyroscope readout ASIC, but it also can be used in other low power applications such as biochips and switched capacitor ADCs.

1. Introduction
With the advantages of low cost, small size and low power consumption, MEMS gyroscopes have been widely applied in both commercial and military fields such as portable devices, industrial robots, automobile safety and navigation [1-2]. The requirement of high-resolution digitalized sensing and control interface circuit imports ASIC technique to the area of angular sensors, which also helps build more integrated and energy-saving gyroscope systems [3]. There is a demand for low power dissipation, low noise, and quick response with the development of high-precision gyroscope. The ASIC usually drives relatively large capacitive loads to reduce noise, for example, in charge amplifier and A/D conversion circuit [4-5]. Generally, the angular rate sensing signal lasts for a short moment and the readout circuit works in static state in most of time. The operational amplifier in such circuit requires large GBW and high slew rate (SR) to detect the sensor's input quickly. Previous works [6-7] chose folded cascode (FC) operational transconductance amplifiers (OTA) to acquire high gain and large signal swing. The conventional class-A op-amp requires much biasing current to achieve high SR [8], but when the circuit works in zero-input state, high SR is not necessary and the amplifier wastes much of the power.

To improve the GBW and SR of folded cascode amplifier, Assaad et al. introduced the recycling folded cascode (RFC) structure, with cross-over current mirrors to make more efficient use of biasing current [9-10]. In recent years, some techniques have been presented to improve the performance of RFC amplifier [11-13]. In this article, we demonstrate a data-driven complementary recycling folded cascode (CRFC) OTA. We established a data-driven scheme with a controlled extra current source branch added to the biasing circuit of the OTA. When the difference of two input signals is small, the data-driven branch is turned off and the OTA consumes relatively low power; when the input
differential signal exceeds a threshold, the extra current are poured into the biasing circuit to enhance the SR and GBW of the OTA and improve its speed. Moreover, we developed the CRFC amplifier topology to augment the GBW and make more efficient use of the current than the conventional recycling folded cascode (RFC) amplifier. The structure of the proposed amplifier is analyzed in Section 2. Simulations are done to examine the performance of the OTA using HJTC 0.18 μm technology and the results are discussed in Section 3. The conclusions are presented in Section 4.

2. Proposed Data-driven CRFC OTA
The proposed data-driven complementary recycling folded cascode OTA consists of two parts: CRFC amplifier circuit and biasing circuit with data-driven scheme.

2.1. CRFC amplifier circuit

![Figure 1. CRFC amplifier circuit.](image)

We introduce a CRFC [14] architecture as the main part of the amplifier, shown in figure 1. Compared with the conventional RFC [9-10], in which there are only PMOS input transistors (as MP1a, MP1b, MP2a, MP2b in figure 1), an NMOS input branch formed by transistors MN1a, MN1b, MN2a, MN2b is added to the CRFC amplifier circuit to compose a complementary input pair. We set the biasing current of either input drivers, i.e. the drain current of MP0 or MN0, equal to $2I_b$, and thus the total static current of the CRFC amplifier is $6I_b$. The transconductance of the amplifier can be written as

$$G_m^{CRFC} = 4g_{mP1a} + 4g_{mN1a}. \quad (1)$$

Suppose a large signal is inputted into the amplifier, assuming $V_{INP} > V_{INN}$, to cut MP2a, MP2b, MN1a and MN1b off. Then the tail current of MP0 flows through MP1b and is amplified by a current mirror with a factor of 3, leading to a total current of $6I_b$ to discharge the capacitive load at $V_{OUTN}$ if we ignore parasitic parameters. Similarly, the current to charge the capacitor at $V_{OUTP}$ is also $6I_b$. So the slew rate of the fully differential output CRFC is

$$SR_{CRFC} = 12I_b / C_L. \quad (2)$$

where $C_L$ denotes capacitive output load. The $G_m$ and $SR$ of conventional RFC can be expressed as [10]

$$G_m^{RFC} = 4g_{mP1a} \quad (3)$$

and

$$SR_{RFC} = 6I_b / C_L. \quad (4)$$
with a total current of $4I_b$. This result indicates the GBW of the CRFC are improved by a factor of 1/3 compared with the RFC, for the same power and capacitive load. If we assume the PMOS and NMOS input transistors have the same $g_m$ and define two FoMs to characterize the amplifiers' performance as

$$F_{oM_1} = \frac{GBW \times C_L}{I}$$

$$F_{oM_2} = \frac{SR \times C_L}{I}$$

we can find $F_{oM_{1, CRFC}} = 4F_{oM_{1, RFC}} / 3$ and $F_{oM_{2, CRFC}} = 4F_{oM_{2, RFC}} / 3$. This indicates the GBW and slew rate of the CRFC are improved by a factor of 1/3 compared with the RFC, for the same power and capacitive load.

2.2. Biasing circuit with data-driven scheme

![Figure 2. Biasing circuit of the CRFC amplifier, with the data-driven scheme.](image)

The biasing circuit for the CRFC amplifier is shown in figure 2. Transistors M1-M24 and the current source I1 form the ordinary current mirror biasing circuit. Its current gain is determined by the aspect ratio of the transistors. The OTA is designed for gyroscope readout circuits and A/D convertors, and it can be used in most circuits with capacitive loads such as switched capacitor filters. Generally, the amplifier has two main working modes defined by the virtual ground state of the amplifier. When there's a large input differential signal, charge is transferred among the capacitors and this should be finished in a very short time leading to a demand of large GBW and high SR. However, Eq. (1) and Eq. (2) indicates that better GBW and SR implies larger current. When the input differential signal gets small to near zero, high SR is not necessary since the current through every transistor hardly changes. This state occupies much of the amplifier's operating time and much power which is designed to enhance SR is wasted. To ease this confliction, we propose a data-driven scheme to realize dynamic accommodation of biasing current.

To realize the data-driven scheme, a branch is added to the biasing circuit, which consists of an extra current source, two comparators and two NMOS switches MS1, MS2, as figure 2 shows. The comparators detect the absolute difference of the input signals to the amplifier. If the differential input signal exceeds the threshold of either comparator, for example, letting $V_{INP} - V_{INN} > V_{thres}$, VC1 will be pulled to VDD and NMOS switch MS1 is turned on. Then current I2 will be added into the biasing circuit and the current flowing through the amplifier is enlarged leading to a higher SR. This function is activated when there is a relatively large amount of input differential signal, so it can improve the speed without spending much more power when the amplifier is exploited in angular rate readout circuit. If the input signal is smaller than the comparators' threshold, the circuit settles to a nearly static
mode and both the comparators output zero, shutting off the switches. Then the extra current source cannot be injected to the biasing circuit and the amplifier works at a low power level. Configuring the threshold slightly over zero also helps reduce overshoot when switching from large-current mode to static mode. The data-driven amplifier works somehow like a digital circuit. A digital module in general have very small static current and sharp current pulse only happens when there's digital state change in the circuit. Transplanting digital concept to analog application is a meaningful effort to improve analog performance [15].

3. Simulation results
The performance of the data-driven CRFC OTA was simulated in HJTC 0.18 μm technology. The capacitive load is 5.6 pF and the DC source voltage is 2.5 V.

First, we examined the open loop frequency response of the OTA. When the OTA operates at small-current mode with the data-driven branch cut off, the DC gain is 64.4 dB and the GBW is 23.1 MHz with a phase margin of 79.3°, as shown in figure 3a. The static current flowing through each part of the OTA is listed in table 1. Then we set VC1 and VC2 (see figure 2) to VDD to simulate the frequency response at large-current mode. The result is shown in figure 3b. The DC gain slightly decreased to 61.3 dB, but the GBW increased to 225.3 MHz with a phase margin of 74.4°.

| Circuit part        | Static current / μA |
|---------------------|---------------------|
| Amplifier and biasing | 69.6                |
| Comparators         | 26.8                |
| Total               | 96.4                |

Table 1. Static current of each part of the OTA.

![Figure 3. Frequency response of the OTA.](image)

(a) Data-driven branch cut off.  
(b) Data-driven branch switched on.

Then we simulated the performance of the data-driven scheme. A unity negative feedback testing circuit was constructed to perform a transient simulation, as figure 4 shows. The inputs to the circuit are a pair of differential square waves, with a peak-to-peak voltage of 1 V and a period of 1 μs. We tested the output differential signal with conventional RFC, CRFC and data-driven CRFC. The results are plotted in figure 5. The RFC OTA was scaled at a total current of 68 μA, almost the equal level to the CRFC's main amplifier circuit. The rising time (1% settling time) with RFC is 150.6 ns and that with CRFC is 101.8 ns, i.e. the slew rate of the CRFC is enhanced 1.48 times over the RFC. The transition with data-driven CRFC OTA lasts for 15.8 ns, indicating that the data-driven scheme improved the speed of the capacitive circuit by over 6 times. The OTA operated at large-current mode only for 21.0 ns in a half period, and the average current in this transient analysis is 151.1 μA, less than twice the total static current displayed in table 1.
The performance simulation results are summarized in table 2, compared with previous RFC amplifiers. Assaad et al. first reported the RFC amplifier [9-10], and the CRFC architecture described in this article makes more efficient use of the static current and improves the FoMs. Yan [11], Akbari [12] and Aghaee [13] did efforts to enhance transconductance and slew rate of the RFC structure. The data-driven CRFC OTA presented in this article has the best dynamic FoMs at large differential input, with the smallest static power consumption.

| Parameter             | [10] | [11] | [12] | [13] | This work                      |
|-----------------------|------|------|------|------|-------------------------------|
| Current (μA)          | 400  | 800  | 483  | 300  | Static: 96.4; data-driven: 151.1 |
| Capacitive load (pF)  | 5.6  | 10   | 5    | 2.5  | 6.7                           |
| GBW (MHz)             | 70.4 | 203.2| 650  | 357  | Static: 23.1; data-driven: 225.3 |
| Phase margin (°)      | 79.8 | 66.2 | 50   | 61   | Static: 79.3; data-driven: 74.4 |
| DC gain (dB)          | 59.7 | 54.5 | 59.1 | 75   | Static: 64.4; data-driven 61.3 |
| Average SR (V/μs)     | 48.1 | 91.6 | 115.2| 30   | Static: 12.4; data-driven: 127.5 |
| FoM1 (MHzpF/mA)       | 985.6| 2540 | 6279 | 2975 | Static: 1605; data-driven: 9990 |
| FoM2 ((V/μs) pF/mA)   | 673.4| 1145 | 1193 | 250  | Static: 861.8; data-driven: 5654 |

4. Conclusions
In this article, we developed a data-driven complementary recycling folded cascode OTA for MEMS gyroscope ASIC driving capacitive loads. The CRFC architecture is adopted to make efficient use of biasing current and achieve a better GBW. The biasing current of the OTA is controlled by the data-driven scheme, to enhance the slew rate of the amplifier and increase the speed significantly without much power dissipation when there’s a large input differential signal. A transient simulation was done to confirm the theoretical analysis, showing that the data-driven scheme improved the circuit’s speed by over six times with the power consumption increased by 57%. It is an attempt to combine digital thought with basic analog circuit block, opening a way to acquire high performance and low power simultaneously. This kind of single-stage OTA is suitable for charge amplifiers, A/D convention circuits, switched capacitor applications, etc.
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