Firmware developments on the TileCoM for the Phase-II Upgrade of the ATLAS Tile Calorimeter

M G D Gololo¹, F Carrio Argos², F Martins³ and B M Garcia¹

1 Institute for Collider Particle Physics, University of the Witwatersrand and iThemba LABS;
2 Instituto de Física Corpuscular, University of Valencia; ³Laboratório de Instrumentação e Física Experimental de Partículas
E-mail: mpho.gift.doctor.gololo@cern.ch

Abstract. The Tile Computer on Module (TileCoM) mezzanine board is one of the auxiliary boards of the Tile PreProcessor (TilePPr) for the Phase-II Upgrade of the readout electronics of the ATLAS Tile Calorimeter (TileCal). This board will be responsible for system monitoring and configuration by interfacing the Trigger Data Acquisition (TDAQ) system and the TilePPr. Features include configuration and monitoring of the Advanced Telecommunications Computing Architecture (ATCA) carrier and Compact Processing Module (CPM) onboard sensors through I2C and Gigabit Ethernet. This contribution presents firmware developments on an embedded Linux for the ZYNQ System-on-Chip (SoC) targeting an Avnet Ultra96-V2 ZYNQ UltraScale+ MPSoC evaluation board. This test bench will serve as a basis for the development of the main functionalities of the TileCoM mezzanine board to interface the TilePPr with the Detector Control System (DCS) and the TDAQ-I system of the Tile Calorimeter.

1. Introduction
The upgrade to High Luminosity Large Hadron Collider (HL-LHC) [1] currently taking place at the European Organization for Nuclear Research (CERN) will provide the ATLAS (A Toroidal LHC ApparatuS)[2] experiment with an instantaneous luminosity of $7 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$. The Tile Calorimeter (TileCal) [3] detector is part of the ATLAS experiment with on-detector electronics to read-out signals to the off-detector electronics. The Phase-II Upgrade of TileCal will replace the legacy system with a fully-digital TDAQ-I and trigger processing, reading out the whole detector at 40 MHz at Level 0 trigger level (Figure 1). The DaughterBoard formats and transmits digitized signals to the off-detector electronics every bunch crossing (~25 ns) which leads to significant increase of the data rate.

2. The Tile PreProcessor (TilePPr)
Figure 2 shows the schematic of the control and monitoring of the the Phase-II upgrade electronics through the network. One TilePPr module is connected to eight (8) TileCal modules. The TilePPr sends LHC synchronized clocks and configuration commands to the on-detector electronics, while receiving monitoring information and PMT samples through MGbps optic fibers. The TilePPr provides remote configuration capabilities for the on- and off-detector electronics through the TileCoM. The TileCoM is accessed through the network via a Tile 16 GbE port switch. The TileCoM on the TilePPr is responsible for three main functionalities:
2.1. Field Programmable Gate Array (FPGA) remote configuration through Ethernet

The TileCoM will be used to remotely program the on- and off-detector FPGAs by sending bitstreams through the Xilinx Virtual Cable. This includes the on-detector FPGAs using Xilinx Kintex UltraScale+ and Intel Cyclone IV, CPM FPGAs using Xilinx Kintex UltraScale+ and Artix 7; and TDAQ-I (RTM) FPGAs using Xilinx Kintex UltraScale+ and Artix 7.

![Figure 1. TileCal Phase-II Upgrade[3].](image1)

2.2. Slow control and configuration of the PreProcessors

The TileCoM will also provide slow control and configuration capabilities by monitoring of ATCA on-board sensors, CPM sensors and on-detector electronics sensors through I2C and GbE. This also includes an interface with the TDAQ to monitor and configure the TilePPr and the on-detector electronics.

![Figure 2. TileCal Phase-II Upgrade[3].](image2)

2.3. Communication with DCS system

For this functionality, Open Platform Communications (OPC) Unified Automation (UA) server is implemented on the ARM processor of the ZYNQ SoC to provide sensor monitoring data from PPr and on-detector electronics to DCS.
3. Firmware implemented on the TileCoM evaluation board

Avnet Ultra96-V2 ZYNQ UltraScale+ MPSoC evaluation board is used for the firmware implementation of the TileCoM. These implementations are on both the Processing System (PS) and Programming Logic (PL) of the ZYNQ SoC. Both of these hardware maps can be accessed by implementing a server on the PS of the ZYNQ SoC as detailed below:

3.1. Community Enterprise Operating System (CentOS) embedded linux

CentOS 8 embedded linux is deployed on the PS of the ZYNQ SoC and used as the operating system for all the firmware implementations. Xilinx petalinux tools were used to build the kernel and boot files of the embedded linux. The CentOS 8 root file systems were created separately to boot with the petalinux kernel on the TileCoM evaluation board.

3.2. OPC-DCS interface

Figure 3 shows an interface between the TilePPr and DCS[4]. The TileCoM request monitoring data through Transmission Control Protocol (TCP) from the CPMs. OPC is implemented on a CentOS 8 embedded Linux on the ZYNQ System-on-Chip (SoC) using quasar. An open source OPC UA backend C++ Toolkit called Open62541 is used for the implementation of the server. The DCS request monitoring data from the TileCoM through the OPC server and read-out the required data on the UA Expert as a client.

3.3. Ironman firmware overview

The Ironman[5] software employed in the L1Calo integrated with IPbus[6] is used as a base to implement the firmware for the TileCoM. The software uses standard twisted protocol applications such as a reactor model, which is a global loop that responds to the listeners when events have been triggered in the server (Figure 4). The SoC client analyzes the incoming packet more thoroughly and sends requests to the hardware. The SoC client reads or writes to the PL or the PS depending on the application request. In case of a request to the PL, an internal communication interface is established through the AXI to access the PL of the ZYNQ SoC. The response is sent back to the client through the server.

4. Experimental setup and results

Figure 5 shows a testbench as part of a representation of Figure 2. The testbench shows the connection of the TilePPr modules to the network. This includes the TileCoM evaluation board, the Tile GbE switch and the Tile GbE switch motherboard. Tile GbE switch and the Tile GbE switch motherboard are designed to specifically accommodate the TilePPr modules with up to 16 GbE links. This testbench is a first stage of TileCoM firmware implementation test and it
does not include the CPM module for this stage. All these modules are powered with a 12V DC power supply and connected to the CERN network. The TileCoM is connected to the Tile GbE switch motherboard through the 1 GbE small form-factor pluggable (SFP) to Registered Jack 45 (RJ45) connector. Thus, packets of data sent from the TileCoM evaluation board to the CERN network goes through the Tile GbE switch.

The testbench exhibit the communication achieved between the implemented server and client using Twisted libraries. The IPbus server is implemented directly on the processing system of the ZYNQ architecture of the Ultra96-V2 ZYNQ UltraScale+ MPSoC TileCoM evaluation board. The client is implemented with Twisted libraries and PyQt5 on Ubuntu 18.04 to read out Xilinx Analog-to-Digital Converters temperature and voltages. Figure 6 shows the temperature and voltage in a graphical format. Numpy was used to plot these readings on top of the PyQt5 application. The top plots shows the temperature readings from the temperature sensors of the evaluation board and the bottom plots shows readings from the voltage sensors.

5. Conclusion
The firmware developments presented in this contribution are a test run for the TilePPr development boards for the ATLAS Tile Calorimeter Phase-II Upgrade. The implementation of the IPbus firmware and software on the TileCoM board have been tested with the Tile 16 GbE port switch. These development boards are connected and accessed remotely to read out Xilinx Analog-to-Digital Converters temperature and voltages. These readings are requested from the IPbus running on the TileCoM evaluation board and presented on the client using PyQt5 application, Twisted libraries and numpys.

References
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