A comprehensive review on time-delay compensation techniques for grid-connected inverters

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Abstract
The control of grid-connected inverters is recently executed with digital microprocessors due to the advances in digital signal processing technology. However, the digital realisation has a drawback of the phase lag induced by the time-delay. This phase lag challenges the stability and robustness of the controller of the inverters. In view of the challenge, this paper presents a comprehensive review of time-delay compensation techniques employed in both model-free (MF), and model-based (MB) controls of an inverter in grid connection. MF techniques mainly use proportional-integral, and proportional resonance controllers with some techniques to reduce time-delay. Meanwhile, for MB, this paper discusses the commonly used control techniques, which are the Smith predictor, modified Smith predictor, deadbeat controller and model predictive controller. Several related techniques from the literature that have been adopted to mitigate the delays are tabulated comprehensively, and critical issues regarding the MF and MB techniques are also discussed. Finally, this paper presents a hypothesis on which technique is superior at present and suggests a hybrid technique from the MF and MB techniques to give readers a direction for further research.

1 | INTRODUCTION

In recent times, conventional power systems are experiencing an evolutional change in the traditional way they operate as a result of the increase in energy demand in the world. Therefore, in response to this global demand, grids need to be liberalised for other sources of energy, such as solar and wind, to be integrated. These renewable energy resources have the potential of making an excellent contribution of power to the primary grid if harnessed and utilised fully under a controlled environment. Distributed generation (DG) is becoming a common approach to meet this demand, where DG systems are systematically connected through a power electronic device called grid-connected inverters to form what is called the microgrid. The idea of putting the individual DG together is to have system flexibility, which ensures system optimisation, reliability, protection, integrity, security and power-quality management.

However, the interfacing devices face some challenges in terms of interaction with the grid, especially when the grid is weak [1], and as such, new and stern standards regarding safe running, power quality and islanding protection are discussed in [2]. Therefore, these challenges in the interconnection have attracted so much attention in recent times, and more research works have been conducted due to the discovery of power electronic devices that can switch very fast, and handle high power and the adoption of real-time-based controllers that can implement advanced and sophisticated control algorithms [3]. The adoption of real-time-based controllers has some drawbacks associated with time-delay in the control loop and the delay during the transition between the grid-connected and islanded modes.

Time-delay is a property of a physical system in which the response to an applied force is delayed in its effect [4]. Whenever a control signal or energy is sent from one point to another, a propagation delay is experienced along the channel. The extent of the propagation delay is associated with the speed of the transmitted signal and the nature of the material the signal is passing through. Therefore, presence of a long delay in the...
inverter’s digital control loop or during the transition between the grid-connected and islanded mode makes the controller design and implementation a bit more complicated, making deviations of frequency and voltage more severe. In contrast, a short delay can be easily handled through various compensation techniques.

In grid-connected inverters with LCL filter, the controller can be a voltage, current or direct power control or a hybrid of any of these controls in a cascaded loop with, either inner-loop or outer-loop structure. The inner current control is employed in many research works with the view of ensuring accurate current tracking, adequate control bandwidth and fast transient response. Meanwhile, in voltage source inverters (VSI), the current controller is employed to make the inverter acts as a current amplifier within the current loop bandwidth [5]. Whereas, the voltage controller in the case of the outer-loop structure, is employed to ensure power flow in the system and to reject disturbances from both input sources and the grid. However, the control bandwidth of the current controller is limited by the presence of time-delay in the control loop, especially in digital implementation.

Furthermore, the control of grid-connected inverters is executed with digital microprocessors due to the advances in digital signal processing technology [6]. The digital realisation has some advantages compared with the analogue control in terms of high reliability, more control flexibility and fast re-programmability. However, this digital implementation has some drawbacks, of which the most critically challenging is the phase lag induced in the control loop by the time-delay. This delay will be further intensified if more control loops are used.

Before reviewing some of the commonly used time-delay compensation techniques, it is imperative to understand the leading causes for the existence of time-delay in grid-connected inverter’s control loop. Time-delay in digital controller implementation is mainly caused by controller computational time [7], zero-order hold effect of the digital pulse-width modulation [8] as well as the sampling and updating of the voltage and current quantities for control purposes [9]. Consequently, when there is a significant time-delay in the control loop, achieving high performance seems to be very difficult. As a result, the controller is characterised by a reduced transient response (low-gain cross-over frequency), high overshoot (unsatisfactory phase margin) and reduced control bandwidth. Moreover, this will further contribute toward degrading the performance of the controller as well as instability, to mention but a few.

Therefore, to solve these effects, compensators are employed to reduce or eliminate the delays. Various time-delay compensation techniques have been proposed in the literature, which can be considered as either model-based (MB) or model-free (MF) techniques [6], as shown in Figure 1. MB techniques are more accurate but sensitive to system modelling accuracy, while MF techniques are less accurate but independent of the model’s accuracy. MB time-delay compensation techniques include; the Smith predictor (SP), modified Smith predictor (MSP), the deadbeat controller (DBC), the model predictive controller (MPC), etc. On the other hand, MF techniques included; the damping technique (DT), filter-based technique (FBT) and the technique of shifting the sampling instant (SSI) of the control variable [6]. The contribution of this paper is to highlight the existing problems and the techniques used in mitigating the effect of time-delay in the control loop of grid-connected inverters and also present a direction for future research on further reducing time-delay.

The remainder of this paper is organised as follows: a brief discussion on MF time-delay compensation techniques is presented in Section 2, issues with MF compensation techniques are presented in Section 3, MB time-delay compensation techniques are presented in Section 4, issues with MB compensation techniques are presented in Section 5, analysis of the performance parameters in terms of THD and time-delay is presented in Section 6, and lastly, the conclusion is presented in Section 7.

2 | MODEL-FREE TIME-DELAY COMPENSATION TECHNIQUES

The LCL filter is employed in recent times to replace the conventional L-type filter for grid-connected inverters because of its ability to attenuate high frequency switching harmonics at the output of the inverter. However, this advantage is not without a demerit of causing instability of the system in practical implementation as a result of zero impedance at the resonance frequency [10]. This shortcoming becomes worse when the time-delay effect is considered in the inverter’s control loop. Therefore, a lot of effort has been made by many researchers to solve the oscillation problem of the LCL filter and reduce the time-delay in the control loop concurrently. In the following subsections, commonly used MF techniques for time-delay compensation will be presented.
2.1 Damping techniques

Time-delay in the control loop and the oscillation problem in the LCL filter are solved using damping techniques, which can be divided into passive and active damping techniques. In the passive damping technique, a resistor is added in series with the filter inductor or capacitor to suppress the resonant peak, which in turn stabilizes the system. This technique is cost-effective and straightforward. However, the added resistor causes power loss, reduces the filter effectiveness and degrades the overall performance of the system [11]. Therefore, these drawbacks make this damping technique less acceptable, especially in a weak distribution grid. An alternative to passive damping is the active damping technique, where the measured state variables are used instead of a resistor to damp the oscillations and to compensate for the time-delay. This technique is divided further into two: the inverter-side active damping and the grid-side active damping techniques.

In the inverter-side active damping technique, single, double or multi-loop feedback or feed-forward current or voltage state variables are used to achieve excellent damping and mitigate time-delay in the control loop, as reported in [12–15]. State variable measurements are carried out on the filter capacitor or inductor at the Inverter-side, as shown in Figure 2. Even though good results were reported from this technique, the single-loop technique cannot guarantee stability in the presence of disturbances; at the same time, there is a need for measuring more than one state variable in the double- and multi-loop topologies and that has a cost implication, reduces reliability and has the tendency of increasing the complexity of the controller [10, 11].

In the grid-side active damping technique, a single-, double- or multi-loop grid current or voltage feedback or feed-forward is used, as shown in Figure 2, to damp the oscillation in the system and to mitigate the time-delay. It has been reported that with the grid-side active damping technique, the system is inherently unstable [16]. Therefore, to achieve stability, a time-delay is added in the control loop. This method has been adopted by the authors in [10], and according to them, the time-delay addition effectively stabilizes the system. However, the stability reported in [10] is only valid for a given range of time-delay, which means that the system is unstable when the time-delay is outside the given range. This method is not suitable for grid-connected inverters that require a fast controller with minimum delay.

2.2 Filter-based techniques

In this compensation technique, the measured state variables are fed into the controller through a filter, or a filter is placed in the cascade with the main controller or is connected to filter the voltage reference to the modulator. In either of the modes, the filter can compensate for the phase lag caused by the time-delay without the need for an additional sensor, and this method was adopted in [14, 17–20]. However, this method has drawbacks in terms of noise amplification, complexity in tuning the filter parameters, sensitivity of the filter to parameter variations and high sensitivity to grid impedance variation.

2.3 Shifting the sampling instant of the control variable or PWM updating instant techniques

It is a common practice to sample the state variables at the middle of every turn-on or turn-off time of pulse width modulation (PWM). This way, the average value of variables such as inductor current, capacitor current or grid current is sampled, as shown in Figure 3(a), where $m_s$ is the single-update PWM wave, the single-update PWM wave $m_s(K − 1)$ of the $(K − 1)^{th}$ carrier cycle is loaded at the peak of the $(K − 1)^{th}$ triangular carrier and the duty cycle is expressed as $M(K) = m_s(K − 1)$, where $m_s(K − 1)$ is the duty cycle calculated by sampling values at the peak of the $(K − 1)^{th}$ triangular carrier [20]. In a single update, as shown in Figure 3(a), there are three sampling points: $m_s(K)$, $m_s(K − 1)$ and $m_s(K − 2)$. Whereas, there are five sampling points,
3 | ISSUES WITH THE MODEL-FREE TIME-DELAY COMPENSATION TECHNIQUES

As earlier mentioned, the use of LCL filter has advantages, but it also has disadvantages: some researchers reported drawbacks in passive damping using the resistor in terms of power loss, which make it unsuitable for grid-connected application [22, 26]. Meanwhile, active-damping using the single-loop inverter-side control has been reported to have inherent stability than the grid-side single-loop control when the time-delay effect is ignored [16]. A contrary opinion was reported when a unit delay is introduced to the system [27], wherein the grid-side single-loop control is more likely to be stable than the Inverter-side. Therefore, an inverter-side control cannot be stable without extra active damping. In [11], the researchers considered variable time-delay and reported that when an inverter-side single-loop control is used with very small time-delay, the system is always stable which is called the first stable region and that the system becomes unstable and then becomes stable when time-delay increases, which is called the second stable region if it exists.

The authors in [11, 16, 27] have the opposite conclusion as to whether the grid or inverter-side single-loop control is more likely to be stable as a result of the dependency of the stability on the ratio of the resonance frequency $f_r$ of the inverter output filter to the state variable sampling frequency $f_s$ due to the presence of time-delay. If the maximum time-delay is given by $T_d = \frac{1}{4f_s}$, then the critical frequency according to [11] and [28] is $f_c = \frac{1}{4\times T_d}$ and the resonance frequency should be one-sixth of the switching frequency $f_s$ [22, 29, 30], and a stable region is achieved when $f_c < f_{critical}$ for the inverter-side current control and when $f_c > f_{critical}$ for the grid-side current control. However, this stable region can easily change due to the drop in resonance frequency as a result of grid impedance variation. It has been reported in [21] that a 10% variation in grid impedance may result in an almost 40% drop in resonance frequency, which consequently shrinks the stable region of a controller.

To ensure stability in the inverter system adopting the earlier discussed compensation technique, the LCL filter should be carefully designed in such a way that the resonance frequency($f_c$) falls within the stable region. However, ensuring the said careful design is not practical in actual implementation, since grid impedance variation is unavoidable and can easily cause a shift in the designed value of the resonance frequency or that the value may change when the inverter is plugged into a weak grid [17, 21, 31, 32]. As tabulated in Table 1, it is evident that the damping and the time-delay compensation using the single-loop technique both in the inverter-side and the grid-side cannot guarantee stability because even the first stable region may be too short and become narrow if the resonant frequency changes [26].

To address issues of the damping technique using a single loop in grid-connected inverters, an intuitive method is to widen the stable region in such a way that the system can
accommodate a wider range of resonance frequency variation. Widening the stable region for the Inverter-side current controller means increasing the critical frequency of the output filter, and increasing in the critical frequency will be achieved when the time-delay is further reduced. Whereas, for the grid-side current control, critical frequency needs to be reduced by adding more delays. However, the method of adding delay is not recommended for a system that requires a fast transient response, e.g. a grid-connected inverter. Moreover, adding more delays will further impose more bandwidth limitation on the current controller. Widening the stable region with delay reduction has been adopted using additional active damping terms to the current control loop (multi-loop) using a capacitor current feedback [12, 15, 32], capacitor voltage feed-forward [26, 33], and grid voltage feed-forward [13, 34–37]. Different from what the other of the research employed, the authors in [37] employed a multi-resonant component-based weighted feed-forward scheme, where multi-quasi resonant components are added to extract the fundamental and the objective harmonics. Table 2 gives a summary of the research works that adopt this technique. Even though remarkable good results have been achieved from this technique, there is a cost implication of the additional sensors, reduction in the reliability of the system and increase in the complexity of the controller, in addition to poor disturbance rejection capabilities.

An alternative to using additional damping terms which has a cost implication and reduced reliability is to use an additional filter in series with the current controller, which requires no additional measurement or estimation and can change the phase-frequency response of the LCL filter. Digital filters such as weighted filter predictor [38, 39], first-order filter [32], second-order generalised integrators (SOGI) [14, 40, 41], notch filter, low-pass filter, High-pass filter, and lead/lag filters [42] are employed to reduce or eliminate time-delay in the control filter, low-pass filter, High-pass filter, and lead/lag filters [42] are employed to reduce or eliminate time-delay in the control filter, low-pass filter, High-pass filter, and lead/lag filters [42] are employed to reduce or eliminate time-delay in the control loop technique. The overall assessment of this technique, as tabulated in Table 3, has been very good. However, the achievement relies upon accurate filter parameter design and may be influenced by grid inductance variation or when the system is plugged into a weak grid. Although online parameter estimation can improve robustness, disturbances from parameter estimation will be injected into the inverter, which may affect current quality [19]. Moreover, the filter-based damping method reduces the controller bandwidth, which affects the dynamic performance and the low-order harmonics suppressing ability [43].

### TABLE 1
Summary of damping and compensation using single-loop techniques

| No | Authors | Filter type | Inverter-side/grid-side control | Inner control loop | Outer control loop | Control parameter | Feedback loop | Technique |
|----|---------|-------------|---------------------------------|-------------------|-------------------|------------------|--------------|-----------|
| 1  | [10]    | LCL         | Grid-side                       | PI                | N/A               | I                | GCF          | SLDAT     |
| 2  | [28]    | LCL         | Both                            | PI                | N/A               | I                | ICF, GCF     | SLDAT     |

Notes: LCL: Inductor-capacitor-inductor; PI: Proportional integral; N/A: Not applicable; I: Current; ICF: Inverter-side current feedback; GCF: Grid-side current feedback; SLDT: Single-loop delay addition techniques.

### TABLE 2
Summary of extending stable region techniques (multi-loop)

| S/No | Authors | Filter type | Inverter-side/grid-side control | Inner control loop | Outer control loop | Control parameter | Feedback loop | Feed-forward loop | Technique |
|------|---------|-------------|---------------------------------|-------------------|-------------------|------------------|--------------|------------------|-----------|
| 1    | [15]    | LCL         | Grid-side                       | PR                | PI                | I, V'            | GCF          | GVFF             | ESRT      |
| 2    | [13]    | LCL         | Inverter-side                   | PI                | N/A               | I                | CVFF         | ESRT             | ESRT      |
| 3    | [37]    | LCL         | Grid-side                       | PI                | N/A               | I                | CVFF         | ESRT             | ESRT      |
| 4    | [34]    | LCL         | Inverter-side                   | PI                | PR                | I, V'            | ICF          | CVFF             | ESRT      |
| 5    | [35]    | LCL         | Grid-side                       | PI                | PR                | I, V'            | GCF          | GVFF             | ESRT      |
| 6    | [36]    | LCL         | Grid-side                       | PI                | PI                | I                | CVFF         | ESRT             | QRCT      |
| 7    | [37]    | LCL         | Grid-side                       | PI                | N/A               | I                | CVFF         | ESRT             | ESRT      |
| 8    | [34]    | LCL         | Grid-side                       | PI                | PI                | I, V'            | ICF, GCF     | N/A              | ESRT      |

Notes: LCL: Inductor-capacitor-inductor; L: Inductor; P: proportional; PI: Proportional integral; PR: Proportional Resonant; N/A: Not applicable; I: Voltage; GCF: Capacitor current feedback; ICF: Inverter-side current feedback; CVFF: Capacitor voltage feed-forward; GVFF: Grid voltage feed-forward; ESRT: Extending stable region technique; QRCT: Quasi-resonant component technique.
Another alternative to reducing time-delay is to shift the state variable sampling time toward the PWM duty cycle, updating instants. This technique was adopted in [11, 43, 45], and computational time-delay was minimised. However, undesirable harmonics content may increase, and the controller may be susceptible to aliasing effects due to the asynchronous sampling process [6, 29]. An alternative to the aliasing problem is to update the PWM reference immediately after the computation finishes, which may keep the synchronous sampling process. This method was adopted in [43], where the aliasing effect was avoided. This technique gives a good result when the computation time of the controller is very short, i.e., not exceeding 0.25Ts [33], where Ts is the sampling period. However, this technique is mainly suitable for high-power applications, where the switching and sampling frequencies are relatively low [29]. It has been suggested in [21] that shifting the sampling instant to the middle of the sampling period has more of a tendency of harmonic rejection but introduces a one-period delay. This one-sampling delay can be further reduced to half by adopting a double sampling of the control variable and a double update for the PWM. This technique was adopted in [22], wherein the delay was reduced, but the computation and complexity were increased. In [46], the authors compared and investigated the different types of carriers employed in multi-sampled PWM, which significantly reduce time-delay. It has also been investigated that multi-sampling the control variable and multi-updating the PWM have the tendency of reducing the half-sampling delay introduced by the double sampling, double updating technique to some fractions [24], which does not require an additional cost [47].

Serious attention has been given to this technique in recent times since it is a promising alternative in reducing the phase lag induced by the time-delay and ultimately in breaking the bandwidth limitation associated with digital controllers. This technique was adopted in [48, 24, 47], and recently in [49]. However, the multi-sampling and updating technique has the drawback of injecting high-frequency disturbances in the form of voltage ripples into the feedback loop. Therefore, there is a need to have an additional high-frequency cancellation. Among the simplest and the most straightforward cancellation approach is the use of an antialiasing filter. But this simple approach imposes a reduction in the phase margin of the controller and consequently limits the so-called advantages of the MSMU techniques.

The research in [47] investigated and proposed the ripple elimination technique, which does not waste the excellent phase margin associated with the MSMU technique. The authors used a repetitive ripple estimation approach to subtract the noise from the sampled error signal. The drawback of this technique is that the controller being used, which is PI, has some limitations regarding disturbance rejection and cost implication for the FPGA used. There is a need to test this approach with other promising types of controllers. The author in [48] used the quadruple-sampling, and updating technique (QSQU) for a single-phase active filter and employed three types of current controllers: the P-controller, the DC controller and the modiﬁed DBC. Good results were achieved in this work, but there is a need to apply this quadruple-sampling to an inverter system, especially the grid-connected type. The drawback is that this technique was implemented on two FPGAs, which has a cost implication. Therefore, there is a need to investigate the possibility of its implementation on a micro-controller, which is cheaper and easier to handle. In [50], the authors conducted research on MSMU carrier-based PWM for multi-level active shunt power filters, but this research merely measured the signals at the peak and valley of each triangular carrier, therefore limiting the dynamics of the multi-level converter. In [24], the authors conducted a comprehensive analysis of the multi-sampling method for a high-power grid-connected inverter with an LCL filter. But this research did not consider the drawbacks of MSMU mentioned earlier.

Recently, the authors in [49] proposed a method of implementing MSMU with minimum sampling interval, which the authors believed avoids sampling the current ripple caused by the switching action and breaking the voltage-second balance in the modulation process. The drawback is that this research considered the single-phase L-type filter only and the PR current
controller used in the study had complexity in tuning the gains and had a lack of robustness in the presence of multiple disturbances. There is a need to try this technique using an LCL filter with other types of controllers. Table 4 gives a summary of the techniques.

All the aforementioned MF time-delay compensation methods in the literature under review in this paper were implemented with cascaded conventional proportional controller (P), proportional integrator controller (PI) or proportional resonant controller (PR). As either an inner-loop or outer-loop controller or a combination of inner and outer-loop control schemes, as shown in Figure 4. Even though satisfactory performance has been reported, the controllers used have shown reduced accuracy and stability when handling time-varying signals, in addition to the poor disturbance rejection ability and slow response to abrupt changes to grid impedance variation and complexity in tuning for the sinusoidal signal [52]. However, some modifications have been proposed to the traditional controller, such as the additional capacitor voltage feed-forward, grid voltage feed-forward and multiple-state variable feedback. These modifications can only expand the controller bandwidth at the expense of the controller stability margin [52]. Therefore, there is need to investigate these time-delay mitigation methods further using more robust controllers that can give a faster response, wider stable region, zero steady-state error, better time-delay mitigation ability, better disturbance rejection and high adaptability to the weak grid, while keeping simplicity and cost implication in mind.

In conclusion, MF techniques using PI or PR controllers cannot guarantee stability in the presence of multiple disturbances especially when there are a time-delay and grid impedance perturbation at the same time, which are common in micro-grids as a result of connected inverters. This effect translates through the system and causes a resonance frequency shift in the output filter, which in turn shrinks the stable region of the controller. Therefore, there is need to adopt these techniques using a more robust controller, which give a wider stable region and faster responses.

### 4.1 MODEL-BASED TIME-DELAY COMPENSATION TECHNIQUES

In grid-connected inverter current control, predictive current controllers (PCCs) have demonstrated good advantages in terms of fast and dynamic response, low-order current harmonic rejection, zero steady-state error, robust time-delay compensation and easy implementation on a digital control system [52]. Among the ones reported in the literature are the SP [53], MSP [54], MPC [55], hysteresis band controller (HBC) [56], DBC, and H-infinity controllers [57] etc. This paper focuses on the common controllers used for time-delay compensation in grid-connected inverters, which are the SP, MSP, DBC and MPC. These controllers are called model-based because they rely on an accurate model of the system to carry out predictions in an attempt to null the error in a given period. As such, these controllers tend to be very sensitive to model accuracy.

The uncertainty in the plant model has several origins which can be broadly classified into two groups; the

### TABLE 4 Summary of different sampling and updating techniques

| S/No | Author   | Filter type | Inverter-side/grid-side control | Inner control loop | Outer control loop | Control parameter | Feedback loop | Feed-forward loop | Techniques          |
|------|----------|-------------|---------------------------------|-------------------|-------------------|-------------------|---------------|------------------|---------------------|
| 1    | [11]     | LCL         | Both                            | PI                | N/A               | I                 | GCF, ICF    | N/A              | SSITUT              |
| 2    | [49]     | L           | Grid-side                       | PR                | N/A               | I                 | GCF         | N/A              | MSMU                |
| 3    | [12]     | LCL         | Grid-side                       | PI                | N/A               | I                 | CCF, GCF    | GVFF             | MSMU                |
| 4    | [22]     | LCL         | Inverter-side                   | N/A               | QPI               | I, V              | ICF         | N/A              | DSDU                |
| 5    | [24]     | LCL         | Inverter-side                   | PI                | PI                | I, V              | ICF         | N/A              | MSMU                |
| 6    | [43]     | LCL         | Inverter-side                   | PR, PI            | N/A               | I                 | ICF         | GVFF             | UIAC                |
| 7    | [51]     | LCL         | Inverter-side                   | N/A               | PI                | I                 | ICF         | N/A              | SSITUT              |
| 8    | [45]     | L           | Grid-side                       | PI                | N/A               | I                 | GCF         | GVFF             | SSITUT              |

Notes: LCL: Inductor-capacitor-inductor; PI: Proportional integral; PR: Proportional Resonant; QPI: Quasi-proportional integral; N/A: Not applicable; I: Current; V: Voltage; ICF: Inverter-side current feedback; CCF: Capacitor current feedback; GCF: Grid-side current feedback; GVFF: Grid voltage feed-forward; SSITUT: Shifting sampling instant toward PWM update time; UIAC: Update immediately after calculation finished; DSDU: Double-sampling, double-updating technique; MSMU: Multi-sampling, multi-updating technique.
parametric uncertainty and the neglected and un-modelled dynamics uncertainty [58]. In parametric uncertainty, the structure of the model is known, but some of the parameters are unknown. Whereas, in the case of neglected and un-modelled dynamics uncertainty, the model has errors because of some missing dynamics, usually at high frequency, either through deliberate neglect or because of a lack of understanding of the physical system. It worth noting that any model of a real system will contain these sources of uncertainty [58]. Even though there are techniques adopted to take care of the errors in the model, some researchers believed that the known sensitivity to parameter variation does not represent a serious problem because, in practice, the variation is very small to cause significant performance degradation [59], as reported in [60].

On the other hand, many researchers believed that the variation is significant and should be given intention. The techniques reported in the literature that handle the variation are the use of a Luenberger observer in the controller formulation [61–63], and the use of line voltage estimation strategy adopted in [64], which was an extension of the analysis initially presented in [65]. In addition, a modified estimation technique for line voltage was proposed in [66], which showed an improvement in the robustness against model error. In [67], the authors used an adaptive uncertainty observer to handle model sensitivity in the system, which improved the stability of the system. In [68] and [69], the authors used neural network estimator and disturbance estimator to improve the robustness against filter inductance mismatch, as reported in [70]. In [71], the authors argued that the sensitivity of the controller to uncertainties increases when the grid voltage is estimated, especially when the grid voltage estimator dynamics depends on the system parameter, as in the case of [64–66], and they proposed a novel neural network interfacing parameter identifier with a neural network grid voltage estimator, which is believed to be a promising alternative. In [72] and [73], the researchers proposed an online inductance identification method, which is believed to take care of the model’s parameter variation. In [74], the authors proposed the use of a virtual damper to increase the robustness against parameter variation. The research of [58] presented an overview of different ways to define uncertainty and proposed H-infinity ($\mathcal{H}_\infty$) frequency domain approach that handles parametric uncertainty. The following subsections discuss the essential operation of the controllers.

### 4.1 Smith predictor

At first, Smith proposed a method of compensating time-delay using a mathematical model of a system by adding a minor feedback loop around the conventional controller, called the Smith predictor, as shown in Figure 5 [75], where $R(s)$ represents the input to the system, $Y(s)$ the output and $D(s)$ the disturbances. Block $C(s)$ represents the conventional controller, while block $P(s)e^{-ds}$ represents the plant, where $P(s) = C(sI - A)^{-1}B$, and $Z(s)$ represents the so-called minor feedback, which can be mathematically represented as $P(s) - P(s)e^{-ds}$ [75].

![FIGURE 5 Smith predictor](image)

Using the Smith predictor, the model of a process is used to predict the future output value. Many industrial processes celebrated this achievement because it was able to eliminate the time-delay from the characteristic equation of the system’s closed-loop. Therefore, a controller design problem for a system with delay can be modelled to the one without time-delay. However, despite the achievement by this controller, the Smith predictor controller is unable to remove delay from the closed-loop characteristic equation of unstable systems [4]. This drawback motivated research, which brought improved methods of handling time-delay effects in unstable systems such as the modified Smith predictor, as shown in Figure 6 [54, 76–78], finite spectrum assignment [79, 80] and internal model control [81, 82]. Because the conventional Smith predictor is unable to control unstable systems and is coupled with a high requirement of a dynamic system model, many modifications have been done by researchers to improve its robustness. It worth noting that the topology of the modified Smith predictor is not unique in the literature. Several topologies are available, with the simplest and most straightforward to understand are those reported in [76–78]. The modified Smith predictor in Figure 6 was proposed in [76], where the authors added a low-pass filter (LPF) in the outermost feedback loop to mitigate the fluctuations in the process output. Three controllers were proposed, shown as $C(s)$, $C_1(s)$ and $C_2(s)$, with the aim to achieve the set point faster, minimise the oscillation, if any, and eliminate the oscillation during the load recovery, respectively. $\mathcal{P}_m(s)e^{-m\omega}$ is the model, where $e^{-m\omega}$ represents the estimated process deadtime. Consequently,
an enhanced set point tracking, along with faster load rejection, was achieved in this research work.

Despite the broad adoption and the satisfactory performance of the SP and MSP techniques in mitigating time-delay in industrial processes, their applications in the grid-connected inverter systems are minimal. Therefore, there is a need to investigate this time-delay mitigation method further for grid-connected inverter applications. In recent times, research on time-delay compensation in grid-connected inverters have given attention to predictive controllers because of their simplicity and easy implementation on microprocessors and digital signal processors (DSPs). These controllers calculate the control variable ahead of time based on the differential equation and then used the calculated control signal to cancel the error in some sampling periods, provided that good modelling is achieved.

### 4.2 Deadbeat controller

Predictive controller’s cover a vast range of controllers. Different classes of predictive controllers and their basic algorithms in inverter applications are presented in detail in [83]. In power electronics applications, the predictive controllers try to determine the control path for the current vector, which is usually at the beginning of the pulse period and then tries to use the determined current vector to generate an appropriate voltage vector by PWM so that the predicted error is minimised. Therefore, when a voltage vector is selected to cancel the predicted error at the end of the pulse period, this predictive controller is called a DBC [5, 84].

DBC increases the step response speed of the system by manipulating the input variable in two ways. The first is to allow the large-signal (positive) to proportionally drive the system response very fast to attend the original constant value. Then, a delayed smaller step signal (negative) follows, which targets to cancel the transient response remainder from the former large step signal [85]. This type of controller makes a prediction which is targeted to reach its output reference value at the end of the next switching period; such consideration introduces one sampling of time-delay. The prediction in this type of control is based on a complete or simplified model of the system employing either model prediction or generalised prediction concept. Therefore, a modulator is required, as shown in the block diagram of Figure 7, in order to apply the desired voltage vector to the inverter, since the output of this type of controller is a continuous value (average value) [86]. In addition, discretisation of the model is required for digital implementation.

Moreover, regarding the application of DBC in grid-connected inverters, it can be broadly classified into two main classes. The first class does not consider the effect of time-delay in modelling the system, where the effect is assumed to have no impact on the stability and robustness of the system. The summary of such related literature is tabulated in Table 5.

The second class of DBC considers the effect of time-delay in modelling the controller, and its impact regarding stability, sensitivity to parameter variation and other disturbances are investigated by adopting some techniques to mitigate the delay in the control loop. The summary of such related literature is tabulated, as shown in Table 6.
4.3 Model predictive controller

MPC is very similar to DBC on the prediction of the system response based on control variable changes in such a way that a minimum error is achieved in the next one or more sampling periods. This type of controller gives a discrete output, which can be easily applied directly to control the converter without discretisation, on like the DBC where discretisation is required. The output is chosen by minimising the cost function, which represents the error between the current and the desired reference, as well as the DC-link voltage error [89]. Measurement is necessary to be carried out at the middle of the sampling period (average value) because the control applies directly one voltage vector for the whole sampling interval. This way, 0.5Ts’s delay is introduced, which can be easily compensated by the controller. In [99], the authors used a long horizon prediction approach to compensate for the computational delay in the control loop of a multi-level inverter. In the research work of [100], the authors employed a simple prediction algorithm technique utilising the reference signals with several switching periods ahead to eliminate the time-delay in the control loop.

5 ISSUES REGARDING THE MODEL-BASED TIME-DELAY COMPENSATION TECHNIQUES

The SP and MSP techniques for time-delay compensation are built using P, PI, and PR controllers; as such, the controller lacks the robustness required to meet the grid connection standard and industrial code due to the intermittent nature of the primary source of energy in the distributed generation units [44]. The main drawbacks of this method include reduced stability and accuracy in handling time-varying signal, sluggish response to sudden disturbances, sensitivity to controller gain and parameter changes and poor disturbance rejection ability. These drawbacks make this technique decidedly less suitable for grid-connected inverters. At the same time, the DBC has issues regarding one-sampling delay, sensitivity to model uncertainties, parameter mismatches, noise on the sensed variables and unpredicted disturbances (from the DC-link voltage and grid impedance) [96].

Many topologies have been presented to overcome the limitations of DBC, such as the double-, quadruple- and multi-sampling and updating techniques to overcome the one-sampling delay. Adaptive model is designed to relax parameter sensitivity and parameter mismatches, a filter is added in series with the sensing devices to filter the noise, and disturbance estimator is used to reject unpredicted disturbances. However, some research works combined two different controllers in their design, for instance, DBC in the inner current or power-loop and the outer-loop is controlled by other types of controllers such as the PI, or in some cases, the DC-bus is assumed as an ideal constant DC voltage source (no outer-loop control). Furthermore, some research works assumed that the effect of time-delay on the controller is negligible. Therefore, its impact on the resonance frequency shift and the stability of the system is ignored. Such literature is summarised in Table 5. However, the assumption of the ideal DC voltage source and the negligible effect of time-delay in the digital controller design leads to reduced performance of the system and the lack of robustness of the controller against disturbances. On the other hand, some research works had taken account that renewable energy sources cannot be assumed to be an ideal constant voltage source. Therefore, they considered the effect of time-delay in their research work, where the delay was drastically reduced using different techniques as tabulated in Table 6.

However, some research works only considered the time-delay effect but assumed an ideal constant DC-source, such as

### Table 6: Summary of DBC considering time-delay effect

| S/No | Author  | Filter type | PWM update | Inner current loop controller | Outer control loop | Control parameter | Feedback | Feed-forward | Technique |
|------|---------|-------------|------------|-------------------------------|-------------------|-------------------|-----------|--------------|-----------|
| 1    | [5]     | L           | Single     | DBC                           | N/A               | I                 | SL        | N/A          | TNE       |
| 2    | [20]    | LC          | Double     | DBC                           | PI                | I, V              | DL        | N/A          | DSDU/FBT  |
| 3    | [94]    | LC          | Single     | PI                            | N/A               | I                 | SL        | N/A          | SO        |
| 4    | [52]    | L           | Single     | DBC                           | N/A               | I, V              | SL        | N/A          | TNE       |
| 5    | [84]    | N/A         | Single     | 1, LP, 2, SP                  | N/A               | I                 | SL        | N/A          | SPT       |
| 6    | [85]    | L           | Single     | SP                            | N/A               | I, V              | SL        | N/A          | SPT       |
| 7    | [95]    | L           | Multiple   | DBC                           | N/A               | I, V              | N/A       | N/A          | MSMU      |
| 8    | [59]    | L           | Multiple   | DBC                           | N/A               | I, V              | N/A       | SL           | MSMU      |
| 9    | [71]    | LC          | Single     | DBC                           | ANN               | I, P, Q           | SL        | N/A          | NCO       |
| 10   | [96]    | LC          | Single     | DBC                           | DBC               | I, V              | ML        | DL           | SO        |
| 11   | [97]    | LCL         | Single     | DBC                           | N/A               | I                 | SL        | SL           | TNE       |
| 12   | [98]    | L           | N/A        | N/A                           | DB                | P, Q              | SL        | N/A          | TNE       |

Notes: L: Inductor; LC: Inductor capacitor; LCL: Inductor-capacitor-inductor; PI: Proportional-integral; SP: Smith predictor; LP: Linear predictor; N/A: Not applicable; I: Current; V: Voltage; P: Active power; Q: Reactive power; DBC: Deadbeat controller; ANN: Artificial neural network; TNE: Techniques not explicit; SL: Single loop; DL: Double-loop; ML: Multi-loop; DSDU: Double-sampling double-updating technique; MSMU: Multi-sampling multi-updating technique; SPT: Smith predictor technique; NCO: Natural current observer technique; SO: State observer.
the research in [5, 51, 84, 85] and [71–98], where the outer-loop voltage control was neglected, which may have severe effects on the overall performance of the controller in the presence of any unpredicted disturbances. At the same time, two research works considered both the non-ideal nature of the DC sources and the time-delay effect, such as the research in [71], where DBC was adopted for the inner current control, and artificial neural network (ANN) was used for the outer power-loop control. Good results were achieved in this research, where the grid voltage sensorless interfacing scheme designed was inherently self-commissioning, self-tuning and guaranteed optimal performance of the system with reduced time-delay. However, the result was characterised by a one-sampling delay, which can be further reduced by adopting double- or multi-loop updating time-delay technique. Furthermore, the influence of grid impedance was not considered in this research, which may challenge the stability of the system.

In another research [96], the author considered a two-cascaded-loop topology, where DBC was adopted in both the inner current loop and the outer voltage loop. A state observer was employed to mitigate the time-delay, and a disturbance observer was used to rejecting load current disturbances. Good results were achieved in this research work. However, the state observer employed was sensitive to changes in the system parameter in addition to the inherent modelling error and large prediction error [12]. Moreover, this research work was applied to the off-grid system. Therefore, the stability, when applied to grid-connected inverters, has not been investigated so far.

6 | ANALYSIS OF PERFORMANCE PARAMETER IN TERMS OF THD AND TIME-DELAY

In recent times, renewable energy sources are being integrated into the main grid using different types of power electronic devices in an attempt to meet global energy demand. However, if the quality of the power generated by the renewable energy sources to the main grid is not good, the grid becomes polluted, which create a serious problem on the power system and equipment at the consumer end. For grid-connected inverters, especially the high power rated with low switching and sampling frequency, the output current is severely affected by grid voltage distortion, grid impedance variation and time-delay in the control loop [101]. Furthermore, if the current injected into the grid by the renewable energy resources contains a large number of harmonics, grid voltage distortion and time-delay effect in the control loop will be further intensified, which degrades system efficiency and the controller’s performance.

Current and voltage total harmonic distortion has been the measure with which the quality of the generated energy sent to the grid is measured [102]. Therefore, IEEE Standard 1547–2003 provides that the current and voltage THD should be less than 5%. It should be noted that current THD is inversely related to switching frequency. Therefore, in the case of a high-power system, which is always the case for grid-connected inverters with switching frequency less than 5 kHz and with a low inductance of less than 0.5 mH, achieving low current total harmonic distortion (CTHD) and minimum time-delay needs an extra effort [35]. Table 7 shows the summary of the performance parameters of the model-free techniques discussed earlier, which indicates that the switching frequency range from 2 to 16 kHz and the sampling frequency is in the range of 5 to 20 kHz, which is equivalent to a maximum time-delay of 200 to 50 µs, respectively.

The CTHD from the literature under consideration are mostly within the acceptable limit. However, there is room for improvement toward a lower minimum CTHD value by further reducing the time-delay using the various techniques reported in Sections 2 and 4. Regarding the minimum time-delay, as observed in Tables 7 and 8, most of the research works did not indicate the minimum time-delay achieved from the compensation technique adopted. Therefore, this will limit the horizon for making a conclusion on which technique has the minimum time-delay. Furthermore, the lack of this information will limit the vision for further research work on improving further what has been achieved. In conclusion, explaining the procedure intuitively for measuring time-delay in a grid-connected control loop from the model-free techniques reported in this paper could be a future research direction.

The performance parameters of the model-based time-delay compensation techniques discussed in Section 4 are summarised in Table 8. The sampling frequency and the switching frequency are in the range of 2–30 kHz and 2.5–28 kHz, respectively, as observed in Table 8. It is evident from the table that minimum CTHD is achieved when the time-delay is considered in the system modelling and controller design as compared with when the time-delay effect is ignored. Regarding the time-delay, there is no clearly defined protocol for measuring the time-delay, and the exact value of the minimum delay achieved by adopting a particular compensation technique in most of the research works under consideration. However, there is always a general comment from the reviewed literature that time-delay has been reduced or eliminated. Therefore, considering the CTHD as a measure, the authors conclude that deadbeat control with the multi-sampling, multi-updating technique achieves the minimum time-delay in the control loop.

7 | CONCLUSIONS

In this paper, analytical contributions from previous research on time-delay compensation techniques in the control loop of grid-connected inverters are comprehensively summarised. This review is classified based on the dependency of the controller to the model of the system (MF and MB), where MF was found to be more adopted in this area of research because of its simplicity and average performance despite the challenges in terms of the stability of the system in both the inverter-side and grid-side topologies. Many techniques to compensate for time-delay and improve the stability of the system with a minimum number of sensors and less complexity were presented, but the robustness of these types of controllers is not guaranteed in the presence of disturbances or when the system is plugged into a weak grid.
The model-based techniques were reviewed, where it was found that the Smith predictor and the modified Smith predictor were the earliest methods adopted in compensating the effect of time-delays based on conventional PID controllers. The drawbacks of these types of controllers in terms of handling time-varying signal and poor disturbance rejection make this technique less applicable to grid-connected inverters. In contrast, DBC has been adopted recently because of its fast current tracking, zero steady-state error, time-delay compensation and disturbance rejection capabilities. This technique is considered into two groups, as reported in this paper, on whether the time-delay effect is considered in the controller design or not. From the review of research works that examined the impact of time-delay, it can be found that many research works assumed that the DC-link voltage and grid voltage are constant, where the outer loop is not included in the controller design. However, only two
| S/No | Author | Type of inverter | Disturbances | CTHD (%) | Time-delay | Switching frequency | Sampling frequency |
|------|--------|------------------|--------------|-----------|------------|--------------------|-------------------|
| 1    | [5]    | N/A              | LIV, LRV, BEMF | 0.93      | N/A        | 6.7 kHz            | N/A               |
| 2    | [20]   | 3 φ, 50 kW       | GCV, FIV     | 2.4       | 30.7 µs    | 10 kHz             | 10 kHz            |
| 3    | [52]   | 1 φ, 10 kW       | GVV, MM      | N/A       | 50 µs      | 10 kHz             | N/A               |
| 4    | [84]   | 3 φ, 5 kW        | N/A          | N/A       | N/A        | 28 kHz             | N/A               |
| 5    | [85]   | 3 φ, 75 MW       | MM, RCV      | N/A       | *23 ms     | N/A                | N/A               |
| 6    | [96]   | 1 φ, 2 kVA       | LV, RCV      | 4.1       | N/A        | 15 kHz             | 30 kHz            |
| 7    | [71]   | 3 φ, 10 kVA      | LIV          | 0.95      | N/A        | 6.7 kHz            | 8.16 kHz          |
| 8    | [95]   | 1 φ, 3 kVA       | PRCV, ARCV   | <1        | N/A        | 20 kHz             | N/A               |
| 9    | [95]   | 1 φ, 3 kVA       | RCV          | <1        | N/A        | 20 kHz             | N/A               |
| 10   | [97]   | 3 φ, 3 kW        | ARCV, GSC    | 1.2       | N/A        | 20 kHz             | 20 kHz            |
| 11   | [98]   | 1 φ, 1.5 kW      | PE, PAS      | 7.03      | N/A        | N/A                | 2 kHz             |
| 12   | [94]   | 3 φ, 1.5 kW      | SCA          | N/A       | 3 kHz      | N/A                | N/A               |

**Summary without time-delay**

| S/No | Author | Type of inverter | Disturbances | CTHD (%) | Time-delay | Switching frequency | Sampling frequency |
|------|--------|------------------|--------------|-----------|------------|--------------------|-------------------|
| 1    | [89]   | 3 φ, 300 kVA     | FE, PJ, AE   | N/A       | N/A        | 2.5 kHz            | 5 kHz             |
| 2    | [87]   | 1 φ, 3.3 kW      | HIC          | 5.00      | N/A        | 10 kHz             | N/A               |
| 3    | [88]   | 3 φ, 100 kW      | LIV, LRV     | *2.01     | N/A        | 10 kHz             | N/A               |
| 4    | [90]   | 3 φ, 1.5 kW      | P, QV        | *9.66     | N/A        | N/A                | 2 kHz             |
| 5    | [86]   | 1 φ, 1 kW        | LIV, LRV     | 4.96      | N/A        | 3.3 kHz            | 5 kHz             |
| 6    | [91]   | N/A              | GVV          | 1.4       | N/A        | N/A                | N/A               |
| 7    | [92]   | 1 φ, N/A         | GVV          | N/A       | N/A        | N/A                | N/A               |
| 8    | [93]   | 1 φ, 1.5 kW      | RCV, MM, GVV, V_{DC,V} | 3.38 | N/A | 20 kHz | N/A |

Note: LIV: Load inductance variation; LRV: Load resistant variation; BEMF: Back EMF; GCV: Grid current variation; FIV: Filter inductance variation; GVV: Grid voltage variation; MM: Model mismatch; N/A: Not application; RCV: Reference current variation; LV: Load variation; PRCV: Phase reference current variation; ARCV: Amplitude reference current variation; GSC: Grid short circuit; HIC: High inrush current; V_{DC,V}: V_{DC} variation; PE: Power error; PAS: Power angular shift; FE: Frequency excursion; PJ: Phase jump; AE: Amplitude excursion; P, QV: Active and reactive power variation; SCA: State change in active power.

Research works considered the intermittent nature of the DC-link voltage, external disturbances and time-delay effect at the same time. It is worth noting that most of the primary sources of grid-connected inverters are renewable energy resources, which are not ideal constant DC sources. Therefore, making assumptions of a constant DC source and ignoring the effect of time-delay on the stability of the system may lead to misleading results when implemented. Also, the influence of grid impedance variation has to be seriously considered when designing a controller in order to have good controller bandwidth.

Therefore, the authors of this paper propose a direction for further research by blending some of the methods proposed and tested from the MF time-delay compensation with DBC: (1) Implementing DBC in both the inner and outer loops with QSQU, (2) implementing DBC in the inner loop and Fuzzy logic in the outer loop, with QSQU and (3) implementing DBC in the inner loop, and MPC in the outer loop, with QSQU. These hybrids have the tendency of producing a controller with fast transient and dynamic response, minimum control-loop time-delay, good output current with minimum total harmonic distortion and high adaptability to various disturbances and parameter variations, which will guarantee the stability of the system adopting an LCL output filter. This type of controllers are lacking at present based on the literature reviewed.

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