Abstract—Bundle adjustment (BA) is a fundamental optimization technique used in many crucial applications, including 3D scene reconstruction, robotic localization, camera calibration, autonomous driving, space exploration, street view map generation etc. Essentially, BA is a joint non-linear optimization problem, and one which can consume a significant amount of time and power, especially for large optimization problems. Previous approaches of optimizing BA performance heavily rely on parallel processing or distributed computing, which trade higher power consumption for higher performance. In this paper we propose $\pi$-BA, the first hardware-software co-designed BA engine on an embedded FPGA-SoC that exploits custom hardware for higher performance and power efficiency. Specifically, based on our key observation that not all points appear on all images in a BA problem, we designed and implemented a Co-Observation Optimization technique to accelerate BA operations with optimized usage of memory and computation resources. Experimental results confirm that $\pi$-BA outperforms the existing software implementations in terms of performance and power consumption.

Index Terms—bundle adjustment, SLAM, structure from motion, FPGA

I. INTRODUCTION

Bundle adjustment (BA) is the problem of refining a visual reconstruction to produce jointly optimal 3D structure and viewing parameter, including camera pose and calibration, estimates. Optimal means that the parameter estimates are found by minimizing some cost function that quantifies the model fitting error, and jointly means that the solution is simultaneously optimal with respect to both structure and camera variations [1] [2]. Given a set of measured image feature locations and correspondences, the goal of BA is to find 3D point positions and camera parameters that minimize the reprojection error. This optimization problem is usually formulated as a non-linear least squares problem, where the error is the squared L2 norm of the difference between the observed feature location and the projection of the corresponding 3D point on the image plane of the camera. However, we are not limited to using the L2 norm; even when robust loss functions like Huber norm are used, the problem can be cast as a re-weighted non-linear least squares problem. In essence, BA is a large sparse geometric parameter estimation problem, the parameters being the combined 3D feature coordinates, camera poses and calibrations.

BA is widely used in many modern applications. Firstly, BA is the core component of 3D scene reconstruction applications: Agarwal et al. present a system that can match and reconstruct 3D scenes from extremely large collections of photographs such as those found by searching for a given city on Internet photo sharing sites [3]. The authors designed and implemented a cluster with 500 compute nodes to reconstruct cities consisting of 150K images in less than a day. In addition, BA is crucial in robotic localization applications: Mur-Artal et al. developed a feature-based simultaneous localization and mapping (SLAM) system, ORB-SLAM. The system consists of four modules, including tracking, mapping, relocalization, and loop closing. BA is used in the mapping stage for optimizing the visual feature map such that the robot can better localize itself [4]. Moreover, BA is used heavily in autonomous driving applications, especially in the production of high-definition maps [5]. BA is also used in space exploration mission as well, in multiple Mars exploration missions, NASA utilized BA technology to generate and optimize Mars explorer localization accuracies [6]. BA is also used in commercial products, such as Google street map, to perform scene reconstruction optimization [7].

In both online real-time localization applications and offline visual reconstructions applications, BA remains the primary performance and power consumption bottlenecks: for real-time localization systems (including mobile robots, autonomous vehicles, and space explorers) that perform local BA involving tens to hundreds of images, the latency of BA can be extremely high and thus fails to provide optimal localization updates in real-time. For offline visual reconstruction systems (including 3D scene reconstruction, street view maps, high-definition maps) that perform global BA involving thousands to millions of images, the power consumption of BA can be extremely costly. Previous approaches of optimizing BA performance heavily rely on parallel processing or distributed computing, which trade higher power consumption for higher performance. Nonetheless, to enable effective and efficient both online and offline applications, we need a BA solution that simultaneously optimize for performance and power consumption, and thus we explore hardware acceleration techniques.

In this paper, aiming to achieve optimal performance and power efficiency for BA, we present $\pi$-BA, the first hardware-software co-designed BA engine on an embedded FPGA-SoC. The contribution of this paper is three-fold: first, this paper is the first exploration study of implementing a BA hardware accelerator, and the proposed $\pi$-BA’s implementation has been
proven effective. Second, based on our key observation that not all points appear on all images in a BA problem, we developed a novel Co-Observation Optimization technique for designing BA hardware accelerators. Third, in addition to achieving performance and power efficiency, we also demonstrate that the proposed \(\pi\)-BA optimizes computing and memory resource usage.

The rest of this paper is organized as follows. In Section II, the related research works are presented. In Section III, we review the fundamentals of BA problems to help readers understand the challenges and complexities of designing BA hardware accelerators. In Sections IV and V we describe the \(\pi\)-BA architecture and delve into the novel Co-Observation Optimization design. In Section VI, we share the detailed experimental methodologies and results to demonstrate the effectiveness of \(\pi\)-BA architecture. Finally, we summarize the conclusions in Section VII.

II. RELATED WORK

In this section, we review several existing approaches of optimizing BA performance. First, to optimize BA performance on CPU, Jeong et al. exploit the block-sparsity pattern that arises in a reduced camera system and enhance the computational speed of the bundler with BLAS library matrix operations accelerations, efficient memory handling, and fast block-based linear solving [8]. Furthermore, the authors proposed novel embedded point iterations, which substantially improved the convergence speed by yielding a high cost decrease from each camera update step. In addition, the experimental results show the improved performance of the proposed bundler and provide useful and detailed comparisons among various choices when compositing a bundler.

Parallel processing using multicore, either on CPU or GPU, can be applied to optimize BA performance. Wu et al. presented multicore solutions to the problem of bundle adjustment that run on currently available CPUs and GPUs [9]. The authors concluded that using multicore systems deliver a 10x to 30x boost in speed over existing systems while reducing the amount of memory used. This was achieved by carefully restructuring the matrix vector product used in the PCG iterations into easily parallelizable operations. This restructuring also opens the door to a matrix free implementation which leads to substantial reductions in the memory consumption as well as execution time. The authors also showed that single precision arithmetic when combined with appropriate normalization gives numerical performance comparable to double precision based solvers while further reducing the memory and time cost. The resulting system enabled running the largest bundle adjustment problems to date on a single GPU.

Distributed computing is another effective way to optimize BA performance. Eriksson et al. proposed a consensus framework to deal with large scale bundle adjustment in distributed system [10]. Instead of merging small problems by the optimization of overlapping regions of small problems, the consensus framework utilizes the proximal splitting method to formulate the bundle adjustment problem, in which the small problems are merged by averaging points in fact, decreasing the cost of merging. The merging process for the same parameters guarantees the consensus of points in different nodes. This design may suffer from several problems. Firstly, in each iteration, each node in the distributed system has to broadcast all overlapping points to the master node to complete the merging process, which is a huge overhead for large scale data-sets. Secondly, parameters of each camera are independent of parameters of other cameras. However, in practice, some cameras may share the same intrinsic parameters. Thirdly, the method by merging points converges a little slowly in very large scale data-sets and may converge in a local minimum early.

Similarly, Zhang et al. proposed a distributed approach for very large scale global bundle adjustment computation [11]. The proposed distributed formulation was derived from the classical optimization algorithm alternating direction method of multipliers, based on the global camera consensus. The authors analyzed the conditions under which the convergence of this distributed optimization would be guaranteed and they adopted over-relaxation and self-adaption schemes to improve the convergence rate. Also, the authors proposed to split the large scale camera-point visibility graph in order to reduce the communication overheads of the distributed computing.

The presented paper proposes \(\pi\)-BA, the first to BA hardware accelerator and its implementation on FPGA. Compared to existing acceleration techniques, \(\pi\)-BA simultaneously optimize both performance and power consumption, thus enabling both real-time local robotic localization applications and efficient offline visual reconstruction applications.

III. PROBLEM STATEMENT

In the following sections, we use boldface to represent vectors and matrices.

A. Perspective camera model

In computer vision area, camera is a device that performs central projection of mapping 3D points onto a 2D image plane. Fig. 1 illustrates the perspective camera model that projects 3D points on a image plane. By employing projective geometry and coordinate transformation, the perspective projection is modeled by the following equation,

\[
x = sK[R|t]X
\] (1)
where $X$ is a $4 \times 1$ vector representing the position of a 3D points in the world coordinate, and $x$ is a $3 \times 1$ vector representing the projection point’s location in the image plane. Note that $X$ and $x$ are represented in the homogeneous coordinate. $[R | t]$ is a $3 \times 4$ matrix composed by a $3 \times 3$ rotation matrix $R$ and a $3 \times 1$ translation vector $t$. $R$ and $t$ are referred to as extrinsic parameters of cameras and specify the rigid transformation from the world coordinate to the camera coordinate, as illustrated by Fig. 4. $K$ is a $3 \times 3$ matrix of intrinsic parameters of cameras, which contains parameters such as focal length, focal position and etc. $s$ is a scale parameter.

B. Bundle adjustment

For visual simultaneous localization and mapping problems, bundle adjustment is employed in the last stage of the processing pipeline to further refine camera trajectories and 3D structures. It aims to minimize the discrepancies between observations of 3D points and predicted projections of the corresponding 3D points. Assume that $a$ 3D points are observed in $b$ images. Let $p_i$ be the $i$-th 3D points, $o_{ij}$ be the observation of the $i$-th point on the $j$-th image, and $c_j$ be the $j$-th camera’s parameter. $P(p_i, c_j)$ denotes the projection function.

Generally, bundle adjustment is formulated as an optimization problem, which is defined by Eq. (2). In the equation, $\sigma_{ij}$ evaluates to 1 if the $i$-th 3D point is observed by the $j$-th camera, otherwise its value is 0. This formulation shows that solving the bundle adjustment problem is to determine camera parameters and 3D points’ positions such that observations are closely approximated by the corresponding re-projection points. Note that in the visual simultaneous localization and mapping problems, intrinsic parameters of cameras are known beforehand. As a result, only extrinsic parameters need to be optimized by bundle adjustment.

$$\min_{p_i, c_j} \sum_{i=1}^{a} \sum_{j=1}^{b} \sigma_{ij} \| o_{ij} - P(p_i, c_j) \|$$  \hspace{1cm} (2)

C. Levenberg-Marquardt’s algorithm

Levenberg-Marquardt’s (LM) algorithm is a non-linear least squares algorithm. It is widely used to find a local minimum of the functions that are expressed as a sum of squares of several nonlinear functions. LM combines the merits of the steepest descent and the Gauss-Newton method. It can converge from a wide range of initial conditions. LM has become a standard algorithm for performing the bundle adjustment in visual SLAM and 3D reconstruction problems [11, 12].

Algorithm 1 shows the pseudo code of LM algorithm. In the pseudo code, $\| \cdot \|$ and $\| \cdot \|_{\infty}$ denote the 2 and infinity norm, respectively. $\cdot^T$ is matrix transposition operator. Assume that there are $a$ 3D points, $b$ cameras and $o$ observations. The inputs of the algorithm are a $n \times 1$ measurement vector $x$ and a $m \times 1$ initial parameter vector $p_0$. According to Eq. (1), it can be derived that $m$ equals $3a + 6b$ and $n$ equals $2o$. $f$ is a vector function that maps a parameter vector $p$ to an estimated measurement vector. The output of the algorithm is an optimized parameter vector $p^+$ that minimize $\epsilon^T \epsilon$, where $\epsilon = x - f(p)$. $J$ is the Jacobian matrix of $f(p)$.

LM algorithm solves a nonlinear optimization problem by iteratively linearizing the nonlinear function and solving the linearized equation. In each iteration, it firstly computes the change of magnitude of $p$, through solving the linear equation, and then updates $p$. The stop conditions of LM algorithm are: 1) the magnitude of gradient, $\|g\|_{\infty}$, is less than $\varepsilon_1$; 2) the change of magnitude of $p$, $\|\delta_p\|$, is less than $\varepsilon_2\|p\|$; 3) the maximum iteration step, $k_{max}$, is reached, $\varepsilon_1, \varepsilon_2, k_{max}$ and $\tau$ are parameters specified by users. More details of LM algorithm for bundle adjustment can be found in [13].

In the LM algorithm, the Jacobian matrix, $J$, is a $(3a + 6b) \times 2o$ matrix. $J^T J + \mu D^T D$ is a $(3a + 6b) \times (3a + 6b)$ square matrix. Directly solving Eq. (3) requires $(3a + 6b)^3$ arithmetic operations, which is computationally intensive. In practice, matrix elimination technique and Cholesky factorization are used to reduce the computational complexity of solving Eq. (3).

$$J^T J + \mu D^T D \delta p = g$$  \hspace{1cm} (3)

The parameter vector $p$ can be divided into a 3D points part and a camera parameter part, and is expressed as $p = [p^T; p^c]^T$. Similarly, the Jacobian matrix $J$ can be divided into a 3D points Jacobian matrix and a camera parameter Jacobian matrix, as shown by the following equation. $J^p$ and $J^c$ represent the Jacobians of 3D points and cameras, respectively.

$$J = [J^p \ | \ J^c]$$  \hspace{1cm} (4)

Given that $A = J^T J$ and $\mu D^T D = \text{diag}(A)$. By combining Eq. (4), $A + \mu D^T D$ can be expressed by a simple
block matrix, shown in the following equation. \( \mathbf{U} \) and \( \mathbf{V} \) are a \( 3a \times 3a \) and a \( 6b \times 6b \) matrix. \( \mathbf{W} \) is a \( 6b \times 3a \) matrix.

\[
\mathbf{A} + \mu \mathbf{D}^T \mathbf{D} = \begin{bmatrix} \mathbf{J}^p \mathbf{T} \mathbf{J}^p & \mathbf{J}^p \mathbf{T} \mathbf{J}^c \\ \mathbf{J}^c \mathbf{T} \mathbf{J}^p & \mathbf{J}^c \mathbf{T} \mathbf{J}^c \end{bmatrix} + \mu \begin{bmatrix} \mathbf{D}^p \mathbf{T} \mathbf{D}^p & 0 \\ 0 & \mathbf{D}^c \mathbf{T} \mathbf{D}^c \end{bmatrix} = \begin{bmatrix} \mathbf{U} & \mathbf{W}^T \\ \mathbf{W} & \mathbf{V} \end{bmatrix}
\]

By combining Eq. (3) and Eq. (5), we obtain the following equation.

\[
\begin{bmatrix} \mathbf{U} & \mathbf{W}^T \\ \mathbf{W} & \mathbf{V} \end{bmatrix} \begin{bmatrix} \delta \mathbf{p}^c \\ \delta \mathbf{p}^c \end{bmatrix} = \begin{bmatrix} \mathbf{J}^p \\ \mathbf{J}^c \end{bmatrix} \epsilon
\]

By eliminating the lower left block, \( \mathbf{W} \), the following equation is obtained. In the equation, \( \mathbf{V} - \mathbf{WU}^{-1} \mathbf{W}^T \) is Schur complement matrix, which is a symmetric matrix and is denoted as \( \mathbf{S} \) in this paper. Vector (\( \mathbf{J}^c - \mathbf{WU}^{-1} \mathbf{J}^p \))\( \epsilon \) is denoted as \( \mathbf{r} \) in this paper. Then, \( \delta \mathbf{p}^c \) can be obtained by solving Eq. (7). In practice, \( \delta \mathbf{p}^c \) is solved by Cholesky factorization.

\[
(\mathbf{V} - \mathbf{WU}^{-1} \mathbf{W}^T) \delta \mathbf{p}^c = (\mathbf{J}^c - \mathbf{WU}^{-1} \mathbf{J}^p) \epsilon
\]

After obtaining \( \delta \mathbf{p}^c \), the change of 3D points vector, \( \delta \mathbf{p}^r \), can be obtained by back substitution. Eq. (8) describes the closed-form solution of \( \delta \mathbf{p}^r \). Note that \( \mathbf{U} \) is a diagonal block matrix, of which diagonal elements are \( 3 \times 3 \) matrices. The cost of computing the inversion of \( \mathbf{U} \) is low.

\[
\delta \mathbf{p}^r = \mathbf{U}^{-1} (\mathbf{J}^r \epsilon - \mathbf{W} \delta \mathbf{p}^c)
\]

The computation of \( \mathbf{S} \) is called Schur elimination in this paper. Directly calculating \( \mathbf{S} \) according to its expression, \( \mathbf{V} - \mathbf{WU}^{-1} \mathbf{W}^T \), is computationally expensive. Since \( \mathbf{U} \), \( \mathbf{V} \) and \( \mathbf{W} \) are sparse matrices, the complexity of calculating \( \mathbf{S} \) can be substantially reduced by exploiting the structure of these sparse matrices. Algorithm 2 describes the procedure of calculating \( \mathbf{S} \) and \( \mathbf{r} \). According to the algorithm, computing \( \mathbf{S} \) requires \( ab^2 \) arithmetic operations. Employing Cholesky factorization to solve Eq. (7) requires \( (6b)^3/3 \) operation. For vSLAM problems and 3D reconstruction problems, the number of 3D points \( a \) is much larger than the number of images \( b \). The Shur elimination is the most computationally intensive step when solving the linear equation in LM algorithm.

### IV. SYSTEM ARCHITECTURE OF LM IMPLEMENTATION

After introducing Schur elimination, the computations in one iteration of LM algorithm can be divided into five parts including Jacobian update (JU), Schur elimination (SE), Cholesky factorization solving \( \delta \mathbf{p} \) (CFS), gain ratio evaluation (GRE) and trust region expand (TRE). One of the most time-consuming parts is SE, which has complexity \( O(ab^2) \). Therefore, we propose a hardware-software co-design in which the SE is accelerated in hardware and other parts are implemented in software. The whole system architecture is shown in Fig. 2.

![Fig. 2. System architecture](image)

The amount of data transferred between hardware and software is \( 18a + b^2/2 \). We use AXI Direct Memory Access (DMA), 6400Mbit/s. The measured performance shows that the data transfer time is less than the hardware computation time, and also both data transfer and computation are pipelined to reduce the data transfer overhead.

As shown in Algorithm 2, the SE mainly computes \( \mathbf{S} (6b \times 6b) \) given input \( \mathbf{J} (2a \times (3a + 6b)) \) and \( \mathbf{D} (3a + 6b) \). Given the large matrices, data storage format is a key to system performance and size.

The Jacobian matrix is a block sparse matrix, like Fig. 3(a). Therefore, Jacobian matrix uses a block compressed sparse row (BCSR) storage format [14]. Typical BCSR format uses three attributes: \( \text{values} \) storing linearly in row-wise order the values of all blocks, \( \text{rows} \) storing the block-column indices in a row, and \( \text{block-starts} \) storing the indices of the first element of each block in values. In this paper, because the block size of \( \mathbf{J} \) is fixed in BA, the block-starts information is not needed. In addition, we convert the \( \text{rows} \) attributes to a set of co-observations, which means a set of images observing a point \( i \), and the number of elements in the set (\( CO_i \)) which is called co-observation value and indicates that point \( i \) is observed by how many images. In Fig. 3(a) the set of co-observations of the second point is \( \{1, 2\} \) and \( CO_2 = 2 \) because the second is observed by the first and second images. The conversion is
The advantages of doing this are that 1) The set and $CO_i$ can address values, and 2) they contain the physical meaning of the BA problem and can be directly used in subsequent computations without the need of calculation on-the-fly in hardware. In addition, $J^p$ and $J^c$ are stored separately in off-chip memory.

The $S$ matrix is a dense matrix and obtained by accumulating the sub-matrices continuously as shown in Algorithm 2. In the entire calculation, the $S$ matrix is divided into three parts. The first part is a diagonal matrix calculated in Line 2 of Algorithm 2, which is stored as a vector shown in Fig. 4(a). The second part is a diagonal block matrix computed in Line 9 of Algorithm 2. Only a half of the diagonal blocks is stored shown Fig. 4(b). The last part is a partial accumulation of $S$ matrix as shown in Line 15 of Algorithm 2. Because $S$ matrix is symmetric positive definite, nearly half of $S$ is stored shown in Fig. 4(c). In order to simplify the hardware control design, the whole diagonal blocks are preserved to maintain computation regularity on the diagonal blocks and other blocks.

V. FPGA IMPLEMENTATION OF SCHUR ELIMINATION WITH CO-OBSERVATION OPTIMIZATION

The customized SE hardware implementation is sketched in Fig. 5. The input buffer temporarily stores the data of the Jacobian matrix transmitted from the off-chip memory. The middle is the main computation of SE, called SE processing element. The accumulation unit computes the Line 2 of Algorithm 2 and adds the intermediate computational results of $S$ and $r$, respectively. The output buffer temporarily stores $S$ and $r$ which need to be transferred back to the off-chip memory. In the next, we present the detailed design of the SE processing element (PE). Because the co-observation value $CO_i$ has impacts on the speed, computation and memory resource usage of the PE, we propose a Co-Observation Optimization design method.

As shown in Fig. 5, the PE is partitioned into four stages according to data dependencies and as early as possible scheduling. The first stage performs the computations of Lines 4-11 in Algorithm 2. Only a half of the diagonal blocks is stored shown Fig. 4(a). The second stage, the inverse of $U_i$ is calculated, corresponding Line 12 of the algorithm. The matrix computation $-W_{ij} \times \text{inv}$ is completed in the third stage. The fourth stage completes the remainder computations of Lines 14 and 16. The matrix multiplications and additions in the matrix $S$ processing unit (SPU) in the fourth stage are fully parallelized.

The latencies of the four stages are affected by $CO_i$. The latencies of the first and third stages are $36CO_i$ cycles. The latency of the fourth stage is $18(CO_i^2 + CO_i)$ cycles. The latency of the second stage is 70 cycles, independent of $CO_i$. The fourth stage is the bottleneck. To speedup the operations, SPU is duplicated for parallel computation on different data.
The number of duplications depends on $CO_i$ and available hardware resources. Given sufficient resources, the matching efficiency between the number of SPUs and $CO_i$ is shown in Fig. 6. We can see that mismatch of both may lead to slow performance or inefficient resource usage. In practice, $CO_i$ varies significantly among points, which will be shown in the result section. Therefore, the structure of PE should be optimized to match to the majority of the $CO_i$ of points.

In our tested data, more than 30% points have $CO_i = 2$. We customize one PE for mainly processing points with $CO_i = 2$. The number of SPUs ($q$) of the PE is roughly determined as

$$18(CO_i^2 + CO_i)/q \approx 36CO_i \approx 70$$  \hspace{1cm} (9)

resulting in $q = 2$.

In addition, the amount of intermediate computational results is related to $CO_i$ as shown in Lines 7-11 of Algorithm 2. As a result, the size of RAMs in a PE is determined by the maximum $CO_i$ processed by the PE. In the customized PE for $CO_i = 2$ the on-chip memory usage can be reduced.

Ideally, PEs can be customized with different $q$ for the points with larger $CO_i$ accordingly. In practice, $q$ is determined not only by Eq. (9), but also by available resources. When the available resources are not enough, SPU duplication is not feasible. In this case, the first three stages of PE can be slowed down to save computational resources. For example, one multiplier and one adder can be removed from the third stage when the fourth stage is the bottleneck.

Moreover, the second stage involves matrix inverse computation. In the original software implementation, Cholesky factorization is used, containing complex operations such as square root and division. Especially, multiple square root operations have interdependencies and can not be parallelized. To solve the issue, we use determinant and adjoint matrix to invert the matrix $U_i^{-1} = \frac{\text{adj} U_i}{\text{det} U_i}$, given the small $3 \times 3$ matrix.

VI. EXPERIMENTAL RESULTS

The proposed hardware-software co-designed BA implementation is evaluated on a Zynq xc7z030sbg485-1 FPGA platform. The software part using double-precision floating-point numerical representation is executed on an ARM
Cortex-A9@667Hz. The hardware part using single-precision floating-point numerical representation is synthesized and implemented on the programmable logic with maximum clock frequency 180 MHz. For the hardware part, three versions are implemented: one PE with one SPU (named Schur_1), one PE with two SPUs (named Schur_2), and two PEs each having two SPUs (named Schur_3).

Our implementation is compared with a software implementation which uses the non-linear optimization library Ceres-Solver [15]. The software implementation using double-precision floating-point numerical representation runs on a Intel Pentium G2030 CPU at 3.0 GHz with 4 GB of RAM and on ARM Cortex-A9 core, respectively.

The datasets used in our experiments are from Bundle Adjustment in the Large (BAL) [2]. We choose five datasets, each containing input images below 50. This is because local BA on 50 images is enough for SLAM application and for simple scene SfM. The number of images, points and observations of the five datasets are shown in Table I. The five datasets contain different combinations of images, points and observations, and represent different scenes.

As mentioned earlier, co-observation value $CO_i$ affects the speed, efficiency and RAM usage of the Schur elimination processing element. Therefore, we first make a statistical analysis of the datasets. From Table I, we can see that for the five datasets, about 50% points are observed in two images ($CO_i = 2$). As $CO_i$ value increases, the percentage decreases. That is, the possibility of a point appearing in a large number of images is low. This feature is exploited in our design to customize hardware design.

In our design Schur_3 with two PEs, the first PE is customized for mainly processing points with $CO_i = 2$. Due to the on-chip memory resource limitation of the target FPGA device, the second PE is designed with only two SPUs. Because the processing time of points with different $CO_i$ is different, the workloads of the two PEs need to be balanced. We design a software controller to assign workloads. For the five datasets, points with $CO_i \in [2, 10]$ are assigned to the first PE, while points with $CO_i \in [5, 50]$ are assigned to the second PE. Here the upper bound is set to 50 because the maximum $CO_i$ is 50 for datasets with up to 50 images.

### A. Resource usage

The experimental results include three parts. The first part analyzes the characteristics of datasets, showing the distribution of $CO_i$. The second part shows the resource usage of the designs. The last part evaluates the speed and power consumption of the designs.

#### B. Dataset analysis

The resource usage of the three hardware designs of the Schur elimination module is reported in Table II including flip-flop (FF), lookup table (LUT), BRAM and DSP blocks. The resource consumption of important submodules is also shown. From the table we can make the following observations. Firstly, using single-precision floating point can save resources 14% FFs, 14% LUTs, 25% BRAMs and 28% DSPs, compared to double-precision floating point implementation, while the computation accuracy of the Schur elimination is not affected. Our experiment result shows that the difference of the Frobenius norm of matrix $S$ is within $10^{-6}$ between double-precision and single-precision implementations. Secondly, comparing Schur_2 with Schur_1, due to SPU duplication by 2, the computational resource usage increases up to 5%, while the BRAM usage increases significantly 18%. This is because two SPUs leads to almost doubling matrix $S$ storage space. Thirdly, in Schur_3, the two PEs are customized leading to DSP or BRAM saving. PE_Small corresponds to the PE processing points with $2 \leq CO_i \leq 10$. This can save 13.5 BRAM blocks compared to the PE (for processing points with $2 \leq CO_i \leq 50$) in Schur_2. PE_Large corresponds to the PE processing points with $5 \leq CO_i \leq 50$. It saves 5 DSP blocks compared to the PE in Schur_2. The DSP saving can be enlarged if the lower bound increases. Lastly, for the parallel Schur elimination implementation, on-chip BRAM is the main limit or obstacle. The consumption source mainly stems from matrix $S$ storage. This also points out a future research direction on matrix $S$ storage reduction.

#### C. Execution time and power consumption

We evaluate the execution time of Schur elimination with different datasets on different computing platforms. The results are shown in Table III. It is shown that on average Schur_3 is 3.7 times and 2 times faster than Schur_1 and Schur_2, respectively. The hardware implementation Schur_3 is about 3.1 times and 57 times faster than the Intel and ARM implementations, respectively.

Moreover, we also evaluate performance and power consumption of the BA implementations on the three computing platforms. Averaging over the five datasets, the execution time per BA iteration of Intel, ARM and our software-hardware design are 0.11s, 1.87s and 1.29s, respectively. The nominal power consumption of the used Intel CPU is 55W, while the power consumption of the ARM core and our design are 1.5W and 2.8W, respectively, reported by Xilinx power estimator. The Intel CPU implementation has the fastest speed, but is not suitable to embedded applications due to its high power consumption. Our design is 1.5 times faster than the ARM implementation. Note that, in our design the Schur elimination part is accelerated on hardware and the rest of BA is executed on the ARM core. The Schur elimination part takes about 30% of the execution time of BA. In future, other parts of BA such


### TABLE II

| COi | 2    | 3    | 4    | 5    | 6    | 7    | 8    | 9    | 10   | 11   |
|-----|------|------|------|------|------|------|------|------|------|------|
| 1   | 38.89| 20.44| 12.96| 9.12 | 6.39 | 4.32 | 2.92 | 2.04 | 1.38 | 0.94 |
| 2   | 51.78| 19.60| 10.97| 6.57 | 4.05 | 2.85 | 1.74 | 1.09 | 0.65 | 0.27 |
| 3   | 51.86| 17.19| 10.03| 5.69 | 4.06 | 3.04 | 2.51 | 1.81 | 1.21 | 0.96 |
| 4   | 44.35| 17.84| 10.60| 6.73 | 5.00 | 3.33 | 2.73 | 2.13 | 1.62 | 1.53 |
| 5   | 32.14| 17.08| 9.30  | 5.21 | 3.93 | 2.69 | 2.40 | 1.75 | 1.48 | 1.02 |

### TABLE III

| HW Designs | FF (%) | LUT (%) | BRAM (%) | DSP (%) |
|------------|--------|---------|----------|---------|
| Schur_1    |        |         |          |         |
| Double-precision | PE  | 30151  | 17913 | 41  | 156  |
|             | MEM_S | 17  | 497 | 84.5 | 0  |
|             | Others | 3889 | 2793 | 16  | 20  |
|             | Total  | 34057(22%) | 21208(27%) | 141.51(37%) | 176(44%) |
| Schur_1    |        |         |          |         |
| Single-precision | PE  | 11534  | 8626  | 21.5 | 57  |
|             | MEM_S | 16  | 250 | 45.5 | 0  |
|             | Others | 1286 | 1362 | 8  | 9  |
|             | Total  | 12850(8%) | 10258(13%) | 73(28%) | 66(10%) |
| Schur_2    |        |         |          |         |
| Single-precision | PE  | 13171  | 10650 | 28.5 | 74  |
|             | MEM_S | 28  | 462 | 85  | 0  |
|             | Others | 1506 | 1571 | 8  | 11  |
|             | Total  | 14750(9%) | 12854(16%) | 121(46%) | 85(21%) |
| Schur_3    |        |         |          |         |
| Single-precision | PE_Large | 13173  | 11103 | 28.5 | 69  |
|             | PE_Small | 13050 | 10656 | 15  | 74  |
|             | MEM_S | 56  | 921 | 169.5 | 0  |
|             | Others | 2598 | 1834 | 16  | 21  |
|             | Total  | 28877(18%) | 24534(31%) | 229(86%) | 164(41%) |

*The number of Block RAMs is accounted in terms of 36Kbit block. 0.5 means a 18Kbit block.

as Jacobian update will also be accelerated on hardware to achieve higher performance improvement.

### VII. CONCLUSION

BA is a fundamental optimization technique used in many crucial applications, and often the primary performance and power consumption bottleneck in these applications. However, due to the complexities of BA algorithms, designing hardware to accelerate BA is extremely challenging. Previous approaches of optimizing BA performance heavily rely on parallel processing or distributed computing, which trade higher power consumption for higher performance. In this paper, we presented π-BA, the first hardware-software co-designed BA engine on an embedded FPGA-SoC. Specifically, we developed a novel Co-Observation Optimization technique, and experimental results confirmed that π-BA outperformed existing BA solutions in both performance and power consumption. With π-BA, we can enable more robotic localization as well as visual reconstruction applications by allowing larger scale online local BA on power-constrained embedded devices and more efficient offline global BA by using less computing resources and power consumption.

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| Dataset | Execution time (ms) | FPGA Speedup |
|---------|---------------------|--------------|
|          | Schur_1 | Schur_2 | Schur_3 | Intel | ARM | Intel | ARM |
| 1       | 59.155  | 31.746  | 15.885  | 43.168 | 817.381 | 2.717 | 51.45 |
| 2       | 20.822  | 11.905  | 5.974   | 18.574 | 341.569 | 3.109 | 57.17 |
| 3       | 50.261  | 27.560  | 13.854  | 35.607 | 662.382 | 2.570 | 44.93 |
| 4       | 35.401  | 19.034  | 9.632   | 20.278 | 373.159 | 3.109 | 38.74 |
| 5       | 66.847  | 36.010  | 18.126  | 43.707 | 805.415 | 2.411 | 44.43 |
| Average | 46.497  | 25.251  | 12.649  | 32.267 | 599.981 | 2.582 | 47.34 |

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