Effect of device design on charge offset drift in Si/SiO$_2$ single electron devices

Binhui Hu,$^{1,3}$a Erick D. Ochoa,$^2$ Daniel Sanchez,$^2$ Justin K. Perron,$^2$ Neil M. Zimmerman,$^3$ and M. D. Stewart, Jr.$^a$$^3$

1) Joint Quantum Institute, University of Maryland, College Park, Maryland 20742, USA
2) California State University-San Marcos, San Marcos, CA 92096, USA
3) National Institute of Standards and Technology, Gaithersburg, MD, 20899, USA

(Dated: 13 July 2018)

We have measured the low-frequency time instability known as charge offset drift of Si/SiO$_2$ single electron devices (SEDs) with and without an overall poly-Si top gate. We find that SEDs with a poly-Si top gate have significantly less charge offset drift, exhibiting fewer isolated jumps and a factor of two reduction in fluctuations about a stable mean value. The observed reduction can be accounted for by the electrostatic reduction in the mutual capacitance $C_m$ between defects and the quantum dot, and increase in the total defect capacitance $C_d$ due to the top gate. These results depart from the accepted understanding that the level of charge offset drift in SEDs is determined by the intrinsic material properties, forcing consideration of the device design as well. We expect these results to be of importance in developing SEDs for applications from quantum information to metrology or wherever charge noise or integrability of devices is a challenge.

I. INTRODUCTION

Single electron devices (SEDs) have many important applications due to their ability to localize and manipulate individual electrons’ degrees of freedom. SEDs have been proposed as current standards in electrical metrology$^{1,2}$ and as memory and logical devices in integrated circuits.$^{10,12}$ They have also been studied as qubits, when there are only a few electrons on the quantum dot.$^{15,16}$ Ultimately, these applications must integrate many SEDs together, which, in turn, requires the operating point of each SED to remain stable in time. However, a long-standing, low-frequency time instability known as charge offset drift $Q_0(t)$ present in real devices remains a challenge to realizing the full potential of SEDs.$^{20,21}$

Up to now, charge offset drift was understood to be a consequence of intrinsic material properties.$^{20,21}$ This material system explanation is based on the experimental fact that SEDs made in two material systems have very different $Q_0(t)$: Al/AlO$_x$-based SEDs exhibit a large change in charge offset ($\Delta Q_0 > 1e$), while in mesa-etched Si/SiO$_2$-based silicon-on-insulator (SOI) devices the change of charge offset is small ($\Delta Q_0 < 0.01e$). Here $e$ is the electron charge and the value of $Q_0(t)$ is normalized to the period of the Coulomb oscillations.$^{21}$ This experimental fact is interpreted microscopically as a distinct difference in the level of interaction between two-level system (TLS) defects present in the amorphous insulators, AlO$_x$ and SiO$_2$. Specifically, TLS defects are not stable over time or gate voltage sweeps in Al/AlO$_x$ devices, while they are stable in Si/SiO$_2$ devices.$^{20,21}$ Unsuccessful attempts to reduce $\Delta Q_0$ in Al/AlO$_x$-based SEDs with different device geometries and structures lend additional weight to this material-only explanation$^{22}$ which has had significant influence over the direction of SED research by emphasizing the expected performance edge implied for Si devices.$^{20}$ However, noise measurements have only been done in a very limited set of Si/SiO$_2$ based SED device structures: mainly mesa-etched SOI devices$^{23,24}$ and Si SEDs with metal gates$^{25,26}$.

Workers at Sandia National Labs and the University of Sherbrooke have pioneered fabrication of Si/SiO$_2$-based SEDs with a single layer of doped polysilicon gates$^{27,28}$ Those devices present an opportunity to assess the robustness of the above explanation for $Q_0(t)$ because they do not have a blanket gate to function as an SED, and their $Q_0(t)$ behavior differs from the mesa-etched SOI devices while not altering the Si/SiO$_2$ material system.$^{28}$ In this manuscript, we present data showing that Si/SiO$_2$ single gate layer devices show significantly larger $\Delta Q_0$ than their SOI counterparts and, moreover, that $\Delta Q_0$ can be reduced with the addition of another gate covering the fine area of the device. This design change mimics the gate stack of the very stable SOI devices mentioned above. Our results show that $Q_0(t)$ is not entirely determined by the material system as previously thought.

II. SAMPLES AND EXPERIMENTAL DETAILS

We have fabricated and measured $Q_0(t)$ on three different types of devices shown in Fig. 1. A single layer of poly-Si gates were patterned on top of a 37 nm thick SiO$_2$ gate oxide. The gate arrangement shown in Fig. 1(a), similar to Ref. 27 and 28, produces two individual SEDs: one in the upper half of the image with the dot

---

$a$To whom correspondence should be addressed. Electronic mail: hnhl@umd.edu, stew@nist.gov
FIG. 1. The different types of devices employed in this study. (a) SEM image of a single gate layer device, showing poly-Si gates on gate oxide, referred to as “bare”. Two individual single electron devices (SEDs) can be formed underneath positively biased enhancement gates UEG and LEG, while other plunger gates are used to define the quantum dot. (b) AFM image of an SED device with a full poly-Si top gate, referred to as “TG”. (c) AFM image of an SED device with a half poly-Si top gate. The upper SED is covered by the poly-Si top gate (“TG”), and the lower one is not and is referred to as “oxide”. Lower gates in these devices have the same geometry.

All devices discussed here were fabricated at NIST on 150 mm boron-doped silicon <100> wafers with a resistivity of 5-10 Ω·cm. The main fabrication process is as follows. The source/drain contacts (ULO, URO, LLO, LRO in Fig. 1(a)) are formed by phosphorus ion implantation. Then, a 125 nm field oxide is grown in a wet oxidation furnace at 900 °C, and a second deposition of in-situ doped N⁺ poly-Si. Then the top gate layer is defined using the same e-beam lithography process as for the lower gates. The final step is aluminum metallization and the 425 °C forming gas anneal.

To measure the charge offset drift, a positive gate voltage is applied to the enhancement gate UEG (LEG) to accumulate electrons at the Si/SiO₂ interface, while other plunger gates are biased to define the quantum dot. The SED is tuned so that Coulomb blockade oscillations can be observed while sweeping either the enhancement gate or one of the plunger gates. We then repeatedly measure the same Coulomb blockade oscillation curve approximately every 15 minutes to track the changes in the local charge environment of the dot. $Q_0(t)$ is extracted from each trace using two different methods. At large source-drain bias (about half of the charging energy), the source-drain current $I_d$ oscillates sinusoidally when sweeping gate voltage $V_p$, and each trace is fit to a sinusoidal function: $I_d(V_p) = A_0 + A \sin(2\pi(V_p/V_0 + Q_0(t)/e) + BV_p$, where $A_0$ is a current offset, $A$ is the amplitude of the oscillations, $V_0$ is the period of the oscillations, and $B$ is used to account for any slope in the sinusoidal curve. If the trace is not sinusoidal, a Gaussian function is used to find the peak location $V_{peak}(t)$, and $Q_0(t) = -e(V_{peak}(t) - V_{peak}(t = 0))/\Delta V_p$, where $\Delta V_p$ is the average voltage difference between the peak of interest and the two neighboring peaks. We have used both methods to analyze sinusoidal traces, and found that the results are consistent within 10%, predominantly due to the uncertainty associated with $\Delta V_p$. Measurements performed at NIST were taken at about 2.5 K in a closed-cycle cryostat. To exclude the possibility that the experimental setup contributes to the measured drift, NIST measurements were performed with two different sets of electronics (discussed in Sect. III). Additional devices were also measured at CSUSM in another closed-cycle cryostat at about 2.5 K. The results (see Table I) from each set of measurements are qualitatively and quantitatively similar to those presented for the same device type.

The measured quantum dots are not necessarily intentional quantum dots. We select the bias conditions and the data fitting range so that the device operates as a stable single quantum dot device, confirmed by two-dimensional gate voltage sweeps and Coulomb diamonds. Each dot measured had a charging energy of about 5 meV. As these quantum dots are used as local charge sensors of the environment, the detailed mechanism for the formation of the quantum dot is not expected to affect our conclusions.
III. RESULTS

Figure 2 shows a typical result for a “bare” (device 4.7-41L) using standard AC lock-in amplifier techniques. The charge offset drift $Q_0(t)$ has three distinct features, which were also observed in devices of the same design fabricated at Sandia National Labs. First, over the course of the first two days, $Q_0(t)$ shows an evolution from rapid drift toward slower drift while winding $Q_0(t)$ through several $e$. This phenomenon has been previously referred to as transient relaxation. Second, the data show isolated discrete jumps or drifts, which are not stationary. Third, the device shows some stable periods where $Q_0(t)$ takes on a value within a stationary band. One such period is indicated by a shaded area in Fig. 2(b). We characterize local fluctuations about a stable mean with the standard deviation $\sigma$. This metric, while useful in quantifying the differences between devices, does not capture discrete jumps or long-term drift; all three metrics affect device integrability.

Figure 3 shows $Q_0(t)$ behavior measured in a “TG” device. There are four main differences from the data depicted in Fig. 2. First, while transient relaxation is still observed in the device with the top gate, $Q_0(t)$ winds through less than 1 $e$ variation before becoming stable and, in the first cooldown data (Fig. 3(b)), reaches a stable value in just a few hours. Second, after the transient evolution, $Q_0(t)$ essentially remains stable for the duration of the measurement in the device with the top gate. Third, $Q_0(t)$ in top-gated devices shows fewer and smaller discrete jumps. Fourth, the local fluctuations about the stable mean value are reduced by more than a factor of two. All the devices of this type which we have measured show this behavior.

Finally, in an effort to investigate the role of the isolation oxide, we also measured neighboring “oxide” and “TG” SEDs. This also enables a comparison of devices within 200 nm of each other in the same cooldown. Figure 4 shows the measurement results. Interestingly, transient relaxation is absent in both devices while a systematic (approximately linear) drift is observed instead indicating a non-stationary process. The origin of the linear drift is not clear and requires further investigation. Notwithstanding the linear drift, we again find a reduction in the frequency and amplitude of discrete jumps as well as fluctuations in the “TG” device. To facilitate a comparison of the fluctuations with the previous data we fit the data to a line and remove this dependence before plotting the histograms shown in the insets. The $\sigma$ obtained this way shown in the “oxide” SED (device 5.4-11L) is about 9 times larger than that in the “TG” SED (device 5.4-11U). When assessed by this metric, the performance of the “oxide” device is the worst of those presented here even when compared to that of the “bare” device (see Fig. 2). This may be due to the dry etching process used to remove the top gate, leaving behind some charge defects in the oxide. When assessed by the long-
term drift, the “oxide” device only shows small monotonic drift with few discrete jumps which is better than the “bare” device. In terms of both metrics, the “TG” device has the best performance.

A natural question when making these measurements is whether or not the measured drift is intrinsic to the device or from some extrinsic source in the measurement setup, especially since these measurements extend over days. To assess this question, measurements at NIST were performed with two separate sets of electronics and additional measurements were performed at CSUSM in a separate cryostat with a third set of electronics. The electronic systems at NIST are a DC measurement system using an Agilent 4156C precision semiconductor parameter analyzer, and an AC measurement system using standard lock-in amplifier techniques at 17 Hz. The DC measurement electronics return all electrodes to zero voltage between measurements of the Coulomb blockade curve while the AC electronics keeps a steady voltage on each electrode while returning the swept electrode to the beginning of the sweep between measurements. The measurement electronics at CSUSM keep every electrode at the voltage corresponding to the end of the sweep between measurements. A comparison of the NIST measurement electronics is made in Fig. 3 for an SED device with a top gate (device 5.4-25U). The DC system data are shown in Fig. 3(a)(b) and the AC system data are shown in Fig. 3(c)(d). Although the DC data are noisier than the AC data, they are qualitatively consistent with each other, and the standard deviation in the shaded areas is only different by 22%. The longer transient relaxation time observed in the AC data is likely due to the intervening thermal cycle, which necessitated different applied voltages.

IV. DISCUSSION

The data are summarized in Table I (additional data is shown in the Supplementary Material S3). In the context of the material-only explanation for $Q_0(t)$, all the devices listed should show similar drift; however, the data show that for Si/SiO$_2$-based SEDs, $Q_0(t)$ is influenced by factors other than the material system. We can characterize our empirical conclusions as follows: i) Long-term drift: “bare” devices (Fig. 2) show random large-amplitude drift over the course of hours or days, similar to the Al/AlO$_x$ system. $^{21,22}$ “oxide” (Fig. 2(b)) and “TG” (Figures 3(b) and 3(d)) devices show no drift or monotonic, predictable drift with fewer and smaller discrete jumps, similar to previous results in SOI devices. $^{23}$ ii) Local fluctuations, i.e. $\sigma$: “bare” and “oxide” devices show substantially larger $\sigma$ than “TG” devices. Below we list possible mechanisms driving the difference in behavior shown in this manuscript.

There are clear electrical differences between the two types of devices. The top gate allows for the application of an electric field across the gate oxide in addition to the field resulting from the work function difference between the gate and the silicon. These fields could freeze defects out. The gate also acts as a ground plane which decreases the electric field across the gate oxide in addition to decreasing the capacitance of charge defects and decreasing the mutual capacitance $C_m$ of defects coupled to the quantum dot. Considering a simplified case where one effective defect is coupled to the quantum dot, $Q_0(t) \approx (C_m/C_d)\Delta Q_d(t)$ (see the Supplementary Material S1), where $\Delta Q_d(t)$ is the variation of the defect charge. Both increasing the total capacitance $C_d$ of charge defects in the SED, and at the same time decreases the mutual capacitance $C_m$ of defects coupled to the quantum dot. Considering the change in $C_m$ and $C_d$ (see the Supplementary Material S2), we have used FastCap to simulate “bare” and “TG” devices. For charge defects located 90 nm away from the dot laterally and at the midpoint of the gate oxide thickness, the top gate reduces $C_m$ by 55% and increases $C_d$ by 16%. This reduces $C_m/C_d$ by about a factor of two which gives the same order of magnitude as the observed reduction in $\sigma$. For defects located nearer to the Si/SiO$_2$ interface, the reduction in $C_m/C_d$ is more muted, while it is more pronounced for defects near the SiO$_2$/gate interface. Similarly, for defects located nearer the quantum dot or other gates, the reduction in $C_m/C_d$
TABLE I. Summary of measured charge offset drift $Q_0(t)$. Devices with a top gate exhibit a factor of two lower $\sigma$ than those devices without a top gate. Uncertainty corresponds to a 95% confidence interval and is estimated based on a $\chi^2$ distribution of $N - 1$ degrees of freedom where $N$ corresponds to the number of data points.

| Device | Type | Isolation Oxide | Measurement | Fitting | $\sigma$ of $Q_0(t) (e)$      |
|--------|------|-----------------|-------------|---------|-------------------------------|
| 4.7-41L | "bare" | No              | NIST AC     | Sine    | $0.020 \pm 0.004$            |
| 4.7-33U | "bare" | No              | CSUSM DC    | Gaussian| $0.017 \pm 0.003$            |
| 5.4-11L | "oxide" | Yes             | NIST DC     | Gaussian| $0.046e \pm 0.005$           |

TABLE I. Summary of measured charge offset drift $Q_0(t)$. Devices with a top gate exhibit a factor of two lower $\sigma$ than those devices without a top gate. Uncertainty corresponds to a 95% confidence interval and is estimated based on a $\chi^2$ distribution of $N - 1$ degrees of freedom where $N$ corresponds to the number of data points.

| Device | Measurement | Fitting | $\sigma$ of $Q_0(t) (e)$      |
|--------|-------------|---------|-------------------------------|
| 5.4-23U | NIST DC     | Sine    | $0.007 \pm 0.001$            |
| 5.4-25U | NIST DC     | Sine    | $0.010e \pm 0.002$           |
| 5.4-25U | NIST AC     | Sine    | $0.008e \pm 0.001$           |
| 5.4-11U | NIST AC     | Gaussian| $0.005e \pm 0.001$           |

due to the top gate is more muted. The detailed spatial distribution of defects will impact the size of the change in $\sigma$, however, these calculations show that the observed reduction of $\sigma$ in $Q_0(t)$ can be accounted for by the electrostatic reduction in $C_m$ and increase in $C_d$, with the change in $C_m$ being dominant. Moreover, it is plausible that the lack of an exposed gate oxide surface for SOI devices and "TG" devices as compared to "bare" or "oxide" single-layer devices can effectively reduce the charge offset drift by reducing the number of defects near the gate oxide surface, where moisture or other ion defects may adsorb to the surface.

Additional electrical differences include the top poly-Si gate acting as a Faraday cage, which can shield the dot in the device from external electrical disturbance. The presence of the gate also necessarily implies additional strain in the device. Finally, though we have worked to minimize them, the gate cannot be introduced without some fabrication differences. These include second layer e-beam exposure, exposure to the dry etch process, and isolation oxide growth.

Whatever the reason for the reduction in $Q_0(t)$, these data indicate the previous understanding of charge offset drift as a material property is incomplete. We hasten to add, however, that the material stacks are still an important factor. In particular, as noted above, it appears that $Q_0(t)$ in "bare" devices (with a low-quality native oxide on the gates) have larger random drift and discrete jumps, similar to previous Al/AlO$_x$ results$^{2,22}$ whereas the devices with deliberate high-quality isolation oxide show monotonic, predictable drift with few or no discrete jumps similar to previous SOI results$^{24}$. This may indicate that the native oxide, which can also pick up moisture from the surrounding air, has the same type of interacting defects that we have previously discussed. In addition to the intrinsic TLS defects, the long-term drift in the native oxide could also be due to such mechanisms as the movement of dissolved hydroxyl ions from adsorbed moisture. Further experiments are necessary to confirm this suggestion.

Earlier work on Al/AlO$_x$/Al based SEDs with a nano-Faraday cage did not show any improvement in the charge offset drift. In fact, enclosing the device in additional AlO$_x$/Al increased $\Delta Q_0$ by approximately a factor of two, in striking contrast to the results presented here. The likely reason is that unlike the AlO$_x$/Al stack, the SiO$_2$/poly-Si top gate does not introduce a significant number of new unstable charge defects, so that the benefit of adding the gate as outlined above (which should not otherwise differ between the two material systems) outweighs the negative effect from additional charge defects.

V. CONCLUSIONS

We have shown that introducing a poly-Si top gate can effectively reduce the level of the charge offset drift in Si/SiO$_2$-based single gate layer SEDs. This clearly demonstrates that the level of charge offset drift measured depends on factors other than simply the material systems used as previously thought, and the device design plays an important role. Not only do these results provide researchers the opportunity to tune the level of stability performance in their devices, it provides an avenue toward further understanding the origin of noise in devices in various material systems.

SUPPLEMENTARY MATERIAL

See supplementary material for the equivalent circuit model to deduce the relationship $Q_0(t) \approx (C_m/C_d) \Delta Q_d(t)$, and the FastCap simulation. It also includes addition data not presented in the main text.
ACKNOWLEDGMENTS

We are grateful to acknowledge useful discussions with Joshua M. Pomeroy, Joseph A. Hagmann, and Ryan Stein. We would also like to thank Ron Manginell, Malcolm Carroll, and co-workers at Sandia National Laboratories for providing us the single layer SED lithographic design. Research was performed in part at the NIST Center for Nanoscale Science and Technology.

DISCLAIMER

Certain commercial equipment, instruments and materials are identified in order to specify experimental procedures as completely as possible. In no case does such identification imply a recommendation or it imply that any of the materials, instruments or equipment identified are necessarily the best available for the purpose.

1M. W. Keller, J. M. Martinis, N. M. Zimmerman, and A. H. Steinbach, Applied Physics Letters 69, 1804 (1996)
2S. J. Wright, M. D. Blumenthal, M. Pepper, D. Anderson, G. A. C. Jones, C. A. Nicoll, and D. A. Ritchie, Phys. Rev. B 80, 113303 (2009)
3V. P. Maisi, Y. A. Pashkin, S. Kafanov, J.-S. Tsai, and J. P. Pekola, New Journal of Physics 11, 113057 (2009)
4J. D. Fletcher, M. Kataoka, S. P. Giblin, S. Park, H.-S. Sim, P. See, D. A. Ritchie, J. P. Griffiths, G. A. C. Jones, H. E. Beere, and T. J. B. M. Jansen, Phys. Rev. B 86, 155311 (2012)
5S. P. Giblin, M. Kataoka, J. D. Fletcher, P. See, T. J. B. M. Jansen, J. P. Griffiths, G. A. C. Jones, I. Farrer, and D. A. Ritchie, Nat. Commun. 3, 930 (2012)
6J. P. Pekola, O.-P. Saira, V. F. Maisi, A. Kempinen, M. Möttönen, Y. A. Pashkin, and D. V. Averin, Rev. Mod. Phys. 85, 1421 (2013)
7G. Yamahata, K. Nakamura, K. Nishiguchi, and A. Fujiwara, Nat. Commun. 5, 5638 (2014)
8Y. Nakamura, S. and Pashkin, J. Tsai, and N. Kaneko, IEEE Trans. Instrum. Meas. 64, 16961701 (2015).
9G. Yamahata, K. Nakamura, and A. Fujiwara, Applied Physics Letters 106, 023512 (2015)
10R. H. Chen, A. N. Korotkov, and K. K. Likharev, in 1995 53rd Annual Device Research Conference Digest (1995) pp. 44–45.
11K. K. Likharev, Proceedings of the IEEE 87, 606 (1999)
12Y. Takahashi, Y. Ono, A. Fujiwara, and H. Inokawa, Journal of Physics: Condensed Matter 14, R955 (2002)
13Y. Takahashi, Y. Ono, A. Fujiwara, and H. Inokawa, in Proceedings. 7th International Conference on Solid-State and Integrated Circuit Technology, Vol. 1 (2004) pp. 624–629 vol.1.
14K. Maeda, N. Okabayashi, S. Kano, S. Takeshita, D. Tanaka, M. Sakamoto, T. Teranishi, and Y. Majima, ACS Nano 6, 2798 (2012)
15D. Loss and D. P. DiVincenzo, Phys. Rev. A 57, 120 (1998)
16E. Kane, Nature 393, 133 (1998)
17W. G. van der Wiel, S. De Franceschi, J. M. Elzerman, T. Fujisawa, S. Tarucha, and L. P. Kouwenhoven, Rev. Mod. Phys. 75, 1 (2002)
18H. Hanson, L. P. Kouwenhoven, J. R. Petta, S. Tarucha, and L. M. K. Vandersypen, Rev. Mod. Phys. 79, 1217 (2007)
19F. A. Zwanenburg, A. S. Dzurak, A. Morelo, M. Y. Simmons, L. C. L. Hollenberg, G. Klimeck, S. Rogge, S. N. Coppersmith, and M. A. Eriksson, Rev. Mod. Phys. 85, 961 (2013)
20M. D. Stewart and N. M. Zimmerman, Applied Sciences 6, 187 (2016)
21N. M. Zimmerman, W. H. Huber, B. Simonds, E. Hourdakis, A. Fujiwara, Y. Ono, Y. Takahashi, H. Inokawa, M. Furlan, and M. W. Keller, Journal of Applied Physics 104, 033710 (2008)
22W. H. Huber, S. B. Martin, and N. M. Zimmerman, in Experimental Implementation of Quantum Computation (IQC01), Vol. 76, edited by R. Clark (Rinton Press, NJ, 2001).
23N. M. Zimmerman, W. H. Huber, A. Fujiwara, and Y. Takahashi, Applied Physics Letters 79, 3188 (2001)
24N. M. Zimmerman, B. J. Simonds, A. Fujiwara, Y. Ono, Y. Takahashi, and H. Inokawa, Applied Physics Letters 90, 033507 (2007)
25N. M. Zimmerman, C.-H. Yang, N. S. Lai, W. H. Lim, and A. S. Dzurak, Nanotechnology 25, 405201 (2014)
26B. M. Freeman, J. S. Schoenfield, and H. Jiang, Applied Physics Letters 108, 253108 (2016) https://doi.org/10.1063/1.4954700.
27L. A. Tracy, T. M. Lu, N. C. Bishop, G. A. T. Eyck, T. Phym, J. R. Wendt, M. P. Lilly, and M. S. Carroll, Applied Physics Letters 103, 143115 (2013)
28M. Rudolph, B. Sarabi, R. Murray, M. S. Carroll, and N. Zimmerman, arXiv:1801.07776.
29A. Rossi, T. Tanttu, F. E. Hudson, Y. Sun, M. Möttönen, and A. S. Dzurak, J. Vis. Exp. 1023512 (2015)
30B. Hu and C. H. Yang, Phys. Rev. B 80, 075310 (2009)
31K. Nabors and J. White, IEEE Trans. Comp.-Aided Des. 10, 1447 (1991)