The VERITAS Upgraded Telescope-Level Trigger Systems: Technical Details and Performance Characterization

**Benjamin Zitzer**, for the VERITAS Collaboration.

1 Argonne National Laboratory

bzitzer@anl.gov

**Abstract:** VERITAS is an array of imaging atmospheric Cherenkov telescopes sensitive to gamma rays in the energy range between ~100 GeV and ~50 TeV. The instrument underwent an upgrade of the camera triggers in November 2011. The new systems use 400 MHz Xilinx Virtex-5 FPGAs for the pixel neighbor coincidence logic necessary to produce a camera-level trigger. The upgraded systems are capable of time-aligning individual triggering pixels to within ~0.2 nanoseconds, allowing for an operational pixel-to-pixel coincidence window of ~5 nanoseconds. This reduced coincidence window provides improved rejection of night-sky background (NSB) which permits a reduction of the energy threshold at the trigger level. The use of FPGAs allows for the future implementation of a topological trigger capable of discriminating events based on an image moment analysis of a bit-wise hit pattern. As part of the commissioning phase for the trigger upgrade, the hardware was initially installed in a single telescope in “parallel” to the (then) current system. This allowed for the detailed performance characterization of the new system relative to the pre-existing trigger. Here we present technical details of the upgraded VERITAS camera trigger system and outline the details of these performance studies.

**Keywords:** Trigger System, VERITAS, Upgrade, IACTs, FPGA

## 1 Introduction

VERITAS (Very Energetic Radiation Imaging Telescope Array System) is an array of four imaging atmospheric Cherenkov telescopes (IACTs) located in southern Arizona, USA, for observing the northern sky in very-high-energy (VHE) gamma rays (above 100 GeV). IACTs detect the Cherenkov light emitted from particles interacting in the Earth’s atmosphere. Primary particles (such as gamma rays and cosmic hadrons) interact in the upper atmosphere, creating showers of secondary particles. Energetic particles in the shower give rise to a Cherenkov light pool that can be seen by IACTs such as VERITAS. Each VERITAS telescope employs a 12m diameter tessellated mirror to reflect the Cherenkov images onto cameras composed of 499 PhotoMultiplier Tubes (PMTs) [1].

IACTs are limited at the lowest energies because of the steeply rising trigger rate produced by the night-sky background (NSB) light (starlight) and by cosmic rays (CRs, dominated by protons, muons and electrons). Cherenkov air showers that are initiated by gamma rays are typically seen as roughly elliptical in a single telescope with a duration of less than 10 ns. NSB events occur in single PMTs with random timing with respect to other NSB events. Showers initiated by CR protons are typically larger and rounder than gamma-ray events. Muon events typically appear as arcs or rings in the camera. VERITAS employs a three-level trigger system to reduce the number of background events. At the first level of triggering (L1), a constant-fraction discriminator (CFD) requires a PMT pulse height above a programmable threshold (typically set around 5-6 photoelectrons). The second level of triggering (L2) requires a L1 signal in at least three adjacent PMTs within a timing coincidence window. A third level of triggering (L3) requires a L2 trigger in at least 2 telescopes within a 50 ns coincidence window. Events which pass the L3 trigger are readout by the data acquisition system and recorded for use in the offline analysis. The data acquisition consists of 500 Msample/s FADCs, which digitize the PMT waveforms and stores them in a 64µs memory buffer [1]. The telescope-level trigger for VERITAS was replaced in November 2011 with a FPGA-based system.

At the single-telescope level, exploiting the event topology for gamma-ray events is not new. The Whipple 10m and the University of Durham telescopes, which were a pioneering instruments in the field of IACTs, employed a nearest-neighbor logic trigger requirement before a similar design was implemented for VERITAS [1,2,3]. The upgraded telescope-level trigger, with more modern technology, including fast FPGAs, provides better pixel-to-pixel timing alignment and allow for a narrower coincidence time width compared to the then-current VERITAS trigger, but still requires the 3-fold neighboring pixel requirement.

## 2 Design of Trigger System

A photograph of the L2 crate for the VERITAS upgrade is shown in Figure 1. Each 9Ux160mm L2 crate contains three types of boards: ten input boards, three L1.5 boards, and one L2 board. A block diagram of the L2 is shown in Figure 2. The design of this trigger system has been discussed before in [4], [5], [6].

### 2.1 Input Boards and Backplane

Each of the 499 L1 outputs is a 13 ns wide emitter-coupled logic (ECL) pulse. These signals are routed to the input boards, which translate the ECL signals to Low-voltage differential signaling (LVDS). The signals are then sent through the high-speed custom VME backplane to the three L1.5 boards. The camera is divided into three L1.5 regions as shown in Figure 3. Pixel signals in overlapping L1.5 regions are copied to both neighboring L1.5 boards to give
Fig. 1: A photograph of the L2 crate for the VERITAS upgrade. The signal cables from the CFDs are unplugged.

a relatively flat triggering efficiency over the entire camera.

2.2 L1.5 Boards

The L1.5 board contains a Xilinx Virtex-5 FPGA that processes the coincidence neighbor logic. The Virtex-5 was chosen for its higher speed and specific cell structure. The higher speed allows for the logic to run significantly faster than the original system. The specific cell structure of the Virtex-5 allows computation of the coincidence equations in individual cells, resulting in a significantly enhanced ability to control the delay of each pixel before entering the coincidence equation. The usefulness of controlling the delay is discussed in the pixel timing alignment section.

Each L1 signal is at the center of a cell within the FPGA consisting of itself and up to six neighboring pixels around it. An L1 signal of the center pixel in the cell and two of the neighbor pixels is required for the trigger. The L1 signal for the pixels located in a overlap region (see Figure 3) may have two or three cells associated with it. The trigger is asynchronous, requiring only minimal overlap time between neighboring pixels before a trigger occurs, meaning that at no point is the data sampled. An additional programmable required overlap time called “detune” is used to control the coincidence gate width. The speed of the trigger is therefore only limited by the propagation delay within the FPGA and the lookup speed of the memory. Trigger bits that pass the neighboring pixel and timing requirements are sent to the L2 processor.

Fig. 2: Block diagram of the pattern trigger for the VERITAS upgrade. Note that the fiber optic data/command to/from L4 is not currently in use, but could potentially be used for a future VERITAS upgrade.

2.3 L2 Board

The L2 board in each telescope-level trigger crate serves as an OR gate between L1.5 boards, sending the L1.5 trigger bit to the L3 array trigger. The Virtex-4 FPGA in the L2 board also contains two time-to-digital converters (TDCs), each with time resolution of 50ps, which are utilized in the timing alignment procedure described in the timing alignment section. It provides the clock source for the L1.5 boards and has the capability of calculating the image moments (\(n, \Sigma x, \Sigma y, \Sigma x^2, \Sigma y^2, \Sigma xy\)) required for the topological trigger described briefly in the conclusions section.

3 Trigger System Performance

The telescope-level trigger for VERITAS was replaced in two days in November 2011, during full moonlight when the telescopes were not in operation, so there was no loss of science data to the experiment during installation. The performance and added benefits of the new trigger system are described in this section.

3.1 Efficiency Studies

Prior to the installation in November 2011, one of the new telescope-level trigger crates was installed in one of the telescopes to monitor the trigger efficiency in situ across the camera. The CFD cables were connected to the new telescope trigger and ECL signals were copied to the primary (pre-upgrade) primary telescope-level system using modified input boards (referred to as I/O boards). The trigger bit output (L2 signal) of the new telescope-level trigger was then sent to the FADCs into a channel with a dead PMT. This allowed event-by-event comparisons of the two triggers in various operating conditions, with a minimal amount of time lost to the experiment. Event topology and relative efficiency of both systems could then be explored in the offline analysis.

An example of one of the results of the efficiency study...
Fig. 4: Efficiency over a VERITAS camera map of the upgraded telescope-level trigger to the pre-upgrade trigger. Each pixel shows the ratio of number of CFD hits of both triggers firing to only the pre-upgrade trigger firing. Note that the scale is from 99% to 100% and that the ratio cannot exceed 100%. Dead PMTs in the camera appear black in this map.

is shown in Figure 4. It shows the ratio of the L1 rates when both systems triggered on the same event to number of times the pre-upgrade system triggered. This efficiency ratio therefore cannot be over 100%. Figure 4 shows that both systems trigger together for $\sim 99.5\%$ of all events used in the offline analysis. The coincidence width that was chosen for the data shown here was one where the coincidence widths of both triggers were closely matched ($\sim 9\,\text{ns}$). Figure 4 indicates no regions of inefficiency across the camera. This was typical for all VERITAS operations when both triggers were functioning properly and the upgrade trigger was time aligned (next section).

### 3.2 Pixel Timing Alignment

Without any sort of pixel alignment, the relative pixel-to-pixel difference in arrival time of leading CFD edges in the L1.5 board is within a window of a few nanoseconds, due to transit time differences of the PMTs, signal cables, CFDs, CFD cables, input boards and the routing in the backplane. In order to ensure that all CFD signals reach the coincidence logic within the L1.5 boards within a window of $\pm 1\,\text{ns}$, a timing alignment procedure is implemented. This requires careful control over the skew and overall delay within the internal routing of the L1.5 boards, as well as the L1.5 FPGAs and the L2 FPGA coincidence signal. The L1.5 FPGAs can be programmed to delay individual input signals in steps of 72ps up to $\sim 10\,\text{ns}$ before they are sent through the coincidence logic. This careful control over the pixel-to-pixel timing allows to narrow the gate width to as little as $\sim 3\,\text{ns}$ while keeping the trigger efficiency relatively flat over the camera’s surface.

The procedure for the timing alignment requires the LED flasher used for calibration running and the telescopes pointing at dark patch of sky at a high elevation to reduce the amount of NSB the telescopes are exposed to during the process. The CFD thresholds are set at a higher threshold to help reduce NSB contamination. Seven different 3-fold coincidence patterns per pixel are tested multiple times and averaged to find the mean arrival time for that pixel. The delay of that pixel is measured relative to the average of two fixed coincidence sets, one in each of the other two L1.5 regions of the camera. These fixed sets are a reference time for all coincidence sets. A delay time is then calculated and added to move that pixel arrival time closer to the mean of the reference coincidence sets.

Figure 5 shows the relative pixel-to-pixel timing for one of the telescopes before and after the alignment procedure. The pixels are plotted relative to the slowest pixel arrival time in the distribution prior to timing alignment.

**Fig. 5:** Histograms showing the relative delays of the CFD leading edges before and after the timing alignment procedure. The pixels are plotted relative to the slowest pixel arrival time in the distribution prior to timing alignment.

3.3 Diagnostic Tools

The upgraded telescope-level trigger has a VME control through a CORBA interface to a GUI on a PC, allowing the VERITAS observers to monitor and control the trigger during operation. The included features are: L1 rate monitors, enable/disable controls for each of the CFDs, control over the timing alignment and coincidence gate width. A pre-scaling factor also exists within the upgraded telescope-level trigger that is also controlled by the GUI. The pre-scaling factor is used for taking single telescope runs dedicated to measuring CR muons. Due to their small collection area and spacing between the telescopes, requiring two telescopes for the array trigger during normal operations removes many of the muons at the trigger level.

3.4 Adjustable Coincidence Width

The pre-upgrade telescope-level trigger has a fixed coincidence gate width of 8-10 ns, depending on telescope. This value was fixed and could not be changed after installation, along with the pixel-to-pixel timing. The new FPGA-based trigger includes firmware optimized for rapidly solving trigger equations and pixel alignment to $\pm 1\,\text{ns}$, and is capable of yielding a coincidence gate width down to 3 ns. The L1.5 FPGA has a programmable parameter called ‘detune’ which is an extra required overlap width required for a trig-
timing alignment allows for a narrower coincidence gate width down to 3 ns with uniform camera efficiency. Studies using Crab Nebula data with varying coincidence widths prior to the camera upgrade showed that 5 ns was optimal for gamma-ray efficiency. New diagnostic features allow VERITAS observers greater diagnostic and control that was not available before.

The upgraded trigger has the hardware capabilities for two potential VERITAS upgrades beyond this current one: a muon trigger and a topological trigger (or L4). The FGPAs in the L1.5 and L2 boards could be utilized to pick out simple ring or arc patterns in L1 signals that are strong muon indicators in IACT cameras. The L4 trigger requires that each L2 board would calculate the image moments and send that information to a central L4 processor which would discriminate hadron events from gamma-ray events at the hardware level. This has been proposed as the array-level trigger design for CTA and work is in progress to apply lessons learned from this trigger upgrade to CTA.

## Acknowledgment
This research is supported by grants from the U.S. Department of Energy Office of Science, the U.S. National Science Foundation and the Smithsonian Institution, by NSERC in Canada, by Science Foundation Ireland (SFI 10/RF-P/AST2748) and by STFC in the U.K. We acknowledge the excellent work of the technical support staff at the Fred Lawrence Whipple Observatory and at the collaborating institutions in the construction and operation of the instrument.

## References

1. J. Holder et. al. *The First VERITAS Telescope*. Astroparticle Physics, 25:391-401, (2006)
2. S. M. Bradbury and H. J. Rose. *Pattern Recognition Trigger Electronics for an Imaging Atmospheric Cherenkov Telescope*, Nucl. Instrum. Meth., A481:521-528,(2002).
3. P., Armstrong, P. M., Chadwick, P. J.,Cottle, et al., *Experimental Astronomy, 9, 51, 1999.
4. J. Anderson et al., *Proc. of Nuclear Science Symposium*, IEEE, 7, 2773 (2008).
5. F. Krennrich et al., *Proc. of the 4th High-Energy Gamma-Ray Astronomy Meeting*, Heidelberg, 894 (2008).
6. B. Zitzer et al., *Proc. of the Technology Instrumentation in Particle Physics 2011*, Chicago (2011).
7. D. Kieda et al., *These proceedings.*