LogicNets: Co-Designed Neural Networks and Circuits for Extreme-Throughput Applications

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Abstract—Deployment of deep neural networks for applications that require very high throughput or extremely low latency is a severe computational challenge, further exacerbated by inefficiencies in mapping the computation to hardware. We present a novel method for designing neural network topologies that directly map to a highly efficient FPGA implementation. By exploiting the equivalence of artificial neurons with quantized inputs/outputs and truth tables, we can train quantized neural networks that can be directly converted to a netlist of truth tables, and subsequently deployed as a highly pipelinable, massively parallel FPGA circuit. However, the neural network topology requires careful consideration since the hardware cost of truth tables grows exponentially with neuron fan-in. To obtain smaller networks where the whole netlist can be placed-and-routed onto a single FPGA, we derive a fan-in driven hardware cost model to guide topology design, and combine high sparsity with low-bit activation quantization to limit the neuron fan-in. We evaluate our approach on two tasks with very high intrinsic throughput requirements in high-energy physics and network intrusion detection. We show that the combination of sparsity and low-bit activation quantization results in high-speed circuits with small logic depth and low LUT cost, demonstrating competitive accuracy with less than 15 ns of inference latency and throughput in the hundreds of millions of inferences per second.

I. INTRODUCTION

Deep Neural Networks (DNNs) have a wide application scope beyond the highly-popular computer vision use cases, promising to replace manual algorithmic implementations in many application domains. Certain applications, such as data collection from particle physics experiments [1], line-rate filtering of packets for network intrusion detection [2] and wireless communications [3], have stringent real-time requirements and extremely high data-rates. Replacing parts of such extreme-throughput applications with machine-learned components requires highly specialized DNN implementations that offer inference rates reaching hundreds of millions of samples per second with sub-microsecond latency. This is the key challenge we try to address in this work: how can we build DNN implementations that are able to meet the performance and latency constraints for extreme-throughput applications?

Popular hardware platform options for accelerating DNN inference include GPGPUs, FPGA overlays and specialized tensor processors [4]. Most of these alternatives apply the traditional paradigm in computer design where hardware and software are designed separately, bridged by a compiler that generates instructions to schedule the required computation onto available hardware. However, this flexibility typically comes at the cost of performance overheads, making it difficult to apply this approach to extreme-throughput applications. Prior work [1], [5]–[7] demonstrated that specialized co-design approaches are able to produce FPGA DNN implementations that yield increased throughput, while still offering the ability to reconfigure to address changing requirements.

In this paper, we present a novel method named LogicNets for co-designing DNN topologies that map directly to an efficient FPGA implementation for extreme-throughput applications. Our scheme is based on the observation that artificial neurons with quantized inputs and outputs can be converted to truth tables. However, an efficient FPGA implementation for a truth table is generally only possible when the number of inputs is small. By limiting neuron fan-in using activation quantization and sparsity, we show how we can design DNN topologies that are still trainable using standard backpropagation, and can be mapped directly to an equivalent hardware circuit with small combinatorial depth. DNNs designed and trained in this manner result in fast and efficient FPGA implementations that can fulfill the performance requirements for extreme-throughput applications. Extending on our abstract in [8], this paper makes the following contributions:

• We describe LogicNets, a DNN-hardware co-design methodology that allows trained quantized networks to be directly converted to an equivalent hardware netlist of truth tables.
• We exploit sparsity and quantization to reduce the neuron fan-in, and provide an analytical cost model to quickly estimate the required FPGA resources to guide topology design.
• We develop a PyTorch library to train sparse, quantized topologies and convert them to Verilog netlists.
• We empirically evaluate our approach on two extreme-throughput tasks, demonstrating FPGA implementations with competitive accuracy and throughput in the hundreds of millions of inferences per second.

II. BACKGROUND

In this section, we briefly describe prior work relating to DNN inference acceleration on FPGAs, and schemes previously used to construct quantized and sparsely-connected DNNs.
A. Sparse and Quantized Neural Networks

In a sparse neural network, each layer of neurons receives inputs from only a few connections of the previous layer of activations, in contrast to dense networks where all previous layer activations are inputs to each neuron of the next layer. Numerous techniques to build sparse DNN topologies exist, including learned sparsity \[9\], pruning techniques \[10\] and a priori fixed sparsity \[11\] which we utilize in this work due to its relative simplicity. Quantization involves restricting weights, activations or both to a set of discrete values. To preserve DNN accuracy with low-bit quantization (e.g. \(\leq 4\)-bits) it is typically necessary to use specialized techniques during training, such as using the Straight-Through Estimator (STE) \[12\] to propagate gradients through non-differentiable quantizers and learned scale factors to reduce approximation error. We refer the reader to the survey by Guo et al. \[13\] for further details.

B. Prior Work on FPGA DNN Inference

DNN inference typically consists of applying a sequence of multiply-accumulates (MACs), followed by a nonlinear activation function. Many alternatives exist when mapping these computations to the FPGA fabric and a large body of prior work exists on FPGA DNN inference; here, we only cover the works closely related to ours and refer the reader to a recent survey by Zhao et al. \[15\] for further reading. We organize our discussion of prior work according to the presence or absence of explicit weight storage, MAC and activation datapaths in the proposed architecture, as illustrated in Figure 1.

Weights in LUT equations. Figure 1a shows architectures with network weights “baked in” into LUT equations, but parts of the MAC and activation datapaths still exist. This enables greater performance with fully unrolled (non-time-multiplexed) implementations without a control path, but is less flexible. Wang et al. \[7\] introduce LUTNet, a LUT-optimized FPGA inference scheme which achieves high LUT density. \[7\] take a pruned version of ReBNet \[16\] in which some of the XNOR-popcount operations are mapped more effectively to \(k\)-input LUTs, although explicit popcount and thresholding datapaths are still present and occupy significant resources. Murovic et al. \[2\] implement binarized networks which have been fully unrolled and implemented directly into LUTs of a small FPGA, although explicit accumulation and activation datapaths are still present. This unrolling allows the synthesis optimization tool to potentially simplify significant portions of the compute logic. Duarte et al. \[1\] present a package called hls4ml which generates high-level synthesis-based FPGA designs which supports two axes of folding, but can also generate full-unrolled designs. \[1\] operates at higher bit-widths (8 or 16-bit) and maps significant portions of the compute to the DSP blocks.

No explicit datapath. Figure 1b shows the architecture proposed in this work, where all operations and weights are packed into a truth table and no explicit MAC or activation datapath is present. Nazemi et al. \[14\] introduce NullaNet, which proposes converting activation-quantized neural networks into large truth tables in a similar fashion to this work. Their stated goal is reducing the number of memory accesses, whereas LogicNets aims to co-design DNNs that can yield FPGA circuits that offer extremely high throughput and low latency. Key differences between NullaNet and this work are as follows:

- NullaNet only considers densely connected networks and suffers from high fan-in, we use sparse topologies to avoid this problem (Section III-C).
- NullaNet uses a lossy truth table sampling method to overcome the fan-in problem which gives an approximation of the DNN, whereas we use a lossless method (Section III-A).
- NullaNet only considers binary quantization of activations, we consider several low-precision variants, which is key to achieving higher accuracy (Section V-B).

III. BUILDING DNNs FROM SMALL TRUTH TABLES

In this section, we explain the core concepts that form the foundations of LogicNets. As the performance demands for extreme-throughput applications are so high, the available hardware must be utilized to its full potential. We aim to answer the following question: given that the building blocks of FPGA hardware are small truth tables that can implement any function, how can we design DNN topologies that map well to these building blocks?

A. Equivalence of Neurons and Truth Tables

The foundation of LogicNets is the equivalence of artificial neurons with quantized inputs/outputs and truth tables. Consider an artificial neuron with \(C_{in}\) different inputs, where each input is \(\beta\) bits wide, and let the neuron produce a single \(\beta\)-bit output. Let \(X\) be the total number of input bits or fan-in, i.e. \(X = \sum_{i=0}^{C_{in}} \beta\) and \(Y = \beta\) be the total number of output bits. Regardless of the internal complexity of the neuron, we can always implement its functionality with an \(X\)-input, \(Y\)-output (denoted \(X : Y\)) truth table by enumerating all of its possible combinations.
2^X different inputs, observing the output, and recording it into the truth table.

In LogicNets, we refer to the Verilog implementation of an X:Y truth table as a Hardware Building Block (HBB), and any trained artificial neuron that can be converted into an HBB as a Neuron Equivalent (NEQ). Since the internal complexity of NEQs does not matter as long as the number of input-output bits are fixed, we can add components that makes the DNN training process easier into the NEQ. Figure 2 illustrates this for a 6:1 NEQ with floating point weights and batch normalization, with six FP32 values for the weights and four for the batch normalization parameters, requiring 10 · 32 = 320 bits of storage. The equivalent HBB only requires 64 bits to store the truth table, which is 5× smaller.

B. The FPGA LUT Cost of Large Truth Tables

To implement NEQs with more than one input or output, we need HBBs with larger X values, which can be implemented by combinations of smaller FPGA LUTs. For instance, the output of two 6:1 LUTs can be fed into a third 6:1 LUT to act as a multiplexer, implementing a 7:1 LUTs using three 6:1 LUTs. For higher output bitwidth Y the cost scales linearly, if each additional output bit is produced by adding a copy of the table. Generalizing this, we can analytically estimate the number of 6:1 FPGA LUTs required to implement an X:Y HBB using Equation 1

\[
\text{LUTCost}(X, Y) = \frac{Y}{3} \cdot (2^{X-4} - (-1)^X)
\]

However, scaling up X in this manner is expensive: the number of LUTs needed grows exponentially with X. For instance, implementing a single 32:1 NEQ would require close to a hundred million 6:1 LUTs, which is much larger than even the largest FP3Gs available today. Thus, it is critical to keep the fan-in X small enough so that each NEQ in the topology has a reasonably small LUT cost.

C. Designing Topologies with Restricted Fan-In

Modern DNN topologies do not necessarily restrict neuron fan-in, which makes them impractical for direct mapping to HBBs. In LogicNets, we propose to co-design DNN topologies with awareness of the FPGA hardware implementation cost by restricting the fan-in of each artificial neuron. Recalling that the fan-in is computed as \( X = \sum_{i=0}^{C_{in}} \beta \), we observe that we have two key topological parameters to control it:

- **Number of inputs \( C_{in} \):** A DNN may have hundreds of neurons per layer, and connecting a neuron’s inputs to every other neuron in the previous layer will result in an intracellularly large fan-in. We take inspiration from the developments in sparse topologies (Section II-A), connecting each neuron to \( \gamma \) previous neurons, with a \( \gamma \) much smaller than the previous layer size.

- **Bitwidth of inputs \( \beta \):** The bitwidth of the activations from the previous layer also has a large impact on fan-in X. We apply training-time techniques developed in prior work (Section II-A) to quantize the activations to \( \leq 4 \)-bits, which reduces the fan-in substantially.

With these fan-in restrictions in place, we can explore topologies with different number of neurons and layers while avoiding the exponential growth in LUT cost, using the cost model to guide the exploration. To compute the total FPGA resource cost for a network, we can simply sum the resources taken up by each NEQ in the topology. We provide an example for the network illustrated in Figure 3. Here, each neuron output is quantized to \( \beta = 2 \) bits, and is connected to \( \gamma = 6 \) outputs from the previous layer as its input. Thus, \( X = 6 \cdot 2 = 12 \) and \( Y = 2 \). According to Equation 1 the cost for a 12-bit-input, 2-bit-output NEQ is \( \text{LUTCost}(12, 2) = \frac{2}{3} \cdot (2^{12-4} - (-1)^{12}) = 170 \) 6:1 LUTs. Since there are 128 such NEQs in total, the estimated cost for this network is 128 · 170 = 21760 6:1 LUTs.

IV. THE LOGICNETS DESIGN FLOW AND IMPLEMENTATION

Having explored the foundational ideas in Section III, we now present LogicNets as a three-step design flow to train DNNs that map directly and efficiently to FPGAs:

1) Define Hardware Building Blocks (HBB) and Neuron Equivalents (NEQ)

2) Define and train a DNN of NEQs in PyTorch then convert to netlist of HBBs

3) Postprocess the netlist, synthesize to obtain a bitfile

Figure 4 illustrates the steps in the LogicNets design flow. We have implemented a prototype of this design flow with a PyTorch library in order to enable faster design space exploration. In the following sections, we describe each step in greater detail.

A. Define HBBs and NEQs

As described in Section III-A, NEQs and HBBs constitute the building blocks of LogicNets on the PyTorch and Verilog side, respectively. The first step in the design flow is to identify the range of X:Y values that yield HBBs with reasonable LUT cost, and to define corresponding NEQs in PyTorch that can be trained with the sparsity and activation quantization restrictions in place. These can be NEQs that map to single 6:1 or 5:2 FPGA LUTs, or a generic X:Y truth table that will be
implemented by the synthesis tool. In this work, we add batch normalization followed by uniform quantization with learned scale factors using Brevitas [17] for better accuracy and easier training. The first step needs to be performed only once per FPGA device family, since the identified building blocks can be used to construct multiple different topologies.

B. Train and convert a network of NEQs

The second step is followed for each new DNN that needs to be trained and deployed, and takes place in the PyTorch machine learning framework. Using the available NEQs identified in Step 1, a deep neural network topology is constructed by instantiating NEQs and connecting them together. We use the approach described in [11] to provide fixed random sparsity with the desired per-neuron fan-in. To guide topology design, our library implements the analytical model from Equation 1 to estimate the required FPGA resources prior to training. Once the topology is defined, the DNN is trained in PyTorch using standard DNN optimizers and backpropagation. Methods applied to improve standard DNN training such as PyTorch using standard DNN optimizers and backpropagation. To assess LogicNets on this domain we use the UNSWNB15 dataset [20] which provides example inputs and outputs for each input combination, and we leave it to the synthesis tool to map the ROMs to FPGA LUTs.

C. Postprocessing, Synthesis and Deployment

Any optimization admitted by a netlist can be applied as the postprocessing step. For instance, a heuristic logic minimizer can be applied to the network to use fewer LUTs, pipeline registers can be inserted between the layers to increase the clock frequency, or the netlist can be split up into chunks for mapping to a smaller FPGA with dynamic partial reconfiguration, one chunk at a time. In this paper, we focus on single-FPGA implementations for extreme-throughput applications and only consider register insertion between layers for postprocessing, as shown in Figure 4c. After any preprocessing is complete, the final netlist is processed with synthesis, place-and-route algorithms to yield an FPGA bitfile. As our results in Section V-C indicate, synthesis-time optimizations such as heuristic logic minimization can yield significant hardware cost savings, effectively pruning the network further to make it more sparse.

V. Evaluation

In order to evaluate LogicNets we picked the following tasks with extreme-throughput requirements from two domains:

- **Jet Substructure Classification (JSC):** Large-scale physics experiments such as those in CERN produce terabytes of instrumentation data every second, which is processed by a hierarchy of triggers to filter out the interesting results. Recent work by Duarte et al. [1] successfully applied DNNs to the Jet Substructure Classification (JSC) task. This task targets the FPGA-based triggers of the CERN ATLAS and CMS experiments, which must be pipelined to handle a data rate of 40 MHz and limit response latency to less than a microsecond. We use the formulation from Duarte et al. [1] for JSC as a 16-input, 5-output classification task, and refer the reader to their work for a more detailed explanation of the task.
- **Network Intrusion Detection (NID):** FPGAs are commonly used for implementing high-performance packet processing systems that still provide a degree of programmability [18]. An advantage of such systems is their ability to facilitate stronger network security by detecting malicious or suspicious network packets, which may be implemented using DNNs [19]. To avoid introducing bottlenecks on the network, the DNN implementation must be capable of detecting malicious ones at line rate, which can be millions of packets per second, and is expected to increase further as next-generation networking solutions provide increased throughput. To assess LogicNets on this domain we use the UNSWNB15 dataset [22] which provides example packets labeled as bad (0) or normal (1) with 49 generated input features extracted from simulated modern intrusion attacks. We follow the approach by Murovic et al. [2] in terms of dataset preprocessing and feature conversion.

We trained a number of sparsely-connected, activation-quantized MLPs on the chosen tasks using the LogicNets.
PyTorch library. All layers use the same $\gamma$ and $\beta$, except when $\gamma_i$, $\gamma_o$, $\beta_i$ and $\beta_o$ are used to specify the first and last layers’ fan-in and bitwidth, respectively. Based on the feedback from our cost model, we limit $X = \beta \cdot \gamma \leq 15$ in our exploration to focus on LogicNets implementable on a single FPGA. All networks presented here are trained for 1000 epochs, with a mini-batch size of 1024, using the ADAM optimizer and a step decay learning rate schedule starting from 0.1. Once the training is complete, we generate Verilog from the trained network as described in Section IV-B. We use Xilinx Vivado 2018.3 in out-of-context mode with the default settings for synthesis and Flow_PerfOptimized_high for place and route without any manual placement constraints, targeting the xcvu9p-flgb2104-2-i FPGA part. We insert registers at the network input, output and between every layer, and constrain the clock to 1 ns to achieve the highest possible frequency. The correctness of the generated hardware is verified by performing post-synthesis simulation and ensuring the same results as the original PyTorch network are returned.

### A. Overview of Key Results

Table I presents several networks obtained using LogicNets on the JSC and NID tasks, picked to illustrate interesting points from our partial design space exploration. The table names each datapoint by indicating which task the network was trained on, specifies the network topology and quantization, the test accuracy, and FPGA resources from both the analytical model and post-synthesis results. We make the following observations:

**Scalable resource footprint.** LogicNets-style models expose many topological knobs to control the size of the network, which translates into FPGA resource savings at the cost of some accuracy. This is reflected in the variety of neurons per layer, $\beta$ and $\gamma$ in Table I. For instance, JSC-S is able to achieve close to 68% accuracy using only 214 LUTs, while JSC-L offers 4% points better accuracy at the cost of 37.9k LUTs.

**Simple, high-frequency circuits.** LogicNets yield simple circuits by design, with as little as a single level of LUTs between registers when neuron fan-in is constrained to be $\beta \cdot \gamma \leq 6$. This is the case for JSC-S, which has a reported $F_{\text{max}}$ of 1.5 GHz. Although this frequency cannot be achieved in practice due to limitations on the global clock network of the FPGA, the positive slack yielded by the simplicity of LogicNets-style netlists is still quite significant and would facilitate timing closure when integrating LogicNets-style DNNs into other high-speed designs. Larger LogicNets-designs such as NID-L with $\beta \cdot \gamma = 15$ require more levels of logic and resources and are more challenging to place and route, but are still capable of achieving high clock rates over 400 MHz.

**Competitive accuracy with sparsity and quantization.** We are able to obtain datapoints which offer accuracy over 70% for the JSC task and over 90% for the NID task, which is competitive with the accuracy reported by related work (Section V-E). We expect accuracy to further increase by using better sparsity methods compared to fixed random sparsity, such as magnitude pruning and sparse momentum, but this investigation is left for future work.

### B. Impact of Activation Bitwidth

To better understand the impact of activation bitwidth ($\beta$) on accuracy, we train a variety of topologies with different number of neurons, fan-ins ($\gamma$) and activation bitwidths ($\beta$), plotting the accuracy on the JSC task against the analytical LUT cost in Figure 5, grouping the datapoints by $\beta$. We observe a general increase in accuracy for the larger models, and some interesting behavior regarding $\beta$. Although binary activations generally have lower LUT cost, we observe that higher $\beta$ can yield higher accuracy at similar LUT cost. For instance, the lowest-cost $\beta = 2$ datapoint offers 88.7% accuracy with 2120 LUTs, whereas the highest-accuracy binary result provides 85.3% with 7392 LUTs. A similar trend is observed for $\beta = 3$, although the accuracy improvement over $\beta = 2$ is smaller.

Figure 6 presents this from another perspective, where LogicNets with the same number of neurons but different $\beta$ and $\gamma$ are clustered in columns. Training the same number of neurons with greater activation bitwidth yields greater accuracy. Increasing the number of neurons improves the results slightly for $\beta = 1$ but brings little to no benefit for $\beta > 1$. In general, it is difficult to estimate the effect of DNN hyperparameters...
on accuracy, but our experiments indicate that the activation bitwidth $\beta$ is vital to achieving good accuracy for LogicNets.

### C. Lossless Pruning via Synthesis Optimizations

There are notable differences in the LUT counts yielded by the analytical model and post-synthesis results in Table II, where the post-synthesis LUT counts are on average $39 \times$ smaller than the LUT cost predicted by the analytical model. To understand why, we take a closer look at the post-synthesis utilization data for NID-S as reported by Vivado. Figure 7 illustrates the pre- and post-synthesis resource usage per layer, and the registers between layers. The extent of pruning is evident in both LUT and FF counts, indicating that many neurons are removed entirely, while others are implemented with much smaller cost. The drastic reduction in resources can be attributed to two effects. Firstly, many NEQs have no path to output owing to a combination of fixed random sparsity, the chosen $\gamma$ and neuron counts. This is reflected in the post-synthesis results, which removes many unconnected neurons and registers due to the over-provisioned topology, resulting in fewer LUTs than what is predicted by our basic analytical model due to effective reduction of $X$ and number of neurons. The JSC models are less over-provisioned and exhibit smaller post-synthesis savings of $1.5–8 \times$. The second effect is the actual cost of single HBBs, which is 682 LUTs for the 14:2 HBB according to the analytical model. Examining the per-neuron resource costs, we observe LUT costs ranging from 10–262, as well as instances F7MUX and F8MUX primitives. This indicates that significant savings of $2.6–68 \times$ can be achieved by applying heuristic logic minimization on the learned HBB functions. We leave a more in-depth study of LogicNets logic minimization for future work.

### D. Limitations

Based on our evaluation, we identify two key limitations of our current approach. The first is the inability to map dense networks with high fan-in neurons commonly used in machine learning, instead requiring custom topologies that apply fan-in restrictions via sparsity and activation quantization. The second is the large design space with combinations of layer and neuron counts, activation bitwidths and fan-ins that must be explored to find suitable networks of sufficiently high accuracy and low resource cost. Although these may be acceptable limitations for extreme-throughput applications that commonly require specialized design effort, we hope to address these limitations in future work to broaden the scope of LogicNets.

### E. Comparison to Related Work

We compare LogicNets to two prior works on extreme-throughput, fully-unfolded (II=1) FPGA implementations on these domains, according to the metrics presented in Table II. For the JSC task, we take the work by Duarte et al. [1] as our baseline, which reports an accuracy of 75% and presents a fully-unrolled FPGA implementation of a pruned and 16-bit quantized and 30% sparse neural network. To focus on the implementation of the core neural network part itself, we exclude the 5-cycle softmax execution from the latency. Our JSC-L implementation is able to offer $1.9 \times$ higher throughput and $3.8 \times$ lower latency at the cost of 3.2% points lower accuracy. Since JSC-L uses less than half of the LUTs compared to [1] and no DSP slices, the accuracy could be potentially increased further by using a larger LogicNets-style network and more resources. For the NID task, we compare against Murovic et al. [2], who implement a dense binarized neural network achieving 90.1% accuracy as a fully-unfolded, combinatorial circuit without any registers. The LogicNets NID-M implementation outperforms their solution in terms of all metrics, offering 1.2% points higher accuracy, $9.2 \times$ higher throughput and $1.9 \times$ lower latency using $3.2 \times$ fewer LUTs.

### VI. Conclusion and Future Work

In this work, we have investigated how DNN topologies that map well to FPGA building blocks can be constructed to obtain efficient implementations for extreme-throughput applications. Noting that quantized neurons with limited fan-in can be converted into small truth tables, we have proposed a flow to design sparse, quantized topologies that map to highly efficient FPGA implementations. On two tasks with extreme-throughput requirements, we were able to demonstrate implementations with competitive accuracy, low latency and throughput in the hundreds of millions of inferences per second.

LogicNets opens up a wide array of possible future work owing to its cross-stack nature which spans machine learning, compilation and FPGA synthesis. On the machine learning

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**TABLE II**

| Work   | Accuracy | $F_{clk}$ | Latency | Resources |
|--------|----------|-----------|----------|-----------|
| JSC-L  | 71.8%    | 384 MHz   | 13 ns    | 37.9k LUT|
| [1]    | 75%      | 200 MHz   | 50 ns    | 88k LUT, 1k DSP |
| NID-M  | 91.30%   | 471 MHz   | 10.5 ns  | 15.9k LUT |
| [2]    | 90.1%    | 51 MHz    | 19.6 ns  | 51k LUT   |

Fig. 6. Accuracy impact of $\beta$ with number of neurons.

Fig. 7. Post-synthesis resource breakdown for NID-S.
side, we plan to explore training-time methods to increase the accuracy of sparse and quantized topologies, exploring the possibilities for sparse convolutions, as well as mixing LogicNets-style layers with more conventional ones in the same topology in order to increase the accuracy and apply it to more difficult problems. On the tooling and hardware synthesis side, we hope to further study the benefits of heuristic logic minimization to design more accurate analytical cost models, as well as techniques to synthesize larger LogicNets models quickly and efficiently.

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