Phase Noise and Jitter in Digital Electronics

Claudio E. Calosso∗and Enrico Rubiola†

January 3, 2017

Abstract

This article explains phase noise, jitter, and some slower phenomena in digital integrated circuits, focusing on high-demanding, noise-critical applications. We introduce the concept of phase type and time type (for short, ϕ-type and x-type) phase noise. The rules for scaling the noise with frequency are chiefly determined by the spectral properties of these two basic types, by the aliasing phenomenon, and by the input and output circuits.

Then, we discuss the parameter extraction from experimental data and we report on the measured phase noise in some selected devices of different node size and complexity. We observed flicker noise between −80 and −130 dB/Hz at 1 Hz offset, and white noise down to −165 dB/Hz in some fortunate cases and using the appropriate tricks.

It turns out that flicker noise is proportional to the reciprocal of the volume of the transistor. This unpleasant conclusion is supported by a gedanken experiment.

Further experiments provide understanding on: (i) the interplay between noise sources in the internal PLL, often present in FPGAs; (ii) the chattering phenomenon, which consists in multiple bouncing at transitions; and (iii) thermal time constants, and their effect on phase wander and on the Allan variance.

Keywords: Phase Noise, Jitter, Aliasing, FPGA, Bouncing, Allan Variance, Thermal Stability.

1 Introduction

Timing analysis is generally driven by the design of logic functions. That is why specs like “the input must be stable 600 ps before the clock edge” are just countless. From this standpoint, it is sufficient to describe the fluctuations in terms of jitter. Broadly speaking, jitter is the time fluctuation, evaluated in
reference conditions. Because of the wide bandwidth, jitter is chiefly determined by the white noise. Notice that proper operation requires an analog bandwidth 3–4 times the switching frequency, and in turn up to a few GHz with nowadays components.

When the design comes to spectral analysis and to highly stable oscillators, language and requirements change radically. Fluctuations are generally described in terms of phase noise, expressed either as $S_\varphi(f)$ or $\mathcal{L}(f)$, and the low-frequency phenomena are no longer negligible. Low phase noise is crucial in radars [1] [2] [3], modern telecom [4], atomic frequency standards [5] and particle accelerators [6] [7], just to mention some.

In the rapidly changing world of digital electronics, the literature on phase noise is rather old and focuses on frequency dividers, either in TTL and ECL components [8] [9], or in transistor-level modeling. Other references found are more about data transfer in telecom networks than about components [10] [11] [12].

At the time of [8] [9], CMOS technology was used only in microprocessors and complex functions. Gate arrays and FPGAs came later, with a new rapid progress [13] [14] [15]. Interestingly for us, gate arrays and FPGAs bridge the gap between logical/computational functions and circuit-level design. The precise control on electrical signals that follows opens a new challenge in understanding noise. However, VLSI engineers are mostly concerned with noise margin, crosstalk, and power distribution [16]. Conversely, amplitude and phase noise are not studied.

The purpose of this article is to set the basic knowledge about phase noise, and to provide examples. We focus on the clock distribution because clock edges are the most critical ones for timing. This does not sounds a limitation, first because critical signals can be synchronized to a clock line, and second because a chip in charge of a highly critical operation should not perform multiple tasks ‘cross-talking’ at random with one another.

Designing the experiments was initially difficult. However, after a noise model and the first results were available, reproducing similar experiments is surprisingly simple. We hope that the reader will be able to port our ideas to other technologies and logic families. The reader may also learn about reverse engineering the noise.

2 Definitions, and Phase Noise Models

Phase noise is often expressed as the one-sided PSD $S_\varphi(f)$ of the random phase $\varphi(t)$. In technical literature we often find $\mathcal{L}(f)$, defined as $\mathcal{L}(f) = \frac{1}{2}S_\varphi(f)$ and given in dBc/Hz [17]. Alternatively, phase noise is represented as the phase time fluctuation $x(t)$, and its PSD $S_x(f)$. Since $x(t)$ is equivalent to $\varphi(t)$ converted...
| Noise Type                  | Dependence on $\nu_0$ | Main Equation | Derived Equation | Parameters |
|----------------------------|------------------------|---------------|------------------|------------|
| Pure phase type            | $C$                    | $1/\nu_0^2$   | $b_{-1} = h_{-1} / V_0^2$ | $k_{-1} = h_{-1} / 4\pi^2 \nu_0^2 V_0^2$ | $\sqrt{h_{-1}} / V_0$ [V] |
| (pure $\phi$-type)         |                        |               |                  |            |
| Aliased phase type         | $1/\nu_0$              | $1/\nu_0^3$   | $b_0 = B h_0 / V_0^2$ | $k_0 = h_0 B / 4\pi^2 \nu_0^3 V_0^2$ | $\sqrt{h_0 B} / V_0$ [V] |
| (aliased $\phi$-type)      |                        |               |                  |            |
| Pure time type             | $\nu_0^2$              | $C$           | $k_{-1} = C$     | $b_{-1} = 4\pi^2 \nu_0^2 k_{-1}$ | $\sqrt{k_{-1}}$ [s] |
| (pure $x$-type)            |                        |               |                  |            |
| Aliased time type          | $\nu_0$                | $1/\nu_0$     | $k_0 = J^2 / \nu_0$ | $b_0 = 4\pi^2 J^2 \nu_0$ | $J$ [s] |
| (aliased $x$-type)         |                        |               |                  |            |
into time, it holds that
\[ x(t) = \frac{1}{2\pi\nu_0} \varphi(t) \]  \[ \text{[s]} \] (1)

\[ S_x(f) = \frac{1}{4\pi^2\nu_0^2} S_\varphi(f) \]  \[ \text{[s}^2/\text{Hz}] \], (2)

where \( \nu_0 \) is the carrier frequency. Our notation is consistent with general literature [17, 18], yet for the choice of fonts for some specific quantities as a minor detail.

A model which is useful to describe phase noise is the polynomial law

\[ S_\varphi(f) = \sum_{j=m}^{0} b_j f^j \quad S_x(f) = \sum_{j=m}^{0} k_j f^j, \] (3)

where the integer \( m < 0 \) depends on the device. After (2), it holds that \( k_j = b_j / 4\pi^2\nu_0^2 \). The sum (3) describes the usual noise types: white phase noise \( b_0 \), flicker phase noise \( b_{-1} / f \), white frequency noise \( b_{-2} / f^2 \), etc. Common sense suggests that in two-port components, noise processes higher than \( 1/f \) (i.e., \( f^j, j < -1 \)) cannot extend over unlimitedly low frequencies, otherwise the input-output delay diverges in the long run.

The polynomial law is also used for the PSD of the voltage noise \( n(t) \)

\[ S_n(f) = \sum_{j=m}^{0} h_j f^j \]  \[ \text{[V}^2/\text{Hz}] \] (4)

(notice the font in \( h_j \), because \( h_j \) reserved for \( S_\varphi(f) = \sum_j h_j f^j \)). The reader familiar with analog electronics finds an obvious analogy with the parameter \( e_n \) \[ \text{[nV}/\sqrt{\text{Hz}}] \], specified separately for white and flicker noise.

The rms time fluctuation \( J \) can be calculated integrating \( S_x(f) \) over the system bandwidth (Parseval theorem)

\[ J^2 = \int_{f_L}^{f_H} S_x(f) \, df. \] (5)

The lower limit \( f_L \) is set by maximum differential delay in the system. The upper limit is \( f_H = \nu_0 \). The reason is that the fluctuations are sampled at the clock edges, thus at \( 2\nu_0 \). The quantity \( J^2 \) can be identified with the variance \( \langle x^2(t) \rangle \), yet after filtering out the \( f < f_L \) part.

For our purposes, \( J \) is approximately equivalent to the \textit{rms jitter}. By contrast, the general term ‘jitter’ has wider scope, mostly oriented to SDH telecomm systems. It includes different types of noise and interferences starting at 10 Hz, with different weight for each (the term ‘wander’ is preferred below 10 Hz). See for example [19] [20] [10] for standards and useful digressions. In a FPGA, there may be a factor 1000 between the rms jitter and the overall jitter, also including interferences.
3 Noise in the Clock Distribution

A lot about phase and time fluctuations can be learned from the simple model sketched in Fig. 1. The input signal of frequency $\nu_0$ is first converted into a square wave with full voltage swing, full slew rate and full bandwidth, and then distributed. Restricting our attention to white and flicker, we get the four behaviors listed in Table 1 and discussed below.

3.1 Spectrum of the Phase-Type ($\varphi$-type) Phase Noise

In digital circuits we often encounter the aliased $\varphi$-type noise. Let us start with $\varphi$-type noise at the input of a digital circuit, where the input signal $v(t)$ crosses a threshold affected by a fluctuation $n(t)$. Under the assumption that the input Slew Rate (SR) is high enough to avoid multiple bouncing (Sec. 6),
we get \( x(t) = n(t)/\text{SR} \) and, after (1),
\[
\varphi(t) = \frac{2\pi \nu_0}{\text{SR}} n(t). \tag{6}
\]

Notice that the direct measurement of \( n(t) \) is possible only in simple circuits which allow the simultaneous access to input and output of the gate.

The sinusoid is the preferred clock waveform because it propagates through circuit boards with best impedance matching and lowest crosstalk and radiation, and because high purity reference oscillators work in sinusoidal regime. Discarding the dc component and setting the threshold at 0, the clock signal
\[
v(t) = V_0 \cos(2\pi \nu_0 t) \tag{7}
\]
has slew rate \( \text{SR}_v = 2\pi \nu_0 V_0 \). In this conditions, the phase fluctuation is
\[
\varphi(t) = \frac{n(t)}{V_0} \tag{8}
\]

Generally, the analog bandwidth \( B \) of a digital circuit is greater than the \( \max \nu_0 \) by a factor of 3–4. This is necessary for the device to switch correctly. In turn, the bandwidth of \( n(t) \) is equal to \( B \). Squaring the input signal samples \( n(t) \) at the zero crossings introduces aliasing. The spectrum of the sampled signal is
\[
S_{n,s}(f) = \frac{B}{\nu_0} h_0 + \ldots \tag{9}
\]
where the \( 1/f \) and higher terms are neglected because of the comparatively noise power. A trivial way to prove (9) is to calculate the variance \( \langle n^2(t) \rangle = h_0 B \) (Parseval theorem) before sampling, and to state that it is equal to the variance \( \sigma^2 = S_{n,s}(f) \nu_0 \) of the sampled signal. Accordingly, the phase noise is
\[
b_0 = \frac{h_0 B}{\nu_0 V_0^2} \tag{10} \quad \text{(white, aliased } \varphi\text{-type)}
\]
\[
k_0 = \frac{h_0 B}{4\pi^2 \nu_0^3 V_0^2} \tag{11} \quad \text{(same, after } (2))
\]

Oppositely, aliasing has negligible effect on flicker \( h_{-1}/f \) and on higher terms \( (1/f^2, 1/f^3 \text{ etc.}) \). It follows from (8) that
\[
b_{-1} = \frac{h_{-1}}{V_0^2}, \quad C \text{ vs. } \nu_0 \tag{12} \quad \text{(flicker, pure } \varphi\text{-type)}
\]
\[
k_{-1} = \frac{h_{-1}}{4\pi^2 \nu_0^2 V_0^2} \quad \text{(same, after } (2)) \tag{13}
\]

Figure 2 shows the spectral properties of the \( \varphi\)-type noise. Aliasing scales the white noise as \( 1/\nu_0 \), but it has no effect on flicker. The corner frequency \( f_c \) which separates white from flicker regions is obtained equating (10) to (12)
\[
f_c = \frac{\nu_0}{B} \frac{h_{-1}}{h_0} \quad \text{(corner, } \varphi\text{-type noise)} \tag{14}
\]
3.2 Spectrum of the Time Type (x-type) Phase Noise

The x-type noise originates after the input comparator, where the clock signal has full SR and bandwidth. Though threshold fluctuations are always present, the voltage-to-time conversion has little effect, and the gate is characterized by its delay fluctuations. So, each gate of the clock distribution contributes to the delay, and the fluctuations add up statistically. At a closer sight, the device may be organized hierarchically, for example in gates and cells, likely with a longer propagation time between cells. Nonetheless, the fluctuation is proportional to the length and to the complexity of the distribution chain.

The pure x-type noise is found in the $1/f$ region and below, not affected by aliasing. The noise spectrum is described by

$$k_{-1} = C \text{ vs. } \nu_0 \quad \text{(flicker, pure x-type)} \quad (15)$$

$$b_{-1} = 4\pi^2 \nu_0^2 k_{-1} \quad \text{(same, after (2))}, \quad (16)$$

where $k_{-1}$ is the technical parameter which results from the clock distribution.

The aliased x-type results from sampling the fluctuation at the frequency $2\nu_0$, which affects the white noise region. The spectral parameter $k_0$ is found in

Figure 2: Spectra originated by the phase type ($\varphi$-type) phase noise.
3.3 Interpretation of Phase Noise Spectra

A series of spectra $S_{\phi}(f)$ taken with several values of $\nu_0$ helps to understand the interplay of noise types. Scaling $\nu_0$ in powers of two seems appropriate.

Let us start with flicker, $S_{\phi}(f) = b_{-1}/f$. Comparing (12) to (16), we expect that the noise is of the $\phi$-type at low $\nu_0$, and of the $x$-type at high $\nu_0$, with a corner frequency

$$\nu_c = \frac{1}{2\pi V_0} \sqrt{\frac{h_{-1}}{k_{-1}}} \quad (\text{flicker}).$$

The spectral properties of the $x$-type noise — i.e., (15)–(18) — are summarized in Fig. 3. The corner frequency which divides the flicker from the white region is calculated by equating (15) to (17)

$$f_c = \frac{\nu_0 k_{-1}}{J^2} \quad (\text{corner, } x\text{-type noise}).$$

Figure 3: Spectra originated by the time type (x-type) phase noise.
This is shown in Fig. 4A. Far from $\nu_c$, we can evaluate

$$h_{-1} = V_0^2 b_{-1} \quad (\nu_0 \ll \nu_c) \quad (21)$$

$$k_{-1} = \frac{b_{-1}}{4\pi^2 \nu_0^2} \quad (\nu_0 \gg \nu_c). \quad (22)$$

The white phase noise $S_{\varphi}(f) = b_0$ is described by (10) at low $\nu_0$, and by (18) at high $\nu_0$, separated by the cutoff

$$\nu_c = \frac{\sqrt{B h_0}}{2\pi V_0 J} \quad (white). \quad (23)$$

This is shown on Fig. 4B. At low $\nu_0$, (10) enables to calculate the noise power $\langle n^2(t) \rangle = h_0 B$ of the input threshold

$$h_0 B = V_0^2 b_0 \nu_0 \quad (\nu_0 \ll \nu_c). \quad (24)$$

Assuming that $B$ is equal to 3–4 times the maximum $\nu_0$, we can infer $h_0$ and the noise voltage $\epsilon_n = \sqrt{h_0}$. Conversely, at high $\nu_0$ we can extract the fluctuation

$$J = \frac{1}{2\pi} \sqrt{\frac{B_0}{\nu_0}} \quad (\nu_0 \gg \nu_c). \quad (25)$$

This can be compared to the rms jitter, if available in the specs.
4 Selected Noise Measurements

We measured the phase noise of several devices routinely used in our labs. This is a necessary step, before considering an unbound search for the best. Accordingly, the measurement method (Fig. 5) is more about flexibility than about sensitivity. Anyway, the phase noise of digital components is generally higher than that of common low noise components (i.e., amplifiers and mixers). On the other hand, we need simple operation in a wide range of frequency, with signals that may not be at the same frequency as the reference. For us, this is the relevant feature of the Microsemi 5125 (1–400 MHz) and 5120 (1–30 MHz) instruments. These instruments make use of correlation and average on the spectra of two nominally equal channels which measure the same quantity, which rejects the single channel noise \[22, 23\]. Notice that the oscillator is common mode, with very small differential delay, hence its noise is highly rejected. The Fourier frequency spans from 1 mHz to 1 MHz.

4.1 Cyclone III (65 nm)

In a first experiment, we measure a Cyclone III \[24\] in a clock buffer configuration. The input sinusoidal clock \( V_0 = 1 \text{ V}_{\text{peak}} (+10 \text{ dBm on } 50 \Omega) \) is squared and distributed as in Fig. 1A. The spectrum is shown in Fig. 6.

We first look at the white noise region. Our model suggests aliased \( \varphi \)-type noise \[10\] at low \( \nu_0 \), and aliased \( x \)-type noise \[18\] beyond the cutoff given by \[23\], as shown on Fig. 4B. Starting from \( \nu_0 = 3.125 \text{ MHz} \), \( b_0 \) scales down as \(-3.5 \text{ dB per factor-of-two} \), in fairly good agreement with the 3 dB predicted by the model. This results from the data fit shown on Fig. 6 top-right. Taking \( V_0 = 1 \text{ V} \), \[10\] gives a threshold fluctuation \( \sqrt{b_0 B} = 550 \pm 65 \mu\text{V} \). The ‘\( \pm 65 \mu\text{V} \)’ results from \( b_0 \propto 1/\nu_0^{1.16} \) instead of the \( 1/\nu_0 \) law. Assuming \( B = 2.5 \text{ GHz} \) (analog bandwidth, four times the maximum toggling frequency), we get \( \sqrt{b_0} = 11 \pm 1.3 \text{ nV/}\sqrt{\text{Hz}} \). This is in agreement with general experience, which suggests that general high-speed electronics has a typical noise level of 10–15 nV/\( \sqrt{\text{Hz}} \).

At \( \nu_0 \geq 100 \text{ MHz} \), the white noise falls outside the 1 MHz span. Since this occultation occurs before the aliased \( x \)-type noise shows up, we have no direct
access to $k_0$. On Fig. 6 at the maximum $f$ (1 MHz) and at 400 MHz carrier, the white noise is below $-138 \, \text{dBrad}^2/\text{Hz}$ (upper bound). This value, integrated over $B = 400$ MHz and converted into time, gives 1 ps, which is an upper bound for $J$.

Flicker noise is in good agreement with pattern of Fig. 4B only at $\nu_0 \geq 100$ MHz. From this part of the plot, we calculate $\sqrt{k_{-1}} = 21 \, \text{fs}$. By contrast, at $\nu_0 \leq 50$ MHz $b_{-1}$ scales as $\approx 1.5 \, \text{dB per factor-of-two}$ instead of being constant. This discrepancy is not understood. However, the $1/f$ region is rather irregular, and corrupted by bumps, even more pronounced at low $\nu_0$.

The lowest flicker found on Fig. 6 ($-115 \, \text{dBrad}^2/\text{Hz}$ at 3.125 MHz carrier), converted into voltage using (12), gives $\sqrt{h_{-1}} = 2.6 \, \mu\text{V}$ (upper bound for the input voltage flicker). Interestingly, this value is similar to the flicker of some CMOS high-speed operational amplifiers (for instance, 1.9 $\mu\text{V}$ for the Texas Instruments OPA354A).

Figure 7 shows the phase noise of the output buffer. The white noise is too
Figure 7: Phase noise of the Cyclone III, measured by comparing two outputs. Take away 3 dB for the noise of one buffer.

low to be visible with the 1 MHz span, masked by flicker and by some bumps at $10^4 \ldots 10^6$ Hz. By contrast, the flicker noise is in perfect agreement with the 6 dB per factor-of-two model (pure $x$-type noise). Comparing Fig. 7 to Fig 6, at $\nu_0 = 400$ MHz the flicker of the complete clock distribution is close to that of the output buffer. So, the contribution of the output buffer is not negligible. Conversely, at lower $\nu_0$ a significantly larger flicker rises in the clock distribution chain.

4.2 Measuring the Time Type ($x$-Type) Noise with the $\Lambda$ Divider

After some tests, we realized that the $\Lambda$ frequency divider \cite{25} is a good tool to measure the $x$-type noise of the clock distribution. First, a frequency divider is useful in that the input time fluctuation ($\varphi$-type noise, \cite{13}) is kept low by using a high input frequency, while the measurement at the lower output frequency is
simpler (both instruments are suitable, and the background is lower). Second, the \( \Lambda \) divider circumvents the aliasing phenomenon. In fact, a \( \Lambda \) divider \( \div D \) provides a triangle-like output waveform by combining \( D \) phases of a square wave, which is equivalent to sampling at the input frequency.

Figure 8 shows the phase noise of some devices used as \( \div 10 \) dividers in \( \Lambda \) configuration, with 100 MHz input and 10 MHz output frequency. The flicker coefficient is clearly identified, not corrupted by artifacts. The bump at 20 kHz (Zynq and Cyclone III) is due to the insufficiently filtered power supply. Finally, the \( \Lambda \) divider implemented with the Max 3000 deserves mentioning for its low noise (\( b_{-1} = -130.5 \text{ dBBrad} \) and \( b_0 = -165 \text{ dBrad}^2/\text{Hz} \)). This is lower than regular dividers (general experience), and just 10 dB above the NIST regenerative dividers [26] at the same output frequency.

5 The Volume Law

The idea that the phase noise coefficient \( b_{-1} \) is proportional to \( 1/V \), where \( V \) is the active volume, has been around for a while. In quartz resonators, this appears either directly or as a side effect of the larger size at lower frequency [27, 28, 29, 30, 31, 32]. In ultrastable Fabry-Perot cavities, flicker is powered by thermal noise and proportional to the reciprocal of the length [33, 34] which is approximately equivalent to \( 1/V \) after mechanical design rules.
The $1/V$ law results from a gedankenexperiment in which we combine $m$ equal and independent devices, giving $b_{-1,\text{total}} = b_{-1,\text{dev}}/m$. This has been confirmed experimentally with amplifiers [35, Chapter 2], [21]. Flicker is of microscopic origin because the probability density function is Gaussian, which originates from a large statistically-independent population through the central limit theorem. So, the $m$ devices can be combined in a factor-of-$m$ larger device exhibiting a factor-of-$1/m$ lower flicker. Similarly, we expect higher flicker if the size of the device is scaled down, until space correlation appears. The limit for small volume is not known.

In digital electronics, the volume $V$ of the active region is proportional to the node size $S$. For reference, $S$ is of 10 $\mu$m in Intel 4004 (1971), and of 16 nm in the Apple A10 Fusion chip of the iPhone 7. While the footprint surface is proportional to $S^2$, the two scaling rules are common in the literature on VLSI systems, known as constant-voltage and Dennard [16, P. 253], [36], agree in the depth proportional to $S$. Thus, $V \propto S^3$. The wire delay may contain $\sqrt{S}$, however, the flicker associated to wires is too small to deserve attention [37].

We measured a few components using the $\div 10$ $\Lambda$ divider configuration. This gives access to the $1/f$ noise of the clock distribution, which is of the $x$-type. We used 100 $\rightarrow$ 10 MHz, or 30 $\rightarrow$ 3 MHz with the Cyclone and the Cyclone II for practical reasons, sharing a 5125A and a 5120A. The results are shown in Fig. 9, which compares the $1/f$ PM noise to $S$.

The MAX V is not accounted for in the analysis because the spectrum was taken in unfavorable conditions, yet kept for completeness. A linear regression gives $k_{-1} = -26.2 \log_{10}(S) - 219.5$ dBs$^2$, with $S$ in nm. Fitting the same data with the exact volume law gives $k_{-1} = -30 \log_{10}(S) - 212.1$ dB$\text{rad}^2$/Hz. The

![Figure 9: Flicker coefficient $b_{-1}$ of digital devices, related to the cell size $S$.](image)

| Technology, nm | $1/f$ phase time coefficient $k_{-1}$, dBs$^2$ |
|---------------|---------------------------------------------|
| 28 nm         | 282 ± 89                                    |
| 130 nm        | 28.2 ± 8.9                                  |
| 180 nm        | 15.8 ± 5.0                                  |
| 300 nm        | 5.0                                         |
−26.2 dB/dec slope is reasonably close to the $1/V$ law ($−30$ dB/dec), with a number of measurement and accuracy insufficient to assess a discrepancy.

6 Input Chatter

Chatter is a fast random switching of a comparator, which occurs in the presence of wideband noise when the mean square slew rate of noise exceeds that of the signal at the threshold, i.e., $\langle \text{SR}_n^2 \rangle > \text{SR}_v^2$. The phenomenon is shown in Fig. 10 and 11.

Following the Rice’s approach [38, 39], noise in the small interval $[f, f + \Delta f]$ can be represented as the sinusoidal signal $n_f(t) = V_f \cos(2\pi f t + \theta_f)$, which has random amplitude $V_f$, random phase $\theta_f$, and slew rate

$$\text{SR}_{n,f} = 2\pi f V_f \sin(\theta_f).$$

The Parseval theorem requires that $\langle n_f^2(t) \rangle = S_n(f) \Delta f$, thus

$$\langle V_f^2 \rangle = 2S_n(f) \Delta f$$

because $\langle \cos^2(\ldots) \rangle = 1/2$ in $n_f(t)$. The mean square slew rate is calculated combining (26) and (27), integrating on frequency, and averaging on $\theta_f$. Since $\langle \sin^2(\theta_f) \rangle = 1/2$,

$$\langle \text{SR}_n^2 \rangle = 4\pi^2 \int_0^\infty f^2 S_n(f) \, df.$$  

In turn, $\langle \text{SR}_n^2 \rangle$ is determined by white noise $S_n(f) = h_0$, $f = [0, B]$. Other noise types are negligible because they occur at low frequency, compared to $B$,
and because of the $f^2$ term in (28). Thus

$$\langle SR^n \rangle = \frac{4\pi^2}{3}h_0 B^3.$$  

(29)

Since the clock signal (7) has slew rate $SR_v = 2\pi\nu_0 V_0$, the chatter threshold is

$$\nu_0 V_0 = \sqrt{\frac{1}{3}}h_0 B^3 \quad \text{(chatter threshold).}$$  

(30)

Taking the Cyclone III parameters (Sec. 4.1, $B = 2.5$ GHz and $e_n = 11$ nV/√Hz, thus $h_0 = 1.21 \times 10^{-16} V^2/Hz$), and $\nu_0 = 4.7$ MHz, (30) suggests a threshold $V_0 = 169$ mV. On Fig. 11, we see that chattering occurs at $V_0 = 100$ mV, and at $V_0 = 50$ mV the transitions are broken. Given the difficulty of identifying the parameters, the agreement between model and observation is satisfactory.

After (30), chattering is more likely at low carrier frequency. However, Fig. 11 shows that this can occur at 5 MHz, a standard frequency of great interest for high stability signals.

7 Internal PLL

The internal PLL is intended to provide high frequency internal clock stabilized to an external reference, often 5-10-100 MHz. We show simple experiments which give insight in the Cyclone III.
The PLLs is shown in Fig.[12]. The VCO operates in the 0.6–1.3 GHz range, extended to 300–650 MHz by the optional ÷2 divider, always present in our tests. A classical phase-frequency detector (PFD) is present, with charge pump output driving the analog feedback to the VCO. The PLL output frequency is $\nu_0 = \frac{N}{C+D} \nu_i$. This leaves three degrees of freedom ($N$, $C$ and $D$), two of which are available to the designer. The programming tool (Quartus) uses one to ensure that internal design rules are satisfied.

The VCO relies on a LC resonator on chip. General literature suggests a quality factor $Q$ of 5–10, limited by the technology [40]. Therefore, we expect a Leeson frequency $f_L = \nu_{\text{VCO}}/2Q$ of the order of 50 MHz.

In a first experiment (Fig.[13]), we use the PLL as a ‘cleanup’ ($\nu_0 = \nu_i$), yet with a high purity input. This gives the noise of the PLL, at different values of $\nu_i$. For lowest noise, we use the phase comparator at the highest possible frequency ($\nu_i$) by setting $D = 1$. The VCO frequency ends up to be 400, 600 or 640 MHz, depending on $\nu_0$. On Fig.[13] the white noise floor is not seen. This is sound because noise can be white only beyond $f_L$, which is beyond the 1 MHz span. Flicker is of the $\phi$-type at 5 and 10 MHz, with $b_{-1} = 2.5 \times 10^{-10}$ rad$^2$/Hz ($-96$ dB). Since this type of noise is not scaled down by the ÷$N$ divider in the loop, we ascribe it to the phase detector. This is because (i) with the tight lock implemented we do not expect to see the VCO; and (ii) the input comparator and the output stage of the ÷$N$ divider have some 10 dB lower noise in similar conditions ($-115$ dBrad$^2$/Hz, Section 4.1).

In the second experiment, we use the PLL as a frequency multiplier in powers of two ($\nu_0 = 2^n \nu_i$) from 10 MHz to 640 MHz, with $\nu_i = 10$ MHz. Again, we use $D = 1$ for lowest noise. The VCO delivers 320, 400 or 640 MHz, depending on $\nu_0$. The phase noise spectrum (Fig.[14]) indicates that flicker is of the $x$-type, scaling up as $\nu_0^2$. This indicates that the phase detector is the dominant source of noise, with negligible contribution of the dividers. So, the time fluctuation $x(t)$ is transferred from the phase detector to the VCO, and then from the VCO to the output. The phase $\varphi(t)$ scales accordingly, that is, $\times N/C$. 

Figure 12: Cyclone III internal PLL frequency multiplier.
Figure 13: The internal PLL is used as a buffer, that is, $\nu_o = \nu_i$.

8 Thermal Effects

8.1 Thermal Transients

Common sense suggests that delay is affected by the junction temperature $T_J$, while other parameters like $T_C$ and $T_A$ (case and ambient temperature) are comparatively smaller importance.

Our method consists in using the electrical power $P$ to heat the chip, and calculate $T_J$ from the thermal resistance $\Theta_{JA}$ and the transients. In turn, $P$ is chiefly set by the charge/discharge cycle of the gate capacitance, whose energy is $E = CV^2$. Thus, $N$ gates switching at $\nu_0$ dissipate $P = NCV^2\nu_0$. Of course, $P$ can be changed instantaneously. The delay is measured with a Symmetricom 5125A test set used as a phase meter and also as a time-interval counter.

We measured a Cyclone III used as a clock buffer (actually, 10 buffers connected in parallel through $330 \, \Omega$ resistors). The temperature had to be low-pass filtered by covering the card with a small piece of tissue. The results are shown in Fig. 15.

In the main body, all the curves show an exponential behavior plus a linear drift

$$x(t) = k'\Delta T (1 - e^{-t/\tilde{\tau}}) + k''t,$$

where $\Delta T = T_J - T_A$ results from setting $\nu_0$ in powers of two, and $\tilde{\tau}$ is the time constant. For reference, we observed $P = 1 \, \text{W}$ at 400 MHz, which means
Figure 14: The internal PLL is used as a frequency multiplier in powers-of-two of multiples of the 10 MHz frequency reference.

\[ \Delta T \approx 10 \text{ K} \text{ with } \Theta_{JA} \approx 10 \text{ K/W} \text{ (including the thermal pad on the pcb), and neglecting the dissipation at } \nu_0 = 0. \]

The linear drift (1 fs/s, or \(10^{-15}\) fractional frequency) does not scale with power. This behavior is typical of the environment temperature, slowly drifting during the measurement (a fraction of a Kelvin over 1 hour). Extrapolating the drift to \( t = 0 \), we get the asymptotic effect of the \( \Delta P \) transient alone.

The time constant \( \tilde{\tau} \) is found as the intercept of the tangent at \( t = 0 \) and the linear drift (dashed lines). This graphical process removes the drift. The value \( \tilde{\tau} = 400 \text{ s} \) is the same for all the transients.

The inset of Fig. 15 shows the delay versus the carrier frequency (dissipated power). As expected, the delay is proportional to \( T_J \), set through \( \nu_0 \). Accounting for \( P \) and \( \Theta_{JA} \), the thermal coefficient of the delay is 10 ps/K.

### 8.2 Allan Deviation

Generally, \( \sigma_y(\tau) \) should follow the \(1/\tau\) law (white and \(1/f\) phase noise). Other types of instability, as frequency noise would reveal a phase noise steeper than \(1/f\), and the delay of the device would diverge in the long run. However, bumps may be present. Notice that \(1/f\) phase noise in practice never yields large integrated delay.

Figure 16 shows the Cyclone III Allan deviation \( \sigma_y(\tau) \), measured with a Symmetricom 5125A test set.
We first discuss the $1/\tau$ region of Fig.16A. At low $\nu_0$, $\sigma_y(\tau)$ decreases proportionally to $1/\nu_0$. For $\tau = 1$ s, we read $\sigma_y = 10^{-12}$ at 3.125 MHz, $5 \times 10^{-13}$ at 6.25 MHz, etc. At higher $\nu_0$ the curves get closer to one another, and overlap at $\nu_0 \geq 100$ MHz.

Taking the classical conversion formulae for Allan variance and spectra (for example, [11], P. 77–80, or [17]), the $1/\nu_0$ behavior is equivalent to $h_1 \propto 1/\nu_0^2$ (frequency fluctuation spectrum $S_y(f) = h_1 f$), thus to $b_{-1} = C$ vs. $\nu_0$. This is the signature of the pure $\varphi$-type noise, as expected at low $\nu_0$ and at low $f$, thus at long $\tau$. We recall that the fluctuation of the input threshold is dominant at low $\nu_0$, and that the low $f$ region is dominated by the $1/f$ phase noise, virtually unaffected by aliasing.

By contrast, the $\sigma_y(\tau) = C$ vs. $\nu_0$ behavior is equivalent to $h_1 = C$ vs. $\nu_0^2$, thus $b_{-1} \sim \nu_0^2$. This is the typical of the pure $\kappa$-type noise, as expected at high $\nu_0$ and at low $f$, thus at long $\tau$. The fluctuation of the input threshold is no longer relevant, and the low $f$ region is still dominated by the $1/f$ phase noise, virtually unaffected by aliasing.

In summary, the $1/\tau$ region of the $\sigma_y(\tau)$ plot is consistent with the predictions of Section 2.

On the right hand of Fig.16A, $\sigma_y(\tau)$ seems to leave the $1/\tau$ law. This can only be a local phenomenon, i.e. a bump. Carrying on the experiment,
Cyclone III clock buffer

Bump due to the residual temperature of the previous run
No significant bump if the measurement is delayed by 1 H after switching

Figure 16: Allan deviation $\sigma_\gamma(\tau)$ derived from the FPGA delay.

in Fig. 16 A the measurement of $\sigma_\gamma(\tau)$ restarts immediately after switching $\nu_0$, while in Fig. 16 B the measurement of $\sigma_\gamma(\tau)$ is delayed by 1 hour after switching $\nu_0$. The relevant difference is that in A each curve suffers from the cooling-down transient of the previous measurement, while in B each measurement starts in steady state. Bumps show up in A at $\tau \geq 30$ s, and they get stronger at higher $\nu_0$, where the thermal dissipation is stronger, and almost disappear in B. This is a qualitative confirmation of the presence of two separate time constants (end of Sec. 8.1).

8.3 Side Effects of the Thermal Dissipation

We have shown that the electrical activity inside the FPGA heats the chip, and in turn affects the delay. Variations exceeding 50 ps have been observed in the presence of a light burden. The analysis gives a warning, thermal crosstalk is around the corner when the same FPGA is in charge of more than one task, made worse by the heat latency. Attempts to fit low noise and high-stability functions (frequency dividers, etc.) in a chip processing at high rate may be difficult or give unpredictable results.
Acknowledgments

This work is a part of the “Programme d’Investissement d’Avenir” projects in progress in Besançon, i.e., Oscillator IMP, First-TF, and Refimeve+. Funds come from the ANR, the Region Franche Comté, INRIM, and EMRP Project IND 55 Mclocks.

We thank the Go Digital Working Group for general help and fruitful discussion, and among them chiefly Jean-Michel Friedt, Pierre-Yves “PYB” Bourgeois, and Gwenhain “Gwen” Goavec-Mérout.

References

[1] M. I. Skolnik, Introduction to Radar Systems, 3rd ed. New York, NY, USA: McGraw Hill, 2001.

[2] M. I. Skolnik, Ed., Radar Handbook, 3rd ed. New York, NY, USA: McGraw Hill, 2008.

[3] G. Krieger and M. Younis, “Impact of oscillator noise in bistatic and multistatic SAR,” Geosci. Remote Sens. Lett., vol. 3, no. 3, pp. 424–428, Jul. 2006.

[4] D. Esman, V. Ataie, B. P.-P. Kuo, N. Alic, and S. Radic, “Subnoise signal detection and communication,” J. Lightwave Technol., vol. 34, no. 22, pp. 5214–5219, Nov. 15, 2016.

[5] F. Riehle, Ed., Proc. 8th Frequency Standards and Metrology Symp. Potsdam, Germany: IOP, Oct. 12–16, 2015, published as vol. 723, 2016 of Journal of Physics: Conference Series.

[6] J. Serrano, P. Alvarez, M. Lipinski, and T. Wlostowski, “Accelerator timing system overview,” in Proc. Particle Accelerator Conf. (PAC’11), New York, NY, USA, Mar. 28 – Apr. 1, 2011.

[7] S. Jablonski, H. Schlarb, and C. Sydlo, “CW laser based phase reference distribution for particle accelerators,” in Proc. Int’l Beam Instrumentation Conf. (IBIC2015), Melbourne, Australia, Sep. 13–17, 2015.

[8] D. Phillips, “Random noise in digital gates and dividers,” in Proc. Int’l Freq. Control Symp., Philadelphia, PA, USA, 1987, pp. 507–511.

[9] W. F. Egan, “Modeling phase noise in frequency dividers,” IEEE Trans. Ultrus, Ferroelec. Freq. Contr., vol. 37, no. 4, pp. 307–315, Jul. 1990.

[10] V. S. Reinhardt, “A review of time jitter and digital systems,” in Proc. Int’l Freq. Control Symp., 2005, pp. 38–45.

[11] S. Bregni, Synchronization of Digital Telecommunications Networks. Chichester, UK: Wiley, 2002.
[12] M. Kihara, “Performance aspects of reference clock distribution for evolving digital networks,” *IEEE Communications Mag.*, vol. 27, no. 4, pp. 24–34, Apr. 1989.

[13] C. Mack, “The multiple lives of Moore’s law,” *IEEE Spectrum*, pp. 29–35, Apr. 2015.

[14] A. B. Huang, “Moore’s law is dying (and that could be good),” *IEEE Spectrum*, pp. 41–44, Apr. 2015.

[15] “Moore’s law 50 years,” a series of articles and editorials on IEEE Spectrum, Apr. 2015 pp. 27–44.

[16] N. H. E. Weste and D. M. Harris, *CMOS VLSI Design, A Circuits and Systems Perspective*, 4th ed. Boston, MA, USA: Addison Wesley, 2011.

[17] E. S. Ferre-Pikal, *IEEE Standard Definitions of Physical Quantities for Fundamental Frequency and Time Metrology–Random Instabilities (IEEE Standard 1139-2008)*, IEEE, New York, Feb. 2009.

[18] CCIR Study Group VII, “Characterization of frequency and phase noise, Report no. 580-3,” in *Standard Frequencies and Time Signals*, ser. Recommendations and Reports of the CCIR. Geneva, Switzerland: International Telecommunication Union (ITU), 1990, vol. VII (annex), pp. 160–171.

[19] The control of Jitter and Wander Within the Optical Transport Network (OTDN), ITU, Sep. 2010, recommendation ITU-T G.8251.

[20] M. P. Li, *Jitter, Noise, and Signal Integrity at High-Speed*. Boston, MA, USA: Prentice Hall, 2008.

[21] R. Boudot and E. Rubiola, “Phase noise in RF and microwave amplifiers,” *IEEE Trans. Ultras. Ferroelec. Freq. Contr.*, vol. 59, no. 12, pp. 2613–2624, Dec. 2012.

[22] E. Rubiola and F. Vernotte, “The cross-spectrum experimental method,” arXiv:1004.5539 [physics.ins-det], Apr. 2010.

[23] S. R. Stein, “The allan variance—challenges and opportunities.” *IEEE Trans. Ultras. Ferroelec. Freq. Contr.*, vol. 57, no. 3, pp. 540–547, Mar. 2010.

[24] *Cyclone III*, Altera, type EP3C25E144C8N, speed grade 8, 24624 logic elements, 144-pin Enhanced Quad Flat Package, commercial temperature range.

[25] C. E. Calosso and E. Rubiola, “The sampling theorem in Π and Λ digital frequency dividers,” in *Proc. Europ. Freq. Time Forum and Freq. Control Symp. Joint Meeting*, Prague, Czech Republic, Jul. 21–25, 2013, pp. 960–962.
[26] A. Hati, C. W. Nelson, C. Barnes, D. Lirette, T. Fortier, F. Quinlan, J. A. DeSalvo, A. Ludlow, S. A. Diddams, and D. A. Howe, “State-of-the-art RF signal generation from optical frequency division,” IEEE Trans. Ultras. Ferroelec. Freq. Contr., vol. 60, no. 9, pp. 1796–1803, Sep. 2013.

[27] V. F. Kroupa, “The state of the art of flicker frequency noise in BAW and SAW quartz resonators,” IEEE Trans. Ultras. Ferroelec. Freq. Contr., vol. 35, no. 3, pp. 406–420, May 1998.

[28] ——, “Theory of 1/f noise—a new approach,” Phys. Lett. A, no. 336, pp. 126–132, Jan. 2005.

[29] A. van der Ziel, “Semiclassical derivation of handel’s expression for the hooge parameter,” J. Appl. Phys., vol. 63, no. 7, pp. 2456–2457, 1988.

[30] F. L. Walls, P. H. Handel, R. Besson, and J.-J. Gagnepain, “A new model of 1/f noise in baw quartz resonators,” in Proc. Int’l Freq. Control Symp., May 27-29 1992, pp. 327–333.

[31] M. M. Driscoll and W. P. Hanson, “Measured vs. volume model-predicted flicker-of-frequency instability in VHF quartz crystal resonators,” in Proc. Int’l Freq. Control Symp., Jun. 2-4 1993, pp. 186–192.

[32] F. Sthal, M. Devel, S. Ghosh, J. Imbaud, G. Cibiel, and R. Bourquin, “Volume dependence in handel’s model of quartz crystal resonator noise,” IEEE Trans. Ultras. Ferroelec. Freq. Contr., vol. 60, no. 9, pp. 1971–1977, Sep. 2013.

[33] P. R. Saulson, “Thermal noise in mechanical experiments,” Phys. Rev. D, vol. 42, no. 8, Oct. 15th, 1990.

[34] K. Numata, A. Kemery, and J. Camp, “Thermal-noise limit in the frequency stabilization of lasers with rigid cavities,” Phys. Rev. Lett., pp. 250602 1–4, Dec. 17, 2004.

[35] E. Rubiola, Phase Noise and Frequency Stability in Oscillators. Cambridge, UK: Cambridge University Press, Nov. 2008.

[36] R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous, and A. R. LeBlanc, “Design of ion-implanted mosfet’s with very small physical dimensions,” IEEE J. Solid-State Circuits, vol. 9, no. 5, pp. 256–268, Oct. 1974, also Proc. IEEE 87(4), Apr 1999.

[37] A. H. Verbruggen, H. Stoll, K. Heeck, and R. H. Koch, “A novel technique for measuring resistance fluctuations independently of background noise,” Acta Phys. Polonica A, vol. 48, pp. 233–236, Mar. 1989.

[38] S. O. Rice, “Mathematical analysis of random noise (Part I and II),” Bell System Technical Journal, vol. 23, no. 3, pp. 282–332, Jul. 1944.
[39] ——, “Mathematical analysis of random noise (Part III and IV),” *Bell System Technical Journal*, vol. 24, no. 1, pp. 46–156, Jan. 1945.

[40] A. Hajimiri and T. H. Lee, “Design issues in CMOS differential LC oscillators,” *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 717–724, May 1999.

[41] V. F. Kroupa, Ed., *Frequency Stability: Fundamentals and Measurement*. New York: IEEE Press, 1983.