SEMULATOR: Emulating the Dynamics of Crossbar Array-based Analog Neural System with Regression Neural Networks

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Abstract

As deep neural networks require tremendous amount of computation and memory, analog computing with emerging memory devices is a promising alternative to digital computing for edge devices. However, because of the increasing simulation time for analog computing system, it has not been explored. To overcome this issue, analytically approximated simulators are developed, but these models are inaccurate and narrow down the options for peripheral circuits for multiply-accumulate operation (MAC). In this sense, we propose a methodology, SEMULATOR (SiMULATOR by Emulating the analog computing block) which uses a deep neural network to emulate the behavior of crossbar-based analog computing system. With the proposed neural architecture, we experimentally and theoretically shows that it emulates a MAC unit for neural computation. In addition, the simulation time is incomparably reduced when it compared to the circuit simulators such as SPICE.

1 Introduction

For the application of neural networks on edge devices, analog computing using emerging memory devices with crossbar array architecture is promising in comparison with digital computing in the aspect of its plentiful representation capability with efficiency. This is because analog computing is based on the motivation that analog computation (e.g., peripheral circuit for accumulation) and memory unit (e.g., crossbar array, memory devices) have infinitely continuous states whereas digital computing has only a few states. Along with it, the time complexity of multiplication and accumulation in the crossbar array is $O(1)$. The nature of analog computing requires accurate circuit simulators such as SPICE, but it takes much time to simulate a cumbersome system like neural networks. Considering that research on deep learning enters golden age thanks to the development of GPU, the low-speed simulators for analog computing system is one of main factors that hinders research on this field.

To enhance simulation speed, approximated simulators, or analytical models, replace accurate circuit simulators. They simplify the computation and memory unit into an analytic function rather than dozens of non-analytic functions, enabling the analytic functions to be merged into high-level programming language and make use of machine learning frameworks which are run on GPU environment. However, they have three problems: Analytically modeled units result in overestimating the issues in analog computing [1,2] due to inaccurate modeling. On top of that, they require human experts to approximately model each unit into simple one, so that this methodology necessitates tremendous amount of human resources. If it is hard to approximate with an analytic function, then the units are modeled with multiple analytic functions with conditional statement such as a spline [3], which is reluctant in the GPU environment.

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In another way, statistical model [4] and neural networks [5] are used to emulate analog computation units or analog circuits. However, these works cannot deal with large input dimensions, while analog computing blocks which are consisted of hundreds of analog computation and memory units have thousands of input parameters. With digital computing system, a digital computing block such as logic gates is relatively smaller than that of analog, so that small fully connected neural network (FCNN) emulates their behavior with little error [6,7]. Instead of emulating the analog computing blocks, neural networks are used to find specific hyper-parameters of them or analog circuit system such as the arrangement of units or blocks [8], layout [9], and non-linear factor of crossbar arrays [2]. On these specific tasks, neural networks and deep learning find reasonable solutions, but there are little research on emulating an analog computing block to build a full analog neural system.

SEMULATOR proposes a methodology and neural network architecture for emulating the analog computing block. The neural network architecture for the purpose of emulating analog computing blocks includes feature extractors that fit with crossbar array architecture and circuit equation solver for extracted features of crossbar arrays (memory units) and circuit parameters of peripheral circuits (computing units). This architecture enables neural networks to emulate analog neural system, resolving the curse of dimension. In addition, while previous works only may use analog-digital-converters (ADCs) for analog computing, this architecture does not restrict the types of analog computing units. To verify the feasibility of our proposed neural architecture, we define the upper bound of error between SPICE simulation results and predicted values of neural networks, which gives conditions for training the neural networks such as required number of training data and epochs. Along with machine learning frameworks, as the architecture is trained on the frameworks, it can reduce simulation time astoundingly with little error compared to the result of SPICE.

2 Related Works

2.1 Simulator for Analog Neural Computing

To systematically design analog computing neural networks, research groups have suggested simulators by approximating memory device and peripheral circuits. According to the type of approaches to model crossbar array [1], analytical inference model [10, 11] depicts the model as matrix and its linear operation. Analytical training models support differential operation for backward path using deep learning frameworks [12]. Some of them includes non-idealities in memory devices, so that assumes more complicated models [13, 14]. However, because of the limitation of linearly-approximated analytical model, statistical model [2] use neural networks to find the ratio of non-linear to linear model.

2.2 Emulation by neural networks

In the aspect of circuit and device, statistical models [4, 3] are widely used to emulate them by regression. As deep neural networks (DNNs) have the ability to solve ordinary or partial differential equations [15, 9], DNNs are used as a model to emulate the circuit behavior which can be represented by differential equations [16, 5]. For the purpose of enhancing simulation speed, [6, 7] suggests to use simple neural networks for emulating logic gates, and then simulate a digital system with the neural networks. In another application of emulation, neural networks emulate the biological models [17].

3 SEMULATOR

3.1 Methodologies

SEMULATOR aims at emulating the response of circuits using crossbar array by neural networks. As shown in Figure [1], general circuit simulators builds circuit equations and find solutions by iterative algorithms such as Newton-Raphson method. However, due to exploding circuit parameters and computation, the simulators require much time and resources. To relieve this issue, analog computation and memory units are approximated by analytical models which are developed by human experts [10, 14]: Crossbar arrays of analog memory units are linearly approximated, and other memory units such as memory devices and computation units are non-linearly approximated. This methodology incorporates the approximated models into deep learning frameworks to pursue efficient simulations. However, this approach narrows down the choice for analog computation and memory...
3.2 Neural Network Architecture for SEMULATOR

The neural network to emulate the analog computation block is mainly composed of two parts: Crossbar array feature extractor and circuit equation solver. Figure 2 shows the schematic of our proposed architecture for SEMULATOR. The extracted hidden features and features of analog computing units which in general accumulates the current from analog memory units are concatenated. The concatenated features are interpreted as boundary conditions for circuit differential equations with respect to time domain, and so the circuit equation solver is expected to solve differential equations to find solutions of specific time slot. As neural networks have the ability to find solutions of specific partial or ordinary differential equations [15, 9], we use FCNN or Neural ODE [18] as circuit equation solvers.

In the crossbar array, the behavior of each cell is mainly determined by the features of the cell such as applied voltage to the cell and the conductance of memory device in the cell. Therefore, the behavior of the crossbar array, $C(X)$, is formulated as follows:

$$C(X) = C(d_{1,1}(x_{1,1}), ..., d_{r,c,t}(x_{r,c,t}))$$

(1)
Figure 3: The architecture of Conv4Xbar. In a feature map, a box with solid line indicates a output feature corresponding to a filter and a box with dotted line indicates a filter for the stage. Input feature maps has \(N\) depths which corresponds to the number of total tiles and \(C_0\) channels whose values are features of a cell in the crossbar array such as resistance, applied voltage, and so on.

\[
X = (x_{i,j,k}) \in \mathbb{R}^{f \times r \times c \times t}
\]

where \(X = (x_{i,j,k}) \in \mathbb{R}^{f \times r \times c \times t}\) is a tensor and \(x_{i,j,k} \in \mathbb{R}\). \(f, r, c,\) and \(t\) indicate the number of features in a cell, row, column, and tiles. According to the choice of a cell, the features of a cell are differed. For instance, 1R cell \([19]\) has two features, applied voltage to the cell and the conductance of the cell, and 1T1R cell \([19]\) has additional 1 transistor whose features such as threshold voltage and W/L ratio.

In most cases of the crossbar array, \(d_{i,j,k}(\cdot)\) has nearly same form, \(d(\cdot)\), because the structure of each cell is similar, which means that the function, \(d(\cdot)\), is shared along all cells along the row, column, and tile. As shown in Figure 3, the architecture of crossbar array has structural and physical similarity with the convolutional neural network (CNN). At the first layer, the unit size filters which has unit width and length isolate the features of the cell to emulate its behavior, \(d(\cdot)\). In the deeper layers, for instance, if the crossbar array is designed to accumulate currents along column, then the filters learn the column-wise locality. In addition, deeper layers allow networks to learn other non-linear behaviors in \(C(\cdot)\).

To guarantee these assumptions, we adopt 3D convolutional neural networks (3D-CNN) whose depth is 1 and the size of length or width increase through the deeper layer. We denote this type of neural networks as Conv4Xbar as shown in Figure 3. In the aspect of optimizing neural networks, it has advantages along with the structural similarity. The filters are trained scanning through all cells in the tiles, which leads to make the filters more generalized. The generalization power of this architecture stems from the belief that incorporating the prior knowledge improves generalization \([20]\). In addition, the filters help neural networks not to suffer from the curse of dimension because the filters are shared for all tiles of input feature maps or activation maps.

4 Emulating analog computing block

4.1 statistical verification

As analog computing has continuous states, the emulated neural networks are not free of error though it is believed small enough. This is because the error can be amplified in deep neural networks as it propagates through deeper layer. \([21]\) addresses error amplification effect of adversarial attacks. To mitigate the effect, the neural networks should be trained under the upper bound of error. In this sense, it is necessary to evaluate training neural networks by observing training or validation. Theorem 4.1 gives the upper bound of the error by directly observing the mean-squared-error (MSE) loss, where the upper bound of loss is represented by the significant bit of error, \(s\), and the probability, \(p\), of the condition that the error is less than half of significant bit. It is also possible to directly evaluate the condition, \(P_{(X,Y)\sim D}\{|Y - f(X)| < 0.5 \cdot 10^{-s}\} > p\), but if target neural networks has multiple outputs, it is controversial to evaluate them respectively.
Table 1: Experimental results of analog computing blocks. Inputs have four axes, each of whom corresponds to (hardware parameters, tile, row address, column address). Outputs spread from voltage, current, and so on, which is the output of analog computing blocks. MAE indicates the mean-average-error between SPICE results and predicted values.

| Computing Blocks | Inputs (C,D,H,W) | Outputs (O) | Data (N) | MAE       |
|------------------|-----------------|-------------|----------|-----------|
| RRAM+PS32 [22]   | (2,4,64,2)      | 1 voltage   | 50,000   | 0.981(mV) |
| RRAM+PS32 [22]   | (2,2,64,8)      | 4 voltage   | 50,000   | 0.955(mV) |

Figure 4: Train and test loss of RRAM32+PS32 case. Learning rate is halved at 1000, 1500, and 1800 epochs.

Theorem 4.1. Let $f$ be a regression neural network and $D$ is the distribution of training data. To satisfy the condition, $P_{(X,Y) \sim D}(|Y - f(X)| < 0.5 \cdot 10^{-s}) > p$, the upper bound of mean-squared error $E_{(X,Y) \sim D}(|Y - f(X)|^2)$ is $\left(\frac{1}{2} \cdot \frac{10^{-s}}{erf^{-1}(p)}\right)$ for the given $s$ and $p$.

Proof. Let the error, $Z = Y - f(X)$. By Lemma 4.2 $Z \sim N(0, \sigma^2)$. Then, we have

$$P_Z(|Z| < 10^{-s}) = P_Z(Z < 10^{-s}) - P_Z(Z < -10^{-s}) = \Phi\left(\frac{10^{-s}}{\sigma}\right) - \Phi\left(-\frac{10^{-s}}{\sigma}\right)$$

$$= \frac{1}{2} \left(1 + erf\left(\frac{10^{-s}}{\sqrt{2}\sigma}\right)\right) - \frac{1}{2} \left(1 + erf\left(-\frac{10^{-s}}{\sqrt{2}\sigma}\right)\right) = erf\left(\frac{10^{-s}}{\sqrt{2}\sigma}\right) > p$$

, where $\Phi(x) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{x} e^{-\frac{t^2}{2}} dt = \frac{1}{2} \left(1 + erf\left(\frac{x}{\sqrt{2}}\right)\right)$. As we know that $\mathbb{E}_Z(|Z|^2) = \sigma^2$, we can find the upper bound of $E_{(X,Y) \sim D}(|Y - f(X)|^2)$ to be $\frac{1}{2} \left(\frac{10^{-s}}{erf^{-1}(p)}\right)^2$.

Lemma 4.2. If a neural network $f$ is trained for regression data $D$ with the mean squared error, then the error $Y - f(X)$ = $Z \sim N(0, \sigma^2)$.

4.2 generalization

Table 1 shows the experimental results for various analog computing blocks with SEMULATOR. We use SPYCE [23] to generate data for SEMULATOR. RRAM+PS32 use 1T1R cell as analog memory units and customized analog circuit, PS32, for analog computing units. In this experiment, we assume 2 cases: 1 MAC unit for an analog computing block and 4 MAC units for an analog computing block. These cases differ from the hardware design choice. As shown in Figure 4, the train loss decreases with little gap between test loss, which means that the neural network is neither overfitted nor underfitted. Following Theorem 4.1, we set the significant bit of error, $s$, to be 3 and the probability, $p$, to be 0.3, so that the upper bound of loss is about $6.7 \cdot 10^{-6}$.

Along with loss, in a more generalized case, Figure 5 shows the outputs of trained neural networks of the case, RRAM+32 and 1 voltage output, when the parameters of a cell are changed and other parameters are randomly chosen: weight axis corresponds to the normalized conductance ($G$) and activation to the normalized applied voltage ($V$). Considering that the output voltage response ($\Delta V$)
Figure 5: For two normalized input parameters, voltage and conductance, the heatmap shows the output of RRAM+PS32. The two figures on the left are the results of the cell corresponding to a positive weight and right one to a negative weight.

The behavior of 1T1R cell is generally as followed,

$$\Delta O \approx G_{const}, \text{ if } V < V_{const}$$

$$\Delta O \approx \frac{1}{2}k(V - V_{const})^\alpha, \text{ otherwise}$$

the neural network properly generalizes the behavior of the non-linear cell. As we discussed before in Section 3.1, approximated models use the non-analytical functions, which leads to inaccurate model.

5 Conclusion

As neural networks have the ability to solve differential equations and emulate their behavior, we propose SEMULATOR which includes a methodology and neural architecture for crossbar array-based analog computing system to enhance simulation speed and accurate simulation. Therefore, it may adopt various types of peripheral circuits, and allow researcher not to simulate whole system on the classical circuit simulators where simulating cumbersome system is impossible. In addition, we suggest an upper bound of loss where the significant bit is specified.

Data Requirements and Loss

Figure 6 shows that as the number of data increases train loss decreases. It indicates that tens thousands of data are required to reduce the error and avoid underfitting. Considering that generating data requires additional resources such as licences for circuit simulators and CPU server, it is promising to suggest an algorithm to reduce the number of required data.

Figure 6: The relationship between the number of data and train loss

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## A The neural network architectures for SEMULATOR.

Table 2: The neural network architectures for SEMULATOR. The format is as follows: `Conv3d(in_channels, out_channels, kernel_size=(D,H,W), stride_size=(D,H,W), padding=(0,0,0)), Linear(in_features, out_features)`, where D,H, and W stands for depth, height, and width.

| Computing Blocks | Neural Network Architecture |
|------------------|-----------------------------|
| RRAM+PS32        | `Conv3d(2,16,(1,1,1),(1,1,1))`-CELU-`Conv3d(16,8,(1,2,1),(1,2,1))`-CELU-`Conv3d(8,4,(1,4,1),(1,4,1))`-CELU-`Conv3d(4,32,(1,8,1),(1,8,1))`-CELU-`Conv3d(32,32,(1,1,2),(1,1,1))`-CELU-`Linear(128,32)`-CELU-`Linear(32,16)`-CELU-`Linear(16,1)` |
| RRAM+PS32        | `Conv3d(2,16,(1,1,1),(1,1,1))`-CELU-`Conv3d(16,8,(1,2,1),(1,2,1))`-CELU-`Conv3d(8,4,(1,4,1),(1,4,1))`-CELU-`Conv3d(4,32,(1,8,1),(1,8,1))`-CELU-`Conv3d(32,32,(1,1,2),(1,1,1))`-CELU-`Linear(256,32)`-CELU-`Linear(32,16)`-CELU-`Linear(16,1)` |
A The additional experimental results.

Figure 7: The error distribution of test data for Table 1.