CJFET Differential Pairs Constructions and Characteristics for Design of CBiCJFet Differential Amplifiers and Differential Difference Amplifiers

Savchenko E. M.1,2,3, Drozdov D. G.1,3, Rodin V. G.1,3, Grushin A. I.1, Dukanov P. A.1, Prokopenko N. N.4,5

1JSC “SPE “Pulsar”, 2JSC “GZ “Pulsar”, Moscow, Russian Federation
3MIREA - Russian Technological University, Russian Federation
4Don State Technical University; 5Institute for Design Problems in Microelectronics of RAS, Russian Federation

E-mail: prorokov1949@gmail.com

We have developed technology and construction solutions system to increase differential pairs (DP) of JFet with p- and n-channels identity, which are included into silicon complementary bipolar process of SPE “Pulsar” (Moscow). The possibility of creating several types of JFet DPs within the process is shown. The paper presents the results of experimental studies of two types of DP JFet designs with p- and n-channels for the spread of gate-source voltage $\Delta V_{GS}$ depending on the drain current and drain-source voltage.

The main features of the first design of p-channel JFets were the following: formation of drain/source area due to passive base of npn-transistor and deep collector areas for pnp-transistor; channel formation based on p-layer collector of pnp-transistor; formation of bottom gate using $p^+$ buried layer; top gate formation due to active base and polysilicon emitter of npn-transistor. A feature of the second JFet design was top gate formation due to passive base. The designs of the first and second types of n-channel Jfet were formed similarly, taking into account the replacement of the applied areas of bipolar transistors with opposite ones in the type of conductivity.

It was found that with increasing drain current $\Delta I_D$ decreases, and with increasing drain-source voltage $\Delta V_{GS}$ at high currents increases for DP based on p-channel JFet with the first type of design. The maximum difference $\Delta V_{GS}$ was in the range of 5-80 mV for a given differential pair JFet with a p-channel. On plots for DP p-channel JFet with the second type design a significantly lowered voltage spread $\Delta V_{GS}$ was shown: for example, for the drain current $I_D = 50 \mu A$ the voltage spread $\Delta V_{GS}$ did not exceed 10 mV. In this case the voltage spread $\Delta V_{GS}$ practically did not depend on drain-source voltage in contrast to differential pair of the first type.

The second type JFet n-channel differential pairs like for the DP p-channel JFet provided lower spread values in comparison with the first type design: $\Delta V_{GS}$ reached values of 5-20 mV. Moreover, for the design of the second type, a significantly weaker effect of the drain-source voltage on $\Delta V_{GS}$ was observed at high current densities. The developed designs of differential pairs based on p- and n-channel JFet are recommended for use in organizing the production of CBiCJFet analog circuits, including operations at low temperatures.

Key words: p-n junction field-effect transistors; differential pair; drain-gate characteristic; silicone complementary bipolar technology

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Introduction

An identity of JFet differential pair (DP) at similar source currents is an important parameter, which characterizes a quality of JFet construction and corresponding JFet process [1–9]. This DP’s property significantly influences zero-level of analog ICs, including operational [10–12] and instrumental [13] amplifiers, as well as errors of input low-noise [14–16], charge-sensitive [17, 18] and transimpedance [19] amplifiers, sources of reference current and voltage [20] and so on is a priority in the design of AM.

A process, developed by SPE “Pulsar” [21], allows to design analog ICs, containing JFets and HF complementary bipolar transistors. But bipolar active elements (especially p-n-p) have extremely low values of base current gain in cryogenic temperature range. So to build low-temperature and low noise sensor interfaces and input stage of corresponding special analog ICs it is appropriate to implement only on...
CJFet components. This limitation causes development problem for analog ICs' functional unit base CJFet, on base of which it is possible to develop different OA, continuously operating voltage stabilizers, current and voltage comparators, active ARC etc. Todays' level of CJFet's circuitry is very low and not developed. It causes a problem of CJFet analog OM circuitry, it is more complicated than the one for CMOS and BJ processes. Its reason is different static voltage polarity between source and gate of JFet in active mode (comparing with drain-source polarity). As a consequence the following is required firstly to design CJFet analog OM: special CJFet current mirrors (CM), which are not implemented per circuits traditional for CMOS and BJT, CJFet input differential stages, buffer amplifiers (BA) with source output, rail-to-rail CJFet BA, input stages of fast CJFet AM, intermediate folded cascode, static mode stabilizer circuit (reference current sources and potential offset circuit), operational amplifiers with increased gain, fast CJFet OA, micropower CJFet OA, differential difference amplifier, OTA amplifiers with controlled slope etc. Conceptually we need updated concept for developing wide class of analog CJFet ICs, which practically were not developed because of dominant impact of cheap technology for CMOS and BJ and small production of low temperature microelectronic devices. However modern necessities of space instrumentation, high energy physics, medicine, quantum computing systems, high speed railway transport etc. stimulate development of this scientific direction. The above circuitry tasks are of high priority.

The methods to increase identity of JFet DP are connected with JFet rational construction and its implementation technology [24]. It is known that CJFet process in BiCom3HV modification of Texas Instruments company [22, 23] allows developing new precision operational amplifiers OPA211 and OPA827 with JFet and BJT, which combine ultralow level of noise coefficient and low power consumption. The said amplifiers are characterized by enabling parameters. BiCom3HV process makes possible to provide next generation of analog electronic component base, it includes all best microelectronic achievements. But OPA211 and OPA827 operate at temperatures of -40°C and higher according to BiCom3HV process, which is provided by bipolar transistors application. It is not enough for several tasks.

The purpose of this article is to develop and describe process and construction solutions, which provide identity improvement for CJFet DP with p- and n-channels, integrated into silicon complementary bipolar technological process of SPE “Pulsar” (Moscow).

1. p-Channel JFet Differential Pairs made by SPE “Pulsar” and their Basic Characteristics

It is possible to develop several types of p-n-junction field-effect transistors (JFet) within silicon-based bipolar process. There is a topology of differential pair of n-channel JFets on Fig. 1. It includes the following sections: S-area — source, G-area — top gate, D-area — drain.

The parameters of the first construction of p-channel JFets (Type 1) are the following:

- development of drain/source area due to passive base of npn-transistor and deep collector areas for pnp-transistor, when a distance between drain/source areas are 4.2 μm;
- channel development based on p-layer collector of pnp-transistor;
- development of bottom gate using p+ buried layer;
- top gate development due to active base and polysilicon emitter of npn-transistor.

There are drain-gate characteristics of p-channel JFets differential pair at 5 V and 10 V of drain voltage. A dependence of drain-source voltage nonidentity ΔVGS from drain current is defined for the above construction of p-channel JFets (Fig. 3). The Fig. 3 shows that ΔVGS reduces when current increases, and ΔVGS increases at high currents, when drain-source voltage increases. A spread of voltages ΔVGS does not go below 80 mV in a drain current rage up to 50 μA.
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There are drain-gate characteristics of second type p-channel JFETs differential pair at 5 V and 10 V on drain.

There is a dependence of drain-source $\Delta V_{GS}$ voltage spread on drain current for this pair of transistors.

The Fig. 5 shows that the second type JFET differential pair has significantly smaller spread of voltages $\Delta V_{GS}$. For example, a voltage spread $\Delta V_{GS}$ does not exceed 10 $\mu$V for drain current $I_D = 50 \mu$A. In this case the voltage spread $\Delta V_{GS}$ practically does not depend on drain-source voltage in contrast to differential pair of the first type.
2 n-Channel JFet Differential Pairs made by SPE “Pulsar” and Their Basic Characteristics

There is a topology of n-channel Fets differential pair on Fig. 6. It includes the following sections: S-area - source, G-area — top gate, D-area — drain.

![Fig. 6. n-Channel JFets Differential Pair Topology](image)

We investigated two types of n-channel JFets similarly to p-channel JFets: Type 1 — top gate area based on active base of npn-transistors, Type 2 — top gate area is developed based on passive base of npn-transistors.

There are drain-gate characteristics of n-channel JFets at 5 V and 10 V on drain for differential pairs of the first and second types on Fig. 7 and 8 correspondently.

![Fig. 7. Dependence $I_D = f(U_{GS})$ at $U_{DS} = 5$ V (a) and 10 V (b) for n-Channel JFET Differential Pair (Type 1)](image)

A cut-off voltage is $U_{T0} \approx 3.2-1.7$ V for n-channel transistors in comparison with $U_{T0} \approx 5.5-4$ V for p-channel transistors. As a result there are smaller current of drain for n-channel JFet at similar area. Thus it is reasonable to compare these transistors at drain current of 10 μA, but not at 50 μA (as was done for p-channel transistors).

Dependence $\Delta V_{GS}$ on drain current (Fig. 9) for the first type n-channel transistor differential pair substantially similar to the difference of the first type p-channel JFet differential pair (Fig. 3). But there is significantly weaker influence of drain-source voltage for n-channel JFet at higher current density. $\Delta V_{GS}$ for drain current $I_D = 10$ mA does not exceed 30 mV.

![Fig. 8. Dependence $I_D = f(U_{GS})$ at $U_{DS} = 5$ V (a) and 10 V (b) for n-Channel JFET Differential Pair (Type 2)](image)

![Fig. 9. Dependence $\Delta V_{GS} = f(I_D)$ at $U_{DS} = 5$ V and 10 V n-Channel JFET Differential Pair (Type 1)](image)
The values of voltage spread \( \Delta V_{GS} \) are significantly lower; from 5 to 21 mV for the second type n-channel transistors (Fig. 10). \( \Delta V_{GS} \) is not higher than 8 mV at \( I_D = 10 \mu A \). Similar to p-channel transistors (Type 2) there is an optimum value of drain current at which there is a minimum of \( \Delta V_{GS} \). When the drain current increases any further, \( \Delta V_{GS} \) weakly depends on drain current value similarly to all considered types of differential pairs.

So it is defined, that to provide minimum values of spread \( \Delta V_{GS} \) for JFet differential pair, including considering low temperature influence, it is reasonable to use the second type of p-n junction complementary field-effect transistors construction.

**Conclusion**

We have developed constructions of p- and n-channel JFets, included into silicon complementary bipolar process of SPE “Pulsar”, which provide relatively high identity of drain-gate characteristics at their differential input (\( U_{DS} \leq 5 \pm 10 \text{ mV} \)) and possibility to develop CBiCFet integral circuits.

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**References**

[1] Goldberg R.T. and Jhabvala M.D. (1995) Fabrication and characterisation of low-noise cryogenic Si JFETs. *Proc. Symp. Low Temperature Electronics and High Temperature Superconductivity*, pp. 95-9.

[2] Lovetskii I. Y., Khanin K. T. and Stepaniak V. R. (2018) Radiation influence on electrical characteristics of complementary junction field-effect transistors exploited at low temperatures. *Materials Physics & Mechanics*, Vol. 39, No. 1., pp. 92-101. DOI: 10.18720/MPM.39.2018.15

[3] Chan K. K. et al. (2016) Junction field-effect transistor with raised source and drain regions formed by selective epitaxy. U.S. Patent No. 9236499.

[4] El-Kareh B. and Hutter L.N. (2020) Silicon Analog Components. DOI: 10.1007/978-3-030-15085-3

[5] Monshipouri M. and Abdil Y. (2015) Field emission current from a junction field-effect transistor. *Journal of Nanoparticle Research*, Vol. 17, Iss. 4. DOI: 10.1007/s11051-015-2974-9

[6] El-Kareh B. and Hutter L.N. (2020) Bipolar and Junction Field-Effect Transistors. Silicon Analog Components, pp. 151-219. DOI: 10.1007/978-3-030-15085-3_5

[7] Kwangy J., Grafi P., Azazoglu H., Flebbe M., Hub K., Nenhaus H. and Möller R. (2019) Temperature dependent electrical characteristics of a junction field effect transistor for cryogenic sub-attomicroampere charge detection. *AIP Advances*, Vol. 9, Iss. 2, pp. 025101. DOI: 10.1063/1.5077039

[8] Cayne E. J. Low gate current junction field effect transistor device architecture. U.S. Patent Application No. 2016/0293182.

[9] Driht V.K., Gupta R., Parvaw V., and Dubey S. (2019) Effect of Surface Induced Surface Potential (SISP) on Threshold Voltage of SOI Junction-Less Field Effect Transistor (JLFET). *Silicon*, DOI: 10.1007/s11664-019-00815-9

[10] Snoeij M. (2018) A 36V 4X8MHz JFET-Input Bipolar Operational Amplifier with 150uV Offset and Overload Supply Current Control. *ESSCIRC 2018*. IEEE 44th European Solid State Circuits Conference (ESSCIR). DOI: 10.1109/ESSCIR.2018.8494262

[11] LF351 Wide bandwidth single JFET operational amplifiers, Available at: <https://www.st.com/resource/en/datasheet/lf351.pdf>

[12] Semig P. and Claycomb T. (2018) Op amps with complementary-pair input stages: What are the design trade-offs?, *Analog Design Journal* (Q), pp. 1-7

[13] Yang T., Lu J., and Holleman J. (2013) A high input impedance low-noise instrumentation amplifier with JFET input. *IEEE 2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS)*. DOI: 10.1109/mwscas.2013.6674613

[14] Scandurra G., Canina G., Giusi G. and Cloti C. (2017) A differential-input, differential-output preamplifier topology for the design of ultra-low noise voltage amplifiers. *2017 International Conference on Noise and Fluctuations (ICNF)*. DOI: 10.1109/icnf.2017.7985947

[15] Giacomini G., Bosio L., Betta G.D., Mendicino R. and Ratti L. (2015) Integrated Source Follower for the Read-Out of Silicon Sensor Arrays. *IEEE Transactions on Nuclear Science*, Vol. 62, Iss. 5, pp. 2187-2193. DOI: 10.1109/TNS.2015.2475402

[16] Manfredi P., Re V. and Specieli V. (1998) Monolithic JFET preamplifier with nonresistive charge reset. *IEEE Transactions on Nuclear Science*, Vol. 45, Iss. 4, pp. 2257-2260. DOI: 10.1109/23.709654

[17] urlaut P., Penner V., Kirchhof C., Quandt E., Knochel R. and Hoff M. (2017) Noise of a JFET Charge Amplifier for Piezoelectric Sensors. *IEEE Sensors Journal*, Vol. 17, Iss. 22, pp. 7360-7371. DOI: 10.1109/JSEN.2017.2750000

[18] Capron S., Mengoci D., Aliaga R.J., Gadea A., Gonzalez V. and Pullia A. (2014) Design of an integrated low-noise, low-power charge sensitive preamplifier for γ and particle spectroscopy with solid state detectors. *2014 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*. DOI: 10.1109/nssmic.2014.7431043
Δвеличина шого типу встановлено, що зі зростанням струму стоку ΔVG, який зростає з інтенсивності струму стоку, для DP на основі p-к анальних JFET з конструкцією першого типу, розглядалися як за великих значеннях напруги сток-відток.

В цих умовах, при великих значеннях напруги сток-відток, ΔVG має максимальну вартість в межах 5 - 80 мВ. Для DP n-к анальних JFET з конструкцією другого типу, розглядалися як за великих значеннях напруги сток-відток.

Δвеличина сток-відток δVG на основі p-к анальних JFET з конструкцією першого типу, розглядалися як за великих значеннях напруги сток-відток.

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сток-исток \( \Delta V_{GS} \) при высоких токах возрастает. Для данной дифференциальной пары JFet с p-каналом максимальная разница \( DV_{GS} \) лежит в пределах 5 – 80 мВ. Для DP p-канальных JFet с конструкцией второго типа приведены графики, показывающие существенно меньшее значение разброса напряжений \( \Delta V_{GS} \): например, для значения тока стока \( I_D = 50 \) мкА разброс напряжений \( \Delta V_{GS} \) не превышает 10 мВ. При этом, в отличие от первого типа DP, разброс напряжения \( \Delta V_{GS} \) практически не зависит от напряжения сток-исток. Как и для DP p-канальных JFet, дифференциальные пары n-канальных JFet второго типа обеспечили меньше значения разброса в сравнении с конструкцией первого типа: \( \Delta V_{GS} \) достигает значений 5 – 20 мВ. Также для конструкции второго типа наблюдалось значительно более слабое влияние напряжения сток-исток на \( \Delta V_{GS} \) при высоких плотностях тока.

Разработанные конструкции дифференциальных пар на основе p- и n-канальных JFet рекомендуется использовать при организации производства CB\&CJFet аналоговых микросхем, в том числе для эксплуатации в условиях низких температур.

**Ключевые слова:** полевые транзисторы с управляемым р-п переходом; дифференциальные пары; стоко-затворная характеристика; кремниевая комплементарная биполярная технология