A CMOS Pulse-Shrinking Mechanism with Improved Resolution

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Abstract. A new CMOS time measurement mechanism based on pulse shrinking applicable to time-to-digital converters (TDCs) is presented to improve resolution. In previous mechanism, the resolution was determined by controlling size ratio between an inhomogeneous and homogeneous logic gates to achieve sub-gate resolution. By only adding an inhomogeneous gate with identical size on the previous mechanism, the proposed mechanism possesses not only a resolution improvement but also a better resolution fluctuation for process and temperature variations. The proposed work was implemented in a 0.35-µm CMOS process for performance evaluation. The results demonstrated that the proposed mechanism achieves a significant resolution improvement with better resolution insensitivity to the process and temperature variations.

Introduction

Accurate time interval measurement is the core block of many physical instruments [1]. The physical quantity is first converted to a time interval and then a time-to-digital converter (TDC) is used to convert the interval into a corresponding digital code. To ease the circuit integration for VLSI system, the TDC fabricated in a CMOS technology is the best choice. The sub-gate time resolution is always required for modern TDCs. In additional to an absolute gate delay with an advanced CMOS technology, the approaches such as parallel scaled delay elements, Vernier delay lines, and time amplification can achieve a sub-gate delay resolution at the expense of circuit complexity and area. With low cost and simple circuit operation, the pulse-shrinking method has the possibility of reaching sub-gate resolution but without requiring circuit complexity [2-6]. When a pulse with a finite time width undergoes a pulse-shrinking unit to cause difference between the rising and the falling propagation times, the pulse width is shrinked by a small amount (i.e., time resolution). A CMOS TDC with a linear voltage-controlled current-starved delay line was proposed to achieve a high resolution [2]. The delay cell controlled by a voltage bias was presented to perform time attenuation. However, the calibration must be done continuously so as to consume much power. Without the bias voltage, a dimension-controlled version with a cyclic pulse-shrinking delay line was presented to greatly enhance the linearity and save the power [3]. The resolution is controlled by size ratio of adjacently inhomogeneous and homogeneous logic gates. This pulse-shrinking mechanism is extremely simple to derive a small pulse-shrinking amount (i.e. high resolution). Several previous works applied it to reach sub-gate resolutions [4-6]. In this paper, an improved version with adding a simple gate is proposed to achieve better performance in resolution for time measurement.

Conventional Pulse-Shrinking Mechanism

As described, the pulse shrinking occurs because of the difference between the falling and the rising delays along the delay chain [2-6]. Without any bias adjustment, the pulse-shrinking mechanism with a dimension-controlled NOT gate was proposed to vary the size of the inhomogeneous (or pulse-shrinking) NOT gate to control the pulse-shrinking amount, as shown in Fig. 1. All NOT gates have the same dimension except for the \((i+1)\)th NOT gate, whose width is \(\beta\) times those of the others. To simplify the derivation of the pulse-shrinking mechanism, the input pulse
in is assumed to be stepwise at each stage for first-order approximation. When the pulse travels from the \(i\)th stage to the \((i+1)\)th stage, the falling time and the rising time can be obtained [7]:

\[
t_{PHI,i} = \frac{2C_{i+1}V_{DD}}{k_{i}(V_{DD} - V_{AN})} + \frac{C_{i}}{k_{i}(V_{DD} - V_{AN})} \ln \left( \frac{1.5V_{DD} - 2V_{AN}}{0.5V_{DD}} \right)
\]

(1)

\[
t_{PLH,i} = \frac{-2C_{i}V_{AN}}{k_{i}(V_{DD} + V_{AN})} + \frac{C_{i+1}}{k_{i}(V_{DD} + V_{AN})} \ln \left( \frac{1.5V_{DD} + 2V_{AN}}{0.5V_{DD}} \right)
\]

(2)

Figure 1. Original pulse-shrinking mechanism with a dimension-controlled NOT gate.

where \(k_{N_{i}}\) and \(k_{P_{i}}\) are the transconductance parameters of the \(i\)th NOT gate, and \(C_{i+1}\) is the effective input capacitance of the \((i+1)\)th NOT gate. Assume that \(-V_{thP} = V_{thN} = V_{th}\) for simplification, the pulse-shrinking amount from stage \(i\) to stage \((i+1)\) can be estimated as

\[
\Delta W_{i} = C_{i} \left( \frac{1}{k_{P_{i}}} - \frac{1}{k_{N_{i}}} \right) \times \phi \times \phi = \left[ \frac{2V_{th}}{(V_{DD} - V_{th})^2} + \frac{1}{(V_{DD} - V_{th})} \ln \left( \frac{1.5V_{DD} - 2V_{th}}{0.5V_{DD}} \right) \right]
\]

(3)

where \(\phi\) is a constant term with approximate layout independence. Similarly, the pulse-shrinking amount from stage \((i+1)\) to stage \((i+2)\) can be analyzed as

\[
\Delta W_{i+1} = -C_{i+1} \left( \frac{1}{k_{P_{i+1}}} - \frac{1}{k_{N_{i+1}}} \right) \times \phi
\]

(4)

As mentioned, because the channel width of the \((i+1)\)th NOT gate is \(\beta\) times those of the other NOT gates, thus \(k_{N_{i+1}} = \beta k_{N_{i}}, k_{P_{i+1}} = \beta k_{P_{i}}\) and \(C_{i+1} = \beta C_{i} = \beta C_{i+2}\) is derived. The total pulse-shrinking amount (\(\Delta W\)) from stage \(i\) to stage \((i+2)\) can be determined by Eq. 3 and Eq. 4:

\[
\Delta W = t_{in} - t_{out} = \Delta W_{i} + \Delta W_{i+1} = (\beta - \frac{1}{\beta})C_{i} \left( \frac{1}{k_{P_{i}}} - \frac{1}{k_{N_{i}}} \right) \times \phi
\]

(5)

For \(\beta = 1\), this means that all NOT gates have the same size and the \(\Delta W\) is zero. Otherwise, the input pulse will be shrunk or expanded for \(\beta > 1\) or \(\beta < 1\), respectively. Thus, by controlling the size ratio (\(\beta\)) between the inhomogeneous NOT gate and those homogeneous NOT gates, the \(\Delta W\) can be determined. With the realization of sub-gate resolution, the pulse-shrinking amount can be designed by controlling \(\beta\) to be slightly greater than 1. However, if \(\beta\) occurs the deviation because of process
variations, the pulse-shrinking function may change into an undesired pulse-stretching function, which causes circuit failure. Thus, a new mechanism based on the original mechanism is proposed in this paper to achieve a better performance.

Proposed Pulse-Shrinking Mechanism

The improved pulse-shrinking mechanism is shown in Fig. 2. Compared with the original mechanism shown in Fig. 1, another pulse-shrinking (inhomogeneous) NOT gate is inserted into the delay chain to form a new pulse-shrinking delay element composed of two inhomogeneous NOT gates. With such a simple modification on the original mechanism, it almost would not increase the circuit complexity and the cost. The operation principle is the same as that shown in Fig. 1. Thus, the total pulse-shrinking amount in this proposed mechanism can be estimated as:

\[
\Delta W = \Delta W_i + \Delta W_{i+1} + \Delta W_{i+2} + \Delta W_{i+3}
\]

\[
= \left[ C_{i+1} \left( \frac{1}{k_{p_i}} - \frac{1}{k_{s_i}} \right) - C_{i+2} \left( \frac{1}{k_{p_{i+1}}} - \frac{1}{k_{s_{i+1}}} \right) + C_{i+3} \left( \frac{1}{k_{p_{i+2}}} - \frac{1}{k_{s_{i+2}}} \right) - C_{i+4} \left( \frac{1}{k_{p_{i+3}}} - \frac{1}{k_{s_{i+3}}} \right) \right] \times \phi
\]

Now we have \( k_{N_{i+1}} = k_{N_{i+2}} = \beta k_{N_i} \), \( k_{p_{i+1}} = k_{p_{i+2}} = \beta k_{p_i} \), and \( C_{i+1} = C_{i+2} = \beta C_i = \beta C_{i+3} = \beta C_{i+4} \). Thus, the pulse-shrinking amount in the proposed technique can be written as:

\[
\Delta W = \left( \beta + \frac{1}{\beta} - 2 \right) C_i \left( \frac{1}{k_p} - \frac{1}{k_{W_i}} \right) \times \phi
\]

Eq. 7 is similar to Eq. 5 except for the difference between the multiplication factors (\( \beta - 1/\beta \)) and (\( \beta + 1/\beta - 2 \)). In this mechanism, regardless of \( \beta > 1 \) or \( \beta < 1 \), the pulse always shrinks expect for \( \Delta W = 0 \) (i.e., \( \beta = 1 \)). More importantly, the resolution improvement can be achieved in this mechanism by only adding a simple inhomogeneous gate with identical size.

Simulation Results

To demonstrate the performance of the proposed technique, the previous and the proposed mechanisms were integrated into the TDCs, as shown in Fig. 3. The TDCs were implemented in a 0.35-µm CMOS standard process for comparison. The improved cyclic delay line presented in [6] was used to eliminate undesired pulse-shrinking amount. Thus, the pulse-shrinking unit (PSU) implemented using the previous or the proposed mechanism can totally determine the resolution (i.e. \( \Delta W \)) to increase accuracy [6]. Fig. 4 shows the layout diagrams for the two TDCs with its mechanism.
The circuit areas of the two works are almost the same. By using HSPICE simulation, the simulated resolutions with different value of $\beta$ for the two mechanisms are shown in Fig. 5. Obviously, the proposed mechanism maintains pulse-shrinking function even $\beta$ becomes smaller than 1 because of process variation. Furthermore, this work achieves the resolution improvement considerably. For the dimension ratio of $\beta=3$, the resolution of 27 ps (TT mode) in the previous mechanism is improved to 18 ps (TT mode) in this mechanism, and equivalently 33 % improvement in resolution is achieved. Moreover, the resolution fluctuation for process and temperature variations are reduced from $\pm 13 \%$ to $\pm 7 \%$ and from $\pm 18 \%$ to $\pm 13 \%$ in the temperature range of 0~70 °C, respectively. These results demonstrated that this proposed mechanism achieves the significant improvements in resolution and the fluctuation without increasing the circuit complexity.
Conclusion

In this paper, an improved pulse-shrinking mechanism has been presented and demonstrated. Without increasing the circuit complexity, the resolution improvement can be achieved considerably by only adding an inhomogeneous logic gate on the previous mechanism. The analysis for the pulse-shrinking amount ($\Delta W$) was deduced to evaluate the performance and the simulation was performed to validate the proposed mechanism. The simulation results showed that this mechanism achieves 33% improvement in resolution and ±6% reduction in resolution fluctuation for process variation when compared with the previous mechanism. Table I list the performance comparison between the two works.

Table 1. Performance Comparison between the previous and proposed mechanism.

| TDC        | Resolution (ps) | Resolution Fluctuation (%) | Area (mm$^2$) | Technology (µm) |
|------------|-----------------|----------------------------|---------------|-----------------|
| Previous   | 27              | ±13                        | 0.03          | 0.35            |
| Proposed   | 18              | ±7                         | 0.03          | 0.35            |

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