Using DSP Slices as Content-Addressable Update Queues

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Abstract—Content-Addressable Memory (CAM) is a powerful abstraction for building memory caches, routing tables and hazard detection logic. Without a native CAM structure available on FPGA devices, their functionality must be emulated using the structural primitives at hand. Such an emulation causes significant overhead in the consumption of the underlying resources, typically general-purpose fabric and on-chip block RAM (BRAM). This often motivates mitigating trade-offs, such as the reduction of the associativity of memory caches. This paper describes a technique to implement the hazard resolution in a memory update queue that hides the off-chip memory readout latency of read-modify-write cycles while guaranteeing the delivery of the full memory bandwidth. The innovative use of DSP slices allows them to assume and combine the functions of (a) the tag and data storage, (b) the tag matching, and (c) the data update in this key-value storage scenario. The proposed approach provides designers with extra flexibility by adding this resource type as another option to implement CAM.

Index Terms—Content-Addressable Memory, CAM, DSP Slices

I. INTRODUCTION

Content-Addressable Memory (CAM) provides valuable functionality at the core of many practical use cases. CAMs allow to associate some data with a set of keys, aka. tags, coming from a considerably larger key space. They are found (a) at the heart of memory caches that buffer the contents of a small subset of memory addresses, (b) in the implementations of network routing tables which typically support ternary wildcard matching, and (c) in the hazard detection logic of command queues of long-latency off-chip memory controllers. Depending on the use case, the associated value may be (a) a data vector such as a cache line, (b) a scalar value as for identifying a forwarding interface, or (c) a simple flag as for indicating that a memory location is currently manipulated.

The implementation of CAM structures on FPGAs is challenging. It requires the efficient integration of both storage capabilities and vastly parallel key matching logic. While modern FPGAs comprise sizable designated on-chip memory in the form of block RAM (BRAM) or UltraRAM (URAM), these RAM abstractions encounter a bottleneck in the number of available memory ports and cannot facilitate the parallel comparison of their contents against a lookup key.

Another hardened special-purpose structure embedded into the fabric of virtually all modern FPGAs is the DSP block [1], [2]. It is best known for comprising a hard-wired word multiplier that can be used for scalar multiplication or put on an accumulation chain together with other DSP blocks to compute dot products.

Applications with little or no need for multipliers often let the DSP blocks of the device sit idle. However, even disregarding the multiplier, the DSP blocks provide interesting infrastructure involving wide datapaths, both internal to a block and cascaded to its neighbors, with an abundance of pipeline registers. Furthermore, simple arithmetic, such as addition and subtraction, bitwise logic operations, as well as word comparison are available independently of the multiplier. These capabilities are an interesting foundation for implementing an integrated key storage and matching logic and render DSP slices an attractive alternative to claiming vast amounts of fabric LUTs, registers, and general-purpose routing. Note that DSP blocks can be operated in a mode (USE_MULT="NONE") that deactivates the multiplier so as to eliminate the power overhead of the unused multiplier.

This paper reviews different techniques used to leverage various FPGA resource types for implementing CAMs. It then makes the case for using DSP slices as another point in the design space offering interesting resource trade-offs. In the rest of this paper, Sec. II gives an overview of the state of the art before Sec. III details the constraints and functional requirements of a use case serving as a running example. Our DSP-based solution is presented in Sec. IV and evaluated in Sec. V. Finally, Sec. VII concludes the paper.

II. RELATED WORK

FPGAs lack hardened CAM structures so that CAM functionality must be emulated. Since employing LUTs and registers is extremely hungry in terms of resources, RAM-based emulation has become a popular technique to implement CAMs. Using the key for an address-based lookup, however, quickly encounters scalability bounds. Zerbini and Finochietto [3] demonstrate that slicing the key into individual subwords allows to partition the lookup using separate but significantly smaller memories. Indeed, slicing the key into individual bits would match the structure of a native CAM that determines the match from an AND tree combining the match results of all key bits. This approach has been elaborated by Jiang [4] who formalizes the approach and adds an extensive experimental evaluation. Both of them consider a networking background and assume an implementation as TCAM that also supports ternary wildcard matches. The TCAM-nature of their emulators renders updates more expensive, requiring $O(2^w)$ RAM.
writes with \( w \) being the bit length of the longest key slice \( [4] \). This update time can, in fact, be reduced to \( O(1) \) when wildcard matching is not needed. In any case, the length of the key slices induces a memory space overhead factor of \( \frac{2}{5} \) over a native CAM \( [4] \). For the typical fabric memory resources, this implies a \( \frac{32}{5} \times 6.4 \times \) overhead for LUTRAM and a \( \frac{512}{5} \times 56.9 \times \) overhead for BRAM.

Large associative mappings require to leverage FPGA-attached off-chip memory, typically DRAM. Use cases include FPGA-accelerated network routing \( [5] \), particularly for IPv6, or key-value stores \( [6] \). While Bando et al. \( [5] \) and Blott et al. \( [6] \) use hashing to randomize storage, trie-based IP routing implementations have also been reported \( [7], [8] \). The practical challenges in these approaches are the hash collision management and the accumulating pointer chasing latency, respectively. Such large, or often even canonical mappings, with a rather high tolerance for lookup latency are not targeted by the solution offered in this paper.

Another use case frequently associated with CAMs is memory caching. As caching is a performance-enhancing technique that tolerates cache misses, its implementation can include more compromises and trade-offs. The critical tuning parameter is, in fact, associativity. Direct-mapped or set-associative implementations with a low associativity of two or four effectively reduces the tag lookup parallelism, thereby enabling a mapping to on-chip RAM resources. The focus of FPGA optimization efforts then moves to device-compatible replacement strategies \( [9], [10] \) and non-blocking implementations that are able to handle parallel outstanding misses \( [11], [12] \).

Hazard detection and prevention is used to guarantee the atomicity of spatially or temporally interleaved data write and read accesses. As long as blocking is tolerable, only the keys under pending updates must be identified safely. Since false positives are functionally tolerable in this set membership formulation, Bloom filters \( [13] \), in particular counting Bloom filters \( [14] \) that support set removal, are a very efficient implementation option. If updates are rare, even more primitive data structures such as sequentially iterated lists may offer a feasible solution as practiced in the key-value store Caribou \( [15] \).

III. USE CASE & CHALLENGE

Our reference use case is the online collection of event stream statistics. As shown in Fig. 1 events serve as the key that is mapped to an associated value, e.g., their occurrence count. A statistics update requires (a) the current value to be read, (b) the update to be applied and (c) the updated value to be written back. While off-chip memory is able to support a space of multi-million keys, the practical implementation of the required read-modify-write cycle must cope with the rather high read latency of this memory. In particular, updates may not be allowed to cause the loss of a previous one by issuing a stale read interleaved with an ongoing, not yet completed update cycle. Indeed, Bloom filters may be used to enforce the sequentialization of updates to the same key. However, this approach will cripple the utilized memory bandwidth and expose the complete memory read latency as event input period under key locality.

The key measure to maintain the event throughput is to conflate secondary updates to a reoccurring key with pending ones. Instead of issuing a read for starting a fresh memory update cycle, the outstanding write back will be manipulated to perform a cumulative update. The required state can be captured by an on-chip mapping associating keys within an update cycle with their scheduled transition function, such as an increment. This mapping must be able to support a subset of the key space whose size, at least, reflects the average read latency of a few 100 ns exposed by the underlying memory controller. Over-provisioning the mapping size helps to hide individual tail latencies as induced by bus turnarounds or memory refreshes. At practical application clock frequencies between 200 MHz and 400 MHz, this amounts to maintaining a few hundred outstanding key-update mappings with fully associative matching capabilities. The described use case comes with a few distinct properties that can be exploited by an implementation:

- The insertion order equals the deletion order as (a) an insertion reflects a read request issued for a key without an outstanding update and (b) its deletion represents the write back upon the reception of the corresponding reply.
- Write backs may be delayed beyond the reception of the current memory value as long as the update conflation is continued and the write back is performed eventually before using the statistics accumulated in memory.

The first property allows the mapping to be structured as a queue. The second one permits a static depth, which may be used for structural simplification.

IV. IMPLEMENTATION CONCEPT

The basic idea for the update conflation queue is illustrated in Fig. 2. A pipeline whose length is matched to the read latency of the off-chip memory carries tuples comprising keys (\( k \)) and the increment values (\( v \)). The pipeline never stalls unless forced so by backpressure from the memory controller. It may transport empty slots, which are identified by a deasserted valid flag, which is prepended to each key and
included in key matching. Empty slots arise (a) from cycles without an update input (strobe $s_0 = 0$) or (b) from updates that have been conflated with a pending one. An update conflation is triggered *locally*; when the parallel matching of the new key $k_0$ with all pending updates encounters a match, the outstanding increment value will subsume the new update $v_0$. If any match has been determined, this information will be fed back through the NOR gate. Only unmatched keys (a) effect a memory read for initiating a read-modify-write cycle and (b) create a valid key-value pair in the conflation queue. Once this pair has propagated through the entire queue, subsuming all updates to the same key during propagation, the memory reply will be available. The overall increment can be performed and written back to external memory.

While the conflation of updates for the same key may reduce the required memory bandwidth, an update stream of distinct keys without gaps will still emit two memory operations, a read and a write, for each clock cycle. As memories are optimized for throughput and expose multi-lane interfaces to a user design, this is not an obstacle per se. However, memory operations should be grouped by kind, i.e. read or write, to reduce bus turnaround overhead. It is critical in any reordering of commands to achieve such a grouping that a read never overtakes a write to the same address. A scheduling that strictly does not allow any reads to pass writes is a simple approach to satisfy this demand. Note that these considerations apply to any implementation regardless of how it chooses to manage read-modify-write cycles with pending memory reads.

The operations needed for the update conflation for each stage of Fig 4 are all available in a DSP slice. However, its completely combinatorial matching is impractical. Firstly, it would result in prohibitively long critical path delays and, hence, an unattractive clock frequency. More fundamentally, the computation must be re-arranged to match the structural composition of a DSP slice. Note particularly that the comparator result is registered along with the accumulated output $\mathbf{11}$. This register delay requires the addition merging two matching updates to occur one pipeline stage later.

The adjusted mapping to actual DSP slices is illustrated in Fig 3. Note that the indeces used in key-value pairs designate their age with index zero aligning with the output of the first DSP slice. The input pipelining within the DSP slice has the consequence that the two following inputs have already entered the slices. The shorter input path through the $C$ register is taken by the latest key for its distributed parallel matching. The match output then controls the merger of the corresponding increment value in the next DSP slice. For the proper alignment, this value is delayed by another input register on the $A:B$ path. Observe the different function of the MUX-controlled input path in the first DSP slice. It replaced any update that was matched by another valid queue entry by an empty slot marked by $\mathbf{11}$.

Again referring to Fig 3 note that the main pipeline path is entirely internal to the chain of DSP slices by using designated cascading busses for forwarding the output registers $P$. These wide, 48-bit busses are typically able to carry the whole payload comprising (a) the key extended by a valid bit and (b) the increment value. For a plain counting statistics, the value range is bounded by the requirements of merging increments, i.e. $\log_2(N)$ where $N$ is the depth of the pipeline. Thus, 9 or 10 bits suffice for a queue matching the memory read latency of a few hundred cycles. Discounting the extra flag added to identify empty pipeline slots, this leaves enough space to support a key space of $2^{17} > 10^{11}$, i.e. more than 100 billion.
The challenges, this DSP mapping leaves unsolved are (a) the fanout of the input pair and (b) the fanin for combining all the individual match results. As the input is latency-insensitive, duplicated input buffers can be used to limit the fanout of individual signals so as to maintain the needed clock speed. Such a trivial pipelining solution is not available for the feedback of the match signals as it forms a cycle involving the decision of admitting an active or an empty slot to the pipeline. A growing hierarchy of LUTs as required for fanin cones of more than six match inputs is prone to become the critical path of the design.

The overall match reduction can be pipelined by inserting an equivalent number of register stages both (a) in the feedback path and (b) on the key-value input path of the first DSP slice as shown by the green markers in Fig. 3. The delay added to the feedback path allows to pipeline the match aggregation as needed. The corresponding delay on the input path ensures that the invalidation of matched inputs is applied to the correct key-value pair. Note, however, that the key-value pairs within the input delay stages are not available for comparison with the following candidate. Unmitigated, this implies a functional hazard if the spacing between identical keys in the input stream is smaller than the number of input delay stages.

A possible measure to obtain the required spacing of input keys is a distancing in stages. A first short conflation queue without a pipelined match aggregation imposes no specific key-spacing requirements on its input. Having a depth of \( N \) comparator stages, it, however, guarantees that any key emitted at its output will be followed by \( N \) different keys or empty pipeline slots. Any matching key that occurred within this window in the input stream will have been merged with its preceding match. Limiting the depth \( N \) of the initial conflation queue, for example, to the fanin of a device’s LUTs ensures a short critical path while also providing the freedom to pipeline the subsequent conflation stage accordingly. Multiple stages may be chained to increase the spacing of identical keys step by step. Observe that the original task of identifying updates with unique keys to initiate and, finally, complete read-modify-write cycles is the sole responsibility of the last of these stages.

For a final operational note, observe that the described approach implements a *forward* conflation of updates with a common key. This choice guarantees important properties that an alternative *backward* conflation could not deliver. It guarantees (a) that updates are not starved by being repeatedly retracted to later ones with a matching key, (b) that accumulated conflated increments are bounded and (c) that the order of unique keys once committed to the conflation queue is maintained. Thus, the arithmetic datapath can be dimensioned precisely, and the association with memory replies occurs naturally by sequence.

V. EXPERIMENTAL CONFIGURATION

We employ the described update conflation to maintain an online occurrence histogram over the items of a continuous data stream in the off-chip RLDRAM memory \[16\] of a VCU118 prototyping board \[17\]. We distinguish \( 2^{24} > 16 \cdot 10^6 \) data buckets, i.e., keys. The counter maintained for each key comprises a master count and a shadow count. The shadow counts are targeted during non-disruptive, consistent snapshot readouts. They are merged into the master count once a snapshot operation completes. The designation of an event occurrence to either go directly to the master count or temporarily to the shadow count during snapshot readouts must be performed as long as their temporal order is intact, i.e., before the conflation queue performs mergers with outstanding increments. Therefore, two separate 10-bit counts constitute the value part of the conflation datapath. The total occupation of the 48-bit datapath amounts to \( 24 + 1 + 2 \cdot 10 \) bits for the key, the valid flag as well as the two count lanes, respectively.

Tab.\[4\] characterizes the implemented conflation schedule. It comprises two stages implementing the DSP mapping of Fig.\[3\] (a) an initial short conflation with a purely combinatorial match feedback, and (b) a deep conflation with 244 parallel matchers. The initial stage pre-processes the stream of updates to ensure that there is a minimum of 6 unrelated slots in between any two identical keys. This enables the introduction of six pipeline stages into the critical match feedback path of the following essential deep conflation.

Observe that the depths of cascaded conflation stages can increase quickly as the critical match reduction can leverage pipelined OR trees of logarithmic height. As the height of this tree grows, the challenging signal crossings out of and into the DSP slices are also more and more separated for an additional benefit to timing closure. As a consequence of the logarithmic growth of the tree height, no practically relevant implementation will demand more than three cascaded conflation stages.

The implementation of deep conflation stages needs to take measures to break the chain of DSP slices. On the FPGA device, the DSP slices are arranged in columns that also facilitate the designated direct cascade datapaths. The height of these columns is physically bounded. In the case of the super logic regions (SLRs) constituting the XCVU9P device of the VCU118 board, there are 120 DSP slices chained in a column. In fact, we break the pipeline into smaller segments, each comprising up to 42 comparators, to prevent the formation of a monolithic placement unit with an extreme aspect ratio. This way, pipeline segments can be placed on neighboring DSP columns to form a more compact, logically interleaved structure. To facilitate feasible routing between these segments, we unbalance the inter-segment match reduction to enable the

| Stage \( i \) | Gap in \( k_i \) | Matchers \( n_i \) | Gap out \( k_i + n_i \) |
|---|---|---|---|
| 0 | 0 | 6 | 6 |
| 1 | 6 | 244 | 250 |

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TABLE I: CHARACTERISTICS OF THE 0-6-250-CONFLATION SCHEDULE
displacement of pipelining fronts to the inter-segment links of the DSP pipeline.

As a reference, we evaluate providing the same functional capability through general-purpose fabric logic. In this scenario, the state of the conflation queue is maintained entirely in fabric registers and, thus, available for a fully unrolled, parallel key matching in fabric LUTs. A competitive clock speed is attained by implementing an analogously staged conflation scheme comprised of (a) a stage with a short combinatorial match feedback, and (b) a deep conflation stage. Thus, we essentially contrast the trade-off between different FPGA resource types.

All design evaluations have been conducted in the minimal application context depicted in Fig. 4. A trivial pseudo-random Event Source is monitored for occurrence statistics. The event stream is fed to the described two-stage update Conflation, which triggers the start and the completion of read-modify-write cycles. The RMW Scheduler takes the memory transaction requests into the slower memory user clock domain while also trying to group reads and writes up to (a) fill the four parallel memory command lanes and (b) to reduce bus turnaround overhead. It guarantees that reads do not surpass writes in this grouping process. The Arbiter allows to funnel in the administrative memory access for (a) the counter initialization and (b) the low-priority snapshot readout. A Xilinx Controller IP [13] implements the last layer before the four parallel command lanes and four doubled data lanes with a user clock of 133.25 MHz. For design synthesis and implementation, Vivado 2019.2 has been used with default flow settings.

VI. EVALUATION

The resource utilization obtained for the experimental setup under different sets of parameters is tabulated in Table II. It shows the consumption of the general-purpose fabric resources in terms of LUTs and FFs (registers) as well as DSP slices for both (a) our proposed conflation mapping and (b) the reference solely relying on fabric resources. All experiments have been conducted for four challenging application frequencies from 350 MHz to 390 MHz. Each result is given with its relevant structural context as stated by Vivado’s hierarchical utilization report. While the memory controller dominates the overall application, the update conflation is, indeed, the most costly part of the event tracker.

First, observe that both the LUT and the DSP slice utilization are largely independent from the choice of the target application frequency. The proposed DSP mapping is a clear trade-off investing DSP slices in exchange for freeing general-purpose LUTs. It is entirely carried by the implementation of the conflation queue freeing 5550 LUTs for an investment of 257 DSP slices, i.e., about 22 LUTs per DSP slice. Note that only 250 of these DSP slices perform the complete functionality within the conflation queue. The remaining seven facilitate internal segmentation of the deep second conflation stage and the final delayed addition at the end of each stage.

A similar resource trade-off is observed for the register utilization. The investment of 257 DSP slices frees more than 10,000 fabric registers, i.e. about 39 FFs per DSP slice. Observe that the register pay-off is higher for lower application frequencies. In contrast to the reference fabric design, the DSP mapping provokes some register duplication as the target frequency increases. This can be attributed to the more challenging input routing to the DSP computation as it produces a greater aspect ratio dictated by the physical columnar arrangement of DSP slices on the device. In addition to this automatic inflation of datapaths, going above 375 MHz also mandated limiting the re-use of the A:B inputs across cascading busses to only two adjacent DSP slices. Leveraging fewer routing capabilities internal to the DSP slices, returns more and more routing load to the fabric, thereby, diminishing one the benefits of moving into the DSP slices. Our results suggest that going beyond 400 MHz is not practical for the given VU9P device.

| Freq. [MHz] | LUTs | FFs | DSPs |
|------------|------|-----|------|
| 350 - Total | 13008 | 11096 | 21545 | 260 | 3 |
| 360 - Total | 13005 | 11137 | 21545 | 260 | 3 |
| 375 - Total | 13010 | 11218 | 21545 | 260 | 3 |
| 390* - Total | 13010 | 11300 | 21545 | 260 | 3 |

| Controller IP | Mapped Ref. | Mapped Ref. | Mapped Ref. |
|---------------|-------------|-------------|-------------|
| MemCtrl       | 11289       | 11289       | 11289       |
| Tracker       | 1280        | 1280        | 1280        |
| Confl.        | 562         | 562         | 562         |
| VU9P          | 11294       | 11294       | 11294       |

* A:B cascading of DSP mapping reduced to single re-use.
The RLD3 memory of the VCU118 board has a peak performance of 1066 MT/s. This performance is reduced by bank cycle times, bus turnarounds and refresh interference. Implementing an access schedule alternating between blocks of 16 reads and blocks of 16 writes with a perfect cycling through the 16 available banks reduces the achievable transaction rate to below 60% of the nominal peak value.

A conflating event tracker running at 375 MHz has a peak requirement of 750 MT/s as up to one read and one write operation can be emitted per cycle. This is a nominal utilization of 70% of the peak memory bandwidth. It will, thus, not constitute the limiting bottleneck of the statistics computation. In terms of operational performance, the fully-associative conflation with 250 comparators and processing events at 375 MHz amounts to 93.75 G comparisons per second.

The described conflation approach can be implemented feasibly both on the basis of the proposed DSP mapping and in the general-purpose fabric. The DSP mapping provides a valuable resource choice in application contexts that are otherwise dominated by fabric logic. Leveraging dormant DSP resources removes the pressure imposed by significant state, comparator logic and pipeline datapath routing from the fabric. In fact, the resource usage can be finely tuned to complement other demands by combining both implementation options. A hybrid approach combining a DSP chain with some parallel state in the fabric would also allow to extend the datapath with a fine granularity beyond the hardened 48-bit DSP accumulation bus.

Very similar DSP slice architectures as used here are available on virtually all contemporary devices offered by different vendors on the market. They share the critical feature of designated cascading datapaths that enable the implementation of an internal pipeline. These datapaths differ somewhat in bit width. Stratix IV devices by Intel provide 44 bits [19], their Stratix V devices already feature 64 bits [20]. However, neither of the Stratix DSP blocks provides an internal comparator so that the key must be fed from the DSP datapath into the fabric for the match computation.

Consider as an alternative, the implementation of the update conflation based on a CAM for the keys leveraging the CAM emulation approach by Jiang [4]. Having no need for wildcard matching, the update delay can, indeed, be reduced from $O(2^w)$ to $O(1)$. Using distributed LUTRAM with an individual address width of $w = 5$ results in the consumption of \[ \left\lceil \frac{244}{w} \right\rceil \cdot 24 = 1220 \] LUTs for the tag memory equating the deep second conflation stage. 244 LUTs are needed to complete the computation of the local key matches into a 244-bit match vector. In order to support both a key entry and a key deletion within each clock cycle, a second port must be emulated by memory duplication with an exclusive OR to form the true output from both LUTRAM sibblings. This results in nearly 3000 LUTs for the key storage and local matching. In contrast to the conflation pipeline, there is no propagation of key-value pairs but the storage is operated as a ring buffer. As the CAM organization supports fast key matching but not retrieval, an additional block RAM buffers the keys for their fast unqueuing and deletion. Another block RAM stores the associated increment values. These memories must be operated in dual-port mode so as to allow the parallel queuing and unqueuing or the conflation with an outstanding buffered increment. Adopting the initial preparative conflation stage of our proposal would enable the attractive pipelining of the needed memory updates. In terms of resources, this approach would invest two block RAMs for freeing about 3000 LUTs.

In summary, our results show that DSP slices offer a capable resource option for implementing the considered non-blocking hazard prevention. They provide a computational base that is able to perform vastly parallel key matching and on-the-fly mergers of matching updates across the off-chip memory read latency. The described DSP mapping enables designers to designate specifically the least constrained resource type of their application to the challenging maintenance of off-chip statistics over high-bandwidth data.

VII. Conclusions

This paper has described the FPGA implementation of a fully-associative key-value mapping with an additive update conflation that serves the hazard avoidance of a high-bandwidth off-chip statistics collection. It delivers the massively parallel matching of new entries against all pending keys of a high-latency read-modify-write cycle so as to match the memory bandwidth. The proposed conflation scheme has been shown to map well to the DSP slices of contemporary Xilinx devices. Concrete timing and utilization results have been reported, interpreted and evaluated for a conflation schedule suitable for collecting event occurrence statistics in the RLDRAM memories of the VCU118 prototyping board. They demonstrate that the recourse to DSP slices offers a very capable resource option freeing valuable general-purpose fabric resources for implementing a challenging non-blocking associative update mapping for the hazard prevention in the statistics collection in off-chip memories with a significant read latency.

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