ABSTRACT

Microarchitectural timing attacks are a type of information leakage attack, which exploit the time-shared microarchitectural components, such as caches, translation look-aside buffers (TLBs), branch prediction unit (BPU), and speculative execution, in modern processors to leak critical information from a victim process or thread. To mitigate such attacks, the mechanism for flushing the on-core state is extensively used by operating-system-level solutions, since core-level state is too expensive to partition. In these systems, the flushing operations are implemented in software (using cache maintenance instructions), which severely limit the efficiency of timing attack protection.

To bridge this gap, we propose specialized hardware support, a single-instruction multiple-flush (SIMF) mechanism to flush the core-level state, which consists of L1 caches, BPU, TLBs and register file. We demonstrate SIMF by implementing it as an ISA extension, i.e., FLUSHX instruction, in scalar in-order RISC-V processor. The resultant processor is prototyped on Xilinx ZCU102 FPGA and validated with state-of-art seL4 microkernel, Linux kernel in multi-core scenarios, and a cache timing attack. Our evaluation shows that SIMF significantly alleviates the overhead of flushing by more than a factor of two in execution time and reduces dynamic instruction count by orders-of-magnitude.

1. INTRODUCTION

One of the fundamental techniques to secure computer program execution is the confinement of programs to eliminate or minimize information leakage [25]. To improve computing performance, contemporary computer systems contain increasingly complex architectures and microarchitectures (shown in Figure 1), which allows for the time-sharing of hardware (much of the hardware is shared with multiple processes), faster memory references, reduced branch penalty etc. These architectural improvements provide unique opportunities for an adversary to orchestrate advanced information leakage attacks upon modern processing systems [9, 17].

Microarchitectural timing attack (MTA) is an information leakage attack which has been recently shown to be successful [8]. Example exploits include, Meltdown [27] and Spectre [24], which were mounted by taking advantage of branch prediction, speculative execution, and caches.

In such an attack, the adversary typically relies on the temporal interference of the persistent state in certain microarchitectural components (such as cache) of processors, to create timing variations (e.g., cache access time difference). Such timing variations, along with a priori knowledge of the victim system (software and hardware), can be used to infer the secret data in a time-shared system’s hardware [42].

In order to mitigate MTA, existing hardware-based techniques focus on redesigning the cache (which targets cache timing attack) as well as adding information flow tracking across a processor by drastically modifying the processor architecture, which must be created with a corresponding new hardware description language. Software-based techniques at hypervisor or OS level seek to maximally close the cache timing channels by cache partitioning (at shared caches), cache flushing (at private caches). To mitigate MTA system-wide (including all the possible timing channels in multiple microarchitectural states), software-based methods, such as temporal isolation (or, time protection) [13] propose the flushing of all on-core states, including private caches, translation look-aside buffers, branch prediction unit, etc.

Recent software-based methods [13, 31, 44] heavily rely on the flushing mechanism. While flushing or cleansing the
We also explored flushing the register file, which has been discussed in-depth in §3.3 and summarized as follows: 1) as shown in Figure 2 two numbers of instructions are used to create routines or functions for flushing each and every microarchitectural component of interest in sequence (sequence is enforced by inserting explicit barrier instructions in between the flushing instructions); and, 2) individual instructions used for flushing may not contain all necessary components, for example, x86 provides one instruction to flush the entire cache hierarchy but lacks a dedicated L1 cache flushing instruction or an instruction to flush the branch prediction unit. As elaborated in §2 and §3 (Figure 3), in our initial estimation, flushing at high frequency can incur more than 30% of additional dynamic instructions, which is equivalent to significant execution time and power overhead (instruction fetch power takes approximately 30% of CPU power [5]).

In this paper, we aim to create one individual specialized flushing instruction to raise the efficiency of temporal isolation at the core level for on-core state towards minimizing the existing and potential timing channels [14]. Based on this instruction, we also aim to explore the upper-bounds of the set of software-based MTA mitigations, which are constructed on top of the flushing mechanism, in terms of efficiency.

To this end, we first propose a single-instruction multiple-flushing (SIMF) scheme, which integrates flushing operations in a single instruction to clear the core-level state. The key advantage of SIMF is: 1) sharply reducing the dynamic instruction count (leading to cycle counts and instruction fetch power) dedicated to flushing; 2) minimal extension (adding one instruction to ISA) to the existing hardware; 3) implicitly enforcing the orders of flushing operations in one instruction, without using explicit barrier instructions; 4) programming benefits, including strong atomicity, which cannot be interrupted in the middle (for the case discussed in [44]) and simplicity.

For thoroughly investigating SIMF, we prototyped SIMF in an open-source scalar in-order RISC-V processor. We extended RISC-V ISA with one additional instruction called FLUSHX, which flushes the core-level state including L1/L2 TLBs, L1 caches, branch prediction unit (BTB, RAS, BHT). We also explored flushing the register file, which has been reported as a potential information leakage target [8]. Our evaluation shows that SIMF significantly alleviates the overhead of flushing by more than a factor of two in execution time and reduces dynamic instruction count by orders-of-magnitude.

The main contributions of this paper are as follows:

- An instruction extension, which can flush L1 caches, TLBs, BPU, and register file in one instruction execution;

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depends on the cache configuration of L1 D-cache in the system — the number of sets $n_{sets}$ and the number of ways $assoc$. Here, we assume the L1 D-cache has the following configuration: $n_{sets} = 64$ and $assoc = 8$.

Based on the above assumption, the total count of dynamic instructions for flushing operation in a program is approximated in the following way: 1) the dynamic instruction count and cycle count of normal program execution are obtained via FPGA emulation; 2) operating frequency, flushing frequency, and cycle count are used to calculate the number of flushing operations performed during the program execution; and, 3) the total dynamic instruction count of flushing is normalized to the total dynamic instruction count of normal program execution.

To briefly envision the scaling of the overhead, we consider two representative operating clock frequencies, 100 MHz and 1 GHz as well as one SPECint2006 workload, 458.sjeng. The flushing frequency is defined as $x = [100, 50000]$ Hz, considering the values that are potential and is adopted in practice [13, 44]. To contrast with the existing flushing mechanism, we also estimate the overhead with the optimal flushing mechanism in theory, which realizes the complete flushing operations in one instruction, for 458.sjeng. The optimal mechanism is denoted as “opt” (whereas “norm” denotes normal system) for the first element in the tuple in the legend of Figure 3.

### 2.2 Observation

Figure 3 provides two principal observations: First, the dynamic instruction count overhead can become substantial as flushing frequency increases. In the case of 100 MHz clock frequency, core-level flushing incurs about 10% overhead with 1 KHz flushing frequency and almost 100% overhead when approaching 10 KHz. For 1 GHz clock frequency, the same flushing frequency results in much fewer occurrences of flushing. Hence, the overhead is less prominent, however it reaches 10% at 10 KHz and approaching 100% at 50 KHz. Second, the optimal design of flushing mechanism can lead to a sharp decrease of orders-of-magnitude in dynamic instruction count overhead. Such a huge gap between “opt” and “norm” suggests significant promise in performance and power efficiency. Flushing operations are performed during context switches. Context switches usually lead to refilling the on-core state (e.g., caches), therefore, the cold state, caused by the flushing during context switches, in turn incurs minimal additional performance overhead [13].

The aforementioned observations and discussion strongly motivate the design of a special compound instruction to efficiently flush the core-level state residing in multiple components in processor architecture.

### 3. BACKGROUND

#### 3.1 Threat Model

The threat model in this study is defined below and is similar to the ones defined in existing advanced microarchitectural timing attacks [24] and research [13]: 1) the adversary Bob is assumed to have control of a user process, which shares the same processor core with the victim Alice’s process, in a contemporary preemptive operating system; 2) based on time-sharing mechanisms (e.g., preemption), Bob aims to manipulate the core-level state, such as L1 caches, to exploit the temporal dependence of the state (e.g., cache contention) between Bob and Alice’s time slice, hence rendering the timing channels; 3) Bob is capable of designing the point of time to invoke the preemption or inter-process interrupt (IPI), such as the attack discussed in [30], to carefully target a specific part of Alice’s execution; and, 4) the system is equipped with necessary temporal isolation mechanisms for protecting L2 caches and LLC, such as [13].

#### 3.2 Temporal Isolation

As shown in Figure 4, temporal isolation [7] prevents temporal interference, hence eliminates timing channels, by spatially or temporally partitioning the hardware resources. Existing OS-level temporal isolation methods generally use cache partitioning (page coloring) for shared large caches, such as L2 and last-level cache (LLC), which typically are indexed by the physical address. This way is also referred as spatial partitioning.

However, applying cache partitioning to core-level “private” resources, e.g., L1 caches and TLB, which are indexed by virtual address is difficult. For enforcing temporal isolation in these components, flushing is advocated to cleanse the state in these components [13]. By cleansing the state, there will be no residual state left by the victim for the attacker to create timing channels. This way is also called temporal partitioning.
The frequency of core-level state flushing is determined by the temporal isolation scheme. The seL4’s time protection [13] initiates flushing upon every security-domain switch, which is approximately once per 10-100 milliseconds. seL4’s domain is a group of threads, and hence, less frequent than the thread switch. The attack from the threads in the same domain is presumed to not happen. In other schemes, such as Düppel [44], flushing is performed as noise injection to prevent cache timing channel. Therefore, flushing is activated “at least 50 times per millisecond”.

### 3.3 Existing ISA Support for Flushing

In existing temporal-isolation systems [13], the implementation of the flushing mechanism is based on existing instructions, such as cache maintenance instructions, provided by the ISA. Table 1 shows how the flushing operations at core level can be implemented with ARM and x86 architectures.

| ISA       | L1DC | L1IC | TLB     | BP     |
|-----------|------|------|---------|--------|
| x86       | wbinvd | wbinvd | invpcid | indirect |
| ARM32     | dcssw | iciallu | tbianl | bpiall |
| ARM64     | dc cisw | ic iallu | tbiall | a/a |

The x86 ISA support for flushing: `clflush` invalidates and writes back (if dirty) the cacheline that contains the virtual address specified with the source operand for entire cache hierarchy (data and instruction). `clflush` is not privileged, and can be executed in user mode. `wbinvd` invalidates and writes back (if dirty) cachelines for entire cache hierarchy, `wbinvd` is privileged, and can only be executed in system mode. `invlpg` invalidates any TLB entries specified with the source operand. `invlpg` is privileged, and cannot be deployed in user programs. `invpcid` invalidates mappings in the TLBs and paging-structure caches based on register operand. x86 has no dedicated instruction to flush the state in branch prediction unit (BPU). To achieve BPU cleansing, the indirect branch control feature [21] must be adopted.

The ARM ISA support for flushing: `dc cisw` invalidates and writes back the specified individual data cacheline (in set/way format, instead of virtual address format) at the specified cache level for ARM64 (aarch64). `dc cisw` is one of ARM’s cache maintenance instructions. This instruction is privileged and hence must be executed in system mode. The equivalent instruction for ARM32 (aarch32) is `dcssw`. `ic iallu` invalidates entire L1 I-cache (to the point of unification, i.e., L2) for ARM64 (aarch64). This privileged instruction also invalidates BPU. The equivalent instruction for ARM32 is `iciallu`. `tbianl` (x ∈ {1, 2, 3}) invalidates all entries in TLB for the specified translate regime (i.e., EL1, EL2, EL3). This set of instructions are ARM64 system instructions, while the ARM32 equivalent is one instruction, `tbianl`. `bpi all` is an ARM32 system instruction, which invalidates all the entries in BPU. The ARM64 equivalent does not exist.

**RISC-V ISA support for flushing:** As an emerging ISA, RISC-V ISA is rapidly including new instructions. There are two privileged instructions for flushing:

1. `fence.i` for synchronizing the instruction and data streams, which essentially flushes the L1 I-cache; and
2. `sfence.vma` for flushing the TLBs.

### 4. SIMF MECHANISM

As shown in Figure 5, SIMF mechanism design includes:

1. hardware of flushing operations for each on-core state;
2. the control logic, which manages the issue order of the flushing operations; and,
3. the instruction deployment in software.

In this paper, for the sake of brevity, we consider an inorder scalar processor architecture as the base system, which does not include prefetech hardware. However, the implementation would not be too onerous for an out-of-order processor. The principles remain similar.

#### 4.1 Sphere of Flushing

Taking into account the study in [14], about microarchitectural timing channels, SIMF targets a comprehensive set of states on-core, which we define as the sphere of flushing (SoF). SoF includes all the on-core state, L1 D-Cache, L1 I-Cache, TLB and the BPU. L1 D-Cache is prone to timing channel [19]. Cache access time can vary substantially depending on whether the access is a hit or miss. An attacker can exploit the access time variation to mount timing channel attacks, for example, as shown using PRIME+PROBE [32, 34]. L1 I-Cache is similar to L1 D-cache, in terms of cache time access variation. The main difference is that L1 I-Cache timing attack relies on creating cache contention via carefully crafted control flow and seeks to leak the execution flow of the victim process (e.g., cryptographic algorithms) [1].

**TLB** timing channel can be constructed by exploiting the time variation of a virtual address translation between TLB hit and miss [15, 20] for control flow (instruction TLB) and data flow (data TLB). We assume a contemporary two-level TLB microarchitecture (e.g., Intel Nehalem and RISC-V Rocket [3]).

BPU incurs varied time cost between a correct and wrong prediction. An attacker can mount the timing channel attack based on this time variation to obtain the execution flow of the victim process [2].

RegFile is not targeted by existing OS-level techniques [13]. It has been discussed as a source of exploitable time variation, when there are data dependencies between registers [10], as well as can leak the data stored in the registers [37].

#### 4.2 Flushing Operations

Figure 6 depicts SIMF’s flushing operations targeting the components in SoF. Depending on the microarchitecture of each component, the flushing operations vary.

**Flushing L1 D-cache** (Figure 6a) mainly aims to flush the valid and dirty bits. These bits represent validity and coherency status of each cache line. Due to data coherence,

2Rocket chip recently added an optional L1 d-cache flushing instruction, CFLUSH.D.L1, which is "only for power-down" and "... only supported on systems without S-mode." This instruction is not available in the version of rocket chip used in this paper.

3www.intel.com/pressroom/archive/reference/whitewpaper_Nehalem.pdf
clearing each cache line’s valid bits and dirty bits must be performed along with write-back operation, if the cache line is dirty. Therefore, the entire L1 D-cache flush includes three sub-operations: 1) look up the cache line status corresponding to one selected cache line from the tag array; 2) write back the cache line, if it is dirty; and, 3) resetting the valid and dirty bits. These steps must be done for every cache line in the cache, which totals to \( N \) sequences of the sub-operations mentioned above.

**Flushing L1 I-cache** (Figure 6b) is a simple form of flushing L1 D-cache, since it is not necessary for I-cache to maintain coherence. Flushing L1 I-cache operation only needs to invalidate or reset the valid bits, where each bit maps to one cache line.

**Flushing TLBs** (Figure 6c) includes flushing TLBs at Level 1 and Level 2. This TLB system includes separate L1 TLBs for instruction (L1 ITLB) and data (L1 DTLB) and one unified L2 TLB (L2 TLB). TLB flushing operation aims to clean the valid bits for each TLB entry.

We assume BPU uses two-level adaptive branch prediction [43]. The operation for flushing BPU (Figure 6d) is composed of three major sub-operations as follows: 1) flushing branch target buffer (BTB) aims to clear the valid bits in BTB; 2) flushing branch history target (BHT) is more complex than BTB, where the history bits in the history register and the entries in the history table are to be cleared; and, 3) flushing return address stack (RAS) can be realized by resetting the stack pointer, which indicates that the RAS is empty.

**Flushing RegFile** aims to remove the user data directly from RegFile. Given a RegFile consisting of \( \#\text{Regs} \) registers, \( \#\text{Regs} \) registers are cleared. In addition, for maintaining the program’s correctness, RegFile flushing must be carefully operated after the registers are saved in cache/memory. Vice versa, the registers need to be recovered after flushing, before continuing the program execution. Hence, the context switch (for process switch) is a convenient point of time, when RegFile flushing can be performed.

### 4.3 Merging Flushing Operations

Based on the design of the flushing operations with respect to the SoF components, SIMF control is realized by merging these operations into one instruction.

Operation merging or fusion problem can be briefly defined as follows: Given the set of predefined flushing operations (FOs), noted as \( \mathcal{O} = \{O_1, O_2, ..., O_N\} \) and pipeline stages \( \mathcal{S} = \{S_1, S_2, S_3, ..., S_M\} \), scheduling \( O_i \) into pipeline stage \( S_j \).

Figure 7 summarizes the design constraints, represented as control and data dependencies, which must be considered when merging flushing operations in one instruction. The control dependencies are denoted as \( \delta^c \). The data dependencies are denoted as \( \delta^d \) for flow/true dependency, also known as read-after-write (RAW), as well as \( \delta^a \) for anti-dependency, a.k.a. write-after-read (WAR). SIMF considers two main data dependencies: 1) Flushing L1 I-cache (\( O_{1ic} \)) will cause refilling the instructions, whose newest version might be in the L1 D-cache and hence depends on flushing L1 D-cache (\( O_{1dc} \)); and, 2) Flushing L1 D-cache might require address translation in D-TLB, which will be flushed by \( O_{dtlb} \).

Table 2 depicts how the proposed SIMF merges the flushing operations \( \mathcal{O} \), assuming a classic 5-stage pipeline \( \mathcal{J} = \{S_{IF}, S_{ID}, S_{EX}, S_{ME}, S_{WB}\} \). Given the constraints, we aim to
schedule the FOs as late as possible (ALAP), which is equivalent to prioritizing issuing the FOs near the commit (i.e., write-back) stage. The first three stages are not considered given the control constraints (flushing must not start before valid execute/issue stage). $O_{11dc}$ is scheduled one stage earlier than the other operations ($\theta \setminus O_{11dc}$) to ensure that the dependencies are satisfied.

### 4.4 SIMF Pipeline Control

Table 3 illustrates the pipeline control mechanism for SIMF with a classic pipeline time table. Column 1 shows the instruction sequence executed from top ($i_0$) to bottom. Row 1 shows the clock cycles starting from the left ($CC_0$) to right. In each clock cycle, at least one pipeline stage, i.e., IF, ID, EX, ME, and WB, is executed, unless the instruction is stalled (denoted as “$\Box$”) or delayed (“$\cdot$”). As shown in Table 3, for maintaining the program’s correctness after flushing, SIMF ($i_1$) needs additional pipeline control mechanism to guarantee: 1) all the prior instructions must have been committed before flushing, which is denoted as $k_0, WB \rightarrow i_1, EX$; and, 2) all the following instructions must observe the resultant state of the components in SoF, which have been flushed, i.e., $i_1, WB \rightarrow i_2, IF$.

### 4.5 SIMF Software

SIMF can be deployed in software depending on the temporal isolation schemes. In this paper, we discuss two potential SIMF based temporal isolation schemes, which both use SIMF in kernel space (as a privileged instruction).

**Aggressive scheme:** Similar to [44], where even the kernel space is not trusted, the SIMF instruction can be deployed at the boundary between the switch from user space to kernel space, and the switch from kernel space to user space. This way ensures that every kernel/user switch will incur flushing, even if there will be no process switch. Such a scheme creates a strict temporal isolation and can introduce high overhead due to much more frequent activation of flushing operations.

**Moderate scheme:** Similar to [13], the SIMF instruction can be integrated in the software path where process/thread switch occurs, for instance, when the current security domain switches to another security domain in seL4 microkernel. This scheme will incur fewer flushing operations, while relying on the security assumptions provided by the security policy of the operating system.

Additional instructions are needed for RegFile flushing, to ensure the context will not be lost. If SIMF is deployed in the software path where context is saved, such as the trap entry of the operating system, the extra instructions needed will be much fewer. A few instructions are still required to be added to load back the values of the registers, which are needed for the system binary interface (SBI). Hence, for ease of deployment, register file flushing can be disabled.

### 5. EVALUATION

In this section, we evaluate SIMF on a RISC-V processor, implemented on an FPGA with various workloads to answer the following questions.

- How expensive the hardware cost is with SIMF implemented (§5.1)?
- What is the performance penalty for the worst case, that is when L1 D-cache is full (§5.2)?
- How SIMF performs when inserted into a state-of-art micro-kernel (§5.4)?
- How much does SIMF slow down a contemporary Linux kernel with SMP in a multi-core scenario (§5.5)?
- How much does SIMF affect user programs (§5.3)?
- What is the security enhancement (§5.6)?

To check the efficacy of SIMF, we implement the proposed SIMF as a new instruction, FLUSHX, in the Rocket core (i.e., in-order scalar RV64GC implementation of RISC-V ISA), which comes with Rocket Chip SoC (multi-core-capable and with hardware support for coherence) [3].
We ported the original repository of Rocket chip’s FPGA which is implemented in the same manner as the software.

Table 6: Core-level flushing performance (ARMv8 implementation is hard IP of Cortex-A53 on ZCU102; RV64GC implementation is soft core on ZCU102; Intel x86 Haswell and ARMv7 Cortex-A9 in Yellow are obtained from [13]).

| Arch. | FO       | #Cycles | #Dyn. Instr. | SoF |
|-------|----------|---------|--------------|-----|
| x86   | Indirect | 91800   | –            |     |
| ARMv7 | dccisw/icielau | 36000   | –           | L1-D&I |
| ARMv8 | dc_cuveic_ivau | 91299   | 65719        | L1-D&I |
| RV64GC| FLUSHX   | 16025.5 | 136          | Core-level |

We use a Xilinx ZYNQ Ultrascale+ FPGA (ZCU102) board to implement the RISC-V processor(s), which technology-advanced and has greater amount of resources than the existing FPGA boards (e.g., ZC702, Zedboard, and ZYBO FPGAs) targeted by the original Rocket chip’s FPGA build. We ported the original repository of Rocket chip’s FPGA build to ZCU102. SIMF (FLUSHX) is implemented into the rocket core with the configuration specified in Table 4.

5.1 Hardware Cost

The FPGA synthesis is performed with Vivado v2017.1 using default strategy.

Table 5 depicts the hardware cost, in terms of FPGA resources when the FLUSHX instruction is implemented. The major FPGA resources utilized include CLB LUTs, CLB flip/flops (F/Fs), block RAMs (BRAMs), DSPs (implementing arithmetic cells), physical input/output ports (I/O), clock buffers (BUFG), and mixed mode clock manager (MMCM). This result shows that supporting FLUSHX instruction mainly increases the total LUTs (by 6.7%) and F/Fs (by 14.8%). We also observe that FLUSHX without $O_{rf}$ (equivalent to the complete functionality of existing temporal isolation) has minimal overheads (1.9% LUTs and 3.0% F/Fs). The maximum clock frequency for FLUSHX is 187 MHz and for the baseline is 195 MHz.

5.2 Flushing Overhead

The first case study aims to measure the performance overhead of the proposed core-level SIMF in comparison to the contemporary ISA support. The test program is manually designed to: one, construct and fill a cache-sized contiguous memory space (via mmap()); and, two, execute the core-level flush.

Table 6 shows the comparison of overhead for core-level flushing between FLUSHX in the RISC-V processor and ARM Cortex-A53 using existing methods. ARM core flush is executed by calling __clear_cache(), which targets the cache-sized memory space, provided by Linux to the user space, which is implemented in the same manner as the software.

We observe the runtime overhead of executing FLUSHX instruction in real-world user programs, we test our systems using a representative embedded application benchmark suite, MiBench [16]. We test FLUSHX with two scenarios: 1) FLUSHXS incur a FLUSHX via a syscall (similar to moderate scheme); and, 2) FLUSHXT incur FLUSHX at every kernel/user crossing (similar to aggressive scheme). The benchmark suite is run on a simple application execution environment (riscv-pk), which provides user programs with

![Figure 8: Median performance overhead (in percentage) of running MiBench.](image)
POSIX syscall services. riscv-pk is customized to deploy FLUSHX in a new syscall and trap entry. For each program, we execute the program 50 times (standard deviation ≤ 1%).

As shown in Table 7, performing FLUSHX instruction once per execution (FLUSHX) incurs negligible overhead in both clock cycles and dynamic instruction count (within the margin of error), especially when compared to pure syscall overhead (“base-ecall”). Performing FLUSHX aggressively at every entering kernel space (FLUSHXT) can substantially increase the execution time and CPI by 15%. The main reason for the difference of overhead between FLUSHX and FLUSHXT is that FLUSHXT scheme activates a greater number of FLUSHX execution in these programs from the original system calls. These system calls do not include FLUSHX in the execution path at runtime in FLUSHX system.

Figure 8a and 8b depict the detailed view of the overhead for each benchmark application. For cycle overhead (shown in Figure 8a), among all the benchmark programs, there are two prominent cases, where FLUSHXT incurs a substantial cycle overhead. These are in stringsearch search (around 70%) and quick sort qsort (roughly 50%). The reason is that these two programs proportionally have more syscalls. In some cases, e.g., bitcounts bitcnts, FFT fft, and JPEG jpeg, the cycle overhead is negative, because the overhead is negligible within the range of standard deviation (due to cache and branch prediction behaviors). For dynamic instruction count, the overhead is negligible across all the benchmark programs.

5.4 seL4 Microkernel

To observe the system-level manifestation of SIMF in a real-world microkernel. We added FLUSHX into seL4 microkernel (v10.1.1), which is a security-oriented capability-based microkernel. We insert FLUSHX instruction into functions for thread switch, such as switchToThread() and switchToIdleThread(). seL4’s domain switch is a special case of thread switch, which largely follows the same execution path as thread switch.

To quantify the performance of SIMF, we measured the cost of scheduling, where thread switch is invoked, with the seL4test as the workload. seL4test is composed of 100 testing programs, each of which targets one set of seL4 properties. During the execution of seL4test, schedule() is called 3,496,281 times, while 427,189 events of thread switch are incurred during schedule. Both systems with and without FLUSHX finish the seL4test correctly, with the same output score.

Table 8 shows the total clock cycles and dynamic instruction count of scheduling for the system with and without POSIX syscall services. riscv-pk is customized to deploy FLUSHX in a new syscall and trap entry. For each program, we execute the program 50 times (standard deviation ≤ 1%).

| Arch. | FO     | #Cycles mean ± std | #Dyn. Instr. mean ± std |
|-------|--------|---------------------|------------------------|
| ARMv7 | –      | 560 ± 1%            | –                      |
| Armv7 | Ge et al. [13] | 21600 ± 1%         | –                      |
| RV64GC | FLUSHX | 940.5 ± 318.7     | 432.8 ± 155.3          |
| RV64GC | FLUSHX | 8568.1 ± 3738.5   | 436.9 ± 147.1          |

5.5 Linux with lmbench

We choose RISC-V Linux kernel v4.20 and add FLUSHX into the thread switch procedure __switch_to. We test the FLUSHX Linux and compare with the baseline Linux kernel by running lmbench [29]. For both systems, we create three types of hardware, composing 1 core, 4 cores, and 8 cores, each with two configurations of caches (16 KiB and 32 KiB) and TLBs (with and without L2 TLB).

Figure 10 shows the overhead of context switch latency due to FLUSHX. For larger caches and TLBs, FLUSHX incurs more overhead with a smaller working set and fewer processes. Using smaller caches and TLBs leads to much smaller flushing overhead (almost 1/2 in 8-core system). It is also seen that as processes increase, the overhead will approach 50% (for large caches and TLBs) or less (for small caches and TLBs). The worst-case overhead is witnessed in an extreme scenario, where two processes runs on one core with larger caches and TLBs, computing with a very small working set (0KiB).

5.6 Temporal Isolation Test

To evaluate the effects of FLUSHX instruction in face of timing channel attacks, we implement a classic L1 D-cache attack, namely Prime+Probe based on the open-source tool called Mastik [41]. We port Mastik to RISC-V to mount Prime+Probe cache timing attacks.
Figure 10: lmbench context switch latency (lat_ctx) as a function of the number of processes (2, 4, 8, 16, 32, 64, 96), with different size of working set, normalized to the baseline. GM: geometric mean. RISC-V Linux kernel version is 4.20 with FlushX inserted in __switch_to(). Each line represents a working set size in the legend.

Figure 11: Timing channel of L1 D-cache by Prime+Probe.

We create a simplified attack using lightweight proxy kernel, PK (riscv-pk). We implement the victim program as a dedicated system call. The content of the victim program is a patterned data cache access, adapted from the example code from Mastik. FlushX is inserted before returning to attacker’s process on FlushX core. We modify the attack program to raise this special system call, after cache prime is finished. The probed samples are set to 20,000, which is sufficient to witness the significance of the cache channels.

Figure 11a and 11b illustrates the samples from Sample 1 to 200, in the cache timing attack, on the baseline and FlushX systems, respectively. The clear cache behavior patterns of cache set accesses can be observed for the unprotected baseline system, where the cache set hit (less than 10 cycles of cache access time, in black) and miss (more than 50 cycles of access time in purple) can be differentiated. Figure 11b shows that the protected system, which executes FlushX before returning to the attacker’s process, and can cleanse the residual state (all cache misses) in the L1 D-cache.

6. RELATED WORK

Timing attack countermeasures have been proposed at differing layers of the computing stack, from hardware right up to the application layer.

Hardware-based countermeasures [33, 35, 38, 39, 40] mostly focus on redesigning the cache against cache based timing channel attacks. The work in [33] enforces cache partitioning to remove cache contention. Newcache [39] introduces randomized mapping in replacement of cache partitioning for better flexibility. CEASE/CEASER [35] uses encrypted cache addressing scheme to implement efficient randomization. [38] and ScatterCache [40] extends encryption-based randomization to combine cache address and process ID as
encryption input. Aiming at speculation-based side channel attacks, CleanupSpec [36] modifies cache policies and coherency management on system bus, in order to roll back the cache state after miss-speculation. These methods extensively modify the original cache operations, largely target cache timing attacks at the last level cache (LLC), and are evaluated in abstract models using system simulators (e.g., GEMS [4]). No hardware implementation has been reported. Another line of hardware-based countermeasures [12, 26] seek to eliminate timing channels by enforcing information flow tracking in hardware. These methods introduce new hardware description languages and usually incur additional memory elements for security tags.

**Software-based** methods are usually implemented in hypervisors, operating systems, or applications. These methods can be categorized as follows: Based on time measurement, FuzzyTime [18] and TimeWarp [28] adds intentional noise to the system clock so as to prevent the adversary from accurately measure the timing of microarchitectural events. The time noise will also affect the original programs system-wide, wherever accurate time is required. StealthMem [11, 22] implements spatial partitioning to enforce information isolation in LLC against timing attacks.

**Flushing** mechanism has been adopted by a variety of OS-level software-based countermeasures [13, 44]. Düppel [44] uses flushing of private L1 and L2 caches to inject timing noise so as to maximize the difficulty of mounting cache-based timing attacks. Düppel assumes the attackers can perform a probe as frequently as every 50,000 (about 60 KHz at 3 GHz clock speed) to 90,000 CPU cycles. Ge et al. [13] leverages core-level flushing along with L2 and LLC cache partitioning to minimize the available timing channels in all the microarchitectural components. The flushing is assumed to be performed at every domain switch.

Varyrs [31] uses flushing for cleansing private L1 and L2 caches, to protect Intel SGX enclave from various timing channel attacks, assuming the extreme case that privileged software is controlled by the attacker. The flushing is performed at the frequency of 100 Hz, 5.5 KHz, and 10 KHz. For 100 Hz, Varyrs incurs 19% drop-down in throughput of Nginx due to indirect flushing in Intel ISA.

Mi6 [6] is an enclave design for out-of-order RISC-V processors, which also includes a purge instruction to flushing on-core state (excluding register-file) upon (de)scheduling. SIMF differs to Mi6 in several aspects: Mi6 is specific to only RiscyOO processor and cannot be generalized, while SIMF can be implemented for any in-order processor; Mi6 relies on the specific features of the baseline processor RiscyOO and does not have the mechanism to actually clean replacement tags in caches and TLBs; Mi6 does not actually clean some microarchitectural states (e.g., issue queue), which may well be exploited by novel attacks; and, Mi6’s flushing mechanism does not write back the dirty cache lines, hence, it does not work for caches with write-back policy (which is dominant in real-world modern processors).

## 7. CONCLUSION

In this paper, we have presented SIMF, a new ISA extension to support efficient temporal isolation. SIMF is capable of flushing core-level state in one instruction execution and can be integrated with OS-level timing attack mitigation. We have prototyped SIMF as a FLUSHX instruction on RISC-V processor and evaluated on FPGA with a real-world microkernel, Linux kernel, user programs, and Prime+Probe cache timing attack. Our evaluation shows that SIMF removes the timing channels effectively with significantly less clock cycles and dynamic instruction count.

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