A novel active-input cascode current mirror with high precision and low power dissipation

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Abstract
In this article, a novel active-input cascode current mirror (CM) with high precision and low power consumption is proposed. First, the cascode input structure is employed upon the active-input CM to reduce the requirement of high-gain op-amp. In addition, the extra branch to the ground is designed. Subsequently, the resistance adaptive loop is separated from the current replication loop to eliminate the matching obstacle between two op-amps. The proposed CM fulfilled in 0.18 μm CMOS technology, is able to operate with a supply voltage of 1.0 V, wide input range of 100 nA–1 mA, low power dissipation of 40 μW, and lower replication error (below 1.4%) than the same configuration using the conventional active-input mechanism.

KEYWORDS
active-input, cascode output, current mirror, replication error

1 | INTRODUCTION

A current mirror (CM) is a unity gain current amplifier which replicates proportionally the input current at its high impedance output node. It is widely adopted as one of the most critical blocks in integrated analog or mixed-signal circuits such as current-mode A/D converters,1–3 low-dropout regulator,4–6 operational amplifiers,7,8 voltage level shifter,9–11 and analog filters12,13 and so forth. Therefore, the performances of CMs could directly influence system performances.14 At the same time, with the rapid development of biomedicine, more and more CMs are used in the fields of biomedical circuits, bio-amplifiers and implantable microstimulators and so forth,15–17 which puts forward higher requirements for the accuracy and power dissipation of CMs. To improve the CM performance and make it compatible with the present industry trends, various high-performance topologies have been proposed. The active-input CM proposed by Serrano and Linares-Barranco could realize adaptive input impedance which decreases with the increasing of input current. Thus, high replication accuracy in active-input CM could be obtained over a wide input range.18 Bhawna Aggarwal et al. reported a very high-performance current mirror in 2014.19 By using super cascode configuration at the output side, the output current accurately copies the input current without any offset component, and the output resistance increases considerably. In 2016, Stefan Leitner and Wang Haibo proposed a current mirror with two feedback loops based on op-amps,
which eliminates the requirements of high impedance and wide swing for its input node, and ensures the accuracy of current replication. However, the principle of active feedback lies in the test of input current changes to control the gate voltage generating the output current. In such structure, the input node, which is mainly the drain of transistor, is connected to the gates through an active device such as Operational transconductance amplifiers and op-amps. Therefore, the op-amps with high gain and excellent matching performance would be required, which increases the design difficulty of op-amps and reduces the applicability of the circuit.

In this article, a novel active-input cascode current mirror with high precision and low power dissipation is proposed, which employs the cascode input structure to reduce the gain requirement of the op-amps. In addition, an extra branch to the ground is inserted to separate the adaptive input impedance loop from the current replication loop to eliminate the op-amp matching problem. In summary, the proposed CM combines the advantages of cascode input stage and active-input CM to improve its overall performance.

2 | PROPOSED CURRENT MIRROR

The schematics of the conventional active-input CM and the proposed CM are respectively depicted in Figure 1A,B. Different from the conventional active-input CM, the proposed CM contains three branches X, Y, Z to the ground and two negative feedback loops. In Figure 1B, M1 and M2 work in critical subthreshold region to obtain lower quiescent current and the maximum gate source voltage swing, and M3–M9 work in saturation region.

The adaptive input impedance loop (loop1) is composed of branches X, Y and op-amp A1, which ensures the input voltage \( V_1 \) is identically equal to the reference voltage \( V_{\text{ref}} \). Thus, the input impedance of the proposed CM decreases with the increasing of the input current. Subsequently, we further illustrate how the input voltage \( V_1 \) is forced to equal the reference voltage \( V_{\text{ref}} \) by the loop1. We assume \( i_{\text{in}} \) increases by \( i_{\text{in}} \). Then, \( V_4 \) (the input of op-amp A1) increases, which results in an increase of M1 gate voltage. As a result, the drain-source equivalent impedance of M1 decreases and input voltage \( V_1 \) remains constant. The small signal model of the loop1 is shown in Figure 2.

Here, \( g_{m1} \) and \( r_{oi} \) represent the transconductance and source-drain equivalent impedance of transistor \( M_i \), respectively. By analyzing this model, it can be found that

\[
i_{\text{in}} = g_{m1} A_{d1} v_4 + \frac{v_{\text{in}}}{r_{o1}} - g_{m4} v_{\text{in}} + \frac{v_4 - v_{\text{in}}}{r_{o4}}
\]

\[
-g_{m4} v_{\text{in}} + \frac{v_4 - v_{\text{in}}}{r_{o4}} + \frac{v_4}{r_{o6}} = 0
\]
Then, from Equations (1) to (2), it is easy to induce that

\[ i_{\text{in}} = \left( g_{m1}A_{d1} - \frac{1}{r_{06}} \right) \left( g_{m4} + \frac{1}{r_{04}} \right) (r_{04}\|r_{06})v_{\text{in}} + \frac{v_{\text{in}}}{r_{01}} \]  

(3)

\[ r_{\text{in}} = \frac{v_{\text{in}}}{i_{\text{in}}} = \frac{1}{\left( g_{m1}A_{d1} - \frac{1}{c_{g}} \right) \left( g_{m4} + \frac{1}{c_{g}} \right) (r_{04}\|r_{06}) + \frac{1}{c_{g}}} \]  

(4)

Since \( r_{04}g_{m4} > 1, A_{d1}g_{m1}r_{06} > 1 \), Equation (4) can be written in simplified form as:

\[ r_{\text{in}} = \frac{1}{A_{d1}g_{m1}g_{m4}(r_{04}\|r_{06})} \]  

(5)

where \( A_{d1} \) represents the gain of op-amp \( A_{1} \), \( A_{d1}g_{m1}g_{m4}(r_{04}\|r_{06}) \) is loop gain of loop1. From Equation (5), the input impedance of the proposed CM is inverse of loop gain, which is very low (less than 1 \( \Omega \)). Therefore, the cascode input structure of M1 and M4 increases the loop gain by \( g_{m4}(r_{04}\|r_{06}) \) times compared with the active-input CM when the gain of the op-amps is constant. As the gain of the op-amps is an important part of the loop gain, the gain requirement of the op-amps is reduced while performance requirements remain unchanged.

The current replication loop (loop2) is consisted of branches Y, Z and op-amp \( A_{2} \), which eliminates the influence of mismatch in drain to source voltages of basic CM pair. In the loop2, the input and output of the proposed CM are connected by the amplifier \( A_{2} \) via negative current–voltage feedback which further increases the output impedance and improves the stability of output current. In addition, two-stage topologies are adopted for op-amp \( A_{2} \) to achieve moderate gain and relatively large output swing. M8 and M9 constitute the source follower, and (M3, M4), (M6, M7) respectively constitute a common gate amplifier with current mirror as load. In the output stage, M2 and M3 form cascode structure to provide high output impedance. In the ideal state \( (A_{d1}, A_{d2} \text{ infinity}) \), \( I_{\text{out}} \) and \( I_{\text{in}} \) are equal under the static equilibrium condition. However, because the gain of \( A_{1}, A_{2} \) is limited, there is an error between \( I_{\text{out}} \) and \( I_{\text{in}} \), that is, replication error. It is equivalent to the difference between the small signal variation \( i_{\text{in}} \) and \( i_{\text{out}} \). Ignoring the bulk effect, it could be seen that

\[ v_{4} = g_{m4}(r_{04}\|r_{06})v_{1} \]  

(6)

\[ v_{5} = g_{m5}(r_{05}\|r_{07})v_{2} \]  

(7)

\[ v_{2} = \left( A_{d2}(v_{4} - v_{5}) - v_{2}\right) g_{m3} - g_{m5}v_{2} + \frac{v_{5} - v_{2}}{r_{05}} \right] r_{02} \]  

\[ -g_{m3}v_{2} + \frac{v_{5} - v_{2}}{r_{05}} + \frac{v_{5} - v_{2}}{r_{07}} = 0 \]  

(9)
where \( A_{d2} \) represents the gain of op-amp \( A_2 \). Meanwhile, \((M1, M2), (M4, M5), (M6, M7)\) are transistor pairs and respectively have the same \( W/L \) ratio. Then

\[
r_{o1} = r_{o2}
\]

(10)

\[
g_{m4}(r_{o4} || r_{o6}) = g_{m5}(r_{o5} || r_{o7})
\]

(11)

Then, from Equations (6) to (11), it can be calculated that

\[
\frac{v_2}{v_1} = \frac{A_{d2}g_{m4}(r_{o4} || r_{o6})g_{m3}r_{o2}}{g_{m4}(r_{o4} || r_{o6}) \left( A_{d2}g_{m3} + \frac{1}{r_{o7}} \right) r_{o2} + g_{m3}r_{o2} + 1}
\]

(12)

Combining Equations (10) and (12), the relationship between output current \( i_{out} \) and input current \( i_{in} \) is obtained as:

\[
\frac{i_{out}}{i_{in}} = \frac{v_2/r_{o2}}{v_1/r_{o1}} = \frac{A_{d2}g_{m4}(r_{o4} || r_{o6})g_{m3}r_{o2}}{g_{m4}(r_{o4} || r_{o6}) \left( A_{d2}g_{m3} + \frac{1}{r_{o7}} \right) r_{o2} + g_{m3}r_{o2} + 1}
\]

(13)

Since \( A_{d2}g_{m3}r_{o7} \gg 1 \), Equation (13) can be simplified as:

\[
\frac{i_{out}}{i_{in}} = \frac{v_2/r_{o2}}{v_1/r_{o1}} = \frac{A_{d2}g_{m4}(r_{o4} || r_{o6})g_{m3}r_{o2}}{A_{d2}g_{m3}g_{m4}r_{o2}(r_{o4} || r_{o6}) + g_{m3}r_{o2} + 1}
\]

(14)

It is noted that the loop2 makes \( i_{out} \) equal to \( i_{in} \) by regulating voltage \( v_2 \) equal to \( v_1 \). Subsequently, the replication error \( \epsilon \) can be given as

\[
\epsilon = \frac{|i_{in} - i_{out}|}{i_{in}} \times 100\% = \frac{v_1/r_{o1} - v_2/r_{o2}}{v_1/r_{o1}} \times 100\%
\]

(15)

Then, from Equations (10), (14) and (15), it is easy to show that

\[
\epsilon = \frac{g_{m3}r_{o2} + 1}{A_{d2}g_{m3}g_{m4}r_{o2}(r_{o4} || r_{o6}) + g_{m3}r_{o2} + 1} \times 100\%
\]

(16)

where \( A_{d2}g_{m3}g_{m4}r_{o2}(r_{o4} || r_{o6}) \) represents the loop gain of loop2. From Equations (6) and (16), by replacing common source input stage in Figure 1A with cascode structure in Figure 1B, the loop gain of loop1 and loop2 are increased by \( g_{m4}(r_{o4} || r_{o6}) \) times. Equation (16) shows that the replication error \( \epsilon \) is very low due to the enormous loop gain of loop2. Meanwhile, since \( i_{in} \) and \( g_{m4} \) are positively correlated, the replication error \( \epsilon \) decreases as \( i_{in} \) increases. Subsequently, the output current \( i_{out} \) can be derived as:

\[
i_{out} = \frac{v_{out} - v_2}{r_{o3}} + A_{d2}g_{m3}(-v_5 - v_2)
\]

(17)

Combining Equations (7) and (17), we get:

\[
r_{out} = \frac{v_{out}}{i_{out}} = r_{o3} + r_{o2} + A_{d2}g_{m3}r_{o2}r_{o3}g_{m5}(r_{o5} || r_{o7}) + 1]
\]

(18)

Since \( g_{m5}(r_{o5} || r_{o7}) \gg 1 \), the output impedance of the proposed CM can be approximated as

\[
r_{out} \approx A_{d2}g_{m3}r_{o2}r_{o3}g_{m5}(r_{o5} || r_{o7})
\]

(19)

From Equation (19), the output impedance of the proposed CM is very high (in G\( \Omega \) range) through the cascode input structure.

Furthermore, when the gain of \( A_1 \) and \( A_2 \) in Figure 1A are the same with that in Figure 1B, respectively, lower input impedance, lower current replication error and higher output impedance in Figure 1B are achieved than that in Figure 1A. The details of the circuit analysis are shown in Table 1.
TABLE 1 Circuit analysis results

| Structure                        | Active-input CM | Proposed CM |
|----------------------------------|-----------------|-------------|
| The loop gain of loop1           | $A_d1g_{m1}$    | $A_d1g_{m1}(r_{o4}||r_{o6})$ |
| The loop gain of loop2           | $A_d2g_{m3}r_{o2}$ | $A_d2g_{m3}r_{o2}g_{m4}(r_{o4}||r_{o6})$ |
| Input resistance                 | $\frac{1}{A_d1r_{o1}}$ | $\frac{1}{A_d1r_{o1}+r_{o6}}$ |
| Output resistance                | $A_d2g_{m3}r_{o2}r_{o3}$ | $A_d2g_{m3}r_{o2}r_{o3}(r_{o5}||r_{o7})$ |
| Replication error                | $\frac{\delta_{d2}r_{o2}+1}{A_d2r_{o2}+1} \times 100\%$ | $\frac{\delta_{d2}r_{o2}+1}{A_d2r_{o2}+1} \times 100\%$ |
| Transfer function                | $\frac{-A_d1g_{m1}}{A_d1r_{o1}+C_{db1}}$ | $\frac{A_d1g_{m1} \left( \frac{r_{o4}}{r_{o4}} - \frac{r_{o6}}{r_{o6}} \right)}{\sqrt{C_{db4}C_{db1}+g_{m4}g_{m1}} + \frac{A_d1g_{m1}}{r_{o6}}}$ |

3 RESULTS AND ANALYSIS

With 0.18 μm CMOS process, the proposed CM is designed by Specter simulator using a 1.0 V power supply and $V_{ref} = 10$ mV. The W/L ratio of MOS transistors (M1, M2, M3 and (M4-M9) are (500/1 μm), (400/0.18 μm), and (5/1 μm), respectively. The gain of $A_1$ and $A_2$ in Figure 1A are the same with that in Figure 1B. The current replication error $\varepsilon$ is shown in Figure 3. It is obvious that the proposed CM has a lower replication error than that in the conventional active-input CM. The “$\varepsilon$” decreases with the increase of the current $I_{in}$, and the larger the gain of loop2, the smaller the “$\varepsilon$”, which is consistent with the trend shown in Equation (16). When the input current is 10 μA, the replication error of conventional CM is about 18 times more than that of the proposed CM.

The input resistance of the proposed CM along with that of the active-input CM is depicted in Figure 4. The input resistance curves show that the input impedance of the proposed CM and active-input CM are 0.04 and 73.21 Ω in the low frequency range, respectively. This shows that the loop1 and the cascode input stage effectively reduce the input impedance of the proposed CM. The output resistance curves of the proposed CM and the active-input CM are shown in Figure 5. In the current–voltage negative feedback loop, the greater the loop gain, the higher the output impedance. Due to the higher loop gain as shown in Table 1, the output impedance of proposed CM is higher than that of conventional CM, as shown in Figure 5. Therefore, the improvement of the proposed CM is effective.

According to the transfer function of Table 1, the proposed CM is a system with two poles and a zero point. The main poles of active-input CM and proposed CM are $A_{d1}g_{m1}/C_{db1}$ and $A_{d1}g_{m1}/C_{db4}$, where $C_{dbi}$ represents the parasitic capacitance between the drain of Mi and the substrate. Since the parasitic capacitance between the drain of the MOS transistor and the substrate is proportional to the channel width, and the channel width of M4 is lower than that of M1, $C_{db4}$ is lower than parasitic capacitance $C_{db1}$. Therefore, the dominant pole location of proposed CM is further shifted away from the imaginary axis in s-plane. As given out in Figure 6, the bandwidth of proposed CM is slightly wider to that of conventional CM.

In order to better demonstrate the performance of CMs, Table 2 lists comparison of multiple parameters. These comparative results illustrate the fact that the proposed CM has lower replication error, smaller input impedance and lower power dissipation.

![Figure 3](image-url) Replication error of the proposed CM and active-input CM when $I_{in}$ changes from 100 nA to 1 mA
**FIGURE 4**  Input resistance of the proposed CM and active-input CM when $I_{in} = 10 \mu A$

**FIGURE 5**  Output resistance of the proposed CM and active-input CM when $I_{in}$ changes from 100 nA to 1 mA

**FIGURE 6**  Frequency response of the proposed CM and active-input CM when $I_{in} = 10 \mu A$
### Table 2  Comparison of performance parameters of CMs

| Parameters          | Proposed CM | 14  | 15  | 18   |
|---------------------|-------------|-----|-----|------|
| Replication error (%)  | 0.1–1.4     | 0.1 | 3.4 | 0.4–5 |
| Range (μA)          | $10^{-1}$–$10^3$ | 0–75 | 0–500 | $10^{-1}$–$10^3$ |
| Input resistance (Ω) | 0.04        | 1.6×$10^4$ | 5×$10^3$ | 73.21 |
| Output resistance (Ω) | 2.3×$10^9$   | 3.2×$10^{11}$ | 9×$10^9$ | 1.8×$10^8$ |
| Bandwidth (Hz)      | 8.2×$10^7$   | 1×$10^8$    | 2.25×$10^9$ | 5.1×$10^7$ |
| Power dissipation (μW) | 40          | 570          | 58.14   | 36.2   |
| Technology (μm)     | 0.18        | 0.13         | 0.18    | 0.18   |

## 4  CONCLUSIONS

A novel active-input cascode current mirror has been presented in this article. Different from the traditional current mirror with two cascaded operational amplifiers, the proposed CM inserts an extra branch to the ground, which separates resistance adaptive loop from the current replication loop. This technique not only solves the matching problem of cascaded op-amps but also decreases the difficulty of circuit design. Additionally, the proposed CM with cascode input structure increases the loop gain of active-input CM and reduces the gain demand of the op-amps. Simulations on a practical implementation along with numerical computation based on the proposed modeling have been carried out, displaying good correlation between the two. Realized in the CMOS 0.18 μm technology under 1.0 V supply voltage, the CM achieves low replication error (below 1.4%) and low power dissipation of 40 μW with the wide input range of 100 nA–1 mA, which makes it well candidate to the realization of the high accuracy and low power dissipation biomedical circuits.

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## CONFLICT OF INTEREST

The authors declare no potential conflict of interests.

## PEER REVIEW

The peer review history for this article is available at https://publons.com/publon/10.1002/eng2.12451.

## DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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