Hierarchical Neural Architecture Search for Single Image Super-Resolution

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Abstract—Deep neural networks have exhibited promising performance in image super-resolution (SR). Most SR models follow a hierarchical architecture that contains both the cell-level design of computational blocks and the network-level design of the positions of upsampling blocks. However, designing SR models heavily relies on human expertise and is very labor-intensive. More critically, these SR models often contain a huge number of parameters and may not meet the requirements of computation resources in real-world applications. To address the above issues, we propose a Hierarchical Neural Architecture Search (HNAS) method to automatically design promising architectures with different requirements of computation cost. To this end, we design a hierarchical SR search space and propose a hierarchical controller for architecture search. Such a hierarchical controller is able to simultaneously find promising cell-level blocks and network-level positions of upsampling layers. Moreover, to design compact architectures with promising performance, we build a joint reward by considering both the performance and computation cost to guide the search process. Extensive experiments on five benchmark datasets demonstrate the superiority of our method over existing methods.

Index Terms—Super-Resolution, Neural Architecture Search

I. INTRODUCTION

Image super-resolution (SR) is an important computer vision task that aims at designing effective models to reconstruct the high-resolution (HR) images from the low-resolution (LR) images [1]–[6]. Most SR models consist of two components, namely several upsampling layers that increase spatial resolution and a set of computational blocks (e.g., residual block) that increase the model capacity. These two kinds of blocks/layers often follow a two-level architecture, where the network-level architecture determines the positions of the upsampling layers (e.g., SRCNN [7] and LapSRN [8]) and the cell-level architecture controls the computation of each block/layer (e.g., RCAB [9]). In practice, designing deep models is often very labor-intensive and relies heavily on human expertise [10]–[13]. More critically, these hand-crafted architectures are often not optimal in practice.

Regarding this issue, many efforts have been made to automate the model designing process via Neural Architecture Search (NAS) [14]. Specifically, NAS methods seek to find the optimal cell architecture [14]–[16] or a whole network architecture [17]. These automatically discovered architectures often outperform the manually designed architectures in both image classification and language modeling tasks [14], [17]. However, existing methods may suffer from two limitations if we apply them to search for an optimal SR architecture.

First, it is hard to directly search for the optimal two-level SR architecture. For SR models, both the cell-level blocks and network-level positions of upsampling layers play very important roles to model performance. However, existing NAS methods only focus on one of the architecture levels. Thus, how to simultaneously find the optimal cell-level block and network-level positions of upsampling layers is still unknown.

Second, most methods only focus on improving image reconstruction performance but ignore the computational complexity. In general, a larger or more complex model often has better performance. However, given limited computation resources, these models are often too large and become hard to be applied to real-world applications [18], [19]. Regarding this issue, how to automatically design promising architectures with low computation cost is very important.

To address the above issues, we propose a novel Hierarchical Neural Architecture Search (HNAS) method to automatically design SR architectures. Unlike existing methods, HNAS simultaneously searches for the optimal cell-level blocks and the network-level positions of upsampling layers. Moreover, by considering the computation cost to build the joint reward, our method is able to produce promising architectures with low computation cost.

Our contributions are summarized as follows:

- We propose a novel Hierarchical Neural Architecture Search (HNAS) method to automatically design cell-level blocks and determine network-level positions of upsampling layers.
- We propose a joint reward that considers both the SR performance and the computation cost of SR architectures. By training HNAS with such a reward, we can obtain a series of architectures with different performance and computation cost.
- Extensive experiments on several benchmark datasets demonstrate the superiority of the proposed method.

II. PROPOSED METHOD

In this paper, we propose a Hierarchical Neural Architecture Search (HNAS) method to automatically design promising two-level SR architectures, i.e., with good performance and low computation cost. To this end, we first define our hierarchical search space that consists of a cell-level search space and a network-level search space. Then, we propose a hierarchical
controller as an agent to search for good architectures. To search for promising SR architectures with low computation cost, we develop a joint reward by considering both the performance and computation cost. We show the overall architecture and the controller model of HNAS in Figure 1.

A. Hierarchical SR Search Space

In general, SR models often consist of two components, namely several upsampling layers that increase spatial resolution and a series of computational blocks that increase the model capacity. These two components form a two-level architecture, where the cell-level identifies the computation of each block and the network-level determines the positions of the upsampling layers. Based on the hierarchical architecture, we propose a hierarchical SR search space that contains a cell-level search space and a network-level search space.

Cell-level search space. In the cell-level search space, as shown in Fig. 2, we represent a cell as a directed acyclic graph (DAG) [14], [15], where the nodes denote the feature maps in deep networks and the edges denote some computational operations, e.g., convolution. In this paper, we define two kinds of cells: (1) the normal cell that controls the model capacity and keeps the spatial resolution of feature map unchanged, and

(2) the upsampling cell that increases the spatial resolution. To design these cells, we collect the two sets of operations that have been widely used in SR models. We show the candidate operations for both cells in TABLE I.

For the normal cell, we consider seven candidate operations, including identity mapping, $3 \times 3$ and $5 \times 5$ dilated convolution, $3 \times 3$ and $5 \times 5$ separable convolution, up and down-projection block (UDPB) [20], and residual channel attention block (RCAB) [9]. For the upsampling cell, we consider 5 widely used operations to increase spatial resolution. Specifically, there are 3 interpolation-based upsampling operations, including area interpolation, bilinear interpolation [7], and nearest-neighbor interpolation [21]. Moreover, we also consider 2 trainable convolutional layers, namely the deconvolution layer (also known as transposed convolution) [22] and the sub-pixel convolution [23].

Based on the candidate operations, the goal of HNAS is to select the optimal operation for each edge of DAG and learn the optimal connectivity among nodes (See more details in Section II-B).

Network-level search space. Note that the position of upsampling block/layer plays an important role in both the performance and computation cost of SR models. Specifically, if we put the upsampling block in a very shallow layer, the

TABLE I

| Normal Cell/Block                      | Upsampling Cell/Block                   |
|----------------------------------------|-----------------------------------------|
| identity (skip connection)             | area interpolation                      |
| $3 \times 3$ dilated convolution       | bilinear interpolation                  |
| $5 \times 5$ dilated convolution       | nearest-neighbor interpolation          |
| $3 \times 3$ separable convolution     | sub-pixel layer                         |
| $5 \times 5$ separable convolution     | deconvolution layer                     |
| up and down-projection block [20]      |                                         |
| residual channel attention block [9]   |                                         |

Fig. 1. Architecture of SR model and the overview of the proposed hierarchical controller. (a) The two-level architecture for SR models that consist of $L = M + N + 1$ cells/blocks. (b) The overview of the hierarchical controller.

Fig. 2. An example of DAG that represents a cell architecture.
feature map would increase too early and hence significantly increase the computational cost of the whole model. By contrast, when we put the upsampling block in a deep layer, there would be little or no layers to process the upsampled features and hence the computation to obtain high resolution images may be insufficient, leading to suboptimal SR performance. Regarding this issue, we seek to find the optimal position of the upsampling block for different SR models.

Let \( N \) and \( M \) denote the number of layers before and after the upsampling block (See Figure 1(a)). Thus, there are \( L = M + N + 1 \) blocks in total. Given specific normal and upsampling cells, our goal is to find the optimal position of the upsampling block among \( L \) layers. We will show how to determine the position in Section B.

B. Hierarchical Controller for HNAS

Based on the hierarchical search space, we seek to search for the optimal cell-level and network-level architectures. Following [14], [17], we use a long short-term memory (LSTM) [24] as the controller to produce candidate architectures (represented by a sequence of tokens) [17]. Regarding the two-level hierarchy of SR models, we propose a hierarchical controller to produce promising architectures. Specifically, we consider two kinds of controllers, including a cell-level controller that searches for the optimal architectures for both normal block and upsampling block, and a network-level controller that determines the positions of upsampling layers.

Cell-level controller. We utilize a cell-level controller to find the optimal computational DAG with \( B \) nodes (See example in Fig. 2). In a DAG, the input nodes \(-2\) and node \(-1\) denote the outputs of the second nearest and the nearest cell in front of the current block, respectively. The remaining \( B-2 \) nodes are intermediate nodes, each of which also takes two previous nodes in this cell as inputs. For each intermediate node, the controller makes two kinds of decisions: 1) which previous node should be taken as input and 2) which operation should be applied to each edge. All of these decisions can be represented as a sequence of tokens and thus can be predicted using the LSTM controller [17]. After repeating \( B-2 \) times, all of the \( B-2 \) nodes are concatenated together to obtain the final output of the cell, i.e., the output node.

Network-level controller. Once we have the normal block and upsampling block, we seek to further determine where we should put the upsampling block to build the SR model. Given a model with \( L \) layers, we predict the position, i.e., an integer ranging from 1 to \( L \), where we put the upsampling block. Since such a position relies on the design of both normal and upsampling blocks, we build the network-level controller that takes the embeddings (i.e., hidden states) of two kinds of blocks as inputs to determine the position. Specifically, let \( h_N \) and \( h_U \) denote the last hidden states of the controllers for normal block and upsampling block, respectively. We concatenate these embeddings as the initial state of the network level controller (See Fig. 1(b)). Since the network-level controller considers the information of the architecture design of both the normal and upsampling blocks, it becomes possible to determine the position of the upsampling block.

Algorithm 1 Training method for HNAS.

**Initial:** The number of iterations \( T \); learning rate \( \eta \), shared parameters \( w \), controller parameters \( \theta \).

1: Initialize \( w \) and \( \theta \).
2: for \( i = 1 \) to \( T \) do
3: // Update \( w \) by minimizing the training loss
4: for each iteration on training data do
5: Sample \( \alpha \sim \pi(\alpha; \theta) \);
6: \( w \leftarrow w - \eta \nabla_w \mathcal{L}(\alpha, w) \).
7: end for
8: // Update \( \theta \) by maximizing the reward
9: for each iteration on validation data do
10: Sample \( \alpha \sim \pi(\alpha; \theta) \);
11: \( \theta \leftarrow \theta + \eta \mathcal{R}(\alpha) \nabla_\theta \log \pi(\alpha; \theta, \Omega) \).
12: end for
13: end for

C. Training and Inference Methods

To train HNAS, we first propose the joint reward to guide the architecture search process. Then, we depict the detailed training and inference methods of HNAS.

**Joint reward.** Note that designing promising architectures with low computation cost is of critical importance for real-world SR applications. To this end, we build a joint reward by considering both performance and computation cost to guide the architecture search process. Given any architecture \( \alpha \), let \( \text{PSNR}(\alpha) \) be the PSNR performance of \( \alpha \), \( \text{Cost}(\alpha) \) be the computation cost of \( \alpha \) in terms of FLOPs\(^1\). The joint reward can be computed by

\[
\mathcal{R}(\alpha) = \lambda \cdot \text{PSNR}(\alpha) - (1 - \lambda) \cdot \text{Cost}(\alpha),
\]

where \( \lambda \) denotes the weight of model performance in the joint reward. In general, the higher PSNR or lower cost the controller produces, the better the model will be. From Eqn. 1, a larger \( \lambda \) would result in the architectures with better performance but higher cost (See results in Table 1). In practice, we can adjust \( \lambda \) according to the requirements of real-world applications.

**Training method for HNAS.** With the joint reward, following [14], [17], we apply the policy gradient [25] to train the controller. We show the training method in Algorithm 1. To accelerate the training process, we adopt the parameter sharing technique [14], i.e., we construct a large computational graph, where each subgraph represents a neural network architecture, hence forcing all architectures to share the parameters.

Let \( \theta \) and \( w \) be the parameters of the controller model and the shared parameters. The goal of HNAS is to learn an optimal policy \( \pi(\cdot) \) and produce candidate architectures by conduct sampling \( \alpha \sim \pi(\alpha) \). To encourage exploration, we introduce an entropy regularization term into the objective to prevent the controllers from premature convergence [25].

**Inferring Architectures.** Based on the learned policy \( \pi(\cdot) \), we conduct sampling to obtain promising architectures. Specifically, we first sample several candidate architectures and then select the architecture with the highest validation performance. Finally, we build SR models using the searched architectures (including both the cell-level blocks and network-level position of upsampling blocks) and train them from scratch.

\(^1\)FLOPs denotes the number of multiply-add operations.
In the experiment, we use the DIV2K dataset [35] to train all the models. To show the effectiveness of our method, we conduct comparisons on five benchmark datasets, including Set5 [36], Set14 [37], BSD100 [38], Urban100 [39], and Manga109 [40]. We compare different models in terms of PSNR, SSIM, and FLOPs. Please see more training details in supplementary. We have made the code of HNAS available at https://github.com/guoyongcs/HNAS-SR.

### A. Quantitative Results

In this experiment, we compare our method with several hand-crafted SR models, including the Bicubic, SRCNN [7], VDSR [27], DRCN [28], DRRN [29], SelNet [30], CARN [31], MoreMNAS [32], and FALSR [33]. By training HNAS with different $\lambda$, we can obtain a series of architectures with different performance and computation cost. To illustrate this, we set $\lambda = \{0.2, 0.6, 0.9\}$ and obtain 3 architectures HNAS-A/B/C accordingly. Please see the detailed architectures in supplementary.

Table II shows quantitative comparisons for $2 \times 2$ SR. Note that all FLOPs are measured based on a $3 \times 480 \times 480$ input LR image. Compared with the hand-crafted models, our models tend to yield higher PSNR and SSIM and lower fewer FLOPs. Specifically, HNAS-A yields the lowest FLOPs but still outperforms a large number of baseline methods. Moreover, when we gradually increase $\lambda$, HNAS-B and HNAS-C take higher computation cost and yield better performance. These results demonstrate that HNAS can produce architectures with promising performance and low computation cost.

### B. Visual Results

To further show the effectiveness of the proposed method, we also conduct visual comparisons between HNAS and three SR methods, such as CARN [31], MoreMNAS [32] and FALSR [33]. We show the results in Fig. 3.

From Fig. 3, the considered baseline methods often produce very blurring images with salient artifacts. By contrast, the searched models by HNAS are able to produce sharper images than other methods. These results demonstrate the effectiveness of the proposed method.

### IV. Conclusion

In this paper, we have proposed a novel Hierarchical Neural Architecture Search (HNAS) method to automatically search for the optimal architectures for image super-resolution (SR) models. Since most SR models follow the two-level architecture design, we define a hierarchical SR search space and develop a hierarchical controller to produce candidate architectures. Moreover, we build a joint reward by considering both SR performance and computation cost to guide the search process of HNAS. With such a joint reward, HNAS is able to design promising architectures with low computation cost. Extensive results on five benchmark datasets demonstrate the effectiveness of the proposed method.
Supplementary Materials for “Hierarchical Neural Architecture Search for Single Image Super-Resolution”

We organize our supplementary materials as follows. First, we show the concrete structure about our derived models, including HNAS-A, HNAS-B and HNAS-C, and then do some brief analysis in Section A. Second, we will depict the implementation details about our HNAS models, including the datasets and training details in Section B.

A. Analysis of Model Structures

The Derived Models. The graph representations of HNAS-A, HNAS-B and HNAS-C are shown in Fig. 4.

As shown in Fig. 4, we can observe that the structures of our derived models, HNAS-A, HNAS-B and HNAS-C, are quite different from each other. We provide enough operations for cell nodes to choose, including seven candidate operations and five upsampling operations in the search space of normal cell and upsampling cell respectively, as mentioned in TABLE I. Besides, the computational DAG consists of B nodes, and the intermediate B-2 nodes can randomly take two previous nodes in this cell as inputs, which provides a series of models that have different structures and performance for model selection.

B. Implementation Details

When training HNAS model, we use different setting about datasets and hyper-parameters. Thus, we will present our implementation details on both the datasets and the training details in this section.

Datasets. Following [27], we train all SR networks using 800 training images from DIV2K dataset [35]. Specially, at search stage, we split DIV2K training set into 40% and 60% slices to train the model parameters \( w \) and the transformer parameters \( \theta \), respectively. Set5 [36] dataset is used as the validation set. After searching stage, we can infer some novel different cell architectures. Then, we re-train these cell architectures from scratch with all the 800 images from DIV2K dataset.

Training details. We employ one-layer Long Short-Term Memory (LSTM) [24] network with 100 as our RNN model. The learning rate follows a cosine annealing schedule with \( \eta_{\text{max}} = 0.001 \) and \( \eta_{\text{min}} = 0.00001 \) [41]. The batch-size is set to 16. The ADAM optimizer is used to train our model. We train the three LSTM controllers using the same settings, except for using \( \eta_{\text{max}} = 0.0003 \) and \( \eta_{\text{min}} = 0.00015 \). We add the controller’s sample entropy to the reward, weighted by 1. Each architecture search is run for 400 epochs. The total number of layer is set to 12 and the channels of each operations to 8. Note that after concatenating the output of cell nodes, the channels of a model is equal to 32. At the inferring stage, we retrain the selected model using the same settings as the searching stage, except for setting 64 channels of each operations.