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Testing and Analysis of MOSFET-Based Absorber Integrated Antenna for 5G/WiMAX/WLAN Applications

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Abstract: A 3D electromagnetic circuit design and analysis of a MOSFET-based absorber active integrated antenna has been performed. It integrates a transmitting dual-band double material substrate (DMS) cylindrical surrounding patch antenna (CSPA) with a MOSFET-based absorber of reflected radio frequency power. It is a solution to the problem of performance degradation in the power amplifier (PA) resulting from antenna and PA impedance mismatch. This fully integrated MOSFET-based absorber antenna can absorb reflected RF power with a diode-based quasi-circulator as part of the integrated design circuitry. The antenna used for the proposed integrated design will operate at frequencies ranging from 2 GHz to 3 GHz and from 4.6 GHz to 6.1 GHz, thus providing a bandwidth of 1 GHz and 1.5 GHz at a resonance frequency of 2.5 GHz and 5.3 GHz, respectively. This makes it suitable for use in lower and upper bands of WLAN/WiMAX medium RF front-end applications. Furthermore, the condition for MOSFET connected to the absorber (I_S ≤ I_D and V_DS = 0) has been satisfied at both instances of resonance. In this proposed design, an antenna radiation efficiency of 84% has been observed.

Keywords: absorber; antenna; circulator; MOSFET; pulse generator; microelectronics; solid-state electronics

1. Introduction

The fast expansion of wireless and mobile communication sectors places significant demands on RF front-end systems that are small in size and high in efficiency [1–5]. While trying to meet these demands, there are numerous challenges, especially during the design stage of these systems [6,7]. These challenges have been solved with the introduction of active integrated designs. Active antennas became an intriguing study topic because of advancements in Microwave Integrated Circuit (MIC) technology.

The use of active antenna arrays in mobile communication and beam control has solved the channel capacity limitation problems by increasing the data rate. The advancement of smart antennas is just one of the many advantages of incorporating an active device into a passive antenna. Other benefits include increasing the effective length of short antennas, increasing the bandwidth, improving the noise factor, impedance matching, and increasing receiver antenna sensitivity. One such integrated design is the active integrated antenna (AlA), a novel technology that combines microstrip antennas with active solid-state electronics and microwave components to provide a variety of useful functionalities [8–12]. Integrated antenna design has been introduced to improve the efficiency of front-end systems and exists in recent times in the form of filtering antennas, rectifying antennas, power amplifier antennas, and low noise amplifier (LNA) antennas [13–17].

Compact fifth-mode and eighth-mode balanced substrate integrated waveguide (SIW) band-pass filters for 39 GHz were constructed and evaluated by Mutepfe and Srivastava [18,19]. A third-order SIW filter/antenna was designed and presented by Lovato et al. [20]; the filter/antenna comprises two cavity resonators, one of which has a slot antenna. The
slot antenna maintains the radiation characteristics of the antenna while the excitation of two modes in the slot cavity produces a third-order filtering response. The integrated filter/antenna design had a center frequency of 3.71 GHz, 8.29% fractional bandwidth, and an antenna gain of 5.10 dBi. Huitema et al. [21] presented a miniaturization approach to designing. The initial stage in this concept was to reduce the size of a cavity filter while maintaining a high-quality factor for reduced insertion loss. A second-order filter was used to achieve down sizing by combining a high dielectric permittivity ceramic with a capacitive effect induced by inserting a post in the center of each resonator. Even when the load was greater than 50, the filter performance was maintained.

Additionally, Ji et al. [22] created a ring-type filtering patch antenna that combines a ring patch and a dual-mode microstrip ring resonator. Within the pass-band, two patch modes were created, and two radiation nulls were formed on both sides of the pass-band. This integrated design reduced the overall size and power loss of the front-end system. From the experiment, the max gain of the proposed filtering antenna was above 10 dBi. Wu et al. [23] developed a wideband circularly polarized filtering patch antenna with three minima in the axial ratio response. In that arrangement, the patch antenna was processed in the same manner as the output port and final resonator of the filter network. In a far-field study, the amplitude and phase responses of a circular polarized (CP) wave were mapped to its axial ratio (AR). An 8.8% AR bandwidth was attained on a low profile of 0.028 λ, and the resultant gain demonstrated strong filtering characteristics.

Furthermore, for the operating frequency of 1575.42 MHz of the GPS band, a microstrip antenna with a low noise amplifier was designed by Rusdiyanto et al. [24]. This consists of a single passive antenna and an LNA. According to the simulation, it had a gain of 28.4 dBi; however, the measured gain was 14.77 dBi. The simulation yielded a circular polarization bandwidth of 60 MHz, while the experiment yielded 25 MHz. The operating frequency had a measured return loss of −23.42 dB and impedance bandwidth of 90 MHz. Li et al. [25] created an E-band high-linearity multi-feed antenna LNA front-end with a 45 nm CMOS SOI technology to investigate antenna electronics. This technology supports wireless backhaul and vehicle radar systems. This design takes advantage of antenna noise cancellation and power division to improve the E-band RX Noise Figure (NF) and linearity achievable in silicon front-ends. It was made possible by the high-resistivity silicon substrate employed in it.

Martin et al. [26] designed an LNA and dipole antenna. The LNA has a two-stage cascode based on a SiGe:C HBT with a 130 nm wavelength designed for maximum gain. At 80 GHz, the circuit is designed for vehicle radar applications. The co-integrated LNA measurement results again reveal NFs of 26 dB and 5 dB, respectively, with a 20 mW power consumption, whereas the antenna exhibits a simulated gain of 0 dB. Using 0.13 m SiGe bipolar complementary metal oxide semiconductor (BiCMOS) technology, a W-band power amplifier (PA) with a dipole antenna was co-designed by Demirel et al. [27]. The co-design enables direct connections between the PA and the transmitter (Tx) antenna, obviating the need for a matching network between the two blocks and allowing for loss reduction, increased energy efficiency, and downsizing. The monolithic integrated circuit (IC) design and measured results were presented. The maximum output power of the 79 GHz differential PA was 17 dBm. With a 1.8 V supply voltage, the chip consumes 300 mA. In the forward direction, the dipole antenna had a gain of −14 dBi, while in the backward direction, it had a gain of −8.5 dBi.

A collaborative design strategy for a co-integrated antenna and PA was provided by Iupikov et al. [28]. This design includes a band-pass RF filter and uses a high-efficiency Doherty PA architecture. After the simulation experiment, a 9% fractional bandwidth (300 MHz) with PAE at the 6 dB output power backed-off level that ranges between 50% and 55% was realized. Similar research work on integrated designs is presented in [29–33]. However, these designed integrated PA antenna structures do not consider the adverse effects of mismatching between the antenna and the PA used in their co-design...
methodology. One of such effects is arching within the PA structure, which results in PA performance degradation.

In this present research work, a novel MOSFET-based absorbing antenna was designed with a diode-based quasi-circulator as part of its circuitry. This device can be directly connected to the power amplifier without the need for a matching circuit. This design is aimed to reduce the 50 Ω impedance matching limitation on both the PA and the proposed DMS antenna of Omoru and Srivastava [34]. On the PA side, the co-design eliminates the challenges of the RF front-end system during matching circuits and eliminates most of the integrated passive parts that serve as a matching circuit. In addition, the rectified reflected power at the MOSFET terminal of the proposed antenna could be amplified and used for low-power operations within the RF front-end system. This paper is organized as follows. Section 2 presents the design of the antenna used for the proposed design. Section 3 shows the design of the MOSFET-based absorber, circulator, and pulse generator used for this antenna. Section 4 presents the design methodology of the antenna. Finally, Section 5 concludes the work and recommends future aspects.

2. Double Material Substrate (DMS) Cylindrical Surrounding Patch Antenna (CSPA) Design and Analysis

The DMS CSPA was designed using a combination of polyimide substrate and FR-4 substrate with dielectric constants of 3.5 and 4.3, respectively, as in previous work [34]. In continuation of this proposed co-design, the dimensions of the cylindrical patch antenna were altered on purpose by reducing the thickness of the polyimide substrate from 2 mm to 0.5 mm, thus reducing the overall dimension and increasing the bandwidth of the antenna. The revised dimension of the antenna used in the proposed MOSFET-based absorber antenna design is shown in Figure 1 and its parameters are given in Table 1. The adopted modeling, algorithm, and 2D radiation pattern for the cylindrical surrounding patch antenna used in the proposed integrated design have been explained in our previous works [34–36].

As shown in Figure 2, the thinner polyimide substrate caused the lower and upper bands of the WiLAN and WiMax frequency bands to move their backward resonance frequencies from 2.68 GHz to 2.37 GHz and from 5.55 GHz to 5.3 GHz, respectively. In addition, there is an increasing change in return loss from −26 dB to −19.5 dB and from −16 dB to −14.5 dB in the lower and upper bands, respectively. These values may not be practical for the physical implementation of the proposed design, but an increase in return loss values at both resonance frequencies has been observed to be advantageous in terms of providing the needed reflected power for the MOSFET-based absorber in the proposed circuitry.
Table 1. Parameters used for CSPA modeling.

| Description                                      | Parameter | Value (in mm) |
|-------------------------------------------------|-----------|---------------|
| The outer radius of ground                      | \( R_{go} \) | 12.12         |
| Inner radius of ground                          | \( R_{gi} \) | 11.32         |
| Outer radius of the polyimide substrate         | \( R_{so.pl} \) | 12.62         |
| Outer radius of FR-4 substrate                  | \( R_{so.fr-4} \) | 15.42         |
| Length of ground                                | \( L_{g} \) | 22.87         |
| Length of substrate                             | \( L_s \) | 39.84         |
| Substrate and patch top difference              | \( \Delta L \) | 2.070         |
| Inset feed length                               | \( Y_0 \) | 3.11          |
| Width of feed                                   | \( W_f \) | 5.70          |
| Height of patch                                 | \( H_p \) | 0.8           |
| Length of patch                                 | \( L_p \) | 11.04         |
| Width of patch                                  | \( W_p \) | 17.26         |
| Assumed width of the ground                     | \( W_g \) | 46.06         |
| Thickness of ground                             | \( H_g \) | 0.8           |
| Thickness of polyimide substrate                | \( H_{s.pl} \) | 2.0          |
| Thickness of FR-4 substrate                     | \( H_{s.fr-4} \) | 2.8          |
| Effective length                                | \( L_{eff} \) | 15.27         |

Figure 2. Return loss and equivalent bandwidth at both resonance frequencies using polyimide substrate of thickness 0.5 mm and 2 mm.

Before the dimensions of the antenna used for the proposed MOSFET-based absorber active integrated antenna design were altered, a bandwidth of 0.7 GHz (2.28 GHz to 3 GHz) and 1.1 GHz (4.9 GHz to 6.1 GHz) was observed for the lower and upper bands, respectively. Now, using a polyimide value of thickness 0.5 mm resulted in an increased bandwidth of 1 GHz (2 GHz to 3 GHz) and 1.5 GHz (4.6 GHz to 6.1 GHz) for the lower and upper bands, respectively.

Considering the directivity and gain values presented in Figures 3 and 4, the antenna efficiency factor \( K \) and radiation efficiency of the DMS antenna are computed as:

\[
G = KD
\]

\[
\text{Radiation efficiency} = \frac{G}{D} \times 100
\]
The dimensionless antenna efficiency factor $K$ must meet the maximum performance requirement of $0 \leq K \leq 1$, where $G$ and $D$ stand for gain and directivity, respectively [37,38]. A lossless antenna is represented by a value of $K = 1$. In addition, as shown in Figures 3 and 4, the benefit is never greater than the directivity ($D$) in practice. Now that $G$ and $D$ values have been input into Equation (1), $K$ has been determined to be equal to 0.843 and 0.848, corresponding to radiation efficiencies of 84.3% and 84.8% for the lower and upper bands, respectively. It has been noted that the computed value of $K$ for the antenna design satisfies the maximum performance criteria of $0 \leq K \leq 1$. Additionally, the DMS CSPA antenna displayed a radiation efficiency of 81% in both bands prior to changing its dimension.

From the gain vs frequency plot presented in Figure 5, it has been observed that there is an increase in gain value as frequency increases from the lowest frequency (2 GHz) of the

Figure 3. Far-field 3D radiation pattern at 5.3 GHz. (a) Directivity value of 6.15 dBi and (b) gain value of 5.2 dBi.

Figure 4. Far-field 3D-radiation pattern at 2.5 GHz. (a) Directivity value of 3.35 dBi and (b) gain value of 2.83 dBi.
lower band to the highest frequency (6.1 GHz) of the high band. In essence, this antenna has been excited by the microwave port for testing and experimentation purposes. One of the main benefits of the suggested design is the reasonably small size that results from the combination of FR-4 and polyimide substrate [34,36]. This antenna design, whose front view is depicted in Figure 6, addresses the issue of device fitting and dimension accuracy during manufacture. This advancement will be helpful in the 5G frequency band, where mobile devices now require a smaller antenna to transmit and receive information.

Figure 5. Gain vs frequency plot at both resonance frequencies.

Figure 6. DMS cylindrical patch antenna.

3. Design Analysis of SRD Pulse Generator and Diode-Based Quasi-Circulator

To aid the designed model for power amplifier simulation, the SRD pulse generator was used, which provides the required circulator’s incident RF power. In this section, a transient of the pulse generator and a diode-based three-port circulator are presented.

3.1. Transient 3D Electromagnetic Circuit Simulation of SRD Pulse Generator

At the prototype design level, there are several techniques for producing wide band pulses [39,40]. Avalanche transistors, tunnel diodes, non-linear transmission lines (NLTLs), photoconductive switches, bipolar transistors, field-effect transistors (FETs), and step recovery diodes (SRDs) are some examples [41]. The pulse generator used in place of the low noise amplifier is made up of a coplanar waveguide layout that includes a helical coil, two lumped capacitors, and a step-recovery diode (SRD). A sinusoidal signal has been used to exit the pulse generator through port-1, thus passing through a low-pass filter (capacitor C$_2$ and helical coil) and reaching an SRD connected in parallel with capacitor C$_3$. The SRD’s strong nonlinearity produces a very sharp peak, further filtered at the output by a DC blocking capacitor (C$_1$), thus producing a signal output at port-2.

In Figure 7, the values of capacitors C$_1$, C$_2$, and C$_3$ and inductors L$_1$ and L$_2$ are 15 pF, 68 pF, 0.35 pF, 0.6 nH, and 0.6 nH, respectively. A maximum frequency of 6 GHz has been defined in both the 3D project and the schematic’s transient tasks to resolve the expected high-frequency material properly. Probes P1 and P2 have been used to record the input and output voltage and current signals at the desired frequency. From Figure 8, the input the peak voltage and current at port-1 or Probe P1 are 2.5 V and 0.269 A, respectively, signifying a total input power of 0.66 Watts, and values are shown in Table 2.
Figure 7. SRD pulse generator used to provide the equivalent incident power for proposed active antenna integrated design testing.

Figure 8. SRD pulse generator time-domain input and output. (a) Voltage; (b) current.

Table 2. Equivalent voltage, current, and power at the input and output terminal of the pulse generator.

|        | Voltage | Current | Power   |
|--------|---------|---------|---------|
| P1     | 2500 mV | 263 mA  | 660 mW  |
| P2     | 2500 mV | 26.9 mA | 67 mW   |

3.2. The 3D Electromagnetic Circuit Simulation of 3-Port Diode-Based Quasi-Circulator Using Directional Couplers

A simplified form of a circulator, a quasi-circulator carries a signal from port-1 to port-2, from port-2 to port-3, and from port-3 to port-1. During this process, one of the ports is isolated; thus, no signal is transmitted to the isolated port. The quasi-circulator has been widely employed as a duplexer in various front-end modules of communication and radar systems, allowing the isolation of different sections within the front-end communication systems [42–45]. The novel diode-based quasi-circulator model used in the proposed MOSFET-based absorber active integrated antenna was designed with directional couplers, high-frequency Schottky diodes, and resistors. In Figure 9, a schematic depiction of a
A three-port active diode-based quasi-circulator is shown and detailed using unilateral power divider/combiner and diode characteristics.

![Three-port active diode-based quasi-circulator](image)

**Figure 9.** Three-port active diode-based quasi-circulator.

Considering the three-port quasi-circulator presented in Figure 8, signals incident on port-1(1) of directional coupler DC1 (port-1 of circulator) are coupled almost in equal shares to the two opposite ports 2(1) and 2(2). At this stage, diode 1 (DIODE 1) is ON while diode 2 (DIODE 2) is OFF. Since DIODE 2 is OFF, signals incident on port-1(1) of directional coupler DC1 will be allowed exit port-2(1), flowing through DIODE 1 to port-1(1) of directional coupler DC2. When the signals reach port-1(1) of directional coupler DC2, the signals are also coupled in almost equal shares to the two opposite ports, ports 2(1) and 2(2). In port-2(2), the signal is matched to a 50 Ω resistor $R_1$, thus allowing the signal to flow through port-2(1) of directional coupler DC2 (port-2 of the circulator). This configuration isolates port-3 of the circulator. A similar process occurs when the signal enters at ports-2 and -3, and then we have an active circulator, as shown in Figure 9.

To test the functionality of the designed diode-based quasi-circulator in terms of power routing capability, the output power from port-2 of the pulse generator presented in Section 3.1 is connected to port-1 of the designed circulator, and peak current and voltage values at each port of the circulator are shown in Figure 10a,b, respectively. Table 3 presents each port’s current, voltage, and power values. It has been observed that more than half of the power incident on port-1 of the circulator is transferred to port-2. Moreover, port-3 is almost fully isolated with an output power of 192 mW, which is minimal compared to the power incident on port-1.

![Current and Voltage](image)

**Figure 10.** Diode-based quasi-circulator port. (a) Current and (b) voltage.
### Table 3. Circulator port parameters.

| Ports | Current (mA) | Voltage (mV) | Power (mW) |
|-------|-------------|-------------|------------|
| 1     | 26.9        | 2623        | 70,559     |
| 2     | 18.9        | 2100        | 39,690     |
| 3     | 0.8         | 240         | 192        |

#### 4. Electromagnetic Circuit Simulation Analysis of MOSFET-Based Absorber Integrated Antenna

The absorbers are classified as broadband absorbers or narrowband absorbers [46,47]. Broadband absorbers work across a large frequency range, but typically exhibit low levels of attenuation, whereas narrowband absorbers work well over a smaller frequency range but exhibit high levels of attenuation [48]. Hu et al. [49] developed a novel downsized absorber frequency selective surface for low-frequency transmission/high-frequency absorption. In this instance, the lower layer’s selection zone of the symmetrical frequency was below 1.8 GHz, and the wave transmission rate was more than 84%. A wave-absorbing frequency selective surface (AFSS) with low-frequency transmission and high-frequency absorption was proposed by Han et al. [50]. To prevent the frequency selection feature from affecting the microwave absorption effect, the unit uses a method that loads the frequency selection structure proportionally to the absorber’s reflective metal surface.

The suggested model offered more than 10 dB insertion loss between 4 GHz and 5.5 GHz. Saikia et al. [51] designed and optimized an absorber design for the C-band using equivalent circuit analysis. Capacitive and analog circuit layers with lumped resistors make up the design. The entire wave simulation of the constructed microwave absorber displays a bandwidth of below $-10$ dB absorption from 4.23 GHz to 8.13 GHz. Although most absorbers are foam absorbers, depending on the frequency needed and the level of absorption they can deliver, they could also be analog circuits [52].

For a MOSFET-based absorber design, it is vital to know the amount of predicted reflected power from the antenna branch of the proposed MOSFET-based antenna design. Knowledge of the peak and RMS values of current, voltage, and power will enable engineers to analyze the proper values of resistors, capacitors, and inductors (resistor inductor–capacitor filter) for the MOSFET-based absorber design [53]. To compute these values, port-1 of the circulator presented in Section 2 is connected to the SRD pulse generator’s output, and port-2 of the circulator is connected to the DMS dual-band antenna. After carrying out a transient 3D EM/co-simulation of the connected device, the reflected peak current and peak voltage from the antenna branch are observed at port-3, with values of 4.36 mA and 722 mV, respectively, as shown in Figure 11a,b.

![Figure 11(a)](image1.png)  ![Figure 11(b)](image2.png)

**Figure 11.** Circulator port after antenna attachment. (a) Current and (b) voltage.
Equations (3) through (12) have been adopted from the existing literature [3,53–57]:

\[ V_{\text{rms}} = V_{\text{peak}} \times 0.707 \]  
(3)

\[ V_{\text{DC}} = \frac{2V_{\text{peak}}}{\pi} \]  
(4)

\[ I_{\text{rms}} = 0.707 \times I_{\text{peak}} \]  
(5)

\[ I_{\text{DC}} = \frac{2I_{\text{peak}}}{\pi} \]  
(6)

Using Equations (3) and (6), the rms and DC values of reflected current and voltage signals have been computed as \( V_{\text{rms}} \) (495 mV), \( I_{\text{rms}} \) (3.08 mA), \( V_{\text{DC}} \) (446 mV), and \( I_{\text{DC}} \) (2.8 mA). In addition, the ripple factor and impedance of the inductor \( (X_L) \) and capacitor \( (X_C) \) influence the capacitor and inductor values required for the MOSFET absorber design. The ripple factor, the impedance of the inductor, and the impedance of the capacitor are defined as:

\[ \text{RippleFactor} = \sqrt{I_{\text{rms}}^2 - I_{\text{DC}}^2} \]  
(7)

\[ X_L = \frac{V_{\text{peak}}}{I_{\text{rms}}} \]  
(8)

\[ X_C = \sqrt{\frac{3X_L \times \text{Ripple factor}}{2}} \]  
(9)

The ripple factor increases to 0.46 when these values for \( I_{\text{rms}} \) and \( I_{\text{DC}} \) are substituted into Equation (7). Additionally, 227 \( \Omega \) and 14 \( \Omega \) were calculated as the respective impedances of the inductor and capacitor. Regarding the design frequency, 6 GHz was chosen for the MOSFET-based absorber. Values of inductors and capacitors for the MOSFET-based absorber can be computed as:

\[ L = \frac{X_L}{2\pi f} \]  
(10)

\[ C = \frac{1}{2\pi f X_C} \]  
(11)

The values of the inductor \( (L) \) and capacitor \( (C_4 \text{ and } C_5) \) were calculated as 8 nH and 2.5 pF, respectively. The load resistor \( (R_2) \) used in the MOSFET-based absorber was computed as a function of the voltage and current component of the peak reflected power, as shown in Equation (12), and the value is 157 k\( \Omega \).

\[ R = \frac{V_{\text{peak}}}{I_{\text{Peak}}} \]  
(12)

The MOSFET-based absorber schematic is presented in Figure 12. In order to complete the rectification process while taking into account the ON and OFF states of the diodes and the potentials at each node of the rectifier, it has been demonstrated that the absorber is a combination of an RLC filter, an N-channel MOSFET, and a four-diode combination [55–57]. The function of the RLC filter, in this case, is to reduce the pulses at the output of the rectifier; this allows for maximum performance of the MOSFET device in the absorber. To turn ON the MOSFET, a DC voltage \( (V_G) \) of 12 V is applied to the MOSFET gate, thus allowing the flow of the current from the drain to the source.
Figure 12. Designed MOSFET-based absorber.

Figure 13 shows the 3D EM/circuit co-simulation schematic of the integrated SiO$_2$ MOSFET-based absorber and dual-band double-material substrate CSPA. To run the co-simulated schematic, the output of the pulse generator was connected to port-1 of the presented schematic (Figure 13). The reflected power resulting from the mismatch between the pulse generator (PA) and the DMS CSPA is rectified, filtered, and observed at P11 (drain terminal of the MOSFET) and P10 (source terminal of the MOSFET). In the proposed MOSFET-based absorber integrated antenna model, reflection is bound to occur from the antenna branch (port-2) under two MOSFET source current ($I_S$) operation conditions. The condition for MOSFET absorption has been used from Refs. [53–56].

Figure 13. Proposed MOSFET-based absorber integrated antenna.
After running a transient simulation on the presented schematic of the MOSFET-based absorber antenna, the drain voltage and current were observed as in Figure 14. Considering the proposed antenna, the MOSFET-based absorber serves its purpose of absorbing the reflected signal from the antenna branch of the circulator, if the relationships $I_S \leq I_D$ (current at P10 greater than or equal to current at P11) and $V_{DS} = 0$ (voltage at P10 equal to 0) are justified. When these conditions are satisfied, adverse effects (such as arching within the transmission line or signal route within the circulator) are eliminated from a mismatch between the PA and the antenna.

![Figure 14. Drain/source (a) voltage and (b) current.](image)

From Table 4, it is observed that the condition for MOSFET absorption is satisfied for the designed antenna (source voltage is 0 and the source current is negative compared to the drain current, implying a condition of $I_S \leq I_D$).

**Table 4. MOSFET drain and source terminal parameters.**

| Terminal    | Voltage (mV) | Current (mA) |
|-------------|--------------|--------------|
| Source (P11)| 0            | −3.6         |
| Drain (P10) | 466          | 3.6          |

5. Conclusion and Future Recommendations

The 3D EM/circuit co-simulation of the MOSFET-based absorber integrated antenna has been observed to have a suitable reflection absorbing capability by satisfying the condition for MOSFET absorption. This device, when directly connected to the power amplifier’s output, reduces the effect of impedance mismatch between the PA and the antenna because the reflected power that would have resulted in arching within the PA structure is absorbed by the MOSFET absorber in the antenna construct. Another advantage of this design is that the model can function as a rectifying antenna for energy harvesting. Furthermore, the dual material antenna used in the proposed integrated design was designed to resonate at 2.5 GHz (2 GHz~3 GHz) and 5.3 GHz (4.6 GHz~6.1 GHz), hence making it suitable for the lower and upper bands of WLAN and WiMAX and the middle band of 5G technology (2.3 GHz to 2.4 GHz and 2.5 GHz to 2.69 GHz). This antenna design can be used in the front end of communication systems, signal intelligence systems, and other forms of transportation (intelligence, surveillance, and reconnaissance) systems.

As a continuation of this work, we will present a block-by-block performance analysis of the proposed model to validate the usability of the 3D electromagnetic circuit simulation design in the 5G regime. Thereafter, a fabricated device will be realized.
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