SUPPLY NOISE REDUCTION VERIFICATION IN PRE-LAYOUT AND POST-LAYOUT STAGES FOR SYSTEM-ON-CHIP

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Abstract

This paper deals with accurate decoupling capacitance estimation which is commonly used for suppression of power supply noise in modern day system-on-chip. Supply noise is a major issue needs to be addressed for proper functioning which may lead to logic failure in digital integrated circuit. Capacitors directly effects the power consumption and delay parameters and hence the overall performance of integrated circuits. In this work design verification has been done between the pre-layout stage and post-layout stage. Simulation results show that the difference in results between pre-layout and post-layout stages is marginal. This early detection of errors can be helpful for the designers in the latter stages of the system design. This CAD flow can also be used on any system-on-chip design.

Keywords: Computer Aided Design (CAD), Decoupling capacitor (decap), Power Distribution Network (PDN), System-on-chip (SoC), White Space (WS).

I. Introduction

In system-on-chip, scaling down of transistor feature size and the design of efficient electrical distribution networks is a major challenge. Enhancing the throughput current is as significant as decreasing the power area, as well as importance in several portable devices. Power emission is a major concern in today’s system-on-chip. Modern day power distribution network (PDN) is expected to supply...
power having very less or no voltage fluctuations and thus optimizing the supply noise. This reduced noise voltage can guarantee proper and improved functioning of the integrated circuit [I], [II], [III], [IV], [V], [XIII].

Previous research work shows that supply noise can be reduced substantially by V inserting decoupling capacitors [VI], [VII], [VIII], [IX], [XI]. However increase in decap may result in critical issues in VLSI design processes, such as rise in leakage current and overall performance of the chip. Also chances of P/G short-circuit goes up with increase in decap budget hence it is necessary to optimize the decap budget in sub-micron design processes [X], [XII], [XIV].

The rest of the paper has been presented as follows: decoupling capacitance estimation has been briefly discussed in section II. Decap placement and CAD approach for this work has been discussed in section III. Section IV presents overall CAD approach and simulation results for design verification. In section V the paper has been concluded.

II. Decoupling Capacitance Estimation

The voltage variation in various electrical nodes is termed as supply noise. There are various sources of supply noise like inductive resistive and switching activity of transistors. Inductive voltage drop occurs in the pads given as [VIII]:

\[ V_L = \frac{L}{d} \frac{dI}{dt} \] (1)

Resistive voltage drops occurs due to internal resistance in electrical wires expressed as [VIII]:

\[ V_R = I.R \] (2)

In this work we have used module-wise approach using SOS algorithm for decap estimation. The focus of this work is the reduction of supply noise with a focus to keep the various design parameters within acceptable limits as excess decap degrades the chip performance i.e. power and delay parameters. Authors have suggested the noise voltage can be reduced approximately by 50% having a decap budget as in article [IV]:

\[ C = \frac{P}{V_{DD}^2} \] (3)

Where \( C \) = decap budget, \( P \) = power consumption of the SoC, and \( V_{DD} \) = supply voltage.

III. Decoupling Capacitance Allocation

An efficient PDN is a very important aspect in the overall manufacturing
process of a chip as it directly effects performance and cost function of the chip. Detection of faults at an early stage has to be done since rectification of errors is very difficult in the latter stages of the design and it is cost effective.

Generally decaps are placed wherever WS is available for suppression of supply noise. But these do not guarantee that the noise will be suppressed significantly without effecting the overall performance of SoC. So more focus have to be given on supply noise analysis and this is a great challenge for the system designers. Initially blank spaces available in the initial floor plan were treated as white space (WS) spaces for placement of decaps. Previously decaps were placed wherever white space was available. But this does not guarantee that the supply noise will get optimized for all the modules. Decaps placed in the WS far away from the noisy functional module does not have much impact on suppression of noise of that particular module.

The problem for suppression of supply noise for modules where nearby WS is not available. So WS has to be created for placement of decaps for suppression of noise, but it increases the wiring length which in turn increases the overall cost function of the chip. The focus is to make best possible utilization of the WS so that the cost function is kept within permissible limits. Also the wiring length will get reduced which has considerable effect on the IR drop and RC delay parameter of the chip. The focus is on maximum utilization of the WS. Additional space has to be created for insertion of the decaps near the noisy modules. Another issue during layout stage is cost function of the chip. Cost function of integrated circuit can be expressed as [X]:

\[ \psi = A + \mu W \]  

(4)

Where A is area, W is wire length, and \( \mu \) is weight parameter. With insertion of decap there will be an increment in cost function and can be expressed as [X]:

\[ \psi = (A + \delta A) + \lambda (W + \delta W) \]  

(5)

The purpose is to optimize the WS so that there is minimum effect on cost function. Generally due to high packing density it is assumed that all the modules have certain amount of supply noise. These allocations of WS allow decaps to be placed nearby the noisy modules. This in turn assures to a significant extent the supply noise can be reduced. The overall area of the chip increases but it is a tradeoff scenario between the cost function and overall performance of the chip. In our algorithm, firstly noisy modules are identified. Secondly, availability of white space (WS) near the noisy module is checked. If WS is available near the noisy module the decaps are placed so that supply noise is reduced and increment in cost function can be optimized. Implementation of floor plan in such cases is a challenging task for the designers.
this work stimulated-annealing technique has been used as discussed in research article [X].

The CAD approach for decap placement is as follows:
(i) Initialize: Noise reduction and cost function without decap.
(ii) For each noisy module
(iii) Check availability of nearby WS.
(iv) Decap placement and check reduction of supply noise. Check various design parameters of the chip after decap placement and cost function.
(v) End.
(ix) For noisy modules where WS is unavailable.
(x) Do modification in physical design stage so that the noisy modules can be made adjacent without having much effect on other design issues. Here stimulated-annealing technique has been used.
(xi) Decap placement check the optimization of supply noise. Check various design parameters of the chip after decap placement and cost function.
(xii) If (results are satisfactory)
(xiii) End.
(xiv) Else
(xv) Continue iteration till termination.
(xvi) Output: Floor plan accepted.
(xvii) Stop.

IV. CAD Approach and Simulation Results

The CAD approach in this entire work is described hereunder:

/*Pre-layout Stage*/
1. Verilog code to develop the SoC and functional verification.
2. Netlist generated.
3. Modules are combined to form the SoC.
4. Estimation and allocation of decap for individual modules.
5. Supply noise reduction, propagation delay and power consumption is checked for each module.

6. Estimation of supply noise, propagation delay and power consumption for the entire SoC.

/* Post-layout*/

7. Physical design.

8. Estimation of supply noise, propagation delay, power consumption and cost function for SoC.

9. Results comparison between pre-layout and post-layout stages.

In this work FFT core of 512-point and 1024-point has been considered as test circuits. FFT cores are complex circuit's finds wide range of applications in today's digital communication systems. The architecture is shown in Fig.1. The FFT core consists of input, memory blocks, address generator, twiddle factor, butterfly and control unit. Results of intermediate stages and twiddle factors are stored in memory block. Address generation block and control blocks are for overall operation on the processor. CADENCE platform has been used for this work. This work is performed at 1V operating voltage with 1GHz switching frequency using TSMC 90 nm process technology.

![Architecture of FFT Core](image)

**Fig. 1:** Architecture of FFT Core [VIII]
Table 1: Analysis of Supply Noise Reduction

| FFT Length | Stages    | Without Decap Peak Noise (mV) | With Decap Peak Noise (mV) | % of Noise Suppression |
|------------|-----------|-------------------------------|--------------------------|-----------------------|
| 512        | Pre-layout| 0.55                          | 0.26                     | 52.7                  |
| 512        | Post-layout| 0.57                          | 0.28                     | 50.8                  |
| 1024       | Pre-layout| 0.59                          | 0.28                     | 52.5                  |
| 1024       | Post-layout| 0.61                          | 0.31                     | 49.2                  |

From table 1, optimization of supply noise for 512-point and 1024-point FFT cores has been presented. Simulation results are almost identical in both pre-layout stage and post-layout stage.

Table 2: Analysis of Power Consumption

| FFT Length | Stages    | Without Decap Power (mW) | With Decap Power (mW) | % increment Power |
|------------|-----------|--------------------------|-----------------------|------------------|
| 512        | Pre-layout| 151.5                    | 154.3                 | 1.85             |
| 512        | Post-layout| 152.9                    | 156.4                 | 2.28             |
| 1024       | Pre-layout| 206.2                    | 208.6                 | 1.16             |
| 1024       | Post-layout| 208.3                    | 211.5                 | 1.53             |

From table 2, power consumption for 512-point and 1024-point FFT cores has been presented. Simulation results are almost identical in both pre-layout stage and post-layout stage.
Table 3: Delay Analysis

| FFT Length | Stages    | Without decap Delay (µ Sec.) | With Decap Delay (µ Sec.) | % Delay increment |
|------------|-----------|-------------------------------|--------------------------|------------------|
| 512        | Pre-layout| 192.5                         | 194.8                    | 1.195            |
| 512        | Post-layout| 194.7                        | 198.5                    | 1.95             |
| 1024       | Pre-layout| 308.2                         | 312.5                    | 1.39             |
| 1024       | Post-layout| 311.7                        | 316.5                    | 1.54             |

From table 3, delay analysis for 512-point and 1024-point FFT cores has been presented. Simulation results shows that increment in delay are almost identical in both pre-layout stage and post-layout stage.

Table 4: Core Area Analysis

| FFT Length | Stages    | Core area Without decap | Core area With decap | % Area Increment |
|------------|-----------|-------------------------|----------------------|-----------------|
| 512        | Post-layout| 3.12 mm²               | 3.41 mm²             | 8.5             |
| 1024       | Post-layout| 4.84 mm²               | 5.26 mm²             | 7.98            |
| Reference II. | ------ | ------                 | ------               | 8.4             |

The core area analysis for this work has been presented in table 3. The area increment is 8.5% and 7.98% for 512-point FFT processor and 1024-point FFT processor respectively. The results are compared with reference II.

In this work simulation results have been compared between pre-layout stage and post-layout stage. Simulation results shows that the various design parameters are identical in both pre-layout and post-layout stages. From the simulation results it has been observed that the supply noise has been reduced significantly. Also from the simulation results it is observed that delay performance of this work is much improved compared to previous research work. The power consumption in this work has also been reduced significantly. Overall the various design parameters of this work for all the test circuits are satisfactory.
V. Conclusion

In this work a result comparison between pre-layout and post-layout stages has been done. The focus was detection of faults in the early stages of design process. The number of transistor count in modern day VLSI design has grown significantly. Propagation delay, power consumption and area are the major concerns for the VLSI designers. With very high packing density design and implementation of an efficient PDN is also becoming a challenging task. This leads to variation of voltages in the electrical nodes which results supply noise. Researches have focused on various techniques for reduction of supply noise as this noise may lead to logic failures and malfunctioning of the chip.

Future work will further focus on CAD approach using soft computing techniques so that the overall performance of the integrated circuit can be improved.

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References

I. C. Tirumurti, S. Kundu, S. Sur-Kolay, Y. Chang, “A modeling approach for addressing power supply switching noise related failures of integrated circuits”, Proceedings of Design, Automation and Test in Europe Conference and Exhibition (DATE) pp.: 1078-1083, 2004.

II. D. Kang, C. Yiran, K. Roy, “Power supply Noise-aware Scheduling and Allocation for DSP Synthesis”, Proceedings of Sixth International Symposium on Quality Electronic Design (ISQED’05), 2005.

III. K. Shah, “Power Grid Analysis in VLSI Designs”, Dissertation in Master of Science (Engineering), Super Computer Education and Research Centre, Indian Institute of Science Bangalore, 2007.

IV. K. Shimazaki, T. Okumura, “A Minimum Decap Allocation Technique Based on Simultaneous Switching for nano-scale SoC”. Proceedings of IEEE Custom Integrated Circuits Conference, 2009.

V. M. Khellah, D. Khalil, D. Somasekhar, Y. Ismail, T. Karnik, V. De, “Effect of power supply noise on SRAM dynamic stability”, Proceedings of Symposium on VLSI Circuits 2007.
VI M. Saint-Laurent, M. Swaminathan, “Impact of power-supply noise on timing in high frequency microprocessors”, IEEE Transactions on Advanced Packaging, Vol.:27, pp.: 135-144, 2004.

VII P. Mitra, J. Bhaumik, “Pre-Layout Decap Allocation for Noise suppression and Performance Analysis for 512-Point FFT core”, Proceedings of 2017 Devices for Integrated Circuits (DevIC), pp.: 341-345, 2017.

VIII P. Mitra, J. Bhaumik, “A CAD Approach for Suppression of Power Supply Noise and Performance Analysis of Some Multi-core Processors in Pre-layout Stage”, Microsystem Technologies, Springer, Vol.: 25, Issue: 5, pp.: 1977-1986, 2019.

IX S. Pant, “Design and analysis of Power Distribution Networks in VLSI Circuits”, Ph.D. Dissertation, University of Michigan, 2008.

X S. Zhao, K. Roy, C.K. Koh, “Decoupling Capacitance Allocation and Its Application to Power-Supply Noise-Aware Flooring”, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, Vol.: 21, Issue: 1, pp.: 81-92, 2002.

XI T.C. Hsueh, F. O'Mahony, M. Mansuri, B. Casper, “An On-Die All-Digital Power Supply Noise Analyzer with Enhanced Spectrum Measurements”, IEEE Journal of Solid-State Circuits, Vol.: 50, Issue: 7, pp.:1711-1721, 2015.

XII T. Karim, “On-Chip Power Supply Noise: Scaling, Suppression and Detection”, Ph.D. Dissertation, University of Waterloo, 2012.

XIII Y.L. Chuang, P.W. Lee, Y.W. Chang, “Voltage-Drop Aware Analytical Placement by Global Power Spreading for Mixed-Sized Circuits Design”, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, Vol.: 30, Issue: 11, pp. 1649-1662, 2011.

XIV Y. Shi, J. Xiong, C. Liu, L. He, “Efficient Decoupling Capacitance Budgeting Considering Operation and Process Variations”, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, Vol.: 27, Issue: 7, pp.: 1253-1263, 2008.