A Fully Digital Semirotational Frequency Detection Algorithm for Bang–Bang CDRs

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Abstract—This brief presents a new frequency acquisition method using a semirotational frequency detection (SRFD) algorithm for referenceless clock and data recovery (CDR) in a serial-link receiver. The proposed SRFD algorithm classifies the bang-bang phase detector (BBPD) outputs to estimate the current phase state and detects the frequency mismatch between the input data and the sampling clock. The voltage-controlled oscillator (VCO)-track path in a digital loop filter (DLF) enables online calibration of a drifted frequency of the VCO caused by temperature or voltage variation after a frequency acquisition. The proposed algorithm can be implemented as a digitally synthesized circuit, lowering design efforts for referenceless CDRs. A 10-Gb/s transceiver IC with the proposed algorithm, fabricated in a 65-nm CMOS process, demonstrates successful recovery of the input phase without any reference clock.

Index Terms—Frequency detector, referenceless clock and data recovery (CDR), serial links.

I. INTRODUCTION

In a high-speed serial communication system, various methods for detecting frequency information from input data have been proposed for cost reduction by eliminating an external reference clock source. A majority of those methods rely on flip-flops operating at a line rate for sampling multi-phase clock signals at the edge of input data, leading to design challenges in high-speed applications [1]–[6]. A 4× oversampling scheme for frequency detection is also disadvantageous as line rate 0.25UI-spaced multiphase clocks are vulnerable to phase mismatch caused by process–voltage–temperature (PVT) variations [7], [8]. Moreover, additional samplers increase the power consumption and the area occupancy of the receiver. A stochastic referenceless clock and data recovery (CDR) scheme requires line rate clock dividers and information on the input signal’s transition density, which limits its application flexibility [9]–[13]. There have been fully synthesizable digital algorithms for frequency detection [14], [17]. The frequency detector in [14] achieved good energy efficiency with the assistance of its simple algorithm. However, the voltage-controlled oscillator (VCO) has to start from the low frequency since the detection algorithm is not bidirectional. Another algorithm introduced in [17] requires a specific baud-rate CDR architecture limiting its application to conventional CDRs.

This brief proposes a new frequency detection algorithm by modifying the principles of the conventional rotational frequency detection (RFD) algorithm neither using 4× oversampling nor with any additional circuitries. This algorithm can be implemented with standard digital logic synthesis and automatic back-end design flow to reduce the design effort. Furthermore, its compatibility with conventional CDR architecture allows the proposed algorithm to be employed in a broad application range in wireline industries.

II. SEMIROTATIONAL FREQUENCY DETECTION ALGORITHM

Fig. 1 shows the operation principle of the proposed semi-RFD (SRFD) algorithm. An ideal bang–bang phase detector (BBPD) determines the up and down (UP and DN) signals based on the 0° and 180° phases of the input data. However, an actual BBPD has slightly different UP/DN criteria for each output for various reasons such as intersymbol interference (ISI) and voltage offset of the comparator. The proposed algorithm roughly classifies the actual BBPD output into two groups having different UP/DN criteria for each other. Those two UP/DN boundaries divide the phase diagram into more than three phase states. One BBPD output cannot specify the phase location of the current input data as one of these phase states. However, assuming that the phase of the input data does not change significantly during the phase-detection period, the current phase state can be estimated by combining successive outputs from two different BBPDs. For example, if “DN2” from the second group and “DN1” from the first group are output sequentially as shown in Fig. 1, the current phase state can be estimated as “S1.” Thus, the rotational direction of these estimated states shows the sign of the frequency error between the input data and the sampling clock. The digital algorithm outputs \( X = +1, -1, \text{ or } 0 \) depending on whether the estimated phase state rotates clockwise or counterclockwise, or stays in the same position, respectively. Then, the integrate-and-dump filter accumulates the algorithm output \( X \) to produce a single SRFD output \( Y \). The proposed frequency detection scheme is named SRFD, since it has a similar operation method to conventional RFDs, but with a different state estimation principle.

The rest of this brief is organized as follows. Section II introduces the underlying principles of the proposed algorithm and presents simulation results. The transceiver architecture and the circuit implementation for demonstrating the feasibility of the proposed algorithm are shown in Section III. Section IV presents the measured results and Section V concludes this brief.
Meanwhile, many different SRFD algorithms are also available depending on the way of classification of the BBPD output into two groups. The SRFD algorithm in this brief exploits the ISI of input data for grouping BBPD output as shown in Fig. 2. Due to ISI, the input data create multiple zero-crossing points at the edge phase, resulting in a data-dependent BBPD output. For example, the zero-crossing point moves forward or backward in time, depending on whether two consecutive bits before the edge are equal [15]. Thus, the two groups of BBPD output that are classified by the result of the exclusive-OR of two previous bits have different UP/DN criteria. The SRFD algorithm using this classification scheme is named dispersion-based SRFD. Previous research [17] also detects frequency information by using ISI of input data, but requires multilevel sampling of the input data. On the other hand, the proposed algorithm requires only the conventional BBPD output for its operation, hence it can be easily applied to the conventional CDR architecture widely employed by industries.

Fig. 3 shows MATLAB simulation results of two BBPD output groups when the input nonreturn to zero (NRZ) data pass through various channel loss models. As the input signal is more dispersed by ISI, the gain of both BBPD output groups decreases, while the difference between their UP/DN criteria increases. Fig. 4 shows the SRFD output Y under the same channel conditions in Fig. 3. In this simulation, the edge sampling period is set to 2UI and the integrate-and-dump filter adds L algorithm outputs to generate one SRFD output. The proposed SRFD algorithm successfully detects the sign of frequency error when there is a loss of about $-10 \text{ to } -15 \text{ dB}$ at the Nyquist frequency ($f_{Ny}$). The detection range of the dispersion-based SRFD is from $-22\%$ to $22\%$ regardless of the integration period of the filter. However, the longer period of the filter achieves more clear SRFD output Y with less noise.

It is worth noting that the proposed algorithm still detects the frequency information with eye diagrams from other channel models as well. It is because the two postcursor data prior to the edge predominantly determine the zero-crossing phase in most channel cases. Once such dependency holds, the proposed algorithm works regardless of the detailed shape of the eye diagram.

### III. Transceiver Architecture

Fig. 5 illustrates the architecture of a 10-Gb/s referenceless transceiver featuring the proposed SRFD algorithm. The RX consists of an analog front-end (AFE), six samplers for the quad-rate operation, a retimer, a demux, a phase rotator, and a synthesized digital core operating at a speed of 312.5 MHz. The digital core includes a variety of test algorithms for the dispersion-based SRFD and a digital loop filter (DLF). The dispersion-based SRFD operates in two modes; a coarse mode using two edges sampled at $\phi_1$ and $\phi_5$ has a wide capture range and a fine mode uses only one edge sampled at $\phi_1$ to avoid the frequency offset due to phase mismatch between $\phi_1$ and $\phi_5$.

In a high-speed link with the data rate above 25 Gb/s, a decision feedback equalizer (DFE) is an essential block since the continuous-time linear equalizer (CTLE) cannot fully equalize the severe channel loss. However, the DFE coefficients are typically set to zero before the CDR phase lock stage is completed [16]. Meanwhile, the proposed SRFD algorithm is turned off after the CDR phase is
Fig. 5. Block diagram of a 10-Gb/s referenceless transceiver.

Fig. 6. Block diagram of a CG and frequency acquisition steps.

locked. Therefore, the operation time of DFE and SRFD does not overlap, making two schemes compatible with each other. The CDR in this brief is only for proving the concept of the SRFD algorithm, and the DFE is not implemented to reduce the hardware complexity.

Fig. 6 summarizes the frequency acquisition procedure of the proposed scheme. The LC-VCO operating at 5 GHz employs a 6-bit MIM capacitor array and an 8-bit MOS capacitor array for coarse- and fine-frequency control, respectively. The operation sequence of the frequency acquisition is as follows. First, the DLF and the control bits of the VCO are initialized. The initial VCO frequency is set to a center frequency to maximize the frequency detection gain of the SRFD algorithm within the VCO tuning range. Second, the VCO frequency is coarsely tuned to the input data rate by using $2^7$ coarse SRFD output. Third, the $2^9$ fine SRFD output adjusts the VCO frequency to match the input data rate precisely. These coarse and fine tuning steps are repeated twice to cover all the VCO tuning range.

The required time for each acquisition step is estimated by the number of SRFD results and the period of the integrate-and-dump filter. Finally, the DLF is initiated for the phase lock. The total frequency lock time is 262.5 $\mu$s, regardless of the initial frequency error.

After recovering the input phase, the SRFD algorithm is turned off and an alternative feedback path is activated to maintain the VCO frequency within the pull-in-range under temperature and voltage variations. Even though the second-order DLF tracks the frequency offset between the input data rate and the sampling clock, the stepwise operation of a rotator-based CDR degrades the jitter and bit error rate (BER) performance under a large frequency offset. Therefore, in case the input value of the second-order path exceeds the predefined threshold, the VCO-track path is activated to directly control the VCO frequency by generating the $UP_{F}/DN_{F}$ signal for the compensation of the slow frequency drift. The update period of $UP_{F}/DN_{F}$ is set to 100 $\mu$s, since the slow on-line calibration of VCO frequency does not interfere with the CDR operation.

IV. MEASUREMENT RESULTS

Fig. 7 shows the open-loop output $Y$ of the dispersion-based SRFD tested using PRBS31 NRZ data. The period of the integrate-and-dump filter is extended to 13.4 ms for filtering the noise at open-loop output results and obtaining a clear relation between the frequency error and the output of the proposed algorithm. The first setup measures the SRFD output $Y$ over a 25% frequency range by sweeping the input
Table I

| Data rate(Gbps) | [7] | [2] | [4] | [13] | [17] | this work |
|----------------|-----|-----|-----|------|------|-----------|
| Process(nm)    | 10  | 20  | 10  | 10   | 32   | 40        |
| PD Type        | PFD | DQPD| CPS | SRCG | Voltage-based | SRFD     |
| PD power(mW)   | 42.2| 25  | 11  | 8    | -    | 9.3       |
| PD area(μm²)   | -   | -   | -   | -    | 49000| -         |
| PD range(%)    | -   | -   | -   | -    | 39   | 44        |
| PD Design      | custom | custom | custom | Digital synthesis | Digital synthesis |
| channel loss(dB) | -  | 7.0 | -   | 14.8 | 12.5 |
| Frequency acquisation time | - | - | - | - | 202ns |
| FOM(Lfiq, pJ/Gb) | 6.55 | 2.45 | 5.525 | 3.19* | 13.8 |

*PFD power included

V. Conclusion

This brief introduced a new frequency acquisition method using the SRFD algorithm for referenceless CDRs. SRFD estimates the phase state of input data using BBPD output with two different phase criteria and detects frequency error between input data and the sampling clock. After the frequency acquisition step, the VCO-track path in DLF keeps the VCO frequency within the locking range of the CDR, regardless of temperature or voltage variation. All of these algorithms can be implemented as synthesized digital blocks without between 29°C and 53°C to validate the operation of the VCO-track path. The VCO without feedback from the VCO-track path shifts the frequency by $-1500$ ppm at 53°C and results in a significant increase in BER. However, when the VCO-track path is turned on, the VCO frequency remains constant without any bit error being detected.

The RX digital core consists of a BBPD, a DLF, an SRFD, and other diverse logic blocks for the test. The measured power consumption of the RX digital core with a retimer and a demux is 34.1 mW under 1.2-V supply for a 10-Gb/s data rate. Since the power consumption of the retimer and the demux is 9.6 mW according to the postlayout simulation, the expected power consumption of the RX digital core is 24.5 mW. The power and the area of the dispersion-based SRFD algorithm estimated by the equivalent gate count ratio are 9.3 mW and 48 900 μm², respectively. The SRFD transceiver including the clock generator (CG) consumes 193.2 mW. The chip photo fabricated in 65-nm CMOS is shown in Fig. 10. Table I compares the proposed SRFD algorithm with other frequency detection methods.
additional analog circuitry, having significantly lower design efforts than other referenceless CDR design based on analog circuits. The 10-Gb/s transceiver including proposed algorithms is implemented in a 65-nm CMOS process. The measured results demonstrate the feasibility of the proposed algorithm with a detection range from $-22\%$ to $22\%$.

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