Variability aware Golden Reference Free methodology for Hardware Trojan Detection Using Robust Delay Analysis

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Abstract Many fabless semiconductor companies outsource their designs to third-party fabrication houses. As trustworthiness of chain after outsourcing including fabrication houses is not established, any adversary in between, with malicious intent may tamper the design by inserting Hardware Trojans (HTs). Detection of such HTs is of utmost importance to assure the trust and integrity of the chips. However, the efficiency of detection techniques based on side-channel analysis is largely affected by process variations. In this paper, a methodology for detecting HTs by analyzing the delays of topologically symmetric paths is proposed. The proposed technique, rather than depending on golden ICs as a reference for HT detection, employs the concept of self-referencing. In this work, the fact that delays of topologically symmetric paths in an IC will be affected similarly by process variations is exploited. A procedure to chose topologically symmetric paths that are minimally affected by process variations is presented. Further, a technique is proposed to create topologically symmetric paths by inserting extra logic gates if such paths do not exist in the design intrinsically. Simulations performed on ISCAS-85 benchmarks establish that the proposed method is able to achieve a true positive rate of 100% with a false positive rate less than 3%. In our experimentation, We have considered the maximum of 15% intra-die and 20% inter-die variations in threshold voltage ($V_{th}$).

Keywords Hardware Trojan detection · Self-referencing · Process variation · Path delay

1 Introduction

Area, power, and performance have been major concerns for integrated circuit (IC) designers traditionally, whereas the security aspects of ICs have now gained a lot of significance. In the present scenario, the semiconductor industry has adopted a horizontal business model to reduce time-to-market and stay competitive. In such a production model, the IC manufacturing process is spread over the globe and involves many third-party design and fabrication houses. The trustworthiness of such design and fabrication houses is not established. Thus, the security of these chips has become a major concern for system designers and gained the interest of many researchers in recent years. Hardware Trojan (HT) is one such threat to the security and trust of ICs [2]. Hardware Trojans can be introduced by an adversary at a design house or an untrusted foundry. Depending on the interests of the adversary the HT can cause changes in functionality, denial-of-service, reliability reduction or leaking of secret information [39]. Skorobogatov et al. have reported an incident of HT in real chips which is a backdoor in military-grade FPGAs [37]. Hardware Trojan (HT) can be defined as the unauthorized modification of the original design by an adversary with malicious intent. Such Trojans can be inserted at any abstraction level of IC design and
manufacturing process. The detailed taxonomy of hardware Trojans at various abstraction levels can be found in [39]. In general, Trojans are intelligently designed to be stealthy, so they do not change the normal functionality of the IC unless they are activated. Such Trojans may not be detected by using conventional functional and structural testing techniques, which are used to test the functionality and detect faults like stuck-at-faults etc. Different methods have been proposed for detecting Trojans inserted at different abstraction levels [24]. Such detection methods can be classified as design verification phase (pre-silicon), test phase (post-silicon) and run-time [4] (post-deployment) methods, based on their applicability at different phases of IC production. The pre-silicon detection methods mainly focus on the Trojans that are inserted by modifying RTL code and/or netlist of the design. These methods use the concepts like unused circuit identification (UCI) [17], identification of signals with very low activation probabilities, etc [43].

The test phase i.e post-silicon detection methods aim to detect hardware Trojans in fabricated ICs inserted at untrusted and malicious fabrication foundries. Even though Logic testing [24,41] based approaches for HT detection have been proposed, their efficiency is limited by the stealthy nature of the hardware Trojans and the generation of tests and test execution time. The majority of existing post-silicon methods are devised based on side-channel analysis i.e analyzing the side channel parameters like power, path delay, and electromagnetic measurements, etc. Many existing side-channel analysis (SCA) based HT detection techniques depend on the availability of genuine ICs (golden ICs i.e ICs without any HTs), which are used for generating a reference signature. This signature is then compared against the side-channel signature of suspect IC to decide whether any Trojan exists in the IC under consideration. Obtaining such golden ICs for all the cases is not always feasible, as it involves expensive invasive techniques such as reverse engineering [5]. Another challenge for side-channel analysis-based methods is the process variation (PV) which impacts the efficiency of detection even if golden ICs are available. To overcome these issues, some golden IC free detection methods have been proposed [9,28,43,45], which are based on the concepts of self-referencing and side-channel signature prediction. If the size of inserted Trojan is very small compared to the size of the design, its effect on side-channel parameters may not be differentiable due to process variations (PVs). In the presence of process variation, even if golden ICs are available, direct comparison of the side-channel signatures of the suspect chip with the golden chips may not accurately detect HTs. To mitigate the effects of process variation on side-channel parameters, researchers have proposed a technique known as self-referencing [13]. In this method, the side channel parameter of an IC is compared with the side channel parameter of the IC itself, instead of comparing with the golden signature. The major advantages of self-referencing-based methods are (i) it eliminates the requirement of golden IC and (ii) the effects of inter-die process variation are mitigated.

In the present work, a golden IC-free methodology is proposed to detect Hardware Trojans inserted during fabrication. We have chosen path delay as a medium for Trojan detection because of its specific advantages such as hardware Trojan effect is local to the path and the Trojan affects path delay irrespective of its activation status eliminating the need to activate Trojans. Every IC contains many paths out of which some paths are topologically similar, which we term as symmetric paths. Any two paths which have an equal number of gates of the same type could be considered symmetric paths (see Fig. 2). We analyze the design netlist to identify vulnerable nets which could be potential locations for hardware Trojan insertion. We select a path through such a vulnerable net and we term it as the suspect path. A symmetric path that is topologically similar to the selected suspect path is identified and it is termed as reference path. A symmetric path pair consisting of a suspect and its corresponding reference path is formed. As both the paths in a symmetric path pair pass through the gates of the same type, their delays experience a strong correlation under the inter-die (global or die-to-die) process variation effects. A symmetric path pair has been selected for each vulnerable net in the design netlist. When the delays of paths in such symmetric path pairs are analyzed by plotting on a two-dimensional space they follow straight lines under inter-die variation (see Fig. 3). If a hardware Trojan has presumably been inserted at a vulnerable net, then the delay of the suspect path will be increased by an amount of HT-induced delay. This in turn deviates the point of path delays away from the expected straight line as shown in Fig. 3. The distance between the expected line and the point of delays, due to Trojan-induced deviation has been used to calculate a detection metric (DM) for a selected pair of IC under test. In the presence of intra-die (local or within-die) process variations, the delays of paths in selected symmetric path pairs may tend to deviate from the expected straight line. Therefore, this detection metric is compared with a pre-defined threshold to separate Trojan inserted ICs from Trojan free ICs. This work mainly focuses on detecting the logical Trojans having payload gate(s). The
detection of other types of Trojans like parametric Trojans is out of the scope of this paper.

1.1 Our Contribution

Following are the contributions of our paper.

- We propose a novel path selection algorithm to select symmetric path pairs in a way to mitigate the effects of inter-die variation as well as to minimize the effects of intra-die process variations on hardware Trojan detection accuracy.
- We present a procedure to create symmetric path pairs if they do not exist in the design intrinsically to cover all vulnerable nodes of the design for efficient Trojan detection.
- The proposed Trojan detection methodology employs the concept of self-referencing wherein the delays of topologically symmetric paths are analyzed for detecting hardware Trojans. The methodology doesn’t need a golden reference IC.

The rest of this paper is organized as follows. A brief overview of existing hardware Trojan detection methods is presented in Section 2. Basics of hardware Trojan structure, process variation model, and problem formulation are presented in Section 3. In Section 4, we present the details of the proposed methodology; and path selection procedure is explained in Section 5. Simulation results are reported in Section 6 and we conclude in Section 7.

2 Related work

The detailed taxonomy and classification of hardware Trojans have been presented in [39]. Several methods based on logic testing have been proposed for detecting such Trojans, but these methods may not always detect active and parametric HTs. The efficiency of these methods is limited due to the large trigger space of hardware Trojan, which is not known to the designer. Thus, side-channel analysis (SCA) based techniques have been considered to be more efficient for detecting hardware Trojans (HTs). Agarwal et al. proposed to use side-channel parameter (power) for Trojan detection [8]. They constructed a fingerprint using golden ICs and compared it with the signatures of suspect ICs for HT detection. Path delays were used to generate the fingerprint of an IC family for HT detection in [20]. They have selected a set of paths that covers the entire design. The path delays of genuine ICs are measured and principle component analysis (PCA) was used to construct the fingerprint. The delays of HT inserted ICs are compared against the fingerprint for HT detection. This method is not scalable for larger designs as it requires a large test time to measure the delays of such a large number of paths covering the entire design. The main limitations of these methods are—(i) the requirement of a set of golden ICs and (ii) the detection accuracy is largely affected by process variations. Authors in [26], a technique was proposed for delay measurement to detect HTs. This technique uses shadow registers to measure the path delays and it can be performed at speed at both test time and run time. This method requires multiple clocks and requires extra registers inserted at the end of each selected path which incurs higher area overhead. The efficiency of delay-based HT detection techniques in the presence of process variations was studied in [22]. Authors have considered process variation in different transistor parameters like channel length (L) and threshold voltage (Vth). They computed path delays for HT detection by leveraging statistical techniques, even though process variation affects the HT detection accuracy. Authors in [24] proposed an embedded test structure by using existing scan structures to measure path delays to detect HTs. In this work, they considered only a small number of arbitrary paths for delay measurement. This technique is not feasible for larger designs as it incurs a large area overhead for on-chip control logic. Authors Xiao et al in [21] proposed a clock sweeping-based path delay measurement technique for detecting HTs. The authors considered a set of few long paths and used transition delay fault (TDF) test patterns for delay measurements. Statistical techniques were used for signature generation and HT detection. This technique can only be used to detect the HTs inserted in long paths and cannot detect the HTs in short paths due to the maximum frequency and power limit of the IC. Authors Cha and Gupta in [8], proposed to choose the shortest paths through each possible Trojan location to enhance the effect of HT thus, improving HT detection accuracy in the presence of process variations. By choosing shortest paths only the effect of inter-die variation is minimized and intra-die variation still dominates the detection accuracy. Moreover, this technique cannot perform well when the HT is inserted at such locations through which no shorter path exists. A clock glitching method was proposed to measure path delays and statistical techniques are used to reduce the effects of process variations in [15].

All the aforesaid hardware Trojan detection methods require golden ICs as reference for detecting HTs and they all suffer more or less from both inter-die and intra-die process variations. A self-referencing-based golden-IC free HT detection method using path delays has been
proposed in [22]. It compares the delays of symmetric paths in the design for detecting HTs. This method identifies the symmetries in the design by applying and analyzing the input vector space. This method cannot scale up for larger ICs and to do so one has to strike through all possible states which are not always feasible. Authors have suggested developing and use algorithms for identifying symmetries in the design, but they have not reported any such procedure in their work. A pulse propagation technique is proposed by authors in [11] to detect extra capacitance induced by HT on logical paths. Instead of measuring path delays, current sensing circuitry is used for sensing the pulse propagating through the logic paths in the design for HT detection. The efficiency of the method decreases with the increasing number of high fanout nets in the design. A high resolution on-chip embedded test structure called time-to-digital converter (TDC) for measuring path delays and a chip-averaging technique was proposed to detect delay anomalies introduced by HTs in [19]. An on-chip self-referencing based HT detection method was proposed in [16]. Two paths with some pre-defined delay difference are connected to a latch and the output of the latch is considered for HT detection. If a Trojan affects the path having minimum delay then the output of latch changes leading to detection of the HT. This method suffers from the inter-die variation effects as the selected paths may not remain symmetric, resulting in high false-positive rates. Moreover, this method incurs higher area and power overheads for implementing the latches and supporting additional logic such as multiplexers. In [14] an HT detection method was proposed by using the ratio of delays of two paths. To reduce the effects of inter-die variations, shorter paths are selected. The design was simulated for identifying paths in order to minimize the effects of inter-die variations. Simulating the design and identifying such paths is very difficult and incurs longer design times for larger circuits as the number of possible paths increases exponentially. Moreover, this method would not perform well if sufficiently shorter paths do not exist in the design. A variability-aware path selection procedure was reported in [40]. Authors have considered only shorter symmetric paths to mitigate process variation effects, in fact, longer symmetric paths could also perform well in detecting if they are close enough.

Our proposed methodology in this paper attempts to mitigate the effects of inter-die variation as well as tries to minimize the effects of intra-die variation as much as possible enabling more accurate detection of hardware Trojans. However, like any other delay-based detection techniques, the proposed method is also not able to detect Trojans that don’t have any impact on path delays.

3 Preliminaries and Problem Formulation

3.1 Path delay affected by Hardware Trojan

A Hardware Trojan is constituted by two parts- trigger and payload. The interconnects in the circuit as shown in Fig. 1 provide inputs to the gates in the HT trigger. However, some additional capacitance, of this additional fanout, in turn, impacts the delay. The attack is launched by the payload gate, which is inserted by ripping a present net in the original circuit (see Fig. 1). This net affects the delay of all such paths, which pass through it. The delay is increased by an amount equal to the delay of the payload gate, which usually is higher than the delay caused by the trigger gate.

3.2 Hardware Trojan insertion at vulnerable locations

To defy detection by either testing or side-channel-based techniques, stealthy HTs might be inserted by the attacker. It has been observed that nodes with very low switching activity satisfy the requirements sought after by the attacker [33][34][36]. Hence, we too consider, low switching nets in the circuit as vulnerable locations [40].

3.3 Process Variations

As the HTs are very small in size compared to the entire design, their effect on side-channel parameters is not distinguishable from the effects due to process variation. The inter-die variation component affects all transistors of an IC in a similar fashion, whereas, the intra-die variation component is different depending on their
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physical locations on the IC [18, 27]. Normally, intra-die variations are smaller than inter-die variations. We have considered variations in transistor threshold voltage $V_{th}$ [40]. The variation model considered in this work is shown in (1). Further, the intra-die component $\Delta v_{intra}(x, y)$ is divided into- (i) a correlated spatial component and (ii) a random component, as shown in (2).

$$v_{th}(x, y) = v_{th,nominal} + \Delta v_{inter} + \Delta v_{intra}(x, y)$$  \hspace{1cm} (1)$$

$$\Delta v_{intra}(x, y) = \Delta v_{spatial}(x, y) + \Delta v_{random}(x, y)$$ \hspace{1cm} (2)

Here, $v_{th,nominal}$ is the nominal value of the threshold voltage, and the inter-die variation is $\Delta v_{inter}$. Also, $\Delta v_{spatial}(x, y)$ is a spatially correlated component, for which a representative model is a correlated multivariate Gaussian random variable; whereas $\Delta v_{random}(x, y)$ is the random component, modeled as an independent Gaussian random variable.

### 3.4 Topologically symmetric paths

In this work, we have considered two paths as topologically symmetric if they pass through similar types of logic gates as shown in Fig. 2. It can be observed that all the three paths shown in Fig. 2 are symmetric to each other. Assuming Fig. 2(a) shows a selected suspect path through a vulnerable net, any one of the two paths shown in Fig. 2(b) and 2(c) can be selected as a reference path for the selected suspect path as these paths are topologically symmetric to path shown in Fig. 2(a). We call the path shown in Fig. 2(b) as type–1 reference path and the path shown in Fig. 2(c) as type–2 reference path. The delay of the paths shown in Fig. 2 may or may not be equal as it also depends on the fanout and interconnects delays experienced by gates in the respective paths of the design.

The fundamental difference between type–1 and type–2 reference paths can be explained by propagating a transition through these paths concerning the suspect path. In the type–1 path the signal transition propagates through gates of the same type in the same order as that of the suspect path. Whereas, in type–2 paths, the signal transition propagates through similar gates but in a different order as that of the suspect path. For example, the XOR gate in Fig. 2(b) experiences the same transition as that of the XOR gate in Fig. 2(a) when an identical transition is applied at the input pin of the two paths. Whereas, the XOR gate in Fig. 2(c) experiences the opposite transition as that of the XOR gate in Fig. 2(a) when an identical transition is applied at the input pin of the two paths. Further, we identify a symmetric path pair as a type–1 (type–2) if the selected reference path is of type–1 (type–2). In our work, the path delay has been considered differently for paths in type–1 and type–2 symmetric path pairs. We assume the delay of a path for propagating a rising (falling) transition at its input port through it is represented by $\text{rise delay}$ ($\text{fall delay}$).

In type–1 symmetric path, every gate in the reference path experiences the same transition (rise or fall) concerning the same type of gate in the suspect path. Thus, the delays of the suspect path and the reference path are highly correlated for the identical transition applied at their input ports. Therefore, for paths in type–1 symmetric path pairs the path delay has been considered as either rise delay or fall delay as shown in (3). i.e. if $\text{rise delay}$ ($\text{fall delay}$) is considered as path delay for suspect path then $\text{rise delay}$ ($\text{fall delay}$) of the reference path has to be considered as path delay.

$$\text{path delay} = \begin{cases} \text{rise delay} \\ \text{fall delay} \end{cases}$$ \hspace{1cm} (3)
Table 1: Correlation between path delays of a symmetric path pair for different delay models

| Symmetric path pair | type–1 | type–2 |
|---------------------|--------|--------|
| Delay model         | rise\_delay | fall\_delay | rise\_delay + fall\_delay | rise\_delay | fall\_delay | rise\_delay + fall\_delay |
| Correlation (%)     | 100    | 100    | 100          | 98.712    | 97.687    | 99.997           |

Table 2: Correlation between path delays of a symmetric path pair for different path lengths and fanout difference

| Symmetric path pair | path length | fanout difference (fod) |
|---------------------|-------------|-------------------------|
| Correlation (%)     | 9, 12, 15, 18 | 0, 3, 6, 9, 12 |
| 99.973, 99.984, 99.995, 99.965 | 100, 99.996, 99.993, 99.974, 99.922 |

In type–2 symmetric path pairs, some gates of reference path may experience different transitions concerning the gates of the same type in the suspect path. To compensate for the effects of such transition difference on the correlation between the suspect and reference path delays, the average of rise and fall delays has been considered as the path delay. The rationale behind the average delay is when rising and falling transitions are applied at the inputs of both suspect and reference paths, all the gates in these paths also experience both rising and falling transitions. Therefore, for paths in type–2 symmetric path pairs the path delay has been considered as the average of rise and fall delays as shown in (4).

\[
\text{path\_delay} = \frac{\text{rise\_delay} + \text{fall\_delay}}{2} \quad (4)
\]

The correlation between different delays of suspect path shown in Fig. 2(a) and reference path shown in Fig. 2(b) of a type–1 symmetric path pair under inter-die variation is shown in Fig. 4(a). It can be observed that the rise, fall and average of rise and fall delays of suspect and reference paths are highly correlated under inter-die variation effects. Therefore, either rise\_delay or fall\_delay can be considered as the path delay for the paths in type–1 symmetric path pairs. The percentage correlation coefficient between the delays of paths in type–1 symmetric path pair is shown in Table 1.

Similarly, a type–2 symmetric path pair has been formed by considering the path shown in Fig. 2(a) as suspect path and the path shown in Fig. 2(c) as reference path. The correlation between the suspect and reference path delays of the type–2 symmetric path pair for different delay models considered under inter-die variations is shown in Fig. 4(b). The percentage correlation coefficient between the rise, fall, and the average of both delays of the suspect and the reference paths is shown in Table 1. It is observed that the correlation between rise delays of the suspect path and the reference path is 98.712%. Similarly, the correlation between the fall delays is 97.687%. Whereas, the correlation between the average rise and fall delays of suspect and reference paths of a type–2 symmetric path pair is 99.997%. Therefore, to maintain a high correlation, the average of rise and fall delays as shown in (4), has been considered as the path delay for the paths in type–2 symmetric path pairs.

The effect of inter-die variation on the delays of paths of symmetric path pairs with different path lengths has been shown in Fig. 5(a). We have considered the number of gates in a path as the path length. The path pairs with path lengths 9 and 12 are extracted from c1908 and c2670 benchmark circuits respectively. The path pairs with path lengths 15 and 18 are selected from the c7552 benchmark circuit. It is observed that the delays are as expected for all the path lengths, thus leading to the inference that the effect of inter-die variation is mitigated irrespective of the length of symmetric paths considered. We can even observe that the nominal delays of suspect and reference paths are not equal even though they pass through the same type of gates. This is due to the difference in fanout of each gate and the length of interconnects between the gates in these paths.

We have analyzed the effect of fanout difference on the correlation between the delays of the suspect and the reference paths shown in Fig. 4(a) and Fig. 4(b) respectively. The fanout difference (fod) is considered as the difference between the total fanout of suspect and reference paths. We have connected INVX1\_RVT gate to the nets in the suspect and reference paths randomly to create the fanout difference. For example, to create a fanout difference of 3, we have connected 2 INVX1\_RVT gates to the randomly chosen nets of the suspect path and 5 INVX1\_RVT gates to the nets of reference path randomly. The correlation between path delays of suspect and reference paths under inter-die variation for several fanout differences has been shown in Fig. 4(b). It can be observed that the fanout difference only affects the slope of the expected lines but does not have
any impact on the correlation between path delays under the effects of inter-die variation. Table 2 presents the correlation between the delays of symmetric paths under inter-die variation for different path lengths and fanout differences. It can be observed that the percentage correlation coefficient is greater than 99.9% in all the considered cases. Therefore, we infer that the inter-die process variation effects on hardware Trojan detection can be mitigated by selecting topologically symmetric paths, irrespective of their type, length, and fanout differences.

Let us consider Fig. 4 the nominal delays of suspect path and reference path are represented by \( P_{s,nom} \) and \( P_{r,nom} \) respectively i.e. these are the delays at nominal transistor threshold voltage \( v_{th,nom} \). \( P_{s,rs} \) and \( P_{r,rs} \) are the delays of suspect and reference paths respectively for a random sample due to inter-die variation i.e. these are the delays at transistor threshold voltage \( v_{th,nom} + \Delta v_{inter} \). where \( \Delta v_{inter} \) is a random sample from inter-die variation distribution modeled using (1), which will be same for all the transistors in the two paths as explained in Section 3.3. The expected straight line equation can be determined by using the nominal and random sample delay points as shown in (5).

\[
y - P_{r,nom} = \frac{P_{s,rs} - P_{s,nom}}{P_{s,rs} - P_{s,nom}} (x - P_{s,nom})
\]  

(5)

By rearranging the terms in (5) we get the equation of the expected straight line as follows, where \( \alpha = (P_{r,rs} - P_{r,nom})/(P_{s,rs} - P_{s,nom}) \) and \( \beta = (P_{r,nom} - \alpha P_{s,nom}) \).

\[
\alpha x - y + \beta = 0
\]

(6)

Assuming a hardware Trojan gate has presumably been inserted in the suspect path and it, in turn, induces some extra delay. The delays of suspect path after Trojan insertion and reference path are represented by \( P_s \) and \( P_r \), respectively. Due to HT-induced extra delay, the point \( (P_s, P_r) \) deviates from the expected straight line. This deviation causes the distance \( d \) between the point \( (P_s, P_r) \) and the expected line. This distance \( d \) has been used to calculate the detection metric (DM) to detect hardware Trojan. The distance \( d \) can be calculated as per (7).

\[
d = \frac{1}{\sqrt{1 + \alpha^2}} (\alpha P_s - P_r + \beta)
\]

(7)

The detection metric DM is calculated as the normalized distance (8) from the expected straight line as shown in (8).

\[
DM = \frac{d}{\sqrt{(P_{s,nom})^2 + (P_{r,nom})^2}}
\]

(8)

Under the influence of process variations, the delays of the suspect and the reference paths may deviate from their nominal values. These delays follow the expected line under inter-die variation as the paths are topologically symmetric. The intra-die variation effects cause the deviation of the delay point away from the expected line as it affects transistors in the symmetric paths differently depending on their physical location on the die. Thus, ideally, under no process variations, the value of DM should be zero. It can be understood that even in the presence of inter-die variation also the DM is zero as the delay points lie on the expected line. But, under intra-die variation as the delay points deviate from the expected line, the DM becomes non-zero i.e. DM > 0. Therefore, the computed detection metric DM is compared with a pre-defined threshold (DT) to separate Trojan inserted ICs from Trojan free ICs. The detection threshold DT can be obtained by performing Monte-Carlo simulations with reliable process variation models. The hardware Trojan detection problem can be formulated as

\[
\text{IC under test} = \begin{cases} 
\text{is Trojan free} & \text{if } DM < DT \\
\text{has Trojan inserted} & \text{otherwise}
\end{cases}
\]

(9)

4 Detection Methodology

In this section, we discuss our proposed methodology in detail. The proposed methodology consists of two stages i.e (i) the Pre-fabrication stage and (ii) the Post-fabrication stage. The complete flow of the proposed HT detection methodology is shown in Fig. 6.

4.1 Pre-fabrication stage

We assume that the golden model of the design is available since we have considered the threat model of HT insertion at untrusted foundry i.e. the HT is assumed to be inserted after design sign-off while fabrication. The design netlist has been analyzed to find vulnerable nets, which are considered to be potential locations of HT insertion. We have considered low activity nets as the vulnerable locations for HT insertion as explained in Section 4.4. The set of vulnerable nets \( \{N_v\} \) has been identified using the simulation of the golden netlist of the design over a large number of random test vectors. A symmetric path pair (SPP) consisting of a suspect path and a reference path is selected for each vulnerable net in the design. The path selection algorithm
which is used to select suspect and reference paths is explained in Section 4. A set of symmetric path pairs \( \{N\} \) is formed by combining a suspect path and its corresponding reference path for each net \( n \) in \( \{N_v\} \). The nominal delays of suspect path and reference path of \( i^{th} \) symmetric path pair corresponding to \( i^{th} \) vulnerable net in \( \{N_v\} \) are represented by \( P_{s,nom}^i \) and \( P_{r,nom}^i \) respectively. The detection metric corresponding to \( i^{th} \) pair \( DM_i \) is calculated as the normalized distance from expected straight line using (7) and (8). Monte-Carlo simulations are performed using reliable process variation models provided by the foundry to generate a set of Trojan-free IC instances. The metric \( DM = \{DM_1, DM_2, \ldots, DM_N\} \) corresponding to all selected symmetric path pairs of the design is calculated for all Trojan free IC instances. Using this data a detection threshold is decided for each symmetric path pair. The set \( DT = \{DT_1, DT_2, \ldots, DT_N\} \) contains these threshold values. This \( DT \) is used in the post-fabrication stage for HT detection.

4.2 Post-fabrication stage

The post-fabrication stage involves the measurement and analysis of delays of the paths present in selected symmetric path pairs. The path delays of all \( 2N \) paths in \( N \) pairs are measured for each suspected IC. Techniques presented in [21, 26] can be used to measure the delays of selected paths. The \( DM \) of each pair is cal-

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**Fig. 4** Correlation between suspect path and reference path delays under inter-die variations for different delay models considered (a) for paths in type-1 symmetric path pair (b) for paths in type-2 symmetric path pair

**Fig. 5** Effect of inter-die process variations on delays of suspect and reference paths along the expected line (a) for different path lengths (b) for different fanout differences
calculated using (7) and (8). Each $DM_i$ is compared with pre-defined detection threshold $DT_i$, in order to infer whether the IC under test is Trojan free as shown in (10).

$$\text{IC under test} = \begin{cases} 
\text{is Trojan free} & \text{if} \quad DM_i < DT_i \\
\text{has Trojan inserted} & \text{otherwise}
\end{cases} \quad (10)$$

5 Path selection Procedure

The proposed path selection procedure and reference path creation technique are described in this Section.

5.1 Path selection algorithm

The proposed path selection technique is presented in Algorithm [1]. This algorithm takes a set of vulnerable nets $N_v$ and the golden design netlist as inputs and returns a topologically symmetric path pair (SPP) consisting of a suspect path and its corresponding reference path for each vulnerable net in the design. All sensitizable paths passing through the vulnerable net $n_i$ are collected in set $S_i^{\text{all-paths}}$. We have used Boolean satisfiability (SAT) based techniques to decide whether a path is sensitizable [29, 31, 35]. For the sake of clarity and simplicity, wherever we refer to a path in the remainder of the paper, it is to be considered as a sensitizable path. All the paths that have symmetric paths (i.e. either type-1 or type-2) are collected in set $S_i^{\text{symmetric}}$. The nets which have at least one symmetric path for at least one path out of all paths passing through them are collected in set $N_{\text{covered}}$ and called covered nets. If there are no symmetric paths for at least one path in $S_i^{\text{all-paths}}$ then we call such nets as uncovered nets. We need to create a symmetric path to be used as a reference path for each of such nets. The procedure as explained in Algorithm [3] is used for reference path creation. All possible suspect paths through the net $n_i$ are collected in set $S_i^{\text{suspect}}$, and all the paths symmetric to the path $P_i^{\text{suspect,j}}$ in $S_i^{\text{suspect}}$ are collected in $S_i^{\text{symmetric,j}}$.

After finding out possible suspect paths and corresponding symmetric paths for each vulnerable net, the final layout of the netlist is prepared. The physical location information of each gate is collected from the layout of the netlist and is used for selecting the nearest symmetric path pair to exploit the spatial correlation component of intra-die variation. We compute the rank of a symmetric path pair as the average of distances between similar gates in a symmetric path pair. The procedure for computing the rank of a symmetric path pair is presented in Algorithm [2]. The suspect path and corresponding symmetric path are represented by $P_i^{\text{suspect,j}}$ and $P_i^{\text{symmetric,k}}$, respectively. The gates in paths $P_i^{\text{suspect,j}}$ and $P_i^{\text{symmetric,k}}$ are collected in sets $G_{\text{suspect}}$ and $G_{\text{sym}}$, respectively. Assume $g_l$ and $g_m$ are similar type gates present in $G_{\text{suspect}}$ and $G_{\text{sym}}$ and their locations on the layout of the design are represented by $(x_l, y_l)$ and $(x_m, y_m)$, respectively. The Euclidean distance $dist_{lq}$ between these two gates $g_l$ and $g_m$ is calculated as shown in line 8 of Algorithm [2]. The rank of the symmetric path pair is computed by taking the average of the distances $dist_{lq}$ for all the gates in $G_{\text{suspect}}$ as shown in line 10 of Algorithm [2]. Here, $|G_{\text{suspect}}|$ represents the cardinality of the set $G_{\text{suspect}}$ which
is nothing but the number of gates in the suspect path. An example illustrating the Algorithm 2 is presented in Fig. 7. A pair that has nearest symmetric paths for at least one path in \( S^i_{\text{all paths}} \) then create a symmetric path.

![Fig. 7 Example for ranking symmetric path pairs according to the locations of gates in the layout (a) suspect path (b) symmetric path with rank = 3 i.e. \((2+2+5)/3\) (c) symmetric path with rank = 21 i.e. \((50 + 5 + 10)/3\)](image)

![Fig. 8 Generating symmetric path (a) selected suspect path (b) a non-critical path (c) generated symmetric path to cover the vulnerable net](image)

5.2 Reference path creation

There may be some vulnerable nets for which a symmetric path pair (SPP) may not exist intrinsically in the design. We call such nets uncovered nets. To cover such nets, we create a symmetric path to be used as a reference path by adding few extra logic gates to the existing non-critical paths of the design as shown in Fig. 8. Algorithm 3 presents the procedure for creating the reference path to cover an uncovered net \( n_i \). We chose the shortest path through the uncovered net \( p_{\text{short}} \) as the shorter paths experience less intra-die variation effects as they consist less number of gates. The non-critical

![Algorithm 1: Path selection algorithm](image)

\[
\text{Algorithm 1: Path selection algorithm}
\]

\[
\begin{align*}
\text{Input} &: \text{ Netlist}, N_v = \text{set of vulnerable nets} \\
\text{Output}: &\text{Symmetric path pairs} \\
\text{foreach} &\text{net } n_i \text{ in } N_v \text{ do} \\
&\text{if } |S^i_{\text{symmetric}, j} | = 0 \text{ then} \\
&\text{else} \\
&\text{if } |S^i_{\text{symmetric}, j} | = 0 \text{ then} \\
&\text{else} \\
&\text{Add net } n_i \text{ to the set of covered nets } N_{\text{covered}} \\
\text{end} \\
\text{end} \\
\text{foreach} &\text{path } P^i_{\text{suspect}, j} \text{ in } S^i_{\text{all paths}} \text{ do} \\
&\text{SymmetricPathPair}_i \leftarrow (p^i_{\text{suspect}}, P^i_{\text{ref}})
\end{align*}
\]
Algorithm 2: Calculation of rank of a path pair – rank()

Input: A pair of paths $P_{\text{suspect,}j}^i$ and $P_{\text{symmetric,}k}^i$
Output: Rank of the path pair

1. $G_{\text{suspect}}$ = Set of all gates in path $P_{\text{suspect,}j}^i$
2. $G_{\text{symmetric}}$ = Set of all gates in path $P_{\text{symmetric,}k}^i$
3. foreach gate $g_i$ in $G_{\text{suspect}}$
   4. foreach gate $g_m$ in $G_{\text{symmetric}}$
      5. if $g_i = g_m$
         6. /* If both gates are of same type */
         7. location of $g_i$ on layout is $(x_i, y_i)$
         8. location of $g_m$ on layout is $(x_m, y_m)$
         9. $\text{dist}_q = (x_i - x_m)^2 + (y_i - y_m)^2$
     10. end
     11. end
     12. return $\text{rank} = \frac{\sum_{g_i}^{|\text{sub}_g|} \text{dist}_q}{|G_{\text{suspect}}|}$

Algorithm 3: Reference path creation – ref-pathgen()

Input: Uncovered vulnerable net $\mathcal{N}_i$, $S^i_{\text{all paths}}$
Output: Symmetric path pair through net $\mathcal{N}_i$

1. $P_{\text{short}}$ = a sensitizable path with minimum delay in $S^i_{\text{all paths}}$
2. $S_{\text{sub}}$ = a set non-critical paths $P_{\text{sub}}$ that have set of all gates in each path as subset of gates in the path $P_{\text{short}}$ i.e. $\text{gatesof}(P_{\text{sub}}) \subseteq \text{gatesof}(P_{\text{short}})$
3. if $|S_{\text{sub}}| = 0$ then
   4. $S^i_{\text{all paths}} = S^i_{\text{all paths}} - P_{\text{short}}$ and goto step: 1
5. end
6. foreach $P_{\text{sub}}$ in $S_{\text{sub}}$
7. $\text{extragates} = \text{gatesof}(P_{\text{short}}) - \text{gatesof}(P_{\text{sub}})$
8. Compute area overhead i.e. area of extra gates
9. end
10. Select the path $P_{\text{sub}}$ from $S_{\text{sub}}$ with minimum area overhead
11. $P_{\text{ref}} = P_{\text{sub}}$ with extragates inserted at its input net
12. Connect off-path inputs of extragates to non-controlling values
13. Check the functionality after extra gates insertion
14. Check the timing of all paths through the input net of $P_{\text{ref}}$
15. if functionality and timing are satisfied then
   16. $P_{\text{suspect}} = P_{\text{short}}$ and $P_{\text{ref}} = P_{\text{ref}}$
17. else
   18. $S_{\text{sub}} = S_{\text{sub}} - P_{\text{sub}}$ and goto step: 10
19. end
20. return $\text{SymmetricPathPair}_i \leftarrow (P_{\text{suspect}}^i, P_{\text{ref}}^i)$

paths which have gates that are a subset of gates of $P_{\text{short}}$ are collected in $S_{\text{sub}}$. The path $P_{\text{sub}}$ in $S_{\text{sub}}$ with minimum area overhead is selected and the extra gates are found as $\text{gatesof}(P_{\text{short}}) - \text{gatesof}(P_{\text{sub}})$. These extra gates are inserted at the input net of $P_{\text{sub}}$, thus forming a type-1 or type-2 symmetric path to be used as a reference path $P_{\text{ref}}$. The off-path inputs of extra inserted gates must be connected to non-controlling values. The functionality of the design should not change due to the addition of extra gates. Moreover, the timing of all paths passing through the input net of $P_{\text{ref}}$ must not violate any timing constraints. The designer has to ensure that all paths through the input net of the created new path must be non-critical even after the addition of extra gates and functionality must remain the same. Moreover, the created paths will be non-critical but are not redundant as they are part of the design. If the functionality and timing are satisfied $P_{\text{short}}$ and $P_{\text{ref}}$ are assigned to suspect $P_{\text{suspect}}$ and reference $P_{\text{ref}}$ paths respectively. A symmetric path pair for an uncovered net $\mathcal{N}_i$ is returned as $\text{SymmetricPathPair}_i \leftarrow (P_{\text{suspect}}^i, P_{\text{ref}}^i)$.

6 Results

Simulations have been performed on ISCAS-85 benchmark circuits [7] to evaluate the proposed methodology. We carried out the experiments on a computer with an Intel Core i5-650@3.2 GHz processor and 8GB memory and the flow and proposed algorithms were implemented in python language. The benchmarks have been synthesized using Synopsys generic (SAED-EDK32m) library. For performing SPICE level simulations 32nm CMOS Predictive Technology Models (PTM) [8] are considered. The netlists are simulated over a large number of random test vectors (i.e. $1 \times 10^6$) and nets with switching activity less than a predefined threshold ($1 \times 10^{-3}$) are considered as vulnerable nets as explained in Section 3.2. Static timing analysis (STA) is performed using Synopsys’s PrimeTime to generate path data. We used SAT-based techniques to isolate sensitzable paths out of all possible paths in the design and the SAT solver used was MiniSat-2.2. Symmetric paths are created to cover the uncovered nets as explained in Section 5.2. Physical layout synthesis of design is carried out using Synopsys IC Compiler for generating the layout. This layout has been partitioned into $16 \times 16$ grids to model spatially correlated intra-die variations. We have assumed that all transistors in a gate and all the gates in a grid experience the same within-die variations. Symmetric path pairs are selected using path selection procedure explained in Section 5. Selected paths are extracted in SPICE netlist format from the layout of the design. Process variation on threshold voltage ($V_{th}$)
Table 3 Run time of the proposed path selection algorithm for ISCAS-85 benchmark circuits (in minutes)

| Circuit | Run time |
|---------|----------|
| c432    | 68       |
| c409    | 12       |
| c880    | 13       |
| c1355   | 27       |
| c1908   | 6        |
| c2670   | 14       |
| c3540   | 765      |
| c5315   | 143      |
| c7552   | 285      |

is modeled as explained in Section 3.3. The 3σ values for inter-die and intra-die variation are considered as 20% and 15% respectively [6,10,22]. As the layout has been partitioned into 16 × 16 grids, 256 correlated multivariate random variables are generated to model the spatial variation. The spatial correlation is considered as 0.8 to 0.3 according to the distance between the grids. Spatial correlation decreases with an increase in distance between grids. 500 IC instances without HT and 500 IC instances with Trojan shown in Fig. 1 are generated using the $V_{th}$ PV model [11] and [22]. HSPICE is used to perform SPICE level simulations using the generated $V_{th}$ profiles.

The summary of our experimental results is presented in Table 4. Rows 2 and 3 present the number of gates and nets present in each benchmark circuit considered. The percentage of sensitizable paths out of total possible paths in the design netlist is shown in row 4. We have considered only sensitizable paths for selecting symmetric path pairs using the proposed path selection algorithm. Total vulnerable nets i.e. the nets with switching activity less than the predefined threshold are presented in row 5. The uncovered nets i.e. the vulnerable nets which do not have symmetric paths intrinsically in the design are presented in row 6. We have created a symmetric path pair for each uncovered net by inserting few additional gates. The number of extra gates added to the design to create symmetric path pairs for all uncovered nets are presented in row 7. The number of symmetric path pairs (SPPs) selected to cover all the vulnerable nets is presented in row 8. We have observed that few suspect paths pass through more than one vulnerable net. Thus, the number of selected SPPs is lower than the number of vulnerable nets in c499, c1355, c2670. As we selected an SPP for every fanout branch of each vulnerable net, the number of selected SPPs is higher than the number of vulnerable nets in c432, c880, c1908, c3540, c5315, c7552. Rows 9 and 10 represent the type-1 and type-2 symmetric path pairs out of the total selected path pairs. Row 11 represents the ratio of nets covered by the selected SPPs. The net coverage ratio of c1355 is 50.6% with no area overhead, whereas it is 11.3% even with 14.2% area overhead for c1908. We have observed that the net coverage ratio is higher if the majority of the paths in selected SPPs are mutually disjoint i.e. they do not share many common segments of other paths, otherwise the net coverage ratio is lower. The area overhead, due to extra gates added to the design for creating SPPs to cover uncovered nets, is presented in row 12. Finally, the true positive rate (TPR) and false-positive rate (FPR) are shown in rows 13 and 14 respectively.

The runtime of the proposed path selection procedure for different benchmark circuits is presented in Table 3. Our automated flow considers a set of vulnerable nets and design netlist as inputs and reports the set of selected symmetric path pairs as output. Circuit c3540 has the longer run time of 765 minutes and c1908 has the shorter run time of 6 minutes. We observe that both of these circuits have a moderate number of gates and nets in comparison to the remaining circuits (i.e. neither c3540 has the highest number of gates and nets nor c1908 has the lowest). Therefore, it can be inferred that the runtime is not dependent on the number of gates and nets present in the design. We observed that it is dependent on the total number of possible paths and the number of sensitizable paths out of the total number of possible paths in the design.

6.1 HT detection analysis

The variation in delays of suspect and reference paths of a symmetric path pair (SPP) of several benchmark circuits is shown in Fig. 3. The path delays vary along the expected straight line passing through the point of nominal delays despite inter-die variations. However, due to intra-die variations they tend to deviate away from the straight line. It is observed that the points representing the delays of SPPs in HT inserted ICs are away from the expected straight line. The graphs illustrating the effect of variation and HT on a selected SPP of some benchmarks are presented in Fig. 8(a), 8(b) and 8(c). Detection metric (DM) for SPPs of each IC under test is calculated as per [6]. The $DM$ of trojan free and with trojan ICs are shown in Fig. 8(d), 8(e) and 8(f). The detection threshold $DT$ has been decided in a pessimistic way by allowing a false positive rate of 3%. The dashed horizontal lines in Fig. 8(d), 8(e) and 8(f) represent the selected $DT$ for the considered SPP of each benchmark. It can be observed that the $DM$ of few HT free ICs, is above the threshold line in Figs. 8(d), 8(e) and 8(f). Nevertheless, the $DM$ of few Trojan inserted ICs is below the threshold line only in Fig. 8(c). True positive rate (TPR) is defined as the ratio of
The TPR and FPR shown in Table 4 are for the worst-case symmetric path pair i.e. the pair with lower TPR and/or higher FPR out of all selected SPPs for a benchmark under consideration. The TPR and FPR for c432 and c5315 benchmarks are 100% and 3%. Though the proposed method correctly detects all the Trojan inserted ICs, it falsely classifies a few Trojan free ICs as Trojan inserted ones. It is because the paths in these SPPs are not close enough to each other. The TPR and FPR of c1908 are 99% and 3%. Even with an FPR of 3%, the proposed methodology cannot detect all the Trojan inserted ICs and few Trojan affected ICs are identified as Trojan free. The SPPs of c432 and c1908 are intrinsic to the design, whereas the SPP of the c5315 circuit is not intrinsic but it is a created SPP to cover an uncovered net. Even though the SPP contains the shortest suspect path the created reference path is not closer to the suspect path. This leads to higher FPR in c5315. One way to improve the detection accuracy is
to place the suspect and reference paths closer to each other manually while preparing the layout. However, this would incur extra area and routing overhead and requires additional design efforts.

6.2 Overhead analysis

The area overhead of the proposed methodology is due to the additional gates used to create symmetric path pairs for covering uncovered nets. The benchmark circuit c1908 has the highest area overhead of 14.2%. Whereas, the area overhead of c499 and c1355 circuits is 0% as all the vulnerable nets are covered by the symmetric path pairs that exist in the design intrinsically. It is observed that the area overhead is dependent on the number of extra gates required to cover the uncovered nets. For circuits c1908 and c2670, even though the number of uncovered nets in c1908 is less than that of c2670, the number of extra gates required for c1908 is higher than that of c2670. Therefore, we conclude that the area overhead of the proposed method is not only dependent on the number of uncovered nets but also depends on the circuit structure.

6.3 Security analysis

As the proposed hardware Trojan detection (HT) method depends on the difference in path delays of two symmetric paths, it may be argued that this method may fail to detect hardware Trojans if the same Trojan gate is inserted in both the symmetric paths considered. To be able to do so, an attacker must be aware of the detection method employed which is highly unlikely. Even if the attacker knows the method, he/she has to double the number of alterations to the design to bypass the proposed method. Even if the attacker possesses the knowledge that a delay-based scheme is being used to detect HT, it is highly unlikely that he can determine the exact paths under consideration. Because there would be many paths available to pick a suspect path and for each of such selected paths there would be many possible reference paths. The probability of identifying the selected path pairs for ISACS-85 circuits is shown in table 5.

The procedure of selecting a reference path arises only during detecting Trojan. To make the advantage of self-referencing, more clear, we compute the probability of selection of a reference path corresponding to the suspect path by the attacker while hiding the Trojan.

Consider a vulnerable net of the design. Assume there are m paths $P_1$, $P_2$, ..., $P_m$ passing through this net. Suppose each one of these m paths has corresponding symmetric paths from which a reference path is chosen i.e path $P_i$ has $k_i$ symmetric paths. The probability of the attacker finding the correct symmetric path pair is $P\{ \text{selecting the correct pair} \} = \frac{1}{\sum_{i=1}^{m} k_i}$. If

Table 5 Probability of an attacker identifying the selected path pair in order to bypass the proposed method

| Circuit | Probability       |
|---------|-------------------|
| c32    | $3.2895 \times 10^{-7}$ |
| c499   | $1.0377 \times 10^{-6}$ |
| c880   | $4.9964 \times 10^{-7}$ |
| c1355  | $1.2752 \times 10^{-7}$ |
| c1908  | $4.3892 \times 10^{-7}$ |
| c2670  | $2.7472 \times 10^{-7}$ |
| c3540  | $1.5922 \times 10^{-7}$ |
| c5315  | $1.8503 \times 10^{-7}$ |
| c7552  | $1.0382 \times 10^{-6}$ |
there are $N$ nets in the design then $P\{\text{Attacker bypassing the method}\} = \frac{1}{\sum_{k=1}^{N} k_i}$

7 Conclusion

In the present work, we have considered a threat model of hardware Trojan insertion during fabrication at untrusted foundries. We have presented a novel methodology for hardware Trojan (HT) detection by analyzing the delays of topologically symmetric paths. Further, we have proposed a procedure to select paths that mitigates the effect of inter-die variation and minimizes the intra-die variation effects. We have selected topologically symmetric paths to mitigate the effects of inter-die variation and selected physically closer paths to exploit the spatial correlation for reducing the impact of intra-die variation on hardware Trojan detection accuracy. Moreover, this method uses the concept of self-referencing, which eliminates the requirement of golden reference ICs. We have proposed and validated a procedure to create symmetric paths to cover all vulnerable nets in the design. Simulation results establish that the proposed method is able to detect HTs, which are as small as one gate. In this work, we have used simulation results to decide the detection threshold. Further work could use on-chip process variation monitors to estimate the detection threshold of each suspect IC. We are currently working on locating the trojan.

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References

1. Predictive Technology Model (2017). URL http://ptm.asu.edu/

2. Adee, S.: The Hunt For The Kill Switch. IEEE Spectrum 45(5), 34–39 (2008). DOI 10.1109/MSPEC.2008.4505310

3. Agrawal, D., Baktir, S., Karakoyunlu, D., Rohatgi, P., Sunar, B.: Trojan Detection using IC Fingerprinting. In: Proceedings of IEEE Symposium on Security and Privacy, pp. 296–310 (2007). DOI 10.1109/SP.2007.36

4. Bao, C., Forte, D., Srivastava, A.: Temperature Tracking : Towards Robust Run-time Detection of Hardware Trojans. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 34(10), 1577–1585 (2015). DOI 10.1109/TCAD.2015.2424929

5. Bao, C., Forte, D., Srivastava, A.: On Reverse Engineering-Based Hardware Trojan Detection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 35(1), 49–57 (2016). DOI 10.1109/TCAD.2015.2488495

6. Bonfiglio, V., Iannaccone, G.: Sensitivity-based investigation of threshold voltage variability in 32-nm flash memory cells and MOSFETs. Solid-State Electronics 84(Supplement C), 127–131 (2013). DOI 10.1016/j.sse.2013.02.029

7. Brglez, F. and Fujiiwa, H.: A Neutral Netlist of 10 Combinational Benchmark Circuits and a Target Translator in Fortran. In: Proceedings of IEEE Int’l Symposium Circuits and Systems (ISCAS’85), pp. 677–692 (1985).

8. Cha, B., Gupta, S.K.: Trojan Detection via Delay Measurements: A New Approach to Select Paths and Vectors to Maximize Effectiveness and Minimize Cost. In: Proceedings of Design, Automation Test in Europe Conference Exhibition (DATE), pp. 1265–1270 (2013). DOI 10.7873/DATE.2013.262

9. Chen, X., Wang, L., Wang, Y., Liu, Y., Yang, H.: A General Framework for Hardware Trojan Detection in Digital Circuits by Statistical Learning Algorithms. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 36(10), 1633–1646 (2017). DOI 10.1109/TCAD.2016.2638442

10. Damrongplasit, N.: Study of Variability in Advanced Transistor Technologies. Ph.D. thesis, University of California, Berkeley (2015)

11. Deyati, S., Muldrey, B.J., Chatterjee, A.: Trojan Detection in Digital Systems Using Current Sensing of Pulse Propagation in Logic Gates. In: Proceedings of 17th International Symposium on Quality Electronic Design (ISQED), pp. 350–355 (2016). DOI 10.1109/ISQED.2016.7479226

12. Dong, C., Xu, Y., Liu, X., Zhang, F., He, G., Chen, Y.: Hardware Trojans in Chips: A Survey for Detection and Prevention. Sensors 20(18), 5165 (2020). DOI 10.3390/s20185165. URL https://www.mdpi.com/1424-8220/20/18/5165

13. Du, D., Narasimhan, S., Chakraborty, R.S., Blumia, S.: Self-referencing: A Scalable Side-channel Approach for Hardware Trojan Detection. In: Proceedings of the 12th International Conference on Cryptographic Hardware and Embedded Systems, vol. CHES’10, pp. 173–187 (2010). DOI 10.1007/978-3-642-15031-9_12

14. Esirci, F.N., Bayrakci, A.A.: Hardware Trojan detection based on correlated path delays in defiance of variations with spatial correlations. In: Proceedings of Design, Automation Test in Europe Conference Exhibition (DATE), pp. 163–168 (2017). DOI 10.23919/DATE.2017.7929976

15. Exurville, I., Zussa, L., Rigaud, J.B., Robisson, B.: Reliable Hardware Trojans Detection based on Path Delay Measurements. In: Proceedings of IEEE International Symposium on Hardware Oriented Security and Trust (HOST), pp. 151–156 (2015)

16. Ghobad, Z., Morteza, S.Z.: Latch-Based Structure: A High Resolution and Self-Reference Technique for Hardware Trojan Detection. IEEE Transactions on Computers 66(1), 100–113 (2017). DOI 10.1109/TC.2016.2576444

17. Hicks, M., Finnicum, M., King, S.T., Martin, M.M.K., Smith, J.M.: Overcoming an Untrusted Computing Base: Detecting and Removing Malicious Hardware Automatically. In: Proceedings - IEEE Symposium on Security and Privacy, pp. 159–172 (2010). DOI 10.1109/SP.2010.18

18. Hongliang, C., Sapatnekar, S.S.: Statistical Timing Analysis Considering Spatial Correlations Using a Single PERT-like Traversal. In: Proceedings of IEEE International Conference on Computer Aided Design, pp. 621–625 (2003). DOI 10.1109/ICCAD.2003.159746

19. Ismari, D., Plusquellic, J., Lamech, C., Bhunia, S., Saqib, F.: On Detecting Delay Anomalies Introduced by Hardware Trojans. In: Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 1–7 (2016). DOI 10.1145/2966986.2967061
