A frequency and sensitivity tunable microresonator array for high-speed quantum processor readout

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Superconducting microresonators have been successfully utilized as detection elements for a wide variety of applications. With multiplexing factors exceeding 1,000 detectors per transmission line, they are the most scalable low-temperature detector technology demonstrated to date. For high-throughput applications, fewer detectors can be coupled to a single wire but utilize a larger per-detector bandwidth. For all existing designs, fluctuations in fabrication tolerances result in a non-uniform shift in resonance frequency and sensitivity, which ultimately limits the efficiency of bandwidth utilization. Here we present the design, implementation, and initial characterization of a superconducting microresonator readout integrating two tunable inductances per detector. We demonstrate that these tuning elements provide independent control of both the detector frequency and sensitivity, allowing us to maximize the transmission line bandwidth utilization. Finally we discuss the integration of these detectors in a multilayer fabrication stack for high-speed readout of the D-Wave quantum processor, highlighting the use of control and routing circuitry composed of single-flux-quantum loops to minimize the number of control wires at the lowest temperature stage.

INTRODUCTION

Since their first demonstration in 2003,[1] superconducting microresonators have become increasingly popular for low-temperature detector applications. They are an attractive option due to their intrinsic frequency-domain multiplexing capability, the wide availability of high-speed digital electronics, and breakthroughs in material physics allowing very high sensitivities to be achieved.[2–8] Arrays of these devices have been successfully demonstrated at sub-mm,[9–11] far-infrared,[12, 13] infrared/optical,[14], and x-ray[15] wavelengths, for phonon imaging[16–18] and in quantum computing.[19, 20]

Despite these achievements, superconducting microresonator arrays typically suffer from inefficient bandwidth utilization due to unavoidable fabrication imperfections. As an example, the operating frequency $f$ of an LC resonator utilizing a parallel plate capacitor suitable for integration with a multi-layer fabrication stack will be sensitive to perturbations of the dielectric thickness $d$ according to the expression $\delta f/f = \delta d/2d$. A realistic $\pm10\%$ tolerance in layer thickness for a modern fabrication facility results in up to $\pm300$ MHz shift for a nominal 6 GHz microresonator. Global variations affecting all devices uniformly can usually be compensated by a simple shift in the readout center frequency, however, local variations are more problematic. These cause each microresonator to exhibit a resonance frequency $f_0$ which deviates randomly from its expected value - often by more than a linewidth. The array designer is thus left with a choice of either sparsely populating the available electronics bandwidth with resonances such that stochastic resonance collisions are avoided, or utilizing a high-multiplexing factor and accepting a decreased array yield due to overlapping resonances.

FIG. 1: Schematic for a single FASTR detector. As described in the text, the microresonator parameters are adjusted with local magnetic flux biases to the DC-SQUID loops which act as tunable nonlinear inductors. Tuning these biases allows in-situ compensation for the unavoidable device variations inherent in fabrication. While both DC-SQUIDs are tunable, only a single loop, labeled SENSE, is coupled to the measurement system. For the D-Wave quantum processor, this is the last stage of a data shift register made from quantum flux parametrons (QFPs).

One way to make an array with efficient bandwidth utilization is to use superconducting microresonators whose frequency and sensitivity can be tuned in-situ, allowing compensation for local fabrication variations. Tuning of these parameters allows an array of detectors to exhibit homogeneous sensitivity and uniform frequency spacing. While superconducting microresonators with tunable frequencies have been previously demonstrated,[21, 22] this single adjustment knob is insufficient in the context of
an efficiently packed array. The detector sensitivity is equally important when the array is subject to a signal with a large dynamic range, as more sensitive detectors will exhibit a larger frequency shift than less sensitive detectors resulting in detector frequency collisions. Adding a second tuning knob that also provides sensitivity tuning allows maximum packing efficiency to be achieved for a fixed electronic bandwidth. A schematic of a Frequency And Sensitivity Tunable Resonator (FASTR) detector is shown in Fig. 1.

The tuning parameters are realized using two DC-SQUID loops in series with a fixed geometric inductance $L_g$. Each of these DC-SQUIDs are nonlinear inductances that can be adjusted using an external flux bias. This inductive branch is in parallel with a shunt capacitor $C_s$. External flux can be applied locally to each DC-SQUID loop either with individual analog wires, requiring $2N$ wires for an array of $N$ detectors, or with an array of flux DACs.[25] This latter option can take advantage of an addressing network which requires only $O(\sqrt{2N_{res}})$ wires, making control of even very large arrays straightforward. Flux sensitivity is achieved by coupling one of the two loops to the system of interest. Proper selection of the DC-SQUID biases is required to achieve a desired operating frequency and sensitivity. The measured detector frequency of a prototype device (discussed below) for various flux biases in the two DC-SQUID loops is shown in Fig. 2.

A contour of constant frequency has been drawn on the surface at a frequency shift of about $-3.5$ linewidths from the zero-flux resonance frequency. Only the SENSE SQUID is coupled to the measurement system. For the schematic shown in Fig. 1 the FASTR detector is coupled to a quantum flux parametron (QFP) which is the last stage of a data shift register. Modulating the state of the QFP while following this contour allows the device responsivity to be measured. The result of this measurement is shown in Fig. 2. Bias selection then consists of first choosing a contour of constant frequency followed by a traversal of the contour until the desired responsivity has been achieved.

Here we discuss the real-world example of utilizing a frequency-multiplexed array of FASTR detectors for readout of the D-Wave Two quantum processor. We first briefly discuss the readout constraints imposed by the D-Wave Two quantum processor. We then present a parametric design and physical realization of a single prototype FASTR detector suitable for processor integration. While this specific application demonstrates a proof-of-principle of a frequency- and sensitivity-tunable superconducting microresonator, it should be kept in mind that this device can be broadly applied to a wide variety of magnetic-flux sensing applications including readout of the family of single flux quantum (SFQ) digital circuitry.

**READOUT CONSTRAINTS OF THE D-WAVE TWO QUANTUM PROCESSOR**

The current D-Wave quantum processor utilizes the quantum annealing algorithm to solve for the low lying energy states of the Ising spin Hamiltonian

$$H = \sum_i h_i \sigma_i^z + \sum_{i<j} J_{ij} \sigma_i^z \sigma_j^z$$

where the $\sigma_i$ are Pauli matrices for the $i$th spin, $h_i$ are local energy scaling factors, and the non-zero coupling terms $J_{ij}$ reflect the underlying connectivity of the processor graph. For the D-Wave Two processor, the graph consists of 64 repeated 8 qubit unit cells. Within a cell the qubits are connected in a K4,4 planar topology. Each qubit is further connected to two qubits in neighboring unit cells to yield 6 connections per processor qubit. The processor topology, qubit parametric design, problem specification (consisting of setting the $h_i$ and $J_{ij}$ terms in Eq. 1), and the annealing algorithm have been previously described.[23–28] It is important to note that during the annealing procedure qubit entanglement...
is eventually frozen out and all qubits are projected into a classical flux state before readout.

FIG. 3: Picture of the D-Wave Two processor chip, made up of 64 eight-qubit unit cells. The shift register streets are highlighted yellow to the outside of the processor where it is straightforward to locate FASTR detectors.

![Diagram of D-Wave Two processor chip](image)

FIG. 4: Simplified schematic of a portion of the QFP-based shift register. $Q_1$ and $Q_2$ are qubits and $\phi_0...\phi_3$ are flux biases that control data flow.

![Simplified schematic of shift register](image)

Processor readout entails detecting the flux state of all qubits at the end of a computation sequence. The readout architecture consists of a shift register lattice interlaced between the 8-qubit unit cells. A picture of the processor chip, with the shift register lattice highlighted in yellow, is shown in Fig. 3. The shift register eliminates the need for an individual detector per qubit and is used to move state information from individual qubits out to detectors on the chip perimeter. A simplified portion of the shift register is shown schematically in Fig. 4.

A shift register stage is composed of a QFP that can be modulated between a monostable unlatched and a bistable latched state using a local flux bias $\phi_n$. In the latched state, information is stored in the QFP as either circulating or counter-circulating current. This current is a flux source which applies a flux bias to the neighboring shift register stages held in the unlatched state. The next stage in the forward direction is subsequently latched before the source stage is unlatched allowing information to be passed down the shift register. Note that two unlatched stages are required between every latched stage in order to protect against back-action from data further ahead in the shift register. As indicated in Fig. 4, three QFP flux biases $\phi_1...\phi_3$ are thus required to pass information along the shift register. A separate QFP stage, biased by $\phi_0$, is directly connected to each qubit and is used to selectively copy data from the qubit to the rest of the shift register.

The topology and operating speed of the shift register set crucial constraints for the FASTR readout array. For the processor shown in Fig. 3 there are 8 vertical and 8 horizontal shift registers. As data can be moved in either direction along the shift register, there are 32 points where detectors can easily be placed. Note, however, that the shift register can only move in one direction at a time so that only half of these detectors can be operated simultaneously. The detector on the other end of each line provides redundancy for shift register breaks caused by inoperable QFPs. While in principle it is possible to increase the shift register fan-out by utilizing more stages, this option increases circuit complexity.

FIG. 5: Simplified system electronics schematic for FASTR array readout. The digital-to-analog and analog-to-digital converters are phase locked and sampled at 2.5 GSPS.

![Simplified system electronics schematic](image)

The shift register operation speed is set by the bandwidth of the QFP flux bias lines $\phi_n$. Currently these lines utilize a 30 MHz low-pass filter to limit noise. As the shift register is composed of three biases $\phi_1...\phi_3$, each shift register line can deliver data at $\sim 10$ Mbits/s. If only a single detector is attached to each shift register line, the detector bandwidth should match or somewhat exceed 10 MHz.

Although the attainable readout speed for a FASTR detector is set by the microresonator linewidth, more than a single linewidth of electronic bandwidth is required per detector. Additional bandwidth is required to accommodate shifting of the resonance frequency due to modulation of the signal coupled into the SENSE SQUID. Even more electronic bandwidth is required to avoid electronic crosstalk with neighboring microresonators, as the
resonance appreciably perturbs the microwave transmission beyond the nominal linewidth.

Given the preceding constraints, the FASTR readout for the D-Wave Two quantum processor is designed to utilize resonances with 19.5 MHz linewidths, modulated by 1 linewidth by the shift register data. Each detector is allotted 4 linewidths of electronic bandwidth to minimize crosstalk. A total of 2.5 GHz of readout electronic bandwidth is therefore required to readout all 32 detectors on a single transmission line. Considering this, the current D-Wave FASTR readout is designed to operate using a 2.5 GHz bandwidth with an array center frequency of 6 GHz. A simplified schematic of the readout circuit is shown in Fig. 4.

The readout design is similar to Kinetic Inductance Detector (KID) based readouts with the notable feature of a large 2.5 GSps sampling frequency of the baseband digitizing electronics. In contrast to KID readouts used for imaging which continuously interrogate the microresonator array, the FASTR readout only measures the array state after completion of a shift register operation cycle. The ~35% duty cycle reduces the data rate to a level at which the Field Programmable Gate Array (FPGA) used for signal processing can continuously sustain. As previously mentioned, the center frequency of the 2.5 GHz of readout bandwidth should be adjustable in order to compensate for any global shift in the detector frequencies. For the current system, global shifts up to ±750 MHz can be tolerated by adjusting the local oscillator frequency. This limit is imposed by the 4-8 GHz operating band of the commercial microwave components used in the readout chain.

Other constraints are imposed when integrating FASTR devices (Fig. 1) into the D-Wave Two quantum processor, which utilizes a multilayer fabrication stack consisting of 6 niobium metal layers separated by planarized dielectric layers. A particular challenge is to realize FASTR devices with this multilayer stack that achieve sufficiently high intrinsic quality factors $Q_i$. The linewidth requirement discussed previously dictates that the microresonator quality factors $Q_i$ are of order $f_0/\Delta f = 6.9/19.569 \approx 300$. In order achieve full signal modulation and minimize processor heating due to dissipation by the FASTR readout, it is desirable for $Q_i$ to be as high as possible. Achieving the limit $Q_i \gg Q_s$ has the added advantage that $Q_s$ is then simply determined by the coupling to the microwave circuit and can be easily set in design with the coupling capacitance $C_c$.

The primary source of dissipation in superconducting microresonators has been extensively studied, and low-loss microresonators made of interdigitated capacitors on crystalline substrates routinely achieve intrinsic quality factors exceeding a million. For example, one technique that is commonly used to improve the $Q_i$ of planar interdigitated capacitor is to increase the finger spacing which decreases the participation ratio of the surface defects.

Compared with single-layer microresonator designs on a crystalline substrate, microresonators incorporating deposited dielectrics suitable for integration in a multilayer fabrication stack typically exhibit much higher loss due to the presence of two-level systems (TLS) in the amorphous dielectric. In this case, simple geometric changes such as increasing the finger spacing of an interdigitated capacitor do not result in an improved device $Q_i$ as the electric field is displaced but remains within the lossy deposited dielectric. Fortunately, these dissipation pathways become saturated above a critical electric field, such that $Q_i$ increases with drive power. In this case, by minimizing the dielectric volume used for fabricating the resonator dielectric, saturation can be achieved for a minimal stored resonator energy. This allows high intrinsic quality factors and minimal heating to be achieved for modest microwave drive powers.

Considering the need to minimize the volume of lossy dielectric, a parallel plate geometry with a minimal dielectric thickness is particularly suitable for the integrated FASTR design. Finally, a lumped-element geometry utilizing a parallel-plate capacitor comes with the added advantage that, as opposed to distributed resonator geometries, no harmonics are inherent in the design. This allows the readout to occupy more than a single octave of bandwidth which is an important consideration for scaling to large array sizes.

CHARACTERIZATION OF A PROTOTYPE DEVICE

We have designed, fabricated, and measured a prototype FASTR detector suitable for integration with the D-Wave Two quantum processor. The layout and fabrication stack are shown in Fig. 6. Testing was performed at 10 mK. The detector resonance frequency with zero flux in either SQUID loop was measured to be 6.91 GHz. This is a large but still acceptable 300 MHz above the design value and attributable to fabrication variation in the capacitor dielectric layer thickness. While only a single prototype FASTR detector was characterized in this initial measurement, the multiplexed readout system shown in Fig. 5 was used for electrical readout while operating at the full 2.5 GSps data rate.

The fabricated prototype device featured a parallel plate capacitor with a nominally 50 nm thick sputtered silicon oxide dielectric. $S_{21}$ transmission data were taken and fit to the expression for a transmission line shunted
required for the 32-resonator design, above the saturation threshold $Q_s$ increases dramatically.

Fig. 4 also shows how the resonance frequency changes with drive power (blue triangles) in units of linewidths according to $a = (f'_0 - f_0) Q_s / f_0$, where $f'_0$ is the low-power resonance frequency. This non-linear response to stored energy is characterized by the Duffing oscillator non-linearity parameter $a = (\alpha Q_s / 4 (1/L_s))^2$. Here, $\alpha = L_J / (L_q + L_J)$ characterizes the contribution of the Josephson Junction kinetic inductance $L_J = \Phi_0 / 2 \pi L_t$ to the total inductance, $I$ is the current through the resonator, and bifurcation occurs at $a \sim 0.77$ linewidths. Keeping the microwave drive power sufficiently low assures only minimal nonlinearity ($a < 0.25$ linewidths) and well-behaved detector operation. This requirement sets the upper bound to the operable region labeled in Fig. 7. The lower bound is set by the a minimum desired amplitude SNR of 5 which gives a bit error probability less than $10^{-6}$. We have measured the system noise temperature to be 7.9 K, limited primarily by the first stage amplifier and the insertion loss of the cryogenic isolators used to prevent amplifier back-action from disturbing the processor. The microwave drive power should exceed $P_g = -96$ dBm to achieve the desired SNR assuming the tone is fully modulated by the 1 linewidth resonance shift. Full modulation is achieved by requiring $Q_t \gg Q_c$ and biasing symmetrically around the resonance, which maps the two qubit states onto the resonance curve as shown in Figure 8a.

**FASTR READOUT OF A QUBIT STATE AND NOISE**

As a proof-of-principle of full-system operation, the prototype FASTR detector was used to readout a qubit via the three-stage shift register shown in Fig. 6. The detector was driven at $P_g = -98$ dBm ($a = 0.05$...
linewidths), slightly below the SNR = 5 lower limit of the operable region indicated in Fig. 7. A large positive flux bias applied to the qubit, followed by annealing, allows for preparation in a known state. Using a large negative flux bias allows the qubit to be prepared in the opposite state. After qubit annealing, the resulting state can be passed along the shift register and read out with the FASTR detector. Repeating this procedure many times with a known data pattern allows the readout fidelity to be assessed. A plot of the measured fidelity data is shown in Fig. 8a, where a linear transformation to the complex transmission has been applied to simplify state discrimination. This process of transformation and discrimination was applied to all subsequent qubit measurements. From the fidelity data, a bit error probability of $\sim 10^{-5}$ was calculated, which matches well with expectation for the device parameters and the microwave drive power utilized. Note that while an SNR < 5 is sufficient for verification of this prototype device, the measurement power will be properly adjusted before full processor readout to ensure the desired bit error probability of $< 10^{-6}$ is achieved.

The previous measurements validate the operation of a FASTR detector and the readout system. It is now possible to repeat two of D-Wave’s standard qubit characterization measurements: a qubit population measurement and a noise power spectral measurement (PSD). [44, 45] The qubit population measurement was made while sweeping the qubit flux bias through degeneracy, with the results shown in Fig. 9a. The fit was done with the equation

$$P = \frac{1}{2} \left[ 1 + \tanh \left( \frac{\Phi_x}{2W} \right) \right],$$

where $\Phi_x$ is the externally applied flux and $2W$ is the width of the transition. Inverting this fit gives a mapping between qubit population and $\Phi_x$. When annealed at a fixed bias point near the center of the transition, on average the qubit population should always return the same value. However, noise will cause the population to wander. Repeated measurement of the population and conversion into an equivalent external flux allows a noise PSD to be calculated. The result of this measurement using the prototype FASTR detector is shown in Fig. 9b. The noise spectra show a combination of $1/f$ noise and white noise $w_n$, where $w_n = \tau_n 4W^2$. The $1/f$ noise component is due to intrinsic device noise, and the white noise is due to the statistical nature of the qubit measurement and drops with increased sample rate or a narrower transition width. Note that traditional DC-SQUIDs are dissipative. Fast operation of these devices results in an increased sample temperature and consequently a wider transition width $W$. This heating can be reduced by increasing the time per sample $\tau_n$. However in either case $w_n$ is increased [44, 45]. Thus the low dissipation and fast duty cycle allowed by a FASTR detector results in a low white noise level as compared with a DC SQUID readout.

**PERSPECTIVE ON READOUT SCALING**

Scaling of the FASTR readout is constrained by the achievable device $Q_i$, available readout bandwidth, and the number of analog wires required to tune the individual resonance frequencies. Based on commercially available electronics, the FASTR array was designed for a 2.5 GHz band centered around 6 GHz. Placing resonators at the ends of each shift register street, the number of resonators for the D-Wave processor goes as $N_{cells} = 4 \sqrt{N_{qubits}}$. Table I shows the scaling of the per-resonator bandwidth and required device $Q_i$ for a fixed 2.5 GHz bandwidth readout design. Figure 7 shows that for the SiO$_2$ dielectric used for the prototype device, a $Q_i$ of $\sim$6,000 was achieved in the operating regime. Increasing the number of devices per line beyond $\sim$48 thus requires incorporation of lower loss deposited dielectrics.

| $N_{qubits}$ | $n_{cells}$ | $n_{res}$ | $\Delta f$ (MHz) | $Q_i$ | $N$ |
|--------------|-------------|-----------|------------------|------|----|
| 512          | 64          | 32        | 19.5             | $\sim$370 | 4  |
| 1152         | 144         | 48        | 13.0             | $\sim$600 | 5  |
| 2048         | 256         | 64        | 9.8              | $\sim$740 | 6  |
| 3200         | 400         | 80        | 7.8              | $\sim$1000 | 6  |
| 4608         | 576         | 96        | 6.5              | $\sim$1110 | 6  |

**TABLE I:** Scaling of the FASTR readout scheme with the size of processor. $N$ is the number of additional analog wires required as discussed in the text. The stated $Q_i$ assumes the need to meet the condition $Q_i \gg Q_c$ to minimize chip heating and design effort.
such as hydrogen-rich amorphous silicon.

A straightforward way to scale the readout is to increase the readout bandwidth. Already, digitizing components with bandwidths exceeding 5 GHz and sufficient dynamic range are commercially available. As the design here utilizes a parallel-plate capacitor incorporated in a lumped-element resonator geometry which does not exhibit harmonics, more than one octave of bandwidth can be readily utilized. Perhaps the greatest difficulty for implementing large bandwidth electronics is the very high data rates that must be handled by the signal-processing hardware. Fortunately, very large FPGAs are becoming available that should be sufficient for this task.

Each FASTR device requires two external flux biases. $2n_{\text{res}}$ lines will be needed if each of these are supplied with individual analog lines. A 32-resonator system would require already a somewhat impractical 64 analog lines. As a better alternative, the D-Wave Two processor uses superconducting digital-to-analog flux converters to apply flux biases to thousands of devices through an addressing scheme that scales as $O(\sqrt{2n_{\text{res}}})$. For instance, a 96-resonator system would require the addition of only 6 analog lines using this addressing scheme, which is far more reasonable than the 192 lines a per-device addressing scheme would require.

CONCLUSION

We have demonstrated a frequency- and sensitivity-tunable resonator detector suitable for a wide variety of magnetic flux sensing applications. The detector tuning parameters allow for compensation of detector-scale fabrication variations, while shifting the center frequency of the readout electronics allows for compensation of wafer-scale variations. Using a combination of these two techniques, the resonator frequencies can be spaced uniformly and a homogenized flux-sensitivity can be realized. In this way a maximum packing efficiency can be achieved for a fixed electronic bandwidth. The utility of this device includes readout of the D-Wave quantum processor, SFQ digital circuitry, and indeed any magnetic flux sensing applications requiring arrays of densely multiplexed detectors.

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