First results on SiSeRO devices: a new x-ray detector for scientific instrumentation

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Abstract. We present an evaluation of an on-chip charge detector, called the single electron sensitive read out (SiSeRO), for charge-coupled device image sensor applications. It uses a p-channel metal-oxide-semiconductor field-effect transistor (p-MOSFET) transistor at the output stage with a depleted internal gate beneath the p-MOSFET. Charge transferred to the internal gate modulates the source-drain current of the transistor. We have developed a drain current readout module to characterize the detector. The prototype sensor achieves a charge/current conversion gain of 700 pA per electron, an equivalent noise charge (ENC) of 15 electrons (e−) root mean square, and a full width half maximum of 230 eV at 5.9 keV. Further, we discuss the SiSeRO working principle, the readout module developed at Stanford, and the first characterization test results of the SiSeRO prototypes. While at present only a proof-of-concept experiment, in the near future we plan to use next generation sensors with improved noise performance and an enhanced readout module. In particular, we are developing a readout module enabling repetitive non-destructive readout of the charge, which can in principle yield subelectron ENC performance. With these developments, we eventually plan to build a matrix of SiSeRO amplifiers to develop an active pixel sensor with an on-chip application specific integrated circuit-based readout system. Such a system, with fast readout speeds and subelectron noise, could be effectively utilized in scientific applications requiring fast and low-noise spectro-imagers. © 2022 Society of Photo-Optical Instrumentation Engineers (SPIE) [DOI: 10.1117/1.JATIS.8.2.026006]

Keywords: single electron sensitive read out (SiSeRO); x-ray detectors; front-end read out electronics; x-ray instrumentation.

Paper 21159G received Dec. 8, 2021; accepted for publication Apr. 14, 2022; published online May 26, 2022.

1 Introduction

Charge-coupled devices (CCDs) have been the detector technology of choice in x-ray astronomy for almost 30 years. First flown on the Advanced Satellite for Cosmology and Astrophysics (ASCA)1 in 1993, these detectors have since been used on many missions, including the flagship Chandra X-ray Observatory2 and x-ray multi-mirror mission (XMM)-Newton3 satellites. The next generation of improved CCD detectors are proposed to form a key component of the anticipated instrument suite of future mission concepts including Lynx,4 advanced x-ray imaging satellite ( AXIS),5 and ARCUS.6 Here, the primary benefit of CCDs is their ability to provide good

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time resolution, low-noise, high spatial, and moderate spectral resolution imaging over relatively large focal planes. The CCD detectors aboard Chandra and XMM-Newton have also been shown to operate robustly in space environments for more than 20 years.

While silicon (Si)-based x-ray imagers routinely show excellent performance, and regularly demonstrate an equivalent noise charge (ENC) of <4e⁻, the application case of small pixels (enhanced charge sharing; supporting the high spatial resolution of concepts such as Lynx and AXIS) and low energy response (<500 eV; an energy range of particular interest for all of these mission concepts) would greatly benefit from improved noise performance, preferably to the point where single electrons can be counted with confidence. MIT Lincoln Laboratory (MIT-LL) has matured their x-ray CCD technology substantially in recent years, including the development of a unique Single electron Sensitive readout stage (hereinafter SiSeRO) for CCDs for proof-of-principle measurements. The SiSeRO amplifier comprises a p-channel metal-oxide-semiconductor field-effect transistor (MOSFET) straddling the n-channel of the CCD’s output register (more detailed discussion is given later). When a charge packet is present in the CCD channel beneath the p-MOSFET channel, it modulates the transistor drain current, which can be sensed directly. This amplifier draws on earlier work on floating-gate amplifiers that demonstrated extremely high responsivity and subelectron noise. The working principle of the SiSeRO amplifier is similar in some respects to the successful depleted field effect transistors (DEPFET) sensor developed for the Athena wide-field imager. Both employs an internal depleted gate and charge in the internal gate modulates the transistor current. However, note that DEPFETs are active pixel sensors where each pixel contains its own readout amplifier whereas SiSeRO is the output stage amplifier in CCDs. The charge is clocked from pixel to pixel in the imaging area to the serial register before being readout by the output SiSeRO amplifier.

For current readout devices like SiSeROs, the noise of the output stage critically depends on the conversion gain, \( G_q (\text{pA/e}) \), which determines the signal, and the transconductance, \( g_m (\mu \text{S}) \) of the transistor, which determines the current noise. For a high conversion gain around 1400 pA/e and a transconductance of around 20 \( \mu \text{S} \), values that seem reasonably achievable, the device output stage noise can be as low as 1 electron root mean square (RMS) for 1 MHz of readout speed. In case of SiSeROs, based on a single polysilicon MOSFET, the internal gate minimizes parasitic capacitance on the sense node resulting in a very high conversion gain and thereby minimizing the noise significantly. Further, MOSFETs show larger transconductance per unit area than JFETs (used in CCDs) and especially small MOSFETs can achieve very high signal speeds. On the other hand, the charge packet in the internal gate is unaffected by the readout process since it is not transferred into a heavily doped sense node and can thus be moved around like any charge packet in a CCD. This allows for a wide variety of new detectors and concepts, including repetitive nondestructive readout (RNDR) techniques, which are expected to reduce noise below the 1/e barrier and deep into the subelectron regime. These properties suggest that the SiSeRO concept could in principle improve the noise performance of x-ray CCDs by a factor of 10 and provide subelectron noise and very high-speed (10 MHz pixel rate) performance. In this article, we report the first test results of prototype SiSeROs using readout electronics developed at Stanford University. The working principle of the SiSeROs is demonstrated in Sec. 2, followed by a description of the readout module and the test stand in Sec. 3. Characterization test results of a prototype SiSeRO are discussed in Sec. 4. We summarize the results and the future plans for testing the SiSeROs in Sec. 5.

## 2 SiSeRO Principle and Operation

A simple schematic of our prototype SiSeRO device is shown in Fig. 1(a). As mentioned earlier, it consists of a p-MOSFET transistor (S: source, G: gate, D: drain of the transistor) that straddles the CCD n-channel for charge transfer and charge can be transferred under the transistor and beyond like in a conventional CCD. As the CCD charge packet is transferred beneath the p-MOSFET, into a region that is effectively a buried gate, the charge packet modulates the source-drain current \( I_{DS} \) of the transistor. To have maximum modulation of the transistor current by the electrons from the buried gate, there is an additional trough implant along the buried n-channel that confines the charge packet into a small area. In the prototype SiSeROs manufactured by MIT-LL, the transistor and the CCD n-channel beneath are around 2 \( \mu \text{m} \) in width.

### 2.1 SiSeRO Structure

The SiSeRO amplifier comprises a p-channel MOSFET straddling the n-channel of the CCD. The charge is clocked from pixel to pixel in the imaging area to the serial register before being readout by the output SiSeRO amplifier. For current readout devices like SiSeROs, the noise of the output stage critically depends on the conversion gain, \( G_q (\text{pA/e}) \), which determines the signal, and the transconductance, \( g_m (\mu \text{S}) \) of the transistor, which determines the current noise. For a high conversion gain around 1400 pA/e and a transconductance of around 20 \( \mu \text{S} \), values that seem reasonably achievable, the device output stage noise can be as low as 1 electron root mean square (RMS) for 1 MHz of readout speed. In case of SiSeROs, based on a single polysilicon MOSFET, the internal gate minimizes parasitic capacitance on the sense node resulting in a very high conversion gain and thereby minimizing the noise significantly. Further, MOSFETs show larger transconductance per unit area than JFETs (used in CCDs) and especially small MOSFETs can achieve very high signal speeds. On the other hand, the charge packet in the internal gate is unaffected by the readout process since it is not transferred into a heavily doped sense node and can thus be moved around like any charge packet in a CCD. This allows for a wide variety of new detectors and concepts, including repetitive nondestructive readout (RNDR) techniques, which are expected to reduce noise below the 1/e barrier and deep into the subelectron regime. These properties suggest that the SiSeRO concept could in principle improve the noise performance of x-ray CCDs by a factor of 10 and provide subelectron noise and very high-speed (10 MHz pixel rate) performance. In this article, we report the first test results of prototype SiSeROs using readout electronics developed at Stanford University. The working principle of the SiSeROs is demonstrated in Sec. 2, followed by a description of the readout module and the test stand in Sec. 3. Characterization test results of a prototype SiSeRO are discussed in Sec. 4. We summarize the results and the future plans for testing the SiSeROs in Sec. 5.

### 2.2 SiSeRO Amplifier Design

The SiSeRO amplifier comprises a p-channel MOSFET straddling the n-channel of the CCD. The charge is clocked from pixel to pixel in the imaging area to the serial register before being readout by the output SiSeRO amplifier. For current readout devices like SiSeROs, the noise of the output stage critically depends on the conversion gain, \( G_q (\text{pA/e}) \), which determines the signal, and the transconductance, \( g_m (\mu \text{S}) \) of the transistor, which determines the current noise. For a high conversion gain around 1400 pA/e and a transconductance of around 20 \( \mu \text{S} \), values that seem reasonably achievable, the device output stage noise can be as low as 1 electron root mean square (RMS) for 1 MHz of readout speed. In case of SiSeROs, based on a single polysilicon MOSFET, the internal gate minimizes parasitic capacitance on the sense node resulting in a very high conversion gain and thereby minimizing the noise significantly. Further, MOSFETs show larger transconductance per unit area than JFETs (used in CCDs) and especially small MOSFETs can achieve very high signal speeds. On the other hand, the charge packet in the internal gate is unaffected by the readout process since it is not transferred into a heavily doped sense node and can thus be moved around like any charge packet in a CCD. This allows for a wide variety of new detectors and concepts, including repetitive nondestructive readout (RNDR) techniques, which are expected to reduce noise below the 1/e barrier and deep into the subelectron regime. These properties suggest that the SiSeRO concept could in principle improve the noise performance of x-ray CCDs by a factor of 10 and provide subelectron noise and very high-speed (10 MHz pixel rate) performance. In this article, we report the first test results of prototype SiSeROs using readout electronics developed at Stanford University. The working principle of the SiSeROs is demonstrated in Sec. 2, followed by a description of the readout module and the test stand in Sec. 3. Characterization test results of a prototype SiSeRO are discussed in Sec. 4. We summarize the results and the future plans for testing the SiSeROs in Sec. 5.

### 2.3 Characterization of SiSeROs

The SiSeRO amplifier comprises a p-channel MOSFET straddling the n-channel of the CCD. The charge is clocked from pixel to pixel in the imaging area to the serial register before being readout by the output SiSeRO amplifier. For current readout devices like SiSeROs, the noise of the output stage critically depends on the conversion gain, \( G_q (\text{pA/e}) \), which determines the signal, and the transconductance, \( g_m (\mu \text{S}) \) of the transistor, which determines the current noise. For a high conversion gain around 1400 pA/e and a transconductance of around 20 \( \mu \text{S} \), values that seem reasonably achievable, the device output stage noise can be as low as 1 electron root mean square (RMS) for 1 MHz of readout speed. In case of SiSeROs, based on a single polysilicon MOSFET, the internal gate minimizes parasitic capacitance on the sense node resulting in a very high conversion gain and thereby minimizing the noise significantly. Further, MOSFETs show larger transconductance per unit area than JFETs (used in CCDs) and especially small MOSFETs can achieve very high signal speeds. On the other hand, the charge packet in the internal gate is unaffected by the readout process since it is not transferred into a heavily doped sense node and can thus be moved around like any charge packet in a CCD. This allows for a wide variety of new detectors and concepts, including repetitive nondestructive readout (RNDR) techniques, which are expected to reduce noise below the 1/e barrier and deep into the subelectron regime. These properties suggest that the SiSeRO concept could in principle improve the noise performance of x-ray CCDs by a factor of 10 and provide subelectron noise and very high-speed (10 MHz pixel rate) performance. In this article, we report the first test results of prototype SiSeROs using readout electronics developed at Stanford University. The working principle of the SiSeROs is demonstrated in Sec. 2, followed by a description of the readout module and the test stand in Sec. 3. Characterization test results of a prototype SiSeRO are discussed in Sec. 4. We summarize the results and the future plans for testing the SiSeROs in Sec. 5.
while the trough implant is around 500 nm. For a reasonable number of electrons in the internal gate (<10,000), the modulation of the transistor current is proportional to the amount of charge in the buried gate. Charge can be transferred out of the buried gate with a suitable clocking of the surrounding gates. For readout, the p-MOSFET external gate is set to a DC bias and is used to adjust the current through the p-MOSFET to an optimum signal-to-noise condition.

Figure 1(b) shows the detector package that was used for testing. The test devices are available in two packages, denoted as CCID85E and CCID85F, each having four different variants of SiSeRO positioned at the four corners of the package. The variants can have different gate structures of the p-MOSFET and different trough locations within the internal channel. For example, the troughs can be located either at the center of the channel or toward the source or drain of the transistor. This feature available in the test devices allows to understand the effect of the trough location in maximizing the modulation of transistor current and complete charge transfer in and out of the internal gate, which will have significant impact on the overall performance of the devices. The detectors are fabricated in an n-channel CCD, using a low-voltage, single-poly process with two metal layers. The imaging area of the detector is ~4 mm × 4 mm in size, with a 512 × 512 array of pixels (nominal pixel size 8 μm). The prototype SiSeRO detectors are currently front-illuminated devices. In Fig. 1(a), S3 and OG stand for the third (or last) serial clock at the output stage, and the output gate, respectively. OG is set to a DC bias to move the charge from S3 to beneath the p-MOSFET. The charge packet is eventually drained to reset drain (RD), which is set to a high positive DC bias, using a reset clock (RG). On the packaged devices, the source and drain of the amplifier are brought directly out of the package. This enables the device to be operated in a drain- (or source-) current readout mode where the drain (or source) current is read out by an external readout electronics module. For our testing, we characterized two different SiSeROs: one has the trough implant closer to the drain, the other one has the trough implant located at the center of the CCD channel.

3 Characterization Test Stand and Readout Module

Here, we give a brief description of the characterization test stand, followed by a discussion on the readout module developed to characterize the SiSeROs. The same test stand has been used earlier in our laboratory to characterize fast, low-noise x-ray CCDs for astronomical applications. The details of the test stand and its components are discussed in Ref. 16. Here, we give only a brief description of the setup.

The experimental set-up is shown in Fig. 2. The detector housing is compact in size (13 cm × 15 cm × 6.5 cm). A narrow slot in the side flange is used to epoxy the preamplifier board. There is a mounting socket (a 19 × 19 position PGA ZIF socket from 3M) for the detector
We cut out a square section from the central region of the socket such that the backside of the device package is in direct thermal contact with an aluminum cold block. The detector is clamped against it with a metal plate from the top to improve the thermal contact. A thermoelectric cooler (TEC), installed inside the chamber, is used to cool down the device package. A proportional-integral-derivative controller loop is employed to adjust the current of the TEC and thereby control the temperature of the device with an accuracy better than 0.2°C. A water-cooled plate at the bottom flange dissipates the heat from the hot side of the TEC. There is a small x-ray entrance window, made of a 500 \( \mu \text{m} \) thick beryllium disc (95% transmission of 5.9 keV photons) in the top flange directly above the detector, to allow x-ray photons from the calibration source to characterize the detector. The other side of the board is connected to an Archon CCD controller\(^\text{17}\) (the black box in Fig. 2). The controller will be described in more detail below.

### 3.1 Readout Module

The readout module is composed of two blocks: a preamplifier that reads the SiSeRO drain current and converts it to a fully differential analog voltage signal and the Archon controller digitizer, which samples, digitizes the fully differential analog voltage signal, and estimates the charge signal amplitude for each pixel. Below, we discuss the preamplifier circuit and the simulation results, followed by a brief description of the Archon controller.

Figure 3(a) shows the schematic of the preamplifier circuit. It has two stages: an I2V amplifier to convert the SiSeRO drain current to an analog voltage signal, followed by a differential analog to digital converter (ADC) driver to produce a fully differential output voltage signal. For the I2V stage, we use a single-ended operational amplifier (an ADA4817 from Analog Devices\(^\text{18}\)). The drain of the p-MOSFET is connected to the inverting input of the amplifier. The voltage at the output of the amplifier is proportional to the SiSeRO drain current \( I_{\text{drain}} \), where \( R_3 \) is the feedback resistor. We provide a DC bias to the drain of the p-MOSFET using \( V_{\text{drain}} \), through the non-inverting input of the ADA4817. \( V_{\text{subtraction}} \) is a DC bias connected to the SiSeRO input that is used to add or subtract excess current in order to adjust the output voltage offset within the allowed voltage swing of the ADA4817. In the second stage, for the differential ADC driver, we use an AD8138 from Analog Devices.\(^\text{19}\) A gain of unity is implemented in this stage. At the output, we get a differential analog signal, \( IN+ \) and \( IN− \), which is fed to the ADC driver of the Archon controller. Although our primary focus here is to demonstrate that SiSeROs can be read...
In drain current readout mode with reasonable noise and spectral performance, the amplifiers in the circuit design were chosen such that both the amplifiers have large bandwidths, in order to support high readout speeds. The ADA4817 has extremely small input capacitance, resulting in a low $RC$ time constant for the circuit. However, due to the large parasitics of the printed circuit board (PCB) setup, the overall bandwidth in the current design is limited by the compensation of the I2V to around 6 MHz. The ADA4817 and the AD8138 both feature low voltage noise densities ($<5\text{nV/}\sqrt{\text{Hz}}$), which ensures the low noise performance of the setup.

We simulated the preamplifier circuit using the LTspice simulator. Figure 3(b) shows the results of a transient simulation for a 500 kHz pulsed input current signal (shown in red). The output from the I2V amplifier is shown as a solid black line, with the inverting and non-inverting outputs of the ADC driver shown as dashed black and dashed-dot black lines, respectively. The circuit bandwidth of 6.7 MHz has been obtained by running a small-signal AC simulation [shown in Fig. 3(c)]. The bandwidth is limited by the $RC$ time constant of the I2V amplifier feedback, whose selected values are needed for stability ($1/2\pi RC \approx 6.4$ MHz). We also performed voltage noise simulations of the circuit in LTspice. The simulation results indicate an input referred current noise density of around 1.5 pA/√Hz. Consequently, the integrated noise floor is 1.5 nA in a 1 MHz bandwidth, which is also equivalent to an ENC of $\sim 2e^-$. The preamplifier board is connected to the Archon controller through an interface board that routes the clock and biases from the internal Archon modules to the detector, whereas at the same time the detector analog outputs from the preamplifier board are routed to the differential ADC inputs on the Archon controller.
The Archon controller, procured from Semiconductor Technology Associates, Inc. (STA), is a Field Programmable Gate Array or FPGA-based CCD controller, which provides the necessary bias (in the range $-14$ to $31$ V) and clocks (14-bit 100 MHz) to the detector, digitizes the detector outputs (using 16-bit 100 MHz ADCs), and estimates the charge signal for each pixel to generate the image. The Archon receives configuration information about the detector bias, clocking sequence, and sampling of digitized waveforms from a host PC and then returns image data via a gigabit Ethernet connection. More details on the Archon controller can be found in Ref. 21. The total (current) signal gain of the implemented drain readout chain is 376 analog digital units (ADU) per $\mu$A of input current. For the prototypes under test here, we estimate around 2 W of power consumption for the clocks and $<100$ mW for the readout stage at $\sim 500$ kHz readout speed.

4 Characterization of the SiSeROs

We characterized two variants of SiSeROs—one with the trough implant located at the center of the channel, and the other where the trough implant is located closer toward the drain. Understanding the effect of the trough and its location on the charge transfer is essential to mature the design of SiSeROs in the future. The device was cooled down to 250 K ($-23^\circ$C) to minimize leakage current. We characterized the detector at 500 kilo-pixel per second read out rate. The clocking sequence (and thereby the readout speed) of the serial register clocks is defined in a timing script inside the Archon Configuration File. The charge packet is first transferred from the imaging region to the serial register of the detector using a three electrode imaging clock sequence (at 400 kHz). The charge in the serial register is moved across the serial gates, $S_1$ to $S_2$ and $S_2$ to $S_3$ sequentially, to the OG, and finally to the depleted internal channel beneath the p-MOSFET. After the charge is read out, an RG drains the charge packet to an RD kept at high DC potential.

Figure 4(a) shows an oscilloscope output from different stages of the readout module. The black line is the analog output of the I2V amplifier. The green and the blue lines are the non-inverting and inverting outputs of the differential ADC driver (AD8138), respectively. The readout speed is set at 500 kHz. Each pixel in the detector generates this type of signal at the output. Figure 4(b) shows the digitized waveform from the Archon controller as a solid red line. The RG and $S_3$ clock, synchronized with the waveform, are shown in solid gray and dashed gray lines, respectively. The waveform can be seen to have three distinct features. It starts with a reset of the internal channel, shown by a large spike in the signal. Following the reset, the output settles to a baseline level. A charge packet is transferred from $S_3$ to the internal channel through the OG.

![Fig. 4](image-url)

(a) Oscilloscope output from the first stage I2V amplifier (black) and the ADC driver (green and blue). (b) The output waveform (red solid line plotted against the right axis) obtained from the Archon controller along with the reset, $r_g$ (solid gray line) and $s_3$ (dashed gray line) clocks. The shaded regions represent the baseline ($s_3$ is high, internal gate empty) and video ($s_3$ is low, charge in internal gate) signals that are used for CDS filtering. The video signal starts with charge transfer from $s_3$ (when $s_3$ is low) to the internal gate through the OG. The reset plateau region starts when $r_g$ sets to baseline.
when $S_3$ is low. This can be seen as a small peak in the signal. The difference in the signal levels before and after the charge transfer is proportional to the transferred charge. A correlated double sampling (CDS) function in the Archon software calculates the charge for each pixel from the two signal levels to generate the detector images. Image cleaning and processing, event selection, generation of spectra, and estimation of the noise and spectral resolution are carried out using Interactive Data Language event processing software.

### 4.1 Optimization in Biasing Parameters

We characterized a SiSeRO p-MOSFET transistor to understand its behavior and optimize biasing conditions $S$, $D$, and $G$ for the transistor. Fine tuning the bias of the OG, RD, and the RG (low and high) is important to assure complete charge transfer to the internal channel and that there is no back injection of charge to the channel. We used an off-centered SiSeRO for detailed characterization. Since the transistors in all the SiSeRO variants are identical, we expect similar I-V behavior for them.

Characterization of the transistor was done for three different source voltages ($V_{SS}$): 4, 5, and 6 V, whereas the source-drain ($V_{DS}$) voltages were kept fixed at 5 V. For each source bias, two different values of OG and RG Low, RGL (0 and 2 V) were used. For each bias setting, we obtain the drain current ($I_{\text{drain}}$) from the analog output of the I2V amplifier as seen from an oscilloscope [see Fig. 4(a)], and known values of the $V_{SS}$, $V_{DD}$, and $V_{\text{subtraction}}$ voltages and the bias resistors (see the schematic). Gate voltage ($V_{GG}$) was varied from +4 to $-6$ V in each case. Figure 5(a) shows the drain current as a function of gate voltage for different biasing conditions.

The top, middle, and bottom panels correspond to $V_{SS}$ values of 4, 5, and 6 V respectively, whereas the OG and RGL potentials are shown in different colors, e.g., red (OG: 2 V, RGL: 2 V), blue (OG: 2 V, RGL: 0 V), and green (OG: 0 V, RGL: 2 V). In a p-MOSFET, we expect the drain current to start flowing when the gate bias is negative and above a certain threshold in order to form the inversion channel. However, we see that even at $V_{GG} > 0$ V, there is a certain amount of drain current for some values of OG and RGL, particularly when they are low, which implies that there might be a parasitic path between the source and the drain, either along the OG or the reset gate. Slightly positive values for OG and RGL are required to minimize the parasitic current as shown in Fig. 5. We obtain the required bias for RGL and OG from the $I - V$ characteristics of the transistor such that at $V_{GG} > 0$ V, the drain current is close to zero, as shown by the gray

![Fig. 5](image-url) (a) The p-MOSFET drain current as a function gate voltage, OG and RGL bias for three different source voltages: 4 V (top), 5 V (middle), and 6 V (bottom). The gray dashed lines are for the 0 μA drain current level in the transistor. We optimize these parameters to find the SiSeRO operating region. (b) Optimization of the RGH bias, showing the noise with RGH for three different source voltages: 4 V (green), 5 V (blue), and 6 V (red). See text for details.
Table 1
Summary of the biasing conditions of SiSeROs.

| Bias potentials       | $V_S = 4$ V, $V_D = -2$ V | $V_S = 5$ V, $V_D = -1$ V | $V_S = 6$ V, $V_D = 0$ V |
|-----------------------|---------------------------|---------------------------|---------------------------|
| Output gate (OG) (V)  | +0.5                      | +1                        | +1.8                      |
| Serial clock (SL, SH) (V) | -1, +2                  | -1, +2.5                  | -1, +3.5                  |
| Reset (RGL, RGH) (V) | +0.5, +6.5                | +1, +6.5 V                | +2, +7.5                  |
| Reset drain (RD) (V)  | +14                       | +14                       | +14                       |

...dashed lines in Fig. 5(a). In Table 1, we give the optimum bias conditions for OG and RGL at each source voltage. Values of the serial clock potentials ($SS_{11}$ High, $SS_{22}$ High, $SS_{33}$ High) depend on the bias of OG such that $SS_{11}$, $SS_{22}$, and $SS_{33} >$ OG.

RGH (reset high) and RD should be positive with respect to the channel potential such that there is no back injection of charge to the internal channel. While RD is kept at high DC potential, with RD > (RGH + channel potential), to determine the required RGH bias, we reset the internal channel soon after the charge transfer ($SS_{33}$ is low) in the presence of x-ray photons on the detector. The CDS filtering is done between the regions before $SS_{33}$ is low and after the second reset. At an optimum RGH bias, we do not expect to see any x-ray photons in the detector images, unless there is back injection of charge to the internal channel. To quantify this, we measure the noise in the imaging region by varying the RGH potential such that at an optimum bias setting for RGH, the noise is minimum because of minimum or no back injection of charge. This is shown Fig. 5(b), where we plot the estimated noise in ADU as a function of RGH for different $VV_{SS}$ values. RD was kept at +14 V, which is the maximum DC bias available from the Archon low voltage modules. The test was done for each source voltage while OG and RGL were kept at their respective optimum potentials. The bias condition for RGH for optimum performance of the SiSeROs is given in Table 1.

4.2 Noise and Spectral Performance

Read noise of the system is estimated from an overclocked region of 50 × 512 pixels, by calculating the standard deviation in charge distribution of the pixels. The noise estimated from the overclocked region includes noise sources from the external readout circuit and the output stage amplifiers. For the centered trough SiSeRO, we estimate the read noise to be around $15e^{-}rms$ for the optimum values of the bias parameters. In the case of the off-centered trough, the read noise is, in general, relatively higher. The best read noise that we achieved in this case is around $17e^{-}rms$. The noise contribution from the PCB side readout electronics to these measurements is estimated to be less than $2e^{-}rms$. The white noise contribution of the SiSeRO is also estimated at around $2e^{-}rms$, implying that the SiSeROs under test exhibit excess noise, possibly because the MOSFETs are surface channel and therefore are subjected to excess 1/f noise.

We used a $^{55}$Fe radioisotope to evaluate the spectral performance of the detectors with 5.9 keV (Mn $KK_{\alpha}$) and 6.4 keV (Mn $KK_{\beta}$) x-ray photons. We take 200 frames with 0 ms acquisition exposure. However, note that there is a default exposure of around 500 ms in order to readout the entire frame of 512 × 512 pixels. For estimation of dark current, around 100 dark frames are taken at the same exposure and temperature. The x-ray images are generated after applying bias correction (subtraction of the overclocked region at 0 ms integration) and dark frame correction (subtraction of dark frames corresponding to the same time integration used for x-ray images) to the raw images. An event selection logic, based on user-defined primary and secondary pixel charge thresholds, is implemented on the entire detector plane to generate graded spectra. Here, we used a primary threshold of seven times the read noise and a secondary threshold of 2.6 times the read noise. Figure 6 shows a small zoomed-in region of one of the raw frames with x-ray photons. The image is scaled (see the scale at the bottom in ADU) such that the primary and secondary pixel amplitudes can be compared with the background noise in ADU. The average background noise is centered around 1300 ADU with standard deviation of around 4 ADU. The secondary pixel values in ADU, as can be seen from the image, are well above the secondary threshold used in our analysis. Since we do not see any noisy pixels in the detector.
plane, there is no bad pixel filter applied for the generation of event list. Figures 7(a) and 7(b) show examples of spectra for the centered and off-centered SiSeRO troughs, respectively.

The spectra shown here were generated with the single pixel (grade 0) events with optimum biasing conditions of the S, D, and G. Because of significant charge sharing in 8 μm pixels, we find only 10% of the total events contribute to the grade 0 events. The Mn Kαα (5.9 keV) and Kββ (6.4 keV) lines are fitted with two Gaussian functions (shown in red solid lines) to estimate the gain and FWHM. The 5.9 keV FWHM values are estimated to be around 230 and 240 eV for the centered and off-centered SiSeRO, respectively.

In Fig. 8, we summarize the spectral and noise performance of the SiSeROs for various source (VVSS), drain (VVDD), and gate (VVG0) voltages. We plot the fitted Gaussian centroid for the 5.9 keV lines in the top panel, read noise in ADU, and electrons in the middle two panels, and 5.9 keV line FWHM in the bottom panel; as functions of drain current and the corresponding gate voltages in the left and right column, respectively. The triangles and crosses stand for the centered and off-centered troughs, respectively. Three different source and drain voltages (VSS = 4 V and VDD = −2 V, VSS = 5 V and VDD = −1 V, VSS = 6 V and VDD = 0 V) are shown in green, red, and blue, respectively. We note a few interesting observations from Fig. 8:
1. Noise, gain (proportional to the centroid), and FWHM can be modeled solely with drain current, irrespective of the source and drain voltages. For both the variants, the gain and the output current noise initially increase with drain current, which is expected. However, when the drain current is high, the gain levels off and declines slightly, whereas the current noise falls strongly. The input referred read noise in electrons therefore first worsens with increased current, but then quickly improves for larger bias currents. As the measured x-ray FWHM is primarily contributed by the total noise, it also follows the same trend. We are currently investigating this noise behavior. Potential issues could be the fact that these devices are surface channel MOSFETs and that they exhibit some parasitic leakage current around the transistor structure.

2. The centered trough SiSeRO variant exhibits higher gain and better noise performance compared to the off-centered trough variant. In our readout, the off-centered trough is located closer to the drain, and therefore the current gain from the charge in the internal gate is reduced. For \( V_S = 4 \), the gain and noise are worse for the off-centered variant but improve with more positive source potential. This is likely due to the fact that the actual physical trough location below the MOSFET is dependent on the surrounding potentials and, for higher positive source potentials \( V_S > 4 \), the location of the most positive potential pocket moves toward the source and therefore improves the gain. Device simulations of the SiSeROs will give better understanding of the observed results.

Fig. 8 Spectroscopic and noise performance of the SiSeROs at various biasing conditions. Peak centroid of the 5.9 keV lines in ADU (top), read noise in ADU (second row), read noise in electron RMS (third row), and 5.9 keV line FWHM (bottom) are plotted against the p-MOSFET drain current (left column) and the corresponding gate voltages (right column). In the plots, the triangles and the crosses stand for the centered and off-centered trough, respectively. Different colors stand for various biasing conditions (refer to Table 1).
5 Summary and Future Plans

SiSeROs are unique output stage amplifiers for x-ray CCDs with potential of very low noise and high speed performance. At the same time, SiSeROs can also enable a broad range of innovative image sensors to be designed, including many small-area arrays, or even single-cell CCDs, where every pixel contains an individual output stage. In this article, we discussed the working principle of the amplifier and the concept of the drain current readout module developed at Stanford. We reported the first results from a prototype SiSeRO and demonstrated that the concept is sound and can be manufactured in the single poly CCD process at MIT-LL. For the optimum biasing conditions, the ENC of the prototype is around 15 electron RMS and the FWHM at 5.9 keV is $\sim 240$ eV.

In future work, we plan to mature the SiSeRO technology through a series of laboratory experiments and simulations, exploring modifications to improve the overall noise and speed performance of the detectors, e.g.,

1. The prototype SiSeRO device we produced and tested is a surface channel transistor. In this case, we expect the Si/SiO$_2$ interface states to capture and release mobile carriers, causing excess noise. Therefore, we plan to test a buried transistor channel SiSeRO where the inversion layer forms some distance below the Si/SiO$_2$ interface.

2. We will combine prototype measurements with three-dimensional device simulations to improve our device modeling for a deeper understanding and improved designs.

3. It might be possible to utilize RNDR for SiSeROs by moving the charge packet multiple times between the internal channel and OG. An advantage of RNDR or repetitive readout of the same charge packet is that a non-white noise (specifically $1/f$ or pink noise) can be significantly attenuated, resulting in extremely low noise. This technique has been successfully demonstrated for DEPFET devices with subelectron read noise yield.

4. Parallel to our SiSeRO research and development, we are developing an application specific integrated circuit (ASIC). This will enable device readout with fewer parasitics, resulting in higher performance and offering a high channel count in a small footprint, which will be particularly useful for large, high speed x-ray imagers. The application specific design will bring a significant reduction in power consumption while offering custom diagnostic and calibration features designed to help tune the sensors to deliver optimal performance. An eight-channel ASIC prototype designed in a 350-nm process node is currently in fabrication.

There is a substantial potential to utilize SiSeROs in the development of fast, low noise spectroscopic imagers for next generation x-ray astronomy missions, and a broad range of other scientific applications.

Acknowledgments

This work has been supported by NASA grants APRA 80NSSC19K0499 “Development of Integrated Readout Electronics for Next Generation X-ray CCDs” and SAT 80NSSC20K0401 “Toward Fast, Low-Noise, Radiation-Tolerant X-ray Imaging Arrays for Lynx: Raising Technology Readiness Further.” We are deeply saddened by the passing of our colleague and co-author Barry Burke. His contribution has helped in the advancement of the X-ray CCD technology. We will miss him as a colleague and above all as a kind human being.

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