A jitter suppression technique against data pattern dependency on high-speed interfaces for highly integrated SoCs

Tsuyoshi Ebuchi\textsuperscript{a)}, Taku Toshikawa, Seiji Watanabe, Tomohiro Tsuchiya, Yutaka Terada, Tomoko Chiba, Keijiro Umehara, Toru Iwata, and Takefumi Yoshikawa

System LSI Business Division, Panasonic Corporation,
1 Kotari-Yakimachi, Nagaokakyo, Kyoto 617–8520, Japan
\textsuperscript{a)} ebuchi.tsuyoshi@jp.panasonic.com

Abstract: This paper proposes a jitter suppression technique for a high-speed interface macro by decreasing the disturbance onto a power node of the macro. The power node fluctuates in accordance with the output data pattern from the macro. Namely, it becomes lower at the dense data pattern and returns near to an initial value at the sparse data pattern. This fluctuation causes the jitter and deteriorates the data eye on the output node. The proposed scheme relaxes the dense and sparse pattern dependency by decreasing the fluctuation. Simulation results show a significant suppression of i) the power node fluctuation from 20 mV to 8 mV, and ii) the jitter from 160 ps to 60 ps on the data eye. Clear data eye openings were obtained at various data rates on actual measurements.

Keywords: jitter, high-speed interface, data eye, power noise

Classification: Integrated circuits

References

[1] B. Leibowitz, R. Palmer, J. Poulton, Y. Frans, S. Li, J. Wilson, M. Bucher, A. M. Fuller, J. Eyles, M. Aleksic, T. Greer and N. M. Nguyen: IEEE J. Solid-State Circuits 45 (2010) 889. DOI:10.1109/JSSC.2010.2040230

[2] VESA Embedded DisplayPort Standard Version 1.3.

1 Introduction

Recent consumer electronics products require higher speed data communication as an amount of necessary digital data is increasing year by year \[1\]. For example, display data is becoming to 4 times at a transition of generation from Full HD to 2K4K. To cope with rapid increase of the data rate, recent System-on-Chips (SoCs) have high-speed interface macros with Giga-bits per second (Gbps) class band-
width and scalable multiple lanes, e.g. embedded Display Port (eDP) and PCI Express (PCIe). In these high speed interface macros, a specified amount of the jitter is allowed to keep compliances for interface standards [2]. However, it is very difficult to suppress the jitter within the specifications especially in highly integrated SoCs of advanced process technologies, because a sensitivity of the power node fluctuation is increasing in accordance with a technology scaling (lower VDD and shorter cell delay) of VLSIs.

In this paper, a novel jitter suppression technique, which is suitable for highly integrated SoCs, is proposed with revealing the relationship of jitters and output data patterns in a high speed interface.

2 Jitter generation mechanisms

Figs. 1(a) and 1(b) show data eye openings at the output node of eDP macro in a highly integrated SoC using experimental PRBS (Pseudo Random Bit Stream) pattern and actual 4B5B coding pattern, respectively. The data rate is 1.5 Gbps. Though a good eye opening is obtained at the PRBS pattern in Fig. 1(a), the significant degradation of an eye opening is observed in the actual 4B5B coding pattern used in AV consumer electronics as shown in Fig. 1(b).

Fig. 1 (a) Experimental PRBS Pattern (b) Actual Pattern (4B5B)

Fig. 1. Data pattern dependency on data eye openings

Fig. 2(a) exhibits a fluctuation of the bit interval at the output data in the time domain on actuals measurements. X-axis exhibits serial bit numbers of an incoming data stream, and Y-axis shows a deviation from an ideal bit-time reference (0.0UI) in each bit of the data stream using Unit Interval (UI).

As shown in this figure, a jitter is occurred on the data eye in every 30 bits at 1.5 Gbps. It means that the jitter period is 20 ns, i.e. 1UI (667 ps) × 30 bits. An analysis in the frequency domain using an FFT methodology is exhibited in Fig. 2(b). A peak is investigated at 50 MHz. As explained by the measurement results in Figs. 3(a) and 3(b), the jitter on the eye is occurred by a noise at 50 MHz.

To search any periodic noise at 50 MHz, simulations were executed to monitor internal nodes of the macro using actual 4B5B coding. Fig. 3 shows the simulation results of the data pattern, an internal power node (1.1 V) and ground node in the macro.
As depicted in Fig. 3, the data pattern has cyclic dense and sparse periods in actual 4B5B coding, and these periods occur every 20 ns (= 50 MHz). Without a package model in simulations between power pads of the macro and a power source (1.1 V), the internal power node fluctuates about 20 mV and does not have any specific frequency. However, after inserting the LCR structure as the package model, the fluctuation enlarges to about 100 mV with 50 MHz frequency. This noise frequency is same as the cyclic dense and sparse periods.

Fig. 4(a) depicts the LCR network for the package model, the SoC and the PC board. A resonance frequency roughly can be calculated by a following equation using the power node capacitance ($C_{int}$) in the SoC, wire and line inductance ($L_p$) of the package and line inductance ($L_n$) of the board.

$$f_r = \frac{1}{2\pi \sqrt{LC_{int}}}$$

$L = L_p + L_n$
To obtain a value of the inductance \((L)\), a power node for the macro (1.1 V) has been specified in an actual BGA (Ball Grid Array) package as shown in Fig. 4(b). In the power node (VDD), total 6 bonding wires are allocated between power pads of the macro and an internal power plane of the package. The power plane is connected to external 4 solder balls of the BGA package through 4 layers package substrate. The package inductance \((L_p)\) has been extracted with referencing the package structure of Fig. 4(b) by quasi-static electromagnetic solver. As for the inductance \((L_n)\) between the external solder balls and the external decoupling capacitor \((C_{ext})\) on the board, the S-parameter model has been extracted by full-wave electrical analysis.

These extracted parameters for \(L_p\) and \(L_n\) have been analyzed on 3D full-wave electromagnetic solver. As a result, the \(L\) is 3.24~3.77 nH at the worst case (the largest \(L\) case) with considering a production tolerance. As for the power node capacitance \((C_{int})\), we assume 2 nF from chip layout of the macro.

Fig. 5 shows the characteristic of an impedance over frequency for the model of Fig. 4(a). The resonance frequency has been calculated as follows using the above equation.

\[ f_r = \begin{cases} \frac{1}{2\pi\sqrt{CL}} \\ \frac{1}{2\pi\sqrt{C\int L}} \end{cases} \begin{align*} i) & f_r = 58.0 \text{ MHz}, \text{ where } C_{int} = 2 \text{ nF and } L = 3.77 \text{ nH,} \\ ii) & f_r = 62.5 \text{ MHz}, \text{ where } C_{int} = 2 \text{ nF and } L = 3.24 \text{ nH} \end{align*} \]
As shown in Fig. 5, the resonance frequency is assumed as 58\textasciitilde62 MHz, which is near to the disturbance frequency caused by the 4B5B pattern. Due to the resonance effect, the power node fluctuation has been enlarged to about 100 mV.

It is concluded that the jitter on the data eye opening comes from the power node fluctuation, which frequency is at almost 50 MHz. The fluctuation is caused by an injected noise onto the power node, and enlarged through the resonance of the LCR network at the power node in the package and SoC. The injected noise is produced by the cyclic dense and sparse periods on the data pattern.

3 Jitter suppression techniques

To suppress the power node fluctuation, it is a straightforward approach where the resonance frequency is intentionally moved by inserting decoupling capacitor (increase \(C_{\text{int}}\)) and adding extra VDD pads & balls (decrease \(L\)). However, these methods are just a symptomatic treatment and its effectiveness is not ascertained until actual measurements. Because the disturbance frequency caused by the dense and sparse periods on the data pattern is strongly depending on data streams in the actual usage, and may be changed by applications and data rates.

We propose another concept with a Transmitter of Fig. 6 where additional data transients are automatically generated during the sparse periods and to move the disturbance frequency near to a half of the data rate.

In the Constant Dynamic Power Transmitter (CDPT) of Fig. 6, the Parallel-to-Serial Converter (P/S) and the Pre Driver consume the dynamic power on the power node (\(VDD_{\text{macro}}\)) as the Normal Path during the dense periods.

On the other hand, the additional data transients are generated in the Data Transient Generator (DTG) and fed to the Dummy Driver for driving the Dummy Load during the sparse periods. The DTG and the Dummy Driver, which compose the Replica Path, produce dynamic current loads onto \(VDD_{\text{macro}}\) during the sparse periods to generate similar conditions as during the dense periods.

By cooperation of the Normal Path and the Replica Path, the total dynamic power of the Transmitter becomes constant regardless of the dense/sparse data pattern and the fluctuation of \(VDD_{\text{macro}}\) can be suppressed significantly.
The Off-Chip-Driver (OCD) performs a differential current driving onto external transmission lines, and its power is fed through a constant current source from the power node \( V_{DD\_OCD} \). Therefore, the dynamic power of the OCD is also constant and the fluctuation of \( V_{DD\_OCD} \) is very small. Therefore, the dynamic power of the CDPT is constant, and its power nodes \( V_{DD\_macro} \) and \( V_{DD\_OCD} \) are stable against the data pattern dependency.

Figs. 7(a) and 7(b) illustrate a circuit diagram and waveforms for the DTG. When original data streams (DT) from the P/S stays at 0 or 1 for more than 2 bit times, positive pulses (PFF) is generated by XNOR operation between the current (DTL) and the next (DT) bit of the original data streams. While ‘PFF’ is high, data transients are generated at an output node (TFF) by oscillation at every bit time through XOR operation. As shown in Fig. 7(b), ‘TFF’ has the data transients only when ‘DT’ does not change its data polarity. Therefore, extra data transients are inserted only in the sparse periods.
4 Simulation and measurement results

Figs. 8(a) and 8(b) show simulation results with and without the CDPT. Fig. 8(a) represents the power node fluctuation. Green and yellow lines are with and without the CDPT, respectively. Though the overall level of power node becomes statically lower at a condition with the CDPT, the dynamic power node fluctuation has been suppressed from 20 mV to 8 mV thanks to the CDPT. Fig. 8(b) exhibits a jitter at a signal cross-point on the data eye. The jitter has been suppressed from 160 ps to 60 ps because of decrease for the power node fluctuation.

![Fig. 8. Simulation results](a) Power Node Fluctuation (b) Jitter on the Data Eye

Fig. 9 shows measurement results of the data eye with the CDPT. As exhibited in the figure, clear eye openings have been obtained at various data rate.

![Fig. 9. Measured data eye with the CDPT](a) 270Mbps  (b) 1.5Gbps  (c) 3Gbps

These results show that the proposed scheme has a scalability for the data rate and its effectiveness is proven for the actual usage of consumer AV electronics.

To be considered effective, the CDPT should work on discrete power and ground nodes (VDD\_macro and VSS\_macro), which are completely separated from others power and ground nodes in the SoC. However, the power and ground nodes are usually allocated separately to analog and interface macros in highly integrated SoCs in order to avoid performance degradations of the macros due to noise.
interferences. Therefore, it is not an actual design constraint in highly integrated SoCs.

The CDPT requires an additional power of almost 1 mW at 1.5 Gbps in each lane, namely about 8 mW will be increased as power consumption at 8 lanes configuration. This additional power consumption will be surely traded with the high tolerance of jitters against power supply fluctuations in an unknown power supply network, and also considered negligible in comparison with the overall power consumption of the order of watts for highly integrated SoCs.

5 Conclusion

The proposed scheme can suppress the jitter by decreasing the power node fluctuation. The proposed circuit (CDPT) inserts data transitions into the sparse pattern period to move the disturbance frequency away from the resonance frequency of the LCR network on the power node. Significant jitter suppressions and data eye openings have been observed in simulations and actual measurements at various data rates.

This scheme increases the power consumption due to dummy data transitions. However, this scheme is still applicable and has scalability for various applications with appropriate data rates, and thence very suitable for highly integrated SoCs with advanced process technologies.