Exploiting Nanoelectronic Properties of Memory Chips for Prevention of IC-Counterfeiting

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Abstract—This study presents a methodology for anti-counterfeiting of Non-Volatile Memory (NVM) chips. In particular, we experimentally demonstrate a generalized methodology for detecting (i) Integrated Circuit (IC) origin, (ii) recycled or used NVM chips, and (iii) identification of used locations (addresses) in the chip. Our proposed methodology inspects latency and variability signatures of Commercial-Off-The-Shelf (COTS) NVM chips. The proposed technique requires low-cycle (∼100) pre-conditioning and utilizes Machine Learning (ML) algorithms. We observe different trends in evolution of latency (sector erase or page write) on cycling with different NVM technologies from different vendors. ML assisted approach is utilized for detecting IC manufacturers with 95.1% accuracy obtained on prepared test dataset consisting of 3 different NVM technologies including 6 different manufacturers (9 types of chips).

I. INTRODUCTION

Counterfeiting of Integrated Circuits (ICs) is a significant concern for the semiconductor supply chain [1]. Reliability and security issues of counterfeited or degraded Non-Volatile Memory (NVM) chips have the potential to threaten various sectors such as automotive, defense/security, medical devices, consumer electronics, etc. [1], [2]. Variation in nanoscale properties of different NVM technologies occurs due to variation in underlying nanostructures and nanomaterials. Various invasive and non-invasive techniques exist in literature which can be employed on Commercial-Off-The-Shelf (COTS) chips to detect IC origin [3] or recycled ICs [1], [2], [4], [5]. In addition, other security primitives like chip identity information, memory-based Physical Uncloneable Functions (PUFs) [6], True Random Number Generator (TRNG) [7], etc. are implemented to track NVM chips. However, most of these techniques are proposed for NAND Flash memory [2] or DRAM [3] chips. Moreover, detailed chip characterization and maintenance of large database for ascertaining COTS NVM chip authenticity is cumbersome. Techniques like physical inspection, statistical analysis [2], introduction of extra circuitry [4], etc. for counterfeit IC identification are either heftily or ineffective when involving many variants of NVM chips, or require modification in CMOS circuitry during fabrication. Significant advancement in Machine Learning (ML) techniques facilitates employing ML algorithms for counterfeit IC detection [8]. In this study, we present a non-invasive anti-counterfeiting technique based on exploiting the nanoelectronic phenomena (switching time variability) of COTS NVM chips. In particular, we exploit latency (for sector erase/page write operation) to provide a solution for (i) identification of the IC manufacturer, and (ii) recycled IC detection for conventional and emerging NVM technologies. The key contributions of this paper are:

1) A generalized methodology to identify (a) NVM chip manufacturer, (b) recycled NVM chips, and (c) used locations on the chip.
2) The identification methodology exploits the switching time variability of NVM chips and requires ∼100 program/erase cycles to be performed on the chip.
3) Generation of custom dataset to train an ML based classifier that can effectively determine IC origin/manufacturer.

The rest of the paper is organized as follows: Section II provides an outline of NVM technologies used. Experimental results and discussion are presented in Section III. Section IV concludes the paper.

II. OUTLINE OF NVM TECHNOLOGIES USED

NOR Flash memory technology utilizes Metal-Oxide-Semiconductor (MOS) structure with a stacked-double-poly Floating-Gate (FG). The gate is bounded by a dielectric material and electrically controlled by a capacitive-coupled-Control-Gate (CG). The working principle of NOR Flash memory is based on threshold voltage (Vth) modulation of FG transistor. During program operation [WordLine (WL)
and BitLine (BL) = positive, source = ground], electrons are trapped into the FG through the dielectric by Channel-Hot Electron (CHE) injection mechanism. During erase operation (WL = ground, BL = float, source = positive), electrons are detrapped from the FG following the Fowler–Nordheim (FN) tunneling mechanism. This trapping (high Vth) and detrapping (low Vth) results in changing of Vth of the FG transistor (high Vth = logic “1,” and low Vth = logic “0”) [shown in Fig. 1(a)] [9]. A particular class of emerging Resistive Random Access Memory (RRAM) technology with metal-insulator-metal device structure, Conductive-Bridging Random Access Memory (CBRAM), works on the formation and dissolution of Conductive Filament (CF). Applying voltage of specific polarity across the device terminals results in formation of CF as a consequence of diffusion and reduction of ions/defects. Applying voltage of reverse polarity (for bipolar devices) leads to dissolution of the CF [Fig. 1(b)]. Formation and dissolution of the CF switch the devices to Low-Resistance State (LRS/ON) and High-Resistance State (HRS/OFF), respectively. The state of the device (HRS/LRS) exhibits the bit stored in the memory cell [10]. Another class of RRAM technology consists of metallic layers or stacks as top and bottom electrodes and a metal oxide insulating layer interposed between the electrodes (metal-oxide-metal structure). The working of these RRAM technologies is based on (i) migration of oxygen ions (ii) thermal dissolution. Initially, the fresh devices are formed due to soft dielectric breakdown and drifting of oxygen ions towards the anode. CF is formed in the bulk oxide due to either oxygen vacancies or metal precipitates [11]. During the programming operation (LRS) current flows through the CF to the electrodes. During erase operation (HRS), oxygen ions migrate back to the bulk leading to filament breakdown due to recombination [as shown in Fig. 1(c)] [11].

### III. EXPERIMENTAL RESULTS AND DISCUSSION

#### A. Experimental Setup

The test setup consists of a soft-core processor implemented on an FPGA evaluation board. The processor performs program and erase operations on the NVM chip. The NVM chip is connected to FPGA board through PMOD connectors. Detailed description of the experimental setup is provided in [12]. Extensive experiments are performed on different SPI based NVM chips i) NOR Flash, ii) CBRAM, and iii) RRAM from multiple vendors (listed in Table I) at room temperature with identical operating conditions. Latency measurements for sector erase operation in NOR Flash and page write operation in CBRAM and RRAM chips are performed by monitoring the Write-In-Progress (WIP) bit [12] in the status register. Erase latency is measured by performing continuous 4kB sector erase operations. Page write latency is measured by initially programming a page with a known data value, followed by programming it with a new data value having bit-flips at particular locations. The latencies of NVM chips are measured successfully as the switching time variations of NVM devices (within ms or µs) used for our study are within the range of the time resolution of our setup (10 ns).

#### B. Electrical Characterization Results and Analysis

Fig. 2(a)-(d) shows the evolution of measured latency values for different NVM chips with cycling (50k cycles). Difference in evolution pattern of the obtained latency values is observed within different NVM technologies and manufacturers. We observe unique latency signatures on comparing different chips of same NVM technology spread across different memory capacities and manufacturers. We also compare the latency signatures among different NVM technologies. The possible reasons for uniqueness in signature may be: variation in chip architecture, technology node, layout design, material stack, process (PVT) variations, etc. [1], [3]. The distinctiveness in latency evolution patterns can thus be used as a fingerprint to predict the NVM chip origin.
TABLE II

| Feature selection technique | ML algorithm | Test accuracy (%) | Inference time (s) | Training time (s) |
|-----------------------------|--------------|-------------------|-------------------|------------------|
| No feature selection (All 100 features) | Decision Tree | 86.1 | 0.0545 | 389.39 |
| | KNN | 95.1 | 0.1957 | 748.43 |
| | Gaussian SVM | 90.1 | 0.72 | 971.31 |
| MRMR test (25 features) | Decision Tree | 87.9 | 0.0346 | 89.54 |
| | KNN | 91.7 | 0.09 | 120.11 |
| | Gaussian SVM | 89.0 | 0.1125 | 332.09 |
| NCA (25 features) | Decision Tree | 89.2 | 0.034 | 98.74 |
| | KNN | 92.4 | 0.0785 | 123.66 |
| | Gaussian SVM | 88.5 | 0.1286 | 315.93 |

We observe that all types of chips can be predicted quite accurately. We utilize our ML classifier to build a swift IC-counterfeiting detection methodology that can predict the actual manufacturer of a given NVM chip by performing ~100 program/erase cycles at any location on the chip, and measuring the latency values in each cycle. These values are then passed to our ML classifier for predicting the actual chip type.

Further, we extend the technique to identify used locations in the NVM chip. To experimentally validate the concept, we generate used locations artificially by carrying out 1k, 5k, 10k, 20k, 30k, and 50k program/erase cycles at random locations. We measure individual latency values in between actual manufacturer of a given NVM chip by performing 1k, 5k, 10k, 20k, 30k, and 50k program/erase cycles at random locations. We measure individual latency values in between 100 program/erase cycles at any location on the chip, and measuring the latency values in each cycle. These values are then passed to our ML classifier for predicting the actual chip type.

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multiple classes of NVM chips. In future extensions of this work, we would like to extend the proposed methodology to predict the range of usage (number of program/erase cycles performed) of the used locations. This can be achieved using the magnitudes of obtained latency values of the predicted chip type. We would also like to explore additional features like current consumption and advanced pattern recognition techniques based on deep neural networks.

IV. CONCLUSION

We present an anti-counterfeiting technique for detecting IC origin (capacity and manufacturer) and recycled (or used) chips, along with used locations. The proposed methodology exploits intrinsic property variations within NVM COTS chips. We experimentally illustrate that latency and variability can be used to detect counterfeit NVM chips. Finally, we present ML based approach for detecting authentic IC manufacturers with high accuracy. A dedicated dataset through experimental characterization is also developed for conventional and emerging NVM technologies to train the ML classifier to high accuracy.

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