Bidirectional automatic release of reserve for low voltage network made with low capacity PLCs

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Abstract. The article presents the design of a bidirectional automatic release of reserve made on two types low capacity programmable logic controllers: PS-3 from Klöckner-Moeller and Zelio from Schneider. It analyses the electronic timing circuits that can be used for making the bidirectional automatic release of reserve: time-on delay circuit and time-off delay circuit (two types). In the paper are present the sequences code for timing performed on the PS-3 PLC, the logical functions for the bidirectional automatic release of reserve, the classical control electrical diagram (with contacts, relays, and time relays), the electronic control diagram (with logical gates and timing circuits), the code (in IL language) made for the PS-3 PLC, and the code (in FBD language) made for Zelio PLC. A comparative analysis will be carried out on the use of the two types of PLC and will be present the advantages of using PLCs.

1. Introduction
Electrical consumers of particular importance such as: steel casting cranes, underground mining ventilation fans, groundwater discharge pumps, electrical consumers in hospital operating rooms, etc., shall be provided with the continuity of supply with electricity. For this purpose, these consumers must be connected to at least two independent power sources with the same or different powers [1], [2].

If the power sources have equal powers and each source can provide the necessary electrical power for the proper operation of all connected consumers, the continuity of the power supply is achieved by means of bidirectional automatic release of reserve (ARR). To this goal, each source is the reserve of the other, but in order to eliminate the pervious effect of the supply between the two sources, when operational, one of them is considered as a priority, which is, usually, the source I. Eliminating the instability of the ARR system is done by using a time-on delay relay when actuated when the automaton is made with classical switching devices or with an electronic timing circuit with time-on delay, when static commutation elements are used when the control system is being used [3], [4].

In the paper there is presented a bidirectional ARR [5], which has the control system made in four variants, namely: with classical switching devices (Figure 4.a), with logical circuits of TTL or made in CMOS technologies (Figure 4.b), and timing devices with time-on and time-off delays (Figure 4.c), PLC type PS-3 and PLC type Zelio, variants have been experimented.

2. Time circuits used in control installations of ARR made on PS-3 PLC
In the ARR control system made with static commutation elements, time-on and time-off delayed electronic time circuits, made on the PLC type PS-3, which are presented below [6-9].
2.1. Time-on circuit made on PS-3 PLC

In order to achieve electronic time circuits with different time functions on the PS-3 PLC, this PLC has 32 timers (time-on delay) that have TR0 ... TR31 addresses with programmable working time in the range of 0.1 ... 6553.5 s. The time-on function is basic, because by using it all the usual time functions can be made on the PS-3 PLC. The timer TR1 has been used to achieve the timer operation. The timer setting is made with the input size I0.1. The STP (stop timing) function was not blocked, the working time \( t_a = 4 \) s (KW40) was set and the output was set to Q0.1. When the time circuit serves a control system, the input and output may, also, be internal memory signals.

For the initial time \( t_0 \), the signals I0.1 and Q0.1 have the 0 logic value (Figure 1.c), the I0.1 button is not actuated, the TR1 of the time relay is not powered, its contact in circuit 3 is open and the signal light H1 is off (Figure 1.a).

After the time \( t_0 \), push button I0.1 (I0.1 = 1) is energized with voltage the TR1, but during operation time \( t_a = 4 \) s of the timing relay, the normally open contact (n.o.c.) with time-on delay Q0.1 in circuit 3 remains in the normal state (Q0.1 = 0), after which it closes (Q0.1 = 1), and the H1 signaling light turns on. This state is maintained until I0.1 (I0.1 = 0) opens, the TR1 coil voltage is off, Q0.1 opens and H1 is turn off.

![Figure 1. Achieve timing function at time-on delay; a. Schematic diagram of the function using a classic timed relay; b. Block diagram of the timing circuit; c. Input signals I0.0 = f_1(t) and output Q0.1 = f_2(t) of the time-on delay circuit](image)

The time-on delay program on PS-3 PLC

```
000 TR0
TR0*S: I0.1
TR0*STP : TR0*IW : KW40
TR0*EQ : Q0.1
```

2.2. Time-off delay circuit on PS-3 PLC with the classic installation

To achieve the program on the PS-3 PLC, the schematic diagram of the classical switching elements are in Figure 2.a [6, 7]. The input and output sizes for this function are I0.1 and Q0.2. In the initial state, button I0.2 (I0.2 = 0) is not actuated during \( t_0 \) (Figure 2.c), the relay is turn off, Q0.2 (Q0.2 = 0), the signaling lamp H2 is turn off, and the signals M0.0 and M0.1 have the 0 logical value.

When pushing button I0.2 (I0.2 = 1), Q0.2 = 1 occurs, H2 lights on, Q0.2 = 1 is stored by closing the n.o.c. Q0.2 in circuit 3. Open normally close contact (n.c.c.) I0.2 of circuit 4, closes n.o.c. Q0.2 of the same circuit, so M0.0 = 0 and n.o.c. M0.0 in circuit 4 remains open, so there is no voltage supply to the TR2 timing relay coil, so M0.1 = 0 and its n.c.c. with opening delay (normally close contact with opening timing – n.c.c.o.t.) remains closed. This condition takes a while.

After time \( t_x \), I0.2 = 0, open n.o.c. I0.2 of circuit 2, but is closed n.c.c. Q0.2 of circuit 3 (Figure 2.a). Closes n.c.c. I0.2 of circuit 4, resulting M0.0 = 1, closes n.o.c. M0.0 of circuit 5 and works TR2 which after \( t \), open n.c.c.o.t., M0.1 of 2 circuit, which causes the lamp H2 to turns off, M0.0 = 0,
M0.1 = 0 and return to the initial state of the n.c.c.o.t. M0.1. Using the control system with the principle diagram in Figure 2.a, program was made on PS-3 PLC.

![Control System Diagram](image)

**Figure 2.** Performing the time-off delay function: a. Scheme diagram using a classical control; b. The circuit blocks of the time-off delay circuit; c. Input signals I0.2 = f₁(t) and output Q0.2 = f₂(t) of the time-off delay circuit

**The time-off delay program on PS-3 PLC (using Figure 2a)**

|   |   |   |
|---|---|---|
| 001 L I0.2 | 007 = M0.0 |
| 002 O Q0.2 | 008 TR2 |
| 003 A NM0.1 | TR2*S : M0.0 |
| 004 = Q0.2 | TR2*STP : |
| 005 L NI0.2 | TR2*IW : KW60 |
| 006 A Q0.2 | TR2*EQ : M0.1 |

Using this program, the time-off delay is 6 s (KW60).

2.3. **Time-off delay circuit with PS-3 PLC and STP command timer**

The schematic diagram of this circuit is given in Figure 3 [6-9], the variations of the input signals I0.3 f₁(t) and output Q0.3 = f₂(t) are those shown in Figure 2.c, in which I0.2 and Q0.2 are replaced by I0.3 and Q0.3.

![Time-Off Delay Circuit Schematic](image)

**Figure 3.** Schematic diagram of the electronic time-off delay with flip-flop R-S circuit, CBB-RS and timer STOP

When changing the signal value I0.3 (I0.3 = 0, S = 0), the state of the signals from the input of the flip-flop RS circuit (CBB-RS) is I0.3 = 0 (S = 0) and M0.2 = 0 (R = 0), but Q0.3 continues to have the 1 logic value due to the previous values of the S and R signals (S = 1, R = 0). Now, the TR3 timer is released which has the working time t_w, after which M0.2 = 1 (R = 1) as a result of Q0.3 = 0 (Q = 0), M0.2 = 0, so, S = 0, R = 0, and Q is maintained at the previous logical value.

**The time-off delay program on PS-3 PLC (using Figure 3)**
Due to the simplicity of design of the time-off delay time function, using the program, when making the bidirectional ARR, the electronic circuit in Figure 3 and the associated program are used.

3. The logical functions of the bidirectional automatic release of reserve

This ARR [5] has the diagram scheme of the main installation given in Figure 4.a. (power diagram), Figure 4.b. (classical control diagram), and Figure 4.c. (control system made with static commutation elements). Basically, the marking of the elements has been done for some of them, according to STAS 11381/83 and 88, and for others, with that recognized by PS-3 PLC.

The logical functions of the classic control device (Figure 4.b), with the marking of the switching devices, recognized by PS-3 PLC, are:

\[
M0.3 = 10.3 \cdot (I0.4 + M0.3) \\
M0.0(t_{al}) = M0.3 \\
M0.1(t_{al}) = M0.3 \cdot I0.1 \\
M0.2(t_{al}) = M0.3 \cdot I0.2 \\
Q0.1 = M0.3 \cdot I0.5 \cdot M0.1(t_{al}) \cdot M0.7(t_{al}) \cdot Q0.2 \\
M0.4(t_{al}) = M0.3 \cdot Q0.1 \\
Q0.2 = M0.3 \cdot I0.6 \cdot M0.0(t_{al}) \cdot M0.2(t_{al}) \cdot M0.4(t_{al}) \cdot Q0.1 \\
M0.7(t_{al}) = M0.3 \cdot Q0.2
\]

With these functions and taking into account the easiest configuration (Figure 3) of the electronic circuit with time-off delay, the ARR control principle was established with static commutation elements (Figure 4.c). For the TR0, TR1, TR2 electronic time-on delay circuits, output values are transmitted to the internal memories M0.0, M0.1, and M0.2. The electronic time-off circuits, with the TR3 and TR4 active elements, have outputs M0.4 and M0.7.

At the bidirectional ARR system, source I is the priority. When the source I falls, or one of the phases of the I-st source is interrupted, it is not deactivated for 2 s as the working time \(t_{al}\) of the timer TR1 (Figure 4.c). If the supply voltage returns during this time, the consumers continue to remain connected to the source I. If after 2 s there is no voltage at the contactor terminals Q0.1 it is triggered and after the working time \(t_{al} = 1\) s to which the TR3 timer is set, the contactor Q0.2 is activated and the source II is activated.

When the source II is activated, the passage of the power supply from the source I goes in the same way, but in this case other logic and timing circuits occur. When passing the power supply from another source to another, if the voltage of the damaged source returns, the last voltage source remains on.
4. Bidirectional ARR operation with logic integrated circuits

In the initial state, if there is voltage on each phase of sources I and II, the relays K3, K4, K5, and K6 are actuated, therefore the normally open contacts of the K4 and K6 relays are closed, the signals I0.1 and I0.2 from the inputs INVERSORS 7 and 10 have logical value 1, so M0.1 = 0, M0.2 = 0, and after INVERSORS 5 and 8, M0.1 = 1, M0.2 = 1. These signals are applied to the inputs 2 and 4 of the AND 1 and 13 circuits. Since the F1 and F2 protections are not actuated, the signals I0.5 and I0.6 have 0 logical value, and after INVERSORS 11 and 16, I0.5 = 1 and I0.6 = 1 and the signals applied to the inputs 3 and 6 of the AND 1 and 13 circuits.

Running the ARR in operation occurs when I0.4 = 1 and I0.3 = 0, then after INVERSOR 3, a = 1, after OR 4, b = 1 and after I0.4 = 0. Signal M0.3 = 1 unlocks the AND 1, 13, 6, 9, 15, and 18 gates. Because Q0.1 = 0 and Q0.2 = 0, after INVERSORS 19 and 20, Q0.1 = 1 and Q0.2 = 1. These signals are applied to the inputs 1 and 5 respectively of the AND 13 and 1 gates. After CBB-RS2, M0.7 = 0, at the INVERSOR 17 output M0.7 = 1 applied to the input 4 of the AND circuit 1. And after CBB-RS1, M0.4 = 0 So at the output of the INVERSOR 14 M0.4 = 1, the signal applied to the input 5 of the AND gate 13. The M0.3 = 1 validation signal of the ARR operating state is applied to the input of the timing circuit TR0, set to operate after 5 s, consequently during this time, the signal M0.0 = 0 applied to the input 2 of the AND 1 gate, blocks this gate. It is noted that on all the inputs of the circuit AND 1 the signals have the logic value 1, so Q0.1 = 1, and Q0.2 = 0 so the source I is activated by actuating the
contactor Q0.1. After INVERSOR 19, a signal that blocks the gate AND 13 and after the TR0 timer works when M0.0 = 1. The TR0 timer ensures stable ARR system operation.

The signal Q0.1 = 1 also applies to the second input of the AND gate 15, so M0.11 = 1 (S = 1). Since M0.5 = 0 (R = 0) at CBB-RS1, S = 1 and R = 0, so M0.4 = 1 and M0.4 = 0 at INVERSOR 14 output and at input 5 of AND 13 gate. Specifies that the M0.4 = 1 signal does not work of the TR3 timer to operation because at the STP input M0.11 = 0. This time circuit provides a delay of 1 s when the power supply passing from the source I to the source II.

When the source I falls or the voltage drops on one of the phases, for example from phase S, the relay K3 with the coil in circuit 1 (Figure 4.a) triggers, the contact K3 from the circuit 6 is open on the relay coil circuit K4 from circuit 7, which causes the logic value of the signal I0.1 (I0.1 = 0) to be changed from the control system (Figure 4.c.), after the AND signal M0.9 = 1, the TR1 timer is activated after the time t_a1 = 2 s due to M0.1 = 1, so M0.1 = 0 from INVERSOR 5 output and input 2 of circuit AND 1, Q0.1 = 0. The signal Q0.1 = 0 causes the contact Q0.1 to trip and the main contacts in the circuit 4 (Figure 4.a) is deactivated source I, Q0.1 = 1 at the INVERSOR 19 output and on the input 1 of the circuit AND 13. Q0.1 = 0 is applied to the input 2 of the AND circuit 15, so M0.11 = 0. Now on S and R CBB-RS1 circuit, the signals have 0 logical values, but Q = 1 due to the previous state of the signal on R and S. Since M0.11 = 0 the STP command is cancelled, the TR3 timer works and after the adjusted time t_r1 = 1 s, the signal R = 1. Now S = 0 and R = 0, so Q = 0 (at CBB-RS1 input and TR3). The signal M0.4 = 1 at input 5 of the AND circuit 13 causes the signal value to change Q0.2 (Q0.2 = 1).

Now the power supply to the consumers is made from the source II by actuating the contactor Q2 with the main contacts in the circuit 11 (Figure 4.a). After INVERSOR 12, Q0.2 = 0 (interlock signal) is applied to the input 5 in the AND circuit 1 and blocks this gate. The signal Q0.2 = 1 is also applied to the input 2 of the AND circuit 18, after which M0.6 = 1 (S = 1). Because M0.8 = 0, R = 0. For this state of the signals M0.6 and M0.8 (S = 1, R = 0) at CBB-RS2 output M0.7 = 1 (Q = 1), so after INVERSOR 17, M0.7 = 0, which is applied to the input 4 in the AND circuit 1. This signal provides a delay of 1 s when receiving the power supply command from the source II to the source I. Operation of the timer TR4 is blocked by the signal M0.6 = 1.

When the source II falls, switching the power to the consumers from the source I takes place just as in the previous situation, but in this case other logic circuits and timing are used. When disabling a source occurs as a result of the complex protection (I0.5 or I0.6), the contactor is instantaneously switched on, after which the timed switch (1 s) takes place at the power supply from the backup source.

5. Making Bidirectional ARR Command on PS-3 PLC

Using the schematic of the bidirectional ARR control system made with integrated logic circuits and electronic timers (Figure 4.c), the corresponding program on PS-3 PLC was established. Following program experimentation, it was found that the operation of the control system made on PS-3 PLC is identical to that shown in Figure 4.c [8], [9].
The bidirectional ARR program on PS-3 PLC (using Figure 4.c)

6. Bidirectional automatic release of reserve on Zelio PLC

The PLC Zelio is a smart relay, manufactured by Schneider Electric, used for small automation with a number of inputs/outputs between 10 and 40. The Zelio PLC is available in compact formats (3 single bloc models with 10, 12, or 20 inputs/outputs with or without display) or modular (2 basic models with 10 or 26 inputs/outputs which can be extended either with Modbus or Ethernet modules or using 6, 10, or 14 individual inputs/outputs and 4 analogue extension modules for inputs/outputs). This relay has a wide range of applications in which it can be used, both in industry and construction, and in the field of services [10].

The Zelio PLC has the advantage of being simple to install and program, allowing control and monitoring of installations in any situation, either locally or remotely. It can be programmed in LD (ladder diagram) and FBD (function block diagram). These languages are much easier to use than IL (instruction list) that is used when programming PS-3 PLC. For the design of ARR program, the FBD language was used, the program being performed after the ARR of Figure 4.c.

In Figures 5-14 (the blue connections are 0 logic, the red connections are 1 logic) the FBD program was presented during the ARR operation. To the left are the PLC’s inputs (I1 presence of voltage on the three-phases of the source I, I2 presence of voltage on the three-phases of the source II, I3 is the
ARR stop button, I4 is the ARR start button, I5 is the input from protection to overloading of 
consumers for source I, I6 is the input from the overload protection of consumers for the source II) 
and the outputs (Q1 the supply of the consumers from the source I, Q2 the supply of the consumers 
from the source II). Inputs are digital and use mechanical locking buttons, and outputs are digital 
and supply coils of three-phase contactors to connect consumers to source I or source II. Both sources 
(I and II) used 2 s time-on delays, in which consumers are not disconnected from those sources. If 
the fault persists for more than 2 s, for 1 s, consumers are disconnected from damaged sources. After 
passing the 1 s interval, consumers are switched to the other source, and then remain connected to it 
even if the voltage on the first source returns the three-phases.

![Figure 5. Principle diagram ARR](image)

![Figure 6. ARR operation, consumers are powered from source I](image)
Figure 7. ARR operation, source I damaged, within 2 s

Figure 8. ARR operation, source I damaged, from 2 s to 3 s, consumers are not powered
Figure 9. ARR operation, consumers are powered from source II, source I is damaged

Figure 10. ARR operation, consumers are powered from source II, source I enabled
Figure 11. ARR operation, source II damaged, within 2 s

Figure 12. ARR operation, damaged source II, from 2 s to 3 s, consumers are not powered with voltage
Figure 13. ARR operation, consumers are powered from source I, source II damaged

Figure 14. ARR operation, consumers are powered from source I, source II enabled

7. Conclusions
The important electrical loads require power supply from two (or even three) power sources.

The paper presents the sequences code for timing performed on the PS-3 PLC, the logical functions for the bidirectional automatic release of reserve, the classical control electrical diagram, the electronic control diagram, and the code (in IL language) made for the PS-3. The same bidirectional automatic release of reserve has been developed on Zelio PLC (in FBD language).
The control of bidirectional automatic release of reserve power supplies can be achieved using classical control installations or using PLCs (a better solution). In all type of control, the scheme of the power installation can’t be replaced. PLCs can successfully replace classical control system diagram and control system made with elements that have static commutation. They can easily adapt to installations and easily debug/develop applications.

It is easiest to use modern PLCs that can be programmed in FBD (semi-graphical program) compared with PLCs can be programmed in IL (like assembler code).

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