HIGH SPEED VLSI ARCHITECTURES OF FIR FILTERS FOR IMAGE APPLICATIONS - A REVIEW

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Abstract- Numerous applications based on VLSI architectures suffer from large size components that lead to an error at the design stage of floating point arithmetic. Therefore, in the design of a VLSI implementation of FIR filter for various applications such as images increases the design complexity and the time delay effect of the model. This lead to have difficulty of architecture that includes the competing requirements like speed, area, and power, application area specialization and knowledge, changing and evolving terms. In this paper, a brief review of VLSI architectures in the field of image processing is depicted such as compression, interpolation, which will be advantageous in order to tackle the issues caused by the complexity in the design and design an optimal architecture with the necessary factors that need to be satisfied.

Keywords— Finite impulse response; Field Programmable Gate Array; Floating point processing element; Image compression; Image Interpolation; Mantissa & exponent value.

1. Introduction

The development of suitable fabrication technology involves Very Large Scale Integration (VLSI) to both computer scientists and computer architects. The digital systems are subjected to various difficulties because of the development in electronic technology that affect the structure, procedure, methodology and their algorithms. Hence, the design of architecture needs a clear idea about the various aspects that lead to novel architecture of VLSI.

Various applications such as image compression, image interpolation techniques and other methodologies are discussed to analyze the design of architecture. Various types of data are commonly transferred over a network and it leads to a bit traffic because of the bulk data (image and videos). The image and video take up over 40% of the volume of the Internet and it leads to compression technology at a premium. Among various compression standards available, the JPEG image compression standard is widely used. Discrete Cosine Transform (DCT) used to offer an image data but the current image data is based on the Wavelet Transform (WT). The WT has various possible realizations that provide a suitable method to represent images. This is because, the WT represent information at a variety of scales with local contrast change as well as larger scale structures. The finding of unknown points using known points is called as image interpolation. They are commonly used in the increasing and conflicting digital images. The interpolation algorithms are associated to provide different optimizations such as, gate amount, frequency, memory buffer, and power.

The Floating Point Processing Element (FPPE) is an important unit for addition, subtraction, multiplication, etc. of binary data in DSP applications. In arithmetic calculation, most of the system struggles in the floating point number estimation due to its exponential term. The aim is to gain a reduction in power loss and also in the area. In this process, the FPPE help to predict the derivation and integration, operation of that given signal. Several techniques are used to estimate Mantissa value and an exponential term, with minimum usage of logical components for modeling FPPE. The techniques used to estimate has some limitations that lead to increase in memory usage and delay.

The goal of this work is to look at the changed VLSI parameters like power, space, and speed of different executions of the engineering. The exhibition of VLSI engineering in image compression, interpolation and different methodologies are improved with the accompanying examination on existing strategies.
1.1 VLSI Architecture for image compression

The design is a half and half structure that comprises of Discrete Wavelet Transform (DWT) and Field Programmable Gate Array (FPGA) [1]. The DWT depends on hyper ghastly pictures of a lossless pressure framework and FPGA is an inserted framework stage. A product for time execution, pressure calculation is utilized to play out the bury band forecast module by equipment acknowledgment. The structure of the FPGA is equipped for preparing 16.5 M pixels/Sec, goes about as a productive calculation for equipment mapping that prompted high throughput. The upgrade of by and large framework execution is efficiently reachable by a lot of improvement methods. This progressive memory get to plot gives different advantages, for example, an abbreviate information move, restrains the transfer speed of the transport and different coding to streamline the product execution.

The proposed work is depended on the engineering of word sequential pipeline and the equal sifting process [2]. Here, an efficient lifting based designs for the 5/3 discrete wavelet change were talked about. The engineering of equal and pipeline comprises of vertical channel and flat channel, where the framework postpones present in the models get decreased. The total duplications are performed by methods for less moves and different increments in the design prompts a few positive methodologies, for example, basic structure stream, high throughput and capacity. The other writing [3] which present a plan of a Block Coder (BC) framework dependent on picture pressure. It forms 21super pixels/second. Inside a solitary clock cycle during a pass, all of the four model zones is taken care of in Bit Plane Coder (BPC) of concurrent image preparing calculation. An Arithmetic Coder (AC) arranged two (C×D) per clock cycle other than the plan. To accomplish a proficient coupling of the proposed BPC and AC modules, design for a middle of the road cradle is proposed. The Block Coder (BC) chip is actualized at Taiwan Semiconductor Manufacturing Company (TSMC). A 0.18 micrometer innovation, involved a region of 1.6 mm2, which is proportional to the entryway tally of 95000 bits that incorporates 24576 memory bits. This is the most noteworthy preparing throughput at any point expressed for a BC motor that is equipped for dealing with both ordinary and causal methods of activity.

Another procedure [4] proposed a reversible square change in coding for cross breed picture pressure method. The proposed technique is actualized by the choice of coefficients that have a place with various changes. The decoder utilized in the proposed structure doesn't require any further alteration and they are applied to different sorts of pictures. It shows an improved presentation for the chose areas, when the whole arrangement of pictures is dynamic utilizing picture coding techniques. At last, the usage of VLSI proposed strategy is appeared with the portion of Hartley and Cosine change that gives a superior presentation of some other model. The Regions of Interests (ROIs) are executed by a method depend on the choice of coefficients that have a place with various changes. No run of the mill change for JPEG2000 decoder is necessary and it is applied over different sorts of pictures. It shows an improved presentation for the chose areas, when the whole arrangement of pictures is dynamic utilizing picture coding techniques. At last, the execution of VLSI proposed technique is appeared with the portion of Hartley and Cosine change that gives a superior presentation of some other model.

The difficulties of the quick structure and transpose structure present in the registers of a FIR channel is dissected and examined the degree of the register reuse [5]. The prompt structure has less registers than the transpose structure and it offers an expansive register sharing for equivalent execution. The further Look-Up Table (LUT) use and various resources of Distributed Arithmetic (DA) taking into account equivalent FIR channel structures contains the outcome, for instance, input delay, coefficient stockpiling, and constrained item age. They moreover share LUT words, when various direct yields are enlisted in equivalent. Therefore, the observations are used in deducing a DA based plan for reconfigurable square based FIR channel that is versatile to higher square size and greater channel length. The register numbers are on the other hand relating towards the size of the square in the proposed structure. It gives high throughput regard than the present strategies. Application Specific Integrated Circuit (ASIC) result shows the proposed structure for square size not actually the present arrangement, and it give on numerous occasions higher testing rate.
The proposed structure has a square size of 4 and 8 that devours 38% and half less force than the current technique that has a comparative throughput rate for different supply voltages.

1.2 VLSI Architecture for image Interpolation

A survey of various image interpolation algorithms is given by their equipment attributes and visual quality. The equipment qualities, for example, usage of area, speed, and utilization of power are predominantly focused.

1.2.1 Digital Image Scaling Algorithm

The picture addition calculation for both gray scale and shading pictures of any goals in any scaling element is proposed [6]. A cutoff of 4 pixels is used right now. The mix of two factors, for example, the level of area and the distinction of glow between the source pixels assist with computing the last radiance for every pixel. This algorithm uses continuous area filtering and it operates in linear domain area. To attain a fast implementation in real time, it performs in both up and down scale processes.

1.2.2 Winscale Image Interpolation

The computational complexity and the improvement in the quality is the main objective of this interpolation method [7]. In this technique, calculation of multifaceted nature is decreased by the quantity of activities/pixel. This technique performs the two scales up and downsizes change utilizing a territory pixel model as opposed to a point pixel model. Four pixel of a unique picture is utilized to get one pixel of a scaled picture. The scaled picture gives a superior quality as far as fine edge and variable smoothness. For showing scenes in a fluid gem show board, the equipment of winscale is executed utilizing FPGA. In this way, winscale has low multifaceted nature with great scale property and requires just a limited quantity of memory. The edge characteristics of an image are preserved well and deliver the data directly. The proposed implementation uses 29000 gates at 65MHz operating frequency. It provides good image quality with low hardware cost.

1.2.3 Linear Interpolation

It is a straightforward sort of addition. Here, the framework to add or measure the pixel assessment of any discretionary point among at least two given focuses. Accurately, linear interpolation is for adding elements of one variable (either ‘x’ or ‘y’) on an efficient 1D network.

\[
P = P_1 + \frac{d(P_2 - P_1)}{D}
\]

OR

\[
P = P_1 + \frac{(x-x_1)(P_2 - P_1)}{(x_2-x_1)}
\]

\[
\text{Figure 1: Linear interpolation}
\]
The above equation used to interpolate the value of arbitrary points of the given points. The distance between the point \( P_1 \) and \( P \) is given by ‘\( d \)’. The distance between \( P_1 \) and \( P_2 \) is given by ‘\( D \)’. Coordinates \( x_1, x, \) and \( x_2 \) are the horizontal coordinates of the linear interpolation.

1.2.4 Bilinear interpolation
This strategy is utilized to interpolate the elements of two factors \((x, y)\) on a methodical 2D matrix that establishes an amplification of linear interpolation technique. It is performed by the mix of two linear interpolations. The significant thought is to accomplish addition of linearity one way first, and afterward the other way next.

\[
P_{12} = P_1 + \frac{d(P_2 - P_1)}{D} \quad \text{OR} \quad P_{12} = P_1 + \frac{(x-x_1)(P_2-P_1)}{(x_2-x_1)}
\]

\[
P_{34} = P_3 + \frac{d(P_4 - P_3)}{D} \quad \text{OR} \quad P_{34} = P_3 + \frac{(x-x_1)(P_4-P_3)}{(x_2-x_1)}
\]

\[
P = P_{12} + \frac{h(P_{12} - P_{34})}{h} \quad \text{OR} \quad P = P_{12} + \frac{(y-y_1)(P_{12}-P_{34})}{(y_2-y_1)}
\]

Using the above equations, the interpolation is executed on both the directions \((x, y)\). The space between the point \((x_1, x)\) and \((x, x_2)\) is given by ‘\( d \)’. The space between \((x_1, x_2)\) is given by ‘\( D \)’. Coordinates \( x_1, x, \) and \( x_2 \) are the horizontal coordinates of the linear interpolation. The distance between the point \((y_2, y)\) and \((y, y_1)\) is given by ‘\( h \)’. The distance between \((y_1, y_2)\) is given by ‘\( H \)’, where \( y_1, y, \) and \( y_2 \) are the vertical coordinates of the linear interpolation. Thus it is used as an effective algorithm in filtering of scaled image.

1.2.5 Adaptive scalar bilinear interpolation
The execution of 2D picture scalar, another scaling calculation is proposed by [8] that involve bilinear interjection, a brace channel, and a spatial channel (honing). To offer a low difficulty and high commonness, bilinear insertion calculation is used. To lessen the effects referenced beforehand, pre-filters, for instance, cinches and honing spatial channels are incorporated. By using \( 5 \times 5 \) basic convolution channel as opposed to \( 3 \times 3 \) cross section coefficients pass on a diminished memory and estimation challenges. The VLSI building is overhauled by participation and gear dissemination.

1.2.6 Nearest Neighbor Interpolation
This introduction strategy gives a basic and quick method for scaling of a picture. During enlarging (up-scaling), the vacant spaces will be supplanted with the closest neighboring pixel, while diminishing (down-scaling), it includes reduction in pixels.

1.2.7 Filter based Interpolation

The Filtering based interpolation strategies utilizes diverse channel to scale a picture. Along these lines it is in any case called as re-sampling technique.

![Fig.3 Filtering based Interpolation / Re-sampling](image)

As shown in Fig.3, the re-sampling from one discrete signal \( x(n) \) to a re-sampled signal \( y(n') \) of a different resolution is computed as:

\[
y(n') = \sum_{t=-w}^{w} h(t) x(n'-t) \quad \ldots \quad (3)
\]

Where, \( h(t) \) is the interpolating function and \( w \) is the desired filtering window.

Various image compression and interpolation methods are discussed that provide an efficient algorithm with high boost filtering. But these algorithms lag in operational speed, excessive power consumption and occupational area. The overview of the existing methods with their advantages and limitations are illustrated in table I as shown below.

| Technique                        | Author                  | Year | Description                                                                                                                                                                                                 | Advantages                                                                                                                                     | Disadvantages                                                                                                       |
|----------------------------------|-------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|
| VLSI architecture in FIR filter  | Modular high-level      | 2016 | The use of pipelined Analog to Digital Converters and medium estimated FPGA gadgets used to accomplish secluded significant level programming continuously gamma beam applications. | 1. Efficient, high density, low power solution for applications that require a large number of channels.                                                                                     | 1. The determination of time-stamp and simulation energy is required.                                                   |
| design                           | programming             |      |                                                                                                                                                                                                             |                                                                                                                                                |                                                                                                                        |
| Statistics Centric design        |                         | 2016 | An intensive measurable investigation of Canonic Signed Digit (CSD) coefficients proposed a novel reconfigurable FIR channel design. It for the most part center around improvement of the channel execution | 1. Advantageous in terms of area, power, and speed for those high order FIR filters.                                                                                                                  | 1. Dynamic reconfigurable mechanism are not explored                                                                   |
Poly-phase filtering based calibration [11] 2016

The alignment procedure for the Time Interleaved Analog to Digital Converters (ADCs) with contribution at any Nyquist Band (NB) is the proposed work. It straightforwardly adjusts the yield signs of sub-ADC and in this manner works at the low rate.

1. The correction technique is simple.
2. Does not require the adaptive digital synthesis filters.

1. Reduction in the power consumption is must.

Geiger-mode Avalanche Photodiodes (GAPDs) [12] 2012

Free-running Analog to Digital Converter (ADC) and Field Programmable Gate Array (FPGA) based sign handling strategy was produced for a cerebrum Positron Emission Tomography (PET) framework utilizing GAPDs.

1. For PET systems, reduced complexity, cost, and development.

Beta gamma coincidence [13] 2013

A phoswich finder with Compton concealment capacity for radio-xenon estimations through beta-gamma happenstance method was created and portrayed.

1. Measurements show that the Compton suppression mechanism reduces Compton continuum in the region of spectrum.

1. Reassembling is needed for phoswich detector.
2. Implementation is needed for the current off-line digital pulse processing.

Multiplier based FIR design

Distributed Arithmetic based reconfiguration [14] 2014

Efficient scheme for high throughput reconfigurable DA-based implementation of FIR digital filters.

1. Cost is reduced by sharing the same registers by the DA units for different bit slices.

1. Produces most number output per cycle.

1. The multiplication time is still dominant factor for determination of instruction cycle time of a DSP chip.

Rounded Truncated Multiple Constant Multiplication [15] 2013

Presented a low cost FIR filter design that considers the optimization of coefficient bit width and hardware resources in implementations.

1. Used in applications of accurate results
2. Low area cost and power consumption.

1. Enhanced speed, area utilization, and power with respect to other multipliers.
2. Vedic multipliers are used only in certain multipliers of applications.

Vedic multiplier [16] 2015

Provides the utilization of various structures of Vedic Multiplier in various tasks like stockpiling, transmission or handling of enormous measure of information as sign or a picture required day by day in an advanced world.

1. Reduces the normal exchanging exercises of the multiplier block.
2. Reduction of switching activities in various FIR channels.

1. Only single constant multiplications are performed.

Vertical Horizontal Binary Common Sub-expression Elimination (VHBCSE) [17] 2015

Presents one new VHBCSE figuring, which clears the fundamental essential sub-enunciations by applying 2-piece BCSE vertically. Further the CSs was performed through finding the CSs present inside the coefficients by applying BCSEs of different lengths on a level plane to different layers of the move and incorporate based consistent multiplier plan.

1. Reduced power dissipation

1. 8*8 and 16*16 multipliers are not designed.

Bypassing multiplier [18] 2014

A low power FIR filter using modified bypassing multiplier was designed. The total
dissipation is calculated and compared with the existing technique.

### Multiplier-less FIR design

| Technique | Year | Description |
|-----------|------|-------------|
| Dynamic power dissipation | 2015 | Different adders and multipliers are analyzed on the basis of their delay and dynamic power dissipation. |
| Harmony Search algorithm (HAS) and Frequency Transformation | 2012 | A new optimization approach using HAS is proposed to solve optimization problems in engineering disciplines, where search space consists of integers. |
| Genetic algorithm | 2013 | A novel genetic algorithm (GA) is proposed for the design of low hardware cost multiplier-less FIR filters both in single stage and cascade forms. |
| Realization of constant multiplications | 2014 | Shown the complexity of a multiplier-less FIR filter design that depends on the filter form, high level synthesis algorithms, design platforms and parameters. |
| Gravitational Search Algorithm (GSA) | 2013 | A design of a multiplier-less sharp Variable Bandwidth Filters (VBF) based Frequency Response Masking (FRM) that are capable of both bandwidth reduction and enhancement. |
| Floating point architecture | | Increase efficiency and performance of inner kernels. Effective for bigger problem sizes that fit on the Linear Algebra Core (LAC) |
| Double Precision Floating Point Comparator | 2016 | The design of a double precision floating point comparator was proposed and used in high precision operations. |

2. Reduced the switching activity and achieves high speed.

1. Used for only low power and low delay digital FIR filter

1. Deployed only when the response is very close to that of the ideal filter.

1. Less computational time
2. Reduced the hardware cost of the resulting designs, for both single stage and cascade designs

1. Significant impact on complexity, performance and power dissipation
1. Only few constraints were considered

1. Better performance in terms of complexity and filter
2. Reduction in power consumption and area

1. Modelled only for optimization problem.

1. Architecture is similar to those of previous work.
1. No comparisons of complexity and flexibility

1. Minimal impact on power and area
2. No degradation of fixed point operations

1. Architecture is similar to those of previous work.

1. No incorporation of comparator to an Floating Point Unit (FPU)

1. Architecture is similar to those of previous work.
2. CONCLUSION
In this paper, VLSI architecture methodologies along with various types of their algorithms were surveyed. Initial work on this topic concentrated on the improvement of the performance of algorithms under different architectures like FPGA, CMOS, etc. On account of problems present in VLSI, the architectural review is categorized into various forms in preceding tabulations. Tabulations enhance the ideas about the method, its pros and cons of the various types of approaches in VLSI. The limitations observed from the survey analysis are low speed, high
occupational area and power consumption. Thus, the survey of traditional studies conveyed that optimization of architecture is considered as the suitable solution for aforementioned problems.

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