Crosstalk Noise Analysis in Coupled On-Chip Interconnects Using MRTD Technique

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Research Article

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DOI: https://doi.org/10.21203/rs.3.rs-430460/v1

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Received: date / Accepted: date

Abstract In this paper, the Crosstalk noise analysis of coupled on-chip interconnects have been analyzed. The multiresolution time-domain method (MRTD) is used to analyze the crosstalk noise model. The crosstalk induced propagation time delay and crosstalk peak voltage on the victim line of interconnects have been determined and compared to those of the conventional finite difference time domain (FDTD) method and validated with HSPICE simulations at the 22nm technology node. The results of the proposed method shows that crosstalk induced propagation delay in dynamic in-phase, out-phase and peak voltage timing, as well as the peak voltage value for functional crosstalk in the copper interconnects are an average error of less than 0.53% for the proposed model and HSPICE simulations. The results of the proposed model are closely similar to those of HSPICE simulations. Electromagnetic interference and electromagnetic compatibility of on-chip interconnects can also be addressed using the proposed method.

Keywords Crosstalk · On-chip Interconnects · Delay · FDTD · MRTD

1 Introduction

Advancement in Very Large Scale Integration technology offers gigascale integrated circuits in system on-chip. The use of interconnects is particularly important in the integration of electronic devices. Because of these requirements, the chip’s complexity and number of sources of variations have increased, and the tightly packed interconnects emit transient crosstalk at high operating frequencies [1,2]. For a long time, accurate peak noise timing and peak crosstalk noise estimation in a driver-interconnect-load system has been a key architecture view [3]. On the basis of lumped and distributed RC interconnects, various crosstalk and delay models are proposed in [4,5]. Masoumi et al. [6] computed crosstalk noise effects in a capacitively coupled RC interconnect line using closed form expressions. Ismail et al. [7] strengthened the model by integrating self-inductance effects and estimated the RLC line propagation delay. Because of the introduction of low resistive interconnect materials and fast operating switching frequencies, parasitic inductance has began to play an important role in on-chip interconnect efficiency. To accurately estimate the output, the on-chip interconnects must be viewed as scattered RLC lines or transmission lines [8].

In order to evaluate crosstalk noise, previous models interpreted the non-linear CMOS driver to be a Simply linear resistor [9,10] which appears to deviate from the effects. MOSFET operates approximately 50 percent of its operating in the saturation region during the transient period, and later in linear (or) cutoff regions. Several methods with different analytical solutions, Finite Difference Time Domain (FDTD) approach and SPICE results have been documented in recent works for the DIL system in [11]. In the current state, several researchers have researched the crosstalk results based on the algorithm of the traditional finite-difference time-domain (FDTD) as it is precise [12] and Vobulapuram et al. [13] applied the FDTD approach to a nonlinear driver of CMOS by using the model of alpha-power law.
and the model of nth-power law, respectively, and studied the effects of crosstalk in Cu interconnects.

The FDTD approach is an important computational procedure used to solve problems of electromagnetic and partial differential equations. The FDTD approach is numerically dispersive [14] and is used for propagation along the discretization. Thus, there is an extreme need for a model with an edge in numerical dispersive properties [15]. Krumpholz and Katehi [16] have suggested a multi-resolution time domain (MRTD) approach with an additional advantage of the numerical dispersion characteristics. Grivet-Talocia [17] suggested the MRTD model in view of the Haar Scaling function as a basic function and gives the same precision as a basic function and gives the same precision

The MRTD model for mutually two-coupled on-chip interconnects is built in this section using basis function of Daubechies’ scaling function with four vanishing moments \( D_4 \).

The Telegrapher’s equations can be used to describe the coupled interconnects mathematically. The coupled on-chip interconnects are defined as [22, 23] using these equations.

\[
\frac{\partial V(z, t)}{\partial t} + L \frac{\partial I(z, t)}{\partial t} = -I(z, t)R \quad (1)
\]

\[
\frac{\partial I(z, t)}{\partial t} + C \frac{\partial V(z, t)}{\partial t} = 0 \quad (2)
\]

where \( x \) and \( t \) are the positions and time, respectively. \( R \), \( L \), and \( C \) are two-dimensional interconnect impedances that are measured using [23]. The current and voltage variables for a two-coupled interconnect line are \( I = [I_1, I_2]^T \) and \( V = [V_1, V_2]^T \).

\[
R = \text{diag}[R_1, R_2]
\]

\[
L = \begin{bmatrix} L_1 & L_m \\ L_m & L_2 \end{bmatrix}
\]

\[
C = \begin{bmatrix} C_1 + C_c & -C_c \\ -C_c & C_2 + C_c \end{bmatrix}
\]
where subscript 1 corresponded to a line 1 and subscript 2 corresponded to a line 2. The voltage and current evaluations point on interconnect line 1 are shown in Figure 3.

Alternatively, current and voltage points are considered in time and space to evaluate telegrapher equations. The currents and voltages are separated by $\Delta t$ in time and $\Delta x$ in space for better accuracy, as shown in Figure 2, where $\Delta t$ is time and $\Delta x$ is space represent in discretization intervals.

The interconnects line l of length is resistive driver at $x = 0$ and terminated at $x = l$ is capacitive load. The line is divided consistently to $N_x$ segments of a length $\Delta x = \frac{l}{N_x}$, indicating the discretization voltages(V) and currents(I) nodes, which are coefficients of unknown as seen in Figure 3, where source current represents $I_0$.

The voltages and currents terms can be extended using a known function $(h_n(t) \text{ and } \Phi_k(x))$ the coefficients of unknown in order to solve equations (1) and (2) by following the method defined in [16] as:

$$I(x, t) = \sum_{n, k = -\infty}^{+\infty} I_{k+\frac{1}{2}}^{n+\frac{1}{2}}(x) h_n(t) = 0 \quad (4b)$$

Where $I_{k+\frac{1}{2}}^{n+\frac{1}{2}}$ is the coefficient of expansion current and $V_k^n$ is the coefficients of the voltage expansion in terms of functions scaling, and the indices n and k are discrete time and space indices related to time and space organizes via $t = n\Delta t$, and $x = k\Delta x$. Functions $h_n(t)$, and $\Phi_k(x)$ defined as:

$$h_n(t) = h\left(\frac{t}{\Delta t} - n\right) = 0 \quad (5a)$$

Where, pulse function $h(t)$ is defined as

$$h(t) = \begin{cases} 
1 & \text{for } |t| < \frac{1}{2} \\
\frac{1}{2} & \text{for } |t| = \frac{1}{2} \\
0 & \text{for } |t| > \frac{1}{2}
\end{cases} \quad (5b)$$

$$\Phi_k(x) = \Phi\left(\frac{x}{\Delta x} - k\right) \quad (5c)$$

Where, $\Phi(x)$ signifies the scaling function of a Daubechies, and h(t) represents the Haar scaling function.

The following integrals [24] are considered in order to derive the MRTD technique for a equations (1) and (2):

$$\int_{-\infty}^{+\infty} h_n(t)h_{n'}(t)dt = (\delta_{n,n'})\Delta t \quad (6a)$$

$$\int_{-\infty}^{+\infty} h_n(t)\frac{\partial h_{n'+\frac{1}{2}}(t)}{\partial t} dt = (\delta_{n,n'} - \delta_{n,n'+1}) \quad (6b)$$

$$\int_{-\infty}^{+\infty} \Phi_k(x)\Phi_{k'}(x)dt = (\delta_{k,k'})\Delta x \quad (6c)$$

$$\int_{-\infty}^{+\infty} \Phi_k(x)\frac{\partial \Phi_{k'+\frac{1}{2}}(t)}{\partial x} dt = \sum_{i=-L_s}^{L_s-1} b(i)\delta_{k+i,k'} \quad (6d)$$

Where the Kronecker symbol is represented by $'\delta_{k,k'}'$ and $'\delta_{n,n'}'$. The effective support sizes of the basis functions is indicated by the Ls. By considering the scaling function of Daubechies as the basis functions with four vanishings moment (D4). The coefficients $b(i)$ are called connections coefficients. Table1 shows $b(i)$ for $1 \leq i \leq L_s$, whereas $b(i)$ for $i < 1$ it can be accomplished by symmetry condition $b(-1-i) = -b(i)$, and zero for $i > L_s$

$$b(i) = \frac{1}{2\pi} \int_{0}^{\infty} \left|\hat{\Phi}(\lambda)\right|^2 \lambda \sin\lambda(i + \frac{1}{2})d\lambda \quad (7)$$
Table 1: Connections coefficients b(i) for Daubechies scalings function (D4) [19]

| b(i) | b(i) for D4 |
|------|-------------|
| 1    | 1.3110343773 |
| 2    | -0.1560100110 |
| 3    | 0.0419957460  |
| 4    | -0.0080547236 |
| 5    | 0.0000303695  |
| 6    | 0.0000108999  |
| 7    | 0.0000000041  |

Where the scaling function of Fourier transform f(x) is $\hat{\phi}(\lambda)$.

The follow iterative calculations for currents and voltages were carried out to employing the Galerkin technique [16] in equation (1) and (2) and by using the test functions $\phi_i h_{n+\frac{1}{2}}(t)$ and $\phi_i h_n(t)$:

$$I_{k+\frac{1}{2}}^{n+\frac{1}{2}} = PI_{k+\frac{1}{2}}^{n+\frac{1}{2}} - \frac{\Delta t}{\Delta z} L^{-1} Q \left( \sum_{i=1}^{L_s} b(i) (V_{k+i}^n - V_{k-i+1}^n) \right)$$

(8a)

$$V_{k+1}^{n+1} = V_k^n - \frac{\Delta t}{\Delta x} C^{-1} \sum_{i=1}^{L_s} b(i) \left( I_{k+i}^{n+\frac{1}{2}} - I_{k-i+1}^{n+\frac{1}{2}} \right)$$

(8b)

where,

$$P = (1 + \frac{\Delta t}{\Delta z} RL^{-1})^{-1} \left( 1 - \frac{\Delta t}{\Delta z} RL^{-1} \right)$$

$$Q = (1 + \frac{\Delta t}{\Delta z} RL^{-1})^{-1}$$

In the iterative equations (8a) and (8b), the near-end voltage $V_{k+1}^{n+1}$ and the far-end voltage $V_{N_x+1}^{n+1}$ are obtained and the iterative equation of the currents and voltages near the boundary necessity to be modified. Near the boundary the currents are expressed by $I_{j+\frac{1}{2}}^{n+\frac{1}{2}}$ and $I_{N_x+1-i+1}^{n+\frac{1}{2}}$ for $i = 1, 2, 3, \ldots, L_s - 1$ and voltages are $V_i^{n+1}$ and $V_{N_x+1-i+1}$ for $i = 2, 3, \ldots, L_s$. Many of these currents and voltages have a number of terms that surpass the index ranges in iterative equations (8a) and (8b).

Equations (8a) and (8b) need to be decomposed using the relationship in [25] to update the iterative equations of currents and voltages, which satisfies the connection coefficients $b(i)$ provided by the connection coefficients $b(i)$ given by

$$\sum_{i=1}^{L_s} (2i - 1) b(i) = 1$$

(9)

By Substituting (9) into (8b), to get

$$\sum_{i=1}^{L_s} b(i) (2i - 1) V_{k+1}^{n+1} = \sum_{i=1}^{L_s} b(i) (2j - 1) V_k^n - \frac{\Delta t}{\Delta x} \left( (2i - 1) b(i) \left( I_{k+i}^{n+\frac{1}{2}} - I_{k-i+1}^{n+\frac{1}{2}} \right) \right)$$

(10)

To decompose (8b) considering a corresponding term with i as:

$$b(i) (2i - 1) V_{k+1}^{n+1} = b(i) (2i - 1) V_k^n - \frac{\Delta t}{\Delta x} C^{-1} \left( (2i - 1) b(i) \left( I_{k+i}^{n+\frac{1}{2}} - I_{k-i+1}^{n+\frac{1}{2}} \right) \right)$$

(11)

for at $i = 1, 2, 3, \ldots, L_s - 1$.

Equation (11) is further adapted by employing the at boundary conditions as proved in Sections 2.3 and 2.4.

2.2 Modeling of CMOS Driver

Two-coupled on-chip interconnect line equivalent electrical circuit model is shown in figure 2. The input voltage (Vs) is a two-dimensional vector with the formula $V_s = [V_{s1}, V_{s2}]^T$. The interconnects line is driven by a CMOS driver [26] that follows a modified Alpha power law model. The velocity saturation effects, as well as the finite drain conductance parameters, are included.

$$I_n = \left\{ \begin{array}{ll} K_{sn} (V_s - V_{tn})^\alpha n (1 + \sigma_n V_1) \\
K_{ln} (V_s - V_{tn})^\alpha n V_1 \\
0 \end{array} \right. \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad (12)$$

$$I_p = \left\{ \begin{array}{ll} K_{sp} (V_{DD} - V_s - |V_{tp}|)^\alpha p (1 + \sigma_p (V_{DD} - V_1)) \\
K_{ip} (V_{DD} - V_{tp} - V_s)^\alpha p (-V_1 + V_{DD}) \\
0 \end{array} \right. \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad (13)$$

The latest equations for PMOS and NMOS are signified by $m \times 1$ vectors, i.e. $I_p = [I_{p1}, I_{p2}]^T$ and $I_n = [I_{n1}, I_{n2}]^T$. The linear region transconductance parameters, threshold voltages, saturation region transconductance parameters, drain conductance parameters and velocity saturation index of NMOS(PMOS) are $K_{ln}$ ($K_{ip}$), $V_{tn}$ ($V_{tp}$), and $K_{sn}$ ($K_{sp}$) respectively. The NMOS/PMOS model parameter values for the 22nm technology node as seen in Table 2 are used for this analysis.
Applying discretization and Galerkin technique to (14) decomposed equation (16) as

\[ I_0 = C_m \frac{d(V_s - V_i)}{dx} - C_d \frac{dV_i}{dx} + I_p - I_n \]  

(14)

Applying discretization and Galerkin technique to (14) then

\[ \Delta x I_0 = \Delta x C_m \frac{1}{\Delta x} [(V_{n+1} - V_n) - (V_{n+1} - V_1)] \]

\[ - \Delta x C_d (V_{n+1} - V_n) + \Delta x I_{n+1} - \Delta x I_{n+1} \]

(15a)

then

\[ V_{n+1} = V_n + \left( \frac{C_m + C_d}{\Delta t} \right)^{-1} \times \]

\[ \left[ C_m \frac{1}{\Delta t} (V_{n+1} - V_n) + (I_{n+1} - I_{n+1} - I_{n+1}) \right] \]  

(15b)

the near end terminal a voltage is carry out at k=1 from (8b)

\[ V_{1}^{n+1} = V_1^n - \frac{\Delta t}{\Delta x} C_{n-1} \sum_{i=1}^{L_s} b(i) \left( I_{i+\frac{1}{2}} - I_{i-\frac{1}{2}} \right) \]  

(16)

By following the steps from the equations (9) (11) to decomposed equation (16) as

\[ b(1)V_{1}^{n+1} = b(1)V_1^n - b(1) \frac{\Delta t}{\Delta x} C^{-1} \left( I_{\frac{1}{2}} - I_{\frac{1}{2}} \right) \]

(17a)

\[ 3b(2)V_{1}^{n+1} = 3b(2)V_1^n - 3b(2) \frac{\Delta t}{3\Delta x} C^{-1} \left( I_{\frac{1}{2}} - I_{\frac{1}{2}} \right) \]

(17b)

\[ \vdots \]

\[ b(L_s)(2L_s - 1)V_{1}^{n+1} = b(L_s)(2L_s - 1)V_1^n \]

- \(2L_s - 1\)b(Ls) \(\frac{\Delta t}{(2L_s - 1)\Delta x} C^{-1} \left( I_{\frac{1}{2}} - I_{\frac{1}{2}} \right) \]

(17c)

Iterative equations (17a)(17c) to be considered as CAD, i.e., central difference equations. in the particular calculations, the subscript to the terms \(I_{n+\frac{1}{2}}, I_{n+\frac{1}{2}}, \ldots\)

\(I_{n+\frac{1}{2}}, I_{n+\frac{1}{2}}, \ldots\) have surpassed the index range. To solve this, substitute the central difference scheme by using the forward difference scheme. By leaving the weight coefficient in each equations unchanged, iterative equations can also be obtained.

\[ b(1)V_{1}^{n+1} = b(1)V_1^n - b(1) \frac{\Delta t}{\Delta x} C^{-1} \left( I_{\frac{1}{2}} - I_{\frac{1}{2}} \right) \]

(18a)

\[ 3b(2)V_{1}^{n+1} = 3b(2)V_1^n - 3b(2) \frac{\Delta t}{3\Delta x} C^{-1} \left( I_{\frac{1}{2}} - I_{\frac{1}{2}} \right) \]

(18b)

\[ \vdots \]

\[ b(L_s)(2L_s - 1)V_{1}^{n+1} = b(L_s)(2L_s - 1)V_1^n \]

- \(2L_s - 1\)b(Ls) \(\frac{\Delta t}{(2L_s - 1)\Delta x} C^{-1} \left( I_{\frac{1}{2}} - I_{\frac{1}{2}} \right) \]

(18c)

From the above equations (18a) - (18c), the iterative equation at the near-end boundary node voltage of \(V_{1}^{n+1}\) is obtained through the following:

\[ V_{1}^{n+1} = V_1^n - \frac{\Delta t}{\Delta x} C^{-1} \sum_{i=1}^{L_s} b(i) \left( I_{i+\frac{1}{2}} - I_{i+\frac{1}{2}} \right) \]

(19)

In equation (19), substituting by \(I_{n+\frac{1}{2}} = I_{n+\frac{1}{2}} + I_{n+\frac{1}{2}}\) and equation (15a) we obtained the equation as

\[ V_{1}^{n+1} = V_1^n - AB \sum_{i=1}^{L_s} b(i) I_{i+\frac{1}{2}} \]

\[ - AB \sum_{i=1}^{L_s} b(i) \left( I_{i+1} + I_{i+1} + I_{i+1} + C_m \left( \frac{V_{n+1} - V_n}{\Delta x} \right) \right) \]

(20)

Where,

\[ A = \left( 1 + (C_m + C_d) \frac{\Delta t}{\Delta x} \sum_{i=1}^{L_s} b(i) \right)^{-1}, B = \frac{\Delta t}{\Delta x} C^{-1} \]

2.4 Modeling at far-end boundary condition

Similarly, the nodal analysis equation at load current \(I_{N + 1}\) is given by the far-end terminal (k = Nx+1) is:

\[ I_{N + 1} = C_d \frac{dV_{N + 1}}{dt} \]

(21)
then the final iterative equations given at the far end of the terminal is

\[ V_{N_x+1}^{n+1} = V_{N_x+1}^n - EF \]

\[ \left( \sum_{i=1}^{L_s} b(i) I_{N_x+1-i}^{n+\frac{1}{2}} - \sum_{i=1}^{L_s} 2b(i) I_{N_x+1-i}^{n+\frac{1}{2}} \right) \]  
\[ \quad \text{Where } E = \left( 1 + \frac{2C}{\Delta t} \right) C^{-1} \sum_{i=1}^{L_s} a(i) \]

F = \frac{\Delta t}{\Delta x} C^{-1} 

Where Some of the term indices surpass the index ranges for all the nodes between the terminals in the algorithm extension to obtain and update the iterative equations, so a truncation method is applied by taking \( V_{N_x+1}^{n+1} \) as an examples for \( k = 2, 3, \ldots, L_s \) and by subsequent the steps of equations (10) and (11), it can be decomposed (8b) as an example for \( k = 2, 3, \ldots, L_s \)

\[ b(1)V_k^{n+1} = b(1)V_k^n - b(1) \frac{\Delta t}{\Delta x} C^{-1} \left( I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-\frac{1}{2}}^{n+\frac{1}{2}} \right) \]  
\[ \text{(23a)} \]

\[ 3b(2)V_k^{n+1} = 3b(2)V_k^n - 3b(2) \frac{\Delta t}{3\Delta x} C^{-1} \left( I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-\frac{1}{2}}^{n+\frac{1}{2}} \right) \]  
\[ \text{(23b)} \]

\[ \vdots \]

\[ b(k-1)(2k-3)V_k^{n+1} = b(k-1)(2k-3)V_k^n - b(k-1)(2k-3) \frac{\Delta t}{(2k-3)\Delta x} C^{-1} \left( I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-\frac{1}{2}}^{n+\frac{1}{2}} \right) \]  
\[ \text{(23c)} \]

\[ \vdots \]

\[ b(k)(2k-1)V_k^{n+1} = b(k)(2k-1)V_k^n - b(k)(2k-1) \frac{\Delta t}{(2k-1)\Delta x} C^{-1} \left( I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-\frac{1}{2}}^{n+\frac{1}{2}} \right) \]  
\[ \text{(23d)} \]

\[ b(k+1)(2k+1)V_k^{n+1} = b(k+1)(2k+1)V_k^n - (2k+1)b(k+1) \frac{\Delta t}{(2k+1)\Delta x} C^{-1} \left( I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-\frac{1}{2}}^{n+\frac{1}{2}} \right) \]  
\[ \text{(23e)} \]

\[ \vdots \]

\[ b(L_s)(2L_s-1)V_k^{n+1} = b(L_s)(2L_s-1)V_k^n - b(L_s) \times \frac{\Delta t}{(2L_s-1)\Delta x} C^{-1} \left( I_{L_s+\frac{1}{2}}^{n+\frac{1}{2}} - I_{L_s-\frac{1}{2}}^{n+\frac{1}{2}} \right) \]  
\[ \text{(23f)} \]

From the equations (23a)-(23f) stated above, it is also observed that the indices of the equation do not surpass the index ranges for the first k terms. In addition, all calculations for which the index terms surpass the index spectrum appear in the remaining \( L_s-k \) term. As \( L_s-k \) terms are out-of-bound these equations are not available for iterative equations in MRTD model.

To prevent problem, a truncations is built in calculations where the index range is surpassed.

first k terms by summing up the in equations (23a)-(23f), iterative equations can be updated for at \( k = 2, 3, \ldots, L_s \) 

\[ V_k^{n+1} = V_k^n - Q \left( \sum_{i=1}^{k} (2i-1)b(i) \right)^{-1} \]

\[ \left( \sum_{i=1}^{k} b(i) \left( I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}} \right) \right) \]  
\[ \text{(24)} \]

Using the same steps illustrated in equations (23a) - (23f), a altered iterative equation of voltages at interiors point as presented in equation (25) and voltages near a load as presented in equation (26) is.

for at the \( k = L_s+1, L_s+2, N_x - L_s, N_x - L_s + 1 \) 

\[ V_k^{n+1} = V_k^n - Q \left( \sum_{i=1}^{L_s} b(i) \left( I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}} \right) \right) \]  
\[ \text{(25)} \]

for at the \( k = N_x - L_s + 2, N_x - L_s + 3, \ldots, N. \) 

\[ V_k^{n+1} = V_k^n - Q \left( \sum_{i=1}^{N_x-k+1} b(i)(2i-1) \right)^{-1} \times \]

\[ \left( \sum_{i=1}^{N_x-k+1} b(i) \left( I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}} \right) \right) \]  
\[ \text{(26)} \]

Iterative current equations can also be modified by subsequent the same voltages iterative equations with minor modifications. As seen in Figure3, it is observed that at the half-integer points the current nodes appear. It implies that at the interior points of the terminals, all the currents are located. Therefore, the current near the terminals need alteration. For iterative current equations near to the terminals, it is necessary to decompose (8a) using the steps of iterative voltage of the equations. The final updated iterative current equations are given as

for at the \( k = 1, \) near at the source

\[ I_{1+\frac{1}{2}}^{n+\frac{1}{2}} = P I_{1+\frac{1}{2}}^{n+\frac{1}{2}} - \frac{\Delta t}{\Delta x} L^{-1} Q \left( \sum_{i=1}^{L_s} b(i) \left( V_{i+1}^{n+1} - V_i^{n+1} \right) \right) \]  
\[ \text{(27)} \]
for \( k=2, 3, \ldots, L_s \)

\[
I_{k+\frac{1}{2}}^{n+\frac{2}{3}} = P I_{k+\frac{1}{2}}^{n+\frac{1}{3}} - Q \left( \sum_{i=1}^{\frac{L_s}{2}} b(i)(2i - 1) \right)^{-1} \times \frac{\Delta t}{\Delta x} L_s^{-1} \left( \sum_{i=1}^{L_s} b(i) \left( V_{k+i}^{n+1} - V_{k-i+1}^{n+1} \right) \right)
\]

(28)

for at the \( k = L_s+1, L_s+2, \ldots, Nx-L_s, Nx-L_s+1 \).

at the Interior point iteratives equations

\[
I_{k+\frac{1}{2}}^{n+\frac{2}{3}} = P I_{k+\frac{1}{2}}^{n+\frac{1}{3}} - Q L_s^{-1} \times \frac{\Delta t}{\Delta x} \left( \sum_{i=1}^{L_s} b(i) \left( V_{k+i}^{n+1} - V_{k-i+1}^{n+1} \right) \right)
\]

(29)

for at the \( k = Nx-L_s+2, Nx-L_s+3, \ldots, Nx \).

Near the load, iteratives equations are

\[
I_{k+\frac{1}{2}}^{n+\frac{2}{3}} = P I_{k+\frac{1}{2}}^{n+\frac{1}{3}} - Q \frac{\Delta t}{\Delta x} L_s^{-1} \times \left( \sum_{i=1}^{Nx-k-\frac{1}{2}} b(i)(2i - 1) \right)^{-1} \times \left( \sum_{i=1}^{Nx-k-\frac{1}{2}} b(i) \left( V_{k+i}^{n+1} - V_{k-i+1}^{n+1} \right) \right)
\]

(30)

In the context of this bootstrapping method, modified voltage and current iterative equations are tested. Firstly, in terms of historical Voltages and current values, voltages iterative equations are solved at a rigid time using equations (20), (22), (24)-(26). Then, equations (27)-(30) solve the iterative equations of currents in terms of voltages measured initially and past values of current. The courant stability condition [19,25] is thus known as the stable output for MRTD iteratives equations.

\[
\Delta t \leq q \frac{\Delta x}{\vartheta}
\]

(31)

Which states that for each cell, the time of propagation must be higher than the time step. Where \( q \) is the current numbers given by \( q = 1/ \sum_{i=1}^{L_s} |b(i)| \) and \( \vartheta \) and \( \vartheta \) is the phase velocity of the line propagation. However, the boundary conditions will always guarantee the stability requirement as these are explicitly derived out of an implicit expression.

3 The MRTD Model is compared and validation

The Performance analyses of two-lines coupled on-chip interconnects structure is presented. The proposed model is validated by comparison it to conventional FDTD model and with HSPICE simulation. The interconnects load is driven by CMOS driver, the interconnects dimensions are taken from ITRS [27,28]. At 22nm technology node, the interconnect is placed from a ground plane is 99nm. thickness of the line is 66nm. The width and space between lines are to be equal and the value is 33nm. The inter level dielectric medium permittivity is 2.3. The length and load capacitance of the interconnects are 1mm and 2fF. The voltage Vdd is 0.8V. The signal voltage swings from 0 to 0.8V (LowHigh) or 0.8 to 0V (HighLow). The input source voltages have a transition time is 20ps. The proposed MRTD model implemented by MATLAB using Intel(R) Xeon(R) CPU E3-1225v6 operating at 3.30GHz and HSPICE tool [29].

The parasitic values of RLC for a two-coupled interconnect line structure are

\[
R = \begin{bmatrix} 10.10 & 0 \\ 0 & 10.10 \end{bmatrix}, L = \begin{bmatrix} 2.082 & 1.86 \\ 1.86 & 2.082 \end{bmatrix} \times \frac{\mu H}{m}, C = \begin{bmatrix} 90.75 & -75.16 \\ -75.16 & 90.75 \end{bmatrix} \times \frac{p F}{m}
\]

3.1 Analysis of transients and crosstalk in two coupled on-chip interconnects

This section covers the transient and crosstalk studies of a two-line coupled on-chip interconnects system. Line 1 is the aggressor in the coupled two on-chip interconnects system seen in Figure 1, and line 2 is the victim line. On the other end of the victim spectrum, the effect for functional, dynamic in-phase, and dynamic out-phase switching has been found using the proposed model, HSPICE, and the conventional FDTD model. On the victim line, the transient reaction is investigated. The effect of functional crosstalk is explored by modifying line 1’s aggressor input from 0.8V to 0V while holding line 2’s victim in quiescent mode. When both aggressor and victim stimuli turn at the same time, the impact of in-phase or out-phase is also explored. At the far end of the victim spectrum, the transient graph results based on the above conditions are compared. Figure (4a) displays the functional, dynamic in-phase, and dynamic out-phase transient responses (4c). Figures 4(b) and 4(c) demonstrate that the victim-line peak solution has higher dispersion errors than the conventional FDTD method. The proposed model, on the other hand, is superior to the conventional FDTD model in terms of precision due to its significant superiority in numerical dispersion properties. Figure 4(c) illustrates how miller coupled capability allows signal transitions to take longer during out-phase than during in-phase switching. The results of proposed MRTD
model match HSPICE correctly in all input switching situations and outperform the conventional FDTD method.

Fig. 4: Transient response comparison at far-end voltage of victim line (a) for functional (b) for in-phase (c) for out-phase

In comparison to HSPICE, Table 3 indicates the computational error associated with estimating functional crosstalk effects over victim line2 for conventional FDTD and then suggested MRTD models. Efficacy at multiple input transition times. The proposed model’s average error in predicting crosstalk peak voltage timing is found to be 0.42 percent, compared to 0.92 percent for the conventional FDTD method. Table 4 also indicates that the proposed model correctly

Fig. 5: Peak voltage timing with varied input transition time for victim line.

Fig. 6: Peak voltage with varied input transition time for victim line.
Table 3: Victim lines computational error for peak voltage timings in functional crosstalk.

| Input Transition time (ps) | HSPICE | Proposed model | Conv.* FDTD | %error proposed model | %error Conv.* FDTD |
|---------------------------|--------|----------------|-------------|-----------------------|--------------------|
| 10                        | 254.55 | 253            | 251        | 0.60                  | 1.39               |
| 20                        | 274.08 | 274            | 273        | 0.03                  | 0.39               |
| 30                        | 292.72 | 292            | 291        | 0.07                  | 0.79               |
| 40                        | 287.39 | 287            | 286        | 0.13                  | 0.48               |
| 50                        | 297.56 | 297            | 295        | 0.18                  | 0.85               |
| 60                        | 311.49 | 310            | 308        | 0.47                  | 1.12               |
| 70                        | 318.37 | 315            | 314        | 1.05                  | 1.37               |
| 80                        | 328.14 | 326            | 324        | 0.65                  | 1.26               |
| 90                        | 339.88 | 338            | 337        | 0.55                  | 0.84               |
| 100                       | 343.72 | 342            | 341        | 0.50                  | 0.79               |

Table 4: Victim lines computational error for peak voltage values in functional crosstalk.

| Input Transition time (ps) | HSPICE | Proposed model | Conv.* FDTD | %error proposed model | %error Conv.* FDTD |
|---------------------------|--------|----------------|-------------|-----------------------|--------------------|
| 10                        | 0.31998 | 0.3190 | 0.3230 | 0.30                  | 0.94               |
| 20                        | 0.31901 | 0.3189 | 0.3228 | 0.03                  | -1.18              |
| 30                        | 0.3190  | 0.3187 | 0.3226 | 0.09                  | -1.12              |
| 40                        | 0.3188  | 0.3184 | 0.3222 | 0.12                  | -1.06              |
| 50                        | 0.31792 | 0.3166 | 0.3208 | 1.98                  | -0.90              |
| 60                        | 0.31746 | 0.3174 | 0.3203 | 0.02                  | -0.89              |
| 70                        | 0.31652 | 0.3176 | 0.3201 | -0.34                 | -1.13              |
| 80                        | 0.31635 | 0.3171 | 0.3196 | -0.23                 | -1.02              |
| 90                        | 0.31588 | 0.3156 | 0.3185 | 0.08                  | -0.82              |
| 100                       | 0.31493 | 0.3127 | 0.3195 | 0.70                  | -1.45              |

Table 5: Computational error for dynamic in-phase switching propagation delay for various transition times.

| Input Transition time (ps) | HSPICE | Proposed model | Conv.* FDTD | In-phase Propagation delay (ps) | %error proposed model | %error Conv.* FDTD |
|---------------------------|--------|----------------|-------------|--------------------------------|-----------------------|--------------------|
| 10                        | 91.906 | 91             | 90          | 0.98                           | 2.07                  |
| 20                        | 97.72  | 97             | 96          | 0.73                           | 1.76                  |
| 30                        | 103.18 | 103            | 102         | 0.17                           | 1.14                  |
| 40                        | 108.7  | 107            | 106         | 1.56                           | 2.48                  |
| 50                        | 114.12 | 114            | 113         | 0.10                           | 0.98                  |
| 60                        | 119.51 | 119            | 118         | 0.42                           | 1.26                  |
| 70                        | 124.7  | 124            | 123         | 0.56                           | 1.36                  |
| 80                        | 130.13 | 130            | 129         | 0.09                           | 0.86                  |
| 90                        | 136.79 | 136            | 135         | 0.57                           | 1.30                  |
| 100                       | 141.21 | 141            | 140         | 0.14                           | 0.85                  |

Table 6: Computational error for dynamic out-phase switching propagation delay for various transition times.

| Input Transition time (ps) | HSPICE | Proposed model | Conv.* FDTD | Out-phase Propagation delay (ps) | %error proposed model | %error Conv.* FDTD |
|---------------------------|--------|----------------|-------------|--------------------------------|-----------------------|--------------------|
| 10                        | 697.86 | 696            | 695         | 0.26                           | 0.40                  |
| 20                        | 702.5  | 700            | 699         | 0.35                           | 0.49                  |
| 30                        | 707.72 | 706            | 704         | 0.24                           | 0.52                  |
| 40                        | 713.21 | 712            | 710         | 0.16                           | 0.45                  |
| 50                        | 719.28 | 718            | 717         | 0.17                           | 0.31                  |
| 60                        | 725.46 | 725            | 724         | 0.06                           | 0.20                  |
| 70                        | 729.19 | 728            | 726         | 0.16                           | 0.43                  |
| 80                        | 737.5  | 736            | 735         | 0.20                           | 0.33                  |
| 90                        | 740.37 | 740            | 738         | 0.04                           | 0.32                  |
| 100                       | 746.29 | 745            | 743         | 0.172                          | 0.44                  |

Crosstalk Noise Analysis in Coupled On-chip Interconnects using MRTD Technique

predicts peak voltage, with an average error of 0.27 percent compared to 1.05 percent using the conventional FDTD method.
The computational error associated with estimating dynamic in-phase crosstalk effects over victim line2 for conventional FDTD and proposed MRTD models is shown in table 5. Sturdiness of input transitions at different times the proposed model is observed to have a 0.53 percent average error in propagation delay estimation, compared to 1.4 percent for the conventional FDTD method.

In table 6 indicates the computational error associated with estimating dynamic out-phase crosstalk effects over victim line2 for conventional FDTD and proposed MRTD models. Sturdiness of input transitions at different times the proposed model has a 0.18 percent average error in propagation delay estimation, compared to 0.38 percent for the conventional FDTD method.

The simulation results of proposed MRTD model match HSPICE correctly in all input switching situations and outperform the conventional FDTD method.

The graphs for peak voltage timing and peak voltage value on the victim line as a result in functional crosstalk generated by a varied in input transition time are seen in Figures 5 and 6. At different input transition times, Figures 7 and 8 illustrate dynamic in-phase and out-phase crosstalk propagation delays. The results for both functional and dynamic crosstalk are MRTD model validated with HSPICE and outperform the conventional FDTD model. Figures 9 and 10 demonstrate the peak voltage timing and peak voltage on victim line.
Fig. 11: Computational time with different crosstalk switching.

4 Conclusion

The modified alpha power law model is used in this paper to build an analytically dependent MRTD model for functional and dynamic crosstalk study of coupled two transmission lines driven by a CMOS driver. For two line coupled on-chip interconnects, in this work provided a detailed study of functional, dynamic in-phase, and out-phase induced effects on the victim line. The Courant condition is strictly followed by the suggested model's stability. The influence of input transition time on crosstalk propagation delay under dynamic and peak voltage timing, as well as the peak voltage value for functional crosstalk, is studied. With regard to HSPICE, the proposed MRTD model and the FDTD validate that the proposed MRTD model is in good agreement with HSPICE. The findings show that the average error of crosstalk-induced propagation delays in both dynamic in-phase and out-phase on-chip interconnects is 0.53 percent and 0.18 percent, respectively, according to the proposed model. Functional crosstalk has a peak voltage timing of 0.42 percent and a peak voltage value of 0.27 percent. Furthermore, the suggested MRTD model and FDTD model are validated with HSPICE for peak voltage timing and peak voltage value on victim line for functional cases for various values of load capacitances with an average error is less than 1%. The proposed model time efficiency over the FDTD model and HSPICE is reported, suggesting that it has the ability to analyses crosstalk in on-chip interconnects quickly and accurately. The analysis was performed on two coupled interconnects, but it can also be generalised to M- mutually coupled on-chip interconnects.

Acknowledgements

The research has been sponsored by the University Grants Commission (UGC) fellowship. Authors would like to thank the Principal, UCE(A) Osmania University for all their support.

Compliance with ethical standards

Conflict of interest

The authors declare that they have no conflict of interest.

Data Availability Statement

Data sharing not applicable to this article as no datasets were generated or analyzed during the current study.

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CMOS drivers driven two-coupled on-chip interconnect lines, which are terminated by capacitive loads.
Figure 2

Space and time discretizations on on-chip interconnect line.

Figure 3

Spatial discretization for I and V on on-chip interconnect line.
Figure 4

Transient response comparison at far-end voltage of victim line (a) for functional (b) for in-phase (c) for out-phase

Figure 5

Peak voltage timing with varied input transition time for victim line.
Figure 6

Peak voltage with varied input transition time for victim line.
Figure 7

The victim line of dynamic in-phase 50% propagation delay varied input transition time.
Figure 8

The victim line of a dynamic out-phase 50% propagation delay varied input transition time.
Figure 9

Peak voltage timing with varied Load capacitance for victim line.
Figure 10

Peak voltage with varied Load capacitance for victim line.
Figure 11

Computational time with different crosstalk switching.