Modeling of thermoelectric processes in a power MOSFET transistor with a structural defect

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Abstract. The results of thermal modeling of the temperature distribution in the structures of a high-power MOSFET transistor with macrodefects of an electrophysical nature are presented. It is shown that the presence of a defect in the structure of the transistor leads to an increase in the maximum temperature of the channel overheating and an increase in the inhomogeneity of the temperature distribution over the area of the active region of the crystal. The influence of the location of the defect on the value of the maximum overheating of the structure and the gate-source voltage is considered. The developed thermal model can serve as the basis for creating methods for diagnosing MOSFET transistors by thermoelectric characteristics and identifying defective products.

1. Introduction

Power MOSFET microwave transistors (PFETs) with different topologies of the base transistor cell are increasingly replacing power bipolar transistors in the RF and microwave equipment [1, 2]. When designing the PFET in order to increase their operating frequencies, the packing density of the base cells in the PFET crystal is increased, but the possibility of such an increase is limited by the minimum achievable topological cell sizes and the temperature of the PFET channel overheating as a result of the crystal being heated by dissipated power. Even with a uniform distribution of the current density in the PFET structure, the channel overheating temperature can reach 120–150 °C [3]. Various macrodefects of the structure, obviously, will lead to an increase in the maximum channel temperature and acceleration of degradation processes in the device [4]. But, studies of the influence of macrodefects on the temperature distribution in the structure of the PFET and their thermal characteristics were not carried out.

The power dissipation PFET, which in the transistor turns into heat, is determined by the following expression:

\[ P = U_{DS} I_D, \]  

where \( U_{DS} \) – drain-source voltage, \( I_D \) – drain current. At a given operating mode (\( U_{DS} \) constantly) the drain current will depend on the temperature. Physical reasons for the dependence of the drain current on temperature \( I_D(T) \) is that as the temperature \( T \) increases, the carrier mobility in the transistor channel and the cutoff voltage decrease \( U_{th} \). The temperature coefficient of the source
current, depending on the operating mode of the PFET, can be either positive or negative. In practice, most field effect transistors operate at a negative temperature coefficient of the source current, that is, negative thermal feedback (NTF) is in effect [5].

In the production of microwave PFET, macrodefects arise in the structure and construction of the transistor as a result of a violation of technological processes, leading to an inhomogeneous distribution of current density and power in the structure of the device and, as a result, to local overheating, thermoelectric instability of current distribution and failures. A defect in the electrophysical kind is a deviation from the nominal values of the electrical parameters of the instrument structure in some local part of its active region. The presence of a defect leads to a redistribution of power dissipated by the structure between the defective and defect-free regions of the structure even in the isothermal mode (before self-heating).

Known thermal models of high-power MOSFETs [6-9] did not take into account thermal feedback in the transistor and do not allow adequately quantify the effect of macrodefects on temperature fields in the transistor structure.

The aim of this work is computer simulation and experimental study of changes in the thermal characteristics of high-power MOSFET transistors when various types of macrodefects are introduced into their structure.

2. Thermoelectric model
To determine the temperature field in the PFET structure, a 3D thermoelectric model was constructed, the scheme of which is shown in Figure 1.

![Figure 1](image)

Figure 1. Geometry PFET structure: 1 – current-carrying metallization; 2 – crystal of semiconductor; 3 – ceramic gasket; 4 – heat sink.

The simplified design of the PFET is a three-layer structure, the first layer of which is a rectangular \((l_{x1} \times l_{y2} \times (h_1 - h_2))\) semiconductor crystal, with current-carrying metallization located on its upper surface, the second layer is a cylindrical ceramic gasket with a radius \(r = l_{x3}/2\) and tall \((h_2 - h_3)\) and the third layer is a heat sink, high \(h_3\).
The temperature distribution in the structure of the transistor is found from the solution of the heat equation
\[
\nabla_{x,y,z} \left( \lambda_i(T_i) \nabla_{x,y,z} T_i(x,y,z) \right) = 0, \quad (i = 2, 3, 4) \tag{2}
\]
where \( T_i = (T_i - T_0) \); \( T_i, T_0 \) – the temperature of the layers of the structure and the environment; \( \lambda_i \) – thermal conductivity coefficients of structure layers.

The boundary conditions are given by the following:
- the lateral surfaces of a rectangular crystal of semiconductor, ceramic gasket and the free upper surface of the ceramic gasket are thermally insulated;
- the heat sink temperature is maintained equal to \( T_0 \);
- power density is set on the upper surface of the faculty
\[
-\lambda_2(T_2) \frac{\partial T_2}{\partial z} \bigg|_{z=h} = \begin{cases} q(x,y), & (x,y) \in S_{ar}, \\ 0, & (x,y) \in S - S_{ar}, \end{cases} \tag{3}
\]
where \( S, S_{ar} \) – the area of the upper surface of the crystal and the active region.

In saturation mode, the dependence of the drain current on temperature can be represented as [5]
\[
I_D = \frac{K_s(T)}{2} \left( U_{GS}(T) - U_{th}(T) \right)^2, \tag{4}
\]
where \( K_s(T) = \mu_n(T) C \frac{W}{L} \) – specific slope of the I-V characteristic; \( W, L \) – width and length of the gate; \( C \) – linear capacity of the gate material; \( \mu_n \) – mobility of charge carriers in the channel. Carrier mobility in the channel decreases with temperature [10]
\[
\mu_n(T) = \mu_n(0) \left( \frac{T_0}{T} \right)^m. \tag{5}
\]

The function of the power density in the active region, taking into account expressions (1), (4) and (5), can be written as follows:
\[
q(x,y) = \frac{U_{DS} I_D}{S_{ar}} = \frac{U_{DS} K_s(T_0)}{2 S_{ar}} U^2 \left( \frac{T_0}{T} \right)^m, \tag{6}
\]
where \( K_s(T_0) = \mu_n(0) C \frac{W}{L}, U(T) = (U_{GS}(T) - U_{th}(T)), U_{GS} \) – gate-source voltage.

For assignment condition for the inclusion of a transistor in an electrical circuit we assume that the drain current of the transistor is constant. This means that with constant \( U_{DS} \) and at any temperature distribution \( T(x,y,h) \) the active region of the semiconductor structure (PPP) must satisfy the condition:
\[
\int_{S_{ar}} \frac{U^2(T)}{T^m} dS = \frac{2 I_D S_{ar}}{K_s(T_0) T_0^m}. \tag{7}
\]

The solution of the thermoelectric model problem (2) – (7) was found by the numerical finite element method using a specially developed program that includes the interactive software COMSOL Multiphysics. Verification of compliance with condition (7) was carried out by the iterative method presented [4]. The controlling variable parameter of the iteration cycle was the voltage \( U(T) \).

For numerical modeling and comparison of calculated characteristics with experimental ones in this work as the object of study was selected silicon powerful field microwave transistor KP907B. A silicon crystal \( (m = 1.5) \) with geometric dimensions \( 1.8 \times 1.3 \times 0.3 \) mm was mounted on a cylindrical plate with a radius \( r = 3.6 \) mm and a height of 1.5 mm made of BeO, which was mounted on an aluminum heat sink. The temperature dependences of the thermal conductivity of the
materials of the structure were selected from the database of the COMSOL program. Temperature the environment \( T_0 = 300 \, \text{K} \). The value of the drain current was set within \( I_D = 0.1 \div 0.5 \, \text{A} \). Drain-source voltage \( U_{DS} = 20 \, \text{V} \).

The appearance of the upper surface of the PFET crystal, into which the defect was introduced, and its model representation are presented in Figure 2. The defect structure was simulated by disconnecting groups of current-carrying metallization paths of 1, 2, 3 base transistor cells.

![Figure 2. The upper surface of the PFET crystal (a) and its model representation (b).](image)

The dependence of the superheat temperature of the semiconductor structure on the flowing drain current was investigated. The introduction of a defect in the structure of the transistor leads to an increase in the maximum superheat temperature and the heterogeneity of the temperature distribution over the active region of the crystal. The highest values of these values are observed when the 1st group of paths is disconnected (Figure 3).

We introduce the coefficient of non-uniformity of the temperature distribution over the active region of the semiconductor structure

\[
\delta = \frac{T_{\text{max}} - T_{\text{av}}}{T_{\text{av}}},
\]

where \( T_{\text{max}} \) and \( T_{\text{av}} \) - maximum and average temperatures of the active region of the faculty.

![Figure 3. The overheating temperature of the crystal surface (y = 0.65 mm) at \( I_D = 0.5 \, \text{A} \), \( U_{DS} = 20 \, \text{V} \): 1 – without defect and with disconnecting group of paths: 2 – 1st, 3 – 2nd, 4 – 3rd.](image)

![Figure 4. The coefficient of non-uniformity of the temperature distribution over the semiconductor structure: 1 – without defect, 2 – the 1st group of paths is disconnecting.](image)
As can be seen from Figure 4, the difference between the coefficients of non-uniformity for the defective (absence of the first group of paths) and defect-free structures increases significantly with an increase in the drain current strength, for the considered option by 24%.

Experimental testing of the results of computational studies was carried out. The maximum temperature of the crystal of field-effect transistors KP907B was measured with a change in the drain current within $I_D = 0.1 \pm 0.7 \, \text{A}$. The constant current source was maintained by changing the voltage at the gate. The transistor was connected to an aluminum heat sink in the form of a flat plate with dimensions of $100 \times 100 \times 10 \, \text{mm}$. The heat sink was installed on the thermostat. The temperature of the thermostat was maintained at $27 \, ^\circ \text{C}$. Drain-source voltage $U_{DS}$ was set equal to $6 \, \text{V}$. The circuit for switching on the tested transistor is shown in Figure 5.

![Figure 5. The circuit of the tested transistor KP907B.](image)

The model was tested by comparing the dependences on the current strength of the source of the relative voltage $U_d / U_0$ where $U_d$ and $U_0$ – voltage $U$ (formula (6)) for defective and defect-free structures, respectively, obtained by calculation (Figure 6) and experimental dependence $U_{GSd} / U_{GS0}$ where $U_{GSd}$ and $U_{GS0}$ – gate-source voltage for defective and defect-free structures (Figure 7).

![Figure 6. Voltage $U = (U_{GS} - U_{th})$ on drain current at $U_{DS} = 6 \, \text{V}$ with disconnecting different group of paths: 1 – the 3rd, 2 – the 2nd, 3 – the 1st.](image)

![Figure 7. Gate-source voltage from the drain current at $U_{DS} = 6 \, \text{V}$ with disconnecting different group of paths: 1 – the 3rd, 2 – the 2nd, 3 – the 1st.](image)

The comparison showed that the calculated and experimental dependences are in good qualitative agreement. The experimental dependences differ from the simulation results by the value of the cutoff
voltage $U_{th}$. As can be seen from the graphs, the steepness of the curves $U(I_D)$ and $U_{DS}(I_D)$ for defective structures more than for defect-free structures.

3. Conclusion
A thermoelectric model of a high-power microwave field-effect transistor was developed and computational studies were carried out for a PFET with an electrophysical defect, which made it possible to obtain a temperature distribution over the structure of the transistor. It is shown that the values of the coefficient of non-uniformity of the temperature distribution over the active region of the semiconductor defect structure of a high-power field-effect transistor are larger than for a defect-free structure. The effect of the location of the defect on the values of the maximum overheating of the structure and the gate-source voltage is estimated. The highest values of these values are observed when the first group of paths is disconnected, which was confirmed by experiment. The steepness of the dependence of the gate-source voltage on the drain current strength for defective structures is greater than for defect-free structures. The results can be used to develop a method for MOSFET diagnostics based on the steepness of the gate-source voltage dependence on the drain current.

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