SOT-MRAM based Sigmoidal Neuron for Neuromorphic Architectures

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Abstract—In this paper, the intrinsic physical characteristics of spin orbit torque (SOT) magnetoresistive random-access memory (MRAM) devices are leveraged to realize sigmoidal neurons in neuromorphic architectures. Performance comparisons with the previously power- and area-efficient sigmoidal neuron circuits exhibit 74× and 12× reduction in power-area-product values for the proposed SOT-MRAM based neuron. To verify the functionality of the proposed neuron within larger scale designs, we have implemented a circuit realization of a 784×16×10 SOT-MRAM based multi-layer perceptron (MLP) for MNIST pattern recognition application using SPICE circuit simulation tool. The results obtained exhibit that the proposed SOT-MRAM based MLP can achieve accuracies comparable to an ideal binarized MLP architecture implemented on GPU, while realizing orders of magnitude increase in processing speed.

I. INTRODUCTION

The neuromorphic computing is the concept of embodying the physical processes that underlie the computations of biological neural networks (NNs) within the physics of the very large-scale integration (VLSI) circuits, as opposed to the conventional power-hungry approaches which emulate the mathematical behavior NNs on conventional computing systems such as GPUs. Recently, various beyond CMOS technologies have been investigated to be leveraged within neuromorphic circuits and architectures, among which memristive devices are one of the most promising solutions [1].

Memristors have been widely used within both synapse and neuron circuits, and provide significant advantages such as small on-chip area, non-volatility, and low-power dissipation [1]. However, they suffer from severe reliability issues such as high device-to-device (D2D) and cycle-to-cycle (C2C) variations [2] and low endurance [3]. On the other hand, spintronic devices have shown some reliability advantages over other memristive devices. For instance, spin orbit torque (SOT) magnetoresistive random-access memory (MRAM) [4] have exhibited infinite write endurance, which is a desirable feature for in-circuit training that can be used to alleviate variation challenges [2] in neuromemristive architectures [1]. While SOT-MRAM devices have been previously used within in-memory computing platforms as a hardware accelerator for artificial neural networks [5], herein we will go beyond the previous work and utilize the intrinsic characteristics of SOT-MRAM cells within the neuromorphic architecture as a natural building block for both synapses and neurons.

II. SOT-MRAM BASED NEURONS AND SYNAPSES

Fig. 1 shows a simplified structure of a SOT-MRAM cell, which includes a magnetic tunnel junction (MTJ) with two ferromagnetic (FM) layers, which are separated by a thin oxide layer. MTJ has two different resistance levels, which are determined according to the angle (θ) between the magnetization orientation of the FM layers. The resistance of the MTJ in parallel (P) and antiparallel (AP) magnetization configurations can be obtained using the following equations [6]:

\[
R(\theta) = \frac{2R_{MTJ}(1 + TMR)}{2 + TMR(1 + \cos \theta)}
\]

where \( R_{MTJ} = \frac{RA_{MTJ}}{1 + (\frac{V_0}{V_0})^2} \) in which the resistance-area product (RA) value of the MTJ depends on the material composition of its layers. TMR is the tunneling magnetoresistance, which relies on temperature (T) and bias voltage (Vb). \( V_0 \) is a fitting parameter, and \( TMR_0 \) is a material-dependent constant.

In the MTJ structure, the magnetization direction of electrons in one of the FM layers is fixed (pinned layer), while the electrons’ directions in the other FM layer (free layer) can be switched. In [4], Liu et al. have shown that passing a charge current (Ic) through a heavy metal (HM) generates a spin-polarized current (Is) using the spin Hall Effect (SHE), which can switch the magnetization direction of the free layer, as shown in Fig. 1. The ratio of the generated spin current to the applied charge current is normally greater than one leading to an energy-efficient switching operation [7]. Herein, we will use SOT-MRAM devices as a building block for both synapse and neuron circuits.

![SOT-MRAM cell](image1)

Fig. 1. (a) SOT-MRAM cell. Positive current along +z induces a spin injection current +z direction. The injected spin current produces the required spin torque for aligning the magnetic direction of the free layer in +y directions, and vice versa. (b) SOT-MRAM Top view.


Table 1

| Parameter   | Description            | Value          |
|-------------|------------------------|----------------|
| $MTJ_{Area}$| $l_{MTJ} \times w_{MTJ} \times \frac{d}{4}$ | $50nm \times 30nm \times \frac{d}{4}$          |
| $HM_{V}$   | $l_{HM} \times w_{HM} \times t_{HM}$          | $100nm \times 50nm \times 3nm$               |
| RA         | resistance-area product | $10 \ \Omega \cdot \mu m^2$           |
| $V_0$      | Fitting parameter      | 0.65           |
| TMR$R_0$   | tunneling magnetoresistance | 100          |

Fig. 2. (a) The SOT-MRAM based neuron, (b) The VTC curves showing various operating regions of PMOS (MP) and NMOS (MN) transistors.

A. SOT-MRAM Based Neuron

Fig. 2 (a) shows the structure of the proposed neuron, which includes two SOT-MRAM devices and a CMOS-based inverter (2T-2R). The magnetization configuration in SOT-MRAM1 is required to be in $P$ state, while SOT-MRAM2 is in $AP$ state. The SOT-MRAMs in the neuron’s circuit operate as a voltage divider, which reduces the slope of the linear operating region in the CMOS inverter’s voltage transfer characteristic (VTC) curve. The reduction in the slope of linear region in the CMOS inverter creates a smooth high-to-low output voltage transition, which enables the realization of the activation function behavior desirable for sigmoid neurons.

In order to verify the functionality of our proposed neuron, first we created a Verilog-A model of the SOT-MRAM device using equations (1) and (2), and the parameters listed in Table 1. Next, we utilized the developed model along with 14nm HP-FinFET PTM library to realize the circuit implementation of the neuron. Fig. 2 (b) shows the SPICE circuit simulation results of the proposed SOT-MRAM based neuron using $V_{DD} = 0.8V$ and $V_{SS} = 0V$ voltages, which validates the desired sigmoidal behavior for neurons.

B. SOT-MRAM Based Synapse

SOT-MRAM cell are capable of realizing two resistive level, i.e. $R_P$ and $R_{AP}$. The combination of two SOT-MRAM cells and a differential amplifier can produce the positive and negative weights required for implementation of a binary synapse. Fig. 3 shows a neuron with $Y_i = \sum_i(W_{in} - I_{in})$ as the input of the neuron, where $X_i$ is the input signal and $W_i$ is a binarized weight. The corresponding circuit implementation is also shown in the figure, which includes two SOT-MRAM cells and a differential amplifier as synapse. The output of the differential amplifier ($Y_i$) is proportional to $(I^+ - I^-)$, where $I^+ = X_iG_i^+$ and $I^- = X_iG_i^-$. Thus, $Y_i \propto X_i(G_i^+ - G_i^-)$ in which $G_i^+$ and $G_i^-$ are the conductance of SOT-MRAM1 and SOT-MRAM2, respectively, that can be tuned as shown in Fig. 3 to realize negative and positive weights in a binary synapse. For instance, for $W_i = -1$, SOT-MRAM1 and SOT-MRAM2 should be in $AP$ state and $P$ states, respectively. According to Eq. (1) $R_{AP} > R_P$, which means $G_{AP} < G_P$ since $G = 1/R$, therefore $G_i^+ < G_i^-$ and $Y_i < 0$.

III. PROPOSED SOT-MRAM BASED MLP ARCHITECTURE

Figures 4 and 5 exhibit the training and inference paths of a 784 x 10 SOT-MRAM based single layer perceptron proposed here, which are shown separately for simplicity. The synaptic connections are designed in form of a crossbar architecture, in which the number of columns and rows are defined based on the number of nodes in input and output layers, respectively. During the training phase, the resistance of the SOT-MRAM based synapses will be tuned using the bit-line (BL) and source-line (SL) interconnections which are shared between different rows, as shown in Fig. 4. The write word line (WWL) control signals will only activate one row in each clock cycle, thus the entire array can be updated using $j$ clock cycles, where $j$ is equal to the number of neurons in the output layer. Moreover, to tune the states of the SOT-MRAMs in neurons according to the requirements mentioned in Section II.A, the BL and SL control signals for the neuron are set to VDD and VSS, respectively, as shown in Fig. 4.

In the inference phase, the BL and SL control signals are in high-impedance (Hi-Z) state, and read word line (RWL) and WWL control signals are connected to VDD and GND, respectively. This will stop the write operation in synapses, and generate $I^+$ and $I^-$ currents shown in Fig. 5, amplitude of which depend on the input (IN) signals and the resistances of SOT-MRAM synapses. Each row includes a shared differential amplifier, which generates an output voltage proportional to $\sum_i(I_{n}^+ - I_{n}^-)$ for the $n$th row, where $i$ is the total number of nodes in the input layer. Finally, the output of the differential amplifiers are connected to the SOT-MRAM based sigmoidal neurons. The entire inference operation occurs in parallel and in a single clock cycle. The required signaling to control the training and inference operations is listed in Table II.
Simulation Results section.

still operate in a single clock cycle as it will be shown in the perceptron (MLP) and deep neural network (DNN), which can is that it can be readily concatenated to form a multi-layer

One of the main advantages of the proposed architecture

is the output of the $i$th neuron.

Table III provides the notations and descriptions for both teacher and student networks, in which $x$ is the input and $o_i$ is the output of the $i$th neuron.

V. SIMULATION RESULTS

To incorporate the features of the SOT-MRAM based synapses and neurons within our training mechanism, we have made two modifications to the approaches previously used for training binarized neural networks [8], [9]. First, we have used binarized biases in the student networks instead of real-valued biases. Second, since our SOT-MRAM neuron realizes real-valued sigmoidal activation function ($\text{sigmoid}(x)$) without any computation overheads, we could avoid binarizing the activation functions and reduce the possible information loss in the teacher or student networks [8]. Herein, after each weight update in the teacher network we clip the real-valued weights within the $[-1, 1]$ interval, and then use the below deterministic binarization approach to binarize the weights:

$$W_{ij} = \begin{cases} +1, & w_{ij} \geq \Delta_B \\ -1, & w_{ij} < \Delta_B \end{cases}$$

(3)

where $\Delta_B = 0$ is threshold parameters for binarized weights. Finally, once all the binarized weights are trained we will use a mapping mechanism to convert them to resistive states in SOT-MRAM based synapses as explained in Section II.B. Stochastic binarization [9] scheme can also be used to quantize the weights and biases. However, stochastic approach exhibits its advantages in very large scale convolutional neural networks (CNNs) which are not the focus of this paper. In fact, we have initially leveraged stochastic mechanisms in our simulations and while the training times were approximately 10-fold longer, the obtained accuracy values were comparable to those realized by deterministic approaches.

V. SIMULATION RESULTS

To evaluate the performance of our proposed SOT-MRAM based neuromorphic MLP architecture, we have utilized a hierarchical simulation approach including circuit-level and application-level simulations as described in the following.

A. Circuit-Level Simulation of SOT-MRAM based Neuron

Herein, we have used SPICE circuit simulator with 14nm HP-FinFET PTM transistor library, Verilog-A model of the SOT-MRAM using, and $V_{DD} = 0.8$ as the nominal voltage to obtain the power consumption of our proposed SOT-MRAM based sigmoid neuron. The obtained simulation results show the average power consumption of $64\mu W$ for the proposed sigmoid neuron. Moreover, the area of our neuron is approximately equal to $13\lambda \times 30\lambda$, that is obtained by the layout design, in which $\lambda$ is a technology-dependent parameter. Herein, we have used the 14nm FinFET technology, which leads to the approximate area consumption of $0.02\mu m^2$ per
neuron. SOT-MRAM devices can be fabricated on top of the transistors, thus incurring no area overhead.

Table IV provides a comparison between our SOT-MRAM based sigmoidal neuron and some of the most power- and area-efficient mixed-signal sigmoid neuron designs. To provide a fair comparison in terms of area and power dissipation, we have utilized General Scaling method [10] to normalize the power dissipation and area of the designs listed in Table IV voltage and area scale at different rate of U and S, respectively. Thus, the power dissipation is scaled with respect to 1/U^2 and area per device is scaled according to 1/S^2 [10]. The obtained results exhibit that the proposed SOT-MRAM based neuron can achieve significant area reduction, while realizing comparable power consumption compared to the existing power- and area-efficient neuron implementations. This results in a 74× and 12× reduction in power-area product compared to the designs introduced in [11] and [12], respectively.

B. Application-level Simulation

To verify the functionality of our SOT-MRAM based neuron and synapse for larger-scale applications, we have developed a Python-based simulation framework based on [13]. The developed simulator realizes the SPICE circuit implementation of our SOT-MRAM based MLP, and measures its corresponding accuracy and power consumption for a specific pattern recognition application. Fig. 6 depicts the accuracy of a 784 × 16 × 10 SOT-MRAM based neuromorphic MLP simulated in SPICE compared to floating-point and binarized MLP architectures implemented by GPU for MNIST handwritten digit recognition application. The results obtained show that within 10 training epochs a comparable test accuracy of 86.54% and 85.56% can be achieved for binarized MLP and SOT-MRAM based MLP architectures, respectively. However, the SOT-MRAM based MLP complete the recognition task in a single clock cycle, while a highly-parallel implementation of binarized MLP on GPU requires ~10^5 clock cycles with similar frequency to complete the same task.

VI. CONCLUSION

Herein, we proposed a power- and area-efficient SOT-MRAM based sigmoidal neuron, which have been leveraged along-with SOT-MRAM based synapses to construct a neuromorphic MLP architecture. The developed neuron played an enabling role in the single-cycle operation of the SOT-MRAM based MLP. We implemented the SPICE circuit realization of a 784 × 16 × 10 SOT-MRAM based MLP and compared its performance with a binarized MLP implemented on GPU for MNIST pattern recognition application. The results obtained exhibited approximately five orders of magnitude increase in the processing speed of our SOT-MRAM based MLP, while realizing comparable accuracy to that of the GPU-implemented binarized MLP. Herein, we have used a small network as a proof-of-concept, while the achieved improvements are expected to be even more significant for larger scale circuits which will be studied in the future work of authors.

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TABLE IV

|                     | [11] | [12] | Proposed Herein |
|---------------------|------|------|-----------------|
| Power Consumption   | 7.4× | 0.98×| 1×              |
| Area Consumption    | 10×  | 12.3×| 1×              |
| Power-Area Product  | 74×  | 12×  | 1×              |

Fig. 6. Accuracy for MNIST application using a 784 × 16 × 10 MLP.