Atomic Layer Deposition of Metal Oxides and Chalcogenides for High Performance Transistors

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Atomic layer deposition (ALD) is a deposition technique well-suited to produce high-quality thin film materials at the nanoscale for applications in transistors. This review comprehensively describes the latest developments in ALD of metal oxides (MOs) and chalcogenides with tunable bandgaps, compositions, and nanostructures for the fabrication of high-performance field-effect transistors. By ALD various n-type and p-type MOs, including binary and multinary semiconductors, can be deposited and applied as channel materials, transparent electrodes, or electrode interlayers for improving charge-transport and switching properties of transistors. On the other hand, MO insulators by ALD are applied as dielectrics or protecting/encapsulating layers for enhancing device performance and stability. Metal chalcogenide semiconductors and their heterostructures made by ALD have shown great promise as novel building blocks to fabricate single channel or heterojunction materials in transistors. By correlating the device performance to the structural and chemical properties of the ALD materials, clear structure–property relations can be proposed, which can help to design better-performing transistors. Finally, a brief concluding remark on these ALD materials and devices is presented, with insights into upcoming opportunities and challenges for future electronics and integrated applications.

1. Introduction

Since the first working transistor was demonstrated in the 1940s, transistors have become a fundamental component of modern electronics. Networks of semiconductor transistors form logic gates essential for the function of microprocessors. Apart from this prominent application, transistors are also widely used in electronic/optoelectronic devices and integrated systems such as flat panel displays, electronic skins, artificial synapses, photodetectors, physical or chemical sensors, and biomedical equipment.[1–11] Thus, the application of transistors is ubiquitous within modern digital products.

The basic design of a transistor is composed of three terminals that consist of source (S), drain (D), and gate (G) electrodes. A semiconductor material, also referred to as a channel, contacts the S and D electrodes. A dielectric serves as an insulation layer between the G electrode and the semiconductor layer to electrically isolate the channel. Variation in channel and electrode placement design affords both bottom-gate and top-gate structures, which are two commonly used types of transistors (Figure 1a,b). The channel length (L) of a transistor is defined as the distance between the S and D regions, and the channel width (W) is the total distance across the channel area parallel to the S and D electrodes. Current manufacturing techniques extensively utilize a silicon substrate for transistors in device fabrication of electronic/optoelectronic systems such as processors, communication chips, and image sensors.[12] However, flexible substrates such as polyethylene terephthalate (PET), polyimide (PI), polydimethylsiloxane (PDMS), and biodegradable polymers, show good potential for use within the next-generation flexible devices as a part of wearable/stretchable electronics, and future technologies.[9,13–15] Most transistors operate using a model based on electro-magnetic field manipulation. Hence, they are termed field-effect transistors (FETs).[16,17] Application of a voltage between the source and gate of a FET device forms an electric field. This field stimulates the accumulation of charge carriers at the semiconductor/dielectric interface, a process termed capacitive carrier injection. As a result, current flow between S and D electrodes may be modulated according to a gate voltage ($V_G$, or recorded as $V_{GS}$). When $V_G$ exceeds a threshold voltage ($V_T$), a conducting channel is established and...
a source-drain current ($I_{DS}$) can be adjusted by controlling a bias across the S and D electrodes ($V_{DS}$). Therefore, transistors can facilitate the adjustment of on-/off-state currents by tuning the applied bias voltages, achieving a higher output power than input power. These attributes afford excellent signal conduction, amplification, and switching functions for various applications such as oscillators, photodetectors, and tactile sensors.

The performance of transistors is generally evaluated through charge-transfer and output characteristics measured for calculating important metrics such as the carrier mobility ($\mu$), $V_T$, on/off current ratio ($I_{ON}/I_{OFF}$), and subthreshold swing (SS). Output curves are obtained by plotting $I_{DS}$ as a function of $V_{DS}$ whilst a sweeping $V_C$ is applied (Figure 1c), while transfer curves are illustrated by plotting $I_{DS}$ as a function of $V_C$ at a constant $V_{DS}$ (Figure 1d). As the $V_{DS}$ applied increases, $I_{DS}$ will continue to increase until the channel current saturates. If $V_{DS}$ is much lower than the applied $V_C$ ($V_{DS} << V_C - V_T$), the transistor operates in a linear regime. At this bias condition, $I_{DS}$ increases linearly with $V_{DS}$ and charge accumulation across the channel is considered to be evenly distributed. Thus, the current–voltage relationship can be determined by Equation (1).\(^{[18]}\)

$$I_{DS} = \left( \frac{W}{2L} \right) C_i \mu_{lin} (V_C - V_T) \ V_{DS}$$

where $C_i$ is the capacitance per unit area of the dielectric, and $\mu_{lin}$ is the field-effect mobility in the linear regime. When $V_{DS}$ is higher than $V_C - V_T$, the conducting channel is pinched off, since the free charge density around the drain contact reduces to nearly (but not quite) zero.\(^{[19]}\) Under this condition, $I_{DS}$ becomes $V_{DS}$ independent, and the device operates through a saturation regime. Thus, the carrier mobility of the transistor can be calculated by Equation (2).\(^{[20]}\)

$$I_{DS} = \left( \frac{W}{2L} \right) C_i \mu_{sat} (V_C - V_T)^2$$

where $\mu_{sat}$ is the mobility in the saturated regime. Transfer curves reflect the conditions of a saturated regime via a plot of $I_{DS}^{1/2}$ against $V_C$ (Figure 1d). This relationship yields a straight line, where the square of its slope is proportional to the charge carrier mobility. Meanwhile, $V_T$ can be obtained by extrapolation to an intercept of the linear part of the $I_{DS}^{1/2}$-$V_C$ plot. Considering that the determination of $V_T$ is sometimes ambiguous, one can employ $V_{ON}$ as a parameter for describing the $V_C$ needed to turn the device on, that is, the potential at which $I_{DS}$ starts to flow because of field-induced charge accumulation at the semiconductor/dielectric interface.\(^{[21]}\) The on-state and off-state currents of FETs can be obtained from the transfer characteristics to afford $I_{ON}/I_{OFF}$, which directly reflects the control of an applied gate bias over the conductive channel. The SS is defined as the inverse of the maximum slope of the logarithmic $I_{DS}$ plot (expressed as $V$/decade) and can be extracted from a transfer curve based on the relationship from Equation (3).\(^{[16]}\)

$$SS = \left( \frac{d \log I_{DS}}{dV_C} \right)_{max}^{-1}$$

Note that lower SS values lead to higher switching speeds and lower power consumption. Thus, low values of SS ($<< 1$) are desirable for improving the ratio between on- and off-currents and making the FET more energy efficient.\(^{[16,19]}\)

Beyond these key parameters, the operating voltages and device stability are also important for practical applications of transistors. FETs based on SiO$_2$ dielectrics suffer from high-operating voltages with tens or hundreds of volts. This limits application in wearable devices, where safety and low power consumption are important factors for adoption. For example, low voltage ($< 5$ V), flexible FETs have been demonstrated through the incorporation of high-capacitance polyelectrolytes as gate dielectrics.\(^{[22–24]}\) Semiconductor materials and processing methods largely determine the performance of FETs. Elemental semiconductors such as amorphous silicon (a-Si) and polycrystalline silicon (poly-Si) were commonly employed for FETs in the electronic industry.\(^{[1]}\) The development of novel semiconductor materials using inorganic compounds, organic conjugated molecules, quantum dots, and 2D nanomaterials for high-performance FETs such as metal–oxide–semiconductor FETs (MOSFETs), organic FETs (OFETs), quantum dot FETs (QFETs), show promising results for integration within next-generation devices.\(^{[19,25–27]}\) Inorganic group-VI (O, S, Se, and Te) materials are recognized as excellent semiconductor candidates for FETs within dedicated applications such as transparent electronics, large-area thin film electronics, active matrix displays, inverters, ring oscillators, and integrated circuits.\(^{[16,21,28]}\) Several examples of metal oxides (MOs) and metal chalcogenides (MCs) have attracted remarkable attention in the development of thin-film transistors (TFTs) and emerging applications,\(^{[10,29–31]}\) indicating good potential for the development of high performance...
Table 1. Comparison of several typical film growth techniques utilized for transistor fabrication.

| Technique                        | ALD     | CVD     | Solution processing | Sputtering | Thermal evaporation |
|----------------------------------|---------|---------|---------------------|------------|--------------------|
| Step coverage                    | Excellent | Good   | Poor                | Moderate   | Moderate           |
| Fine thickness control           | Excellent | Good   | Moderate            | Moderate   | Good               |
| Film uniformity                  | Excellent | Good   | Moderate            | Poor       | Good               |
| Interface quality                | Excellent | Good   | Moderate            | Moderate   | Good               |
| Processing temperature           | Low     | High    | Low                 | High       | Moderate           |
| Compatibility with flexible substrate | Good     | Poor    | Excellent           | Moderate   | Good               |
| Large-area scalability           | Moderate | Moderate | Excellent           | Moderate   | Good               |
| Growth rate                      | Low     | Moderate | High               | High       | Moderate           |
| Manufacturing cost               | High    | Moderate | Low                | Moderate   | Moderate           |

electronic/optoelectronic devices as well as integrated systems with state-of-the-art silicon electronic and photonic devices.

Beyond innovation of semiconductor materials, research and development of transistors have also been driven by the fast-developing application of fabrication technologies such as solution-processing, thermal evaporation, sputtering, chemical vapor deposition (CVD), atomic layer deposition (ALD), and many others.\cite{42,48–51} Table 1 briefly compares the advantages and disadvantages of these different film growth techniques. In particular, ALD is recognized for producing thin-films with good conformity and reproducibility. These attractive features are beneficial for the fabrication of high-quality semiconductor films and dielectric layers in FETs at the nanoscale.\cite{52}

An ALD protocol is comprised of a series of self-limiting surface reactions between gaseous precursors at the interface of a solid substrate.\cite{53,54} Alternating pulse and purge sequences of different precursor reactants supplied using an inert carrier gas ensure that only selective self-limiting reactions occur (Figure 2a). The sequential nature isolates reactants, which greatly enhances control over the chemisorption reaction at surface-active growth sites. In this manner, the film thickness may be tuned according to the number of ALD cycles, affording angstrom level precision.\cite{55} In addition, low growth temperatures and the conformal coating capabilities of ALD make it compatible with a greater variety of flat and curved substrates.\cite{56–59} The demonstration of ALD in fabricating numerous types of thin-film materials including pure elements, oxides, chalcogenides, carbides, nitrides, and phosphates on various rigid or flexible supports, highlights its adaptability.\cite{60–63} A variety of bandgap-tunable MO materials have been fabricated using ALD techniques for applications as semiconductor channels, electrodes, and electrode interlayers in TFTs.\cite{54–67} Further adaptations of ALD have yielded MO insulators integrated as gate dielectrics and encapsulating layers in FETs.\cite{68–70} An increased focus on 2D materials for applications within FETs has stimulated further interest in layered materials such as transition metal chalcogenides (TMCs).\cite{28,31,71,72} Furthermore, ALD-fabricated TMC semiconductors have been combined with conventional silicon-based devices to produce hybrid devices, enabling the integration of flexible designs.\cite{73,74} The large variety of semiconductor materials (Figure 2b) fabricated by ALD, indicates its potential as a transistor component manufacturing method. Thus, the integration of ALD-MOs and MCs within FETs may serve to improve the performance of existing designs, as well as provide complementary and novel properties for next-generation electronic/optoelectronic devices.

In this article, we aim to present recent advances in the transistor-based applications of ALD MOs and MCs. Emphasis is placed on the tunability of materials using ALD, the influence of ALD on the performance optimization of FETs as well as device applications. The review will first explore the application of ALD for various MO materials used as channel, dielectric and
were deposited by ALD, which performed promisingly upon with precisely controlled thicknesses and adjustable properties integration within FET devices. Recently, uniform Mo films as semiconductors or insulators, according to the differences in band position and bandgaps. Over the past decades, MOs have gained attention for electronic applications due to their tunable structures, unique properties, and facile processing methods. MOs are generally grouped as semiconductors, with a focus on their high-performance semiconductors, with a focus on their opportunities and challenges in future electronics.

2. ALD of Metal Oxides for FETs

Over the past decades, MOs have gained attention for electronic applications due to their tunable structures, unique properties, and facile processing methods. MOs are generally grouped as semiconductors, with a focus on their high-performance semiconductors, with a focus on their opportunities and challenges in future electronics.

2.1. Metal Oxide Semiconductors

MO semiconductors, with tunable bandgap values from 1 to 3 eV, are promising transparent channel materials that have attracted great interest in the microelectronics industry. Binary MO semiconductors deposited by ALD, such as ZnO, In2O3, SnO, and TiO2, have exhibited transport and switching properties meeting the prerequisites for applications in FETs. Besides, multinary MO semiconductors such as indium oxide (IZO) and indium gallium zinc oxide (IGZO) can be effectively fabricated by facile modification of existing ALD processes. Compared with binary MOs used for FETs, multinary MO semiconductors have been demonstrated to deliver more attractive device performance, such as higher mobility, better stability, lower leakage current, and smaller SS. In addition to the success of n-type MO semiconductors, p-type MO materials such as SnO, CuO, and Cu2O as well as emerging alternatives, are also involved in this review due to their significant roles in new-generation electronics. Table 2 summarizes key electrical performance

Table 2. Device characteristics of representative FETs using semiconducting MOs synthesized by ALD techniques.

| Material   | Method | T_{ALD} [°C] | Precursors | Pre | n-type | p-type | $\mu$ [cm$^2$ V$^{-1}$ s$^{-1}$] | $I_{ON}/I_{OFF}$ | SS [V dec$^{-1}$] | $V_T$ [V] | Ref. |
|------------|--------|--------------|------------|-----|--------|--------|--------------------------------|----------------|----------------|---------|------|
| ZnO        | ALD    | 170          | DEZn + H2O | -   | 17     | -      | $10^4$                         | -              | -              | -       | [86] |
| ZnO        | ALD    | 100          | DEZn + NH3 + H2O | -   | -      | -      | $10^5$                         | -              | -              | -       | [87] |
| ALD        | ≤ 110  | 20.2         | DEZn + H2O | -   | 10     | -      | $0.38$                         | 2.4             | -              | -       | [88] |
| SALD       | 200    | 17           | DEZn + H2O with NH3 | -   | -      | -      | -                             | -              | -              | -       | [89] |
| PEALD      | 200    | 11.3         | -          | -   | -      | -      | 2.2                           | -              | -              | -       | [90] |
| InOx       | ALD    | 150          | InCA-1 + H2O | -   | 10     | -      | $0.63$                         | -              | -              | -       | [91] |
| PEALD      | 100–250| 39.2         | -          | -   | -      | -      | 0.2                           | -              | -              | -       | [92] |
| In2O3      | ALD    | 225          | TMIn + H2O | 4   | $10^10$| -      | 0.13                          | -              | -              | -       | [93] |
| ALD        | 300    | 4.18         | DADI + ozone | 10  | -      | -      | $0.8$                         | -              | -              | -       | [94] |
| SnO2       | ALD    | 91           | TMT + H2O plasma | $8.23 \times 10^{-5}$ | - | - | - | - | - | - | [95] |
| PEALD      | 60     | 12           | Sn(DMP)$_2$ + O$_2$ plasma | - | - | - | - | - | - | [96] |
| PEALD      | 70–130 | 6.24         | Sn(dmp)$_2$ + O$_2$ plasma | 2 | - | $10^6$ | 1.8 | - | - | [97] |
| SnO        | ALD    | 150–210      | Sn(dmp)$_2$ + H$_2$O | - | $10^6$ | - | 1.8 | - | - | [98] |
| ALD        | 200    | 16.6         | Sn(dmp)$_2$ + H$_2$O | 1.6 | $12 \times 10^6$ | 0.1 | 3.5 | - | - | [99] |
| CuO        | ALD    | 100          | (hfac)Cu(i)(DMB) + O$_2$ | - | - | - | - | - | - | [100] |
| Cu$_2$O    | PEALD  | 160–240      | Cu$_2$(Bu-Me-amd)$_2$ + O$_2$ plasma | 0.1 | $10^1$ | - | - | - | - | [101] |
| TiO$_2$    | ALD    | 150          | TMAT + H$_2$O | 6.7 | $2.5 \times 10^6$ | 0.35 | 6.5 | - | - | [102] |
| ALD        | 250    | 400          | TMAT + H$_2$O | - | - | - | - | - | - | [103] |
| InSnO      | ALD    | 225          | TMIn/TDMASn + H$_2$O | 28 | $3.3 \times 10^2$ | 0.08 | 0.33 | - | - | [104] |
| InZnO      | SALD   | 160          | DEZn/TMIn + O$_2$ plasma | 32 | - | - | 0.25 | - | - | [105] |
| NbZnO      | ALD    | 175          | DEZn(Nb(OEt)$_3$ + H$_2$O | 7.9 | $10^4$ | 0.34 | 8.5 | - | - | [106] |
| InGaZnO    | SALD   | 200          | DEZn/TMIn/TiGa + H$_2$O | 3.5 | $10^3$ | 0.8 | 2.25 | - | - | [107] |
| MgZnO      | ALD    | 200          | Mg(CpEt)$_2$/DEZn + H$_2$O | 3.6 | $7 \times 10^6$ | 0.8 | 8.1 | - | - | [108] |
| AlZnO      | ALD    | 150          | DEZn/TMA + H$_2$O | 6 | - | - | - | - | - | [109] |
| HfZnO      | ALD    | 200          | TEMAH/DEZn + H$_2$O | 4.2 | - | - | 0.52 | - | - | [110] |

Note that DEZn is diethylzinc; InCA-1 is [1,1,1-trimethyl-N-(trimethylsilyl)silanaminato] indium; DADI is (3-(dimethylamino)propyl) dimethylindium; Et$_3$InN(SiMe$_3$)$_2$ is diethyl[bis(trimethylsilyl) amido]indium; TM is tetramethylindium; (hfac)Cu(i)(DMB) is hexafluoroacetyl-acetone Cu(i) (3,3-dimethyl-1-butene); TMAT is tetrakis(dimethylamino) titanium(IV); Cu$_2$(Bu-Me-amd)$_2$ is bis(N,N'-di-sec-butylacetamidinato)dicopper(I); TMIn is trimethylindium; TDMASn is tetrakis(dimethylamino)tin; TEGa is triethyl gallium; TMGa is trimethylgallium; Nb(OEt)$_3$ is niobium pentaethoxide; Mg(CpEt)$_2$ is bis(ethylcyclopentadienyl) magnesium; TMA is trimethylaluminium; TEMAH is tetrakis(trimethylsilyl)amino-hafnium.

Encapsulating materials within FETs, as well as electrode and electrode interlayers. The latter section will discuss MC materials as high-performance semiconductors, with a focus on their applications in FETs as well as their opportunities and challenges in future electronics.

2.1. Metal Oxide Semiconductors

MO semiconductors, with tunable bandgap values from 1 to 3 eV, are promising transparent channel materials that have attracted great interest in the microelectronics industry. Binary MO semiconductors deposited by ALD, such as ZnO, In$_2$O$_3$, SnO, and TiO$_2$, have exhibited transport and switching properties meeting the prerequisites for applications in FETs. Besides, multinary MO semiconductors such as indium oxide (IZO) and indium gallium zinc oxide (IGZO) can be effectively fabricated by facile modification of existing ALD processes. Compared with binary MOs used for FETs, multinary MO semiconductors have been demonstrated to deliver more attractive device performance, such as higher mobility, better stability, lower leakage current, and smaller SS. In addition to the success of n-type MO semiconductors, p-type MO materials such as SnO, CuO, and Cu$_2$O as well as emerging alternatives, are also involved in this review due to their significant roles in new-generation electronics. Table 2 summarizes key electrical performance...
parameters of some representative FETs based on various MO semiconductors fabricated using ALD under different conditions.

2.1.1. Zinc Oxide

Due to a wide bandgap of 3.37 eV, zinc oxide (ZnO) is a promising transparent oxide semiconductor and attracts great attention for applications in solar cells and TFTs.\[103,104\] ZnO-based TFTs exhibit notable performance characteristics such as a high \(I_{\text{ON}}/I_{\text{OFF}}\) ratio of 10\(^9\) and a mobility of 80 cm\(^2\) V\(^{-1}\) s\(^{-1}\).\[86,105–107\] Synthesis of ZnO by ALD commonly uses diethyl zinc (DEZ) as a precursor.\[87,108\] ALD-fabricated ZnO films deposited at a low reaction temperature (80 to 250 °C), exhibit excellent \(I_{\text{ON}}/I_{\text{OFF}}\) (10\(^9\)) and mobility (50 cm\(^2\) V\(^{-1}\) s\(^{-1}\)) metrics.\[86,109\] However, deposition temperature greatly influences the electrical properties of ALD-ZnO films.\[110\] Mobility decreases at low deposition temperatures, in contrast, the \(I_{\text{ON}}/I_{\text{OFF}}\) increases.\[109\] High deposition temperatures can generate greater numbers of defects such as oxygen vacancies, resulting in increased carrier mobility of ALD-ZnO films.\[110\] Correspondingly, oxide film defects resulting from low temperatures can be passivated by O-H species, which will reduce the mobility, but increase the \(I_{\text{ON}}/I_{\text{OFF}}\).\[112\] Generally, ALD-ZnO films fabricated using higher deposition temperatures exhibit higher carrier concentrations (\(\geq 10^{19}\)), much higher than the appropriate carrier concentration of \(\approx 10^{14–10^{17}}\) for the traditional MO channel layer.\[111\]

It was reported that post-annealing in an oxygen atmosphere could efficiently reduce the carrier concentration, thus obtaining high-quality ZnO films with appropriate semiconductor-related properties.\[113,114\] For instance, the electrical performance of ALD-ZnO films deposited at a relatively high temperature (\(\approx 200–250 \, ^\circ\text{C}\)), is improved by a post-annealing at 300 °C in \(O_2\).\[110\] The annealed ZnO films exhibit similar transfer characteristics as films fabricated at lower temperatures. Besides the high-temperature-deposited films, Bang et al. also improved the electrical performance of low-temperature-deposited ZnO films via higher temperature post-annealing treatment.\[114\] The ALD-ZnO film deposited at 100 °C using DEZ, showed good device performance with a mobility of 1.2 cm\(^2\) V\(^{-1}\) s\(^{-1}\) and an \(I_{\text{ON}}/I_{\text{OFF}}\) of 3.1 \times 10\(^6\), which can be further improved to 1.8 cm\(^2\) V\(^{-1}\) s\(^{-1}\) and 1.7 \times 10\(^7\), respectively, after post-annealing the ALD-ZnO film at 250 °C in ambient air. As a consequence, the SS decreased from 0.53 to 0.34 V dec\(^{-1}\). The enhanced electrical performance of ZnO transistors can be attributed to the formation of a Zn-rich phase between the semiconductor layer and the metal electrode during the post-annealing treatment, which may increase the carrier concentration at the metal/semiconductor interface and decrease the contact resistance. Higher annealing temperatures cause faster diffusion of metal atoms, resulting in a rougher interface. Thus, the highly conducting Zn-rich phase may alter the length of the semiconducting channel.

In addition to the deposition temperature, oxygen source is another critical factor that affects the quality of ALD-ZnO films. Strong oxidants such as \(O_3\) yield smaller average grain sizes in comparison to \(H_2O\) in application with DEZ (Figure 3a,b).\[115\] X-ray diffraction (XRD) analysis shows additional changes in the preferred grain orientation of ZnO film, indicating the tunability of growth direction according to oxidant selection (Figure 3c). The two ALD-ZnO films and their bilayer structure can be employed as n-type channels in TFTs (Figure 3d). Analysis of their individual transfer curves clearly indicates that the \(O_3\)-derived ZnO film shows better electrical performance than the \(H_2O\)-derived ZnO film (Figure 3e). Moreover, by using the \(H_2O\)-derived ZnO interlayer to decrease the interfacial trap density, the resulting bilayer ALD-ZnO channel shows improved electrical performance relative to the single layer channel (Figure 3e–h).

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**Figure 3.** a,b) Scanning electron microscope (SEM) images and c) XRD patterns of ALD-ZnO films derived from \(H_2O\) (a) and \(O_3\) (b) as the reactant agent, respectively. d) Schematic of ALD-ZnO TFTs with the single and double channel structures. e) Transfer and f) output curves of ALD-ZnO TFTs with the single and bilayer channel structures. g) Transfer characteristics of the bilayer ALD-ZnO TFTs with varying thicknesses of the \(H_2O\)-derived ZnO interlayer. h) Trend in mobility (black), \(V_T\) (red), and SS (blue) of the ALD-ZnO TFTs with different channel structures. Reproduced with permission.\[115\] Copyright 2020, Elsevier.
Upon increase to the interlayer thickness, the SS of the TFTs decreases while the mobility increases significantly. However, when its thickness exceeds 7 nm, the electrical performance starts to degrade again (Figure 3g–h). As a result, the optimized bilayer ALD-ZnO TFTs deliver a highly improved mobility of 31.1 cm$^2$ V$^{-1}$ s$^{-1}$ with a low $V_T$ of 0.14 V, a large $I_{ON}/I_{OFF}$ of $10^8$, a small SS of 0.21 V dec$^{-1}$, and a good positive bias stress stability.

Assisted by the generation of oxygen vacancies, ALD-ZnO films are considered intrinsic n-type semiconductors. However, Guziewicz et al. has demonstrated successfully the deposition of p-type ZnO semiconductors through in situ nitrogen doping. During the ALD process, an ammonia water solution was used as an oxygen source instead of pure water or oxygen, and the film was annealed briefly in a nitrogen atmosphere after deposition. As a result, the N-doped ZnO exhibited a p-type characteristic with a Hall carrier concentration of $\approx 10^{18}$ cm$^{-3}$. Moreover, a p-n homojunction was demonstrated by depositing an n-type ZnO layer onto the p-type ZnO, showing an $I_{ON}/I_{OFF}$ close to $10^6$.

ALD-ZnO also shows good potential for application within transparent and flexible electronics because of its high transmittance and low-temperature processing requirements. For instance, ZnO-based transparent TFTs with good optical transmission in the visible range were successfully fabricated using ALD on transparent glass substrates at a temperature below 100 °C. Separated by a dielectric of ALD-Al$_2$O$_3$/HfO$_2$/Al$_2$O$_3$, the ALD-ZnO film acted as both a channel material and a gate electrode. Flexible TFTs using the ALD-ZnO channel and TiO$_2$/Al$_2$O$_3$ passivated layers were also achieved on plastics at low temperatures. The flexible ALD-ZnO TFTs showed outstanding electrical performance with electron mobility of $\approx 17$ cm$^2$ V$^{-1}$ s$^{-1}$, an $I_{ON}/I_{OFF}$ of $10^5$, and a SS of 0.4 V dec$^{-1}$.

With the use of plasma-enhanced ALD (PEALD), flexible ZnO-based TFTs have been fabricated via the deposition of ZnO thin-films onto PI substrates. The TFTs deposited on a 3.5 μm flexible PI substrate exhibit comparable electron mobility (1.3 ± 1.2 cm$^2$ V$^{-1}$ s$^{-1}$) and $V_T$ (2.2 ± 0.3 V) values to those of TFTs on a glass substrate (Figure 4a). Investigation of device performance before and after fold-induced mechanical stress (Figure 4b), shows a negligible degradation of mobility and $V_T$. The practical application of ZnO-based TFTs was further demonstrated using a cross-coupled LC oscillator circuit, with the flexible PI substrate outperforming analogous TFTs deposited onto glass. Using a $V_{supply}$ of 9 V, the oscillation frequency ($f_{OSC}$) measured 17 MHz (Figure 4c), well above the cutoff frequency ($f_c$) for operation on glass substrates (12.9 MHz).

Printed inverters using ZnO-based TFTs (Figure 4d) were prepared using a modified version of ALD, which applies spatial isolation techniques to achieve ALD (SALD). The fabricated TFTs (Figure 4e) exhibited excellent electrical performance with high mobility (15 cm$^2$ V$^{-1}$ s$^{-1}$). Furthermore, inverters arranged within a five-stage, enhancement-mode ring oscillator architecture displayed a frequency response of 2.68 kHz at an input voltage of 20 V (Figure 4f). In conclusion, the tunable nature of ALD has afforded ZnO semiconductors with strong electrical performance upon integration within TFTs. Its compatibility with flexible substrates, along with its performance within integrated circuits, reflects its promise for use within more complex device architectures.
2.1.2. Indium Oxide

Investigation into heavier MOs has demonstrated that indium oxide (In$_2$O$_3$) possesses excellent properties as a wide bandgap (≈3.6 eV) semiconductor/conducting material.[65,106] Deposition of In$_2$O$_3$ using low-temperature ALD yields highly optically transparent (>85%) films, which perform moderately well according to mobility (15 cm$^2$ V$^{-1}$ s$^{-1}$) and $V_T$ (≈−0.2 V) metrics.[116]

Films grown using PEALD with the precursor di-ethyl[bis(trimethylsilyl)amido]indium [Et$_2$In(N(SiMe$_3$)$_2$)] and O$_2$ plasma (100–250 °C) resulted in polycrystalline In$_2$O$_3$, which upon the application within a TFT displayed a significantly better mobility (39.2 cm$^2$ V$^{-1}$ s$^{-1}$).[89] The low voltage threshold and high mobility suggest ALD-In$_2$O$_3$ is an extremely promising candidate for transparent TFT-containing devices.[117] However, In$_2$O$_3$ films grown at low temperatures typically form non-stoichiometric amorphous films with carrier concentrations analogous to metal-like materials, likely resulting from excess oxygen vacancy site formation.[29] Simulations applying density functional theory (DFT) suggest increasing the order of the film leads to an attenuation in the metal-like conductivity.[118] These findings are also supported experimentally. Transmission electron microscopy (TEM) analysis indicates that as-deposited amorphous In$_2$O$_3$ undergoes transformation upon post-deposition annealing at 300 °C within an oxygen atmosphere, resulting in crystalline In$_2$O$_3$.[65] The annealed In$_2$O$_3$ films exhibited improved electrical performance within TFT devices. The mobility was increased from 20.12 to 41.82 cm$^2$ V$^{-1}$ s$^{-1}$, the SS was decreased from 400 to 100 mV dec$^{-1}$, and the $V_T$ was reduced from −6.7 V to −0.8 V.

In another study, amorphous InO$_x$, deposited at 150 °C was post-treated with N$_2$O plasma under different exposure times (600–2400 s) to investigate the effects on device performance (Figure 5).[79] Prolonged plasma exposure leads to an increase in roughness of the InO$_x$ surface and a considerable decrease in O-deficiency (Figure 5g). The TFTs made by using the plasma-treated InO$_x$ films transit from a metal-like conductor to a semi-conducting device. The switching performances such as the $I_{ON}/I_{OFF}$ are greatly improved with an increase in the plasma time (Figure 5d). The low-temperature approach enabled further investigation into flexible ALD-InO$_x$ TFTs through deposition on a PI substrate (Figure 5a). Repetitive bending tests were carried out to evaluate the electrical performance of the flexible TFTs with two different bending axes, along the channel length (case I, Figure 5b) and along the channel width (case II, Figure 5c), respectively. For case I, the $V_T$ shifts gradually in a negative direction after 3000 bending cycles, whilst the mobility and SS exhibit only slight changes (Figure 5e,h). However, more dramatic changes were measured for case II. After 700 bending cycles, the mobility and $V_T$ decrease dramatically, while the SS increases drastically (Figure 5f,i). These results suggest that ALD-fabricated InO$_x$ films may be suitable for integration within flexible TFT devices. However, the TFT architecture influences durability significantly. Furthermore, both methods demonstrating stoichiometric enrichment of amorphous InO$_x$ utilize oxygen enrichment post-processing techniques at significantly different temperatures, suggesting the barrier of formation for In$_2$O$_3$ is kinetic in nature. Further mechanism investigation may assist in supporting this correlation as well as assisting in the optimization of future ALD protocols.

2.1.3. Tin Oxides

Tin dioxide (SnO$_2$), a wide bandgap (≈3.6 eV) n-type semiconductor, exhibits excellent electrical properties such as large electron mobilities (≤147 cm$^2$ V$^{-1}$ s$^{-1}$) and high $I_{ON}/I_{OFF}$ ratios (10$^4$).[75,119–121]

Deposition of high-quality SnO$_2$ films may be achieved using a range of tin precursors such as TDMASn,[66,122] dimethylaminomethyl-2-methyl-2-propoxy-tin(II) [Sn(dmamp)],[92] and tetrakis-(dimethylamino)propyl tin(IV) [Sn(DMP)].[75] SnO$_2$ films deposited using Sn(DMP)$_2$ and oxygen plasma at low temperatures (60 °C) feature small hillocks (a low surface roughness value of 0.22 nm, Figure 6a).[75] Evaluation of transfer characteristics within bottom-gate TFTs indicates that the film thickness greatly influences mobility and $V_T$ (Figure 6b,c). In thicker layers, the bulk SnO$_2$ remains in a non-depleted state, causing parallel conduction. In comparison, thin films suffer from surface roughness scattering. However, at an optimized film thickness (6 nm), the TFTs display typical n-type output and transfer characteristics (Figure 6d,e), yielding an electron mobility of 12 cm$^2$ V$^{-1}$ s$^{-1}$ and an $I_{ON}/I_{OFF}$ of 10$^4$. The deposition temperature of ALD-SnO$_2$ has also been demonstrated to influence electrical performance.[92] Improvements in channel mobility (2.31 to 6.24 cm$^2$ V$^{-1}$ s$^{-1}$) and $V_T$ (7.47 to 1.88 V) are observed upon increasing deposition temperature (70 to 130 °C). Above 130 °C, carrier concentration increases in tandem with a decrease in resistivity (Figure 6f), resulting in conductor characteristics. By contrast, room-temperature ALD-SnO$_2$ using tetramethyltin [Sn(CH$_3$)$_4$] and plasma-excited humidified argon, can also be used as a channel material to display n-type behaviors but with pretty low mobility (8.23 × 10$^{-5}$ cm$^2$ V$^{-1}$ s$^{-1}$).[91]

Differing from SnO$_2$, tin monoxide (SnO) behaves as a p-type semiconductor with a wide bandgap (≤3.0 eV) and offers a moderate field-effect mobility (≤6.75 cm$^2$ V$^{-1}$ s$^{-1}$).[123,124] Although a variety of studies on tin oxides synthesized by ALD have been reported, it is still a challenge to obtain high-quality p-type SnO films.[80,93] Han et al. demonstrated tunability of Sn/O film composition through the use of different oxygen-containing co-reactants.[123] Reactions using a strong oxidant such as O$_3$ or O$_2$ plasma yielded n-type SnO$_2$ films, whilst H$_2$O afforded SnO films. Deposition temperature also influenced morphology with higher temperatures (150–210 °C) resulting in greater SnO crystallinity and corresponding improvements to the electrical performance of ALD-SnO TFTs (Figure 7a,b).[91] The increased $I_{ON}/I_{OFF}$ is mainly attributed to effective reduction of extrinsic hole concentrations in the SnO films, while the improved mobility may result from the increased grain size of ALD-SnO films grown at relatively high temperatures. Optimization of TFT channel thickness using ALD demonstrated further improvements in TFT performance (Figure 7c). The optimized ALD-SnO TFTs exhibited interesting electrical performance with a hole mobility of ≈1 cm$^2$ V$^{-1}$ s$^{-1}$, an $I_{ON}/I_{OFF}$ of 2 × 10$^4$, and a SS of 1.8 V dec$^{-1}$. Diffusion of Sn(IV) into the SiO$_2$ insulator layer forms trap sites during both ALD and post-annealing, leading to poor device
Figure 5. a) Photograph of the flexible ALD-InOx TFTs based on PI substrates. b,c) Schematic of InOx TFTs with two bending axes along the channel width (b, case I) and the channel length (c, case II), respectively. d) Transfer curves of TFTs based on the ALD-InOx with different N2O plasma time. e,f) Transfer curves and h,i) the corresponding change in Vth, mobility and SS at different bending cycles of flexible InOx TFTs with case I bending (e and h) and with case II bending (f and i). g) Change in the surface roughness and O-deficiency of InOx films with an increase of N2O plasma treatment time. Reproduced with permission. [79] Copyright 2016, American Chemistry Society.
performance. Adoption of an insulating Al2O3 interfacial layer (IL) between the SiO2 gate dielectric and ALD-SnO2 channel layer reduces trap site density (Figure 7d,e). Comparison of Al2O3 IL thickness (Figure 7f–i) highlights the effects of ILs upon hysteresis voltage (V_hys) with significant attenuation of V_hys observed at 5 nm. Further optimization of the Al2O3 IL afforded a V_hys of 0.2 V, a mobility of 1.6 cm² V⁻¹ s⁻¹, and an I_ON/I_OFF of 1.2 × 10⁶.

In short, both SnO2 and SnO films made by ALD show good potential as semiconductor channel materials in FETs for promising applications in transparent and flexible electronics. The adaptability of ALD protocols also highlights its capacity to optimize tin oxide thin films for electronic applications. Finally, combining p-type and n-type tin oxides to construct p-n junctions, inverters or other complex structures by ALD will also be a promising and significant direction toward advanced electronics in the future.

2.1.4. Other Binary Metal Oxides

Semiconducting titanium oxide (TiO2) has also attracted extensive interest in the field of FETs due to its high transparency, good stability, and low-cost growth process. Excellent electrical performance characteristics, such as a high field-effect mobility of ~10 cm² V⁻¹ s⁻¹, attribute further to the use of TiO2 as a promising channel material.

Early reports revealed that high-quality TiO2 films fabricated by ALD can be applied as channel materials in FETs. Ali et al. demonstrated TFT applications of TiO2 using thermal ALD in conjunction with post-annealing. The annealed TiO2 film exhibited efficient electronic performance, with electron mobility of 0.672 cm² V⁻¹ s⁻¹, an I_ON/I_OFF of 2.5 × 10⁶, and a SS of 350 mV dec⁻¹. Although TiO2 is typically considered as an n-type semiconductor material owing to oxygen vacancies, p-type behavior has also been demonstrated. Application of epitaxial growth mechanisms using ALD in combination with a [001] oriented Al2O3 substrate, can afford p-type TiO2 (anatase) thin films. Furthermore, variation in post-annealing conditions demonstrated that TiO2 may be natively p-type and hole mobility may be further enhanced through titanium deficiencies.

Copper oxide (CuO) and cuprous oxide (Cu2O), another family of promising binary oxide channel materials, likewise show p-type behaviors and comparable electrical performance in electronic applications. The influence of post-annealing temperatures on the optical, electrical, and chemical properties of ALD-CuOx films deposited at 100 °C, were recently investigated by
Maeng et al. Spectroscopic ellipsometry and X-Ray photoelectron spectroscopy were used to distinguish the relationship between the optical bandgap and annealing temperature of the deposited films (Figure 8a,b). The band edge position of ALD-CuO$_x$ films with controlled energy levels clearly relies on annealing temperatures. The as-deposited ALD-CuO$_x$ film has an optical bandgap of $\approx 2.17$ eV which then decreases to 2.08, 1.47, 1.43, and 1.43 eV according to the annealing temperatures of 200, 300, 400, and 500 °C, respectively. The electrical properties of the ALD-CuO$_x$ films were evaluated via TFT devices, revealing typical p-type transfer characteristics (Figure 8c). The as-deposited CuO$_x$ exhibits a low $I_{ON}/I_{OFF}$ in addition to a high SS (Figure 8d), which may be attributed to poor stoichiometry at lower temperatures resulting in greater conducting behavior. The higher temperatures used during the annealing process enhance stoichiometry and thus crystallinity, leading to better semiconductor performance output. As a result, the optimized TFTs using ALD-CuO$_x$ film annealed at 300 °C showed overall improvement in electrical performance, such as the increased hole mobility and $I_{ON}/I_{OFF}$ of 5.64 cm$^2$ V$^{-1}$ s$^{-1}$ and 10$^5$, respectively. However, the formation of grain boundaries at 500 °C hinders the carrier transport, suppressing further enhancements in TFT performance achieved using post-deposition annealing. Compared with typical p-type CuO and Cu$_2$O, some emerging metal halide semiconductors, such as p-type cuprous halides (i.e., CuBr, CuI, and Zn-doped CuI) and metal halide perovskites, can deliver better device performance of FETs. In particular, a very recent report by Liu and Noh et al. presented p-channel perovskite FETs based
Figure 8. a) Tauc plot of the optical absorption and b) energy level diagram for the as-deposited ALD-CuOx films and the annealed films at different temperatures. c) Transfer curves of TFTs based on the ALD-CuOx films. Reproduced with permission.[94] Copyright 2016, Elsevier. d) Statistics of $\mu$, $V_{T}$, SS, and $I_{ON}/I_{OFF}$ depending on the annealing temperature, where these data were collected from the Ref. [94]. on cesium tin triiodide (CsSnI$_3$). The resultant FETs exhibited large field-effect hole mobilities (>50 cm$^2$ V$^{-1}$ s$^{-1}$), high $I_{ON}/I_{OFF}$ ratios of 10$^6$, and excellent operational stability, demonstrating their promising potential for advanced electronics.[134] Currently, there are several reports on the ALD of metal halides.[135,136] However, these ALD-metal halides are isolated nanoparticles and evaluations of their semiconductor characteristics are not reported. Therefore, the research emphasis on high-quality ALD p-type semiconductors should not be limited to MOs. Metal halides and other inorganic hybrid materials are also promising avenues for exploration. The atomic layer control afforded by ALD is highly advantageous for the further development of conventional and emerging p-type semiconductor channels and may yield new high-performance transistors for electronic/optoelectronic applications.

2.1.5. Multinary Metal Oxides

Multinary MOs such as IZO and amorphous indium gallium zinc oxide (a-IGZO) are emerging as novel semiconductor materials for TFTs due to their flexible compositions and excellent electrical properties in contrast to conventional binary MOs.[83,84] The influence of elemental composition on the electrical properties of multi-metal semiconductors has been well established within literatures.[84,85] For example, minor compositional alteration of a-IGZO from In$_{0.45}$Ga$_{0.15}$Zn$_{0.40}$O to In$_{0.38}$Ga$_{0.18}$Zn$_{0.44}$O results in an 18% reduction in mobility from 48.3 to 39.4 cm$^2$ V$^{-1}$ s$^{-1}$.[85] In this respect, ALD affords facile tunability of metal precursor ratios; it enables the fabrication of multinary MOs in a precise manner. A unique approach accessible only using ALD applies the standard half-reaction protocol, but includes an additional separate half-reaction with a different metal precursor during the growth cycle.[97] For example, alternating bilayers of In$_2$O$_3$ and ZnO were deposited according to a fixed ratio of 0.6 (6:4 half-reactions per cycle, respectively), resulting in a pseudo-multinary semiconducting heterostructure.[137] Furthermore, selective deposition of the initial In$_2$O$_3$ layer onto the dielectric interface significantly improves TFT performance in comparison to a reverse ZnO-first architecture. Indeed with field-effect mobility (1.07 to 6.5 cm$^2$ V$^{-1}$ s$^{-1}$), and $I_{ON}/I_{OFF}$ ($5.2 \times 10^6$ to $5.0 \times 10^7$) are greatly improved whilst $V_T$ (10 to 8.9 V) and SS (1.85 to 0.7 V dec$^{-1}$) are deteriorated. In another study, Illiberi and coworkers deposited IZO using spatial-ALD at atmospheric pressure.[83] The ratio of indium/zinc (In/Zn) in the deposited film was accurately tuned by controlling the ratio of In/Zn precursor pulses. A 2:1 In/Zn ratio exhibits both high mobility (> 30 cm$^2$ V$^{-1}$ s$^{-1}$) and good stability. The same team further designed quaternary zinc compounds of indium gallium zinc oxide with tunable electrical properties by adjusting the ALD cycle numbers of each binary MO.[84] The field-effect mobility of indium gallium zinc oxide decreased with an increase in Ga-content, while the corresponding $V_T$ rose significantly (Figure 9a,b). The decreased mobility and increased $V_T$ of oxide TFTs are attributed to the incorporation of
Ga-atoms in IZO, which suppresses oxygen vacancy formation through strong Ga-O bond enthalpy.

It is worth noting that hetero-element doping in binary MOs represents an effective strategy to produce several multinary MOs.\[98\] For example, ZnO has been widely doped with aluminum, boron, indium, niobium, and magnesium, to improve its electrical properties and promote its applications in optoelectronic devices.\[64,98,138–140\] Mg-doped ZnO (MZO) films show gradual bandgap increases from 3.18 eV (binary ZnO) to 3.37 eV (ternary Zn\(_{1-x}\)Mg\(_x\)O) after suitable Mg doping (Figure 9c).\[107\] Nb-dopants also exhibit analogous bandgap tunability when applied to ZnO films.\[89\] Adaptation of precursor ratios during deposition cycles affords further compositional tuning possibilities for MZO films.\[141\] Figure 9d exhibits the influence of Mg content in ALD-MZO films on the TFT performance.\[141\] With a cycle ratio of MgO/ZnO deposition increases from 1:10 to 1:2, the ALD-MZO TFTs deliver suppressed electrical performance with a mobility decreased from 4.32 to 0.47 cm\(^2\) V\(^{-1}\) s\(^{-1}\) and a \(V_T\) increased from 6.05 to 9.51 V. In contrast, the \(I_{ON}/I_{OFF}\) and \(N_{it}\) are almost unchanged.

Among various doped-ZnO materials, Al-doped ZnO (AZO) thin films have received much attention owing to their unprecedented high mobility up to 136 cm\(^2\) V\(^{-1}\) s\(^{-1}\), as well as the low-cost, high abundance, and non-toxic nature of elemental Al.\[143\] Investigation of Al-doping effects on the bias-stress stability of ALD-AZO transistors indicates that 3% Al greatly preserves \(V_T\) hysteresis fidelity, whilst retaining adequate output curve characteristics.\[144\] However, beyond 5% Al the formation of insulating Al\(_2\)O\(_3\) greatly inhibits TFT performance. XRD analysis of the 3%-AZO showed greatly improved grain orientation and size, which is postulated to enhance stability through the attenuation of trap site formation. Hf is also widely used as a doping element for achieving stable ZnO TFTs. Integration of novel channel architectures using n-type Hf-doped ZnO (HZO) has demonstrated improved bias stability, whilst retaining comparable mobility (4.2 cm\(^2\) V\(^{-1}\) s\(^{-1}\)).\[102\] The HZO/ZnO/HZO sandwich heterostructure affords enhanced surface layer stability under ambient conditions, whilst the additional HZO layer in contact with the dielectric interface reduces \(V_T\). Similarly, n-type ZnO/HfO\(_2\) multilayer architecture has been fabricated as a channel in TFTs by ALD (Figure 10a).\[145\] This multilayer structure (TFT-C) exhibits a comparable field-effect electron mobility of \(\approx 13.1\) cm\(^2\) V\(^{-1}\) s\(^{-1}\), but a particularly high \(I_{ON}/I_{OFF}\) of \(\approx 8 \times 10^9\) which is over 7 times higher than that of TFT-A (pure ZnO) and TFT-B.
Figure 10. a) Schematic illustration of TFTs based on ALD-ZnO/HfO$_2$ with various structures and b) their corresponding transfer characteristics. Reproduced with permission.\cite{145} Copyright 2015, AIP Publishing. c) Cross-sectional TEM image and false-colored HRTEM image of the multinary-ZnO film made by ALD. d) Optical image of a NMOS inverter based on the ALD ZnO-based TFT (scale bar: 250 μm). Transfer curves of the TFT measured under e) PBS and f) NBS at room temperature. g) V$_T$ shift for the SL- and ML-ZnO TFTs was compared under PBS and NBS measurements. h) Voltage transfer curves of the NMOS inverter at different V$_{DD}$ values. Reproduced with permission.\cite{146} Copyright 2016, Wiley-VCH.

(ZnO/HfO$_2$) (Figure 10b). A multilayer structure analogous to that of TFT-C was further investigated by HRTEM, as shown in Figure 10c.\cite{146} The multilayer heterostructure affords fully transparent devices and circuits, where all oxide components including the ZnO/HfO$_2$ multilayer channel, AZO electrodes, and HfO$_2$ dielectric were deposited by ALD and entirely indium-free. The TFTs can be fabricated on polyethylene naphthalate (PEN) to deliver high electrical performance ($\mu_{sat}$ of 8.5 cm$^2$ V$^{-1}$ s$^{-1}$, I$_{ON}$/I$_{OFF}$ over 10$^9$, and SS value of 0.201 V dec$^{-1}$). Moreover, the multilayer channel TFTs (ML-TFTs) show a maximum V$_T$ shift of only +0.3 V and −0.1 V after 3000 s of positive bias stress (PBS) and negative bias stress (NBS), respectively, demonstrating the excellent device operational stability (Figure 10e,f). Compared with the single-layer TFTs (SL-TFTs), the ML-TFTs show a comparable V$_T$ shift under the PBS but a much smaller V$_T$ shift under the NBS (Figure 10g), due to efficient passivation of the multilayer ALD-ZnO channel by the ultrathin HfO$_2$ layer. The ML-TFTs based on ALD-ZnO can be further used for designing logic devices such as a negative channel MO semiconductor (NMOS) inverter (Figure 10d), displaying high-performance static voltage transfer characteristics (Figure 10h). The voltage transfer curves exhibit the typical supply voltage (V$_{DD}$) dependent rectangle shape. The output voltage ($V_{out}$) remains the same within the transition voltage ($V_{th}$) and then drops immediately to V$_{GND}$ when the input voltage ($V_{input}$) exceeds $V_{th}$.

In the interest of expanding the catalog of suitable materials for complementary logic circuits, research in p-type MO semiconductors has increased in tandem to the rapid development of novel n-type materials. The above examples highlight how sequential deposition using ALD may be used to fabricate high-quality heterostructures. Thus, ALD remains an extremely promising technique for the development of future p-n-type heterojunctions.

2.2. Metal Oxide Insulators

Over the past decades, several MO insulators have been extensively utilized in electronic devices as gate dielectrics and/or protecting layers due to their high dielectric constant, large optical transparency, and excellent stability.\cite{87,147–150} Combining MO insulators with different semiconductor channel layers can significantly optimize the device performance and stability of FETs. Primarily, MO insulator/channel optimization has been demonstrated to greatly improve mobility, I$_{ON}$/I$_{OFF}$, hysteresis suppression, and operation stability.\cite{69,151} It is worth noting that the trap state generated at the surface/interface of semiconductors such as those of group III-V compounds are influenced by atmosphere or impurities, resulting in poor device performance.\cite{152} Thus, attenuation of trap density is necessary for improving the electrical performance of various FETs. Adoption of ALD-processed MO insulators on group III-V semiconductors suppresses interface trap state formation due to the high quality of oxide–dielectric or -passivation layer deposited.\cite{153} For instance, the ALD-Al$_2$O$_3$/GaAs structure exhibited an upper limit for N$_t$ of 5 × 10$^{11}$–10$^{12}$ cm$^{-2}$ eV$^{-1}$.\cite{154} In this section, MO insulators fabricated by
ALD are discussed. Influences on device performance, contribution as functional dielectrics, and protecting/encapsulating layers in FETs-based electronic devices will be highlighted. Electrical performance parameters and transistor function of representative ALD-MO insulators are summarized in Table 3.

### 2.2.1. Aluminum Oxide

Aluminum oxide (Al₂O₃) is widely applied as an insulator within electronic devices due to its high dielectric constant (k) and wide bandgap.[164,165] Currently, trimethylaluminum (TMA) is the most commonly used aluminum precursor for depositing Al₂O₃ by ALD.[158,159,155] Utilizing an ALD-Al₂O₃ dielectric, MgZnO-based TFTs have shown improved electrical performance compared with devices with a SiO₂ dielectric.[166] The corresponding mobility and the \( I_{ON}/I_{OFF} \) were improved from 5.65 to 7.73 cm² V⁻¹ s⁻¹, and 4.4 × 10⁵ to 1.2 × 10⁷, respectively, while the SS was decreased from 0.80 to 0.29 V dec⁻¹.

ALD-Al₂O₃ has also been used as a gate dielectric layer in TMCs-based FETs to improve their electrical performance.[168] For instance, WSe₂-based FETs coupled with an ALD-Al₂O₃ top-gate dielectric layer exhibited excellent mobility of 70.1 cm² V⁻¹ s⁻¹ and a high \( I_{ON}/I_{OFF} \) of 10⁶.[155] However, the lack of nucleation sites, which are mainly provided by dangling bonds on the surface of TMCs, hinders the formation of a conformal dielectric layer on the channel surface.[167] Moreover, island-like growth of high-\( k \) oxide clusters on the pristine MoS₂ layer easily forms some defects such as pinholes, leading to increased gate leakage currents.[157,158] Therefore, thicker MO dielectrics are required for the top-gated TMD transistors. High-temperature requirements commonly observed for processing MO dielectrics may result in

| Material         | Method | \( T_{ALD} \) [°C] | Precursors[^5] | Function & Device                  | Performance                                                                 | Ref. |
|------------------|--------|---------------------|----------------|------------------------------------|----------------------------------------------------------------------------|-----|
| \( \text{Al}_2\text{O}_3 \) | ALD    | –                   | –              | Interfacial passivation on p-type SnO-based TFTs | An improved \( \mu \) from 1.8 to 5.4 cm² V⁻¹ s⁻¹, a reduced SS from 0.88 to 0.51 V dec⁻¹, and good stability in performance of the passivated SnO TFTs for over 1 year | [80] |
| ALD              | 150    | TMA + H₂O           |                | Organic/inorganic bilayer dielectric on OFETs | An improved \( \mu \) from 0.08 to 0.65 cm² V⁻¹ s⁻¹, a reduced leakage current, and an \( I_{ON}/I_{OFF} \) of 1.6 × 10⁴ | [147] |
| PEALD            | 150    | TMA + O₂ plasma     |                | Dielectric on WSe₂-based FETs | \( \mu = 70.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1} \) and \( I_{ON}/I_{OFF} = 10^6 \) | [155] |
| PEALD            | 250    | TMA + H₂O/O₂ plasma |                | Dielectric on AlGaN/GaN MIS-HEMTs | \( V_F = -5.8 \text{ V} \), \( SS = 68 \text{ mV dec}^{-1} \), \( V_{FF} = 50 \text{ mV} \), and \( I_{ON}/I_{OFF} = 10^{10} \) | [149] |
| \( \text{HfO}_2 \) | ALD    | 150                 | TDMAHf + H₂O   | Dielectric on TMCs-based TFTs | \( SS = 60 (\text{MoS}_2) \) or 67 mV dec⁻¹ (WSe₂), and \( I_{ON}/I_{OFF} = 10^7 \) (MoS₂ with < 5 nm HfO₂) | [70] |
| ALD              | –      | TEMAH + H₂O         |                | Dielectric and blocking oxide on MoS₂-based logic-in-memory devices | A memory window of 10.6 V, and a tunable \( V_F \) of memory devices by adding/removing charge carriers from the floating gate | [157] |
| BeO              | ALD    | 120                 | TDMAHf + H₂O   | Encapsulation on MoS₂-based FETs | Reduced hysteresis and retained on-currents | [157] |
| \( \text{Al}_2\text{O}_3 \) | ALD    | 200                 | TDMAZr + H₂O   | Interlayer between the sapphire substrate and the β-Ga₂O₃ channel | \( \text{ZrO}_2 \) is beneficial for heat transfer from the channel to the sapphire substrate, resulting in a 35% less channel temperature increase | [159] |
| \( \text{Y}_2\text{O}_3 \) | ALD    | 250                 | Y(MeCp)₃ + H₂O | Interlayer between the HfO₂ dielectric and the native SiO₂ layer (< 1 nm) | A negative shift \( V_F \) of 224 mV; an improved \( \mu \) from 228 (the single HfO₂ dielectric) to 278 cm² V⁻¹ s⁻¹ (with the \( \text{Y}_2\text{O}_3 \) interlayer) | [160] |
| \( \text{La}_2\text{O}_3 \) | ALD    | 150                 | La(PrCp)₃ + H₂O | Dielectric on InGaAs-based MOSFETs | \( SS = \approx 80 \text{ mV dec}^{-1} \) for the devices with a 15 nm La₂O₃ dielectric | [161] |
| \( \text{V}_2\text{O}_5 \) | ALD    | 50                  | V(dma)₄ + H₂O  | Charge injection interlayer in OFETs | Three times higher \( I_{ON} \) of OFETs (with \( \approx 10 \text{ nm VO}_2 \)) than that of reference devices, and an improved \( \mu \) from 0.29 to 0.80 cm² V⁻¹ s⁻¹ | [67] |
| TiAlO alloy      | PEALD  | 170                 | TiCl₄ + H₂O    | Dielectric on InGaAs/InP-based MOSFETs | A breakdown field of 5.6 MV cm⁻¹, low-frequency dispersion (≈11%), and \( V_{FF} = 90 \text{ mV} \) | [162] |
| \( \text{Al}_2\text{O}_3/\text{Ta}_2\text{O}_5 \) | –      | –                   | –              | Bilayer dielectric on ZnO-based TFTs | A low leakage current density of \( \approx 10^{-8} \) A cm⁻², an improved \( \mu \) from 0.1 (single Ta₂O₅ dielectric) to 13.3 cm² V⁻¹ s⁻¹ (bilayer Al₂O₃/Ta₂O₅ dielectric), and an \( I_{ON}/I_{OFF} \) of \( 10^4 \) | [147] |

[^5]: Note that TDMAHf is tetrakis(dimethylamino)hafnium; DMBe is dimethylberyllium; TDMAZr is tetrakis(dimethylamino)zirconium; Y(MeCp)₃ is tris(methylcyclopentadienyl) yttrium; La(PrCp)₃ is tris(isopropylcyclopentadienyl)Lanthanum.
oxidation damage to TMC channels. Thus, deposition of high-quality ultrathin MO dielectrics onto novel TMC channel materials remains a challenge for developing new TFT technologies.

The interfacial chemistry of ReS2 was in situ analyzed with XPS during the deposition cycles of Al2O3. Standard PEALD combined with a UV-Ozone pretreatment promotes the formation of weak S=O bonds, which can facilitate nucleation and hence uniformity of the Al2O3 dielectric layer. Thus, the application of non-thermal ALD techniques may be beneficial for suppressing non-ideal surface growth mechanics among TMCs lacking appropriate nucleation density. The deposition of Al2O3 using TMA and water as co-reactants has been widely adopted due to the well-established robustness of the reaction and detailed mechanistic understanding. However, the stability of chemical bonds formed during this process, such as Al-Al and Al-O-H, may lead to unwanted defects, which will influence the performance of final electronic devices. Previous literature has demonstrated that defect suppression occurs when using ozone (O3), through the removal of -OH groups or direct use of O3 as a co-reactant. However, the use of O3 plasma has also demonstrated reduced levels of -OH impurities, resulting in high-quality Al2O3 films. Wang et al. deposited high-quality Al2O3 gate dielectrics by PEALD using both H2O and O2 plasma as oxygen sources within one cycle (Figure 11a down). Compared with a sample without O2 plasma (Figure 11a above), AlGaN/GaN-based metal-insulator-semiconductor high electron mobility transistors (MIS-HEMTs) with the O2 plasma-derived Al2O3 dielectric exhibited improved electrical performance with a much smaller hysteresis (Figure 11b). Moreover, a lower SS of 68 mV dec−1 and a higherIon/Ioff of ≈1010 are achieved compared with a SS of 97 mV dec−1 and an Ion/Ioff of ≈108 for the sample without O2 plasma (Figure 11c).

As discussed above, besides the trap states induced by –OH impurities in the Al2O3 dielectric, surface oxides on the surface of non-oxide semiconductors, particularly for group III-V semiconductors, seriously degrade the electrical performance of final devices. Indeed, eliminating surface oxidation of the semiconductor and reducing the interfacial trap state density are effective strategies to improve the electrical performance of group III-V semiconductor-based MOSFETs. Native oxide ILs on group III-V semiconductors are diminished during Al2O3 deposition by ALD due to the formation of volatile IL products and conversion of interfacial oxides to Al2O3. The so-called interfacial oxide self-cleaning, resulted in lower trap densities and better electrical properties. Moreover, the ALD-Al2O3 dielectric as an encapsulation layer efficiently minimized the moisture-absorption effects on the insulator/semiconductor interface, thus contributing to a more stable interface state and improved electrical performance.

High-temperature induced surface oxidation of the semiconductors whilst depositing high-k oxides by ALD is another factor that leads to the degradation of electrical performance for...
FET-based devices. Therefore, decreasing the ALD temperature for processing MO insulators is an attractive route to improve device performance.\[180\] Decreased temperature during ALD of an Al₂O₃ dielectric layer onto p-type GaSb-based FETs has resulted in an increase in the hole mobility.\[176\] This improvement may be attributed to suppressed oxidation and trap state density at the semiconductor/insulator interface, which is known to easily occur in response to higher ALD temperatures. As a result, compared with the high-temperature derived Al₂O₃, GaSb-based MOSFETs with the ALD-Al₂O₃ dielectric deposited at only 150 °C delivered a highly decreased N_b of 4.5 × 10¹¹ cm⁻² eV⁻¹. Enhanced TFT performance at lower ALD temperatures was also reflected in the deposition of an Al₂O₃ dielectric/passivation layer on a polycrystalline diamond. Devices fabricated at 200 °C displayed a higher output current, larger V_T, and lower on-resistance compared with that deposited at 300 °C.\[180\]

In addition, ALD-processed Al₂O₃ has been also employed as an effective passivation layer to reduce the surface trap density, and thus suppress the threshold voltage hysteresis significantly.\[80\] Si et al. demonstrated enhanced FET performances through the passivation of indium selenide (α-In₂Se₃) by ALD-Al₂O₃.\[175\] Figure 11d presents a top-view SEM image (up) and a schematic device (down) of α-In₂Se₃-FETs with the ALD-Al₂O₃ passivation. Non-passivated FETs exhibit transfer curves with clockwise hysteresis loops with large memory windows (>70 V) at different V_DS values (Figure 11e), whilst I_ON/I_OFF remains above 10⁷ at a V_DS of 0.5 V. By contrast, the ALD-Al₂O₃ passivated FETs exhibit clockwise hysteresis loops with reduced memory windows and an enhanced I_ON/I_OFF of 10⁷ at a V_DS of 1 V, as well as a low SS of 0.65 V dec⁻¹ and a significantly improved mobility of 312 and 488 cm² V⁻¹ s⁻¹ in the forward and reverse sweep, respectively (Figure 11f).

Additionally, the adoption of an ALD-Al₂O₃ passivation interlayer between the p-type SnO film and the SiO₂ dielectric layer can efficiently improve the mobility of SnO TFTs from 1.8 to 5.4 cm² V⁻¹ s⁻¹, whilst decreasing the V_DS from 4 to 0.2 V.\[80\] The passivated SnO channel showed outstanding electrical performance stability and negligible degradation after long-term storage for over 1 year. Enhanced performance of OFETs was also observed when inserting a thin ALD-Al₂O₃ interlayer between the organic dielectric and semiconductor layers.\[147\] Passivated OFETs with the ALD-Al₂O₃ dielectric interlayer (only 1 nm) showed a significantly reduced leakage current and elevated mobility of 0.65 cm² V⁻¹ s⁻¹, much higher than 0.08 cm² V⁻¹ s⁻¹ for the devices without an Al₂O₃ interlayer.

In short, ALD is a mature technique to grow Al₂O₃ films for electronic applications that can participate in the improvement of device performance. However, homogenous nucleation when processing 2D materials, which may limit its application in short-channel devices, is another factor that can be tuned to optimize both structural characteristics and electrical properties of the ALD-Al₂O₃ films.\[170\]

Recently, the incorporation of HfO₂ into 2D semiconductor devices has also emerged as a promising development for enhanced device performance. However, homogenous nucleation of ultrathin dielectric films remains a significant challenge during the ALD process. Price et al. demonstrated the deposition of a sub-5 nm uniform HfO₂ dielectric onto 2D MoS₂ and WS₂, using PEALD when fabricating top-gate FETs.\[191\] Compared with thermal ALD, PEALD can yield significantly improved nucleation on 2D crystals, resulting in a uniform and smooth HfO₂ thin-films. Plasma damage to the surface of TMCs remains an issue when processing 2D materials, which may limit its application for 2D TMCs approaching monolayer thickness.\[157\] Similar to the utilization of perylene tetracarboxylic acid (PTCA) for depositing uniform Al₂O₃ on graphene,\[192\] a monolayer (ML) molecular crystal of 3,4,9,10-perylene-tetracarboxylic dianhydride (PTCD) was used as a nucleation layer to deposit ultrathin HfO₂ dielectrics by ALD on 2D materials including graphene, MoS₂, and WS₂. (Figure 12a).\[170\] This method affords reduced density of trap states at the interface, suppressed leakage currents, and an improved breakdown field. AFM images (Figure 12b) and...
height profiles (Figure 12c) support the uniform deposition of both PTCDA ML film and the HfO₂ dielectric layer. Graphene-based FETs with the hybrid PTCDA/ALD-HfO₂ dielectric show a high mobility (~3500 cm² V⁻¹ s⁻¹), and outperform an intrinsic cutoff frequency (f_c) reaching 60 GHz (Figure 12d). Integration of ML-PTCDA/ALD-HfO₂ (3 nm) within monolayer TMC FETs (Figure 12e) brings excellent transfer characteristics (Figure 12f). Both MoS₂ and WSe₂ FETs respectively displayed I_{ON}/I_{OFF} ratios of 10⁷ and 10⁶, with SS values of 60 and 67 mV dec⁻¹.

Passivation of 2D TMC interfaces is another feature of ALD-HfO₂, which may be exploited for improving device performance. Passivation of 2D TMC interfaces is another feature of ALD-HfO₂, which may be exploited for improving device performance. For example, the hysteresis of HfSiO₂ transistors reduced significantly after passivation using ALD-HfO₂ and corresponded with enhancement to the source-drain current. FETs using a MoS₂ channel encapsulated by an ALD-HfO₂ layer can also display enhanced electrical performance compared with reference devices without encapsulation. Layer thickness of HfO₂ may also reduce charge impurity-induced scattering, in addition to screening from atmospheric interferences.

More practical electronic device application of ALD-HfO₂, was demonstrated by Marega et al. through designing floating-gate FETs (FGFETs) for logic-in-memory devices and circuits. The ALD-HfO₂ dielectric film can work as a blocking and tunnel oxide to efficiently modulate the electric field within the MoS₂ channel. Basic characterization of the devices is performed under a V_{DS} of 50 mV and a V_{G} ranging from −12.5 to 12.5 V, delivering a memory window of 10.6 V (Figure 13d). Moreover, the FGFETs are further designed and integrated into two-input and three-input logic circuits (Figure 13e). As a representative, a complete three-input NAND logic, is normally operated and its corresponding logic input and output curves are shown in Figure 13f. The stable operation of these reprogrammable logic-in-memory devices highlights the practical benefits of adopting ALD for optimizing FET performance in developing areas of the electronics industry.

2.2.3. Other Insulating Metal Oxides

Despite rapid advances in the commonly used Al₂O₃ and HfO₂, additional insulating MOs such as ZrO₂, BeO, La₂O₃, and Y₂O₃ have recently attracted attention in electronics owing to their high dielectric constants and large bandgap values. For example, Anderson et al. deposited a ZrO₂ gate dielectric on AlGaN/GaN MOSFETs by ALD, resulting in a much lower interface trap site at a density of 7.00 × 10¹² cm⁻² eV⁻¹ than that of the Schottky-gate reference device (2.03 × 10¹³ cm⁻² eV⁻¹). Moreover, the gate leakage current was reduced by up to four orders of magnitude. Chen and co-workers encapsulated organic
light-emitting diodes (OLEDs) with ZrO₂ by PEALD and molecular layer deposition (MLD), leading to the efficiently improved water barrier properties of up to $3.08 \times 10^{-5}$ g m⁻² day⁻¹. \cite{196}

In addition, multinary ALD-MO insulators such as titanium aluminum oxides (TiAlO)\cite{162} and magnesium calcium oxides (MgCaO)\cite{197} are also promising candidates as gate dielectrics or encapsulating materials.

The potential size reduction obtained from using thinner MO with high dielectric constants, such as ZrO₂ and Ta₂O₅, make ALD a promising technique for novel device manufacturing.\cite{198}

2.2.4. Metal Oxide Dielectric Heterostructures

Insulating single MO dielectrics have been successfully applied on various channel layers to improve the electrical performance of the final devices. However, it is still a challenge to deposit ultra-thin, continuous, and pinhole-free MO films on the surface of a channel layer due to nucleation site deficiency, especially on 2D channel materials.\cite{68,70} Therefore, several methods have been employed to promote surface nucleation and obtain high-quality dielectric layers. Examples include, pretreatment (activation) of
the substrate surface before the ALD reaction, using strong oxidants like O₃ or O₂ plasma during the ALD process, and adopting higher reaction temperatures. As discussed in previous sections (ALD-Al₂O₃ and ALD-HfO₂), the oxidation of channel materials is predominantly caused by high deposition temperatures and the use of strong oxidizing agents. This remains a consistent hindrance to the broad adoption of ALD in the fabrication of ultrathin MO dielectric films.

A successful strategy to suppress channel layer degradation during ALD and enhance dielectric properties is the incorporation of an intermediate layer to design MO dielectric heterostructures. Similar to the use of a PTCDA seeding layer as mentioned above, an ultrathin MO layer is preemptively deposited onto the channel as a seeding layer prior to MO ALD. For example, an Al₂O₃/ZrO₂ dielectric heterostructure was deposited onto MoS₂, yielding significant improvements to device performance. A 5 nm layer of Al₂O₃ was initially deposited onto the MoS₂ channel by ALD at 150 °C using TMA and H₂O as precursors. The corresponding second ZrO₂ dielectric (45 nm) was then deposited at an increased temperature (300 °C) onto the Al₂O₃ seeding layer. Compared with the MoS₂-TFTs using a single ZrO₂ dielectric layer, the TFTs decorated with the Al₂O₃/ZrO₂ heterostructure showed better electrical performance with improved mobility from 5.1 to 7.1 cm² V⁻¹ S⁻¹.

Besides deposition of high-quality dielectric films onto a channel layer, an intermediate/nucleation layer in heterostructured MO dielectrics can also protect channel materials during the ALD process, and prevent the creation of metal atomic vacancies or interstitial defects. For example, the formation of Zn vacancies during the ALD of a ZnO film onto a dielectric Ta₂O₅ layer leads to inferior properties of ZnO TFTs. To solve this problem, a thin ALD-Al₂O₃ layer has been adopted between the ZnO channel layer and the Ta₂O₅ dielectric layer to improve the electrical performance of ZnO-based TFTs. Compared with a single Ta₂O₅ dielectric, a series of Al₂O₃/Ta₂O₅ dielectric heterostructures grown by ALD show comparable dielectric constants but dramatically suppressed leakage currents. Further increasing the Al₂O₃ film thickness results in the gradual attenuation of leakage current density, which is beneficial for reducing off-currents and improving total device performance. These ALD-MO dielectrics also have good stability in capacitance at frequencies from 1 kHz to 1 MHz. As a result, the ZnO-TFTs with an optimized Al₂O₃/Ta₂O₅ dielectric layer show a greatly improved mobility (13.3 cm² V⁻¹ S⁻¹) than that of the single Ta₂O₅ dielectric layer (0.1 cm² V⁻¹ S⁻¹), as well as a suppressed SS value and an improved I_D ON/I_D OFF (Figure 14d).

Examples of advanced dielectric heterostructures using sputtering deposition (SD) of Ta₂O₅ onto an ALD-Al₂O₃ thin buffer layer have also been demonstrated. In contrast with the SD method, ALD techniques have several additional advantages for depositing MO dielectrics, including low growth temperatures, uniform film deposition, and controllable film thicknesses.
Moreover, transfer from ALD to SD chamber may introduce surface-adsorbed air contaminants, which may impact the subsequent purity of SD-deposited films and hence the electronic performance of TFTs. Liu et al. studied the electrical properties of different TiO$_2$/Al$_2$O$_3$ dielectrics which were prepared by SD and ALD, respectively.\[202\] Compared with MOSFETs with the SD-TiO$_2$/Al$_2$O$_3$ dielectric, the devices with the ALD-TiO$_2$/Al$_2$O$_3$ films exhibit a much lower leakage current density and better capacitance-voltage characteristics due to the better quality of thin-film MO dielectric heterostructures made by ALD.

Apart from utilizations in inorganic semiconductors-based FETs, MO dielectric heterostructures have also been widely used in OFETs for enhancing their electrical performance.\[181,200\] Composition and thickness are important parameters of MO dielectrics and strongly influence transistor performance.\[163,203,204\] Thus, MO heterostructures with suitable compositions and optimized thicknesses for TFTs remain a major research focus for ALD.

### 2.3. Metal Oxide Electrodes and Electrode Interlayers

In addition to its application as semiconductor channel materials and insulators, ALD-MOs have been adopted for use as transparent conductive oxide electrodes (TCO) and semiconducting electrode interlayers in transistors. For example, indium-tin-oxide (ITO), a well-known heteroatom doped SnO$_2$, is widely employed as a kind of TCO electrode.\[205\] Introduction of heteroatoms into oxides increases the carrier concentration, thus converting MO semiconductors to conductors. For pure SnO$_2$ made by ALD, it can be transformed from the semiconductor to conductor by adjusting ALD conditions (i.e., temperature) to alter carrier concentrations.\[92\] For instance, highly conductive SnO$_2$ serving as a transparent gate electrode has been fabricated by controlling the ALD reaction temperature.\[66\] The ALD-SnO$_2$ films deposited at 200 °C exhibit a large carrier concentration (>10$^{20}$ cm$^{-3}$), a low resistivity (∼0.0031 Ω cm), and a high transparency (∼93%) in most of the visible range (Figure 15a). ZnO-based TFTs with such an ALD-SnO$_2$ gate electrode (Figure 15b) exhibit excellent electrical performance with a high saturation mobility of 15.3 cm$^2$ V$^{-1}$ s$^{-1}$, a low SS of 130 mV dec$^{-1}$, a very high $I_{on}/I_{off}$ ratio of ∼10$^9$, and a low gate leakage current ($I_G$) of less than 10$^{-12}$ A (Figure 15c,d). The ALD-SnO$_2$ gated-TFTs outperform other devices based on oxides of conventional ITO ($\mu$ = 15 cm$^2$ V$^{-1}$ s$^{-1}$, SS = 160 mV dec$^{-1}$, and $I_{on}/I_{off}$=10$^8$) and ALD-AZO ($\mu$ = 11 cm$^2$ V$^{-1}$ s$^{-1}$, SS = 180 mV dec$^{-1}$, and $I_{on}/I_{off}$=10$^8$). Based on these findings, NMOS inverters were designed to further demonstrate the practical application of ALD-SnO$_2$ gate electrodes. The NMOS inverter with the ALD-SnO$_2$ gate (Figure 15e) displays static voltage-transfer curves (Figure 15f), highlighting its excellent room temperature performance under varying $V_{DD}$ values ranging from 2.5 to 25 V. Moreover, the maximum gain values of the inverter gradually increase from 20 to 382 upon raising $V_{DD}$ from 2.5 to 25 V (Figure 15g,h). Additionally, transition metal oxides (TMOs) such as VO$_x$,\[67\] and MoO$_x$,\[206\] possess suitable semiconducting properties and high stability, enabling them to serve as electrode interlayers for efficient charge injection in optoelectronic/electronic devices.\[207\] Large contact resistance at organic/metal interfaces seriously limits the carrier mobility and $I_{on}/I_{off}$ of OFETs.\[208\] Reduction of interfacial contact resistance has been demonstrated using an ultrathin ALD-VO$_x$ film at the electrode/semiconductor interface in OFETs. It functions as a hole injection layer, promoting electrode work function tunability and charge transport.\[67\] The VO$_x$ interlayer with controlled thicknesses was deposited by ALD with tetrakis(dimethylamino) vanadium [V(dma)$_4$] and H$_2$O at a low
temperature (50 °C). After 20 ALD cycles, the resulting OFETs exhibited remarkably improved electrical performance with a reduced contact resistance from 71 to 10 kΩ cm and enhanced mobility from 1.09 to 1.56 cm² V⁻¹ s⁻¹. The ALD-VOₓ interlayer also performed well as a barrier material against moisture/oxygen transmission in OFETs, delivering a good retention (over 83% after 30 days) in the mobility for devices with a combined ALD-Al₂O₃ layer for encapsulation.

3. ALD of Metal Chalcogenides for FETs

Interest in applications of MCs and particularly TMCs within next-generation electronics has risen steeply over the past decade, driven by their intrinsic layered crystal structures and unique properties. TMCs typically consist of a metal/chalcogen atomic ratio of 1:2, although exceptions of 1:1, 2:3 and 3:1 are possible. TMCs have three classical polymorphs, which are tetragonal (1T), hexagonal symmetry (2H), and rhombohedral (3R). Their electrical properties strongly depend on the polymorph and structural phase transition, where the TMCs with 1T and 2H phases show metallic and semiconducting behaviors, respectively. For further details on TMCs, their chemical compositions, electronic structures, and applications have been described in a comprehensive review by Chhowalla and co-workers.

Versatile processing methods such as exfoliation, CVD, and magnetron sputtering have been reported for the synthesis of TMCs for applications in electronics. However, intrinsic factors arising from these methods often limit the fabrication of TMC films in a uniform, repeatable, scalable, and tunable manner. Precise film thickness is of particular importance to TMCs for applications in electronics. However, intrinsic limitations arising from these methods often limit the fabrication of TMC films in a uniform, repeatable, scalable, and tunable manner. Precise film thickness is of particular importance to TMCs due to their layer-dependent bandgap characteristics. Bandgap magnitude and crystal structures are influenced by the thickness of TMCs, resulting in a transition from an indirect to direct bandgap material, in the bilayer to a monolayer transition.

The tunability of ALD has established it as an ideal candidate for the fabrication of high-quality MCs as channel materials, particularly with regard to thickness control at the nanoscale. Channel length (L) is affected by the thickness of both channel and dielectric layers according to the following Equation (4),

\[ L = \sqrt{\frac{\varepsilon_{ch}}{N_{ox}} d_{ch} d_{ox}} \]  

where \( N \) is the number of gates, and the \( \varepsilon_{ch} \) (\( d_{ch} \)) and \( \varepsilon_{ox} \) (\( d_{ox} \)) are the dielectric constants (thickness) of the channel and the oxide, respectively. Thus, ALD is an efficient technique to minimize the size of electronic devices by using ultrathin channel materials, such as few- or mono-layer (<1 nm) TMCs.

This section will discuss MCs and their heterostructures fabricated using ALD for applications in transistors, with an emphasis on film structural characteristics and device performances. Representative examples of various MCs synthesized by ALD and their related electrical properties as well as device performance are presented in Table 4.

3.1. Molybdenum Dichalcogenides

Molybdenum disulfide (MoS₂), which occurs naturally as a mineral (molybdenite), has attracted great attention in high-performance FETs due to its tunable intrinsic bandgap (1.2–1.9 eV) and high carrier mobility (up to 500 cm² V⁻¹ s⁻¹). The first publication of single-layer MoS₂, used within transistors reported excellent semiconductor properties with a mobility of 200 cm² V⁻¹ s⁻¹ and an \( I_{ON}/I_{OFF} \) of 10⁸ at room temperature. Subsequent demonstrations of mono-to-few layer MoS₂ transistors further supported the initial findings.

Numerous MoS₂ precursor combinations have been used in the ALD of TMCs such as MoCl₅ and H₂S, Mo(CO)₆ and H₂S, and CH₄, S₂CH₂, Mo(NMe₂)₄, and H₂S as well as Mo(NMe₂)₂(NtBu)₂ and H₂S. Benefiting from the layer-controllability and reproducibility, ALD-MoS₂ shows great potential for applications in FETs. For example, MoS₂ channel fabricated by ALD from MoCl₅ displays an effective mobility of 1.0 cm² V⁻¹ s⁻¹ in back-gate FETs with a 20 μm channel. However, temperature requirements of the MoCl₅-based process are beyond the upper limit tolerated by organic polymer substrates and photoresists. Additionally, the generation of chlorine-containing by-products such as HCl results in etching damage to both substrates and deposited films.

Metal amides show promise as metal precursors for low-temperature ALD due to their high reactivity and generation of volatile byproducts. By adopting Mo(NMe₂)₂ as a metal precursor and H₂S as a co-reactant, ALD-MoS₂ films were deposited at a record low reaction temperature of 60 °C. Low ALD temperatures enable simple device fabrication using lithographic lift-off patterning. After a silicon nitride-coated silicon wafer is covered by a patterned resist using a maskless lithography protocol, the MoS₂ film of the desired thickness is then deposited by ALD at 80 °C. Removal of the resist using n-methyl-2-pyrrolidone (NMP) at 75 °C yields uniform arrays of patterned MoS₂ (Figure 16b–d). Finally, post-deposition sulfurization is performed under an atmosphere of sulfur vapor for 5 h, yielding highly crystalline MoS₂. The electrical characteristics of the MoS₂ semiconductor are further evaluated as FET components, delivering a mobility of 0.23 cm² V⁻¹ s⁻¹ and an \( I_{ON}/I_{OFF} \) of \( \times 10^2 \). However, the low temperature used to deposit MoS₂ results in amorphous films with numerous defects, leading to poor FET performance observed in the large off-state current and low mobility. Improved crystallinity and better electrical performance of TMC films may be achieved using post-deposition sulfurization of the film at high temperatures. The standard sulfur sources such as sulfur powder and H₂S may also be replaced by carbon disulfide (CS₂), a strong sulfurizing reagent with low toxicity and cost. Moreover, the relatively low sulfurization temperature used for CS₂ may be more compatible with electronic devices, especially for flexible transistors. Compared with as-deposited ALD-MoS₂, improved electrical performance was demonstrated by sulfurization using CS₂ to obtain \( \approx 100 \) times higher \( I_{ON}/I_{OFF} \) (5 \( \times 10^4 \)) and 36 times higher mobility (0.36 cm² V⁻¹ s⁻¹).

Sulfurizing MoO₃ films pre-deposited by ALD is another possible technique to synthesize high-quality MoS₂ films with controlled thicknesses. Sulfurization of the ALD-MoO₃ film at 500 °C followed by annealing at 900 °C with sulfur powder yields a MoS₂ film (Figure 17a,b). The layer thickness of MoS₂ may also be precisely adjusted from monolayer to four layers (Figure 17c). When used to prepare a top-gate FET (Figure 17d), the...
monolayer MoS₂ film shows a typical n-type FET behavior with a mobility of 0.76 cm² V⁻¹ s⁻¹ and an $I_{ON}/I_{OFF}$ of 10⁶ (Figure 17e). By contrast, the electron mobility of the tetra-layer-MoS₂ (5.9 cm² V⁻¹ s⁻¹) is more than 8 times higher than that of the monolayer MoS₂ (Figure 17f). Similar trends are observed for CVD-MoS₂ with mobility values increasing from 3.6 to 15.6 cm² V⁻¹ s⁻¹ in the monolayer and trilayer, respectively.[256] The improved performance of MoS₂ may be due to the enhanced screening effect induced by an increase in layer numbers of MoS₂.[253] Generally, monolayer MoS₂ suffers from fluctuating potential, which is caused by the formation of traps at the interface between the dielectric layer and the semiconductor channel.[252] The additional layers of TMCs can efficiently suppress the negative effects of potential fluctuation, thus resulting in a higher carrier mobility.

Although previous reports have presented deposition of TMCs on various substrate materials, it remains challenging to synthesize wafer-scale, uniform 2D TMCs in a scalable manner via direct ALD routes.[250,251] This obstacle hinders the integration of 2D TMCs for practical applications in the semiconductor industry. Thus, advances in ALD protocols to produce large-scale, homogeneous 2D TMC thin films are necessary. Consequently, Leon et al. have synthesized homogeneous few layers of MoS₂ on a 6-inch wafer by ALD with the utilization of diethylsulfide (DES) as an inhibitor layer.[209] The deposited MoS₂ films exhibited a significant increase in grain size and surface coverage (>620%), as well as excellent room temperature mobility (13.9 cm² V⁻¹ s⁻¹) and $I_{ON}/I_{OFF}$ of 10⁶.

Conformal surface coating of TMC films onto nonplanar, large surface-to-volume ratio substrates has been extensively demonstrated using ALD, highlighting the benefits to flexible electronic applications.[224,227,233] Deposition of an ultrathin MoS₂ layer onto a SiO₂ nanowire via ALD (Figure 18a) affords a core-shell nanowire FET architecture (Figure 18b) with an omega (Ω)-shaped top gate.[224] Cross-sectional TEM images of the deposited nonplanar MoS₂ (Figure 18c) highlight the formation of uniform and high-crystalline MoS₂ layers. The fabricated Ω-shaped MoS₂ FETs exhibit a mobility of 0.02 cm² V⁻¹ s⁻¹ and an $I_{ON}/I_{OFF}$ of 10⁶ (Figure 18d), which are comparable to those of the planar MoS₂ FETs with a mobility of 0.01 cm² V⁻¹ s⁻¹ and an $I_{ON}/I_{OFF}$ of 3.5 × 10⁶ (Figure 18e).

In comparison with MoS₂, molybdenum selenide (MoSe₂) displays a similar high average room temperature mobility (>50 cm² V⁻¹ s⁻¹) and a high $I_{ON}/I_{OFF}$ ratio (10⁶) in addition to bandgaps ranging from 1.1 to 1.6 eV.[254] MoSe₂ materials are typically prepared by exfoliation and CVD.[234,235] However, ALD techniques may also deposit MoSe₂ using Mo(CO)₆ or MoCl₅ and ((CH₃)₃Si)₂Se as molybdenum and selenium precursors, respectively.[256] Selenization of ALD-MoO₃ also achieves
high-quality MoSe$_2$ films with the desired thickness.$^{[257,258]}$ Similarities between silicon and MoSe$_2$, including bandgap size and electronic properties, make the latter an excellent candidate for application as a semiconductor channel material.

Molybdenum ditelluride (MoTe$_2$) possesses a smaller bandgap (1.1 eV for monolayer and 0.88 eV for multi-layers) than its lighter chalcogenide analogs, but exhibits unique ambipolar-type FET properties.$^{[259–261]}$ Fabrication of MoTe$_2$ films may be accomplished through direct ALD methods,$^{[262]}$ or post-deposition tellurization of ALD-MoO$_3$ films.$^{[263]}$

3.2. Tungsten Dichalcogenides

Tungsten disulfide (WS$_2$), another representative of TMCs, exhibits an indirect bandgap of 1.4 eV (bulk) and a direct bandgap of 2.1 eV (monolayer).$^{[266]}$ It shows great potential in FET applications due to its high theoretical mobility.$^{[264]}$ WS$_2$-based FETs have been predicted with the highest mobility of over 1100 cm$^2$ V$^{-1}$ s$^{-1}$ in a monolayer at room temperature.$^{[265]}$ Up to now, WS$_2$ has been successfully prepared by ALD with WF$_6$ and H$_2$S,$^{[266–268]}$ tungsten chlorides (WCl$_4$ and WCl$_6$) and H$_2$S,$^{[226,269]}$ W(CO)$_6$ and H$_2$S,$^{[270]}$ W(NMe$_2$)$_2$(NtBu)$_2$ (BTBMW) and H$_2$S,$^{[59]}$ as well as sulfurizing thickness-controlled ALD-WO$_3$ films.$^{[228,229]}$

Earlier reports have demonstrated that ALD-WS$_2$ can exhibit both n-type and p-type semiconducting characteristics.$^{[227,228]}$ For example, atomically thin WS$_2$ films prepared by sulfurizing ALD-WO$_3$ operate as n-type semiconductors with an electron mobility of 4.5 cm$^2$ V$^{-1}$ s$^{-1}$ and an $I_{ON}/I_{OFF}$ of $\approx 10^5$.$^{[229]}$ The thickness of ALD-WO$_3$ precisely controls the layer number of WS$_2$ from monolayer to tetra-layer (Figure 19a).$^{[228]}$ The WS$_2$-based top-gate FET displays impressive transfer and output characteristics with a high electron mobility of 3.9 cm$^2$ V$^{-1}$ s$^{-1}$ and a low SS of 0.6 V dec$^{-1}$ (Figure 19b,c). In general, the impurity content as well as structural defects of deposited films significantly affects the electrical properties and even alter the semiconducting behaviors of
2D materials.\textsuperscript{[209]} For instance, PEALD-WS\textsubscript{2} with a large crystal grain size operates as a p-type semiconductor with an $I_{\text{ON}}/I_{\text{OFF}}$ of $\approx 10^5$ (Figure 19d).\textsuperscript{[227]} It is speculated that p-type behaviors of ALD-WS\textsubscript{2} FETs may arise from S deficiency in the WS\textsubscript{2} films.

Currently, research into tungsten selenide (WSe\textsubscript{2}) for electronic applications is limited, although exfoliated single-crystal WSe\textsubscript{2}-based FETs have been demonstrated to exhibit a high hole mobility of 350 cm\textsuperscript{2} V\textsuperscript{-1} s\textsuperscript{-1} at 300 K and a high $I_{\text{ON}}/I_{\text{OFF}}$ of $10^6$.\textsuperscript{[271]} Park et al. prepared WSe\textsubscript{2} by self-limited layer synthesis (SLS) using WCl\textsubscript{6} and diethyl selenide at a high temperature above 600 °C.\textsuperscript{[231]} Unlike conventional ALD processes, the layer number of target films prepared by this SLS process mainly depends on the reaction temperature rather than the SLS cycles. Control of the SLS temperature from 600 to 800 °C affords WSe\textsubscript{2} films with a tunable layer number, from five-layers to a monolayer (Figure 19e). Back-gated FETs were used to evaluate a trilayer-WSe\textsubscript{2} film, exhibiting a hole mobility of 2.2 cm\textsuperscript{2} V\textsuperscript{-1} s\textsuperscript{-1} and an $I_{\text{ON}}/I_{\text{OFF}}$ of $\approx 10^6$ (Figure 19f).

The ambipolar characteristics of ALD-WSe\textsubscript{2} were further demonstrated on large area (5 × 5 cm\textsuperscript{2}) silicon wafers in back-gated FETs.\textsuperscript{[230]} High mobility for both n-type (531 cm\textsuperscript{2} V\textsuperscript{-1} s\textsuperscript{-1}) and p-type (354 cm\textsuperscript{2} V\textsuperscript{-1} s\textsuperscript{-1}) carriers were recorded with high $I_{\text{ON}}/I_{\text{OFF}}$ ratios ($\approx 10^6$).

### 3.3. Tin Chalcogenides

Tin disulfide (SnS\textsubscript{2}) is an intrinsic n-type semiconductor with a bandgap of 2.1 eV, larger than that of monolayer MoS\textsubscript{2}.\textsuperscript{[272]} The high bandgap suppresses source/drain tunneling in FETs, affording a high $I_{\text{ON}}/I_{\text{OFF}}$ of $10^8$.\textsuperscript{[273]} Furthermore, large electron mobility (230 cm\textsuperscript{2} V\textsuperscript{-1} s\textsuperscript{-1}) was demonstrated using adsorbate-suppressing conditions, indicating its potential for applications in FETs.\textsuperscript{[274]} The fabrication of SnS\textsubscript{2} films by ALD has been demonstrated using TDMASn and H\textsubscript{2}S,\textsuperscript{[222,234,275]} bis(1-dimethylamino-2-methyl-2-propoxy) tin(II) and H\textsubscript{2}S plasma,\textsuperscript{[274]} Sn(OAc)\textsubscript{4} and H\textsubscript{2}S,\textsuperscript{[276]} as well as sulfurizing ALD-SnO\textsubscript{x}.\textsuperscript{[233]} Phase engineering of precursor thin films via sulfurization methods has shown promising results. Back-gated FET channels prepared via deposition of an ALD-SnS film followed by a sulfurization step, performed as an n-type semiconductor with small mobility (0.014 cm\textsuperscript{2} V\textsuperscript{-1} s\textsuperscript{-1}).\textsuperscript{[233]} Such poor electrical properties of SnS\textsubscript{2} can be improved by enhancing its crystallinity and control crystal orientation,\textsuperscript{[273]} as well as optimizing the gate structures.\textsuperscript{[277]}

ALD-SnO as a precursor for SnS\textsubscript{2} was demonstrated using a two-step sulfurization process, consisting of an initial thermal post-deposition sulfurization (350 °C), and then an H\textsubscript{2}S plasma treatment (Figure 20a).\textsuperscript{[233]} The SnS\textsubscript{2} film with subsequent H\textsubscript{2}S plasma treatment shows better-suited crystal orientation and improved crystallinity than that with simple sulfurization (Figure 20b). Back-gate TFTs fabricated using these SnS\textsubscript{2} films show typical n-type behaviors (Figure 20c,d), where the $I_{\text{ON}}/I_{\text{OFF}}$ is greatly increased to $10^6$ for the TFTs with two-step sulfurized SnS\textsubscript{2}, compared with $10^3$ for that with one-step sulfurized SnS\textsubscript{2}. Similarly, the field-effect mobility is also dramatically improved from $2 \times 10^{-4}$ to 0.02 cm\textsuperscript{2} V\textsuperscript{-1} s\textsuperscript{-1}.

A two-step ALD process was demonstrated for obtaining crystalline and continuous SnS\textsubscript{2} films at a low temperature.\textsuperscript{[276]} An amorphous SnS\textsubscript{2} thin layer deposited at 150 °C was sulfurized...
at a relatively high temperature (250 °C), then the formed crystalline SnS$_2$ acted as a seed layer for promoting the growth of crystalline SnS$_2$ films by low-temperature ALD (150 °C). Another two-step ALD procedure demonstrated by Pyeon et al., applies low temperature (150 °C) deposition of monolayer amorphous SnS$_2$ followed by a subsequent SnS$_2$ thin channel layer (240 °C) (Figure 20e).[74] The amorphous monolayer selectively promotes basal growth of SnS$_2$ (001) during the second deposition, thus suppressing non-uniform nuclei orientation. The relationship between surface energy and grain orientation was not explored but may offer an avenue for further research. Analysis of the electrical performance as a bottom-gate TFT revealed that the as-deposited SnS$_2$ film mobility could be improved using an additional sulfurization step (300 °C), from 0.2 to 0.8 cm$^2$ V$^{-1}$ s$^{-1}$. The excellent control of grain orientation made this procedure well suited for fabricating non-planar (Figure 20f) and flexible SnS$_2$ TFTs (Figure 20h). Thus, direct deposition onto non-planar substrates was undertaken to investigate the practical application of this method. Cross-sectional TEM images (Figure 20g) of a diagonally constructed TFT highlight the excellent conformality and basal growth of the 2D SnS$_2$ channel layer. The mobility and $I_{ON}/I_{OFF}$ display moderate outputs of 0.4 cm$^2$ V$^{-1}$ s$^{-1}$ and $\approx 10^6$ for the non-planar ALD-SnS$_2$ TFTs after post-annealing, respectively. The flexible ALD-SnS$_2$ TFTs exhibit stable electric performance with a mobility of 0.57 ± 0.02 cm$^2$ V$^{-1}$ s$^{-1}$ and an $I_{ON}/I_{OFF}$ of $10^6$ (Figure 20i). After 2000 bending cycles at a radius of 17.5 mm, the flexible TFTs show slight performance degradation (Figure 20j). These results highlight the practicality of ALD for the preparation of flexible and nonplanar MC devices.

In contrast to SnS$_2$, tin monosulfide (SnS) is intrinsically p-type, with a small indirect bandgap (1.0 eV).[122,235] ALD synthesis affords p-type SnS films with a hole mobility of 0.21 cm$^2$ V$^{-1}$ s$^{-1}$ but a relatively small $I_{ON}/I_{OFF}$ of $8.8^{[234]}$. Generally, SnS films with high-crystal orientation can be synthesized at a relatively low ALD temperature,[235] which is beneficial for the fabrication of electronic devices.[73,122] For instance, the Hall mobility of SnS-based FETs was improved from 0.82 to 15.3 cm$^2$ V$^{-1}$ s$^{-1}$ by tuning ALD reaction temperatures.[235] The significant improvement in carrier transport is ultimately attributed to the preferred crystal orientation of the ALD-SnS film.

The purity of channel materials is also an essential parameter that cannot be ignored in evaluating the influence on electrical
In some cases, multiple phases of SnS may be present, including mixtures of SnS, SnS$_2$, and Sn$_2$S$_3$, which may seriously limit electrical properties. However, conversion of the as-deposited SnS mixtures to a single-phase SnS film may be achieved via post-deposition annealing under H$_2$ (360 °C), contributing to a greatly improved Hall mobility of 15.66 cm$^2$ V$^{-1}$ s$^{-1}$ compared with the as-deposited SnS$_x$ film of 2.83 cm$^2$ V$^{-1}$ s$^{-1}$.

An analogous two-step strategy has also been applied for the ALD of SnS semiconductors. A continuous amorphous ALD-SnS film was previously deposited at lower temperatures (90 °C), followed by a high-temperature deposition of a crystalline SnS at 240 °C. The SnS TFTs exhibit p-type behaviors with a mobility of 0.18 cm$^2$ V$^{-1}$ s$^{-1}$ and an $I_{ON}/I_{OFF}$ ratio of 80 (Figure 1a). Correspondingly, the ALD-SnS gas sensors also display high sensitivity for NH$_3$ detection (Figure 21b). The facile transformation of ALD-SnS$_2$ to SnS with the assistance of Sn(dmamp)$_2$ vapors is also feasible (Figure 21c). Sn(dmamp)$_2$ molecules adsorb onto the SnS$_2$ surface, triggering a reduction of the Sn(IV) forming SnS and volatile byproducts. The opposing behaviors of bottom-gate TFTs using SnS$_2$ and SnS in response to NO$_2$ gas sensing (Figure 21d) support the majority carrier species of the two phases are electrons and holes, respectively.

In addition to SnS$_2$ and SnS, tin selenide (SnSe) shows promise as a low bandgap (0.9 eV for indirect and 1.3 eV for direct) layered nanomaterial for electronic applications. Semiconducting ALD-SnSe films can exhibit good p-type
behavior with a high hole mobility of $10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and an $I_{ON}/I_{OFF}$ of $\approx 10^5$.

3.4. Other Metal Chalcogenides

Aside from Mo, W, and Sn-based MCs, the fabrication of alternative MC materials such as lead sulfide (PbS), manganese sulfide (MnS), and rhenium disulfide (ReS$_2$) is possible using ALD,[210,281,282] with their development for electronic applications attracting growing interest.[238,283] MnS, is a p-type semiconductor with a wide bandgap of 3.7 eV, and it has been deposited with crystal phase-control by ALD using bis(ethylcyclopentadienyl)Mn(II) (Mn(EtCp)$_2$) and H$_2$S precursors.[283] The remarkable properties include an $I_{ON}/I_{OFF}$ of $>10^6$ and a field-effect hole mobility of 0.1 cm$^2$ V$^{-1}$ s$^{-1}$, when applying $\alpha$-MnS in a top-gate FET.[283] Moreover, the MnS FETs without dielectric encapsulation show negligible degeneration of device performance after being exposed to air for 30 days, indicating their excellent air stability. Similarly, ReS$_2$ films can be synthesized on large-area substrates by ALD using ReCl$_5$ and H$_2$S precursors at a wide deposition temperature range between 120 and 500 °C.[282] Their use as channel materials in FETs has displayed attractive electrical performances (i.e., an $I_{ON}/I_{OFF}$ of $10^6$ and a SS of 750 mV dec$^{-1}$).[284]

Very recently, uniform and crystalline PbS thin-films have been produced by low-temperature ALD using rac-N$_2$N$_3$-di-tert-butylbutane-2,3-diamide lead [Pb(dbda)] and bis(trimethylsilyl)-
amide lead \([\text{Pb(btsa)}_2]\) as lead precursors, with \(\text{H}_2\text{S}\) as a sulfur source.\(^{[210]}\) The PbS films exhibited typical p-type behaviors with excellent mobility up to 70 cm\(^2\) V\(^{-1}\) s\(^{-1}\). Lead chalcogenides are a well-established class of ambipolar semiconductors, with carrier transport determined by an excess of either metal or chalcogen within the crystal structure. Thus, chalcogen- and lead-rich materials possess p- and n-type characteristics, respectively.\(^{[238]}\) Post-synthesis colloidal ALD (PS-cALD) applies spin-casting (or other solution-processing techniques) to generate nanocrystals (NCs) with precise size control, followed by NC surface modifications using an adapted ALD protocol. Selective stoichiometric enhancement of the NC thin film using ALD (Figure 22a) was achieved through subsequent modification of the NC surface using chalcogen- or lead-based salts dissolved into an organic solvent (65 °C).\(^{[238]}\) The electrical properties of the stoichiometry-controlled lead chalcogenides were evaluated in a bottom-gate FET (Figure 22b). The transfer curves of PbSe after post-treatment with PbCl\(_2\) reveal the influence of increasing Pb-surface stoichiometry on carrier transport as a function of time (Figure 22c). The initial PbSe NC FETs treated with Na\(_2\)Se exhibit p-type characteristics with a mobility of 7.5 \(\times\) 10\(^{-3}\) cm\(^2\) V\(^{-1}\) s\(^{-1}\), which is decreased to 2.2 \(\times\) 10\(^{-3}\) cm\(^2\) V\(^{-1}\) s\(^{-1}\) after 1 h PbCl\(_2\) treatment. By extending the treatment time to 6 h, an ambipolar behavior appears in the FETs. After 12 h, n-type NC FETs can be achieved with electron mobility as high as 4.5 cm\(^2\) V\(^{-1}\) s\(^{-1}\) and an \(I_\text{ON}/I_\text{OFF}\) of \(\approx 10^2\). This transformation is also reflected in the output curves, as after 1 h PbCl\(_2\) post-treatment, clear p-type characteristics are observed (Figure 22d), whilst at 12 h n-type characteristics are dominant (Figure 22e).

3.5.2 2D Heterostructures Based on MCs

In addition to single MC semiconductors, MCs-based 2D heterostructures such as MoS\(_2\)/graphene,\(^{[222]}\) MoS\(_2\)/WSe\(_2\),\(^{[225]}\) and MoS\(_2\)/WS\(_2\),\(^{[285]}\) may be constructed by stacking different 2D materials together.\(^{[213]}\) These heterostructures have been extensively studied in various applications including vertical tunneling FETs,\(^{[286]}\) photodetectors,\(^{[222]}\) and inverters.\(^{[223]}\) The low contact resistance within MC/graphene heterostructures affords improved performance in electronic devices,\(^{[222]}\) whilst TMC/TMC heterostructures can function as current rectifiers due to the formation of p-n junctions.\(^{[226,287]}\)

The deposition of single-layer MoS\(_2\) directly onto graphene via ALD, combines properties of both materials in MoS\(_2\)/graphene heterostructures to achieve a FET-based photodetector.\(^{[222]}\) An \(I_\text{DS}-V_\text{DS}\) curve evaluates the fluctuation of potential in response to light (Figure 23a), with a 116 nA photocurrent difference.
Figure 22. a) Schematic of PS-cALD for preparing lead chalcogenide NC films and their corresponding TEM images. The left is an as-synthesized NC thin-film, the middle is a thin-film treated with either Na$_2$Se, Na$_2$S or KHS solution, the right is a thin-film with further treatment in PbCl$_2$ solution. b) A schematic FET based on the channel of PbS or PbSe thin-films. c) Transfer curves of Na$_2$Se-treated PbSe NCs without (black) and with 1 h (blue), 6 h (green), and 12 h (red) of PbCl$_2$ treatment at 65 °C. d,e) Output curves of Na$_2$Se-treated PbSe with followed by further PbCl$_2$ treatment for 1 h (d) and 12 h (e), respectively. Reproduced with permission.[238] Copyright 2014, American Chemical Society.

Figure 23. a) $I_{DS}$-$V_{DS}$ curves and b) dynamic photoresponse of the ALD-MoS$_2$/graphene heterostructure-based FETs. Reproduced with permission.[222] Copyright 2019, Elsevier. c) Schematic device and optical image of the MoS$_2$/WSe$_2$ FET-based PN diode, and d) the corresponding $I$-$V$ curves with various gate biases. Reproduced with permission.[225] Copyright 2016, Nature Publishing group.
observed at a \( V_{BG} \) of 0.1 V and a responsivity of 241 mA W\(^{-1}\). The on/off switching behavior (Figure 23b) further demonstrates its optoelectronic applications, highlighting the potential of ALD-derived 2D heterostructures.

Precursor selection is an important factor when fabricating 2D MC heterostructures using ALD, as by-products such as HCl may result in surface etching. Thus, metal halide precursors using chloride ligands are typically avoided when used in conjunction with sensitive substrates, as is the case of MoS\(_2\)/WSe\(_2\) heterostructures. The MoS\(_2\)/WSe\(_2\) heterostructures have also been fabricated using the SLS process at 800 °C, where MoS\(_2\) was deposited onto exfoliated WSe\(_2\) flakes.\[^{225}\] As a result, a top-gated FET device (Figure 23c) performs as a typical p-n diode, showing rectifying characteristics with a forward/reverse current ratio of \( \approx 80 \) at a \( V_G \) of \(-60\) V (Figure 23d). Similarly, a p-n diode based on InSe/Sb\(_2\)Se\(_3\) heterostructure was also fabricated by stacking a p-type Sb\(_2\)Se\(_3\) layer on n-type InSe, which were both deposited by ALD.\[^{287}\] The resulting heterostructure exhibited typical diode characteristics with a maximum leakage current of \(10^{-7}\) A at \(-1\) V bias.

The ALD of WS\(_2\)/SnS heterostructures ensues to give an ambipolar thin film with electron mobility of 48 cm\(^2\) V\(^{-1}\) s\(^{-1}\) for n-type FETs and a hole mobility of 20 cm\(^2\) V\(^{-1}\) s\(^{-1}\) for p-type FETs at room temperature.\[^{226}\] However, the hole mobility of SnS in the heterostructure dropped significantly compared with that of the pure SnS (\(\approx 818\) cm\(^2\) V\(^{-1}\) s\(^{-1}\)). This result is attributed to hole transport resistance, which may be caused by the misalignment of the SnS and WS\(_2\) layers. The difference between crystal structures led to the growth of the SnS layer on WS\(_2\) at an orientation of \(\approx 15^\circ\), resulting in a remarkable drop in the hole mobility of SnS. Thus, misalignment between different TMCs remains a continuing challenge for the fabrication of ALD heterostructures.

Although ALD is well-suited to depositing MCs, there are still limited studies about the electrical applications of ALD-MCs. Moreover, reports on constructing 2D MC heterostructures by ALD in electronics are also limited.\[^{222,226,287}\] Considering the attractive features of nanoscale MCs, 2D ALD-MCs and their related heterostructures will play an important role in the development of next-generation electronic devices. Additionally, multifunctional MCs with tunable properties and improved performance are also worthy of in-depth studies. For example, Mo\(_0\),W\(_1\),S\(_2\) exhibits a tunable optical bandgap from 1.87 to 2.00 eV, and displays an improved photocurrent relative to MoS\(_2\) and WS\(_2\), respectively.\[^{288}\] Continued research should focus on the broad applications and possibilities provided by ALD-MCs and their derived architectures for advanced electronics and optoelectronics.

### 4. Conclusions and Perspective

In summary, this review has outlined recent advances in the fabrication of FET materials using ALD, as well as assessed their corresponding performances as integrated devices. The well-established merits of ALD yielded FET materials with atomically precise layer thickness, whilst maintaining conformality to numerous substrate/device architectures. The large variety of key FET materials fabricated using ALD includes semiconductor channels, dielectrics, passivation/encapsulation layers, electrodes, and electrode interlayers, highlighting the benefits of ALD for FET manufacturing. The continuously expanding library of ALD precursors has enabled numerous MOs and MCs to be deposited as ultrathin films, whilst additional ALD factors facilitate control over stoichiometry, structure and bandgap properties. These factors, in conjunction with electronic performance metrics such as the charge carrier mobility, on/off current ratio, switching speed and device stability, enable the rapid and successive optimization of new materials for applications in FETs and their derived devices. Several wide/medium bandgap n- and p-type MO have been fabricated as channel materials as well as transparent electrodes and electrode interlayers, resulting in improved charge transport and signal switching. Large bandgap MOs have also served as effective gate dielectrics or protecting/encapsulating layers for enhancing device performance, particularly the durability and operational stability. The rapid development of 2D materials and devices has also triggered investigation on the design of ALD-MCs as promising channel materials for n-type and p-type transistors. These narrow/medium-bandgap semiconductors are used as single channel layers as well as heterostructures for promoting charge transport, photodetection, gas sensing, and more.

Despite significant progress, ALD application still requires the development of cost-effective precursors and methods, to further promote the integration of FET materials in high-performance devices. Previous reports have focused on n-type MO and MC semiconductors due to the absence of p-type and bipolar counterparts. Impressively, reports of some p-type semiconductors derived from ALD, including SnO, CuO, Cu\(_2\)O, WS\(_2\), and WSe\(_2\), SnS and SnSe, as well as InSe, highlight the growing progress of p-type ALD materials. Examples such as ZnO, TiO\(_2\), and lead chalcogenides may also display a transition to p-type characteristics through appropriate doping with heteroatoms, substrate selection, and enrichment with metal elements. However, further research on p-type materials using ALD is required for a more detailed evaluation of their electric, optoelectronic and mechanical properties, as well as their device stability (e.g., operational stability, air stability, photostability, bending stability, and so forth).

The capacity for ALD to tune the composition of MOs and MCs makes it well adapted to explore multinary FET materials. By controlling ALD reaction parameters (e.g., temperature, time, precursor, substrate, and pre-/post-treatment, etc.), thin-film fabrication according to a desired stoichiometric composition affords facile optimization possibilities for the bandgap, mobility, and other physical/chemical properties. Moreover, ALD has the potential to fabricate more complex heterostructures in a manner that is not accessible with other techniques, but currently remains underexplored. For example, simple alternating bilayers of MO insulators have proven an effective adaptation for shielding devices against atmospheric water and oxygen surface adsorption. Design of such heterostructure using ALD is a promising strategy for boosting the electrical performance of FET devices using MO/MO, MC/MC, and hybrid MO/MC architectures. In addition, the uniqueness of ALD may also provoke greater integration of ALD techniques with other established methods (i.e., 3D printing, inject printing, flexographic printing, solution-process patterning, and laser processing, etc.) towards advanced FET design and fabrication, which may prove useful for developing future micro-/nano-scale structures and devices.

The successful demonstration of ALD of MOs and MCs in high-performance FETs reflects their promising potential as...
future components within electronic devices such as inverters, oscillators, and integrated circuits. In addition, other ALD-derived materials, such as III-V group semiconductors, metal nitrides, metal halides, perovskites, and hybrids, also show significant potential in advanced electronics and semiconductor-integrated systems. However, current researches on most ALD-materials still mainly focus on individual FET fabrication and is limited to laboratory-scale. Meanwhile, translation of the ALD processes to device arrays based on FETs is an important step for developing the technology for larger-scale manufacturing. This demand may stimulate the adoption of ALD-FETs within newly emerging technologies such as multifunctional sensing, artificial synapses, self-driving systems, smart manufacturing as well as an intelligent medical diagnosis and health monitoring. The emerging ALD processes of MOs and MCs with tunable compositions, structures, and electronic properties can provide the possibility to optimize optoelectronic and mechanical properties and promote widespread applications within electronics, photonics, information, and Internet of Things. Nowadays, the ever-developing uses of artificial intelligence (AI) are accelerating the discovery and deployment of advanced materials as well as functional devices.[289] Thus AI techniques such as machine learning and deep learning may be used to further develop ALD-derived materials and FETs/chips for flexible circuits, actuators, intelligent robotics, integrated networks of quantum devices, wearable applications, and human-machine interactions, etc. Moreover, the electronic information industry continues to gradually favor low-power electronic devices as a strategy to reduce carbon emissions and achieve global carbon neutrality.[290] Therefore, emphasis must be placed on the fabrication of electronic materials and devices by ALD, that match the growing global demands for green and sustainable electronics. The coming decades will continue to witness the rapid development in both improved ALD technologies and the availability of diverse MOs, MCs, and other emerging materials for new-generation devices and realistic applications.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

atomic layer deposition, electronics, metal chalcogenides, metal oxides, transistors

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[1] A. D. Franklin, Science 2015, 349, aab2750.
[2] S. Wang, J. Xu, W. Wang, G. N. Wang, R. Rastak, F. Molina-Lopez, J. W. Chung, S. Niu, V. R. Feig, J. Lopez, T. Lei, S. K. Kwon, Y. Kim, A. M. Fodeh, A. Ehrlich, A. Gasperini, Y. Yun, B. Murmann, J. B. Tok, Z. Bao, Nature 2018, 555, 83.
[3] T. Someya, M. Amagai, Nat. Biotechnol. 2019, 37, 382.
[4] A. Nawaz, L. Merces, D. M. de Andrade, D. H. S. de Camargo, C. C. Bof Bufon, Nat. Commun. 2020, 11, 841.
[5] F. S. Yang, M. Li, M. P. Lee, I. Y. Ho, J. Y. Chen, H. Ling, Y. Li, J. K. Chang, S. H. Yang, Y. M. Chang, K. C. Lee, Y. C. Chou, C. H. Ho, W. Li, C. H. Lien, Y. F. Lin, Nat. Commun. 2020, 11, 2972.
[6] W. Shi, Y. Guo, Y. Liu, Adv. Mater. 2020, 32, 1901493.
[7] P. C. Y. Chow, T. Someya, Adv. Mater. 2020, 32, 1902045.
[8] Z. Yin, Z. Yin, Y. Zhang, Q. Zheng, A. P. Zhang, Nano Energy 2019, 58, 96.
[9] Y. Dai, H. Hu, M. Wang, J. Xu, S. Wang, Nat. Electron. 2021, 4, 17.
[10] K. Myny, Nat. Electron. 2018, 1, 30.
[11] X. Ge, Z. Xia, S. Guo, Adv. Funct. Mater. 2019, 29, 1900318.
[12] A. H. Atabaki, S. Moazeni, F. Pavanello, H. Gevorgyan, J. Notaros, L. Alloatti, M. T. Wade, C. Sun, S. A. Kruger, H. Meng, K. Al Qubaisi, I. Wang, B. Zhang, A. Khilo, C. V. Baioocco, M. A. Popovic, V. M. Stojanovic, R. J. Ram, Nature 2018, 556, 349.
[13] M.-C. Choi, Y. Kim, C.-S. Ha, Prog. Polym. Sci. 2008, 33, 581.
[14] G. Shan, X. Li, W. Huang, Innovation 2020, 1, 100031.
[15] L. Mi, Innovation 2020, 1, 100015.
[16] E. Fortunato, P. Barquinha, R. Martins, Adv. Mater. 2012, 24, 2945.
[17] Z. Liu, Z. Yin, S.-C. Chen, S. Dai, J. Huang, Q. Zheng, Org. Electron. 2018, 53, 205.
[18] G. Horowitz, Adv. Mater. 1998, 10, 365.
[19] F. Hetsch, N. Zhao, S. V. Kershaw, A. L. Rogach, Mater. Today 2013, 16, 312.
[20] Y. Jiang, Z. Liu, Z. Yin, Q. Zheng, Mater. Chem. Front. 2020, 4, 1459.
[21] S. R. Thomas, P. Pattanansattayavong, T. D. Anthopoulos, Chem. Soc. Rev. 2013, 42, 6910.
[22] Z. Yin, M. J. Yin, Z. Liu, Y. Zhang, A. P. Zhang, Q. Zheng, Adv. Sci. 2018, 5, 1701041.
[23] Z. Liu, Z. Yin, J. Wang, Q. Zheng, Adv. Funct. Mater. 2019, 29, 1806092.
[24] Y. D. Park, B. Kang, H. S. Lim, K. Cho, M. S. Kang, J. H. Cho, ACS Appl. Mater. Interfaces 2013, 5, 8591.
[25] H. J. Yun, J. Lim, J. Roh, D. C. J. Neo, M. Law, V. I. Klimov, Nat. Commun. 2020, 11, 5280.
[26] H. Chen, W. Zhang, M. Li, G. He, X. Guo, Chem. Rev. 2020, 120, 2879.
[27] H. Kleemann, K. Kreehan, A. Fischer, K. Leo, Adv. Funct. Mater. 2020, 30, 1907113.
[28] M. Chhowalla, M. A. Amat, J. Zhou, F. Liu, B. K. Tay, H. Zhang, S. J. Pennycook, Z. Liu, Adv. Mater. 2018, 30, 1806092.
[29] W. Shi, Y. Guo, Y. Liu, Adv. Mater. 2020, 32, 1901493.
[30] Q. Fu, C. Zhu, X. Zhao, X. Wang, A. Chaturvedi, C. Zhu, X. Wang, Q. Zeng, J. Zhou, F. Liu, B. K. Tay, H. Zhang, J. J. Pennycook, Z. Liu, Adv. Mater. 2019, 31, 1804945.
[31] Z. Lin, Y. Liu, U. Halim, D. Jing, Y. Liu, Y. Wang, C. Jia, P. Chen, X. Duan, C. Wang, F. Song, M. Li, C. Wan, Y. Huang, X. Duan, Nature 2018, 562, 254.
[32] S. Lee, S. Kim, S. Shin, Z. Jin, Y.-S. Min, J. Ind. Eng. Chem. 2018, 58, 328.
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