Safety Verification of Phaser Programs

Zeinab Ganjie, Ahmed Rezine, Petru Eles and Zebo Peng
Linköping University, Sweden

Abstract

We address the problem of statically checking control state reachability (as in possibility of assertion violations, race conditions or runtime errors) and plain reachability (as in deadlock-freedom) of phaser programs. Phasers are a modern non-trivial synchronization construct that supports dynamic parallelism with runtime registration and deregistration of spawned tasks. They allow for collective and point-to-point synchronizations. For instance, phasers can enforce barriers or producer-consumer synchronization schemes among all or subsets of the running tasks. Implementations are found in modern languages such as X10 or Habanero Java. Phasers essentially associate phases to individual tasks and use their runtime values to restrict possible concurrent executions. Unbounded phases may result in infinite transition systems even in the case of programs only creating finite numbers of tasks and phasers. We introduce an exact gap-order based procedure that always terminates when checking control reachability for programs generating bounded numbers of coexisting tasks and phasers. We also show verifying plain reachability is undecidable even for programs generating few tasks and phasers. We then explain how to turn our procedure into a sound analysis for checking plain reachability (including deadlock freedom). We report on preliminary experiments with our open source tool.

1 Introduction

We focus on safety verification of programs using phasers for synchronization [1, 2, 3]. This sophisticated construct dynamically unifies collective and point-to-point synchronizations. For instance, it allows for dynamic registration and deregistration of tasks allowing for a more balanced usage of the computing resources when compared to static barriers or producer-consumer constructs [4]. The construct can be added to any parallel programming language with a shared address space. For instance, it can be found in Habanero Java [3], an extension of the Java programming language. Phasers build on the clock construct from the X10 programming language [1]. They can be created dynamically and spawned tasks may get registered or deregistered at runtime.

Intuitively, each phaser associates two phases (hereafter wait and signal phases) to each registered task. Apart from creating phasers and registering
each other to them, tasks can individually issue \texttt{wait} and \texttt{signal} commands to a phaser they are registered to. Intuitively, \texttt{signal} commands are used to inform other registered tasks the issuing task is done with its \texttt{signal} phase. The command is non-blocking. It increments the \texttt{signal} phase associated to the issuing task on the given phaser. The \texttt{wait} command is instead used to check whether all registered tasks are done with (i.e., have a \texttt{signal} phase that is strictly larger than) the issuing task’s \texttt{wait} phase. This command may get blocked by a task that did not yet finish the corresponding phase. Unlike classical barriers, phasers need not force registered tasks to wait for each other at each single phase. Instead they allow them to proceed with the following phases (by issuing \texttt{signal} commands), or even to exit the construct by deregistering from it. Such dynamic behavior allows for better load balancing and performance, but comes at the price of making it easy to introduce programming mistakes such as assertion violations, race conditions, runtime errors and, in the important situation where \texttt{wait} and \texttt{signal} commands are decoupled for maximum flexibility, deadlocks. We summarize our contributions in this work:

- We propose an operational model based on [2, 3, 5].
- We show undecidability of checking deadlock-freedom for programs with fixed numbers of tasks and phasers.
- We describe an exact gap-order based symbolic verification procedure for checking control state reachability (as in assertion violations, race conditions or runtime errors) and plain reachability (as in checking deadlock freedom).
- We show termination of the procedure for control state reachability when numbers of tasks and phasers are fixed.
- We describe how to turn the procedure into a sound over-approximation for plain reachability.
- We report on our preliminary experiments with our open source tool.

Related work. We are not aware of automatic formal verification works that focus on constructs allowing for such a degree of dynamic parallelism. Unlike [6], we focus on fully automatic verification and consider the richer and more challenging phaser construct. The work of [5] considers the dynamic verification of phaser programs and can therefore only reason about particular program inputs and runs. The work in [7] uses Java Path Finder [8] to explore several runs, but still for one concrete input at a time. The works in [9, 10] target gap-order systems. Although phaser programs share some of their properties (larger gaps can do more), the results in [9, 10] do not apply since gap-order systems crucially forbid exact increments.

Outline. We describe a phaser program and recall some preliminaries in Sections 2 and 3. This is followed in Section 4 by a formal description of phaser programs and of the properties we want to check. We also establish the
undecidability of checking deadlock freedom. In Section 5 we introduce our gap-order based symbolic representation. In Section 6 we describe our verification procedure and show decidability of checking control state reachability. We then introduce our relaxation procedure for checking plain reachability and briefly describe in Section 7 our application of view abstraction to the parameterized case. Finally, we report on our experiments and conclude the work.

2 Motivating example

The program listed in Fig. (1) uses Boolean shared variables B = \{a, b, done\}. A main task creates two phasers (lines 5 and 6). When creating a phaser, the task gets automatically registered to it. The main task also creates three other task instances (lines 9, 10 and 11). Several tasks can be registered to several phasers. When a task t is registered to a phaser p, a pair of numbers \((wait^t_p, sig^t_p)\), each in \(\mathbb{N} \cup \{+\infty\}\), is associated to the couple \((t, p)\). The pair represents the individual wait and signal phases of task t on phaser p.

Registration of a task to a phaser can occur in one of three modes: Sig\_Wait, Wait and Sig. In Sig\_Wait mode, a task may issue both signal and wait commands. In Wait mode, a task may only issue wait commands on the phaser. Finally, when registered in Sig mode, a task may only issue signal commands. Issuing a signal command by a task on a phaser results in the task incrementing its signal phase associated to the phaser. This command is non-blocking. On the other-hand, issuing a wait command by a task on a phaser p will block until all tasks registered on p exhibit signal values on p that are strictly larger than the wait value of the issuing task on phaser p. In this case, the wait phase of the issuing task is incremented. Intuitively, a signal command allows the issuing task to state other tasks need not wait for it to complete its signal phase. In retrospect, a wait command allows a task to make sure all registered tasks have moved past its wait phase.

Upon creation of a phaser, wait and signal phases are initialized to 0 (except in Wait mode where the signal phase is instead initialized to \(+\infty\) in order to not block other waiters). The only other way a task may get registered to a phaser is if an already registered task does register it in the same mode (or in Wait or Sig if the registrar is registered in Sig\_Wait). In this case, wait and signal phases of the newly registered task are initialized to those of the registrar. Tasks are therefore dynamically registered (e.g., lines 9-11). They can also dynamically deregister themselves (e.g., lines 25-26).

In this example, two producers and one consumer are synchronized using two phasers. The consumer requires the two producers to be ahead of it (wrt. the phaser main pointed to with prod) in order for it to consume their respective products. At the same time, the consumer needs to be ahead of both producers (wrt. the phaser main pointed to with cons) in order for these to produce their pair of products. It should be clear that phasers can be used as barriers for synchronizing dynamic subsets of concurrent tasks. Observe producers need not, in general, proceed in a lock step fashion. Producers may produce many
```c
bool a, b, done;
main()
{
done = false;
prod = newPhaser(SigWait);
cons = newPhaser(SigWait);
cons.signal();
async(aProducer, prod(Sig), cons(Wait));
async(bProducer, prod(Sig), cons(Wait));
async(abConsumer, prod(Wait), cons(Sig));
prod.drop();
cons.drop();
}
async(aProducer(p(Sig), c(Wait))
{
c.wait();
while(!done){
a = true;
p.signal();
c.wait();
}c.drop();
p.drop();
c.drop();
}
async(bProducer(p(Sig), c(Wait))
{
c.wait();
while(!done){
b = true;
p.signal();
c.wait();
}c.drop();
p.drop();
c.drop();
}
async(abConsumer(p(Wait), c(Sig))
{
while(!done){
p.wait();
assert(a && b);
a = false;
b = false;
if(ndet())
done = true;
c.signal();
}c.drop();
p.drop();
c.drop();
p.drop();
}
}
```

Figure 1: Two producers and one consumer are synchronized using two phasers. In this construction, the consumer requires both producers to be ahead of it (wrt. prod phaser) in order for it to consume their respective products. At the same time, the consumer needs to be ahead of both producers (wrt. cons phaser) in order for these to be able to produce their pair of products.
items before consumers “catch up”.

We are interested in checking: (a) control state reachability as in assertions (e.g., line 44), race conditions (e.g., mutual exclusion of lines 20 and 49) or runtime errors (e.g., signaling a dropped phaser), and (b) plain reachability as in deadlocks (e.g., a producer at line 23 and a consumer at line 50 with equal phases). Intuitively, both problems concern themselves with the reachability of target sets of program configurations. The difference is that control state reachability defines the targets with the states of the tasks (their control locations and whether they are registered to some phasers). Plain reachability can, in addition, use values or relations between values of involved phases. Observe that control state reachability depends on the values of the actual phases, but these values are not used to define the target sets. For example, assertions are expressed as predicates over boolean variables (e.g., line 44). Establishing such an assertion requires capturing the constraints imposed by the phasers on the program behaviors.

Our work proposes a sound and complete algorithm for checking control state reachability in case a bounded number of tasks and phasers are generated. The algorithm can handle arbitrarily large phases, e.g., generated using nested signaling loops. The algorithm starts from a symbolic representation of all bad configurations and successively computes sets of predecessor configurations. We show termination based on a well-quasi-ordering argument that imposes restrictions on what can be expressed with our symbolic representation. For instance putting upper bounds on differences between phases is forbidden. Deadlock configurations cannot be faithfully captured with such restricted representations. Intuitively, a deadlocked configuration will have a cycle where each involved task is waiting for the task to its right but where the wait phase of each task equals the signal phase of the task it is waiting for. We show the
problem of checking deadlock freedom to be undecidable even for programs only
generating a bounded number of tasks and phasers. We explain how to turn
our verification algorithm into a sound but incomplete procedure for checking
deadlock-freedom. Precision can then be augmented on demand to eliminate
false positives.

3 Preliminaries

We use \( \mathbb{N} \) and \( \mathbb{Z} \) for natural and integer numbers respectively. We write \( A \sqcup B \) to
mean the union of disjoint sets \( A \) and \( B \). We let \( \mathsf{Pfn}(A, B) \) be the set of partial
functions from \( A \) to \( B \) and use \( \emptyset_A \) for the empty function over \( A \), i.e., \( \emptyset_A(a) \) is undefined (written \( \emptyset_A(a) \uparrow \)) for all \( a \in A \). Given function \( g \in \mathsf{Pfn}(A, B) \) we write \( g(a) \downarrow \) to mean that \( g(a) \) is defined and write \( g\{a\} \) to mean the
restriction of \( g \) to the domain \( A \setminus \{a\} \). We write \( g\[a \leftarrow b\] \) for the function that
coincides with \( g \) on \( A \) except for \( a \) that is sent to \( b \). We abuse notation and let \( g\{a_i \leftarrow b_i \mid i \in I\} \), for a set \( \{a_i \mid i \in I\} \) of pairwise different elements, mean
the function that coincides with \( g \) on \( A \) except for each \( a_i \) that is sent to the
 cor responding \( b_i \). We sometimes write a function \( g \) as a set \( \{a \mapsto g(a) \mid a \in A\} \).
It is then implicitly undefined outside of \( A \).

4 Language

A program may use a set \( B \) of shared boolean variables and a set \( V \) of local phaser variables:

\[
\text{prg ::= bool } b_1,\ldots,b_{|B|}; \\
\text{task}_1(v_1,\ldots,v_{k_1})\{\text{stmt}_1\} \\
\vdots \\
\text{task}_n(v_{1_n},\ldots,v_{k_n})\{\text{stmt}_n\}
\]

\[
\text{stmt ::= v = newPhaser()} \mid \text{async(task, } v_1,\ldots, v_k) \\
\mid \text{v.drop()} \mid \text{v.signal()} \mid \text{v.wait()} \mid \text{exit} \\
\mid \text{stmt; stmt } b = \text{cond} \mid \text{assert(}\text{cond}) \\
\mid \text{while(}\text{cond}\{\text{stmt}\} \mid \text{if(}\text{cond}\{\text{stmt}\})
\]

\[
\text{cond ::= ndet()} \mid \text{true} \mid \text{false} \mid b \mid \text{cond } \lor \text{cond} \\
\mid \text{cond } \land \text{cond} \mid \neg\text{cond}
\]

A program consists in a set of tasks \( T \). A task is declared with \( \text{task}(v_1,\ldots,v_k)\{\text{stmt}\} \)
where \( v_1,\ldots,v_k \) are phaser variables that are local to the declared task. A task
can also create a new phaser with \( v = \text{newPhaser()} \) and store the identifier
of the phaser in a local variable \( v \). We let \( V \) be the union of all local phaser
variables. When creating a phaser, a task gets registered to it. To simplify our
description, we will assume all registrations to be in \text{Sig\_Wait} mode. Including
the other modes is a matter of changing the initial phase values at registration and of statically ensuring the issued commands respect the registration mode. A task can deregister itself from a phaser referenced by a variable \(v\) with \(v\text{.drop}()\). It can also issue signal or wait commands on a phaser on which it is registered and that is referenced by \(v\). A task can spawn another task with \(\text{async}(\text{task}, v_1, \ldots, v_n)\). The issuing task registers the spawned task to the phasers it points to with \(v_1, \ldots, v_n\). The issuing task need not wait for the spawned task and may directly continue its execution.

Assume a phaser program \(\text{prg} = (B, V, T)\). We inductively define the finite set \(S\) of control sequences as follows. \(S\) is the smallest set containing: (i) suffixes of each “\(\text{stmt}_i\)” appearing in some “\(\text{task}_i(v_1, \ldots, v_k)\{\text{stmt}_i\}\)” and “\(\text{while}(\text{cond})\{\text{stmt}_i\};\text{stmt}_j\)” (respectively “\(\text{while}(\text{cond})\{\text{stmt}_i\}\)” in \(S\)); and (iii) suffixes of “\(\text{stmt}_i;\text{stmt}_j\)” (respectively “\(\text{if}(\text{cond})\{\text{stmt}_i\}\)” appearing in \(S\). We write \(s\) to mean some control sequence in \(S\), and \(\text{hd}(s)\) and \(\text{tl}(s)\) to respectively mean the head and the tail of the sequence \(s\).

### 4.1 Semantics.

A configuration \(c\) of \(\text{prg} = (B, V, T)\) is a tuple \((T, \mathcal{P}, \mathcal{B}, \mathcal{P}_c, \mathcal{P}_v, \varphi)\) where:

- \(T\) is the current finite set of task identifiers. We let \(t, u\) range over the values in \(T\).
- \(\mathcal{P}\) is the current finite set of phaser identifiers. We let \(p, q\) range over the values in \(\mathcal{P}\).
- \(\mathcal{B}: B \rightarrow \{\text{true}, \text{false}\}\) is a total mapping that associates a value to each \(b \in B\).
- \(\mathcal{P}_c : T \rightarrow S\) is a total mapping that associates tasks to their remaining sequences (i.e., control location).
- \(\mathcal{P}_v : T \rightarrow \text{Pfn}(V, \mathcal{P})\) is a total mapping that associates, to each task identifier in \(T\), a partial mapping from the local phaser variables \(V\) to phaser identifiers \(\mathcal{P}\). It captures the values of the phaser variables \(V\) of each task.
- \(\varphi : \mathcal{P} \rightarrow \text{Pfn}(T, \mathbb{N}^2)\) is a total mapping that associates to each phaser \(p \in \mathcal{P}\) a partial mapping \(\varphi(p)\) that is defined exactly on the identifiers of the tasks registered to \(p\). For such a task \(t\), \(\varphi(p)(t)\) is the pair \((\text{wait}^t_p, \text{sig}^t_p)\) representing wait and signal values of \(t\) on \(p\).

The set of tasks \(T\) is altered by \(\text{async}(\text{task}, v_1, \ldots, v_n)\) and \(\text{exit}\) statements (rules (\text{async}) and (\text{exit}) in Fig.(3) of the appendix). The set of phasers \(\mathcal{P}\) is updated upon creation of new phasers (rule (\text{newPhaser}) in Fig.(3)) of the appendix. The mapping \(\mathcal{P}_v\) associates values to program phaser variables. Accessing variables with undefined values, or phasers to which the task is not
currently registered, leads to runtime errors (rule (runtime error)). The total mapping \( \varphi \) captures states of phasers. It associates to each phaser identifier \( p \) in \( \mathcal{P} \) a partial mapping \( \varphi(p) \). This partial mapping is defined for a task identifier \( t \in \mathcal{T} \) (i.e., \( \varphi(p)(t) \)) if the task \( t \) is registered to the phaser \( p \). In this case, \( \varphi(p) \) gives the waiting phase \( \text{wait}_p \) and the signaling phase \( \text{sig}_p \) of the task \( t \) on the phaser \( p \). Initially, a unique “main” task \( t_0 \) starts executing its stmt with no phasers. \( \varphi \) is the empty function with an empty domain \( \emptyset \). After a task \( t \) executes a \( v := \text{newPhaser}() \) statement (rule (newPhaser) in Fig. (3)) of the appendix, a new phaser \( p \) is associated to the variable \( v \) using \( p_v \) and \( \varphi(p) \) becomes the partial function \( \{ t \mapsto (0, 0) \} \). The initial configuration is \( c_{\text{init}} = (\{ t_0 \}, \emptyset, \emptyset, \emptyset, \emptyset) \), where a “main” task with identifier \( t_0 \) and code stmt is the unique initial task. No phasers are present in the initial configuration, and all boolean variables are mapped to false.

Given two configurations \( c \) and \( c' \) with \( c = (\mathcal{T}, \mathcal{P}, \text{bv}, \text{pc}, p_v, \varphi) \), we write \( c \rightarrow c' \) if there is a task \( t \in \mathcal{T} \) such that one of the rules in Fig. (3) of the appendix holds. We use \( \rightarrow^* \) for the reflexive transitive closure of \( \rightarrow \) and write \( c \rightarrow^* c' \) to mean that \( c' \) is reachable from \( c \). A configuration is said reachable if it is reachable from the initial configuration \( c_{\text{init}} \).

### 4.1.1 Control-state reachability

Checking the possibility of assertion violations, of runtime errors and of race conditions amounts to checking reachability of configurations respectively in \( \text{badConfs}_{\text{assert}}^{(n,p)} \), \( \text{badConfs}_{\text{runtime}}^{(n,p)} \) and in \( \text{badConfs}_{\text{race}}^{(n,p)} \) for some number of tasks \( n \) and number of phasers \( p \). We introduce in Section 5 a complete procedure for checking reachability of such sets of configurations and show it to be sound for programs with a fixed upper bounds on numbers of generated phasers and tasks.

### 4.1.2 Plain reachability and deadlocks.

We are also interested in checking the possibility of deadlocks. For this we need to define the notion of a blocked task. Assume in the following a configuration \( c = (\mathcal{T}, \mathcal{P}, \text{bv}, \text{pc}, p_v, \varphi) \).

**Definition 1** (Blocked). A task \( t \in \mathcal{T} \) is blocked at phaser \( p \in \mathcal{P} \) by task \( u \in \mathcal{T} \) if \( \text{hd}(\text{pc}(t)) \) = \( v \cdot \text{wait}() \) with \( p_v(t)(v) = p \) and \( \varphi(p)(t) = (\text{wait}_p, -) \) when \( \varphi(p)(u) = (\_ \_ \_ \_ \_ \text{sig}_p^u) \) and \( \text{sig}_p^u \leq \text{wait}_p^t \).

Intuitively, a task \( t \) is blocked by a task \( u \) if it cannot finish its \( \text{wait} \) command on some phaser because it is waiting for task \( u \) that did not issue enough \( \text{signal} \) commands on the same phaser.

**Definition 2** (Deadlock). \( (\mathcal{T}, \mathcal{P}, \text{bv}, \text{pc}, p_v, \varphi) \) is a deadlock configuration if each task of a non empty subset \( \mathcal{U} \subseteq \mathcal{T} \) is blocked by some task in \( \mathcal{U} \).

**Theorem 1** (Deadlock-Freedom). It is undecidable in general, even for programs with only three phasers and four tasks, to check for deadlock-freedom.
Proof. Sketch. We encode the reachability problem of any given 3-counters reset-VAS (vector addition system with reset arcs) as the reachability problem of a configuration with a simple cycle involving three tasks. Indeed, reachability of configuration \((s_F, 0, 0, 0)\) (three counters \(x, y, z\) with zero values at some control location \(s_F\)) is undecidable for reset-VASs. Figures 13 in the appendix describe a phaser program where a main task \(t\) spawns three tasks \(\{t_{12}, t_{23}, t_{31}\}\) s.t. \(t_{a\#b}\) runs \(\text{task}\#a\#b\) for each \(a\#b \in \{12, 23, 31\}\). The main task orchestrates the simulation and is registered to three phasers \(p_1, p_2\) and \(p_3\). Main and the other tasks use their respective local variable \(v_i\), for \(i \in \{1, 2, 3\}\), to point to phaser \(p_i\). The idea is to encode the value of counter \(x_{\#b}\) using the difference \(\text{sig}_{t_{a\#b}} - \text{wait}_{t_{a\#b}}\), for \(a\#b \#c \in \{123, 231, 312\}\). Resets of counter \(x_{\#b}\) are encoded by asking task \(t_{a\#b}\) to exit (hence deregistering from all phasers) and having task \(t_{a\#b}\) spawn a new \(\text{task}\#a\#b\). Finally asking each task \(t_{a\#b}\) to perform a \(\text{wait}\) on phaser \(v_{\#a}\) ensures a simple cycle of size 3 is built exactly when the three counters are 0. \(\square\)

5 Symbolic verification of phaser programs

We briefly introduce gap-order constraints and use them to define a symbolic representation (hereafter constraints) that we use in Section 6 for checking reachability.

5.1 Gap-order constraints and graphs [11, 12, 10, 9].

Gap-order constraints can be regarded as a particular case of the octagons or the unit two variables per inequality (utvi) constraints. Assume in this section that \(x\) and \(y\) are integer variables and that \(k\) is an integer constant. We use \(X\) and \(Y\) to mean finite sets of integer variables. A valuation \(\text{val}\) is a total function \(X \rightarrow \mathbb{Z}\). Valuations are implicitly extended to preserve constants (i.e. \(\text{val}(k) = k\) for any \(k \in \mathbb{Z}\)). A gap-order clause \(\delta\) over \(X\) is an inequality of the form \(a - b \geq k\) where \(a, b \in X \cup \{0\}\). A gap-order constraint \(\Delta\) over \(X\) is a finite conjunction of gap-order clauses over the same set \(X\). Observe that \((x = y + 2 \land y \leq 5)\) is essentially a gap-order constraint because it can be equivalently rewritten as the conjunction \((x - y \geq 2 \land y - x \geq 2 \land 0 - y \geq -5)\). Given a gap-order constraint \(\Delta\) over \(X\) and a valuation \(\text{val}: X \rightarrow \mathbb{Z}\), we write \(\text{val} \models \Delta\) to mean that \(\text{val}(a) - \text{val}(b) \geq k\) holds for each gap-order clause \(\delta: a - b \geq k\) appearing in \(\Delta\). We let \(\text{Sat}(\Delta)\) be the set \(\{\text{val}: X \rightarrow \mathbb{Z} \mid \text{val} \models \Delta\}\).

A gap-order graph (or graph for short) \(\varphi\) over \(X\) is a graph \((V, E)\) with vertices \(V = X \cup \{0\}\) where edges in \(E\) are of the form \(a \xrightarrow{k} b\) with \(a, b \in V\) and weight \(k\) in \(\mathbb{Z} \cup \{-\infty, +\infty\}\). We let \(\text{vars}(\varphi) = X\). Given a gap-constraint \(\Delta\) over \(X\), we can build the graph \(\text{graph}(\Delta)\) with vertices \(X \cup \{0\}\) and where \(E\) only contains a representative \(a \xrightarrow{k} b\) edge for each clause \(a - b \geq k\) appearing in \(\Delta\). A valuation \(\text{val}: X \rightarrow \mathbb{Z}\) satisfies a graph \(\varphi = (V, E)\) (written \(\text{val} \models \varphi\)) iff \(\text{val}(a) - \text{val}(b) \geq k\) for each \(a \xrightarrow{k} b \in E\). We let \(\text{Sat}(\varphi)\) be the set
\{\text{val} : X \to \mathbb{Z} | \text{val} \models \varphi\}. Clearly, \text{Sat}(\text{graphOf}(\Delta)) = \text{Sat}(\Delta). The closure \text{clo}(\varphi) of a graph \varphi = (V, E) is the unique complete graph with the same vertices V and where \( a \xrightarrow{k'} b \) is an edge of \text{clo}(\varphi) iff \( k' \in \mathbb{Z} \cup \{-\infty, +\infty\} \) is the least upper bound of all weight-sums for any path in \varphi from \( a \) to \( b \). Closure allows us to deduce \((0 - x \geq -7)\) from \((y - x \geq -2 \land 0 - y \geq -5)\). The result of the closure procedure is a special graph \( \varphi_{\text{false}} \) denoting the graph without any satisfying valuation each time a weight \( k = +\infty \) is generated. The closure of a graph can be computed in polynomial time and we get \( \text{Sat}(\text{clo}(\varphi)) = \text{Sat}(\varphi) \).

We define the degree of a graph \( \varphi \) (written \( \text{degreeOf}(\varphi) \)) to be 0 if no edge in \( \text{clo}(\varphi) \) has a negative weight apart from \( -\infty \). Otherwise, \( \text{degreeOf}(\varphi) \) is the largest natural \( k \in \mathbb{N} \) such that there is an edge in \( \text{clo}(\varphi) \) with weight \(-k\). For instance, the degree of the graph resulting from \((x - y \geq 2 \land y - x \geq -4)\) is 4. We systematically close all manipulated graphs and write \( G(X) \) for the set of closed graphs over \( X \). Given a graph \( \varphi \), we write \( \varphi[x/y] \) to mean the graph obtained by replacing the vertex \( x \) by the vertex \( y \). We abuse notation and write \( \varphi[\{x_i/y_i \mid i \in I\}] \), for pairwise different \( x_i \) elements to mean the simultaneous application of the individual substitutions. For a set of variables \( Y \), we write \( \varphi \ominus Y \) to mean the graph obtained by removing the variables in \( Y \) from the vertices of \( \varphi \). Given two closed graphs \( \varphi \) and \( \varphi' \) over the same \( X \), we write \( \varphi \subseteq \varphi' \) to mean that each directed edge in \( \varphi \) is labeled with a larger weight in \( \varphi' \). As a result, \( \text{Sat}(\varphi') \subseteq \text{Sat}(\varphi) \). Finally, we write \( \varphi \odot \varphi' \) to mean the closure of the graph obtained with merging the two sets of vertices and edges. As a result, \( \text{Sat}(\varphi \odot \varphi') = \text{Sat}(\varphi) \cap \text{Sat}(\varphi') \).

### 5.2 Constraints as a symbolic representation.

A constraint \( \varphi \) is a tuple \((T, P, \text{bu, pc, pv, p}, \gamma)\) where the only difference with the definition of a configuration \((T, P, \text{bu, pc, pv, p}, \varphi)\) is the adoption of a gap-order constraint \( \gamma \) instead of \( \varphi \). More specifically, \( \gamma : P \to \bigcup_{U \subseteq \varphi} G(\bigcup_{s \in U} \{\omega^t, \sigma^t\}) \) is a total mapping that associates a gap-order graph to each phaser \( p \in P \).

Intuitively, we use variables \( \omega^t_p \) and \( \sigma^t_p \) to constrain in graph \( \gamma(p) \) possible values of both wait \( (\text{wait}^t_p) \) and signal \( (\text{sig}^t_p) \) phases of each task \( t \) registered to phaser \( p \). As a result, we can check if task \( t \) is registered to phaser \( p \) according to graph \( \varphi = \gamma(p) \) by checking if \( \{\omega^t_p, \sigma^t_p\} \subseteq \text{varsOf}(\varphi) \). We will write \( \text{Reg}(p, \varphi) \) to mean the set of tasks \( \{t \mid \{\omega^t_p, \sigma^t_p\} \subseteq \text{varsOf}(\varphi)\} \). We also write \( \text{isReg}(t, p, \varphi) \) for the predicate \( t \in \text{Reg}(p, \varphi) \). Observe that the language semantics impose that, for each phaser \( p \) and for any pair \( t, u \) of tasks in \( \text{Reg}(p, \varphi) \), the predicate \( 0 \leq \text{wait}^t_p \leq \text{sig}^u_p \) is an invariant. For this reason, we always safely strengthen, in any obtained \( \gamma(p) = \varphi \), weights \( k \) in \( \omega^t_p \xrightarrow{k} \omega^u_p \), \( \sigma^t_p \xrightarrow{k} 0 \) and \( \omega^t_p \xrightarrow{\max(k,0)} \). The following definition helps us characterize configurations for which our procedure terminates.

**Definition 3** (degree and freeness of constraints). A constraint \((T, P, \text{bu, pc, pv, p}, \gamma)\) has as degree the largest degree among all its graphs \( \gamma(p) \) for \( p \in P \) if \( P \) is not empty and 0 otherwise. Furthermore, a constraint is said to be “free” if, for
any $p \in \mathcal{P}$, the only edges in $\gamma(p)$ with weights different from $-\infty$ are edges of the forms (i) $\sigma_p^{k(\sigma_p, \omega_p)} \rightarrow \omega_p^u$, (ii) $\sigma_p^{k(\sigma_p)} \rightarrow 0$, or (iii) $\omega_p^{k(\omega_p)} \rightarrow 0$ for some $t, u \in \text{Reg}(p, \gamma(p))$ and $k(\sigma_p, \omega_p), k(\sigma_p), k(\omega_p) \in \mathbb{N}$.

Free constraints are only allowed to impose, for the same phaser, non-negative lower bounds on differences between signals and waits, between signals and 0, and between waits and 0. Like degree-0-constraints, free constraints are not allowed to put a positive upper bound on how much a signal is larger than a wait. Unlike degree-0-constraints, they are not allowed to put bounds on the differences among signal values, or among wait values. For instance a free constraint cannot impose $\sigma_p^i - \sigma_p^j = 0$ while a degree-0-constraint can. Intuitively, freeness does not oblige our verification procedure to maintain exact differences when firing "signal" or "wait" instructions, jeopardizing termination. This will be stated in Section 5.3.

**5.3 Denotations of constraints.**

Given a configuration $c = (T, \mathcal{P}, \textbf{bu}, \textbf{pc}, \textbf{pv}, \phi)$ and a constraint $\phi = (T', \mathcal{P}', \textbf{bu}', \textbf{pc}', \textbf{pv}', \gamma')$, we say that $c$ satisfies $\phi$, and write $c \models \phi$, if $c$ satisfies (up to a renaming of the tasks and the phasers) conditions imposed by $\phi$. More concretely, $c \models \phi$ if $\textbf{bu} = \textbf{bu}'$ and there are bijections $\tau: T \rightarrow T'$ and $\pi: \mathcal{P} \rightarrow \mathcal{P}'$ such that: (i) $\textbf{pc}(t) = \textbf{pc}'(\tau(t))$ for each $t \in T$; and (ii) $\pi(\textbf{pv}(t)(v)) = \textbf{pv}'(\tau(t))(v)$ for each $t \in T$ and $v \in V$; and (iii) the renaming of tasks and phasers in $\phi$ wrt. $\tau$ and $\pi$ satisfies $\gamma$, i.e., (iii.a) for each $t \in T$ and each $p \in \mathcal{P}$, $\phi(p)(t) \downarrow$ iff $\text{isReg}(\tau(t), \pi(p), \gamma(\pi(p)))$, and (iii.b) for each $p' \in \mathcal{P}'$, $\phi(\bigwedge_{t' \in \text{Reg}(p', \gamma(p'))} (\omega_{p'}^{t'}, \sigma_{p'}^{t'}) = \phi(\pi^{-1}(\gamma(p'))(\tau^{-1}(t')))) \models \gamma(p')$. We let $[\phi]$ denote $\{c \mid c \models \phi\}$. Intuitively, $[\{T, \mathcal{P}, \textbf{bu}, \textbf{pc}, \textbf{pv}, \gamma\}]$ contains all configurations $c$ with the same number of tasks and phasers and such that there are renamings of tasks and phasers that preserve in $c$ the correspondence between $\textbf{pc}$, $\textbf{pv}$ and $\gamma$. We write $[\Phi]$, for a set $\Phi$ of constraints, to mean the union $\bigcup_{\phi \in \Phi} [\phi]$. Given a program $(B, V, T)$, we can exactly characterize with a finite set of constraints all configurations involving $n$ tasks and $p$ phasers and satisfying the premises of rules (runtime error), (assert fault), (race) and (deadlock) from Fig. 3 of the appendix.

**Lemma 1** (Characterizing badness). Given a program $(B, V, T)$ and natural numbers $(n, p)$, we can exhibit finite sets of constraints $\text{badCstrs}_{\text{race}}^{(n, p)}$, $\text{badCstrs}_{\text{assert}}^{(n, p)}$, $\text{badCstrs}_{\text{runtime}}^{(n, p)}$ and $\text{badCstrs}_{\text{deadlock}}^{(n, p)}$ such that:

\[
\begin{align*}
\text{badCstrs}_{\text{race}}^{(n, p)} &= [\text{badCstrs}_{\text{race}}^{(n, p)}] \\
\text{badCstrs}_{\text{assert}}^{(n, p)} &= [\text{badCstrs}_{\text{assert}}^{(n, p)}] \\
\text{badCstrs}_{\text{runtime}}^{(n, p)} &= [\text{badCstrs}_{\text{runtime}}^{(n, p)}] \\
\text{badCstrs}_{\text{deadlock}}^{(n, p)} &= [\text{badCstrs}_{\text{deadlock}}^{(n, p)}]
\end{align*}
\]

In addition, we can choose the constraints in $\text{badCstrs}_{\text{deadlock}}^{(n, p)}$ to be of degree 0 while those in $\text{badCstrs}_{\text{race}}^{(n, p)}$, $\text{badCstrs}_{\text{assert}}^{(n, p)}$ or in $\text{badCstrs}_{\text{runtime}}^{(n, p)}$ to be free.
Proof. Observe that $n$ and $p$ are given naturals. Fix a task set $T = \{t_1, \ldots, t_n\}$ of size $n$ and a phaser set $P = \{p_1, \ldots, p_p\}$ of size $p$. We can therefore enumerate all tuples $(T, P, bv, pc, pv)$ where:

- $bv : B \to \{true, false\}$ is a total mapping that associates a value to each $b \in B$.
- $pc : T \to S$ is a total mapping that associates tasks to a sequence $s \in S$
- $pv : T \to \text{Pfn}(V, P)$ is a total mapping that associates, to each task identifier in $T$, a partial mapping from the local phaser variables $V$ to phaser identifiers $P$.

Let $C$ be the set of such tuples. Observe that tuples in $C$ are missing information about tasks’ registration and wait and signal values. We complete this information in the following. Given a set $U \subseteq T$ of tasks and a phaser $p \in P$, we write $\text{topOf}(U, p)$ to mean the graph of the conjunction $\bigwedge_{u, v \in U}(\sigma^t_u \geq \omega^p_u \geq 0)$. Observe that an invariant of all phaser programs is that signal and wait phases (of all tasks registered on a given phaser) are always non-negative with the formers always larger or equal than the laters. For this reason, $\text{topOf}(U, p)$ is the weakest possible graph where the set $U$ is registered to a phaser $p$. Observe that $\text{topOf}(U, p)$ is free. We now finish the definitions of $\text{badCstrs}_{\text{race}}(n, p)$, $\text{badCstrs}_{\text{assert}}(n, p)$, $\text{badCstrs}_{\text{runtime}}(n, p)$, $\text{badCstrs}_{\text{deadlock}}(n, p)$:

- Add to $\text{badCstrs}_{\text{race}}(n, p)$ all constraints $(T, P, bv, pc, pv, \gamma)$ where:
  - $(T, P, bv, pc, pv)$ is a tuple of $C$ with two different tasks $t$ and $u$ in $T$ executing a read or a write on a boolean variable with at least one of them writing it (see $\text{badConf}_{\text{race}}(n, p)$ in Fig. 3) of the appendix.
  - The total mapping $\gamma$ associates $\text{topOf}(U_p, p)$ to each phaser $p$, where $U$ is some subset of $T$. Intuitively, for each phaser $p$, we consider all registration possibilities (some subset $U \subseteq T$) while imposing the weakest possible constraints on the signal and wait phases of the registered tasks. Observe $\gamma$ is free.

- Add to $\text{badCstrs}_{\text{assert}}(n, p)$ all constraints $(T, P, bv, pc, pv, \gamma)$ where:
  - $(T, P, bv, pc, pv)$ is a tuple of $C$ with some task $t$ in $T$ executing an assertion on a boolean condition that evaluates to false with $bv$ (see $\text{badConf}_{\text{assert}}(n, p)$ in Fig. 3) of the appendix.
  - The total mapping $\gamma$ associates $\text{topOf}(U_p, p)$ to each phaser $p$, where $U$ is some subset of $T$. Observe $\gamma$ is free.

- Add to $\text{badCstrs}_{\text{runtime}}(n, p)$ all constraints $(T, P, bv, pc, pv, \gamma)$ where:
  - $(T, P, bv, pc, pv)$ is a tuple of $C$ with some task $t$ in $T$ is executing a statement that involves a phaser variable $v$. 

12
By construction, we have considered all possible tuples \((T, p)\), where \(T\) is some subset of \(\mathcal{T}\). In addition, we require that either \(\text{pv}(t)(\nu) \uparrow\) or \(p = \text{pv}(t)(\nu)\) with \(t \not\in \text{Reg}(p, \gamma(p))\). (see \text{badConf}^{(n,p)}\text{runtime}\) in Fig. 3 of the appendix. Observe \(\gamma(q)\) is free for all \(q\) on which \(\gamma\) is defined. Observe \(\gamma\) is free.

- Add to \text{badCstrs}^{(n,p)}\text{deadlock}\) all constraints \((T, \mathcal{P}, \mathcal{B}, \mathcal{P}, \mathcal{C}, \mathcal{P}, \mathcal{U})\) where:
  - \((T, \mathcal{P}, \mathcal{B}, \mathcal{P}, \mathcal{C}, \mathcal{P}, \mathcal{U})\) is a tuple of \(\mathcal{C}\) where a set of tasks \(t_0, \ldots, t_{m-1}\) in \(T\) are executing wait commands on phaser variables \(v_0, \ldots, v_{m-1}\) in \(V\).
  - Again, the total mapping \(\gamma\) associates \text{topOf}(\mathcal{U}, p)\) to each phaser \(p\), where \(\mathcal{U}\) is some subset of \(\mathcal{T}\). We however require that: \(p_i = \text{pv}(v_i)\) for each \(i: 0 \leq i < m\) and, \(t_i\) is waiting for \(t_{(i+1)\%m}\) in \(\gamma p_i\), i.e., \(\gamma p_i\) imposes the wait phase of \(t_i\) on \(p_i\) is equal to the signal phase of \(t_{(i+1)\%m}\) on \(p_i\). In other words, the edge \(\sigma_{p_i}^{t_{(i+1)\%m}} \rightarrow \omega_{p_i}^{t_i}\) in \(\gamma p_i\). (see \text{badConf}^{(n,p)}\text{deadlock}\) in Fig. 3 of the appendix. Observe the graphs in \(\gamma\) are not all free since some of them put an upper bound on how large some signal value are compared to some wait values. They are however of degree 0 since the only negative weights are \(-\infty\).

By construction, we have considered all possible tuples \((T, \mathcal{P}, \mathcal{B}, \mathcal{P}, \mathcal{C}, \mathcal{P}, \mathcal{U})\) and registration combinations. We have all considered the weakest possible constraints on the phases for the registred tasks. In addition, any configuration in the denotation constraints will belong to the corresponding bad set. \(\square\)

5.4 Entailment.

We say that a constraint \(\phi = (T, \mathcal{P}, \mathcal{B}, \mathcal{P}, \mathcal{C}, \mathcal{P}, \mathcal{U}, \gamma)\) is weaker than a constraint \(\phi' = (T', \mathcal{P}', \mathcal{B}', \mathcal{P}', \mathcal{C}, \mathcal{P}, \mathcal{U}', \gamma')\), written \(\phi \subseteq \phi'\), to mean the following. First, the two constraints have the same number of phasers and tasks, agree on the values of the boolean variables and, up to renamings, on the values of the phaser variables and on which tasks are registered to which phasers. Second, the constraints on the wait and signal values are stronger in \(\phi'\) than in \(\phi\). More formally, \(\phi \subseteq \phi'\) if \(\mathcal{B} = \mathcal{B}'\) and there are bijections \(\tau: T \rightarrow T'\) and \(\pi: \mathcal{P} \rightarrow \mathcal{P}'\) s.t. for each \(t \in T\) and \(p \in \mathcal{P}\) the following four conditions hold: (i) \(\text{pc}(t) = \text{pc}'(\tau(t))\); and (ii) \(\pi(\text{pv}(t)(\nu)) = \text{pv}'(\tau(t))(\nu)\); and (iii) \(\pi(\text{Reg}(p, \gamma(p))) = \text{Reg}(\pi(p), \gamma'(\tau(p)))\); and (iv) \(\gamma(p) \subseteq \gamma'(\tau(p))\) \(\left\{\omega_{\pi(p)}^{\tau(t)}, \omega_{\pi'(p)}^{\tau(t)}, \sigma_{\pi(p)}^{\tau(t)}, \sigma_{\pi'(p)}^{\tau(t)} \mid t \in \text{Reg}(p, \gamma(p))\right\}\). Clearly, \(\phi \subseteq \phi'\) implies \([\phi'] \subseteq [\phi]\). We say that \(\subseteq\) is sound.

We can show that \(\subseteq\) is a well-quasi-order\(^1\) over constraints of bounded degrees and involving fixed numbers of tasks and phasers since \(\subseteq\) is itself a well-quasi-ordering over graphs of bounded degrees over a finite set of variables \((\mathcal{I} \cap \mathcal{G})\).

\(^{1}\)A reflexive and transitive binary relation \(\leq\) is a well-quasi-order over a set \(A\) if there is no infinite sequence \(a_0, a_1, \ldots\) of \(A\) elements s.t. \(a_i \not\leq a_j\) for all \(i < j\).
Lemma 2 (WQO). Given \( k, n, p \in \mathbb{N} \), the entailment relation \( \sqsubseteq \) over the set of constraints of degree \( k \) involving at most \( n \) tasks and \( p \) phasers is a well-quasi-order.

Proof. Assume an infinite sequence \( \phi_1, \phi_2, \ldots \) of constraints where \( \phi_i = (T_i, \varphi_i, \mathbf{b}_i, \mathbf{p}_i, \mathbf{v}_i, \gamma_i) \) where \( |T_i| = n \) and \( |T_i| = p \) for all \( i \geq 1 \) and where all appearing graphs have degree \( k \) or less. We can assume wlog that \( T_i = T_j \) and \( \varphi_i = \varphi_j \) for any \( i, j \geq 1 \). We show there are \( i < j \) such that \( \phi_i \sqsubseteq \phi_j \). There is a finite number of different values for \( \mathbf{b}_i, \mathbf{p}_i, \gamma_i \) and for the domains of \( \gamma_i(p) \) for each \( p \in \mathcal{P} \). We can therefore extract an infinite subsequence where:

- \( \mathbf{b}_i = \mathbf{b}_j, \mathbf{p}_i = \mathbf{p}_j, \gamma_i(p) = \gamma_j(p) \), and
- for each \( p \in \mathcal{P} \), the domains of \( \gamma_i(p) \) and \( \gamma_j(p) \) coincide.

Observe that for each phaser \( p \in \mathcal{P} \), the graphs \( \gamma_i(p) \) are the same up to possible differences on the weights. Let \( \leq \) be the component-wise ordering on vectors. Each graph \( \gamma_i(p) \) is of degree \( k \) or less. We can therefore organize its weights as a vector \( \text{vectorOf}(\gamma_i(p)) \) with elements in \( \mathbb{Z} \cup \{-\infty, +\infty\} \) but where the only allowed negative elements are those larger than \(-k\). The vectors can be organized in a way that \( \text{vectorOf}(\gamma_i(p)) \leq \text{vectorOf}(\gamma_j(p)) \) means \( \gamma_i(p) \sqsubseteq \gamma_j(p) \). We then repeat the following steps for each \( p \in \mathcal{P} \): using Higman’s lemma \([13]\) and the degree boundedness of the constraints, we extract an infinite sequence of constraints where \( \text{vectorOf}(\gamma_{a_i}(p)) \leq \text{vectorOf}(\gamma_{a_c}(p)) \) if \( a_b < a_c \).

6 Verification Procedure

\begin{itemize}
  \item \textbf{Input:} A program \( \text{prg} = (B, V, T) \), a set \( \Phi_{\text{bad}} \) of pairwise \( \sqsubseteq \)-incomparable constraints, maximum upper bounds \( t^* \) and \( p^* \) (in \( \mathbb{N} \cup \{+\infty\} \)) on coexisting tasks and phasers.
  \item \textbf{Output:} A symbolic run to \( \Phi_{\text{bad}} \) or the value \textbf{unreachable}
  \begin{enumerate}
    \item Initialize both Working and Visited to \( \{(\phi, \tau) \mid \phi \in \Phi_{\text{bad}}\} \);
    \item while there exists \( (\phi, \tau) \in \text{Working} \) do
      \begin{enumerate}
        \item remove \( (\phi, \tau) \) from Working;
        \item let \( (\tau, \varphi, \mathbf{b}, \mathbf{p}, \mathbf{v}, \gamma) = (\phi) \);
        \item if \( |\mathcal{T}| > t^* \) or \( |\mathcal{P}| > p^* \) then continue;
        \item if \( c_{\text{init}} = \phi \) then return \( \tau \);
        \item foreach \( t \in T \) do
          \begin{enumerate}
            \item foreach \( \phi' \in \text{pre}(t, \phi) \) do
              \begin{enumerate}
                \item if \( \psi \sqsubseteq \phi' \) for all \( \psi, \tau \in \text{Visited} \) then
                  \begin{enumerate}
                    \item Remove from Working and Visited each \( (\psi, \tau) \) for which \( \phi' \sqsubseteq \psi \);
                    \item Add \( (\phi', \phi' \cdot t \cdot \tau) \) to both Working and Visited;
                  \end{enumerate}
              \end{enumerate}
            \end{enumerate}
          \end{enumerate}
      \end{enumerate}
    \end{enumerate}
  \end{itemize}

Procedure \texttt{check(prg, \Phi_{\text{bad}}, t^*, p^*)}, a simple working list procedure for checking constraints reachability.

14
We discuss in the following the procedure depicted below and assume a program \( \text{prg} \) and a set \( \Phi_{bad} \) of constraints the reachability of which we want to check. \( \Phi_{bad} \) can for example be any subset of \( \text{badCstrs}^{(n,p)}_{\text{deadlock}} \) (degree 0) or of \( \text{badCstrs}^{(n,p)}_{\text{assert}} \) (free) in case we want to check the possibility of a deadlock or of an assertion violation.

It is not difficult to show that \( \left[ \text{pre}(t, \phi) \right] \) (obtained as described in Fig.6 of the appendix) coincides with \( \{c' \mid c' \vdash c \text{ and } c \in [\phi]\} \). Using the soundness of \( \sqsubseteq \), we can show by induction the partial correctness of the procedure \( \text{check(prg,} \Phi_{bad},+\infty,+\infty) \).

**Lemma 3** (Partial correctness). If \( \text{check(prg,} \Phi_{bad},+\infty,+\infty) \) returns unreachable, then \( c_{\text{init}} \not\rightarrow [\Phi_{bad}] \). If it returns a trace \( \phi_n \cdot t_n \cdots t_1 \cdot \phi_1 \) then there are \( c_n, \ldots, c_1 \) with \( c_n = c_{\text{init}}, c_1 \in [\Phi_{bad}] \) and \( c_i \vdash c_{i-1} \) for \( i : 1 < i \leq n \).

**Proof.** Sketch. Assume a constraint \( \phi = (T, \text{P}, \text{bv, pc, pv, } \gamma) \). It should be clear that we can complete the definition of \( \sim \) (with the rules for the non-phaser-related statements) in such a way that \( \bigcup_{\phi \in \text{pre}(t, \phi)} \) coincides with \( \{c' \mid c' \vdash c \text{ with } c \in [\phi]\} \). We can establish by induction the following procedure invariants. At iteration \( m \):

- \( \text{Working}_m \subseteq \text{Visited}_m \)
- \( (\phi_n, \phi_n \cdot t_n \cdots t_1 \cdot \phi_1) \in \text{Visited}_m \) then there are \( c_n, \ldots, c_1 \) with \( c_n \in [\phi_n] \) and \( c_1 \in [\Phi_{bad}] \) and \( c_i \vdash c_{i-1} \) for \( i : 1 < i \leq n \).
- If \( c = c_m \) is such that: \( c_i \vdash c_{i-1} \) for \( i : 1 < i \leq m \) with \( c_1 \in [\Phi_{bad}] \) then, by soundness of \( \sqsubseteq \), there is \( (\phi, \tau) \in \text{Visited}_m \) such that \( c_m \in [\phi] \).

**Theorem 2** (Free termination). \( \text{check(prg,} \Phi_{bad},t^*,p^*) \) terminates for \( t^*, p^* \in \mathbb{N} \) and free \( \Phi_{bad} \).

**Proof.** Sketch. Freeness is preserved by the \( \text{pre} \) computation (Fig.6 of the appendix). Then we use, similar to [14, 15], the fact that non-termination would allow us to build an infinite sequence of constraints passing the test at line 9 of the procedure. More concretely, let \( \phi_1, \phi_2, \ldots \) be the sequence of constraints that pass (in that order) the test at line 9. If a constraint \( \phi_i \) is replaced by another constraint \( \phi_k \), then \( \phi_k \subseteq \phi_i \). This holds for any replaced constraint. By transitivity, this means all replacements happen with weaker constraints. This means \( \phi_i \nsubseteq \phi_j \), for any \( i < j \). This violates well quasi ordering of \( \sqsubseteq \) over the degree-0 constraints.

In order to check reachability of arbitrary constraints, we may need to force termination. We do this by soundly bounding the degree of generated constraints using a relaxation \( \rho_k \). The relaxation \( \rho_k((T, \text{P}, \text{bv, pc, pv, } \gamma)) \) replaces, in each graph \( \gamma(p) \), each weight \( k'' \) s.t. \( k'' < -k \) with \( -\infty \).
foreach $\phi'' \in \text{pre}(t, \phi)$ do
  Let $\phi' = \rho_k(\phi'')$;

Fig. 6. Systematic relaxation

**Theorem 3** (Forced termination). *Independently of the degree of $\Phi_{\text{bad}}$, Procedure check$(\text{prg}, \Phi_{\text{bad}}, t^*, p^*)$, where line 8 is replaced by the two lines of Fig. (6), is sound and guaranteed to terminate.*

*Proof.* Soundness is due to the validity of $\rho_k(\phi) \subseteq \phi$ while the termination argument relies, similarly to Theorem (2), on well-quasi orderedness of $\subseteq$ on the set of constraints with bounded degree and fixed numbers of tasks and phasers. \hfill \square

7 The parameterized case

We apply view abstraction [16] to derive a sound analysis for programs with arbitrary numbers of coexisting tasks. In this preliminary work, only the number of tasks is parameterized. Assume a program $\text{prg} = (B, V, T)$.

**Constraint views.** The view $(T, P, bv, pc, pv, \gamma)\mid_U$ of a constraint $(T, P, bv, pc, pv, \gamma)$ wrt. set $U \subseteq T$ is the tuple $(U, P, bv, pc)\mid_U, pv\mid_U, \{p \mapsto \gamma(p)\mid_U \mid p \in P\}$ where:

i) $pc\mid_U$ is the restriction of $pc$ to the domain $U$.

ii) $pv\mid_U$ is the restriction of $pv$ to the domain $U$.

iii) $\gamma(p)\mid_U$ is obtained by restricting the variables of $\gamma(p)$ to $\{\sigma^t, \omega^t \mid t \in U\}$, i.e., capturing $U$'s signals and waits.

Intuitively, views are obtained by projecting on subsets of tasks. A view $\phi\mid_U$ is said to be of size $k = |U|$. For $k \geq 0$, we aim to compute a least fixpoint $\Psi_k$ starting from $\alpha_k(\text{constraintOf}(c_{\text{init}}))$ and satisfying $\Psi_k \subseteq \alpha_k(\text{post}_\rho(\gamma_k(\Psi_k)))$ ($\Phi \subseteq \Psi$ if there is $\phi \in \Phi$ with $\phi \not\subseteq \psi$ for each $\psi \in \Psi$). The idea is to restrict the computations to a finite number of tasks using the abstraction $\alpha_k$ and the concretization $\gamma_k$ (see [16] for more details). The operator $\text{post}_\rho$ consists in a simple post computation (see Fig. (7) of the appendix) followed by a relaxation $\rho$ that bounds the degree of the obtained views to some predetermined value. The relaxation is applied to ensure termination for bounded view sizes. Intuitively, any $\text{post}_\rho$ reachable constraint will have all its views of size $k$ captured by some views in $\Psi_k$.

Abstraction and concretizations are defined as follows:

1. Abstraction $\alpha_k(\Phi)$ of set $\Phi$ is the union $\alpha_k^1(\Phi) \cup \alpha_k^2(\Phi)$ where:

   a) $\alpha_k^1(\Phi) = \{(T, P, bv, pc, pv, \gamma) \in \Phi \mid |T| \leq k\}$

   b) $\alpha_k^2(\Phi) = \{\phi\mid_T \mid \phi \in \Phi \wedge |T| = k\}$.  

    16
2. Concretization $\gamma_k(\Phi)$ of a set $\Phi$ is the union $\gamma_k^1(\Phi) \cup \gamma_k^2(\Phi)$ where:

(a) $\gamma_k^1(\Phi) = \Phi$, and
(b) $\gamma_k^2(\Phi)$ is the set of $\phi = (T, P, bv, pc, pv, \gamma)$ constraints s.t. $U \subseteq T \land |U| = k$ implies $\phi|_U \in \Phi$

We first compute the fixpoint using only $\alpha^1_k$ and $\gamma^1_k$. If the denotation of the fixpoint’s views intersects the one of $\Phi_{\text{bad}}$, then we return the faulty trace. Because we only use $\alpha^1_k$ and $\gamma^1_k$, the only approximation is due to the relaxation $\rho$. The precision of the relaxation can then be increased. Otherwise, we use $\alpha_k$ and $\gamma_k$ in order to over-approximate the fixpoint. If the obtained views still do not include bad configurations, then we conclude that no matter how many tasks are generated, bad configurations are unreachable. In case the views do include bad configurations then we restart the analysis with views of bigger sizes (i.e., restart with a larger $k$).

8 Experimental Results

We report on experiments with our open source prototype hjVerify for the verification of phaser programs. We conducted experiments on 12 different programs (some of which are from [5]). We considered both deadlocks and assertions reachability problems. For each property, we considered correct and buggy versions. This gave 48 different instances with 2 to 3 phasers and 2 to 4 tasks (except for the parameterized case). Our tool uses global phaser and task variables as in [5]. We have experimented with adapting the view abstraction technique [16] to verify phaser programs generating arbitrary many tasks, i.e., parameterized verification where the number of phasers is fixed. (see appendix for more details.) We report on two parameterized examples. Experiments were conducted on a 2.9GHz processor with 8GB of memory.

https://gitlab.ida.liu.se/apv/hjVerify
| program                  | property          | safe / buggy | times         |
|--------------------------|-------------------|--------------|---------------|
| 01.Loopless              | deadlock: ok / trace | 1s / 1s      |               |
|                          | assertion: ok / trace | 1s / 1s      |               |
| 02.Iterative            | deadlock: ok / trace | 1s / 1s      |               |
| averaging               | assertion: ok / trace | 1s / 1s      |               |
| 03.Ordered              | deadlock: ok / trace | 1s / 1s      |               |
| phasers                 | assertion: ok / trace | 13s / 1s     |               |
| 04.Conditional          | deadlock: ok / trace | 2s / 1s      |               |
|                          | assertion: ok / trace | 4s / 7s      |               |
| 05.Loop Synch.          | deadlock: ok / trace | 178s / 145s  |               |
|                          | assertion: ok / trace | 7s / 13s     |               |
| 06.Nested forks         | deadlock: ok / trace | 2s / 1s      |               |
|                          | assertion: ok / trace | 1s / 1s      |               |
| 07.Conditional          | deadlock: ok / trace | 1s / 1s      |               |
| membership              | assertion: ok / trace | 12s / 3s     |               |
| 08.Producer-consumer    | deadlock: ok / trace | 37s / 222s   |               |
|                          | assertion: ok / trace | 79s / 34s    |               |
| 09.Parameterized        | deadlock: ok / trace | 20s / 1s     |               |
| loopless                | assertion: ok / trace | 6s / 1s      |               |
| 10.Parameterized        | deadlock: ok / trace | 1s / 1s      |               |
| iterative-averaging     | assertion: ok / trace | 1s / 1s      |               |
| 11.Running-2            | deadlock: ok / trace | 5s / 1s      |               |
|                          | assertion: ok / trace | 26s / 4s     |               |
| 12.Running-3            | deadlock: ok / trace | 4318s / 128s |               |
|                          | assertion: ok / trace | 18631s / 54s |               |

Our implemented procedure does not eagerly concretize all tasks states as described in the predecessor computation of Section 5. Instead we collect conditions on the phases of the threads that did not take any action yet and lazily concretize them. Reported times for checking deadlocks are the sums of the times required to check reachability for each cycle. The prototype is only a proof of concept. For instance, the example (12.Running-3) is a variant of (11-Running-2) where a task instance is spawned twice leading to two symmetrical tasks (out of four). This required up to three orders of magnitude more time to check. We believe partial order reduction techniques would help here. Other relevant heuristics would be to make use of priority queues and to organize the minimal sets. All examples are available on the tool homepage.

9 Conclusion

We have proposed a gap-order based reachability analysis for phaser programs. We have showed our analysis to be exact and guaranteed to terminate when checking runtime, race and assertion errors. We have established the undecidability of deadlock verification and explained how to turn our analysis into a sound over-approximation. To the best of our knowledge, this is beyond the ca-
pabilities of current verification techniques which currently only target concrete inputs to phaser programs. We are currently working on tackling the parameterized case and have obtained preliminary encouraging results. Apart from improving the scalability of the tool and from using it in combination with predicate abstraction and abstract interpretation in order to analyze actual source code, we are investigating the applicability of the presented techniques for the verification of similar synchronization constructs.

References

[1] P. Charles, C. Grothoff, V. Saraswat, C. Donawa, A. Kielstra, K. Ebcioglu, C. von Praun, and V. Sarkar, “X10: An object-oriented approach to non-uniform cluster computing,” SIGPLAN Not., vol. 40, no. 10, pp. 519–538, Oct. 2005. [Online]. Available: http://doi.acm.org/10.1145/1103845.1094852

[2] J. Shirako, D. M. Peixotto, V. Sarkar, and W. N. Scherer, “Phasers: a unified deadlock-free construct for collective and point-to-point synchronization,” in 22nd annual international conference on Supercomputing. ACM, 2008, pp. 277–288.

[3] V. Cavé, J. Zhao, J. Shirako, and V. Sarkar, “Habanero-java: the new adventures of old x10,” in Proceedings of the 9th International Conference on Principles and Practice of Programming in Java. ACM, 2011, pp. 51–61.

[4] J. Shirako, D. M. Peixotto, V. Sarkar, and W. N. Scherer, “Phaser accumulators: A new reduction construct for dynamic parallelism,” in Parallel & Distributed Processing, 2009. IPDPS 2009. IEEE International Symposium on. IEEE, 2009, pp. 1–12.

[5] T. Cogumbreiro, R. Hu, F. Martins, and N. Yoshida, “Dynamic deadlock verification for general barrier synchronisation,” in 20th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming, ser. PPoPP 2015. New York, NY, USA: ACM, 2015, pp. 150–160. [Online]. Available: http://doi.acm.org/10.1145/2688500.2688519

[6] D.-K. Le, W.-N. Chin, and Y.-M. Teo, “Verification of static and dynamic barrier synchronization using bounded permissions,” in International Conference on Formal Engineering Methods. Springer, 2013, pp. 231–248.

[7] P. Anderson, B. Chase, and E. Mercer, “Jpf verification of habanero java programs,” SIGSOFT Softw. Eng. Notes, vol. 39, no. 1, pp. 1–7, Feb. 2014. [Online]. Available: http://doi.acm.org/10.1145/2557833.2560582

[8] K. Havelund and T. Pressburger, “Model checking java programs using java pathfinder,” International Journal on Software Tools for Technology Transfer (STTT), vol. 2, no. 4, pp. 366–381, 2000.
[9] R. Mayr and P. Totzke, “Branching-time model checking gap-order constraint systems,” *Fundamenta Informaticae*, vol. 143, no. 3-4, pp. 339–353, 2016.

[10] L. Bozzelli and S. Pinchinat, “Verification of gap-order constraint abstractions of counter systems,” *Theoretical Computer Science*, vol. 523, pp. 1 – 36, 2014. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S030439751300892X

[11] P. Z. Revesz, “A closed-form evaluation for datalog queries with integer (gap)-order constraints,” *Theoretical Computer Science*, vol. 116, no. 1, pp. 117–149, 1993.

[12] S. Lahiri and M. Musuvathi, “An efficient decision procedure for utvpi constraints,” in *Frontiers of Combining Systems (FroCos ’05)*. Springer Verlag, May 2005. [Online]. Available: https://www.microsoft.com/en-us/research/publication/an-efficient-decision-procedure-for-utvpi-constraints/

[13] G. Higman, “Ordering by divisibility in abstract algebras,” *Proceedings of the London Mathematical Society*, vol. 3, no. 1, pp. 326–336, 1952.

[14] P. A. Abdulla, K. Cerans, B. Jonsson, and Y.-K. Tsay, “General decidability theorems for infinite-state systems,” in *Logic in Computer Science, 1996. LICS’96. Proceedings., Eleventh Annual IEEE Symposium on*. IEEE, 1996, pp. 313–321.

[15] A. Finkel and P. Schnoebelen, “Well-structured transition systems everywhere!” *Theoretical Computer Science*, vol. 256, no. 1, pp. 63 – 92, 2001. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S030439750000102X

[16] P. A. Abdulla, F. Haziza, and L. Holík, “All for the price of few,” in *International Workshop on Verification, Model Checking, and Abstract Interpretation*. Springer, 2013, pp. 476–495.
Figure 3: Operational semantics of phaser statements.
main(){
  v1 = newPhaser();
  v2 = newPhaser();
  v3 = newPhaser();
  q = s0;
  com = done;
  async(task12,v1,v2,v3);
  async(task23,v2,v3,v1);
  async(task31,v3,v1,v2);
  v1.drop();
  v2.drop();
  v3.drop();
  while (true){
    // check reachability
    if(( * ) && (q == sF)){
      com = check;
      exit;
    };
    // let f,g,h be strings automorphisms on strings
    // that coincide with the identity except for
    // that (f($a)=1, f($b)=2 and f($c)=3), (g($a)=2,
    // g($b)=3 and g($c)=1) and (h($a)=3, h($b)=1
    // and h($c)=2). Syntactically apply each
    // morphism to the remaining part of the while loop.
    // case (si ,inc ( x$a ),sj)
    if(( * ) && (q == si)){
      com = t($c$a)_inc_x($a);
      while(com != done){}
      q = sj;
    };
    // case (si, dec ( x$a ),sj)
    if(( * ) && (q == si)){
      com = t$a$b_dec_x$a;
      while(com != done){}
      q = sj;
    };
    // case (si, reset ( x$a ),sj)
    if(( * ) && (q == si)){
      com = t$a$b_reset_x$a;
      while(com != done){}
      q = sj;
    };
  }
}
// Syntactically apply each morphism in \{f,g,h\} to the whole body of the task. This gives three tasks \text{task12}(v_1,v_2,v_3), \text{task23}(v_2,v_3,v_1) and \text{task31}(v_3,v_1,v_2)

\begin{verbatim}
task$a$b(v$a,v$b,v$c)
    while(true){
        if (com = t$a$b_inc_x$b){
            v$b.sig();
            com = done;
        }
        if (com = t$a$b_dec_x$a){
            v$a.sig();
            com = t$b$c_dec_x$a;
            v$a.wait();
            while(com != t$a$b_dec_x$a) {
                com = done;
            }
        }
        if (com = t$a$b_dec_x$b){
            v$b.wait();
            com = t$c$a_dec_x$b;
        }
        if (com = t$a$b_dec_x$c){
            v$c.sig();
            com = t$b$c_dec_x$c;
            v$c.wait();
            while(com != t$a$b_dec_x$c) {
                com = t$c$a_dec_x$c;
            }
        }
        if (com = t$a$b_reset_x$a){
            v$a.sig();
            com = t$b$c_reset_x$a;
            while(com != t$a$b_reset_x$a) {
                v$a.wait();
                asynch(taskc$a,v$c,v$a,v$b);
                com = done;
            }
        }
        if (com = t$a$b_reset_x$b){
            com = t$b$c_reset_x$b;
            exit;
        }
        if (com = t$a$b_reset_x$c){
            v$c.sig();
            com = t$b$c_reset_x$c;
            while(com != t$a$b_reset_x$c) {
                v$c.wait();
                com = t$c$a_reset_x$b;
            }
        }
        if (com = check){
            v$a.sig();
            v$a.wait();
        }
    }
\end{verbatim}

Figure 5: Three tasks: task12, task23 and task31 synchronize with the main task in the encoding of the reachability of any three counters reset machine as reachability of a deadlock configuration of a phaser program.
Figure 6: Derivation rules for computing \( \text{pre}(t, \phi) \) as union of all \( \{\phi' \mid \phi \overset{t}{\rightarrow} \phi' \} \) with \( \phi = (T, \mathcal{P}, \mathcal{B}, \mathcal{P}, \gamma) \) and \( t \in T \).
\[
\text{graphOf } \omega = \text{newPhaser}; s \land p \not\in \mathcal{P} \land \\
\gamma' = \gamma \left[ p \leftarrow \left( \text{graphOf } \left( \omega^p_s = \sigma^p_s = 0 \right) \right) \right] \\
(\forall \mathcal{P}, \mathcal{Q}, \mathcal{R}, \mathcal{P}_\text{pc}, \omega, \gamma) \overset{\text{newPhaser}}{\rightarrow} (\forall \mathcal{P}', \mathcal{Q}', \mathcal{R}', \mathcal{P}_\text{pc}', \omega', \gamma') \\
\text{pc}(t) = v.\text{signal}; s \land \\
\gamma' = \gamma \left[ p \leftarrow \left( \left( (\gamma(p) | \sigma^p_s / \sigma) \odot \text{graphOf } \left( \sigma^p_s = \sigma + 1 \right) \right) \oplus \{ \sigma \} \right) \right] \\
(\forall \mathcal{P}, \mathcal{Q}, \mathcal{R}, \mathcal{P}_\text{pc}, \omega, \gamma) \overset{\text{signal}}{\rightarrow} (\forall \mathcal{P}', \mathcal{Q}', \mathcal{R}', \mathcal{P}_\text{pc}', \omega', \gamma') \\
\text{pc}(t) = \text{assert(\text{cond})}; s \land \\
\text{be(\text{cond}) = true} \\
(\forall \mathcal{P}, \mathcal{Q}, \mathcal{R}, \mathcal{P}_\text{pc}, \omega, \gamma) \overset{\text{assert, ok}}{\rightarrow} (\forall \mathcal{P}', \mathcal{Q}', \mathcal{R}', \mathcal{P}_\text{pc}', \omega', \gamma') \\
\text{pc}(t) = v.\text{drop}; s \land \text{pc}(t)(v) = p \land \\
\text{isReg}(t, p, \gamma(p)) \land \\
\gamma' = \gamma \left[ p \leftarrow \left( \gamma(p) \odot \left( \omega^p_s = \omega^p_s \land \sigma^p_s = \sigma^p_s \right) \right) \right] \\
(\forall \mathcal{P}, \mathcal{Q}, \mathcal{R}, \mathcal{P}_\text{pc}, \omega, \gamma) \overset{\text{drop}}{\rightarrow} (\forall \mathcal{P}', \mathcal{Q}', \mathcal{R}', \mathcal{P}_\text{pc}', \omega', \gamma') \\
\text{pc}(t) = \text{asynch(task, v_1, \ldots, v_n); s_1} \land \text{paramOf(task) = (v_1, \ldots, v_n)} \land \\
\text{for all } i : 1 \leq i \leq k, \text{pc}(t)(v_i) = p_i \land \text{isReg}(t, p_i, \gamma(p_i)) \land \\
u \not\in \mathcal{P} \land \text{pc}(t)(v) = p \land \\
\text{pc}(t)(v_i) = p_i \text{ for } p_i \in \mathcal{P} \text{ and } 1 \leq i \leq k \\
\gamma' = \gamma \left[ \left\{ p_i \leftarrow \gamma(p_i) \odot \text{graphOf } \left( \omega^p_s = \omega^p_s \land \sigma^p_s = \sigma^p_s \right) \right\} \right] \\
(\forall \mathcal{P}, \mathcal{Q}, \mathcal{R}, \mathcal{P}_\text{pc}, \omega, \gamma) \overset{\text{asynch}}{\rightarrow} (\forall \mathcal{P}', \mathcal{Q}', \mathcal{R}', \mathcal{P}_\text{pc}', \omega', \gamma') \\
\text{pc}(t) = v.\text{wait}; s \land \text{pc}(t)(v) = p \land \text{isReg}(t, p, \gamma(p)) \land \\
\pi' = \Lambda_{(u,v) \in \gamma(p)} \left( \omega^p_s < \sigma^p_s \right) \land \text{isSat}(\gamma(p) \odot \pi) \land \\
\gamma' = \gamma \left[ p \leftarrow \left( (\gamma(p) \odot \pi) \odot \text{graphOf } \left( \omega^p_s = \omega + 1 \right) \right) \oplus \{ \omega \} \right] \\
(\forall \mathcal{P}, \mathcal{Q}, \mathcal{R}, \mathcal{P}_\text{pc}, \omega, \gamma) \overset{\text{wait}}{\rightarrow} (\forall \mathcal{P}', \mathcal{Q}', \mathcal{R}', \mathcal{P}_\text{pc}', \omega', \gamma') \\
\text{pc}(t) = \text{exit} \land \text{pc}' = \text{pc} \setminus \{ t \} \land \\
\gamma' = \gamma \left[ \left\{ p \leftarrow \gamma(p) \odot \left( \omega^p_s, \sigma^p_s \right) \right\} \right. \\
\left. \left. \land p \in \mathcal{P} \right\} \right] \\
(\forall \mathcal{P}, \mathcal{Q}, \mathcal{R}, \mathcal{P}_\text{pc}, \omega, \gamma) \overset{\text{exit}}{\rightarrow} (\forall \mathcal{P}', \mathcal{Q}', \mathcal{R}', \mathcal{P}_\text{pc}', \omega', \gamma') \\
\text{Figure 7: Computing } \text{post}(t, (\mathcal{P}, \mathcal{Q}, \mathcal{R}, \mathcal{P}_\text{pc}, \omega, \gamma)) \text{ for some } t \in \mathcal{T}. \text{ Phasers' related part of the symbolic successor computation used during the view abstraction based parameterized analysis of phaser programs.}