Achieving short high-quality gate-all-around structures for horizontal nanowire field-effect transistors

J G Gluschke1, J Seidl1, A M Burke1,2, R W Lyttleton1,2, D J Carrad1,3, A R Ulah1,4, S Fahlio, S Lehmann2, H Linke2 and A P Micolich1

1 School of Physics, University of New South Wales, Sydney NSW 2052, Australia
2 Solid State Physics and NanoLund, Lund University, SE-22100, Lund, Sweden
3 Center for Quantum Devices, Niels Bohr Institute, University of Copenhagen, Copenhagen DK-2100, Denmark
4 School of Chemical and Physical Sciences, Victoria University of Wellington, Wellington 6021, New Zealand

E-mail: adam.micolich@nanoelectronics.physics.unsw.edu.au

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Abstract
We introduce a fabrication method for gate-all-around nanowire field-effect transistors. Single nanowires were aligned perpendicular to underlying bottom gates using a resist-trench alignment technique. Top gates were then defined aligned to the bottom gates to form gate-all-around structures. This approach overcomes significant limitations in minimal obtainable gate length and gate-length control in previous horizontal wrap-gated nanowire transistors that arise because the gate is defined by wet-etching. In the method presented here gate-length control is limited by the resolution of the electron-beam-lithography process. We demonstrate the versatility of our approach by fabricating a device with an independent bottom gate, top gate, and gate-all-around structure as well as a device with three independent gate-all-around structures with 300, 200, and 150 nm gate length. Our method enables us to achieve subthreshold swings as low as 38 mV dec−1 at 77 K for a 150 nm gate length.

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(Some figures may appear in colour only in the online journal)

1. Introduction
The continuous miniaturisation of the field-effect transistor (FET) has enabled the fabrication of increasingly powerful circuits on a single microchip. The performance of traditional planar FETs drops significantly as the source–drain separation is pushed below 50 nm due to short channel effects [1]. These short channel effects can be mitigated by improving the gate coupling [1–4]. This led to the development of fin-FET devices with gates interfacing the channel from three sides [1–5]. Optimal gate coupling is obtained from gate structures that enclose the transistor channel from all sides [1, 6, 7]. These structures can be difficult to make using the conventional top-down fabrication techniques employed for planar devices [6–8]. Yet, significant research efforts are directed towards developing top-down gate-all-around devices by industrial manufacturers, for example, dense stacked-channel arrays [9–11].

A bottom-up approach exploiting self-assembled nanowires offers a simpler pathway to fully conformal ‘gate-all-around’ structures [12]. These nanowires stand vertically, enabling a conformal coating of gate oxide and gate metal to be applied in a straightforward way [13–17]. The nanowires can be processed into vertical FET arrays on the growth substrate [13–15] or can be transferred to a separate device substrate to create horizontal devices [16, 17]. Vertical nanowire arrays have achieved near thermal-limit subthreshold swings [18].
integration of III–Vs on Si [19], and continue down a road towards practical applications [20]. This orientation has also seen work to incorporate heterostructured nanowires towards high-performance tunnel-FETs [21, 22] and produce multiple independent ‘wrap gates’ [23]. Turning to horizontal wrap-gated nanowire transistors, these are of interest for basic research devices, e.g. quantum electronics, but also as a possible complement for vertical transistors in 3D-integrated circuits [24]. Fabrication of multiple independent wrap-gates has also been achieved in the horizontal orientation, giving a significant advantage on scalability over the vertical orientation [17].

A major limitation of horizontal wrap-gate nanowire transistors [16, 17] is that the gate length is defined by wet-etching. This limits control and restricts the minimum achievable gate length [17]. Shorter gates are also intrinsically of lower quality in this instance because unintentional over-etching introduces ‘mouse-bite’ defects—small holes in the gate metal and oxide that compromise both performance and yield [17]. Burke et al [17] found that the shortest gate length that could be reliably achieved was ~300 nm. The minimal gate length is important for electronics applications and basic research. For industrial applications, the gate length governs the density of devices on a microchip. For research studies, sub-200 nm gates are desirable for nanowire quantum devices e.g. gate-defined quantum dots [25, 26] and nanowire quantum point contacts [27–30].

Here, we introduce a fabrication process for horizontal nanowire FETs with multiple gate-all-around structures that maintains the advantages of the horizontal orientation while overcoming the limitations arising from wet-etching. The gate length is defined instead by electron-beam lithography (EBL) patterned metal deposition. This presents the challenge of obtaining the portion of the gate directly underneath the nanowire. We achieve this by depositing nanowires on pre-fabricated bottom gates before completing the gate-all-around structure by depositing a top gate aligned with the bottom gate. A crucial aspect of the fabrication process is that the nanowire is aligned perpendicular to the bottom gate. This alignment is achieved with high accuracy using a resist-trench technique (see figure 1) [31, 32]. As a result, the minimal achievable gate length, control over gate length, and gate-metal quality are limited by the EBL process rather than wet-etch steps. At this point we note a nomenclature distinction regarding wrap-gates and gate-all-around structures. The wrap-gate devices [16, 17] have unambiguously conformal gate metallisation. In contrast, our process has the possibility of small voids under the nanowire edges (see figure 2(e)). For clarity, in distinguishing between them, we refer to our devices as gate-all-around structures rather than wrap gates.

We demonstrate the full capacity of our method with two devices. The first is a single-nanowire with independently controllable bottom gate, top gate, and gate-all-around structures. It highlights that the strongest gating is obtained.
2. Experimental details

2.1. Nanowire alignment

Our devices are made on an n$^+$-Si substrate capped with 100 nm of SiO$_2$ and 10 nm of HfO$_2$. The HfO$_2$ layer serves as an etch-stop layer when the Al$_2$O$_3$ gate insulator is etched during contact formation [16]. Arrays of bottom gates were patterned by EBL and evaporation of Ni/Au (5/25 nm), as shown in figure 1(a). The bottom gates are 150–300 nm wide, 10 µm long and have variable inter-gate spacing. There are 20 bottom-gate arrays per 100 × 100 µm$^2$ device field (figure 1(g)) to enable satisfactory device yield.

The nanowires are positioned using a resist-trench method [31, 32], as follows: the substrate was spin-coated with ~300 nm of MicroChem polymethyl methacrylate (PMMA) 950k A5 EBL resist. Trenches with length 10 µm and width 200–400 nm were defined by EBL. These trenches are perpendicular to the underlying bottom gates (see figure 1(e)). Any resist residue in the trenches was removed with a 30 s oxygen-plasma etch after development (50 W, 340 mTorr).

Wurtzite InAs nanowires approximately 50 nm in diameter and 3–10 µm long were grown by chemical beam epitaxy [35] (device in figure 3) or metal organic vapour phase epitaxy [36] (device in figure 4). They were conformally coated with a 16 nm Al$_2$O$_3$ gate dielectric by atomic layer deposition. The oxide coating of the nanowire removes the need to cover the bottom gates with an insulator as done previously [26, 30]. The nanowires were picked up from the growth substrate with the tip of a triangular piece of clean-room tissue and deposited on top of the patterned resist. Approximately 20–50 nanowires were transferred to each of the 24 100 × 100 µm$^2$ regions with 20 bottom-gate arrays per 100 × 100 µm$^2$ region (figure 1(g)). The substrate was then covered in a single droplet of isopropyl alcohol. A piece of clean-room tissue was used to brush the nanowires into the trenches until the isopropyl alcohol evaporated completely (see figures 1(b) and (c)). This process was repeated 2–4 times until no nanowires were visible on top of the resist near the area patterned with trenches under a dark-field microscope. Finally the PMMA resist was removed in an acetone bath leaving the aligned nanowires adhered to the bottom-gate array (see figure 1(d)). Any nanowires left on top of the resist were washed away, leaving only aligned nanowires. Empty trenches cannot be distinguished from trenches with nanowires using a 1000× optical microscope prior to the removal of the resist.

We estimated the yield of the alignment procedure by counting the nanowires in seven 100 × 100 µm$^2$ regions each with 100 trenches after the initial deposition and again after
removal of the resist. Typically, 5%–30% of 20–50 distributed nanowires were aligned successfully (see figure 1(g)). This yield is sufficient for research applications as a complete device only requires one nanowire per $100 \times 100 \mu m^2$ region. Lard et al [32] have demonstrated the assembly of highly-ordered nanowire arrays with this method using higher nanowire density and fine-tuning of the trench dimensions. This demonstrates the scalability of this approach, which could be used, e.g. to prototype integrated nanowire circuits with multiple nanowires on the same chip. 

In this study, the trench width had no significant impact on the yield of captured nanowires for trench widths of 200, 300, and 400 nm. We rarely observed multiple nanowires captured in the same trench. This is likely due to the large supply of trenches relative to the number of available nanowires. An unexpected finding was that the accuracy of angular nanowire alignment was independent of trench width. We attribute this to the nanowires sticking to the trench side-walls during capture, resulting in optimal angular alignment for nearly all nanowires (see figure 1(e)). The orientation is generally maintained upon removal of the resist as shown in figure 1(f).

### 2.2. Nanowire contacts

The fabrication process for the source, drain, and gate electrodes for a device with a gate-all-around structure, a top gate, and a bottom gate is shown in figure 2. Figure 3(a) shows the finished device. The same processing steps can be applied to create devices with multiple gate-all-around structures such as the nanowire FET shown in figure 4(a). The substrate with the aligned nanowires (figure 2(a)) was once more coated with EBL resist. Top gates were exposed and metallised (Ni/Au, 6/134 nm) after a 30 s oxygen-plasma treatment to remove any resist residue (see figure 2(b)). Excess metal was removed together with the EBL resist in an acetone lift-off at 60 °C. 

Source and drain contacts were exposed in a final EBL step. The Al$_2$O$_3$ coating was removed from the exposed nanowire ends by a 15 s buffered HF etch (1:7 HF:NH$_4$F) as shown in figure 2(c). Wet-etching can be eliminated by substituting the gate oxide with the organic gate insulator parylene, which can be removed by oxygen-plasma etching [38]. The sample was treated with (NH$_4$)$_2$S$_2$ solution immediately prior to the metal deposition by thermal evaporation (Ni/Au, 6/134 nm) to ensure ohmic contacts [39]. Excess metal was removed in an acetone lift-off at 60 °C giving the completed device shown in figure 2(e).

### 2.3. Electrical measurements

All electrical measurements were performed in liquid nitrogen (temperature $T = 77$ K) to improve gate stability and reduce hysteresis due to charge trapping at the Al$_2$O$_3$/InAs interface [17]. A dc source–drain voltage $V_{sd} = 50$ mV was applied at the source contact to drive a drain current $I_d$ measured using a Keithley 6517A electrometer at the drain. The gate voltage $V_g$ was applied using the dc auxiliary ports of a Stanford Research SR830 lock-in amplifier after confirming negligible gate leakage ($<100$ pA) for the individual gates with a Keithley K2401 source-measure unit. $I_d$ was recorded for decreasing $V_g$. Only one gate was swept at a time with all other gates kept grounded.

### 3. Results and discussion

#### 3.1. Bottom, top, and gate-all-around structure

Figure 3(a) shows a scanning-electron microscopy image of a device with three different gate types: a top gate, a gate-all-around structure, and a bottom gate. All three gates are approximately 250 nm in length. The EBL process yielded smooth, conformal metal gates without the ‘mouse-bite’ defects found in short horizontal wrap gates [17]. Overlapping top and bottom gates are aligned to within 10 nm. The top gates are up to 20 nm wider than the bottom gates because top gate evaporation was carried out at an angle of 15–20° under rotation to ensure gate continuity across the nanowire. If required, this can be compensated for by reducing the width of the top gates in the EBL pattern. We estimate the coverages as 100% for the gate-all-around structure, 73% for the top gate, and 17% for the bottom gate based on geometrical considerations.

Figure 3(b) shows the electrical performance of the three individual gates from a nominally identical device. The gate-all-around structure gives the steepest subthreshold swing $S = 33$ mV dec$^{-1}$. This is approximately twice the thermal
limit of $15.3 \text{ mV dec}^{-1}$ at 77 K and competitive with the $S = 25$ to 43 mV dec$^{-1}$ reported by Burke et al [17] for InAs nanowire FETs with longer, etch-defined wrap-gates at 77 K. The $\Omega$-shaped top gate performs almost as well giving $S = 38 \text{ mV dec}^{-1}$. This is consistent with modelling predictions [33, 34]. The bottom gate performs significantly worse with $S = 256 \text{ mV dec}^{-1}$ due to reduced gate coupling resulting from the limited gate coverage of the nanowire circumference. The reduced gate coupling means that higher gate voltages are required to deplete the nanowire. This causes a shift in threshold voltage $V_{th}$ to more negative values. The shift is small for the top gate but larger for the bottom gate.

### 3.2. Different gate lengths

A device with three different length gate-all-around structures demonstrates the enhanced control over gate length and ability to make shorter gates. Figure 4(a) shows a false-coloured SEM image of a device with three gate-all-around structures 300, 200, and 150 nm long. Data from a nominally identical device is displayed in figure 4(b). The threshold voltage $V_{th} = -1.10 \text{ V}$ for the 300 nm gate-all-around structure is similar to the $V_{th} = -1.15 \text{ V}$ obtained for the 250 nm gate-all-around structure in figure 3. $V_{th}$ is shifted significantly to larger negative $V_{th}$ for the 150 nm and 200 nm gates indicating decreased effective gate coupling per gate length. Interestingly, no degradation in subthreshold swing is observed with decreased gate length. In fact, $S$ improves slightly for the shorter gates with $S = 51 \text{ mV dec}^{-1}$ for the 300 nm long gate, 44 mV dec$^{-1}$ for the 200 nm gate, and 38 mV dec$^{-1}$ for the 150 nm gate. A similar behaviour was observed by Burke et al [17] in wrap-gated InAs nanowire transistors at 77 K (see supplementary information, available online at stacks.iop.org/NANO/30/064001/mmedia). Three-dimensional electrostatic-modelling studies have shown that effective gate capacitance per length decreases for shorter gates due to fringing effects [40–43]. This leads to a shift in threshold voltage to more negative values as the gate length decreases. This shift is non-linear and increases with reduced length [2, 40, 41]. Generally, drain-induced barrier lowering also contributes, driving an associated degradation in subthreshold swing [2, 41]. This is clearly not observed in figure 4(b) and we speculate that the small source-drain bias and the strong gate coupling [1, 2, 6, 44] make this effect insignificant for the gate lengths studied here. This effect may become significant for gate lengths <100 nm. Electrostatic simulations [45] for this aspect of these devices could generate further insight and are encouraged.

### 4. Conclusion

We introduced a versatile fabrication technique for gate-all-around structure nanowire FETs. Single nanowires were positioned perpendicularly on top of pre-defined bottom gates using a resist-trench alignment technique [31, 32]. Top gates were then created in alignment with bottom gates to form gate-all-around structures. This approach overcomes a key limitation of established wrap-gate methods [16, 17] where a metal etch is used to define gate segments; namely the limitation of gate-length control and minimal gate length due to over-etching. Gate length and quality in our approach are only limited by the resolution of the EBL process. We demonstrated the length control by fabricating a device with independent 300, 200, and 150 nm long gate-all-around structures with a subthreshold swing of $38 \text{ mV dec}^{-1}$ at 77 K for the 150 nm gate. We expect process optimisation will yield further significant reduction in minimal gate length as sub-20 nm features can be achieved with commercial EBL systems [46, 47]. This platform may be interesting to systematically study gate-length dependent transistor performance. Our process also enables the fabrication of multiple gate types such as gate-all-around structures, top gates and bottom gates on the same nanowire. The gate-all-around structure performed best followed by the top gate and then the bottom gate. This is expected due to the different electrostatic couplings of the gate geometries [33, 45].

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### ORCID iDs

J G Gluschke © https://orcid.org/0000-0001-7165-8852
A M Burke © https://orcid.org/0000-0001-9345-2812
D J Carrad © https://orcid.org/0000-0003-0372-8593
S Lehmann © https://orcid.org/0000-0002-4091-905X
A P Micolich © https://orcid.org/0000-0003-2855-3582

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