torchgpipe: On-the-fly Pipeline Parallelism for Training Giant Models

Chiheon Kim\*  Heungsub Lee\*  Myungryong Jeong\^  Woonhyuk Baek\^  Boogeon Yoon\  Ildoo Kim\  Sung Lim\^  Sungwoong Kim\^  
\^Kakao Brain  \\^UNIST

\{chiheon.kim,heungsub.lee,myungryong.jeong,wbaek,eric.yoon,ildoo.kim,swkim\}@kakaobrain.com

\[sungbin@unist.ac.kr\]

Abstract

We design and implement a ready-to-use library in PyTorch for performing micro-batch pipeline parallelism with checkpointing proposed by GPipe \[11\]. In particular, we develop a set of design components to enable pipeline-parallel gradient computation in PyTorch’s define-by-run and eager execution environment. We show that each component is necessary to fully benefit from pipeline parallelism in such environment, and demonstrate the efficiency of the library by applying it to various network architectures including AmoebaNet-D \[23\] and U-Net \[24\]. Our library is available at \[https://github.com/kakaobrain/torchgpipe\].

1. Introduction

In recent years, deep learning has seen significant growth, driven by several methodologies which enable the training of deep neural networks (DNNs) in a scalable way and by development of more powerful hardwares. It is observed that increased capacity of DNN effectively has improved the performance. For example, AmoebaNet-B \[23\] scaled with GPipe \[11\] has 557 million parameters and has achieved top-1 accuracy 84.4% which was state-of-the-arts result at the time, and GPT-2 \[22\] is a Transformer-based \[28\] language model which has 1.5 billion parameters (see Figure 1 of \[11\] for the effect of model scaling). However, training such a massive model is very resource intensive. One can mitigate this issue by reducing the size of the model without losing the performance by pruning the model \[8, 1\], designing more efficient architectures \[10, 27\], architecture search under resource constraints \[3\], and many more.

We may wonder a rather direct approach is possible: can we train a massive model fast enough, given a large pool of devices? One obstacle is that common optimization techniques to train a neural network are sequential in nature. Those algorithms repeatedly compute the gradient of the loss with respect to the given mini-batch at a time and update the model parameters using the gradient. With abundant computational resource, data parallelism \[17\] is commonly used to speed up the overall optimization procedure by dividing the mini-batch into micro-batches and delegating per micro-batch computation to available devices. With careful hyperparameter tuning, this effectively reduce the training time up to a certain size of mini-batch which may depend on model, optimization algorithm, and data \[6, 25\].

One drawback of data-parallel training is that devices hold their own version of network for executing the subdivided task, and network parameters must be synchronized after each parameter update. This may induce heavy communication load when there are lots of parameters to synchronize.

Note that data parallelism is not applicable when the model is so big that it is impossible to compute gradient even when a single data point is fed into the network. Model parallelism \[5\] is a method for training such a massive model, which partitions the model into several pieces and places them on different devices. Each device only computes a small part of the model, and updates only the parameters in that part. However, model parallelism suffers from its underutilization behavior. Since most neural networks consist of sequence of layers, the device holding the later part of the model must wait until computation in devices holding earlier parts of the model.

Another possible solution is to use gradient checkpointing \[4\] which saves memory by only storing the subset of activation maps and re-computing the discarded activation maps when necessary. Obviously, this requires certain part of the model be computed twice and overall training time would be increased.

It is benefitting to combine different types of parallelization strategies \[16, 14, 26, 12, 9, 11, 7\], and recent lines of research questions how to find an optimal strategy.
among them, pipeline parallelism a way to accelerate neural network training by combining model parallelism with data pipelining, either in synchronous way as in GPipe [11] or in asynchronous way as in [12], PipeDream [9], and XPipe [7]. We remark that gradient checkpointing (also called re-materialization) is further combined in GPipe to allow training even bigger models.

In this paper, we design and implement torchgpipe, a ready-to-use library for GPipe in PyTorch [21]. In particular, we develop a set of design components for optimized pipeline-parallel computations in PyTorch’s define-by-run and eager execution environment. We show that each component is necessary to fully benefit from pipeline parallelism in such environment, and demonstrate the efficiency of torchgpipe by conducting the speed and memory benchmarks on AmoebaNet-D [23] and U-Net [24] when trained with the library.

The rest of the paper is organized as follows. In Section 2, we discuss how the forward and backward passes can be decomposed into subtasks (under certain assumptions), describe the device placement strategy of micro-batch pipeline parallelism, and demonstrate what the desired order of execution per device is. In Section 3, we discuss complications for achieving the optimal timeline of pipeline parallelism in PyTorch and explain how torchgpipe resolves them. Additionally, we relax the assumption that the model is sequentially composed, and provide a way for expressing models with long skip connections so that pipeline parallelism still applies without giving up the efficiency. Then, we demonstrate that the optimization components suggested in the paper are essential for the performance, and evaluate the performance of the proposed library in Section 4.

2. Pipeline Parallelism

Suppose that we have a neural network which is represented as a composition of sequence of subnetworks. Let us denote the subnetworks by $f^1, \cdots, f^n$ with parameters $\theta^1, \cdots, \theta^n$ and let the full network be

$$f = f^n \circ f^{n-1} \circ \cdots \circ f^1,$$

parameterized by $\theta = (\theta^1, \cdots, \theta^n)$. For clarity, we call $f^j$ the $j$th partition of $f$ and assume that the parameters of partitions are mutually disjoint.

When training the network, gradient-based methods such as stochastic gradient descent requires computing the outcome $f(x)$ of the network given a mini-batch $x$ of training data and the corresponding loss, and the gradient $\partial_x$ of the loss with respect to the network parameter $\theta$. Those two stages are called forward and backward pass, respectively.

Since $f$ is sequentially composed, in forward pass $f(x)$ can be computed by letting $x^1 = x$ and sequentially applying the partitions as $x^j = f^j(x^{j-1})$ for $j = 1, \cdots, L$.

Furthermore, if $x$ consists of $m$ smaller batches $x_1, \cdots, x_m$ called micro-batches, computing $f(x)$ dissolves into tasks $F_{i,j}$ where $x^j_i = x_i$ and

$$x^j_i \leftarrow f^j(x^{j-1}_i) \quad (F_{i,j})$$

for $i = 1, \cdots, m$ and $j = 1, \cdots, n$, assuming that $f$ does not involve any intra-batch computation. One prominent exception for this is batch normalization [13]. The loss is obtained by aggregating $x^m_i = f(x_i)$ and evaluating the loss function on them.

In a similar fashion, backward pass is decomposed into tasks $B_{i,j}$ where $dx^j_i$ is the gradient of the loss with respect to $x^j_i$ and

$$dx^{j-1}_i \leftarrow \frac{\partial x f^j(dx^j_i)}{dx} \quad (B_{i,j})$$

for $i = 1, \cdots, m$ and $j = 1, \cdots, n$. Here

$$\frac{\partial x f^j}{\partial x} : v \mapsto v^T \cdot \frac{df^j}{dx} \bigg|_{x = x^{j-1}}$$

is a function which does backward propagation (also known as vector-Jacobian product) through the partition $f^j$, and $\partial_{x^j} f^j$ is defined likewise. As a result, we get the gradient of the loss with respect to $\theta_i$ by summing $g^j_i$ over $i$’s.

Note that there are data dependencies between tasks. For example, $F_{i,j}$ requires $x^{j-1}_i$ which is only available after $F_{i,j-1}$, hence $F_{i,j-1}$ must be completed before starting $F_{i,j}$ and the same applies for $B_{i,j}$ and $B_{i,j+1}$. Figure 1 shows the full dependency graph in the case of $m = 4$ and $n = 3$.

Given the set of tasks $\{F_{i,j}\}$ and $\{B_{i,j}\}$ and a pool of devices which can work in parallel, different parallelization strategies have their own rule to assign tasks to devices. Each device computes one or more assigned tasks as soon as the dependencies are resolved. In the setting above, all dependencies are among the tasks with the same micro-batch index $i$. Hence, one can effectively parallelize the tasks by assigning tasks with different micro-batch indices to different devices — which is data parallelism.

2.1. Dependency Graph of GPipe

Pipeline parallelism’s strategy is to assign tasks with respect to the partition index $j$ so that $j$th partition entirely lies in the $j$th device. In addition to this, it is enforced that $F_{i,j}$ must be completed before executing $F_{i,j+1}$ and $B_{i,j}$ must be completed before executing $B_{i,j+1}$.

In addition to the micro-batch pipelining, GPipe [11] further reduces the memory requirement by utilizing gradient checkpointing for each $B_{i,j}$. Since $j$th device executes $B_{i,j}$

\[1\text{Applying pipeline parallelism to a network with batch normalization is feasible while the computation is not identical anymore. Indeed, this discrepancy also exists in data-parallel training scheme and it may results in degradation of the result.} \]
one at a time, only the activation maps obtained from $F_{i,j}$ are needed to complete $B_{i,j}$. By recomputing the forward pass $F_{i,j}$ right before executing $B_{i,j}$, memory consumption is reduced by a factor of $m$. Moreover, the re-computation can take place while the device is waiting for $B_{i,j+1}$ being done. This is summarized in Figure 2, where dashed arrows denotes the execution order between independent tasks induced by the micro-batch order, and $F'_{i,j}$ denotes the re-computation of $F_{i,j}$.

We remark that re-computations for the last micro-batch, i.e., $F'_{m,j}$ for $j = 1, \cdots, n$ are unnecessary. This is because that on $j$th device the last task in the forward pass is $F_{m,j}$, so discarding intermediate activations of it in forward pass and re-computing them in the beginning of backward pass has no effect of reducing memory, only slowing down the pipeline. For this reason, $F'_{m,j}$ is omitted from the graph.

2.2. Device-wise Execution Order

To summarize, in pipeline parallelism (with checkpointing) each device is assigned with a set of tasks with the prescribed order. Each device will execute the given tasks one-by-one as soon as cross-device dependencies are met. However, there is a missing component in this picture — data tranfer between the devices. For illustration, the full execution order that device $j$ must follow is shown in Figure 3. Here data transfer operations are explicitly denoted as ‘receive’ and ‘send’ for emphasis.

3. torchgpipe: A PyTorch Library for GPipe

torchgpipe is a PyTorch library for micro-batch pipeline parallelism with checkpointing, as known as GPipe. The library provides a simple way to apply GPipe to a generic sequential module written in PyTorch. The usage of torchgpipe resembles that of the data parallel module of PyTorch — just wrap your model with the wrapper.

Users must specify the number of micro-batches $m$ and how consecutive layers form $n$ partitions. Here we remark that even though we simplified our assumption to that the model is a sequence of partitions, it is strictly required in torchgpipe that the model is a sequence of $\textit{layers}$ to give flexibility for users how to split the model. torchgpipe will assume that each layer is a non-divisible, black-box, and referentially transparent\footnote{This is required especially for checkpointing: referential transparency ensures that recomputation is identical to the computation done in the forward pass.} algorithm.

---

**Figure 1:** Minimal dependency graph for forward and backward pass.

**Figure 2:** Dependency graph for pipeline parallelism with checkpointing. Colors denote the devices that tasks are computed in.

**Figure 3:** The execution order that $j$th device must follow.
For convenience, the library provides the submodule `torchgpipe.balance` which computes a partition whose pairwise resource discrepancy is small, where resource consumption is computed by profiling. Specifically, we used the algorithm from [2].

As `torchgpipe` is built on PyTorch equipped with CUDA backend, we will often assume that devices are NVIDIA GPU throughout this section. Nevertheless, the underlying principle of the library applies in general for implementing pipeline parallelism any eager execution environments.

### 3.1. Complications in PyTorch

Our primary concern is efficiency. As we discussed in Section 2.2, in order for pipeline parallelism to work as desired, the tasks must be assigned to each device in the correct order. There are several complications to achieve this in PyTorch.

First of all, kernels are issued to each device on-the-fly due to PyTorch’s define-by-run style and its eager execution behavior (as opposed to in construct-and-run type frameworks). Hence, one must design the host code carefully so not only that device-bound tasks are issued in the correct order within each device, but also that execution of the tasks on devices (asynchronous to CPU) are not delayed due to the Python interpreter failing to request it ahead of the time. This kind of delay may happen when some of the tasks are CPU-intensive or involve a lot of cheap kernel calls. As a solution, `torchgpipe` introduces deterministic clock-cycle which gives the total ordering of the tasks.

Secondly, the computation graph for backward pass is constructed dynamically during the forward pass in PyTorch. In other words, “it avoids ever materializing a “forward graph”, recording only what is necessary to differentiate the computation.” [21] Since PyTorch does not record the forward computation graph nor maintain a gradient tape, the automatic differentiation (autograd) engine of PyTorch does back-propagation solely with respect to the graph. It implies that autograd engine may not run exactly in the reverse order of execution as in the forward pass, unless enforced by the structure of the graph. To deal with this, we develop a pair of primitive functions called ‘fork’ and ‘join’ to create explicit dependencies on the fly in the backward computation graph.

Thirdly, communication between several devices can cause two-way synchronization, if not carefully managed. This may cause under-utilization since sender may wait to synchronize with the receiver even when there is no explicit dependency between the copy and next task in queue, or vice versa. `torchgpipe` avoids this issue by using non-default CUDA streams so that copies would never block computations unless the computation must wait for the data.

Lastly, `torchgpipe` attempts to relax the restriction of micro-batch pipeline parallelism that model must be sequential. Although any neural network can be written in a sequential form in principle, this requires knowing the entire computation graph ahead of the time which is not the case in PyTorch. In particular, if there is a tensor which skips from a layer in device $j'$ to another layer in device $j > j' + 1$, the tensor will be copied to all devices in between since `torchgpipe` cannot know it ahead. To circumvent this issue, we design an interface to signify which intermediate tensors are skipped and which layers use them.

### 3.2. Optimization Components

In the remainder of this section, it is explained how the components of `torchgpipe` are designed and why each of them is essential for performance.

#### 3.2.1 Forward Dependency: Deterministic Clock-cycle

As we discussed in Section 3.1, the total ordering of tasks is determined by the host code in the forward pass. Each device implicitly understands the dependency between tasks by the order they are assigned by CPU. Ideally, if tasks could be assigned to devices with no cost, CPU may assign tasks to devices in any order as long as the ordering within device is correct. However, this assumption is not realistic enough, as launching kernels on a GPU is not free for CPU, memory transfer between GPUs may require synchronization, or a task is CPU-intensive. For this reason, we minimize the delay coming from CPU by sorting all tasks by the distance to $F_{1,1}$.

**Algorithm 1: Deterministic clock-cycle**

```plaintext
for k from 1 to m + n - 1 do
    for i, j such that $i + j - 1 = k$ do
        if $j > 1$ then
            Copy $x_{i,j}^{l-1}$ to device j.
        for i, j such that $i + j - 1 = k$ do
            Execute $F_{i,j}$.
```

We call this deterministic clock-cycle (Algorithm 1). In the algorithm, CPU executes the clock cycles starting from the counter $k = 1$ to $k = m + n - 1$. In $k$th clock cycle, all copy kernels for data needed to execute tasks $F_{i,j}$ where $i + j - 1 = k$ are first issued, and then the computation kernels for executing the tasks are registered to corresponding devices (which can be safely multithreaded since tasks in the same clock cycle are independent).

#### 3.2.2 Backward Dependency: Fork and Join

Suppose now that we run a forward pass according to the deterministic clock-cycle. The resulting computation graph
for backward will look rather like 1 than 2, even when the forward tasks $F_{i,j}, \ldots, F_{m,j}$ on device $j$ were executed in order. From such a graph, autograd engine of PyTorch would never know that $B_{i+1,j}$ must be executed before $B_{i,j}$, and this messes up the timeline of the backward pass. For this reason, virtual dependencies (dashed arrows in Figure 2) must be explicitly drawn during the forward pass.

We design a pair of primitive functions called Fork and Join to express such dependency. Basically, Fork is the autograd function mapping a tensor $x$ to the pair $(x, \emptyset)$ where $\emptyset$ is an empty tensor\(^3\); and Join is the autograd function mapping a pair $(x, \emptyset)$ to the tensor $x$. Now, dependency of $F_{i+1,j}$ upon $F_{i,j}$ (which translates to the dependency of $B_{i+1,j}$ upon $B_{i,j}$ in the backward computation graph) can be expressed as

$$
(x^i_j, \emptyset) \leftarrow \text{Fork}(x^i_j)
$$

$$
x^{j-1}_{i+1} \leftarrow \text{Join}(x^{j-1}_{i+1}, \emptyset).
$$

See Figure 4 for illustration.

\(^3\)In principle, the tensor which indicates the virtual dependency can be arbitrary. We chose to use the empty tensor for this, however, to remove any unnecessary computation caused by the tensor such as gradient accumulation in PyTorch.

### 3.2.3 Concurrent Copy and Computation: Streams

PyTorch issues every device-bound kernels to the default stream, unless it is specified otherwise. Stream is a device-bound sequence of kernels that is executed in order. Kernels in the same stream are guaranteed to be executed in the prescribed order, but kernels in different streams can be interleaved, and even can overlap when possible. In particular, nearly all CUDA devices with compute capability 1.1 and higher support concurrent copy and execution: data transfer between devices can always overlap with kernel execution (see section 4.5.1.5 of [20]).

torchpipe registers every copy kernel to non-default streams while keeping computation kernels on the default stream. This allows the device $j$ processing $F_{i,j}$ in concurrent with sending $x^j_{i-1}$ to the device $j+1$ and/or receiving $x^{j-1}_{i}$ from the device $j-1$. Moreover, each device uses different streams for each micro-batch. Since there is no true dependency between different micro-batches, this use of streams is safe and this allows copies to occur as fast as possible. See Figure 5 for illustration.

### 3.2.4 Autograd Functions with Shared Memory

So far in this section, we did not discuss how to schedule re-computation tasks $F'_{i,j}$ when gradient checkpointing is in use. It must be scheduled in prior to the back-propagation task $B_{i,j}$ upon completion of $B_{i+1,j}$. This must be encoded in the computation graph as well for autograd engine. Indeed, PyTorch supports such functionality via an in-house autograd function for checkpointing.

Checkpoint in PyTorch is implemented by defining an autograd function which computes as usual function in the forward pass without storing intermediate activation maps but the inputs. In the backward pass, this function constructs a local computation graph for backward by recomputing the function using the stored inputs, and computes gradients by back-propagating through the local graph. However, this tightly binds $F'_{i,j}$ and $B_{i,j}$ together. Ultimately, we would like to insert the instruction for waiting

![Figure 4: The backward computation graph with Fork and Join. Different colors correspond to different devices. Arrows are drawn according to the direction in backward computation graph and these relations are constructed during the forward pass. Here the virtual dependency of $F'_{i,j}$ on $B_{i+1,j}$ is created via Fork and Join, which is illustrated by dashed arrows.](image)

![Figure 5: Timeline of device $j$ with or without non-default streams for copy. (a): If only default streams are used, copy kernels may block computation kernels (and vice versa) until the copy is completely finished. (b): With copy streams, computation can happen in concurrent with sending or receiving data from other devices.](image)
the result $dx_j^i$ of $B_{i,j+1}$ to be copied from device $j+1$ to device $j$ in between $F_{i,j}^j$ and $B_{i,j}$, to allow that $F_{i,j}^j$ and the copy happens concurrently.

For such a fine-grained order control, torchgpipe implements checkpointing with two separate autograd functions Checkpoint and Recompute. At the execution time of the task $F_{i,j}$, a pair of Checkpoint and Recompute which have a shared memory is generated. This shared memory is used in the backward pass for transferring the local computation graph made by executing Recompute to Checkpoint for back-propagation. By arranging the functions so that $F_{i,j}^j$, synchronization for receiving $dx_j^i$, and $B_{i,j}$ are executed in the order during the backward pass, it is ensured that re-computation and copy can happen concurrently.

3.3. Dealing with Non-sequential Models

In Section 2, we assumed that the model $f$ is composed of partitions $f^1, \ldots, f^n$ in sequence. In principle, any neural network can be represented in this form by sorting all nodes in the forward computation graph of $f$ in topological ordering. Hence, pipeline parallelism is applicable to any model.

However, consider a symptomatic case that all the partitions except the first and the last one are parallel, i.e.,

$$f(y) = g^n(x^2, \ldots, x^{n-1})$$

where $x^1 = g^1(x)$ and $x^j = g^j(x^1)$ for $j=2, \ldots, n-1$. In a sequential form, this is equivalent to $f = f^n \circ \cdots \circ f^1$ such that

$$f^n(x^1, x^2, \ldots, x^{n-1}) := g^n(x^2, \ldots, x^{n-1}),$$

$$f^j(x^1, \ldots, x^{j-1}) := (x^1, \ldots, x^{j-1}, f^j(x^1))$$

for $j = 2, \ldots, n-1$, and $f^1 = g^1$. In this case, it is quite inefficient to use pipeline parallelism in its native form since at the boundary of device $j-1$ and $j$, the tuple $(x^1_i, \ldots, x^{j-1}_i)$ must be copied instead of a single tensor $x^j_i$ which is the only required data to compute $j$th partition.

torchgpipe provides a submodule which allows users to indicate skipping tensors from which layer to which layer: torchgpipe.skip. With the decorator @skippable, user-defined layer can stash a tensor for later or pop a stashed one via yield operator in Python without returning it. This in particular does not change the input and output signature of a layer. Hence, minimal effort is needed for adding skip connection to a preexisting sequential model.

3.3.1 Hiding Skip Tensors in the Graph: Portals

Adding skip connections into the dependency graph (Figure 2) is fairly straightforward. Indeed, no additional dependency would be introduced no matter how many skip connections are added, hence only the copy kernels for skip connections need extra care. In torchgpipe, this is taken care by portals consisting of three autograd functions PortalBlue, PortalOrange, and PortalCopy sharing memory, like Checkpoint and Recompute in Section 3.2.4. Each does the job of saving the skip tensor, loading the tensor, and moving the saved tensor to the skipped device, respectively (and vice versa in the backward pass). This mechanism is illustrated in Figure 6.

4. Experiments

Every experiment was conducted with NVIDIA Tesla P40 GPUs with CUDA 10.1.243, each having 22 GiB of memory. For reproducibility, codes for all benchmarks provided in this section is made available in the repository^4.

4.1. Effects of Optimization Components

We conducted an experiment to show that every component of torchgpipe is necessary to achieve the maximal efficiency. Starting from the baseline which only has deterministic clock-cycle but no others, each component (backward dependency via Fork and Join, non-default streams for copy kernels, and portals for skip connections) is added.

^4Further details available at this link.

---

(a) Without portals

(b) With portals

![Figure 6: The flow of skip connection with or without portals. (a): Without portals, skipped tensor from device 1 is copied to device 2 and subsequently to device 3. (b): With portals, the tensor is directly copied to device 3. The gradient flows in the exact reverse direction in the backward pass.](image-url)
Table 1: Performance of torchgpipe when optimization components are incrementally added. The U-Net model with \((B,C) = (5,64)\) is used for the experiment. The batch size and the number of micro-batches are fixed as 128 and 8, respectively. The model is partitioned and placed on four devices via torchgpipe. Here the partition was found manually with the aid of torchgpipe.balance.

| Optimization components | Throughput | Speed up | Utilization | Memory usage |
|-------------------------|------------|----------|-------------|--------------|
| × × ×                   | 30.662/s   | 1        | 44%         | 52.2 GiB     |
| Dependency × ×          | 41.306/s   | 1.347    | 59%         | 19.1 GiB     |
| Dependency Streams ×    | 55.191/s   | 1.800    | 71%         | 30.0 GiB     |
| Dependency Streams Portals | 58.477/s | 1.907    | 75%         | 23.5 GiB     |

Figure 7: Detailed view of CUDA timeline for each setting in Table 1, profiled with NVIDIA Nsight Systems 2019.5.1.58. Starting from the top, adjacent lanes with blue bars and red bars visualize the timeline per device. Blue bars represent computation kernels while red bars represent device-to-device copy (length proportional to time).

incrementally. We report the throughput, GPU utilization, and memory usage under each setting to measure how each component contributed to the performance of torchgpipe. We find that addition of each component gives a speed-up, and with all components torchgpipe runs nearly twice as fast as the baseline. Results can be found in Table 1.

We used U-Net for the experiment. Details of the architecture can be found in Section 4.2.2 and we set \((B,C)\) to be \((5,64)\) as in the speed benchmark. In settings without portals, the model is implemented as a fully sequential version where skip connections are encoded as inputs and outputs of layers that they pass through, as described in the symptomatic example of Section 3.3. For the setting with all components, it is implemented with torchgpipe.skip while the architecture is identical.

We also visualized per GPU timelines to help understanding each component’s role, illustrated in Figure 7. Explanation for each picture is summarized as follows.

(a) By deterministic clock-cycle, all kernels are issued in the correct order during forward pass. It is illustrated by the left part of the timeline. However, without explicit dependency encoded in the computation graph, the autograd engine processes the micro-batches in an uncontrollable order so the timeline is messed up.

(b) With backward dependency, kernels are now issued in the correct, deterministic order in backward pass.

(c) By using non-default copy streams, copies and computations are now concurrent as illustrated by overlapping blue and red bars.

(d) Portals remove unnecessary copies caused by transferring the skipping tensor to all devices in between. This is illustrated by that the length of red bars are reduced compared to (c).

4.2. Performance Benchmarks

To demonstrate the efficiency of torchgpipe, we report performance benchmarks similar to that conducted by GPipe [11].

4.2.1 AmoebaNet-D Speed Benchmark

We measured the throughput of AmoebaNet-D with various number of devices. For this, we measured the throughput of the model when torchgpipe is applied, with \(n\) partitions and \(m\) micro-batches. Here throughput means the number of samples processed per second.

The experiment is conducted for each pair \((m,n)\) where \(m \in \{1,4,32\}\) and \(n \in \{2,4,8\}\). When \(m = 1\), we used
checkpointing to all micro-batches\(^5\) to make a fair comparison of loss due to checkpointing with [11]. The model we used is our implementation of a sequential version of AmoebaNet-D in PyTorch.\(^6\)

The model is trained by plain SGD for 10 epochs and reported the average throughput over the epochs except the first one. To exclude the overhead caused by data loading, we used a synthesized dataset which consists of 10,000 images whose dimension is \(3 \times 224 \times 224\). For each setting, the batch size and the number of micro-batches are chosen to maximize the throughput. Relative speed-up is calculated against the baseline case \((m, n) = (1, 2)\) and reported in Table 2. We included the speed-up of GPipe for comparison.

The relative speed-up of torchgpipe shows similar trend to that of GPipe. We remark that differences in performance reported in Table 2 might be due to many unknown factors such as balance of the partitions, discrepancy between the implementation, difference in devices, and so on.

### 4.2.2 U-Net Memory Benchmark

To evaluate the effectiveness of torchgpipe for models with long skip connections, we used U-Net [24] for 2-dimensional segmentation. The version of U-Net we used has five down-sampling layers and five up-sampling layers, and two hyper-parameters \(B\) and \(C\) determining the size of the model. Here \(B\) stands for the number of convolution blocks in between down-sampling layers, and \(C\) stands for the number of output channels of the first convolution. Channels are doubled after each down-sampling layers (or halved after each up-sampling layers, respectively). Our implementation of U-Net is rather symmetric than the original model proposed in [24] for effective balancing.

We conducted an experiment to measure the ability of torchgpipe for training a bigger model. For 1, 2, 4 and 8 GPUs, we found maximum \((B, C)\) to occupy each number of devices. In all settings, the input size is set to \(3 \times 192 \times 192\), the output size to \(1 \times 192 \times 192\), and the batch size to 32. The total memory usage for training each model is reported in Table 3. Here parameters consumes 8 bytes each for itself and its gradients.

### 4.2.3 U-Net Speed Benchmark

We also measured the throughput of U-Net with various number of devices. Naive-1 denotes the baseline without pipeline parallelism nor checkpointing, and Pipeline-1, -2, -4, -8 denotes that the model is trained with torchgpipe

with the corresponding number of partitions. The hyper-parameters determining the size of U-Net is set to \((B, C) = (5, 64)\) in this experiment. The batch size, the number of micro-batches \((m)\), and the balance to partitions are chosen to maximize the throughput. For each setting, throughput is measured as in Section 4.2.1 except that the image size was \(3 \times 192 \times 192\) in this experiment. Result is summarized in Table 4.

### 5. Conclusion

In this paper, we introduced torchgpipe, a ready-to-use library in PyTorch for micro-batch pipeline parallelism with checkpointing proposed by GPipe [11]. This library is designed and implemented in PyTorch’s define-by-run and eager execution environment. Ablation study and performance benchmarks presented in Section 4 demonstrate that all components of torchgpipe are essential to endeavor the desired advantages of pipeline parallelism with checkpointing in eager execution environment. We believe that general principles we established in the paper apply to any other frameworks with eager execution environment.

We tried to avoid going too deep into technical details involved in torchgpipe. Our code is available at https://github.com/kakaobrain/torchgpipe for those who are interested in further details, and those who want to apply pipeline parallelism to their model in PyTorch.
References

[1] Jose M Alvarez and Mathieu Salzmann. Learning the number of neurons in deep networks. In Advances in Neural Information Processing Systems, pages 2270–2278, 2016.

[2] Imre Bárany and Victor S Grinberg. Block partitions of sequences. Israel Journal of Mathematics, 206(1):155–164, 2015.

[3] Han Cai, Ligeng Zhu, and Song Han. ProxylessNAS: Direct neural architecture search on target task and hardware. In International Conference on Learning Representations, 2019.

[4] Tianqi Chen, Bing Xu, Chiyuan Zhang, and Carlos Guestrin. Training deep nets with sublinear memory cost. arXiv preprint arXiv:1604.06174, 2016.

[5] Jeffrey Dean, Greg Corrado, Rajat Monga, Kai Chen, Matthieu Devin, Mark Mao, Marc’Aurelio Ranzato, Andrew Senior, Paul Tucker, Ke Yang, et al. Large scale distributed deep networks. In Advances in neural information processing systems, pages 1223–1231, 2012.

[6] Priya Goyal, Piotr Dollár, Ross Girshick, Pieter Noordhuis, Lukasz Wesolowski, Aapo Kyrola, Andrew Tulloch, Yangqing Jia, and Kaiming He. Accurate, large minibatch sgd: Training imagenet in 1 hour. arXiv preprint arXiv:1706.02677, 2017.

[7] Lei Guan, Wotao Yin, Dongsheng Li, and Xicheng Lu. Xpipe: Efficient pipeline model parallelism for multi-gpu dnn training. arXiv preprint arXiv:1911.04610, 2019.

[8] Song Han, Jeff Pool, John Tran, and William Dally. Learning both weights and connections for efficient neural network. In Advances in neural information processing systems, pages 1135–1143, 2015.

[9] Aaron Harlap, Deepak Narayanan, Amar Phanshishey, Vivek Seshadri, Nikhil Devanur, Greg Ganger, and Phil Gibbons. Pipedream: Fast and efficient pipeline parallel dnn training. arXiv preprint arXiv:1806.03377, 2018.

[10] Andrew G Howard, Menglong Zhu, Bo Chen, Dmitry Kalenichenko, Weijun Wang, Tobias Weyand, Marco Andreetto, and Hartwig Adam. Mobilenets: Efficient convolutional neural networks for mobile vision applications. arXiv preprint arXiv:1704.04861, 2017.

[11] Yanning Huang, Youlong Cheng, Ankur Bapna, Orhan Firat, Dehao Chen, Mia Chen, HyoukJoong Lee, Jiquan Ngiam, Quoc V Le, Yonghui Wu, et al. Gpipe: Efficient training of giant neural networks using pipeline parallelism. In Advances in Neural Information Processing Systems, pages 1097–1105, 2012.

[12] Zhihao Jia, Sina Lin, Charles R. Qi, and Alex Aiken. Exploring hidden dimensions in accelerating convolutional neural networks. In Jennifer Dy and Andreas Krause, editors, Proceedings of the 35th International Conference on Machine Learning, volume 80 of Proceedings of Machine Learning Research, pages 2274–2283, Stockholmsmssan, Stockholm Sweden, 10–15 Jul 2018. PMLR.

[13] Sergey Ioffe and Christian Szegedy. Batch normalization: Accelerating deep network training by reducing internal covariate shift. In Francis Bach and David Blei, editors, Proceedings of the 32nd International Conference on Machine Learning, volume 37 of Proceedings of Machine Learning Research, pages 448–456, Lille, France, 07–09 Jul 2015. PMLR.

[14] Zhihao Jia, Sina Lin, Charles R. Qi, and Alex Aiken. Exploring hidden dimensions in accelerating convolutional neural networks. In Jennifer Dy and Andreas Krause, editors, Proceedings of the 35th International Conference on Machine Learning, volume 80 of Proceedings of Machine Learning Research, pages 2274–2283, Stockholmsmssan, Stockholm Sweden, 10–15 Jul 2018. PMLR.

[15] Zhihao Jia, Matei Zaharia, and Alex Aiken. Beyond data and model parallelism for deep neural networks. In The Conference on Systems and Machine Learning (SysML), 2019.

[16] Alex Krizhevsky. One weird trick for parallelizing convolutional neural networks. arXiv preprint arXiv:1404.5997, 2014.

[17] Alex Krizhevsky, Ilya Sutskever, and Geoffrey E Hinton. Imagenet classification with deep convolutional neural networks. In Advances in neural information processing systems, pages 1097–1105, 2012.

[18] Azaíla Mirhoseini, Anna Goldie, Hieu Pham, Benoit Steiner, Quoc V. Le, and Jeff Dean. A hierarchical model for device placement. In International Conference on Learning Representations, 2018.

[19] Azaíla Mirhoseini, Hieu Pham, Quoc V Le, Benoit Steiner, Rasmus Larsen, Yuefeng Zhou, NAVen Kumar, Mohammad Norouzi, Samy Bengio, and Jeff Dean. Device placement optimization with reinforcement learning. In Proceedings of the 34th International Conference on Machine Learning-Volume 70, pages 2430–2439. JMLR. org, 2017.

[20] NVIDIA. NVIDIA CUDA programming guide 1.1. (link), 2007.

[21] Adam Paszke, Sam Gross, Soumith Chintala, Gregory Chanan, Edward Yang, Zachary DeVito, Zeming Lin, Alban Desmaison, Luca Antiga, and Adam Lerer. Automatic differentiation in PyTorch. In NIPS Autodiff Workshop, 2017.

[22] Alec Radford, Jeffrey Wu, Rewon Child, David Luan, Dario Amodei, and Ilya Sutskever. Language models are unsupervised multitask learners.

[23] Esteban Real, Alok Aggarwal, Yannping Huang, and Quoc V Le. Regularized evolution for image classifier architecture search. In Proceedings of the AAAI Conference on Artificial Intelligence, volume 33, pages 4780–4789, 2019.

[24] Olaf Ronneberger, Philipp Fischer, and Thomas Brox. U-net: Convolutional networks for biomedical image segmentation. MICCAI, Springer, LNCS, 9351:234–241, 2015.

[25] Christopher J Shallue, Jaehoon Lee, Joe Antognini, Jascha Sohl-Dickstein, Roy Frostig, and George E Dahl. Measuring the effects of data parallelism on neural network training. arXiv preprint arXiv:1811.03600, 2018.

[26] Noam Shazeer, Youlong Cheng, Niki Parmar, Dustin Tran, Ashish Vaswani, Penporn Koanantakool, Peter Hawkins, HyoukJoong Lee, Mingsheng Hong, Cliff Young, et al. Mesh-tensorflow: Deep learning for supercomputers. In Advances in Neural Information Processing Systems, pages 10414–10423, 2018.

[27] Mingxing Tan and Quoc Le. Efficientnet: Rethinking model scaling for convolutional neural networks. In International Conference on Machine Learning, pages 6105–6114, 2019.
[28] Ashish Vaswani, Noam Shazeer, Niki Parmar, Jakob Uszkoreit, Llion Jones, Aidan N Gomez, Łukasz Kaiser, and Illia Polosukhin. Attention is all you need. In Advances in neural information processing systems, pages 5998–6008, 2017.

[29] Yanqi Zhou, Sudip Roy, Amirali Abdolrashidi, Daniel Wong, Peter C Ma, Qiumin Xu, Ming Zhong, Hanxiao Liu, Anna Goldie, Azalia Mirhoseini, et al. Gdp: Generalized device placement for dataflow graphs. arXiv preprint arXiv:1910.01578, 2019.