On the Separate Extraction of Self-Heating and Substrate Effects in FD-SOI MOSFET

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Abstract—This paper proposes an original approach to separately characterize self-heating and substrate effects in Fully-Depleted Silicon-on-Insulator (FD-SOI) devices. As both dynamic self-heating and drain to source coupling through the back-gate and substrate of an FD-SOI MOSFET induce a frequency transition in the Y-parameters in a common frequency range, it is crucial to properly separate them for further modeling. The proposed novel method is based on the extraction of the back-gate and substrate networks from the S-parameters measured at the zero-temperature coefficient bias. It enables the accurate and unambiguous extraction of thermal impedance for different biases, thus providing the extraction of the device thermal resistance and capacitance for different power levels from S-parameters measurements.

Index Terms—Back-gate modeling, FD-SOI MOSFET, RF extraction, self-heating, S-parameters measurements, substrate coupling, ultra-wideband modeling.

I. INTRODUCTION

The downscaling of CMOS technology has been crucial for improving device performance and reducing manufacturing cost. However, aggressive scaling results in higher current and power densities, thereby increasing the self-heating (SH) effect and the lattice temperature ($T_c$). Fully-Depleted Silicon-on-Insulator (FD-SOI) transistors offer outstanding electrostatic control, very low mismatch, excellent analog and RF figures of merit [1]–[4]. However, due to the presence of the buried oxide (BOX), SH of more significance is present in FD-SOI MOSFETs than in their bulk counterparts [5]. Dynamic self-heating is known to induce a transition in the Y-parameters over frequency that is used in turn to extract the thermal parameters [5]–[13]. Furthermore, the drain to source coupling through the back-gate (B-G) node (or Si substrate under the BOX) also induces a transition in the Y-parameters in a similar frequency range [9], [14]. Although this transition was originally very pronounced in FD-SOI devices with thin BOX [9] contrarily to previous device generations [14], the introduction of a highly-doped region below the BOX strongly reduces the transition [5]. The transition associated to the coupling via substrate is thus usually neglected/ignored in these devices, which may however lead to misinterpretation and erroneous modeling of SH [5], [10]. To the best of the authors’ knowledge, no method has been proposed to separately characterize each contribution, i.e. SH and B-G effect (also called substrate effect, SE), into Y-parameter frequency response. In this paper, we will (i) demonstrate that the SE partially overlaps SH forming a common, indistinguishable distributed transition from 100 kHz to 10 GHz, (ii) show that the dynamic SH effect vanishes at the zero-temperature coefficient (ZTC) bias point, (iii) use this bias point to extract the SH-free transistor electrical model including the B-G and substrate nodes, (iv) extract the frequency-dependent thermal impedance $Z_{th}(f)$ for different bias conditions, and (v) compare it to the conventional extraction procedure that neglects the transitions associated to the B-G node.

II. SELF-HEATING AND BACK-GATE NODE EXTRACTION

A. Advantage of ZTC Bias for Unambiguous Extraction

An FD-SOI super-low threshold voltage nMOSFET from 22FDX® [2] featuring a gate length of 20 nm, finger width of 0.5 μm, 20 fingers and a multiplicity of 6 for a total width of 60 μm is studied. Its S-parameters are measured on-wafer from 100 kHz to 10 GHz using a vector network analyzer from Keysight, coupled with a probe station hosting a thermal chuck for additional dc I-V measurements at 300, 320, 335, 350, 370 and 390 K. The back-gate voltage ($V_{bg}$) is set to 0 V. The RF MOSFETs are probed using a Ground-Signal-Ground (GSG) configuration. A Short-Open-Load-Thru (SOLT) calibration is performed and dedicated open and short structures are measured to de-embed the transistor measurements down to the first metal layer.

The conventional method to extract SH parameters from S-parameter measurements [6]–[8] relies on the fact that the lattice temperature is able to follow a “slowly” (w.r.t. its thermal time constant) varying ac signal, but ceases to follow the ac signal if it is too “fast”, leading to a step between the low and high frequency values of $Y_{dd}$ ($Y_{22}$) and $Y_{dg}$ ($Y_{21}$). This so-called dynamic SH effect has been rigorously put into equations for a general two-port device in [11]. In our case, the equations simplify into:

\[ Y_{dd} = Y_{ddT} + Z_{th} \frac{dI_d}{dT_A} (Y_{dgt} V_d + I_d), \]  
\[ Y_{dg} = Y_{dgT} + Z_{th} \frac{dI_g}{dT_A} Y_{dgt} V_d \]  

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biased at \( V_d \) genic temperatures \([21],[22]\), the proposed methodology can \([16]–[20]\) and has been experimentally verified down to cryo-effects. As the ZTC bias point is not specific to this technology B-G and substrate nodes without any dependency on the SH.

The curve for \( V_g = 0.54 \) V in solid lines, \( I_d \) decreases with \( T_A \) for large \( V_g \) biases because of stronger phonon scattering decreasing carrier mobility. These two mechanisms compensate each other at the ZTC bias point \([15]\), such that the \( I_d \) associated to this bias does not change with temperature. For the studied device, the ZTC bias is \( V_g, ZTC = 0.62 \) V for \( V_d = 0.8 \) V and \( V_{bg} = 0 \) V.

Fig. 1(a) shows the variation of \( g_d(f) \) computed as \( \text{Re}(Y_{dd}) \) for different ambient temperatures. Due to the threshold voltage reduction with increasing temperatures, \( I_d \) increases with \( T_A \) at low \( V_g \). Whereas, \( I_d \) decreases with \( T_A \) for large \( V_g \) biases because of the ac signal. \( Y_{ddT} \) and \( Y_{dgT} \) are by definition not affected by dynamic self-heating. \( T_A \) is the ambient temperature.

The inset in Fig. 1(a) shows the \( I_d-V_g \) curves for different ambient temperatures. From (2) and (3), it is plain to see that the low frequency values of \( g_d \) and \( C_{dd} \) (and the transition sign) depend on the sign of \( dI_d/dT_A \), and is thereby governed by the two opposing mechanisms of mobility and threshold voltage reduction with increasing temperature \([6],[7],[23]\). The frequency transition in itself is due to a delay in the heat transport mechanism from device to heat sink, yielding a lattice temperature that is not able to follow instantaneous variations of an ac power at frequencies above the isothermal frequency.

**Fig. 1.** Variation of the output conductance \( g_d(f) \) (\( \text{Re}(Y_{dd}) \)) w.r.t. its value at 100 kHz (a) and \( C_{dd}(f) \) (\( \text{Im}(Y_{dd}) \)), (b) of a 20 nm FD-SOI MOSFET biased at \( V_d = 0.8 \) V and \( V_g = 0.54, 0.62, \) and 0.7 V (symbols). Fitted electrical model at ZTC bias point \( V_g = V_{g,ZTC} = 0.62 \) V in solid lines, such that the dynamic self-heating effect is not present. Inset of (a): Measured \( V_d-V_g \) at \( V_d = 0.8 \) V from an ambient temperature of 300 K to 390 K.

**III. RESULTS**

We observe that a very good fitting is obtained across a very wide frequency range from 100 kHz up to approximately 10 GHz for the different bias points. The sign of the step (either positive or negative) is correctly reproduced in accordance with (2) and (3). To the best of our knowledge, it is

![Fig. 2.](image-url)
the first time that $g_{d}(f)$ and $C_{dd}(f)$ curves for $V_{g} < V_{g,ZTC}$ with a negative step in $g_{d}(f)$ are shown and that the total $R_{th}$ is extracted from them. Although the physical origin of this negative step is known and explained in Section II.A, such curves have not been presented previously, since high biases -where SH has higher impact, and thus a positive step in $g_{d}(f)$- are commonly used in self-heating characterization. With technology scaling down and power reduction, the voltage range below ZTC becomes of interest. Even if SH is lower at intermediate power and still performs well at low power, with resulting errors below 5% and 20%, respectively. The small remaining error at low $V_{g}$ can be explained by a slightly bias-dependent $Y_{ddT}$ not accounted for. The corresponding temperature rise ($\Delta T = R_{th, P}$) versus power ($P$) is displayed in the inset of Fig. 5. The extracted $R_{th}$ is roughly constant across the whole $V_{g}$ range and gives a median value of 202 K$\mu$m/mW.

IV. CONCLUSION

In this paper, we propose a method to extract the thermal impedance from device measurements unaffected by the substrate network in the frequency range of interest for dynamic self-heating. The ZTC bias condition can be used to extract any dynamic self-heating-free small-signal model. It can therefore be directly applied to measurements without requiring a compact model or simulation to capture the transition not related to SH. The developed procedure enables the extraction of $R_{th}(P,T_{A})$ from S-parameters at different bias conditions and related to SH. The developed procedure enables the extraction of $R_{th}(P,T_{A})$ from S-parameters at different bias conditions and related to SH. The developed procedure enables the extraction of $R_{th}(P,T_{A})$ from S-parameters at different bias conditions and related to SH.
