Flexible Instruction-Set Semantics via Type Classes

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Instruction sets, from families like x86 and ARM, are at the center of many ambitious formal-methods projects. Many verification, synthesis, programming, and debugging tools rely on formal semantics of instruction sets, but different tools can use semantics in rather different ways. As a result, a central challenge for that community is how semantics should be written and what techniques should be used to connect them to new use cases. The best-known work applying single semantics across quite-different tools relies on domain-specific languages like Sail, where the language and its translation tools are specialized to the realm of instruction sets. We decided to explore a different approach, with semantics written in a carefully chosen subset of Haskell. This style does not depend on any new language translators, relying instead on parameterization of semantics over type-class instances. As a result, a semantics can be a first-class object within a logic, and application of a semantics for a new kind of tool can be a first-class operation in the logic, allowing sharing of theorems across applications. Our case study is for the open RISC-V instruction-set family, and we have used a single core semantics to support testing, interactive proof, and model checking of both software and hardware. We especially highlight an application of a first-class semantics within Coq that can be instantiated in different ways within one proof: simulation between variants where multiplication is implemented in hardware or in the machine code of a particular software trap handler.

1 INTRODUCTION

Machine-language instruction sets are at the center of many aspects of systems implementation and verification. Such an important interface deserves a formal semantics. One semantics should be usable for all of documentation, simulation, testing, model checking, and interactive theorem proving. Furthermore, it should be usable for all the above applied to both software and hardware.

Many past projects demonstrated individual semantics usable for minorities of these cases. Leading approaches like Sail [Armstrong et al. 2019] involve domain-specific languages (DSLs) and ad-hoc translators from them into different languages appropriate to different use cases. Certainly, in many ways, it is hard to compete with languages purpose-built for a given style of program. It is not hard to stock a bestiary of potential domain-specific specification languages: high-level-language semantics, distributed-systems invariants, temporal logic for hardware, even pure mathematics. All the above might be brought together in one end-to-end-verified system for e.g. a cryptographic protocol implementation, with different layers verified using different tools and styles. However, there is a lurking risk of a classic “\[n^2\]” compilers problem: a translator must be built between each relevant pair of specification language and input language of a formal-methods tool. We might also worry about learnability challenges, for when one engineer encounters a specification in a new domain and must get to know a new language and not just a new library.

The two extremes of fully domain-specific and fully general-purpose specification languages present a challenging space of trade-offs, and it will take much more work to approach anything like a universal answer on which is “better.” However, in the study we report in this paper, our goal was to demonstrate that an important specification category, of instruction sets, can be handled pragmatically within a general-purpose specification language. Applications of our semantics for RISC-V achieved the following firsts for that instruction-set-architecture (ISA) family, to our knowledge.

- The first use of one semantics for both model-checking and interactive proof of deep functional-correctness properties of RISC-V machine code
- The first use of one semantics for both model-checking and interactive proof of deep functional-correctness properties of RISC-V processor implementations
Further, our semantics was at the center of the work of Erbsen et al. [2021], one of only a few results so far of deep functional-correctness proof of both hardware and complete software applications, formally linking their theorems through the common interface of an instruction-set semantics. Each use case involves different choices of complexities to bring in (e.g., virtual memory? weak memory model? I/O device interface?). We also support direct execution of the semantics with decent performance, and the original form of the semantics is decently readable (if not yet writable) even by an audience with the standard backgrounds of software or hardware engineers. It is difficult to be sure how much more or less smoothly these different exercises would have gone using other specification styles. Rather than trying to assert a clear directional comparison, we only aim to show that a promisingly complete ecosystem of tools can be stood up at reasonable cost, around a semantics written in a general-purpose language.

Our prototype semantics is implemented in a relatively small subset of Haskell. An advantage of choosing such a (relatively!) popular language is that translators for it already exist to a variety of other relevant languages; our case studies use translators to Coq and Verilog. The specific language and set of translators are somewhat incidental to our larger message. The right common specification language of the future might very well be quite different, but at least it would still only need one translator per target language, avoiding the $n^2$ problem we warned about above. However, one celebrated Haskell feature is central to how we make a single specification very flexible.

Wadler [1992] introduced monads in functional programming as a way to write code that is abstracted over kinds of effects. Indeed, they had already been used in projects like the Lava hardware framework [Bjesse et al. 1998] to allow flexible alternative interpretations of definitions. We will show that essentially the same kind of abstraction is a good fit for the variation across uses of instruction-set specifications. All the work of adapting the semantics for a new use case is in defining an instance of our new type class that extends monads with operations relevant to RISC-V execution. In other words, reusing our semantics is more like the standard experience of using a library than of picking and choosing generators associated with a DSL. An advantage of library status is that the semantics has first-class status, so, for instance, mechanized proofs of important metatheorems can be completed once-and-for-all. We will demonstrate this last point with a Coq proof that relates two instantiations of the semantics, one where the multiply instruction is implemented in hardware and one where it is implemented in software, by a trap handler for unimplemented instructions. The two instantiations are merely choosing different monads (three, in fact) to run a single semantics with. Instantiation takes place within the logic, rather than via tooling that generates new source files with no a-priori connection across instantiations.

Let us give a bit of background on RISC-V, the instruction set we chose, before turning to detail on how the semantics is written and how it is applied.

### 1.1 RISC-V as a formal-methods-research enabler

Until recently, formal-methods projects requiring specifications of processors were in an uncomfortable situation: the ISAs used in real processors were very complex, did not have openly accessible specifications, or were protected by patents. Therefore, each formal-methods project either invented its own ISA (e.g. Chlipala [2013]; Lööw et al. [2019]) or formalized from-scratch, at the desired abstraction level, a small subset of an existing ISA (e.g. Leroy [2009]).

Basic researchers breathed a sigh of relief with the increasing popularity of RISC-V\(^1\), which is controlled by a nonprofit foundation that does not limit who may implement the architecture. It is particularly compelling for formal-methods research, because it is a simple clean-slate design easy to reason about and yet features a mature open ecosystem. RISC-V is a family of instruction sets

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\(^1\)https://riscv.org/
broken into different native bitwidths (32, 64, 128) and extensions (e.g., multiplication and division instructions, atomics, \ldots) that may be mixed and matched. On the software side, there are fully upstreamed versions of Clang, GCC, and Linux. On the hardware side, the set of commercial and open-source processor designs is growing rapidly [Ken 2019; Sif 2019; Wes 2020; Celio 2018; Chen et al. 2020; Davide Schiavone et al. 2017; Zhang et al. 2018; Zimmer et al. 2015]. It makes for a very compelling platform for experimentation in basic research, progressively extensible to full-fledged realistic systems, where it is easy to tinker with any part of the software-hardware ecosystem.

Another advantage of RISC-V is existing community momentum around formal specification. There is an institutionally blessed semantics in the Sail DSL. While we would like to prove our semantics against that one eventually, we are held back for the moment by precisely the $n^2$ problem we described earlier, as we found the Sail-to-Coq translator to output unusably verbose code that was very challenging to work with interactively. That behavior is not surprising for a relatively young Sail tool mostly sharing code oriented around fast simulation via C code, and this weakness might very well be corrected soon, at which point we would be glad to undertake this exercise (no longer needing to do significant Sail-specific tool hacking ourselves).

1.2 Outline

The remaining sections review important elements of the RISC-V ISA, explain our specification style, and discuss how to cover different use cases with different type-class instances. Our implementation, including case studies, is available as a supplement to this submission.

The core claim we aim to defend throughout is that a formal semantics for an industrial-strength instruction-set family can be implemented fruitfully in a general-purpose language and applied across a representative set of examples, in formal methods and elsewhere, without writing any spec-language translators. We defend that claim by showing how each example works merely by choosing the right type-class instances and perhaps also by calling a from-Haskell translator that already existed. We also aim to illustrate the benefits of first-class parameterized semantics, where a semantics can be specialized to new applications within a proof assistant, allowing proof of metatheorems that apply to all specializations.

2 OVERVIEW

The nonprofit RISC-V Foundation (since renamed RISC-V International) developed an instruction-set-architecture specification in English [Waterman and Asanovic 2019a,b]. The goal of our project is to translate the English specification into a broadly applicable, machine- and human-readable formal specification.

There is a particular emphasis on avoiding overspecification: Platform-specific details that are left unspecified by the English specification should also be unspecified in the formal specification, while at the same time enabling users of the formal specification to pin down as many of these platform-specific details as appropriate for their use cases.

Orthogonally, we want to support the many different use cases shown in Figure 1: For instance, some users want an executable specification that returns one single final machine state, while others might want to leave some inputs, parameters, or nondeterministic choices abstract and obtain a logic formula restricting the set of possible final states, or obtain a list of final states, or obtain a checker that simply answers whether a given execution trace is allowed by the specification, etc.

To summarize, these requirements lead us to the following dimensions of parameterization:

- Supported extensions (see Table 1) and bitwidth (32-bit, 64-bit or left abstract)\(^2\)
- Platform-specific details

\(^2\)The RISC-V specification also defines a 128-bit variant that we did not consider.
• Use-case-specific details

2.1 Choice of language

Serious commitment to a multipurpose specification requires careful thought about the language it should be written in. One goal was to write readable functional programs that could be understood intuitively by hardware engineers or compiler hackers, even if they are not familiar with the underlying features (such as monads, type classes, etc.) enabling readability and parameterizability of the specification. Further goals were to create a specification that is practical to use in interactive theorem provers and to connect to other specifications, especially from the hardware world.

We found that Haskell was able to cover most of the constraints, thanks to the following:

• do notation provides syntactic sugar for readable imperative-looking code, particularly useful for this specification.
• the Clash compiler [QBayLogic 2020], compiling Haskell (with bounded recursion and finite datatypes) to Verilog/VHDL, is a bridge to hardware-model-checking tools.
• hs-to-coq [Breitner et al. 2018], a compiler that uses the GHC frontend to generate Haskell-like Coq code, built to prove Haskell programs in Coq, is a good bridge to interactive theorem proving in Coq.

We restrict ourselves to concepts supported by these three Haskell compilers (hs-to-coq, Clash, GHC). Via hs-to-coq, we produced a semantics that was chosen as the reference machine model in several Coq projects. Via Clash, we produced a minimal "single-cycle" Verilog execution model for which external people (authors of other specifications) checked the agreement between our spec and theirs. Finally, via GHC, we demonstrated the possibility to explore the basics of the RISC-V memory model and to test our specification as a simulator.

In our work, Haskell is a convenient stand-in for whatever turns out to be the ideal general-purpose language for writing a variety of multipurpose specifications. Writing translators to the input formats of different formal-methods tools can be a significant undertaking, so that it pays to introduce as few languages as possible that require translation. It may turn out that the ideal community-shared spec language is quite different from Haskell, but our interest here is...
showing that a general-purpose language can work well as the host for a multipurpose spec, leaving fine-tuning of the approach for future work. An important point is that we avoid use of any spec-language features specialized to ISAs.

### 2.2 Structure of the specification

Our RISC-V specification is composed of several extensions listed in Table 1, and an implementation can choose which subset of them to support. Our formalization of the specification only covers the most important of them.

**The primitives.** The key to supporting many different use cases is to specify the semantics of each instruction in terms of a small number of primitives listed in Figure 2, while leaving the implementations of these primitives to be filled in by the concrete use cases. The primitives include state-like constructs (for the registers, the memory, …) plus control-flow-like constructs (endCyc1e) to capture the control-flow change in case of an exception (see subsection 3.2) raised in the middle of the semantics of a function (an early return).

**Missing axioms.** One use of our semantics is verification of properties that hold for multiple (even infinitely many) different possible instantiations of this type class. In that way, we are able to establish metatheorems that hold across applications of the semantics, a goal hard to achieve when new applications are supported with new code produced by ad-hoc translators. However, for now, we do not support proving deep properties of our semantics for any possible instance of this type class, rather imposing additional restrictions on instances where needed. The reason is that we are not using axiomatic type classes [Wenzel 1997] that additionally assert logical axioms that any instance must validate. For instance, one might hope that, for any valid instance, getting the value of a register that we just wrote should return the value we have just written.

The trouble is that what counts as “reasonable” becomes much murkier very quickly, as we consider other aspects of the semantics. Foundational research questions remain around e.g. memory models in the presence of multisize accesses, virtual memory, self-modifying code, etc. These questions may come to be sufficiently settled to allow a complete-enough set of axioms to be included in our type class. For now, though, we explore just (1) the benefits of allowing the code for the instruction definitions themselves to be shared fruitfully across a variety of tools and (2) the possibilities of instance-parameterized theorems within Coq, with further local constraints.

**Instantiation.** The abstract monad p (of kind * -> *) can be instantiated differently by each use case, which keeps our spec agnostic to the concrete state of the machine and to the kinds of effects that instructions can have. For instance, depending on the platform and the use case, an invocation of the storeWord primitive could update the memory of the machine state, or it could fail if the address is outside of the physical address range, or it could record constraints in a

| Description                  | Name   | hs? | Coq? | Clash? |
|------------------------------|--------|-----|------|--------|
| Integer                      | I      | ✓   | ✓    | ✓      |
| Integer Multiply/Divide      | M      | ✓   | ✓    | ✗      |
| Atomics                      | A      | ✓   | ✗    | ✗      |
| Single Floating-Point        | F      | ✓   | ✗    | ✗      |
| Control & Status Registers   | Zicsr  | ✓   | ✓    | ✗      |

Table 1. Standard Extensions of RISC-V 20191213 (excluded: E, D, Q, L, C, B, J, T, P V, N, Zifencei, Zam, Ztso)
-- Indicates which stage is the source of a memory access

data SourceType = VirtualMemory | Fetch | Execute

-- Type class providing the RISC-V primitives:

class (Monad p, MachineWidth t) => RiscvMachine p t | p -> t where
  -- getRegister :: Register -> p t
  -- setRegister :: Register -> t -> p ()
  -- getFPRegister :: FPRegister -> p Int32
  -- setFPRegister :: FPRegister -> Int32 -> p ()
  -- loadByte :: SourceType -> t -> p Int8
  -- loadHalf :: SourceType -> t -> p Int16
  -- loadWord :: SourceType -> t -> p Int32
  -- loadDouble :: SourceType -> t -> p Int64
  -- storeByte :: SourceType -> t -> Int8 -> p ()
  -- storeHalf :: SourceType -> t -> Int16 -> p ()
  -- storeWord :: SourceType -> t -> Int32 -> p ()
  -- storeDouble :: SourceType -> t -> Int64 -> p ()
  -- makeReservation :: t -> p ()
  -- checkReservation :: t -> p Bool
  -- clearReservation :: t -> p ()
  -- getCSRField :: CSRField -> p MachineInt
  -- unsafeSetCSRField :: (Integral s) => CSRField -> s -> p ()
  -- getPC :: p t
  -- setPC :: t -> p ()
  -- getPrivMode :: p PrivMode
  -- setPrivMode :: PrivMode -> p ()
  -- commit :: p ()
  -- endCycle :: forall z. p z
  -- flushTLB :: p ()
  -- fence :: MachineInt -> MachineInt -> p ()
  -- getPlatform :: p Platform

Fig. 2. The primitives of the abstract RISC-V monad

memory-model graph, or it could record an I/O event if the address is in a range that the platform uses for memory-mapped I/O, etc., and our specification is completely agnostic to these options.

The abstract type \( t \) is the type of the values stored in the integer registers. It can be instantiated with \( \text{Int32} \), \( \text{Int64} \), or left abstract for use cases where it makes sense to reason about all bitwidths at once. Requiring a \( \text{MachineWidth} \) type-class instance for \( t \) guarantees that there are arithmetic and logical operators for \( t \). To distinguish \( t \) from helper integer values that do not live in registers, we introduce an additional integer type \( \text{MachineInt} \), which is an alias for \( \text{Int64} \), and whose more-significant bits are sometimes ignored. In fact, whenever we need an \( n \)-bit integer (with \( n \leq 64 \)) that does not live in a register, we use \( \text{MachineInt} \), applying bitmasking where necessary. In this way, we dodge use of dependent bitvector types indexed by width, as provided by DSLs like Sail. The tradeoffs on this question may also be debated, but at least representation is eased in general-purpose languages with rich but not dependent types, and our case studies will demonstrate that a variety of tasks in programming and formal methods remain tractable with laxer help from typing.
Instructions. The above choice also shows up in our algebraic datatype of instructions:

```
data InstructionI =  
  Sw { rs1 :: Register, rs2 :: Register, simm12 :: MachineInt } |  
  Add { rd :: Register, rs1 :: Register, rs2 :: Register } |  
  Beq { rs1 :: Register, rs2 :: Register, sbimm12 :: MachineInt } | ...  
```

For instance, even though the offset field of the store-word instruction is only a signed 12-bit immediate, we represent it with a (64-bit) `MachineInt` for simplicity. Note that this simplification does not compromise correctness, because the specification only creates instructions in the decoder, which only ever writes 12-bit values into that field.

Decode. The decoder starts by defining symbolic names for notable bitfields of the instruction `inst` being decoded:

```
opcode = bitSlice inst 0 7  
rd = bitSlice inst 7 12  
rs1 = bitSlice inst 15 20  
rs2 = bitSlice inst 20 25  
simm12 = signExtend 12 $(shift (bitSlice inst 25 32) 5 .|. bitSlice inst 7 12  
  ...  
```

and then defines a decoder for each RISC-V extension:

```
decodeI  
| opcode==opcode_STORE, funct3==funct3_SW = Sw rs1 rs2 simm12  
| opcode==opcode_BRANCH, funct3==funct3_BEQ = Beq rs1 rs2 sbimm12 ...  
```

and finally, checks if the decoded instruction is part of the supported extensions.

Execute. For each RISC-V extension supported, there is an `execute` function that expresses the effects of each instruction of the extension in terms of the primitives listed in Figure 2. For instance, here is the definition of the jump-and-link-register instruction, for which explanatory prose will be provided shortly thereafter:

```
execute (Jalr rd rs1 oimm12) = do  
x <- getRegister rs1  
pc <- getPC  
  let newPC = (x + fromImm oimm12) .&. (complement 1)  
if (remu newPC 4 /= 0)  
  then raiseExceptionWithInfo 0 0 (fromIntegral newPC)  
else do  
  setRegister rd (pc + 4)  
  setPC newPC  
```

It was transcribed from the following English definition:

The indirect jump instruction JALR (jump and link register) uses the I-type encoding. The target address is obtained by adding the sign-extended 12-bit I-immediate to the register \( r_s1 \), then setting the least-significant bit of the result to zero. The address of the instruction following the jump \( (pc + 4) \) is written to register \( rd \). Register \( x_0 \) can be used as the destination if the result is not required. The JAL and JALR instructions will generate an instruction-address-misaligned exception if the target address is not aligned to a four-byte boundary.
It uses Haskell’s do notation to chain monadic operations, and it can also use standard Haskell constructs such as let or if. The binary operators (such as +, /= and .&, in this example) are provided through the MachineWidth type class. It inherits from Haskell’s standard type classes Integral and Bits, allowing us to use the standard infix operators. MachineWidth also provides fromImm to convert immediates from instructions into register values.

Run. Finally, we define what it means to run one instruction. For the Coq proofs, we use a simplified version that just fetches an instruction, decodes and executes it, and updates the program counter, whereas the Haskell version also considers interrupts and exceptions.

Use-case- and platform-specific code. The components described so far form the specification and are grouped together in a directory called Spec. However, we have not yet defined how state is represented and how the primitives of Figure 2 are to be implemented. These use-case- and platform-specific definitions are in a separate directory called Platform and are the subject of the next section. The Spec and Platform directories each are about three thousand lines of code.

3 DIFFERENT MONADS FOR DIFFERENT USE CASES

Our RISC-V specification benefits from using a monad (the p in Figure 2) in the very same way as Wadler’s interpreter in his classic “The Essence of Functional Programming” paper [Wadler 1992]. In this section, we tour the wide variety of applications that can be connected to this single semantics. The key claim we emphasize throughout is that each application is supported simply by picking new type-class instance(s) and perhaps also by calling general-purpose translators from Haskell – no new translators or even parsers specific to ISA descriptions were required.

We begin with a brief description of mundane use cases in interpretation (essentially the original application of monads that concerned Wadler). Next, we spend the bulk of our discussion on different flavors of interactive proofs with Coq, before wrapping up with case studies of automated model-checking (outside Coq) of both machine-code programs and RISC-V processors.

3.1 Simulation

Support fast interpretation of machine-code programs by choosing efficient but harder-to-reason-about data structures.

The most common way of modeling processors in the formal-methods world is to consider the machine to be deterministic, each cycle updating the state of the registers and the memory depending on the instruction present in memory at the location pointed to by the program counter.

Concretely, we wrote two instances of the RiscvMachine type class, named Minimal32 and Minimal64, to obtain a 32- and a 64-bit machine simulator. We instantiated the type class in the I/O monad, using references and arrays to implement registers, program counter, and memory.

3.2 Supporting RISC-V exceptions

Support early exit via exceptions by using a variant of the classic monad transformer for failure.

Many formal-methods-oriented projects do not want to deal with exceptions or interrupts, while others are interested in modeling and leveraging them. The formal-spec user should experience the costs of those further features incrementally as they are brought into play.

Raising an exception involves two components: modifying a bunch of state (namely numerous special state registers [CSRs]) and bailing out of a cycle early, not performing the effects of the instruction that would have come after an exception is raised. In RISC-V, exceptions can be caused

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3 but still accurate with respect to real software and hardware, because both the processor and the compiler are proven to respect this same simplified specification
by virtual-memory translation failures, failed system privilege checks, and alignment problems, among other causes.

To be able to write monadic values carrying this early-exit information, we encode the early return in a layer of a MaybeT monad transformer. The crucial primitive already appeared in our definition of the RiscvMachine monad.

```
endCycle :: forall z. p z
```

Conspicuously, an implementation of endCycle is missing from the base machine previously described as Minimal64/32, but there is one given in source file Machine.hs:

```
instance (RiscvMachine p t) => RiscvMachine (MaybeT p) t where
  getRegister r = lift (getRegister r)
  setRegister r v = lift (setRegister r v)
  ...
  endCycle = MaybeT (return Nothing) ...
```

This instance demonstrates something powerful about our spec: composability. It takes some existing instance of the same type class and builds on it, adding in the functionality of the Maybe monad. In that monad, a computation halts as soon as a step returns Nothing, precisely capturing the “early-return” behavior we want upon encountering an exception.

With this two-layer specification, we ran in simulation the riscv-tests test suite (rv64mi, rv64si, rv64ui, rv64ua), which is the standard community-maintained test suite.

### 3.3 Platform modeling, MMIO, and devices

Support I/O features by providing additional monad transformers.

We actually use this kind of instance augmentation repeatedly in our code, first to encode the semantics of core features (like RISC-V exceptions, as we have just seen) but also to add features like memory-mapped I/O devices to existing RiscvMachine instances.

For example, we enrich the platform with a concurrently memory-mapped device: a UART connected to from a terminal, which generates interrupts received by the main loop of the simulator.

With this implementation, composed of three layers of specifications, we were able to run Linux in January 2019 at about 100k instructions per second. (We have not tracked newer Linux versions.)

While this strategy allows us to experiment, test, and vouch for our good coverage of the spec, this artifact is not especially competitive for running significant RISC-V programs, e.g. the popular QEMU runs at several hundred million instructions per second.

### 3.4 Interactive theorem proving

3.4.1 Translation from Haskell. Using hs-to-coq [Breitner et al. 2018], we can translate the Haskell specification to Coq. Since hs-to-coq was designed to model Haskell semantics in Coq as faithfully as possible, it ships with handwritten and auto-generated translations of Haskell’s standard-library files, and by default they are referenced by the Coq files produced by hs-to-coq. However, for this project, we were not seeking a faithful reproduction of Haskell semantics in Coq but rather an idiomatic RISC-V specification in Coq. Therefore, we used hs-to-coq’s edit files feature, which allows one to provide renaming and rewriting patterns to be applied during the translation, so that we could map all Haskell standard-library references to reasonably close Coq equivalents and obtain an idiomatic, Haskell-independent Coq specification.

We used hs-to-coq to translate the files specifying how each instruction is executed, the instruction decoder, as well as the CSR-file specification, while we manually wrote remaining files like utility definitions, the definition of the RiscvMachine type class, and proof-specific files.
3.4.2 Use as the interface between software and hardware. Our RISC-V Coq specification was used successfully in a project [Erbsen et al. 2021] that combines a compiler-correctness proof with a processor-correctness proof.

The combined theorem states that the I/O trace produced by the processor matches the one produced by the source program fed to the compiler, without referencing the RISC-V specification any more. Thus, auditors of the system can know the behavior of the system without having to audit whether both the compiler and the processor interpret the RISC-V specification in the same way, which greatly reduces the auditing burden.

3.4.3 Opting out of features and opting back in.

Support different applications referring to different complexities of the ISA family by connecting those complexities to methods of the type class.

Our first version of the translation to Coq was driven by the requirements of the compiler-correctness project mentioned above, which required a very simple and manageable spec to get started, so it was decided that initially, CSRs should not be modeled. However, this also meant that we could not use the real raiseException function, nor the translate function (translating virtual to physical addresses), which starts by reading a CSR that indicates whether virtual memory is enabled. The solution was surprisingly simple: Since we had already chosen manual translation of the file containing the declaration of the RiscvMachine type class, we were free to abstract over raiseException and translate by adding them to the primitives of RiscvMachine (Figure 2). That is, we made our specification more configurable than RISC-V allows, and for the compiler, we instantiated translate to the identity function and raiseException to hard failure, because no instructions emitted by the compiler rely on exceptions, while at the same time, we kept open the possibility to instantiate these two functions with (more) real definitions.

These modifications are not RISC-V-compliant, but we consider it an important feature of our specification that we were able to make them, while still being able to translate most of the specification to Coq automatically and thus continuously pull updates and bugfixes made in Haskell into the Coq code base.

Later, when we added CSRs to the Coq specification, we wrote a simplified raiseException function. Since the compiler does not use it, it was trivial to integrate this update with the proof.

3.4.4 Simulator in Coq.

Support interpretation within a proof assistant by developing similar instantiations to the earlier simulator case, using more naive purely functional data structures. A failure monad provides convenient opportunities to indicate unsupported language features, such that individual programs must then be proved not to exercise those features.

State monad. In Coq, the simplest-possible instantiation of the monad is \( p := \text{State MachineState} \), where State is the state monad defined as \( \text{State}(S A : \text{Type}) := S \rightarrow (A * S) \), and MachineState is a record containing the values of the processor’s registers, the program counter, the memory, the CSR file, and the current privilege level. This instantiation can be used to obtain a deterministic RISC-V simulator.

State monad with failure. An arguably even-simpler monad instantiation is \( p := \text{OState MachineState} \), where \( \text{OState}(S A : \text{Type}) := S \rightarrow (\text{option} A) * S \) uses a None answer to indicate that a failure occurred. Its Bind and Return operations are implemented as

\[
\begin{align*}
\text{Bind} & \ A \ B \ (m : \text{OState} S A) \ (f : A \rightarrow \text{OState} S B) := \\
& \quad \text{fun} \ (s : S) \Rightarrow \text{match} \ m \ s \ \text{with} \ (\text{Some} \ a, s') \Rightarrow f \ a \ s' \ | \ (\text{None}, s') \Rightarrow (\text{None}, s') \ \text{end}; \\
\text{Return} & \ A \ (a : A) := \text{fun} \ (s : S) \Rightarrow (\text{Some} \ a, s)
\end{align*}
\]
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and an unrecoverable (hard) failure can be implemented as
\[
\text{fail-hard } S A := \text{fun } (s : S) \Rightarrow (\text{None}, s)
\]
For compiler-correctness proofs, \text{fail-hard} can be used to indicate that a situation occurred that the compiler is supposed to avoid, e.g., memory access at an invalid address, and a compiler-correctness proof then states that all valid source programs are translated to RISC-V programs that never fail.

Moreover, if the compiler has been designed to emit code that does not use certain features, the RISC-V specification can be simplified by implementing the primitives of Figure 2 used by these features as just \text{fail-hard}. For instance, the compiler presented by Erbsen et al. [2021] emits code that does not depend on the CSRs, does not use floating-point operations or atomics, and assumes that there is no virtual memory and that the code always runs at the \text{MachineMode} privilege level. Therefore, the monad instantiation used to specify its correctness implements the primitives \text{makeReservation}, \text{checkReservation}, \text{clearReservation}, \text{getCSRField}, as well as \text{unsafeSetCSRField}, \text{getPrivMode}, \text{setPrivMode} of Figure 2 as just \text{fail-hard} (while the TLB- and floating-point-related methods were omitted altogether in the translation from Haskell to Coq).

3.4.5 Nondeterminism.

Support \text{nondeterministic execution} by choosing a monad that associates executions with mathematical sets of results (a possibility not available directly in Haskell).

One way to add nondeterminism is to use the nondeterministic option state monad,
\[
\text{OStateND } S A := S \rightarrow \text{option } (A \times S) \rightarrow \text{Prop},
\]
where the option’s \text{None} constructor is used to indicate failure, and \text{option } (A \times S) \rightarrow \text{Prop} can be thought of as the set of all possible outcomes. Its \text{Bind} and \text{Return} operations are implemented as
\[
\text{Bind } A B (m: \text{OStateND } S A)(f : A \rightarrow \text{OStateND } S B) := \text{fun } (s : S) (obs: \text{option } (B \times S)) \Rightarrow (m s \text{ None } \land obs = \text{None}) \lor (\exists a s', m s (\text{Some } (a, s')) \land f a s' obs);
\]
\[
\text{Return } A (a : A) := \text{fun } (s : S) (oas: \text{option } (A \times S)) \Rightarrow oas = \text{Some } (a, s)
\]

3.4.6 Runtime input.

Support \text{input and output} by combining nondeterminism with a state type extended to store a trace of interactions.

Once we have nondeterminism, we can use it to model memory-mapped I/O (MMIO). For instance, in the implementation of the \text{loadWord} primitive, if the address is not a physical memory address, we delegate to the following helper function:
\[
\text{mmio_load32 addr: OStateND } S \text{ int32} := \text{fun } s oas \Rightarrow (\text{isMMIOAddr } addr \land \exists v : \text{int32}, oas = \text{Some } (v, (\text{appendLog } (\text{mmioLoadEvent } addr v) s))) \lor (\neg \text{isMMIOAddr } addr \land oas = \text{None})
\]
It can be read as a function that for each current state \(s\) returns a proposition that indicates whether an outcome \(oas\) of type \(\text{option } (\text{int32} \times \text{MachineState})\) is in the set of possible outcomes, distinguishing two cases based on whether the address lies in the address range reserved for MMIO. We also augment \text{MachineState} with a log to which we append an MMIO event on each load and store that falls into the MMIO address range.

Proof of a compiler targeting this specification will have to show that all states in the outcome set given by \text{mmio_load32} satisfy the compiler’s correctness guarantees (such as being related to a state of the source-language execution), so the body of \text{mmio_load32} will appear on the left-hand side of
an implication, so the existentially quantified \( v \) becomes universally quantified, and as expected, the compiler has to prove that its guarantees hold for all possible values \( v \) that this MMIO load could have read.

### 3.4.7 Nondeterminism by means of weakest preconditions.

Support smooth integration with Hoare-logic-style program verification by first assigning programs meanings in the style of interaction trees and then applying recursive functions (like weakest-precondition computation) to those trees.

The Bedrock2 compiler [Erbsen et al. 2021] using our RISC-V specification requires RISC-V semantics that given an initial state \( s \), a monadic computation \( m \) corresponding to the execution of a sequence of primitives from Figure 2, and a desired postcondition, returns the weakest precondition that must hold in order for the postcondition to hold. Therefore, it seems that we need the following bridge definition that tells when a monadic \( \text{OStateND} \) computation satisfies a postcondition:

\[
\text{mcomp_sat} \; S \; A \; (m:\; \text{OStateND} \; S \; A) \; s \; \text{post} := \\
\forall \; o, \; m \; s \; o \rightarrow \exists \; a \; s', \; o = \text{Some} \; (a, \; s') \land \; \text{post} \; a \; s'
\]

For an example relating this definition to the previous subsection, \( m \) could be instantiated with \( \text{mmio_load32} \; \text{addr} \), and \( \text{post} \) could be instantiated with the claim that the final state is related to a state of the source-language execution.

When instantiating \( m \) with a monadic computation involving many \( \text{Binds} \), unfolding \( \text{mcomp_sat} \) and all the \( \text{Binds} \) quickly leads to huge formulas involving an existential for each intermediate state and answer, and we found these formulas to be larger than what human brains can deal with productively. The solution was to treat \( \text{mcomp_sat} \) and \( \text{Bind} \) as opaque and to prove weakest-precondition-style rules for each primitive of Figure 2, using only these rules in the compiler-correctness proof, so that the large formulas were confined to just the proofs of these rules.

However, when a processor in the Coq-embedded hardware-description language Kami [Choi et al. 2017] was being proved against our RISC-V specification, the same formula-explosion problem struck again, but this time, on the other (left-hand) side of the implication. Inversion rules for \( \text{mcomp_sat} \) of primitives, dual to the weakest-precondition-style rules mentioned above, might have been a way to go, but it turned out that it is simpler (both for the compiler and the processor) to use an instantiation that is more suitable for weakest-precondition generation, namely a free monad.

In the style of interaction trees [Xia et al. 2020], we use a Coq \textbf{Inductive} for effects with one constructor per primitive of Figure 2, and a generic free monad with one constructor for an effect followed by a continuation, plus a second constructor to indicate termination. \( \text{Bind} \) for this monad can be defined as a \textbf{Fixpoint} that flattens monadic computations that might have nested \( \text{Binds} \) as the first argument of \( \text{Bind} \) into a more canonical form. A result is almost a sequential list of effects (ended by the termination constructor of the free monad), except in the case of nondeterminism, where branching can occur, so the shape becomes a tree there.

On this free-monad structure, we can run an interpreter that computes weakest preconditions. The crucial difference between \( \text{OStateND} \) and the free-monad interpreter is that the former creates an existential for the intermediate state and answer of each \( \text{Bind} \), whereas the latter works similarly to a continuation-passing-style interpreter and just passes updated states to the right-hand sides of the \( \text{Binds} \), leading to considerably simpler formulas. For comparison, here is the helper function that the interpreter invokes in the \text{loadWord} case when the address is not a physical memory address:

\[
\text{mmio_load32} \; \text{addr} := \text{fun} \; s \; \text{post} \Rightarrow \\
\text{isMMIOAddr} \; \text{addr} \land \forall \; v: \text{int32}, \\
\text{post} \; v \; (\text{appendLog} \; (\text{mmioLoadEvent} \; \text{addr} \; v) \; s)
\]
Note how, contrary to OStateND, no case for failure is needed, and the value v being read is already universally quantified, rather than existentially quantified on the left-hand side of the implication of mcomp_sat, and if more code follows after this snippet, it will be put into post and thus be invoked with the updated state (appendLog (mmioLoadEvent addr v) s), with no intermediate existential.

3.5 Multiplication in software: Reasoning about multiple instantiations of our spec

Support proving connections between semantics variants (e.g. standing for capabilities of different conformant processors) by simply instantiating the semantics with different type-class instances and mentioning the different instantiations in single theorem statements and proofs.

As a case study to showcase the benefits of instantiations of our spec being first-class objects, we present a Coq proof of the correctness of a trap handler that implements multiplication in software, for embedded processors that only implement the `I` extension of RISC-V and thus raise exceptions when encountering multiplication instructions.

We want to show that a machine without hardware support for multiplication, but correctly configured with an exception handler that implements multiplication in software, behaves like a machine that supports multiplication in hardware. This theorem could then be used to simplify reasoning about programs running on a machine without hardware multiplication, because it saves the burden of reasoning about the trap handler and instead makes it as easy as reasoning about the specification with multiplication in hardware:

```coq
match inst with
| Mul rd rs1 rs2 ⇒ x ← getRegister rs1; y ← getRegister rs2; setRegister rd (mul x y)
| ...
end
```

Parts of the exception handler are implemented in the Bedrock2 source language [Erbsen et al. 2021] and compiled using the Bedrock2 compiler, but the handler also needs some low-level operations that are not expressible in the Bedrock2 source language and are therefore implemented by-hand in assembly. Our proof combines a program-logic proof about the Bedrock2 handler function, the compiler-correctness proof, and a proof about the assembly instructions, guaranteeing that all these parts have been put together correctly, and the final statement only mentions RISC-V semantics. All the other interfaces have been canceled out by combining the proofs and thus are not part of the trusted code base any more.

In this case study, three instances of our RISC-V semantics are involved (where the first one does not appear in the final theorem statement but only inside its proof):

- An instance used by the compiler-correctness proof, which does not have any CSRs (control and status registers, required by the exception mechanism) in its state and fails (with undefined behavior) on all CSR-related instructions. For the compiler, this instance was chosen to simplify the proof, because the compiler does not emit any instructions that depend on CSRs.
- The instance with hardware support for multiplication
- The instance with a trap handler implementing multiplication in software

3.5.1 The theorem statement. We can state the theorem as follows:

**Theorem** softmul_correct: forall (initialH initialL: State) (post: State → Prop),
runsTo (mcomp_sat (run1 mdecode)) initialH post →
related initialH initialL →
runsTo (mcomp_sat (run1 idecode)) initialL (fun finalL ⇒
  exists finalH, related finalH finalL ∧ post finalH).
It uses $\text{run1}$, a function that defines how one single instruction is executed, which is parameterized over the instruction decoder, and to which we pass $\text{mdecode}$ (a decoder that supports the multiplication instruction) in the hypothesis and $\text{idecode}$ (a decoder that returns $\text{InvalidInstruction}$ for the multiplication instruction) in the conclusion:

**Definition** run1$(\text{decoder}: \mathbb{Z} \rightarrow \text{Instruction}): \text{M unit} :=$

- $\text{pc} \leftarrow \text{getPC};$
- $\text{inst} \leftarrow \text{Machine.loadWord Fetch pc};$
- $\text{Execute.execute (decoder (LittleEndian.combine 4 inst))};$
- $\text{endCycleNormal}.$

The $\text{mcomp_sat}$ function is of type $\text{M unit} \rightarrow \text{State} \rightarrow (\text{State} \rightarrow \text{Prop}) \rightarrow \text{Prop}$ and asserts that a monadic program (consisting of primitives of Figure 2), applied to some initial state, satisfies a postcondition, and $\text{runTo}$ lifts it to an arbitrary (but finite) number of steps. The predicate $\text{related}$ is used to relate a high-level state (i.e. the state of a machine that supports multiplication in hardware) to a low-level state (i.e. the state of a machine that implements multiplication in software using a trap handler), and it also contains all the preconditions on how the low-level machine needs to be configured. That is, $\text{related}$ asserts that the two states have the same values for the registers and the program counter, and that the memory (modeled as a partial map from 32-bit addresses to bytes) of the low-level machine contains everything of the high-level memory, as well as the instructions of the exception handler and some scratch space that the exception handler can use as its stack (which must be available even if the main program has used up all of its stack). To define at which address in memory the handler and the scratch space are located, RISC-V defines some control-and-status registers (CSRs) that our definition of $\text{related}$ mentions:

- The CSR called $\text{MTVecBase}$ is used to store the address of the trap handler.
- The CSR called $\text{MScratch}$ is a read/write register dedicated for use by machine mode, and we use it to store the address of the end of this scratch space.

So overall, the theorem $\text{softmul-correct}$ can be read as follows: If a machine with hardware multiplication runs to a high-level state satisfying a postcondition, then every related machine with software multiplication runs to a low-level state which, when translated back to a high-level state, satisfies the same postcondition.

### 3.5.2 The handler code.

The exception-handler code is implemented partially in handwritten assembly and partially in the Bedrock2 [Erbsen et al. 2021] source language and compiled to bytes by the Bedrock2 compiler. In order to prove the $\text{softmul-correct}$ theorem, we use the correctness theorem of the Bedrock2 compiler, but note that the statement of the $\text{softmul-correct}$ theorem does not depend on the Bedrock2 language semantics or on anything related to the fact that we used the Bedrock2 compiler, so the auditing burden for someone (who trusts the Coq proof checker) auditing our handler is much smaller, because one does not need to worry about the compiler, its language semantics, and its interaction with the assembly code.

The first few instructions of our handler (handwritten in Coq) are as follows:

**Definition** handler_init :=

```
[ [ Csrw sp sp MScratch; (* swap stack pointer (sp) and MScratch CSR *)
  Sw sp zero (-128); (* save the 0 register (for uniformity) *)
  Sw sp ra (-124); (* save ra *)
  Csr ra MScratch; (* use ra as a temporary register... *)
  Sw sp ra (-120); (* ... to save the original sp *)
  Csrw sp MScratch; (* restore the original value of MScratch *)
  Addi sp sp (-128) ]]. (* remainder of code will be relative to updated sp *)
```
After that, the registers 3 to 31 are saved to the scratch space as well, and then the Bedrock2-generated part is called by passing it the value of the CSR register MTVal, which contains the invalid instruction that caused the exception, and a pointer to the scratch space in which we saved the registers. The Bedrock2 code is written directly in Coq using the custom-notations feature, a C-like syntax, and operator precedence as suggested by whitespace in this example:

```
Definition softmul := func! (inst, a_regs) {
  a = a_regs + (inst>>15 & 31)<<2;
  b = a_regs + (inst>>20 & 31)<<2;
  d = a_regs + (inst>>07 & 31)<<2;
  unpack! c = rpmul(load(a), load(b));
  store(d, c)
}
```

It extracts the three 5-bit fields of the instruction that indicate the two source registers (operands of the multiplication operation) and the destination register, respectively, and then calls another Bedrock2 function rpmul that implements multiplication in terms of addition, storing the result back into the scratch space. The rpmul function iterates over the bits of the second operand while repeatedly doubling the first operand, a technique sometimes called “Russian peasant multiplication.” Both softmul and rpmul are verified using the Bedrock2 program logic. The spec of the former is:

```
Instance spec_of_softmul : spec_of "softmul" :=
  fnspec! "softmul" inst a_regs / rd rs1 rs2 regvals R,
  { requires t m :=
      mdecode (word.unsigned inst) = MInstruction (Mul rd rs1 rs2) ∧
      List.length regvals = 32 ∧
      seps [a_regs ↦→ word_array regvals; R] m;
    ensures t' m' := t = t' ∧
      seps [a_regs ↦→ word_array (List.upd regvals (Z.to_nat rd) (word.mul
          (List.nth (Z.to_nat rs1) regvals default)
          (List.nth (Z.to_nat rs2) regvals default))); R] m' }. 
```

Its pre- and postcondition are expressed in terms of an (unused) I/O trace t and the memory m, for which we assert a list of two separation-logic clauses (a word array corresponding to the scratch space containing the register values, and a generic frame R for the rest of the memory).

By combining the program-logic proofs about the two Bedrock2 functions with the compiler-correctness theorem, we obtain that if we run the compiler within Coq to obtain a list of instructions mul-insts, these instructions satisfy a verbose but unsurprising specification, laying out calling-convention details.

### 3.5.3 Correctness proof of assembly part

The assembly part of the handler is proven correct by induction over the runsTo hypothesis of softmul_correct. If the machine with hardware multiplication executes any instruction besides multiplication, we just need to show that after executing the same instruction on the machine with software multiplication, the related judgment is preserved, but we can do that once-and-for-all by inspecting each primitive of Figure 2, instead of analyzing the much larger number of instructions that RISC-V has. The interesting case is when the machine with hardware multiplication encounters a multiplication instruction, and we have to show that the machine with software multiplication steps to a related state. We do so by first symbolically executing the specification of what the hardware does in case of an exception, which boils down to setting some CSR fields and then setting the PC to the exception-handler address found in the MTVecBase CSR. After that, we symbolically execute the handwritten assembly instructions, using
Coq’s proof context to keep track of all the facts that we know about the current state of the machine. For each assembly instruction, we encounter its specification in terms of the primitives of Figure 2, and for each primitive, we have a helper lemma that updates our symbolic state. At the point where we reach the call to the Bedrock2-generated code, we apply the correctness lemma for the compiled trap handler. After that call, we step through more handwritten assembly instructions that restore the registers and then call the Mret instruction that jumps back to one instruction past the multiplication instruction that caused the exception. At that point, we need to prove that the symbolic state accumulated in the Coq proof context implies that the two machines are still related, which only works if there are no bugs in the handler code.

3.5.4 Bugs found during verification. At that final point in the proof described above, we actually found two interesting bugs. The first one was that we forgot to reset the MScratch CSR, so one invocation of the exception handler works fine, but the next one will use a wrong address for its scratch space. The second bug was the corner case where the multiplication instruction stores its result into the stack pointer. In that case, we must not override the stack pointer with the original stack pointer that we swapped into the MScratch register at the beginning of the handler.

We also found two more obvious bugs related to when to set the stack pointer and what stack-pointer offsets to use.

3.6 Model checking with weak memory models

So far, in considering breadth of applications of our semantics, we have covered the classic examples of program interpretation and interactive proof. We finish with another classic, model checking, first of software programs and then of hardware designs.

Support model-checking of all possible program executions under weak memory by choosing a type-class instance that records information on alternative paths that should be tried later.

In this section we outline our approach to instantiate the type class to generate all outcomes of small multicore litmus tests with respect to the memory model. We instantiate the type class with a runtime implementing the exploration algorithm of Kokologiannakis and Vafeiadis [2020].

This algorithm revolves around 4 data structures:

- a control/data/addr dependency-bookkeeping data structure, to maintain a list of all the memory events that imply dependencies on the currently interpreted instruction
- a current partial execution graph, which is the graph of the memory events and their memory-model relations
- two bookkeeping data structures necessary for backtracking during search: a list of alternative partial execution graphs to explore later and a maintained set of all the read events that would be subject to revisiting, if a store to the same address would occur.

Intuitively, our implementation goes as follow: we write an interpreter in charge of exploring an execution path depth-first. That interpreter also records all the alternative decisions that it could have taken on its way. The interpreter can either return successfully with a valid execution, or it can return that the execution that it explored ended up violating the memory model. In both cases, the interpreter updates the global bookkeeping of alternative executions.

More precisely, the interpreter is a classic interpreter except for the following twists.

- It keeps track of the dependencies that previous memory events have on the different registers.
- It is worth noting that this functionality does not need to be interleaved in the execution semantics. Rather, it can be done directly from the decoded instruction without looking at register values. The reason is that, for one instruction, dependencies are known statically.
instance RiscvMachine (MaybeT (ReaderT Ptrs IO)) Int64 where
loadWord Execute ad = do
  refs ← ask
  (ev, execution) ← readEnv refs
  if Set.member ev (domain execution)
    then getValFromDomain ev execution
    else do
      updateRevisitSet refs ev
      (writeToReadFrom, altExecs) ← generateReadExecs refs ev execution ad
      lift . lift $ writeIORef (r_currentExecution refs) newExec
      storeAltExecs refs altExecs
      checkAlloyModel writeToReadFrom newExec

where ...

Fig. 3. Excerpts from the memory-model-checking instantiation of the RISC-V type class

- On a load, the interpreter adds to the partial execution that the load reads from one of the stores to the same address already present in the current partial execution. The interpreter also adds all other possible alternative stores to the same address as alternative executions to explore later. The interpreter then calls Alloy [Jackson 2002] with the partial execution graph that it just extended. Alloy verifies that this extension is RISC-V-compliant. If not, the interpreter signals failure after updating backtracking structures; otherwise, it keeps running.
- On a store, the interpreter both adds a new store event to the current execution and updates the alternative partial executions: any load in the revisit set that loads from the address of the current store is the source of a new partial execution to record.
- When the interpreter reaches the end of one thread, it starts running the next thread. When the interpreter finishes running the last thread successfully, it returns that the current execution is a valid execution.

This straightline interpreter does not do the backtracking itself. Instead, it is called from a top-level loop that keeps calling the interpreter on the next partial execution to explore, each time either getting a valid execution or a failure but an updated backtracking structure.

We implement this model-checking interpreter by instantiating the RiscvMachine type class in the I/O monad. We use references to track state associated with the model-checking algorithm. We modify the Minimal64 machine described in Section 3.1 and add the partial-execution graph and bookkeeping data structures described above. The RiscvMachine instance implements dependency tracking in the loadWord, storeWord, and fence primitives; other primitives are implemented similarly to the Minimal64 simulator. Figure 3 shows excerpts from the definition of this instance.

The complete implementation is 800 lines of Haskell.

We use the upstream official Alloy specification [Lustig 2018] for RVWMO, one of the several machine-readable forms available online for the RISC-V weak memory model.

We only support word load and store instructions plus a TSO fence, as our intention was simply to demonstrate that one can implement state-of-the-art memory-model-exploration algorithms using our specification. Hence we did not go through the implementation of the exploration for atomics and release/acquire fences, which, based on the study of Kokologiannakis and Vafeiadis [2020], we predict would not require interestingly different ingredients.
3.6.1 Running RISC-V memory-model litmus tests. To demonstrate the usefulness of our model-checker, we develop a simple test harness to symbolically execute litmus tests for the RISC-V memory model. We use the litmus tests provided by Flur et al. [2019], which were also used by the RISC-V Memory Model Task Group during development of the ISA specification. These litmus tests were generated using the diy tool suite [Alglave and Maranget 2020] and test a range of possible memory-model behaviors including store buffering, load buffering, and message-passing; each test has several variants that add fences, address dependencies, control dependencies, or data dependencies to highlight possible behaviors of the RISC-V memory model. Each test consists of some initialization conditions on registers or memory, the instructions to be run on each thread to test the behavior of interest, and a postcondition which is met if the behavior of interest occurred. For example, the message-passing litmus test has a postcondition testing for the case where the flag is set but the value was not set.

The architecture of our test harness is as follows. We first parse the litmus-test specification file into a simple symbolic representation. We then compile the initialization conditions and testing instructions into a small RISC-V assembly file, which first initializes the register state of each thread and then executes each thread’s instructions. We use gcc to compile the assembly file into an ELF file, which is then passed to our model-checking algorithm as described in subsection 3.6. The model-checking algorithm is modified to store the final register state of each thread (upon reaching the stopping PC value). For every execution deemed valid by the Alloy solver, we check whether these final register states satisfy the test postcondition; if so, this is reported to the user.

It is important to note that the litmus-test postconditions do not constitute a specification for the memory model; rather, they indicate particular weak-memory-model behaviors that may or may not be allowed by the ISA or by implementations thereof. We therefore validate our model-checker by checking that it generates the same behaviors as the axiomatic herd and operational rmem model-checking tools [Flur et al. 2019].

We are able to run all of the basic 2-thread litmus tests from the RISC-V litmus-test suite, and we anticipate that adding support for more complex tests or higher numbers of threads would not pose significant engineering difficulties. On the basic 2-thread tests, wall-clock running times range from approximately 20 seconds for the smallest test cases to 3 minutes for the largest; we are able to run all 36 test cases in 50 minutes. Tests were run on a lightly loaded machine with a Haswell i7-5930K CPU and 64GB of DDR4 RAM running Arch Linux. The performance bottleneck here is fully in interaction with Alloy, e.g. spawning a new Java Virtual Machine per query and no doubt tuning Alloy parameters suboptimally.

3.7 Model-checking the decode and execute functions

Support compilation to hardware circuits by carefully tweaking interpreter-style instances to avoid unbounded types.

The riscv-formal project [Wolf 2018] proposes a Verilog description of the Boolean function updating one cycle: assuming a single-cycle machine, it specifies how the register file and the memory are transformed by an arbitrary instruction from the backbone of the base ISA. They also have infrastructure to model-check their Verilog description against other descriptions, for example the standard RISC-V simulator Spike [spi 2020]; and against real processors, using the Yosys tool. As our final case study, we decided to connect our specification to that ecosystem, validating it against the existing riscv-formal specification. It presumably is also possible to check our specification directly against processors using Yosys, though we have not carried out that experiment yet.

The tooling here works directly on Verilog code, so it was convenient to translate our specification into that language. At some level, it forced us to confront challenges that are not fundamental, as a
specification does not actually need to execute as a finite hardware circuit. However, there could be other applications of compiling to hardware, like testing of processor designs on FPGAs, so we felt it was worth investing in this path. We used the Haskell-to-hardware converter Clash [QBayLogic 2020] to transform our specification, using a minimal state-monad instance, into a Verilog Boolean function, and the authors of riscv-formal model-checked that output against their reference riscv-formal to find discrepancies (as revealed by any single instructions of execution from matching initial states).

Interestingly enough, the Clash instance of the specification is quite similar to the Minimal instances. However, the Minimal instances are not directly usable in Clash because they use a Map for the register file, and these potentially arbitrary-sized maps do not normalize well in Clash. Instead, we use the Vector datatypes in Clash. We also fought with instabilities of Clash’s partial evaluation of programs, where sometimes it would fail to notice dead code or otherwise take advantage of predictability of some code spans. As a result, we did make a few more lines of change to our spec just to save Clash some trouble.

4 RELATED WORK

Most recent work on multipurpose ISA specs has employed domain-specific languages toward ends similar to ours. The Sail [Armstrong et al. 2019; Mundkur et al. 2020] language is the highest-profile today for defining ISA semantics. Work there can be helped by specialized features on a spectrum of generality, from examples like dependently typed bitvectors (fairly generic) to specialized support for instructions and their bit-level representations. A DSL in this category requires new tools to translate into specification languages required across use cases, and languages in this tradition had not previously allowed application-agnostic semantics to be first-class objects in logics.

Another DSL specific to the ARM ISA family [Reid 2016] received a lot of attention recently, thanks to systematic adoption for several of ARM’s most important ISA variations. That second DSL has also been translated automatically to Sail. A notable predecessor to Sail was L3 [Fox 2012]. These DSLs have been used for encoding several significant mainstream ISAs beyond RISC-V, and indeed it is possible that our approach would be less appropriate for legacy ISAs with complications and baggage beyond what we had to deal with in RISC-V.

There has also been a good amount of past work writing ISA semantics directly in the languages of proof assistants. For instance, Fox and Myreen [2010] defined and validated an ARM semantics in HOL4. As in our semantics, theirs uses a monadic style for state-threading and incorporation of effects. However, they implemented a single monad, rather than using parameterization over a monad as the central approach to applying one semantics in different use cases. They also performed extensive validation across a few use cases, most notably in automated testing against processors.

Goel and Hunt [Goel 2016; Goel and Hunt 2013] developed a detailed model of x86 in ACL2. Like us, they observed that different use cases impose different constraints on the formalization: On one hand, they want to execute their model efficiently to validate it against real x86 processors, and on the other hand, they want to prove correctness of programs against their x86 model. To bridge between these different requirements, they use an abstract state representation for program verification and a concrete state representation for execution, define correspondence predicates between the two, and prove that all modifications preserve the correspondence. Our approach can be seen as generalizing theirs to consider more than two logic interpretations of a semantics.

Crafting semantics for multicore systems with weak memory models has become a substantial research area in its own right, with some of the earliest work on mainstream ISAs centered at the University of Cambridge [Alglave et al. 2009; Sarkar et al. 2009]. With the Sail language and others, it had already been demonstrated that opcode meanings could be separated from memory-model definitions. Our preliminary results show that the same should work with our semantics style.
ISA semantics is the natural meeting point of software and hardware proofs, though we have been surprised to see how few past multipurpose specifications have been used for substantial proofs on both sides. Considering more single-purpose specs, CompCert [Leroy 2009] includes quite a few assembly-language backends with associated operational semantics (including for RISC-V), as far as we know not reused to reason about hardware. The CakeML project has connected hardware and software proofs via a semantics for the Silver ISA [Lööw et al. 2019], where, to our knowledge, neither that ISA nor its semantics have been applied outside that case study. The other two significant examples of that kind (around bespoke, verification-motivated ISAs) came earlier, in the CLI stack [Bevier et al. 1989] and the VeriSoft project [Alkassar et al. 2008].

The most-involved functional-correctness proofs we know of, connected to prior multipurpose specifications of industrial ISAs, relate to Sail ARM specs, proving correctness of address translation in Isabelle/HOL [Armstrong et al. 2019] (with an ongoing port to Coq [Campbell 2020]) and then capability security of the Morello ISA extension [Bauereiss et al. 2022]. These results are metatheorems about the semantics themselves, which require a different sort of detail-oriented reasoning than proof of particular significant machine-code programs or of processors. In contrast, our specification has been validated through a case study [Erbsen et al. 2021] doing a complete functional-correctness proof for a simple embedded system, connecting proofs of hardware and software parts into a final theorem whose statement does not depend on our semantics. The software and hardware sides of that project are compatible with mainstream RISC-V artifacts: the verified software runs on an off-the-shelf RISC-V microcontroller, while the verified processor also runs RISC-V machine code produced by GCC.

Sail ISA semantics have also recently been connected to program proof with Islaris [Sammler et al. 2022], a framework that uses SMT-based symbolic execution of the semantics to produce more manageable verification conditions, to be discharged in Coq. The verification experience seems to be quite streamlined, though, contra our approach, at least one new trusted translator between languages is involved. The SMT solver is also trusted, rather than somehow using it to generate proofs checkable by Coq. Islaris has been applied successfully to both RISC-V and more complex ARM ISAs.

5 CONCLUSION

We have presented a new approach to formal specification of hardware instruction sets, relying on type classes for easy instantiation to different use cases, thus avoiding any requirement for domain-specific language features. As a result, such a semantics can be written directly in popular general-purpose languages and translated to other forms using tools that are not domain-specific. Our example is for the up-and-coming RISC-V ISA family and has been applied across hardware and software and across different styles of formal methods, without requiring that a single new parser/translator be written to integrate with tools backed by interactive proof (Coq), relational model finding (Alloy), and SMT-based model checking (Yosys).

Some rough edges certainly remain, which should be considered in comparing our approach to that of domain-specific languages, motivating the search for new coding patterns to achieve better modularity in general-purpose languages. We would rather not have our RiscvMachine type class always contain the getFPRegister and setFPRegister primitives. It would be better if they were only present if the floating-point extension is supported, and similarly for makeReservation, checkReservation, and clearReservation required by the atomics extension. The instruction-decode function is quite large, and every property about it that we proved (or tried to prove) in Coq leads to performance issues that require very careful, performance-aware proof engineering.

Nonetheless, this approach allowed for a small arsenal of nontrivial tools to be constructed fairly quickly, and related mechanizations may have a place in future formal-methods ecosystems.
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