Multi-kV class \(\beta\)-Ga\(_2\)O\(_3\) MEFSTEs with a Lateral Figure of Merit up to 355 MW/cm\(^2\)

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Abstract—We demonstrate over 3 kV gate-pad-connected field plated (GPFP) \(\beta\)-Ga\(_2\)O\(_3\) lateral MESFETs with high lateral figure of merit (LFOM) using metalorganic vapor phase epitaxy (MOVPE) grown channel layers and regrown ohmic contact layers. Using an improved low-temperature MOVPE selective area epitaxy process, we show that a total contact resistance to the channel as low as 1.4 \(\Omega\)mm can be achieved. The GPFP design adopted here using plasma-enhanced chemical vapor deposited (PECVD) \(\text{SiN}_x\) dielectric and \(\text{SiN}_x/\text{SiO}_2\) wrap-around passivation exhibits up to \(\sim\)14% improved \(R_{\text{on}}\) up to \(\sim\)70% improved breakdown voltage \((V_{\text{BR}} = V_{\text{DS-VGS}})\) resulting in up to 3x higher LFOm compared to non-FP \(\beta\)-Ga\(_2\)O\(_3\) lateral MESFETs. The \(V_{\text{BR}}\) (2.5 kV) and LFOM (355 MW/cm\(^2\)) measured simultaneously in our GPFP \(\beta\)-Ga\(_2\)O\(_3\) lateral MESFET (with \(L_{\text{do}} = 10\mu\text{m}\)) is the highest value achieved in any depletion-mode \(\beta\)-Ga\(_2\)O\(_3\) lateral device to date.

Index Terms—\(\text{Ga}_2\text{O}_3\), MESFETs, MOVPE, regrown contacts, breakdown, kilovolt, lateral figure of merit, passivation, field plates.

I. INTRODUCTION

\(\text{Ga}_2\text{O}_3\)-based devices have increasingly gained momentum as a potential technology that demonstrates numerous strengths for high voltage/power applications. The high projected breakdown field (~8 MV/cm) of \(\beta\)-Ga\(_2\)O\(_3\) and the availability of high-quality melt-grown \(\beta\)-Ga\(_2\)O\(_3\) bulk substrates offers compelling promise for high efficiency power devices[1]–[6]. The \(\beta\)-Ga\(_2\)O\(_3\)-based device performance has rapidly progressed in both lateral and vertical geometries thanks to the simultaneous progress in high-quality epilayer growth technologies that includes mainly molecular beam epitaxy (MBE), metalorganic vapor phase epitaxy (MOVPE), halide vapor phase epitaxy (HVPE) and low-pressure chemical vapor deposition (LPCVD) as well as device processing techniques [7]–[16]. All of these epitaxial growth techniques, MOVPE has captivated widespread attention due to its versatility and ability to grow comparatively higher-quality epilayers that enables high room-temperature electron mobility values (close to the theoretical limit) and could be promising for fabricating Ga\(_2\)O\(_3\) lateral FETs with high current densities as well as high breakdown voltages [8], [17]–[19].

Many new field management techniques have been successfully demonstrated in lateral \(\beta\)-Ga\(_2\)O\(_3\)-based devices that enabled high-breakdown voltages, high average breakdown fields, and high \((V_{\text{BR}}/R_{\text{on}})\) lateral figures of merit but not simultaneously in the same device [3], [4], [20]. In other words, \(V_{\text{BR}} > 2\text{kV}\), lateral \(V_{\text{BR}}/R_{\text{on}} > 300\text{MW/cm}^2\) and \(E_{\text{BRAVG}} > 2\text{MV/cm}\) could not be achieved simultaneously in the same device. This could be due to a combination of factors such as device design, device processing techniques (bulk or surface leakage paths) and more importantly the epilayer material quality. In this work, we address these issues using a gate-pad connected field plate (GPFP) design using a PECVD deposited \(\text{SiN}_x\) dielectric in a \(\beta\)-Ga\(_2\)O\(_3\) MESFET with MOVPE-grown channel and contact layers.

II. DEVICE GROWTH AND FABRICATION

The epitaxial structure shown in Fig. 1(a) consists of a \(\beta\)-Ga\(_2\)O\(_3\) channel (230 nm thick Si-doped \(\sim 3.6\times 10^{17}\text{cm}^{-3}\)) on a Fe-doped (010) bulk substrate grown using Agnitron Technology’s Agilis 700 MOVPE reactor with TEGa, O\(_2\), and silane (SiH\(_4\)) as precursors and argon as carrier gas. The 10×15 mm\(^2\) edge-defined film fed grown (EFG) semi-insulating Fe-doped (010) Ga\(_2\)O\(_3\) bulk substrate was acquired from Novel Crystal Technology (NCT), Japan. Before the channel layer growth, the substrate was cleaned using HF for 30 mins. From Hall measurement, the channel charge and mobility were measured to be \(5.7\times 10^{12}\text{cm}^{-2}\) and 95 cm\(^2\)/Vs respectively, yielding a channel sheet resistance, \(R_{\text{sh,ch}} = 11.7\ \text{k}\Omega/\square\). The device mesa isolation and the source/drain ohmic contacts were selectively regrown by MOVPE technique using a Ni/SiO\(_2\) mask pattern [21]. The contact recess etch was performed using a low power SF\(_6\)/Ar ICP-RIE dry etching, followed by a quick dip in a diluted BOE solution. The etching
in the contact regions was extended down to the Ga2O3 epitaxial layer with an estimated Ga2O3 trench depths of 10-20 nm (Ga2O3 etch rate ~ 1.5 nm/min). The Si-doping in the regrown n+ layer was ~ 2.6×10^{20} cm^3. Following the contact regrowth process, ohmic metal stack Ti/Au/Ni (20 nm/100 nm/30 nm) was evaporated on the regrown contact regions using photolithography patterning and lift off, followed by a 450°C anneal in N2 for 1.5 mins. Ni/Au/Ni (30 nm/100 nm/30 nm) metal stack was then evaporated to form the Schottky gate for the MESFET structure.

The gate field plate design used in this work is shown in Fig.1(a), where the gate field plate metal was electrically connected to the gate pad (shorted) outside the device mesa, hence, named gate-pad-connected field plate (GPFP). This design was adopted to protect the channel region from the dry-etching plasma that occurs in the conventional gate field plate etch process flow and has been reported to cause plasma-damage induced ON resistance increase [4], [22]. Unlike MOSFETs, due to the absence of any gate dielectric that can act as etch stop/protective layer, avoiding the etch step in the active region played a key role to maintain ON resistance in our FP MESFETs as discussed later. The gate field plate metal was deposited following a SiNx (170 nm thick) passivation layer deposited using plasma-enhanced chemical vapor deposition (PECVD at 300°C). The field plate extension (LFP) was varied from ~ 0.3 to 3.5 µm as the gate-to-drain distance (LGD) varied from 2 to 45 µm. Finally, the whole active region was passivated using an SiN/SiO2 (50 nm/50 nm) bilayer dielectric deposited using the same PECVD (300°C) technique. The SiN/SiO2 wrap-around bi-layer allowed for a thicker overall dielectric passivation with lower SiN thickness to prevent excessive stress in the SiN film. The final device optical image is shown in Fig.1(b). The non-FP MESFET devices had no dielectric surface passivation.

III. RESULTS AND DISCUSSIONS

Fig. 2(a) & 2(b) show the DC output and transfer curves for the GPFP MESFET (solid lines) and the unpassivated non-FP MESFET (dashed lines) for device with dimensions LGD/LGD = 1.0/2.8/2.4 µm. No hysteresis was observed in MESFET (dashed lines) for device with dimensions the GPFP MESFET (solid lines) and the unpassivated non-FP MESFET (dash lines) for device with LGD = 10 µm. The Si-doping in the active region played a key role to maintain ON resistance in our FP MESFETs as discussed later. The gate field plate metal was deposited following a SiNx (170 nm thick) passivation layer deposited using plasma-enhanced chemical vapor deposition (PECVD at 300°C). The field plate extension (LFP) was varied from ~ 0.3 to 3.5 µm as the gate-to-drain distance (LGD) varied from 2 to 45 µm. Finally, the whole active region was passivated using an SiN/SiO2 (50 nm/50 nm) bilayer dielectric deposited using the same PECVD (300°C) technique. The SiN/SiO2 wrap-around bi-layer allowed for a thicker overall dielectric passivation with lower SiN thickness to prevent excessive stress in the SiN film. The final device optical image is shown in Fig.1(b). The non-FP MESFET devices had no dielectric surface passivation.

Fig. 2(d) shows the three-terminal breakdown characteristics at VGS = 20 V for the non-FP MESFETs and the GPFP MESFETs with various LGD values. All the breakdown measurements were performed with the wafer submerged in FC-40 Fluorinert dielectric liquid. Comparing devices with identical LGD values, the GPFP MESFETs show significant improvement in breakdown voltage (VBR = VDS – VGS) over the non-FP MESFETs. The highest measurable VBR recorded was 2462V (LGD = 10µm) for the GPFP MESFET, which is ~70% higher compared to the non-FP MESFET (1462V) of the same dimension showing the efficacy of the FP design demonstrated here. The reverse leakage current rise was mainly due to gate leakage for both types of MESFETs. Fig. 2(e) and 2(f) show the OFF-state gate and drain terminal currents of the non-FP and GPFP MESFETs respectively with LGD of 10 µm, showing that the leakage current is dominated by the gate leakage before the catastrophic breakdown.
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The lateral figures of merit (V BR²/ron,sp) of the GPFP MESFETs were calculated, where ron,sp is RON normalized to the device length (LSD +2LT). The LFOM values for the GPFP and non-FP MESFETs are plotted as a function of L GD. The highest LFOM of 355 MW/cm² was calculated for GPFP MESFET (V BR = 2462V, ron,sp = 17.05 mΩ.cm²) with an L GD of 10 µm which is more than 3× higher compared to the non-FP MESFET (LFOM = 115 MW/cm², V BR = 1466V, ron,sp = 18.6 mΩ.cm²). Overall, the GPFP design is found to have 2-3 times higher LFOM compared to the non-FP design. This is because of the improved ron,sp (up to 14% lower) and V BR (up to 70% higher) values simultaneously with the GPFP design. Given the GPFP MESFET with L GD = 20 µm have V BR >3 kV, these devices can demonstrate LFOM >200 MW/cm² for >3kV class transistors.

IV. CONCLUSION

We demonstrate gate-pad connected field plated MOVPE-grown kV-class β-Ga2O3 lateral MESFETs with high LFOM and E BR,AVG using PECVD deposited SiN x and SiO 2 field/passivation dielectrics. A record high LFOM of 355 MW/cm² with a V BR of ~2.5 kV and E AVG of ~2.5 MV/cm simultaneously is demonstrated in a GPFP β-Ga2O3 MESFET with L GD = 10 µm. This LFOM value is the highest for any β-Ga2O3 lateral device with V BR > 2kV. These devices show great potential of MOVPE-grown β-Ga2O3 FETs for future high-voltage applications in the low to medium voltage range.
