On the performance characterization of silicon MOSFETs on 4° off-axis substrate

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Abstract: Circular metal-oxide-semiconductor field-effect transistors (MOSFETs) with various gate dimensions are fabricated on 4° off-axis and regular (100) silicon substrates. The influences of substrate orientation, gate length and width on the dc performance of the MOSFETs are investigated and the underlying mechanism is discussed. The on/off ratio, threshold voltage, field effect mobility, transconductance and drain current are compared and the differences can be explained by the interface state density and the surface roughness scattering. The results provide guidelines for the optimization and reliability of the MOSFETs on the off-axis silicon wafers.

Keywords: 4° off-axis, gate length, gate width, MOSFETs, mobility, transconductance

Classification: Electron devices, circuits and modules

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1 Introduction

Silicon (Si) substrate rotated a few degrees off-axis has been widely studied and used over the past few decades. The major reason is that high quality III-V
semiconductor materials can be directly grown on it [1, 2, 3]. This enables great possibilities of monolithic integration of the III-V devices (as well as optoelectronic and microelectronic devices) with silicon devices [4, 5, 6, 7]. Considering that the MOSFETs are the major microelectronic devices for the integration, it is necessary to investigate the performance of MOSFETs on off-axis substrates. Characteristics of the MOSFETs are strongly dependent on the wafer orientation [8, 9, 10, 11, 12] and oxide thicknesses [13]. In particular, the crystallographic orientation of the interface has a strong impact on the performance of the vertical channel MOSFETs for extremely high density memories [14]. It was also found that gate leakage current and 1/f noise of MOSFETs were sensitive to off-axis substrates [15]. The characteristics and reliability of the oxides and MOSFETs have been investigated on silicon substrates with off-axis angle ranging from 0° to 8° [16, 17, 18]. It has been found that the surface roughness and difference in transconductance and mobility between MOSFETs on the off-axis and (100) silicon wafers is a monotonically increasing function of misorientation angle (0° to 8°) [16]. In particular, silicon wafers with a misorientation angle of 4° or 6° are mostly used for the hybrid-integration purpose for the reason that they effectively reduce the step spacing and mismatch of the silicon and III-V lattices, thus enable high efficiency of the semiconductor lasers. Therefore we choose a silicon substrate with 4° rotated around the [011] axis as a representative example to compare the performance of MOSFETs with devices on regular (100) substrate. Few works have been done on the detailed characterization and comparison of MOSFETs with various gate lengths and widths on different Si wafer orientations. This study presents the fabrication, dc characterization and performance comparison of circular n-MOSFETs with various gate lengths and gate widths on regular (100) and 4° off-axis silicon substrates. Influences of off-axis plane, gate length and width on the performance of MOSFETs are investigated and the underlying mechanism is discussed.

2 Device fabrication

The substrates used in this study are lightly boron-doped (≈5 × 10^{14} \text{cm}^{-3}), p-type silicon (100) wafers and 4° off-axis silicon wafers, the crystalline plane of which is rotated by 4° around the [011] axis. Circular n-MOSFETs with different gate lengths of 3, 6, 9 μm and gate diameters of 74, 94, 100 μm were fabricated on the two substrates. Identical fabrication processes are used for the circular gate MOSFETs on 4° off-axis and regular silicon substrates. Fig. 1 shows an optical microscope image and cross-section schematic of the circular MOSFETs on 4° off-axis silicon substrates.

The process begins with the growth of ≈35 nm thick gate oxide (relatively thin oxide with no gate leakage current and can provide higher transconductance (gm) and mobility) on the two substrates by dry oxidation in the furnace at 1050 °C for 30 minutes in N₂/O₂ ambient and the SiO₂ thickness is considered to be same on the two wafers. Then the circular-shape gates with different gate dimensions are patterned by optical lithography. We choose the circular gate MOSFET to measure the transconductance or mobility value averaged over all the electric field direc-
tions. In this way, we can compare the performance of only one type of MOSFETs on two substrates instead of MOSFETs built on multiple channel directions. Identical fabrication processes on both substrates and the circular-shape gate of the MOSFETs enable us to perform a comparison between devices independent of the channel orientation and thus the 4° off-axis substrate orientation is the only difference. Gate electrode stack consisting of Ti/Au is formed by e-beam evaporation and lift-off process. After that, self-aligned (by gate) high-energy high-dosage (4 × 10¹⁵ cm⁻³) phosphorus ion implantation was performed for the source and drain regions on the two substrates followed by rapid thermal annealing at 700 °C for 1 min. The source/drain regions are then patterned and the thermal oxide is etched by buffered hydrofluoric acid (HF) solution. Finally, a ~10/120 nm Ti/Au stack layer is evaporated for the source/drain electrodes (the circle electrodes are the drains).

### 3 Results and discussions

Direct current (dc) characteristics of circular MOSFETs with gate lengths of 3, 6, 9 µm and same gate width of 295 µm on the regular and 4° off-axis substrates were measured and shown in Fig. 2. From Figs. 2(a)–(c), considerable reduction of the peak $g_m$ is observed for the MOSFETs on the off-axis substrate compared to those with same gate dimensions on the regular substrate. The field-effect mobility ($\mu_{FE}$) can be calculated by

$$\mu_{FE} = \frac{g_m L}{(C_{OX} V_{DS} W)}$$

Where $C_{OX}$ is the oxide capacitance, $V_{DS}$ is the drain-source voltage, $L$ is the gate length, $W$ is the gate width. Table I lists the values of $g_m$ and $\mu_{FE}$ of MOSFETs on the two substrates for different geometries.
The obtained mobilities are in a reasonable range, but relatively lower. This is possibly due to that the ion implantation, doping profile and annealing conditions.
are un-optimized, thus the parasitic source/drain contact and series resistances are higher. And as the gate geometries increase, the width of source/drain electrodes increase, thus the resistance of the source/drain slightly decreases, leading to a slightly higher $g_m$ and mobility. More importantly, the lower $g_m$ and mobility of MOSFETs on the off-axis wafer (compared to that on regular one) is mainly due to the more severe surface roughness scattering in the off-axis wafer. The off-axis surface has tilt-induced atom steps on the vertical direction to the rotation axis, resulting in a larger surface roughness, and the amount of surface roughness increases as the tilt angle increases [16]. The effect of surface roughness scattering on the transconductance and mobility between the 4° off-axis and regular (100) substrates has been examined by ensemble Monte Carlo simulations [10]. The roughness is described by an exponential autocovariance function, $\langle \delta(r)\delta(r - r')\rangle = \Delta^2 e^{-\sqrt{2}\tau/\lambda}$, where $\delta(r)$ is a local deviation of the Si/SiO$_2$ boundary position from a perfect plane as a function of the in-plane coordinate $r$, $\Delta$ is the rms value of $\delta(r)$, and $\lambda$ is the correlation length. The function is used to fit the mobility values extracted from experimental data with various gate dimensions. The obtained surface roughness parameters are $\Delta = \sim 5$ Å, $\lambda = \sim 4$ nm for the (100) substrate, and $\Delta = \sim 5.4$ Å, $\lambda = \sim 4.3$ nm for the off-axis substrate. Larger $\Delta$ and $\lambda$ indicates rougher interface, and thus the transconductance and mobility become lower.

The $g_m$ difference (also mobility difference) between the MOSFETs on the two substrates is calculated to be 7.5%, 18%, 21% with a gate length of 3, 6, 9 µm. The $g_m$ and mobility differences ($\Delta g_m$ and $\Delta$mobility: $\Delta g_m = \frac{g_m(\text{regular}) - g_m(\text{off-axis})}{g_m(\text{regular})} \times 100\%$, $\Delta$mobility = $\frac{\text{mobility(regular)} - \text{mobility(off-axis)}}{\text{mobility(regular)}} \times 100\%$) become larger as the gate length increases, mainly due to the surface roughness scattering effect [10]. Although the surface roughness is independent of the gate length, the influences of the different surface roughness on the MOSFETs performance on different substrates become larger as the gate length becomes larger. In addition, as the channel length gets shorter while $V_G-V_{th}$ and $V_{DS}$ are kept constant, the total inversion sheet charge density and the average effective field from the gate decrease, while the average distance of carriers from the rough surface slowly increases. Therefore, there are fewer scattering carriers among all the carriers as the gate length is decreasing. Therefore, the $g_m$ difference between the two substrates caused by scattering decreases as the gate length is decreasing. Furthermore, the effective channel resistance decreases as the gate length becomes smaller, thus the channel resistance becomes a smaller component of the total device resistance. As the different surface roughness has more influence on the channel region, the total $g_m$/mobility difference becomes smaller as the gate length decreases.

The $\Delta g_m$ and $\Delta$mobility decrease as the gate width increases with the consistent reason. The effective channel resistance becomes smaller with larger gate width, therefore the channel resistance becomes a smaller component of the total device resistance. As a result, the total $g_m$/mobility difference becomes smaller as the gate width increases, since the surface roughness has more influence on the channel region.

As shown in the inset panel of Fig. 2, the drain current decreases as the gate length increases for the MOSFETs on both substrates. And the degradation of drain current is larger for MOSFETs on the off-axis substrate than those on the regular
substrate. In addition, at same dc bias (i.e. same gate voltage ($V_G$) and drain voltage ($V_D$)), the drain current ($I_D$) of the MOSFETs on the off-axis substrate has no determined relationship than those on the regular substrate. This is because of the different threshold voltage and channel mobility for the MOSFETs on the two substrates, and is consistent with the $I_D$-$V_G$ relationship. The on/off ratios of the off-axis and regular circular MOSFETs are similar ($\sim 10^7$), as shown in Figs. 3(a)–(c). The result indicates that the devices on off-axis substrates are properly functioning in the normal range.

Comparisons of the circular MOSFETs on the regular and off-axis substrates with different gate widths are also shown in Figs. 4 and 5. For the MOSFETs on the $4^\circ$ off-axis substrate, the peak $g_m$ and channel mobility increase as the gate width increases. Fig. 4 shows $g_m$ (mobility) difference between the MOSFETs on the two substrates, changing with various gate lengths and widths. Fig. 6 shows the transconductance and mobility difference for the MOSFETs with various gate dimen-

![Saturation transfer (drain voltage is 3 V) characteristics of the MOSFETs with different gate lengths (same gate width $W_G = 295 \, \mu m$) on the 4° off-axis Si substrate (blue solid curves) and regular (100) Si substrate (red dashed curves). (a) $L_G = 3 \, \mu m$. (b) $L_G = 6 \, \mu m$. (c) $L_G = 9 \, \mu m$.](image)
Fig. 4. \(I_D\), \(g_m\)-\(V_G\) and \(I_D\)-\(V_D\) (the inset) characteristics of MOSFETs with different gate widths (same gate length \(L_G = 3 \mu m\)) on the 4° off-axis Si substrate (blue solid curves) and regular Si substrate (red dashed curves). (a) \(W_G = 232 \mu m\). (b) \(W_G = 295 \mu m\).

Fig. 5. Characteristics of MOSFETs with different gate widths (same gate length \(L_G = 6 \mu m\)) on the 4° off-axis Si substrate (blue solid curves) and regular Si substrate (red dashed curves). (a) \(W_G = 232 \mu m\). (b) \(W_G = 295 \mu m\).
sions on the off-axis and regular substrates. As shown in Figs. 4 and 6, the degradation of the $g_m$ and $\mu_{FE}$ of the MOSFETs on the off-axis substrate (compared to that on the regular substrate) becomes smaller as the gate width increases. In the inset of Fig. 4, we can see that the drain currents increase as the gate width increases, for MOSFETs on both substrates at same bias. And the increment is larger for the MOSFETs on off-axis substrate than those on regular substrate. Fig. 5 shows the consistent results with Fig. 4.

Furthermore, from Figs. 2, 4 and 5, we can see that the threshold voltages ($V_{th}$) of the MOSFETs on the 4° off-axis substrate ($\sim-2.65$ V) are $\sim0.5$ V lower than those on the regular substrate ($\sim-2.15$ V). The different $V_{th}$ is mainly due to a different concentration of interface states. The subthreshold slope ($S$, mV/decade) can be extracted from the log ($I_D$) versus $V_G$ curves with a low value of $V_D$. And the interface state density ($D_{it}$) can be approximately calculated by the following equations [17, 18]:

$$S = \frac{kT}{q} \ln 10 \cdot \left(1 + \frac{C_{it}}{C_{OX}}\right) \quad (2)$$

$$C_{it} = qD_{it} \quad (3)$$

Where $C_{OX}$ is the oxide capacitance. The extracted subthreshold slope $S$ of the MOSFETs with the gate length of 9 µm and gate width of 295 µm is $\sim240$ and 200 mV/decade on the off-axis and (100) substrates, respectively. And the calculated $D_{it}$ from equations (2)–(3) is $\sim1.9 \times 10^{12}$ and $1.6 \times 10^{12}$ eV$^{-1}$ cm$^{-2}$ for the off-axis and regular (100) substrates, respectively. The extracted $D_{it}$ is similar for the MOSFETs of other gate dimensions, which is consistent with the result that the threshold voltage is kept similar for devices with all gate dimensions. Table II lists the values of $D_{it}$ and $V_{th}$ of the MOSFETs on the two substrates with gate lengths of 3, 6, 9 µm.

The higher $D_{it}$ (or smaller threshold slope) than the values reported in the works [16, 17] is possibly due to the annealing condition (lower temperature and shorter time) for ion implantation and circular shape gate in this work. The $D_{it}$
The difference between the off-axis and (100) substrates is similar for the MOSFETs with all gate dimensions. This maybe leads to the similar threshold voltage shift of the MOSFETs on the off-axis and regular (100) substrates. One reason of the different interface state density is that the off-axis wafer has a larger surface roughness than the on-axis wafer. The interface state density depends strongly on the orientation of the substrate. And the larger surface roughness of the off-axis substrate is mainly due to the higher density of steps formed by vicinal planes. This leads to enhanced Coulomb scattering and hence to reduced mobility at lower effective fields, which is consistent with the previous discussion [14, 15]. The microroughness at Si/oxide interfaces affects the interface state density: the interface state density of an atomically smooth interface is much lower than that of an atomically rough interface [16, 19]. The correlation between the Dit and Vth is explained as follows:

With the application of a negative bias to the gate electrode, both the conductor/valence energy level and interface state energy level near the Si/SiO2 interface bend upward. When the donor energy level below the Fermi level rise to the upper position, no electrons are filled in the donor type of the interface state (the accepter energy level below the Fermi level is presented as neutral when rise to the upper position), therefore the interface state is presented as positive which will compensate part of the negative charges from the gate electrode. Hence the trends of band bending and holes accumulation are weakened. As a result, more negative gate voltage (V_G) (or larger absolute value |V_G|) needs to be applied to the gate electrode to achieve the same inversion state, when Dit is larger. Therefore a more-negative shift of the Vth is observed. On the other hand, with the application of a positive bias to the gate electrode, the higher positive voltage (V_G) should be applied to the gate electrode to achieve the same state, when Dit is larger. A larger positive voltage should be applied to the enhancement mode n-MOSFET (positive Vth) gate with larger Dit.

For the p-MOSFETs, similar performance relations are expected as the n-MOSFETs on the off-axis and regular silicon substrates. However, due to the different transport and mobility between electrons and holes in different channel directions, the actual performance difference could be different for the p-MOSFETs and the n-MOSFETs on off-axis and regular substrates.

| MOSFET    | Regular | Off-axis | Regular | Off-axis | Regular | Off-axis |
|-----------|---------|---------|---------|---------|---------|---------|
| L (µm)    | 3       | 3       | 6       | 6       | 9       | 9       |
| W (µm)    | 295     | 295     | 295     | 295     | 295     | 295     |
| Dit (eV⁻¹ cm⁻²) | 1.48 * 10¹² | 1.89 * 10¹² | 1.52 * 10¹² | 1.90 * 10¹² | 1.61 * 10¹² | 1.92 * 10¹² |
| Vth (V)   | -2.49   | -2.99   | -2.54   | -3.02   | -2.58   | -3.08   |

Table II. Interface state densities and threshold voltages of the MOSFETs with various gate dimensions on the 4° off-axis and regular substrates.
4 Conclusion

In summary, circular MOSFETs with various gate lengths of 3, 6, 9 µm and gate widths of 232, 295, 320 µm are fabricated on the regular (100) and 4° off-axis silicon substrates. Dc characteristics have been investigated and compared between the MOSFETs on different substrates, gate lengths and gate widths. On/off ratios of the circular MOSFETs on the off-axis and regular substrates are similar, regardless of the gate dimensions. The mobility and transconductance $g_m$ difference between the MOSFETs on the off-axis and regular substrates decreases with smaller gate length while increases with smaller gate width. Different surface roughness scattering in the off-axis and regular wafers is believed to be the major reasons.

The saturation current of MOSFETs on the two substrates decreases with larger gate length while increases with larger gate width, and the change is bigger for MOSFETs on off-axis substrate than those on regular substrate. The threshold voltage of the MOSFETs on the off-axis substrate is $\sim$0.5 V lower than those on the regular substrate, and is also independent of the gate length or width. The major reason for the threshold voltage variation is due to higher interface trap density in the off-axis wafer. Higher interface trap density is also expected to induce larger threshold voltage for the enhancement mode MOSFETs. The results provide useful guidelines for the optimization and reliability of the MOSFETs on the off-axis silicon wafers.
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