Fabrication and Electrical Characterization of Fully CMOS-Compatible Si Single-Electron Devices

P. J. Koppinen, M. D. Stewart, Jr., and Neil M. Zimmerman

Abstract—We present electrical data of silicon single-electron devices fabricated with CMOS techniques and protocols. The easily tuned devices show clean Coulomb diamonds at $T = 30 \text{ mK}$ and a charge offset drift of $0.01e$ over eight days. In addition, the devices exhibit robust transistor characteristics, including uniformity within about $\pm 0.25 \text{ V}$ in the threshold voltage, gate resistances greater than $10 \text{ G}\Omega$, and immunity to dielectric breakdown in electric fields as high as $4 \text{ MV/cm}$. These results highlight the benefits in device performance of a silicon-foundry-compatible process for single-electron device fabrication.

Index Terms—Complementary metal–oxide–semiconductor (CMOS), Coulomb blockade, quantum dot, silicon-on-insulator (SOI), single-electron transistor, single-electron tunneling (SET).

I. INTRODUCTION AND MOTIVATION

SINGLE-ELECTRON tunneling (SET) devices [1] are promising candidates for a wide variety of nanoelectronics applications, such as sensitive electrometers [2], thermometers [3], electron pumps and turnstiles for current standards [4], [5], and quantum bits for quantum information processing [6]–[8]. In recent years, silicon has drawn a lot of attention as a candidate for practical SET devices for several reasons. These advantages include compatibility with complementary metal–oxide–semiconductor (CMOS) processing, good electrostatic control of the tunnel barriers [9], greater device stability as demonstrated by a lack of charge offset drift [10]–[12], and a relative lack of nuclear spins, an important source of decoherence in spin-based quantum information applications [13].

However, to become truly viable in any of these applications, devices must be manufactured which overcome the device-to-device variations and low yield associated with the processing of typical of small-scale research programs. At the single device level, the gate voltage variation from one device to another may not be an important parameter; however, uniform device operation becomes crucial when trying to operate several SET devices simultaneously, e.g., in the large-scale integration of SET devices. The choice of device architecture can also impact the integrability of devices. For example, gate-to-gate variations in an architecture where more than one gate [7], [14] controls a single tunnel barrier can make finding the desired operating point a laborious iterative process.

In this paper, we demonstrate robust behavior and good uniformity of easily tuned fully CMOS single-electron devices, which contain only silicon, thermally grown silicon dioxide ($\text{SiO}_2$), and phosphorous-doped polycrystalline silicon (poly-Si) in the active device region. The motivation for a fully CMOS approach to fabrication is twofold: 1) to minimize the number of impurities and defects near the active device region and 2) to avoid the instabilities associated with metallic oxides and, in particular, aluminum oxide. In this way, we avail ourselves of the best opportunity to fabricate uniform robust devices. In the following, we will discuss and demonstrate the robustness of our devices with respect to basic metal–oxide–semiconductor field-effect transistor (FET) (MOSFET) characteristics and SET device operation. In particular, we show that these devices exhibit only small variations of the threshold voltage from device to device, dielectrics which are robust against breakdown, and charge offset stability on the order of $0.01e$ over a period of several days.

II. OPERATING PRINCIPLE OF THE DEVICE AND FABRICATION

Our devices each contain a lightly boron-doped (p-type) mesa-etched single-crystal Si nanowire, n$^+$-type source and drain, and two layers of gates; see Fig. 1(a). The topmost gate layer, which we call the upper gate (UG), covers the entire device between the heavily doped source and drain. Applying a positive voltage to the UG inverts the underlying Si nanowire and provides conduction. The second gate layer, which we call the lower gates, consists of three finger gates which wrap around the Si nanowire. These are denoted as LGS (closest to the source), LGC (center gate), and LGD (closest to the drain); see Fig. 1(b). The LG fingers are primarily used to locally deplete the electron gas and, therefore, to create electrostatically controlled tunnel barriers (LGS and LGD), or to modulate the electrostatic potential of a quantum dot (LGC).

1We use “fully CMOS” as a shorthand to indicate that our techniques and protocols are compatible with CMOS processing and avoid metals and dopants near the QDs as in silicon foundries; we do not intend this phrase to imply that our process flow can be implemented without modification in any specific CMOS node.

2We note that, as discussed later, yield issues drove us to use long gates and large dots for this first fabrication run. These large dot sizes also precluded the possibility of achieving the few electron regime.
Fig. 1. (a) Schematic view of a sample. Device operation is described in the text. (b) (Left) Optical micrograph of a sample. (Right) SEM micrograph (before UG deposition) of the active device area, and schematics of an electrical measurement circuit (does not show $V_{UG}$). Lower gates LGS, LGC, and LGD are poly-Si, and the conducting channel (S/D) is single-crystal Si. Channel and lower gates sit on top of the buried silicon oxide (BOX). The white arrow next to the finger gate indicates the gate length. (c) Cross-sectional SEM image of a device along the dashed white line in (b). The darker areas are Si, the gray areas are SiO$_2$, and the bright layer on top is a protective layer of Pt deposited prior to the FIB cut.

The devices are fabricated on a 150 mm silicon-on-insulator (SOI) wafer, with a doping density of about $10^{15}$ cm$^{-3}$, an initial SOI thickness of 100 nm, and a buried oxide (BOX) thickness of 200 nm. To minimize the interface trap density at the gate oxide interface of the nanowire [15], [16], we fabricate the SOI nanowires at a 45° angle with respect to the flat ($\langle 110 \rangle$) of the wafer in order to obtain a $\langle 100 \rangle$ crystallographic equivalent orientation on each facet of the nanowire.

As previously mentioned, we fabricate these devices with a fully CMOS process flow developed at the Center for Nanoscale Science and Technology nanofabrication user facility at the National Institute of Standards and Technology.

Fig. 2. Flowchart of the condensed fabrication process described in the text. The fabrication process is shown in Fig. 2. To put our work in context, our processing differs from others [14], [17]–[19] in that we avoid metal gates and their associated lower quality metal oxides in favor of Si, poly-Si, and high-quality thermal SiO$_2$. Moreover, unlike other fully CMOS efforts [20], we also avoid deliberately placing dopants near the Si quantum dots. The nanowire, lower gate, and upper gate lithography and etching were performed with negative tone electron beam lithography using hydrogen silsesquioxane as a resist and dry etching in Cl$_2$ chemistry. Our etch recipe was to first condition the chamber by performing a 15 min clean on a dummy Si wafer and then perform our etch with 50 sccm of Cl$_2$, 20 sccm of O$_2$, 50 W RF power, 5 mtorr pressure, and zero ICP power. Source and drain areas located about 10 $\mu$m away from the active device area were implanted with phosphorous at 30 keV with a dose of $10^{15}$ cm$^{-2}$. We grew sacrificial oxide on both the
nanowire and the lower gate layer in order to remove possible etch damage produced during the dry etch. Both the sacrificial oxide and the gate oxide on the nanowire were grown in a tube furnace at 850 °C and 950 °C, respectively, with a 20 min anneal in N₂ at the oxidation temperature to reduce the charge density in the oxide. The sacrificial oxide was removed with a short 100 : 1 HF dip. The lower gate and upper gate layers were 75 nm thick in situ phosphorous-doped poly-Si deposited by low-pressure chemical vapor deposition (LPCVD) at 625 °C. Both gate layers were degenerately doped to ensure electrical conduction at low temperatures with a typical resistivity of 10–30 mΩ cm (determined from two terminal measurements at 2.2 K). The sacrificial oxide on the lower gate and the isolation oxide between the lower gate and the upper gate were grown with rapid thermal oxidation (RTO) at 1000 °C. The final steps of the process were metallization of ohmic contacts with sputter-deposited Al–1% Si and a forming gas anneal at 425 °C for 30 min. Except for the addition of sacrificial oxidation and stripping, the basic processing is the same as that in [12] but differs in several details. We note that the devices presented here possess superior performance to those in [12].

To date, we have fabricated devices on two 150 mm wafers which we call A and B; see Fig. 2. The main differences between the wafers are the nominal gate oxide thickness and the finger gate lengths. The SOI nanowire width and length are 70 and 800 nm, respectively, for both wafers. Each wafer contained 48 dies: 36 with two devices as in Fig. 1 on each and 12 diagnostic dies located on the diagonals of the wafer. The diagnostic dies contained conventional FETs with a 70 nm wide SOI nanowire as a channel and test structures to measure the resistance of ohmic contacts and the resistivity of the poly-Si.

A cross-sectional SEM image produced by a focused ion beam (FIB) cut along the LGC finger [the white dashed line in Fig. 1(b)] of a finished device is shown in Fig. 1(c). The darker areas in the micrograph are Si, and the gray areas are SiO₂. The cross-sectional image shows that both poly-Si films of upper gate and lower gate layers conformally coat the layers underneath as is expected from LPCVD growth and that the oxides are continuous, as needed for electrical isolation.

III. RESULTS AND DISCUSSION

We characterized many devices and FETs from randomly chosen dies across both wafers at room temperature and at 2.2 K. In addition, one of the devices was cooled down and measured in a dilution refrigerator at 30 mK. The summary of the electrical characterization is presented in Table I.

| Test                          | Wafer A result | # tested | Wafer B result | # tested |
|-------------------------------|----------------|----------|----------------|----------|
| Threshold voltage value and uniformity at 300 K | [-0.4 V, -0.1 V] | 8        | [-0.1 V, 0.3 V] | 4        |
| Threshold voltage value and uniformity at 2.2 K  | [0.2 V, 0.4 V] | 3        | [0.5 V, 1 V]   | 4        |
| LG Turn–off voltage value and uniformity at 300 K | –               | –        | [-1.5 V, -1 V] | 4        |
| LG Turn–off voltage value and uniformity at 2.2 K  | –               | –        | [-1 V, -0.5 V] | 4        |
| On/off ratio ⁵                  | 10⁴            | 8        | 10⁴           | 4        |
| Subthreshold slope (300 K)     | –              | 80 mV/decade | 4              |
| UG-channel leakage ⁶           | >10 GΩ at ± 0.25 MV/cm | 7/8⁴    | >10 GΩ at ± 4 MV/cm | 4/4⁴    |
| UG breakdown ⁶                 | no breakdown at ± 2.5 MV/cm | 2/2⁴    | 2 breakdown at ± 4 MV/cm | 2/2⁴    |
| LG–UG leakage ⁶                | >10 GΩ at ± 0.4 MV/cm | 24/24⁴  | >10 GΩ at ± 4 MV/cm | 46/49⁴  |
| LG breakdown ³                 | no breakdown at ± 4 MV/cm | 6/6⁴    | no breakdown at ± 4 MV/cm | 46/49⁴  |
| Functional nanowires           | 8              | 8        | 4              | 4        |
| Functional LG fingers          | 0              | 24       | 12             | 12       |

Notes: ⁵ One sample on wafer A showed leakage resistance of 100 MΩ to the channel.
⁶ Breakdown generated threshold voltage shift after the voltage excursion.
⁷ Breakdown generated leakage path.
⁸ number tested that showed the result/total number tested.

аблица 1: Сводка характеристик подложек

| Тест | Результат Wafer A | # Измерений | Результат Wafer B | # Измерений |
|------|-------------------|-------------|-------------------|-------------|
| Напряжение смещения в вакууме при 300 К | [-0.4 В, -0.1 В] | 8           | [-0.1 В, 0.3 В] | 4           |
| Напряжение смещения в вакууме при 2.2 К | [0.2 В, 0.4 В] | 3           | [0.5 В, 1 В] | 4           |
| Угловые электрические характеристики сброса при 300 К | – | – | [-1.5 В, -1 В] | 4           |
| Угловые электрические характеристики сброса при 2.2 К | – | – | [-1 В, -0.5 В] | 4           |
| Отношение на/от | 10⁴ | 8 | 10⁴ | 4 |
| Подпороговой порог (300 К) | – | 80 мВ/декада | 4 |
| Потенциал излучения UG ⁶ | >10 GΩ при ± 0.25 MV/cm | 7/8⁴ | >10 GΩ при ± 4 MV/cm | 4/4⁴ |
| Потенциал разрыва UG ⁶ | нет разрыва при ± 2.5 MV/cm | 2/2⁴ | 2 разрыва при ± 4 MV/cm | 2/2⁴ |
| Потенциал излучения LG–UG ⁶ | >10 GΩ при ± 0.4 MV/cm | 24/24⁴ | >10 GΩ при ± 4 MV/cm | 46/49⁴ |
| Потенциал разрыва LG ³ | нет разрыва при ± 4 MV/cm | 6/6⁴ | нет разрыва при ± 4 MV/cm | 46/49⁴ |
| Наноразмерные нити | 8 | 8 | 4 | 4 |
| Ноги LG | 0 | 24 | 12 | 12 |

Примечания: ⁵ Один образец на wafer A показал утечку сопротивления 100 МОм к каналу.
⁶ Разряд, созданный скачком напряжения после сброса напряжения.
⁷ Разряд, созданный путем образования разряда.
⁸ Количество проб, которое дало результат/общее количество проб.

В панели 1: Сводка характеристик подложек
slope is 60 mV/decade [22]) with an on/off ratio of $10^4$; see the inset in Fig. 3(a). Typical turn-off characteristics for each of the finger gates (LGS, LGC, and LGD) measured at both room temperature and 2.2 K for wafer B are shown in Fig. 3(b). The room-temperature data were taken with an upper gate voltage $V_{UG} = 1.3$ V, while the low-temperature data were taken with $V_{UG} = 2$ V. The ranges for turn-off voltages, i.e., the lower gate voltage $V_{LG}$ at 100 pA of drain current $I_D$, were from $-1.5$ to $-1$ V at room temperature and $-1$ to $-0.5$ V at 2.2 K for all measured lower gates for all devices.

We also tested the robustness of the gate oxide and the isolation oxide on wafer B. In these tests, the gate voltage was swept in steps up to $\pm 10$ V while the source-drain and leakage currents were simultaneously measured to the other gates and to the channel. All leakage resistances between the channel and either layer of gates or between gates were $> 10$ GΩ up to gate voltages of $\pm 10$ V. After each gate voltage excursion, the turn-on characteristics were remeasured in order to determine if there was a change in the threshold voltage or slope. Diagnostic FETs were immune to electric fields up to 4 MV/cm ($\pm 10$ V), showing no change in $V_T$ nor generation of a leakage path (Fig. 4). Similar robustness measurements for SET devices showed no threshold shift up to 2.8 MV/cm ($\pm 7$ V) and only a small ($0.05$ and $0.2$ V) threshold shift after a gate excursion of 4 MV/cm ($\pm 10$ V) in two out of four devices. No observable leakage path developed during the sweep. A typical literature value of the breakdown field of metal–oxide–semiconductor capacitors is about 10 MV/cm, before generating a leakage path [23]. We also performed robustness measurements of the isolation oxide between the lower gates and the upper gate on about 50 different lower gate fingers on different devices across the wafer. Only three fingers developed a breakdown path during the $\pm 10$ V sweep.

Previously, we have discussed the robustness and uniformity of devices in terms of MOSFET performance, and in the following, we present device characteristics when operated in a single-electron device mode. First, we discuss ease of tuning. The right-hand side of Fig. 1(b) shows a schematic of a typical measurement circuit for a device. Tuning the device to display SET oscillations took very little time, on the order of minutes, because there was very little cross-capsitance between gates and each barrier was controlled by a single gate voltage. To tune a device into SET mode, we first applied a small bias voltage to the drain (on the order of 1 mV) and set the upper gate to a voltage (obtained from a short upper gate sweep, typically about 2 V) which gave about 1 nA of current. Next, a two dimensional sweep of $V_{LGS}$ and $V_{LGD}$ (with $V_{LGC}$ well above the turn-off voltage) was performed to find the voltages where each of these gates began to turn off conduction. Typically, the barrier voltages were about $-0.6$ V. We note that barrier resistances responded symmetrically to $V_{LGS}$ and $V_{LGD}$ after fine-tuning $V_{LGS}$ and $V_{LGD}$, we measured SET oscillations by sweeping $V_{LGC}$ with the other gate voltages fixed.
of the island and material restrictions. To further improve the usefulness of these devices as current standards and quantum information processors, our next tasks include the following: 1) substantially increasing the yield and 2) making shorter finger gates so that the gate begins to turn off conduction (the inset of Fig. 7).

While the previous results indicate that the cleanliness of our CMOS fabrication is quite good, many devices in this first device run failed electrically either by not turning on or through an inability to turn off conduction with the LG fingers. This drove our yield of fully functioning (in which we were able to measure intentional Coulomb blockade) devices down to 4/34 devices measured. We have been able to identify the gross fabrication failures, by cross-sectioning devices with FIB in conjunction with the electrical results. In brief, the failure modes are the result of overoxidation of the SOI nanowire and the LG fingers, as well as the overall amount of oxide removed in the processing. We believe that further development of our process flow will ameliorate these failures.

IV. SUMMARY AND CONCLUSIONS

In summary, we have demonstrated devices which show good uniformity in electrical characteristics from device to device within a wafer and between wafers. Moreover, the devices are quite robust against dielectric breakdown up to electric fields of 4 MV/cm. Finally, and most importantly, when operated as a single-electron device, these devices show very stable behavior. Taken together, these characteristics indicate a relatively clean and stable electrostatic environment throughout the fabrication process. We attribute these successes to the minimization of impurities and defects which result from our CMOS processing and material restrictions. To further improve the usefulness of these devices as current standards and quantum information devices, our next tasks include the following: 1) substantially increasing the yield and 2) making shorter finger gates so that we can use those gates both to generate barriers and as plunger gates.

While these results indicate that a fully CMOS process pays dividends in device performance, it also complicates the
Fig. 7. (a) Example of single-electron oscillations taken at different times spanning the total duration of charge offset drift measurements; curves are offset vertically for clarity. (b) Charge offset drift derived from Coulomb oscillations; red and blue (gray) dashed horizontal lines are a guide for the eye. The data in the inset before and (red or gray line) after the thermal cycle. The data in the inset before the increased complexity of fabrication.

Acknowledgment

The authors would like to thank T. Thorbeck, J. Bonevich, J. Bowser, and V. Luciani for the fruitful discussions and J. Bowser and V. Luciani for guidance with the fabrication. Research was performed in part at the Center for Nanoscale Science and Technology, National Institute of Standards and Technology. The authors would like to thank T. Thorbeck, J. Bonevich, D. E. Prober, “The radio-frequency single-electron transistor (RF-SET): A fast and ultrasensitive electrometer,” Science, vol. 280, no. 5367, pp. 1238–1242, May 1998.

References

[1] H. Grabert and M. H. Devoret, Single Charge Tunneling, vol. 294. New York: Plenum, 1992.

[2] R. J. Schoelkopf, P. Wahlgren, A. A. Kozhevnikov, P. Delsing, and D. E. Prober, “The radio-frequency single-electron transistor (RF-SET): A fast and ultrasensitive electrometer,” Science, vol. 280, no. 5367, pp. 1238–1242, May 1998.

[3] J. P. Pekola, K. P. Hirvi, J. P. Kauppinen, and M. A. Paalanen, “Thermometry by arrays of tunnel junctions,” Phys. Rev. Lett., vol. 73, no. 21, pp. 2903–2906, Nov. 1994.

[4] J. Gallop, “The quantum electrical triangle,” Philos. Trans. Roy. Soc. A, vol. 363, no. 1834, pp. 2221–2247, Sep. 2005.

[5] N. Z. Zimmerman and M. W. Keller, “Electrical metrology with single electrons,” Meas. Sci. Technol., vol. 14, no. 8, pp. 1237–1242, Aug. 2003.

[6] T. Fujisawa, T. Hayashi, and S. Sasaki, “Time-dependent single-electron transport through quantum dots,” Rep. Prog. Phys., vol. 69, no. 3, pp. 759–796, Mar. 2006.

[7] R. Hanson, L. P. Kouwenhoven, J. R. Petta, S. Tarucha, and L. M. K. Vandersypen, “Spins in few-electron quantum dots,” Rev. Mod. Phys., vol. 79, no. 4, pp. 1217–1265, Oct. 2007.

[8] J. L. Morton, D. R. McCamey, M. A. Eriksson, and S. A. Lyon, “Embracing the quantum limit in silicon computing,” Nature, vol. 479, no. 7373, pp. 345–353, Nov. 2011.

[9] A. Fujiwara, H. Inokawa, K. Yamazaki, H. Namatsu, Y. Takahashi, N. M. Zimmerman, and S. B. Martin, “Single electron tunneling transistor with tunable barriers using silicon nanowire metal–oxide–semiconductor field-effect transistor,” Appl. Phys. Lett., vol. 88, no. 5, pp. 053121–1–053121–3, Jan. 2006.

[10] N. M. Zimmerman, W. H. Huber, B. Simonds, E. Houdarkis, A. Fujiwara, Y. Ono, Y. Takashi, H. Inokawa, M. Furlan, and M. W. Keller, “Why the long-term charge offset drift in Si single-electron tunneling transistors is much smaller (better) than in metal-based ones: Two-level fluctuator stability,” J. Appl. Phys., vol. 104, no. 3, pp. 033710–1–033710–12, Aug. 2008.

[11] N. M. Zimmerman, B. J. Simonds, A. Fujiwara, Y. Ono, Y. Takahashi, and H. Inokawa, “Charge offset stability in tunable-barrier Si single-electron tunneling devices,” Appl. Phys. Lett., vol. 90, no. 3, pp. 033507–1–033507–3, Jan. 2007.

[12] E. Houdarkis, J. A. Wahl, and N. M. Zimmerman, “Lack of charge offset drift is a robust property of Si single electron transistors,” Appl. Phys. Lett., vol. 92, no. 6, pp. 062102-1–062102-3, Feb. 2008.

[13] W. M. Witzel, M. S. Carroll, A. Morello, L. Cywiński, and S. Das Sarma, “Electron spin decoherence in isotope-enriched silicon,” Phys. Rev. Lett., vol. 105, no. 18, pp. 187602-1–187602-4, Oct. 2010.

[14] L. A. Tracy, E. P. Nordberg, R. W. Young, C. B. Pinilla, H. L. Stalford, G. A. T. Eyck, K. Eng, K. D. Childs, J. R. Wendt, R. K. Grubbs, J. Stevens, M. P. Lilly, M. A. Eriksson, and M. Carroll, “Double quantum dot with tunable coupling in an enhancement-mode silicon metal–oxide semiconductor device with lateral geometry,” Appl. Phys. Lett., vol. 97, no. 19, pp. 192110–1–192110–3, Nov. 2010.

[15] G. Kapila, B. Kaczer, A. Nackaerts, N. Collaert, and G. V. Greeseneken, “Direct measurement of top and sidewall interface trap density in SOI FinFETs,” IEEE Electron Device Lett., vol. 28, no. 3, pp. 232–234, Mar. 2007.

[16] P. V. Gray and D. M. Brown, “Density of SiO2/Si interface states,” Appl. Phys. Lett., vol. 8, no. 2, pp. 31–33, Jan. 1966.

[17] C. H. Yang, W. H. Lim, F. A. Zwanenburg, and A. S. Dzurak, “Dynamically controlled charge sensing of a few-electron silicon quantum dot,” AIP Adv., vol. 1, no. 4, pp. 042111-1–042111-6, Dec. 2011.

[18] H. Pan, M. G. House, X. Hao, and H. W. Jiang, “Fabrication and characterization of a silicon metal–oxide–semiconductor field-effect transistor,” Appl. Phys. Lett., vol. 105, no. 26, pp. 263109-1–263109-5, Jun. 2012.

[19] J. R. Prance, Z. Shi, C. B. Simmons, D. E. Savage, M. G. Lagally, L. R. Schreiber, L. M. K. Vandersypen, M. Friesen, R. Joynt, S. N. Coppersmith, and M. A. Eriksson, “Single-shot measurement of triplet–singlet relaxation in a Si/SiGe double quantum dot,” Phys. Rev. Lett., vol. 108, no. 4, pp. 046808-1–046808-4, Jan. 2012.

[20] M. Pierre, B. Roche, R. Wacquez, X. Jehl, M. Sanquer, and M. Vinet, “Intrinsic and doped coupled quantum dots created by local modulation of implantation in a silicon nanowire,” J. Appl. Phys., vol. 109, no. 8, pp. 084346-1–084346-3, Apr. 2011.

[21] S. M. Zee and K. K. Ng, Physics of Semiconductor Devices, 3rd ed. Hoboken, NJ: Wiley, 2007.

[22] D. K. Schroder, Semiconductor Material and Device Characterization, 3rd ed. Hoboken, NJ: Wiley, 2006.

[23] E. Harari, “Dielectric breakdown in electrically stressed thin films of thermal SiO2,” J. Appl. Phys., vol. 49, no. 4, pp. 2478–2489, Apr. 1978.

Authors’ photographs and biographies not available at the time of publication.