VARIABLE BLOCK CARRY SKIP LOGIC USING REVERSIBLE GATES

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Abstract: Reversible circuits have applications in digital signal processing, computer graphics, quantum computation and cryptography. In this paper, a generalized k*k reversible gate family is proposed and a 3*3 gate of the family is discussed. Inverter, AND, OR, NAND, NOR, and EXOR gates can be realized by this gate. Implementation of a full-adder circuit using two such 3*3 gates is given. This full-adder circuit contains only two reversible gates and produces no extra garbage outputs. The proposed full-adder circuit is efficient in terms of gate count, garbage outputs and quantum cost. A 4-bit carry skip adder is designed using this full-adder circuit and a variable block carry skip adder is discussed. Necessary equations required to evaluate these adder are presented.

1. INTRODUCTION

The input vector of reversible circuit can be uniquely recovered from the output vector, that is, for each input pattern there is a unique output pattern. Logic computations that are not reversible necessarily generate heat irrespective of their implementation technologies. According to [2], zero energy dissipation would be possible only if the network consists of reversible gates.

Synthesis of reversible logic circuits differs significantly from the synthesis of combinational (classical) logic circuits. Because in a reversible circuit the number of inputs must be equal to the number of outputs, every output can be used only once (i.e., no fan-out is permitted), and the resulting circuit must be acyclic.

Therefore, a good synthesis method must take into account the following rules:
1. use as many outputs of every gate as possible, and thus minimize garbage (unused) outputs.
2. do not create more constant inputs (required to make an irreversible specification to a reversible one) to gates than is absolutely necessary.
3. avoid leading output signals of gates to more than one input, because each fan-out of two requires adding one copying circuit.

The rest of the paper is organized as follows: section 2 presents the families of reversible gates and their quantum cost. Section 3 presents a generalized k*k reversible gate and discusses an instance of this family of gates. Section 4 first establishes the minimum number of constant inputs and garbages are required to design a full adder circuit, and then composition of a new full adder circuit is proposed. Section 5 presents the design of a carry skip adder using the proposed full adder circuit for which it is used as basic building block. Section 6 presents a variable block carry skip adder block. Experimental results are shown in section 7. Section 8 concludes the paper. References are listed in section 9.

2. FAMILIES OF REVERSIBLE GATES AND THEIR QUANTUM COST

There exist many universal reversible gates [1,3,7,10,11]. There exists only one 1*1 reversible gate called inverter (A → A'). This gate is very important since it does not introduce garbage outputs. Some of the popular and important gates are 2*2 Feynman ((A, B) → (P = A, Q = A ⊕ B)), 3*3 Toffoli ((A, B, C) → (P = A, Q = B, R = AB ⊕ C)), 3*3 Fredkin ((A, B, C) → (P = A, Q = A'B ⊕ AC, R = A'C ⊕ AB)) and Peres [1] ((A, B, C) → (P = A, Q = A ⊕ B, R = AB ⊕ C)) gate.

![Figure 1. 2*2 Feynman Gate](image)

![Figure 2. 3*3 Toffoli Gate](image)

The detailed cost of a reversible gate depends on any particular realization technology of quantum logic. According to [9], it is assumed that the cost of every 2*2 is the same. A 1*1 cost nothing, since it can be always included to arbitrary 2*2 gate that preceded or follows it. Thus, every permutation quantum gate will be build from 1*1 and 2*2 quantum primitives and its cost calculated as a total sum of 2*2 gates.
Using the well known realization of Toffoli gate with truly quantum 2*2 primitives, according to [9], the cost of Toffoli gate is five 2*2 gates, or simply, 5 as shown in figure 2. The cost of Fredkin gate is exactly the same as the cost of Toffoli gate [5], which is shown in figure 3. Peres gate can be realized with cost 4 [9]. This is the cheapest quantum realization of a complete (universal) permutation gate.

3. A GENERALIZED K*K REVERSIBLE GATE FAMILY

A generalized k*k reversible gate family is proposed in Figure 4(a), \( f_{k-2}(A_1, A_2, \ldots, A_{k-2}) \) is an arbitrary function of \( A_1, A_2, \ldots, A_{k-2} \) and \( f_{k-1}(A_1, A_2, \ldots, A_{k-1}) \) is the function of \( A_1, A_2, \ldots, A_{k-1} \). The gate is a \( (k-2) \)-through gate. Mathematical properties of the gate family and systematic method for reversible logic synthesis using this family of gates are now being studied.

With \( k=2 \), this family of gate performs the same function as the Feynman gate. A 3*3 gate of the family is shown in Figure 4(b). The equation of this gate was known to Peres [1]. The quantum cost of this circuit is 4. The operation of this gate is shown in figure 5.

4. COMPOSITION OF FULL ADDER CIRCUIT

**Theorem:** A full-adder can be realized with at least two garbage output and one constant input.

Proof:
The full-adder output \( S = (A \oplus B \oplus C_n) \) and \( Cout = ((A \oplus B)Cin \oplus AB) \) equations produce the same output (1,0) for the three distinct input combinations (0,0,1), (0,1,0), and (1,0,0). Therefore, to separate all repeated values of outputs \( S \) and \( Cout \) we need at least two garbage outputs. Thus, a total of outputs is \( 2+2 = 4 \). Since in reversible circuits number of inputs must be equal to number of outputs and there are three inputs (\( A, B, \) and \( Cin \)), at least one constant input is necessary.

A full adder implementation using two 3*3 Toffoli gates and two 2*2 Feynman gate is presented in [8]. The circuit requires four reversible gates, produces two garbage outputs and the quantum cost is of 10.

Another full adder implementation using four 3*3 Fredkin gates is presented in [6]. The circuit requires four reversible gates, produces two garbage outputs and the quantum cost is of 20.

In this paper, we present a new full adder composition. It consists only of two Peres gate and the quantum cost is of 8, which is minimum than all of the existing compositions. This we will call Peres full-adder which shown in figure 6.

5. CARRY SKIP-ADDER

The carry skip adder reduces the delay due to the carry computation. Consider the full-adder’s operation. If either input is a logical 1, the cell will propagate the carry input to the carry output. Therefore, the \( i \)th full-adder carry input, \( C_{in} \), will propagate the carry input to its carry output, \( C_{out} \), when \( P_i = A_i \oplus B_i \). Multiple full-adders, called a block, can generate a “block” propagate signal to detour the incoming carry around to the block’s carry output signal. Figure 7 shows a 4-bit carry skip adder block. Each block is a small ripple carry adder producing the block’s sum and carry bits.
However, each block quickly calculates whether the block’s carry input is propagated to its carry output.

\[
\begin{align*}
\text{d}_{\text{ripple}}(B) &= B + 1 \\
\text{d}_{\text{skip}} &= \lceil \log_2 B \rceil + 3
\end{align*}
\]

The full adder in figure 6 generate sum bit \( S_i \), carry bit \( C_i \), and propagate signal \( P_i \) passing through 2, 2, and 2 reversible gate. Therefore, the delay to generate \( S_i \) is 2. The delay to generate \( P_i \) is 2. And the delay to generate \( C_i \) is 2 reversible gates. Then, all propagate signals for the carry skip adder block are combined with a B bit AND gate with delay \( \lceil \log_2 N \rceil \). Finally, the Peres gate in the left of figure 7 generates \( C_{\text{out}} \).

Consider the B bit carry skip adder block in figure 7 generating a block carry out \( C_{\text{out}} \) generates via carry ripple through the full adders. The least significant full adder requires a path delay of 2 Peres gates to generate \( C_i \) from the addends. Then, the carry “ripples” through the subsequent full adders with a path delay of 1 Peres gate per bit. Finally, the Peres gate in the left of figure 7 generates \( C_{\text{out}} \) (via ripple) with a B bit carry skip adder is

\[
\begin{align*}
T_{\text{fixed}}(B) &= (B + 1) + \left( \frac{N}{B} - 2 \right) \left( \lceil \log_2 B \rceil + 3 \right) + (B + 1) (1)
\end{align*}
\]

Assuming \( \lceil \log_2 B \rceil = B/2 \) we get

\[
T_{\text{fixed}} = B + \frac{N}{2} + \frac{3N}{B} - 4
\] (4)

Minimizing \( T_{\text{fixed}} \) with respect to block size \( B \) gives

\[
1 - \frac{3N}{B^2} = 0 \text{ or } B_{\text{opt}} = 1.73 \sqrt[3]{N}
\] (5)

Substituting (5) into (4) gives the shortest delay for a fixed block size carry skip adder

\[
T_{\text{fixed}} = \frac{N}{2} + 3.47 \sqrt[3]{N} - 4
\] (6)

6. VARIABLE BLOCK CARRY SKIP ADDER

Varying the size of the carry skip adder blocks can reduce the total worst-case delay. Since carries generated or absorbed in the adder circuits have shorter data paths. Without loss of generality, the first and last carry skip blocks are \( b \) bits wide, and the carry skip adder is divided into \( t \) blocks, where \( t \) is even.

Assuming the carry skip adder block sizes are

\[
\begin{align*}
b + 1 \ldots b + \frac{t}{2} &- 1 \ldots b + \frac{t}{2} - 1 \ldots b + 1 \ldots b
\end{align*}
\] (7)

Summing the number of bits in the blocks, equating to \( N \), and rearranging gives

\[
b = \frac{N}{t} = \frac{1}{2} - \frac{1}{4} + \frac{1}{2}
\] (8)

The total worst case delay \( T_{\text{variable}} \) of an \( N \) bit carry skip adder with the variable block sizes is the sum of the ripple carry delay through the first carry skip adder block, the skip delays through the intermediate blocks, and the ripple carry delay through the last block.

Assuming the variable block sizes in (3), the total delay is

\[
T_{\text{variable}} = 2 \left( b + 1 \right) + 2 \sum_{k=0}^{b-1} \left( \log_2 2^{t-k} + 3 \right)
\] (9)

Assuming \( \lceil \log_2 k \rceil = k/2 \) and rearranging (9) becomes

\[
T_{\text{variable}} = 4b - 4 + 3t + \left( b + \frac{t}{2} - 1 \right) \left( b + \frac{t}{2} \right) - b(b+1)
\]

Inserting (8) into (10), and collecting terms gives

\[
T_{\text{variable}} = \frac{9t}{4} - \frac{5}{2} + \frac{3N}{t} + \frac{N}{2}
\] (11)

The optimal number of blocks is found with
\[
\frac{\delta T_{\text{variable}}}{\delta t} = \frac{9}{4} \cdot \frac{3N}{t^2} = 0 \quad \text{or} \quad t_{\text{opt}} = \frac{2}{3} \cdot \sqrt{3} \cdot \sqrt{N} \quad (12)
\]

Therefore, the optimal variable block size carry skip adder has delay

\[
T_{\text{variable}} = \frac{N}{2} + \sqrt{3} \cdot \sqrt{N} - \frac{5}{2} \quad (13)
\]

7. RESULTS

We compare our proposed full adder circuits with existing designs and result is shown in Table 1 and Table 2. In the previous paper Quantum costs of those circuits are not considered. We calculate the Quantum cost of those adder circuits and compare them with our proposed design.

Table 1: Comparison Table 1

| Full-adder Composition | No. Of gates used | No. Of Garbage Output | No. Of Constant input | Quantum Cos t |
|------------------------|-------------------|-----------------------|-----------------------|--------------|
| Proposed Peres         | 2                 | 2                     | 1                     | 8            |
| Toffoli, Khan and Feynman [4] | 3           | 2                     | 1                     | -            |
| Toffoli and Feynman [8] | 4                 | 2                     | 1                     | 10           |
| Khan and Feynman gate [7] | 3              | 3                     | 2                     | -            |
| Fredkin [6]            | 4                 | 3                     | 2                     | 20           |

The analytical performance of the carry skip adder in [6] and our carry skip adder (Figure 7) is given in table 3. It's evident from Table 3 that our design performs better. For smaller block size our carry skip adder performs best (approximately double) and practically smaller block size is required. We choose binary exponential values for the block size, which is natural for block size.

Table 2: Comparison Table 2

| Full-adder Composition | Unit Clock Cycle | Gate Calculations |
|------------------------|------------------|-------------------|
|                        |                  | Two input EXOR    |
|                        |                  | Two input AND     |
|                        |                  | NOT               |
| Proposed Peres         | 2                | 4                 |
| Toffoli, Khan and Feynman [4] | 3             | 4                 |
| Toffoli and Feynman [8] | 4                | 4                 |
| Khan and Feynman gate [7] | 3               | 5                 |
| Fredkin [6]            | 4                | 8                 |

8. CONCLUSION

The main goal of this paper is finding a good architecture for adder circuits using reversible logic based on minimizing gate count, garbage outputs, constant inputs, and quantum cost. Technology independent analysis of these adder circuits is given since quantum or optical logic implementations are not available.

Table 3: Showing $T_{\text{max}}$ for different Implementations

| No. Of Bits | $T_{\text{max}}$ for[6] | $T_{\text{max}}$ for Peres |
|-------------|--------------------------|-----------------------------|
| 4           | 13.49                    | 4.93                        |
| 8           | 21.9                     | 9.80                        |
| 16          | 34.98                    | 17.86                       |
| 32          | 55.82                    | 31.60                       |
| 64          | 89.97                    | 55.71                       |
| 128         | 147.64                   | 99.19                       |
| 256         | 247.94                   | 179.43                      |
| 512         | 427.27                   | 330.38                      |
| 1024        | 755.87                   | 618.85                      |
| 2048        | 1370.54                  | 1176.77                     |
| 4096        | 2539.74                  | 2265.70                     |

9. REFERENCES

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