Design and Implementation of Ethercat Master Based On ZYNQ

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Abstract. In order to realize the functional requirements of EtherCAT protocol and EtherCAT master station in the field of industrial automation, and to solve the problem that the real-time performance and stability of the current embedded master station controller is not high enough, a hardware scheme for implementing the function of EtherCAT master station is proposed based on the architecture of embedded Zynq-soc (ARM+FPGA). The scheme is herein proposed for implementing Ethernet card equipment of EtherCAT master based on FPGA to improve the stability and response speed of the link layer. Real-time system software implementation scheme based on Linux has been improved. Xenomai is adopted to improve the real-time performance of the system and the accuracy of control cycle. Finally, an embedded real-time EtherCAT master station is constructed, and the EtherCAT slaves are the testing platform of two sets of panasonic AC SERVO Driver MADHT series. The experimental results show that the master controller meets the compatibility of EtherCAT standard protocol, with high real-time performance and stability.

1. Introduction

At present, there are many kinds of buses. Common buses include Modbus, CAN, DeviceNet, Profibus, EtherNet/IP, Lonworks, FF, EtherCAT, Modbus TCP, ProfiNet, InterNet/IP, etc. EtherCAT (Ethernet control automation technology), an Ethernet based on open architecture field bus system, which is an open real-time Ethernet communication protocol developed by Beckhoff automation in Germany. With high performance, low cost and ease of use, EtherCAT is widely used in motion control, robotics, CNC and other industrial automation applications [1].

Currently, for the implementation of EtherCAT master, most of the hardware solutions are developed by single embedded ARM [2-3], and most of the software solutions take Linux and open source Xenomai as the real-time system [3-4]. The current software scheme can meet the actual demand, but the real-time response and stability of the hardware scheme need to be greatly improved [5]. Literature [6] proposed the hardware design scheme based on ARM+FPGA and the Linux and open source Xenomai software implementation scheme, and the final system has good protocol compatibility and stability.

Zynq ® - 7000 fully programmable SoC (AP) SoC device integrates ARM ® software programmable processor and FPGA hardware programmability, which can realize a variety of flexible and efficient operation [7]. For this reason, the combination of the two is a reliable implementation...
scheme for developing EtherCAT high performance master. In summary, this paper designs and implements the development of the hardware and software of the Ethernet master controller based on Zynq, which solves the current problem of insufficient real-time performance and stability of the embedded master controller.

2. Design of control system of EtherCAT master

EtherCAT (Ethernet control automation technology) is a high-performance industrial communication protocol for deterministic Ethernet. It extends the IEEE 802.3 Ethernet standard, making data transmission predictable timing and high-precision synchronization. As part of IEC 61158, this open standard is often used in mechanical design and motion control applications. EtherCAT adopts the standard IEEE 802-3 Ethernet frame, and the frame structure is shown in figure 1. The EtherCAT protocol transmits data directly in the frame format of standard Ethernet without modifying its basic structure.

EtherCAT implements the CANopen protocol. Data in CANopen is transmitted periodically through PDO (process data object), which is of high priority and can be used for real-time transmission. Non-periodic data such as configuration parameters and object dictionaries are transmitted through SDO (service data object). Each PDO contains a single or multiple address from the device, and this data-address structure (with the transmission count bit for validation) constitutes EtherCAT's message. Each Ethernet frame may contain several messages, and in one cycle multiple frames may be required to transmit all the required messages.

Traditional Ethernet communication solutions first accept Ethernet packets from the slave, then interpret and copy the process data, and finally forward the data. EtherCAT Ethernet frames can be processed while transmitting with the help of special hardware modules. Each slave node has FMMU (field bus storage and management unit). The FMMU analyzes the address of the packet, reads the data of the node, and forwards the message to the next device. The data that needs to be transmitted can also be inserted when the message passes through. The entire process of reading, inserting, forwarding data has only a nanosecond delay. As shown in figure 2, assuming an Ethernet frame is similar to a moving train, an EtherCAT message is each train carriage, and a PDO data bit is the passenger in the carriage, and the appropriate slave device can be extracted and inserted. The whole train goes through all the slave equipment without stopping, turns around at the end of the

![Figure 1. EtherCAT data frames](image-url)
slave, and goes back through all the slave equipment again. (note: EtherCAT not only supports master-slave communication, but also slave communication, namely S2S).

3. Design of EtherCAT master station software based on Zynq
This paper adopts Linux and Xenomai to improve the real-time system operating system. The software architecture of the main station is shown in figure 3. The master protocol stack adopts modularized architecture, which can realize each special project application. The functions of each module of master software are shown in table 1.

![Figure 2. EtherCAT data transmission.](image)

![Figure 3. Hierarchical structure.](image)
Table 1. Functions of each layer.

| Layer                          | Function                                                                 |
|--------------------------------|-------------------------------------------------------------------------|
| The application layer          | Program/configure environment interaction, application or device interaction. Ensure access to master functions; TCP/IP and UDP connectivity are provided. |
| Mailbox Module                 | Data transfer and data exchange. Support for CoE, FoE, EoE, SoE, VoE, AoE and other email services. |
| Process Image Module           | The presentation of PI, address, and the ENI file can be automatically generated by the configuration tool; Slave control, the process task access process image is performed by the master interface. |
| Distribution Clock module      | Same EtherCAT system time sharing.                                       |
| Frame Schedule Module          | Different scan rates from the station are defined according to different scan cycles. The frame scheduling module manages the EtherCAT frame rate and forwards them to the EtherCAT network driver. |
| OSAL operating system abstract layer module | Processing threads, timers, mutexes, etc. Including the network adapter driver module: extract the core core of the host stack from the underlying network implementation |

4. Hardware design of EtherCAT master based on Zynq

4.1. Hardware Architecture Diagram

The hardware architecture of the master is mainly composed of three parts in figure 4: PC terminal, Zedboard main station development board and external FMC network card. The PC realizes the instruction input of the operating system through the serial port terminal. The EtherCAT network diagnostic configuration tool on the PC connects the main platform of Zedboard through RPC service, which can realize the configuration of the master and the slave and generate the network configuration file through scanning. The master board of Zedboard is a Soc development board based on Zynq device design. The schematic diagram of the development board is shown in figure 5 below.
4.2. Hardware Internal Architecture Diagram

In the hardware architecture, the internal structure framework of the Master board of Zedboard is shown in figure 6 below.

Figure 6. Hardware internal architecture diagram.
In the hardware internal architecture diagram, the PS layer, namely the ARM processor part of Zynq, is loaded with the improved real-time operating system of Linux and Xenomai and the EtherCAT Master Core. The improved real-time operating system brings the entire communication process to the us level, while the master source code of EtherCAT is responsible for processing data according to the EtherCAT mechanism and packaging it to NIC Driver (network card Driver), which passes the packaged data to IP core in the PL layer through the AXI bus.

The PL layer in the hardware internal architecture diagram, namely the FPGA hardware part of Zynq, loaded the IPcore of the master, which used logic to build two NIC (MAC) and Timer and encapsulated together. The NIC 0/1 receives the data from NIC Driver through the AXI bus, rearranges the data and finally gives it to PHY. RJ45 then sends the EtherCAT data frames through the transformer. Timer provides a clock source for synchronization of NIC Driver and NIC 0/1.

5. Testing and results of EtherCAT master
In this paper, we built an embedded real-time EtherCAT master based on Zynq, and the slave is a testing platform of two sets of panasonic AC SERVO Driver MADHT series. The testing content mainly includes three parts: the EtherCAT system to be tested, the real-time data acquisition unit and the offline experimental data analysis unit. The content of the test is to compare the test data with and without DC function in the period of 250us.

5.1. Real-time Data Acquisition Unit
The real-time data acquisition unit uses network analyzer Profishark 100M or Profishark 1G, and the two network ports are standard 100M/1Gbps Ethernet interfaces. It supports the separate capture of upstream and downstream data, and the captured data packets can be used for data analysis by software such as Wireshark /Profishark Manager. In addition, it can capture data packet timestamp resolution up to 5ns, which ensures the accuracy of experimental data, as shown in figure 7 below.

5.2. Offline Data Analysis Unit
The offline data analysis unit is implemented by the open source software Wireshark running on PC. At the end of the experiment, all the captured experimental data will be handed to the offline data unit for processing and analysis. Wireshark is used to separately capture data with and without DC. The test results of EtherCAT data are shown in table 2 below.
Table 2. EtherCAT data test result unit: us

|       | Circle time in default | Circle time with DC | Circle time without DC |
|-------|------------------------|---------------------|------------------------|
| 1     | 250                    | 245                 | 248                    |
| 2     | 250                    | 249                 | 243                    |
| 3     | 250                    | 253                 | 267                    |
| 4     | 250                    | 252                 | 249                    |
| 5     | 250                    | 251                 | 243                    |
| 6     | 250                    | 254                 | 263                    |
| 7     | 250                    | 251                 | 248                    |
| 8     | 250                    | 252                 | 241                    |
| 9     | 250                    | 253                 | 268                    |

It can be seen from the table that circle time, the main station design scheme based on Zynq platform, can achieve the level of 250us. Adding DC functions with two shafts from the site, there is basically no jitter, but without DC, the cycle time is unstable and the jitter is relatively large.

6. Conclusion

In this paper, the EtherCAT protocol and the EtherCAT master controller architecture were analyzed, and the EtherCAT software and hardware implementation scheme was studied. By comparing the advantages and disadvantages of the common network card scheme based on embedded processor and FPGA, the author designs the hardware and software implementation scheme of EtherCAT master station based on zynq-soc, realizes the functions of EtherCAT master controller combining ARM-PS layer and FPGA-PL, and can meet the control requirements of high speed, high precision and high stability in industrial automation.

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References

[1] J. Xun, Y.Q. Liu, Design and application of Ethernet field bus EtherCAT driver [M], Beijing:Beihang University Press, 2010.
[2] H.J. Wang, Implementation of EtherCAT master on embedded platform, Journal of Computer Applications,2018,38:165-169.
[3] E.B. Gao, G.F. Yan, EtherCAT master based on linux embedded platform BeagleBone Black,Journal of Industrial Control Computer,2016,29:28-30.
[4] K. Xie, G.F. Yan, Design of motion control system based on EtherCAT, Journal of Modular Machine Tool&Automatic Manufacturing Technique, 2017,2:68-72.
[5] Cereia M,Scanzio S. A user space EtherCAT master architecture for hard real-time control systems [C],Krakow: 2012.
[6] J. Xu, X.Q. Tang, B. Song, Design and implementation of EtherCAT master based on ARM+FPGA, Journal of Modular Machine Tool&Automatic Manufacturing Technique,2016,6:84-87.
[7] B. He, Y.H. Zhang, Design and implementation of Xilinx Zynq-7000 embedded system [M],Beijing: Publishing House of Electronics Industry,2016.
[8] W.J. Shi, The structure of the hardware abstraction layer based on multi-domain and the research of its application in real-time linux [D], Southwest Jiaotong University, 2010.
[9] Y. Zhu, Study of real-time based on embedded linux operating system [D], Chang’an University, 2012.
[10] Start Here [Z]. http: //xenomai.org/.