Implementing quantum algorithms on realistic devices requires translating high-level global operations into sequences of hardware-native logic gates, a process known as quantum compiling. Physical limitations, such as constraints in connectivity and gate alphabets, often result in unacceptable implementation costs. To enable successful near-term applications, it is crucial to optimize compilation by exploiting the capabilities of existing hardware. Here we implement a resource-efficient construction for a quantum version of AND logic that can reduce the compilation overhead, enabling the execution of key quantum circuits. On a high-scalability superconducting quantum processor, we demonstrate low-depth synthesis of high-fidelity generalized T offoli gates with up to 8 qubits and Grover's search algorithm in a search space of up to 64 entries. Our experimental demonstration illustrates a scalable and widely applicable approach to implementing quantum algorithms, bringing more meaningful quantum applications on noisy devices within reach.

Quantum algorithms are predicted to provide a computational speed-up over their classical counterparts. To be implemented, these algorithms need to be compiled on specific quantum hardware to decompose global operations into the naturally available elementary gates. Given the stringent resource constraints offered by the noisy intermediate-scale quantum (NISQ) technology foreseeable in the next 5–10 years, it is essential to optimize the use of every qubit and every gate cycle to enable successful near-term applications. One effective strategy is to fully explore the hardware capabilities and diversify the available gate alphabets to optimize compilation. Several global or multi-qubit operations are textbook circuit components essential for building quantum algorithms. The best-known examples are the quantum arithmetic circuits used in Shor’s factoring algorithm and the multiply controlled gates used in Grover’s search algorithm. The latter are nontrivial multi-qubit quantum logics that perform unitary operations on target qubits conditioned on the states
of all the control qubits. Relevant applications include quantum error correction\textsuperscript{17–23}, quantum simulation\textsuperscript{24–26} and quantum machine learning\textsuperscript{27–30}. One brute-force approach for an extensible implementation of these large operations is to decompose them into a finite set of universal gates. For example, the generalized Toffoli gate, that is, the $n$-qubit controlled-NOT (CNOT) gate, can be constructed using quadratically many $O(n^2)$ two-qubit CNOT gates plus single-qubit gates on a qubit array with all-to-all connections\textsuperscript{31} and even more gates on devices with nearest-neighbour couplings\textsuperscript{32}. A more efficient approach is to concatenate together small Toffoli gates, assisted by ancilla qubits\textsuperscript{33}. Leaving aside the extra resources needed, it is challenging to achieve high-quality small Toffoli gates. Apart from brute-force decomposition, small Toffoli gates may be obtained via one-step manipulations\textsuperscript{34–36} or by leveraging either, again, ancilla qubits\textsuperscript{37} or ancilla levels\textsuperscript{38–40}. Despite successful demonstrations of single small Toffoli gates in various systems, a scalable synthesis has never been experimentally realized because of the prohibitive implementation cost. A scheme that is, at the same time, hardware-efficient, low-depth, easy to control and compatible with state-of-the-art hardware\textsuperscript{41–43} is yet to be realized. We note that native global entangling operations are available in ion traps, which have unique all-to-all connections\textsuperscript{44}, and in specially designed superconducting circuits\textsuperscript{45}. However, these global operations are based on pairwise interactions and thus not equivalent to the multiply controlled gate, although they may be used for faster synthesis\textsuperscript{46}.

In this Article we introduce a quantum version of the AND (QuAND) gate, a novel gate type that, as inspired by ref.\textsuperscript{28}, utilizes an ancilla level for temporary information storage only. The QuAND gate enables a scaling advantage in the circuit depth when synthesizing arithmetic circuits and multiply controlled gates. We experimentally implement QuAND gates on a superconducting quantum processor featuring simplified wiring and low crosstalk, and demonstrate a linear-depth synthesis of generalized Toffoli gates with up to eight qubits, that is, a total of seven control qubits. Our demonstration is large in size and shows high performance (truth table fidelity: 89.1%, 53.2% and 39.1% for $n = 4$, 6 and 8, respectively). Using these gates, we perform Grover’s search algorithm with multiple amplification cycles and achieve significant success probabilities (46.8% and 3.9% for searches of 16 and 64, respectively), demonstrating the feasibility of our method for scaled applications. Note that alternative efficient compilation schemes have been proposed in recent theoretical studies\textsuperscript{47–49}. However, these schemes generally require the manipulation of a multi-level system with high degrees of freedom, adding considerable operational complexity.

**Simplifying quantum logic using QuAND gates**

The logic AND operation is a basic ingredient for designing both classical and quantum algorithms. Unfortunately, it cannot be directly implemented on qubits because of the reversibility of quantum operations. One workaround is to extract it from a Toffoli gate at the cost of an extra qubit\textsuperscript{50}. This overhead hinders scaled implementation on realistic hardware. In this Article we propose a resource-efficient QuAND gate scheme (Fig. 1a) in which one of the two outputs registers the AND result of the inputs, that is, $|\text{A&B}\rangle$, and the other output $|C\rangle$ spans three different states, in our case, $|1\rangle$, $|2\rangle$ and $|0\rangle$ for input states $|00\rangle$, $|10\rangle$ and $|11\rangle$, respectively. The use of the ancilla level $|C\rangle$ preserves reversibility; the reverse QuAND gate simply switches the inputs and outputs. We refer to the AND-value qubit as the ‘parent’ and the other qubit as the ‘child’. The circuit notation, truth table and decomposition schemes of the QuAND gate and its reversal are illustrated in Fig. 1a. Here we decompose the QuAND gate (or its reversal) into a single-qubit $X$ gate in front of (or after) an iSWAP\textsuperscript{11–20}—like operation between $|11\rangle$ and $|20\rangle$ (denoted iSWAP$_{11–20}$), which is naturally available on our hardware, as shown later.

One direct application of a QuAND gate is to simplify the compilation of large gate operations, in particular, multiply controlled gates, which are experimentally challenging to realize and focus of this study. Figure 1b shows the circuit decomposition for an $n$-qubit CZ gate on a one-dimensional (1D) qubit chain divided into three stages: embedding, the controlled-unity operation and recovery. Let $|s⟩ = |s_1s_2...s_n⟩$ ($s = 0, 1$) denote a basis state at the input. During embedding, we apply QuAND gates sequentially to the chain from both ends inward. At the end of the QuAND sequence, the two root parents in the middle, $Q_{k−1}$ and $Q_{k+1}$, temporarily register the AND result of all the qubits from the upper and lower halves of the chain onto the two root parents, $Q_{k−1}$ and $Q_{k+1}$, respectively. The embedded information is later released via the reverse QuAND gates to recover the original binary encoding. The CZ gate is only effective when $k = 0$, that is, at the same time, hardware-efficient, low-depth, easy to control and compatible with state-of-the-art hardware\textsuperscript{41–43} is yet to be realized. We note that native global entangling operations are available in ion traps, which have unique all-to-all connections\textsuperscript{44}, and in specially designed superconducting circuits\textsuperscript{45}. However, these global operations are based on pairwise interactions and thus not equivalent to the multiply controlled gate, although they may be used for faster synthesis\textsuperscript{46}.

![Fig. 1](image_url) | Simplifying compilation using the quantum version of the AND (QuAND) gate. (a) Circuit notation, truth table and decomposition of the QuAND gate and its reversal. The AND-value qubit, indicated by an $\&$, is referred to as the ‘parent’, and the other qubit is referred to as the ‘child’. A QuAND gate is indicated by an arrow pointing from the child to the parent, with an arrow in the opposite direction indicating a reverse QuAND gate. Both can be synthesized with a single-qubit $X$ gate and an iSWAP-like operation between $|11\rangle$ and $|20\rangle$, which is indicated by a double-cross sign with a dashed cross on the child qubit. (b) Circuit decomposition of an $n$-qubit controlled-$Z$ (CZ) gate on a 1D qubit chain using a sequence of QuAND gates, a CZ gate and a sequence of reverse QuAND gates, shown here with time progressing from left to right. During embedding, the sequentially applied QuAND gates register the AND results of all the qubits from the upper and lower halves of the chain onto the two root parents, $Q_{k−1}$ and $Q_{k+1}$, respectively. The embedded information is later released via the reverse QuAND gates to recover the original binary encoding. The CZ gate is only effective when all qubits are in state $|1⟩$. (c) Sketch showing a quantum processor with qubits connected in an arbitrary topology. A branching tree is enacted for implementing the QuAND gate sequence (arrows) with time progressing from dark blue to light green. The CZ gate is performed between the two root parents. The QuAND gate could also be performed across multiple processors (arrows pointing from outside) to efficiently implement global operations on a larger quantum network.
identify the key idea of our proposal, that is, to enact a branching tree graph on an arbitrarily connected qubit array and apply QuAND gates sequentially to register the AND results of neighbouring qubits onto the parents, layer by layer, from the leaves up to the root, as illustrated in Fig. 1c. Ignoring the constant, the optimal circuit depth is then equivalent to the depth of the tree. For example, the circuit depth can be reduced to $O(\sqrt{n})$ on a 2D square array and to $O(\log n)$ on a binary tree (Supplementary Section II); such polynomial or exponential speed-up in compiling global operations can constitute a huge boost for relevant quantum applications. In addition, because this scheme only requires that qubits be connected, it is well suited to a distributed quantum network where only sparse connections are likely to be available.

**Implementing a QuAND gate with superconducting qubits**

Our experimental device (Fig. 2a), tested inside a dilution refrigerator at a base temperature of 10 mK, consists of eight fixed-frequency transmon qubits\(^5\), known for long coherence and simplified control, arranged in a ladder array and interconnected via ten frequency-tunable couplers. The two couplers in the middle have no control lines, resulting in the qubit array having a ring topology. Each qubit has a dedicated readout resonator, and all the resonators share a common feed line enabling a multiplexed dispersive readout. The qubit frequencies are arranged alternately between a red band (6.2–6.5 GHz) and a blue band (7.0–7.3 GHz) along the ring; such frequency planning helps suppress microwave crosstalk. The qubits are strongly coupled (with an interaction strength of $g/2\pi = 100$ MHz) to their adjacent couplers, which are tunable via their flux biases $\Phi_e$. The couplers are designed to turn off the inter-qubit coupling via multi-path interference\(^3\) near their maximum frequencies (8.0–8.4 GHz) at $\Phi_e = 0$, which resolves the frequency-crowding problem and reduces the nearest-neighbour ZZ crosstalk down to ~50 kHz. In addition, the use of tunable couplers enables fast two-qubit gates between the fixed-frequency qubits, for example, the adiabatic CZ gate\(^4\)\(^5\). We use a shared control line to deliver the doped signals for both the qubit (4–8 GHz) and coupler (DC-1 GHz) control; these signals are synthesized at room temperature and transmitted to the device inside the dilution refrigerator. This design substantially simplifies the wiring effort both on the chip and inside the refrigerator, promising higher scalability. See Supplementary Section III for details concerning the device and experimental set-up.

The QuAND and iSWAP\(_{11-20}\) gates on our device were implemented using coupler-assisted level transitions. According to the tri-mode (qubit, coupler, qubit) notation, the iSWAP\(_{11-20}\) gate is a full swap operation between $|10\rangle$ and $|20\rangle$, which is realized by a flux pulse sent to the coupler to activate such a transition we applied a flux pulse to the coupler. T o activate such a transition we applied a flux pulse to the coupler. Under this pulse, as shown by the thin black line with embedded arrowheads, the system state first follows an adiabatic excursion on state $|20\rangle$ transition is inhibited at $\Phi_e = 0.26$ $\Phi_e$, then transits to $|20\rangle$ via a parametric drive resonant with the instantaneous frequency gap between $|10\rangle$ and $|20\rangle$, and eventually adiabatically returns to the idling bias. There are two major concerns when choosing the transition bias. First, the flux-induced $|10\rangle \to |20\rangle$ transition is inhibited at $\Phi_e = 0$ but is significantly enhanced at a sufficiently large bias as a result of wavefunction hybridization, as is evident by the strong bending of the energy levels\(^4\)\(^5\). Second, a proper bias is critical to avoid spurious transitions (Supplementary Section IV).

In the experiment, we calibrated the iSWAP\(_{11-20}\) gate by optimizing both the frequency and the amplitude of the parametric pulse. An example of the continuous swapping between $|11\rangle$ and $|20\rangle$ as a function of the pulse amplitude $A_p$ is shown in Fig. 2c. The average observed transition error of 2.7% is primarily caused by energy relaxation during the pulse. All data presented here were corrected to account for the state preparation and measurement error. Note that, so far, we have
ignored the phase factor of the iSWAP$_{11-20}$ gate. In fact, a pair of iSWAP$_{11-20}$ gates exchange the excitation back and forth, leading to a conditional phase on state $|11\rangle$, which can be calibrated away by adjusting the relative phase between the two iSWAP$_{11-20}$ gates. Supplementary Section V provides details concerning the gate scheme, calibration procedures and data processing.

**Fig. 3** Low-depth synthesis of generalized Toffoli gates. a. Schematic showing the compiled sequence for implementing the 4-qubit (left), 6-qubit (centre) and 8-qubit (right) CZ gate circuits described in Fig. 1b on the 8-qubit processor with qubits indexed from 0 to 7. The arrows denote the QuAND gate sequence, with time progressing from dark blue to light green. We have omitted the reverse QuAND sequence. b. Measured truth tables of the corresponding generalized Toffoli gate. In these examples, the controlled-NOT operation is performed on $Q_7$ in all cases.

**Fig. 4** Demonstration of Grover’s search algorithm with multiple amplification cycles. a. Circuit diagram implementing Grover’s search algorithm. In this example, the encoded solution is 110101. $Y^{\pm \pi/2}$ indicates a ±$\pi/2$ rotation about the $Y$ axis. b. Measured output state probability distribution for each of the $2^n$ encoded states in the 4-qubit and 6-qubit Grover’s search algorithms. c. Average algorithm success probabilities (dots) and four times the standard deviations (error bars) of all $2^n$ cases versus the number of oracle-amplification cycles. The solid lines are fits to equation (1) with finite gate fidelity. The dashed lines correspond to the ideal case with unity fidelity.
Low-depth synthesis of multi-qubit Toffoli gates

Using calibrated QuAND gates, we demonstrate the low-depth synthesis of a generalized Toffoli gate, which is equivalent to the n-qubit CZ circuit described in Fig. 1b, with two additional single-qubit gates. Figure 3a illustrates how we compile, on the 8-qubit ring, an n-qubit CZ gate with incremental size (n = 4, 6 and 8) in linear time steps. We characterize these large gates by measuring their truth tables, $U_{exp}$, that is, the output state probability distribution for each of the $2^n$ input states, which are shown in Fig. 3b. The truth-table fidelities, $F_i = \frac{1}{2} \text{Tr}(U_{exp} U_{ideal})$, are 89.1%, 53.2% and 39.1% for $n = 4$, 6 and 8, respectively. We note that the 4-qubit Toffoli truth-table fidelity is higher than the measured gate fidelity (83.6%) from process tomography (Supplementary Section VI), as a result of underestimated phase errors when measuring the truth table. The relaxation-limited gate fidelities (total duration) for the 4-qubit, 6-qubit and 8-qubit Toffoli gates are 92.5% (0.4 μs), 66.7% (1.3 μs, staggered pulses) and 62.3% (1.1 μs), respectively, and are responsible for ~70% of the total error; the remaining error is due in part to dephasing and in part to stray couplings [42–44].

Grover’s search algorithm

Finally, we performed Grover’s search algorithm as a complementary method to benchmark our multi-qubit gates. The core steps of this algorithm encode a solution bit-string $j$ with a phase oracle $O_j = \sum_{s \neq j} |s \rangle \langle j |$, a unitary that accesses the input function, and amplify the probability of finding $j$ via phase diffusion, with each step containing an n-qubit CZ gate (Fig. 4a); these two steps may be repeated for further amplification. Here, the phase oracle performs a conditional phase flip on $j$; therefore, an arbitrary oracle can be constructed from an n-qubit CZ gate with additional pairs of $X$ gates applied to qubits being conditioned on $|0 \rangle$ instead of $|1 \rangle$. We note that there is an alternative way to implement Grover’s search by replacing the diffuse operator with single-qubit gates at the cost of more oracle queries [45].

Figure 4b shows the results of the 4-qubit and 6-qubit single-solution Grover’s search’s algorithm with one oracle-amplification cycle (the Supplementary Information provides extended data of the multi-solution Grover’s search). The diagonal matrix elements correspond to the probabilities of finding the correct states, that is, the algorithm success probability (ASP), and are substantially higher than the other elements, on average 34.2% versus 4.4% for the 4-qubit Grover’s search and 3.9% versus 1.5% for the 6-qubit Grover’s search, showing the effectiveness of the amplification. Because of its insufficient fidelity, the 8-qubit Grover result (not shown) does not display a significant ASP gain.

To optimize the ASP, we tested Grover’s search algorithm with multiple rounds of amplification. As shown in Fig. 4c, the average ASP in the 4-qubit case shows a clear improvement to 46.8% with one additional cycle ($M = 2$), and a clear dependence is visible up to ten cycles, that is, a total of 20 CCCZ gates, due to the high gate fidelity. Ignoring contributions from the single-qubit gate error, which is estimated to be 0.14% from simultaneous randomized benchmarking, we developed a simplified model for estimating ASP (Supplementary Section VII):

$$\text{ASP} = \pi^{2M} \sin^2 \left(2(M + 1) \arcsin \left(2^{-\frac{n}{2}} \right) \right) + \frac{1 - \pi^{2M}}{2^n},$$

(1)

where $\pi$ is the n-qubit CZ gate fidelity. Fitting the data to equation (1) gives $\pi = 84.4%$ and 50.9% for the 4-qubit and 6-qubit cases, respectively, which are close to the above-measured truth-table fidelities.

Discussion

The low-depth circuit synthesis using the QuAND logic enabled our implementation of multiply controlled gates and Grover’s search algorithm at a high scale, confirming the feasibility of a scalable and resource-efficient approach to simplify algorithm compilation. At the essence of our scheme is engineering a coherent, selective transition between one of the computational levels and an ancilla level, enabling the quantum analogue of AND logic. Therefore, the scheme can be applied to other quantum computing platforms by encoding the ancilla level using, for example, different internal states in ion traps [46], path variation in optical systems [46], valley freedom in Si/SiGe systems and nuclear spin in the SiP system [46]. This study should not only stimulate interest in exploring alternative compilation schemes using QuAND logic, but should also help reduce hardware-related challenges, in particular, the connectivity problem for which solid-state devices have long been criticized. With further improvements to fidelity, our work will help close the gap between most anticipated near-term applications and available NISQ devices.

Online content

Any methods, additional references, Nature Research reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41567-022-01813-7.

References

1. Preskill, J. Quantum computing in the NISQ era and beyond. Quantum 2, 79 (2018).
2. Chong, F. T., Franklin, D. & Martonosi, M. Programming languages and compiler design for realistic quantum hardware. Nature 549, 180–187 (2017).
3. Foxen, B. et al. Demonstrating a continuous set of two-qubit gates for near-term quantum algorithms. Phys. Rev. Lett. 125, 120504 (2020).
4. Abrams, D. M., Didier, N., Johnson, B. R., da Silva, M. P. & Ryan, C. A. Implementation of XY entangling gates with a single calibrated pulse. Nat. Electron. 3, 744–750 (2020).
5. Gu, X. et al. Fast multijubit gates through simultaneous two-qubit gates. PRX Quantum 2, 040348 (2021).
6. Nielsen, M. A. & Chuang, I. Quantum Computation and Quantum Information (Cambridge Univ. Press, 2002).
7. Shor, P. W. Algorithms for quantum computation: discrete logarithms and factoring. In Proc. 35th Annual Symposium on Foundations of Computer Science 124–134 (IEEE, 1994).
8. Grover, L. K. Quantum mechanics helps in searching for a needle in a haystack. Phys. Rev. Lett. 79, 325 (1997).
9. Cory, D. G. et al. Experimental quantum error correction. Phys. Rev. Lett. 81, 2152–2155 (1998).
10. Dennis, E. Toward fault-tolerant quantum computation without concatenation. Phys. Rev. A 63, 052314 (2001).
11. Inada, T. et al. Measurement-free ultrafast quantum error correction by using multi-controlled gates in higher-dimensional state space. Preprint at https://arxiv.org/abs/2109.00086 (2021).
12. Childs, A. M., Maslov, D., Nam, Y., Ross, N. J. & Su, Y. Toward the first quantum simulation with quantum speedup. Proc. Natl Acad. Sci. USA 115, 9456–9461 (2018).
13. Tacchino, F., Macchiavello, C., Gereace, D. & Bajoni, D. An artificial neuron implemented on an actual quantum processor. npj Quantum Inf. 5, 1–8 (2019).
14. Barenco, A. et al. Elementary gates for quantum computation. Phys. Rev. A 52, 3457–3467 (1995).
15. Mandviwalla, A., Ohshiro, K. & Ji, B. Implementing grover’s algorithm on the IBM quantum computers. In Proc. 2018 IEEE International Conference on Big Data (Big Data) 2531–2537 (IEEE, 2018).
16. Maslov, D. Advantages of using relative-phase Toffoli gates with an application to multiple control Toffoli optimization. Phys. Rev. A 93, 022311 (2016).
17. Reed, M. D. et al. Realization of three-qubit quantum error correction with superconducting circuits. Nature 482, 382–385 (2012).
18. Song, C. et al. Continuous-variable geometric phase and its manipulation for quantum computation in a superconducting circuit. Nat. Commun. 8, 1061 (2017).
19. Li, S. et al. Realisation of high-fidelity nonadiabatic CZ gates with superconducting qubits. npj Quantum Inf. 5, 84 (2019).
20. Levine, H. et al. Parallel implementation of high-fidelity multiqubit gates with neutral atoms. Phys. Rev. Lett. 123, 170503 (2019).
21. Roy, T. et al. Programmable superconducting processor with native three-qubit gates. Phys. Rev. Appl. 14, 014072 (2020).
22. Hendrickx, N. W. et al. A four-qubit germanium quantum processor. Nature 591, 580–585 (2021).
23. Kim, Y. et al. High-fidelity three-qubit iToffoli gate for fixed-frequency superconducting qubits. Nat. Phys 18, 841 (2022).
24. Figgatt, C. et al. Complete 3-qubit Grover search on a programmable quantum computer. Nat. Commun. 8, 1918 (2017).
25. Gidney, C. & Jones, N. C. A CCCZ gate performed with 6 T gates. Preprint at https://arxiv.org/abs/2106.11513 (2021).
26. Lanyon, B. P. et al. Simplifying quantum logic using higher-dimensional Hilbert spaces. Nat. Phys. 5, 134–140 (2009).
27. Mariantoni, M. et al. Implementing the quantum von Neumann architecture with superconducting circuits. Science 334, 61–65 (2011).
28. Fedorov, A., Steffen, L., Baur, M., da Silva, M. P. & Wallraff, A. Implementation of a Toffoli gate with superconducting circuits. Nature 481, 170–172 (2012).
29. Hill, A. D., Hodson, M. J., Didier, N. & Reagor, M. J. Realization of arbitrary doubly-controlled quantum phase gates. Preprint at https://arxiv.org/abs/2108.01652 (2021).
30. Galda, A., Cubbeddu, M., Kanazawa, N., Narang, P. & Earnest-Noble, N. Implementing a ternary decomposition of the Toffoli gate on fixed-frequency transmon qutrits. Preprint at https://arxiv.org/abs/2109.00558 (2021).
31. Arute, F. et al. Quantum supremacy using a programmable superconducting processor. Nature 574, 505–510 (2019).
32. Mooney, G. J., White, G. A. L., Hill, C. D. & Hollenberg, L. C. L. Whole-device entanglement in a 65-qubit superconducting quantum computer. Adv. Quantum Technol. 4, 2100061 (2021).
33. Wu, Y. et al. Strong quantum computational advantage using a superconducting quantum processor. Phys. Rev. Lett. 127, 180501 (2021).
34. Monz, T. et al. 14-qubit entanglement: creation and coherence. Phys. Rev. Lett. 106, 130506 (2011).
35. Song, C. et al. Generation of multicomponent atomic Schrödinger cat states of up to 20 qubits. Science 365, 574–577 (2019).
36. Maslov, D. & Nam, Y. Use of global interactions in efficient quantum circuit constructions. N. J. Phys. 20, 033018 (2018).
37. Gokhale, P. et al. Asymptotic improvements to quantum circuits via qutrits. In Proc. 46th International Symposium on Computer Architecture 554–566 (ACM, 2019).
38. Koch, J. et al. Charge-insensitive qubit design derived from the Cooper pair box. Phys. Rev. A 76, 042319 (2007).
39. Yan, F. et al. Tunable coupling scheme for implementing high-fidelity two-qubit gates. Phys. Rev. Appl. 10, 054062 (2018).
40. Collodo, M. C. et al. Implementation of conditional phase gates based on tunable ZZ interactions. Phys. Rev. Lett. 125, 240502 (2020).
41. Xu, Y. et al. High-fidelity, high-scalability two-qubit gate scheme for superconducting qubits. Phys. Rev. Lett. 125, 240503 (2020).
42. Chu, J. & Yan, F. Coupler-assisted controlled-phase gate with enhanced adiabaticity. Phys. Rev. Appl. 16, 054020 (2021).
43. Cai, T.-Q. et al. Impact of spectators on a two-qubit gate in a tunable coupling superconducting circuit. Phys. Rev. Lett. 127, 060505 (2021).
44. Zajac, D. et al. Spectator errors in tunable coupling architectures. Preprint at https://arxiv.org/abs/2108.11221 (2021).
45. Jiang, Z., Rieffel, E. G. & Wang, Z. Near-optimal quantum circuit for Grover’s unstructured search using a transverse field. Phys. Rev. A 95, 062317 (2017).
46. Erhard, A. et al. Characterizing large-scale quantum computers via cycle benchmarking. Nat. Commun. 10, 5347 (2019).
47. Gilbert, W. et al. On-demand electrical control of spin qubits. Preprint at https://arxiv.org/abs/2201.06679 (2022).
48. Muhonen, J. T. et al. Storing quantum information for 30 seconds in a nanoelectronic device. Nat. Nanotechnol. 9, 896–914 (2014).

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Methods

Coupler-assisted iSWAP_{11, 20}

In the tri-mode (Q−C−Q) system, the static part of the Hamiltonian in the laboratory frame is \( \hat{H}_{\text{static}} \):

\[
H_{\text{static}} = \sum_{i=1, 2} \left( \omega_i a_i^\dagger a_i + \frac{g_{\text{cc}}}{2} (a_i^\dagger a_i + a_i^\dagger a_i) \right) + \sum_{i=1, 2} g_{\text{cc}} (a_i^\dagger + a_i) (a_{12}^\dagger + a_{12}) + \xi_{12} (a_i^\dagger + a_i) (a_{12}^\dagger + a_{12}).
\]  

(2)

Here \( \omega_i \) and \( g_i \) denote the frequency and the anharmonicity of mode \( i \), and \( a_i^\dagger \) is the corresponding annihilation (creation) operator. The qubits Q1 and Q2 couple to the coupler with coupling strength \( g_{\text{cc}} \) and \( g_{\text{cc}} \), respectively, and to each other with a coupling strength \( g_{\text{cc}} \). The time-dependent drive \( H_{\text{drive}} = H_{\text{static}}(t) + H_{\text{adiab}}(t) \) can be divided into an adiabatic part \( H_{\text{adiab}}(t) \) and a diabatic part, that is, the parametric drive, \( H_{\text{static}}(t) = \left( \xi(t) a_i a_i^\dagger + \xi(t) (a_i^\dagger + a_i) \right) \). \( \omega_i \) and \( \theta_i \) denote the frequency and the phase of the parametric pulse, respectively. Note that we have absorbed into the adiabatic part a drive-amplitude-dependent frequency shift, which arises from the nonlinear relation between the coupler frequency and the applied flux. Following the instantaneous eigenbasis defined by \( H_{\text{static}} + H_{\text{adiab}}(t) \), we may rewrite the approximate Hamiltonian of the two-level \((i)\) and \((j)\) system:

\[
H_{\text{TLS}}(t) = \frac{1}{2} \left[ \Delta_i + \xi(t) \beta_{ij} \right] a_i^\dagger a_i + \xi(t) (n_i \delta_{ij} + \text{h.c.}).
\]  

(3)

where \( \delta_{ij} = |i\rangle \langle i| - |j\rangle \langle j| \) is the instantaneous level spacing, \( n_i = \langle a_i^\dagger a_i \rangle \) and \( \Delta_i = \omega_i - \Omega_i \).

Defining the unitary operator \( A(t) = \exp \left[ i \Delta_i t + \frac{\xi(t)}{2} \right] \), where \( \xi(t) = \xi(t) \), we assume a constant drive amplitude \( \Lambda(t) = \beta \), we can express the effective Hamiltonian in the rotating frame as

\[
H_{\text{TLS}}(t) = \Lambda H_{\text{TLS}}(t) + i \partial_t A(t) = \frac{1}{2} \left( \Omega \delta_{ij} + \text{h.c.} \right).
\]  

(4)

where \( \Omega = \beta \left[ \left| J_{\text{cc}} \right|^2 + J_{12}^2 \right] n_i \). In the above equation, we have omitted fast oscillating terms and high-order Bessel terms in the Jacobi−Anger expansion. Here, it can be seen that the effect of the parametric modulation is similar to a Rabi drive between the two selected levels in the instantaneous eigenframe.

Under the resonant condition \( \Delta_i = \omega_i = 0 \), the corresponding unitary operator in this subspace is

\[
U_{\text{TLS}} = \begin{pmatrix} \cos(\Omega t/2) & -ie^{i\theta} \sin(\Omega t/2) \\ -ie^{-i\theta} \sin(\Omega t/2) & \cos(\Omega t/2) \end{pmatrix}.
\]  

(5)

where \( \Omega = |\xi| \) after ignoring an irrelevant initial phase from \( n_i \). The dynamics is a coherent Rabi cycling with an effective Rabi frequency \( \Omega \), in which one can swap excitation between the two levels. A full excitation swap is realized by setting \( \Omega t = \pi \), leading to \( U_{\text{TLS}} = -ie^{-i\theta}(i - e^{i\theta})/\xi \). Note that the phase of the Rabi drive can be controlled by the phase of the parametric drive \( \theta \).

Phase calibration of the QuAND gate

From equation (5), the coupler-assisted iSWAP_{11, 20} operation can be expressed by a unitary \( -ie^{-i\theta}(i - e^{i\theta})/\xi \), where the phase \( \theta \) is controlled by the parametric drive. Because the ancilla state \( \ket{20} \) is used only for temporary storage, the individual phase is irrelevant and only the relative phase between two iSWAP_{11, 20} gates matters. Two consecutive iSWAP-like gates (with phases \( \theta_1 \) and \( \theta_2 \)) cause the state evolution to follow \( |11\rangle \rightarrow -ie^{-i\theta_2}|20\rangle \rightarrow -ie^{i\theta_1-\theta_2}|11\rangle \), restoring the population distribution in the end but with an additional phase factor. Viewed in the computational subspace \((00), (01), (10), (11)\), the extra phase \( \theta \) becomes a conditional phase, which is unwanted if our goal is to retain an identity operation as prescribed in the QuAND scheme. The conditional phase may be eliminated by letting \( \theta_1 - \theta_2 = \pi \). However, in practical implementations, there are a few more details to consider. First, the \( |20\rangle \) state is at a different energy from the \( |11\rangle \) state, and an additional phase accumulates during the idling period between the two iSWAP_{11, 20} gates. After the second iSWAP_{11, 20} gate, this phase shows up as a conditional phase on \( |11\rangle \). Besides idling, an extra phase may also accumulate during the period of frequency modulation. Fortunately, we do not need to measure each of these contributions for correction. These phases can be grouped together as a total conditional phase, which we can calibrate away by sweeping \( \theta \) (assuming an arbitrary \( \theta \)) while measuring the final conditional phase in the conditional Ramsey experiment. Further discussion on the calibration procedures is provided in Supplementary Section V.

Data availability

Data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request. Source data are provided with this paper.

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Author contributions

J.C., X.H. and F.Y. conceived and designed the experiment. Y.Z. and F.Y. designed the devices. J.C. conducted the measurements. J.C., X.H., Y.F. and F.Y. analysed the data. Y.Z., H.J. and L.Z. performed sample fabrication. J.C., X.H., X.S. and F.Y. wrote the manuscript. F.Y., X.S. and D.Y. supervised the project. All authors discussed the results and contributed to revising the manuscript and the Supplementary Information. All authors contributed to the experimental and theoretical infrastructure to enable the experiment.

Competing interests

The authors declare no competing interests.

Additional information

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