An analysis of reversible multiplier circuits

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Abstract

Multiplier circuits play an important role in reversible computation, which is helpful in diverse areas such as low power CMOS design, optical computing, DNA computing and bioinformatics. Here we propose a new reversible multiplier circuit with optimized hardware complexity. The optimized multiplier circuit is compared with the earlier proposals. We have shown that the quantum cost of earlier proposals can be further reduced with the help of existing local optimization algorithms (e.g. template matching, moving rule and deletion rule). A systematic protocol for reduction of quantum cost has been proposed. It has also been shown that the advantage in gate count obtained in some of the earlier proposals by introduction of new reversible gates is an artifact and if it is allowed then every circuit block can be reduced to a single gate. Further, it is shown that the 4x4 reversible gates proposed for designing of a component of multiplier circuit (full adder) is neither unique nor special and many such 4x4 gates may be proposed. As example three such new gates have been presented here and it is shown that the proposed gates are universal. It is also shown that the total cost of our design is minimum.

1 Introduction

In VLSI circuit designing where power dissipation plays an important role, there has been an increasing trend of packing more and more logic elements into smaller and smaller volumes and clocking them with higher frequencies. The logic elements are normally irreversible in nature and according to Landauer’s principle irreversibility logic computation results in energy dissipation due to power loss. This is because, erasure of each bit of information dissipates at least $K T ln 2$ Joules of energy where $K = 1.3806505 \times 10^{-23} m^2kg^2K^{-1}(JoulesKelvin^{-1})$ is Boltzamann’s constant and $T$ is the absolute temperature at which the operation is performed. By 2020 this will become a substantial part of energy dissipation, if Moore’s law continues to be in effect. This particular problem of VLSI designing was realized by Feynman and Bennet in 1970s. In 1973 Bennet [2] had shown that energy dissipation problem of VLSI circuits can be circumvented by using reversible logic. This is so because reversible computation does not require to erase any bit of information and consequently it does not dissipate any energy for computation. Reversible computation requires reversible logic circuits and synthesis of reversible logic circuits differs significantly from its irreversible counterpart because of different factors [4]. The technological requirement of designing of energy dissipation free VLSI circuits, particular characteristics of synthesis and testing of reversible circuits and the tremendous advantage of quantum circuits have motivated scientists and engineers from various background (e.g. Physics, Electronics, Computer science, Mathematics, Material science, Chemistry) to study various aspects of reversible circuits.

Quantum mechanical operations are always reversible and consequently all quantum gates are reversible. A classical reversible gate can not handle superposition of states (qubit) so it forms a special case of quantum circuit or a subset of the set of the quantum circuits. But from the construction point of view classical reversible gates are easy to build [4][5]. A lot of interesting works are already reported in literature in the field of synthesis [6][10], optimization [11], evaluation [12] and testing [13] of reversible circuits. In a short period the reversible computation has emerged as a promising technology having applications in low power CMOS [14], nanotechnology [15], optical computing [16], optical information processing, DNA computing [17], bioinformatics, digital signal processing and quantum computing [18]. It is very clear that reversible circuits will play dominant role in future technologies. These facts have motivated us to do the present work.

Reversible circuits for different purposes eg. half adder, full adder, flip flop [22][23], multiplier [25][29] have been proposed in recent past. Among these reversible circuits, multiplier circuits are of special importance because of the fact that they are the integral component of every computer system, cellular phone and most digital audio/video devices etc. It is important for every processor to have high speed multiplier. In 1997 a low power and high speed irreversible multiplier architecture was proposed by Maaz [30] and thereafter in 2005 its reversible version was proposed by Thapliyal [25]. The proposed reversible circuit required a considerable amount of resources (circuit complexity, quantum cost and garbage bits) and it had several fan outs. Soon various other designs of reversible multiplier circuits were proposed [25][29]. These designs have gradually reduced the quantum cost, circuit complexity and number of garbage bits, but to do so the authors have often introduced New gates [18]. For example, Thapliyal and Srinivas [19] has introduced TSG gate, Haghparast and Navi [21] has introduced MKS gate and HNG gate [21], Islam et. al. [28] has introduced PFAG gate etc in reversible circuit designing. It is important to choose a gate library which is universal. The choice of the gate library
The physical complexity of gates may not be same in two different implementation of reversible circuits. For example, it may be easy to build a particular gate 'A' in MOSFET technology but it may not be that easy to implement it in optical technology \[31, 32\]. Earlier we have shown that the use of New gates to reduce the gate complexity as an artifact \[33\]. An N-qubit reversible gate is represented by \(2^N \times 2^N\) unitary matrix and product of any arbitrary number of unitary matrices is always unitary. Consequently, if we put a set of reversible quantum gates in a black box then an unitary matrix will represent the box and one can technically consider it as a New gate. If we allow such construction of new gates then any circuit block (of arbitrary size) can be reduced to a single New gate. Thus it is straightforward to observe that the use of New gate to reduce the gate count \[18, 21-25\] is an artifact.

Multiplier circuits essentially have two components. Partial product generation and parallel full adder. To construct the full adder several 4x4 gates (e.g. TSG \[19\], MKG \[20\], HNG \[21\] and PFAG \[28\]) have been proposed. We have already mentioned that the reduction of gate count obtained by introduction of such large gates is an artifact. Here we will further show that these gates are neither unique nor special. We will show that different 4x4 gates can be used to construct reversible full adder circuit having gate count one. To establish the point we have shown three different ways in which one can propose a new 4x4 reversible gate which can construct a full adder. We can construct many more such new gates but it does not make any significance as these gates neither reduce quantum cost nor the gate complexity. Recently Mohammadi \[29\] has proposed a new reversible multiplier circuit design with the optimized circuit cost and the quantum cost. We present a systematic protocol to calculate and reduce the quantum cost of a circuit. We have used this protocol to reduced the quantum cost of some multiplier circuits proposed by Mohammadi and others. We have also proposed a novel reversible multiplier circuit using NCT gate library and have discussed some conceptual issues.

In section II we have presented some background of reversible circuits, in section III we have briefly described the past works. Section IV describes our proposed designs and section V is dedicated for conclusions.

### 2 Background

A reversible logic circuit comprises of reversible gates. A gate is reversible if it has equal number of inputs and outputs and the boolean function is bijective. Consider Fig. 1, where input vector \(I\) is \((x_1, x_2, ......x_n)\) and output vector \(O\) is \((y_1, y_2, ......y_n)\) the reversible function satisfies the condition of one to one and onto mapping between input and output domains.

A garbage bit is the additional output that makes an n input output function reversible and it is not used for further computations. Therefore large number of garbage outputs are undesirable in a reversible circuit. As an example in Table I we have shown an irreversible and a reversible AND gate. It is evident that the Z output gives us the required output and the other outputs X and Y are garbage.

Constant inputs are inputs of a reversible circuit with arbitrary constant values. It is important for reversible realization of an irreversible function.

Maslov has prescribed a reversible logic synthesis benchmark \[34\] in which he has suggested several universal gate libraries, which are NCT (NOT, CNOT, Toffoli), NCTSF (NOT, CNOT, Toffoli, Swap Fredkin), GT (generalized n-bit Toffoli) and GT & GF (generalized Toffoli and generalized n-bit Fredkin). Among these libraries NCT library is the smallest complete set. Consequently NCT is a good choice of gate library. Further, these gates can be experimentally realized using MOSFET \[4, 5\] and simple optics \[31, 32\]. Keeping all these facts in mind, we have chosen NCT gate.
library. The circuits from NCT gate library are called NCT circuits. Table II shows the reversible gates that constitutes NCT gate library. To calculate the quantum cost we have also synthesized NCV circuits for the same. This is required because Toffoli is not a quantum primitive gate. The NCV circuits are made using gates from NCV gate library, which includes N, C, controlled V and controlled V+ gates. In [3] the universality of this gate library is proved and this library is also used in earlier work [9, 35]. It is also interesting to note that according to the Solovay-Kitaev theorem [36] translation between different universal sets causes only poly-logarithmic overhead. We have used these facts to compare the quantum cost of our designs of reversible multiplier circuits with the existing proposals.

The quantum cost [12, 35, 37, 38] of a reversible circuit is the number of primitive quantum gates needed to implement a circuit. The quantum cost of primitive gates (1 \times 1) and (2 \times 2) is considered to be one, regardless of their internal structure. We can construct Toffoli with square root of not gate (V) and CNOT and in that construction the total gate count of Toffoli is five [39]. Thus the quantum cost of Toffoli is 5. Following two methods have been provided by Mohammadi [29] to find the quantum cost of a large gate or a circuit

1. Implement a circuit/gate using only the quantum primitive [(1 \times 1) and (2 \times 2)] gates and count them [29, 35, 37].
2. Synthesize the new circuit/gate using the well known gates whose quantum cost is specified and add up their quantum cost to calculate total quantum cost [28, 29].

At this point we would like to mention that quantum cost obtained in these two procedures may be higher than the actual one unless local optimization algorithm is applied to equivalent circuit obtained in terms of quantum primitive gates. Further we would like to mention that there is a conceptual difference between optimization algorithm used for reduction of circuit complexity and the one used for reduction of quantum cost. This is so because in case of circuit optimization we are restricted to a gate library but to reduce the quantum cost we can introduce any new gate as long as the gate is (1 \times 1) or (2 \times 2). Let us show how the modified local optimization algorithm may help. Consider a Fredkin gate as given in Fig 2a. which has 3 Toffoli gates. This can further be reduced by template matching to one Toffoli and two CNOT gates as shown in Fig. 2b. If we substitute the Toffoli gates by quantum primitives we obtain the circuit shown in Fig. 2c. According to Mohammadi's methods [29] the quantum cost is seven. We now apply the moving rule [11] twice to circuit in Fig 2c (the movements are shown by arrows) to obtain Fig. 2d, in which and thus the quantum cost of Fredkin gate is 5. Here we would like to draw your attention towards the fact that the moving rule (which was essentially designed to reduce circuit complexity) has not reduced the circuit complexity but it has reduced the quantum cost.

Thus we have established that local optimization play a very crucial role in reducing the quantum cost, earlier works have not provided adequate attention towards this fact and consequently we observe that quantum cost of several gates proposed in earlier works can be reduced using local optimization algorithms.

We have shown this protocol in Fig. 3 and used it to find quantum cost of our circuit and also the quantum cost of different circuits proposed in [28, 29, 34].

### 3 Past works

The existing reversible multiplier circuits are the reversible counterpart of conventional multiplier circuit proposed by Maaz [30]. It has two important components: the reversible partial product generator circuit (PPGC) and the reversible parallel adder (RPA). First reversible PPGC was proposed by Thapliyal [25] using Fredkin gates but the design had several fan outs and the resource requirement was also high. A Fredkin gate [40] is a 3x3 conservative reversible logic gates and is shown in Fig. 2 and Table III. Another PPGC circuit was proposed using Peres gate [41] but it also had several fan
outs in their designs. A Peres gate is also known as New Toffoli gate, it comprises of a Toffoli and a CNOT gate and it has been preferred over Toffoli gate because of its lower quantum cost. A CNOT gate can be used for reversible (binary) computation in the manner shown in Fig. 4 as a substitute for fan out. We have substituted each fan out by a CNOT gate in the earlier designs (having fan outs) for a fair comparison with other existing designs and our proposed design.

There are many new reversible gates introduced by several authors \[18-21, 28\] to reduce the gate count of multiplier circuit. We have shown the functions of these gates in Table IV. The primary objective behind the introduction of these gates is the fact that the Maslov circuit, TSG, MKG and HNG gates can singly perform the full adder operation. The HNG gate and PFAG gate were claimed to be best reported reversible gates that can work as a full adder because its reported quantum cost was least. But contrary to the earlier claim present protocol establishes that the quantum cost of all these proposals are same. We have shown that these gates are not unique and there can exist several such reversible gates few of them are described in the next section.

We have shown that the quantum cost of Maslov’s full adder is 6, [see Table V] and not 8 as mentioned in \[28, 29, 34\] and thus the new reversible gates do not provide any advantage over Maslov’s full adder circuit. Also after applying moving and deletion rule the quantum cost of PFAG is reduced to 6 from earlier known value of eight \[28, 29\]. Further Mohammadi \[29\] has proposed designs for TSG and MKG reversible gates and has given their quantum cost as 14 and 13 respectively. We find that quantum cost for both the gates can be reduced to 10 each. The primitive circuits equivalent to Maslov, PFAG, New TSG and MKG gates along with their quantum cost are given in Table V. The quantum cost of Maslov’s circuit, PFAG, TSG and MKG found in present work is considerably less compared to the quantum cost found by Mohammadi \[29\].

In Fig. 5 we show that the circuit design proposed by Mohammadi \[29\] for TSG gate is not unique and we propose a circuit design for New gate having same quantum cost as proposed by Mohammadi \[29\].

Here we would also like to note that the universality of earlier proposed 4x4 gates (TSG \[19\], MKG \[20\] and HNG \[21\]) do not provide them any advantage over Maslov’s circuit, PFAG, A₁, A₂ and A₃. This is so because Maslov’s circuit, PFAG, A₁, A₂ and A₃ are also universal. The universality of these are shown in them are shown in Table VI.

### 4 Proposed reversible multiplier circuit

We have proposed PPGC and RPA circuits using NCT gate library. The RPA circuit as shown in Fig. 8 needs reversible full adder (FA) and half adder (HA). As mentioned in earlier section many reversible full adders have been proposed in

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2 The same reduction of quantum cost in both is expected as PFAG is just the black box representation of Maslov’s circuit. This fact can be easily verified by taking appropriate tensor products of unitary operators equivalent to the gates used in Maslov’s circuit.

3 The functions TSG and New TSG are identical as can be verified from Fig 5 and Table V, but the quantum cost of TSG circuit presented in \[29\] is 10 and that of New TSG is 9.
Table 4: Reversible gates introduced by different authors

| Novel Reversible gates | Size | Function |
|------------------------|------|----------|
| New gate               | 3x3  | $A \oplus B \oplus C$
|                        |      | $A \oplus C \oplus B$ |
| TSG                    | 4x4  | $A \oplus C \oplus B' \oplus D$
|                        |      | $(A \oplus C \oplus B') \oplus (D \oplus AB \oplus C)$ |
| MKG                    | 4x4  | $A \oplus B \oplus C$
|                        |      | $(A \oplus D) \oplus C \oplus (B.A \oplus D)$ |
| PFAG                   | 4x4  | $A \oplus B \oplus C$
|                        |      | $(A \oplus B) \oplus C \oplus (B.A \oplus D)$ |
| HNG                    | 4x4  | $A \oplus B \oplus C$
|                        |      | $(A \oplus B) \oplus C \oplus (B.A \oplus D)$ |

Table 5: New reversible gates and their reduced quantum cost

| New reversible gates | quantum implementation | quantum cost |
|----------------------|-------------------------|--------------|
| A - B - C - D        |                         | 6            |
| A - B - C - D        |                         | 6            |
| A - B - C - D        |                         | 9            |
| A - B - C - D        |                         | 10           |

Figure 5: Circuit for a) New gate, b) TSG gate.
Table 6: Proposed new gates can perform all boolean functions.

| Gates   | $A_1$ | $A_2$ | $A_3$ | PPAG-G Mashlov |
|---------|-------|-------|-------|---------------|
| AND     |       |       |       |               |
| NOT     |       |       |       |               |
| NOR     |       |       |       |               |
| XOR & NAND |   |       |       |               |
| OR      |       |       |       |               |

Figure 6: Earlier proposed designs for full adders are given with their non equivalent circuit, quantum circuit using our protocol and its realization as full adder.

the past. For example, the full adder proposed in [28, 29] along with their implementation using quantum primitive gates are given in Fig 6 but these are not unique and several such reversible blocks $A_1$, $A_2$ and $A_3$ as shown in Fig. 7 can exist. The gate count and quantum cost of these circuits are the same as given in Table VII. The proposed reversible blocks $A_1$, $A_2$ and $A_3$ can also be used as half adder and full adder.

The proposed PPGC uses only Toffoli gates as it suffices the requirement and is shown in the Fig. 8. There is an intrinsic advantage of this circuit over others. As it is made up of same gates, it is easy to implement.

5 Conclusions

The earlier designs of reversible circuits use different gate libraries. Therefore for the purpose of comparison of circuit complexity of our proposals, with the existing proposals we have converted the non NCT gates into their equivalent NCT circuits/gates using transformation based algorithm [11] and optimized it using quantum templates [35] and moving and deletion rules, thereafter we replaced the optimized circuit in the original circuit. While comparing with the existing circuits we have substituted each fan out by CNOT. We have found that the PPGC circuit having lowest gate complexity can be achieved through Toffoli gates but the quantum cost is higher in this design. To reduce the quantum cost many

Figure 7: Full adders can be designed using large number of 4x4 gates having same quantum cost and circuit complexity. As example three such new gates are shown here.
Table 7: Table shows that none of the gates has advantage over others as far as construction of full adder is concerned.

| Full Adder | NCT gate count | Quantum cost |
|------------|----------------|--------------|
| Maslov     | 4              | 6            |
| HNG        | 4              | 6            |
| PFAG       | 4              | 6            |
| A₁         | 4              | 6            |
| A₂         | 4              | 6            |
| A₃         | 4              | 6            |

Figure 8: Proposed reversible full adder: a) PPGC b) Reversible multiplier circuit in which output of PPGC are input of RPA as shown here.
Table 8: Table showing comparison of resource cost of proposed PPGC circuit with existing circuits

| Circuit | No. of gates | No. of garbage bits | Quantum cost | TC |
|---------|--------------|---------------------|--------------|----|
| Ours (Toffoli gate) | 16 | 8 | 0 | 104 |
| Mohammadi et al. [29] (Toffoli and Peres gate) | 22 | 8 | 73 | 164 |
| Sharma et al. [28] (Peres gate) | 32 (+12 CNOTs for avoiding fan out ≥4) | 32 | 84 (+12 CNOTs for avoiding fan out ≥76) | 138 |
| Thapliyal and Sinha [25] | 48 (+12 CNOTs for avoiding fan out ≥80) | 32 | 92 | 172 |

Table 9: Table showing comparison of resource cost of proposed reversible multiplier with existing circuits

| Reversible Multiplier | No. of gates | No. of garbage bits | Quantum cost | TC |
|-----------------------|--------------|---------------------|--------------|----|
| Ours                  | 58           | 26                  | 144          | 226 |
| Mohammadi et al. [29] | 63           | 28                  | 137          | 226 |
| Mohammadi et al. [29] | 63           | 28                  | 137          | 226 |
| Islam et al. [27]     | 84           | 92                  | 149          | 286 |
| Haghani et al. [27]   | 84           | 92                  | 149          | 286 |
| Sharma et al. [28]    | 118          | 56                  | 198          | 366 |
| Thapliyal and Sinha [25] | 118       | 56                  | 299          | 495 |

Authors have substituted Toffoli gate by Peres gate but this leads to more garbage bits. Mohammadi has wisely used Toffoli gate and Peres gate to reduce its quantum cost though its circuit complexity increases. Resource requirement of different proposals of PPGC circuits are compared in Table VIII and the resource requirement of complete multiplier circuit is compared in Table IX. We have seen in this particular case that the reduction of circuit complexity often increases quantum cost and vice-versa. This fact suggests to define a new parameter (we may call it total cost; TC) for the quantitative measure of total resource cost of a reversible circuit. Sum of garbage bit, quantum cost and gate count (circuit cost) may be considered as the total cost TC of the circuit. The value of total cost of the circuits shown in Table VIII and IX clearly establishes the present designs and the design proposal by Mohammadi [29] are better than that of others [25-28]. Thus the use of Peres gate does not provide any advantage. Here we would also like to note that the present work has strongly established the importance of modified local optimization algorithm in analysis of quantum cost of a gate. The reduction of quantum cost of existing multiplier circuits obtained by the present protocol is also expected to open up a new window for similar research related to other reversible circuits.

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