Trench based structure to modulate the stress induced by silicide metallized electrodes in semiconductor device

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Abstract. Though the silicide metallized electrodes which are widely used in semiconductor devices have their advantage of low contact resistance, they often induce harmful stress in devices. Considering this, a trench-based structure designed to manipulate the silicide induced stress is reported in this letter. The effects of the structure are demonstrated by the numerical simulation results based on the typical PMOSFETs with their electrodes formed by CoSi2 and NiSi. It is shown that, while the trench-based structure is applied, the harmful tensile channel stress caused by the silicide electrode can be reduced as low as about 50%. As a result, the output current can be increased about 7.5%. These results indicate the potential of this novel trench based structure to serve as the stress modulation structure in the semiconductor device with silicide electrodes.

Keywords. trench; silicide electrode; stress; strain; semiconductor device

1. Introduction

Silicide metallized electrodes are more and more widely used in semiconductor devices for their low contact resistances and high scalability. This trend is increasingly evident in the development of short channel CMOS devices, since the influence of inhomogeneities of surfaces and interfaces becomes increasingly important when device dimensions are reduced. [1] However, as CMOS scales to the nanoscale regime, the electrode induced contact resistance is becoming comparable to the on-state channel resistance, which will considerably lower the on-current and significantly increase the delay. [2] For this reason, researchers have a variety of silicide materials in last several decades, [3-5] among which CoSi2 and NiSi demonstrate the best features. [6] But silicide electrodes are accompanied by some thermal stability problems. [7, 8] In particular, silicide often agglomerates during the electrode fabrication process, and hence induces tensile stress into the device channel. [9, 10] With this problem, silicide electrodes tend to induce unexpected stress in device. In most cases, this kind of stress has detrimental effects on the device. The disadvantages arising from the silicide-induced stress are especially significant in the cases of the short channel PMOSFETs whose electrodes are made of NiSi. In each PMOSFET of this kind, the silicide electrodes always induce tensile stress in the device channel, which in turn makes the hole mobility there reduced due to piezoresistive effect. [11, 12] As a result, the device performance is degraded. [13, 14]

Considering this, a trench-based structure designed to manipulate the silicide induced stress is reported in this paper. Two types of PMOSFETs whose electrodes are made of CoSi2 and NiSi respectively are used to evaluate the effects of the trench-based structure. The results will be indicative while other semiconductor devices with silicide electrodes are considered.
2. Device structure

Fig. 1(a) shows the device structure of the silicide metallic source/drain PMOSFET with a trench-based structure. Unlike the situation in a conventional PMOSFET, there are two trenches near the source and drain respectively. It should be noted that these trenches are not the conventional shallow trench isolation structures for they are not filled up by any silicon oxidation and hence left to be empty.

To evaluate the effects of the trench-based structure on the stress distribution in device and on the device performance, the numerical simulations using Sentaurus TCAD are performed. The gate-thickness and gate-length are set to be 110 nm and 500 nm, respectively. The thickness of the spacer is 20 nm. The electrode-length is 90 nm. The doping concentrations in the substrate and source/drain region are $3 \times 10^{17}$ cm$^{-3}$ and $6 \times 10^{19}$ cm$^{-3}$ respectively. The physical models used in the simulation include hydrodynamic carrier transport model, SRH and Auger recombination model, high-field-saturation mobility model, surface-roughness-scattering mobility model and the piezo models of deformation potential, etc..

![Figure 1. The device structure of the silicide electrode PMOSFET with (a) a trench-based structure and (b) a conventional structure.](image)

3. Results and discussion

3.1. The dependence of the channel stress on the trench size

The simulation results show that the channel stress $\sigma$ is dominated by its xx component $\sigma_{xx}$. Firstly, the dependence of $\sigma_{xx}$ on trench depth is investigated. Without losing generality, the magnitude of the channel stress is characterized by the value of $\sigma_{xx}$ at the middle point of the channel. In the simulation, the trench width is fixed to be 200 nm, and the trench depth varies from 0 nm to 200 nm. With fig.2, it is observed that the depth of 150 nm is a critical value. Only when the trench depth is less than 150 nm, the channel stress significantly decreases with the trench depth. Then, the dependence of $\sigma_{xx}$ on trench width is also evaluated. We investigated two typical situations in which the trench depths are set to be 50 nm and 200 nm respectively. As shown in Fig. 3, the numerical results demonstrate that the channel stress is insensitive to the variation of the trench width.

With the above results, one can regard 150 nm as the optimized trench depth, no matter the trench width is large or small. Therefore, there is no special requirement for the aspect ratio of the trench, which ensures the process realizability of the trench fabrication.
3.2. The dependence of the channel stress on the silicide electrodes’ size

Fig. 4 demonstrates the dependence of the channel stress on the silicide electrode thickness. We use the difference between the middle channel stresses of the trench-based device and the conventional device, say, $\Delta \sigma_{xx}$, to characterize the stress relaxation caused by the trenches. It is observed that $\Delta \sigma_{xx}$ increases with the silicide electrode thickness. Fig. 5 shows the dependence of the channel stress on the silicide electrode length. It is observed that $\Delta \sigma_{xx}$ decreases with the silicide electrode length, which means that the trench based structure is more effective in a device with relatively short silicide electrodes.

3.3. The dependence of the channel stress on the gate length

Figure 6 and figure 7 demonstrate the dependence of the channel stress on the gate length. It is observed that in each of the devices with their gate lengths larger than 30nm but shorter than 150nm, the trench-based structure makes the channel stress effectively relaxed. Fig. 7 shows that, while the trench based structure is adopted, the channel’s tensile stress induced by either the NiSi electrodes or the CoSi2 electrodes can be reduced by about 50%. With fig. 7, it is seen that the effects of the trench based structure on the channel stress has a negative relationship with the gate length.

3.4. devices’ electrical performance

Fig. 8 (a) and (b) show the transfer characteristic curves of the devices with NiSi electrodes and CoSi2 electrodes respectively. The output characteristic curves of these devices are shown in Fig. 9. It is observed that, for each of these two types of devices, the application of the trench based structure
makes both the drain current and the transconductance enhanced. This can be explained by fact that the tensile channel stress which making down the hole mobility is effectively relaxed by the trenches.

Figure 8. The transfer characteristic curves of the (a) NiSi and (b) CoSi2 electrode PMOSFETs with the trench-based structure. For comparison, the transfer characteristic curves of the conventional devices without any trench are also shown.

Figure 9. The Ids-Vds curves of the (a) NiSi and (b) CoSi2 electrode PMOSFETs with the trench-based structure. For comparison, the Ids-Vds curves of the conventional devices without any trench are also shown.

4. Conclusion
In this paper, a trench-based structure to suppress the silicide electrode induced channel stress in the PMOSFET is investigated by numerical simulation. The calculation results show that, while the trench based structure is adopted, the channel’s tensile stress induced by either the NiSi electrodes or the CoSi2 electrodes can be reduced by about 50%. Hence, the degradation of the hole mobility there caused by piezoresistive effect is significantly suppressed. As the consequence, the output drain current and the transconductance are both improved. This work provides a new approach to enhance the performance of sub-micro PMOSFET NiSi or CoSi2 electrodes. It should be noted that this approach is not only limited to the NiSi and CoSi2 electrode devices. In principle, while the metallized electrodes formed by other silicide, such as WSi2, and TiSi2 etc., are considered, the trench based structure mentioned above can also be used to adjust the channel stress and hence to suppress the degradation of hole mobility there.

5. References
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