Class-C architecture for cross-coupled FBAR oscillator to further improve phase noise

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Abstract: In this letter, a class-C architecture for an oscillator employing film bulk acoustic resonator (FBAR) is presented to improve the phase noise significantly in 1/f³ region. The advantages offers by class-C operation are exploited in order to reduce the noise contributed by the current-source transistor in cross-coupled topology. An adaptive biasing circuit is used in order to ensure the oscillation start-up. The post-layout simulation incorporating all parasitic and representing FBAR by modified Butterworth Van Dyke (MBVD) model illustrates the phase noise improvement by 17 dBc/Hz at 100 kHz offset of a 1.9 GHz carrier compared to the FBAR based cross-coupled topology presented by the authors [1].

Keywords: class-C oscillator, FBAR, cross-coupled topology

Classification: Microwave and millimeter-wave devices, circuits, and modules

References

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1 Introduction

In GHz-frequency range applications, the integration of FBAR on CMOS circuit is getting attractive and promising for low noise low power oscillator [1, 2, 3, 4, 5, 6, 7] because of the high quality factor, Q (>1000) offered by the FBAR. Recently, using cross-coupled topology, the present authors also implemented 1.9 GHz oscillator by integrating FBAR on 0.18 µm CMOS wafer [1]. Nevertheless, the proposed topology in [1], which is operating in class-B, suffers from non-idealities of the architecture itself, which prohibits it to achieve better phase noise performance. A preliminary design to mitigate this problem was proposed by employing Class-C operation [8, 9]. In this letter, the reasons for further improvement of phase noise in Class-C operation [8, 9] are further identified, and is employed to design the proposed oscillator by selecting carefully the value of capacitor at the common-source of differential pairs (Ctail) to improve the phase noise further in the flicker noise zone (up to 100 KHz offset) compared to previous class-C design [8, 9]. The post-layout simulation incorporating all parasitic and representing FBAR by modified Butterworth Van Dyke model [10] shows that the proposed design in this letter improves the phase noise at 100 kHz offset from carrier by 3.4 dB than the design presented in [8, 9].

2 The design of class-C CMOS cross-coupled FBAR oscillator

In previous design of class-C FBAR oscillator [7, 8], the class-C operation was achieved by; 1) biasing the gate of the differential pairs (M1/M2 and M3/M4) in
Fig. 1(a) near to the transistor’s threshold voltage by means of RC network, therefore the transistors will always be in saturation region, 2) adding large capacitor $C_{tail}$ to guarantee the generation of impulse-like current waveform, and thus increases the current efficiency and improves the phase noise. Another benefit of having a large capacitor at the source of the differential pairs is it provides a low-impedance path to the ground, therefore the noise that comes from the current source transistors is filtered out. However, the $1/f$ noise from the current source transistors, which will be up-converted as AM by the differential pair, affects the phase noise in $1/f^3$ region due to AM-PM conversion [11, 12], and the improvement of this up-converted noise was not considered in our previous design [7, 8]. The simulation result in Fig. 1(b) shows that we can obtain lower phase noise with larger $C_{tail}$ in $1/f^3$ region, while the phase noise improves slightly (0.4 dB difference between minimum and maximum value) at 1 MHz from the carrier ($1/f^2$ region). At close-in offset frequency, the phase noise is $-82.2$ dBc/Hz and $-98.2$ dBc/Hz for $C_{tail} = 500$ fF and $C_{tail} = 3$ pF respectively. Therefore, there is an improvement of more than 10 dB in $1/f^3$ region by choosing the optimum value of $C_{tail}$.

Fig. 2. (a) Op-amp schematic view (b) transfer function of the op-amp
3 Adaptive biasing circuit

A disadvantage of class-C oscillator is the gate of the transistor pair requires a dynamic biasing. It is because, at start-up, in order to deliver the required amount of transconductance $-gm$, the gate has to be high bias voltage. However, at steady state, the gate bias voltage needs to be reduced in order to ensure the class-C operation. For a complementary cross-coupled topology, the start-up condition is defined by the transconductance of both NMOS and PMOS differential pairs, which is given by $-2/\left(\frac{gm_N + gm_P}{2}\right)$. In order to reduce the complexity of having dynamic biasing circuit for each differential pair, the gate voltage of PMOS pair (M3/M4) is statically biased by the required voltage for the pair to operate in class-C. Therefore, only the gate of NMOS pair will be dynamically biased to ensure the oscillation start-up. For that reason, an operational amplifier (op-amp) is used to control the bias voltage at the gate of M1 and M2, by sensing the variation at the common-source voltage, $V_{cm}$ of the pair, enforcing it to be equal to reference voltage, $V_{ref}$ and adjusting the gate bias voltage accordingly. Since the $V_{cm}$ is the saturation voltage of transistors M5 and M6, $V_{ref}$ is chosen equal to 170 mV.

The op-amp creates a negative feedback for the NMOS pair, therefore it is necessary that the loop is unconditionally stable and does not affect the oscillation. The steady-state error, stability, and accuracy between $V_{cm}$ and $V_{ref}$ depends on the op-amp bandwidth and the DC gain. To ensure the unconditional stability of the loop, a single pole architecture with a DC gain of 25–30 dB is enough [13]. Furthermore, the high output impedance of the current source transistors ensures the stability of oscillation amplitude even though with the presence of the feedback loop [13]. Therefore, a differential amplifier with current mirror load topology is used for the op-amp as shown in Fig. 2(a). The PMOS transistors are chosen as the input pair, and the reasons are two folds; firstly, the small value of $V_{cm}$ and $V_{ref}$ which is less than 200 mV, and secondly, the low $1/f$ noise of PMOS compared to NMOS transistor [14] in order to lower noise contribution from the op-amp. The transfer function in Fig. 2(b) shows that the DC gain of this op-amp is 26 dB, and
the bandwidth is 25.9 MHz. Fig. 3 plots the simulated waveform of output voltage of the oscillator, $V_{out}$, the $V_{cm}$ and the $V_{bias,N}$. At start-up, the output voltage of the op-amp, which is $V_{bias,N}$ that bias the gate of M1 and M2, is high, where $V_{bias,N} \approx 0.78$ V. When the oscillation amplitude starts to grow, the op-amp counteracts the variation of $V_{cm}$ by adjusting the gate bias voltage of the pair in order to keep $V_{cm}$ equal to $V_{ref}$. When it reaches the steady-state, $V_{bias,N}$ is reduced to 0.68 V, which is the required value for M1 and M2 to operate in class-C. Fig. 4(a) shows the layout of the proposed class-C FBAR oscillator.

![Layout of the proposed circuit in 0.18 um CMOS technology](image)

![Phase noise comparison between oscillators](image)

**Fig. 4.** (a) Layout of the proposed circuit in 0.18 um CMOS technology (b) Phase noise comparison between oscillators in this work and in [8].

### 4 Simulation results and discussions

The implementation of class-C cross-coupled FBAR oscillator has been carried out in 0.18 µm CMOS technology. The fundamental frequency of our oscillator is 1.96 GHz. The output harmonics are more than 30 dB below the fundamental oscillation frequency output. While operating at the supply voltage of 1.5 V, this oscillator consumes 1.21 mW DC power, with simulated output power of −2.3 dBm. The simulated phase noise is −98.3 dBc/Hz, −142.4 dBc/Hz, and −156.0 dBc/Hz at 1 kHz, 100 kHz, and 1 MHz offset respectively from 1.96 GHz carrier. Table I shows the summary performance of our FBAR oscillator and the comparison with other published research work. The figure-of-merit (FOM) is used in the comparison, which expression is given by:

$$FOM = L[Δf] + 20 \log_{10}\left(\frac{f_0}{Δf}\right) + 10 \log_{10}\left(\frac{P}{1 \text{ mW}}\right)$$

(1)

By optimizing the value of the capacitors $C_{tail}$ and $C_s$, the phase noise of the proposed oscillator is improved of 3.4 dBc/Hz at 100 kHz offset from the carrier compared to the oscillator in [8], resulting in a FOM of 227. Furthermore, the proposed oscillator is compared with the class-B FBAR oscillator in [1]. There is a significant improvement in phase noise in $1/f^3$ region. At 100 kHz offset form the carrier, the difference of phase noise is 17.4 dBc/Hz. By adopting the class-C operation, the phase noise can be reduced. Moreover, value of some parameters can be optimized for lower phase noise in class-C operation, which is before, could not be done in class-B.
This letter presents a CMOS cross-coupled FBAR oscillator adopting the class-C operation in order to enhance the phase noise performance of the previously proposed FBAR oscillator [1, 8]. The class-C operation gives possibilities to optimize the value of the capacitance at common-source node of the differential pairs, which are previously could not be done in class-B. However, an adaptively biasing circuit is required in order to ensure the oscillation start-up. The design class-C FBAR oscillator oscillates at 1.96 GHz with a phase noise of $-142.4 \text{ dBc/Hz}$ at 100 kHz offset and a power consumption of 1.21 mW, resulting a figure of merit of 227 which is better than 3 dB and 17 dB compared to the previously proposed cross-coupled FBAR oscillators [8] and [1], respectively.

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| Table 1. Comparison with other published oscillator |
|---------------------------------------------------|
| Process  | This work* | [8]* | [1]** | [4]** |
| Topology | Cross-coupled | Cross-coupled | Cross-coupled | Pierce |
| Vdd (V)  | 1.5 | 1.5 | 1.1 | - |
| $f_0$ (MHz) | 1964 | 1964 | 1984 | 1925 |
| Power (mW) | 1.21 | 1.21 | 1.7 | 1.6 |
| Phase noise @ 100 kHz offset (dBc/Hz) | $-142.4$ | $-139$ | $-125$ | $-137$ |
| FOM | 227 | 224 | 209 | 221 |

*post-layout simulation **experimental result