Asymmetrical ZVS-PWM Switched-Capacitor Based Half-Bridge DC-DC Converter With Switch Peak Voltage of Vin/2

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Abstract

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Index Terms - Asymmetrical dc-dc converter, pulse-widthmodulation, switched-capacitor, zero voltage switching.
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I. INTRODUCTION

In recent years, the increasing demand for power sources with high voltage and efficiency and low electromagnetic interference, together with light weight and reduced size, has led to the need for designers to develop new techniques or improve existing ones. Thus, dc-dc converters, which process high levels of power and energy, are currently one of the main subjects of focus in power electronics research.

The asymmetrical half-bridge dc-dc converter, initially presented by P. Imbertson and N. Mohan in [1] and studied in [2-12], presents high gain and high efficiency, soft commutation in the power semiconductors, small number of components, and is one of the most promising topologies in low-to-medium power applications. However, the voltage stresses on the switches are the same as the voltage in its power source, which hinders its implementation in applications that require high input voltages. For this reason, in applications where the input stage is as high as 750-1000 V, this converter is not always a suitable choice, since it would require the use of semiconductors with rated voltages of 1200 V.

Three-level isolated dc-dc converters [13-16] may solve this issue and are the most commonly used solutions for isolated dc-dc converter designs with these specifications. However, they use a larger number of components in the power stage, in addition to the need, in many applications, to control the voltages across the input capacitors, as this equalization does not occur spontaneously. This control requires the use of voltage sensors and additional circuitry, contributing to the increase in equipment cost and complexity. In addition, these topologies are not suitable for asymmetric operation, as this type of operation does not allow the equalization of the voltages in the capacitors. Even for symmetrical topologies, the distribution of voltages across the capacitors is sensitive to the modulation employed or to the imperfections of the gate signals of the switches.

The series asymmetrical half-bridge converter with voltage autobalance is proposed to reduce the power semiconductors voltage stress to half of the input voltage [17]. Besides reducing the voltage across the switches, the proposed solution provides ZVS transition and natural voltage equalization across the input dividing voltage capacitors without control.

As a solution for the issue of high-voltage input, it is also possible to use commutation cells in a switched-capacitor, such as the ladder cell [18]. However, the switched capacitor converter does not allow control of the load voltage by adjustments of the duty cycle D and this is its main disadvantage in relation to conventional converters.

Isolated dc-dc converters combining switched capacitor circuits and conventional isolated dc-dc topologies were proposed, aiming to reduce power switches voltage ratings and allow operation with wide voltage conversion range [19].

With the aim of combining the features of the asymmetrical half-bridge converter and the ladder-type commutation cell, this paper presents the asymmetrical half-bridge switched capacitor converter, as an alternative solution to the issue of high-voltage input, which preserves all the attributes of the original asymmetrical half-bridge converter, such as the output current and soft commutation, with a natural reduction in voltage stress of the components of the power stage to half the voltage value of the power source.

In the proposed converter, as will be shown below, the voltages of the input capacitors are naturally balanced, without the need for control, as usually occurs in isolated dc-dc converters based on multi-level topologies.

II. PROPOSED CONVERTER

The power stage of the proposed converter shown in Fig. 1(a) is comprised of four power semiconductors \( S_1, S_2, S_3 \) and \( S_4 \), two fixed capacitors \( C_1 \) and \( C_2 \), a floating capacitor \( C_8 \), a high frequency transformer \( T_1 \), an output rectifier stage made
up of diodes $D_1$, $D_2$, $D_3$ and $D_4$, and an output filter comprised of $L_0$ and $C_o$. The load is represented by resistance $R_o$. The inductances $L_m$ and $L_c$ represent, respectively, the magnetizing inductance of the transformer and the commutation inductance, usually formed by the leakage inductance of the transformer in addition to an external inductance.

The capacitor $C_d$ is used to block the dc component of the voltage $V_{abr}$ generated due to the asymmetry of the converter, as occurs in the conventional asymmetrical half bridge converter.

![DC-DC hybrid half bridge converter](image)

Fig. 1. (a) DC-DC hybrid half bridge converter. (b) Gate signals.

Fig. 1(b) shows the gate signals of the ideal switches, without the dead time, which will be included later in Section V, where the commutation analysis of the converter switches is made. The proposed converter operates with asymmetrical pulse-width modulation (PWM). The switches $S_1$ and $S_2$ are set to conduct during the time interval $(0- DT_3)$ and $S_2$ and $S_4$ are set to conduct during the complementary time interval $(DT_5-T_3)$.

The voltages across the capacitors $C_1$, $C_2$ and $C_3$ and the switches $S_1$, $S_2$, $S_3$ and $S_4$ are equal to half the voltage of the input source designated by $V_{in}$, this being the additional characteristic of this converter in relation to the conventional asymmetrical half-bridge converter.

### III. OPERATION PRINCIPLES OF THE PROPOSED CONVERTER

In order to simplify the description of the operation and the analysis of the converter in the steady-state regime, the following simplifying hypotheses are adopted: 1) all power semiconductors, inductors and capacitors are considered ideal; 2) the voltages of capacitors are considered constant during a switching period; 3) the inductance $L_o$ of the output filter is considered sufficiently high so that its current can be considered constant during a period of operation; and 4) a single resistance $R_o$, associated in series with the floating capacitor $C_o$, represents all the conduction losses of the power semiconductors.

During a period of operation, the ideal converter has six operation stages which are described as follows. The topological stages are shown in Fig. 2 and the corresponding relevant waveforms are given in Fig. 3.

#### A. First stage of operation ($t_2 - t_5$)

The first stage of operation, which is shown in Fig. 2(a), starts at the moment when the current in the inductance $L_c$ reaches a value equal to the output current reflected to the primary side of the transformer ($I_o'$), thus enabling the switches $S_1$ and $S_3$ to conduct. In this operation stage, the voltage source $V_m$ supplies energy to the converter and the load.

#### B. Second stage of operation ($t_3 - t_4$)

The second stage of operation, which is shown in Fig. 2(b), starts at the moment when $S_1$ and $S_3$ are gated off. The current in the commutation inductance ($i_{lc}$) does not reverse its direction instantly. Thus, the current is conducted through the intrinsic diodes of the switches $S_2$ and $S_4$. All diodes of the output rectifier start to conduct and the voltage at its terminals becomes zero.

#### C. Third stage of operation ($t_4 - t_5$)

The third stage of operation, which is shown in Fig. 2(c), starts at the moment when $i_{lc}$ reaches a null value, reversing its direction. Thus, $i_{lc}$ is conducted through the channels of $S_2$ and $S_4$. All diodes of the output rectifier continue to conduct.

#### D. Fourth stage of operation ($t_5 - t_6$)

The fourth stage of operation, which is shown in Fig. 2(d), starts at the moment when $i_{lc}$ reaches a value equal to $-I_o'$. In this time interval, the capacitor $C_o$ supplies energy for the load. $C_2$ and $C_3$ are connected in parallel, allowing the discharge of $C_5$. This stage is concluded at the moment when the switches $S_2$ and $S_4$ are gated off and $S_1$ and $S_3$ are gated on.

#### E. Fifth stage of operation ($t_6 - t_7$)

The fifth stage of operation, which is shown in Fig. 2(e), starts at the moment when the switches $S_2$ and $S_4$ are gated off. As occurs in the second stage of operation, the current in the commutation inductance is not reversed instantly. Thus, all diodes of the output rectifier start to conduct and the converter does not provide energy transfer for the load.

#### F. Sixth stage of operation ($t_7 - t_8$)

The sixth stage of operation, which is shown in Fig. 2(f), starts at the moment when $i_{lc}$ reaches a null value, therefore reversing its direction and enabling the current, which up to this point is conducted by the intrinsic diodes of the switches $S_1$ and $S_3$, to flow through the channel of the MOSFETs. However, the load voltage remains equal to zero since $i_{lc}$ is lower than the absolute value of $I_o'$.

### IV. THEORETICAL ANALYSIS OF THE PROPOSED CONVERTER

The average value of the load voltage $V_o$ can be determined by analyzing the waveform of the voltage at the terminals of the output rectifier $V_{vrect}$. In order to simplify the analysis, $V_{vrect}$ is reflected to the primary side of the transformer and its waveform is represented in Fig. 4.

On analyzing the topological stages presented in Fig. 2, the equations which define the voltages in the primary side of the transformer are determined. These are presented for the first and fourth stages of operation by expressions (1) and (2), respectively. For the other operating stages the voltage is null, as described in the previous section.
Based on the analysis of the stages of operation, the values for $v_{\text{ret}}$ during the time intervals represented by $t_a$ and $t_b$ are defined by (3) and (4), respectively.

$$v_{\text{ret}(t_a-t_b)} = (1-D)\frac{V_m}{2}$$

$$v_{\text{ret}(t_a-t_b)} = D\frac{V_m}{2}$$

In Fig. 4 it can be noted that, for the time intervals represented by $t_a$ and $t_b$, $v_{\text{ret}}$ is null, which leads to a reduction in the static gain of the converter. Thus, in order to the static gain to be determined it is necessary to determine the time intervals $t_a$ and $t_b$.

On analyzing the waveforms of the voltage and the current on the commutation inductance ($v_{L_c}$ and $i_{L_c}$), in Fig. 3, it can be observed that there is a voltage across $L_c$ only during the time intervals represented by $t_a$ and $t_b$. Thus, the duration of these time intervals can be defined through determining $v_{L_c}$.

$$v_{L_c(t_a-t_b)} = (1-D)\frac{V_m}{2}$$

$$v_{L_c(t_a-t_b)} = -D\frac{V_m}{2}$$

As previously defined, at the moment that $i_{L_c}$ reaches the output current value reflected to the primary side of the transformer, the converter once again supplies energy to the load. Thus, the current in $L_c$ at the moment when the third stage of operation is concluded is equal to $-I_o$. 
Fig. 3. Typical waveforms of the proposed converter.

\[ t_a = \frac{4L_i I_o'}{(1-D)V_{in}} \]  

(5)

\[ t_b = \frac{4L_i I_o'}{DV_{in}} \]  

(6)

Fig. 4. Waveform of the voltage at the output terminals of the bridge rectifier reflected to the primary side of the transformer.

Having defined the values for \( t_a \) and \( t_b \), the average value for the output voltage reflected to the primary is obtained through the following equation

\[ V_o = \frac{1}{T_s} \left[ \int_{t_a}^{DT_a} (1-D) \frac{V_{in}}{2} dt + \int_{DT_a + t_b}^{T_s} (D) \frac{V_{in}}{2} dt \right] \]  

(7)

Evaluating (7), we find the static gain given by

\[ q = \frac{V_o}{V_{in}} = \frac{D(1-D)}{n} - \frac{4f_s L_i I_o'}{nV_{in}}. \]  

(8)

where \( n \) is the transformer turns ratio.

Fig. 5 shows the converter static gain for different values of \( D \) as function of the normalized load current reflected to the transformer primary side, given by

\[ \bar{I}_o = \frac{4f_s L_i I_o'}{V_{in}}. \]  

(9)

To determine the current stresses in the capacitors of the switched-capacitor stage, the non-idealities of the transformer are neglected. Thus, it is considered that the current through commutation inductance is instantly reversed and the proposed converter operates in only two stages.

To simplify the analysis of the switched capacitor stage formed by \( S_1-S_4, C_1, C_2, C_3, R_s, \) and \( V_{in}, \) a current source with a current equal to \( I_o' \) is connected at the terminals \( ab. \)
During the first stage of operation, shown in Fig. 6(b), the instantaneous currents in the capacitors $C_1$, $C_2$ and $C_S$ are given by (10), (11) and (12), respectively.

\[
 i_{C_1}(t) = \frac{D I_o'}{12 f_s \tau} \left( 1 - e^{-\frac{D}{f_s \tau}} \right) e^{\frac{t}{\tau}} + \frac{I_o'}{3} \quad (10)
\]

\[
 i_{C_2}(t) = -\frac{D I_o'}{12 f_s \tau} \left( 1 - e^{-\frac{D}{f_s \tau}} \right) e^{-\frac{t}{\tau}} + \frac{I_o'}{3} \quad (11)
\]

\[
 i_{C_S}(t) = \frac{D I_o'}{6 f_s \tau} \left( 1 - e^{-\frac{D}{f_s \tau}} \right) e^{-\frac{t}{\tau}} + \frac{I_o'}{3} \quad (12)
\]

During the second stage of operation, the above mentioned currents are given by (13), (14) and (15), respectively.

\[
 i_{C_1}(t) = \frac{D I_o'}{4 f_s \tau} \left( 1 - e^{-\frac{(1-D)}{f_s \tau}} \right) e^{\frac{t}{\tau}} \quad (13)
\]

\[
 i_{C_2}(t) = -\frac{D I_o'}{4 f_s \tau} \left( 1 - e^{-\frac{(1-D)}{f_s \tau}} \right) e^{-\frac{t}{\tau}} \quad (14)
\]

\[
 i_{C_S}(t) = \frac{D I_o'}{4 f_s \tau} \left( 1 - e^{-\frac{(1-D)}{f_s \tau}} \right) e^{-\frac{t}{\tau}} \quad (15)
\]

Let us assume that $C_1 = C_2 = C_S = C$. Thus, the time constant $\tau$ is given by

\[
 \tau = \frac{4 C R_s}{3} \quad (16)
\]

The resistance $R_s$ is equal to twice the $R_{\text{dson}}$ resistance of one of the switches, defined in the manufacturer’s data sheet, for the junction temperature provided in the dimensioning of the converter’s power stage.

Using (10), (11), (12), (13), (14) and (15), the effective values of the normalized currents in $C_1$, $C_2$ and $C_S$ are found and represented in Fig. 7 as a function of the product $f_s \tau$, for $D=0.45$.

On analyzing the curves shown in Fig. 7, it can be noted that the effective value of the current in $C_S$ is higher than those in $C_1$ and $C_2$, regardless of the value of $f_s \tau$. It can also be observed that for values of $f_s \tau$ higher than 0.2, the effective values for the currents in the capacitors practically remain constant and close to their minimum values. However, for values of $f_s \tau$ below 0.2, the effective values of the currents increase exponentially, contributing to the elevation of the conduction loss.
V. COMMUTATION ANALYSIS

Due to the asymmetry of the converter, the currents in inductor \( L_c \) at the instant \( S_2 \) and \( S_4 \) are turned off is different from the instant \( S_1 \) and \( S_3 \) are turned off. These currents are given by (17) and (18), respectively.

\[
i_{t_{c1,2}} = I_o' + I_o' (1 - 2D) \left[ 1 - \frac{4f_L I_o'}{D(1-D)V_m} \right] - \frac{D(1-D)nV_m}{4L_m f_s}
\]

\[
i_{t_{c1,3}} = I_o' + I_o' (1 - 2D) \left[ 1 - \frac{4f_L I_o'}{D(1-D)V_m} \right] + \frac{D(1-D)nV_m}{4L_m f_s}
\]

(17)

(18)

The ZVS range depends on the energy stored in the inductor \( L_c \) at the instant of the commutation, to charge and discharge the commutation capacitors associated in parallel with the switches. Thus, the ZVS is not achieved if the necessary energy is not stored in \( L_c \) before the beginning of the commutation. Consequently, the limit load range with ZVS is imposed by the smallest current in \( L_c \), that occurs at the instant the switches \( S_2 \) and \( S_4 \) are turned off.

Due to similarity in the analysis of the two commutations, in this study the analysis for the commutation of switches \( S_3 \) and \( S_4 \) is described, since it is the more critical of the two. Before the start of the commutation, the current \( i_{L_c} \) circulates through switches \( S_2 \) and \( S_4 \) and the corresponding topological stage is given in Fig. 8(a), where \( V_{C2} = V_{C4} = 0 \) and \( V_{C4} = V_{C3} = V_m/2 \).

At time \( t = t_o \), the resonant stage of commutation starts, represented by the topological stage shown in Fig. 8(c). During this time interval the voltage across the inductance \( L_m \) is null and there is some resonance between the inductance \( L_c \) and the commutation capacitance. This stage of commutation ends when \( V_{CS2} = V_{CS4} = V_m/2 \) and \( V_{CS1} = V_{CS3} = 0 \).

In Fig. 9 the main waveforms for turn off of \( S_2 \) and \( S_4 \) are shown.

**B. Resonant stage \( (t_o - t_{oa}) \)**

At time \( t = t_o \) the resonant stage of commutation starts, represented by the topological stage shown in Fig. 8(c). During this time interval the voltage across the inductance \( L_m \) is null and there is some resonance between the inductance \( L_c \) and the commutation capacitance. This stage of commutation ends when \( V_{CS2} = V_{CS4} = V_m/2 \) and \( V_{CS1} = V_{CS3} = 0 \).

In Fig. 9 the main waveforms for turn off of \( S_2 \) and \( S_4 \) are shown.

After time \( t = t_{oa} \), the diodes arranged in antiparallel with \( S_1 \) and \( S_3 \) start to conduct the current \( i_{L_c} \). The corresponding topological stage is shown in Fig. 8(d).

At time \( t = t_{oa} \), the semiconductors are enabled to conduct before the current \( i_{L_c} \) is reversed, so that ZVS is achieved. The dead time \( t_{d2} \) must be longer than the commutation time \( t_{c2} \).

**C. Duration of Commutation**

The duration of the linear stage of the commutation of the semiconductors \( S_2 \) and \( S_4 \) is

\[
t_{c2} = 2C_e \frac{(1-D)V_m}{I_{Lc}}.
\]

(19)

The normalized state plane trajectory is shown in Fig. 10, which represents the resonant stage of commutation, shown in Fig. 8(c).

The duration of the resonant time interval is...
Fig. 10. Normalized state plane trajectory for the resonant stage of soft commutation.

\[
t_{c2} = \frac{1}{\omega} \left[ \frac{\pi}{2} - \cos^{-1} \left( \frac{D V_{in}}{2 \sqrt{\left( \frac{D V_{in}}{2} \right)^2 + \left( Z I_{Lc} \right)^2}} \right) \right]
\]

where

\[
Z = \sqrt{\frac{L_c}{4 C_C}}
\]

and

\[
\omega = \frac{1}{\sqrt{\frac{L_c C_C}{2}}}
\]

The duration of the commutation is the sum of the time intervals \(t_{d2}\) and \(t_{c2}\) and is given by

\[
t_{c2} = t_{d2} + t_{c2}.
\]

As previously mentioned, the dead time \(t_{d2}\) must be longer than the time \(t_{c2}\). Thus,

\[
t_{d2} > t_{c2}.
\]

In general, \(t_{d2} \approx 0\) and can be neglected.

VI. EXPERIMENTAL RESULTS

In order to validate the theoretical analysis of the proposed topology, an experimental prototype was designed and built, as shown in Fig. 11, and its specifications are given in Table I.

| Specifications       | Symbol | Value   |
|----------------------|--------|---------|
| Power Level          | \(P_o\) | 1.4 kW  |
| Input voltage        | \(V_{in}\) | 800 V   |
| Output voltage       | \(V_o\)  | 48 V    |
| Switching frequency  | \(f_s\) | 100 kHz |

The gate signals of the switches, with a dead time of 300 ns between them, generated by a DPS TMS320F28069, are shown in Fig. 12.

In the experimental prototype a voltage clamping circuit was included, comprised of a fast diode (\(D_g\)), a resistor (\(R_g\)) and a capacitor (\(C_g\)), as shown in Fig. 13. This clamping circuit is employed to limit the peaks in the voltage across the diodes \(D_1\), \(D_2\), \(D_3\) and \(D_4\) of the output rectifier, caused by the reverse recovery currents during the commutations.

The voltage clamping circuit allows part of the energy stored in the commutation inductor \(L_c\) to be transferred to the output filter capacitor \(C_o\), which contributes to increasing the efficiency of the converter.

The components employed in the clamping circuit, along with the other components used in the prototype, are given in Table II. The semiconductor used was a (SiC) MOSFET, with a rated drain-source voltage of 650 V.
TABLE II
PARAMETERS OF EXPERIMENTAL PROTOTYPE.

| Component                      | Value   |
|--------------------------------|---------|
| Input capacitor ($C_1$-$C_2$) | 25 µF   |
| Floating capacitor ($C_3$)     | 25 µF   |
| DC blocking capacitor ($C_d$)  | 4.7 µF  |
| Output capacitor ($C_o$)       | 1000 µF |
| Clamp capacitor ($C_g$)        | 4.5 µF  |
| Total commutation inductance ($L_c$) | 9.62 µH |
| Output inductor ($L_o$)        | 25.2 µH |
| Clamp resistor ($R_g$)         | 2.2 kΩ  |
| Diode clamp ($D_g$)            | MUR4100 |
| Secondary side diodes ($D_1$-$D_4$) | MBR40250TG |
| Main switches ($S_1$-$S_4$)    | SCT3120AL / 650 V |
| Transformer turns ratio ($n$)  | 2.25    |
| Magnetizing inductance ($L_m$) | 183 µH  |
| Leakage inductance ($L_k$)     | 1.62 µH |
| Dead time ($t_d$)              | 300 nS  |

Fig. 13. Voltage clamping circuit to limit the voltage across diodes $D_1$, $D_2$, $D_3$, and $D_4$, included in the experimental prototype.

Fig. 14 shows the experimental waveforms of the currents in the primary and secondary windings of the high frequency transformer of the converter, operating with a power of 1.4 kW and rated input and output voltages.

Fig. 14. Current waveforms in the transformer primary and secondary windings.

Fig. 15 shows the experimental waveforms of voltages across the switches $S_1$, $S_2$, $S_3$, and $S_4$. It can be observed that the voltages across them are equal to 400 V, that is, half the value of the input voltage, which is 800 V. The main attribute of this converter in relation to the conventional asymmetrical half-bridge converter, which is the reduction in the voltage stresses on the components of the power stage, is then verified experimentally. It is also verified that the equalization of the voltages across the capacitors occur naturally, without any action of control.

Fig. 15. (a) Voltages across semiconductors $S_1$ and $S_2$. (b) Voltages across semiconductors $S_3$ and $S_4$.

Fig. 16 shows the gate signals and the voltages across the switches $S_1$ and $S_2$ during turning off. It can be observed that both switches turn off with ZVS. The gate signals and the voltages across the switches $S_3$ and $S_4$ presented in Fig. 17 show that both switches also turn off with ZVS.

Fig. 16. Gate signals and voltage stress of semiconductors $S_1$ and $S_2$.

Fig. 17. Gate signals and voltage stress of semiconductors $S_1$ and $S_4$. 
These waveforms show that in the proposed converter, as in the conventional asymmetrical half-bridge converter, the switches operate with soft commutation. The minimum value for the processed power with soft commutation is dependent on the parameters of the converter design, as is the case for all other PWM converters with soft commutation.

The efficiency of the experimental prototype, for different power values, was measured with the aid of a Tektronix power analyzer (PA3000), and the resulting curve is shown in Fig. 18. The maximum efficiency obtained is equal to 93.6% for a power load of 1 kW. The aim of building the prototype was to demonstrate its functioning and validate the theoretical analysis and it was not optimized to reduce losses. The theoretical distribution of the losses is shown in Fig. 19, where it is noted that half of these losses occur in the diodes of the output rectifier stage. Therefore, the replacement of the full bridge rectifier with four diodes, by a midpoint rectifier with two diodes, should contribute to reduce losses and increase efficiency. It is also observed that these losses can be reduced with the use of a better material in the design and construction of the magnetic devices.

Fig. 18. Efficiency of the experimental prototype of the proposed converter.

Fig. 19. Theoretical distribution of losses in the converter power stage.

VII. CONCLUSIONS

A new isolated dc-dc converter topology, generated by the integration of the asymmetrical half-bridge dc-dc converter and the switched-capacitor ladder cell, for high input voltage operation with soft commutation has been proposed. The advantage of the proposed converter with respect to the conventional asymmetrical half-bridge dc-dc converter is the reduction of the voltage stress across the power switches to the half of the input dc bus voltage, enabling the utilization of lower voltage rating power semiconductors. Moreover, in contrast to the isolated three-level dc-dc converters, there is a natural balance of the voltages across the input voltage dividing capacitors, without the need for control. An experimental prototype has been designed, constructed and tested in the laboratory to verify the converter operation principle and the theoretical analysis results. The authors believe that the proposed converter, like the series asymmetrical half-bridge converter with voltage autobalance for high input-voltage introduced in [17], can be a competitive candidate for low-to-medium power and high input voltage applications.

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