Novel Digital Camera with the PCIe Interface

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Abstract—Digital cameras are commonly used for diagnostic purposes in large-scale physics experiments. A typical image diagnostic system consists of an optical setup, digital camera, frame grabber, image processing CPU, and data analysis tool. The standard architecture of the imaging system has a number of disadvantages. Data transmitted from a camera are buffered multiple times and must be converted between various protocols before they are finally transmitted to the host memory. Such an architecture makes the system quite complicated, limits its performance and, in consequence, increases its price. The limitations are even more critical for control or protection systems operating in real-time.

Modern megapixel cameras generate large data throughput, easily exceeding 10 Gb/s, which often requires some additional processing on the host side. The optimal system architecture should assure low overhead and high performance of the data transmission and processing. It is particularly important during the processing of data streams from several imaging devices, which can be as high as several terabits per second.

A novel architecture of image acquisition and processing system based on the PCI Express interface was proposed to meet the requirements of real-time imaging systems applied in large-scale physics experiments. The architecture allows to transfer an image stream directly from the camera to the data processing unit and therefore significantly decreases the overhead and improves performance.

Two various architectures will be presented, compared and discussed in the paper.

Index Terms—Digital Camera, Image Acquisition, Image Processing, Camera Interface, PCI Express Interface, Programmable Device, Plasma Diagnostics, Beam Diagnostics

I. INTRODUCTION

Digital cameras are usually applied for diagnostic purposes in various large-scale physics experiments. A good example is the imaging system for beam diagnostics in particle accelerators that allow measuring the beam charge profile or its transverse emittance [1]. Another example is plasma diagnostics in tokamaks [2] or stellarators [3], such as the imaging systems of the ITER tokamak that require more than 200 digital cameras working in the visible, infrared, and gamma radiation range [4]. Tokamak vision systems should allow for the image acquisition and processing with the resolution of 1 to 8 million pixels registered within the range of 50 to 50000 frames per second. For example, a digital 8-bit camera with a resolution of 1 megapixel working with a frame rate of 1000 frames per second generates a stream of data not less than 8 Gb/s. In this situation, the tokamak image acquisition system, which provides a stream of data from 10 cameras, requires a data throughput of at least 80 Gb/s.

A classic approach to capturing and computing video data is presented in Fig. 1. The system interfaces with several cameras, performs data processing and provides the resulting streams to archiving and machine control networks. The system should provide synchronisation and timestamping of the images from the cameras with an accuracy better than 50 ns (rms). The image acquisition system needs to process the images in real-time, providing information to the safety subsystems in order to protect the tokamak against damage. Such data should be processed in less than 100 µs. Moreover, the data used to control the plasma should be delivered in less than tens of ms.

Field Programmable Gate Array (FPGA) devices are applied for low latency and relatively simple image processing to meet real-time constraints of several ms or less. However, more complex, but less time-critical algorithms could be implemented using a standard CPU with a parallel GPU (Graphics Processing Unit) acceleration.

The development of an efficient and simple architecture suitable for processing of large amounts of data in real-time is a challenging task especially in systems computing data from cameras equipped with various camera interfaces. Unification and standardisation of camera interface could simplify the architecture, however the system still suffer from multiple data copying and buffering.

II. ARCHITECTURE

The standard architecture of imaging system (Fig. 2) consists of:

- a Camera – converting optical signal to electrical and transferring it via a dedicated Camera Interface (CI) protocol,
- a Frame Grabber – capturing data from the Camera Interface and converting to the PCI Express (PCIe) host interface,
- a Host Computer – receiving and processing raw data stream, controlling the camera.

Camera sensor registers images that are further processed with either a dedicated Application-Specific Integrated Circuit...
This approach eliminates the need for a separate Camera Interface and for a Frame Grabber. The Camera Interface is often the main bottleneck of the whole path, whereas the Frame Grabber is a source of an additional latency. The FPGA and memory available in the camera could be used for the PCIe transmission and therefore there is no additional costs for such a design.

The architecture of the novel image acquisition system proposed by the authors is shown in Fig. 3.

A direct application of the PCIe interface in the camera enables unprecedented transmission rates. A single (x1) PCIe gen. 3 lane offers more throughput (~7.88 Gb/s) than the highest speed mode of the legacy Camera Link interface (~7.14 Gb/s). The two further generations of the standard allow to transfer with data rates up to ~16 Gb/s (PCIe gen. 4) and ~32 Gb/s (gen. 5). The interface throughput could be also easily scaled and adjusted for camera needs reaching up to 504 Gb/s when 16 lanes of PCIe gen. 3 are used, see Fig. 3.

The camera architecture based on the PCIe Express standard allows to obtain the most optimal design for the image acquisition and processing system. This allows to decrease the total latency, decrease the price of the system and improve the total performance. Since the PCIe is a well standardised interface and it is maintained by the Peripheral Component Interconnect Special Interest Group (PCI-SIG), it guarantees an easy and simple upgrade path to the future revisions and full compatibility with future computers.

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