Analog / Radio-Frequency Performance Analysis of Nanometer Negative Capacitance Fully Depleted Silicon-On-Insulator Transistors

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Abstract: The negative capacitance field-effect transistor can break the limitation of the Boltzmann tyranny. In this study, the analog and radio-frequency (RF) performance of a nanometer negative-capacitance fully depleted silicon-on-insulator (NC-FDSOI) transistor is investigated. The analog/RF parameters of the NC-FDSOI device are compared with the conventional FDSOI counterparts for transconductance, output conductance, gate capacitance, cutoff frequency, and maximum oscillation frequency. In addition, the effect of ferroelectric thickness on the analog/RF performance of NC-FDSOI device is analyzed and discussed. The results show that even when operated at low voltages, NC-FDSOI transistors enable analog/RF performance improvement in traditional FDSOI counterparts at low power in the case of a suitable ferroelectric thickness.

Keywords: negative capacitance effect; NC-FDSOI transistor; analog / RF Performance; ferroelectric capacitance

1 Introduction

In the past decade, complementary metal-oxide-semiconductor (CMOS) transistors have experienced unprecedented development, shrinking device sizes, and advances in integrated device design and fabrication, bringing the CMOS technology into the nanometer era. However, continued miniaturization has also brought about various new constraints, such as high-power consumption caused by chip overheating [1]. To solve these problems, steep switching characteristics and lower operating voltage can be achieved by lowering the sub-threshold slope (SS). NCFETs based on ferroelectric on a gate stack have attracted significant attention in the field of advanced CMOS devices due to their lower SS (<60 mV/decade) [2]-[8]. Recently, NCFETs have proven to be suitable for a variety of low-
power applications, such as wearables, bioelectronics, and the Internet of Things [9]-[12]. Furthermore, with the advent of the 5G era in radio-frequency (RF) applications, the analog/RF performance of NCFETs must be tested. FDSOI technology is popular because it better overcomes short channel effects and is significantly less expensive to manufacture than fin field effect transistors (FinFETs). In previous studies, FDSOI transistors showed good analog/RF performance [13, 14]. However, the relationship between the negative capacitance effect and analog/RF performance parameters for FDSOI devices is not still understood. Therefore, in this work, we address this deficiency by simulating analog/RF performance of 20-nm NC-FDSOI transistors with different ferroelectric thicknesses ($T_{fe}$) utilizing a computer-aided-design (TCAD) tool.

## 2 Materials and methods

At present, most negative-capacitance transistors are implemented by adding ferroelectric materials [15]-[20]. There are two main types of structures used in the negative capacitance transistors: metal-ferroelectric-metal insulator-semiconductor (MFMIS) and metal-ferroelectric insulator-semiconductor (MFIS). Owing to the better performance of the MFMIS NCFET in terms of it being hysteresis-free [21], a NCFET with MFMIS structure is used in this work. Then, the TCAD tool is used to add a ferroelectric capacitor to the gate on the underlying conventional FDSOI to form an NC-FDSOI transistor. The structure of the FDSOI and NC-FDSOI transistor are shown in Fig. 1. The gate of NC-FDSOI used an HfO2 based ferroelectric with coercive field, $E_c = 1$ MV/cm and remnant polarization, $P_r = 5$ μC/cm2. For better compatibility with the CMOS process [22], a smaller ferroelectric thickness is chosen ($T_{fe} = 1, 2, 3, and 4$ nm).

The device parameters used for numerical simulation are summarized in Table 1. The TCAD mixed-mode device simulator is used to simulate the NC-FDSOI and FDSOI transistors [23], and the frequency characteristics of the NCFDSOI and FDSOI are discussed by AC small-signal analysis. The simulation uses a variety of physical models, such as Fermi statistics, doping-dependent mobility, high-field saturation, mobility degradation at interfaces, Shockley-Read-Hall recombination, and density-gradient quantization. The Poisson and Landau-Khalatnikov equations are solved self-consistently by the TCAD tool [24, 25]. The LK equation, which relates the polarization ($P$) and electric field ($E$), is given in Eq. (1) [26, 27]:

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho \frac{dP}{dt}$$  \hspace{1cm} (1)

where $\alpha$, $\beta$, $\gamma$, and $\rho$ are ferroelectric material parameters and $P$ is the polarization strength. In this work, RF performance parameters are extracted from the two-port network.

### Table 1: device structural parameters

| Parameter                   | FDSOI | NC-FDSOI |
|-----------------------------|-------|----------|
| Channel Length ($L_g$)      | 20nm  | 20nm     |
| Spacer Length ($L_{sp}$)    | 10nm  | 10nm     |
| Channel Doping ($N_d$)       | $10^{14}$cm$^3$ | $10^{14}$cm$^3$ |
| Channel Thickness ($T_{channel}$) | 5nm  | 5nm     |
| Oxide Thickness ($T_{ox}$)  | 0.9nm | 0.9nm    |
| Work-function ($\Phi_m$)    | 4.52  | 4.52     |
| ferroelectric thickness ($T_{fe}$) | 0, 1, 2, 3, 4nm | 0, 1, 2, 3, 4nm |
| Coercive Field ($E_c$)      | 0     | 1MV/cm$^3$ |

### 3 Results and discussion

Fig. 2(a) and (b) shows the transfer characteristics of drain current ($I_{ds}$) versus gate voltage ($V_{gs}$) for a conventional FDSOI and NC-FDSOI fixed at drain voltages ($V_{ds}$) of 0.7 and 0.05 V. It can be seen that the current of the NC-FDSOI is always greater than that of the FDSOI, and the SS is lower, whether it is working in a linear or saturated region. The results show that the current-amplifi-
cation capability of the NC-FDOI is significantly stronger than that of the conventional FDSOI (~60% addition, $T_{fe}=3$ nm) at $V_{ds}=0.7$ V. When the thickness of the ferroelectric ($T_{fe}$) of the NC-FDSOI is set to 6 nm, SS = 43 mV/decade breaks the limit of the SS for the transistor at room temperature, where SS is extracted from Eq. (2):

$$SS = \frac{1000}{d/d_{V_{gs}} \log_{10} I_{ds}}$$

As the SS decreases, the ratio of on- and off-state currents ($I_{on}/I_{off}$) increases compared to the FDSOI, which indicates that the NC-FDSOI is more suitable for high-speed switching applications than the conventional FDSOI. Experiments under actual environmental measurements also show that NC-FDOSI has good current amplification capability and low SS, which the SS is reduced from 78 mV/decade to 73 mV/decade, and the drain current is increased from 4 μA to 7 μA [28]. Fig. 2(c) and (d) shows the output characteristics of $I_{ds}$ versus $V_{ds}$ for their fixed values at $V_{gs}=0.7$ and 0.4 V. As shown in Fig. 2(c) and (d), the ferroelectric has an enhanced effect on the output characteristics of the device, whether at high or low $V_{gs}$. However, at low $V_{gs}$, the internal gate voltage ($V_{in}$) is lowered due to the influence of the ferroelectric, and the negative differential resistance (NDR) effect is generated [29].

Figure 2: (a) $I_{ds}$ with $V_{gs}$ for FDSOI and NC-FDSOI at $V_{ds}=0.7$ V. (b) $I_{ds}$ with $V_{ds}$ for FDSOI and NC-FDSOI at $V_{gs}=0.05$ V. (c) $I_{ds}$ with $V_{gs}$ for FDSOI and NC-FDSOI at $V_{ds}=0.7$ V. (d) $I_{ds}$ with $V_{ds}$ for FDSOI and NC-FDSOI at $V_{gs}=0.4$ V.

Figure 3: (a) Transconductance ($g_{m}$) with $V_{gs}$ for FDSOI and NC-FDSOI. (b) output conductance ($g_{ds}$) with $V_{ds}$ for FDSOI and NC-FDSOI.
Fig. 3(a) shows transconductance ($g_m$) with $V_{gs}$ at $V_{ds} = 0.7$ V and the output conductance ($g_{ds}$) as a function of $V_{gs}$, fixed at $V_{gs} = 0.7$ V, where $g_m$ determines the device’s gain. The $g_m$ and $g_{ds}$ values for both the devices are obtained by Eqs. (3) and (4), respectively:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}}$$

(3)

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}}$$

(4)

It can be clearly seen from Fig. 3(a) and (b) that the $g_m$ and $g_{ds}$ values of the NC-FDSOI are much larger than those of the FDSOI device, and the $g_m$ and $g_{ds}$ values of the NC-FDSOI are further increased as the thickness of the ferroelectric increases. As the current gain decreases, $g_m$ will gradually decrease after reaching the peak, but overall it will be larger than that of the FDSOI. This indicates that the NC-FDSOI transistor gain increases as $T_{fe}$ increases within a certain range due to the negative-capacitance effect. The high transconductance makes the NC-FDSOI suitable for high-gain amplifier applications.

Fig. 4(a) and (b) shows the total gate capacitance ($C_{gg}$) and ferroelectric capacitance ($C_{fe}$) of the NC-FDSOI with $V_{gs}$ at different ferroelectric thicknesses ($T_{fe} = 1$, 2, 3, and 4 nm). Simply lowering the threshold voltage ($V_{th}$) and lowering SS is not enough to improve circuit performance. The important device parameters that affect performance specifications, such as power dissipation and intrinsic delay, are the total gate capacitance [30]. Therefore, it is necessary to analyze the impact of the ferroelectric thickness in the gate stack on $C_{gg}$. As shown in Fig. 4(a), as the thickness of the ferroelectric increases, the gate capacitance increases compared with the FDSOI total capacitance ($C_{gg}^{mos}$). As shown in Fig. 4(b), this is mainly due to the decrease in the absolute value of the ferroelectric capacitance ($C_{fe}$). Fig. 4(c) shows the variation of $C_{gg}$ with frequency at $V_{gs} = 0.4$ and 0.7 V. In Fig. 4(c), $C_{gg}$ begins to decrease after approximately 100 GHz, and the $C_{gg}$ of NC-FDSOI is larger at $V_{gs} = 0.4$ V. This result is consistent with that shown in Fig. 4(a).

In Fig. 5(a) and (b), the cutoff frequency ($f_c$) and maximum oscillation frequency ($f_{max}$) with $V_{gs}$ at $V_{ds} = 0.7$ V, where $f_c$ is extracted from current gain (h21) through an extrapolation of a 20-dB/decade slope, and $f_{max}$ is extracted from Mason’s unilateral gain through an extrapolation of a 20-dB/decade slope. It can be seen from Fig. 5(a) that the maximum $f_c$ of the NC-FDSOI is the same as that of the conventional FDSOI. However, with the increase of $V_{gs}$, the NC-FDSOI leads to $f_c$ achieving peaks at lower $V_{gs}$, which is caused by a decrease in $V_{th}$ as $T_{fe}$ increases [31]. It can be seen from Eq. (6) that $f_{max}$ is mainly affected by $f_c$ and gate resistance ($R_g$), so $f_{max}$ in Fig. 5(b) is the same as the $f_c$ trend and peaks at a lower gate voltage. Under the influence of $g_{ds}$ reduction, $f_c$ and $f_{max}$ gradually decrease after reaching
the peak value and are lower than that of the FDSOI at high gate voltage, and the RF performance of the circuit will deteriorate at high gate voltage. Therefore, the NC-FDSOI performs better at low bias voltages:

\[ f_T = \frac{g_m}{2\pi C_{ss}} \]  
(5)

\[ f_{\text{max}} = \frac{f_T}{\sqrt{4R_g \left( \frac{g_{ds}}{2} + 2\pi f_TR_gC_{gd} \right)}} \]  
(6)

4 Conclusions

In this work, a comparison of analog/RF performance between NC-FDSOI and FDSOI transistors is demonstrated, and the effects of ferroelectric thickness on the analog/RF parameters of the NC-FDSOI are analyzed. The \( f_{\text{max}} \) was measured for the first time, and through a one-to-one comparison with FDSOI, the high frequency dependence of the \( C_{gg} \) and the \( V_{ds} \) dependence of the \( g_{ds} \) were achieved for the first time. The results show that the NC-FDSOI is superior to the conventional FDSOI in terms of \( SS, g_m \), and \( g_{ds} \), and the effect is more significant with the increasing thickness of the ferroelectric. After the addition of the ferroelectric negative capacitance, the \( f_T \) and \( f_{\text{max}} \) values of the NC-FDSOI also peak at a low bias voltage. Therefore, in the case of a suitable \( T_{fe} \), the NC-FDSOI can not only outperform the conventional FDSOI in terms of digital circuits but also achieve better analog/RF performance compared to the FDSOI with reduced power consumption. In the future we will also study the effects of different ferroelectric parameters on analog/RF performance.

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6 Conflict of Interest

The authors declare no conflict of interest. The founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results.

7 References

1. H. Amrouch, G. Pahwa, A. D. Gaidhane, et al.: “Negative Capacitance Transistor to Address the Fundamental Limitations in Technology Scaling: Processor Performance,” IEEE Access, 6, 52754-52765, 2018, https://doi.org/10.1109/ACCESS.2018.2870916.

2. W.F. Lü, L. Dai, Z. F. Zhao et al.: “Performance Improvements of Random Dopant Fluctuation-Induced Variability in Negative Capacitance MOSFETS,” Fluctuation and Noise Letters, 19, 205002, 2020, https://doi.org/10.1142/S0219477520500029.

3. H. Agarwal, P. Kushwah, Y. K. Lin, et al.: “Proposal for Capacitance Matching in Negative Capacitance Field Effect Transistors,” IEEE Electron Device Letters, 40, 3, 463-466, 2019, https://doi.org/10.1109/LED.2019.2891540.

4. P. H. Cheng, Y. T. Yin, I. N. Tsai, et al.: “Negative capacitance from the inductance of ferroelectric switching,” Communications Physics, 2, 1, 1-8, 2019, https://doi.org/10.1038/s42005-019-0120-1.
5. M. Y. Kao, Y. K. Lin, H. Agarwal, et al.: “Optimization of NCFET by Matching Dielectric and Ferroelectric Nonuniformly along the Channel,” IEEE Electron Device Letters, 40, 5, 822-825, 2019, https://doi.org/10.1109/LED.2019.2906314.
6. J. Zhou, G. Han, J. Li, et al.: “Negative Differential Resistance in Negative Capacitance FETs,” IEEE Electron Device Letters, 39, 4, 622-625, 2018, https://doi.org/10.1109/LED.2018.2810071.
7. S. Smith, K. Chatterjee, S. Salahuddin, et al.: “Multi-domain Phase-Field Modeling of Negative Capacitance Switching Transients,” IEEE Transactions on Electron Devices, 65, 1, 295-298, 2018, https://doi.org/10.1109/TED.2017.2772780.
8. H. Mehta, H. Kaur: “Study on Impact of Parasitic Capacitance on Performance of Graded Channel Negative Capacitance SOI FET at High Temperature,” IEEE Transactions on Electron Devices, 66, 7, 2904-2909, 2019, https://doi.org/10.1109/TED.2019.2917775.
9. P. Sharma, J. Zhang, K. Ni, et al.: “Time-Resolved Measurement of Negative Capacitance,” IEEE Electron Device Letters, 39, 2, 272-275, 2018 https://doi.org/10.1109/LED.2017.2782261.
10. M. A. Alam, M. Si, P. D. Ye, et al.: “A critical review of recent progress on negative capacitance field-effect transistors,” Applied Physics Letters, 114, 9, 090401, 2019, https://doi.org/10.1063/1.5092684.
11. C. Cheng, C. C. Fan, C. Y. Tu, et al.: “Implementation of Dopant-Free Hafnium Oxide Negative Capacitance Field-Effect Transistor,” IEEE Transactions on Electron Devices, 66, 1, 825-828, 2019, https://doi.org/10.1109/TED.2018.2881099.
12. M. H. Lee, P. G. Chen, S. T. Fan, et al.: “Ferroelectric Al:HF02 negative capacitance FETs,” IEEE International Electronic Devices Meeting, 2017, 565-568, https://doi.org/10.1109/EDM.2017.8268445.
13. B. K. Esfeh, V. Kilchytska, V. Barral, et al.: “Assessment of 28nm UTBB FD-SOI technology platform for RF applications: Figures of merit and effect of parasitic elements;” Solid-state Electronics, 117, 130-137, 2016, https://doi.org/10.1016/j.sse.2015.11.020.
14. R. Carter, J. Mazurier, L. Pirro, et al.: “22nm FD-SOI technology for emerging mobile, Internet-of-Things, and RF applications,” IEEE International Electron Devices Meeting, 2016, 27, https://doi.org/10.1109/IEDM.2016.7838029.
15. C. Jiang, M. Si, R. Liang, et al.: “A Closed Form Analytical Model of Back-Gated 2-D Semiconductor Negative Capacitance Field Effect Transistors;” IEEE Journal of the Electron Devices Society, 6, 1, 189-194, 2018, https://doi.org/10.1109/JEDS.2017.2787137.
16. H. Lee, Y. Yoon, C. Shin: “Current-Voltage Model for Negative Capacitance Field-Effect Transistors,” IEEE Electron Device Letters, 38, 5, 669-672, 2017, https://doi.org/10.1109/LED.2017.2679102.
17. M. A. Alam, M. Si, P. D. Ye, et al.: “A critical review of recent progress on negative capacitance field-effect transistors,” Applied Physics Letters, 114, 9, 090401, 2019, https://doi.org/10.1063/1.5092684.
18. T. Srimani, G. Hills, M. D. Bishop, et al.: “Negative Capacitance Carbon Nanotube FETs,” IEEE Electron Device Letters, 39, 2, 304-307, https://doi.org/10.1109/LED.2017.2781901.
19. M. Bansal, H. Kaur: “Impact of negative capacitance effect on Germanium Double Gate, p FET for enhanced immunity to interface trap charges;” Superlattices and Microstructures, 117, 189-199, 2018, https://doi.org/10.1016/j.spalmat.2018.03.001.
20. H. Mulasmanovic, T. Mikolajick, S. Slesazeck: “Random Number Generation Based on Ferroelectric Switching;” IEEE Electron Device Letters, 39, 1, 135-138, 2018, https://doi.org/10.1109/LED.2017.2771818.
21. G. Pahwa, T. Dutta, A. Agarwal, et al.: “Physical Insights on Negative Capacitance Transistors in Nonhysteretic and Hysteretic Regimes: MFMIS Versus MFIS Structures,” IEEE Transactions on Electron Devices, 65, 3, 867-873, 2018, https://doi.org/10.1109/TED.2018.2794499.
22. T. Dutta, G. Pahwa, A. R. Trivedi, et al.: “Performance Evaluation of 7-nm Node Negative Capacitance FinFET-Based SRAM,” IEEE Electron Device Letters, 38, 8, 1161-1164, 2017, https://doi.org/10.1109/LED.2017.2712365.
23. S. Tayal, A. Nandi: “Analog/RF performance analysis of channel engineered high-K gate-stack based junctionless Trigate-FinFET,” Superlattices and Microstructures, 112, 287-295, 2017, https://doi.org/10.1016/j.spmi.2017.09.031.
24. Y. K. Lin, H. Agarwal, P. Kushwaha, et al.: “Analysis and Modeling of Inner Fringing Field Effect on Negative Capacitance FinFETs,” IEEE Transactions on Electron Devices, 66, 4, 2023-2027, 2019, https://doi.org/10.1109/TED.2019.2899810.
25. C. Jiang, R. Liang, J. Wang, et al.: “Simulation-based study of negative capacitance double-gate junctionless transistors with ferroelectric gate dielectric;” Solid-state Electronics, 126, 130-135, 2016, https://doi.org/10.1016/j.sse.2016.09.001.
26. R. Singh, K. Aditya, S. S. Parihar, et al.: “Evaluation of 10-nm Bulk FinFET RF Performance—Conventional Versus NC-FinFET;” IEEE Electron Device Letters, 39, 8, 1246-1249, 2018, https://doi.org/10.1109/LED.2018.2846026.
27. K. Chatterjee, A. J. Rosner, S. Salahuddin, et al.: “Intrinsic speed limit of negative capacitance transistors,” IEEE Electron Device Letters, 38, 9, 1328-1330, 2017, https://doi.org/10.1109/LED.2017.2731343.

28. D.W. Kwon, K. Chatterjee, A.J. Tan, et al.: “Improved Subthreshold Swing and Short Channel Effect in FDSOI n-Channel Negative Capacitance Field Effect Transistors,” IEEE Electron Device Letters, 39, 2, 300-303, 2018, https://doi.org/10.1109/LED.2017.2787063.

29. S. Gupta, M. Steiner, A. Aziz, et al.: “Device-Circuit Analysis of Ferroelectric FETs for Low-Power Logic,” IEEE Transactions on Electron Devices, 64, 8, 3092-3100, 2017, https://doi.org/10.1109/TED.2017.2717929.

30. J. Madan, R. Chaujar: “Gate Drain Underlapped-PNIN-GAA-TFET for Comprehensively Upgraded Analog/RF Performance,” Superlattices and Microstructures, 102, 17-26, 2017, https://doi.org/10.1016/j.spmi.2016.12.034.

31. Y. Li, Y. Kang, X. Gong, et al.: “Evaluation of Negative Capacitance Ferroelectric MOSFET for Analog Circuit Applications,” IEEE Transactions on Electron Devices, 64, 10, 4317-4321, 2017, https://doi.org/10.1109/TED.2017.2734279.