Low-Jitter CMOS Digital PLL for the generation of the clock in synchronous serial communication systems

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Abstract: The major building block of linear systems is the Phased Locked-Loop (PLL). Contrasting to analog PLL, the clock period profile of digital PLL (DPLL) is often segmented. Hence the phase and/or frequency tracking of traditional PLL’s may suffer from large jitter when Voltage Controlled Oscillator (VCO) operating point shifts from one clock period segment to another. To address this issue, a Low-Jitter CMOS Digital PLL for the generation of the clock in synchronous serial communication systems is presented in this paper. The design of the PLL will be implemented by considering important CMOS parameters like propagation delay, jitter performance, and power dissipation. Designing of digital PLL includes the design of a phase detector, LPF, Error amplifier, and VCO. The VLSI realization of digital PLL is implemented using the TANNER EDA software tool using a 0.18µm CMOS process.

Keywords: Digital Phase-Locked Loop, Error amplifier, Phase detector, VCO, RMS Jitter.

1. Introduction

Advances in the process of VLSI production have contributed to a rise in circuit clock frequencies. Today several hundred megahertz frequencies are within reach. Unfortunately, difficulties are found in the propagation of clock signals over a whole device at such high frequencies. It is not possible to have an external clock, thereby the requirement of an on-chip clock generator for high-speed synchronous devices [1]. The overall device output is increasingly decided by the clock generation network itself, and, clocking becomes a core constraint on the VLSI architecture.

In several full custom designs, clock multipliers are extensively employed like high-end microprocessors and DSP processors [2]. But the time to market for ASIC is crucial and, as a result, the full custom approach is not feasible. Frequency multiplication can be realised by several methods: analogue PLL [3], digital PLL [4], and delay-locked loop (DLL) [5], [6]. The first one requires not only more time for locking but also needs internal or external or analogue elements (resistors,
capacitances, etc.) that require very precise adjustment depending on the technology. The replacement by digital parts of analogue components (phase comparator, VCO) occurring in DPLL removes the external passive components[7]. Unfortunately, this digital method creates quantification errors which minimize the efficiency of the PLL. In addition, adding phase error to the overall loop delay and induces phase jumps which are greater than the quantification stage on the clock output.

The rest of the article is presented as follows. Section 2 describes the problem statement. Section 3 presents the design proposed DPLL design. Section 4 presents the results of the overall design of DPLL and the discussion of the results. Finally, section 5 presents the conclusion of the proposed design.

2. Problem formulation
In modern IC design, the PLL is frequently employed for the Clock generation for synchronization purposes [8]. The general communication system employing a PLL for the synchronization data bit with clock signal shown in Fig. 1.

![Diagram](image)

Fig. 1 The general communication system employing a PLL for the synchronization data bit with the clock signal shown in [9].

At the transmitting end, the digital data is fed into shift registers. The data is moved serially to the output driver for the transmitter. The receiver section amplifies the data and converts data into digital logic levels, where data which be analogue after going through the communication channel. The next step in this series of events is to transfer the information back to the receiver's shift register and process the data obtained. Lack of a clock signal however makes this difficult. The PLL does the role of producing a locked clock signal, or in sync with the arriving signal. In the receiver, the clock signal produced PPL is employed to clock the shift register and thereby recover the data. This PLL application is sometimes referred to as a circuit of bit synchronization or clock-recovery circuit [10].

3. Design of DPLL
PLLs are generally classified as either analog or digital based on the type of phase detector that is used [2]. Both analog PLL (APLL) and digital PLL (DPLL) consists of the following three basic elements
1. Phase Detector (PD).
2. Low pass filter (LPF)
3. Error amplifier
4. Voltage Controlled Amplifier (VCO).
3.1 Digital type PD(XOR gate): There are two types of phase detectors one is digital type phase detector (XOR gate) and another one is analog type phase detector (Balanced modulator). The simplest phase detector is the XOR gate phase detector which is shown in fig.2.

![Fig. 2 Exclusive-OR phase detector](image)

The output of the XOR gate is high when only one of the input signal \( f_s \) or \( f_o \) is high. This type of detector is used when both input signals are square waves[2]. The input and output waveforms for \( f_s = f_o \) are shown in Fig. 3.

![Fig. 3 Input and output waveforms of the XOR gate.](image)

In Fig. 3, \( f_s \) is leading by \( \Phi \) degrees. The dc output voltage variation concerning phase difference \( \Phi \) is shown in Fig. 4.

![Fig. 4 DC output voltages versus phase difference \( \Phi \) curve [7].](image)
The maximum dc output voltage occurs when $\Phi = \Pi$ and at this condition the output of PD remains high. In fig. 4 the slope curve gives phase detector conversion ratio $K_\Phi$. So, conversion ratio $K_\Phi$ for a supply voltage $V_{cc} = 5v$ is,

$$K_\Phi = \left( \frac{5}{\Pi} \right) = 1.59V \text{ rad}$$  \hspace{1cm} (1)$$

3.2 Low Pass Filter: The simple RC LPF is shown in Fig.5. The LPF is mainly employed to remove high-frequency components and noise. Also, it controls characteristics of the PLL such as bandwidth, lock range, capture range, and transient response. If LPF bandwidth is minimized, the response time is increased. Besides, a decrease in the bandwidth of LPF also minimizes the capture range of PLL. The charge on the LPF capacitor gives short term memory to PLL. Thus, even though for a few cycles the signal is less than the noise, the dc voltage on the compressor tends to change the VCO frequency until it picks up the signal again. This gives more locking stability and noise immunity[11].

![Fig. 5 Low pass filter (a) Active (b) Passive][6]

3.3 Operational amplifier: The first factor to be considered is the requirements to be met in the design. The standard CMOS operational amplifier was selected for a clear understanding of the requirements because it was assumed that such a design could meet the specifications and that the design of such an amplifier is fairly simple[12]. The schematic of the op-amp is shown in Fig. 6. Choose $I_{ds}$ to be as a reference current which will be decided by power dissipation and slew rate.

- Calculate compensation capacitor value $C_c = \frac{I_d}{\text{Slew Rate}}$
- Calculate $g_{m1}$ from gain bandwidth=$g_{m1}/2\pi*C_c$
- Calculate $g_{m5}$ from the condition of stability $g_{m5} = 2.2*g_{m1}$
- Open-loop Gain

$$A_0 = \frac{(g_{m1}g_{m5})}{(g_{ds2} + g_{ds4})(g_{ds5} + g_{ds7})} = \frac{(g_{m1}g_{m5})}{\{I_{D2}(\lambda_2 + \lambda_4)I_{D7}(\lambda_5 + \lambda_7)\}}$$

- The gain-bandwidth product is by the following equation

$$A_0 = \frac{1}{2\lambda^2} \sqrt{\frac{K_NK_pW_5}{I_{DI}I_{D2}L_1L_2}}$$  \hspace{1cm} (2)$$

$$GB = \frac{g_{m1}}{C_c} = \frac{1}{C_c} \sqrt{\frac{2K_NW_1I_{DI}}{L_1}}$$  \hspace{1cm} (3)$$
For matching and symmetry, we choose
\[
\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 \quad \& \quad \left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 \tag{4}
\]
If we force \(V_{gs3}\) to be equal to \(V_{gs5}\) by the following relationship
\[
\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_3 \left(\frac{I_3}{I_4}\right) \tag{5}
\]
But \(I_3=I_4\) & \(I_5=I_6\) and equation \(\rightarrow (3.5)\) may be expressed as
\[
\left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_6 \left(\frac{I_6}{I_8}\right) \tag{6}
\]
\[
\left(\frac{I_7}{I_8}\right) = \left(\frac{W}{L}\right)_7 + \left(\frac{W}{L}\right)_8 \tag{7}
\]
However, because \(I_4=0.5I_7\) and, the condition for \(M4\) to remain in saturation becomes
\[
\left(\frac{W}{L}\right)_4 = \frac{W}{L}_5 \left(\frac{W}{L}_7 \left(\frac{W}{L}_6 \frac{I_7}{I_8}\right)\right) \tag{8}
\]
3.4 Voltage Controlled Oscillator: The typical characteristics of a VCO shown in fig. 7. The frequency \(f_{center}\) when \(V_{in}(=V_{center})\) is VDD/2 (typically) of output square wave of the VCO. The other two frequencies of interest are \(f_{max}\) and \(f_{min}\), with input voltage \(V_{max}\) and \(V_{min}\), respectively. The VCO continues to oscillate without any input data. The VCO is generally constructed to have an equal input data rate and VCO centre frequency. This minimises the time it takes the DPLL to lock.

Fig. 7 Input control voltage vs Output frequency of VCO
The gain of the VCO is the slope of the curve shown in Fig. 7 and it can be represented as:

\[
K_{\text{vco}} = 2\pi \frac{f_{\text{max}} - f_{\text{min}}}{V_{\text{max}} - V_{\text{min}}} \quad \text{(radians/s.V)}
\]  

(9)

The relationship between \( f_{\text{clock}} \) and the VCO input voltage is given by

\[
\omega_{\text{clock}} = 2\pi f_{\text{clock}} = K_{\text{vco}} V_{\text{inVCO}} + \omega_o \quad \text{(radians/s)}
\]  

(10)

where \( \omega_o \) is a constant. The variable given as feedback is not frequency but a phase. The phase of the VCO output is related to \( f_{\text{clock}} \) by

\[
\Phi_{\text{clock}} = \int \omega_{\text{clock}} \cdot dt = \frac{K_{\text{vco}}}{j\omega} V_{\text{inVCO}} \quad \text{(radians)}
\]  

(11)

The current-starved VCO is shown schematically in Fig. 8. The operation current-starved VCO is similar to the ring oscillator. M2 and M3 MOSFETs act as an inverter, whereas M1 and M4 MOSFETs operate as current sources. The current sources, M1 and M4, limit the current available to the inverter, M2, and M3; in other words, the inverter is starved for current. The MOSFETs M5 and M6 are mirrored in each inverter/current source stage[14].

Only one stage of the current-starved VCO shown in Fig. 9 is considered to formulate design equations very simple. The M2 and M3 transistors total drain capacitances are given by:

\[
C_{\text{tot}} = C_{\text{out}} + C_{\text{in}} \left( \frac{C_{\text{ox}}}{C_{\text{ox}} (W_p L_p + W_n L_n)} + \frac{3}{2} C_{\text{ox}} (W_p L_p + W_n L_n) \right)
\]  

(12)

The eq(12) can be rewritten and simplified as more useful form as:

\[
C_{\text{tot}} = \frac{5}{2} C_{\text{ox}} (W_p L_p + W_n L_n)
\]  

(13)
The time taken for charging $C_{tot}$ from zero to $V_{sp}$ with a constant-current $I_{D4}$ is represented as:

$$ t_1 = \frac{V_{sp}}{I_{D4}} C_{tot} \tag{14} $$

and the time taken for discharging $C_{tot}$ from $V_{DD}$ to $V_{sp}$ is represented as:

$$ t_2 = \frac{V_{DD} - V_{sp}}{I_{D1}} C_{tot} \tag{15} $$

If we choose $I_{D4} = I_{D1} = I_D$ ($I_{D_{center}}$ when $V_{in\text{VCO}} = V_{DD}/2$), then the sum charging and discharging time is given as:

$$ t_1 + t_2 = \frac{V_{DD} C_{tot}}{I_D} \tag{16} $$

The oscillation frequency of the current-starved VCO for $N$ (an odd number $\geq 5$) of stage is:

$$ f_{osc} = \frac{1}{(t_1 + t_2).N} = \frac{I_D}{V_{DD} C_{tot} \cdot N} = f_{center} [@V_{in\text{VCO}} = V_{DD}/2 \text{ and } I_D = I_{D_{center}}] \tag{17} $$

Equation (17) represents the center frequency of the current starved VCO when $I_D = I_{D_{center}}$. The VCO stops oscillation, ignoring sub threshold currents, when $V_{THN} > V_{in\text{VCO}}$. Then we can define.

$$ V_{min} = V_{THN} \text{ and } f_{min} = 0 \tag{18} $$

The $f_{max}$ is derived from $I_D$ when $V_{in\text{VCO}} = V_{DD}$. At the maximum frequency then, $V_{max} = V_{DD}$

![Simplified view of a single stage of the current-starved VCO](image)

Fig. 9 Simplified view of a single stage of the current-starved VCO

The average current drawn by the VCO is

$$ I_{avg} = \frac{V_{DD} C_{tot} \cdot N}{T} = V_{DD} C_{tot} \cdot N \cdot f_{osc} \tag{19} $$

or
The average power dissipated by the VCO is
\[
I_{avg} = I_D
\]
(20)
The average power dissipated by the VCO is
\[
P_{avg} = V_{DD} \cdot I_{avg} = V_{DD} \cdot I_D
\]
(21)
If we consider the power dissipated from mirror MOSFETs (M5&M6), the power is doubled form the given by Eq. (2.20) with the assumption of \( I_{DS} = I_{DS} = I_D \).

4. Results and Discussion
The overall design of DPLL is implemented in the TANNER EDA tool. The individual results of each block of DPLL and overall results of DPLL are as follows

4.1 XOR Phase detector: Fig. 10 shows an eight-transistor implementation of the XOR function, using two CMOS Transmission Gates and two CMOS inverters. Tanner has two viewing modes, one is a schematic mode and the other one is symbol mode. The schematic and symbol of the XOR phase detector is shown in Fig. 10

![Fig. 10 (a) XOR PD schematic diagram (b) symbol](image)

Fig. 10 (a) XOR PD schematic diagram (b) symbol

Fig. 11 shows the result of the XOR phase detector, where a,b are input signals and y is the output signal for the XOR phase detector. For different values of phase difference, the error voltages are generated shown in tabular form as illustrated in Table 1.

![Fig. 11 Simulation results of XOR PD](image)
Table 1 Phase difference versus generated error voltage at the output of XOR PD

| Phase difference (Φ) | Error voltage (V) |
|----------------------|-------------------|
| 0                    | 0                 |
| 18                   | 0.5               |
| 36                   | 1                 |
| 54                   | 1.5               |
| 72                   | 2.0               |
| 90                   | 2.5               |
| 108                  | 3                 |
| 126                  | 3.5               |
| 144                  | 4                 |
| 16                   | 4.5               |
| 180                  | 5                 |

With phase-difference (Φ) on X-axis and error voltage on Y-axis, the characteristics are shown in Fig. 12

![Error voltages versus phase difference of XOR PD](image)

Fig. 12 Error voltages versus phase difference of XOR PD

The slope of the above curve indicates, phase angle-to-voltage transfer coefficient (KΦ) or, the conversion ratio of the phase detector.

4.2 LPF: The simple RC LPF is shown in Fig. 13. The LPF is mainly employed to remove high-frequency components and noise. In addition, it also controls characteristics of the PLL such as bandwidth, lock range, capture range, and transient response. If LPF bandwidth is minimized, the response time is increased. In addition, a decrease in the bandwidth of LPF also minimizes the capture range of PLL. The charge on the LPF capacitor gives short term memory to PLL. Thus, even though for a few cycles the signal is less than the noise, the dc voltage on the comparator tends to change the VCO frequency until it picks up the signal again. This gives more locking stability and noise immunity [15].

By taking the above considerations resistor is chosen to 1KΩ and the capacitor to be 10pf. The circuit diagram for LPF is shown in Fig. 4.4.
4.3 Operational Amplifier: The specifications considered for the simulation of the error amplifier is given in Table 2.

| Name               | Specification |
|--------------------|---------------|
| Gain (Ao)          | 100 dB        |
| Gain Bandwidth     | 300 MHz       |
| Slew rate          | 1V/µs         |
| Choosing $I_{D1}$  | 10µA          |

Using Eq (4) to Eq (8). The MOSFET transistors sizes are computed and simulated using 0.18µm technology.

- $I_{DS}=100$µA
- $C_{C}=0.55$PF
- $(W/L)_{1,2} = 4$
- $(W/L)_{5} = 15$
- $(W/L)_{3,4} = 1.5$
- $(W/L)_{6} = 1$
- $(W/L)_{7,8} = 0.2$

By using these W/L ratios, the op-amp implemented on S-Edit is shown in Fig.14. After simulating the S-Edit spice with one of the inputs connected to the ground, W-Edit displays the result shown in Fig.15.

![Fig.13 Simple RC LPF](image)

![Fig.14 Op-amp circuit implemented on S-Edit.](image)
Fig.15 Simulation results of the two-stage op-amp.

For stability criterion of the op-amp circuit, it has to maintain around 90deg phase margin, by verifying for different values of capacitance, it has been found that the above circuit maintains a phase margin of 85° for C=.55pf. The op-amp open-loop gain is 82db with a unity gain frequency of 300MHz.

The op-amp circuit instance is called for the design of a non-inverting amplifier and two external resistors are added as feedback resistance (Rf) and input resistance (R1). The circuit for the non-inverting amplifier in S-Edit is shown in Fig. 16.

The gain of the non-inverting amplifier given as, (A) = 1+ (Rf/R1), where Rf is feedback resistance and R1 is the input resistance for the op-amp.

Fig.16 Non-inverting amplifier.

For S-Edit operations, it is required to maintain the gain of 1.8. Input resistance for the op-amp must be large as possible, but in layout maximum resistance takes much area to implement. so it is a trade-off between maximum resistance and area. That’s why input resistance is chosen as 1MΩ. To maintain the gain criterion feedback resistance should have to maintain the resistance of 0.8Meg Ω. The result of the non-inverting amplifier is shown in Fig. 17. The input signal amplitude is 1.0V and this sinusoidal input is amplified to 1.8V by the non-inverting amplifier.
Fig. 17 Simulation results of the non-inverting amplifier.

4.4 Voltage Control Oscillator: Circuit implemented on S-Edit shown in Fig. 4.11. While designing the current-starved VCO first calculate $C_{\text{tot}}$. Using Eq. (2.12) and MOSFET inverters a resized for equal drive, i.e., $L_n = L_p = 0.2 \, \mu m$, $W_n = 0.3 \, \mu m$, and $W_p = 0.9 \, \mu m$, the capacitance is

$$C_{\text{tot}} = \frac{5}{2} \cdot \frac{aF}{\mu m^2} \cdot (0.2 + 3 \cdot 2) \, \mu m^2 = 5 \, fF$$

Here the oscillator having a minimum number of stages, that is, 5, the center drain current using Eq. (2.16), is given by

$$I_{\text{Dcenter}} = 100 \, \text{MHz} \cdot 5 \cdot 5 \, fF \cdot 5\, V = 12.5 \, \mu A.$$

To determine the size of M5 and M1 of Fig. 2.12 we solve for $W/L$ in

$$I_{\text{Dcenter}} = \beta_5 \cdot (V_{GS} - V_{THN})^2 = \frac{50 \, \mu A}{5 \, V^2} \cdot \frac{W_n}{L_n} \cdot (2.5 - 0.83)^2 = 12.5 \, \mu A$$

Giving $W_n/L_n = 1.72$. We will use $W_n = 0.5 \, \mu m$ and $L_n = 0.3 \, \mu m$ as a close approximation. We use these values to set the size of M5 and M1 (of each stage). Sizing p-channel we require, $\beta_6 = \beta_5$; this causes M5 to go into the triode region when $V_{\text{inVCO}}$ is approximately 3 and above. This requirement sets the size of M6 M4 at $W_p = 1.5 \, \mu m$ and $L_p = 0.3 \, \mu m$. The circuit implemented on S-Edit is shown in Fig. 18.

Fig. 18 Current-starved VCO
When dc control voltage to VCO is 2.5V it will produce oscillations with a frequency of 122Meg Hz as shown in Fig. 19.

For this oscillator oscillations will start for dc control voltage of 2.5V. Similarly, for different values of control voltage, the generated frequencies are shown in Table 3.

The minimum control voltage generated for VCO is 1.1V, similarly, the maximum control voltage generated for VCO is 2.1V. But the generated frequency for minimum control voltage is 42.9MHz and the generated frequency for maximum control voltage is 118.4MHz. Then the voltage to frequency conversion factor \( K_v \) of VCO is given by

\[
K_v = \frac{\Delta f_o}{\Delta V_c}
\]

Where \( \Delta V_c \) is the modulation voltage needed to generate a frequency shift \( \Delta f_o \).

Hence,

\[
K_v = \frac{116.2 - 74.6}{2.3 - 1.3} \frac{MHz}{V} = 41.6 \frac{MHz}{V}
\]

![Fig.19 Simulation results for VCO](image)

| Control Voltage (V) | Generated Frequency (MHz) |
|---------------------|---------------------------|
| 0.6                 | 35.4                      |
| 0.7                 | 87.0                      |
| 0.8                 | 119.6                     |
| 0.9                 | 152.3                     |
| 1.0                 | 175                       |
| 1.1                 | 42.9                      |
| 1.2                 | 55.6                      |
| 1.3                 | 68.5                      |
| 1.4                 | 79.4                      |
| 1.5                 | 89.2                      |
| 1.6                 | 96.7                      |
| 1.7                 | 103.1                     |
| 1.8                 | 108.1                     |
| 1.9                 | 112.4                     |
| 2.0                 | 115.6                     |
| 2.1                 | 118.4                     |
| 2.2                 | 120.4                     |
| 2.3                 | 121.8                     |
| 2.4                 | 123                       |
| 2.5                 | 124                       |
4.5 Overall design of DPLL: By calling the instance of each block in S-Edit, the overall PLL is designed. The inter connection between blocks is shown in Fig. 20.

![Overall design of DPLL](image)

Here $V_{out}$ is the response of PLL. Input signal (a) frequency is 116 MHz which is in the lock-in range, so PLL locks the input signal after 60nS as shown in Fig. 21.

For every input signal frequency to overall PLL generates a known frequency. This frequency is the free-running frequency for PLL. For the above design free-running frequency ($f_0$) is around 95.4MHz.

Input signal ($V_{in}$) frequency increased from zero frequency to higher values at some frequency the input signal is locked by one for one cycle. This gives the starting point of the lock-in range. Similarly, the input signal ($V_{in}$) frequency decreased from a very high value at some frequency again locks with the input signal. This gives the highest point for the lock-in range. The difference between maximum and minimum values is the lock-in range.

![Simulation results of overall PLL](image)
For the above S-Edit design, when the input signal is a square wave with a time period 13.4nsec, PLL starts locking the input signal. Thus the starting point of lock-in range
\[ f_1 = \frac{1}{13.4\text{nsec}} = 74.6\text{MHz} \]

Similarly, when the input signal period is 8.6nsec, PLL again locks. Thus higher point of lock-in range is,
\[ f_2 = \frac{1}{8.6\text{nsec}} = 116.2\text{MHz} \]

Hence, the lock-in range is
\[ 2\Delta f_c = (116.2-74.6)\text{MHz} = 41.6\text{MHz} \]

The relation between capture and lock-in range for the proposed design is shown in fig.22. The results summary is illustrated in Table 4.

| Parameter                  | Value  |
|----------------------------|--------|
| Capture range (2\Delta f_C)| 24.4MHz|
| Lock-in Range (2\Delta f_L)| 41.6MHz|
| Pull-in time               | 60nS   |
| Power consumption          | 250\mu W|
| RMS jitter                 | 250ps  |

Fig. 22 Relation between capture and lock-in range

5. Conclusion

The single-chip continuous tracking CMOS is DPLL implemented using 0.18\mu m technology. For a simpler design, the XOR gate is used as a phase detector and for better tracking, a two-stage amplifier and the current-starved VCO is used. The proposed DPLL operates within the range of 74.6MHz to 116MHz. The lock-in the range is 41.6MHz and capture the range of 24.4MHz with an RMS jitter of 250ps. The pull-in time of the design is 60ns and power consumption is about 250\mu W when the DPLL is running at 9MHz.

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