Alternative Spin-On-Glass (SoG) material characterization
For Deep-Submicron (<0.35 um) soft reflow fabrication process

F Packeer¹, M A M Zawawi¹, N Z I Hashim¹, N M Noh¹, W M Jubadi², and M Missous³

¹School of Electrical and Electronic Engineering, Engineering Campus, Universiti Sains Malaysia, 14300 Nibong Tebal, Pulau Pinang, Malaysia
²Department of Electronics, Faculty of Electrical and Electronic Engineering, University Tun Hussein Onn Malaysia, Parit Raja, 86400 Batu Pahat, Johor, Malaysia
³School of Electrical and Electronic Engineering, University of Manchester, Sackville Street, Manchester, M13 9PL, United Kingdom

E-mail: fauzi.packeer@usm.my

Abstract. Currently a submicron soft reflow process developed in University of Manchester uses silicon nitride (Si₃N₄) as the hard mask layer to support the T-Gate structure of pHEMTs in order to make it mechanically stable. However, an alternative material known as Spin-on-Glass (SoG) is introduced to replace Si₃N₄, offering shorter processing time and consequently, a much simpler and more cost-effective alternative to the e-beam lithography of nanometre-scale gate length transistors. The SoG deposition through plasma-enhanced chemical vapour deposition process requires only 30 minutes to complete, as opposed to the one-day process of depositing Si₃N₄. In this study, the SoG material used is Silicafilm, and the minimum deposition thickness achieved is 138 nm, enabling 150-nm gate length devices to be fabricated. The SoG is also successfully etched at very low power (20 W) and very low pressure (< 50 mTorr) respectively, eliminating the detrimental effect of high power plasma etching to the 2DEG carriers. In addition to that, no film cracks observed even by using a single coating and a single baking temperature of 200 °C. All these results indicate the potential of SoG as a suitable hard mask layer alternative to the silicon nitride for the use soft reflow fabrication process.

1. Overview

Currently a submicron soft reflow process developed in University of Manchester uses Silicon Nitride (Si₃N₄) as the hard mask layer to support the T-Gate structure of pHEMTs in order to make it mechanically stable [1]. However development and characterization of alternative material know as Spin-on-Glass (SoG) is being performed to replace silicon nitride (Si₃N₄) as the hard mask layer giving altogether a truly simple and cost effective alternative to e-beam lithography of nanometre scale gate length transistors [2-4] (refer figure 1a and 1b).

In this study, the minimum thickness that could be achieve with Silicafilm is 138 nm enabling ~ 150 nm gate length devices to be fabricated. The challenging issue of SoG is the etching whereby the required high power (>100 W) plasma etching is detrimental to the 2DEG carriers. Here we demonstrate that the SoG is etchable at very low power (20 W) and very low pressure (< 50 mTorr). Furthermore, most literature [5, 6] use multiple coating and ramping for the baking temperature
roughly from 80 °C to 230 °C to avoid film cracks but in this study only single coating and single baking temperature (200 °C) applied, with no cracks observed. This simplified the process even further.

Figure 1. Silicon Nitride (Si$_3$N$_4$) (a & c) and Spin-on-Glass (SoG) (b & d) hard mask deposition with its respective equipment.

2. Introduction of SoG
The motivation thus to evaluate SoG material has been of interest to replace Silicon Nitride (Si$_3$N$_4$) deposition through Plasma-enhanced Chemical Vapour Deposition (PECVD) by a much simpler and shorter processing time, that is from almost a one day task to only 30 minutes (refer figure 1c and 1d). Basically the technique draws from the planarizing nature of a liquid when applied to a surface topography. The focus is to make the material as close to Silicon Dioxide (SiO$_2$) as possible. The dielectric and optical characteristics of SoG are quite similar to the characteristics of pure SiO$_2$ formed by the oxidation of silicon at high temperature.

The SoG material used in this study (Silicafilm) [7], is an alcohol solution which is applied to a semiconductor surface to yield a pure SiO$_2$ film. Such film may be formed on a wide variety of flat surfaces by spinning, spraying or dipping. However, for precise control of flatness and greatest uniformity, it is performed using spinning methods (refer figure 1d).

3. SoG deposition
Coated sample is spun at the desired speed for thickness of choice for 30 s. During this time, the liquid film will spread uniformly on the entire sample and the solvents in the liquid will eventually evaporate, leaving a thin film of solid component [8] on the sample. Finally, baking the sample on hot plate at
200 °C for 15 minutes will turn the thin film of solid component to SoG (refer figure 2). Some studies [5, 6] use sequences of hot plate bakes from low to high temperature, with one minute baking for each temperature, then high temperature (> 350 °C) curing in an oven with Nitrogen flow. This to avoid flakes.

Figure 2. Silicafilm SoG surface profile before and after soft bake.

4. SoG thickness check

Figure 3. Lift-off process to determine Silicafilm SoG thickness and its measurement at spin-speed 3000 rpm and spin time 30 s.
Figure 4. Silicafilm SoG spin-speed curve: in-house data vs. supplier data under same soft-bake conditions (a) and Silicafilm SoG colours at different thickness with respect to spin speed (b).

The thickness check is done using a liftoff process (refer figure 3a). SoG thickness measurement is then performed using a DEKTAK 3 ST surface profiler. The measurement look rough but it is within +/- 5% variation from the centre value as shown in figure 3b. This liftoff process concept is unique, repeatable and gives a high degree of confidence in the measurement results and much simpler compare to plasma etching.

Figure 4a shows that the thickness of the SoG film will shrink if the spin-speed increases. The thinnest SoG film is at maximum speed i.e. 8000 rpm while the thicker film is at the slowest speed of 1500 rpm. The red curve is the data from the supplier where the minimum spin-speed is 3000 rpm while the maximum spin-speed is at 10000 rpm. The colour of the SoG film is also different from one thickness to another as shown in figure 4b. These colours represent variations in thickness as the light refracts.

5. Pin holes verification

Figure 5. Lift-off process to fabricate MIM capacitor using Silicafilm SoG as dielectric for pin holes verification.

The quality of a thin film is sometimes affected by the defect on the film surface or pinholes, which have potential for causing reliability problem and shorts. Visual inspection shows no pinholes but investigated further by fabricating Metal-Insulator-Metal (MIM) capacitor (figure 5). The concept is, if the thin film which is the dielectric or insulator of the capacitor has pinholes then it will short. Testing
for continuity basically means testing to see if there is an electric connection between two points. If two points are electrically connected they are said to be continuous or shorted. In this case it means, if the SoG has pinholes, it will allow metal 2 to be in contact with metal 1 below. Hence, 100% continuity check on the capacitors give 100% yield on no short, which means the 216 nm and 138 nm SoG are reliable and suitable to be an alternative hard mask layer for submicron reflow process.

6. SoG etch study
In this study, the etching is done using the Reactive Ion Etching (RIE) plasma chamber. The etching parameters are to be as close as possible to those used to etch Si₃N₄ as previously mentioned i.e. low RF power and low pressure. Low RF power need to be maintained to avoid degradation of the 2DEG later on when making a device and low pressure can minimize loading effect. The etching time must also be reasonably short as longer ones will erode the S1805 resist which is just 500 nm in thickness. All of this restrictions are basically a challenge to etch SoG as reported in most literature [9, 10], to etch SiO₂ or SoG, the minimum RF power used is 100 Watt and the resist thickness is usually more than 2 μm. Figure 6a and 6b show the etch rate and selectivity respectively. While figure 6c illustrate the etch rate on patterned sample.

7. Soft reflow on SoG
The main motivation for the use of SoG is to have alternatives for hard mask layer for the submicron soft reflow study. This SoG coating process is simpler and less time consuming as mentioned previously compared to the Si₃N₄ deposition process. Hence, with the success in the etch rate studies using thicker resists, the study of 138 nm SoG was continued for soft reflow. The trial runs used thick S1805 (with 20 minutes EBR) on patterned samples.

The results for the 90 s soft reflow run are shown in figure 7 on thicker S1805 (with 20 minutes EBR). Base on the result shown figure 7, the soft reflow works on the 138 nm SoG as hard mask layer. The initial 1 μm features shrink after 90 s reflow at a solvent temperature less than 50 °C. Further optimization on soft reflow conditions and etching could enable gate length ~ 150 nm.

Figure 6. Silicafilm SoG etch rate (a), selectivity (b) and Silicafilm SoG on device pattern after etch & clean (c).
8. Conclusions
The possibility of using Spin-on-Glass (SoG) material as an alternative to Silicon Nitride ($\text{Si}_3\text{N}_4$) hard mask deposition was explored. The motivation for this study is that the SoG process is much simpler than the $\text{Si}_3\text{N}_4$ one and save a lot of processing time. However, the key challenge of this SoG is etching as it needs high power (>100 W). In order to maintain low power (20 W) to avoid degrading the device 2DEG, etch studies were performed and a successful recipe to etch SoG of thickness 216 nm and 138 nm was developed. The developed etching recipe however has low selectivity to resist and attacks the resist around the reflowed area. The future works would be further optimizing the current process of soft-reflow on SoG to realize smaller gate length down to 150 nm, these include using thinner SoG material and using more aggressive etching gas such as Sulfur Hexafluoride ($\text{SF}_6$) or Buffered Oxide Etch (BOE).

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10. References
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