Leaving Your Things Unattended is No Joke!
Memory Bus Snooping and Open Debug Interface Exploits

Yang Su and Damith C. Ranasinghe
Auto-ID lab, School of Computer Science, The University of Adelaide, Australia
{yang.su01; damith.ranasinghe}@adelaide.edu.au

Abstract—Internet of Things devices are widely adopted by the general population. People today are more connected than ever before. The widespread use and low-cost driven construction of these devices in a competitive marketplace render Internet-connected devices an easier and attractive target for malicious actors. This paper demonstrates non-invasive physical attacks against IoT devices in two case studies in a tutorial style format. The study focuses on demonstrating the: i) exploitation of debug interfaces, often left open after manufacture; and ii) the exploitation of exposed memory buses. We illustrate a person could commit such attacks with entry-level knowledge, inexpensive equipment, and limited time (in 8 to 25 minutes).

I. INTRODUCTION

A considerable amount of IoT devices have been adopted by consumers and industries over the last decades; the strong growth momentum is set to continue. In 2020, the number of Internet-connected smart devices reached 11.7 billion and is expected to increase by more than five-fold by 2025 [1]. Apart from the popular consumer electronics, health care, and manufacturing, the automotive industry is the next promising market, followed by retail, logistics, agriculture, and animal husbandry sectors [16]. Despite the rapid growth, there are still many challenges related to security, especially for devices involved personal and sensitive data. By 2025, the amount of data gathered by those devices are expected to reach 73.1 zettabytes [1]. The widespread existence and access to sensitive data render Internet-connected devices a lucrative attack target for malicious actors [13].

Despite user privacy concerns, it is difficult to choose products with adequate protections without an in-depth knowledge on security and privacy [2]. Meanwhile, manufacturers have generally focused on reducing time-to-market delays [12], improving cost-effectiveness and quality of service [9] but skipping over some necessary security measures [4].

Our Focus and Contributions. This paper will focus on investigating the vulnerabilities arising from common debug interfaces left open and exposed memory buses in IoT (Internet of Things) devices. Notably, unlike software that can be patched, we focus on exploiting vulnerabilities related to the hardware design that are difficult to be fixed after products are released to the market. To demonstrate the ease with which snooping\(^1\) on exposed memory buses and exploiting open debug interfaces can be, we apply techniques that are simple in practice, only require inexpensive gadgets, and do not impose irrecoverable or noticeable damage to the device. In particular, in this article, we:

- Investigate the practical threat posed by: i) debug interfaces left open; and ii) exposed buses to off-chip memory commonly used for storing data and secrets in COTS (commercial off-the-shelf) devices.
- Demonstrate the relatively low cost and the level of skills required to extract sensitive data from devices.
- Conduct and describe two case studies, in the style of a tutorial, to demonstrate the realistic threat by extracting executable code and secrets from COTS electronic devices. A demonstration video of gaining remote access to a portable Internet connected camera after an exploit is available at https://youtu.be/fInl9QugrXI.

Organisation. The rest of the paper is organized as follows. In Section II, we summarize previous work and useful resources related to physical attacks on IoT devices. Section III presents the threat model. Exploitable debug interfaces and memory buses are discussed in Section IV followed by two case studies using popular IoT devices. Section VII provides concluding remarks.

II. BACKGROUND

Software attacks. Attacks against software exploit security vulnerabilities of the communication protocols, cryptographic algorithms, or software implementation of the product [21], [6], [20]. Software attacks are possible without physical access to the victim device. However, the manufacturer could easily fix the software vulnerabilities through system updates [18], [22]. In this paper, we would like to focus on exploiting vulnerabilities related to the hardware design that are difficult to be fixed after products are released to the market.

Invasive physical attacks. These attacks require direct access, for example, dissect a smart card and the use of microprobes to read the secure storage of cryptographic keys [26] from its internal components [21], [10]. We consider methods that obviate invasive attacks since it generally requires expensive equipment (e.g., a US$5,000+ microprobe workstation) and, inevitably, leaves traces of tampering with the device [19].

\(^1\)Snooping: unauthorized access, similar to eavesdropping but not limited to data collection during transmissions.
Non-invasive physical attacks. Vasile et al. [24] summarized three major firmware extraction techniques: i) Debug interfaces; ii) Raw Flash Dump; and Software Methods. The author also examined 24 popular COTS smart devices in 2018, and 100% of them are vulnerable to at least one of the techniques, followed by three case studies. This work also proposed countermeasures for each of the exploits. Although the study is inspiring and covers a wide spread of target devices, the focus of the study was the techniques to dump the firmware from the devices—leading to intellectual property theft. However, exploitation or what useful information the dumped firmware could provide, time and monetary cost of an attack or a practical adversary model extracting the firmware and the consequence of having access to that firmware was unclear. Krishnan and Schaumont, in [14] investigated exploiting the JTAG (Joint Test Action Group) interface in an intermittent computing system. They demonstrated the extraction of the AES (Advanced Encryption Standard) secret key from the device [5], [18].

III. THREAT MODEL

We build our threat model on the basic assumption that without technical knowledge, ordinary users would not treat IoT devices without obvious mark of tampering as malicious and warrant further investigation. The attacker’s goal is to extract sensitive information from the IoT device hardware, including but not restricted to the user’s personal information, usage data, device configuration and executable code.

A. Victim Devices

We classify the victim IoT devices into: i) **Class-I**: The device implements debugging or programming interfaces, and such interfaces were left open in the final product; and ii) **Class-II**: The devices store sensitive data in off-chip NVM (non-volatile memory). However, in their adversary model, an active attacker has unrestricted physical access and can corrupt and modify the target device’s memory content.

B. Attacker Capabilities

- Has physical procession to the victim device for a restricted time window—a few minutes to half an hour—such a short time generally does not attract the device owner’s attention. Notably, this setting renders it impractical for physical attacks that require a longer time [10] for specialized laboratory setups and data collection.
- Has a basic understanding of electronics, computer security, knows how do debug interfaces and serial buses function. It is important to highlight that it is easy to acquire the simple knowledge needed from materials freely available online, such as [3] and [8].
- Has access to inexpensive tools as exemplified in Section III-C and a computer with open-source decryption and binary file analysis programs.

Our attacker capabilities are reasoned based on [14], with following changes to consider more generic threats: 1) the duration of attacker’s physical access is restricted; 2) an attack does not leave visible traces (e.g., modify the configuration or data) to avoid drawing a user’s attention; 3) we obviated attacks that requires expert knowledge or expensive equipment.

C. Resources and Costs

We assume an attacker has access to the tools listed in Appendix B to facilitate memory bus snooping and open debug interface exploits. The reference prices were obtained from www.ebay.com. For the attacks we explore, the total cost of a memory bus exploit attack is US$15, and the cost of an open JTAG interface exploit attack is US$45. We can observe that an attack under this threat model is inexpensive, and tools can be easily acquired to facilitate memory bus snooping and open debug interface exploits. Notably, an attack under the settings does not leave irreversible or visible damage to the device [19] or attempt to modify firmware (as that could permanently brick the device [5], [18]).

IV. EXPLOITABLE DEBUG INTERFACES AND EXPOSED MEMORY BUSES

This section will introduce exploitable debug interfaces and memory buses in COTS IoT devices and demonstrate how we can easily identify these interfaces for exploitation.

A. Open Debug Interfaces

JTAG is a commonly used debug interface for embedded systems. We may find one or two rows of jumper pins with a printed JTAG, JT_x or Jx label, where x might be a number as in Fig. 1 (a). Occasionally, we can also find individual pins labelled with TDI, TDO, TMS or TCK as seen in Fig. 1 (b). In some products, JTAG headers are there without any label—Fig. 1 (c)—or even hidden from sight as seen in Fig. 1 (d).

![Fig. 1. JTAG debug interface found in IoT devices: (a) labeled with JTAG silk print; (b) labeled with JTAG pin-outs (e.g., TDI, TDO, TMS or TCK); (c) one or two row of test points nearby the MCU; and (d) hidden JTAG.](image)

| Signal name | Direction | Description |
|-------------|-----------|-------------|
| TRST_N      | Programmer → Device | JTAG reset (active low) |
| TDI         | Programmer → Device | JTAG scan-chain input |
| TDO         | Programmer ↔ Device | JTAG scan-chain output |
| TMS         | Programmer → Device | JTAG mode selection |
| TCK         | Programmer → Device | JTAG clock |
| GND         | Programmer ↔ Device | Common ground |

To use the basic functionality of the JTAG debug interface, the five signals shown in Table I need to be wired up correctly.
to a JTAG Debugger—see Fig. 5. There are no concrete definitions of the pin-out order for the JTAG header. A manufacturer can place the JTAG pins in any order. To determine the JTAG pin-definition, we can use the manual inspection method in Section V or use the open-source JTAGenum described in Appendix B.

Other than JTAG, manufacturers may implement different debug interfaces, such as ARM SWD (Serial Wire Debug in Fig. 2 (a)) and TI SWB (Spy-Bi-Wire in Fig. 2 (b)). IoT device manufacturers can also implement a proprietary two-wire debug interface (e.g., the that found in a TP-Link WiFi access point Fig. 2 (c). The two-wire programming interfaces typically consist of one bi-directional data wire and one clock wire, sometimes including GND (ground) and Vcc (common collector voltage) for potential reference and power supply. Two-wire debug interfaces benefit from the reduced pin design and are suitable for IoT devices with small form factors.

B. Exposed Memory Buses

Since the on-chip NVM is limited and expensive [15], many IoT devices use off-chip Flash or EEPROM (electrically erasable programmable read-only memory) to store firmware images, settings, and secrets.

Fig. 3 lists a number of off-chip memory in IoT devices. EEPROM in SOT12-5 package in Fig. 3 (a) often appears in tiny devices, such as a smartwatch, due to its small footprint. Flash or EEPROM chips in the SOP-8 package are common off-chip storage in many IoT devices; such memory communicates with the microcontroller via a serial bus such as I2C (Inter-Integrated Circuit) and SPI (Serial Peripheral Interface), as exemplified in Fig. 3 (b). IoT devices requiring relatively higher storage space and faster access speeds may employ Flash chips with parallel buses, such as those shown in Fig. 3 (c) and (d)—parallel buses employ more wires to transfer data and address signals. We focus on memory chips using serial buses, as parallel buses are generally difficult to access and require professional and costly equipment. In addition, memory chips with parallel buses can use a BGA (ball grid array) package where all signal pins are hidden behind the package; therefore, it is more difficult to access [24].

V. OPEN JTAG INTERFACE EXPLOIT CASE STUDY

Post identification of interfaces for possible access, this section investigates the potential threat posed by demonstrating the extraction of memory contents in IoT devices in two example case studies under the practical threat model we consider in Section III.

Scenario. Consider the following scenario for our first case study: Elizabeth is an 87-year-old widow, she lives alone in an apartment equipped with an electronic lock. One day the electronic lock runs out of battery. Elizabeth asked one of her neighbors to replace the battery for the lock. However, the battery in the lock is an unusual model. The neighbor suggests bringing the lock to the hardware store to match the correct battery model. Half an hour later, the neighbor returned with the battery and re-installs the electronic lock for Elizabeth. Could the neighbor extract the key code for the electronic lock within the 30-minute time window to gain unauthorized access to Elizabeth’s house?

Attack. We use a Schlage electronic lock FE575 as an example. The tear-down of the electronic lock is summarized in Appendix Fig. 8. The mainboard of the Schlage electronic lock FE575 is shown in Fig. 4. Its circuit layout is uncomplicated. The black square in the middle is a buzzer. It makes a sound when the keyboard is pressed. At the left bottom corner of the buzzer is an MSP430G2433 microcontroller—the electronic lock’s brain. Other components are mostly responsible for powering, motor operation—the circuit needs to drive a DC motor to release the lock when a correct password is pressed. More importantly, there are seven pins in a row labeled with JT1, which is highly like a JTAG interface.

Unfortunately, the pin definitions for JT1 are not labeled on the PCB; hence a strategy is needed to identify the correct order of JTAG signals. Fortunately, as seen in Fig. 4, the MSP430G2433 microcontroller is in an SOP-28 package, all pins are easily accessible. Hence a US$10 multimeter is adequate to identify pin definitions of JT1 without using professional tools such as the US$200 JTAGulator.

Our technique to find correct JTAG pins is to use the diode and continuity mode of a multimeter. The diode and continuity mode is commonly labeled with a diode and a sound wave symbol (e.g., ). This mode measures the forward bias of a diode (if there is one between the two probes of the multimeter). If there is a direct wire connection (or short circuit), the multimeter buzzer will sound. Depending on the multimeter manufacturer, different probe polarities in diode test mode may be used. For our model Stanley STHT77364, the red probe is connected to the cathode, and the black probe is connected to the anode of the tested diode (although, typically, red is the anode and black is the cathode, refer to the multimeter model used for probe polarities). We will start with selecting for the GND, which can be easily accessed at: i) The negative terminal of the battery; ii) any EMI (Electromagnetic interference) shielding used; iii) any pin connected to the

---

Fig. 2. Two-wire debug interfaces found in IoT devices: (a) ARM SWD debug interface; (b) TI SWB debug interface; and (c) manufacturer defined proprietary two-wire debug interface.

Fig. 3. Different NVM chips in IoT devices: (a) EEPROM in SOT23-5 package; (b) Flash in SOP-8 package; (c) Flash in TSOP-56 package and (d) Flash in eMMC-153b package.
ground copper pour; iv) metal case of connectors, such as USB; v) the GND or Vss pin of a known IC.

Plug the probes into the correct receptacle of the multimeter, select the diode and continuity mode. Attach the red meter, select the diode and continuity mode. Attach the red probe to each of the five highlighted microcontroller leads, and measure the V in Fig. 4. Now attach the multimeter’s black probe to each of the seven pins in JT1. As summarized in Table II under the column GND, the 5th pin of the JT1 has a forward-biased voltage drop $V_F = 0$, which implies the JT1.5 is the GND pin in this JTAG connector.

Other JTAG signals can be determined using a similar method. By looking up the datasheet of the MSP430G2433 microcontroller, we have highlighted the six JTAG signal pins in Fig. 4. Now attach the multimeter’s black probe to each of the five highlighted microcontroller leads, and measure the $V_F$ between them and each JT1 pin. The results are summarized in Table II.

**TABLE II**  THE FORWARD-BIASED VOLTAGE DROP (IN mV) MEASURED BETWEEN EACH JTAG SIGNAL AND JT1 PINS. HERE, OL STANDS FOR OPEN LOOP.

|       | GND | TRST_N | TDI | TDO | TMS | TCK | TEST |
|-------|-----|--------|-----|-----|-----|-----|------|
| JT1.1 | 687 | OL     | OL  | OL  | OL  | OL  | OL   |
| JT1.2 | 714 | OL     | OL  | 0   | 0   | OL  | OL   |
| JT1.3 | 711 | OL     | 0   | OL  | OL  | OL  | OL   |
| JT1.4 | 714 | OL     | OL  | 0   | OL  | OL  | OL   |
| JT1.5 | 0   | 715    | OL  | OL  | 478 | 450 | 430  |
| JT1.6 | 716 | 0      | OL  | OL  | OL  | OL  | OL   |
| JT1.7 | 523 | OL     | OL  | OL  | OL  | OL  | 0    |

**TABLE III**  THE ESTIMATED JT1 PINS DEFINITIONS.

| TCK | TMS | TDI | TDO | GND | TRST_N | TEST |
|-----|-----|-----|-----|-----|--------|------|
| JT1.1 | JT1.2 | JT1.3 | JT1.4 | JT1.5 | JT1.6 | JT1.7 |

Based on the results in Table II, we can conclude that JT1.1 is the TCK signal, as there is a direct wire connection between the two points. Similarly, JT1.2 is TMS; JT1.3 is TDI; JT1.4 is TDO; JT1.5 is GND and JT1.6 is TRST_N. The JT1.7 is directly connected to the 25th pin of the MSP430G2433. According to the datasheet, this is the TEST pin connected to the internal device protection fuse. The product manufacturer should blow the internal fuse by applying a 6 V, 100 mA current to prevent further JTAG access. In addition, Vcc is absent in JT1; in this case, the board is powered from a battery while debugging instead of the JTAG debugger. The estimated JT1 pin definitions are summarized in Table III.

Next, we use a TI MSP430 JTAG debugger (or a lower cost, compatible model from a third party) and connect to the pins identified above. We opted to solder a connector to the PCB and use jumper wires to connect to the JTAG debugger as shown in Fig. 5. Soldering is not compulsory, a data repair tool (typically costing US$20) can be used instead.

To access the internal memory contents, we used Texas Instrument’s UniFlash software available at: https://www.ti.com/tool/download/UNIFLASH. If a suitable JTAG debugger is selected to match the target system, the connections are correct, and the JTAG fuse was not blown by the manufacturer, UniFlash will automatically detect the chip model. As shown in Fig. 6 (a) the memory content read out from information memory (0x1000-0x10FF according to [11]), contains the lock’s programming code, and user codes. All stored in plaintext. Those codes match that printed on the user’s manual of the electronic lock and should be kept secret. Even if the user has changed the default codes, an adversary...
can still extract the new value from the same address. With the user code, one can gain entry without letting the homeowner know. This raises important questions regarding the security of such devices to insider attacks, and in a more practical setting, leaving the house unattended and in the company of individuals with lower degrees of trust—e.g. short term rental settings. Simple mitigation would be to change the default programming code and blow the fuse by putting a 6 V by 100 mA current to the TEST pin of JT1 to prevent further JTAG access.

VI. MEMORY BUS SNOOPING CASE STUDY

In the second case study, we consider the following.

Scenario. Emiko is an international student who lives in a shared house with a few housemates. She bought a WiFi IP camera to monitor her room when she was out. One day, her suburb experienced power outages, and Emiko decided to stay at the University until power was restored. We demonstrate the risk of a malicious actor, under our treat model, sneaking into Emiko’s room (when the camera will not raise any potential alarms, given the power outage) and access the WiFi IP camera to gain control and potentially facilitate peeping whilst leaving no visible marks of tampering and a fully operational device.

Attack. We employed a TP-link Tapo C100 IP camera as shown in Fig. 9 (a) to illustrate an attack that exploits an exposed memory bus. The casing of the camera is held together by snap-fit joints; we could disassemble it with a simple lever without leaving irrecoverable damage as shown in Fig. 9 (b). Most of the important logic components are located at the backside of the mainboard, as shown in Fig. 9 (c). The brain of the IP camera is the Realtek SoC (System-on-chip) RTS3903. Unfortunately, its datasheet is not publicly available. Besides the RTS3903, there is an 8 MiB SPI Flash chip XM25QH64C. In this case study, we target extracting information stored in this Flash chip. The XM25QH64C Flash chip is in an SOP-8 package. All its pins are exposed, pin definitions, reproduced from [25], are shown in Fig. 9 (d). As we demonstrate, we can easily use low-cost tools to access the exposed memory bus.

To snoop on the Flash memory chip, the easiest way is to use a US$10 CH341A programmer with a test clip as shown in Fig. 7. The programmer will power the Flash chip and override the SPI bus to send access commands, even when the camera is powered off. The memory contents can be dumped out using freely available software.

The IP camera we studied has the Flash chip and the Realtek SoC powered from the same power rail. When the test clip powers the Flash chip, the Realtek SoC will also start up and attempt to access the Flash chip. This will interfere with our memory readout. The easiest way to prevent the interference is to keep the Realtek SoC in a reset state. We spotted four unpopulated connectors near the SoC by inspecting the IP camera circuit board. Using the multimeter, we can conclude pin 1 and pin 4 are GND and 3.3 V Vcc, respectively. Pin 3 is pulled up to 3.3 V via a 4.7 KΩ resistor. We suspect it is either the reset pin or the TCLK signal of the cJTAG (Compact JTAG designed by MISP company) debugging interface. By trying to short pin 3 and pin 1, we observed the IP camera is reset, so we can conclude that pin 3 is the reset pin of the Realtek SoC. During the entire readout process, we need to short the reset pin, and the GND pin with tweezers to keep the SoC inoperative, as illustrated in Fig. 7 (b).

At this point, the binary image is dumped from the Flash chip, and the victim device can be re-assembled. No further physical access is required. Next, we extract the sensitive information. The user configurations (password, WiFi SSID, and passphrase) are located in memory address 0x40000-0x50000 in the dumped file. However, this partition is compressed with Zlib and encrypted with DES (data encryption standard).

The camera must first decrypt the configurations at start-up and read the WiFi password before connecting to the Internet. Hence the DES key must be stored on-device. According to the blog post, the key is derived from a string “C200 1.0” (corresponding to the model number and hardware version) at address 0x600c0. However, at this address, in the memory image we dumped, there is a meaningless string (0x06 0x68 0x7a 0x88 0xa8 0xa7 0x01 0x97). We know the model number of our IP camera is C100, and the hardware version is 2.0 according to the nameplate. Therefore, it is natural to seek to search for “C100 2.0” in the dumped file. A matched string appears at memory address 0x700c0. The sting “C100 2.0” is the model-specific key material. To derive the correct DES key, a hash function extracted from IP camera’s firmware is used. By replacing the key material “C200 1.0” with “C100 2.0”, a 64-bit DES key “249c6923” can be derived. Since OpenSSL takes hex strings instead of character strings, we must convert the key into hexadecimal value 0x3234396336393233. Subsequently, we can employ the following command to decrypt the dumped memory image:

```
# openssl enc -d -des-ecb -nopad -K [DES key] -in [dumped image] -out [out file]
```

This command specified using the encrypting function “enc” in the OpenSSL toolbox. The parameter “-des-ecb” specifies selecting the DES cipher and operating it in ECB (electronic codebook) mode. No padding is used as “-nopad”. The DES

---

2Available: https://www.instructables.com/CH341A-Programmer/

3We follow the Blog post at https://drmnsamoliu.github.io/

4Available: https://drmnsamoliu.github.io/assets/code/key.c
key 323439633693233 should be filed after the keying flag “-K”. The dumped memory image is passed in, following the “-in” flag. In the end, use the “-out” flag to specify a location to save the decompressed file. Once the dumped memory image is decrypted, we can use binwalk command to decompress it:

```
binwalk -e [decompressed file]
```

binwalk is an open-source toolbox for firmware image analysis. Flag “-e” indicates to extract known file types automatically. The extracted user configuration will be placed in a new folder. If successful, a readable user configuration should be available.

Inside the extracted user configuration file, we can see the IP address, supported network protocols, user name, and passwords. Instead of storing a clear text password, the IP camera stores a hash value of the password. As a hash function, it is undesirable to be able to invert a hash value to its plaintext form (a.k.a., pre-image attack [20]). One promising attack to revert the hash is to use a rainbow table. Rainbow table is a pre-computed mapping table from chosen plaintext to hash values and vice versa. We have used the online rainbow table website https://crackstation.net/ to successfully revert the password of one shared account in our IP camera and used this information to successfully gain access to the RTSP (real-time streaming protocol) from the IP camera.

We demonstrate obtaining unauthorized access to a video stream using information extracted from the WiFi IP camera’s memory dump in https://youtu.be/fnIn9QugrXI. Importantly, the entire attack process takes less than 25 minutes. Only the first 8 minutes require physical access to the target camera. The firmware analysis and cracking of the dumped firmware can be done offline, using freely available tools.

**Summary.** The data stored in off-chip Flash memory can be easily read out through the exposed memory bus even when the system is powered off. The manufacturer has employed multiple techniques to enhance the security, such as encrypting the user configuration partition and storing hash value instead of the original password. The shared password can be reverted from hash using a rainbow table in our demo. Password salting could effectively mitigate such attacks.

**VII. CONCLUSION AND DISCUSSION**

We considered the dangers of open debug interfaces and exposed memory buses in commercial IoT devices. With two case studies, we showed the simplicity and the low cost of attacks by a person with entry-level knowledge on embedded systems—notably, the first attack only required less than 30 minutes and the second, only requires less than 8 minutes of access to the device. Evidently, security of IoT devices still require further emphasis from device manufacturers. Strategies such as disabling the debug interface supported by SoCs, securing the exposed memory buses by encrypting sensitive memory partitions and salting passwords are minimal to no additional cost step to improve current state-of-practice. However, secure on-device key derivation remains a challenging problem where memory fingerprint based methods can provide secure alternatives [17], [23], [7]. We hope our work will help support development of mitigation methods, inform threat models, and increase awareness of a different threat dimension posed by electronic devices employed in everyday life.

**REFERENCES**

[1] A. Afuang, T. Rago, A. Mukherjee, B. Rojas, and H. Uijhazi. IoT growth demands rethink of long-term storage strategies, says IDC, 7 2020.

[2] H. Badran. IoT security and consumer trust. In Proc. Annu. Int. Conf. on Dig. Gov. Res. (DG.O), pages 133–140, 2019.

[3] J. Bartlett. Electronics for Beginners. Apress, 2020.

[4] M. Capelluto, J. Liranzo, M. Z. A. Bhuian, T. Hayajneh, and G. Wang. Security and attack vector analysis of IoT devices. In Proc. Springer Int. Conf. on Secu., Privacy and Anonymity in Comp., Comm. Storage (SpaCCS), pages 593–606, 2017.

[5] A. Cui, M. Costello, and S. Stolfo. When firmware modifications attack: A case study of embedded exploitation. In Proc. The Network and Distributed System Security Symposium (NDSS), 2013.

[6] B. D. Davis, J. C. Mason, and M. Anwar. Vulnerability studies and security postures of IoT devices: A smart home case study. Internet of Things J., 7(10):10102–10110, 2020.

[7] Y. Gao, Y. Su, W. Yang, S. Leni, S. Nepal, and D. C. Ranasinghe. Building secure SRAM PUF key generators on resource constrained devices. In Proc. IEEE Int. Conf. on Pervasive Comput. Comm. Workshops (PerCom Workshops), pages 912–917, 2019.

[8] A. Gupta. The IoT Hacker’s Handbook: A Practical Guide to Hacking the Internet of Things. Apress, 2019.

[9] Y. Hammi, S. Zeadally, H. Labiod, R. Khatoun, Y. Begriche, and L. Khoukhi. A secure multipath reactive protocol for routing in IoT and HANETs. Ad Hoc Networks, 103:102118, 2020.

[10] A. Ibrahim, A.-R. Sadeghi, and G. Tsudik. Us-aid: Untangled scalable attestation of IoT devices. In Proc. IEEE Symp. on Reliable Distributed Syst. (SRDS), pages 21–30, 2018.

[11] T. Instruments. MSP430G2x33 Datasheet, Apr 2016.

[12] A. Jha and M. Sunil. Security considerations for internet of things, L&T Technology Services, 2014.

[13] M. A. Khelif, J. Lorandel, and O. Romain. Non-invasive I2C hardware trojan attack vector. In Proc. IEEE Int. Symp. on Defect and Fault Tolerance in VLSI and Nanotec. Syst. (DFT), pages 1–6, 2021.

[14] A. S. Krishnan and P. Schaumont. Exploiting security vulnerabilities in intermittent computing. In Proc. Int. Conf. on Secur. Privacy, and Applied Cryptography Eng. (SPANCE), pages 104–124, 2018.

[15] H. Li, M. Bhargav, P. N. Whatmough, and H.-S. P. Wong. On-chip memory technology design space explorations for mobile deep neural network accelerators. In Proc. ACM/IEEE Des. Autom. Conf. (DAC), pages 1–6, 2019.

[16] M. Liyanage, A. Braeken, P. Kumar, and M. Ylianttila. IoT Security: Advances in Authentication. John Wiley & Sons, 2020.

[17] R. Maes, A. Van Herrewege, and I. Verbauwhede. PUFSKY: A fully functional PUF-based cryptographic key generator. In Int. Workshop on Crypto. Hardw. and Embed. Syst. (CHES), pages 302–319, 2012.

[18] L. Morel and D. Couroussé. Idols with feet of clay: On the security of bootloader and firmware updaters for the IoT. In Proc. IEEE Int. New Circuits and Syst. Conf. (NEWCAS), pages 1–4, 2019.

[19] A. A. Pammu, K.-S. Chong, W.-G. Ho, and B.-H. Gwee. Interception side channel attack on AES-128 wireless communications for IoT applications. In Proc. IEEE Asia Pacific Conf. on Circuits and Syst. (APCCAS), pages 650–653, 2016.

[20] Y. Sasaki and K. Aoki. Finding preimages in full MD5 faster than exhaustive search. In Proc. Springer Annu. Int. Conf. on the Theory and App. of Crypto. Tech. (Eurocrypt), pages 134–152, 2009.

[21] S. Skorobogatov. Physical attacks and tamper resistance. In Introduction to Hardware Security and Trust, pages 143–173. Springer, 2012.

[22] Y. Su, M. Chesser, Y. Gao, A. P. Sample, and D. C. Ranasinghe. Wisecr: Secure simultaneous code dissemination to many devices. In Proc. IEEE Symp. on Dependable and Secure Comput., 18(4):1699–1717, 2021.
A key resource is a book by reverse engineering expert Edwin Sobey\(^5\). Sobey talks about salvaging useful components from broken or old electronics in this book. More importantly, readers can study how to use correct tools to dissect the device, identify valuable parts that can be reused, basic knowledge about things they work, and safety rules to follow when unscrewing devices. Notably, this book was published in 2011 and some techniques are outdated with the rapid evolution of industrial designs. For example, nowadays, more and more devices have their casing held together with adhesive or ultrasound welding rather than screws and clips commonly used in 2011. For readers without an electronics background, an introductory book to build and test some simple circuits is a good starting point. This book covers basic electronics concepts, schematics, circuit analysis and calculations. Given some familiarity with electronics, *The IoT Hacker's Handbook* written by Aditya Gupta [8] provides in-depth insights into hardware and embedded system exploitation to firmware exploitation.

Then, iFixit\(^6\) is a wiki-based website for user-generated content sharing focusing on repairing technological devices. The website provides video content from experienced people with step-by-step recipes to tear down the device. This may largely reduce the risk of having your device damaged or injuring yourself. Another wiki-based website, exploitee.rs, focuses on hacking where the content provides information on how to find hidden debug interfaces and how to decrypt dumped firmware from the examples provided therein.

### APPENDIX B

#### ATTACKER TOOLS

- **Multimeter:** An instrument that can measure basic electrical properties, such as voltage, current, resistance, and so on. We recommend choosing a multimeter with diode forward biasing and wire connectivity function. The model we used in this work is a US$33 Stanley STHT77364, an US$10 alternative Gator XL830L from could be an alternative.
- **Logic analyzer:** An instrument that can measure fast varying digital signals, records those signals over time domain, and performs analysis to discover the information encoded. In this work, we did not use a logic analyzer, in future work we will use a US$300 Digilent Analog Discover 2 to demonstrate the analysis of U-Boot entry point by monitoring the off-chip Flash memory bus traffic. For such kind of task a 24MHZ 8 Channel open-source logic analyzer priced US$15 is adequate.
- **Flash memory programmer:** A low-cost (US$15) device to read out the Flash (generally also supports EEPROM) memory content from or write image files to Flash memory chips. A model with a test clip for fast and clean hooking up the exposed memory bus is more useful. The CH341A Pro Flash memory programmer used in this work is priced US$10 on ebay.com.
- **JTAG programmer/debugger:** JTAG is also known as the IEEE 1149.1 standard for deploying and debugging firmware on the chip and also offers low-cost and time-saving testing for all components in a system through boundary-scan. JTAG is widely used in industry. Different system architectures may require different JTAG programmers, the one we used to extract electronic lock programming code from MSP430G2433 is an US$150 MSP-FET430UIF. Compatible MSP430 JTAG programmer from a third party is around US$35. An universal JTAG programmer supports ARM, MIPS and RISC-V also priced at US$35 on ebay.com.
- **Embedded system development board:** Such as Raspberry Pi Zero (US$10), Arduino UNO R3 (US$22) or STM32 Bluebell (US$15). Those development boards are useful, for example, to deploy JTAGenum\(^7\), an open-source program for identifying JTAG pin-out definitions.

## DISASSEMBLY OF THE ELECTRONIC LOCK AND IP CAMERA

To disassemble the electronic lock, a T-10 screwdriver is required to remove the four bolts holding the back panel in place. Subsequently, all internal parts can be removed by hand within 1 minute, without a tool, as illustrated in Fig. 8. Our technique to get access to the JTAG pins is to solder a 1.27 mm 7-pin header. This requires 5 minutes. Accessing the internal NVM using MSP-FET430UIF debugger can take another 3 minutes. We can de-solder the jumper wire header in 3 minutes with a hot air gun and take another 3 minutes to put all parts together. The entire process takes 15 minutes and could be further shortened by using a data repair tool (available on ebay.com for US$21) instead of soldering a pin header.

The disassembly of the WiFi IP camera simpler. We can remove the front panel of the camera by inserting a lever into its edge and gently applying a force as shown in Fig. 9. Then the mainboard is removed by freeing the snap-fit in less than one minute. It takes tens of seconds to attach the Flash programmer test clip to the exposed Flash chip and

---

\(^5\)E. Sobey. *Unscrewed: Salvage and Reuse Motors, Gears, Switches, and More from Your Old Electronics*. Chicago Review Press, 2011.

\(^6\)www.ifixit.com

\(^7\)https://github.com/cyphunk/JTAGenum

---

[24] S. Vasile, D. Oswald, and T. Chothia. Breaking all the things—a systematic survey of firmware extraction techniques for IoT devices. In *Proc. Springer Int. Conf. on Smart Card Res. and Adv. App. (CARDIS)*, pages 171–185, 2018.

[25] X. Wuhan. Xm25q664c 3v 64m-bit serial flash memory with dual/quad spi &amp; qpi, Nov 2020.

[26] H. Yuan, J. Zhao, B. Zhao, X. Xie, Z. Li, Q. Zhang, G. Wang, F. Ma, Y. Zhi, and S. Chang. A fast and simple method for obtaining microcircuit card information. In *Proc. Adv. Info. Manage., Comm., Elec. and Auto. Control Conf. (IMCEC)*, pages 1075–1079, 2019.
short circuit the **RESET** pin of the SoC. Reading the Flash memory via SPI is the most time-consuming part, taking 3 to 4 minutes. Once the memory image is dumped, the target IP camera is re-assembled in another minute. We conclude the entire process is possible in 8 minutes. The firmware analysis and cracking of the dumped firmware can be done offline, as shown in our demo video [https://youtu.be/fnln9QugrXI](https://youtu.be/fnln9QugrXI).

Fig. 8. Tear-down of the electronic lock: (a) front side; (b) back side; (c) with back panel removed; (d) the electronic assembly; (e) the circuit board is visible after removing the waterproof silicone rubber keyboard.

Fig. 9. (a) the front side of the TP-link Tapo C100 IP camera; (b) with the front panel removed; (c) the back side of the main board; and (d) the pin definition of the MX25QH64 SPI Flash chip.