Design and Testing of the Address in Real-Time Data Driver Card for the Micromegas Detector of the ATLAS New Small Wheel Upgrade

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Abstract—The address in real-time data driver card (ADDC) is designed to transmit the trigger data in the micromegas gaseous structure (Micromegas, MM) detector of the ATLAS new small wheel (NSW) upgrade. The address in real-time (ART) signals are generated by the front-end application-specific integrated circuit (ASIC), named VMM chip, to indicate the address of the first above-threshold event. A custom ASIC (ART ASIC) is designed to receive the ART signals from the VMM chip and implement the hit selection. The processed data from the ART ASIC will be transmitted out of the NSW through the gigabit transceiver (GBTx) serializer, the unidirectional versatile twin transmitter (VTTx), and fiber-optic links. The ART signal is used to generate the trigger decision [4]. This signal can test all the functions of the ADDC and it has long-term stability. This article will introduce the design, testing procedure, and results of the ADDC and the FMC testing platform.

Index Terms—ATLAS, embedded system, field-programmable gate array (FPGA), gigabit Ethernet transceiver, micromesh gaseous structure (Micromegas) detector, trigger electronics.

I. INTRODUCTION

The new small wheel (NSW) is part of the ATLAS Phase I upgrade project which is planned to replace the present muon small wheel, providing the capability to meet the increased luminosity, and reduce the rate of fake coincidences induced by the environmental background (fake triggers) [1], [2]. In the NSW upgrade, two different types of detectors are used: the small-strip thin gap chambers (sTGCs) and the micromesh gaseous structure (Micromegas) detector. The signals from both detectors will contribute to the trigger decision. By cross-checking the results from the NSW and the current big wheel trigger station, most of the fake triggers can be eliminated [3].

In the Micromegas detector, the address in real-time (ART) signal is used to generate the trigger decision [4]. This signal is generated by the 64-channel front-end application-specified integrated circuit (ASIC), called the VMM chip, when a detector channel is hit and the output pulse goes above a given threshold [5]. In every bunch crossing (BC), the VMM chip will only provide one encoded 6-bit address of the first hit channel. This encoded 6-bit address is the ART signal.

The block diagram of the NSW electronics is shown in Fig. 1 [6]. Both the sTGC and the MM detectors will have their own electronics for data transmission. In the MM detector electronics, the Level-1 data (time, charge, and strip address corresponding to a single hit) will be transferred through the Level-1 data driver card (LDDC) [7] to a network interface called front-end link exchange (FELIX) [8]. The address in real-time data driver card (ADDC) is in the trigger path to transfer the ART signals from the front-end boards to the trigger processor [9] for the trigger decision. In traditional trigger electronics, the trigger primitives will not be processed during transmission. This structure can be seen in many experiments, including the legacy ATLAS Muon Chamber Small Wheel [10], and the legacy and upgraded Compact Muon Solenoid (CMS) muon trigger system [11]. On the contrary, in the NSW upgrade, the ADDC is designed to perform preliminary hit selection on the board. This hit selection helps to reduce the processing pressure on the trigger processor but import processing latency which should be carefully evaluated and taken care of. The trigger decision from the NSW is part of the ATLAS global trigger system and the latency needs to be controlled within $\sim 1 \mu s$ [12]. Several simulations have...
been performed and the preliminary conclusion is that about 500 ns are required for the trigger processor to make the trigger decision, leaving about 500 ns for the ART data transmission and processing by the ADDC [13].

All the NSW electronics will be synchronized to the global 40.079-MHz BC clock. This clock will be generated by the timing, trigger and control (TTC) module and distributed along with the slow control commands through the FELIX. The FELIX will also distribute the slow control commands. To ensure the upload bandwidth, the optical module on the ADDC is the versatile twin transmitter (VTTx) [14] which has only a dual-channel transmitter but no receiver. The FELIX will send the clock and command signals to the L1DDC and then transfer to the ADDC via another miniSAS connection.

To reduce the ART signal attenuation and also equalize the cable length, the ADDC will be placed close to the Micromegas front-end (MMFE) boards in the middle of the detector. The estimated radiation dose is up to 1700 Gy (inner radius) and the magnetic field is up to 0.4 T. To guarantee the performance and stability in such an environment, several custom ASICs are being used. The ART signals will be processed by one of the custom ASICs, the ART ASIC [15], and each of the ART ASIC can receive up to 32 ART signals from 32 VMM chips on four different MMFE boards. To meet the data transmission requirement in the Large Hadron Collider (LHC), a set of several chips was developed by CERN under the gigabit transceiver (GBT) architecture, namely GBT chipset [16]. In the ADDC design, the serializer–deserializer chip GBTx [17] and the dual-channel transmitter VTTx module are adopted for the data transmission, and the slow control ASIC GBT-steel-reinforced aluminum cable (SCA) [18] is used for the configuration and control purpose.

To take advantage of the dual optical transmitter links on one VTTx module, each ADDC board is designed to handle 64 ART signals with two ART and two GBTx ASICs. In the NSW upgrade plan, a total of 512 ADDC boards will be used to interface with the 4096 front-end boards.

This article will introduce the design of the ADDC and the history of its prototypes. To accelerate the testing of the ADDC, a test platform is designed based on the VC707 commercial field-programmable gate array (FPGA) development kit. The design of this test platform, including the functionality test results and the latency performance, will be presented.

II. ADDC DESIGN AND PROTOTYPES

The ART signal generated by the VMM front-end ASIC consists of a flag pulse followed by six bits, which indicate the address of the strip that received a hit (see Fig. 2). When several channels receive a signal nearly at the same time, the internal circuitry of the VMM always selects the first channel that was hit. The ART circuit can be triggered either by the threshold crossing of the strip signal or by the peak detection circuit. For minimum latency, only the threshold-crossing determination will be used in the experiment. The flag pulse is high for two falling edges of the 160-MHz clock and is kept low until the next rising edge of the clock. The 6-bit address is then serialized on each edge of the clock. Following the ART address, the ART circuit is internally reset for approximately 10 ns.

The ADDC is required to be synchronized with the LHC BC clock (40.079 MHz). It also needs to receive remote configuration and monitoring from FELIX (distributed via L1DDC). The input voltage for board power supply is 12 V, which is the unique power supply voltage to all the NSW electronics.

The final ADDC structure is shown in Fig. 3. As introduced earlier, each ADDC can receive 64 channels of ART inputs from 8 miniSAS connectors. Each miniSAS is connected with an MMFE front-end board (with eight VMM chips on each MMFE board) and the ART data transmission is under scalable low-voltage signaling for 400 mV (SLVS-400) standard [20].
A 160-MHz ART clock, which is synchronized to the global 40-MHz clock, will be provided to the VMM chip to generate the ART signal in the double data rate (DDR) mode. After the hit selection in the ART ASIC, the processed data will be transmitted to the GBTx and then sent to the VTTx optical module in the GBT widebus format.

In addition to the miniSAS for the ART signal, another miniSAS connector is utilized to receive the reference clocks, the bunch-crossing reset (BCR) signals, and other configuration/control signals from the L1DDC. The FELIX will send out these configuration and control signals to the two ART ASICs and GBTx chips via the SCA using the high-level data link control (HDLC) protocol [21]. It will also provide the 40.079 MHz reference clocks to the GBTx reference clock input pins. Then, each GBTx will distribute the 40.079 and 160.316 MHz reference clocks to its corresponding ART ASIC. A radiation-tolerant dc–dc converter ASIC, named FEAST [22], will be used on this board to provide power for all the chips on ADDC.

Up to now, four ADDC prototypes were designed and tested. The first version was designed at very early stage of the project and the major purpose was to verify the data transmission with the GBTx chip. The ART, SCA, and FEAST ASICs were replaced by an FPGA and a commercial power chip due to their unavailability at that time. The second version which was designed with all the ASICs and compiled with the space restrictions is shown in Fig. 3. The third version was designed to finalize the design and was supposed to be the last version before mass fabrication. However, during the tests, the ART ASIC 144 pin low profile quad flat pack (LQFP) package yield rate did not meet the requirement. A preproduction version was designed to evaluate the change in the ART ASIC package and can also be used with sockets as an ASIC testing board. The details of each prototype are introduced in the following sections.

A. ADDC Prototype Version 1 (FPGA-Based)

The first version of ADDC prototype was built based on the Xilinx Artix-7 FPGA and is at half of the final scale (handles 32 channels of the ART input) [23]. At this time, the ART ASIC was still under development, and thus, the FPGA was used to verify the ASIC design and the communication with the GBTx chip. With the help of the ART ASIC designer group, the hardware description language (HDL) code of the ART ASIC was migrated to the Artix-7 FPGA to implement the hit-selection algorithm. The versatile transceiver (VTRx) module, which has one transmitter for the uplink data transmission and one receiver for the downlink configuration, is used instead of the VTTx module. The Joint Test Action Group (JTAG) standard based remote configuration in the Artix-7 FPGA is achieved by the optical fiber with the quad small form-factor pluggable (QSFP) module. The photo of the assembled ADDC version one prototype is shown in Fig. 4. There are no restrictions in the dimensions because it is only used in the laboratory. Also, the commercial dc–dc converter LTM4619 was used in this prototype instead of the FEAST module as the latter power module was not available at that time.

B. ADDC Prototype Version 2 and Version 3

In the ADDC prototype version 2 and version 3 (as shown in Fig. 5), the dimensions were restricted, and all the radiation-tolerant ASICs were evaluated. Dedicated inductors and capacitors are selected to ensure the performance under radiation and strong magnetic field environment. These prototypes were also at the full scale to handle 64 channels of the ART inputs. Each ART ASIC has 32 differential input ports to receive the ART signals at 320 Mbps. After hit selection, the result will be transmitted to 14 GBTx e-link ports, which run under widebus mode at 320 Mbps. Then, the VTTx module is used to collect the data from the two GBTx chips and transmit them to the trigger processor.

C. ADDC Preproduction Prototype

In the second and third prototypes, the ART ASIC used the 144 pin LQFP package. However, the yield rate of this package did not meet the requirement and thus a 128 pin LQFP package is proposed as a replacement. According to this change, the ADDC preproduction prototype (as shown in Fig. 6), design was also revised. The use of mounting
holes makes the board compatible with sockets. With sockets mounted on the board, it can also serve as an ART ASIC test board to verify its functionality before assembly. Various tests are already planned for the preproduction prototype and once the tests are finished successfully the massive production will start.

III. TESTING OF THE ADDC

To provide a complete and extensive test environment for the ADDC boards, a test platform has been deployed based on the VC707 FPGA kit plus specially designed FPGA mezzanine card (FMC). This test platform works with the VC707 development kit, connects to the ADDC, and provides the simulated ART signals and configuration/clock signals to the ADDC board. A dedicated FPGA firmware has been developed to generate the ART signals and also receive the two channels of processed data from the VTTx of the ADDC, to examine whether there is any error during the ART hit selection or data transmission. The diagram of this test platform and its connections to the ADDC is shown in Fig. 7. There are eight miniSAS connectors on this FMC test board to provide the simulated ART signals to the ADDC and an additional miniSAS connector to provide the configuration/clock signals. To emulate the configuration communication from FELIX/L1DDC, a GBTx is placed on the FMC test board (which emulates the GBTx on L1DDC). This GBTx can be bypassed by sending the configuration data directly from the FPGA to another preserved miniSAS (CH 4 in Fig. 7). In order to ensure that it ideally simulates the real environment, this is only a backup plan for early debugging purpose. With the VTRx module, it communicates with the VC707 FPGA that runs a GBT–FPGA-compatible firmware (which emulates the FELIX). Two small form-factor pluggable (SFP) modules are placed on the FMC board to receive the two optic channels from the VTTx on the ADDC. The received data will be transmitted to a computer for data analysis (which emulates the trigger processor).

A. ADDC Test Platform Firmware Design

In the test platform firmware (as shown in Fig. 8), the Microblaze soft processor core will handle all the data transmission to/from the computer via the Ethernet port. Additionally, the firmware implements three major modules to communicate with the ADDC.

The first part is the module that distributes the ART signals to the miniSAS ports. The simulated parallel ART data will be generated by the software consisting of the BCID, ART channel (0–63), and the 6-bit address. This module will translate the simulated ART data to the corresponding miniSAS channel in the serial bit stream.

The second one is the configuration module that communicates with the SCA chip on the ADDC. Although this module has the direct link to communicate with the SCA chip through the reserved miniSAS connector, in normal tests it will go through the GBTx chip on the FMC mezzanine. The purpose of this route is to simulate the real use case when the ADDC receives the commands from FELIX via the GBTx on the L1DDC board. The configuration data will be encapsulated under the HDLC protocol by the software and then, in the firmware, it will be organized in the GBT frame.

The third part is a revised version of GBT–FPGA firmware to receive the processed data from the ADDC. The DDR module is integrated to achieve the Ping-Pong buffering structure for the data. Then, the data can be read out by the Ethernet under the direct-memory-access function through the Advanced eXtensible Interface (AXI) bus.

B. ADDC Test Software Design

The software, designed in Python, provides the configuration data to the ADDC and performs the full test of all ADDC functions. Since the configuration data to the ADDC will go through the SCA ASIC, the HDLC protocol is implemented. The ADDC can be configured to run under several different modes and for each mode the test software will generate corresponding data to send to the ADDC miniSAS inputs and then check the results back from the ADDC fibers.
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Fig. 9. Flowchart of the test platform software. When the test starts, it will first perform the configuration and phase alignment and then step into the test of each aspect. If any error is detected, it will be recorded and ends the testing.

Fig. 10. ADDC under testing with the test platform. No other NSW electronics are required during the laboratory test of the ADDC.

The flowchart of the test software is shown in Fig. 9. Initially, the connection with the VC707 is established via the Ethernet and then follows the configuration of the GBTx on the FMC mezzanine. Then, it will start to configure the GBTx and ART ASICs on the ADDC via the SCA chip. After every power on, the phase relationship between the GBTx/ART might be changed; thus, the ART ASIC has to be configured to send out preset static data to align with the output phase. The 64 input channels have also to be aligned with the preset data pattern that can be chosen by the software. After all the chips are configured and the phases are aligned, the software will go through each test on the ADDC. If any error is found during these tests, the information will be recorded and the board will be marked.

Fig. 11. Block diagram of the latency test for the ADDC. In addition to the overall latency for the full ADDC board, the detailed latency for the ART ASIC and the GBTx + VTTx module are also measured.

The ADDC is a key component on the MM trigger path; hence, the latency performance is of great importance and as it was described in Section I is required to be under 500 ns. This latency test was also performed with the FMC test platform. The scheme of the test is described in Fig. 11. Two test points are placed on the FMC to measure the delay of the transmitted test signal and the received processed result. Another test point is placed on the ADDC to measure the hit-selection processing time by the ART ASIC.

There are five points shown in Fig. 11, and the latency of the ADDC is the delay from point “0” to point “2.” Since point “2” is the output from an optical module, it is difficult to do the measurement directly; the latency from “Start” to “Stop” is measured instead and the result between point “0” and “2” is calculated by subtraction. When the test platform begins to send the serial ART data to the miniSAS connectors of the ADDC, it will also generate a flag signal which can be captured by the oscilloscope as the “Start” point. On the other hand, after the test platform receives the results from the ADDC, it will also generate a flag signal indicating the “Stop” point. For better understanding the latency of the ART ASIC, a differential probe is used to monitor its output at point “1.”

The latency between the start and stop points is measured to be around 254 ns. This result includes the latency from the ADDC, the propagation delay in the 0.5-m miniSAS cable (estimated to be about 3 ns), and the 2-m fiber (estimated to be about 10 ns), and the last part is from the SFP module and the RX end of the customized GBT–FPGA firmware, which has been analyzed and measured previously in the test of [24] and is around 54 ns. So, the latency of the ADDC can be calculated and it is around 187 ns, which is much less than the 500 ns requirement.

Furthermore, the measurement shows a latency between the start and point “1” to be around 47 ns. Thus, the latency of the ART ASIC is around 44 ns and the latency of the GBTx plus VTTx module is around 143 ns.

IV. CONCLUSION

The NSW deployment in the ATLAS Phase I upgrade is planned to maintain the efficient muon detection with increased event rate. For the Micromegas detector, the ART signal which reflects the 6-bit address of the hit channel is the trigger primitive. The ADDC board is designed to implement the preliminary hit selection and transmission of
the ART signal to the trigger processor and its performance is a critical part of the trigger system in the NSW. The ART ASIC is custom designed to deal with the ART signal on the ADDC. Before this chip is delivered, an Artix-7 FPGA has been used on the first version of ADDC prototype to evaluate its design and the communication with the other radiation-tolerant chips used on ADDC. Since the second version of ADDC prototype, all these radiation-tolerant chips, including ART ASIC, have been evaluated and tested. In addition to the integration tests of ADDC and other NSW electronics, an FMC-based test platform has been designed to provide the individual test environment for the ADDC prototypes and for future mass production ADDC boards. This test platform is controlled by a computer via Ethernet, and the Microblaze soft core is used for configuration and data transmission. With the help of this platform, all the functions of the ADDC and the latency performance have been verified.

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