A new hybrid DC circuit breaker topology

C C Zhu¹, K J Li¹,², R Li³, H Zhang², L J Sun² and Y L Hu³

¹Institute of Renewable Energy and Smart Grid, Shandong University, Jinan, Shandong 250061, China
²China Electric Power Research Institute, Beijing 100192, China
³Jinan University, Jinan, Shandong 250022, China

E-mail: lkjun@sdu.edu.cn

Abstract. Being advantageous for long-distance power transmission and new energy connection, DC system has wide range of applications in many scenarios. As the capacity of DC power grids increases, the fault current is more difficult to interrupt. And the DC circuit breaker which is very important for protecting DC grid attracts more and more attention of researchers. In this paper, a new hybrid DC circuit breaker topology based on the technique of thyristor forced current zero is proposed. The breaker is able to interrupt the fault current in several milliseconds, and the mechanical switch can be cut off at zero current. In addition, no extra power supply and control devices are needed, the pre-charging capacitor can obtain energy from DC grid directly. Therefore, the control process is simpler and the reliability is greatly improved. The operating principle of the proposed circuit breaker is analyzed in detail, and then the simulation is carried out in PSCAD/EMTDC which verifies the correctness of the theoretical analysis and the feasibility of the breaker.

1. Introduction

With the sustained and rapid growth of the national economy, the power grid capacity is gradually increasing [1]. And the high voltage direct current (HVDC) system has been widely used in long-distance and large-capacity transmission and asynchronous interconnection of AC systems. With the rapid development of renewable energy, especially offshore wind power, it is urgent to solve the problem of large-scale new energy grid connection. The HVDC technology provides an effective solution for the grid-connection of distributed generation. It has become possible to construct a multi-terminal DC system that connects a plurality of converter stations, as the flexible HVDC technology based on voltage source converter (VSC) develops rapidly and it can be foreseen that the DC grid will become a development tendency of the future grid [2].

Unlike AC grid, there are no transformers in DC grid, and the impedance of DC system is significantly reduced. When a short-circuit fault occurs, the current rises quickly and the amplitude is high. The power electronic devices of VSC with low overload capacity will be locked and the converter station will quit operation. This potential risk greatly reduces the reliability of DC grid [3]. In addition, the technical difficulty in achieving the rapid breaking is also greatly increased because there is no natural zero-crossing point in the DC short-circuit current. Therefore, the development of high voltage DC circuit breaker with quick acting capability will be one of the key technologies to ensure stable operation of DC grid [4,5].

There are mainly three types of the DC circuit breaker: the mechanical breaker, the solid-state
breaker and the hybrid breaker, where the third type is the research focus [6,7]. ABB has developed a hybrid HVDC circuit breaker based on IGBTs in series-parallel which can cut off the fault current with a high speed [8]. However, the breaker has the problem of poor economy because of the high price of IGBT, and the breaking capacity is also limited.

Due to the advantage of flow capacity, many scholars have been researching the thyristor-based hybrid DC circuit breaker. In [9], the author proposed a zero current hybrid breaker topology where the mechanical switch can be opened almost without arc. In [10], an improved topology with higher reliability was proposed in which the diode is anti-parallel with the mechanical switch. However, the capacitor in the breakers should be charged by additional power supply, where the control difficulty and the cost are increased, and what’s more, the design of the charging power should be solved.

According to the present research situation, this paper proposes a hybrid DC circuit breaker topology based on the thyristor forced current zero technique, which requires no additional charging power and the control is simper. The process of cutting off the short circuit current is elaborated, and also it is verified by simulation in PSCAD/EMTDC.

2. Topological structure
The topology of the DC circuit breaker proposed in this paper is shown in the figure 1. The circuit breaker is composed of three branches in parallel. Among them, the main branch is composed of a fast mechanical switch $K$ and freewheeling diode $D$ in parallel; The current transfer branch consists of thyristor $T$, inductor $L$ and capacitor $C$; Resistor $R_1$ and capacitor $C_1$ constitute an auxiliary charging branch to precharge capacitor $C$; and the energy absorption branch is formed with plenty of metal oxide arresters (MOVs) in series-parallel. $U_{dc}$ is the DC power source, $L_{dc}$ is the current limiting reactor, $L$ is the line reactance and $R_s$ is the line resistance.

![Figure 1. Topology of the proposed DC circuit breaker.](image)

In normal operation, the fast mechanical switch $K$ is closed and the thyristor $T$ is turned off, the current is supplied to the load via the main branch, and the capacitor $C$ is charged via the $C$-$R_1$-$C_1$ branch. The current value in the auxiliary charging branch is zero during steady-state operation, and the voltage is distributed between the two capacitors according to the capacitance of $C$ and $C_1$. Ignoring the line impedance, the voltage of capacitor $C$ in steady state is

$$U_{c,0} = \frac{C_1}{C+C_1} U_{dc}$$

(1)

Therefore, without the need for extra charging power supply and charging control devices, the charging voltage of $C$ can be obtained from the DC system directly, which not only reduces the difficulty of control and the cost of investment, but also improves the overall reliability of the switchgear.
3. Operation principle

Figure 2 shows the waveform diagrams of the DC circuit breaker when breaking fault current, where $i_s$ is the total short-circuit current, $i_K$ is the current flowing through the fast mechanical switch $K$, $i_T$ is the current flowing through thyristor $T$, $i_D$ is the current flowing through freewheeling diode $D$, $i_{mov}$ is the current flowing through MOV, and $u_{brk}$ is the voltage across the breaker.

![Waveform Diagrams](image)

**Figure 2.** Breaking waveforms of the breaker.

The line current rises rapidly if a fault occurs. When the pre-set value of action current $I_a$ is reached, the detection device of the breaker detects the fault and sends a signal, so that the breaker operates to switch off the short-circuit current.

Since the resistance value of $R_1$ in the auxiliary charging branch is several kΩ, the current flowing through is much smaller than the short-circuit current, so the influence of the branch can be ignored during the process. The equivalent circuit in each stage of the turn-off process is shown in figure 3.

![Equivalent Circuits](image)

**Figure 3.** Equivalent circuit of each stage.
The first stage: $t_0$--$t_1$. The fault occurs at time $t_0$ and the current increases rapidly, when it reaches $I_0$, the detection device sends the signal, and after a short delay, $T$ starts to turn on at time $t_1$. According to the equivalent circuit, the expression of the short-circuit current is

$$i_s = \frac{U_{dc}}{R_s} + (I_0 - \frac{U_{dc}}{R_s})e^{-\frac{t}{\tau_s}}$$

(2)

Where, $I_0$ is the load current, $\tau_s = (L_s + L_{dc})/R_s$.

The second and the third stages: $t_1$--$t_3$. After $T$ turns on, $L$ and $C$ form an oscillating circuit through $K$, $i_T$ increases rapidly, and $i_s$ starts to decrease and falls to zero at time $t_2$. Then the main branch current begins to increase in reverse. If $K$ is broken at time $t_2$, the main branch current will flow in the reverse direction through $D$, the voltage across $K$ will be close to zero and there will be no arc between the break. Then $i_T$ starts to decrease gradually after it reaches the peak value, at time $t_3$, $i_T$ is equal to $i_s$, $i_D$ drops to zero and $D$ turns off. The current expression of the transfer branch during this process is

$$i_T = \frac{U_{c0}}{\sqrt{LC}} \sin \frac{t-t_1}{\sqrt{LC}}$$

(3)

Time $t_2$ and time $t_3$ can be obtained by solving the simultaneous equations of (2) and (3), where the condition is that when $i_T$ peaks, it must be larger than $i_s$ at the moment, so

$$\frac{U_{c0}}{\sqrt{LC}} > \frac{U_{dc}}{R_s} + (I_0 - \frac{U_{dc}}{R_s})e^{-\frac{(t-t_1)\pi}{\tau_s}}$$

(4)

The interval from $t_2$ to $t_3$ should be long enough to ensure that the switch $K$ can be opened reliably.

The fourth stage: $t_3$--$t_4$. After $T$ turns off, $i_T$ charges to $C$ flowing through the path of $T-L-C$, and the voltage of the capacitor $C$ rises quickly. Regardless of the effect of $L_s$, the voltage across the circuit breaker $u_{brk}$ is equal to the capacitor voltage $u_C$. When $u_{brk}$ rises to $U_{dc}$, $i_s$ peaks and then starts to decrease, and at time $t_4$, $u_{brk}$ reaches the operating voltage of MOV. If the voltage direction of $C$ under polarity reversal is the reference direction, the equation that the voltage across the circuit breaker should be satisfied is

$$(L_s + L_{dc})C \frac{d^2 u_{brk}}{dt^2} + R_s C \frac{du_{brk}}{dt} + u_{brk} = U_{dc}$$

(5)

The expression of $u_{brk}$ can be obtained according to the voltage of capacitor $C$ and the current of inductor $L$ at time $t_3$, and then the short-circuit current at this stage can be obtained by

$$i_s = C \frac{du_{brk}}{dt}$$

(6)

The fifth and the sixth stages: $t_4$--$t_6$. After $t_4$, the impedance of MOV drops rapidly, so that $i_s$ transfers to the energy absorbing branch and $i_{mov}$ gradually increases. At time $t_5$, $u_{brk}$ reaches the protective level of MOV and $i_s$ only flows through the arrester, $i_T$ decreases to zero and $T$ turns off, then the arrester continuously absorbs the inductive energy. At time $t_6$, the stored energy of the inductor is consumed, meanwhile $i_s$ reduces to zero and $u_{brk}$ reduces to $U_{dc}$. At this point the whole breaking process is completed.

4. Simulation evaluation

In order to verify the feasibility of the DC circuit breaker topology proposed in this paper, a simulation circuit was built in PSCAD/EMTDC to research the fault current cut-off process of the breaker, and
Table 1. Simulation parameters.

| Parameter                      | Value  | Parameter                      | Value  |
|-------------------------------|--------|-------------------------------|--------|
| Voltage of DC source \(U_{dc}\) | 10 kV  | Oscillation capacitance \(C\) | 100 μF |
| Line resistance \(R_s\)       | 0.2 Ω  | Charging capacitance \(C_1\)  | 100 μF |
| Line reactance \(L_s\)        | 0.2 mH | Charging resistance \(R_1\)   | 1 kΩ   |
| Current-limiting reactance \(L_{dc}\) | 2.8 mH | Action current \(I_a\)       | 3 kA   |
| Oscillation reactance \(L\)   | 100 μH |                               |        |

During normal operation, the load current is 1 kA. At the 1.0s, a fault occurs, and then the whole switch-off process continues for about 4ms. Figure 4 shows the current waveforms of each branch.

As shown in the figure, the line current rises rapidly after the fault occurs, and when it reaches 3 kA, the single of action is send. After a delay of 100 μs, the thyristor \(T\) turns on and \(i_T\) gradually increases, while the main branch current \(i_{main}\) starts to decrease. After about 80 μs, \(i_{main}\) drops to zero and begins to increase in the opposite direction. At this moment, the fast mechanical switch is broken and \(i_{main}\) continues to flow through the freewheeling diode \(D\). Afterwards, \(i_D\) increases first and then decrease to zero, so that the switch can be shut off at zero current with the process lasting for about 130 μs.

The peak value of \(i_T\) is approximately 4.8 kA, which is slightly lower than the calculated value due to the effect of the auxiliary charging branch and the forward voltage drop of the semiconductor device, and it is within the short-term current endurance capability of the thyristor. After \(D\) turns off, the fault current charges the capacitor \(C\) in reverse. And the short-circuit current reaches the peak value of about 4.1 kA when the capacitor voltage rises to \(U_{dc}\). Then the fault current starts to decrease.

As shown in figure 5, when the voltage of \(C\) reaches 11 kV, which is equal to the operating voltage of the arrester, the fault current transfers to MOV. Although the inductance of \(L\) is small, the inverse...
voltage across \( L \) can not be ignored because the impedance of the arrester drops rapidly, the voltage of capacitor \( C \) is higher than that of the arrester. As the voltage across the breaker rises to the arrester protection level of 15 kV, the current flowing through \( T \) drops to zero and \( T \) turns off. At the same time, the voltage of \( C \) peaks at about 18 kV.

![Figure 6. Circuit waveform of the auxiliary charging branch.](image)

The current waveform of the auxiliary charging branch is as shown in figure 6. The current is reversed, then turns forward and decays. However, the current peak value is less than 15 A, which is much smaller compared to the short-circuit current. Therefore, the switch-off process is not affected by the branch, thus verifying the rationality of the operating principle analysis.

5. Conclusions
This paper presents a thyristor-based hybrid DC circuit breaker topology. According to researching the equivalent circuit in each stage of the breaking process, the working principle of the breaker is analyzed. The breaker not only can interrupt the fault current rapidly without arc, but also has low condition losses and large breaking capability. Moreover, no need for additional charging power supply and control device, the control is simpler and the cost is lower. A simulation model of the breaker is built in PSCAD/EMTDC, and the result shows that the fault can be cut within 4ms, which verifies the feasibility of the proposed topology.

The circuit breaker topology proposed in this paper is suitable for applications with large short-circuit current, such as large-capacity load centres. Since the circuit breaker parameters are designed based on the condition of the maximum short-circuit fault current, it is necessary to charge the capacitor in the resonant branch for a long time to operate the arrester during the turn-off process of a small current such as the normal operating current, which causes the break time to be much longer. Therefore, the limitation remains to be further studied. In addition, the breaker is in the theoretical research stage, the technology is not mature, and it faces challenging issues. Then, the following aspects should be focused to strengthen the mechanism research and tackle problems in key technologies.

- The research on typical short-circuit faults of DC grids and the requirement of system protection strategy for the action characteristics of protective equipment under different fault types should be analyzed, which provides detailed short-circuit current waveform, breaking time insulation coordination and other data for the research of the DC breaker, and lay the foundation for guiding equipment development and standard setting.
- The research problems of key components should be overcome to improve its performance stability and reliability. For example, further reducing the opening time and dispersion of the high-speed drive mechanism and improving the mechanical switch life; strengthening the research on triggering technology, voltage and current equalization in the series-parallel application of power electronic devices.

Acknowledgment
This study is supported by State Grid science and technology project ‘Topological Research and
Prototype Development of the Key Equipment for DC Distribution’ (no. PDB17201700161).

References
[1] Flourentzou N, Agelidis V G and Demetriades G D 2009 VSC-based HVDC power transmission systems: An overview IEEE Trans. Power Electron 24 592-602
[2] Wang W, Barnes M, Marjanovic O, et al 2016 Impact of DC Breaker Systems on Multi-terminal VSC-HVDC Stability IEEE Trans. Power Del 31 769-79
[3] Franck C M 2011 HVDC circuit breakers: A review identifying future research needs IEEE Trans. Power Del 26 998-1007
[4] Novello L, Baldo F, Ferro A, et al 2011 Development and testing of a 10 kA hybrid mechanical-static DC circuit breaker IEEE Trans. Appl. Supercond 21 3621-7
[5] Sano K and Takasaki M 2014 A surgeless solid-state DC circuit breaker for voltage-source-converter-based HVDC systems IEEE Trans. Ind. Appl. 50 2690-9
[6] Jean M and Alfred R 2006 A DC hybrid circuit breaker with ultra-fast contact opening and integrated gate-commutated thyristors (IGCTs) IEEE Trans. Power Del. 21 646-51
[7] Wen W, Huang Y, Cheng T, et al 2016 Research on a current commutation drive circuit for hybrid dc circuit breaker and its optimization design IET Generation Transmission & Distribution 10 3119-26
[8] Hassanpoor A, Hafner J and Jacobson B 2015 Technical assessment of load commutation switch in hybrid HVDC breaker IEEE Trans. Power Electron 30 5393-400
[9] Greenwood A and Lee T 1972 Theory and application of the commutation principle for HVDC circuit breakers IEEE Trans. Power App. Syst. 91 1570-4
[10] Liu L, Zhuang J, Wang C, et al 2015 A hybrid DC vacuum circuit breaker for medium voltage: Principle and first measurements IEEE Trans. Power Del. 30 2096-101