Field Programmable Gate Array based Front-End Data Acquisition Module for the COSMICi Astroparticle Telescope System

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Abstract—We describe an FPGA based Front-End Data Acquisition Module (FEDAM) for implementing Time-over-Threshold (ToT) Time-to-Digital conversion (TDC) of pulses obtained from the COSMICi astroparticle telescope detector system photomultiplier tubes. The telescope system consists of a minimum of three scintillation detectors configured to detect particle airshowers likely initiated by Ultra High Energy Cosmic Rays (UHECR). The relative time delay of detection events between the detectors is used to estimate the angle of incidence of the shower. The FEDAM provides time-over-threshold measurements with a resolution of 2 ns. This allows determination of shower direction to an error of 0.035 (cos $\theta$)$^{-1}$ radians where $\theta$ is the angle between the baseline axis through a pair of detectors and the plane representing the shower front.

Index Terms—High energy physics instrumentation computing

I. INTRODUCTION

Time over Threshold (ToT) techniques for determination of high energy particle detector output pulse characteristics is increasingly being applied or under consideration for use in both space and ground based high energy particle and particle astrophysics experiments [1], [2], [3]. In contrast to the more traditional method of analog to digital converter (ADC) based systems for pulse acquisition and digitization [4], ToT approaches are well suited for use with time to digital converters (TDCs) implemented on reconﬁgurable computing hardware such as Field Programmable Gate Arrays (FPGAs). Whereas in the recent past, ToT/TDC systems might have required application specific integrated circuits (ASICs) for implementation, the increasing availability of FPGAs avoids the cost and complication of the ASIC design process [5]. The reprogrammability of FPGAs also provides ﬂexibility in terms of real-time filtering and analysis of the detector pulses according to evolving science priorities of a particular experiment. Additionally, using multiple voltage thresholds in the ToT system provides two data points for pulse shape reconstruction at every voltage threshold level crossed. In the COSMICi Front-End Data Acquisition Module (FEDAM) described herein, a ToT-TDC system implemented using an FPGA is used to estimate the orientation of the front of extensive air showers (EAS) initiated by interactions between high energy astroparticles and the atmosphere of the Earth and to estimate the charge content of the photomultiplier tube output pulses (to be discussed in detail in a subsequent publication). In section II, we describe the FEDAM architecture and hardware design. In section III, we describe the method by which the TDC is implemented on the FPGA. Finally, in section IV, we present time resolution performance data for the FEDAM.

II. FEDAM BOARD DESIGN

A. FEDAM Layout

Figure 1.1 shows the FEDAM electronics board developed through a collaboration between the AstroParticle and Cosmic Radiation Detector Research and Development Laboratory (APCR-DRDL) of the Physics Department at Florida A&M University (FAMU) and Brookhaven National Laboratory. Layout and fabrication of the board was performed in the Instrumentation Division of Brookhaven National Laboratory. The development of the electronics was pursued to facilitate participation of FAMU in the MARIACHI experiment [6].

Voltage pulses from the scintillation detector PMTs are input to the FEDAM through SMA ports located on the left side of the board. The input signal is compared to voltage level thresholds provided by programmable Digital to Analog Converters (DACs) located on the board. Comparators in low-voltage differential signaling (LVDS) input pins of the FPGA determine whether the input pulse voltage on each input channel is greater than each DAC level.

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By setting the DACs to specific threshold levels and recording the times at which each input crosses them, pulses can be represented by a series of bits that represent the shape and time of arrival of input pulses. After the data has been acquired, it is then transferred from the board via a UART serial connection for further processing.

B. FPGA Architecture

Fig 1.2 provides a system level diagram of the FPGA architecture. The COSMICi FEDAM FPGA is a model Stratix II donated to FAMU through the Altera University Program (AUP). The FPGA Architecture consists of three main top level modules. The High-Speed Time Counter (HSTC), a multi-channel pulse-form input-capture datapath, and the Nios II Microcontroller System. The HSTC counts cycles of a 500 MHz on-chip clock derived from the 50 MHz system clock using a phase-locked loop (PLL). The Pulse Capture Datapaths (PCDPs) use the HSTC to timestamp the instants at which the rising and falling edges of the input pulse cross each voltage threshold. The absolute time of each pulse arrival event is determined by counting the number of cycles of a reference high-precision oscillator occurring between GPS 1 pulse per second (1 PPS) clock signals. A soft-core Nios II microcontroller system, developed using the Altera SOPC (system-on-a-programmable chip) Builder tool, is used to run the application firmware.

C. Time-over-Threshold Implementation

The Time-over-Threshold technique is used to represent a pulse by the amount of time that the pulse magnitude exceeds some defined threshold level or levels. The applications of ToT techniques for pulse processing are described in many references [1], [2].

Custom peripheral device interfaces were designed to program the DACs to allow the threshold levels to be controlled in software. Currently, the threshold levels are logarithmically spaced over the expected range of pulse heights; however, sufficient flexibility exists to space threshold levels arbitrarily according to linear, polynomial, logarithmic or other distributions appropriate for adequate pulse shape reconstruction.

III. FPGA BASED TDC

The original plan for implementation of the TDC in the FPGA was based on a ring oscillator design developed by one of the authors (Junnarkar, S.) [7]. Difficulty in reproducibly setting ring oscillator frequencies required pursuing a simpler design described hereafter. Fig. 3.1 and Fig. 3.2 aid in discussion of the TDC conversion.

As shown in the aforementioned figures, the counter value is latched when the threshold levels are crossed from below and above the threshold. By calculating the difference in the latched counter states for each threshold, the time that the input exceeded each threshold can be computed. Combining the pulse width information obtained above along with the voltage magnitude provided by the threshold crossings, the pulse shape can be reconstructed.

IV. Time Resolution Performance

A. Overall Performance

Presently, the maximum sustained rate at which the system can transmit pulse-shape data to the server is measured to be approximately 175 pulses per second, limited by the baud rate of the serial communication link, although this could be improved upon by compressing the data encoding.

The time resolution of the system is defined as the minimum time increment, as measured, between two subsequent digitized time values [8]. For example, a 500 MHz clock yields a time resolution of 2 ns, resulting in a standard deviation for the error of pulse width measurements of approximately 1.15 ns. With respect to a HSTC value, the actual time of threshold crossing of the rising and falling edge of an arbitrary input pulse are randomly distributed within a 2-ns-wide-window according to a uniform probability distribution. The 1.15 ns standard deviation was obtained by analyzing the triangular distribution of the input signal pulse widths for their difference (assuming independence of the rise and fall times). Fig. 4.1 shows the probability distributions used in the analysis. Each voltage threshold crossing time is registered within a uniformly distributed range of 2 ns, providing the triangular distribution from which the error was calculated.

Fig. 4.2 and 4.3 show test results of the FEDAM when supplied an input pulse from an external waveform generator. Multiplying the digitized time values by the time resolution and plotting against the threshold values, Fig. 4.3 is constructed.

B. Determination of Shower Front Orientation

The time difference between detection events occurring between scintillators in a given shower provides a simple estimate of the shower front orientation. See Fig. 4.4 for an illustration of the basic approach in a simplified two-detector scenario.

The figure depicts the detection time delay,

$$t = \frac{r \sin \theta}{c}, \quad (1)$$

between two detectors A and B separated by a distance r, due to a shower event in which the angle between the shower front and the baseline axis between detectors is $\theta$. c is the speed of light, which is appropriate for the highly relativistic particles in high-energy EAS showers. The error in angle is determined from taking the differential of both side of the time delay equation as follows

$$\delta t = \frac{r (\cos \theta) \delta \theta}{c}. \quad (2)$$

Therefore,

$$\delta \theta = \frac{c \delta t}{r \cos \theta}. \quad (3)$$

For a detector separation distance of 10 meters and a pulse width standard deviation of 1.15 ns, we obtain for the error in angle, 0.035/cos $\theta$ radians.
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REFERENCES

[1] T. Akesson, et al., “Particle identification using the time-over-threshold method in the ATLAS Transition Radiation Tracker,” *Nuclear Instruments and Methods in Physics Research* Sec. A 474, pp. 172-187, 2001.

[2] A. Aloisio, P. Branchini, R. Cicaelese, R. Giordano, V. Izzo, S. Loffredo, R. Lomoro, “High-Resolution Time-to-Digital Converter in Field Programmable Gate Array,” *Topical Workshop on Electronics for Particle Physics*, 2008.

[3] J. Bregon, “Design and performance of the silicon strip tracker of the Fermi Large Area Telescope” *Journal of Instrumentation*, vol. 6, pp 1-6, Sept. 2011.

[4] P. Cogan and VERITAS Collaboration, “Analysis of Flash ADC Data With VERITAS,” *30th International Cosmic Ray Conference*, 2007.

[5] R. Cicaelese, A. Aloisio, P. Branchini, R. Giordano, V. Izzo, S. Loffredo, “Implementation of High-Resolution Time-to-Digital Converters on two different FPGA devices,” *WSPC – Proceedings*, 200 pp 1-5.

[6] M. F Bugallo, H. Takafi, M Marx, D. Bynum, J. Hover, “MARIACHI: A multidisciplinary effort to bring science and engineering to the classroom,” in *IEEE ICASSP*, 2008, pp. 2661-2664.

[7] Junnarkar, S “Time-to-Digital Converter Circuits in Radiation Detection Systems”, in *Electronics for Radiation Detection*, K. Iniewski, Ed. Boca Raton, FL: CRC Press, 2011, pp. 337-358.

[8] J. Kalisz, “Review of methods for time interval measurements with picosecond resolution” *Metrologia*, vol 41.1, pp 17-32, 2004.

[9] M. Frank, S. Junnarkar, T. Fagan, R. O’Neal, Jr., Helio Takai, “Design of a Wireless Sensor Network with Nanosecond Time Resolution for Mapping of High-Energy Cosmic Ray Shower Events” in *Proc. SPIE Defense, Security, and Sensing Symposium*, Orlando, FL, Apr. 8, 2010.

Fig. 1.1(a): Front-End Data Acquisition Module. A: Stratix II FPGA (thermal paste applied for cooling system). B: SMA port location for PMT inputs. C: Digital-to-Analog Converters. D: DE9 connector

Fig. 1.1(b): System level diagram of FEDAM. This diagram shows the flow of data through each module of the FEDAM.
Fig. 1.2: Top Level FPGA Architecture Schematic. As shown, two clocks govern the timing of the system, both of which are used in the FPGA—the 50 MHz FPGA system clock and the designed PLL clock used for generating the high speed counter for high time resolution.

Fig. 3.1: Timing diagram representing system clock and high-speed Phase Locked Loop (PLL) clock. The inset depicts high-speed counter sequence from system start.

Fig. 3.2: Diagram depicting a typical analog input pulse along with its resulting digital representation. The threshold voltages compared against the input signal can be selected by dynamic system calibration. The comparator outputs shown below the input pulse are logic high when the input voltage is greater than that of the corresponding threshold and logic low otherwise.

Fig. 4.1: Diagram that depicts the functions $p(t)$ and $q(t)$, the uniform probability distributions of the rising and falling edge threshold crossing times of input pulses, respectively. After convolution of the two distributions, the triangular probability distribution $q(t) \ast p(t)$ is yielded. Using the time resolution of 2 ns, the standard deviation of this triangular probability distribution is 1.15 ns.
Fig. 4.2: Pulse generated by external waveform generator with a nominal pulse height of +2.6V, 20/60 ns leading/trailing edge transition times, and 58 ns pulse width. (In this trace, the horizontal scale is 20 ns/division and vertical is 0.5V/div.)

Fig. 4.3: Plot of results of data from test in Figure 4.3. Blue line was reconstructed with a time resolution of 4 ns. Red line with resolution of 2 ns. The six threshold levels used in this test were 0.24, 0.50, 1.00, 1.50, 2.00, and 2.41V respectively.

Fig. 4.4: Diagram depicting a two-detector configuration labeled with parameters used to determine the orientation of the shower front.