A Soft Cancellation Decoder for Parity-Check Polar Codes

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Abstract—Polar codes has been selected as the channel coding scheme for 5G new radio (NR) control channel. Specifically, a special type of parity-check polar (PC-Polar) codes was adopted in uplink control information (UCI). In this paper, we propose a parity-check soft-cancellation (PC-SCAN) algorithm and its simplified version to decode PC-Polar codes. The potential benefits are two-fold. First, PC-SCAN can provide soft output for PC-Polar codes, which is essential for advanced turbo receivers. Second, the decoding performance is better than that of successive cancellation (SC). This is due to the fact that parity-check constraints can be exploited by PC-SCAN to enhance the reliability of other information bits over the iterations. Moreover, we describe a cyclic-shift-register (CSR) based implementation “CSR-SCAN” to reduce both hardware cost and latency with minimum performance loss.

Index Terms—Polar codes, Soft cancellation, Parity Check, PC-Polar, PC-SCAN, CSR-SCAN.

I. INTRODUCTION

A. Background and related works

Polar codes, proposed by Arikan [1], has been selected as the channel coding scheme for 5G NR control channel. Polar codes with SC decoding is proved to achieve channel capacity at infinite length. To improve error-correction performance at short or moderate length, SC-list (SCL) decoding [2] is proposed by keeping L codeword candidates during the sequential decoding process. In practice, cyclic redundancy check (CRC) [3], parity-check (PC) [4] and convolutional code (CC) [5] bits can be inserted as outer codes to further improve the performance. They can be unified as pre-transformed polar codes [6].

Among the pre-transformed polar codes, PC-Polar codes exhibit low-complexity, flexibility and robust performance gain under fine-granularity evaluations [4]. A simplified version of PC-Polar [7, 8] is adopted by 3GPP [9] to enhance the performance of 5G UCI channel. The PC bit values are set to linear combinations of some preceding information bits, implemented by simple cyclic shift registers. Such a simple pre-transformation, like CA-Polar and PAC-Polar, can improve the code minimum distance [6]. It is shown in [4] that PC-Polar outperforms CA-Polar by 0.2 ~ 1.0dB under SCL decoders with $L = 8$.

B. Motivation and Contribution

The problem with SC and SCL decoders is they cannot output soft decoding results. The latter is essential for many applications such as decoding of concatenated codes [10] and advanced turbo receivers [11] (e.g., in multiple-input multiple-output and non-orthogonal multiple access). To address this issue, a soft-cancellation (SCAN) decoding [12] is proposed to both provide soft output and improve bit error rate (BER) performance. If multiple iterations are allowed, the frame error rate (FER) performance can also improve over SC decoding. Unfortunately, current SCAN algorithms do not support PC-Polar codes, or any pre-transformed polar codes.

In this paper, we propose a parity-check soft-cancellation (PC-SCAN) algorithm and its simplified version to decode PC-Polar codes. This is the first attempt to implement a SCAN decoder on PC-polar codes. Our algorithm incorporates an additional layer in factor graph to account for the PC constraints, and specifies a scheduling method to update the soft information. Simulation results show better BER and FER (with more than one iterations). An example of $N = 64, K = 32$ polar codes is given in Fig. 5.

PC-SCAN requires an additional module on top of SCAN. The module updates the log-likelihood ratio (LLR) of the information/PC bits. At the first glance, the updating rules are similar to those in LDPC codes. However, they turn out to be quite different due to the sequential scheduling of SCAN decoders. Hence, we propose novel LLR updating rules to address this change. Furthermore, to facilitate hardware-friendly implementation, we propose a simplified version of PC-SCAN named CSR-SCAN. The simplification mainly exploits the regular structure of PC-Polar. We show that the performance loss is minimum ($< 0.1$dB in FER) while the additional hardware area beyond the original SCAN decoder is very small.

II. TREE REPRESENTATION OF SOFT CANCELLATION

In this section, we review the basic methods of SCAN to decode the basic Polar codes. The SCAN decoder has a recursive architecture that is similar to the SC decoder. Therefore, it can be represented as a binary tree traversal [13], as shown in Fig. 1(a). Following the notations in [13], a node $v$ in a tree is directly connected to a parent node $p_v$, left child node $v_l$ and right child node $v_r$, respectively. The stage of a node $v$ is defined by the number of edges between node $v$ and its nearest leaf node. All leaf nodes are at stage $s = 0$. The set of nodes of the subtree rooted at node $v$ is denoted by $\mathcal{S}(v)$.

$1$A leaf node $v_{leaf}$ has no child node, and a root node $v_{root}$ has no parent node.
decoding, the vector terminates after a maximum of $T_{\text{max}}$. Thus $V_{\text{root}}$ denotes the full binary decoding tree. The set of all leaf nodes is denoted by $U$, the index of a leaf $u$ is denoted by $l(u)$. The set of all information bits are denoted by $I$ and that of all frozen bits by $I^c$. We denote the information bit indices among the decoding tree by $I = \{l(u), u \in I\}$ Denote the frozen bit indices among the decoding tree by $I^c = \{l(u), u \in I^c\}$ Similar to [13], knowledge about decoded bits, e.g., in the form of log-likelihood ratio (LLR), is exchanged between neighboring nodes. The root node $v_{\text{root}}$ receives LLRs $\alpha_{\text{root}}$ directly from the channel output. As illustrated in Fig. 1(b), node $v$ receives an LLR vector $\alpha_v$ from its parent $p_v$, and feeds back an LLR vector $\beta_v$ to its parent $p_v$. The difference from [13] is that here $\beta_v$ is no longer the hard decisions (partial sums), but soft information. It is called response LLR [12]. If node $v$ is at stage $s$, vectors $\alpha_v$ and $\beta_v$ both have $2^s$ elements, respectively denoted by $\alpha_v^i$ and $\beta_v^i, i \in [0, 2^s - 1]$. According to [12], a node $v$ at stage $s$ passes information to its child nodes $\alpha_{v_l}$ and $\alpha_{v_r}$ as follows:

$$\begin{align}
\alpha_{v_l}^i &= \alpha_v^i \oplus (\beta_v^i + \alpha_v^{i + 2^s - 1}), i \in [0, \ldots, 2^s - 1 - 1] \\
\alpha_{v_r}^i &= (\alpha_v^i \oplus \beta_v^i) + \alpha_v^{i + 2^s - 1}, i \in [0, \ldots, 2^s - 1 - 1] 
\end{align}$$

(1)

The soft information feedback to its parent node is as follows:

$$\begin{align}
\beta_v^i &= \beta_{v_l}^i \oplus (\alpha_{v_l}^{i + 2^s - 1} + \beta_v^{i + 2^s - 1}), i \in [0, \ldots, 2^s - 1 - 1] \\
\beta_v^{i + 2^s - 1} &= (\beta_{v_l}^i \oplus \alpha_{v_l}^i) + \beta_{v_r}^i, i \in [0, \ldots, 2^s - 1 - 1] 
\end{align}$$

(2)

Unlike SC, the SCAN decoder runs iteratively, which means binary tree can be traversed several rounds. In the first iteration, we should initialize $\alpha_{v_{\text{root}}}$ as the channel output LLRs, and $\beta_v, v \in V_{\text{root}} \setminus U_{\text{root}}$ as all zeros. During the course of decoding, the vector $\beta_v$ will be updated by (2). The algorithm terminates after a maximum of $T_{\text{max}}$ iterations.

The soft messages $\beta_v, v \in U_{\text{root}}$ at leaf nodes do not change over time. They are always either $+\infty$ (for zero-valued frozen bits) or 0 (for information bits).

3In [12], there is a bit-reversal step before forwarding each LLR vector. But this step is unnecessary [14] and is removed in many other recent works.

III. Parity-Check Polar Codes

For PC-Polar codes, there are three types of bits, i.e., information bits, frozen bits and PC bits. We address three PC-Polar schemes in this paper:

- NR(new radio)-PC-Polar as described in “5G; NR; Multiplexing and channel coding” [9], where there are three PC bits.
- FC(full check)-PC-Polar as described in [4], where all non-information bits are treated as PC bits. This gives the best performance.
- MC(min-check)-PC-Polar as described in [7], where all non-information bits with specific row weight(s) are selected as PC bits. The row weight can be $w_{\min}$, the minimum row weight in the information set, or $2 \times w_{\min}$, the second lowest row weight in the information set.

The only difference among NR-PC-Polar, FC-PC-Polar and MC-PC-Polar is the PC bits number/positions. As said, NR-PC-Polar has a fixed number of PC bits. But for MC-PC-Polar, the PC bits number is controlled by a coefficient $\lambda$. The PC bit values are linear combinations of some preceding information bits. Such a pre-coding, or pre-transform, can improve the code minimum distance [6].

Algorithm 1 shows the encoding steps of a length-$N$ PC-Polar code, where $N = 2^n$ is the mother code length. Comparing with the original Polar encoder, it only has an additional step 4.

**Algorithm 1 Parity-check Polar encoding [4]**

1. Generate the information/frozen/PC bits positions.
2. Generate an all-zero sequence of length $N$.
3. Fill in the transmitted bit values at information positions, resulting in sequence $s$.
4. PC pre-coding, get the new sequence $q$.
5. Polar encoding, $q \times G$, where $G$ is a $N \times N$ Kronecker matrix.

In [4], a very simple way of PC pre-coding is proposed. The value of a PC bit $u \in \mathcal{P}$ is the sum of all its preceding information bits with a spacing of $L$ (or multiples of $L$). The PC constraints can be formulated as

$$s[i] = \sum_{j \in (i-j)\%L=0} s[j],$$

(3)

where $i$ is the index of the PC bit, and $j$ denotes the indices of all preceding information bits checked by the PC bit.

The PC pre-coding can be easily implemented by cyclic shift registers $\sigma$ of length $L$. The circuit is very simple, as shown in Fig. 2 where a register state is updated by

$$\sigma_x = \sigma_x \oplus s[i], x = i\%L, i < N.$$  

(4)

Traditionally, its decoder is modified from SC or SCL by adding a PC bit calculation module. During path extension

$^3$The notation of the coefficient is originally $\alpha$ in [4]. To avoid conflict with the soft input $\alpha$ in this paper, we use $\lambda$ to rename the coefficient.
and pruning, only the paths that satisfy the PC constraints are kept. The process resembles hard decoding where the PC bit values serve as “hard constraints” to select the valid paths.

IV. Parity Check Soft Cancellation

In this section, we introduce a novel soft cancellation decoding algorithm, namely PC-SCAN, that supports PC-Polar code. Unlike SC/SCL decoders, the proposed method treats PC bits as “soft constraints” to process the soft information generated by SCAN. Consequently, PC-SCAN can generate the soft outputs.

We still use $I$ and $F$ to denote the set of information bits and frozen bits, respectively. The set of PC bits is denoted by $P$. The frozen and PC bit indices among the decoding tree’s leaf nodes $U$ are respectively denoted by

$F = \{l(u), u \in F\}$,

$P = \{l(u), u \in P\}$.

By definition, $F \cup P = \tilde{I}^c$ and $F_v \cup P_v = I^c_v$.

According to (3), only bit positions with a spacing of $L$ (or multiples of $L$) will engage in the same PC constraint. Based on this observation, we can separate the leaf nodes in $I$ and $P$ into $L$ independent groups. Specifically, the $i$-th information/PC bit belongs to the $i\%L$-th group, where the group index takes value in $\{0, 1, \cdots, L - 1\}$. Since the nodes in the different groups are independent in terms of PC constraints, we call each group a “parity-check chain”.

To facilitate description, we specify the following notations. Denote by $I(u)$ the set of all information bits checked by a PC bits $u \in P$. The bit indices in a “checked information set” $I(u)$, $u \in P$ is denoted by

$I(u) = \{l(u'), u' \in I(u)\}$, for $u \in P$.

The union set of all checked information bits is denoted by

$\tilde{I} = \bigcup_{u \in P} I(u)$. \hspace{1cm} (5)

The bit indices in $\tilde{I}$ are denoted by

$\tilde{I} = \{l(u), u \in \tilde{I}\}$.

In principle, the method also supports any pre-transformed polar codes [6], while our focus is on PC-Polar codes [4] due to its simplicity and performance.

The remaining set of all unchecked information bits is denoted by

$\tilde{I}^c = I \setminus \tilde{I}$

The bit indices in $\tilde{I}^c$ are denoted by

$\tilde{I}^c = \{l(u), u \in \tilde{I}^c\}$.

Similarly, denote by $P(u)$ the set of all PC bits checking an information bits $u \in \tilde{I}$. The bit indices in a “checking PC set” $P(u)$, $u \in \tilde{I}$ is denoted by

$P(u) = \{l(u'), u' \in P(u)\}$, for $u \in \tilde{I}$.

The PC-SCAN algorithm first constructs a binary-tree in the recursive manner as in the original SCAN decoder, and then traverse the tree. It can be divided into two parts:

- Traverse the tree and apply (1) and (2) to calculate the input/output soft information of each node $v$ when entering/leaving the subtree $V_v$. When the tree traversal reaches a leaf node $u$, such that $u \notin \{P \cup \tilde{I}\}$, we directly obtain the soft feedback $\beta$ as follows

$\beta_u = \infty$, for $u \in F$. \hspace{1cm} (6)

$\beta_u = 0$, for $u \in \tilde{I}^c$. \hspace{1cm} (7)

- The second part calculates the soft feedback $\beta$ at leaf nodes such that $u \in \{P \cup \tilde{I}\}$. These are the information/PC bits that engage in PC constraints. The $L$ “parity-check chains” are modelled by $L$ Tanner graphs representing the parity-check relationships between information bits and PC bits. As will be described shortly, we use leaf nodes input $\alpha_u$ to calculate the soft feedback $\beta_u$.

Fig. 3 shows an example of the connections between the original SCAN decoding tree and parity check chains. In this example, the number of information bits (including CRC bits) is 32 and the code length is 64. Specifically, the reliability order is determined by polarization weight (PW) [15], and the number and positions of PC bits are determined as in PC-PC-Polar [4]. In the interest of space, the leaf nodes before the first information bit and after the last parity check bit are omitted, as they do not affect parity-check decoding. The length of cyclic shift registers is $L = 5$, resulting in five independent parity-check chains.

The set of bits in parity-check chain-0 is denoted by

$U(0) = \{u, u \in U \text{ and } l(u) \% 5 = 0\}$

According the Fig. 3, the indices of $u \in U(0)$ are grouped as follows

$\{0, 5, 10\} \subseteq F$

$\{20, 35, 40, 50\} \subseteq P$

$\{15, 25, 30, 45\} \subseteq \tilde{I}$

$\{55, 60\} \subseteq \tilde{I}^c$

The PC constraints are illustrated by a Tanner graph is plotted in Fig. 3(a). It includes all the checked information bits and PC bits in the PC chain-0 and model their parity-check relationship. All the checked information bits and PC
bits are regarded as variable nodes in the Tanner graph. The number of check nodes is equal to the number of PC bits in this PC-chain, as each check node represents a PC constraint.  

In this example, there are eight variable nodes and four check nodes.

Fig. 4(b) and Fig. 4(c) show how to update the variable nodes’ soft output $\beta$ with the soft input $\alpha$ from the SCAN decoder.

For a PC bit $u \in \mathcal{P}$, its soft output $\beta$ is calculated by

$$\beta_u = \lambda_P \times f(\alpha_{u_0} \oplus \alpha_{u_1} \oplus \cdots \oplus \alpha_{u_N}),$$

where $\{u_0', \cdots, u_N'\} = \mathcal{I}(u)$ for $u \in \mathcal{P}$.

For an information bit $u \in \mathcal{I}$, its soft output $\beta$ is

$$\beta_u = \sum_{u' \in \mathcal{P}(u)} \eta_{u'},$$

where $\eta_{u'}$ is contributed by its neighboring PC bit $u'$

$$\eta_{u'} = \lambda_{\mathcal{P}} \times (\alpha_{u'} \oplus \alpha_{u_0} \oplus \cdots \oplus \alpha_{u_N}),$$

where $\{u_0', \cdots, u_N'\} = \mathcal{I}(u') \setminus u$ for $u' \in \mathcal{P}(u)$.

Note that $\lambda_{\mathcal{P}}$ and $\lambda_{\mathcal{I}}$ are non-negative damping factors, which vary over code lengths and iterations. They are usually determined empirically.

In practice, the “box-plus” operation $\boxplus$ is implemented in an approximate but hardware-friendly way

$$x \boxplus y \approx f(x, y) = (1 - 2(sign(x) \oplus sign(y))) \times \min(abs(x), abs(y)),$$

where $sign(x)$ is the sign of $x$, $abs(x)$ is the absolute value of $x$, and $\min$ is minimum of input variables.

The $f$-function can also take multiple inputs

$$x_1 \boxplus \cdots \boxplus x_n \approx f(x_1, \cdots, x_n) = (1 - 2(sign(x_1) \oplus \cdots \oplus sign(x_n))) \times \min(abs(x_1), \cdots, abs(x_n)).$$

With the above simplification, (8) can be rewritten as

$$\beta_u = \lambda_{\mathcal{P}} \times f(\alpha_{u_0}, \alpha_{u_1}, \cdots, \alpha_{u_N}) \mid \{u_0', \cdots, u_N'\} = \mathcal{I}(u)$$

Likewise, (9) can be rewritten as

$$\beta_u = \sum_{u' \in \mathcal{P}(u)} \lambda_{\mathcal{I}} \times f(\alpha_{u'}, \alpha_{u_0}, \cdots, \alpha_{u_N}) \mid \{u_0', \cdots, u_N'\} = \mathcal{I}(u') \setminus u$$

PC SCAN follows a special scheduling that sequentially updates the soft information of leaf nodes. Specifically, the
Algorithm 2 Parity-check Soft Cancellation (PC-SCAN)

**Input:** $\mathcal{I}, \mathcal{F}, \mathcal{P}, \alpha_{\text{root}}, T_{\text{max}}$

**Output:** $\beta$

Derive $\tilde{I}$ according to (5);

**soft_cancellation_iterations**

for ($t = 0; t < T_{\text{max}}$; $t = t + 1$)

Call **recursive_decoder**($v_{\text{root}}, \alpha_{\text{root}}$);

**recursive_decoder**($v, \alpha_v$)

Calculate $\alpha_{v_{l}}, \alpha_{v_{r}}$ according to (1);

if ($v \notin \mathcal{U}$)

Call **recursive_decoder**($v_l, \alpha_{v_l}$);

Call **recursive_decoder**($v_r, \alpha_{v_r}$);

else

Call **leaf_decoder**($u_l, \alpha_{u_l}$);

Call **leaf_decoder**($u_r, \alpha_{u_r}$);

Calculate $\beta_u$ according to (2);

**leaf_decoder**($u, \alpha_u$)

if ($u \in \mathcal{P}$)

Calculate $\beta_u$ according to (11);

else if ($u \in \mathcal{I}$)

Calculate $\beta_u$ according to (12);

else if ($u \in \mathcal{F}$)

$\beta_u = \infty$;

else

$\beta_u = 0$;

The FER and BER performances under PC-SCAN is shown in Fig. 5 in which the code construction is given in Fig. 3. In this case, the FER of PC-SCAN is similar to that of SC after the first iteration, but the BER is better by 0.1dB. After a few iterations, the PC-SCAN decoder outperforms SC on both FER and BER. Besides, PC-SCAN can output soft decoding results.

V. CYCLIC-SHIFT-REGISTER-BASED HARDWARE

The leaf node decoder characterized by (6), (7), (11) and (12) can be further simplified to facilitate hardware implementation. While (11) and (12) support the soft decoding of any pre-transformed polar codes [6] (e.g., CA-Polar [3] and PAC-Polar [5]), they do not exploit the regular structure of PC-Polar [4] for further simplification.

We propose a cyclic-shift-register (CSR) based soft feedback generator. Compared with the general method of (11) and (12), it does not need to store the factor graph in Fig. 4 and all the variables. This is a huge complexity reduction given the irregularity of the graph and the number of variables therein.

The LLR calculation can also be simplified. For information bits, we found that the soft feedback can be set to zero. For PC bits, the damping factor $\lambda_P$ can be set to one to avoid multiplication operations. As will be shown, both simplifications incur only negligible performance loss.

The simplified soft feedback generation is

$$
\begin{cases}
\beta_u = \infty, & \text{for } u \in \mathcal{F} \\
\beta_u = f(\alpha_{u_l}, \alpha_{u_r}, \ldots, \alpha_{u_N}) | (u_l, u_r, \ldots, u_N) = \mathcal{I}(u), & \text{for } u \in \mathcal{P} \\
\beta_u = 0, & \text{for } u \in \mathcal{I} 
\end{cases}
$$

(13)

The simplified circuit is shown in Fig. 6 and described as follows. We set up an array of registers $\Delta$ of length $L$. Each register processes one parity-check chain. The registers only store the intermediate states that are necessary for generating the next soft feedback.

Before each iteration, all register states are reset to zero. As the registers shift, the $f$-function in (13) can be calculated on the fly. Upon decoding an information bit $u \in \mathcal{I}$, the input soft LLR $\alpha_u$ is accumulated into the register $\Delta$ as follows:

$$
\Delta_x = f(\Delta_x, \alpha_x), \quad u \in \mathcal{I}, \quad x = l(u)\%L. \quad (14)
$$

Upon decoding a PC bit $u$, the soft feedback $\beta_u$ can be immediately obtained as:

$$
\beta_u = \Delta_x, \quad u \in \mathcal{P}, \quad x = l(u)\%L. \quad (15)
$$

![Fig. 6. Soft feedback generator for PC-SCAN leaf decoder](image-url)
Therefore, to implement PC-SCAN, we only need a small additional circuit on top of SCAN, thanks to the structural regularity of PC-Polar [4]. We name this optimized method CSR-SCAN decoder. The circuit comprises only an $f$-function, defined in (10), and a cyclic buffer of length $L$. As shown in Fig. 6 it is very similar to the PC pre-coding circuit in Fig. 2. Both are very hardware friendly and highly efficient in terms of area, power and latency.

VI. PERFORMANCES

We simulate the performances of PC-SCAN decoder using the best damping factor $\tilde{\lambda}_{\text{best}}$ and CSR-SCAN decoder within all the PC-types introduced in section III. The results in Fig. 7, Fig. 8 and Fig. 9 show such simplifications incur minimum performance loss. After the first iteration, the optimized circuit produces the same performance as the original one. With more iterations, a little performance loss can be observed. For all simulated cases, the FER loss is within 0.05dB.

The damping factor is obtained empirically through simulations.
We also compare the performance between SC decoder and CSR-SCAN decoder. We show the FER and BER performance comparison in the Fig. 10 ~ Fig. 14. We find that in the cases of shorter code length ($N=128$), the FER of CSR-SCAN after the first iteration is 0.1 dB inferior to that of SC decoder at $FER = 10^{-3}$, while the BER is 0.1 dB better. After the second iteration, both FER and BER of CSR-SCAN are better than those of SC decoder. In the cases of long codes ($N=512$), CSR-SCAN’s slope at the waterfall region is better than that of SC decoder, and the performances after the second iteration are similar to that of SC decoder when $FER = 10^{-3}$. The NR-PC-Polar has 3 PC-bits, and exhibits less gain from the 2-rd to the 4-th iteration. The FER of CSR-SCAN’s second iteration is better than that of SC-decoder by 0.1 dB.

Fig. 10. FC-PC-Polar, $N=128$, $K=[32, 64, 96]$, $\alpha=1.0$, performances of SC decoder and CSR-SCAN decoder.

Fig. 11. MC-PC-Polar, $N=128$, $K=[32, 64, 96]$, $\alpha=1.0$, performances of SC decoder and CSR-SCAN decoder.

Fig. 12. FC-PC-Polar, $N=512$, $K=[128, 256, 384]$, $\alpha=1.5$, performances of SC decoder and CSR-SCAN decoder.

VII. CONCLUSION

In this paper, we propose a soft-output PC-SCAN decoder for pre-transformed polar codes including CA-Polar, PC-Polar and PAC-Polar. The proposed algorithm treats PC bits as “soft constraints” to process the soft information generated by SCAN. An additional factor graph is formulated to process these constraints. According to the factor graph,
four types of leaf nodes are defined, i.e., frozen/PC/checked information/unchecked information, and decoded accordingly. With focus on the hardware implementation, a cyclic-shift-register-based optimization is proposed to dramatically reduce the hardware overhead named CSR-SCAN decoder. Finally, performance simulations show both the gain from PC bits and the insignificant performance loss due to CSR-SCAN decoder.

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