E-band broadband digital controlled phase-inverting variable gain amplifier in 65-nm CMOS

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This letter reports an E-band phase-inverting variable gain amplifier in 65-nm complementary metal-oxide-semiconductor (CMOS) technology. A fractional bit based structure with replica cells is proposed to minimise the phase error and ensure the tuning accuracy between different gain modes. This structure has 9-bits digital-controlled amplifiers and allows 180° phase shifting. The implemented phase-inverting variable gain amplifier achieves 16 dB tuning range and 0.5 dB tuning step at 80 GHz. The root mean square (RMS) gain and phase errors across 3 dB bandwidth (i.e. 72–87 GHz) are less than 0.3 dB and 2.7°, respectively. The phase-inverting variable gain amplifier consumes 8 mW at 1 V supply voltage.

Introduction: Phased-array technique is a key method to improve link robustness and effective isotropic radiated power for millimeter-wave (mm-Wave) wireless systems [1]. In a phased-array transceiver, variable gain amplifier (VGA) controls the gain of each channel and reduces side-lobes [2]. An important goal of the VGA design is to minimise the phase error between different gain stages and ensure accurate tuning steps which will be seriously affected by the input and output impedances in a mm-Wave phased-array transceiver. Besides, the increasing of frequency results in higher path loss and lower power gain [3]. Therefore, the trade-off between step accuracy, tuning range, maximum gain and power consumption has also become challenge. In general, VGAs at mm-Wave frequencies usually achieve gain tuning by changing the transconductance of the input stage and ensure the phase inmutability by applying parasitic capacitance elimination technologies.

The works in [4] present a phase-inverting variable gain amplifier (PIVGA) in 65-nm CMOS technology. A replica transistor is introduced to compensate the output parasitics. However, the PIVGA in [4] has a limited tuning range and a changeable output impedance. A common source structure in [5] solves the above problems and ensures the phase invariance by using replica differential pairs with selectable polarities. Nevertheless, it shows relatively low accuracy and power gain.

This letter introduces a parallel replica array of different transistor sizes to increase the accuracy and improve the power gain. Besides, the proposed core structure implements digital-controlled scheme and achieves two tuning modes with 180° phase shifting, which brings linear-in-decibel gain variation characteristics and benefits of modular design methods. Therefore, the PIVGA can reduce the required phase range of the cascade phase shifters from 360° to 180°, which decreases system power consumption and improves bandwidth [6]. Besides, the output impedance and phase error between different gain stages keep constant which brings convenience for broadband matching. Fabricated in 65-nm CMOS, the PIVGA can achieve 0.5 dB step and 16 dB tuning range with 4.5 dB power gain at 80 GHz.

Topology of the phase-inverting variable gain amplifier: The architecture of the PIVGA is shown in Figure 1. It is composed of nine digital controlled cells with different transistor sizes. Six of them are integral-bit cells and the other three are proposed fractional-bit cells. Each fractional-bit structure consists of two integral-bit cells and each integral-bit cell consists of two differential common-source amplifiers which are controlled by digital signals with opposite polarity. With a fully symmetric design, the proposed PIVGA has an excellent balance.

The PIVGA realises gain tuning by the parallel superposition of the output signals from different cells. Therefore, the transistor size in each cell will determine the tuning range and accuracy. Since transistors of small size can achieve relatively high gain and small step, a transistor with the finger width of 0.6 μm is used as the unit cell.

Figure 1(b) shows the normalised unit of the integral-bit cells. The six integral-bit cells can afford relatively large transistor widths to guarantee a wide gain-tuning range. Since the digital-control logics of two differential pairs are opposite, there is always one differential pair working at the amplifying state and the other at the off state. The output current is either (I_m – I_O) or (–I_m – I_O). The negative sign represents the opposite phase. Therefore, 180° phase shift can also be realised. Because the size of the transistors in different cells increases in binary, the output current of each cell is: 2^n(I_m – I_O) or –2^n(I_m – I_O) and the six parallel integral-bit cells in the blue box of Figure 1(a) can achieve a tuning range from –2^n(I_m – I_O) to 2^n(I_m – I_O) (i.e. ±2^n, ±2^n, ±2^n, ±2^n, ±2^n) (I_m – I_O)) with a tuning step of 2(I_m – I_O). It shows that the tuning step is limited by the minimum transistor width of the normalised unit. Therefore, a fractional bit based structure with replica arrays is proposed in this letter to realise an equivalent transistor width which is smaller than 1 × 0.6 μm.

Fractional bit based structure with replica cells: Given that the increase of power gain in decibels is not linearly correlated to the change of the equivalent transistor width, the tuning step brought by changing the polarity of one cell will keep decreasing as the power gain increases. Therefore, smaller transistor widths should be applied at the state of low power gain. Considering the output current of the cell whose width is 1 × 0.6 μm as the normalisation criterion, three fractional-bit cells (i.e. two 0.25 × cells and one 0.5 × cell) which use replica arrays are introduced to ensure an accurate 0.5 dB step between all 64 states.

To achieve a 0.5 dB tuning step, the transistor width at high gain mode should be 1 of 34 larger than that at the adjacent low gain mode. It means that the required transistor width in low gain modes will be smaller than that in high gain modes. Therefore, if the tuning step at the minimum gain mode is accurate enough, the accuracy at other modes can be guaranteed. To achieve 64 states, at least 6 bits are required. As is shown in Figure 1(a), the 6 control bits of the integral-bit cells are 000101 at the minimum gain mode. The equivalent width is 5.4 (i.e. 19.2 – 9.6 – 4.8 – 2.4 – 1.2 – 0.6) μm. Therefore, transistors with the finger width of 0.15 (i.e. 5.4/34 μm) are needed to achieve an accurate 0.5 dB tuning step.

The fractional-bit cell of 1 × 0.15 μm (i.e. 0.25×) is shown in Figure 2. It consists of an integral-bit cell G1 and a parallel replica cell G2 which have different transistor widths (i.e. 1 × 0.6 μm and 1 × 0.75 μm) and opposite digital-control signals. If G1 outputs inverted signal, the output current of G2 will be –(I_m – I_O) and the output current of G2 will be 1.25(I_m – I_O). Considering the fractional-bit cell is the parallel superposition of G1 and G2, the output current of the fractional-bit cell will be 0.25(I_m – I_O). Therefore, the fractional-bit cell can realise the same fine-tuning step as that brought by the cell with transistors of 1 ×
0.15 μm. Besides, $G_1$ and $G_2$ are controlled by a pair of complementary digital signals. By employing two inverters, four differential common-source amplifiers in the fractional-bit cell can be controlled by one-bit digital signal. It means that this structure can minimise the digital-control bits of the PIVGA and restrict the output of fractional-bit cells to only two modes with opposite phases. Note that the proposed fractional-bit structures need more transistors than integral-bit cells and this may lead to larger active area. However, compared to commonly used cascode structures in [1,4,6], the proposed bit-based common-source structures do not need extra coupling inductances to resonate with the parasitic capacitances between two stages and the required area of spiral inductors in 65-nm CMOS is much larger than that increased by replica cells. Therefore, this PIVGA still has smaller chip area than traditional cascode structures overall.

Figure 3 shows the minimum tuning steps at different gain modes with or without fractional-bit cells. Under the same maximum transistor size and power consumption, it is obvious that the PIVGA with fractional-bit cells can achieve much smaller tuning steps at different gain modes. Besides, given that the transistor widths of three fractional-bit cells are very small, the PIVGA with fractional-bit cells can realise 4.3 dB maximum gain which is almost the same as that without fractional-bit cells.

**Phase-invariant and wideband matching technique:** Figure 4(a) shows the equivalent schematic of an integral-bit cell with parasitics. This structure has the same output impedance and phase characteristic in all gain modes. In Figure 4(a), no matter which differential pair is working, the parasitic capacitance from the output port to ground is $2C_{gd, on} + 2C_{gd, off}$ which makes the PIVGA have the same phase characteristic at all gain modes. Similarly, since two differential pairs have the same transistor width and opposite phases, the output impedance observed from the output port is always has a constant value of $R_{out, on}/R_{out, off}$.

As is shown in Figure 4(b), the output impedance of the integral-bit cell can be regarded as a parallel RC model and the values of $R_S$ and $C_1$ are constant. Therefore, the same matching network can be applied for all gain modes. A two-pole transformer matching network is employed to realise the wideband matching [7] and an equivalent T-type network is applied to simplify the design. However, a typical transistor has an output impedance of $R_S$ much larger than 50 Ω, which will bring a low $k$ value and then increase the loss. In this letter, the PIVGA has nine parallel cells and each cell has at least four parallel transistors. Therefore, it can decrease the output impedance which increases the coupling factor $k$ to ensure wideband matching.

**Measurement results:** The differential PIVGA has been fabricated in 65-nm CMOS technology and tested on a high-frequency probe station. Figure 5 shows the die photograph of the PIVGA. It occupies an area of 0.429 mm² (i.e. including DC and radio frequency pads) while the active area of the PIVGA is only 0.0162 mm² (i.e. 65 μm × 250 μm).

Figure 6 shows the measured phases at all gain-tuning modes. The measured $S$-parameters of the 64 gain-tuning modes are plotted in Figure 7. The maximum gain is 4.5 dB when the control bits are 11111010 (i.e. at the positive phase mode) or 00000010 (i.e. at the negative phase mode). This design is centred at 80 GHz with $-1$ dB bandwidth from 76 to 84 GHz and $-3$ dB bandwidth from 72 to 87 GHz. The variable gains of all gain modes are plotted across 72 to 87 GHz in Figure 7(a) and (b). The tuning range is from $-11.5$ to $4.5$ dB with accurate phase selection.
This work presents a wideband digital controlled PIVGA and analyses the mechanism of phase-invariant and gain-tuning technique. Three fractional-bit cells with replica arrays are introduced to minimise the tuning step and ensure the maximum gain. Besides, a compact and symmetric layout floor-plan is utilised to reduce the losses and parasitics. Fabricated in 65-nm CMOS technology, the proposed PIVGA with 180° phase variation achieves a measured tuning range of 16 dB and an accurate 0.5 dB step. The maximum gain is 4.5 dB at 80 GHz and the RMS gain error is <0.3 dB across 3 dB bandwidth (i.e. 72–87 GHz). The RMS phase errors are <2.7° and <1.5° at two-phase modes, respectively. The measured power consumption is 8 mW at 1 V supply voltage.

**Table 1. Performance comparison**

| Reference | Technology | Bandwidth (GHz) | Power gain (dB) | Tuning range (dB) | Resolution (dB) | Phase error (°) | Supply voltage (V) | DC power consumption (mW) | Chip area (mm²) |
|-----------|------------|----------------|----------------|-------------------|----------------|----------------|------------------|------------------------|----------------|
| [6]       | 65 nm CMOS | 53–63          | 6              | 15                | 1              | <3             | 1                | 25                     | 0.116          |
| [8]       | 65 nm CMOS | 57–64          | 7              | 22                | 2.5            | <7.5           | 1                | 9                      | N/A            |
| [9]       | 65 nm RFCMOS | 58–72        | 21.8           | 9                 | Continuous     | N/A            | 1                | 36                     | 0.4875         |
| This work | 65 nm CMOS | 72–87          | 4.5            | 16                | 0.5            | <2.7           | 1                | 8                      | 0.0162         |

Besides, the proposed PIVGA can realise wider tuning range, more accurate tuning step, lower power consumption and smaller chip area.

**Conclusion:** This work presents a wideband digital controlled PIVGA and analyses the mechanism of phase-invariant and gain-tuning technique. Three fractional-bit cells with replica arrays are introduced to minimise the tuning step and ensure the maximum gain. Besides, a compact and symmetric layout floor-plan is utilised to reduce the losses and parasitics. Fabricated in 65-nm CMOS technology, the proposed PIVGA with 180° phase variation achieves a measured tuning range of 16 dB and an accurate 0.5 dB step. The maximum gain is 4.5 dB at 80 GHz and the RMS gain error is <0.3 dB across 3 dB bandwidth (i.e. 72–87 GHz). The RMS phase errors are <2.7° and <1.5° at two-phase modes, respectively. The measured power consumption is 8 mW at 1 V supply voltage.

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**Fig. 7** Measured S-parameters at different gain modes: (a) measured gains at positive phase modes, (b) measured gains at negative phase modes, (c) measured input and output return losses at positive phase modes, and (d) measured input and output return losses at negative phase modes.

**Fig. 8** Measured RMS error versus frequency at different phase modes: (a) RMS gain error and (b) RMS phase error.

0.5 dB steps at both positive and negative phase modes. Figure 7(c) and (d) shows the input and output return losses (i.e. $S_{11}$ and $S_{22}$) of two different phase states, respectively. From 82 to 87 GHz, the $S_{11}$ and $S_{22}$ are less than −10 dB, while the $S_{11}$ and $S_{22}$ are less than −4 dB from 72 to 82 GHz. Due to the differential and symmetric design, each gain-tuning mode has the same output impedances and parasitics, leading to the result that both $S_{11}$ and $S_{22}$ are not sensitive to the change of gain modes. This feature brings superiority to optimise matching networks. Besides, it prevents the PIVGA from affecting the cascaded circuits in the signal chain of the complete transceiver.

The RMS gain error shown in Figure 8(a) is less than 0.4 dB in the −3 dB bandwidth. The value is less than 0.2 dB from 73 to 84 GHz and less than 0.1 dB from 78 to 82 GHz. As shown in Figure 8(b), the RMS phase error is less than 1.5° from 72 to 87 GHz at the positive phase mode and the value is less than 2.7° from 72 to 87 GHz at the negative phase mode. The value '1' (i.e. blue lines) or '0' (i.e. red lines) of the digital signal $F_{cont}$ in the 32 × cell determines the phase states. Note that no calibration is applied during all the measurements.

Table 1 compares the performance of the PIVGA with recent topologies fabricated in 65-nm CMOS. This structure has broader bandwidth than [6,8] because of the constant input and output impedences and the utilisation of transformer matching networks. Compared to [8,9], this work can achieve 180° phase inversion and has lower phase error due to the application of superimposed bipolar differential cells.

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**Table 1. Performance comparison**

| Reference | Technology | Bandwidth (GHz) | Power gain (dB) | Tuning range (dB) | Resolution (dB) | Phase error (°) | Supply voltage (V) | DC power consumption (mW) | Chip area (mm²) |
|-----------|------------|----------------|----------------|-------------------|----------------|----------------|------------------|------------------------|----------------|
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| This work | 65 nm CMOS | 72–87          | 4.5            | 16                | 0.5            | <2.7           | 1                | 8                      | 0.0162         |
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