Efficient Implementation of Multi-Channel Convolution in Monolithic 3D ReRAM Crossbar

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Abstract—Convolutional neural networks (CNNs) demonstrate promising accuracy in a wide range of applications. Among all layers in CNNs, convolution layers are the most computation-intensive and consume the most energy. As the maturity of device and fabrication technology, 3D resistive random access memory (ReRAM) receives substantial attention for accelerating large vector-matrix multiplication and convolution due to its high parallelism and energy efficiency benefits. However, implementing multi-channel convolution naively in 3D ReRAM will either produce incorrect results or exploit only partial parallelism of 3D ReRAM. In this paper, we propose a 3D ReRAM-based convolution accelerator architecture, which efficiently maps multi-channel convolution to monolithic 3D ReRAM. Our design has two key principles. First, we exploit the intertwined structure of 3D ReRAM to implement multi-channel convolution by using a state-of-the-art convolution algorithm. Second, we propose a new approach to efficiently implement negative weights by separating them from non-negative weights using configurable interconnects. Our evaluation demonstrates that our mapping scheme in 16-layer 3D ReRAM achieves a speedup of 5.79×, 927.81×, and 36.8× compared with a custom 2D ReRAM baseline and state-of-the-art CPU and GPU. Our design also reduces energy consumption by 2.12×, 1802.64×, and 114.1× compared with the same baseline.

Index Terms—convolutional neural network (CNN), 3D resistive random access memory (ReRAM), mapping, accelerator.

I. INTRODUCTION

Deep learning algorithms are adopted in a wide range of systems, whether small edge devices or large data centers [1]. Convolutional neural networks (CNNs) have revolutionized deep learning applications by achieving unprecedented accuracy for object detection and image classification. However, CNNs are time-consuming and power-hungry during the computation process. For example, AlexNet [16] performs 10^9 operations for a single image input without batching [4]. Convolution layers are the most computation-demanding in CNNs. It is estimated that the convolution layers of VGG-16 [14] take 67.8% of the total execution time [19].

Recently, resistive random access memory (ReRAM) is becoming an attractive technology solution for accelerating convolution layers, due to its promising parallelism and energy efficiency benefits. ReRAM is a novel memory technology which consists of a crossbar structure of memristors. It combines storage and computation together and accelerates deep neural networks in the analog domain. Recently, several ReRAM-based processing-in-memory (PIM) accelerators have been proposed such as PRIME [2], ISAAC [3], and PipeLayer [4]. These architectures all focused on efficiently architectsing 2D ReRAM for CNN applications. However, monolithic 3D integration technology has grown rapidly. Compared with 2D ReRAM, 3D ReRAM can provide more parallelism, take less area, produce less noise, and consume less energy in computations [7]. Monolithic 3D ReRAM can be either vertically integrated or horizontally integrated. In our work, we focus on mapping multi-channel convolution to horizontally integrated monolithic 3D ReRAM because it can be more reliably fabricated [7], as shown in Fig. 1.

Nonetheless, leveraging 3D ReRAM for processing multi-channel convolution in parallel still faces three challenges. First, even though previous works have successfully designed several accelerators which used 2D ReRAM to process multi-channel convolution, simply extending 2D ReRAM to 3D ReRAM without any modification will produce incorrect results due to the stacked structure. Second, even multi-channel convolution can be correctly implemented, a naive implementation will exploit only partial parallelism of 3D ReRAM. Third, kernels in multi-channel convolution, like edge detection filters, sometimes has negative weights. An efficient way to implement negative weights in 3D ReRAM is necessary.

Our goal in this paper is to efficiently map multi-channel convolution to horizontally integrated monolithic 3D ReRAM.
In order to achieve our goal, we propose an convolution accelerator with two design principles. First, to solve challenges 1 and 2, we for the first time exploit the massive parallelism of 3D ReRAM to accelerate CNNs by using a newly proposed algorithm to implement multi-channel convolution [9]. Second, to solve challenge 3, we propose a new approach to efficiently implement negative weights in 3D ReRAM using configurable interconnects.

II. BACKGROUND

In this section, we describe ReRAM background and motivate our design.

A. Convolutional Neural Networks

CNNs are the heart of current deep learning applications. A typical CNN consists of multiple layers, such as convolution layers, pooling layers, and fully-connected layers, as shown in Fig. 2.

B. Memristor and 2D ReRAM

2D ReRAM is a grid structure consisting of multiple memristors, as shown in Fig. 3. Each ReRAM cell contains one memristor. Such design can exploit the analog characteristics of ReRAM to perform fast and energy-efficient matrix multiplication and convolution. Vector-matrix multiplication can be easily calculated using ReRAM, because of two basic electrical theorems, Ohm’s law and Kirchhoff’s current law. Ohm’s law states that the current through a resistor is equal to the voltage across the resistor divided by the resistance of the resistor \(I = V / R\), which is also equal to the voltage across the resistor multiplied by the conductance of the resistor \(I = VG\). This law makes performing analog floating-point multiplication possible. Kirchhoff’s current law states that the total current output is equal to the sum of all input current for a node in the circuit. This law makes performing analog floating-point addition possible. Vector-matrix multiplication can be mapped to ReRAM in the following three steps, as shown in Fig. 3. First, the digital input is converted to analog signals by digital-to-analog converters (DACs) and then mapped to the voltage on horizontal bit lines (WLs); Second, the weight matrix is quantized and then mapped to the conductance of memristors; Third, the output signals are read from the current on the vertical bit lines (BLs) and then converted to digital output by analog-to-digital converters (ADCs).

C. Monolithic 3D ReRAM

Monolithic 3D ReRAM integrates ReRAM cells in either a vertical or a horizontal manner. For example, B. Chakrabarti et al. developed an 8-layer vertically integrated monolithic 3D ReRAM [6], while M. Mao et al. designed a horizontally integrated monolithic 3D ReRAM [7]. Horizontally integrated monolithic 3D ReRAM has more reliable manufacturing technology [7]. An example of horizontal 3D ReRAM is shown in Fig. 1. Its intertwined structure ensures that WLs and BLs between adjacent layers are shared. The 4-layer 3D ReRAM has three voltage planes with three WLs on each plane. It also has two current planes with three BLs on each plane. Different layers of memristors have different colors.

III. PROPOSED APPROACH

In order to exploit the massive parallelism provided by monolithic 3D ReRAM to implement the computation-intensive multi-channel convolution layers in CNNs, we propose a convolution accelerator which uses the same structure for multi-channel convolution.

A. Architecture Design

We employ an optimized architecture for accelerating CNNs, as shown in Fig. 4. The architecture is composed of multiple tiles of ReRAM cells connected by an on-chip mesh. Each tile has an eDRAM buffer, a shared bus, a controller, and multiple ReRAM-based processing engines. We substitute the conventional 2D ReRAM crossbar with monolithic 3D ReRAM crossbar. Each processing engine communicates with the buffer via the shared bus. The controller...
B. Convolution Algorithm

Common 2D convolution algorithms include single kernel single channel (SKSC), single kernel multiple channel (SKMC), and multiple kernel multiple channel (MKMC). MKMC is widely used in many CNN architectures. In order to present how MKMC without batching works, we define image to be \( I \) and kernel to be \( K \). \( I \) is a 3D matrix with dimensions \( c(\text{channel}) \times h(\text{height}) \times w(\text{width}) \). \( K \) is a 4D matrix with dimensions \( n(\text{kernel}) \times c(\text{channel}) \times l(\text{length}) \times l(\text{length}) \).

SKSC is a simple convolution between one channel of the image and one channel of one kernel, which is defined as

\[
SKSC(I, K_{j,i}) = conv(I_i, K_{j,i})
\]

where \( i \in [0, c) \) and \( j \in [0, n) \). SKMC is calculated by summing the result of SKSC of every corresponding channel of the image and one kernel, which is defined as

\[
SKMC(I, K) = \sum_{i=0}^{c-1} conv(I_i, K_{j,i})
\]

where \( j \in [0, n) \). MKMC is computed by concatenating the result of SKMC of every corresponding channel of the image and every kernel, which is defined as

\[
MKMC(I, K) = SKMC(I, K_0) \cdots \cdot SKMC(I, K_{n-1})
\]

where \( \mid \) represents concatenation.

Traditionally, MKMC is calculated by unrolling each kernel into a row vector in the kernel matrix and corresponding image pixels to a column vector in the image matrix. Then multiplying the two matrices gives the result. However, this approach is not suitable for mapping to 3D ReRAM because the property in equation (1) cannot be easily applied. Recently, new approaches to compute MKMC have been proposed \[9\]. One of them is to compute the \( n^2 \) convolution using \( n^2 \) different \( 1 \times 1 \) convolutions. It unrolls the corresponding \( 1 \times 1 \) weights in all channels within one kernel into a row vector in the kernel matrix and the corresponding \( 1 \times 1 \) pixels in all channels within the image into a column vector. After multiplying the two matrices, there are \( l^2 \) submatrices of size \( n \times (h \times w) \). We need to superimpose the submatrices together into one matrix and reshape it to be \( h \times w \times n \), as shown in Fig. 5. This algorithm is suitable for mapping to 3D ReRAM. In particular, the superimposition step can be efficiently implemented using the property in equation (1).

C. Efficient Mapping of Convolution to 3D ReRAM

We design an efficient mapping of the algorithm to 3D ReRAM. We start with mapping the \( n \times c \times l \times l \) kernel to 3D ReRAM. We employ \( c \) WLs in each voltage plane and \( n \) BLs in each voltage plane. Since we use 3D ReRAM with shared WLs and BLs, the number of layers has to be an even number for reconfiguration. If \( l^2 \) is an even number, we use \( l^2 \) layers of memristors, \( l^2 + 1 \) voltage planes, and \( l^2 \) current planes. If \( l^2 \) is an odd number, we use \( l^2 + 1 \) layers of memristors, \( \frac{l^2+1}{2} \) voltage planes, and \( \frac{l^2+1}{2} \) current planes. Note when \( l^2 \) is odd, one layer of memristors is not in use (dummy layer). We need to either set the resistance of the memristors close to zero or set the voltage on the relevant WL to zero to ensure correct output current. For each voltage plane, \( c \) WLs correspond to one column of the image matrix. WLs from different voltage planes but on the same vertical plane have the same voltage to maximize parallelism of the 3D structure. One column of the image matrix can be fed into 3D ReRAM at one logical cycle. It takes \( h \times w \) logical cycles to pass the \( c \times h \times w \) image into 3D ReRAM. For each current plane, \( n \) BLs correspond to \( n \) kernels in the output. BLs from different current planes but on the same vertical plane are accumulated simultaneously to implement the superimposition. 3D ReRAM produces \( n \) sums at one logical cycle. After \( h \times w \) logical cycles, it will produce the \( n \times h \times w \) output.

In addition, we present a new approach to implement

![Fig. 4. Overall architecture.](image)

![Fig. 5. Computation process of MKMC.](image)

![Fig. 6. Flow diagram of the full mapping scheme.](image)
negative weights using configurable interconnects. The full mapping scheme is summarized in the flow diagram in Fig. 6. First, we scan each of $n$ kernels and count the number of negative weights and non-negative weights. Note there is a voltage plane that separates negative weights from non-negative weights for each kernel. Second, negative weights are mapped to the lower layers below the voltage separation plane and non-negative weights are mapped to the upper layers above the voltage separation plane. Third, interconnects are configured for negative weights and non-negative weights accordingly. Fourth, negative weights and non-negative weights are accumulated separately and then fed into peripheral circuits which are used to read the difference between the two accumulated currents.

D. Putting It All Together: An Example

We demonstrate our approach using an example of applying an edge detection filter to an image with three channels. The filter has two kernels each with three channels of the same value, as shown in Fig. 7(a)-(b). We use a 10-layer 3D ReRAM (0 to 9) with six voltage planes (0 to 5) and five current planes (0 to 4). For kernel 0, we set the voltage on voltage plane 5 to zero because we do not use memristors in layer 9. We use four layers (0 to 3) for negative weights and five layers (4 to 8) for non-negative weights. The separation plane is voltage plane 2. After configuring interconnects, we accumulate two current planes (0 to 1) for negative weights as $I_n$ and three current planes (2 to 4) for non-negative weights as $I_p$, as shown in Fig. 7(c). For kernel 1, we set the voltage on voltage plane 0 to zero because we do not use memristors in layer 0. We use one layer (1) for negative weights and eight layers (2 to 9) for non-negative weights. The separation plane is voltage plane 1. After configuring interconnects, we accumulate one current plane (0) for negative weights as $I_n$ and four current planes (1 to 4) for non-negative weights as $I_p$, as shown in Fig. 7(d). In order to read the current difference, we slightly modify the typical inverting operational amplifier circuit, as shown in Fig. 7(e). Measuring the output current $I_2$ gives the difference between $I_p$ and $I_n$.

We prove the correctness of the circuit in Fig. 7(e). Since the current into the negative input of the op amp is zero, Kirchhoff’s current law gives $I_0 = I_n$. Then Ohm’s law states $V_0 = I_nR_0$. Using Kirchhoff’s voltage law, $V_1 = -I_nR_0$ holds, and then $I_1 = -I_n$ is true according to Ohm’s law again. Finally, we reach the conclusion that $I_2 = I_p - I_n$ after applying Kirchhoff’s current law again.

IV. Evaluation

In this section, we evaluate the performance and energy consumption of our proposed design.

We first compare the performance of 2D ReRAM with other popular memory technologies such as SRAM, eDRAM, PCM, and STT-RAM. We use DESTINY tool [10] to simulate 1 GB of 3D ReRAM using 32 nm technology. We use the read/write latency and energy of 2-layer 3D ReRAM as baseline and normalize 3D ReRAM with more layers to it, as shown in Fig. 8. We observe that for the same memory capacity, as the number of layers increases, read/write energy and read/write latency also increase. In our experiment, we use profiling results to optimize the number of layers in 3D ReRAM to balance between more parallelism versus higher read/write latency and energy.

TABLE I: Parameters of several memory types.

| Memory Type | Write Energy $(nJ)$ | Read Energy $(nJ)$ | Write Latency $(ns)$ | Read Latency $(ns)$ |
|-------------|-------------------|------------------|---------------------|--------------------|
| ReRAM       | 1.907             | 1.623            | 15.274              | 13.948             |
| eDRAM       | 3.407             | 3.324            | 34.207              | 66.661             |
| SRAM        | 6.687             | 6.688            | 144.556             | 279.546            |
| STT-RAM     | 2.102             | 1.975            | 13.469              | 18.06              |

A. Experiment Setup

Configuration and Simulation. In our experiment, we use 3D ReRAM with 16 layers for two reasons. First, 16 layers are enough to handle a typical kernel size $3 \times 3$. Second, it provides the optimal latency based on the extended report of DESTINY [12]. We sacrifice the parallelism to support larger kernels, such as $5 \times 5$. If we had smaller number of layers such as 10 or 12, we must repeat the computation more than twice to support the larger kernel. For ReRAM crossbars, we use DESTINY [10] to measure the execution time and energy consumption. For interconnects, we model with CACTI.
ReRAM achieves the same inference accuracy as our baseline.

Workload and Baseline. We benchmark several selected MKMC layers from the inference phase of three popular CNN architectures, VGG-16 [14], GoogLeNet [15], and AlexNet [16]. All three architectures are trained in Tensorflow framework [18] and evaluated on the widely used ImageNet database [20]. For our baseline, we do not use experimental results from previous works for two reasons. First, it is unfair to compare the performance with different design focuses. Second, it is difficult to obtain all the detailed design parameters from previous papers.

Instead, we compare the execution time and energy consumption of our design with a custom 2D ReRAM baseline, a CPU platform, and a GPU platform. We implement MKMC using this algorithm [9] for the CPU and GPU platform. For the custom 2D ReRAM baseline, we assume 2D ReRAM crossbars in the same architecture with same amount of memristors as our proposed 3D ReRAM design for fair comparison. For the CPU platform, we choose Intel Core i7-5700HQ processor, which has 4 cores, 6 MB cache, and operates around 2.7 GHz. For the GPU platform, we choose NVIDIA GeForce GTX 1080 Ti, which has 3584 CUDA cores, 11 GB GDDR5X graphics memory, and operates around 1582 MHz. The CPU and GPU execution time is measured within the framework. The CPU energy consumption is estimated by Intel Product Specifications [17] and the GPU energy consumption is estimated by NVIDIA System Management Interface (nvidia-smi).

C. Energy Results

Fig. 9(b) compares the energy consumption of 3D ReRAM with a custom 2D ReRAM baseline, a CPU platform, and a GPU platform. We use the CPU energy consumption as the baseline and normalize GPU, 2D ReRAM, and 3D ReRAM to it. The energy saving of 3D ReRAM compared with 2D ReRAM, CPU, and GPU are 2.12×, 1802.64×, and 114.1×, respectively. 3D ReRAM consumes less energy compared to 2D ReRAM because shared WLs and BLs reduce roughly half digital-to-analog and analog-to-digital computations. It also benefits from less complex interconnects. 3D ReRAM can achieve huge energy reduction compared to CPU and GPU due to two reasons. First, 3D ReRAM uses the analog properties to compute vector-matrix multiplication, which is more energy efficient than most digital computations. Second, 3D ReRAM passes data through stacked layers, which is shorter than the data movement between processing units and memory hierarchy in most digital processors.

V. Related Works

Recently, several architectures have been proposed to use ReRAM to accelerate CNN applications. PRIME [2], ISAAC [3], and PipeLayer [4] demonstrate the promising performance gain when off-loading the CNN computation to 2D ReRAM crossbar. Our paper contributes in similar but yet different aspects. First, 2D ReRAM has limited parallelism in computation, while our work extends the structure to 3D with shared WLs and BLs to fully exploit its computational capability to process multi-channel convolution layers. However, since our design focus is different from previous works, we cannot use their works as our baseline. Instead, we compare our design with a custom 2D ReRAM baseline and state-of-the-art CPU and GPU. Second, kernel mapping is not efficiently addressed in PRIME, while we present a more efficient mapping based on a recently proposed approach to compute MKMC [9].

VI. Conclusion

This paper presents a convolution accelerator which efficiently maps multiple kernel multiple channel convolution to monolithic 3D ReRAM. By using a newly proposed algorithm, we for the first time take advantage of the property in equation (1) and maximize parallelism of 3D ReRAM to improve the performance and energy efficiency of convolution layers in convolutional neural networks. In order to implement
negative weights, we present a new approach to accumulate negative weights and non-negative weights separately using configurable interconnects and calculate the final results using peripheral circuits. Our experiment demonstrates that the proposed mapping achieves a speedup of \(5.79 \times\), \(927.81 \times\), and \(36.8 \times\) compared with a custom 2D ReRAM baseline and state-of-the-art CPU and GPU. Our design also reduces energy consumption by \(2.12 \times\), \(1802.64 \times\), and \(114.1 \times\) compared with the same baseline.

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