Charge trapping in Si-implanted SiO₂-Si memory devices at high electric fields and elevated temperatures

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Abstract. In the paper an influence of different electric fields and elevated temperatures on charge trapping in Si nanoclusters enriched SiO₂ is considered. It is shown that in the case of the voltage applied to virgin structure, independently on the applied voltage polarity, an increase of the electric field and measurements temperature results in the appearance of similar charging effect – positive charge generation in the dioxide. Careful analysis of the obtained results allows us to conclude that this positive charge generation on its first stage can be associated with the electron field emission from the electrically neutral Si nanoclusters. Study of the temperature dependence of charge relaxation connected with the electron emission from Si nanoclusters allows us to determine a band gap (near 1.50 eV) and size (near 3.5 nm) of Si nanoclusters imbedded in the SiO₂ by high-dose Si⁺ ion implantation.

1. Introduction
As we have shown in our previous paper [1] recharging of nanoclusters memory structures under 6.4 MV/cm field in dielectric leads to the accumulation of positive charge in virgin samples independently on the polarity of the applied voltage. This phenomenon had been accounted for the field emission of electrons from Si nanoclusters. In this connection two questions of the great interest arise. First, connected with a write/erase charge relaxation behavior in Si-nanocluster memory structures in the vicinity of the previously used switching potential (±25.6 V) on Si-poly gate and, second, what is the influence of temperature, as an alternative free carriers source in nanoclusters, on charge storage and dissipation in memory structures.

2. Samples and experimental details
In our study we used poly-Si-SiO₂-p-Si structures with SiO₂ thickness of 40 nm. The SiO₂ was implanted at room temperature with 15 KeV Si⁺ ions with dose of 2x10¹⁶ ions/cm², corresponding to 10% of excess Si at the project range about 25 nm. Subsequent annealing and final distributions of the nanocrystals are described in details in paper [2].

The charge storage behaviour of the MOS structures was investigated by measuring the shift of the high-frequency (1MHz) C-V characteristics at flat-band conditions (V_{FB}) after applying a programming voltage pulse in the range from ±20V to ±30V with duration from 20 ms to 20 s. Additional relaxation measurements cycles were performed in the temperature range of 20°C to 300°C range with the purpose to study trapping processes at elevated temperatures. It should be noted, that
bias stress (BS) cycles at the positive voltage pulse applied were performed under peripheral illumination of the sample in the region of Si intrinsic absorption in order to enhance an inversion layer generation at the p-Si/SiO₂ interface.

3. Experimental results and discussion

Figure 1 illustrates the relaxation process of $V_{fb}$ setting during write/erase cycling with different symmetrical reprogramming voltages (20.0 V, 22.5 V, 25.6 V and 27.5 V). From this figure it can be concluded that qualitative changes of charge storage in the experimental structure during first BS in the electric field changing from 5 MV/cm to 6.8 MV/cm took place.

![Figure 1](image.png)

**Figure 1.** Reprogramming relaxation cycles of $V_{fb}$ during 6 write/erase cycles in nanomemory test structures under different bias on poly-Si gate starting with the positive bias (a). Enlarged view of the first programming cycle (b). Every set of the curves starts from the virgin sample.

At low field cycling (5 MV/cm) only negative charge trapping and detrapping was observed. Moreover, this charge can be attributed to the electrons capturing in the structure because of the positive $V_{fb}$ observed for relaxation cycles for the positive voltage applied. If a negative bias was applied to the gate of the virgin structure no charge trapping was observed for the measurement time. On the other hand, at the high field (>6.4 MV/cm) positive charge storage prevails at the first BS cycle (figure 1b). As it can be seen from the same figure, there is a latent period (40-200 ms) when there are no changes in $V_{fb}$. This period appears due to the initial switching of the p-Si space charge region (SCR) in the deep nonequilibrium depletion and, hence, the absence of free electrons in p-Si/SiO₂ interface which can be captured in the traps in the SiO₂. Next, the diffusion of electrons from the periphery of the gate supplies the negative charge that can be stored on the traps. The further kinetics depends upon the field applied. If this field is not sufficient to produce free electrons in nanoclusters (+20 V bias) only negative charge is accumulated. In the opposite case (bias >+25.6 V) silicon clusters are ionized with electrons withdrawal to Si-poly and subsequent positive charge storage in nanoclusters (figure 1b). It should be noted, that without illumination no charge capturing while BS period of 7 s was observed, that can be easily explained by the long minority carriers generation time (hundreds of seconds). Moreover, no charge trapping in experimental structures was observed under low negative biasing (-20 V) of the virgin samples in the BS time used.

The above stated facts lead us to the conclusion that silicon behavior in nanoclusters is similar to intrinsic silicon – no free carriers, no charge injection. But except for field ionization, there is an alternative way to get free carriers in the nanoclusters, namely, to raise the temperature of the sample.
So we performed a series of the above described experiment under the elevated temperatures in the range 20 C – 300 C. The results of these experiments are summarized in figures 2 and 3.

**Figure 2.** $\Delta V_{fb}$ relaxation cycles at elevated temperatures with positive gate bias of +20V (a) and +25.6V (b).

From the figures 1 and 2 it may be concluded that negative charge storage takes place only for +20V bias which is due to the electron trapping on the sites in the SiO$_2$. Some residuals of negative charge trapping is also observed for +25.6V bias at the beginning of the relaxation process when the field in dielectric is too small to ionize nanoclusters but the concentration of electrons in SCR is sufficient for their trapping in SiO$_2$.

**Figure 3.** $\Delta V_{fb}$ relaxation cycles at elevated temperatures with negative gate bias of -20V (a) and -25.6V (b).

In the cases of figures 2b, 3a and 3b on the first stage of charging prevails positive charge accumulation due to the field (figures 2b and 3b) and thermal (figure 3a) ionization of silicon in
nanoclusters. If we guess some analogy between nanoclusters and bulk Si then in common this process can be described as following:

$$\Delta N_p(t,T) \sim N_0(T)[1 - \exp(-\frac{t}{\tau(T)})],$$  \hspace{1cm} (1)

where $\Delta N_p$ is the charge stored in nanocluster, $N_0$ is the concentration of free electrons in nanocluster, $\tau$ is the relaxation time constant. If we assume that Si nanocluster can be considered as intrinsic semiconductor, $N_0(T)$ can be presented as following:

$$N_0(T) = n_i(T) = \sqrt{N_c N_v} \exp(-\frac{E_G}{2kT}),$$  \hspace{1cm} (2)

where $N_c$, $N_v$ and $E_G$ – analogs of the bulk density of states in conduction and valence bands and bandgap correspondingly. The similar suggestion was presented in paper [3].

Assuming thermal activation of the charge transport through the boundary barrier ($\tau = \tau_0 \exp(-E_A/kT)$) we calculated activation energy for $\tau$. This energy was in the range of 0.05..0.22 eV. This is a very low value for experimental temperatures over 150 $^\circ$C but allows us to neglect second exponent in equation (1) and estimate $E_G$ of the nanoclusters from expression (2). This energy had been calculated for figure 3a in the temperature range 200..300 $^\circ$C and relaxation times $<300$ms when the side effects of the barrier rising due to the clusters depletion were minor. The obtained value of $E_G$=1.50±0.12 eV is in the good agreement with one found for the band gap for Si nanoclusters with size of near 3.5 nm [4].

4. Conclusions

Study of the charge trapping in Si nanoclusters enriched SiO$_2$ at different electric fields and elevated temperatures allows us to conclude that Si nanoclusters can be considered as uncharged intrinsic silicon, which can be ionized by high electric field and elevated temperature and positively charged. In our case, the calculated band gap of the Si nanoclusters is near 1.50 eV that corresponds to Si nanoclusters size about 3.5 nm.

5. Acknowledgements

This work has been partly funded by the European Commission under the frame of the Network of Excellence “SINANO” (Silicon-based Nanodevices, IST-506844).

6. References

[1] Turchanikov V I, Nazarov A N, Lysenko V S, Carreras J and Garrido B Microelectronics reliability (accepted for publication)

[2] Gonzalez-Varona O, Garrido B, Cheylan S, Perez-Rodrigues A, Cuadras A and Morante J R 2003 Appl. Phys. Lett. 82 2151-53

[3] De Salvo B, Ghibaudo G, Pananakakis G, Masson P, Baron T, Buffet N, Fernandes A and Guillaumot B 2001 IEEE Trans. Electron. Dev. 48 1789-99

[4] Garrido-Fernandez B, Lopez M, Garsia C, Perez-Rodriguez A, Morante J R, Bonafos C, Carrada M and Claverie A 2002 J.Appl.Phys. 91 798-807