LETTER

A low-loss high-linearity SOI SP6T antenna switch using diode biasing method

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Abstract This letter describes a single-pole six-throw (SP6T) antenna switch in a 180nm silicon-on-insulator (SOI) CMOS technology for receive diversity and LTE transmit/receive applications. Using a new diode biasing method, the conventional biasing resistor and supply voltage are removed at the body of the stacked-FET switch, a diode is used to connect the body and gate for body bias instead. The biasing diode turns off and on and functions as a high and small resistor for the on and off state. The proposed design helps to achieve low loss and high linearity. The measured insertion loss (IL) at 0.9 and 1.9GHz are roughly 0.29 and 0.46dB, respectively. The switch shows a second harmonic of -86 and -83dBc, and third harmonic power of -94 and -87dBc with a +26dBm input power at 0.9 and 1.9GHz, respectively.

key words: Silicon-on-insulator (SOI) switch, diode biasing, low loss

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

As more and more communication standards such as Wideband Code Division-Multiple-Access (WCDMA), High-Speed Packet Access (HSPA), and 3GPP Long Term Evolution (LTE) are added into smart devices, multimode multiband front-end architectures are utilized. Besides, more wireless communication technologies such as 5G and Narrow Band Internet of Things (NB-IOT) are being integrated into mobile terminals[1]. Both trends lead to a greater need for RF switch components on front-end design of these devices[2-4].

Compared to the positive-intrinsic-negative(PIN) diode [5,6], micro-electro-mechanical systems (MEMS) [7,8], and gallium arsenide (GaAs) pseudomorphic high electron mobility transistor (pHEMT) [9,10], Silicon-on-insulator (SOI) CMOS process shares the important features of being fast, reliable, and highly integratable, and thus, becomes a preferred choice for switch applications[11-14]. The low break-down voltage and conductive substrate limit the standard bulk CMOS for RF switch applications[15-17]. In a partially-deleted (PD) technology[18], both floating body (FB) and body contacted (BC) FETs are offered[19]. The FB switches are beneficial to lower insertion loss(IL) whereas the BC switches achieve lower harmonics[20,21]. To the contrary, the BC FET benefits the switch linearity due to the ability to prevent the junction diodes from forward biasing using negative body voltage bias[22-24], but the drawback with it is the increased loss[25-27].

This letter implements a single-pole six-throw (SP6T) antenna switch implemented in a 180nm SOI CMOS process. To reduce the IL while maintaining excellent linearity, a stacked-FETs switch strategy employing BC devices with a novel diode biasing scheme has been proposed.

2. Circuit Design

Fig.1. SP6T switch with (a)traditional biasing method;(b) proposed diode biasing method.

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As the ability to provide an advantage to reduce waveform distortion and improve linearity by applying a negative DC bias to the body to prevent the forward-bias of the junction diodes, the BC FET is employed as the switching device. Fig.1(a) shows the traditional SP6T switch structure with BC-FET stacking strategy to improve the power handling capability[28]. Both the gate and body of the BC FETs require a high resister to offer RF isolation for the biasing circuit and a biasing voltage to control the FET ON and OFF state for the switching. When the switch is in the ON state, bias voltage of +2.5V and 0V are applied, respectively, to the gate and body of the BC switch-FETs, whereas a -2.5V bias voltage is applied to both gate and body in the OFF state. However, the major problem of the traditional switch structure is the additional wiring and contacts on and outside the BC stacked-FETs, as well as the need of biasing resistors and control voltage for the body. This results in more complex control and parasitic effect, and slightly larger chip size.

In allusion to the issues mentioned above, we propose a novel diode bias method for the BC SP6T switch, as shown in Fig.1(b). The diode anode is connected to the body of the BC switch-FET whereas the cathode is tied to the gate. When a +2.5V biasing voltage is applied to the switch-FET, the biasing diode would turn off which leads to a +2.5V DC bias voltage at the gate and a slight positive voltage (near to zero) at the body, and thus, turning on the switch device. Also, when a -2.5V biasing voltage is applied, the diode would be forward-biased and enables the body voltage of the BC switch-FET to maintain at nearly same negative DC potential as the gate.

Fig.2 exhibits the SP6T equivalent circuit model when TX1 enabled. In contrast to the conventional version, the proposed scheme reduces the leakage loss for the body, leading to smaller on-state resistance. Since off-state capacitance is small enough, the IL from TX1 to antenna port can be simply expressed as:

\[
IL = 20 \log \left[ 1 + \frac{R_{on\_series}}{2Z_0} \right]
\]  

(1)

It is observed that from (1) that the new bias method is capable of achieving lower IL as it contributes to the decrease of the total on-state resistance \( R_{on\_series} \).

Fig.3 depicts the simulated IL and second/third harmonics when the input power is +26dBm of the two biasing method. It can be seen, on one hand, that the traditional and proposed switch biasing methods show similar low harmonics performance since both methods achieve almost same DC biasing voltage at the gate and body; on the other hand, the result agrees well with the analysis that the novel diode biasing method helps to reduce the IL of the proposed switch due to the absence of the biasing resistor and voltage supply for the body, which contributes to lower parasitic capacitance and loss.

Furthermore, the new bias scheme can achieve smaller chip area. Fig.4 illustrates the top architecture of the designed SP6T antenna switch. The regulator and charge pump are utilized to generate adequate positive and negative biasing voltage, and a 3-bit GPIO CMOS/ TTL-compatible control decoder is applied for path switching, and it is followed by a series of level shifters to shift the biasing voltage. It can be observed that the proposed bias strategy help to decrease the number of level shifters, control wiring and contacts on and outside the switch-FETs by removing the body resistor and voltage supply, and thus, reducing chip size and cost.
3. Fabrication and Results

Fig.5 shows the chip photo of the proposed SP6T antenna switch using diode biasing method with a size of 1000×750μm². Each TX unit consists of a series chain and a shunt chain. Both series and shunt chains have 8 stacked-FETs switch devices. The device width of the series and shunt stacked-FETs devices are set as 3000 and 500μm, respectively, which is optimized for the trade-off of the IL, isolation, and linearity performance.

![Chip photo of proposed SOI SP6T antenna switch.](image)

Fig.5. Chip photo of proposed SOI SP6T antenna switch.

![De-embedded measurement results of proposed SP6T switch: (a) IL; (b) Isolation and Return Loss.](image)

Fig.6. De-embedded measurement results of proposed SP6T switch: (a) IL; (b) Isolation and Return Loss.

Fig.6(a) and (b) plot the de-embedded measurement IL, isolation and return loss of the proposed SOI SP6T antenna switch from 0 to 3.0 GHz. The SP6T switch exhibits low IL of 0.29dB at 0.9GHz and 0.46dB at 1.9GHz. These results agree well with the analysis that the proposed switch can achieve lower IL with the use of the new diode biasing strategy. The isolation is roughly 44dB at 0.9GHz and 37.2dB at 1.9GHz, while the RL is around 27.9dB and 22.7dB at 0.9 and 1.9GHz, respectively.

The 2nd- and 3rd-order harmonic responses at 0.9 and 1.9GHz are measured and depicted in Fig.7(a) and (b), respectively. With a +26dBm input power, the 2nd- and 3rd-order harmonic are -86dBc and -94dBc at 0.9GHz, and -83dBc and -87dBc at 1.9GHz. It can be seen that the SP6T switch reveals low 2nd- and 3rd-order harmonics, which demonstrates that the proposed diode biasing method, without using extra biasing resistor and DC supply for the body, is able to achieve low harmonic distortion and high linearity.

![Measurement results of the 2nd- and 3rd-order harmonic powers for the proposed SP6T switch at the fundamental frequencies of: (a) 0.9GHz; (b) 1.9GHz.](image)

Fig.7. Measurement results of the 2nd- and 3rd-order harmonic powers for the proposed SP6T switch at the fundamental frequencies of: (a) 0.9GHz; (b) 1.9GHz.

Table 1 compares the switch performance of this letter and other published works. In contrast to other SOI-CMOS switches, the proposed SP6T switch achieves competitive IL, isolation, RL, and harmonic distortion. The switch obtains a low IL of 0.29 and 0.46dB at 0.9 and 1.9GHz, respectively, which is lower than those of other reported works. It can be concluded that the proposed switch using the novel diode biasing method provides an advantage to reduce the IL, and meanwhile, maintains favorable harmonic and linearity performance.
5. Conclusion

A low-loss and high-linearity SP6T antenna switch using a diode to connect the body and gate of the BC switch-FET without employing the biasing resistor and supply voltage to the body, has been implemented in a 180nm SOI CMOS process. The new body bias strategy achieves an analogous DC bias as the traditional structure, which helps to reduce the IL without degrading the linearity performance. The switch shows the IL of 0.29 and 0.46dB, second-order harmonics of -86 and -83dBc, and third-order harmonics of -94 and -87dBc with a +26dBm input power at 0.9 and 1.9GHz, respectively. In conclusion, the diode biasing method is a suitable way to achieve high-performance switches.

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