LETTER

A CMOS bandgap reference based on switched capacitor with temperature compensation method

Xiongfei Ran1,2, Ming Chen1, Weiguang Wang1, Li Zhou1, Haiyong Wang1 and Jie Chen1(*)

Abstract  A CMOS bandgap reference based on switched capacitor is proposed in this paper. Temperature compensation is adopted to achieve better temperature coefficient (TC). Two first order compensated reference voltages are combined to realize a new reference voltage with lower TC. Due to the switched capacitor operation, power and area of circuit are reduced. Simulation result shows that the bandgap reference achieves TC of 14.5 ppm/°C from -40°C to 120°C. Bandgap reference output voltage is 235 mV with a ripple voltage of 700 μV.

key words: bandgap, temperature compensation, switched capacitor, current-starved ring oscillator

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Reference circuits are always in demand in many analog, digital or mixed-signal integrated circuits such as low drop-out voltage regulator, analog to digital converter, digital to analog converter, phase-locked loop [1, 2, 3, 4, 5, 6]. Bandgap reference (BGR) circuits provide a voltage which is insensitive to the drift of absolute temperature and supply variation. The stability and efficiency of reference circuits also play a critical role in performance of the subsequent circuit [7, 8].

Continuous time (CT) BGR is the most widely used reference type. A typical CT BGR circuit is shown in Fig. 1. A proportional-to-absolute-temperature (PTAT) current and a complementary-to-absolute-temperature (CTAT) current flowing through R2 and R1, respectively, are combined. This combined current is then copied by current mirror structure to realize a voltage independent of temperature on R4. This BGR is extensively used due to its sub-1V operation [9]. Many compensation techniques have been proposed for this current mode BGR to achieve better performance in TC [10, 11, 12, 13, 14, 15].

However, the drawback of this approach is the tradeoff between area and power. Mega-ohm resistors are required to reduce bias currents. Compared to resistor, capacitor has no quiescent current consumption, which can solve the restriction between layout area and power consumption [16]. The mismatch of resistors and capacitors is also crucial to the accuracy of BGR [17, 18]. The typical value of mismatch error of capacitors in standard CMOS process is 0.1% [19, 20]. This error can be further reduced as process progresses.

V. Ivanov et al. proposed a switched capacitor BGR circuit and used it as a part of a large system on chip [21]. In addition, some other studies on switched capacitor BGR circuits have been published [22, 23, 24, 25, 26, 27, 28, 29]. Because of the simple first order compensation method, the TC of these reference voltage is significantly large.

According to the above review, the realization of low TC on the basis of low power switched capacitor BGR design is a key issue. Therefore this paper presents a novel switched capacitor BGR circuit, by combining two first order compensated reference voltages to achieve compensation for the second order TC of VREF. The TC of voltage reference can be reduced. Additionally, large resistor is not needed in the proposed design. Thus the area/power tradeoff is relieved.

This article is organized as follows. In part 2, the compensation principle used in the proposed design is elaborated. In part 3, the implementation of circuit will be described. Finally, simulation results are presented in part 4.

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2. Compensation principle

In CMOS BGR design, the CTAT voltage is provided by the base-emitter voltage of bipolar junction transistor (BJT). The PTAT voltage is obtained by the difference between the base-emitter voltage of two BJTs biased at different current densities [30].

Reference voltage after first order compensation shows finite curvature in temperature range. One of reasons of this curvature is because $V_{BE}$ has high order TCs [31].

The base-emitter voltage of BJT can be expressed as

$$V_{BE} = \alpha_0 + \alpha_1 T + \alpha_2 T^2$$  \hspace{1cm} (1)

In Eq. (1), $\alpha_0$, $\alpha_1$ and $\alpha_2$ are zero, first and second order TC of $V_{BE}$, respectively. TC higher than second order are neglected here.

Similarly, $\Delta V_{BE}$ can be expressed as

$$\Delta V_{BE} = \frac{kT}{q} \ln N = \beta T \quad (\beta > 0)$$  \hspace{1cm} (2)

Eq. (2) shows that $\Delta V_{BE}$ is linearly proportional to absolute temperature, where $\beta$ is the scale factor [30].

A first order compensated reference voltage can be expressed as

$$V_{ref,1} = k_1 V_{BE} + \Delta V_{BE}$$

$$= k_1 (\alpha_0 + \alpha_1 T + \alpha_2 T^2) + \beta T$$

$$= k_1 \alpha_2 \left[ \frac{\alpha_1 + \frac{\beta}{k_1}}{2\alpha_2} \right]^2 + \frac{\alpha_0 - \frac{(\alpha_1 + \frac{\beta}{k_1})^2}{4\alpha_2}}{\alpha_2}$$  \hspace{1cm} (3)

Similarly,

$$V_{ref,2} = k_2 V_{BE} + \Delta V_{BE}$$

$$= k_2 \alpha_2 \left[ \frac{\alpha_1 + \frac{\beta}{k_2}}{2\alpha_2} \right]^2 + \frac{\alpha_0 - \frac{(\alpha_1 + \frac{\beta}{k_2})^2}{4\alpha_2}}{\alpha_2}$$  \hspace{1cm} (4)

In Eqs. (3) and (4), $k_1$ and $k_2$ are the scale factors for first order compensation. The expression of zero TC points of $V_{ref,1}$ and $V_{ref,2}$, $T_1$ and $T_2$, can be derived from the two equations above, as shown in Eqs. (5) and (6).

$$T_1 = \frac{-\alpha_1 + \frac{\beta}{k_1}}{2\alpha_2}$$  \hspace{1cm} (5)

$$T_2 = \frac{-\alpha_1 + \frac{\beta}{k_2}}{2\alpha_2}$$  \hspace{1cm} (6)

Eqs. (5) and (6) indicate that $T_1$ and $T_2$ are adjustable by choosing different $k_1$ and $k_2$.

At this point, $V_{ref,1}$ and $V_{ref,2}$ can be rewritten as

$$V_{ref,1} = -\frac{\alpha_1 \alpha_2}{\alpha_1 + 2\alpha_2 T_1} \left[ (T-T_1)^2 + \frac{\alpha_0}{\alpha_2} - T_1^2 \right]$$  \hspace{1cm} (7)

$$V_{ref,2} = -\frac{\alpha_1 \alpha_2}{\alpha_1 + 2\alpha_2 T_2} \left[ (T-T_2)^2 + \frac{\alpha_0}{\alpha_2} - T_2^2 \right]$$  \hspace{1cm} (8)

A new reference $V_{REF}$ can be achieved by adding $V_{ref,1}$ and $V_{ref,2}$ together. That is

$$V_{REF} = V_{ref,1} + V_{ref,2}$$  \hspace{1cm} (9)

In the temperature range from $T_1$ to $T_2$, obviously

$$\frac{\partial V_{REF}}{\partial T} = \frac{2\alpha_2 \beta}{\alpha_1 + 2\alpha_2 T_1} \left( T - T_1 \right) \cdot \frac{2\alpha_2 \beta}{\alpha_1 + 2\alpha_2 T_2} \left( T - T_2 \right)$$

$$= \frac{\partial V_{ref,1}}{\partial T} + \frac{\partial V_{ref,2}}{\partial T}$$

$$= \frac{2\alpha_2 \beta}{\alpha_1 + 2\alpha_2 T_1} \left( T - T_1 \right) \cdot \frac{\partial V_{ref,1}}{\partial T}$$  \hspace{1cm} (10)

Eq. (10) shows that the TC of $V_{REF}$ is smaller than $V_{ref,1}$. Similar analysis can be done for $V_{ref,2}$.

In summary, two first order compensated reference voltages can realize a new reference voltage with a lower TC. The compensation principle described in this part is shown in Fig. 2. Two reference voltages on the left side have higher TC in overall temperature range. The compensated reference voltage on the right side achieves lower TC between $T_1$ and $T_2$.

![Fig. 2 Compensation principle of proposed design](image-url)
3. Circuit design

The proposed reference circuit is shown in Fig. 3. Two switched capacitor networks (SCN) SCN_A, SCN_B are connected by an op-amp working as a voltage follower. Each SCN contains four capacitors and six switches. Non-overlapping clock \( \phi_1 \) and \( \phi_2 \) are used to control every switches in SCN.

![Fig. 3 Proposed switched capacitor BGR circuit](image)

The operation of SCN_A is analyzed as follows: During phase \( \phi_1 \), the charge stored in SCN_A is

\[
Q_1 = (V_{BE1} - V_{BE2})(C_{A1} + C_{A2}) + V_{ref,1}C_{A3}
+ (V_{ref,1} - V_{BE1})C_{A4}
\]  

(11)

During phase \( \phi_2 \), the charge stored in SCN_A is

\[
Q_2 = (V_{ref,1} - V_{BE1})(C_{A1} + C_{A4}) + V_{ref,1}(C_{A2} + C_{A3})
\]  

(12)

Due to the conservation of charge, we can find

\[
Q_1 = Q_2
\]  

(13)

Thus, \( V_{ref,1} \) can be derived as

\[
V_{ref,1} = \frac{C_{A1}}{C_{A1} + C_{A2}}V_{BE1} + \frac{V_{BE1} - V_{BE2}}{C_{A1} + C_{A2}}
\]

(14)

Similar analysis can be done for SCN_B. \( V_{REF} \) can be derived as

\[
V_{REF} = \frac{C_{B1}}{C_{B1} + C_{B2}}V_{BE1} + \frac{\Delta V_{BE}}{C_{B1} + C_{B2}}V_{ref,1}
\]  

(15)

In general, the negative TC of \( V_{BE} \) is much bigger than the positive TC of \( \Delta V_{BE} \). The negative TC of \( V_{BE} \) is about -2 mV/°C, and the positive TC of \( \Delta V_{BE} \) is about 0.04 mV/°C. The difference is 50 times [23]. Therefore, the value of \( C_{B2} \) should far exceed \( C_{B1} \) for the purpose of compensation.

According to the above analysis, \( V_{REF} \) can be expressed as

\[
V_{REF} = \frac{C_{B1}}{C_{B1} + C_{B2}}V_{BE1} + \frac{\Delta V_{BE} + V_{ref,1}}{C_{B1} + C_{B2}}
\]  

(16)

In Eq. (16), the first two items represent another first order compensated reference voltage \( V_{ref,2} \). Thus

\[
V_{REF} = V_{ref,2} + V_{ref,1}
\]  

(17)

Eq. (17) shows that the reference voltage \( V_{REF} \) is a combination of two first order compensated reference voltages \( V_{ref,1} \) and \( V_{ref,2} \).

In the proposed design, the values of \( C_{A3}, C_{A4}, C_{B3} \) and \( C_{B4} \) are same and chosen as 50 fF. The values of \( C_{A1}, C_{A2}, C_{B1} \) and \( C_{B2} \) are 50, 500, 50 and 750 fF, which makes \( k_1 \) for SCN_A is about 0.091 and \( k_2 \) for SCN_B is about 0.063. As mentioned in part 2, Eqs. (5) and (6) show that \( T_1 \) and \( T_2 \) of \( V_{ref,1} \) and \( V_{ref,2} \) are adjustable. The ideal values of \( T_1 \) and \( T_2 \) for this design are -40°C and 120°C. However, it’s difficult to adjust \( T_1 \) and \( T_2 \) very accurately in practice. \( T_1 \) and \( T_2 \) can only be as close as possible to the ideal value.

![Fig. 4 Schematic of current-starved ring oscillator](image)

In switched capacitor circuits, clock frequency is related to power consumption and circuit area. Frequency of the switched capacitor operation in this design is selected as 100 Khz. Ring oscillator can provide clock signal with low power consumption and simple circuit realization. However, the propagation delay of a single stage inverter is usually picoseconds or nanoseconds. To obtain a low oscillation frequency in traditional ring oscillator structure, the number of stages will be large.
and intolerable. Therefore, current-starved ring oscillator is adopted. As shown in Fig. 4, M₆₃-M₆₅ and M₆₂-M₆₄ work as active loads to control the operating current of the oscillator circuit [32]. M₆₀-M₆₆ and M₆₃-M₆₇ are three inverters in ring.

Two-phase non-overlapping clock generator is shown in Fig. 5. The output signal of the ring oscillator in Fig. 4 is used to generate four clock signals for controlling CMOS switches in each SCN [33].

![Fig. 5 Two-phase non-overlapping clock generator](image)

The op-amp applied in this design is shown in Fig. 6. With p-type input transistors and a folded-cascode structure, the typical characteristics for the op-amp are 64.3 dB gain and 240 nA current consumption.

![Fig. 6 Schematic of single stage op-amp](image)

The circuits of Vₜₜ generator and bias current provider are shown in Fig. 7. Q₁ and Q₂ are PNP BJTs biased at same current. The emitter area of Q₂ is N times of Q₁ and the number of N in this design is eight. Bias currents in Fig. 4, 6 and 7(a) are provided by the circuit in Fig. 7(b). In order to improve power supply restriction (PSR), cascode current mirror structure is adopted. The start-up circuit and other cascode current source structures are not shown in the figure.

![Fig. 7 (a)Schematic of Vₜₜ generator. (b)Schematic of bias current provider](image)

### 4. Simulation results

The proposed voltage reference circuit based on switched capacitor is designed with a 0.18 µm process and its simulation results are shown in this part.

Fig. 8 shows the variation of the reference voltage output with temperature under different supply voltages. The TCs are 14.1, 14.5 and 16.3 ppm/°C for 2.1, 1.8 and 1.5 V supply voltages, respectively. The maximum voltage change under 1.8 V supply voltage is 0.56 mV.

Fig. 9 shows the variation of the reference voltage output with temperature for different process corners. The TCs are 14.5, 54.1, 131, 20.8 and 96.9 ppm/°C for TT, SS, FF, SF and FS corners, respectively.

Fig. 10 shows the distribution of Vₜₜ obtained from 250 points Monte Carlo analysis with an average of 235.9 mV and a standard deviation of 1.132 mV.
Fig. 11 shows the transient waveform of reference voltage. The start-up time of BGR is approximately 0.75 ms.

The highest error of the reference voltage comes from ripple during the switched capacitor operation. Ripple voltage can be eliminated by better non-overlapping control and charge injection compensation technique. However, this is not necessary if the reference is not used during ripple moments [21]. The ripple voltage of this design is 700 µV as shown in Fig. 11.

The layout of the design using a 0.18 µm standard CMOS process is shown in Fig. 12 and the active area is approximately 0.0312 mm² (130 µm × 240 µm).

Table I is a comparison of the performance of switched capacitor BGR mentioned in different literatures. Compared with previous literatures, the TC of the reference voltage is reduced, indicating that the reference circuit proposed in this paper achieves the compensation effect and has lower TC on the basis of low power.

| Performance parameter     | [21] | [27] | [28] | [29] | This work |
|---------------------------|------|------|------|------|-----------|
| Process(µm)               | 0.13 | 0.35 | 0.35 | 0.18 | 0.18      |
| Supply Voltage(V)         | 0.75 | 5    | 3.6  | 1.8  | 1.8       |
| Vdiss(V)                  | 0.256-0.9 | 1.26 | 1.196 | 0.52 | 0.235     |
| Temperature Range(°C)     | -20–85 | -20–100 | -40–120 | -40–85 | -40–120 |
| TC(ppm/°C)                | 40   | 112  | 78   | 17   | 14.5      |
| Ripple Voltage(mV)        | 20   | N/A  | N/A  | N/A  | 0.7       |
| Power(µW)                 | 0.17 | 170  | 39.6 | 28   | 1.09      |
| Area(mm²)                 | 0.07 | 0.048| 0.15 | N/A  | 0.0312    |

5. Conclusion and future work

A CMOS bandgap reference based on switched capacitor is proposed in this paper. The use of switched capacitor allows a combination of two first order compensated reference voltages to achieve a new reference voltage with lower temperature coefficient. The proposed design circuit is realized by a 0.18 µm CMOS process. The TC of reference output voltage under 1.8 V supply voltage from -40°C to 120°C is 14.5 ppm/°C. The proposed reference voltage is 0.235 V and the ripple voltage caused by switched capacitor operation is 700 µV. Results show that the bandgap reference described in this paper achieves better TC than other works and is suitable for low power application.

For the purpose of saving layout area of switched capacitor BGR, small capacitor is used in the proposed design. This will cause large random noise and have effect on the accuracy of reference output. The power consumption of op-amp and layout area of capacitor will be increased if the reduction of random noise is needed.

TC of proposed design under some corners may not be good due to the effect of process variation. Besides, device mismatch and fabrication error may also lead to inaccuracy of BGR circuit. Such problems can be solved by adding a trimming block to get a suitable or required value for the correct functioning of circuit. Trimming block is not included in this design. However, it is suitable for the structure of proposed design and can be done as a future work.

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References

[1] R. Magod, et al.: “A low-noise output capacitorless low-dropout regulator with a switched-RC bandgap reference,” IEEE Trans. Power Electron. 32 (2017) 2856 (DOI:10.1109/TPEL.2016.2576
21. Y. Ivanov, et al.: “An ultra low power bandgap operational at supply from 0.75V,” IEEE J. Solid-State Circuits 47 (2012) 1515 (DOI:10.1109/JSSC.2012.2191192).

22. H. Klimach, et al.: “A resistorless switched bandgap voltage reference with offset cancellation,” 2013 26th Symposium on Integrated Circuits and Systems Design (2013) 1 (DOI:10.1109/SBCCL.2013.6644882).

23. A. Shrivastava, et al.: “A 32nW bandgap reference voltage operational from 0.5V supply for ultra-low power systems,” IEEE International Solid-State Circuits Conference (2015) 1 (DOI: 10.1109/ISSCC.2015.7062942).

24. Z. Luo, et al.: “0.45-V 5.4-nW switched-capacitor bandgap reference with intermittent operation and improved supply immunity,” IEEE Electronics letters 54 (2018) 1154 (DOI:10.1049/EL.2018.5524).

25. J. H. Boo, et al.: “A Single-Trim Switched Capacitor CMOS Bandgap Reference with a 5% Inaccuracy of ±0.02%, -0.12% for Battery Monitoring Applications,” 2020 IEEE Symposium on VLSI Circuits (2020) 1 (DOI:10.1109/VLSICircuits.2018.9162987)

26. B. R. Gregory: USA Patent 6819163 (2004).

27. J. Zheng, et al.: “An offset-insensitive switched-capacitor bandgap reference with continuous output,” J. Solid-State Circuits 38 (2003) 1085006 (DOI:10.1088/1674-4926/30/8/085006).

28. J. Chen, et al.: “A novel switched capacitor bandgap reference with a correlated double sampling structure,” J. Solid-State Circuits 34 (2013) 025009 (DOI:10.1088/1674-4926/34/2/025009).

29. J. Ebrahimi and M. Arbabnezy: “A New Sub-1V Volt 17 ppm/℃ Offset-insensitive Resistorless Switched-capacitor Bandgap Voltage Reference,” J. Circuits, Systems and Computers 30 (2021) 2150029 (DOI: 10.1142/S021812662150029).

30. J. Razavis: Design of Analog CMOS Integrated Circuits (McGraw-Hill Education Co. & Xian Jiaotong University Press, Xian, 2002.) 319

31. P. R. Gary: Analysis and Design of Analog Integrated Circuits (Wiley, New York, 2001) 4th ed. 306

32. A. Das, et al.: “CMOS temperature sensor using a current starved ring oscillator for low power and low leakage IOT applications,” International Conference on Electronics, Materials Engineering and Nano-Technology (2017) 1 (DOI:10.1109/IEMENETECH.2017.8076963).

33. C. Kumar, et al.: “An efficient two-phase NOC generator for low frequency applications,” IEEE International Conference on Advanced Communications, Control and Computing Technologies (2014) 6 (DOI: 10.1109/ACACCCT.2014.7019180).