Abstract—Interferometric Vision-Based Navigation (iVisNav) is a novel optoelectronic sensor for autonomous proximity operations. iVisNav employs laser emitting structured beacons and precisely characterizes six degrees of freedom relative motion rates by measuring changes in the phase of the transmitted laser pulses. iVisNav’s embedded package must efficiently process high frequency dynamics for robust sensing and estimation. A new embedded system for least squares-based rate estimation is developed in this paper. The resulting system is capable of interfacing with the photonics and implement the estimation algorithm in a field-programmable gate array. The embedded package is shown to be a hardware/software co-design handling estimation procedure using finite precision arithmetic for high-speed computation. The accuracy of the finite precision FPGA hardware design is compared with the floating-point software evaluation of the algorithm on MATLAB to benchmark its performance and statistical consistency with the error measures. Implementation results demonstrate the utility of FPGA computing capabilities for high-speed proximity navigation using iVisNav.

Index Terms—Interferometry, state estimation, least squares, FPGA

I. INTRODUCTION

Precise characterization of a vehicle’s state is critical to ensure safe navigation operations. Be it a spacecraft rendezvous or an aircraft landing/take-off operation, the state-of-the-art places great emphasis on safe and precise unmanned and autonomous execution [1]. Technical advancements in microelectronics and embedded systems aid in the autonomy of sensing and control. Reliable control actions demand high-quality information from the sensing devices as well as processing the information in real-time [2]. Hence, rapid enhancements in high-fidelity sensing and computing capabilities advance the real-time execution of autonomous navigation algorithms.

Traditionally, inertial sensors or inertial measurement units (IMUs) have been used to accomplish the position and attitude sensing for navigation in both autonomous and guided applications [1], [3]. Although IMUs can capture the dynamics of a fast-moving vehicle, the measurements are typically corrupted by biases, drifts, and noises which accumulate over the rendezvous and lead to considerable errors in pose measurements. Fusing the IMU data with GPS [4] partially addresses this problem by providing another set of measurements (global position) to periodically compensate for the IMU drifts. Close-range rendezvous operations are too critical to entirely depend on the GPS because of bandwidth limitations and ambiguity in resolution for minute positional changes.

Opto-electronics and machine vision are being embraced at a rapid pace for relative navigation applications [5]–[7]. The corresponding vision-based sensing modalities provide rich information context of the surrounding world to the ego-vehicles [8], [9]. LiDAR sensors in particular, directly provide range measurements in the interest of landing/take-off operations. However, LiDARs are prone to degradation of measurement density with range [10], [11]. Computing range rate from range measurements may lead to large errors and turn out to be unacceptable for precise landing environments. Recent advancements leveraging structured light solutions to realize velocimetry capabilities are found to be robust to most of the issues [12]–[16].

In addition to sensing, filtering, and optimal state estimation are statutory to effectively utilize the available sensor modalities and thereby achieve mission objectives [17]. An online implementation of a filtering approach allows for real-time state estimation which is critical for autonomous proximity operations [18]. Online sensing and filtering algorithms would benefit from execution on dedicated low-cost embedded solutions such as Field Programmable Gate Arrays (FPGAs) [19]. FPGAs implement customized logic on bare-metal hardware resources and provide infrastructure for processing measurements in real-time.

Customized FPGA-based embedded solutions deploying hardware-software co-design approaches are highly sought-after in robotics. Modular interfacing with multiple sensing channels, parallel processing of estimation and control schemes at significantly lower footprints is an attractive choice for embedded developers to look away from. Consequently, FPGA accelerated solutions are demonstrated to improve performance in sensor fusion and navigation operations utilizing filtering algorithms [20]–[25] and digital signal processing [26], [27].

In this article, we propose a least squares-based method that leverages FPGA architecture to estimate rate in real-time. We outline our previous work on sensor design and the estimation process first and then present the hardware design. We demonstrate the functionality of the FPGA framework in
II. RELATED WORK

An analog vision sensor - VisNav is first conceived to overcome the drawbacks of passive vision-based navigation for high precision relative pose estimation [12], [13]. VisNav uses a set of optical beacons for radiating bursts of frequency-modulated light. Position Sensing Diodes (PSD) on the approaching spacecraft or aircraft sense the modulated optical signals and determine the line of sight toward each beacon. Although the VisNav system supports high-speed optical measurements for position and attitude estimation, it demands a great amount of calibration and installation efforts for the involved analog optoelectronic elements. Alternately, the emergence of high-speed digital cameras replace the PSDs and counters the bandwidth limitations with custom embedded system design [14]. The compatibility of monocular camera and LEDs for a variation of VisNav is explored by Wong et al. [14]. To achieve the same levels of robustness of VisNav using low-frequency camera measurements, a custom digital hardware design, for filtering and estimation along with sensor data processing is needed.

Building upon the VisNav system, an Interferometric Vision-based Navigation sensor (iVisNav) [28] shown in Fig. 1, is proposed for high-frequency velocimetry of a landing base with respect to the sensor system. This is accomplished by illuminating the base with modulated laser light from onboard structured beacons. In one method, Doppler shifts between the illuminated and the reflected light could be captured to estimate the rates of position and angular degrees of freedom [29]. Doppler frequency measurements demand high fidelity and high sampling sensors supported by a high-performance digital computing framework. A simpler and cost-effective approach is to replace the Doppler measurements with phase shift measurements attainable from a Time-of-Flight (ToF) LiDAR.

Referring to Fig. 1, the ToF LiDAR on-board the aircraft illuminates a landing base with modulated infrared (IR) laser source and computes the phase shift ($\phi$) of the detected reflection according to Eq. (1). The phase shift measurements translate to the range ($r$) of the moving base from the sensor system as

$$\phi = \frac{2\pi r f_0}{\lambda}$$  \hspace{1cm} (1)

where $\lambda$ is the wavelength of the laser source, $f_0$ is the modulation frequency, and $c$ is the velocity of light ($2.99 \times 10^8$ m/s).

From consecutive records of phase shift data, a time derivative of the phase is evaluated to derive the relative radial velocity of the aircraft along the projected laser beam.

$$\frac{d\phi}{dt} = \frac{4\pi v_r}{\lambda}$$  \hspace{1cm} (2)

This implies that from digitized time-keeping and successive phase shift measurements captured at a high sampling rate, radial velocity or range rate $v_r$ at $k^{th}$ measurement can be approximated as:

$$v_r = \frac{\lambda}{4\pi} (\phi_k - \phi_{k-1}) = \frac{\lambda}{4\pi} \Delta \phi = \frac{c}{4\pi f_0} \Delta \phi$$  \hspace{1cm} (3)

The geometric setup of the structured beacon system, bench-top prototype, and rate estimation procedures are described in [18], [28]. To re-emphasize the algorithmic procedure, least squares-based rate estimation steps are outlined in the next section.

A. iVisNav: Rate estimation

A set of six or more measurement equations acquired from the iVisNav sensor model assist in the estimation of 6-DOF translational and angular velocity profiles of a rigid body in relative motion. As shown in Eq. (3), the phase shift measurements along the beacon directions $\hat{r}_i$ are obtained from the ToF LiDAR as

$$\Delta \phi_i = \frac{4\pi (\mathbf{v}_i \cdot \hat{r}_i)}{c} f_0$$  \hspace{1cm} (4)

The ToF range measurements are combined with the direction vectors $\hat{r}_i$ calibrated in the camera frame to obtain range vectors from the beacons to the projections as $r_i = k_i \hat{r}_i$ ($i = 1, \ldots, 6$). The scalar $k_i$ is obtained from the ToF sensor’s range value measurements. The displacement of beacon projections $\rho_i$ from the origin of the world frame are expressed in terms of the range vectors as

$$\mathbf{r}_i = \mathbf{r}_c + \rho_i$$  \hspace{1cm} (5)

The vectors $\mathbf{r}_i$ and $\mathbf{r}_c$ are coordinatized in the camera frame of reference, while the projection displacements $\rho_i$ are described in the body-fixed frame attached to the moving object (aircraft).

The time derivative of Eq. (5) is written using the transport theorem [30] as

$$\mathbf{v}_i = \mathbf{v}_c + (\omega \times) \mathbf{\rho}_i$$  \hspace{1cm} (6)

where $\omega$ denotes the relative angular velocity vector and $(\omega \times)$ denotes the corresponding skew-symmetric matrix.
From Eqs. (3) and (4), the rate measurements from the \(i^{th}\) beacon module are re-written as

\[
v_i \cdot \hat{r}_i = \frac{\Delta \phi_i}{4\pi} \lambda = \hat{v}_c \cdot \hat{r}_i + \hat{r}_i \cdot [\omega]_{\times} \rho_i = \hat{r}_i \cdot \hat{v}_c - \hat{r}_i \cdot [\rho_i]_{\times} \omega
\]  

(7)

By stacking the system of vectors obtained from each of the six projections, the least squares problem is obtained as

\[
\begin{bmatrix}
\Delta \phi_1 \\
\Delta \phi_2 \\
\Delta \phi_3 \\
\vdots \\
\Delta \phi_6
\end{bmatrix}
\begin{bmatrix}
\hat{r}_1^T \\
\hat{r}_2^T \\
\hat{r}_3^T \\
\vdots \\
\hat{r}_6^T
\end{bmatrix}
\begin{bmatrix}
\hat{v}_c \\
\omega
\end{bmatrix}
= \begin{bmatrix}
\rho_1 \\
\rho_2 \\
\rho_3 \\
\vdots \\
\rho_6
\end{bmatrix}
\]

(8)

The optimal estimate (in the realm of least squares) for the translational and angular velocity profiles of the center of mass is obtained by the solution to the normal equations as

\[
\hat{v}_c = \frac{\lambda}{4\pi} (H^T W H)^{-1} H^T W \tilde{y}
\]  

(9)

where the \(6 \times 6\) symmetric weight matrix \(W\) is chosen to be the reciprocal of measurement error covariance matrix \(\Sigma\) such that \(W = \Sigma^{-1}\). This choice of \(W\) places error proportional emphasis on each of the measurement equations.

Equation (9) is the least squares solution for the estimation of translational and angular rates. The solution demands six phase shift measurements from the structured light setup and also the displacement of the projections \(\rho_i\) from utilizing the pose estimation from a low-frequency camera sensor.

III. HARDWARE DESIGN

Fig. 2: iVisNav HW/SW co-design: The 32-bit integer arithmetic iVisNav core is deployed on programmable logic (PL) to perform the least squares operation. The ARM-based processing system (PS) facilitates the streaming of sensor data and estimation results via the AXI4 bus. The PS additionally performs floating-point operations to stream appropriate system and measurement information to the PL to evaluate Eq. (9).

The embedded system design for iVisNav estimation framework follows a hardware-software (HW/SW) co-design philosophy as indicated in Fig. 2. The least squares-based state estimation is realized as a custom intellectual property (IP) core implemented on the programmable logic (PL) of the FPGA. The phase difference measurements and the projection vectors (Eq. (9)) are generated on the processing system (PS). Simulated measurements on the PS are utilized to validate the least squares implementation.

A. Development Environment

HW/SW co-design advantageously combines the traits of development efficiency in software implementation (ARM processor) with high-performance capabilities of the hardware implementation (PL) for the design of FPGA embedded systems [31]. The iVisNav estimation framework is designed to evaluate the repetitive and computationally expensive least squares algorithm on the PL while the application-specific measurement pre-processing and data flow control are handled by the PS. The embedded system works by efficiently delivering data from PS (via C code running on ARM CPU cores) to the PL (re-configurable FPGA logic, programmed using Verilog hardware description language) for continuous and accelerated evaluation of state estimation sequence. The PS-PL communication is controlled by a state machine (shown in Fig. 4) and supported by an advanced extensible interface (AXI4) bus protocol utilizing software-accessible registers on the PL. The proposed co-design is implemented on a Xilinx Zynq 7020 FPGA System-on-Chip (SoC) [32] and programmed using Vivado 2019.1 and Vivado High-Level Synthesis (HLS) tools. Operations on the PL are based on 32-bit fixed-point arithmetic except for a matrix inversion module which evaluates using IEEE 754 single-precision floating-point format for extended dynamic range.

B. Architecture: iVisNav Core

The pipelined architecture of the iVisNav core is built with a focus on implementing the sequence of linear algebra operations as depicted in Fig. 3. Four major modules evaluate the computationally expensive filter operations: matrix transpose, matrix multiplication, matrix inversion, and matrix-vector multiplication. The PS controls the data flow by reading and writing to the software-accessible registers. The PL polls these registers for system and measurement data streams as well as to read/write the status of operations. The implementation overview of the said major modules is as follows:

1) Matrix transpose: Matrix transpose operation is performed by reshuffling the buffered row-major matrix data stream to output the data in a transposed column-major order. The transpose module utilizes 3% of the lookup tables (LUTs) available on the Zynq 7020 FPGA SoC.

2) Matrix multiplication: Matrix multiplication is based upon systolic array architecture (SAA) [33]. SAA is a pipelined network arrangement of Processing Elements (PEs) in a 2D mesh-like topology [18]. The PEs perform multiply and accumulate (MAC) operations on the incoming element and share this information immediately with the neighboring PEs. SAA avoids repeated memory accesses for matrix elements and thereby is very effective for low-latency matrix multiply operations. The \(6 \times 6\) matrix multiplication is an area optimized implementation to meet the stringent resource
Fig. 3: The flow of operations implemented on the iVisNav core for least-squares realization. ARM Processor on the PS communicates and controls the data flow via the AXI4 bus interface.

constraints on the number of digital signal processor (DSP) slices on the Zynq 7020. The high-performance multiplication module occupies 16% of DSPs and 45% of LUTs on board the FPGA.

3) Matrix inverse: A scalable single-precision floating-point matrix inversion is implemented using LU decomposition algorithm [34]. Inversion is hardware implemented in stages of:

(a) decomposition of the full-rank matrix $A$, in an iterative manner, to compute a lower triangular matrix $L$, a diagonal matrix $D$, and an upper triangular matrix $U$ as

$$ A = L D U $$  \hspace{1cm} (10)$$

(b) Inversion of the $L$, $D$, $U$ matrices. Special structures enable the computation of their respective inverses with much reduced complexity as shown by Ruan [34].

(c) Multiplication of $U^{-1}$, $D^{-1}$, $L^{-1}$ to obtain the final output, $A^{-1}$ as

$$ A^{-1} = U^{-1} D^{-1} L^{-1} $$ \hspace{1cm} (11)$$

The inversion module is pipelined at the sub-system levels and optimized for high throughput. The complex inversion module is programmed in C and synthesized into register transfer level (RTL) logic using Vivado HLS. The 32-bit inversion module operates using floating-point representation to accommodate a higher dynamic range for internal data representation. To be consistent with the fixed-point implementation of the core, fixed to floating-point and float to fixed-point conversions are performed at the respective input and output ports of the inverse module. Alternative to a floating-point solution, a scaled fixed-point inverse solution might not be able to sustain bit overflows and loss of precision as commonly observed in higher dimensional matrix operations. This reason is based on failing edge cases in our previous development of a 32-bit fixed-point matrix inversion module using Schur’s complement [18]. Resource-wise the inverse module occupies 17% LUTs, 27% DSPs, 9% block RAM, 8% of on-board flip-flops, and 6% of LUT based RAM.

4) Matrix vector multiplication: Analogous to the systolic array architecture, the matrix-vector multiplication utilizes multiply-and-accumulate (MAC) units that operate on the time-aligned input streams of matrix and measurement vector channels. This module takes 11% of LUTs and 12% of DSPs on board the Zynq 7020 FPGA SoC.

Table I shows the FPGA resource utilization of the iVisNav hardware architecture.

| Table I: Implementation requirements for iVisNav core. |
|-----------------------------------------------|
| Resource | Available | Utilization | Utilization % |
|-----------|-----------|-------------|----------------|
| LUT       | 53200     | 35488       | 66.71          |
| LUTRAM    | 17400     | 1555        | 8.94           |
| FF        | 106400    | 14968       | 14.07          |
| BRAM      | 140       | 12.50       | 8.93           |
| DSP       | 220       | 120         | 54.55          |

C. State Machine

The incoming data stream is buffered on the PL using block memory and a state machine shown in Fig. 4 controls the data flow on the PL subject to the state of operation. The PL remains IDLE until it is ready and a start is signalled by the PS. Transfer of data via the software accessible registers takes place until the process of sending is complete. The PL remains in a COMPUTE state until the filtering process is DONE and the cycle continues.

IV. RESULTS

Experimental prototyping of the iVisNav structured light sensor system is demonstrated in [18], [28]. Data obtained from the calibrated as well as the simulated sensor platform setup is utilized for validating the proposed hardware-based state estimation. The linear least squares estimation process is studied for analyzing sensitivity to a single axis rotation and translation maneuver of the sensor relative to the projection surface. In this work, we analyze the performance of the fixed-point hardware implementation of the least squares estimation in Eq. (9). Double-precision floating-point implementation of the least squares on MATLAB is taken as the golden reference for comparison with the FPGA hardware implementation.

Sensor calibration process involves configuring the direction vectors $\hat{r}_i$’s ($i = 1, ..., 6$) in a bench-top experiment [28]. These values for the said experiment with only axial translation
Fig. 4: State machine for the iVisNav hardware architecture: The PL remains in IDLE state until data is ready and the start of filtering is asserted. Data is buffered during the SEND_DATA state and filtering process takes in the COMPUTE state. The PL remains in a DONE state until it is asked to restart the cycle of operation.

and rotation maneuver are cataloged and shown in Table II. Projection displacements \( p_i \)'s are determined using machine vision (such as in Ref. [28]). ToF Lidars in the sensor setup delivers the phase shift measurements from which the phase differences are computed. The least squares algorithm shown in Eq. (9) is implemented on the acquired data while the projection plate is configured to translate and rotate axially with respect to the beacon setup.

TABLE II: Direction vectors corresponding to each of the beacons as configured in the bench top experiment. ©2020 IEEE. Reprinted, with permission, from Sung et al. [28].

| Beacon Index | \( p_i \) |
|-------------|-----------|
| 1           | (0.87264, 0.4977, 0.1367) |
| 2           | (0.8927, −0.5082, 0.1304) |
| 3           | (−0.8586, −0.4957, 0.1391) |
| 4           | (−0.8168, 0.4957, 0.1412) |
| 5           | (0.0001, 0.9999, 0.1249) |

Hardware implementation of the iVisNav core is validated with the simulated inputs that correspond to system and covariance matrices \( H \) and \( R \) respectively, as well as the phase shift measurements, \( \tilde{y} \). The results obtained from the hardware implementation are compared with the true rates and are shown in Figs. 5 and 6. The figure also juxtaposes the estimates from the MATLAB’s implementation for comparing the hardware implementation accuracy with that of the MATLAB’s. We report relatively larger deviations from MATLAB’s results along \( v_x, v_y, \omega_x, \omega_y \) channels where no motion is induced. The finite precision quantization errors appear to dominate the fractional bit representation while representing near 0 values. These errors appear to have propagated through the matrix operations yielding the deviations. Scaling the data prior to finite precision processing, higher number of fractional bits for representation, and floating-point representation are some techniques observed to mitigate this issue and these alternative solutions are being studied to improve accuracy in the edge-cases of filter implementation.

![Fig. 5: iVisNav estimation results: The estimates (axial components) from the FPGA implementation (blue) are compared against their true rates (green) respectively. The MATLAB’s estimation results (red) are also marked for comparison.](image)

(a) Estimates of translational velocity axial component (where motion is induced).

![Fig. 5: iVisNav estimation results: The estimates (axial components) from the FPGA implementation (blue) are compared against their true rates (green) respectively. The MATLAB’s estimation results (red) are also marked for comparison.](image)

(b) Estimates of angular velocity axial component (where rotation is induced).

Fig. 5: iVisNav estimation results: The estimates (axial components) from the FPGA implementation (blue) are compared against their true rates (green) respectively. The MATLAB’s estimation results (red) are also marked for comparison.

The percentage of absolute errors in the channels \( v_z \) and \( \omega_z \) (where motion is induced) are shown in Fig. 7. The percentage error for an estimate \( \hat{x} \) obtained at the \( i^{th} \) instance from the hardware (HW) in contrast with the software (SW) is computed as indicated in Eq. (12). These errors are a relative comparison between the output obtained from MATLAB to that obtained from the iVisNav core’s hardware simulation. The errors at maximum are at 0.8% which indicates the
(a) Estimates of translational velocity $x$ and $y$ components (no relative motion).

(b) Estimates of angular velocity $x$ and $y$ components (no relative motion).

Fig. 6: iVisNav estimation results: The estimates (along the $x$ and $y$ channels) from the FPGA implementation (blue) are compared against their true rates (green) respectively. The MATLAB’s estimation results (red) are also marked for comparison.

accuracy that our 32-bit finite precision hardware implementation offers. The results demonstrate that the Register Transfer Level (RTL) design for the FPGA based estimation reliably replicates a software implementation.

$$\% \text{Error} = \left| \frac{\hat{x}_i, \text{HW} - \hat{x}_i, \text{SW}}{|\hat{x}_i, \text{SW}|} \right| \times 100 \quad (12)$$

Fig. 7: Percentage errors in $v_z$ and $\omega_z$ components: MATLAB simulation results are used as reference for relative error computation.

V. CONCLUSION AND FUTURE WORK

A finite-precision FPGA framework to estimate the relative rates of a moving projection base with respect to the iVisNav sensor system is developed in this paper. While designed for electro-optical sensors like iVisNav, the framework is applicable for motion rate estimation utilizing other Doppler sensors that use RF or other forms of energy modulation. The embedded system is capable of achieving high data throughput and accuracy requirements for real-time navigation tasks. Simulated phase difference measurements are used to verify the functioning of the iVisNav estimation logic on the FPGA. The estimation results from the 32-bit fixed-point implementation are observed to have a maximum deviation of 0.8% from a double-precision MATLAB implementation of the same method. Although specific to the presented use case, the FPGA implementation is observed to be accurate to the quantization bandwidth and forms a basis for optimism to potentially replace floating-point operations. Thereby the authors conclude that similar approaches can be effectively used for high-speed pipelined frameworks and advanced sensing architectures of the future.

The framework is designed as a standalone IP core for interfacing with external modules. The state estimation was found to be realizable in a flight system by implementing it on an FPGA combined with a high-speed digitizer. Robust estimation pipelines are also being researched to improve performance and accuracy in next-generation embedded avionics.
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