Low-Voltage Operation of Ring Oscillators Based on Room-Temperature-Deposited Amorphous Zinc-Tin-Oxide Channel MESFETs

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Schottky diode FET logic (SDFL) ring oscillator circuits comprising metal-semiconductor field-effect transistors (MESFETs) based on amorphous zinc-tin-oxide (ZTO) n-channels are presented. The ZTO channel layers are deposited entirely at room temperature by long-throw magnetron sputtering. Best MESFETs exhibit on/off current ratios as high as 8.6 orders of magnitude, a sub-threshold swing as low as 250 mV dec$^{-1}$, and a maximum transconductance of 205 $\mu$S. Corresponding inverters show peak gain magnitude (pgm) values of 83 with uncertainty levels as low as 0.5 V at an operating voltage of 5 V. Single stage delay times down to 277 ns are measured for three-stage ring oscillators, corresponding to oscillation frequencies as high as 451 kHz. Oscillations are observed at operating voltages as low as 3 V. These results prove the feasibility of room-temperature-deposited, amorphous semiconducting oxide based integrated circuits with SDFL layout. The presented approach provides more efficient as well as fail-safe device fabrication and similar oscillation frequencies at significantly lower operating voltages compared to conventional, high-temperature processed logic circuits based on insulating gates.

1. Introduction

Transparent amorphous oxide semiconductors (TAOSs) exhibit remarkable transport properties despite their disordered structure.[1] Additionally, their high transparency in the visible range associated with the possibility of large-area deposition at low temperatures enables the cost-efficient fabrication of transparent and even bendable circuits. For instance, the TAOS indium-gallium-zinc-oxide (IGZO) is already commercially exploited, however, ongoing research is targeting toward replacing elements such as indium and gallium by abundant elements.[2] One promising material for sustainable, green circuitry is the TOAS zinc-tin-oxide (ZTO) since it can be deposited at room temperature (RT) enabling the low-cost fabrication of transparent, flexible circuits.[3,4]

So far, several ZTO-based metal-insulator field-effect transistors (MISFETs) and related inverters have been reported in the literature, however, those devices required a deposition at elevated temperatures or post-growth annealing processes in order to perform well.[5–7] Reports on associated integrated circuits comprising ZTO MISFETs are restricted to thin film transistor (TFT) logic technology, based on depletion and enhancement transistors, as well as complementary metal oxide semiconductor logic technology, requiring compatible p-type and n-type FETs. Further, an additional fabrication step is necessary for the preparation of the gate insulator. Such MISFETs and related integrated circuits usually require high operating voltages due to the voltage drop across the insulator as well as a limited switching speed due to carrier scattering at the channel-insulator interface.[8] Previously reported ZTO-based ring oscillators, consisting of five or seven stages, exhibited oscillation frequencies between 0.85 and 800 kHz at operating voltages ranging from 5 to 60 V.[9–11] Single stage delay times, resulting in oscillation frequencies compatible with an ISM band, have so far not been reported for ZTO-based ring oscillators.

Recently, first metal-semiconductor field-effect transistors (MESFETs) and simple inverter circuits, comprising depletion-type MESFETs based on room temperature-deposited ZTO channel layers, have been reported.[12,13] Concerning device performance and fabrication efficiency, the absent gate insulator in case of MESFETs enables improved switching behavior as well as more fail-safe and faster processing. However, in case of inverters consisting of depletion-type FETs only, a shifting of the output signal is necessary to cover the voltage range required for switching a subsequent inverter. In the current work, we employ the Schottky diode FET logic (SDFL) approach that facilitates a sufficient level shift of the inverters output signal to enable a successful cascading of a series connection of inverters (see Figure 1). Since the SDFL layout consists of unipolar devices only, transistor channels can be deposited using a single photolithographic patterning process.
2. Results and Discussion

The static RT current–voltage characteristics of a ZTO-based MESFET as well as a schematic cross section through a MESFET sample, illustrating the basic material stacking order, are depicted in Figure 2. The gate width \( W \) and gate length \( L \) are 200 µm and 3 µm, respectively. Figure 2a displays the transfer characteristic as well as the gate leakage current for both voltage sweep directions. The MESFET exhibits a clear field effect with an on/off current ratio of 8.6 orders of magnitude and can be switched on and off within a voltage range of 3 V. The obtained sub-threshold swing and maximum transconductance are 250 mV dec\(^{-1}\) and 205 µS, respectively. A channel mobility of \( \approx 1.8 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1} \) has been calculated using the relation \( \mu = \frac{g_{\text{max}}L}{eWnD} \). \( g_{\text{max}} \) denotes the maximum transconductance derived from the transfer characteristic and the free-carrier density of \( n = 4.3 \times 10^{18} \text{ cm}^{-3} \) was determined by Hall effect measurements. It should be noted the channel mobility clearly underestimates the free-carrier mobility of \( \mu_{\text{H}} = 5.4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1} \), obtained from Hall effect measurements, and hence has to be understood as a lower mobility limit, since the maximum transconductance cannot be determined due to the influence of gate leakage currents for positive gate voltages. The investigated MESFETs are normally-on with threshold voltages ranging from \(-0.6\) to \(-0.3\) V. Further, all investigated devices show a hysteresis of the drain current, especially for low gate voltages. The transfer characteristics obtained for different bias sweep directions cross around \( V_G = 0 \text{ V} \). This dependence on the sweep direction can be attributed to localized states at the interface between the amorphous channel and the gate contact acting as charge traps. A similar effect has already been reported for ZnO-based junction field-effect transistors (JFETs) with amorphous ZnCo\(_2\)O\(_4\) gates.[14,15]

Corresponding output characteristics for various gate voltages \( V_G \) are depicted in Figure 2b. It is notable that the current does not fully saturate with further increasing the source-drain voltage. At \( V_C = 0 \text{ V} \), which corresponds to the operational state of the pull-down transistor and pull-up transistor within the SDFL circuits (see Figure 1), the drain current increases with a slope of 0.15 µA V\(^{-1}\). The shift of the output characteristic for \( V_C \) > 0.5 V is caused by an increased leakage current flow over the gate diode and is a common phenomenon for MESFETs.

An essential step toward the realization of ring oscillators are investigations on the cascadability of the respective inverters. Here, we employ the SDFL approach that has already been
successfully demonstrated for ZTO-based inverters comprising depletion-type MESFETs and JFETs.[16] To achieve compatible output and input voltage levels, our SDFL circuits implement PtO₅/ZTO Schottky barrier diodes for shifting of the output voltage by means of a voltage drop across the diodes in order to switch a subsequent inverter. In addition to these diodes, the level shift configuration contains a transistor with its gate and source shorted, as depicted in Figure 1. This transistor is supplied with a negative operating voltage $V_{\text{bias}}$ and acts as constant-current bias source for the level shifting diodes, hence the denotation pull-down transistor.

Voltage transfer characteristics (VTCs) of a ZTO-based SDFL inverter without and with three level shifting diodes are depicted in Figure 3a for operating voltages $V_{DD}$ between 1 and 6 V. The pull-down transistor was supplied with a negative voltage of $V_{\text{bias}} = -2$ V for all measurements. The gate width and length of the associated driving and pull-up transistor are 100 µm and 5 µm, respectively, while the pull-down transistor has a gate width-to-length ratio of 30 µm/5 µm. For negative input voltages, the output voltage approaches $V_{DD}$. In the on-state of the $V_{m/5}$ width-to-length ratio of 30 µm and voltages approaching 0 V. However, a decreased logic swing has previously been achieved using MESFETs and JFETs with threshold voltages of approximately 0 V.[16] Furthermore, we investigated the cascadability of our SDFL inverters within inverter chains consisting of four series-connected stages. Each SDFL inverter stage consists of three diodes for level shifting. For cascading of these inverters, $V_{IN}$ was applied at the input of the first inverter while $V_{OUT}$ was measured at the output of the last inverter stage. The corresponding VTCs are depicted in Figure 3b for various operating voltages and exhibit the expected inverting behavior. $V_{DD}$ ranges from 3 to 5 V and $V_{\text{bias}}$ was fixed at $-2$ V. Due to an observed level shift of approximately $V_{\text{shift}} = 2.5$ V, operating voltages of $V_{DD} \leq 2.5$ V result in incompatible output driving voltages that do not match the input voltage range. Hence, a successful cascading with inverting behavior was only achieved for operating voltages of $V_{DD} > V_{\text{shift}}$. As expected, it was also observed that the VTCs become significantly steeper the more inverter stages are connected within the chain. In case of four series-connected inverters, the $pgm$ increases up to 700 while simultaneously uncertainty levels as low as 0.08 V are obtained for $V_{DD} = 5$ V.

Measured frequencies as a function of $V_{DD}$ as well as the typical time trace of a three-stage ZTO-based SDFL ring oscillator are depicted in Figure 4. The FET geometry of $W/L = 100 \mu m/5 \mu m$ is analogous to the presented inverter circuits. A

![Figure 3](image-url)  
Figure 3. a) VTCs of an SDFL inverter with no level-shifting diodes as well as three level-shifting diodes based on the circuit schematically depicted in Figure 1. The gate width-to-length ratio of the driving transistor and pull-up transistor is 100 µm/5 µm. The operating voltage of the pull-down transistor is fixed at $V_{\text{bias}} = -2$ V, while the pull-up transistor is supplied with operating voltages ranging from 1 to 5 V. b) Associated VTCs of an inverter chain consisting of four SDFL inverters. Three-level shifting diodes are implemented at the input of each inverter to adjusting the output driving voltage in order to switch the subsequent inverters.

![Figure 4](image-url)  
Figure 4. Oscillation frequencies of a typical ZTO-based three-stage ring oscillator dependent on the applied operating voltage $V_{DD}$. The dashed lines mark the expected frequency range that was calculated based on related FET and inverter parameters, using Equation (1). The inset displays an example for a measured time trace of a ring oscillator at $V_{DD} = 4$ V, exhibiting an oscillation frequency of 351 kHz with an output voltage ranging from 0 to 3.2 V.

Characteristic parameters of the VTCs such as the peak gain magnitude ($pgm$), that is, the maximum gain, and the uncertainty level $V_{UC}$ are depicted in Figure 3a and have been determined for various operating voltages. The $pgm$ can be calculated as $\max|\partial V_{OUT}/\partial V_{IN}|$. $V_{UC}$ is defined as the difference between both input voltages, where the gain equals $-1$. The presented inverter exhibits a $pgm$ and $V_{UC}$ (level shift not considered) of 83 and 0.5 V for $V_{DD} = 5$ V, respectively. Regarding the shifted VTCs in Figure 3a, a total voltage shift of $V_{\text{shift}} = 2.25$ V is obtained for three level shifting diodes. In this case, the $pgm$ slightly decreases to 75, whereas $V_{UC}$ remains 0.5 V at an operating voltage of 5 V. Previously reported ZTO-based SDFL inverters, comprising MESFETs, exhibited a remarkable $pgm$ of 294 at $V_{DD} = 5$ V.[16] This significant discrepancy in maximum gain can be attributed to the voltage dependency of the saturation current of the pull-up transistors and driving transistor at $V_{G} = 0$ V for our devices (see Figure 2b).[17,18]

Furthermore, we investigated the cascadability of our SDFL inverters within inverter chains consisting of four series-connected stages. Each SDFL inverter stage consists of three diodes for level shifting. For cascading of these inverters, $V_{IN}$ was applied at the input of the first inverter while $V_{OUT}$ was measured at the output of the last inverter stage. The corresponding VTCs are depicted in Figure 3b for various operating voltages and exhibit the expected inverting behavior. $V_{DD}$ ranges from 3 to 5 V and $V_{\text{bias}}$ was fixed at $-2$ V. Due to an observed level shift of approximately $V_{\text{shift}} = 2.5$ V, operating voltages of $V_{DD} \leq 2.5$ V result in incompatible output driving voltages that do not match the input voltage range. Hence, a successful cascading with inverting behavior was only achieved for operating voltages of $V_{DD} > V_{\text{shift}}$. As expected, it was also observed that the VTCs become significantly steeper the more inverter stages are connected within the chain. In case of four series-connected inverters, the $pgm$ increases up to 700 while simultaneously uncertainty levels as low as 0.08 V are obtained for $V_{DD} = 5$ V.
maximum oscillation frequency of 451 kHz is observed at $V_{\text{DD}} = 3$ V, corresponding to single stage delay times of 277 ns. Oscillations start to occur at a minimum operating voltage of 3 V, which is attributed to the voltage drop $V_{\text{shift}}$ across the level shifting diodes. For $V_{\text{DD}} < V_{\text{shift}}$, no oscillations are observed since the output voltage range does not match the input voltage range of the subsequent inverter. Within the operating voltage range of approximately $V_{\text{shift}} < V_{\text{DD}} < V_{\text{shift}} + 1$ V, a shift in the frequency can be observed for most of the investigated devices, which has also been reported for ZnO-based SDFL ring oscillators.\[19] For $V_{\text{DD}} \geq V_{\text{shift}} + 1$ V, the observed frequencies of $\approx 350$ kHz stay constant as expected for SDFL circuits, since the supply current is limited by the pull-up and pull-down transistors which operate in saturation and act as constant current sources.

Klüpfel et al. developed an analytical model to estimate the single stage delay time $\tau_0$ based on easily obtainable FET and inverter quantities\[19] $\tau_0$ was calculated using the relation

$$\tau_0 = \frac{\Delta V_C}{I_{\text{PU}} F}$$

where $C_g$, $I_{\text{PU}}$, and $F$ are the driving gate capacitance, the saturation current of the pull-up FET, and the fan-out, respectively.\[19] $\Delta V = V_{\text{shift}}/N_{\text{diode}} - V_{\text{bias}}$ denotes the voltage swing which is present at the input of each driving gate. $N_{\text{diode}}$ is the number of implemented level shifting diodes. If the previous inverter within the cascaded chain drives $F$ gates, the maximum supply current available for recharging of gate capacitances is $I_{\text{PU}}/F$. Since the presented ring oscillator circuits consist of $(N-1)$ inverter stages with $F = 1$ and one inverter stage with $F = 2$ (see Figure 1), the oscillation frequency can be estimated by the relation $f = \frac{2(N+1) \tau_0}{F^2 - 1}$.[19]

The results in terms of expected maximum and minimum oscillation frequencies are represented by the dashed lines in Figure 4. The scattering of calculated frequencies results from variations of the device properties across the sample. $C_g$ was constant and $\approx 15 \mu F$ and $\Delta V$ was determined from the VTCs of the corresponding inverters. $I_{\text{PU}}$ ranged from 50 to 200 $\mu A$, resulting in estimated oscillation frequencies between 170 and 670 kHz. The slight deviations in observed frequencies for various $V_{\text{DD}}$ can be attributed to the saturation current dependence on the source-drain potential.

### 3. Conclusion

In summary, we have realized ring oscillators comprising MESFETs based on room-temperature-deposited amorphous zinc-tin-oxide. Oscillation frequencies up to 451 kHz with single stage delay times of 277 ns have been observed for three-stage ring oscillators with $W = 100 \mu m$ and $L = 5 \mu m$ at $V_{\text{DD}} = 3$ V and $V_{\text{bias}} = -2$ V. Demonstrated ring oscillators operated at voltages as low as 3 V, which is significantly lower compared to previously reported high-temperature processed, ZTO-based three-stage ring oscillators, exhibiting similar single stage delay times at $V_{\text{DD}}$ between 8 and 60 V.\[8,10] In case of amorphous IGZO, similar single stage delay times have been observed for TFT-based ring oscillators, operating at $V_{\text{DD}}$ between $8$ and $80$ V.\[20–25]

Since the single stage delay time of SDFL circuits is strongly dependent on device layout parameters, high-frequency circuits at low operating voltages based on amorphous semiconducting oxides are feasible. By scaling down the gate length by a factor of 10 (leading to a gate length of 0.5 $\mu m$) using state-of-the-art photolithographic patterning techniques, an increase of oscillation frequencies up to 100 times higher is expected due to the linear dependency of the gate length on the driving gate capacitance as well as the total driving current. To operate in the desired ISM band frequency range of for instance 13.56 MHz, a reduction of the gate length to $\approx 0.4 \mu m$ (under otherwise constant device parameters) is necessary.

Overall, the presented results prove that room-temperature-deposited amorphous ZTO is a suitable candidate for more cost-efficient, sustainable green circuitry, and an indium-free and gallium-free alternative to the commercially exploited, far more mature amorphous representative IGZO. Furthermore, it was shown that low-temperature-processed ZTO thin films and associated integrated circuits can compete with previously reported high-temperature-treated devices concerning their performance. Additionally, room-temperature-deposited of entire device structures offers the possibility of utilization of organic substrates, allowing the realization and investigation of flexible and even transparent integrated circuits.

### 4. Experimental Section

The integrated circuits presented in this study comprise MESFETs based on amorphous n-ZTO channels fabricated by radio frequency, long-throw magnetron sputtering. To ensure amorphous growth, the ZTO thin films were deposited at RT using a ceramic target with a $33 \%$ ZnO and 67 wt% SnO$_2$ composition.\[4] A comparatively large target-to-substrate distance of 25 cm was chosen to prevent the impingement of high energetic particles and droplets allowing growth of homogeneous thin films without sputter induced damage. All thin films were deposited on $10 \times 10 \ mm^2$ SiO$_2$ substrates. Since all thin films were deposited at RT, photolithography was used for patterning of transistor structures as well as inverters and ring oscillator circuits.

Previous investigations on ZTO-based MESFETs indicated the formation of a highly conductive layer at the interface close to the substrate, preventing a sufficient depletion of the channels.\[23] Thus, ZTO mesa structures were deposited in two steps: first the sputtering process was ignited in a 25/30 sccm O$_2$/Ar flow atmosphere and subsequently an $\approx 13 \ nm$ thick conductive ZTO layer was sputter-deposited under pure argon flow, resulting in a nominal thickness of 25 nm. The basic material stacking order that was present in all investigated devices is illustrated in Figure 2c. The channel fabrication step was followed by the deposition of source and drain contacts, using DC-sputtered Au. Between the two necessary SDFL design-related metallization steps, a 200 nm thick insulating HfO$_2$ layer was deposited at RT. This insulating layer has also been used to realize multi-gate FET structures, that were implemented in inverters and ring oscillator circuits to increase the maximum current flow through the channel. The gate contact was deposited in a single final step. Reactive sputtered PtO, with a Pt capping was used as gate material to reduce the free-carrier density close to the ZTO/PtO interface due to a saturation of under-coordinated cation bonds via transfer of oxygen from PtO, to ZTO.\[26] The resulting increase in depletion layer width leads to a decrease in tunneling current through the gate diode. Schlupp et al. showed that an additional thin intrinsic ZTO layer (i-ZTO) between channel and gate contact significantly enhances this effect without affecting the device properties otherwise.\[2,22] Hence, an $\approx 10 \ nm$ thick i-ZTO layer was sputtered underneath the gate contact and on top of the conducting ZTO channel in a 25/5 sccm O$_2$/Ar atmosphere.
prior to the deposition of the PtO$_x$/Pt gate contact. Eventually, all gate contacts and their corresponding conduction paths were shorted by a final deposition of a thin Au layer in order to obtain ideal ohmic behavior within the circuits.

Current–voltage measurements and quasi-static capacitance-voltage measurements were carried out using an Agilent 4155C semiconductor parameter analyzer to obtain static current–voltage characteristics and the driving gate capacitance $C_G$, respectively. The capacitance values, necessary for calculating the single stage delay times of the presented ring oscillators, were estimated for gate voltages between 0 and −0.5 V where the capacitance was nearly constant. All measurements were performed in the dark at ambient temperature. Electrical parameters of the ZTO channel layers such as the free-carrier concentration of $n = 4.3 \times 10^{18} \text{ cm}^{-3}$ and a free-carrier mobility of $\mu_0 = 5.4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ were determined by Hall effect measurements. Voltage oscillations of the presented ring oscillators were recorded using a Tiepie Engineering Handyscope HS3 oscilloscope. For signal outcoupling, a high input impedance active probe by GGB Industries Inc. was used to connect the output of ring oscillators to the input of the oscilloscope.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

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