A 0.2–6 GHz linearized Darlington-cascode broadband power amplifier

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Abstract: A pre-distortion linearized Darlington cascode power amplifier cell is explored for broadband amplifier implementation, with additional inclusion of a RLC peaking network at the base terminal of the cascode transistor, and a RC feedback network at the input Darlington transistor. The RLC peaking network optimizes bandwidth and large signal power gain. The RC feedback network simplifies the design of broadband matching for the input Darlington pair. Most importantly, an optimization method of the input Darlington transistor biased at saturation mode is proposed to function as a predistortion linearizer, which can compensate for gain compression and phase deviation effects of the following cascode power stage. With this compensation technique, the proposed broadband PA operating over a frequency range from 0.2 to 6 GHz achieves higher OIP3 than the conventional Darlington cascode amplifier, resulting in a 5 dB improvement of OIP3 at 6 GHz. A P1 dB ranging from 24 to 27 dBm over the frequency range is achieved by this broadband power amplifier with a 0.27 mm2 InGaP/GaAs HBT chip die.

Keywords: power amplifier, linearizer, predistortion, Darlington-cascode

Classification: Microwave and millimeter-wave devices, circuits, and modules

References

[1] M. Iwamoto, et al.: “Optimum bias conditions for linear broadband InGaP/GaAs HBT power amplifiers,” IEEE Trans. Microw. Theory Techn. 50 (2002) 2954 (DOI: 10.1109/TMTT.2002.805135).

[2] M. Koh, et al.: “Broadband linearization of InGaP/GaAs HBT power amplifier,” 40th European Microwave Conference (2010) 878 (DOI: 10.23919/EUMC.2010.5616675).

[3] K. W. Kobayashi: “High linearity dynamic feedback Darlington amplifier,” IEEE CSIC (2007) 1 (DOI: 10.1109/CSICS07.2007.53).
1 Introduction

The 0.2–6 GHz band is the most crowded band for civil communications applications, such as RFID (433 MHz, 915 MHz), LTE (1.8–3.6 GHz), WiMAX (3.3–3.8 GHz), Wi-Fi (2.4 GHz, 5.8 GHz), etc. High linearity broadband power amplifiers (PAs) are of great value for potential use in multi-bands system implementation. Various design techniques and circuit topologies have been proposed for broadband PA implementation [1, 2, 3, 4]. To improve InGaP/GaAs HBT broadband amplifier linearity, the use of a distributed amplifier (DA) has been explored by optimizing collector biasing current [1] or an inductor-capacitor termination (LC trap) at the envelope frequency to reduce third order intermodulation at the input and output terminal [2]. While good RF performance has been achieved, relatively large die areas are observed in the above DAs. A Darlington feedback design [3] has been reported for broadband PA design, showing high linearity. However, its IP3 decreases at high frequency. Our previous work [4] proposed a linearized drive power amplifier; it showed good linearity complementation effect due to the RLC peaking network at the cascode out stage to suppress the 2nd harmonic of the power stage to achieve high linearity. However, both gain and OIP3 of this drive PA decrease immensely as frequency increases, because the drive PA doesn’t have a linearity complementation effect to cover broad frequency band. In this letter, a broadband PA with a common-collector input stage biased at saturation mode is proposed to cover 200 MHz–6 GHz multi-band power amplify application. Table I illustrates design goal of the proposed PA. The linearity complementation mechanism of the input stage is specifically discussed, a close form equation of the gain and phase of this stage is derived, and the method to control linearity complementation using feedback resistor $R_F$ and $C_F$ is illustrated in this paper. With this
compensation technique, OIP3 of a compact broadband PA can be increased by 2∼5 dB, and OIP3 is relatively flat over the broad operation frequency range.

2 Circuit architecture

Fig. 1 is a circuit diagram of the proposed broadband PA. A cascode amplifier is employed for the output power stage due to its reduced Miller effect at high frequencies. It is well known that when it is used as a PA [5, 6, 7, 8], a cascode amplifier suffers the major drawback of unbalanced voltage swing between the bottom transistor Q2 and the top transistor Q3, owing to a different impedance of each transistor at large signal operation. To alleviate this unbalance, an active bias transistor Q5, which replaces a typical resistor divider used in a biasing circuit, is set to track the dynamic current variation of the top and bottom transistors, yielding an equal voltage swing for both transistors in the cascode stage to achieve good linearity performance. This structure was proposed in our previous work [9] to tune the broadband small signal performance. In this work, it is also used to tune the output power impedance which affects the AM-AM and AM-PM modulation characteristics of the output stage.

At the input stage of the proposed PA, R_F and C_F function as a parallel negative feedback, and the emitter resistor R_E serves as a series negative feedback. While the parallel feedback lowers the input impedance of this stage, the series feedback increases its impedance, thus simultaneously adjusting the feedback factor of both the parallel and series networks to achieve broadband matching. In contrast to a typical linear amplifier design, the input transistor Q1 is biased at saturation mode by tweaking collector resistor R_C1 to adjust its collector voltage. This transistor biased at the saturation mode acts as a predistortion linearizer to generate amplitude

| Bandwidth (GHz) | Gain (dB) | VCC (V) | Ibias (mA) | P1dB (dBm) | OIP3 (dBm) |
|-----------------|-----------|---------|------------|------------|------------|
| 0.2–6           | 16–20     | 5       | <50        | >24        | >33        |

Table 1. Design goal of proposed broadband PA

Fig. 1. Schematic of linearized Darlington cascode power amplifier
and phase modulation to compensate the nonlinear distortion originating from the following cascode power stage. More importantly, the degree of the compensation can be accurately controlled by the value of \( R_F \) and \( C_F \). Such a predistortion linearizer uses only a few carefully optimized components without compromising chip area and power consumption.

3 Large signal analysis

Normally, for an output cascode power stage in PA, its power gain is firstly constant and then decreases with increasing input power level, while its phase is firstly constant and then increases at higher power, as shown in Fig. 2, so that both the gain and phase of a power amplifier show nonlinearity at high signal power level. The initial methodology of this work is to design a pre-distortion input stage with reversed AM-AM and AM-PM characteristics to compensate the nonlinearity effect of the cascode output power stage. Hence the input pre-distortion linearizer should show positive gain expansion and negative phase deviation as input power increases.

For the pre-distortion linearizer shown in Fig. 1, its gain and phase dependence on input power is determined by the large signal nonlinear properties of components in transistor \( Q_1 \) under different biasing conditions, and feedback lumped elements: \( R_C, R_F \) and \( C_F \). A large signal nonlinear circuit model based on the Gummel–Poon model [10] for the transistor is developed by incorporating RMS value of input RF power amplitude into its bias condition. The simplified analytical large signal circuit model of the input linearizer stage is shown in Fig. 1. Using KCL and KVL, the voltage transfer function for large signal analysis can be derived from the model:

\[
\frac{V_{out}}{V_{in}} = \frac{(AC + \omega^2 BD) + j\omega(AD - BC)}{A^2 + \omega^2 B^2}
\]

(1)

Phase dependence is given by:

\[
\theta = \arctan \left( \frac{\omega(AD - BC)}{AC + \omega^2 BD} \right)
\]

(2)

where,
\[ A = G_1 G_2 - G_3 g_{ce} - \omega^2 B_1 B_2 + \omega^2 C_{ce}^2 \]
\[ B = G_1 B_2 + G_2 B_1 - G_3 C_{ce} - g_{ce} C_{ce} \]
\[ C = G_1 G_4 + G_5 g_{ce} - \omega^2 B_1 C_{be} - \omega^2 B_F C_{ce} \]
\[ D = G_1 C_{be} + G_4 B_1 + G_5 C_{ce} + g_{ce} B_F \]

The transfer functions of gain and phase of the linearizer can be calculated from amplitude equation (1) and angle equation (2), respectively. Compared with a conventional common collector (CC) transistor, the input linearizer in this work is biased at saturation mode to obtain a positive gain expansion and negative phase deviation, which negate the action of the following cascode stage, as shown in Fig. 3.

Gain and phase deviation of this linearizer can be tuned by the feedback resistor \( R_F \). Fig. 4 plots the power gain and phase delay variation of the input linearizer stage with \( R_F \) from 100 \( \Omega \) to 300 \( \Omega \). It illustrates that the gain expansion amplitude can be adjusted from 1.2 dB to 3 dB by tuning the value of feedback resistor \( R_F \).

Gain and phase deviation of this linearizer can also be tuned by the feedback resistor \( C_F \). Fig. 5 plots the feedback capacitor \( C_F \)'s influence on the phase.
deviation of the input linearizer stage. As $C_F$ changes from 0.5 pF to 2.0 pF, the phase deviation of the input linearizer with the increasing power level can be tuned from 35° to 45°.

It is demonstrated that the input drive stage has the capacity to generate positive gain expansion and negative phase deviation, and the amplitude and phase compensation can both be controlled.

The AM-AM and AM-PM characteristic of a broadband PA with this saturated biased input stage and normal class A biased input stage is simulated. As shown in Fig. 6, when input power is 10 dBm, the PA shows a strong nonlinearity AM-AM and AM-PM effect, the AM-AM compression of PA with the saturation biased input stage is decreased by 14 dB compared with that of a normal biased PA, and the AM-PM deviation is decreased by 18°. It is demonstrated that, both AM and PM distortion of the broadband power amplifier are well compensated for by adjusting the feedback resistor $R_F$ and capacitor $C_F$.

4 Design and measurement results

In this work, we design a broadband PA with the architecture shown as Fig. 1. The cascode transistors $Q_2$ and $Q_3$ are used as the output power stage, both with emitter size of $8 \times 40 \, \mu m^2$. This output stage is biased at Class AB, AND the bias current is 16 mA. The common collector transistor $Q_1$ is used as a pre-distortion input stage,
and the device size is \(4 \times 40 \text{um}^2\). This input stage is biased at saturation mode, and the bias current is 24 mA. The proposed PA is implemented in a commercial 2 µm InGaP/GaAs HBT technology with \(f_T\) of 30 GHz. The die size is only 0.27 mm\(^2\), and the chip photo is shown in Fig. 7.

\[\text{Fig. 7. Small signal s-parameter measurement results}\]

S parameters were measured up to 6 GHz under the biasing conditions: \(V_{cc} = 5 \text{V}, I_{cc} = 40 \text{mA}\), as shown in Fig. 7. It is shown that the average gain \(S_{21}\) is 20 dB during the 0.2–6 GHz bandwidth, \(S_{11}\) is lower than \(-15 \text{dB}\), \(S_{22}\) is lower than \(-10 \text{dB}\). Thus a 0.2–6 GHz broadband amplifier is implemented with good small signal performance.

The power performance of the proposed broadband PA is measured by the high-power test bench as shown in Fig. 8(a). \(\text{OIP}_3\) is measured using 5 MHz offset frequency, and \(\text{P}_{1\text{dB}}\) is measured using continuous wave. \(\text{P}_{1\text{dB}}\) and \(\text{OIP}_3\) versus operation frequency are shown in Fig. 8(b). It is shown that with this saturation biased input compensation stage \(\text{OIP}_3\) is more than 35 dBm up to 4 GHz, resulting in a 2–5 dB improvement over the 0.2–6 GHz frequency range. \(\text{P}_{1\text{dB}}\) is higher than 26 dBm up to 4 GHz, resulting in a 2–6 dB improvement over the 0.2–6 GHz frequency range.

A performance comparison is summarized in Table II. The proposed broadband PA shows good \(\text{P}_{1\text{dB}}\) and \(\text{IP}_3\) with relatively low bias voltage and current, which illustrates that this PA can be operated with low DC power to get high \(\text{P}_{1\text{dB}}\) and \(\text{OIP}_3\) over the 0.2–6 GHz broad bandwidth.

\[\text{Fig. 8. (a) High power test bench (b) \(\text{P}_{1\text{dB}}\) and \(\text{OIP}_3\) measurement results}\]
5 Conclusion

A novel linearized Darlington cascode PA was implemented using InGaP/GaAs HBT technology. The output cascode stage adopted an RLC peaking network to tune both bandwidth and power properties. The large signal gain and phase performance of the input stage with RC feedback was analyzed and optimized. An input linearizer was then demonstrated with the gain and phase properties that, in a manner, negates effects of the cascode power stage to improve overall linearity performance of the amplifier.

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Table II. Performance comparison of previous broadband PA

| REF | Technology | Bandwidth (GHz) | Gain (dB) | VCC (V) | Ibias (mA) | P1dB (dBm) | OIP3 (dBm) |
|-----|------------|-----------------|----------|---------|------------|------------|------------|
| [1] | GaAs HBT   | 0.5–11          | 6.5–8.5  | N/A     | N/A        | 22–25      | 32–40      |
| [2] | GaAs HBT   | 0.5–3           | 6–12     | 5       | 61         | 19–22      | 33–39      |
| [3] | GaAs HBT   | 0.05–4          | 17–20    | 5       | 30         | 20@2G      | 40@2G      |
| [4] | GaAs HBT   | 0.1–4           | 16–28    | 5       | 80         | 17–26      | 26–36      |
| [7] | 0.18 CMOS  | 4–17            | 8–12     | 3.6     | 85         | 15–17      | >25        |
| This work | GaAs HBT | 0.2–6          | 18–20    | 5       | 40         | 24–27      | 33–36      |