Accelerating Recommender Systems via Hardware “scale-in”

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Abstract—In today’s era of “scale-out”, this paper makes the case that a specialized hardware architecture based on “scale-in”—placing as many specialized processors as possible along with their memory systems and interconnect links within one or two boards in a rack—would offer the potential to boost large recommender system throughput by $12-62\times$ for inference and $12-45\times$ for training compared to the DGX-2 state-of-the-art AI platform, while minimizing the performance impact of distributing large models across multiple processors. By analyzing Facebook’s representative model—Deep Learning Recommendation Model (DLRM)—from a hardware architecture perspective, we quantify the impact on throughput of hardware parameters such as memory system design, collective communications latency and bandwidth, and interconnect topology. By focusing on conditions that stress hardware, our analysis reveals limitations of existing AI accelerators and hardware platforms.

I. INTRODUCTION

Recommender Systems serve to personalize user experience in a variety of applications including predicting click-through rates for ranking advertisements [34], improving search results [30], suggesting friends and content on social networks [30], suggesting food on Uber Eats [53], helping users find houses on Zillow [54], helping contain information overload by suggesting relevant news articles [55], helping users find videos to watch on YouTube [43] and movies on Netflix [59], and several more real-world use cases [60]. An introduction to recommender system technology can be found in [58] and a set of best practices and examples for building recommender systems in [56]. The focus of this paper is recommendation systems that use neural networks, referred to as Deep Learning RecSys, or simply RecSys[1]. These have been recently applied to a variety of areas with success [34] [30].

Due to their commercial importance—by improving the quality of Ads and content served to users, RecSys directly drives revenues for hyperscalers, especially under cost-per-click billing—it is no surprise that recommender systems consume the vast majority (\sim80\%) of AI inference cycles within Facebook’s datacenters [1]; the situation is similar [30] at Google, Alibaba and Amazon. In addition, RecSys training now consumes \geq50\% of AI training cycles within Facebook’s datacenters [10]. Annual growth rates are $3.3\times$ for training [10] and $2\times$ for inference [31]. The unique characteristics of these workloads present challenges to datacenter hardware including CPUs, GPUs and almost all AI accelerators. Compared to other AI workloads such as computer vision or natural language processing, RecSys tend to have larger model sizes of up to 10TB [7], are memory access intensive [30], have lower compute burden [31], and rely heavily on CC operations \times [6]. These characteristics make RecSys a poor fit for many existing systems, as described in Sec. [II] and call for a new approach to accelerator HW architecture.

In this paper, various HW architectures are analyzed using Facebook’s DLRM [30] as a representative example and the resulting data are used to derive the characteristics of RecSpeed, an architecture optimized for running RecSys. Specifically, we:

- Describe the DLRM workload in terms of its characteristics that impact HW throughput and latency.
- Identify HW characteristics such as memory system design, CC latency and bandwidth, and CC interconnect topology that are key determinants of upper bounds on RecSys throughput.
- Use a generalized roofline model that adds communications cost to memory and compute to show that specialized chip-level HW features can improve upper bounds on RecSys throughput $4\times$ by reducing latency and $7\times$ by improving bandwidth. It is known that a fixed-topology quadratic interconnect can offer CC all-to-all performance gains of $2.3\times-15\times$ [10].
- Explain why AI accelerators for RecSys would benefit from supporting hybrid memory systems that combine multiple forms of DRAM.
- Evaluate the practical implementation of specialized HW for RecSys and show how this has the potential to improve throughput by $12-62\times$ for inference and $12-45\times$ for training compared to the NVIDIA DGX-2 AI platform.

II. RELATED WORK

There are several published works that describe systems and chips for accelerating RecSys. Compared to these, our work focuses on sweeping various hardware parameters for a homogeneous[2] system in order to understand the impact

1While the term is often used to denote any recommender system, it is specifically used for Deep Learning recommenders here.

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of each upon upper bound DLRM system throughput. As such, we do not evaluate, from the standpoint of RecSys acceleration, any of the other types of systems described below.

A. Heterogeneous Platforms

Facebook’s Zion platform [2] is a specialized heterogeneous system for training RecSys. Fig. [1] shows the major components and interconnect of the Zion platform, which are summarized in Table I. Zion offers the benefit of combining very large CPU memory to hold embedding tables with high compute capability and fast interconnect from GPUs, along with 8 100GbE NICs for scale-out. AIBox [7] from Baidu is another heterogeneous system. A key innovation of AIBox is the use of SSD memory to store the parameters of a model up to 10TB in size; the system uses CPU memory as a cache for SSD. The hit rate of this combination is reported to increase as training proceeds, plateauing at about 85% after 250 training mini-batches. A single-node AIBox is reported to train a 10TB RecSys with 80% of the throughput of a 75-node MPI cluster at 10% of the cost.

| Feature            | Example of Implementation |
|--------------------|---------------------------|
| CPU                | 8x server-class processor such as Intel Xeon |
| CPU Memory speed   | DDR4 DRAM, 6 channels/socket, up to 3200MHz, ~25.6GB/s/channel |
| CPU memory capacity| Typical 1 DIMM/channel, up to 256GB/DIMM = 2TB/CPU |
| CPU Interconnect   | UltraPath Interconnect, coherent |
| AI HW Accelerator  | PCIe Gen4 x16 per CPU, ~30GB/s |
| Accelerator Interconnect | 7 links per accelerator, x16 serdes lanes/link, 25G, ~350GB/s/card |
| Accelerator Power  | Up to 500W @ 54V/48V, support for liquid cooling |
| Scale-out          | 1x NIC per CPU, typically 100Gb Ethernet |

B. Homogeneous Platforms

NVIDIA’s DGX-A100 and Intel/Habana’s HLS-1 are two representative examples of homogeneous AI appliances. Tables II and III respectively summarize their key characteristics.

TABLE II: Key Features of NVIDIA DGX-A100 [76].

| Feature            | Example of Implementation |
|--------------------|---------------------------|
| CPU                | 2x AMD Rome 7742, 64 cores each |
| CPU Memory speed   | DDR4 DRAM, 8 channels/socket, up to 3200MHz, ~25.6GB/s/channel |
| CPU memory capacity| Typical 1 DIMM/channel, up to 256GB/DIMM = 2TB/CPU |
| AI HW Accelerator  | 8x NVIDIA A100 |
| Accelerator Memory | HBM2 @ 2430MHz [75], 40GB/chip, 320GB total |
| System Power       | ~6.5kW max. |
| Scale-out          | 8x 200Gb/s HDR Infiniband |

In this example, the typical buffer chip found on each DIMM is replaced by a specialized NMP (Near-Memory Processing) chip such as TensorDIMM [20] or RecNMP [19] that can access both ranks simultaneously, cache embeddings, and pool them prior to transfer over the bandwidth-constrained channel. For a high-performance server configuration with one dual-rank DIMM per memory channel, simulations [19] indicate speedups of $1.61 \times$ to $1.96 \times$.

It is also possible to provide a memory/compute module in a non-DIMM form factor. An example is Myrtle.ai’s SEAL Module [77], an M.2 module specialized for recommender systems embedding processing. This is built from Bittware’s 250-M2D module [78] that integrates a Xilinx Kintex UltraScale+ KU3P FPGA along with two 32-bit channels of DDR4 memory. Twelve such modules can fit within an OpenCompute Glacier Point V2 carrier board [79], in the space typically taken up by a Xeon CPU with its six 64-bit channels of DDR4 memory.

The second approach is to build a processor directly into a DRAM die. UpMem [27] has built eight 500MHz processors into an 8Gb DRAM. Due to the lower speed of the DRAM process, the CPU uses a 14-stage pipeline to boost its clock rate. Several factors limit the performance gains available with this approach. These include the limited number of layers of metal (e.g. 3) in DRAM semiconductor processes, the need to place the processor far downstream from sensitive analog sense amplifier logic, and the lag of DRAM processes behind logic processes.

TABLE III: Key Features of Intel/Habana HLS-1 [25].

| Feature            | Example of Implementation |
|--------------------|---------------------------|
| AI HW Accelerator  | 8x Habana Gaudi |
| Accelerator Memory | HBM, 32GB/chip, 256GB total |
| System Power       | ~3.2kW max. |
| Scale-out          | 24x 100Gb Ethernet configured as 3 links per chip |

C. In/Near Memory Processing

RecSys models tend to be limited by memory accesses to embedding table values that are then combined using pooling operators [19], which makes the integration of memory with embedding processing an attractive solution. The first approach for this is to modify a standard DDR4 DIMM by replacing its buffer chip with a specialized processor that can handle embedding pooling operations.

Fig. [2] shows the idea behind this concept for a scenario involving two dual-rank DIMMs sharing one memory channel. In such a scenario, the buffer chip of a single memory channel is replaced by a specialized NMP (Near-Memory Processing) chip such as TensorDIMM [20] or RecNMP [19] that can access both ranks simultaneously, cache embeddings, and pool them prior to transfer over the bandwidth-constrained channel. For a high-performance server configuration with one dual-rank DIMM per memory channel, simulations [19] indicate speedups of $1.61 \times$ to $1.96 \times$.

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Fig. 1: FB Zion System: Major components and interconnect.

Fig. 2: Near-Memory Processing via Modified DIMM Buffer Chip. Example shows two DIMMs, each dual-rank, sharing a single memory channel.

D. DRAM-less Accelerators

DRAM-less AI accelerators include the Cerebras CS1 [15], Graphcore GC2 [13] and GC200 [16]. The CS1 and GC2 lack attached external DRAM, and the GC200 likely offers low-bandwidth access to such DRAM since two DDR4 DIMMs are shared between four GC200s via a gateway chip.

E. Other approaches

Centaur [61] offloads embedding layer lookups and dense compute to an FPGA that is co-packaged with a CPU via coherent links. NVIDIA’s Merlin [62], while not a HW platform for RecSys, is an end-to-end solution to support the development, training and deployment of RecSys on GPUs. Intel [6] describes optimizations that improve DLRM throughput by $110 \times$ on a single CPU socket, to a level about $2 \times$ that of a V100 GPU, with excellent scaling properties on clusters of up to 64 CPUs.

There is also a considerable body of work on domain-specific architectures for accelerating a broad set of AI applications and there are several surveys of the field [71] [72] [73]. An up to date list of commercial chips can be found in [68]. Approaches using FPGAs are described in [70] [69], and [74] describes a datacenter AI accelerator.

III. OVERVIEW OF RECOMMENDER SYSTEMS

In this section, we provide an overview of a representative RecSys, Facebook’s DLRM [34], from both application and algorithm/model perspectives, including relevant deployment constraints and goals that will guide the development of our architecture. An overview of several other RecSys can be found in [30].

A. Black box model of RecSys: Inputs & Output

The focus of this paper is a RecSys for rating an individual item of content, as opposed to RecSys that process multiple items of content simultaneously [63]. Inputs to the RecSys are a description $u$ of a user and a description $c$ of a piece of content; the RecSys outputs the estimated probability $P(u, c) \in (0, 1)$ that the user will interact with the content in some specified way. Both the user and the content are described by a set of dense features $\in \mathbb{R}^n$ and a set of sparse features $\in \{0, 1\}^m$. Dense features are continuous, real-valued inputs such as the click-through rate of an Ad during the last week [33], the average click-through rate of the user [33], and the number of clicks already recorded for an Ad being ranked [35]. Sparse (or categorical) features each correspond to a vector with a small number of 1-indices out of many 0s in multi-hot vectors, and represent information such as user ID, Ad category, and user history such as visited product pages or store pages [64] [65].

From a conceptual standpoint, the RecSys could be run on every piece of content considered for a user and the resulting output probabilities could then be used to determine which items of content to show that user to achieve business objectives such as maximizing revenue or user engagement. Note that the RecSys output may be combined with other components in order to decide what content to ultimately show the user, as described in Sec. [III-B]
B. Deployment Scenario

A typical deployment scenario of a RecSys model is illustrated in Fig. 3:

1) User loads a page, which triggers a request to generate personalized content. This request is sent from the user’s device to the company’s datacenter.

2) Based on available content, an input query is generated, consisting of a set of \( B \) (the query size) features, each one representing the piece of content and the user, and possibly their interactions. \( B \) varies by recommendation model. There is typically a hierarchy of recommendation models whereby easier-to-evaluate models rank larger amounts of content first with high \( B \), and then pass the top results to more complex models that rate smaller amounts of content with lower \( B \). \( B \) in the low to mid-hundreds is representative [30], with some \( B \) as large as \( \sim900 \).

3) This query is then passed on to the RecSys. This system outputs, for each of the \( B \) pieces of potential content, the probability that the user will interact with that content in some way. In the case of advertising, this often means the probability that the user will click on the Ad. For video content, it could be metrics related to user engagement [43].

4) Based on these probabilities, the most relevant content is returned to the user, for instance “the top tens of posts.” [1]. However, for Ad ranking, the probabilities generated by the RecSys are first fed to an auction where they are combined with advertiser bids to select the Ad(s) that are ultimately shown to the user [42] [51].

C. System Constraints

RecSys operate under strict constraints.

Inference Constraints: The system must return the most accurate results within the (SLA and thus inviolate) latency constraint defined statistically in equation [1] where \( PPF(D_Q, P) \) is the percentage point function or inverse CDF, \( D_Q \) is the distribution of the times to evaluate each query, \( P \) is a percentile, such as 99th or 90th, and \( C_{SLA} \) is the latency constraint, typically in the range of “tens to hundreds of milliseconds” [1]. Tail latencies are dependent on the QPS (queries per second) throughput of the serving system [30]; one method to trade off QPS and tail latency which [30] explores adjusting the query size.

\[
PPF(D_Q, P) \leq C_{SLA}
\]  

Training Constraints: The system must train the most accurate model within the minimum amount of time. Recommendation models need to be retrained frequently in order to maintain accuracy when faced with changing conditions and user preferences [32], and time spent training a new model is time when that model is not contributing to revenue.

Total deployment cost for the hardware needed to run the system is also a consideration. This is measured as the TCO, or Total Cost of Ownership, of that hardware.

D. Model Overview of DLRM

The DLRM structure was open-sourced by Facebook in 2019 [34]. Fig. 4 illustrates the layers that comprise the DLRM model. DLRM is meant to be a reasonably general structure; for simplicity, the “default” implementation is used, with sum pooling for embeddings, an FM based [36] feature interactions layer, and exclusion of the diagonal entries from the feature interactions layer output.

Inputs to DLRM are described in Sec. III-A. We note that each sparse feature is effectively a set of indices into embedding tables. We now describe embedding tables and the other main components of DLRM.

Embedding tables are look-up tables, each viewed as a \( c \times d \) matrix. Given a set of indices into a table, the corresponding rows are looked up, transposed to column vectors and combined into a single vector through an operation called pooling. Common pooling operators include sum and concatenation [30]. An example of a sparse feature is user ID—a single index denoting the user for whom Ads are being ranked, corresponding to a single vector in an embedding table [39]. We typically refer to the output of embedding tables as

\(^{3}\)Factorization Machine.
embedding vectors, and embedding tables themselves may be referred to as embedding layers.

**FC Layers**: The DLRM contains two Multi-Layer Perceptrons (MLPs), which consist of stacked (or composed) fully connected (FC) layers. The “bottom MLP” processes the dense feature inputs to the model, and the “top MLP” processes the concatenation of the feature interactions layer output and the bottom MLP output. DLRM uses ReLU activations for all FC layers except the last one in the top MLP which uses a sigmoid activation; this is to convert the 1-dimensional output of that layer to a click probability \( \in (0, 1) \).

**Feature interactions layer**: This layer is designed to combine the information from the dense and sparse features. The FM-based feature interactions layer forces the embedding dimension of every table and the output dimension of the final FC layer in the bottom MLP to all be equal. After the dense features are first run through the bottom MLP, the output size is \( b \times d \), where \( b \) is the batch size being used for inference or training, and \( d \) is the common embedding dimension. Further, each of the \( s \) sparse feature embedding tables produces a \( b \times d \) output after pooling. These are concatenated along a new dimension to construct a \( b \times (s+1) \times d \) tensor which we will call \( A \). Let \( A' \in \mathcal{R}^{b \times d \times (s+1)} \) be constructed by transposing the last two dimensions of \( A \). \( F \) is then calculated as the batch matrix multiplication of \( A \) and \( A' \) such that \( F \in \mathcal{R}^{b \times (s+1) \times (s+1)} \). Roughly half of these entries are duplicates, and those are discarded along with optionally the diagonal entries, which we opt to do. After flattening the two innermost dimensions, the result is the output matrix \( F' \in \mathcal{R}^{b \times \frac{(s+1)^2}{2}} \). This batch of vectors, after being concatenated with the bottom MLP output, is then fed to the top MLP. In algorithms [1] and [2], part of Sec. [IV-C] where we cover the implementation of DLRM from a HW architecture perspective, for simplicity, this concatenation is considered as part of the feature interactions layer.

**E. RecSys vs. other AI models**

The two key factors that set RecSys models apart from other AI models (such as those for computer vision or natural language processing) are arithmetic intensity—the number of compute operations relative to memory accesses—and model size. RecSys models are significantly larger and have significantly lower arithmetic intensity as shown in Table [IV] resulting in increased pressure on memory systems and interconnect structure.

**IV. DLRM FROM A HARDWARE ARCHITECTURE PERSPECTIVE**

A. Distributed model setup

The characteristics of recommender systems require a combination of model parallelism and data parallelism. On a large homogeneous system, dense parameters such as FC layer weights are copied onto every processor. However, embedding tables are distributed across the memory of all processors, such that no parameters are replicated. This arises from the fact that embedding tables can easily reach from several 100 GBs to multiple TBs in size [40].

While each processor can compute the dense part of the model for a batch, it cannot look up the embeddings specified by the sparse features, because some of those embeddings are stored in the memory of other processors. Thus, each processor...
needs to query other processors for embedding entries. This leads to the communication patterns outlined in Sec. IV-B.

There are multiple ways to split up the embedding tables. The distribution and (if beneficial) replication of tables across processors must be optimized to avoid system bottlenecks by evening out memory access loading across the memory systems of the various processors. One extreme is “full sharding” of the tables, where tables are split up at a vector-level across the attached memory systems of multiple processors to get very close to uniformly distributing table lookups—at the cost of increased communication. This increased communication and the resulting stress on the HW is due to the fact that, with full sharding, each processor is prevented from doing local pooling of embeddings, thus requiring unpooled vectors to be communicated, of which there are many more than pooled vectors, as described in Sec. III-D. As such, many systems today attempt to fit entire tables into the memory of single processors (which we call “no sharding”), or to break up the tables as little as possible as shown on slide 6 of [2].

B. CC operations

The following CC operations are key to distributed RecSys throughput. For more information on CC operations, please see [8]. In all of the scenarios described below, there are \( n \) processors, numbered \( 1, 2, \ldots, n \).

All-to-all: This CC primitive essentially implements a “transpose” operation. Each processor starts out with \( n \) pieces of data. Supposing \( A_{ij} \) denotes the \( j \)th piece of data currently residing on the \( i \)th processor, then the all-to-all operation will move \( A_{ij} \) such that it is instead on the \( j \)th processor and is ordered as the \( ij \)th piece of data there. This operation is useful when each processor needs to send some data to every other processor.

All-reduce: All-reduce is an operation which replaces local data on each processor with the sum of data across all processors. If processor \( i \) contains data \( A_i \), then after the all-reduce operation, all processors will contain \( A_R = \sum_{i=1}^{n} A_i \). Efficient all-reduce algorithms exist for ring interconnects [8] which are popular in AI systems; however, all-reduce can also be implemented in equivalent time by first performing a reduce-scatter operation and then an all-gather operation.

Reduce-scatter: This operation may be best described as an all-to-all operation followed by a “local reduction.” Similar to the all-to-all setup, the starting point is \( A_{ij} \) as the \( j \)th piece of data on processor \( i \). Where all-to-all will result in this being the \( ij \)th piece of data on processor \( j \), reduce-scatter performs an extra reduction, such that the only piece of data on processor \( j \) at the end is \( \sum_{i=1}^{n} A_{ij} \).

All-gather: In this operation, the starting point is a single piece of data \( A_i \) on each of the \( n \) processors, and the result of the operation is to have every \( A_i \) on every processor. For example, with 4 processors initially containing \( A_1, A_2, A_3, \) and \( A_4 \), respectively, after the all-gather operation, each processor will contain all of \( A_1, A_2, A_3, \) and \( A_4 \).

C. Detailed steps for DLRM Inference and Training

Please refer to the Appendix for a description of operators and an in-depth view of the steps involved in DLRM inference and training.

D. Key HW performance factors

Our performance model (Sec. V-B) helps identify several HW characteristics that are major determinants of throughput for the RecSys that we evaluate. As could be expected from the DLRM operations described in the previous three sections, these are CC performance, memory system performance for embedding table lookups, compute performance for running the dense portions of the model, and on-chip buffering. The following sections examine each of these factors in more detail.

1) CC Performance: RecSys make extensive use of CC for exchanging embedding table indices, embedding values, and for gradient averaging during training backprop. Table IV summarizes HW factors that impact RecSys CC performance. In particular, all-to-all with its smaller message sizes is especially sensitive to latency and scales poorly with interconnect such as rings [10]. Various lower bounds on the latency and throughput of these operators have been derived for representative system architectures [8].

| TABLE IV: Recommender System vs. Other AI Models. Data from Table 1 of [31]. |
|-----------------------------------------|
| Category | Model Type | Size #Parms | Arithmetic Intensity | Max. Live Activations |
| Computer Vision | ResNetXt0101-32x4-48 | 43-829M | Avg. 188-380 | 2.4-29M |
| Language | Seq2Seq ORULSTM | 100M-1B | 2-20 | >100K |
| Recommender | Fully Connected Layers | 1-10M | 2-200 | >100K |
| Recommender | Embedding Layers | >10B | 1-2 | >10B |

TABLE V: Summary of HW Collective Communications factors for RecSys.

| Factor | Impact |
|--------|--------|
| Per-processor bandwidth | Sets upper-bounds on CC all-reduce and all-to-all throughput |
| Interconnect topology | Major determinant of all-to-all throughput |
| Ring interconnect | Well-suited for all-reduce, poorly-suited for all-to-all |
| CC latency | Particularly important for all-to-all due to smaller message sizes |

For the purposes of HW analysis on homogeneous systems, we note the following [8]:

1. Systems where all processors share equally in the communications and arithmetic components of CC.
For an all-to-all with data volume $V$ and $n$ processors, the lower bound on the amount of data sent and received by each processor is $V \times \frac{(n-1)}{n}$.

Similarly for an all-reduce, the lower bound is $2 \times V \times \frac{(n-1)}{n}$.

The above bounds impose a minimum per-processor data volume that must be transferred. As a consequence, the bandwidth per processor will limit overall all-to-all and all-reduce throughput, even as more processors are added to a system. As a rule of thumb, for a large system with a per-processor interconnect bandwidth $BW$, the maximum achievable system-wide all-to-all and all-reduce throughputs are roughly $BW$ and $\frac{BW}{2}$.

The above rule of thumb works well for NVIDIA's DGX-2 system built from 16 V100 processors [9] since it achieves an “all-reduce bandwidth” of ~118GB/s with a maximum per-processor bandwidth (Fig. 9 of [9]) of 150GB/s from six NVLink2 interconnects per V100 chip, for an efficiency of 79% of the theoretical peak.

Fig. 5 illustrates the impact of latency on CC throughput. Due to the ~100μs latency for all-gather on the DGX-2, the time to perform an all-gather for smaller message sizes is latency dominated.

The other important factor for CC, available per-chip peak bandwidth, is summarized in Table VII. Note that Broadcom’s Tomahawk 4 switch chip supports an order of magnitude more bandwidth than any AI HW chip, demonstrating the headroom available to improve per-chip bandwidth for AI applications.

TABLE VII: HW communication peak bandwidth for various chips.

| Chip | Peak HW bandwidth, each direction, per chip |
|------|-------------------------------------------|
| CPU: Intel Xeon Platinum 8180 | 62GB/s UPI, 48GB/s PCIe aggregate [6], [22], [23] |
| GPU: NVIDIA A100 | NVLink3, 300GB/s [21] |
| FPGA: Achronix Speedster AC7i1500 | 400GB/s via 112G SerDes [18] |
| AI HW: Graphcore GC200 | 320GB/s via 10x IPU-Links [14] |
| AI HW: Intel/Habana Gaudi | 125GB/s via 10x 100GbE [25] |
| Network Switch: Broadcom Tomahawk 4 | 3,200GB/s [26] |

2) Memory System Performance: This section refers to external DRAM memory attached to an AI HW accelerator or CPU. RecSys applies considerable pressure on the memory system due to the large number of accesses to embedding tables. Furthermore, these accesses have limited spatial locality (but some temporal locality) [19], resulting in scattered memory accessed of 64B-256B in size [1] that exhibit poor DRAM page hit characteristics. Multiple ranks per DIMM and internal banks and bank groups per memory die help by increasing parallelism, within memory device timing parameters such as command issue rates and on-die power distribution limitations.

TABLE VIII: External Memory systems for select AI HW.

| Chip | Memory System |
|------|---------------|
| Intel Xeon CPU | DDR4, 6 channels for Xeon Gold, up to 1.5TB [5] |
| NVIDIA A100 | HBM, 5 stacks, 40GB total |
| NVIDIA TU102 | GDDR6, 11 chips, 11GB total |
| RTX2080Ti | DDR4, 2 channels, 16GB |
| Habana Goya | DDR4, 2 channels, 16GB |
| Graphcore GC2 | None, 300MB on-chip |
| Graphcore GC200 | 900MB on-chip, 2x DDR4 channels for 4 chips [13] |
| Cerebras CS1 | None, all memory is on-wafer, 18GB total |

Table VIII shows memory types for a few representative AI HW chips and Fig. 6 show achievable effective memory bandwidth for various memory system configurations and embedding sizes. HBM has considerably higher performance for random embedding accesses, while the typical 6-channel DDR4 server CPU memory system has far lower performance, especially for smaller embedding sizes. However HBM and GDDR6 suffer from limited capacity compared to DDR4 as shown in Fig. [7].

3) Compute Performance: Table IX shows available compute capability of various chips. For the specific workload that we analyze, compute capability is not a limiting factor (see Sec. V-A) and this is believed to be the case for many RecSys workloads when run on specialized AI accelerators [30].
Fig. 6: Peak Random Embedding Access Bandwidth for common memory systems based on memory timing parameters, assuming auto-precharge. Data transfer frequency shown; device clock is half for DDR4 & HBM, one-eighth for GDDR6. DDR4 memory systems have far lower performance than HBM for embedding lookups.

Fig. 7: Total capacity of common memory systems.

Table IX: Peak Compute capability of various chips.

| Chip                | FLOPS capability |
|---------------------|------------------|
| CPU: Intel Xeon Platinum 8180 | 4.1 TFLOPS FP32 [6] |
| GPU: NVIDIA A100   | 19.5 TFLOPS FP32, 32 TFLOPS FP16/32 [21] |
| FPGA: Achronix Speedster | 3.84 TFLOPS FP32, 750MHz [17], [18] |

Table X: Uses for on-chip buffer memory.

| Item                              | Buffering memory                                    |
|-----------------------------------|-----------------------------------------------------|
| Dense weights for data parallelism| Model-dependent, replicated across each chip        |
| Embeddings for one mini-batch     | Dependent on embedding table sizes, mini-batch size, and (temporal) locality across mini-batch |
| Working buffers for data transfers| Used to overlap processing and transfers for input features and embedding lookups |
| Data during training              | Activations, gradients, optimizer state [44], [52] |

4) On-Chip Buffering: Buffering memory serves several purposes as shown in Table XI. While some of these are straightforward to estimate—such as the number of weights in the dense layers of a model—others are harder to quantify, such as the number of unique embedding values across one or multiple mini-batches. Analyses by Facebook [19] indicate hit rates of 40% to 60% with a 64MB cache.

E. Improving existing AI HW accelerators for RecSys

Table XI: Improving existing AI HW accelerators for RecSys.

| Chip                | Potential Changes                                      |
|---------------------|--------------------------------------------------------|
| NVIDIA A100         | Increase on-chip memory for buffering; Add DDR memory support; Enable sixth HBM stack; support deeper stacks; reduce compute capability to fit die area budget |
| Graphcore GC200     | Add external high-speed DRAM support                    |
| Cerebras CS1        | Change from mesh to fully connected topology, Add external high-speed DRAM support |
| All of the above    | Increase I/O bandwidth; Add HW support for CC; Add dual external DRAM support (Sec. VII-A) |

Table XI illustrates potential changes to enhance the performance of existing AI HW accelerators on RecSys workloads.

V. PERFORMANCE MODEL

A. Representative DLRM Models

Our choice of representative model is Facebook’s DLRM-RM2 [30]. In order to reveal limitations of various HW platforms, two model configurations are analyzed. These are positioned at the low and high end of batch size and embedding entry size; specifically, 200 and 600 as the batch size points, and 64B and 256B as the embedding size points. We refer to the 200 batch size/64B embedding size combination as “Small batch/Small embeddings”, while the 600 batch size/256B combination is “Large batch/Large embeddings”.

Similarly, the two extremes of table distribution are analyzed. “Unsharded” refers to each table being able to fit within the memory attached to an AI accelerator, such that only pooled embeddings need be exchanged. “Sharded” refers to “full sharding” (see section IV-A) where each table is fully distributed across the attached memory of every accelerator—a worst-case scenario. The reality will likely fall between these two extremes.

Note that the same batch sizes are used for both our inference and training performance models and that all parameters are stored in FP16 for both inference and training. As the size of the tables for the production model is not publicly available, we assume that the model is large enough to occupy the memory of all chips in the system. This is a reasonable assumption based on other recommendation systems [7].

8 Roughly 200 is the median query size; 600 is significantly farther out in the query size distribution [30].

9 Facebook has noted that embedding sizes in bytes are typically 64B-256B [19].
TABLE XII: DLRM-RM2 configurations.

| Parameter                        | Value(s)               |
|----------------------------------|------------------------|
| Number of embedding tables       | 40                     |
| Lookups per table                | 80                     |
| Embedding size                   | 32 FP16 = 64B (small), 128 FP16 = 256B (large) |
| Number of dense features         | 256                    |
| Bottom MLP                       | 256-128-32-Embedding dimension |
| Top MLP                          | Interactions-512-128-1 |
| Feature Interactions             | Dot products, exclude diagonal |
| FLOPS/Inference                  | ~1.40 MFLOPS (small), ~2 MFLOPS (large) |
| Batch size                       | 200 (small), 600 (large) |

B. Overview of Performance Model

We have developed a performance model that computes the time, memory usage and communications overhead for each of the steps detailed in Sec. IV-C. Our model takes as input a specific DLRM configuration as described in Sec. V-A as well as various parameters that describe batch size, embedding table sharding, processing engine capabilities and configuration, memory system configuration, memory device timing parameters from vendor datasheets, communication network latencies and bandwidths, and system parameters that control the level of overlap and concurrency within the HW. In order to maximally stress the HW, our model assumes zero (temporal) locality within the embedding access stream.

Results are reported in Sec. VI for the stated configurations, assuming the HW and system exploit maximal overlap within a batch for inference by grouping memory accesses and overlapping memory activity with communications where possible, and for training by pipelining the collective communications with backpropagation computations and parameter updates. For embedding parameter updates during training, the originally looked up embeddings are buffered on-chip, thereby only requiring a write to update them instead of a read-modify-write. In particular, sufficient on-chip buffering to support the above capabilities is assumed—doing so over-estimates the performance capabilities of most current AI accelerator HW.

VI. Evaluation of System Performance

A. Systems Parameters

We focus our performance evaluation on homogeneous systems, where one type of processor provides the bulk of compute and communications capability.

Table XIII shows the range of parameters that we consider for our reference homogeneous system. In terms of CC performance, these ranges are, for the most part, significantly in excess of what is supported by state of the art AI HW accelerators. This is consistent with our goal of showing the benefit of further optimizing these parameters. In particular, the CC latency range is lower than measured numbers for NVIDIA’s DGX-2 system (Sec. VII-B). The range of per-chip bandwidth spans popular training accelerators as well as about 3× beyond NVLink3.

TABLE XIII: Ranges of Key Parameters for Homogeneous Systems.

| Parameter                        | Range                                               |
|----------------------------------|-----------------------------------------------------|
| CC all-to-all                     | Latency of 0.5μs to 10μs, Bandwidth 100 to 1000GB/s |
| CC all-reduce                     | Latency of 0.5μs to 10μs, Bandwidth 100 to 1000GB/s |
| Bandwidth per chip                | 100 to 1000GB/s aggregated across all links         |
| #chips/system                     | 8                                                   |
| Compute capability                | 200 TFLOPS FP16                                     |
| Memory system                     | 6 stacks of HBM2E per chip @ 2400 MHz               |

B. Inference

Fig. 8 shows upper bounds on achievable system throughput for inference. For the large batch, large embeddings case, unsharded, throughput is primarily limited by memory accesses for embeddings such that interconnect is of secondary importance. Such models would run well on existing systems including scale-out topologies with limited bandwidth.

Latency, as opposed to bandwidth, matters most for small batch/embedding workloads, as detailed in Fig. 9. For the unsharded case this sensitivity applies at high bandwidth as well as at low bandwidth, with throughput dropping by almost 5× as latency increases. This is not surprising since the typical all-to-all message sizes for this configuration are 320KB of indices per processor and 64KB for pooled embeddings, small messages that would typically fall within the latency-dominated regime of CC.

This would indicate that when batch sizes are relatively small and tables are allocated to each fit within the memory attached to each processor, it is more important to design systems to minimize latency as opposed to pushing per-chip bandwidth. Scale-out architectures, with multiple interconnect hops and long physical distances, make this difficult. On the other hand, “scale-in” system design can help reduce latency.

The sharded, small batch/embeddings case is sensitive to both latency and bandwidth since the exchange of unpooled embeddings results in an all-to-all message size of ~5.2MB per processor. However, even in this situation, there is limited benefit in improving bandwidth unless such improvement is also accompanied by reduced latency.

The unsharded, large batch/embeddings case is very slightly sensitive to latency and largely insensitive to bandwidth. This is because the communication volume, compared to the unsharded small batch/embeddings case, increases by 3× for indices and by 12× for embeddings; the resulting message sizes are still typically within the latency-dominated region of CC. However, the number of bytes of memory lookups for embedding tables increases by 12× such that memory lookup time becomes the dominant term.

The sharded, large batch/embeddings case depends on both latency and bandwidth due to the larger message sizes from exchanging unpooled embeddings.
In all cases, higher bandwidth minimizes the throughput impact of sharding. As shown in Fig. 10, increasing bandwidth from 100GB/s to 1000GB/s reduces the impact of full sharding from about $3.1 \times$ loss down to $1.2 \times$ for the small batch/embddings case. Similarly significant gains are seen for the large batch/embddings case with sharding.

**C. Training**

Fig. 11 shows upper bounds on achievable system throughput for training. Similarly to inference, we note that the case of unsharded large batches/embeddings is primarily memory-bound, hence does not depend much on CC latency or bandwidth.

For the other configurations, compared to inference, the importance of optimizing bandwidth and latency are more balanced for training. For the small batch/embeddings case, bandwidth matters to training QPS as detailed in Fig. 12. High bandwidth cuts dense all-reduce times since the message sizes involved are $\sim 2.4$MB per processor; the impact of bandwidth is, as expected, most felt at latencies under $4 \mu$s.

As with inference, higher bandwidth helps mitigate the throughput penalty of sharding. In the large batch/embeddings scenario, overall throughput increases almost proportionally with bandwidth as shown in Fig. 13. The all-to-all exchange of unpoole embeddings between processors dominates, with message sizes of $\sim 60$MB per processor.

**VII. RecSpeed: An Optimized System Architecture for RecSys**

This section describes the features of RecSpeed, a hypothetical system architecture for RecSys workloads. The objectives of RecSpeed are to:

- Maximize throughput for inference and training of large RecSys models;

![Fig. 8: Inference performance upper bounds as a function of Collective Communications latency and bandwidth for small/large batches, with and without Sharding. See text for analysis.](image-url)
Fig. 9: Impact of latency on QPS for small batch size, small embedding vectors, Unsharded. Latency matters at both high and low bandwidth, and there is benefit in driving CC latency down to typical network switch port to port levels.

Fig. 10: High Bandwidth helps minimize the performance loss from sharding, even at high latency, due to the all-to-all exchange of unpooled embedding entries between processors.

- Support future, ever-larger RecSys models;
- Allow implementation using existing process technologies, and to fit into common datacenter power envelopes;
- Support existing SW and HW interfaces for datacenter AI server racks.

A. RecSpeed Architecture Features

Fig. 14 shows a sketch of the proposed chip and interconnect structure for a 6-chip RecSpeed system. Key features of the architecture are as follows:

- Fixed-topology quadratic point-to-point interconnect without any form of switching to minimize latency.
- HW support for Collective Communications to minimize synchronization and SW-induced latency.
- Fast HBM memory attached to each chip, as many stacks as practical; as of the writing of this paper, NVIDIA’s A100 has room for 6 stacks of HBM (of which only 5 are used), each 4-deep; however, 8-deep stacks are available.
- Slow bulk memory, such as DDR4.
- Optimized packaging and system design to allow “scale-in”, packing as many RecSpeed chips as possible in close physical proximity.

High-density physical packaging of chips is particularly important in order to achieve maximum throughput; when interconnect moves from intra-board to the system level, the energy consumed per bit goes up by 25×, bandwidth falls by over 20×, and overhead increases markedly [29].

Fixed-topology vs. switched all-to-all interconnect: The proposed interconnect for RecSpeed could reduce latency compared to the all-to-all switched interconnect found in NVIDIA’s DGX-2 [9] or Habana’s HLS-1 training system [25]. Specifically, the presence of a switch introduces several hundred nanoseconds of additional latency [45] [46]. A quadratic interconnect offers performance gains of 2.3× for large CC all-to-all messages on an 8-node system, compared to a ring interconnect, and for smaller message sizes the gain can range as high as 15× [10].

HW support for CC: We note that the proposed interconnect structure can efficiently support both CC all-to-all and all-reduce operations with minimal latency and bandwidth usage that matches the theoretical lower bound [8].

Implementing High-Bandwidth Links: The proposed high-bandwidth RecSpeed links can be implemented via existing technology, amounting to ∼31% of the bandwidth of a Tomahawk 4 switch chip [26].

Hybrid Memory Support: Certain embedding tables and vectors are accessed less often than others [7]. It is therefore useful to provide a two-level memory system, with large bulk memory in the form of DDR4 combined with fast HBM memory. Tables can be allocated to one memory or the other statically—sharded or not—or the faster HBM can be used as a cache. Static allocation is preferred, as dealing with such a large cache structure where the smaller memory has latency comparable to that of the larger memory may not offer much benefit, based on prior efforts such as Intel’s Knights Landing HPC architecture [47]. With the configuration shown, up to
5.5TB of memory can be provided for a RecSpeed system, of which 27% would be fast HBM. Baidu reports that their AIBox [7] system is able to effectively hide storage access time, despite the two order of magnitude latency difference and the greater than one order of magnitude bandwidth difference between SSD and main memory. Since the performance gap between DDR and HBM memory is smaller, it is reasonable to assume that careful system design can enable a hybrid memory system to run closer to the performance of a full HBM system.

B. RecSpeed Performance vs. DGX-2

Table XIV shows the system characteristics that we use for computing the performance upper bound for RecSpeed, and Table XVI for the DGX-2. Note that we assume a “modified” V100 chip with more on-chip buffering memory than the actual V100.

The resulting throughput numbers and comparison versus NVIDIA’s DGX-2 estimated upper bounds are shown in Table XVI for inference and Table XVII for training. In our
model, the DGX-2 is largely bound by its high CC latency, which can likely be reduced via software optimization.

**Limitations:** In this section, we do not discuss trade-offs and issues—important as they may be—relating to die size, power, and thermal design.

**Conclusion**

This paper reviews the features of a representative Deep Learning Recommender System and describes hardware architectures that are used to deploy this and similar workloads. The performance of this representative Deep Learning Rec-

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**TABLE XV:** Numbers used for NVIDIA DGX-2 performance upper bounds.

| Parameter                      | Value        |
|--------------------------------|--------------|
| CC all-to-all                  | Derived from CC all-gather [12] |
| CC all-reduce, CC all-gather   | Data from [12] |
| Memory System                  | HBM2, 4 stacks @ 2300MHz |
| Bandwidth per chip             | 150GB/s      |
| #chips/system                  | 16           |
| Compute capability             | 125 TFLOPS FP16 |
| On-chip memory                 | Assumed sufficient—not the case in practice |

---

**TABLE XVI:** RecSpeed Inference Upper Bounds.

| Config      | QPS Mem. DGX-2 Potential | Util. QPS Mem. Speedup |
|-------------|---------------------------|------------------------|
| Sm. Unshard | 300K 67% 4.9K 1.8%        | 45×                    |
| Sm. Shard   | 207K 47% 4.5K 1.6%        | 46×                    |
| Lg. Unshard | 56K 93% 4.7K 15%          | 12×                    |
| Lg. Shard   | 30K 50% 2.1K 7%           | 14×                    |

All-reduce refers to dense reduction and update.

---

**TABLE XVII:** RecSpeed Training Upper Bounds.

| Config      | QPS Allred. DGX-2 Potential | %Time QPS Allred. | Util. DGX-2 Allred. Speedup |
|-------------|-----------------------------|-------------------|-----------------------------|
| Sm. Unshard | 99K 33% 2.2K 31%            | 45×               |
| Sm. Shard   | 83K 28% 2.1K 30%            | 39×               |
| Lg. Unshard | 25K 9% 2.1K 28%            | 12×               |
| Lg. Shard   | 16K 6% 1.2K 18%            | 13×               |

All-reduce refers to dense reduction and update.
ommender is investigated with respect to its sensitivity to hardware system design parameters for training and inference.

We identify the latency of collective communications operations as a crucial, yet overlooked, bottleneck that can limit recommender system throughput on many platforms. We also identify per-chip communication bandwidth, on-chip buffering and memory system lookup rates as further factors.

We show that a novel architecture could achieve substantial throughput gains for inference and training on recommender system workloads by improving these factors beyond state of the art via the use of “scale-in” to pack processing chips in close physical proximity, a two-level high-performance memory system combining HBM2E and DDR4, and a quadratic point-to-point fixed topology interconnect. Specifically, achieving CC latencies of 1µs and chip-to-chip bandwidth of 1000GB/s would offer the potential to boost recommender system throughput by 12–62× for inference and 12–45× for training compared to upper bounds for NVIDIA’s DGX-2 large-scale AI platform, while minimizing the performance impact of “sharding” embedding tables.

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APPENDIX

STEPS AND OPERATORS FOR DLRM

This appendix presents a high-level algorithm representing the steps for training a DLRM model in a distributed fashion with $n$ identical processors. The forward pass is covered in algorithm 1 (used in both inference and training, note that for training it is assumed that activations are checkpointed as needed and optimally \[7\] to facilitate backpropagation) and the backward pass and weight update in algorithm 2. Note that most operations are performed concurrently across all processors as the inference query or training batch is split up across all $n$ processors. For simplicity, it is also assumed that the concatenation of the bottom MLP output and the pairwise dot products (after duplicate removal, diagonal removal, and vectorizing is completed) is performed as part of the FeatureInteractions operation.

For training, the optimizer used is vanilla SGD. AdaGrad is reported to achieve slightly better results for DLRM on the Criteo Ad Kaggle dataset \[34\], however we use vanilla SGD in our steps and performance model for consistency with the DLRM repo. The pipelining during the dense backward pass of collective communications (i.e. all-reduce operations) with the backpropagation computations and parameter updates is not shown; in practice, this is certainly feasible as long as the all-reduce latency is acceptable.

The notations used are shown in Table XVIII.

Other operations

This section introduces additional operations (other than collective communications operations) mentioned in algorithms 1 and 2.

**FC:** The forward pass of the FC layer.

**FeatureInteractions:** The forward pass of the dot-product feature interactions layer with exclusion of the diagonal feature interactions matrix entries.

**Concat:** The concatenation operation of the batched bottom MLP output and batched pooled embedding vectors along a new dimension as mentioned in Sec. III-D.

**FCBackward:** This operator takes in the gradient of the loss with respect to the output of a given FC layer, uses the checkpointed input activations to the layer, and returns both the gradient of the loss with respect to the weights of the layer as well as the gradient of the loss with respect to the input to the layer. This will then be used by the next FCBackward operator.

**FeatureInteractionsBackward:** This operator takes in the gradient of the loss with respect to the output of the feature interactions layer and returns the gradient of the loss with respect to each of the batched inputs to the feature interactions layer, which are the output of the bottom MLP as well as the pooled embeddings resulting from the embedding lookups in the model. Note that there are no weights in the feature interactions layer so this is sufficient for FeatureInteractions-Backward.

**Expand_sparse_grads:** Because of pooling in this model, all of the gradients on embeddings that are pooled into a single output are identical. After communicating only the gradients on the pooled vectors, these values are simply “expanded”, or copied, to every unpooled vector that was summed to generate the pooled vector. This operation also averages the gradients on the pooled vectors, these values are simply “expanded”, or copied, to every unpooled vector that was summed to generate the pooled vector. This operation also averages the gradients on the pooled vectors across the batch.

**Params:** Shorthand operator to denote the parameters associated with a given FC layer or embedding table.

| Symbol | Usage | Meaning |
|--------|-------|---------|
| $n_d$  | Constant | Number of dense features in the model |
| $n_c$  | Constant | Number of sparse features or embedding tables |
| $c_i$  | Constant | Cardinality of the $i$th categorical feature |
| $l_i$  | Constant | Number of lookups performed on the $i$th embedding table |
| $l_b$  | Constant | Number of bottom MLP layers |
| $l_t$  | Constant | Number of top MLP layers |
| $d$    | Constant | Embedding dimension |
| $O_B$  | Fwd   | Output of bottom MLP up to a given layer |
| $L_i$  | Fwd   | Local embedding lookup indices for $i$th table after indices all-to-all |
| $O_E$  | Fwd   | Local embedding lookup vectors (possible pooled) |
| $V_i$  | Fwd   | Pooled embedding vectors (after second all-to-all) resulting from lookups for the $i$th table |
| $F$    | Fwd   | Feature interactions input denoted as $A$ in feature interactions layer description of Sec. III-D |
| $O_T$  | Fwd   | Output of bottom MLP up to a given layer |
| $G_{T_i}$ | Bckwd/update | Gradient of loss w.r.t. output of $i$th top MLP FC layer |
| $G_{B_i}$ | Bckwd/update | Gradient of loss w.r.t. output of $i$th bottom MLP FC layer |
| $G_{E_i}$ | Bckwd/update | Pooled gradient (i.e. on processor which doesn’t own relevant embeddings) of loss w.r.t. lookups from $i$th embedding table |
| $L_{E_i}$ | Bckwd/update | Pooled gradient of loss w.r.t. lookups from $i$th table on processor which owns relevant embeddings after all-to-all/all-gather |
| $F_{GE_i}$ | Bckwd/update | Unpooled/expanded batch-reduced gradient of loss w.r.t. lookups from $i$ table on processor which owns relevant embeddings after all-to-all/all-gather |
Algorithm 1: DLRM forward pass steps.

**Input:** Number of processors $p$; $b \times n_d$ batch of dense features $D$; $n_c$ sets of sparse features each one called $S_i$, each one $b \times l_i$; bottom MLP layers $FC_{B_i}$, $i \in [1, l_b]$; top MLP layers $FC_{T_i}$, $i \in [1, l_t]$; $n_c$ embedding tables denoted as $E_i$ with each table representing a $c_i \times d$ matrix.

$O_B \leftarrow D$

for $i = 1 \cdots l_b$
  $O_B \leftarrow FC_{B_i}(O_B)$
end

$L_1, L_2, \cdots, L_{n_c} \leftarrow all_to_all([S_1, S_2, \cdots, S_{n_c}])$

$O_E \leftarrow []$

for $j = 1 \cdots n_c$
  $O_{E_j} = E_j(L_j)$
  if no_sharding then
    $O_{E_j} = pool(O_{E_j})$
  end
  $O_E.append(O_{E_j})$
end

if full_sharding then
  $V_1, V_2, \cdots, V_{n_c} \leftarrow reduce_scatter(O_E)$
end

if no_sharding then
  $V_1, V_2, \cdots, V_{n_c} \leftarrow all_to_all(O_E)$
end

$F \leftarrow \text{concat}([O_B, V_1, V_2, \cdots, V_{n_c}])$

$F' \leftarrow \text{FeatureInteractions}(F)$

$O_T \leftarrow F'$

for $i = 1 \cdots l_t$
  $O_T \leftarrow FC_{T_i}(O_T)$
end

$p \leftarrow O_T[:, 0]$

**Output:** Predicted click probabilities vector $p$

Algorithm 2: DLRM backward pass and weight update steps.

**Input:** Number of processors $p$; $b \times n_d$ batch of dense features $D$; $n_c$ sets of sparse features each one called $S_i$, each one $b \times l_i$; bottom MLP backward operators $FC_{Backward_{B_i}}$, $i \in [1, l_b]$; top MLP backward operators $FC_{Backward_{T_i}}$, $i \in [1, l_t]$; $n_c$ embedding tables denoted as $E_i$ with each table representing a $c_i \times d$ matrix. Learning rate $\gamma$; predictions $p \in (0, 1)^n$; labels $l \in [0, 1]^n$; loss function $\mathcal{L}(p, l) = \frac{1}{n} \sum_{i=1}^{n} l_i \log p_i + (1 - l_i) \log (1 - p_i)$

$L_{BCE} \leftarrow \mathcal{L}(p, l)$

$\nabla_p \mathcal{L} \leftarrow \frac{1}{n} \sum_{i=1}^{n} \left( \frac{l_i}{p_i} - \frac{1 - l_i}{1 - p_i} \right)$

$GT_{t+1} \leftarrow \nabla_p \mathcal{L}$

for $i = l_t, l_t - 1, \cdots, 1$
  $GT_i, \nabla_{FC_{T_i}} \mathcal{L} \leftarrow FC_{Backward_{T_i}}(GT_{i+1})$
end

$GB_{l_b+1}, GE_1, \cdots, GE_{n_c} \leftarrow \text{FeatureInteractionsBackward}(GT_1)$

if no_sharding then
  $LGE_1, \cdots, LGE_{n_c} \leftarrow all_to_all([GE_1, \cdots, GE_{n_c}])$
end

if full_sharding then
  $LGE_1, \cdots, LGE_{n_c} \leftarrow all_gather([GE_1, \cdots, GE_{n_c}])$
end

$FGE_1, \cdots, FGE_{n_c} \leftarrow \text{expand_sparse_grads}([LGE_1, \cdots, LGE_{n_c}])$

for $i = l_b, l_b - 1, \cdots, 1$
  $GB_i, \nabla_{FC_{B_i}} \mathcal{L} \leftarrow FC_{Backward_{B_i}}(GB_{i+1})$
end

$GB_1, GB_2, \cdots, GB_{l_b}, GT_1, GT_2, \cdots, GT_{l_t} \leftarrow \frac{1}{p_t} \text{all_reduce}([GB_1, GB_2, \cdots, GB_{l_b}, GT_1, GT_2, \cdots, GT_{l_t}])$

for $i = 1 \cdots l_t$
  $\text{Params}(FC_{T_i}) \leftarrow \text{Params}(FC_{T_i}) - \gamma \nabla_{FC_{T_i}} \mathcal{L}$
end

for $i = 1 \cdots l_b$
  $\text{Params}(FC_{B_i}) \leftarrow \text{Params}(FC_{B_i}) - \gamma \nabla_{FC_{B_i}} \mathcal{L}$
end

for $i = 1 \cdots n_c$
  $\text{Params}(E_i) \leftarrow \text{Params}(E_i) - \gamma FGE_i$
end

**Output:** Current loss $L_{BCE}$