High Speed and Low Power Sensing Schemes for STT-MRAM with IPMTJs

Mesut Atasoyu, Mustafa Altun, Serdar Ozoguz

Abstract—STT-MRAM with interfacial-anisotropy-type perpendicular MTJ (IPMTJ) is a powerful candidate for the low switching energy design of STT-MRAM. In the literature, the reading operation of STT-MRAM structured with IPMTJs have been not studied until this time, in our knowledge. We investigated the reading operation of STT-MRAM structured with IPMTJs. To enumerate the read operations of the NVSenseAmp have successfully been performed a 2.5X reduction in average low power and a 13X increase in average high speed compared with the previous works.

Index Terms—STT-MRAM, IPMTJ, sensing, BER, low-power, high-speed.

I. INTRODUCTION

Recent developments in scalability of the spin-transfer torque magnetic RAM (STT-MRAM) have led to a renewed interest in a promising nonvolatile memory solution due to its CMOS compatibility, low power and high-speed operations, and especially high endurance [1]. In the STT-MRAM technology, a magnetic tunnel junction (MTJ) is used as a storage element. Information is encoded in a MTJ as a high (AP) or low (P) resistance state based on the relative magnetization directions of the ferromagnets constituting the device. In read operations of STT-MRAM, tunnel magnetoresistance ratio (TMR) is used to distinguish the RAP and RP states from each other. On the other hand, during the write operations, the switching threshold current (IC) of a MTJ is an important parameter determining the current required to easily switch between the RAP and RP states. Low values of IC are obtained while MTJ dimensions are scaled down. However, scaling down the dimensions of MTJ has its own drawbacks. These drawbacks often cause a read disturbance (RD) and incorrect decisions because of low sensing margin (SM) [1]. This is because, while low IC is required for low power and low area overhead, it can lead to RD because the minimum reading current (IRD) might be close to IC. To successfully avoid RD, IRD must be less than 20% of IC. The SM issues originate in CMOS technology as a process, supply voltage, and temperature variations, and mainly variations of the oxide thickness (TOX) in MTJ technology. In particular, the large TMR will be chosen to increase the SM. Interfacial-anisotropy-type perpendicular MTJ (IPMTJ) have large TMR values such as TMR ratio of 248% [2], low resistance-area (RA), and high thermal stability. Importantly, IPMTJs consume low switching energy [2]. Note that there is a trade-off between the RD and the SM required IRD [3]. A low value of IRD is better for RD rather than the SM. The previous works on the sensing scheme of STT-MRAM have highlighted several sensing approaches that are structured in the self-reference cells [4], two transistors and two MTJs cells [5], the dynamic data dependent reference cells [6], [3], [7] and the only RP reference cells [8]. These works are aimed to address the vulnerabilities of a sensing scheme, and especially to increase the low SM. However, using simple current mirror circuitry in the sensing schemes [3], [8], [7] can address the vulnerability of a sensing scheme. The dynamic data dependent sensing schemes [6], [3], [7] are a good solution to increase the SM and to decrease bit error rate (BER). However, the power consumption of the sensing scheme will be increased because of utilization of two latch based sense amplifier (SenseAmp) or differential amplifier for RAP and RP states. Although the realization of STT-MRAM cell arrays with two transistor and two MTJs succeeds to increase the low SM, it proves to be detrimental in terms of low cost and low area [5]. To emphasize, multiple SenseAmps can be used to decrease readout delay time [9], at the same time to increase the decision circuity (DC) sensitivity, which is composed of cross-coupled inverter pairs in the sensing structure [6]. Lowering DC sensitivity will increase the BER. Reducing the secondary noise effects on the DC such as capacitive couplings (CCs) and hysteresis noises improves BER performance. However, investigations have been relatively scarce [10] with respect to these secondary noise effects on the DC. In addition most of the works have been focused on improving low SM by increasing the voltage or the current difference between the selected cell and the reference cell. It is important to note that the debate over the offset-aware design of a sensing scheme comes into conflict between a low power design or very precise design because of a trade-off between the power and the offset [9]. In this brief, we explore the possible difficulties of a sensing scheme for the STT-MRAM structured with IPMTJs. Meanwhile, we assumed these devices have 1nm oxide thickness (TOX) and low resistance-area product RA. The thin (TOX) values will increase the BER because of the high resistance variation of the IPMTJ devices. To improve the BER result of the STT-MRAM structured with IPMTJ, we investigated a possible BER performance improvement on the STT-MRAM structured with IPMTJ by increasing the sensitivity of the DC while reducing these noise effects. Also, we review both the voltage mode SenseAmp (VSenseAmp) and the current mode SenseAmp (CSenseAmp) in terms of their decision failure rates (BER). At the same time we compared the VSenseAmp and the CSenseAmp in terms...
of their high-speed reading operations under high threshold voltage \(V_{TH}\) variations of the transistors in the CMOS deep submicron technologies (i.e., 65m, 45nm). In the point of view, VSenseAmp is robust than CSenseAmp in terms of high speed operation \[11\] when they are designed in these technologies. To clarify, for this comparison, the VSenseAmp is adopted \[8\] and the CSenseAmp is designed similar to \[8\]. In addition, the clamped reference circuitry of the CSenseAmp and the VSenseAmp are not self biased because high resistance variations in IPMTJ devices are not preferred to use as a voltage or current reference source differently than \[8\]. By extension, in our proposed SenseAmps, the reference cells of STT-MRAM are set to the only \(R_p\) states due to their lower resistance variation than \(R_{AP}\) state \[8\]. Moreover, we used three serially stacked IPMTJ expanding their area three times bigger (3S) than their normal size (S) to ensure the RD protection of reference cells with low cost \[12\]. In this approach, without doubt, the increased \(I_C\) of the reference cells provides the RD protection on these cells \[12\]. Since each design approach has its pros and cons, we checked the impact of this design approach on the BER results. Because, one of the key ideas of this work is BER performance degradation or improvement with specified techniques. The second is low power STT-MRAM by using IPMTJ devices. The last one is high speed reading operation by reducing the effects of secondary noise sources. Specifically, applying the clamped reference capacitive neutralization technique (CRCNT) to reduce the impacts of CCs on the DC, will be discussed later. In conclusion, our contributions: 1) We firstly report the sensing schemes for the STT-MRAM structured with IPMTJs. 2) We attempt speed comparisons taking into account BER results between VSenseAmp and CSenseAmp. 3) We assess the significance of CCs and hysteresis noise effects on BER performance. In our belief, low power and high-speed sensing scheme design efforts will be pursued with the renewed size dimensions of the MTJ devices decreasing below 20nm. In fact, it is impossible to cover all specifications in a singular design approach. In this brief, the rest of the paper is prepared as follows: Section II studies the design aspects of the proposed VSenseAmp, Section III shows the results and their effects on the key design metrics, Section IV concludes this brief.

II. THE EVOLUTION OF THE NVS\textsc{SenseAmp}

A SenseAmp in STT-MRAM converts resistive information to digital information during reading phases. A latch type SenseAmp is widely used due to its positive feedback mechanism. Reading phases in the proposed SenseAmps are carried out in three phase: pre-charge, evaluation, and decision. Our timing strategy for the proposed SenseAmps is adopted \[8\] and our clock signals are SAE, SAE1, and WL. In the pre-charge phase, the memory cells or the reference cells are activated through word lines (WLs), and then both BLs and REFLs are pre-charged to \(V_{DD}\) equalizing via \(M_0\) to provide same delays among the BLs and the REFLs. In the evaluation phase, the proposed SenseAmps are activated with SAE and disconnected from cell arrays via SAE1. And then seen a differential voltage at the output nodes of the proposed SenseAmps (SAOUT, SAOUTB). Finally, this differential output voltage is amplified by the DC via its high gain positive feedback mechanism and then converted to digital signal. A VSenseAmp takes more time than a CSenseAmp because of longer discharging time of BL capacitance (\(C_{BL}\)) or REFL capacitance (\(C_{REFL}\)). In particular, the readout speed of the VSenseAmp is faster than the CSenseAmp when the variation of \(V_{TH}\) is higher than 12mV \[11\]. The variations of \(V_{TH}\) are 30mV or more in deep submicron technologies. In our simulations, we used TSMC 65nm CMOS model parameters and the MTJ model from \[13\]. Particularly, some essential parameters are listed as follow: power supply (\(V_{DD}\)) is 1.0V, the dimensions of IPMTJ are 40(width)x 40(length)x 1(oxide thickness)nm \(^3\). In addition, the process variations of MTJs and CMOS are used 2\% (3\%), and specified using TSMC 65nm CMOS model. Our proposed VSenseAmp with CRCNT, that is, the NVSenseAmp with only \(R_p\) reference cells, as shown in Fig.1. The activation orders for the stages in the proposed SenseAmps are shown in Fig.2. Firstly, the WL is activated at 0ns with 1ns of pulse width. Secondly, the SAE is activated at 0.5ns with 0.5ns of pulse width. Thirdly, the SAE1 is activated at 0.75ns with 0.25ns of pulse width. The output signals of the NVSenseAmp for the \(R_{AP}\) and \(R_p\) states are shown in Fig.2.

A. The Hysteresis Effects

The sensed data which is previously stored in parasitic capacitances, mainly \(C_{GD}\) of the SAOUT and SAOUTB nodes of the proposed SenseAmps, and this previous stored data causes hysteresis effects. Furthermore the hysteresis effects causes the sensing errors when the recovery time of the DC is inefficient. As a solution, we propose a technique which
the SAOUT and SAOUTB nodes are directly connected to the drains of MC and MR (the clamped reference transistors) to reduce the effects of $C_{GD}$ on these nodes, respectively. We tested the recovery time of the NVSenseAmp. Regarding the test configuration, we assumed that the load capacitances of NVSenseAmp are initially set at 0V or $V_{DD}$ to stimulate these effects on the SAOUT and SAOUTB nodes. As a result, we obtained the same BER or failure rates, for the NVSenseAmp, by taking into account the hysteresis effects.

B. The Capacitive Couplings Effects on the Clamped Reference

The main function of clamped reference circuitry (MC and MR) is that it provides both overcurrent protection and an inequality between BLs and REFLs to easily distinguish a $R_P$ state when the data and the reference cells are the $R_P$ state. Meanwhile, the MC and MR are biased at $V_C = 0.8$ and $VR = 0.7$ values that are chosen for the optimal BER via the parametric analyzes. However, these clamped reference transistors will be driven in the deep triode region to optimize the BER, so that the values of VC and VR can be chosen as high as possible. The output nodes (SAOUT and SAOUTB) of SenseAmps have large output swings. These variations cause a voltage disturbance in the gate of the clamped reference transistors (MR and MC) and current accuracy errors in the read current through CCs. The main CCs on the DC of the CSenseAmp and the NVSenseAmp are shown in Fig.3a and Fig.3b, respectively. CRCNT is realized through C1 and C2 MOS capacitances to minimize the effects of CCs, as shown in Fig.1. The CRCNT works as a capacitive voltage divider between a BL and a REFL to balance the read and the reference cell currents. In addition, the values of $C_{GD}$ vary the width and length of a MOS transistor. Therefore the size of the MOS capacitances (C1 and C2) should be chosen the same as MC and MR. It is important to note that currents of BLs and REFLs can be balanced together with these capacitances, as formulated in Eq.1-2. Indeed, The reduced effects of CCs can boost the high-speed operation of the NVSenseAmp.

$$\frac{V_{SAOUT} - VC}{V_{SAOUT} - V_{SAOUTB}} = \frac{C_{GDC}}{C_1 + C_{GDR}}$$ (1)

$$\frac{V_{SAOUTB} - VR}{V_{SAOUT} - V_{SAOUT}} = \frac{C_{GDR}}{C_2 + C_{GDC}}$$ (2)

C. Power Comparisons

Our proposed SenseAmps are structured dynamically. The power dissipation is mainly determined by the duty cycle and voltage swings on the BLs and REFLs, as formulated in Eq.3.

$$P_{dyn} = \alpha(\text{activity})x\text{C}_{\text{total}}x\text{V}_{\text{swing}}xV_{DD}xf$$ (3)

Firstly, the DC is a power hungry unit needs to effectively disconnected during read cycles to advance the power performance of the proposed SenseAmps. The disconnection of the DC is controlled by SAE1. We analyzed possible timing strategies of SAE1 as given following approaches: First, SAE1 is taken the same as SAE, second SAE1 is taken after the SAE with one or two inverter delays. However, we did not find the improved solution different than [8]. Thirdly, we applied CRCNT to reduce the effects of parasitic capacitances. The reading current of the CSenseAmp is less than both the VSenseAmp and the NVSenseAmp. The NVSenseAmp or the VSenseAmp with the multiple reference cells in the $R_P$ state have almost the same power dissipation as they are configured with single reference cell in the $R_P$ state, indicated in Table I. As a result, the power dissipation is the lowest in the CSenseAmp, and the highest in the NVSenseAmp. However, the output voltage of the NVSenseAmp has not rail to rail voltage swings, so will be provided by taking the outputs of the NVSenseAmp after an inverter stage but the given power results of the NVSenseAmp will be increased. We compared the power dissipation (at 66.7MHz) of the some previous works and the NVSenseAmp. Our proposed design has less power dissipation than these previous works, as shown in Fig.4. In addition, our power dissipation results are obtained through Monte Carlo simulations (with 1K samples), and separately for the $R_{AP}$ and $R_P$ states.
D. Readout Time Comparisons

The clamped bitline scheme can be used to reduce the readout delay of the proposed sensing schemes. The readout time of CSenseAmp is insensitive to $C_{BL}$. For this reason, in our simulations, we compared the readout time between the proposed SenseAmps for 50fF which is the predicted maximum $C_{BL}$ in sub memory cell arrays. Basically, the readout time depends on the transconductance of nmos transistors in DC and the load and parasitic capacitances of DC. Secondly, the readout time of VSenseAmp is sensitive to the discharging time of $C_{BL}$ and the voltage swing of BLs, on the contrary CSenseAmp. As a comparison, the NVSenseAmp and the VSenseAmp are faster than the CSenseAmp because of above 12mv threshold voltage ($V_{TH}$) values [11] in deep submicron technologies (in this design, 65nm). The NVSenseAmp is faster than the VSenseAmp with a single reference but slower than the VSenseAmp with multiple references because of the increased read current values of BLs. Importantly, the NVSenseAmp is less sensitive to the increased current of BLs due to CRCNT. However, these readout delay comparisons are not the same for the $R_{AP}$ and $R_{P}$ because of the asymmetric resistance distribution of $R_{AP}$ and $R_{P}$. In addition, the parasitic output capacitance value considering the total of $C_{GD}$ of the NVSenseAmp is greater than the CSenseAmp. As a reminder, the high speed operation will consume high power in terms of speed-power trade-off. As a result Table II shows the comparison of the readout time of the proposed designs. Fig. 5 shows the readout time comparisons of the previous works and the NVSenseAmp, our readout time value is a mean value obtained from Monte Carlo analysis (1K samples). As a conclusion, the NVSenseAmp has faster readout time among these compared works.

| Designs                          | $R_{P}$ | $R_{AP}$ |
|---------------------------------|---------|----------|
| The CSenseAmp with single reference cell | 656     | 707      |
| The VSenseAmp with single reference cell | 669     | 649      |
| The VSenseAmp with multiple reference cells | 167     | 151      |
| The NVSenseAmp with multiple reference cells | 271     | 244      |
| The NVSenseAmp with single reference cell | 270     | 244      |

E. The Resistance Variations

The resistance variations of the IPMTJs in our designs are 13% for both $R_P$ (the current value is 742Ω) and $R_{AP}$ (the current value is 1.97KΩ) associated with $t_{OX}$ (1nm) variations of 2% for $3\sigma$. These resistance variations are more than the variations of which are commonly taken as 5% and $3\sigma$ in previous works. Figure 6 shows the mean variations of $R_{AP}$ and $R_P$. Comparatively, their variations are close to each other despite their asymmetric structures.

F. The BER Comparisons

The effects of CMOS and MTJ process variations for the BER performance of the proposed SenseAmps were evaluated through Monte Carlo simulations with 1K samples. IPMTJ devices have high TMR values but the resistances of the IPMTJ cells are comparable with the resistance of the access transistors. However, the higher TMR values of IPMTJ devices will be better for SM and BER results [5]. To emphasize that the IPMTJ devices have the high TMR values with the values of $t_{OX} > 0.8nm$ but the TMR values change exponentially below the values of $t_{OX} < 0.8nm$ [14]. As a matter of fact our opinion is that difficult to find a optimum solution in terms of BER performance between $R_P$ and $R_{AP}$ states, as shown Table III. By comparison the CSenseAmp has lower BER performance for the $R_P$ state than the VSenseAmp or the NVSenseAmp, shown in Fig.7-8. The NVSenseAmp has the partially better BER performance among the other proposed SenseAmps.
TABLE III
BER COMPARISONS

| Designs                                      | \( R_P \) | \( R_{AP} \) |
|----------------------------------------------|-----------|-------------|
| The CSenseAmp with single reference cell     | 427       | 0           |
| The VSenseAmp with single reference cell     | 17        | 4           |
| The VSenseAmp with multiple reference cells  | 17        | 6           |
| The NVSenseAmp with multiple reference cells | 8         | 6           |
| The NVSenseAmp with single reference cell    | 2         | 8           |

![Fig. 7. Monte Carlo Simulations for P states a) The CSenseAmp b) The NVSenseAmp.](image)

![Fig. 8. Monte Carlo Simulations for P states a) The CSenseAmp b) The NVSenseAmp.](image)

III. CONCLUSION AND DISCUSSIONS

In this brief, we investigated the evolution of sensing schemes for STT-MRAM structured with IPMTJs. Moreover, we compared the proposed sensing schemes in terms of power, speed, and BER results. As a comparison the NVSenseAmp has a great advantage in sensing speed and a partial better BER performance among the other proposed designs that are the CSenseAmp and the VSenseAmp. However, the design of the NVSenseAmp or the VSenseAmp with multiple reference cells is a valuable solution for RD protection but degrades the BER performance of the NVSenseAmp or the VSenseAmp. Consequently, the proposed NVSenseAmp with single reference cell is a good solution for high-speed and low-power reading operations among the compared literature works. To enumerate the read operations of the NVSenseAmp have successfully been performed a 2.5X reduction in average low power and a 13X increase in average high speed compared with the previous works. STT-MRAM structured with IPMTJs as a remarkable candidate as a universal memory have its low switching energy. However, their accuracy rates are low and must be increased by developing new techniques. Our future work will be a design of offset reduction technique for the NVSenseAmp to improve the accuracy rates of NVSenseAmp.

ACKNOWLEDGMENT

This work is part of a project that has received funding from the European Union’s H2020 research and innovation programme under the Marie Skodowska-Curie grant agreement No 691178, and by the TUBITAK-BIDEB 2214/A.

REFERENCES

[1] X. Fong, Y. Kim, R. Venkatesan, S. H. Choday, A. Raghunathan, and K. Roy, “Spin-transfer torque memories: Devices, circuits, and systems,” Proceedings of the IEEE, vol. 104, no. 7, pp. 1449–1488, July 2016.
[2] N. Tezuka, S. Oikawa, I. Abe, M. Matsunari, S. Sugimoto, K. Nishimura, and T. Seino, “Perpendicular magnetic tunnel junctions with low resistance-area product: High output voltage and bias dependence of magnetoresistance,” IEEE Magnetics Letters, vol. 7, pp. 1–4, 2016.
[3] W. Kang, T. Pang, W. Lv, and W. Zhao, “Dynamic dual-reference sensing scheme for deep submicrometer stt-mram,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 1, pp. 122–132, Jan 2017.
[4] Y. Chen, H. Li, X. Wang, W. Zhu, W. Xu, and T. Zhang, “A 130 nm 1.2 v/3.3 v 16 kb spin-transfer torque random access memory with nondestructive self-reference sensing scheme,” IEEE Journal of Solid-State Circuits, vol. 47, no. 2, pp. 560–573, Feb 2012.
[5] J. W. Ryu and K. W. Kwon, “A reliable 2mtj nonvolatile static gain cell stt-mram with self-referencing sensing circuits for embedded memory application,” IEEE Transactions on Magnetics, vol. 52, no. 4, pp. 1–10, April 2016.
[6] C. Kim, K. Kwon, C. Park, S. Jang, and J. Choi, “7.4 a covalent-bonded cross-coupled current-mode sense amplifier for stt-mram with 11mtj coupled source-line structure array,” in 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, Feb 2015, pp. 1–3.
[7] X. Xue, Y. Fu, Y. Zhao, J. Xu, J. Yang, Y. Xie, Y. Lin, R. Huang, Q. Zou, and J. Wu, “Dynamic data-dependent reference to improve sense margin and speed of magnetoresistive random access memory,” IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, no. 2, pp. 186–190, Feb 2017.
[8] K. Tsuchida, T. Inaba, K. Fujita, Y. Ueda, T. Shimizu, Y. Asao, T. Kajiyama, M. Iwayama, K. Sugita, S. Ikegawa, T. Kishi, T. Kai, M. Amano, N. Shimomura, H. Yoda, and Y. Watanabe, “A 64mb mram with clamped-reference and adequate-reference schemes,” in 2010 IEEE International Solid-State Circuits Conference - (ISSCC), Feb 2010, pp. 258–259.
[9] D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, “A double-tail latch-type voltage sense amplifier with 18ps setup-hold time,” in 2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, Feb 2007, pp. 314–360.
[10] P. M. Figueiredo and J. C. Vital, “Kickback noise reduction techniques for cmos latched comparators,” IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 53, no. 7, pp. 541–545, July 2006.
[11] M. Sinha, S. Hsu, A. Alvandpour, W. Burleson, R. Krishnamurthy, and S. Borkar, “High-performance and low-voltage sense-amplifier techniques for sub-90nm smrams,” in IEEE International [Systems-on-Chip] SOC Conference, 2003, Proceedings., Sept 2003, pp. 113–116.
[12] M. Aoki, H. Noshiro, K. Tsunoda, Y. Iba, A. Hatada, M. Nakabayashi, A. Takahashi, C. Yoshida, Y. Yamazaki, T. Takenaga, and T. Sugii, “Novel highly scalable multi-level cell for stt-mram with stacked perpendicular mtjs,” in 2013 Symposium on VLSI Technology, June 2013, pp. T134–T135.
[13] X. Fong, S. K. Gupta, N. N. Mojumder, S. H. Choday, C. Augustine, and K. Roy, “Knack: A hybrid spin-charge mixed-mode simulator for evaluating different genres of spin-transfer torque mram bit-cells,” in 2011 International Conference on Simulation of Semiconductor Processes and Devices, Sept 2011, pp. 51–54.
[14] K. L. Wang, J. G. Alzate, and P. K. Amiri, “Low-power non-volatile spintronic memory: Stt-ram and beyond,” Journal of Physics D: Applied Physics, vol. 46, no. 7, p. 074003, 2013. [Online]. Available: http://stacks.iop.org/0022-3778/46/i=7/a=074003