A 2 GS/s 14-bit current-steering DAC in 65 nm CMOS technology for wireless transmitter

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Abstract: A 14-bit 2 GS/s current-steering digital-to-analog converter (DAC) for transmitter application has been fabricated in TSMC 65 nm CMOS technology. To obtain high linearity, the DAC is segmented as 5+9, where the 5-MSB bits are implemented in unary architecture and 9-LSB bits are implemented in binary architecture. The current source array utilizes the random switching scheme to suppress the graded error and symmetrical error caused by process or thermal gradient. In addition, the DAC’s dynamic performance is enhanced by adopting a digital pre-distortion algorithm and measurement results validate the proposed technique. The measured spurious free dynamic range (SFDR) before and after enabling pre-distortion scheme improves from 63.8 dBc to 70.0 dBc at 240 MHz output signal. Dual-tone and four-tone measurement results show that the DAC achieves the 3rd order intermodulation (IM3) lower than −64 dBc. The DAC occupies an active area of 0.19 mm² and consumes a total power of 490 mW from 1.3 V and 2.0 V supplies.

Keywords: DAC, digital pre-distortion, SFDR

Classification: Integrated circuits

References

[1] S. Spiridon, et al.: “A 375 mW multimode DAC-based transmitter with 2.2 GHz signal bandwidth and in-band IM3 < −58 dBc in 40 nm CMOS,” IEEE J. Solid-State Circuits 48 (2013) 1595 (DOI: 10.1109/JSSC.2013.2253219).

[2] M. Khafaji, et al.: “SFDR considerations for current steering high-speed digital to analog converters,” IEEE Bipolar/BiCMOS Circuits and Technology Meeting (2012) 1 (DOI: 10.1109/BCTM.2012.6352646).

[3] F.-T. Chou, et al.: “A compact 12-bit DAC with novel bias scheme,” IEICE Electron. Express 11 (2014) 20140572 (DOI: 10.1587/elex.11.20140572).

[4] P. Palmers and M. S. J. Steyaert: “A 10-bit 1.6-GS/s 27-mW current-steering D/A converter with 550-MHz 54-dB SFDR bandwidth in 130-nm CMOS,” IEEE Trans. Circuits Syst. I, Reg. Papers 57 (2010) 2870 (DOI: 10.1109/TCSI.© IEICE 2018
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1 Introduction

Digital-to-analog converter (DAC) is widely used in applications such as wireless communication, signal processing and instruments. Fig. 1 shows a typical block diagram of a direct transmitter [1].

DAC is usually the first analog block in the signal transmission chain, which often determines the performance of the overall transmitter, and becomes the bottleneck for the signal chain. In a typical wireless transmitter, the base-band signals are converted to analog signals by two DACs. Current-steering architecture may be the most suitable DAC architecture because it is inherently fast and can drive resistive load without using output buffer [2]. In this work, the current source array are arranged in random switching scheme to obtain high linearity. And the application of digital pre-distortion further improves the dynamic performance of the DAC.
2 DAC architecture

The current steering DAC works by “steering” current between a set of differential outputs. Current-steering DAC typically has three structures: binary weighted, thermometer decoded and segmented architecture. Table I lists the comparison of these three structures. Binary weighted DAC is simple and low power, however, with a poor monotonicity. Thermometer coded DAC mandates complex decoding circuit and results in large chip area and high power consumption. Segmented DAC combines the advantages of both architecture and can achieve high precision. Simultaneously, the segmented architecture highlights an optimum trade-off between accuracy and power consumption, which leads to a relative small chip area and moderate power consumption for DAC implementation.

| Specs        | Binary | Thermometer | Segmented |
|--------------|--------|-------------|-----------|
| DNL          | −      | +           | +         |
| Glitch       | −      | +           | +         |
| Monotonicity | −      | +           | +         |
| Power        | +      | −           | +         |
| Area         | +      | −           | +         |
| Complexity   | +      | −           | +         |

Fig. 2. The block diagram of a 14-bit current-steering DAC

In this paper, the proposed 14-bit current-steering DAC adopts segmented architecture, whose block diagram is shown in Fig. 2. The DAC circuit includes a thermometer decoder, a switch driver, a switch array and a current source matrix. The input of the DAC complies with the LVDS (low voltage differential signal) standard, which provides high digital input data rate. Furthermore, the 14 bit differential signal is split into 5 bits MSB and 9 bits LSB parts. The 5 MSB bits are encoded into 31 bits of thermometer code by a binary-to-thermometer decoder.
The 9 LSB bits are delayed by a series of buffers with an approximately equal delay to that of the decoder. The decoded signals are then synchronized by a group of flip-flops, which also shape the waveforms in an overlap fashion for the following block, the current switching cells. The switches turn on or off, alternating current from the current source array to either $I_{outp}$ or $I_{outn}$.

3 High speed and low spur switching current source

The current source is the crucial component of a current-steering DAC, which determines the static and dynamic performance of converters. For instance, the Integral Non-linearity (INL) is mainly decided by the matching between the current sources [3]. The spurious free dynamic range (SFDR) can be seriously degraded due to the switching voltage or current glitches from the current source array. In order to minimize these effects, we need to reduce undesired voltage or current variation during switching event. Therefore, a cascode current source and cascode switch structure is applied, as shown in Fig. 3.

![Fig. 3. The current cell with thick oxide layer cascoded switch transistor](image)

The cascode current source (M1, M2) is used to isolate actual current sources from the voltage fluctuations at the common node A. The cascode current source presents a high output impedance and improves linearity of the DAC. The maximum relative non-linearity of the DAC can be approximately expressed as [4],

$$\text{max. relative INL} = \frac{NR_L}{4r_o}$$  \hspace{1cm} (1)

Where $N$ is the resolution, $R_L$ is load resistance and $r_o$ is the output impedance of the unit current cell of the converter. In addition, the mismatch of current source is given by [5],

$$\frac{\sigma(I)}{I} = \sqrt{\frac{A_{ih}^2}{2WL} + \left(\frac{g_m}{I}\right)^2 \cdot \frac{A_{th}^2}{2WL}}$$  \hspace{1cm} (2)

Increasing the area of transistor can improve matching of the current sources with excessive chip area, which however may degrade dynamic performance of the DAC at high signal frequencies. So it is a trade-off in order to optimize DAC performance. To reduce the occupied chip area of the current source array, a large device overdrive voltage 435 mV of M1 is used, which support a 20 mA output full swing current with 3.2 µm/3 µm unit current cells.

Prior arts often use a pair of differential switches (M3, M4) to alternate the current between differential branches, which however suffers from charge feed-
through problem [6]. The feed-through is induced by the gate-drain capacitive coupling through each active switch, which results in undesired voltage fluctuations at the output terminals and seriously deteriorates the DAC dynamic performance.

![Graph](image)

**Fig. 4.** (a) Time-domain (b) Frequency-domain waveform for two different current sources at 240-MHz output signal

In order to improve DAC dynamic performance, cascode switches are employed to reduce the charge feed-through effect significantly by isolating the current switches from the output nodes of the converter, which reduces voltage glitches and increase switching speed as well. Moreover, thick oxide cascode switch (M5, M6) transistors are used to boost voltage headroom significantly with an increased supply voltage of 2 V. During operation, one of the cascode transistors could be off if no current flow through it, which could seriously impact DAC performance due to its low speed on-off switching, channel charging and discharging effect. To remove these effects, a pair of auxiliary current sources can be applied to maintain the cascode transistors in always on status at the cost of extra biasing current sources and increased power consumption. As shown in Fig. 4, this structure effectively reduces output glitch and improves dynamic performance compared with traditional structure.

### 4 DAC current source randomization

To implement the 5-bit thermometer-coded DAC, thirty-one current sources are arranged in a matrix. One of the design keys to a high performance DAC is to ensure the output current of each current source exactly same. A couple of factors would introduce the mismatches among current sources. First, there is voltage drop along the ground connection of current sources caused by non-uniform flowing current, which effectively modulates the bias voltage of the current sources and
presents linear gradient errors or quadratic errors depending on the ground connection style. Second, device mismatches due to different doping and oxide thickness over DAC chip could produce errors as well, often in approximately linear gradient fashion [7]. Third, non-uniform thermal distribution and stress inside the chip might also introduce approximately quadratic errors. In summary, the ultimate error distribution of the current cell matrix can be derived by superposing all these error components together, where graded and symmetrical errors tend to accumulate and result in a large integral linearity error.

Fig. 5. A possible switching sequence of random walk switching scheme

To compensate these errors, we should randomize the current source array (M1) in physical layout. There are thirty-one unary current sources in a 5-bit thermometer coded DAC, in which each unary current source consists of eight parallel elements. We adopt a jumping selection method to scramble the current source matrix as Fig. 5 illustrates. This scheme prevents the accumulation of residual systematic errors, averages random errors from current sources, and improves DAC’s INL/DNL. Surrounding dummy current sources are added to avoid boundary effects, which ensures that all active cells experience identical environment.

We have analyzed DAC’s INL performance in three layout arrangements: conventional sequential switching, centroid switching [8] and random walk switching, as shown in Fig. 6(a) and Fig. 6(b). The analytic results present linearity errors induced by graded error distribution and symmetrical error distribution respectively. We assume a peak-to-peak error $\varepsilon$ for these error distributions. When using conventional sequential switching scheme, large linearity errors are introduced by graded error. When using centroid switching scheme, large linearity errors are introduced by symmetrical error. When using random switching scheme, the linearity errors caused by symmetrical and graded errors can be suppressed. However, this layout scheme does increase wiring complexity and induce large parasitic capacitance due to longer interconnection, which could result in long settling time and degrade dynamic performance. Post-simulation does show 1 dB degradation of SFDR with negligible dynamic power consumption increase.
Fig. 7 exemplifies the layout techniques of the DAC, where the current source array occupies majority chip area with 0.18 mm² for a single channel DAC.

5 Digital pre-distortion

For a differential current-steering DAC, major distortion comes from its third harmonic distortion, determining DAC’s SFDR at a high-speed sampling frequency. When with differential mismatches, DAC’s SFDR could be dominated by the second harmonic HD2. Although a large device size and more sophisticated physical design techniques could be leveraged to further improve that, it is at the cost of circuit complexity and power consumption. Hence, we propose to use digital pre-distortion to minimize these harmonic distortions. Fig. 8 shows the block diagram of the digital pre-distortion calibration.

![Fig. 8. A block diagram of the proposed DAC pre-distortion scheme based upon off-line linearity measurements](image)
The algorithm compares the off-line measured analog output spectrum to the desired spectrum, compute corresponding calibration matrix, and then pre-distorts the digital input signals to achieve an optimum linearity performance. For simplicity, we neglect signal delay variation with frequency and assume an static, time invariant nonlinearity inside the DAC. In addition, we neglect the higher order nonlinearities. So the transfer function can be described by the equation:

\[ y(t) \approx a_1x(t) + a_2x^2(t) + a_3x^3(t) + \cdots \]  \hspace{1em} (3)

Where \( x(t) \) is the input and \( y(t) \) is the output signal, positive number \( a_1, a_2 \) and \( a_3 \) are the first-, second- and third-order coefficient respectively. When a sinusoid signal is applied to this nonlinear time-invariant system, the output contains components at integer multiples of the input frequency, that can be expressed as

\[ x_0 = \cos \omega t \]  \hspace{1em} (4)

\[ y_0 \approx m \left( \cos \omega t + \frac{a_2}{2m} \cos 2\omega t + \frac{a_3}{4m} \cos 3\omega t + \frac{a_2}{2m} + \cdots \right) \]  \hspace{1em} (5)

Here, \( m = a_1 + \frac{a_3}{4m} \). In the first iteration, the algorithm attempts to compensate the distortion by subtracting the unwanted component from the digital input signal, here mainly for the second harmonic:

\[ x_1 = x_0 - \frac{a_2}{2m} \cos 2\omega t \]  \hspace{1em} (6)

When this new signal \( x_1 \) passes through the DAC, the output is determined by equation (3) as:

\[ y_1 \approx \left( a_1 - \frac{a_2}{2m} + \frac{3a_3}{4} + \frac{3a_2^2a_3}{8m^2} \right) \cos \omega t + \left( \frac{a_2}{2} - \frac{a_1a_2}{2m} - \frac{3a_2a_3}{4m} - \frac{3a_2^3a_3}{32m^3} \right) \cos 2\omega t \]  

\[ + \left( \frac{a_3}{4} + \frac{3a_2^2a_3}{16m^2} - \frac{a_2^2}{2m} \right) \cos 3\omega t + \left( \frac{a_2^3}{8m^2} - \frac{3a_2a_3}{8m} \right) \cos 4\omega t + \cdots \]  \hspace{1em} (7)

Obviously, the second harmonic amplitude decrease from \( \frac{a_2}{2} \) to \( \frac{a_2}{2} - \frac{a_1a_2}{2m} - \frac{3a_2a_3}{4m} - \frac{3a_2^3a_3}{32m^3} \). We repeat this process with several iterations until it reduces the magnitude of the distortion to an acceptable level. Fig. 9 shows the flow chart of

![Flow chart of the proposed digital pre-distortion algorithm](image)

Fig. 9. Flow chart of the proposed digital pre-distortion algorithm
the pre-distortion algorithm, it is convenient to achieve for a highly integrated transceiver containing analog-to-digital converter (ADC). Simultaneously, this process pushes the majority of harmonics to higher frequencies that can be filtered out by external low pass filter. Fig. 10 shows the SFDR with digital pre-distortion improves from 75 dBc to 95 dBc with a 240 MHz signal clocked at 2 GS/s by simulation.

6 Measured results

The DAC has been designed and fabricated in TSMC 65 nm CMOS technology, which is embedded in a transceiver, as shown in Fig. 11. The DAC’s output current is converted to a voltage through an off-chip 50 Ω resistive differential load and coupled to a spectrum analyzer through a wide-band transformer.

![Fig. 10. Simulated SFDR performance before/after enabling pre-distortion from 75 dBc to 95 dBc](image)

![Fig. 11. Micro-photograph of the SOC containing the designed DAC](image)

The designed DAC demonstrates a SFDR of 70 dB for a 240 MHz signal at 2 Gsample/s, as shown in Fig. 12. In order to evaluate the DAC linearity performance, we use dual-tone or four-tone test. The DAC produces an IM3 < −64 dBc for a dual-tone test and <−63.0 dB IM tones for a four-tone test, as shown in Fig. 13 and Fig. 14. The 5+9 segmented DAC consumes 490 mW power with 2.0/1.3 V supply voltage.

The Fig. 15 shows the measured SFDR and IM3 with sampling rates up to 2 Gsample/s, since the test input signal of DAC is up-converted by a Numerically Controlled Oscillator (NCO), the measurable frequency range is limited. Here, we
present the results from 130 MHz to 330 MHz frequency range. At each operating frequency, we use digital pre-distortion algorithm once.

Table II compares this DAC with recently published state-of-the-art 12–16-bit DACs in resolution, power consumption and SFDR. This DAC achieves an extremely small chip area, with moderate linearity performance due to the digital pre-distortion algorithm.

Fig. 12. Measured SFDR performance (a) before (b) after enabling pre-distortion from 63.8 dBc to 70.0 dBc

Fig. 13. Measured dual-tones spectrum showing (a) a $-64.7$ dBc of IM3 for 180 MHz and 200 MHz signals, (b) a $-64.94$ dBc of IM3 for 210 MHz and 215 MHz signals
Conclusion

In this paper, the design of a 14 bit DAC for a wireless transmitter is presented. This DAC utilizes a segmented architecture to obtain a high linearity with a small chip area. With digital pre-distortion scheme, the DAC achieves a good linearity at high signal frequencies without area penalty. The measured SFDR with a 240 MHz input signal at 2 Gsample/s is 70 dB with 490 mW power consumption.

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