Towards merged-element transmons using silicon fins: the FinMET

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A merged-element transmon (MET) device, based on silicon (Si) fins, is proposed and the first steps to form such a “FinMET” are demonstrated. This new application of fin technology capitalizes on the anisotropic etch of Si(111) relative to Si(110) to define atomically flat, high aspect ratio Si tunnel barriers with epitaxial superconductor contacts on the parallel sidewall surfaces. This process circumvents the challenges associated with the growth of low-loss insulating barriers on lattice matched superconductors. By implementing low-loss, intrinsic float-zone Si as the barrier material rather than commonly used, potentially lossy AlOx, the FinMET is expected to overcome problems with standard transmons by (1) reducing dielectric losses; (2) minimizing the formation of two-level system spectral features; (3) exhibiting greater control over barrier thickness and qubit frequency spread, especially when combined with commercial fin fabrication and atomic-layer digital etching; (4) potentially reducing the footprint by several orders of magnitude; and (5) allowing scalable fabrication. Here, as a first step to making such a device, the fabrication of Si fin capacitors on Si(110) substrates with shadow-deposited Al electrodes is demonstrated. These fin capacitors are then fabricated into lumped element resonator circuits and probed using low-temperature microwave measurements. Further thinning of silicon junctions towards the tunneling regime will enable the scalable fabrication of FinMET devices based on existing silicon technology, while simultaneously avoiding lossy amorphous dielectrics for the tunnel barriers.

INTRODUCTION

The invention of the transmon qubit has fueled the rapid development of quantum-information research over the past decade [1], and landmark breakthroughs have been achieved with this technology[2]. Modern transmons are typically based on a small Al/AlOx/Al tunnel junction formed by thermal oxidation of Al in parallel with a large shunt capacitor. A variety of methods exist for defining the Josephson junctions (JJs) that function as nonlinear inductances. These include Dolan bridges [3], the Manhattan shadow evaporation process[4] and overlap designs[5], [6].

However, the transmon qubits are difficult to scale for a couple of reasons. First, the associated shunt capacitors are typically defined as planar structures grown on a low-loss substrate. While very low-loss substrates (i.e., intrinsic, float-zone silicon (i-Si)) with loss tangent in the low 10^-7 range can be obtained [7], it is well known that the interfaces and surfaces of the planar shunt capacitor participate significantly in the total loss [8], [9]. In general, while it has been observed that increasing the size of the shunt capacitor can dilute the high loss contributions [10], this results in very large structures, with dimensions of the order of 100s of micrometers. This is problematic for scaling up to systems with many qubits and warrants capacitors with lower form factors. Second, the frequency allocations of transmons using thermally oxidized aluminum have a significant spread [11]. While there have been advances on this front using post-processing, i.e. laser-annealing of individual devices [12], this remains a significant obstacle to large-scale integration of transmons. To this end, better control of the tunnel-barrier thickness and interfaces in the fabrication process is desired.

Recently, an alternative approach to scaling these circuits was demonstrated [13], i.e. the merged-element transmon (MET). The MET minimizes the transmon qubit size and radiation while providing an avenue to potentially reduce losses due to surfaces and interfaces. This design entails engineering the junction itself to satisfy the transmon requirements for frequency, anharmonicity, and charge noise by merging the external shunt capacitor and the JJ inductance into a single element. This design is constructed from a...
superconductor–insulator–superconductor trilayer where the insulator is made from a dielectric material that has a low barrier height and may even be a semiconductor at room temperature. This design has several advantages over the traditional transmon. First, the MET allows a significant reduction, on the order of $10^4$, in the device area [13]. Second, the resulting small qubit dimensions effectively suppress unwanted radiation and qubit-qubit coupling through direct interactions or box modes. Third, the MET frequency should be less susceptible to the variation in lithography because the associated capacitive and inductive contributions toward the qubit frequency cancel out to first order [1], [13]. Moreover, one may choose a low-barrier-height material as the junction tunnel barrier. This enables the use of a relatively thick tunnel barrier that may reduce the percentage variation in junction inductance, potentially alleviating the frequency allocation problem.

The energy-level transitions of a MET device, from two-tone spectroscopy measurements confirmed that the MET is indeed operating in the transmon qubit regime [13]. An in-depth TLS-loss analysis identified the lossy amorphous silicon tunnel barrier and surrounding interfaces as the major limiting factor for the qubit relaxation time [13]. Subsequently, Mamin et al. (and the IBM team) demonstrated METs with coherences up to 41 and 234 μs, using as-grown-and annealed-AlOx overlap junctions respectively [14].

While the MET demonstration [14] confirmed the possibility of obtaining long coherence times in selected devices, the extreme oxidation (several hours at 600 torr of O₂) and annealing conditions (rapid thermal anneal at 425°C) resulted in significant frequency spread for the devices. This is reminiscent of conventional transmons and is most likely due to several reasons. First, the tunneling critical current varies exponentially with the tunnel barrier thickness, which is difficult to control in a 2 nm thick tunnel barrier formed by thermal oxidation. In addition, there are tunneling hotspots due to the barrier being structurally and chemically inhomogeneous, resulting in only a small percentage of the 2 nm thick AlOₓ barrier actually contributing to the tunneling [15]. Second, the critical current can be affected by atomic-level defects in and around the barrier and wiring [16]. These can cause two-level-system spectral features [17] that are detrimental to the operation of the devices. This illustrates the importance of developing a more robust method of defining the tunnel junction. Specifically, we note that a crystalline tunnel barrier with a low barrier height can mitigate this problem because it can be thicker, making monolayer scale thickness variations less significant.

Here, we propose the concept of a FinMET device that can overcome a number of the problems discussed above. This process capitalizes on the fact that crystalline Si fins can be formed on the surface of a wafer using an anisotropic wet etch (FIG 1). In the FinMET, these Si fins act as tunnel barriers for the MET. The fin walls can, in principle, be atomically flat, parallel, and engineered to be a very specific thickness. With Si barriers the small band gap compared to that of AlOₓ also results in a lower tunnel-barrier height [13]. This allows the use of a relatively thick Si tunnel barrier, on the order of 5-10 nm, leading to a natural extension of the MET to a more scalable geometry.

In addition to being used as a junction, the fin geometry also allows the fabrication of low-loss parallel plate silicon capacitors with a significant reduction in utilized area on chip. Such capacitors can be used in conjunction with conventional Josephson junctions to reduce the size of conventional transmons while improving their coherence times or to enable new, novel protected qubits [18].

In this work, as first steps towards realizing a FinMET device, we demonstrate both the fabrication of high-aspect-ratio Si fins and the self-aligned process to deposit superconductors on such fins. Subsequently, we integrate these Al-Si-Al fin capacitors in resonator circuits and perform microwave measurements at millikelvin temperatures. The measurements clearly demonstrate the presence of working fin capacitors and their compatibility with traditional superconducting qubit fabrication. These scalable techniques are unique in that both capacitive elements and METs can be formed from the Si substrate resulting in reduction in both form-factor and losses and directly improving qubit scalability.

**FIN FABRICATION AND STRUCTURAL CHARACTERIZATION**

Both fin-based capacitors and FinMET designs comprise parallel-plate electrodes that can be fabricated using standard processing techniques, and capacitively coupled through the low-loss substrate for scalable integrated circuits. In this case, it is critical to have low loss, epitaxial interfaces between the fin and the metal layer. This can be achieved using careful...
surface cleaning and growth methods, as shown by Place, et al. [19].

**Fin fabrication:** The FinMET devices are composed of a Si fin [20], [21] with superconducting electrodes grown on both the surfaces of the fin, effectively forming a horizontal superconductor-semiconductor-superconductor junction, as illustrated in Figure 1. The Si fin is formed by top-down etching of a commercial intrinsic Si substrate, which are commonly grown using float-zone technique and exhibit high resistance and low loss. To achieve atomically flat surfaces, we start with a Si(110) substrate and use anisotropic wet etching to fabricate Si fins with smooth (111) surfaces.

For the anisotropic wet etch, a silicon nitride (SiNₓ) hard mask is used. The SiNₓ layer is deposited using a low-pressure chemical vapor deposition technique which results in a high density, low stress SiNₓ layer on top of the silicon substrate. This mask is lithographically defined using electron beam lithography (EBL) and CF₄/O₂ based plasma dry etching.

Before the wet etch to define the fin, the sample is cleaned under a C₆F₅/SSF₆/CF₄ Si etching chemistry in a plasma based dry etcher for 30 seconds to remove the top damaged layer from the previous dry etch for the SiNₓ mask. This was found to considerably improve the cleanliness of the substrate and the uniformity of the wet etch. The wet etch is subsequently performed using 45% potassium hydroxide (KOH) solution at 87°C. Figure 2 shows fin structures defined on a Si(110) substrate. Fin mask widths were varied from 100nm to 1um for test samples. The undercutting from the wet etch is considerable (~50-80nm). The thinnest fins that were reliably fabricated without rigorous optimization of process parameters were approximately 80nm (with a length and height of 100nm and 3um respectively).

By using the intrinsically parallel crystallographic {111}-faces that are exposed by the anisotropic etch, the tunnel junction can be expected to have well-defined, homogeneous tunneling currents. In addition, the low-tunnel-barrier-height material can be much thicker than standard junction material and thus mass-fabricated with better margins.

**Fin metallization:** Metallization of the fins can be accomplished by cleaning the exposed Si{111}-faces and then epitaxially growing a superconducting metal, such as Al. Prior to Al growth, a buffered HF etch followed by high temperature annealing of the Si fin is expected to result in a pristine interface, thus optimizing coherence. Additionally, since the bottom edge is surrounded by low-loss substrate a reduced participation of the Al-air exposed interface is expected.

Two different process flows can be followed, either self-aligned or planarized, as illustrated in Figure 3. Both processes start by etching Si fins as described previously, using a SiNₓ hard mask and a combination of dry and wet etches. The planarization process is not demonstrated here but explained in the discussion section.

The process flow that is followed in this article, involves retention of the SiNₓ hard mask that was initially used to etch down the Si fins. Using the overhang in the SiNx on top of the fin, an angled deposition of aluminum can lead to a break in the metal layer at the top of the fin. This shadow-evaporation technique therefore enables direct creation of a fin capacitor using a self-aligned process. This eliminates the need to etch off Al from the top of the fin to electrically disconnect the pads on either side of the fin (Fig. 3A). Contact pads can then be patterned using optical lithography. This self-aligned process was followed in this work. Figure 4 shows fin structures coated with Al, as described below. Fins were fabricated according to the above recipe and the Al was shadow deposited with an effusion cell in a molecular beam epitaxy chamber. The substrate temperature was maintained close to 0°C (Fig. 4 A-F). Smoother Al films can be grown by performing the deposition in a cryogenic cold stage maintained at -196 °C following a process similar to Refs. [22]–[25]. For the microwave measurements, the Al layer on the fins was shadow deposited using an electron beam evaporator at room temperature.

Connection to other parts of the circuit, for example superconducting resonators and wiring, can be accomplished using the Al pads on the sides of the fins using standard processing techniques.
Lumped element (LE) resonators were made using fin capacitors having widths greater than 200nm, meander inductors, and interdigitated capacitors (IDCs). These LE resonators were used to demonstrate feasibility of integration of fins in superconducting circuits and to characterize fabricated fins in the capacitive regime and evaluate preliminary dielectric losses. The concept of the LE design is depicted in Fig. 5. The design consists of eight LE resonators inductively coupled to a single 50 Ohm coplanar waveguide feedline in a standard ‘hanger’ arrangement[26].

To characterize the fin capacitors and minimize uncertainties due to capacitance of metallized leads, fins are incrementally added between the fingers of the IDC as shown in Fig. 5. The meander inductor and other IDC parameters are kept the same while the number of fins in each LE resonator is varied. In this way, the resonant frequencies of the LE resonators are separated, and capacitance of the fins may be determined experimentally.

3um tall fins having lengths of 120um and patterned widths of 300nm and 400nm were fabricated on a 50.8mm diameter Si(110) wafer using the process outlined above. The fin capacitor height and width are set during fin formation while the fin capacitor length is lithographically defined in the metallization (superconductor) layer using optical lithography. Following fin formation, the wafer was etched in 6:1 BHF for 2 minutes to remove surface oxide and immediately loaded into high vacuum for Al deposition.

30nm of Al was deposited using e-beam evaporation on each side of the fins using deposition angles of ±25° to obtain a uniform Al coating on each side of the fins with a self-aligned break in the Al near the top of the fin due to the overhang of the silicon nitride mask. Following Al deposition, the test resonator circuits were defined using direct-write photolithography and wet etching. The wafer was diced into
DISCUSSION AND SUMMARY

The use of amorphous-AlO$_x$ Josephson junctions for quantum computing transmon applications is challenged by frequency allocation, frequency stability, spurious two-level states (TLS) and loss issues. In addition, the large size of shunt capacitors required to dilute the TLS losses at surfaces and interfaces severely limits the scalability.

In order to transition to a more scalable system and reduce footprint, a significant effort on the front-end is required in order to bootstrap a completely new function fabrication process and device design. To this end, we have proposed and demonstrated one of the necessary elements of a new FinMET technology. These include the fin structures needed to develop a more scalable system and reduce footprint. Although the fin thicknesses used in this work are not low enough to demonstrate tunneling, working low-loss fin capacitors integrated with superconductor resonator circuitry have been characterized. Next steps include integration of these capacitors with tunnel junctions to form qubits with reduced footprint and demonstration of tunnel junctions in the fins to form the proposed FinMET device.

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To achieve tunneling through the silicon fins the fin thicknesses need to be approximately 5-10 nm. Structures of such extreme aspect ratios are on the cutting edge of modern fin technologies [20]. Thinning of the fins can then be achieved, by timing an additional wet etch and/or subsequent digital etching. The digital etching process is typically achieved by oxidizing the Si(111) surface using O$_2$ plasma at room temperature to form an oxide layer that is approximately 5-7nm thick. This oxide can then be etched away using HF and the process repeated to achieve the desired fin thickness. The second envisioned process to thin the fin involves using atomic layer etching (ALE) with a O$_2$, HF, and Al(CH$_3$)$_3$
chemistry [29]. A final wet etch in KOH can then be used to regain the smooth Si(111) surface followed by a HF dip to remove any oxides, prior to Al metal deposition.

The entire process can be also performed using photolithography by using SiNₓ deposited on step edges [30] that can form SiNₓ masks with similar dimensions. This can result in a more reliable wafer-scale fabrication of fin-based qubit devices.

To deposit the side superconductors, in addition to the process demonstrated, the second proposed process flow uses planarization (Fig. 3B). This involves removing the SiNₓ hard mask and then depositing a layer of aluminum onto the fins. Back-etching of a subsequent resist layer, either by dry etching or chemical mechanical polishing (CMP), can thereafter be used to expose the metal at the top of the fin and a wet or dry etch is used to remove the top aluminum. Contact pads would then be patterned in a way similar to the previous process flow.

While this is feasible to demonstrate at the small scale, the importance of these developments is that it should be possible to scale up significantly by decreasing the yield variation and material defects, based on existing Si-fin infrastructure and expertise in the field.

In conclusion, in this work, we first propose and outline a new geometry to define Si fin based self-aligned superconductor/Si/Superconductor trilayer structures to form fin merged element transmons (FinMETs). Following this, we successfully fabricate, and measure low-loss resonators consisting of Al/Si/Al fin capacitors. This also establishes the compatibility of this technology with conventional qubit or novel [18]qubit fabrication platforms. Further thinning of the Si barrier layer will enable the subsequent realization of FinMET devices.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

AUTHOR CONTRIBUTION

AG, APM, CJP and DPP initiated the study. AG fabricated the Si fin structures. AG, HI, JTD performed MBE Al deposition. APM performed electron beam Al deposition and fabrication of resonators. AG performed SEM and TEM measurements. APM performed microwave measurements. APM, CRHM and RWS analyzed the measurement data. RZ contributed to the initial MET simulations. TZ performed COMSOL simulations. AG wrote the manuscript with inputs from all the authors, under supervision of CJP, RWS and DPP.

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