Real-Time Waveform Matching with a Digitizer at 10 GS/s

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Abstract—Side-Channel Analysis (SCA) requires the detection of the specific time frame within which Cryptographic Operations (COs) take place in the side-channel signal. In laboratory conditions with full control over the Device under Test (DuT), dedicated trigger signals can be implemented to indicate the start and end of COs. For real-world scenarios, waveform-matching techniques have been established which compare the side-channel signal with a template of the CO’s pattern in real time to detect the CO in the side channel. State-of-the-art approaches are implemented on Field-Programmable Gate Arrays (FPGAs). However, current waveform-matching designs process the samples from Analog-to-Digital Converters (ADCs) sequentially and can only work with low sampling rates due to the limited clock speed of FPGAs. This makes it increasingly difficult to apply existing techniques on modern DuTs that operate with clock speeds in the GHz range.

In this paper, we present a parallel waveform-matching architecture that is capable of performing waveform matching at the speed of fast ADCs. We implement the proposed architecture in a high-end FPGA-based digitizer and deploy it to detect AES COs from the side channel of a single-board computer operating at 1 GHz. Our implementation allows for waveform matching at 10 GS/s with high accuracy, thus offering a speedup of 50× compared to the fastest state-of-the-art implementation known to us.

Index Terms—Side-Channel Analysis, Hardware Security, Waveform Matching, Parallel FPGA Design, Signal Processing

I. INTRODUCTION / MOTIVATION

Non-invasive physical attacks on implementations are a serious threat to all embedded systems. Side-channel attacks and fault attacks can break or circumvent cryptographic methods and have been shown to be applicable to many systems (iPhones [1], One-Board Computers [2], PCs [3], IoT (Internet of Things) devices [4]). All side-channel-based methods apply triggering mechanisms, which detect the exact time frame during which a specific operation takes place within the side-channel signal, and then activate the data acquisition or the execution of a fault attack.

The most reliable method for triggering is a signal emitted from the device under test which has a constant distance to the operation of interest. However, in most real-world examples, this is not possible due to: 1) Restrictive access to the device that will not allow a normal user to modify the code, e.g., to generate trigger signals. 2) Non-deterministic execution due to preemptive scheduling, interrupts, branch prediction, and other methods [5]. For example, triggering on I/O (Input/Output) events that can be detected with normal oscilloscope triggering mechanisms such as rising edges, pulses, or level changes are affected by such non-deterministic fluctuations. These I/O events may then not be equidistant to the operation of interest for each execution, making it hard to align the different events.

Waveform-matching triggering techniques are state-of-the-art when it comes to circumventing the problems of these approaches. A waveform template is used in a pattern-matching system that triggers if the stored template is similar to the waveform of the incoming side-channel signal. To the best of our knowledge, there are three different solutions for pattern-based triggering.

All three solutions feature either Sum of Absolute Differences (SAD) or interval matching as a similarity measure at sample rates of approximately 200 MS/s. However, many systems currently run at frequencies of over 1GHz. Applying SCA methods like Differential Power Analysis (DPA) [6] or Correlation Power Analysis (CPA) [7] requires sampling frequencies that are multiple times faster than the frequency of the device under test [8]. All current designs for waveform matching make use of FPGAs to implement sequential pattern matching in real time. Newer ADCs, which are responsible for the accurate data conversion between the analogue measurement and the digital acquisition, can already sample at rates well above 1 GS/s [9]. However, the maximum clock speed of most FPGA designs is below 1 GHz, which shows that sequential designs will not become fast enough to process at the speed of fast ADCs.

In this paper, we present an FPGA design that is capable of performing waveform matching at sampling rates of fast ADCs by utilizing a generic parallel architecture that scales with the available number of Lookup Tables (LUTs) in FPGAs. Furthermore, we implement this architecture in a high-end digitizer with a programmable FPGA and evaluate the resource demands for such a parallel design. With this digitizer featuring a high memory depth of 4 GB on-board RAM and a high-

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speed PCIe connection to the host PC, the implementation offers a powerful one-device solution for SCA setups in the field. Further, we can program the FPGA to record, trigger, and filter traces from any DuT. With the pattern matching being implemented within the pipeline of the digitizer, trigger delays become inconsequential for the recording of operations, as the pattern matching happens at line rate. Furthermore, we show that the design and implementation allows for waveform matching at 10 GS/s with high accuracy.

II. STATE-OF-THE-ART

A. Waveform Matching

Waveform matching with side-channel information has the goal of comparing a previously obtained pattern, which we will call template \( c \) with length \( n \), to a continuous incoming signal \( T \). Let \( t \) be a part of the data stream \( T \) at any instance of time. Trace \( t \) has the same length \( n \) as the template \( c \).

If this trace \( t \) is sufficiently similar to the template \( c \), we can then infer that a specific operation has taken place on the DuT at that instance of time. Various methods can be used to calculate such a similarity \( s \) that have different qualities and advantages.

a) Correlation: This similarity measure can be used to find linear dependencies but also to rate the similarity between different time series. The Pearson correlation coefficient can be calculated with

\[
s_{\text{PearsonCorr}} = \frac{\sum_{i=1}^{n}(t_i - \bar{t})(c_i - \bar{c})}{\sqrt{\sum_{i=1}^{n}(t_i - \bar{t})^2 \sum_{i=1}^{n}(c_i - \bar{c})^2}},
\]

where \( t_i \) denotes the \( i \)-th sample of trace \( t \), and \( \bar{t} \) is the average over all samples. The Pearson correlation coefficient can be used to successfully find COs within a recorded trace and is not influenced by a static vertical offset in the recording [10]. The Pearson correlation also corrects for any scaling in the compared time series, which makes it more robust to small variations in the measurement setup. Its main disadvantage is its resource-heavy implementation, as it uses several multiplications and divisions. Additionally, it requires the calculation of several sums and averages over the entire time series, which also makes the correlation computationally too expensive. This will lead to a long delay, and will use many resources on an FPGA. Furthermore, a valid representation of small rational numbers must be chosen and calculations must be made in floating point numbers, which again is resource intensive.

b) SAD: As shown in Eq. (2), the Sum of Absolute Differences (SAD) first calculates a sample-wise absolute difference between the incoming time series and the template, and then sums the results. SAD returns a low score if the two series are similar.

\[
s_{\text{SAD}} = \sum_{i=1}^{n}|t_i - c_i|
\]

The calculation of the SAD is significantly less resource intensive than the Pearson correlation and is a commonly used similarity indicator for normalized traces. However, one disadvantage is the dependency for equal vertical offsets and scaling. If these two properties are not equal for the template and the incoming signal, proper detection cannot be guaranteed, thereby requiring adjustments to the threshold. Furthermore, single outliers can distort the entire matching process. Multiple outliers or measurement errors can lead to an extremely large sum which, in turn, could lead to an overflow, making the implementation less stable. All summed values must have at least the same resolution as the template and the trace, which implies a complex addition.

c) Interval Matching: This similarity measure specifies an interval with a chosen offset above and below the established template for every sample position \( i \), see Eq. (3). The similarity is measured as the sum of samples that lie within this interval, see Eq. (4). A visual explanation is given in Fig. 1.

\[
f_{\text{int}}(t, c, i, o_{\text{offset}}) = \begin{cases} 
1, & \text{if } c_i + o_{\text{offset}} \geq t_i \geq c_i - o_{\text{offset}} \\
0, & \text{otherwise.}
\end{cases}
\]

\[
s_{\text{Interval}} = \sum_{i=1}^{n}f_{\text{int}}(t, c, i, o_{\text{offset}})
\]

Similar to SAD, vertical offsets and scaling are a challenge when using the interval matching method. Success here strongly depends on the correct calibration of the offset \( o_{\text{offset}} \) and the matching threshold in \( s_{\text{Interval}} \). When a trace \( t \) is considered a match. However, interval matching has the advantage of summing binary information alone. This leads to simple additions and a maximal sum that is already known at design time and without being arbitrarily large as in SAD. Furthermore, extreme outliers will not have a disproportionate effect on the overall result. Additionally, with Eq. (3) we can set the offset \( o_{\text{offset}} \) and the threshold for the similarity \( s_{\text{Interval}} \). This provides one additional degree of freedom compared to the other methods, which may facilitate a more accurate calibration. Due to these myriad advantages, we use interval matching in our implementation.

B. Devices that use waveform matching for triggering

There are already several solutions that utilize waveform-matching triggering systems. All utilize FPGAs as target platforms. Both icWaves from Riscure [11] and the ChipWhisperer Pro (CW1200) [12] are two commercial products that use
SAD as a similarity measure. icWaves is capable of matching an incoming signal to a template at 200 MS/s with an 8-bit resolution, and the ChipWhisperer Pro can achieve 105 MS/s with a 10-bit resolution. The size \( n \) of the template can, at maximum, be 1024 samples for icWaves and 128 samples for the ChipWhisperer Pro. The trigger box from Beckers et al. [5] utilizes interval matching and can match waveforms at 125 MS/s with a 14-bit resolution. The maximum length of a template is 1500 samples, which can be improved if the resolution is lowered. The trigger box [5] is constructed with fault injections in mind, which is why its design is heavily tuned to have a low response time between the pattern occurring in the side channel and the emission of a trigger signal. In principle, the low sampling rates are not detrimental as long as the side-channel waveform patterns can also be successfully detected with undersampling a faster DuT’s side channel. The waveform matcher can emit a trigger signal to start recording with a higher-end oscilloscope for high-resolution measurements. This does, however, increase the complexity of the measurement setup overall. Note that the waveform matching would still operate with a signal at a low sampling rate and this might not work if the relevant operation contains high-frequency side-channel patterns.

To summarize, state-of-the-art techniques for waveform-template matching often feature sampling rates below the rate necessary for a direct side-channel attack. Hence, these techniques have to utilize the help of an additional oscilloscope to collect traces from a system operating in the GHz range. Furthermore, patterns that arise from operations only lasting a few clock cycles might not be detectable at all. As a remedy, we propose a highly parallel design which can be scaled to even higher sampling rates than 10 GS/s given the resources on the FPGA and a sufficiently fast ADC.

### III. Hardware Architecture for Parallel Waveform Matching

In order to have a significantly higher sample rate of 10 GS/s and to be able to match waveforms at such high speeds, a parallel architecture is inevitable as most FPGAs will not run faster than 500 MHz with a sufficiently complex design. Therefore, we must process multiple samples in each clock cycle in order for the architecture to be scalable. We denote this degree of parallelism as \( d \) and need to process \( d \) samples each clock cycle. With a higher degree of parallelism, the design can scale with the speed of modern ADCs, but must also, at the same time, account for higher resource requirements in terms of LUTs. To achieve a design capable of matching waveforms at 10 GS/s, a potential degree of parallelism where \( d = 32 \) on an FPGA clocked at 312.5 MHz would be required, which is an achievable clock speed for modern FPGAs.

Fig. 2 shows our proposed the parallel matching architecture. Our waveform matching module receives \( d \) samples per clock cycle each with \( p \)-bits of resolution as the input, and also outputs \( d \) samples per clock cycle. The memory for buffering samples is implemented as a shift register \( \text{SRG} \) of length \( l_{\text{SRG}} \). It contains \( d \) samples at each register stage. With each clock cycle, the \( d \) samples are shifted to the next stage while the new samples are inserted into the first register stage. As each shift register stage holds \( d \) samples of \( p \)-bit sizes, they have a width of \( d \times p \) bits.

The length \( l_{\text{SRG}} \) of the shift register is determined as follows:

In order to compare the incoming waveform to the entire template \( c \) of length \( n \), we store at least \( n \) samples. In practice, more than \( n \) samples should be stored in the SRG to first compensate for the latency \( l \) of the circuit until a match is detected and a valid signal is emitted. Second, there might be cases where the template only covers the waveform at the end of the operation (starting at position \( l_{\text{positionalBuffer}} \) within the operation). However, if the waveform of the entire operation is required for further analysis, all samples of the operation preceding the template should also be stored and transferred to the host PC. We denote this number of excess samples as \( e_{\text{samples}} \) calculated as follows:

\[
e_{\text{samples}} = l \cdot d + l_{\text{positionalBuffer}}.
\] (5)

The shift register therefore has a length of

\[
l_{\text{SRG}} = n + e_{\text{samples}}
\] (6)

and a width of at least \( p \)-bit.

As each of the simultaneously obtained \( d \) samples could be a potential starting position of a CO, segments starting at each of the \( d \) positions must be compared to the template \( c \). Hence, to maintain the throughput, we compare \( d \) vectors of length \( n \) to the template at each clock cycle. This is implemented by \( d \) matcher modules (see Fig. 2) that all read from their respective part of the shift register. Each MatcherModule, with \( 0 \leq j < d \) receives the vector \( \text{SRG}[j : j + n] \). Every MatcherModule must only compare its share of the SRG to the template and yield a valid signal which as an indication of a matched sequence starting at position \( j \). Each of the \( d \) valid signals is then routed into the TriggerLogic module. This module ensures that the trigger signal is maintained as a logic 1 for the duration of the entire operation of interest if one of the MatcherModules is emitting a valid signal. Furthermore, it also acts as a hold-off counter, preventing a trigger signal twice in a row if there are multiple matches within one operation of interest. Since the latency of the design is included as per equation (5) and (6), the module thereby synchronizes the emitted trigger signal with the sample output.

A matcher module (see Fig. 3) compares the \( n \) samples with the intervals in parallel, sums up the matches, and compares the sum to a threshold. With parallelism in mind, we cannot use the same architecture for the MatcherModules as the authors of [5]. There, Beckers et al. compared the incoming sample from the ADC to each possible point of the template and used a register adder chain to add up potential matches. In doing so, they achieved a low latency of only 4 clock cycles when a pattern similar to the template \( e \) occurs on the incoming stream. However, we cannot utilize a similar design, since we have to compare multiple samples per clock cycle simultaneously which will not work with a sequential adder.
chain. Instead, we use an adder tree to add up the values of the different Comparator modules in parallel, displayed as the $\sum$ block in Fig. 3. As we are only adding single bit binary values, we can utilize LUTs for this.

As we chose interval matching for our design, we compare samples against the upper and lower boundaries. The Comparator modules (Fig. 4) are nearly identical to the design in [5]. We need to compare each sample $t_i$ in the trace $t = SRG[j : j + n - 1]$ to the respective boundaries of the template $c$ at the same position. Here, we can directly apply the function $f_{int}(t, c, i, o_{offset})$ from (3) for each sample. The boundaries are already precomputed for each sample $i$ and substituted with the registers $o_{i, upperLimit}$ and $o_{i, lowerLimit}$. Also, other similarities measures could be implemented in the MatcherModule, as long as the FPGA has sufficient resources to implement the design.

![Fig. 2: Parallel matching architecture with the SRG that takes $d$ samples with $p$-bit length every clock cycle.](image1)

![Fig. 3: The MatcherModule with all parallel comparators.](image2)

![Fig. 4: The Comparator$_i$ that is used for each sample $i$ in the template.](image3)

**IV. IMPLEMENTATION OF PARALLEL WAVEFORM MATCHING AT 10GS/s ON A DIGITIZER**

This section discusses the implementation of the proposed parallel architecture within the FPGA of a digitizer. A digitizer is an electronic acquisition device that first captures analog signals, then samples and digitizes them using ADCs, and finally sends them to a buffer where they can be stored before being processed by a host computer. FPGA-based digitizers also allow implementing additional application-specific logic for processing the digitized signal. FPGA-based digitizers thus couple the high sampling rates of modern ADCs directly with the programmability and high parallelism of modern FPGAs. They thus pose the ideal single-device target platform to implement the proposed parallel waveform matching.

We use the ADQ7 from SP-Devices [13] which features an onboard Xilinx Kintex UltraScale FPGA (KU85). It uses two parallel ADCs for recording at $10 \text{ GS/s}$ with a 14-bit resolution. With 4 GB of onboard memory, very long traces can be recorded and stored. A PCIe interface enables the communication between the digitizer and the host PC. As PCIe is limited to $6.8 \text{ GBytes/s}$ and the ADC has a data rate of up to $20 \text{ GBytes/s}$, a reduction of the data is necessary to continuously monitor a device for SCA. Consequently, for...
long SCA measurements, triggering to only record operations of interest (COs) is essential.

The datapath of the ADQ design is shown in Fig.5 and has two blocks (shown in blue) representing User Logic 1 and User Logic 2. Within these blocks, filters and other real-time signal processing can be implemented. The FPGA is clocked at 312.5 MHz and has to process $d = 32$ samples with $p = 14$ bit precision per clock cycle in order to process 10 GS/s. The parallel matching design presented in Section III is implemented in User Logic 1.

A. Implementation Details

The following outlines our FPGA implementation on the Xilinx Kintex UltraScale FPGA of the digitizer. It employs 6-input LUTs (LUT6) and 8-bit carry logic per slice (CARRY8).

a) Shift Register: The implementation of the shift register SRG consists of a cascade of the 32-bit shift register (SRL32) elements found in Xilinx FPGAs. This is a scalable implementation for shift registers based on the distributed RAM cells in the SLICEM slices, compared to the dedicated flip-flop-based shift register implementation. Because of the FPGA featuring more than enough LUTRAM, which is the main resource used by the shift register, the shift register could hold up to 30,000 samples. Our design does not use other primitives like dedicated (Block)RAM and DSPs. Thus, LUTs are the limiting resource for our design.

b) Comparators: These are implemented in LUTs. Usually, dedicated carry logic of the Configurable Logic Block (CLB) can achieve a much better performance compared to LUTs for small arithmetic operations thanks to its structure and independent routing resources. However, even a multi-level LUT implementation satisfies the timing requirements as our case requires only a simple comparison with a limited bit width. If carry-lookahead gates are used, then each comparator module requires 22 LUTs per sample on average. On the other hand, for a LUT-based implementation, only 6 LUTs are needed on a per-sample basis. These 6 LUTs alone allow implementing both comparisons contained in the module as well as the conjunction (AND gate) operation of the comparator. Therefore, a LUT-based implementation, as opposed to the default implementation, is preferred as it leads to approximately 3.5 times less LUT usage.

B. Overall Resource Footprint and Comparison

Waveform matching is implemented in User Logic 1 of the digitizer’s datapath pipeline shown in Fig. 5. For the implementation, we can thus use the logic that is not yet occupied by other components of the datapath. Table I shows the LUT usage of our waveform matching module only. We show the number of LUTs used for the implementation of the comparators utilizing carry logic or following an LUT-based approach. The utilization of LUTs in percent is calculated in accordance with the Xilinx KU85 used in the ADQ7DC [14]. As shown, implementing the adders of the design using the dedicated carry logic would result in unnecessarily large designs. By implementing the adders in LUTs, we can implement matchers that scale better: For each sample of the template $e$, we need approximately 244 LUTs. Therefore, the approach scales linearly with the number of samples in our template, making it rather easy to fit a specific template into our design.

Table II compares our implementation to the trigger box by Beckers et al. [5] and the icWaves solution [11]. With a maximum of $n = 1, 400$ samples as the template length, our implementation is comparable to the state of the art in terms of template lengths, while achieving a much higher sample rate. With $n = 1, 400$, we need approx. 68% of the available LUTs, which leaves resources for other functions being implemented on the FPGA. A further reduction of the template length will therefore linearly reduce the needed number of LUTs. The memory of the ADQ7DC can store 4 GB of data, making it theoretically possible to store 1,000,000 k samples with a resolution of 16 bit. However, for our tests, we never stored more than 100,000 k samples, which is sufficient for evaluating the workflow to perform SCA based on waveform matching.

V. WORKFLOW AND EVALUATION

We evaluate the proposed technique by performing SCA based on waveform matching on a BeagleBone Black. The BeagleBone Black runs Linux based on Debian 10 with kernel version 4.19.94-ti-r42, with a TI AM335x ARM processor clocked at a fixed frequency of 1 GHz [15]. The measurement setup is based on the setup proposed by Balasch et al. [2] and features a Langer magnetic near-field probe, model RF-B, on the decoupling capacitor C66 on the back of the BeagleBone. The electromagnetic (EM) signal was amplified by a wideband 30 dB amplifier from Langer.

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TABLE I: Resource footprint of the entire parallel waveform-matching implementation using carry logic or a LUT-based adder for the 1-bit additions.

| Template length $n$ (samples) | Carry logic LUTs | LUT-based LUTs |
|------------------------------|------------------|----------------|
| 1280                         | 2,447,533        | 680,172        |
| 1400                         | 1,222,969        | 338,948        |
| 700                          | 611,651          | 169,386        |

1While the presented numbers of LUT utilization will not exactly match for any implementation on FPGA with older logic (e.g. LUT4 or CARRY4), the bigger picture will remain the same.
TABLE II: Features of our implementation, the trigger box [5], and icWaves [11]. Values adapted from similar list in [5]

| Feature                | Our implementation | trigger box [5] | icWaves [11] |
|------------------------|--------------------|-----------------|--------------|
| Algorithm              | Interval matching  | Interval matching | SAD         |
| Sample rate            | 10 GS/s            | 125 MS/s        | 200 MS/s     |
| Max. resolution        | 14-bit             | 14-bit          | 8-bit        |
| Template length        | 1400               | 1500            | (1 × 512) or (2 × 256) |
| Memory depth           | 10 000 k           | 60 k            | 8 000 k      |

Fig. 6: Trace with 256 AES-128 encryptions performed by the BeagleBone at 1 GHz.

model PA303. We recorded the side-channel signal with the ADQ7DC at 10 GS/s with a resolution of 14 bits.

The operation of interest was AES-128 encryptions which were performed as part of OpenSSL (1.1.1d) operations. We applied OpenSSL on 256 blocks of random data. We used the standard OpenSSL encryption without special hardware acceleration or similar optimizations.

SCA based on waveform template matching can be divided into three phases (see [16]): 1) the calibration stage, 2) measuring stage, and 3) evaluation stage. In the calibration stage, a waveform template is constructed, e.g., based on side-channel measurements from the DuT. In the measuring stage, the waveform template is applied for triggering, so that single COs can be detected on the side channel with pattern matching in real time and recorded for subsequent analysis. Finally, in the evaluation stage, the recorded traces of COs are used for further attacks such as key recovery. In the following, we concentrate on phases 1 and 2 which are directly related to waveform matching.

In order to calibrate our waveform matching design for this experiment, we first recorded the entire encryption process comprising all 256 AES-128 operations without knowing the exact timing of the COs. With the help of an algorithm by Trautmann et al. [10] for semi-automatically locating the COs in this trace and the knowledge that one encryption round of AES-128 takes 28 cycles, we were able to find the locations of the COs. The entire trace with all 256 encryption operations can be seen in Fig. 6. 254 of the 256 AES-128 encryptions were successfully found with the semi-automatic approach. The first encryption operations recorded in this trace are deformed, as is always the case for this device, which is caused by empty caches leading to a different pattern in the side-channel trace [5]. The trace of one of the 254 detected encryption COs can be seen in Fig. 7.

An averaged trace of the COs was then calculated with the information on the locations of the 254 well-formed COs. The averaged trace is shown in Fig. 8. It can then be used as a template c for the interval-matching approach.

However, in full resolution, the template has 2800 samples, which would overwhelm our implementation, as we can only fit 1400 samples into the current implementation. A simple solution to this problem is to reduce the number of comparisons between the template and the incoming trace t done by the waveform matcher: It is possible to only compare every 4-th value in the incoming trace t to our template c and still find the same matches as with a template at full resolution. While this reduces the number of Comparator instances per MatcherModule by a factor of 4, we still record and acquire data at 10 GS/s and also maintain the shift register SRG at full length. This is possible because SRG only uses LUTRAM, which is not the limiting resource. This stands in contrast to LUTs, which are the bottleneck of this implementation. We furthermore use a software environment to determine the offsets and threshold for interval matching based on the detected CO traces.

Finally, the parallel waveform-matching design was loaded onto the digitizer. With our calibrated configuration, we found all well-formed encryptions. There were also some malformed COs in the side-channel trace for our experiment. The first CO at the beginning of a batch execution or after an interrupt may well look different due to caching effects of our specific device under test and may therefore not be detected by waveform-matching. However, this is a general challenge of waveform matching and well-known among practitioners, see [5]. Still, techniques have been developed for successfully performing
side-channel attacks on the basis of waveform matching despite such malformed COs. A basic solution here is to omit the malformed COs or treat them differently. By following such an approach, successful DPA attacks even in the presence of not always well-formed encryptions have been shown in [2]. Therefore, such attacks could beneficially use our proposed design.

One major advantage of our measurement setup is that it does not need additional upstream analog circuitry such as an envelope detector or other filters for successful waveform matching, as is required in the related work. Since our waveform matching functionality is directly integrated into the pipeline of the digitizer, we can obtain traces of operations at a high sampling rate without the need for an additional oscilloscope or other hardware components.

**VI. CONCLUSION AND FUTURE WORK**

Waveform matching is one method of applying SCA on real-world systems without needing to modify them. In comparison to the state of the art, our proposed design can scale with faster ADCs and is capable of enhancing the matching speed by over 50 times. This will be important to enable implementation based attacks or SCA on faster and more complex systems.

Furthermore, an implementation and evaluation of our design in the pipeline of a high-performance digitizer shows that a one-device solution is possible without sacrificing performance. As a consequence of the less complex measurement setup, the work of SCA evaluators in the field will also be alleviated.

One challenge that accompanies a parallel, as opposed to a sequential, design is the increased resource demands. However, for most examples, a template that is sub-sampled will lower the resource demands while yielding accurate trigger results nonetheless, as demonstrated in our case study. For future work, an exploration of different techniques that methodologically minimizes a template without compromising accuracy is planned. Furthermore, other matching techniques that require fewer features in the template can also be under current investigation.

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