Running Neural Network Inference on the NIC

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Abstract

In this paper we show that the data plane of commodity programmable Network Interface Cards (NICs) can run neural network inference tasks required by packet monitoring applications, with low overhead. This is particularly important as the data transfer costs to the host system and dedicated machine learning accelerators, e.g., GPUs, can be more expensive than the processing task itself. We design and implement our system - N3IC - on two different NICs and we show that it can greatly benefit three different network monitoring use cases that require machine learning inference as first-class-primitive. N3IC can perform inference for millions of network flows per second, while forwarding traffic at 40Gb/s. Compared to an equivalent solution implemented on a general purpose CPU, N3IC can provide 100x lower processing latency, with 1.5x increase in throughput.

1 Introduction

With the slowdown of Moore’s law [22][13][23], the architecture of modern servers is evolving to include an increasing number of domain-specific co-processors dedicated to tasks such as cryptography, video processing and machine learning [26]. Network Interface Cards (NICs) are also following the same trend and now integrate programmable components, i.e., Systems-on-Chip (SoC), FPGA, within their hardware data path [16][54][44][20] to lower the pressure on the host CPU, which is usually the bottleneck [57].

Several efforts have already took advantage of end-host hardware programmability to improve data center scalability [15][16], applications performance [12] or specific functions such as load balancing [2], consensus protocols [35] and key-value store [39]. Lately, an increasing number of networking-related applications require machine learning inference as first-class-primitive [14][42]. However, the complex operations required by machine learning algorithms, specially deep neural networks, often do not allow such applications to effectively leverage programmable NICs [18].

In response to this, we design, implement, and evaluate N3IC, a solution for adding a lightweight neural network (NN) inference support to the list of tasks that can be efficiently run on commodity NICs. This idea aligns with the current trend of research that moves machine learning capabilities into programmable hardware, but takes a novel direction (See Figure 1). Recent efforts focused either on implementing basic machine learning algorithms, e.g., decision trees, using programmable switches [8][79], or deploying expensive and dedicated fully-fledged network-attached accelerators (e.g., BrainWave [49] and Taurus [70]). In N3IC, we design and
implement a NN executor that mainly uses already available hardware in the data plane of off-the-shelf programmable NICs, instead. NNs are general-purpose machine learning algorithms that suite a growing set of applications [80, 37, 36], but they are widely considered too resource-hungry and computationally complex to run on commodity NICs [8, 79]. We demonstrate that modern programmable NICs can run NN inference, thereby offloading a significant amount of computation from the CPUs, and enabling applications with strict timing constraints. In fact, we show that PCI Express (PCIe) data transfer overheads [55] to the host system can be more expensive than the actual NN inference process (§2).

We share the challenges of implementing NN executors taking into account both resource and computational constraints of today’s commodity programmable NICs (§3). We then report the design of N3IC (§4) on two different hardware targets: a System-on-Chip (SoC) based NIC from Netronome [53], and an FPGA-accelerated NIC (NetFPGA [83]). Our solution relies on a quantization technique known as binarization [10], which reduces the number of bits used to represent NN’s inputs and parameters. The resulting NN, i.e., Binary Neural Network (BNN), has low memory requirements in the order of KBytes, and its computation can be performed using much lighter mathematical operations with small impact on the considered use cases’ inference accuracy (§5). We provide three implementations of N3IC. First, leveraging existing NIC programming languages’ primitives, using microC for the Netronome NIC and P4 for the NetFPGA. In this last case, we developed a compiler that derives fully functional P4 code from a given NN architecture, which can be then synthesized in hardware with the P4-NetFPGA framework. Finally, we provide a third implementation that realizes NN inference with a dedicated hardware circuitry, which can be exposed as a new primitive to the high-level languages.

To evaluate the versatility of N3IC, we implemented three different use cases related to network monitoring: (i) traffic classification, (ii) anomaly detection, and (iii) network tomography. In the first two, we seek to identify specific patterns into the traffic data. The latter infers occupation levels of a datacenter’s switch queues using probe packets, by implementing a slightly modified version of SIMON [18]. Using the presented implementations, we show (§6) that N3IC can greatly improve the performance of typical networking applications that need relatively small NNs. Our evaluations show that N3IC can perform traffic analysis for millions of network flows per second, while forwarding traffic at 40Gb/s. Compared to a similar system implemented entirely on a general purpose CPU, N3IC can provide 100x lower processing latency, 1.5x higher throughput, and save precious CPU’s cores. Furthermore, N3IC allows applications to run NN inference even when their time budget is of few µs.

In summary, the main contributions of this paper are:

- We present N3IC, an approach to accelerate NN inference for network traffic on commodity programmable NICs, and implement it on two different hardware targets, showing the flexibility of our approach and its applicability on off-the-shelf NIC hardware.

- We share the three implementation designs: a microC-based implementation for the NFP4000 network processor; a P4-based implementation for the P4-NetFPGA framework; and a Verilog hardware design for the NetFPGA;

- We provide a compiler that generates fully functional P4 code from NN abstractions. The compiler targets both a software bmv2 switch and a P4 NIC, using the P4-NetFPGA framework.

- We present three different use cases related to network monitoring: (i) anomaly detection, (ii) traffic classification and (iii) network tomography and we study the trade-offs and benefits in offloading neural network inference on modern NICs.

2 Motivation

Given the wide availability of PCIe-attached off-the-shelf NN accelerators, i.e. GPUs, one may reasonably consider...
2.1 Observations

I/O operations are expensive. Host-attached accelerators, i.e., GPUs, may introduce considerable data transfer overheads, as they are generally connected to a host system via the PCIe bus (Figure 2). This rules them out as offloading engines for time-sensitive network applications. For example, offloading the computation of NN inference to a GPU requires the input data to enter the host system (first PCIe transfer), then to reach the GPU (second PCIe transfer), and finally to transfer the result back to the CPU (third PCIe transfer). If the NN inference result is needed for packet forwarding decisions, this may involve a potential additional transfer to the NIC (fourth PCIe transfer).

To better understand the overheads in place, we measured the time needed to transfer an increasingly bigger input vector to a GPU through the PCIe and then retrieve back just the result from the inference. We compared this with the amount of time needed to directly run the inference on the CPU itself for a variable-sized NN (Figure 3). The results show that transferring just few bytes of input vector and retrieving back the result from the GPU might already require 8-10µs. To put this in perspective, executing relatively small NNs directly on the CPU takes as much as a single transfer. For instance, an efficient binary NN with about 2k neurons takes about 8µs to be executed. Furthermore, depending on the specific use case, and as demonstrated in [5] in the context of traffic analysis, the NN might need less than 50 neurons. In this scenario, the CPU only needs about 400ns to run the inference, making inefficient the use of ML accelerators that need to be reached through PCIe. While batching the execution of multiple NNs together could be an effective way to reduce the data transfer overhead, it would also significantly impact the processing latency. For time sensitive workloads, NN inference is typically performed directly on the CPU, as it is a more effective solution than using a PCIe connected accelerators [24].

Observation 1: Running NN inference on a NIC could completely avoid crossing the PCIe bus and help in the execution of time sensitive workloads.

NN processing is memory-bounded in many cases. A NN is generally composed of several layers. Depending on the neurons’ interconnections and operations, different types of layers can be defined, and, accordingly, different types of NN. N3IC implements fully connected layers (FCs), which are the building block of Multi-layer Perceptrons (MLPs). Other well-known and widely used NNs are Recurrent NNs (RNNs) and Convolutional NNs (CNNs). However, in classification and prediction tasks for formatted and tabular data, with low dimensions and lower number of target categories, MLPs are usually used, being fairly efficient. Indeed, despite the popularity of RNNs and CNNs, large industries such as Google and Facebook report that the large majority (e.g., above 60%) of their NNs workloads requires the execution of MLPs [30, 25].
MLPs, compared to other NNs, are a better fit to the constraints of networking devices, mainly due to the computation profile of FCs, which require much lower computation than other types of layers as demonstrated in the following test. We used Intel’s optimized Caffe [32] to perform tests on a machine equipped with an Intel Xeon E5-1630 v3 CPU (4 cores@3.7GHz), and run VGG16 [67] as test workload. VGG16 is a well-known CNN with a sequential structure, with convolutional (conv) layers followed by FCs, which allows us to clearly observe the different computation profiles of such layers. We use a single core to perform the computations, and pre-load the model in the local memory.

With perf, we monitor the CPU’s performance counters for number of instructions, cycles and L3 cache misses. We use the Instructions per Cycle (IPC) rate as a proxy for the arithmetic intensity of the workload, i.e., the number of operations performed per byte of data loaded. Intuitively, high IPC and low L3 cache misses tell that the workload keeps most of the CPU’s pipeline busy. Low IPCs and high L3 cache misses are a good indicator of memory-bound workloads, i.e., a small number of operations is executed for byte of loaded memory.

Figure 4 shows that the IPC is high when executing convolutional layers, while it is low during the execution of FC layers. The increase in L3 cache misses shows that this happens due to the need to wait for data to be loaded from memory, confirming the relatively low arithmetic intensity of MLPs.

**Observation 2:** MLPs have relatively low arithmetic intensity. This makes hardware architectures optimized for fast memory accesses a good fit for their execution.

NICs processing load depends on traffic patterns. A NIC handling a bandwidth of 40Gb/s needs to process about 3 million packets per second (Mpps) when packets are 1500B in size. In contrast, for the same bandwidth, a NIC would need to process 15Mpps of size 256B, which is a 5x bigger processing load. Given that the hardware of NICs is often designed to handle worst case traffic scenarios, i.e., processing many small network packets, this creates opportunities to run additional operations without paying operational penalties. To illustrate this, we show in Figure 5 the throughput of a Netronome NIC when performing an increasingly higher number of per-packet operations, i.e, integer arithmetic over the received packet, beside the common parsing and forwarding tasks, when loaded with 25Gb/s of constant bit-rate traffic with packet sizes of 512B, 1024B and 1500B. The figure shows that as the packet size increases, the NIC can perform more per-packet operations in addition to its regular forwarding tasks, without affecting the forwarding throughput. Specifically, considering an average case of 512B input packets, typical for a data center scenario [61], the available budget is of 10K operations per-packet before trading with operational performance. Notably, the processing budget grows by ten times when the packets size doubles.

**Observation 3:** The relatively small arithmetic intensity of MLPs aligns well with the potentially available processing power of a NIC.

### 2.2 A motivating use case

NNs are a relevant tool for traffic classification [50, 42] and anomaly detection [33]. Usually, the end-to-end process requires the reception of packets, then the calculation of traffic statistics that will ultimately feed an NN in charge of producing the final result. In this scenario, a NIC usually unloaded the CPU only for the network flows statistic collection. The NN inference has to be entirely run on
the host’s CPU, which therefore has to continuously fetch the traffic statistics from the NIC’s hardware to perform the NN inference. Although the CPU no longer has to run expensive operations such as packet reception and statistics collection, the NN inference can already occupy an entire CPU core, even when performing optimized batched computation of the per-flow statistics.

In Figure 6, we show the performance achieved by using a single CPU core for NN inference. Here, the traffic analysis can scale to process up to 1.2M network flows per second, but only when performing input batching. Unfortunately, batching increases the processing latency from 10s of µs, for a batch of size 1, to 10s of ms, for a batch of size 10k. This hinders the implementation of time-sensitive applications relying on quick results. N3IC, instead, without using expensive hardware, allows the system to completely offload most of the computation using available NIC’s resources, thereby avoiding data movements, freeing CPU cores, providing timely results and reducing processing latency by up to 100x.

3 Neural Networks on the NIC

In this section we describe the challenges of supporting NN inference in the data plane of a commodity programmable NIC, and how we overcame them with N3IC.

Challenge 1: The need for small NN models: A typical NIC has at most few 10s of MBs of fast on-chip SRAM memory [53, 72, 72], which is commonly used to store the data required for packet processing. Small NNs, which are common in networking use cases [15], could fit their model’s parameters in such space. However, the on-chip memory needs to also host forwarding and policy tables. Such tables can easily take several MBs of memory, leaving little space available for the NNs. An important observation is that NNs, being inherently a tool of approximate computing [27], can effectively take advantage of compression and quantization techniques. These techniques reduce the number of bits used to represent the NN’s parameters, e.g., 8b instead of 32b, and are already widely applied to improve the efficiency of NN accelerators. Recent approaches have pushed quantization even further, using just few bits per parameter [38, 60, 81]. Effectively, this provides opportunities to reduce memory requirements by 2-8x even when compared to already efficient 8b representations. Although there is a trade-off between memory requirements and NN accuracy, for many use cases the drop in accuracy is usually tolerable [38].

Challenge 2: The need for a low complexity algebra: A second major constraint is related to the arithmetic capabilities of networking devices. Networking hardware often only has the ability to perform bitwise logic, shifts and simple integer arithmetic operations [69]. Implementing the operations required by a NN, such as multiplications, may not always be possible. Certain quantization techniques help in addressing this issue, since they can simplify the arithmetic operations required to compute a NN. Indeed, the already mentioned 8b quantization is used by the TPU [30] to enable the use of integer multiplications in place of floating point. More interestingly, some quantization techniques can even completely change the nature of the operations required to compute a NN. For example, log domain quantization [38] uses log base-2 values to represent NN parameters, which enables replacing multiplications with simple shift operations.

Challenge 3: The need for hardware compatibility: The number of currently available quantization techniques is fairly large, e.g. [28, 38, 60, 81, 21, 9, 82, 40]. However, our solution space is reduced by a third final constraint: networking devices have quite heterogeneous hardware ar-
architectures, ranging from SoCs, FPGAs, embedded CPUs to switching ASICs. Thus, the selected quantization technique should guarantee a wide hardware compatibility. Effectively, this translates into selecting a quantization approach that uses arithmetic operations widely supported in the above architectures.

Algorithm 1: FC processing function. Weights and inputs are in groups of block_size.

| Input | x input vector, w weights matrix, n num. of output neurons; |
|-------|-----------------------------------------------------------|
| Output| y output vector                                           |
| 1     | block_size ← 32;                                          |
| 2     | assert(n % block_size == 0);                              |
| 3     | sign_thr = (len(x) * block_size)/2;                       |
| 4     | y[n/block_size] ← {0};                                    |
| 5     | for neur ← 0 to n by 1 do                                  |
| 6     | tmp ← 0;                                                  |
| 7     | for i ← 0 to len(x) by 1 do                               |
| 8     | | tmp += popcnt(w[neur][i] ⊙ x[i]);                        |
| 9     | end                                                       |
| 10    | if tmp >= sign_thr then                                    |
| 11    | | tmp_out |= (1 << (neur % block_size));                   |
| 12    | end                                                       |
| 13    | if (neur + 1) % block_size == 0 then                       |
| 14    | | y[neur] ← tmp_out;                                        |
| 15    | | tmp_out ← 0;                                             |
| 16    | end                                                       |

3.1 The solution adopted by N3IC

With the previous challenges in mind, we finally select binary neural networks (BNN) as the N3IC’s quantization technique to implement NN in the network data plane of a NIC. A BNN uses only 1b to represent inputs and weights [10], and replaces multiplications with a combination of simpler operations, i.e., bitwise XNOR, and population count (popcnt). Compared to other solutions, such as log domain quantization, which requires shift operations, BNNs provide better opportunities for parallelizing the computation. Finally, despite the significantly lower computation and memory complexity, BNNs can still achieve remarkable results. In many tasks, BNNs provide prediction accuracy only 3-10% points lower than the accuracy of the much heavier non-quantized models [43]. While this may be a significant drop for some use cases, it still enables such models to be used in a large set of applications, as we will discuss more thoroughly in §5. Precisely, starting from the original NN, we first applied the binarization technique from Courbariaux and Bengio [10], which is based on a canonical back-propagation algorithm. This solution ensures that the NN’s weights converge to values included in the [-1, 1] range, and that are normally distributed around the 0. This helps in losing only little information when the real weight values are mapped to just two values, i.e., 0 and 1 [10]. In fact, the MLP’s weights obtained after training are still real numbers, and an additional final step is required to obtain the binarized weights. This is done by setting the NN weights to 0 if their value is negative or 1 otherwise.

We implemented the processing of a BNN with Algorithm 1 which parametrizes the BNN operations according to the variable block_size. This corresponds to the largest contiguous set of bits on which an operation can be performed in the target hardware executor. For instance, a modern CPU could have a block_size of 64, corresponding to the CPU’s registers size. Specifically, for each of the NN’s neurons, the algorithm performs (1) a XNOR operation on the input with the weights vector, (2) a population count operation and (3) a comparison. The comparison checks if the result of the population count is smaller than half the number of neuron’s inputs, in which case the neuron’s output is 1.

3.2 N3IC architecture

The above described BNN algorithm is integrated in the NIC data plane as depicted in Figure 7. The NN Executor is separated from the forwarding module, although some implementations may allow both instances to be integrated.
The NN Executor is triggered either by the reception of a network packet, or directly by the forwarding module in charge of the regular packet processing. In fact, the forwarding module may collect network flows statistics and only trigger the NN Executor when enough packets have been received.

The input selector allows to choose the input of the NN executor between a packet field or a specific memory area, e.g., containing collected flow statistics. The output selector is used instead to write the inference output either to a packet field, or to a specified memory location. When the input and output selectors are configured to read or to write to a packet field, the NN Executor works as an inline module.

4 Implementations

In this section we describe the implementation of N3IC on two different programmable hardware targets: a SoC-based (NFP4000 Netronome [53]) and an FPGA-based (NetFPGA [83]) NICs. We first show the implementation of N3IC using only the currently available NICs’ primitives accessible through high level programming, i.e., microC and P4. We then describe the design of a new hardware module that implements a dedicated BNN executor using Hardware Description Language (HDL). This provides a pathway to enable the use of our solution as a primitive for high-level languages.

4.1 SoC NIC: Netronome NFP4000

The NFP4000 architecture comprises several different hardware blocks. Some of them are dedicated to network-specific operations, e.g., load balancing, encryption. Others are bound to programmable components that are used to implement custom packet operations. The architecture is shown in Figure 8 and comprises tens of independent processing cores, which in Netronome terminology are named micro-engines (MEs). MEs are programmed with a high level language named micro-C, a C dialect. Each ME has 8 threads, which allow the system to efficiently hide memory access times, e.g., context switching between threads as they process different packets. MEs are further organized in islands, and each island has two shared SRAM memory areas of 64KB and 256KB, called CLS and CTM, respectively. Generally, these memory areas are used to host data required for the processing of each network packet. Finally, the chip provides a memory area shared by all islands, the IMEM, of 4MB SRAM, and a memory subsystem that combines two 3MB SRAMs, used as cache, with larger DRAMs, called EMEMs. These larger memories generally host forwarding tables, access control lists and flow counters. MEs can communicate and synchronize with any other ME, irrespective of the location. Communications across islands take longer and may impact the performance of a program.

When developing N3IC on this hardware platform we have to share the MEs and memory resources between tasks, thus, we had to strike the right balance between the needs of quickly forwarding network packets and running NN inference. For both processing tasks the main bottleneck is the memory access time. Thus, selecting the memory area to store NN’s weights has played a major role in our design.

If the NN is small, as for the use cases considered in this paper, it is worth considering the fastest available on chip memories, i.e., the CTM and CTS, with an access time of less than 100ns [53]. However, the CTM memory is usually dedicated to packet processing tasks, being the memory used by the NFP to store incoming packets and making them available to the MEs. Thus, using the CTM may impact packet processing and should be avoided. Because of this, we decided to load the NN’s weights at configuration time in the CLS memory. At boot time, each of the MEs’ threads registers itself to be notified of packets reception, with the NFP taking care of distributing packets to threads on a per-flow basis. This is a standard approach when programming the NFP. Thus, whenever a new packet is received, the NFP copies its content in an island’s CTM, and notifies one of the island’s threads to start packet processing. The notified thread performs regular packet processing tasks, such as parsing, counters update, forwarding table lookups. If a trigger condition is verified, the thread starts the processing of the configured NN. Typical conditions could be the arrival of a new flow, the reception of a predefined number of packets for a given flow, the parsing of a given value in a packet header. To run the NN, a thread performs Algorithm 1 with input and weights packed in 32b integers, i.e., block size is 32. As a consequence, multiple threads can perform NN inference in parallel (Figure 8).
4.2 From Neural Networks to P4 and to NetFPGA

P4 [5] is a domain-specific, platform agnostic language for the programming of packet processing functions. We designed a compiler that transforms an NN description into a N3IC implementation described with P4. In principle, the P4-based implementation allows us to separate the N3IC solutions from the underlying hardware-specific details, thus generalizing our approach. However, as we will discuss at the end of the section, the target hardware architecture has still an important impact on the final implementation.

Compiling NN to P4. Our compiler, NNtoP4, takes as input a NN description, i.e., number of layers with corresponding number of neurons, and generates P4 code for a generic P4 target based on the PISA architecture. PISA is a spacial forwarding pipeline architecture, with a number of match-action units (MAUs) in series. A packet header vector (PHV), containing both the input packet and metadata information, is passed through the MAUs to perform the programmed processing tasks. Each MAU combines a table memory structure, for quick lookups using the PHV fields, with arrays of ALUs that perform operations on such fields. The code generated by NNtoP4 implements a function, on top of the PISA architecture, which reads the input value from the PHV, performs the NN execution and writes back to a PHV’s field the result of the computation. The NN weights are stored in the MAUs’ fast memories to enable runtime reconfiguration. The generated P4 code also includes headers definition, parser, de-parser and control blocks. The code can therefore be easily extended to integrate with any other required packet processing function.

Algorithm 2: popcount implementation. B is the number of bits required to represent n. \(X_y\) indicates the y-times concatenation of the binary number X and \(Z_{jW}\) is the concatenation of the binary numbers Z and W.

| Input | :n input number; |
| Output | :c output counter |
| 1 | \(L \leftarrow \log_2 B;\) |
| 2 | \(\text{bits}[L] \leftarrow \{1, 2, 4, ..., B/2\};\) |
| 3 | \(\text{masks}[L] \leftarrow \{01jB/2, 0011jB/4, 00001111jB/8, ..., 0jB/2j1jB/2\};\) |
| 4 | \(c \leftarrow n;\) |
| 5 | for \(i \leftarrow 0 \text{ to } L - 1 \text{ by 1 do}\) |
| 6 | \(c \leftarrow (c \& \text{masks}[i]) + ((c >> \text{bits}[i]) \& \text{masks}[i]);\) |
| 7 | end |

The basic operations needed to implement Algorithm 1 are (1) XNOR, (2) popcount and (3) SIGN function. Executing a XNOR and a comparison (SIGN) is readily supported by the P4 language. Unfortunately, the popcount operation is not. The main issue is that its execution time depends on the input size, which makes popcount difficult to implement in networking hardware, and therefore not supported in the PISA architecture. To overcome this issue using only current P4 primitives, we adopted the solution proposed in [4] and reported in Algorithm 2. The idea is to implement the popcount by combining basic integer arithmetic and logic operations in a tree structure whose depth is dependent on the input size. A tree structure is easily parallelizable and allows the distribution of computations in the pipeline, with the processing of different tree’s levels assigned to different pipeline’s stages.

Overall, the processing includes five steps, each one mapped to a logical pipeline stage, except for the popcount which requires multiple stages, depending on the input size (cf. Figure 9). In the first step, the NN input is repli-
Porting P4 code to NetFPGA. The NetFPGA is a programmable hardware platform with 4x10GbE Ethernet interfaces incorporating a Xilinx Virtex-7 FPGA. We implemented N3IC on top of the reference NIC project provided with the main NetFPGA-SUME code base. We used the P4-NetFPGA workflow to port the generated target-independent P4 code to the NetFPGA platform. The P4-NetFPGA workflow is built upon the Xilinx P4-SDNet compiler and the NetFPGA-SUME code base. It translates P4 code to HDL (Verilog), and integrates it within the NetFPGA pipeline.

The P4-NetFPGA workflow required several adaptations to P4toP4, in order to meet the FPGA resources and timing constraints. First, the P4-SDNet compiler does not support if statements among the operations of a MAU. Thus, we replaced all the if statements required by the SIGN function using a combination of bitwise logic operations and masks. Second, MAUs use the CAM IP core from Xilinx to implement lookup tables, which restricts the maximum width size that can be used for each entry. Consequently, a maximum of 32B can be fetched from memory every time a table is called, limiting the number of neuron weights that could be loaded in parallel by each table. To overcome this issue we had to write the weights as constant values in the MAU’s operations code, effectively trading the possibility to perform runtime reconfiguration with the ability to compute more neurons in parallel. Finally, P4-SDNet is capable of performing a large number of operations on a field in a single MAU. This is in contrast with ASIC targets, which are instead usually constrained to execute a single operation per MAU. This allowed us to describe several steps of a BNN computation in a single MAU, thus reducing the number of MAUs required to implement the BNN computation.

4.3 BNN inference primitive

Finally, we designed a dedicated NN executor for the NetFPGA in HDL, which allows the NIC to expose BNN inference as an offloading primitive. Figure 10 shows the
architecture of our NN executor as per Algorithm 1. The module is composed by multiple blocks. Each of them performs the computation of a single NN layer, and can be parametrized providing the sizes \( n \) and \( m \) for the input and output vectors, respectively. Together, the blocks build an NN Executor for specific NN architectures. For instance, three of these blocks are required to build a 3 layers MLP. The NN layer weights are stored in the FPGA on-chip memories, i.e., Block RAM (BRAM). The BRAMs are organized as tables with a number of rows strictly dependent to the amount of neurons and with a width of 256b. Each row can be read in 2 clock cycles and, depending on the size \( n \) of the input vector, can store one or multiple weights, e.g., 1x256b or 16x23b. The BRAMs are shared by all the blocks of a NN Executor module.

A single block is a pipeline of three stages. The first reads the weights from the BRAM and performs the XNOR with the input. The second performs a first step of the popcount. Here, we create Lookup-Tables (LTs) of 256 entries each, in order to associate one 8b integer (address) to the corresponding population count value. Each block has \( n/8 \) of these LTs. As a consequence, for a 256b input we create 32 LTs that operate in parallel. In the last stage, the LTs outputs are summed together, the sign function is applied on the final sum and its result is stored in one of the \( m \) bits of the output register. If multiple weights are placed in a single BRAM’s row, the module performs the execution of several neurons in parallel.

5 Use cases

In this section, we show how N3IC can benefit applications from both backbone and datacenter networks. Table 1 summarizes the three implemented use cases. More details are provided in the Appendix.

#1: Traffic classification. Backbone network operators use traffic classifiers to make a best-guess about the type of traffic carried by a flow, in order to assign priority classes and improve user experience [31]. This operation is often carried at the network edge [76] using software middleboxes for enhanced flexibility [45, 46, 66] at the cost of reduced performance [65, 3, 34]. In this context, N3IC can be used to reduce the amount of traffic processed by the software classifier by performing a pre-classification task to reduce the pressure on the host CPU (See Figure 11).

To illustrate this use case, we used the UPC-AAU dataset [7]. The dataset has more than 750K flows, including 76 commonly used applications and services, which account for 55GB of packet-level data. Here, N3IC can be used to classify the traffic class that contributes the most. In the UPC-AAU dataset, this corresponds to the identification of P2P traffic. With this approach, N3IC would be in charge of directly classifying P2P traffic, while passing the rest to the software middlebox running on the host system for more fine-grained classification. That is, N3IC can be used as an effective flow-shunting system. We trained a binarized MLP to classify traffic in two classes (i.e., P2P and other), and deploy it with N3IC. On this classification task, a binarized MLP with 32, 16, 2 neurons is capable of achieving 88.6% accuracy, while requiring only 1KB of memory.

#2: Anomaly detection. Anomaly detection is the practice of analyzing traffic to seek anomalies and reveal suspicious behavior [59]. Unfortunately, to cope with the ever-increasing large traffic volumes, operators only perform analysis on randomly chosen samples of the flows [75]. With N3IC, instead, we can allow software middleboxes deployed at the edge network to perform continuous flow-level analysis for all the flows, without impacting the resource usage of the host CPU.

For this use case we used the the UNSW-NB15 dataset [52], which provides over 170K network flows labeled in two main categories, i.e., good, bad, and their flow-level statistics. A regular MLP with 3 FCs of 32, 16, 1 neurons achieves 90.3% accuracy on this dataset, requiring
### Table 1: Use cases implemented with N3IC.

| Use Case          | Input size (bits) | NN size (neurons) | Memory (KBytes) | Accuracy (%) |
|-------------------|-------------------|-------------------|-----------------|--------------|
| Traffic           | 256               | 32, 16, 2         | 1.1             | 88.6         |
| Classification    | 256               | 32, 16, 2         | 1.1             | 85.3         |
| Anomaly Detection | 152               | 128, 64, 2        | 3.4             | 92.0         |
| Network Tomography|                  |                   |                 |              |

35KB of memory. Using a similar binarized MLP (32, 16, 2 neurons and 1KB in total of memory) with N3IC achieves an 85.3% accuracy, instead. While the N3IC NN gives a 5% lower accuracy, it is applicable to large volumes of traffic, enabling a type of security monitoring that would not be economically viable otherwise.

**#3: Network Tomography.** In datacenter networks, end-host based network monitoring approaches are being explored for their ease of deployment and lightweight operations [51, 19, 18]. For example, SIMON [18] periodically sends probe packets to measure datacenter’s network paths delays. This allows to accurately infer congestion points and the size of the related queues. SIMON uses MLPs to speed-up the inference tasks. However, it relies on GPUs to run the MLPs, which makes the tool better applicable for debugging than for creating a feedback loop between measurement and control, i.e., for path selection. Here, notice that according to [18] the probe periodicity depends on the fastest link speed. For instance, in the presence of 10Gb/s links, probes have to be sent every 1ms, while for 40Gb/s links this lowers to 0.25ms. As a consequence, for this use case to work at higher link speeds and in real time, the execution latency has to be lower than the probe sending periodicity. This can be challenging considering I/O overheads and MLP processing time as previously discussed in [2]. With N3IC, we implemented a modified version of SIMON that can quickly identify congestion points, and timely notify them to the network control plane.

We tested the use case simulating a CLOS-like Fat Tree datacenter network with ns3 [74], using different link speeds (from 100Mb/s to 10Gb/s) and traffic workloads. Following the methodology suggested by [18], we split the problem of inferring queue sizes in multiple sub-problems, each targeting a subset of the queues. This allows us to run smaller MLPs on each of the NICs. Unlike SIMON, our approach does not infer the actual size of a queue, but it only infers which queues are bigger than given thresholds levels. This information is usually sufficient for the control plane to take a flow-steering decision, while more accurate inferences, e.g., for debugging, can be still run offline (See Figure [12]).

Each binarized MLP running with N3IC has 19 probes’ one-way delays as input, and 128, 64, 2 neurons. A NIC can run multiple of these NNs, since each of them infers the congestion status of a specific queue. Across all the queues of the simulated network, we achieve a median accuracy in predicting a congested queue above 92%.

### 6 Evaluation

In this section we present the experimental evaluations of N3IC. We report and discuss the end-to-end performance of the use cases presented in §3 and evaluate the scalability of the three implementations with targeted micro-benchmarks. More details alongside the performance of alternative design choices are discussed in appendices.

**Testbed.** Unless stated otherwise, we run all the tests on a machine equipped with an Intel Haswell E5-1630 v3 CPU and either a single Netronome Agilio CX SmartNIC, with an NFP4000 processor, or a NetFPGA-SUME. The Haswell is clocked at 3.7GHz, the NFP at 800MHz, and the NetFPGA at 200MHz for both the N3IC-FPGA and N3IC-P4 implementations. The NIC under test is connected back-to-back to a 40Gb/s capable DPDK packet generator. The host system runs Linux, kernel v.4.18.15.

**Comparison term.** We compared our prototypes with a software implementation that runs binary layers (bnn-exec), available at [58]. bnn-exec has been written in C, and optimized for the Haswell CPU, with some parts in assembler to take fully advantage of the CPU’s architecture features, such as AVX instructions. We setup bnn-exec to read flows statistics/data from the Netronome NIC and ran bnn-exec only with the...
Figure 13: For traffic analysis, N3IC implementations match the offered load of 1.8M inferences per second, while forwarding packets at 40Gb/s. This is 1.5x the maximum throughput provided by bnn-exec.

Figure 14: For traffic analysis use cases, N3IC implementations can provide at least 10-100x lower latency than bnn-exec, avoiding the need of performing batching to amortize data transfer costs.

Figure 15: N3IC-FPGA can support the network tommography use case even in fast 400Gb/s networks with probes sent every 25μs. N3IC-P4 can only run this use case with smaller and less accurate NNs.

Figure 16: Box plot of the accuracies for the predicted queues in the network tomography use case. Larger NNs have longer execution latency but better accuracy.

6.1 Traffic analysis use cases

In both the traffic classification and anomaly detection use cases, we configured the NICs to collect flow statistics. We assumed that the provided traffic contains 1.8M flows per second, which need to be analyzed by running NN inference. This is a challenging load for a single server, being more common in ToR switches handling high throughput user-facing services. Here, we observe that if N3IC can meet this performance goal, it is likely to be capable of handling a large range of ordinary use cases.

We first measured the NIC performance when only collecting flow statistics, that requires for each received packet: packet parsing; a lookup in a hash-table for retrieving the flow counters; and updating several counters. The Netronome provides its 40Gb/s line rate only with packets of size 256B (18.1Mpps) or bigger. This is achieved using 90 out of the 480 available threads, and it is inline with the device’s expected performance for such class of applications. The NetFPGA, instead, is capable of forwarding 40Gb/s with minimum size (64B) packets while collecting flow statistics.

We summarized the throughput results in Figure 13. The N3IC implementations can all achieve the offered throughput of 1.81M flow analysis/s, while forwarding packets at 40Gb/s (40Gb/s@256B in the case of the Netronome). That is, N3IC does not reduce the packet forwarding performance of the NICs. In comparison, even if using larger batch sizes, bnn-exec is unable to cope with such load, when running on a single CPU core. bnn-exec maximum throughput is 1.18M analyzed flows/s, when using very large batches of 10K flows. More interestingly, Figure 14 shows that N3IC implementations provide also a low processing latency, with a 95-th percentile of 42μs for N3IC-NFP, and only 2μs and 0.5μs for N3IC-P4 and N3IC-FPGA, respectively. In comparison, for bnn-exec to achieve a throughput above the 1M flows/s, the processing latency is 1ms and 8ms with batch sizes 1K and 10K, respectively.

Result 1: when performing traffic analysis, N3IC saves at least an entire CPU core, while providing a 1.5x higher throughput and 10-100x lower processing latency than a system running on the host’s CPU.
6.2 Network Tomography

When testing the network tomography use case, the NIC stores the one-way-delay value for the received network probes, before passing them to the analysis engine, i.e., either N3IC or bnn-exec. Here, processing latency is the critical performance indicator, since in networks with 40, 100, 400Gb/s links, SIMON requires a new set of probe packets to be generated every 250, 100, 25µs, respectively [18].

Figure 15 shows that bnn-exec provides a processing latency of about 40µs, which is within the budget of 100µs [19]. However, upcoming network links of 400Gb/s could not be supported, since they would lower the periodicity of the probes to 25 µs [18]. N3IC processing latency for SIMON’s NN with 128, 64, 2 neurons is 170 µs for N3IC-NFP and below 2 µs for N3IC-FPGA. As we further clarify next, N3IC-P4 cannot scale to run such NN, and can only run the smaller 32, 16, 2 neurons networks with about 2 µs of delay, at the cost of reduced accuracy. In Figure 16 we show the accuracies for the predicted queues, using different network sizes. Larger networks improve accuracy by up to 10 percentage points. Thus, for future high-performance networks, unless a lower accuracy with a smaller NN is tolerable, only N3IC-FPGA can meet the SIMON’s timing constraints.

Result 2: compared to a host-based system, for low throughput but latency-sensitive use cases N3IC-FPGA can reduce processing latency by 20x. This enables applications like SIMON to run in real time in networks running at 400Gb/s and beyond.

6.3 Neural Network size

We now evaluate the processing throughput and latency when varying the size of the binary neural network. We performed this evaluation fully loading N3IC, and by executing a single FC layer with 256 binary inputs. We varied the number of neurons to be 32, 64 and 128 [11].

We can use a batch size of 1 in this use case, since high-throughput is not required.

Notice that the FC size is number of input times number of neurons: the FC layer with 128 neurons has 4KB of weights, i.e., 4x the size of

Figure 17 and Figure 18 show that both metrics have a linear decrease/increase with the NN size for N3IC-NFP and N3IC-FPGA, which is expected. In comparison, N3IC-P4 throughput results are much higher for an FC with 32 and 64 neurons. Unfortunately, results for 128 neurons are missing. As anticipated, N3IC-P4 could not scale to handle such layers. Both results can be explained with the constraints imposed by the PISA architecture as implemented by the P4-NetFPGA toolchain. The computations of the NN described by P4 are expanded and unrolled in the FPGA, to serialize the execution in the pipelined model implemented by P4-NetFPGA. This consumes a large amount of the FPGA resources, thereby providing very high throughput at the cost of limited scalability.

Result 3: N3IC-NFP’s and N3IC-FPGA’s processing throughput decreases linearly, while latency increases linearly, with the NN size. N3IC-P4 does not scale to larger NNs.

6.4 NIC resources usage

Finally, we quantify the NIC resources needed by N3IC prototypes to run the NNs used in the traffic analysis use cases.

In the NFP case, N3IC has to store the NN’s weights in the NFP4000’s memory system. The NNs used with the traffic analysis use cases require 1.5% of the CLS memory, and 480 threads to face the offered load, instead of the NN used for the traffic analysis use cases.
of the 90 required to achieve line rate throughput when the NIC is only collecting flow statistics. Here, it should be noted that it is possible to use less threads, as well as the larger and slower EMEM memories to store NN’s weights, if a performance drop in NN inference throughput is acceptable. For instance, using only 120 threads, i.e., 30 additional thread compared to the baseline, reduces the throughput of flows analyzed per second by 10x (more details in the Appendix). This still provides the ability to analyze over 100k flows per second, which is sufficient for many workloads.

In the NetFPGA cases, we measured the hardware resources required to synthesize N3IC implementations on the Virtex7 FPGA, and compare them to the standard NetFPGA reference NIC design’s resources. Table 2 summarizes the results. N3IC-FPGA requires only an additional 0.6% and 1.2% of the FPGA’s LUTs and BRAMs, respectively. The N3IC-P4 implementation, as anticipated, requires a more significant amount of resources, with an additional 22% for both LUTs and BRAMs, when compared to the reference NIC.

It is worth noticing that N3IC-FPGA is designed to match the required performance for the use cases, using minimum resources. The design allows for computing neuron results serially in a loop structure. E.g., we are able to match the throughput of N3IC-P4 for a FC layer of 32 neurons by using 16 NN Executor modules in parallel within N3IC-FPGA. The N3IC-FPGA’s throughput scales linearly with the number of modules, but so does the resources usage, which grows to additional 10% of the LUTs and 19% of the BRAMs.

Table 2: NetFPGA resources usage. N3IC-FPGA requires little additional resources. N3IC-P4 uses a large amount of NIC resources due to the PISA computation model constraints.

| DESIGN      | LUT (#, % TOT) | BRAM (#, % TOT) |
|-------------|----------------|-----------------|
| REFERENCE NIC | 49.4k, 11.4%   | 194, 13.2%      |
| N3IC-FPGA   | 52.0k, 12.0%   | 211, 14.4%      |
| N3IC-P4     | 144.5k, 33.4%  | 518, 35.2%      |

7 Discussion

Our evaluation results show that N3IC can benefit a number of networking use cases. However, like in similar solutions that leverage in-network computation [48, 35, 39, 11, 41, 64, 8], the benefits of bringing the inference closer to the wire come at a cost: (1) there is a need to convert the machine learning models in binary NNs; and (2) applications have to be designed taking into account the network-host split.

A second interesting observation is that it is possible to readily implement N3IC on commercial programmable NICs, using existing programming models such as microC and P4, even though these implementations come with some limitations. N3IC-NFP is unable to meet latency requirements in the order of the µs, while N3IC-P4 is inefficient in using the hardware resources, which significantly limits the NNs maximum size. Both limitations can be overcome if the NIC supports natively binary NN execution as a primitive with a dedicated hardware module, as shown by N3IC-FPGA. In fact, our tests show that supporting such primitive comes at very little overhead in terms of required hardware resources.

Furthermore, N3IC-FPGA can be considerably more efficient in running the NNs, thereby enabling larger NNs, or even supporting multiple different NNs at the same time. For instance, in the network tomography use case, our modified version of SIMON runs several small NNs, each predicting the congestion status of a given queue. In N3IC-NFP, running them requires a good share of the network processor’s threads to compute the NNs in parallel, leaving little space for other computations. Instead, N3IC-FPGA uses a single NN executor module, which serially processes NNs one after the other, while still respecting

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Result 4: N3IC-FPGA consumes a very small fraction of the NetFPGA resources, and both N3IC-FPGA and N3IC-NFP can be configured to trade-off used NICs’ resources with provided performance.

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12 We did not optimize the NN Executor modules to share the use of CAMs across modules. It is thus likely possible to considerably reduce this BRAM utilization if needed.
the strict timing constraints of the use case. Each NN execution takes in fact few µs, and given the small resource overhead of the NN executor module, it would be possible to include multiple of them if the need arises.

Finally, it should be noted that N3IC is not a generic tool to run any NN on the NIC. For large NNs, e.g., with thousands of neurons, its execution time may grow significantly, making the overhead of the PCIe transfer relatively lower. In such cases, a better choice is the use of a different NN executor, i.e., BrainWave and Taurus, or keeping the computation on the host system. More details in the Appendix.

8 Related Work

N3IC relates with the works that move machine learning capabilities into programmable hardware. This has been explored in the context of programmable switches [8, 29], or by using fully-fledged network-attached accelerators [49, 70]. In this paper, instead, we show that it is possible to design and implement a significantly smaller scale NN executor in the data plane of commodity off-the-shelf programmable NICs.

In this direction, we extend some ideas presented in [68, 62]. However, those works focused either on a conceptual design for RMT [6] switches [68], or on end-host ML applications, in which the NIC works as a co-processor for CNNs running on the host. Instead, in this paper, we present a complete evaluation of BNN executors on two NICs, propose a dedicated hardware-native implementation, and include an end-to-end evaluation of three networking use cases, with related trade-offs in terms of model size and specific hardware limitations. N3IC can be also positioned in the larger trend of in-network computing research. In fact, researchers have been exploring ways to apply programmable switches to domains not necessarily related to networking, such as key-value store [41], distributed consensus [11], and the acceleration of parameter servers for ML model training [63, 64]. Another related area is the design of hardware for NN accelerators. A valuable survey on the topic is provided by [71]. Particularly relevant to our work are architectures such as YodaNN [1] and FINN [77]. Finally, while not directly related to N3IC, recent work on the security of network applications that use machine learning [47] is likely to influence developments in this area.

9 Conclusion

In this paper, we presented N3IC, a technique to run neural networks in the data plane of commodity programmable NICs. We experimentally evaluated N3IC on the Netronome NFP4000 and on the NetFPGA. We showed that N3IC can greatly benefit network applications discussing three use cases: traffic classification, anomaly detection and network tomography. Our results show that N3IC can be readily implemented in existing commercial programmable NICs. By doing so, in the traffic analysis use cases, we demonstrated that N3IC provides 1.5x higher throughput and 100x lower latency than a state-of-the-art software implementation, while saving precious CPU resources. At the same time, supporting N3IC as a primitive with dedicated hardware requires only little additional hardware resources: the N3IC NetFPGA implementation increases the logic and memory resources of a standard NIC design by less than 2%, and it enables a real time network tomography use case, which would be otherwise unfeasible.

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A Netronome: implementation details

This section reports additional detail regarding the N3IC implementation on the Netronome NFP4000 when running large NNs. Netronome NFP4000 NICs have several different memory areas, with different sizes and access performance. Table 3 summarizes the memory properties.

| MEMORY TYPE | ACCESS TIME (NS) | MEMORY SIZE |
|-------------|-----------------|-------------|
| CLS         | 25              | 64KB        |
| CTM         | 62.5            | 256KB       |
| IMEM        | 187.5           | 4MB         |
| EMEM        | 312.5           | 3MB         |

When NNs are large, running them in a single ME’s thread would take a long time, making the use of multiple threads more effective, even if synchronization among threads incurs some overhead. Furthermore, the use of multiple threads allows the NFP to context switch them when waiting for memory, hiding memory access time and enabling a more effective use of the MEs’ processing power. For this reason depending on the NN size, we provided two different operation modes for N3IC over Netronome: (1) data parallel and (2) model parallel (cf. Fig[19]. The former, described in [4], is preferable when NN size is small. The latter, instead, when NN is big. In Model Parallel mode MEs’ threads are configured with two different types of processing tasks. A first subset of threads registers for packet reception notification. We call such threads dispatchers, and distribute them evenly across the available MEs and islands. In our implementation, we empirically found that two of such threads per ME is enough to achieve our performance goals. The second subset of threads, named executors, is instead dedicated to the processing of NNs, and organized in an execution chain. At boot time, dispatchers registers themselves for packet reception notifications. When a new network packet is received, the notified dispatcher parses the packet and performs the regular forwarding function. If a NN processing is triggered, a NN processing function is executed by the MEs’ threads in the execution chain. The dispatcher works as a coordinator for the NN processing, by starting the processing of one NN layer, and waiting for the result before starting the processing of the next layer. Figure 20 depicts this process.

**Execution Chain** The execution chain is statically defined, with each thread knowing its predecessor and successor.
threads at boot time. To start processing a layer, the dispatcher notifies the first thread in the chain with a start notification, which is then propagated throughout the chain, with each thread notifying its successor, until the last thread. After receiving the start notification, and sending it to the next thread in the chain, a thread performs the computation of a subset of the current layer’s neurons, with the actual number depending on the number of neurons in the layer and the level of configured execution parallelism. Each of the threads is an executor from the perspective of N3IC, so the configured number of executors (threads) defines the level of parallelism. For instance, for a layer with 4096 neurons, and using 128 executors, each executor would be in charge of computing 32 neurons. This effectively means, e.g., that N3IC would use 32 MEs, and 4 threads per ME, with each of the threads processing 32 neurons: $32 \times 4 \times 32 = 4096$. The execution of the neurons happens like in the data parallel case, with the main difference being that the model’s weights are stored in the DRAM-backed EMEM. Here, the weights are placed in a contiguous memory space, which allows an executor to directly point to the weights of a set of neurons given its position in the execution chain. At the end of a layer computation, each executor writes its final result to the global IMEM memory, from which the dispatching thread can read it. The last executor in the chain sends an end notification to its predecessor after writing its portion of the result to IMEM. The notification is propagated backward through the chain as all executors conclude their computations and write their results, until it is received by the dispatcher. Here, either the computation for a new layer is started or the final result is collected.

It is worth noticing that the spatial organization of the MEs, which are distributed across islands and at different distances from each other, makes more efficient the notification chain, when compared to other mechanisms, such as broadcast messages. That is, the notification system is faster even if some MEs remain idle while waiting to propagate the end notification back to the dispatcher. Unfortunately, explicit notifications are required since each ME’s execution time depends on the memory reads from the EMEM, which may take a variable amount of time. Second, the notification propagation time is relatively short, making the use of an asymmetric number of threads (or neurons to compute) per-ME inefficient. For instance one could assign more work to MEs early in the chain, but this in fact rises a problem of stragglers that harms the overall performance.

## B Evaluation details

### B.1 NFP4000

During the development and evaluation of N3IC-NFP we run a number of benchmarks to understand the nuances of the NFP4000 architecture, and to tune our implementation. In all the tests, the system is always loaded with 40Gb/s@256B. Next we report a subset of those results.

#### B.1.1 Benchmarks for small NNs (data parallel)

To better characterize the data parallel performance, we measured the packet forwarding capabilities and analyzed flow/s the system achieves when using different flow arrival rates, in the orders of 10k, 100k and 1M new flows per second, and executing a NN inference for each new received flow. This should cover a wide spectrum of possible workloads [48]. Furthermore, we changed the number of NFP’s threads used by N3IC, and measured the NN execution time for different configurations. Figure 21 shows that N3IC matches the baseline performance by using 120 threads, i.e., 30 more threads than baseline, when handling 200k new flows per second and performing as many NN executions per second. This confirms that the computation of the per-flow statistics is a memory-bound operation for the NFP4000, which therefore has idle computing resources that could be leveraged for NN execution. When further increasing the threads to 240 and 480, N3IC can come close to, or match, the baseline performance even while processing about 2M NN executions per second. This confirms that the computation of the per-flow statistics is a memory-bound operation for the NFP4000, which therefore has idle computing resources that could be leveraged for NN execution. When further increasing the threads to 240 and 480, N3IC can come close to, or match, the baseline performance even while processing about 2M NN executions per second, as mentioned in [48]. To check the maximum achievable throughput under heavy load, we configured the NFP to process the traffic classification’s NN for each received packet, i.e., a stress test. In this case, Figure 21 shows N3IC can forward 7.1Mpps, i.e., line rate of 40 Gb/s for packet sizes bigger than 512B, while running a NN for each packet using the 480 threads configuration.

#### NN Size (Figure 22)

In data parallel mode we placed a copy of the BNN’s weights in each of the available CLS memories, since each island is provided with a dedicated one. The weights are accessed in read-only mode and
Figure 21: N3IC-NFP data parallel forwarding performance (y axis), when processing 40Gb/s@256B, as a function of the number of flows to analyze (x axis). X axis in log scale.

Figure 22: N3IC-NFP data parallel maximum BNN execution throughput (y axis) as a function of the BNN size (x axis). The throughput scales linearly with the BNN size.

Figure 23: N3IC-NFP data parallel maximum BNN execution throughput (y axis) as a function of the number of used threads (x axis), and for different memories. Y axis in log scale.

Shared among all the island’s threads. We can fit, at most, about 32k weights in CLS. Figure 22 shows how varying the size of an FC scales linearly the N3IC-NFP maximum throughput. The tested layer has 256 inputs, and we run it with a different number of neurons: 32 (8.1k weights), 64 (16.3k weights), 128 (32.7k weights).

Memory benchmarks. To understand the impact of the memory selected to store NNs’ weights, we re-run the stress test using the IMEM and EMEM in place of the CLS, and measure both throughput and NN execution latency. Figure 23 shows that throughput lowers to 1.4Mpps in both cases. Likewise, Figure 24 shows that the NN execution latency is significantly worse. In particular, the 95-th percentile of the latency when using the CLS is 42µs, instead, the use of IMEM and EMEM incurs a much larger...
variation, with a 95-th percentile inference time of 352µs and 230µs, respectively. This latency variability is due to the need to share the NFP4000’s data buses among multiple threads. Interestingly, although generally faster, there are cases in which using the IMEM is slower than using the EMEM. We believe this is an artefact of the NFP’s memory access arbiter.

B.1.2 Benchmarks for big NNs (model parallel)

We measured the impact of using a different number of threads and different FC sizes when running N3IC-NFP in model parallel mode. We compared the results to those achieved by bnn-exec when running on a single core for latency measurements, and on 4 cores for throughput ones. We defined the maximum batch size bnn-exec can use setting a maximum of 7ms for the processing latency [30]. The 7ms execution latency constraint allows bnn-exec to run with a batch size of 64, 32, 16 and 8 for the 2k, 4k, 8k and 16k neurons layers, respectively. The layer has 4096 inputs.

**Latency (Figure 25).** For layers between 2k and 16k neurons (8M to 67M weights), N3IC-NFP achieves a processing latency which is 4 times higher than bnn-exec’s one, varying between 400µs and 2700µs. Considering that the Haswell CPU has a clock frequency more than 4 times higher than NFP’s 800MHz, i.e., each operation is effectively executed in less than a fourth of the time, this shows that the NFP is slightly more efficient than the Haswell in performing the FC layer operations.

**Throughput (Figure 26).** N3IC-NFP, though unable to perform batching, and using only a subset of the NFP resources, can still provide 4-5% of the bnn-exec throughput running on a much more powerful Intel CPU. Here, take into account that the NFP provides only 3MB of SRAM that have to be shared with with packet processing function, while the CPU’s over 10MB of L3 cache are dedicated to bnn-exec processing. Furthermore, unlike the CPU (4 cores) that is dedicated to the processing of NNs, N3IC-NFP performs such processing while forwarding 18.1Mpps.
B.2 NetFPGA

We designed the NN Executor module in HDL. This allows us to provide predictable performance, i.e., throughput and latency, when performing NN inference.

NN Size (Figure 27 and Figure 28). Figure 27 shows how varying the size of an FC scales linearly the N3IC-FPGA maximum throughput. The tested layer has 256 inputs, and we run it with a different number of neurons: 32 (8.1k weights), 64 (16.3k weights), 128 (32.7k weights). Increasing the number of NN Executor modules linearly scales the throughput. Since each module is dedicated to the execution of a NN, adding more modules does not impact the latency of execution, which is only affected by the size of the processed network (cf. Figure 28).

Resources scaling (Figure 29, Figure 30, and Figure 31). N3IC-FPGA performance can be increased by deploying multiple NN Executor in parallel. Since the logic to manage multiple modules is negligible, also the required FPGA resources scale linearly. Figure 29 shows the maximum throughput performance when running the anomaly detection NN (cf. §5), during the stress test explained in §6. Each NN Executor module increases by about 1.8M inferences per second the obtained performance. Figure 30 and Figure 31 show that the LUTs and BRAMs resources also scale linearly with the number of NN Executors. Here, it is worth noticing that the use of BRAMs can be considerably optimized. In the current setting, each NN Executor has a dedicated CAM element to store the NN weights. However, weights are read-only, thus, sharing a CAM module across multiple NN Executors can be achieved with relatively little effort. We did not provide such optimizations, since a single NN Executor could already achieve the performance goals we set for N3IC-FPGA.

C Use cases details

We present three use cases to demonstrate the versatility of N3IC. The results are summarized in Table 5.

C.1 Classification and Anomaly Detection

We consider two typical networking applications: traffic classification and anomaly detection. The former aims at training a NN for application identification and requires the system to be able to extract per packet features. The latter focuses on discovering suspicious data flows by analyzing flow level features in the network traffic.

Datasets. For the traffic classification use case, we used UPC-AAU dataset [7] of more than 750K flows, including per packet traffic traces from 76 commonly used applications and services, which account for 55GB of packet-level data. For the anomaly detection use case we used the the UNSW-NB15 dataset [52], which provides over 170K network flows labeled in two main categories, i.e., good, bad, and their flow-level statistics. In our experiments, we used only the 16 most important features by computing the chi-squared value between each feature and the class label [17]. Furthermore, to train a binary classifier, we only use features that can be computed in the NIC hardware. Hence, we ignored features related to the packets’ content, which we assumed encrypted. For the UPC-AAU dataset, we trained a binary classifier to detect encrypted BitTorrent flows.

MLP Classifier. For the traffic classification use case, we first trained a regular MLP to classify the traffic in 10 classes provided by the UPC-AAU dataset (see Table 4), achieving 69.4% accuracy. When training a similar binarized MLP model, we achieve 59.1% accuracy. Figure 32 shows the classification confusion matrix for the binarized MLP. As we can see, there are some classes, such as code 1, 2, 6, and 8 in Table 4 which cannot be easily distinguished from other classes. Furthermore, we could achieve this classification accuracy only using a larger binarized MLP with 256 neurons in each of the two hidden layers. Using the binarized MLP presented in §5 only achieves about 14% accuracy. To address the issue, we transformed the classification problem in a binary classification. That is, we trained the MLP to classify only between BitTorrent traffic and non-BitTorrent traffic. In such a setting we achieved 96.2% accuracy for the regular MLP and 88.6% for a binarized MLP with only 32, 16, 2

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14https://cba.upc.edu/monitoring/traffic-classification
15https://www.unsw.adfa.edu.au/unsw-canberra-cyber/cybersecurity/ADFA-NB15-Datasets/
16Although in UPC-AAU dataset there 76 different class, there are not enough data samples for each class to train a reliable multiclass classifier on it. For this reason, we choose the 10 biggest classes in terms of number of available samples.
Table 4: Traffic classes of UPC-AAU with at least 10000 samples.

| Code | Name                        | Size  |
|------|-----------------------------|-------|
| 0    | bittorrent-all-encrypted    | 25000 |
| 1    | bittorrent-outgoing-non-encrypted | 25000 |
| 2    | emule-outgoing-non-obfuscated | 10960 |
| 3    | pandem Mediabooster         | 12070 |
| 4    | rdp                         | 25000 |
| 5    | web-browser                 | 24914 |
| 6    | dns                         | 10761 |
| 7    | new-samba-session-service   | 25000 |
| 8    | ntp                         | 17834 |
| 9    | ssh                         | 25000 |

Table 5: Memory requirements and accuracies of the NNs used by the presented use cases.

| DATA | NN size | MEMORY | ACCURACY |
|------|---------|--------|----------|
|      | MLP | BIN | MLP | BIN |
| UNSW | 32,16,2 | 35KB | 1.1KB | 90.3% | 85.3% |
| UPC  | 32,16,2 | 35KB | 1.1KB | 96.2% | 88.6% |
| NS3  | 32,16,2 | 21.6KB | 676B | 92.0% | 90.0% |
| NS3  | 64,32,2 | 47.2KB | 1.5KB | 94.0% | 90.0% |
| NS3  | 128,64,2 | 110.8KB | 3.4KB | 94.0% | 92.0% |

Figure 32: Confusion matrix for multiclass classification on UPC-AAU dataset. Numbers show the accuracy (%). Rows and columns shows the class code in Table 4.

We configured an MLP with 3 FCs of 32, 16, 1 neurons for the anomaly detection use case as well. For both use cases, since each selected feature’s numeric value falls in the range [0, 65k], we represented them using 16b for each, and provide each bit as separated input to the MLP. With this configuration, the MLP has a total of 8.7k weights, and a memory requirement of 35KB, assuming 4B to represent each weight. We then performed training using a typical state-of-the-art approach, which employs a back-propagation algorithm with Adam optimizer, Dropout on the output of each hidden layer with probability 0.25, and binary cross-entropy as loss function. The trained classifier achieves 90.3% accuracy.

Binarized MLP. We then designed a binarized MLP to process the same set of features. The binarized MLP has 32, 16, 2 neurons and a total of 8.7k weights. Being binary weights, the overall required memory is only 1KB. Binarization mainly consists in applying a training technique that ensures that the weights converge to values included in the range [-1, 1] and normally distributed around the 0. In particular, we apply the binarization technique from Courbariaux and Bengio [10], and again train the network using back-propagation, Dropout with probability 0.25, Adam optimizer and a squared hinge loss function. The trained MLP’s weights obtained after training are still real numbers, thus, an additional final step is required to obtain the binarized weights. This step is a simple application of a step function to the weights, which are set to 0 if their value is lower than 0, or to 1 otherwise. After this, the binarized MLP achieves a 85.3% and 88.6% accuracy on the test set for UNSW-NB15 and UPC-AAU, respectively. We observe that the BNN provides only 5 and 8 percentage points lower accuracy than the non-binarized version.
C.2 Network Tomography

In this use case, we run SIMON [18], a network tomography application which infers congestion points and queue sizes in a datacenter network starting from host-to-host network paths’ delays. All the end-hosts periodically exchange probe packets among them and send the measured delays to a centralized node which is then responsible for running the reconstruction engine and whose algorithm has been approximated using a Neural Network. We implemented a modified version of SIMON where we are interested in quickly detecting the congestion point without estimating the exact size of the queues. Rather than running a single NN in the centralized node, a set of NICs is in charge of computing the congestion status of the queues.

Dataset. We simulated a small CLOS-like Fat Tree datacenter network in ns3 [74]. The network, reported in Fig. 33 includes 10 switches and 32 hosts organized in two pods (4 ToR switches, 4 aggregation switches and 2 core switches). The datacenter operates under an incast traffic load as described in [18]. In addition to the traffic, all the servers (except the first one) periodically send a probe packet (once every 10ms) towards the first server to measure the network paths delays. From any server there are up to 8 distinct paths towards the first server, traversing in total 17 distinct output queues (reported as green dots in Fig. 33). Our task is to train multiple NNs, one for each queue, each one in charge of detecting the queue congestion status.

We selected a subset of 19 out of 31 probes in order to keep 1 probe per distinct path. Our dataset consists of 30k samples, one per each 10ms interval, with 19 features (path delays, in ms) and 17 corresponding outputs (queue sizes, in packets). We considered 17 independent binary classification problems where the output class is 1 if in a given 10ms interval the corresponding queue is above a configurable threshold, 0 otherwise.

MLP Classifier. We first trained a regular MLP, with the same hyperparameters used in the previous use cases, with three different architectures (32x16x1, 64x32x1 and 128x64x1). The 19 inputs of the MLP are represented using 8 bits and, as in the previous use cases, we provide each bit as separated input to the MLP. Table 5 reports the memory requirements for the different NN architectures. The resulting median accuracies range from 92% to 94% for an increasing NN size.

Binarized MLP. We then designed a binarized MLP to process the same set of features with three different architectures (32x16x2, 64x32x2 and 128x64x2), all with 19 inputs and two output neurons. The drop in the median accuracy when moving from a full precision NN to a binarized NN ranges from 2% to 4%. Fig. 34 reports more in detail the distribution of the median accuracies for different NN sizes.