Bio-mimetic Synaptic Plasticity and Learning in a sub-500mV Cu/SiO$_2$/W Memristor

S. R. Nandakumar$^1$ and Bipin Rajendran$^{2,3}$

$^1$New Jersey Institute of Technology, Newark, NJ 07102, USA
$^2$King’s College London, Strand, London WC2R 2LS, United Kingdom

(Dated: 28 January 2020)

The computational efficiency of the human brain is believed to stem from the parallel information processing capability of neurons with integrated storage in synaptic interconnections programmed by local spike triggered learning rules such as spike timing dependent plasticity (STDP). The extremely low operating voltages (approximately 100mV) used to trigger neuronal signaling and synaptic adaptation is believed to be a critical reason for the brain’s power efficiency. We demonstrate the feasibility of spike triggered STDP behavior in a two-terminal Cu/SiO$_2$/W memristive device capable of operating below 500mV. We analyze the state-dependent nature of conductance updates in the device to develop a phenomenological model. Using the model, we evaluate the potential of such devices to generate precise spike times under supervised learning conditions and classify handwritten digits from the MNIST dataset in an unsupervised learning setting. The results form a promising step towards creating a low power synaptic device capable of on-chip learning.

I. INTRODUCTION

Today’s state-of-the-art computing platforms are capable of performing quadrillions of precise logical operations in a second, albeit consuming millions of Watts. However, they still lag behind the capabilities and efficiencies of the human brain, especially for unstructured data analytics and decision-making tasks. The reason behind the inefficiency of conventional machines for such applications is the underlying von Neumann architecture, requiring constant shuttling of data between the physically separated processor and memory units. In contrast, the human brain is a massively parallel information processing system with approximately 100 billion neurons that interact with each other by transmitting electrical signals through 1000 trillion neuronal junctions or synapses. The parallel operation of networks in the brain which integrates memory locally in its synaptic junctions and their plastic nature enable adaptation and learning depending on neuronal spike based information processing activities. The von Neumann machines we use today are incapable of such learning and adaptation and executes its tasks based on pre-programmed algorithms in a sequential manner. This stark difference in the two computational paradigms calls for architectural innovations that could aid the development of intelligent computing platforms that could learn in real-time and in the field.

The neurons in the brain encode information by issuing voltage signals called action potentials or spikes whose amplitude is around 100mV above the resting potential. These spikes are then transmitted in a parallel fashion along the axons to thousands of other neurons through synaptic junctions. The post-synaptic neurons issue further spikes based on the integration of weighted sum of its inputs. Coincident spiking activity of the pre- and post-synaptic neurons alters the effective conductivity of the synapses due to the insertion or internalization of receptor molecules on the synaptic terminals. Such unsupervised local training rules are believed to be integral to the energy and computational efficiency of the brain. An example of a spike timing dependent plasticity (STDP) rule observed in a rat hippocampal neuron is shown in Fig. 1, where a post-neuron spike immediately following a pre-neuron spike (within 40–80 ms) leads to an increase in conductance (potentiation) and a pre-neuron spike following a post-neuron spike leads to a decrease in conductance (depression).

Mimicking human brain’s architecture and computational primitives to build intelligent information processing systems is the key goal of neuromorphic engineering research activities worldwide. While there have been several demonstrations of neuromorphic computational platforms using standard complementary metal-oxide semiconductor (CMOS) technology and demonstrations of nanoscale devices to mimic neuronal and synaptic dynamics, none of these have achieved the target energy efficiency specifications necessary to build systems that can learn in real-time and in the field.

In order to build systems that mimic the massive parallelism and local learning aspects of the human brain, compact electronic devices that implement the dynamics of neurons and synapses are required. 3D integration of crossbar circuits with synaptic
FIG. 1. Spike timing dependent plasticity (a) Neurons connect and exchange information via junctions between axons and dendrites, called synapses. (b) Synaptic conductance modification observed in a rat hippocampal neuron [10], an example of spike timing dependent plasticity (STDP) observed in biology. Positive and negative changes in excitatory post-synaptic current (EPSC) indicate synaptic potentiation and depression, respectively. (c) Bio-inspired programming waveforms used in the experiment to demonstrate STDP in a memristive device.

devices at its junctions and neuronal devices at the periphery is an efficient architectural paradigm to achieve the parallel connectivity of the human brain, mitigating the memory-processor bottleneck of conventional von Neumann systems. Memristive devices that exhibit conductivity modulation based on past programming history are excellent candidates to realize synaptic memory [32,33]. There have been numerous synaptic device demonstrations in oxides [34–36] and chalcogenides [26,37] which show analog conductivity modulation based on non-volatile rearrangements of atomic configurations within the active volume of the device. However, these devices present many challenges in terms of programming stochasticity and asymmetry, granularity, reliability, and the energy required for implementing conductivity modulation, and no single device has so far achieved all the target specifications. For example, Ta/TaO\textsubscript{x}/TiO\textsubscript{2}/Ti device has demonstrated femto-Joule level programming energies, but requires programming voltages above 18 V [38]. Similarly, chalcogenide-based phase change memory devices have pico-Joule level programming energies, however, the high programming current limits parallel programmability and require access transistors at every cross-point in an array [26]. Hence, physics-driven device engineering to improve various synaptic device requirements and finding the right trade-offs for the targeted applications are necessary.

Resistive random access memories (RRAMs) are non-volatile memory devices with a metal-insulator-metal structure capable of realizing synaptic networks of high integration density. These devices store information in their resistance states which could be modulated by external programming pulses. The resistance transition in these devices typically involves a redox reaction where ionized atoms migrate in the direction of the field and get reduced at one of the electrodes. Depending on the nature of the ionic species involved in the atomic rearrangement, these devices are classified either as Oxide-RAMs (OxRAMs) or conductance bridge-RAMs (CBRAMs). The conductance modulation in OxRAMs is due to the movement of Oxygen atoms or their vacancies in the dielectric, while that in CBRAMs is due to the movement of metallic ions (e.g., Cu, Ag) from one of the electrodes. Due to the relatively higher mobility of the metallic ions in dielectrics such as SiO\textsubscript{2} and GeS\textsubscript{2}, CBRAMs tend to have smaller operating voltages compared to OxRAMs. The non-uniformities or the defects in the thin dielectric lead to localization of the applied programming field and hence the atomic rearrangement often leads to the formation of low resistance nano-filamentary structures. Further, the relatively higher resistivity contrast between the dielectric and the filament material in CBRAM accentuates the electric field in the filament gap which accelerates the filament growth/decay and conductance switching. While the low operating voltages of the CBRAM is advantageous, a more gradual conductance change is desirable for synaptic implementation. Doping the dielectric with the active electrode material (e.g., Cu) could reduce the resistivity contrast between the dielectric and filament material and could improve the probability of a non-filamentary conductance transition.
Doping the dielectric by annealing has been demonstrated to achieve gradual conductance change in Cu/SiO$_2$/W based devices. Also, the feasibility of using CBRAM devices for STDP has been shown by model simulations.

In this work, we experimentally demonstrate STDP in a Cu/SiO$_2$/W based memristor. Using a computationally simpler phenomenological model of the device that captures all its salient operating characteristics, we demonstrate the feasibility of using these devices in both supervised and unsupervised learning scenarios. We also evaluate the learning performance of these networks with non-ideal device characteristics and estimate the synaptic energy consumption under chosen programming scheme.

II. RESULTS

A. Synaptic device based on Cu/SiO$_2$/W memristor

Our device has a 10nm SiO$_2$ dielectric layer sputter deposited between a Cu top electrode (TE) and a W bottom electrode (BE). The device is fabricated as a cross-point structure using a two mask process. The SiO$_2$ dielectric and Cu electrode are deposited without breaking the vacuum and are patterned together. The device undergoes a final 400°C, 5min anneal during which Cu species diffuses into the dielectric (see appendix).

The device exhibits typical memristive pinched hysteresis I-V with switching threshold below 500mV (Fig 2a). Bipolar voltage sweeps of approximately 2V/s ramp rate are applied to the Cu electrode while the W is kept at ground potential. A sufficiently large positive voltage across the device results in the ionization of relatively active Cu atoms. The migration of the resulting ions under the electric field and reduction at the bottom electrode eventually leads to the formation of metallic nano-filament paths connecting the top and bottom electrode causing the device to switch from a high resistance state (HRS) to a low resistance state (LRS), known as SET transition. Previously, we observed conductance quantization as half-integer multiples of quantum conductance $G_0 = 2e^2/h$ in its LRS state during current sweep measurements confirming the presence of nano-filaments. The actual conductance evolution trajectory will depend on factors such as magnitude and duration of programming pulses, the thickness of the dielectric layer, distribution of migrating ionic species and imperfections in the dielectric. Depending on the maximum amplitude of the voltage sweep applied to the device, we observed abrupt memory switching (corresponding to a metal filament completely bridging the top and bottom electrodes - blue curve in Fig[2]a) as well as a gradual memristive switching where the maximum device conductance is below the unit of quantum conductance $G_0$, enabling us to realize intermediate conductance states that could be used for synaptic memory (orange curve in Fig[2]a). A negative voltage of sufficient magnitude reverses the ionic migration direction, reducing the extent of the metallic filament and bringing the device back to the HRS states (RESET transition). This bipolar switching behavior indicates that the conductance transitions in the device are due to the field-driven motion of charged ions through the dielectric.

B. Demonstration of spike timing dependent plasticity

Our demonstration assumes that the device is connected between two spiking neurons. To emulate the spike timing dependent plasticity in our devices, the programming waveforms are designed as shown in Fig[1]. The spikes from the pre- and post-synaptic neurons are converted to waveforms ($V_{\text{pre}}$ and $V_{\text{post}}$) mimicking the action potential in the biological neurons. These waveforms are applied at the instants of spike activity of the two neurons to the respective terminals of the synaptic device. The waveforms, $V_{\text{pre}}$ and $V_{\text{post}}$, are constructed using two decaying exponentials (equation [1]) to capture the depolarization-repolarization-hyperpolarization cycles in the biological action potential waveforms.

\[
V_{\text{pre}}(t) = A_1 e^{-t/\tau_m} u(t) - A_2 e^{-(t-3\tau_m)/\tau_u} u(t-3\tau_m) \\
V_{\text{post}}(t) = A_2 e^{-t/\tau_m} u(t) - A_1 e^{-(t-3\tau_m)/\tau_u} u(t-3\tau_m)
\]

where $A_1 = 0.1V$, $A_2 = 0.25V$, $\tau_m = 3ms$, $\tau_u = 30ms$ and $u(t)$ is the Heaviside step function. The amplitudes of $V_{\text{pre}}$ and $V_{\text{post}}$ are chosen such that they are below the minimum SET and RESET voltages of the device when there is no or very little overlap between the waveforms. However, when the spikes are closer, the magnitude of the instantaneous voltage across the device increases, resulting in non-volatile conductivity modulation. In our experiment, the time constants of the programming waveforms are chosen to have non-zero overlap between the pre- and post-synaptic neuron spike waves for a desired duration for this STDP window. Our programming scheme assumes that the $V_{\text{post}}$ signal is sent in the backward direction from the post-synaptic neuron when it spikes. If spikes from both the pre- and post-synaptic neurons occur close in time, there will be significant overlap in the voltage waveforms generated across the device. Depending on the direction and magnitude of the field across the device, the conductance of the device could increase or decrease.
FIG. 2. STDP in memristor (a) Memory switching behavior of the Cu/SiO$_2$/W cross-point device for two voltage sweeps with maximum amplitude of 350 mV and 450 mV. The current corresponding to a conductance of $G_0(=2e^2/h)$ is marked using a dashed line. The conductance response above the $G_0$ level (blue curve) indicates at least one filamentary path connecting the top and bottom electrode, while the orange curve shows partial conductance switching in the sub-quantization regime. The 3D device structure is shown in the inset. (b) STDP programming and measurement set-up (c) Example STDP programming waveforms applied (top) and the measured device conductance evolution (bottom) where $\Delta t = 5\mathrm{ms}$ results in a synaptic potentiation and $\Delta t = -5\mathrm{ms}$ results in a synaptic depression. (d) STDP response of the device determined as the average conductance change (normalized) versus the spike time difference based on 400 measurements. $\Delta G_{\text{norm}} = (G_f - G_i)/\text{min}(G_i, G_f)$ (e) Evolution of the device conductance during the STDP measurement tracks the overall causal/anti-causal signal correlation. The orange curve is a cumulative sum of the sign of the $\Delta t$ across the sequence of measurements. (f) Energy consumption per spike pair as a function of $\Delta t$ for the chosen programming waveforms and the conductance range observed from the device.

For the experimental demonstration, we assume that the Cu electrode is connected to the post-synaptic neuron and W to the pre-synaptic neuron. However, instead of applying the $V_{\text{pre}}$ and $V_{\text{post}}$ to the respective terminals we compute the difference waveform $V_{\text{post}} - V_{\text{pre}}$ as a function of time and is applied to the Cu terminal with the W electrode at ground (Fig 2b). Such waveforms were created using an arbitrary waveform generator for different spike time differences. Example waveforms applied to the device for a positive and negative time difference of 5 ms and the corresponding device conductance evolutions are plotted in Fig 2c. Each programming waveform is appended with an initial and final non-disruptive read pulse of 50 mV to measure the device conductance. As indicated in the figure, the $\Delta t = 5\text{ ms}$ signal leads to potentiation and $\Delta t = -5\text{ ms}$ leads to depression in device conductance. The average conductance change for the spike time differences in an interval of $[-40\text{ ms}, +40\text{ ms}]$ is plotted in Fig 2d based on 400 randomly chosen $\Delta ts$. The average $\Delta G_{\text{norm}} = (G_f - G_i)/\text{min}(G_i, G_f)$ versus $\Delta t$, where $G_i$ is the initial and $G_f$ is the final conductance for a spike time difference of $\Delta t$, is similar to the STDP response from a biological synapse shown in Fig 1b. In Fig 2e we show the conductance evolution of the device during the STDP measurement. We observed that the device always stayed below the quantized conductance level of $G_0(=2e^2/h)$ with its minimum conductance at 0.016$G_0$. The filamentary paths often formed in the conductance-bridge resistive memory devices act as nanoscale electron channels and result in conductance levels which are integer multiples of $G_0$. The sub-quantized levels in our device are indicative of non-filamentary atomic rearrangement based conductance modulation. Further, the superimposed orange curve, which is a cumulative representation of the sign of the applied $\Delta ts$ during each spike-time difference based programming event follows the same trend as the device conductance evolution. Thus, the device plasticity has successfully captured the overall causal-anti-causal spike pair relations. In Fig 2f we plot the distribution of energy consumed in the synaptic device during the propagation of $V_{\text{pre}}$ and $V_{\text{post}}$ spike waveforms as a function of the time difference between them. The average energy consumed per spike is 5 nJ based on the spike triggered waveforms and the average device conductance range; the energy consumed slightly increases
or decreases depending on whether the programming event leads to potentiation or depression of the synapse.

C. Phenomenological model for state-dependent conductance update

A careful analysis of the device response reveals the state dependency of the conductance change as a function of the timing difference of the applied waveforms. We study the device response for three regimes, demarcated in units of quantum conductance $G_0$: (a) when $G_i < 0.05 G_0$, (b) when $0.05 G_0 < G_i < 0.16 G_0$, (c) when $G_i > 0.16 G_0$. From the average $\Delta G_{norm}$ vs $\Delta t$ plotted for different ranges of initial conductance, we observe that when the initial conductance is in the intermediate range, conductance change in the direction of potentiation and depression is in the same range for the same spike time difference, while potentiation is pronounced and depression is weak in the low initial conductance regime (Fig.3a,b). Albeit noisy, a similar trend was also visible in high initial conductance regime, where device shows more tendency for conductance depression than potentiation. This behavior indicates a reduction in the incremental conductance change and a conductance saturation as the device reaches closer to its upper and lower conductance limits.

![Figure 3](image_url)

**FIG. 3. Device state-dependency and phenomenological model** (a) Average $\Delta G_{norm}$ defined as $(G_f - G_i)/\min(G_i, G_f)$ response from the device measurement when the initial conductance is below 0.05 $G_0$ with an average of 0.03 $G_0$ and when (b) it is in the range between 0.05 $G_0$ and 0.16 $G_0$ with an average of 0.1 $G_0$. (c) The response of the phenomenological model, when programmed with a sequence of randomly chosen $\Delta t$s. (d) The device conductance after the application of the pulse $(G_f)$, calculated from the phenomenological model is well correlated with the experimental values ($R^2 \sim 0.56$), for the same initial conductance values and programming $\Delta t$s as in the experiment over a dynamic range of two orders of magnitude.

To study how such device characteristics will be effective in emulating synapses in neural network implementations, we developed a computationally simpler phenomenological model that predicts the next state of the device, $G_f$, given the current state, $G_i$, and spike pair time-difference, $\Delta t$. Our model essentially captures these state dependent conductivity modulation characteristics by modelling the normalized change in conductivity $\Delta G_{norm}$ as:

When $\Delta t > 0$,

$$\Delta G_{norm} = A \exp \left( \frac{-\Delta t}{\alpha_{ap} + g\beta_{ap}} \right) - A \exp \left( \frac{-\Delta t}{\alpha_{ap} + g\beta_{ap}} \right)$$

and when $\Delta t \leq 0$,

$$\Delta G_{norm} = -A \exp \left( \frac{\Delta t}{\alpha_{ap} + g\beta_{ap}} \right) + A \exp \left( \frac{\Delta t}{\alpha_{ap} + g\beta_{ap}} \right)$$

$A = 9, g = \log_{10}(G_i/G_0)$, and other parameters are listed in Table II. Further, the model is limited to operate within a conductance range of $G_{min} = 0.016 G_0$ and $G_{max} = 0.5 G_0$. The equations (2,3) are formed as the difference of two decaying exponentials.
with different time constants (see appendix). The time constants are functions of the device conductance and converges to the same value at the boundary points such that the conductance change gradually becomes zero. Such state dependent behavior is akin to the saturating conductance responses observed in many of the gradual conductance and STDP demonstrations in the memristive devices [22, 23, 40, 43].

| Symbol | Value | Symbol | Value |
|--------|-------|--------|-------|
| $\alpha_{ap}$ | 5.2 ms | $\beta_{ap}$ | −3.8 ms |
| $\alpha_{bp}$ | 6.9 ms | $\beta_{bp}$ | 1.9 ms |
| $\alpha_{an}$ | 9.1 ms | $\beta_{an}$ | −1.9 ms |
| $\alpha_{bn}$ | 2.3 ms | $\beta_{bn}$ | −5.7 ms |

The STDP response from the phenomenological model is shown in Fig. 3c, where the model conductance is initialized to 1 $\mu$s and is programmed with a sequence of random $\Delta t$s. To compare the model and device response, the model is initialized with the exact device conductance measured before each $\Delta t$ from the experiment and the correlation between the model and the device conductance responses after each $\Delta t$ based STDP programming is plotted in Fig. 3d. The $R^2$ estimation between these experimental and model conductance values measured over two orders of magnitude is 0.56.

### D. Supervised learning emulation

Next, we discuss how this device could be used in an exemplary spiking neural network (SNN) for implementing event-triggered learning. An STDP derived supervised learning algorithm, similar to the ReSuME [44], is used to train a network with 1000 inputs neurons and one leaky-integrate and fire (LIF) output neuron (Fig. 4a) (see appendix for details on SNN simulation). The task is to determine the weights of the 1000 synapses of the output neuron such that it creates spikes at the desired instants within $\pm 10$ ms. In our simulation shown in Fig. 4c,d, the network generates all the spikes at the desired times within $\pm 10$ ms in 9 epochs. The weight evolution generated by our model for a few synapses during the training is shown in Fig. 4e.

Such algorithms are at the heart of supervised learning platforms in spike domain. Once input and output data are translated to spike domain, it can be used to efficiently train networks for different tasks, provided the synaptic realization has sufficient analog programmability. The $N \times 1$ network could be extended for more complex problems. For example, we realize a $900 \times 900$ SNN whose synapses are represented by our phenomenological model (see appendix). The network acts as a sequence predictor for English letters $N \rightarrow J \rightarrow I \rightarrow T$ such that when the input layer is presented with one of the letters, the network creates the image of the next letter in the sequence at the output layer. The pixel intensities of $30 \times 30$ grayscale images are used as rate constants for a Poisson process to generate the corresponding input and desired output spike streams. The network synapses are trained using the same supervised STDP rule as before. The input and the resulting output spike rates from the network after 40 epochs of training are mapped to the input and predicted output image as shown in Fig. 4f. The conductance distributions of the synapses connected to three output neurons (akin to a receptive field) are shown in Fig. 4g. The relative distribution of the conductance illustrates the features the network have learned, enabling it to efficiently map the input spike streams to the corresponding output spike streams, in an event-triggered manner. Note that the first set of synapses are connected to an output neuron responding to both letters N and J, illustrating the complex information representation capacity of synapses obeying the plasticity rules.
FIG. 4. Supervised training of SNN (a) An exemplary spiking neural network with $N$ input neurons connected to a single output neuron. The training task is to discover the synaptic weights such that the output spike response, $S_d(t)$, matches the desired response, $S_o(t)$, for a specified input spike excitation, $S_i(t)$. (b) Training rule: the synapse is potentiated or depressed based on the time difference of desired or observed spikes respectively from the efferent spike using the STDP model. (c) A raster plot of the spike streams from each input neuron in a $1000 \times 1$ SNN is shown. (d) The desired and observed spike trains over the training epochs (top) and the final membrane potential (bottom) from the output neuron as a function of time. (e) Device conductance evolution for four exemplary synapses during the training of the $1000 \times 1$ neural network. (f) Input (top) and observed output (bottom) neuron spike rate in an SNN trained for sequence prediction. (g) Relative conductance distribution of synaptic device models connected to three output neurons showing the features learned after training. The first set of synapses is connected to a neuron responding to letters N and J. The second set of synapses is connected to an output neuron responding only to letter N.

E. Unsupervised learning emulation

We now evaluate the unsupervised learning capability of device based on the observed STDP characteristics on the commonly used benchmark task of classifying handwritten digits from the MNIST dataset. We study two fully connected SNNs - both the networks receives 784 inputs (corresponding to $28 \times 28$ pixels in the image); the first network has 10 LIF output neurons, while the second has 30 LIF output neurons and in both the SNNs a winner-take-all dynamic is implemented between the output neurons. The unsupervised classification performance has been shown to improve by increasing the number of output neurons.\textsuperscript{45,46} The $28 \times 28$ pixel intensities of the training images were binarized and presented as spike streams to the input of the SNNs. Each image is applied for 200ms. \textit{Off} pixel values do not receive any spikes and \textit{on} pixel values receive a spike at 50 ms. Corresponding to each spike, a voltage signal $-V_{pre}(t)$ is applied to the synapses. The LIF neurons integrate the currents to generate output spikes and the synaptic conductance values are modulated based on the STDP model. The winner-take-all dynamics in the output layer resets the integrated membrane potential of all the output neurons when any one of the neuron issues a spike, preventing them from spiking for the next 3ms. For each output neuron spike, the synapses with a pre-neuron spike within a 40ms duration are potentiated based on the spike time difference and those without a spike is depressed assuming a spike time difference of $-60ms$. Further, we maintained homeostasis between the output neurons by adjusting the threshold voltage of the LIF neurons every 100 images such that all the output neurons have a similar spike rate on average.\textsuperscript{45}

We emulated the synapses with 1, 5, and 10 devices as a method to improve the conductance change granularity.\textsuperscript{47} A reference corresponding to the minimum conductance level was assumed per synapse such that synaptic conductance is $n(G - G_{min})$ where $n = 1, 5,$ or 10. To implement pulse overlapping STDP programming in a multi-memristive synapse, as envisioned in our conductance update scheme, the output neurons integrate current from all the devices in a synapse, however, the $V_{post}$ is sent back through only one of the devices chosen cyclically. In a crossbar array of memristive devices, this will involve a neuron integrating currents from multiple bit lines and sending a voltage through one of the bit lines when the neuron issues a spike. This permits uniformly distributing the programming events across multiple devices in a synapse.

Further, to evaluate the learning performance in the presence of programming noise, weight updates are assumed to be Gaussian random processes such that the mean of the normalized conductance updates ($\mu$) are determined using the equations\textsuperscript{2} and \textsuperscript{3} and standard deviations $\sigma$ are determined as a fraction (varied from 0 to 0.5) of $\mu$. Cumulative conductance evolution when the model was subjected to a sequence of programming pulse corresponding to spike pairs of $|\Delta t| = 5$ ms and $15$ ms is shown in Fig.5.

During each training epoch, the 60,000 images in the database were presented to the SNN and the weights were updated
using STDP for 10 epochs. The features learned by the weights connected to ten of the output neurons at the end of training is illustrated in Fig. 5c. We observe that the average features corresponding to different digits in the dataset are captured by the weights corresponding to different output neurons. The image labels were not used to determine the weight updates. At the end of every epoch, each output neuron is assigned a label corresponding to the digit for which it generated the maximum number of spikes during the presentation of the last 10,000 images from the training set. These labels are used to determine the prediction performance of the SNN on a test set of 10,000 images which were not shown during training (Fig. 5d). Under the memristive STDP response, we observe the classification performance to improve with the number of output neurons and with more number of devices per synapse. More remarkably, the test accuracies seem extremely tolerant to the programming noise. We achieved a maximum test set accuracy of 76.65% using 30 output neurons and 64.2% using 10 output neurons, both of which have 10 memristive devices per synapse and were programmed with $\frac{\sigma}{\mu} G_{\text{norm}} = 0.5$.

![FIG. 5. Unsupervised training of SNN](image)

(a) SNN used for the unsupervised training of handwritten images of digits. (b) The conductance evolution behavior of the phenomenological model used to emulate the SNN synapses. Model response when trained with a sequence of programming pulses corresponding to spike time intervals of 5 ms and 15 ms is are shown. (c) Features learned by the weights (normalized in the figure) corresponding to ten output neurons. (d) The classification performance of the SNN on 10,000 test images from the MNIST dataset. The results are average of three random simulations. The performance corresponding to different amount of programming noise added to the synapse model during training is shown.

### III. DISCUSSION

While there have been numerous demonstrations of CBRAM devices, including some based on the Cu/SiO$_2$/W material system, they were non-volatile memory devices with binary states and high on-off ratios ($\sim 10^3$). For neuromorphic systems that learn and adapt, it is desirable to have synaptic devices with incremental conductance changes. STDP behavior has also been demonstrated before in silicon based and oxide based memristive devices. However, these devices are characterized by either high operating voltages (typically $> 1$ V) or high operating current (0.1 mA to 10 mA) or low on-off ratio ($< 10$). Also, gradual conductance change by modulating the filament thickness in CBRAM is undesirable due to the high power con-
sumption associated with transport through metallic filaments. In contrast to the bipolar memristive device which implements STDP via overlapping programming pulses, unipolar devices such as phase-change memory suffer from the requirement for more complicated programming waveforms or circuits to implement STDP behavior. Hence, our demonstration of STDP in the sub-quantized (conductance $< 38.7 \mu S$) regime in a CMOS compatible memristor operating below 500 mV is a significant step towards realizing efficient neuromorphic learning systems.

The unsupervised learning performance using the state-dependent STDP model of our device on the standard MNIST benchmark dataset is at par with similar results in literature. For instance, approximately 60% accuracy in an SNN with 10 output neurons and 80% accuracy with 50 output neurons have been reported using synaptic models with tunable update granularity or learning rate. However, one of the major challenges in synaptic device based learning systems is the fixed range of realizable conductance changes. Multi-memristive synaptic architecture and mixed-precision architecture for supervised learning have been proposed to compensate the limited device granularity. Our demonstration of software-equivalent performance for unsupervised learning using realistic device STDP models, and its high tolerance to programming noise during training, is thus a promising step towards realizing functional learning machines using extremely scaled stochastic analog memory devices.

Such analog memory devices can be integrated in crossbar arrays to create high-density synaptic networks. While the sneak path issue is not so severe during parallel weighted summation of the neuronal inputs, the necessity to perform device programming without altering the neighboring devices may make a selector device at the cross point in series with the synaptic device desirable. The bipolar nature of the conductance update in the memristive device permits STDP programming by overlapping pulses from the bit lines and word lines of a crossbar array. Several programming methods have been proposed to achieve this, including the amplitude modulated rectangular pulse sequence schemes and those based on continuous analog waveforms, drawing different levels of biological inspiration. One of the initial approaches has been to convert the sign and magnitude of the spike-time difference into the polarity and width of a rectangular programming pulse. However, this necessitates a global circuit to generate the programming pulse with tunable width. In a true pulse overlapping programming scheme, the main challenge is the difference in the device switching time and the desired STDP window. The exponential programming waveforms we used for the CBRAM has been tuned such that sufficient electric field is set up across the device to initiate an ionic drift while keeping the duration and amplitude of the voltage sufficiently low to avoid rapid switching transitions to the extreme conductance levels. This is due to the fact that the ionic migration velocity in the device dielectric is exponentially dependent on the electric field and hence the actual conductance evolution characteristic is also dependent on the time-scale and shape of the programming waveform. If the STDP based learning is expected to detect correlation between events in real time encoded using sparse spikes, the STDP window, and correspondingly the input waveforms, need to last few tens of milliseconds, while the switching time of the CBRAM devices has been shown to vary from tens of microseconds to a few milliseconds. The long programming waveforms also lead to high energy consumption in the synapses. The average energy consumed per spike in the memristive device is approximately 5 nJ (which translate to an average of 10 nJ per spike pair used for STDP programming). Based on the average spike rate received by a synapse and the number of synapses in the SNN, the energy consumption in the synaptic network can be estimated. For example, approximately 0.1 mJ per epoch is required in the 1000 × 1 analog memory array for the supervised training and 0.16 mJ per image in a 784 × 10 analog memory array for the unsupervised learning. To realize large scale SNNs approaching the efficiency of the brain, further optimization of these synaptic devices is required, including operating in lower conductance ranges, switching in smaller time scales, and innovative STDP programming schemes that take into account the device programming characteristics and the application at hand.

STDP like local learning rules are key to the decentralized and parallel processing capabilities of the biological neural networks. Realization of biological plasticity mechanisms in nano-scale memristive devices when combined with their high integration density and scaling potential enables power efficient implementations of large-scale learning networks. While this proof-of-concept demonstration establishes the basic feasibility of our device for learning, there are challenges in terms of device reliability, and variability that warrants further research and optimization. For example, the Cu/SiO$_2$/W based devices we fabricated was responsive to approximately 1000 STDP measurements. The higher mobility of Cu in SiO$_2$, though useful for low voltage operation, might be the reason behind the rapid deterioration in endurance and retention performance. Further, the stochastic nature of atomic rearrangement upon programming results in stochasticity in the conductance modulations as well. Also, the device-to-device and cycle-to-cycle variation of the resistive memory devices could affect the array-level performance, though it is expected that some of these reliability issues could be mitigated by improved industrial fabrication processes. Furthermore, the targeted neuromorphic applications are more error tolerant as decisions are based on overall synaptic distributions rather than the absolute conductance levels of any particular device, making resistive memory based synapses more attractive for cognitive hardware.

**IV. CONCLUSION**

We have experimentally demonstrated STDP behavior, an unsupervised local neural learning strategy observed in nature, in a CMOS compatible 500mV memristive device using biomimetic programming waveforms. Using a phenomenological model of the observed characteristics, we have also demonstrated the suitability of the device to implement complex supervised
learning algorithms to generate spikes at precise time instances and to perform unsupervised learning on handwritten digits using MNIST dataset. The computationally simple non-linear model helps to study the suitability of such devices in different learning scenarios. With further optimizations, the cyclability and retention characteristics of the device can be improved, enabling the fabrication of crossbar array platforms for large spiking neural circuits for accelerating learning applications.

APPENDIX

A. Device fabrication

A p-type Si(100) wafer is used as the substrate for the device fabrication. A thin layer of SiO$_2$ was thermally grown over the wafer, which acts as an insulating layer to provide electrical isolation between the devices. A double layer photoresist (LOR3B and S1813) is spin-coated and is patterned for bottom electrode (BE) with 100$\mu$m features using photolithography. The BE metal stack Ti(20nm)/TiN(20nm)/W(50nm) is sputter deposited over the patterned photoresist. The BE is then patterned using a lift-off process during which the photoresist is removed leaving the deposited metal in the photoresist-free region. The photoresist is spin-coated and patterned as before again for the next layer in the device. A 10nm SiO$_2$ film followed by a 100nm Cu film is sputter deposited inside the same chamber without breaking the vacuum at room temperature. The SiO$_2$ and Cu is patterned together by another lift-off process. The resulting 100$\times$100$\mu$m$^2$ cross-point devices (Fig.A1) were subjected to 400$^\circ$C, 5 min annealing in Ar environment.

![Micrograph of the 100$\times$100$\mu$m$^2$ cross-point device with contact pads.](image)

B. STDP programming and plot

In this section, we describe how the STDP characterization of the device was performed. We used Agilent B1500 semiconductor parameter analyzer with a B1530 unit. B1530 is an arbitrary waveform generator and fast measurement unit (WGFMU) capable of applying 100ns pulses and accurate current measurement with up to 5ns sampling rate. The set-up is connected to a probe station where the device is probed and characterized. The programming waveforms were created in Matlab and the B1530 was controlled from Matlab using custom functions.

The spike programming waveforms were designed using Matlab and were converted to voltage signals using the WGFMU. A slow dual voltage sweep with a ramp rate of approximately 2V/s was used to characterize the device for its discrete switching behavior. For the STDP characterization of the device, 1s long patterns where used at a time, and in that duration each 250ms was used for a waveform corresponding to one spike pair. The waveforms were created from data-points at a resolution of 0.5ms. Read pulses of 5ms duration and 50mV amplitude were inserted at the ends and in between the programming waveforms to determine the state of the device. Programming waveforms corresponding to randomly chosen 2000 $\Delta t$ ($\in [-80ms, +80ms]$) were applied to the Cu terminal of the device. The resulting current as a function of time is read using the measurement unit. The average current during the read pulse is divided with the read voltage to get the device conductance changes due to each STDP event. However, after approximately 1000 programming events the device became relatively unresponsive and was stuck to a narrow range of conductance. Also, the conductance response outside the window of $[-40ms, +40ms]$ was not well correlated and are discarded from the study. Now, to determine the STDP plot in Fig.2d, $\Delta G_{norm}$s corresponding to each unique $\Delta t$ were averaged. For the state-dependent responses in Fig.3a,b the $\Delta G_{norm}$s were averaged whose $G_i$ were in the chosen range.
FIG. A2. Peak points and the corresponding double-exponential function fit for $\Delta G_{norm}$ versus $\Delta t$ data with low (a, b) and medium (c,d) initial conductance are shown separately for positive and negative $\Delta t$s.

C. Data fitting and phenomenological model

Here, we describe how the parameters in the phenomenological model (equation (2, 3)) are obtained from the device STDP response. We first obtained peak-fits of the experimentally measured average $\Delta G_{norm}$ data points for medium and low initial conductance range separately for the positive and negative $\Delta t$ range (Fig.A2). The phenomenological model for the STDP behavior of the device was obtained by fitting a function, $f = A(\exp(-\Delta t/\tau_A) - \exp(-\Delta t/\tau_B))$, to the peak-fit points of the $\Delta G_{norm}$ vs $\Delta t$ in a state dependent manner. Fig.A2a shows the peak-points in a moving $\Delta t$ window of 5ms within the range of [0, 40ms] for $\Delta G_{norm}$ data points which are in a low initial conductance range ($G_i \in [0.016 G_0, 0.05 G_0]$) with a mean of 0.03 $G_0$ where $G_0 = 2e^2/h$). The corresponding function $f$ fit line obtained using gradient descent is also shown over the peak-fit points. Fig.A2b shows the peak-fit points and the corresponding model fit line for the negative $\Delta t$ range. Fig.A2c,d show the similar model fitting results for the medium initial conductance range ($G_i \in [0.05 G_0, 0.16 G_0]$) which has a mean of 0.1 $G_0$. The exponential fit lines give the time constants $\tau_A$ and $\tau_B$ as a function of the initial conductances for positive and negative $\Delta t$s. The phenomenological model determine the next state for each spike-pair based programming using the relation $\Delta G_{norm} = A(\exp(-\Delta t/\tau_A) - \exp(-\Delta t/\tau_B))$. We observed that the $\tau_A$ and $\tau_B$ are functions of the conductance of the device before programing and the sign of the time difference between the programming spike pairs ($\Delta t$). We approximated the time constant versus initial conductance relation using linear functions of $\log(G_i)$ as $\tau = \alpha + \beta \times \log(G_i/G_0)$. Fig A3a shows the linear fits for $\Delta t > 0$ and Fig A3b shows the linear fits for $\Delta t < 0$. At the points where the two lines meet, we have $\tau_A = \tau_B$ and $\Delta G_{norm} = 0$. We limit the range of the phenomenological model within the boundary points at which $G_{norm}$ becomes zero. Slopes and intercepts of the linear fits are used to determine the parameters $\alpha$s and $\beta$s.

D. Spiking neural network emulation

In our SNNs the input layer encodes information in the form of spikes using a Poisson process. An input, such as image pixel intensity, is used as the rate constant for the random process to generate a sequence of events representing the spikes. These spikes are propagated via the synaptic junctions and the resulting currents are integrated by the next layer neurons. Here, we used LIF models to emulate the neurons where the neurons are leaky capacitors integrating the input current and fire a spike when the integrated voltage crosses a threshold ($\theta$) and then the voltage across the capacitor is reset to neuron resting potential ($E_L$). This LIF neuron dynamics are emulated by the integral, $V_m = (1/C_m) \int \Sigma_{syn} - g_L(V_m - E_L)dt$ whose approximate solution is determined using second-order Runge-Kutta method. The capacitor voltage, $V_m$, which emulates the biological neuron membrane potential, is held at $E_L$ for a refractory period of 5ms after a spike. The $I_{syn}$ is the current through
FIG. A3. The \( \tau_A \) and \( \tau_B \) as a function of \( G_i \) is fitted with linear functions for positive \( \Delta t \) in (a) and negative \( \Delta t \) in (b). The solid markers denote the \( \tau \) values obtained by the data fitting and open markers are obtained by extending the linear fit. The meeting points of the lines determine the boundary conductance for the STDP operation of the phenomenological model.

The synapse in response to a spike and is modeled as \( W(\exp(-t/\tau_1) - \exp(-t/\tau_2)) \), where \( W \) represent the synaptic strength and the difference of two exponentials model the synaptic current kernel. Each spike from the pre-synaptic layer will cause a current \( I_{syn} \) to pass through the synapse, and the currents from all such input synapses will be integrated at the post-synaptic neuron. In our simulation we used \( \tau_1 = 5 \text{ms} \) and \( \tau_2 = 1.25 \text{ms} \), \( C_m = 300 \text{pF} \), \( g_L = 30 \text{nS} \), \( \theta = 20 \text{mV} \), and \( E_L = -70 \text{mV} \) and the simulation time-step was 0.1 ms.

E. Sequence predictor network

The spiking neural network structure used for the sequence predictor is shown in Fig. A4. The input image pixels are binarized using a threshold and is encoded using a high and low spike rate for a Poisson random process. Each image is shown for 100 ms and followed by a gap period of 50 ms. The input image sequence was \( N \rightarrow J \rightarrow I \) and output image sequence was \( J \rightarrow I \rightarrow T \). The network synapse-updates during the training were implemented in a state-dependent manner using the phenomenological model.

FIG. A4. The network structure for the sequence predictor. The image pixel intensities are used as time constants for a Poisson process to generate input and desired output neuron spike responses. The network synapses are realized using the phenomenological model for the STDP response from the Cu/SiO\(_2\)/W memristive device.
The device fabrication and characterization was carried out at IIT Bombay Nanofabrication Facility with partial support from grant 5102-1 from Indo-French Centre for the Promotion of Advanced Research (CEFIPRA). The analysis, modeling, and training simulations were carried out while the authors were at New Jersey Institute of Technology, Newark, USA.

ACKNOWLEDGEMENT

A. Sadik, I. Antonoglou, H. King, D. Kumaran, D. Wierstra, S. Legg, and D. Hassabis, “Human-level control through deep reinforcement learning,” Nature 518, 529–533 (2015).

C. Szegedy, S. Ioffe, and V. Vanhoucke, “Inception-v4, Inception-ResNet and the Impact of Residual Connections on Learning,” Proceedings of the Thirty-First AAAI Conference on Artificial Intelligence (2017), 1602.0726.

P. J. Sjöström, G. G. Turrigiano, and S. B. Nelson, “Rate, timing, and cooperativity jointly determine cortical synaptic plasticity,” Neuron 32, 1149–1164 (2001).

A. Citri and R. C. Malenka, “Synaptic Plasticity: Multiple Forms, Functions, and Mechanisms,” Neuropsychopharmacology 33, 18–41 (2007).

F. Zenke, E. J. Agnes, and W. Gerstner, “Diverse synaptic plasticity mechanisms orchestrated to form and retrieve memories in spiking neural networks,” Nature Communications 6 (2015), 10.1038/ncomms10722.

L. F. Abbott and W. G. Regehr, “Synaptic computation,” Nature 431, 796–803 (2004).

B. Nessler, M. Pfeiffer, L. Buesing, and W. Maass, “Bayesian computation emerges in generic cortical microcircuits through spike-timing-dependent plasticity,” PLOS Computational Biology 9, 1–30 (2013).

T. Masquelier, R. Guayonneau, and S. J. Thorpe, “Spike timing dependent plasticity finds the start of repeating patterns in continuous spike trains,” PLOS ONE 3, 1–9 (2008).

G. Q. Bi and M. M. Poo, “Synaptic modifications in cultured hippocampal neurons: dependence on spike timing, synaptic strength, and postsynaptic cell type,” J. Neurosci. 18, 10464–10472 (1998).

P. A. Merolla, J. V. Arthur, K. Alvarez-Icaza, A. S. Cassidy, J. Sawada, F. Akopyan, B. L. Jackson, N. Imam, C. Guo, Y. Nakamura, B. Brezzo, I. Vo, S. K. Esser, R. Appuswamy, B. Tabu, A. Amir, M. D. Flickner, W. P. Risk, R. Manohar, and D. S. Modha, “A million spiking-neuron integrated circuit with a scalable communication network and interface,” Science 345, 668–673 (2014).

S. K. Esser, P. A. Merolla, J. V. Arthur, A. S. Cassidy, R. Appuswamy, A. Andreopoulos, D. J. Berg, J. L. McKinstry, T. Melano, D. R. Barch, C. Di Nolfo, P. Datta, A. Amir, B. Tabu, M. D. Flickner, and D. S. Modha, “Convolutional networks for fast, energy-efficient neuromorphic computing,” Proceedings of the National Academy of Sciences (2016), 10.1073/pnas.1604850113.

S. B. Furber, F. Galluppi, S. Temple, and A. Plana, “The SpiNNaker project,” Proceedings of the IEEE 102, 652–665 (2014).

B. V. Benjamin, P. Gao, E. McQuinn, S. Choudhary, A. R. Chandrasekaran, J. M. Bussat, R. Alvarez-Icaza, J. V. Arthur, P. A. Merolla, and K. Bouhen, “Neurogrid: A mixed-analog-digital multichip system for large-scale neural simulations,” Proceedings of the IEEE 102, 699–716 (2014).

J. Schemmel, D. Bruderle, A. Grund, M. Hock, K. Meier, and S. Millner, “A wafer-scale neuromorphic hardware system for large-scale neural modeling,” Proceedings of the 2010 IEEE International Symposium on Circuits and Systems (ISCAS’10), 1947–1950 (2010).

I. Gehrhaar, “Neuromorphic processing: A new frontier in scaling computer architecture,” in Proceedings of the 19th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), (2014) pp. 317–318.

N. Qiao, H. Mostafa, F. Corrada, M. Osswald, F. Stefanini, D. Sumislawski, and G. Indiveri, “A reconfigurable on-line learning spiking neuromorphic processor comprising 256 neurons and 128k synapses,” Frontiers in Neuroscience 9, 141 (2015).

Y. H. Chen, T. Krishna, J. S. Emer, and V. Sze, “Eyeriss: An energy-efficient reconfigurable accelerator for deep convolutional neural networks,” IEEE Journal of Solid-State Circuits 52, 127–138 (2017).

B. N. Panwar, D. Kumar, N. Upadhyay, P. Arya, U. Ganguly, and B. Rajendran, “Memristive synaptic plasticity in Pr0.7Ca0.3MnO3 RRAM by bio-mimetic programming,” in Device Research Conference (DRC), 2014 72nd Annual (2014) pp. 135–136.

S. Mandal, A. El-Amin, K. Alexander, B. Rajendran, and R. Jia, “Novel synaptic memory device for neuromorphic computing,” Nature Scientific Reports 4 (2014), 10.1038/srep05533.

B. Rajendran and F. Alibart, “Neuromorphic computing based on emerging memory technologies,” IEEE Journal on Emerging and Selected Topics in Circuits and Systems PP, 1–14 (2016).

B. L. Jackson, B. Rajendran, G. S. Corrado, M. Breitwisch, G. W. Burr, R. Cheek, K. Gopalakrishnan, S. Raoux, C. T. Rettner, A. Padilla, A. G. Schrott, R. S. Shenoy, B. N. Kurd, C. H. Lam, and D. S. Modha, “Nanoscale Electronic Synapses using Phase Change Devices,” in ACM Journal of Emerging Technologies for Computing Vol. 9 (2013) pp. 12:1–12:20.

D. Querlioz, O. Bichler, A. F. Vincent, and C. Gamrat, “Bioinspired programming of memory devices for implementing an inference engine,” Proceedings of the IEEE 103, 1398–1416 (2015).

D. Kuzum, R. Jeyasingh, S. Yu, and H.-S. Wong, “Low-Energy Robust Neuromorphic Computation Using Synaptic Devices,” Electron Devices, IEEE Transactions on 59, 3380–3404 (2012).

M. Prezioso, F. Merrikh-Bayat, B. Hoskins, G. Adam, K. Likharev, and D. Strukov, “Training and operation of an integrated neuromorphic network based on metal-oxide memristors,” Nature 521, 61–64 (2015).

S. R. Nandakumar, M. Minvielle, S. Nagar, C. Dubourdieu, and B. Rajendran, “A 250 mW Cu/SiO2/W Memristor with Half-Integer Quantum Conductance States,” Nano Letters 16, 1602–1608 (2016).

B. Rajendran, Y. Liu, J. Seo, K. Gopalakrishnan, L. Chang, D. Friedman, and M. Ritter, “Specifications of nanoscale devices and circuits for neuromorphic computational systems,” IEEE Transactions on Electron Devices, 246–253 (2015).
D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, “The missing memristor found,” Nature 459, 1154–1154 (2009).

P. Mazumder, S. M. Kang, and M. S. Waser, “Memristors: Devices, Models, and Applications,” Proceedings of the IEEE 100, 1911–1919 (2012).

S. Park, H. Kim, M. Choo, J. Noh, A. Sheri, S. Jung, K. Seo, J. Park, S. Kim, W. Lee, J. Shin, D. Lee, G. Choi, J. Woo, E. Cha, J. Jang, C. Park, M. Jeon, B. Lee, B. H. Lee, and H. Hwang, “RRAM-based synapse for neuromorphic system with pattern recognition function,” in 2012 International Electron Devices Meeting (IEEE), pp. 10.2.1–10.2.4.

S. Park, A. Sheri, J. Kim, J. Noh, J. Jang, M. Jeon, B. Lee, B. R. Lee, B. H. Lee, and H. Hwang, “Neuromorphic speech systems using advanced ReRAM-based synapse,” in 2013 IEEE International Electron Devices Meeting (IEEE), pp. 25.6.1–25.6.4.

W. Chen, R. Fang, M. B. Balaban, W. Yu, Y. Gonzalez-Velo, H. J. Barnaby, and M. N. Kozicki, “A CMOS-compatible electronic synapse device based on Cu/SiO2/W programmable metallization cells,” Nanotechnology 27, 255202 (2016).

M. Suri, O. Bichler, D. Querlioz, O. Cueto, L. Periulna, V. Sousa, D. Vuillaume, C. Gamrat, and B. DeSalvo, “Phase change memory as synapse for ultra-dense neuromorphic systems: Application to complex visual pattern extraction,” in Electron Devices Meeting (IEDM), 2011 IEEE International (2011) pp. 4.4–1.4.4.

T.-T. Wang, Y.-C. Lin, Y.-F. Wang, C.-W. Hsu, and T.-H. Hou, “3D synaptic architecture with ultralow sub-10 fJ energy per spike for neuromorphic computation,” in 2014 IEEE International Electron Devices Meeting Vol. 2015-February (IEEE) pp. 28.5.1–28.5.4.

S. Yu, T.-S. Philip Wong, “Modeling the switching dynamics of programmable-metallization-cell (PMC) memory and its application as synapse device for a neuromorphic computation system,” in 2010 International Electron Devices Meeting (IEEE), pp. 22.1.1–22.1.4.

M. Prezioso, F. Merrikh-Bayat, B. Hoskins, K. Likharev, and D. Strukov, “Self-adaptive spike-time-dependent plasticity of metal-oxide memristors,” Nature Scientific Reports 6, 21331 (2016), arXiv:1505.05549.

C. Wang, W. He, Y. Tong, and R. Zhao, “Investigation and manipulation of different analog behaviors of memristor as electronic synapse for neuromorphic applications,” Scientific Reports 6, 21331 (2016), arXiv:1505.05549.

M. Prezioso, Y. Zhong, D. Gavrilov, F. Merrikh-Bayat, B. Hoskins, G. Adam, K. Likharev, and D. Strukov, “Spiking neuromorphic networks with metal-oxide memristors,” in 2016 IEEE International Symposium on Circuits and Systems (ISCAS) (IEEE) Vol. 2016-July (IEEE) pp. 177–180.

G. Pedretti, V. Milo, S. Ambrogio, R. Carboni, S. Bianchi, A. Calderoni, N. Ramaswamy, A. S. Spinelli, and D. Ielmini, “Stochastic learning in neuromorphic hardware via spike timing dependent plasticity with RRAM synapses,” IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 1–1 (2017).

F. Ponulak and A. Kasifski, “Supervised learning in spiking neural networks with ReSuMe: Sequence learning, classification, and spike shifting,” Neural Comput. 22, 467–510 (2010).

D. Querlioz, O. Bichler, and C. Gamrat, “Simulation of a memristor-based spiking neural network immune to device variations,” in The 2011 International Joint Conference on Neural Networks (IEEE), pp. 1775–1781, arXiv:arXiv:1011.1669v3.

P. U. Diehl, D. Neil, J. Binas, M. Cook, S. C. Liu, and M. Pfeiffer, “Fast-classifying, high-accuracy spiking deep networks through weight and threshold balancing,” in 2015 International Joint Conference on Neural Networks (IJCNN) (IEEE) pp. 1–8.

I. Boybat, M. Le Gallo, S. R. Nandakumar, T. Moraatis, T. Parnell, T. Tuma, B. Rajendran, Y. Leblebici, A. Sebastian, and E. Eleftheriou, “Neuromorphic computing with multi-memristive synapses,” Nature Communications 9, 1–12 (2018), arXiv:1711.06507.

M. Kozicki, M. Balakrishnan, C. Gopalan, C. Ramakumar, and M. Mitkova, “Programmable metallization cell memory based on Ag-Ge-S and Cu-Ge-S solid electrolytes,” in Symposium Non-Volatile Memory Technology 2005, (IEEE), pp. 83–89.

C. Schindler, S. C. P. Thermadam, R. Waser, and M. N. Kozicki, “Bipolar and Unipolar Resistive Switching in Cu-Doped SiO2,” IEEE Transactions on Electron Devices 54, 2762–2768 (2007).

U. Russo, D. Kamalanathan, D. Ielmini, A. L. Lacaita, and M. N. Kozicki, “Study of Multilevel Programming in Programmable Metallization Cell (PMC) Memory,” IEEE Transactions on Electron Devices 56, 1040–1047 (2009).

I. Valov, R. Waser, J. R. Jameson, and M. N. Kozicki, “Electrochemical metallization memories–fundamentals, applications, prospects,” Nanotechnology 22, 254003 (2011).

J. R. Jameson, P. Blanchard, C. Cheng, J. Dinh, A. Gallo, V. Gopalakrishnan, C. Gopalan, B. Guichet, S. Hsu, D. Kamalanathan, D. Kim, F. Koushan, M. Kwan, K. Lau, D. Lewis, Y. Ma, V. McCaffrey, S. Park, S. Puthentharmad, E. Runnion, J. Sanchez, J. Shields, K. Tsai, A. Tysdal, D. Wang, R. Williams, M. N. Kozicki, J. Wang, V. Gopinath, S. Hollmer, and M. Van Buskirk, “Conductive-bridge memory (CBRAM) with excellent high-temperature retention,” Technical Digest - International Electron Devices Meeting, IEDM, 738–741 (2013).

J. R. Jameson, P. Blanchard, J. Dinh, N. Gonzales, V. Gopalakrishnan, B. Guichet, S. Hollmer, S. Hsu, G. Intrader, D. Kamalanathan, D. Kim, F. Koushan, M. Kwan, D. Lewis, B. Pedersen, M. Ramsbey, E. Runnion, J. Shields, K. Tsai, A. Tysdal, D. Wang, and V. Gopinath, “(Invited) Conductive Bridging RAM (CBRAM): Then, Now, and Tomorrow,” ECS Transactions, 41–54.

N. Gonzales, J. Dinh, D. Lewis, N. Gilbert, B. Pedersen, D. Kamalanathan, J. R. Jameson, and S. Hollmer, “An Ultra-Low-Power Non-Volatile Memory Design Enabled by Subquanutm Conductive-Bridge RAM,” in 2016 IEEE 8th International Memory Workshop (IMW) (IEEE) pp. 1–4.

S. H. Jo, T. Chang, J. Bong, B. B. Bhadvia, P. Mazumder, and W. Lu, “Nanoscale Memristor Device as Synapse in Neuromorphic Systems,” Nano Letters 10, 1297–1301 (2010).

E. Covi, S. Brivio, A. Serb, T. Prodromakis, M. Fanciulli, and S. Spiga, “Analog memristive synapse in spiking networks implementing unsupervised learning,” Frontiers in Neuroscience 10, 1–13 (2016).

D. Mahalanabis, M. Sivaraj, W. Chen, S. Shah, H. J. Barnaby, M. N. Kozicki, J. B. Christen, and S. Vrudhula, “Demonstration of spike timing dependent plasticity in CBRAM devices with silicon neurons,” in 2016 IEEE International Symposium on Circuits and Systems (ISCAS) (IEEE) Vol. 2016-July (IEEE) pp. 2314–2317.

S. Lim, C. Sung, H. Kim, T. Kim, J. Song, J. J. Kim, and H. Hwang, “Improved Synapse Device with MLC and Conductance Linearity Using Quantized Conductance for Device Learning,” IEEE Electron Device Letters 39, 312–315 (2018).

S. R. Nandakumar, M. Le Gallo, I. Boybat, B. Rajendran, A. Sebastian, and E. Eleftheriou, “Mixed-precision architecture based on computational memory for training deep neural networks,” in 2018 IEEE International Symposium on Circuits and Systems (ISCAS) (IEEE) pp. 1–5.

C. Zamarro-Ramos, L. A. Camunas-Mesa, J. A. Pérez-Carrasco, T. Masquelier, T. Serrano-Gotarredona, and B. Linares-Barranco, “On Spike-Timing-Dependent-Plasticity, Memristive Devices, and Building a Self-Learning Visual Cortex,” Frontiers in Neuroscience, 1–22.

N. F. Mott and R. W. Gurney, Electron Processes in Ionic Crystals (Oxford University Press, 1948).

C. Schindler, G. Staikov, and R. Waser, “Electrode kinetics of Cu-SiO2 based resistive switching cells: Overcoming the voltage-time dilemma of electrochemical metallization memories,” Applied Physics Letters 94, 92–95 (2009).

S. Menzel, U. Böttger, W. Wimmer, and M. Sallina, “Physics of the Switching Kinetics in Resistive Memories,” Advanced Functional Materials 25, 6306–6325 (2015).