A Phase-Shifted Full-Bridge Converter Used for DC Charging Pile

Mingda Zhang¹, Sijin Wang¹, Yihui Sun¹, Zhejun Guo¹, Jianyu Bao²,*

¹State Grid Zhejiang Ningbo Fenghua Electric Power Co.Ltd., China
²School of Electronic and Information Engineering, Ningbo University of Technology Ningbo, China

*Corresponding author e-mail: jianyu_bao@126.com

Abstract. The zero-voltage switching (ZVS) phase-shifted full-bridge (PSFB) converter has the advantages of simple circuit topology, low voltage and current stress, and controllable working frequency. If applied to the dc charging pile, it can effectively reduce the switching loss and improve the overall operating efficiency of the power supply system. The working principle of ZVS PSFB converter is analyzed, and the main circuit topology of the converter is determined by combining with the technical specifications required by the dc charging pile. Based on PI control, wide range dc voltage output of converter is realized. Finally, PSIM is used to carry out simulation test on the PSFB converter, and the simulation results verify the correctness of ZVS operation and the effectiveness of closed-loop control.

1. Introduction

At present, the main circuit of the DC charging pile of electric vehicles usually uses three-phase ac as the input power supply [1], the DC bus voltage is obtained through the diode rectifier bridge and LC filter link, and then uses the isolated full-bridge DC/DC converter to implement the voltage transformation. The available isolated full-bridge DC/DC converters include hard switching PWM converters, series/parallel resonant converters and phase-shifting full-bridge converters [2-4]. Among them, the traditional hard switching PWM converter has become the most mature technology and the most popular circuit topology for high-power DC charging pile because of its simple main circuit structure and control method. However, it also has some disadvantages such as large volume, low switching frequency and high noise. The ZVS phase-shifting full-bridge converter, due to its small size, high efficiency, low noise and low loss, is gradually replacing the hard switching PWM converter and is increasingly used in the DC charging pile system of electric vehicles.

The phase-shifting full-bridge soft switching technology can be divided into two categories. One is ZVS, the zero-voltage switching of converter switch is completed by virtue of resonant capacitor and resonant inductor (or leakage inductor), and no additional auxiliary circuits are required. It has the advantages of constant working frequency, simple control method and small switching loss, but at the same time it also has the disadvantages of transformer side duty-ratio loss, lag bridge arm ZVS difficult to realize [5]. The other type is zero-voltage zero-current switching (ZVZCS) [6], which is different from ZVS in that the leading bridge arm realizes ZVS, while the lagging bridge arm does not need resonant capacitance to realize ZCS. The advantage of ZVZCS over ZVS technology is that there is no loss of duty-cycle of transformer side, and the conversion efficiency is improved. However, this technology requires the addition of more complex auxiliary circuit, which increases the area of the
control board and improves the difficulty of control and debug. By comparing with two kinds of soft switching technology, although the former maybe lead to a transformer duty ratio loss, and the lag bridge arm of the soft switch is more difficult to achieve, but such technology can fully use the parasitic parameters of the main circuit, which makes the phase shifting full bridge ZVS converter of simple structure, convenient control and easy implementation, so more and more medium and large-sized power converters adopt the phase-shifting full bridge ZVS soft switching technology.

2. The operational principle of PSFB

\( \text{Figure 1. Main circuit of PSFB} \)

The main circuit topology of the phase-shifting full-bridge ZVS converter is shown in Figure 1. Among them, \( S_1 \sim S_4 \) are the four MOSFETs, \( D_1 \sim D_4 \) are the anti-parallel diodes of the four MOSFETs, and \( C_1 \sim C_4 \) are the external resonant capacitors. \( L_r \) is the resonant inductor, wherein \( L_r \) includes leakage inductance of transformer; \( D_5 \sim D_8 \) are output rectifier diodes, \( L_f \) and \( C_f \) constitute the output filter circuit. Due to the high input voltage of the dc charging pile, the full-bridge rectifier is adopted at the output side of the phase-shifting full-bridge converter, which can meet the requirements of high output voltage and high power.

2.2. The operational principle of phase-shift PWM

The phase-shifting PWM control is obviously different from the symmetrical PWM control, as shown in Figure 2. Each top and bottom switch of the two bridge legs is 180° complementary conduction, and the driving signals of two diagonal switches have a phase difference \( \theta \), this is called the phase-shifting angle. Between the two groups of bridge arms, the driving signal of \( S_1 \) is ahead of \( S_4 \) with angle \( \theta \). Similarly, the driving signal of \( S_3 \) is also ahead of \( S_2 \) with angle \( \theta \). Therefore, \( S_1 \) and \( S_3 \) constitute the leading bridge arm, while \( S_2 \) and \( S_4 \) constitute the lagging bridge arm. If the dead-zone time between the upper and lower switches of the same bridge arm is excluded, the driving signals of the two diagonally inclined switches will shift according to the required duty-ratio. The larger the overlap of the two driving signals, the wider the square-voltage wave on the primary side of the transformer and the higher the output voltage. Therefore, for the phase-shifting control method, the duty-cycle is changed by adjusting the phase angle, so as to realize the adjustment of output dc voltage.
3. The implementation principle of ZVS

The full bridge converter can generate resonance by using the resonant inductor in series with the primary-side leakage inductor of the transformer and the buffer capacitors in parallel with the power switches, so that both the leading bridge arm and lagging bridge arm switches can achieve zero-voltage opening and zero-voltage closing, the specific implementation process is shown in Figure 3.

(1) Mode 0: \([0, t_0]\)

\(S_1\) and \(S_4\) conducted at the same time. The primary current \(i_p\) is supplied by the input dc source through \(S_1\), the equivalent resonant inductor \(L_r\) of the transformer, the primary winding of the transformer and the rectifier diodes \(D_1\) and \(D_4\) at the transformer secondary-side to supply for the load.

(2) Mode 1: \([t_0, t_1]\)

At time \(t_0\), \(S_1\) is switched off, and the primary current \(i_p\) is transferred from \(S_1\) to capacitor \(C_1\) and \(C_3\). The primary current \(i_p\) is close to constant, equivalent to a constant-current source, \(C_1\) is charging and \(C_3\) is discharging. The voltage of capacitor \(C_1\) gradually rises from the initial 0 to the input voltage \(U_i\), while the voltage of \(C_3\) drops from \(U_i\) to 0. \(D_3\) conducts naturally, which creates the condition of zero-voltage switching on for \(S_3\).

(3) Mode 2: \([t_1, t_2]\)

When \(D_3\) is switched on, the drain-source voltage of \(S_1\) is naturally clamped at zero. At this time, when \(S_3\) is switched on, the zero-voltage switching can be obtained. To ensure that \(S_3\) can be ZVS, the dead-zone time between \(S_1\) and \(S_3\) must be greater than the duration time of mode 1.

(4) Mode 3: \([t_2, t_3]\)

At \(t_2\), \(S_4\) is switched off, and the primary current charges \(C_4\) and discharges \(C_2\) at the same time. Because of them, \(S_4\) was zero-voltage off, and \(u_{AB} = -u_{C4}\), the voltage polarity of \(u_{AB}\) changes from zero to negative. At the moment of \(t_3\), the voltage on \(C_4\) rises to the input voltage \(U_i\), \(D_2\) conducts naturally, creating condition for \(S_2\) to realize zero-voltage on.

(5) Mode 4: \([t_3, t_4]\)

At the moment of \(t_3\), \(D_2\) is naturally conducted to clamp the voltage of \(S_2\) at zero. At this time, if \(S_2\) is switched on, ZVS is realized. Similarly, in order to realize ZVS, a certain dead-zone time must be left between the driving signals of \(S_2\) and \(S_4\). Till the moment of \(t_4\), resonant current \(i_p\) drops to zero, \(D_2\) and \(D_1\) turns off naturally, \(S_2\) and \(S_3\) starts working.

(6) Mode 5: \([t_4, t_5]\)

At time \(t_4\), \(i_p\) drops to zero. After that, \(S_2\) and \(S_3\) provides the current loop for \(i_p\), it gradually increases at the negative direction with the dc voltage.

(7) Mode 6: \([t_5, t_6]\)

During this period, the input dc voltage supplies power to the load through \(S_2\) and \(S_3\), and the primary current \(i_p\) rises slowly. At the moment of \(t_6\), \(S_3\) is switched off and the whole circuit enters another half cycle. Its working condition is similar to the six working modes described above.
4. Simulation analysis

4.1. Simulation model

The simulation model of the phase-shifting full-bridge ZVS converter is built in the PSIM environment [7], as shown in Figure 4. The input dc voltage is 800V, the switching frequency is 20kHz, the leading arm resonant capacitor is 16nF and the lagging arm resonant capacitor is 10nF, the output filter inductance is 600μH, the output filter capacitor is 200μF, the load size is 15Ω, the resonant inductance is 50μH.

![Figure 4. The simulation model of PSFB](image)

The phase-shifting pulse signals are generated by two monostable triggers, one of which generates the driving signal of the leading bridge arm, the other generates the driving signal of the lagging bridge arm, and the duty-cycle is fixed at 50%. In order to achieve ZVS, the dead-zone time is set at 2.8μs between the driving signals of upper and lower bridge arm.

4.2. Simulation results

4.2.1. PWM waveforms. According to the technical requirements, the working frequency is set at 20kHz, that is, the period is 50μs. The duty cycle of PWM signal is 50%, that is, the pulse width of each group of PWM signal is 25μs, as shown in Figure 5. It can be seen from the figure that the dead-zone time of PWM signal of two switches on the upper and lower bridge arms is about 2.8μs.

![Figure 5. PWM waveforms](image)

4.2.2 ZVS waveforms. Figure 6 shows the ZVS waveforms realized by the leading bridge arm, $S_1$ is the PWM pulse signal of switch $S_1$, and $u_{C1}$ is the voltage of switch $S_1$ ($C_1$). As can be seen from the figure, when the PWM pulse signal sends a high level, the voltage at switch $S_1$ has been reduced to 0,
so ZVS is obtained on the leading bridge arm.

Figure 7. The waveforms of lag bridge arm

Figure 8. DC output voltages

Figure 7 shows the driving pulse signal of \(S_4\) and the voltage of switch \(S_4\) (\(C_4\)) on the lagging bridge arm, compared to Figure 6, it can be seen that the capacitor voltage on the lagging bridge arm drops slower than that of the leading bridge arm, especially when the circuit worked at light load, which may lead to the failure of ZVS for lag bridge arm switch. That is to say, the soft switch implementation of lagging bridge arm is more difficult than that of the leading bridge arm.

4.2.3 The wide-range voltage output. Taking a pure resistance as the load, given with the different reference voltages at the input, the corresponding dc output voltage waveforms of the full-bridge converter are obtained in Figure 8. It can be seen that the regulation time of the system takes about 10ms, and the overshooting is very small. By giving different reference values, the dc voltage can be output stably in the range of 225V-600V, which reflects good voltage output characteristics in a wide operating range.

5. Conclusion

The phase-shifting full-bridge converter is the core of the main circuit of the dc charging pile. The different operation modes of ZVS full-bridge converter with leading and lagging bridge arms are analyzed and discussed. Based on PI control, the wide-range voltage output of full-bridge converter is implemented. Finally, a simulation circuit model is built based on PSIM simulation software to verify the correctness of ZVS and the effectiveness of voltage closed-loop control. Applying ZVS full-bridge phase-shifting converter to dc charging pile, which has important practical significance for improving harmonic and reactive power pollution problems in power system.

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