LOW-POWER DYNAMIC COMPARATOR WITH HIGH PRECISION FOR SAR ADC

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ABSTRACT
In this work, low-power dynamic comparator is presented with auto-zeroing technique for successive approximation register (SAR) analogue-to-digital converter (ADC). The comparator designed with DTMOS technique operates in sub-threshold region. The designed circuit consumes low power with high gain. The dynamic range of the comparator is increased with a new biasing technique for DTMOS transistors. The core design consumes 6.01µW power and overall design consumes 17.06µW. The design is realized with two different supply voltage with 600mV (core design) and 1.8V (biasing circuit). The comparator has been simulated with 0.18µm TSMC process in Cadence environment.

Keywords: SAR ADC, Comparator, CMOS analog integrated circuits
1. INTRODUCTION

Comparative circuits are indispensable interface elements between analog and digital world. Also, comparators play key roles in the design of analog-to-digital converters, memories, dynamic logic, and sense amplifiers as decision-making circuits (Cohen et al. 2005; Kim, Choi, and Lee 2015; Ming-Dou Ker and Jung-Sheng Chen 2008; Verma and Chandrakasan 2007). The input referred offset voltage in the design of comparator circuits is the biggest problem affecting the resolution of converters. Auto-zeroing and chopper methods are useful techniques to cancel offset and low-frequency noise (Cohen et al. 2005; Witte, Makinwa, and Huijsing 2006; Wu, Makinwa, and Huijsing 2009). Dynamic switches with auto-zeroing technique are the common and successful approach to cancel offset (Schinkel et al. 2007; Sepke et al. 2006).

Dynamic comparators are suitable for low-supply, low-power and high-speed applications (Zhong, Bermak, and Tsui 2017). Furthermore, various types of sensors to gather information are applied to everyday objects of Internet of Things (IoT). These sensor requirements oblige the need of analog-to-digital converters (ADCs) dissipated low power with high resolution and high linearity for use in an energy-constrained environment (Shim et al. 2018). Moreover, the power consumption of the dynamic comparators is called the dynamic power. The dynamic power is defined as the power of dissipated during the evaluation of signal in one period of clock. The successive approximation register (SAR) ADCs has the resolution of 12-14 bit level and are very energy-efficient (Yan et al. 2018).

Furthermore, in wide common mode range applications, for example, the speed and offset of CMOS designs in A/D converters depends on the common mode voltage of the input and this is a challenging situation for sub-micron CMOS technologies. However, a large voltage headroom, which is problematic, especially in circuits with transistor stacks and especially in low-voltage deep-micron CMOS technologies (Schinkel et al. 2007; Wicht, Nirschl, and Schmitt-Landsiedel 2004; Wong and Yang 2004).

In this work, offset cancelled low power dynamic comparator for successive approximation register (SAR) ADCs is designed. The CMOS implementation of the designed comparator is realized with standard 0.18µm CMOS technology with DTMOS technique. The designed circuit has mixed 0.6V-1.8V supply voltage. The biasing circuitries (current sources and current sinks) are designed with normal CMOS transistor to extend headroom. The core design is implemented with DTMOS transistors (Achigui et al. 2006; Ramirez-Angulo et al. 2001). DTMOS transistor is realized for only pMOS transistor by connecting its gate to the body without the need for another manufacturing process or step. As a result, the DTMOS transistors can be used in standard CMOS process. DTMOS offers the low power designs for especially biomedical applications and portable devices.

This paper is organized as follows. Section 2 explains the CMOS implementation and layout with analysis. Corner and Monte-Carlo analysis are also given in the same section. Finally, section 3 gives some conclusions.

2. COMPARATOR DESIGN

Due to the nature of analog signals, all IoT applications require both analog and digital system design for a high integration level with low cost. Although many analog designs can perform digitally, the analog-digital converters (ADCs) are still required as an interface between the analog domain and the digital (Lin, Wei, and Lee 2018). Many wireless sensor node (WSN) for IoT applications require low-power ADCs ranging in resolution (8 - 12 bit) and speed around (MS/s) (Ding et al. 2018). Comparators are the essential building block of the successive approximation register (SAR) ADCs. Comparators need extremely low offset, and very low input noise. The dynamic range of the comparator can be improved by cancelling the low-frequency noise and offset with auto-zeroing technique (Enz and Temes 1996).

Operational amplifiers have been used as basic circuit components in analog circuit design since the emergence of integrated circuits. After the emergence of new analog circuit applications, the performance characteristics of the voltage-mode operational amplifiers are not sufficient for analog signal processing requirements. The compensation capacitance, which ensures the stability of the OPAMP (operational amplifier), reduces the bandwidth of the operational amplifier due to the excessive voltage gain expected from OPAMP (Palmasano G. 1999). Therefore, OPAMPs are replaced by operational transconductance amplifiers (OTAs) whose output resistance is quite high (Maloberti 2006). At the same time, in a fully differential system not only rejects the common mode voltages but also eliminates the external noise. For the reasons mentioned above, the CMOS implementation of comparator is realized with fully differential operational transconductance amplifier in sub-threshold region.

Fig. 1 shows a block diagram of the comparator structure. The proposed implementation is developed based on the comparator proposed in (Allen and Holberg 2012). The structure of the comparator is made up of a fully differential operational transconductance amplifier, latch and switch. The gain of the overall design is 142.8dB. The overall design consists of three cells. Each cell has the gain of 35.7dB. The input referred offset is $V_{OSS1} + V_{OSS2} / A_{V1} + V_{OSS3}/A_{V1}A_{V2}$. $V_{OSS1}$ and $A_{V1}$ is the first cell’s offset voltage and gain, respectively. $V_{OSS2}$ and $A_{V2}$ define the second cell’s offset voltage and gain while the third stage offset and gain is defined as $V_{OSS3}$ and $A_{V3}$, respectively.

OTAs and dynamic latch operate in sub-threshold region and the supply voltage is 0.6V. The biasing circuit operates with 1.8V supply voltage. pMOS transistor of core design are designed with DTMOS technique to decrease the power dissipation and to increase the gain and dynamic range of the design.
Fig. 1 Block diagram of the designed comparator

Fig. 2 CMOS implementation of overall comparator
(1) shows the transistor current in sub-threshold region. \( I_0 \) and \( m \) are technology dependent parameters, \( V_T = kT/q \) is thermal voltage.

\[
I = I_0 W \frac{V_{GS}-V_{th}}{mV_T^2} (1 - e^{-(V_{GS}/V_T)}) \tag{1}
\]

The sub-threshold current-voltage relationship of the MOS transistor is very similar to the bipolar transistor, but still the gain effect of the threshold voltage is clearly visible as in (1). The threshold voltage of the transistor is decreased dynamically by connecting the device gate and body, seen as the relationship given in (2).

The DTMOS transistor under the same \( V_{GS} \) voltage has a higher \( g_m \) than the MOS transistor. (3) gives the relationship of \( g_m \) under sub-threshold region. As a result, DTMOS transistor has higher gain than the standards under same conditions.

Only pMOS transistors can be selected as DTMOS because of the single well process of used 0.18µm CMOS process. The biasing circuit is designed with standard CMOS transistor with 1.8V supply voltage to increase the swing and gain of amplifier. Table 1 gives the size of the transistors.

Table 1. The size of the transistors

| Transistors | W/L       |
|-------------|-----------|
| Supply Voltage (1.8V) Biasing Transistors | B1, B2, B3, B4, B5, B6, B7 | 10µm/2µm |
| Supply Voltage (1.8V) Switch | S1 | 100µm/180nm |
| Supply Voltage (0.6V) Switch | S2 | 100µm/180nm |
| Operational Transconductance Amplifier | M1, M2, 8µm/360nm |
| | M3, M4, 4µm/360nm |
| | M5, M6, 8µm/360nm |
| | M7, M8, 10µm/360nm |
| | M9, M10, M11, M12, 8µm/360nm |
| Latch | DT莫斯 Technique | T1, T1, 6µm/180nm |
| | | T2, T2, 1.3µm/180nm |
| | | T3, T1, 6.6µm/180nm |
| | | T4, T1, 6.6µm/180nm |
| | | T5, 4µm/180nm |
| | | T11, T11, 3µm/180nm |
| | | T12, T11, 1µm/180nm |

The CMOS implementation of the comparator is given in Fig. 2. The implementation of temperature independent current generator is designed based on (Alaybeyoğlu and Kuntman 2016). Layout of the comparator is given in Fig. 3. The core occupation area of the designed circuit is 61.5µm x 115.4µm; 0.007mm².

\[ |V_{th,p}| = |V_{th,0}| + \gamma (\sqrt{|2\Phi_F|} + V_{SB} - \sqrt{|2\Phi_F|}) \tag{2} \]

\[ g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{I_D}{nV_I} \tag{3} \]

Fig. 3 The layout of overall comparator

Fig. 4 shows the DC gain of single cell. The gain of the overall circuit is 142.8dB for four cascaded OPAMPs. The timing diagram of comparator is given in Fig. 5. Reset and Comparison phased of the comparator are two operation duration. The evaluation of the comparison is realized after the offset cancellation in reset time.

Fig. 4 DC gain of single cell.

Fig. 5 Timing diagram of comparator.
Offset analysis under the variation of process (ss, tt, ff, sf, fs), power supplies (AVDD [0.54V, 0.66V]) and temperatures (−40°C, 85°C) is given in Fig. 6. The solution in Fig. 6 is realized without offset cancellation. Table 2 gives the offset value for each corners. Offset coming from fourth stage is suppressed by the 1st, 2nd and 3th stage gain. Furthermore, offset coming from third stage is suppressed by the 1st and 2nd stage gain. As a result, the most dominant offset contributed by M7, M8 is 1st-stage offset (Zhong, Bermak, and Tsui 2017). The 1st-stage offset is cancelled out with auto-zeroing capacitances (50fF). Fig. 7 shows the Monte Carlo analysis of offset without offset cancellation (OC). Histograms of offset with OC technique given in Fig. 1. is shown in Fig. 8.

Table 2 The offset values according to the each corner

| Temperature | 40°C | 27°C | 85°C |
|-------------|------|------|------|
| AVDD=0.54V  | 22.9m | 5.1m | 3.3m |
| AVDD=0.60V  | 4.9m  | 3.2m | 5.1m |
| AVDD=0.66V  | 5.1m  | 3.5m | 3.1m |

Table 3 Comparison with the State of Art comparator designs

| Parameters | (Cohen et al. 2005) | (Pipino et al. 2016) | (Belloni et al. 2010) | (Lu and Holleman 2013) | This Work |
|------------|---------------------|----------------------|-----------------------|------------------------|-----------|
| Technology | 0.35µm              | 28nm                 | 0.18-0.5µm            | 0.5µm                  | 0.18 µm   |
| Supply Voltage | 3.3/4.5V | 0.9V                             | 1.8/5V                | 5V                     | 0.6/1.8V |
| DC Gain    | 55.7dB              | 106dB                | 168dB                 | 118.1dB                | 142.8dB   |
| GBW        | -                   | 329kHz               | 260kHz                | -                      | 33.3MHz   |
| Input Referred Offset | 413µV | 2.2µV                             | 1.94µV                | 50.57µV                | 6.5 µV    |
| Supply Current | 40µA    | 60µA                         | 14.4µA                | 0.93µA                 | 10.01µA   |
| Power       | 160µW              | 54µW                 | 26/72µW               | 4.62µW                 | 6.01/17.06 µW |
| Area        | 0.0024mm²          | 0.014mm²             | 1.14mm²               | 0.062mm²               | 0.007mm²  |

Fig. 6 Offset analysis (under the variation of process (ss, tt, ff, sf, fs), power supplies (AVDD [0.54V, 0.66V]) and temperatures (−40°C, 85°C)).

Table 3 shows the comparison with state of art. The performances of designed comparator is higher than the previous works in terms of gain, GBW (gain bandwidth product) and core occupation area. GBW of the designed comparator is 33.3MHz while the core occupation area is 0.007mm² without Electrostatic Discharge Protection.

Fig. 7 Monte Carlo analysis of Offset without Offset Cancellation.

Fig. 9 shows the dynamic range of a single amplifier. The dynamic range of the comparator is increased with a new biasing technique for the positive rail. The positive rail of 0.56V approximately approaches to the positive supply voltage of 0.6V with the proposed biasing technique.
Fig. 8 Monte Carlo analysis of Offset with Offset Cancellation.

Fig. 9 Dynamic range of a single amplifier.

3. CONCLUSION

In this work, the design of a low power high precision comparator with 142.8dB gain is presented. The subcircuits (OTA, latch) of the comparator is designed with DTMOS technique. The standard deviation of offset voltage is reduced from 3.31mV to 30.2µV. The core occupation of the designed circuit is 0.007mm². The comparator designed with offset cancellation can operate up to 30MHz with energy consumption per comparison of 20pJ. The designed comparator is implemented with TSMC 0.18µm process in Cadence environment.

REFERENCES

Achigui, Hervé Facqong, Christian Jésus B Fayomi, Mohamad Sawan, and PMC-Sierra. 2006. “1-V DTMOS-Based Class-AB Operational Amplifier: Implementation and Experimental Results.” IEEE Journal of Solid-State Circuits 41(11): 2440–48.

Alaybeyoğlu, Ersin, and Hakan Kuntman. 2016. “CMOS Implementations of VDTA Based Frequency Agile Filters for Encrypted Communications.” Analog Integrated Circuits and Signal Processing 89(3): 675–84.

Allen, P. E., and D. R. Holberg. 2012. CMOS Analog Circuit Design. Oxford uni.

Belloni, Massimiliano, Edoardo Bonizzoni, Andrea Fornasari, and Franco Maloberti. 2010. “A Micropower Chopper - CDS Operational Amplifier.” IEEE Journal of Solid-State Circuits 45(12): 2521–29.

Cohen, M H et al. 2005. “A Floating-Gate Comparator with Automatic Offset Adaptation for 10-Bit Data Conversion A 750MHz 6b Adaptive Floating Gate Quantizer In.” 52(August): 1316–26.

Ding, Ming et al. 2018. “A Hybrid Design Automation Tool for SAR ADCs in IoT.” IEEE Transactions on Very Large Scale Integration (VLSI) Systems 26(12): 2853–62.

Enz, C., and Gabor Temes. 1996. “Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization.” Proc. of the IEEE 84(1): 1584–1614.

Kim, Kichan, Keun Yeong Choi, and Hojin Lee. 2015. “A-InGaZnO Thin-Film Transistor-Based Operational Amplifier for an Adaptive DC-DC Converter in Display Driving Systems.” IEEE Transactions on Electron Devices 62(4): 1189–94.

Lin, Chin Yu, Yen Hsin Wei, and Tai Cheng Lee. 2018. “A 10-Bit 2.6-GS/s Time-Interleaved SAR ADC with a Digital-Mixing Timing-Skew Calibration Technique.” IEEE Journal of Solid-State Circuits 53(5): 1508–17.

Lu, Junjie, and Jeremy Holleman. 2013. “A Low-Power High-Precision Comparator with Time-Domain Bulk-Tuned Offset Cancellation.” IEEE Transactions on Circuits and Systems I: Regular Papers 60(5): 1158–67.

Maloberti, F. 2006. Analog Design for CMOS VLSI Systems. Springer S.

Ming-Dou Ker, and Jung-Sheng Chen. 2008. “Impact of MOSFET Gate-Oxide Reliability on CMOS Operational Amplifier in a 130-Nm Low-Voltage Process.” IEEE Transactions on Device and Materials Reliability 8(2): 394–405.

Palmisano G., Palumbo G. and Pennisi S. 1999. CMOS Current Amplifiers. Boston MA: Kluwer Academic Publishers.

Pipino, A et al. 2016. “A Rail-to-Rail-Input Chopper Instrumentation Amplifier in 28nm CMOS.” Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems 2016-March: 73–76.

Ramirez-Angulo, J, R G Carvajal, J Tombs, and A Torralba. 2001. “Low-Voltage CMOS Op-Amp with Rail-to-Rail Input and Output Signal Swing for Continuous-Time Signal Processing Using Multiple-Input Floating-Gate Transistors.” IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing 48(11): 111–15.

Schinkel, Daniël et al. 2007. “A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+hold Time.” Digest of Technical Papers - IEEE International Solid-State Circuits Conference: 314–16.

Sepke, Todd et al. 2006. “Switched-Capacitor Circuits for Scaled CMOS Technologies.” ISCC Dig. Tech. Papers 41(12): 2658–68.
Shim, Junho, Min Kyu Kim, Seong Kwan Hong, and Oh Kyong Kwon. 2018. “An Ultra-Low-Power 16-Bit Second-Order Incremental ADC with SAR-Based Integrator for IoT Sensor Applications.” *IEEE Transactions on Circuits and Systems II: Express Briefs* 65(12): 1899–1903.

Verma, Naveen, and Anantha P. Chandrakasan. 2007. “An Ultra Low Energy 12-Bit Rate-Resolution Scalable SAR ADC for Wireless Sensor Nodes.” *IEEE Journal of Solid-State Circuits* 42(6): 1196–1205.

Wicht, Bernhard, Thomas Nirschl, and Doris Schmitt-Landsiedel. 2004. “Yield and Speed Optimization of a Latch-Type Voltage Sense Amplifier.” *IEEE Journal of Solid-State Circuits* 39(7): 1148–58.

Witte, Johan F., Kofi A.A. Makinwa, and Johan H. Huijsing. 2006. “A CMOS Chopper Offset-Stabilized Opamp.” *ESSCIRC 2006 - Proceedings of the 32nd European Solid-State Circuits Conference* 42(7): 360–63.

Wong, K. L J, and C. K K Yang. 2004. “Offset Compensation in Comparators with Minimum Input-Reflected Supply Noise.” *IEEE Journal of Solid-State Circuits* 39(5): 837–40.

Wu, Rong, Kofi A. A. Makinwa, and Johan H. Huijsing. 2009. “A Chopper Current-Feedback Instrumentation Amplifier With a 1 MHz 1/f Noise Corner and an AC-Coupled Ripple Reduction Loop.” *IEEE Journal of Solid-State Circuits* 44(12): 3232–43.

Yan, Na et al. 2018. “A 10-Bit 16-MS/s Ultra Low Power SAR ADC for IoT Applications.” *2018 14th IEEE International Conference on Solid-State and Integrated Circuit Technology, ICSICT 2018 - Proceedings*: 1–3.

Zhong, Xiaopeng, Amine Bermak, and Chi Ying Tsui. 2017. “A Low-Offset Dynamic Comparator with Area-Efficient and Low-Power Offset Cancellation.” *IEEE/IFIP International Conference on VLSI and System-on-Chip, VLSI-SoC*. 