A lateral field non-binary split weighted capacitor array based on fractal curve for SAR ADC

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Abstract: A non-binary split-type MOM weighted capacitor array based on fractal geometry for SAR (Successive Approximation Register) ADC is proposed. By taking advantage of the geometric characteristics of the Hilbert curve, the capacitor array avoids the use of complex common-centroid structure and complex wiring. The test results of the SAR ADC using this capacitor array show that, the measured DNL and INL were -0.26/0.38 LSBs and -0.37/0.38 LSBs, respectively. The ENOB is 8.66 bits. The SAR ADC was implemented using a 180-nm CMOS process with a supply voltage of 1.8V. Its active area and power consumption are 330 μm × 1190 μm and 1.89 mW, respectively.

key words: fractal curve, weighted capacitor array, SAR ADC

Classification: Integrated circuits (analog)

1. Introduction

As the core component in SAR ADC, capacitor array has always been a concern for designers. At present, the commonly used capacitors are mainly (metal insulator metal) capacitors and mom (metal oxide metal) capacitors. Lin et al. [1] further proposed a parasitic matching method to reduce unit capacitor size resulting in less area and less power consumption. All of the above work is based on metal insulator metal (MIM) capacitors. However, according to [2] and [3], MIM capacitors require dedicated metal layers and a special insulator layer, which are not available in many standard silicon-based technologies and have high fabrication cost. However, due to the mismatch between mature technology and several femto farads (fF), there are still many designs based on MIM capacitors [4, 5, 6]. Compared with MIM capacitors, there is obviously smaller minimum capacitance limit on MOM capacitors, since their dimensions can be as small as minimum metal width. MOM capacitors also take advantage of lateral electrical fields to achieve smaller area and generally larger capacitance density. In order to achieve such capacitance density, smaller parasitic capacitance and higher speed, in [7-12], MOM capacitance is used as a weighted capacitor array. In order to reduce the error introduced by weight capacitor mismatch, more and more SAR ADCs use non-binary capacitor arrays to provide redundancy for correction errors [4, 7-10, 13, 14]. In order to reduce the overall capacitance value and the total number of capacitors per unit, the split capacitor array becomes a capacitor array commonly used by many SAR ADCs [5, 6, 13, 15, 16], which connects different groups of capacitors with series capacitors. However, from the existing literature, non-binary split array ADC using MOM capacitor has not been reported.

In this paper, a split structure non-binary MOM weighted capacitor array for SAR ADC is designed based on fractal geometry. Use the proposed design method the capacitor array avoids the using of complex common-centroid structure and complex wiring, so that a reduction in the stray capacitance can be achieved.

2. Proposed Fractal Capacitor Array

Fractal geometry has been widely studied in the existing literature, especially in the field of chip design [17-19], transducers [20], transformers [21-23], couplers [24], transmission lines [25], and capacitors [3, 26-31]. Among them, the capacitors using fractal design are usually used in microwave liquid crystal tuning capacitors, radio frequency circuits and MEMS fields. The case of weighted capacitor array applied to SAR ADC has not been reported. There are many curves used in fractal design, such as the piano curve [26-28], the Moore curve and the Hilbert curve [34]. The Hilbert curve is a continuous curve that traverses all the points in a square and, through multiple iterations, has an infinite length over a finite area. As shown in Fig. 1, the first three Hilbert curves can traverse the whole square, but the square is not divided into two unconnected parts. Therefore, we need to modify the curve to segment the upper and lower plates of the capacitor from a square of limited area with the modified Hilbert curve. Taking the third-order Hilbert curve as an example, the starting two ends of the Hilbert curve are extended to the bottom edge of the square at the same time and connected, thus dividing the square into red and white parts as the top and bottom plates of the capacitor, as shown in Fig. 2.

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Hilbert curve in a finite area is also limited. The minimum size of capacitance of different orders can also be determined by the line width and spacing in a particular process. According to the definition of the Hilbert curve, for the n-order Hilbert curve, the unit squares are averaged out to be $2^n$ and the side length are $c_{sn}$, the curve traverses the center of all the small squares, as shown in Fig. 4. As the $c_{sn} = 2 \cdot \Delta W + \Delta S$, as due to $\Delta W = \Delta S$, then as, $c_{sn} = 3 \cdot \Delta W$, $c_n = 2^n \cdot c_{sn}$ and there

$$c_n = 3 \cdot 2^n \cdot \Delta W$$  \hspace{1cm} (4)

where, $c_n$ is the side minimum length of n-order square capacitor. When the side length of the highest order capacitor is determined according to $\Delta W$, the square side length of other orders and the coordinates of Hilbert fill curve are scaled up to meet Eq. (1).

Since the Hilbert curve consists of a straight edge and a corner, the capacitance value of the fractal capacitor can be expressed as:

$$C = \sum_i \Delta C_i + \sum_j \Delta C'_j$$  \hspace{1cm} (5)

where, $\Delta C_i$ unit length $\Delta l$ gap capacitance value, $\Delta C'_{ij}$ is the gap corner capacitance value.

As shown in Fig. 5, since the spacing at the corner will increase, $\Delta S' > \Delta S$. The capacitance of the capacitor is inversely proportional to the distance between the plates, so...
the capacitance at the corner is less than that at the non-corner, \( \Delta C' < \Delta C \). According to the properties of Hilbert curve, the recursive relationship between the number of turning angles and the order \( n \) can be concluded:

\[
N_{\text{cor}}(1) = 2,
\]

\[
N_{\text{cor}}(n) = \begin{cases} 
4 \cdot (N_{\text{cor}}(n-1) + 2) - 2, & n \text{ is even} \\
4 \cdot N_{\text{cor}}(n-1) - 6, & n \text{ is odd}
\end{cases} \quad (6)
\]

Assuming that the acting length of the capacitance at the corner of the curve is equal to the width of the gap, i.e. \( \Delta l' = \Delta s = \Delta w \). We can figure out the acting length of the corner of the Hilbert curve of \( n \)-order \( l'_n = N_{\text{cor}}(n) \cdot \Delta w \). It can be calculated from Eq. (1) that the length of the \( n \)-order Hilbert curve is \( l_n = 2^n \cdot c \), where \( c \) is the side length of the highest order capacitor square determined by Eq. (4). So the ratio of the length of the angular action in the \( n \)-order capacitance in the whole curve can be calculated by \( \Delta w \), as shown in Table I.

| \( n \) | \( l_n(\Delta w) \) | \( N_{\text{cor}}(n) \) | \( l'_n(\Delta w) \) | \( l'_n/l_n \) |
|---|---|---|---|---|
| 1 | 384 | 2 | 2 | 0.0052 |
| 2 | 768 | 14 | 14 | 0.0182 |
| 3 | 1536 | 50 | 50 | 0.0326 |
| 4 | 3072 | 206 | 206 | 0.0671 |
| 5 | 6144 | 818 | 818 | 0.1331 |
| 6 | 12288 | 3278 | 3278 | 0.2668 |

Therefore, Eq. (5) can be expressed as:

\[
C_n = l'_n \cdot \Delta C' + (l_n - l'_n) \cdot \Delta C, \quad n = 1, 2, 3, \ldots \quad (7)
\]

Since, \( \Delta C' < \Delta C \), \( l_n = 2 \cdot l_{n-1} \), there is \( C_n < 2 \cdot C_{n-1} \), which just satisfies the condition of sub-2-radix capacitor array, that is, MOM capacitor constructed with different Hilbert curves can directly constitute the non-binary weighted capacitor array of SAR ADC.

3. Design and simulation of the proposed Capacitor Array

The capacitance of a fractal capacitor by Y-parameters is given by

\[
C = -\frac{\text{Im}(Y_{21})}{2\pi f} \quad (8)
\]

And the Quality factor is given by

\[
Q = \frac{\text{Im}(Y_{11})}{\text{Re}(Y_{11})} \quad (9)
\]

In order to verify that the proposed structure of capacitor array can support a variety of integrated circuit manufacturing processes, finite element analysis was performed on the capacitors designed for the 180nm CMOS process and 28nm CMOS process, respectively.

The simulation results of capacitance are shown in Fig. 6

![Fig. 6. Simulation capacitances and Q values of the proposed fractal capacitors](image)

According to the simulation results, the capacitance values of each order obtained by simulation at 10MHz are shown in Table II:

| order | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| \( \omega \) | 32.412 | 60.004 | 111.51 | 206.11 | 387.02 | 648.61 |
| \( \omega \) | 1.000 | 1.852 | 1.857 | 1.848 | 1.878 | 1.676 |
| \( \omega = 10 \text{MHz} \) | 6.5604 | 12.163 | 22.821 | 42.366 | 79.124 | 135.08 |
| \( \omega = 10 \text{MHz} \) | 1.000 | 1.854 | 1.876 | 1.856 | 1.868 | 1.707 |

* In 180 nm process, ** In 28 nm process

In 180 nm CMOS process, when the action frequency is less than 3GHz, the capacitance values of different orders of capacitors maintain a relatively stable proportional relationship, and in 1-order to 5-order capacitors, the ratio of the adjacent two capacitance values is maintained at about 1.85, which can provide calibration redundancy for the mismatch of no more than 5% [35]. In 180 nm process, the capacitance value of the 6-order is 648.61fF and the area is \((53.76 \times 53.76) \mu m^2\). Compared with the design method provided in literature [33] and literature [31], higher capacitance density is obtained under the same process conditions. In the 28nm CMOS process, the proposed structure shows a stable proportional relationship as in the 180nm CMOS process, and this stable proportional relationship extends to higher frequency band.

Besides the capacitance values, the Self Resonant Frequency is an important factor for the on-chip capacitors.
The impedance of capacitor becomes inductive if the operational frequency exceeds the Self Resonant Frequency. It can be seen from the simulation results that in 180 nm process the self-resonance frequency of each capacitor is greater than 20 GHz, the self-resonance frequency is higher with the 28 nm process, which can meet the requirements of high-speed ADC design.

Two groups of LSB and MSB are composed of MOM capacitor units of order 1~5, and these two groups of capacitors are coupled by $C_{series}$ capacitor to form Splits capacitor array, as shown in Fig. 7. Where $C_{series}$ is the series proportional capacitor, by adjusting the shape of the curve, the weights of LSB segment and MSB segment are matched.

![Fig. 7. Structure of weighted capacitor array](image)

The capacitor array is simulated by finite element method, and the potential of the top plate of MSB segment is calculated when the bottom plate of each weighted capacitor is connected to $V_{ref}$, as shown in Fig. 8, Table III and Table IV after normalization:

![Fig. 8. Electrostatic simulation of capacitor array.](image)

According to Table III, and Table IV, $\log_2 582.25 = 9.16 > 9$, $radix \approx 1.86$, $\log_2 601.72 = 9.23 > 9$, $radix \approx 1.87$, meet constitute a resolution of the calibrated for 9-bit sub-2-radix SAR ADC the basic requirement of the ADC. In 180 nm process, the total DAC capacitance equals $757.68 \, \text{fF}$, the total load of $769.21 \, \text{fF}$ for the DAC, the parasitic capacitance is less than $2 \, \text{fF}$, and the parasitic capacitance is about $2\%$ of the total capacitance. As shown in Table V, compared with the traditional structure in [11], the proposed structure has outstanding advantage in parasitic capacitance suppression.

### Table III. The normalized weight value and radix of each weighted capacitor in 180 nm

| Bit | 0 | 1 | 2 | 3 | 4 | 5 |
|-----|---|---|---|---|---|---|
| Weight | 1.00 | 0.99 | 1.88 | 3.53 | 6.51 | 11.95 |
| radix | 1.00 | 0.99 | 1.89 | 1.88 | 1.85 | 1.84 |
| Bit | 6 | 7 | 8 | 9 | 10 | Sum |
| Weight | 22.36 | 42.24 | 79.35 | 146.61 | 265.82 | 582.25 |
| radix | 1.87 | 1.89 | 1.88 | 1.85 | 1.81 |

### Table IV. The normalized weight value and radix of each weighted capacitor in 28 nm

| Bit | 0 | 1 | 2 | 3 | 4 | 5 |
|-----|---|---|---|---|---|---|
| Weight | 1.00 | 0.99 | 1.84 | 3.45 | 6.54 | 12.39 |
| radix | 1.00 | 0.99 | 1.86 | 1.88 | 1.89 | 1.89 |
| Bit | 6 | 7 | 8 | 9 | 10 | Sum |
| Weight | 23.12 | 42.75 | 79.91 | 149.43 | 280.30 | 601.72 |
| radix | 1.87 | 1.85 | 1.87 | 1.87 | 1.88 |

### Table V. Performance summary of DAC Capacitor Array

| Structure | Parallel stacked wires [11] | Proposed fractal structure |
|-----------|----------------------------|---------------------------|
| Technology | 90 nm | 180 nm | 28 nm |
| Total capacitance | $777 \, \text{fF}$ | $769.21 \, \text{fF}$ | $159.6 \, \text{fF}$ |
| DAC capacitance | $126 \, \text{fF}$ | $757.68 \, \text{fF}$ | $158.7 \, \text{fF}$ |
| Parasitic capacitance | $251 \, \text{fF}$ | $< 2 \, \text{fF}$ | $< 1 \, \text{fF}$ |
| Common-centroid | Yes | No | No |
| Interconnect parasitics | Serious condition | almost none | almost none |

### 4. Chip Implementation and measurement results of the SAR ADC with proposed Capacitor Array

The SAR ADC using proposed Array uses a charge redistribution scheme, that is, the weighted capacitance is also the sampler holding capacitance. The weighted capacitor array uses a split structure to reduce the value of the total capacitance. The CDAC schematic diagram is shown in Fig. 9:

![Fig. 9. The CDAC schematic diagram of the Prototype ADC with proposed Capacitor Array](image)

The 9-bit 5-MS/s SAR ADC with proposed lateral field non-binary weighted capacitor array based on fractal curve was implemented by using a 180 nm CMOS process with a
supply voltage of 1.8V. Its active area and power consumption are 330 μm × 1190 μm and 1.89 mW, respectively. The size of capacitor array is 650μm × 60μm, as shown in Fig. 10.

![Die micrograph of Prototype ADC with proposed Capacitor Array](image)

Fig. 10. Die micrograph of Prototype ADC with proposed Capacitor Array

In the case of non-calibration, differential nonlinearity (DNL) and integral nonlinearity (INL) measured are shown in Fig. 11, are +0.56/-1 LSBs and +2.66/-2.72 LSBs. Analyzing the curve of DNL, it can be found that the capacitor array indeed conforms to the characteristics of sub-2-radix [14]. According to the algorithm provided in literature [14], the normalized weight value of each weight capacitor are obtained as shown in Table VI:

| Bit | 0   | 1   | 2   | 3   | 4   | 5   |
|-----|-----|-----|-----|-----|-----|-----|
| Weight | 1.00 | 1.00 | 1.83 | 3.45 | 6.17 | 11.17 |
| radix | 1.00 | 1.00 | 1.83 | 1.88 | 1.78 | 1.80 |
| Bit | 6   | 7   | 8   | 9   | 10  | Sum |
| Weight | 21.12 | 38.44 | 70.29 | 129.89 | 234.80 | 519.15 |
| radix | 1.89 | 1.81 | 1.83 | 1.85 | 1.85 | 1.81 |

Table VI. The normalized weight value and radix of each weighted capacitor calculated by the algorithm in literature [14]

After correcting the output results, DNL and INL were -0.26/0.38 LSBs and -0.37/0.38 LSBs, respectively. Sinusoidal signals of 50 kHz and 2.4 MHz were the ADC input under low-frequency test and Nyquist frequencies test, respectively. After calibration, SFDR values were 61.71dB and 58.82dB, SNDR values were 53.91 dB and 52.81 dB, ENOB values were 8.66 bits and 8.48 bits, respectively, as shown in Fig. 12.

![Measured dynamic performances SAR ADC with the proposed capacitor array](image)

Fig. 12. Measured dynamic performances SAR ADC with the proposed capacitor array (a) f_in = 50 kHz  (b) f_in = 2.4 MHz.

5. Conclusion

In this letter, a sub-2-radix (radix 1.85) array base on Hilbert curves for SAR ADC is designed to offer calibration redundancy for the capacitance mismatch errors less than 5%. By employing the geometric characteristics of the Hilbert curve, the sub-2-radix array is constructed without complicated wiring, with reduced parasitic capacitance, and with a wide frequency range to ensure the relative stability of the ratio of different weight capacitors. Experimental results from ADC showed that the measured DNL and INL after calibration were -0.26/0.38 LSBs and -0.37/0.38 LSBs, respectively, SFDRs at low frequency and Nyquist frequencies were 61.71dB and 58.82dB, SNDRs were 53.91dB and 52.81dB, and ENOB were 8.66 bits and 8.48 bit, respectively. The 9-bit SAR ADC with proposed weighted capacitor array based on fractal curve was implemented by 180-nm CMOS technology with a supply voltage of 1.8V. Its active area and power consumption are 330 μm × 1190 μm and 1.89 mW, respectively.

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