STUDY OF NANOWIRE CHARACTERISTICS OF A JUNCTIONLESS TRANSISTOR DEPENDING ON THE GATE LENGTH

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INTRODUCTION

- Following the trends for constant increase of performance, power efficiency, and miniaturization of microelectronic devices we are reaching the limits of conventional technologies: short-channel effects and phenomena as well as manufacturing challenges.

- To surmount the above limitations new device structures and new materials are being developed and implemented. One representative of the above solutions is the junctionless nanowire transistor invented by J. P. Colinge in 1996.

- This transistor is very perspective because it enables the best possible channel control by the gate and consequently, utmost control of short-channel effects with maintaining compatibility with existing CMOS technology.
JUNCTIONLESS TRANSISTOR

- The transistor is junctionless because its channel is a nanowire.
- The current in the channel is controlled by the gate voltage applied over the nanowire.
- The nanowire is highly doped to enable enough carriers for the channel current when the device is on and the nanowire is thin to enable full depletion of carriers when the device is off; depletion is caused by the work-function difference between the gate and the doped Si.
- This transistor structure has IV characteristics similar to conventional MOS transistors with applications as amplifiers, logic gates and sensors.
Technology modeling of junctionless transistor structures is carried out in commercial software suits such as COMSOL, Synopsis Sentaurus, etc.

These models are based on the equations of Poisson and Boltzmann.

The research focus so far is mainly on the impact of channel thickness and channel width upon charge distribution and carrier concentration. These concentrations shape the $IV$ characteristics of the transistor. Furthermore, the impact of the randomly distributed dopant in the nanowire is also studied.

Junctionless transistors (JLTs) are very prospective for sensor applications. For instance, by functionalizing the surface of the gate of a JLT, the JLT can be used for a sensor of presence of certain molecules in the ambient air. The large surface-to-volume ratio of nanowires means that trapping of molecules on their surface can effectively modulate the carrier distribution over the entire channel, making these devices highly sensitive. In addition, decreasing the size of the nanowire reduces the capacitances and enables shorter time responses.

The influence of the charge distribution along the nanowire over the $IV$ characteristics of the junctionless transistor is not well enough studied. In this paper we investigate the influence of the channel length (under the gate) upon the charge distribution and carrier concentration in the nanowire.
We constructed a simplified 3D model of the junctionless transistor consisting of highly doped Si-nanowire covered with SiO$_2$ layer with software defined terminals of source, drain and gate. In all simulations we have constant thickness, length and width of the nanowire as well as the oxide layer. We vary the gate length along the nanowire.

In our 3D model of the nanowire we are varying the gate length in order to estimate the active device area.

Our model employs the density-gradient theory to account for the effect of quantum confinement in the conventional formulation of the drift-diffusion approximation, at a low computational cost.
Model calculations in TCAD software are based on the finite-element method (FEM). In numerical calculus FEM is handy for numerical solution of partial differential equations. These equations describe the dynamics of modeled structures. In our model we take into account the density-gradient effective mass tensor of the charge carriers.

Our objective is to obtain the DC characteristics and the electron density along the transverse and longitudinal center-lines of silicon nanowire. The quantum confinement effect for the SiO2 interface is added by selecting the potential barrier option for the insulator interface boundary condition.
RESULTS AND DISCUSSION

- We modeled characteristics of a nanowire for 7 gate lengths: 10, 20, 30, 40, 50, 60, 70 nm.
- For each gate length we set VDS = 0.05 V and we vary VG between 0.1 to 0.8 V.
- A number of parameters such as carrier confinement, effects of parallel and transverse field-dependent mobilities, and carrier scattering due to Coulomb effects, acoustic phonons, impurity doping profile and surface roughness influence the transport process in the active regions.
- The effective mass of a semiconductor is obtained by fitting to a parabola of the actual E-k dispersion diagram around the conduction band minimum or the valence band maximum (the E-k diagram gives the relationship of the energy vs. momentum of available quantum mechanical states for electrons in the material).
We studied the electron concentration along channel width at 3 gate voltages: $V_G = 0.1 \; ; \; 0.3 \; ; \; 0.5 \; V$. The results are compared to [13].

It can be observed that the concentration is of the same order of magnitude for the same gate voltages of $V_G = 0.1 \; ; \; 0.3 \; V$. 
We studied the electron concentration at different values of the longitudinal DG (density gradient) effective mass $f_{mx}$: 0.1, 0.2, 0.3, 0.5 and 0.8.
DRAIN CURRENT VERSUS GATE VOLTAGE

We studied the transfer characteristic of the structure for 4 gate lengths: 10, 30, 50, 70 nm. It can be observed that the drain current decreases with the increase of gate length.

At LG = 10 nm ID is on the order of 10^6 A. At VG = 0.1 V the drain current is on the order of 10^-12 A. The results are juxtaposed to [14].
The inhomogeneity can be clearly seen by comparing Fig. LEFT and Fig. RIGHT, which present the electron concentrations at gate length of 70 nm and 50 nm. This inhomogeneity in charge distribution characteristics could lead to disturbance and erroneous interpretation of sensor data in the event of radical binding to the sensor.
The difference between gate length of 70 nm and 50 nm is even more pronounced in Fig. LEFT and RIGHT. In Fig. LEFT electron concentration “well” is rough and in Fig. RIGH it is smooth.

In Fig RIGHT it can be clearly seen that the depletion area is narrower at 70 nm gate length compared to the depletion area at 20 nm.

Such narrow characteristics do not depend on the gate voltage.

Hence, the gate length of the JLT should be smaller for sensors applications.
CONCLUSION

The developed 3D model of a simple nanowire junctionless transistor is in a good agreement with the models presented by other authors. It demonstrates the quantum confinement effect for the silicon-oxide interface. These effects implemented in the model result in accurate description of transistor behavior. The analysis of the function of electron concentration versus gate length proved that it is desirable to use transistors with as small gate length as possible.

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