Metal organic chemical vapour deposition regrown large area GaN-on-GaN current aperture vertical electron transistors with high current capability

Philipp Doering,1,5 Rachid Diriad,2 Richard Reiner,2 Patrick Waltereit,2 Michael Mikulla,2 and Oliver Ambacher1,2
1 Department of Power Electronics, Albert-Ludwigs University, Freiburg 79108, Germany
2 Fraunhofer Institute for Applied Solid State Physics IAF, Freiburg 79108, Germany
5 E-mail: philipp.doering@inatech.uni-freiburg.de

Introduction: The current aperture vertical electron transistor (CAVET) is a promising candidate for vertical GaN-devices, as it combines the established gate-source module of a lateral high electron mobility transistor (HEMT) and the two-dimensional electron gas (2DEG) at the AlGaN/GaN interface with the benefits of a vertical depletion- and drift-region. Additionally, the peak electric field is buried in the bulk material, which was shown to avoid surface related dispersion [1, 2]. As a result, most of the surface-related fabrication processes of the lateral HEMT are adoptable for CAVETs, without the need of a complex field-plate design. A major challenge in the fabrication of CAVET structures has been the diffusion of Mg from the current blocking layer (CBL), which serves as a potential barrier between source and drain, during the overgrowth of the GaN-channel and the AlGaN-barrier. This has mostly been addressed by molecular beam epitaxy (MBE) regrowth of the GaN-channel, as the lower growth temperature with respect to MOCVD allows for much sharper doping profiles. Small gate width transistors were published fabricated to establish a robust device design with respect to the gate-aperture overlap for a simplified fabrication process. Small gate width CAVETs were fabricated to establish a robust device design with respect to the gate-aperture overlap to ensure gate control in the regrown GaN-channel and to suppress substantial source-drain leakage. Optimized gate-aperture dimensions of the vertical layout are combined with the standard comb structure design and an established gate-source module of the lateral HEMT [6]. As a result, a large area CAVET comb structure demonstrates a chip size of 2 x 2 mm². A maximum drain current of ID_MAX = 20 A is shown in pulsed measurements with a differential on-state resistance of RDSON = 2.15 Ω. The breakdown in this device was measured at VBR = 122 V. The maximum drain current is measured at a drain-source voltage of VDS = 45 V, which accords with a pulse power of I_D = 20 A at a drain-source voltage of VDS = 45 V, corresponding to a power of P = 900 W.

Experimental section: The fabrication of the CAVET structure started with the MOCVD growth of a 2 µm uidd-GaN drift layer (nominally Nd = 5 x 10¹⁶ cm⁻³) on a 2 inch bulk GaN substrate having a thickness of 380 µm. A current blocking layer was formed by Mg-ion implantation at an energy of 100 keV and a dose of 2 x 10¹⁵ cm⁻² (Figure 1a), which is one order of magnitude lower than the dose used in [1], resulting in a peak Mg-concentration of 1 x 10¹⁸ cm⁻³. A 3 µm thick photore sist served as a protection for the aperture region during implantation. The photore sist was removed, the CAVET structure was finally sealed by a planar AlGaN/GaN regrowth with a 25 nm thin barrier and a 250 nm uidd-GaN channel (Figure 1b), to separate the 2DEG from the CBL. The regrowth temperature of about 1050 °C also served as an in-situ annealing of the Mg-implanted CBL without the requirement of a capping layer. The morphology of the final CAVET structure was measured after regrowth by atomic force microscopy (AFM) and revealed a root mean square of RMS = 0.18 nm in a 10 x 10 µm² scan.

The device fabrication is based on standard III-V processing technology. A Ti/AI/Ni/Au metal stack is deposited and alloyed at around 825 °C to form the ohmic source contacts. The devices are then passivated with a SiNx dielectric layer deposited by plasma enhanced chemical vapour deposition (PECVD) and subsequently isolated by Ar-ion implantation. Afterwards, inductively coupled plasma reactive ion etching (ICP-RIE) is used for gate-via opening. Schottky gate contacts are fabricated with an Ni-Au-based metal stack. The surface process is finished by an additional SiNx dielectric layer and a TiPtAu-based interconnection metallization stack. Finally, the drain contact is realized at the backside of the bulk GaN substrate (Figure 1c) with the same aforementioned ohmic metal stack.

Results and discussion: A critical parameter in the design of the CAVET is the gate aperture overlap L_GAP [1] shown in Figure 1d. L_GAP determines the gate control in the device by suppressing source-drain leakage as an in-situ annealing process of the implanted CBL, which allows for a simplified fabrication process. Small gate width CAVETs were fabricated to establish a robust device design with respect to the gate-aperture overlap to ensure gate control in the regrown GaN-channel and to suppress substantial source-drain leakage. Optimized gate-aperture dimensions of the vertical layout are combined with the standard comb structure design and an established gate-source module of the lateral HEMT [6]. As a result, a large area CAVET comb structure demonstrates a chip size of 2 x 2 mm². A maximum drain current of ID_MAX = 20 A is shown in pulsed measurements with a differential on-state resistance of RDSON = 2.15 Ω. The breakdown in this device was measured at VBR = 122 V. The maximum drain current is measured at a drain-source voltage of VDS = 45 V, which accords with a pulse power of I_D = 20 A at a drain-source voltage of VDS = 45 V, corresponding to a power of P = 900 W. The achieved high current handling capability demonstrates the potential of the CAVET technology, in combination with the comb structure design and an industrial MOCVD process for the use in high current/power applications.

Fig. 1 Schematic fabrication process of the GaN-on-GaN CAVETs. (a) Mg-implantation to create the current blocking layer. (b) Planar AlGaN/GaN overgrowth after photore sist removal. (c) Deposition of the metal contacts and dielectric passivation layers. (d) Definition of design parameters.
through the GaN-channel. The required overlap needs to be adjusted with respect to the channel thickness between the CBL and source contact in the fabricated device structure. In order to derive an optimum dimension of the gate-aperture overlap, small gate width CAVETs were fabricated with $L_{GAP}$ ranging between 0 and 2 $\mu$m and a gate width of $W_{G}=100$ $\mu$m. As the product of the aperture length and the doping concentration in the aperture determines the impact of the aperture resistivity on the total device resistance [2], either substantial doping or high aperture length are required. Since high doping of the aperture region and an aperture length of 2 $\mu$m was used in all devices, which was verified by TCAD simulations to have a negligible effect for donor concentrations above $N_D = 1 \times 10^{18}$ $\text{cm}^{-3}$.

Figure 2 exhibits the transfer characteristics of the small CAVETs at a drain-source voltage of $V_{DS}=10$ $V$. The CAVET with a gate-aperture overlap of $L_{GAP}=2$ $\mu$m reveals a threshold voltage of $V_{TH}=-2.8$ $V$ with a low leakage current of $4.5 \times 10^{-4}$ $\text{A/cm}^2$ in the off-state. The device presented an $I_{DS}/I_{OFF}$ ratio of $10^5$ with a sub-threshold slope $S_{TH}$ of around 90 $\text{mV/dec}$. Breakdown was measured to be at 282 $V$ at room temperature, corresponding to a critical electric field of $E_C=1.25$ $\text{MV/cm}$ (assuming depletion over the complete gate to drain distance). Similar results were obtained for test structures without an aperture, indicating that the breakdown is related to the current blocking layer. It is also worth noting that, the calculated field strength is higher than published values in [1] (86 $\text{MV/cm}$, 3 $\mu$m drift layer), which demonstrates the suitability of the low dose implantation and the in-situ annealing process during MOCVD overgrowth. A decrease in $L_{GAP}$ to 1 $\mu$m leads to a significant increase in the sub-threshold swing to around 420 $\text{mV/dec}$, while the leakage current increased slightly by half an order of magnitude. Without any gate overlap ($L_{GAP}=0$), the transistor did not turn off, and substantial source-drain leakage could not be suppressed even at high negative $V_{GS}$, which is in agreement with the expected loss in gate control.

With the optimized dimensions of the gate-aperture overlap, a multi-finger transistor with an aperture length of $L_{AP}=10$ $\mu$m, an aperture-gate overlap of $L_{GAP}=2$ $\mu$m, an aperture width of $W=58 \times 1.32 = 77$ $\text{mm}$ (number $\times$ width) and an active finger area of $1.85 \times 1.32$ $\text{mm}$ was subsequently fabricated and characterized. The total chip, including gate and source pad, has an area of $2 \times 2$ $\text{mm}^2$. The transfer characteristics of the large device is shown in Figure 3a. I was measured in wafer measurements up to a constant current of 1 $A$ (high power source measurement unit, Keysight-B1505A). As the current compliance is exceeded in the on-state above $V_{GS}=-2$ $V$, the transfer characteristics are only shown up to $V_{GS}=-1.8$ $V$. The CAVET exhibits a threshold voltage of $V_{TH} = -2.8$ $V$ similar to the small gate CAVET. However, the sub-threshold slope increased for the large device to around $S_{TH}=140$ $\text{mV/dec}$, when compared to the small CAVET test structures, indicating less gate control in the GaN-channel in the large device. In addition, the large area device reveals an off-state current in the range of $5 \times 10^{-5}$ $\text{A/cm}^2$, which is two orders of magnitude higher, when compared to the small CAVETs.

Breakdown was measured to be at 122 $V$ at room temperature, as shown in Figure 3b. It is assumed that the reduction in voltage robustness and the increase in leakage current and sub-threshold slope is attributed to the reduction in yield over the large device. The pulsed output characteristics (pulsed width $= 500$ $\mu$s) of the fabricated comb structure are shown in Figure 4 for $V_{GS}$ from $-5$ to $+3$ $V$. A maximum drain current of 20.1 $A$ was measured at $V_{GS} = 3$ $V$. The inset shows a top-view image of the multi-finger comb structure by scanning electron microscopy.

**Figure 2** Transfer characteristics of small CAVETs with varying $L_{GAP}$ of 0, 1 and 2 $\mu$m at $V_{DS}=10$ $V$. $V_{GS}$ is varied between $-5$ and $0$ $V$. All devices feature an aperture length of $L_{AP}=10$ $\mu$m, $W_{G}=100$ $\mu$m and an active device length of $L_{ACT} = 32$ $\mu$m (including both source contacts). The gate lines show the impact of reduction in $L_{GAP}$ on the $I_{DS}/I_{OFF}$ ratio and the $S_{TH}$.

**Figure 3** Transfer and off-state characteristics of the large area CAVET. (a) Transfer characteristics at $V_{GS} = −10$ $V$. $V_{DS}$ is varied from off-state at $−5$ $V$ to on-state $V_{TH}=1.7$ $V$ at $L_{DS}=1A$, which is the maximum current of the used curve tracer. The device revealed a $V_{TH} = −2.8$ $V$ and a $S_{TH}=140$ $\text{mV/dec}$. (b) Corresponding off-state characteristics at $V_{GS} = −5$ $V$ with $V_{BR}=122$ $V$.
in the nominally undoped aperture and drift region. Hall measurements of the AlGaN/GaN heterostructure revealed a sheet carrier concentration of $n_S = 8 \times 10^{12} \text{ cm}^{-2}$ and a carrier mobility of $\mu = 1380 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Thus, a high compensation of the 2DEG by Mg-diffusion can be ruled out. Similar on-state resistances can be reproduced in TCAD simulations, when the donor concentration in the aperture and drift region are reduced below $N_D < 1 \times 10^{16} \text{ cm}^{-3}$, which further supports the assumption of donor compensation. Aperture and drift region compensation might be caused by carbon but a partial depletion of the aperture region, due to the mentioned lateral pn-junction cannot be ruled out to cause additional series resistance.

In Table 1, we compare the achieved characteristics to the relatively limited data on CAVETs, regarding active area, current density, absolute current and breakdown voltage. It can be clearly seen that, in contrast to our investigation, most of the studies reported only small CAVET devices, which resulted in limited absolute drain currents.

Additionally, the breakdown voltage in the published devices has been a critical issue, due to very high leakage currents [2–4], which was successfully addressed in this work. However, the results of our large CAVETs indicate a reduction in current density $J$ when compared to results of small CAVETs published in [1, 2, 4]. Thus, we believe that further optimization in AlGaN barrier layout, n-type doping concentration of the aperture region and process technology will push its performance beyond its lateral counterpart. Moreover, increasing the drift layer thickness in the CAVET structure will be essential for higher voltage sustainability and thus power handling capability to reveal the full potential of this device design.

Table 1. Published CAVETs and their channel regrowth technique, gate width $W_G$, length of the active device area $L_{ACT}$, current density $J$, absolute drain current $I_D$ (*calculated from $I$ and $W_G \times L_{ACT}$) and breakdown voltage $V_{BR}$

| Ref | Technique | $W_G$ [µm] | $L_{ACT}$ [µm] | $J$ [kA/cm$^2$] | $I_D$ [A] | $V_{BR}$ [V] |
|-----|-----------|-------------|--------------|----------------|----------|----------|
| [1] | MBE       | 75          | 22           | 3.8            | 0.063    | 220      |
| [2] | MBE       | 75          | –            | 10.9           | –        | –        |
| [3] | MOCVD     | 200         | 33           | 0.19           | 0.018    | –        |
| [4] | MBE       | 54          | –            | 4              | –        | –        |
|     | MOCVD     | 1320        | 1850         | 0.84           | 20.1     | 122      |

This work - MOCVD 1320 1850 0.84 20.1 122

Conclusion: In this work, a CAVET is presented using Mg-implantation and MOCVD growth, without the need of post annealing and MBE regrowth. A large area CAVET comb structure is achieved by combining the proven gate-source module of an HEMT structure with the vertical transistor design. The device exhibited a maximum drain current of 20.1 A, and a total on-state resistance $R_{ON} = 2.15 \text{ Ω}$. The presented high power density structure demonstrates the potential of this CAVET design for high current applications.

Acknowledgments: This work was supported by the Deutsche Forschungsgemeinschaft (DFG) under grant AM 105/47-1. Financial support by the Fraunhofer society through the “VERTIGO” grant is greatly acknowledged.

Open access funding enabled and organized by Projekt DEAL.

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Received: 4 November 2020 Accepted: 19 December 2020
doi: 10.1049/ell2.12068

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