Optimization of thermal oxidation for 4H-SiC and fabricate/characterize MOS capacitor

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Abstract. On the 4H-SiC substrate, C-face and Si-face oxide layers have been grown by thermal oxidation process and sputtering. The thermal oxidation temperature dependence of 4H-silicon carbide (SiC) is systematically investigated using capacitance-voltage (C–V) measurements. The oxidation quality and thickness vary according to the temperature and time duration of the thermal oxidation. The layers’ thicknesses are determined by atomic force microscopy (AFM), and the temperature range is between 800 °C and 1110 °C. The primary reason to fabricate the Metal-Oxide-Silicon (MOS) capacitor is to know the thermal oxidation process and a working principle. In this paper, we optimize a thermal oxidation process and fabricate the MOS structure. Then we determine the various parameters such as flat band voltage ($V_F$), Inversion threshold voltage ($V_{th}$), Surface depletion capacitance ($C_{dep}$), Oxide capacitance ($C_{ox}$), the total capacitance of the device ($C_t$), doping concentration ($N_d$), Depletionwidth ($X_d$), Maximum depletion width ($X_{ox}$) and Interface trap density ($D_{it}$). Finally, we analyze and discuss the MOS capacitance.

Keywords- Fabrication, Thermal oxidation, Sputtering, Capacitance-voltage (C–V) measurements.

1. Introduction

In VLSI Technology, semiconductors can be oxidized by different methods like, e.g., plasma-enhanced chemical vapor deposition (PECVD), electrochemical anodization, and thermal oxidation. To grow top-quality oxide (SiO$_2$) layer on a Si wafer, various grown methods exist, and continuous research is going on. Thermal oxidation is a way the foremost importance for device fabrication. Same as the Si-technology, Silicon Carbide (SiC) is a single compound semiconductor that is thermally oxidized in the form of SiO$_2$. This suggests that we will directly try to the enlargement of SiC-Technology.

Several researchers and various groups are exceptionally performing on the growth mechanism of SiO$_2$ on the SiC substrate surface beside the Si growth mechanism. Since a compound semiconductor, SiC material having Si and C atoms, C atoms’ character is detected to be very critical during the thermal growth of the SiO$_2$. Several experiments [7–9] verify that the MOS-structure interface and dielectric
properties are directly affected by the availability of the C species during the thermal grown oxidation [10]. To understand and control the electrical characteristics of the SiC-based device, the nature of thermally grown SiO$_2$ on SiC wafer plays an important role; this is one reason various researchers rigorously work in this area. According to the reports, the comparison with the Si substrate growth rate of oxide on the SiC substrate is much lesser [11-13]. In equivalent oxidation condition speed of reaction on the Si-wafer is far faster than of SiC-wafer.

It has been also noted that a remarkable phenomenon occurred that the face termination oxidation on SiC substrate surfaces, which indicates that different oxidation thickness has on both the polar faces (Si and C face). This thickness, quality of oxidation layer, and oxidation rate change upon the polytypes and crystal orientation of SiC.

The metal-oxide-semiconductor (MOS) structure is the core of MOS technology. MOS structure (customarily known as a MOS capacitor) is connected as a two-terminal device, with one electrode connected to the metal and, therefore, the other electrode attached to the semiconductor. As a result, the voltage-dependent capacitance characteristic is drawn. During this paper, we first consider constructing a MOS capacitor then drawn the capacitance-voltage (C-V) relationships, which can utilize in the development of the MOS transistor model [26].

2. **4H-SiC substrate Specification**

| Parameter                              | Value                                           |
|----------------------------------------|-------------------------------------------------|
| **Substrate**                          |                                                 |
| Substrate diameter                     | 3 inches                                        |
| Substrate material                     | SiC-4H single crystal wafer                     |
| Substrate wafer orientation            | 0001 with 4-degree off axis                     |
| The thickness of the substrate wafer   | 350 $\mu$m                                      |
| Substrate face                         | Silicon Face                                    |
| Substrate doping type                  | n-type                                          |
| Resistivity of substrate               | 0.015-0.028 $\Omega$ cm                        |
| Polishing of substrate                 | Chemo Mechanically Polished, Double side polished |
| Micro-pipe density in substrate        | $\leq 1/cm^2$                                   |
| **Epilayer 1 (buffer layer)**          |                                                 |
| Epilayer 1 doping type                 | n-type                                          |
| Epilayer 1 doping density              | $10^{18}$/cc                                    |
| Epilayer 1 thickness                   | 1 $\mu$m                                       |
| **Epilayer 2**                         |                                                 |
| Epilayer 2 doping type                 | n-type                                          |
| Epilayer 2 doping density              | $8\times10^{14}$/cc                             |
| Epilayer 2 thickness                   | 50 $\mu$m                                      |

**Figure 1.** The schematic picture of quarter pieces of 4H-SiC substrate.
M/s CREE Research Inc USA provides the Single crystalline SiC-wafer. In our paper, an n-type 4H-SiC material was with small doping concentration and the epitaxy layer thickness (50 µm) on Si-face.

3. Thermal oxidation Furnace
The thermal oxidation furnace was used for the thermal growth of SiO2 on the 4H-SiC substrate, as shown in figure 3. It is usually contained of following parts: heating zone (consists of several heating coils), measurement system, cabinet, temperature controller, horizontal quartz tubes (the place where the wafers experience oxidation), loading station (used for loading or unloading) wafers into (or from) the process tubes and a gas flow meter (for observing used gases flow into and out from furnace). There are mainly three quartz tube heating zones, i.e., left-hand, right-hand, and middle. The temperature 4000±500 °C was fixed for the left-hand and right-hand zone at the complete process. There is three digital control system to increase and decrease the furnace temperature for all three different zones. The furnace is having two gas pipelines and one gas flow controller (MATHESON’s). Too pure DI-water has been produced by quartz bubbler, and the temperature of the bubbler can be controlled by heating metal. In the quartz furnace, various gases (Wet O2/dry O2 or dry N2) have been passed with the help of a quartz nozzle [27].

4. Cleaning process of the wafer
The SiC wafer clean-up technique is the same as Silicon, and all substances utilized in the wet-chemical process remained MOS grade. The SiC-wafer was a three-step chemical cleaning method like the Si-wafer, i.e., Degreasing, the standard Radio Corporation of America (RCA), and Piranha. Degreasing has three clean-up stages. In the first stage, to remove grease particles from the wafer’s surface, wafers were dropped and boiled for 10 minutes in Trichloroethane (TCE). In the second stage, to remove light metal ions or particles, the wafers were dropped and boiled for 10 minutes in acetone. In the third stage, the wafers were dropped and boiled for 10 minutes in methanol. Finally, with the help of de-ionized (DI) water, the wafers were cleaned.

The standard Radio Corporation of America (RCA) clean-up method has two phases, the first phase is known as standard cleaning-I (SC-I), and the second stage is known as standard cleaning-I (SC-II). In the SC-I at room temperature, the wafers were dipped for 10 min in a high pH alkaline mixture (NH4OH/H2O2/DI-water) within the relative amount of (1:1:5). SC-I is employed to remove the organic substances on the wafer, exposing the surface and remove hydrous oxide film. Then the wafer was clean in DI-water and dipped for one minute in hydrofluoric (HF) acid. The SC-II, at room temperature, the wafer was dipped in a combination of (HCl/H2O2/DI-water) within the relative amount of (1:1:6). Finally, clean in DI-water and with the 10 percent HF solution remove the native oxide. The SC-II cleaning is used to remove water-insoluble hydro oxide compounds, any dual-trace
metals, and alkali ions disrobed by SC-I. The last cleaning treatment is Piranha cleaning. The wafers are
dipped for 15 minutes in piranha solution (H₂SO₄ and H₂O₂ within the ratio of 4:1) to remove any heavy metal resident on the wafer surface. After All, using DI-water, the wafers were clean-up and
dipped in the 10 percent HF. The temperature ranging from 800 °C to 1110 °C was used for thermal
oxidation procedure for various oxidation time. It tried to find the precise performance of thermal
oxidation on both sides of SiC-wafer in both dry and wet oxidizing environments.

5. Oxidation Process
The thermal oxidation process temperature ranges from 800 °C to 1110 °C for different periods for
both the process, as shown in figure 4 and figure 5. The wafers were placed in the middle zone of the
furnace in the boat (quartz glassware), which carries multiple wafers. The oxidant process was started,
and diffusion takes place. In the wet oxidation process, the quartz bubbler’s temperature is always kept at
a constant 850°C. The helical path has controlled the wet molecular oxygen (0.4 LPM) during the
process. The wafers were loaded and

Figure 3. Schematic details 3-inches diameter 4H-SiC Substrate.

Figure 4. Process flow of wet thermal oxidation for 1.5 hour.
unloaded in the 1.9 LPM flow of nitrogen at 800 °C, increasing and decreasing the furnace’s temperature by 5 °C/min, which is shown in Figures 4 and 5. In the first process (figure 4), oxidation (wet oxidation and annealing duration is 1.5 hr each) for 3hrs at 1110 °C and re-oxidation (wet oxidation and annealing duration is 1 hr each) for 2 hr at 950 °C. In the second process, as shown in figure 5, oxidation (wet oxidation and annealing duration is 4 hrs and 1 hr respectively) for 5 hrs at 1110 °C and re-oxidation (wet oxidation and annealing duration is 1 hr each) for 2 hr at 950 °C. The thickness of oxide was measured by the ellipsometry technique with verification of DAKTEK surface profiler on both end faces. The thermally grown oxide layer thickness is found 147.4nm on C-face and 16.4 nm on Si-face (Process flow of wet thermal oxidation for 1.5 hours). The thickness of thermally grown oxide layer oxide is 474.61 nm on C-face and 55.2 nm on Si-face (Process flow of wet thermal oxidation 4 hours). Wet thermal oxidation of 4H-SiC is depended on various conditions such as temperature, pressure, and time.

6. Fabrication of MOS Capacitor
The structure of a MOS capacitor is demonstrated in Figure 6. MOS capacitor consists of the oxide-
coated n-type 4H-SiC wafer. The oxide layer (silicon dioxide SiO$_2$) is grown by thermal oxidation, and after the oxide layer, a conducting layer (Ni) (called a gate) is grown by sputtering. Through a metal defining mask, the gate structure is defined the metal is vaporized on the wafer. The ohmic contact is obtained by evaporating the metal on back (bulk) contact, which is in intimate contact with SiC. Vacuum annealing of 1hrs at 300°C is done before and after contact deposition.

| Table 2. Specification of parameter |
|-------------------------------------|
| Vacuum-4x10$^{-7}$ (during deposition) | Thickness-2000Å |
| Thickness-300 Å for Ti | Deposition Rate-1.4 Å/sec |
| -2000 Å for Au | Rev Time-4.5 |
| Deposition rate- 0.4 Å/sec for Ti | Power -100 W (DC) |
| -1.7 Å /sec for Au | Frequency-100kHz |
| Time-24 min for Ti | Argon-7.0 sccm |
| -60 min for Au | RF-13.56 MHz |

The MOS capacitor structure useful for studying the silicon surface, and the appropriate MOS transistors and C-V characteristics are employed to examine IC fabrication method. For this justification, the MOS capacitor as a test device is used to measure HF and LF C-V plots, which measure gate oxide thickness $t_{ox}$, oxide charges and interface-state density $D_{it}$, flat band voltage $V_{fb}$, doping concentration etc. [1]-[3].

**7. Analysis of C-V characteristics**
Across the device, by applying the dc bias from -40 V to 1 V at 1 MHz frequency, the C-V characteristics were measured using a 4284A LCR meter. Through the LabVIEW software, data has been carried out through computer-aided measurement facilities. As shown in figure 8, the characteristics of the fabricated structure of applied voltage with capacitance at a different frequency, and figure 9 show the different voltage and $1/C^2$. Various parameters have been calculated by applying appropriate equations with the help of the drawn C-V characteristics. Characteries the MOS capacitor and find the various parameter like flat band voltage $V_{fb}$.

![Figure 7. Fabricated Final Device](image_url)
Figure 8. Measured characteristic curves of applied bias voltage vs. capacitance at a different frequency.

Figure 9. Applied Voltage vs $1/C^2$.

1.09V, Inversion threshold voltage $V_{t}$, 2.66 V, Surface depletion capacitance $C_{dep}$, 68.67 nF/cm², Oxide capacitance $C_{ox}$, 115 nF/cm², Total Capacitance of the device $C = 0.7482 \times 10^{-18}$ F, doping concentration $N_D = 7.69 \times 10^{14}$ CC, Depletion width $X_d = 1.37 \times 10^{-4}$ cm, Maximum depletion width $X_{dt} = 1.937 \times 10^{-4}$ cm and Interface trap density $D_{it} = 3.6 \times 10^{-9}$ states/cm² are calculated.

8. Conclusions
This paper represents an optimized 4H-SiC thermally grown oxide mechanism through an
experiment. Based on experimental results achieved, various conclusions have been discovered, such as A face terminated oxidation performance has been studied, which suggests that the oxidation growth rate on Si-face is slower than C-face. In the wet oxidation, Si-face oxide thickness is 8 to 12 times slower than the C-face. Finally, we successfully fabricated and characterized the MOS capacitor and found the device’s various related parameters.

Acknowledgments

The authors would like to thank all the Semiconductor Device Design Group staff members for their enormous support during the batch fabrication of diode structures. The authors are thankful to Director CSIR-CEERI for his continuous support and encouragement. Financial support from DRDO through project no CLP 6555 is acknowledgeable.

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