Memory Window and Endurance Improvement of Hf$_{0.5}$Zr$_{0.5}$O$_2$-Based FeFETs with ZrO$_2$ Seed Layers Characterized by Fast Voltage Pulse Measurements

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Abstract

The HfO$_2$-based ferroelectric field effect transistor (FeFET) with a metal/ferroelectric/insulator/semiconductor (MFIS) gate stack is currently being considered as a possible candidate for high-density and fast write speed non-volatile memory. Although the retention performance of the HfO$_2$-based FeFET with a MFIS gate stack could satisfy the requirements for practical applications, its memory window (MW) and reliability with respect to endurance should be further improved. This work investigates the advantage of employing ZrO$_2$ seed layers on the MW, retention, and endurance of the Hf$_{0.5}$Zr$_{0.5}$O$_2$ (HZO)-based FeFETs with MFIS gate stacks, by using fast voltage pulse measurements. It is found that the HZO-based FeFET with a ZrO$_2$ seed layer shows a larger initial and 10-year extrapolated MW, as well as improved endurance performance compared with the HZO-based FeFET without the ZrO$_2$ seed layer. The results indicate that employing of a direct crystalline high-k/Si gate stack would further improve the MW and reliability of the HfO$_2$-based FeFETs.

Keywords: HfO$_2$-based FeFET, Memory window, Retention, Endurance, ZrO$_2$ seed layer

Background

HfO$_2$-based ferroelectric thin films are considered as promising gate-stack materials for ferroelectric field effect transistors (FeFETs) because of their complementary metal-oxide-semiconductor (CMOS) compatibility and scalability. Among several kinds of gate stack structures that can be used in FeFETs, a metal/ferroelectric/insulator/semiconductor (MFIS) represents a more practical configuration because it follows the current MOS device architectures and matches well with the modern high-k metal-gate (HKMG) processes. Therefore, great efforts have been made to design and fabricate FeFETs with MFIS gate stack structures for applications in embedded nonvolatile memories, negative capacitance field effect transistors, artificial neurons, synapses, and logic-in-memory devices [1–8].

Up to now, high-density and fast write speed FeFETs with MFIS gate stack structures have been successfully fabricated using HKMG processes [9, 10]. In addition to the high integration density and fast write speed, a large memory window (MW) and a high reliability with respect to retention and endurance are also critical for employing FeFETs for nonvolatile memory applications [11–14]. Owing to a large band offset to silicon, a high coercive field and a moderate dielectric constant of the HfO$_2$-based ferroelectric thin films, HfO$_2$-based FeFETs with MFIS gate stack structures exhibit reliable retention properties (10-year extrapolation) [15–17]. However, although the HfO$_2$-based thin films demonstrate moderate endurance over $1 \times 10^8$ switching cycles [14, 18], HfO$_2$-based FeFETs with MFIS gate stack structures have a rather limited endurance ranging from $1 \times 10^4$ to $1 \times 10^7$ switching cycles [17, 19–23]. Theoretically, employing of high-k insulator layers is expected to...
reduce the electric field in the MFIS gate stack, which would alleviate the band bending, thereby improving the endurance properties and the MWs of the HfO$_2$-based FeFETs [12, 14]. Experimentally, Ali et al. verified that increasing the $k$ value of the ultrathin insulator layer (i.e., using SiON instead of SiO$_2$) can effectively improve the endurance properties as well as the MW of the HfO$_2$-based FeFETs [13]. In our previous research [24], we reported that the insertion of a crystalline ZrO$_2$ high-k layer in the MFIS gate stacks could improve the crystalline quality and suppress the formation of monoclinic phase in Hf$_{0.5}$Zr$_{0.5}$O$_2$ (HZO) thin films, which leads to a large MW of 2.8 V characterized by DC voltage sweep method.

In this work, we report on the characterization of the MWs, retention, and endurance of the HZO-based FeFETs with and without crystalline ZrO$_2$ seed layers by using fast positive and negative voltage pulse measurements. Moreover, the advantage of employing crystalline ZrO$_2$ seed layers on the MW and endurance properties is discussed.

**Methods**

The n-channel FeFETs with and without ZrO$_2$ seed layers were fabricated using a gate last process, as described in [24]. The ZrO$_2$ seed layer and the HZO layer were both grown at a growth temperature of 300 °C by atomic layer deposition (ALD). The schematic of the fabricated FeFETs is shown in Fig. 1a, whose channel width ($W$) and length ($L$) were 80 and 7 µm, respectively. Meanwhile, TaN/HZO/TaN and TaN/HZO/ZrO$_2$/TaN capacitors were also fabricated to evaluate the ferroelectric properties of the HZO thin films. The polarization–voltage ($P$–$V$) hysteresis loops of the capacitors were measured using a Radiant Technologies RT66A ferroelectric test system, while the device characteristics of FeFETs were measured by an Agilent B1500A semiconductor device analyzer with a pulse generator unit (B1525A) [20]. Two main test sequences used for MW and endurance measurements are shown in Fig. 1b and c. For MW and retention measurements, program/erase (P/E) pulses were first applied to the gates of FeFETs, and read operations were performed at different time intervals using $I_D$–$V_D$ sweep ($V_D$ = 0.1 V) to sense $V_{TH}$. Generally, $V_{TH}$ is determined as a gate voltage corresponding to a drain current of $10^{-7}$ A·W/L [25], and the MW is defined as the difference of $V_{TH}$ values between programmed and erased states. For endurance measurements, the MW was measured after a certain number of alternating P/E pulses.

**Results and Discussion**

Figure 2a shows the $P$–$V$ hysteresis loops of the TaN/HZO/TaN and TaN/HZO/ZrO$_2$/TaN capacitors. Remarkably, the TaN/HZO/ZrO$_2$/TaN capacitor possesses even better ferroelectric properties than the TaN/HZO/TaN capacitor, which is consistent with the reported results [26], indicating that the crystalline ZrO$_2$ seed layer could indeed improve the crystalline quality and suppress the formation of monoclinic phase in HZO thin films [24]. Figure 2b shows the $I_D$–$V_G$ curves of the HZO-based FeFETs with and without additional crystalline ZrO$_2$ seed layers after P/E pulses. The red symbol lines represent the $I_D$–$V_G$ curves after applying a program pulse of 7 V/100 ns, while the blue symbol lines represent the $I_D$–$V_G$ curves after applying an erase pulse.

**Fig. 1** a Schematic of the fabricated FeFETs. The additional crystalline ZrO$_2$ seed layer is marked by black gridlines. b, c Test sequences used for MW and endurance measurements.
of $-7\, \text{V}/100\, \text{ns}$. One can see that the $I_D-V_G$ curves of both FeFETs show counterclockwise switching characteristics, suggesting that the MWs of the present FeFETs are originated from the polarization switching of the HZO layers, rather than the charge trapping and injection. Nevertheless, the HZO-based FeFET with the additional crystalline ZrO$_2$ seed layer exhibits an improved MW of 1.4 V, approximately 1.8 times larger than that (0.8 V) of the HZO-based FeFET without the additional crystalline ZrO$_2$ seed layer. Moreover, the obtained MW of 1.4 V is comparable to the best results reported to date [9, 11, 14, 17, 21–23, 27].

Reliability with respect to the retention of the HZO-based FeFETs with and without additional crystalline ZrO$_2$ seed layers was also evaluated. Figure 3 shows the $V_{TH}$ retention characteristics after applying a program pulse of $7\, \text{V}/100\, \text{ns}$ and an erase pulse of $-7\, \text{V}/100\, \text{ns}$ at room temperature. It is clear that the $V_{TH}$ values are approximately linear with the logarithmic time scale. The extrapolated MW after 10 years for the HZO-based FeFET with the additional crystalline ZrO$_2$ seed layer is 0.9 V, larger than that (0.6 V) for the HZO-based FeFET without the additional crystalline ZrO$_2$ seed layer. Since the thick capacitance equivalent thickness (CET) of the ZrO$_2$ (1.5 nm)/SiO$_2$ (2.6 nm) gate insulator layers would lead to an enhanced depolarization field in the gate stack [13, 15], further improvement in retention properties could be expected if the thickness of the SiO$_2$ layer is reduced.

Figure 4 shows the evolution of $I_D-V_G$ curves after ±$7\, \text{V}/100\, \text{ns}$ alternating P/E cycles. For the FeFET with the additional crystalline ZrO$_2$ seed layer, both significant shift and slope degradation in the $I_D-V_G$ curves are observed from the early stages of P/E cycling, and the $I_D-V_G$ curves in the erased states exhibit more slope degradation compared with the program states. For the FeFET with the additional crystalline ZrO$_2$ seed layer, although the $I_D-V_G$ curves in erased states exhibit an obvious positive shift during the early stages of P/E cycling that is attributed to the “wake up” effect [13, 28–32], no obvious shift of $I_D-V_G$ curves in the program states is observed up to $1 \times 10^8$ cycles. Moreover, for the FeFET with the additional crystalline ZrO$_2$ seed layer, the $I_D-V_G$ curves in both erased and program states exhibit only a slight slope degradation up to $1 \times 10^8$ cycles.

According to previous reports [12, 28, 33], the parallel shift in $I_D-V_G$ curves is attributed to the gradual accumulation of trapped charges in the gate stack, while the slope degradation in $I_D-V_G$ curves is the result of interface trap generation. Since trapped charges can be detrapped by electrical means, but generation of interface...
traps is irreversible, minimizing interface trap generation is extremely important for improving the endurance properties [28]. The interface traps generated by P/E cycling (Δ\(N_{it}\)) can be described using Eq. (1) [34, 35]:

\[
\Delta SS = \frac{\Delta N_{it} k T \ln 10}{C_{FI} \Phi_F}
\]  

(1)

where ΔSS is the change of the subthreshold swing, \(k\) is the Boltzmann constant, \(T\) is the absolute temperature, \(C_{FI}\) is the total capacitance of gate stack, and \(\Phi_F\) is the Fermi potential. The Δ\(N_{it}\) as a function of the P/E cycle for the HZO-based FeFETs with and without additional crystalline ZrO\(_2\) seed layers is shown in Fig. 5. Clearly, for the FeFET without the additional crystalline ZrO\(_2\) seed layer, the Δ\(N_{it}\) increases obviously from the early stages of the P/E cycling, and Δ\(N_{it}\) in the erased states is much larger than that in the program states. However, the Δ\(N_{it}\) for the FeFET with the additional crystalline ZrO\(_2\) seed layer almost does not change up to 1 × 10\(^3\) cycles, and it is always smaller than that for the FeFET without the additional crystalline ZrO\(_2\) seed layer. Because inserting the additional ZrO\(_2\) seed layer reduces the electric field in the gate stack and thus the band bending is weaker, the interface trap generation is alleviated [12, 14].

Figure 6 shows the evolution of gate leakage current characteristics (\(I_G-V_G\) curves) of HZO-based FeFETs with and without ZrO\(_2\) seed layers with P/E cycling. For the FeFET without the additional crystalline ZrO\(_2\) seed layer, the gate leakage current increases dramatically from the early stages of the P/E cycling. However, the gate leakage current for the FeFET with the additional crystalline ZrO\(_2\) seed layer almost does not change up to 5 × 10\(^2\) cycles, and it is always smaller than that for the FeFET without the additional crystalline ZrO\(_2\) seed layer. It is reported that the increase in the gate leakage current might be related to the generated interface traps [28]. The reduction in the gate leakage current with cycling for the FeFET with the additional crystalline ZrO\(_2\) seed layer would be attributed to the suppression of interface trap generation.

The \(V_{TH}\) values for program and erase states extracted from the \(I_D-V_G\) curves of the HZO-based FeFETs with and without additional crystalline ZrO\(_2\) seed layers are shown in Fig. 7. The HZO-based FeFET with the additional crystalline ZrO\(_2\) seed layer always exhibits a larger MW than the HZO-based FeFET without the additional crystalline ZrO\(_2\) seed layer. Moreover, the MW of the HZO-based FeFET without the additional crystalline ZrO\(_2\) seed layer decreases obviously from the early stages of P/E cycling, while the MW of the HZO-based FeFET with the additional crystalline ZrO\(_2\) seed layer decreases slightly up to 1 × 10\(^3\) cycles. As the P/E cycling number is further increased, the HZO-based
FeFET with the additional crystalline ZrO\textsubscript{2} seed layer also shows obvious degradation in the slope of the \( I_D - V_G \) curves and the MW, due to the enhanced generation of interface traps. However, the MW of the HZO-based FeFET with the additional crystalline ZrO\textsubscript{2} seed layer is still larger than 0.9 V up to \( 1 \times 10^4 \) cycles, which is approximately 2.3 times larger than that (0.4 V) of the HZO-based FeFET without the additional crystalline ZrO\textsubscript{2} seed layer. As discussed previously, the decrease of the required electric field for obtaining more saturated polarization states are probably responsible for the improved endurance properties.

**Conclusions**

The MWs as well as the reliability with respect to retention and endurance of the HZO-based FeFETs with the TaN/HZO/SiO\textsubscript{2}/Si and TaN/HZO/ZrO\textsubscript{2}/SiO\textsubscript{2}/Si MFIS gate stacks were characterized by fast voltage pulse measurements. The results show that the HZO-based FeFET with the additional crystalline ZrO\textsubscript{2} seed layer exhibits a large initial memory window of 1.4 V and an extrapolated 10-year retention of 0.9 V, larger than the initial memory window (0.8 V) of the HZO-based FeFET without the additional crystalline ZrO\textsubscript{2} seed layer. Moreover, the reliability with respect to the endurance of the HZO-based FeFET can be improved by inserting the crystalline ZrO\textsubscript{2} seed layer in between the HZO layer and the SiO\textsubscript{2}/Si substrate. The MW and endurance improvement of HZO-based FeFETs with ZrO\textsubscript{2} seed layers are primarily related to the improved crystalline quality of the HZO layer and the suppressed generation of interface traps due to the decrease of the required electric field for obtaining more saturated polarization states. On the basis of this work, it is expected that employing of a direct crystalline high-k/Si gate stack would further improve the MWs and reliability of the HfO\textsubscript{2}-based FeFETs, and thus warrant further study and development.

**Abbreviations**

CMOS: Complementary metal-oxide-semiconductor; FeFET: Ferroelectric field effect transistor; FeFETs: Ferroelectric field effect transistors; HKMG: High-k metal-gate; HZO: Hf\textsubscript{0.5}Zr\textsubscript{0.5}O\textsubscript{2}; I\textsubscript{D}: Drain current; L: Length; MFIS: Metal/ferroelectric/insulator/semiconductor; MW: Memory window; P/E: Program/erase; P–V: Polarization–voltage; SS: Subthreshold swing; V\textsubscript{G}: Gate voltage; V\textsubscript{TH}: Threshold voltage; W: Width; \( \Delta N \text{it} \): The generated interface traps

**Acknowledgements**

Not applicable.

**Authors’ Contributions**

WWX carried out the experiments and drafted the manuscript. WWX and CL did the data analysis and interpreted the results. WWX, ML, YP, and SZZ designed the experiments. CL helped to measure the device. ML and SZZ helped to revise the manuscript. WWX, CL, and ML participated in the discussion of results. QF, CFZ, JCZ, YH, and YCZ supported the study. All the authors read and approved the final manuscript.
Funding
This work was financially supported by the National Natural Science Foundation of China (Grant No. 51702273), the “Huxiang Young Talents Plan” Support Project of Hunan Province (Grant No. 2018RS3087), the general project of Hunan Provincial Education Department (Grant No. 18C0108), and the Science and Technology Innovation Project of Hunan Province (Grant No. 2017XK02048).

Availability of Data and Materials
The datasets supporting the conclusions of this article are included within the article.

Competing Interests
The authors declare that they have no competing interests.

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Received: 27 April 2019 Accepted: 24 June 2019

Published online: 26 July 2019

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