Dual-output unity power factor rectifier power block

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Abstract: Unity power factor rectifiers find applications in modern utility systems and consumer electronic devices. However, a dedicated rectifier is required for a given load. In this study, a Unity Power Factor (UPF) power block is described which can generate two DC outputs, one buck and one boost, with a reduced number of switches and associated driver circuits. The topology adapts well with conventional control as it retains the dynamic behaviour of a buck and boost topology. While supplying simultaneous loads it exhibits minimal cross-regulation interference between the outputs. The controller implementation for the proposed power block is described and its difference with the conventional Power Factor Correction (PFC) controller is outlined. The topology along with its control to regulate the outputs and force UPF operation are validated using a 200 W prototype with 110 V utility input and 180–24 V DC outputs.

1 Introduction

A typical single-output UPF rectifier uses a diode bridge rectifier cascaded to a boost stage converter (e.g. boost or buck–boost converter) as shown in Fig. 1a. The boost stage converter uses current programming in such a way that the diode bridge rectifier output current (i_r) tracks the rectified voltage (v_r) both in shape and phase on a cycle-to-cycle basis in each switching cycle. The boost converter output (V_{bo}) is regulated at about 10–20% higher than the peak voltage of V_{ac} [1]. The boost terminal can also be used as an output. As shown in Fig. 1a, a buck stage is cascaded to the boost output to interface loads at lower voltages.

Unity power factor rectifiers find application in systems that interface utility to battery operated systems, e.g. chargers, appliances with variable frequency drives etc. They are also proposed to interface a DC system to an AC system in a smart-grid scenario [2]. Conventionally, each appliance is supplied from a dedicated UPF rectifier. For the applications where isolation of outputs is not required, it is desirable to supply multiple outputs from a single UPF rectifier. This is especially desirable for non-sensitive loads like lighting, low-cost consumer electronic devices etc.

Producing multiple outputs from a single-phase AC input supply has been reported in the literature. Integration of rectifier bridge with a flyback converter for multiple output is reported in [3]. In this scheme, the multiple secondaries are present and only one of these secondary outputs is regulated. Therefore, this scheme results in poor regulation as well as cross-regulation performance [4]. A technique presented in [5] uses a controlled switch at one of the secondary outputs which results in better regulation of the outputs. This topology is proposed for lower power applications and it also has the inferior cross-regulation performance. The method presented in [6] uses two converters which are simply connected in parallel at the secondary.

On the other hand, PFC circuits giving simultaneous buck and boost output are discussed in [7–9]. In [7], the buck–boost-based topology is modified to generate an isolated as well as a non-isolated output. It works in discontinuous conduction mode (DCM) operation with one output being galvanically isolated. Single inductor multiple output PFC operating in DCM is discussed in [8]. This topology is generally used for low-power applications. In [9] an interleaved PFC topology is described which is nothing but the parallel operation of two converter blocks. Therefore, there is no significant advantage in terms of a number of switching elements and passive components.

This paper proposes a novel UPF rectifier-based power electronic interface to supply two DC outputs (one step-up and one step-down) from a single AC source with a reduced number of semiconductor switches. The basic block diagram is shown in Fig. 1b. The proposed converter is derived from integrated dual-output converter (IDOC) [10] and has similar dynamic properties as compared to a conventional buck and boost topology. It has excellent cross-regulation properties between the outputs. The proposed work in this document is an extended version of [11].

The topology and its operation are described in the next section. The dynamic properties of the proposed converter and its comparison to conventional topologies are described in Section 3. Implementation of control to regulate both the outputs as well as to achieve UPF operation is covered in Section 4. Some important experimental validations are described in Section 5. Section 6 provides some extension of this philosophy to other converter circuits. Section 7 outlines some important conclusions.
Fig. 2 Schematic of an IDOC

Fig. 3 Schematic of the proposed topology

Fig. 4 Converter waveforms
(a) Switching interval in a switching cycle, (b) Converter waveforms in a power cycle

2 Proposed topology and operation

A method to generate two outputs using an integrated boost and a buck topology is described in [10]. This topology has two controlled switches and an uncontrolled switch. It is called an IDOC. As shown in Fig. 2, an IDOC topology uses time multiplexing of switching operation to utilise the same set of switches for boost and buck converter output regulation. IDOC also has shoot-through immunity for buck converter operation, which makes it suitable for low-power high-frequency implementation.

This paper describes the use of an IDOC topology as a dual-output PFC rectifier. Implementation as a rectifier leads to several new challenges in converter operation and associated control implementation. As a rectifier, the same set of control switches is responsible for the regulation of both the DC outputs as well as for UPF control of input current.

The schematic of the proposed rectifier is shown in Fig. 3 and its operating waveforms are shown in Fig. 4. In this topology, the boost switch is replaced with a synchronous buck converter (SBC) with switches $S_1$ and $S_2$. The SBC works during the $D'$ interval of the boost topology. Therefore, it has a fixed voltage of $V_{bat}$ at its input. Boost interval is realised by turning on $S_1$ and $S_2$, simultaneously.

If the diode rectifier and the AC source are replaced by a DC source, it can be shown that the boost output is controlled by controlling the turn on of $v_{g1}$ and buck converter by controlling the switching time of $v_{g2}$ [10–12]. The switching waveforms for this case are shown in Fig. 4a.

However, as soon as the AC source and diode rectifier are connected, the topology needs to work as a UPF rectifier with two control variables $v_{g1}$ and $v_{g2}$. These two control variables need to perform the following functions: (a) regulate $V_{bat}$ at a voltage higher than the peak of $v_{ac}$, (b) regulate $V_{bk}$, (c) force $I_{L1}$ to follow $|v_{ac}|$ both in shape and phase, (d) regulate the magnitude of $I_{L1}$ such that power balance is maintained. If ideal PFC operation is assumed, the pulse width of $v_{g1}$ required for a fixed $V_{bat}$ is given by

$$d_1(t) \cdot T_s = \left[1 - \frac{|v_{ac}(t)|}{V_{bat}}\right] \cdot T_s$$

As the boost converter output is fixed by varying the duty cycle $d_1$, the buck converter output is given by

$$V_{bk} = D_2 \cdot V_{bat}$$

Ideally, $D_2$ is a fixed, if the boost converter output is assumed to have minimum ripple. The overall pulse width of $v_{g2}$ is given by

$$d_2(t) \cdot T_s = \left[d_1(t) + D_2\right] \cdot T_s$$

3 Dynamic modelling

There are three distinct intervals of the converter as shown in Fig. 3a. Intervals I and III are similar. Dynamic equations during the switching intervals can be written as:

$$L_1 \frac{dI_{L1}}{dt} = v_1 - (1 - d_1) V_{bat} - r_1 I_{L1}$$

$$L_2 \frac{dI_{L2}}{dt} = (1 - d_1) V_{bat} - v_{bk} - r_2 I_{L2}$$

$$C_1 \frac{dv_{bat}}{dt} = (1 - d_1) I_{L1} - d_2 I_{L2} - \frac{V_{bat}}{R_i}$$

$$C_2 \frac{dv_{bk}}{dt} = I_{L2} - \frac{v_{bk}}{R_i}$$

(4) to (7)

Here, $r_1$, $r_2$, and $r_3$ are the internal resistance of the inductors $L_1$ and $L_2$, respectively. The small-signal linearisation of these equations is used for finding out the bode plots, as shown in Fig. 5. The plots are experimentally verified for a scaled down prototype and the results are also plotted in Fig. 5.

4 Controller implementation

A controller is designed to regulate both DC output voltages while maintaining UPF operation at the input side. As identified in Section 2, both $V_{g1}$ and $V_{g2}$ are functions of time; however, the difference between them is nearly constant. The implementation of this control philosophy is shown in Fig. 6. Similar to conventional boost converter-based PFC, the regulation of step-up voltage $V_{bat}$ involves two loops. The outer voltage loop is regulated by a compensator ($G_{batt}$), which is a lower bandwidth compensator. The
inner current loop is designed with a higher bandwidth compensator \((G_i)\). The output of this compensator \((v_{m1})\) is used to generate \(v_{g1}\) which intern generates the duty cycle as given by (1). This compensator forces the current \(i_{L1}\) to follow \(i_{ref}\) while maintaining low Total Harmonic Distortion (THD) [1, 13].

The shaded control block is an addition to the conventional UPF controller. It consists of a voltage compensator \((G_{bk})\) to regulate voltage \(V_{bk}\). The output of this compensator is added to \(v_{m1}\) in order to generate \(v_{m2}\). This modulation signal is used to generate the switching pulse of switch \(S_2\). If \(V_{ref2}\) is set to zero, the shaded control block sets \(v_{g1} = v_{g2}\), the system works exactly like a boost converter. Compared to a conventional IDOC converter, the control for this topology requires one additional current sensor (to sense \(i_{L1}\)). On the contrary, if we compare this controller to a conventional boost PFC, it requires one additional voltage sensor (\(V_{bk}\)).

5 Experimental verification

A 200 W laboratory prototype was built to verify the operation of the proposed UPF rectifier. It is designed to work from a 110 V AC supply and provide a 180 and 24 V regulated DC supply. The switching frequency of the switches is set to 100 kHz. The inductors used in the design are \(L_1 = 992 \mu H\), \(L_2 = 496 \mu H\), \(C_1 = 360 \mu F\), and \(C_2 = 360 \mu F\).

The steady-state waveforms of rectified voltage and inductor currents are shown in Fig. 7. The utility voltage and current along with the regulated outputs are shown in Fig. 8. It is noted that as there is a distortion in the input voltage, the input current simply follows it, which points to the excellent control characteristic of the controller. The excellent cross-regulation performance of the converter is shown in Fig. 9. It is shown that a 50% step-up boost converter output has minimal impact on the regulated outputs.

6 Extension of the concept

The scheme proposed in this work can be extended to achieve multiple buck outputs as shown in Fig. 10a. Similarly, as shown in Fig. 10b, this scheme can be modified to obtain AC output for inverter or isolated converters such as dual active bridge. In both the extensions, the converters will work similar to a voltage fed topology.
Conclusion

The paper proposes a dual-output UPF rectifier topology. The converter operation validates that it can provide two regulated DC output voltages, one higher and the other lower in magnitude with respect to the peak input voltage. A controller is proposed for this converter topology. The controller maintains the regulation of both the outputs and also achieves near unity power factor operation. Excellent cross-regulation immunity between the regulated outputs is verified for the proposed topology.

8 Acknowledgement

The work was supported by Department of Science and Technology, India, under the Mission Innovation Program with grant DST/CERI/MSG/2017/086. Some of the experimental results were obtained by Mr. Sagar Rastogi as a part of his Master's thesis work. The authors will also like to thank him for this contribution.

9 References

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