SOI wafer fabricated with extremely thick deposited BOX layer using a surface activated bonding technique at room temperature

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The fabrication cost of bonded silicon on insulator (SOI) wafers for customized power devices is high owing to the high temperature required and the very long fabrication process involving both thermal oxidation and bonding. In addition, SOI wafers are contaminated with metallic impurities during the formation of the buried oxide (BOX) layer and the bonding of a silicon layer on the BOX layer. Therefore, we propose an alternative SOI wafer fabrication method combining BOX layer deposition and surface activated bonding at room temperature in a vacuum without any voids. There is also no fixed charge in the deposited BOX layer, and the breakdown voltage of this layer is 11–12 MV cm$^{-1}$, the same as that for a thermal oxide layer.

1. Introduction

The reduced use of fossil fuels has become increasingly important to counter global warming. For example, the type of automobile has been changing from gasoline cars to hybrid and electric cars, which contain various power devices. It is necessary for advanced and next-generation vehicles to employ custom power devices with breakdown voltages of more than 500 V between these devices. Because such cars are powered by battery motors, it is most important to decrease the leakage current in electrical isolation regions between such power devices. Thus, it is important how the electrical isolation regions between such devices are formed.

When an electrical isolation region is formed by a pn junction, leakage current is generated between devices at high voltage and temperature. Such isolation is not useful for conventional power devices. It is most efficient for decreasing the leakage current through an isolation region to replace a pn junction with a silicon dioxide (SiO$_2$). In general, silicon-on-insulator (SOI) wafers have been used to form all the isolation regions around power devices using SiO$_2$. SiO$_2$ is used as the buried oxide (BOX) layer inside an SOI wafer. Figure 1 shows a cross-sectional image of an SOI wafer fabricated for power devices. The BOX layer is formed between the power devices and the silicon substrate, and the isolation regions between the devices are formed from SiO$_2$ using shallow trench isolation (STI).

It is becoming increasingly important to decrease the leakage current of custom power devices of hybrid and electric cars above 150 °C compared with that of conventional power devices. Leakage current is increased in the insulator region, which comprises an isolation region and a BOX layer. Thus, it is extremely important to optimize the isolation region and BOX layer of custom power devices.

The isolation region is fixed by the device patterning design (pitch between devices) and device fabrication process (photolithography, etching, and deposition to perform STI), and the BOX layer is optimized by increasing its thickness during the wafers fabrication process.

The thickness of the silicon oxide layer must be increased to decrease leakage current in electrical isolation regions. Thus, the BOX layer must be thicker than the currently available SOI wafers. In general, a BOX layer is formed by thermal oxidation. It takes 2–3 months of heating above 1000 °C to form a BOX layer of more than 10 μm thickness by thermal oxidation. In addition, it also takes 3–4 h to fabricate an SOI wafer to bond a silicon layer to the BOX layer above 800 °C. Because it takes a very long time to fabricate an SOI wafer at a high temperature by the conventional method, the fabrication process is more complicated and SOI wafers have a higher cost than other wafers such as polished and epitaxial wafers. Additionally, SOI wafers are contaminated with metallic impurities during BOX layer formation and the bonding of the silicon layer to the BOX layer.

There is generally a transition layer (SiO$_{x}$, $x < 2$) between the thermal oxide film and the silicon substrate, and this transition layer has a fixed charge. This fixed charge is not neutral but positive. Thus, the conductivity in the silicon layer on the BOX layer changes and the leakage current consequently increases in a well region of power devices in the silicon layer. If the BOX layer is formed by deposition, it might not have any fixed charge, and the conductivity might not change in a silicon layer on this BOX layer. However, the deposited BOX layer might not be denser than a thermal oxide layer. Thus, the breakdown field of the deposited BOX layer might be less than that of a thermal oxide layer (8–15 MV cm$^{-1}$). In addition, the silicon substrate might separate from the deposited BOX layer during power device fabrication at a high temperature.

Therefore, we propose an alternative fabrication method to resolve these issues by depositing a BOX layer below 1000 °C and bonding a silicon layer to the BOX layer at room temperature in a vacuum. Because the deposited BOX layer does not have a transition layer, it might have no fixed charge. In addition, there is a positive correlation between thickness and treatment time in the deposition process. Thus, there is no limit to the thickness of the BOX layer. Because a silicon layer can be rapidly bonded without a high temperature heating, there is no thermal stress. Therefore, metallic impurities will not contaminate the silicon and BOX layers, and the doping element will not out-diffuse from the silicon layer to the BOX layer.

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2. Experimental methods

Figure 2 shows our method of fabricating an SOI wafer with an extremely thick BOX layer. We fabricated two silicon
wafers: a base wafer and a bonding wafer. A BOX layer was deposited on the base wafer by plasma-enhanced chemical vapor deposition (PE-CVD). If the bonding energy between the BOX layer and the base wafer is small, the BOX layer might separate from the base wafer during device fabrication above 1000 °C. CVD is generally carried out below 400 °C. The BOX layer was deposited at 500 °C in this study to strongly bond it to the base wafer. After depositing the BOX layer, only its top surface was polished by chemical mechanical polishing (CMP), so that a bonding wafer could be bonded to the deposited BOX layer without forming voids.

The bonding wafer was then bonded to the base wafer with the polished BOX layer by surface activated bonding (SAB) at room temperature in an ultrahigh vacuum for a short time. Because a silicon oxide layer has many dangling bonds and is stable in the atmosphere, it is very difficult to bond a silicon wafer to a silicon oxide layer by connecting the dangling bonds by SAB. Figure 3 illustrates the SAB process in this study. The silicon element is sputtered from the bonding wafer with argon ions and is then deposited onto the BOX layer made of silicon oxide. This deposited silicon element can act as an adhesive layer between a silicon layer and a BOX layer. The thickness of the adhesive silicon layer can be controlled by varying the conditions of argon-ion irradiation. Thus, it is possible to bond the silicon wafer to the BOX layer by optimizing the conditions of argon-ion irradiation.

After bonding the two wafers (a bonding wafer and a base wafer with the BOX layer), the bonding wafer is ground and polished from the back side, which is opposite the wafer-bonding region, until it has the thickness of the active layer of the device.

2.1. Sample preparation

Table I lists the experimental conditions for the case of 2 inch silicon wafers polished to a thickness of 500 μm. These wafers were made of (100) Czochralski (CZ) silicon single crystals. The resistivity of the n- and p-type wafers was 2–6 Ω cm, and their oxygen concentration was 1.0–1.2 × 10¹⁸ atoms cm⁻³. The n-type wafer was doped with phosphorus and the p-type wafer was doped with boron.

As illustrated in Fig. 2, the base wafer was deposited onto a 10 μm thick silicon oxide layer as the BOX layer at 500 °C for 4 h by PE-CVD. The surface of this BOX layer was polished by CMP. Then, the bonding wafer was bonded to the polished BOX layer of the base wafer as a silicon layer by SAB in an ultrahigh vacuum of 1×10⁻⁵ Pa at room temperature (Mitsubishi Heavy Industries Machine Tool Co. Ltd., MWB08-AX). The top surface of the bonding wafer was irradiated with argon ions with energy below 1 keV. After bonding the two wafers (the bonding wafer and the base wafer with the BOX layer), the back side of the bonding wafer was ground and polished until its thickness was 2 μm. A reference sample was fabricated by thermal oxidation and bonding at a high temperature to compare a currently available SOI wafer and the studied SOI wafer. A
1.2 μm thick BOX layer was formed by thermal oxidation at 1100 °C, and a bonding wafer was bonded to the BOX layer by high temperature treatment at 800 °C for 2 h then at 1200 °C for 1 h.

2.2. Experimental procedure
As illustrated in Fig. 2, we looked for voids after bonding the bonding wafer to the deposited BOX layer [steps (a) and (b)] and after heat treatment during device fabrication [step (c)]. We then evaluated the breakdown electric field of the deposited BOX layer [step (d)] and determined the concentration of the doping element and the resistivity in the bonded bonding wafer after grinding and polishing it to the thickness of the device active layer [steps (e) and (f)].

2.2.1. Evaluation of remaining voids after bonding silicon wafer to BOX layer of base wafer. We evaluated the voids by the infrared transmission (IR) observation after bonding the silicon wafer to the deposited BOX layer by SAB at room temperature in an ultrahigh vacuum. We used an IRise (Moritex) system for the IR observation. In this system, the wavelength of the IR radiation is higher than 1000 nm. Because this IR radiation is transmitted through the silicon wafer and reflected at voids, the voids remaining in a wafer can be detected by IR radiation.

2.2.2. Observation of cross section of studied sample. We used an H9000UHR-I microscope (Hitachi) for the transmission electron microscopy (TEM) observation of wafer-bonding-induced defects. Cross-sectional TEM and high-resolution TEM micrographs were used to characterize structural defects, such as wafer-bonding-induced defects, during the fabrication of the SOI wafer and the heat treatment during device fabrication. This heat treatment was carried out at 1100 °C for 4 h in nitrogen atmosphere,24,25 and the sample stage was loaded and unloaded at 900 °C in an ambient gas of nitrogen in a furnace.

2.2.3. Evaluation of breakdown electric field of BOX layer. Two samples (studied and reference) were also fabricated to form a 100 nm thick BOX layer to investigate the intrinsic breakdown electric field. We evaluated the breakdown electric field of the BOX layer for these samples by time zero dielectric breakdown (TZDB) measurement17) after patterning and fabricating a test element group (TEG) in the silicon layer on the BOX layer. We used a Keithley 237 High-Voltage Source-Measure Unit (Keithley) as the measurement system and an STN-W010-D0.5-L32 system (Tiatech) as the probing equipment. The probe was made of tungsten and had a diameter of 10 μm.

2.2.4. Evaluation of depth profile of doping element concentration in bonding wafer after fabricating SOI wafer. We used an IMS7f device (CAMECA) for secondary ion mass spectroscopy (SIMS) analysis to evaluate the depth profile of the phosphorus concentration, where is the doping element. Small chips were cut from the SOI wafer for SIMS analysis after fabricating the SOI wafer. Then, we analyzed the phosphorus concentration from the surface of the SOI wafer to the bonding interface for the cut chip using the IMS7f device. The phosphorus concentration was estimated from the intensity of the impurity-related SIMS peaks in the IMS spectra.

2.2.5. Evaluation of depth profile of resistivity in bonding wafer after fabricating SOI wafer. We used an SSM2000 device (Solid State Measurements) for the measurement of spreading resistance (SR) to evaluate the resistivity profile in the bonding wafer on the BOX layer. Small chips were cut from the fabricated SOI wafer for SR measurement and lapped at an angle. Then, we measured the resistivity of the lapped chip from the surface of the SOI wafer to the bonding interface while monitoring the electric current using two probes with voltage application.
3. Results and discussion

3.1. Evaluation of remaining voids after bonding silicon wafer to deposited BOX layer of base wafer

We evaluated the remaining voids through IR transmission imaging after bonding the silicon wafer to the deposited and polished BOX layer by SAB at room temperature under a pressure of $1 \times 10^{-5}$ Pa. Figure 4 shows an IR transmission image of the studied sample. The studied sample has no voids except in the three regions indicated by arrow. These three regions were marks left by the tweezers used to place the base and bonding wafers in the bonding equipment. Because this evaluation method can detect gaps of larger than 200 nm, this studied sample has no voids larger than 200 nm except in the regions marked by tweezers. Therefore, we assumed that the silicon wafer could be bonded to the deposited BOX layer by SAB at room temperature in a high vacuum, and similar observations were made for the reference sample fabricated by thermal oxidation and thermal bonding.\(^{26}\) In a previous study, a silicon layer was successfully bonded to a crystalline silicon substrate with the surface amorphized by ion implantation,\(^{27}\) and to a polycrystalline diamond layer deposited on a crystalline silicon substrate.\(^{28}\) Therefore, we found that the SAB method can bond not only a crystalline material but an amorphous noncrystalline material.

3.2. Observation of cross-sectional TEM micrographs of region between bonding silicon wafer and deposited BOX layer of base wafer

We diced the studied SOI wafer, then observed the bonding region of the chips at the center of the wafer through cross-sectional TEM micrographs. Figure 5(a) shows the result of the cross-sectional TEM observation after SOI wafer fabrication. The bonded interface was flat and had no voids larger than 0.5 nm. In a previous study, there was an amorphous layer of 5 nm thickness under the bonding interface after bonding a silicon wafer to a base wafer with a BOX layer.\(^{26}\) This previously studied sample had a polycrystalline diamond layer made of many single crystals as the BOX layer. When argon ions irradiated the surface of a diamond layer to activate it to enable the bonding of a silicon wafer to the diamond layer, the diamond crystals at the surface of the diamond layer were transformed into an amorphous layer. On the other hand, this studied sample does not have a new amorphous layer formed by argon-ion irradiation under the bonding interface, as illustrated in Fig. 5(a). Because the BOX layer of this studied sample is an amorphous layer of SiO\(_2\), argon-ion irradiation does not form a new amorphous layer in the BOX layer. In another previous study, a silicon layer was successfully bonded to a silicon substrate whose surface was amorphized by ion implantation.\(^{27}\) This previous sample also did not have a new layer amorphized by SAB at the surface of the base wafer. Therefore, we found that the SAB method can bond not only crystalline materials but noncrystalline materials such as amorphous materials. In addition, we also observed the cross section of the bonding interface after heat treatment to evaluate the thermal stability of the bonding region. This heat treatment was carried out at 1100 °C for 4 h in an ambient gas of nitrogen in a furnace. Figure 5(b) shows the result of the cross-sectional TEM observation after this heat treatment. There were no extended defects, such as punch-out dislocations, and no new voids at the bonded interface. The bonding interface between the silicon layer and the deposited BOX layer formed by SAB had thermal stability. In the previous study, the silicon layer bonded to the polycrystalline diamond layer by SAB was not removed during the fabrication of the device at 1000 °C, and this bonding interface also had thermal stability.\(^{26}\) On the other hand, Takagi and co-workers reported that a wafer with two crystalline silicon wafers bonded by SAB did not have extended defects or voids at the bonding interface after heat treatment at 700 °C.\(^{29}\) Therefore, we concluded that a bonded amorphous material as well as a crystalline material had thermal stability.

3.3. Evaluation of breakdown electric field of deposited BOX layer

The breakdown electric field of the BOX layer was measured for the studied and reference SOI samples by TZDB, which is a voltage-step-stress method. While a voltage of 0 V was supplied to the silicon substrate under the BOX layer, an additional input-voltage of 0.1 V was supplied to the silicon layer on the BOX layer. In the previous study, we found that the parasitic resistances in the silicon substrate and silicon layer were much smaller than those in the BOX layer and could be ignored for the BOX layer.\(^{26}\) Therefore, this measurement method can evaluate the breakdown electric field of a BOX layer between a silicon layer and a silicon substrate. The electric field of a BOX layer is generally defined as the input-voltage divided by the BOX layer thickness. When the leakage current through the BOX layer from the silicon layer to the silicon substrate was larger than $1 \times 10^{-3}$ A cm\(^{-2}\), the intrinsic breakdown electric field was defined as the C mode.

Figures 6(a) and 6(b) respectively show the results of TZDB measurement for the studied (deposited BOX layer, SAB) and reference (oxidized BOX layer, thermal bonding) samples. The breakdown electric field of both samples was 11–12 MV cm\(^{-1}\). The breakdown electric field of a thermal oxide layer is generally 8–15 MV cm\(^{-1}\).\(^ {17}\) Because the breakdown electric field of the reference sample in the previous study was 8 MV cm\(^{-1}\),\(^ {28}\) that of the reference sample in this study is at least 3 MV cm\(^{-1}\) larger than that of the previously studied sample. Because this difference might have been due to the conditions of the metal fabrication process for TEG, i.e. the sputtering of the metal and the removal photoresist, we thus concluded that these results were reasonable. As illustrated in Fig. 6(a), the leakage
current of the studied sample was larger than that of the reference sample [Fig. 6(b)] for the range of electric fields of $0 \text{–} 10 \text{ MV cm}^{-1}$. We assumed that metallic impurities from the PE-CVD equipment contaminated the BOX layer during the deposition of the BOX layer on the base wafer. This issue will be resolved by coating the metallic components of the PE-CVD equipment with silica. Therefore, the deposited BOX layer has the characteristic of a breakdown electric field as well as thermal oxidation.

3.4. Evaluation of depth profile of doping element concentration in bonded silicon layer on BOX layer

When the devices are fabricated in an SOI wafer, the doping element concentration must be constant in the bonded silicon layer to ensure constant resistivity in the layer. Phosphorus was doped into the silicon layer as an n-type conductor in this study, and we analyzed the depth profile of phosphorus in the silicon layer by SIMS analysis.

Figure 7 shows the results of the SIMS analysis for the studied and reference samples. The parallel axis is the distance from the bonding interface and the vertical axis is the phosphorus concentration obtained by SIMS analysis. The concentration of phosphorus for the studied sample was constant from the top surface of the silicon layer to the bonding interface, as illustrated in Fig. 7(a). When an SOI wafer was fabricated by SAB also in the previous study, the concentration of phosphorus in the silicon layer was constant. On the basis of the diffusion coefficient of phosphorus in silicon crystal, phosphorus will out-diffuse within a region of at least $0.3 \text{ μm}$ from the silicon layer to the BOX layer during the bonding of the silicon wafer to the BOX layer at a high temperature of more than $800 ^\circ \text{C}$ for a few hours. Phosphorus out-diffused within a region of $0.2 \text{ μm}$ from the bonding interface in the previous study, and the range of diffusion in this study is at least $0.1 \text{ μm}$ wider than that in the previous study. The bonding process in the previous study was carried out $800 ^\circ \text{C}$ for 2 h and at $1150 ^\circ \text{C}$ for 1 h, where the latter temperature is $50 ^\circ \text{C}$ lower than that in this study. Thus, we concluded that the difference of $0.1 \text{ μm}$ for the range of diffusion was due to this difference in bonding temperature and that the obtained result was reasonable. Therefore, we found that the silicon layer was bonded to the BOX layer of the studied sample at room temperature without the out-diffusion of phosphorus.

3.5. Evaluation of depth profile of resistivity in bonded silicon layer on BOX layer

When devices are fabricated in an SOI wafer, because a silicon layer is fabricated in the devices, the resistivity of the silicon layer must be constant. Thus, we evaluated the resistivity profiles of the studied and reference samples by SR measurement.

Figure 8 shows the results of the SR measurement. The parallel axis is the distance from the bonding interface and the vertical axis is the resistivity obtained by SR measurement. The resistivity of the studied sample was constant from...
the top surface of the silicon layer to the bonding interface, as illustrated in Fig. 8(a). On the other hand, the resistivity of the reference sample increased from a depth of 0.8 μm to the bonding interface between the silicon layer and the BOX layer. The resistivity at the bonding interface was about 10^4 times that in the region of constant resistivity from depths of 0.8–2.0 μm. Because the bonding process was performed at a high temperature of more than 800 °C, the phosphorus in the silicon layer out-diffused to the BOX layer. The concentration of phosphorus decreased by a factor of 10 from a depth of 0.3 μm to the bonding interface owing to the out-diffusion of phosphorus, as illustrated in Fig. 7(b). Thus, the resistivity in this region should increase by a factor of 10. However, the resistivity increased by a factor of about 10^4, which cannot be explained by the decrease in the concentration of phosphorus. Therefore, we concluded that another phenomenon caused this increase in the resistance of the silicon layer at the bonding region.

3.6. Mechanism of resistivity-change in bonded silicon layer on thermally oxidized BOX layer

For the reference sample (oxidized BOX layer, thermal bonding), according to SIMS analysis [Fig. 7(b)], the phosphorus concentration decreased in the depth 0.3 μm from the bonding surface between the silicon and BOX layers. If the phosphorus concentration decreases from 1 × 10^{15} atoms cm^{-3} to 1 × 10^{14} atoms cm^{-3}, the resistivity of this region will increase tenfold. However, according to the SR measurements [Fig. 8(b)], the resistance in this region was more than 10^4 times that in the other regions. This increase in resistance cannot be explained only by the decrease in phosphorus concentration.

In our previous study, we hypothesized that a positive fixed charge in this BOX layer increased the resistance of the silicon layer at the bonding interface.28) Because we could not demonstrate this hypothesis, we attempted to demonstrate it in this study. We consider that a positive fixed charge in the BOX layer might affect the n-type silicon layer. When the n-type region comes into contact with the p-type region, such as in the pn-junction, the carrier concentration of the n-type region is balanced by that of the p-type region, and the actual carrier concentration of the n-type region decreases from the concentration before coming into contact with the p-type region.33) Figure 9 shows the carrier concentration in the silicon layer after fabricating the reference sample (oxidized BOX layer, thermal bonding). Figure 9(a) shows the depth profile of the carrier concentration calculated by resistivity SR measurement, and Fig. 9(b) illustrates the depth profile of the phosphorus concentration calculated by SIMS analysis. \(D_{\text{ref}}\) denotes the total phosphorus concentration obtained by SIMS analysis in region 1 after fabricating the SOI wafer, \(D_{\text{dep}}\) is the total carrier concentration calculated using the resistivity obtained by SR measurement in region 1, and \(D_{\text{BOX}}\) is the positive fixed charge in the BOX layer. Because the silicon layer is n-type and the fixed charge in the BOX layer is positive (p-type), the following equation was used to investigate the effect of the fixed charge:

\[ R = \frac{1}{nev} \]
\[ D_{\text{BOX}} = D_{\text{ref}} - D_{\text{dep}} \]  

\( D_{\text{ref}} \) is the doped-element concentration multiplied from 0 to 0.8 \( \mu \text{m} \) (1.66 \( \times \) 10\(^{16}\) atoms cm\(^{-3}\)) in the silicon layer, and \( D_{\text{dep}} \) is the concentration from 0 to 0.8 \( \mu \text{m} \) obtained by SR measurement (7.28 \( \times \) 10\(^{15}\) atoms cm\(^{-3}\)). Using Eq. (1), we obtained 7.46 \( \times \) 10\(^{11}\) cm\(^{-2}\) per unit area for \( D_{\text{BOX}} \). The fixed charge of thermal oxide layer is generally 1.0 \( \times \) 10\(^{11}\) - 1.0 \( \times \) 10\(^{12}\) cm\(^{-2}\). The estimated fixed charge \( (D_{\text{BOX}}) \) was near this general value. Thus, we concluded that a fixed charge existed in the BOX layer formed by the thermal oxidation of the reference sample.

On the other hand, we evaluated the SOI wafer with a polycrystalline diamond layer instead of a BOX layer in the previous study.\(^2^8\) The resistivity of a silicon layer on the diamond layer is constant from the surface of the silicon layer to the bonding interface on the diamond layer. We thus concluded that a fixed charge did not exist in this diamond layer, and the deposited SiO\(_2\) layer in this study also did not have a fixed charge. Therefore, the fixed charge was generated in the thermal BOX layer of the reference sample and the resistance in the silicon layer on the thermal BOX layer increased because of this fixed charge.

4. Conclusions

We proposed a fabrication process for an SOI wafer with an extremely thick BOX layer for custom power devices. The BOX layer is depositions by PE-CVD at 500 °C for a short time, and a silicon layer is bonded to the deposited BOX layer by SAB at room temperature in an ultrahigh vacuum without thermal stress for a short time. The bonding region has no voids or extended defects after bonding and heat treatment. The breakdown electric field of the BOX layer is 11–12 MV cm\(^{-1}\), the same as that of the thermal oxide, and because the BOX layer has no fixed charge, the resistivity of the silicon layer does not change. Because power devices are fabricated on a silicon layer bonded to a BOX layer, it is important that the resistivity is constant from the silicon layer surface to the BOX layer. Therefore, we believe that SOI wafers fabricated by our method will be beneficial for advanced and next-generation power device fabrication.

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