A novel approach for FPGA-to-server data transmission over an Ethernet-based network using the eXpress Data Path technology

C. Dülsen, T. Flick, T. Göhring, W. Wagner* and M. Wensing

University of Wuppertal, Gaußstraße 20, 42119 Wuppertal, Germany
E-mail: wagner@uni-wuppertal.de

Abstract: In the context of the upgrade of the Large Hadron Collider at CERN for high-luminosity operation, the particle detectors have to cope with much higher data rates and therefore need to upgrade their data acquisition systems. This upgrade is taken as an opportunity to exchange the currently used highly customized hardware by commercial solutions. Nevertheless, some part of the data processing still needs to be done within Field Programmable Gate Arrays (FPGA), requiring the transfer of data between the FPGAs and the commercial servers. This paper reports on a study of direct data transmission from FPGAs to servers via a commercial network. Large data buffers as required for reliable data-transmission protocols are avoided by using an emerging technique named eXpress Data Path (XDP). Based on XDP, the transmission of 5.2 PB (i.e. $2.92 \times 10^{12}$ packets) was achieved within 168 h without a single missing packet.

Keywords: Electronic detector readout concepts (solid-state); Data acquisition concepts

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1 Introduction

The Large Hadron Collider (LHC) at CERN is the world’s most powerful particle accelerator, searching for rare or even unknown particles and performing precision measurements of standard model processes. To improve the capability of detecting even more rare particle processes, the LHC will be upgraded within the next decade, resulting in an increased number of concurrent proton-proton collisions, while keeping the time between proton bunch crossings at 25 ns, i.e. an event rate of 40 MHz. As a consequence, the experiments ATLAS and CMS will be upgraded in two steps (i.e. Phase I and Phase II) to cope with the higher number of particles produced in one collision event. An important part of the Phase II detector upgrades is the replacement of the inner tracking systems. The spatial granularity of the sensors is increased to resolve the hits produced by the high number of charged particles. The increase in track density and detector granularity leads to more data being generated for the individual collision events. At the same time, the trigger rate is increased from 100 kHz to 1 MHz for ATLAS and 750 kHz for CMS [1, 2]. The data acquisition (DAQ) systems of ATLAS and CMS will be upgraded to cope with these challenges.
Figure 1. The two designs of the readout and process chains used by the ALTAS and CMS collaborations [1, 2]. The event data from the detector elements goes through several processing steps before it is written to the long term storage. The ALTAS experiment makes use of PCIe cards within commodity servers (top chain) for the protocol translation, while CMS favors the usage of a MicroTCA system (bottom chain).

Due to the geometry of particle detectors and the requirement of a low mass implementation, only a limited set of cables with a fixed bandwidth can be used. The same limitations apply to the amount of memory being incorporated into the data acquisition (DAQ) front-end electronics of the detector system. These boundary conditions lead to the requirement of data transmission without any capability for resending data. The loss of data packets must be as low as possible.

Communication with the detector is subject to constraints such as precise timing, radiation tolerance of the front-end electronics, a low material budget to keep multiple scattering at a low level, limited bandwidth, and error tolerance, requiring the usage of custom protocols. Therefore, the DAQ systems make use of Field Programmable Gate Arrays (FPGAs) in the first DAQ stage for being able to process these protocols while keeping the flexibility of a programmable system. All subsequent stages can be implemented in software.

Once data is received by the FPGA it has to be transmitted to a server farm for further processing and event reconstruction implemented in software. This paper describes a proposal for the data transmission from the FPGA-cards to servers meeting the constraints of the future Inner Tracker (ITk) of the ALTAS detector [3].

2 Motivation

With the high-luminosity detector upgrades the DAQ chain will be renewed to accommodate the much higher data rates of 5.2 TB/s for ALTAS and 51 Tb/s for CMS [1, 2]. In the past years, the LHC experiments decided to move from custom designs for the off-detector part of their DAQ systems to commercially available (commercial off-the-shelf, COTS) components, especially for the communication part. The only custom-made part in the off-detector sections of the DAQ chains is an FPGA card converting between detector specific and industry-standard protocols, and performing further aggregation steps to higher-bandwidth links to facilitate the data processing in commercial networks and PCs. All further processing is done by software on commodity servers. The designs of ALTAS and CMS are depicted in figure 1.

These requirements place certain constraints on the design of the DAQ systems. The output bandwidth of the FPGA has to be higher than its input bandwidth in order to not block the data.
transmission. Also, space and power is limited in the service cavern and therefore, a small-sized system is highly desirable. Another requirement of the DAQ system is its reliability in terms of data transmission. Over the lifetime of the detector data losses should be less than 1 % in the transmission and storage of data, including losses due to radiation inside the detector [3].

3 Upgrades of the DAQ for Phase I + II

For the Phase I + II upgrades, the ATLAS and CMS experiments have chosen different methods to transfer the event data from the FPGAs in the service caverns to commodity servers for further processing. This transmission step is depicted in figure 1 as the part within the service cavern.

3.1 The ATLAS DAQ upgrades

For the Phase I upgrade, the ATLAS experiment decided to use a 16-lane third-generation PCI-Express (PCIe) link to transfer the data from the FPGA cards into the host memory and further over the commercial network to the servers for processing [4]. For the Phase II upgrade, the system will be replaced by an updated version. The discussion about the PCIe standard to be used (PCIe generation 5 is favored) is still ongoing, but the data transmission scheme will stay the same.

In the development of the Phase I upgrade, the protocol used for transmission was switched from TCP to Remote Direct Memory Access (RDMA) since the processing of the TCP protocol generates a large CPU workload and data is copied several times. The RDMA protocol offers the reception of data without any involvement of the CPU because the network interface card (NIC) stores the data directly into a buffer being prepared by the receiving software within the host memory of the receiving server. For the Phase II upgrade, research work has started in ATLAS to study the usage of RDMA inside the FPGA. Promising first studies have been performed, getting close to the theoretical bandwidth limit of the communication link [5].

While the usage of RDMA helps to reduce the workload of data reception, the DAQ system still has to store the data on the sending side until the correct transmission is acknowledged.

3.2 The CMS DAQ upgrades

The CMS experiment uses a MicroTCA system holding the FPGAs for the Phase I upgrade. The network interface is implemented in the firmware using TCP. TCP was developed as an internet protocol and thus covers the complete path from the sender to the recipient, including all its subsections. The available bandwidth for a transmission needs to be constantly probed since the available bandwidth for each subsection is not known in advance and can vary over time. This is done by increasing the sending rate until the fraction of dropped packets is getting too high, making retransmission a key requirement of the protocol. Furthermore, the algorithms used by the TCP protocol are optimized for a software implementation. Therefore, CMS developed a simplified version of TCP on the sending side, but is still compatible with the standard on the receiving side, such that a commodity server running an unmodified Linux can be used. As in the case of RDMA the usage of TCP also requires sufficient memory in the sending FPGA.

The current system uses a single 40 Gb/s port consisting of four 10 Gb/s links per FPGA. The FPGA provides enough internal memory resources to store the data for possible retransmissions, so no external memory is needed. For the Phase II upgrade [2], these 40 Gb/s ports are planned to
be replaced by several $100\text{ Gb/s}$ ports ($4 \times 25\text{ Gb/s}$ each) per FPGA. The Xilinx VU35P FPGA is chosen since it features sufficient built-in high bandwidth memory (HBM) required for buffering data to ensure a lossless transmission from the off-detector cards to the event builder.

### 3.3 Motivation for studies without buffering of data

The described usage of the TCP and RDMA protocols in the DAQ of ATLAS and CMS is different from what the protocols were originally developed for. In this sense, they may not be the most ideal choice. Both solutions require the buffering of data until the receiving side acknowledges the reception of the data. The memory needed for the buffering requires the use of specific FPGAs with a large amount of memory, or the design of a complex interface to high-speed external memory. In addition, TCP constantly probes the available bandwidth of the transmission chain. However, for the LHC experiments, the bandwidth of the optical data links between the front-end electronics and the off-detector hardware defines the maximum data rate of each stream. Exploiting this knowledge, the subsequent network can be specifically optimized to have enough bandwidth for all transfers. Furthermore, reliable data transmission is not guaranteed over the full data path at the LHC experiments, since the detectors are not able to deliver error free data all the time. The reasons for this are the radiation environment and general operational issues. Nevertheless, each component should contribute as little as possible to the data loss. However, the inevitable occurrence of data loss poses the question whether the implementation of reliable data transmission between the FPGA and the higher level DAQ servers is necessary or whether this requirement can be lifted, resulting in a considerable reduction of system costs with a sufficiently small amount of data being lost. Choosing an unreliable data transmission scheme suggests the usage of UDP which in addition has the benefit of requiring significantly less processing power.

### 4 Data reception in Linux systems

Because the Linux network stack is optimized in terms of functionality and performance for average usage, it lacks performance in more specific scenarios. Most of these scenarios have to handle either a very high packet rate or very high data throughput.

A way to increase the performance is to bypass the Linux kernel and its network stack and to handle the whole chain in userspace. This means, that the user programs take control of all involved components including the network card. Such a solution requires the user programs to also include the corresponding drivers. Frameworks like the Data Plane Development Kit (DPDK) thereby provide an abstraction layer to abstract also from the operation system [6]. The downside of such solutions is that the user program needs to handle the complete network traffic, including network traffic not meant for the specific application. This traffic is simply dropped since the re-injection into the Linux network stack would generate too much overhead. Therefore, such solutions are only viable if the framework has access to a separate NIC.

To solve this issue, a novel technique called eXpress Data Path (XDP) [7] was developed for the Linux kernel. This technique offers a fast lane which bypasses the Linux network stack and reduces the processing overhead for data reception of selected network traffic. The remaining traffic is still handled by the Linux network stack. XDP makes use of a virtual machine called Berkeley Packet Filter (BPF) [8] within the Linux kernel to filter the arriving network traffic right after the NIC issues
Figure 2. Comparison of the DAQ architectures used by the ATLAS experiment (top) and the CMS experiment (center) versus the novel architecture proposed by this paper (bottom). While the architecture used by ATLAS favors simplicity on the receiving side, the CMS experiment focused on the optimization of the sending side. The novel architecture combines both approaches and applies additional optimizations to reduce the needed resources even further.

the network interrupt. This filtering is based on the receive queues of the NIC and results in one of the predefined actions:

- drop the packet
- send it out on the same NIC again
- redirect to another interface
- redirect to an XDP socket
- forward it to the network stack

In case of redirection to an XDP socket, the selected packets are moved into a memory area prepared by the user application. The communication via the socket is therefore reduced to manage the individual packet slots within this memory area, for example notifications of filled slots or marking them as available again. The drawback of this technique is, that no protocol decoding or error checking is done by the Linux network stack and therefore these tasks need to be implemented in the user application. This new technique is mainly used for network management or filtering software or to accelerate the network interfaces of virtual machines. No prior case of its use for improving direct data reception is known to the authors of this paper.

5 Novel architecture

To overcome the limitations of the current DAQ systems, a novel architecture is proposed in this paper which is shown in figure 2. The data are transmitted directly from the FPGA into the network as in the CMS experiment, but the UDP protocol is used rather than the TCP protocol. The direct transmission enables a better scalability of the system compared to the usage of a PCIe card with a fixed bandwidth, while usage of the UDP protocol reduces the system complexity by obviating the need for additional
memory components due to the omission of guaranteed data transmission. The combination of both optimizations results in a reduction of the required resources (space, power, costs).

However, the simplicity of the UDP protocol comes at a price: In UDP, each packet stands for itself and there is no information about the order of packets or completeness included in the protocol. This also means that the information of the UDP protocol header is not enough to determine the fraction of lost packets. To be able to determine this fraction, additional information is needed to establish a fixed relationship between the network packets. The easiest solution for this problem is the usage of a packet identifier field which is filled by a packet counter. In contrast to the identifier of the IP protocol which is increased by all packets of the same network interface, the identifier implemented here is used for each individual data stream and therefore the stream processors should see continuously increasing values. This packet identifier is implemented in a new protocol called Data ReadOut Protocol (DROP) [9]. A retransmission of lost packets is deliberately not included in this protocol to avoid a requirement for additional memory in the FPGA.

Even if the content of subsequent packets is independent of each other and therefore no ordering is required, the ordered structure of the identifier field eases the check of packet loss as depicted in figure 3.

With the packet identifier being counted up, the packet identifiers of consecutive packets should have a distance of exactly 1. There are two error cases if only the distance between the packet identifiers of consecutive packets are checked:

- Is the distance larger than 1, the packets in between are regarded as being dropped.
- Is the distance 0 or negative, it is assumed that additional packets are seen.

More complex patterns of unexpected behavior can be modeled by combinations of the two cases. For example, the out of order delivery of a packet would result in three error reports:

1. a distance larger than 1 is reported (i.e. the delayed packets are reported as missing)
2. a negative distance is reported (i.e. the delayed packets are now reported as additional packets)
3. a distance larger than 1 is reported (i.e. the early packets are now reported as missing)

\footnote{Also a pseudo random ordering can be used as long as the receiver can determine the expected counter value.}
This example shows that certain combinations of such error reports can still indicate a lossless data transmission. However, the intention is to achieve a data transfer without any of such reports.

On the receiving side, the XDP technique is used to achieve a reduction of the CPU load for data reception similar to the RDMA used by the ATLAS experiment. XDP redirects the incoming network packets to the software instance dedicated to the data stream as described in the previous section. To steer the redirection by the BPF program, the received packets are sorted by their UDP destination port into the corresponding receive queues.

To reach maximum performance of the receiving program, it has to be optimized for the architecture of the used CPUs. Also, the receiving program needs to be split up into threads to ensure that each task can work as independently as possible and not be blocked by other tasks. Since the transfer of data between the CPU cache and the host memory needs a considerable amount of time, the whole protocol processing should happen within the CPU caches. This requires good knowledge of the architecture of the CPU, especially about the connections between the CPU cores and the different cache blocks. For test setup under study an optimized assignment of tasks to CPU cores is presented in section 9.

6 Test setup

To determine the fraction of lost packets and evaluate the new approach, a test system was set up as shown in figure 4. The setup consists of Xilinx FPGA evaluation kits as data sources and a commodity server as data sink. The boards used are the ZCU102, featuring a Zynq Ultrascale+ FPGA, and the VCU128 with a Virtex Ultrascale+ FPGA. Since the ZCU102 supports only a single 40 Gb/s Ethernet connection, two of these are used to reach the intended data rate. This setup has the benefit of having two independent data sources whose data streams needed to be interlaced. The VCU128 supports up to four 100 Gb/s Ethernet connections from which one is used for presented tests. The firmware of the FPGA consists of an UDP/IP network stack with a line rate of 40 Gb/s or 100 Gb/s (i.e. 40GbE and 100GbE) depending on the firmware version, a module implementing the DROP protocol and multiple data generators, producing a data rate of up to 10.24 Gb/s each [9]. The resources utilised inside the FPGA for implementing the network stack are given in table 1. The data generator can be configured using the following parameters:

- block size specifying the amount of data to be generated,
- packet size for the maximum size of the parts the block is split into,\(^2\)
- the selected pattern type (e.g. 16 b counting pattern).

\(^2\)The last packet may not reach the full size since the remaining number of bytes within the block is limited.

|                  | Ethernet subsystem (100G) | UDP/IP stack | DROP protocol |
|------------------|--------------------------|--------------|---------------|
| LUTs             | 10100                    | 5600         | 1900          |
| Flipflops        | 14100                    | 15800        | 2800          |
| Block RAM (kBit)| 144                      | 918          | 0             |
Figure 4. The test setup consists of up to three FPGA evaluation boards with different link speeds as data sources, a 100 Gb/s Ethernet switch and the commodity server being used as data sink.

Figure 5. In general, a core complex (CCX) of the AMD Zen2 architecture [10] houses four CPU cores and their CPU caches. In the used variant of the CPU, only two out of the four cores are activated, while all four L3 cache blocks are available.

Furthermore, the generated data rate can be reduced by introducing artificial pauses after each data word or at the end of a packet. The output of the data generators is then packed into DROP streams with the packet identification field being counted up for each packet. Thereby, the output of several data generators can be packed into the same DROP stream when a data rate higher than 10.24 Gb/s for a single data stream is needed or the data stream should include packets of different sizes.

The FPGA boards and the servers were connected by a 100GbE network switch. The network was reserved for the presented tests and not used for other services, and had no direct connection to other networks. In addition, the server was connected to a 1 Gb/s management network used to access the server from remote.

The used server is equipped with two AMD EPYC 7302 CPUs with 16 cores / 32 threads each and a clock frequency of up to 3.3 GHz. A Mellanox ConnectX-5 100GbE NIC was used as network interface. The operation system is Fedora in version 30 and the Linux kernel version is 5.2.9. To reduce the interruptions by the remaining system, a complete CPU³ of the server is isolated from the Linux scheduler such that no other process than the ones needed for the test is running on these.

The AMD Zen2 architecture used in the EPYC CPUs groups processor cores into core complexes (CCXs) [10] with a combined level 3 cache for all cores within the CCX as shown in figure 5. To avoid unnecessary data transfers all threads of an instance of the user program including the network interrupt running the BPF program were placed on the same CCX.

The user program was split into a thread taking care of the XDP sockets as well as monitoring the incoming data (i.e. checking the packet identifier, counting received packets and bytes) and

³The one which provided the PCIe lanes used by the NIC.
the threads histogramming the payload (i.e. counting the occurrence of each 16 b word). The histogramming is done to include a workload similar to the decoding of the data streams coming from the detector elements. Since the test data consists of simple counting patterns, there is nothing to be decoded. However, the histogramming ensures that each byte of the payload is accessed and therefore the whole packet was loaded into the CPU cache. The management thread is common for all data streams being received by the instance of the user program while the threads histogramming the data serve a single data stream each. To keep the data locally in the cache of the CCX, an individual instance of the user program is started for each CCX used. In other words, only a single instance of the user program should run on a CCX to make best usage of its limited resources.

7 Measurements

The described setup was used to perform a series of measurements which can be grouped into three phases. The first phase addresses the total maximum packet rate (measured in million packets per second, Mp/s) the server can handle. It is assumed that this packet rate only depends on the number of packet headers (i.e. the number of packets) to be processed. Since the memory for the packet buffers is pre-allocated, the payload size is assumed to have no impact on the total maximum packet rate as long as a constant data rate is maintained. With the maximum user data rate being the product of the maximum packet rate and the payload size used, these measurements are important for determining the minimum payload size needed to achieve a given data rate.

The second phase deals with the question of how many CPU cores are needed to process the total data rate. The processing capability of a single CCX is evaluated by investigating the packet loss for different assignments of the threads. The result of this group of measurements is a set of rules on how to assign the different threads to reach the best performance as well as a recommendation about the distribution of processing of individual data streams on the used CPU.

In the third phase, the results of the other phases are validated by performing long term measurements. The long duration is necessary since the limit on the packet loss rate corresponds to the total amount of transferred data.

8 Measurement: maximum packet rate

Since the processing of the protocol headers is expected to be the most time-consuming part of the data reception process, the number of packets (and therefore the number of headers to be processed) which can be received in a given time period is an important characteristic of the server. This value defines the minimum packet size needed to reach an intended data rate.

The measured packet rates are expected to vary around a fixed point. Since only the order of magnitude of the fixed points is of interest, the duration of the tests was only a few minutes for each measurement until the results settled.

**Measurement: packet rate with packet loss.** To measure the total maximum packet rate of the server, a very large number of packets was sent at a very high rate to the server and the number of packets seen by the receiving software was recorded. The data generators were configured to send packets with a payload size of 64 B at the highest possible rate, resulting in a packet rate of
Figure 6. Measured packet rate for different numbers of data streams for packets with a payload size of 64 B. The results for up to three data streams show a good linearity, i.e. the additional streams do not interfere with the existing ones. Starting with four data streams, the total packet rate saturates and reveals the limits of the system.

around 16 Mp/s per data stream [11]. Since a single CPU core is expected to be unable to cope with the total packet rate, the number of active data streams (i.e. pairs of data generators and receive programs) was increased during the test while the configuration of the data generators was fixed. On the receiving side, the number of recognized packets per data stream was measured and the sum over all streams was taken. The total maximum packet rate is expected to saturate at a constant value for the packet rate, which marks the end of this test. Since it is obvious that packets will get lost in these measurements, the fraction of lost packets is ignored.

The results of the measurement are shown in figure 6. A single data stream achieved a maximum packet rate of 4.66 Mp/s without any decoding and 3.88 Mp/s when the decoding was turned on. With the increasing number of data streams used, the corresponding multiple of these values were measured, showing the limitation by the CPU cores. At a rate of around 15 Mp/s, the total packet rate saturated with four data streams and remains quite stable when the number of data streams is further increased. Therefore, the maximum packet rate the server can handle is determined to be at the level of 15 Mp/s.

Measurement: packet rate without packet loss. Since the first measurement ignored the fraction of lost packets, the measurements were repeated in a slightly different way to get the limit on a lossless transmission. The packet rate was varied by changing the length of the pause between consecutive packets while the packet size and the number of data streams were kept constant. The maximum packet rate of each data stream was chosen such that the accumulated packet rate of all streams exceeded the total maximum packet rate of the server measured in the first measurement by about 10%. The payload size was set at a value such that the maximum packet rate per data stream is reached by a generator when only the minimum pause length is applied. This results in the use of five data streams, a maximum packet rate per stream of 3.4 Mp/s and a value of 350 B for the...
Figure 7. The relation between measured and expected total packet rate for the repeated measurements with five data streams, a payload size of 350 B and with an artificial delay of different length. The length of the delay was reduced for each individual measurement until the ratio between both differs from one. The limit on the total packet rate was already found at a lower point with respect to the measurement with a payload size of 64 B. At that point, length of the delay has not reached zero meaning that the limit is not caused by the sending side i.e. the full data rate of the data generators is not reached.

payload size. The length of the pause between packets was set to very high values (i.e. low packet rates) at the start of the tests and was reduced for each measurement to increase the total packet rate. Since the total packet rate of all data streams is set to be larger than the maximum packet rate of the server, packets are expected to start to get lost at some point and the total packet rate saturates at the total maximum packet rate of the server.

In this second measurement, the data was transferred without packets being dropped for packet rates below 12 Mp/s. When exceeding a packet rate of around 12 Mp/s, all data streams started to lose packets, limiting the measured packet rate at that level as shown in figure 7. Since the observed total maximum packet rate in this measurement is different from the one in the first measurement, a dependence on the packet size is inferred.

Measurement: influence of the packet size on the packet rate. To investigate the dependence of the total maximum packet rate on the packet size, a third series of measurements was done. Compared to the second series of measurements, the packet sizes was varied. The packet size was chosen to be a power of two up to 2048 B\(^4\) and multiples of 64 B up to 512 B. In addition, packet sizes one Byte larger than the aforementioned values are tested.

The measurements of the third series revealed several steps in the achievable packet rates as shown in figure 8. The steps were found for each aforementioned pair of packet sizes. For example, the server can handle packets of 257 B at a notably lower rate than packets of size of 256 B. However, the reduction of the packet rate for each step shows no clear pattern. In addition to the measured packet rates, the maximum packet rates that can be generated with four and eight data generators (i.e. around 40 Gb/s and 80 Gb/s respectively) are depicted.

\(^{4}2048\) B is the largest packet size being a power of two and being supported by XDP.
**Figure 8.** The measured total packet rates for different payload sizes. The measurements revealed steps in the achievable packet rate at packet sizes being a multiple of 64 B up to 512 B as well as at 1024 B and 2048 B. The packet sizes below 192 B are not shown as their results were at the same level as for 192 B. In addition to this, the maximum total packet rates for four and eight data generators are included. Only a small range of packet sizes is able to reach the full data rate of eight data generators.

**Discussion.** An important result of the tests is the very narrow range of parameters to be used to achieve the optimal performance. Only packet sizes just below 2048 B were able to support the full payload data rate of around 80 Gb/s of the eight data generators used,$^5$ resulting in a packet rate of around 5 Mp/s. For all other packet sizes, the packet rate had to be reduced to prevent packet loss. This might restrict the possible patterns used to transfer data from the detector towards the processing system. With most detector elements having no or only a very small number of hits to report, it can take some time to fill a complete frame and therefore might hit the timing requirements. In such cases, it would be better to combine the responses of the same event from different detector elements instead of the event fragments of the same detector element from multiple events.

### 9 Measurement: optimization of task assignment

With the reachable packet rate of the server (i.e. around 5 Mp/s) being known from the previous set of measurements and the corresponding packet size (i.e. 2048 B) to reach the intended overall data rate (i.e. a payload data rate of about 80 Gb/s), the question arises how to distribute the processing tasks across the CPU cores. To minimize the number of CCX needed for the reception and decoding, the maximum data rate a sole CCX can handle is determined. Thereby, the basic test setup stayed the same as used for the packet rate measurements.

The achievable performance is expected to depend on the assignment of the different threads to the available logical cores of a CCX. Therefore, the possible combinations of thread assignments are

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$^5$A payload data rate of around 80 Gb/s is regarded as maximum reasonable data rate to leave some headroom for other network traffic.
evaluated and rated by the fraction of lost packets for different number of data streams (starting with a single one). The goal is to find the combination with the highest data rate without losing packets.

After all measurements for a given number of data streams were conducted, some general rules for conflicting combinations (i.e. the combinations with packet loss) were derived. These rules were then applied for the next round of measurements to keep the number of measurements at a manageable level. If no combination for a given number of data streams was able to achieve a lossless data transmission, the combinations with the lowest packet loss were repeated with reduced data rate until no packets were lost or the overall data rate was below previously obtained rates.

In contrast to the previous measurements, the requirement to minimize the packet loss is to be taken into account for this and all the following measurements. The payload size is set to 2000 B as a result of the previous tests. The data rate per stream is set to 10 Gb/s if no other value is specified. The duration of each test run is limited to 1 h for broader searches and to a few hours for some special cases.

Since the interrupt thread is fixed in position by the system configuration, only the assignment of the receiving thread and the worker threads for each data stream can be changed. The four different positions are defined as:

- **Position 0** is the logical core on which the interrupt thread runs.
- **Position 1** is the other logical core of the same physical core on which the interrupt thread is running on.
- **Position 2 and position 3** are the logical cores of the second physical core of the CCX.

If multiple data streams are used, it is assumed that all worker threads behave the same and therefore the order of these can be ignored. These threads are assigned with increasing stream number (i.e. stream 0 always gets a smaller position number than stream 1).

**Measurement: one stream.** For measurements of a single data stream per CCX, 16 combinations were tested since both the receiving thread and the worker thread were allowed on all four positions. Since the CPU used contains eight CCX, eight of the combinations were tested in parallel.

With a single data stream, all combinations with the worker thread having its own position (i.e. not shared with other threads) showed no data loss. As soon as the same position was shared with another thread (either the receiving or the interrupt thread), packet loss was seen. Having the receiving and interrupt threads share the same position (i.e. position 0) did not generate packet loss. The combinations with packet loss did not show a general pattern. For example, no indication was found that the packet loss is smaller if the worker thread runs on the opposite physical core than the receiving thread. Therefore, the only rule derived from these tests is that the worker threads need their own position which should not be shared with any other workload.

**Measurement: two streams.** When following the rule that a worker thread should not share its position with any other workload, the number of possible combinations for the two-data-stream scenario is reduced drastically. An additional feature of the setup is, that the ordering of the data
streams and their associated worker threads is not changed, that is, the lowest stream number always runs on the lowest available position. Thus, only six combinations remain:

- When the receiving thread runs on position 0, the two worker threads can run on any of the other three positions, resulting in three possible combinations (i.e. one combination for each unused position).

- When the receiving thread runs on any position other than 0, the worker threads are fixed in their position since they are not allowed to run on position 0, which always hosts the interrupt thread. This results again in three possible combinations.

In the case of two data streams, all tested combinations resulted in packets being lost. The two combinations with both worker threads running on the second physical core (i.e. position 2 and 3) and the receiving thread running on position 0 or 1 had the highest fraction of lost packets (larger than 30%). Both combinations with the first worker thread on position 1 and the second worker thread as well as receiving thread on the second physical core (i.e. each thread with its own position and both worker threads running on different physical cores) had the lowest packet loss observed at the level of a few 10 ppm.

**Measurement: two streams, reduced data rates.** Since the two cases with the lowest packet loss had roughly the same fraction of lost packets, both were tested again with reduced data rates. For both combinations, the data rates for both data streams were reduced alternately until no lost packets were observed over a period of 12h.

The best result was achieved with the receiving thread running on position 2 and the two worker threads running on position 1 and 3. The total data rate reached 15.5 Gb/s (7.5 Gb/s for the first stream and 8.0 Gb/s for the second stream). As soon as the data rate of either stream was slightly raised (i.e. by 0.5 Gb/s) the first stream started to lose packets while the second stream did not.

The same was true when a third data stream was added to the tests, independent of its position. As a result, the maximum achievable data rate per CCX is found to be 15.5 Gb/s.

**Discussion.** The presented results confirm the use of a complete CPU for the data reception and processing. With the histogramming of the data being only a very simple reflection of the real processing to be done, some additional processing capabilities should be reserved for the more complex data formats. Therefore, it would be better to rather process only a single data stream on a CCX than to use this processing power for the reception of a second data stream. This helps in keeping the data locally in the cache. In addition to this, the real setup would require the transmission of the data to the next processing step which will also occupy processing resources and was not done in the test setup presented.

10 **Measurement: long duration tests**

In this set of measurements, the duration of the measurements was increased to include spurious effects that may occur only very rarely.
**Measurement.** For the long duration tests eight data streams with the maximal data rate of 10.24 Gb/s each were used, resulting in a payload data rate of around 80 Gb/s, not including any protocol overhead. Each data stream was assigned to a separate CCX since the measurements at maximum data rate showed that a single CCX cannot handle two of these streams without losing packets.

The data generators produced a 16 b counting pattern and the processing was implemented by counting the occurrence of each 16 b word. Since the block size is a multiple of 128 kb, each counter value has the same frequency in the data stream. The used payload size per packet of 2000 B, however, is not equal to a power of two (i.e. only having a relative small common factor with respect to the block size) and thus the time period is increased until the identical payload is seen again.

Histogramming of the data words was used as a method to check the completeness and correctness of the transferred data. The 16 b words are split into an upper and a lower byte. These two bytes are used as indices in a two-dimensional array with the entry at the given position holding the number of occurrences of the corresponding 16 b word. When the histogram is plotted, each data word is represented by a pixel with a color corresponding to the value of its counter. In case of a lossless data transmission, the difference between the highest and lowest occurrence of data words seen is one at most. The difference occurs for the cases in which the amount of transferred data is not exactly a multiple of 128 kb since the test is aborted at a random point. Therefore, the plotted histogram for a lossless data transmission features at most two homogeneously filled areas. In contrast to a successful test, an example histogram of a flawed data transmission is depicted in figure 9.

In this test, data words were lost at the level of $10^{-6}$. The histogram shows a clear indication of unevenly distributed occurrences of data words.

The duration of the long-term measurements was set to seven days. If a notable packet loss occurred, the measurement was aborted to investigate the cause of it. This was repeated until an acceptable fraction of packet loss was achieved.

**Results.** The final long duration test ran seven days with a total amount of 5.2 PB of data transferred within 2.92 trillion packets. During this test, not a single packet was lost in any of the eight data streams. To give an upper limit on the ratio of lost to transferred data packets, it is assumed that the next packet got lost, resulting in a ratio of $3.423 \times 10^{-13}$. This result was reproduced in tests with a similar duration.

The correctness of the result was checked by multiple methods. First of all, the reporting of the receiving software was checked by provoking an error situation. An instance of the receiving software was started and kept running until the end of the test. Then, a data stream was started, sent towards the previously started software instance and stopped at a random point. Afterwards, a second data stream with a different value of its packet identifier field was started and sent towards to same software instance. The result of this test was the correct detection of the jump of the value of the packet identifier field.

The plotted histograms generated by the worker threads can also be used to check the correctness of the result as described in the measurements section. In case of the final long duration test, all these packets were lost at the level of $10^{-6}$. The histogram shows a clear indication of unevenly distributed occurrences of data words.

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*The data generators were configured to start the counting pattern with a value of 0 and were started after the receiving programs were ready. Therefore, there cannot be a second step resulting from a misaligned starting point.*
Figure 9. An example of a histogram of transmitted data words for a flawed data transmission. The histogram counts the occurrence of 16 b words received in the payload. The words are split into an upper and a lower byte both of which are used as indices defining a two-dimensional array. The strips of different (darker) color indicate the loss of data words. A lossless transmission, in contrast, would result in two monochromatic areas with the counter values for both areas being off by one. In this example, bit flips in the payload resulted in invalid checksums and complete packets were dropped. Since a payload size of 2000 B was used, a packet corresponds to slightly less than four lines in the histogram.

plots were divided only into two monochromatic areas with the counter values for both being off by one. This does not only prove that no packet was lost in between, but also that no bit got flipped. Another way to verify the result is to sum up all counter values of a histogram. Since a data word contains two bytes, the sum should thus be equal to half the number of bytes transferred by the corresponding data stream. This third method also confirmed the result of no packet being dropped. The amount of transferred data per data stream was around 700 TB.

Discussion. The most important result of the performed tests is that not a single packet was dropped during the long duration tests. This is the optimal outcome and was achieved by using the XDP feature of the Linux kernel, leading to a significant reduction of the processing overhead. Thus, the proposed system allows for a highly reliable data transfer, while the usage of protocols with guaranteed data transmission like TCP offer little additional benefit, but requires much larger system resources. The presented approach based on direct data transmission from the FPGA to the DAQ servers via a UDP-based protocol offers a valid opportunity to reduce the overall system complexity and system costs.

7Each stream had its own set of values since the streams were not started and stopped exactly simultaneously and therefore the amount of transferred data differs from stream to stream.
8The occurrence of only combinations that cancel each other out is unlikely and therefore ignored.
11 Conclusion

In this paper, a novel approach of transferring data between FPGAs and commodity servers was studied. This alternative is based on waiving guaranteed data transmission to enable a reduction of the system complexity and system costs. The XDP technique was used for the first time in the context of high energy physics to accelerate the data reception in the DAQ systems. XDP helps to reduce the CPU workload and therefore plays a key role in achieving a lossless transmission of 5.2 PB of data with a payload data rate of 80.0 Gb/s. This result proves the validity of this alternative approach.

The studies showed that the performance of the data transmission in terms of the achieved payload rate depends critically on the chosen packet size. The maximum packet rate is a feature of a given server, providing a certain number of CPU cores. The rate depends on the tasks of the CPU cores and has to be determined for a given configuration. Discontinuous strong drops in the packet rate are observed when passing powers of 2 in the packet size. To obtain an optimized transmission for a specific server configuration, the packet rate and the packet size need to be carefully adjusted. For the specific setup under study optimal performance is observed for a packet size just below 2048 B, the largest packet size supported by XDP.

Furthermore, the system performance depends critically on the assignment of tasks to the logical cores of the CCX. Processing a single data stream per CCX is recommendable, even though the processing of two streams in a single CCX is found to be possible without losses if the data rates are reduced accordingly.

The next step of further evaluating the proposed system will be the use of realistic data patterns as expected from the tracking detectors at the LHC. This includes the use of the real data format being generated by the detector elements and the corresponding decoding routines. Since the parameters for the data transmission had to be optimized for the system used, the optimization process needs to be repeated as soon as the system is changed, for example if a different type of CPU is used.

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References

[1] ATLAS collaboration, *Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ System*, CERN-LHCC-2017-020, CERN, Geneva (2017) [DOI: 10.17181/CERN.2LB.4IAL].

[2] CMS collaboration, *The Phase-2 Upgrade of the CMS Data Acquisition and High Level Trigger*, CERN-LHCC-2021-007, CERN, Geneva (2021).

[3] ATLAS collaboration, *Technical Design Report for the ATLAS Inner Tracker Pixel Detector*, CERN-LHCC-2017-021, CERN, Geneva (2017) [DOI: 10.17181/CERN.FOZZ.ZP3Q].

[4] ATLAS collaboration, *FELIX and SW ROD Commissioning of the New ATLAS Readout System*, ATL-DAQ-PROC-2020-026, CERN, Geneva (2020).

[5] M. Vasile et al., *Integration of FPGA RDMA into the ATLAS readout with FELIX in High Luminosity LHC*, 2023 JINST 18 C01025.
[6] The Linux Foundation, *DPDK, Data Plane Development Kit*, https://www.dpdk.org/ visited on 18/11/2020.

[7] T. Høiland-Jørgensen et al., *The eXpress data path*, in the proceedings of the *CoNEXT ’18: The 14th International Conference on emerging Networking EXperiments and Technologies*, Heraklion, Greece, December 4–7, 2018 [DOI:10.1145/3281411.3281443].

[8] Cilium Authors, *BPF and XDP Reference Guide*, https://docs.cilium.io/en/latest/bpf/ visited on 21/10/2020.

[9] C. Dülsen, *A high data rate readout system for particle detectors based on FPGA-to-server ethernet connections and the eXpress Data Path technology*, https://cds.cern.ch/record/2779997.

[10] T.P. Morgan, *A Deep Dive Into AMD’s Rome Epyc Architecture*, https://www.nextplatform.com/2019/08/15/a-deep-dive-into-amds-rome-epyc-architecture/ visited on 11/06/2020.

[11] T. Göhring, *Performance Measurements of High-Bandwidth Transmission between FPGAs and Server Computers*, CERN-THESIS-2020-212.