PolyDL: Polyhedral Optimizations for Creation of High Performance DL primitives

SANKET TAVARAGERI, Intel Labs
ALEXANDER HEINECKE, Intel Labs
SASIKANTH AVANCHA, Intel Labs
GAGANDEEP GOYAL, IIT Hyderabad
RAMAKRISHNA UPADRASTA, IIT Hyderabad
BHARAT KAUL, Intel Labs

Deep Neural Networks (DNNs) have revolutionized many aspects of our lives. The use of DNNs is becoming ubiquitous including in softwares for image recognition, speech recognition, speech synthesis, language translation, to name a few. The training of DNN architectures however is computationally expensive. Once the model is created, its use in the intended application – the inference task, is computationally heavy too and the inference needs to be fast for real time use. For obtaining high performance today, the code of Deep Learning (DL) primitives optimized for specific architectures by expert programmers exposed via libraries is the norm. However, given the constant emergence of new DNN architectures, creating hand optimized code is expensive, slow and is not scalable.

To address this performance-productivity challenge, in this paper we present compiler algorithms to automatically generate high performance implementations of DL primitives that closely match the performance of hand optimized libraries. We develop novel data reuse analysis algorithms using the polyhedral model to derive efficient execution schedules automatically. In addition, because most DL primitives use some variant of matrix multiplication at their core, we develop a flexible framework where it is possible to plug in library implementations of the same in lieu of a subset of the loops. We show that such a hybrid compiler plus a minimal library-use approach results in state-of-the-art performance. We develop compiler algorithms to also perform operator fusions that reduce data movement through the memory hierarchy of the computer system. Using Convolutional Neural Network (CNN) models, we demonstrate that our approach automatically creates high performing DNN building blocks whose performance matches the performance of hand crafted kernels of Intel’s oneDNN library on high end CPUs. At the same time, our techniques take only a fraction of time (1/20 or less) compared to AutoTVM, a deep learning auto-tuner to create optimized implementations.

1 INTRODUCTION

Deep learning has revolutionized many spheres of human activity, examples of which include, speech recognition [26], image recognition [25, 31], web search [1], language translation [44], conversational artificial intelligence [17] etc. Training and inference using deep neural networks (DNNs) that lie at the heart of Deep Learning (DL) are computationally intensive tasks. In today’s datacenters, predominantly CPUs are used for inference tasks partly due to latency considerations. According to a recent McKinsey study [7], CPUs account for 75% of the inference market. Software frameworks such as TensorFlow, and PyTorch have been created to allow data scientists to write high performance deep learning code in an efficient manner. However, all these frameworks use manually optimized primitives to deliver high performance.

Given the ubiquity of CPUs and their widespread use for inference in deep learning applications, in this work we focus on automatically creating high performance implementations of DL primitives on CPU platforms. Creating a high performance implementation of a DL primitive requires that the code is parallelized in a load balanced fashion to take advantage of the multiple cores. Within a
single core, the code should be cache friendly: this often means the loops of the code are tiled so that effective data reuse out of different levels of cache (L1, L2, and L3) is possible. Tiling/blocking program transformation [9] facilitates data reuse from caches and therefore masks the long latency of fetching data from the main memory. Additionally, CPUs feature wide SIMD/vector units. Therefore, the loops should be adequately vectorized. Oftentimes, the different transformations mentioned are intertwined and that presents challenges for the compiler to produce fully optimized code automatically. Existing automatic compilation, and auto-tuning techniques [4, 6, 9, 10, 12, 14, 15, 23, 29, 34, 38–40] are either 1) inadequate to generate code that matches the performance of hand-tuned library implementations – later on in the paper we show that the state-of-the-art compiler generated code can lag library implementations by as much as ~10X or more, or 2) expensive – it would require running of 1000s of code versions to discover the best performing version and yet, fall short of reaching the peak performance of the machine. The main reason for the failure of automatic compilation techniques in achieving very high performance levels needed is that the sophistication in the CPU microarchitecture has increased over successive generations of CPUs (data prefetching, speculative execution, vector units, deep memory hierarchies, complex cache replacement algorithms etc). Consequently, the cost functions used to optimize code are unable to capture the nitty-gritties of the underlying architectures, and therefore are unable to derive the most effective execution schedules. Auto-tuning is an alternative approach where one explores a large number of program variants and selects the best performing version, sidestepping the complexity of defining a cost function that adequately models the intricacies of the underlying hardware architecture. However, auto-tuning is expensive and furthermore, it may fall short of manually created library in performance as our study shows later on in the paper with respect to AutoTVM [12], a deep learning auto-tuning system. We characterize the performance, productivity trade-off qualitatively in Figure 1.

At the one end of the spectrum, expert coded primitives such as that of Intel oneDNN library attain high performance at the cost of productivity – expert programmers have to hand craft the logic of the primitives for the target architectures. Autotuning systems ease the burden on programming to an extent but do not attain highest levels of performance. Using functionally correct code with vendor supplied compilers is most productive but comes at the expense of performance. Our work – PolyDL is close to attaining the highest levels of performance at the same time being most productive.

It has been shown that 95% of all deep learning applications running in the data centers today have a recurring pattern in their inner most loops, namely blocked matrix multiplication [19, 28]. We decompose the overall DL primitive optimization problem into two parts: 1) efficient parallelization of the code and discovering a structure of the loops that uses the multi level caches well, and 2) effective vectorization of the code for a high degree utilization of the vector units. In this paper, we develop a novel polyhedral model based data reuse algorithm to derive load balanced parallel
loops and cache friendly execution schedules. For the latter i.e., to use the vector units optimally, we develop a flexible framework where the inner most loops of kernels can be replaced with microkernels, i.e., manually optimized library implementations. As the number of recurring patterns in the inner most loops of DL primitives is small, our hybrid approach is more scalable because the number of microkernels that the expert programmers have to create is small as well. Thus, the problem of DL library development will now be reduced to hand coding a few microkernels as opposed to hand coding each of the large number of DL primitives.

To account for the sophisticated memory hierarchy, we use a code-generator to create a number of program variants - \( n \) in number - for a given program. The generated code variants are then analyzed by our novel data reuse algorithm – PolyDL to characterize their cache behavior. We have developed a relative ranking algorithm which ranks the \( n \) variants based on their potential performance. The top \( k \) variants are selected and are run on the target hardware and the best performing program version is discovered. Thus, PolyDL narrows down the number of variants to actually run on the target architecture from \( n \) to a small, manageable \( k \) \((k << n)\). Through our experimental evaluation on convolutions of a range of popular and the state-of-the-art image recognition models, we show that the top variant (a single variant) picked by our compilation machinery is one of the best performing variants, and the realized performance is close to and in many cases, higher than that of Intel’s oneDNN library [3] (formerly known as MKL-DNN), a hand-tuned library for deep learning kernels. Additionally, we develop a fusion algorithm that “fuses” element-wise operators with their preceding or succeeding compute-intensive operators. Such patterns where a computationally heavy operator such as convolution is succeeded by element-wise operators such as ReLU, occur frequently in DL workloads. Therefore, the DL domain specific fusion algorithm that we develop will increase the overall performance by reducing the extra memory traffic that the element-wise operators would otherwise incur.

The contributions of the paper are the following:

- We present a novel cache data reuse analysis to characterize a loop nest’s behavior with respect to a multi-level cache hierarchy.
- We describe a methodology to rank program variants in terms of performance using the compiler generated statistics and the system parameters, i.e., cache sizes. To this purpose, we develop two ranking techniques: one, a heuristic for ranking and two, a DNN based approach.
- We develop a deep learning domain specific operator fusion algorithm.
- We conduct extensive experiments comparing our technology with the Intel oneDNN library and with AutoTVM. The experiments show that we are able to match the performance of expert coded DL primitives in the oneDNN library and exceed the performance of the ones discovered by AutoTVM via extensive auto-tuning.

To the best of our knowledge, this is the first work that examines automatic compilation techniques and the use of microkernels in an integrated fashion. The rest of the paper is organized as follows. We motivate the need for derivation of automatic execution schedules for loops in Section 2. Section 3 describes preliminary concepts that will be used in developing the compiler algorithms. In Section 4, we develop algorithms for compiler-time selection of top performing code version(s). We present a cache data reuse analysis and a poly-ranking system to rank the candidate program variants in terms of performance. The operator fusion algorithm is expounded in Section 5. Section 6 details the experimental evaluation conducted. The related work is discussed in Section 7 while Section 8 presents the conclusions from this work.
2 MOTIVATION

The deep learning primitives are computationally intensive and most of the neural network training and inferencing time is spent in them. However, for different layers of the deep neural networks, the optimizations (e.g., loop order, tile sizes in tiled code etc) that need to be applied are different. Using a version of the code optimized for one layer of a neural network for all others can yield poor performance for the overall neural network. It is this need for custom optimization for different layers of neural networks (the number of layers in a deep neural network can be large) that makes generating efficient code for deep learning primitives a challenging problem. To illustrate the need for such tailored loop optimizations we consider the convolution layers of the Fast R-CNN model [21], one of the leading image recognition CNN models. We generate four variants of convolution code which differ only in the loop order and the rest of the loop structure remains the same for all of them (more details are provided in §6) and measure performance on a 28-core Intel(R) Xeon(R) Platinum 8280 (a.k.a Cascade Lake) CPU server. Figure 2 shows the normalized performance of the code variants on 25 convolution layers of Fast R-CNN: the performance is normalized with respect to the highest performing code among the four variants.

From Figure 2, we observe that the performances of different versions of the code vary widely from layer to layer. A convolution layer differs from another convolution layer in problem sizes – image sizes, channel widths, filter sizes, strides, and padding. The code version v2 has the best performance from layer 1 through 19, and is subpar from layer 20 through 25. The efficiencies of the other versions viz., v1, v3, and v4 are much more widely varying. Using the compiler technology we have developed – PolyDL that we detail in the rest of the paper, we are able to effectively analyze the four code variants and pick the best performing variant for each layer. The performance achieved by PolyDL picked code shown in Figure 3 is close to the highest performance among the four variants for all 25 layers of Fast R-CNN. Thus using the PolyDL system, using compile-time static analysis alone, we are able to automatically identify and apply the loop optimizations required for each layer of a deep neural network in order to achieve high performance.

3 PRELIMINARIES

3.1 Notation

We use the polyhedral model [18], which is an advanced mathematical framework to reason about dependences and loop transformations, to develop our data reuse algorithm. We use the Integer Set Library [41] for performing polyhedral operations in this work and we use the same notation as used in ISL to elucidate the concepts and the algorithm. The matrix multiplication code shown in Figure 4 will be used to illustrate the workings of the data reuse analysis.
for (i = 0; i < M; i++) {
    for (j = 0; j < N; j++) {
        for (k = 0; k < K; k++) {
            C[i][j] += A[i][k] * B[k][j];
        }
    }
}

Fig. 4. Matrix multiplication code

Sets. A set is a tuple of variables $x_i$s along with a collection of constraints $c_k$s defined on the tuple variables. $s = \{[x_1, \ldots, x_n] : c_1 \land \ldots \land c_m\}$

The iteration spaces of loop nests are represented by sets. The iteration space of the loop in Figure 4 is defined as the following set.

$I = \{S[i, j, k] : 0 <= i < M \land 0 <= j < N \land 0 <= k < K\}$

Relations. A relation is a mapping from input tuple variables $x_i$s to output tuple variables $y_j$s. In addition, a set of constraints $c_k$s can be defined for a relation that will place constraints on the input/output tuple variables.

$r = \{[x_1, \ldots, x_n] \mapsto [y_1, \ldots, y_m] : c_1, \ldots, c_p\}$

The read and write access functions of a loop nest can be modeled with relations. The read relations in the Figure 4 code are shown below.

$r_1 = \{S[i, j, k] \mapsto C[i, j]\}$

$r_2 = \{S[i, j, k] \mapsto A[i, k]\}$

$r_3 = \{S[i, j, k] \mapsto B[k, j]\}$

The sole write relation in the loop is:

$w_1 = S[i, j, k] \mapsto C[i, j].$

The domain of a relation $r$ is denoted by $\text{dom} \ r$.

Apply operation. When a relation $r$ is applied on a set $s$, the domain of $r$ will be intersected with $s$ and the resulting range will be a new set $s'$. The set $s'$ is said to be the result of the apply operation. The operation is mathematically defined as: $(\forall y \in s') \iff (\exists x \text{ s.t. } (x \in s \land x \mapsto y) \in r)$

The data footprint of the loop can be computed by applying read and write relations on the iteration space set: $r_1(I) \cup r_2(I) \cup r_3(I) \cup w_1(I)$

Lexicographic operations. The lexicographical operations can be applied on sets. $s_1 << s_2$ outputs all the elements of $s_1$ that are lexicographically strictly smaller than all the elements of $s_2$, while $s_1 <= s_2$ gets us the elements of $s_1$ that are lexicographically smaller than or equal to the elements of $s_2$. The lexicographically smallest element of a set $s$ is queried using lexmin $s$. Similarly, the lexicographically largest element is obtained using lexmax $s$.

Set difference. The set difference between set $s_1$ and $s_2$ is denoted by $s_1 - s_2$, i.e., the resulting set will have elements of $s_1$ that do not appear in $s_2$.

3.2 Polyhedral dependences

The exact data dependences in loop nests can be computed in the polyhedral model and are expressed as maps from source iterations to target iterations involved in the dependence. For cache data reuse analysis developed in §4, we consider four kinds of dependences – Read-After-Read (RAR), Read-After-Write (RAW, a.k.a flow), Write-After-Read (WAR, a.k.a anti), and Write-After-Write (WAW). The data dependencies of the matrix multiplication code in Figure 4 are shown below.
\[d_1 = \{S[i, j, k] \mapsto S[i', j', k'] : i' = i \land j' = j \land k < k' < K\}\]
\[d_2 = \{S[i, j, k] \mapsto S[i', j', k'] : i' = i \land k' = k \land j < j' < N\}\]
\[d_3 = \{S[i, j, k] \mapsto S[i', j', k'] : j' = j \land k' = k \land i < i' < M\}\]

The dependence \(d_2\) is induced by array reference \(A[i][k]\). An element of array \(A\), say \(A[0][0]\) which is accessed in source iteration \([i = 0, j = 0, k = 0]\) gets reused in target iterations \([i' = 0, j' > 0, k' = 0]\). The source to target iteration relationships such as this are expressed in a parametric fashion as the relation \(d_2\).

4 Compile Time Selection of Top Performing Code Version

The input to our compiler tool is the loop nest to be optimized – \(L\) along with the microkernel that forms the inner-most loops. Figure 5 shows the overall system design. The loop based specification of the microkernel – \(M\) is substituted in the code for further analysis. The resulting loop structure – \(L'\) is regular. The code generator takes the loop nest \(L'\) and generates a large number of program variants while keeping the inner most loops that correspond to \(M\) intact. For each generated code variant, the working set sizes are computed as described in §4.1. The statistics calculated for all the variants are then input to the poly-ranking algorithm described in §4.2 and it picks the top \(k\) best performing versions. The original microkernels are inserted back into the code of the \(k\) picks. The top performing variants selected analytically are now run on the target architecture and best performing code among the \(k\) loop nests is determined.

Microkernel Specification

The microkernel function call is annotated with a pragma compiler directive which contains the loop-based functionally equivalent code. The microkernel function call is substituted with the loop based code for the compiler analysis in a pre-processing pass. When the cache data reuse analysis and ranking of the code variants are done, in a post-processing pass, the loop-based inner most loops are replaced with the call to the microkernel.

We assume that the data accessed by the microkernel’s equivalent loop based code and by the implementation of the microkernel are the same. The order of the loops within the microkernel implementation could be potentially different. There is no assumption on how the microkernel is implemented. The only assumption is that the data set accessed should be the same.

4.1 Working set size computation

We develop a polyhedral model based cache data reuse analysis to characterize a loop-nest’s behavior with respect to a given cache hierarchy. The analysis computes the various existing data reuses of a program and then for the input cache hierarchy determines which data reuses are exploitable at various levels of cache.
Algorithm 1: Compute working set sizes

Input: Loop nest: $\mathcal{L}$
Output: The working set sizes: $W_{\text{Sall}}$

1. [Iteration space: $I$, Read relations: $r_{\text{read}}$, Write relations: $r_{\text{write}}$, Schedule: $\delta$] ← Parse the loop nest $\mathcal{L}$
2. $\mathcal{D}_{\text{RAR}}, \mathcal{D}_{\text{RAW}}, \mathcal{D}_{\text{WAR}}, \mathcal{D}_{\text{WAW}}$ ← Compute read-after-read, read-after-write, write-after-read, write-after-write dependences of $\mathcal{L}$
3. $\mathcal{D}_{\text{all}} ← \mathcal{D}_{\text{RAR}} \cup \mathcal{D}_{\text{RAW}} \cup \mathcal{D}_{\text{WAR}} \cup \mathcal{D}_{\text{WAW}}$
4. $W_{\text{Sall}} ← \emptyset$
5. /* Iterate through all dependences to compute the working set sizes */
6. for $d \in \mathcal{D}_{\text{all}}$
7.   /* The dependence spans iterations of the parallel loop(s) */
8.     $i_p ←$ The outermost parallel iterator in dom $d$
9.     $I_{\text{par}} ←$ Parameterize iterators outer to $i_p$ in $I$
10.    $W_{\text{Spar}} ← |r_{\text{read}}(I_{\text{par}}) \cup r_{\text{write}}(I_{\text{par}})|$
11.    Add $W_{\text{Spar}}$ to $W_{\text{Sall}}$
12. else /* The dependence spans iterations of the sequential loops */
13.     $I_{\text{source}} ←$ lexicmin dom $d$
14.     $I_{\text{min\_tar}} ←$ lexicmin $d(I_{\text{source}})$
15.     $I_{\text{max\_tar}} ←$ lexicmax $d(I_{\text{source}})$
16.     $I_{\text{min\_WS}} ← (I \ll I_{\text{min\_tar}}) − (I \ll I_{\text{source}})$
17.     $I_{\text{max\_WS}} ← (I \ll I_{\text{max\_tar}}) − (I \ll I_{\text{source}})$
18.     $W_{\text{Smin}} ← |r_{\text{read}}(I_{\text{min\_WS}}) \cup r_{\text{write}}(I_{\text{min\_WS}})|$
19.     $W_{\text{Smax}} ← |r_{\text{read}}(I_{\text{max\_WS}}) \cup r_{\text{write}}(I_{\text{max\_WS}})|$
20.    Add $W_{\text{Smin}}$ and $W_{\text{Smax}}$ to $W_{\text{Sall}}$

Each data dependence in a loop is also a case of data reuse – the source and target iterations involved in the dependence touch the same data element and therefore, the data is reused. For a data dependence and hence data reuse to be realizable in a given level of cache, all the data elements accessed between the source and target iterations of the dependence – the working set – have to be retained in the cache so that when the execution reaches the target iteration, the data element(s) used in the source iteration will still be present in the cache.

Algorithm 1 computes all the working sets of the input loop nest. First, the input C source file is parsed using the Polyhedral Extraction Tool (PET) [42] to obtain the polyhedral representation of the program, namely iteration space of the loop nest, read and write relations and the schedule (line 1). The exact (and not transitive) RAR, RAW, WAR, WAW dependences are then computed and a union of all the four kinds of dependences is formed (line 2 and 3). The task now is to compute the working set size for each dependence which is carried out from line 6 through 19.

We distinguish between the data dependences that span parallel iterations and those that do not. The working set sizes for the two kinds of dependences are computed differently. If a dependence spans a parallel loop and the data set used in the entire set of parallel iterations is held in the given level of cache, then the data reuse is guaranteed to happen out of that cache. This is because, irrespective of the order of execution of the iterations of the parallel loop, the data accessed by the source and target iterations will be present in the cache as the cache is big enough to hold the entire set of data elements accessed by all parallel iterations collectively. The working set for such a dependence is calculated by parameterizing the iterations outer to the parallel loop variable and evaluating the size of the read and write sets within the parameterized iteration set (line 7 to 9).

For the data dependences that span sequential loops, we compute the working set size as follows. We consider a representative source – the first iteration (lexicographically) of all the source iterations of a dependence (line 12). We can now compute the target iterations for the lexicographically first/minimum iteration. If the data element that is used in the source iteration is used in multiple
We have built a code generator to emit a number of program variants. The code generator creates as far as array A is concerned, the poly-ranking system considers caches at different levels (typically L1, L2, and L3) and for each target iteration are determined (line 15). Similarly, iterations between the source and the last target iteration are derived (line 16). The working sets will be the union of all the read and written data elements between the source and the first/last iterations of the target iteration set (line 17 and 18). Correspondingly, for each dependence we compute two working set sizes – \( W_{S_{\min}} \) and \( W_{S_{\max}} \), if there are multiple target iterations for a source iteration in a given dependence. What this means is, in order to be able to exploit at least one data reuse arising from the dependence \( d \), the cache memory should be capacious enough to hold at least \( W_{S_{\min}} \) data elements. If all the data reuses are to be realized – till the last target iteration, then the cache should of size equal to or greater than \( W_{S_{\max}} \) times the datatype size.

We illustrate the operation of the algorithm using the running example in Figure 4. Let us examine the following dependence carried by the \( j \) loop arising because of the array reference \( A[i][k] \); \( d_{2} = \{ S[i, j, k] \leftrightarrow S[i', j', k'] : i' = i \land k' = k \land j < j' < N \} \). Of all the source iterations, the first/lexicographically minimum iteration is: \( I_{\text{source}} = \{ S[i = 0, j = 0, k = 0] \} \). Its target iterations are: \( \{ S[i = 0, j, k = 0] : 0 < j < N \} \). Among the target iterations, the first one is: \( I_{\text{min\_tar}} = \{ S[i = 0, j = 1, k = 0] \} \) and the last one is: \( I_{\text{max\_tar}} = \{ S_{\max}[i = 0, j = N - 1, k = 0] \} \)

The number of data elements of the three arrays – A, B, C accessed between \( I_{\text{source}} \) and \( I_{\text{min\_tar}} \) is derived by applying the read and write relations on the intervening iteration set and it is:

\[
W_{S_{\min}} = 2K + 3
\]

The \( K \) elements of array A – \( A[0][0, 1, \ldots, K - 1] \), the \( K + 1 \) elements of array B – \( B[0, 1, \ldots, K - 1][0] \) and \( B[0][1] \), and finally 2 elements of array C – \( C[0][0], C[0][1] \) accessed between the source iteration \( S[i = 0, j = 0, k = 0] \) and the target iteration \( I_{\text{min\_tar}} = S[i = 0, j = 1, k = 0] \) lead to the \( W_{S_{\min}} \) size of \( 2K + 3 \).

The maximum working set size – the size of the data touched between \( I_{\text{source}} \) and \( I_{\text{max\_tar}} \) is:

\[
W_{S_{\max}} = N \times K + N + 1
\]

The \( W_{S_{\max}} \) size is arrived at by counting the number of array elements accessed between the source iteration - \( S[i = 0, j = 0, k = 0] \) and the target iteration - \( I_{\text{max\_tar}} = \{ S_{\max}[i = 0, j = N - 1, k = 0] \} \). As far as array A is concerned, \( K \) elements of it – \( A[0][0, 1, \ldots, K - 1] \) are read. Array B’s elements – \( B[0, 1, \ldots, K - 1][0, 1, \ldots, N - 2] \) plus \( B[0][N - 1] \) are read which total \( K \times (N - 1) + 1 \). \( N \) elements of array C are read and written – \( C[0][0, 1, \ldots, N - 1] \). Therefore, a total of \( N \times K + N + 1 \) are read and written.

### 4.2 Poly-ranking algorithm

We have built a code generator to emit a number of program variants. The code generator creates the loop variants by applying tiling and loop interchange program transformations. The tile sizes are varied as well. The working set size computation analysis – §4.1 is performed on each program version generated. Among the many variants generated, the poly-ranking algorithm described below picks the top \( k \) best performing versions, where \( k \) is a parameter. In this work, we pick the top 1 variant the code generator produces, i.e., \( k = 1 \). That is, a single version is selected.

We assume fully associative, and exclusive caches. If the working set size corresponding to a data reuse in the program is smaller than the cache size then the data reuse is exploitable in the cache. The poly-ranking system considers caches at different levels (typically L1, L2, and L3) and for each data reuse, determines at what level of cache hierarchy is the data reuse realizable. Algorithm 2

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Algorithm 2: Compute working set sizes w.r.t cache sizes

| Input: The working set sizes: $WS_{all}$.
| Cache sizes: $Size_{L_1}, \ldots, Size_{L_n}$.
| Output: Working set sizes per cache: $WS^{L_i}$ for $i = 1, \ldots, n$.
| Memory working set size: $WS^{mem}$.
| 1. Initialize $WS^{L_i}$ to 0 for $i = 1, \ldots, n$.
| 2. Sort working set sizes in $WS_{all}$ from smallest to largest.
| 3. for $WS_j \in WS_{all}$ do
| 4. for $Size_{L_i} \in Size_{L_1}, \ldots, Size_{L_n}$ do
| 5. if $(WS_j + WS^{L_i}) \leq Size_{L_i}$ then
| 6. $WS^{L_i} = WS^{L_i} + WS_j$.
| 7. break.
| 8. Add the working sets $WS_j \in WS_{all}$ that do not fit any cache to $WS^{mem}$.

shows the steps to determine the cumulative working set sizes at each level of cache. The inputs to the algorithm are the working set sizes computed for a loop nest, and the cache sizes of the target system. The algorithm determines the fastest level of cache where the working set size corresponding to each data reuse fits and adds it to that cache’s working set size. The working set sizes that fit in a particular level of cache $L_i$ are denoted by $WS^{L_i}$. If a working set does not fit in any cache, then the data reuse happens out of the main memory. Consequently, the memory’s working set size is updated.

4.2.1 Performance cost model based ranking. The running time of the loop is directly related to the latency of the cache where the data reuse occurs as well as the working set size. Furthermore, the running time is inversely related to the bandwidth of the cache. Based on these observations, we define the following cost function:

$$C = \sum_{L_i} WS^{L_i} \times \frac{lat^{L_i}}{bw^{L_i}} + WS^{mem} \times \frac{lat^{mem}}{bw^{mem}} \quad (1)$$

The latency of cache $L_i$ is $lat^{L_i}$ while its bandwidth is denoted by $bw^{L_i}$. For each code variant generated, we run the cache data reuse analysis and calculate the above cost function. Then, the variants are ranked in the decreasing order of the value of the cost function. The working set size at cache level is multiplied with that cache’s latency and divided by its bandwidth. The multiplicands are then added together. The lower the value of the cost function, the higher is its presumed performance, and higher is its rank.

4.2.2 DNN-based ranking algorithm. We explore the use of deep neural networks (DNNs) for ranking of code variants. For the purposes of training the DNN model, we collect the performance
data of code variants generated and the statistics as outputted by Algorithm 2 – working set sizes at different levels of the memory hierarchy.

We train the DNN model to perform relative ordering of two code variants. We then use a tournament based ranking system to assign ranks to the different code versions created – we play each code variant against every other code variant. For each variant, we record the number of wins it has accumulated. We then rank the variants based on the number of wins – the higher the number of wins, the higher the rank.

We use a four layer feed forward neural network architecture shown in Figure 6. We normalize the compiler generated statistics of two code variants in the following fashion and input them to the DNN. We sum the working set sizes of the two variants together:

\[ \text{sum} = W_{S_{v1}} + W_{S_{v1}}^{L1} + W_{S_{v1}}^{L2} + W_{S_{v1}}^{L3} + W_{S_{v1}}^{mem} + W_{S_{v2}} + W_{S_{v2}}^{L1} + W_{S_{v2}}^{L2} + W_{S_{v2}}^{L3} + W_{S_{v2}}^{mem} \]

and divide the individual statistic by this sum. The rationale for considering the sum of the two statistics together is that if one of the variants is creating higher volume working set sizes then its statistics should appear bigger to the DNN. This is because the smaller the working set sizes, we can expect higher performance. Therefore, for the DNN to learn the relative performances of the two variants, it is crucial that it sees the relative sizes of the working set sizes. Normalizing each variant individually (by considering the sum of statistics of one variant alone) would not bring out the differences in the absolute values of the working set sizes of the two variants at different cache levels. The output layer consists of two neurons and we use the softmax function for the output layer. The values of the two output neurons, because of the use of the softmax function, sum to 1. If the output value is above a threshold - \( \theta \), we consider it a 1, otherwise a 0. If the first neuron fires a 1, then the first variant is considered the winner. If the second neuron fires a 1, then the second variant is considered the winner. If both of them are zero because none of them are above the threshold, then it is a draw between the two variants. In this work, we set the threshold \( \theta \) to 0.6. We experimented with deeper models as well. However, the depth beyond four layers did not have any discernible effect on accuracy.

5 OPERATOR FUSION

Algorithm 3: Perform operator fusion

| Input: | Loops of computationally heavy operator: \( \text{op}_{hy} \), loops of element-wise operator \( \text{op}_{ew} \) |
| Output: | Fused operator: \( \text{op}_{fused} \) |

1. \( W_{hy} \leftarrow \text{the write set of } \text{op}_{hy} \)
2. \( W_{ew} \leftarrow \text{the write set of } \text{op}_{ew} \)
3. \( \text{op}_{fused} \leftarrow \emptyset \)
4. if \( W_{hy} = W_{ew} \) then
5. if \( |I_{ew}| = |W_{ew}| \) then
6. if No writes or reads to any element of \( W_{hy} \) between \( \text{op}_{hy} \) and \( \text{op}_{ew} \) then
7. // We will now fuse the two ops
8. \( I_{ew} \leftarrow \text{instructions in the innermost loops of } \text{op}_{ew} \)
9. \( \text{op}_{fused} \leftarrow \text{Apply index set splitting on } \text{op}_{fused} \)
10. \( \text{op}_{fused} \leftarrow \text{Insert } I_{ew} \text{ in the last iteration of } \text{op}_{hy} \text{‘s reduction loops} \)
11. if \( \text{op}_{fused} = \emptyset \) then
12. // We will return the original loop nests
13. \( \text{op}_{fused} \leftarrow \{ \text{op}_{hy}, \text{op}_{ew} \} \)

Often, in the DNN architectures, a heavy operator (where most of the compute cycles are spent) is followed by activation functions which are element-wise operators. The output of the heavy operator is processed by the activation functions such as ReLU, Sigmoid etc. in an element-wise fashion, i.e., without involving any reduction. The element-wise operator is mainly a memory
bound operator, fused with the heavy operator in order that the extra data movement through the
memory hierarchy that would otherwise be necessitated by the element-wise operator is eliminated.

Algorithm 3 presents a generic algorithm that fuses a heavy operator with the subsequent
element-wise operator. The following conditions have to be met for an element-wise operator $op_{ew}$
to be fused with the arithmetically intensive, heavy operator $op_{hy}$:

- The two operators — $op_{ew}$ and $op_{hy}$ should be writing to the same set of elements (line 4 in
  the algorithm).
- The element wise operator $op_{ew}$ should be writing to each array element only once. We check
  if the cardinality of the iteration space of $op_{ew}$ is equal to the cardinality of the write set of
  $op_{ew}$ (line 5). This check will confirm that $op_{ew}$ is indeed an element-wise operator and does
  not involve a reduction.
- The operator $op_{hy}$ should be immediately followed by $op_{ew}$ without any intervening code.
  Or, if there is any code between the two operators, it should not be writing to or reading
  from the write set of the two operators (line 6).

Once the aforementioned conditions are met, the instructions of $op_{ew}$ are inserted in the last
iteration of $op_{hy}$ operator’s reduction loops subsequent to the instructions of $op_{hy}$ (line 9). To reduce
the overheads stemming from the conditional checking if an iteration of the $op_{hy}$ operator’s loops
is the last iteration of the reduction loops, we apply index set splitting transformation to peel the
last iteration from the rest of the iterations.

A symmetric analysis can be applied to fuse an element-wise operator with a subsequent heavy
operator as well. In that case the operation of the element-wise operator will be fused with the first
iteration of the heavy operator’s reduction loops.

6 EXPERIMENTAL EVALUATION

We conduct experiments to evaluate the efficacy of the PolyDL system in its ability 1) to derive high
performance primitives, and 2) to create efficient fused operators. The aims of PolyDL are two-fold:
one, to achieve performance competitive with manually optimized code, and two, to do so with
compile-time analyses alone without requiring auto-tuning which can be expensive. Accordingly,
we gauge the performance of PolyDL against a state-of-the-art library created specifically for deep
learning networks – the latest version of Intel oneDNN [3] viz., v1.4. We also compare PolyDL’s
performance with AutoTVM system’s. AutoTVM system is an auto-tuning system – it generates a
large number of program variants, runs them on the target architecture, and identifies the best
performing variant.

6.1 Set up

In this work, we evaluate the performance benefits of the PolyDL system on CPUs for inference
tasks. The forward pass convolution operation, batch-normalization, and ReLU and its variants
form the bulk of the compute of inference CNN models for image recognition. Therefore, we focus
on them in our experimental evaluation.

We use the PolyDL system to optimize the convolutions of Resnet-50 [25], Fast R-CNN (fastrcnn)
[21], Mask R-CNN (maskrcnn) [24], Xception (xception) [13], You Only Look Once v2 (yolov2) [33],
MobileNets (mobilenet) [27], AlexNet (alexnet) [32], OverFeat (overfeat) [35] GoogLeNet v1 and
v3 [37], and (googlenetv1, googlenetv3), the popular and the state-of-the-art image recognition
neural network models. We also measure the performance of the same convolutions using the
implementations from the Intel oneDNN library and those obtained via auto-tuning with the
AutoTVM system.
We evaluate the benefits of operator fusion algorithm presented in the paper on two sequences: 1) batch normalization followed by the activation function ReLU, 2) convolution followed by the activation function ReLU6, which is a variant of ReLU. The activation function ReLU is defined as: $y = \max(x, 0)$, while ReLU6 is defined as $y = \min(\max(x, 0), 6)$ [30], that is, the output value is capped at 6.

The experiments are run on the latest Intel servers – Intel(R) Xeon(R) Platinum 8280 (Cascade Lake) CPU servers running at the frequency of 2.70 GHz. Each processor has 28 cores, 32KB private L1 cache, 1MB private L2 cache, and 39MB shared L3 cache.

### 6.2 Evaluation of Compile Time Selection of Top Performing Code Version

```c
#pragma omp parallel for private(ofm_tile, ifm_tile, ij, oj, kj, ki, ii)
for (img = 0; img < imgn; ++img) {
  for (ofm_tile = 0; ofm_tile < nOfm / GEMM_BLOCK; ++ofm_tile) {
    for (ifm_tile = 0; ifm_tile < nIfm / GEMM_BLOCK; ++ifm_tile) {
      for (oj = 0; oj < ofh; ++oj) {
        ij = oj * STRIDE_H;
        for (kj = 0; kj < kh; ++kj) {
          for (ki = 0; ki < kw; ++ki) {
            /* GEMM operation begins */
            for (oi = 0; oi < ofw; ++oi) {
              ii = oi * STRIDE_W;
              for (ofm = 0; ofm < GEMM_BLOCK; ++ofm) {
                for (ifm = 0; ifm < GEMM_BLOCK; ++ifm) {
                  output[img][ofm_tile][oj][oi][ofm] +=
                    filter[ofm_tile][ifm_tile][kj][ki][ifm][ofm] *
                    input[img][ifm_tile][ij+kj][ii+ki][ifm];
                }
              }
            }
            /* GEMM operation ends */
          }
        }
      }
    }
  }
}
```

Fig. 7. The 2-D Convolution code

Figure 7 shows the convolution code. The shown code is data tiled in the input and output channel dimensions. The convolution code has a matrix multiplication operation (denoted GEMM in the code) embedded in it. We use the performance obtained using the code shown in 7 as the baseline. The GEMM (matrix multiplication) operation will be replaced with a call to a library implementation of matrix multiplication. We use the LIBXSMM [2] implementation for matrix multiplication – the microkernel.

PolyDL performs outer loop optimization around the call to the matrix multiplication microkernel by loop reordering and tiling using various tile sizes. We show the performance obtained by inserting the LIBXSMM microkernel in the code listed in Figure 7 under the banner of Microkernel in the subsequent performance graphs. Comparing the performance of Microkernel with PolyDL will show the need to perform outer loop tuning as done by PolyDL to obtain high performance for all layers and for all models. Depending on the tensor sizes, we generate different number of code variants for each layer. The number of variants generated varies from 5 to 21. This is because, the number of tile sizes we can explore is a function of the tensor sizes. We generate a larger number of variants for convolutions on larger tensors and fewer variants for convolutions on smaller tensors. On average, for each layer, 11 versions are generated. Consequently, the task of the PolyDL system is to rank the generated variants based on performance. Each program is run a 1000 times and the average performance across those runs is reported in the paper. The programs are compiled with Intel icc compiler 19.0.3.199.
The machine has a 512-bit SIMD vector unit and supports AVX-512 vector instructions. Consequently, 16 floating point arithmetic operations can be performed at a time (each floating point number is 32 bits long, and therefore, 16 floating point numbers make up 512 bits: $32 \times 16 = 512$). Since the microkernel vectorizes along the input and output channel loops ($i f m$ and $o f m$ loops in the code), to fully utilize the vector unit, the input and output channel widths have to be 16 or multiples of 16. In the CNN models considered, 86% of the convolutions meet this criterion and those convolutions are selected for experimental evaluation. The peak single precision floating point performance of a Cascade Lake processor is ~3,300 GFLOPS/s. We set the mini-batch size to 28 and use data parallelism: the convolution operator is applied on 28 images simultaneously.

To train a DNN model for performing ranking of code variants as described in §4.2.2, we use 70% of the experimental data collected (to avoid overfitting) – that is, performance data of 70% of the code versions generated are used to form the training data set. We create a single DNN model using data from all CNN models and use it to rank variants across the CNN models.

Figure 8 shows the performance in terms of GFLOPS/s (Giga Floating point Operations per second) of the baseline code, PolyDL, AutoTVM and oneDNN on convolutions of fastrcnn. The PolyDL performance shown is the performance of the top code variant selected using the cost modeling based poly-ranking algorithm described in §4.2.1. The performance of PolyDL vis-a-vis the baseline code is anywhere between 4X and 11X across layers. The higher performance of PolyDL is due to 1) the optimization of outer loops 2) the use of optimized GEMM microkernel for the inner loops. PolyDL performance is close to oneDNN’s. For some layers such as layer 11, PolyDL is 9% faster than oneDNN while for a few layers notably layer 1, and 3, oneDNN performs better. AutoTVM’s performance often lags that of PolyDL’s. The geometric average of GFLOPS/s numbers are also shown in the graph. They are 1965, 2322, and 2408 for AutoTVM, PolyDL, and oneDNN respectively.

Figure 9 shows the performance distribution for all layers of fastrcnn. The performance is normalized with respect to that of the best performing variant found empirically. The crux of the PolyDL technology presented in the paper is to rank a given set of code variants using compile-time static analysis. Therefore, the closer the performance of the PolyDL picked version is to the maximum performance seen by any code variant explored, the more efficacious the PolyDL algorithms are. In the graph, we show the minimum performance observed, the maximum performance seen, the performance of the variant with default loop order shown in Figure 7 with microkernel inserted – Microkernel, the performance of the code picked per the poly-ranking algorithm (§4.2.1) – PolyDL and the performance of the code picked per the DNN based ranking algorithm (§4.2.2) – PolyDL-DNN. Here, we see that the performance distribution is great: the difference between the performance of the best and the worst code variant seen is vast for all layers except layers 1, and 18.
We observe that PolyDL is able to pick a variant whose performance is close to the performance of the best performing version. In the case of fastrcnn, we see that PolyDL outperforms Microkernel significantly clearly showing the need for outer loop tuning in addition to having a high performance implementation of matrix multiplication in the inner most loops. PolyDL picked code achieves ~2X performance gains over the code with the default loop order for layers 4, 7, 8, 10, and 11 while for layer 25, PolyDL is 56% higher performing. Across all layers of fastrcnn, PolyDL improves the performance over the default loop order by 28% on average.

The performances achieved by different methods for the convolutions of resnet are shown in Figure 10. The performance of PolyDL over the baseline is 5X to 10X for all layers. In most cases, PolyDL closely matches the performance of oneDNN library. In several instances, PolyDL outperforms oneDNN, notably for layers with IDs 7, 11, 15, and 16 where the performance gain is over 10%. On some layers such as layer 1, oneDNN fares better. This is explained by customizations for specific problem sizes including insertion of careful data prefetching instructions in the oneDNN library code. In contrast, PolyDL’s approach is automatic and in the case of Resnet-50, we observe that we are able to attain the same performance levels as oneDNN overall. PolyDL is 14% higher performing than AutoTVM on average.

Figure 11 shows the performance distribution of code variants generated for each layer of Resnet-50. We note that the performance of the PolyDL version is close to the maximum performance in most layers save layer 9. Even though in terms of cache behavior (PolyDL primarily models the cache behavior), the variant selected by PolyDL may be the best, other factors such as prefetching, TLB behavior etc may cause its performance to be lower than those of other variants. The minimum performance seen i.e., the performance of the worst code variant, varies across layers – for layer 12 through 19, the minimum performance is much farther from the maximum performance. For the initial layers however, the different code variants generated perform similarly. For Resnet-50, performance levels of Microkernel and PolyDL are similar indicating that the original loop order shown in Figure 7 gets good performance. Even so, for layer 1, PolyDL is 7% higher performing than Microkernel. We observe that there is not a considerable difference in the performance achieved by the cost model based ranking method – PolyDL, and the DNN based ranking method – PolyDL-DNN.

From Figure 12 through Figure 27, we show the performance achieved by various systems and the performance distribution of code variants seen for all other CNN models, namely, maskrcnn, xception, yolov2, mobilenet, alexnet, overseat, googlenetv1, and finally googlenetv3. In Figure 12 we observe that the performances of two layers of maskrcnn – layer 31, and 32 are very low compared to the machine peak. The reason is, the image sizes for the two layers are 7X7 and 1X1 respectively. Consequently, the amount of work that each core has to perform is less and therefore, all three systems – AutoTVM, PolyDL, and oneDNN are not able to attain performance
close to the machine peak. For maskrcnn too, we discover that the default loop order – Microkernel, leaves a lot of performance on the table: for layers 4, 5, 6, 9, 10, 14, 15, PolyDL gets more than 2X
extra performance compared to only the use of the microkernel. For layer 7, PolyDL is 3X higher performing than Microkernel. Across all layers of maskrcnn, on average PolyDL is 1.29X faster compared to Microkernel. In Figure 15, we see that PolyDL-DNN picks the right variant for all layers of xception. For yolov2 from Figure 16, we note that PolyDL performance closely matches that of oneDNN. AutoTVM’s performance lags behind that of PolyDL’s and oneDNN’s. Through Figure 17, we see there is a great spread in performance of various code variants run. In mobilenet, PolyDL consistently outperforms AutoTVM and on average is 1.14X faster (Figure 18). Further, the different code variants perform very similarly for for layers 1, 3, 4, and 5 in mobilenet while the performance spread is greater for other layers (Figure 19). In alexnet, PolyDL achieves superior performance compared to both AutoTVM and oneDNN for all layers (Figure 20) and on average is 1.19X and 1.09X faster than AutoTVM and oneDNN respectively. In overfeat, PolyDL is slightly higher performing than oneDNN and the performance spread is fair among different code variants generated (Figures 22, and 23). googlenetv1 and googlenetv3 feature many more unique layers and PolyDL’s performance is slightly better than oneDNN’s for googlenetv1 and is slightly worse for googlenetv3 (Figures 24, and 26).

Across different models, the performance of PolyDL-DNN is consistently slightly better than that of PolyDL. Further, PolyDL achieves magnitudes of higher performance compared to the baseline
code and is very competitive with respect to the hand crafted oneDNN library code. In fact, PolyDL outperforms oneDNN in the case of alexnet, overfeat, and googlenetv1 and is significantly better than AutoTVM for all models except googlenetv1.

AutoTVM generates and runs typically over 1000 code variants for each layer and takes \( \sim 15 - 20 \) minutes to discover the best performing variant for a single layer. The PolyDL method zeroes in on the best version in under one minute. We note that AutoTVM’s methodology is not fully automatic. For example, we have obtained the performance results using CPU X86 specific implementations of Convolution code within AutoTVM [43], [16]. AutoTVM developers have created CPU specific and additionally architecture specific (i.e., Cascade Lake) code within the framework. Although AutoTVM discovers good tile sizes through auto-tuning, a lot of customized code has also been written to obtain high performance on Cascade Lake CPUs. Therefore, for the purposes of this experimental evaluation, AutoTVM represents a combination of library development and auto-tuning approach.

Comparison with prior compiler works. In this paper, we presented an approach to characterizing the working set sizes of the loops and relating them to the cache sizes of a computer system. Such an analysis formed the basis for ranking different code variants and selecting the best performing program version in our work. Alternately, one could compute the number of cache misses for a given program variant at different levels of the cache hierarchy and using the number of cache misses approximate its execution time. Subsequently, the code variant with the smallest estimated execution time can be considered to be the code variant that achieves the highest performance. Prior works have developed analytical cache miss computation methods [5, 20, 22]. However, none of them can analyze parallel programs. Our PolyDL compiler algorithms presented in this paper can analyze parallel code in addition to sequential code. Even so, we compare PolyDL with the latest analytical cache miss calculation work, viz., Gysi et al.’s cache modeling work [22] in the following manner. In our convolution related experiments, the image – img loop is parallel (Figure 7). For the sake of this experimental evaluation, we convert the problem to a sequential one by assuming that the loop length of the img loop is 1 and each core of the processor gets an equal share of the shared L3 cache. This is a reasonable assumption because in our experiments, each core processes an image each. The execution time of a program is estimated to be:

\[
L_1 \text{ misses} \times \text{lat}^{L2} + L_2 \text{ misses} \times \text{lat}^{L3} + L_3 \text{ misses} \times \text{lat}^{mem}
\]

The running time is equal to the sum of latencies at different cache levels. One of the summands, for example is, the number of misses at L1 cache is multiplied by the latency of the L2 cache (because L1 misses are serviced from L2 cache). For this comparison study, we invoke sequential analysis in PolyDL too with identical assumptions (img loop length being set to 1, and each processor getting an equal share of the L3 cache).

Figure 28 shows the speed-ups obtained by PolyDL and PolyDL-DNN with respect to Gysi et al.’s cache modeling work [22]. Their tool is termed HayStack and the same name is used in Figure 28. For most of the total 201 convolution layers (corresponding to the layers of fastrcnn, resnet, maskrcnn, xception, yolov2, mobilenet, alexnet, overfeat, googlenetv1, googlenetv3), the performances of code versions picked by PolyDL, and HayStack are identical. In some instances HayStack is better and in others PolyDL/PolyDL-DNN are higher performing. On average, PolyDL-DNN achieves marginally better performance – it has a 1.002X speed-up over HayStack. Between PolyDL and HayStack, HayStack has a slight edge: PolyDL is at 0.99X performance levels of HayStack. We attribute the observed performance levels of the different methods to the nature of statistics we obtain using the PolyDL algorithms (working set sizes) and those that we obtain using the HayStack algorithm (the number of cache misses). It is straight-forward to relate the number of cache misses to the running
time of the program using the cache latencies as done above. However, relating working set sizes to the running time of the program could be more complicated and the use of DNN techniques (i.e., PolyDL-DNN) is therefore superior to approximating the running time using cache latencies directly (i.e., PolyDL).

We observed that the running time of the HayStack tool is highly variable. In our experiments, HayStack took anywhere from a couple of seconds to 37 minutes to process a single code variant. On average, it takes \( \sim 35 \) seconds. PolyDL’s running time was more uniform – it takes 2 - 3 seconds for any variant. Thus, PolyDL’s analysis is orders of magnitude faster than HayStack’s.

### 6.3 Evaluation of Operator Fusion

We evaluate the performance benefits that accrue using the operator fusion algorithm presented in §5.

We study the performance of batch normalization (bnorm for short) and ReLU sequence. This combination occurs frequently in CNN models including that of Resnet-50. We compare the performances of 1) bnorm, ReLU unfused code which forms the baseline 2) fused bnorm + ReLU operator using our fusion algorithm 3) fused bnorm + ReLU operator in the oneDNN library. There is no facility in AutoTVM to perform operator fusion automatically and therefore, we do not compare its performance on the sequence. Figure 29 shows the speed-ups obtained by our fused operator vis-a-vis the baseline code and oneDNN’s corresponding fused operator for the tensor sizes of all layers of CNN models we have considered in our experiments. The speed-ups achieved by the fused operator are 1.59X and 1.20X (geometric average across tensor sizes) compared to the unfused baseline code and the oneDNN’s operator respectively. Batch normalization is a memory bandwidth bound operation and therefore, fusing the subsequent ReLU operation reduces round trips to the main memory which substantially improves the performance.

We perform fusion experiments with the convolution and ReLU6 sequence too. We compare the performances of unfused and fused versions of the sequence. We note that ReLU6 is not supported in the oneDNN library. Researchers have found that ReLU6 improves the performance of image recognition models [30]. However, ReLU6 is not widely adopted and it is not supported in the oneDNN library presumably because the high investment in supporting it is not justified. This underscores that 1) hand coding of a plethora of DNN primitives researchers experiment with is not scalable, 2) when an operator is not available in a library like oneDNN, it hampers the data scientists’ ability to quickly experiment and refine the DNN models. Therefore, automatic compilation techniques like the one developed in this paper are needed to address these bottlenecks.
Figure 30 shows the speed-ups of the fused operator when compared to the corresponding unfused operator. The ReLU6 activation function is applied on the output of the convolution. When the size of the output tensor is large, we observe a higher speed-up. When the output size is smaller, fusion has a marginal benefit. On average, the fused operator is 1.10X faster (geometric average). Furthermore, convolution is a compute-bound operation and therefore, the time spent in it is large relative to the time spent in the ReLU6 operation. This explains the contrasting speed-ups seen in the two sequences we have evaluated. For the bnorm + ReLU sequence, the speed-ups are larger because one, bnorm is a memory bound operation and two, the time spent in it is less compared to convolution. Consequently, the time spent in ReLU as a percentage of the time spent in bnorm is larger. Therefore, fusing the two operators shows larger performance gains for the bnorm + ReLU sequence.

7 RELATED WORK

Researchers have developed auto parallelization and program transformation systems to automatically transform code to achieve high performance [9, 29]. The Pluto [9] compiler derives a schedule for the code that attempts to minimize data reuse distances. The effect of the Pluto transformation will be that the iterations that use the same data will be executed close to each other in time and therefore, it will be cache friendly. The Pluto algorithm can accomplish fusion of loops too. However, Pluto’s performance can be far from what we can achieve with the use of microkernels that exploit the vector hardware effectively and by doing outer loop tuning in the way we have developed this work. Furthermore, the Pluto algorithm experiences scalability issues – as the number of loops in a loop nest increases, the algorithm/Pluto tool can take exceedingly long time to derive a schedule. When we inputted the convolution followed by ReLU code sequence, the tool took several hours and did not produce an output. Kong et al. [29] develop a framework to decompose a program into sub-parts and use customized criteria (as opposed to using a single objective function) – such as stride optimization, outer loop optimization, inner loop optimization to transform code. They show that their work without tiling transformation is able to achieve comparable results to that of Pluto.

Compile-time modeling of cache behavior and in particular calculating the number of cache misses has been an active area of research [5, 20, 22]. The researchers have demonstrated good accuracy in predicting the number of cache misses on simulators. The modern computer architectures employ a hash based scheme to map memory addresses to cache sets [45] which breaks the assumptions behind the cache miss analyses. In the present work, we model the behavior of caches as well. However, we do not model cache misses rather we consider data reuses and determine the size of cache needed to exploit the data reuses under conservative conditions. We ignore streaming...
accesses as their misses in cache will not be crucial in the resulting performance. Our analysis works on parallel code, whereas prior works are not equipped to handle parallel loops. Because of these techniques, we show that we are able to accurately rank code variants in terms of performance. Our experimental evaluation comparing against the latest cache miss analysis work [22] using sequential loop setting shows that the working set size approach we have adopted in our present work is as good as using cache misses for modeling of performance or is slightly better. Strout et al [36] introduce the novel concept of universal occupancy vector (UOV) for storage optimization — expand the arrays to a minimal degree so that the false dependences are eliminated paving the way for better scheduling of the code.

Automating systems using parametric tiling [6, 15, 23, 34, 38, 39] perform tile size exploration with tiled code generated with tile sizes as parameters (rather than hard-coded tile sizes). The parametric tiling technology reduces the code generation time during auto-tuning as the same code can be used for multiple tile size explorations. TVM [11], a compiler for deep learning, introduces the concept of tensorization, where a unit of computation can be replaced with a microkernel written using hardware intrinsics. AutoTVM [12] which is based on TVM, is targeted at accelerating deep learning workloads and uses machine learning to guide auto-tuning of deep learning primitives. We compared our techniques with AutoTVM in this paper and showed that the DL primitives created by PolyDL (our work) enjoy superior performance vis-a-vis AutoTVM. Further, the time it takes for our techniques to create high performance code is a fraction of the time AutoTVM takes. Tiramisu [4] is a polyhedral model based compiler framework that introduces a scheduling language to allow the programmer to explore various program transformations.

Bondhugula et al. [8] propose a fusion model that considers loss of parallelism with aggressive fusion. In addition, the number of available hardware prefetch streams is also used as a constraint to determine the beneficial fusion structures. In this paper, we have proposed a domain specific fusion algorithm that fuses heavy operators with element-wise operators. Consequently, by construction, we are sure of there not being any loss of parallelism. Furthermore, the data accessed by the element-wise operator always being a subset of the data accessed by the preceding/succeeding compute-intensive operator, it is known apriori that there will not be additional stress on memory bandwidth. Because of these reasons, we have simplified the criteria for when to fuse operators. However, since the patterns that our algorithm tackles occur frequently in DL workloads, the fusions that our approach accomplishes will be useful and it presents a first generic approach towards automatic fusions of operators in the context of deep learning.

8 CONCLUSION

In this paper, we presented novel compiler algorithms to derive high performing DL primitive implementations automatically and to perform operator fusions. We proposed a methodology to optionally use microkernels for the inner most loops of DL primitives to optimally use the vector pipelines of modern CPUs. With a combination of the above techniques, we demonstrated through experimental evaluation that we are able to match the performance of expert coded implementations of the Intel oneDNN library for CNN models. Additionally, because our method works at compile-time, we require much less time and compute resources to derive efficient implementations compared to auto-tuning systems such as AutoTVM. Our system – PolyDL will ease the development of computer architecture specific libraries by at most requiring the development of only a small number of microkernels. Additionally, it will allow data scientists to enjoy high performance on the new DNN architectures they develop immediately and automatically, without waiting for their DNN structures to be implemented in a library by expert programmers.
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