LXI Device of Timing and Synchronization

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ABSTRACT

For automatic test system of multiple instruments to be synchronized work to accomplish more functional requirements of the situation, in-depth analysis of the LXI bus specification, satellite system timing technology and time synchronization technology, developed LXI timing and synchronization module design functional requirements and overall program to achieve the time synchronization between the LXI bus instrument.

KEYWORD: LXI, timing, synchronization

And performance indicators to synchronize the device will be granted when LXI analysis to determine the system performance to be achieved and complete LXI timing synchronized with the overall design of the module. Automatic network test and measurement system may be composed of LXI instruments provide a reference clock timing, clock as the master clock is the timing. Precision clock synchronization protocol PTP can be achieved from other synchronization clock to the master clock.

LXI MODULE TIMING AND SYNCHRONIZATION FUNCTIONS AND TECHNICAL INDICATORS

The module should have the functional and technical indicators are as follows:
(1) module can receive the satellite signal, satellite timing function.
(2) having a main clock function, to achieve its other clock synchronization.
(3) stability within 60ns timing.
(4) clock synchronization accuracy of 100ns.

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HARDWARE DESIGN

LXI timing synchronization with the main function of the module with an external device (PC, timing modules, etc.) and through communication timing algorithm when LXI devices delegation.

For the communication part, it is due LXI Ethernet technology as a standardized communication protocol of the device and therefore supports TCP / IP protocol is a basic requirement. Moreover, the most important aspect of this paper is a timing clock, and LXI Class B is added IEEE1588 Precision Time Protocol on the basis of the class C, and therefore must meet LXI Class B requirements. For hardware requirements comprising LAN interface for physical layer connectivity, along with a LAN interface driver microcontroller is also essential in the timing module circuit, select Compass / GPS timing OEM board EZ3204 completion timing, and with the timing module turn electric circuits for communication timing module and LXI interface; the choice in terms of software support TCP / IP protocol of the Linux system, and the preparation of related software on this basis to achieve timing module control, master and slave clock synchronization, based on the command trigger mode and Web interface.

LXI interface timing modules are interconnected by timing module switching circuit, LXI module timing and synchronization hardware features specific block diagram shown in Figure 1. This selection of Atmel's AT91RM9200 as master LXI interface, the most important part is the core of embedded system circuit, with Altera's FPGA for time synchronization time stamp acquisition and completion of the master clock function. Following are descriptions LXI interface hardware circuit and timing module hardware circuit design principles.

![Figure 1. LXI timing and synchronization module hardware circuit diagram.](image_url)

LXI Interface Hardware Design

LXI interface circuit to the ARM microprocessor core, by the communication interface portion, namely LAN interface, based interconnection with PC's. LAN interface hardware includes RJ45 ports, isolation, network communication interface chips. Isolator primarily as electrical isolation effect, to avoid interference on the bus signal LAN device cause irreversible damage. Network communication interface chip is mainly responsible for the data on the LAN bus for encoding and decoding. This selection of AT91RM9200 own Ethernet controller, Ethernet controller according to the configuration of the output I / O, can be used independent media interface MII data...
transfer is complete, you can send or receive in order to achieve 10 / 100Mbps data rate single clock frequency 50MHz.

LXI interface circuit core of the device is the ARM microprocessor, which directly determines the performance of the LXI interfaces can be realized. This selection AT91RM9200 as the processor, the processor supports Linux, Plam OS, Wince and other mainstream operating system, can be reliable and stable operation in complex environments[2], through advanced processor interrupt priority level interrupt handler is divided source reduction interrupt processing time, a strong interrupt handling. Meanwhile, the processor has a low cost and reliability advantages of the dual [3], by writing the appropriate program can be achieved on data extraction and processing [4-6].

In the LXI interface circuit must have an Ethernet interface. AT91RM9200 itself with network control devices, FIFOs stack and specialized data controllers receive and transmit channels, enabling OSI reference model network between the physical layer and the data link layer MAC layer hardware, but it does not have physical layer interface, so should external access an Ethernet physical layer transmission channel controller with. In this paper, Intel produced a lower error rate of Fast Ethernet physical layer transmission control chip LXT971A network to send and receive data [1]. It can be easily connected with the AT91RM9200 network controller via media independent interface.

**Timing Module Hardware Circuit Design**

Timing is a key part of the module hardware circuit when LXI grant award and synchronization module when. The hardware part of the function is the use of satellite signal receiver module to receive satellite send down the standard time information and accurate second pulse signal, the received time information is sent to the master via RS-232, you will receive a master of time after the information is parsed, with the output module receives the second pulse signal, the rising edge of the pulse signal in the second time, the time is written FPGA internal clock counter, and the FPGA internal clock counter then acted as the local clock and the master clock, and other reference time from the clock to provide synchronization module. FPGA is connected to the output of the network chip (MII layer), to complete the process of extracting the synchronization time stamp, and communicate with the ARM controller through the EBI bus.

Currently the world's major manufacturers of FPGA Altera and Xilinx, Altera company EP1C6Q240I7 paper selected chip, which has a wealth of programmable resources, can easily achieve real-time clock and hardware synchronization message detection and time stamp capture functions.

**SOFTWARE DESIGN**

LXI timing and synchronization module software design can be divided into three parts commands, PC control panel design, control and embedded granted resolver, clock synchronization synchronization software design. User to LXI synchronization module transmits a control through the PC control panel timing command module, run the command parser in response to the host computer sent commands to perform different control codes depending on the command, in order to
achieve the Beidou receiver module control, analytical the program also can receive Beidou receiving module to send information out of time, and returns the time information to the host machine. Beidou receiver module sends standard time information at the same time, also the second pulse signal transmission standard, when the command parser Beidou receiving module receives the time information and the time after the completion of the solver, the solver out time is written FPGA, complete timing function.

**Control Panel Design**

In order to facilitate LXI configure and timing synchronization module, and you can easily monitor the status of the current paper was developed control panel with user-friendly configuration. It provides visualization of data to enable real-time display, both to provide information to users, but also convenient for the debugger. In line with the principles of friendly and easy to use, when granted for LXI synchronization modules in Visual C++ 2008 and Java 1.6 environment is designed based on IVI-COM soft front panel and Web-based soft front panel and Java Applet.

According LXI specification, LXI instrument must provide a Web interface, some information about the instrument can be obtained by HTML. If only some static display pages, HTML almost no impact on the user. However, if the requirements of real-time display some information or requirements LXI timing and synchronization module can respond to a form submitted by the user at once and immediately returns the result, the browser and the server will continue to encoding and decoding HTML form, this has led to a lot of computing resources occupied ARM processor, but also increase the load on the network, requiring Java Applet technology to replace static bandwidth-consuming dynamic HTML technology. Java Applet is executed on the browser Java applet, there are contemporary Java Applet Web page is accessed, the code into the local machine to perform, thus reducing the load on the server. At the same time, Java Applet can be Socket connection with the server has been, so when LXI grant synchronization module in response to the user control command, the response can be returned immediately to the Applet by the Socket interface. Java program and the design is complete, almost without modification can be performed on other platforms, such a large degree of savings in cost and time of development. Therefore, this paper has designed a soft panel Web interface based on Java Applet technology. Development environment select Eclipse, in conjunction with JDK 1.6, Java Applet finally completed the design process, compile and debug.

**Design of Embedded Control Software**

Embedded control software is based on AT91RM9200 written, since the processor running the Linux operating system, the control program is developed under Linux environment. Embedded control program for direct control of the timing module also includes an embedded Linux operating system based on chip driver implementations. For LXI timing and control synchronization module in the PC running based IVI-COM drivers operating panel and IVI-COM drivers, and then access when LXI grant synchronization module through the network, and the synchronization module LXI timing and Embedded Controller AT91RM9200 Run parser to handle PC commands sent from the control panel. Command parser after receiving instructions for command parsing, and then perform the appropriate action.
depending on the command, if it is a control command timing module, the satellite receiver module corresponding initialization control, and has made receiver module to receive the time data, and returns data to the host computer IVI-COM software, real-time display standard satellite time and quantity of available satellite signals on the control panel. When time data satellite signal receiver module is parsed, it is necessary to complete the timing of time to write to the FPGA in operation, the program to take the arrival time in seconds Beidou receiver module output pulse rising timing of realization.

For Linux software development, mostly in native way, namely local development, commissioning and operation mode. The ways of the development environment and debugging software often requires extensive memory, embedded systems and limited resources, we can not use that way. For embedded systems, we use the cross compiler debugging method, this method of development and debugging tools are installed on the host (that run the Linux operating system, PC) on the corresponding embedded controller is called the target board. To write software code to complete the cross-compile the host can generate can run on ARM binary file, and then download the file to the target board to run.

**Synchronization Software Design**

LXI instruments running in embedded Linux systems, synchronization software used to synchronize clocks LXI instruments, so the synchronization software implementation code running in embedded Linux systems. The synchronization software runs on top of UDP / IP protocol, the software code in accordance with the IEEE 1588 standard design.

Between LXI instrument is achieved through four types of messages sent or received from the master clock synchronization, four messages are messages Sync (synchronization message), Delay-Req message (delay request message), Follow-Up message (message Follow ), Delay-Resp message, and it will record the time when clock synchronization sync to send or receive messages or Delay-Req message, and this time the recording is called time stamp. It includes two clock synchronization calculation of the amount, i.e. the amount of delay and the offset.

**CONCLUSION**

Chapter LXI-depth study of the timing and synchronization module design requirements, through the grant of LXI synchronization module performance analysis shows the functional framework of the corresponding hardware circuit design and software. Using the interface LXT971A, plus one isolators improve system stability and anti-interference, timing module timing EZ3204 Compass module together with RS-232 circuits, power module timing module hardware circuit by means of special hardware FPGA synchronization process the time stamp of the capture. At the same time, about the use of VC ++ ATL template developed under the Windows platform feasibility IVI-COM driver software panel based on the Web-based interface to analyze the soft surface and Java Applet Web dynamic interactive technology rationality was also introduced for embedded control software need to implement functionality, as well as clock synchronization process.
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