Controlled oxide interlayer for improving reliability of SiO$_2$/GaN MOS devices

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The impact of controlling Ga-oxide (Ga$_2$O$_3$) interlayers in SiO$_2$/Ga$_2$O$_3$/GaN gate stacks is investigated by means of physical and electrical characterizations. Direct deposition of SiO$_2$ insulators produces thin Ga$_2$O$_3$ interlayers, and subsequent oxidation treatment attains high-quality insulator/GaN interface. However, the Ga diffusion into the SiO$_2$ layers severely degrades the breakdown characteristics of GaN-MOS devices. To improve reliability of such devices, we proposed a two-step procedure with the initial SiO$_2$ deposition conducted under nitrogen-rich ambient, followed by thick SiO$_2$ capping. We found that this two-step procedure enables nitrogen incorporation in the insulator/GaN interface to stabilize GaN surface. Consequently, the Ga diffusion into the SiO$_2$ overlayer during the oxidation annealing is effectively suppressed. The proposed method allows us to achieve a SiO$_2$/Ga$_2$O$_3$/GaN stacked structure of superior electrical property with improved Weibull distribution of an oxide breakdown field and with interface state density below 10$^{10}$ cm$^{-2}$ eV$^{-1}$. © 2019 The Japan Society of Applied Physics

1. Introduction

Gallium nitride (GaN) has attracted considerable attention for use in future power-switching devices because its physical characteristics are superior to those of Si. The wide bandgap and high-breakdown electric field of GaN allow power devices to be made that are capable of high-temperature operation and low on-resistance. After successful commercialization of lateral AlGaN/GaN heterojunction field-effect transistors (HFETs), vertical power devices have been intensively investigated. Similarly to vertical Si and silicon carbide (SiC) power devices, normally-off switching devices such as GaN-based metal–oxide–semiconductor field-effect transistors (MOSFETs) are highly required in fail-safe systems. As for the gate insulators in GaN power devices, deposited dielectric films with sufficiently large band offset against the GaN-based semiconductors, such as Al$_x$O$_y$, SiO$_2$, and their oxynitrides, can be possible candidates for limiting the gate leakage current. Actually, these wide bandgap insulators have been used in recent development of AlGaN/GaN MOS-HFETs, advanced deposition techniques, post-deposition annealing, and their combinations have been investigated by many researchers. While the two-dimensional electron gas in AlGaN/GaN MOS-HFETs is separated from the insulator/semiconductor interface with the AlGaN barrier layer, inversion carriers in the GaN MOSFETs are directly accumulated at the interface. This indicates that the quality of the interface between the deposited gate dielectric films and GaN substrates is crucial for good performance and high reliability of GaN MOSFETs.

Aiming at high-quality GaN-MOS gate stacks, oxidation of the GaN surface other than dielectric film deposition was investigated previously to produce Ga$_2$O$_3$/GaN MOS devices. Although sufficient conduction-band offset is not achievable at the oxide interface, very low interface state density ($D_{it}$) of 10$^{11}$ cm$^{-2}$ eV$^{-1}$ order or less was demonstrated. This indicates the superior intrinsic nature of the Ga$_2$O$_3$/GaN interface. On the basis of these findings, we have studied the use of a thin layer of Ga-oxide (Ga$_2$O$_3$) as an interlayer between wide bandgap SiO$_2$ dielectrics and freestanding GaN substrates. The stacked SiO$_2$/Ga$_2$O$_3$/GaN MOS capacitors subjected to subsequent oxidation treatment at the optimum temperature of 800 °C exhibited excellent interface properties, in which $D_{it}$ value estimated by a conductance method was below 10$^{10}$ cm$^{-2}$ eV$^{-1}$. However, it was found that the oxidation treatment causes diffusion of Ga atoms into the SiO$_2$ dielectrics, leading to severe degradation of the insulating property of GaN-MOS devices such as increased gate leakage current and deteriorated dielectric breakdown characteristics. To overcome these problems, we employed rapid thermal treatment in subsequent oxidation of SiO$_2$/Ga$_2$O$_3$/GaN structures and achieved an improved dielectric reliability together with superior interface properties.

Despite the fact that the rapid thermal treatment indeed suppresses Ga diffusion into the SiO$_2$ upper layers, the thermal budget needed for improving dielectric properties of the deposited films is limited. Moreover, in order to further enhance device reliability and reproducibility, it is necessary to understand and control the Ga diffusion in SiO$_2$/Ga$_2$O$_3$/GaN stacks. In this research, we focus on controlling the oxide interlayers by means of SiO$_2$ deposition under nitrogen-rich ambient. Oxide growth on the GaN surface caused by SiO$_2$ deposition and subsequent oxidation treatment was systematically investigated by means of physical characterizations and electrical measurements of the fabricated GaN-MOS capacitors.

2. Experimental methods

The SiO$_2$/Ga$_2$O$_3$/GaN stacked structures used in this study were fabricated on free-standing GaN(0001) substrates with 5 μm thick Si-doped n-type GaN epilayers. The doping concentration of the epilayers was about 1 × 10$^{16}$ cm$^{-3}$. After wet cleaning the GaN surfaces with a diluted hydrochloric acid solution, SiO$_2$ dielectric film of about 20 nm thick was directly deposited on the GaN surface by...
plasma-enhanced chemical vapor deposition (PECVD) using tetraethyl orthosilicate (TEOS) and oxygen (O2) gas mixtures at a substrate temperature of 370 °C, hereafter named “O2-PECVD”. The TEOS/O2 flow ratio was set to 1/500 (0.5/250 sccm), where massive O2 flow is preferable to obtain good insulating properties of SiO2 films by reducing carbon impurity. The input power and operating chamber pressure during deposition were maintained at 30 W and 79 Pa, respectively. It should be noted that plasma oxidation of the GaN surface proceeds at the initial stage of SiO2 deposition, resulting in a formation of SiO2/GaOx/GaN stacked structures with a simple procedure. The thickness of the GaOx interlayer was estimated to be about 2 nm in our previous research. In this study, engineering of the oxide interlayer was achieved by changing the conditions for TEOS-SiO2 deposition as follows. In order to suppress the initial plasma oxidation of the GaN surface and incorporate nitrogen in the insulator/GaN interface, PECVD was conducted with a low O2 flow ratio (TEOS/O2 = 0.5/10 sccm) diluted by nitrogen (N2), in which the input power was reduced to 20 W, and the chamber pressure was kept at 79 Pa (partial N2 pressure of about 66 Pa) for stable plasma discharge. As the radical nitrogen was dominant in the reaction chamber, suppressed plasma oxidation, nitrogen incorporation into the film (SiON), and stabilization of the GaN surface were expected. However, because the insulating property of the deposited films was severely deteriorated due to oxygen deficiency under such conditions, a conventional TEOS-SiO2 layer (O2-PECVD) of 15 nm thick was stacked on a 5 nm thick SiON layer formed under the nitrogen-rich ambient. This two-step procedure is denoted hereafter as “O2/N2-PECVD”. Then, the single O2-PECVD and stacked O2/N2-PECVD samples received oxidation treatment in dry O2 atmosphere at 800 °C for the prolonged duration of 30 min to evaluate the thermal robustness of SiO2/GaOx/GaN structures.

Formation of the GaOx interlayer was characterized by synchrotron-radiation X-ray photoelectron spectroscopy (SR-XPS) with excitation energy of 1253.6 eV and a photoelectron take-off-angle of 90° at BL23SU in SPring-8. Prior to the SR-XPS measurements, 20 nm thick SiO2 layers were thinned to about 2 nm by dipping in a diluted hydrofluoric acid solution to detect the plasma insulator/GaN interface. The Ga diffusion within the SiO2/GaOx/GaN stacked structures was evaluated by dynamic secondary ion mass spectrometry (SIMS) using the O2+ primary ion beam with the impact energy of 1 keV. For electrical measurements, circular Ni gate electrodes with a diameter of 100 μm and Al back contact were formed by vacuum evaporation to fabricate GaN-MOS capacitors. The quality of the insulator/GaN interface and the insulating properties of GaN-MOS capacitors were evaluated by capacitance–voltage (C–V) and current–voltage (I–V) measurements, respectively. Dref values were estimated by a conductance method at room temperature. Reliability of the gate stacks was also studied by time-zero dielectric breakdown (TZDB) measurements of GaN-MOS capacitors.

3. Results and discussion
3.1. Characterization of GaOx interlayer by SR-XPS

Figure 1 shows Ga 2p3/2 core-level spectra obtained from the O2-PECVD and O2/N2-PECVD samples with and without oxidation treatment at 800 °C for 30 min. Fine calibration of binding energy for the acquired Ga 2p3/2 Spectra was done using N 1s peak (397.5 eV) corresponding to a N–Ga bonding component from the GaN substrate. A Shirley-type background was subtracted from the measured data, and the spectral intensities were normalized for all samples. In order to characterize the formation of GaOx interlayers, peak deconvolution of the Ga 2p3/2 spectra was performed. A good curve fitting (black lines) to the experimental data (open circles) was obtained with Ga–N (blue lines) and Ga–O (red lines) bonding components determined from the wet-cleaned GaN surface and that oxidized at 1000 °C (a thick Ga2O3 layer), respectively. The detailed procedure for peak deconvolution can be found in our previous reports. As shown in Fig. 1(a), the Ga–O component was detected in the as-deposited O2-PECVD sample. This indicates plasma oxidation of the GaN surface at the initial stage of SiO2 deposition and corresponds with the results of our previous study, showing the formation of a GaOx interlayer about 2 nm thick. The area-intensity ratio of Ga–O to Ga–N components (I(3d-Ga–O)/I(3d-Ga–N)) was almost unchanged after the oxidation treatment at 800 °C [see Fig. 1(b)], indicating negligible additive oxide growth with the subsequent treatment. Note that, in the as-deposited O2/N2-PECVD sample [Fig. 1(c)], the initial plasma oxidation of the GaN surface was apparently
suppressed. This is probably due to the significantly reduced O₂ flow ratio (reduced oxygen radical density) and effective nitrogen passivation of the GaN surface under the nitrogen-rich ambient. Moreover, the subsequent oxidation of the O₂/N₂-PECVD sample resulted in an additive oxide growth and produced a GaOₓ interlayer almost identical to that in the O₂-PECVD sample, as seen in Figs. 1(b) and 1(d), which suggests excellent interface properties even for the O₂/N₂-PECVD sample subjected to the oxidation treatment.

3.2. Dynamic SIMS analysis of Ga diffusion into SiO₂ layer

Ga diffusion into the SiO₂ dielectrics and nitrogen incorporation in the insulator/GaN interface were next analyzed using dynamic SIMS method. Figure 2(a) shows the depth profiles of Ga atoms within the SiO₂/GaOₓ/GaN stacked structures with and without oxidation treatment at 800 °C. Owing to high diffusivity of Ga atoms in SiO₂, slight Ga incorporation in the as-deposited SiO₂ films was observed for both O₂- and O₂/N₂-PECVD samples before the oxidation treatment. The Ga atoms tended to segregate on the surface, and the SiO₂ deposition under the nitrogen-rich PECVD conditions had negligible impact on the initial Ga distribution in the SiO₂ overlayer. In contrast, while a distinct Ga diffusion into the SiO₂ layer formed with the O₂-PECVD procedure was induced by the oxidation treatment at 800 °C, the two-step O₂/N₂-PECVD procedure was found to be beneficial for suppressing the Ga diffusion. This remarkable difference implies significant improvement in thermal robustness of the SiO₂/GaOₓ/GaN gate stacks.

We also evaluated nitrogen incorporation in the insulator/GaN interface with the O₂/N₂-PECVD process. For this purpose, the nitrogen atoms were detected with a SiN⁻ fragment for the top-side SIMS measurement. Figure 2(b) shows the obtained nitrogen profiles in the SiO₂/GaOₓ/GaN stacks with and without oxidation treatment. For all measured samples, nitrogen concentration in the upper SiO₂ layers was close to the background level, and intense nitrogen signals within the GaN epilayers were originated from the artifact fragments caused by intermixing at the interfaces. Note that the interface region of the as-deposited O₂/N₂-PECVD sample exhibited increased nitrogen content, as indicated in Fig. 2(b). This corresponds to incorporation of a few atomic percent of nitrogen into the bottom SiO₂ portion formed under the nitrogen-rich conditions. However, it was impossible to detect the excess nitrogen content at the interface after the oxidation treatment at 800 °C.

Based on these findings from SR-XPS and SIMS analyses, possible mechanisms can be proposed to improve stability against Ga diffusion into SiO₂ films. First, nitrogen incorporation into SiO₂ is an effective way to suppress diffusion of foreign elements; it is known as an established method for suppressing boron penetration into ultrathin SiO₂ (SiON) gate dielectrics in Si-LSI technology. Therefore, nitridation of the bottom SiO₂ portion with the O₂/N₂-PECVD process should improve the thermal budget of the SiO₂/GaOₓ/GaN stacks. But because the excess nitrogen content was not detected after the subsequent oxidation treatment at 800 °C (see Fig. 2(b)), the impact of the nitried-SiO₂ bottom layer is limited. Another possible explanation is preservation of the stable GaN surface (insulator/GaN interface) with radical nitrogen exposure. This is because nitrogen deficiency on the GaN surface produces metallic-phase Ga to act as a diffusion source. In fact, the growth of the GaOₓ interlayer was minimized with the O₂/N₂-PECVD process, as shown in Fig. 1(c). Moreover, assuming that an unstable and excessive GaOₓ interlayer is responsible for the diffusion source, thick GaOₓ interlayers will have harmful effects on thermal stability of the gate stack. Although contributions of these candidate mechanisms cannot be clarified from the current SR-XPS and SIMS analyses, the resulting SiO₂/GaOₓ/GaN stack formed with the O₂/N₂-PECVD and subsequent oxidation treatment has a GaOₓ interlayer identical to that in the O₂-PECVD, while suppressing Ga diffusion into the upper SiO₂ layer.

3.3. Electrical properties of SiO₂/GaOₓ/GaN stacked MOS capacitors

The electrical properties of the SiO₂/GaOₓ/GaN gate stacks fabricated by O₂-PECVD and O₂/N₂-PECVD procedures were investigated by C–V measurements at room temperature. Bidirectional C–V curves taken with measurement frequencies ranging from 10 Hz to 1 MHz and ideal C–V curves are shown in Fig. 3. The ideal curve was horizontally shifted by assuming an appropriate work function of the gate electrodes. In general, clockwise hysteresis and frequency dispersion in the C–V characteristics correspond to slow charge injection into electrical defects in SiO₂ layers (and/or
near the interface region) and fast trapping/detrapping phenomena at the GaO
x
/GaN interface, respectively. As shown in Figs. 3(a) and 3(b), very small hysteresis and frequency dispersion were achieved for the as-deposited O2-PECVD sample. In addition, frequency dispersion was further reduced by the oxidation treatment, indicating improved interface quality with an appropriate treatment. Regarding the O2/N2-PECVD sample [Figs. 3(c) and 3(d)], whereas hysteresis and frequency dispersion slightly increased, the oxidation treatment at 800 °C was found to be effective. Consequently, mostly identical C–V characteristics were obtained for the O2- and O2/N2-PECVD processes. The slight negative shifts of C–V curves were observed in both samples with oxidation treatment, which is more remarkable for O2-PECVD sample. Considering the improvement of interface quality by oxidation treatment, the negative shift may result from the formation of positive fixed charges within the SiO2 overlayer. Therefore, it may be correlated with Ga diffusion into the SiO2 overlayer. However, the cause of the negative shift is still unclear at present. The energy distributions of Dit extracted from the conductance method39) for the as-deposited samples are shown in Fig. 4. As expected from minor frequency dispersion in Figs. 3(a) and 3(c), low Dit values ranging 1010–1011 cm−2 eV−1 were obtained at the energy levels of Ec − E = 0.2–0.5 eV. Furthermore, conductance peaks were hardly detected for the SiO2/GaOx/GaN stacks fabricated by O2- and O2/N2-PECVD processes after the oxidation treatment, which corresponds to the Dit reduction below 1010 cm−2 eV−1 (in the order of 109 cm−2 eV−1). These results demonstrate that, as is the case with the reported O2-PECVD process, GaOx interlayer formed by O2/N2-PECVD and the subsequent oxidation treatment is quite beneficial, preventing Ga diffusion into SiO2 upper layer.

Finally, reliability of GaN-MOS capacitors was evaluated by means of TZDB measurements. Figure 5 represents Weibull plots of the cumulative failure for the fabricated GaN-capacitors with O2- and O2/N2-PECVD processes. Although, fairly good interface properties were achievable even with the as-deposited SiO2/GaOx/GaN stacks (see Figs. 3 and 4), poor insulating properties and deteriorated reliability were confirmed by the TZDB test, especially for the as-deposited O2/N2-PECVD sample. This is probably due
to the poor quality of the bottom SiO$_2$ layer, having oxygen vacancies and carbon impurities formed under the nitrogen-rich conditions. It is obvious that the oxidation treatment at 800 °C shifted Weibull plots toward higher electric field, suggesting positive impact of the high-temperature oxidation on film densification and recovery of oxygen deficiency in the film. However, a wide distribution was observed for the O$_2$/N$_2$-PECVD sample, which anomalously high-breakdown field under 12 MV cm$^{-1}$ was attributable to charge trapping into Ga-related defects in the SiO$_2$ film (electric field near the insulator/GaN interface is relaxed by electron trapping within the SiO$_2$ film). In contrast, although minor (low probability) oxide breakdown under low electric field was difficult to exclude in our laboratory-based device fabrication, a steep Weibull slope at around 12 MV cm$^{-1}$ was successfully obtained for the O$_2$/N$_2$-PECVD sample. This intrinsic breakdown field of the GaN-MOS capacitor is comparable to that of a commercial SiO$_2$/SiC system (11 MV cm$^{-1}$), having a similar conduction-band offset. These results indicate the importance of controlling the oxide interlayer and the advantage of the proposed two-step O$_2$/N$_2$-PECVD process combined with the oxidation treatment for achieving GaN-MOS structures of high reliability and quality for power device applications.

4. Summary

The reliability of SiO$_2$/GaO$_x$/GaN gate stacks was successfully improved by engineering the oxide interlayer. By conducting the two-step SiO$_2$ deposition named O$_2$/N$_2$-PECVD procedure, an excessive plasma oxidation of the GaN surface during the initial stage of SiO$_2$ deposition was suppressed, and a small amount of nitrogen was incorporated in the insulator/GaN interface. Thermal diffusion of Ga atoms into the SiO$_2$ overlayer during the oxidation treatment was significantly suppressed with the O$_2$/N$_2$-PECVD process, while preserving excellent interface quality. As a result, highly reliable GaN-MOS capacitor exhibiting very high oxide breakdown fields of about 12 MV cm$^{-1}$, together with superior interface properties with extremely low $D_{it}$ value below the detection limit was achieved. These results demonstrate the importance of controlling the interlayer for designing highly reliable GaN-MOS power devices.

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