Development of RSFQ voltage drivers for arbitrary AC waveform synthesisers

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Abstract. We have realised RSFQ circuits for an integrated bit pattern generator to drive large Josephson junction arrays and synthesise arbitrary AC waveforms. We present test circuits to investigate the driving of junction arrays by sequences of voltage pulses. To elevate the level of voltage pulses, the circuits have been terminated by SQUID stack voltage drivers. Drivers of various bit lengths and different designs, in pure-serial and in combined parallel-and-serial SFQ pulse processing modes, were developed, fabricated and tested. Voltage amplification by factors four and eight were obtained. The circuits were realised in 4-µm Nb SIS trilayer technology with externally shunted Josephson junctions (critical current density: 1 kA/cm²).

1. Introduction
Integrated superconducting circuit architectures combining Rapid Single Flux Quantum (RSFQ) circuit modules and large Josephson junction series arrays offer new solutions for applications in digital signal processing. Recently, we presented a concept for RSFQ devices in which circular shift registers serve as memories for sequences of binary information [1]. RSFQ circular shift registers are versatile building blocks in superconducting circuitry because of their ability of recurrent operation [2], [3]. They can be utilised advantageously as local memories for circulating binary information. For a digital-to-analog conversion device, we proposed a setup of an RSFQ bit pattern generator based on circular shift register operation. The purpose of the generator is to convert sequences of binary code into voltage pulses to drive Josephson junction arrays and synthesise arbitrary AC waveforms for metrology applications. To drive large junction arrays, the created voltage pulses are to be amplified by semiconductor circuits. In this paper, we present RSFQ voltage drivers based on SQUID stacks.

2. RSFQ circuits for an integrated bit pattern generator
In our previous study [1], we described the operating principle and flow of data processing of a bit pattern generator in which all digitising, memorising, and further processing functions are carried out on-chip. We have realised circular shift registers of several bit lengths serving as memories for the binary code created by a digitiser, e.g., by a two-junction interferometer. The design of the registers is based on the $z^+$ register type using an elastic pipeline mode of operation [4] and has been optimised for clock frequencies of up to 25 GHz and with ranges of operation of about ±25% [5]. To convert the
memorised sequence of SFQ pulses into voltage pulses, the register outputs are followed by the combination of an SFQ pulse doubler and an SFQ/DC sensor (T-flipflop with SFQ/DC converter).

The circuits were realised in 4-µm Nb SIS (S: Superconductor, I: Insulator) trilayer technology with externally shunted Josephson junctions, [6] (critical current density \( j_c : 1 \text{kA/cm}^2 \), characteristic voltage \( V_c : 250 \mu \text{V} \), Stewart-McCumber parameter \( \beta_c : \leq 1 \)).

3. Development of RSFQ voltage drivers: design, parameter optimisation, and experimental test

The SFQ/DC converters at the output of the pattern generator convert the coded information inherent in SFQ pulses into voltage pulses with amplitudes of about 100 µV and at a low output impedance of about 1 Ω (parameters mainly determined by the technology parameters of the fabrication process [6]). At present, at bandwidths higher than 1 GHz, semiconducting amplifiers lack the capability of further processing the voltage pulses available.

In order to elevate the level of voltage pulses, the circuits were terminated by SQUID stack voltage multipliers. Drivers of different bit lengths (4 and 8 SQUID stacks) were realised. Figure 1 shows the schematic diagram of test circuits to investigate the flow of signal processing. They consist of a phase generator (DC/SFQ converter), a Josephson transmission line (JTL), a T-flipflop with an SFQ/DC converter, and are terminated by voltage driver units. The SFQ/DC converter generates trains of SFQ pulses controlled by T-flipflop operation. In succession, the SFQ pulses propagate along the JTL. In difference to [7], each section of the JTL is inductively coupled to one bit of the stack. Each SFQ pulse propagating along the JTL consequently switches the junctions of the interferometers in the stack.

The SFQ pulse trains of repetition frequency \( f \) create a voltage \( V \) according to the Josephson relation, \( f = V/\Phi_0 \) (\( \Phi_0 = h/2e \) is the flux quantum, \( h \) is Planck’s constant, \( e \) is the elementary charge), and are multiplied by the SQUID stack up to a voltage level of \( nV \) (\( n \): number of SQUIDs in the stack). To optimise the bandwidth, drivers in different configurations were realised, see figure 1. They differ by various modes of SFQ pulse processing, pure-serial (left), and combined parallel-and-serial (right). In the latter case, SFQ pulse trains are splitted to parallel branches. As regards the signal flow within the setup of the waveform synthesiser, the drivers are utilised as interfaces between the bit pattern generator and the semiconducting amplifiers.

**Figure 1.** Schematic diagram of RSFQ test circuits terminated by 2n SQUID stack voltage drivers designed to different configurations, left: in pure-serial, right: in combined parallel-and-serial SFQ pulse processing modes (\( V_{in}, V_{out} \): input, output voltages at the amplifier ports).
Figure 2. Simulation of the voltage driver output for 4-stage serial (left) and 2x2-stage serial-parallel (right) mode. Time and voltage are in PSCAN units, 1.32 ps and 250 µV, respectively.

The voltage drivers were optimised with respect to optimum voltage amplification and maximum circuit parameter margins by PSCAN und COWBOY simulations [8]. To investigate time delays in signal propagation, we have simulated the shapes of the voltage pulses at the input and output of the voltage amplifiers. As an example, figure 2 illustrates the shapes of the voltage pulses at the output of 4-SQUID-stack voltage drivers according to both SFQ pulse processing modes. It shows the output voltage as well as its running time average over 12 time units, which corresponds to about 60 GHz low-pass filtering. This is also the frequency of the incoming SFQ pulse train (not shown, average voltage about 0.5 in PSCAN units). As can be seen, both modes yield approximately the desired amplification, with slightly higher values for the pure-serial mode. Although the parallel mode shows slightly steeper edges, the actual rise-time (~30 ps) is not significantly different. The parallel mode advantageously exhibits correct operation at approximately 20% higher frequencies of the input pulse train. A significant advantage in rise-time should only be expected for larger levels of parallelism.

Figure 3 illustrates the layout of a section of a JTL and a single bit stage of a SQUID-stack-based voltage driver. Figure 4 shows the current voltage characteristic of an 8-stage voltage driver laid out in pure-serial mode. At a critical current of $I_c = 380$ µA, it exhibits a normal-state resistance of $R_N = 8 \Omega$. Besides signal amplification, an increase in the circuit impedance was simultaneously obtained (output impedance at the SFQ/DC converter: 1 Ω), thus providing an easier match with semiconductor amplifiers (50 Ω).

To experimentally investigate the test circuits, first the RSFQ part of the circuit was biased to the level of 0.7 of its critical current. In a second step, the stack circuit was biased, in this case to a value $I_c = 380$ µA, $R_N = 8 \Omega$.
Figure 5. Operation of an RSFQ voltage driver circuit containing 4 SQUIDs in series at different amplitudes of current fed to the DC/SFQ converter; left: creation of one SFQ pulse, right: creation of two SFQ pulses per period. Upper traces: input current (500 µA/div), middle traces: output of SFQ/DC converter (100 µV/div), lower traces: output of the voltage drivers (200 µV/div).

slightly lower than its critical current. Correct circuit performance was demonstrated for voltages proportional to pulse repetition frequencies at the driver input of up to 50 GHz with bias current margins larger than ±15%. Its operation was tested up to 20 MHz; investigations at higher frequency bandwidths are in progress. Circuit functionality was confirmed for both polarities of biasing the SQUIDs. Its operation is sensitive to the spread of critical currents of the stacked SQUIDs. Figure 5 shows the operation of a 4-bit serial SQUID stack circuit and demonstrates correct amplification by a factor of 4.

4. Conclusion
We have designed, optimised, and fabricated RSFQ voltage drivers for the setup of an arbitrary AC waveform synthesiser. We have realised voltage driver units laid out at various bit lengths and at different configurations of signal processing, in pure-serial and combined parallel-and-serial SFQ pulse processing modes. The drivers were experimentally tested in properly designed RSFQ test circuits. Voltage amplification by factors four and eight was achieved (increase in the output voltage up to 0.4 mV). Simultaneously, for easier match with semiconductor circuits, an increase in the output impedance was obtained.

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