Application-Specific System Processor for the SHA-1 Hash Algorithm

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Abstract

This work proposes an Application-Specific System Processor (ASSP) hardware for the Secure Hash Algorithm 1 (SHA-1) algorithm. The proposed hardware was implemented in a Field Programmable Gate Array (FPGA) Xilinx Virtex 6 xc6vlx240t-1ff1156. The throughput and the occupied area were analyzed for several implementations in parallel instances of the hash algorithm. The results showed that the hardware proposed for the SHA-1 achieved a throughput of 0.644 Gbps for a single instance and slightly more than 28 Gbps for 48 instances in a single FPGA. Various applications such as password recovery, password validation, and high volume data integrity checking can be performed efficiently and quickly with an ASSP for SHA1.

Keywords: Hash code, Acceleration, FPGA, SHA-1.

1. Introduction

The Secure Hash Algorithm version one, SHA-1, is an algorithm used to verify the integrity of variable length data streams from an operation called hash. A hash function outputs a fixed-length code $C$ given a message of variable length $K$ as input. It may be said that the output of the hash function, also called
the hash code, is a signature of the input message, known in the literature as a fingerprint. These features are used in Message Authentication Codes (MAC), mainly the Keyed-Hash Message Authentication Code (HMAC), which make extensive use of SHA-1 (Kakarountas et al., 2006).

The SHA-1 is a revised version of the SHA-0, a substitute for the MD5 (Message Digest 5) algorithm in 1995 by the National Institute of Standards and Technology (NIST). Then, the SHA-1 was published as a Federal Information Processing Standard (FIPS) number 180-1 (Stallings, 2015).

The SHA-1 hash function, in addition of being selected for Digital Signature Algorithm (DSA) as standardized by FIPS 186-4 (NIST, 2013), it acts verifying the sequence of data associated with communication protocol messages, files, passwords storage and it was used in digital certificates before being replaced by SHA-2. The SHA-1 generates hash codes of $C = 160$ bits for any size of $K$. However, with the advent of the Big Data, Internet of Things (IoT) and other emergent areas. It is necessary to the hash code to be generated more quickly for situations associated with a large volume of data and with small energy consumption in the case of devices within a sensor network in the IoT context. Thus, this project aims to develop a dedicated hardware implementation proposal for the SHA-1 algorithm. The proposed hardware can be seen as a specific application processor also called in the literature by Application-Specific System Processor (ASSP).

The presented hardware was developed in a Field-programmable gate array (FPGA), reconfigurable hardware platform formed by thousands of logical cells, that after a synthesis process behaves as specific hardware associated to a given algorithm. The FPGA has been an indispensable tool in the development of ASSPs, Application Specific Integrated Circuits (ASICs) and as a platform for accelerating complex algorithms as presented in (de Souza & Fernandes, 2014; Kara et al., 2017; Shaikh et al., 2017; Venkateshan et al., 2015; Shi et al., 2012). One of the advantages in developing specific circuits is the clock reduction when compared to implementations in systems with general purpose processors (GPP). The hardware SHA-1 algorithm can be used in the development of an
ASIC for IoT applications or used in the FPGA itself, aiming to accelerate hash code calculation in several applications such as password recovery, password validation and integrity checking in large volumes of data.

2. Related Work

The work presented in Jarvinen (2004) used a Xilinx Virtex-II XC2V2000-6 FPGA to implement the SHA-1 with Iterative Looping (IL). This implementation occupied around 1,275 Logic Cells (LC) operating at a throughput of 734Mbps. The works presented in Michail et al. (2005); Kakarountas et al. (2006) also used a Xilinx Virtex-II XC2V2000-6 FPGA to implement the SHA-1. These implementation proposals present a scheme using Full Pipeline (FL) that consumed around 3,519 LC for a throughput of 2.5267 Gbps. Comparing with the proposal presented in Jarvinen (2004), the throughput is 4× higher due to the use of 4 SHA-1 pipelined modules. However, the occupancy area is also around 4× larger. In Lee et al. (2009) it is also presented a proposal using FL that reached a throughput of 5.9 Gbps.

In Iyer & Mandal (2013) the SHA-1 implementation was executed in a Xilinx Virtex 5 Xc5vlx50t FPGA using hardware description language Verilog. The implementation performed with IL was similar to that presented in Jarvinen (2004). However, it had a slightly higher occupancy rate, around 1,351 LC, and the throughput also a little higher, around 786 Mbps.

The work presented by Khan et al. (2014) brought a solution of the SHA-1 in FPGA with low power for uses in devices lacking high power capacity and with high throughput, in addition to a small area size compared to the similar implementations. For this, the authors relied on the work presented in Michail et al. (2005) and Kakarountas et al. (2006). In this work the LC number was reduced by making a more serial implementation, also reducing the throughput. Another implementation-based approach described in Michail et al. (2005) and Kakarountas et al. (2006) was showed in Michail et al. (2016), in which an implementation in a TSMC 90 nm ASIC was proposed. In this proposal, a
throughput of around 15 Gbps was observed.

A comparison of several Xilinx FPGA platforms with SHA-1 implementation was presented in Michail et al. (2014). The implementation was based on the proposal presented in Michail et al. (2005) and Kakarountas et al. (2006) and a maximum throughput of about 14.3 Gbps was observed for a Xilinx Virtex 7 FPGA.

Works with SHA-1 implementation on other hardware platforms can be found in Marks & Niewiadomska-Szynkiewicz (2014) and Al-Kiswany et al. (2009) in which comparisons between Graphics Processing Units (GPUs) and CPUs were performed. The GPUs NVIDIA Tesla M2050 with 448 CUDA cores and AMD FirePro V7800 with 1440 stream processors could achieve throughput peaks of up to 1.5 Gbps.

The proposal here developed used as target device a Virtex FPGA 6 xc6vlx240t-11156 FPGA and the results showed a throughput of 652 Mbps for a single SHA-1 module. The implementation used the Iterative Looping strategy which occupied less circuit area when compared to other strategy Michail et al. (2005) and Kakarountas et al. (2006) and unlike the results presented in the literature, it was possible to synthesize up to 48 SHA-1 modules in a single FPGA device yielding a throughput of 28.160 Gbps.

3. Secure Hash Algorithm 1 (SHA-1)

The SHA-1 is a hashing algorithm described by the Federal Information Processing Standards Publication (FIPS) 180-4 NIST (2015) and by RFC 3174 Network Working Group (2001), which operates with variable length input messages. For each $i$-th incoming message, $m_i$, (of length $K_i$ bits), expressed as

$$ m_i = \left[ m_0 \quad m_1 \quad \ldots \quad m_{K_i-1} \right] \text{ where } m_k \in \{0,1\} \forall k, \quad (1) $$

the SHA-1 algorithm generates an output message, $h_i$, called a hash code, of fixed size $C = 160$ bits, characterized as

$$ h_i = \left[ h_0 \quad h_1 \quad \ldots \quad h_{C-1} \right] \text{ where } h_k \in \{0,1\} \forall k. \quad (2) $$
The $i$-th incoming message, $m_i$, of $K_i$ bits is extended by inserting two binary words. The first one, called here, $p_i$, has $P_i$ bits and it is inserted by an operation called Append Padding. The second, called here $v_i$, has $T$ bits and it is inserted by an operation called Append Length. Thus, the calculation of the hash code, $h_i$, for each $i$-th incoming message is carried out in an extended message, here called $z_i$, which corresponds to a concatenation of the messages $m_i$, $p_i$ and $v_i$, that is, $z_i = [m_i, p_i, v_i]$. Each $i$-th message $z_i$ has $Z_i = K_i + P_i + T$ bits that can be divided into $L_i$ blocks of length $M = 512$ bits, that is,

$$L_i = \frac{Z_i}{M} = \frac{K_i + P_i + T}{512}.$$  \hspace{1cm} (3)

The pseudo-code presented in the Algorithm 1 displays the sequence of steps required to generate the hash code. These steps are going to be described in detail in the following subsections.

### 3.1. Padding Insertion

This step (lines 2 and 3 of the Algorithm 1) is performed before calculating the hash code and it makes the $i$-th message length, $m_i$, divisible by $M = 512$ after the Append Length step. The padding message, $p_i$, associated with the $i$-th incoming message is formed by a binary word of $P_i$ bits in which the most significant bit is 1 and the rest of the bits are 0. The generation of the padding message is performed by the function PaddingGeneration($K_i$) shown in the line 2 of the algorithm 1.

The calculation of the $P_i$ value can be expressed by

$$P_i = \begin{cases} 
448 - (K_i \mod 512) & \text{for } (K_i \mod 512) < 448 \\
512 - (K_i \mod 512) + 448 & \text{for } (K_i \mod 512) \geq 448 
\end{cases},$$  \hspace{1cm} (4)

where the $(a \mod b)$ operation returns the modulo of the division between $a$ and $b$. Thus, $p_i$ can be expressed as

$$p_i = \left[ p_0 \ p_1 \ \ldots \ \ p_{P_i-1} \right],$$  \hspace{1cm} (5)

where, $p_0 = 1$ and $p_i = 0$ for $i = 1 \ldots P_i - 1$. 

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Algorithm 1 SHA-1 for each $i$-th message $W_i$

1: $z_i \leftarrow [m_i]$
2: $p_i \leftarrow \text{PaddingGeneration}(K_i)$
3: $z_i \leftarrow [m_i, p_i]$
4: $v_i \leftarrow \text{LengthGeneration}(K_i)$
5: $z_i \leftarrow [m_i, p_i, v_i]$
6: $h_i \leftarrow \text{HashInitialization}( )$
7: for $j \leftarrow 0$ until $L_i - 1$ do
8:     $b_j \leftarrow \text{MessageSplit}(z_i)$
9:     $n \leftarrow -1$
10:    $H(n) \leftarrow \text{HashVariablesInitialization}( )$
11:   for $n \leftarrow 0$ until 79 do
12:       $w(n) \leftarrow \text{WFunctionCalculation}(n, b_j)$
13:       $f(n) \leftarrow \text{FFunctionCalculation}(n, B(n), C(n), D(n))$
14:       $H(n) \leftarrow \text{HashVariablesUpdate}(H(n))$
15:     end for
16:    $h_i \leftarrow \text{UpdateHash}(H(n))$
17:   end for
3.2. Length Insertion

In this step (lines 4 and 5 of the Algorithm 1) the message \( v_i \) is added, which is characterized by a binary word of \( T = 64 \) bits and expressed as

\[
v_i = \begin{bmatrix} v_0 & v_1 & \ldots & v_{T-1} \end{bmatrix} \quad \text{where } v_k \in \{0,1\} \forall k. \tag{6}
\]

The generation of the message length is performed by the function \text{LengthGeneration}(K_i) presented in the line 4 of the algorithm 1. The message \( v_i \) stores the length value of the \( i \)-th incoming message \( m_i \), that is,

\[
v_i = \text{Binary}(K,T) \tag{7}
\]

where \( \text{Binary}(a,b) \) is a function that returns a vector of size \( b \) with the binary representation of a decimal number \( a \) with \( b \) bits according to the big-endian standard.

The 180-4 FIPS norm NIST (2015), assumes that the size, \( K_i \), of most messages can be represented by 64 bits, that is, \( K_i < 2^T \).

Finally, at the end of the second step the message, \( z_i \), which is an extension of the \( i \)-th original input message, \( m_i \), is generated (line 5 of the Algorithm 1). In this work the message \( z_i \) is identified as a \( Z_i \) bits vector expressed as

\[
z_i = \begin{bmatrix} z_0 & z_1 & \ldots & z_{Z-1} \end{bmatrix} \quad \text{where } z_k \in \{0,1\} \forall k. \tag{8}
\]

3.3. Hash Code Initialization

The hash code initialization (line 6 of the Algorithm 1) is standardized by the FIPS 180-4 NIST (2015) according to the following expressions:

\[
\begin{align*}
ha &= \begin{bmatrix} h_0 & \ldots & h_{31} \end{bmatrix} = \text{Binary}(1732584193,32), \tag{9} \\
hb &= \begin{bmatrix} h_{32} & \ldots & h_{63} \end{bmatrix} = \text{Binary}(4023233417,32), \tag{10} \\
hc &= \begin{bmatrix} h_{64} & \ldots & h_{95} \end{bmatrix} = \text{Binary}(2562383102,32), \tag{11} \\
hd &= \begin{bmatrix} h_{96} & \ldots & h_{127} \end{bmatrix} = \text{Binary}(0271733878,32), \tag{12} \\
he &= \begin{bmatrix} h_{128} & \ldots & h_{159} \end{bmatrix} = \text{Binary}(3285377520,32), \tag{13}
\end{align*}
\]
where
\[ h_i = \begin{bmatrix} h_a & h_b & h_c & h_d & h_e \end{bmatrix}. \] (14)

3.4. Message Split

In this step, line 8 of the Algorithm 1, the message \( z_i \) is split into \( L_i \) blocks of \( M = 512 \) bits, that is,
\[ z_i = \begin{bmatrix} b_0 & b_1 & \ldots & b_{L_i-1} \end{bmatrix}, \] (15)
where each \( j \)-th block associated with \( i \)-th message is expressed as
\[ b_j = \begin{bmatrix} b_{j,0} & b_{j,1} & \ldots & b_{j,M-1} \end{bmatrix} \text{ where } b_{j,k} \in \{0,1\} \forall k. \] (16)
The \( j \)-th block, \( b_j \), can also be represented as
\[ b_j = \begin{bmatrix} u_j[0] & u_j[1] & \ldots & u_j[15] \end{bmatrix}, \] (17)
where \( u_j[k] \) is a 32 bits message, that is,
\[ u_j[k] = \begin{bmatrix} u_j[k,0] & u_j[k,1] & \ldots & b_{j,k,31} \end{bmatrix} \] (18)
where \( u_j[k,l] \in \{0,1\} \forall l.

3.5. \( H(n) \) Hash Variables Initialization

The SHA-1 algorithm has five 32 bits variables, called \( A(n) \), \( B(n) \), \( C(n) \), \( D(n) \) and \( E(n) \) that are updated during iterations of the algorithm. These variables are identified in this work as vectors:
\[ X(n) = \begin{bmatrix} x_0 & x_1 & \ldots & x_{31} \end{bmatrix} \text{ where } x_k \in \{0,1\} \forall k, \] (19)
where, the combination of these five variables form a vector of 160 positions identified as
\[ H(n) = \begin{bmatrix} A(n) & B(n) & C(n) & D(n) & E(n) \end{bmatrix}. \] (20)

The initialization of these variables, in the instant \( n = -1 \), (line 10 of the Algorithm 1) according to FIPS 180-4 NIST (2015) occurs with the receipt of the same values that start the hash \( h_i \), so \( A(-1) = h_a, B(-1) = h_b, C(-1) = h_c, D(-1) = h_d \) and \( E(-1) = h_e. \)
3.6. \textbf{w}(n) Variable Calculation

In SHA-1, it takes 80 iterations for a valid output, \( h_i \), associated with a \( i \)-th message be generated (Algorithm 1, line 11). In each \( n \)-th iteration a \( w(n) \) variable is calculated, expressed as

\[
\begin{align*}
\text{w}(n) = & \begin{cases} 
u_j[n] & \text{for } 0 \leq n \leq 15 \\
\text{sw}[n] & \text{for } 16 \leq n \leq 79
\end{cases}, 
\end{align*}
\]

(21)

where

\[
\text{sw}[n] = \text{lr}(u_j[n-3] \oplus u_j[n-8] \oplus u_j[n-14] \oplus u_j[n-16], 1)
\]

(22)

where \( \oplus \) is the exclusive or operation and \( \text{lr}(r,s) \) represents the leftrotate function that is expressed as

\[
\text{lr}(r,s) = (r \ll s) \lor (r \gg (32-s)),
\]

(23)

where \( \lor, \ll, \text{ and } \gg \) are the bitwise OR and left and right bitwise shift, respectively.

3.7. \textbf{f}(\cdot) Function Calculation

In each \( n \)-th iteration of each \( j \)-th block, \( b_j(n) \), a nonlinear function, \( f(\cdot) \), is calculated from the information of the hash variables \( B(n), C(n) \) and \( D(n) \). The output of the function, \( f(\cdot) \) is stored in the vector \( f(n) \) (line 13 of the Algorithm 1), expressed as

\[
f(n) = f(n, B, C, D) = \begin{cases} 
\alpha(n) & \text{for } n = 0 \ldots 19 \\
\beta(n) & \text{for } n = 20 \ldots 39 \\
\gamma(n) & \text{for } n = 40 \ldots 59 \\
\delta(n) & \text{for } n = 60 \ldots 79
\end{cases},
\]

(24)

where

\[
\alpha(n) = (B(n-1) \land C(n-1)) \lor (\neg B(n-1) \land D(n-1)),
\]

(25)

\[
\beta(n) = B(n-1) \oplus C(n-1) \oplus D(n-1),
\]

(26)
\[ \gamma(n) = (B(n-1) \land C(n-1)) \lor (B(n-1) \land D(n-1)) \lor (C(n-1) \land D(n-1)) \]  \hspace{1cm} (27) 

and

\[ \delta(n) = B(n-1) \oplus C(n-1) \oplus D(n-1), \]  \hspace{1cm} (28) 

where \( \neg \) and \( \land \) are negation operation and bitwise AND, respectively.

### 3.8. Hash Variables Update

Also, in each \( n \)-th iteration of each \( j \)-th block \( b_j(n) \), the values of the variables \( A(n) \), \( B(n) \), \( C(n) \), \( D(n) \) and \( E(n) \) are updated after the calculation of \( f(n) \) (line 14 of the Algorithm 1). The update of these variables is represented by the following equations:

\[ E(n) = D(n-1), \]  \hspace{1cm} (29) 

\[ D(n) = C(n-1), \]  \hspace{1cm} (30)

\[ C(n) = \text{lr}(B(n-1), 30), \]  \hspace{1cm} (31) 

\[ B(n) = A(n-1) \]  \hspace{1cm} (32) 

and

\[ A(n) = V(n) + Z(n) + \text{lr}(A(n-1), 5), \]  \hspace{1cm} (33) 

in which,

\[ Z(n) = W(n) + E(n-1) \]  \hspace{1cm} (34) 

and

\[ V(n) = f(n) + k(n). \]  \hspace{1cm} (35) 

The SHA-1 has four 32 bits constants \( k(n) \), which are used in the \( n \)-th iteration of each \( j \)-th block \( b_j n \), as specified by

\[ K(n) = \begin{cases} 
1518500249 & \text{for } n = 0 \ldots 19 \\
1859775393 & \text{for } n = 20 \ldots 39 \\
2400959708 & \text{for } n = 40 \ldots 59 \\
3395469782 & \text{for } n = 60 \ldots 79 
\end{cases} \]  \hspace{1cm} (36)
3.9. Hash Code Update

For each \( j \)-th block, \( b_j \), SHA-1 executes 80 iterations, and at the end of every \( j \)-th block the hash code is updated linearly following the expressions:

\[
\begin{align*}
ha &= ha + A(79), \\
hb &= hb + B(79), \\
hc &= hc + C(79), \\
hd &= hd + D(79), \\
he &= he + E(79).
\end{align*}
\]

and

\[
\begin{align*}
N_i &= L_i \times 80
\end{align*}
\]

iterations, where \( N_i \) is defined in this work as the total number of interactions for the calculation of the hash associated with a message \( m_i \).

4. Proposed Implementation

Figure 1 presents the general architecture of the proposed SHA-1 hardware implementation. The structure allows the visualization of the algorithm in Register Transfer Level (RTL), in which one can observe the signal flow (or variables) between the components of datapath and the registers RA, RB, RC, RD and RE. The hardware starts with the \( i \)-th message \( m_i \) entering a module called INIT which is responsible for the functionalities presented between the lines 1 and 6 from the Algorithm 1, the control of the two loops (lines 7 and 11) and the initialization of hash variables (\( A(n), B(n), C(n), D(n) \) and \( E(n) \)) to each \( j \)-th block, \( b_j \), through the \( h0 \) signal.

The CJ and CN blocks are \( \log_2(L) \) and 7 bits counters, respectively. The CN counter is responsible for the loop iteration of line 11 of the Algorithm 1, generating the signal \( n \). The CJ counter is incremented by the counter CN
and controls the loop iteration of the line 7 of the Algorithm 1, through the signal \( j \). Based on line 8 of the Algorithm 1 and subsection 3.4, the DM module splits the \( i \)-th message \( z_i \) into \( L \) blocks of \( M = 512 \) bits, in which each \( j \)-th block is displayed in Figure 1 by the signal \( b_j \). This \( M = 512 \) bits signal \( b_j \) is then equally divided into 16 buses of the 32-bits, in which each \( i \)-th bus is represented by the signal \( u_j[i] \). After this step, the \( w[n] \) signal is generated by the GW module (line 12 of the Algorithm 1) from the signal counter CN.

The modules GF, GK and GW represent the operations expressed by Equations 24, 36 and 21, respectively. The modules LR5 and LR30 represent leftrotate operations expressed by Equations 33 e 31. It is observed that unlike implementations in sequential processors such as GPP, uC (Micro-controllers) and others, these equations are executed in parallel, accelerating the SHA-1 algorithm. The details regarding the implementation of the modules GF, GK, GW, LR5 and LR30 are detailed in the following subsections.

4.1. GF Module

The GF module implements the function described in subsection 3.7 and presented in the line 13 of the Algorithm 1. This module contains a multiplexer
called GF-MUX which selects the function type from the $n$ value according to Equation 24 and detailed in Figure 2.

Figure 2: GF Module Architecture.

The function type selection in the GF-MUX multiplexer is controlled by the GV module, through binary logic with comparators and logic gates corresponding to each interval, having the following outputs,

$$ GV = \begin{cases} 
0 & \text{for } n = 0 \ldots 19 \\
1 & \text{for } n = 20 \ldots 39 \\
2 & \text{for } n = 40 \ldots 59 \\
3 & \text{for } n = 60 \ldots 79 
\end{cases} $$

Each one selecting a function $f(n)$ based on the 7 bits counter of the CN module.

4.2. GW Module

The GW module consists of 16 messages $u_j[n]$ (with 32-bits) in the input, originating from $b_j[n]$, according to Equation 17 of Subsection 3.4, and has the
purpose to perform the operation demonstrated by the equation 21 described in the subsection 3.6 and line 12 of the Algorithm 1.

Figure 3 details the module that is formed by a 80 multiplexer inputs, called W-MUX which is selected from the $n$ signal. For the values of $n$ from 16 to 79, the signal $sw[n]$ is expressed by the equation 22 through the $SW_k$ module where $k = 16...79$, specified in Figure 4.

![Figure 3: GW Module Architecture](image)

![Figure 4: SWk Module Operation](image)

Each $k$-th module $SW_k$ is formed by a register, called here $RW_k$, a leftrotate module (Equation 23) called LR1 a exclusive OR (XOR) gate and a comparator. The $RW_k$ register stores the value of the signal $sw[n]$ through the comparator when $n = k - 3$. The XOR logic gate performs the operation described in Equation 22 and the LR1 module performs the leftrotate function for $s = 1$. 

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Figure 5 details a generic module associated with the leftrotate implementation based on Equation 23.

\[ \text{Figure 5: Arquitetura do módulo RLs.} \]

The RL5 and RL30 modules perform the leftrotate operation for \( s = 5 \) (see Equation 33) and \( s = 30 \) (see Equation 31), respectively. The implementation of these modules is also depicted by Figure 5.

4.3. \( h_i \), Hash Processing

After generating the signals \( w(n), k(n), f(n) \), in each \( n \)-th iteration, and the value \( E(n - 1) \), the signals \( Z(n) \) and \( V(n) \), both of 32 bits, are calculated through the sum modules \( S_1 \) and \( S_2 \), executed in parallel, subsequently \( S_3 \) and \( S_4 \). All the sum modules used in the implementation are 32-bit-specific circuits, which optimize the processing time and the space occupied by the total circuit. The calculation of the signals \( Z(n) \) and \( V(n) \) are expressed by Equations 34 and 35 and are executed during the line 14 of the Algorithm 1. The last step of every \( n \)-th iteration is the update of the hash variables, \( A(n), B(n), C(n), D(n) \) and \( E(n) \), stored in the RA, RB, RC, RD e RE registers, respectively. Another important step in the SHA-1 is that one described in Section 4.2, in which the value of the RC register is updated through the \( \text{lr}(r, 30) \) operation, expressed in detail by Equation 23. At each iteration of \( n \) the values of the registers move between them by updating the other hash variables according to Equations 29 to 33. These steps are executed in the line 14 of the Algorithm 1.

At the end of the 80 loop iterations in \( n \) (Line 11 of Algorithm 1), the parts that make up the hash, \( ha, hb, hc, hd \) and \( he \) (Equation 14), are updated by the modules HA, HB, HC, HD and HE, respectively. This step is performed on
the line 16 of the Algorithm 1. Finally, at the end of the $N_i$ iterations (Equation 42) the hash code final value, $h_i$, associated to the $i$-th message is achieved. The CO module has the function of concatenating the 5 buses of the 32-bits formed by the signals $h_a$, $h_b$, $h_c$, $h_d$ and $h_e$ and generating a serial signal with the hash code $h_i$.

5. Results

The Table 1 presents the results obtained after the hardware synthesis of the implementation proposed in this work (Figure 1). Results concerning the hardware occupancy in the target FPGA (Virtex 6 xc6vlx240t-11156) as well as the results associated with the latency and the throughput achieved after the synthesis process are presented. Results were generated for several parallel implementations of the SHA-1 algorithm according to Figure 1, differently from other works presented in Michail et al. (2005); Kakarountas et al. (2006); Khan et al. (2014); Michail et al. (2016), which used serial (pipeline) structures. The proposal here presented, used several SHA-1 parallel modules, enabling the throughout acceleration which is especially useful in cases of brute force password recovery, in which there are a large number of hash codes to be generated.

Table 1: Results concerning occupancy, sampling rate and throughput for various parallel implementations of the SHA-1 algorithm.

| NI | NR  | PR (%) | NLUT | PLUT (%) | $T_s$ (ns) | $R_s$ (Gbps) |
|----|-----|--------|------|----------|------------|--------------|
| 1  | 2.154 | 0.71 | 2.605 | 1.72 | 9,932 | 0,644 |
| 4  | 8.575 | 2.84 | 10,388 | 6.89 | 9,961 | 2,570 |
| 8  | 17.136 | 5.68 | 20,662 | 13.71 | 9,965 | 5,138 |
| 16 | 34.255 | 11.36 | 43,263 | 28.70 | 9,994 | 10,246 |
| 32 | 68.498 | 22.72 | 86,873 | 57.64 | 9,994 | 18,296 |
| 48 | 102.733 | 34.08 | 129,902 | 86.19 | 10,909 | 28,160 |

The first column of the table, called NI, indicates the number of parallel
implementations performed. The second column, NR, shows the number of registers used in the target FPGA and the third column, called PR, represents the percentage of registers used regarding the total available in the FPGA which is 301,440. The fourth and fifth columns, called NLUT and PLUT, represent the number of logical cells used as LUTs (Lookup Tables) for constructing digital circuits and the percentage of LUTs regarding the total amount available which is 150,720. Finally, the sixth and seventh columns show the results, obtained for various implementations, of the sampling rate, $T_s$ and throughput, $R_s$, respectively.

The hardware, was developed in parallel as shown in Section 4, with 32 bits buses so that the sampling time, $T_s$, is corresponding to the clock, that is, every $n$-th iteration (see Loop of the line 11 of the Algorithm 1) is performed in a clock pulse time, here called $t_{CLK} = T_s$. The $T_s$ values are displayed in the sixth column of the table 1. It is possible to verify that there is not a significant change with the increase of NI, that is, for an increment of $48 \times$ of NI there was only an increment of less than $1 \text{ ns}$ in $T_s$, which represents an increase of almost $32 \times$ in hash throughput.

Based on the Algorithm 1 and the architecture presented in Figure 1, for every $j$-th $M = 512$ bits block $b_j$, 80 iterations are executes (Equation 42), so the proposed hardware throughput can be calculated as

$$R_s = \frac{M \times NI}{80 \times T_s} = \frac{512 \times NI}{80 \times T_s} = \frac{64 \times NI}{10 \times T_s}.$$  \hspace{1cm} (44)

It is important to note that the values of throughput greater than 15 Gbps are unpublished in the literature (NI = 32 e NI = 48). A 28.16 Gbps throughput is equivalent to retrieve a totally unknown 6 digits numeric password (using the brute force method) in a maximum of 20 ms or a 6 digits alpha numeric password (each digit with 62 possibilities) from a hash code in a maximum of 17.4 minutes.
6. Conclusion

This work presented a SHA-1 hardware implementation proposal. The proposed structure, also called ASSP, was synthesized in an FPGA aiming to validate the implemented circuit. All implementation details of the project were presented and analyzed regarding occupation area and processing time. The results obtained are quite significant and point to new possibilities of using hash algorithms in dedicated hardware for real-time and high-volume applications.

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