Electronically and Independently Controllable Quadrature Sinusoidal Oscillator with Low Output Impedances

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Abstract. This work presents the quadrature sinusoidal oscillator using two Voltage Differencing-Differential Input Buffered Amplifiers (VD-DIBAs), two resistors, and two capacitors. The VD-DIBA is an electronically controllable active building block with high input and low output impedances that can connect to other circuits directly without the buffers. With these distinguished features, the VD-DIBA is employed in this design. The proposed oscillator can produce two sine waves with a phase shift of 90 degrees. Over the entire tuning frequency range, the magnitude of the quadrature output voltages is constant. The proposed oscillator is independently adjustable in terms of frequency and oscillation condition. Moreover, the frequency of oscillation can be electronically and linearly adjusted by the bias currents. The condition of oscillation is adjustable by resistors, $R_1$ and $R_2$. The performances of the proposed quadrature oscillator are tested through the PSpice simulation and the experiment. In the simulation, the VD-DIBA is built from the 0.18 $\mu$m Taiwan Semiconductor Manufacturing Company (TSMC) CMOS process with $\pm 0.9$ V supply voltages. In the experiment, the VD-DIBA is implemented using the commercial ICs, LM13700, and AD830 with $\pm 5$ V supply voltages. The simulated Total Harmonic Distortion (THD) values of the output voltages, $V_{o1}$ and $V_{o2}$ at $f_0 = 1.03$ MHz are 1.63 $\%$ and 1.81 $\%$, respectively. The experimental THD values of the output voltages, $V_{o1}$ and $V_{o2}$ at $f_0 = 536.6$ kHz, are 1.43 $\%$ and 1.00 $\%$, respectively.

Keywords

AD830, electronical controllability, VD-DIBA, LM13700, quadrature sinusoidal oscillator, 0.18 $\mu$m TSMC CMOS.

1. Introduction

A sinusoidal oscillator that provides two output signals with a 90° phase difference is known as a “quadrature sinusoidal oscillator”. It is a fundamental circuit that is important in electrical engineering systems. Many applications need the quadrature sinusoidal oscillator as the sub-circuit, such as electrical measuring systems, medical equipment, audio-visual system, signal processing system, communication, and telecommunication [1] and [2].

Numerous researchers have attempted to design a sinusoidal oscillator using several kinds of active building blocks. The use of active building blocks in the circuit design is convenient and flexible when it is compared with using the BJT or CMOS transistors. Moreover, using the active building block in the circuit design requires a few passive elements which are easy to analyse for finding out the equation of the circuit parameters. Literature [3] and [4] now recognizes the benefits, applications, and utility of a newly introduced active
building block called Voltage Differencing-Differential Input Buffered Amplifier (VD-DIBA). The VD-DIBA is the electronically controllable active function block with high impedance at input voltage terminals and low impedance at an output voltage terminal. Moreover, the voltage differencing unit at the output section of VD-DIBA is very useful for designing the voltage mode circuit without using an external voltage subtracting circuit. With these distinguished features, the VD-DIBA is employed to design the quadrature sinusoidal oscillator in this work. In our literature review, several analogue circuit designs using VD-DIBA have been proposed [5, 6, 7, 8, 9, 10, 11, 12, 13] and [14]; for example, inductance simulator [5] and [6], voltage-mode first-order all-pass filter [7] and [8], voltage-mode biquad filter [9, 10, 11] and [12], and sinusoidal oscillators [13, 14, 15, 16, 17] and [18].

Herein, the review of sinusoidal oscillators [13, 14, 15, 16, 17, 18] using VD-DIBA as the active building block is given. The simple sinusoidal oscillator with a single VD-DIBA is proposed in [13] and [15]. The oscillators in [13, 14, 15, 16] and [17] use grounded capacitors which is attractive from an integration point of view. The proposed oscillators in [15] and [16] are adjustable independently of frequency and oscillation frequency. The frequency of the oscillator proposed in [13] and [16] is linearly and electronically tuned. However, there are some drawbacks existing from these oscillators. The oscillators in [15, 14, 16] and [17] cannot provide the quadrature output waveform. The output voltage nodes of the quadrature oscillators in [18] are not low impedance. The proposed oscillators in [13, 14, 15, 17] and [18] are not adjustable independently of frequency and oscillation frequency. The frequency of the oscillators in [14, 15, 17] and [18] is not linearly and electronically controlled. Table 1 shows the comparison of the sinusoidal oscillators using VD-DIBA.

| Ref. | No. of VD-DIBA | No. of passive element | Low output impedance at all output nodes | Quadrature waveform | Independent control of frequency and condition | Linearly and electronically adjustable frequency | Experiment |
|------|----------------|------------------------|------------------------------------------|---------------------|-----------------------------------------------|-----------------------------------------------|------------|
| [13] | 2              | 3                      | Yes                                      | No                  | Orthogonal                                    | Yes                                           | No         |
| [14] | 1              | 4                      | Yes                                      | No                  | Orthogonal                                    | Yes                                           | No         |
| [15] | 2              | 4                      | Yes                                      | No                  | Orthogonal                                    | Yes                                           | No         |
| [16] | 2              | 2                      | No                                       | Yes                 | Yes                                           | Yes                                           | Yes        |
| [17] | 1              | 4                      | Yes                                      | Yes                 | No                                            | Orthogonal                                    | No         |
| [18] | 2              | 3                      | No*                                      | Yes                 | Yes                                           | Yes                                           | No         |

* In [18], output voltage node, $V_{o2}$ is not low impedance.

of the wave can be adjusted linearly and electronically. The workability of the circuit is verified by PSpice simulation and experiment in a laboratory using VD-DIBAs constructed from the 0.18 $\mu$m TSMC CMOS process (simulation) and the commercial IC LM13700 and AD830 (experiment).

2. Theories and Principle

2.1. VD-DIBA

The VD-DIBA’s circuit symbol is shown in Fig. 1 which consists of two parts, the transconductance amplifier and the unity gain voltage differentiating amplifier. At the first part, the input voltage terminals $V_{+}$ and $V_{-}$ and the output current terminal $Z$ have high impedance. The transconductance, $g_m$ of the first part is adjustable by controlling the bias current, $I_B$. In the second part, the input voltage terminals, $V$ and $Z$ are high impedance. While, the output voltage terminal, $W$ is low impedance. The equivalent schematic of VD-DIBA is illustrated in Fig. 2. The input and output relationship of VD-DIBA is shown in Eq. (1).

\[
\begin{bmatrix}
I_{v+} \\
I_{v-} \\
I_v \\
V_w
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
g_m & -g_m & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
V_{+} \\
V_{-} \\
V_v \\
V_w
\end{bmatrix}.
\]

Fig. 1: Symbol of VD-DIBA.
The internal construction of VD-DIBA realized from the CMOS transistors is depicted in Fig. 3. It is found that the transconductance amplifier is constructed from the MOS transistors, M₁–M₈, and the unity gain voltage differencing amplifier, which is modified from the Differential Difference Current Conveyor (DDCC) [19], is constructed from the MOS transistors, M₉–M₁₈. With this structure, the $g_m$ is electronically adjusted by the bias current ($I_B$) as depicted in Eq. (2).

$$g_m = \sqrt{\mu_n C_{ox} \frac{W}{L} I_B},$$  \hspace{1cm} (2)

where $\mu_n$ is the electron mobility, $C_{ox}$ is the oxide capacitance, and $W/L$ is the aspect ratio of MOS M₁ and M₂ channel width and length.

Fig. 2: Electrical equivalent schematic of VD-DIBA.

The VD-DIBA implemented from the commercially available ICs is cost-effective and easier to implement. In this design, the VD-DIBA is implemented from the commercially available ICs, LM13700 by Texas Instruments [20], and AD830 by Analog Devices [21] as shown in Fig. 4. For LM13700, the $g_m$ for this VD-DIBA structure is given in Eq. (3).

$$g_m = \frac{I_B}{2V_T},$$  \hspace{1cm} (3)

where $V_T$ is the thermal voltage.

Fig. 3: CMOS transistor implementation of VD-DIBA. [19]

2.2. Proposed Circuit

In this paper, a VD-DIBA-based voltage-mode first-order all-pass filter [8] and a lossless integrator are utilized to construct the quadrature sinusoidal oscillator circuit. As shown in Fig. [5] both a first-order all-pass filter and a lossless integrator are realized using VD-DIBA as the active building block. The first-order all-pass filter consists of the components VD-DIBA₁, $C_1$, and $R_1$, $R_2$. The lossless integrator is constructed from VD-DIBA₂ and $C_2$, which is grounded. Circuit structure in Fig. 5 reveals that the output voltage nodes $V_{o1}$ and $V_{o2}$ are at the low impedance output voltage nodes $W_1$ and $W_2$, respectively. Therefore, they can be connected directly to other circuits without the need for a buffer circuit.

Fig. 4: Commercially available ICs implementation of VD-DIBA.

Fig. 5: The proposed quadrature sinusoidal oscillator.

The characteristic equation of the proposed quadrature sinusoidal oscillator shown in Fig. 5 is given in Eq. (4).

$$s^2C_1C_2 + sC_2g_{m1} - sC_1g_{m2} + g_{m1}g_{m2} = 0.$$  \hspace{1cm} (4)

If $g_{m} = g_{m1} = g_{m2}$ and $C = C_1 = C_2$, the Frequency of Oscillation (FO) of the second order characteristic
equation is given as:
\[ \omega_0 = \frac{g_m}{C}. \]  
(5)

Also, the Condition of Oscillation (CO) of the second-order characteristic equation is given by:
\[ \frac{R_1}{R_2} \geq 1. \]  
(6)

From Eq. (5) and Eq. (6), the FO and CO of the proposed quadrature oscillator can be independently adjusted. Additionally, the frequency of oscillation can be linearly and electronically controlled. For amplitude stabilization, the resistor \( R_2 \) can be easily realized from a photoresistor. This device is a part of the 3WK16341 (optocoupler with photoresistor) \[22\]. More details of the amplitude stabilization using 3WK16341 can be seen in \[24\] and \[25\]. The circuit in Fig. 5 gives the voltage ratio of \( V_{o2} \) and \( V_{o1} \) as shown in Eq. (7).

\[
\frac{V_{o2}(s)}{V_{o1}(s)} = \frac{-g_m}{sC}. 
\]  
(7)

It is found from Eq. (7) that the phase difference of output voltages \( V_{o2} \) and \( V_{o1} \) is 90° when phase of \( V_{o2} \) leads phase of \( V_{o1} \). At the frequency of oscillation \( (\omega = \omega_0) \), the magnitude ratio voltage ratio of \( V_{o2} \) and \( V_{o1} \) in Eq. (7) becomes

\[
\left| \frac{V_{o2}}{V_{o1}} \right|_{\omega = \omega_0} = \frac{g_m}{\omega_0 C}. 
\]  
(8)

Substituting the frequency of oscillation, \( \omega_0 \) depicted in Eq. (5) into Eq. (8), the magnitude ratio of \( V_{o2} \) and \( V_{o1} \) is unity as shown in Eq. (9).

\[
\left| \frac{V_{o2}}{V_{o1}} \right|_{\omega = \omega_0} = 1. 
\]  
(9)

Equation (9) revealed that if \( C_1 = C_2 \) and the frequency of oscillation is tuned by simultaneously changing \( g_{m1} \) and \( g_{m2} \) \( (I_{B1} = I_{B2}) \), the amplitude of the output voltages, \( V_{o2} \) and \( V_{o1} \) is equal over the tuning frequency range.

3. Non-Ideal Study

In this section, the effect of the non-ideal properties of VD-DIBA on the oscillator performance is considered. The non-ideal properties of VD-DIBA can be expressed in Eq. (10).

\[
\begin{bmatrix}
I_{v+} \\
I_{v-} \\
I_z \\
I_w \\
V_v \\
V_{v-} \\
V_{v+} \\
V_z \\
I_w \\
\end{bmatrix} = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
g_m & -g_m & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & -\beta_z & -\beta_v & 0 \\
-\beta_z & -\beta_v & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
\end{bmatrix} \begin{bmatrix}
V_w \\
V_v \\
V_{v-} \\
V_{v+} \\
V_z \\
V_v \\
V_{v+} \\
V_{v-} \\
I_w \\
\end{bmatrix}. 
\]  
(10)

In Eq. (10), \( \beta_z \) is the voltage gain error from \( z \) to \( w \) terminal and the \( \beta_w \) is the voltage gain error from \( v \) to \( w \) terminal. Considering those voltage gain errors, the characteristic equation of the proposed oscillator is shown in Eq. (11).

\[
\begin{bmatrix}
s^2C_1C_2 + \frac{R_1}{R_2}(1 - \beta_{v1}) + 1 \\
+ sC_2g_{m1} \left( \frac{R_1}{R_2}(1 - \beta_{v1}) + 1 \right) + \\
+ sC_1g_{m2} \left( \beta_{v1}\beta_{z2} - \beta_{z1}\beta_{v2} \right) + \frac{R_1}{R_2} - \beta_{z1}\beta_{z2}\right) + \\
\right) = 0. 
\]  
(11)

If \( g_m = g_{m1} = g_{m2} \) and \( C = C_1 = C_2 \), the frequency of oscillation of the second-order characteristic equation in Eq. (11) is given by:

\[
\omega_0 = \frac{g_m}{C} \sqrt{\frac{\beta_{v1}\beta_{z2}R_2}{R_1(1 - \beta_{v1} + R_2)}}. 
\]  
(12)

Also, the condition of oscillation of the second-order characteristic equation in Eq. (11) is given by:

\[
\frac{R_1}{R_2} \geq \frac{1 + \beta_{v1}\beta_{z2} - \beta_{z1}\beta_{v2}}{\beta_{v1} + \beta_{z1}\beta_{v2}}. 
\]  
(13)

It is found that the voltage gain errors affect both the oscillation frequency and condition frequency.

![Fig. 6: Parasitic elements in the proposed circuit.](image)

The influence of the parasitic elements in VD-DIBAs on the performance of the proposed quadrature oscillator is also studied. Figure 6 shows the involvement of parasitic elements in the proposed circuit. For easy analysis of the proposed circuit, the parallel of the parasitic element is considered as the admittance, where the admittances, \( Y_1, Y_{V1}, Y_{2+}, \) and \( Y_2 \) appeared in Fig. 6 are defined as follows:

\[
\begin{align*}
Y_1 &= s(C_{-1} + C_{Z1}) + G_{-1} + G_{Z1}, \\
Y_{V1} &= sC_{Y1} + G_{V1}, \\
Y_{2+} &= sC_{Z2} + G_{Z2} + G_{2+}, \\
Y_2 &= s(C_2 + C_{Z2}) + G_{Z2} + G_{2+}, \\
\end{align*} 
\]  
(14)

where \( G_{-1} = 1/R_{-1}, G_{Z1} = 1/R_{Z1}, G_{V1} = 1/R_{V1}, \) and \( G_{2+} = 1/R_{2+} \) and \( G_{Z2} = 1/R_{Z2}. \)
If $R_1$ and $R_2$ are much less than $R_{-1}$, $R_{Z1}$, $R_{V1}$, $R_{+2}$ $R_{Z2}$, and the operational frequency of the proposed quadrature oscillator is much less than $1/[2\pi C_1(R_1//R_2)]$, $1/[2\pi C_1(R_{W2}//R_1)]$ and $1/[2\pi C + 2(R_{W1}//R_2)]$, the characteristic equation of the proposed quadrature oscillator is given by:

$$
\begin{align*}
&= 0, \\
&\left\{ \\
&+ C_2 g_{m1} + C_{-1} g_{m2} = C_1 g_{m2} \cdot \frac{R_1}{R_2} + \\
&G_{-1} Z_{Z2} + G_{-1} Z_{m2} + g_{m1} g_{m2} \\
&\end{align*}
$$

where $C_2^* = C_2 + C_{Z2}$. The frequency and condition of oscillation of the second-order characteristic equation in Eq. (15) are given by:

$$
\omega_0 = \frac{G_{-1} Z_{Z2} + G_{-1} Z_{m2} + g_{m1} g_{m2}}{C_2^* (C_1 + C_{-1})}.
$$

and

$$
C_1 g_{m2} \frac{R_1}{R_2} \geq C_2^* G_{-1} + C_{-1} G_{Z2} + C_1 G_{Z2} + \\
+ C_2^* g_{m1} + C_{-1} g_{m1}. \\
$$

It is found that the parasitic element in VD-DIBA affects the frequency and condition of oscillation as well as the operating limitation at high frequency. It is also noted that $R_1$ and $R_2$ should be low for getting a higher frequency of operation.

4. Simulated Results

PSPICE is used to be the tool for simulating the workability of the proposed quadrature sinusoidal oscillator shown in Fig. 3. The simulation is carried out by using the VD-DIBA constructed from the CMOS transistors as shown in Fig. 3. The CMOS model parameters are offered by 0.18 μm TSMC technology in level 7 [22]. The power supply is ±0.9 V, $V_B = 0.23$ V and $I_{B1} = I_{B2} = 22 \mu A$ ($g_{m1} = g_{m2} = 80 \mu A$). The aspect ratios (W/L) of MOS transistors, M1–M2, M3–M6, M7–M13, M14–M15 and M16–M18 are respectively chosen as: 2.4 μm/1.8 μm, 3.6 μm/1.8 μm, 40.5 μm/0.54 μm, 2.4 μm/1.8 μm and 13.5 μm/0.54 μm. The passive elements are chosen as: $C_1 = C_2 = 12$ pF, $R_1 = 1.075$ kΩ, $R_2 = 1$ kΩ. The simulation illustrated in Fig. 6 is the sinusoidal output waveform in the initial state until steady state. It is found that the sinusoidal signal has entered a steady state after $t \approx 200 \mu s$. The quadrature sinewave at a steady state is shown in Fig. 7. It is found that the amplitudes of sinusoidal output voltages, $V_{o1}$ and $V_{o2}$ are 162.01 mV$_{pp}$ and 160.17 mV$_{pp}$, respectively. The simulated magnitude ratio of $V_{o2}$ and $V_{o1}$ is 0.988 (1.2 % error) which is closed to unity as depicted in Eq. (9). The phase of the sinusoidal output voltage $V_{o2}$ leads the phase of the sinusoidal output voltage $V_{o1}$ by 89.41° (0.65 % error) which is consistent with the theoretical analysis as depicted in Eq. (7). The simulated $f_0$ is 1.03 MHz (2.64 % error). The THDs of the sinusoidal output voltages, $V_{o1}$ and $V_{o2}$ are 1.63 % and 1.81 %, respectively. Figure 9 shows the output spectrum of the sinusoidal output voltages $V_{o1}$ and $V_{o2}$.

![Fig. 7: Output response during initial state.](image)

![Fig. 8: Quadrature sinusoidal waveform.](image)

![Fig. 9: Simulation result of the output spectrum.](image)

The plot of theoretical and simulated $f_0$ against the bias current is shown in Fig. 10. In this simulation, the bias current ($I_{B1} = I_{B2} = I_B$) is varied from 10 μA to 80 μA. With these variations of the bias current, the simulated $f_0$ is adjusted from 0.71 MHz to 1.72 MHz which is consistent with the theoretical analysis as depicted in Eq. (8). This simulation result confirms that the frequency of oscillation is electronically controlled. This advantage feature is easily controlled by the microcomputer or microcontroller.
for modern circuit applications. Figure 11 shows the simulated $V_{o2} - V_{o1}$ phase relationship against the frequency of oscillation. The phase difference swings from 86.75$^\circ$ (at $f_0 = 1.2$ MHz) to 91.41$^\circ$ (at $f_0 = 0.86$ MHz) which is close to the theoretical expectation (90$^\circ$) as depicted in Eq. 7.

![Fig. 10: Dependence of frequency of oscillation on the bias current.](image)

![Fig. 11: $V_{o2} - V_{o1}$ phase relationship against the simulated frequency of oscillation.](image)

Figure 12 depicts the amplitude of the quadrature sinusoidal output voltages $V_{o1}$ and $V_{o2}$ versus the simulated oscillation frequency. Over the tuning frequency range, the amplitude of the sinusoidal output voltage, $V_{o1}$, is found to be close to the amplitude of the sinusoidal output voltage, $V_{o2}$, as determined by Eq. 9. Due to the non-ideal features of VD-DIBA, the amplitude of the sinusoidal output voltage, $V_{o2}$, is somewhat less than the amplitude of the sinusoidal output voltage, $V_{o1}$. Figure 13 depicts the percent THD of the quadrature sinusoidal waveforms $V_{o1}$ and $V_{o2}$ versus the oscillation frequency. THD varies from 1.48 % (at $f_0 = 0.86$ MHz) to 3.51 % (at $f_0 = 1.2$ MHz) for the sinusoidal output voltage, $V_{o1}$. $V_{o2}$ THD varies from 0.84 % (at $f_0 = 1.70$ MHz) to 1.81 % (at $f_0 = 1.03$ MHz).

![Fig. 12: Amplitudes of $V_{o1}$ and $V_{o2}$ against the simulated $f_0$.](image)

![Fig. 13: The THD of the quadrature waveforms $V_{o1}$ and $V_{o2}$ against the simulated $f_0$.](image)

5. Experimental Results

Using the VD-DIBA constructed from commercial ICs AD830 and LM13700, as shown in Fig. 4, the performance of the proposed quadrature sinusoidal oscillator is experimentally evaluated. The power supply is ±5 V, $I_{B1} = I_{B2} = 172 \mu$A ($g_{m1} = g_{m2} = 3.44$ mS), $C_1 = C_2 = 1$ nF, $R_1 = 1.14$ kΩ, $R_2 = 1$ kΩ. The measured quadrature waveform is shown in Fig. 14. It is found that the amplitudes of the quadrature sinusoidal output voltages, $V_{o1}$ and $V_{o2}$, are 54.90 mVp–p and 56.76 mVp–p, respectively. The experimental magnitude ratio of the sinusoidal output voltages $V_{o2}$ and $V_{o1}$ is 1.034 (3.4 % error) which is closed to unity as depicted in Eq. 9. In this experiment, the phase of the sinusoidal output voltage $V_{o2}$ leads the phase of the sinusoidal output voltage $V_{o1}$ by 92.27$^\circ$ (2.52 % error) which is consistent with the theoretical analysis as depicted in Eq. 7. The experimental $f_0$ is 536.6 kHz (2.11 % error). The THDs of the sinusoidal output voltages, $V_{o1}$ and $V_{o2}$ obtained from the experiment are 1.43 % (~36.875 dB) and 1.00 % (~40 dB), respectively. Fig. 15 shows the measured output spectrum of the sinusoidal output voltages $V_{o1}$ and $V_{o2}$.

The plot of theoretical and experimental $f_0$ against the bias current is shown in Fig. 16. In this exper-
Fig. 14: Measured quadrature sinusoidal waveform.

Fig. 15: Experimental output spectrum of the sinusoidal waveforms.

Fig. 16: Dependence of the measured $f_0$ on the bias current.

The amplitude of the quadrature sinusoidal waveforms, $V_{o1}$ and $V_{o2}$ against the frequency of oscillation obtained from the experiment is plotted in Fig. 18. It is found that the amplitude of the sinusoidal output voltage, $V_{o1}$ is close to the amplitude of the sinusoidal output voltage, $V_{o2}$ over the tuning frequency range as analyzed in Eq. (9). However, the amplitude of the sinusoidal output voltage, $V_{o1}$ is a little less than the amplitude of the sinusoidal output voltage, $V_{o2}$ due to non-ideal properties of VD-DIBA. Figure 19 shows the experimental result of the percent of THD of the quadrature sinusoidal waveforms $V_{o1}$ and $V_{o2}$ against the frequency of oscillation. The percent of THD for the sinusoidal output voltage, $V_{o1}$ swings from 0.931% (at $f_0 = 1.25$ MHz) to 2.943% (at $f_0 = 103.51$ kHz). The percent of THD for the sinusoidal output voltage, $V_{o2}$ swings from 0.45% (at $f_0 = 1.25$ MHz) to 2.54% (at $f_0 = 103.51$ kHz).
The simulated power consumption is 1.37 mW. In addition, the proposed oscillator is experimentally tested using VD-DIBA constructed from the commercial ICs with ±5 V. The experiment revealed that the magnitude ratio of \( V_{o2} \) and \( V_{o1} \) is 1.034 (3.4 % error). The phase of \( V_{o2} \) leads the phase of \( V_{o1} \) by 92.27° (2.52 % error). The experimental \( f_0 \) is 536.6 kHz (2.11 % error). The THDs of \( V_{o1} \) and \( V_{o2} \) obtained from the experiment are 1.43 % and 1.00 %, respectively. The experimental power consumption is 265.7 mW.

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### Author Contributions

Conceptual framework, A.K., D.D. W.J.; Simulation, D.D., and S.Y.; Experimental, A.K., and W.J.; Formal analysis and writing-original draft preparation, A.K., W.J., D.D., and S.Y.; Verified the analytical methods, A.K.; All authors have discussed the results and contributed to the final manuscript.

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