HDI flexible front-end hybrid prototype for the PS module of the CMS tracker upgrade

M. Kovacs, G. Blanchot, T. Gadek, A. Honma and A. Koliatos

CERN, European Organization for Nuclear Research
Route de Meyrin, CH-1211 Geneva 23, Switzerland

E-mail: mark.istvan.kovacs@cern.ch

ABSTRACT: The CMS tracker upgrade for the HL-LHC relies on different module types, depending on the position of the respective module. They are built with high-density interconnection flexible circuits that are wire bonded to silicon strip and pixel-strip sensors. The Front-End hybrids will contain several flip-chip bonded readout ASICs that are still under development. Mock-up prototypes are used to qualify the advanced flexible circuit technology and the parameters of the hybrids. This paper presents the Pixel-Strip (PS) mock-up hybrid in terms of testing, interconnection, fold-over, thermal properties and layout feasibility. Plans for circuit testing at operating temperature (-30°C) are also presented.

KEYWORDS: Front-end electronics for detector readout; Radiation-hard electronics; Detector design and construction technologies and materials; Manufacturing

1 Corresponding author.
## 1 Introduction to the CMS tracker upgrade for the HL-LHC

A major upgrade of the CMS detector is required to cope with the planned 3000 fb$^{-1}$ integrated luminosity of the High Luminosity LHC (HL-LHC) [1]. The development of the new front-end modules for the CMS outer tracker aims to deliver electronics, featuring approximately 4 times higher granularity, lower mass (23–25 g per module) and capability for data rates up to 10,24 Gbps/module [1, 2]. Rejection of low momentum tracks is executed in the front-end electronics by correlating the signals locally from a pair of silicon sensors. A new Level one (L1) track triggering functionality, which helps to reduce the L1 trigger rate, is also implemented [3]. In the upgraded outer tracker design, there are two main module types and several module subtypes with different sensor separations ranging from 1.6 mm to 4 mm. The two main module types are the Strip-Strip (2S) (figure 1) and the Pixel-Strip (PS) (figure 2) modules. The 2S module is constructed from two silicon strip sensors to enable the low momentum track rejection. The PS module consists of a silicon strip and a pixel strip sensor paired in order to provide additional z-axis information. The PS front-end hybrid hosts the Short Strip ASICs (SSA) [4] and a Concentrator ASIC (CIC) [5]. The SSA and the CIC chips will use bump bonds to interconnect to the front-end hybrid circuit. Due to the 250 and 270 µm pitch of the bump bonds on the CIC and the SSA respectively, the hybrid circuits have to use...
High Density Interconnect (HDI) technology. This technology allows for a direct sensor wirebond connection to the front-end hybrids and it provides significant size and mass reduction compared to conventional printed circuit technology.

1.1 The PS module and the PS front-end hybrid

The PS module is constructed from two PS front-end hybrids, a power service hybrid, an optical link service hybrid, a silicon strip sensor, a Macro Pixel Sensor Assembly (MAPSA) with the Macro Pixel ASICs (MPA) [6] and several structural components. The MAPSA and the strip sensor are placed on a special spacer to provide the appropriate spacing required for the low momentum track rejection. The PS hybrid is designed to match this spacing and it is folded over to provide wirebond connections for both sides of the module (figure 3). The front-end hybrid is glued on carbon fibre stiffeners, providing sufficient stiffness and flatness for the flip-chip bonding. The stiffeners improve the thermal properties of the hybrid, while preserving the low mass of the assembly. The PS hybrid is using HDI circuit technology to accommodate all the required features in a very small circuit area [7].

![Figure 1](image1.png) Top view of the 2S module design.  
![Figure 2](image2.png) Top view of the PS module design.  
![Figure 3](image3.png) PS module cross section view at the front-end hybrid fold over.

2 PS-MCK project introduction

Flexible HDI substrate circuits using flip-chip bumped ASICs were recently introduced to the High Energy Physics (HEP) community [7] and limited information is available on the reliability, yield, cost and other parameters of these circuits. Therefore, the hybrid development requires several
prototyping steps to achieve a mature design. The hybrid assembly procedure and the mechanical structures of the modules require precise alignment tools and complex assembly procedures. State-of-the-art structural materials such as aluminium-carbon composites are used to achieve light modules with an excellent thermal performance. A prototype hybrid is required to test the materials, assembly procedure, test methods and the thermal performance of the modules while the SSA, CIC and MPA ASICs are all under development. The PS-MCK is designed to serve as a test hybrid to help the prototyping related to the module construction. This paper presents the design of this hybrid emphasising the implementation of different test features.

2.1 PS-MCK hybrid requirements and features

The main requirement of the mock-up hybrid is to serve as an object that has the mechanical properties of the fully functional PS front-end hybrids. In order to fulfill this requirement, the hybrid is built on a four-layer polyimide substrate, featuring HDI technology [7]. Seven dummy flip-chips, two active CMS Binary Chip second prototype (CBC2) [8] chips, several passive components and connectors are assembled on the circuit. The PS-MCK assembly requires a fold-over, such as the PS front-end hybrid (figure 4). Carbon fibre stiffeners are glued on the backside of the circuit to provide sufficient stiffness and a good thermal performance. Heating resistors and a thermistor are placed along the circuit to aid the module thermal performance verification. The PS-MCK hosts also test circuits to qualify different solutions for the electronic design of the PS front-end hybrid. The module data and power connectivity plans need to be tested. The PS-MCK is equipped with several connectors for this reason. A prototype high voltage biasing circuit is required for sensor tests. The first prototype of this high voltage circuit is implemented in the PS-MCK.

![Figure 4. The 3D model of the PS-MCK hybrid after folding.](image)

The production testing of PS front-end hybrids requires several signals to be interconnected with a test system and specific test routines to assure that the hybrid operates properly. Two spring loaded needle tester patterns and an antenna evaluation circuit are implemented in the PS-MCK to validate these test methods. An antenna tester evaluation circuit (section 3.8) is implemented to qualify a test method for the analogue front-end connectivity on the hybrid [9].

The PS-MCK serves as a sample design for the hybrid circuit supplier qualification procedure. It implements fine line structures, via daisy chains, layer alignment test, controlled impedance test circuit and a daisy chain flip-chip to provide basis for comparison of different suppliers. A 4 × 4 mm² area is allocated for an encoded optical identification of the hybrid serial number and other information.

3 PS-MCK hybrid layout implementation

The PS front-end hybrid has limited space due to the PS module requirements. The dummy CBC flip-chips and the CBC2 chips occupy a large surface area on the hybrid. The implemented test
features and the high voltage circuit leave almost no free space on the circuit. The HDI flex design requires special features to improve the production yield of the hybrids: the copper film area has to be well balanced to achieve good circuit surface flatness, fillets are needed to improve the circuit reliability and holes need to be etched in the copper planes larger than 1 mm$^2$ to improve the adhesion of the adhesive layers used for the circuit build-up process. In the circuit routing, 45 $\mu$m wide traces and spacing are used. The smallest via capture pad diameter is 110 $\mu$m with 25–50 $\mu$m diameter holes. Via in pad technology with copper filled vias is used to improve the circuit reliability and to ease the fan-out routing of the flip-chips. The substrate has 25 $\mu$m dielectric thickness and 9–12 $\mu$m copper thickness.

3.1 Hybrid floorplan

The PS-MCK provides the best achievable representation of the PS front-end hybrid, while it implements numerous test features. The figure 5 shows the distribution of different functions along the two sides of the unfolded hybrid marked with numbers.

![Figure 5. The floorplan of the PS-MCK hybrid.](image)

The features of the PS-MCK are explained in the following sections:

1. Test coupon (3.2).
2. Spring loaded needle connection pads and wirebond pads for dummy MPA chips (3.3).
3. Space allocated for the individual hybrid identification (3.4).
4. Fold-over region with voids and impedance test structures (3.5).
5. High voltage bias circuit with HV and low voltage input connectors (3.6).
6. Dummy CBC chips with heating resistors and fine line daisy chain. (3.7).
7. CBC2 chips with implemented hybrid routing failures (3.8).
8. Mezzanine connector for testing (3.9).

3.2 Test coupon

The PS-MCK serves as a reference design to qualify different hybrid suppliers [13]. A test coupon is designed to test the quality and reliability of each circuit. The coupon is manufactured together with the circuit substrate and it is separated just before the assembly of the surface mount components. The test coupon can be used for accelerated stress tests to evaluate the reliability of the
via metallization and the flip-chip bump bonds without sacrificing the main circuit. To enable these tests, the coupon hosts a via daisy chain with more than 700 vias and a Topline FC317G5E254-DC flip-chip with 317 Sn$_{63}$Pb$_{37}$ eutectic bumps [10]. A layer alignment test and a fine line test structure are also implemented. The figure 6 illustrates the implemented elements in the test coupon.

![Layout of the test coupon](image1)

![Layout of the test flip-chip](image2)

![Via structure cross section](image3)

![Layer alignment test structure](image4)

**Figure 6.** Illustration of the implemented structures in the test coupon.

### 3.3 Spring loaded needle connection pads

Testability is an important feature of a circuit design. It has to be planned carefully, otherwise it can result in additional design iterations causing delay in the development. The PS hybrid is highly miniaturized, therefore it is complicated to test the functionality of a standalone hybrid. The current PS module design also complicates the standalone functional testing, because the MPA ASIC is connected to the hybrid at the last module construction step by wirebonds (figure 3). The MPA is one of the key elements of the PS module data path (figure 7) as the correlation logic is located in this ASIC. All the interconnections between the MPA to SSA and the MPA to CIC chips need to be probed in order to carry out a full functional test of the hybrid. One solution is to use 350 spring loaded needle probe (POGO) test points to access the SSA to MPA and MPA to CIC signals, together with a 70 POGO pin contact array or a mezzanine connector to connect to the optical link service hybrid data signals.

![Data and control signal path on the PS module](image5)

**Figure 7.** Data and control signal path on the PS module.

A daisy chain probe pattern and a fine pitch mezzanine connector are implemented in the PS-MCK to test the feasibility and reliability of these connectivity methods. The POGO test needles
have to be inserted in a custom socket (figure 8), which needs to be aligned precisely to the hybrid. Alignment holes are laser cut in the hybrid to aid the assembly and to align the test sockets precisely.

![Figure 8. Drawings of a 70 pin POGO socket (left) and a 350 pin POGO socket (right).](image)

The pitch of the probe needles is 825 µm and the contact pad size is 400 µm in the case of the large MPA, SSA and CIC signal probe socket (figure 8). In the case of the smaller socket to probe the optical link service hybrid data signals, the pitch of the needles is 850 µm and 600 µm depending on the direction. The contact pad diameter is 350 µm. The applied dimensions of the sockets require high precision manufacturing and alignment. The two probe sockets and the interfacing PCB boards will be installed in a test box that is designed to cool the PS-MCK to the module operating temperature (-30°C) to perform a realistic functional test [9].

### 3.4 Individual hybrid identification

Each hybrid has to have a unique identifier assigned at the circuit manufacturer. By using this identifier, each step can be tracked towards the full module assembly. This identifier needs to be readable by an optical scanner device. Due to the space requirements, the allocated space for this identifier is 4 × 4 mm$^2$ and the pixel size can be as small as 100 × 100 µm$^2$. The format of the identifier can be any type of a two dimensional pixel matrix, which can encode up to 26 characters. The readability and implementation of different formats are tested on the PS-MCK.

### 3.5 Fold-over region with voids and impedance test structure

The PS-MCK is used to practice the assembly and fold-over process of the final PS hybrid. The hybrid has a flexible region to enable the folding, but the sharp folding of a 100 mm long edge is difficult and requires large forces. The PS-MCK introduces voids in the flexible circuit region to reduce the required force needed for the folding. High speed differential signals are passing through the fold-over region of the circuit. The folding process might change the characteristic impedance of the signal lines [11]. The PS-MCK has differential test lines to measure this effect.

### 3.6 High voltage bias circuit and low voltage power connector

The PS module requires a high voltage biasing circuit to be placed on one of the front-end hybrids. The circuit is rated, for up to 1000V and it has to fit all the components in the less than 15 × 10 mm$^2$ space allocated. In order to decrease the electric field close to the component pins, all the contact pad corners are rounded. The high voltage circuit is conformal coated after the assembly for safety reasons. A one pin (JAE ES3) connector is used for high voltage supply input and the high voltage ground return connection is routed together with the low voltage supply. The bias connection to the silicon strip sensor uses a flexible tab connected to an FPC connector (Panasonic YPW5) and
wirebonded to the strip sensor. The low voltage supply from the power service hybrid is connected through a miniaturized mezzanine connector (JAE WP10). All the listed connectors in figure 9 will be tested for radiation tolerance, reliability and assembly.

![Figure 9. Pictures of three different types of connectors mounted on the PS-MCK.](image)

### 3.7 Dummy CBC chips with fine line daisy chain

Dummy CBC flip-chips are substituting the mechanical properties of the SSA and the CIC chips on the PS-MCK. The dummy CBC chips have 738 high lead bumps with 250 µm pitch and 147 µm ball diameter. The dummy CBCs are providing a good representation of the assembly difficulty and the mechanical properties that the SSA chip will have. The PS-MCK is used to validate the PS module thermal performance. To simulate the heat dissipation of the SSA and CIC ASICs, the hybrid is fitted with several heating resistors with a total heat dissipation power of 1.2 W. The hybrid has large heat management planes and several vias implemented to improve the heat conduction in the hybrid. Metallized contact pads are facing the carbon fibre stiffener to enhance the cooling path.

A daisy chain structure with three individual nets is routed on the hybrid to represent the fine line routing required to connect the SSA analogue inputs to the silicon strip sensor wirebond pads. With this test structure, open lines and shorts can be detected (figure 10).

![Figure 10. The fine line daisy chain (left) and the front side of the CBC dummy chip (right).](image)
3.8 Two CBC2 chips with implemented hybrid routing failures for test method validation

Testing the interconnection of the silicon strip sensor wirebond pads through the bump bonds to the analogue front-end is part of the functional testing. The bump connections cannot be inspected visually and probing the wirebond pads is difficult, due to the 130×300 µm pad size and the 100 µm staggered pitch. In addition, probing the surface of the pads can cause damage and contamination that can affect the quality and reliability of the wirebonds. A test method, which does not require physical contact to the surface of the wirebond pads, was developed using the charge sensitivity of the analogue front-end. An antenna is placed close to the wirebond pads and a fast transition signal is applied. Due to the capacitive coupling to the pads, charge is injected into the front-end inputs. If the signal trace has an open circuit, the signal will not be sensed by the front-end, therefore it can suspect a failure [9]. If the antenna is applied externally, it has to be placed very precisely to keep the test reproducible. The antenna placement and alignment requires complicated mechanical structures (figure 11) and significant time and manpower during the production testing of the front-end hybrids.

![Figure 11. External antenna circuit with metal frame, designed for testing a 2S front-end hybrid prototype [7].](image)

The integration of the antenna pads in the hybrid can eliminate the alignment problem, but it consumes valuable routing space in the highest routing density region of the hybrid. This embedded antenna pad would be grounded after the functional tests of the front-end hybrid, as the floating pad might couple noise or unwanted cross talk into the analogue inputs. The PS-MCK implements failures to enable the validation of the embedded antenna and the external antenna test method (figure 12). The hybrid is designed with two CBC2 chips with 127 analogue inputs routed to the strip sensor wirebond pads. One of the chips is equipped with the embedded antenna to provide comparable information about the added noise to the system. Each chip routing has missing via drills, shorted bump pads, shorted traces, shorts to ground and broken traces equally distributed along the inputs. The antenna pads are placed below the wirebond pads and their size is set to inject the same amount of charge to each channel. The coupling capacitance is approximately 35 fF to each input channel.
3.9 Mezzanine connector for data connection and testing

The Panasonic A35S [12], a recently developed miniaturized mezzanine connector, featuring 350 μm pitch and 50 pins is tested on the PS-MCK. The connector could replace the wirebonded connections to and from the optical link service hybrid and it could simplify the module assembly procedure. The connector could also serve as a testing interface with the usage of a special mating part. In this case, one of the spring probes is not required for the functional testing. On the PS-MCK the Panasonic A35S connector is providing access to the important test signals in parallel with the 70 pin POGO spring probe, therefore both interfaces can be used for testing this circuit. Only limited information can be found on the reliability and radiation tolerance of the A35S connector, therefore these tests will be performed on the PS-MCK as a verification. On later prototypes this connector will replace the 70 pin POGO spring probe if promising test results are produced with the PS-MCK.

4 Future work

The testing of the PS-MCK requires a dedicated test setup and interface card with test features. The mock-up will be tested at the nominal operating temperature (-30°C). A hermetic test box with dry air injection is currently being designed for the PS-MCK. The test box will host the interface PCB which implements a USB to SPI interface to control and read the different test peripheries such as analogue to digital converters, oscillator, potentiometer and switches. Reliability and radiation tolerance testing is also planned for the PS-MCK.

5 Conclusion

The PS-MCK is designed to represent the geometrical and the thermal properties of the PS front-end hybrid until the SSA, MPA and CIC ASICs are designed and manufactured. The mock-up is used to practice the complicated PS module construction. Test features are implemented in order to efficiently use the circuit. These tests will provide valuable information for the design, production and testing of the PS front-end hybrid. A high voltage circuit, miniature mezzanine connectors, spring loaded needle contacts and a laser marked identification are placed on the circuit. The effect
of the fold-over on the characteristic impedance, the performance of the embedded antenna and the spring loaded needle contacts are tested. The hybrid assembly steps, the fold-over process and the thermal performance are also evaluated. The PS-MCK serves as a reference design for the price enquiry No.: DO-30038/EP [13] to select the appropriate hybrid manufacturer consortia.

References

[1] D. Abbaneo, Upgrade of the CMS Tracker with tracking trigger, 2011 JINST 6 C12065.
[2] D. Abbaneo et al., Technical proposal for the Phase-II upgrade of the compact muon solenoid, https://cds.cern.ch/record/2020886/files/LHCC-P-008.pdf.
[3] N. Pozzobon, Development of a Level I Track Trigger for the CMS Experiment at the High-Luminosity LHC, Nucl. Instrum. Meth. A 732 (2013) 151.
[4] A. Caratelli, D. Ceresa, J. Kaplon, K. Kloukinas and S. Scarfi, Short Strip ASIC specification document.
[5] L. Caponetto, S. Viret and Y. Zoccarato, CIC1 specification document.
[6] A. Caratelli, D. Ceresa, J. Kaplon, K. Kloukinas, S. Scarfi, Macro Pixel ASIC Specification, https://espace.cern.ch/CMS-MPA/SiteAssets/SitePages/Documents/MPA_specs_V1_1.pdf.
[7] M. Kovacs et al., Flexible Front-End Hybrids for the CMS Outer Tracker Upgrade, 2015 JINST 10 C01046.
[8] D. Braga, G. Hall, L. Jones, P. Murray, M. Pesaresi, M. Prydderch and M. Raymond, CBC2: a microstrip readout ASIC with coincidence logic for trigger primitives at HL-LHC, 2012 JINST 7 C10003.
[9] T. Gadek et al., Testing of the Front-End Hybrid Circuits for the CMS Tracker Upgrade, in the proceedings of the Topical Workshop on Electronics for Particle Physics, Karlsruhe, Germany, 2017 JINST 12 C01010.
[10] Datasheet of the FC317G5E254-DC daisy chain flip-chip, http://www.topline.tv/drawings/pdf/flip_chip/FC317G5.08E254.pdf.
[11] M. Kovacs et al., Transmission lines implementation on HDI flex circuits for the CMS tracker upgrade, 2016 JINST 11 C01081.
[12] Datasheet of the Panasonic A35S mezzanine connector, https://www.panasonic-electric-works.com/pew/hu/downloads/ds_65318_en_a35s.pdf.
[13] G. Blanchot, A. Honma, M. Kovacs and F. Vasey, Technical Specification for the Development of Hybrid Circuit Prototypes for the CMS Tracker Upgrade.