Analysis of Capacitor Voltage Imbalance in Hybrid Converters and Inherently Balanced Operation Using Symmetric Architecture

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Abstract—This letter investigates the origin of the flying capacitor voltage imbalance in hybrid converters. An intuitive voltage-charge relationship is established to give a general explanation of the flying capacitor voltage balance in hybrid converters. The relationship is applied to devise a relatively simple and intuitive method to identify the behavior and performance difference of capacitor voltage and inductor current balancing performance in hybrid converters for $V_{\text{out}} < \frac{V}{N}$ cases. Conventional hybrid converters with an even number of inductor charging intervals are shown to be susceptible to flying capacitor voltage imbalance, while flying capacitors in hybrid converters with odd charging intervals have inherently balanced operations. As a direct result of the analysis, a new symmetric architecture and the operation of three-level buck converters are introduced to achieve an inherent balance of flying capacitor voltages, which can be applied to other flying capacitor multilevel converters. Hardware prototypes are implemented and measured for the verification of the analytical analysis and the new symmetric operation.

Index Terms—FCML converters, hybrid converters, multilevel converters, switched capacitor, voltage balance.

I. INTRODUCTION

WITCHED-CAPACITOR (SC)-based converters with added inductors for the partial or full soft charging of flying capacitors, simply known as hybrid converters, have drawn a lot of recent interest from industry and academia because of their benefits in optimizing passive components, inductors, and capacitors for higher performance operations [1], [2]. The voltage balancing of flying capacitors in flying capacitor multilevel (FCML) converters is a well-known challenge that attracts a lot of effort in the research community. While effective solutions can be relatively diverse [3], [4], it is important to understand the original mechanism that causes this problem. Using two different approaches, i.e., Fourier-based harmonic analysis in [5] and state-space analysis in [6], it has been shown that capacitor voltages in an $(N+1)$-level FCML converter $(N$ is the number of flying capacitors), shown in Fig. 1(a), become exponentially unbalanced at some nominal conversion ratios. Additional operating states were introduced in [7] to overcome the problems in a five-level FCML converter. Analytical efforts to explain the problem with practical timing mismatches in FCML converters were also carried out in [8] and [9]. The work in [8] numerically shows that the balancing performance of odd-level $(N$ is even) FCML converters is more sensitive than that of even-level $(N$ is odd) ones. This analysis is also aligned with the one reported in [10] in terms of identifying the difference of odd- and even-level converters. In [9], the sensitivity of the flying capacitor voltage was calculated for a three-level buck converter and a four-level series capacitor buck converter.

The analysis in this letter focuses on the converters with output voltages $V_{\text{out}}$ satisfying $V_{\text{out}} < \frac{V}{N}$, where $V_{\text{in}}$ is the input voltage, and develops a general method to identify the balancing issue in hybrid converters with fundamentally different structures. This letter starts with deriving the voltage–charge relationship, which is later applied to explain the differences in the balancing performances of different hybrid converters. A modified symmetric architecture is also proposed to achieve inherent balance in popular FCML converters.

II. VOLTAGE–CHARGE RELATIONSHIP

In order to accurately determine the capacitor voltages to analyze a possible voltage imbalance scenario, it is critical to monitor the switching node voltages that directly reflect flying capacitor voltages as well as inductor currents. For this goal, we first develop a relationship between the charge flow and switching node voltages in a general FCML converter shown in Fig. 1(a). This relationship can be constructed by the inductor current ripples that actually carry the information of the switching node voltages, the output voltage, as well as the charges passing through each capacitor.

Fig. 2 depicts a general waveform of the inductor current of an FCML converter in Fig. 1(a), operating in the inductive region and $V_{\text{out}} < \frac{V}{N}$. $D_{k-2}T_S$, $D_{k}T_S$, and $D_{k+2}T_S$ represent three consecutive charging intervals, while $D_{k-1}T_S$ and $D_{k+1}T_S$ are the intermediate freewheeling intervals when the inductor is connected between ground and $V_{\text{out}}$. Note that in a three-level buck converter [see Fig. 1(b)], a special FCML converter, $D_{k-2}T_S$ and
Fig. 1. Schematics of several FCML converters. (a) \((N + 1)\)-level FCML converter. (b) Three-level buck converter. (c) Four-level FCML converter. (d) Five-level FCML converter. (e) Six-level FCML converter.

\(D_{k+2}T_S\) denote the same interval of two consecutive switching periods.

Assume that \(Q_{k-2}, Q_k,\) and \(Q_{k+2}\) are the charges through the corresponding voltages at the switching node \(V_x\) [see Fig. 1(a)], \(V_{k-2}, V_k,\) and \(V_{k+2},\) during the timing intervals \(D_{k-2}T_S,\) \(D_kT_S,\) and \(D_{k+2}T_S,\) respectively. Using the median currents and discharging coefficients \(b_{k-2}, b_k,\) and \(b_{k+2}\) in Fig. 2 for the voltage–second balance and charge balance, a relation among these charges and the corresponding switching node voltages, \(V_{k-2}\) and \(V_{k+2},\) can be found

\[
(V_{k-2} - V_{out}) \frac{b_{k-2}D_{k-2}T_S}{L} - (V_{k+2} - V_{out}) \frac{b_{k+2}D_{k+2}T_S}{L}
= \frac{2}{T_S} \left[ \frac{2Q_k}{b_kD_k} - \frac{Q_{k-2}}{b_{k-2}D_{k-2}} + \frac{Q_{k+2}}{b_{k+2}D_{k+2}} \right]
+ 2V_{out} (D_{k-1} - D_{k+1}) \frac{T_S}{L}.
\]

(1)

As shown in [9], while \(b_{k-2}, b_k,\) and \(b_{k+2}\) are very close to 1 in most practical cases, their actual values are important for modeling accuracy. The relationship described by (1), which was not established in [9], is general for all the step-down \(V_{out} < \frac{V_x}{N}\) hybrid converters with inductor(s) at the output and freewheeling to the ground, regardless of timing mismatches, voltage imbalances, or other nonidealities in the converter operations.

Analyzing this relationship in an ideal (no mismatch) case or in the case of small mismatches among parameters of the same type that satisfy the following four conditions: 1) \(b_{k-2} \rightarrow b_k \rightarrow b_{k+2};\) 2) \(D_{k-2} \rightarrow D_k \rightarrow D_{k+2};\) 3) \(D_{k-1} \rightarrow D_{k+1};\) and 4) \(Q_{k-2} \rightarrow Q_k \rightarrow Q_{k+2}\) (the arrow \(\rightarrow\) means “approaches” or “approximately equals”), one can find that the two alternate charging voltages converge

\[V_{k-2} \rightarrow V_{k+2}.
\]

(2)

This corollary is true for any alternate charging voltages at \(V_x\) regardless of their positions in the cycle or across two switching cycles of the converter. While the alternate charging voltages converge, the two consecutive charging voltages at \(V_x\) node, \(V_{k-2}\) and \(V_k,\) or \(V_k\) and \(V_{k+2},\) can diverge and become significantly different along with capacitor voltage imbalances because of load conditions and various nonidealities, such as input impedance, equivalent series resistance, parasitic resistance, and timing mismatches in the circuit. The exact amount of divergence can only be calculated if all these parameters are known. The two consecutive voltages only converge in the case of balanced operation. In other words, the \(V_x\) swing in the FCML converter essentially has one of the two voltage levels in the current charging phases of the inductor. These two voltage levels are at two consecutive charging phases. They diverge in imbalanced operations but converge when balanced.

The corollary can be used to understand the voltage imbalance and inductor current fluctuations in FCML converters as well as other hybrid converters.

III. APPLICATION TO MULTILEVEL CONVERTERS

Odd- and even-level FCML converters show significantly different balancing performances. In a traditional architecture and operation, an even-level (odd-level) FCML converter has an odd (even) number of flying capacitors and an odd (even) number of inductor charging intervals. In our analysis, we found that difference in the balancing performance has directly resulted from the number of inductor charging intervals rather than the capacitor numbers or the SC voltage division. Sections III-A and III-B explain this difference using the voltage–charge relationship and its corollary.

A. Inductor Current With an Odd Number of Charging Intervals

As an example, Table I lists the switching node voltages at \(V_x\) of a six-level \((N = 5)\) FCML converter [see Fig. 1(e)]. There are
TABLE I
VX OF THE SIX-LEVEL FCML CONVERTER

| States | 1 | 2, 4, 6, 8, 10 |
|--------|---------------|
| VX     | Vx in − VC1  | VC2 − VC3 |
| 1      | 3            | 5          | 7          | 9          | 0        |

Fig. 3. Symmetric three-level buck converter.

| States | 1 | 2, 4, 6, 8, 10 |
|--------|---------------|
| VX     | Vx in − VC1  | VC2 − VC3 |
| 1      | 3            | 5          | 7          | 9          | 0        |

Table II shows the switching node voltages at VX of a five-level (N = 4) FCML converter [see Fig. 1(d)]. There are four charging intervals (1, 3, 5, and 7) and four discharging intervals (2, 4, 6, and 8) for the inductor current. Switching node voltages at VX during intervals 1 and 5 make one converging group, Vx in − VC1 ≅ VC2 − VC3, whereas those of intervals 3 and 7 make another group, VC1 − VC2 ≅ VC3. Note that, unlike even-level converters, these two sets of charging voltages neither exchange in the next cycle nor converge. Therefore, when timing mismatches occur, these two sets of voltages can diverge and cause voltage imbalance in flying capacitors as well as fluctuations in the inductor current. The same characteristic is present in all other odd-level members (N is even) of the FCML converters, which becomes a challenge in fully utilizing the benefits of the FCML architecture.

B. Inductor Current With an Even Number of Charging Intervals

Table II shows the switching node voltages at VX of a five-level (N = 4) FCML converter [see Fig. 1(d)]. There are four charging intervals (1, 3, 5, and 7) and four discharging intervals (2, 4, 6, and 8) for the inductor current. Switching node voltages at VX during intervals 1 and 5 make one converging group, Vx in − VC1 ≅ VC2 − VC3, whereas those of intervals 3 and 7 make another group, VC1 − VC2 ≅ VC3. Note that, unlike even-level converters, these two sets of charging voltages neither exchange in the next cycle nor converge. Therefore, when timing mismatches occur, these two sets of voltages can diverge and cause voltage imbalance in flying capacitors as well as fluctuations in the inductor current. The same characteristic is present in all other odd-level members (N is even) of the FCML converters, which becomes a challenge in fully utilizing the benefits of the FCML architecture.

C. Balancing Performance of Other Conventional Hybrid Converters With Vout < Vin

The results using the voltage-charge relationship and its corollary so far align with the results found in [8] and [10] for the imbalance performance of odd- and even-level FCML converters, but the analysis provides a more intuitive approach to understanding the imbalance mechanism in other hybrid converters. The key is in the number of inductor current charging phases in a switching cycle.

Converters having inductors with an odd number of charging intervals in a switching period, such as even-level FCML converters [1], six-phase six-level dual inductor hybrid converters [11], or series capacitor buck converter [12], have naturally balanced operations. The work in [13] demonstrated a hybrid converter with seven (odd) SC levels and one charging interval for each inductor, exhibiting no capacitor voltage imbalance.

As another example, the hybrid converter in [11] provides 1/6 division (even level) to the switching node voltages with each inductor having three charging intervals in each fundamental switching period, also exhibiting naturally balanced operations.

On the contrary, an even number of inductor charging phases cause odd-level FCML converter operation to be highly susceptible to small timing mismatches and imbalanced capacitor voltages. All the traditional odd-level FCML converters, including three-level buck converter, fall into this category. Two-level series capacitor buck converter [12] with a partially coupled
inductor also has an even number of inductor charging phases if modeled with a transformer and an inductor \[14\], and hence, it is also susceptible to voltage imbalance. Note that, some other factors, for instance, parasitic resistance and/or hard-charging operation between flying capacitors in higher level hybrid Dickson converters \[15\] or four-phase four-level dual inductor hybrid converters \[16\], can inadvertently desensitize and minimize imbalance issues at the cost of degraded efficiency.

### IV. Multiphase Symmetric Converter Architecture for Voltage Balancing

Inspired from the analysis above, we propose a new symmetric architecture, which can provide natural balanced operation even with an even number of inductor charging intervals, particularly applicable to balance odd-level FCML converter operations. Fig. 3 shows a symmetric three-level converter that has two symmetric SC halves tied to a common switching node with one inductor. This converter is operated with four 90°-phase-shifted pulsewidth modulation (PWM) signals, A, B, C, and D, and derived signals \( (C \rightarrow B \rightarrow D) \), \( (A \rightarrow B \rightarrow D) \), \( (D \rightarrow A \rightarrow C) \), and \( (B \rightarrow A \rightarrow C) \). This operation also ensures that there is no charge sharing between the two SC halves.

Fig. 4(a) and (b) shows the switching node voltages of a conventional three-level buck converter and a symmetric three-level buck converter, respectively. In the conventional three-level buck converter [see Fig. 1(b)], alternate switching node voltages are generated in the same way in every cycle. Therefore, \( V_{Sx} \) has two levels, \( V_{Sm} - V_{C} \) and \( V_{C} \), that do not naturally converge, as proved by (1) and (2). On the contrary, for the symmetric three-level buck converter (see Fig. 3), the interleaved operation forces \( V_{Sm} = V_{C} \) and \( V_{C1} \) \( (V_{Sm} - V_{C2} \) and \( V_{C2} \)) to converge as they are the alternate switching node voltages. As the result, the flying capacitors have half of the input voltage, \( V_{C1} = V_{C2} = V_{in}/2 \), ensuring an inherently balanced operation. Other than generating the right PWM signals, there is no separate control required to tackle voltage imbalance. Moreover, the inductor in this converter operates with \( 4 \times F_{S} \), where \( F_{S} \) is the fundamental switching frequency of the converter, whereas a traditional three-level buck converter’s inductor has twice the fundamental frequency. This enables the choice of a much smaller inductor. Similar symmetric SC structures can be applied to higher odd-level FCML converters to solve a similar voltage imbalance problem.

### V. Experimental Verification

To verify the voltage–charge relationship and its analytical results above, three-level and four-level buck converters have been implemented to represent the odd- and even-level members of FCML converters that have an even and odd number of inductor charging intervals shown in Fig. 1(b) and (c), respectively. A symmetric three-level buck converter has also been built to verify the proposed inherent balancing. All these three converter prototypes have been built on the printed circuit board, shown in Fig. 5, using the same active and passive components and have the same input voltage of 48 V. Reconfigurations for different converters in experiments only require different PWM control signals for different active devices. No duty cycle adjustment has been done for any of the converters for the demonstration of good or poor mismatch.

The inductor current and flying capacitor voltage waveforms of these three converters are shown in Fig. 6. In Fig. 6(a), the three-level buck converter exhibits a poor balancing performance, particularly visible in its inductor current. In fact, its balancing problem is also corroborated by its median capacitor voltage, shown in Fig. 7(a), which deviates from the ideal value of 24 V and quickly deteriorates with higher currents. Fig. 6(b)
and (c) shows the waveforms of the four-level and symmetric three-level buck converters, respectively, proving their balanced operations with no apparent visual fluctuation in the inductor currents. Their median capacitor voltages in Fig. 7(b) and (c) also reveal better-balanced operations with $\sim 10 \times$ smaller deviation from the ideal values and up to $\sim 10 \times$ less variation across the load range.

VI. Conclusion

A fundamental voltage–charge relationship was devised in this letter to provide a direct intuitive analysis of flying capacitor imbalance in hybrid converters with $V_{\text{out}} < \frac{V_{\text{in}}}{N}$. The analysis in this letter shows that the reason for different balancing performances comes from the number of inductor charging intervals, even or odd. This approach simplifies identifying balanced or imbalanced characteristics in traditional hybrid converters to only counting the number of inductor charging intervals within a fundamental switching period. Experimental results for the verification of the analysis were achieved with three- and four-level FCML converters. A new symmetric architecture was also proposed, implemented, and verified for a three-level buck converter (representing traditional odd-level FCML converters) to show that hybrid converters with an even number of inductor charging intervals can be made naturally balanced with appropriate architecture and operation. The analysis and the method for identifying imbalanced converters and the proposed symmetric architecture to achieve naturally balanced operations in odd-level FCML converters can be extended to other hybrid converters.

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