AUSN: Approximately Uniform Quantization by Adaptively Superimposing Non-uniform Distribution for Deep Neural Networks

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Abstract

Quantization is essential to simplify DNN inference in edge applications. Existing uniform and non-uniform quantization methods, however, exhibit an inherent conflict between the \textit{representing range} and \textit{representing resolution}, and thereby result in either underutilized bit-width or significant accuracy drop. Moreover, these methods encounter three drawbacks: i) the absence of a quantitative metric for in-depth analysis of the source of the quantization errors; ii) the limited focus on the image classification tasks based on CNNs; iii) the unawareness of the real hardware and energy consumption reduced by lowering the bit-width. In this paper, we first define two quantitative metrics, i.e., the \textit{Clipping Error} and \textit{rounding error}, to analyze the quantization error distribution. We observe that the boundary- and rounding- errors vary significantly across layers, models and tasks. Consequently, we propose a novel quantization method to quantize the weight and activation. The key idea is to \textit{Approximate the Uniform quantization by Adaptively Superposing} multiple Non-uniform quantized values, namely AUSN. AUSN is consist of a decoder-free coding scheme that efficiently exploits the bit-width to its extreme, a superposition quantization algorithm that can adapt the coding scheme to different DNN layers, models and tasks without extra hardware design effort, and a rounding scheme that can eliminate the well-known bit-width overflow and re-quantization issues. Theoretical analysis (see Appendix A) and accuracy evaluation on various DNN models of different tasks show the effectiveness and generalization of AUSN. The synthesis (see Appendix B) results on FPGA show $2 \times$ to $4 \times$ reduction of the energy consumption, and $2 \times$ to $4 \times$ reduction of the hardware resource.

1 Introduction

Deploying DNN on edge devices, such as Internet-of-Things devices or mobile phones, is challenging on account of the limited computing and storage resources and energy budge provided by these edge devices. For instance, it takes 16 seconds on a mobile to complete an image recognition using VGG16 \textsuperscript{25}, which is intolerable for most applications \textsuperscript{17}. Therefore, it is essential to compress the DNN for lower storage requirements and simpler arithmetic operations.

Among various compression techniques, quantization maps the weight values distributed in the infinite space of real numbers to the finite space of discrete numbers. Existing quantization methods,
however, mainly encounter several issues. Uniform quantization, such as INT8 [11], uses an affine function to map real value weights to uniformly distributed integers. This method results in a constant distance between the two adjacent quantized numbers, which denoted as Representing Resolution. The representing resolution becomes coarse as the bit-width decreases, which degrades the model accuracy. Non-uniform quantization, such as power-of-two [34], maps the weight values to exponential space. Non-uniform quantization has a extremely large Representing Range of real number with low bit-width exponents. However, both of them can not balance the relationship between Representing Resolution and Representing Range using a low bit-width. For example, the Representing Resolution of non-uniform distribution is too coarse when the exponent number is large and results in a significant quantization error.

Then, we find that some low bit-width quantization methods have poor generality. They cannot apply to the tasks like object detection and sequential network. For example, LSQ [6] only quantizes the weights representing important image features in the convolution layer. Thus, this method only works for CNN based classification tasks.

Most quantization methods presume that lower bit-width can achieve higher speed up or smaller hardware consumption. The introduced decoder, however, may cause significant hardware and energy overhead. Various accelerator architectures may need different quantization bit-width. For instance, Digital-Signal-Processor (DSP) and CPU with AVX prefer 4-bit and 8-bit quantization because the fundamental Multiply-and-accumulate (MAC) can process 4-bit data. It is desired to build a relationship between the quantization bit-width and the real hardware/energy consumption. Such relationship can guide an efficient quantization given a specific accelerator architecture.

In this work, First, AUSN, what we prose is not simply an algorithm, but a framework, including algorithm, coding, rounding, adaptively adjusting scheme. Second, we follow the principle of minimum accuracy drop and extremely small bit-width, to further salvage redundant bit-width to gain more quantization choices. Contributions of this paper are as follows:

1) We first combines these two quantization methods and proposed a coding scheme without the decoder. The bit-width is divided into two parts, which are the symbol and data. The data part can be further divided into “basic part”, and “subdivision part” for the superposition, which determine the Representing Range and Representing Resolution, respectively. Then, we use the superposition of multiple numbers non-uniformly quantized with extremely small bit-width, to represent the weights and activations.

2) We explore in-depth reasons for the quantization error in existing quantization methods: Clipping Error and rounding errors. According to these errors, we propose an adaptively adjusting scheme to reallocate the bit-width according to the weight distribution, reducing the quantization error.

3) We design the rounding scheme to solve the problems about the extra computation effort and hardware overhead caused by overflow of bit-width and re-quantization.

4) We verify the quantized CNNs, sequential networks, and Yolov3-tiny by AUSN on various datasets without retraining and achieve excellent results that exceed state-of-the-art accuracy, and we prove the savings brought by AUSN in hardware resources and energy consumption on FPGA (see Appendix B).

5) We measure the effect of quantization on the model through information loss from the information theory. We also discuss the tradeoff between quantization methods and performance of hardware, which can guide the design of accelerator (see Appendix A).

2 Background

2.1 Uniform quantization

Uniform quantization defines a Representing Range $[\text{min}, \text{max}]$ and quantize weights in the range by first applying an affine function on them and then rounding to the closest integer. For example, all the floating-point weights are quantized to an integer in $[0, 255]$ in INT8 quantization [11].

If the original weights of the DNN exceed the Representing Range, they will be quantized to the boundary values; if these quantized weights are of significant importance, the DNN model may suffer from substantial accuracy loss. Uniform quantization [11, 19] is widely used both in academia and
2.2 Non-uniform quantization

The non-uniform quantization methods [31, 18], similar to clustering, aims at finding some “centers” (i.e., the average value) that can represent the majority of the weight values in the original weight distribution. Therefore, these quantization methods need to store these “centers”, and the quantized number stores the index of “centers” (such as Deep Compression [9]), which causes an obvious resource cost.

Power-of-two quantization [13, 18] quantizes weights to the form of exponents (of power-of-two). This quantized number symbolizes the exponent, i.e., a 3-bit quantized value “111” means that the exponent is 7 and the original value is $2^7 = 128$. It has good Representing Range since the range of quantized weights grows exponentially as the quantization bit-width increases. Besides, the power-of-two scheme is hardware-friendly: the multiplication operation can convert to a shift operation. For example, $\times 4$ can be substituted by shifting the bit sequence two bits to the left. Such conversion is of great significance for the DNN hardware accelerator implemented in ASIC or FPGA [5], because a tremendous amount of power- and resource-consuming DSPs in the multiplier can be substituted by the simple-and-effective Look-Up Tables (LUTs). Take Xilinx Artix-7 as an example, this FPGA contains 53, 200 LUTs and 220 DSP Slices, and the LUT resources are hundreds of times of the DSP. LUTs are a promising alternative to the implementation of multiplication [5]. Such conversion can typically bring up to 50% resource reductions on Xilinx FPGAs [7].

3 Key idea of AUSN quantization

How close the weights in a quantized model can approach its original value inherently determines its quantization error. We define two metrics to evaluate the quantization error.

- **Rounding Error**: The error caused by rounding a weight to the nearest quantized value.
- **Clipping Error**: The error caused by clipping weight out of Representing Range to extremum value.

Uniform quantization pursues finer Representing Resolution result in the larger Clipping Error with the limited bit-width. The finer-grain Representing Resolution is, the more narrow the Representing Range will be, and verse visa. Thus, the accuracy of the DNN model inevitably decreases as the bit-width reduces. As shown in Fig. 1(a), the values quantized to 2bit by the uniform quantization

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2https://china.xilinx.com/support/documentation/data_sheets/ds190-Zynq-7000-Overview.pdf

We divide the bit-width into three parts, which are “sign”, “basic part”, and “subdivision part”. In Fig. 2(a), taking 6bit as an example, the bit-width of general quantization consists of one sign bit and five data bits, while bitwidth of power-of-two quantization is composed of two sign bits and four data. AUSN separates the original five-bit data into the three-bit “basic” part and two-bit “subdivision” part. By sharing the same sign bit of the value, the superposition of the “basic” part and “subdivision” part
Algorithm 1 The procedure for AUSN quantization with Superposition

**Input:** Weight \( w \), maximum number of superposition \( n \), power basis for each superposition \( B_i \)

**Output:** The quantized number of \( w \), \( w_q \)

1: Let \( rem \leftarrow w \), current superposition number \( tier \leftarrow 0 \)
2: while \( rem > 0 \) and \( tier \leq n \) do
3: \( w_q[tier] = \arg\max_p B_{tier}[p] \leq rem \)
4: \( rem = rem/w_q[tier] - 1 \)
5: \( tier += 1 \)
6: end while
7: return \( w_q = \text{Join}_{0 \leq i \leq n} w_q[i] \)

can save 1 bit. Given the total bit-width, the proposed AUSN coding scheme allocates the bit-width to the “basic” and “subdivision” part to ensure a good trade-off between resolution and the range of weight distribution according to the later adaptive adjustment.

![Algorithm 1 diagram](image)

**Figure 3:** The execution process of AUSN Quantizer

### 4.2 Quantization scheme with superposition

*Note that the value stored in quantized bits is not the quantized number, but the power.* If \( B_{\text{basic}} \) bits are used to indicate the basic part, we have an intuitive power basis \( \text{Pow}_{\text{ori}} = \{0, 2^{-1}, \ldots, 2^{-(2^{B_{\text{basic}}}-1)}\} \), whose powers are all negative. Thus, we can save them as unsigned numbers and save one “sign” bit. In practice, however, the range of \( \text{Pow}_{\text{ori}} \) may mismatch with that of \( W_j \). Thus, we introduce a scaling operation called “PreConvert” to make the *Representing Range* of the quantized model closer to the weight distribution of original model, and reduce the *Clipping Error*. Since the values stored in bit-width are the powers, the scaling operation on the original values is converted to the shift operation on the power.

The specific process of AUSN quantization is preformed as follows:

First, we calculate the power indicating the largest weight of the layer \( W_j \):

\[
\text{power}_j = \lceil \log_2 \max |W_j| \rceil \tag{1}
\]

Then, we perform the “PreConvert” operation on \( \text{Pow}_{\text{ori}} \):

\[
\text{Pow}_{\text{pre}} = \text{Pow}_{\text{ori}} \ast 2^{\text{power}_j} \tag{2}
\]

We denote the power of basic part after “PreConvert” operation \( \text{Pow}_{\text{pre}} \), as \( B_0 \), and it satisfies Equation (3), which means we use \( \text{Pow}_{\text{pre}} \) to approximate the range of \( W_j \).

\[
\max(\text{Pow}_{\text{pre}}) \leq \max |W_j| \leq 2 \max(\text{Pow}_{\text{pre}}) \tag{3}
\]

Furthermore, for the \( n \)-th superposition that have \( B_1, B_2, \ldots, B_n \) bits respectively, we also have the corresponding superposition power \( B_i = \{0, 2^{-1}, \ldots, 2^{-(2^{B_i}-1)}\} \). Then, we use Algorithm 1 to derive the superposition of each quantized number \( w_q \). In the procedure of AUSN quantization with superposition defined (as shown in Fig. 2(b)), a proximate representation of \( w \) can be expressed as

\[
w = \sum_{i=0}^{n} \prod_{j=0}^{1} 2^{-w_q[i]} \tag{4}
\]

Our AUSN algorithm can naturally round the weight \( w \) to the quantized number and decide whether to superpose. We can also apply Algorithm 1 to the activations.
4.3 Adaptively adjusting the coding scheme

Our AUSN algorithm can naturally round the weight \( w \) to the quantized number and decide whether to superpose, and also adaptively adjust internal allocation of bit-width to the base part and the subdivision part according to the **Clipping Error** and **Rounding Error**. For example, AUSN quantization with 5bit, the weight distribution of CONV1 layer, the 4bit for the basic part and 1bit for the subdivision part, while 3bit for the basic part and 2bit for the subdivision part in CONV2 layer. Suppose that the initial distribution of the weights in a layer is normal. Without losing universality, we suppose that the weight follows standard normal distribution \( \mathcal{N}(0, 1) \) and is clipped at \((-\mathcal{L}, \mathcal{L})\).

Since quantization distribution is usually evenly distributed about 0, we only consider the positive part. Suppose that AUSN quantization has a **Representing Range** \([0, R]\) and a set of quantized numbers \( \mathcal{P} \), we can use the following equation to present the **Clipping Error** \( \mathcal{E}_b \) and **Rounding Error** \( \mathcal{E}_r \):

\[
\mathcal{E}_b = \int_{R}^{\mathcal{L}} w \cdot |w - R| \cdot \mathcal{N}(w; 0, 1) \, dw \quad \mathcal{E}_r = \int_{0}^{R} w \cdot \min_{p \in \mathcal{P}} |p - w| \cdot \mathcal{N}(w; 0, 1) \, dw \quad (5)
\]

First, AUSN initializes the coding scheme according to the given bit-width and quantizes the weights. Then, the **Clipping Error** \( \mathcal{E}_b \) and **Rounding Error** \( \mathcal{E}_r \) between the quantized weights and original weights is calculated according to equation (5). Last, based on \( \mathcal{E}_r \) and \( \mathcal{E}_b \), AUSN adjusts the boundary \( \mathcal{R} \) of **Representing Range** and the set of quantized value \( \mathcal{P} \) (that is, the allocation of bit-width). The above process is iterated until an optimal allocation of bit-width is found.

4.4 AUSN rounding scheme

Although AUSN quantization has effectively solved the problem of the power-of-two quantization in the reduction of accuracy, there still exists two critical issues for almost quantization methods:

1. **Overflow of Bit-width**: The output resulted from the convolution operation (Multiply and Accumulate) occupies a larger bit-width to maintain the precision than that of the quantized number. For example, the convolution operation of two \( 2 \times 2 \) matrix consisting of all 8-bit numbers first result in four 16-bit dot-products and then accumulate to the 32-bit sum.

2. **Overhead of Re-quantization**: In deep neural networks, the output of the previous layer is the input of the next layer. The outputs have a high likelihood of exceeding the range of the quantized numbers for the input layer. Thus, existing methods have to re-quantize the output values — such re-quantization results in significant cost of computation and resource.

We formulate the above problems as follows. Suppose the next layer only accepts an activation value with a double superposition due to the bit-width limit, but in the process of multiplication with AUSN, the number of superposition will increase, e.g., \((a + b) \times (c + d) = A + B + C + D\). Thus, we have to eliminate some power-of-two terms (one term in this example) and round up/down the activation value with a minimized rounding error. Consequently, after the multiplication operation, we can substitute the accumulation operation with rounding scheme, which eliminates the overflow and re-quantization issue.

The basic principle of rounding operation is simple enough and to minimize the rounding error. Given the data in the form of a polynomial of power-of-two, we need to determine the power after rounding. **Principle**: \(2^n \leq data \leq 2^{n+1}, m \in \mathbb{N},\) so that **Quant** (data) \(\approx 2^m\) or **Quant** (data) \(\approx 2^{m+1}\).

The rounding scheme can be categorized into the following four scenarios:

**Scenario 1**: \( m+n+1 \geq B_{sub}+2 \), wherein \( B_{sub} \) is the bit-width of the subdivision part indicating the number of superposition.

**Scenario 2**: When the condition \( m = n \) is satisfied, it’s obvious that \( 2^n + 2^m \approx 2^{m+1} \).

**Scenario 3**: If \( m > n + B_{sub} \), then \( 2^n + 2^m \approx 2^n \).

**Scenario 4**: If \( m = n + B_{sub} \), then \( 2^n + 2^m \approx 2^n \) or \( 2^n + 2^m \approx 2^{m+1} \).

Based on the above scenarios, we round the data using the following algorithms.

**Step 1**: Find the maximum terms in data that can apply Scenario 1.

**Step 2**: Find pair of terms that can apply Scenario 2.
Step 3: Apply Scenario 3 if the condition \( \text{num}(\text{rest}) \geq B_{sub} + 2 \) is met.

Step 4: If Equation (6) work, carry out the Scenario 4.

\[
\begin{cases}
\text{num}(\text{rest}) = B_{sub} + 1 \\
B_{sub} < \text{bit} - \text{width}(\text{min}(\text{rest}))
\end{cases}
\]  

(6)

Following the above steps, we can eliminate the number of power-of-two to satisfy \( B_{sub} \) and minimize the rounding error. Take the data 412 = \( 2^2 + 2^3 + 2^4 + 2^6 + 2^8 \) as example, assuming \( B_{sub} = 1 \), that is the quantized number is single superposition of power-of-two. Step1: merge the \( 2^5 = 2^2 + 2^3 + 2^4 \) and get the \( 2^5 + 2^6 + 2^8 \); Step 2: merge the \( 2^7 = 2^5 + 2^6 \) and get the \( 2^5 + 2^7 + 2^8 \); Then, the condition of step 3 is not met, and thus step 4 is performed: merge the \( 2^7 = 2^5 + 2^7 \) and get the \( 2^7 + 2^8 \); Finally, we find the result 384 = \( 2^7 + 2^8 \) satisfy the requirement of quantization.

5 Experiments

To evaluate the performance of our algorithm, We quantize several models and verify the accuracy of the models on the different datasets. By using Cifar10 [15] and ImageNet [4], we compare AUSN with several state-of-the-art quantization methods on CNN. We implement the AUSN quantization using the CNN model structures and pre-trained models in Pytorch library.

In addition, we verified the sequential network and the network used in target detection task through the Google Speech Commands dataset, the VoxCeleb dataset and COCO datasets. We compared our results with full-precision baselines models to demonstrate the broad applicability of our approach.

Remarkably, we quantize the pre-trained models without fine-tuning or retraining.

5.1 Result of quantized networks on Cifar10

From the data in table 1, we can see that both the self-adapting shifting and the better resolution brought by subdivision part enhanced our result. For the 2-bit result, both schemes quantize weights into power-of-twos, but our AUSN find a better covering range and thus get a better result. For the result of 3, 4 and 5-bit quantization, our AUSN method retained the basic part as 3 bits and set the subdivision part as 0, 1 and 2 bits, respectively. Compared with the INQ result, we can find that our accuracy progress for each bit added is much larger than that of INQ counterpart. This means that when the representation range is guaranteed (presented by the bit-width for the basic part in AUSN or the whole bit-width in INQ), it is the resolution (presented by the bit-width for the subdivision part in AUSN) that helps the accuracy to grow.

Especially, we quantized the pruned model of ResNet-18 to show the harmonious cooperation between the AUSN and the pruning method.

Table 1: Accuracy on Cifar10 for typical quantized networks comparison by different bit-width. The last one is the pruned ResNet50 model at 50% sparsity. Compared quantization is INQ.

| Model      | Baseline 32bit | AUSN quantization (Ours) | power-of-two INQ [34] |
|------------|---------------|--------------------------|------------------------|
|            | 5bit/Top-1(%) | 4bit/Top-1(%) | 3bit/Top-1(%) | 2bit/Top-1(%) | 5bit/Top-1(%) | 4bit/Top-1(%) | 3bit/Top-1(%) | 2bit/Top-1(%) |
| AlexNet    | 85.13         | 85.21          | 85.00         | 84.80         | 83.21         | 81.90         | 81.89         | 80.29         | 80.27         |
| GoogleNet  | 90.89         | 90.85         | 90.01         | 89.37         | 89.11         | 88.28         | 88.28         | 88.27         | 88.21         |
| VGG16      | 93.92         | 93.95         | 93.58         | 93.68         | 92.75         | 91.88         | 91.84         | 91.27         | 91.26         |
| ResNet18   | 92.22         | 92.25         | 91.83         | 91.80         | 91.46         | 90.47         | 90.31         | 90.14         | 90.10         |
| ResNet18(pruned) | 94.17     | 94.11         | 94.09         | 93.52         | 92.65         | 92.87         | 92.85         | 92.83         | 88.15         |

5.2 Result of quantized networks on ImageNet

In the experiments on ImageNet, we choose the most widely used models ResNet18 and ResNet50 and compare our result with other quantization schemes. Table 2 shows that the Top-1 accuracy loss in our 5-bit AUSN is less than 0.1%, far better than other schemes.

Find out more information on our methodology here: [https://github.com/pytorch/vision/tree/master/torchvision/models](https://github.com/pytorch/vision/tree/master/torchvision/models)
Table 3: The accuracy comparison of DNNs uses existing methods on the datasets of image recognition, target detection, and speech recognition tasks. The quantized models by AUSN quantization without fine-tuned and any augmentation tricks.

| ImageNet Dataset | Method | bit-width | Top-1(%) | Drop in Top-1(%) | Method | bit-width | Top-1(%) | Drop in Top-1(%) |
|------------------|--------|-----------|----------|------------------|--------|-----------|----------|------------------|
|                  | ResNet50 (baseline: 76.13%) | 4bit | 70.20 | -5.93 | BWN | 24 | 2bit | 60.8 | -8.5 |
|                  | ResNet18 (baseline: 69.76%) | 5bit | 74.81 | -1.59 | Dual | 37 | 4bit | 66.63 | -3.13 |
|                  | Focused compression  | 5bit | 74.86 | -1.54 | LAPQ | 23 | 4bit | 62.6 | -7.16 |
|                  | ADMM Quantization  | 6bit | 75.93 | -0.2 | Focused compression  | 5bit | 68.36 | -1.40 |
|                  | SYMM  | 6bit | 72.58 | -3.55 | UNIQ | 1 | 5bit | 68.00 | -1.76 |
|                  | Biscaled-FxP  | 6bit | 70.46 | -5.67 | DFQ | 37 | 6bit | 66.3 | -3.4 |
|                  | V-Q | 7bit | 75.89 | -0.24 | INT8 | 11 | 8bit | 67.3 | -2.4 |
|                  | Focused compression  | 5bit | 74.86 | -1.5 | RQ | 18 | 6bit | 68.6 | -1.16 |
|                  | Ours  | 4bit | 75.37 | -0.76 | Ours | 4bit | 68.84 | -0.92 |
|                  | Ours  | 5bit | 76.09 | -0.94 | Ours | 5bit | 69.67 | -0.09 |

| Speech Command Dataset | Method | bit-width | Top-1(%) | Drop in Top-1(%) | Method | bit-width | Top-1(%) | Drop in Top-1(%) |
|------------------------|--------|-----------|----------|------------------|--------|-----------|----------|------------------|
|                        | GRU (Network cfg†: S = 40, N = 154) | 32bit | 93.62 | - | GRU (Network cfg†: S = 20, N = 400) | 32bit | 94.62 | - |
|                        | baseline | 32bit | 93.15 | -0.47 | Ours | 4bit | 94.34 | -0.28 |
|                        | Ours | 5bit | 93.47 | -0.15 | Ours | 5bit | 94.57 | -0.08 |

| Speech Command Dataset | Method | bit-width | Top-1(%) | Drop in Top-1(%) | Method | bit-width | mAP | Drop in Acc. |
|------------------------|--------|-----------|----------|------------------|--------|-----------|-----|-------------|
|                        | CRNN_A † | 32bit | 93.50 | - | CRNN_C † | 32bit | 94.56 | - |
|                        | baseline | 32bit | 93.17 | -0.33 | Ours | 4bit | 94.28 | -0.28 |
|                        | Ours | 5bit | 93.38 | -0.12 | Ours | 5bit | 94.48 | -0.08 |

| VoxCeleb Dataset | Method | bit-width | Top-1(%) | Drop in Top-1(%) | Method | bit-width | mAP | Drop in Acc. |
|------------------|--------|-----------|----------|------------------|--------|-----------|-----|-------------|
|                  | TDNN | 32bit | 80.38 | - | YOLOv3–tiny | 32bit | 33.1 | - |
|                  | baseline | 32bit | 79.98 | -0.40 | Ours | 4bit | 31.6 | -1.5 |
|                  | Ours | 5bit | 80.25 | -0.13 | Ours | 5bit | 32.2 | -0.9 |

† S: Frame Stride, N: Cells of GRU
‡ The Network cfg of CRNN_A is: C(48,10,4,2,2)-N(60)-N(60)-F(84); the Network cfg of CRNN_C is: C(100,10,4,2,1)-N(136)-N(136)-F(188), where C: Shape of Convolutional layer, N: Cells of GRU, F: Cells of fully connected layer

Meanwhile, we quantize the weights of pre-trained models without fine-tuning and got the results in Table 3, which means that the time of quantization has significantly been saved. Also, in Table 2, we quantize both weights and activations to optimize the inference process. According to the advantages mentioned above, our AUSN method reached state-of-the-art result in existing quantization schemes.

5.3 Result of quantizing sequential models and Yolo

We explore the effect of the AUSN quantization on the sequential network such as GRU, CRNN [32], and TDNN [26] through the Google Speech Commands dataset and the VoxCeleb dataset, and the effect of the AUSN quantization on the target detection task such as YOLOv3-tiny through the COCO datasets, as shown in Table 3. There is few decrease in accuracy (i.e. mAP for Yolov3-tiny in COCO and Top-1 accuracy for sequential models) for quantizing weights from 32bit to 4bit or 5bit.

Table 2: ResNet18 on ImageNet. Top-1 accuracy loss (%) with quantized weights and activations by various quantization method, including SR+DR [8], INT [11], RQ ST [16], PACT [2], QIL [14].

| Method | Bit-width | SR+DR INT RQ ST PACT QIL | Ours |
|--------|-----------|--------------------------|------|
| Acc. loss | 5/5 | 5/5 5/5 5/5 5/5 5/5 | -10.5 -2.5 -1.6 -0.3 -0.8 -0.3 |
| Bit-width | 5/5 | 5/5 5/5 5/5 5/5 | 5/5 | 5/5 5/5 5/5 5/5 5/5 |
### Table 4: The comparison of FPGA resources and energy consumption for 64 x 64 MAC array

| Resources | Multiplier & Accumulator | Shifter & Adder | Performance need decoder | Ours |  |
|-----------|--------------------------|----------------|--------------------------|------|---|
| LUT       | 212388 187262 181248 225280 212942 203712 133120 112071 108544 | 8/8 8/5 8/4 8/8 8/5 8/4 8/8 8/5 8/4 | 2.0× |
| FF        | 192293 143142 108729 86317 512731 45729 54313 45127 44032 | 4.4× |
| Energy Consumption | 4.21W 3.75W 3.67W 4.51W 4.26W 4.07W 2.65W 2.24W 2.17W | 1.9× |

1 A/B refers to A-bit input multiplied by B-bit weights

### 5.4 Result of quantized networks deployed on FPGA

AUSN doesn’t need a decoder. Decoder is necessary only when the control information is encoded into bit-word. AUSN directly “multiply” two exponents composing the weight with the input in parallel by shift operations, whose results is added up (superposition) to the output. AUSN is not only as easy to compute as uniform quantization (like INT8), but also hardware friendly because the expensive multiplication operation is replaced by the simple bit shift and add operations. Compared with the traditional 8-bit multiply-accumulator, the shifter can be realized only by logic units such as LUTs. As shown in Table 4, we found that the quantized model by AUSN not only DSPs are not required, but also saves the LUTs 2.0×, FFs 4.4× and power 1.9× by using the Xilinx Vivado HLS suite, which dramatically reduces the hardware cost (The evaluation platform is Xilinx ZCU104).

### 6 Conclusion

In this paper, we introduced a novel quantization method called AUSN, which combines the advantages of broad representing range of power-of-two quantization and the constant representing resolution of the uniform quantization. This method can quantize both the activation and weight of a pre-trained model to low bit-width (less than 8bit) without accuracy loss. AUSN shows an excellent generality because it can adaptively adjust the number of superposition and the coding scheme given a fixed bit-width. We further design a rounding scheme in AUSN to eliminate the overhead of re-quantization. The thorough experiments show the superiority of AUSN quantization against state-of-the-art methods. Compared with other quantization methods, AUSN quantize the pre-trained model without retraining. Notably, the AUSN quantization is hardware-friendly. The synthesis (see Appendix B for detail) results on FPGA proved that AUSN can effectively reduce the resources and energy consumption. We measure the effectiveness of quantization methods by information loss from the theoretical perspective and analysis of the relationship between the quantization methods and performance of hardware (as in Appendix A).
Broader Impact

The high accuracy of DNNs is achieved by consuming a lot of computing and storage resources, which significantly hinders the application of DNNs in edge devices. Quantization is proposed and widely used for storage and computation reduction. As for AUSN quantization, results in fewer bits representing these operands and corresponding operations by lowering the precision demands of operations and operand, which reduces the cost of datapath and memory. Furthermore, it can also reduce the energy consumption and resources of hardware and expand the accelerator design space of many terminal devices with limited hardware resources. It is worth noting that AUSN quantization is a general quantization method, which can be used in many tasks, such as image recognition, speech recognition, target detection.

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A Theoretical analysis

We explore the choice of quantization in the context of information theory, which enables us to reinterpret quantization as the Minimum Description Length (MDL) problem [10, 27]. Both MDL and quantization can be regarded as a search problem, aiming at finding out the optimal method to compress data with balancing the accuracy and the complexity (including bit width, quantization method, etc.) of the model. We define the loss function to measure the loss of information between the distribution of original weights, $M$, and the distribution of quantized weights, $M_q$, mainly including the error and the complexity. Specifically:

$$\mathcal{L}(M, M_q) = \log \frac{p(D|M)}{p(D|M_q)} + \text{KL}(M, M_q)$$

(7)

where $D$ denotes the dataset that $M$ and $M_q$ is trained on. $-\log \frac{p(D|M)}{p(D|M_q)}$ indicates the error caused by the misfit between model $M$ and quantized model $M_q$ trained on the dataset $D$. The dataset $D$ consists of inputs $X$ and expected output $Y$, $p(D|M)$ can be further expressed as $p(Y|X, M)$, which means the probability of achieving the correct output $Y$ given the input $X$ and model $M$. KL$(M, M_q)$ indicates the complexity of the quantization methods.

According to the information theory, KL$(P, Q)$ is used to measure the average number of extra bits required by $Q$ encoding $P$, i.e., the distance between them. We then consider $Q$ as an approximation of the distribution of $P$. Thus, KL$(M, M_q)$ represents KL divergence, which measures the similarity between the distributions of $M$ and $M_q$. For KL$(M, M_q)$, firstly we divide the original distribution of $M$ according to the set of points of the quantized distribution $\hat{M}$, and then calculate the probability of differences between $M$ and $\hat{M}$:

$$\text{KL}(M, \hat{M}) = \sum M(X) \log \frac{M(X)}{\hat{M}(Y)}$$

s.t. $M(X) = \frac{\text{sum}_x(y_i)}{\sum_{y_i} \text{sum}_x(s)} \text{sum}_x(y_i) = \int_{y_i-\frac{1}{2}}^{y_i+\frac{1}{2}} \text{distri}_x(s)dx$

(8)

where $\text{distri}_x$ is the distribution of weight in real number field. $\text{sum}_x(y)$ is the approximate count of weights according to $\text{distri}_x$ at $y$. $Y$ is the set of quantized numbers.

| Bit-Width | Quant | KL divergence | Accuracy loss | Information loss |
|-----------|-------|---------------|---------------|------------------|
| 5bit      | Ours  | 0.014         | -0.001        | 0.013(1)         |
|           | INQ   | 0.004         | 3.23          | 3.234(4)         |
| 4bit      | Ours  | 0.062         | 0.13          | 0.192(2)         |
|           | INQ   | 0.004         | 3.24          | 3.244(5)         |
| 3bit      | Ours  | 0.261         | 0.15          | 0.411(3)         |
|           | INQ   | 0.004         | 4.84          | 4.844(6)         |

The smaller value of information loss, the less accuracy loss induced by quantization. In Table 5, the figure in brackets is in the ascending order of information loss. The red label is the best quantization effect.

B Efficiency Analysis

B.1 Analysis on the Evolution

Most existing quantization methods focus on reducing the bit-width and improve accuracy. However, these approaches ignore the limitation of hardware. As the bit-width of the quantized model decreases, the reductions of the resource and energy consumption manifest themselves differently in various accelerator architectures and arithmetic logics. Fig. 4 describes the evaluation method of the proposed AUSN quantization. Generally speaking, multiplication is more expensive than addition and shift operations in terms of the complexity of digital circuits, the number of transistors and the power consumption as well. For example, on FPGA, the shift operation implemented with Look Up
Tables (LUTs) is more than $30 \times$ more efficient in energy consumption than the multiplication and accumulation operations conducted with the Digital Signal Processors (DSPs). The DSPs on FPGA are also limited, and the difference between DSP resources and LUT resources is more than two orders of magnitude.

The power-of-two quantization transforms multiplication operation into shift operation, making the quantized network hardware-friendly to balance the cost of hardware resources. For example, the quantized DNN (the power-of-two quantization quantizes the weights, the input is quantized into the fixed-point number) is deployed on the FPGA, and the multiplication operation can be converted to the shift operation of the fixed-point number. Although shift operation can alleviate the shortage of DSP resources to a certain extent, the accumulation operation still depends on DSP and requires additional hardware overhead for the re-quantization. LUT resources may become a new bottleneck because of the bit-width of input. Moreover, due to the significant rounding error caused by the power-of-two quantization, the accuracy will inevitably decrease, so that the power-of-two quantization can not be further applied.

To further reduce the bit-width and computing resources, the weights and activations both are quantized by the power-of-two quantization, which can further convert the shift operation into the addition operation. However, it will lead to a more significant accuracy decrease. However, AUSN quantization can not only reduces the accuracy loss but also is reasonable for LUT resources.

We can quantize weights and activations using proposed AUSN quantization, and transform re-quantization into AUSN rounding. We can eliminate the intermediate value (i.e., partial sums generated in the calculation of convolutional layers) stored on the Block RAMs (BRAMs) for data storage through the logic gate. It can also assure the final accuracy and make full use of LUT resources. In theory, we can even deploy the DNN quantized by AUSN quantization on FPGA without DSP resources or design a reasonable accelerator to realize parallel computing on convolution layer by LUTs and DSPs.

https://china.xilinx.com/support/documentation/sw_manuals/xilinx147/ug440-xilinx-power-estimator.pdf

Figure 4: The evaluation of AUSN quantization.
B.2 Analysis on LUT Resource

The LUT resource consumed by AUSN quantization is far less than that consumed by the shift operation of the fixed-point number as the bit-width of inputs is further reduced. The specific analysis is as follows (take 6bit for both weights and activations as an example).

Figure 5: The consumption of LUT resources.
To make good use of the resources, we implemented addition or shift operation with 6-input LUT (for Modern Xilinx FPGAs, like whole 6 series, 7series). If inputs and weights are quantized to the fixed-point number and power-of-two, respectively, then multiplication of the input and the weight is implemented by the shift operation, the bit-width of the result of the multiplication is 12 bits (6 bits \( \times 6 \) bits \( \rightarrow \) 12 bits).

In contrast, we quantize the inputs and weights by AUSN quantization, which converts the shift operation of the value into addition operation of the power. We divide the addition operation into 3 times, each addition consuming 4 LUTS. Through this, the result only needs 7 bits (6 bits + 6 bits \( \rightarrow \) 7 bits). Fig. 5 describes the consumption of LUT resources.

We can found the number of 6-input LUT consumed by the multiplication operation of 6bits implemented by the shift operation on the value (in Fig. 5(a)) is \( 12 \times 2 = 24 \) LUTs, where the number of 6-input LUT consumed by the addition operation on the power (in Fig. 5(b)) is \( 3 \times 4 = 12 \) LUTs. AUSN quantization consumes less LUT resources than the shift operation of fixed-point numbers. Remarkably, there is almost no accuracy loss of the quantized model by AUSN quantization.

B.3 The analysis on implementation

\[ \text{Computation to Communication Ratio} = \frac{\text{FLOPs per second}}{\text{Memory access per second}} = \frac{\text{total number of operations}}{\text{total amount of external data access}} = \frac{\text{total number of operations}}{4 \times (\text{weight memory} + \text{output memory})} = \frac{\text{time complexity of model}}{\text{space complexity of model}} \]

The RoofLine model is the upper bound of theoretical performance that the model and algorithm can achieve under the limitation of the computing power and bandwidth of the accelerator. In the Fig. 6 the x-axis represents the CCR or operational intensity, which the higher CCR is, the higher the memory efficiency is; the y-axis represents the computing performance of the accelerator; \( R \) is the boundary. The bandwidth of machine limits the left area of \( R \) and the computing power of the machine limits the right. The upper limit of bandwidth and the upper limit of computation is determined by the accelerator, called bandwidth roof and computational roof. The space/optimization space provided by the machine is the area on the right side of the bandwidth roof.

Figure 6: Optimization space provided by hardware.

We refer to the classic performance evaluation model, called the RoofLine model \([29]\), to analyze the quantization methods and the performance gains of the quantized model on the machine. It can be concluded that quantization reduces the accuracy of operations and operands, resulting in fewer bits representing these operands and corresponding operations, which significantly increase the Computation to Communication Ratio (CCR) as defined in Equation (9).
performance can only be the projection on the bandwidth roof or computational roof if it is above the bandwidth roof or computational roof.

As the model is quantized, the CCR becomes larger, and the position of the model moves to the area to the right of $R$, changing from being limited by bandwidth of accelerator to being limited by computing power of accelerator (transfer from point $A$ to point $B$ in the Fig. [6]). Though the bit-width of weights is further reduced, the performance cannot be further improved due to the limitation of computational roof. For FPGA, the computing core is DSPs. The quantized model by the AUSN converts the multiplication operation to shift or even addition operation. These operations can be realized by the LUTs, which is equivalent to adding a computing core to the FPGA, increasing the theoretical calculation peak of FPGA (the computational roof moves up in the Fig. [5]), and providing more design space for further optimization.

Compared with AUSN, the other quantization methods with low bit-width(such as less than 5bit) also can achieve a high compression ratio, it may need to increase the process of decoding. The process of decoding will increase a lot of hardware resources and energy consumption, which is hardware-unfriendly. As shown in Table [4], the 4bit shift operation with indexes requires additional decoders to be deployed on the hardware, resulting in logic resources and power that even exceed the overhead of 8bit multiplication. Therefore, lowering the bit-width does not indicate the increase of actual benefits.