Performance Analysis on Effect of Variation in Oxide Material of Double Gate Tunnel Field Effect Transistor

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Abstract. In this paper structure of Double Gate Tunnel Field Effect Transistor work to increase the efficiency of the device performance of Tunnel Field Effect Transistors making it one of the potential candidates for small scale devices. The essential point of this research work is to consider the performance analysis of the structure. This work is accomplished with the assistance of tool Cogenda TCAD version 1.9.2. The designing of the device, simulation and correlation of results have been gotten on this tool. The section gives the stream of Research Methodology and clarifies the footsteps for Design and Simulation of Double Gate Tunnel Field Effect Transistor.

Index Term: TFET, DG-TFET, DIBL, BTBT, SCE.

1. Introduction

An important area under consideration in semiconductor field, specifically in devices, is the continual scaling down of device measurements. In the past, we came across large vacuum tubes to first MOSFET with a Channel length of 300 μm to transistors with Channel lengths of 14 nm or less. This leads to integration of circuits with billion of transistors on a single VLSI chip. By Scaling the length of a MOSFET i.e. by reducing the Channel length, we can increase the number of transistors which leads to a increased Gate capacitance, increased switching speed of VLSI circuit. Additionally, the voltage scaling that is an essential part of a device likewise causes decrease in the power utilization of the device.

A comparison of SGTFET and DGTFTET is done and a novel design for DGTFTET with significant improvements is proposed. It is also shown that current associated to the device is not confined to Gate-Dielectric surface [1]. A complete survey on TFET with various structures available for its design and also with variation in various parameters was done [2]. The Dual Modulation effects on Surface potential of Channel i.e. Channel is controlled by Gate supply and Drain supply voltage in different operating regimes. [3]. In pseudo-2-D analytical model to analyze the electrostatics of Multiple Gates TFETs, with convenient set of equations to describe and compare SOI, DGTFTET and Cylindrical Nano wire devices simultaneously on the basis of numerical simulations [4]. Two dimensional analytical models were analyzed for Surface potential, Electric Field, ID, Sub threshold Swing and VT. In the proposed model, Dual Material Double Gate TFET with stacked SiO₂/HfO₂ is analyzed. All the simulations are carried out on Silvaco ATLAS TCAD [5]. Ambipolar conduction in tunnel field-effect transistors (TFETs) occurred due to drain-channel tunnelling [6][7].

2. Schematic Structure of Double Gate TFET

Double Gate TFET structure is like that of MOSFET aside from that Source and drain are doped with dopants of opposite polarity and Channel is intrinsic or uniformly doped. Fig.1. shows N-TFET in which drain side is doped with donor type of impurities (n+) , Source side is doped with acceptor type impurities (p+) and Channel is n-type intrinsic region and TFET forms a gate PIN diode in which drain is applied positive with respect to Source and works under reverse biased condition. The Tunnelling occurs between Source and Channel region, so Channel region is to be made of n-type material to further cause the bending of Conduction band in the Channel region than p-type material.
Figure 1. Schematic Structure of Double Gate TFET

Table 1. Device Parameters

| S.NO | PARAMTRES                          | SIZE      |
|------|------------------------------------|-----------|
| 1.   | Channel Length                     | 30nm      |
| 2.   | Oxide Thickness                    | 3nm       |
| 3.   | Body Thickness                      | 10nm      |
| 4.   | Source/Drain Length                | 10nm      |
| 5.   | Work Function of metal contact     | 4.5eV     |
| 6.   | Source Concentration               | $10^{17}$/cm$^3$ |
| 7.   | Drain Concentration                | $5 \times 10^{18}$/cm$^3$ |
| 8.   | Intrinsic Channel Concentration    | 1020/cm$^3$ |
The Table 1 above shows the various specifications associated with the Double Gate TFET. The Tunneling model is used is Non Local BTBT model used extensively for simulation of ON Current i.e. to study the Charge Transfer through the Potential barrier by taking into consideration the Potential profile in the region of Tunneling.

3. Results and Discussion

3.1 Effect of Channel Length on various parameters

In case of MOSFET, when we decrease the Channel length, there are various unusual Short Channel Effects (SCE) that are taken under consideration eg. DIBL, Hot Carrier effects, Saturation Velocity etc. But in case of TFET no SCE are present we reduce the Channel length. So, TFET is the future candidate for Low Power high speed VLSI circuits and Short Channel devices. In the graph shown in Fig.2, depicts that as the Channel length is diminished from 50nm to 10nm, the value of $I_{ON}$ remain same of the order of $10^{-6}$ A and the leakage current is increased i.e the $I_{OFF}$ value increases as we move beyond 20nm to a large extent i.e. of the order of $10^{-9}$ A. In short, there is large unacceptable variation in Subthreshold Swing [8]. In case of 20nm Channel length, if we increase the drain voltage the leakage current increases because of tunneling in drain side. So, the Channel length of the order of 30nm is proposed for better results.

![Figure 2](image-url)

**Figure 2.** $I_{D}-V_{GS}$ Characteristics of DG-TFET for varying Channel Length from 50nm to 10nm

3.2 Effect of Variation in Oxide Material

TFET is a device which is more sensitive to the change in the capacitance i.e. by changing Dielectric Constant of Gate oxide, Gate length and Gate oxide thickness. As we move from low-k material to the high-k material, there is increase in capacitance due to improved coupling between Gate and Tunneling barrier.
Figure 3. Comparative plot of $I_D-V_{GS}$ Characteristics of DG-TFET for Different Oxide Materials (a) Si3N4,(b)SiO2(c)HfO2

Due to increase in capacitance, the drain current i.e. $I_{ON}$ current increase exponentially with decrease in barrier width. But, with this the OFF current or the Ambipolar currents also increases from $10^{-15}$ A for SiO$_2$, $10^{-12}$ A for Si$_3$N$_4$ and for $10^{-7}$ A for HfO$_2$ [6]-[7].

4. Conclusion

The performance and Simulation analysis of Double Gate Tunnel Field Effect Transistor observed. The device structure of Double Gate TFET optimize by varying different parameters. In the Future, various changes can be incorporated in the future work to increase the efficiency of the device. Fin structures, Nanowire Structure and Graphene tubes can be used in device design. Also, Ferroelectric materials can be used for better performance of Tunnel Field Effect Transistors making it one of the potential candidates for ultra small scale devices.
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