A Closed-loop Sleep Modulation System with FPGA-Accelerated Deep Learning

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Abstract—Closed-loop sleep modulation is an emerging research paradigm to treat sleep disorders and enhance sleep benefits. However, two major barriers hinder the widespread application of this research paradigm. First, subjects often need to be wire-connected to rack-mount instrumentation for data acquisition, which negatively affects sleep quality. Second, conventional real-time sleep stage classification algorithms give limited performance. In this work, we conquer these two limitations by developing a sleep modulation system that supports closed-loop operations on the device. Sleep stage classification is performed using a lightweight deep learning (DL) model accelerated by a low-power field-programmable gate array (FPGA) device. The DL model uses a single channel electroencephalogram (EEG) as input. Two convolutional neural networks (CNNs) are used to capture general and detailed features, and a bidirectional long-short-term memory (LSTM) network is used to capture time-variant sequence features. An 8-bit quantization is used to reduce the computational cost without compromising performance. The DL model has been validated using a public sleep database containing 81 subjects, achieving a state-of-the-art classification accuracy of 85.8% and a F1-score of 79%. The developed model has also shown the potential to be generalized to different channels and input data lengths. Closed-loop in-phase auditory stimulation has been demonstrated on the test bench.

I. INTRODUCTION

Sleep plays a critical role in a vast array of physiological and pathophysiological processes, including in neurodegenerative diseases such as Huntington’s and Alzheimer’s disease [1]. New therapies will emerge through an improved understanding of sleep mechanisms. Sleep is composed of an alternation of rapid eye movement (REM) sleep and three non-REM (NREM) sleep stages (i.e., N1-3). Sleep stages can be classified using surface electroencephalogram (EEG). Causal investigations of sleep increasingly rely on closed-loop paradigms in which a real-time sleep stage classifier is used to deliver stage-specific stimulation [2]–[5]. For example, studies have shown that auditory stimulation can be applied in phase with the prominent slow wave activity of NREM to enhance long-term memory [6], [7].

However, closed-loop sleep investigations are only feasible if the sleep stages can be detected accurately in real time and the stimulus signal can be delivered in phase with the sleep oscillation. The system should also minimize adverse effects on the subjects’ sleep process, which excludes the use of rack-mounted instrumentation. These requirements motivate the development of a miniature system that supports closed-loop on-device sleep modulation and can be worn comfortably during sleep.

In this work, we fill this important research gap by developing a closed-loop sleep modulation system that is self-contained and can be miniaturized. Fig. 1 shows the high-level block diagram of the system and its operational principle. The system uses a single-channel EEG as input. Sleep stage classification is performed using a novel lightweight deep learning (DL) model implemented in a low-power field-programmable gate array (FPGA). Auditory stimulation is activated on the basis of the specific sleep stage and the detected sleep oscillation.

The FPGA-accelerated DL model is a key component of the system. Although machine learning (including DL) algorithms have been developed to classify sleep stages, existing models have several common limitations: (1) demanding too much computational resources that are not available in energy-constrained wearable devices [8]; (2) using too many input channels that result in high power dissipation for signal acquisition and causing inconvenience in electrode placement; (3) using long time series as input (for example, more than a minute [2]), which causes latency in real-time operation and thus is not suitable for closed-loop modulation. In this work, we develop a DL model that uses only one EEG channel as input with a segment of 20 or 30 seconds. A sliding window with overlap is used to further reduce inference latency. The overall model consists of only 1.28 M parameters, which makes it suitable for FPGA implementation.

The block diagram of the proposed sleep modulation system is illustrated in Fig. 2. The key building modules include: an analog front-end (AFE) module for EEG acquisition and oscillation detection, a FPGA module for DL based sleep stage classification and closed-loop control, a stimulator module for delivering auditory feedback, and peripheral modules such as Flash memory and power management units.
The rest of the paper is organized as follows. Section III presents the DL model for the sleep stage classification. Section IV discusses the FPGA implementation of the DL model and the design of analog modules. Section V shows the experimental results. Finally, Section VI concludes the paper.

II. DEEP LEARNING MODEL FOR SLEEP STAGE CLASSIFICATION

Machine learning models have been developed to classify sleep stages [9]–[12]. Conventional machine learning models rely upon handcrafted features, including features in the frequency domain (e.g., fast Fourier transform [9]), the time domain (e.g., change in slope sign [11], waveform length [12]), or the time-frequency domain (e.g., discrete wavelet transform [10]). Although machine learning models with hand-crafted features have proven their ability to automate sleep scoring, they often render poor generality when applied to different subjects and electrode placements. Recently, DL models have shown promising results in classifying sleep stages without hand-crafted feature selection [13], [14]. Deep belief networks [13] and convolutional neural network (CNN) [14] models have been developed using time-domain signals directly as input. These models have shown the ability to extract time-invariant features, but miss time-variant features. To capture time-variant features, such as sleep stage transitions, recurrent neural networks (RNNs) can be used [15].

In this work, we developed a hybrid DL model that takes advantage of both CNN and RNN. Fig. 3 shows the model architecture. The model consists of three parts. The first part uses representation learning to capture time-invariant information from the input vector. The second part uses sequential learning to capture the sleep stage transition using features encoded in the first part. The third part consists of a dense network with residual connection to generate the prediction.

The representation learning part consists of two CNN paths, which are trained to learn features with different time scales. One path has a large filter size to capture general shape characteristics ($a_{shape}$) with low-frequency content, and the other path has a small filter size to capture detail shape characteristics ($a_{detail}$) with high-frequency content. Both CNN paths consist of four 1-D convolutional layers, two dropout layers, and one max-pooling layer. Each 1-D convolutional layer is followed by batch normalization and a rectified linear unit (ReLU) activation function. Two dropout layers are added to reduce overfitting. To demonstrate the generalizability of the model, we designed the representation learning part to accommodate input EEG signals with a length of 20-sec or 30-sec. This is made possible by adjusting the max-pooling
layer and the dropout layers in the two CNN paths, providing a similar output data length for the sequential learning part. Transitions between sleep stages often occur in patterns. Therefore, we designed a sequential learning part using a bidirectional LSTM network to capture the sleep transition. Only \( a_{\text{detail}} \) is used as input to the LSTM model for sequential learning, instead of concatenating \( a_{\text{detail}} \) and \( a_{\text{shape}} \). This allows us to obtain optimal performance at a low computational cost. The sequential learning part outputs the final forward hidden state \( h_f \) and the first reverse hidden state \( h_r \) of the extracted features.

The last part of the model is a dense network that generates the final prediction. Both the outputs of the representational learning part \( (a_{\text{shape}}, a_{\text{detail}}) \) and the sequential learning part \( (h_f, h_r) \) are taken as input. \( a_{\text{shape}} \) and \( a_{\text{detail}} \) are given to the dense network as residual connections. They add frequency content that is degraded in sequential learning, \( h_f \) and \( h_r \) are concatenated to provide sufficient time domain features in both the forward and reverse directions.

### III. HARDWARE DESIGN

#### A. FPGA-Accelerated Deep Learning Model

The DL model was implemented on Zynq®-7000 XC7Z020-CLG484-1 from AMD Xilinx. The blocks of the FPGA implementation are depicted in Fig. 2. A microcontroller unit (MCU) block integrated in the FPGA manages system control. The weights of the DL model are stored in the Flash memory and loaded to the data engine for processing. The MCU monitors the status of the data engine and loads the corresponding weights into the buffers.

The convolution engine processes the EGG data from the MCU subsystem and generates \( a_{\text{detail}} \) and \( a_{\text{shape}} \). Subsequently, the LSTM engine calculates \( h_f \) and \( h_r \) from \( a_{\text{detail}} \). Then the convolution engine performs the dense operation with the above results and sends the result to the MCU through the output buffer. Finally, the MCU performs softmax and obtains the final detection result. To minimize memory access, the convolution engine shown in Fig. 2 processes 4 kernels in parallel, with ReLu and max pooling operations. The address generator in the controller enables flexible data arrangement of input and output data, so that no additional data moving or reordering is required.

The LSTM engine concatenates the input and hidden states of each layer, so that the convolution engine is used to generate intermediate results of the forget gate, input gate, cell gate and output gate in scratch memory in working RAM. Then the LSTM datapath performs Sigmoid and Tanh operations, as well as the following multiplications and additions, to generate the updated cell state and hidden state. An optimized interpolation algorithm is used to implement Tanh and sigmoid operations. The interpolation algorithm shares the same multiplier with other LSTM operations for lower hardware complexity.

For simplicity of the memory system and better performance, memory blocks are designed with simple dual-port memory. The engine could process 20-sec input data within 1 sec when running at 20 MHz clock. It provides flexibility to support multiple EEG inputs as well as future algorithm enhancement. To further reduce the hardware cost, we applied static quantization for both weight and activation to signed 8 bit. We bench-marked three calibration methods, MinMax, entropy, and percentile. Appropriate data shifting and saturation operations are performed in the operations. Table I summarizes the final resources used for the FPGA implementation.

#### TABLE I

| Parameters                  | Multiplication Operation | Memory Required |
|-----------------------------|--------------------------|-----------------|
| CNN-shape                   | 425984                   | 7936            |
| CNN-detail                  | 278528                   | 425984          |
| LSTM                        | 196608                   | 7936            |
| Residual & dense            | 376832                   | 1277952         |
| Total                       | 1277952                  | 69004544        |

**B. Analog Front-end Module Design**

The AFE consists of an EEG acquisition path and a sleep oscillation detection path. The EEG acquisition path uses a commercial neural amplifier (RH2216, Intan Technologies) for signal amplification and digitization. The amplifier has a gain of 49.5 dB and a digitization resolution of 16 bits. The sleep oscillation detection path uses a 4th-order biquad filter, as shown in Fig. 2(a). The circuit uses only one operational amplifier per biquad core to save power consumption [16], [17]. The transfer function of the biquad filter is given by:

\[
H(s) = \frac{-s\left(\frac{\alpha}{C_1 R_{eq}}\right)}{s^2 + s\left(\frac{1}{C_1} + \frac{1}{C_2}\right) \frac{1}{R_3} + \frac{1}{C_1 C_2 R_3 R_{eq}}} \tag{1}
\]

where \( R_{eq} = (1/R_1 + 1/R_2)^{-1} \) and \( \alpha = R_4/R_1 \). The center frequency is

\[
\omega_0 = \frac{1}{\sqrt{C_1 C_2 R_3 R_{eq}}} \tag{2}
\]

and the quality factor is given by

\[
Q = \left[\frac{\sqrt{C_1 C_2 R_3 R_{eq}}}{R_3}\left(\frac{1}{C_1} + \frac{1}{C_2}\right)^{-1} \right]^{-1} \tag{3}
\]

A comparator is used to detect the zero-crossing point of the filtered oscillation signal. The detection signal is sent to the
FPGA and a programmable delay is added before triggering the stimulation.

C. Auditory Stimulation Module Design

The pink noise generation was implemented in the analog domain, as shown in Fig. 4(b). A 150 kΩ resistor is used as the source of white noise, which is amplified and filtered by a first-order low-pass filter to generate pink noise. The frequency characteristics can be further shaped by the filter. An energy-efficient class-D amplifier (TPA2005D1, Texas Instruments) was used to drive an 8 Ω piezo transducer speaker (AS01008MR-2-R, PUI Audio).

IV. EXPERIMENTAL RESULTS

A. Validation of the DL Model

A public database from the Montreal Archives of Sleep Studies (MASS) [18] was used to train and test the DL model. The MASS database contains 5 subsets (SS1-5) of adult polysomnography recordings, which were labeled by experts. We evaluated our model on the subset SS2 [19] and SS3 [20]. SS2 contains recordings of 19 subjects labeled per 20-sec EEG epoch based on the Rechtschaffen and Kales (R&K) standard; SS3 contains recordings of 62 subjects labeled per 30-sec EEG epoch based on the AASM standard. All EEG recordings have a sampling rate of 256Hz. Our model was developed to predict sleep stages based on the AASM standard. To convert the labels from R&K to AASM, N-REM stages 3 and 4 are combined to N3 and unknown stages are not taken into account.

To evaluate the model performance, we adopted a leave-one-subject out cross-validation strategy for SS2, and leave-two-subjects-out for SS3 since it contains more data. 10% of the test subjects’ data were used for fine-tuning per validation, and the remaining 90% of the data were used for testing. All test data were excluded from training. Adam optimizer was used for training with \( \text{lr} = 10^{-4} \), \( \text{beta1} = 0.9 \), \( \text{beta2} = 0.999 \) for 100 epochs. L2 weight decay was adopted to prevent overfitting with a value of \( 10^{-3} \). We used a batch size of 256 for general training. The sequence length of 3 is used in sequential learning. The extracted features of the previous two segments and the current segment were used as input to the sequential learning section. We used overall accuracy (ACC), macro F1-score, Cohen’s Kappa coefficient \((k)\) and per-class accuracy to evaluate the performance of our model.

Table II summarizes the performance of our model based on the evaluation in MASS-SS2. Performance before and after quantization is shown. The result suggests a marginal degradation of approximately 1% for significant hardware savings. Table III shows the performance of our model evaluated in MASS-SS2 and SS3 compared to the state-of-the-art works. On average of the 81 subjects, the accuracy of our model is 85.8% and the F1-score is 79%, which are comparable to the state-of-the-art DL models without hardware implementation.

| Data | Year | Publication | Methods | Overall Metrics |
|------|------|------------|---------|----------------|
| MASS | 2021 | EEGNet [21] | CNN+RNN | 83.1 76.4 75 |
| -SS3 | 2020 | IITNet [22] | CNN+RNN | 86.6 80.8 80 |
| | 2017 | DeepSleepNet [23] | CNN+RNN | 86.2 81.7 80 |
| | 2020 | TinySleepNet [24] | CNN+RNN | 87.5 83.2 82 |
| This work | | CNN+RNN | 86.1 80.0 79.4 |
| MASS | 2021 | MetaSleepLearner [25] | CNN | 77.3 69.9 68 |
| -SS2 | 2020 | TinySleepNet [24] | CNN+RNN | 82.6 75.5 75 |
| This work | | CNN+RNN | 84.9 75.8 77.8 |

B. Validation of Analog Modules and Closed-loop Operation

The analog front-end and auditory stimulation modules have been fully characterized on a bench. Fig. 5 shows the experimentally measured results for biquad filtering and pink noise generation. Closed-loop auditory stimulation has also been demonstrated (at the moment without the DL model). Fig. 6 illustrates the experiment, in which the system successfully detected the sinusoid test signal of 1 Hz and triggered synchronized auditory stimulation (picked up by a microphone).

V. CONCLUSION

This paper presents a first-of-its-kind closed-loop auditory sleep modulation system, featuring a FPGA-accelerated DL model that delivers real-time sleep stage classification with state-of-the-art performance. This design holds great promise in enabling novel sleep research paradigms with potential for clinical translation.
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