Accumulation-mode two-dimensional field-effect transistor: Operation mechanism and thickness scaling rule

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ABSTRACT: Understanding the operation mode of a two-dimensional (2D) material-based field-effect transistor (FET) is one of the most essential issues in the study of electronics and physics. The existing Schottky barrier-FET model for devices with global back gate and metallic contacts overemphasizes the metal-2D contact effect, and the widely observed residual conductance cannot be explained by this model. Here, an accumulation-mode FET model, which directly reveals 2D channel transport properties, is developed based on a partial top-gate MoS$_2$ FET with metallic contacts and a channel thickness of 0.65–118 nm. The operation mechanism of an accumulation-mode FET is validated and clarified by carefully performed capacitance measurements. A depletion capacitance-quantum capacitance transition is observed. After the analysis of the MoS$_2$ accumulation-mode FET, we have confirmed that most 2D-FETs show accumulation-mode behavior. The universal thickness scaling rule of 2D-FETs is then proposed, which provides guidance for future research on 2D materials.

INTRODUCTION

An accurate understanding of the operation mechanism of electronic devices is critical, especially for new channel materials, because the extraction of physical properties and the further control of the device characteristics are based on the operation mode. In recent years, transition metal dichalcogenide (TMD) field effect transistors (FETs) have attracted significant attention due to their potential application in ultimate scaled devices.1-5

Typical TMD-FET devices are composed of a metallic source and drain contacts, and the metal/channel interfaces are under gate control, that is, a typical global back gate structure, as shown in Figure 1a. One of the key performance-limiting factors in 2-dimensional (2D) FETs is the 2D/metal contact.6 Based on this idea and on the historical background of similar structures for carbon nanotubes,7 ultrathin silicon on insulator (SOI),8 and silicon nanowire FETs,9 the Schottky barrier FET (SB-FET) model is proposed and developed to explain the 2D-FET operation mechanism.10-12 Since the tunneling transport at the SB junction is dominant, studies on achieving low contact resistance by choosing metal types and inserting van der Waals materials and so on13-15 are promoted. The most important success in SB-FETs is the explanation of the ambipolar behavior. However, this model oversimplifies the channel effect in many cases. Although the injected carriers from contact will inevitably be scattered through the commonly used micro-long channel, the scattering issues are often neglected in the SB-FET model. Moreover, the residual conductance observed in most multilayer 2D-FETs when over the critical thickness16-31 cannot be explained by only the SB-FET model, suggesting a 2D depletion nature.18,28 These contradictions suggest the existence of an additional operation mode focusing on the channel properties.

Here, to clarify this channel depletion-related operation mode, we focus on partial top-gate FETs with ohmic metallic contacts, where the 2D/metal contact is not modulated as shown in Figure 1b.4,32,33 This type of device structure is often explained by accumulation mode (ACCU) FETs in a Si nanowire,34 as shown in Figure 1a, where the gate controls the on and off states via accumulation and depletion of the majority of carriers in the partial gate region. The unipolar behavior is achieved due to p/n junction formation. However, the accumulation mode mechanism in 2D-FETs and Si nanowires has not been systematically investigated.

The fundamental technique to directly detect carrier density and interface states in semiconductors is capacitance measurements (C-V),35-37 which provides critical insights to elucidate the 2D-FET operation mechanism. Although C-V measurements
are quite informative, blindly applying this method established based on a bulk metal-oxide-semiconductor (MOS) FET/capacitor to an ACCU-FET can lead to incorrect conclusions. Experimentally, C-V measurements in small-area 2D materials are very sensitive and always suffer from several difficulties. A systematic study on the parasitic capacitance resulting from an n'-Si/SiO₂ substrate and the channel resistance effect in C-V is necessary. Theoretically, quantum capacitance in monolayer MoS₂ has been clarified in our previous work. However, the study on capacitance transition from monolayer to bulk MoS₂ is still lacking.

In this work, mechanically exfoliated MoS₂ with a thickness from 0.65 (monolayer) ~ 118 nm is selected as the channel material for top-gate FET devices. Systematic investigations of C-V and I-V measurements are carried out for the same samples. For C-V, the parasitic capacitance is totally suppressed by using a quartz substrate. Frequency dispersion for low-mobility thin 2D channels mainly comes from the channel resistance effect. A transition from quantum capacitance (C₀) to depletion capacitance (C₅₀) is observed from monolayer to bulk MoS₂. Having clarified the electrostatic field-effect control mechanism of carriers by C-V, the electrical transport data are explained by ACCU-FET for all channel thicknesses. The thickness scaling rule is proposed based on the ACCU-FET mechanism, which provide the complete picture of the transport properties for most of the 2D materials.

**RESULTS AND DISCUSSION**

**I-V characterization; increase in on-state conductivity and residual conductance.** Figure 1a, b shows a schematic drawing and optical image of the Al₂O₃ top-gate MoS₂ FET on the insulating quartz substrate. Figure 2a shows the typical conductivity (σ) – top gate voltage (V TG) characteristic at V DS = 0.1 V with a MoS₂ thickness (tMoS₂) of 0.65, 16, 44, and 58 nm. It should be noted that σ is normalized by the width and length without the thickness of MoS₂ flakes. Monolayer MoS₂ shows a clear off and subthreshold region. There are two distinct features observed by increasing the MoS₂ thickness. One is the increase in the on-state conductivity for the 16-nm-thick sample, which gradually saturates for thicker MoS₂ samples. The other is the abrupt increase in the residual conductance for the 44-nm-thick sample.

To focus on these two features, the maximum conductivity and the ratio of on-state to off-state current (IOn/IOFF) are shown in the range of tMoS₂ = 0.65 ~ 118 nm in Figure 2b. The maximum conductivity is controlled by the conductivity of the

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**Figure 1.** (a) Schematic of a back-gate SB-FET (left). Band diagrams of the n-branch, off state, and p-branch are shown below. Schematic of a top-gate ACCU-FET (right). Band diagrams of the accumulation and depletion states are shown below. The x and z directions in the Cartesian coordinate are defined. (b) Optical image of the device on a quartz substrate. The access region refers to the channel region uncovered by the top gate electrode. The existence of access region guarantees that contact region is not modulated by top-gate bias, and the effective channel length is defined by top-gate electrode width. S, D and TG indicate the source, drain and top gate electrodes, respectively.
accumulation layer, not by the parasitic resistance since $\sigma$ gradually increases with increasing $V_{\text{TG}}$, even for the 58-nm-thick sample. Therefore, it is discussed similarly to the mobility analysis in MoS$_2$. Instead of intrinsic photon scattering, coulomb scattering due to interfacial impurities is found to be dominant in the scattering mechanism of ultrathin MoS$_2$. The extrinsic Debye length ($L_D$) is given here for the screening length of Coulomb scattering since most of the 2D materials are intrinsically charged by defects and impurities.

$$L_D = \sqrt{\frac{\varepsilon_{\text{MoS}_2} k_B T}{e^2 N_D}}. \quad (1)$$

$\varepsilon_{\text{MoS}_2}$, $k_B$, $T$, and $e$ are defined as the dielectric constant of MoS$_2$ in the direction normal to the basal plane, the Boltzmann constant, the temperature, and the elementary charge, respectively. $N_D$ is the density of the donors (density of acceptors $N_A$ for $p$-type 2D). $2 \times L_D$ is used in the following discussion to account for both the top and bottom interfaces. The MoS$_2$ with $t_{\text{MoS}_2} > 2L_D$ will be undisturbed by the interfaces and maximum conductivity is saturated. Consideration of quantum-mechanical effect of accumulation capacitance ($C_A$) would give a more accurate carrier distribution in thick MoS$_2$ flakes.\(^{45}\)

For $I_{\text{ON}}/I_{\text{OFF}}$, two regions are clearly observed: $I_{\text{ON}}/I_{\text{OFF}} > 10^5$ for $t_{\text{MoS}_2} = 0.65 - 35$ nm and $I_{\text{ON}}/I_{\text{OFF}} < 10$ for $t_{\text{MoS}_2} > 60$ nm. The transition occurs at $t_{\text{MoS}_2} \approx 48 - 55$ nm. For ACCU-FET,\(^{46}\) the conduction comes from “body current flow”, which is modulated by the depletion region in the channel. The screening length ($\lambda_{\text{ACCU-FET}}$) is determined by the maximum depletion width ($W_{\text{Dm}}$), which can be expressed as follows:

$$\lambda_{\text{ACCU-FET}} = W_{\text{Dm}} = \sqrt{\frac{4e\varepsilon_{\text{MoS}_2} k_B T \ln(N_D/n_i)}{e^2 N_D}}, \quad (2)$$

where $n_i$ is intrinsic carrier density. $\lambda_{\text{ACCU-FET}}$ is independent of oxide capacitance ($C_{\text{ox}}$). An increase in the residual conductance occurs (e.g., 44-nm-thick sample in Figure 2a) when $t_{\text{MoS}_2}$ becomes close to $W_{\text{Dm}}$ due to screening of the gate control. The present data indicates that $W_{\text{Dm}}$ is $\approx 48 - 55$ nm. It should be noted that this $W_{\text{Dm}}$ is roughly consistent with that in the previous data for global back gate MoS$_2$ FETs.\(^{18,19}\) Generally, the global back gate 2D layered channel FET has been considered an SB-FET. In the case of SB-FETs, the off-state is achieved by controlling the barrier height at the MoS$_2$/metal contact independent of the channel thickness. This behavior is inconsistent with the SB-FET model. Moreover, for the global back gate 2D devices, the degradation of subthreshold swing (S.S.) with increasing channel thickness has been claimed as evidence for SB-FETs.\(^{12}\) However, the similar degradation of S.S. is clearly observed due to the reduction in gate control by $t_{\text{MoS}_2} \sim W_{\text{Dm}}$, as shown in

![Figure 2](image_url)

**Figure 2.** (a) $\sigma-V_{\text{TG}}$ characteristics at $V_{\text{DS}} = 0.1$ V with a MoS$_2$ thickness of 0.65, 16, 44, and 58 nm. (b) Maximum conductance and $I_{\text{ON}}/I_{\text{OFF}}$ ratio as a function of thickness.
These discussions suggest that ACCU-FET mode could exist in conjunction with SB-FET mode, even in widely fabricated back-gate 2D-FETs. In the following discussion, we use “bulk” for MoS$_2$ with $t_{MoS2} > W_{Dm}$ and “multilayer” for $t_{MoS2} < W_{Dm}$ for simplicity.

**C-V characterization; $C_Q$ & $C_D$.** To gain further insight into the operation mechanism of ACCU-MoS$_2$ FETs, C-V measurements with a frequency range of 1 k ~ 1 MHz are also conducted for the same devices. It should be noted that MoS$_2$ flakes with a large area (> 30 $\mu$m$^2$) were selected to improve the signal-to-noise ratio in the capacitance measurement. The full equivalent circuit used to model the top gate MoS$_2$-FETs is shown in Figure 3a. Here, $C_{par1}$ and $C_{par2}$ are the two types of commonly observed parasitic capacitance. $R_{acc}$ is defined as the sum of MoS$_2$/metal contact resistance and MoS$_2$ resistance at the access region indicated in Figure 1b, which is constant. $R_{channel}$ is the MoS$_2$ channel resistance just below the top gate electrode and is modulated by the top gate bias. $C_{it}$ and $R_{it}$ are the interface states’ capacitance and resistance, respectively, which account for carrier capture and emission processes. $C_{D(A)}$ and $C_Q$ are the focus of this paper, and they determine the carrier density in the conduction band (CB). $R_D$ is the resistance that models the supply of carriers to the depletion layer when $C_{D(A)}$ dominates the capacitance.

Several pitfalls are first discussed for MoS$_2$-FET-based C-V. The first pitfall is the parasitic capacitance effect, which comes from the widely used n$^+$-Si/SiO$_2$ substrate. As indicated previously, in the double-gated geometry, there is capacitive coupling between back and top gates through the large contact pad area, which induces large parasitic capacitance. $C_{par1}$ refers to the parasitic capacitance that is charged or discharged through constant $R_{acc}$. This will induce large frequency dispersion (> $C_{ox}$) in C-V and corresponding peaks in the conductance-frequency ($G_p$/ω-f) measurement (Supplementary Figure S1). $C_{par2}$ refers to the parasitic capacitance that could shift the baseline of the C-V curve. A quartz substrate is used in this paper to totally remove these parasitic capacitances (Supplementary Figure S2). In this situation, $C_{ox}$ can be obtained in the strong

![Figure 2a](image1.png)

![Figure 3a](image2.png)

![Figure 3b](image3.png)

![Figure 3c](image4.png)

![Figure 3d](image5.png)

![Figure 3e](image6.png)
accumulation region when no frequency dispersion is observed.

The second pitfall is the access resistance effect, which could induce frequency dispersion in the accumulation region in $C-V$. $R_{\text{access}}$ is experimentally measured as the residual impedance at the high-frequency limit in the strong accumulation region where the other resistance is shunted. The measured $R_{\text{access}}$ is on the order of $\approx 10$ k$\Omega$ in most of the samples due to the natural $n$-doped property of MoS$_2$ and the low contact resistance with Ni. As shown in Supplementary Figure S3 and Note S1, the $R_{\text{access}}$ effect in our measured frequency range can be neglected since $R_{\text{access}}$ is smaller than $\approx 5 \times 10^4$ $\Omega$. We have to mention that $R_{\text{access}}$ can still severely affect capacitance measurements at low temperature and for other 2D materials with higher resistance. Now, the equivalent circuit can be simplified (Figure 3a), where the experimentally measured source/drain to gate capacitance is defined as $C_{\text{total}}$.

Figure 3b-e shows the experimental $C_{\text{total}}$-$V_{\text{TG}}$ curves in the frequency range of 1 kHz - 1 MHz with $t_{\text{MoS}_2} = 0.65$, 10, 16 and 58 nm, respectively. Since the parasitic capacitance is totally removed by using the quartz substrate, the minimum capacitance plateau observed for $t_{\text{MoS}_2} = 58$ nm results from the contribution of $C_D$ with $W_{\text{Dm}}$. That is, the inversion layer is formed, resulting in a constant depletion width. The electrical communication still passes through free electrons at the edge of the depletion region because the $p$-$n$ junction is formed between the inversion layer and un gated $n$-channel region. This $C-V$ curve is consistent with that of a 1-$\mu$m-thick MoS$_2$ capacitor,38 which also supports that $W_{\text{Dm}}$ is shorter than $t_{\text{MoS}_2} = 58$ nm. This cannot occur in SB-FET but is unique to the depletion behavior in ACCU-FET. As a result, the undepleted MoS$_2$ layer will always remain, which results in residual conductance and low $I_{\text{ON}}/I_{\text{OFF}}$ in $I-V$. On the other hand, for monolayer MoS$_2$, $C_Q$ contributes to $C_{\text{total}}$, instead of $C_D$. It originates from the partially occupied density of states (DOS) of CB modulated by the Fermi energy ($E_F$) in the Fermi-Dirac distribution.48,49 Distinct from $C_D$, one of the main behaviors of $C_Q$ is that it follows an exponential decrease with respect to $E_F$ when $E_F$ is modulated in the band-gap. Due to the large band-gap of MoS$_2$, $C_Q$ can reach a small value, which results in an extremely low carrier density. This will be experimentally observed as a decrease to almost zero in $C-V$ (Figure 3b) and a clear subthreshold/off region in $I-V$ (Figure 2a). Although Figure 3c, d shows the transition from $C_Q$ to $C_D$, it is somewhat complicated. Therefore, it will be discussed later with the help of the quantitative analysis.

**Frequency dispersion by channel charging effect in $C-V$.** Before considering the transition from $C_Q$ to $C_D$ with increasing $t_{\text{MoS}_2}$, $R_{\text{channel}}$ is discussed since it could induce frequency dispersion in the depletion region in $C-V$. Shockley-Read-Hall (SRH) theory is the basis to study carrier capture and emission process by the traps.50 Based on this theory, a series $R_{\text{tr}}$-$C_{\text{tr}}$ network is modeled in the equivalent circuit, and experimental impedance spectroscopy always tries to capture this $R_{\text{tr}}$-$C_{\text{tr}}$-induced signal by excluding other capacitance or resistance effects. Large frequency dispersion is widely observed in the capacitance measurement of thin MoS$_2$ and other 2D-FET.5,33,39,41 It is often treated as $R_{\text{tr}}$-$C_{\text{tr}}$-induced signals. However, other resistance effects could also introduce frequency-dependent signals. $R_{\text{channel}}$ is always parasitic in the FET structure, which cannot be avoided. In this section, $R_{\text{channel}}$ effect will be studied quantitatively. Monolayer MoS$_2$ is selected here because it shows the largest frequency dispersion and the simplest $C_Q$ expression.

Figure 4a shows the equivalent circuit of monolayer MoS$_2$ FET. $C_1$ is defined as the ideal capacitance by neglecting any resistance effect, and $C_1 = \frac{(C_Q+C_{\text{tr}})C_{\text{ox}}}{C_Q+C_{\text{tr}}+C_{\text{ox}}}$. Experimentally, when resistance exists in the equivalent circuit, it will give the $R$-$C$ circuit, in which the time constant ($\tau$) is determined. $C_{\text{total}}$ will decay from $C_1$ for $\omega \tau > 1$, where $\omega$ is angular frequency. $\tau_{\text{Rch}}$ and $\tau_{\text{in}}$ are defined as the time constants from $R_{\text{channel}}$ and $R_{\text{in}}$, respectively. Figure 4b shows measured $C_{\text{total}}$ as a function of frequency ($C$-$f$) at different $V_{\text{TG}}$ for the monolayer device in Figure 3b. The clear decay of $C_{\text{total}}$ at a specific frequency indicates that the capacitance is limited by one type of resistance.

For $\tau_{\text{Rch}}$, it is derived from a transmission line model51,52 as follows (Supplementary Figure S4, Note S2):

$$\tau_{\text{Rch}} = \frac{C_1R_{\text{S, channel}}L^2}{4},$$

where $L$ is the channel length and $R_{\text{S, channel}}$ is the sheet resistance of MoS$_2$ channel. The drift current model49
is applied to express $R_{\text{S,channel}}$. Because the channel is
on the order of micrometers in length and the drain bias is small, the diffusion current is negligible. Moreover, the drift current model reveals free carrier transport in the conduction band, which enables us to correlate $C-V$ with $I-V$ in the next part. $R_{\text{S,channel}} = \frac{1}{\epsilon n_{\text{ch}} \mu}$, where $n_{\text{ch}}$ is the channel carrier density and $\mu$ is the drift mobility. $C_{\text{it}}$ and $\mu$ are extracted from the $I-V$ characteristics$^{33}$ (Supplementary Figure S5). A higher $C_{\text{it}}$ means that more states need to be charged, which results in a larger $R_{\text{it}}$. On the other hand, $\tau_{\text{it}}$ is calculated based on SRH theory$^{33}$ in a 2-dimensional system as follows:

$$\tau_{\text{it}} = \frac{1}{\sigma_{\text{capture}-2D} V_{\text{th}} n_{\text{ch}}}$$

where $\sigma_{\text{capture}-2D}$ is the capture cross section of interface states, which largely depends on the type of interface states. For point defects (e.g., sulfur vacancy), it would be close to the atom size of $\sim 0.3$ nm. For band tail interface states induced by bond bending of Mo-$d$ orbitals,$^{33}$ it could be on the order of 10 nm.$^{34}$ Therefore, $\sigma_{\text{capture}-2D}$ is assumed to be in the range of 0.3$\sim$10 nm. $V_{\text{th}}$ is thermal velocity of $\sim 1.2 \times 10^7$ cm/s at room temperature by considering the electron effective mass of monolayer MoS$_2$ as $m^* = 0.6 m_0$, where $m_0$ is the electron mass in a vacuum.

The calculated time constant as a function of $E_F$ is shown in Figure 4c. $\tau_{\text{it}}$ w/ $C_{\text{it}}$ is $\sim 3$ orders of magnitude larger than $\tau_{\text{it}}$ and is distributed across the measured frequency range of 1 kHz to 1 MHz, which indicates that the time constant due to the channel charging effect is the origin of the frequency-dependent capacitance behavior in Figure 4b. It is noted that both $\tau_{\text{it}}$ and $\tau_{\text{Rch}}$ with $C_{\text{it}}$ have a similar exponential $E_F$ dependence because the parameter $n_{\text{ch}}$ is included.

The experimental $C-V$ and $C-f$ curves are then reproduced by considering $R_{\text{channel}}$ instead of $R_{\text{it}}$. $C_{\text{total}}$ is derived as (Supplementary Note S2):

![Figure 4](image-url)

**Figure 4.** (a) Simplified lumped equivalent circuit to model monolayer MoS$_2$-FET $C-V$. Both $R_{\text{channel}}$ and $R_{\text{it}}$ could limit the frequency response of the capacitance. (b) Experimental $C_{\text{total}}$ as a function of frequency at different $V_{\text{TG}}$ (-3.4$\sim$2.4 V) from monolayer MoS$_2$ FETs. A large frequency response is observed, which corresponds to the frequency dispersion of $C-V$ in Figure 3b. (c) Calculated time constant as a function of $E_F$. Monolayer MoS$_2$ is assumed to have a bandgap of 1.9 eV. $E_F = 0.95$ eV indicates the bottom of the CB. Dash line indicates the experimental measured frequency range by using $\tau=1/\omega$. (d) Calculated plot of $C_{\text{total}}$-$V_{\text{TG}}$ curves. (e) Calculated plot of $C_{\text{total}}$-$f$ curves at different $V_{\text{TG}}$ values (-3.4$\sim$2.4 V). (f) Maximum $\tau_{\text{Rch}}$ as a function of mobility at different $L$. 

\[ C_{\text{total}} = C_1 \text{Re} \left[ \frac{\tan \lambda}{\lambda} \right], \]

where \( \lambda = \sqrt{j \omega \tau_{\text{rch}}} \).  \( (5) \)

\[ V_{\text{TG}} \text{ is calculated as follows:} \]

\[ V_{\text{TG}} = V_{\text{TG,mid-gap}} + \int_{0}^{E_{F}/e} \left( C_{Q}(\mu) + C_{\infty} \right) / C_{\infty} d(E_{F}/e) \]

\( (6) \)

\( V_{\text{TG,mid-gap}} \) is a fitting parameter to compensate the MoS\(_2\) n-doping effect. Equation (6) will be used to correlate \( E_{F} \) with \( V_{\text{TG}} \). Later, we will study multilayer MoS\(_2\), where the surface potential \( \mu_{S} \) is used instead of \( E_{F}/e \). \( C_{\infty} \) is included in equation (6) since the interface states always respond to the direct current (dc) \( V_{\text{TG}} \). The simulation reproduces the experimental data quite well (Figure 4 d,e), suggesting that the experimentally observed frequency dispersion in \( C-V \) does not result from the electron capture/emission process at the interface traps but from the channel charging effect. From the above study of \( R_{\text{channel}} \) effect, let us review our previous work on the \( C-V \) study of monolayer MoS\(_2\).\(^{33}\) \( C_{Q} \) with a clear temperature dependence is correctly extracted since it is obtained at the strong accumulation region where \( R_{\text{channel}} \) is shunted. Although the band-tail type energy distribution for the interface states is also reserved qualitatively, the widely used high-low frequency method on 2D-FET-based \( C-V^{5,33,39,41} \) will not reveal the true \( C_{\infty} \) value quantitatively because the extracted time constant is indeed \( \tau_{\text{rch}} \) instead of \( \tau_{\text{it}} \).

To provide guidance on how to avoid the channel charging effect in all 2D-FET-based \( C-V \) with different thicknesses from monolayer to multilayer, the universal expression is derived. The region where \( C_{Q} \ll C_{\infty} \) should be considered since the \( R_{\text{channel}} \) effect is severe due to the low carrier density. We assume that \( C_{\infty} \) is smaller than \( C_{Q} \), that is, attention should always be paid to improve the interface. In this case, \( C_1 = C_{Q} \). Then, based on equations (3, 8) and the definition of \( C_{Q} = \frac{\text{dn}_{\text{ch}}}{d\phi_{S}}, \tau_{\text{rch}} \) will have a constant maximum, which is similar to \( \tau_{\text{it}} \) in the monolayer case (Figure 4c). This is because \( \tau_{\text{rch}} \) in both \( C_{Q} \) and \( R_{\text{S,channel}} \) cancel with each other. This constant maximum is shown as follows:

\[ \text{Maximum } \tau_{\text{rch}} = \frac{L^2}{4 \mu (k_{B}T/e)} \]  \( (7) \)

The maximum \( \tau_{\text{rch}} \) is shown as a function of \( \mu \) for various \( L \) in Figure 4f. \( \tau_{\text{rch}} \) should be smaller than the measured frequency range to avoid the channel charging effect. For \( L = 1 \mu m \), the allowable \( \mu \) can be as low as \( 1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1} \). However, due to both experimental difficulty and small signal-to-noise ratio, \( L \) is usually in the range of \( 5 \sim 20 \mu m \) in our samples. In this case, \( \mu \) is very important, \( \mu \) is usually low in monolayer 2D materials, i.e., \( < 100 \text{ cm}^2\text{V}^{-1}\text{s}^{-1} \), at room temperature, while multilayer 2D materials have a higher \( \mu \), which has the potential to avoid the channel charging effect. This has been confirmed in our 16-nm-thick device with suppressed frequency dispersion in Figure 3d. On the other hand, for graphene-based FETs, this effect can usually be neglected due to the extremely high \( \mu \), which accounts for the recently observed frequency dispersion-free \( C_{\infty} \) in a bilayer graphene/h-BN/graphite heterostructure.\(^{55}\)

**C\(_D\)-C\(_Q\) transition and MoS\(_2\) ACCU-FET operation mechanism.** Now let us consider the \( C_{D}-C_{Q} \) transition. Most of the measured MoS\(_2\) FETs with \( t_{\text{MoS2}} > 55 \text{ nm} \) show depletion capacitance (accumulation capacitance)-dominant \( C-V \) without thickness dependence. \( C_{D} \) and \( C_{A} \) are separated by flat-band voltage \( (V_{\text{FB}}) \). Moreover, channel resistance-induced frequency dispersion is totally suppressed because \( R_{\text{channel}} \) is shunted by the unmodulated conductive MoS\(_2\) region, which results in a low charging resistance \( R_{\text{ch}} \). Thus, the equivalent circuit can be simplified as a lumped circuit, and conventional \( C_{D(A)} \) analysis method can be applied. This enables us to extract parameters such as \( N_{D} \) and \( \epsilon_{\text{MoS2}} \) of bulk MoS\(_2\). The minimum \( C_{D} \) is given as \( \text{Minimum } C_{D} = \frac{\epsilon_{\text{MoS2}}}{W_{\text{dm}}} \). By considering that \( W_{\text{dm}} \) is 48~55 nm and the minimum \( C_{D} \) is \( \sim 0.1 \mu\text{F/cm}^2 \), bulk \( \epsilon_{\text{MoS2}} \) is extracted as 6.3. This is roughly consistent with the calculated bulk \( \epsilon_{\text{MoS2}} \) in the 5 z direction.\(^{56}\)

Based on equation (2), \( N_{D} \) is determined to be \( 2\sim3 \times 10^{17} \text{ cm}^{-3} \). With these parameters, by using conventional \( C_{D} \) expression (Equation (11) in Supplementary Note S3) and equation (6) without \( C_{\infty} \), the \( C-V \) of 58-nm-thick MoS\(_2\) is fitted (Figure 5a). The simulated \( C-V \) fits well with the experimental data. The slight deviation is due to \( C_{\infty} \)-induced distortion and the stretch-out effect.
C \text{D}\text{r-CQ} \text{ transition always occurs in multilayer MoS}_2 \text{ FET-based C-V. Firstly, free electrons at the edge of the depletion region still communicate electrically with S/D through the un gated n-channel region. By modulating } V_{TG} \text{ negatively, the depletion width will reach } t_{MoS2} (16 \text{ nm}). As a result, the electrical communication in C-V occurs between S/D and the quite small density of free electrons in the “depletion region”. Based on this scenario, when the depletion width reaches } t_{MoS2}, \text{ it can be considered that the } C_{\text{D}}\text{-CQ transition occurs, since the carrier density in the “depletion region” can be controlled by } C_{Q}. \text{ Therefore, the C-V curve goes to zero even for the multilayer. After the whole channel is depleted, the surface potential will be continuously increased by further decreasing } V_{TG}. \text{ Finally, the inversion layer will be formed. However, inversion capacitance corresponding with the } p\text{-branch in } I-V \text{ cannot be observed because of the } p-n \text{ junction, as schematically illustrated in Figure 5b.}

Now, let us reproduce the C-V curve for } t_{MoS2} = 16 \text{ nm by simple analytical calculation. Since the expression for } C_{\text{D(A)}} \text{ is already obtained, the surface potential } (\psi_{s}) \text{ is calculated in order to obtain the expression for } C_{Q} \text{ of multilayer MoS}_2. \text{ The boundary condition of electric field } = 0 \text{ at } z = t_{MoS2} \text{ is used for the solution of the one-dimensional Poisson equation. This is the intrinsic condition for the present 2D-FET structure, where the channel is always surrounded by the insulator or other insulating environment. The calculated potential distribution is shown in the inset in Figure 5b. By modulating the surface potential with the change of } \Delta \psi_{s}, \text{ the potential in the channel changes everywhere } (\Delta \psi_{z}) \text{ with the same value, that is, } \Delta \psi_{z} = \Delta \psi_{s}, \text{ indicating that the whole channel can be fully controlled by } \psi_{s} \text{ and } \psi_{s} \text{ has a similar function as } E_{F} \text{ in monolayer } C_{Q} \text{ to modulate } n_{\text{L}}. \text{ With the calculated potential distribution, } C_{Q} \text{ is shown below (Supplementary Note S3):}

\begin{equation}
C_{Q} = N_{Q} \exp\left(\frac{\psi_{s}}{k_{B}T}\right), \tag{8}
\end{equation}

where } N_{Q} \text{ is a constant independent of } \psi_{s}. \text{ It is not surprising to see that } C_{Q} \text{ in the multilayer has a similar formula as that in the monolayer case with the same exponential } e/k_{B}T \text{ dependence.} \text{ Then, using } C_{Q} \text{ and } C_{\text{D(A)}} \text{ without } C_{\text{IT}}, \text{ the experimental data are}

Figure 5. (a) Depletion capacitance (accumulation capacitance) of a 58-nm-thick MoS2 FET. The green circle is the experimental C_{\text{D(A)}}-V_{TG} \text{ curve at } 1 \text{ MHz from Figure 3e. The blue and orange solid lines are the theoretical fitting curve based on } C_{Q} \text{ and } C_{A} \left( C_{\text{total}} = \frac{C_{\text{D(A)}}C_{\text{IT}}}{C_{\text{D(A)}}+C_{\text{IT}}}, \right) \text{ respectively. The inset is the simplified lumped equivalent circuit to model bulk MoS}_2\text{-FET C-V. The bottom schematic shows the situation for } V_{TG} < 0 \text{ V. (b) } C_{\text{D}}\text{-CQ transition in a 16-nm-thick MoS}_2 \text{ FET. The green circle is the experimental C_{\text{D(A)}}-V_{TG} \text{ curve at } 1 \text{ MHz from Figure 3d. The blue, orange and red solid lines are the theoretical plots based on } C_{D}, C_{A} \text{ and } C_{Q} \left( C_{\text{total}} = \frac{C_{\text{D}}C_{\text{IT}}}{C_{\text{D}}+C_{\text{IT}}}, \right) \text{ respectively. The inset shows the potential distribution calculated as a function of MoS2 thickness } (z \text{ direction) at different values of } \psi_{s}. \text{ The bottom schematic shows the situation for } V_{TG} < 0 \text{ V. (c) Transfer characteristics of a } 16\text{-nm-thick MoS}_2 \text{ ACCU-FET. The green circuit is the experimental } \sigma\text{-V}_{TG} \text{ curve from Figure 2a. The orange and red solid lines are the ideal theoretical fitting curves without } C_{\text{IT}} \text{ and with } C_{\text{IT}}, \text{ respectively.}
well fitted, as shown in Figure 5b. The cross point indicates the transition from $C_D$ to $C_Q$ at $t_{MoS_2} = W_D$. The slight deviation from the analytical $C_Q$ comes from the contribution of $C_h$. In Figure 3b-e, the transition from $C_D$ to $C_Q$ is clearly seen with decreasing MoS$_2$ thickness. Moreover, it is interesting that the frequency dispersion is observed only in the $C_Q$-dominant region. This is because the charging resistance $R_D$ is low enough for the $C_{D(A)}$-dominant region, while $R_{\text{channel}}$ is quite high for the $C_Q$-dominant region.

A large advantage for $C-V$ on the FET structure is that it directly estimates the carrier density in the transport phenomenon of $I-V$. Meanwhile, for $C-V$ on the capacitance structure, the potential distribution in the channel is affected by the additional back metal contact, and the whole depletion channel cannot be obtained.\(^{57}\) Having theoretically calculated all of the components in $C_{\text{total}}$, it is possible to further reproduce the $I-V$ characteristics by introducing the drift current model. $n_{ch}$ is calculated as $n_{ch} = \int C_{Q/D(A)} d\psi$. The $V_{\text{TG}}-\psi_e$ relation is again calculated from equation (6) (parameters are shown in Supplementary Figure S5). The simulation result of this 16-nm-thick MoS$_2$ sample is shown in Figure 5c. The ideal $S.S.$ of ~60 mV/dec can be obtained without the $C_h$ effect, which comes from the thermal limitation in $C_Q$. The experimental $I-V$ from the off state to the linear region is then fully reproduced by including the $C_h$ effect. $S.S.$ is degraded to ~130 mV/dec as well as a gradual transition from linear to the subthreshold region in the linear region. In the ACCU-FET, the equation to describe $S.S.$ is given equivalently as in the conventional MOSFET as:

$$S.S. = \ln10 \frac{k_B T}{e} \frac{C_{as} + C_h}{C_{ox}}.$$  \hspace{1cm} (9)

This equation is valid from monolayer to multilayer when $t_{MoS2} \ll W_{Dm}$. $C_Q$ does not appear in this equation since it is much smaller than $C_h$ and $C_{ox}$ at the $S.S.$ region. $S.S.$ will be degraded when $t_{MoS2}$ becomes close to or larger than $W_{Dm}$ due to losing the gate control of the whole channel, as shown in Figure 2a. Combined with the $I-V$ analysis in monolayer MoS$_2$ (Supplementary Figure S5) as well as the $C-V$ analysis, we have successfully clarified the operation mechanism of MoS$_2$ ACCU-FET from monolayer to bulk flakes.

**Thickness scaling rule.** Compared with SB-FETs, where the tunneling transport at the SB contact junction is dominant, the channel transport properties are straightforwardly revealed for the present ACCU-FETs. The carrier density modulation with the drift

![Figure 6. Thickness scaling rule of a 2D ACCU-FET. Baselines of $W_{Dm}$ and $2L_D$ are calculated from the parameters of bulk MoS$_2$. Band-gap = 1.29 eV and $\epsilon = 6.3$. With a scaling thickness of 2D from bulk to monolayer, three regions will be observed. They are divided by $W_{Dm}$ and $2L_D$. Different types of 2D materials are shown here as a function of $N_0$ ($N_A$). Most of the 2D materials summarized here come from the mechanical exfoliation method, which gives a relatively stable $N_0$ ($N_A$). This situation might be different when using synthesis approaches.](image-url)
current model used above gives a complete picture of carrier band transport under the gate field-effect condition. Now, the transport mechanism is divided into three regions as a function of $t_{\text{MoS}_2}$. When $t_{\text{MoS}_2} > W_{\text{Dm}}$, the channel is only partially controlled by the gate and shows band transport. The existence of residual conductance is the sign of this region. When $2L_D < t_{\text{MoS}_2} < W_{\text{Dm}}$, the channel is fully controlled with optimized mobility because of screening of interfacial Coulomb scattering. Band transport also dominates in this region. When $t_{\text{MoS}_2} < 2L_D$, band transport is still dominant at room temperature, but it often suffers from mobility degradation due to prominent interfacial Coulomb scattering. In the subthreshold region at low temperature, the localized states induced transport such as hopping will become dominant. It should be noted that both $W_{\text{Dm}}$ and $2L_D$ are independent of $C_{\text{ox}}$, which enables us to propose the thickness scaling rule of transport properties for various 2D materials as a function of $N_D$ ($N_A$) (Figure 6). The summarized 2D materials here have a band-gap of 1–2 eV and a similar dielectric constant. A WSe$_2$ global back-gate FET on a SiO$_2$ (90 nm)/$n^+$-Si substrate was fabricated and characterized for comparison (Supplementary Figure S6). Although the observation of both $n$- and $p$-branches is explained by the SB-FET model, the increase in the maximum conductance and residual conductance with increasing WSe$_2$ thickness also reveals ACCU-FET behavior. As mentioned before, transport properties for the present top gate MoS$_2$ FET are consistent with that from global back gate MoS$_2$ devices. Therefore, almost all of the data on $W_{\text{Dm}}$ and $L_D$ in Figure 6 are obtained from global back gate devices in the previous literature. At high $N_D$ ($N_A$) region ($>10^{19}$ cm$^{-2}$), $W_{\text{Dm}}$ will decrease substantially, resulting in a small thickness window for “fully controlled band transport”, that is, fully depleted. In fact, full control of channel will be lost when the 2D thickness become greater than $W_{\text{Dm}}$. Moreover, it will be more degraded by considering a heavy doping effect such as band gap narrowing. This explains why well-controlled FETs with high $I_{\text{ON}}/I_{\text{OFF}}$ are difficult to achieve in recent heavily doped 2D materials such as PtS$_2$, PtSe$_2$, SnS, and SnSe. Meanwhile, $2L_D$ is scaled down to just several atomic layers of thickness. This strong electrostatic confinement effect combined with increased $N_D$ ($N_A$) will introduce strong scattering. Band transport is difficult to achieve in atomically thin flake of these heavily doped 2D materials, and the Anderson localization phenomenon is suggested to be observed. Moreover, in terms of 2D/metal contact, heavily doped 2D materials generally show low contact resistance because of the thin Schottky barrier width. From the above analysis, well controlled doping approaches on 2D crystals are in great demand for improving the performance of 2D ACCU-FET.

CONCLUSION

As a conclusion, the top gate MoS$_2$-FETs are found to work at accumulation-mode, whose operation mechanism is clarified by capacitance measurement with special precautions. The ACCU-FET study here provides a new platform and analytical mode for the electronics and physics of novel nanomaterials. Moreover, the universal thickness scaling rule of 2D-FETs is proposed in terms of $W_{\text{Dm}}$ and $L_D$, which is applicable to most of semiconductor 2D materials.

Methods

MoS$_2$ films were mechanically exfoliated onto the insulating quartz substrate from natural bulk MoS$_2$ flakes. Ni/Au was deposited as source/drain electrodes. Then, Y metal with a thickness of 1 nm was deposited via thermal evaporation of the Y metal in a PBN crucible in an Ar atmosphere with a partial pressure of $10^4$ Pa, followed by oxidization in the laboratory atmosphere to form the buffer layer. The Al$_2$O$_3$ oxide layer with a thickness of 10 nm was deposited via atomic layer deposition, followed by the Al top-gate electrode formation. Raman spectroscopy and atomic force microscopy (AFM) were employed for determining the flake thickness. $I$–$V$ and $C$–$V$ measurements were conducted using Keysight B1500 and 4980A LCR meters, respectively. All electrical measurements were performed in a vacuum prober with a cryogenic system.

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SUPPORTING INFORMATION

Details of $C_{\text{para1}}$ effect on capacitance measurement; Details of $C_{\text{para2}}$ effect on capacitance measurement; Details of analysis
on $R_{\text{access}}$ effect in capacitance measurement; Details of transmission line model in MoS$_2$ FET; Used parameters in the calculation; Transfer characteristics of back-gate WS$_2$ FET; Details of analysis on channel resistance effect in capacitance measurement; Detailed analyses of $C_{\text{G}}$-$C_{\text{G}}$ transition. This material is available free of charge via the Internet at http://pubs.acs.org.

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**Notes**

The authors declare no competing financial interests.

**REFERENCES**

1. Novoselov, K. S.; Jiang, D.; Schedin, F.; Booth, T. J.; Khotkevich, V. V.; Morozov, S. V.; Geim, A. K. Two-Dimensional Atomic Crystals. *Proc. Natl. Acad. Sci. U. S. A.* 2005, 102, 10451-10453.

2. Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-Layer MoS$_2$ Transistors. *Nat. Nanotechnol.* 2011, 6, 147-150.

3. Kim, S.; Konar, A.; Hwang, W. S.; Lee, J. H.; Lee, J.; Yang, J.; Jung, C.; Kim, H.; Yoo, J.; Choi, J.; Jin, Y. W.; Lee, S. Y.; Jena, D.; Choi, W.; Kim, K. High-Mobility and Low-Power Thin-Film Transistors Based on Multilayer MoS$_2$ Crystals. *Nature Commun.* 2012, 3, 1011.

4. Desai, S.; Madhvapathy, S.; Sachid, A.; Llinas, J.; Wang, Q.; Ahn, G.; Pitner, G.; Kim, M.; Bokor, J.; Hu, C.; Wong, H. S. P.; Javey, A. MoS$_2$ Transistors with 1-Nanometer Gate Lengths. *Science* 2016, 354, 99-102.

5. Zhu, W.; Low, T.; Lee, Y.; Wang, H.; Farmer, D.; Kong, J.; Xia, F.; Avouris, P. Electronic Transport and Device Prospects of Monolayer Molybdenum Disulphide Grown by Chemical Vapour Deposition. *Nature Commun.* 2014, 5, 3087.

6. Liu, H.; Neal, A. T.; Ye, P. D. Channel Length Scaling of MoS$_2$ MOSFETs. *ACS Nano* 2012, 6, 8563-8569.

7. Appenzeller, J.; Knoch, J.; Derycke, V.; Martel, R.; Wind, A.; Avouris, P. Field-Modulated Carrier Transport in Carbon Nanotube Transistors. *Phys. Rev. Lett.* 2002, 89, 126801.

8. Knoch, J.; Zhang, M.; Zhao, Q.; Lenk, S.; Mantl, S.; Appenzeller, J. Effective Schottky Barrier Lowering in Silicon-on-Insulator Schottky-Barrier Metal-Oxide-Semiconductor Field-Effect Transistors Using Dopant Segregation. *Appl. Phys. Lett.* 2005, 87, 263505.

9. Zhao, Y.; Candelab, D.; Delker, C.; Zi, Y.; Janes, D.; Appenzeller, J.; Yang, C. Understanding the Impact of Schottky Barriers on the Performance of Narrow Bandgap Nanowire Field Effect Transistors. *Nano Lett.* 2012, 12, 5331-5336.

10. Penumatcha, A.; Salazar, R.; Appenzeller, J. Analyzing Black Phosphorus Transistors Using an Analytic Schottky Barrier MOSFET Model. *Nat. Commun.* 2015, 6, 8948.

11. Das, S.; Chen, H.; Penumatcha, A.; Appenzeller, J. High Performance Multilayer MoS$_2$ Transistors with Scandium Contacts. *Nano Lett.* 2012, 13, 100-105.

12. Prakash, A.; Appenzeller, J. Bandgap Extraction and Device Analysis of Ionic Liquid Gated WSe$_2$ Schottky Barrier Transistors. *ACS Nano* 2017, 11, 1626-1632.

13. Wang, J.; Yao, Q.; Huang, C.; Zou, X.; Liao, L.; Chen, S.; Fan, Z.; Zhang, K.; Wu, W.; Xiao, X.; Jiang, C.; Wu, W. High Mobility MoS$_2$ Transistor With Low Schottky Barrier Contact by Using Atomic Thick h-BN as a Tunneling Layer. *Adv. Mater.* 2016, 28, 8302-8308.

14. Shih, C.; Wang, Q.; Son, Y.; Jin, Z.; Blankschtein, D.; Strano, M. Tuning on-off Current Ratio and Field-Effect Mobility in a MoS$_2$-Graphene Heterostructure via Schottky Barrier Modulation. *ACS Nano* 2014, 8, 5790-5798.

15. Kwon, J.; Lee, J. Y.; Yu, Y. J.; Lee, C. H.; Cui, X.; Hone, J.; Lee, G. H. Thickness-Dependent Schottky Barrier Height of MoS$_2$ Field-Effect Transistors. *Nanoscale* 2017, 9, 6151-6157.

16. Xu, K.; Wang, Z.; Wang, F.; Huang, Y.; Wang, F.; Yin, L.; Jiang, C.; He, J. Ultrasensitive Phototransistors Based on Few-Layered HfS$_2$. *Adv. Mater.* 2015, 27, 7881-7887.

17. Kang, M.; Rathi, S.; Lee, I.; Li, L.; Khan, M.; Lim, D.; Lee, Y.; Park, J.; Yun, S.; Youn, D.; Jun, C.; Kim, G. Tunable Electrical Properties of Multilayer HfSe$_2$ Field Effect Transistors by Oxygen Plasma Treatment. *Nanoscale* 2017, 9, 1645-1652.

18. Zhang, Y.; Li, H.; Wang, H.; Xie, H.; Liu, R.; Zhang, S.; Qiu, Z. Thickness Considerations of Two-Dimensional Layered Semiconductors for Transistor Applications. *Sci. Rep.* 2016, 6, 29561.

19. Bao, W.; Cai, X.; Kim, D.; Sridhara, K.; Fuhrer, M. High Mobility Ambipolar MoS$_2$ Field-Effect Transistors: Substrate and Dielectric Effects. *Appl. Phys. Lett.* 2013, 102, 042104.

20. Abderrahmane, A.; Ko, P.; Thu, T.; Ishizawa, S.; Takamura, T.; Sandhu, A. High Photosensitivity Few-Layered MoSe$_2$ Back-Gated Field-Effect Phototransistors. *Nanotechnology* 2014, 25, 365202.

21. Xu, H.; Fathipour, S.; Kinder, E. W.; Seabaugh, A. C.; Fullerton-Shirey, S. K. Reconfigurable Ion Gating of 2H-MoTe$_2$: Field-Effect Transistors using Poly(ethylene oxide)-CsClO$_4$ Solid Polymer Electrolyte. *ACS Nano* 2015, 9, 4900-4910.

22. Luo, W.; Zhu, M.; Peng, G.; Zheng, X.; Miao, F.; Bai, S.; Zhang, X.; Qin, S. Carrier Modulation of Ambipolar Few-Layer MoTe$_2$ Transistors by MgO Surface Charge Transfer Doping. *Adv. Funct. Mater.* 2017, 28, 1704539.

23. Ciarrocchi, A.; Avsar, A.; Ovchinnikov, D.; Kis, A. Thickness-Modulated Metal-to-Semiconductor Transformation in a Transition Metal Dichalcogenide. *Nature Commun.* 2018, 9, 919.

24. Zhao, Y.; Qiao, J.; Yu, P.; Hu, Z.; Lin, Z.; Lau, S. P.; Liu, Z.; Ji, W.; Chai, Y. Extraordinarily Strong Interlayer Interaction in 2D Layered PtS$_2$. *Adv. Mater.* 2016, 28, 2399-2407.

25. Zhao, Y.; Qiao, J.; Yu, Z.; Yu, P.; Xu, K.; Lau, S.; Zhou, W.; Liu, Z.; Wang, X.; Ji, W.; Chai, Y. High-Electron-Mobility and Air-Stable 2D Layered PtSe$_2$ FETs. *Adv. Mater.* 2017, 29, 5.

26. Baek, I.; Baek, I.; Pyeon, J.; Song, Y.; Chung, T.; Kim, H.; Baek, S.; Kim, J.; Kang, C.; Choi, J.; Hwang, C.; Han, J.; Kim, S. Synthesis of SnS Thin Films by Atomic Layer Deposition at Low Temperatures. *Chem. Mater.* 2017, 29, 8100-8110.

27. Choi, H.; Lee, J.; Shin, S.; Lee, J.; Lee, S.; Park, H.; Kwon, S.; Lee, N.; Bang, M.; Lee, S.; Jeon, H. Fabrication of High
Crystalline SnS and SnS₂ Thin Films, and Their Switching Device Characteristics. Nanotechnology 2018, 29, 215201.
28. Sucharitkul, S.; Rajesh Kumar, U.; Sankar, R.; Chou, F.; Chen, Y.; Wang, C.; He, C.; He, R.; Gao, X. Screening Limited Switching Performance of Multilayer 2D Semiconductor FETs: the Case for SnS. Nanoscale 2016, 8, 19050-19057.
29. Xu, X.; Song, Q.; Wang, H.; Li, P.; Zhang, K.; Wang, Y.; Yuan, K.; Yang, Z.; Ye, Y.; Dai, L. In-plane Anisotropies of Polarized Raman Response and Electrical Conductivity in Layered Tin Selenide. ACS Appl. Mater. Interfaces 2017, 9, 12601-12607.
30. Pradhan, N.; Rhodes, D.; Memaran, S.; Pourmiroj, J.; Smirnov, D.; Talapatra, S.; Feng, S.; Perea-Lopez, N.; Elias, A.; Terrones, M.; Ajayan, P.M.; Balicas, L. Hall and Field Effect Mobilities in Few Layered P-WSe₂ Field-Effect Transistors. Sci. Rep. 2015, 5, 8979.
31. Zhou, C.; Zhao, Y.; Raju, S.; Wang, Y.; Lin, Z.; Chan, M.; Chai, Y. Carrier Type Control of WSe₂ Field-Effect Transistors by Thickness Modulation and MoO₃ Layer Doping. Adv. Funct. Mater. 2016, 26, 4223-4230.
32. Yang, Z.; Liu, X.; Zou, X.; Wang, J.; Ma, C.; Jiang, C.; Ho, J.; Pan, C.; Xiao, X.; Xiong, J.; Liao L. Performance Limits of the Self-Aligned Nanowire Top-Gated MoS₂ Transistors. Adv. Funct. Mater. 2016, 26, 1602250.
33. Fang, N.; Nagashio, K. Band Tail Interface States and Quantum Capacitance in a Monolayer Molybdenum Disulfide Field-Effect-Transistor. J. Phys. D 2018, 51, 065110.
34. Shan, Y.; Ashok, S.; Fonash, S. J. Unipolar Accumulation-Type Transistor Configuration Implemented using Si Nanowires. Appl. Phys. Lett. 2007, 91, 093518.
35. Schroder, D. K. Semiconductor Material and Device Characterization, 3rd ed.; John Wiley & Sons: New York, 2006.
36. Nicollian, E. H.; Brews, J. R. MOS Physics and Technology; Wiley: New York, 1982.
37. Martens, K.; Chui, C.; Brammertz, G.; De Jaeger, B.; Kuzum, D.; Meuris, M.; Heyns, M.; Krishnamohan, T.; Saraswat, K.; Maes, H.; Groeseneken, G. On The Correct Extraction of Interface Trap Density of MOS Devices with High-Mobility Semiconductor Substrates. IEEE Trans. Electron Devices 2008, 55, 547-556.
38. Takenaka, M.; Ozawa, Y.; Han, J.; Takagi, S. Quantitative Evaluation of Energy Distribution of Interface Trap Density at MoS₂ MOS Interfaces by The Terman Method. International Electron Devices Meeting (IEDM) Tech. Dig. 2016, 5-8.
39. Zhao, P.; Azcatl, A.; Gomieniu, Y.; Bolshakov, P.; Schmidt, M.; McDonnell, S.; Hinkle, C.; Hurley, P.; Wallace, R.; Young, C. Probing Interface Defects in Top-Gated MoS₂ Transistors with Impedance Spectroscopy. ACS Appl. Mater. Interfaces 2017, 9, 24348-24356.
40. Michailow, W.; Schülein, F.; Möller, B.; Preciado, E.; Nguyen, A.; von Son, G.; Mann, J.; Hörner, A.; Wixforth, A.; Bartels, L.; Krenner, H. Combined Electrical Transport and Capacitance Spectroscopy of a MoS₂-LiNbO₃ Field Effect Transistor. Appl. Phys. Lett. 2017, 110, 023505.
41. Bae, H.; Kim, C.; Choi, Y. Characterization of Intrinsic Subgap Density-of-States in Exfoliated MoS₂ FETs Using a Multi-Frequency Capacitance-Conductance Technique. AIP Adv. 2017, 7, 075304.
42. Li, S.; Wakabayashi, K.; Xu, Y.; Nakaharai, S.; Komatsu, K.; Li, W.; Lin, Y.; Aparecido-Ferreira, A.; Tsukagoshi, K. Thickness-Dependent Interfacial Coulomb Scattering in Atomically Thin Field-Effect Transistors. Nano Lett. 2013, 13, 3546-3552.
43. Yu, Z.; Ong, Z.; Li, S.; Xu, J.; Zhang, G.; Zhang, Y.; Shi, Y.; Wang, X. Analyzing the Carrier Mobility in Transition-Metal Dichalcogenide MoS₂ Field-Effect Transistors. Adv. Funct. Mater. 2017, 27, 1604093.
44. Yu, Z.; Pan, Y.; Shen, Y.; Wang, Z.; Ong, Z.; Xu, T.; Xin, R.; Pan, L.; Wang, B.; Sun, L.; Wang, J.; Zhang, G.; Zhang, Y.; Shi, Y.; Wang, X. Towards Intrinsic Charge Transport in Monolayer Molybdenum Disulfide by Defect and Interface Engineering. Nature Commun. 2014, 5, 5290.
45. Stern, F. Quantum Properties of Surface Apathe-Charge Layers. Crit. Rev. Solid State Mater. Sci. 1973, 4, 499.
46. Colinge, J.; Flandre, D.; Van de Wiele, F. Subthreshold Slope of Long-Channel, Accumulation-Mode P-Channel SOI MOSFETs. Solid-State Electronics 1994, 37, 289-294.
47. Fuhrer, M. S.; Hone, J. Measurement of Mobility in Dual-Gated MoS₂ Transistors. Nature Nanotechnol. 2013, 8, 146.
48. Luryi, S. Quantum Capacitance Devices. Appl. Phys. Lett. 1988, 52, 501-503.
49. Ma, N.; Jena, D. Carrier Statistics and Quantum Capacitance Effects on Mobility Extraction in Two-dimensional Crystal Semiconductor Field-Effect Transistors. 2D Materials 2015, 2, 015003.
50. Shockley, W.; Read, W. Statistics of the Recombinations of Holes and Electrons. Phys. Rev. 1952, 87, 835-842.
51. Chow, P.; Wang, K. L. A New AC Technique for Accurate Determination of Channel Charge and Mobility in Very Thin Gate MOSFETs. IEEE Trans. Electron Devices 1986, 33, 1299-1304.
52. Haddara, H.; El-Sayed, M. Conductance Technique in MOSFETs: Study of Interface Trap Properties in the Depletion and Weak Inversion Regimes. Solid-State Electronics 1988, 31, 1289-1298.
53. Brammertz, G.; Martens, K.; Sioncke, S.; Delabie, A.; Caymax, M.; Meuris, M.; Heyns, M. Characteristic Trapping Lifetime and Capacitance-Voltage Measurements of GaAs Metal-Oxide-Semiconductor Structures. Appl. Phys. Lett. 2007, 91, 133510.
54. Shin, B.; Han, G.; Yun, S.; Oh, H.; Bae, J.; Song, Y.; Park, C.; Lee, Y. Indirect Bandgap Puddles in Monolayer MoS₂ by Substrate-Induced Local Strain. Adv. Mater. 2016, 28, 9378-9384.
55. Uwanno, T.; Taniguchi, T.; Watanabe, K.; Nagashio, K. Electrically Inert h-BN/Bilayer Graphene Interface in All-2D-Heterostructure FETs. ACS Appl. Mater. Interfaces 2018.
56. Cheiwchanchamnangij, T.; Lambrecht, W. R. Quasiparticle Band Structure Calculation of Monolayer, Bilayer, and Bulk MoS₂. Phys. Rev. B 2012, 85, 205302.
57. Chen, X.; Wu, Z.; Xu, S.; Wang, L.; Huang, R.; Han, Y.; Ye, W.; Xiong, W.; Han, T.; Long, G.; Wang, Y.; He, Y.; Cai, Y.; Sheng, P.; Wang, N. Probing the Electron States and Metal-Insulator Transition Mechanisms in Molybdenum Disulphide Vertical Heterostructures. Nature Commun. 2015, 6, 6088.
58. Qiu, H.; Xu, T.; Wang, Z.; Ren, W.; Nan, H.; Ni, Z.; Chen, Q.; Yuan, S.; Miao, F.; Song, F.; Long, G.; Shi, Y.; Sun, L.; Wang, J.; Wang, X. Hopping Transport Through Defect
Induced Localized States in Molybdenum Disulphide. *Nature Commun.* **2013**, *4*, 2642.

59. Fang, N.; Nagashio, K.; Toriumi, A. Subthreshold Transport in Mono- and Multilayered MoS$_2$ FETs. *Appl. Phys. Express* **2015**, *8*, 065203.

60. Fang, N.; Nagashio, K.; Toriumi, A. Experimental Detection of Active Defects in Few Layers MoS$_2$ through Random Telegraphic Signals Analysis Observed in its FET Characteristics. *2D Materials* **2016**, *4*, 015035.

61. Lindefelt, U. Doping-Induced Band Edge Displacements and Band Gap Narrowing in 3C-, 4H-, 6H-SiC, and Si. *J. Appl. Phys.* **1998**, *84*, 2628-2637.

62. Kramer, B.; MacKinnon, A. Localization: Theory and Experiment. *Rep. Prog. Phys.* **1993**, *56*, 1469-1564.

63. Takahashi, N.; Nagashio, K. Buffer Layer Engineering on Graphene via Various Oxidation Methods for Atomic Layer Deposition. *Appl. Phys. Express* **2016**, *9*, 125101.

64. Kurabayashi, S.; Nagashio, K. Transport Properties of the Top and Bottom Surfaces in Monolayer MoS$_2$ Grown by Chemical Vapor Deposition. *Nanoscale* **2017**, *9*, 13264-13271.

65. Braga, D.; Gutiérrez, I.; Berger, H.; Morpurgo, A. Quantitative Determination of the Band Gap of WS$_2$ with Ambipolar Ionic Liquid-Gated Transistors. *Nano Lett.* **2012**, *12*, 5218-5223.
Supporting Information.

Accumulation-mode two-dimensional field-effect transistor: Operation mechanism and thickness scaling rule

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**Supplementary Figure S1.** (a) Full equivalent circuit to show $C_{\text{para}1}$. (b) The configuration of capacitance measurement. Source is connected to low-terminal and drain is floating. Top gate is connected to high-terminal. This configuration combined with $n^+\text{-Si}/\text{SiO}_2$ substrate introduce large frequency dispersion ($>C_{\text{ox}}$) in (c) $C$-$V$ and (d) corresponding peaks in conductance-frequency ($G_p/\omega$-$f$) measurement. It should be noted that these peaks are not related with the interface traps.
**Supplementary Figure S2.** (a) Full equivalent circuit to show $C_{para2}$. (b) The configuration of capacitance measurement. Both source and drain are connected to low-terminal and top gate is connected to high-terminal. Under this configuration, $C_{para1}$ can be suppressed even on $n^+\text{-Si/SiO}_2$ substrate. However, $C_{para2}$ still induces large baseline shift in $C-V$, which cannot be removed as shown in (c). By fabricating MoS$_2$ FET on quartz substrate, all the parasitic capacitance is totally removed.
Supplementary Figure S3. (a) Simplified equivalent parallel circuit to study \( R_{\text{access}} \) effect. (b) Maximum \( C_{\text{para}} \) at 1 MHz/\( C_{\text{ox}} \) as a function of \( R_{\text{access}} \). (c,d) Experimental and simulated \( C_{\text{total}}-V_{\text{ TG}} \) characteristics of MoS\(_2\) FET with different \( R_{\text{access}} \). The decrease in Maximum \( C_{\text{para}} \) at 1 MHz is clearly observed in (d) due to high \( R_{\text{access}} \approx 1000 \, \text{kΩ} \).
Supplementary Figure S4. (a) Transmission line equivalent circuit of MoS$_2$ FET. This equivalent circuit is valid when the whole channel of MoS$_2$ is depleted. (b,c,d) Calculated plot of $C_{\text{total}}$-$V_{TG}$ curves without $C_{\text{it}}$ at different $\mu$ and $L$. Although frequency dispersion is observed, experimental $C_{\text{total}}$-$V_{TG}$ curves in Figure 3b of the main text cannot be reproduced without band tail shape $C_{\text{it}}$. 
Supplementary Figure S5. (a) $C_Q$, $C_{it}$ and $C_{ox}$ used in monolayer MoS$_2$ $I$-$V$ and $C$-$V$ simulation. $C_{ox}$ is experimentally extracted from $C_{total}$ at strong accumulation region. $C_Q$ is theoretically calculated. $C_{it}$ and drift mobility are extracted from $I$-$V$ fitting.$^1$ Drift mobility is slightly higher than conventional experimentally extracted field-effect mobility due to reduced carrier controllability of the gate by $C_{it}$. But field-effect mobility extraction is still one of the fastest way to study carrier transport properties. Drift mobility $\mu$ is assumed to be independent of $E_F$ with a constant value for simplicity. Here for studied monolayer MoS$_2$, $\mu = 2.2$ cm$^2$V$^{-1}$s$^{-1}$. This is a rough assumption because $\mu$ is usually dependent on carrier density through screening effect. But the dominant factor in determining $I_{DS}$ is the carrier density instead of the drift mobility especially at subthreshold region. This explains why we can give a good $I$-$V$ fitting even at constant $\mu$ condition. (b) Experimental and calculated $\sigma$-$V_TG$ curve of monolayer MoS$_2$ FET. Red dot is experimental result and solid black line is simulated result by using parameters in (a). (c) $C_{Q/D}$, $C_{it}$ and $C_{ox}$ used in 16 nm-thick MoS$_2$ FET $I$-$V$ and $C$-$V$ simulation. Here for studied 16 nm-thick MoS$_2$, $\mu = 60$ cm$^2$V$^{-1}$s$^{-1}$. 
Supplementary Figure S6. (a) Schematic diagram of the device. (b) Transfer characteristics of back-gate WSe$_2$ FET with different channel thickness.
Note S1. Access resistance effect on capacitance measurement.

$R_{\text{access}}$ can cause error in measured capacitance. $R_{\text{access}}$ effect is simulated based on equivalent parallel circuit and other resistance effect is not included in this simulation as shown in Supplementary Figure S3a. Here, $C_{\text{ideal}}$ is defined as ideal $C-V$ in monolayer MoS$_2$ without $C_t$. Change of $C_{Q/D}$ will not affect the conclusion in $R_{\text{access}}$ simulation. $C_{ox}$ is given as 0.3 μF/cm$^2$ with 10×10 μm$^2$ area. Equivalent parallel capacitance is shown as follows:

$$C_{\text{Para}} = C_{\text{ideal}} \left(1 + \frac{\omega^2 C_{\text{ideal}}^2 R_{\text{access}}^2}{\omega^2 R_{\text{access}}^2} \right).$$  \hspace{1cm} (1)

As we can see in Supplementary Figure S3c,d, the large error occurs in the accumulation region of $C-V$. Experimentally, access resistance can be extracted by Cole-Cole plot at accumulation region where other resistance is shunted. Maximum $C_{\text{para}}$ at 1 MHz remains to $C_{ox}$ when $R_{\text{access}} = 10^4$ Ω and decrease when $R_{\text{access}} = 2 \times 10^5$ Ω. So maximum $C_{\text{para}}$ at 1 MHz/$C_{ox}$ is the good parameter to indicate $R_{\text{access}}$ effect. This parameter equals to 1 when $R_{\text{access}}$ can be neglected at measured frequency range and decrease when $R_{\text{access}}$ limit the measured capacitance as shown in Supplementary Figure S3b.

Note S2. MoS$_2$ Channel resistance effect on capacitance measurement.

Transmission line model has been applied to study channel resistance effect on $C-V$ for Si MOSFET.$^{2,3}$ Here, transmission line model will also be used in MoS$_2$ FET to model $R_{\text{channel}}$ effect (Supplementary Figure S4). Notice that substrate is insulating in MoS$_2$ FET, which simplifies the mathematical expressions of equivalent circuit by neglecting charge supply from the substrate. Assume that all variables are in phasor quantities. $v_0$ refers to small ac variation. $R_{S,\text{channel}}$ refers to sheet resistance of $R_{\text{channel}}$. $i$ refers to current from one side (source or drain) of the electrode. So the total current from both sides $i_{D,S}$ is 2×$i$.

Firstly,

$$\frac{dv}{dx} = -\frac{R_{S,\text{channel}}}{W} i,$$  \hspace{1cm} (2)

$$\frac{di}{dx} = j\omega C_1 W (v_0 - v).$$  \hspace{1cm} (3)

Differentiating eq. 2 with respect to x and substituting it into eq. 3,

$$\frac{dv^2}{dx^2} = -j\omega C_1 R_{S,\text{channel}} (v_0 - v)$$  \hspace{1cm} (4)

Assume $u = v - v_0$, we have:

$$\frac{du^2}{dx^2} = \gamma^2 u,$$  \hspace{1cm} (5)

where $\gamma = \sqrt{R_{S,\text{channel}} / \omega C_1}$.

The solution of this eq. 5 is

$$u = Ae^{-\gamma x} + Be^{\gamma x}$$  \hspace{1cm} (6)
Based on the boundary conditions,
\[ v = 0 \text{ when } x = 0 \quad \text{and} \quad \frac{dv}{dx} = 0 \text{ when } x = \frac{L}{2}, \]
we have:
\[ A = \frac{V_0}{e^{-\gamma L} + 1}, \quad B = -\frac{e^{-\gamma L}V_0}{e^{-\gamma L} + 1}. \] (7)

Based on eq. 2 at \( x = 0 \), source/drain current:
\[ i_{DS} = 2i = -\frac{2W}{R_{S, \text{channel}}} \frac{dv}{dx} = LWj\omega C_V V_0 \frac{\tanh \frac{L}{2}}{L}. \] (8)

The propagation constant \( \lambda \) and channel resistance limited time constant \( \tau_{Rch} \) are given as below:
\[ \lambda = \frac{L}{2} = \sqrt{j\omega \tau_{Rch}}, \quad \tau_{Rch} = \frac{C_V R_{S, \text{channel}} L^2}{4}. \] (9)

So the experimental measured equivalent parallel capacitance and conductance \( C_{\text{total}} \) and \( G_{\text{total}} \) are:
\[ C_{\text{total}} = C_V \text{ Re} \left[ \frac{\tanh \frac{\lambda}{\lambda}}{\lambda} \right], \quad G_{\text{total}} = -C_V \text{ Im} \left[ \frac{\tanh \frac{\lambda}{\lambda}}{\lambda} \right]. \] (10)

Note S3. \( C_{D-C_Q} \) transition.
Classical depletion capacitance (accumulation capacitance) expression of MoS\(_2\) is given below by neglecting holes,\(^4\)
\[ C_{D(A)} = \frac{\varepsilon_{\text{MoS}_2}}{\sqrt{2L_D}} \frac{\exp(\nu S) - 1}{k_B T} \left\{ \frac{\exp(\nu S) - \nu S}{k_B T} - 1 \right\}. \] (11)

Notice that often used \( E_F \) in monolayer MoS\(_2\) discussion is unsuitable in multilayer and bulk MoS\(_2\) since potential \( \psi \) changes from surface to body. Instead, surface potential \( \psi_S \) is used.

By neglecting free carriers in the depletion region, the depletion layer width is shown as:
\[ W_D = \sqrt{\frac{2\varepsilon_{\text{MoS}_2} \nu_S}{eN_P}}. \] (12)

As for bulk MoS\(_2\) (Thickness > 55 nm), \( W_{Dm}\) is obtained when \( \nu_S \) saturates at strong inversion region. While for multilayer MoS\(_2\) (Thickness < 35 nm), transition from depletion capacitance to quantum capacitance occurs when \( W_D \) reaches MoS\(_2\) body thickness. Transition condition of \( \psi_S \) is given as below:
\[ \psi_{S(D\rightarrow Q)} = \frac{eN_D t_{\text{MoS}_2}^2}{2\varepsilon_{\text{MoS}_2}}. \] (13)

Thickness of MoS\(_2\) is defined as \( t_{\text{MoS}_2}\). Quantum capacitance is calculated based on Poisson equation
and boundary conditions. The potential distribution is firstly calculated. Parabolic function is used due to Poisson equation as shown:

$$\psi_x = C_0 + C_1 z + C_2 z^2.$$  \hspace{1cm} (14)

One dimension Poisson equation is given as below:

$$\frac{d^2 \psi_z}{dz^2} = -\frac{eN_D}{\varepsilon_{MoS_2}} = A.$$ \hspace{1cm} (15)

Two boundary conditions are given below:

(1) Potential at surface (z=0) is $\psi_S$.

$$\psi_z \big|_{z=0} = \psi_S.$$ \hspace{1cm} (16)

(2) The electric field at $z=t_{MoS_2}$ is approximately zero, which is due to insulating quartz substrate.\textsuperscript{5}

$$\frac{d\psi_z}{dz} \bigg|_{z=t_{MoS_2}} = 0.$$ \hspace{1cm} (17)

This condition is the intrinsic condition for present 2D-FET structure, where channel is always surrounded by the insulator or environment and is important for obtaining $C_Q$ dominant region. Either additional making metal contact to MoS$_2$ such as capacitor structure or $t_{MoS_2}>W_{Dm}$ will degrade this condition to conventionally used one, that is $\psi_x=0$.

Using eq. 14-17, potential distribution is obtained as

$$\psi_z = \frac{Az^2}{2} - At_{MoS_2} z + \psi_S = f(z) + \psi_S.$$ \hspace{1cm} (18)

Then free electron statistics is calculated. Free electron density per unit volume at position $z$ is written as

$$n(z) = N_D \exp\left( \frac{e\psi_z}{k_BT} \right).$$ \hspace{1cm} (19)

By integrating eq. 19 with $z$ from 0 to $t_{MoS_2}$, and replacing $\psi_z$ with eq. 18, we get total channel free electron per unit area as:

$$n_{ch} = N_D \exp\left( \frac{e\psi_S}{k_BT} \right) \int_0^{t_{MoS_2}} \exp\left( \frac{ef(z)}{k_BT} \right) dz.$$ \hspace{1cm} (20)

Quantum capacitance is calculated from the definition $C_Q = \frac{dn_{ch}}{d\psi_x}$, which is given as below:

$$C_Q = \frac{eN_D}{k_BT} = N_Q \exp\left( \frac{e\psi_S}{k_BT} \right),$$ \hspace{0.5cm} where constant \hspace{0.5cm} $$N_Q = \frac{\int_0^{t_{MoS_2}} \exp\left( \frac{ef(z)}{k_BT} \right) dz}{k_BT}.$$ \hspace{1cm} (21)

To simplify the calculation of $N_Q$, capacitance continuity condition is finally used. That is
\[ C_D = C_Q \left| \psi_S = \psi_{S(D \rightarrow Q)} \right. \]  

(22)

Capacitance in multilayer MoS\(_2\) (C\(_{\text{MoS}_2}\)) is given by two piece-wise functions combined with eq. 11,13,21,22,

\[ C_{\text{MoS}_2} = \begin{cases} 
C_D & \psi_{D \rightarrow Q} \\
C_Q & \psi_{Q \rightarrow D} \end{cases} \]  

(23)

REFERENCES

1. Fang, N.; Nagashio, K. Band Tail Interface States and Quantum Capacitance in a Monolayer Molybdenum Disulfide Field-Effect-Transistor. *J. Phys. D* 2018, 51, 065110.
2. Chow, P.; Wang, K. L. A New AC Technique for Accurate Determination of Channel Charge and Mobility in Very Thin Gate MOSFET’s. *IEEE Trans. Electron Devices* 1986, 33, 1299-1304.
3. Haddara, H.; El-Sayed, M. Conductance Technique in MOSFETs: Study of Interface Trap Properties in the Depletion and Weak Inversion Regimes. *Solid-State Electronics* 1988, 31, 1289-1298.
4. Nicollian, E. H.; Brews, J. R. *MOS Physics and Technology*; Wiley: New York, 1982.
5. Yan, R.; Ourmazd, A.; Lee, K. Scaling the Si MOSFET: from Bulk to SOI to Bulk. *IEEE Trans. Electron Devices* 1992, 39, 1704-1710.