Hardware Acceleration of Sampling Algorithms in Sample and Aggregate Graph Neural Networks

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Abstract—Sampling is an important process in many GNN structures in order to train larger datasets with a smaller computational complexity. However, compared to other processes in GNN (such as aggregate, backward propagation), the sampling process still costs tremendous time, which limits the speed of training. To reduce the time of sampling, hardware acceleration is an ideal choice. However, state of the art GNN acceleration proposal did not specify how to accelerate the sampling process. What’s more, directly accelerating traditional sampling algorithms will make the structure of the accelerator very complicated.

In this work, we made two contributions: (1) Proposed a new neighbor sampler: CONCAT Sampler, which can be easily accelerated on hardware level while guaranteeing the test accuracy. (2) Designed a CONCAT-sampler-accelerator based on FPGA, with which the neighbor sampling process boosted to about 300-1000 times faster compared to the sampling process without it.

Index Terms—GNN, sampling, hardware acceleration, FPGA

I. INTRODUCTION

Graph neural networks show excellent practicability in various situations, such as social networks, protein molecule structure prediction, citation networks and so on. Among various graph neural networks, some of them[1][2][3][4][5] gather full graph information (such as Graph Laplacian) to learn parameters, which are limited by the fixed graph data structure and cannot be quickly applied to the ever-changing graph structure. Inductive representation neural networks[6][7] can solve this problem, which can be applied to rapidly changing data structures and shows high accuracy. At the same time, their various structures can be applied to different kinds of datasets, which have great practical value.

Another advantage of inductive representation neural networks is that they can gather graph local information very well. By aggregating local information from nodes’ neighborhood, these networks avoid directly computing whole graph Laplacian, which can reduce computational complexity. In order to reduce computational complexity more, the sampling process was proposed. By sampling a given number of neighbor nodes and only aggregating their information while training, sample-aggregate networks can make it possible to train very large graph at a relatively low cost while guaranteeing test accuracy. However, compared to other processes of GNN, sampling process still consumes much time and computing resources, especially on large datasets. For example, if we train Reddit dataset with traditional GraphSAGE network 1, we will find that the sampling process takes more than 100 times longer than other GNN processes like aggregate, update, and so on. This is because the traditional sampling process requires frequent access to the dataset and its edge index. Therefore, hardware acceleration for the sampling process is necessary.

Currently, there are several hardware acceleration proposals for GNN. For example, HyGCN[9] proposed a hardware accelerator using an aggregation engine and a combination engine to exploit various parallelism and reuse highly reusable data efficiency. At the same time, AWB-GCN[10] was proposed to monitor the sparse graph pattern and adjust the workload distribution among a large number of processing elements; GCNAX[11] optimized dataflow for GCNs that simultaneously improves resource utilization and reduces data movement; However, except HyGCN, these accelerators did not contain a module that accelerates sampling process. Even though HyGCN contains a sampling module, it did not show how it works in a detailed way and the performance of the sampling accelerator. Therefore, we decided to design a novel sampling accelerator, it should be simple, yet performs well.

There are several state-of-the-art sampling algorithms that can guarantee test accuracy well, like GraphSAGE traditional stochastic sampler[6], GraphSAINT sampler[7], adaptive sampler[12] and so on. However, if we want to accelerate...
these processes with hardware, the structure of hardware may be very complicated (see section IV). Therefore, a new sampling algorithm is needed in order to reduce the complexity of the hardware accelerator.

In this work, we propose a novel sampling algorithm, CONCAT (CONCATenate) sampler, which creatively concatenates low-level-sample-graph into higher-depth-sample-graph, making it easier to be accelerated with hardware (FPGA) while ensuring the test accuracy. We also designed a hardware accelerator for CONCAT sampler, with which the sampling process can be boosted to about 300-1000 times (see section V-B) compared to the traditional only-software process.

II. BACKGROUND AND RELATED WORK
A. Notations and Definitions
Here we recap some basic concepts of Graph. Notations and their explanations are listed below. We also want to clarify the difference between $K$-neighborhood and $K$-hop neighborhood. In this paper, we refer $K$-neighborhood as a set of neighbor nodes $v_j$ with $\text{dist}(v_i, v_j) \leq K$, and refer $K$-hop neighborhood as a set of neighbor nodes $v_j$ with $\text{dist}(v_i, v_j) = K$.

| Notation | Definition |
|----------|------------|
| $V$ | (undirected) graph |
| $\mathcal{V}$ | set of nodes in graph $G$ |
| $\mathcal{E}$ | set of edges in graph $G$ |
| $A$ | adjacency matrix of graph $G$ |
| $L$ | Laplacian matrix of graph $G$ |
| $v_i$ | nodes of graph $v_i \in \mathcal{V}$ |
| $d_{v_i}$ | degree of node $v_i$ |
| $h_{v_i}$ | feature vector of node $v_i$ |
| $x$ | feature matrix of graph (composed by feature vectors) |
| $\text{dist}(v_i, v_j)$ | distance between node $v_i$ and node $v_j$ |
| $N_{K}(v_i)$ | $K$-neighborhood $N_{K}(v_i) = \{v_j \in \mathcal{V} | \text{dist}(v_i, v_j) \leq K\}$ |
| $S_{K}(v_i)$ | Sampling subset of $N_{K}(v_i)$ |
| $N_{K}^{\prime}(v_i)$ | $K$-hop neighborhood $N_{K}^{\prime}(v_i) = \{v_j \in \mathcal{V} | \text{dist}(v_i, v_j) = K\}$ |
| $S_{K}^{\prime}(v_i)$ | Sampling subset of $N_{K}^{\prime}(v_i)$ |
| $G_{v_i, K}$ | $K$-computational graph of node $v_i$ with $v_j \in N_{K}(v_i)$ |

For sampled nodes from the dataset, their basic information is required, including node degree and neighbor nodes. We use a column of serial data to represent each node’s degree, as shown in Fig. 2, we call it "degree list". They are stored in RAM, using node IDs as their corresponding offset address.

Meanwhile, we use “edge index” to represent neighborhood information from each node, in which the first column represents start node ID and the second column represents end node ID. They are sorted according to start node’s ID number. As a matter of fact, in sampling process, we only need to store second column, as they are sorted in order and we can locate them via node ID and degree information. Therefore, we only store the second column in RAM and called them "edge list", as shown in Fig. 2.

B. GNN models
Here we will introduce the basic information of some GNN models.

1) Graph Convolutional Network (GCN): Graph Convolutional Network is one of the most classical graph neural networks which successfully applies convolutional network on graph learning.[5][13]. Its inference model can be described as:

$$ a_v^{(k)} = \sum_{u \in N_v} h_u \frac{1}{\sqrt{d_u d_v}} $$

$$ h_v^{(k+1)} = \text{ReLU}(W^k a_v^{(k)} + b^k) $$(1)

2) GraphSAGE: Based on GCN, GraphSAGE adopted a sampling process in training in order to alleviate the exponential growth of computational complexity on large datasets when using GCN[6]. In GraphSAGE, the forward propagation process can be described as:

$$ a_v^{(k)} = \sum_{u \in S_v \cup \{v\}} h_u \frac{1}{n} $$

$$ h_v^{(k+1)} = \text{ReLU}(W^k a_v^{(k)} + b^k) $$(2)

Where $n$ is the number of nodes sampled from $v_i$’s neighborhood. In this work, we mainly focus on GraphSAGE model. Our proposed sampling algorithm and hardware acceleration are applied and tested based on GraphSAGE model.

In fact, GCN and GraphSAGE can be described in a uniform equation[11]:

$$ X^{(k+1)} = \sigma \left( \hat{A} X^{(k)} W^{(k)} \right) $$

For GCN, $\hat{A} = D^{-\frac{1}{2}} (A + I) D^{-\frac{1}{2}}$. For GraphSAGE, $\hat{A}$ denotes adjacency matrix of sampled nodes with a scaling factor of 1/n.

C. Neighbor Sampling methods
Before our work, there are several neighbor sampling methods proposed. Here we want to introduce two of them that have relationship with our work

1) Stochastic (Random) Sampler: Traditional Stochastic (Random) Sampler[6] samples neighbor nodes with uniform distribution, which means the possibility that a node being sampled is $1/n$, where $n$ is the number of nodes in the neighborhood, like Fig.3 shown.

2) Importance Sampler: Importance Sampler is firstly proposed in FastGCN[14]. In Importance Sampler, it assumes that every node has the same distribution $q$, and samples neighbor nodes according to $q$. In fact, the Stochastic Sampler is a special case of Importance Sampler. In Stochastic Sampler, every node has uniform distribution, which means $q \sim U[0, 1]$.

All of these samplers presented impressive performance and reduced the cost of training GNNs, which makes it possible to train very large graphs. However, from our perspective, if we want to accelerate the sampling process via FPGA, more considerations are needed. For example, if we sample nodes in n-neighborhood ($n > 1$), the sampled edge list will be stored in RAM, and the sampler will sample in n-hop neighborhood according to the sample result in (n-1)-hop-neighborhood. The constant access to edge list (which means constant access to RAM) will cause the hardware structure very complicated,
and the limited space of on-chip memory will restrict the performance of the accelerator on large datasets. Therefore, we need to design a new sampler, which can cater to small on-chip memory space even in large datasets. At the same time, the test accuracy shouldn’t be reduced a lot.

III. PROPOSED A NEW SAMPLER: CONCAT SAMPLER

In order to solve the problems mentioned above, we proposed a novel yet effective sampler—CONCATenate (CONCAT) sampler. In CONCAT sampler, neighbors are sampled following the way below:

1) Sample in 1-neighborhood to generate the original computational graphs \( G_{v,1} \);
2) Concatenate the sample result into the original computational graphs;
3) Generate 2-neighborhood computational graphs \( G_{v,2} \);
4) Iterate the sample methods above to get a k-neighborhood computational graphs \( G_{v,K} \).

To be more specific, we can compare CONCAT sampler with the traditional sampler, like GraphSAGE stochastic sampler, as Fig. 3 shown. If we sample 2 neighbor nodes for each node and search in depth \( K = 2 \), we can generate computational graphs for each node. We will find in each computational graph, every node is sampled independently. For example, in node 1 and 4’s computational graph, node 5 are sampled, however, the neighbor nodes that are sampled from node 5 are totally different (node 17, 4, and node 15, 16). Different from the traditional samplers, CONCAT sampler samples neighbor nodes in a totally new way. In fact, it only samples in 1-neighborhood, concatenate within \( G_{v,1} \) to generate higher-neighborhood computational graph. Like Fig. 3 shown, the node 1 and 4’s \( G_{v,2} \) are derived from the concatenation of node 1, 2, 4, and 5’s \( G_{v,1} \). From the experiment result mentioned later, CONCAT sampler can guarantee the test accuracy while simplifying the process of acceleration with FPGA.
IV. HARDWARE ACCELERATION OF SAMPLING PROCESS

So far, few works mainly focus on hardware acceleration of neighbor sampling process, most of them concern about the whole acceleration of training pipeline and regard neighbor sampling as a step of data preprocessing, or implement sampler in the architecture without giving more detailed description[15][16][17]. Some other works [18][19][20][21][22] proposed some new samplers or sampling methods from software level without thinking about acceleration from hardware level. In this work we proposed a hardware architecture in order to accelerate our CONCAT sampler and use FPGA as out platform.

As mentioned above, in sampling process, the information we need includes target nodes’ degree and node IDs that have connection with target nodes, and they are stored in "degree list" and "edge list" in RAM, respectively. In degree list, the nodes’ degree are stored according to node IDs, in other words, we use node ID as offset address. In edge list, neighbor node IDs are also stored according to target node ID (For undirected graph, we use two directed edges opposite in direction to represent one undirected edge). Therefore, if we use $x_d$ to represent the address that stores node $i$’s degree, use $x_e$ to represent the address that stores node $i$’s 1-hop neighborhood's node ID, and $x_{d0}$, $x_{e0}$ represent degree list’s base address and edge list’s base address, $x_d$ and $x_e$ can be represented as:

$$x_d = x_{d0} + d_{vi}$$  

$$x_{e0} + \sum_{n=0}^{i} d_{vn} \leq x_e < x_{e0} + \sum_{n=0}^{i+1} d_{vn}$$

Due to the limited BRAM size in FPGA, hardware structure should change according to the size of input dataset. For the small datasets like Cora, Citeseer, PubMed and so on, the on-chip BRAM can entirely store their edge lists and degree lists, which enables sampler directly read full information from it, and complete sampling process for a single time. However, for larger datasets like NELL, ogbn-arxiv[23], Reddit and so on, the on-chip memory cannot store whole edge lists and degree lists, due to which their degree lists and edge lists must be stored in off-chip memory like DDR, and they can be load into FPGA in sampling process. In sampling process of large datasets, for each time the sampler loads a batch of data lists and edge lists, samples a given number of neighbor nodes in and outputs the sample result. The data lists and edge lists are loaded sequentially, according to node IDs.

A. Sampling module for small datasets (Fig.4)

For small datasets (Cora, Citeseer, Pubmed etc.), the sampling process mainly includes:

1. Generate random number $r$.
2. $r$ modulo $d_{vi} (r = r \mod d_{vi})$ to make sure the random number does not exceed the degree of the node.
3. The address of node ID of neighbor node going to be sampled can be computed according to $x_{e0} + \sum_{n=0}^{i} d_{vn} + r$, and the sampler will read from target address and output the result to the specific port.

As a kind of stochastic sampler, CONCAT sampler needs a random number generator. However, for hardware devices, a completely-true random number generator is actually difficult to be implemented. Therefore, we designed a pseudo-random number generator. Many types of random number generators use linear congruence algorithm, their periods are very long in order to make the generated numbers seem completely random. For linear congruence algorithm, it consists a lot of modulo operation, which is complicated and slow in hardware devices. If we implement this method in FPGA, it will consume a large amount of resources and will let FPGA work at a lower frequency. To solve this problem, we choose LFSR (Linear-feedback shift register) structure to generate random number. In this structure, we used 16 registers so the original generated random number is between 0 and 65535.
It is important to note that we still used modulo operation after the random number is generated. We only avoid modulo operation in the generation process.

After the generation of random number, we used modulo operation to make the range of the random number is between 0 and \( d_{v_i} \), random number bigger than node’s degree is meaningless in sampling process. As mentioned above, modulo operation is a long time process in FPGA. To solve this problem, we used 8 parallel modulo operation modules in our architecture. They work in parallel, and take turns to input and output data to improve the frequency. The process is controlled by the logic and timing control unit. Based on this way, we can generate a random number between 0 and \( d_{v_i} \) in one clock cycle.

After modulo operation, as Fig.5 shown, if we note \( x_{e0} + \sum_{n=0}^{i} d_{v_n} \) as the base address of node \( v_i \), and random number \( r \) works as offset address, then the address that stores neighbor node ID being sampled equals \( x_{e0} + r \). After sampled the given number of neighbor nodes of node \( v_i \), the base address changed to \( x_{e(i+1)} \) and the sampler will start the sampling process of node \( v_{i+1} \). In the end, the sampled result can be sequentially sent to a given port or stored in RAM, depends on user’s intention.

### B. Sampling module for large datasets (Fig.6)

Sampling of large datasets requires data from off-chip sources (See Chapter IV). Off-chip data can be read from IO ports and stored into data registers, and sampling module samples the data stored in registers. Here we use Reddit dataset as an example to introduce our solution of sampling from large datasets. Due to the limited bus width, the maximum bit width of data transmitted into FPGA at one time is 1024 bits. However, for Reddit dataset, it has a large number of nodes (232965 nodes), which means that we need 18 bits number to store node IDs. Therefore, for a single time, the sampler can only load 56 neighbor node IDs, with 16 bits width free regarding the maximum 1024 bits. We use the free bus width to transmit node degree. As a matter of fact, some nodes have more than 56 neighbor nodes, in other words, we cannot load all neighbor nodes at once. To solve this problem, we found that we can simply discard the neighbors other than the first 56 neighbors when the number of neighbors exceeds the limit and then sample among only 56 neighbors. Due to the reduction in the number of neighbors that should participate in sampling, it is necessary to verify whether this solution will lead to an unacceptable decrease in accuracy before using it. The data in Fig. 7(a) shows that the test accuracy of this solution does not decrease, which indicates that this solution is feasible.
Different from the sampler of small datasets, 56 neighbor node IDs are stored in 56 register arrays. Random number is generated with the range of 0 and \( \min(d_{vi}, 56) \), and it selects the corresponding neighbor node ID as sample result. After sampling given number of neighbor nodes, the sampler will read the next node’s 56 neighbor IDs into register, and repeat the process mentioned above.

V. EXPERIMENTS

A. Accuracy of CONCAT Sampler and its comparison with the traditional 2-neighborhood sampler

| Dataset | Optimizer | aggregation | learning rate | Hidden layer dim |
|---------|-----------|-------------|---------------|-----------------|
| Cora    | Adam      | mean        | 0.001         | 32              |
| Citeseer|           |             | 0.001         | 32              |
| PubMed  |           |             | 0.001         | 512             |
| NELL    |           |             | 0.001         | 256             |
| OGB-archiv |       |             | 0.001         | 64              |

To apply CONCAT sampler into training and evaluation process, we designed a dataloader derived from torch_geometric.loader.NeighborSampler (A class in Pytorch Geometric [8] to generate mini-batch in training process). It uses CONCAT sampler to sample from each node, and generate mini-batch in train, test and validation process. Our hyperparameter settings are listed in table II.

Obviously, for each dataset, their test accuracy will be higher if more neighbor nodes are sampled in the training process. In this work, we tested the relationship between test accuracy and number of sampled neighbor nodes (num_neighbors, from 1 to 15). The test result are shown in Fig.7(b). From the result we can find the accuracy will converge when num_neighbors reaches to about 15. In table III we listed different datasets’ test accuracy when num_neighbors=15, and compared test accuracy between CONCAT sampler and 2-neighborhood sampler. From the result we can find that the accuracy loss of the CONCAT sampler is less than 1.5%, thus we can say that CONCAT sampler can keep the accuracy within acceptable limits. Specifically, for Reddit, if we sample [12,12] neighbors with CONCAT sampler, we can reach the same accuracy (0.950) as if we had sampled [25,10] neighbors with 2-neighborhood sampler.

B. Hardware acceleration test

We used Xilinx Virtex®-7 FPGA VC707 Evaluation Kit as our hardware platform. We applied our proposed acceleration architecture on this device, and conducted several experiments to test the performance of hardware accelerator. In our experiments, the sampling accelerator works at a maximum frequency of 250MHz.

The module can sample one neighbor node in each clock cycle. The number of sampled neighbor nodes can be ad-
TABLE III
ACCURACY ON DIFFERENT DATASETS

| Dataset | Nodes | Edges | Accuracy with 2-neighborhood sampler | Accuracy with CONCAT sampler |
|---------|-------|-------|---------------------------------------|-----------------------------|
| Cora    | 2708  | 5429  | 0.737                                | 0.797                       |
| Citeseer| 3327  | 4712  | 0.639                                | 0.648                       |
| PubMed  | 19717 | 44338 | 0.747                                | 0.746                       |
| NELL    | 65755 | 251350| 0.8641                               | 0.5507                      |
| OGB-arxiv | 160543 | 1106241 | 0.7396                               | 0.769                       |
| Reddit  | 252965| 37407946| 0.9547                               | 0.9528                      |

TABLE V
DYNAMIC POWER CONSUMPTION OF PARALLEL SAMPLING MODULES (Cora)

| Dynamic Power Consumption Type | Power (W) | Percentage |
|--------------------------------|-----------|------------|
| clocks                        | 0.208     | 5%         |
| signals                       | 0.736     | 16%        |
| logic                         | 0.48      | 11%        |
| BRAM                          | 0.16      | 4%         |
| others                        | 2.912     | 64%        |

just based on model configuration. In our experiment, num_neighbors is set to 15 according to test result mentioned above, and other hyperparameter settings are the same as table II. Under this samples number setting, the acceleration test results are listed in the table IV.

From the results we can find the sampling process has been greatly accelerated (about 300 to 1000 times faster). It also proves that our proposed CONCAT sampler is easy to be accelerated on hardware device.

In fact, for a single sampling module, it only consumes small amount of on-chip resources. Therefore, we can implement multiple sampling modules on our device in order to utilize all on-chip resources. Each sampling module can carry out sampling process independently, and their data input and output are in a parallel state. For dataset that needs to be sampled, we can divide the dataset beforehand, which means that we will divide its degree list and edge list into several segments, and each module independently sample from the corresponding segment, as shown in Fig.8. Each module’s sample result is output independently and can be directly concatenated into a complete sample result. Based on this idea, the sampling process can be further accelerated.

Here we give an example of dynamic power consumption data of the parallel sampling modules for small-scale datasets (use Cora as an example), as shown in the table V. In our platform, 16 parallel modules can fully use the on-chip resources. It is important to note that the power consumed by the BRAM is related to the size of the dataset and the size of the segment, and the proportion of BRAM power consumption will increase if the size of degree list and edge list becomes larger.

VI. CONCLUSION

In this work, we proposed a novel, dedicated to hardware acceleration neighbor sampler — CONCAT Sampler. It can easy to be accelerated on hardware platform, and ensure the model’s test accuracy at the same time. We also designed and hardware architecture to accelerate sampling process of CONCAT sampler. For CONCAT Sampler, its algorithmic features allow it to only sample 1-neighborhood to achieve n-neighborhood sampling, making its hardware acceleration architecture very simple and easy to implement.

In our experiment, we implemented our architecture on FPGA, and shortened sampling time by a factor of 300 to
1000. Meanwhile, we ensured that the final test accuracy of the model is consistent with the existing baseline, even improved a bit in some cases. For larger datasets, the speedup of our sampler is more pronounced. In fact, larger datasets often take more time in sampling process. Therefore, our proposed sampler is a good solution to slow sampling phenomenon, especially on large datasets.

REFERENCES

[1] Joan Bruna, Wojciech Zaremba, Arthur Szlam, and Yann Lecun. Spectral networks and locally connected networks on graphs. In International Conference on Learning Representations (ICLR2014), CBLS, April 2014, pages http-openreview, 2014.
[2] David K Duvenaud, Dougal Maclaurin, Jorge Iparraguirre, Rafael Bombarell, Timothy Hirzel, Alán Aspuru-Guzik, and Ryan P Adams. Convolutional networks on graphs for learning molecular fingerprints. Advances in neural information processing systems, 28, 2015.
[3] Michaël Defferrard, Xavier Bresson, and Pierre Vandergheynst. Convolutional neural networks on graphs with fast localized spectral filtering. Advances in neural information processing systems, 29, 2016.
[4] Mathias Niepert, Mohamed Ahmed, and Konstantin Kutzkov. Learning convolutional neural networks for graphs. In International conference on machine learning, pages 2014–2023. PMLR, 2016.
[5] Thomas N Kipf and Max Welling. Semi-supervised classification with graph convolutional networks. arXiv preprint arXiv:1609.02907, 2016.
[6] Will Hamilton, Zhitao Ying, and Jure Leskovec. Inductive representation learning on large graphs. Advances in neural information processing systems, 30, 2017.
[7] Hanqing Zeng, Hongkuan Zhou, Ajitesh Srivastava, Rajgopal Kannan, and Viktor Prasanna. Graphsaint: Graph sampling based inductive learning method. arXiv preprint arXiv:1907.04937, 2019.
[8] Matthias Fey and Jan E. Lenssen. Fast graph representation learning with PyTorch Geometric. In ICLR Workshop on Representation Learning on Graphs and Manifolds, 2019.
[9] Mingyu Yan, Lei Deng, Xing Hu, Ling Liang, Yujing Feng, Xiaochun Ye, ZhiMin Zhang, Dongrui Fan, and Yuan Xie. Hygc: A gcn accelerator with hybrid architecture. In 2020 IEEE International Symposium on High Performance Computer Architecture (HPCA), 2020.
[10] Tong Geng, Ang Li, Runbin Shi, Chunshu Wu, Tianqi Wang, Yanfei Li, Guangyu Sun, Xiaochun Ye, and Dongrui Fan. Tgl: A general framework for temporal gnn training on billion-scale graphs. arXiv preprint arXiv:2203.14883, 2022.
[11] Bowen Hao, Jing Zhang, Hongzhi Yin, Cuiping Li, and Hong Chen. Pre-training graph neural networks for cold-start users and items representation. In Proceedings of the 14th ACM International Conference on Web Search and Data Mining, pages 265–273, 2021.
[12] XiaoQing Yan, Riquan Chen, Litong Feng, Jingkang Yang, Huabin Zheng, and Wayne Zhang. Progressive representative labeling for deep semi-supervised learning. arXiv preprint arXiv:2108.06070, 2021.
[13] Weihsia Hu, Matthias Fey, Marinka Zitnik, Yuxiao Dong, Hongyu Ren, Bowen Liu, Michele Catasta, and Jure Leskovec. Open graph benchmark: Datasets for machine learning on graphs. Advances in neural information processing systems, 33:22118–22133, 2020.
[14] Ziqi Liu, Zhengwei Wu, Zhiqiang Zhang, Jun Zhou, Shuang Yang, Le Song, and Yuan Qi. Bandit samplers for training graph neural networks. Advances in Neural Information Processing Systems, 33:6878–6888, 2020.
[15] Qingru Zhang, David Wipf, Quan Gan, and Le Song. A biased graph neural network sampler with near-optimal regret. Advances in Neural Information Processing Systems, 34, 2021.
[16] Hongkuan Zhou, Da Zheng, Israt Nisa, Vasileios Ioannidis, Xiang Song, and George Karypis. Tgl: A general framework for temporal gnn training on billion-scale graphs. arXiv preprint arXiv:2203.14883, 2022.

ACM Computing Surveys (CSUR), 54(9):1–38, 2021.