Tech Report:
One-stage Lightweight Object Detectors

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Abstract

This work is for designing one-stage lightweight detectors which perform well in terms of mAP and latency. With baseline models each of which targets on GPU and CPU respectively, various operations are applied instead of the main operations in backbone networks of baseline models. In addition to experiments about backbone networks and operations, several feature pyramid network (FPN) architectures are investigated. Benchmarks and proposed detectors are analyzed in terms of the number of parameters, Gflops, GPU latency, CPU latency and mAP, on MS COCO dataset which is a benchmark dataset in object detection. This work propose similar or better network architectures considering the trade-off between accuracy and latency. For example, our proposed GPU-target backbone network outperforms that of YOLOX-tiny which is selected as the benchmark by 1.43x in speed and 0.5 mAP in accuracy on NVIDIA GeForce RTX 2080 Ti GPU.

1 Introduction

Object detection [1, 2] is one of the various vision tasks that localizes and classifies objects in a scene. In recent years, object detection is applied to numerous fields such as unmanned stores, and face-recognition based security systems. Early Studies about object detection are based on two-stage detectors [3], which show high performance but low hardware efficiency. Nowadays, the more object detection permeates in real life, the higher demand increases for lightweight detectors. For instance, there may need real-time object detection in a field of surveillance systems, or some constraints such as battery limit and computing power can exist in edge devices. However, the efficiency of a detector is affected by not only operations in the network, but also hardware architectures that the detector is executed on. For instance, inverted residual bottleneck, which is proposed in MobileNetv2 [4], is designed for better efficiency while barely sacrificing accuracy. Meanwhile, Google’s TPU [5] is one of the most remarkable hardware which is optimized for executing DNNs. Unfortunately, inverted residual bottleneck performs poorly on TPU for its architectural advantage is not suitable for exploiting TPU [6]. Therefore, it is necessary to design networks while considering properties of operations and hardware architectural features comprehensively.

In this work, we examined novel one-stage lightweight detectors [7, 8] and various modern operations in terms of accuracy and latency. Based on the examination, we propose the best operations and architectures on GPU and CPU, respectively. In GPU experiments, our suggested object detector is based on YOLOX [7] and it adopts fused inverted residual bottleneck [9] in the front and inverted residual bottleneck in the back. It outperforms YOLOX-tiny 1.43x in speed and 0.5 mAP in accuracy. In CPU experiments, despite that YOLOX-tiny is the best in terms of mAP, our suggested one which is based on PP-PicoDet [8] shows only 74% of the number of parameters and 1.12x in speed while sacrificing 1.3 mAP in accuracy.

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2 Related works

2.1 One-stage detector

One-stage detector often consists of a backbone network, feature pyramid network (FPN) [10], and detection head. Backbone network is a general feed-forward network and it extracts meaningful properties from input images. Unlike two-stage detectors, one-stage detectors directly use features from backbone networks in bounding box regression and classification. Thus, backbone network is highly related to the performance of the detector.

From each stage of a backbone network, various sizes of features are obtained. High-resolution features from earlier stages have weak semantics, while low-resolution features from later stages have strong semantics. FPN combines these various sizes of features and makes features from earlier stages have rich information.

Detection head is the most important part of detectors. The two tasks of object detection, bounding box regression and classification, are done in detection head by using features from backbone network and FPN. Detection head is highly related to the loss function of the detector.

There are two baselines in this work, each of which targets GPU and CPU, respectively. YOLOX [7] is one of the latest one-stage object detectors, which is used as the main baseline for GPU in this work. The backbone network of YOLOX is CSPDarknet and the FPN of YOLOX is path aggregation feature pyramid network (PAFPN) [11]. PP-PicoDet [8] is also a novel one-stage detector that targets on CPU. The backbone network of PP-PicoDet is PP-LCNet (lightweight CPU convolutional neural network) [12]. The FPN of PP-PicoDet is Lightweight CPU Path Aggregation Network (LCPAN), which is a variant of PAFPN.

2.2 Operations

There are several works that pursue efficiency while trying to barely sacrifice performance. CSP layer [13], which is the main operation in YOLOX backbone network, is an architecture for achieving abundant gradient combinations while reducing computational costs. Depthwise separable convolution operation, which is the main operation of PP-LCNet, was proposed in MobileNet [14] which is one of the early works in this field. It reduces computational costs by using depthwise convolution operation and combines information among channels with a $1 \times 1$ convolution operation. MobileNetv2 [4] is a follow-up research of MobileNet and it proposed inverted residual bottleneck architecture, which is a dominant architecture in mobile settings. Based on depthwise separable convolution, it expands input channels of the depthwise convolution operation with a $1 \times 1$ convolution operation in front of that. EfficientNetv2 [9] tackled MobileNetv2 that using inverted residual bottleneck in the whole network is not efficient, and it proposed fused inverted residual bottleneck architecture, which replaces the first $1 \times 1$ convolution and the depthwise convolution operation of inverted residual bottleneck with a convolution operation, for replacing inverted residual bottleneck at the front of networks. X block used in RegNet [15] is a result of designing generalized architecture across settings, and sandglass bottleneck [16] is designed to improve inverted residual bottleneck for mitigating information loss and gradient confusion. Blueprint separable convolution [17] is a variant of depthwise separable convolution which aims for improving MobileNet by replacing cross-kernel correlations in depthwise separable convolution with intra-kernel correlations.

2.3 Feature pyramid network

In a general feed-forward neural network, high-resolution features from early layers have weak semantics while low-resolution features from later layers have strong semantics. FPN is an architecture for combining various sizes of features to make all features have strong semantics. The FPN architectures in both YOLOX and PP-PicoDet are based on PAFPN. PAFPN is based on FPN architecture which adds bottom-up path augmentation for enhancing semantics of features by propagating low-level features to others. SepFPN is an FPN architecture based on PAFPN, which removes the bottom-up path in PAFPN and adds residual paths from inputs to outputs of FPN. It pursues faster latency even at the expense of accuracy a little.
3 Lightweight detector design

3.1 Micro architectures for backbone network

In GPU experiments, CSP layer in CSPDarknet is replaced with several bottleneck architectures, such as inverted residual bottleneck (MBConv), fused inverted residual bottleneck, RegNet bottleneck, and sandglass bottleneck to verify whether CSP layer is the best architecture in YOLOX backbone network. EfficientNetv2 proposed that using fused inverted residual bottleneck to the front of networks and inverted residual bottleneck to the rest is good for both accuracy and efficiency. In this paper, each network that comprises inverted residual bottleneck only, fused inverted residual bottleneck only, and use both operations simultaneously are addressed. A policy that uses inverted residual bottleneck and fused inverted residual bottleneck in a single network is named mixed inverted residual bottleneck.

In CPU experiments, depthwise separable convolution operation and blueprint separable convolution operation are examined with PP-PicoDet. For a fair comparison with YOLOX baseline, channels of each block are set the same as those of YOLOX. Additionally, FPN architecture and detection head in PP-PicoDet are replaced with those of YOLOX.

3.2 Feature pyramid network

The main operation of YOLOX’s PAFPN is CSP layer and that of LCPAN is depthwise separable convolution, respectively. In addition, the major difference between these two FPN is whether channels of input features are equalized before FPN operation or not. In PAFPN, channels of input features are not equalized. Rather, channels of FPN outputs are equalized before they are fed to the detection head. It leads to better performance in terms of accuracy but is bad for latency because channels in FPN are large. On contrary, in LCPAN, channels of input features are equalized in front of FPN. Then, channels of output features are the same, while channels in FPN are reduced. SepFPN is based on PAFPN of YOLOX. That is, the main operation of SepFPN is CSP layer and channels of input features are not equalized. In this work, a modified PAFPN architecture is proposed, which replaces concatenation operations in FPN with sum. By doing so, channels in FPN can be reduced while rich semantics in feature maps are expected to preserve. This technique is applied to both YOLOX’s PAFPN and PP-PicoDet’s LCPAN and examined.

4 Experimental results

4.1 Experimental settings

For a fair comparison, a detection head from YOLOX is applied in both baselines. That is, several operations, backbones, and FPN architectures are targets in this work. In GPU experiments, expand ratios of bottleneck architectures except sandglass bottleneck are set to 1, and that of sandglass bottleneck is set to 0.5. Hyperparameters related to network design (e.g., the number of blocks, channels of each block, etc.) are set as the same with YOLOX-tiny. While training networks, any other hyperparameters except network architectures follow the default settings of YOLOX. In GPU experiments, NVIDIA GeForce RTX 2080 Ti is used to measure GPU latency. In CPU experiments, Intel(R) Core(TM) i9-9900K CPU @ 3.60GHz is used to measure CPU latency. While measuring latency, mini batch size and the number of threads are set to 1.

4.2 Baseline latency breakdown

Figure 1 shows GPU and CPU latency of the baseline model. The backbone network accounts for 40% of the total latency on GPU, and 53% on CPU. Thus, it is critical to reducing backbone latency to lighten detectors. FPN, which is also the target to improve in this work, accounts for 27% of total latency on GPU and 18% on CPU. Detection head occupies more compared to FPN. However, because it is highly related to the loss function of detectors, detection head is fixed in all experiments for a fair comparison.
4.3 GPU-target detector

Figure 2 shows GPU latency of backbone network and mAP depending on the main operation of backbone networks. As shown in the Figure 2a, YOLOX tiny is the best in terms of mAP, but its GPU latency is the worst. A backbone network that consists of fused inverted residual bottleneck has the largest number of parameters. However, its GPU latency is the fastest among all settings. Fused inverted bottleneck is the only one that uses a $3 \times 3$ convolution operation rather than a $3 \times 3$ depthwise convolution operation. $3 \times 3$ convolution operation is the most basic convolution operation, and it is highly optimized on GPU. That’s the reason a detector that adopts fused inverted residual bottleneck as the main operation of the backbone is the fastest on GPU even though the number of parameters is the largest.

This work focuses on the policy which is proposed in EfficientNetv2 [9]: Use fused inverted residual bottleneck to the front of the network and inverted residual bottleneck to the rest. In Figure 2a, mixed inverted residual bottleneck is noticeable because it is fast, lightweight, and has a lot of diversity in terms of design. Mixed inverted residual bottleneck can leverage parallel computing and get better mAP by using fused inverted residual bottleneck while pursuing lightness by using inverted residual bottleneck. Also, it has a lot of potential because the number of fused inverted residual bottleneck operations is an important design policy. CSPDarknet, which is the backbone network of YOLOX, has 4 blocks. Therefore, networks that use 1 or 2 fused inverted bottlenecks are examined. Furthermore, because the number of parameters in mixed inverted bottleneck is smaller than that of YOLOX baseline, networks that set expand ratio to 1.5 is also investigated. Figure 2b shows the results of this ablation study. Using 2 fused inverted residual bottlenecks and 2 inverted residual...
bottlenecks is better than 1 fused inverted residual bottleneck and 3 inverted residual bottlenecks, in terms of latency and mAP. Moreover, a policy that uses a larger expand ratio is still faster than YOLOX baseline. Therefore, the purple dot in Figure 2b is chosen as the best detector in GPU experiments.

4.4 CPU-target detector

In this section, CSPDarknet, which is the backbone network of YOLOX, is replaced with PP-LCNet in PP-PicoDet. In addition, blueprint separable convolution operation is applied to PP-LCNet as an alternative of depthwise separable convolution, which is the main operation of PP-LCNet. The channels of PP-LCNet are set the same as those of CSPDarknet in order to compare fairly. However, because PP-LCNet is much smaller than CSPDarknet, detectors that use twice as large as the default network are also examined. Note that FPN architecture of these detectors is different from others in order to use the same detection head for a fair comparison.

Figure 3a shows CPU latency of backbone network and mAP of the above detectors. Using PP-LCNet as the backbone leads to generating lightweight detectors. Detectors that adopt blueprint separable convolution operation as the main operation are slower and show higher mAP compared to those which adopt depthwise separable convolution operation. Unfortunately, detectors that adopt PP-LCNet as the backbone network show low mAP as much as small the number of parameters they have compared to that of YOLOX baseline. To improve mAP, backbone networks with larger channels are also analyzed. They show a lot of improvement in mAP, while sacrificing latency. Even though the number of parameters in each backbone is similar to that of YOLOX, either latency or mAP is worse than that of YOLOX. When the number of channels in the backbone network is changed, that in FPN also should be changed. However, because detection head is fixed in all experiments, the output channels of PP-LCNet with larger channels are equalized and therefore their FPN architectures are smaller than others. Figure 3b shows CPU latency of whole detector and mAP of the same detectors in Figure 3a, for taking their FPN architectures into account. A detector that adopts DSConv as the main operation and has larger channels shows faster latency and a much less number of parameters compared to YOLOX baseline. The number of parameters is also a major constraint in real-world scenarios, and thus this setting can be a good solution when a fast detector with less number of parameters is needed.

Figure 3: Results of CPU experiments.
4.5 FPN architecture analysis

In this section, the performances of FPN architectures are investigated with the backbone network which is searched in section 4.3. PAFPN, which is the default FPN architecture of YOLOX is the best in terms of mAP. LCPAN, which is the default FPN architecture of PP-PicoDet is the best in terms of the number of parameters and latency. Proposed FPN architectures (replace concatenation operation with sum) perform bad compare to baseline. The expected effect of proposed FPN architectures is preserving semantics while reducing channels in FPN by summing features from different blocks. However, it doesn’t work as expected. Especially, PAFPN-based proposed FPN architecture performs badly on GPU. It means that reducing channels in FPN doesn’t lead to reducing latency because GPU has huge parallel computing power.

5 Conclusion

This work analyzes the architectural design spaces of a novel one-stage detector. Optimal architecture design in object detectors depends on target hardware and purpose. Figure 5 shows searched networks.
in section 4 along with YOLOX baseline. Figure 5a denotes mAP and latency of the baseline, the GPU target detector, and the CPU target detector executed on GPU. The GPU target detector which is marked with an orange dot shows the best mAP while achieving the best GPU latency, even though the CPU target detector has a less number of parameters. Therefore, the GPU target detector searched in this paper is the best in both aspects. Figure 5a denotes mAP and latency of detectors the same as Figure 5a executed on CPU. The CPU target detector which is marked with a blue dot shows the worst mAP, yet it is much faster than others on CPU. Further, it has a much less number of parameters compared to others. Therefore, if there is not enough computing power and energy budget, the CPU target detector can be a good solution. Figure 5 doesn’t plot FPN results. Nevertheless, FPN is also an important factor in detectors and should be designed carefully depending on the purpose.

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A Appendix

A.1 Experimental results with values

The below tables show the stats of each detector searched in section 4. A bold value represents the best value in each column.

| Architecture            | backbone # of params (M) | backbone Gflops | backbone GPU latency (ms) | mAP  |
|-------------------------|--------------------------|-----------------|---------------------------|------|
| YOLOX tiny              | 2.3723                   | 2.6648          | 1.7260                    | 32.8 |
| Inverted bottleneck     | 1.6080                   | 1.5884          | 1.2242                    | 31.2 |
| Mixed inverted bottleneck| 1.6167                   | 1.6953          | 1.2091                    | 31.1 |
| Fused inverted bottleneck| 3.7042                   | 3.9063          | **1.1431**                | 32.3 |
| RegNet bottleneck       | 1.6329                   | 1.6668          | 1.3197                    | 31.3 |
| Sandglass bottleneck    | **3.3432**               | **1.3997**      | **1.4159**                | 30.8 |

Table 1: Results of GPU experiments in Figure 2a

| Architecture                                    | backbone # of params (M) | backbone Gflops | backbone GPU latency (ms) | mAP  |
|------------------------------------------------|--------------------------|-----------------|---------------------------|------|
| YOLOX tiny                                      | 2.3723                   | 2.6648          | 1.7260                    | 32.8 |
| Fused 1: Inverted 3, expansion=1.0              | **1.6167**               | **1.6953**      | **1.1209**                | 31.6 |
| Fused 2: Inverted 2, expansion=1.0              | 1.7978                   | 2.5971          | 1.2237                    | 32.5 |
| Fused 1: Inverted 3, expansion=1.5              | 1.9054                   | 2.2505          | 1.2046                    | **33.3** |
| Fused 2: Inverted 2, expansion=1.5              | 2.1771                   | 3.6032          | 1.2046                    | **33.3** |

Table 2: Results of GPU ablation studies in Figure 2b

| Architecture                                    | # of params (M) | Gflops | CPU latency (ms) | mAP  |
|------------------------------------------------|----------------|--------|------------------|------|
| YOLOX tiny                                      | 5.0559         | 6.4150 | 73.4122          | 32.8 |
| PP-PicoDet DConv                                | **3.2680**     | **4.4628** | **49.8036** | 31.5 |
| PP-PicoDet BConv                               | 3.3307         | 4.7980 | 59.0566          | 32.7 |
| PP-PicoDet DConv (×2 channels)                  | 3.7591         | 5.3934 | 65.5060          | 31.5 |
| PP-PicoDet BConv (×2 channels)                  | 3.9951         | 6.8249 | 89.5966          | 32.7 |

Table 3: Results of CPU experiments in Figure 3a

| Architecture                                    | # of params (M) | Gflops | GPU latency (ms) | CPU latency (ms) | mAP  |
|------------------------------------------------|----------------|--------|------------------|------------------|------|
| PAFPN                                          | 4.8606         | 7.3894 | 3.6284           | 80.6611          | **33.3** |
| LCPAN                                          | 3.5535         | 6.6907 | 3.2626           | 76.6075          | 31.9 |
| PAFPN (cat to sum)                             | 4.7224         | 7.2399 | 3.6354           | 79.3600          | 32.0 |
| LCAPN (cat to sum)                             | **3.3845**     | **6.3338** | **3.2180** | **71.4919** | 31.2 |
| SepFPN                                         | 4.3532         | 7.1149 | 3.5134           | 77.9030          | 32.3 |

Table 5: Results of FPN experiments in Figure 4
A.2 Scale-up

In section 4.3, we designed the GPU target detector which has a similar size to YOLOX tiny. Figure 6 shows various sizes of YOLOX baseline and the GPU target detector searched in section 4.3 to verify the design policy established on section 4.3 is efficient with other sizes. Red dots denote YOLOX baselines of various sizes and orange dots denote GPU target detectors which are designed with the policy proposed in section 4.3. As shown in the figure, orange dots are better than red dots considering the latency-mAP trade-off. As scaling up, improvements in latency are much better while mAP increases smoothly compared to YOLOX counterpart. This trend will continue as the network grows in size.

Figure 6: GPU target detectors at scale.