Laser-Assisted Multilevel Non-Volatile Memory Device Based on 2D van-der-Waals Few-Layer-ReS\textsubscript{2}/h-BN/Graphene Heterostructures

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Few-layer rhenium disulfide (ReS\textsubscript{2}) field-effect transistors with a local floating gate (FG) of monolayer graphene separated by a thin hexagonal boron nitride tunnel layer for application to a non-volatile memory (NVM) device are designed and investigated. FG-NVM devices based on two-dimensional van-der-Waals heterostructures have been recently studied as important components to realize digital electronics and multifunctional memory applications. Direct bandgap multilayer ReS\textsubscript{2} satisfies various requirements as a channel material for electronic devices as well as being a strong light-absorbing layer, which makes it possible to realize light-assisted optoelectronic applications. The NVM operation with a high ON/OFF current ratio, a large memory window, good endurance (>1000 cycles), and stable retention (>10\textsuperscript{4} s) are observed. The successive program and erase states using 10 ms gate pulses of +10 V and −10 V are demonstrated, respectively. Laser pulses along with electrostatic gate pulses provide multibit level memory access via opto-electrostatic coupling. The devices exhibit the dual functionality of a conventional electronic memory and can store laser-pulse excited signal information for future all-optical logic and quantum information processing.

1. Introduction

The atomically flat two-dimensional (2D) surfaces of layered materials make it possible to realize tuneable properties via strong electrostatic coupling. A van-der-Waals (vdW) 2D heterostructure combining a semiconductor, an insulator, and a conductor has various important applications in digital electronics and memory operations.\textsuperscript{[1–3]} For instance, insulating atomically flat hexagonal boron nitride (h-BN) can function as a tunnelling layer between a conductor and a semiconducting channel thus allowing perfectly planar charge injection across the atomically flat interface.\textsuperscript{[3,5]} Recently non-volatile memories (NVMs) based on 2D heterostructures and their tunable and multibit operation under laser light have been reported.\textsuperscript{[6–15]} Laser-assisted memory operation provides a new degree of freedom for multifunctional optoelectronic devices with the extra functionality of optically communicated multilevel access.\textsuperscript{[1,16–18]} Laser light can travel through free space without losing power and this allows us to operate optoelectronic devices from a long distance away at low power and with little need for maintenance. Therefore, there is a need for a low operating power and optical control through fiber cable for the multi-level operation of NVM devices. In addition to the data storage capability, there is a strong need for an NVM optoelectronic device that can distinguish light wavelengths for color sensing in digital imaging.\textsuperscript{[19]}

Floating gate (FG)-NVM devices based on 2D vdW heterostructures have recently been studied as important components with which to develop digital electronics and optoelectronics. Compared with conventional Si 3D semiconductors, all-2D layered materials and their heterostructures are superior for NVM applications due to their atomically flat surfaces without dangling bonds, high carrier mobility, vdW interaction in a vertically stacked geometry, and the potential for increasing the integration density. Direct bandgap multilayer rhenium disulfide (ReS\textsubscript{2}) satisfies various requirements as a channel material for memory device applications since it exhibits excellent electrical properties with high carrier mobility compared with other transition metal dichalcogenides (TMDCs), such as molybdenum disulfide (MoS\textsubscript{2}). Few-layer ReS\textsubscript{2} material is a good channel material for field-effect transistors (FETs). Moreover, it is a good light absorbing material thanks to its thickness-independent direct band gap (∼1.4–1.5 eV), which is useful for optics and optoelectronics applications.\textsuperscript{[20–23]}

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A thin layer of h-BN can be used to further enhance field-effect mobility due to reduced charge trapping/scattering sites and atomically flat electrostatic modulation. BN is used as a thin insulating tunnel layer, and highly conductive monolayer graphene (MLG) can be used as a FG that can store charge carriers for device applications. Despite the outstanding electrical, optical, and optoelectrical properties of this device, which consists of a vertical heterostack with a semiconductor/insulator/conductor structure formed of ReS\textsubscript{2}/h-BN/FG-graphene, there is still a need to realize a multibit photo-signalling memory structure that operates at low power, with a high ON/OFF current ratio and a large memory window for all-optical logic processing devices.

The main purpose of this work is to evaluate the device performance of multilayer ReS\textsubscript{2} FETs with a local FG and to investigate the effects of a graphene floating gate when separated with a thin h-BN tunnel layer, for application to a multilevel NVM device via opto-electrostatic coupling. The proposed photoelectronic memory of multilayer-ReS\textsubscript{2}/h-BN/FG-graphene/SiO\textsubscript{2} devices can be operated in the same way as a conventional electronic memory at a low programming gate voltage. Moreover, the device can store laser pulse information as an electronic readout. In addition to offering dual functionality, a memory device with a large hysteresis window could open the way to achieving multibit data storage via both electrostatic and incident laser pulses. In this work, we demonstrate the first NVM operation via electrostatic coupling. The output characteristics \((I_d-V_d)\) under a constant gate bias and different gate bias pulse widths indicate a large hysteresis, which is related to the charge accumulation in FG-graphene as the result of tunnelling through thin h-BN. We investigated low power operation and a large memory window for multibit storage applications. The drain current-time characteristics \((I_d-t)\) at positive (+10 V) and negative (−10 V) gate pulse biases, respectively, make it possible to access two different states, namely “Program” and “Erase,” during NVM operation with a fast reading/writing speed (of the order of milliseconds). We demonstrate successive store/erase operations corresponding to logic “0” and “1,” respectively, via a cycle of positive/negative electrostatic gate pulses. In the second part of this work, we characterize the device performance under light illumination with laser wavelength of 532 nm, whose energy is higher than ReS\textsubscript{2} direct bandgap energy. Multi-level memory operation was demonstrated using opto-electrostatic coupling, in which the device communicated by using laser pulses along with the gate pulse dependence of the “ON” and “OFF” states of the memory device. Also, incident laser coupling at different powers allowed us to store multibit memory states. In addition to laser-power-dependent multi-level memory operation, we demonstrate memory operation by irradiating fixed power laser pulses and programmed gate pulses, where the device readout electronic memory state depends on the incident laser pulse frequency and electrostatic gate pulse frequency. This study provides an overview of the use of all-2D atomically flat layered materials to realize various electronic components including sensors, detectors, and memory devices for the Internet-of-Things (IoT) era. The photonic signal storage that we propose in this work can potentially enable all-optical logic processing and quantum information processing.

2. Results and Discussions

Our FET structure for NVM application is a vdW heterostructure consisting of a channel layer of multilayer ReS\textsubscript{2}, supported by high-quality thin h-BN as a carrier tunnelling layer, where we placed monolayer graphene beneath the h-BN as a FG to store charge carriers. Optical images of the different components used to fabricate the heterostructure and the electrical contacts used to form the device are shown in Figure 1a,b, respectively. The flake transfer method that we employed to form the heterostructure of the NVM device is described in the Experimental Section and the Supporting Information (Figure S1, Supporting Information). The transfer method involves the deterministic transfer of large-area high-quality 2D flakes onto an arbitrary substrate. Three-dimensional (3D) and cross-sectional views of a typical device architecture are shown in Figure 1c,d, respectively. We applied a back-gate voltage (control gate bias \(V_g\)) to the degenerately doped silicon substrate \((p^{++}\text{Si})\) to tune the memory characteristics via electrostatic coupling and the systematic shifting of the Fermi level of the ReS\textsubscript{2} channel along with band alignment across the ReS\textsubscript{2}/h-BN/FG-graphene heterostack. Before testing the electrical characteristics of the heterostructure FETs, we tested the electrical performance of graphene, ReS\textsubscript{2}, and ReS\textsubscript{2}/h-BN FET devices. Figure S2a,b (Supporting Information) shows the p-doped electrical characteristics of a monolayer graphene FET that result from the absorption of oxygen or water in air.[24] Here, a gate voltage of +20 V is needed to reach the charge neutrality point. Graphene was immediately transferred to the top of the treated SiO\textsubscript{2}/Si substrate, and the result was that there was almost no hysteresis in the sweep transfer characteristics \((I_d-V_d)\) due to the lack of water molecules at the graphene/SiO\textsubscript{2} interface. Figure S2c,d (Supporting Information) shows the electrical performance of ReS\textsubscript{2} FETs with and without a bottom
h-BN layer. The field mobility of the device was enhanced because there were fewer charge trapping/scattering sites and an atomically flat electrostatic modulation was realized by using a thin layer of h-BN as the tunnel layer of the device.

We confirmed the crystalline quality of the transferred ReS$_2$ layer by Raman spectroscopy (Figure 2a), which indicated the highly crystalline and high chemical purity of the ReS$_2$ flake material. The ReS$_2$ layer was a few atomic layers (≈5 nm) thick, which was further verified with an atomic force microscopy (AFM) scan and a line profile monitoring the thickness (Figure 2d). We observed typical E$_{2g}$ (in-plane vibration mode) and A$_{1g}$ (out-of-plane vibration mode) peaks at 162 and 212 cm$^{-1}$, respectively, along with other labelled peaks. The Raman spectrum of graphene (Figure 2b) exhibits a highly crystalline monolayer thickness signature as it has a 2D/G peak integral intensity ratio greater than 2 and a narrow (and symmetric) 2D peak width-full width half maximum (FWHM) of 22.1 ± 0.5 cm$^{-1}$ at 2680.4 cm$^{-1}$. Other Raman peak signatures were present, namely those of an E$_{2g}$ in-plane phonon caused by the stretching C–C vibration mode and of a D peak at 1350 cm$^{-1}$, which is related to defects. The h-BN signature was observed in the E$_{2g}$ peak, which is the in-plane phonon vibration mode at 1366.4 cm$^{-1}$, where the thickness was ≈ 6 nm as monitored from the AFM topography image and the line profile (Figure 2c). Choosing the right h-BN thickness is very important if we are to promote Fowler–Nordheim (F-N) tunnelling and as well as protect the ReS$_2$ channel after charge storage in conductive monolayer graphene. Figure S3a,b (Supporting Information) distinguishes different region of direct tunnelling and F-N tunnelling with the F-N equation fitting at higher reverse bias region. Figure S3c (Supporting Information) shows the flat band alignment with the values of various parameters of the vertically integrated ReS$_2$/h-BN/graphene system. We found 5–7 nm to be the optimum h-BN thickness for multilevel memory applications. Thickness of h-BN dependent tunnelling behavior has been demonstrated elsewhere.\cite{65}

2.1. Electro-Static Memory Operation

The representative output characteristics ($I_d$–$V_d$) for different $V_g$ values (−30 V to +30 V) of a few-layer ReS$_2$/h-BN/FG-graphene FET structure shows a linear $I_d$–$V_d$ relation representing good electrical contacts with low contact resistance at both source and drain under a sweep $V_g$ bias without hysteresis (Figure 3a). Linear $I_d$–$V_d$ characteristics under various back-gate-dependent voltages indicate ohmic contact between the ReS$_2$ channel and source/drain electrodes. The representative transfer characteristics ($I_d$–$V_d$; sweep $V_d$) for different $V_d$ values represent the formation of a large hysteresis width for each drain bias (Figure 3b and Figure S4b, Supporting Information). The device exhibits n-channel charge transport with an electron mobility of around 10–20 cm$^2$ V$^{-1}$ s$^{-1}$ and an ON/OFF current ratio of $10^4$ at $V_d$ = 50 mV. The retention (Figure 3c and Figure S4c, Supporting Information) of the program/erase state of the memory device was measured with a $V_d$ of 50 mV for different gate bias $V_g$ values. The charges trapped in the graphene layer are maintained without any significant loss. We monitored the program/write state and erase state current over 1000 s with positive (+30 V, 5 s) and negative (−30 V, 5 s) gate voltage pulses, respectively. The logical “0” and “1” outputs are defined with the drain output current of the transistor below and above a current of 500 nA, respectively. Good data retention properties of the NVM devices were achieved in the time range of $10^4$ s (Figure S5, Supporting Information). Previously thermal assist memory operations have been studied in ReS$_2$, MoS$_2$ based FET devices, where it was found that the intrinsic
oxide traps, intrinsic defects/traps in channel material, and/or charge trapping and detrapping between the oxide and p++Si gate are the various reasons for the hysteresis modulation in memory operation.[26,27] Thermal stability of the retention properties and hysteresis width of the ReS₂/h-BN/graphene memory operation are tested (Figures S6 and S7, Supporting Information), which indicates that the memory operation is almost independent of temperature variation. Moreover, ReS₂/h-BN FET shows very less temperature dependent transfer characteristics, which further nullify the possibility of thermal assist memory operation of the ReS₂/h-BN transistors (Figure S8, Supporting Information). Bottom layer of h-BN could be assisting to reduce the intrinsic oxide traps and/or charge trapping and detrapping process between the oxide and p++Si gate induce effects on the transistor performance. Figures S9 and S10 (Supporting Information) show the NVM operation of few-layer ReS₂ with different thickness of h-BN, where monolayer graphene was used as FG-gate. To gain insight regarding the dynamics of charge carrier trapping and tunnelling and their role in terms of transfer characteristics when producing hysteresis under a sweep bias, we have monitored the transport characteristics while pulses the gate bias value from a program/write state—“OFF” state (+ 30 V) to an erased state—“ON” state (−30 V) (Figure 3d and Figure S4d, Supporting Information). The drain current was recorded, while the gate was repeatedly pulsed between V_g = −30 and 30 V. When we switched the pulse from a large negative bias to a positive bias, there was a sudden fast rise in the current in the channel followed by a slow decay. Whereas, when the gate pulse was returned to a high negative bias, the current decreased followed by a slow increment. The decay in the ON state during the program is due to electrons being captured in the traps of the bulk defects in the ReS₂ or ReS₂/h-BN interface states or the defect states of h-BN. On the other hand, the slow current increment in the OFF state is due to the electron emission from the captured states and/or gate field stress induced carriers’ leakage (Figure S11 and Supplementary Note 1, Supporting Information).[19,28]

Before we investigated multilevel photoelectric memory operation, we look at two-level memory operation via electro-static coupling. The sweep transfer characteristics (I_d–V_g) for different V_g,max values represent a large hysteresis window with a high sweep bias operation (Figure 4a), which is shown on a logarithmic scale plot in Figure S12c (Supporting Information). The shift of the threshold voltage in a positive direction corresponds to electron trapping in FG-graphene. The deduced threshold voltage shift (ΔV) as a function of gate voltage maxima (V_g,max) is summarized in Figure 4b. The amount of charge stored in the FG-graphene as a charge-trap layer can be estimated from the following expression:

n = \frac{ΔV \times C_{FG-CG}}{q} \tag{1}

where q is the electron charge, and ΔV is the difference between the threshold voltages for the read and erase states. C_{FG-CG} is...
the capacitance between a floating gate and the control gate and is defined as
\[
C_{FG-CG} = \varepsilon_0 \frac{d_{SiO_2}}{\varepsilon_{SiO_2}},
\]
where \( \varepsilon_0 \) and \( \varepsilon_{SiO_2} \), respectively, are the vacuum permittivity and relative dielectric constant of the SiO\(_2\) layer and \( d_{SiO_2} \) is its thickness (285 nm). This results in a stored carrier density of
\[
N = 2.9 \times 10^{12} \mathrm{cm}^{-2} \Delta V \approx \Delta V_{g,max}
\]
for \( \Delta V = 38 \mathrm{~V} \) (memory window) under a sweep gate bias of \( \pm 30 \mathrm{~V} \) \( (V_g, \text{max}) \). There may be a small error in the calculated value of the stored carrier’s density in FG-graphene caused by the charging/emission process of graphene–SiO\(_2\) interface traps. In agreement with other reports\,[29,30,31] the stored electron density allows a large memory window with strong potential for multibit data storage. Here we estimated the electron trapping rate in floating-gate graphene and quantify the tunnel current value by using the following expression:
\[
\frac{dn_{\text{trap}}}{dt} = \frac{C_{\text{ox}} dV_g}{q A}
\]
(2)
where \( dV_g \) and \( dV_{\text{g, max}} \) are the gate voltage (10 V) shift on a \( \Delta t \) (200 ms) time scale. Thus, we estimate the charge trapping rate to be \( \frac{dn_{\text{trap}}}{dt} = 3.8 \times 10^{12} \mathrm{cm}^{-2} \mathrm{s}^{-1} \). The charge trapping rate is relatively fast compared with the typical value for a metal-insulator-semiconductor, which is of the order of \( \approx 10^9 \mathrm{cm}^{-2} \mathrm{s}^{-1} \). A faster charge trapping rate than a typical MOS based memory device is another advantage of the NVM device, and this could be due to the reduced body thickness of the tunnelling layer h-BN in a vertical integrated heterostructure device. Finally, we estimate the tunnel current magnitude using the following formula:
\[
\frac{dn_{\text{transfer}}}{dt} = \frac{I_{\text{tunnel}}}{q A}
\]
(3)
where \( I_{\text{tunnel}} \), \( q \) and \( A \) are the tunnel current, electric charge and h-BN cross-sectional area, respectively. As calculated earlier, \( \frac{dn_{\text{transfer}}}{dt} = 2.3 \times 10^{15} \mathrm{cm}^{-2}\mathrm{s}^{-1} \), which provides a tunnel current value of \( I_{\text{tunnel}} = 18.4 \times 10^{-12} \mathrm{~A} \).

Figure 4c shows the dynamic behavior (logarithmic scale plot in Figure S12c, Supporting Information) of the NVM device in a single cycle with multiple pulses of low positive and negative gate bias, which includes programming, readout, erasing, and readout after erasing processes under a cycle of electrostatic gate pulses as shown in Figure 4d. Data reliability tests of NVM devices are measured for up to 1000 cyclic measurements of program/erase operation, which is shown in the Figure S13 (Supporting Information) cyclic endurance measurements. The fluctuations in the cyclic tests are quite small up to 1000 cycles operation, suggesting that the programmed data in the memory device is highly reproducible. Moreover, we have studied the tread-off relation between gate pulse width and amplitude of such gate field stressed memory operation (Figures S14 and S15, Supporting Information). It is observed that if we reduce the amplitude of the pulse gate voltage below 5 V at fixed width of

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**Figure 4.** Multi-level access via electrostatic coupling: a) Sweep drain current (\( I_d \)) versus gate bias (\( V_g \)) for different gate voltage maxima (\( V_{g,\text{max}} \)), which exhibits a large memory window. A large memory window enables us to realize multi-level operation. b) Hysteresis width (i.e., memory window) versus \( V_{g,\text{max}} \). The inset shows the band alignment across the heterostructure of Au/SiO\(_2\)/graphene/h-BN/ReS\(_2\) under a positive gate bias. Successful program/erase operations using an arbitrary gate pulse of \( \pm 30 \mathrm{~V} \) with a pulse width of 10 ms: c) \( I_d-t \) response of the NVM device under a drain bias condition of 0 V for 0.2 s and 0.05 V for the next 3 s, when using an arbitrary gate pulse of \( \pm 10 \mathrm{~V} \) with a pulse width of 10 ms as shown in (d).

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10 ms then the memory operation window gets reduce. Similarly, if we fixed the amplitude of pulse gate voltage at 10 V and reduce the pulse width below 5 ms then the memory window decreases. FG-graphene has the advantage that it can store electrons (negative potential) or holes (positive potential) in order to switch the ReS$_2$ channel with a high memory window “OFF” or “ON.” The positive control gate bias of a 10 V pulse with a 10 ms width has the effect of partially storing electrons at the FG-graphene, which turns the operation of the partial write/program state (“0” memory state) of the NVM device. Similarly, a negative gate pulse of (−10 V), which induces the partial storage of holes at FG-graphene, results in “ON” states with a higher ON current magnitude in the ReS$_2$ channel transistor that represents the “1” erase memory state. Next a positive gate pulse of (+10 V) removes the “1” memory states and brings the device current level to an initial “OFF” state corresponding to a low current level, which is program state “0.” The NVM operation and data reliability test of cyclic endurance measurements at ±10 V gate bias with 10 ms pulse width from another device is shown in Figure S9 (Supporting Information). The mechanisms of the writing, reading, and erasing processes are illustrated in Figure S16 (Supporting Information). A high positive (write/program) and a negative gate bias (erase) with a small drain bias (even at a zero-drain bias) can be used to tune the band alignment to pull electrons from ReS$_2$ and inject electrons into ReS$_2$, respectively. The read operation is performed under a zero gate bias and a low drain bias. Thus, different gate bias strengths can lead to switching to a different current level in a memory device, which can be operated as a multi-level memory device using electrostatic pulses with a range of bias voltages. Successive gate pulses constituting arbitrary electrical stress were used to switch the device between a high (ON) and a low (OFF) current state by applying a positive 10 V (write/program) pulse and a negative 10 V (erase) pulse, respectively (Figure 4c,d). Thus, the programming and erasing processes can be controlled by tuning the polarity of the control back-gate voltage. As a proof of concept, the two current states at a given gate voltage (±10 V) caused by hysteresis can be used as the two logic states of a solid-state memory. The various device parameters and figures-of-merit (FOM) of the multibit storage memory device are listed in Table 1.

### Table 1. Various parameters of the laser assisted multi-level non-volatile memory device.

| Parameters laser assist | Multilevel 2D flash memory |
|-------------------------|---------------------------|
| Channel material        | ReS$_2$                   |
| Barrier                 | h-BN                      |
| Charge storage/floatine gate | Graphene                |
| Carrier mobility (cm$^2$ V$^{-1}$ s$^{-1}$) | 10–20                     |
| On/off current ratio    | $10^{-3}$ to $10^{-4}$    |
| Memory window           | 38 V from ±30 V           |
| Operating power         | $V_g = 50$ mV/Pulse ± 10 V |
| Endurance               | >1000 cycles              |
| Retention time          | >$10^4$ s                 |
| Sample size             | Lateral size < 5 um Thickness = 10 nm |
| Laser used for multilevel | Wavelength 532 nm Intensity = 1–4 mW cm$^{-2}$ |

2.2. Opto-Electrostatic Memory Operation

The memory device has dual functionality; its memory can store both the electrostatic gate pulse state and incident laser pulse information. The laser illumination (532 nm, 4 mW cm$^{-2}$) can generate both positive and negative photocurrents in the NVM device depending on the applied gate bias for a fixed drain bias of 50 mV (Figure 5a). Zero and positive gate bias produces positive photocurrent (PPC) pulses, whereas a negative gate bias produces negative photocurrent (NPC) pulses under a successive ON/OFF cycle of laser pulse illumination. Laser illumination excites electrons from the valence band into the conduction band of ReS$_2$, and simultaneously the application of positive gate pulses for the program/write state induces electron storage in the FG-graphene. Laser irradiation under the programmed state of the NVM device does not allow the memory states to be switched as the charges at the FG-graphene induce holes in the conduction band of the ReS$_2$ channel, which recombines with the photogenerated electrons and makes the channel remain in the OFF state. Therefore, we observe no significant difference in photocurrent ON state ($I_p^{ON}$) with laser irradiation under a pulse positive gate bias (Figure 5b). Hence, the laser pulses do not allow us to program the NVM for multi-level program/write states. There was very little photocurrent, $I_p$, generation, and it decreased instantaneously after removal of the laser pulse, however the laser pulse was unable to switch the fully programmed state into a partially programmed state as shown in Figure 5b.

Here we describe photo-excited carrier generation and carrier separation under an electrostatic field. A positive gate bias makes it possible to store electrons in FG-graphene, which does not allow the extra photogenerated electron of the ReS$_2$ channel to tunnel through h-BN and the device has a PPC under laser illumination (Figure 5c). On the other hand, a zero gate bias has no inward or outward vertical electric field across the ReS$_2$/h-BN/graphene and thus produces a PPC under laser illumination (Figure 5d). The origin of the NPC phenomenon observed under a negative gate pulse and laser pulses in the ReS$_2$/h-BN/FG-graphene vdW heterostructure can be described in terms of the charge transfer between the floating layer graphene and the conduction channel ReS$_2$. Initially we assume the FG-graphene to be hole-doped, as seen in Figure S2b (Supporting Information), and the Fermi energy ($E_F$) shifts below the Dirac point at zero voltage and in a thermodynamic equilibrium condition. Additional positive gate voltage results in a shift of the charge neutrality point of FG-graphene to a more negative voltage. Therefore, photogenerated electrons from ReS$_2$ would not be able to occupy already filled energy states in FG-graphene via FN-tunnelling (Figure 5c). This results in a net PPC pulse under a laser pulse. Similarly, when we remove the gate bias (i.e., $V_g = 0$ V), electrons trapped in the FG-graphene do not allow a photoelectron to tunnel through h-BN. This again creates a PPC under pulse laser illumination (Figure 5d). The opposite scenario will be observed with a negative gate bias, where the gate induces higher hole doping at the FG-graphene. Initially we set the device in the erase state (sweep bias ranging from 40 to −40 V) then we applied a negative 20 V control gate bias, which made it possible to have a small drain current. The gate bias was set at −20 V, which lowers the $E_F$ level in the higher hole-doped FG-graphene.
(Figure 5e). When there is higher energy laser excitation with the applied drain bias, the generated hot electrons in the ReS$_2$ channel can have sufficient kinetic energy to cross over the h-BN barrier toward the control gate electric field. The photogenerated holes recombine with available free electrons in the ReS$_2$ channel thus reducing the dark current. Therefore, the separation of photogenerated electrons from ReS$_2$ to FG-graphene is not governed by the FN-tunnelling, which results in a sharp decrease in the dark current under laser irradiation. The electrons from the ReS$_2$ will recombine with the holes trapped in the graphene and increase the negativity of the graphene potential. Once the laser is in the “OFF” state, the electrons stored at the FG-graphene move to the ReS$_2$ via FN-tunnelling, which has a slow time response to retain the current state with the initial dark current value. This optical characterization further confirms the carrier transport mechanism and tunnelling phenomena in our NVM device.

Optical erasure is a highly energy efficient and non-contact method designed to achieve multi-level access in the memory device (inset Figure 6a). Optical erasure operations with different laser pulse intensities allow us to modulate the logic “1” operation of the memory device. Figure 6a shows four different accessible logic “1” states (i.e., L$_1$, L$_2$, L$_3$, and L$_4$) that were realized by varying the laser intensity of the incident laser pulse under an erasing condition, where the laser pulses were programmed and synchronized with the electrostatic gate pulses as shown in Figure 6b. Multi-level memory operation under varying gate pulses at the control gate shows readout erased pulses (ON current) drain current (Figure 6c). Now we see that we have a two-level erased state operation with the help of laser irradiation along with electrostatic pulses. We describe the result obtained with pulsed photo illumination cycles under a pulsed gate bias (Figure 6d). Binary number digits are used to represent three different memory states as “00”—fully write, “11”—fully erase, and “(11)$_{\text{after laser ON}}$”—partially erase state, which are labelled in Figure 6d with two different drain current levels, $I_d$ and $I_{d2}$, corresponding to two different erased states, respectively. The device is illuminated by a laser pulse (duration 1 s, 532 nm, intensity 4 mW cm$^{-2}$) under a zero-gate pulse after the programmed/write operation of the memory device, which results in a noticeable PPC as the photon-excited electrons in the ReS$_2$ channel contribute to the total current. A negative gate bias (~20 V) allows the NVM device to readout the drain current corresponding to the fully

**Figure 5.** Photocurrent generation mechanism in the NVM device with FG-graphene: a) $I_d$–$t$ response at a fixed $V_g$ of 50 mV for different $V_d$ values under multiple ON, OFF states of the laser (4 mW cm$^{-2}$, 532 nm), where the laser ON state is shown by blue shading. b) Dynamic response ($I_d$–$t$) of the device under both gate pulses (+30 V) as shown by the dashed red line, and the incident laser pulses (4 mW cm$^{-2}$, 532 nm) shown by the green line were used. c–e) Band alignment and positive photocurrent (PPC), zero gate bias, and negative photocurrent (NPC) mechanisms under positive, zero, and negative gate bias conditions, respectively.
erase state—“11.” On turning the laser on, the photocurrent ($I_p$) increases sharply and the $I_p^{ON}$ magnitude does not saturate at a fixed value; instead we observed a slow decrement at a 0 V gate bias. The slow degradation in the current state could be due to the presence of various interfaces (e.g., Au-ReS$_2$/ReS$_2$/h-BN) and/or defect trap states (ReS$_2$/h-BN and ReS$_2$/h-BN), where photogenerated carrier electrons become trapped in defect/interface states during light exposure. This is also observed in this NVM device at $V_g = 0$ V (Figure 5a) and in other reported optoelectronic memory devices.[18] There could be other factors such as defects and trap states at the ReS$_2$, h-BN, and ReS$_2$/h-BN interface, which maintains a decrement in the total readout drain current along with the $I_p^{ON}$ magnitude.[19] And turning the laser off does not simply remove the photocurrent component completely, instead the drain current saturates at a new (smaller) magnitude $I_p^{OFF}$, indicating a new readout current state corresponding to a partially erased state—“11’.” The optical erase process is fast at less than 10 ms (limit set in measurement instrument) as the current level immediately reaches a new accessible state 11’ after the laser has been turned off. For the fully programmed/write state (“00”), a positive gate pulse (+20 V) can be used as discussed above in Figures 3 and 4. Here we discuss the operational mechanism of the ReS$_2$/h-BN/FG-graphene optoelectronic memory. The photo-memory operation is investigated in this 2D heterostructure device by employing the modulation of the conductance of a multilevel ReS$_2$ field-effect transistor via the simultaneous application of laser pulses and electrostatic gate potential pulses. The main mechanism relies on the manipulation of a charging effect at the AF-graphene of the NVM device by the transfer of photogenerated and/or electrostatic induced free carriers of the ReS$_2$ channel through the insulating tunnel layer of h-BN. The offset (time: 2 s) synchronization of the laser pulse (fixed power and frequency) with a gate bias pulse (fixed voltage and frequency) allows the operation of a multibit memory storage device. Furthermore, synchronization of the gradual increase in the optical power of the laser pulses (light-controlled) with the gradual increase in the positive gate bias voltage (voltage-controlled) could lead to a more robust multifunctional device along with the ability to realize multibit photo-signalling memory and all-optical logic processing devices.

3. Conclusion

In summary, our work demonstrates the NVM operation of few-layer ReS$_2$/h-BN/FG-graphene-based FET devices. The memory device response can further expand the possibilities of multi-level application via both optical laser excitation and pulse gate bias. Few-layer direct gap ReS$_2$ acted as both a channel material and a light-absorption layer, which allowed us to demonstrate memory operation via opto-electrostatic coupling. Multi-level operation can be achieved depending on the laser intensity and number of pulses for a fixed intensity. We demonstrated multi-level memory operation via 532-nm laser pulse and electrostatic gate pulse coupling. The robustness and stability of the laser-assisted tuneable ReS$_2$/h-BN/FG-graphene memory show the potential for multibit information storage. Our results extend the possibility of multibit memory application via opto-electrostatic coupling in 2D heterostructures.
4. Experimental Section

Methods: Sample Preparation and Measurement Techniques: Standard dry-transfer techniques were used to prepare a hetero stack consisting of ReS2, h-BN, and graphene. Initially a SiO2 (285 nm)/Si substrate was used, which was treated with oxygen plasma (100% O2, 300 W, 20 Pa for 5 min) to remove contaminants and to induce a chemically and structurally modified surface layer on the SiO2 with functional silanol groups (Si–OH).[7] Then mechanically exfoliated graphene flakes from HOPG were deposited on the surface of the treated SiO2 at a substrate temperature of 180 °C.

Next an h-BN layer and ReS2 flakes were transferred to the top of the graphene/SiO2 sample using the transfer procedure shown in Figure S1 (Supporting Information), whereby a large uniform area of ReS2 flakes was fabricated and it was transferred to the top of the h-BN/graphene/SiO2/Si substrate. A SiO2 (90 nm)/Si substrate was spin-coated (3000 rpm, 60 s) with a water-soluble layer of polyacrylic acid (PAA) and then heated on a hotplate for 5 min at 110 °C. The second layer of PMMA-A6 was spin-coated (3000 rpm, 60 s) then heated on a hotplate at 150 °C for 5 min. Bulk ReS2 crystal (HQ Graphene supplier) was mechanically exfoliated on thermal tape (Nitto Denko, model NO319Y-4LSC) just before Au metal deposition. Au (100 nm thick) was sputtered directly onto the exfoliated ReS2/thermal tape using an electron-beam deposition technique. The fresh thermal tape was used to exfoliate the Au/ReS2 flakes from the Au/ReS2 coated thermal tape. Then, Au-mediated[24] exfoliated ReS2 flakes were pasted onto the PMMA/PAA/SiO2/Si substrate at 100 °C. The flake/PMMA was detached from the wafer in a water bath and then transferred to a polypropylene carbonate coated PDMS stamp holder. The target flake was aligned with the heterostructure of h-BN/graphene using a microscope. Contact connection. Standard electron beam lithography (EVL, ELS-7000, F125 KV) techniques were used to pattern the electrodes on the fabricated heterostructure device. An electron beam sputtering unit was used to deposit Cr/Au (Cr: 5 nm in 0.03 nm s deposition rate, Au: 50 nm, 0.15 nm s deposition rate in a high vacuum of 10 Pa). All electrical measurements were performed in the standard three-probe measurement configuration. The current–voltage (I–V), current–time (I–t), and all the optoelectrical characteristics (photocurrent–time) of the device were measured using an Agilent 2636A and a semiconductor device analyzer (Agilent B1500A) source–measurement unit. The gate pulses and I–t characteristics were recorded with a digital oscilloscope (Tektronix TBS1052B (50 MHz, 2 ch, USB)) and Keysight (Agilent) 33220A function generator which was synchronized with the source–measurement unit, was used to produce gate pulses. The devices were tested in a high-vacuum chamber (5 × 10 Pa) in a Lakeshore probe station at room temperature. The optical coupling with the memory device was achieved using a pulsed-wave laser beam emitted from a diode laser (532 nm, diode-pumped solid-state DPSS laser), which was synchronized with the source–measurement unit. A power meter (Ophir Optics, PD300) was used to measure light intensity. The laser beam irradiated the device directly through the transparent glass window of the Lakeshore vacuum chamber. An atomic force microscope (Olympus/SHIMADZU, Nano search microscope, model OLS3500/SFT-3500, dynamic scanning probe) and a Raman microscope (Nanophoton, model Ramanplus, 532 nm laser, with ×100–0.9 N.A. objective lens and 1200 lines mm grating) were used for the thickness measurement and sample characterization, respectively.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

graphene, heterostructures, memory, multibit, photoelectric memory, ReS2, two-dimensional materials

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