Improved Monolayer MoS$_2$ Performance With Two-Step Atomic Layer Deposited High-κ Dielectrics

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ABSTRACT Gate dielectric engineering is crucial to enable two-dimensional (2D) transition metal dichalcogenides (TMDs) for logic transistor applications. In this work, we demonstrate a uniform and pinhole-free bilayer high-κ fabricated on monolayer (1L) molybdenum disulfide (MoS$_2$) through thermal atomic layer deposition (ALD) without surface pretreatment. A thin low-temperature (75 °C) AlO$_x$ film deposited directly on 1L-MoS$_2$ mitigates 2D channel damage and serves as a nucleation and protection layer for high-temperature (250 °C) HfO$_x$ high-κ layer. The 1L-MoS$_2$ back-gate (BG) devices with low-temperature ALD capping show minor mobility degradation, less threshold voltage shift, smooth surface topography, and lower device variability compared to those with high-temperature ALD capping. These electrical differences are closely related to the coverage of the AlO$_x$ film at the initial ALD stage and the resultant quality of the AlO$_x$-MoS$_2$ interface after HfO$_x$ deposition. The underlying mechanism of ALD on the TMDs is proposed in terms of physical analysis and electrical findings. This work provides a practical and scalable ALD approach in gate dielectrics toward high performance 2D electronics.

INDEX TERMS MOSFET, high-κ dielectric materials, semiconductor materials.

I. INTRODUCTION

The success of the IC industry has relied on conventional silicon field-effect transistor (FET) scaling, however, fin scaling of Si-based transistors encounters great difficulty due to stronger surface scattering as the fin width goes thinner than 4 nm [1], [2], [3]. Therefore, two-dimensional (2D) layered materials, especially transition metal dichalcogenides (TMDs), have been explored as a promising channel material for the future ultra-small devices, thanks to their potent immunity against short channel effect (SCE) and relatively high mobility at an ultrathin physical thickness (6 Å). Not limited to the area of high performance logic transistors, several kinds of monolayer (1L) TMDs have a direct bandgap, also making them very suitable for a wide range of applications, from biomedical sensors to optoelectronic devices [4], [5], [6], [7]. Even so, an easily appreciable drawback for these TMDs is the susceptibility to ambient moisture and oxygen, requiring the need for an overlying encapsulation layer that could serve as the top-gate gate dielectrics in most cases [7], [8], [9]. As is well known, a high-quality, uniform, and smooth high-κ film is essential for sufficient electrostatic coupling of high performance TMDs devices. To achieve that, ALD is the most favorable deposition method owing to its superior controllability of thickness, uniformity, and conformity [10], [11].

Irrespective of these advantages, however, integrating TMDs with traditional ALD has been proved extremely challenging since the featuring chemically inert basal plane of TMDs would tend to hamper the reactants from chemisorption and often lead to a pinhole-like or island-like dielectric layer [12], [13], [14], [15]. In particular, on non-single crystalline TMD films, nucleations prefer to first happen mostly at the defect sites and/or grain boundaries instead of evenly on the entire film surface, which then results
in the exceedingly non-uniform deposition of dielectric materials during ALD [12], [16], [17]. The outcome will be that the dielectric is so leaky that it cannot act as a competent protection layer for the underlying TMDs or as a suitable insulator for devices. In order to solve this issue, many surface modification methods such as organic-based buffer layers, UV/ozone, plasma treatment, etc., have been studied [18], [19], [20], [21], [22], [23]. All approaches were performed with the purpose of creating surface functionalized sites on the TMDs surface or enhancing the precursor adsorption during the ALD process. However, these proposed schemes apparently have their own drawbacks. For example, the UV/ozone process contains strong oxidants that could oxidize the surface of TMDs, thereby causing deterioration of their intrinsic properties [21]. Damaging the topmost layer of TMDs is very likely to occur during all kinds of plasma treatment because ion bombardments are inevitable, even if the supply power is controlled to be mild [23].

Therefore, developing a reliable technique for depositing uniform good quality high-κ dielectrics by ALD in a manner of preserving the excellent properties of TMDs is worthy of further investigation. In this work, a scheme of two-step thermal ALD through temperature and purge time optimization was proposed and shown to be able to improve the non-uniform nucleation phenomenon often observed in the deposition of dielectric on the 1L-MoS₂. Without resorting to surface modification, our approach seems more straightforward and efficient since there was no increased integration difficulty and process complexity. We successfully deposited an ultrathin complete AlOₓ film via chemical vapor deposition (CVD) like growth at low temperatures. With the aid of this preexisting AlOₓ interfacial layer (IL), a high-quality and pinhole-free HfOₓ layer can be successively formed at a higher temperature.

With depicted satisfactory material and electrical properties of the bilayer composite high-κ dielectric on the 1L-MoS₂, we think our developed technique is relatively mature and practical for depositing well behaved thin dielectrics on the TMDs.

II. EXPERIMENTAL SECTION

Fig. 1(a) indicates the critical steps of the 1L-MoS₂ device fabrication. In this study, the 1L-MoS₂ flakes were grown on a c-plane sapphire substrate by chemical vapor deposition (CVD) and transferred onto 100 nm thermally grown SiNₓ/ highly p-doped Si substrate via the semi-dry approach. First, the MoS₂ flake on the sapphire substrate was coated with poly (methyl methacrylate) (PMMA), and the thermal release tape (TRT) was pressed onto the PMMA-coated substrate. Next, the sample was placed in 80°C buffered oxide etchant (BOE) to peel the TRT/PMMA/ MoS₂ assembly off from sapphire, and the assembly was dried out in an N₂ environment. Then the assembly was attached to the target SiNₓ/Si substrate and baked at 150°C to release the TRT. Last, the sample was immersed in the acetone overnight to remove PMMA. The source/drain metal contacts were defined by optical lithography, followed by e-gun evaporation of 40 nm Ni and the standard liftoff process. The MoS₂ back-gated (BG) devices were measured in vacuum before dielectric encapsulation.

After measurement, the devices were capped with three different ALD conditions to study the low-temperature physisorption and the high-temperature chemisorption on MoS₂, as listed in Fig. 1(b). Trimethylaluminum (TMA) and tetrakis-(dimethylamino)-hafnium(IV) (TDMAH) were used as the ALD precursors for aluminum and hafnium, respectively, and H₂O was used as the oxidant. The ALD cycle numbers were kept at 10 cycles for the AlOₓ first layer followed by 70 cycles for the HfOₓ second layer, but with various deposition temperatures. We deposited the AlOₓ layer at 75°C and 250°C and the HfOₓ layer at 120°C and 250°C. The low deposition temperature of HfOₓ was set at 120°C instead of 75°C owing to the decomposition efficiency of the TDMAH precursor. For simplicity, conditions 1, 2, and 3 were denoted as LL, LH, and HH, respectively, indicating the ALD temperature of the bilayer high-κ. Note that p-type Si (100) substrates also underwent the same ALD conditions to fabricate Metal-oxide-Semiconductor (MOS) capacitors as the reference samples.

The schematic of the final MoS₂ BG transistors is displayed in Fig. 1(c). Both MoS₂ BG transistors and Si MOS capacitors were measured using the Keysight B1500A system to understand the electrical characteristics of the bilayer high-κ dielectric. Moreover, atomic force microscopy (AFM), transmission electron microscopy (TEM), and Raman spectroscopy were employed to examine surface morphology and ALD film quality of the LL, LH, and HH conditions.

III. RESULTS AND DISCUSSION

To better understand the influence of changing the ALD process scheme on our targeted dielectric system, we started our experiments with the fabrication of the conventional Si MOS capacitors and studying their electrical properties by capacitance-voltage (C-V) measurement. Fig. 2(a), (b),
and (c) show the TEM images of the Si MOS capacitors with LL, LH, and HH capping dielectrics, respectively. The LL sample had a thick bilayer thickness of $\sim$11.6 nm with a blurry high-$\kappa$/Si interface; on the contrary, the HH sample had a thinner bilayer thickness of 10.2 nm with a sharp interface. An increase in thickness was believed to be closely related to the enhanced physisorption of the metal precursors by lowering the AlO$_x$ deposition temperature to 75 °C [24], [25]. Shortening the purge time from 15 sec to 2 sec between precursor and oxidant pulses also had a high possibility of increasing the concentration of precursors and oxidants in the vicinity of the sample surface, leading to the CVD-like deposition behavior in the LL samples [26], [27], [28]. Besides, it should be noticed that the AlO$_x$ interfacial thickness in the LH sample became thinner as compared to that in the LL sample. This observation might be attributed to the densification of the AlO$_x$ film or further interaction with the following HfO$_x$ deposition at 250 °C.

The C-V characteristics of the Si MOS capacitors under three ALD conditions are shown in Fig. 3(a) and (b). First, a higher accumulated capacitance was observed with increasing the deposited temperatures, arising from the fact that ALD deposition at high temperatures had a higher film density, lower carbon-related contamination, and great opportunity to achieve the ideal stoichiometry [29]. This statement is consistent with the previous studies that the high-quality AlO$_x$ and HfO$_x$ can be achieved with 250 °C deposition temperature [29], [30], [31]. Furthermore, as shown in Fig. 3(c), the increasing trend of the effective dielectric constant ($\varepsilon_{\text{eff}}$) from 12 to 13.4 when the deposition condition changed from LL to HH was another good piece of evidence supporting this conclusion. Second, only the C-V curve of the LL sample shifted negatively and significantly, implying that the low-temperature AlO$_x$ - HfO$_x$ bilayer was oxygen rich owing to the higher density of hydroxyl groups [30]. This might have an impact on the interfacial quality, as a small hump was noticed in the low-frequency (1 kHz) C-V curve. We roughly estimated the density of interface states ($D_{it}$) through the single frequency conductance method [32]. The $D_{it}$ values of the LL, LH, and HH samples were $6.8 \times 10^{11}$, $3.4 \times 10^{11}$, and $4.8 \times 10^{11}$ cm$^{-2}$eV$^{-1}$, respectively. A larger $D_{it}$ value was characterized in the LL sample as expected and the LH sample had the lowest $D_{it}$ value among all samples. A relatively low C-V hysteresis width was also noticed in the LH sample. We further analyzed the breakdown field ($E_{BD}$) of these dielectric samples, as plotted in Fig. 3(c). Both LL and LH samples exhibited the identical $E_{BD}$ and the HH sample had a larger $E_{BD}$. This indicates that the AlO$_x$ IL dominates the dielectric strength. With the measured capacitance and the physical thickness from the TEM images, the values of the capacitance equivalent thickness (CET) obtained in the LL, LH, and HH bilayer dielectric stacks are 3.77 nm, 3.36 nm, and 2.97 nm, respectively. The results of Si MOSCAP showed
a decreasing trend in CET with increasing ALD temperatures, which can be attributed to higher dielectric constant and reduced physical thickness in the formed ALD dielectric bilayer. In summary, the LH sample showed better dielectric quality in terms of both $\varepsilon_{\text{eff}}$ and $D_{\text{it}}$ on the Si substrate. These observations also provided a preliminary trend line when depositing these ALD conditions onto the monolayer MoS$_2$ film.

For the 1L-MoS$_2$ channel, we examined the physical effect of encapsulating dielectric on intrinsic MoS$_2$ quality through Raman analysis using a 532 nm laser, as displayed in Figs. 4(a) and (b). Raman spectroscopy has been widely used to characterize TMDs properties since the shift of Raman peaks strongly depends on external strain, doping, etc. [33], [34]. The pristine 1L-MoS$_2$ showed typical Raman peaks of in-plane $E$ mode and out-of-plane $A_{1g}$ mode at 385 cm$^{-1}$ and 404 cm$^{-1}$, respectively [35], [36]. Interestingly, the $A_{1g}$ peak in Raman was blueshifted after HH dielectric capping, but redshifted after LL dielectric one. The shift of the $A_{1g}$ peak in MoS$_2$ towards different directions might suggest different doping polarities [37], [38], [39]. Therefore, the HH and LL dielectrics were speculated to induce p-doping and n-doping on the underlying MoS$_2$ film, respectively. It should be pointed out that the changes in Raman spectra could be related to not only doping and strain but also the modification of the interface properties. Interfacial defects can lead to the confinement of phonon correlation length since the interfacial defects interfere with the spatial translation invariance of the lattice structure. Therefore, the phonon confinement model is employed to explain the correlation between the changes and the interface defect [40]. From the phonon confinement model, we can predict that the Raman peak will be shifted and broadened [41].

Surprisingly, in Fig. 4(b) no Raman peak at 820 cm$^{-1}$ was noticed, suggesting no detectable formation of MoO$_3$. Even so, the changes in Raman observed in LL and HH samples still indicate certain changes in the intrinsic property of MoS$_2$, but there was no notably shift in Raman peaks for the LH sample, suggesting that the intrinsic properties of MoS$_2$ were hardly affected after LH dielectric deposition. Above these findings could be examined by the following material and electrical analyses.

Fig. 5(a)–(f) illustrate TEM and AFM images of the 1L-MoS$_2$ channel with LL, LH, and HH capping dielectrics, respectively. From the cross-sectional TEM image, the AlO$_x$/HfO$_x$ bilayer high-$\kappa$ can be identified in both the LL and LH samples, while only a single layer of HfO$_x$ was found in the HH sample. The surface morphology of the dielectric layer also became smooth when depositing film at a lower temperature, especially the first ALD layer on TMD. As confirmed by AFM in Figs. 5(d)–(f), the phenomena of discontinuous film and pinholes could be diminished by lowering the first AlO$_x$ deposition temperature down to 75 °C. The surface would be further smoothed by lowering the deposition temperature of the second HfO$_x$ layer to 120 °C. The root-mean-square (RMS) roughness was measured to be 0.47, 0.78, and 1.27 nm after LL, LH, and HH dielectric deposition, respectively. As a consequence, a uniform and pinhole-free bilayer dielectric was realized on MoS$_2$, mainly by virtue of the low-temperature physisorbed AlO$_x$ film [13], [42]. On the contrary, a high temperature of 250 °C endowed the precursor with more thermal energy, resulting in a higher probability of escaping physisorption potential well, i.e., the precursor desorbed more easily from the surface [13], [27], [43], [44], [45]. The high desorption rate of precursors on the dangling bond free MoS$_2$ leads to
the formation of islands or clusters eventually. As a result, the surface morphology of MoS$_2$ devices after HH dielectric deposition was pinhole-like and non-uniform, as depicted in Fig. 5(c) and (f). According to TEM and AFM results, it is then faithful to conclude that the physisorption of ALD precursors does play a crucial role in forming an uninterrupted continuous IL on the intact MoS$_2$ surface with the lack of the dangling bonds.

As known, the van der Waals (vdW) structure of TMDs reduces the screening ability and is susceptible to the surface impurities, thus successively producing stronger interfacial Coulombic scattering in the fabricated devices. To get further insight into the high-$\kappa$ dielectric and interfacial qualities of the MoS$_2$ devices, the drain current ($I_D$) versus back gate voltage ($V_{BG}$) characteristics are shown in Figs. 6(a)–(c). First of all, the pristine MoS$_2$ films showed identical device performance in these three samples before the dielectric encapsulation. With increasing deposition temperature in either AlO$_x$ or HfO$_x$ layer, the device depicted decreased on current ($I_{ON}$) along with the positive threshold voltage ($V_{TH}$) shift. Accordingly, the HH sample showed the worst $I_{ON}$ degradation and the largest $V_{TH}$ shift after dielectric capping among the three samples. Through using the Y-function method, the extracted intrinsic mobility is reduced by approximately 60% from 8.7 to 3.5 cm$^2$/V·s after capping the HH bilayer, but only slightly degraded ($< 5\%$) from 8.7 and 6.2 cm$^2$/V·s to 8.6 and 5.9 cm$^2$/V·s after the LL and LH bilayers capping, respectively [46]. Severe mobility degradation probably resulted from MoS$_2$ damage during ALD. Due to the fact that MoS$_2$ tends to interact with ambient oxygen and moisture, not to mention atomic oxygen, so exposing MoS$_2$ to a 250 °C ALD chamber filled with H$_2$O precursors is likely to cause surface oxidation or deterioration. As a consequence, a less steep linear $I_D$-$V_{BG}$ curve was thus observed as in Fig. 6(c) [47], [48]. We also observed electrical variability in the devices after ALD capping. A considerably large mobility variation up to 40% in the HH sample was found, which was only 15% in the LL and LH samples, because the deterioration of the intrinsic MoS$_2$ properties affected by HH dielectric capping happened randomly. And a positive $V_{TH}$ shift of $\sim$15 V was clearly seen, indicating an obvious p-doping effect, as evidenced by the observation of blueshift in the A$_{1g}$ Raman peak, which was induced as the HH dielectric capping on MoS$_2$ was employed. Low-temperature ALD process aids to reduce the performance variability in devices. It is concluded that among three ALD conditions, the LH bilayer has the least impact other monolayer MoS$_2$ channel with the best yield in terms of the back-gated device characteristics.

Based on the material and electrical analyses, a preliminary ALD mechanism of the LH bilayer dielectric formation on MoS$_2$ is proposed, as the schemes in Figs. 7(a)–(d). During the first few ALD cycles, metal precursors and oxidants, i.e., TMA and H$_2$O in this study, can adsorb easily onto the surface of MoS$_2$ via physisorption. But, these physisorbed molecules also detach easily by external energy sources such as thermal heating or long purge time since the bond strength of physisorption is weak or the intermolecular distance is far [49], [50]. In other words, adopting low temperature and short purge time can facilitate the formation of a few AlO$_x$ islands at the early stage of the ALD process, as shown in Fig. 7(b). Such a CVD-like process does form a continuous AlO$_x$ ultrathin layer on MoS$_2$, which acts as a protective IL, enabling HfO$_x$ film to deposit at high temperature while preserving MoS$_2$ quality. It is known that a higher ALD temperature promotes chemisorption rather than physisorption during ALD, thereby achieving a denser HfO$_x$ high-$\kappa$ film with better quality. According to the Lennard-Jones (LJ) potential curves, the attraction force of chemisorption is relatively strong ($\sim$1 eV) with
a close distance (<3 Å) as compared to that of physisorption (≈0.04 eV) with a far distance (>3 Å) [51]. The calculations above in the LJ potential model can support the perspective of the ALD deposition of AlOₓ and HfOₓ bilayer here. It is believed that the two-step bilayer high-κ dielectric developed in this work also represents a key enabling step for high-performance top-gate TMD transistors.

IV. CONCLUSION

We systematically studied the effect of ALD temperatures in two-step high-κ dielectrics on the 1L-MoS₂ BG device characteristics. It was found that depositing the first layer of AlOₓ at a low temperature of 75 °C with a short purge time mitigates the degradation of MoS₂ mobility. The AlOₓ seeding layer also facilitated uniform deposition of the HfO₂ second layer at a high temperature of 250 °C during ALD. The resultant surface roughness of the ALD bilayer high-κ can be reduced from 1.27 nm to 0.78 nm. Moreover, MoS₂ devices with the developed LH bilayer capping had a minor Iₚ/vat reduction and V_TH shift, different from the results of a large Iₚ/vat deterioration and positive V_TH shift for devices with the HH bilayer capping. The improved electrical performance could be explained by the enhanced physical adsorption of ALD precursor on the dangling bond free TMDs. The possible ALD mechanism was also depicted to discuss the physics of dielectric deposition on the TMDs. This study successfully presents a two-step thermal ALD process on the TMDs and further gives a guideline for forming good quality high-κ dielectric on other semiconductor materials with the chemically inert surface.

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