Realization of LNA and Mixer Using CMOS 0.18µm Technology for 3.1 to 10.6 GHz

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Abstract. In this paper, low noise amplifier and mixer circuits are realized using 0.18µm CMOS technology in the frequency range of 3.1 to 10.6 GHz. LNA circuit uses the cascade topology with source degeneration technique, which help in reducing the non-linearity in the circuit. The current reuse topology is used to decrease the biasing voltage and hence to decrease the power consumption in the circuit. Realized circuit simulated in 0.18µm technology and various results shows highest gain S21 is 19.982dB and has the positive value in the entire frequency band, minimum NFmin is 1.270dB occurs at 1.27GHz and the highest NFmin is 3.4dB. S11 i.e. input reflection coefficient is -31.670dB and it is negative throughout the entire frequency range while the reflection at output port is report to be -7.449 dB. The resistive feedback topology helps in getting the flat gain in the frequency. Mixer circuit is also realize in 0.18µm CMOS technology, which uses current bleeding topology. Transformer help in converting the single ended signal into differential format. Maximum value of gain is 6.584dB, gain is positive in the entire RF frequency range, S11 i.e. the reflection at port1, which give the negative values in the entire frequency band, simulation of S12 i.e. leakage between the port 1 and 2 has negative values in the entire frequency band means proper isolation between the ports. The future work can the realization of the superheterodyne receiver in UWB band.

1. Introduction
The first block in ant receiver system is the low noise amplifier, which increases the power level of signal without introducing the much noises. The next block is mixer circuit, which is used to lower the frequency of incoming signal i.e. called as the down conversion mixer.

![Figure. 1 RF Receiver Systems](image-url)
The performance of receiver depends on the performance of LNA, mixer and local oscillator. Block diagram of receiver system is shown in Figure 1[12]. Noise figure, gain, s-parameters etc. are the parameters of LNA and mixer. The trade-off between these parameters makes difficult to design the circuit. The low noise amplifier should have low noise figure in order to maintain the good quality of the signals, the requirement of low power consumption makes the circuit compact and cheap as well as saving the environment energy [1]. Now the high speed requirement has to be fulfilled by the designed circuits. The band of 3.1-10.6 GHz given by FCC for the ultra-wideband systems [13]. The ultra-wideband system requirement is the low power signal strength so that they must not get overlap with the other signal presented in the environment. The data rate of ultra-wideband systems is the approximately 100Mbps and has the bandwidth greater than 500MHz. The different techniques to improve the LNA performance parameters are discussed here. Basic topology is common source stage (CS) [6] in which gain is given by \( A_V = -g_m R_D \); \( g_m \) represents transconductance while \( R_D \) represent drain connected resistance. By increasing \( R_D \) or \( g_m \); gain gets improved. But it is having the disadvantage of poor matching.

![Figure 2: (a) Inductive Load CS (b) Resistive Feedback CS](image)

Inductive Load CS [7] is used for good matching as shown in Figure 2(a). In resistive feedback CS stage shown in Figure 2(b), drain and gate connected via feedback resistance provide circuit stability but has high NF. Bandwidth is increased using this topology.

Input impedance is decreased in Common gate (CG) topology [8] as shown in Figure 3(a). Gain headroom is occurred in CG topology, \( R_{in} = \frac{1}{g_m} \).

![Figure 3: (a) CG Topology (b) Distributed Amplifier Topology](image)

\( L_1 \) helps in resonating MOS capacitance at output [4] in which \( A_V = \frac{R_L}{2 R_c} \). Distributed amplifier as shown in Figure 3(b), has MOS connected in series for the purpose of high gain and bandwidth at the cost of high power NF. Another technique is source degeneration as shown in Figure 4(a) in which inductor at source cancel MOS parasitic capacitances and improve linearity at the cost of large area and power consumption.
BPF technique, LC filter helps good input matching but has narrow bandwidth as shown in Figure 4(b). So, different LNA topologies trade off in their parameters. Gain, NF, linearity, current consumption are also the parameters of mixer and it is followed by IF amplifier whose performance also decide by it. Trade-off between these parameters are to be optimize by using the biasing metric, the decrement in one parameter degrades the performance of mixer circuit. $G_m$ boost technique is use to increase the gain of the circuit but which results in increasing the power consumption of the circuit [14]. Different mixer techniques such as body bias, source degeneration, current reuse, current bleeding etc. to improve the mixer performance. Ultra-wideband system use the frequency band of 3.1GHz to 10.6 GHz for transmitting the data at high rate. But the power of the signal should be such that they must not interfere with the signals which are in the license band[17]. In order to produce the correct IF signal, oscillator play a very important role. It must provide the sustained oscillations for correct output. Barkhausen criteria must be followed for sustained oscillation that is the multiplication of forward gain and feedback gain should be equal to one and total phase provided by the amplifier and feedback circuit should be 0°. The intermediate frequency is the difference of RF signal and oscillator signal. Various oscillator circuits such as crystal oscillator, LC and RC oscillators whose application depends on the frequency usage. RC oscillators use for the frequency range of KHz while LC circuits use for frequency range of MHz. Colpitt and Hartley are types of LC oscillator circuits. Hartley circuit has one capacitors and two inductors in the feedback path and oscillation frequency is $f = \frac{1}{2\pi \sqrt{(L_1 + L_2 + 2M)C_1}}$. Figure 5 shows the Hartley oscillator circuit with common source amplifier.

![Hartley Oscillator Circuit](image)
2. LNA Circuit Realization
First low noise amplifier circuit is realized using 0.18µm CMOS technology and the circuit is shown in Figure 6. Various components uses are as follows: Vi the input signal received from the antenna and Rs is the source resistance, C1 the coupling capacitors use to block DC and pass only the ac component, R1 is providing the resistance shunt feedback, M1 and M2 form the cascade connection also using the current reuse topology to reduce the power consumption of the circuit. L1 providing the source degeneration technique used to overcome the effect of MOS parasitic capacitance. Vdc use for biasing the MOSFET, M1 MOS is in common source configuration while M4 is providing the biasing to M3 transistor, MOS M3 is connected in common drain configuration also known as source follower, inductor L2 and L4 helps in getting the constant gain throughout the entire frequency. Small signal model of the realized circuit is shown in Figure 7.

![Figure 6: Realized LNA Circuit](image)

![Figure 7: Small Signal model of Realized Circuit](image)

Realized circuit simulated in 0.18µm technology and various results are shown in Figure 8. The highest gain S21 is report to be 19.982dB and has the positive value in the entire frequency band as shown in Figure 8(a), minimum NFmin is at 1.270dB occurs at 1.27GHz and the highest NFmin is 3.4dB as shown in Figure 8(b).
Figure 8: Simulation Results for Realized LNA circuit (a) S21 w.r.t. frequency (b) Noise Figure w.r.t. frequency (c) S11 with respect to frequency (d) S22 with respect to Frequency

S11 i.e. input reflection coefficient is -31.670dB and it is negative throughout the entire frequency range while the reflection at output port is report to be -7.449 dB as shown in Figure 8 (c), (d) respectively. The resistive feedback topology helps in getting the flat gain in the frequency

3. Mixer Circuit Realization

Mixer circuit realized in 0.18µm CMOS technology, the realized circuit is shown on Figure 9. Gilbert cell is the basic of mixer. MOS M1 and M2 amplifies the signal and do the conversion into current. M3 to M6 MOS use the switching purpose and output intermediate frequency voltage is in differential format. Source degeneration topology help is providing the linearity in circuit. Transformer help in converting the single ended signal into differential format. At the output port, second transformer change the differential signal into the single ended format. M9 and M10 MOS are forming the current mirror. MOS M11 connected in common source configuration to maintain the MOS M1 and M2 in saturation region.
Figure 9: Realized Mixer Circuit in 0.18µm CMOS Technology

Figure 10: Simulation Results of Realized Mixer Circuit: (a) Down Conversion Gain w.r.t. RF Frequency (b) S11 w.r.t. RF Frequency (c) NF w.r.t. RF Frequency (d) S12 w.r.t. RF Frequency
Simulation results for realized mixer shows in Figure 10(a) that the maximum value of gain 6.584dB and gain is positive in the entire RF frequency range. Figure 10(b) give the simulation for S11 i.e. the reflection at port1, which give the negative values in the entire frequency band. Figure 10(c) shows the simulation of noise figure while 10(d) shows the simulation of S12 i.e. leakage between the port 1 and 2 and has negative values in the entire frequency band means proper isolation between the ports.

**Conclusion**

The low noise amplifier and mixer circuits are realized using 0.18µm CMOS technology in the frequency range of 3.1 to 10.6 GHz. LNA circuit uses the cascade topology with source degeneration technique, which help in reducing the non-linearity in the circuit. The current reuse topology is used to decrease the biasing voltage and hence to decrease the power consumption in the circuit. Realized circuit simulated in 0.18µm technology and various results shows highest gain S21 is 19.982dB and has the positive value in the entire frequency band, minimum NF min is 1.270dB occurs at 1.27GHz and the highest NF min is 3.4dB. S11 i.e. input reflection coefficient is -31.670dB and it is negative throughout the entire frequency range while the reflection at output port is report to be -7.449 dB. The resistive feedback topology helps in getting the flat gain in the frequency. Mixer circuit is also realize in 0.18µm CMOS technology and maximum value of gain 6.584dB, gain is positive in the entire RF frequency range, S11 i.e. the reflection at port1, which give the negative values in the entire frequency band, simulation of S12 i.e. leakage between the port 1 and 2 has negative values in the entire frequency band means proper isolation between the ports. Future work can be the realization of the super-heterodyne receiver in UWB band.

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