High Productivity DRIE solutions for 3D-SiP and MEMS Volume Manufacturing

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Abstract. Emerging 3D-SiP technologies and high volume MEMS applications require high productivity mass production DRIE systems. The Alcatel DRIE product range has recently been optimised to reach the highest process and hardware production performances. A study based on sub-micron high aspect ratio structures encountered in the most stringent 3D-SiP has been carried out. The optimization of the Bosch process parameters has resulted in ultra high silicon etch rates, with unrivalled uniformity and repeatability leading to excellent process. In parallel, most recent hardware and proprietary design optimization including vacuum pumping lines, process chamber, wafer chucks, pressure control system, gas delivery are discussed. These improvements have been monitored in a mass production environment for a mobile phone application. Field data analysis shows a significant reduction of cost of ownership thanks to increased throughput and much lower running costs. These benefits are now available for all 3D-SiP and high volume MEMS applications. The typical etched patterns include tapered trenches for CMOS imagers, through silicon via holes for die stacking, well controlled profile angle for 3D high precision inertial sensors, and large exposed area features for inkjet printer heads and Silicon microphones.

1. Introduction

The latest developments in MEMS, Wafer Level Packaging [1] and Active and Passive electronic devices using DRIE have recently allowed the introduction of superior product performances. The future of DRIE technology is now widening thanks to an ever-increasing recognition as an enabling technology. The use of DRIE in high volume applications like mobile phones or automotive sensors is now a reality and manufacturers are always looking for ways to increase capacity by improving throughput and controlling costs.

Unlike CMOS applications, etching high aspect ratio structures of up to 100:1 [2] with DRIE, suffers from long process times that result in throughputs of only few wafers per hour. The first way to improve throughput is to increase the etching rate with Bosch process [3], and it is obvious that the latest announced etching rates are not sufficient; in this paper, experimental works will be presented showing that 25-30 µm/min etching rate will be accessible. Another way to improve the overall productivity of the DRIE step is to optimize production parameters such as process uniformity, process stability, process yield, system production time, reduction of consumable and scheduled...
maintenance. Solutions that result in dramatically increasing the wafer throughput and significantly reducing the C.o.O. are being presented in this document.

2. Experimental set up

The experiments in this study have been carried out on an Alcatel AMS 200 “I-Productivity” DRIE etching tool, optimized for high volume manufacturing.

The Alcatel AMS 200 “I-Productivity” is a new generation after the Alcatel “I-Speeder” series and is fitted with an Alcatel patented high-density ICP type plasma source. The source is fixed on top of a diffusion chamber surrounded by a number of permanent magnets. This arrangement allows an optimized process gas delivery as well as high ion density uniformity. The Alcatel AMS 200 “I-Productivity” can be equipped with mechanical or electrostatic wafer clamping solutions. All of the experiments have been performed with patterned silicon wafers of 150 mm diameter size.

The Alcatel DRIE tools are offered with several types of processes. The most popular one is the well known Bosch process based on the use of alternative steps of SF6 and C4F8. The SF6 is used to etch the Silicon, and the C4F8 to passivate the surfaces and to achieve the anisotropic etch of the Silicon. This alternation of etching and passivation steps results in a waving side wall profile, also commonly called scalloping. With the control of the gas flows and pressures, this scalloping can be significantly reduced, to as low as 14 nm.

3. Solutions for a higher process productivity

3.1. Pushing up Etch Rate to 25-30 µm/min

In 2002, the “I-Speeder” Project [4] developed with Bosch and PerkinElmer resulted in tools which had the fastest etch rate for Silicon etching in the market. The latest “I-Productivity” project has resulted in further improvement of the etch rate and is now exceeding 25 µm/min., with an excellent etch depth uniformity (Figure 1).

![Figure 1: Etch rate versus exposed area](image-url)
3.2. Improving the process YIELD

To achieve a high process yield requires a good depth uniformity as well as good profile uniformity. Such performances can only be obtained with a well-designed process chamber, which leads to a uniform gas phase, uniform plasma, and uniform temperature range across the wafer.

3.2.1. Uniform gas phase

Thanks to its important market share in the high demanding microelectronics business, Alcatel Vacuum Technology has a well-recognized position in vacuum expertise. Part of this success is due to the extensive R&D division, and the use of simulation software to achieve the best pump performances possible. One of these 2D software programs [5] has been used to study the neutral flows at the wafer level for different process regimes on the AMS 200 “I-Productivity” tool. It has also allowed to optimize the Bosch process in order to achieve the best etch rate and with high etch depth uniformity (Figure 2: Plasma simulation). Optimization simulations now show excellent gas velocity uniformity all above the wafer surface.

![Plasma condition 1: Low uniformity](image1)

![Plasma condition 2: High uniformity](image2)

**Figure 2**: Plasma simulation of the SF6 gas velocity (ms⁻¹) in the chamber for 2 different process conditions

3.2.2. Uniform plasma

The AMS 200 “I-Productivity” is equipped with the patented high density ICP type plasma source. The source is fixed on top of a diffusion chamber surrounded by permanent magnets. The inherent non uniformity of ICP plasmas has been dramatically reduced through both chamber dimensioning and magnetic multipolar confinement. Magnet strength and spacing together with inner chamber diameter have been optimized regarding the ion uniformity while providing the maximum pumping speed for processing 8” wafers.

With an 8” wafer, the plasma potential uniformity is better than 5%, which also leads to a comparable etch depth uniformity.
3.2.3. Uniform Temperature

The surface temperature at the wafer level is a key parameter to achieve good depth and profile uniformity. Furthermore, lots of 3D-SiP applications have a requirement in terms of maximum process temperature allowed, due to the type of devices and components on the wafer.

From all the energies arriving at the wafer surface, the most important one is the energy coming from the chemical reaction of the Silicon with the fluorine gas:

\[
\text{Si (s)} + 4\text{xF (g)} \Rightarrow \text{SiF}_4 \text{ (g)} \quad \Delta G_0 = 435 \text{ Kcal/mol}
\]

This energy (PE) is proportional to the amount of Si removed by time and surface unit:

\[
P_E = \frac{\text{Si mol}}{(T \times \text{Mmol})} \times \Delta G_0
\]

with : Mmol: The molar mass (28g/mol), Si mol: quantity of removed Si, T: time, \( \Delta G_0 \) is the chemical reaction

So, \( P_E \) is directly proportional to the etch rate and the exposed area. That means that an significant increase of the etch rate requires an efficient chuck design to evacuate all the heat generated at the wafer level.

In order to evacuate all this heat and achieve the best uniformity of temperature, Alcatel has designed a “P” type electrostatic chuck (ESC) with an innovative design, allowing to adjust the temperature regarding the wafer patterns. For a given process, the “P” type ESC, gives a uniform temperature of ±0.15 degree across the wafer, with an excellent thermal conductivity. The improved cooling capability of the ESC “P” allows the development of some new processes leading to higher etch rates.

3.2.4. Reduced edge exclusion

An another way to increase the process yield is to reduce the edge exclusion, in order to increase the number of properly etched features. The new ESC “P” has been specially designed to avoid any distortion of the plasma sheath at the wafer edge (Figure 3), and therefore has an edge exclusion not exceeding 3 mm.

![Fig. 3: Reduced edge exclusion](image-url)
4. Solutions for an increased production time

4.1. Clean Free Process Chamber

The C4F8 used for the passivation during the Bosch process creates a polymer that is deposited on all the cold surfaces in the process chamber. The accumulation of this polymer on the chamber wall used to oblige some frequent mechanical cleanings, leading to downtime, and conditioning procedures. In order to avoid any wet cleaning to remove the polymers from the process chamber wall, Alcatel developed a unique patented heated liner [6], that allows the control of the temperature to avoid the deposition of polymers. This unique design avoids an excessive warming up of the outer part of the process chamber, minimizing the electrical consumption.

Furthermore, the heated liner maintains a constant plasma condition of the chamber wall, resulting in a Silicon etch rate that is very stable even after multiple plasma hours (Figure 4).

![Etch depth=f(Nb of wafers)](image)

**Figure 4**: Etch stability within ±3%

4.2. Reduced C.o.O.

For high volume production, the Cost of Ownership is an important parameter to take into account. More often, The DRIE ICP is used to etch micron or sub-micron features to an etch depth between a few microns up to hundreds of microns. Compared to typical microelectronics processes, the duration of the etch is usually longer even with etch rates ten to hundred times faster. The most efficient way to reduce the C.o.O. is to lower the running costs of the tool.

There are several ways to do this, one of them is to increase the etch rate. An another way is to reduce the C4F8 consumption, a quite expensive gas. As the C4F8 step is more efficient at high pressure, the hardware was modified in order to allow a different pressure for the SF6 and the C4F8. The C4F8, therefore, can be set up at high pressure whatever the value of SF6 pressure. Another way to improve the C.o.O. is to increase the availability of the chamber for process by using the patented heated liner that reduces the cleaning frequency and duration. The low electrical consumption of the heated liner further adds to the low C.o.O. In addition to the above hardware improvements, the tool design was also significantly modified to reduce the cost and number of spare parts.
5. Benefits for a high volume application

5.1. Integration of passive components

All the benefits of the AMS 200 “I-Productivity” DRIE etcher were notably applied to a high volume application for the integration of passive components. Compared to the previous AMS 200 “I-Speeder”, the AMS 200 “I-Productivity” improved the etch rate by 43%, and thanks to the reduction of the cleaning frequency the throughput was increased of 83%. The higher range of available process allowed for a decrease of 42% in the consumption of the expensive C₄F₈ (Figure 5).

|                | AMS 200 “I-Speeder” | AMS “I-Productivity” | Improvement |
|----------------|---------------------|----------------------|-------------|
| Etch duration  | 15min               | 8min 30s             | 43%         |
| Etch drift     | -9%                 | ±2%                  |             |
| Throughput     | 300 wafers per week | 550 wafers per week  | 83%         |
| C4F8 consumption | 1.964 l/wafer | 1.133 l/wafer      | 42%         |

Figure 5: Benefits of the AMS “I-Productivity”

5.2. Other applications

The AMS 200 “I-Productivity” benefits can also be applied to the high volume MEMS market, such as Silicon microphone or inkjet head applications, but also power devices, passive components, and the emerging 3D applications (interconnection, Cmos Imager…).

6. Conclusion

The latest developments and improvements applied to the Alcatel AMS 200 “I-Productivity” result in much higher production performances, thanks to lower etch drift, extended cleaning frequency, limited edge exclusion, higher etch rate, better process stability and higher etch uniformity. It is now possible to offer an unrivaled set of hardware and process solutions, using AMS 200 “I-Productivity” DRIE tools for high volume manufacturing, applied to 3D-SiP and MEMS.

References

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[6] M Puech, PCT Patent : WO 2004008477.