Deep Analog-to-Digital Converter for Wireless Communication

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With the advent of the 5G wireless networks, achieving tens of gigabits per second throughputs and low, milliseconds, latency has become a reality. This level of performance will fuel numerous real-time applications, such as autonomy and augmented reality, where the computationally heavy tasks can be performed in the cloud. The increase in the bandwidth along with the use of dense constellations places a significant burden on the speed and accuracy of analog-to-digital converters (ADC). A popular approach to create wideband ADCs is utilizing multiple channels each operating at a lower speed in the time-interleaved fashion. However, an interleaved ADC comes with its own set of challenges. The parallel architecture is very sensitive to the inter-channel mismatch, timing jitter, clock skew between different ADC channels as well as the nonlinearity within individual channels. Consequently, complex post-calibration is required using digital signal processing (DSP) after the ADC. The traditional DSP calibration consumes a significant amount of power and its design requires knowledge of the source and type of errors which are becoming increasingly difficult to predict in nanometer CMOS processes. In this paper, instead of individually targeting each source of error, we utilize a deep learning algorithm to learn the complete and complex ADC behavior and to compensate for it in real-time. We demonstrate this “Deep ADC” technique on an 8G Sample/s 8-channel time-interleaved ADC with the QAM-OFDM modulated data. Simulation results for different QAM symbol constellations and OFDM subcarriers show dramatic improvements of approximately 5 bits in the dynamic range with a concomitant drastic reduction in symbol error rate. We further discuss the hardware implementation including latency, power consumption, memory requirements, and chip area.

Keywords: Interleaved ADC, Deep ADC, LSTM, Convolutional Neural Network, 5G, OFDM, AI

1. INTRODUCTION

In information theory, the Shannon–Hartley theorem establishes the maximum rate at which information can be transmitted over a communications channel of a specified bandwidth in the presence of noise [1]. The 5G communication systems can achieve tens of gigabits per second throughputs and provide very low latency in tens of milliseconds range. The tremendous increase in the bandwidth challenges traditional signal processing techniques and calls for fresh ideas [2, 3]. Among the critical components in the receiver chain, Analog-to-Digital Converters (ADC) is a key bottleneck because its bandwidth cannot be scaled as easily compared to other electrical components. Sampling rate and effective-number-of-bits (ENOB) are the most important parameters of an ADC [4]. The lower bound on the sampling rate is set by the Nyquist criterion. The ENOB determines the dynamic range of the ADC and must be high enough to handle the dense constellations used in modern communication systems. A popular approach to creating high-
resolution wideband ADCs is utilizing multiple channels each operating at a lower speed in the time-interleaved pattern [5, 6, 7, 8]. However, an interleaved ADC comes with its own set of challenges. The parallel architecture is very sensitive to the inter-channel mismatch, timing jitter, clock skew between different ADC channels as well as the nonlinearity within individual channels. Consequently, complex post-calibration is required using digital signal processing (DSP) after the ADC. Traditional methods become challenging for future wideband signals spanning several Gigahertz. One reason is the existence of the parasitic components (resistive, capacitive, and inductive) and their mismatches between interleaved-ADC channels. In narrowband applications, the frequency response of the parasitics is almost constant and a simple scaling can neutralize their effect. However, in wideband systems, the frequency responses can dramatically change with frequency. As a result, new methodologies are required to overcome this issue. Besides, as the feature size of the CMOS technologies is decreasing, traditional CMOS transistor models are not valid anymore and analog circuit designers are having a difficult time designing a robust and accurate circuit. Since traditional DSP methods require knowing the behavior of the ADC circuit, they are less effective in newer CMOS technologies. In contrast to these traditional calibration techniques, neural network (NN) can be used to address the calibration issues of an ADC without requiring knowledge of the circuit behavior. NN has made significant advances in image and voice recognition and synthesis. Recently, several studies [9, 10, 11, 12] have been done about their application in circuit designing and the results have been very promising.

A common NN is made up of several layers connected through multi-dimensional matrix weights. The NN must first be trained with known input/output pairs (ground truth) to find the optimum weights. Different training algorithms such as stochastic gradient descent (SGD) are used to do this [13]. Among network architectures, convolutional networks perform exceptionally well for image processing whereas LSTM networks are best suited for temporal data such as speech processing in which the memory effects are important [14].

Traditional DSP calibration algorithms for ADC errors require a knowledge of the behavior of the error. Owing to a large number of adjustable parameters, neural networks are highly adaptive and can perform ADC calibration without the knowledge of error behavior [15, 16, 17]. In fact, NN has been used for system identification for a long time [18]. Because of these important advantages of the NN over traditional DSP approaches, several studies have been done to prove their ability in removing the non-linear effects in ADCs [19, 20]. However, they utilize primitive neural network architectures and required extensive preprocessing using conventional techniques. They also attempt to calibrate errors for purely analog signals which violate information-theoretic considerations. Consequently, previous attempts have not been successful.

In this paper, we introduce the “Deep ADC” concept where realtime inference by a trained neural network corrects for ADC errors over more than an octave of bandwidth and for a wide range of signal constellations and OFDM subcarrier counts. We show that a single convolutional LSTM neural network that can simultaneously learn and correct the ADC errors including non-linearity induced errors, channel-mismatch, time-skew, phase distortions, and memory effects. We show proof of concept results for an 8G Sample/s 8-channel time-interleaved ADC with the QAM–OFDM modulated data. Dramatic enhancement of approximately 5 bits in the dynamic range is observed with drastic improvement in symbol error rate.
2. NEURAL NETWORK ADC CALIBRATION ALGORITHM

The bandwidth (BW) and spectral purity are two of the important topics in cognitive and spectrum sensing. Time interleaving is a widely used method in which multiple similar ADCs quantize the input data series at an aggregate rate that is faster than the operating sample rate of each data converter [5, 6, 7, 8]. Figure 1(a) shows an M-channel interleaved ADC. The sampling clock used in each channel is $1/M$ times the final sampling rate and all the channel clocks experience a phase offset of $F_s/M$ from each other. In a time-interleaved ADC, the common sources of error are clock jitter, time-skew, and mismatches between channels (memory effects and non-linearity). These sources of error limit the final dynamic range as measured by SNDR and achievable effective number of bits (ENOB). While traditional DSP algorithms can address these issues in a narrow band system (Hundreds of MHz), they won’t be able to calibrate a wideband time-interleaved ADC working at several Gigahertz of Nyquist frequency and providing decent resolution such as 12 bits as used in wireless communication. This is due to mismatches in the frequency responses of channels which is negligible in a narrowband but significant in a wideband scenario.

![Diagram of an M-channel interleaved ADC](image)

Figure 1. An M-channel interleaved ADC is composed of M individual ADCs working with the rate of $F_s/M$. The sampling clock of each channel has a phase offset of $F_s/M$ from the previous channel [5].

To overcome this issue, we propose an advanced NN system that calibrates ADCs over a wide bandwidth. Specifically, we design the demonstrate the system for OFDM/QAM modulated communication signals as this modulation format is the workhorse of wireless communication (LTE, 5G, 6G). The 8-channel Interleaved ADC is modeled in the MATLAB (Figure 2 (a)) and different kinds of error sources are added to make the system behave like a real ADC. Figure 2(b) depicts the block diagram of each ADC channel.
Figure 2. a) Block diagram of an 8-channel interleaved ADC simulated in MATLAB. b) Block diagram of each ADC channel including non-linear effects such as jitter, time-skew, 3rd order nonlinearity, and memory effect.

Each ADC channel includes its own sources of non-linearity such as 3rd order nonlinearity (2nd order is removed by using differential processing), jitter, time-skew, and memory effect (parasitics). The resolution of the ADCs is 13-bit and a full-scale voltage of 1Vp-p. Memory effects include parasitic components that can degrade the performance of the ADC. Figure 3 demonstrates how the NN calibration is trained and implemented in the system design. The network uses current and future samples of the time domain signal. To ensure causality, we buffer the required future time samples and pass the vector to the NN when the buffer is full. Figure 4 shows the architecture of the NN used in this project. It is comprised of a combination of convolutional and LSTM layers. First, several convolutional layers extract the local features temporal features (i.e. with short memory). Then these feature maps are passed through LSTMs
layers that capture longer range the memory effects while ensuring causality. Table 1 shows the details of our designed NN architecture.

Table 1. Details of the neural network architecture for ADC error compensation

| Conv1 | Conv1d (in channel: 1, out channel:64, kernel 3x3, stride:1) + BatchNorm1d + ReLU |
|-------|----------------------------------------------------------------------------------|
| Conv2 | Conv1d (in channel:64, out channel:64, kernel 3x3, stride:1) + BatchNorm1d + ReLU |
|       | Conv1d (in channel:128, kernel 3x3, stride:1) + BatchNorm1d + ReLU               |
| LSTM1 | LSTM (in features: 128, hidden state features: 64, layer: 1)                    |
| LSTM2 | LSTM (in features: 64, hidden state features: 32, layer: 1)                    |
| LSTM3 | LSTM (in features: 32, hidden state features: 4, layer: 1)                     |
| Linear| Linear (in features: 256, out features: 1)                                     |
3. SIMULATION RESULT

In this section, we demonstrate the performance of the Deep ADC and compare its performance under different QAM constellations (64, 128, 256, 512, and 1024). It’s important to note that a single network learns the ADC response to all these constellations simultaneously and no retraining is required for inference of different constellations. Only the 256QAM simulation results are presented here. The 64QAM and 1024QAM results are provided in the Appendix section, the rest are similar. The 8-channel interleaved ADC has 13-bit of nominal resolution (12-bit + 1 bit for differential input) and each ADC operates at a sampling rate of 1.024 GSample/s. This provides a total sampling rate of 8.192 GSample/s. The signals under test have a bandwidth of 1 GHz with center frequency at 1.3 GHz. This signal is generated by passing the QAM symbols through an OFDM modulator with 128 subcarriers and a frequency resolution of 8 MHz. Figure 5 shows the PAPR distribution for each QAM constellation. The time skew for each channel is generated randomly with a uniform distribution. The absolute difference between the maximum and minimum time-skew is 12 ps. The jitter has an RMS of 390 fs and bandwidth of 20 MHz. As it is customary, odd-order nonlinearity is modeled by using the tanh transfer function. Memory effects are simulated by passing each channel through a different Chebyshev analog filter (passband ripple: 1.5 - 6 dB, corner frequency: 5 - 8 GHz, order=8) (Figure 6). The corner frequency of the filters is adjusted such that all the signal spectra pass without attenuation but do suffer from amplitude and phase ripples in the passband. The reason for the difference in the frequency responses is to represent the mismatches between channels. This mismatched ripple behavior poses a significant challenge for traditional error calibration algorithms. Figure 7 compares the performance of the NN calibrated ADC with the shifting method for a quantized OFDM symbol in the time domain.

Figure 5. The PAPR distribution for each QAM constellation.
Since the memory effect filters have an almost-linear phase response in the signal spectrum, it would make sense that a shift in time could fix the time domain signal greatly. However, the shifted signal still faces some degradation compared to the ideal signal. Figure 7(c) shows the AI calibrated ADC response. It is interesting to notice that the NN can detect this shift and apply this shift through its network. In Figure 8(a), the time domain error with respect to LSB is shown. Figure 8(b) compares the resulted ENOB by the three approaches. As it is visible from the plots, the NN calibrated method provides a huge improvement compared to other methods. The NN calibrated ADC approximately can improve the ENOB by 8 bits.

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**Figure 6.** Magnitude and phase response of the filters used to implement memory effects for each of the 8 ADC channels. (passband ripple: 1.5 - 6 dB, corner frequency: 5 - 8GHz, order=8).

**Figure 7.** (a) OFDM symbol with ideal (blue) and non-ideal (red) ADC. The data is 256QAM. A large part of the error is a deterministic time shift that can be measured using cross-correlation and easily corrected. This is shown in (b). Figure (c) shows the output of the neural network. Operating as an error compensating postprocessor, the network can learn and correct all the errors including the time shift.
Figure 8. (a) This plot compares the time domain error with normalized to the least significant bit (LSB). The data is 256QAM. (b) Operating as an error compensating postprocessor, the network provides a dramatic improvement in the number of bits.

Figure 9. The impact of neural network compensation on the magnitude and phase spectra. Data is 256QAM. From left to right: Frequency spectrum of the one OFDM symbol at the output of an ideal, the non-ideal ADC, and the nonideal ADC after compensation by the neural network. The resolution bandwidth (RBW) is 1MHz.

The simulation results for 64 and 1024 QAM constellations are provided in appendix A and the results for 128QAM and 512QAM are very similar.
4. TOWARD HARDWARE IMPLEMENTATION

Although here the training of the NN is done with floating-point calculation, the implementation in either ASIC or FPGA takes place in fixed-point formats. This poses the main challenge for the physical realization of the Deep ADC proposed here. There have been several studies about the quantization of neural networks in both the training and testing phase to realize efficient and accurate fixed-point inference networks [21] [22]. As an example, previous works [23] [24] have demonstrated the FPGA implementation of popular neural network architectures such as convolutional neural networks (CNN) and recurrent neural networks (RNN). Motivated by these successful fixed-point implementations, we believed that the proposed solution can also be implemented in fixed-point formats in hardware. We note that most of the prior works have been classification tasks that are more robust against quantization errors, whereas the ADC calibration is essentially a regression problem that is more sensitive to quantization errors. We anticipate that these quantization errors will place an upper limit on the maximum number of bits that can be achieved.

5. CONCLUSIONS

In this project, we presented the concept of Deep ADC where a judiciously designed neural network acts as an error compensating post-processor to enhance the resolution of the ADC. According to the simulation results, this method can calibrate the ADC in a very wide frequency spectrum and improve the resolution for a wide range of OFDM/QAM signals. We show that a single network learns the ADC response to all constellations, simultaneously, and no retraining is required for inference of different constellations. This technology can benefit cognitive and spectrum sensing applications that require wide bandwidth ADCs.

6. FUTURE WORK

The main future task is to compress our network by lowering its fixed-point resolution and removing unnecessary weights (pruning). By doing so, the area, memory requirement, and power consumption of the chip are reduced to make it suitable for embedded devices including edge AI.

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Appendix

Below are the test results for the 64 QAM. Please check the simulation section for further information about the test results.

(a) OFDM symbol with ideal (blue) and non-ideal (red) ADC. The data is 64QAM. A large part of the error is a deterministic time shift that can be measured using cross correlation and easily corrected. This is shown in (b). Figure (c) shows the output of the neural network. Operating as an error compensating postprocessor, the network is able to learn and correct all the errors including the time shift.
(a) This plot compares the time domain error with normalized to the least significant bit (LSB). The data is 64QAM.
(b) Operating as an error compensating postprocessor, the network provides a dramatic improvement in the number of bits.

![Graphs showing impact of neural network compensation on magnitude and phase spectra. Data is 64QAM. From left to right: Frequency spectrum of the one OFDM symbol at the output of an ideal, the non-ideal ADC, and the nonideal ADC after compensation by the neural network. The resolution bandwidth (RBW) is 1MHz.]

Below are the test results for the 1024 QAM. Please check the simulation section for further information about the test results.
(a) OFDM symbol with ideal (blue) and non-ideal (red) ADC. The data is 1024QAM. A large part of the error is a deterministic time shift that can be measured using cross correlation and easily corrected. This is shown in (b). Figure (c) shows the output of the neural network. Operating as an error compensating postprocessor, the network is able to learn and correct all the errors including the time shift.

(a) This plot compares the time domain error with normalized to the least significant bit (LSB). The data is 1024QAM. (b) Operating as an error compensating postprocessor, the network provides a dramatic improvement in the number of bits.
The impact of neural network compensation on the magnitude and phase spectra. Data is 1024QAM. From left to right: Frequency spectrum of the one OFDM symbol at the output of an ideal, the non-ideal ADC, and the nonideal ADC after compensation by the neural network. The resolution bandwidth (RBW) is 1MHz.