Design of class E power amplifiers by using scalable electro-thermal GaN HEMT model

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Abstract: In this paper, a scalable large signal GaN HEMT model including nonlinear thermal sub-circuit is described. Only two scalable parameters are needed in the $I_d$ scalable model by introducing a simple correction factor. The established model can predict the I–V curves at different-in-size AlGaN/GaN HEMTs devices accurately. Small signal S-parameters and large signal load pull tests with on-wafer measurement is used to further validate the proposed model. Finally, the proposed scalable model is used to design a broadband high efficiency continuous class-E power amplifier (PA). Experimental results show that this class E PA is realized from 2.5–3.5 GHz with drain efficiency of 60%–70%, over 8.2 dB gain and over 35.2 dBm output by using a GaN HEMT with 1.25 mm total gate width. The results show that the proposed model is useful for high efficiency amplifier design.

Keywords: GaN HEMT, large signal model, scalable model, class E power amplifier

Classification: Microwave and millimeter-wave devices, circuits, and modules

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1 Introduction

Nowadays, AlGaN/GaN HEMTs have been widely used in microwave and millimeter wave solid state high power amplifiers in radar applications [1, 2, 3, 4, 5]. Moreover, GaN HEMT is also highly attracted in high efficiency power amplifier design (i.e. class E, class F, wave form engineering, etc.) in communication systems, taking the advantage of high breakdown voltages and low Ron [6, 7, 8]. Accurate large signal model of GaN HEMTs is important for power amplifier with certain device geometry, especially for high efficiency design. However, in practical GaN power amplifier, the number of fingers and periphery of GaN HEMTs need to be optimized at given certain specification or best design of GaN amplifier. As a result, an accurate and scalable large signal model of GaN HEMT is necessary to design high performance GaN circuits [9, 10, 11, 12, 13].

Scalable large signal models of multiple fingers or multiple cells FET devices have been widely investigated, especially for parasitic effects and electro-thermal effects. Typically, linear scaling rules are widely adopted for the device. As the frequency up to millimeter-wave, the accurate parasitic effects of the device can be obtained by using the full-wave electromagnetic (FW-EM) analysis of the actual device layout in [14]. Though this FW-EM method is much more accurate, it is too complex ion, and the thickness of epitaxial layer and the doping density of the device are sensitive to EM simulations, and the exact process parameters of the device needed for EM simulations tend to be confidential. As an alternative in [15], the novel distributed parasitic networks are adopted for dealing with device scaling on the basis of EM device layout simulations. Moreover, the conventional linear-scalable intrinsic model for different-in-size FET devices is inappropriate for the AlGaN/GaN HEMTs. As the self-heating effect is significant for the device and the thermal resistances of the device demonstrate to be geometry dependent [16]. Recently, Darwish et al. presented an accurate closed-form expression for thermal resistance, which can be used for scalability of thermal resistance [17]. However, this method is too complex to be implemented in SPICE like simulator. Moreover, few effects were considered in accurate modeling the scalability of electro-thermal model, including both thermal resistance and thermal capacitance.

In this paper, we report a nonlinear GaN HEMT scalable model. To simplify the parasitic parameters, empirical parasitic network with linear scalability are used. And a nonlinear scalable electro-thermal model is proposed and implemented in empirical large signal model. The equivalent circuit described within has been extracted for the 0.25 μm GaN transistor. In section 2, we proposed our scalable large-signal nonlinear model based on Angelov model. In section 3, we test and verify the scalable model from I-V curve, small signal S-parameters, and large signal load-pull results. In section 4, we designed and fabricated a class E power amplifier using the 0.25 μm GaN HEMT to certificate the value of the proposed scalable model.
2 Large signal model development

The topology of proposed scalable large signal model is shown in Fig. 1. The extrinsic linear elements of the model consist of the parasitic resistances, inductances and capacitances. The intrinsic elements include the bias dependent $C_{gs}$, $C_{ds}$, $C_{gd}$, the drain-source current $I_{ds}$, and gate diodes $D_{gs}$ and $D_{gd}$. The dispersive effects are accounted by the thermal and trapped sub-circuits. $R_{th}$ and $C_{th}$ represent the thermal resistance and thermal capacitors.

![Fig. 1. The topology of scalable large-signal model.](image)

In order to accurately describe the $I_{ds}$ characteristic, an improved $I_{ds}$ model based on the Angelov model [18], for AlGaN/GaN HEMTs is proposed by the expressions [1].

$$I_{ds} = I_{pk0} \times (1 + M_{pkth} \times \tanh(\psi)) \times \tanh(aV_{ds})$$  \hspace{1cm} (1)

where

$$I_{pkth} = I_{pk0} \times (1 + k_{pk0} \times \Delta T_{ch}')$$  \hspace{1cm} (2)

$$\psi = p_{k1th} \times (V_{gs} - V_{pk0}) + p_{k2th} \times (V_{gs} - V_{pk2})^2$$
$$+ p_{k3th} \times (V_{gs} - V_{pk3})^3$$  \hspace{1cm} (3)

$$P_{knth} = (k_{n0} + k_{n1} \times V_{ds}) \times \tanh(a_n \times V_{ds})$$
$$\times (1 + k_{pn} \times \Delta T_{ch}') \quad n = 1, 2, \text{ and } 3$$  \hspace{1cm} (4)

$$M_{pkth} = (1 + 0.5 \times (M_{pkth} - 1)) \times (1 + \tanh(qm \times (V_{gs} - V_{gsm}))))$$
$$\times (1 + k_M \times \Delta T_{ch}')$$  \hspace{1cm} (5)

$$\Delta T_{ch}' = P_{diss} \times R_{th} \times (1 - \exp(-t/\tau))$$  \hspace{1cm} (6)

$\Delta T_{ch}'$ is the channel temperature variation dependence on $P_{diss}$.

As for the scalable capability of the $I_{ds}$ model, the important parameter $I_{pk0}$ is then modeled with the device geometry as the expression (7), and a simple
correction factor $kf$ is employed for scaling capability, since the drain source currents are not invariably linearly dependent on the geometry.

\[ I_{pk0_{sc}} = I_{pk0} \times (1 + kf) \times sfw \times sfn \]  
\[ sfw = \frac{Wg}{Wg_{rf}} \]  
\[ sfn = \frac{Ng}{Ng_{rf}} \]

where $Wg_{rf}$ and $Ng_{rf}$ are the unit gate width and number of fingers of the reference device, respectively. $sfw$ and $sfn$ denote the scaling factors of the unit gate width and number of fingers, respectively.

2.1 Thermal sub-circuit model

The analysis of the electro-thermal effects have been investigated [19]. The approach of electro-thermal finite element method (FEM) simulations is widely used in identifications of the $R_{th}$ and $C_{th}$ for its convenience, as compared with the experimental method, such as pulse I-V measurements under different temperatures. In addition, the simulations are very time-saving and suitable for different-in-size devices to determine the thermal parameters. The scalable $R_{th}$ and $C_{th}$ model in [1] is employed in this paper. The channel temperature variations can be easily captured, and then the thermal resistances are also easily derived.

2.2 Trapping effects dispersive model

The traps induced dispersion is generally characterized by two approaches in modeling: analytical and empirically equivalent circuit methods [18]. The latter one with trap dispersion network (Idsf, Rf and Cf), which is effectively and widely used, is employed in our paper. The relevant parameters extraction procedure is the same as [20]; the trap dispersion network is determined by comparing the gm and gds obtained from S-parameters. And the scaling rule for the trapping effects is the same as that for Ids model.

3 Validation of the scalable model

The proposed scalable model is validated by means of several 0.25-µm AlGaN/GaN HEMTs with different-in-size devices. A $4 \times 100$ µm HEMT is used as the reference device. The other devices are considered for scaling.

For high efficiency amplifier design (i.e. class E, class F, etc.), the model accuracy near pin-off voltage and linear region is very important. As a result, we investigate the accuracy of gm near pin-off gate voltage. The predicted and measured transconductance gm are shown in Fig. 2(a). And the results of output conductance gd at different $V_{gs}$ are shown in Fig. 2(b). A good agreement between the modeled and measured results has been achieved. It can be attributed to the accurate scalable $I_{ds}$ model for the different sizes devices.

The developed large signal model is embedded by using the Symbolically Defined Devices (SDD) in spice-like software Agilent Advance Design Systems (ADS v. 2011). The devices are measured by using the on-wafer load-pull system (Focus/MPT-3620-TC) for validation purpose. Fig. 3 shows the comparison between measurements and simulations of the output power (Pout), Gain and PAE.
under the conditions terminated for max output power for \( V_{gs} = -2.5 \, \text{V}, \, V_{ds} = 28 \, \text{V} \).

The source and load impedances of the \( 4 \times 100 \, \mu\text{m} \) device at 10 GHz are 5.95 \( + j \times 13.22 \, \text{Ohm} \) and 38.67 \( + j \times 55.99 \, \text{Ohm} \), respectively, while they are 10.51 \( + j \times 21.18 \, \text{Ohm} \) and 43.12 \( + j \times 105.23 \, \text{Ohm} \), respectively, for the \( 4 \times 50 \, \mu\text{m} \) device. The close agreements between the simulations and measurements demonstrate that the proposed scalable model can accurately predict the large signal behavior for different device geometries.

### 4 Design of class E PA by using the proposed model

Class E power amplifier is a kind of switching mode amplifier, introduced in 1975 by Sokal [21]. As compared to the class A and AB or B PA, where the active device is basically represented by a controlled current source replicating the input driving stimulus, in switch mode PAs the active device is assumed to be ideally driven in the ON and OFF states, just like a switch. The class E power amplifier can offer high efficiency in theory since simultaneous nonzero switching voltage and current are prevent from occurring. Due to its simplicity and high efficiency, the class E PA has become very popular in RF and microwave amplifier.
In this part, to verify the accuracy of the model, a class E PA were designed and fabricated based on the modeled 10 × 125 μm GaN HEMT device described above. The design of the amplifier consist of gate and drain bias networks, input and output networks. Decoupling capacitor and high impedance λ/4 transmission line were exploited in the bias network. And we use a type Pi broadband matching network based on input/output low-pass matching network, in order to enhance the bandwidth of Domestic technology GaN HEMT class E PAs. The schematic of class E PA, which shown in Fig. 4, is realized on the Taconic RF-60 substrate (εr = 6.15, h = 0.635 mm).

The simulated drain current and voltage waveforms are shown in Fig. 5, obviously we can see the drain current and voltage exhibits an approximate switching characteristic and the almost no-overlap waveform, from which reflect the class E features. Single tone large signal simulated and measurement values of Pout, PAE, and Gain are shown in Fig. 6, with the transistor biased with f0 = 3.0 GHz, Vgs = −3.0 GHz, Vds = 28 V.

The good agreement between simulated and measured values indicated the good accuracy model technology when we use it to design a high efficiency power amplifier. There are many other reasons that can cause the difference between simulated and measured values, such as the process error of the GaN HEMT die, considering this point and its value, we can use the large-signal statistical model for further exactitude design [22]. The measured output power, DE, PAE, and gain in the whole frequency are shown in Fig. 7. The results show that this class E PA is realized from 2.5–3.5 GHz with drain efficiency of 60%–70%, over 8.2 dB gain and over 35.8 dBm output. This further proves that the proposed model is good for design class E amplifier.
Fig. 5. The simulated drain current and voltage waveforms.

Fig. 6. Single tone large signal simulated and measurement values of Pout, PAE, and Gain.

Fig. 7. The simulate and measured output power, DE, PAE, and gain at $V_{gs} = -2.5 \, \text{V}$, $V_{ds} = 25 \, \text{V}$, $Pin = 27 \, \text{dBm}$. 
5 Conclusion

A scalable nonlinear model for GaN HEMTs with different device periphery has been presented in this paper. The I-V curve, small and large signal behaviors are validated in 0.25 µm GaN HEMTs with different periphery. And a class E power amplifier has been designed and fabricated in order to verify the accuracy of the proposed scalable large signal model. Experimental results show that the validity of the model has been demonstrated with a high accuracy in class E design technology.

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