Design of Low Power Multiplier with Less Area Using Quaternary Carry Increment Adder for New-Fangled Processors

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Abstract
Multiplication is one of the most basic processes, in digital signal processing applications. To process the instructions, most processors require multiplication. Because multipliers are employed in almost all arithmetic operations, they consume the majority of time and power. As a nutshell, the multiplier’s efficiency is critical in terms of enhancing processor performance. The array multiplier is one of the most efficient multipliers since it is both quick and simple. However, power consumption is high. The basic components of an array multiplier are adders. The multiplier’s efficiency will improve if the adders are much more efficient. The prior study used Complementary Metal Oxide Semiconductor (CMOS) to construct a Quaternary Carry-Lookahead Adder (CLA) that substitutes the adder circuit in the array multiplier. Quaternary number system circuits are quicker than binary number system circuits and can execute arithmetic operations without carry. However, Quaternary circuits take up more space. As a solution, the Quaternary Carry Increment Adder (CIA) is proposed. The proposed adder consumes less power and occupies less area than the existing Quaternary CLA. In the array multiplier, the Quaternary CIA substitutes the Quaternary CLA. This helps to lower the multiplier’s power and area consumption. Tanner EDA tool is used to designing the circuits and were simulated with 180 nm technology. Various parameters such as delay, power and power-delay product of the existing and the proposed are measured and compared.

Keywords Quaternary signed-digits · Carry increment adder · Multiplier and low power

1 Introduction
The circuits in VLSI are everywhere, for example in our cars, computers, digital camera, cell phones, etc. The first integrated circuits contain only a very less number of transistors. This provides very few logic gates. Based on the number of transistors the IC era has been
differentiated into SSI, MSI, LSI and then VLSI [1]. Very large scale integration is extensively handed down to integrated circuits, component designing and microchip processors [2].

The processors’ performance is solely relying on the multipliers’ performance. Array multiplier is one of the fastest multipliers that can be designed easily [3]. Adders makes the building blocks of the multipliers. In VLSI, the efficiency of these circuits depends on the parameters delay, area, power and Power-Delay Product (PDP). Circuits designed using Complementary Metal Oxide Semiconductor (CMOS) transistor has low power consumption, high noise immunity and it is widely used in VLSI chips [4]. CMOS follows binary logic. Some of the disadvantages of the binary can be lack of states for representation, only two states (0 and 1) are available, number of bits required for the representation of the digits are high and the propagation of carry across the bits during arithmetic operation [5–7].

Multipliers play a vital role in various digital signal processing and many other applications [8]. Multiplication related operations to the digital signal processing, such as filters, convolutions, Fast Fourier Transform (FFT) are implemented whereas in microprocessor, it is arithmetic and logic units [9–11]. As multiplication subordinates the execution time for many DSP algorithms so there is a requirement of high-speed multiplier [12, 13].

Many researchers, with evolution in technology have already tried and are still endeavouring to craft multiplier units which furnishes either greater operating performance, less power consumption, regularity of layout and consequently with small area or even combination of them in one multiplier which makes them appropriate for several increased speed, decreased power and compact VLSI implementation [14].

In digital combinational circuits, an array multiplier is used for multiplying two binary numbers by utilizing an array of full adder and half adder. This type is used for almost simultaneous addition of the several product terms concerned. Array architecture is a prominent technology to execute these multipliers due to its regular compact structure [15]. High power dissipation in these designs is mainly due to its shifting of a large numbers of forged transistors on internal nodes [16–18].

Adders are building blocks of the multipliers. There are many adders like Ripple-Carry Adder (RCA), Carry-Look ahead Adder (CLA), Carry Increment Adder (CIA), Carry Select, Carry Skip and Carry Save Adder (CSA). Various adder performances are analysed by several research works. Carry Increment adder is more efficient than Carry-Lookahead Adder. The Quaternary CLA in the array multiplier is replaced by the Quaternary CIA. The number of interconnections in circuits are reduced when Quaternary number system is used [19–22].

The objective of the proposed idea is to design a multiplier with quaternary carry increment adder by reducing the factors like power and area. In the other part of the paper, Sects. 2 and 3 dedicated to existing and proposed method, preceded by in Sect. 4 dedicated to result as well as discussion, and the end Sect. 5 is about the conclusion of the work carried in this paper.

2 Existing Methods

Higher radix number system like Quaternary Number System can be used to perform carry free addition [23]. They can also be used to perform subtraction without borrow, multiplication and division. Numbers that can be represented in QSD are −3, −2, −1, 0, 1, 2 and 3. The number 0, 1, 2, 3 are used to represent real numbers [24]. The carry
propagation and formation are increased when the number of bits are increased which leads to increase in delay, power and area. This problem in the binary circuits can be overcome by using the number system having higher radix than binary number system. When compared with binary more states can be represented by quaternary because of its higher radix. With help of the higher radix, the number of interconnections in the circuits can be reduced. By minimizing the interconnections, the intricacy of the circuit is reduced. This leads to increase in speed of the circuits [25].

The most important task is to upturn the input signal applied. Whether the bidden input is low or high, the result will be high. One NMOS transistor or one PMOS transistor paired with a resistor can be used to create inverters. In different logic circuits, Quaternary inverter plays a major role. Input signal is enhanced utilizing inverter function. Totally six CMOS transistors are required for the designing the quaternary inverter [26].

The combination of inverter with AND gate forms NAND gate, or the AND gate is form by applying inverter at the output of NAND gate. The AND function causes the AND circuit’s output to be the truncated value of numerous inputs. The NAND circuit with two quaternary inputs is implemented. The circuit is built using an inverter circuit and a standard binary NAND circuit [27]. For any other input voltage level cases, by setting the input to zero voltage makes the output to 3 V. The NMOS transistors inclined in series construct the tracks to 1 V, 2 V, and ground to be opened only when both inputs are equal to or higher than the $V_t$ of both transistors. PMOS transistors are at the helm of to close the path when both inputs are higher than their $V_t$ values [28].

In case of OR gate the output sets to the highest of the input value. Opposite is the function of NOR gate i.e. NOR is the inversion of OR gate. So, the combination of inverter with OR gate forms NOR gate, or the OR gate is form by applying inverter at the output of NOR gate.

The normal Carry-Look ahead logic is used to design the Quaternary gates. The only difference is the instead of binary logic gates. Quaternary logic gates are used. The same propagate and generate logic of binary Carry-Look ahead. Carry-Look ahead generated in order to generate carry every other bit with the help of the input carry $C_{in}$. The output of the generate is given to carry-look ahead generated for carry generation [29]. Then XOR gates are used the propagate and carry to generate the output as in Fig. 4. This quaternary adder can be used to perform fast addition than binary CLA due to lesser number of interconnections. The power consumption of the adder is also reduced. The formula are as follows

\begin{align}
    P_i &= A_i \oplus B_i \\
    G_i &= A_i \cdot B_i \\
    C_i &= P_i \oplus G_i \\
    S_i &= P_i \oplus C_i
\end{align}

The array multiplier is used here. The basic component of the multiplier is adder. An N bit array multiplier requires N-1 adder. Array Multiplier is a structured layout of a combinational multiplier. Since QSD multiplier can be handed down as a vital block for all arithmetic processes, it can be implemented for building of a high performance multiprocessor [30]. So, it can be constructed easily. It relies on the preceding partial sum generated for the computation of the output device. A multiplication operation is
usually divided into two procedures: parallel and iterative. QSD multiplication may be done in two methods, with the key components of being a QSD partial product generator and a QSD adder [31].

3 Proposed Work

In the proposed system, the quaternary CLA replaced with the 8-bit quaternary Carry Increment Adder in order to minimize the power consumption and area of the existing system. Two quaternary inputs X and Y are given as inputs and the output is obtained as Sum and Carry as shown in Fig. 1. The half adder consists of QSD XOR and QSD AND gates for generating sum and carry respectively.

The quaternary full adder is constructed utilizing quaternary half adders. The additional input Carry (C\text{in}) is used for the completion of the full adder. The carry digit and two quaternary digits are sum up by this circuit. This circuit generates quaternary sum and quaternary carry as shown in the Fig. 2. In order to implement carry free addition, the carry in for the adder circuit restricted to values upto 1, that is, the carry can be either 0 or 1 as in binary number system. Execution of circuit is clarified by this assumption. Two QSD Half adder circuits and one QSD OR gate are required for the design of the full adder circuit as shown in Fig. 2. It is same as that of designing the conventional full adder circuit. Three inputs X, Y and Carry in (C\text{in}) are given as the input and the sum and carry are obtained as the outputs.

The Ripple-Carry Adder (RCA) and an incrementor block form the traditional Carry Increment Adder (CIA), which is shown in the Fig. 3. Half adder circuits are used as incrementor circuit in the Carry Increment Adder sequentially. The total bits are divides into several 4 bits and then 4-bit Ripple-Carry Adders perform the addition operation.

Fig. 1 Tanner design of QSD half adder
Fig. 2  Schematic diagram of QSD full adder

Fig. 3  Block diagram of Quaternary CIA
The adders perform only one partial addition and the sum is increased if it is required, this eliminates the need for calculating two partial sums and choosing the exact one.

The 8-bit Quaternary CIA is made up of an incremental circuit block and two 4-bit Quaternary RCA as shown in Fig. 4. Four bits of LSB are added with the help 4 bit Quaternary RCA which produces sum and carry. The carry produced in the first block is used as $C_{in}$ for the incrementor block. Similarly, the second four bits are added with the help of 4 bit Quaternary RCA. The partial sum that is produced by the second block is used as input for the incrementor circuit. The two 4 bit Quaternary RCAs adds the number in parallel manner since the $C_{in}$ of the circuits are given as 0. The incremental block produces same output when the carry from the first Quaternary RCA block is 0 and increments the output by 1 when the carry from the first Quaternary RCA block is 1.

The same array multiplier, which is used in the existing method, is used. Only the adder part is changed. The Carry-Look ahead Adder is replaced with the Carry Increment Adder for the better performance of the multiplier. The $8 \times 8$ array multiplier have the ability of multiplying two 8-bit quaternary numbers. Since ripple-carry adder is used in place of carry-look ahead adder, the power intake of the circuit is reduced [32]. The number of transistors used in the circuit is also reduced. The efficiency if the design is increased. The Power-Delay Product of the design is also improved (Fig. 5).

Fig. 4 Schematic of 8 bit Quaternary CIA
4 Results and Discussion

The circuits that are designed with the help of Tanner EDA tool in S-Edit using 250nm technology are simulated. The output of the designed circuits is obtained in the W-Edit. The inputs that are given to both the designs are shown in the Figs. 6, 7, 8 And 9.

The design consists of 16 inputs, that is, 8-bit multiplicand and 8-bit multiplier in order to produce 16-bit output. Two different sets of the inputs are given to the circuits.

The first set of the input as follows:

8 bit Multiplicand, A [7:0] = 00000000
8 bit Multiplier, B [7:0] = 00000000

The second set of the inputs are as follows:

8 bit Multiplicand, A [7:0] = 11111111
8 bit Multiplier, B [7:0] = 11111111
Fig. 6  8-bit input A0–A3

Fig. 7  8-bit input A4–A7
Fig. 8 8-bit input B0–B3

Fig. 9 8-bit input B4–B7
The inputs shown in the Figs. 6, 7, 8 And 9 are given to quaternary CLA multiplier and the results are obtained as waveforms in W-Edit.

The outputs for the quaternary CLA multiplier are obtained and they are shown in the Figs. 10, 11 and 12.

The output for the first set of the input as follows

8 bit Multiplicand, $A[7:0] = 00000000$
8 bit Multiplicand, $A[7:0] = 00000000$
8 bit Multiplier, $B[7:0] = 00000000$
16 bit Product, $M[15:0] = 0000000000000000$

The output for the second set of the inputs are as follows

8 bit Multiplicand, $A[7:0] = 11111111$
8 bit Multiplier, $B[7:0] = 11111111$
16 bit Product, $M[15:0] = 1111111000000001$
Fig. 11  Output of CLA multiplier M5–M9

Fig. 12  Output of CLA multiplier M10–M15
**Fig. 13** Output of CIA multiplier M0–M4

**Fig. 14** Output of CLA multiplier M5–M9

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The glitches can be seen in the outputs, this is due to parallel inputs given to the adders in the circuit. Further works are need to be done in order to remove these glitches.

The inputs shown in the Figs. 6, 7, 8 and 9 are given to Quaternary CIA multiplier and the results are obtained as waveforms in W-Edit.

The output for the Quaternary CIA multiplier is obtained and it is shown in the Figs. 13, 14 and 15.

The output for the first set of the input is shown below.

Inputs:

8 bit Multiplicand, \( A_{7:0} = 00,000,000 \).
8 bit Multiplier, \( B_{7:0} = 00,000,000 \).

Output:

16 bit Product, \( M_{15:0} = 0,000,000,000,000,000 \).

The output for the second set of the inputs is shown below.

Inputs:

8 bit Multiplicand, \( A_{7:0} = 11,111,111 \).
8 bit Multiplier, \( B_{7:0} = 11,111,111 \).
Output:

16 bit Product, \( M_{[15:0]} = 1,111,111,000,000,001 \)

The glitches can be seen in the outputs, this is due to parallel inputs given to the adders in the circuit. Further works are need to be done in order to remove these glitches.

The Table 1 compares the results of the Quaternary CLA Multiplier with Quaternary CIA Multiplier with reference to power, delay, Power-Delay Product (PDP) and number of transistors used for the construction of the design. The transient analysis is done using the Tanner EDA with 250 nm technology.

From the Table 1, it is said that the proposed Quaternary CIA has low power consumption. The Quaternary CLA multiplier consumes power of about 104.18 mW whereas, the Quaternary CIA multiplier consumes 89.76 mW which 13.84% less than it consumes the former. This is due to the minimization of the number of gates used in the proposed method. As the number of transistors is reduced, the switching activity during the working of the design is reduced. Dynamic power of the circuit depends on the switching activity. Since the switching activity is reduced, the dynamic power dissipation of the circuit is reduced.

As per the Table 1, the worst-case delay in obtaining for Quaternary CLA multiplier is 1.298 ns but the Quaternary CIA multiplier has a delay of 1.317 ns, which is 1.44% higher when compared with the existing. This is due to the usage of Ripple-carry adder blocks in the Carry Increment Adder since delay due to carry propagation is more in RCA. But the delay produced by the CIA is less when compared with the RCA. This is due to the usage of two RCAs as parallel blocks in the Carry Increment Adder.

The Table 1 shows that the Power-Delay Product of the proposed is 12.57% lesser then the existing method. Thus, the efficiency is improved in the Quaternary CIA multiplier. The number transistor count in the proposed is also 19.7% less than the existing method, which leads to the lesser area than the Quaternary CLA multiplier.

The existing method uses Quaternary Carry-Lookahead Adder in the multiplier. By replacing the Quaternary CLA with Quaternary CIA in the array connection the power consumption is reduced. The Quaternary CIA is made up of 2 Ripple-Carry Adder and an Increment circuit. The increment adder uses only 4 half adders. The Ripple-Carry Adder consumes less static power than any other adders. The area consumed by the Quaternary CIA is less than Quaternary CLA. The area and power consumption of the circuits are directly related. When the area is reduced, i.e., the number of the transistors used are reduced. The switching activities that take place in the circuits are reduced. The reduction in the switching activity leads to less consumption of the dynamic power in the circuits. This is the reason consumption of low power in the array multiplier. Power-Delay Product is production of the power consumed during switching and the delay. PDP is mainly used

| Performance metrics | Quaternary CLA multiplier | Quaternary CIA multiplier | Percentage |
|---------------------|--------------------------|---------------------------|------------|
| Power (milli watts) | 104.18                   | 89.76                     | 13.84      |
| Delay (nano second) | 1.298                    | 1.317                     | 1.44       |
| Power-delay product (pico watt seconds) | 135.22 | 118.21 | 12.57 |
| No. of transistors | 14,616                   | 11,736                    | 19.7       |
to determine the performance. From the analysis, it can be seen that the PDP of the Quaternary CIA is greater than Quaternary CLA. It makes Quaternary CIA more efficient than Quaternary CLA.

5 Conclusion

In this paper, we proposed a Carry Increment Adder by using QSD number system in order to replace Quaternary Carry-Look ahead Adder in array multiplier circuit. In VLSI, power consumption, delay and area are the factors determining the efficiency of the design. Tanner EDA tool with 250 nm technology is used for the simulation of the circuits and the above-mentioned analysis are done. These analyses are also done for the existing Quaternary Carry-Look ahead Adder multiplier and the results are compared. The QSD offers carry free addition, which minimizes the carry propagation delay that occur during binary arithmetic. This enhances the speed of the Quaternary Carry Increment Adder. Quaternary Carry Increment Adder has a lower power consumption and occupies lesser area than the existing method. This is because, the number of transistors present in the proposed method is lesser than the existing Quaternary Carry-Look ahead Adder multiplier. From the results, we come to know that the PDP of the proposed method is 12.57% reduced proving that the proposed is more efficient. In future works, the area of the designed circuits can be improvised.

In future, the multiplier with Quaternary Carry Increment adder can be used to develop ALU, Processors, filters, etc. The delay of the Quaternary Carry Increment adder can be improvised.

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Declarations

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