A K/Ka-band Switchless Reconfigurable 65nm CMOS LNA based on Suspended Substrate Coupled Line

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ABSTRACT This article presents a K/Ka (18-40) GHz dual-band switch-free reconfigurable 65nm CMOS Low-Noise Amplifier (LNA) realized by inter-stage and output-stage Suspended-Substrate Coupled-Lines (SSCL) for the first time to the author's best knowledge. The amplified input signal from the broadband drive stage is divided into two parallel single band stages by the proposed inter-stage SSCL. Two split-band signals are amplified by the corresponding High-band (Ka) and Low-band (K) stages. The proposed output-stage SSCL combines the amplified two single-bands at the output. The proposed SSCL also provides the required network matching to the LNA. The single band of operation can be achieved by simply turning off the unused transistor band's drain voltage. The proposed LNA achieves a maximum noise figure (NF) taken in dual-mode of 1 dB and 1.2 dB and a gain of 27 dB with 0.2 dB and 2 dB variation in the K-band and Ka-band, respectively. Statistical analysis and design of experiment (DoE) are applied to predict the percentage error tolerance and validate the contribution of the parameters towards gain, return loss, and noise figure. This LNA exhibits an input and output 1-dB compression point (IP1dB & OP1dB), third-order input & output intercept point (IIP3 & OIP3) of -17/-16 dBm, +7.1/6.4 dBm, 0 dBm and +25/+23 dBm over 18-24/25-40 GHz respectively. The fabricated LNA draws 21.4 mA from 1.2 V with a size of 0.61×0.92 mm².

INDEX TERMS Suspended Substrate Coupled Lines (SSCL), Low Noise Amplifier (LNA), CMOS, K-band, Ka-band

I. INTRODUCTION

The K-Ka band (18-40 GHz) applications such as 5th generation (5G) networking, radar, and astronomy detection depend heavily on wideband mm-wave front-ends. As one of the most critical active components, low noise amplifiers (LNAs) are the primary block in the mm-wave receiver front-ends. We expect to achieve a low noise figure, a modest gain, high linearity, and low power consumption for LNAs to extend the dynamic range and increase the receiver system's sensitivity, which adds to the LNA design challenges. In recent decades exhaustive research has been done on wideband LNAs [1]. The most promising topology used to realize the ultra-wideband LNA is a Distributed amplifier (DA) [2]. But DA is not suitable in many cases because of low unity-gain bandwidth, high NF, and larger area. Other bandwidth enhancement techniques such as shunt-resistive feedback, dual inductive peaking, improving dynamic load, a frequency-dependent feedback loop (FDFL), split common gate transistor (SCGT) have been reported in [3-6]. These proposed bandwidth enhancement techniques degrade the other RF parameters like noise performance. The main issue with wideband LNAs is that they amplify the unwanted signal with the desired signal, degrading the receiver's sensitivity. Reconfigurable LNAs are another approach to develop wideband receivers with good interference rejection, and many multiband LNAs are reported in [7-22]. A reconfigurable multimode LNA realized by incorporating a switched multilayer transformer into the input matching network and tunable load based on electrical and magnetic tuning operating at 3 single bands (24/28/39 GHz) is proposed in [8], but they have less gain.
around 12 dB and high NF up to 5 dB.

A 28/60 GHz reconfigurable LNA based on RF switches for mm-wave transceivers is reported in [12]. This LNA also suffers from a feeble gain of 14 dB with an NF of 4.6 dB. By using highly optimized RF switches, they still suffer ON-loss of 1 dB and OFF-loss of 0.7 dB. A 44/60 GHz reconfigurable LNA based on Q-enhanced metamaterial transmission lines is presented in [13], but they have a high NF of 5.6 dB and IIP3 of -14 dBm. The notable advantage of this paper is that it achieves 30 dB rejection between two bands, but they didn't achieve good FoM, and this design is not suitable for wideband frequency of operation. A dual-band switchable LNA based on LC tunable tank and tunable stub based on Hetero-junction Bipolar Transistor (HBT) switch working at 28/60 GHz is reported in [14]. This LNA also has one of the best LNA with triple coupled transformer technique is reported simultaneously controlling stopband rejection and passband gain balance and 4.3 dB dual inductors is presented in [16]. This LNA has one of the best techniques are not suitable for operation and had their design tradeoffs operating at mm-wave bands have only a narrow band of performance and had their design tradeoffs, and their design techniques are not suitable for the wideband application, which is our goal here.

A 22-47 GHz, two-stage LNA with 22.2 dB peak gain and 4.3 dB NF using coupled L-type interstage matching inductors is presented in [16]. This LNA has one of the best design tradeoffs with only the demerit of poor IIP3. The research gap is that the asymmetric L-type inductors used here cause instability due to pole-zero shifts. A concurrent dual-band single-ended input to differential output LNA operating at 18-25 GHz and 33-46 GHz with 16 dB gain and 4.3 dB NF is reported in [17]. Though this LNA has low gain and high NF, it also has a unique advantage in controlling stopband rejection and passband gain balance simultaneously. A 21-41 GHz, 28.5 dB gain, and 3.2 dB NF LNA with triple coupled transformer technique is reported in [18]. This LNA also has one of the best design tradeoffs; still, no LNA has achieved ultra-low NF with high linearity.

In [19], LNA with 12.8 dB gain and 1.4 dB NF operating at 14-31 GHz is reported. This is the only LNA among all the discussed works with NF less than 1.5 dB, but gain falls below 13 dB. A 19.5-28.5 GHz variable low power LNA achieving a gain of 7.8-23.2 dB with a 0.4-1.6 V supply is presented in [20]; still, they have not achieved ultra-low NF. The literature reported in [16-20] is suitable for wideband mm-wave receiver systems, but they have their limitations of the LNA design tradeoffs in gain, NF, linearity, power consumptions, area, and sensitivity. The point of observations in all the reported works except [13] uses one or more components such as tunable inductors, varactors, transformer, and RF switches, which require additional power supplies and are difficult to implement at high frequencies due to the associated loss and tradeoffs.

Considering the drawbacks of the bandwidth enhancement and other reconfigurable techniques for the ultra-wideband LNA, this article proposes a new switchless reconfigurable LNA based on the inter-stage and output-stage Suspended Substrate Coupled Line (SSCL) for the full K-Ka band (18-40 GHz). An 8-20 GHz switchless dual-band reconfigurable LNA and a 6-18 GHz switchless dual-band reconfigurable power amplifier (PA) are reported in [21-22] using a coupled line-based diplexer which is similar to the SSCL used in this article.

This article presents a K/Ka dual-band switchless reconfigurable and wideband LNA based on interstage and output stage SSCL, providing the necessary LNA matching network. The statistical analysis and Design of Experiments (DoE) are done to test the design’s yield and robustness. The DoE analysis notices each passive and active parameter’s percentage contribution and sensitivity to the overall response. This makes the optimization an easy task as it identifies the sensitive parameters perfectly. This CMOS-based switchless reconfigurable LNA has achieved a better LNA design tradeoff with better harmonics and linearity performance comparing the reported works.

This paper outline is presented as: Section 2 explains the suspended substrate coupled line’s design and consideration. The LNA circuit design stages and considerations are discussed in section 3, while the experimental setup, simulation, and measured results with the comparison table are presented in section 4. Finally, the conclusion is given in section 5.

II. SSCL DESIGN AND CONSIDERATION

A. COUPLED LINE ANALYSIS

The traditional coupled microstrip line is shown in Fig. 1 (a). Its analysis is discussed here as an example to understand the proposed SSCL’s dual-band activity mechanism better. In a coupled line structure, the load impedance $Z_{\text{load}}$ is considered to be the same as the coupled line’s characteristic impedance $Z_0$. In this case, the output voltage of the coupled port (port 3) and through port (port 2) can be determined as a function of the input voltage $V_{in}$ denoted in equations (1) and (2).[23]

$$V_{\text{through}} = V_{in} \cdot \frac{\sqrt{1 - K^2}}{\sqrt{1 - K^2 \cos \theta + j \sin \theta}} = T \cdot V_{in} \quad (1)$$

$$V_{\text{coupled}} = V_{in} \cdot \frac{j K \sin \theta}{\sqrt{1 - K^2 \cos \theta + j \sin \theta}} = C_F \cdot V_{in} \quad (2)$$

Where $T = \frac{\sqrt{1 - K^2 \cos \theta + j \sin \theta}}{\sqrt{1 - K^2}}$ and $C_F = \frac{K \sin \theta}{\sqrt{1 - K^2 \cos \theta + j \sin \theta}}$

Voltage coupling factor $C_F$ of port 3 as a function of the coupling coefficient, $K$ and electrical length $\theta$ can be given.
by:
$$20 \log|C_F| = 20 \log \left| \frac{jK \sin \theta}{\sqrt{1 - K^2 \cos \theta + j \sin \theta}} \right|$$

(3)

Here $K$ is the coupled line's coupling coefficient, and $\theta$ is the coupled line's electrical length. According to the current flow mechanism in an electromagnetic situation, there are two modes for the coupled line. In the first mode, the current flows down on the conductor with a contra-flow current back up the other conductor caused by displacement current coupling between the two conductors. This is termed the odd mode current, and it has associated odd mode characteristic impedance $Z_{0o}$. In the other mode, the current flow by displacement current between each center conductor carries the same polarity and the common ground between them. Hence this is called even mode current, and it has an associated even mode characteristic impedance $Z_{0e}$ [23]. The coupling coefficient $K$ as a function of odd mode impedance $Z_{0o}$ and even mode impedance $Z_{0e}$ can be given by:

$$K = \frac{Z_{0e} - Z_{0o}}{Z_{0e} + Z_{0o}}$$

(4)

The relation between the characteristic impedance $Z_0$ and odd and even mode impedance is given as:

$$Z_0 = \sqrt{Z_{0e} Z_{0o}}$$

(5)

From (1) and (2), we can see that at very low frequencies or terse line length ($\theta \ll \pi/2$), nearly all input power is transmitted to port 2, with none being coupled to port 3. The maximum coupled power transmitted to port 3 is achieved at $\theta = \pi/2$ or $l = \lambda/4$, as shown in Fig. 2(a). From Fig. 2(a), the maximum coupled power is approximately -3 dB with a long-coupled line ($\theta = \pi/2$) for $K = 0.7$. For this reason, the traditional coupled line structure in Fig. 1(a) may not be applicable in the proposed LNA.

The scattering matrix $[S]$ of a four-port coupled-line coupler can be written as:

$$[S]_{4x4} = \begin{bmatrix}
0 & -j\sqrt{1 - K^2} & K & 0 \\
-j\sqrt{1 - K^2} & 0 & 0 & K \\
K & 0 & 0 & -j\sqrt{1 - K^2} \\
0 & K & -j\sqrt{1 - K^2} & 0
\end{bmatrix}$$

(6)

The modified structure of the coupled line is shown in Fig. 1(b). The isolated port (port 4) is grounded initially (without $C_F$). The shunt capacitance $C_F$ at port 2 (through port) behaves as a short circuit for ideal high-band frequencies operation. The input impedance matching network of the low-band LNA absorbs this $C_F$ during the low-band frequency operation. The through port output signal is mirrored with an $180^\circ$ phase shift and re-enters the coupled line. The signal is then coupled to the isolated port, mirrored with an $180^\circ$ phase shift, and finally emerges from the coupled port (port 3) with the initial coupled signal. The output voltage of isolated port (port 4) and coupled port (port 3) as a function of the input voltage $V_{in}$ can be expressed as:

$$V_4^+ = C_F \cdot V_{in}^+ + C_F \cdot \Gamma \cdot V_4^- = C_F \cdot \Gamma \cdot V_{in}$$
$$V_3^- = C_F \cdot V_{in} + T \cdot V_4^+ = C_F \cdot V_{in} + T \cdot \Gamma \cdot V_{in}$$

(7)

(8)

Coupled power of port 3 as a function of the coupling coefficient $K$ and electrical length $\theta$ can be expressed as:

$$20 \log \left| V_3^+ \right| = 20 \log |C_F + C_F \cdot T^2|$$

(9)

It is noted that from (8), the coupled port output signal consists of two parts: $C_F \cdot V_{in}$ and $C_F \cdot T^2 \cdot V_{in}$. The phase difference between the two parts is identical to the coupled line's double electrical length, as shown in Fig. 2(b). When the coupled line's electrical length is $\lambda/4$, the phase difference between the two parts of the coupled power is $180^\circ$; then, the minimum coupled power is obtained. Fig. 2(b) and Fig. 2(c) illustrate the coupled power in port 3 of the coupled line shown in Fig. 1(b) according to different coupling coefficient $K$ and electrical lengths $\theta$ of the coupled line. When the electrical length is $30^\circ - 45^\circ$ or $135^\circ - 150^\circ$, maximum coupled power can be obtained for a definite $K$. Here, a maximum coupled power of -4 dB can only be achieved for $K = 0.7$, which is not sufficient to be used in the interstage of the LNA. The phase difference between the two parts of the coupled power $C_F \cdot V_{in}$ and $C_F \cdot T^2 \cdot V_{in}$ is the cause of inadequate coupled power, and it is shown in Fig. 2(d). To compensate for the phase difference between two parts of the coupled power, we added a shunt capacitance $C_S$ to the isolated port. The phase response after adding $C_S$ is shown in Fig. 2(e). From
Fig. 2(d) and Fig. 2(e), without the capacitor $C_8$, there is $180^\circ$ phase difference when the electrical length is $90^\circ$ or $\lambda/4$, causing minimum coupling, but after adding shunt capacitance $C_8$ to the isolated port, the phase difference becomes $0^\circ$ at $\lambda/4$ electrical length which maximizes the coupling.

![Coupled Power of Basic Coupled Line Structure With Proposed SSCL](image)

**B. COMPARISON OF BASIC COUPLED LINE STRUCTURE WITH PROPOSED SSCL**

The proposed coupled line is first tested with the traditional microstrip line (MCL) and Shielded microstrip line (SMCL) shown in Fig. 3(a) as an inter-stage. The schematic of the proposed structure shown in Fig. 4(a) is simulated, and the simulation results in Fig. 5(a) show that the coupling power suffers a loss of around $-4.8$ dB because of the described reason in the above subsection. Due to dispersion, fringing effects, and other EM losses due to mm-waves, the losses occur. We have already developed a wafer-level integrated suspended substrate line (SSL) platform to avoid these losses in our previous work [24].

Based on the SSL, we developed the coupled lines in the SSL platform named Suspended Substrate Coupled Lines (SSCL). The 1-D and 3-D schematics of the proposed SSCL are shown in Fig. 3(b) and Fig. 3(c). It consists of two substrates made of Silicon Nitride (SiN) with a thickness of 25 $\mu$m separated by an air gap of 50 $\mu$m. Each substrate has top and bottom metal layers with a thickness of 2.5 $\mu$m marked as M1, M2, M3, and M4.

The metal layers M1 and M4 act as the ground, while the metal layer M3 act as a signal trace. The metal layer M2 act as a signal reflection path. When the signal passes through the metal layer M3 at such high mm-wave bands, an EM field is developed, which causes a fringing effect around the M3 layer. Additional losses such as dispersion loss and dielectric loss also occur. But here, as the signal trace path has a reflection path (M2) and ground layers (M1, M4), the developed EM field is confined to the air cavity. This allows us to have the minimum loss, and we receive high coupled power at the output.
The schematic of the proposed SSCL as interstage and output-stage are shown in Fig. 4(a) and (b), respectively. The length (L) of the coupled line is 193 µm with 30°–40° electrical lengths over 18-40 GHz. Width (W) and separation distance (S) is 10 µm and 4.93 µm, respectively. The coupling coefficient (K) is 0.72 approximately. Shunt capacitance of $C_7 = 0.01$ pF is added to the through-port, and Shunt capacitance of $C_8 = 0.24$ pF is added to the isolation port to increase coupled power. From the simulation results as shown in Fig. 5(b), over 25-40 GHz, the coupled power is approximately -1.5 dB, which is about 3 dB higher than the traditional MCL (shown in Fig. 5(a). By this, the input broadband signal (18-40) GHz is successfully split into (18-24) GHz at the through-port and (25-40) GHz at the coupled port. The odd mode characteristic impedance $Z_{0o}$ and even mode characteristic impedance $Z_{0e}$ are calculated to be 20.16 Ω and 127.34 Ω, respectively.

Thus, the proposed SSCL can be applied in the reconfigurable LNA’s interstage. Fig. 4(b) is the schematic of the proposed output-stage SSCL, and the simulation result is shown in Fig. 5(c).
It is the symmetric structure of the interstage SSCL with optimized S, L, and Capacitors. Insertion loss is less than 3 dB over 18-24 / 25-40 GHz. This stage combines the signal from the high-band and low-band stages and couples the power to the output as a broadband signal. The phase difference in the coupler is also shown in the same Fig. 5(a), (b), and (c).

III. DESIGN AND ANALYSIS OF CMOS LNA

The simplified block showing the proposed dual-band switchless reconfigurable LNA topology is shown in Fig. 6.

A. BROADBAND DRIVE STAGE DESIGN

The broadband drive stage is the first block in the proposed reconfigurable LNA topology where the input RF signal is received, as shown in Fig. 7. This stage plays a decisive role in the input matching and noise performance of the reconfigurable LNA. It consists of a two cascaded CS stage using the transistor M1 and M2 operating at gate voltage $V_{g1} = 0.43\, \text{V}$. Capacitors ($C_1$, $C_2$) and transmission lines with length $L_1$ and width $W_1$ form the input matching network where the signal passes and is fed to the gate of the transistor $M_1$. The drain and gate voltage are given to $M_1$ and $M_2$ through transmission lines with lengths $L_3$, $L_2$, and $L_5$, $L_4$. Source degeneration is incorporated through the transmission line with length $L_{s1}$ and $L_{s2}$ to $M_1$ and $M_2$ to bring the optimum impedance for minimum NF close to the complex conjugate of input impedance. By this, low NF and input impedance matching is achieved simultaneously. The capacitor $C_3$ is used to block the dc from flowing from the first stage to the next stage.

![Figure 8. Simplified small-signal model of first CS stage for input impedance](image)
The input impedance ($Z_{in}$) of the circuit, which depends mainly on this stage, can be calculated using the simplified small-signal model of the first CS stage as shown in Fig. 8. $Z_{OX}$ denotes the combined impedances of all the preceding stages. For simplicity, impedance in transmission lines such as $L_2$, $L_{S1}$, and $L_1$ is considered inductance. In Fig. 8, $g_m$ denotes the transconductance of the transistor $M_1$, whose value is proportional to the width of the transistor, $C_{gs}$ and $C_{ds}$ denotes gate-source and drain-source capacitance, $C_{Mi}$ and $C_{Mo}$ denotes equivalent input and output Miller capacitance due to gate-drain capacitance $C_{gd}$. $C_{Mi} = C_{gd}(1 - A_V)$, $C_{Mo} = C_{gd}(1 - 1/A_V)A_V$ denotes the gain of the corresponding stage.

The input impedance of the circuit ($Z_{in} = V_{in}/i_{in}$) is calculated as follows:

$$V_{in} = i_{in} \left[ j\omega(L_2 + L_{S1}) + \frac{1}{j\omega C_{in}} \right] + g_m V_{gs} j\omega L_{S1}$$  \hspace{1cm} (10)

Here $C_{in} = C_{gs} + C_{Mi}$ is the equivalent input capacitance at the gate terminal. Substituting $V_{gs} = i_{in}/j\omega C_{in}$ in equation (10) and simplifying gives

$$Z_{in} = \frac{V_{in}}{i_{in}} = \frac{g_m L_{S1}}{C_{in}} + j \left[ \omega(L_2 + L_{S1}) - \frac{1}{\omega C_{in}} \right]$$ \hspace{1cm} (11)

Similarly, the gain of the stage $A_V$ can be calculated and shown in equation 12.

$$A_V = \frac{-g_m}{j\omega C_{in}} \frac{1}{j\omega L_3} \frac{1}{j\omega C_{out}} \left( Z_{OX} \right) \left( \frac{1}{j\omega C_{out}} \right)$$ \hspace{1cm} (12)

The simulated S-parameters of the broadband drive stage are shown in Fig. 9. The gain ($S_{21}$) is above 20 dB till 33 GHz, and it falls to 16 dB at 40 GHz. The return loss ($S_{11}$) is well below -10 dB from 18-40 GHz.

**FIGURE 7.** Schematic of the proposed reconfigurable LNA

**FIGURE 9.** Simulated S-Parameters performance of the separate broadband drive stage.
B. DESIGN OF HIGH BAND (KA) AND LOW BAND (K) LNA STAGES

The broadband drive stage's simulated results show that the gain variation is 7 dB from 18-40 GHz. Though it is challenging to maintain almost gain flatness over the entire bandwidth, the high-band and low-band stages consist of two transistors employed to reduce the gain variation below 2 dB. The low-band stage consists of transistor $M_3$ and $M_6$ in CS two-stage cascaded topology operating in the gate voltage $V_{g3} = 0.4$ V. This stage is designed to operate only in the K-band, from 18-24 GHz. The simulated S-parameters of the low-band drive stage are shown in Fig. 10(a). The gain ($S_{21}$) is 10 dB to 8 dB in the passband of 18-24 GHz, then it falls to 2 dB at 40 GHz. The return loss ($S_{11}$) is well below -10 dB from 18-24 GHz, and high reflections are received above this range.

The high-band stages consist of transistor $M_1$ and $M_4$ in CS two-stage cascaded topology operating in the gate voltage $V_{g2} = 0.47$ V. This stage is designed to operate only in the Ka-band, which is from 25-40 GHz. The simulated S-parameters of the high-band drive stage are shown in Fig. 10(b). The gain ($S_{21}$) is 12 dB to 10 dB in the passband of 25-40 GHz. The return loss ($S_{11}$) is well below -10 dB from 25-40 GHz, and high reflections are received in the 18-24 GHz band. To avoid instabilities due to possible oscillation loops in the multi-device amplifier's complex structure or due to the device's nonlinear behavior, R-C resistive feedback using ($R_1$, $C_{10}$) at the gate and drain of the transistor $M_4$ is incorporated. Connecting the coupled port (port 3) of the output stage SSCL directly to the 50 Ω output load is not advisable. This is because the SSCL is formed using stacked layer by layer formation in the substrate, which is challenging to connect to the output load directly. Also, the impedance of SSCL changes with a change in frequency, which is predominantly inductive. In some worst cases, the impedance may be purely inductive and may cause instability to the circuit. We have connected an R-C ($R_2$-$C_{17}$) circuit between the output stage SSCL and the output load to avoid these all. The connected R-C network neutralizes any abrupt change in inductive impedance that arises in the worst case and improves output matching($S_{22}$).

C. MERGING OF ALL STAGES

After individually designing and testing all the stages like SSCL interstage, SSCL output-stage, Broadband stage, High and low band stages. All the stages are connected, as shown in Fig. 6. The broadband drive stage's output is fed to port 1 of the SSCL interstage, where the signal got divided into two single bands as Ka-band and K-band. Based on the principle of SSCL as described in the previous section. The Ka-band is coupled through port 3 of SSCL, and the leftover K band passes through port 2 and is fed to the corresponding amplifier stages. After getting amplification from the corresponding stages, two single-band signals merged at the output using the designed output stage SSCL. As already described, SSCL at output merges the signal from port 2 and port 3 and gives the broadband signal at port 1 as output. Table 1 shows the total dc drain current in various modes of operation and the drain voltage states of single-band transistors used to achieve switch-free dual-band operation.

D. NOISE FIGURE ANALYSIS

The general method to convert any noisy multi-port network to an equivalent noise-less network plus standard current and voltage noises at the input port is depicted as follows to analyze the complete LNA's noise figure. Representing all of the internal noise sources as current noises, general noisy multi-port can be explained as a combination of a noise-less multi-port and some current noises at the ports, as shown in Fig. 11(a). The input and output ports are represented as port1 and port 2, respectively, and Fig. 11(b) shows the equivalent standard multi-port network.
Equivalent noise conductance $G_u$ is defined as

$$G_u = \frac{I_{nu}^2}{4kTB} = \frac{I_n^2 - I_{nu}^2}{4kTB} = \frac{I_n^2 - |Y_c|^2 V_n^2}{4kTB}$$  \hspace{1cm} (22)$$

This expression is used in the above equation

$$I_{nu}^2 = I_n^2 - \frac{|c|^2}{V_n^2}$$  \hspace{1cm} (23)$$

The optimum source admittance $Y_{S, opt}$ for minimum noise factor is calculated as:

$$Y_{S, opt} = \sqrt{\frac{G_c + G_u}{R_n} - jB_c} = \frac{I_n^2}{V_n^2} - B_c^2 - jB_c$$  \hspace{1cm} (24)$$

The minimum noise figure $F_{min}$ is calculated as:

$$F_{min} = 1 + \frac{G_u + R_n(G_{Sopt} + G_c)}{G_{Sopt}}$$  \hspace{1cm} (25)$$

Finally, the noise factor $F$ of the multi-port is calculated as:

$$F = 1 + \frac{G_u + R_n|Y_s + Y_c|^2}{G_s}$$  \hspace{1cm} (26)$$

The simulated NF of the individual broadband, high band, and low band stages are shown in Fig. 12. The broadband stage NF follows a U shape curve with a maximum value of 1.15 dB at 40 GHz. This shows that the technique discussed above optimized the NF to a low value of 1.15 dB only. The NF of the low band stage is around 1.6 dB in the K band, and it increases above this band. The NF of the high band stage is around 1.2 dB in the Ka-band and is highly intolerable up to 7 dB in the K band.

### E. STATISTICAL ANALYSIS

As the device parameters are subject to Process Voltage and Temperature (PVT) variation, the yield analysis is essential in estimating the actual yield and the confidence levels. The confidence level is the area under a normal Gaussian curve over a given number of standard deviations. The designed LNA is tested for 5% and 1% error tolerance under Gaussian distribution. The results for NF, Gain, and return loss are shown in Fig.13 (a), (b), and (c), respectively. It is noted that the stable gain of 25 dB, NF of 1.6 dB, and return loss of -11 dB are achieved with 1% tolerance. It results in a yield estimation of 100%, giving a 99.7% confidence level for 1000 iterations. But for the 5% tolerance

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**TABLE I**

| Band                  | $V_{dd}$ (V) | $V_{as}$ (V) | Total current |
|----------------------|-------------|-------------|--------------|
| K (18-24) GHz        | 0           | 1.2         | 13.8 mA      |
| Ka (25-40) GHz       | 1.2         | 0           | 14.5 mA      |
| K and Ka (18-40) GHz | 1.2         | 1.2         | 21.4 mA      |

To find equivalent current and voltage source noises at the input port, we describe the network by Y matrix:

$$Y = \begin{bmatrix} Y_{11} & Y_{12} & \cdots & Y_{1N} \\ Y_{21} & Y_{22} & \cdots & Y_{2N} \\ \vdots & \vdots & \cdots & \vdots \\ Y_{N1} & Y_{N2} & \cdots & Y_{NN} \end{bmatrix}$$  \hspace{1cm} (13)$$

Now we define a new matrix:

$$Y' = \begin{bmatrix} Y_{21} & Y_{23} & \cdots & Y_{2N} \\ Y_{31} & Y_{33} & \cdots & Y_{3N} \\ \vdots & \vdots & \cdots & \vdots \\ Y_{N1} & Y_{N3} & \cdots & Y_{NN} \end{bmatrix}$$  \hspace{1cm} (14)$$

Equivalent current and voltage noises in Fig. 11(b) are depicted as:

$$\begin{cases} I_n = \frac{\Delta_{12}I_{n1} + \Delta_{22}I_{n2} + \cdots + \Delta_{N2}I_{nN}}{\Delta_{12}} \\ V_n = \frac{\Delta_{11}I_{n2} + \Delta_{21}I_{n3} + \cdots + \Delta_{N1}I_{nN}}{\Delta_{12}} \end{cases}$$  \hspace{1cm} (15)$$

Where $\Delta_{ij}$ and $\Delta^*_{ij}$ are the determinant of the adjoint matrix of the $ij$th element of the Y and Y' matrix respectively. Using the correlation coefficient $I_n$ and $V_n$, is correlated.

$$c = \frac{I_nV_n^*}{1}$$  \hspace{1cm} (16)$$

$I_n$ can be divided into two terms, one is correlated to $V_n$ and the other is uncorrelated

$$I_n = I_{nc} + I_{nu}$$  \hspace{1cm} (17)$$

$$I_nV_n^* = (I_{nc} + I_{nu})V_n^* = I_{nc}V_n^*$$  \hspace{1cm} (18)$$

The correlation admittance $Y_c$ is defined as:

$$Y_c = G_c + jB_c = \frac{I_{nc}}{V_n}$$  \hspace{1cm} (19)$$

$$Y_c = \frac{c}{V_n^2}$$  \hspace{1cm} (20)$$

Equivalent noise resistance $R_n$ is defined as

$$R_n = \frac{V_n^2}{4kTB}$$  \hspace{1cm} (21)$$

**FIGURE 11.** Noisy multi-port (a) and its equivalent noiseless multi-port network (b) with equivalent current and voltage noise sources at the input

**FIGURE 12.** Simulated Noise Figure performance of the broadband, high band, and low band stages
yield estimation, 10% of the iteration failed to yield 90%. The parameters' limit is set as a minimum 20 dB gain, maximum 2 dB NF, and minimum -10 dB return loss. But usually, CMOS process PVT variations are less than 1% only, which means the designed reconfigurable switchless LNA provides a stable and accurate design.

![Yield estimation graphs](image)

**FIGURE 13.** Yield estimation of LNA (a) Gain (b) NF. (c) Return Loss

**F. DOE ANALYSIS**

Design of Experiments (DOE) is a data-driven technique for robust design to understand the design parameter's contribution in achieving the specific goal like a flat gain of 25 dB, NF of 1.5 dB with good return loss, and high linearity. The design parameter's percentage contribution to the specific goal, such as NF, Gain, and return loss, are shown in Fig. 14. To test at both the K and Ka bands, the LNA is tested at 20 GHz and 35 GHz, shown in Fig. 14 (a) and (b), respectively. It is observed that the same parameter from the broadband drive stage contributes to design goals with the only variation in the percentage sensitivity. It is also observed that the parameter M5_W from the low-band stage contributes to gain a little at 20 GHz, and the parameter M3_W from the high-band stage contributes to gain a little at 35 GHz.

![Parameter contribution graphs](image)

**FIGURE 14.** Design parameter contribution at (a) Low-band at 20 GHz (b) High-band at 35 GHz

The design parameters which contribute less than 1% are neglected in Fig. 14 for better clarity. Extra care has been taken for these sensitive and contributing parameters while fabricating to get reliable, accurate measurement results.

**IV. PERFORMANCE ANALYSIS OF RECONFIGURABLE SWITCHLESS LNA**

The LNA is implemented using RF 65nm process design technology and fabricated using the Magnachip Hynix Samsung process. The fabricated chip is a layer-by-layer formation using substrates and metal oxide metal (MoM) capacitors. The six-layer copper interconnects fabricated using nano-clustering silica. These six layers are stacked up on silicon wafers along with other components of LNA to provide flexibility, which in turn avoids parasitic losses by CMOS mm-wave process. The stacking multi-layer process is used for mounting the passive components on the silicon die. The microchip die photograph of the fabricated LNA is shown in Fig. 15(a). The total core area of the chip is 0.61×0.92 mm². The full-wave simulation and measurement readings of LNA have characterized performance parameters with optimized dimensions to achieve high performance over a wideband of operation.
A. EXPERIMENTAL VERIFICATION

For on-wafer LNA, S-parameters and noise performance are measured using micro-probe sets such as Karl Suss (KSM) microprobe system, PNA-X (N5245B) Keysight's technologies up to 50 GHz, and Cascade Microtech microprobe tips, with 100 µm pitch. The PNA and micro-probes must be calibrated before going to measurement. The short-open-load-through calibration technique has been employed for microprobe systems.

![Microchip die photo of fabricated LNA](image)

**TABLE II**

| Comp  | Value  | Comp  | Value  | Comp  | Value  | Comp  | Value  | Comp  | Value |
|-------|--------|-------|--------|-------|--------|-------|--------|-------|-------|
| M_{1,W} | 88 µm | C_{4} | 0.24 pF | C_{14} | 0.6 pF | L_{7} | 405 µm | L_{63} | 36 µm |
| M_{2,W} | 179 µm | C_{5} | 0.48 pF | C_{15} | 0.47 pF | L_{8} | 438 µm | L_{64} | 23 µm |
| M_{3,W} | 36 µm | C_{6} | 0.44 pF | C_{16} | 0.8 pF | L_{9} | 481 µm | L_{65} | 305 µm |
| M_{4,W} | 24 µm | C_{7} | 0.01 pF | C_{17} | 0.8 pF | L_{10} | 462 µm | L_{66} | 452 µm |
| M_{5,W} | 192 µm | C_{8} | 0.24 pF | L_{1} | 430 µm | L_{11} | 100 µm | R_{1} | 1 KΩ |
| M_{6,W} | 184 µm | C_{9} | 0.15 pF | L_{2} | 157 µm | L_{12} | 384 µm | R_{2} | 47 Ω |
| W_{1} | 10 µm | C_{10} | 0.5 pF | L_{3} | 510 µm | L_{13} | 148 µm |       |       |
| C_{1} | 2.6 pF | C_{11} | 0.18 pF | L_{4} | 520 µm | L_{14} | 362 µm |       |       |
| C_{2} | 0.14 pF | C_{12} | 1.6 pF | L_{5} | 500 µm | L_{41} | 35 µm |       |       |
| C_{3} | 1.6 pF | C_{13} | 0.02 pF | L_{6} | 94 µm | L_{42} | 2 µm |       |       |

The calibration sets include gold short circuits (Short), gold open pads (Open), and gold plus thin film resistors (Load or Match) [25]. The complete measurement setup using PNA-X is shown in Fig. 15(b). PNA-X uses a more accurate cold source method than the usual Y-factor method, where the NF of the device under test (DUT) is calculated from two separate measurements. The first measurement is the available gain of the DUT. This is done with great precision using vector air corrected S-parameters measurement. The second measurement is the noise power coming from the output of the DUT, with room temperature (25°C) loaded at the input. This PNA-X noise figure option includes a built-in low noise receiver with 3 different gain settings. This means a broad range of devices with any combination of gain and NF can be tested without the need for any additional hardware.

Vector Air corrected S-parameters correct the mismatch between the imperfect source match of the test system and the input impedance of the DUT. Mismatch correction is also applied when measuring the DUT output noise power. The source mismatch caused by the KSM probes and microprobe-tips is corrected using the standard impedance tuner module. By varying the source impedance presented to the input of the DUT, and measuring the resulting NF, accurate 50 Ω NF is calculated. Pasternack PE6085 50 Ω impedance converter adapter connector is used for good output match of S_{22}. The comparison of state-of-art LNA with other reported ones is shown in Table 3. The FoM expressions are given below.
The input and output impedance of the dual-band LNA is shown as a smith chart in Fig. 16. It is noted that the input impedance starts from the capacitive region at 18 GHz marked as m3 and touches the real axis at 20 GHz. It then follows the inductive region and again touches the real axis at 28 GHz, marked as m2. From m2, it again passes through the capacitive region and touches the real axis at the end frequency 40 GHz marked as m1.

The output impedance is capacitive dominance from starting frequency 18 GHz marked as m6 and meets the real axis at 25 GHz, marked as m4. Hence it is noted that the K-band (18-24) GHz impedance is capacitive, and Ka-band (25-40) GHz impedance is inductive. For the RF frequency range, the stability is determined using the K factor that depends on S-parameters. To achieve stability, it is required to have $K > 1$ and $\Delta < 1$.

Both $K$ and $\Delta$ are given by the equations given below.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2 |S_{12}S_{21}|}$$ (29)

$$\Delta = |S_{11}S_{22} - S_{12}S_{21}|$$ (30)

LNA stability is measured and plotted in Fig. 17. It is noted that the designed reconfigurable switchless LNA is unconditionally stable in the desired frequency range of 18 to 40 GHz.

The measured and simulated NF and S-parameters of the proposed reconfigurable switchless LNA in all three modes, dual-band mode, high-band mode, and low-band mode, are shown in Fig. 18 to Fig. 20. It is noted that from Fig. 18, the NF varies from 1.05 dB at 18 GHz to 1.2 dB at 40 GHz in dual-band mode with a minimum of around 0.9 dB at 21 GHz. The gain of 27 dB with only 0.2 dB variation and 2
dB variation is achieved across the entire frequency range of 18 to 24 GHz and 24 to 40 GHz, as seen from Fig. 19(a). This is phenomenal performance in terms of gain for having such a slight variation for the entire 22 GHz bandwidth comparing the reported works discussed. The return loss ($S_{11}$) is sufficiently well below 10 dB to avoid any reflection. Other parameters, such as $S_{12}$ and $S_{22}$, also show satisfactory performance. The simulated Group delay and the phase response for the proposed LNA in dual-band are shown in Fig. 19(b) also provides satisfactory performance.

![Figure 19](image1.jpg)

**FIGURE 19.** (a) Simulated and measured S-parameters of the designed LNA in dual-band mode (b) Simulated Group delay and phase response.

As seen in Fig. 20(a), a stable gain of 22 dB with 2 dB variation is achieved in Ka-band mode (25 to 40 GHz) in high-band mode. NF of around 1.5 dB is achieved with a good return loss of below 10 dB. In low-band mode, as seen in Fig. 20(b) stable gain of 25 dB with 1 dB variation is achieved in K-band mode (18 to 24 GHz). NF of around 1.5 dB is achieved with a good return loss of below 10 dB.

![Figure 20](image2.jpg)

**FIGURE 20.** Measured S-parameters and NF of the designed LNA in (a) high-band mode (b) low-band mode.

![Figure 21](image3.jpg)

**FIGURE 21.** Pin vs. IP3, IP2, and Pout (fundamental) at (a) K-band (b) Ka-band
The linearity analysis has been done to compute the fundamental signal’s harmonics, such as third-order harmonics. Here as we are dealing with mm-wave bands till 40 GHz, even second harmonics analysis has been done. The measured values at 20 GHz (K-band) and 35 GHz (Ka-band) are shown in Fig. 21(a) and (b), respectively. From the plot, it is noted that at 20 GHz Input 1-dB compression point (I_{IP1dB}) of -17 dBm, output 1-dB compression point (O_{IP1dB}) of +7.1 dBm, Input intercept Third-order point (OIP3) of 0 dBm, output intercept Third-order point (OIP3) of +25 dBm and Input intercept second-order point (IIP2) of +5 dBm are achieved.

Similarly, it is observed from the Fig. 21(b) at 35 GHz Input 1-dB compression point (I_{IP1dB}) of -16 dBm, output 1-dB compression point (O_{IP1dB}) of +6.4 dBm, Input intercept Third-order point (IIP3) of 0 dBm, output intercept Third-order point (OIP3) of +23 dBm and Input intercept second-order point (IIP2) of +5 dBm are achieved. This value shows that our designed reconfigurable switchless LNA performs better in suppressing harmonics to provide high linearity to the input. This is achieved by using optimized source degeneration using transmission lines at each CS stage to keep the gain under 28 dB and proposed SSCL at interstage and at the output to reduce the intermodulation distortion effects (IMD). The IIP3 increases automatically once the IMD reduces, which results in a better linear device.

V. CONCLUSION

This article demonstrates and fabricated a switch-free reconfigurable dual-band LNA operating in 18-40 GHz in 65nm CMOS technology. We theoretically analyzed and developed Suspended Substrate Coupled Lines (SSCL) in the interstage and output-stage to obtain frequency reconfigurable capabilities. The input dual-band signals are divided into single band amplifiers by the interstage SSCL and combined in the output port by the output-stage SSCL. The unit transistor of the proposed LNA is designed in Common-Source (CS) architecture and uses the inductive effect of transmission lines to degenerate the source by obtaining low noise and input matching simultaneously. The fabricated 0.56 mm² LNA chip exhibits a measured small-signal gain of 27-27.2 dB with around 1 dB NF in 18-24 GHz and a measured small-signal gain of 25-27 dB with around 1.2 dB NF in 24-40 GHz. The statistical and DoE analysis is presented to test the yield and robustness of the design. The designed LNA is highly linear by achieving I_{IP1dB} of -16 dBm, IIP3 of 0 dBm, O_{IP1dB} of +6.4 dBm, OIP3 of +25 dBm. The proposed chip also consumes only 25.7 mW in the dual-band operation. The reason for having three modes of operation is to minimize the power dissipation by 8-9 mW which comes in handy during limited power supply in remote areas. The state of art comparison shows that the designed LNA achieves reasonably well mean values in all parameters, leading to achieving the highest FOM among the reported works and applied in modern wireless receiver systems.

| Ref | Tech | Freq (GHz) | Gain (dB) | NF (dB) | I_{IP1dB} (dBm) | IIP3 (dBm) | O_{IP1dB} (dBm) | OIP3 (dBm) | P_{dc} (mW) | Area (mm²) | FOM | FOM_{(P)} |
|-----|------|------------|-----------|----------|----------------|-----------|----------------|------------|-----------|-----------|-----|-----------|
| [8] | 45nm SOI | 24-28 | 9.5-12 | 15.5 | 4.5 | 4.5-5.5 | -12 | -13 | N/A | N/A | N/A | 15.5 | 0.317 | 0.3 | N/A |
| [14] | 130nm SiGe | 28-60 | 16.2 | 15 | 5.5 | 6.5 | -12 | -7 | N/A | N/A | N/A | 8.2 | 21 | 0.1 | 0.3 | N/A |
| [15] | 28nm CMOS | 24-33 | 29.9 | 32.4 | 32.3 | 5.5 | -40 | -42 | N/A | N/A | N/A | 25.6 | 0.22 | 0.4 | N/A |
| [16] | 130nm SiGe | 22-47 | 22.2 | 3-4.3 | N/A | -13.8 | N/A | N/A | 9.5 | 0.13 | 19.1 | 0.76 |
| [17] | 180nm SiGe BiCMOS | 18-25 | 16 | 17 | 4.3 | 4.3 | -24 | -15 | N/A | N/A | N/A | 73.8 | 0.69 | 0.7 | 0.02 |
| [18] | 65nm CMOS | 22-40 | 28 | 3.2 | -25 | N/A | N/A | N/A | 32 | 0.4 | 14 | N/A |
| [19] | 45nm CMOS | 14-31 | 1.8 | N/A | 5 | N/A | N/A | N/A | 15 | 0.3 | 12 | 38.4 |
| [20] | 22nm FDSoi | 23-27 | 28.5 | 2.4 | -21 | -10.4 | N/A | 1.95 | 20 | 0.19 | 7.6 | 0.76 |
| [21] | 150nm GaAs | 8-10 | 25-25.2 | 13.1-1.4 | N/A | 0.5-1.7 | 0.76 | 227.5 | 3.6 | 1.8 | N/A |
| This Work | 65nm CMOS | 18-24 | 27-27.2 | 0.85-1.05 | -17 | 0 | +7.1 | +25 | 16.5 | 0.56 | 59.9 | 40.7 |

TABLE III: COMPARISON WITH STATE OF ART.
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