A Synchronous Rectified Flyback AC-DC Converter Using Capacitor-Coupled Isolated Communication

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Abstract This paper presents a synchronous rectified (SR) flyback AC-DC converter based on capacitor-coupled isolated communication. Instead of bulky opto-couples as isolators, the proposed converter integrates an isolated capacitor to accomplish communication between the primary and secondary side, in an attempt to reduce system size. In secondary side, an adaptive zero-current detector (ZCD) for driving synchronous rectifier is adopted to increase efficiency. The converter is designed and fabricated in a 0.18-μm BCD process. The experimental results demonstrate that our scheme shrinks the isolator size by a factor of 52.24 times and simultaneously improves the system efficiency by 3% with ZCD.

Key words: synchronous rectified, flyback, capacitor-coupled, zero-current detector

Classification: Integrated circuits

1. Introduction

With the rapid development of portable electronics and the quick charging technology of batteries, there is a growing need for significant power density improvement for travel chargers or adapters [1, 2, 3]. The flyback AC-DC converters for chargers have been widely used in portable devices [4, 5, 6, 7], such as laptop, tablet and smart phone, etc. In flyback topology, the sensing of the outputs and communication of feedback signals for regulating output voltage or current is usually accomplished by utilizing external safe isolation components [8]. The known method uses opto-couplers but adds unwanted size as well as cost to flyback converter [9, 10, 11]. In addition, they suffer from CTR degradation over time and temperature [12]. The primary-side control scheme uses an auxiliary winding instead of opto-coupler to achieve the output voltage information [13, 14, 15, 16]. However, it decreases the accuracy of output voltage and increases the size of transformer. [17] introduces secondary-side control with magnetically coupled isolation. It directly senses the output voltage without additional winding, which increases output voltage accuracy. Meanwhile, the isolated magnetically coupled conductive loops integrated in IC package reduce the size of the converter. But the signal coupled from magnetic lead frame is easily interfered by external electromagnetic under certain condition.

Any size reduction through isolation innovation should be accompanied by efficiency improvement to maintain low component and adapter case temperatures. Therefore, a synchronous rectified (SR) flyback converter under discontinuous conduction mode (DCM) is usually adopted [18, 19, 20, 21]. While operating in DCM, the secondary side inductor reverse current may occur if synchronous switch is turned off later. The reverse energy flowing from the secondary side to the primary side increases the conduction loss and degrades system efficiency [22]. If turned off early, the converter would suffer from body diode conduction loss of the switch. Therefore, a zero-current detector (ZCD) is required for synchronous switch to trigger the switch turning-off at the zero-crossing point [23, 24, 25, 26]. Such featured ZCD is usually realized by a high-speed voltage comparator with a small fixed offset [27] to enable an early output to compensate for the response delay. However, this is impractical due to both the offset and the delay are process-voltage-temperature (PVT) dependent.

Motivated by the concerns above, a SR flyback using capacitor-coupled isolated communication for AC-DC converter is proposed in this paper. The output voltage or current is regulated by secondary side feedback, and then a digital signal is transmitted to primary side to control the main switch through isolated capacitor. Moreover, a dedicated ZCD utilizing a comparator with tunable input offset is employed in secondary side. It can perform self-calibration according to the secondary side switching voltage, therefore ensuring precise gate driving regardless of PVT factors.

2. System Architecture

Fig. 1 shows the proposed two chips solutions for the SR flyback converter with capacitor-coupled isolation. The primary-side controller (PSC) IC integrates three different kinds of 700 V MOSFETs. QH provides startup from the 85-265VAC input AC mains. It is turned on during startup and off after the power for PSC is built up. QF is the main switch of the converter and responsible for delivering input power to the output according to the loading condition. The switch
Q_{P,CS} copies 1/450 current flowing Q_P to detect the primary peak current. The method can decrease power losses compared with adding a sense resistor. The PWM control signal comes from the isolated capacitor and receiver at RX pin. The secondary side controller (SSC) IC is mainly used to implement the proposed adaptive ZCD for synchronous switch Q_S and provide output voltage regulation scheme.

To successfully communicate between PSC and SSC, a hand-shake flowchart is proposed in this paper as shown in Fig. 2. The communication starts when the PSC is powered on. The PSC initially switches with fixed on-time and frequency to power up the SSC. Meanwhile, the PSC waits for the respond from the secondary. If the waiting exceeds time T_s, then the PSC enters restart mode and the SSC starts powering down. After the time T_RST, the PSC retries to power up SSC. Under normal condition, after SSC powered up, the handshake procedure between the primary and secondary starts. When the switching information from PSC is detected by SSC, the secondary will try to transmit a control pulse to the primary. If the PSC succeeds receiving the pulse from SSC, it will switch according to the control pulse. The SSC continue waiting for the respond from PSC. The switching respond can be achieved from pin SSW. Upon receiving the PSC switching information, the SSC will resend a pulse to the primary and restart the process until receiving the second pulse from PSC. During the handshake procedure, any of the check failing results in restarting the protocol between primary and secondary. When the handshake succeeds, the PSC stops switching and hands over control to SSC. The secondary starts transmitting pulse to the primary based on output voltage and current. In the event of a fault condition such as the primary does not respond to switching requests from the secondary, the SSC stops sending signals and PSC has no switching. The SSC starts powering down until PSC restarts switching.

To facilitate the understanding on operation of ZCD, some key waveforms are shown in Fig. 3. The proposed ZCD works during t_{dem} subinterval, where Q_P is off and Q_S conducts. The secondary side inductor current I_{SEC} starts to decrease when Q_S is on. Normally, the Q_S should be turned off when I_{SEC} drops to zero. However, due to the delay of
ZCD and gate driver, a reverse current may occur. This current will pull secondary side switching node voltage $V_S$ up to $V_{out} + V_{in}/N$, where $V_{out}$, $V_{in}$, $N$ are the output voltage, input voltage and turn ratio of the converter, respectively. The high peak voltage results in large primary side power loss. Thus, the ZCD is designed to be negative-offset in order to turn off $Q_S$ before $I_{SEC}$ becomes zero. If $Q_S$ is turned off early, $V_S$-undershoot [25] will appear because the remaining current $I_{SEC}$ flows through $Q_S$’s body diode, and it induces extra power loss. To achieve the ideal switching for $Q_S$, a self-calibration algorithm is employed in proposed ZCD. We assume that the ZCD employs a voltage comparator with tunable input offset. The circuit implementation of this comparator will be discussed in the next section. The voltage $V_S$ is monitored at each switching cycle and its width $t_d$ is recorded if $V_S$-Undershoot occurs. Comparing $t_d$ with a predesigned nanosecond $t_{ideal}$, then an improved switching operation for $Q_S$ is employed at the next cycle according to the comparison result. If $t_d$ is larger than $t_{ideal}$, the excess dead time happens, and the input offset will be increased in the subsequent cycle to turn off $Q_S$ later. The similar operation is performed when $t_d$ is less than $t_{ideal}$. The same process continues until the optimum input offset is finally achieved and $t_d$ equals to $t_{ideal}$.

3. Circuit Implementation

3.1 Circuit Implementation of the isolated capacitor

Fig. 4 is the cross section of the integrated isolated capacitor process. The capacitor top plate is comprised of top metal and bottom plate is formed by a doped n+ layer in p-type well. The p-well is placed in a deep n-well which is tied to the supply voltage vdd. Due to the bottom plate surrounded by p-well and deep n-well, the structure can decrease the mutual interference on received signals between capacitor and other circuits. Moreover, utilizing N+ active region is able to reduce the equivalent resistance and parasitic capacitance, further improving the reliability of transferring useful signal. Between the top and bottom plate, oxide such as SiO$_2$ is used, as the isolation barrier material. The field strength of SiO$_2$ is about 700 Vrms/um [28]. Standard 0.18 um CMOS process can provide > 2.5 um SiO$_2$ dielectric isolation barrier, and over 1.5 kV isolation rating can be achieved.

3.2 Circuit Implementation of the isolated capacitor

Fig. 5(a) describes the circuit implementation for the proposed ZCD. The designed ZCD is based on $V_S$ detection.
and it is comprised of a comparator with adjustable voltage. A high voltage (HV) MOSFET M₀ is applied to endure high voltage stress at Vₛ from the pad SSW. When Vₛ is below certain voltage value, M₀ will operate in the triode region and the voltage Vₛ can be transmitted to the input of comparator with no distortion. The comparator consists of a common gate structure which can swiftly sense the voltage difference between the source nodes of M₁ and M₂. The input pair M₁-M₄ and current mirror M₅-M₈ form the folded cascode topology. Due to large output resistance, high gain and accuracy of current matching are achieved. The adjusted input offset is realized by M₁₃. M₁₃ has a tunable saturation current Iₘ₁₃ controlled by its gate voltage Vctrl, which is generated by offset control module. Equations (2) and (3) can be derived from the unbalanced input pair, where Iref is the bias current for the comparator and VOS is the equivalent input offset of the comparator. The transistor parameters K, VTH, W and L are transconductance parameter, threshold voltage, channel width and length, respectively.

$$V_{OS} = I_{ref} \cdot (R_2 - R_1) - \frac{2R_2K(W/L)_{M13}(V_{ref} - V_{TH} - I_{ref} \cdot R_1) + 1}{2R_2K(W/L)_{M13}}$$

Here, the resistance R₂ is set lower than R₁, so that a negative offset is achieved. As illustrated in Fig. 5(b), the offset control module employs some dedicated control logics to detect “Vₛ-Undershoot” and records its pulse width t_d. The gate voltage of M₃, VCTRL represents the information t_d. Similarly, the gate voltage of M₄, VDIS represents the ideal pulse width t_ideal. Both of them charges or discharges the capacitor CCTRL to adjust the value of VCTRL. In such a way, the input offset of comparator changes, realizing the self-calibration as explained in section 2. An increased (reduced) VCTRL results in a larger (smaller) input offset, which will postpone (advance) the comparator triggering point in the subsequent cycle. The final triggering point for Q₅ is determined by the preset t_ideal and M₄.

4. Measurement Results and Discussions

The proposed synchronous rectified flyback converter with the capacitor isolation has been implemented with 0.18-μm 700 V BCD process and is shown in Fig. 6. The active die area of the primary-side controller is 8.64 mm², including a 700 V HV NMOS to withhold the 220 V|rms input voltage, 2 kV isolated capacitor and control logics. The integrated isolated capacitor occupies only 0.014 mm², if including package, 0.31 mm², which has significantly
×52.42 reduction in system size compared with the smallest opto-coupler [29]. The novel adaptive ZCD and voltage/current regulation scheme are implemented in the secondary-side controller as depicted in Fig. 6(b). The 90 ~ 220 V|rms input and 5 V, 2 A output flyback converter utilizes a 1.5 mH off-chip transformer, a 560 µF off-chip output capacitor and a synchronous rectifier SI7478DP [30].

Fig. 7 shows the measured waveforms during startup in primary-side controller and secondary-side controller, respectively. As shown in Fig. 7(a), when the system is powered up, it enters into primary-side control mode (PCM). The system switching operation is independent of the secondary until receiving pulses from the secondary. The normal handshake process lasts four switching cycles. Then the secondary takes over control and the system starts to regulate output voltage on certain load condition. The secondary-side controller has the same process as shown in Fig. 7(b). When the primary operates in PCM, the secondary powers up through the SSW pin or directly from output voltage. Then it transmits handshaking pulses to the primary and waits for the respond of the primary. After handshake proceed, the secondary takes over control.

The performance evaluation for the proposed ZCD is carried out through a comparison between: (1) the SR flyback converter with the proposed adaptive ZCD; and (2) the SR flyback converter with the conventional ZCD, which is the comparator with fixed input offset. The measurement result of the comparison is shown in Fig. 8. Due to the fixed input offset, the flyback converter with conventional ZCD demonstrates a nonnegligible “V_s-Undershoot” and the width is about 1.4 µs. In Fig. 8(b), the converter with the proposed ZCD demonstrates nearly no “V_s-Undershoot” and the Q_s is turned off at the precise zero current crossing. Fig. 9 shows the measured efficiency over different loads under 110 V|rms input. The proposed ZCD improves the efficiency by up to 3% at 0.4 A load.

5. Conclusion

A SR flyback AC-DC converter based on capacitor-coupled isolated communication applied in adapter or charger is presented in this paper. To accomplish the communication between the primary and secondary side, an integrated isolated capacitor is employed for reducing the size as well as cost of the converter. By monitoring the converter secondary side switching node voltage, the operating condition of the synchronous rectifier can be estimated and adjusted. After several adjusting cycles, the near-optimal turn-off time is obtained. A 10 W lab-made prototype of SR flyback converter is built up to verify the driving strategy. The experimental results show that the proposed ZCD technique can achieve near zero current when the synchronous switch is turned off. Besides, the power efficiency of the converter can be improved from 79.5% to 82.4% at 110 V|rms input and 0.4 A load current.

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