Trigger Merging Module for the J-PARC E16 Experiment

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Abstract—An experiment to measure an invariant mass of φ mesons in nuclear medium is planned as the J-PARC E16 experiment. A trigger merging module (TRG-MRG) has been developed to detect leading-edges from 256 channels of discriminator-output signals and transmit those serialized hit data to trigger decision module with four optical links. The result of the test shows enough performance of the TRG-MRG as 1 ns TDC and data multiplexer with four 6.25 Gbps transceivers.

I. INTRODUCTION

A major part of the hadron mass in vacuum is considered to be originated from the spontaneous breaking of chiral symmetry characterized by quark condensate. It is expected that, at finite density or high temperature, the broken symmetry restores partially and the hadron mass is modified. The J-PARC E16 experiment measures an invariant mass of φ mesons in nuclear medium and investigate the partial restoration of breaking of chiral symmetry at nuclear density [1], [2].

In the experiment, φ mesons are produced in nuclei by the exposure of 30 GeV proton beam of $1 \times 10^{10}$/pulse, with a duration of 2 s, to nuclear targets at the high momentum beam-line at J-PARC. We measure φ mesons in the electron-positron decay channels and reconstruct the invariant mass.

A. Setup of Spectrometer

Figure 1 shows a top view of the spectrometer. Four types detectors are used for momentum measurement of electron/positron. From an inner side, silicon-strip detectors (SSD) and three layers of GEM trackers (GTR1, 2, 3) are located in the strong magnetic field for flight-path detection and momentum reconstruction [3]. The electron/positron identification is performed with hadron-blind detectors (HBD) and lead-glass calorimeters (LG) [4]. The number of readout channels is 112,996 and waveform data from all types of detectors are taken to solve piled up signals. The waveform data are buffered with modules using APV25-S1 chips [5] and DRS4 chips [6] with the buffering-time of 4 $\mu$s and 2 $\mu$s, respectively [7]. Therefore required latency for the trigger signal is less than 2 $\mu$s.

B. Trigger System

For the trigger generation, discriminator-output signals from GTR3, HBD, and LG are used. The number of trigger channels

Fig. 1. (Top) Top view of the spectrometer. (Bottom) Enlarged view of the one-module of detectors.
is 2,620. The maximal single rate is expected to be typically 1 MHz/ch and the minimal width of the discriminator-output signals is 3 ns. Therefore the sampling time must be less than 3 ns. Overview of the trigger system is shown in Fig. 2. Analog signals from detectors are discriminated by DRS4 ADC/TDC or ASD (Amplifier-Shaper-Discriminator) developed for the experiment [8]–[10]. In the trigger merging modules, called TRG-MRG, leading-edges are detected and serialized data of them are transmitted to a trigger decision module by optical transceivers. Belle II UT3, that has 16 QSFP+, is used for them.

The latency of the detection of the leading-edge and transmitting, TRG-MRG, leading-edges are detected and serialized data of them are transmitted to a trigger decision module by optical transceivers. Belle II UT3, that has 16 QSFP+, is used for the trigger decision module [11]. Finally, the trigger signal is distributed to readout modules by Belle II FTSW [12].

The latency before the TRG-MRG is estimated to be 600 ns, mainly due to the drift time of GTR3, To make the latency less than the waveform buffering-time of 2 µs, we design the latency of the detection of the leading-edge and transmitting, trigger decision, and trigger distribution as 500 ns, 500 ns, and 300 ns, respectively. With the design value, the total latency including the drift time of GTR3 becomes 1,900 ns.

The requirement to the TRG-MRG is summarized in Table I.

| **Point**                        | **Value**              |
|----------------------------------|------------------------|
| Function                         | TDC + Optical Transceiver |
| Cable Reduction                  | 2,620 LVDS → <64 optical cables |
| Single Rate                      | 1 MHz/ch               |
| Sampling Time                    | <3 ns                  |
| Latency                          | <500 ns                |

II. DEVELOPMENT

Figure 3 is a picture of the TRG-MRG. The module consists of one main board and two mezzanine cards. The mezzanine card has four 32 channels LVDS receivers and converters from LVDS to 1.8 V LVCMOS format and is replaceable according to the formats of the input connectors. In the main board, two FPGAs (Xilinx Kintex-7 160T-2 and Xilinx Spartan-3 50AN-4), two crystal oscillators of 125 MHz, and eight SFP+ transceivers are installed [13], [14]. The 1 ns and 256 channels multi-hit TDC and 6.25 Gbps and four-lanes GTX transceivers are implemented in the Kintex-7 by Vivado2017.2 provided by Xilinx. The channel reduction from 2,620 channels to maximal 64 optical transceivers is realized by using about 15 TRG-MRGs.

![Fig. 2. Overview of the trigger system.](image1)

**TABLE I**

| **Point**                              | **Value**          |
|----------------------------------------|--------------------|
| **Function**                           | TDC + Optical Transceiver |
| **Cable Reduction**                    | 2,620 LVDS → <64 optical cables |
| **Single Rate**                        | 1 MHz/ch           |
| **Sampling Time**                      | <3 ns              |
| **Latency**                            | <500 ns            |

![Fig. 3. The picture of the TRG-MRG.](image2)

![Fig. 4. The diagram of the firmware implemented in the TRG-MRG.](image3)

A. Firmware

The diagram of the firmware implemented in the FPGA is shown in Fig. 4. The firmware of TDC and transceiver sections is explained in the following paragraphs.

1) TDC Section: The TDC section consists of deserializers, edge detectors, delay controllers, and hit buffers. The input signals are sampled with 1 ns by 500 MHz DDR (Double Data Rate) deserializers of Vivado IP core, I$\text{SERD}$ESE2. The component converts 1 Gbps to four 250 Mbps. In the edge detector, leading-edges are detected from each 4 bits data. To calibrate the intrinsic time difference among channels, delays are added in the delay controller. The component is implemented by using RAM based shift register to save the number of flip-flops and able to delay the data of each channels up to 1,024 ns with a 4 ns unit. If the leading-edges are detected, the hit timing and channel number data are buffered in the hit buffer. Maximal eight hits data are buffered for 64 ns in each 64 channels. The efficiency of event transfer with this criteria is discussed in Sec. III-C. The data to the transceiver section have the width of 32 bits and are output during 5 cycles in each 64 channels.

2) Transceiver Section: The transceiver section consists of FIFO and Aurora8B/10B protocol [15]. The Aurora8B/10B is a link-layer protocol for high-speed serial communication. Because the clock frequency in the protocol is determined from the line rate and lane width of the transceiver, FIFO is installed for clock domain crossing. In the Aurora transmit-
Fig. 5. The schematics of the circuit setup for the measurement of the time resolution.

Fig. 6. An example of the distribution of measured time difference.

III. PERFORMANCE EVALUATION

Items of evaluated performance are described below.

A. Time Resolution

The time resolution was evaluated by inputting two signals with a fixed delay to two channels of the TRG-MRG as illustrated in the Fig. 5. The time difference of the output from the TRG-MRG was measured as shown in Fig. 6. The time resolution is defined from the distribution as \( \sigma / \sqrt{2} \). The measured resolution depends on the remainder of \( (t_{in} - t_{out}) / \text{LSB} \), represented as \( t_{in} \) in this paper, as \( \sqrt{t_{in}(1 - t_{in})} \). The measured distribution is in good agreement with the expected quantization error as shown in Fig. 7. The time resolution of better than 0.35 ns are obtained.

B. Integral Non Linearity

The integral non linearity (INL) was estimated by the same data described in Sec. III-A. Figure 8 shows the relation between input time difference and output time difference. By fitting the measured points as \( At + B \) and calculating the residual between the measured points and the fitting line, the INL was estimated as maximal value of the residual of \([-0.04 \text{ LSB}, +0.04 \text{ LSB}] \) (fig. 9). The effect of INL turned out to be negligible for the performance.

C. Differential Non Linearity

In the TRG-MRG, the differential non linearity (DNL) is expected to be originated from the deserializer. The accuracy of the output from clock generator and the skew of interconnection length in the deserializer make the DNL worse. As mentioned above, the input data are deserialized to 4 bits in each 4 ns. Therefore, the DNL is expected to have a periodicity of 4 ns. The DNL measurement was performed by code density test with a clock with the period of 80.008 ns. The edges of the input clock is expected to distribute with the interval of 0.008 ns into the expected periodicity of 4 ns. The distribution of the those edges is shown in Fig. 10. As expected, the 4 ns periodicity is seen. The DNL was estimated at \([-0.022 \text{ LSB},

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D. Minimum Pulse Width

As mentioned previously, the TRG-MRG must detect the narrow signal of 3 ns, expected in the experiment. By inputting such narrow signals, the detection efficiency was measured. As the result, it is understood that the TRG-MRG can detect signals of 1.0 ns width in 100% efficiency. Therefore, the performance of the TRG-MRG about minimum pulse width satisfies the requirement from the experiment.

E. Double Pulse Separation

The double pulse separation was estimated by measuring the signal detection efficiency with changing the width between the trailing-edge of first signal and the leading-edge of second signal, shown in Fig. 12. The TRG-MRG can discriminate two signals with the interval of 2.5 ns in 100% efficiency. From the result, the inefficiency due to the TRG-MRG is estimated to be 0.27% at the worst case.

F. Latency

The latency was evaluated in two sections, TDC and transceiver sections as defined in Sec. II-A separately.

1) TDC Section: The latency of the TDC section was estimated by using a logic simulator in Vivado. The latency before the TRG-MRG is 600 ns, which delays added by delay controller is included. The result is shown in Fig. 13. Including the buffering-time of 64 ns, the latency of the TDC section is maximal 179 ns.

2) Transceiver Section: The latency of the transceiver section is measured by inputting the output of 250 MHz counter to the FIFO and receiving the data passing Aurora and optical cable of 1 m (expected length). The latency is mainly defined from necessary time for data receiving (deserializing and decoding). Figure 14 shows a schematic view of the measurement. The data are transmitted in five cycles (20 ns) continuously in each 16 cycles (64 ns) of 250 MHz clock, corresponding to the transmission in the experiment.

The obtained result is shown in Fig. 15. The latency of 290 ns is obtained for 99.8% data, which is consistent with the
result from a measurement with a logic analyzer in Vivado. On the other hand, the data of 0.2% have longer latency of 310 ns. It seems to be due to the busy signal of Aurora protocol for clock compensation. Clock compensation is the basic function of the Aurora protocol and outputs busy among three cycles (19.2 ns) in each 2,500 cycles of the clock for Aurora of 156.25 MHz [15]. The results of the value and percentage of the increase of the latency are consistent with the expectation from clock compensation. As a result, the latency of the transceiver section is maximal 318 ns.

3) Total Latency: The latency of the TDC and transmission is estimated to be maximal \(179 + 318 = 497\) ns. It satisfies the requirement of less than 500 ns.

G. Transfer Efficiency

As mentioned in Sec. II-A1 in the TRG-MRG, the hit data are transferred according to the criteria that the maximal eight hit data are buffered for 64 ns in each 64 channels. A detector simulation with a simulator of passage of particle, Geant4, was performed to estimate the transfer efficiency under the expected experimental condition [16]–[18]. In the experiment, the proton-beam intensity is \(1 \times 10^{10}/\text{pulse}\) and the maximal single rate reaches 1 MHz/ch. For considering the micro structure of the beam intensity, instantaneous beam intensity distributes up to \(2 \times 10^{10}/\text{pulse}\). Figure 16 shows the hit multiplicities for 64 ns time windows under the beam intensity of \(1 \times 10^{10}/\text{pulse}\) (full line) and \(2 \times 10^{10}/\text{pulse}\) (dotted line). The fraction of discarded hits depends on the beam intensity. The beam rate dependence of the transfer efficiency is shown in Fig. 17. At the expected beam intensity of \(1 \times 10^{10}/\text{pulse}\) (5 GHz), the transfer efficiency is expected to be 99.95%. Even at the intensity of \(2 \times 10^{10}/\text{pulse}\) (10 GHz), the efficiency stays better than 98%. In conclusion, it is confirmed that he developed module meets the required performance.

H. Summary of the Performance Evaluation

At the last of this section, the result of the performance evaluation is summarized in TABLE II. All the results satisfy the requirement of the experiment.

IV. CONCLUSION

The J-PARC E16 experiment is planned in order to investigate the partial restoration of breaking of chiral symmetry at nuclear density. To handle a massive number of trigger channels of 2,620, the trigger merging module, named TRG-MRG, has been developed. The TRG-MRG consists of one
main board and two mezzanine cards and will be installed between discriminators and the trigger decision module. It works as 1 ns TDC and data multiplexer with four 6.25 Gbps transceivers. From the results of the performance tests, for example time resolution, latency, transfer efficiency, it is confirmed that the TRG-MRG achieves the requirement for the experiment which will be started in JFY 2019.

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| Point                        | Value                                  |
|------------------------------|----------------------------------------|
| Time Resolution             | <0.35 ns                               |
| INL                          | −0.041 LSB, +0.041 LSB                 |
| DNL                          | −0.022 LSB, +0.022 LSB                 |
| Minimum Pulse Width          | 100% efficiency of 1.0 ns width        |
| Double Pulse Separation      | 100% efficiency of 2.5 ns interval     |
| Latency                      | <497 ns                                |
| Transfer efficiency          | 99.95% at the expected condition       |