A portable coding strategy to exploit vectorization on combustion simulations

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Abstract

The complexity of combustion simulations demands the latest high-performance computing tools to accelerate its time-to-solution results. A current trend on HPC systems is the utilization of CPUs with SIMD or vector extensions to exploit data parallelism. Our work proposes a strategy to improve the automatic vectorization of finite-element-based scientific codes. The approach applies a parametric configuration to the data structures to help the compiler detect the block of codes that can take advantage of vector computation while maintaining the code portable. A detailed analysis of the computational impact of this methodology on the different stages of a CFD solver is studied on the PRECICINSTA burner simulation. Our parametric implementation has proven to help the compiler generate more vector instructions in the assembly operation: this results in a reduction of up to $9.39 \times$ of the total executed instruction maintaining constant the Instructions Per Cycle and the CPU frequency. The proposed strategy improves the performance of the CFD case under study up to $4.67 \times$ on the MareNostrum 4 supercomputer.

Keywords: vectorization, high performance computing, combustion simulations, performance analysis

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1. Introduction and related work

The decarbonization of the transportation sector is one of the fields with high strategic importance for our society [1, 2]. Implementing new greener fuels in real combustion systems demands advanced combustion simulations, as their physical and chemical properties are expected to be significantly different from those of conventional transportation fuels [3]. In such complex simulations, the investigation of more accurate and efficient numerical algorithms is of key importance to increase the accuracy and reduce the time-to-solution. The difficulty relies on the constant evolution of the High-Performance Computing (HPC) systems. Consequently, scientific software requires periodic updates to exploit the new features and run efficiently on those systems.

On modern CPUs, the use of vector or Single Instruction Multiple Data (SIMD) extensions is becoming more and more relevant. Beside the AVX-512 SIMD extension by Intel, we detect appearing on the market the first CPU implementing the Arm SVE extension (Fujitsu A64FX, ranked first in the Top500) and the NEC SX-Aurora vector engine, a discrete accelerator leveraging vector CPUs able to operate with registers of up to 256 double precision elements. On top of this market movements, we can not ignore the RISC-V architecture which recently ratified v1.0 of the V-extension, boosting vector computation from the academic world and the open-source community.

The efficient use of vector units within CPUs relies on auto-vectorization by the compiler and often requires to adapt or rewrite classical algorithms to exploit their full computing power [4]. Large-scale CFD codes are generally dominated by two operations: the linear solver and the matrix assembly. The first can be considered a black-box component that receives a matrix and a right-hand-side as an input and returns a solution vector [5]. The solver is composed of algebraic operations that can exploit vectorization by using specific libraries [6]. This strategy allows to port a part of large scientific codes to vector accelerators in a relatively smooth way [7]. Regarding the matrix assembly, the algorithm for unstructured meshes depends on the discretization method, where finite vol-
ume (FV) or finite elements (FE) are the most common strategies. Obtaining gains from vectorization in FV assembly requires introducing changes that have proved not practical on large-scale combustion codes [8, 9]. On the contrary, the FE assembly is constituted by matrix-like structures with the potential application of SIMD-friendly functions [10]. Our work is implemented on Alya [11], a large-scale computational mechanics code (FE-based) that is one of the thirteen Unified European Applications Benchmark Suite codes. We propose and analyze a parametric configuration to its data structure, allowing the compiler to enable auto-vectorization. We evaluate the proposed implementation on a state-of-the-art supercomputer, MareNostrum 4, powered by Intel Skylake CPUs. We show that Alya takes advantage of AVX-512 SIMD units present in the Skylake CPUs while keeping the code portable. The strategy is extensible to any other FE-based code.

The main contributions of this paper are: \(i\) we propose a parametric configuration of the data structure for a complex fluid-dynamic code; \(ii\) we measure and explain the impact of the proposed configuration from a computational point of view; \(iii\) we quantify the overall performance gain on a state-of-the-art HPC supercomputer.

The remaining part of the paper is structured as follows: Section 2 summarizes the computational fluid-dynamics problem solved with Alya; Section 3 briefly presents the technological context of the study performed in this paper, including details of the hardware and software configurations. Section 4 analyzes the optimizations applied to Alya in terms of execution time, instruction mix and cache effects to quantify the overall performance gain. Section 5 closes the paper with general remarks and conclusions.

2. Application context

2.1. Governing equations

The governing equations describing the reacting flow field in the turbulent premixed flame correspond to the low-Mach number approximation of the
Navier-Stokes equations with the energy equation represented by the total enthalpy. The combustion process is assumed to take place in the flamelet regime and the flamelet database is based on the tabulation of a laminar premixed flamelet at constant equivalence ratio that uses the chemistry from the San Diego mechanism [12]. A Favre-filtered description of the governing equations is followed to avoid modelling of terms including density fluctuations [13]. The governing equations are given by:

\[ \frac{\partial \rho}{\partial t} + \nabla \cdot (\rho \bar{u}) = 0 \]  
\[ \frac{\partial (\rho \bar{u})}{\partial t} + \nabla \cdot (\rho \bar{u} \bar{u}) = -\nabla p + \nabla \cdot \left[ \rho (\bar{v} + \nu_t) \left( 2S - \frac{2}{3} \frac{\nabla \bar{u}}{I} \right) \right] \]  
\[ \frac{\partial (\rho \bar{h})}{\partial t} + \nabla \cdot (\rho \bar{u} \bar{h}) = \nabla \cdot \left[ \rho \left( D + \nu_t P_{rt} \right) \nabla \bar{h} \right] \]

where \( \rho, t, \bar{u}, p, v, \bar{h}, D \) represent the density, time, velocity vector, pressure, kinematic viscosity, total enthalpy and thermal diffusion coefficient respectively. Heating due to viscous forces is neglected in the enthalpy equation and the unresolved heat flux is modelled using a gradient diffusion approach [14]. The formulation is closed by an appropriate expression for the subgrid-scale or eddy-viscosity \( \nu_t \) that in this study is defined by the closure proposed by Vreman [15] with a model constant of \( c_s = 0.1 \). The viscous stress tensor is defined based on Stokes' assumption and the turbulence contribution is determined by the use of the Boussinesq approximation [13], in which \( S = \frac{1}{2} \left[ \nabla \bar{u} + (\nabla \bar{u})^T \right] \) and \( I \) are the strain and the identity tensor respectively. A unity Lewis number assumption has been made to simplify the multicomponent transport in the governing equations. Turbulent Schmidt and Prandtl numbers are both set constant with value of 0.7.

For the present combustion model, a controlling variable based on a reactive scalar is used to couple the chemical states with the fluid flow. This controlling variable can be understood as a progress variable \( Y_c \) that is used to describe the thermochemical state from an unreacted mixture to a fully reacted mixture.
For numerical reasons [16], a scaled progress variable $c$ is defined as:

$$c = \frac{Y_c - Y_c^0}{Y_c^eq - Y_c^0}$$  \hspace{1cm} (4)$$

where $Y_c^0$ and $Y_c^eq$ are the values of the progress variable of the unreacted mixture and at equilibrium conditions respectively. Considering the application of this flamelet combustion model to premixed combustion in LES, the subscale effects need to be addressed. The tabulated properties $\psi$ are integrated with a presumed-shape probability density function (PDF) that is constructed from the filtered progress variable $\tilde{c}$ and the subgrid variance $\tilde{c}^2 = \overline{c^2} - \overline{c^2}$ using a $\beta$-function [16]. A closure for the subgrid scale variance is provided by the solution of the transport of $\tilde{c}^2$ following Domingo et al. (2005) [16].

The chemical state of the perfectly premixed flame in the LES framework is ultimately described by the two controlling variables: $\overline{c}$ and $\overline{c^2}$, so the governing equations describing the chemical evolution of the flame are given by:

$$\frac{\partial (\rho \tilde{c})}{\partial t} + \nabla \cdot (\rho \tilde{u} \tilde{c}) = \nabla \cdot \left[ \rho \left( \frac{D}{Sc_t} + \frac{\nu_t}{Sc_t} \right) \nabla \tilde{c} \right] + \tilde{\omega}_c$$  \hspace{1cm} (5)$$

$$\frac{\partial (\rho \tilde{c}^2)}{\partial t} + \nabla \cdot (\rho \tilde{u} \tilde{c}^2) = \nabla \cdot \left[ \rho \left( \frac{\tilde{D}}{Sc_t} + \frac{\nu_t}{Sc_t} \right) \nabla \tilde{c}^2 \right] + 2\rho \tilde{D} |\nabla \tilde{c}|^2$$  \hspace{1cm} (6)$$

$$+ 2 \left( \overline{\tilde{c} \tilde{\omega}_c} - \overline{\tilde{c}_c} \tilde{\omega}_c \right)$$  \hspace{1cm} (7)$$

$$2 \rho \tilde{\omega}_c$$  \hspace{1cm} (8)$$

where $\tilde{\chi}_c$ represents the scalar dissipation rate and $\tilde{\omega}_c$ is the filtered source term of the progress variable. The scalar dissipation rate is composed by the resolved and unresolved parts, which are given by:

$$\tilde{\chi}_c = 2 \tilde{D} |\nabla \tilde{c}|^2 + \chi_c^{gs} = 2 \tilde{D} |\nabla \tilde{c}|^2 + \frac{C_d}{\tau_t} \tilde{c}^2$$  \hspace{1cm} (9)$$

where $\tau_t$ is a turbulent time scale, which is obtained following Ventosa et al. [17].
2.2. About Alya

The governing equations (1), (2), (3), (5), and (6) are solved by means of a low-dissipation finite-element method implemented into the code Alya [18]. The code Alya has been used to resolve turbulent reacting flows in premixed and partially premixed conditions [19, 20, 21, 22]. The use case uses a perfectly premixed model with presumed-shape PDF to account for turbulent-chemistry interactions. The convective term is discretized using an extension to variable density flows of the scheme recently proposed by Charnyi et al. [23], which conserves linear/angular momentum and kinetic energy at the discrete level. Second-order spatial discretizations are used. In order to use equal-order elements, numerical dissipation is introduced only for the pressure stabilization via a fractional step scheme [24]. The set of equations is integrated in time using a third-order Runge-Kutta explicit method combined with an eigenvalue-based time-step estimator [25]. This approach has been shown to be significantly less dissipative than traditional stabilized FEM approach [26]. Scalar equations are solved by a third-order explicit Runge-Kutta scheme combined with the ASGS stabilization method [22].

Alya is a modular scientific code in which each module handles a set of equations. The momentum equations are solved by the nastin module that applies the fractional step method. The algorithm consists of two procedures: the application of the third-order Runge-Kutta for the discretization of the convection-diffusion equation and the solution of the Poisson equation that imposes the mass conservation constraint. The Runge-Kutta is an iterative method that assembles the laplacian matrix and a right-hand side that forms the Poisson system. This linear system is solved utilizing an iterative Krylov method. The temper module is responsible for calculating the contribution of the energy equation, and the chemic module manages the chemical transport equations. All modules define a unique thermo-chemical state of the simulated gas flow. These modules are based on an explicit scheme that assembles the arrays related to thermal conductivity, viscosity, and variable density. Latter creates a strong coupling between nastin and the other modules, since the temporal
derivative of density appears as a source term in the continuity equation used in the fractional step method. A general view of the Alya’s workflow is shown in Figure 1. The simulation of combustion phenomena requires of millions of time integration steps to attain meaningful results. The operations within the time-integration step become the dominant ones.

![Figure 1: Workflow of Alya for a combustion simulation.](image)

The assembly procedure is present in all the modules since it is an essential part of the finite element method. The assembly is applied on each element locally, not requiring MPI communications. The primary operations within the time integration step are the element assembly and the algebraic solver. Table 1 summarizes the relative weight of the assembly within the time-integration step for a combustion simulation using the flamelet model.

The number of iterations in the element assembly depends on two variables: the number of gauss points (\(n_{gauss}\)) and the number of integration nodes (\(n_{nodes}\)). The values of \(n_{gauss}\) and \(n_{nodes}\) varies according to the shape of the element (cell of the mesh) and the discretization order. Using a first-order discretization on linear elements produces an equal number of integration nodes and gauss points. For instance, in tetrahedrons, prisms, and hexahedrons, the
Table 1: Relative weight of the main operations within the time integration step

| Module               | Nastin | Temper | Chemic | Total  |
|----------------------|--------|--------|--------|--------|
| Element Assembly     | 43.14% | 12.66% | 39.57% | 95.37% |
| Algebraic Solver     | 4.47%  | -      | -      | 4.47%  |
| Others               | 0.04%  | 0.03%  | 0.09%  | 0.16%  |
| Total                | 47.65% | 12.69% | 39.66% | 100%   |

number of integration points is four, six, and eight, respectively.

The elemental matrix (Ae) is calculated using the shape functions (N) and the Jacobian element matrix (Jac). The traditional approach consists of assembling one after the other as shown in Algorithm 1. The number of integration nodes and gauss points might vary from one element to another, thus preventing the automatic vectorization by the compiler of the inner loop. At the end of the assembly phase, a reduction along the gauss points calculates the contribution of each element.

\[
\text{do } ig = 1, ngauss \\
\text{do } jn = 1, nnodes \\
\quad \text{do } in = 1, nnodes \\
\quad \quad \text{Ae}(in,jn) = \text{Ae}(in,jn) + \text{Jac}(ig) \ast N(in,ig) \ast N(jn,ig) \\
\text{end do} \\
\text{end do} \\
\text{end do}
\]

Algorithm 1: Element assembly

2.3. Implementation details

One of the most important constraints when developing a scientific code adopted by a large community is that the code must be understandable, easy to maintain, and portable. One way to comply with these requirements is to limit
(and if possible avoid) compiler-specific and architecture-specific implementa-
tions. Ideally one would like to squeeze the maximum performance avoiding
coding styles that over-specialize the implementation of the scientific applica-
tion. In the case of data parallelism, the hope is that the compiler detects the
vectorizable zones (e.g., loops) without the need of using specific SIMD code /
assembly. The software design approach presented in Algorithm 1 fails to un-
lock the potential vectorization and data reuse that exists within the assembly
algorithm. To leverage the performance boost delivered by SIMD / vector units
of modern CPUs, the following set of preprocessing functions are proposed:

- **Grouping**: The elements are organized in groups. Each group contains
elements with the same geometrical form. Then, the elemental assembly
within a group has the same number of gauss points and integration points.
This reorganization creates a regularity in the operations performed within
elements of the same group. The goal is to unlock the potential vector
operations.

- **Renumbering**: The elements within a group are renumbered using a
Cuthill-Mkee algorithm. The idea is to minimize the cache misses by
reducing the bandwidth of the connectivity matrix.

- **Packing**: Each group is divided into packs of VECTOR_SIZE elements.
The definition of the VECTOR_SIZE takes place at compilation time. The
elemental multi-dimensional arrays involved in the assembly operation in-
corporate a new dimension of size VECTOR_SIZE. In Fortran, the extra
dimension is added at the first position of the arrays since the memory
distribution follows a column-major order. The idea is to perform the
assembly operations to all the elements of a pack at once. The column-
major order and the extra dimension help the compiler to generate vector
operations.

- **Padding zeros**: If the number of elements within a group is not divisible
by the VECTOR_SIZE, zeros are padded in the elemental arrays to maintain
the regularity of the pack.

In our case, the proposed functions have been integrated into Alya. The implementation of those depends heavily on the specific scientific code: parallelization strategy, internal data structures, and programming language. The preprocessing functions are called only once at the beginning of the simulation. An Alya execution consists of thousands or millions of iterations, making the cost of the preprocessing stage negligible; therefore, these functions are not further studied in this manuscript.

Additionally, a data structure stores the relevant information of each group, i.e., number of gauss points, integration points, and element ids. Such data structure works as an index that allows jumping between packs, gathering the global data, and scattering the outcome results. For instance, the assembly operation using \texttt{VECTOR\_SIZE} is shown at Algorithm 2. Using the subscript-triplet notation of Fortran (1:\texttt{VECTOR\_SIZE}) provides extra information to the compiler for unlocking the vectorization. Note that performing the operations in packs also exposes the temporal locality of the reusable arrays as the shape functions. Moreover, using \texttt{VECTOR\_SIZE=1} is equivalent to the original code in terms of memory accesses and performance. Our study focuses on the impact of this parametric variable on enabling the SIMD instructions and improving memory accesses.

do ig = 1,ngauss
    do jn = 1,nnodes
        do in = 1,nnodes
            \texttt{Ae(1:VECTOR\_SIZE,in,jn) = Ae(1:VECTOR\_SIZE,in,jn) + Jac(1:
            VECTOR\_SIZE,ig) * N(in,ig) * N(jn,ig)}
        end do
    end do
end do

Algorithm 2: Matrix element assembly using \texttt{VECTOR\_SIZE}
2.4. Application context: The PRECCINSTA burner

The use case is a premixed swirl-stabilized flame of a gas turbine model combustor, also known as the PRECCINSTA burner [27]. This is a traditional benchmark for combustion simulations that permits to evaluate the main operations involved in production runs. Alya is set up to run a large-eddy simulation using the flamelet method for calculating the tabulated chemical transport. The burner operates at atmospheric pressure and ambient temperature with an equivalence ratio of $\phi = 0.67$. The domain discretization consists of an unstructured mesh of 16 million elements with different shapes: tetrahedrons, pentahedrons, and pyramids. Most of the elements are tetrahedrons (76.4%), followed by pentahedrons (23.5%), while the rest are pyramids (0.1%) used to smooth the transition between the other two. After the preprocessing stage, twenty-six elements with empty entries are padded to maintain regularity for a $\text{VECTOR\_SIZE}=32$; this amount of padded elements is insignificant compared to the 16 million element mesh. The loop size in Algorithm 2 takes a different number of gauss points depending on the element shape. The tetrahedrons, pyramids, and pentahedrons require four, five, and six gauss points, respectively. Sample results of the Large Eddy Simulation (LES) fields are shown in Figure 2 for the axial velocity, temperature, and hydroxyl (OH) radical. Details of the analysis and validation of this case can be found in Govert et al. [20], and Both et al. [22].

3. Technological context

In this section we describe the hardware and software as well as the methodology and metrics that we employ in our study.

3.1. Environment

MareNostrum 4 is the flagship supercomputer at the Barcelona Supercomputing Center. Table 2 summarizes the hardware characteristics of MareNostrum 4. The cluster is composed of 3456 compute nodes. Each node houses...
Figure 2: Instantaneous contour plots of the LES results of the PRECCINSTA burner. Left: axial velocity, middle: temperature, right: hydroxyl radical mass fraction.

two Intel Xeon Platinum 8160 CPU with 24 cores running at 2.10 GHz. The CPUs implement the Intel x86 Skylake microarchitecture and support SIMD instructions SSE, AVX, and AVX-512 which operate with registers of 128, 256, and 512 bits respectively. For example, the AVX-512 registers can hold up to eight double precision floating point elements.

The approach we present in this paper is portable because it is independent from the architecture and the compiler. However, as we rely on the auto-vectorization capabilities of the compiler, the performance results can depend on the compiler used. We compiled Alya with three different compilers based on software availability, and having vendor specific compilers (Intel) and generic ones (GNU). For both compilers we used the flags suggested by the application developers and the support team of the cluster on which we were running.

When compiling binaries with the Intel Compiler, we used the optimization flags `-xCORE-AVX512 -mtune=skylake`; whereas when compiling with the GNU compiler we used the flags `-O3 -march=skylake-avx512 -ffp-contract=fast -ffast-math`. In addition to the optimization flags, the `-DVECTOR_SIZE=<x>` defines, at compile time, the element packing as explained in Subsection 2.3.
Table 2: Hardware configuration of MareNostrum 4

| System integrator | Lenovo  
|-------------------|---------|
| Core architecture | Intel x86 |
| SIMD extensions   | SSE, AVX, AVX-512 |
| CPU name          | Skylake Platinum |
| Frequency [GHz]   | 2.10 |
| Sockets/node      | 2 |
| Core/node         | 48 |
| L1 cache size     | 64 kB |
| L2 cache size     | 256 kB |
| L3 cache size     | 33 MB |
| Memory/node [GB]  | 96 |
| Memory tech.      | DDR4-2666 |
| Memory channels   | 6 per socket |
| Peak memory bandwidth [GB/s] | 256 GB/s |
| Number of nodes   | 3456 |
| Interconnection   | Intel OmniPath |
| Peak network bandwidth [GB/s] | 12.00 |
Where the value of $\langle x \rangle$ is $\{1, 2, 4, 8, 16, 32, 64, 128, 256, 512\}$. As the parallel MPI performance is not part of the study, we use the same MPI library (i.e., Intel MPI 2018.4) for all runs.

3.2. Methodology

All experiments and results shown in this paper are obtained using a single node of the MareNostrum 4 cluster (48 cores) and launching 48 MPI ranks. For this study, we follow a top-down approach, from more general metrics to more detailed ones. The goal is to understand the inherent behaviour of the different executions we are comparing. We leveraged the hardware counters in MareNostrum 4 to gather information during the execution of Alya. To read these hardware counters we use PAPI [28, 29] combined with Extrae [30]. Table 3 lists the counters we included in our study and a brief description of the events that they measure. We instrumented the code to trigger an Extrae event that measures the hardware counters at the start and the end of each phase in a time-integration step.

When reading hardware counters, we run Alya with five time-integration steps per execution. For each execution, we gathered the hardware counters information when the processes are performing useful computation (i.e., not during MPI calls).

![Example of trace obtained to measure hardware counters showing the different phases](image)

Figure 3: Example of trace obtained to measure hardware counters showing the different phases

In Figure 3, we show an example of a trace obtained to measure the different
Table 3: List of hardware counters

| Name                                                  | Description                                                                 |
|-------------------------------------------------------|-----------------------------------------------------------------------------|
| UNHALTED_REFERENCE_CYCLES                             | CPU cycles                                                                  |
| INST_RETIRED                                          | Total number of executed instructions                                       |
| FP_ARITH:SCALAR_DOUBLE                                | Scalar floating point arithmetic instructions                              |
| FP_ARITH:128B_PACKED_DOUBLE                           | 128-bit SIMD floating point arithmetic instructions                         |
| FP_ARITH:256B_PACKED_DOUBLE                           | 256-bit SIMD floating point arithmetic instructions                         |
| FP_ARITH:512B_PACKED_DOUBLE                           | 512-bit SIMD floating point arithmetic instructions                         |
| BRANCH INSTRUCTIONS_RETIRED                           | Branch instructions                                                         |
| MEM_UOPS_RETIRED:ALL_LOADS                            | Load micro-operations                                                       |
| MEM_UOPS_RETIRED:ALL_STORES                           | Store micro-operations                                                      |
| MEM_LOAD_UOPS_RETIRED:L1_HIT                          | L1 cache hits produced by load operations                                   |
| MEM_LOAD_UOPS_RETIRED:L1_MISS                          | L1 cache misses produced by load operations                                  |
| MEM_LOAD_UOPS_RETIRED:L2_HIT                          | L2 cache hits produced by load operations                                   |
| MEM_LOAD_UOPS_RETIRED:L2_MISS                          | L2 cache misses produced by load operations                                  |
| MEM_LOAD_UOPS_RETIRED:L3_HIT                          | L3 cache hits produced by load operations                                   |
| MEM_LOAD_UOPS_RETIRED:L3_MISS                          | L3 cache misses produced by load operations                                  |
hardware counters. On the $x$-axis we represent the time, and in the $y$-axis the different MPI processes. The color shows the event added with Extrae to delimit the FE assembly of the different modules. If we compare it with the workflow shown in Figure 1 we can easily identify the different phases: Preprocess, 5 time-integration steps and postprocess.

Figure 4: Example of trace obtained to measure hardware counters showing 1 time step

In Figure 4, we zoom-in focusing on one time-integration step of the same trace. For each module execution, there are three FE assembly calls due to the third-order Runge-Kutta used in the explicit formulation of Alya (see Section 2.2). The remainder corresponds to the algebraic solver that is called only once per time-integration step. We aggregate the values of the hardware counters obtained in all the regions with the same color. This means that the measurements reported in Subsection 4.3 and Subsection 4.4 represent the sum of all the events recorded by a given hardware counter across all processes in a given phase (i.e., in a region with the same color).

4. Performance analysis

In this section we study the performance impact of the coding changes explained in Section 2.3 in the environment and using the methodology explained in Section 3.1. The study is guided by the \textit{computing performance equation} where the execution time $t$ of a program is computed as:

\[ t = \frac{I}{C + f} \]  \hspace{1cm} (10)
where ‘C’ stands for *Instructions Per Cycle* and measures the efficiency of the processor in terms of how many instructions can be processed in one clock cycle. $I$ is the total number of instructions executed and $f$ the frequency at which the processor is working.

The remaining part of this section analyses each of the operands of the *computing performance equation* expressed in Equation 10: first we measure the elapsed time and then we study $f$ (the frequency), $I$ (the number and the types of instructions involved in the computation), and ‘C’ (the IPC which we demonstrate is correlated with the cache reuse).

### 4.1. Elapsed Time analysis

For the elapsed time analysis we use the elapsed time per phase, each value reported in this section is an average of 5 time steps. Alya follows an iterative pattern were each iteration performs the same computation. We verified that the variations of our measurements do not exceed 3\%. 5 time steps is a tradeoff between statistical significance, execution time of the tests and size of the traces collected.

In Figure 5 we show three plots corresponding to the three phases that we are studying, top to bottom: Nastin, Temper and Chemic. In the $y$-axis we can see the average elapsed time in a given phase and in the $x$-axis the value used for the `VECTOR_SIZE`, each line corresponds to a different compiler.

Measurements of the master process (rank zero) are discarded. Thus, each point in Figure 5 represents the elapsed time averaged across 47 processes, five time steps, and three assembly steps.

In Figure 5 we observe that in all phases the GNU compiler obtains a worse performance than the different versions of the Intel compiler, this difference is more important for the Temper and Chemic phases than for Nastin. Also, for Temper and Chemic the difference is more important for low values of the `VECTOR_SIZE`.

Comparing the different versions of the Intel compiler we also see a difference in performance. For `VECTOR_SIZE` values below 16 Intel 2020 generates a code
Figure 5: Elapsed time per phase and time step varying the vector size with different compilers
that performs better than the code generated with the 2018 version.

Increasing the `VECTOR_SIZE` up to a value of 32 reduces the elapsed time for all compilers. When using values of `VECTOR_SIZE` greater than 32 there is a slight degradation of the performance for all the phases and all the compilers. However, the performance degradation is more important for the Nastin assembly. To better explain these results, we look in more details at the hardware counters.

### 4.2. Cycles and Frequency

In this subsection we analyze the data obtained with the hardware counter `UNHALTED_REFERENCE_CYCLES`, that counts the total number of clock cycles. With this hardware counter we compute two metrics, the first one the total number of cycles used in a phase to do useful work, $C_{\text{tot}}$, and the second one the number of cycles per $\mu$s. The cycles per $\mu$s can also be expressed as the measured frequency, $F$, and is computed as: $F = C_{\text{tot}} / T_{\text{tot}}$, where $T_{\text{tot}}$ is the total time spent in a phase while performing useful work.

In Figure 6 we show the number of cycles used to compute each phase in the $y$-axis. In the $x$-axis we see the different values of the `VECTOR_SIZE`. With a constant frequency and knowing that there is no communication during the measured time, the results in this plot should express the same trend as the one of the elapsed time depicted in Figure 5.

In Figure 7 we show the frequency ($y$-axis) for the different executions and phases while changing the `VECTOR_SIZE` ($x$-axis). We can verify that there are no major changes in the frequency when varying the `VECTOR_SIZE`, the phase nor the compiler.

It important to note that the operational frequency of the CPUs of MareNostrum 4 is set to 2.1 GHz, Dynamic Voltage and Frequency Scaling (DVFS) is disabled and we verified that there is no throttling of the frequency due to thermal protection (even when enabling AVX-512).

From this part of the study we can conclude that the differences that we observe in the elapsed time in Section 4.1 are not explained by a variation in
Figure 6: Cycles used to compute each phase varying the vector size with different compilers
Figure 7: Frequency measured in each phase varying the vector size with different compilers
4.3. Instruction mix analysis

The next factor that can affect the execution time is the number of instructions. In this section, we analyze the total number and the type of instructions executed. The goal is to understand how the VECTOR_SIZE affects the instruction mix generated by the compilers and the overall performance. In Figure 8, we show the total number of instructions executed in each phase. The x-axis represents the different values of the VECTOR_SIZE, and each series corresponds to the total number of instructions of different compilers (y-axis). We observe that the number of instructions executed when using the GNU compiler is much higher than when using either of the Intel compiler versions. This difference is more notable in the Temper and Chemic phases than in the Nastin one. This observation can explain the results shown in subsection 4.1 when measuring the elapsed time (Figure 5).

We can see that for some values of VECTOR_SIZE (1 for Nastin, 1, 2, 4 for Chemic and Temper), the number of instructions executed by the code compiled with Intel 2020 is higher than the instructions used when compiled with Intel 2018. This also partially explains the difference in time obtained by the two compilers, as the difference between the two compilers was observed for all the phases and all the VECTOR_SIZE below 8.

For all phases and all compilers, the total number of instructions executed decreases while we increase the VECTOR_SIZE up to 32. For values of VECTOR_SIZE greater than 32 there is no impact in the number of instructions and they keep stable when increasing the VECTOR_SIZE.

To understand the cause of the difference in the amount of instruction in each case, we look at the types of instructions executed. With the available hardware counters in the cluster, we can group the instructions in memory accesses (loads and stores), branches, and floating-point instructions. Within floating-point instructions we distinguish among instructions operating scalar and vector operands. Thus, we keep track of floating-point scalar, floating-point
Figure 8: Number of instructions executed in each phase varying the vector size with different compilers
Figure 9: Absolute Instruction Mix for different phases and compilers
128 bits (SSE), floating-point 256 bits (AVX), and floating-point 512 bits (AVX-512). We plot this data in two ways: absolute values where the height of the column is equivalent to the total number of instructions (Figure 9) and relative where all the bars have the same height (Figure 10). Each class of instruction is represented by a color: green for memory accesses, blue for branches and red for floating-point.

In Figure 9, we show the different plots with the absolute number of instructions of each type, each column of plots corresponds to one compiler, and each row of plots corresponds to one phase. To ease the comparison of phases with different compilers, the plots in the same row share the same scale in the $y$-axis. In the $x$-axis of each plot we can see the different values of $\text{VECTOR\_SIZE}$.

When comparing the number of instructions executed using the different compilers, we can see that the GNU compiler inserts between $3\times$ and $5\times$ more branch instructions, between $1.5\times$ and $4\times$ more store instructions, and between $1.5\times$ and $3.4\times$ more load instructions. For $\text{VECTOR\_SIZE}=1$, there is not a very relevant difference in the floating-point instructions: the only observation is that the Intel compiler emits AVX-512 instructions while GNU only generates SSE instructions. For $\text{VECTOR\_SIZE}=2$, GNU is able to vectorize more than the Intel compiler but it is not enough to overcome the more branch, load, and store instructions executed.

In Nastin, when increasing the $\text{VECTOR\_SIZE}$ from 2 to 4 with the Intel compilers, the number of load, store, and branch instructions are divided by 2. This drastic reduction is not present when increasing $\text{VECTOR\_SIZE}$ from 4 to 8, but happens again when increasing from 8 to 16. As expected, each time that the compiler is able to take advantage of the SIMD units, the absolute number of scalar floating-point instructions executed decreases and also the number of memory accesses and branches decreases proportionally. This explains the instruction reduction when increasing the value of $\text{VECTOR\_SIZE}$ from 2 to 4 and from 8 to 16.

For Temper and Chemic the reduction in the number of load, store, and branch instructions is progressive from $\text{VECTOR\_SIZE}$ 2 to 16.
In Figure 10, we plot the same data relative to the total number of instructions executed. In this view, we highlight the differences in the instruction mixes of all cases. As we increase $\text{VECTOR\_SIZE}$ from 1 to 16, we see that the Intel compilers can make use of floating-point vectors of 128 (SSE), 256 (AVX), and 512 bits (AVX-512), respectively. With $\text{VECTOR\_SIZE}$ 16, almost all floating-point operations are vectorized using AVX-512 instructions, i.e., FP 512 bits. The GNU compiler behaves similarly but it is only able to generate AVX instruction (FP 256 bit), hence using half of the vector length compared to the Intel compilers.

From the data shown in this section, we conclude that the difference in performance between the code generated by the GNU and Intel compilers is mainly due to the capacity of the compiler of taking advantage of the CPU vector extension: we notice in fact that the code transformations in Alya allow to generate floating-point instructions using a vector length of 128 bits (using SSE), 256 bits (using AVX), and 512 bits (using AVX-512). This results in a proportional reduction of memory accesses (load and stores) and branch instructions.

The reduction of the number of instructions also explains the performance
improvement achieved when increasing the VECTOR\_SIZE by all compilers in all phases. In the Intel compilers, the maximum vectorization is achieved with VECTOR\_SIZE 16. For higher values, there is no change in the number of vector instructions. For the GNU compiler, the maximum vectorization is attained with VECTOR\_SIZE 32. The performance degradation observed when increasing the VECTOR\_SIZE beyond 32 cannot be explained by the number of instructions nor the instruction mix shown in this section.

4.4. IPC and cache reuse analysis

In this section, we study $C$ that is the third factor of the performance equation 10, how it changes, how it affects the performance and the causes of its change.

Figure 11 shows $C$ that we call “Instructions Per Cycle” (IPC) on the y-axis and the VECTOR\_SIZE in the x-axis. Each compiler is represented with a different color.

We observe that in the Temper and Chemic phases for VECTOR\_SIZE below 8, the GNU compiler obtains less IPC than the Intel compilers. This means that the performance degradation that we see in Section 4.1 is explained not only by a higher number of instructions as seen in Section 4.3 but also by a worse IPC. For VECTOR\_SIZE above 8 in Nastin and Chemic the GNU compiler obtains a higher IPC than Intel compilers, while in Chemic, this behaviour appears for VECTOR\_SIZE greater than 64.

The difference between the two Intel compilers that is not explained by the number of instructions in Section 4.3 is explained here. In Nastin Intel 2018 obtains, in fact, a higher IPC than Intel 2020.

In general, increasing the VECTOR\_SIZE decreases the IPC. The pattern is slightly different for Nastin, where the best IPC is obtained with VECTOR\_SIZE 2, while in Temper and Chemic VECTOR\_SIZE 1 and 2 show the same IPC. Increasing the VECTOR\_SIZE above 16 decreases the IPC for all compilers and phases.
Figure 11: IPC obtained in each phase varying the vector size with different compilers
To understand the IPC changes observed, we look at the misses in the different levels of cache. Figure 12 shows the number of misses issued by the first level cache (L1) for every 1000 instructions.

![Graphs showing L1 misses per thousand instructions in different phases with varying vector sizes and compilers.]

Comparing the compilers, we observe that the code generated by the GNU compiler obtains fewer L1 misses in all cases. This can be an effect of the GNU compiler executing more instructions than the Intel compilers. The two Intel compilers present a very similar miss ratio in L1.

In general, we observe that for VECTOR_SIZE below 8, there is no relevant variations in the number of L1 misses. On the other hand, for VECTOR_SIZE above 32, we notice an increment of the number of misses in L1. The changes
In Figure 13, we can see the analogous chart corresponding to the number of petitions missed in the second level of cache (L2) for every million instructions. The conclusions are very similar to the ones obtained looking at the L1 misses. The GNU compiler generates less L2 misses per million of instructions but this metric can be affected by the fact that GNU generates more instructions than the other compilers. The two Intel compilers show an equivalent number of L2 misses.

For values of VECTOR_SIZE below 8, the number of L2 misses is very low and...
does not change when changing the value of \texttt{VECTOR\_SIZE}. When increasing the \texttt{VECTOR\_SIZE}, we can see an increment in the number of L2 misses. The main difference with the previous chart (L1 misses per thousand instructions, Figure 12) is that the drastic increase starts with a \texttt{VECTOR\_SIZE} above 128. This can indicate that some of the data structures are increasing in size as we increase the \texttt{VECTOR\_SIZE} and do not fit in the caches. This effect can be seen because L1 is saturated first as is smaller and L2 latter.

Finally, we look at the number of misses of the last cache level (L3). We plot them in Figure 14, where the y-axis is the total number of misses in L3.

Figure 14: L3 misses per million instructions in each phase varying the vector size with different compilers
per million instructions executed. In this case, we can see a different behavior in the different phases. For Nastin, there is not an important difference in the number of L3 misses for VECTOR_SIZE below 256 but we see a dramatic increase with VECTOR_SIZE 512. This effect follows our previous assumption that some data structure is growing as we increase the VECTOR_SIZE and fills the different caches as we increase the VECTOR_SIZE.

In Temper and Chemic, the L3 miss ratio is relatively stable up to VECTOR_SIZE 8. For values of VECTOR_SIZE between 8 and 64 or 128, the L3 miss ratio increases. Then, the L3 miss ratio decreases as we increase the VECTOR_SIZE, and finally, for VECTOR_SIZE 512, it reaches its maximum value. With the current information, we cannot explain this effect. However, we can see that this effect is not reflected in the IPC, meaning that the increase in L1 and L2 misses have more impact than the L3 ones in this case.

Analyzing the IPC, we have seen that the better performance observed by the Intel compilers with respect to the GNU one is also explained by the better IPC achieved by the Intel compilers for VECTOR_SIZE below 8. When looking into the miss ratio of the different caches, we see that the worse IPC of the GNU compiler is not because of a higher miss ratio. Therefore, based on the observations in Section 4.3 about the instruction mix, we can assume that the IPC of the GNU compiler is affected by the higher number of branch instructions.

For VECTOR_SIZE above 16, the GNU compiler obtains better IPC than the Intel compilers. This is not explained by the miss ratio of the different levels of cache, so we conclude that it is the effect of the high number of vector instructions executed by the Intel versions. However, it is important to note that the Intel compilers attain better performance than the GNU compiler in the overall analysis.

Regarding the impact of VECTOR_SIZE, we conclude that the performance degradation observed for VECTOR_SIZE greater than 32, which could not be explained in the previous sections, is explained by the decrement of IPC. Also, the IPC decrement is explained by the increasing miss ratio in the different levels of cache as we rise the value of VECTOR_SIZE.
4.5. Overall performance

In this section, we evaluate how the proposed changes to the combustion code affect the overall execution. All results shown in this section are the elapsed time of 10 time integration steps.

Figure 15: Elapsed time for 10 time integration steps varying the vector size with different compilers

In Figure 15, the $y$-axis represents the elapsed time to execute 10 time integration steps of Alya, while the $x$-axis shows the different values used for the VECTOR_SIZE. We can conclude that the best VECTOR_SIZE for the overall execution is 32 for the GNU compiler, while it is around the values of 16, 32, and 64 (within a margin of 5%) for the Intel compilers. In this plot, we observe that the code generated by the GNU compiler is $1.5\times$ slower than the one generated by the Intel compilers in the best case (with VECTOR_SIZE 32). Also, the two Intel compilers have similar performance, except for VECTOR_SIZE 1 and 2, where Intel 2018 outperforms Intel 2020.

In Figure 16, we show the speedup of the execution of 10 time integration steps of Alya achieved by increasing the VECTOR_SIZE with respect to the time spent with VECTOR_SIZE of 1. Notice that each compiler uses its own reference for the computation of the speedup. Compared with VECTOR_SIZE 1, we observe that the best VECTOR_SIZE achieves a speedup of $4.7\times$ with Intel 2020, and $3.9\times$ with Intel 2018 and GNU compilers. Both Intel 2018 and GNU (the best and worse compilers) obtain the same speedup relative to their base case with
Figure 16: Speedup when increasing VECTOR_SIZE with different compilers

VECTOR_SIZE 1. This is interesting especially in view of our observations in Section 4.3 were we show that the GNU compiler is only able to generate AVX instructions (256 bits) while the Intel compiler takes full advantage of the AVX-512 SIMD extension (512 bits).

5. Conclusions

The efficient exploitation of SIMD/vector units is often enforced using non-portable methods: e.g., vendors provide optimized libraries that are often tight to the underlying hardware or application developers code part of their code using calls to intrinsics directives. While both approaches are valid for performance validations on benchmarks or relatively small codes, these approaches could be counterproductive on complex codes with a large community of users and developers that requires to be executed on different HPC clusters (e.g., powered by different architectures). This paper presented a portable method for enabling vectorization within a complex multi-physics code, Alya. We studied the benefits and limitations of our implementation.

Studying the dynamic instruction mix with the help of hardware counters, we have been able to show that i) indeed, our implementation favor vector computation and different compilers are able to exploit it with different degrees of efficiencies; ii) pushing to the extreme our implementation proposal (i.e., increasing the values of VECTOR_SIZE) affects the data layout in memory,
hindering the benefits of data locality in the caches.

The portability of our solution opens the doors to move our code to HPC clusters with different CPU generations or even different architecture, without the need of tuning the code for a new SIMD/vector extension. While the portability of our solution is a precious added value, we recognize that its efficiency is inherently tight to the ability of the compilers to auto-vectorize our code. Anyhow, in our study, we show that both compilers, two vendor-specific and the GNU suite, are mature enough on the x86 architecture to enable a high degree of data parallelism using the SIMD units.

Our implementation has been finally evaluated and quantified, showing an overall speed-up respect to the original code ranging from $3.38 \times$ up to $4.67 \times$ depending on the compiler.

6. Discussion and Future work

The portable coding strategy described in the manuscript enables the vectorization independently of the initial conditions of the simulation. The geometry of the elements can negatively affect the performance when dealing with polyhedrons with many faces. Our work was oriented to the more common shapes found in simulations using unstructured grids (tetrahedrons, pentahedrons, and pyramids). Our strategy of adding an extra dimension causes an increase in the memory footprint that could reduce the vectorization benefits when dealing with more complex shapes. A future line of work in this direction could be to parametrize and estimate the performance based on the computer architecture and the element shape. Another future work is finding a way to reutilize the SIMD-friendly data structures to exploit GPU devices. A detailed performance analysis would be needed to estimate the achievable performance by following this methodology.
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