FPGAs excel in low power and high throughput computations, but they are challenging to program. Traditionally, developers rely on hardware description languages like Verilog or VHDL to specify the hardware behavior at the register-transfer level. High-Level Synthesis (HLS) raises the level of abstraction, but still requires FPGA design knowledge. Programmers usually write pragma-annotated C/C++ programs to define the hardware architecture of an application. However, each hardware vendor extends its own C dialect using its own vendor-specific set of pragmas. This prevents portability across different vendors. Furthermore, pragmas are not first-class citizens in the language. This makes it hard to use them in a modular way or design proper abstractions.

In this paper, we present AnyHLS, a library to synthesize FPGA designs in a modular and abstract way. AnyHLS resorts to standard programming language features such as types and higher-order functions to accomplish this as follows: First, partial evaluation specializes and optimizes the user application based on a library of abstractions. Ultimately, the backend of AnyHLS generates vendor-specific HLS code for Intel and Xilinx FPGAs. To validate the effectiveness of our approach, we implemented an image processing library on top of AnyHLS. We show that this library’s performance is on par with or exceeds the one achieved with existing full-blown domain-specific compilers.

1 INTRODUCTION

Field Programmable Gate Arrays (FPGAs) consist of a network of reconfigurable digital logic cells that can be configured to implement any combinatorial logic or sequential circuits. This allows the design of custom application-tailored hardware. In particular memory-intensive applications benefit from FPGA implementations by exploiting fast on-chip memory for high throughput. These features make FPGA implementations orders of magnitude faster/more energy-efficient than CPU implementations in these areas. However, FPGA programming poses challenges to programmers unacquainted with hardware design.

FPGAs are traditionally programmed at Register-Transfer Level (RTL). This requires to model digital signals, their timing, flow between registers, as well as the operations performed on them. Hardware Description Languages (HDLs) such as Verilog or VHDL allow for the explicit description of arbitrary circuits but require significant coding effort and verification time. This makes design iterations time-consuming and error-prone, even for experts: The code needs to be rewritten for different performance or area objectives.

High-Level Synthesis (HLS) [7] increases the abstraction level to an untimed high-level specification similar to imperative programming languages and automatically solves low-level design issues such as clock-level timing, register allocation, and structural pipelining. HLS languages such as Vivado HLS or Catapult-C are usually based on various C dialects [28]. However, an HLS code that is optimized for synthesis of high-performance circuits is fundamentally different from a software program delivering high performance on a CPU. This is due to the significant gap between the programming paradigms. An HLS compiler must optimize the memory hierarchy of a
Fig. 1. We decouple the algorithm description sobel\_x from its realization in hardware make\_local\_op. The hardware realization is a function that specifies important transformations for exploitation of parallelism and memory architecture. The function generate(vhls) selects the backend for code generation, which is Vivado HLS in this case. Ultimately, an optimized input code for HLS is generated by partially evaluating the algorithm and realization functions.

hardware implementation and parallelize its data paths [8]. In order to achieve good performance, HLS languages demand programmers to also specify the hardware architecture of an application instead of just its algorithm. For this reason, HLS languages offer hardware-specific pragmas. This ad-hoc mix of software and hardware features makes it difficult for programmers to optimize an application.

Pragmas allow to exploit different design choices, but they cannot be used in a modular way because the preprocessor already resolves them. In addition, most HLS tools rely on their own C dialect, which prevents code portability. For example, Xilinx Vivado HLS [45] uses C++ as base language while Intel SDK [19] (formerly Altera) uses OpenCL C. These severe restrictions make it hard to use existing HLS languages in a portable and modular way.

In this paper, we advocate to describe FPGA designs using functional abstractions and partial evaluation to generate optimized HLS code. Consider Figure 1 for an example from image processing: With a functional language, we separate the description of the sobel\_x operator from its realization in hardware. The hardware realization make\_local\_op is a function that specifies the data path, the parallelization, and memory architecture. Thus, the algorithm and hardware architecture descriptions are described by a set of higher-order functions. A partial evaluator, ultimately, combines these functions to generate an HLS code that delivers high-performance circuit designs when compiled with HLS tools. Since the initial descriptions are high-level, compact, and functional, they are reusable and distributable as a library. We leverage the AnyDSL compiler framework [24] to perform partial evaluation and extend it to generate input HLS code for Intel and Xilinx FPGA devices. We claim that this approach leads to cleaner and better composable code than existing HLS approaches, and is able to produce highly efficient hardware implementations.

Contributions: In summary, this paper makes the following contributions:

- We extend AnyDSL framework by hardware-specific memory types and parallelization constructs to target FPGAs (see Section 2).
- We present AnyHLS\(^1\), a set of major abstractions that significantly eases the design of libraries for HLS-based FPGA implementations. These functional abstractions include important loop transformations for performance optimizations as well as control structures such as Finite State Machines (FSMs), multiplexers (MUXs), and reduction operators (see Section 2).

---

1https://github.com/cg-saarland/anyhls.git
As a case study, we present a library for image processing that is based on AnyHLS’s abstractions (see Section 3). We demonstrate that the performance of the circuits synthesized from this library is on par with or even exceeds those using existing state-of-the-art domain-specific compilers (see Section 4).

2 THE AnyHLS LIBRARY

Efficient and resource-friendly FPGA designs require application-specific optimizations. These optimizations and transformations are well known in the community. For example, de Fine Licht et al. [11] discuss the key transformations of HLS codes such as loop unrolling and pipelining. In our setting, the programmer defines and provides these abstractions using AnyDSL for a given domain in the form of a library (see Figure 2). They describe the whole hardware design from the low-level memory layout to the operator implementations with support for low-level loop transformations throughout the design. We rely on partial evaluation to combine those abstractions and to remove overhead associated with them. This is in contrast to other domain-specific approaches like Rigel [18] or Hipacc [37], which rely on domain-specific compilers to instantiate predefined templates or macros.

In the following, we briefly present the relevant key concepts of AnyDSL (Section 2.1) before presenting our extensions to AnyDSL, key abstractions for FPGA designs, and HLS code generation (Section 2.2). Then, Section 3 introduces an image processing library based on these key abstractions. Finally, Section 4 evaluates the overall approach.

2.1 AnyDSL Compiler Framework

AnyDSL2 [23, 24] is a compiler framework for designing high-performance, domain-specific libraries. It provides the imperative and functional language Impala. Its syntax is inspired by Rust. We will now briefly discuss Impala’s most important features we rely on in AnyHLS.

https://anydsl.github.io
2.1.1 Partial Evaluation. Impala enables programmers to partially evaluate [16] their program at compile time. Programmers control the partial evaluator via filters [9]. These are Boolean expressions of the form \( @(expr) \) that annotate function signatures. Each call site instantiates the callee’s filter with the corresponding argument list. If the expression evaluates to `true`, the call will be specialized. Additionally, the expression `?expr` yields `true`, if `expr` is known at compile time; the expression `$expr` is never considered constant by the evaluator. For example, the following \( @(?n) \) filter will only specialize calls to `pow` if `n` is statically known at compile time:

```plaintext
fn @(?n) pow(x: int, n: int) -> int {
    if n == 0 {
        1
    } else {
        if n % 2 == 0 {
            let y = pow(x, n / 2);
            y * y
        } else {
            x * pow(x, n - 1)
        }
    }
}
```

Thus, the calls
```
let z = pow(x, 5);
let z = pow(3, 5);
```
will result in the following equivalent sequences of instructions after specialization:
```
let y = x * x;
let z = x * y * y;
let z = 243;
```

As syntactic sugar, \( @ \) is available as shorthand for \( @(true) \). This causes the partial evaluator to always specialize the annotated function.

2.1.2 Generators. Because iteration on various domains is a common pattern, Impala provides syntactic sugar for invoking certain higher-order functions. The loop

```plaintext
for var1, ..., varn in iter(arg1, ..., argn) { /* ... */ }
```

translates to

```plaintext
iter(arg1, ..., argn, |var1, ..., varn| { /* ... */ });
```

The body of the `for` loop and the iteration variables constitute an anonymous function
```
|var1, ..., varn| { /* ... */ }
```

that is passed to `iter` as the last argument. We call functions that are invokable like this `generators`. Domain-specific libraries implemented in Impala make busy use of these features as they allow programmers to write custom generators that take advantage of both domain knowledge and certain hardware features, as we will see in the next section.

Generators are particularly powerful in combination with partial evaluation:

```plaintext
type Body = fn(int) -> ();
fn @(a & ?b) unroll(a: int, b: int, body: Body) -> () {
    if a < b { body(a); unroll(a+1, b, body) }
}
fn @(range(a: int, b: int, body: Body) -> () {
    unroll($a, b, body)
}
```

Both generators iterate from `a` (inclusive) to `b` (exclusive) while invoking body each time. The filter `unroll` tells the partial evaluator to completely unroll the recursion if both loop bounds are statically known at a particular call site. The function `range` wraps a call to `unroll` but prevents the partial evaluator from unrolling because it always considers `$a` as dynamic.
2.2 Building Abstractions for FPGA Designs

In the following, we present abstractions for the key transformations and design patterns that are common in FPGA design. These include (a) important loop transformations, (b) control flow and data flow descriptions such as FSMs and reductions, (c) MUXs, and (d) the explicit utilization of different memory types. Approaches like Spatial [21] expose these patterns within the language—new patterns require dedicated support from the compiler. Hence, these languages and compilers are restricted to a specialized application domain they have been designed for. In AnyHLS, Impala's functional language and partial evaluation allow us to design the abstractions needed for FPGA synthesis in the form of a library. New patterns can be added to the library without dedicated support from the compiler.

2.2.1 Loop Transformations. C++ compilers usually provide certain preprocessor directives that perform particular code transformations. A common feature is to unroll loops (see left-hand side):

```c++
for (int i=0; i<N/W; ++i) {
    for (int w=0; w<W; ++w) {
        #pragma unroll
        body(i*W + w);
    }
}
```

Such pragmas are built into the compiler. The Impala version (right-hand side) uses generators that are entirely implemented as a library.

Generators, unlike C++ pragmas, are first-class citizens of the Impala language. This allows programmers to implement sophisticated loop transformations. For example, the following function tile returns a new generator. It instantiates a tiled loop nest of the specified tile size with the Loops inner and outer:

```impala
type Loop = fn(int, int, fn(int) -> ()) -> ();
fn @ tile (size : int, inner : Loop, outer : Loop) -> Loop {
    @|beg, end, body| outer(0, (end - beg) / size,
    |i| inner(i * size + beg, (i + 1) * size + end, |j| body))
} 
let schedule = tile(W, unroll, range);
for i in schedule(0, N) {
    body(i)
}
```

Passing W for the tiling size, unroll for the inner loop, and range for the outer loop yields a generator that is identical to the loop nest at the beginning of this paragraph. With this design, we can reuse or explore iteration techniques without touching the actual body of a for loop. For example, consider the processing options for a two-dimensional loop nest as shown in Figure 3: When just passing range as inner and outer loop, the partial evaluator will keep the loop nest and, hence, not unroll body and instantiate it only once. Unrolling the inner loop replicates body and increases the bandwidth requirements accordingly. Unrolling the outer loop also replicates body, but in a way that benefits data reuse from temporal locality of an iterative algorithm. Unrolling both loops replicate body for increased bandwidth and data reuse for temporal locality.

C/C++-based HLS solutions often use a pragma to mark a loop amenable for pipelining. This means parallel execution of the loop iterations in hardware. For example, the following code on the left uses an initiation interval (II) of 3:

```c++
for (int i=0; i<N; ++i) {
    #pragma HLS pipeline II=3
    body(i);
}
```

Instead of a pragma (on the left), AnyHLS uses the intrinsic generator pipeline (on the right). This enables the programmer to invoke and pass around pipeline—just like any other generator.
2.2.2 Finite State Machines. AnyHLS models computations that do not only depend on the inputs but also on an internal state with an FSM. In order to define an FSM, programmers need to specify states and a transition function that determines when to change the current state based on the machine’s input. This is especially beneficial for modeling control flow. To describe an FSM in Impala, we start by introducing types to represent the states and the machine itself:

```plaintext
type State = int;
struct FSM {
    add: fn(State, fn() -> (), fn() -> State) -> (),
    run: fn(State) -> ()
}
```

An object of type FSM provides two operations: adding one state with add or running the computation. The add method takes the name of the state, an action to be performed for this state, and a transition function associated with this state. Once all states are added, the programmer runs the machine by passing the initial state. The following example adds 1 to every element of an array:

```plaintext
let buf = /* ... */;
let mut (idx, pixel) = (0, 0);
let fsm = make_fsm();
fsm.add(Read, || pixel = buf(idx),
        if idx >= len { Exit } else { Compute });
fsm.add(Compute, || pixel += 1, || Write);
fsm.add(Write, || buf(idx++) = pixel, || Read);
fsm.run(Read);
```

Just like the other abstractions introduced in this section, the constructor for an FSM is not a built-in function of the compiler but a regular Impala function (see Appendix A). In some cases, we want to execute the FSM in a pipelined way. For this scenario, we add a second method run_pipelined (see Section 3 and Appendix A for details).

Reductions are useful in many contexts. The following function takes an array of values, a range within, and an operator:

```plaintext
type T = int;
fn @(?beg & ?end) reduce(beg: int, end: int, input: &[T],
                       op: fn(T, T) -> T) -> T {
    let n = end - beg;
    if n == 1 {
        input(beg)
    } else {
        let m = (end + beg) / 2;
        let a = reduce(beg, m, input, op);
        let b = reduce(m, end, input, op);
        op(a, b)
    }
}
```

In the above filter, the recursion will be completely unfolded if the range is statically known. Thus,

```plaintext
reduce(0, 4, [a, b, c, d], |x, y| x + y)
```
yields: \((a + b) + (c + d)\).

2.2.3 Reductions.

2.2.4 Multiplexers. MUXs are devices that take \(n\) inputs and a selection index \(i \in [0, n - 1]\). They yield the \(i\)-th input. AnyHLS models this with the following function that takes an array of inputs as the argument:

```c
type T = int;
fn @(?n) mux(i: int, n: int, input : &[fn() -> T]) -> T {
    for j in unroll(0, n - 1) {
        if i == j { return(input(j)()) }
    }
    input(n - 1)()
}
```

If the number of inputs \(n\) is known, the partial evaluator will generate a sequence of \texttt{if} statements for each possible case because the constant \(n\) will be propagated to the call to \texttt{unroll}. This will in turn trigger the evaluator to unroll the loop. For example, the partial evaluator will specialize the call

```c
let sel = value & 3;
mux(sel, 4, [multiple_four, odd, even, odd])
```

to the following sequence of \texttt{if} statements:

```c
let sel = value & 3;
if sel == 0 { multiple_of_four() }
else if sel == 1 { odd() }
else if sel == 2 { even() }
else { odd() }
```

2.2.5 Memory Types and Memory Abstractions. FPGAs have different memory types of varying sizes and access properties. Impala supports four memory types specific to hardware design (see Figure 5): global memory, on-chip memory, registers, and streams. Global memory (typically DRAM) is allocated on the host using our runtime and accessed through regular pointers. On-chip memory (e.g., BRAM or M10K/M20K) for the FPGA is allocated using the \texttt{reserve_onchip} compiler intrinsic. Memory accesses using the pointer returned by this intrinsic will map to on-chip memory. Standard variables are mapped to registers, and a specific \texttt{stream} type is available to allow for the communication between FPGA kernels. Memory-wise, a \texttt{stream} is mapped to registers or on-chip memory by the HLS tools.

Vivado HLS uses a pragma to annotate register arrays:

```c
typedef int T;
T Regs1D[size];
#pragma HLS variable=Regs1D array_partition dim=0
```
Since normal variables are stored in registers, a recursive structure that holds one register per recursion level constitutes a register array:

```plaintext
type T = int;
struct Regs1D {
  read: fn(int) -> T,
  write: fn(int, T) -> ()
  size: int
}
fn @ make_regs1d(size: int) -> Regs1D {
  if size == 0 {
    Regs1D {
      read: @|_| 0,
      write: @|_, _| ()
      size: size
    }
  } else {
    let mut reg: T;
    let others = make_regs1d(size - 1);
    Regs1D {
      read: @|i| if i+1 == size { reg }
        else { others.read(i) },
      write: @|i, v| if i+1 == size { reg = v }
        else { others.write(i, v) },
      size: size
    }
  }
}
```

In the base case, this function generates an empty register array that always reads as 0 and cannot be written to. When the size is not zero, the function allocates a register by declaring a variable named reg, and creates a smaller register array with one element less named others. The read and write functions test if the index i is equal to the index of the current register. In the case of a match, the current register is used. Otherwise, the search continues in the smaller array.

Note that we have annotated `make_regs1d`, `read`, and `write` for partial evaluation. Thus, any call to these functions will be inlined recursively. This means that the search to find the register to read to or write from will be performed at compile-time, and no test will remain in the specialized code. By doing this, we created a generator for register arrays that we instantiate with the following code:

```plaintext
let regs = make_regs1d(size);
```

The generated code will not contain any compiler directives, and thus targets Vivado HLS or Intel FPGA SDK for OpenCL (AOCL) alike. Moreover, these registers will be optimized by the AnyDSL compiler, just like any other variables: unnecessary assignments are avoided, and a cleaner HLS code is generated. Based on this one-dimensional register array, AnyHLS provides generators for two-dimensional register arrays. Generators for arrays of on-chip memory and streams work the same way (see Figure 6).

2.2.6 HLS Code Generation. For HLS code generation, we implemented an intrinsic named `vhls` in AnyHLS to emit Vivado HLS and an intrinsic named `opencl` to emit AOCL:

```plaintext
with vhls() { body() } with opencl() { body() }
```
With OpenCL we use a grid and block size of \((1, 1, 1)\) to generate a single work-item kernel, as the official AOCL documentation recommends. To provide an abstraction over both HLS backends, we create a wrapper `generate` that expects a code generation function:

```rust

```type Backend = fn(fn() -> ()) -> ();
fn @ generate(be: Backend, body: fn() -> ()) -> () {
    with be() { body() }
}
```Switching backends is now just a matter of passing an appropriate function to `generate`:

```rust
let backend = vhls; // or opencl
with generate(backend) { body() }
```

# 3 DESIGN OF A LIBRARY FOR IMAGE PROCESSING ON FPGA

In this section, we present a library for image processing based on the fundamental abstractions introduced in Section 2.2. Our low-level implementation is similar to existing domain-specific languages targeting FPGAs [18, 37]. For this reason, we focus on the interface of our abstractions as seen by the programmer.

## 3.1 Vectorization

Image processing applications consist of loops that possess a very high degree of spatial parallelism. This should be exploited to reach the bandwidth speed of memory technologies. A resource-efficient approach, so-called *vectorization* or *loop coarsening*, is to aggregate the input pixels to vectors and process multiple input data at the same time to calculate multiple output pixels in parallel [40, 33, 43]. This replicates only the arithmetic operations applied to data (so-called datapath) instead of the whole accelerator, similar to Single Instruction Multiple Data (SIMD) architectures. Vectorization requires a control structure specialized to a considered hardware design. We support the automatic vectorization of an application by a given factor \(v\) when using our image processing library. For example, the `make_local_op` function has an additional parameter to specify the desired vectorization and will propagate this information to the functions it uses internally: `make_local_op(op, v)`. For brevity, we omit the parameter for the vectorization factor for the remaining abstractions in this section.

## 3.2 Memory Abstractions for Image Processing

### 3.2.1 Memory Accessor

In order to optimize memory access and encapsulate the contained memory type (on-chip memory, etc.) into a data structure, we decouple the data transfer from the data use via the following memory abstractions:
Similar to hardware design practices, these memory abstractions require the memory address to be updated before the read/write operations. The update function transfers data from/to the encapsulated memory to/from staging registers using vector data types. Then, the read/write functions access an element of the vector. This increases data reuse and DRAM-to-on-chip memory bandwidth [5].

3.2.2 Stream Processing. Inter-kernel dependencies of an algorithm should be accessed on-the-fly in combination with fine-granular communication in order to pipeline the full implementation with a fixed throughput. That is, as soon as a block produces one data, the next block consumes it. In the best case, this requires only a single register of a small buffer instead of reading/writing to temporary images:

We define a stream between two kernels as follows:

```
fn make_mem_from_stream(size: int, data: stream) -> Mem1D;
```

3.2.3 Line Buffers. Storing an entire image to on-chip memory before execution is not feasible since on-chip memory blocks are limited in FPGAs. On the other hand, feeding the data on demand from main memory is extremely slow. Still, it is possible to leverage fast on-chip memory by using it as FIFO buffers containing only the necessary lines of the input images (W pixels per line).

This enables parallel reads at the output for every pixel read at the input. We model a line buffer as follows:

```
type LineBuf1D = fn(Mem1D) -> Mem1D;
fn make_linebuf1d(width: int) -> LineBuf1D;
// similar for LineBuf2D
```

Akin to Regs1D (see Section 2.2.5), a recursive call builds an array of line buffers.

3.2.4 Sliding Window. Registers are the most amenable resources to hold data for highly parallelized access. A sliding window of size $w \times h$ updates the constituting shift registers by a new column of $h$ pixels and enables parallel access to $w \cdot h$ pixels.
This provides high data reuse for temporal locality and avoids waste of on-chip memory blocks that might be utilized for a similar data bandwidth. Our implementation uses \texttt{make\_regs2d} for an explicit declaration of registers and supports pixel-based indexing at the output.

\begin{verbatim}
type Swin2D = fn(Mem2D) -> Mem2D; fn @ make_sliding_window(w: int, h: int) -> Swin2D {
  let win = make_regs2d(w, h);
  // ...
}
\end{verbatim}

### 3.3 Loop Abstractions for Image Processing

#### 3.3.1 Point Operators

Algorithms such as image scaling and color transformation calculate an output pixel for every input pixel. The point operator abstraction in AnyHLS yields a vectorized pipeline over the input and output image. This abstraction is parametric in its vector factor \( v \) and the desired operator function \( \text{op} \).

\begin{verbatim}
type PointOp = fn(Mem1D) -> Mem1D; fn @ make_point_op(v: int, op: Op) -> PointOp {
  @ |img, out| {
    for idx in pipeline(1, 0, img.size) {
      img.update(idx);
      for i in unroll(0, v) {
        out.write(i, op(img.read(i)));
      }
      out.update(idx);
    }
  }
}
\end{verbatim}

The following figure illustrates the AnyHLS point operator:

The total latency is

\[
L = L_{\text{arith}} + \lceil \frac{W}{v} \rceil \cdot H \text{ cycles}
\]

where \( W \) and \( H \) are the width and height of the input image, and \( L_{\text{arith}} \) is the latency of the data path.

#### 3.3.2 Local Operators

Algorithms such as Gaussian blur and Sobel edge detection calculate an output pixel by considering the corresponding input pixel and a certain neighborhood of it in a local window. Thus, a local operator with a \( w \times h \) window requires \( w \cdot h \) pixel reads for every output. The same \((w-1)\cdot h\) pixels are used to calculate results at the image coordinates \((x, y)\) and \((x+1, y)\). This spatial locality is transformed into temporal locality when input images are read in raster order for burst mode, and subsequent pixels are sequentially processed with a streaming pipeline implementation. The local operator implementation in AnyHLS (shown below) consists of line buffers and a sliding window to hold dependency pixels in on-chip memory and calculates a new result for every new pixel read.

---

3 Appendix A depicts an alternative point operator implementation that is based upon the FSM abstraction in combination with \texttt{run\_pipelined}. Both variants generate similar HLS code.
This provides a throughput of \( v \) pixels per clock cycle at the cost of an initial latency (\( v \) is the vectorization factor)

\[
L_{\text{initial}} = L_{\text{arith}} + \left( \left\lfloor \frac{h}{2} \right\rfloor \cdot \left\lceil \frac{W}{v} \right\rceil + \left\lfloor \frac{w}{v} \right\rfloor \right)
\]

that is spent for caching neighboring pixels of the first calculation. The final latency is thus:

\[
L = L_{\text{initial}} + \left( \left\lceil \frac{W}{v} \right\rceil \cdot H \right)
\]

Compared to the local operator in Figure 1, we also support boundary handling. We specify the extent of the local operator (filter size / 2) as well as functions specifying the boundary handling for the lower and upper bounds. Then, row and column selection functions apply border handling correspondingly in \( x \)- and \( y \)-directions by using one-dimensional multiplexer arrays similar to Özkan et al. [33].

### 3.4 Algorithm Specification

We design applications by decoupling their algorithmic description from their schedule and memory operations. For instance, typical image operators, such as the following Sobel filter, just resort to the `make_local_op` generator. Similarly, we implement a point operator for RGB-to-gray color conversion as follows:

```rust
fn sobel_edge(output: &mut [T], input: &[T]) -> {} {
    let img = make_raw_mem2d(width, height, input);
    let dx = make_raw_mem2d(width, height, output);
    let sobel_extents = extents(1, 1); // for 3x3 filter
    let operator = make_local_op(4, // vector factor
        sobel_operator_x, sobel_extents, mirror, mirror);
    with generate(hls) (operator(img, dx); )
}
```
The image data structure is opaque. The target platform mapping determines its layout. AnyHLS provides common border handling functions as well as point and global operators such as reductions (see Section 2.2.3). These operators are composable to allow for more sophisticated ones.

4 EVALUATION AND RESULTS

In the following, we present experimental results for a Cyclone V GT 5CGTD9 FPGA and a Zynq XC7Z020 FPGA using Intel FPGA SDK for OpenCL 18.1 and Xilinx Vivado HLS 2017.2, respectively. We compare the results of AnyHLS to other state-of-the-art domain-specific approaches including Halide-HLS [35] and Hipacc [37].

4.1 Applications

We evaluate the following applications:

- **Gaussian (Gauss)** blurring an image with a $5 \times 5$ integer kernel
- **Harris corner detector (Harris)** consisting of 9 kernels that resort to integer arithmetic and horizontal/vertical derivatives
- **Jacobi** smoothing an image with a $3 \times 3$ integer kernel
- **filter chain (FChain)** consisting of 3 convolution kernels as a pre-processing algorithm
- **bilateral filter (Bilateral)**, a $5 \times 5$ floating-point kernel as an edge-preserving and noise-smoothing function based on the exponential function
- **mean filter (MF)**, a $5 \times 5$ filter that finds the average within a local window via 8-bit arithmetic
- **SobelLuma**, an edge detection algorithm provided as a design example by Intel. The algorithm consists of RGB to Luma color conversion, Sobel filters, and thresholding

4.2 Evaluation of the Implementation Results

This section evaluates the generated hardware designs based on their throughput, latency, and resource utilization. FPGAs possess two types of resources:

1. computational: LUTs and DSP blocks;
2. memory: Flipflops (FFs) and on-chip memory (BRAM/M20K).

A SLICE/ALM is comprised of look-up tables (LUTs) and flip flops, thus indicate the resource usage when considered with the DSP block and on-chip memory blocks.

The implementation results presented for Vivado HLS feature only the kernel logic, while those by Intel OpenCL include PCIe interfaces. The execution time of an FPGA circuit (Vivado HLS implementation) equals to $T_{clk} \cdot$ latency, where $T_{clk}$ is the clock period of the maximum achievable clock frequency (lower is better). We measured the timing results for Intel OpenCL by executing the applications on a Cyclone V GT 5CGTD9 FPGA. This is the case for all analyzed applications. We have no intention nor license rights [10, §4] [20, §2] to benchmark and compare the considered FPGA technologies or HLS tools.
4.3 Library Optimizations

AnyHLS exploits stream processing and performs implicit parallelization. The following subsections show the impact of those optimizations.

4.3.1 Stream Processing. Memory transfers between FPGA’s programmable logic and external memory are one of the most time-consuming parts of many image processing applications. AnyHLS streaming pipeline optimization passes dependency pixels directly from the producer to the consumer kernel, as explained in Section 3.2.2. This allows pipelined kernel execution and makes intermediate images between kernels superfluous. The more intermediate images are eliminated, the better the performance of the resulting designs. For example, this eliminates 8 intermediate images in Harris corner and 2 in filter chain, see Figure 7 for the performance impact.

![Execution time for naïve and streaming pipeline implementations of the Harris and FChain for an Intel Cyclone V for images of 1024 × 1024.](image)

The throughput of both streaming pipeline implementations is indeed determined by their slowest individual kernel, which is a local operator. Consider Table 1, which displays the Vivado HLS reports. The latency results correspond to Equation (3).

| App. | Largest mask | Sequential Dependency | Latency [cyc.] | Throughput [MB/s] |
|------|--------------|------------------------|---------------|-------------------|
| FChain | 5 × 5        | local + local + local | 1050649       | 821               |
| Harris | 3 × 3        | local + local + point  | 1049634       | 825               |

4.3.2 Vectorization. Many FPGA implementations benefit from parallel processing in order to increase memory bandwidth. AnyHLS implicitly parallelizes a given image pipeline by a vectorization factor v. As an example, Figure 8 shows the Post Place and Route (PPnR) results, along with the achieved memory throughput for different vectorization factors for the mean filter on a Cyclone V. The memory-bound of the Cyclone V is reported by Intel’s diagnosis tool. The speedup is almost linear, whereas resource utilization is sub-linear to the vectorization factor, as Figure 8 depicts. AnyHLS exploits the data reuse between consecutive iterations of the local operators. Data is read and written with the vectorized data types. The line buffers and the sliding window are extended to hold dependency pixels for vectorized processing. Thus, only the datapath is replicated instead of the whole accelerator implementation (see Section 3.1). All the considered applications except...
Throughput [MB/s] vs Vectorization factor ($v$)

**Fig. 8.** PPnR results of AnyHLS’s mean filter implementation on an Intel Cyclone V. The memory bound of the device for our setup is 1344.80 MB/s.

Bilateral in Figure 10 reach the memory bound. Bilateral is compute-bound due to its large number of floating-point operations.

### 4.4 Hardware Design Evaluation

We evaluate the generated hardware designs based on their throughput, latency, and resource utilization. As a reference, we use the designs generated by Halide-HLS [35] and Hipacc [37], two state-of-the-art image processing DSLs that generate better results than previous approaches (e.g., Xilinx OpenCV). In contrast to these, which implement dedicated HLS code generators, AnyHLS is essentially implemented as a library within the AnyDSL framework, as illustrated in Figure 2. Our focus is to show that higher-order abstractions, together with partial evaluation, are powerful enough to design a library targeting different HLS compilers.

#### 4.4.1 Experiments using Xilinx Vivado HLS

We evaluate the results of circuits generated using AnyHLS in comparison with the domain-specific language approaches Hipacc and Halide-HLS. We consider two representative applications from the Halide-HLS repository with different configurations (border handling mode and vectorization factor): Gauss and Harris. The applications are rewritten for Hipacc and AnyHLS by respecting their original descriptions. This ensures that Halide-HLS applications have been implemented with adequate scheduling primitives. Hipacc and AnyHLS implementations require only the algorithm descriptions as input.

As Tables 2 and 3 report, AnyHLS provides the implementations with the lowest latency (number of clock cycles) amongst the considered approaches. The execution time of an implementation equals $T_{clk} \cdot \text{latency}$, where $T_{clk}$ is the clock period of the maximum achievable clock frequency (lower is better). Overall, AnyHLS processes a given image faster than the other DSL implementations.

Let us consider the number of BRAMs utilized for the Gaussian blur: The line buffers need to hold 4 image lines for the $5 \times 5$ kernel, as explained in Section 3.3.2. The image width is 1020 and the pixel size is 32 bits. Therefore, eight 18K BRAMs are required, as shown in Table 2. The number of BRAMs is sub-linear to the vectorization factors ($v$).

Unlike Hipacc and AnyHLS, Halide-HLS pads input images according to the border handling mode. This requires more on-chip memory and increases latency. In the worst case, the number of BRAMs doubles as shown in Table 3 (1024 integer pixels require 16 18K BRAMs to buffer four image lines).

For almost all applications in Tables 2 and 3, AnyHLS implementations demand fewer resources and deliver higher performance. The DSLs have been developed by FPGA experts and perform better than many other existing libraries. The performance difference between AnyHLS and Hipacc
Table 2. PPnR results for the Xilinx Zynq board for images of size 1020 × 1020 and $T_{\text{target}} = 5$ ns (corresponds to $f_{\text{target}} = 200$ MHz). Border handling is undefined.

| App   | $v$ | #BRAM | #SLICE | #DSP | $T_{\text{clk}}$ [ns] | Latency [cyc.] | Throughput [MB/s] |
|-------|-----|-------|--------|------|------------------------|----------------|------------------|
| Gauss | 1   | AnyHLS| 8      | 463  | 16                     | 4.82           | 1042456          |
|       |     | Halide-HLS| 8     | 1823 | 50                     | 9.02           | 1052673          |
|       |     | Hipacc | 8      | 473  | 16                     | 5.21           | 1044500          |
| Harris| 4   | AnyHLS| 16     | 1441 | 80                     | 5.25           | 260626           |
|       |     | Halide-HLS| 16    | 4112 | 180                    | 9.53           | 266241           |
|       |     | Hipacc | 16     | 1519 | 64                     | 5.19           | 261649           |

Table 3. PPnR results for the Gaussian blur with clamping at the borders. Image sizes are 1024 × 1024, $v = 1$, $f_{\text{target}} = 200$ MHz.

| Framework | #BRAM | #SLICE | #DSP | $T_{\text{clk}}$ [ns] | Latency [cyc.] | Throughput [MB/s] |
|-----------|-------|--------|------|------------------------|----------------|------------------|
| AnyHLS    | 8     | 1646   | 16   | 4.94                   | 1050641        | 801.8            |
| Halide-HLS| 16    | 2096   | 50   | 8.55                   | 1060897        | 458.7            |
| Hipacc    | 8     | 1709   | 16   | 4.82                   | 1052693        | 820.1            |

is not significant since the latency of both implementations is close to optimal. Equation (3) shows the minimum number of clock cycles required for a local operator iteration. For instance, the theoretical latency of Gauss is 1042442 cycles for $v = 1$. Latency of the Gauss generated by AnyHLS and Hipacc is only 14 and 2058 clock cycles, respectively. In conclusion, we claim that AnyHLS is on par with or exceeds existing approaches.

4.4.2 Experiments using Intel FPGA SDK for OpenCL (AOCL). Table 4 presents the implementation results for an edge detection algorithm provided as a design example by Intel. The algorithms consist of RGB to Luma color conversion, Sobel filters, and thresholding. Intel’s implementations consist of a single-work item kernel that utilizes shift registers according to the FPGA design paradigm. These types of techniques are recommended by Intel’s optimization guide [19] despite that the same OpenCL code performs drastically bad on other computing platforms. We implemented this algorithm with Hipacc and AnyHLS using algorithmic abstractions (as in Section 3.4). Both Hipacc and AnyHLS provide a higher throughput even without vectorization. In order to reach memory bound, we would have to rewrite Intel’s hand-tuned design example to exploit further parallelism. AnyHLS uses slightly less resource, whereas Hipacc provides slightly higher throughput for all the vectorization factors. Similar to Figure 8, both frameworks yield throughputs very close to the memory bound of the Intel Cyclone V.

The OpenCL NDRange kernel paradigm conveys multiple concurrent threads for data-level parallelism. OpenCL-based HLS tools exploit this paradigm to synthesize hardware. AOCL provides attributes for NDRange kernels to transform its iteration space. The `num_compute_units` attribute
Table 4. PPnR results of an edge detection application for the Intel Cyclone V. Image sizes are 1024 × 1024. None of the implementations use DSPs.

| v | Framework | #M10K  | #ALM   | #DSP | Throughput [MB/s] |
|---|-----------|--------|--------|------|------------------|
| 1 | Intel’s Imp. | 290    | 23830  | 0    | 419.5            |
|   | AnyHLS    | 291    | 23797  | 0    | 422.5            |
|   | Hipacc    | 318    | 25258  | 0    | 449.1            |
| 16| Intel’s Imp.| -      | -      | 0    | -                |
|   | AnyHLS    | 337    | 29126  | 0    | 1278.3           |
|   | Hipacc    | 362    | 35079  | 0    | 1327.7           |
| 32| Intel’s Imp.| -      | -      | 0    | -                |
|   | AnyHLS    | 401    | 38069  | 0    | 1303.8           |
|   | Hipacc    | 421    | 44059  | 0    | 1320.0           |

Fig. 9. Design space for a 5 × 5 mean filter using an NDRange kernel (using the num_compute_units / num_simd_work_items attributes) and AnyHLS (using the vectorization factor v) for an Intel Cyclone V.

replicates the kernel logic, whereas num_simd_work_items vectorizes the kernel implementation. Combinations of those provide a vast design space for the same NDRange kernel. However, as Figure 9 demonstrates, AnyHLS achieves implementations that are orders of magnitude faster than using attributes in AOCL.

Finally, Figures 10 and 11 present a comparison between AnyHLS and the AOCL backend of Hipacc. As shown in Figure 2, Hipacc has an individual backend and template library written with preprocessor directives to generate high-performance OpenCL code for FPGAs. In contrast, the application and library code in AnyHLS stays the same. The generated AOCL code consists of a loop that iterates over the input image. Compared to Hipacc, AnyHLS achieves similar performance but outperforms Hipacc for multi-kernel applications such as the Harris corner detector. This shows that AnyHLS optimizes the inter-kernel dependencies better than Hipacc (see Section 3.2.2).

4 These parallelization attributes are suggested for NDRange kernels, not for the single-work item kernels using shift registers such as the edge detection application shown in Table 4 [19].
Fig. 10. Throughput measurements for an Intel Cyclone V for the implementations generated from AnyHLS and Hipacc. Resource utilization for the same implementations are shown in Figure 11.

| App   | v | Framework | #M10K | #ALM | #DSP | Throughput [MB/s] |
|-------|---|-----------|-------|------|------|------------------|
| Gauss | 16| AnyHLS    | 401   | 37509| 0    | 1330.1           |
|       | 16| Hipacc    | 402   | 35090| 0    | 1301.2           |
| Jacobi| 16| AnyHLS    | 370   | 31446| 0    | 1328.8           |
|       | 16| Hipacc    | 372   | 30296| 0    | 1282.9           |
| Bilat. | 1 | AnyHLS    | 399   | 79270| 153  | 326.6            |
|       | 1 | Hipacc    | 422   | 79892| 159  | 434.7            |
| MF    | 16| AnyHLS    | 400   | 39266| 0    | 1255.68          |
|       | 16| Hipacc    | -     | -    | -    | -                |
|       | 8 | Hipacc    | 351   | 31796| 0    | 1275.9           |
| FChain| 8 | AnyHLS    | 418   | 44807| 0    | 1230.6           |
|       | 8 | Hipacc    | 645   | 64225| 0    | 427.4            |
| Harris| 8 | AnyHLS    | 442   | 50537| 96   | 1158.5           |
|       | 8 | Hipacc    | 668   | 74246| 96   | 187.14           |

Fig. 11. PPnR for the Intel Cyclone V. Missing numbers (-) indicate that the generated implementations do not fit the board.

5 RELATED WORK

Languages at Register-Transfer Level (RTL). HDL-based design is time-consuming and error-prone. Often, the modification of an existing design is tedious: Programmers must rewrite the code several times to meet performance and/or area constraints. Recent languages such as Chisel [1], VeriScala [25], and MyHDL [12] let programmers create a functional description of their design but remain at the RTL.

High-Level Synthesis. HLS increases the abstraction level to an untimed high-level specification such as C++ or Java from a fully-timed RTL. This eases the hardware design problem by eliminating low-level issues such as clock-level timing, register allocation, and gate-level pipelining [34, 7]. Moreover, it enables software-like development for library design and verification. Modern HLS
tools such as AOCL and Xilinx SDX also offer system synthesis from the same code, utilizing hardware/software co-design to map program parts to either software or hardware.

After some early attempts, with the second wave [26], HLS tools are now able to generate high-quality results for DSP and datapath-oriented applications. Several authors [e.g., 7, 26, 2] have argued the following points as key to this success: (i) advancements in RTL design tools, (ii) device-specific code generation, (iii) domain-specific focus on the target applications, and (iv) generating both software and hardware from the same code. However, the lack of standardization of HLS languages and compilers hinders progress in this area [2]. In contrast, our approach allows developing HLS libraries in a portable and modular way.

C-based HLS. There is an ongoing discussion about whether C-based languages are good candidates for HLS [14, 39, 7, 2, 21]. The problem is that a high-performance C-based code written for HLS is entirely different from a software program. Thereby, the developer should express the FPGA implementation of an application using the language abstractions of software (i.e., arrays, loops to specify the memory hierarchy and hardware pipelining). Language extensions like pragmas fill the gap for the lacking FPGA-centric features. Since HLS compilers optimize the Intermediate Representation (IR) and not the source program [7], different programming styles may lead to different results [32, 38]. This ad-hoc mix of software and hardware is hard to optimize [21, 32]. The modularity and readability of C/C++ descriptions often conflict with best coding practices of HLS compilers [15, 41]. FPGA implementations must be defined statically for high-performance: types, loops, functions, and interfaces must be resolved at compile time [38, 15, 31, 41]. One option to achieve this in a generic way is C++ template metaprogramming. However, creating high-level abstractions in C++ using template metaprogramming is challenging [44, 38]. As a solution, we use partial evaluation to synthesize optimized HLS code from a given functional description of an algorithm. The generated code goes to the selected HLS tool. Consequently, we achieve competitive performance for different HLS tools from the same algorithm description (as shown for Vivado HLS and AOCL in Section 4).

DSLs for FPGAs. Developing efficient designs for FPGAs is difficult. DSLs use domain-specific knowledge to parallelize algorithms and generate low-level, optimized code [29]. Programming accelerators using DSLs is thus easier, in particular for FPGAs because the compiler performs scheduling. A prominent example of that is the FPGA version of Spiral [27]. It generates HDL for digital signal processing applications. In the domain of image processing, recent projects include Darkroom [17], Rigel [18], and the work of Pu et al. [35] based on Halide [36]. Hipacc [37], PolyMage [6], SODA [4], and RIPL [42] create image processing pipelines from a DSL. Rigel/Halide, PolyMage, and RIPL are declarative DSLs, whereas Hipacc is embedded into C++. All of these compilers, except Rigel, generate HLS code in order to simplify their backends. Other examples include Lift that targets FPGAs via algorithmic patterns [22] and Tiramisu [3] for data-parallel algorithms on dense arrays. It takes as input a set of scheduling commands from the user and feeds it to the polyhedral analysis of the compiler. However, a considerable portion of these scheduling primitives remains platform-specific [13]. Spatial [21] is a language for programming Coarse-Grained Reconfigurable Architectures (CGRAs) and FPGAs. Koepflinger et al. [21] argue against the usual mix of hardware and software abstractions in existing HLS languages. Instead, they provide language constructs to express control, memory, and interfaces of a hardware implementation.

Unlike these approaches, AnyHLS allows programmers to build the basic blocks and abstractions necessary for their application domain by themselves. This means that there is no need to change the compiler when adding support for a new application domain, since programmers can design custom control structures. Previously, we have shown how to abstract image border handling implementations for Intel FPGAs using AnyDSL [30]. In this paper, we present AnyHLS and an
image processing library to synthesize FPGA designs in a modular and abstract way for both Intel and Xilinx FPGAs. Partial evaluation removes the overhead of custom functional abstractions: As we have discussed in the paper, the final generated designs are competitive with those generated by DSL compilers such as Halide or Hipacc.

6 CONCLUSIONS

In this paper, we advocate the use of modern compiler technologies for high-level synthesis. We combine functional abstractions with the power of partial evaluation to decouple a high-level algorithm description from its hardware design that implements the algorithm. This process is entirely driven by code refinement, generating input code to HLS tools, such as Vivado HLS and AOCL, from the same code base. To specify important abstractions for hardware design, we have introduced a set of basic primitives. Library developers can rely on these primitives to create domain-specific libraries. As an example, we have implemented an image processing library for synthesis to FPGAs. Finally, we have shown that our results are on par or even better in performance compared to state-of-the-art approaches.

ACKNOWLEDGMENTS

This work is supported by the Federal Ministry of Education and Research (BMBF) as part of the Metacca and ProThOS projects, and the Intel Visual Computing Institute (IVCI) as well as the Cluster of Excellence on Multimodal Computing and Interaction (MMCI) at Saarland University.

REFERENCES

[1] J. Bachrach, H. Vo, B. Richards, Y. Lee, A. Waterman, R. Avižienis, J. Wawrzynek, and K. Asanović. 2012. Chisel: Constructing hardware in a Scala embedded language. In Proceedings of the 49th Annual Design Automation Conference (DAC). IEEE, (June 3–7, 2012), 1212–1221. DOI: 10.1145/2228360.2228584.

[2] D. F. Bacon, R. Rabbah, and S. Shukla. 2013. FPGA programming for the masses. Communications of the ACM, 56, 4, 56–63. DOI: 10.1145/2436696.2443836.

[3] R. Baghdadi, J. Ray, M. B. Romdhane, E. D. Sozzo, A. Akkas, Y. Zhang, P. Suriana, S. Kamil, and S. P. Amarasinghe. 2019. Tiramisu: A polyhedral compiler for expressing fast and portable code. In Proceedings of the IEEE/ACM International Symposium on Code Generation and Optimization (CGO). IEEE, (February 16–20, 2019), 193–205. DOI: 10.1109/CGO.2019.8661197.

[4] Y. Chi, J. Cong, P. Wei, and P. Zhou. 2018. Soda: stencil with optimized dataflow architecture. In 2018 IEEE/ACM International Conference on Computer-Aided Design (ICCAD). IEEE, 1–8. DOI: 10.1145/3240765.3240850.

[5] Y.-k. Choi, J. Cong, Z. Fang, Y. Hao, G. Reinman, and P. Wei. 2016. A quantitative analysis on microarchitectures of modern CPU-FPGA platforms. In Proceedings of the 53rd Annual Design Automation Conference (DAC). ACM, (June 5–9, 2016), 109:1–109:6. DOI: 10.1145/2897937.2897972.

[6] N. Chugh, V. Vasista, S. Purini, and U. Bondhugula. 2016. A DSL compiler for accelerating image processing pipelines on FPGAs. In Proceedings of the International Conference on Parallel Architecture and Compilation Techniques (PACT). ACM, (September 11–15, 2016), 327–338. DOI: 10.1145/2967938.2967969.

[7] J. Cong, B. Liu, S. Neuendorffer, J. Noguera, K. Vissers, and Z. Zhang. 2011. High-level synthesis for FPGAs: From prototyping to deployment. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 30, 4, 473–491. DOI: 10.1109/TCAD.2011.2110592.
[8] J. Cong, P. Wei, C. H. Yu, and P. Zhang. 2018. Automated accelerator generation and optimization with composable, parallel and pipeline architecture. In *Proceedings of the 55th Annual Design Automation Conference (DAC)*. ACM, (June 24–29, 2018), 154:1–154:6. DOI: 10.1145/3195970.3195999.

[9] C. Consel. 1988. New insights into partial evaluation: The SCHISM experiment. In *Proceedings of the 2nd European Symposium on Programming (ESOP)*. Springer, (March 21–24, 1988), 236–246. DOI: 10.1007/3-540-19027-9_16.

[10] 2014. Core evaluation license agreement. Version 2014.06. Xilinx, Inc., (June 2014). https://www.xilinx.com/products/intellectual-property/license/core-evaluation-license-agreement.html.

[11] J. de Fine Licht, S. Meierhans, and T. Hoefler. 2018. Transformations of high-level synthesis codes for high-performance computing. *The Computing Research Repository (CoRR)*. arXiv: 1805.08288 [cs.DC].

[12] J. Decaluwe. 2004. MyHDL: A Python-based hardware description language. *Linux Journal*, 127, 84–87.

[13] E. Del Sozzo, R. Baghdadi, S. Amarasinghe, and M. Santambrogio. 2018. A unified backend for targeting FPGAs from DSLs. In *Proceedings of the 29th Annual IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*. IEEE, (July 10–12, 2018), 41–48. DOI: 10.1109/ASAP.2018.8445108.

[14] S. A. Edwards. 2006. The challenges of synthesizing hardware from C-like languages. *IEEE Design & Test of Computers*, 23, 5, 375–386. DOI: 10.1109/MDT.2006.134.

[15] H. Eran, L. Zeno, Z. István, and M. Silberstein. 2019. Design patterns for code reuse in HLS packet processing pipelines. In *27th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*. IEEE, 208–217.

[16] Y. Futamura. 1982. Parital computation of programs. In *Proceedings of the RIMS Symposium on Software Science and Engineering*, 1–35. DOI: 10.1007/3-540-11980-9_13.

[17] J. Hegarty, J. Brunhaver, Z. DeVito, J. Ragan-Kelley, N. Cohen, S. Bell, A. Vasilyev, M. Horowitz, and P. Hanrahan. 2014. Darkroom: Compiling high-level image processing code into hardware pipelines. *ACM Transactions on Graphics (TOG)*, 33, 4, 144:1–144:11. DOI: 10.1145/2601097.2601174.

[18] J. Hegarty, R. Daly, Z. DeVito, J. Ragan-Kelley, M. Horowitz, and P. Hanrahan. 2016. Rigel: Flexible multi-rate image processing hardware. *ACM Transactions on Graphics (TOG)*, 35, 4, 85:1–85:11. DOI: 10.1145/2978249.2925892.

[19] Intel. 2017. Intel FPGA SDK for OpenCL: Best practices guide. (2017).

[20] 2009. Intel program license subscription agreement. Version Rev. 10/2009. Intel Corporation, (October 2009). https://www.intel.com/content/www/us/en/programmable/downloads/software/license/lic-proglic.html.

[21] D. Koepler, M. Feldman, R. Prabhakar, Y. Zhang, S. Hadjis, R. Fiszel, T. Zhao, L. Nardi, A. Pedram, C. Kozyrakis, and K. Olukotun. 2018. Spatial: A language and compiler for application accelerators. In *Proceedings of the 39th ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*. ACM, (June 18–22, 2018), 296–311. DOI: 10.1145/3192366.3192379.

[22] M. Kristien, B. Bodin, M. Steuwer, and C. Dubach. 2019. High-level synthesis of functional patterns with Lift. In *Proceedings of the 6th ACM SIGPLAN International Workshop on Libraries, Languages and Compilers for Array Programming, ARRAY@PLDI 2019, Phoenix, AZ, USA, June 22, 2019*, 35–45. DOI: 10.1145/3315454.3329957.

[23] R. Leißa, K. Boesche, S. Hack, R. Membarth, and P. Slusallek. 2015. Shallow embedding of DSLs via online partial evaluation. In *Proceedings of the International Conference on Generative
[24] R. Leißa, K. Boesche, S. Hack, A. Pérard-Gayot, R. Membarth, P. Slusallek, A. Müller, and B. Schmidt. 2018. AnyDSL: A partial evaluation framework for programming high-performance libraries. *Proceedings of the ACM on Programming Languages (PACMPL)*, 2, OOPSLA, (November 4–9, 2018), 119:1–119:30. DOI: 10.1145/3276489.

[25] Y. Liu, Y. Li, Z. Qi, and H. Guan. 2019. A scala based framework for developing acceleration systems with FPGAs. *Journal of Systems Architecture*, 98, 231–242. DOI: 10.1016/j.sysarc.2019.08.001.

[26] G. Martin and G. Smith. 2009. High-level synthesis: Past, present, and future. *IEEE Design & Test of Computers*, 26, 4, 18–25. DOI: 10.1109/MDT.2009.83.

[27] P. Milder, F. Franchetti, J. C. Hoe, and M. Püschel. 2012. Computer generation of hardware for linear digital signal processing transforms. *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, 17, 2, 15:1–15:33. DOI: 10.1145/2159542.2159547.

[28] R. Nane, V.-M. Sima, C. Pilato, J. Choi, B. Fort, A. Canis, Y. T. Chen, H. Hsiao, S. Brown, F. Ferrandi, et al. 2015. A survey and evaluation of FPGA high-level synthesis tools. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 35, 10, 1591–1604. DOI: 10.1109/TCAD.2015.2513673.

[29] G. Ofenbeck, T. Rompf, A. Stojanov, M. Odersky, and M. Püschel. 2013. Spiral in Scala: Towards the systematic construction of generators for performance libraries. In *Proceedings of the International Conference on Generative Programming: Concepts & Experiences (GPCE)*. ACM, (October 27–28, 2013), 125–134. DOI: 10.1145/2517208.2517228.

[30] M. A. Özkan, A. Pérard-Gayot, R. Membarth, P. Slusallek, J. Teich, and F. Hannig. 2018. A journey into DSL design using generative programming: FPGA mapping of image border handling through refinement. In *Proceedings of the 5th International Workshop on FPGAs for Software Programmers (FSP)*. VDE.

[31] M. A. Özkan, O. Reiche, F. Hannig, and J. Teich. 2017. A highly efficient and comprehensive image processing library for C++-based high-level synthesis. In *Proceedings of the 4th International Workshop on FPGAs for Software Programmers (FSP)*. VDE.

[32] M. A. Özkan, O. Reiche, F. Hannig, and J. Teich. 2016. FPGA-based accelerator design from a domain-specific language. In *Proceedings of the 26th International Conference on Field-Programmable Logic and Applications (FPL)*. IEEE, (August 29–September 2, 2016), 9 pages. DOI: 10.1109/FPL.2016.7577357.

[33] M. A. Özkan, O. Reiche, F. Hannig, and J. Teich. 2017. Hardware design and analysis of efficient loop coarsening and border handling for image processing. In *Proceedings of the International Conference on Application-specific Systems, Architectures and Processors (ASAP)*. IEEE, (July 10–12, 2017), 155–163. ISBN: 978-1-5090-4825-0. DOI: 10.1109/ASAP.2017.7995273.

[34] L.-N. Pouchet, P. Zhang, P. Sadayappan, and J. Cong. 2013. Polyhedral-based data reuse optimization for configurable computing. In *Proceedings of the ACM/SIGDA international symposium on Field programmable gate arrays*. ACM, 29–38. DOI: 10.1145/2435264.2435273.

[35] J. Pu, S. Bell, X. Yang, J. Setter, S. Richardson, J. Ragan-Kelley, and M. Horowitz. 2017. Programming heterogeneous systems from an image processing DSL. *ACM Transactions on Architecture and Code Optimization (TACO)*, 14, 3, 26:1–26:25. DOI: 10.1145/3107953.

[36] J. Ragan-Kelley, C. Barnes, A. Adams, S. Paris, F. Durand, and S. Amarasinghe. 2013. Halide: A language and compiler for optimizing parallelism, locality, and recomputation in image processing pipelines. In *Proceedings of the Conference on Programming Language Design and Implementation (PLDI)*. ACM, (June 16–19, 2013), 519–530. DOI: 10.1145/2491956.2462176.
[37] O. Reiche, M. A. Özkan, R. Membarth, J. Teich, and F. Hannig. 2017. Generating FPGA-based image processing accelerators with Hipacc. In Proceedings of the International Conference On Computer Aided Design (ICCAD). IEEE, (November 13–16, 2017), 1026–1033. ISBN: 978-1-5386-3094-5. DOI: 10.1109/ICCAD.2017.8203894.

[38] D. Richmond, A. Althoff, and R. Kastner. 2018. Synthesizable higher-order functions for C++. Transactions on Computer-Aided Design of Integrated Circuits and Systems, 37, 11, 2835–2844.

[39] J. Sanguinetti. 2006. A different view: Hardware synthesis from SystemC is a maturing technology. IEEE Design & Test of Computers, 23, 5, 387–387. DOI: 10.1109/MDT.2006.111.

[40] M. Schmid, O. Reiche, F. Hannig, and J. Teich. 2015. Loop coarsening in C-based high-level synthesis. In Proceedings of the 26th Annual IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP). IEEE, 166–173.

[41] J. S. da Silva, F.-R. Boyer, and J. P. Langlois. 2019. Module-per-object: a human-driven methodology for C++-based high-level synthesis design. In 27th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM). IEEE, 218–226.

[42] R. Stewart, G. Michaelson, D. Bhowmik, P. Garcia, and A. Wallace. 2016. A dataflow IR for memory efficient RIPL compilation to FPGAs. In Proceedings of the International Conference on Algorithms and Architectures for Parallel Processing (ICA3PP). Springer, (December 14–16, 2016), 174–188. DOI: 10.1007/978-3-319-49956-7_14.

[43] G. Stitt, A. Gupta, M. N. Emas, D. Wilson, and A. Baylis. 2018. Scalable window generation for the Intel Broadwell+Arria 10 and high-bandwidth FPGA systems. In Proceedings of the ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA). ACM, (February 25–27, 2018), 173–182. DOI: 10.1145/3174243.3174262.

[44] T. L. Veldhuizen. 1998. C++ templates as partial evaluation. The Computing Research Repository (CoRR), (November 2, 1998). arXiv: cs/9810010 [cs.PL].

[45] Xilinx. 2017. Vivado Design Suite user guide high-level synthesis UG902. (2017).

A APPENDIX

A.1 Finite State Machine Constructor

```rust
fn @ make_fsm() -> FSM {
    let mut states : fn(State) => State = @ |cur| cur;
    FSM {
        add: @ |name, action, next| {
            let old = states;
            states = @ |cur: State| {
                if name == cur {
                    action();
                    next();
                } else {
                    old(cur)
                }
            }
        },
        run: @ |init| {
            let mut cur : State = init;
            let old = states;
            while true {
                match old(cur) {
                    Exit => break(),
                    label => cur = label,
                }
            }
        },
        run_pipelined: @ |init, ii, beg, end| {
            let loop = if ii == 0 {
                @ |beg, end| range(beg, end)
            } else {
                @ |beg, end| pipeline(ii, beg, end)
            }
        }
    }
}
```
let mut cur : State = init;
let old = states;
for i in loop(beg, end) {
  match old(cur) {
    Exit => break(),
    label => cur = label,
  }
}

A.2 Description of Point Operator using FSM

type PointOp = fn(Mem1D) -> Mem1D;
fn make_point_op(v: int, op: Op) -> PointOp {
  @ |img, out| {
    let mut idx = 0;
    let fsm = make_fsm();
    fsm.add(1, || img.update(idx), || 2);
    fsm.add(2, || {
      for i in unroll(0, v) {
        out.write(i, op(img.read(i)));
      }
    }, || 3);
    fsm.add(3, || {
      out.update(idx);
      idx++;
    }, || 1);
    // start at 1, use ii of 1
    fsm.run_pipelined(1, 1, 0, img.size);
  }
}