Improved Ferroelectric Performance of Mg-Doped LiNbO$_3$ Films by an Ideal Atomic Layer Deposited Al$_2$O$_3$ Tunnel Switch Layer

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Abstract

Bilayer structures composed of 5% Mg-doped LiNbO$_3$ single-crystal films and ultrathin Al$_2$O$_3$ layers with thickness ranging from 2 to 6 nm have been fabricated by using ion slicing technique combined with atomic layer deposition method. The transient domain switching current measurement results reveal that the P-V loops are symmetry in type II mode with single voltage pulse per cycle, which may be attributed to the built-in electric field formed by asymmetric electrodes and compensation of an internal imprint field. Besides, the inlaid Al$_2$O$_3$, as an ideal tunnel switch layer, turns on during ferroelectric switching, but closes during the post-switching or non-switching under the applied pulse voltage. The Al$_2$O$_3$ layer blocks the adverse effects such as by-electrode charge injection and improves the fatigue endurance properties of Mg-doped LiNbO$_3$ ferroelectric capacitors. This study provides a possible way to improve the reliability properties of ferroelectric devices in the non-volatile memory application.

Keywords: Tunnel switch, Mg-doped LiNbO$_3$, Atomic layer deposition, Ion slicing, Ferroelectric memory

Background

Lithium niobate (LN) single-crystal films, due to their excellent physical properties, [1–6] have been widely used in surface acoustic wave oscillators, electro-optic modulators, and data storage based on the domain switching. Recently, wafer-scale lithium niobate-on-insulator (LNOI), which has great potential application for high-density integrated circuits in electro-optic, acousto-optic, and data storage devices, is fabricated by an ion implantation and wafer bonding technology. This technology allows for a wide variety of substrates, such as LN, silicon, and even the CMOS circuit [3, 7–9]. However, the imprint hysteresis loop originated from preferred orientations and the poor fatigue endurance of LN films, due to by-electrode charge injection, destabilize the retention of polarization reversal, which limits their application in non-volatile memory devices [10–13]. The preferred orientations related to interfacial passive layers formed between ferroelectric layers and electrodes, which can induce a strong depolarization field in the opposite direction of polarization. It can drive out the injected charges after the removal of the applied voltage or during intermittent time of the sequent pulse stressing [11, 12]. On the other hand, because of the presence of interfacial passive layers, the fatigue endurance of LN films will be improved by blocking the charge injection from by-electrode after ferroelectric switching. However, the fatigue process accelerates if the time of the applied pulse periodicity is shortened below 0.5 s. This is described by the interfacial passive layers contribution of the accumulative space charge at certain frequencies [11]. It is reported that an inlaid Al$_2$O$_3$ dielectric film can play as a tunnel switch in the dielectric/ferroelectric bilayer capacitor, for example, in Al$_2$O$_3$/Pb (Zr,Ti)O$_3$, and Al$_2$O$_3$/Mn-doped BiFeO$_3$ bilayer structures [14–16]. The Al$_2$O$_3$ tunnel switch turns on as a conductor during polarization switching, but switches off as an insulator to block the by-electrode charge injection after completed polarization switching or no switching operation [14]. Therefore, it can prevent the unwanted injected charges and polarization backswitching, and then improve the reliability of dielectric/ferroelectric bilayer capacitor.
In this paper, we fabricated 200-nm-thickness Z-cut 5% Mg-doped congruent LN single-crystal thin films and then deposited ultrathin Al₂O₃ layers with various thicknesses (2–6 nm) on LN to form bilayer capacitor structures. The Al₂O₃ films as tunnel switch layers can improve the fatigue endurance. Asymmetric electrodes (Au/Pt electrodes) are designed to form a built-in electric field against the depolarization field induced by the interfacial passive layers. The electrical results exhibit the symmetrisation of hysteresis loop transferred from the domain switching current transients with time. Meanwhile, it also proves that the inlaid Al₂O₃ layer plays as a tunnel switch layer, which can turn up during the ferroelectric switching and close after completed polarization switching or no switching operation.

Methods
The Z-cut 5% Mg-doped congruent LiNbO₃ (LN) single-crystal thin films were peeled off from their bulk crystals by using an ionic implantation and wafer bonding technology, as described elsewhere [10, 11, 17, 18]. In detail, the surface layer of a LN bulk crystal was first implanted with He ions in desired depth by controlling the implantation energy and the dose of injected ions, and then 5 nm Cr adhesion layer and 100 nm Pt bottom electrode layer are deposited by DC sputtering (K. J. Lesker PVD-75). The surface layer was bonded to another LN substrate covered with 1-μm-thick SiO₂ buffer layer and sliced off. The thickness of LN film is controlled to about 200 nm by chemical mechanical polishing. Subsequently, ultrathin Al₂O₃ films with thicknesses (d) of 2–6 nm were deposited by ALD (TFS-200, Beneq, Finland). In detail, the precursor gases are diethyl zinc and de-ionized water. They were pulsed alternately into the reaction chamber with a pulse time of 50 ms and separated by purging steps using argon for 2 s at the reaction temperature of 200 °C [19]. Finally, top Au square electrodes with areas of 1.0 × 10⁻⁴ cm² were deposited through a metal shallow mask.

The thicknesses of Al₂O₃ layers deposited on the Si wafer as contrast were measured by a spectroscopic ellipsometry system (GES-5E, SOPRA, Courbevoie, France). The film structure was analyzed by the X-ray diffraction (XRD) (Bruker D8 Advance) in a θ-2θ scanning mode with Cu Kα radiation as well as cross-sectional scanning electron microscopy (SEM, Sigma HD, Zeiss). To study the domain switching dynamics, several square pulses with a rising time of 10 ns were applied to top electrodes by using a single-channel Agilent 8114A pulse generator, where bottom electrodes were grounded. In the circuit, the domain switching current (Iₜₗₜ) across in-series internal resistors of all instruments with the total resistance was monitored using a LeCroy HDO6054 oscilloscope. The values of both output resistance of the pulse generator Rᵦ and the input resistance of the oscilloscope Rᵦᵦ are 50 Ω, respectively.

Results and Discussion
Figure 1a shows the XRD result of the LN thin film on a Pt/Cr/SiO₂/LN substrate. The film has strong (00 1) reflections indexed in the rhombohedral phase symmetry. In addition, there are also some diffraction peaks of Pt and Cr films marked in Fig. 1a. The absence of any other peaks confirms the high crystallinity of the LN film without phase impurity. The cross-sectional SEM image of the sample shown in Fig. 1b demonstrates the clear interface structure with LN, Pt, Cr, and SiO₂ stacking layers.

In order to study the domain switching kinetic mechanism, two types of pulse voltage modes are designed as clearly shown in Fig. 2a and b [11]. Type I is configured as double pulses in opposite polarities with the time interval of 5 s. The first pulse is applied to switch the upward polarization state pointing to the top electrode and the second one can switch the downward polarization. However, limited by programming time of a single-channel pulse generation, the minimum time interval is too long.
to catch the domain switching current transient invoked by the second pulse, due to the preferred domain orientation. To catch the domain switching current transient, a single pulse overlapping a negative baseline DC bias is proposed in type II, where the initial negative DC bias can switch the upward polarization state and the positive pulse sets the domain downward. Here, the width of the two type pulses is set to 1 μs.

Figure 2c and d show the domain switching current transients versus time (t) of Au/LN/Pt structure sample under various applied voltages (V) in type I and type II modes, respectively. The plateaus of domain switching current transients are observed that narrow in width but increase in height with V increasing after the initial capacitor charging current at 30 ns. The height of plateau in two modes both shows a linear relationship with the increase of V and the results are summarized in the insets by the solid-line fitting of the data [11, 13]. The coercive voltage (V_c) value in the two modes can be derived to about 24.7 V from the line interception with the voltage axis. After the termination of the switching pulse, the capacitor discharging current occurs after 1 μs, which suggests that the preferred domain orientation is the upward polarization state pointing to the top electrode.

P-V hysteresis loops under different applied voltages in two type modes can be transferred directly from the corresponding domain switching current transients in Fig. 2c and d, and the results are shown in Fig. 2e and f.
respectively [11, 20]. A determined forward coercive voltage of about 25 V invariable with V is obtained in the two types pulses. The coercive voltage approaches to $V_C$ extracted from the linear $I_{sw}-V$ plot in the inset of Fig. 2c and d. Unlike the non-doped LN film, the $V_C$ is variable and the value is equal to the maximum applied voltages [10]. For the 5% Mg-doped LN, the defined $V_C$ is invariable with $V$, as shown in Fig. 2e and f. This is because the Mg dopant can generate Li-site metal vacancies and oxygen vacancy-related defects, [21–23] which can trap space charges and effectively shorten the resistance degradation time across the interfacial layers between the film and top/bottom electrodes [11]. Therefore, domain switching currents overlap with capacitor charging currents in acceleration of domain switching speed with a definite $V_C$, as shown in Fig. 2c and d. However, limited by the pulse generator, the output baseline voltage in type II mode cannot be shift symmetrically when increasing applied pulse voltage over 32 V. Compared to the imprinted loops along the positive voltage axis in Fig. 2e, the symmetrisation of the loops are achieved along the voltage axis in Fig. 2f, different from those in Pt/LiNbO$_3$/Pt structures where the $P-V$ hysteresis loops in either type I or type II are imprinted toward a positive voltage [11]. The reason of the symmetrical $P-V$ loops in Fig. 2f may be attributed to the designed asymmetric electrodes (here Au/Pt). The work function of Au electrode is 5.1 eV, which is slightly smaller than that of Pt (5.65 eV) [24]. There will induce a built-in electric field ($E_b$) with the direction pointing from the top electrode to the bottom electrode, shown in the inset of Fig. 2e. The depolarisation field ($E_d$) induced by the interfacial passive layers has the opposite direction to $E_b$. The $E_d$ can switch back the polarization in a very short time after the termination of the switching pulse in type II for the symmetrical electrodes (Pt/Pt) [11]. In our experiment, the $E_b$ can partially screen the $E_d$ and accumulate injected charges in compensation of an internal imprint field, [16] which can slow down the backswitching time. Hence, the switched domain can maintain and backswitching current transient will be captured by type II pulse. However, the time interval of the two pulses with opposite polarities in type I mode is too long. After the first pulse, the trapped injected charges by $E_d$ will be gradually driven out of the film by $E_d$ before the arrival of the second pulse in type I [11]. In order to prove the attribution of built-in electric field to the symmetrisation of the loops, Pt/LiNbO$_3$/Pt symmetrical structure sample was prepared and the imprinted loops along the positive voltage axis were transferred directly from the corresponding domain switching current transients in Additional file 1: Figure S1a at positive pulse with voltages/widths of 30–40 V/500 ns, shown in Additional file 1: Figure S1b.

Figure 3a and b show the domain switching current ($I_{sw}$) transients versus time ($t$) of LN and Al$_2$O$_3$ (6 nm)/LN samples under different applied voltage ($V$) in type I mode. After the plateau of domain switching, the switching current $I_{sw}$ decays and is given by: [13]

$$I_{sw} = I_{sw}^0 \exp \left( -\frac{t-t_0}{R_1C_1} \right) (t_0 \leq t \leq t_{sw})$$

(1)

where $t_0$, $t_{sw}$, $R_1$, and $C_1$ are the beginning time of domain switching, the completion time of domain switching, the total resistance of all the in-series resistors in the circuit, and the interfacial non-ferroelectric capacitance, respectively. This describes the charge trapping effect which can be modeled as an interfacial passive layer in series with an ideal ferroelectric layer. $I_{sw}^0$ is defined as switching current and is given by:

$$I_{sw}^0 = \frac{V-V_C}{R_1}$$

(2)

During domain switching, the voltage applied on the ferroelectric layer is fixed at the coercive voltage $V_C$, and the extra voltage ($V-V_C$) is applied to $R_L$. $R_L$ also included the circuit parasitic resistance ($R_P$) and contact resistance ($R_C$) between the film and electrodes; hence, $R_L = R_O + R_W + R_P + R_C$. The decayed part of the switching current transients versus time can be fitted by Eq. (1). The time constant $R_1C_1$ can be estimated from the slope of the fitted lines. Figure 3c shows $I_{sw}^0-V$ plots with different Al$_2$O$_3$ thicknesses. $R_1$ and $V_C$ were estimated from the slopes and the X-axis intercept of the linear fitted lines. It can be seen that the $V_C$ is increased linearly with increasing the Al$_2$O$_3$ thickness $d$, as shown in Fig. 3d. Here, the $C_1$ values were estimated as the error bounds at each $V$ in Fig. 3e [13]. The results show that $C_1$ value almost kept constant (1.4 ± 0.2) nF with increasing Al$_2$O$_3$ layer thickness from 0 to 6 nm.

In order to calculate $R_C$, the top and bottom electrodes are shorted, which can obtain the $R_P$ (~ 2 Ω) with different applied voltages, shown as the circuit calibration by the opened symbols in Fig. 3c. Therefore, the $R_C$ corresponding to $d$ is calculated and the result is showed in Fig. 3f. $R_C$ increases linearly from 3 ± 2.5 Ω at $d = 0$ to 55 ± 10 Ω at $d = 6$ nm. The almost $d$-independent large $C_1$ values suggest that the Al$_2$O$_3$ layer works as a series resistor during domain switching. This means that the Al$_2$O$_3$ tunnel switch was switched on during FE switching.

In order to obtain the total capacitance of the bilayer during FE nonswitching, the switching ($P_{sw}$) and non-switching ($P_{nsw}$) polarizations versus $V$ with $d$ increased from 0 to 6 nm under pulses in type I mode are measured and the result are showed in Fig. 4a. The purpose of choosing the type I pulse is to obtain the curve of $P_{nsw}-V$ when the direction of the applied voltage is
Fig. 3  a, b  $I_{sw,t}$ dependences in type I under different $V$ applied to the Al$_2$O$_3$/LN bilayer with the Al$_2$O$_3$ thickness $d = 0$ and 6 nm, respectively, fitted by a series of parallel dotted lines to Eq. (1). c The plateaus of domain switching current as a function of the applied voltage with different Al$_2$O$_3$ layer thicknesses, where the solid lines show the best fit of the data to Eq. (2). d The Al$_2$O$_3$-layer-thickness $d$ dependence of the coercive voltage ($V_c$) extracted from c. e, f The extracted interfacial capacitance $C_i$ and contact resistance $R_C$ as functions of the Al$_2$O$_3$ layer thickness $d$.

Fig. 4  a The switching ($P_{sw}$) and nonswitching ($P_{nsw}$) polarizations versus $V$ with $d$ increased from 0 to 6 nm under pulses in type I mode. b The Al$_2$O$_3$-layer-thickness $d$ dependence of $1/C_{tot}$ measured by an impedance analyzer at 100 kHz.
consistent with the polarization orientation, from which the total capacitance \( C_{\text{tot}} \) of the bilayer can be calculated from the relation, \( C_{\text{tot}} = SdP_{\text{new}}/dV \), where \( S \) is the electrode area. It can totally exclude the charge effects by FE switching in the type I pulse mode, but using the type II mode cannot achieve this effect with the negative switching polarization, which can switch back the polarization involved with the charges injection. The difference between \( P_{\text{sw}} \) and \( P_{\text{nsw}} \) is \( 2Pr \), as shown in Fig. 4a. It has small change with \( d \) from 0 to 6 nm, whereas the \( P_{\text{nsw}} \) (open symbols) signals are too weak to be monitored by an oscilloscope. To prove the \( \text{Al}_2\text{O}_3 \) tunnel switch layer working as a dielectric capacitor, the direct \( C_{\text{tot}} \) measurements using a low-frequency impedance analyzer at 100 kHz with no additional DC bias were carried out and their results are shown in Fig. 4b, which can be fitted by Eq. (3):

\[
\frac{1}{C_{\text{tot}}} = \frac{1}{C_f} + \frac{d}{\varepsilon_0 \varepsilon_{\text{Al}} S}
\]  

(3)

where \( \varepsilon_{\text{Al}} \) is the dielectric constant of the \( \text{Al}_2\text{O}_3 \) layer and \( \varepsilon_0 \) is the vacuum permittivity of free space. \( C_f \) and \( S \) represent the capacitance of the ferroelectric layer and the electrode area, respectively. Figure 4b shows the linear \( 1/C_{\text{tot}} \) versus \( d \) plot, which suggests that the \( \text{Al}_2\text{O}_3 \) layer becomes a highly insulating dielectric film under nonswitching situation or post-switching. It can be derived that \( C_f \approx 14 \text{ pF} \) and \( \varepsilon_{\text{Al}} \approx 7.9 \) from Eq. (3). Therefore, the interposed thin \( \text{Al}_2\text{O}_3 \) layer is proved as a dielectric capacitor. During FE nonswitching as well as after FE switching, the \( \text{Al}_2\text{O}_3 \) tunnel switch closes as an insulator.

Figures 5 show schematic diagrams of the \( \text{Al}_2\text{O}_3/\text{LN} \) bilayer structure switched in type I or type II mode. Figure 5a sketches the equivalent on-off circuit of the in-series resistors and capacitors for the \( \text{Al}_2\text{O}_3 \) tunnel switch. In the initial state, as shown in Fig. 5b, the preferred polarization orientation is the upward polarization state pointing to the top electrode. The built-in electric field induced by the asymmetric electrodes directs from Au electrode to Pt electrode. When applying the polarization voltage, the FE switching occurs. It is understood that the voltage is applied inversely proportional to the capacitance in the circuit. In \( \text{Al}_2\text{O}_3/\text{LN} \) bilayer structure, during the FE switching, the LN layer has a large capacitance. Therefore, most of the external applied voltage applies on the \( \text{Al}_2\text{O}_3 \) layer. Ultrathin \( \text{Al}_2\text{O}_3 \) layer is injected by electrode charge. It switches on as a resistor when the applied voltage exceeds the \( \text{Al}_2\text{O}_3 \) tunneling threshold, as shown in Fig. 5c. After the completion of FE switching or for the case of a nonswitching situation, the capacitance of LN layer is very small and the applied voltage on \( \text{Al}_2\text{O}_3 \) decreases lower than the tunneling threshold voltage. At this moment, the \( \text{Al}_2\text{O}_3 \) layer plays as an insulator and switches off, as shown in Fig. 5d.

Figure 6 shows the cycling number dependences of switched polarizations in \( \text{Al}_2\text{O}_3/\text{LN} \) bilayer structure with the thickness of \( \text{Al}_2\text{O}_3 \) ranging from 0 to 6 nm in type I mode. The width of pulses is 1000 ns with a periodicity of 0.5 s. It can be clearly seen that the fatigue endurance of the \( \text{Al}_2\text{O}_3/\text{LN} \) bilayer structure is improved gradually with increasing the \( \text{Al}_2\text{O}_3 \) thickness with over \( 10^4 \) cycles of pulse stressing. The fatigue property in type II mode is similar to the result in type I mode, which was showed in Additional file 1: Figure S2 of supporting.

![Fig. 5 Schematic diagrams of the Al2O3/LN bilayer structure switched in type I or type II. a The sketch of the equivalent on-off circuit of the in-series resistors and capacitors for the Al2O3 tunnel switch. b Initial preferred polarization orientation and built-in electric field; c The Al2O3 tunnel switch turning on and domain switching; d The Al2O3 tunnel switch switching off and polarization maintain](image-url)
information. Unfortunately, the electrical breakdown would occur easily in the type II mode after longtime DC voltage applied with near $10^4$ cycles of pulse stressing. The data can be fitted using the model for the coexistence of domain-wall pinning and depinning within each cycle, as shown by the solid lines in Fig. 6, where the fatigue physics was attributed to by-electrode charge injection [13]. When the Al$_2$O$_3$ layer inserted between the Au electrode and LN layer, it can block the by-electrode injection charge path and improve the fatigue endurance. However, in the bilayer structure, some issues should be further considered. For example, with increasing the thicknesses of Al$_2$O$_3$ from 0 to 6 nm, the coercive voltage enlarged from near 25 to 34 V, which can be reduced by improving the quality of the Al$_2$O$_3$ layer. Actually, a few atomic layers of Al$_2$O$_3$ with high quality or less defect can effectively block the charges injected by electrodes, which is confirmed elsewhere by optimizing atomic layer deposition processing conditions (such as temperature and time) [25].

Recently, ferroelectric domain-wall memories based on the erasable conducting charged domain walls and the non-destructive electrical read-out of the polarization states have been proposed in our following research work [26, 27]. Large conductivity of charged domain walls in lithium niobate single crystals is obtained after domain switching [28, 29]. Therefore, the thinner lithium niobate single crystal thin films on silicon substrates are the promising materials for integrated ferroelectric domain-wall memories and its retention and fatigue endurance properties can be improved by design of Al$_2$O$_3$/lithium niobate bilayer.

**Conclusions**

Two hundred nanometer LiNbO$_3$ single-crystal films with 5% Mg-doping were prepared by ion slicing of surface layers from bulk LN single crystals, and then the ultrathin Al$_2$O$_3$ films with thicknesses ranging from 2 to 6 nm as tunnel switch layers were deposited on 5% Mg-doped LN film to form bilayer structures by atomic layer deposition. The symmetrized $P-V$ hysteresis loops along the voltage axis are observed under applied pulse voltages in type II mode, which may be attributed to the built-in electric field induced by asymmetric electrodes in Au/LiNbO$_3$/Pt and compensation of the internal imprint field. The domain switching current ($I_{sw}$) transients and its transferred $P-V$ hysteresis loops reveal that the ultrathin Al$_2$O$_3$ layer plays as an idea tunnel switch. It turns on during FE switching, but closes during the nonswitching or after FE switching, minimizing the adverse interference with FE switching. Furthermore, the fatigue endurance of the FE capacitor is improved gradually with increasing the tunnel switch layer thicknesses from 2 to 6 nm. The Al$_2$O$_3$/LN bilayer structure paves the way to design robust ferroelectric devices in alleviating the fatigue problem by-electrode charge injection.
Additional file

Additional file 1: The imprinted P-V hysteresis loops of Pt/LiNbO$_3$/Pt symmetrical structure sample in type II mode and the fatigue property of Al$_2$O$_3$/LiNbO$_3$ bilayer structure in type II mode. (DOCX 144 kb)

Abbreviations
ALD: Atomic layer deposition; CMOS: Complementary metal oxide semiconductor; FE: Ferroelectric; LN: Lithium niobate; SEM: Scanning electron microscopy; XRD: X-ray diffraction

Acknowledgements
This work was supported by the National Natural Science Foundation of China (grant number 61674044), the Basic Research Project of Shanghai Science and Technology Innovation Action (grant number 17JC1400300), and the Program of Shanghai Subject Chief Scientist (grant number 17XD1400800).

Availability of Data and Materials
The datasets generated during and/or analyzed during the current study are available from the corresponding author on reasonable request.

Authors’ Contributions
YZ and QHR prepared the materials and draft the manuscript. AQJ, YZ, and JJ designed the work. YZ, XC, JGJ, and QHR carried out the structural analyses and switching current measurements of the samples. AQJ edited the whole manuscript. All authors had read and approved the final manuscript.

Competing Interests
The authors declare that they have no competing interests.

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Received: 28 January 2019 Accepted: 3 April 2019
Published online: 16 April 2019

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