1. Introduction

The overall interchip bandwidth in central processing units (CPUs) used for high-end servers is expected to reach the 10-Tbit/s level by the late 2010s. Multi-core CPUs, 3D-memories, and 3D solid state drives are expected to be integrated on a silicon optical interposer that will support high-bandwidth optical interconnects among the components in an on-chip server targeted for development in the 2020s.[1] Optical interconnection using silicon photonics is a promising solution to the problem of bandwidth bottleneck among LSI chips because of the intrinsic properties of optical signals and the compatibility with complementary metal oxide semiconductor process technology. We previously proposed a photonics-electronics convergence system in which a continuous wave (CW) light source, optical modulators, and photodetectors are linked by silicon optical waveguides on a silicon interposer and LSI chips are mounted and electrically connected to the optical modulators and photodetectors.[2–4] In this system, the integrated CW light source must be multi-channel, and have high density and high power. An over-1,000-channel light source is required to reach a bandwidth of around 10-Tbit/s, if 10 Gbit/s per channel is assumed. We previously developed a hybrid integrated light source with a laser diode array on a silicon optical waveguide platform,[5] demonstrated a light source with over 100 output ports in which the number of output ports is increased by using a waveguide splitter and multichip bonding[6] and estimated the power uniformity of the output ports.[7] More recently, we demonstrated a hybrid integrated light source with over 1,000 channels.[8, 9]

In this paper, we present a multi-channel hybrid integrated light source for ultra-high-bandwidth optical interconnections. In section 2, we describe its hybrid integration structure and fabrication technology. In section 3, we describe its optimization to reduce power consumption based on consideration of the thermal interference between the channels in a laser diode (LD) array and also...
between LD array chips. A 1,000-channel integrated light source based on this optimized structure is described in Section 4. Then, the key points are summarized and a potential application is mentioned in Section 5.

2. Hybrid Integration Structure and Fabrication

The hybrid integrated light source with an LD array on a silicon optical waveguide platform is shown in Fig. 1. Each LD in the array is a Fabry-Perot (FP) LD with a spot-size converter (SSC) including an inverse taper at the waveguide facet side and has a structure consisting of InGaAsP base strained multiple-quantum-well buried heterostructure at lasing wavelength of about 1.55 μm.[7] The LD array chip is 600 μm wide and 400 μm long. The LD array has 13-, 19-, and 25-channel stripes with 30-, 20-, and 15-μm pitches, respectively, and has alignment marks. The stripe pitch can be drastically reduced by using a single electrode compared with the wide stripe pitch used in a conventional LD array. The operating current is injected into these stripes through a single electrode, and the LD array simultaneously outputs optical signal.

The platform consists of silicon optical waveguides with SSCs and an LD mounting stage. The core section of the silicon waveguide is 440 nm wide and 220 nm high. The tip width and length of the tapered waveguide are 150 nm and 200 μm, respectively. The waveguides include a 0.5-μm-thick SiOx slab layer with a refractive index of 1.52, a 1.7-μm-thick upper cladding layer with a refractive index of 1.46, and a 3-μm-thick lower cladding layer. The core layer and lower cladding layer correspond to the silicon on insulator (SOI) layer and the buried oxide (BOX) layer on the SOI substrate, respectively. The LD mounting stage has silicon alignment marks and silicon pedestals that were formed by dry etching after fabricating the waveguide facet and removing the BOX layer from the mounting area. An electrode was then formed on the silicon substrate. Figure 2 shows a scanning electron microscope image of a waveguide facet made by dry etching. The measured angle of the facet was ~85°.

The SiOx slab layer in the upper cladding layer stabilizes the spot-size of the converter with optical confinement in the vertical direction against SSC tip width variation.[10] The optical coupling loss between the LD and SSC with and without the slab layer was measured for different Si taper tip widths. As shown in Fig. 3, the loss with a conventional inverse taper SSC increased when the tip width was reduced from 180 nm. In contrast, the loss with SiOx slab layer SSC was almost constant when the width was between 100 nm and 180 nm at the range of 100 nm. The optical coupling tolerance between the FP-LD and the SSC (tip width: 160 nm) was measured in the horizontal and...
vertical directions. As shown in Fig. 4, the loss was 2.6 dB at zero deviation. The 1-dB loss tolerances of the slab layer SSC were \( \pm 1.2 \) \( \mu m \) in the horizontal direction and \( \pm 0.9 \) \( \mu m \) in the vertical direction, although those of the conventional SSC (tip width: 170 nm) were \( \pm 0.9 \) \( \mu m \) in the horizontal direction and \( \pm 0.8 \) \( \mu m \) in the vertical direction. Therefore, the slab layer SSC enables the fabrication margin of the tip width to be drastically increased and enables the use of a simple fabrication technique without etching.

The LD arrays are mounted on the platform with AuSn solder bumps by flip-chip bonding.[7] We adapted the visual alignment between the alignment marks on the LD array and mounting stage by infrared transmission for horizontal positioning. The vertical alignment of the LD array was precisely adjusted by the positioning of the silicon pedestals by fabrication. Since AuSn bumps were crimped to the electrode on the platform and a load was held on the flip-chipped LD array chip toward the platform from the bottom of the LD array substrate, the LD chip was prevented from rotating while heating AuSn solder. As a result, the horizontal accuracy was better than \( \pm 0.5 \) \( \mu m \) by visual alignment and the vertical accuracy was better than \( \pm 0.1 \) \( \mu m \) by fabrication controllability. In this way, those accuracies were within the 1 dB tolerances of the spot-size converter.

### 3. Structural Optimization for Low Power Consumption by Considering Thermal Interference between LD Arrays

The hybrid integrated light source with a single channel LD and a waveguide splitter was previously estimated in the viewpoint of wall plug efficiency (WPE) for low power consumption.[11] While the number of output ports of a light source with multiple LD arrays has been expanding, one of the most important goals in the light source is to reduce the temperature increase caused by the thermal interference of multiple LD arrays. There are two types of interference in the hybrid integration of LD arrays fabricated by multichip bonding. One is thermal interference between the channels in an LD array chip, and the other is that between the LD array chips. To obtain the maximum WPE, both the number of LD array channels and the number of LD array chips mounted were optimized by considering these thermal interferences.

A schematic of our multi-channel hybrid integrated light source with waveguide splitters and multiple LD array chips is shown in Fig. 5, where \( n \) is the number of LD array channels, \( N \) is the number of output ports per LD array, \( M \) is the number of LD array chips, and \( P_{\text{out}} \) is the optical output power at each port. The total number of output ports is \( M \times N \). The platform mainly used for thermal simulation was 9,700 \( \mu m \) wide and 1,300 \( \mu m \) long, and the
LD array is the same size described in Sec. 2. Increasing the number of LD array channels reduces the channel pitch. Increasing the number of LD chips reduces the chip pitch. In this section, we describe a temperature dependence of the LD performance, thermal analysis of the multichannel hybrid integrated light source using the finite element method, and structural optimization from the viewpoint of WPE.

3.1 Temperature dependence of LD performance

The threshold current and differential efficiency of a MQW FP-LD with an increasing temperature can be characterized using an overall characteristic temperature ($T_0$) and an above threshold characteristic temperature ($T_1$),\(^{12}\) as defined in (1) and (2), respectively, where $I_0$ and $I_{\text{PO}}$ are fitting parameters.

\[
I_{\text{th}} = I_0 e^{T/T_0} \quad (1)
\]
\[
I - I_{\text{th}} = I_{\text{PO}} e^{T/T_1} \quad (2)
\]

These characteristic temperatures were extracted by measuring a set of single-sided light output vs. injection current (L-I) characteristics of a laser diode mounted on silicon platform at temperature range from 25, 50, and 75°C, as shown in Fig. 6(a). Equation (1) was used to extract $T_0$ and $I_0$ by fitting the natural log of threshold current vs. the temperature. The results, shown in Fig. 6(b), gave an overall characteristic temperature of 50°C, and an $I_0$ of 6.6 mA. Fitting the difference in current between threshold and that required for 1 mW of output power enables this characteristic temperature to be determined. The results, shown in Fig. 6(c), gave an above threshold characteristic temperature of 204°C with an $I_{\text{PO}}$ of 2.6 mA.

3.2 Thermal interference between channels in LD array chip

Figure 7 shows the dimensions of the light source and the LD array used in the finite element thermal model (1/2 scale model) (unit: μm).
was set to 20°C as a thermal boundary condition. Using this model, we calculated the thermal interference between channels in an LD array chip. As shown in Fig. 9, the thermal resistance of the central channel increased with the number of channels. Figure 10 shows the calculated temperature distribution around a mounted 25-ch LD array at a current of 80 mA/ch, and Fig. 11 shows the calculated temperature increase in the 25-ch array for various operating currents for each channel. The temperature for each channel increased while the operation current increased. In addition, the temperature increase for the central channel (channel 13) was slightly higher than that of the outer channels because of the heat generated from both sides. The temperature increase for the central channel with the number of LD array channels is shown in Fig. 12.

The number of the channels is 1 in Fig. 9 corresponds to the single channel LD. The thermal resistance of hybrid silicon laser at the cavity length of 850 μm was reported as 41.8°C/W experimentally and 43.5°C/W in thermal analysis.[12] On the other hand, the thermal resistance of a hybrid integrated light source was 34.4°C/W at the cavity length of 400 μm corresponding to 16.7°C/W at the cavity length of 850 μm.[13] By measuring the temperature and applied electrical power dependence of the lasing wavelength, the thermal resistance was estimated as 37.4°C/W at the cavity length of 400 μm. Since the LD mounting stage was formed by removal of the BOX layer, the thermal resistance was lower than that of the hybrid silicon laser with existence of the BOX layer.

3.3 Thermal interference between discrete LD array chips

The dimensions of the multiple LD arrays and light source used in the finite element thermal model (full-scale 3D model) are shown in Fig. 13. A mesh structure in the case of light source with five LD array chips and mesh structures of the LD array chip and the segment of LD array corresponding to LD facet are shown in Fig. 14. The boundary condition was same condition in Sec. 3.2. Using the thermal model, we calculated the thermal interference between LD array chips. Figure 15 shows the temperature distribution for 3-, 5-, 8-, and 10-chip 25-ch LD arrays with LD chip pitches of 3.2, 1.8, 1.2, and 0.9 mm, respectively. Figure 16 shows the dependence of the thermal resistance of the central channel on the number of the array chips which was normalized by the resistance of one array chip. The thermal interference was relatively low, because the
Fig. 13 Dimensions of (a) light source with multiple LD arrays, (b) segment of light source corresponding to discrete LD array, and (c) LD array used in finite element thermal model (full-scale 3D model) (unit: μm).

Fig. 14 Mesh structures of (a) light source with 5 LD array chips, (b) LD array, and (c) segment of LD array corresponding to LD facet used in Fig. 13.

Fig. 15 Temperature distribution in light source at 80 mA/ch for 25 ch-LD array chips: (a) 3, (b) 5, (c) 8, and (d) 10 chips.
spacing between chips was not quite small.

3.4 Wall plug efficiency

We optimized the structure of the light source from the viewpoint of WPE by considering how the light output vs. current (L-I) characteristics are affected by those thermal interferences and the efficiency of coupling to the silicon waveguide, as formulated in (3),[12] the optical output in each port $P_{out}$, as formulated in (4), and the electrical power dissipation $w$, as formulated in (5), for a light source with $N$ output ports divided by splitters from $n$-channel LD array at silicon backside temperature $T$.

$$P_0 = \frac{\eta_0}{\eta} \left( \frac{h\nu}{q} \right) e^{-\left( \frac{1}{k_1} \right) \left( T_0 + i_0 \right)}$$

(3)

$$P_{out} = C_{loss} \cdot \frac{N}{P_0}$$

(4)

$$w = V_0 \cdot I + R_s \cdot I^2$$

(5)

In these equations, $P_0$ is the optical output power in each LD array channel, and $R_T$ is the thermal resistance. $T_0$ and $T_1$ are the overall characteristic temperature and the above threshold characteristic temperature, as described in Sec. 3.1, $i$ and $i_0$ are the operation current and the fitting parameter, $C_{loss}$ is the total optical loss including coupling loss between an LD array and a waveguide facet, $V_0$ is LD turn-on voltage, and $R_s$ is series electrical resistance.

From (4) and (5), the WPE of the light source is given by

$$WPE = \frac{1}{\sum \frac{N}{P_{out}}} \sum \frac{N}{P_{out}} w.$$  

(6)

The WPE was calculated when $P_{out}$ was 1 mW, which is assumed as the standard required output power for an optical link. The results are shown in Fig. 17. The total number of output ports was defined as the product of the number of LD array chips $M$ and the number of output ports $N$. When the number of LD array channels $n$ was reduced, the number of splitters was increased and the operation current in each channel increased. Therefore, electrical power dissipation $w$ increased. When the number of array channels $n$ was increased, the temperature in the array increased due to the thermal interference between each channel in the array and the operation current in each channel was increased to maintain the level of output power at each port $P_{out}$. Therefore, electrical power dissipation $w$ increased. The WPE had a maximum value, depending on the number of LD array channels. Although the thermal interference between chips was low, the number of LD array chips $M$ is not expected to be large from the viewpoint of practical LD mounting.

As shown in Fig. 17, for example, the WPE for 5 chips $\times$ 200 output ports decreased slightly when the number of LD arrays exceeded 10. One optimum solution for operating a 25-ch LD array with 1,000 output ports is thus to combine 5-chip LD arrays and $1 \times 8$ splitters.

4. Demonstration of 1,000-channel Hybrid Integrated Light Source

On the basis of the structural optimization described above, we fabricated a light source with 1,000 output ports in which the silicon optical waveguides were split into eight waveguides by using cascaded $1 \times 4$ and $1 \times 2$ multimode interferometer splitters and in which five LD array chips were mounted on a silicon waveguide platform by multi-chip bonding (Fig. 18). The size of the light source was $9,700 \mu m \times 1,250 \mu m$. The LD array chip was $600 \mu m$ wide and $400 \mu m$ long. The pitch of the 25-ch LD array was $15 \mu m$. The pitch of the output ports was set to $9 \mu m$ in order to include 1,000 ports in 1 cm, corresponding to the stepper shot size.

The near-field pattern of the light source at an operation...
current of 1 A at each chip is shown in Fig. 19. 1,000 optical outputs were observed. A light source with 1,000 output ports corresponds to a 10^4 Tbit/s transmitter, assuming 10 Gbit/s for each port. We expect this multi-channel hybrid integrated light source to be easily adaptable to a photonics-electronics convergence system for ultra-high-bandwidth interchip interconnections.

5. Conclusion

We have developed a multi-channel hybrid integrated light source using a novel spot-size converter with a SiO_x slab layer. It has a wide fabrication margin and output ports with high power uniformity. The configuration of the light source was optimized to reduce power consumption by considering the thermal interference between the channels in an LD array and also between the LD array chips. On the basis of the optimization, we demonstrated a 1,000-channel light source based on this optimization had an optical interconnection with a bandwidth of over 10 Tbit/s. This hybrid integrated light source is expected to be easily adaptable to a photonics-electronics convergence system for ultra-high-bandwidth interchip interconnections.

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