Structural Synthesis for GXW Specifications

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Abstract. We define the GXW fragment of linear temporal logic (LTL) as the basis for synthesizing embedded control software for safety-critical applications. Since GXW includes the use of a weak-until operator we are able to specify a number of diverse programmable logic control (PLC) problems, which we have compiled from industrial training sets. For GXW controller specifications, we develop a novel approach for synthesizing a set of synchronously communicating actor-based controllers. This synthesis algorithm proceeds by means of recursing over the structure of GXW specifications, and generates a set of dedicated and synchronously communicating sub-controllers according to the formula structure. In a subsequent step, 2QBF constraint solving identifies and tries to resolve potential conflicts between individual GXW specifications. This structural approach to GXW synthesis supports traceability between requirements and the generated control code as mandated by certification regimes for safety-critical software. Synthesis for GXW specifications is in PSPACE compared to 2EXPTIME-completeness of full-fledged LTL synthesis. Indeed our experimental results suggest that GXW synthesis scales well to industrial-sized control synthesis problems with 20 input and output ports and beyond.

1 Introduction

Embedded control software in the manufacturing and processing industries is usually developed using specialized programming languages such as ladder diagrams or other IEC 61131-3 defined languages. Programming in these rather low-level languages is not only error-prone but also time- and resource-intensive. Therefore we are addressing the problem of correct-by-construction and automated generation of embedded control software from high-level requirements, which are expressed in a suitable fragment of linear temporal logic.

Moreover, an explicit correspondence between the high-level requirements and the generated control code is essential, since embedded control software is usually an integral part of safety-critical systems such as supervisory control and data acquisition (SCADA) systems for controlling critical machinery or infrastructure. In particular current industrial standards for safety-related development such as IEC 61508, DO 178C for avionics, and ISO 26262 for automotive applications mandate traceability between the control code and it requirements. Controllers generated by state-of-the-art LTL synthesis algorithms and tools such as generalized reactivity(1) (GR(1)) [15,25] or bounded LTL synthesis [8,11,28], however, usually do not explicitly support such traceability requirements. For example, the GR(1) synthesis tool Anzu generates circuit descriptions in Verilog from BDDs [15].

We are therefore proposing a novel approach for synthesizing structured control software. In essence, the control code is generated by means of structural recursion on the given LTL formulas. Therefore, the structure of the control code corresponds closely to the syntactic structure of the given requirements, and there is a direct correspondence between controller components and sub-formulas of the specification.

In a first step towards this goal, we identify a fragment of LTL for specifying the input-output behavior of typical embedded control components. Besides the specification of input assumptions, invariance conditions on outputs, and transition-like reactions of the form $G(input \rightarrow X^i output)$, this fragment also contains specifications of reactions of the form $G(input \rightarrow X^i(output \text{ release}))$, where input is an LTL formula containing at most $i$ consecutive X operators (i.e., an LTL formula whose validity is determined by the next $i$ input valuations). The latter reaction formula states that if there is a temporal input event satisfying the constraint input, then the output constraint should hold on output events until there is a release event (or output always holds). The operator
**G** is the universal path quantifier, **X**\(^i\) abbreviates \(i\) consecutive next-steps, \(W\) denotes the weak until temporal operator, the constraint output contains no temporal operator, and the subformula release may contain certain numbers of consecutive next-steps but no other temporal operators. The resulting fragment of LTL is called GXW.

So far we have successfully modelled more than 70 different embedded control scenarios in GXW. The main source for this set of benchmarking problems are publicly available collections of industrial training materials for PLCs (including CODESYS 3.0 and AC500) [210-231]. The proposed GXW fragment of LTL is also similar to established requirements templates for specifying embedded control software in the aerospace domain, such as EARS [23].

Previous work on LTL synthesis (e.g., [211-228, 223, 237, 231-232]) usually generates gate-level descriptions for the synthesized control strategies. In contrast, we generate control software in an actor language with high-level behavioral constructs and synchronous dataflow communication between connected actors. This choice of generating structured controllers is motivated by current practice of programming controllers using, say, Matlab Simulink [4], continuous function charts (IEC 61131-3), and Ptolemy II [12], which also supports synchronous dataflow (SDF) models [19]. Notice, however, that the usual notions of LTL synthesis also apply to synthesis for SDF, since the composition of actors in SDF may also be viewed as Mealy machines with synchronous cycles [30].

Synthesis of structured controllers from GXW specifications proceeds in two subsequent phases. In the first phase, the procedure recurses on the structure of the given GXW formulas for generating dedicated actors for monitoring inputs events, for generating corresponding control events, and for wiring these actors according to the structure of the given GXW formulas. In the second phase, appropriate values for unknown parameters are synthesized in order to realize the conjunction of all given GXW specifications. Here we use satisfiability checking for quantified Boolean formula (2QBF) for examining if there exists such conflicts between multiple GXW specifications. More precisely, existential variables of generated 2QBF problems capture the remaining design freedom when an output variable is not constrained by any trigger of low-level events.

We demonstrate that controller synthesis for the GXW fragment is in PSPACE as compared to the 2EXPTIME-completeness result of full-fledged LTL [27]. Under some further reasonable syntactic restrictions on the GXW fragment we show that synthesis is in coNP.

An implementation of our GXW structural synthesis algorithm and application to our benchmark studies demonstrates a substantial speed-up compared to existing LTL synthesis tools. Moreover, the structure of the generated control code in SDF follows the structure of the given GXW specifications, and is more compact and, arguably, also more readable and understandable than commonly used gate-level representations for synthesized control strategies.

The paper is structured as follows. We introduce in Section 2 some basic notation for LTL synthesis, a definition of the GXW fragment of LTL and SDF actor systems together with the problem of actor-based LTL synthesis under GXW fragment. Section 3 illustrates GXW and actor-based control for such specifications by means of an example. Section 4 includes the main technical contributions and describes algorithmic workflow for generating structured controllers from GXW, together with soundness and complexity results for GXW synthesis. A summary of our experimental results is provided in Section 5, and a comparison of GXW synthesis with closely related work on LTL synthesis is included in Section 6. The paper closes with concluding remarks in Section 7.

## 2 Problem Formulation

We present basic concepts and notations of LTL synthesis, and we define the GXW fragment of LTL together with the problem of synthesizing actor-based synchronous dataflow controllers for GXW.

### 2.1 LTL Synthesis

Given two disjoint sets of Boolean variables \(V_{in}\) and \(V_{out}\), the linear temporal logic (LTL) formulae over \(2^{V_{in} \cup V_{out}}\) is the smallest set such that (1) \(v \in 2^{V_{in} \cup V_{out}}\) is an LTL formula, (2) if \(\phi_1, \phi_2\) are LTL-formulae, then so are \(\neg \phi_1, \neg \phi_2, \phi_1 \lor \phi_2, \phi_1 \land \phi_2, \phi_1 \rightarrow \phi_2\), and (3) if \(\phi_1, \phi_2\) are LTL-formulae,
then so are \(G\phi_1, X\phi_1, \phi_1U\phi_2\). Given an \(\omega\)-word \(\sigma\), define \(\sigma(i)\) to be the \(i\)-th element in \(\sigma\), and define \(\sigma^i\) to be the suffix \(\omega\)-word of \(\sigma\) obtained by truncating \(\sigma(0)\ldots\sigma(i-1)\). The satisfaction relation \(\sigma \models \phi\) between an \(\omega\)-word \(\sigma\) and an LTL formula \(\phi\) is defined in the usual way. The weak until operator, denoted \(W\), is similar to the until operator but the stop condition is not required to occur; therefore \(\phi_1W\phi_2\) is simply defined as \((\phi_1U\phi_2) \lor G\phi_1\). Also, we use the abbreviation \(X^i\phi\) to abbreviate \(i\) consecutive \(X\) operators before \(\phi\).

A deterministic Mealy machine is a finite automaton \(C = (Q,q_0,2^{V_{in}}, 2^{V_{out}}, \delta)\), where \(Q\) is set of (Boolean) state variables (thus \(2^Q\) is the set of states), \(q_0 \in 2^Q\) is the initial state, \(2^{V_{in}}\) and \(2^{V_{out}}\) are sets of all input and output assignments defined by two disjoint sets of variables \(V_{in}\) and \(V_{out}\). \(\delta: 2^Q \times 2^{V_{in}} \rightarrow 2^{V_{out}} \times 2^Q\) is the transition function that takes (1) a state \(q \in 2^Q\) and (2) input assignment \(v_{in} \in 2^{V_{in}}\), and returns (1) an output assignment \(v_{out} \in 2^{V_{out}}\) and (2) the successor state \(q' \in 2^Q\). Let \(\delta_{out}\) and \(\delta_s\) be the projection of \(\delta\) which considers only output assignments and only successor states. Given a sequence \(a_0 \ldots a_k\) where \(\forall i = 0 \ldots k, a_i \in 2^{V_{in}}\), let \(\delta_{out}(q_0, a_0 \ldots a_k)\) abbreviate the output state derived by executing \(a_0 \ldots a_k\) as an input sequence on the Mealy machine.

Given a set of input and output Boolean variables \(V_{in}\) and \(V_{out}\), together with an LTL formula \(\phi\) on \(V_{in}\) and \(V_{out}\) the LTL synthesis problem asks the existence of a controller as a deterministic Mealy machine \(C\phi\) such that, for every input sequence \(a = a_0a_1a_2\ldots\), where \(a_i \in 2^{V_{in}}:\) (1) given the prefix \(a_0\) produce \(b_0 = \delta_{out}(q_0, a_0)\), (2) given the prefix \(a_0a_1\) produce \(b_1 = \delta_{out}(\delta_s(q_0, a_0), a_1)\), (3) given the prefix \(a_0 \ldots a_k\) produce \(b_{k+1} = \delta_{out}(\delta_s(q_0, a_0 \ldots a_k), a_{k+1})\), and (4) the produced output sequence \(b = b_0b_1\ldots\) ensures that the word \(\sigma = a_1a_2\ldots\), where \(a_i = a_ib_i \in 2^{V_{in}\lor V_{out}}\), \(\sigma \models \phi\).

### 2.2 GXW Synthesis

We formally define the GXW fragment of LTL. Let \(\phi^i, \psi^i, \psi^j\) be LTL formulae over input variables \(V_{in}\) and output variables \(V_{out}\), where all formulas are (without loss of generality) assumed to be in disjunctive normal form (DNF), and each literal is of form \(X^jv\) or \(\neg X^jv\) with \(0 \leq j \leq i\) and \(v \in V_{in}\lor V_{out}\). Clauses in DNF are also called clause formulae. Moreover, a formula \(\phi^i_{in}\) is restricted to contain only input variables in \(V_{in}\), and similarly, \(\phi^0_{out}\) contains only output variables in \(V_{out}\). Finally, \(\phi_{out}\) denotes either \(v_{out}\) or \(\neg v_{out}\), where \(v_{out}\) is an output variable.

For given input variables \(V_{in}\) and output variables \(V_{out}\), a GXW formula is an LTL formula of one of the forms (P1)-(P6) as specified in Table 1. For example, GXW formulas of the form (P2) stop locking \(\phi_{out}\) as soon as \((\psi^i_{in} \lor \rho^0_{out})\) holds. GXW specifications are of the form

\[
\psi \rightarrow \bigwedge_{m=1\ldots k} \eta_m ,
\]

where \(\psi\) matches the GXW pattern (P6), and \(\eta_m\) matches one of the patterns (P1) through (P5) in Table 1. Furthermore, the notation “\(^\ast\)” is used for projecting subformulas from \(\eta_m\), when it satisfies a given type. For example, assuming that sub-specification \(\eta_m\) is of pattern P3, i.e., it matches \(G(\phi^i_{in} \rightarrow X^j\phi_{out})\), \(\eta_m \cdot \phi_{out}\) specifies the matching subformula for \(\phi_{out}\). Notice also that GXW specifications, despite including the \(W\) operator, have the finite model property, since the smallest number of unrolling steps for disproving the existence of an implementation is linear with respect to the structure of the given formula (cmp. Section 4.4).

Instead of directly synthesizing a Mealy machine as in standard LTL synthesis, we are considering here the generation of actor-based controllers using the computational model of synchronous dataflow.
(SDF) without feedback loops. An actor-based controller is a tuple $\mathcal{S} = (\mathcal{V}_{in}, \mathcal{V}_{out}, Act, \tau)$, where $\mathcal{V}_{in}$ and $\mathcal{V}_{out}$ are disjoint sets of external input and output ports. Each port is a variable which may be assigned a Boolean value or undefined if no such value is available at the port. In addition, actors $\mathcal{A} \in Act$ may be associated with internal input ports $U_{in}$ and output ports $U_{out}$ (all named apart), which are also three-valued. The projection $\mathcal{A}.u$ denotes the port $u$ of $\mathcal{A}$. An actor $\mathcal{A} \in Act$ defines Mealy machine $\mathcal{C}$ whose input and output assignments are based on $2^{U_{in}}$ and $2^{U_{out}}$, i.e., the output update function of $\mathcal{C}$ sets each output port to true or false, when each input port has value in $\{true, false\}$. Lastly, $\mathcal{A}^{(i)}$ denotes a copy of $\mathcal{A}$ which is indexed by $i$.

Let $Act.U_{in}$ and $Act.U_{out}$ be the set of all internal input and output ports for $Act$. The wiring $\tau \subseteq (\mathcal{V}_{in} \cup Act.U_{in}) \times (\mathcal{V}_{out} \cup Act.U_{out})$ connects one (external, internal) input port to one or more (external, internal) output ports. For convenience, denote the wiring from port out of $\mathcal{A}_1$ to port in of $\mathcal{A}_2$ as $\mathcal{A}_1.out \rightarrow \mathcal{A}_2.in$. All ports are supposed to be connected, and every internal input port and every external output port is only connected to one wire (thus a port does not receive data from different sources). Also, we do not consider actor systems with feedback loops here (therefore no cycles such as the one in Figure 1(c)), since systems without feedback loops can be statically scheduled.\[1\]

Evaluation cycles are triggered externally under the semantics of synchronous dataflow. In each such cycle, the data received at the external input ports is processed and corresponding values are transferred to external output ports. Notice also that the composition of actors under SDF acts cycle-wise as a Mealy machine [39]. We illustrate the operational semantics of actor-based systems under SDF by means of the example in Figure 1(a), with input ports $in1$, $in2$, output port $out$, and actors $f_1$, $f_2$, $f_3$, $f_4$ (see also Figure 1(b)).\[1\]Now, assume that in the first cycle, the input ports $in1$ and $in2$ receive the value (false, true) and in the second cycle the value (false, true). The false value in $in1$ is copied to $f_1.i$. As $f_1$ is initially at state where $v = false$, it creates the output value true (places it to $f_1.o$) and changes its internal state to $v = true$. The value true from $f_1.o$ is then transferred to $f_4.i_1$ and $f_2.i_1$. However, at this stage one cannot evaluate $f_2$ or $f_4$, as the $i_2$ port is not yet filled with a value. $f_3$ receives the value from $in2$ and produces $f_3.o$ to false. Continuing this process, at the end of first cycle $out$ is set to true, while in the second cycle, $out$ is set to false.

As we do not consider feedback loops between actors in $Act$, from input read to output write, one can, using the enumeration method as exemplified above, create a static linear list $\Xi$ of size $|Act| + |\tau|$, where each element $\xi_{ind} \in \Xi$ is either in $Act$ or in $\tau$, for specifying the linear order (from the partial order) how data is transferred between wires and actors. Such a total order $\Xi$ is also called an evaluation ordering of the actor system $\mathcal{S}$.

One may wrap any Mealy machine $\mathcal{C}$ as an actor $\mathcal{A}(\mathcal{C})$ by simply creating corresponding ports in $\mathcal{A}(\mathcal{C})$ and by setting the underlying Mealy machine of $\mathcal{A}(\mathcal{C})$ to $\mathcal{C}$. Therefore, actor-based controllers

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\[1\] The formal operational semantics, as it is standardized notation from SDF, is relegated to the appendix.
may be synthesized for a given LTL specification $\phi$ by first synthesizing a Mealy machine $C$ realizing $\phi$, followed by the wrapping $C$ as $A(C)$, creating external I/O ports, and connecting external I/O ports with $A(C)$.

Given a GXW specification $\phi$ over the input variables $V_{in}$ and output variables $V_{out}$, the problem of GXW synthesis is to generate an actor-based SDF controller $S$ realizing $\phi$. As one can always synthesize a Mealy machine followed by wrapping it to an actor-based controller, GXW synthesis has the same complexity for Mealy machine and for actor-based controllers.

3 Example

We exemplify the use of GXW specifications and actor-based synthesis for these kinds of specification by means of an automatic sliding door $1$, which is visualized in Figure 2. Inputs and outputs are as follows: $in0$ is true when someone enters the sensing field; $in1$ denotes a closing limit switch - it is true when two doors touch each other; $in2$ denotes an opening limit switch - it is true when the door reaches the end; $out0$ denotes the opening motor - when it is set to true the motor rotates clockwise, thereby triggering the door opening action; and $out1$ denotes closing motor - when it is set to true the motor rotates counter-clockwise, thereby triggering the door closing action. Finally, the triggering of a timer $t0$ is modeled by means a (controllable) output variable $t0\text{start}$ and the expiration of a timer is modeled using an (uncontrollable) input variable $t0\text{expire}$.

Before stating the formal GXW specification for the example we introduce some mnemonics.

- $entering^1 := \neg in0 \land X in0$
- $\text{lim}\_\text{reached}^1 := \neg in2 \land X in2$
- $\neg t0\text{expire} \land (Xt0\text{expire})$
- $\text{closing}\_\text{stopped} := in1 \lor in0 \lor out0$

The superscripts denote the maximum number of consecutive next-steps. Now the automatic sliding door controller is formalized in GXW as follows.

$$S1: \ G(entering^1 \rightarrow X(out0 W in2))$$
$$S2: \ G(expired^1 \rightarrow X(out1 W closing\_\text{stopped}))$$
$$S3: \ \neg out0 W entering^1$$
$$S4: \ G(in2 \rightarrow \neg out0)$$
$$S5: \ G(\text{lim}\_\text{reached}^1 \leftrightarrow X(t0\text{start}))$$
$$S6: \ G(in0 \rightarrow \neg out1)$$
$$S7: \ G(\neg(out0 \land out1))$$

In particular, formula (S1) expresses the requirement that the opening of the door should continue ($out0 = true$) until the limit is reached ($in2$), and formulas (S3) and (S7) specify the expected initial behavior of the automatic sliding door. The GXW specifications for the sliding door example are classified as follows: formulas (S1), (S2) are of type (P2), (S3) is of type (P1), (S4), (S6) is of type (P3), (S5) is of type (P4), and (S7) of type (P5) according to Table 1.

Figure 3 visualizes an actor-based automatic sliding door controller which realizes the GXW specification (S1)-(S7). It is constructed from a small number of building blocks, which are also described in Figure 3. Monitor actors, for example, are used for monitoring when the $entering$, $\text{expired}$, and $\text{lim}\_\text{reached}$ constraints are fulfilled, the OR actor is introduced because of the $\text{closing}\_\text{stopped}$ release condition in specification (S1), and the two copies of the trigger-until actors are introduced because of the (P2) shape of the specifications (S1) and (S2). The input and output ports of the trigger-until actor are in accordance with the namings for (P2) in Table 2. Resolution actors are used for resolving potential conflicts between individual GXW formulas in a specification. These actors are parameterized with respect to a Boolean $A$, which is the output of the resolution actor in case all inputs of this actor may be in \{true, false\} (this set is denoted by the shorthand “∼” in Figure 3). The presented algorithm sets up a 2QBF problem for synthesizing possible values for these parameters. Because of the constraint (S7) on possible outputs $out0$ and $out1$, the parameter $A$ for the resolution actor for output $out0$, for example, needs to be set to $A := false$. Figure 3 also includes the operational behavior of selected actors in terms of high-level transitions and/or Mealy machines. The internal state and behavior for monitor actors, however, is synthesized, in linear time, from a given GXW constraint on inputs (see Section 1).

Finally, the structural correspondence of the actor-based controller in Figure 3 with the given GXW specification of the sliding door example is being made explicit by superscripting actors with index ($i$) whenever the actor has been introduced due to the $i$-th specification.
4 Structural Synthesis

We now describe the algorithmic details for generating structured controllers from the GXW specifications of the form \( \varrho \rightarrow \bigwedge_{m=1}^{k} \eta_m \). The automated sliding door is used as running example for illustrating the result of each step.

First, our algorithm prepares I/O ports, iterates through every formula \( \eta_m \) for creating high-level controllers (Step 1) based on the appropriate GXW pattern. For specifications of types P1 to P3, Table 2 lists the corresponding LTL specification (as high-level control objective), where input and release are input Boolean variables, output is an output Boolean variable.

Then, for each GXW formula, the algorithm constructs actors and wirings for monitoring low-level events by mimicking the DNF formula structure (Steps 2 and 3). On the structural level of clause formulas in DNF, the algorithm constructs corresponding controllers in linear time (Algorithm 1). Finally, the algorithm applies 2QBF satisfiability checking (and synthesis of parameters for resolution actors) for guaranteeing nonexistence of potential conflicts between different formulas in the GXW specifications (Step 4).

4.1 High-level Control Specifications and Resolution Actors

The initial structural recursion over GXW formulas is described in Step 1.
Step 1: Prepare external I/O ports, initiate high-level controller and resolution controllers

| Input   | LTL specification $\phi = \varphi \rightarrow \bigwedge_{m=1}^{k} \eta_m$, input variables $V_{in}$, output variables $V_{out}$ |
|---------|------------------------------------------------------------------------------------------------------------------|
| Output  | Actor-based (partial) controller implementation $S = \langle V_{in}, V_{out}, Act, \tau \rangle$, $map_{out}$ |
| 1       | let $map_{pattern} := \{ P1 \mapsto InUB, P2 \mapsto TrUB, P3 \mapsto IfTB \}$ |
| 2       | $V_{in} := \{ \overrightarrow{v_{in}}, v_{in} \in V_{in} \}$ |
| 3       | $V_{out} := \{ \overrightarrow{v_{out}}, v_{out} \in V_{out} \}$ |
| 4       | foreach $\eta_m, m = 1 \ldots k$ do |
| 5       | if $(p := \text{DetectPattern}(\eta_m)) \in \{ P1, P2, P3 \}$ then |
| 6       | Create actor $A^{(m)}$ from $A := map_{pattern}.get(p)$, and add to $S$; |
| 7       | else if $(p := \text{DetectPattern}(\eta_m)) \not\in \{ P4, P5, P6 \}$ then return error |
| 8       | let $map_{out} := \text{NewEmptyMap}()$; |
| 9       | foreach $v_{out} \in V_{out}$ do $map_{out}.put(v_{out}, \text{NewEmptyList}())$; |
| 10      | foreach $\eta_m, m = 1 \ldots k$ do |
| 11      | $map_{out}.get(v_{out}).add(m)$, where $v_{out}$ is the output variable used in $\tau_m.\varrho_{out}$; |
| 12      | foreach $v_{out} \in V_{out}$ do Add actor $Res_{v_{out}} := \text{CreateResActor}(map_{out}.get(v_{out}).size())$ to Act |
| 13      | foreach $\eta_m, m = 1 \ldots k$ do |
| 14      | let $v_{out}$ be the variable used in $\tau_m.\varrho_{out}$, ind := $map_{out}.get(v_{out}).indexOf(m)$; |
| 15      | if $\neg v_{out} \text{ equals } \tau_m.\varrho_{out}$ then // negation is used in literal |
| 16      | Create a negation actor $A^{(m)}$ and add it to Act; |
| 17      | $\tau := \tau \cup \{(A^{(m)}.\varrho_{out} \rightarrow \overrightarrow{A^{(m)}}, \text{input}), (A^{(m)}.\varrho_{out} \rightarrow Res_{v_{out}}, \text{input}_{out})\}$; |
| 18      | else $\tau := \tau \cup \{(A^{(m)}.\varrho_{out} \rightarrow \overrightarrow{Res_{v_{out}}, \text{input}_{out}})\}$ |
| 19      | foreach $v_{out} \in V_{out}$ do $\tau := \tau \cup \{(Res_{v_{out}}, \text{output} \rightarrow \overrightarrow{v_{out}})\}$ |

Step 1.1 - Controller for high-level control objectives. Line 1 associates the three high-level controller actors InUB, TrUB, IfTB with their corresponding pattern identifier. Implementations for the actors InUB, TrUB, IfTB are listed in Figure 3(b). For example, the actor IfTB is used for realizing actors InUB, TrUB, IfTB with their corresponding pattern identifier. Implementations for the actors are shown in Figure 3(b) - Res_{v_{out}}. The output of $\tau_{out}$ is true when one of its inputs is true, outputs false when one of its inputs is false, and outputs $A$ (which is currently an unknown value to be synthesized later) when all inputs are “-”. The number of input pins is decided by calling the map. E.g., for $Res_{out0}$ in Figure 3(a), three inputs are needed because $map_{out}.get(out0).size() = 3$. The output of
Step 2: Synthesize monitoring controllers (for pattern P1, P2, P3)

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Input : φ = g → \bigwedge_{m=1...k} \eta_m, V_{in}, V_{out}, S = (V_{in}, V_{out}, Act, \tau) from Step 1
Output: Actor-based (partial) controller S = (V_{in}, V_{out}, Act, \tau) by adding more elements

1. foreach \eta_m, m = 1...k do
   2. p := DetectPattern(\eta_m);
   3. if p ∈ {P1, P2, P3} then
      4. foreach \phi_{in} with size(\eta_m, \phi_{in}) inputs to Act;
         foreach clause formula \chi_{in} from DNF of \eta_m, \phi_{in} do
            Add A(C) to Act, where C := Syn(G(\chi_{in} ↔ X^{out}) ∧ \bigwedge_{i=0}^{h-1} X^i → out, \ln(\chi_{in}), \{out\});
            v_{in} ∈ ln(\chi_{in}) do τ := τ ∪ \{(v_{in} → → A(C), v_{in})\}
         τ := τ ∪ \{(\phi_{in} → → A(m).input)\};
   5. if p ∈ {P2} then
      6. Add an OR-gate actor OR_{\phi_{in}} with size(\eta_m, (\phi_{in} \lor \rho_{out})) inputs to Act;
         foreach clause formula \chi_{in} from DNF of \eta_m, \phi_{in} do
            Add A(C) to Act, where C := Syn(G(\chi_{in} ↔ X^{out}) ∧ \bigwedge_{i=0}^{h-1} X^i → out, \ln(\chi_{in}), \{out\});
            v_{in} ∈ ln(\chi_{in}) do τ := τ ∪ \{(v_{in} → → A(C), v_{in})\}
            if h = 0 then Add (A(C).out → → OR_{\phi_{in}} in_{index}(\chi_{in}, \phi_{in})) to τ else
            Add A(C_{\phi_{in}}) to Act, where C_{\phi_{in}} := CreateThetaCtrl(h);
            τ := τ ∪ \{(OR_{\phi_{in}} out → → A(C_{\phi_{in}}).set), (A(C).out → → A(C_{\phi_{in}}).in), (A(C_{\phi_{in}}).out → → OR_{\phi_{in}} in_{index}(\chi_{in}, \phi_{in}))\};
   7. Add an AND-gate actor AND_{\eta_m, \chi_{out}} with size(\chi_{out}) inputs to Act;
   8. foreach literal \omega_{out} of \chi_{out} do
      9. let \omega_{out} be the variable used in \omega_{out};
         if \omega_{out} equals ¬v_{out} (i.e., negation is used in literal) then
            Create \ACA_{\omega_{out}} and add it to Act (if not exists in Act);
            Add (\ACA_{\omega_{out}} output → → \ACA_{\omega_{out}} input) to τ (if not exists in τ);
            Add (\ACA_{\omega_{out}} output → → AND_{\omega_{out}} in_{index}(\omega_{out}, \chi_{out})) to τ;
         else τ := τ ∪ \{(\ACA_{\omega_{out}} output → → AND_{\omega_{out}} in_{index}(\omega_{out}, \chi_{out}))\};
      10. τ := τ ∪ \{(OR_{\phi_{in}} \lor \rho_{out}) out → → A(m).release)\};
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the high-level controller A^{m} is connected to the input of Res_{\omega_{out}}. When negation is needed due to
the negation symbol in \rho_{out} (line 15), one introduces a negation actor \ACA which
negates A^{m}.output when A^{m}.input is true or false (line 16,17). To ensure that connections are wired
appropriately, map\_{out} is used such that the number “ind” records the precise input port of
the Res\_{out} (line 14). Consider again the door example. Due to the
maintained list \{1, 3, 4\}, TrUB(1).output is connected to Res_{\omega_{out}}.input, i.e.,
the first input pin of Res_{\omega_{out}}. Also, as ¬0 is used in S3 and S4, the
wiring from InUB(3) and IfTB(4) to Res_{\omega_{out}} in Figure 3(a) has a negation actor in between.
Lastly, line 19 connects the output port of a resolution actor to the corresponding external
output port. If Res_{\omega_{out}} receives simultaneously true and false from two of its input ports, then
Res_{\omega_{out}}.output needs to be simultaneously true and false. These kinds of situations are
causing unrealizability of GXW specification, and Step 5 is used for detecting these kinds of inconsistencies.

4.2 Monitors and Phase Adjustment Actors

The second step of the algorithm synthesizes controllers for monitoring the appearance of an event
matching the subformula, and connects these controllers to previously created actors for realizing
high-level control objectives. For a formula \phi in DNF form, let size(\phi) return the number of clauses in
\( \phi \). For clause formula \( x^i_{in} \) in \( \phi \), let \( \ln(x^i_{in}) \) return the set of all input variables and \( \alpha = \text{index}(x^i_{in}, \phi_{in}) \) specify that \( x^i_{in} \) is the \( \alpha \)-th clause in \( \phi_{in} \).

**Step 2.1 - Realizing “input” part for pattern P1, P2, P3.** In Step 2 from line 3 to 9, the algorithm synthesizes controller realizing the portion input listed in Table 2 or equivalently, the \( \phi_{in} \) part listed in Table 1. Line 4 first creates an OR gate, as the formula is represented in DNF. Then synthesize a controller for monitoring each clause formula (line 5, 6) using function \( \text{Syn} \), with input variables defined in \( \ln(x^i_{in}) \) and a newly introduced output variable \( \{\text{out}\} \). The first attempt is to synthesize \( G(x^i_{in} \leftrightarrow X^i_{out}) \). By doing so, the value of \( x^i_{in} \) is reflected in \( \text{out} \). However, as the output of the synthesized controller is connected to the input of an OR-gate (line 8) and subsequently, passed through the port “input” of the high-level controller (line 9), one needs to also ensure that from time 0 to \( i - 1 \), \( \text{out} \) remains false, such that the high-level controller \( A_m \) for specification \( \eta_{in} \) will not be “unintentionally” triggered and subsequently restrict the output. To this end, the specification to be synthesized is \( G(x^i_{in} \leftrightarrow X^i_{out}) \land A_{i=0...i-1} X^i_{out} \), being stated in line 6.

For above mentioned property that needs to be synthesized in line 6, one does not need to use full LTL synthesis algorithms. Instead, we present a simpler algorithm (Algorithm 3) which creates a controller in time linear to the number of variables times the maximum number of \( X \) operators in the formula. Here again for simplicity, each state variable is three-valued (true, false, u); in implementation every 3-valued state variable is translated into 2 Boolean variables. In the algorithm, state variable \( v_{in}[i] \) is used to store the i-step history of for \( v_{in} \), and \( v_{in}[i] = u \) means that the history is not yet recorded. Therefore, for the initial state, all variables are set to u (line 4). The update of state variable \( v_{in}[i + 1] \) is based on the current state of \( v_{in}[i] \), but for state variable \( v_{in}[1] \), it is updated based on current input \( v_{in} \) (line 17). With state variable recording previously seen values, monitoring the event is possible, where the value of \( \text{out} \) is based on the condition stated from line 6 to 16.

Consider a controller realizing \( \chi_{in} := \neg in1 \land Xin1 \land Xin2 \land XX\neg in2 \) being executed under a run prefix (false, false)(true, true)(true, false). As shown in Figure 4 the update of state variables is demonstrated by a left shift. The first and the second output are false. After receiving the third input, the controller is able to detect a rising edge of in1 (via in1[2]=false and in1[1]=true) is immediately followed by a falling edge of in2 (via in2[1]=true and in2=false).

**Step 2.2 - Realizing “release” part for pattern P2.** Back to Step 2 the algorithm from line 10 to 29 synthesizes a controller realizing the portion release listed in Table 2 or equivalently, the \( \varphi_{in} \lor \rho_{out} \) part listed in Table 1. The DNF structure is represented as an OR-actor (line 11), taking input from \( \varphi_{in} \) (line 12-18) and \( \rho_{out} \) (line 19-28).

For \( \rho_{out} \) (line 19-28), first create an AND-gate for each clause in DNF. Whenever output variable \( v_{out} \) is used, the wiring is established by a connection to the output port of \( \text{Res}_{out} \) (line 27). Negation in the literal is done by adding a wire to connect \( \text{Res}_{out} \) to a dedicated negation actor \( \Box_{\text{Res}_{out}} \) to negate the output (line 23 to 26). Consider, for example, specification S2 of the automatic door running example, where the “release” part (in1 \lor in0 \lor out0) is a disjunction of literals using output variable \( \text{out} \). As a consequence, one creates an AND-gate (line 20) which takes one input \( \text{Res}_{out0}\; \text{output} \) (line 27), and connects this AND-gate to the OR-gate (line 28). Figure 3(a) displays an optimized version of this construction, since the single-input AND-gate may be removed and \( \text{Res}_{out0}\; \text{output} \) is directly wired with the OR-gate.

For \( \varphi_{in} \) (line 12 to 23), similar to Step 2.1, one needs to synthesize a controller which tracks the appearance of \( \chi_{in} \) (line 13). However, the start of tracking is triggered by \( \phi_{in} \) (the input subformula). That is, whenever \( \phi_{in} \) is true, start monitoring if \( \varphi_{in} \) has appeared true. This is problematic when \( \chi_{in} \) contains \( X \) operators (i.e., \( h > 0 \)). To realize this mechanism, at line 19, the function \( \text{CreateThetaCtrl} \) additionally initiates a controller which guarantees the following: Whenever input variable set turns
true, the following \( h \) output value of \( out \) is set to \( false \). After that, the value of output variable \( out \) is the same as the input variable \( in \). This property can be formulated as \( \Theta_h \) (to trigger consecutive \( h \) false value over \( out \) after seeing \( set = true \)) listed in Equation 2 with implementation shown in Figure 6. By observing the Mealy machine and the high-level transition function, one infers that the time for constructing such a controller in symbolic form is again linear to Figure 6. By observing the Mealy machine and the high-level transition function, one infers that the formula

\[
\Theta_h := (\neg out \ W set) \land G(set \rightarrow (\bigwedge_{z=0}^{h-1} \neg X^z out \land X^h((in \leftrightarrow out) W set)))
\]  

(2)

The overall construction in Step 2 is illustrated using the example in Figure 5 which realizes the formula

\[
G((-in1 \land Xin1) \rightarrow X(out1 W (-in2 \land Xin2)))
\]  

(3)

with \( V_{in} = \{in1, in2\} \) and \( V_{out} = \{out1\} \). This specification requires to set output \( out1 \) to \( true \) when a rising edge of \( in1 \) appears, and after that, \( out0 \) should remain \( true \) until detecting a raising edge of \( in2 \). Using the algorithm listed in Step 2, line 6 synthesizes the monitor for the input part (i.e., detecting rising edge of \( in1 \)), line 13 synthesizes the monitor for the release part (i.e., detecting rising edge of \( in2 \)), line 14 creates the wiring from input port to the monitor. As \( h = 1 \) (line 16), line 17 creates \( A(C_{\Theta_1}) \), and line 18 establishes the wiring to and from \( A(C_{\Theta_1}) \).

The reader may notice that it is incorrect to simply connect the monitor controller for \(-in2 \land Xin2\) directly to TrUB.release, as, when both \(-in1 \land Xin1\) and \(-in2 \land Xin2\) are \( true \) at the same time, TrUB.output is unconstrained. On the contrary, in Figure 5 when \(-in1 \land Xin1\) is \( true \) and the value is passed through TrUB.input, \( A(C_{\Theta_1}) \) enforces to invalidate the incoming value of TrUB.release for 1 cycle by setting it to \( false \).

**Step 3 - Realizing “input” for pattern P\( 4 \).** For pattern P4, in contrast to pattern P1, P2, and P3, the synthesized controller (following Step 3) is directly connected to a Resolution Actor. To maintain maximum freedom over output variable, one synthesizes the event monitor from the specification allowing the first \( i \) output to be \( \neg \), via \( \bigwedge_{z=0}^{i-1} X^z dc \land X^i G \neg dc \). The construction is analogous to Algorithm 1.

**Optimizations.** Runtimes for Steps 2 and 3 may be optimized by using simple pattern matching and hashing of previously synthesized controllers. We are listing three different opportunities for

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**Algorithm 1: Realizing Syn without full LTL synthesis**

**Input:** LTL specification \( G(\chi_{in1} \leftrightarrow X^i out \land \bigwedge_{z=0}^{i-1} X^z out) \), input variables \( in(\chi_{in1}) \), output variables \( \{out\} \)

**Output:** Mealy machine \( C = (Q, q_0, 2^{V_{in}}, 2^{V_{out}}, \Delta) \) for realizing the specification

1. \( V_{out} := \{out\}, V_{in} := \text{in}(\chi_{in1}) \);
2. \( \text{foreach} \ \text{variable} \ v_{in} \in \text{in}(\chi_{in1}) \ \text{do} \) // Create all state variables in the Mealy machine
3. \( \quad \text{for} \ j = 1 \ldots i \ \text{do} \ Q := Q \cup \{v_{in}[j]\}, \text{where} \ v_{in}[j] \ \text{is three-valued (true, false, u)} \)
4. \( q_0 := \bigwedge_{v_{in} \in \text{in}(\chi_{in1}), j \in \{1 \ldots i\}} v_{in}[j] := u \) // Initial state;
5. \( \quad \text{let} \ Cond := true \);
6. \( \text{foreach} \ \text{literal} \ X^k v_{in} \ \text{in} \ \chi_{in1} \ \text{do} \)
7. \( \quad \text{if} \ k = i \ \text{then} \)
8. \( \quad \quad \text{Cond} := \text{Cond} \land (v_{in} = \text{true}) \)
9. \( \quad \text{else} \)
10. \( \quad \quad \text{Cond} := \text{Cond} \land (v_{in}[i - k] = \text{true}) \)
11. \( \text{foreach} \ \text{literal} \ X^k \neg v_{in} \ \text{in} \ \chi_{in1} \ \text{do} \)
12. \( \quad \text{if} \ k = i \ \text{then} \)
13. \( \quad \quad \text{Cond} := \text{Cond} \land (v_{in} = \text{false}) \)
14. \( \quad \text{else} \)
15. \( \quad \quad \text{Cond} := \text{Cond} \land (v_{in}[i - k] = \text{false}) \)
16. \( \delta_{out} := (\text{out} := \text{Cond}) \) // Output assignment should follow the value of \( Cond \);
17. \( \delta_z := (\bigwedge_{v_{in} \in \text{in}(\chi_{in1}), j = 1 \ldots i - 1} v_{in}[j + 1] := v_{in}[j]) \land (\bigwedge_{v_{in} \in \text{in}(\chi_{in1})} v_{in}[1] := v_{in}) \);
Fig. 4. Executing monitor with $\tilde{X}_a := \neg in1 \land X in1 \land X in2 \land XX \neg in2$, by taking first three inputs $(false, false)(true, true)(true, false)$.

Fig. 5. Correct controller construction for specification satisfying pattern $P_2$.

Fig. 6. Implementing $\Theta_h$ (state variables not mentioned in update remain the same value).

optimized generation of monitors. First, the controller in Figure 3(a) for monitoring $\neg in0 \land X in0$ is connected to two high-level controllers. The second case can be observed in Figure 3 where by rewriting in1 and in2 to in, the controller being synthesized is actually the same. Therefore, one can also record the pattern for individual monitor and perform synthesis once per pattern. A third opportunity for optimization occurs when Algorithm 1 takes $i = 0$ (i.e., no $X$ operator is used). In these case there is no need to create a controller at all and one may proceed by directly building a combinatorial circuit, similar to the constructions of line 19 to 28 in Step 2. For example, for specification $S_2$ of the automatic door, the release part is in1 $\lor$ in0 $\lor$ out0; since no $X$ operator occurs, a combinatorial circuit is created by wiring directly in1 and in0 to the OR-gate.

4.3 Parameter Synthesis for 2QBF without Unroll

Step 3 as described above constructs actors as building blocks and wires the actors according to the structure of the given GXX specification. The resulting (partial) controller, however, does not yet realize this specification as it may still contain unknowns in the resolution actors. Further checks are necessary, and a controller is rejected if one of the following conditions holds.

(Condition 1) The wiring forms a directed loop in the constructed actor-based controller.
(Condition 2) It is possible for a resolution actor Res$_{v_{out}}$ to receive true and false simultaneously.
(Condition 3) Outputs violate invariance conditions of pattern P5.

Condition 1 is checked by means of a simple graph analysis: (1) let all ports be nodes and wirings be edges; (2) for each actor, create directed edges from each of its input port to each of its output port; (3) check if there exists a strongly connected component in the resulting graph using, for example, Tarjan’s algorithm 29.

Conditions 2 and 3 are checked by means of creating corresponding 2QBF satisfiability problems. Recall that each resolution actor Res$_{v_{out}}$ is parameterized with respect to the output $A$ when all incoming inputs for Res$_{v_{out}}$ are “$-$”. The corresponding parameter assignment problem is encoded as a 2QBF formula, where existential variables are the parameters to be synthesized, universal variables are input variables, and the quantifier-free body is a logical implication specifying that the encoding of the system guarantees condition 2 and 3.

Step 4 shows a simplified algorithm for generating 2QBF constraints which does not perform unrolling. Stated in line 15, the quantifier free formula is of form $\Gamma_n \rightarrow \Gamma_g$, where $\Gamma_n$ are input assumptions and system dynamics, and $\Gamma_g$ are properties to be guaranteed.

3 Quantified Boolean Formula with one top-level quantifier alternation.
Step 3: Synthesize monitoring controllers (for pattern P4)

Input : LTL specification \( \phi = \phi_1 \rightarrow \bigwedge_{m=1}^{k} \eta_m, V_{in}, V_{out} \), actor-based (partial) controller \( S = (V_{in}, V_{out}, Act, \tau) \) and map\(_{out}\) from Step 2.

Output: Actor-based (partial) controller \( S = (V_{in}, V_{out}, Act, \tau) \) by adding more elements

1. \textbf{foreach} \( \eta_m, m = 1 \ldots k \) do
2. \quad \textbf{if} DetectPattern\((\eta_m) \in \{ P4 \} \) then
3. \quad \quad \textbf{foreach} clause formula \( \chi_{in} \) from \(\phi\) of \( \eta_m, \phi_{in} \) do
4. \quad \quad \quad \text{Add a size(\(\eta_m, \phi_{in}\))-input OR-gate actor OR(\(\phi_{in}\)) to Act;}
5. \quad \quad \quad \text{\( C_{\chi_{in}} := \text{Syn}(G(\chi_{in}) \leftrightarrow X^*\text{out}) \land \bigwedge_{m=1}^{k} \chi_{out} \land X^*G\text{dc}, \text{dc}, \text{ln}(\chi_{in}), \{ \text{out}, \text{dc} \}); \)}
6. \quad \quad \quad \text{Add \( A(C_{\chi_{in}}) \) to Act;}
7. \quad \quad \quad \text{\( \tau := \tau \cup \{ (\text{OR}_{\phi_{in}} \cdot \text{out} \rightarrow \text{Res}_{\text{out}} \cdot \text{input}) \} \)}
8. \quad \textbf{let} \( v_{out} \) be the variable used in \( \tau_m \cdot \text{Act}, \text{ind} := \text{map}_{out} \cdot \text{get}(v_{out}) \cdot \text{indexOf}(m); \)
9. \quad \textbf{if} \( v_{out} \) equals \( \neg v_{out} \) then \quad \text{// negation is used in literal}
10. \quad \quad \text{Create a negation actor \( \square(m) \) and add it to Act;}
11. \quad \quad \text{Add (\( \text{OR}_{\phi_{in}} \cdot \text{out} \rightarrow \square(m) \cdot \text{ind}) \cdot (\square(m) \cdot \text{output} \rightarrow \text{Res}_{\text{out}} \cdot \text{input} \cdot \text{mod}) \) to \( \tau \);}
12. \quad \textbf{else} \text{ Add (\( \text{OR}_{\phi_{in}} \cdot \text{out} \rightarrow \text{Res}_{\text{out}} \cdot \text{input} \cdot \text{mod}) \) to \( \tau \)}

First, unknown parameters are added to the set of existential variables \( V_3 \) (line 2). All other variables are universal variables. Then based on the evaluation ordering of \( S \), perform one of the following tasks:

- When an element \( \xi \) in the execution ordering \( \Xi \) is a wire (line 5), we add source and dest as universal variables (as \( V_\gamma \) is a set, repeated variables will be neglected), and establish the logical constraint (source \( \leftrightarrow \) dest) (lines 6 to 8).

- When an element \( \xi \) in the execution ordering \( \Xi \) is an actor, we use function EncodeTransition to encode the transition (pre-post) relation as constraints (line 11), and add all state variables (for pre and post) in the actor (recall our definition of Mealy machine is based on state variables) to \( V_\gamma \) using function GetStateVariable (line 10).

\( \gamma_a \) is initially set to \( g \) (line 1) to reflect the allowed input patterns regulated by the specification (specification type P6). Line 12 creates the constraint stating that no two inputs of a resolution actor should create contradicting conditions. As the number of input ports for any resolution actor is finite, the existential quantifier is only an abbreviation which is actually rewritten to a quantifier-free formula describing relations between input ports of a resolution actor.

The encoding presented in Step 4 does not involve unroll (it encodes the transition relation, but not the initial condition). Therefore, by setting all variables to be universally quantified, one approximates the behavior of the system dynamics without considering the relation between two successor states. Therefore, using Step 3 only guarantees soundness: If the formula is satisfiable, then the specification is realizable (line 15, 16). Otherwise, unknown is returned (line 17).

As each individual specification of one of the types \{P1, P2, P3, P4\} is trivially realizable, the reason for rejecting a specification is (1) simultaneous true and false demanded by different sub-specifications, (2) violation of properties over output variables (type P5), and (3) feedback loop within \( S \). Therefore, as Steps 1-4 guarantees non-existence of above three situations, the presented method is sound.

Theorem 1. (Soundness) Let \( \phi \) be a GXW specification, and \( S \) be an actor-based controller as generated by Steps 1-4 from \( \phi \); then \( S \) realizes \( \phi \).

---

\footnote{Even without unroll, one can infer relations over universal variables via statically analyzing the specification. As an example, consider two sub-specifications \( S_1 : G(\text{in}1 \rightarrow (\text{out} \text{W} \text{in}2)) \) and \( S_2 : G(\text{in}2 \rightarrow (\neg \text{out} \text{W} \text{in}1)) \). One can infer that it is impossible for \( \text{TrUB}^{(1)} \) and \( \text{TrUB}^{(2)} \) to be simultaneously have state variable \( \text{lock} = \text{true} \), as both starts with \( \text{lock} = \text{false} \), and if \( S_1 \) first enters \( \text{lock} (\text{lock} = \text{true}) \) due to \( \text{in}1 \), the \( S_2 \) cannot enter, as release part of \( S_2 \) is also \( \text{in}1 \). Similar argument follows vice versa.}
Step 4: Parameter synthesis by generating 2QBF constraints

Input: LTL specification \( \phi = g \rightarrow \bigwedge_{m=1}^{k} \eta_m \), input variables \( V_{in} \), output variables \( V_{out} \), partial controller implementation \( S = (V_{in}, V_{out}, Act, \tau) \) with unknown parameters.

Output: Controller implementation \( S \) or "unknown"

1. let \( T_a := g, T_g := := \text{NewEmptySet;} \)
2. foreach \( \nu \in V_{out} \) do \( V_2 := V_2 \cup \{ \text{Res}_{\nu}, \text{Act} \} \)
3. let \( \Xi \) be the evaluation ordering of \( S \)
4. foreach \( \xi \in \Xi \) do
   5. if \( \xi \in \tau \) then // \( \xi \) is a wire; encode biimplication among two ports
      6. let \( \xi \) be (source \( \rightarrow \) dest);
      7. \( V_{\xi}.add(\text{source}) \), \( V_{\xi}.add(\text{dest}) \);
      8. \( T_a := T_a \land (\text{source} \leftrightarrow \text{dest}) \);
   9. else
      10. \( V_{\eta}.add(\text{GetStateVariable}(\xi)) \);
      11. \( T_a := T_a \land (\text{EncodeTransition}(\xi)) / \ast \xi \in \text{Act} / \ast ; \)
12. for \( \nu \in V_{out} \) do \( T_g := T_g \land (B_{i,j} : (\text{Res}_{\nu}, \text{input}, i) = \text{true} \land (\text{Res}_{\nu}, \text{input}, j) = \text{false}) \)
13. foreach \( \eta_m, m = 1 \ldots k \) do
   14. if \( \text{DetectPattern}(\eta_m) \in \{ P5 \} \) then \( T_g := T_g \land \eta_m \)
15. if \( \text{Solve2QBF}(V_2, V_g, T_a \rightarrow T_g).\text{isSatisable} \) then
   16. return \( S \) by replacing each \( \text{Res}_{\nu}, \text{Act} \) by the value of witness in 2QBF;
17. else return unknown

The GXW synthesis algorithm as described above, however is incomplete, as controllers with feedback loops are rejected; that is, whenever output variables listed in the release part of P2 necessitate simultaneous reasoning over two or more output variables. Figure 7 display an controller (with feedback loop) for realizing the specification \( G(\text{in1} \rightarrow (\text{out1Wout2})) \land G(\text{in2} \rightarrow (\text{out2Wout1})) \). However, our workflow rejects such a controller even though the given specification is realizable. With further structural restriction over GXW (which guarantees no feedback loop in during construction) and by using unrolling of the generated actor-based controllers, the workflow as presented here can be made to be completeness, as demonstrated in Section 4.4.

(Remarks) Notice that in the presented algorithm, the synthesized controller does not contain a detector for checking if environment assumption (type P6) is violated. Practically, input assignments violating P6 should never appear. If such a violation is possible, then immediately after the assumption violation and from that time onwards, the controller is allowed to produce arbitrary output assignment. Here we omit details, but would like to stress that one can easily mediate such scenarios by several ways. E.g., one can append a detection actor (by building a combinational circuit out of the specification type P6) to detect the event whether the environment assumption is violated. At the same time, provide an additional input port on every resolution actor to override the output (i.e., a resolution actor should consider first if environment assumption is violated: if so, then continuously output false), and link the detection actor with the newly created port.

Also, there are unlikely scenarios such as declaring output variables without having them used in any specification. One can mediate it by always connecting a wire from one input port to the output port of a unused output variable, without building a resolution actor. The presented algorithm here also omits details of such corner cases.

### 4.4 General Properties for GXW Synthesis

Since unrealizability of a GXW specification is due to the conditions (1) simultaneous true and false demanded by different sub-specifications, and (2) violation of properties over output variables (type

\[ \text{in2} \quad \text{TrUB} \quad \text{Resout1} \quad \text{out1} \]

\[ \text{in2} \quad \text{TrUB} \quad \text{Resout2} \quad \text{out2} \]
P5, one can build a counter-strategy by first building a tree that provides input assignments to lead all runs to undesired states violating (1) or (2), then all leaves of the tree violating (1) or (2) are connected to a self-looped final state, in order to accept $\omega$-words. As the input part listed in Table 2 does not involve any output variable, a counter-strategy, if exists, can lead to violation of (1) or (2) within $\Omega$ cycles, where $\Omega$ is a number sufficient to let each input part of the sub-specification be true in a run.

**Lemma 1.** For GXW specification $\varrho \rightarrow \bigwedge_{m=1\ldots k} \eta_m$, if (a) $\rho_{\text{out}}^0$ is false for all $\eta_m$ of type P2 and (b) no specification of type P5 exists, then if the specification is not realizable, then there exists a counter-strategy which leads to violation of (1) or (2) in $\Omega$ steps, where $\Omega$ is bounded by the sum of (i) the number of specifications $k$, and (ii) the sum of all $i$ value defined within each $\phi_i^{\text{in}}$ of $\eta_m$.

When $\rho_{\text{out}}^0$ is false for all $\eta_m$ of type P2, our presented construction guarantees no feedback loop. As no specification of type P5 exists, the selection of $\mathcal{A}$ never influences whether the specification is realizable. Therefore, quantifier alternation is removed. To this end, checking unrealizability is equivalent to nondeterministically guessing $\Omega$ input assignments and subsequently, checking if a violation of (1) or (2) appears by executing $\mathcal{S}$. This also means that under the restriction from Lemma 1, a slight modification of Step 4 to perform unrolling the computation $\Omega$-times makes our synthesis algorithm complete.

**Lemma 2.** Deciding whether a given GXW specification, which also obeys the additional restrictions as stated in Lemma 1, is realizable or not is in $\text{co-NP}$.

For the general case, the bound in Lemma 1 remains valid (as input part is not decided by the output variable). Complexity result is achieved by, without using our construction, directly using finite memory to store and examine all possible control strategies in $\Omega$.

**Lemma 3.** For GXW specification $\varrho \rightarrow \bigwedge_{m=1\ldots k} \eta_m$, if the specification is not realizable, then there exists a counter-strategy which leads to violation of (1) or (2) in $\Omega$ steps, where $\Omega$ is bounded by condition similar to Lemma 1.

**Lemma 4.** Deciding whether a given GXW specification is realizable or not is in $\text{PSPACE}$.

The above mentioned bounds are only conditions to detect realizability of a GXW specification, while our presented workflow in Section 4 targets generating structured implementations. Still, by unrolling the computation $\Omega$-times, one can detect if a controller, following our regulated structure, exists.

### 4.5 Extensions

One can extend the presented workflow to allow richer specification than previously presented GXW fragment. Here we outline how these extensions are realized by considering the following sample specification: $G((\text{in1} \rightarrow \text{out1}) \land G((\text{in2} \lor \text{out1}) \rightarrow ((\text{out2} \land \neg \text{out3}) \land \text{in3})))$. The SDF controller implementation is shown in Figure 8. First, conjunctions in $\varrho_{\text{out}}$ can be handled by considering each output variable separately. E.g., for $\varrho_{\text{out}} \equiv \text{out2} \land \neg \text{out3}$, in Figure 8 both are connected to the same TrUB.

![Fig. 8. Control implementation.](attachment:image)

Second, the use of output variables in “input” part for pattern P1, P2, P3 is also supported, provided that in effect a combinatorial circuit is created (i.e., output variables should always proceed with $X'$), and the generated system does not create a feedback loop. E.g., for the antecedent (in2 $\lor$ out1), it is created by wiring the $\text{Res}_\text{out1, out}$ to an OR-gate.

6 Rejecting feedback loops on the controller structure is only a restriction of our presented method and is not the reason for unrealizability; similar to Figure 7 feedback loop can possibly be resolved by merging all actors involving feedback to a single actor.

7 A counter-strategy in LTL synthesis a state machine where the environment can enforce to violate the given property, regardless of all possible moves by the controller [27].
5 Experimental Evaluation

We implemented a tool for GXW synthesis in Java, which invokes DepQBF [21] (Version 5.0) for QBF solving. Table 3 includes experimental results for a representative subset of our PLC benchmark examples. Execution times is recorded using Ubuntu VM (Virtual Box with 3GB RAM) running on an Intel i7-3520M 2.9 Ghz CPU and 8GB RAM). Most control problems are solved in less than a second.

GXW synthesis always generated a controller without feedback loops for all examples. Table 3 lists a comparison of execution times of GXW synthesis and the bounded LTL synthesis tool Acacia+ [8] (latest version 2.3). We used the option --player 1 of Acacia+ for forcing the environment to take a first move, but we did not do manual annotation in order to support compositional synthesis in Acacia+, as it is not needed by our tool. For many of the simpler case studies, the reported runtimes of Acacia+ are similar to GXW synthesis. However, GXW seems to scale much better to more complex case studies with a larger number of input and output variables such as examples 5, 9, 11, 12, 13, 15, 16, 17, 18, 19 in Table 3. The representation of the generated controller in terms of a system of interacting actors in GXW synthesis, however, allows the engineering to trace each sub-specification with corresponding partial implementation. In fact the structure of the controllers generated by GXW is usually similar to reference implementations by the case study providers. In contrast, a controller expressed in terms of single Mealy machine is rather difficult to grasp and to maintain for problems such as example 18 with 13 input and 13 output variables.

6 Related Work

Apart from the description in Section 1 here we compare GXW synthesis with related GR(1) synthesis (e.g., [15,25,31,5]) and bounded LTL synthesis (e.g, [8,11,28]) techniques.

Synthesis for the GR(1) fragment of LTL is in time polynomial to the number of nodes of a generated game, which is EXPTIME when considering exponential blow-up caused by input and output variables. GXW is in PSPACE, where GXW allows W and GR(1) allows F. Even though it has been demonstrated that the expressiveness of GR(1) is enough to cover many practical examples, the use of an until logical operator, which is not included in GR(1), proved to be essential for encoding a majority of our PLC case studies. Also, implementations of GR(1) synthesis such as Anzu [15] do not generate structured controllers. Since GR(1) synthesis, however, includes a round-robin arbiter for circulating among sub-specifications, the systematic structuring of controllers underlying GXW synthesis may be applicable for synthesizing structured GR(1) controllers.

Bounded synthesis supports full LTL and is based on a translation of the LTL synthesis problem to safety games. By doing so, one solves the safety game and finds smaller controllers (as demonstrated in synthesis competitions via tools like Simple BDD solver [13], AbsSynthe [9], Demiurge [17]). The result of solving safety games in bounded LTL synthesis usually is a monolithic Mealy (or Moore) machine, whereas our GXW synthesis method of creating SDF actors may be understood as a way of avoiding the expensive construction of the product of machines. Instead, we are generating controllers by means of wiring smaller sub-controllers for specific monitoring and event triggering tasks. The structure of the resulting controllers seem to be very close to what is happening in practice, as a number of our industrial benchmark examples are shipped with reference implementation which are usually structured in a similar way. The size of the representations of generated controllers is particularly important when considering resource-bounded embedded computing device such as a PLCs. LTL component synthesis, however, has the same worst-case complexity as full LTL synthesis [22].

7 Conclusion

We have identified a useful subclass GXW of LTL for specifying a large class of embedded control problems, and we developed a novel synthesis algorithm (in PSPACE) for automatically generating structured controllers in a high-level programming language with synchronous dataflow without

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8 Approximately 0.25 seconds is used for initializing JVM in every run.
cycles. Our experimental results suggest that GXW synthesis scales well to industrial-sized control problems with around 20 input and output ports and beyond.

In this way, GXW synthesis can readily be integrated with industrial design frameworks such as CODESYS [3], Matlab Simulink, and Ptolemy II, and the generated SDF controllers (without cycles) can be statically scheduled and implemented on single and multiple processors [18]. It would also be interesting to use our synthesis algorithms to automatically generate control code from established requirement frameworks for embedded control software such as EARS [23]. Moreover, our presented method supports traceability between specifications and the generated controller code as required by safety-critical applications. Traceability is also the basis for an incremental development methodology.

One of the main impediments of using synthesis in engineering practice, however, is the lack of useful and automated feedback in case of unrealizable specifications [6, 10, 20] or realizable specifications with unintended realizations. The use of a stylized specification languages such as GXW seems to be a good starting point for supporting design engineers in identifying and analyzing unrealizable specifications, since there are only a relatively small number of potential sources of unrealizability in GXW specifications. Finally, hierarchical SDF may also be useful for modular synthesis [30].

Acknowledgement

We thank Lăcrămioara Aștefănoaei for her feedback during the development of the paper.

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Observe the example in the paper, closing stopped contains out0. This is the only part that is not mentioned in the textural specification, but it is required to make the specification realizable. Introducing out0 needs creativity, and it is the part where one needs an engineer in the loop. Not mentioned in this paper, we are also developing concepts in order to automatically add such a disjunction, similar to discovery of environment assumptions as investigated by us and also by others (e.g., [20]).
Appendix

A  Operational Semantics of SDF

The operational semantics of SDF can be summarized using the below action sequence; one can use the example in Figure 1(a)(b) to ease understanding.
(i) All ports start with initial value undefined;
(ii) A cycle is started by reading inputs andb setting the external input ports to either true or false;
(iii) For all wires connected to the same source (external input port / internal output port), copy data to the connected destination (internal input port / external output port). Lastly, change the value for the source port to be undefined.
(iv) When values of all input ports of an actor are not undefined, produce output and update to the corresponding output ports, by executing the underlying Mealy machine of the actor.
(v) When all external output ports are true or false and all internal ports are undefined, proceed to Step (vi). Otherwise, continue with Step (iii).
(vi) Produce output based on the data in the external output port, where each port can only be true or false following Step (v). Reset each external output port to undefined, and move to Step (ii).

B  Soundness

We prove that the if a controller $\mathcal{S}$ is produced following the workflow from Step 1 to Step 4, then it is correct, meaning that it realizes the GXW specification $\varphi \rightarrow \bigwedge_{m=1...k} \eta_m$.

The correctness proof can be understood using the following structure: (A) Prove that the behavior the controller is well-defined, i.e., given any (infinite) input sequence, the controller can generate an infinite output sequence such that the combined sequence forms an $\omega$-word. (B) As the specification under synthesis has the structure $\varphi \rightarrow \bigwedge_{m=1...k} \eta_m$ where $\varphi$ is a property over input variables, it suffices to prove individually that all produced $\omega$-words satisfy $\eta_m$. For each $\eta_m$, we then prove that the created partial dataflow model realizes $\eta_m$. We use operational semantics to discuss the data transfer in each cycle; an alternative method is to view the data processing in each cycle analogous to applying functional composition.

(A) The internal dataflow of a synthesized controller, due to the sanity check of Condition 1 in Section 4.3, obeys the following structure (here we omit the logic gates): external input ports $\Rightarrow$ high-level controllers $\Rightarrow$ resolution actors $\Rightarrow$ external output ports.

The satisfiability of 2QBF guarantees that for each output variable $v_{\text{out}}$, under any input assignment, $\text{Res}_{v_{\text{out}}}$ cannot receive from two input ports true and false. Therefore, the output value of $\text{Res}_{v_{\text{out}}}$ is well-defined, and as $\text{Res}_{v_{\text{out}}} \dashrightarrow v_{\text{out}}$ the value of $v_{\text{out}}$ at the end of a cycle is either updated to true or to false.

(B, Specification Type 5) For specification $\eta_m$ which is of type 5 (invariance condition), they are guaranteed by line 15 of Step 4.

(B, Specification Type 3) In Step 2 the algorithm synthesizes the monitor controller $G(\chi_\text{in} \leftrightarrow X^\text{out}) \land \bigwedge_{k=0...i-1} X^k\text{-out}$ and connect the controller to external input ports. The output of the monitor is connected to an OR-gate, which then connects to the input port (input) of the high-level controller realizing $G(\text{input} \rightarrow \text{output})$. The output of the high-level controller is connected to one of the input ports of $\text{Res}_{v_{\text{out}}}$ (when $\varrho_{\text{out}} \equiv \neg v_{\text{out}}$, a negation actor is inserted in between), which then produces output to $v_{\text{out}}$.

Our goal is to prove that the composition of these sub-controllers via wiring of ports is a controller realizing $G(\phi_\text{in}^j \rightarrow X^i \varrho_{\text{out}})$. Based on the definition, the synthesized controller realizes $G(\phi_\text{in}^j \rightarrow X^i \varrho_{\text{out}})$, if for all produced $\omega$-words satisfies the property $G(\phi_\text{in}^j \rightarrow X^i \varrho_{\text{out}})$, i.e.,

(G) for all $j \geq 0, \phi_\text{in}^j \rightarrow X^i \varrho_{\text{out}}$ holds
(\neg) for all $j \geq 0$, if $\phi_\text{in}^j$ holds then $X^i \varrho_{\text{out}}$ holds
(X), proof goal for all $j \geq 0$, if $\phi_\text{in}^j$ holds at time $j$, then $\varrho_{\text{out}}$ holds at $j + 1$.

Based on the definition, $\varrho_{\text{out}}$ is either $v_{\text{out}}$ or $\neg v_{\text{out}}$, where $v_{\text{out}}$ is an output variable. Here we prove only for case where $\varrho_{\text{out}} \equiv v_{\text{out}}$; for case $\varrho_{\text{out}} \equiv \neg v_{\text{out}}$ only a negation actor is introduced and the proof is similar. For the synthesized controller:
The specification of the monitor contains $G(\chi_{in}^i \leftrightarrow X^i_{out})$. Thus it guarantees that for all $j \geq 0$, if $\chi_{in}^i$ holds (does not hold) at time $j$, then at $j + i$, the value of $\text{out}$ is computed to true (false) after executing the monitor.

All monitors are connected to an OR gate, mimicking the formula structure. It guarantees that for all $j \geq 0$, if $\phi_{in}^i$ holds at time $j$ (due to one of its sub-formula $\chi_{in}^i$ being true at time $j$), then output port $\text{out}$ of the OR gate is true at $j + i$ (as the port out of the monitor is true at time $j + i$, and it is wired to an input of the OR-gate).

Similarly, if $\phi_{in}^i$ does not hold at time $j$ (due to all of its sub-formula $\chi_{in}^i$ being false at time $j$), then output port $\text{out}$ of the OR gate has value false at $j + i$ (as every port out of the monitor is false at time $j + i$, and it is wired to an input of the OR-gate).

The high-level controller $\text{IFTB}$ realizes $G(\text{input} \rightarrow \text{output})$, which guarantees that at time $j + i$, if input holds then output holds. As the output port of the OR-gate is wired to $\text{IFTB.input}$, if $\phi_{in}^i$ holds at time $j$, then at time $j + i$ $\text{IFTB.output}$ is updated to true, after executing $\text{IFTB}$.

At time $j + i$, whenever a resolution actor $\text{Res}_{\text{out}}$ receives a true from the input, the execution of $\text{Res}_{\text{out}}$ produces the true to $\text{Res}_{\text{out}}$, thus for output port $\text{out}$, it is updated to true at time $j + i$. As $\text{out} \equiv \text{out}$, $\text{out}$ holds at time $j + i$.

Proof similar to type 3, by first decomposing the specification formula, followed by showing that the dataflow guarantees desired behavior.

Informal sketch; to ease understanding Again the proof follows the structure of decomposing the specification formula, followed by showing that the dataflow guarantees desired behavior. As the controller monitoring event $\phi_{in}^i$ is connected to the $\text{InUB}$ block, to guarantee correctness, before observing event $\phi_{in}^i$, $\text{InUB}$ should always set output to true. In line 6 of Step 2 the first $i - 1$ output of the monitor is false. Therefore, $\text{InUB}$ does not change to ”¬(¬)” within time 0 to $i - 1$. From time $i$ onwards, $\phi_{in}^i$ is well defined and correctness is guaranteed.

Formal argument Here we again consider $\text{out} \equiv \text{out}$, as the other case ($\text{out} \equiv \neg \text{out}$) is analogous. Based on the definition, the synthesized controller realizes $\text{out} \equiv \text{out} W \phi_{in}^i$, if for all produced $\omega$-words satisfies the property $\phi_{out}^i W \phi_{in}^i = (\phi_{out}^i U \phi_{in}^i) \lor G \phi_{out}^i$, i.e., it satisfies $(\text{out} \lor \neg \phi_{in}^i)$ or $G \text{out}$. We now consider whether an input sequence makes ($\phi_{in}^i$) holds or not - this condition partitions all input sequences to two categories, and subsequently, make either left or right part of the disjunction hold.

Assume there $\exists j$ such that $\phi_{in}^i$ first holds at $j$, we prove that an implementation following the construction guarantees that $\text{out}$ is true from 0 to $j - 1$, thereby satisfying the strong-until part (U).

As $\phi_{in}^i$ uses consecutive $i \text{X}$ operators, although at cycle $j$ the output can no longer produce output true, as the controller cannot perform clairvoyance over future inputs, it needs to continuously output true until cycle $j + i$, such that it can decide $\chi_{in}^i$ holds at time $j$. In other words, as $j$ is the first time where $\chi_{in}^i$ is true and the controller can only know it at time $j + i$, the output should always be true from time 0 to $j + i - 1$, in order to satisfy the formula.

- From cycle 0 to $i - 1$, the output is always true. Consider the monitor component. Within cycle 0 to $i - 1$, it produces false, due to ”$\bigwedge_{z=0}^{i-1} X^{z} \text{out}$” in realizing the specification $G(\chi_{in}^i \leftrightarrow X^i_{out}) \land \bigwedge_{z=0}^{i-1} X^{z} \text{out}$. As all monitors are connected to an OR-gate, the output of produced by the OR-gate is false from cycle 0 to $i - 1$. As the output of the OR-gate is connected to $\text{InUB}$ which turns “¬” only after it receives true, the output of $\text{InUB}$ is true from 0 to $i - 1$. Thus, $\text{out}$ is updated with value true from 0 to $i - 1$.

- From time $i$ to $j + i - 1$, due to ”$G(\chi_{in}^i \leftrightarrow X^i_{out})$” in realizing the specification $G(\chi_{in}^i \leftrightarrow X^i_{out}) \land \bigwedge_{z=0}^{i-1} X^{z} \text{out}$, as $\chi_{in}^i$ first holds at $j$, so out first holds at time $j + i$, meaning that before time $j + i$, the monitor produces false. As all monitor produces false before time $j + i$, the input to the $\text{InUB}$ is false. Thus, the output produced by $\text{InUB}$ is true. Therefore, before time $j + i$, $\text{out}$ is always updated with value true, making the strong-until condition hold.
(v, right) Assume $\beta j$ such that $\varphi^i_{in}$ holds at $j$, we prove that an implementation following the construction guarantees that $v_{out}$ remains true, thereby satisfying the Global part ($G$).

- For time $0$ to $i-1$, the monitor component generates false, due to “$\wedge_{z=0...i-1} X^z \neg \text{out}$” in realizing the specification $G(\chi^i_{in} \leftrightarrow X' \text{out}) \wedge \wedge_{z=0...i-1} X^z \neg \text{out}$.
- For time $i$ onwards, the output of a monitor is governed by whether $\chi^i_{in}$ is true or false. As $\beta j$ such that $\varphi^i_{in}$ holds at $j$, and $\chi^i_{in}$ is a formula in the DNF of $\varphi^i_{in}$, $\beta j$ such that $\chi^i_{in}$ holds at $j$; thus the output of each monitor is always false.
- For InUB, it produces “-” after receiving a true in its input port. Before that, it produces true in its output port. As InUB never receives input with value true, the generated output value is always true. Due to the dataflow, $v_{out}$ is always true. Thus $Gv_{out}$ holds.

(B, Specification Type 2) (Informal sketch; to ease understanding) The proof strategy is similar. Essentially the property can be viewed as Type 3 where the right-hand part of the implication is replaced/nested by a Type 1 specification. When the triggering of left-hand part (the input part) appears at time $t$, based on the formula one needs to “start” the monitor which constitutes the release part. As “starting a monitor” is not possible, an alternative is to perform proper reset such that it appears at time $t$. As our monitor is designed not to take reset signals (this is to facilitate monitor reuse among multiple specifications), one can alternatively achieve the same effect by the introduction of $C_{\Theta_h}$, which contains the mechanism to set consecutive $h$ outputs to be false, whenever its input port set receives value true.

C General Properties for GXW Synthesis

As each individual specification of {P1, P2, P3, P4} is trivially realizable, the reason that lead to unrealizability is (1) simultaneous true and false demanded by different sub-specifications, (2) violation of properties over output variables (type P5), which are invariance properties over output variables. Notice that our method, as it generates structured controller, can also report unknown when there exists a feedback loop in the constructed system, i.e., when output variables listed in the release part of P2 create a need for simultaneous reasoning over two or more output variables. It is only a restriction imposed on the controller structure and is not the reason for unrealizability.

Therefore, as unrealizability of a GXW specification is due to (1) and (2), one can construct a counter strategy by first constructing a tree which provides input assignments that lead to undesired states violating (1) or (2), then all tree leaves violating (1) or (2) are connected to a self-looped final state, in order to accept $\omega$-words created by inputs and outputs. As the input part listed in Table 1 does not involve any output variable, a counter-strategy, if exists, can lead to violation of (1) or (2) within $\Omega$ cycles, where $\Omega$ is a number sufficient to let each input part of the sub-specification be true in a run.

Lemma 1. For GXW specification $\rho \rightarrow \wedge_{m=1...k} \eta_m$, if (a) $p^0_{out}$ is false for all $\eta_m$ of type P2 and (b) no specification of type P5 exists, then if the specification is not realizable, then there exists a counter-strategy which leads to violation of (1) or (2) in $\Omega$ steps, where $\Omega$ is bounded by the sum of (i) the number of specifications $k$, and (ii) the sum of all $i$ value defined within each $\phi^i_{in}$ of $\eta_m$.

(Note) With the constraint where $p^0_{out}$ is always false, it is impossible to create feedback loops during the construction, as feedback loops are created due to the connecting output to the monitoring subsystem which corresponds to the release part of a formula.

Proof. When $p^0_{out}$ is false for all $\eta_m$ of type P2, then for type P2 specification, locking the output to $\eta_{out}$ and the release of the locking is completely determined by two input events $\phi^0_{in}$ and $\varphi^j_{in}$. Similarly, for specifications of type P1, P3, P4, whether output is locked to $\eta_{out}$ is decided by $\phi^i_{in}$.
Consider the simplest case with two specifications \( \tau_1 := G(\phi_{in,1}^i \rightarrow X^i(\varphi_{out,1}^j W \varphi_{in,2}^j)) \) and \( \tau_2 := G(\phi_{in,2}^{i+1} \rightarrow X^{i+1}(\varphi_{out,2}^j W \varphi_{in,2}^j)) \). Let \( \varphi_{out,1} \) be \( out_1 \) and \( \varphi_{out,2} \) be \( \neg out_1 \). Thus these two specifications can lead to conflicts (\( \tau_1 \) demanding \( out_1 \) to true while \( \tau_2 \) demanding \( out_1 \) to false). Consider a finite time window of size \((i_1 + 1) + (i_2 + 1)\). It is sufficiently large to first (from time 0 to \( i_1 \)) make \( \phi_{in,1}^i \) true, and subsequently (from time \( i_1 + 1 \) to \( i_1 + 1 + i_2 \)), let \( \phi_{in,2}^{i+1} \) be true. Then if \( \varphi_{in,1}^i \) is always false in between (from time \( i_1 \) to \( i_1 + 1 + i_2 \)), a counter-strategy is created within length \((i_1 + 1) + (i_2 + 1)\). The overall concept is demonstrated in Figure 9.

**Fig. 9.** A timeline describing the time windows required to produce conflict at time \( i_1 + 1 + i_2 \).

For the case in Figure 9, the sufficient and necessary condition for producing conflict is to keep \( \varphi_{in,1}^i \) always false from time \( i_1 \) to \( i_1 + 1 + i_2 \). That is, if within time \([i_1, i_1 + 1 + i_2]\), when the environment provides a sequence of inputs to make \( \phi_{in,2}^{i+1} \) true, the sequence will also make \( \varphi_{in,1}^i \) true, then it is impossible to create a counter strategy. Similarly, one can reverse the ordering of events by first making \( \phi_{in,2}^{i+1} \) true followed by making \( \varphi_{in,1}^i \) true; the sufficient and necessary condition for producing conflict is to keep \( \varphi_{in,2}^{i+1} \) to false from time \( i_2 \) to \( i_2 + 1 + i_1 \). In both cases, a time horizon \((i_1 + 1) + (i_2 + 1)\) is sufficient to demonstrate the existence of a counter-strategy.

One can also replace \( \tau_1 \) and \( \tau_2 \) by any specification pattern in \{P1, P2, P3, P4\}, and the bound \((i_1 + 1) + (i_2 + 1)\) is still sufficient. Lastly, by generalizing the result to \( k \) specifications, we have derived the bound \((i_1 + 1) + (i_2 + 1) + \ldots + (ik + 1)\).

Lemma 1 is based on the premise where no specification is of type P5, while input and release parts in Table 2 are only controlled by input variables. When no constraints are imposed to output variables due to input events, an implementation can freely select output variable assignments, as it can neither influence release nor violate properties type P5. Therefore, when checking the existence of a counter-strategy, there is no need to use quantifier alternation, thereby making the synthesis problem easier.

**Lemma 2.** For a GXW specification under constraint of Lemma 1 deciding whether the specification is realizable is in co-NP.

**Proof.** (A) We first argue that the construction after Step 1, 2, and 3 whether an input of a resolution block is to true or false (i.e., not "¬") is only controlled by input events.

- For specification P3, the high-level controller outputs – once when its input receives a false, but monitor component only sends true when \( \phi_{in}^j \) turns true. Therefore, an input of a resolution block is to true or false (i.e., not "¬") only when needed.

- For specification P1, the high-level controller continuously outputs – once when its input receives a true, and before that, it outputs true. But monitor component only sends true when \( \phi_{in}^j \) turns true, and before that (from 0 to \( i-1 \)), the monitor sends false.

- Specification P2 is a combination of P3 and P1.

- For specification P4, the monitor component is connected directly to Resolution Actor; it only sends true or false when \( \phi_{in}^j \) turns true or false and before that (from 0 to \( i-1 \)), the monitor component sends – (dc = true).

(B) Using the result in Lemma 1, one can perform a bounded unroll over the generated actor system from Step 1, 2, and 3 in order to check if there exists a counter-strategy. This is because for the
Lemma 3. For GXW specification \( \varphi \rightarrow \bigwedge_{m=1\ldots k} \eta_m \), if the specification is not realizable, then there exists a counter-strategy which leads to violation of (1) or (2) in \( \Omega \) steps, where \( \Omega \) is bounded by the sum of (i) the number of specifications \( k \), and (ii) the sum of all \( i \) value defined within each \( \phi^i_m \) of \( \eta_m \).

The number of constraints created in each unroll can be understood by how data is flowed from source to destination, which follows the ordering (here we omit the logic gates): external input ports \( \Rightarrow \) monitor controllers \( \Rightarrow \) skeleton controllers \( \Rightarrow \) resolution actors \( \Rightarrow \) external output ports. Evaluating constraints in single cycle takes time linear to the number of actors, and evaluating \( \Omega \) = \( (i_1 + 1) + (i_2 + 1) + \ldots + (i_k + 1) \) steps using index 0, \ldots, \( \Omega \) (line 5 for using \( \alpha \) to iterate over 0, \ldots, \( \Omega \)).

As for each output variable \( v_{out} \), the existential variable \( Res\_{v_{out}}.A \) can neither influence release nor violate properties type P5 (due to the restriction stated in Lemma 4), one can simply set it to true. Therefore, the constraint system with one quantifier alternation is simplified to checking the validity of a quantifier-free Boolean formula, or equivalently, checking the existence of an assignment to make the quantifier-free formula false.

As running one cycle requires time linear to the number of actors and wires, which is bounded by length of the complete specification formula, deciding whether the specification is unrealizable is in co-NP.

(C) The result follows the fundamental property of LTL synthesis - an LTL specification is either realizable or unrealizable. As deciding whether the specification is unrealizable is in co-NP, the dual problem of whether the specification is realizable can be decided in time co-NP.

(Remark) We can also analyze the number of variables and the number of clauses created in each unroll. Those numbers are timed with \( \Omega = (i_1 + 1) + (i_2 + 1) + \ldots + (i_k + 1) \) to derive the total number of variables and clauses.

- For all global input and output ports, they are encoded as variables.
- For each resolution block, it takes at most \( k \) inputs, so at most \( 2k \) variable is needed (a factor of 2 is due to the use of \( \neg \)). The output of a resolution block can be syntactically replaced by the corresponding global output port.
- For each specification \( \eta_m \):
  - Implementing each \( \chi^i_{in} \) of \( \phi^i_m \) uses variables of size \( i \) times the number of input variables in \( \chi^i_{in} \). For type P4, one adds a counter for counting \( i \) steps. Thus for \( \eta_m \), one at most uses \( i_m |V_{in}| + \log_2(i_m) \) variables.
  - Similar estimation holds as an upperbound for the release part of specification type P2, but there is a need to add state variable of \( \Theta_j \). Thus a conservative estimation is \( j_m |V_{in}| + 2 \times \log_2(j_m) \).
  - A high-level control block uses at most two state variables, and has at most four ports. Each port is modeled as a variable.
  - All input ports of event monitor (for monitoring \( \chi^i_{in} \)) can be syntactically replaced by global input ports. All inputs of a OR-gate can be syntactically replaced by the output port of an event monitor or global output ports. The output of a OR-gate can be syntactically replaced by the input port of a high-level block.

Therefore, the total number of variables is bounded by

\[
\Omega(|V_{in}| + |V_{out}| + \sum_{m=1\ldots k} (2k|V_{out}| + (i_m|V_{in}| + \log_2(i_m)) + (j_m|V_{in}| + 2 \times \log_2(j_m)) + 6))
\]

The number of constraints created in each unroll can be understood by how data is flowed from source to destination, which follows the ordering (here we omit the logic gates): external input ports \( \Rightarrow \) monitor controllers \( \Rightarrow \) skeleton controllers \( \Rightarrow \) resolution actors \( \Rightarrow \) external output ports. Evaluating constraints in single cycle takes time linear to the number of actors, and evaluating \( \Omega \) = \( (i_1 + 1) + (i_2 + 1) + \ldots + (i_k + 1) \) rounds takes polynomial time. Therefore, given an assignment over all variables, deciding whether the formula is violated is done in polynomial time.

The following result shows that, the bound is still valid even without the above mentioned restriction.
Proof. For general GXW, the effect of enabling output variable to certain value within a given time point $\alpha$ is not carried to time point $\alpha + 1$, as no $X$ is bundled with any output variable in the specification.

We again refer readers to Figure 9. Now, view the control of output variables being governed by an imaginary SAT solver. In each time point, the produced output assignments should satisfy invariance properties of P5, while being constrained by the locking condition. When possible, it tries to produce output assignment that turns $\rho^{0}_{out}$ to true, such that the output is no longer constrained to $\varrho_{out}$. For example in Figure 9, starting from time $i_1$, the SAT solver has independently $i_1 + 1$ opportunities to make the release part to true. If it succeeds, then conflict does not appear. Otherwise, counter strategy is produced latest at time $i_1 + 1 + i_2$.

Lemma 4. For a GXW specification, deciding whether the specification is realizable is in PSPACE.

Proof. We check if the specification is not realizable $S$ by the following: non-deterministically provide input variable assignments for $(i_1 + 1) + (i_2 + 1) + \ldots + (i_k + 1)$ times, and check for all output assignments for $(i_1 + 1) + (i_2 + 1) + \ldots + (i_k + 1)$ rounds, it is possible to violate the specification. Checking whether it is possible to violate the specification can be done in PSPACE: The process is similar to the above unroll case, but for each variable $v_{out}$, instead of setting $Res_{v_{out}}A$ to true, we simply let output variable to process $(i_1 + 1) + (i_2 + 1) + \ldots + (i_k + 1)$ different copies, meaning that one can freely select the value in each round. The total memory used is $((i_1 + 1) + (i_2 + 1) + \ldots + (i_k + 1))|V_{out}|$, which is polynomial to the problem size.

Then given input assignment for $(i_1 + 1) + (i_2 + 1) + \ldots + (i_k + 1)$ rounds, one can use the memory to check if for all possible output variable assignments of they all unfortunately lead to conflict. If so, then report that the specification is not realizable. Therefore, deciding whether the specification is unrealizable is in NPSPACE (non-deterministic input assignment + PSPACE complexity for checking if conflict appears).

As NPSPACE = DPSPACE = PSPACE, and an LTL specification is either realizable or unrealizable, deciding whether the specification is realizable is in PSPACE.

Notice that although the complexity for checking if a GXW specification is realizable is in PSPACE, the algorithm presented previously only sets every $Res_{v_{out}}A$ as a constant that does not change over time. This creates a simpler structure for the implemented controller. Soundness is still guaranteed by performing an unroll to the above mentioned bound.
Step 5: Generating 2QBF constraints for bounded unroll

Input: LTL specification $\phi = \varrho \rightarrow \bigwedge_{m=1}^{k} \eta_{m}$, input variables $V_{in}$, output variables $V_{out}$, partial controller implementation $S = (V_{in}, V_{out}, Act, \tau)$ with unknown parameters, integer unroll bound $\Omega$

Output: 2QBF constraint $(V_{\exists}, V_{\forall}, \Upsilon)$, where $V_{\exists}$ and $V_{\forall}$ are sets of Boolean variables, and $\Upsilon$ is a quantifier free constraint over variables in $V_{\exists} \cup V_{\forall}$

1. let $T_{a}, T_{g} := true$;
2. let $V_{a}, V_{r} := \text{NewEmptySet}();$
3. foreach $v_{out} \in V_{out}$ do $V_{a} := V_{a} \cup \{Res_{v_{out}}, A\}$
4. let $\Xi$ be the evaluation ordering of $S$;
5. for $\alpha = 0 \ldots \Omega$ do
6.    foreach $\xi \in \Xi$ do
7.        if $\xi \in \tau$ then
8.            /* $\xi$ is w wire; encode biimplication among two ports */
9.                Let $\xi$ be (source $\rightarrow$ dest);
10.               $V_{r}.add(source_{\alpha})$;
11.               $V_{r}.add(dest_{\alpha})$;
12.               $T_{a} := T_{a} \land (source_{\alpha} \leftrightarrow dest_{\alpha})$;
13.        else
14.            /* $\xi$ is an actor; encode transition using index $\alpha$ and $\alpha + 1$ */
15.                $V_{r}.add(GetStateVariable(\xi, \alpha))$;
16.                $T_{a} := T_{a} \land (\text{EncodeTransition}(\xi, \alpha))$
17.                $T_{a} := T_{a} \land (\text{VariableReplace}(\varrho, \alpha))$
18. for $v_{out} \in V_{out}$ do
19.    $T_{g} := T_{g} \land (\neg k : (Res_{v_{out}, a}.input_{i} = true) \land (Res_{v_{out}, a}.input_{j} = false))$;
20. foreach $\eta_{m}, m = 1 \ldots k$ do
21.    $p := \text{DetectPattern}()$;
22.    if $p \in \{P5\}$ then $T_{g} := T_{g} \land \text{VariableReplace}(\eta_{m}, \alpha)$
23. /* Add initial condition, to achieve bounded unroll */
24. foreach $\xi \in \Xi$ do
25.    if $\xi \notin \tau$ then
26.        /* $\xi$ is an actor; encode initial state with index 0 */
27.            $T_{a} := T_{a} \land (\text{EncodeInitialState}(\xi, 0))$
28. return $(V_{a}, V_{r}, T_{a} \rightarrow T_{g})$