Run-time Performance Monitoring of Heterogenous Hw/Sw Platforms Using PAPI

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Abstract

In the era of Cyber Physical Systems, designers need to offer support for run-time adaptivity considering different constraints, including the internal status of the system. This work presents a run-time monitoring approach, based on the Performance Application Programming Interface, that offers a unified interface to transparently access both the standard Performance Monitoring Counters (PMCs) in the CPUs and the custom ones integrated into hardware accelerators. Automatic tools offer to Sw programmers the support to design and implement Coarse-Grain Virtual Reconfigurable Circuits, instrumented with custom PMCs. This approach has been validated on a heterogeneous application for image/video processing with an overhead of 6% of the execution time.

1 Context and Objectives

Cyber-Physical Systems (CPS) are complex systems, composed of different components characterized by a strong interaction with environment and users. In particular, they need to adapt their behaviour according to the environment, any user requests and also their internal status \cite{1}. The H2020 CERBERO European Project \cite{2, 3} is developing a continuous design environment for CPS, relying on a set of tools developed by project partners. Effective support for run-time adaptation in heterogeneous systems, taking into account a plethora of different internal and external triggers, is among the CERBERO expected outcomes, and a fundamental step is monitoring the hardware (Hw) and software (Sw) elements of the heterogeneous system \cite{4}. This paper focuses on one fundamental step necessary to design self-adaptive systems: the monitoring of heterogeneous architectures, where processing cores are connected to custom hardware accelerators that can be reconfigured at run-time. One of the Hw reconfigurable infrastructures supported in CERBERO is the Coarse-Grain Virtual Reconfigurable Circuits (CG-VRCs) \cite{5}. CG-VRCs offer fast and low power reconfiguration, with a good trade-off between performance and flexibility, being suitable for providing run-time Hw adaptation. In these kinds of systems, all the resources belonging to all the configurations are instantiated in the substrate and different configurations are enabled by multiplexing resources in time \cite{6}, they can be implemented on both Field Programmable Gate Array (FPGA) or Application Specific Integrated Circuit (ASIC) systems. These kinds of accelerators are suited to support:

1. \textit{Functional oriented adaptivity}: the application is able to execute different functionalities over the same substrate (e.g., algorithm changes) \cite{7}.

2. \textit{Non-functional oriented adaptivity}: the application is able to execute only one functionality, but with different performance (e.g., the precision of a filter could be reduced to save energy) \cite{8}.

In CERBERO, the Multi-Dataflow Composer (MDC) \cite{9} tool automates the development of CG-VRCs. Users describe the applications to be accelerated as dataflows and MDC automatically merges them through a datapath merging algorithm, generating a Xilinx-compliant IP with its drivers to delegate computing tasks to the coprocessor \cite{10}. The first step to enable a feedback loop that allows for the design of self-adaptive CPS, consists of instrumenting the system with monitors to capture its internal status changes \cite{4}. The most extended Sw approach for enabling self-awareness is based on accessing the existing Performance Monitoring Counters (PMCs) of modern CPUs. On the other hand, a Hw accelerator can be specialized by the designer to include custom monitors. This second solution is not suitable for Sw developers who may have limited knowledge of the Hw design flow. Furthermore, if these solutions rely on custom methods to read the monitors, the process of reading the monitors in the Hw accelerators and the PMCs already available on the CPU could not be the same, and heterogeneity of solutions, complex to be implemented, may be required. In CERBERO, PAPIFY \cite{11, 12} provides a lightweight monitoring infrastructure by means of an event library aimed at generalizing the Performance Application Programming Interface (PAPI) \cite{13} for embedded heterogeneous architectures.

In a previous work \cite{14} we proposed the idea of using PAPIFY in combination with MDC to offer support for the
design, implementation and monitoring of run-time reconfigurable systems, as the CG-VRCs, using PAPIFY. In that work we presented a PAPI-compliant component that could be automatically configured with events information using an XML file. The work presented in this paper relies on the idea of offering to Sw developers the support to design and implement run-time reconfigurable systems and to monitor both the processor and the Hw accelerator using a unified methodology based on PAPIFY. Being in a heterogeneous-core computing era, a unified methodology allows a fairer comparison of Hw and Sw performance and facilitates the performance analysis in terms of debugging (e.g., monitor the correct execution of internal modules) and optimization (e.g., monitoring of CG-VRC allows for prospectively switching among different configuration if the users require better performance).

- In this work the MDC tool has been extended to provide automatic instrumentation of the CG-VRCs with custom PMCs and to automatically generate the XML file necessary to automatically configure the previous developed PAPI-component. This automatic flow allows Sw programmers to define the applications to be accelerated and instrumented as dataflow descriptions, without the need of any Hw knowledge.

- The Application Programming Interfaces (APIs) provided by MDC, in combination with the Sw libraries provided by PAPIFY, offer the transparent PAPI-compliant access to the Hw PMCs.

- The monitoring of heterogeneous Hw/Sw systems is a mandatory step to allow self-adaptation of CPS. Nevertheless, in this preliminary exploration the design under test is not a CPS one. Assessment on a processor-coprocessor system for image processing, validates the automatic design flow, the monitoring PAPI-based approach and the effectiveness of PAPIFY on heterogeneous Hw/Sw systems.

The paper is organized as follows: Section 2 explores the solutions at the state of the art, Section 3 presents the proposed Hw/Sw unified monitoring approach together with the exploited tools, and Section 4 presents a proof of concept evaluation of the effectiveness of the approach. At the end, Section 5 summarizes and concludes the paper with some directions for future works.

2 Related Works

In literature, several works have dealt with the issue of monitoring Sw and Hw systems to gather relevant data on the system status and its performance for run-time evaluation and/or adaptivity purpose. In particular, PAPI provides a unified method to access the PMCs available on the CPUs [13]. The PAPI community is big, and there are several research works. For instance, Adhianto et al. [15] proposed a sampling monitoring infrastructure based on PAPI applied to High-Performance Computing systems, and Knüpfer et al. [16] focused on providing a graphical interface to analyze trace data based on already completed application executions. While PAPIFY generalizes PAPI for embedded heterogeneous architectures [11].

To implement self-aware run-time Hw adaptation, a proper instrumentation of the target substrate with monitors is necessary. Various examples of monitoring solutions are available at the state of the art, for instance, in the AMD64 [17] and Intel [18] processors. The AMD64 [17] presents a Lightweight Profiling (LWP) extension to allow user mode processes to gather run-time performance data with very low overhead, while the Intel Processor Trace (IPT) [18] offers Hw performance counters and Sw able to use information acquired at low-level.

Other works focus on the custom instrumentation of existing Hw architectures. Schmidt et al. [19] proposed Hw Performance Monitoring Interface, which involves the insertion of performance monitoring networks into existing Hw designs, and Patrigeon et al. [20] presented an FPGA-based platform, instrumented with monitors, for real-time evaluation of Ultra Low Power Systems on Chip. While Valente et al. [21, 22] defined a custom profiling system for embedded applications and a library of elements to compose a Hw profiling system for specific applications. Generally speaking, Sw developers do not have deep knowledge of the Hw design flow and, to ease their access to run-time data, Application Program Interfaces (APIs) should be offered them. APIs are a perfect solution to

- hide the details behind the definition and customization of dedicated monitoring infrastructures; and

- ease the usage of Sw monitoring calls in the application.

The Xilinx SDC Development Environment gives users the possibility to use counters in ARM Cortex A9 and performance monitoring units in programmable logic side [23]. While Shannon et al. [24] presented ABACUS, a performance-monitoring framework that can be used to debug the execution behaviours and interactions of multi-application workloads in reconfigurable logic scenarios. Some works have tried to exploit PAPI for Hw systems. For instance, Ho et al. [25] proposed a performance monitoring unit integrated with the perf_event API. Suriano et al. [26] presented a custom approach that uses PAPIFY for reading monitors of a Hw slot-based architecture that exploits Dynamic and Partial Reconfiguration [27].

With respect to above works, this paper proposes a generic PAPI-based approach for monitoring Hw accelerators, suitable also to enable the proper feedback of a CG-VCR architecture. In particular, we extended the MDC tool to automatically instrument with custom PMCs the generated Hw accelerators, providing the necessary Sw support to monitor both Sw and Hw Processing Element (PEs) through the same interface, PAPIFY.

3 Toolchain for Heterogeneous Monitoring

This section presents the toolchain for the development, implementation and management of monitored heterogeneous platforms. Section 3.1 depicts the design flow of
MDC tool, Section 3.2 illustrates the run-time monitoring capabilities of the PAPIFY Tool, and Section 3.3 presents the proposed monitoring approach. Indeed, a set of definitions must be clarified in advance:

- **Dataflow (DF):** an application represented as a set of functional elements, *the actors*, exchanging data, the *tokens*, through a set of communication links, the *edges*.
- **Actor:** univocal functional element, encapsulating a given functionality or operation, in which a dataflow application is divided.
- **Edge:** exclusive interconnection between two actors implemented as a FIFO.
- **Processing Element (PE):** Hw resource where one or more actors are scheduled for execution. It can be a Sw core or a complete Hw accelerator.
- **Functional Unit (FU):** custom implementation of one single actor instance inside the Hw accelerator. FUs can be manually defined or synthesized using High Level Synthesis tools.

### 3.1 The Multi-Dataflow Composer Tool

![MDC design flow](image)

A Hw design can be described as a modular composition of FUs. The same level of expressiveness can be given by a higher level representation, as a dataflow network, where each FU can be represented by an *Actor* of the network, through a 1:1 mapping. Several high level description, mapped on one unique Hw description, can represent a CG-VRC design. However, the mapping is not longer 1:1, but it becomes *N*:1, through the sharing of the common *Actor* and the insertion of ad hoc switching elements.

The Multi-Dataflow Composer (MDC) is an automated framework that generates heterogeneous and irregular CG-VRCs, through an application-to-hardware approach. Applications to be implemented are specified as XML Dataflow Format (XDF) models and combined through a datapath-merging algorithm that merges the input specifications and allows sharing the actors in common among the different dataflow applications. In the resulting multi-functional CG-VRC heterogeneous accelerator, in Verilog Hardware Description Language (HDL), the FUs are actor-specific. To access shared resources, multiplexers named Switching-Boxes (SBboxes) are inserted in the datapath. The user is required to model the applications to be accelerated as dataflows while MDC takes care of automatically generating the corresponding CG-VRC accelerator.

Top part of Figure 1 depicts an example of the MDC operation. Nodes of the networks (i.e., A, B, C, etc…) are *Actors*. The three input dataflow specifications are merged into a multi-functional dataflow, in which the switching elements (e.g., SB_0, SB_1, SB_2) guarantee the correct operation of the different functionalities. During the merging process MDC keeps also trace of the programmability of the switching elements (*C_TAB*). The Hw description of the single *Actors* (HDL Component Library) can be manually written or automatically generated by means of High Level Synthesis (HLS) tools, as for instance CAPH [29]. MDC properly connects them keeping into account handshake protocol among the FUs thanks to the communication protocol specified as input file (*protocol*).

MDC also offers the possibility of seamlessly integrating the CG-VRC logic into a processor-coprocessor system for Xilinx environments [10]. By analyzing the features of the combined dataflow specifications, suitable wrappers for different processor-coprocessor communication infrastructures (memory-mapped or stream) are automatically provided. The bottom part of Figure 1 shows the resulting CG-VRC embedded in the Xilinx IP generated by MDC. MDC also provides the APIs to delegate computation to the coprocessing unit and manage processor-coprocessor communication, masking the system configuration complexity, providing a C function for each configuration of the CG-VRC coprocessor that allows the user to access the accelerator transparently, without taking care of the implementation of data transmission according to the implemented bus protocol. The Listing 1 shows the interface for one configuration of a memory-mapped CG-VRC coprocessor computing the Roberts edge detection algorithm. *data_<port_name>* and *size_<port_name>* are respectively input (or output) port and the number of data related to that port. In the considered example there are three ports: *in_size*, *in_data* and *out_data*.

#### Listing 1 Coprocessor drivers interface.

```c
//Memory-Mapped Interface Driver
int mm_accelerator_roberts(
    // port out_data
    int size_out_data , int* data_out_data ,
    // port in_data
    int size_in_data , int* data_in_data ,
    // port in size
    int size_in_size , int* data_in_size ) ;
```

The underline C code manages the co-processor configuration and data transfer. For each I/O port of the reconfigurable computing core, a configuration word...
Figure 2 PAPIFY configuration using PREESM.

(size_in_size, size_in_data, size_out_data) is written into the proper co-processor register. Then, for each input port involved in the current computation, a specific primitive is used to send the data (data_in_size, data_in_data) to be computed from the host processor to the co-processor. At last, a specific primitive is adopted to read back the results (data_out_data) into the processor from the output ports.

3.2 The PAPIFY Tool

PAPIFY [11] is a tool aiming at easing the instrumentation and PAPI-based monitoring of applications. In order to use it, a dedicated library called eventLib is available. This library is composed of 9 functions and is built on top of PAPI. With this library, the user only needs to include a set of functions at the beginning of the application where all the monitoring is configured. Additionally, both the PE (i.e., a physical Sw core or an accelerator) and the actor (functional block) configurations are isolated from each other. During the configuration of the PE monitoring, the available PAPI components are linked to the corresponding PEs. Secondly, the configuration of the actors is performed associating events contained in any PAPI component to it. Once the monitoring configuration is included, the user only needs to set the starting and stopping points for the monitoring. By doing so, the instrumentation of the code will be complete and, independently of the PAPI component that is accessed and the PE that is executing the actors, the structure of the monitoring will be homogeneous. Regarding the behaviour in execution time, PAPIFY manages the different configurations for PEs and actors combining them in a completely transparent way to the user. That is, it automatically selects the PAPI events that are available for the specific PE and stores the results accordingly. Additionally, PAPIFY stores the configurations that have been already set up during one execution in order to reuse it, hence, reducing the monitoring overhead.

Listing 2 depicts an example of code necessary to instrument an application using PAPIFY. The user can monitor the application instrumenting the code by hand or automatically, thanks to the integration of PAPIFY with a dataflow development framework called PREESM [30]. PREESM provides automatic code generation of dataflow applications and, together with PAPIFY, automatic code instrumentation is provided to the user. The user only needs to fill a graphical configuration as the one shown in Figure 2 following the same organization shown in Listing 2.

Listing 2 PAPIFY usage example.

```
// Initial monitoring configuration
configure_papify_PE(char* coreName, char* PAPIComp, int PEid);
configure_papify_actor(&papify_action, char* PAPIComps, char* actorName, int numOfEvents, char* eventNames, char* configIDs, int numConfigs);
// Monitoring
event_start(&papify_action, int PEid);
actor_to_be_monitored();
event_stop(&papify_action, int PEid);
```

The run-time use of PAPIFY in the context of reconfigurable dataflow, as the one of the SPIDER tool [31], is graphically explained in Figure 3. As can be seen, the process is divided into five steps:

1. **Schedule Actors**: a master process is in charge of scheduling the actors composing the dataflow application.
2. **Send Order**: the master process maps the application actors over the available slave PEs (either Sw cores or Hw accelerators).
3. **Fire Actors**: PEs execute the scheduled actors and, during these executions, the PAPI events are retrieved using PAPIFY.
4. **Exchange Dataflow Tokens**: PEs, according to the application flow, exchange tokens.
5. Retrieve Performance Information: Once the whole application has been executed, the performance data is retrieved by the master process together with timings and application parameters. This will enable the master process to take re-mapping and scheduling decisions based on this new information.

### 3.3 Proposed approach

The proposed approach relies on the integration of PAPIFY and MDC, to provide a toolchain able to offer the support in the process of designing, implementing and managing monitored CG-VRCs. PAPIFY provides an interface to access performance monitoring information of the different PEs existing in the target platform. As PAPI is built based on components, i.e., each resource is isolated from each other to separate also the low-level details of each HW resource) PAPIFY automatically inherits this structure. Nevertheless, this new tool has been built to transparently manage the monitoring configuration independently of the nature of the PE executing each part of the application.

Figure 3 PAPIFY in a dataflow context.

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Figure 4 Hw/Sw monitoring infrastructure, with custom PAPI component and PMCs for MDC.

Figure 4 illustrates the PAPI-based monitoring infrastructure. At the Application Layer the user only needs to specify the application as dataflow and instrument it with the PAPIFY calls. On the bottom, the Hardware Layer presents the PMCs for both the host processor (CPU PMCs) and the HW accelerators on the FPGA (MDC PMCs). At the Library Layer, the PAPI components are the C interface between the high-level user Application Layer and the Hardware Layer and take care of accessing the PMCs. To ease both the configuration and the management of the monitoring, including the transparent access to the PAPI components associated with either Sw or HW PEs, PAPIFY offers the eventLib Library. Enabling the monitoring of the HW CG-VRCs using PAPIFY, required to develop both a PAPI component and the PMCs suitable for MDC.

As mentioned in Section 1 in modern CPUs there are built-in PMCs to monitor various kinds of events, while on HW accelerators it is necessary to rely on custom solutions. Figure 5 illustrates an MDC-generated IP, instrumented with monitors. This memory-mapped IP communicates with the host processor (not shown in Figure 5) through the System Bus. The MDC CGR Accelerator is connected to the System Bus by means of a memory bank (Local Memory) to exchange data between the processor and the coprocessor, and through a register bank (Configuration Registers) to send the words necessary to configure the coprocessor. In this IP the monitors are placed at two levels of abstraction:

1. accelerator-level: this monitoring, placed outside the MDC CGR Accelerator, is homogeneous for every accelerator that can be implemented using MDC. It keeps trace of standard dataflow metrics during execution, such as the execution time, the number of input tokens and the number of output tokens.

2. low-level: this monitoring, placed inside the MDC CGR Accelerator, is specific for the current accelerator, e.g. by profiling the bottleneck FUs internally.

The accelerator-level monitors are automatically inserted by MDC, while at the moment the low-level monitoring still requires manual steps to be used within the IP. In both cases, the HW monitors are accessed by the host processor through the Configuration Registers of the IP.

![Figure 5 Hw Monitoring at two levels of abstraction: (1) accelerator level; (2) low-level.](image)
erator under evaluation are loaded, the PAPI-MDC component is automatically configured, using a configuration XML file, as the one depicted in Listing 3. In the current XML file the user shall specify the physical base address of the accelerator to be monitored (baseAddress), the number of available events (nbEvents) and their type (event), but this approach can be easily extended to consider other variables. This kind of monitoring is transparent for the user, that only needs to insert the APIFY call in the Sw application.

Listing 3 Configuration file for the PAPI component.

```xml
<mdcInfo>
  <baseAddress>0xADDRESS</baseAddress>
  <nbEvents>N</nbEvents>
  <event>
    <name>MDC_EVENT_NAME</name>
    <desc>Event Description</desc>
  </event>
</mdcInfo>
```

The heterogeneous Hw/Sw system that can be monitored with such approach is a SoC platform like the ones provided by the Xilinx Zynq family, in which the chip includes both one or more processors and a programmable logic part. The board requires to run Linux, in which are installed APIFY and PAPI (that needs to include the PAPI-compliant MDC-component).

The Hw accelerator is modelled starting from a set of XDF dataflow networks that are parsed by MDC to generate a Xilinx-compliant IP able to execute all the different functionalities described by the input dataflow specifications, one at a time (see Section 4.1). MDC also generates the C APIs to mask the communication between the processor and the coprocessor. Thanks to the extension of MDC, the user can specify to instrument the generated Verilog HDL code to incorporate the accelerator-level monitors above described and to generate the XML file necessary to configure the PAPI-compliant MDC-component. This Hw accelerator is used by a Sw C/C++ application, that can be either manually developed or modelled as a PiSDF specification using the APIFY-PREESM-SPIDER flow described in Section 3.2, that automatically integrates the APIFY monitoring code.

When the application is launched the PAPI-MDC component is automatically configured using the generated configuration XML file described above. The PAPI components access the PMCs and APIFY collects the data and save them into csv files that can be analyzed using APIFY-VIEWER.

4 Assessment

In this Section, as a proof of concept, the proposed monitoring approach and toolchain is evaluated through an application for Image Processing, involving a multifunctional accelerator for edge detection, able to compute two different algorithms: Sobel and Roberts. The system is based on the Zynq-7000 XC7Z020CLG484-1 device running Linux. It is composed of a Sw Application, mapped among the two ARM Cortex A9 cores available on the adopted board, that acquires an input video (Section 4.1.1) and of a Hw accelerator, implemented on the Programmable Logic of the FPGA, to compute the edge detection (Section 4.1.2).

4.1 Design Under Test

Edge detection algorithms estimate the magnitude and the orientation of edges on an image [29]. In this proof of concept we adopted discrete first-order differentiation operators, in which the boundary of an object is the difference of the intensity levels in its pixels with respect to the surrounding pixels. These operators are applied to evaluate the gradient image (G), that corresponds to the magnitude of the edge. The computation consists of a convolution of a 3x3 kernel (k) with the source image (A) for Sobel, while for Roberts k is 2x2: \[ G = k \ast A \] Graphically illustrates the convolution operation necessary to compute Roberts algorithm. For a complete description of the adopted Edge Detection algorithms please see [33]. Both the Sw and the Hw parts of the system are modelled as dataflow networks, and are described more in details in the Section 4.1.1 and Section 4.1.2.

4.1.1 Sw Application

The Sw application has been designed using a Parameterized Interfaced Synchronous Dataflow (PiSDF) specification and the toolchain composed of the design-time tool PREESM [30] and the run-time manager SPIDER (integrating the automatic code generation of APIFY monitoring). In this context, actors exchange tokens through edges depending on the feasible working points of the application scenario. The configuration parameters established at design-time and run-time are respectively called static and dynamic. The latter ones imply on-the-fly re-scheduling and re-mapping when their values change. The use-case algorithm depicted in Figure 7 can be described as follows:

- Given as an input to the actor Read_YUV, a YUV video is read frame by frame, where the number of rows and columns correspond to height and width parameters respectively. Filtering is applied only to the Y component,
In this work the dataflow processed by MDC have been explained in Section 4.1.2. As described in CAPH language [29], considering, to implement the CG-VRC accelerator, the the design flow proposed in [34], which enables benefits compared to the main tools available in the market (e.g., Intel FPGA SDK for OpenCL [35] and Xilinx Vivado HLS [36]). Figure 8 depicts a schematic graph representation of the Sobel and Roberts kernels. The line buffer actors are adopted to store previous rows of the image, while delay actors are in charge of memorizing one previous pixel within a row. Once the actors are filled with the proper numbers of rows and pixels, the convolution actors can compute the horizontal and vertical gradients. Actor abs sum sums up the absolute values of the horizontal and vertical gradients and right-shifts the result for a given scaling factor n. Lastly, the thresholding actor thr sets to 255 all the magnitudes that are above a a threshold (in this case it has been fixed to 80), while setting to 0 the others. These dataflow specifications has been processed by MDC, to generate a CG-VRC able to compute both Sobel and Roberts algorithms, which has been automatically embedded into the ready-to-use Xilinx IP.

While the other ones are directly sent to be displayed.

- Before the edge detection, the block Split divides the image in slices depending on the degree of exploitable parallelism. In this assessment, having available one single Hw accelerator, no adaptation has been considered in this sense (nbSlice = 1, that is sliceHeight = height).

- At this point, verified the on-the-fly selected kernel (set by IdSetter) among Sobel and Roberts, an initialization phase is performed in EdgeMDC_1. In this phase, the processing data and the communication with the accelerator (through the Direct Memory Access) are handled.

- Then, processing occurs by blocks of pixels of a size suitable for the accelerator specifications (in the assessed example, 32 × 32). EdgeMDC_2 sends a number of blocks corresponding to width_blk × height_blk to the EdgeMDC_hw_filter, which forwards the data to the coprocessor. Therefore, EdgeMDC_3 receives the result of each iteration, which is collected in EdgeMDC_4.

- Finally, the filtered frame is merged and displayed with the applied type of kernel and the execution time expressed in Frames per Second (FpS).

With respect to the mapping strategy, SPIDER handles all Sw tasks taking into account the constraints given as input by the application designer. In the evaluated case, the actors performing splitting and merging have to be executed onto the same core. Moreover, SPIDER has managed 305 instances of the single-rate graph. Indeed, 8 actors are executed 1 time per firing, and 99 times the other 3 ones (EdgeMDC_2, EdgeMDC_hw_filter, and EdgeMDC_3), since 99 32 × 32 blocks are present in the frame size considered in this assessment (352x288 pixels). Regarding the actual filtering, this has been accelerated on Hw, as explained in Section 4.1.2.

4.1.2 Hw accelerator

As described in Section 4.1.1 MDC takes as input the dataflow descriptions of the applications to be accelerated. In this work the dataflow processed by MDC have been described in CAPH language [29], considering, to implement the CG-VRC accelerator, the the design flow proposed in [34], which enables benefits compared to the main tools available in the market (e.g., Intel FPGA SDK for OpenCL [35] and Xilinx Vivado HLS [36]). Figure 8 depicts a schematic graph representation of the Sobel and Roberts kernels. The line buffer actors are adopted to store previous rows of the image, while delay actors are in charge of memorizing one previous pixel within a row. Once the actors are filled with the proper numbers of rows and pixels, the convolution actors can compute the horizontal and vertical gradients. Actor abs sum sums up the absolute values of the horizontal and vertical gradients and right-shifts the result for a given scaling factor n. Lastly, the thresholding actor thr sets to 255 all the magnitudes that are above a a threshold (in this case it has been fixed to 80), while setting to 0 the others. These dataflow specifications has been processed by MDC, to generate a CG-VRC able to compute both Sobel and Roberts algorithms, which has been automatically embedded into the ready-to-use Xilinx IP.
4.2 Experimental Results

The described Sw application has been mapped onto two cores. Specifically, display and Read_YUV actors are mapped onto the Core 0 while the others are mapped onto the Core 1 of the adopted board. Among the actors mapped onto Core 1 three actors are repeated more than one time per firing: EdgeMDC_2, EdgeMDC_hw_filter, and EdgeMDC_3. These actors are executed for each 32 × 32 block of the frame (in our case we have 99 blocks). As explained in Section 4.1.1, the EdgeMDC_hw_filter takes care of communicating with the Hw accelerator to compute the edge detection. On the bases of the described design under test, three different configurations are evaluated.

- **DUT_1** - Hw/Sw system where the Hw accelerator includes the PMC, and both the Sw application and the Hw accelerator are monitored. In the Sw application the display and Read_YUV actors are selected for the monitoring of the clock cycles and number of instructions events, while in the Hw accelerator the monitored events are the execution time (clock cycles) and the throughput (number of output tokens).

- **DUT_2** - Hw/Sw system in which the Hw accelerator includes the PMC, but no monitoring is performed.

- **DUT_3** - The same than DUT_2 but without any PMC inside the Hw accelerator.

Table 1 reports, for Roberts execution, the performance of the different designs in terms of average (FpS). As expected the monitoring does not come for free, and the monitored design (DUT_1) has a performance loss of 6.20%, with respect to its no-monitored version (DUT_2). Specifically, this overhead is due to the fact that the application is executing a total amount of 305 actors in each iteration. Consequently, the same amount of lines are written in csv files that are provided to 1) analyze the application and 2) locate possible bottlenecks using PAPI components. Please, note that DUT_3 does not have any PMC, thus Table 1 does not report any overhead data.

For the sake of completeness, Table 1 also depicts the performance variation of the not monitored design, in which the accelerator embeds the custom PMCs (DUT_2), with respect to its equivalent version in which the Hw accelerator has no any monitor. In this case, the different performance (1.49%) are due not to Sw reasons, rather to the different Hw designs that, having a different number of configuration registers and different logic, can be synthesized in a different manner by Xilinx Vivado, leading to different performance in terms of access to the memory and the registers normally used to communicate with the accelerator. Finally, the events obtained through PAPI can be easily analyzed using its viewer, the so-called PAPI-FY.

As can be seen in Figure 9, the events obtained at run-time during the execution of Sobel-Roberts application can be analyzed one by one. First, in Figure 9a timing is monitored for every actor and, as can be seen, EdgeMDC_1, EdgeMDC_4 and Read_YUV are the actors taking longer. This is coherent with the reality because these three actors are the ones managing the whole frame. On the contrary, the actor being executed 99 times per iteration (EdgeMDC_hw_filter), is one of the fastest actors in the specification. Secondly, in Figure 9b and Figure 9c events associated to perf_event and MDC PAPI components are shown, respectively. In here, it can be observed that the events associated to the real execution of the Hw accelerator (EdgeMDC_hw_filter) are properly measured for the only actor associated to real Hw accelerator execution.

### Table 1: Performance of the three considered designs.

| Design       | FpS  | St. Dev | Overhead |
|--------------|------|---------|----------|
| DUT_1        | 11.03| 0.0489  | 6.20%    |
| DUT_2        | 11.76| 0.0138  | 1.49%**  |
| DUT_3        | 11.94| 0.0034  | —        |


4.3 Advantage of the Proposed Approach

It is important to highlight the effectiveness of the proposed flow in terms of design time and effort. The design of CG-VRCs requires to analyze the common resources of different dataflow specification, and to combine them, keeping trace of the Actors belonging to different functionalities and to program the multiplexers properly. Therefore, the manual design of CG-VRCs is time consuming and error prone. The proposed approach speeds-up and simplifies the design of monitored CG-VRCs by automatically mapping different input specifications in one MDC multi-flow IP, instrumented with monitors. The usage of dataflow specifications allows for the exploitation of HLS dataflow-to-hardware tools (such as CAPH [29]), which not only speed the design process up by automating HDL generation, but also allow developers that are not expert in Hw design to adopt the proposed approach. The users only need to define the applications through abstract high level input dataflow specifications; then, the toolchain takes care of the complete process from dataflow to the processor-coprocessor system. The generated APIs mask the complexity of the processor-coprocessor communication, and thanks to Sw-compliant MDC-PAPI component and the support for heterogeneous architectures provided by PAPIFY, the users can transparently access every monitor, by means of a call to a PAPIFY function. PAPIFY autonomously collect the data related to the monitored events and save them in csv files, offering to the user to post process them and to analyze them using PAPIFY-FY.

5 Conclusions and Future Works

This paper presented the combination of PAPIFY and MDC tools to support Sw developers in the design and implementation of Coarse-Grain Virtual Reconﬁgurable Circuits instrumented with custom monitors and integrated into a
Processor-Coprocessor System. The users specify the applications to be accelerated as dataflow specifications, and the automated toolchain deploys the final system together with the Application Programming Interfaces (APIs) to mask the processor-coprocessor communication. The combination of these APIs and of Sw Libraries provided by PAPIFY offer a unified approach for monitoring heterogeneous Hw/Sw platforms based on the Performance Application Programming Interface (PAPI), in which both Sw and Hw monitoring information can be retrieved in a transparent way.

Experimental evaluation demonstrates the effectiveness and the advantages of the proposed approach. Using this monitoring has an impact on the application performance of 6.20%, due to the fact that information are written into csv files. Indeed, the proposed approach is one of the mandatory steps to implement self-adaptive systems, but at the moment the collected data are not automatically fedback to any adaptation manager. When the monitoring information will be directly fed to the adaptation manager and not written into a file, this overhead would be potentially reduced and the system would be self-adaptive.

For instance, in the use-case adopted for the assessment, monitoring the latency would help to verify that the application is working properly. Once estimated, at the design time, that the application should complete in $x$ clock cycles, if after $3x$ the execution is not complete and the number of output tokens is less than expected, the manager could assume that the execution stacked for any reason and decide to reset and restart the application.

As a follow up, and to deal both with the overhead impact and the analysis of the information, all the monitoring data will be feeding SPIDER. By doing so, the low-level hardware information could be used to improve the workload distribution decision making carried out by this manager. This last step will close the loop and enable the self-adaption of a heterogeneous parallel system, integrating monitoring, decision making and reconfiguration capabilities [4].

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