An Optimized Space Vector Based Switching Algorithm With Reduced Switching Transitions for Impedance Source Inverter

SANTOSH SONAR\textsuperscript{1}, (Member, IEEE), SANJOY MONDAL\textsuperscript{2}, JAWHAR GHOMMAM\textsuperscript{3}, (Member, IEEE), AND SUBRATA BANERJEE\textsuperscript{4}, (Senior Member, IEEE)

\textsuperscript{1}Department of Electrical and Instrumentation Engineering, TIET, Patiala, Punjab 147004, India  
\textsuperscript{2}Department of Electrical Engineering, Institute of Engineering and Management, Kolkata 700091, India  
\textsuperscript{3}Department of Electrical and Computer Engineering, College of Engineering, Sultan Qaboos University, Muscat 123, Oman  
\textsuperscript{4}Department of Electrical Engineering, National Institute of Technology Durgapur, Durgapur 713209, India  

Corresponding author: Santosh Sonar (santosh.sonar@thapar.edu)

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\textbf{ABSTRACT} In a 3L-VSI, to realize reference vector, maximum of six switching per sub-cycle are permitted. A similar condition is looked for in 3L-ZSI (Z source inverter). The current continuous SVPWM methods of 3L-ZSI have adopted two approaches to meet the desired condition. These are a selection of sub-cycles generating six and eight switching employing correct volt-second balance. The sub-cycles generating eight switching has the demerit of increased losses. Here a new switching pattern has been proposed to optimize the number of switching. The dependency of the modulation index and sub-cycle duration on the switching frequency has also been discussed. With the increase in carrier frequency, the proposed PWM technique offers a decrease in switching losses compared to the existing ones. This leads to the improved efficiency of 3L-ZSI. To verify the efficacy of the proposed technique, simulation and prototype results are presented.

\textbf{INDEX TERMS} ZSI, SVPWM, CDBC 3L-ZSI.

\section{I. INTRODUCTION}

\textbf{LIST OF SYMBOLS AND ABBREVIATIONS}

$T_s$ \hspace{1cm} Half sub cycle period.  
$M$ \hspace{1cm} Modulation Index.  
$V_{cr}$ \hspace{1cm} Corrected reference vector.  
$d_{sh}$ \hspace{1cm} Shoot through duty ratio.  
$B$ \hspace{1cm} Boost factor.  
$F_{sw}$ \hspace{1cm} Switching frequency.  
$D$ \hspace{1cm} Duty ratio of switch.  
$U_{ce}$ \hspace{1cm} Collector emitter saturation voltage.  
$V_f$ \hspace{1cm} Forward voltage drop across diode.  
$i_c$ \hspace{1cm} Forward current through IGBT.  
$i_f$ \hspace{1cm} Forward current through diode.  
$T_j$ \hspace{1cm} Junction temperature.  
$E_{on},E_{off}$ \hspace{1cm} Energy loss during turn on and turn off resp.  
$E_{rec}$ \hspace{1cm} Reverse recovery energy loss of diode.  
$N_{ST}$ \hspace{1cm} non shoot through.  
$L_{ST}$ \hspace{1cm} lower shoot through.

The Z-source inverter [1] is used for various applications in 2-L and multilevel [2]–[18] inverters. Topology and PWM technique development [4]–[18], are two major research areas of 3L-ZSI. As compared to the two level ZSI, the operation principle and switching state selection procedure of the 3L-ZSI is more complex. The early attempt to extend the concept of ZSI to the three-level dc to ac conversion can be seen in [4] where two LC impedance network has been used between input dc source and neutral point clamped three level inverter circuitry. The two major modifications in VSI which transform it to a ZSI are; (i) the placement of LC network between dc source and inverter switches, and (ii) suitable modification in the PWM technique. The modified switching pattern of ZSI has one added state called shoot-through state (ST). During shoot-through state, the LC network is intentionally shorted through one or all phase legs for charging the inductors. The sine triangle comparison based on various PWM techniques of 3L-ZSI can be seen in [4]–[17]. It is clear from [4]–[17] that, at least five reference signals and two triangular carrier signals are required to achieve the shoot through condition. So, the practical implementation of the sine triangle comparison-based technique is too much complex. On the
other hand, the space vector PWM (SVPWM) approach offers easier implementation with more flexibility in the switching states selection. The SVPWM for the 3L-ZSI has been reported in [18], [24] and [25]. In these SVPWM techniques, ST state has been implemented using the time duration of small vectors only. In this aspect, these SVPWM techniques are equivalent to the continuous edge insertion sine triangle PWM proposed in [4]. However, the main difference between the continuous edge insertion PWM of [4] and SVPWM techniques of [24]–[25] is that, in former, every sub cycle causes exact eight switching and in later, the number of switching per sub cycle depends upon the position of reference vector (i.e. some sub cycle offers eight switching and other offers six switching. Reference [24] concludes that the number of switching per sub cycle are six in their SVPWM technique. But it is not true. For example, consider the condition when reference vector is in the region 2(a) (Fig. 4 of [24]). The switching pattern in this region is shown in Fig. 5(b) of [24]. This switching pattern causes eight switching per sub cycle. These types of regions have not been noticed in [25] also. There is maximum six permissible switching states when any continuous/discontinuous PWM (sine triangle or SVPWM based) technique is applied to the 3L-VSI. The researchers tried to achieve similar condition in 3L-ZSI in order to ensure that the insertion of ST states does not cause increase in switching losses. As discussed earlier, when continuous edge insertion PWM of [4] is used in 3L-ZSI, none of the sub cycle offers six switching. This is the main drawback of [4]. However, the authors of [4] also proposed continuous modified reference PWM technique which offers six switching per sub cycle throughout the fundamental line cycle, but this technique suffers following drawback: In continuous modified reference PWM, in one sub cycle two ST states are inserted. One ST state utilizes the interval of active vector and the other uses equivalent null state duration. Therefore, equalizing the time duration of both ST states is difficult. The unequal ST state duration per sub cycle cause unequal voltage boosting resulting increased impedance network inductor size and degraded output voltage quality. Also, when the SVPWM pattern used by [24], [25] is analyzed over a fundamental cycle, it is observed that, there are some regions which offer eight switching per sub cycle. These types of sub cycles violate the condition of maximum six switching per sub cycle in the case of 3L-ZSI. The novel contribution of this paper is the identification of regions in 3L-ZSI where eight switching per sub cycle occurs and a new switching technique is proposed to reduce it. The authors here claim that using continuous SVPWM technique in 3L-ZSI and small vectors as ST state, it is not possible to generate exact six switching in every sub cycle. An attempt is made to optimize the switching of the regions to 7 where [24] [25] causes eight switching per sub cycle. In this paper the efficacy of the proposed technique is presented based on switching frequency, inverter power losses, efficiency and THD of the output line voltage. Further, it is observed that the average switching frequency is dependent on modulation index and sub cycle duration. The proposed technique is implemented in a new configuration of the inverter, CDBC 3L-ZSI. As compared to the T-type and diode clamped ZSI configurations, CDBC ZSI offers some advantages, explained in section II. Section III discusses the concept of SVPWM and the ways of ST state introduction. The proposed and existing SVPWM is discussed in section IV. A brief comparison of frequency, losses, efficiency and THD is presented in section V. To verify the merits of the proposed technique, simulation and prototype results are presented in section VI. Finally, section VII concludes this paper.

Fig. 1 represents a new topology of 3L-ZSI. The conventional LC impedance network has been considered in combination with CDBC (controlled diode bridge clamped) 3L-VSI topology [19]. Each phase leg of 3L-ZSI is linked to the midpoint of dc bus through a bidirectional switching device, a combination of single IGBT and four diodes; so, the naming, CDBC 3L-ZSI is given in this paper. Table 1 shows the voltage levels corresponding to different switching states of this inverter configuration. A = R, Y, B and X = r, y, b For the medium power application, the CDBC version has the following merits: At any instant, for powering the load, conduction of one switch per phase leg is needed compared to two switches as in diode clamped ZSI. So, switching and conduction losses are comparatively less. Saving of one IGBT and associated gate driver circuitry compared to diode clamped and T-type ZSI [25].

III. SPACE VECTOR BASED PWM TECHNIQUE FOR 3L-ZSI

The 3L-VSI has been controlled effectively as a 2L-VSI in [21], [24]. A similar approach is implemented in 3L-CDBC ZSI and the corresponding diagram is presented in Fig. 2(a).
and (b). The equivalent null vectors are small vectors used as shoot-through states. Medium and large vectors are treated as equivalent active vectors in each two-level hexagon. As per the location of the original reference vector, the corresponding corrected reference vector is shown in 2L-hexagon. Then, the dwell time of each voltage vector is found out using two level SVPWM principal. For example, please see Fig. 2(b) subsector 1, the corrected reference vector ($V_{cr}$) can be realized using $V_1$, $V_{13}$ and $V_7$ having time interval $T_a$, $T_b$ and $T_z$ respectively. Description of switching vectors is presented in Table 2. Following equations are used for dwell time calculation (hexagon-1, subsector-1) [24].

$$T_a = \frac{V_{cr}}{0.5 V_{dc}} \sin(60^\circ - \beta) T_s$$

$$T_b = \frac{V_{cr}}{0.5 V_{dc}} \sin(60^\circ) T_s$$

$$T_Z = T_s - T_a - T_b$$

$T_a$, $T_b$ are the equivalent active vector durations and $T_Z$ is the equivalent null vector duration per half sub cycle.

The original reference vector ($V_{cr}$), for modulation index range '0.66-1.15' pass through four sub-sectors namely 1, 2, 5 and 6 as shown in Fig. 2(b). For ease of explanation, the sub-sectors are further designated as outer (5, 2) and inner sub sector (6, 1). The small vectors in 3L-ZSI are equivalent to null vectors in 2L-ZSI. Though, these small vectors do not produce zero line-voltage. So, at higher modulation index it is not possible to achieve nearest three vectors to achieve quality waveform. Keeping above mentioned conditions in mind, there are following two main approaches for shoot through selection.

1) USING SMALL AND MEDIUM VECTORS DURATION

In this approach switching vectors are generated by comparing sinusoidal and triangular signals. This approach has been chosen in [6]. It offers desired six switching per sub cycle over full fundamental period but the shoot through states duration is not equal resulting unequal voltage boosting. The complexity of equalizing both shoot through state (U_ST/L_ST) of a sub cycle is the major deremit of this approach. So, this approach is not popular in SVPWM domain.

2) USING ONLY SMALL VECTOR DURATION

ST state can also be implemented using the duration of small vectors only. For example, for shoot through insertion, continuous edge insertion PWM technique proposed in [4] uses only small vectors. The main drawback of this technique is that it generates eight switching in every sub cycle. The SVPWM switching pattern of [24], [25] also uses small vectors for ST state insertion, but in these cases, not all the sub cycles cause eight number of switching. For example, when SVPWM switching pattern of [24], [25] is applied, the outer sub-sectors of each hexagon cause eight switching and inner sub-sector of each hexagon cause six switching per sub cycle. The analysis of [24] and [25] reveals that the modulation

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### TABLE 1. Shoot through and non-shoot through states of 3L-ZSI.

| Shoot through naming | Operating IGBTs | $V_{XO}$ Pole-voltages | Switching conditions |
|----------------------|----------------|------------------------|----------------------|
| N_ST                 | SA1            | V/2                    | +                    |
| N_ST                 | SA2            | 0                      | -                    |
| N_ST                 | SA3            | -V/2                   | -                    |
| F_ST                 | SA1, SA3       | 0                      | Full-shoot through   |
| U_ST                 | SA1, SA2       | 0                      | Upper-shoot through  |
| L_ST                 | SA2, SA3       | 0                      | Lower-shoot through  |

$A = R, Y, B$ and $X = r, y, b$

### TABLE 2. Description of switching vectors.

| Outer hexagon | Inner hexagon |
|---------------|---------------|
| $V_1$ [- - -] | $V_2$ [+] [-] |
| $V_3$ [- + +] | $V_4$ [- + +] |
| $V_5$ [- + +] | $V_6$ [- - +] |
| $V_{13}$ [- + 0] | $V_{14}$ [0 + -] |
| $V_{15}$ [- - 0] | $V_{16}$ [-0 +] |
| $V_{17}$ [0 - +] | $V_{18}$ [-0 -] |
| $V_{19}$ [0 0 0] | [+ + +] [+ - -] |

A. SELECTION OF SHOOT THROUGH STATES

In order to have balanced voltage boosting in 3L-ZSI, the time interval of upper shoot through and lower shoot through must be equal within a sub cycle. Also, the corrected reference vector should be realized using the nearest three vectors to achieve quality waveform. Keeping above mentioned conditions in mind, there are following two main approaches for shoot through selection.
index and switching cycle duration cumulatively decides the spent duration of reference vector in these sub-sectors. This is discussed in next section. The proposed technique also uses small vector duration for the insertion of shoot through states.

IV. PATTERN OF SWITCHING STATES
In this paper maximum constant boost (MCB) control technique [25] has been used to decide shoot through duration within a sub cycle. The total duration of small vectors is minimum when original reference vector is at $\alpha = 30^\circ$. As per MCB principal, the small vectors duration when original reference vector is at $\alpha = 30^\circ$ should be taken as the reference duration of ST state for each sub cycle. Mathematically, it can be stated that:

$$T_Z = T_{ZSC} + T_{ZSX} \quad (4)$$

$T_Z$ is equivalent null vector duration within a sub cycle and $T_{ZSC}$ is the equivalent null vector interval at angle $\alpha = 30^\circ$ of the reference vector $V_{cr}$. Or it can be said that, this is the reference duration for ST state of each sub cycle. $T_{ZSX}$ is leftover equivalent null vector duration in a sub cycle. When upper and lower ST states are used using single LC impedance network, the relation between modulation index and ST duty ratio can be written as:

$$d_{sh} = \frac{T_{ZSC}}{T_S} = \frac{1}{2}[1 - \frac{\sqrt{3}}{2}M] \quad (5)$$

With single LC impedance network, ‘$d_{sh}$’ offered by UL_ST scheme is half as compared to the F_ST scheme. This is written as:

$$(d_{sh})_{UL\_ST} = \frac{1}{2} \times (d_{sh})_{F\_ST} \quad (6)$$

Boost factor is related to shoot through ratio as:

$$B = \frac{1}{1 - 2d_{sh}} \quad (7)$$

From (5),(6) and (7) it is concluded that for a particular value of modulation index, boosting offered by UL_ST scheme is lower as compared to the F_ST scheme of 3L-ZSI using single LC impedance network. This paper considers UL_ST scheme. This technique offers better output waveform quality because of the nearest three vector (NTV) switching. NTV switching is not possible using F_ST scheme.

A. LATEST SVPWM SWITCHING STATES PATTERN
The latest SVPWM switching sequences of 3L-ZSI are reported in [24], [25] is explained here as under.

1) ST INSERTION FOR THE INNER SUBSECTORS
Table 3 shows the sequences for the inner subsectors (6,1) of hexagon 1. Highlighted rows indicate the ST states. In subsector 6 when the sequence traverses from ‘+ $O\_O$’ to ‘+ – $O$’ the switch SY2 and SY3 changes from on to off and off to on state respectively. The advanced on of switch SY3 inserts a new state ‘+ $L\_O$’ before ‘+ – $O$’. This state shorted the impedance network by ‘y’ phase leg and produce same line voltage as that of ‘+ $O\_O$’. Likewise upper shoot through (U_ST) is generated when the state traverses from ‘+ –’ to ‘$O\_O$’.

Fig. 3(a) represents the switching pattern for inner subsector1, hexagon 1, for 3L-VSI. Fig. 3(b) represents the switching pattern for 3L-ZSI. The switching per sub cycle is just six in both switching patterns of Fig.3.

2) SHOOT THROUGH INSERTION PROCESS IN THE OUTER SUBSECTORS
Table 4 displays the switching sequences of outer subsectors (5, 2) of the hexagon 1. These are same as that of inner subsectors (i.e. ST state is always applied after first switching state and before the last switching state) using the existing SVPWM technique of 3L-ZSI [24], [25].

Consider subsector 5 of the Table 4, in between ‘+ + $O\_O$’ and ‘+ – $O$’, L_ST state is inserted. Similarly, in between ‘$O\_O$’ and ‘$O\_O$’, U_ST state ‘U –’ is applied. For the outer subsector 2, Fig. 4(a) and Fig. 4(b) displays the switching pattern of 3L-VSI and 3L-ZSI respectively. The number of switching per sub cycle are six and eight using the switching pattern of Fig. 4(a) and Fig. 4(b) respectively. Similarly, all the outer subsectors of equivalent 2L-hexagons cause eight switching per sub cycle for the case of 3L-ZSI using existing SVPWM [24], [25].
TABLE 4. Switching states of a sub cycle in the outer subsectors of the hexagon 1 using existing SVPWM switching pattern.

| Outer subsectors of Hexagon 1 using existing SVPWM pattern | Subsector 1 | Subsector 2 |
|-----------------------------------------------------------|-------------|-------------|
| State | SR | SY | SB | State | SR | SY | SB |
| +00 | 100 | 010 | 010 | +00 | 100 | 010 | 010 |
| +0 | 100 | 011 | 010 | +0 | 100 | 011 | 010 |
| 00 | 100 | 001 | 010 | 00 | 100 | 001 | 010 |
| -0 | 100 | 001 | 011 | -0 | 100 | 001 | 011 |
| 0- | 110 | 001 | 001 | 0- | 110 | 001 | 001 |
| 0- | 010 | 011 | 001 | 0- | 010 | 011 | 001 |

Total transitions: 8

FIGURE 4. (a) 3L-VSI switching pattern (b) modified by the reference [24], [25] for 3L-ZSI in the similar region (c) Proposed SVPWM switching pattern for 3L-ZSI in the similar region.

B. PROPOSED SVPWM SWITCHING STATES PATTERN

1) SHOOT THROUGH INSERTION IN THE INNER SUBSECTORS

As shown in Table 3, the inner subsectors already offered minimum switching (six per sub cycle) using existing SVPWM switching pattern. It is not possible to further reduce switching per sub cycle using any continuous SVPWM technique in these regions. So, the switching pattern in the inner subsectors is kept same with the proposed SVPWM.

2) SHOOT THROUGH INSERTION IN THE OUTER SUBSECTORS

Table 4 shows that there is total 8 switching per sub cycle using existing SVPWM switching pattern. Similarly, other 5 hexagon offers 8 switching per sub cycle in the outer subsectors. Another important observation form the Table 4 is that, the ST state is always applied after first equivalent null state (i.e. ‘+ O O’) and before second equivalent null state (i.e. ‘O – –’). However, when the upper ST state ‘U – –’ of Table 4 is shifted to the position after the state ‘O – –’ (i.e., at last position as shown in Table 5), one switching per sub cycle is reduced.

The proposed pattern is shown in Fig. 4(c). It is found that the proposed technique generates seven switching per sub cycle in all outer sub sectors. It is also observed that the location of the shoot through state is not same in outer and inner subsectors. For example, the position of ST states in the Fig. 3(b) is different from the Fig. 4(c).

V. COMPARISON OF EXISTING AND PROPOSED SVPWM PATTERN

A. SWITCHING FREQUENCY

Previous section concludes that the outer subsectors switching are more compared to inner sub subsectors of each 2L-hexagon. Table 6 summarize the switching per sub cycle.

It is also observed that for a fixed carrier frequency, with decrease in modulation index, the half sub cycles in the inner subsectors decreases and outer subsector increases. In Table 7, three sets of carrier frequency have been taken and the mapping of half sub cycles has been done depending upon their position in the corresponding subsector. Each equivalent
two-level hexagon is symmetrical (i.e., number of sub cycle and pattern is same for each). As in the outer sub sectors, number of half sub cycles increases, the inverter switching frequency also increases. Therefore, switching frequency of 3L-ZSI increases with the decrease in modulation index. This is contrary to the case of 3L-VSI where switching frequency is independent of reference vector position.

Proposed and existing patterns are implemented in CDBC 3L-ZSI and corresponding switching frequencies are summarized in Table 8. Again, three cases of carrier frequency have been considered and the switching frequency is calculated for the different values of modulation index. The switching transitions during hexagon-to-hexagon changeover has also been taken into account in order to have exact value of switching frequency. Consider a case of Table 8, when carrier frequency is 10.65 kHz and modulation index is 1. At this condition, switching frequency using proposed and existing SVPWM switching pattern is 5700Hz and 6025Hz respectively. This shows, a reduction of 325Hz per switch is achieved using proposed switching pattern. It suggests the merits of proposed pattern even at higher modulation index. The same advantage of the reduced switching frequency is equally valid in diode clamped and T-type ZSI using proposed SVPWM switching pattern.

### B. LOSSES AND EFFICIENCY

Switching and conduction loss contributes a significant portion of total power loss in an inverter. The average conduction loss per sub cycle across IGBT and diode can be obtained as follows:

\[
P_{\text{conduction--IGBT}} = V_{ce}(T_j, I_c) \times I_c \times D \quad (8)
\]

\[
P_{\text{conduction--Diode}} = V_f(T_j, I_f) \times I_f \times D \quad (9)
\]

The switching losses can be further categorized as turn-on and turn-off energy losses and in case of IGBT it is defined as:

\[
P_{\text{(switching--IGBT)}} = (E_{on} + E_{off}) \times F_{sw} \quad (10)
\]

For diodes, only reverse recovery losses are considered and can be expressed as:

\[
P_{\text{(recover--Diode)}} = E_{(rec)} \times F_{sw} \quad (11)
\]

The above-mentioned parameters are taken from datasheets. The total power losses using proposed SVPWM pattern and the existing SVPWM pattern has been plotted in Fig. 5. Fig. 5(a) and 5(b) shows the total power losses of the inverter at the carrier frequency of 1.65 kHz and 5.25 kHz respectively. It is clear from the Fig. 5(a) and Fig.5(b) that, for a fixed carrier frequency, as the modulation index decreases the difference between the total power loss of proposed SVPWM pattern and existing SVPWM pattern increases.

Fig. 6(a) and Fig. 6(b) shows the comparison of efficiency between proposed and existing switching pattern at the carrier frequency of 1.65 kHz and 5.25 kHz respectively. From Fig.6, it can be concluded that the proposed SVPWM pattern offers better efficiency as compared to existing pattern. The difference between the efficiency offered by both approaches increases with decrease in modulation index and increase in carrier frequency.

### C. THD CONTENT

The line voltage and line current THD offered by both approaches is listed in Table 9. The THD percentage is almost same in the both approaches. It confirms the suitability of proposed switching pattern without compromising the quality of the output waveforms.

### VI. PASSIVE COMPONENT DESIGN

Considering the high frequency ripple component, LC network is designed as follows. The inductor current peak to peak ripple is expressed as:

\[
\Delta I_L = \frac{V_c}{L} \left[ \frac{d_{sh} T_s}{2} \right] 
\]

\[
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\]
The average capacitor voltage is expressed as:

\[ V_c = V_{dc} \left[ 1 - d_{sh} \right] \left( 1 - 2d_{sh} \right) \]  

(13)

The allowable ripple in inductor current is:

\[ \Delta i_L = r_L \cdot I_L \]  

(14)

Here \( r_L \) is the allowable ripple current in percentage and the average inductor current is represented as:

\[ I_L = \frac{P}{V_{dc}} \quad P= \text{inverter output power} \]  

(15)

Putting (5), (12) and (13) into (11), the expression for ‘L’ can be written as:

\[ L = \frac{(1 - d_{sh})V_{dc}(2 - \sqrt{3}M)T_s}{8(1 - 2d_{sh})r_L I_L} \]  

(16)

Similarly, the capacitor voltage ripple component is expressed as:

\[ \Delta V_c = \frac{I_L}{C}\left( \frac{d_{sh}T_s}{2} \right) \]  

(17)

The allowable ripple of capacitor voltage is:

\[ \Delta V_c = r_c V_c \quad r_c = \% \text{allowable voltage ripple} \]  

(18)

Using (5), (12), (16) and (17), the expression for ‘C’ is obtained as:

\[ C = \frac{I_L(1 - 2d_{sh})(2 - \sqrt{3}M)T_s}{8r_c V_c(1 - d_{sh})V_{dc}} \]  

(19)

**VII. RESULTS**

The proposed SVPWM switching pattern have been validated using Matlab/Simulink software and experimental prototype using the parameters mentioned in the Table 10. Fig. 7 shows the simulation waveforms of gating pulses for switch SR1, SR2 and SR3 employing proposed switching pattern. For the positive half cycle of output pole voltage, switch SR1 conducts in conjunction with bidirectional switch SR2. Switch SR3 remains OFF during this period. For negative half cycle of pole voltage, switch SR3 conducts in conjunction with bidirectional switch SR2. Switch SR1 remains in OFF position during negative half cycle of pole voltage.

Output line voltage \((V_{ry})\) is shown in Fig. 8(a). The line voltage waveform confirms that the proposed technique
TABLE 10. Parameter used for simulation and prototype.

| Parameters          | Values/Name   |
|---------------------|---------------|
| DC input            | 100V          |
| inductor/capacitor  | 2mH/220nF     |
| hardware used for PWM| TMS320F28379D |
| Carrier frequency (Fc) | 1.65 kHz   |
| Half sub cycle period (Ts) | 303μsec.    |

follows nearest three vector approach for generating correct volt sec balance. For ‘M = 1’, ‘B’ comes out to be 1.15 using equation (5) and (7). Simulation waveform of line voltage has a peak of 113.5V which is almost equal to the expected theoretical value of 115V according to the relation ‘B.Vdc’. Simulation waveform of the pole voltage (Vro) shown in Fig. 8(b) has a peak of around ±56.5 V. This value matches with the expected theoretical value of ±57.5 V according to the relation ±B.Vdc/2.

The lower dc link voltage (Vnx) is shown in Fig. 8(c). It switches between zero and −B.Vdc/2. Upper dc link voltage (Vpx) is shown in Fig.8(d). It switches between zero and +B.Vdc/2. Fig. 9(a) and Fig.9(b) shows the neutral point capacitor voltages for ‘M’ = 1 and ‘M = 0.73’ respectively.

The neutral point capacitor voltages(VC1, VC2) are balanced around the half of the source voltage (Vdc). In order to have experimental verification of the proposed SVPWM switching technique, a laboratory prototype has been built. The photograph of laboratory prototype is shown in Fig.10. Fig.11 represents the switching pulses of the three IGBTs of ‘r’ phase leg. These are exactly similar to the simulation waveforms of Fig7. This ensures the practical feasibility of the
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SANTOSH SONAR (Member, IEEE) was born in Ansals, West Bengal, India, in November 1979. He received the Graduate and master’s degree in electrical engineering from NIT Durgapur, India, in 2004 and 2009, respectively, and the Ph.D. degree in electrical engineering from the Indian School of Mines, Dhanbad, India, in 2014. He is currently working with the Department of Electrical and Instrumentation Engineering, Thapar Institute of Engineering and Technology, Patiala, Punjab, India. His research interests include Z-source inverters, AC-AC converters, and SMPS design.
SANJOY MONDAL received the bachelor’s and master’s degrees in electrical engineering from the Department of Electrical Engineering, National Institute of Technology Durgapur, India, and the Ph.D. degree in electrical engineering from the Indian Institute of Technology Guwahati, India, in 2013. He is currently working with the Department of Electrical Engineering, Institute of Engineering and Management, Kolkata, India. His current research interests include distributed control of multiagent systems, transportation, and energy management.

JAWHAR GHOMMAM (Member, IEEE) received the B.Sc. degree in computer and control engineering from the National Institute and Applied Sciences and Technology (INSAT), Tunis, in 2003, the D.E.A. (M.Sc.) degree from the Laboratoire d’Informatique, Robotique et Micro-électronique (LIRMM), University of Montpellier, France, in 2004, and the joint Ph.D. degree in control engineering from the National Engineering School of Sfax and the University of Orleans. From 2008 to 2017, he was with the National Institute of Applied Sciences and Technology, where he held a tenured Associate Professor with the Department of Physics and Instrumentation. In January 2018, he joined the Department of Electrical and Computer Engineering, Sultan Quaboos University (SQU), Oman. He is a member of the Control and Energy Management Laboratory and also an Associate Researcher with the GREPCI-Laboratory, Ecole de Technologie Superieure, Montreal, QC, Canada. His research interests include fundamental motion control concepts for non-holonomic/underactuated vehicle systems, nonlinear and adaptive control, intelligent and autonomous control of networked unmanned systems, team cooperation, consensus achievement, and sensor networks. He serves as a regular referee and associate editors for many international journals in the filed of control and robotics.

SUBRATA BANERJEE (Senior Member, IEEE) is currently working as a Professor with the Department of Electrical Engineering, National Institute of Technology Durgapur, India. He has successfully completed several research and consultancy projects. He has authored about 200 research papers in national/international journals and conference records. He has filed three Indian patents out of which one has been granted. He has guided ten Ph.D. and 22 M.Tech. students and many are pursuing their degree under his guidance. His research interests include modeling & control of switch-mode converters and inverters, multilevel inverters & different modulation techniques, electromagnetic levitation, active magnetic bearing, controller design, and intelligent control. He was a recipient of several academic awards, including ten nos. He received best paper awards and TATA RAO Prize. He is a fellow of the Institution of Engineers (India), the Institution of Electronics and Telecommunication Engineers (India), and the Institution of Engineering and Technology (U.K.). He is a Regular Reviewer of IEEE/IET TRANSACTIONS and also acting as an Associate Editor/an Editorial Board of IEEE ACCESS (USA), IET Power Electronics (U.K.)/IEEE Transportation Electrification Community e-Newsletter (USA).

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