Derivation of OCC Modulator for Grid-Tied Single-Stage Buck-Boost Inverter Operating in the Discontinuous Conduction Mode

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Abstract: This paper is concerned with the derivation of a one-cycle controller for driving a single-stage buck-boost DC-AC micro-inverter in grid-tied applications. The topology under study is based on a full-bridge switch arrangement with no unfolder circuit. The proposed micro-inverter attains a high gain by applying a multi-winding tapped inductor and, therefore, can operate at grid-level voltage without using a DC-DC step-up stage. To minimize the switching loss, the proposed inverter is operated in the discontinuous conduction mode. The operation principles of the proposed topology in the discontinuous conduction mode are discussed and analyzed. Based on the analysis, the one-cycle control law and modulator circuitry needed to control the proposed micro-inverter are developed. The feasibility of the proposed modulation scheme is verified by simulation.

Keywords: one-cycle control; grid-tied; single-stage; buck-boost; discontinuous conduction mode

1. Introduction

For many years, considerable research and development efforts were invested in the development of solar energy technologies. While some were focused on harvesting the solar thermal power [1,2], others were dedicated to photovoltaic (PV) power generation. The rapid progress of photovoltaic power generation systems has aroused much interest in micro-inverter technologies. Micro-inverters are designed to directly connect a single PV panel to the grid, attain maximum power point tracking (MPPT), provide a “plug-and-play” feature, and allow easy expansion of the PV array. Micro-inverters rely on high voltage step-up capability to boost the low PV panel voltage to the utility level.

A two-stage micro-inverters employ a high-gain DC-DC stage followed by a regular inverter. The two-stage configuration is quite popular due to its ease of implementation and control. A prominent advantage of the two-stage approach is the presence of a DC link. Placed in between the DC-DC and the DC-AC stage, the DC link capacitor helps to balance the DC and AC power flow. The high voltage DC link requires a relatively low capacitance, possibly a non-electrolytic one. However, the downside of the two-stage concept is the higher cost and lower efficiency.

A single-stage micro-inverter can combine the voltage step-up and inversion functions in one power stage. Such a concept allows for low component counts, low cost, and high efficiency compared with the traditional two-stage solution. Therefore, much of the recent research was in the field of single-stage micro-inverters. As a result, a significant number of boost-derived single-stage inverters with high voltage step-up capability were developed [3–5]. However, the boost-derived inverters typically have a dead-time gap in the output current near the line voltage zero crossing and, thus, a lower power factor.

The buck-boost derived single-stage micro-inverter topologies, due to their voltage step-up/down capability, can sustain the output current throughout the line period and therefore attain a high-power
The recent literature reports on several buck-boost-derived single-stage inverters with reduced cost and improved performance. The buck-boost-derived single-stage inverters with four switches were proposed in [6–9]. Furthermore, the single-stage buck-boost topologies with only three switches were reported in [10,11]. However, the voltage gain of the aforementioned topologies is comparable to the traditional buck-boost converter. Other attempts to attain a higher gain, based on the buck-boost configuration, were also reported. A few selected topologies of high-gain single-stage buck-boost inverters are shown in Figure 1. The topology in [12] adopted a switched inductor to have a higher gain by the factor of $\sqrt{2}$ over that of the conventional buck-boost converter. However, the proposed topology has four switches, eight diodes, and four inductors. The single-stage buck-boost inverters with tapped inductor were proposed in [13,14], which can have much higher voltage gain than the classic topologies, whereas the total switches count sum up to eight. A tapped-inductor-based single-stage buck-boost topology in [15,16] had five switches, while only one switch operated at a high frequency so as to minimize the switching loss.

![Figure 1. Earlier high-gain single-stage buck-boost micro-inverters: (a) Reference [10]; (b) Reference [11]; (c) Reference [12]; (d) Reference [13,17].](image)

The high switch count of the earlier counterparts, their topological complexity, and relatively high cost diminish the attractiveness of the single-stage inverters. Therefore, recently, additional efforts have been taken to develop an effective and affordable single-stage buck-boost micro-inverter topology.

Recently, a family of single-stage buck-boost micro-inverters was proposed in [17]. A prominent representative of this inverter family is illustrated in Figure 2. Hereafter, the topology in Figure 2 is referred to as the Single-Stage Buck-Boost Inverter (SSBBI). Initially, this earlier SSBBI version was successfully tested in the stand-alone application and was operated in the continuous conduction mode (CCM). SSBBI testing indicated the feasibility of the proposed scheme. However, most of the
renewable energy systems are aimed at grid-tied applications. Therefore, this study is dedicated to the investigation of the challenges involved with the grid-tied operation of the SSBBI.

![Diagram of grid-tied single-stage buck-boost inverter (GT-SSBBI)](image_url)

Figure 2. The grid-tied single-stage buck-boost inverter (GT-SSBBI).

Switching losses caused by reverse recovery of the diodes is a major concern in inverter applications. One possible way to minimize the switching loss is to operate the power stage in the discontinuous conduction mode (DCM) to achieve zero-current turn-off and, thus minimize diodes’ reverse recovery. This calls for derivation of the appropriate controller suited for the DCM operational mode.

While a variety of control methods is available, here, the One-Cycle Control (OCC) approach is pursued. OCC is a nonlinear control strategy and pulse-width-modulation method applicable to switch-mode systems [18,19]. By controlling the duty cycle of the switches, OCC can enforce the average value of the switched variable to precisely follow the reference signal in each switching cycle. Therefore, OCC can reject the input source perturbation within a single cycle and with no application of a feedback loop. Furthermore, OCC has the merits of the constant switching frequency, fast dynamic response, and can attain a superior performance in power electronics applications.

For these reasons, OCC has received significant attention in the scientific community and has been widely used in practical industrial applications. OCC was applied in DC-DC switching converters [20,21], power factor corrector (PFC) rectifiers [22–24], and active power filters (APF) [25,26]. OCC was developed to meet the challenges of single and three-phase renewable energy applications such as grid-tied inverters (GTI) for photovoltaic (PV), fuel cells (FC), and wind power (WP) energy sources, together with the maximum power point tracking (MPPT) control [27,28]. OCC control schemes were also employed for uninterruptable power supplies (UPS), var generator, dynamic voltage restorer (DVR), electronic load, and motor control applications.

The objectives of this study were to develop the required OCC control law and, consequently, the OCC modulator circuitry needed for controlling the grid-tied SSBBI. The rest of the paper is organized as follows. The SSBBI is reviewed in Section 2. Section 3 introduces the operation principles of the SSBBI in the DCM regime. In Section 4, the derivation of the OCC law and the modulator implementation are presented. The design guide and example are given in Section 5. Section 6 reports the simulation results and, finally, concluding remarks are provided in Section 7.

2. SSBBI Review

The SSBBI topology in Figure 2 comprises a grounded source and a ground-referenced full-bridge. Here, the lower switches Q1 and Q3 are considered as primary devices, while the high switch pair Q2 and Q4 are operated as synchronous rectifiers. Furthermore, the body diodes of the high switches can be exploited as rectifiers. Hence, reverse recovery problems should be considered. To minimize the problem, DCM operation is attempted to provide zero-current switching and reduced switching loss.
The SSBBI makes use of a single multi-winding tapped inductor (TI). The TI is comprised of two symmetrical pairs of windings. The turns of the primary windings are \(N_1 = N_2\). Similarly, equal secondary windings are used \(N_3 = N_4\). The turn ratio of the tapped inductor is defined as \(n = N_3/N_1 = N_4/N_2\).

In practice, an output filter capacitor, \(C_o\), is needed to reduce the switching ripple penetrating the grid. The voltage across \(C_o\) is dictated by the AC line, \(v_{ac}\). Better filtering of the high-frequency current components can be provided by a CLC type output filter (not considered in this paper).

Bipolar output current can be generated by SSBBI due to its symmetrical structure and symmetrical operation, and so can perform DC-AC inversion function. Properly chosen TI’s turn ratio, \(n\), helps SSBBI to generate output current at grid level voltage when fed by a low DC voltage source. The desired output current can be controlled using any common control strategy, preferably at a constant frequency (for the ease of electro-magnetic interference (EMI) filtering). However, in this paper, the OCC modulation strategy is investigated.

The advantageous merits of the SSBBI are:

1. Generating bipolar output current at grid level AC output voltage from a relatively low DC input voltage source without using an additional high-gain DC-DC stage;
2. Low component count topology comprising a single magnetic device and four switches;
3. The switches are assembled in a traditional full-bridge arrangement, suited for low-cost integrated-circuits drivers.

3. SSBBI Operation in the Discontinuous Conduction Mode

While operating in the DCM of the tapped inductor, the SSBBI has three switching states in each line half-cycle: states A, B, and C appear during the positive line half-cycle and the mirror (complementary) states A', B' and C' during the negative line half-cycle.

The switching states of the SSBBI’s semiconductor switches are listed in Table 1, whereas the equivalent circuits of SSBBI’s states are illustrated in Figure 3.

![Figure 3](image_url)

**Figure 3.** Equivalent circuits (switching states) of the proposed SSBBI: (a) State A; (b) State B; (c) State C; (d) State A'; (e) State B'; (f) State C'.
Table 1. Switching states of SSBBI’s semiconductor devices.

| Switches      | Positive Line Voltage | Negative Line Voltage |
|---------------|-----------------------|-----------------------|
|               | State A | State B | State C | State A' | State B' | State C' |
| Q₁            | On      | Off     | Off     | Off      | Off      | Off      |
| Q₂            | Off     | Off     | Off     | On       | On       | On       |
| Body Diode of Q₂ | Off   | On      | Off     | Off      | Off      | Off      |
| Q₃            | Off     | Off     | Off     | On       | Off      | Off      |
| Q₄            | On      | On      | On      | Off      | On       | Off      |
| Body Diode of Q₄ | Off   | Off     | Off     | Off      | On       | Off      |

The key theoretical waveforms of the SSBBI in the DCM mode are illustrated in Figure 4. Here, \( S_{Q1} \text{–} S_{Q4} \) are the driving signals for the \( Q_1 \text{–} Q_4 \) switches, respectively. Since the SSBBI operates symmetrically, only the positive half-cycle is analyzed. The primary winding of the tapped inductor is charged by the input source when \( Q_1 \) is turned on and \( Q_2 \) is turned off. Thus, the magnetizing current of the tapped inductor begins to ramp up. When \( Q_1 \) is turned off, the energy stored in the tapped inductor is discharged to the grid through all four of its windings. Hence, the magnetizing current of the tapped inductor is decreased from its peak to zero.

![Figure 4](image)

Figure 4. Illustration of key waveforms of the proposed SSBBI.

In grid-tied applications, the task of the converter’s control circuit is to shape the average output current into a sinusoidal waveform (see \( i_{N_4} \) in Figure 4). However, in stand-alone applications, the controller should regulate the output voltage.

4. Derivation of OCC Control Law

State A, see Figure 3a, appears at the beginning of each switching cycle in the positive line half-cycle. In this state, the switch \( Q_1 \) is turned on for the duration of \( DT_s \), determined by the controller. Here, \( D \) is the ON duty cycle of the switch \( Q_1 \) and \( T_s \) is the switching period. As a result, the TI’s magnetizing inductance, \( L_m \), (referred to \( N_1 \) winding) is charged by the DC input voltage source, \( V_g \), and by the end of state A, reaches its peak current, \( I_{pk} \), see Figure 5:

\[
I_{pk} = \frac{1}{L_m} DT_s V_g
\]
At this instant, the energy stored in the magnetizing inductance, $E_{pk}$, is

$$E_{pk} = \frac{1}{2} L_m I_{pk}^2 = \frac{1}{2 L_m} (DT_s V_g)^2$$  \hspace{1cm} (2)

State B, see Figure 3b, begins when the switch $Q_1$ is turned off and lasts for the duration needed for the TI current to drop to zero. During this state, the energy stored in the tapped inductor is discharged into the grid. Therefore, the average power per switching cycle, $P_{av}$ is

$$P_{av} = \frac{E_{pk}}{T_s} = \frac{1}{2 f_s L_m} (DV_g)^2$$  \hspace{1cm} (3)

Here, $f_s = 1/T_s$ is the switching frequency.

State C, see Figure 3c is the DCM idle state. Here, none of the switches conduct and no energy flow occurs.

The average current per switching cycle, $i_{acav}(t)$, injected into the grid can be found from Equation (3) as:

$$i_{acav}(t) = \frac{P_{av}}{v_{ac}(t)} = \frac{1}{2 f_s L_m} \left(\frac{DV_g}{v_{ac}(t)}\right)^2$$  \hspace{1cm} (4)

The control goal of the grid-tied SSBBI is to fulfill the unity power factor constrain:

$$i_{acav}(t) = \frac{v_{ac}(t)}{R_e}$$  \hspace{1cm} (5)

Here, $R_e$ is the emulated resistance of the inverter, assumed to be constant throughout the line cycle.

Combining Equations (4) and (5) implies

$$k_s v_{ac}(t) = k_s V_g \sqrt{\frac{R_e}{2 f_s L_m}} D = V_m D$$  \hspace{1cm} (6)

where the modulating voltage, $V_m$, is defined as
\[ V_m = k_v V_g \sqrt{\frac{R_e}{2f_L L_m}} \]  

(7)

and \( k_v \) has the meaning of the line voltage sensor gain.

From Equation (7), the emulated resistance, \( R_e \), can be expressed as a linear function of the modulating voltage, \( V_m \):

\[ R_e = \frac{2f_L L_m}{(k_v V_g)^2} V_m^2 \]  

(8)

Therefore, the average power, \( P_L \), delivered by the GT-SSBBI to the grid throughout the line cycle is

\[ P_L = \frac{V_{rms}^2}{R_e} = \frac{(k_v V_g V_{rms})^2}{2f_L L_m} \frac{1}{V_m^2} = \frac{k_p}{V_m^2} \]  

(9)

Here, the power constant, \( k_p \), is defined as

\[ k_p = \frac{(k_v V_g V_{rms})^2}{2f_L L_m} \]  

(10)

Assuming that the modulating voltage, \( V_m \), is a slowly varying signal, Equation (6) can be written applying the one-cycle control (OCC) technique as

\[ k_s v_{ac}(t) = \frac{1}{T_s} \int_0^{DT_s} V_m df \]  

(11)

where the integrator’s time constant is set equal to the switching period, \( T_s \).

In fact, Equation (11) can be regarded as the desired OCC control law for the DCM GT-SSBBI. The block diagram of the required OCC modulator, which implements the control law Equation (11), is illustrated in Figure 6.

**Figure 6.** One-cycle control (OCC) modulator for the DCM GT-SSBBI: (a) circuit implementation; (b) key waveforms.

The proposed OCC modulator in Figure 6 is a very simple circuit comprised of a resettable integrator, a comparator, a set/reset flip flop (SRFF) memory device, and a constant frequency clock. A line voltage sensor and an absolute value circuit are also needed.

It is worth noting that in photovoltaic applications the modulation voltage, \( V_m \), is supposed to be provided for the OCC modulator by an external maximum power point tracker (MPPT) (not discussed in this paper).
5. Design Guidelines

5.1. Turn Ratio and Duty Cycle Constraints

During the state B (or B’), when the tapped inductor discharges the stored energy to the grid, the grid voltage is distributed across all four windings according to the turn ratio. Thus, an undesirable situation may arise if the voltage across the \( N_2 \) (or \( N_1 \)) winding tends to be higher than the value of the DC source voltage, \( V_g \). In such a case, the stored energy will be recycled back to the DC source (via the antiparallel diode of one of the lower switches) instead of being transferred to the grid. Therefore, for the proper operation of the SSBBI, the voltage across the primary windings must always be lower than the DC input voltage, \( V_g \). The worst case occurs at the peak of the line:

\[
\frac{v_{ac}(t)}{2(n+1)} \leq \frac{V_{rms}}{\sqrt{2}(n+1)} < V_g
\]

Hence, the design constrain on TI’s turn ratio should be observed:

\[
n > \frac{V_{rms}}{\sqrt{2}V_g} - 1
\]  

(13)

The volt-sec balance of the TI’s magnetizing inductance (referred to the \( N_1 \) winding) states that

\[
D' \frac{v_{ac}(t)}{2(n+1)} = DV_g
\]

(14)

since in the DCM mode

\[
D' < 1 - D
\]

(15)

and, since the maximum duty ratio, \( D_{\text{max}} \), occurs at the peak of the line, Equations (14) and (15) imply that to sustain the DCM, the duty-cycle, \( D_{\text{max}} \), generated by the controller should be constrained by

\[
D_{\text{max}} < \frac{1}{1 + \frac{\sqrt{2}(n+1)V_g}{V_{rms}}}
\]

(16)

5.2. Design Procedure

The design procedure of the OCC GT-SSBBI is required to establish the parameters of the tapped inductor: the turn ratio, \( n \), and the magnetizing inductance, \( L_m \); and the parameters of the controller circuit: the sensor gain constant, \( k_s \), and the integrator’s gain constant, \( T_i \). The parameters given are the effective line voltage, \( V_{rms} \); the input source DC voltage, \( V_g \); and the inverter’s full rated power, \( P_{L_{\text{max}}} \). The procedure unfolds as follows:

1. Choose an acceptable switching frequency, \( f_s \);
2. Choose the turn ratio, \( n \), to satisfy Equation (13);
3. Calculate the maximum duty cycle, \( D_{\text{max}} \), according to Equation (16). Considering parameter variations and possible transients, allow the practical maximum duty cycle to assume a somewhat smaller value of \( D_{pk} = 0.85 \times D_{\text{max}} \);
4. According to Equation (9), the average power injected into the grid is inversely proportional to the square of the modulation voltage. Thus, to generate the full rated power, \( P_{L_{\text{max}}} \), the modulation voltage has to assume its minimum value, \( V_{m_{\text{min}}} \). Hence, choose an acceptable value of the modulation voltage, \( V_{m_{\text{min}}} \), that suites the dynamic range of the controller’s circuitry signal;
5. The theoretical gain of the line sensor can be derived applying the full power and the peak of the line conditions as well as using \( D_{pk} \) for the maximum duty cycle to Equation (6):
\[ k_s = \frac{V_{m\text{min}}D_{pk}}{\sqrt{2}V_{\text{rms}}} \]  

(17)

(6) The magnetizing inductance can be obtained from Equation (9) so to satisfy the rated power requirements

\[ L_m = \frac{(k_s V_g V_{\text{rms}})^2}{2f_s P_{\text{Lmax}} V_{s \text{rms}}^2} \]  

(18)

(7) In practice, the output voltage of the line sensor should not exceed the maximum allowed input voltage, \( V_{\text{in max comp}} \), of the OCC comparator, nor can it be too small a value. To exploit the entire dynamic range of comparator’s input, the practical value of the line voltage sensor gain, \( k_s' \), can be selected according to

\[ k_s' = \frac{V_{\text{in max comp}}}{V_{\text{rms}}} \]  

(19)

(8) Finally, to correctly implement the OCC control law Equation (11), the integrator’s time constant is adjusted considering the ratio of the theoretically required \( k_s \), see Equation (17), and the practical \( k_s' \), set according to (19):

\[ T_i = \frac{k_s}{k_s'} T_s \]  

(20)

The tuned OCC control scheme is shown in Figure 7, which also shows the line polarity detection and steering logic needed to distribute the driving signals to the power switches.

![Figure 7. Improved OCC modulator for the DCM GT-SSBBI.](image)

5.3. Design Example

Design OCC GT-SSBBI micro-inverter to deliver \( P_{\text{L max}} = 100 \) W into the \( V_{\text{rms}} = 110 \) V line when fed by a \( V_g = 48 \) V input source. The suggested design procedure is applied as follows.

(1) The switching frequency of \( f_s = 50 \) kHz is chosen;

(2) The turn ratio according to Equation (13) is constrained by \( n > 0.62 \). Here, \( n = 1 \) is recommended;

(3) The maximum duty cycle according to Equation (16) is \( D_{\text{max}} = 0.447 \). Here, a more conservative value of \( D_{pk} = 0.38 \) is chosen;

(4) By designer’s choice, \( V_{m \text{min}} = 0.5 \) at full power;

(5) The required gain of the line sensor can be obtained using Equation (17) as \( k_s = 0.0012 \);

(6) The magnetizing inductance can be found, see Equation (18), as \( L_m = 16 \mu \text{H} \);

(7) By designer’s choice \( V_{\text{in max comp}} = 3 \) V and applying Equation (19), the practical gain of the line sensor is obtained as \( k_s' = 0.02 \);

(8) Using Equation (20), the integrator’s time constant can be found as \( T_i = 1.2 \times 10^{-6} \) s.

Based on the design example, the calculated emulated resistance is \( R_c = 120.6 \) Ω, and average output power, \( P_L = 100.3 \) W.
The theoretical expectations were verified by simulation. The comparison plots of the calculated vs. the simulated results of output power, $P_L$, and emulated resistance, $R_e$, and operating maximum duty cycle, $D_{pk}$, are shown in Figure 8. As can be seen from the plots, the calculated results are consistent with the simulated results, which again proves the accuracy of the design results.

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**Figure 8.** Comparison of the calculated and the simulated results as a function of the modulating voltage, $V_m$: (a) the output power, $P_L$; (b) the emulated resistance, $R_e$; (c) the operating maximum duty cycle, $D_{pk}$. 

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(6) The magnetizing inductance can be found, see Equation (18), as $L_m = 16 \, \mu H$.

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Simulated Results of OCC Controlled DCM GT

To verify the feasibility of the proposed OCC GT-SSBBI, simulations were carried out by the PSIM v. 9.1 simulation software. The key simulation parameters of GT-SSBBI were: output power $P_o = 100 \, W$; input voltage $V_g = 48 \, V$; line voltage $V_{ac} = 110 \, V/60 \, Hz$; switching frequency $f_s = 50 \, kHz$; magnetizing inductance of the tapped inductor $L_m = 16 \, \mu H$; turn ratio $n = 1$. The parameters of OCC controller were: line voltage sensor gain $k_s' = 0.02$; modulator voltage $V_m = 0.5$; integrator time constant $T_i = 1.2 \times 10^{-6} \, s$. 

The key waveforms of the OCC controller are shown in Figure 9.
6. Simulated Results of OCC Controlled DCM GT-SSBBI

To verify the feasibility of the proposed OCC GT-SSBBI, simulations were carried out by the PSIM v. 9.1 simulation software. The key simulation parameters of GT-SSBBI were: output power \( P_o = 100 \) W; input voltage \( V_S = 48 \) V; line voltage \( V_{ac} = 110 \) V/60 Hz; switching frequency \( f_s = 50 \) kHz; magnetizing inductance of the tapped inductor \( L_m = 16 \) µH; turn ratio \( n = 1 \). The parameters of OCC controller were: line voltage sensor gain \( k_v' = 0.02 \); modulator voltage \( V_m = 0.5 \); integrator time constant \( T_i = 1.2 \times 10^{-6} \) s.

The key waveforms of the OCC controller are shown in Figure 9.

![Waveforms of the OCC controller](image)

Figure 9. Key waveforms of the OCC controller: (a) on switching period scale; (b) on the line period scale.

Figure 9a illustrates the generation of the duty cycle, \( D \), by the OCC technique. Here, \( D \) assumes “high” at the beginning of each switching cycle and is set to “low” when the integrator output, \( v_i \), equals the reference signal of \( v_L \). Evidently, the duty cycle is generated properly.

The top trace in Figure 9b is the output of the line voltage sensor, \( v_{ac} \); the second trace is the rectified output of the sensed line voltage used as OCC reference signal, \( v_1 \approx |v_{ac}| \). The bottom trace shows the OCC integrator’s output, \( v_i \), where the peak follows the rectified sinusoidal waveform and, thus, has the same outline as \( v_1 \).

Key simulation results of OCC controlled GT-SSBBI at 100 W output power level are shown in Figure 10. Examining the waveforms reveals that the GT-SSBBI stands up to the theoretical expectations and generates the desired sinusoidal average output current at unity power factor. The parasitic parameters of the active and passive components were not considered, as the simulation was aimed at verification of the proposed OCC control scheme. Since the step-by-step simulation is generally...
accepted to be quite accurate tool, this provides confidence in the proposed topology and the OCC approach derived above.

![Diagram of SSBBI topology and waveforms](image)

**Figure 10.** Key simulation waveforms of the proposed OCC controlled GT-SSBBI: (a) driving signal and currents on the switching period scale; (b) \( V_{ds} \) of the switches in one leg, output current, \( i_{ac} \), line voltage, \( v_{ac} \) and average output current, \( i_{acav} \); (c) switch currents on the line period scale.

As it can be observed in Figure 10a, the simulation results are in close agreement with the analytical key waveforms in Figure 4. The idle period is visible at the end of each switching period, which proves...
the DCM operation of proposed GT-SSBBI. Furthermore, the line voltage and average output current of the proposed GT-SSBBI is given in Figure 10b, as well as the voltage across the switches in one leg. It can be observed in Figure 10b that the OCC-controlled GT-SSBBI can produce high-quality sinusoidal output current with the unity power factor. The currents flowing through the switches are presented in Figure 10c.

7. Conclusions

This paper introduced an OCC-controlled grid-tied single-stage buck-boost inverter. The proposed SSBBI topology is very simple and is comprised of a H-bridge switching structure and a single four-winding tapped inductor. Therefore, SSBBI can attain high voltage gain required in PV energy generation systems applications, while keeping a lower component count.

The paper described the SSBBI’s operation in DCM mode as a grid-tied inverter. The one-cycle control algorithm to operate the SSBBI in grid-tied operation was derived. Based on the theoretical derivations, the OCC modulator needed to control the SSBBI stage was developed. Design procedure for engineering design of the power stage and the associated control circuitry was also developed.

A grid-tied SSBBI was designed and verified by simulation. The reported simulation results stand in accord with the theoretical expectations. The simulation results are encouraging, having shown that the SSBBI topology is capable of delivering a well-shaped sinusoidal average current into the grid. Therefore, the SSBBI seems a feasible solution to single-stage micro-inverter applications.

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Nomenclature and Abbreviations

| Symbol | Description |
|--------|-------------|
| Q1, Q2, Q3, Q4, Q5 | the power switches |
| N1, N2, N3, N4 | the tapped-inductor windings |
| n | the turn ratio of the tapped-inductor |
| C_o | output filter capacitor |
| V_ac | the AC line voltage |
| i_ac | the output/line current |
| i_n1, i_n2, i_n3, i_n4 | the currents through the windings |
| V_g | the input voltage |
| i_g | the input current |
| i_Q1, i_Q3 | the currents through the switches Q1, Q3 |
| L_cp | the tapped-inductor |
| S_Q1, S_Q2, S_Q3, S_Q4 | the driving signals of the switches Q1-Q4 |
| D | the ON duty cycle |
| D’ | the OFF duty cycle |
| T_s | the switching period |
| T | the line period |
| i_ac_av | the average output current |
| L_m | the tapped-inductor magnetizing inductance |
| i_pk | the peak inductor current |
| E_pk | the peak energy stored in the magnetizing inductance |
| P_av | the average power per switching cycle |
| f_s | the switching frequency |
| i_ac_av(t) | the average current per switching cycle |
Re: the emulated resistance of the inverter
$V_m$: the modulating voltage
$k_s$: the line voltage sensor gain
$P_L$: the average power delivered to the grid throughout the line cycle
$k_p$: the power constant
$T_i$: the integrator’s time constant
$V_{\text{rms}}$: the root-mean-square value of output voltage
$D_{\text{max}}$: the maximum ON duty cycle ratio
$P_{L\text{ max}}$: the inverter’s full rated power
$D_{pk}$: the practical maximum duty cycle
$V_{m\text{ min}}$: the minimum value of the modulation voltage
$V_{\text{in max comp}}$: the maximum allowed input voltage of the OCC comparator
$k_s'$: the practical line voltage sensor gain
$P_o$: the output power
$v_i$: the integrator output signal of the OCC controller
$v_1$: the reference signal of the OCC controller
$v_{\text{acs}}$: the output signal of the line voltage sensor
$v_{ds1}, v_{ds2}$: voltage stress across the switches $Q_1, Q_2$
PV: photovoltaic
MPPT: maximum power point tracking
SSBBI: single-stage buck-boost inverter
CCM: continuous conduction mode
GT-SSBBI: grid-tied single-stage buck-boost inverter
DCM: discontinuous conduction mode
OCC: one-cycle control
PFC: power factor corrector
APF: active power filters
GTI: grid-tied inverters
FC: fuel cells
WP: wind power
UPS: uninterruptable power supplies
DVR: dynamic voltage restorer
TI: tapped inductor
EMI: electro-magnetic interference
SRFF: set/reset flip flop

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