Research and Hardware Design of Image Processing Algorithm Based on FPGA

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Abstract. With the continuous development of computer technology and microelectronics technology, image processing technology is constantly being improved, especially real-time image processing technology has been studied by a large number of scholars. This article aims to achieve the purpose of FPGA-based fast image processing through the research of FPGA's fast image processing algorithm. Based on the advantages of FPGA high-speed hardware computing and parallel computing, this paper proposes a design based on FPGA parallel dual template strategy, and designs a comparative experiment to verify. Obtain objective evaluation indexes of image processing results through experiments, and analyze the data results. The experimental results show that: the implementation of the mean filter algorithm based on FPGA parallel dual templates, the time required is about half that of the mean filter algorithm based on FPGA single templates. Relative to the reference Matlab software programming method to achieve 678 times performance improvement. It shows that the realization method of the mean filter algorithm based on FPGA parallel dual template is feasible. Give full play to the advantages of FPGA parallel processing data, improve the processing speed of the image algorithm module.

Keywords: FPGA Device, Image Processing Algorithm, Hardware Design, Parallel Dual Template

1. Introduction

With the rapid development of computer information technology, microelectronics and integrated circuit technology, image processing technology has been greatly developed both in system structure and algorithm, and is widely used in machine vision, target recognition and detection And other fields [1-2]. Due to the practical application of high precision and high speed requirements for image processing, the study of real-time image processing technology has attracted more and more attention from scholars and engineers. Digital image processing technology contains a very rich content. It is...
applied in different fields and different application requirements. It is necessary to adopt different digital image processing methods to achieve the desired goal\textsuperscript{[3-4]}.

At present, most image processing projects use computer software to complete image processing and analysis tasks. Due to the limitations of the computer's own performance, the speed of completing digital image processing is limited, and the goal of real-time processing cannot be achieved. Therefore, how to efficiently complete the task of image processing analysis is the research focus of real-time image processing projects\textsuperscript{[5-6]}. Today, the development of various industries is inseparable from technological innovation, including microelectronics technology and computer technology is no exception. These include original innovations, technological innovations and application innovations. In these innovations, the development of new fields starts from these innovations. Each innovation will even bring a new and huge market, which is also profound. Affects our production and lifestyle\textsuperscript{[7-8]}. In view of the lack of software processing system in speed and real-time, image processing algorithm using hardware is becoming a research hotspot. A is A programmable logic device widely used today. Combining FPGA technology with image processing technology, it can give full play to the advantages of FPGA hardware design, parallel processing and multi-stage pipeline design, and improve the data processing capacity and speed of image processing system. Compared with the fully customized CIRCUIT ASIC, as a programmable semi-customized circuit, the reconfigurability of FPGA makes the system highly flexible and adaptable\textsuperscript{[9-10]}.

In this paper, through the research of FPGA’s fast image processing algorithm, a design based on FPGA parallel dual template strategy is proposed, and a comparative experiment is designed. The results show that the implementation of mean filtering algorithm based on FPGA parallel dual template is feasible. Give full play to the advantages of FPGA parallel processing data, improve the processing speed of the image algorithm module.

2. Features and Image Processing Algorithms of FPGA

2.1. Features of FPGA

FPGA can enable developers to reuse hardware and software resources. With the development of FPGA, developers can quickly complete embedded systems with customizable hardware and software. FPGA has the following characteristics: flexible development. Many FPGAs provide dedicated function blocks like DSP blocks. It means that in the development of FPGA, these functional blocks in the system can be easily changed in software, compiled hardware and DSP. In addition, different parameters of different implementation types are also very convenient for testing. The development cycle is short and the risk is low. The hardware that needs to be marketed is due to the flexible development method, and the hardware prototype is only produced when the system has been working normally, tested and the performance is acceptable. Has a large number of IP cores. In the development of FPGAs, many manufacturers provide a large number of IP cores. Developers can easily call these IP cores to complete their own designs without repeating work. These IP cores are strictly tested. Performance and stability are guaranteed. Can be used as an ASIC. Using FPGA to design ASIC circuits, users do not need to produce the first chip to get a suitable chip.

2.2. FPGA-Based Image Processing Algorithm

The mean filtering algorithm is not only simple, but also has a fast calculation speed, especially for
Gaussian noise. The mean filtering algorithm uses a 3*3 standard mean filter template, and the filter generates the average of the standard pixels below the template. Then the output response $R$ of the corresponding point mean filter processing is:

$$ R = \frac{1}{9} \sum_{i=1}^{9} Z_i $$

(1)

$Z_i$ is the gray value of the response image covered by the filter. At the same time, the denoising performance of the mean filtering algorithm can be improved by weighting.

The commonly used objective evaluation indexes of the filtering effect of the spatial filtering algorithm are mean square error (MSE), peak signal-to-noise ratio (PSNR) and mean absolute error (MAE), such as:

$$
\begin{align*}
MSE & = \frac{1}{M \times N} \sum_{i=1}^{M} \sum_{j=1}^{N} \left( I(i,j) - \hat{I}(i,j) \right)^2 \\
PSNR & = 10 \log \left( \frac{2^8 - 1}{MSE} \right) \\
MAE & = \frac{1}{M \times N} \sum_{i=1}^{M} \sum_{j=1}^{N} \left| I(i,j) - \hat{I}(i,j) \right|
\end{align*}
$$

(2)

The mean filter algorithm is implemented using a standard 3*3 mean filter template. Lena images with a resolution of 192*192 are added in the range of $[0.1\% , 1\%]$, with 10 different gaussian noise concentrations at intervals of $0.1\%$. Three ways to implement the mean filtering algorithm.

3. Hardware Design of Image Processing Algorithm Based on FPGA

Image algorithm processing subsystem includes storage module, arithmetic unit and control module, which is the core part of the system. The functions of each module are as follows: The storage module mainly stores grayscale image data prepared in advance; The arithmetic unit mainly completes the reading of digital image grayscale data in ROM, the realization of digital image algorithm and the output of data. By using the RAM-based shift register IP core, the neighborhood operation of image processing is realized, and the realization of various digital image processing algorithms is completed. The control module completes the control tasks of the image algorithm processing subsystem to ensure the successful completion of the image processing algorithm and the data transmission after image processing. The FPGA model selected for all experiments in this paper is the DE2-115 development platform of the Cyclone IVE series of Altera Corporation. The 50M clock is used as the internal clock of the FPGA. The model of the PC processor is Intel Core i5-3317U.1.70GHz. Matlab runs on Windows7. On the system, as shown in Table 1.

| Table 1. Operating platform |
|-----------------------------|
| Operating platform | Name |
|----------------------|------|
| FPGA model           | Cyclone IVE DE2-115 |
4. Design and Implementation of Mean Filtering Algorithm

4.1. Realization of the Mean Filtering Algorithm in Three Ways

Matrices and arrays are the core of Matlab. Simulated images are converted to grayscale images after sampling, quantization, and a series of image preprocessing. The image can be equivalently regarded as a matrix, and the grayscale image can be represented by a real matrix. Therefore, this paper uses Matlab software to implement the mean filtering algorithm, which is used as the reference method for the other two means to achieve the mean filtering algorithm. The output results are compared with the results of the hardware mean filtering algorithm. The average filtering algorithm based on FPGA single template is realized. By using the RAM-based shift register IP core, the function of outputting the image grayscale image data covered by the 3*3 filter template is completed, thereby completing the average filtering based on FPGA single template algorithm. The realization of mean filtering algorithm based on FPGA parallel dual template is based on the realization of mean filtering algorithm based on FPGA single template. The mean filtering algorithm strategy based on FPGA parallel dual templates uses two mean filter templates, taking advantage of FPGA's parallel execution, using the same clock signal, and processing Lena grayscale images at the same time. The Lena grayscale image with a resolution of 192*192 used in the experimental test is stored in the ROM, and there is a corresponding address for each pixel. When a certain grayscale value is called, it only needs to be set when the ROM is instantiated. The corresponding address is sufficient. After the image is processed by the mean filter algorithm implemented in matlab software, the mean filter algorithm based on FPGA single template and the mean filter algorithm based on FPGA parallel dual template, the measured objective evaluation index values of each image are shown in Table 2. The mean square error MSE of the three methods is shown in Figure 1.

| Gaussian noise concentration (%) | PSNR | MSE | MAE | PSNR | MSE | MAE | PSNR | MSE | MAE |
|----------------------------------|------|-----|-----|------|-----|-----|------|-----|-----|
| 0.1                              | 25.62| 177.95 | 7.75 | 24.89 | 180.77 | 7.97 | 25.6 | 178.9 | 7.77 |
| 0.2                              | 25.44| 185.74 | 8.24 | 24.62 | 194.32 | 8.49 | 25.42 | 186.55 | 8.26 |
| 0.3                              | 25.31| 191.31 | 8.68 | 24.63 | 193.59 | 8.88 | 25.29 | 192.25 | 8.69 |
| 0.4                              | 25.11| 200.13 | 9.07 | 24.44 | 193.69 | 9.28 | 25.1 | 200.76 | 9.08 |

Table 2. Objective evaluation indicators of mean filtering
| 0.5 | 24.98 | 206.37 | 9.4 | 24.25 | 214.01 | 9.64 | 24.96 | 207.29 | 9.42 |
|-----|-------|--------|-----|-------|--------|-----|-------|--------|-----|
| 0.6 | 24.79 | 215.56 | 9.78| 24.18 | 218.18 | 9.99| 24.77 | 216.46 | 9.8  |
| 0.7 | 24.7 | 220.2  | 10.02| 24.1  | 222.65 | 10.23| 24.68 | 221.14 | 10.04|
| 0.8 | 24.57 | 227.02 | 10.32| 23.98 | 229.56 | 10.52| 24.55 | 227.81 | 10.33|
| 0.9 | 24.4 | 235.91 | 10.62| 23.91 | 234.12 | 10.81| 24.38 | 236.98 | 10.64|
| 1   | 24.33| 239.66 | 10.84| 23.77 | 242.43 | 11.05| 24.31 | 240.64 | 10.86|

**Figure 1.** Mean square error of three methods

It can be seen that the mean value filtering algorithm based on matlab and the mean value filtering algorithm based on FPGA parallel dual template basically coincide. The mean square error (MSE) increases with the increase of the noise density. At the same density, most of the values are smaller than those measured by the implementation of the average filter algorithm based on the FPGA single template. The smaller the MSE value, the better the image. The higher the quality. The peak signal-to-noise ratio (PSNR) tends to decrease as the noise density increases. The curves measured by the implementation of the mean filter algorithm based on matlab and the mean filter algorithm based on the FPGA parallel dual template are basically the same. At the same concentration, the measured values are larger than the mean filter algorithm based on the FPGA single template. PSNR value The larger, the less image distortion. The average absolute error (MAE) increases with the increase of noise density, and the test values of the three methods are relatively close.

4.2. Comparison and Analysis of Experimental Results

The statistics of FPGA resource occupancy and image processing schedule of three methods of mean filtering based on Matlab's mean filtering algorithm implementation, FPGA-based single template mean filtering algorithm implementation, and FPGA-based parallel dual-template mean filtering
algorithm implementation are calculated. The time value is obtained by averaging the experimental image processing algorithm time of 10 times, as shown in Table 3.

| Experimenta l method | Total logic elements | Total combination al functions | Dedicated logic registers | Total memory bits | Time (ms) |
|----------------------|----------------------|--------------------------------|--------------------------|------------------|-----------|
| Matlab               | —                    | —                              | —                        | —                | 267.3     |
| Single_mode          | 673                  | 568                            | 361                      | 829968           | 0.773     |
| Parallel_mode        | 1311                 | 1086                           | 606                      | 2708551          | 0.394     |

The architecture of the FPGA and the processor of the PC are different, and the results of the algorithms it implements can only be analyzed qualitatively. The implementation of the mean filter algorithm based on FPGA parallel dual templates, on the one hand, shortens the time of the image processing algorithm at the expense of FPGA resources. The resources used are about twice the implementation of the mean filter algorithm based on the FPGA single template. After the image processing, the reference index value is relatively close to the realization of the average filter algorithm based on matlab. On the other hand, the time it takes is about half of the implementation of the average filter algorithm based on FPGA single template, which is 678 times better than the reference matlab software programming method. Therefore, on the premise of ensuring image accuracy, the experiment verifies that the implementation of mean filtering algorithm based on FPGA parallel dual template can implement the strategy of mean filtering algorithm more quickly.

5. Conclusion

In recent years, image processing technology has received extensive attention in practical applications, but due to the complexity of image processing algorithms, image processing technology has not been able to solve real-time problems well in practical applications. With the improvement of FPGA device performance, cost reduction and the maturity of development tools, its application research in image processing has been paid more and more attention. In this paper, FPGA is used as a development tool for image processing algorithms. With its parallel execution and fast features, it can optimize the time of image processing algorithms. Using Verilog language to write image processing algorithm programs that can be executed on FPGA, based on FPGA's high-speed hardware calculation and parallel computing advantages, a design based on FPGA parallel dual template strategy to shorten image processing time was completed. The hardware circuit of the image processing algorithm designed and implemented was experimentally verified in the development environment, the data results were analyzed, and the optimization of the FPGA-based parallel dual-template image processing strategy in terms of time optimization was feasible.

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