Electrical characteristic fluctuation of 16-nm-gate high-κ/metal gate bulk FinFET devices in the presence of random interface traps

Sheng-Chia Hsu1,2 and Yiming Li1,2,3*

Abstract
In this work, we study the impact of random interface traps (RITs) at the interface of SiOx/Si on the electrical characteristic of 16-nm-gate high-κ/metal gate (HKMG) bulk fin-type field effect transistor (FinFET) devices. Under the same threshold voltage, the effects of RIT position and number on the degradation of electrical characteristics are clarified with respect to different levels of RIT density of state (Dit). The variability of the off-state current (Ion) and drain-induced barrier lowering (DIBL) will be severely affected by RITs with high Dit varying from 5 × 10^{12} to 5 × 10^{13} eV^{−1} cm^{−2} owing to significant threshold voltage (Vth) fluctuation. The results of this study indicate that if the level of Dit is lower than 1 × 10^{12} eV^{−1} cm^{−2}, the normalized variability of the on-state current, Ion, Vth, DIBL, and subthreshold swing is within 5%.

Keywords: Density of interface traps; Random interface traps; Bulk FinFETs; Interface trap fluctuation; Electrical characteristic fluctuation; Statistical device simulation

Background
For the last decades, the technology of silicon-based CMOS devices suffered significant fabrication challenges and sizeable characteristic variability [1-5]. Characteristics could be affected by various traps in high-κ/metal gate (HKMG) devices [6]. For emerging ultra-scaled transistors, the characteristic degradation induced by interface traps at the interface of SiOx/Si is severe for giga-scale circuit designs [7]. Furthermore, random interface traps (RITs) appearing at the interface of SiOx/Si depend on different fabrication processes of HKMG [8-13]. Except planar MOSFETs, fin-type field effect transistors (FinFETs) with HKMG play a key role in sub-22-nm technology nodes to boost electrical performance [14-16] and suppress various fluctuations. Recent studies reported the density of interface traps (Dit) resulting from the orientations of the vertical fin channel of FinFETs [6,17]. The effects of RITs on sub-22-nm FinFETs have also been reported and compared between different device structures [18,19]. Unfortunately, the impact of RITs on 16-nm-gate HKMG bulk FinFET devices has not been clearly discussed yet.

In this work, we study the DC characteristic fluctuation induced by RITs at the SiOx/Si interface of 16-nm TiN/HfSiON gate stack bulk FinFET devices by using experimentally calibrated three-dimensional (3D) device simulation. Under the same threshold voltage, more than 50% suppressions on the standard deviation of threshold voltage and subthreshold swing (SS) are achieved, benefiting from the nature of the vertical channel, compared with the planar MOSFET devices. By considering different levels of Dit, the effects of RIT position and number on the degradation of electrical characteristics are also examined. This paper is organized as follows: In the ‘Methods’ section, we illustrate the RIT simulation flow. In the ‘Results and discussion’ section, we report the results and discuss the characteristic fluctuation resulting from RITs on 16-nm-gate bulk FinFET devices. Finally, the conclusions are drawn.

Methods
RIT simulation method for FinFET devices
We study Si-based 16-nm-gate HKMG bulk FinFETs and planar MOSFET with amorphous-based titanium nitride/...
hafnium oxide/silicon oxide (TiN/HfO$_2$/SiO$_x$) stacks of gate dielectric and an effective oxide thickness (EOT) of around 0.95 nm (EOT = $T_o + T_h \times \varepsilon_{SiO2}/\varepsilon_{HfO2} = 0.6 + 2 \times 3.9/22 = 0.95$ nm), where $T_o$ is the thickness of SiO$_x$, $T_h$ is the thickness of HfO$_2$, and the dielectric constant of HfO$_2$ is assumed to be 22. An aspect ratio of 4 (i.e., $H_f/W_f = 32$ nm/8 nm = 4), a 30-nm-long source/drain (S/D), and an 8-nm-long S/D extension for the explored FinFET are considered, as shown in Figure 1 (a). The doping applied to the channel ($N_{ch}$), source/drain ($N_{S/D}$), substrate ($N_B$), and source/drain extension regions is $4 \times 10^{18}$ cm$^{-3}$, $5 \times 10^{20}$ cm$^{-3}$, $10^{15}$ cm$^{-3}$, and $6 \times 10^{18}$ cm$^{-3}$ for the n-type 16-nm-gate HKMG bulk FinFET devices, respectively. First, we calibrate the nominal DC characteristic of the studied devices according to the International Technology Roadmap for Semiconductor (ITRS) roadmap for low-power applications, which was experimentally quantified in our recent study, and fix the threshold voltage at 300 mV. To estimate device characteristics, a set of 3D drift-diffusion equations coupled with the density gradient equation for quantum correction is performed [20-23]. The mobility model used in the 3D device simulation involves channel surface roughness, high-field saturation, and impurity scattering. The mobility model was quantified with our device measurements for the best accuracy, and the characteristic fluctuation was validated with the experimentally measured DC baseband data from 15/20-nm CMOS and FinFET devices in our earlier work [24].

To perform 3D device simulation with two-dimensional (2D) interface trap fluctuation (ITF) for each randomly

Figure 1 The RIT simulation technique for the bulk FinFET devices. (a) and (a’) are the device structures. (b)-(b”) are the distribution of ITs. (c) and (c’) illustrate the IT planes. (d) shows the individual trap’s density versus the trap’s energy.
generated device sample, we assume that the size of each RIT (SRIT) is equal to 2 nm × 2 nm at the interface of SiOx/Si. Notably, the value of SRIT is numerically set for the simulation of ITF [2,25]. To generate RITs for the statistical device simulation of ITF, we first generate 3,389 acceptor-like traps marked as pink color in the three large 2D planes for the n-type FinFET device, as shown in Figure 1, and the corresponding concentration of RITs is around 1.5 × 10^{12} cm^{-2} [26,27]. The total number of generated acceptor-like traps follows the Poisson distribution, as shown in Figure 1 (b)-(b”). Then, we partition the large planes into many subplanes and map them to form a surface of RITs, as shown in Figure 1(c), where the number of traps in the subplanes varies from 0 to 6 at the top side and from 0 to 14 at the lateral sides, and the average number of interface traps is 3, 8, and 8, respectively. The concentration of each RIT (N_{RIT}) on a subplane is randomly assigned according to the RIT’s energy following the relationship, as shown in Figure 1 (d). Then, the level of D_{it} is the total product of (N_{it} × SRIT) divided by the total area of the SiOx/Si interface. Ultimately, we repeat this process until all subplanes are assigned. Notably, each subplane with RITs is numerically solved with the quantum mechanically corrected device model, where the RITs appear at the right-hand side of the Poisson equation.

Notably, the D_{it} varies with respect to the different process treatments on the TiN/HfSiON gate stacks [9,11,13], so we also consider the impact of three different D_{it} levels on device performance degradation. The ranges of high, typical, and low D_{it} vary from 5 × 10^{12} to 5 × 10^{13} eV^{-1} cm^{-2}, 1 × 10^{12} to 1 × 10^{13} eV^{-1} cm^{-2}, and 5 × 10^{11} to 5 × 10^{12} eV^{-1} cm^{-2}, respectively. For the p-type devices, we have a similar simulation setting with modification of the acceptor-like traps to donor-like traps. For the planar MOSFET ITF simulation, it follows

![Figure 2: I_d-V_G curves of the studied devices with different D_{it} levels.](image)

The line indicates the I_d-V_G of a fresh sample. (a, b) n-/p-type bulk FinFET and (c, d) n-/p-type planar MOSFET devices.
our recent work, as shown in Figure 1 (a’), (b’), and (c’), and the details could be found in [7,28].

Results and discussion
The nominal $V_{th}$ for the fresh device (i.e., device with ultra-low $D_{it}$) is calibrated to 300 mV using a constant-current method. To meet the ITRS roadmap for low-power applications, the voltages applied for the 16-nm-gate HKMG bulk FinFET and planar MOSFET devices were 0.6 and 0.8 V, respectively. As shown in Figure 2, we firstly simulate the RIT-fluctuated $I_D$-$V_G$ curves for the n-/p-type bulk FinFET (Figure 2a,b) and n-/p-type planar MOSFET (Figure 2c,d) devices with different levels of $D_{it}$, respectively. For all devices, the magnitude of ITF becomes smaller as the level of $D_{it}$ decreases. The inset tables list the estimated fluctuation of $I_{on}$ ($\sigma_{I_{on}}$), $I_{off}$ ($\sigma_{I_{off}}$), and $V_{th}$ ($\sigma_{V_{th}}$) for devices with different levels of $D_{it}$. As shown in Figure 3, we compare the ITs-fluctuated $V_{th}$ under different levels of $D_{it}$, where the normalized standard deviation ($\sigma/\mu$) of $V_{th}$ is calculated, and $\sigma$ and $\mu$ are the standard deviation and average of the fluctuated cases, respectively. The $V_{th}$ shifts and its normalized standard deviation becomes larger when the level of $D_{it}$ is increased. Both the n- and p-type FinFET devices, as shown in Figure 3a,c, have comparable magnitudes of $\sigma/\mu$ which are smaller than that of the planar MOSFET devices (about 50% reduction), as shown in Figure 3b,d. Nevertheless, the ITs-fluctuated $V_{th}$ is strongly governed by high $D_{it}$ varying from $5 \times 10^{12}$ to $5 \times 10^{13}$ eV$^{-1}$ cm$^{-2}$. In Figure 4, we show the $I_{on}$ versus $I_{off}$ for all devices with different levels of $D_{it}$. The results of the normalized standard deviation of $I_{on}$ and $I_{off}$ imply that the advantage of the vertical channel in the suppression of ITF will be weakened when the level of $D_{it}$ is increased; for example, the ellipsoid-shape distribution of $I_{on}$ and $I_{off}$ is broadened as the $D_{it}$ increases. For the cases of low $D_{it}$, as shown in Figure 4a,c, the FinFET $\sigma/\mu$ of $I_{on}$ and $I_{off}$ is about three times smaller than that of...
the planar device, owing to their significant structural dominance. However, such strength is destroyed with the increasing level of $D_{it}$; as listed in the inset tables, the normalized standard deviations are considerable and comparable between the two devices for the cases of high $D_{it}$, in particular, the $\sigma/\mu$ of $I_{off}$.

The degradation of SS becomes more critical when the level of $D_{it}$ increases. Owing to large gate capacitance ($C_g$) coupling in FinFETs, the dependence relationship of ITs-fluctuated SS versus drain-induced barrier lowering (DIBL) is reduced, as shown in Figure 5a,c; however, the distribution of SS versus DIBL exhibits a negative dependency in the planar MOSFETs, as shown in Figure 5b,d. The significant dependence relationship of ITs-fluctuated SS versus DIBL indicates that the characteristic degradation was caused by an even stronger short-channel effect [29]. To maximize $V_{DD}$ scaling for logical application, the fluctuations of transconductance ($g_m$) and subthreshold swing must be minimized. As shown in Figure 6, the ITs-fluctuated transconductances are calculated for the studied devices with different levels of $D_{it}$. The flatter normalized standard deviations (within 2%) of the maximum transconductance ($g_{m,max}$) listed in the inset tables are found for the FinFET devices with high $D_{it}$, as shown in Figure 6a,c.

To go deep into the physics of the results reported above, as shown in Figure 7, we now examine the advantage of the vertical structure and the effect of random distribution (i.e., the random position) and the random number of ITs on the surface potential profiles of the ITs-fluctuated devices. As shown in the inset of Figure 7a, along the channel direction (Z-direction) from the source (S) to the drain (D) at the interface of SiO$_2$/Si on the top gate, the two profiles of conduction band are extracted...
Figure 5 SS versus DIBL for the studied devices with different $D_i$ levels. (a, c) n-/p-type bulk FinFET and (b, d) n-/p-type planar MOSFET devices.

Figure 6 ITs-fluctuated $g_{m_{\text{max}}}$ for the studied devices with different $D_i$ levels. (a, c) n-/p-type bulk FinFET and (b, d) n-/p-type planar MOSFET devices.
and compared for the fresh FinFET device and the FinFET device with high $D_{it}$ under off-state condition, where the barrier difference induced by a single interface trap is about 0.1365 eV. Similarly, as shown in Figure 7b, for the planar MOSFET device, the barrier difference is about 0.2732 eV. Comparison between Figure 7a and 7b indicates the significant structural effect; the planar MOSFET device severely suffers from the impact of RIT compared to the FinFET one. The coupling of gate electrodes from both the lateral sides to the top gate enhances the $C_g$, and thus, it effectively reduces the impact of RITs on the energy band. The findings of this comparison confirm the superiority of a 3D channel structure and the aforementioned results. The random position effect of RITs is further examined for the FinFET device. For similar $I_{on}$ and different $I_{off}$, the two illustration cases (case A and case B) shown in Figure 7c have the same number of ITs (15 ITs) but different $V_{th}$ owing to the different positions of RITs. For similar $I_{off}$ and different $I_{on}$, the numbers of ITs for the two illustration cases (case A and case C) shown Figure 7c are 15 and 17. Therefore, according to the random number effect, they have different $V_{th}$ because the effective $D_{it}$ of case C is higher than that of case A. Thus, the device has similar $I_{off}$ and different $I_{on}$.

**Conclusions**

In this work, we have investigated the impact of RITs on n-/p-type 16-nm-gate HKMG bulk FinFETs using an experimentally validated device simulation technique. We examined the ITs-fluctuated short-channel effect (SCE) parameters for the bulk FinFET and planar MOSFET devices. Benefiting from the improved gate controllability and stronger gate coupling capability, the estimated normalized standard deviation indicates that the 16-nm-gate HKMG bulk FinFET devices can effectively suppress the DC characteristic and SCE parameter fluctuations induced by RITs with respect to different levels of $D_{it}$. The insets of Figures 3, 4, 5, 6 listed the fluctuation magnitudes of $I_{off}$ and DIBL which are severely governed by RITs with high $D_{it}$ level ranging from $5 \times 10^{12}$ to $5 \times 10^{13}$ eV$^{-1}$ cm$^{-2}$. Due to the strong screening effect for devices under high gate bias, the fluctuation magnitudes of SS and $g_m$ induced by different levels of RITs are minimized. To effectively control the magnitude of normalized fluctuation within 5% for the $V_{th}$, $I_{off}$, $I_{on}$, SS, and DIBL, the $D_{it}$ should be lower than $1 \times 10^{12}$ eV$^{-1}$ cm$^{-2}$. We are currently designing a proper experiment to measure the characteristic fluctuation induced by RITs and study the random bulk traps’ influence together with RITs on device characteristic variability.
Abbreviations

$\alpha_{\text{L}}$: Standard deviation of $V_{\text{th}}$, $\alpha_{\text{V}}$: Standard deviation of $V_{\text{th}}$, $\alpha_{\text{C}}$: Standard deviation of $V_{\text{th}}$; 2D: Two-dimensional; 3D: Three-dimensional; $C_{\text{g}}$: Gate capacitance; DBL: Drain-induced barrier lowering; $D_{\text{g}}$: Density of interface traps; EOT: Effective oxide thickness; FinFET: Fin-type field effect transistor; $g_{\text{m}}$: Transconductance; $g_{\text{off}}$: Maximum transconductance; HKMG: High k/metal gate; ITs: Interface traps; $I_{\text{off}}$: Off-state current; $I_{\text{on}}$: On-state current; $N_{\text{ch}}$: Channel doping; $N_{\text{s}}$: Substrate doping; $N_{\text{it}}$: RIT concentration; $N_{\text{so}}$: Source/drain doping; RTs: Random interface traps; SCE: Short-channel effect; $S_{\text{t}}$: RIT size; $S_{\text{s}}$: Subthreshold swing; $V_{\text{th}}$: Threshold voltage.

Competing interests

The authors declare that they have no competing interests.

Authors’ contributions

S-Ch performed the numerical simulation and data analysis. YL conducted the entire study including manuscript preparation. Both authors read and approved the final manuscript.

Acknowledgements

This work was supported in part by the Ministry of Science and Technology, Taiwan, under contract no. NSC-102-2221-E-009-161 and no. MOST-103-2221-E-009-180, and by TSMC, Hsinchu, Taiwan, under a 2012-2013 grant.

Author details

1. Parallel and Scientific Computing Laboratory, National Chiao Tung University, 1001 Ta-Hsueh Road, Hsinchu 300, Taiwan. 2. Institute of Communications Engineering, National Chiao Tung University, 1001 Ta-Hsueh Road, Hsinchu 300, Taiwan. 3. Department of Electrical and Computer Engineering, National Chiao Tung University, 1001 Ta-Hsueh Road, Hsinchu 300, Taiwan.

Received: 29 June 2014 Accepted: 2 November 2014

Published: 25 November 2014

References

1. Li Y, Cheng HW, Chiu YY, Yu CY, Su HW: A unified 3D device simulation of random dopant, interface trap and work function fluctuations on high-k/metal gate device. In Proceedings of the IEEE International Electron Devices Meeting. Washington, DC: IEEE, 2011:107–110.

2. Cheng HW, Li FH, Han MH, Yu CY, Yu CH, Lee KG, Li Y: Device simulation of work-function and interface trap fluctuations on high-k/metal gate devices. In Proceedings of the International Electron Devices Meeting. San Francisco: IEEE, 2011:379–382.

3. Wang X, Brown AR, Cheng B, Asenov A: Statistical variability and reliability in nanoscale FinFETs. In Proceedings of the International Electron Devices Meeting. Washington, DC: IEEE, 2011:103–106.

4. Penumatcha AV, Svanvondo S, Cooper JA: Limitations of the high-low C-V technique for MOS interfaces with large time constant dispersion. IEEE Trans Electron Devices 2013, 60:232–236.

5. Li Y, Cheng HW, Chiu YY: Interface traps and random dopants induced characteristic fluctuations in emerging MOSFETs. Microelectron Eng 2011, 88:1269–1271.

6. Tallarico AN, Cho M, Franco J, Ritzenhauer T, Togo M, Horiguchi N, Groeseneken G, Crupi F: Impact of the substrate orientation on CHC reliability in n-FinFETs—separation of the various contributions. IEEE Trans Device Mater Reliab 2014, 14:52–56.

7. Li Y, Cheng HW: Random interface-traps-induced electrical characteristic fluctuation in 16-nm-gate high-k/metal gate complementary metal-oxide-semiconductor device and inverter circuit. Jpn J Appl Phys 2012, 51:04 DC08.

8. Takanaka M, Zhang R, Takagi S: MOS interface engineering for high-mobility Ge MOS. In Proceedings of the IEEE International Reliability Physics Symposium. Anaheim, CA: IEEE, 2013:1–11–4C.1.8.

9. Lee JW, Simon E, Veloso A, Cho MJ, Aturimu H, Boccardi G, Ragnanion LA, Chiarella T, Horiguchi N, Thean A, Groeseneken G: Low frequency noise analysis for post-treatment of replacement metal gate. IEEE Trans Electron Devices 2013, 60:2960–2963.

10. Mao LF: Interface traps and quantum size effects on the retention time in nanoscale memory devices. Nanoscale Res Lett 2013, 8:369.

11. Kapila G, Kaczer B, Nakkaents A, Colaent N, Groeseneken G: Direct measurement of top and sidewall interface trap density in SOI FinFETs. IEEE Electron Device Lett 2007, 28:232–234.

12. O’Sullivan BJ, Hurley PK, Leveugle C, Das JH: Si(100)-SiO2 interface properties following rapid thermal processing. J Appl Phys 2001, 89:3811–3820.

13. Tettamanzi GC, Paul A, Lee S, Mehrotra SR, Colaent N, Biesmans S, Klimeck G, Rogge S: Interface trap density metrology of state-of-the-art undoped Si n-FinFETs. IEEE Electron Device Lett 2011, 32:440–442.

14. Chen SH, Liao WS, Yang HC, Wang SJ, Liow YG, Wang H, Hu H, Wang MC: High-performance III-V MOSFET with nano-stacked high-k gate dielectric and 3D fin-shaped structure. Nanoscale Res Lett 2012, 7:431.

15. Bijesh R, Ok I, Baykan M, Hobbs C, Majhi P, Jamen R, Datta S: Hole mobility enhancement in uniaxially strained SiGe FinFET analysis and prospects. In Proceedings of the IEEE 69th Annual Device Research Conference. Santa Barbara: IEEE, 2011:237–238.

16. Koh SM, Samudra GS, Yeo YC: Contact technology for strained nFinFETs with silicon-carbon source/drain stressors featuring sulfur implant and segregation. IEEE Trans Electron Devices 2012, 59:1046–1055.

17. Paul A, Tettamanzi GC, Lee S, Amodio SR, Colaent N, Biesmans S, Rogge S, Klimeck G: Interface trap density metrology from sub-threshold transport in highly scaled undoped Si FinFETs. J Appl Phys 2011, 110:124507.

18. Chen YY, Huang WT, Hsu SC, Chang HT, Chen CY, Yang CM, Chen LW, Li Y: Statistical device simulation of intrinsic parameter fluctuation in 16-nm gate n- and p-type bulk FinFETs. In Proceedings of the IEEE International Conference on Nanotechnology. Beijing: IEEE, 2013:442–445.

19. Wang Y, Wei K, Liu X, Du Q, Kang J: Random interface trap induced fluctuation in 22nm high-k/metal gate junctionless and inversion-mode FinFETs. In Proceedings of the IEEE International Symposium on VLSI Technology, Systems, and Applications. Hsinchu: IEEE, 2013:1–2.

20. Ancona MG: Density-gradient theory: a macroscopic approach to quantum confinement and tunneling in semiconductor devices. J Comp Elect 2011, 10:65–97.

21. Li Y, Sze SM, Chao TS: A practical implementation of parallel dynamic load balancing for adaptive computing in VLSI device simulation. Eng Comput 2002, 18:124–137.

22. Tang TW, Wang X, Li Y: Discretization scheme for the density-gradient equation and effect of boundary conditions. J Comp Elect 2002, 13:389–398.

23. Odataka S: Multidimensional discretization of the stationary quantum drift-diffusion model for ultrasmall MOSFET structures. IEEE Trans Comput Aided Des Integr Circuits Syst 2004, 23:837–842.

24. Li Y, Yu SM, Hwang JR, Yang FL: Discrete dopant fluctuated 20 nm/15 nm-gate planar CMOS. IEEE Trans Electron Devices 2008, 55:1449–1455.

25. Andricapria P, Tuinhout PH, Vries BD, Wils NH, Scholten AJ, Kaassen DBM: Impact of interface states on MOS transistor mismatch. In Proceedings of the International Electronic Devices Meeting. Baltimore: IEEE, 2009:711–714.

26. Covern NEB: Intersitial traps and diffusion in epitaxial silicon films. Appl Phys Lett 1994, 64:2646–2648.

27. Han G, Tass Z: Application of quadrupole ion trap for the accurate mass determination of submicron size charged particles. J Appl Phys 1995, 77:4245–4250.

28. Li Y, Cheng HW: Statistical device simulation of physical and electrical characteristic fluctuations in 16-nm-gate high-k/metal gate MOSFETs in the presence of random discrete dopants and random interface traps. Solid-State Electron 2012, 77:12–19.

29. Mizuta T, Kumar A, Hiramoto T: Analysis of transistor characteristics in distribution tails beyond ±1 of 11 billion transistors. In Proceedings of the International Electronic Devices Meeting. Washington, DC: IEEE, 2013:826–829.

Cite this article as: Hsu and Li Nanoscale Research Letters 2014 9:633

doi:10.1186/1556-276X-9-633