Polynomial Circuit Verification using BDDs

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Abstract

Verification is one of the central tasks during circuit design. While most of the approaches have exponential worst-case behaviour, in the following techniques are discussed for proving polynomial circuit verification based on Binary Decision Diagrams (BDDs). It is shown that for circuits with specific structural properties, like e.g. tree-like circuits, and circuits based on multiplexers derived from BDDs complete formal verification can be carried out in polynomial time and space.

1 Introduction

With the increasing complexity of digital circuits, ensuring functional correctness is a challenging problem. Various techniques for verification have been proposed. While simulation and emulation can be carried out very fast, the coverage that can be obtained is very low. Only formal verification approaches can ensure 100% correctness (see e.g. [7]). Several automatic proof techniques have been proposed for the bit-level, like e.g. BDDs or SAT solvers, and for the word-level, like WLDDs or SMT solvers. For an overview see [6]. In the following, only BDDs are considered, while many of the arguments can directly be transferred to other proof techniques as well.

Based on formal proof techniques, correctness can be ensured, but the techniques have exponential worst case behavior and for this are known to not scale well in general. Even in cases where the final result can efficiently be represented, intermediate results might be too large to be handled.

Example 1. Consider the general formulation of circuit equivalence based on a miter circuit in Figure 1. If the two circuits Circuit 1 and Circuit 2 are functionally equivalent, the output signal out becomes 0. This can be represented trivially e.g. by a BDD. But dependent on the circuits, the construction of the intermediate BDDs might fail.
This has already been observed in early applications of BDDs and as a consequence approaches have been presented to reduce the peak size during the construction [16, 14, 11]. These techniques were either heuristic in nature or had prohibitive large run times. Efficient construction could not be guaranteed in general.

Recently it has been proven in [8] that for different kind of adder circuits a complete formal verification based on BDDs can be carried out in polynomial time and space. This not only holds for the representation of the outputs, but for the complete construction.

While the study in [8] was restricted to adders, in the following it is shown that for restricted types of circuits polynomial verification based on BDDs can be carried out. This contains tree-like circuits and circuits derived by a 1-to-1 mapping from BDDs. The later ones have intensively been studied and are known for their good testability properties (see e.g. [11, 12]).

2 Notation and Definition

Let \( f : B^n \rightarrow B^m \) be a Boolean function over variable set \( X_n = \{x_1, \ldots, x_n\} \).

2.1 Circuit

A circuit is a Directed Acyclic Graph (DAG) \( G(V, E) \) with vertex set \( V \) and edges \( E \). It represents a Boolean function \( f : B^n \rightarrow B^m \) with \( n \) variables that are associated with the Primary Inputs (PIs) and \( m \) output signals associated with the Primary Outputs (POs). The internal nodes are associated with basic
Figure 2. MUX representation by basic gates

Boolean functions, like AND, OR, NAND, NOR or INV (=inverter). The edges represent the signals connecting the nodes, PIs and POs.

**Example 2.** The circuit for function \( f = x \cdot g + x \cdot h \) is shown in Figure 2. This circuit is also denoted as multiplexer – MUX for short – in the following.

### 2.2 Binary Decision Diagrams

Reduced ordered Binary Decision Diagrams (BDDs) \([4, 9]\) are DAGs where a Shannon decomposition

\[
f = \overline{x}_i f_{x_i} + x_i f_{\overline{x}_i} (1 \leq i \leq n)
\]

is carried out in each node. The size of a BDD is the number of non-terminal nodes.

An important property of BDDs is that the synthesis operations, like AND, OR or composition, can be carried out in polynomial time and space using the apply-operation \([3]\). This can also be described by the operator if-then-else (ite) \([2]\), since \( \text{ite} \) allows for an easy and elegant implementation in a BDD package. A sketch of the algorithm is shown in Figure 3, where \( T (=\text{then}) \) and \( E (=\text{else}) \) denote the high- and low-successors, respectively, and e.g. \( F_{x_i} (F_{\overline{x}_i}) \) is the cofactor to \( 1 \) \((0)\) with respect to variable \( i \):

The \( \text{ite} \)-operator has a polynomial worst case behavior, i.e. for graphs \( F, G \) and \( H \) the result is bound by \( O(|F| \cdot |G| \cdot |H|) \). This bound holds under the assumption of an optimal hashing in \( O(1) \). But also in the case of a worst case behavior of the hashing function, \( \text{ite} \) remains polynomial (see \([13]\)).

Simple examples for terminal cases that might occur are as follows:

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\(^1\)Notice that in the following for the discussion and the proofs BDDs without CEs are considered.
ITE(F, G, H) {
    if (terminal case) {
        return (result of terminal case);
    } else {
        if ((F, G, H) ∈ computed-table)
            return computed_table (F, G, H);
        else {
            let x_i be the top variable of (F, G, H);
            T = ITE(F_{x_i}, G_{x_i}, H_{x_i});
            E = ITE(F_{\overline{x_i}}, G_{\overline{x_i}}, H_{\overline{x_i}});
            if (T = E) return T;
            R = find_or_add_unique_table(v, T, E);
            insert_computed_table (F, G, H, R);
            return R;
        }
    }
}

Figure 3. ITE algorithm

- if (F == 1 || G == H) return G;
- if (F == 0) return H;

In software implementations of BDDs, typically more complex cases are considered to allow for an early termination of the recursive calls (see e.g. [17, 18]).

2.3 Symbolic Simulation

To build the BDDs for the output signals of a circuit, the circuit is traversed in a topological order starting from the inputs. For the inputs signals the corresponding BDDs are initially generated. Then, for each gate in the circuit the corresponding synthesis operation based on \(ite\) is carried out. This process is called symbolic simulation in the following.

Example 3. The symbolic simulation for a circuit consisting of a single AND gate is shown in Figure 4.

3 Polynomial Verification

While for several types of circuits it is known that the BDD representing the output has a polynomial size, it is not obvious that during the construction of the output BDD (significantly) larger intermediate results are computed (see Example 1). In the following we consider different circuit structures and show that under some constraints a polynomial symbolic simulation can be ensured.

3.1 Tree-like Circuits

For tree-like circuits, i.e. circuits without fanouts, it is well known that the BDDs representing the output function have linear size. This means that for each input variable only a single node is needed, if
the variable ordering results from a Depth First Search (DFS) traversal of the circuit. This is typically proven by induction (see e.g. Lemma 5.3 (Section 5.4.1) in [9]). But this again only considers the BDD for the output of the circuit, but not during the construction. For this, in the following we will use a different argument to obtain the same result. But this argument can later be generalized to also reason about circuits that do not have a tree-like structure.

For the AND-gate the value 0 (1) is a controlling value (cv) (non-controlling value (ncv)), since the output is (not) determined, if one of the inputs assume this value. In a similar way these values can be described for other Boolean gates, like NAND, OR or NOR.

When constructing BDDs based on the ite-operator introduced above, a cv directly leads to a terminal case and by this ends the recursion. This implies that not only the final BDDs have a linear size in the number of input variables, but also during the construction it can never occur that additional nodes are generated.

The same argument can be applied to general circuits.

**Theorem 1.** Let \( g \) be a BDD representing a circuit and \( x_i \) a variable that does not occur in \( g \). Then \( f = x_i \cdot g \) can be constructed in \( O(|g|) \), if \( x_i \) is the top-variable in the ordering of \( f \).

**Proof.** For the case of \( x_i = 0 \), in the recursive call of ite, directly a terminal case is reached, since 0 is the cv for the AND-gate. On the 2nd branching, the BDD of \( g \) has to be traversed, but no additional nodes are created.

The same results hold, if the AND-operation is substituted by OR, NAND or NOR or for the complemented variable \( \overline{x}_i \). Also the same argument can be applied if we consider gates with more than two inputs, e.g. a 4-input AND. Then the gate has to be first decomposed into 2-input gates and then the theorem can be applied.

### 3.2 General Circuits

For arbitrary circuits without any restrictions on the structure, polynomial symbolic simulation can not be ensured. E.g. in the case of the multiplier function in contrast each BDD construction will lead
to an exponential blow-up, since the final BDD has an exponential size (see [5]). But, if the sizes of the BDDs representing the internal signals of the circuit are polynomially bound, the complete construction of the output BDDs can be carried out efficiently:

**Theorem 2.** Let $C$ be a circuit over $n$ input variables. If the BDD size of each internal signal of the circuit has a size polynomial in $n$, then the complete symbolic simulation of the circuit can be carried out in polynomial time and space.

**Proof.** This directly follows from the observation that $ite$ has a polynomial worst case behavior and the fact that each internal signal has a polynomial BDD representation. \qed

The theorem can be easily be relaxed to not consider all internal signals.

**Remark 1.** To ensure polynomial worst case behavior not all internal signals have to be considered, while it is sufficient to have a constant number $c$ of gates between these signals. The number $c$ should not be too large, since this would result in a still polynomial but for practical reasons too large estimate.

This property will be used in Section 3.3 and was also (implicitly) applied in [8] for the special case of adder circuits, i.e. the *Conditional Sum Adder* (CoSA) particularly.

### 3.3 BDD-Circuits

A BDD-circuit results from a BDD by substituting each internal node of the BDD by a MUX (see Figure 2).

**Example 4.** For the OR-function $f_{OR} = x_1 + x_2$ the BDD is shown on the left hand side of Figure 5. The resulting circuit is shown on the right hand side, where each internal node is substituted by a MUX cell. Notice that the circuit is drawn upside down compared to the BDD in the common way that the outputs are at the lower end of the figure.

Since this is a 1-to-1 mapping, it is obvious that the BDD for each of the signals in the circuit have polynomial size. Thus, Theorem 2 can be applied. When we also want to argue over the internal signals of the MUX, the way the MUX is represented has to be considered as well. If we assume the standard realization from Figure 2 and following Remark 1 it can be observed:

1. The side input $x_i$ only consists of one node.
2. The negation of this input also consists of one node only.
3. Due to the ordering restriction of the original BDD, the function represented at the inputs (beside the selection signal) of the MUX are independent of $x_i$ (see also Theorem 1).
4. Thus, the internal signals at the outputs of the AND-gates have polynomial sizes.
5. Due to the polynomial worst-case behavior of the $ite$-operator, also the output of the OR-gate has polynomial size.

In summary, we obtain:

**Theorem 3.** For BDD-circuits with MUX using the standard representation the complete symbolic simulation of the circuit can be carried out in polynomial time and space.
4 Conclusion

Ensuring verification of designed circuits is a central aspect of successful chip design in the future. The concept of polynomial circuit verification has only been demonstrated before for adder circuits, while here it has been shown to be applicable to more general Boolean functions. This includes functions that can be represented by tree-like circuits. Furthermore, it has been shown that circuits derived from BDDs by a 1-to-1 mapping can efficiently be formally verified.

Future work will go into two directions: On the one hand side the class of functions that can be polynomially verified using BDDs should be extended. Besides this, alternative proof concept can be investigated, like it has been done successfully using BMDs for multipliers (see [15]). The investigation becomes more difficult here, since polynomial synthesis operations, like \( \text{ite} \) for BDDs, do not exist in general in this case.

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