Pushdown Timed Automata:  
a Binary Reachability Characterization  
and Safety Verification*

Zhe Dang

School of Electrical Engineering and Computer Science  
Washington State University  
Pullman, WA 99164, USA  
zdang@eecs.wsu.edu

Abstract. We consider pushdown timed automata (PTAs) that are timed automata (with dense clocks) augmented with a pushdown stack. A configuration of a PTA includes a control state, dense clock values and a stack word. By using the pattern technique, we give a decidable characterization of the binary reachability (i.e., the set of all pairs of configurations such that one can reach the other) of a PTA. Since a timed automaton can be treated as a PTA without the pushdown stack, we can show that the binary reachability of a timed automaton is definable in the additive theory of reals and integers. The results can be used to verify a class of properties containing linear relations over both dense variables and unbounded discrete variables. The properties previously could not be verified using the classic region technique nor expressed by timed temporal logics for timed automata and CTL* for pushdown systems. The results are also extended to other generalizations of timed automata.

1 Introduction

A timed automaton [3] can be considered as a finite automaton augmented with a number of dense (either real or rational) clocks. Clocks can be reset or progress at rate 1 depending upon the truth values of a number of clock constraints in the form of clock regions (i.e., comparisons of a clock or the difference of two clocks against an integer constant). Due to their ability to model and analyze a wide range of real-time systems, timed automata have been extensively studied in recent years (see [1,35] for recent surveys). In particular, by using the standard region technique, it has been shown that region reachability for timed automata is decidable [3]. This fundamental result and the technique help researchers, both theoretically and practically, in formulating various timed temporal logics [2,4,5,6,27,32,33,34] and developing verification tools [11,26,30].

Region reachability is useful but has intrinsic limitations. In many real-world applications [14], we might also want to know whether a timed automaton satisfies a

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non-region property, e.g.,

\[ x_1 - 2x_2 + x_3' > x_1' + 4x_2' - 3x_3 \]

holds whenever clock values \((x_1, x_2, x_3)\) can reach \((x_1', x_2', x_3')\). Recently, Comon and Jurski [16] have shown that the binary reachability of a timed automaton is definable in the additive theory of reals augmented with an integral predicate that tells whether a term is an integer, by flattening a timed automaton into a real-valued counter machine without nested cycles [13]. The result immediately paves the way for automatic verification of a class of non-region properties that previously were not possible using the region technique.

On the other hand, a strictly more powerful system, called a pushdown timed automaton (PTA), can be obtained by augmenting a timed automaton with a pushdown stack. PTAs are particularly interesting because they contain both dense clocks and unbounded discrete structures. They can be used to study, for instance, a timed version of pushdown processes [22] or real-time programs with procedure calls. A configuration of a PTA is a tuple of a control state, dense clock values, and a stack word. The binary reachability of a PTA is the set of all pairs of configurations such that one can reach the other. Comon and Jurski’s result for timed automata inspires us to look for a similar result for PTAs. Is there a decidable binary reachability characterization for PTAs such that a class of non-region properties can be verified? The main result in this paper answers this question positively.

There are several potential ways to approach the question. The first straightforward approach would be to treat a PTA as a Cartesian product of a timed automaton and a pushdown automaton. In this way, the binary reachability of a PTA can be formulated by simply combining Comon and Jurski’s result and the fact that pushdown automata accept context-free languages. Obviously, this is wrong, since stack operations depend on clock values and thus can not be simply separated. The second approach is to closely look at the flattening technique of Comon and Jurski’s to see whether the technique can be adapted by adding a pushdown stack. However, the second approach has an inherent difficulty: the flattening technique, as pointed out in their paper, destroys the structure of the original timed automaton, and thus, the sequences of stack operations can not be maintained after flattening.

Very recently, the question has been answered positively, but only for integer-valued clocks (i.e., for discrete PTAs). It has been shown in [19] that the binary reachability of a discrete PTA can be accepted by a nondeterministic pushdown automaton augmented with reversal-bounded counters (NPCA), whose emptiness problem is known to be decidable [28]. However, as far as dense clocks are concerned, the automata-based technique used in [19] does not apply. The reason is that traditional automata theories do not provide tools to deal with machines containing both real-valued counters (for dense clocks) and unbounded discrete data structures.

In order to handle dense clocks, we introduce a new technique, called the pattern technique, by separating a dense clock into an integral part and a fractional part. Consider a pair \((v_0, v_1)\) of two tuples of clock values. We define (see Section 3 for details) an ordering, called the pattern of \((v_0, v_1)\), on the fractional parts of \(v_0\) and \(v_1\). The definition guarantees that there are only a finite number of distinct patterns. An equivalent relation “\(\approx\)” is defined such that \((v_0, v_1)\approx(v'_0, v'_1)\) iff \(v_0\) and \(v'_0\) \((v_1\) and \(v'_1\) will
also) have the same integral parts, and both \((v_0, v_1)\) and \((v'_0, v'_1)\) have the same pattern. The \(\approx\) essentially defines an equivalent relation with a countable number of equivalent classes such that the integral parts of \(v_0\) and \(v_1\) together with the pattern of the fractional parts of \(v_0\) and \(v_1\) determine the equivalent class of \((v_0, v_1)\). A good property of \(\approx\) is that it preserves the binary reachability: \(v_0\) can reach \(v_1\) by a sequence of transitions iff \(v'_0\) can reach \(v'_1\) by the (almost) same sequence of transitions, whenever \((v_0, v_1)\approx(v'_0, v'_1)\). Therefore, the fractional parts can be abstracted away from the dense clocks by using a pattern. In this way, by preserving the (almost) same control structure, a PTA can be transformed into a discrete transition system (called a pattern graph) containing discrete clocks (for the integral parts of the dense clocks) and a finite variable over patterns. By translating a pattern back to a relation over the fractional parts of the clocks, the decidable binary reachability characterization of the pattern graph derives the decidable characterization (namely, \((D + NPCA)\)-definable) for the PTA, since the relation is definable in the additive theory of reals. With this characterization, it can be shown that the particular class of safety properties that contain mixed linear relations over both dense variables (e.g., clock values) and discrete variables (e.g., word counts) can be automatically verified for PTAs. For instance, whenever configuration \(\alpha\) can reach configuration \(\beta\), 
\[
\alpha_{x_1} + 2\beta_{x_2} - \alpha_{x_2} > \#_a(\alpha_w) - \#_b(\beta_w)
\]
holds.

Fractional orderings are an effective way to abstract the fractional parts of dense clocks. The idea of using fractional orderings can be traced back to the pioneering work of Alur and Dill in inventing the region technique [3]. Essentially, the region technique makes a finite partition of the clock space such that clock values in the same region give the same answer to each clock constraint in the system (i.e., the automaton of interest). Comon and Jurski [16] notice that Alur and Dill’s partition is too coarse in establishing the binary reachability of a timed automata. They move one step further by bringing in the clock values before a transition was made. But Comon and Jurski’s partition is still finite, since their partition, though finer than Alur and Dill’s, is still based on answers to all the clock constraints (there are finitely many of them) in the system. In this paper, \(\approx\) deduces an infinite partition of both the initial values \(v_0\) and the current values \(v_1\) of the clocks. Essentially, this partition is based on answers to all clock constraints (not just the ones in the system). That is, \(\approx\) is finer than Comon and Jurski’s partition as well as Alur and Dill’s. This is why the flattening technique [16] destroys the transition structure of a timed automaton but the technique presented in this paper is able to preserve the transition structure. A class of Pushdown Timed Systems...
was discussed in [10]. However, that paper focuses on region reachability instead of binary reachability.

This paper is organized as follows. Section 2 reviews a number of definitions and, in particular, defines a decidable formalism in which the binary reachability of PTAs are expressed. Section 3 and Section 4 give the definition of patterns and show the correctness of using patterns as an abstraction for fractional clock values. Section 5 and Section 6 define PTAs and show that the pattern graph of a PTA has a decidable binary reachability characterization. Section 7 states the main results of the paper. In Section 8, we point out that the results in this paper can be extended to many other infinite state machine models augmented with dense clocks.

2 Preliminaries

A nondeterministic multicounter automaton is a nondeterministic automaton with a finite number of states, a one-way input tape, and a finite number of integer counters. Each counter can be incremented by 1, decremented by 1, or stay unchanged. Besides, a counter can be tested against 0. It is well-known that counter machines with two counters have an undecidable halting problem, and obviously the undecidability holds for machines augmented with a pushdown stack. Thus, we have to restrict the behaviors of the counters. One such restriction is to limit the number of reversals a counter can make. A counter is \( n \)-reversal-bounded if it changes mode between nondecreasing and nonincreasing at most \( n \) times. For instance, the following sequence of counter values:

\[ 0, 0, 1, 1, 2, 2, 3, 3, 4, 4, 3, 3, 4, 4, 3, 3, 2, 2, 1, 1, 1, \ldots \]

demonstrates only one counter reversal. A counter is reversal-bounded if it is \( n \)-reversal-bounded for some fixed number \( n \) independent of computations. A reversal-bounded nondeterministic multicounter automaton (NCA) is a nondeterministic multicounter automaton in which each counter is reversal-bounded. A reversal-bounded nondeterministic pushdown multicounter automaton (NPCA) is an NCA augmented with a pushdown stack. In addition to counter operations, an NPCA can pop the top symbol from the stack or push a word onto the top of the stack. It is known that the emptiness problem (i.e., whether a machine accepts some words?) for NPCAs (and hence NCAs) is decidable.

**Lemma 1.** The emptiness problem for reversal-bounded nondeterministic pushdown multicounter automata is decidable. [28]

When an automaton does not have an input tape, we call it a machine. In this case, we are interested in the behaviors generated by the machine rather than the language accepted by the automaton. We shall use NPCM (resp. NCM) to stand for NCPA (resp. NCA) without an input tape.

Let \( \mathbb{N} \) be integers, \( \mathbb{D} = \mathbb{Q} \) (rationals) or \( \mathbb{R} \) (reals), \( \Gamma \) be an alphabet. We use \( \mathbb{N}^+ \) and \( \mathbb{D}^+ \) to denote non-negative values in \( \mathbb{N} \) and \( \mathbb{D} \), respectively. Each value \( v \in \mathbb{D}^+ \) can be uniquely expressed as the sum of \( \lceil v \rceil + \lfloor v \rfloor \), where \( \lceil v \rceil \in \mathbb{N} \) is the integral part of \( v \), and \( 0 \leq \lfloor v \rfloor < 1 \) is the fractional part of \( v \). A dense variable is a variable over
D. An integer variable is a variable over $\mathbb{N}$. A word variable is a variable over $\Gamma^*$. Let $m \geq 1$. For each $1 \leq i \leq m$, we use $x_i$, $y_i$, and $w_i$ to denote a dense variable, an integer variable, and a word variable, respectively. We use $\#_a(w_i)$ to denote a count variable representing the number of symbol $a \in \Gamma$ in $w_i$. A linear term $t$ is defined as follows:

$$t ::= n \mid x_i \mid y_i \mid \#_a(w_i) \mid t - t \mid t + t,$$

where $n \in \mathbb{N}$, $a \in \Gamma$ and $1 \leq i \leq m$. A mixed linear relation $l$ is defined as follows:

$$l ::= t > 0 \mid t = 0 \mid t_{\text{discrete}} \mod n = 0 \mid \neg l \mid l \land l,$$

where $t$ is a linear term, $0 \neq n \in \mathbb{N}$, and $t_{\text{discrete}}$ is a linear term not containing dense variables. Notice that a mixed linear relation could contain dense variables, integer variables, and word count variables. A dense linear relation is a mixed linear relation that contains dense variables only. A discrete linear relation is a mixed linear relation that does not contain dense variables. Obviously, any discrete linear relation is a Presburger formula over integer variables and word count variables.

Each integer can be represented as a unary string, e.g., string “00000” (resp. “11111”) for integer +5 (resp. −5). In this way, a tuple of integers and words can be encoded as a string by concatenating the unary representations of each integer and each of the words, with a separator # if $\notin \Gamma$. For instance, $(2, -4, w)$ is encoded as string “00#1111#w”.

Consider a predicate $H$ over integer variables and word variables. The domain of $H$ is the set of tuples of integers and words that satisfy $H$. Under the encoding, the domain of $H$ can be treated as a set of strings, i.e., a language. A predicate $H$ over integer variables and word variables is an NPCA predicate (or simply NPCA) if there is an NPCA accepting the domain of $H$. A $(D + \text{NPCA})$-formula $f$ is defined as follows:

$$f ::= l_{\text{dense}} \land H \mid l_{\text{dense}} \lor H \mid f \lor f,$$

where $l_{\text{dense}}$ is a dense linear relation and $H$ is an NPCA predicate. Therefore, a $(D + \text{NPCA})$ formula is a finite disjunction of formulas in the form of $l_{\text{dense}} \land H$ or $l_{\text{dense}} \lor H$, where dense variables (contained only in each $l_{\text{dense}}$) and discrete variables (contained only in each $H$) are separated. Let $p, q, r \geq 0$. A predicate $A$ on tuples in $\mathbb{D}^p \times \mathbb{N}^q \times (\Gamma^*)^r$ is $(D + \text{NPCA})$-definable if there is a $(D + \text{NPCA})$-formula $f$ with $p$ dense variables, $p + q$ integer variables, and $r$ word variables, such that, for all $x_1, \cdots, x_p$ in $\mathbb{D}$, for all $y_1, \cdots, y_q$ in $\mathbb{N}$, and for all $w_1, \cdots, w_r$ in $\Gamma^*$,

$$(x_1, \cdots, x_p, y_1, \cdots, y_q, w_1, \cdots, w_r) \in A$$

iff $f([x_1], \cdots, [x_p], [x_1], \cdots, [x_p], y_1, \cdots, y_q, w_1, \cdots, w_r)$ holds.

**Lemma 2.** (1). Both $l_{\text{discrete}} \land H$ and $l_{\text{discrete}} \lor H$ are NPCA predicates, if $l_{\text{discrete}}$ is a discrete linear relation and $H$ is an NPCA predicate.

(2). NPCA predicates are closed under existential quantifications (over integer variables and word variables).

(3). If $A$ is $(D + \text{NPCA})$-definable and $l$ is a mixed linear relation, then both $l \land A$ and $l \lor A$ are $(D + \text{NPCA})$-definable.

(4). The emptiness (or satisfiability) problem for $(D + \text{NPCA})$-definable predicates is decidable.
Proof. (1). \( l_{\text{discrete}} \) is a Presburger formula. (The domain of) \( l_{\text{discrete}} \) can therefore be accepted by a deterministic NCA [29]. Hence, \( l_{\text{discrete}} \land H \) and \( l_{\text{discrete}} \lor H \) can be accepted by NPCAs by “intersecting” and “joining” the deterministic NCA and the NPCA that accepts \( H \), respectively.

(2). Let \( H \) be an NPCA predicate containing variable \( z \) (either an integer variable or a word variable). Assume \( H \) is accepted by NPCA \( M \). An NPCA \( M' \) can be constructed to accept \( \exists z H \) by guessing each symbol in the encoding of \( z \) (on the input tape of \( M \)) and simulating \( M \).

(3). We first show that any mixed linear relation \( l \) is definable by a separately mixed linear relation \( l' \) (i.e., \( l' \) is a Boolean combination of dense linear relations and discrete linear relations. So, \( l' \) does not have a term containing both dense variables and discrete variables.). That is, for all \( x_1, \ldots, x_p, \in D, y_1, \ldots, y_q \in \mathbb{N} \),

\[
l(x_1, \ldots, x_p, y_1, \ldots, y_q) \text{ iff } l'(\lfloor x_1 \rfloor, \ldots, \lfloor x_p \rfloor, \lfloor x_1 \rfloor, \ldots, \lfloor x_p \rfloor, y_1, \ldots, y_q).
\]

Instead of giving a lengthy proof, we look at an example of \( l \): \( x_1 - x_2 + y_1 > 2 \). This can be rewritten as: \( \lfloor x_1 \rfloor - \lfloor x_2 \rfloor + y_1 - 2 + \lfloor x_1 \rfloor - \lfloor x_2 \rfloor > 0 \). Term \( \lfloor x_1 \rfloor - \lfloor x_2 \rfloor \) is the only part containing dense variables. Since \( \lfloor x_1 \rfloor - \lfloor x_2 \rfloor \) is bounded, separating cases for this term being at (and between) -1, 0, 1 will give a separately mixed linear relation \( l' \).

This separation idea can be applied for any mixed linear relation \( l \). If \( A \) is definable by a \( (D + \text{NPCA}) \)-formula \( f \), then \( l \land A \) (resp. \( l \lor A \)) is definable by \( l' \land A \) (resp. \( l' \lor A \)). By re-organizing the dense linear relations (in \( l' \) and \( f \)) and the discrete linear relations (in \( l' \)) such that the discrete linear relations are grouped with the NPCA predicates in \( f \). \( l' \land A \) and \( l' \lor f \) can be made \( (D + \text{NPCA}) \)-formulas using Lemma 2 (1).

(4). The emptiness problem for \( l_{\text{discrete}} \land H \) and \( l_{\text{discrete}} \lor H \) is decidable, noticing that the emptiness for \( l_{\text{discrete}} \), which is expressible in the additive theory of reals (or rationals), is decidable, and the emptiness of NPCA predicate \( H \) is decidable (Lemma 2 (3)). Therefore, the emptiness of any \( (D + \text{NPCA}) \) formulas, as well as, from Lemma 2 (3), any \( (D + \text{NPCA}) \)-definable predicates, is decidable.

3 Clock Patterns and Their Changes

A dense clock is simply a dense variable taking non-negative values in \( D^+ \). Now we fix a \( k > 0 \) and consider \( k + 1 \) clocks \( x = x_0, \ldots, x_k \). For technical reasons, \( x_0 \) is an auxiliary clock indicating the current time \textit{now}. Let \( K = \{0, \ldots, k\} \), and \( K^+ = \{1, \ldots, k\} \). A subset \( K' \) of \( K \) is abused as a set of clocks; i.e., we say \( x_i \in K' \) if \( i \in K' \). A (clock) valuation \( v \) is a function \( K \to D^+ \) that assigns a value in \( D^+ \) to each clock in \( K \). A discrete (clock) valuation \( u \) is a function \( K \to \mathbb{N}^+ \) that assigns a value in \( \mathbb{N}^+ \) to each clock in \( K \). For each valuation \( v \) and \( \delta \in D^+, \lfloor v \rfloor, \lfloor v \rfloor \) and \( v + \delta \) are valuations satisfying \( \lfloor v \rfloor(i) = \lfloor v(i) \rfloor \), \( \lfloor v \rfloor(i) = \lfloor v(i) \rfloor \) and \( (v + \delta)(i) = v(i) + \delta \) for each \( i \in K \). The relative representation \( \hat{v} \) of a valuation \( v \) is a valuation satisfying:

- \( \hat{v} = [v] \).
- \( \hat{v}(0) = 1 - \lfloor v(0) \rfloor \).
- \( \hat{v}(i) = \lfloor v(i) + \hat{v}(0) \rfloor \), for each \( i \in K^+ \).

A valuation \( v_0 \) is initial if the auxiliary clock \( x_0 \) has value 0 in \( v_0 \).
Example 1. Let \( k = 4 \) and \( v_1 = (4.296, 1.732, 1.414, 5.289, 3.732) \). It can be calculated that \( \tilde{v}_1 = (4.704, 1.436, 1.118, 5.993, 3.436) \). Let \( v_2 = v_1 + .268 = (4.564, 2, 1.682, 5.557, 4) \). Then, \( \tilde{v}_2 = (4.436, 2.436, 1.118, 5.993, 4.436) \). It is noticed that all the fractional parts (except for \( \tilde{v}_1(0) \) and \( \tilde{v}_2(0) \)) are the same in \( \tilde{v}_1 \) and \( \tilde{v}_2 \). It is easy to show that a clock progress (i.e., \( x_0, \cdots, x_k \) progress by the same amount such as .268) will not change the fractional parts of clock values (for clocks \( x_1, \cdots, x_k \)) in a relative representation. ■

3.1 Clock Patterns

We distinguish two disjoint sets, \( K^0 = \{0^0, \cdots, k^0\} \) and \( K^1 = \{0^1, \cdots, k^1\} \), of indices. A pattern \( \eta \) is a sequence

\[ p_0, \cdots, p_n, \]

for some \( 0 \leq n < 2(k + 1) \), of nonempty and disjoint subsets of \( K^0 \cup K^1 \) such that

- \( 0^0 \in p_0 \) and
- \( \cup_{0 \leq i \leq n} p_i = K^0 \cup K^1 \).

In pattern \( \eta \), \( p_i \) is called the \( i \)-position. A pair of valuations \( (v_0, v_1) \) is initialized if \( v_0 \) is initial. The pattern of \( (v_0, v_1) \) characterizes the fractional ordering between elements in \( \tilde{v}_0 \) and \( \tilde{v}_1 \) (where \( K^0 \) is for indices of \( v_0 \) and \( K^1 \) is for indices of \( v_1 \)).

Formally, an initialized pair \( (v_0, v_1) \) has pattern \( \eta = p_0, \cdots, p_n \), written \( (v_0, v_1) \in \eta \), or \( [(v_0, v_1)] = \eta \), if, for each \( 0 \leq m, m' \leq n \), each \( b, b' \in \{0, 1\} \), and each \( i, i' \in K \), \( i^b \in p_m \) and \( i'^{b'} \in p_{m'} \) imply that

\[ \tilde{v}_b(i) = \tilde{v}_{b'}(i') \quad \text{(resp. <)} \quad \text{iff} \quad m = m' \quad \text{(resp.} \ m < m' \).\]

Though this definition of a pattern is quite complex, a pattern can be easily visualized after looking at the following example.

Example 2. Consider \( v_1 \) in Example 1 and an initial valuation \( v_0 = (0, 3.118, 5.118, 2, 1.876) \). Since \( v_0 \) is initial, \( \tilde{v}_0 = v_0 \). The fractional parts of \( v_0 \) and \( v_1 \), in the relative representation, can be put on a big circle representing the interval \([0, 1)\) as shown in Figure 1. Each fractional value \( \tilde{v}_0(i) \) for \( v_0 \) is represented by an oval; each fractional value \( \tilde{v}_1(i) \) for \( v_1 \) is represented by a box. The pattern of \( (v_0, v_1) \) can be drawn by collecting clockwise (from the top, i.e., \( \tilde{v}_0(0) = 0 \)) the indices (superscripted with 0, e.g., \( 3^0 \) for \( \tilde{v}_0(3) \)) for each component in \( \tilde{v}_0 \) and the indices (superscripted with 1, e.g., \( 3^1 \) for \( \tilde{v}_1(3) \)) for each component in \( \tilde{v}_1 \); i.e., the pattern is

\[ \eta = p_0, \cdots, p_5 \]

with \( p_0 = \{0^0, 3^0\}, p_1 = \{1^0, 2^0, 2^1\}, p_2 = \{1^1, 4^1\}, p_3 = \{0^1\}, p_4 = \{4^0\}, p_5 = \{3^1\} \).

There are at most \( 2^k(k+1)^2 \) distinct patterns. Let \( \Phi \) denote the set of all the patterns (for the fixed \( k \)). A pattern is initial if it is the pattern of \( (v_0, v_0) \) for some initial valuation \( v_0 \). If \( \eta \) is the pattern of \( (v_0, v_1) \), we use \( \text{init}(\eta) \) to denote the pattern of
the following statements hold:

(1) the pattern of \((v_0^1, v_1)\) is initial iff \([v_1] = [v_0^1]\),

(2) \(v_1\) is initial (i.e., \(v_1(0) = 0\)) iff \(v_2\) is initial,

(3) \(v_1 = v_0^1\) iff \(v_2 = v_0^2\).

A valuation \(v_1\) has pattern \(\eta\) if there is an initial \(v_0\) such that \((v_0, v_1)\) has pattern \(\eta\). \(v_1\) may have a number of patterns, by different choices of \(v_0\). A pattern of \(v_1\) tells the truth values of all the fractional orderings \([v_1](i) \# [v_1](j)\) and \([v_1](i) \neq 0\) (where \# stands for \(<, >, \leq, \geq, =\)) for all \(i, j \in K^+\), as shown in the following lemma.

**Lemma 3.** For any two initialized pairs \((v_0^1, v_1)\) and \((v_0^2, v_2)\) with \((v_0^1, v_1) \approx (v_0^2, v_2)\), the following statements hold:

1. the pattern of \((v_0^1, v_1)\) is initial iff \([v_1] = [v_0^1]\),
2. \(v_1\) is initial (i.e., \(v_1(0) = 0\)) iff \(v_2\) is initial,
3. \(v_1 = v_0^1\) iff \(v_2 = v_0^2\).

**Lemma 4.** Let \(\eta = p_0, \cdots, p_n\) be a pattern of a valuation \(v\). Assume \(0^1 \in p_i\) for some \(0 \leq i \leq n\). Then, for any \(m_1\) and \(m_2\) (with \(0 \leq m_1, m_2 \leq n\)), for any \(j_1\) and \(j_2\) in \(K^+\) (with \(j_1^1 \leq p_{m_1}\) and \(j_2^1 \leq p_{m_2}\)), the following statements hold.

1. \([v](j_1) > [v](j_2)\) iff one of the following conditions holds:
   \[m_1 < i \leq m_2,\]
   \[m_2 < m_1 < i,\]
   \[i \leq m_2 < m_1.\]
2. \([v](j_1) = [v](j_2)\) iff \(m_1 = m_2\).
3. \([v](j_1) > 0\) iff \(m_1 \neq i\).
\begin{equation}
|v| (j_1) = 0 \text{ iff } m_1 = i.
\end{equation}

**Proof.** Directly from the definition of a pattern. \hfill \Box

Recall $0^1 \in K^1$ stands for the index for the value of clock $x_0$ (representing now) in $v_1$. Let $\eta = p_0, \ldots, p_n$ be a pattern. $p_i$ is the now-position of $\eta$ if $0^1 \in p_i$. A pattern $\eta$ is regulated if the now-position of $\eta$ is $p_0$. Note that the pattern of an initialized pair $(v_0, v_1)$ is regulated if and only if the auxiliary clock $x_0$ takes an integral value in $v_1$ (i.e., $|v_1|(0) = 0$). A pattern is a merge-pattern if the now-position is a singleton set (i.e., $0^1$ is the only element). A pattern is a split-pattern if it is not a merge-pattern, i.e., the now-position contains more than one element. (“Merge” and “split” will be made clear in a moment.) Obviously, a regulated pattern is always a split-pattern. This is because the now-position of a regulated pattern, which is $p_0$, contains at least two elements $0^0$ and $0^1$.

### 3.2 Clock Progresses

For each $0 < \delta \in D^+$, $v + \delta$ is the result of a clock progress from $v$ by an amount of $\delta$. How does a pattern change according to the progress? Let us first look at an example.

**Example 3.** Consider $v_1, v_2 (= v_1 + 0.268)$ in Example 1 and $v_0$ in Example 2. In Example 1 we indicated that the pattern $\eta_1$ of $(v_0, v_1)$ is
\[
\{0^0, 3^0\}, \{1^0, 2^0, 2^1\}, \{1^1, 4^1\}, \{0^1\}, \{4^0\}, \{3^1\}.
\]
Similar steps can be followed to show that the pattern $\eta_2$ of $(v_0, v_2)$ is
\[
\{0^0, 3^0\}, \{1^0, 2^0, 2^1\}, \{1^1, 4^1, 0^1\}, \{4^0\}, \{3^1\}.
\]

A helpful way to see the relationship between $\eta_1$ and $\eta_2$ is by looking at Figure 1. Holding the box labeled by $\tilde{v}_1(0)$ (for the current time) and sliding counter-clockwisely along the big circle for an amount of $0.268$ will stop at the box labeled by $\tilde{v}_1(1)$ and $\tilde{v}_1(4)$. Thus, the pattern $\eta_2$ (after sliding) is exactly $\eta_1$ (before sliding) except that $0^1$ in the 3-position in $\eta_1$ is merged into the 2-position in $\eta_2$. Notice that $\eta_1$ is a merge-pattern and the resulting $\eta_2$ is a split-pattern. The integral parts $|v_1|(1)$ and $|v_1|(4)$ change to $|v_2|(1) = |v_1|(1) + 1$ and $|v_2|(4) = |v_1|(4) + 1$. But all the other components of $|v_1|$ do not change. The reason is that, after merging $0^1$ with $1^1$ and $3^1$ in $\eta_2$, the fractional parts $|v_2|(1)$ and $|v_2|(4)$ are “rounded” (i.e., become 0). What if we further make a clock progress from $v_2$ for an amount of $\delta' = .12$? The resulting pattern $\eta_3$ of $(v_0, v_3)$ with $v_3 = v_2 + \delta'$ is the result of splitting $0^1$ from the 2-position $\{1^1, 4^1, 0^1\}$. That is, $\eta_3$ is
\[
\{0^0, 3^0\}, \{1^0, 2^0, 2^1\}, \{0^1\}, \{1^1, 4^1\}, \{4^0\}, \{3^1\},
\]
which is a merge-pattern again. This process of merging and splitting can be formally defined as the following function $\text{next}$.

Function $\text{next} : \Phi \times (N^+)^{k+1} \to \Phi \times (N^+)^{k+1}$ describes how a pattern changes upon a clock progress. Given any discrete valuation $u$ and pattern $\eta = p_0, \ldots, p_n$ with the now-position being $p_i$ for some $i$, $\text{next}(\eta, u)$ is defined to be $(\eta', u')$ such that,
Lemma 5. For any initialized pair \((v_0, v)\) and any \(0 < \delta \in D^+\), the following statements are equivalent:

1. \(\text{next}([v_0, v], [v]) = ([v_0, v + \delta], [v + \delta])\),
2. \(v\) has one pattern change for \(\delta\).

- (the case when \(\eta\) is a merge-pattern) if \(i > 0\) and \(|p_i| = 1\) (that is, the now-position \(p_i = \{0^1\}\)), then \(\eta'\) is

\[
p_0, \ldots, p_{i-1} \cup \{0^1\}, p_{i+1}, \ldots, p_n
\]

(that is, \(\eta'\) is the result of merging the now-position to the previous position), and for each \(j \in K^+\), if \(j^1 \in p_{i-1}\), then \(u'(j) = u(j) + 1\) else \(u'(j) = u(j)\). Besides, if \(i = 1\) (i.e., the now-position is merged to \(p_0\); in this case, \(\eta'\) is a regulated pattern), then \(u'(0) = u(0) + 1\) else \(u'(0) = u(0)\),

- (the case when \(\eta\) is a split pattern) if \(i \geq 0\) and \(|p_i| > 1\), then \(\eta'\) is the result of splitting \(0^1\) from the now-position. That is, if \(i > 0\), \(\eta'\) is

\[
p_0, \ldots, p_{i-1}, \{0^1\}, p_i - \{0^1\}, p_{i+1}, \ldots, p_n.
\]

However, if \(i = 0\), \(\eta'\) is

\[
p_0 - \{0^1\}, p_1, \ldots, p_n, \{0^1\}.
\]

In either case, \(u' = u\).

If \(\text{next}(\eta, u) = (\eta', u')\), (1). \(\eta'\) is called the next pattern of \(\eta\), written \(\text{Next}(\eta)\), (2). \(\Delta_\eta \in \{0,1\}^{k+1}\) is called the increment vector of \(\eta\) with \(\Delta_\eta = u' - u\). Obviously, \(\text{Next}(\eta) \neq \eta\) and \(\text{Next}(\cdot)\) is total and 1-1.

To better understand \(\text{Next}(\cdot)\), we visualize pattern \(\eta\) as a circle shown in Figure 3. Applications of \(\text{Next}(\cdot)\) can be regarded as moving the index \(0^1\) along the circle, by performing merge-operations (Figure 3(a)) and split-operations (Figure 3(b)) alternatively. After enough number of applications of \(\text{Next}(\cdot)\), \(0^1\) will return to the original now-position after moving through the entire circle. That is, for each pattern \(\eta\), there is a smallest positive integer \(m\) such that \(\text{Next}^m(\eta) = \eta\); i.e., \(\eta_0, \ldots, \eta_m\) satisfies \(\eta_0 = \eta_m = \eta\), and \(\text{Next}(\eta_i) = \eta_{i+1}\) for each \(0 \leq i < m\). More precisely, by looking at Figure 3 if \(\eta\) is a merge-pattern, \(m = 2n\); if \(\eta\) is a split-pattern, \(m = 2(n + 1)\). Furthermore, elements \(\eta_0, \ldots, \eta_m\) are distinct. The sequence \(\eta_0, \ldots, \eta_m\) is called a pattern ring. The pattern ring is unique for each fixed \(\eta_0\). Notice that \(\text{Next}^m(\eta, u) = (\eta, u + 1)\) for each \(u\). Since the next pattern \(\text{Next}(\eta)\) is a merge-pattern (resp. split-pattern) if \(\eta\) is a split-pattern (resp. merge-pattern), on a pattern ring, merge-patterns and split-patterns appear alternately.

Fix any initialized pair \((v_0, v)\) and \(0 < \delta \in D^+\). Assume the patterns of \((v_0, v)\) and \((v_0, v + \delta)\) are \(\eta\) and \(\eta'\), respectively. We say \(v\) has no pattern change for \(\delta\) if, for all \(0 \leq \delta' \leq \delta\), \((v_0, v + \delta')\) has the same pattern. We say \(v\) has one pattern change for \(\delta\) if \(\text{Next}(\eta) = \eta'\) and, for all \(0 < \delta' < \delta\), \((v_0, v + \delta')\) has pattern \(\eta\), or, for all \(0 < \delta' < \delta\), \((v_0, v + \delta')\) has pattern \(\eta'\). The following lemma on the correctness of \(\text{next}\) can be observed.

Lemma 5. For any initialized pair \((v_0, v)\) and any \(0 < \delta \in D^+\), the following statements are equivalent:

1. \(\text{next}([v_0, v], [v]) = ([v_0, v + \delta], [v + \delta])\),
2. \(v\) has one pattern change for \(\delta\).
We say \( v \) has \( n \) pattern changes for \( \delta \) with \( n \geq 1 \), if there are positive \( \delta_1, \ldots, \delta_n \) in \( D^+ \) with \( \sum_{1 \leq i \leq n} \delta_i = \delta \) such that \( v + \sum_{1 \leq i \leq j} \delta_i \) has one pattern change for \( \delta_{j+1} \), for each \( j = 0, \ldots, n-1 \). It is noticed that for any \( \delta \leq 1 \), \( v \) has at most \( m \) pattern changes, where \( m \) is the length of the pattern ring starting from the pattern \( \eta \) of \( (v_0, v) \). This \( m \) is uniformly bounded by \( 4(k + 1) \).

Lemma 6. For any initialized pair \( (v_0, v) \) and any \( \delta \in D^+ \), (1) \( v \) has at most \( 4(k + 1) \) pattern changes for \( \delta \) if \( \delta \leq 1 \), (2) \( v \) has at least one pattern change for \( \delta \) if \( \delta \geq 1 \), (3) if \( v \) has no pattern change for \( \delta \) then \( \lceil v \rceil = \lceil v + \delta \rceil \).

3.3 Clock Resets

In addition to clock progresses, clock resets are the other form of clock behaviors. Let \( r \subseteq K^+ \) be (a set of) clock resets. \( v \downarrow_r \) denotes the result of resetting each clock \( x_i \in r \) (i.e., \( i \in r \)). That is, for each \( i \in K \),

\[
(v \downarrow_r)(i) = \begin{cases} 
0 & \text{if } i \in r \\
 v(i) & \text{otherwise.}
\end{cases}
\]

Example 4. Consider \( v_0 \) and \( v_1 \) given in Example \( \Box \) and Example \( \Box \). Assume \( r = \{4\} \). By definition, \( v_1 \downarrow_r = (4.296, 1.732, 1.414, 5.289, 0) \). It can be calculated that the relative representation of \( v_1 \downarrow_r \) is \( (4.704, 1.436, 1.118, 5.993, 0.704) \). The pattern of \( (v_0, v_1 \downarrow_r) \) can be figured out again by looking at Figure \( \Box \). The reset of clock \( x_4 \) can

Fig. 2. A graphical representation of a pattern \( \eta = p_0, \ldots, p_n \). Operator \( \text{Next}(\cdot) \) has the same effect as moving the now-position counter-clockwisely. In case (a), the now-position is merged to the previous position. In case (b), index \( 0^1 \) is split from the now-position.
be conceptually regarded as moving the label \( v_1(4) \) from the box of \( v_1(1) \) and \( v_1(4) \) to
the box of \( v_1(0) \) (the current time). Therefore, the pattern after the reset changes from
\[
\{0^0, 3^0\}, \{1^0, 2^0, 2^1\}, \{1^1, 4^1\}, \{0^1\}, \{4^0\}, \{3^1\}
\]
of \((v_0, v_1)\) to
\[
\{0^0, 3^0\}, \{1^0, 2^0, 2^1\}, \{1^1\}, \{0^1, 4^1\}, \{4^0\}, \{3^1\}
\]
of \((v_0, v_1 \downarrow_r)\) by moving 4\(^1\) into the position containing 0\(^1\).

Functions \( \text{reset}_r : \Phi \times (\mathbb{N}^+)^{k+1} \rightarrow \Phi \times (\mathbb{N}^+)^{k+1} \) for \( r \subseteq K^+ \) describe how
a pattern changes after clock resets. Given any discrete valuation \( v \) and any pattern
\( \eta = p_0, \ldots, p_n \) with the now-position being \( p_i \) for some \( i \), \( \text{reset}_r(\eta, v) \) is defined to be
\( (\eta', u') \) such that,
\begin{itemize}
  \item \( \eta' \) is \( p_0 - r^1, \ldots, p_{i-1} - r^1, p_i \cup r^1, p_{i+1} - r^1, \ldots, p_n - r^1 \), where \( r^1 = \{ j^1 : j \in r \} \subseteq K^1 \). Therefore, \( \eta' \) is the result of bringing every index in \( r^1 \) into the
now-position. Notice that some of \( p_m - r^1 \) may be empty after moving indices in
\( r^1 \) out of \( p_m \), for \( m \neq i \). In this case, these empty elements are removed from \( \eta' \)
(to guarantee that \( \eta' \) is well defined.),
  \item for each \( j \in K \), if \( j \in r \), then \( u'(j) = 0 \) else \( u'(j) = u(j) \).
\end{itemize}
If \( \text{reset}_r(\eta, v) = (\eta', u') \), \( \eta' \) is written as \( \text{Reset}_r(\eta) \). Note that \( \text{Reset}_r(\eta) \) is unique
for each \( \eta \) and \( r \), and is independent of \( v \). The following lemma states that \( \text{reset} \) is
correct.

**Lemma 7.** For any initialized pair \((v_0, v)\) and any \( r \subseteq K^+ \),
\[
\text{reset}_r([[(v_0, v)]], [v]) = ([(v_0, v \downarrow_r)], [v \downarrow_r]).
\]

### 4 Clock Constraints and Patterns

An atomic clock constraint (over clocks \( x_1, \ldots, x_k \), excluding \( x_0 \)) is a formula in the
form of \( x_i - x_j \# d \) or \( x_i \# d \) where \( 0 \leq d \in \mathbb{N}^+ \) and \( \# \) stands for \(<, >, \leq, \geq, =\). A
clock constraint \( c \) is a Boolean combination of atomic clock constraints. Let \( \mathcal{C} \) be the
set of all clock constraint (over clocks \( x_1, \ldots, x_k \)). We say \( v \in c \) if clock valuation \( v \)
(for \( x_0, \ldots, x_k \)) satisfies clock constraint \( c \).

Any clock constraint \( c \) can be written as a Boolean combination \( I(c) \) of clock constraints
over discrete clocks \([x_1], \ldots, [x_k]\) and fractional orderings \([x_i] \# [x_j]\) and
\([x_i] \# 0\). For instance, \( x_i - x_j \leq d \) is equivalent to: \([x_i] - [x_j] \leq d\), or, \([x_i] - [x_j] = d \) and
\([x_i] < [x_j]\). \( x_i > d \) is equivalent to: \([x_i] > d\), or, \([x_i] = d \) and \([x_i] > 0\). Therefore,
testing \( v \in c \) is equivalent to testing \([v]\) and the fractional orderings on \([v]\)
satisfying \( I(c) \).

Assume \( v \) has a pattern \( \eta = p_0, \ldots, p_n \). A fractional ordering on \([v]\) is equivalent to
a Boolean condition on \( \eta \), as shown in Lemma 4. Whenever \( \eta \) is fixed, each fractional
ordering in \( I(c) \) has a specific truth value (either 0 or 1). In this case, we use \( I(c)^n \), or
simply \( c^n \), to denote the result of replacing fractional orderings in \( I(c) \) by the truth
values given by \( \eta \). \( c^n \), without containing fractional orderings, is just a clock constraint
(over discrete clocks). Notice that the pattern space $\Phi$ is finite, therefore, $v \in c$ is equivalent to

$$\bigvee_{\eta \in \Phi} (v \text{ has pattern } \eta \land \lfloor v \rfloor \in c^\eta).$$

Hence, the truth value of $v \in c$ only depends on a pattern of $v$ and the integral parts of $v$. These observations conclude the following results. In particular, Lemma 8 (2) indicates that it is sufficient to test the two end points $v \in c$ and $v + \delta \in c$ in order to make sure that $c$ is consistently satisfied on each $v + \delta'$, $0 \leq \delta' \leq \delta$, if from $v$ to $v + \delta$, there is at most one pattern change.

**Lemma 8.** (1) For any initialized pair $(v_0, v)$, any pattern $\eta \in \Phi$, if $(v_0, v)$ has pattern $\eta$, then, for any clock constraint $c \in C$, $v \in c$ iff $\lfloor v \rfloor \in c^\eta$.

(2) For any initialized pair $(v_0, v)$ and any $0 < \delta \in \mathbb{D}^+$, if $v$ has at most one pattern change for $\delta$, then, for any clock constraint $c \in C$,

$$\forall 0 \leq \delta' \leq \delta(v + \delta' \in c) \text{ iff } v \in c \text{ and } v + \delta \in c.$$

(3) For any initialized pairs $(v_0^1, v_1)$ and $(v_0^2, v_2)$. If $(v_0^1, v_1) \approx (v_0^2, v_2)$, then, for any $c \in C$, $v_1 \in c$ iff $v_2 \in c$.

**Proof.** (1) is from the observations made before this lemma in this section. (2) is from (1) and Lemma 8 (3) is directly from (1).

Now, we consider two initialized pairs $(v_0^1, v_1)$ and $(v_0^2, v_2)$ such that

$$(v_0^1, v_1) \approx (v_0^2, v_2).$$

That is, from the definition of $\approx$, $v_0^1$ (resp. $v_1$) has the same integral parts as $v_0^2$ (resp. $v_2$). Besides, the two pairs have the same pattern. From Lemma 8 (3), any test $c \in C$ will not tell the difference between $v_1$ and $v_2$. Assume $v_1$ can be reached from a valuation $v^1$ via a clock progress by an amount of $\delta_1$, i.e., $v^1 + \delta_1 = v_1$. We would like to know whether $v_2$ can be reached from some valuation $v^2$ also via a clock progress but probably by a slightly different amount of $\delta_2$ such that $(v_0^1, v^1)$ and $(v_0^2, v^2)$ are still equivalent($\approx$). We also expect that for any test $c$, if during the progress of $v^1$, $c$ is consistently satisfied, then so is $c$ for the progress of $v^2$. The following lemma concludes that these, as well as the parallel case for clock resets, can be done. This result can be used later to show that if $v_1$ is reached from $v_0^1$ by a sequence of transitions that repeatedly perform clock progresses and clock resets, then $v_2$ can be also reached from $v_0^2$ via a very similar sequence such that no test $c$ can distinguish the two sequences.

**Lemma 9.** For any initialized pairs $(v_0^1, v_1)$ and $(v_0^2, v_2)$ with $(v_0^1, v_1) \approx (v_0^2, v_2)$,

(1). for any $0 \leq \delta_1 \in \mathbb{D}^+$, for any clock valuation $v^1$, if $v^1 + \delta_1 = v_1$, then there exist $0 \leq \delta_2 \in \mathbb{D}^+$ and clock valuation $v^2$ such that

(1.1). $v^2 + \delta_2 = v_2$ and $(v_0^1, v^1) \approx (v_0^2, v^2)$,

(1.2). $v^1$ is initial iff $v^2$ is initial,

$v^1 = v_0^1$ iff $v^2 = v_0^2$, and

for any $c \in C$, $v^1 \in c$ (resp. $v_1 \in c$) iff $v^2 \in c$ (resp. $v_2 \in c$).
(1.3). For any clock constraint $c \in C$, $\forall 0 \leq \delta' \leq \delta_1(v^1 + \delta \in c)$ iff $\forall 0 \leq \delta' \leq \delta_2(v^2 + \delta \in c)$.

(2). For any $r \subseteq K^+$, for any clock valuation $v^1$, if $v^1 \downarrow_r = v_1$, then there exists a valuation $v^2$ such that

(2.1). $v^2 \downarrow_r = v_2$ and $(v_1^0, v_1^1) \approx (v_0^2, v^2)$.

(2.2). Same as (1.2).

Proof. (1). Assume $\delta_1$ is “small”, i.e., from $v^1$ to $v_1 = v^1 + \delta_1$, there is at most one pattern change. Let $\eta = p_0, \cdots, p_n$ be the pattern for $(v_0^2, v_2)$ (and, hence, for $(v_0^1, v_1)$). Assume $0^1 \in p_i$ for some $i$. If $\delta_1$ causes no pattern change for $v^1$, then simply take $\delta_2 = 0$. If $\delta_1$ causes one pattern change for $v^1$, then we put $(v_0^1, v_2)$ on a circle (e.g. Figure 1). If $\eta$ is a split-pattern (i.e., $|p_i| > 1$), then we separate a new box (only labeled by $[v_2^1(0)]$ from the original box labeled by $[v_2^1(0)]$ and slide the new box backwards (i.e., clockwise) for a small positive amount (taken as $\delta_2$) without hitting any box or oval. If $\eta$ is a merge-pattern (i.e., $|p_i| = 1$), then we slide the box labeled by $[v_2^1(0)]$ (this is the only label) backwards (i.e., clockwise) for a positive amount (taken as $\delta_2$) until a box or an oval is hit. Take $v^2 = v_2 - \delta_2$. Obviously, $(v_1^0, v_1^1) \approx (v_0^2, v^2)$. It can be checked that (1.2) and (1.3) hold using Lemma 3 and Lemma 4.

Any larger $\delta_1$ that causes multiple pattern changes for $v^1$ can be split into a finite (Lemma 3) sequence of small $\delta$’s that causes exactly one pattern change. In this case, $\delta_2$ can be calculated by working on each small $\delta$ (the last one first) as in the above proof.

(2). The case when $r = \emptyset$ is obvious. Assume $r$ contains only one element $j \in K^+$. Assume $\eta$ is the pattern of $(v_0^1, v_1^1)$. A desired $v^2$ is picked as follows. The integral parts of $v^2$ are exactly those of $v^1$; i.e., $[v^2] = [v^1]$. The fractional parts of $v^2$ are exactly those of $v_2$, except that, in the relative representation, $[v^2](j)$ may be different from $[v_2^1](j)$. Then what is $[v^2](j)$? It is chosen such that the pattern of $(v_0^2, v^2)$ is $\eta$. For instance, if $[v^1](j)$ equals to, say, $[v_1^1](j_1)$ (resp. $[v_0^1](j_1)$), for some $j_1$, then $[v^2](j)$ is picked as $[v_2^1](j_1)$ (resp. $[v_0^1](j_1)$). If $[v^1](j)$ lies strictly between, say, $[v_1^1](j_1)$ (or, $[v_0^1](j_1)$) and $[v_2^1](j_2)$ (or, $[v_0^1](j_2)$), for some $j_1$ and $j_2$, such that no other component in $[v^1]$ and $[v_0^1]$ lies strictly between these two values, then $[v^2](j)$ is picked as any value lies strictly between $[v_2^1](j_1)$ (or, $[v_0^1](j_1)$) and $[v_2^1](j_2)$ (or, $[v_0^1](j_2)$) accordingly. Since $(v_0^1, v_1^1) \approx (v_0^2, v^2)$, we can show $[v^2](j)$ can always be picked. The choice of $[v^2](j)$ guarantees that the pattern of $(v_0^1, v_1^1)$ is the same as the pattern of $(v_0^2, v^2)$. The rest of conditions in (2) can be checked easily.

For the case when $r$ contains more than one element, the above proof can be generalized by resetting clocks in $r$ one by one.

5 Pushdown Timed Automata

A pushdown timed automaton (PTA) $A$ is a tuple

$$(S, \{x_1, \cdots, x_k\}, I_{ov}, R, \Gamma, PD),$$

where
for any fixed two states
We write
word
state
A
A reader might wonder why we don’t have a stack operation for a progress transition. That is,

– (a progress transition) \( s_1 = s_2, w_1 = w_2, \) and \( \exists \delta < \delta' \in \mathbb{D}^+ \), \( v_2 = v_1 + \delta \) and for all \( \delta' \) satisfying \( 0 \leq \delta' \leq \delta, v_1 + \delta' \in \text{Inv}(s_1) \). That is, a progress transition makes all the clocks synchronously progress by amount \( \delta > 0 \), during which the invariant is consistently satisfied, while the state and the stack content remain unchanged.

– (a reset transition) \( v_1 \in \text{Inv}(s_1) \) and \( c, v_1 \downarrow_r \Rightarrow v_2 \in \text{Inv}(s_2) \), and \( w_1 = aw, w_2 = \gamma w \) for some \( w \in \Gamma^* \), where \( R(s_1, s_2) = (c, r) \) for some clock constraint \( c \) and clock resets \( r \), and \( PD(s_1, s_2) = (a, \gamma) \) for some stack symbol \( a \in \Gamma \) and string \( \gamma \in \Gamma^* \). That is, a reset transition, by moving from state \( s_1 \) to state \( s_2 \), resets every clock in \( r \) to 0 and keeps all the other clocks unchanged. The stack content is modified according to the stack operation \( (a, \gamma) \) given on edge \( (s_1, s_2) \). Clock values before the transition satisfy the invariant \( \text{Inv}(s_1) \) and the reset condition \( c \); clock values after the transition satisfy the invariant \( \text{Inv}(s_2) \). \( \square \)

We write \( \rightarrow^*_A \) to be the transitive closure of \( \rightarrow_A \). Given two valuations \( v^1_0 \) and \( v_1 \), two states \( s_0 \) and \( s_1 \), and two stack words \( w_0 \) and \( w_1 \), assume the auxiliary clock \( x_0 \) starts from 0, i.e., \( v^1_0 \) is initial. The following result is surprising. It states that, for any initialized pair \( (v^2_0, v_2) \) with \( (v^1_0, v_1) \approx (v^2_0, v_2) \), \( (s_0, v^1_0, w_0) \rightarrow_A (s_1, v_1, w_1) \) if and only if \( (s_0, v^2_0, w_0) \rightarrow^*_A (s_1, v_2, w_1) \). This result implies that, from the definition of \( \approx \), for any fixed \( s_0, s_1, w_0 \) and \( w_1 \), the pattern of \( ([v^1_0], [v_1]) \) (instead of the actual values

\[ 1 \] A reader might wonder why we don’t have a stack operation for a progress transition. That is, a state \( s \) can also be assigned with a stack operation \( (a, \gamma) \) such that each progress transition by an amount \( \delta > 0 \) on state \( s \) also modifies the stack content according to \( (a, \gamma) \). However, this progress transition can be treated as a sequence of three transitions: a progress transition (without a stack operation) by \( \delta_1 > 0 \), a clock reset transition (by adding a dummy clock) performing stack operation \( (a, \gamma) \), followed by a progress transition (without a stack operation) by \( \delta_2 > 0 \), whenever \( \delta = \delta_1 + \delta_2 \). A translation can be worked out by expressing any PTA with a stack operation for each progress transition by a PTA defined in this paper. Since we focus on the clock/stack behaviors of a PTA, instead of the \( \omega \)-language accepted by it, input symbols are not considered in our definition. (The input to a timed automaton is always one-way. Thus, input symbols can always be built into states.)
of $|v_0^1|$ and $|v_1^1|$, the integral values $\lfloor v_0^1 \rfloor$, and the integral values $\lfloor v_1 \rfloor$ are sufficient to determine whether $(s_0, v_0^1, w_0)$ can reach $(s_1, v_1, w_1)$ in $A$.

**Lemma 10.** Let $A$ be a PTA. For any states $s_0$ and $s_1$, any two initial clock valuations $v_0^1$ and $v_0^2$, any two clock valuations $v_1$ and $v_2$, and any two stack words $w_0$ and $w_1$, if $(v_0^1, v_1) \approx (v_0^2, v_2)$, then,

$$(s_0, v_0^1, w_0) \xrightarrow{\star_A} (s_1, v_1, w_1) \iff (s_0, v_0^2, w_0) \xrightarrow{\star_A} (s_1, v_2, w_1).$$

**Proof.** Lemma 8 and Lemma 9 already give the result, but for $\rightarrow_A$ instead of $\rightarrow_{\star_A}$, noticing that Lemma 8 guarantees that tests (and obviously stack operations) are consistent in $(s_0, v_0^1, w_0) \rightarrow_A (s_1, v_1, w_1)$ and in $(s_0, v_0^2, w_0) \rightarrow_A (s_1, v_2, w_1)$. An induction (on the length of $\rightarrow_{\star_A}$) can be used to show the lemma, by working from $(s_1, v_1, w_1)$ back to $(s_0, v_0^1, w_0)$.  

**Example 5.** It is the time to show an example to convince the reader that Lemma 10 indeed works. Consider a timed automaton $A$ shown in Figure 3. Let $v_0^1 = (0, 4.98, 2.52)$, $v_0^2 = (0, 5.36, 2.89, 7.88)$. $(s_1, v_0^1) \rightarrow_A (s_2, v_1)$ is witnessed by: $(s_1, v_1) \rightarrow_A (s_2, v_2)$ (progress by 2.47 at $s_1$) $(s_1, v_1^1) \rightarrow_A (s_2, v_2^1)$ (progress by 2.89 at $s_2$), $(s_2, v_2^1) \xrightarrow{A} (s_2, v_2^2) \rightarrow_A (s_1, v_1)$ and transit to $s_1$ at $x_1 = 4.98 < 7$. Take a new pair $v_0^3 = (0, 4.89, 2.11)$, $v_0^3 = (5.28, 2.77, 7.39)$. It is easy to check $(v_0^3, v_1) \approx (v_0^3, v_1)$. From Lemma 10 $(s_1, v_0^3) \rightarrow_{\star_A} (s_2, v_2^3)$. Indeed, this is witnessed by $(s_1, v_0^3) \rightarrow_A (s_2, v_2^3)$ (progress by 2.51 at $s_1$) $(s_1, v_2^3) \rightarrow_A (s_2, v_2^3)$ (progress by 2.77 at $s_2$). These two witnesses differ slightly (2.47 vs. 2.51 and 2.77). We choose 2.77 and 2.51 by looking at the first witness backwardly. Thus, $v_2^3$ is picked such that $(v_2, v_2^3) \approx (v_0^3, v_1)$. Then, $v_2^3$ is picked such that $(v_2, v_2^3) \approx (v_0^3, v_1)$. The existence of $v_2^3$ and $v_2^3$ is guaranteed by Lemma 8. Finally, according to Lemma 9 again, $v_2^3$ is able to go back to $v_0^3$. This is because $v_2^3$ goes back to $v_0$ through a one-step transition and $v_0^3$ is initial.

![Fig. 3. An example timed automaton $A$.](image)

$v_1^3 = (5.36, 2.89, 7.88)$. $(s_1, v_0^1) \rightarrow_{\star_A} (s_2, v_1^3)$ is witnessed by: $(s_1, v_1^3) \xrightarrow{A} (s_2, v_2^3)$ (progress by 2.47 at $s_1$) $(s_1, v_1^3) \rightarrow_A (s_2, v_2^3)$ (progress by 2.89 at $s_2$). Next, take a new pair $v_0^4 = (0, 4.89, 2.11)$, $v_0^4 = (5.28, 2.77, 7.39)$. It is easy to check $(v_0^4, v_1^3) \approx (v_0^4, v_1^3)$. From Lemma 10 $(s_1, v_0^4) \rightarrow_{\star_A} (s_2, v_2^4)$. Indeed, this is witnessed by $(s_1, v_0^4) \rightarrow_A (s_2, v_2^4)$ (progress by 2.51 at $s_1$) $(s_1, v_2^4) \rightarrow_A (s_2, v_2^4)$ (progress by 2.77 at $s_2$). These two witnesses differ slightly (2.47 vs. 2.51 and 2.77). We choose 2.77 and 2.51 by looking at the first witness backwardly. Thus, $v_2^4$ is picked such that $(v_2, v_2^4) \approx (v_0^4, v_1^3)$. Then, $v_2^4$ is picked such that $(v_2, v_2^4) \approx (v_0^4, v_1^3)$. The existence of $v_2^4$ and $v_2^4$ is guaranteed by Lemma 8. Finally, according to Lemma 9 again, $v_2^4$ is able to go back to $v_0^4$. This is because $v_2^4$ goes back to $v_0$ through a one-step transition and $v_0^4$ is initial. 

Now, we express $\rightarrow_{\star_A}$ in a form treating the integral parts and the fractional parts of clock values separately. For any pattern $\eta \in \Phi$, any discrete valuations $u_0$ and $u_1$, and any stack words $w_0$ and $w_1$, define $(s_0, u_0, w_0)$ $\rightarrow_{A, \eta} (s_1, u_1, w_1)$ to be

$$\exists v_0 \exists v_1 (v_0(0) = 0 \land \lfloor v_0 \rfloor = u_0 \land \lfloor v_1 \rfloor = u_1$$

$$
\land (v_0, v_1) \in \eta \land (s_0, v_0, w_0) \rightarrow_{\star_A} (s_1, v_1, w_1)).$$
Lemma 11. Let $\mathcal{A}$ be a PTA. For any states $s_0$ and $s_1$, any initialized pair $(v_0, v_1)$, and any stack words $w_0$ and $w_1$, $(s_0, [v_0], w_0) \rightarrow^{*}_{\mathcal{A}} (s_1, [v_1], w_1)$ iff

$$\bigvee_{\eta \in \Phi} (((v_0), [v_1]) \in \eta \land (s_0, [v_0], w_0) \rightarrow^{*}_{\mathcal{A}, \eta} (s_1, [v_1], w_1)).$$

Proof. ($\Rightarrow$) is immediate.

($\Leftarrow$) uses the following observation (from the definition of $\rightarrow^{*}_{\mathcal{A}, \eta}$ and Lemma 10): for any pattern $\eta$, $((v_0), [v_1]) \in \eta \land (s_0, [v_0], w_0) \rightarrow^{*}_{\mathcal{A}, \eta} (s_1, [v_1], w_1)$ implies $((v_0), [v_1]) \in \eta \land (s_0, [v_0] + (v_0), w_0) \rightarrow^{*}_{\mathcal{A}} (s_1, [v_1] + [v_1], w_1).$ \hfill \Box

Once we give a characterization of $\rightarrow^{*}_{\mathcal{A}, \eta}$, Lemma 11 immediately gives a characterization for $\rightarrow^{*}_{\mathcal{A}}$. Fortunately, the characterization of $\rightarrow^{*}_{\mathcal{A}, \eta}$ is a decidable one, as shown in the next section.

6 The Pattern Graph of a Timed Pushdown Automaton

Let $\mathcal{A} = (S, \{x_1, \ldots, x_k\}, \text{Inv}, R, \Gamma, PD)$ be a PTA specified in the previous section. The pattern graph $G$ of $\mathcal{A}$ is a tuple

$$(S \times \Phi, \{y_0, \ldots, y_k\}, E, \Gamma)$$

where

- $S$ is the states in $\mathcal{A}$,
- $\Phi$ is the set of all patterns. A node is an element in $S \times \Phi$,
- Discrete clocks $y_0, \ldots, y_k$ are the integral parts of the clocks $x_0, \ldots, x_k$ in $\mathcal{A}$,
- $E$ is a finite set of (directed) edges that connect between nodes. An edge can be a progress edge, a stay edge, or a reset edge. A progress edge corresponds to progress transitions in $\mathcal{A}$ that cause one pattern change. A stay edge corresponds to progress transitions in $\mathcal{A}$ that cause no pattern change. Since a progress transition can cause no pattern change only from a merge-pattern, a stay edge connects a merge-pattern to itself. A reset edge corresponds to a reset transition in $\mathcal{A}$. Formally, a progress edge $(s, \eta) \rightarrow (s, \eta')$ that connects node $(s, \eta)$ to node $(s, \eta')$ is in the form of $((s, \eta), (s, \eta'))$ such that $c = \text{Inv}(s), \eta' = \text{Next}(\eta)$ (thus $\eta \neq \eta'$). A stay edge $(s, \eta, \eta)$, with $\eta$ being a merge-pattern, that connects node $(s, \eta)$ to itself is in the form of $((s, \eta), (s, \eta))$ such that $c = \text{Inv}(s)$. A reset edge $(s, \eta, r, (a, \gamma))$ that connects node $(s, \eta)$ to node $(s', \eta')$ is in the form of $((s, \eta), (c, r, a, \gamma), (s', \eta'))$

where $R(s, s') = (c, r)$ and $PD(s, s') = (a, \gamma)$. $E$ is the set of all progress edges, stay edges, and reset edges wrt $\mathcal{A}$. Obviously, $E$ is finite.

A configuration of $G$ is a tuple $(s, \eta, u, w)$ of state $s \in S$, pattern $\eta \in \Phi$, discrete valuation $u \in (\mathbb{N}^+)^{k+1}$ and stack word $w \in \Gamma^*$. $(s, \eta, u, w) \rightarrow^e (s', \eta', u', w')$ denotes a one-step transition through edge $e$ of $G$ if the following conditions are satisfied:
- if \( e \) is a progress edge, then \( e \) takes the form \((\langle s, \eta \rangle, c, \langle s, \eta' \rangle)\) and \( s' = s, u \in c^\eta, u' \in c^\eta, \text{next}(\eta, u) = (\eta', u') \) and \( w = w' \). Here \( c^\eta \) and \( c^\eta' \) are called the pre- and the post- (progress) tests on edge \( e \), respectively.
- if \( e \) is a stay edge, then \( e \) takes the form \((\langle s, \eta \rangle, c, \langle s, \eta \rangle)\) and \( s = s', u \in c^\eta, u = u', \eta = \eta' \) and \( w = w' \). Here \( c^\eta \) is called the pre- and the post- (stay) tests on edge \( e \).
- if \( e \) is a reset edge, then \( e \) takes the form \((\langle s, \eta \rangle, c, \langle s', \eta' \rangle)\) and \( u \in (c \land \text{Inv}(s))^\eta, u' \in \text{Inv}(s')^\eta, \text{reset}_c(\eta, u) = (\eta', u') \) and \( w = aw', w' = \gamma w'' \) for some \( w'' \in T^* \) (i.e., \( w \) changes to \( w' \) according to the stack operation). Here \( (c \land \text{Inv}(s))^\eta \) and \( \text{Inv}(s')^\eta \) are called the pre- and the post- (reset) tests on edge \( e \), respectively.

We write \((s, \eta, u, w) \rightarrow_G (s', \eta', u', w')\) if \((s, \eta, u, w) \rightarrow^e (s', \eta', u', w')\) for some \( e \).

The binary reachability \( \rightarrow_G^* \) is the transitive closure of \( \rightarrow_G \).

The pattern graph \( G \) simulates \( \mathcal{A} \) in a way that the integral parts of the dense clocks are kept but the fractional parts are abstracted as a pattern. Edges in \( G \) indicate how the pattern and the discrete clocks change when a clock progress or a clock reset occurs in \( \mathcal{A} \). However, a progress transition in \( \mathcal{A} \) could cause more than one pattern change. In this case, this big progress transition is treated as a sequence of small progress transitions such that each causes one pattern change (and therefore, each small progress transition in \( \mathcal{A} \) can be simulated by a progress edge in \( G \)). We first show that the binary reachability \( \rightarrow_G^* \) of \( G \) is NPCA. Observe that discrete clocks \( y_0, \ldots, y_k \) are the integral values of dense clocks \( x_0, \ldots, x_k \). Even though the dense clocks progress synchronously, the discrete clocks may not be synchronous (i.e., that one discrete clock is incremented by \( 1 \) does not necessarily cause all the other discrete clocks incremented by the same amount). The proof has two parts. In the first part of the proof, a technique is used to translate \( y_0, \ldots, y_k \) into another array of discrete clocks that are synchronous. In the second part of the proof, \( G \) can be treated as a discrete PTA \( [19] \) by replacing \( y_0, \ldots, y_k \) with the synchronous discrete clocks. Therefore, Lemma 12 is obtained from the fact \( [19] \) that the binary reachability of discrete PTA is NPCA.\(^2\)

**Lemma 12.** For any PTA \( \mathcal{A} \), the binary reachability \( \rightarrow_G^* \) of the pattern graph \( G \) of \( \mathcal{A} \) is NPCA. In particular, if \( \mathcal{A} \) is a timed automaton, then the binary reachability \( \rightarrow_G^* \) is Presburger.

**Proof.** We start with a technique that makes discrete clocks \( y_0, \ldots, y_k \) (i.e., the integral parts of dense clocks) synchronous on any path of \( G \).

A pattern ordering graph \( \mathcal{P} \) is a directed graph on \( \Phi \). For each (ordered) pair \((\eta, \eta')\) in \( \Phi \times \Phi \), \((\eta, \eta')\) is a progress edge, written \( \eta \rightarrow_p \eta' \), if \( \text{Next}(\eta) = \eta' \). In this case, we say the edge has label \( p \) (stands for “progress”) and \( \eta' \) is called the \( p \)-successor of \( \eta \). \((\eta, \eta')\) is a reset edge with \( r \subseteq K^+ \), written \( \eta \rightarrow_r \eta' \), if \( \text{Reset}_r(\eta) = \eta' \). In this case, we say the edge has label \( r \) and \( \eta' \) is called the \( r \)-successor of \( \eta \). An edge can have multiple labels.

\( ^2\)For the purpose of this paper, we assume in Lemma 12 that \( \rightarrow_G^* \) is restricted in such a way that \( \eta \) is a regulated pattern whenever \((s, \eta, u, w) \rightarrow_G^* (s', \eta', u', w') \). This is because the auxiliary clock \( x_0 \) in \( \mathcal{A} \) starts from 0.
A path $\tau$ on $\mathcal{P}$ is a sequence of edges

$$\eta_0 \rightarrow i_1 \cdots \rightarrow i_m, \eta_m$$

such that each $l_i$ is a label (either $p$ or some $r \subseteq K^+$). $j \in K^+$ is reset on path $\tau$ if $j \in l_i \subseteq K^+$ for some $1 \leq i \leq m$. Path $\tau$ is a $p$-path if each edge on the path is a progress edge; i.e., label $l_i$ is $p$ for all $1 \leq i \leq m$. Path $\tau$ is a regulated path if $\eta_0$ is a regulated pattern. Path $\tau$ is a $p$-ring of $\eta_0$ if $\tau$ is a $p$-path, and $\eta_0, \ldots, \eta_m$ is the pattern ring of $\eta_0$.

Now we augment $\mathcal{P}$ with counters $y = (y_0, \ldots, y_k)$ taking values in $(\mathbb{N}^+)^{k+1}$. Values of counters $y$ change along a path in $\mathcal{P}$. For each progress edge $\eta \rightarrow_p \eta'$, counters $y$ change to $y'$ as follows: $y' := y + \Delta_\eta$ (recall $\Delta_\eta$ is the increment vector for $\eta$), consistent to the definition that $\text{next}(\eta, y) = (\eta', y + \Delta_\eta)$. For each reset edge $\eta \rightarrow_r \eta'$, counters $y$ change to $y'$ as follows: $y' := y \downarrow_r$, consistent to the definition that $\text{reset}_r(\eta, y) = (\eta', y \downarrow_r)$. For a $p$-path $\tau = \eta_0, \ldots, \eta_m$, $\Delta_\tau = \sum_{0 \leq i \leq m-1} \Delta_{\eta_i}$ is the net increment for counters $y$ after walking through the path. In particular, $\Delta_\tau = 1$ for each $p$-ring $\tau$.

A progress edge $\eta \rightarrow_p \eta'$ is add-1 if $\eta'$ is a regulated pattern. A path is short if it is a regulated path and, it does not contain an add-1 edge or it contains an add-1 edge but only at the end of the path. A path is add-1 if it is a short path containing an add-1 edge. By definition, an add-1 path starts and ends with regulated patterns and each pattern in between along the path is not a regulated pattern. The following lemma is directly from the definitions of reset and next.

**Lemma 13.** For any path $\tau$, (1). if $\tau$ is a short path, then for each $i \in K^+$ that is reset on $\tau$, $y_i$ has value 0 at the end of $\tau$, (2). if $\tau$ is an add-1 path, then for each $i \in K^+$ that is not reset on $\tau$, $y_i$ has progressed by exactly 1 at the end of $\tau$.

When walking along a path in $\mathcal{P}$, a counter in $y$ is always nondecreasing except sometimes it resets. However, counters $y$ are not synchronous: that one counter’s advancing by 1 at some progress edge does not always cause all the other counters to advance by the same amount.

Now we are going to show that, on any regulated path, $y$ can be simulated by a set of synchronous counters $z = z_0, \ldots, z_k$. The ideas are as follows. Let $\tau$ be any regulated path of $\mathcal{P}$. $\tau$ then can be concatenated by segments: a number of add-1 paths followed by a short path. We introduce an increment vector $\Delta \in \{0, 1\}^{k+1}$ to denote how much a counter in $y$ progresses on a segment. Besides, we use $I \subseteq K^+$ to remember the indices $i \in K^+$ that are reset on each segment. Assume counters $y$ walk through $\tau$ and change counter values from $u$ to $u'$. Then, in the simulation, counters $z$ starts from $u$ with $\Delta = 0$ and $I = \emptyset$. After walking through $\tau$ (while updating $\Delta$ and $I$ along the path), counters $z$ have values satisfying $u' = (z + \Delta) \downarrow_I$. The simulation is defined by the following translation. For each progress edge $\eta \rightarrow_p \eta'$, the instruction $y' := y + \Delta_\eta$ is replaced by:

- if $\eta'$ is a regulated pattern (hence the edge is an add-1 edge), i.e., the end of the current segment, then $z' := (z + 1) \downarrow_I$ (synchronous progress followed by resets);
  $I' := \emptyset; \Delta' := 0$;
- else, 
  \[ z' := z; \ I' := I; \ \Delta' := \Delta + \Delta_y. \]

For each reset edge \( \eta \rightarrow_r \eta' \), the instruction \( y' := y \downarrow_r \) is replaced by:

- \[ z' := z \downarrow_r; \ \Delta' := \Delta \downarrow_r; \ I' := I \cup r. \]

Obviously \( z \) are synchronous. The correctness of the algorithm is stated as follows.

Claim. For any regulated path \( \tau \), \( y = (z + \Delta) \downarrow_I \) at the end of \( \tau \).

Proof. Given a regulated path \( \tau \). Since \( \tau \) can be split into a number of segments as mentioned before, and by looking at the translation, at the end of each add-1 path, \( \Delta = 0 \) and \( I = \emptyset \) (i.e., the initial values for \( \Delta \) and \( I \)). Therefore, it suffices to show the claim for a segment, i.e., a short path \( \tau \), by induction on the length of \( \tau \). Notice that, from the translation, \( I \) stands for the set of indices that has been reset on the short path; \( \Delta \) stands for the increment that has been made on the short path for counters \( y \). The relationship between \( I \) and \( \Delta \) is established in Lemma 13, which will be used in the proof.

Case 1. The claim trivially holds for \( \tau \) with length 1.

Case 2. Assume the claim holds for short paths with length \( \leq m \). Now consider a short path with length \( m + 1 \). This path can be written as a short path \( \tau \) followed by an edge \( e \) of \( (\eta, \eta') \). Note that, by the induction hypothesis, \( y = (z + \Delta) \downarrow_I \) at \( \eta \) (the end of \( \tau \)). Now we are going to show \( y' = (z' + \Delta') \downarrow_{I'} \) where primed values are for node \( \eta' \).

Case 2.1. If edge \( e \) is a progress edge and \( \eta' \) is a regulated pattern, then, from the translation, \( z' = (z + 1) \downarrow_I \), \( I' = \emptyset \), \( \Delta' = 0 \). Therefore,

\[
\begin{align*}
\ y' & = y + \Delta_y = (\text{induction}) \\
(z + \Delta) \downarrow_I + \Delta_y & = (\text{Lemma 13(1)}) \\
(z + \Delta + \Delta_y) \downarrow_I & = (\text{Lemma 13(2)}) \\
(z + 1) \downarrow_I & = z' \quad (\text{since } I' = \emptyset, \Delta' = 0) \\
(z' + \Delta') & \downarrow_{I'}. 
\end{align*}
\]

Case 2.2. If the edge is a progress edge and \( \eta' \) is not a regulated pattern, then, from the translation, \( z' = z \), \( I' = I \), and \( \Delta' = \Delta + \Delta_y \). Therefore,

\[
\begin{align*}
\ y' & = y + \Delta_y = (\text{induction}) \\
(z + \Delta) \downarrow_I + \Delta_y & = (\text{Lemma 13(1)}) \\
(z + \Delta + \Delta_y) \downarrow_I & = (\text{Lemma 13(2)}) \\
(z' + \Delta') & \downarrow_{I'}. 
\end{align*}
\]

Case 2.3. If the edge is a reset edge \( \eta \rightarrow_r \eta' \), then, from the translation, \( z' = z \downarrow_r \), \( \Delta' = \Delta \downarrow_r \), and \( I' = I \cup r \). Therefore,

\[
\begin{align*}
\ y' & = y \downarrow_r = (\text{induction}) \\
(z + \Delta) \downarrow_I & = (\text{Lemma 13(1)}) \\
(z' + \Delta') & \downarrow_{I'}. 
\end{align*}
\]

Hence, the claim holds.

Now we continue the proof of Lemma 13. Let \( G \) be the pattern graph of a timed automaton \( A \). A path in \( G \) witnessing

\[
(s, \eta, u, w) \rightarrow_G (s', \eta', u', w')
\]
(with $\eta$ being a regulated pattern) between two configurations corresponds to a regulated path (by properly adding stack operations) in the pattern ordering graph $P$. In above, we have demonstrated a technique such that counters $y = y_0, \ldots, y_k$ can be simulated by synchronous counters $z = z_0, \ldots, z_k$ using an increment vector $\Delta \in \{0, 1\}^{k+1}$ and a reset set $I \subseteq K^+$. The relationship between $y$ and $z$ is $y = (z + \Delta) \downarrow I$.

To show that

\[ y \rightarrow y' \text{ when the fractional parts of dense clocks are abstracted away by a pattern.} \]

**Lemma 14.** Let $A$ be a PTA with pattern graph $G$. For any states $s_0$ and $s_1$ in $S$, any pattern $\eta \in \Phi$, any stack words $w_0$ and $w_1$ in $\Gamma^*$, and any discrete valuation pairs $(u_0, u_1)$ with $u_0(0) = 0$, we have,

\[ (s_0, u_0, w_0) \rightarrow_A^{s_0} (s_1, u_1, w_1) \text{ iff } (s_0, \text{init}(\eta), u_0, w_0) \rightarrow_G^{s_0} (s_1, \eta, u_1, w_1). \]

**Proof.** Fix any states $s_0, s_1 \in S$, any pattern $\eta \in \Phi$, any stack words $w_0$ and $w_1$ in $\Gamma^*$, and any discrete valuation pairs $(u_0, u_1)$ with $u_0(0) = 0$.

($\Rightarrow$). By the definition of $(s_0, u_0, w_0) \rightarrow_A^{s_0} (s_1, u_1, w_1)$, there exists an initialized pair $(v_0, v_1)$ such that

1. $(v_0, v_1)$ has pattern $\eta$,
2. $[v_0] = u_0$, $[v_1] = u_1$,
3. $(s_0, v_0, w_0) \rightarrow_A^{s_0} (s_1, v_1, w_1)$.

In order to show that $(s_0, [v_0], [w_0]) \rightarrow_G^{s_0} (s_1, [v_0], [w_1])$ (notice that $\text{init}(\eta) = ([v_0], v_0)$), it suffices to show that each one-step transition in $A$ can be simulated by $\rightarrow_G^{s_0}$ properly: for any valuations $v, v'$, any states $s$ and $s'$, and any stack words $w$ and $w'$, if $(s, v, w) \rightarrow_A^{s_0} (s', v', w')$ then $(s, [v_0], [v], w) \rightarrow_G^{s_0} (s', [v_0], [v'], w')$.

Case 1. For any valuation $v$ and state $s$, consider a progress transition in $A$, $(s, v, w) \rightarrow_A (s + \delta, w')$, $\delta > 0$, such that (by definition) $w = w'$, and $v(0) \leq \delta' \leq \delta, v + \delta' \in Inv(s)$. Let $\eta_0$ be the pattern of $(v_0, v)$. If $v$ has no pattern change for $\delta$, then $\eta_0$ must
be a merge-pattern. This progress transition in $A$ can therefore be simply simulated by the stay edge in $G$ at state $s$. If, however, $v$ has at least one pattern change for $\delta$, then assume the $p$-ring of $\eta_0$ is $\eta_0, \ldots, \eta_m = \eta_0$. This progress transition in $A$ can be simulated by the following path consisting of progress edges in $G$: looping along the $p$-ring for $[\delta]$ times on state $s$ in $G$, followed by a prefix of the $p$-ring ended with the pattern $\eta_i$, for some $i$, of $(v_0, v + \delta)$. From Lemma 5 and Lemma 6, it can be established $(s, \eta_0, [v], w) \rightarrow^* (s, \eta_i, [v + \delta], w)$ through the path in $G$, noticing that tests for $Inv(s)$ are consistent in $A$ and $G$ (Lemma 8), and the stack word does not change for progress transitions in both $A$ and $G$.

Case 2. For any valuation $v$ and states $s$ and $s'$, consider a reset transition $(s, v, w) \rightarrow_A (s', v \downarrow_r, w')$ in $A$ such that (by definition) $w = aw''$, $w' = \gamma w''$ for some $w''$ with $PD(s, s') = (a, \gamma)$, $R(s, s') = (c, r)$ and $v \in Inv(s) \cap c, v \downarrow_r \in Inv(s')$. Assume the pattern of $(v_0, v)$ is $\eta_0$ and the pattern of $(v_0, v \downarrow_r)$ is $\eta'_0$. This reset transition in $A$ corresponds to the reset edge in $G$: $((s, \eta_0), c, r, a, \gamma, (s', \eta'_0))$. From Lemma 5, it can be established $(s, \eta_0, [v], w) \rightarrow^*_G (s', \eta'_0, [v \downarrow_r], w')$ through this edge, noticing that tests for $Inv(s) \cap c$ and $Inv(s')$ are consistent in $A$ and $G$ (Lemma 8), and the stack operations are the same in $A$ and $G$.

$(\Rightarrow)$. Suppose $(s_0, init(\eta), u_0, w_0) \rightarrow^*_G (s_1, \eta, u_1, w_1)$. We would like to show

$$(s_0, u_0, w_0) \rightarrow^*_A (s_1, u_1, w_1).$$

Pick any initial valuation $v_0$ such that $(v_0, v_0)$ has pattern $init(\eta)$ and $[v_0] = u_0$. Suppose $(s^0, \eta_0, u^0, w^0) \rightarrow^{e_1} \cdots \rightarrow^{e_m} (s^m, \eta_m, u^m, w^m)$ is a path (in $G$) witnessing $(s_0, init(\eta), u_0, w_0) \rightarrow^*_G (s_1, \eta, u_1, w_1)$ through edges $e_1, \ldots, e_m$ such that

$$(s^0, \eta_0, u^0, w^0) = (s_0, init(\eta), u_0, w_0)$$

and

$$(s^m, \eta_m, u^m, w^m) = (s_1, \eta, u_1, w_1).$$

A path in $A$

$$(s^0, v^0, w^0) \rightarrow^{t_1} \cdots \rightarrow^{t_m} (s^m, v^m, w^m)$$

is constructed as follows, where $v^0 = v_0$ and each transition $t_i$ in $A$ corresponds to each edge $e_i$ in $G$. From $i = 1$ to $m$, each $t_i$ belongs to one of the following three cases:

Case 1. $e_i$ is a progress edge in $G$. In this case, $next(\eta_{i-1}, u^{i-1}) = (\eta_i, u^i)$, $w^i = w^{i-1}$, and $s^i = s^i$. We pick $t_i$ to be a progress transition (at state $s^{i-1}$) in $A$ from $v^{i-1}$ with an amount of $\delta$ that causes exactly one pattern change (Lemma 6 and Lemma 7). Take $w^i = w^{i-1} + \delta$. Notice that both the progress edge and the progress transition do not change the stack content, i.e., $w^i = w^{i-1}$.

Case 2. $e_i$ is a stay edge in $G$. In this case, $\eta_{i-1} = \eta_i$ must be a merge-pattern with $w^i = w^{i-1}$ and and $s^{i-1} = s^i$. We pick $t_i$ to be a progress transition (at state $s^{i-1}$) in $A$ from $v^{i-1}$ with an amount of $\delta$ that causes no pattern change (Lemma 6). Similarly to Case 1, $w^i = w^{i-1}$.

Case 3. $e_i$ is a reset edge from state $s^{i-1}$ to state $s^i$ with clock resets $r$ in $G$, then $t_i$ is the reset transition from state $s^{i-1}$ to state $s^i$ with clock resets $r$ in $A$. Notice that
both $e_i$ and $f_i$ have the same stack operation. Take $v^i = v^{i-1} \downarrow r$ and $w^i$ is the result of the stack operation on $w^{i-1}$.

Notice that, for each $i = 1 \cdots m$,
- $(v_0, v^i)$ has pattern $\eta_i$,
- $[v^i] = u_i$.

This can be shown using Lemma 5 for Case 1, Lemma 6 for Case 2, and Lemma 7 for Case 3. Therefore, this constructed path of $\mathcal{A}$ keeps the exactly the same patterns and integral parts of clocks as well as the stack word as in the path for $G$. From Lemma 8, clock tests (and obviously the stack operations) are consistent between the path in $G$ and the constructed path in $\mathcal{A}$. Hence, $(s_0, u_0, w_0) \rightarrow^*_A (s_1, u_1, w_1)$ since, by taking $v_1 = v^m$,
- $(v_0, v_1)$ has pattern $\eta$,
- $[v_0] = u_0, [v_1] = u_1$,
- $(s_0, v_0, w_0) \rightarrow^*_A (s_1, v_1, w_1)$.

Now, we conclude this section by claiming that $\rightarrow^*_A, \eta$ is NPCA by combining Lemma 12 and Lemma 14.

Lemma 15. For any PTA $\mathcal{A}$ and any fixed pattern $\eta \in \Phi$, $\rightarrow^*_\mathcal{A}, \eta$ is NPCA. In particular, if $\mathcal{A}$ is a timed automaton, then $\rightarrow^*_\mathcal{A}, \eta$ is Presburger.

7 A Decidable Binary Reachability Characterization and Automatic Verification

Recall that PTA $\mathcal{A}$ actually has clocks $x_1, \cdots, x_k$. $x_0$ is the auxiliary clock. The binary reachability $\sim^*_\mathcal{A}$ of $\mathcal{A}$ is the set of tuples
\[
\langle s, v_1, \cdots, v_k, w, v'_1, \cdots, v'_k, w' \rangle
\]
such that there exist $v_0 = 0, v'_0 \in \mathbb{D}^+$ satisfying
\[
(s, v_0, \cdots, v_k, w) \sim^*_\mathcal{A} (s', v'_0, \cdots, v'_k, w').
\]
The main theorem of this paper gives a decidable characterization for the binary reachability as follows.

Theorem 1. The binary reachability $\sim^*_\mathcal{A}$ of a PTA $\mathcal{A}$ is $(\mathbb{D} + \text{NPCA})$-definable. In particular, if $\mathcal{A}$ is a timed automaton, then the binary reachability $\sim^*_\mathcal{A}$ can be expressed in the additive theory of reals (or rationals) and integers.

Proof. From Lemma 11, $\sim^*_\mathcal{A}$ is definable by the following formula:
\[
\exists u'_0 \in \mathbb{N}^+ \exists v'_0 \in \mathbb{D}^+ (\bigvee_{\eta \in \Phi} ((0, v_1, \cdots, v_k), (v'_0, \cdots, v'_k)) \in \eta \land
\]
on integer variables \( s, u_1, \ldots, u_k, \), \( s' = (s_0, \ldots, s_k), w \) and dense variables \( v_1, \ldots, v_k \) (over \( D^+ = D^+ \cap [0, 1) \)), and on word variables \( w \) and \( w' \). This formula is equivalent to

\[
\bigvee_{\eta \in \Phi} P^D_\eta(v_1, \ldots, v_k, v'_1, \ldots, v'_k) \land Q^N_\eta(s, u_1, \ldots, u_k, w, s', u'_1, \ldots, u'_k, w')
\]

where \( P^D_\eta(v_1, \ldots, v_k, v'_1, \ldots, v'_k) \) stands for

\[
\exists v'_0 \in D^+(((0, v_1, \ldots, v_k), (v'_0, \ldots, v'_k)) \in \eta)
\]

and \( Q^N_\eta(s, u_1, \ldots, u_k, w, s', u'_1, \ldots, u'_k, w') \) stands for

\[
\exists u'_0((s, (0, u_1, \ldots, u_k), w) \sim_{A, \eta}(s', (u'_0, \ldots, u'_k), w')).
\]

From the definition of patterns, \( P^D_\eta \), after eliminating the existential quantification, is a dense linear relation. On the other hand, \( Q^N_\eta \) (after eliminating the existential quantification, from Lemma 3 and Lemma 2) is NPCA. Therefore, \( \sim_{A, \eta}^B \) is \( (D + NPCA) \)-definable.

In particular, if \( A \) is a timed automaton, \( \sim_{A, \eta}^B \) is \( (D + NPCA) \)-definable by a formula in the additive theory of reals (or rationals) and integers. Hence, \( \sim_{A, \eta}^B \) itself can be expressed in the same theory.

The importance of the above characterization for \( \sim_{A, \eta}^B \) is that, from Lemma 2, the emptiness of \( (D + NPCA) \)-definable predicates is decidable. From Theorem 1 and Lemma 2(3)(4), we have,

**Theorem 2.** The emptiness of \( l \cap \sim_{A, \eta}^B \) with respect to a PTA \( A \) for any mixed linear relation \( l \) is decidable.

The emptiness of \( l \cap \sim_{A, \eta}^B \) is called a mixed linear property of \( A \). Many interesting safety properties (or their negations) for PTAs can be expressed as a mixed linear property. For instance, consider the following property of a PTA \( A \) with three dense clocks \( x_1, x_2, \) and \( x_3, \)

"for any two configurations \( \alpha \) and \( \beta \) with \( \alpha \sim_{A, \eta}^B \beta \), if the difference between \( \beta_{x_3} \) (the value of clock \( x_3 \) in \( \beta \)) and \( \alpha_{x_1} + \alpha_{x_2} \) (the sum of clocks \( x_1 \) and \( x_2 \) in \( \alpha \)) is greater than the difference between \( \#_a(\alpha_w) \) (the number of symbol \( a \) appearing in the stack word in \( \alpha \)) and \( \#_b(\beta_w) \) (the number of symbol \( b \) appearing in the stack word in \( \beta \)), then \( \#_a(\alpha_w) - 2\#_b(\beta_w) \) is greater than 5."

The negation of this property can be expressed as the emptiness of

\[
(s, x_1, x_2, x_3, w) \sim_{A, \eta}^B (s', x'_1, x'_2, x'_3, w') \land \neg l
\]

where \( l \) is the negation of a mixed linear relation (hence \( l \) itself is also a mixed linear relation):

\[
x'_3 - (x_1 + x_2) > \#_a(w) - \#_b(w') \rightarrow \#_a(w) - 2\#_b(w') > 5.
\]
Thus, from Theorem 2, this property can be automatically verified. We need to point out that

- \( x_3' - (x_1 + x_2) > \#_a(w) - \#_b(w') \) is a linear relation on both dense variables and discrete variables. Thus, this property can not be verified by using the decidable characterization for discrete PTAs [19], where only integer-valued clocks are considered.
- Even without clocks, \( \#_a(w) - 2\#_b(w') > 5 \) expresses a non-regular set of stack word pairs. Therefore, this property can not be verified by the model-checking procedures for pushdown systems [9, 23].
- Even without the pushdown stack, \( x_3' - (x_1 + x_2) > 0 \) (by taking \( \#_a(w) - \#_b(w') \) as a constant such as 0) is not a clock region, therefore, the classical region-based techniques can not verify this property. This is also pointed out in [16].
- With both dense clocks and the pushdown stack, this property can not be verified by using the region-based techniques for Timed Pushdown Systems [10].

When \( \mathcal{A} \) is a timed automaton, by Theorem 1, the binary reachability \( \sim_{\mathcal{A}}^{\mathcal{B}} \) can be expressed in the additive theory of reals (or rationals) and integers. Notice that our characterization is essentially equivalent to the one given by Comon and Jurski [16] in which \( \sim_{\mathcal{A}}^{\mathcal{B}} \) can be expressed in the additive theory of reals augmented with a predicate telling whether a term is an integer. Because the additive theory of reals and integers is decidable [11, 12], we have,

**Theorem 3.** The truth value for any closed formula expressible in the (first-order) additive theory of reals (or rationals) augmented with a predicate \( \sim_{\mathcal{A}}^{\mathcal{B}} \) for a timed automaton \( \mathcal{A} \) is decidable. (also shown in [16])

For instance, consider the following property for a timed automaton \( \mathcal{A} \) with two real clocks:

“there are states \( s \) and \( s' \) such that, for any \( x_1, x_2, x_2' \), there exists \( x_1' \) such that if \( (s, x_1, x_2) \) can reach \( (s', x_1', x_2') \) in \( \mathcal{A} \), then \( x_1 - x_2 > x_1' - x_2' \).”

It can be expressed as

\[
\exists s, s' \forall x_1, x_2, x_2' \exists x_1' ((s, x_1, x_2) \sim_{\mathcal{A}}^{\mathcal{B}} (s', x_1', x_2') \rightarrow x_1 - x_2 > x_1' - x_2'),
\]

and thus can be verified according to Theorem 3.

### 8 Conclusions, Discussions and Future Work

In this paper, we consider PTAs that are timed automata augmented with a pushdown stack. A configuration of a PTA includes a control state, finitely many dense clock values and a stack word. By introducing the concept of a clock pattern and using an automata-theoretic approach, we give a decidable characterization of the binary reachability of a PTA. Since a timed automaton can be treated as a PTA without the pushdown stack, we can show that the binary reachability of a timed automaton is definable in the additive theory of reals and integers. The results can be used to verify a class of safety
properties containing linear relations over both dense variables and unbounded discrete variables.

A PTA studied here can be regarded as the timed version of a pushdown machine. Carefully looking at the proofs of the decidable binary reachability characterization, we find out that the underlying untimed machine (e.g., the pushdown machine) is not essential. We can replace it with many other kinds of machines and the resulting timed system still has a decidable binary reachability characterization. We will summarize some of these machines in this section.

Consider a class of machines $X$. We use $X_{CM}$ to denote machines in $X$ augmented with reversal-bounded counters. We are looking at the binary reachability characterization of the timed version of machines in $X$. The characterization is established in the previous sections when $X$ represents pushdown machines. In the proofs, a dense clock is separated into a fractional part and an integral part. The fractional parts of dense clocks are abstracted as a pattern and the integral parts are translated into synchronous discrete clocks, which are further translated into reversal-bounded counters [19]. The result of the translation is the underlying untimed machine in $X$ augmented with these reversal-bounded counters, i.e., a machine in $X_{CM}$. Suppose a class of automata $Y$ accept the binary reachability of machines in $X_{CM}$. In the case of $X$ being pushdown machines, $X_{CM}$ represents NPCMs and $Y$ can be chosen as NPCAs (it is known that the binary reachability of NPCMs can be accepted by NPCAs [19]). The fact that this $Y$ (i.e., NPCA) satisfies Lemma 2 is the only condition we need in order to obtain the decidable reachability characterization in Theorem 1. Definitions like NPCA predicates and $(D+\text{NPCA})$-definability can be accordingly modified into $Y$ predicates and $(D+Y)$-definability once $Y$ is clear. The above discussions give the following result.

**Theorem 4.** Let $Y$ be a class of automata, $X$ be a class of machines and $X_{CM}$ be the class of machines in $X$ augmented with reversal-bounded counters. If, for each machine in $X_{CM}$, an automaton in $Y$ can be constructed that accepts the binary reachability of the machine, and Lemma 2 holds (replacing NPCA with $Y$), then the binary reachability of the timed version of $X$ is $(D+Y)$-definable.

Notice that Lemma 2 (4) requires that the emptiness problem for $Y$ in Theorem 4 be decidable. Theorem 2 can be immediately followed from Theorem 4 for the timed version of $X$.

According to Theorem 4, the timed version of the following machines $X$ has a decidable $(D+Y)$-definable characterization for binary reachability by properly choosing $Y$:

- NPCM. Here $Y$=NPCA;
- NCM with an unrestricted counter. Notice that the counter is a special case of a pushdown stack (when the stack alphabet is unary). Here, $Y$=NPCA;
- Finite-crossing NCM [28] (i.e., NCM augmented with a finite-crossing read-only worktape. The head on the worktape is two-way, but for each cell of the tape, the head crosses only a bounded number of times.). Here, $Y$ is finite-crossing NCAs [28] that are NCM augmented with a finite-crossing input tape.
- Reversal-bounded multipushdown machines [17] that are multipushdown machines [13] augmented with reversal-bounded counters. Here, $Y$ is reversal-bounded multipushdown automata [17].
Let $X$ be a class of machines. The pattern technique tells us that, for a decidable binary reachability characterization of the timed version of $X$, the density of clocks (and even clocks themselves) is not the key issue. This is because, using the technique, these dense clocks can be reduced to reversal-bounded integer counters. The key issue is whether $X$ and its reversal-bounded version $X_{CM}$ have a decidable binary reachability characterization (i.e., the binary reachability can be accepted by a class $Y$ of automata with a decidable emptiness problem). In particular, when the binary reachability of $X$ is effectively semilinear (and hence the binary reachability is decidable), in most cases, the binary reachability of $X_{CM}$ is also effectively semilinear. Such $X$ includes all the machines mentioned above. In this case, once we can show the untimed machines in $X$ have a decidable binary reachability characterization, we are getting really close to the decidable characterization for their timed version. But, we do have exceptions. For instance, consider $X$ to be a finite state machine with a two-way read only worktape. $X$ has a decidable binary reachability characterization (witnessed by two-way multitape finite automata). However, augmenting $X$ with reversal-bounded counters makes the binary reachability undecidable. The pitfall here is that a two-way tape makes reversal-bounded counters too powerful. In fact, the emptiness problem is undecidable for two-way automata augmented with reversal-bounded counters. In the case when there is only one reversal-bounded counter, the emptiness problem is decidable if the machines are deterministic. The nondeterministic case is still open [29].

In practice, augmenting timed automata with other unbounded data structures allows us to study more complex real-time applications. For instance, the decidable characterization of PTAs makes it possible to implement a tool verifying recursive real-time programs containing finite-state variables against safety properties containing linear constraints over dense clocks and stack word counts. This tool will be a good complement to available tools for recursive finite state programs (for regular safety properties, e.g., termination) [23]. On the other hand, for the existing tools analyzing real-time systems (such as UPPAAL [30] and its extensions [31], TREX [31], HyTECH [24], Kronos [11]), the traditional region-based technique used in the tools may be enhanced with the pattern technique. Doing this makes it possible for the tools to verify complex timing requirements that may not be in the form of clock regions. The results in this paper can also be used to implement a model-checker for a subset of the real-time specification language ASTRAL [14]. The subset includes history-independent ASTRAL specifications containing both dense clocks and unbounded discrete control variables.

As mentioned in this section, the timed version of NPCM (i.e., PTAs further augmented with reversal-bounded counters) also has a decidable characterization. This timed model has many important applications. For instance, a real-time recursive program (containing unbounded integer variables) can be automatically debugged using the reversal-bounded approximation (i.e., assign a reversal-bound to the variables). Additionally, a free counter (i.e., an unrestricted counter) is a special case for a pushdown stack (when the stack alphabet is unary). Therefore, this model can also be used to specify real-time systems containing a free counter and many reversal-bounded counters. It seems that “reversal-bounded counters” appear unnatural and therefore their applications in practice are remote. However, a non-decreasing counter is also a reversal-bounded counter (with zero reversal-bound). This kind of counters have a lot of appli-
cations. For instance, a non-decreasing counter can be used to count digital time elapse, the number of external events, the number of a particular branch taken by a non-deterministic program (this is important, when fairness is taken into account), etc. For instance, consider a timed automaton with input symbols (i.e., a transition is triggered by an external event as well as the enabling condition). We use \( \#_a \) to denote the number of event \( a \) occurred so far. The enabling condition of a transition, besides clock constraints, may also include comparisons of the counts \( \#_a \) against an integer constant and comparisons of one specific linear term \( T \) (on all \( \#_a \)) against an integer constant. For instance, a transition may look like this (in pseudo-code):

\[
s: \text{if } \text{event}(a) \text{ and } x_2 - x_1 > 10 \text{ and } \#_b > 21 \text{ and } 2\#_c - 3\#_b < 5, \text{ then progress(); goto } s'
\]

where \( x_1 \) and \( x_2 \) are dense clocks. Notice that comparisons of the linear term \( 2\#_c - 3\#_b \) against an integer constant may show up in other transitions. But this term is unique in the automaton: a comparison like \( 4\#_a - 3\#_b > 8 \) that involves a different term \( 4\#_a - 3\#_b \) can not be used in the enabling conditions of the automaton. This timed automaton is a standard timed automaton augmented with reversal-bounded counters \( \#_a \) (which are non-decreasing) and a free counter (representing the linear term \( 2\#_c - 3\#_b \)). Hence, the following property can be automatically verified:

"It is always true that whenever \( x_1 - 7\#_b + 3x_2 > 2\#_a \) holds, \( x_1 \) must be greater \( \#_c - \#_a \).
"

A future research issue is to investigate whether the decidable results [21] for Presburger liveness of discrete timed automata can be extended to timed automata (with dense clocks) using the technique in this paper. We are also going to look at the possibility of extending the approximation approaches for parameterized discrete timed automata [20] to the dense clocks. This is particularly interesting, since the reachability set presented in [20] is not necessarily semilinear. Another issue is on the complexity analysis of the decision procedure presented in this paper. However, the complexity for the emptiness problem of NPCAs is still unknown, though it is believed that it can be derived along Gurari and Ibarra [24].

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