Improvement of fabrication accuracy of vertically curved silicon waveguide optical coupler using hard mask shielded ion implantation bending

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To obtain high device fabrication uniformity and reproducibility for vertically curved silicon waveguide optical coupler, we developed the high accuracy ion implantation bending (IIB) method by incorporating a tungsten mask that can partially shield the ion implantation. The developed IIB method improved the positional accuracy of the origin of vertically curved Si wire bending from a wet etching-level of 1 μm order to a dry etching-level of several 100 nm order, and we obtained a fabrication accuracy of about less than ±0.4 μm of the tip position of the Si-wire vertically curved structures. © 2020 The Japan Society of Applied Physics

Silicon photonics is a technology platform based on CMOS manufacturing processes for the fabrication of very small, high-density, and high-performance silicon photonic integrated circuits (Si-PICs). Recently, optical transceivers consisting of Si-PIC have been launched commercially for use in short reach optical interconnections in hyper-scale data centers. Thus silicon photonics has entered into large-scale manufacturing stage, and fabrication accuracy and reproducibility of the devices become very important.

Compared with electronics devices, input/output (I/O) coupling interfaces of silicon photonics require peculiar technologies, and optical couplers that bridge optical signals between Si waveguides and optical fibers have been important research issues. In silicon photonics, there have been two major approaches for optical coupling: edge coupling and surface coupling. Edge coupling can yield a broad spectrum bandwidth and polarization-insensitive nature but the device footprints and fiber assembly costs tend to be large.1–4 On the other hand, surface coupling enables large-scale manufacturing endowments of wafer-level testing and cost-effective fiber assembly but the typical surface coupling method using grating couplers is accompanied with limited spectrum bandwidths and strong polarization dependence.5–8

Recently, we developed an alternative surface coupler consisting of a vertically curved silicon waveguide at the terminal of Si-PIC.9–15 This coupler (called “elephant coupler”) bends the propagating direction of light to vertical angle from the Si-PIC plane with broad spectrum bandwidth and polarization-insensitive nature. In addition, since multiple elephant couplers can be placed two-dimensionally on a Si-PIC chip, elephant coupler is suited for the attachment of multiple fiber lines using V-grooved fiber arrays and multicore fibers. Therefore, the properties of the elephant couplers mentioned above will be promising to increase the bandwidth of silicon photonics using wavelength division multiplexing and space division multiplexing in cost-effective manufacturing.

In our latest fabrication we realized an elephant coupler with a 2.5 dB coupling loss at 1550 nm wavelength and a 1 dB bandwidth of 130 nm for optical fibers with a mode-field diameter (MFD) of 5 μm by incorporating an reversed taper of Si vertically curved waveguide (VCW) for SSC and a SiO2 dome for a light collimating lens. These properties seem to be promising for practical applications if fabrication accuracy and reproducibility are realized. For optical fibers with a MFD of 5 μm, assembly tolerance of alignment positions between elephant couplers and centers of fiber cores is estimated to be ±0.5 μm. This tolerance requires the fabrication accuracy and reproducibility of ±0.5 μm for the elephant coupler positions.

In the fabrication of elephant couplers, silicon waveguides are bent vertically by the ion implantation bending (IIB) method. In this method, stress generation and relaxation in the Si waveguide cantilever suspended in free space become the driving force of bending.9–15 The bending occurs only in the implanted and suspended region and the bending structure is very sensitive to the length of this region. However, in the IIB process,10–20 isotropic wet etching required for cantilever formation can only guarantee uniformity and reproducibility on the order of micrometers. Therefore, it is challenging to achieve the requirement. In this work, we developed a high accuracy IIB method by using a metal mask that can partially shield the ion implantation with dry etching-level fabrication accuracy.

Figure 1(a) shows the original scheme of the IIB method of Si wire for optical waveguide formed from Si on insulator (SOI) wafer as an example. First, the end of the Si waveguide is suspended freely as a cantilever structure; then, ions are implanted from the vertical direction, and the cantilever structure is bent vertically. The process will be described in detail later, but we should note here that the cantilever structure is fabricated using the isotropic wet etching process, and the bending structure is sensitive to the length of the ion-implanted region that is equivalent to undercut length. To obtain the VCW fabrication with high uniformity and reproducibility, we desire control undercut length with high accuracy on the order of 100 nm. The wet etching process, however, cannot satisfy this 100 nm scale accuracy requirement, and the development of a method that can achieve this level of accuracy was thus needed.

We explain the necessity for isotropic etching that causes the problem for the IIB inaccuracy. In the IIB process, the thin layer that has several hundred nanometers thickness can be bent by stress generation and relaxing during the ion
implantation. During the IIB process, the influence of the ion implantation stress on the depth direction depends on the ion species and ion energy, which is only about a hundred of nanometers within the energy of about a hundred keV to form Si-VCW. Therefore, to bend the Si waveguide that has about two hundred nanometers thick, it must be separated from the substrate and must be in the form of a cantilever structure. To form Si waveguide cantilever formation, the isotropic etching process is required to remove the material around the Si waveguide. In the case of the Si-PICs, the isotropic etching with the hydrofluoric acid solution that is widely used in MEMS processing\textsuperscript{21}) is appropriate to remove the SiO\textsubscript{2} for the cladding layer which around the Si waveguide without damaging the Si cantilever layer.

The inaccurate nature of the undercutting caused by isotropic wet etching under the photoresist mask, as shown in Fig. 1(a), affects the uniformity and reproducibility of the shape of the VCW to an unacceptable level of optical coupler applications. When ion implantation is performed on such cantilevers, the VCWs are formed with inaccurate. The tip position, orientation, and radius of curvature of the VCW are all dependent on the length of the cantilever because the undercut termination position defines the starting position of the bending process.

To overcome this issue, we have developed a high accuracy IIB that uses a hard mask, as shown in Fig. 1(b). Because the hard mask blocks the irradiated ions, partial control of the ion irradiation region of the cantilever becomes possible. When the hard mask is processed via anisotropic dry etching, which can accurately carry out patterning of the order of 100 nm or less, the bending process produced by ion implantation can thus be controlled on a scale of 100 nm or less, irrespective of the variations in the isotropic wet etching.

The mask material must satisfy the following three conditions. (1) The ion implantation process must not bend the hard mask itself to ensure that the patterning accuracy is not reduced. This means that keeping the ion implantation depth into the mask layer below about 10%. In this condition, the bending effect hardly occurs, as shown in previous paper.\textsuperscript{16}) Thus the mask material must be heavy material and/or thick-layer. (2) In many cases, SiO\textsubscript{2} is useful as a sacrificial layer for cantilever formation and cladding layer for Si-PICs; the mask material must be resistant to the hydrofluoric acid solution that removes the SiO\textsubscript{2} layer to form the thin layer cantilever. (3) The mask material must also be compatible with CMOS manufacturing technology to reap the benefits of this technology. As a result of consideration of materials that may be suitable and meet the three conditions above, copper (Cu) and tungsten (W), which are used in wiring and plug of conventional CMOS processes, respectively, are the first candidates to be considered. In this work, we have selected the W layer as a mask material because W is easier to handle in our lab-line, and have demonstrated high accuracy IIB.

We have demonstrated the effectiveness of the use of the metal mask experimentally. Si waveguides (220 nm thick, 430 nm wide) on the SiO\textsubscript{2} layer were patterned with ArF-immersion lithography, which brought high uniformity as experimental samples. After SiO\textsubscript{2} deposition for cladding layer (1 \(\mu\)m thick) and dicing the wafer into 20 mm square chips, a 200 nm thick W layer was deposited on the SiO\textsubscript{2} layer by CVD and patterned with an i-line stepper and reactive ion etching. Then, parts of the upper and lower SiO\textsubscript{2} layers were removed by isotropic wet etching using a hydrofluoric acid solution to form the Si waveguide cantilever. We intentionally changed the undercut length by using wet etching times of 32, 35, and 38 min. In the case of the SiO\textsubscript{2} layer used in this experiment, a difference of 6 min corresponds to a difference of about 1 \(\mu\)m of the undercut length. Ion implantation was performed on the three chips for each of the different undercut lengths.

![Fig. 1. (Color online) Cross-sectional schematic illustrations of (a) original scheme for Si vertically curved waveguide fabrication and (b) developed scheme. And typical SEM images of the Si vertically curved waveguide obtained using W mask (c) before and (d) after W hard mask removal.](https://example.com/fig1.png)
Fig. 2. (Color online) Tip positions of the Si vertically curved waveguides with and without the W mask.

under the same conditions, and the shapes of the resulting vertically curved Si waveguide were observed by a scanning electron microscope (SEM).

Figures 1(c) and 1(d) show typical SEM images of the Si-VCW before and after the removal of the W mask. These images show that the metal mask blocks the irradiated ions and the Si cantilever can be bent at a starting point at which the extended line of the overhanging W layer end intersects with the Si cantilever. Figure 2 shows the results of measuring 16 Si-VCWs tip positions from every three samples. The plots are normalized to the average of the 35 min results. The difference of the tip position using the W mask plotted in the red circle is about less than ±0.4 μm in the x-direction and ±0.2 μm in the y-direction. On the other hand, in the sample without a W mask, the difference of the tip position plotted in the black square is about more than ±1 μm in the x-axis and about ±1 μm in the y-axis. In this experiment, because the length of the cantilever differs by about 1 μm, the positions of the tips of the curved shapes varied on the order of microns. These results clearly show that in the absence of a W mask, micron-order variations occur depending on the undercut variation, and in the presence of a W mask, the variations can be suppressed to the submicron level.

The metal hard mask separated from the silicon waveguide by the 1 μm thick cladding layer does not affect the optical propagation characteristics of the waveguide. The optical coupling of the fabricated elephant couplers showed promising characteristics.14,15

Finally, we discuss the practical process integration of the developed metal mask process with Si-PICs. In this work, since the W layer is easy to be processed in our lab-line, we used W mask patterned by dry etching. However, in the Si-PIC process based on the standard CMOS manufacturing, this is not a standard method in using W. In the Si-PIC process, the practical material candidates for the hard mask are Cu and W, as mentioned above. Usually, Cu and W are used to form the wire and plug via structures that electrically connect optical modulators and/or detectors. They have been patterned using chemical mechanical polishing (CMP) known as “damascene.” In the damascene process, the trenches or via holes are formed by dry etching, and thus Cu or W patterning maintains the dry etching patterning accuracy even when CMP is used. Therefore, the fabrication accuracy of the hard mask will also be maintained. If Cu wiring and/or W plug processes are included as part of the Si-PIC fabrication, the hard mask layer for the IIB method would be formed simultaneously with only minor revision of the Si-PIC process. In this way, we will be able to integrate the IIB method with Si-PICs.

In summary, to obtain high uniformity and reproducibility of the IIB process for vertically curved Si optical couplers, we developed a high accuracy IIB that incorporates a metal hard mask to shield the ion implantation process partially. This method enables an excellent position definition of the bending origin with dry etching-scale fabrication accuracy of several 100 nm order. Such a high accuracy of the developed IIB process can meet the requirements of submicron alignment in optical coupler applications. Furthermore, the developed process has high versatility, so it would be used for electronic device fabrication that needs three-dimensional structures such as field emitter emitter.22

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