Quantum Annealing Machine based on Floating Gate Array

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Quantum annealing machines based on superconducting qubits, which have the potential to solve optimization problems faster than digital computers, are of great interest not only to researchers but also to the general public. Here, we propose a quantum annealing machine based on a semiconductor floating gate (FG) array. We use the same device structure as that of the commercial FG NAND flash memory except for small differences such as thinner tunneling barrier. We theoretically derive an Ising Hamiltonian from the FG system in its single-electron region. Recent high-density NAND flash memories are subject to intrinsic obstacles that originate from their small FG cells. In order to store information reliably, the number of electrons in each FG cell should be sufficiently large. However, the number of electrons stored in each FG cell becomes smaller and can be countable. So we utilize the countable electron region to operate single-electron effects of FG cells. Second, in the conventional NAND flash memory, the high density of FG cells induces the problem of cell-to-cell interference through their mutual capacitive couplings. This interference problem is usually solved by various methods using software of error-correcting codes. We derive the Ising interaction from this natural capacitive coupling. Considering the size of the cell, 10 nm, the operation temperature of quantum annealing processes is expected to be approximately that of a liquid nitrogen. If a commercial 64 Gbit NAND flash memory is used, ideally we expect it to be possible to construct 2 megabytes (MB) entangled qubits by using the conventional fabrication processes in the same factory as is used for manufacture of NAND flash memory. A qubit system of highest density will be obtained as a natural extension of the miniaturization of commonly used memories in society.

I. INTRODUCTION

Artificial intelligence (AI), whose progress is a momentous trend in science and technology, is expected to lead to drastic changes in society. Faster solving of combinatorial optimization problems is a prerequisite for efficient development of AI algorithms such as machine learning algorithms. A quantum annealing machine (QAM) is expected to solve the combinatorial optimization algorithms of NP-hard problems in a shorter time than is possible with classical annealing methods. Nishimori et al. developed the theoretical foundation of the QAM\(^\text{\ref{1}}\), and QAMs based on superconducting circuits are widely used\(^\text{\ref{2,3}}\).

NP-hard problems such as the traveling salesman problem can be mapped to the problems to find ground states of the Ising Hamiltonian, expressed by\(^\text{\ref{2}}\):

\[ H = \sum_{i<j} J_{ij} s_i^x s_j^x + \sum_i h_i s_i^z, \]  

(1)

where the variable \(s_i\) is a classical bit of two values (\(s_i = \pm 1\)). The first term is the interaction term with a coupling constant \(J_{ij}\), and the second term is the Zeeman energy with an applied magnetic field \(h_i\). This classical Ising machine has already been realized by a conventional semiconductor memory\(^\text{\ref{4}}\). In the case of a quantum annealing machine, a tunneling term is added and expressed by

\[ H = \sum_{i<j} J_{ij} \sigma_i^x \sigma_j^x + \sum_i [h_i \sigma_i^z + \Delta_i(t) \sigma_i^z] \]  

(2)

where the variables are expressed by Pauli matrices \(\sigma_i^\alpha\) \((\alpha = x, z)\) instead of digital bits. The tunneling term is controlled such that it disappears at the end of the calculation, given by

\[ \Delta(t \to \infty) \to 0. \]  

(3)

The Hamiltonian \(\text{\ref{2}}\) can be found in many physical systems in nature. To use physical systems as QAMs, the tunneling term and the Ising term should be controlled separately and locally by electric gates. The development of QAMs based on superconducting qubits has advanced the furthest\(^\text{\ref{3}}\). The advantage of superconducting qubits lies in the long coherence time of superconducting states.

Let us consider the possibility of constructing QAMs based on semiconductor devices. The greatest advantage of using semiconductor devices is that the smallest artificial structures at the highest density can be manufactured in factories. Obviously, the competitor of the QAM is the conventional digital computer. For the QAM to prevail, integration of a huge amount of cell is unavoidable. During the past 20 years, many qubits based on semiconductor devices have been investigated\(^\text{\ref{5,6}}\). In quantum computation, accurate control of wave functions is required from initial states to final states for measurements. Because it is not easy to precisely control the wave functions of electrons and spins in semiconductor devices, even two-qubit logic operation has been proven only recently\(^\text{\ref{7}}\). Moreover, it is known that the coherence times of charge qubits are shorter than those of spin qubits. On the other hand, in the quantum annealing machine, the condition of the strict control of wave functions can be loosened provided that the final state is an eigenfunction of the target Hamiltonian, and the intermediate processes can include disturbance with several kinds of noise. Thus, we can exploit the advantages of...
Here, we propose a QAM using the conventional NAND flash memory consisting of floating gate (FG) cells. NAND flash memory has a dominant share of the growing market for storage applications extending from mobile phones to data storage devices in data centers. The NAND flash memory has the advantages of high-density memory capacity and low production cost per bit with low power consumption and high-speed programming and erasing mechanisms. Data storage of personal computers is also transitioning from hard disk to flash memory. An FG cell corresponds to 1 bit for a single level cell type and m bit for a multi-level type. Each FG is typically made of highly doped polysilicon and placed in the middle of a gate insulator of a transistor. If there is no extra charge in an FG, the cell behaves like a normal transistor. In the programming or writing step, electrons are injected into the FG by applying voltage to the control gate. In the erasing step, electrons are ejected from the FG to the substrate by applying voltage to the back gate. The amount of the charge of FG determines the threshold voltage above which the current between the source and drain changes. In NAND flash memories, the FG cells are connected like a NAND gate. In general, the distance between the FGs is of the same order as the size of FG, resulting in high-density memory. For example, Sako et al. developed 64 Gbit NAND flash memory in 15 nm CMOS technology, which is organized by a unit of 16KB bit-lines × 128 word-lines. This means that the number of closely arrayed FG cells in a single unit is 16KB×128≈2MB. The integration and miniaturization of flash memory cells have progressed continuously and the current flash memories have stacked 3D structures using trapping layers.

We theoretically prove that a two-dimensional (2D) FG array can be used as a QAM. The QAM proposed here has the structure shown in Fig.1. The FG cells are capacitively connected to each other, which is the same arrangement as that in a commercial flash memory. The fundamental idea is that we will be able to regard a small FG cell in the single-electron region as a charge qubit. Now the size of the NAND flash memory is 15 nm, and the size can shrink to beyond 7 nm. In the flash memory with 15 nm cell, single-electron effects can be observed at room temperature. When the doping concentration of electrons is 10²⁰ cm⁻³, the number of electrons in a volume of 15×15×50 nm³ is about 1125 and countable. Once we can control the single-electron effects, we can realize a two-level system by using a crossover region between two different quantum states with different numbers of electrons, following such as Ref.

The distance between FG cells is of the same order as the size of FG cells in conventional NAND flash memories. Thus, the capacitive coupling cannot be neglected. The changes of electrostatic potentials of neighboring cells affect the electronic static potentials of target FG cells. In regard to the conventional use of the memory cell, these capacitance couplings between FG cells are undesirable. In the conventional NAND flash memories, this effect is alleviated by computer software of various error-correcting codes. But, here we use this coupling as the interaction between quantized cells. We derive the Ising interaction term and the Zeeman term in Eq. from a simple capacitance network model.

In the conventional usage of FG memory, the gate voltage is applied either positively or negatively corresponding to WRITE (programming data) and ERASE (erasing data) processes, respectively. Thus, in order to realize the tunneling between the FG cells and the substrate in both directions, both gate electrode and substrate have the same voltage whereas the voltage of FG should be low. By controlling the voltages, we realize the third term of Eq. This QAM has two major structural differences compared with conventional FG memories. The first major difference is that the tunnel barrier between FGs and substrate in the present proposal is thinner than that of the commercial FG array, in order to realize the bidirectional tunneling. The second major difference is that we do not use the air-gap between FG cells in order to increase the electrostatic coupling between FG cells.

Semiconductor devices consist of many different regions on the substrate. There are several doping concentrations with n-type and p-type semiconductors. The conventional FG devices are based on the silicon transistor with additional floating gates. Thus, there are several regions with different electrostatic potentials. It is necessary to investigate how the above-mentioned idea can be implemented in a realistic potential profile. Here, we use a technology computer aided design (TCAD) tool to check whether we can generate the desired potential profile of tunneling within an appropriate voltage region. Although this simulator does not include the single-electron effect and we provide results of coupling three cells, we can sketch a rough engineering drawing in a realistic situation.
The great advantage of using semiconductor devices instead of superconducting devices is that they are the smallest structures that humans can reliably integrate in Gbit order. Our proposed QAM will be able to be fabricated using a mask set and a product line that are almost same as those used for the conventional NAND flash memory. We believe that integration capabilities backed by mass-production technologies will eventually lead to quantum computers that are far more controllable than those available today. This QAM will be of far more benefit than QAMs without commercial antecedents in mass-productions, because the progress from fundamental science to a commercial product involves a huge cost and time.

This paper is organized as follows: In Sec. II we briefly review an implementation of a QAM for a 2D qubit array. In Sec. III we explain the basic idea of how to implement QAM into an FG array. In Sec. IV we derive an Ising Hamiltonian from an FG array. In Sec. V we present the results of TCAD simulation based on realistic FG sizes. In Sec. VI we discuss the noise and decoherence problem of our QAM. In Sec. VII we discuss the possibility of high-frequency operation. We close with a summary and conclusions in Sec. VIII. Additional information is presented in the Appendix.

II. HOW TO CONSTRUCT QAM IN 2D NAND FLASH MEMORY STRUCTURE

The simpler the structure and mechanism, the greater is the reduction in variations among cells, and the more stable the operations become. Thus, in order to realize a reliable large-scale QAM, the structure and mechanism should be as simple as possible. For the simplest QAM, the coupling $J_{ij}$ has a fixed value determined by its cell structure. The typical optimization problem with a fixed $J_{ij}$ is the MAX-CUT problem $^{25,26}$. The MAX-CUT problem is given as follows: Given a graph $G(V,E)$, $|V|=n$ with weights $J_{ij}$ for all $(i,j) \in E$, the max-cut is a problem of finding $S \subseteq V$ such that the cut $S \setminus V \setminus S$ is the maximum. Introducing the variables: $s_i = 1$ if $i \in S$, $s_i = -1$ if $i \in V \setminus S$. The max cut problem can be expressed as finding the minimum of the Ising model of $\sum_{i<j} J_{ij} (s_i s_j - 1)$ under a constraint of $s_i^2 = 1$ for $i = 1, ..., n$. The MAX-CUT problem $^{25,26}$ is applied to the noise reduction problem $^{8}$. On the other hand, in general, the values of the coupling $J_{ij}$ are chosen depending on each optimization problem $^{6}$. For example, in the traveling salesman problem, $J_{ij}$ are taken as the distances between two cities $^{6}$. Thus, there is a trade-off between the range of application and the simplicity of device structure. Here, we consider a QAM whose coupling $J_{ij}$ is determined by the capacitive coupling between two FG cells. Because the distances between FG cells are all the same, a fixed value of $J_{ij}$ is provided in our system in its original condition. Note that this limitation can be resolved and arbitrary variable of $J_{ij}$ can be realized by applying high-frequency electric fields as shown in Ref. $^{27}$. Because we would like to present the fundamental proposal of QAM based on FG arrays, we will concentrate on our QAM for a conventional operation region of the fixed $J_{ij}$.

In addition, we consider a 2D planer FG array. In order to solve general problems in the QAM, all connections between two cells are required $^{28}$. This means that the coupling $J_{ij}$ should be formed in any two cells. A coherent Ising machine $^{29,30}$ can realize this situation by using optical systems. Because the connections between solid-state cells are fixed, it is not possible to directly connect two arbitrary cells in solid-state circuits with minimum distances. If we apply the methods proposed in Ref. $^{25,26}$, we can implement connections between distant qubits. We can also use the advantage of conventional circuits, i.e., we can implement digital circuits for connecting distant FG cells similar to Ref. $^{6}$. In this case, there is no quantum coherence between digitally connected FG cells. Although the speed up is less than that of a fully quantum-connected QAM, it is still expected to operate in the partial quantum regions.

Let us think about using the lithography mask set of the conventional NAND flash memory of Ref. $^{31}$. The "page" in NAND flash memory corresponds to the number of the digital bits in the bit-line. Because Ref. $^{31}$ has 2 bits per cell, the number of connected FG cells in the direction is 128 and one block consists of $16KB \times 128 = 16384 \approx 2MB$ cells. These blocks are digitally connected and form the single plane of the memory. This means that the coupling $J_{ij}$ exists between nearest neighboring 2MB cells. Thus, ideally, 2MB FG charge qubits form an entangled state. By connecting the blocks digitally, we would be able to realize a quantum annealing machine like that of Ref. $^{6}$. Hereafter, we would like to prove that the 2D FG cell array realizes the Ising Hamiltonian with the fixed $J_{ij}$. The digital connection and concrete application to annealing problems are beyond the scope of this paper.

III. BASIC IDEA OF QAM BASED ON FG ARRAY

We would like to conceptually explain how to realize a QAM in the conventional FG structure.

A. Floating gate cell

First, let us consider the single-electron effect in FG cells. The basic physics of the FG cell can be explained by the simple model of series of capacitance depicted in Fig. 2 given by $^{34}$

$$Q = C_D(V_{FG} - V_{sub}) - C_A(V_{CG} - V_{FG}), \quad (4)$$

where $Q$ is a charge stored in the FG, $V_{CG}$, $V_{FG}$ and $V_{sub}$ are potential energies of the control gate(CG), FG, and
substrate, respectively. From Eq. (1), we have

$$V_{FG} = \frac{Q}{C_A + C_B} + \frac{C_AV_{CG} + C_BV_{sub}}{C_A + C_B}.$$  (5)

This equation shows that the FG potential energy $V_{FG}$ is determined by the charging energy of FG (1st term of the right side of the equation) and the controllability of CG and substrate. When the capacitance $C_{\text{eff}} \equiv C_A + C_B$ is sufficiently small, the change of the number of single electrons $Q \pm e$ can be detected if $e/C_{\text{eff}}$ is larger than the operation temperature $T$. If we simply express $C_{\text{eff}} = \epsilon_{\text{ox}} S/d_{\text{ox}}$, where $\epsilon_{\text{ox}}$, $S$, and $d_{\text{ox}}$ are the dielectric constant of a tunneling oxide SiO$_2$, the area, and the thickness of the capacitor, and use the value of $\epsilon_{\text{ox}} = 3.9 \times 8.854 \times 10^{-21}$ F/nm, $S = 15 \times 15$ nm$^2$, and $d_{\text{ox}} = 3.5$ nm, we have the voltage shift, $e/C_{\text{eff}} = 0.00721$ eV, by the change of a single electron (The Boltzmann constant $k_B = 8.617 \times 10^{-5}$ K/(eV) is used.) Thus, the single-electron effect will be detectable. Because the single-electron region can be used to construct a two-level system as Makhlin et al. showed, the small size of the FG gate array allows construction of a two-level system, which is quantitatively discussed in the next section.

As in the field of FG memory, we define a coupling ratio $CR$ defined by

$$CR = \frac{C_A}{C_A + C_B},$$  (6)

as an indication of the degree of controllability of the gate electrode. We also assume that the capacitance is represented by a simple parallel plate capacitor such as

$$C_A = \epsilon_A LW/d_A, \quad C_B = \epsilon_{\text{ox}} LW/d_{\text{ox}},$$  (7)

where $L$ and $W$ are the length and width of the FG cell, $d_A$ and $d_{\text{ox}}$ are the thickness of tunneling oxides, and $\epsilon_A$ and $\epsilon_{\text{ox}}$ are dielectric constants. Then, when $d_{\text{ox}}$ and $CR$ are given, $d_A$ is given by $CR$ and $d_A$ is given by

$$d_A = \frac{1.0 - CR \epsilon_A}{CR \epsilon_{\text{ox}}} d_{\text{ox}}.$$  (8)

B. Interaction between FG cells

In commercial 2D NAND flash memories, the distance between FG cells is of the same order as the size of the FG cells. Thus, the interference effects between FG cells are one of the major issues in NAND flash memories. In order to reduce the interference between FG cells, the air-gap technologies are used, because the dielectric constant of air is smaller than that of the tunneling oxide such as SiO$_2$ (whose dielectric constant is 3.8). However, here we use SiO$_2$ between FG cells to increase the electrostatic coupling between FG cells.

C. Tunneling

In the conventional FG memory, tunneling phenomenon of electrons is used for WRITE and ERASE processes of data by biasing the voltage between the gate and substrate electrodes. However, in the conventional WRITE and ERASE processes, electron flow is unidirectional as shown in Figs. (a) and (b). In the case of a QAM, electron tunneling should be bidirectional between the FG and substrate. Bidirectional tunneling occurs when we lower the potential of the interface between the FG and substrate. This situation will be realized by biasing the gate and substrate electrodes compared with the source and drain as shown in Fig.

FIG. 2: A single cell of the floating gate (FG) array. Charges are stored in the FG. The charges $Q$ and the potential of the FG, $V_{FG}$, are controlled by the control gate (CG) voltage, $V_{CG}$, and the substrate voltage $V_{sub}$.

D. FG array

Figure shows a schematic of a 2D FG cell array. The FG cells are coupled capacitively with each other in both word and bit directions. The source and drain are attached to the both ends of bit-lines. When we look at each bit-line, biases are applied to the source and drain as well as to the gate. Thus, the regions between FG cells in the bit-line are in electronically floating states. In order to switch on the tunneling of all FG cells at once, we will have to apply higher gate voltage to the cells far from the source and drain.
FIG. 3: Conventional process of writing data ((a)) and erasing data ((b)). In the conventional FG array, the tunneling oxide is thick (∼7 nm), and a large voltage (∼20 V) is applied.

FIG. 4: Proposed idea for both bidirectional electron tunneling. The voltages of the gate and substrate are raised compared with the voltages of the source and drain. The tunneling rate is controlled by the relative potential between the gate/substrate and the source/drain.

IV. DERIVATION OF QAM HAMILTONIAN FROM FG ARRAY

Here, we derive the Ising Hamiltonian from the FG array described in Fig. 1 by using a capacitance network model (Fig. 6). The charging energy is reduced to the 1st and 2nd term of Eq. (4). The last term of Eq. (2) is derived from tunneling of carriers between FGs and substrate. We assume that the FG cells are sufficiently small that the single-electron effects is observable. The Coulomb interaction between the charges of neighboring FG cells. Usually this interference effect is an obstacle to the conventional flash memories. But here we can use it effectively for the cell-to-cell interaction.

A. Ising interaction parts and Zeeman energy

Here, we derive the 1st and 2nd term of Eq. (2) by describing the FG cells using the capacitance network model described in Fig. 6

1. Analytical formation of Ising interaction parts and Zeeman energy

The charging energy of M FG cells is expressed by

\[ U = \frac{1}{2} \sum_{i=1}^{M} \left[ \frac{q_{A_i}^2}{C_{A_i}} + \frac{q_{B_i}^2}{C_{B_i}} + \frac{q_{D_i}^2}{C_{D_i}} + \frac{q_{E_i}^2}{C_{E_i}} + \frac{q_{F_i}^2}{C_{F_i}} + \frac{q_{H_i}^2}{C_{H_i}} + \frac{q_{D_0}^2}{C_{D_0}} \right] - \sum_{i=1}^{M} \left[ (q_{A_i} + q_{E_i} + q_{F_{M-i}}) V_{CG_i} + q_{B_i} V_{sub} + q_{H_i} V_{st} + q_{D_i} V_{dt} \right], \]  

(9)

where \( q_{E_{M+1}} = q_{E_{M+1}} = 0 \), and \( V_{di} = V_{i+1} \). The number of charges \( n_i \) in the \( i \)-th FG is given by

\[ n_i = -q_{A_i} - q_{B_i} - q_{D_i} - q_{E_{i-1}} - q_{F_i} - q_{H_i} - q_{D_0}, \]  

(10)

where \( q_{D_0} = q_{E_0} = 0 \). The capacitances are defined by

\[ C_D = \epsilon_{ox} Z_{FG} W / X_D, \quad C_E = \epsilon_{ox} (L W / 2) / X_E, \]  

\[ C_H = \epsilon_{ox} (L W / 2) / X_H, \]  

(11)

(12)

with \( X_E = \sqrt{(L / 2)^2 + d^{2}_{ox}} \) and \( X_H = \sqrt{(L / 2)^2 + d^{2}_{ox}} \). For simplicity, from now on we formulate a case of three cells. The charge distribution is obtained after mini-

FIG. 6: The capacitance network model of three floating gate (FG) cells. The electronic states are controlled by the control gate (CG), substrate, source and drain voltages. The width (or depth) of each FG cell is assumed to equal its length, \( L \), and the distance between two FG cells also equals \( L \).
Lagrange multipliers minimizing the capacitance energy by using the method of the single-electron effect can be controlled or not. See Fig. 9.

indicates a typical scale by which the single-electron effect can be observed or not. $U_h$ indicates a typical scale by which the single-electron effect can be controlled or not. See Fig. 8.

mizing the capacitance energy by using the method of Lagrange multipliers and given by

\[
U = \sum_{i=1}^{2} \left[ \frac{1}{2C_{a_i}} \left( 1 + \frac{C_D}{C_{a_i}C_{a_{i+1}}} \right) (n_i + Q_{v_i}^0)^2 \right] + \frac{1}{2C_{a_3}} (n_3 + Q_{v_3}^0)^2 - \sum_{i=1}^{3} \frac{W_i}{2} + \sum_{i=1}^{2} \frac{C_D}{4C_{a_i}C_{a_{i+1}}} (n_i + Q_{v_i}^0)(n_{i+1} + Q_{v_{i+1}}^0). \tag{13}
\]

We consider a Coulomb blockade regime where the number of electrons can be controlled such that we can define a quantum state $|n_i\rangle$ by the number of electrons $n_i$ in $i$-th FG as shown in Fig. 7. The superposition state is constituted by the coupling region of $|n_i\rangle$ and $|n_i\pm 1\rangle$, which is realized when the parabolic charging energy of $|n_i\rangle$ state crosses that of $|n_i + 1\rangle$ state as discussed in Ref. 23. The crossover point where the charging energy of $n_i$ electrons equals that of the $n_i + 1$ electrons is given by

\[
(n_i + Q_{v_i}^0)^2 = (n_i + 1 + Q_{v_i}^0)^2. \tag{14}
\]

When we define an effective gate voltage $n_{G_i}$ given by

\[
n_i + Q_{v_i}^0 = n_{G_i} - 1/2, \tag{15}
\]

then, the crossover point is given by $n_{G_i} = 0$ and the superposition state is constituted around $n_{G_i} \ll 1$. $n_{G_i}$ accounts for the effect of the gate voltage of the $i$-th cell.

Thus, the charging energy term as a function of $n_{G_i}$ is transformed to

\[
U = \sum_{i=1}^{3} h_i \sigma_i^z + \sum_{i=1}^{2} J_{ij} \sigma_i^z \sigma_{i+1}^z + \text{Const}, \tag{16}
\]

where

\[
h_i = \frac{1}{2C_{a_i}} \left[ 1 + \frac{C_D^2}{C_{a_i}C_{a_{i+1}}} \right] n_{G_i} + \frac{C_{D_{i+1}} n_{G_{i+1}} + C_{D_{i}} n_{G_{i+1}}}{2C_{a_i}C_{a_{i+1}}}, \tag{17}
\]

\[
h_3 = \frac{1}{2C_{a_3}} n_{G_3} + \frac{C_{D_2}}{2C_{a_2}C_{a_3}} n_{G_2}, \tag{18}
\]

\[
J_{ij} = \frac{C_{D_{i}}}{4C_{a_i}C_{a_j}}, \tag{19}
\]

and

\[
\sigma_i^z = |n_i\rangle \langle n_i + 1| + |n_i + 1\rangle \langle n_i|, \tag{20}
\]

\[
\sigma_i^z = -|n_i\rangle \langle n_i| + |n_i + 1\rangle \langle n_i + 1|, \tag{21}
\]

\[
I_i = |n_i\rangle \langle n_i| + |n_i + 1\rangle \langle n_i + 1|. \tag{22}
\]

(Details of the definitions and derivations are noted in the Appendix). We can define a height of charging energy $U_h$ as the coefficient of $n_{G_i}$ in Eq. (17) and $U_w$ given by

\[
U_h \equiv \frac{1}{8C_{a_i}} \left[ 1 + \frac{C_D}{C_{a_i}C_{a_{i+1}}} \right] \tag{23}
\]

$U_w$ is defined by a voltage difference of the parabolas for $n_i$ and $n_i + 1$. When we see $Q_{v_i}^0$ as a function of the gate voltage $V_{CG}$, we obtain $U_w = e/C_A$ from two equations of $n_i + Q_{v_i}^0 (V_{CG}) = 0$ and $n_i + 1 + Q_{v_i}^0 (V_{CG} + U_w) = 0$.

When the quantum computations, such as Grover’s algorithm, are carried out, we have to maintain the electronic system in the range of its two-level system. For that purpose, we have to maintain the superposition state between $|n_i\rangle$ and $|n_i+1\rangle$ in the present setup, and we have to take care such that $|n_i-1\rangle$ or $|n_i+2\rangle$ states do not affect the target quantum operations, when we apply the gate and substrate bias beyond $U_w$. In contrast, the purpose of the quantum annealing process is to finally obtain the $n_{G_i} = 0$ state. Thus, as long as we can restore the point of $n_{G_i} = 0$, we can apply the gate and substrate bias beyond $U_w$.

2. Numerical estimation of charging part

Figure 8 shows an example of the numerical calculation of the charging energy of three coupled FG cells for $CR = 0.3$ and $L = 15$ nm with $V_{CG3} = V_{CG1}$. In order to experimentally observe single-electron effects, the charging energy should be sufficiently large to be observed at the operation temperature. It is found that smaller $CR$ is better for increasing charging effects. Each parabola has its own electronic state of a fixed $n_i$. Where two parabolas cross, the charging energies of different numbers of electrons cross as shown in Eq. (14). Figure 9 shows $U_h$ and $U_w$ as functions of the size of FGs with various parameters of the thickness of the tunneling barrier $d_{ox}$. $U_h$ indicates a metric of charging energy, and therefore, $U_h$ is described as a unit of temperature in Fig. 9. $U_w$ indicates a metric of gate controllability, and therefore, $U_w$ is described as a unit of voltage in Fig. 9.
From Figs. 9 it can be seen that a smaller FG is better for a larger charging energy as expected. It is also found that thicker $d_{ox}$ is desirable. Comparison of Fig. 9 (a) and Fig. 9 (b) reveals that smaller height of FG is better for higher temperature operations.

Figure 10 shows $J$, Eq. (19), as a function of the size of the FG. As the size $L$ becomes larger, the magnitude of $J$ becomes smaller. It can also be seen that the larger $d_{ox}$ is better for larger $J$. This is because the larger $d_{ox}$ induces a larger area of Coulomb interactions with their neighboring FGs.

![FIG. 8: Numerical calculation of the charging energy Eq. (16) of three FGs for $V_{CG3} = V_{sub} = V_{CG1}$ and $V_{si} = 0$ ($i = 1, ... , 4$). The electron density of the FG is $10^{20}$ cm$^{-3}$. The size of FG is $L = W = 10$ nm, the height of FG is $Z_{FG} = 100$ nm. The thickness of tunneling oxide is $d_{ox} = 3.5$ nm, and the thickness of the control gate oxide is $d_A = 8.2$ nm. The coupling ratio is 0.3.](image)

![FIG. 9: $U_h$ and $U_w$ that determine the single-electron effect (Fig. 2) are calculated as a function of the size of FGs. (a) $U_h$ for $Z_{FG} = 10$ nm. (b) $U_h$ for $Z_{FG} = 100$ nm. (c) $U_w$ for $Z_{FG} = 10$ nm. (d) $U_w$ for $Z_{FG} = 100$ nm. The thickness of the control gate oxide depends on $d_{ox}$ by the coupling ratio $CR = 0.3$.](image)

![FIG. 10: The coupling $J$, Eq. (19), as a function of the size of FGs in which the width of FGs equals $L$. The vertical axis is described by a unit of temperature. (a) The height of FG is 10 nm and (b) 100 nm. The thickness of the control gate oxide depends on $d_{ox}$ by the coupling ratio is $CR = 0.3$.](image)

![FIG. 11: The magnitude of tunneling, Eq. (21), as a function of the size of FGs. (a) The height of FG is 10 nm. (b) The height of FG is 100 nm. The coupling ratio is $CR = 0.3$. We use $1$eV$=2.41799 	imes 10^6$ Hz.](image)

### B. Derivation of tunneling part

#### 1. Analytical formation of tunneling term

Here, we derive the tunneling term in Eq. (2) by using the WKB approximation as shown in Ref. [38]. The tunneling term is expressed in the form of annihilation operators and given by

$$
\sum_{k,k'} \Delta_{k,k'} c^\dagger_{kR} c_{kL} \approx v^2 \int \frac{d^3k d^3k'}{(2\pi)^6} \frac{h^2 k_x}{2m_0 L} e^{-\int k_x(x)dx} \int_{k_{F}}^{k_{F}'} \frac{d^3k_x}{(2\pi)^3} c^\dagger_{kR} c_{kL}
$$

$$
= N_L N_R \frac{m_0 R_y}{m^*_s} \left[ \frac{\pi \alpha_0}{L} \right]^2 e^{- \frac{d_{ox}}{m_0} \sqrt{\frac{m_0 V_{ox} - E_F}{m_0 \alpha_0}}} \int_{k_{F}}^{k_{F}'} c^\dagger_{kR} c_{kL}
$$

(24)

where $V_{ox}$ is the potential height of the tunneling barrier, $m^*_s = 0.19 m_0$ and $m^*_ox = 0.5 m_0$ are the effective masses of electrons in Si and tunneling barrier, respectively ($m_0$ is an electron mass in vacuum). $c_{kL}$ and $c_{kR}$ are annihilation operators of both sides of the tunneling barrier. $k_F$ is a wave vector at a Fermi energy. $\alpha_0 \approx 0.0529$ nm is the Bohr radius and $R_y \approx 13.6$ eV is the Rydberg constant. $v$ is a volume of tunneling electrons, and $N_L, N_R$ are the numbers of electrons of the two sides of the tunneling barrier, respectively, which participate in the tunneling event, given by

$$
N_L = N_R = v \sum_k 1 = v \int dk_y dk_z k_Z / (2\pi)^3.
$$

(25)
This tunneling term is a function of the gate voltage \( V_{CG} \) through the shift of Fermi energy \( E_F \) such as \( E_F = E_F + V_{CG} \), and \( E_F \) is calculated by the FG doping concentration for which we use 10\(^{20} \) cm\(^{-3} \). When \( E_F \) increases, the effective tunneling barrier is lowered and the tunneling rate increases (switch on). Conversely, when \( E_F \) decreases, the effective tunneling barrier becomes larger, and the tunneling is switched off. Thus, the tunneling can be switched on or off by controlling the gate and substrate bias.

2. Numerical estimation of tunneling term

Figure 11 shows a result of the numerical calculations of the tunneling term as a function of the FG sizes when \( d_{ox} \) and \( Z_{FG} \) are changed. It can be seen that the tunneling rate increases as \( L \) and \( Z_{FG} \) increase. These are opposite trends to \( U_h \) and \( U_w \) in Fig. 9 and show that the increasing tunneling rate makes the saving of electrons difficult. Tables 1 and 2 show typical results from Figs. 911 as a summary of the basic calculations mentioned above.

Figure 12 shows the amplitude of the tunneling term as a function of \( V_{CG} \). It is seen that, when we change \( V_{CG} \) in the range of \( \pm 1 \) V, we can change the tunneling rate in the range of \( 10^4 \). For example, for \( Z_{FG} = 100 \) nm and \( d_{ox} = 3.5 \) nm in Fig. 12(b), the tunneling term for \( V_{CG} = 0 \) is approximately 26.4 Hz and can be neglected. That for \( V_{CG} = -1 \) V corresponds to a case that an electron tunneling is expected to occur by approximately 2.2kHz.

3. Normally-off and normally-on

So far, we have considered a QAM in which tunneling is switched on when external biases are applied. Thus, these devices can be called “normally-off” devices. On the other hand, as \( d_{ox} \) becomes thinner, the tunneling frequency becomes larger and larger and the tunneling is always on even for \( V_{CG} = 0 \). For example in Fig. 12(a), the tunneling term for \( d_{ox} = 1.5 \) nm of \( L = 15 \) nm is 17.1 THz, and in Fig. 12(b), the tunneling term for \( d_{ox} = 1.5 \) nm is 1717 THz. For these cases, we can switch off the tunneling by applying positive electric voltages. Thus, we call these devices “normally-on” devices. Compared with normally-off devices, the power consumption of the normally-on devices is considered to be larger. Thus, we mainly consider the normally-off devices and discuss the normally-on devices briefly in the Appendix.

V. RESULTS OF TCAD SIMULATIONS

In general, FG memories consist of many different regions with different doping concentrations and doping types. Different regions have different work functions without bias. Typically, a p-type substrate, n-type source/drain and an n-type FG are employed where the doping concentration of the FG is higher than that in the substrate. Figure 13(a) shows the typical doping pattern. Figures 13(b) and (c) show the band structures depending on a bias voltage.

Here, we would like to show the results of the conventional TCAD simulation in our targeted parameter regions. We calculated the device characteristics of the three FG array of Fig. 13(a) by using our in-house TCAD simulator. This simulator was developed for conventional semiconductor devices, and cannot include the single-electron effect. The number of the coupled cells is limited by our calculation resources. Here we do not calculate \( J_{ij} \) (Eq. (17)) nor \( J_{ij} \) (Eq. (19)), because capacitances change depending on applied biases as a result of the change of depletion layers. Elaborate estimation will be required. Accordingly, the crossover point of \( n_G \approx 0 \) in Fig. 7 should be estimated in the near future.

In order to generate electrons at the surface of the substrate (Fig. 13(b) and (c)), \( V_{CG} > V_{sub} \) is required. Figure 14 shows the bird’s eye views of the electronic potentials of zero bias (Fig. 14a) and the case of \( V_{sub} = -3 \) V and \( V_{CG1} = V_{CG2} = V_{CG3} = -1 \) V (Fig. 14b)). Figure 15 shows the calculated electron and hole densities, potential energies and quasi-Fermi energies. It is realized that the electron density is larger than the hole density at the substrate interface. It can be also seen that Figs. 15(c) and (d) are similar to Figs. 15(e) and (f), respectively. This means that the case of \( V_{CG1} < 0, V_{CG2} < 0, \) and \( V_{CG3} < 0 \) is an extension of the case of \( V_{CG1} = V_{CG2} = V_{CG3} = 0 \) when \( V_{sub} < 0 \). The quasi-Fermi energy and potential energy of the FGs in Fig. 15(f) be-

| TABLE 1. Examples of the result of the analytical calculations for \( d_{ox} = 2.5 \) nm and \( Z_{FG} = 10 \) nm. |
|---|---|---|---|
| Size | \( J \) [K] | \( U_h \) [K] | Tunnel [GHz] |
| \( L = 5 \) nm | 596.0 | 249.7 | 5.61 |
| \( L = 10 \) nm | 85.8 | 80.4 | 22.5 |
| \( L = 15 \) nm | 23.5 | 39.5 | 50.5 |
| TABLE 2. Examples of the result of the analytical calculations for \( d_{ox} = 3.5 \) nm and \( Z_{FG} = 100 \) nm. |
|---|---|---|---|
| Size | \( J \) [K] | \( U_h \) [K] | Tunnel [GHz] |
| \( L = 5 \) nm | 534.4 | 100.1 | 1.65 |
| \( L = 10 \) nm | 251.0 | 61.5 | 6.61 |
| \( L = 15 \) nm | 124.0 | 39.3 | 14.9 |
The thickness of the substrate is 1 μm, and only the upper part of the substrate is shown. The source and drain in the substrate are set close to the outer interface between the tunneling barrier and substrate is seen that the time scale of the change of the potentials is of the order of 10^{-11} sec. Thus, tunneling event is very fast as estimated in the previous sections.

FIG. 13: Schematics of FG cell in the proposed QAM. (a) Doping pattern of an FG cell in our QAM. The FG and substrate consist of n-type and p-type semiconductors, respectively. (b) Band structure of no bias and no tunneling events. (c) Band structure of finite tunneling. Both the gate bias and substrate bias are applied negatively.

FIG. 14: Bird’s-eye views of the electrical potential profile of three FG cells calculated by in-house TCAD simulator. The interface between the tunneling barrier and substrate is z = 0 where, for simplicity, the tunneling barriers are not shown. The source and drain in the substrate are set close to the outer two FGS, and their contact holes exist at |z| ≥ 0.2075μm and z < 0. The thickness of the substrate is 1 μm, and only the upper part of the substrate is shown. L = W = 15 nm, d_{ox} = 3.0 nm and d_{s} = 7.0 nm. (CR = 0.3 in Eq. (3)). The heights of FG and CG are 0.1 μm. The doping rates of FG, source, and substrate are given by 10^{20} cm^{-3}, 2.0×10^{20} cm^{-3} and 3×10^{17} cm^{-3}, respectively. (a) V_{CG1} = V_{CG2} = V_{CG3} = V_{sub} = 0. (b) V_{sub} = -3 V, and V_{CG1} = V_{CG2} = V_{CG3} = -1 V.

FIG. 15: The carrier densities (electrons and holes), the potential energies, and the quasi-Fermi energies of the center FG2, as a function of the distance from the surface of the substrate. (a) and (b) show the results of zero bias (V_{CG1} = V_{CG2} = V_{CG3} = V_{sub} = 0). (c) and (d) show the results of V_{CG1} = V_{CG2} = V_{CG3} = 0 V and V_{sub} = -3 V. (e) and (f) show the results of V_{CG1} = V_{CG2} = V_{CG3} = -1 V and V_{sub} = -3 V. Those of the FG1 and FG3 have similar values as these results.

VI. NOISE AND DECOHERENCE

Here, we discuss the noise and decoherence problems in the QAM based on an FG array. In the conventional FG array, the thickness of the tunneling oxide is of the order of 7 nm to store the charge in the FG for many years. In the present setups, we apply a thinner tunneling oxide (d_{ox} ≤ 3.5 nm) to control switching on and off the tunneling. Thus, natural leakage of charges occurs more often than in the case of the conventional FG memory. Therefore, after the QAM process, the results should be quickly transferred to a conventional memory block.

The unexpected trap sites are ones of the problems of NAND flash memories. These will become more serious when we use an FG array as a qubit system. However, the physical properties of the traps persist on each cell as shown in Ref. 40. Once we check the trap distributions and their properties and store that information to conventional memory, we could apply appropriate voltages depending on each FG cell and improve the QAM performance.

Next, let us estimate the coherence time by taking into account the electron-phonon interactions, following the
We assume that the acoustic phonon in the tunneling material of SiO$_2$ is the principal origin of decoherence and apply the standard spin-boson theory. According to Leggett et al., the complete information about the effect of the environment is encapsulated by the spectral function $\mathcal{J}(\omega)$. In the present case, the two-state system is formed through the tunneling of SiO$_2$ and it has two types of spectral function given by:

$$\mathcal{J}(\omega) = \frac{\gamma^2}{\rho c\omega^3} + \frac{\gamma^2\nu^2}{\rho c\omega^2},$$

The first term shows a superohmic dissipation and corresponds to an underdamped coherent oscillation, whose damping rate $\Gamma_{so}$ at $T = 0$ is given by:

$$\Gamma_{so} = \frac{\gamma^2\Delta^3}{4\pi\rho c^5},$$

where $\Delta$ is the renormalized tunneling frequency $\Delta$, and given by:

$$\Delta = \Delta \exp\left(-\frac{\gamma^2\omega_c^2}{2\pi^2\hbar\rho c^5}\right).$$

When we use $\gamma \sim 10$ eV, $c \sim 4300$ m/s, $\rho \sim 2200$ kg/m$^3$, and $\omega_c = k_B\Theta_D/\hbar$ with $\Theta \sim 450$K, we have $\Delta \sim \Delta e^{-1323}$, and thus this term can be neglected. The second term of Eq. (26) expresses an ohmic dissipation. The parameter $\alpha$ of the ohmic dissipation is given by $\alpha = \gamma^2\nu^2/(2\pi^2\hbar\rho c^5d^2) \sim 7.05 \times 10^{-9}$. Then $P(t) \equiv \langle \sigma_z(t) \rangle = P_{coh}(t) + P_{inc}(t)$ is given by:

$$P_{coh}(t) \approx \cos \Delta t \exp\left(-\frac{\pi\alpha\Delta t}{2}\right),$$

$$P_{inc}(t) \approx \alpha \{\Delta t (ci(\Delta t) \sin \Delta t - si(\Delta t) \cos \Delta t)\},$$

where $ci(y) = -\int_y^\infty (\cos x)/xdx$ and $si(y) = -\int_y^\infty (\sin x)/xdx$. When we estimate the coherence time from the exponential part of $P_{coh}(t)$ such as $\alpha\pi\Delta t_{coh}/2 = 1$, we have $t_{coh} \sim 4.33$ msec for $\Delta = 10$K and $t_{coh} \sim 0.433$ msec for $\Delta = 100$K, respectively. Therefore, the increase of the tunneling excites more phonons, and a low tunneling rate is desirable. However, tunneling that is too slow induces many noises. Thus, there will be an optimal point for the tunneling rate, depending on each system.

VII. DISCUSSION

In Ref. 35, we have proposed a charge-qubit system based on coupled quantum dots (CQDs). When we regard FGs as quantum dots (QDs), the previous CQD proposal is different from the present proposal in that there are additional FGs stacked on the first FG layer. Although additional fabrication processes are required for the CQD system, the structure of the CQD system can be manufactured by the same set of photo masks as that in the present proposal. Because the electron moves in the close-coupled QDs in the previous proposal, its coherence time is considered to be longer than that of the present proposal. Besides the fact that the present proposal is more close to the conventional flash memory, the advantage of the present proposal is that the electron tunneling is directly changed by the external electrodes. In contrast, the tunneling barrier of the CQD system is fixed, and qubit states are mainly controlled in the rotating frame by applying high-frequency electric field.

We have to readout the final state after the annealing process. At the readout stage, the number of electrons in the FG should be detected by applying gate voltage and switching on current between the source and drain. As in the conventional FG array, the applied voltage of the reading out is smaller than that of the ‘switching-on’ process. The readout process should not change the number of electrons in the FG array. The thickness of the tunneling oxide of the normally-off type is greater than that of the normally-on type (as discussed in the Appendix). Thus, it is considered that the normally-off type is more easily constructed than the normally-on type. In any event, detailed optimizations of the structure and operation voltages are subjects for future work.

VIII. CONCLUSION

We have shown that the conventional FG memory structure can be used as the quantum annealing machine. It is assumed that the FG is sufficiently small for the appearance of the single-electron effect. The electrostatic Coulomb interaction between FG cells is the origin of the Ising interaction. The tunneling between the FG and substrate is brought about by applying voltages to both the CG and substrate, while the source/drain voltage is set to zero. Using TCAD simulation, we have shown an example of the device characteristics under possible bias
conditions. Optimization of many parameters is a subject for future work.

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Appendix A: Detailed derivation process of the charging energy

Here, we show additional information for the derivation process of Eq. (16). The parameters in Eq. (13) in the text are given by

\[ C_{a_1} = C_{A_1} + C_{B_1} + C_{D_1} + C_{F_1} + C_{H_1} + C_{I_1}, \]

\[ C_{a_2} = C_{A_2} + C_{B_2} + C_{D_2} + C_{F_2} + C_{H_2} + C_{I_2}, \]

\[ + C_{D_1} + C_{E_1} - \frac{C_{D_1}^2}{C_{a_1}}, \]

\[ C_{a_3} = C_{A_3} + C_{B_3} + C_{D_3} + C_{F_3} + C_{H_3} + C_{I_3}, \]

\[ + C_{D_2} + C_{E_2} - \frac{C_{D_2}^2}{C_{a_2}}, \]

\[ Q_{v_1}^0 = C_{A_1} V_{CG1} + C_{B_1} V_{sub} + C_{F_1} V_{CG2} + C_{H_1} V_{s_1} + C_{I_1} V_{d_1}, \]

\[ Q_{v_2}^0 = C_{A_2} V_{CG2} + C_{B_2} V_{sub} + C_{F_2} V_{CG3} + C_{H_2} V_{s_2} + C_{I_2} V_{d_2}, \]

\[ Q_{v_3}^0 = C_{A_3} V_{CG3} + C_{B_3} V_{sub} + C_{H_3} V_{s_3} + C_{I_3} V_{d_3}, \]

\[ W_1 = C_{A_1} V_{CG1} + C_{B_1} V_{sub} + C_{F_1} V_{CG2} + C_{H_1} V_{s_1} + C_{I_1} V_{d_1}, \]

\[ W_2 = C_{A_2} V_{CG2} + C_{B_2} V_{sub} + C_{F_2} V_{CG3} + C_{H_2} V_{s_2} + C_{I_2} V_{d_2}, \]

\[ W_3 = C_{A_3} V_{CG3} + C_{B_3} V_{sub} + C_{H_3} V_{s_3} + C_{I_3} V_{d_3}, \]

(A1)

where \( V_{d_1} = V_{s+1} \). Following Ref. 23, we consider the region around

\[ (n_i + Q_{v_i}^0)^2 = (n_i + 1 + Q_{v_i}^0)^2 \]  

(A2)

This is the region where the charging energy of \( n_i \) electrons equals that of the \( n_i + 1 \) electrons, and the \( \{n_i\} \) and \( \{n_i + 1\} \) states constitute a superposition state. We use the effective gate voltage \( n_{G_{i}}, \) given by

\[ n_i + Q_{v_i}^0 = n_{G_{i}} - 1/2. \]  

(A3)

\( (n_{G_{i}} \ll 1) \). For this region, we can approximate the following equation

\[ \sum_{m=0}^{1} (n_i + m + Q_{v_i}^0)^2 \rightarrow \frac{1}{2} n_{G_{i}} \sigma_i^z + \left( n_{G_{i}}^2 + \frac{1}{4} \right) I_i. \]  

(A4)

where \( \sigma_i^z \), \( I_i \) are Pauli matrix and unit matrix, respectively based on \( \{n_{i} + 1\} \{n_{i}\} \) system. Thus we obtain

\[ \begin{array}{c}
\text{FIG. 17: Schematics of FG cell of a normally-on QAM. (a) Band structure without bias. Tunneling is switched off. (b) Band structure without tunneling events. Both the gate bias and substrate bias are applied positively.}
\end{array} \]

Appendix B: Normally-on and normally-off

In the main text, we consider a case in which tunneling occurs only when the gate and substrate biases are applied. These devices can be called "normally-off" devices. In this section, we briefly discuss a "normally-on" device in which tunneling is switched off only when the gate and substrate bias are applied.

Figure 17 shows an example of the normally-on set up. The electron tunneling always occurs between the FG and the substrate without bias as shown in Fig. 17(a). The effective thickness of the effective tunneling barrier is changed by the change of the potential of the FG and substrate. If we prepare a p-type substrate like that of the conventional NAND flash memory, the current from the substrate to the source and drain flows when the tunneling is switched off (Fig. 17(b)). This is because the source and drain are n-type semiconductors. Thus, in the normally-on type QAM, there are always some current flows in the cell. Detailed calculations are subjects for future work.

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