A flexible control system for atomic, molecular and optical physics experiments

A. Trenkwalder, M. Zaccanti and N. Poli

Istituto Nazionale di Ottica del Consiglio Nazionale delle Ricerche (INO-CNR), 50019 Sesto Fiorentino, Italy
European Laboratory for Nonlinear Spectroscopy (LENS), 50019 Sesto Fiorentino, Italy
Dipartimento di Fisica e Astronomia and INFN Sezione di Firenze, Università degli Studi di Firenze, Via Sansone 1, 50019 Sesto Fiorentino, Italy

(*Electronic mail: trenkwalder@lens.unifi.it)
(*Electronic mail: poli@lens.unifi.it)
(Dated: 8 June 2021)

We have implemented a control system for experiments in atomic, molecular and optical physics based on a commercial low-cost board, featuring a field-programmable gate array as part of a system-on-a-chip on which a Linux operating system is running. The board features Gigabit Ethernet, allowing for fast data transmission and operation of remote experimental systems. A single board can control a set of devices generating digital, analog and radio frequency signals with a precise timing given either by an external or internal clock. Contiguous output and input sampling rates of up to 40 MHz are achievable. Several boards can run synchronously with a timing error approaching 1 ns.

I. INTRODUCTION

Experimental control and data acquisition systems are widespread in many fields of scientific and industrial research where test and measurement systems need to be controlled and experimental data have to be gathered. For the application of controlling experiments in the field of atomic, molecular and optical (AMO) physics digital pulses, analog, radio and microwave frequency signals need to be generated at well-defined times. For instance, laser cooling and trapping of atomic gases down to ultralow temperatures typically require a temporal resolution of one microsecond. For this task, field programmable gate arrays (FPGAs) are very well suited. These can generate arbitrary digital pulses which can be used to program digital-to-analog converters (DAC), direct-digital synthesizers (DDS), and other devices with the requested timing resolution. As a result, FPGAs are already successfully employed in both commercial and open source control systems.

Owing to their flexibility, FPGAs also find application for a wide range of different tasks, encompassing clock signal generation, DDS programming, arbitrary waveform generation, lock-in demodulation, high-speed data acquisition (DAQ), digital feedback servo systems. Moreover, FPGAs are increasingly used for the control of quantum systems and processors and as feedback devices for quantum measurements, and can be even used within cryogenic environments. Applications of FPGAs in space are becoming of growing interest. Despite all of these applications, the development of a custom FPGA-based system is time consuming and commercial solutions tend to be expensive. Nonetheless, the advent of cheap, multi-purpose FPGA development boards targeted for hobbyists and students, offers a solution with low-cost and short development time, from which also experimental research can benefit thanks to the impressive capabilities of these boards.

Here we present a control system with a novel approach based on a commercial, low-cost system-on-a-chip (SoC) board, consisting of a central processing unit (CPU) which is tightly connected to an FPGA and to a set of hardware interfaces used to communicate with external devices. A Linux operating system, executed on the CPU, gives the flexibility to use high-level programming languages, which can be quickly adapted to any specific request, such as interfacing with external devices like USB, Secure Digital (SD) memory card or Ethernet with no need of additional hardware or specifically designed micro-controllers. Furthermore, the presence of an electrically isolated Gigabit Ethernet interface, allows fast data transfer and easy connection to remote locations.

All these features represent a clear advantage of FPGA-SoC systems with respect to previously realized FPGA-based solutions, not only in terms of the superior data rates offered by the Ethernet interface, but also by the additional flexibility given by the presence of the easy programmable CPU and the fact that these are stand-alone systems which can be utilised independently on the hardware and software environment.

As a powerful simple application of such extended capabilities, here we demonstrate a novel scheme to auto-synchronize several boards using only two coaxial cables and the Ethernet communication. Without user interaction or dedicated real-time networking hardware, the propagation delays of the signals among distant boards are measured by the boards and are corrected automatically with a residual timing error approaching 1 ns.

The paper is organized as follows: First, we present the board architecture in Sec. I and the developed software in Sec. II. We then present the measured performance and the auto-synchronization scheme in Sec. III and discuss the results in Sec. IV.
The heart of our control system is the Cora-Z7 board from Digilent\textsuperscript{22}, which hosts the Zynq-7007S (Zynq-7010) FPGA-SoC from Xilinx with a single (dual) core CPU (ARM Cortex A9) clocked at 650 MHz. This represents the smallest FPGA-SoC from the Xilinx Zynq-7000 series. The board is provided with 512 MB of DDR3 SDRAM (16 bits data clocked at 525 MHz) with Gigabit Ethernet and USB host and device ports. The FPGA part is nearly the same for the two variants and is similar to the low-end Artix-7 FPGA series, aiming for low-cost, low-power consumption and less demanding applications. It should be noted, that, while we choose a particular FPGA-SoC board with Gigabit Ethernet to implement our control system, the system and the methods presented in this paper can be implemented with any other FPGA-SoC boards with similar performance. For example, the DE10-Nano from Terasinc Inc. is a possible alternative\textsuperscript{23}.

A custom designed buffer card\textsuperscript{22} is used to buffer the FPGA-SoC board signals and to shift the voltage level from the internal 3.3 V logic level to the 5 V (TTL) level of the bus. The buffer card also provides the needed buffers for the clock and trigger line used for the synchronization of different boards, as described below. An image of the FPGA-SoC board mounted on the buffer card is shown in Fig. 1b, and in Fig. 1c an image of the FPGA-SoC board (front side) is shown.

A. The FPGA logic

Here we give an overview on the logic used in the FPGA to generate the experiment control data on the bus and all the signals necessary for the synchronization of several boards. A simplified block diagram is shown in Fig. 2. The board is basically composed of two parts: the processing system (PS, top, green), consisting of a CPU on which a Linux operating system is running, and the programmable logic (PL, bottom, yellow), where our custom hardware is implemented. The two parts of the FPGA-SoC are tightly bound via interfaces and buses, enabling mutual data exchange at high speed. In such a way, the two main tasks of the board are effectively separated among the two independent parts of the FPGA-SoC system itself. While the processing system handles the communication via Ethernet with an external control computer, the logic part produces the signals on the bus. The driver mediates between both parts and coordinates the access to the external memory. The source code for programming the FPGA is written in Verilog. It is synthesized and implemented with the Vivado
GigE

ext. clock

ext. trigger

PL (PS)

CPU

PLL0

clock (red), the pulse round-trip number of cycles the data on the bus. In combination with a phase-shifted detection AXI-4 Lite interface reading and writing of memory mapped registers (via AMBA.

resources used for this application is reported in Tab. III in 2017.4 software from Xilinx running on Ubuntu 18.04 LTS, and is available online[29]. Detailed information on the FPGA resources used for this application is reported in Tab. III in Appendix D.

In brief, we use one general purpose I/O (GPIO) port for the reading and writing of memory mapped registers (via AMBA AXI-4 Lite interface[29], and one high performance (HP) port to efficiently transfer the experiment control sequence from the memory to the PL part and vice-versa (using direct memory access DMA[29] via an AXI stream bus). The clock frequency for the PL part, CPU and the DDR memory are set to their default values, corresponding to 50 MHz, 650 MHz and 525 MHz respectively.

The experiment control sequence (represented by thick lines in Fig. 2) is sent via Ethernet from the control computer to a TCP/IP server application running on the CPU. The server application interacts with a Linux kernel driver module[29] which writes the data into DDR memory and programs the FPGA registers using the AXI Light bus. The data are transferred via DMA from the memory into a transmit (TX) first-in-first-out (FIFO) buffer[29] which holds a maximum of 8192 samples of 128 bits each. The FIFO serves to buffer gaps in the DMA data transmission, and allows efficient transfer of data between regions using different clocks (clock domains). In addition, we have implemented a receive DMA channel (RX), which can be used, for example, to read data from an analog input device that sends data on the bus.

In our case, the experiment control sequence consists of 64 bits per sample: 32 bits are used for the time-stamp, 7 address bits select which device on the bus to be updated, and 16 device specific bits define the new state of the device[29]. The time-stamp defines at which time the bus should be updated with the specific data and address of the corresponding device. After the bus has been updated, a pseudo-clock pulse (strobe) is generated by the FPGA on another pin of the bus, to initiate the state change of the selected device[29]. The time-stamp is defined in units of $1/\Gamma_{\text{sample}}$ with $\Gamma_{\text{sample}}$ being the output sampling rate of the bus, typically set to 1 MHz or 10 MHz.

The timing module is responsible to output the data on the bus. It first takes out one 64 bits-wide sample from the 128 bits of the TX FIFO, and it compares the time-stamp with an internal counter running at $\Gamma_{\text{sample}}$. When they are equal, the module outputs the 16+7 data and address bits, and it generates the previously mentioned strobe signal. The timing module internally uses a dedicated 50 MHz bus clock, which can be either the PL system clock (i.e. the internal oscillator of the FPGA-SoC board), or it can be generated from an external clock signal using a phase locked loop (PLL) of the FPGA-SoC. In the latter case, the frequency allowed for the external clock signal ranges from a minimum value of 10 MHz, limited by the PLL, to a maximum of 300 MHz, limited by the input buffer on the buffer card. A second PLL is used as a software controlled multiplexer (MUX) to switch between the two clock sources[29]. Both PLLs enable to dynamically change the phase of the generated clock signals. The auto-synchronization module, discussed in Sec. II B is using these signals to synchronize several boards. The timing module can also trigger the output of the experimental sequence, which alternatively can be started by an external hardware trigger or via software. Finally, both the DMA TX/RX channels and the timing module communicate with the driver via interrupts. The DMA channels generate interrupts when buffers need to be updated. The timing module generates one interrupt when the experimental control sequence has been completed. Further interrupts are generated at a configurable frequency, typ-
ically 16 Hz, and are used to update the board status in the control software.

B. Auto-synchronization

In order to synchronize several FPGA-SoC boards, all boards need to start the experimental control sequence simultaneously and they need to use the same clock source to execute each command at the same time. The common clock can be either generated by one board, or provided externally. In both cases, a suitable amplification and distribution system to all boards is needed, which might introduce unknown phase shifts. Additionally, a starting (trigger) signal needs to be distributed from one board to all the others, and can accumulate an unknown delay. As discussed in the following, our scheme takes into account and corrects for these effects.

To compensate the delay on the start trigger signal, we adopt a scalable scheme, where one trigger line is connected with high impedance to all participating boards, see Fig. 3a. The trigger line is a coaxial cable with 50 Ω impedance on both ends to avoid unwanted reflections. One board, called the primary board, receives the start signal from the control computer (or from an external hardware trigger), and generates a pulse in the trigger line which is detected by the other “secondary” boards. In order to compensate for the pulse propagation time between the boards, the propagation time is automatically measured in advance, such that each board can delay its execution accordingly and all boards can start at the same time.

To measure the propagation delay, the primary board instructs via Ethernet one of the secondary boards to introduce a short circuit in the trigger line using a bipolar or a field-effect transistor. Then the primary board generates a pulse in the trigger line, and it measures the round-trip time \( t_{RT}^i \) needed by the pulse to propagate to the secondary board \( i \), be reflected at the short circuit, and travel back (see Fig. 3b). Here \( N_{RT}^i = N_{det}^i - N_{gen}^i \) is the number of cycles between the generation \( N_{gen}^i \) and detection \( N_{det}^i \) of the pulse, and \( \Delta t_{RT}^i < T \) is a fraction of the period \( T \) of the bus clock of the primary board. While \( N_{RT}^i \) can be measured directly, \( \Delta t_{RT}^i \) cannot. This limits the resolution to the period \( T \), which is 20 ns for the chosen 50 MHz bus clock frequency, and would not be satisfactory for bus output rates above 10 MHz. To measure the total delay with higher accuracy, the reflected pulse is sampled with a phase shifted replica (detection clock) of the bus clock signal. A train of trigger pulses is generated, and the phase shift of the detection clock is varied between pulses. For a linear increase of the detection clock phase, at:

\[
\phi_{p,i} = \frac{\Delta t_{RT}^i \cdot 360^\circ}{T},
\]

the measured \( N_{RT}^i \) reduces by one. This change in \( N_{RT}^i \) is detected, and \( \Delta t_{RT}^i \) can be obtained. In principle, this method would allow one to achieve a time resolution of about 20 ps, given the 0.3° phase resolution of the PLL at the used clock frequency. However, noise in the generation and detection of the pulse actually limits the resolution to larger values. This measurement is repeated for each secondary board \( i \in \{0, \ldots, N\} \). With the measured round-trip time \( t_{RT}^i \), the propagation time of the pulse from the primary board to the \( i \)-th secondary board is calculated as:

\[
t_{p}^i = t_{RT}^i / 2.
\]

It is important to notice that in this simplified treatment we neglect all additional (but constant) delays, both internal to the FPGA and due to the electronics needed for the generation and detection of the pulse. Details of the full model accounting for these additional delays are given in Appendix A 1.

![FIG. 3. Triggering and auto-synchronization scheme for multiple boards.](image-url)
In order to achieve a perfect synchronization among all boards, the measurement of $\tau_i^c$ for each board discussed above is not sufficient, since the clocks of the secondary boards must be corrected for the delays $\tau_i^c$ introduced along the clock distribution line (see Fig. 3). In this case however, one needs to know only the introduced clock delay $\Delta\tau_i^c = \tau_i^c\%T$, where $\%$ is the modulus. To this end, a second set of measurements is carried out, where the primary board generates a train of pulses similarly to the previous scheme, but the measurement is now taken on the secondary boards. Since the pulses do not need to be reflected, all the secondary boards can measure the respective clock delay simultaneously. Each secondary board determines the time $\Delta\tau_i^c$ between the arrival of the pulse and the previous rising bus clock edge, local to the secondary board. Similarly to the delay $\Delta\tau_{RT}^i$, here the quantity $\Delta\tau_i^c$ is obtained by detecting the arrival of the pulse with both the detection and the bus clock simultaneously, giving $N_{det}^i$ and $N_{bus}^i$ (blue dashed line in Fig. 3b), respectively. The difference between the two signals $N_{det}^i - N_{bus}^i$ is monitored for a reduction of one cycle at the phase:

$$\phi_i^{c,l} = \frac{\Delta\tau_i^c \cdot 360^\circ}{T},$$

and $\Delta\tau_i^c$ can be obtained. At the secondary board location, the calculated pulse delay with respect to the primary bus clock is $\Delta\tau_{RT}^i / 2$ and the difference to the observed delay $\Delta\tau_i^c$ gives the unknown clock delay:

$$\Delta\tau_i^e = \frac{\Delta\tau_{RT}^i}{2} - \Delta\tau_i^c.$$

Once $\Delta\tau_{RT}^i$ and $\Delta\tau_i^c$ are determined for each secondary board $i = 0 \ldots N$, the external clock PLL phases $\phi_{bus}^i$ of each secondary board can be set to $\phi_{bus}^i = -\Delta\tau_i^c \cdot \frac{360^\circ}{T}$. In this way, the clocks of all secondary boards are synchronized with that of the primary one and the auto-synchronization measurement is completed and all parameters are set. In order to simultaneously generate data on all boards, the primary board sends a pulse in the trigger line. It then waits until all secondary boards have detected the trigger pulse, i.e., i.t. it waits the largest propagation time $\tau_p^i$. Each secondary board $i$ waits $\tau_p^i$ less time than the primary board. After these waiting times, all boards synchronously start generating output of data on their bus.

While we refer the reader to Appendix A for more details, we emphasize that our auto-synchronization scheme allows for the synchronization of many boards on time scales of order of nanoseconds with a relatively simple scheme and few external components. A first experimental demonstration of this scheme together with measurements of the residual synchronization timing error are presented in Sec. IV.

III. SOFTWARE

In this section we summarize the software implementation on the PS/CPU part of the SoC, on which a Linux operating system is running. This is a fully featured operating system which provides system services and interfaces to external devices, and that can be configured for our specific needs. The PL part appears for the operating system like an external device, and our device driver can communicate with it via registers.

A. Control computer software

Many research laboratories, including ours, typically employ either Labview or LabWindows/CVI as user application programs. While our setup is currently adapted to work with this software, we emphasize that any other user application can be easily implemented on our hardware, provided that the data need to be sent via Ethernet to our TCP/IP server running on the FPGA-SoC. No additional driver nor hardware is required, and no constraints on the operating system are given for the control computer. For example, the freely-available, Python-based control software “labscript suite” might be a viable alternative to the above mentioned commercial solutions. We provide the necessary files in Ref. 22 to use our FPGA-SoC board together with the suite.

In our specific case, we upgraded an existing control system based on a digital I/O card installed on the experiment control computer, driving the bus via a 2 m long cable and a buffer card. The FPGA-SoC system replaces completely the former system, maintaining the compatibility with previous hardware and software. For this, a new Windows dynamic link library (DLL) has been written, which communicates via Ethernet with the FPGA-SoC while keeping the same functions of the previous I/O card.

B. TCP/IP server and Linux device driver

We have designed a simple TCP/IP server application, running on the FPGA-SoC, which receives commands and the user data from the control computer, and which communicates with our device driver that mediates with the two FPGA-Soc parts, see Fig. 2.

Our server application can control, via the device driver, the FPGA PL part, write the user data into reserved DMA (coherent) memory, and receive status information from it. The driver allows a user application to read back data from the PL part, wait for interrupts or for the end of the sequence. The driver maintains the ring buffers for the DMA transfer, and respond to the corresponding interrupts. We have reserved 128 MiB of memory for coherent DMA transfer. This size corresponds to $10^7$ samples and 10 seconds of contiguous data output at $f_{sample} = 1$ MHz. However, most applications typically do not require such a large number of samples and dense output of data. If needed, data could be uploaded via Ethernet during the experimental run as well. The reserved size is sufficiently large to store all user data directly into coherent memory, which keeps the server and driver simple, and it avoids additional copying for repeated runs. A timer interrupt, generated by the PL part, and transmitted by the driver, allows the server application to send status information at regular intervals to the control computer.
C. Startup script

When the board is powered up, a bootloader reads from a SD card the binary data to program the PL part and to load the required Linux image into memory, and to start the operating system. After this is completed, our startup script reads a configuration file from the SD card which contains the IP address and other information, with which it configures the Linux system and launches our TCP/IP server application. The server may either initiate the auto-synchronization procedure on startup, or wait for instructions from the control computer. A startup script and a text configuration file are used to change the configuration of the board without the need of recompiling the binary code from the sources.

IV. MEASUREMENTS AND RESULTS

In this section we present and discuss measurements done on the FPGA-SoC board. For these measurements, specific code running on the FPGA-SoC system has been written, and the data has been acquired directly on the board and stored on a micro-SD card[37] for further analysis. Except for the verification of the synchronization error, no external measurement was needed. All the data presented in the paper is available in Ref. [38].

In the first part, Sec. [IV A] measurements of the DMA transmission rates are shown, defining how fast data can be transmitted from the external memory into the PL part and back. This represents a direct measure of the maximum sampling rate at which the board can continuously output and input data. In the second part, Sec. [IV B] we present measurements on the data uploading rates over Gigabit Ethernet for both the Cora-Z7-10 and Cora-Z7-07S boards. This measurement confirms that Gigabit Ethernet is a good choice for experiments where a fast cycle time is required. In the last part, Sec. [IV C] we present first measurements of the proposed auto-synchronization scheme outlined in Sec. [II B] tested on a simple two-board configuration. An additional measurement presented in Appendix [C] demonstrates the start- and stop trigger option in cycling mode.

A. DMA transmission rates

In order to measure the DMA data transmission rates of the FPGA-SoC board we have temporarily added a module in the PL part which allows one to transmit data without delay in a “loop-back” configuration between the TX and the RX FIFO buffers (see Fig. 2), and to measure the time interval required to transmit a certain number of samples. From the measured time \( t \) and the number of samples \( N \) we calculate the average data rate \( \Gamma \) in MB/s using: \( \Gamma = \beta \times \frac{N}{t} \), with \( \beta = 12 \) bytes per sample for this measurement. In particular, we measure three distinct rates, shown in Fig. 4 for the Cora-Z7-10 board, as a function of the number of samples \( N \): the transmission rate from the memory to the PL part (TX DMA, red circles), the transmission rate from the PL part to the memory (RX DMA, orange squares) and the transmission rate through the RX FIFO (green diamonds). Each experimental point (error bar) shown in the figure represents the mean value (standard deviation) of at least 20 repeated measurements for each \( N \).

The second measurement (orange squares in Fig. 4) shows the RX transmission rate obtained from the time interval between the first sample written into the RX FIFO and the RX DMA buffer (see Fig. 2), and to measure the time interval required to transmit a certain number of samples. From the measured time \( t \) and the number of samples \( N \) we calculate the average data rate \( \Gamma \) in MB/s using: \( \Gamma = \beta \times \frac{N}{t} \), with \( \beta = 12 \) bytes per sample for this measurement. In particular, we measure three distinct rates, shown in Fig. 4 for the Cora-Z7-10 board, as a function of the number of samples \( N \): the transmission rate from the memory to the PL part (TX DMA, red circles), the transmission rate from the PL part to the memory (RX DMA, orange squares) and the transmission rate through the RX FIFO (green diamonds). Each experimental point (error bar) shown in the figure represents the mean value (standard deviation) of at least 20 repeated measurements for each \( N \).

For the measurement of the TX transmission rate (red circles in Fig. 4) we measure the time interval from the first sample received out of the TX FIFO until the \( N \)-th sample is received. The first four samples are transmitted with the maximum possible rate of one sample per cycle, i.e. \( \Gamma_{\text{max}} = \beta \times f_{\text{PL}} = 600 \text{ MB/s} \) (horizontal black dotted line) for the PL clock frequency of \( f_{\text{PL}} = 50 \text{ MHz} \). This is because the TX FIFO already contains three to four samples when the measurement starts (in agreement with the simulated latency of the used FIFO). As \( N \) is increased, the rate reduces rapidly until it reaches a constant rate \( \Gamma_{\text{DMA}} \) (horizontal red dotted line), corresponding to the transmission rate from memory to the PL part. We remark, that this characterization does not allow to measure a possible delay between the start of the DMA transmission, initiated by the CPU and the arrival of the first sample.

The second measurement (orange squares in Fig. 4) shows the RX transmission rate obtained from the time interval between the first sample written into the RX FIFO and the RX DMA buffer (see Fig. 2), and to measure the time interval required to transmit a certain number of samples. From the measured time \( t \) and the number of samples \( N \) we calculate the average data rate \( \Gamma \) in MB/s using: \( \Gamma = \beta \times \frac{N}{t} \), with \( \beta = 12 \) bytes per sample for this measurement. In particular, we measure three distinct rates, shown in Fig. 4 for the Cora-Z7-10 board, as a function of the number of samples \( N \): the transmission rate from the memory to the PL part (TX DMA, red circles), the transmission rate from the PL part to the memory (RX DMA, orange squares) and the transmission rate through the RX FIFO (green diamonds). Each experimental point (error bar) shown in the figure represents the mean value (standard deviation) of at least 20 repeated measurements for each \( N \).

For the measurement of the TX transmission rate (red circles in Fig. 4) we measure the time interval from the first sample received out of the TX FIFO until the \( N \)-th sample is received. The first four samples are transmitted with the maximum possible rate of one sample per cycle, i.e. \( \Gamma_{\text{max}} = \beta \times f_{\text{PL}} = 600 \text{ MB/s} \) (horizontal black dotted line) for the PL clock frequency of \( f_{\text{PL}} = 50 \text{ MHz} \). This is because the TX FIFO already contains three to four samples when the measurement starts (in agreement with the simulated latency of the used FIFO). As \( N \) is increased, the rate reduces rapidly until it reaches a constant rate \( \Gamma_{\text{DMA}} \) (horizontal red dotted line), corresponding to the transmission rate from memory to the PL part. We remark, that this characterization does not allow to measure a possible delay between the start of the DMA transmission, initiated by the CPU and the arrival of the first sample.

The second measurement (orange squares in Fig. 4) shows the RX transmission rate obtained from the time interval between the first sample written into the RX FIFO and the RX DMA buffer (see Fig. 2), and to measure the time interval required to transmit a certain number of samples. From the measured time \( t \) and the number of samples \( N \) we calculate the average data rate \( \Gamma \) in MB/s using: \( \Gamma = \beta \times \frac{N}{t} \), with \( \beta = 12 \) bytes per sample for this measurement. In particular, we measure three distinct rates, shown in Fig. 4 for the Cora-Z7-10 board, as a function of the number of samples \( N \): the transmission rate from the memory to the PL part (TX DMA, red circles), the transmission rate from the PL part to the memory (RX DMA, orange squares) and the transmission rate through the RX FIFO (green diamonds). Each experimental point (error bar) shown in the figure represents the mean value (standard deviation) of at least 20 repeated measurements for each \( N \).

For the measurement of the TX transmission rate (red circles in Fig. 4) we measure the time interval from the first sample received out of the TX FIFO until the \( N \)-th sample is received. The first four samples are transmitted with the maximum possible rate of one sample per cycle, i.e. \( \Gamma_{\text{max}} = \beta \times f_{\text{PL}} = 600 \text{ MB/s} \) (horizontal black dotted line) for the PL clock frequency of \( f_{\text{PL}} = 50 \text{ MHz} \). This is because the TX FIFO already contains three to four samples when the measurement starts (in agreement with the simulated latency of the used FIFO). As \( N \) is increased, the rate reduces rapidly until it reaches a constant rate \( \Gamma_{\text{DMA}} \) (horizontal red dotted line), corresponding to the transmission rate from memory to the PL part. We remark, that this characterization does not allow to measure a possible delay between the start of the DMA transmission, initiated by the CPU and the arrival of the first sample.
initial increase is consistent with a constant delay of 202(8) PL cycles, required for the RX DMA channel to start or finish the transmission. This delay is larger than expected and it points to a significant latency in the RX channel. Nonetheless, the large RX FIFO can easily compensate for such a latency.

The third measurement, shown in Fig. 4 as green diamonds, was taken simultaneously with the RX transmission rate, and it shows the data rate through the RX FIFO: namely, the rate obtained from the time N samples need to pass through the RX FIFO during active RX transmission. As long as the RX FIFO is not full, one sample per cycle is transmitted, corresponding to $\Gamma_{\text{DMA}}$. When the RX FIFO becomes full with $N_{\text{FIFO}} = 8192$ samples (dotted vertical line in Fig. 4), the rate reduces to the RX and TX data transmission rate $\Gamma_{\text{DMA}}$. Since the RX FIFO is simultaneously loaded with $\Gamma_{\text{max}}$, and unloaded with $\Gamma_{\text{DMA}}$, we expect this rate to drop once the number of transmitted samples reaches $N_{\text{FIFO}} = \frac{\Gamma_{\text{max}}}{\Gamma_{\text{DMA}}} \approx 19 \times 10^3$ samples, a value close to the observed one of $20(1) \times 10^3$ samples.

All three measurements give for large number of samples a consistent DMA transmission rate of $\Gamma_{\text{DMA}} = 341(1)\text{MB/s}$ (averaged over all measurements). This rate deviates with the specified rates from Xilinx\textsuperscript{[24]} for the default settings. In particular, the TX rate is lower while the RX rate is higher than specified. However, their measured sum is 684(2) MB/s, which is only 2% lower than the value expected from the specification of 700 MB/s. Although the exact reason for this discrepancy is not clear (the ratio between the TX and RX rates can be adjusted\textsuperscript{[24,25]}), the observed overall performance allows us to conclude that our DMA transmission rates are indeed close to the maximum possible ones for a single HP port. Finally, from the measured DMA transmission rate we can also directly deduce the maximum contiguous bus data rate of $\Gamma_{\text{DMA}}/\beta = 30 - 40 \text{MB/s}$\textsuperscript{[25]}

We note that, the FPGA-SoC has 4 HP ports, and in our design there should be enough free resources to use at least an additional one to increase the DMA rate even further, if higher bus rates are needed. Short “bursts” of data output (input) of up to 8192 samples at higher frequencies are already possible with the present setup as long as there is sufficient time before the “burst” to fill (empty) the TX (RX) FIFO and the rate afterwards is slow enough to prevent the TX (RX) FIFO from becoming empty (full). Although not shown here, we have performed the same measurement for the Cora-Z7-07S board, finding no significant deviation from the results presented in Fig. 4.

B. Ethernet uploading rates

The uploading rate from the control computer to the FPGA-SoC board over Gigabit Ethernet is another measure of the performance of our system. It can be a limitation for experiments where short cycle times are need, like experiments with optical tweezers\textsuperscript{[25]} or with ions\textsuperscript{[46]}

Fig. 5a shows the uploading rate measured for the Cora-Z7-10 (solid blue circle) and Cora-Z7-07S (solid orange square) board. This measurement includes the total time of uploading and writing into reserved DMA memory. For each board the fastest strategy is used depending if a dual-core CPU is present (Cora-Z7-10) or only a single-core CPU (Cora-Z7-07S): for the dual-core CPU the server uses one thread to receive the uploaded data and a second thread to write the data into reserved DMA memory in parallel. For the single-core CPU it is fastest to immediately write the uploaded data into reserved DMA memory using a single thread\textsuperscript{[47]}. Fig. 5b shows the corresponding times for the same data as in Fig. 5a.

The rates are calculated from $\Gamma = N\beta/(t_{\text{tot}} - t_{\text{ACK}} - t_{\text{RT}})$ where $N$ is the number of transmitted samples and $\beta = 12$ bytes per samples used for the measurement. The time $t_{\text{tot}}$ is when uploading and writing to memory is finished, and $t_{\text{ACK}}$ is the time when the server acknowledged to receive the data from the user application. The network round-trip time $t_{\text{RT}}$ is obtained during each individual measurement as the time from the acknowledge of the server ($t_{\text{ACK}}$) until the arrival of the first data at the server. We take half of $t_{\text{RT}}$ under the assumption that sending and receiving involves the same delays, which is not necessarily the case. For each datapoint we have taken at least 15 measurements and plot the mean value and standard deviation (error bar).

For small number of samples the observed uploading rate is small. This can be interpreted as a fixed delay (of order of a few 100 µs, see Fig. 5b), which the user application or the server needs to start sending or receiving the data. For
increasing number of samples, this delay becomes less important and the rate reaches a peak of about 70 – 80 MB/s at 32 × 10^3 samples (vertical dotted line) and decreases for number of samples beyond this. At 10^7 samples the uploading and writing rate is 56.5(3) MB/s (47.2(4) MB/s) for the Cora-Z7-10 (Cora-Z7-07S) board, which corresponds to a time of 2.13(1) s (2.54(2) s). This time is even faster than the typical calculation time the user application needs (about 7 s with linscript-suite) to generate this number of samples.

The peak in the rate is correlated with the receive buffer size (512 kiB) of the server. If chosen too small the decrease in the rate at higher N becomes much worse. This indicates that the overhead in handling large lists of small buffers can become significant. In this respect the Cora-Z7-10 board performs slightly better than the Cora-Z7-07S board, which is limited by a single-core CPU.

For comparison, we present another measurement where only data are uploaded, but no writing to the reserved DMA memory is done. The resulting rates for the Cora-Z7-10 (open blue circle) and Cora-Z7-07S (open orange square) board are shown in Fig. 5a and b. For the calculation of the rate, \( t_{\text{tot}} \) is now the time until all data is uploaded without writing to reserved DMA memory. For the Cora-Z7-10 board the peak uploading rate reaches about 110 MB/s which is very close to the theoretical maximum of 118.7 MB/s for Gigabit Ethernet. The Cora-Z7-07S board is with about 90 MB/s only slightly slower. In this measurement the CPU is still copying data into temporary buffers which explains the difference of the boards, and the observed decrease of the rate after the peak.

With Eq. (B1) in Appendix B we fit the measurements with a delay time and a single transmission rate (dotted curves in Fig. 5). We use the standard deviation of each data point to get more weight on the large number of samples with less noise. See Tab. I for the fit results. The numbers in the figure are the fitted rates and times for both boards when uploading and writing 10.5 × 10^6 samples to reserved DMA memory.

The observed fast uploading and writing rates confirm that the FPGA-SoC board is indeed the right choice for applications where fast cycle times are requested.

C. Auto-synchronization

Here we present the first realization of the auto-synchronization scheme proposed in Sec. II B. In particular, first tests have been done utilizing two boards connected with different trigger cable lengths and using different external clock phases. Without loss of generality, we present the synchronization of the two boards that are directly connected with the trigger line, terminated with 50Ω on the primary board side and switchable on the secondary board side from 50Ω to high impedance to reflect the pulse. In the following we omit the index \( i = 0 \) since here only one secondary board is used. For details on the theoretical analysis and the measurement of the secondary board external clock PLL phase we refer the reader to Appendix A1 and A2.

On the primary board we measure the round-trip cycle time \( N_{\text{RT}} \) of the reflected pulse, and the phase \( \phi^p \) at which \( N_{\text{RT}} \) is reduced by one, see Fig. 6a for different lengths of the trigger coaxial cable. Combining both measured values of \( N_{\text{RT}} \) and \( \phi^p \) we obtain, from Eq. (A1) in Appendix A1, the round-trip time \( t_{\text{RT}} \) shown in Fig. 6b. From a linear fit to the data (green line) we obtain the propagation delay per unit of cable length \( L \) of \( \frac{d\tau}{dt} = 4.9(4) \text{ ns/m} \), when averaged over leading and trailing edges of the pulse. This value is consistent with the expected one.

Based on a similar measurement protocol, the secondary board determines the phase \( \phi^s \) of the negative jump in \( N_{\text{det}} - N_{\text{max}} \) for the received pulse. The local clock of the second board is locked to the external clock provided by the primary one, where a short (ca. 20 cm long) cable is employed to ensure no additional phase shifts. To simulate different delays \( \Delta \tau \) of the external clock, four different auto-synchronization measurements are performed, where the external clock PLL phase of the secondary board is set to 0, 90, 180 or 270°, corresponding to \( \Delta \tau = 0, 5, 10 \) or 15 ns respectively.

![Fig. 6. Auto-synchronization result for two boards at different trigger cable lengths. a) Round-trip cycle time \( N_{\text{RT}} \) for the reflected pulse leading edge vs. detector phase. b) Pulse round-trip time \( t_{\text{RT}} \) calculated with Eq. (A1) for the trailing edge of the pulse for 12 cable lengths. c) Synchronization error as a function of cable length.](image-url)
The resulting synchronization error is verified in a final measurement for each cable length and $\Delta \tau_c$, after the auto-synchronization is finished, see Fig. [6]. For this measurement, the resulting phase $\phi_{ext}$, obtained from Eq. (A12) in Appendix A1, is added to the previously set external PLL clock phase $\Delta \phi_{ext} = 360^\circ$, which, for perfect synchronization, should be compensated by $\phi_{ext}$. Then the primary board generates a trigger pulse and waits $N_{pr} = \tau_p / T$ cycles (see Eq. (A7) and (A8) in Appendix A1), to trigger the primary board and start generating data on the bus. The secondary board starts generating data on the bus as soon as the trigger signal is detected. The synchronization error corresponds to the difference between the times at which secondary and primary boards start generating data on their own buses. The corresponding traces are recorded with an oscilloscope, see the inset of Fig. [6] and are fitted with a sigmoid function to obtain the synchronization error. See Appendix A3 for further details. In Fig. [6], each data point (error bar) represents the mean (standard deviation) of the synchronization error, measured at least five times for each of the four external clock phases ($\Delta \tau_c$). Averaging over all cable lengths, we obtain a synchronization error of $(-0.5 \pm 1.3)$ ns (red shaded area in Fig. [6]), which is much smaller than the 25 ns time resolution for the maximum possible bus output rate of 40 MHz of the board.

Finally we remark that, although the basic principle of our auto-synchronization scheme is very simple, being based on a round-trip time measurement, the details can be involved. Developing such a scheme on a FPGA-only platform is feasible, but it might be challenging and time-consuming. In turn, our FPGA-SoC board allows one to implement a simple pulse generation and detection in hardware, but to analyze the data and calculate the ideal settings to minimize the error, via the CPU, by software. In this way, the system could be quickly developed, errors corrected and the formulas implemented in software with no need to change the hardware every time. We believe that, the auto-synchronization is not only a useful feature, but it is also a perfect example of the flexibility which the FPGA-SoC approach offers.

V. CONCLUSIONS AND OUTLOOK

In conclusion, we have successfully implemented a versatile experimental control system based on a commercial, low-cost, and stand-alone FPGA-SoC board. We have demonstrated that the board can sustain bus output and input rates of up to 40 MHz and we have shown how the board can automatically synchronize with a timing error approaching 1 ns. Furthermore, we have proven the extreme flexibility, easy Ethernet connectivity, and computational power of the FPGA-SoC system, showing several examples in which the operating system, running on the board itself, is used not only to control the FPGA hardware, but also for data acquisition and analysis. Finally, we stress that no specific device driver or proprietary software, or operating system is needed to use our device, and that the whole source code to program the FPGA-SoC is freely available[52]. Although not discussed in the present work, our system can be easily extended to include the control of additional devices through the on-board USB host controller[51] or via adapter with the older GPIB standard[52], widespread in many laboratories, or to directly read data with analog-to-digital converters (ADC). We also emphasize that our design is stand-alone and lightweight, and the power consumption of less than 2 W, makes it compatible for the operation in remote locations, and even for experiments in space[53]. We believe that the auto-synchronization feature, devised and implemented in this work, will also help several experimental setups on ground with growing complexity: for instance, setups which must bridge large distances to challenge relativity[54] to detect gravitational waves with large-scale atom interferometers[55], and to measure difference of gravitational red-shift between two separated atomic lattice clock[56]. Finally, our architecture, thanks to the rich features and flexibility offered by the new FPGA-SoC board, may find application in various research fields, extending well beyond our original purpose of controlling AMO physics experiments.

ACKNOWLEDGMENTS

We thank Jacopo Catani for fruitful discussions, borrowing equipment and careful reading of the manuscript, Roberto Concas and Fabio Corti for machining and soldering a prototype buffer card, Giacomo Mazzamuto for help with github, and all members of the Quantum Gases Group at LENS, in particular Leonardo Fallani and Daniele Tusi and the Yb team for testing the boards in their experiment. This work was supported by the ERC through grant No. 637738 PoLiChroM and by the Italian MIUR through the FARE grant No. R168HMHFYM P-HELiCS. N.P. acknowledges support from European Research Council, Grant No. 772126 (TIC-TOGRAV).

The authors declare that they have no competing interests.

DATA AVAILABILITY STATEMENT

| AVAILABILITY OF DATA | STATEMENT OF DATA AVAILABILITY |
|----------------------|------------------------------|
| Data openly available in a public repository that issues datasets with DOIs | The data that support the findings of this study are openly available at https://doi.org/10.5281/zenodo.4893285 |

Appendix A: Auto-synchronization

In Sec. A1 we present the full model of the auto-synchronization scheme outlined in Sec. II B and in Sec. A2 we show additional data for the first implementation presented in Sec. IV C. In Sec. A3 the fitting function is presented.
which is used to obtain the synchronization error shown in Fig. 6c in Sec. IV C. In Sec. A 4 sample detector signals are shown.

1. Theoretical Model

A graphical representation of all the quantities and delays involved in the synchronization scheme is presented in Fig. 7 for the primary and secondary boards. The measurement on the primary board gives for each secondary board for the primary and secondary boards. The measurement on the primary board generates the pulse and waits until detection of the reflected signal after a propagation time of \(2 \times \tau_{p}^{i} \) (light gray). Delays involving the generation \( \theta_{g}, \) and the detection \( \theta_{d}, \) of the pulse have to be added for the calculation of the round-trip time \( t_{RT} = N_{RT}^{p} T + \Delta t_{RT}^{p}, \) with \( T \) the clock cycle time. Lower part: the secondary board \( i \) detects the pulse after the propagation time \( \tau_{p}^{i} \) (dark gray) and it is assumed the same delays as for the primary board. The delay of the local clock of the secondary board with respect to the primary board is \( \Delta t_{RT}^{i} \) and can be calculated from the difference of \( \phi_{p}^{i} - \phi_{p}^{i}. \) The measured quantities \( N_{RT}^{i}, \Delta t_{RT}^{i} \) and \( \Delta t_{RT}^{i} \) are indicated in red. The width of the pulse \( w_{p} \) is changing during the propagation due to dispersion, and affects the measurement if this involves both leading and trailing edges of the pulse (not shown here).

From the propagation time \( \tau_{p}^{i}, \) the phase \( \phi_{p}^{i} \) can be calculated:

\[
\phi_{p}^{i} = \left( \left( \tau_{p}^{i} + t_{g} \right) \% T / T \right) 360^{\circ} / T
\]

The symbols \% and // represent modulo and integer division, respectively. The factor \( \left( \tau_{RT}^{i} \% T / T \right) \) adds \( T/2 \) to \( \phi_{p}^{i} \) when \( \phi_{p}^{i} < \phi_{p}^{i}. \) \( \phi_{p}^{i} \) is the expected phase of the pulse which the secondary board would measure for \( \Delta t_{RT}^{i} = 0. \) The actual pulse phase which the secondary board obtains is:

\[
\phi_{p}^{i} = \left( \Delta t_{RT}^{i} - t_{g} \right) 360^{\circ} / T ,
\]

TABLE I. Used constants for the auto-synchronization. The measured standard deviation is given in brackets.

| name          | value         | remark                  |
|---------------|---------------|-------------------------|
| \( t_{0} - t_{d} \) | 205(1) ns     | offset from linear fit Fig. 6a               |
| \( t_{d} \)   | -2(1) ns      | offset from linear fit Fig. 6b               |
| \( \phi_{p} \) | 25(1)°        | measured \(^a\)              |
| \( \phi_{p}^{\text{crit}} \) | 180(20)°     | measured \(^b\)              |
| \( \theta_{0} \) | 20°          | fine-adjusted manually to minimize the error |
| \( \theta_{m} \) | 90°          | chosen \(^c\)               |
| \( \theta_{add} \) | 70°          | chosen                  |
| \( \Delta \phi_{p}^{\text{crit}} \) | 20°          | chosen \(^c\)               |
| \( \delta \phi_{p}^{\text{crit}} \) | 30°          | chosen \(^c\)               |

\(^a\) Obtained from earlier measurements.  
\(^b\) At \( f_{s} = 50 \text{ MHz} \).  
\(^c\) Error is smaller than \( \Delta \phi_{p}^{\text{crit}} \) but was not systematically measured.

\( \tau_{g} \) is at a small and positive detector clock, the measured \( \Delta \phi_{p} \) increments by one cycle. \( \phi_{p} \) is at a small and positive detector clock, the measured \( \Delta \phi_{p} \) increments by one cycle. \( \phi_{p} \) is at a small and positive detector clock, the measured \( \Delta \phi_{p} \) increments by one cycle. \( \phi_{p} \) is at a small and positive detector clock, the measured \( \Delta \phi_{p} \) increments by one cycle. \( \phi_{p} \) is at a small and positive detector clock, the measured \( \Delta \phi_{p} \) increments by one cycle. \( \phi_{p} \) is at a small and positive detector clock, the measured \( \Delta \phi_{p} \) increments by one cycle. \( \phi_{p} \) is at a small and positive detector clock, the measured \( \Delta \phi_{p} \) increments by one cycle. \( \phi_{p} \) is at a small and positive detector clock, the measured \( \Delta \phi_{p} \) increments by one cycle. \( \phi_{p} \) is at a small and positive detector clock, the measured \( \Delta \phi_{p} \) increments by one cycle. \( \phi_{p} \) is at a small and positive detector clock, the measured \( \Delta \phi_{p} \) increments by one cycle. \( \phi_{p} \) is at a small and positive detector clock, the measured \( \Delta \phi_{p} \) increments by one cycle. \( \phi_{p} \) is at a small and positive detector clock, the measured \( \Delta \phi_{p} \) increments by one cycle. \( \phi_{p} \) is at a small and positive detector clock, the measured \( \Delta \phi_{p} \) increments by one cycle. \( \phi_{p} \) is at a small and positive detector clock, the measured \( \Delta \phi_{p} \) increments by one cycle. \( \phi_{p} \) is at a small and positive detector clock, the measured \( \Delta \phi_{p} \) increments by one cycle. \( \phi_{p} \) is at a small and positive detector clock, the measured \( \Delta \phi_{p} \) increments by one cycle. \( \phi_{p} \) is at a small and positive detector clock, the measured \( \Delta \phi_{p} \) increments by one cycle. \( \phi_{p} \) is at a small and positive detector clock, the measured \( \Delta \phi_{p} \) increments by one cycle.
The secondary board:

$\phi_{\text{ext}}^i = -\Delta \varepsilon^i \frac{360^\circ}{T} = \phi_p^i - \phi_s^i - \phi_0 + \xi(\phi_p^i)$.

(A4)

This is the full relation corresponding to Eq. 4 in Sec. II B.

The additional phase factor $\phi_0$ is manually adjusted to minimize the synchronization error. This corrects an eventual mismatch in $t_d$ between the primary and secondary board and corrects for our choice to measure $\phi_p^i$ on the trailing edge and $\phi_s^i$ on the leading edge of the pulse. When $\phi_p^i$ happens to be close to the critical phase $\phi_p^{\text{crit}}$, the resulting synchronization error shows random jumps by $T$ in either positive or negative direction. The security phase $\xi(\phi_p^i)$ is introduced to avoid this region which we define as $\pm \Delta \phi_p^{\text{crit}}$ around $\phi_p^{\text{crit}}$. $\xi(\phi_p^i)$ is nonzero only if $\phi_p^i$ is inside this region and adds in this case $\pm \Delta \phi_p^{\text{crit}}$ to $\phi_{\text{ext}}$ according to:

$\xi(\phi_p^i) = \begin{cases} 
\xi \phi_p^i \text{ for } |\phi_p^i - \phi_p^{\text{crit}}| < \Delta \phi_p^{\text{crit}} \\
0 \text{ otherwise }
\end{cases}$.  

(A5)

The function $\text{sign}(x)$ gives $\pm 1$ depending on the sign of $x$. When $\xi(\phi_p^i)$ is nonzero, the synchronization error increases by about $\Delta \phi_p^{\text{crit}} T / 360^\circ \approx 1.7$ ns, but avoids uncontrollable outliers. The data points at 20 m and 31.3 m in Fig. 3 and 4 represent such cases where the measured $\phi_p$ is about $\pm 15^\circ$ near $\phi_p^{\text{crit}}$ (see green shaded region in Fig. 3). Note, that this correction depends only on the measured $\phi_p$ and is automatically applied by the boards. For applications where the added synchronization error is unacceptable, the board can give a warning to the user and a slightly shorter or longer trigger cable might be used.

The detection clock phase $\phi_d^i$, is used not only during the auto-synchronization measurement, but also afterwards to detect the pulse on the secondary boards. It does not directly influence the synchronization error, but it is set such that the detection of the trigger pulse happens neither close to the rising or falling edges of the pulse, nor to the rising edge of the bus clock. This ensures reliable timing but might require one additional cycle to wait. $\phi_d^i$ is set at least $\phi_{\text{add}}$ after the arrival of the pulse:

$\phi_d^i = \begin{cases} 
\phi_{\text{add}} & \text{if } \phi_d^i \leq \phi_m \\
\phi_m & \text{if } \phi_m < \phi_d^i \leq 360^\circ - \phi_m \\
\phi_d^i & \text{if } 360^\circ - \phi_m < \phi_d^i \leq 360^\circ + \phi_m \\
\phi_d^i - 360^\circ & \text{otherwise }
\end{cases}$.  

(A6)

The phase margin $\phi_m$ ensures that $\phi_d^i$ has a phase outside of the region $[-\phi_m \ldots + \phi_m]$ to avoid that the detection of the pulse is too close to the bus clock rising edge where the timing would be unreliable. It was chosen to be significantly larger than $\phi_+$. The last parameters to be determined are the number of cycles each board has to wait before it can start output data on the bus. For this the propagation number of cycles $N_p^i$ have to be calculated:

$N_p^i = (c_i + t_g + t_d) / T + \left\{ \begin{array}{ll} 
N_0 & \text{for } \phi_{\text{det}}^i \leq 360^\circ - \phi_m \\
N_0 + 1 & \text{otherwise .}
\end{array} \right.$  

(A7)

Here the experimentally determined constant integer $N_0 \in \mathbb{Z}$ adds a few cycles to account for the cycles needed to start the output. The +1 accounts for the above mentioned case, that the detection clock was adjusted to detect the pulse one cycle later, to ensure reliable timing. With the knowledge of all $N_p^i$ of the secondary boards the waiting number of cycles of the primary and secondary boards can be calculated:

$N_{\text{w prim}} = \max_j(N_p^j)$

$N_{\text{w}} = N_{\text{w prim}} - N_p^i$.  

(A8)

The waiting number of cycles of the primary board is the largest of the $N_p^i$, i.e. $\max_j(N_p^j)$, and each secondary board has to wait less until the last board does not need to wait.

The first demonstration of this scheme is presented in Sec. IV C and Fig. 6 shows the results. In Fig. 6 in the next section the different phases are shown for the same data.

2. Measured external clock phase

Fig. 8 shows the phases $\phi_p$ (green circles), $\phi_s$ (blue squares) and $\phi_{\text{ext}}$ (orange diamonds) for the corresponding data presented in Fig. 6 in Sec. IV C. The linear fit (modulo $360^\circ$) of $\phi_p$ vs. cable length (blue dashed line) gives a propagation delay per unit length of $\frac{\Delta \phi_p}{\Delta L} = 4.9(3)$ ns/m (averaged over leading and trailing edge of the pulse), which is the same as the one measured on the primary board (see Fig. 3). When $\Delta \tau_p = 0$, the offset of the linear fit gives the detection delay of the pulse $t_d$. For nonzero $\Delta \tau_p$ the offset is shifted accordingly.

In Fig. 9 we show the synchronization error as a function of the sum $\phi_{\text{ext}} + \Delta \tau_c - \frac{360^\circ}{T}$, i.e. how well the measured $\phi_{\text{ext}}$ compensates the externally applied clock delay $\Delta \tau_c$ (see Eq. (44)). A linear fit (orange dashed line) gives a slope of $80(1)$ ps/degree which is slightly larger than the expected $20 \text{ps}/\text{degree}$ and the offset of $263(4)^\circ$ indicates that there is an additional unaccounted phase shift on the external clock. The used 20 cm long clock cable would introduce a phase shift of only about $20^\circ$ at the 50 MHz external clock frequency used for this measurement. Additional phase shifts can come from input and clock buffers and propagation delays inside of the FPGA. The main contribution to the synchronization error can be attributed to the small difference of the measured pulse propagation delay per unit length $\frac{\Delta \phi_p}{\Delta L}$ between the primary board $\tau_p$ and the secondary board $\tau_s$. To compensate for this we have chosen to use the leading edge of the pulse on the primary board and the trailing edge on the secondary board. But with this choice the pulse width needs to be compensated (using $\phi_0$), which we do at the moment only
FIG. 8. a) Example phases for $N_c = 360^\circ$ corresponding to the data in Fig. 7: primary pulse phase ($\varphi_p$, green circles), secondary pulse phase ($\varphi_s$, blue squares) and external PLL phase ($\varphi_{ext}$, orange diamonds). The dashed (blue) line is a linear fit modulo $360^\circ$ through $\varphi_p$ and gives $\frac{d\varphi_p}{dt} = 4.9(3)$ ns/m. For cable lengths 20 m and 31.3 m, the phase $\varphi_s$ is within $\pm 20^\circ$ of $\varphi_p$ (green shaded area) and the security phase is set nonzero $\varphi_p = \mp 30^\circ$. This causes that $\varphi_{ext}$ is shifted away from the ideal value but ensures that the synchronization error, although slightly increased, does not jump arbitrarily by $\pm T$. b) Correlation between the error of the external clock phase and measured synchronization error plotted for all $\tau$ (different colors). The dashed (orange) line is a linear fit which gives a slope of 80(1) ps/degree and an offset of 263(4)°.

under the assumption that it does not change for varying cable length. This assumption is not true due to the dispersion of the pulse. Nevertheless, even with the present scheme, the resulting synchronization error in Fig. 6 is already very low.

3. Fitting function for the synchronization error

Here we present the fitting function used to fit the oscilloscope traces shown in the inset of Fig. 6. For each trace the auto-synchronization was performed as described in Sec. IV C. After this, in order to measure the resulting synchronization error, another pulse is generated by the primary board and it waits the calculated waiting time $N_{w}^{prim}$ and generates a signal on an auxiliary I/O pin which is recorded by an oscilloscope (blue traces in inset of Fig. 6). Each trace consists of 14 data points with a resolution of 2 ns. After the secondary board detects the pulse, it immediately generates a signal on an auxiliary I/O pin which is used to trigger the oscilloscope and is recorded (orange traces) together with that of the primary board. The saved traces are fitted with a sigmoid function which is constructed from a piecewise defined linear slope $s(t, t_0, k, y_-, y_+)$ and is smoothed with a Gaussian kernel $g(t, \sigma)$:

$$g(t, \sigma) = \frac{1}{\text{norm}} e^{-\frac{t^2}{2\sigma^2}}$$

$$\mu = \frac{y_- + y_+}{2}, \quad \nu = \frac{y_+ - y_-}{2k}$$

$$s(t, t_0, k, y_-, y_+) = \begin{cases} y_- & t < t_0 \\ \mu + (t - t_0)k & |t - t_0| \leq \nu \\ y_+ & t > t_0 \end{cases}$$

$$f(t, t_0, k, \sigma, y_-, y_+) = s(t, t_0, k, y_-, y_+) * g(t, \sigma).$$

The symbol $*$ means the discrete convolution with fixed steps in time and the Gaussian is normalized (norm) such that the sum over the discrete kernel entries is one. The function $f(t, t_0, k, \sigma, y_-, y_+)$ smoothly changes from the value $y_-$ for $t < t_0$ to the value $y_+$ for $t > t_0$. The slope $k$ and the width $\sigma$ of the Gaussian define how fast is the change between the extremes around the time $t_0$.

Each trace is fitted individually with $f(t, t_0, k, \sigma, y_-, y_+)$ with free parameters $t_0$, $k$, $y_-$ and $y_+$ and $\sigma = 2$ ns is kept fixed. The resulting synchronization error is the difference of the fitted $t_{0}^{rec}$ of the secondary board minus that one of the primary board $t_{0}^{prim}$.
4. Measured detection signal

Here we show examples of trigger signals and the 
detection signal for varying detector phase used for the auto-
synchronization described in Sec. IV A. The schematics of 
the pulse generation and detection electronics can be found 
Cora-Z7-10 and Cora-Z7-07S board (-10 and -07S in table headings 
for demonstration the possibility to interrupt the ex-
ternal event, like waiting until the atom number reaches a 
maximum possible bus output rate, but are as well an excel-
sent tool to verify the efficiency of the driver. Any delays in 
time-critical parts, like the interrupt service routine or where 
DMA buffers are updated, severely impact the DMA trans-
smission rate. For example, output of text messages for debug-
ging purposes cannot be done since the serial transmission of 
the text via USB to a host computer is too slow and would 
block the driver.

Appendix B: Data rate fitting function

Here we give the function used for modeling the data transmission rates presented in Fig. 4 and Sec. IV A and the data uploading rates presented in Fig. 5 and Sec. IV B. The fit results can be found in Tab. II.

The model function gives the resulting rate \( \Gamma(N) \) as a function of number of samples \( N \) and includes a delay time (latency) \( \tau \) and two data transmission rates where \( \Gamma_0 \) is active for \( N \leq N_\Theta \) and \( \Gamma_1 \) active for \( N > N_\Theta \):

\[
\Gamma(N) = \frac{1}{\frac{\tau}{N} + \frac{\Theta(N-N_\Theta)}{\Gamma_0} + \frac{\Theta(N-N_\Theta)}{\Gamma_1}}
\]

\[
\Theta(x) = \begin{cases} 
0 & \text{for } x \leq 0 \\
1 & \text{otherwise} 
\end{cases}
\]

The value \( \beta = 12 \) bytes per sample for this measurement. The delay takes into account that data cannot be transmitted immediately after the start signal has been given. The two rates are used to model that data transmission can run at different speeds, for example when FIFO buffers are involved.

For the measurement of the TX DMA rate an eventual delay cannot be detected and it was set to \( \tau = 0 \). The initial rate was set to the maximum possible \( \Gamma_0 = \Gamma_{\text{max}} \) and the second rate \( \Gamma_1 \) is left as a fitting parameter. The threshold number of samples is set to fixed \( N_\Theta = 4 \) since this is the smallest number of samples which can be transmitted. This is because we have chosen to use a 16 byte wide (128 bits) data stream and \( \beta = 12 \) bytes, which have 48 bytes as the least common multiple, i.e. 4 samples. Unused samples are marked by the driver with a “no-operation” (NOP) bit, such that non-multiple number of samples of 4 are no problem. For the measurement of the RX DMA rate and the data uploading rate, the fitting parameters are the delay \( \tau \) and the rate \( \Gamma_0 \). No second rate is needed. For the measurement of the RX FIFO rate \( \Gamma_1 \) and \( N_\Theta \) are fitting parameters, the delay and initial rate is again set to 0 and \( \Gamma_{\text{max}} \) respectively.

Note that the DMA rate measurements give not only the maximum possible bus output rate, but are as well an excellent tool to verify the efficiency of the driver. Any delays in time-critical parts, like the interrupt service routine or where the DMA buffers are updated, severely impact the DMA transmission rate. For example, output of text messages for debugging purposes cannot be done since the serial transmission of the text via USB to a host computer is too slow and would block the driver.

Appendix C: Start- and stop trigger

In Fig. 10 we present a measurement of the start trigger and the cycling method of the board. In addition, we implemented for demonstration the possibility to interrupt the execution of the sequence when the start trigger signal is reset after the board has been started. This might be useful to manually check the state of the experiment, or to wait for some external event, like waiting until the atom number reaches a
certain value. The experimental sequence consists of an analog output performing a triangular ramp (orange) which is executed repeatedly in cycling mode. The dotted lines indicate the beginning of each cycle. A waveform generator provides the trigger signal (blue). See Fig. 10b for the unperturbed experiment: without the start-stop trigger activated, there is no relation between the trigger and the ramp, which we show for 5 realisations of the experiment. In Fig. 10b we show the result when the start-stop trigger is activated which is starting the execution of the ramp and then interrupting it as long as the trigger signal is low. We have again repeated this measurement 5 times and now all repetitions overlap.

Appendix D: Resource utilization

Tab. III gives a summary of the used resources of the PL part and shows that we do not use all of the available resources although the FPGA is relatively small. This allows to implement further improvements or customization in case it is needed.

TABLE III. Used resources for Cora Z7-10 (Zynq-7010) and Cora Z7-07S (Zynq-7007S) FPGA-SoC boards: Flip-flops (FF) store single-bit data, lookup tables (LUT) are used to represent logic operations, block-RAM (BRAM) is a much larger (36 kbit) collection of flip-flops, and mixed-mode manager (MCMC), are phase-locked loops (PLL) but allow dynamic phase shifting. We use neither classical PLLs nor digital signal processing (DSP) cells.

| device   | FF | LUT | BRAM | MCMC | PLL | DSP |
|----------|----|-----|------|------|-----|-----|
| Z7-10    | available | 35200 | 17600 | 60 | 2 | 2 | 80 |
|          | used percent | 13275 | 9824 | 38 | 2 | 0 | 0 |
| Z7-07S   | available | 28800 | 14400 | 50 | 2 | 2 | 66 |
|          | used percent | 13274 | 9825 | 38 | 2 | 0 | 0 |

FIG. 10. Demonstration of a start and stop trigger option in cycling mode. a) Analog output triangular ramp (orange) running with 4 μs per sample in cycling mode. The FPGA board is freely running without waiting for the trigger signal (blue). b) Same ramp but with start and stop trigger enabled. Both panels show the accumulated signal for 5 repetitions (number in brackets of labels). The vertical dotted lines indicate the beginning of each experimental cycle.

1National Instruments Digital Reconfigurable I/O Device, https://www.ni.com/en-us/shop/hardware/products/digital-reconfigurable-io-device.html
2ARTIQ, open-source experimental control system, https://m-labs.hk/experiment-control/artiq/
3A. Keshet and W. Ketterle, Rev. Sci. Instrum. 84, 015105 (2013)
4G. Ramola, A versatile digital frequency synthesizer for state-dependent transport of trapped neutral atoms, Master thesis (2015) Rheinischen Friedrich-Wilhelms-Universität Bonn.
5T. Pruttivarasin and H. Katori, Rev. Sci. Instrum. 86, 115106 (2015).
6Y. Du, W. Li, Y. Ge, H. Lu, K. Deng, and Z. Lu, Rev. Sci. Instrum. 88, 096103 (2017).
7S. Donnellan, I. R. Hill, W. Bowden, and R. Hobson, Rev. Sci. Instrum. 90, 043101 (2019).
8S. W. Mattingly and F. Skiff, Rev. Sci. Instrum. 89, 043508 (2018).
9S. Shu, L. Wang, D. Liu, C. Miewen, Y. Zhang, L. Jiaron, and F. Ji, Rev. Sci. Instrum. 89, 10.1063/1.5035364.
10E. Perego, M. Pomponio, A. Detti, L. Duca, C. Sias, and C. E. Calosso, Rev. Sci. Instrum. 89, 113116 (2018).
11S. J. Yu, E. Fajae, L. Q. Liu, D. J. Jones, and K. W. Madison, Rev. Sci. Instrum. 89, 025107 (2018).
12D. Risté, M. Dukalski, C. A. Watson, G. de Lange, M. J. Tiggelman, Y. M. Blanter, K. W. Lehnert, R. N. Schouten, and L. DiCarlo, Nature 502, 350 (2013).
13J. Lamb, J. Colless, J. Hornibrook, S. Penna, S. Waddy, M. Frechtlting, and D. Reilly, Rev. Sci. Instrum. 87, 014701 (2016).
14H. Homüls, S. Visser, B. Patra, G. Ferrari, E. Prati, F. Sebastiany, and E. Charbon, Rev. Sci. Instrum. 88, 045103 (2017).
15X. Qin, W. Zhang, L. Wang, Y. Zhao, Y. Tong, X. Rong, and J. Du, IEEE Trans. Instrum. Meas. 69, 1127 (2020).
16Y. Xu, G. Huang, J. Balewski, R. Naik, A. Morvan, B. Mitchell, K. Nowrouzi, D. I. Santiago, and I. Siddiqi, arXiv (2021) arxiv.org/abs/2101.00071.
17S. Habinc, Suitability of reprogrammable FPGAs in space applications (Gaisler Research, 2002) http://microelectronics.esa.int/techno/fpga_002_01-0-4.pdf
18A. Bertoldi, C.-H. Feng, H. Eneriz, M. Carey, D. S. Naik, Z. Junca, Z. Zou, D. O. Sabulsky, B. Canuel, P. Bouyer, and M. Prevedelli, Rev. Sci. Instrum. 91, 033203 (2020).
19CERN, The White Rabbit Project, https://white-rabbit.web.cern.ch/
20Cora-Z7-10 and Cora-Z7-07S development boards from Digilent Inc., https://reference.digilentinc.com/programmable-logic/cora-z7/start.
21DE10-Nano Kit from Terasic Inc., https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=167&ItemNo=1046.
22The source code, electronic schemes and Gerber files, the instructions for installation of the software and the compilation of the sources can be found at https://github.com/1MQ-quantum-FPGA-SoC-experiment-control.
23C. E. Cummings, “Clock Domain Crossings (CDC) Design & Verification Techniques Using System Verilog,” (2008), SNUG 2008, Boston. https://www.sunburst-design.com/papers/CummingsSNUG2008Boston_CDC.pdf
24Second release of AMBA AXI and ACE Protocol Specification, Issue E, 22 February 2013. The Advanced extensible Interface (AXI) protocol is a part of ARM Advanced Microcontroller Bus (AMBA) structure. https://developer.arm.com/documentation/tn0022/l/latest/
25Xilinx AXI DMA v7.1 LogicCORE IP product guide. PG021, June 14 2019, https://www.xilinx.com/support/documentation/ip documentation/axi_dma/v7_1/pg021_axi_dma.pdf
26C. E. Cummings, “Simulation and Synthesis Techniques for Asynchronous FIFO design,” (2002), SNUG 2002, San Jose, https://www.sunburst-design.com/papers/CummingsSNUG2002_SynCh_FIFOpdf.pdf
The measured \( \Gamma_{\text{sample}} \) corresponds to a maximum \( \Gamma_{\text{sample}} \) of 42 MHz (28 MHz) for the 8 (12) bytes per sample versions. The given rates apply independently for data output and input on the bus and for simultaneous output and input (if the bus supports).

IEEE 802.3ab (1999), Gigabit Ethernet, 1000BASE-T with TCP/IP over Ethernet (II) protocol efficiency of 95\% for 1460 bytes payload per frame of 1538 bytes.

M. Endres, H. Bernien, A. Keesling, Levine, E. R. Anschuetz, A. Krajenbrink, C. Senko, V. Vuletic, M. Greiner, and M. D. Lukin, Science 354, 1024 (2016) https://science.sciencemag.org/content/354/6315/1024.full.pdf

C. Sahin, P. Geppert, A. Mullers, and H. Ott, New J. Phys. 19, 123005 (2017)

The change in the rate between using a single or two threads on both boards is only about 10\%.

For cable lengths < 3 m the actual setup cannot detect the round-trip time since the reflected pulse is too close to the generated one. However, this situation is automatically detected and with the proposed scheme and further technical improvements shorter cables should be detectable.

Tasker RG58 CU coaxial cable specification gives velocity factor 0.66, corresponding to a propagation delay of 5.05(4) ns/m. See https://www.tasker.it/db_files/products/2760447e2.pdf

For the measurement on the secondary board the pulse is not reflected to avoid interference of the incoming with the reflected pulse. However, we have not observed a difference in the measurement result.

General purpose interface bus (GPIB), IEEE 488.2, standards.ieee.org/standard/488_2-1992.html

L. Liu, D.-S. Lu, W.-B. Chen, T. Li, Q.-Z. Qu, B. Wang, L. Li, W. Ren, Z.-R. Dong, J.-B. Zhao, W.-B. Xia, X. Zhao, J.-W. Ji, M.-F. Ye, Y.-G. Sun, Y.-Y. Yao, D. Song, Z.-G. Liang, S.-J. Hu, D.-H. Yu, X. Hou, W. Shi, H.-G. Zhang, J.-F. Xiang, X.-K. Peng, and Y.-Z. Wang, Nat. Commun. 9, 2760 (2018)

D. C. Aveline, J. R. Williams, E. R. Elliott, C. Dutenhofer, J. R. Kellogg, J. M. Kohel, N. E. Lay, K. Oudhiri, R. F. Shotwell, N. Yu, and R. J. Thompson, Nature 582, 193 (2020)

M. D. Lachmann, H. Ahlers, D. Becker, A. N. Dinkelaer, J. Grosse, O. Hellmig, H. Müntinga, V. Schkolnik, S. T. Seidel, T. Wendrich, A. Wenzlowski, B. Carrick, N. Gaaloul, D. Lüdtke, C. Braxmaier, W. Emmert, M. Krutzik, C. Lümerzahl, A. Peters, W. P. Schleich, K. Sengstock, A. Wicht, P. Windpassinger, and E. M. Rasel, Nat. Commun. 12, 1317 (2021)

B. Hensen, H. Bernien, A. E. Dréau, A. Reiserer, N. Kalb, M. S. Blok, J. Ruitenberg, R. F. L. Vermeulen, R. N. Schouten, C. Abellán, W. Amaya, V. Brunner, M. W. Mitchell, M. Marshall, D. J. Twitchen, D. Elckous, S. Wehner, T. H. Taminiau, and R. Hanson, Nature 526, 682 (2015)

P. W. Graham, J. M. Hogan, M. A. Kasevich, and S. Rajendran, Phys. Rev. Lett. 110, 171102 (2013)

B. Canuel, A. Bertoldi, L. Amand, E. Pozzo di Borgo, T. Chantair, D. Quigny, M. Dovale Alvarez, B. Fang, A. Freise, R. Geiger, J. Gillot, S. Henry, J. Hinderer, D. Holleville, J. Junca, G. Lefèvre, M. Merzougui, P. Bouyer, Sci. Rep. 110, 14064 (2018)

M. Takamoto, I. Ushijima, N. Ohmae, T. Yahagi, K. Kokado, H. Shinkai, P. Bouyer, C. Lämmerzahl, A. Peters, W. P. Schleich, K. Sengstock, A. Wicht, P. Windpassinger, and E. M. Rasel, Nat. Commun. 12, 1317 (2021)

If \( \phi \sim \phi \), the measurement is not reliable due to its sensitivity to noise.

This choice was motivated to have similar \( \Delta \tau \) for the measurements of the primary and secondary board. The average in \( \Delta \tau \) for the leading and trailing edge of the pulse is the same for both boards, but the primary board shows a larger discrepancy between the values obtained for the two edges. The difference is caused by the dispersion of the pulse. \( \phi \) corrects the phase shift introduced by half of the pulse width \( \Delta \tau \) (see Fig. 1) but does not correct for the changing width along the path.

The value of \( \Delta \tau \) (see Tab. 1) has been determined experimentally, but there might be a dependence with our choice of parameters. Its exact origin has not been investigated.

We do not use the feedback option which cancels such phase shifts.

When fitting \( \sigma \), the correlation to the slope \( k \) causes that for some traces the fit has problems to converge and attains big errors.

In cycling mode the board repeats the experimental sequence for a programmed number of times or infinitely until a stop command is sent.