Comparison of phonon scattering in nanowire field effect transistors with Si, GaAs and InGaAs cores using the NEGF formalism

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Abstract.
Using the Non-equilibrium Green's Function (NEGF) formalism, the impact of electron-phonon scattering on the performance of different core nanowire field effect transistors (NWFETs) has been investigated. Three core materials have been considered: Si, GaAs and InGaAs. The effective mass approximation has been used, with masses extracted from tight-binding simulations. The I_D-V_G characteristics at low and high drain bias are shown. It was found that at low drain bias, scattering caused a 86%, 72% and 50% percentage reduction in the current at high gate bias in the Si, GaAs and InGaAs core, respectively. The phonon-limited mobility and percentage tunnelling have also been calculated.

1. Introduction
Gate-all-around nanowire field effect transistors (NWFETs) are a likely contender to succeed FinFETs. They have strong electrostatic integrity and good scaling properties, with 6 nm channel lengths achievable. The introduction of III-V channel materials such as GaAs and InGaAs are of interest due to their high mobility. In this work, ballistic and scattering simulations of n-channel Si, GaAs and In0.3Ga0.7As, 2.2×2.2 nm² and 4.2×4.2 nm² cross-section NWFETs with a 6 nm channel length are studied. The source and drain of the NWFETs are doped at 10²⁰ cm⁻³ and the channel is undoped. A schematic of the 2.2×2.2 nm² cross-section NWFET can be seen in figure 1. All the relevant scattering mechanisms involving acoustic, optical and polar optical phonons have been included. The scattering parameters were taken from ref. [1].

![Figure 1. Schematic of 2.2×2.2 nm² cross-section, 6 nm channel NWFET.](image-url)
2. Theory
This study uses the Non-equilibrium Green’s Function (NEGF) formalism. Within the NEGF formalism one-particle electronic Green’s functions, \( G \), are used. The retarded Green’s function, \( G_r \), is given by
\[
G_r(E) = \left[ E1 - H - \Sigma(E) \right]^{-1}
\]
where \( H \) is the Hamiltonian of the system. Within the effective mass approximation the Hamiltonian is given by
\[
H_\nu(\vec{r}) = -\frac{\hbar^2}{2} \nabla_i \left( \frac{1}{m_\nu} \right) \nabla_j + V(\vec{r})
\]  
(1)

At these scales bulk masses are not valid, so new confinement effective masses have been calculated using the results of tight-binding simulations, which capture the dependence of the bandstructure on the cross-section of the nanowire [2].

3. Results
In this section, the \( I_D-V_G \) characteristics at low and high drain bias are presented. The sub-threshold slope, percentage reduction in the current due to scattering and the percentage tunnelling are also studied. At the end of this section, the phonon-limited mobility is briefly discussed.

Figure 2. \( I_D-V_G \) characteristics at low drain bias, \( V_D = 1 \) mV, for Si, GaAs and InGaAs for the (a) 2.2\( \times \)2.2 nm\(^2\) (b) 4.2\( \times \)4.2 nm\(^2\) cross-section NWFETs. The ballistic simulations are denoted by the solid lines and the scattering simulations by the dotted lines.

Figure 2 shows the \( I_D-V_G \) characteristics at low drain bias for all the simulated devices. For both cross-sections, the highest current is in the Si devices. For the 2.2\( \times \)2.2 nm\(^2\) cross-section devices, the scattering sub-threshold slope is 76, 69 and 71 mV/dec for the Si, GaAs and InGaAs cores respectively. For the 4.2\( \times \)4.2 nm\(^2\) cross-section devices, the sub-threshold slope is 99, 109 and 112 mV/dec for scattering in the Si, GaAs and InGaAs cores respectively. The ideal value for the sub-threshold slope is approximately 60 mV/dec. A higher sub-threshold slope indicates worse electrostatic control.

In the 2.2\( \times \)2.2 nm\(^2\) cross-section, there is a 86%, 72% and 50% percentage reduction in the current due to scattering at high \( V_G \) for the Si, GaAs and InGaAs cores respectively. For the 4.2\( \times \)4.2 nm\(^2\) cross-section devices, there is a 58%, 40% and 37% percentage reduction in the current due to scattering at high \( V_G \) for the Si, GaAs and InGaAs cores respectively. The greater percentage reduction in the current for 2.2\( \times \)2.2 nm\(^2\) NWFETs is due to the strength of electron-phonon coupling increasing with decreasing cross-section.

For the 2.2\( \times \)2.2 nm\(^2\) cross-section devices at both low and high drain bias, the current is much lower in the III-V NWFETs. However, in the 4.2\( \times \)4.2 nm\(^2\) cross-section NWFETs the current in the III-V devices is much closer to that of the Si device, approaching the same value for the
ballistic on-current. The much lower current in the III-V 2.2×2.2 nm² NWFETs is because of the strong confinement. In bulk GaAs and InGaAs, the order of valleys in increasing energy is Γ, L then X. For the III-V 2.2×2.2 nm² cross-section devices the low mass Γ-valley becomes raised in energy such that it’s higher than the heavier L and X-valleys, whereas in the III-V 4.2×4.2 nm² cross-section NWFETs, the valleys have the same order as bulk. The elevation the Γ-valley results in much lower current in the III-V 2.2×2.2 nm² devices. The greater degradation of the sub-threshold slope with increasing cross-section for the III-V NWFETs is because of the lower mass Γ-valley beginning to contribute more to the transport as the cross-section increases.

In order to understand why the current is generally lower in the III-V NWFETs, the percentage tunnelling must be considered. The amount of percentage tunnelling is mostly determined by the effective mass and the size of the potential barrier. For the 2.2×2.2 nm² cross-section NWFETs, the Si device has the lowest percentage tunnelling as it has a smaller barrier (due to the poorer electrostatic control) and the main valleys contributing to the transport have smaller effective masses than the III-V devices (as in the 2.2×2.2 nm² III-V devices the contribution of the low mass Γ-valley has been reduced as it is elevated). The scattering percentage tunnelling at low drain bias and at high V_G is 11%, 54% and 45% for the Si, GaAs and InGaAs cores respectively. The higher percentage tunnelling in the III-V devices results in a lower total current. The lower tunnelling current in the Si devices contributes to the higher current reduction due to scattering than the III-V NWFETs.

For the 4.2×4.2 nm² cross-section devices the scattering percentage tunnelling at low drain bias and high V_G is 3%, 12% and 9% in the Si, GaAs and InGaAs NWFETs respectively. The reduction in the percentage tunnelling with increasing cross-section is because the effective mass decreases with increasing cross-section. A more detailed discussion on the effects of confinement, scattering and percentage tunnelling in GaAs NWFETs can be found in ref. [3].

Figure 3 (a) shows the I_D-V_G characteristics at low drain bias for each valley in the GaAs core 2.2×2.2 nm² cross-section NWFET. Most of the current is in the high mass L and X-valleys, with little current in the low mass Γ-valley. For the 4.2×4.2 nm² cross-section NWFET more of the current is in the Γ-valley [3]. This behaviour is also seen in the InGaAs NWFETs. Figure 3 (b) shows the energy-resolved current spectra with the first subband of each valley superimposed, showing the elevation of the Γ-valley. In comparison to the 4.2×4.2 nm² cross-section NWFET, the Γ-valley has been shifted a further 0.7 eV from the potential. By increasing the thickness of the oxide the Γ-valley will lower; resulting in much higher current [4].

Figure 4 shows the I_D-V_G characteristics at high drain bias for all the simulated NWFETs. For the 2.2×2.2 nm² cross-section devices, the scattering sub-threshold slope is 71, 66 and 63
Figure 4. $I_D$-$V_G$ characteristics at high drain bias, $V_D = 0.6$ V, for Si, GaAs and InGaAs for the (a) $2.2 \times 2.2$ nm$^2$ (b) $4.2 \times 4.2$ nm$^2$ cross-section NWFETs. The ballistic simulations are denoted by the solid lines and the scattering simulations by the dotted lines.

mV/dec for the Si, GaAs and InGaAs cores respectively. For the $4.2 \times 4.2$ nm$^2$ cross-section devices, the scattering sub-threshold slope is 97, 116 and 121 mV/dec for the Si, GaAs and InGaAs cores respectively.

In the $2.2 \times 2.2$ nm$^2$ cross-section devices, there is a 67%, 57% and 43% percentage reduction in the current due to scattering at high $V_G$ for the Si, GaAs and InGaAs cores respectively. For the $4.2 \times 4.2$ nm$^2$ cross-section devices, there is 61%, 20% and 15% percentage reduction in the current due to scattering at high $V_G$ for the Si, GaAs and InGaAs cores respectively. In comparison to low drain, the high drain characteristics generally show a decrease in the percentage reduction of the current due to scattering. This is because the percentage tunnelling is greater at high drain bias than low drain [3].

The phonon-limited mobility has been calculated at low drain bias for low channel charge. For the $2.2 \times 2.2$ nm$^2$ cross-section NWFETs the highest mobility is in the Si core device. At low channel charge the phonon-limited mobility is 229, 62 and 139 cm$^2$/Vs for the Si, GaAs and InGaAs NWFETs respectively. However, for the $4.2 \times 4.2$ nm$^2$ NWFETs the InGaAs device has the highest mobility. For the Si, GaAs and InGaAs core devices at low channel charge, the phonon-limited mobility is 546, 1290 and 1887 cm$^2$/Vs respectively. The low mobility for the III-V $2.2 \times 2.2$ nm$^2$ cross-section devices is due to the elevation of the $\Gamma$-valley.

4. Conclusion
Different dimension NWFETs with Si, GaAs and InGaAs cores have been investigated using the NEGF formalism. For both the $2.2 \times 2.2$ nm$^2$ and $4.2 \times 4.2$ nm$^2$ cross-section, the Si core device has the highest current. This is because there is higher percentage tunnelling in the III-V devices. For the III-V $2.2 \times 2.2$ nm$^2$ cross-section devices, the low mass $\Gamma$-valley becomes elevated in energy above the heavier L and X-valleys. This results in very low current and mobility in those NWFETs. Scattering was found to cause a large reduction in the current for all the simulated devices.

References
[1] M. Lundstrom, “Fundamentals of carrier transport,” Cambridge University Press (2000).
[2] Y. M. Niquet, A. Lherbier, N. H. Quang, M. V. Fernandez-Serra, X. Blase and C. Delerue, Phys. Rev. B 73, 165319 (2006).
[3] A. Price and A. Martinez, J. Appl. Phys. 117, 164501 (2015).
[4] A. Price and A. Martinez, J. Phys. Conf. Ser. 609, 012004 (2015).