Tradeoffs between Settling Time and Jitter in Phase Locked Loops

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Abstract—In most PLL architectures, trade-off exists between settling time and jitter performance, which is ignored during Figure of Merit calculation. This work derives a new Figure of Merit for PLL, which has settling time as added performance parameter, along with jitter and power. Here, the trade-off between settling time and jitter is analyzed theoretically, and with behavioral simulations for (i) linear Time-to-Digital based PLL (ii) non-linear Bang-Bang Phase Detector based PLL (iii) Hybrid PLL with adaptive gain, to obtain settling time vs. jitter relation, based on which commonly used Figure of Merit is modified. To understand trade-off relation between settling time and jitter for Bang-Bang Phase Detector based PLL, this work also derives settling time equation for non-linear PLL, by using recursive time-domain equations.

I. INTRODUCTION

Phase Locked Loops, used in various applications, are required to generate frequency with low power consumption, within low settling time and reduced spurious tones. But, in most PLL architectures, the trade-off existing between jitter, lock time and power does not allow all PLL performance parameters to be optimized simultaneously.

Figure of Merit (FoM) defined in [1], which is commonly used to benchmark PLL performance, does not include effect of increase in settling time, while reducing loop gain to reduce jitter, as shown in Eqn. (1).

\[
FoM = 10 \log \left[ \left( \frac{\sigma_t}{1s} \right)^2 \left( \frac{P}{1mW} \right) \right]
\] (1)

For example, PLL design in [3], having low jitter and power values, has good Figure of Merit as per Eqn. (1). But, this architecture achieves low jitter (0.4ps) and low power (2.8mW), at the cost of very high settling time (300µs). This instance signifies that without considering settling time as a performance parameter, the Figure of Merit in Eqn. (1) is inadequate for benchmarking PLL performance.

In this regard, the trade-off between lock time and jitter is analyzed in this work, for different PLL architectures. Accordingly, commonly used Figure of Merit for PLL is modified, to benchmark PLL performance with consideration to all important specifications i.e. lock time, power and jitter.

This work is organized as follows. Section II analyzes trade-off between settling time and jitter for non-linear Bang-Bang Phase Detector based PLL (BBPLL), Time-to-Digital Converter (TDC) based linear PLL, and Hybrid PLL with adaptive gain. Theroretical analysis for trade-off inherent in these PLL systems, is backed up by results from behavioral simulation of Verilog-A model of PLL architectures, with varied loop gain. Based on settling time vs. jitter curve fitting equation, obtained from PLL behavioral simulations, Section VII proposes a new Figure of Merit, modified to consider lock time also as PLL performance parameter. Section VII uses results from existing PLL designs [3]-[10], to show that proposed Figure of Merit correctly rates PLL performance, based on overall improvement in specifications of lock time, jitter and power.

II. TRADE-OFF ANALYSIS FOR BANG-BANG PHASE DETECTOR BASED PLL

Bang-bang phase detector quantizes phase error between reference clock and feedback clock to only two levels, similar to signum function. Being a non-linear system, Bang-Bang Phase Detector based PLL has its response characteristics dependent on input phase/frequency error magnitude. Unlike PFD or TDC based architectures, wherein output response could be characterized with linear system transfer function in frequency domain; analysis for BBPLL has to be done in time domain. So, for analyzing trade-off between lock time and jitter in this system, settling time is derived using time-domain equations, by tracing trajectory of phase-detector output.

A. Settling Time derivation

Considering a case, wherein, at initial time-step (t = 0), phase error input is \( \phi_o \) and frequency error input is 0; method explained below illustrates derivation of settling time for BBPLL, by tracing number of UP/DOWN pulses in loop’s transient state.

Step 1: Calculate number of UP pulses

(i) At \( t = T_{ref} \) : Initial phase error = \( \phi_o \)
Solving above quadratic equation gives to initial phase error:-

$$\Delta f = (K_P + K_I)K_{VCO}$$

Phase correction, due to incremental frequency correction:

$$\Delta \phi_{cor,1} = \frac{2\pi (K_P + K_I)K_{VCO}}{f_0^2 T_{ref}} N_{div}$$

(iii) At $t = 3T_{ref}$ : Phase correction, due to added frequency ($\Delta f = K_I K_{VCO}$), is :-

$$\Delta \phi_{cor,2} = 2\pi K_I K_{VCO} T_{ref}$$

(iv) At $t = N_{up}T$ : Reference clock and feedback clock align in phase, if accumulated phase correction due to frequency correction done by loop in each reference cycle, becomes equal to initial phase error :-

$$\phi_o = 2\pi T_{ref} \left( \frac{K_{VCO}}{N_{div}} \right) \left[ (K_P + K_I)N_{up} + K_I(N_{up} - 1) + K_I(N_{up} - 2) + \ldots + K_I \right]$$

$$\Rightarrow \phi_o = 2\pi T_{ref} \left( \frac{K_{VCO}}{N_{div}} \right) \left( N_{up}K_P + \frac{N_{up}(N_{up} + 1)K_I}{2} \right)$$

Solving above quadratic equation gives $N_{up}$ value as,

$$\Rightarrow N_{up} = \frac{1}{2} \left[ - \left( 1 + \frac{2K_P}{K_I} \right) \right]$$

$$\pm \sqrt{ \left( 1 + \frac{2K_P}{K_I} \right)^2 - \frac{4\phi_o N_{div}}{\pi T_{ref} K_P K_{VCO}}}$$

$$(2)$$

Though, after $N_{up}$ cycles, phase of reference clock and feedback clock is aligned, but, resultant frequency error (normalized w.r.t $K_{VCO}$) accumulates to:-

$$\Delta f' = \left[ \left( K_P + \frac{N_{up}(N_{up} + 1)}{2} K_I \right) - 2K_P \right]$$

$$= \frac{N_{up}(N_{up} + 1)}{2} K_I - K_P$$

Step 2: Calculate number of DOWN pulses

Due to resultant frequency error ($\Delta f = f_{ref} - N_{div} f_{VCO}$) after $N_{up}$ cycles, phase error starts accumulating with time; which results in sequence of asserted DOWN cycles.

If phase error ($\phi_{err}$) becomes 0 after $N_{down}$ cycles, then, number of down pulses are calculated as :-

$$0 = 2\pi \frac{K_{VCO}}{N_{div}} T_{ref} \left[ \Delta f' N_{down} - \frac{N_{down}(N_{down} + 1)}{2} K_I \right]$$

$$\Rightarrow N_{down} = \frac{2\Delta f'}{K_P} - 1 = N_{up}(N_{up} + 1) - 2K_P K_I - 1$$

$$(3)$$

Therefore, to derive settling time, equation for $N_{up}$ and $N_{down}$ cycles has to be recursively calculated until frequency error becomes 0, at phase error alignment :-

$$t_{settling} = (N_{up1} + N_{down1} + N_{up2} + \ldots.)T_{ref}$$

According to Eqn. $2$-$3$, settling time decreases non-linearly with increase in filter proportional gain($K_P$), Digitally Controlled Oscillator gain ($K_{DCO}$), and ratio of filter’s integral gain to proportional gain ($K_I/K_P$).

B. Jitter Equation

Peak to Peak Jitter for BBPLL, derived in $2$ as Eqn. $5$, indicates that jitter reduces with decrease in loop gain parameters, which are (i) $K_P$ (ii) $K_{DCO}$ (iii) $\frac{K_I}{K_P}$ ratio.

$$\Delta t_{pp} = N K_P K_{TDC} \left[ 2(1 + D) + (1 + D) \frac{K_I}{K_P} \right]$$

$$+ (1 + D)^2 \left( \frac{K_I}{K_P} \right)^2 + O\left( \frac{K_I^3}{K_P^3} \right)$$

$$(5)$$

C. Settling Time vs Jitter Trade-Off

Eqn. $2$-$5$ indicates that settling time and jitter holds inverse non-linear relation to filter parameters and Digitally Controlled Oscillator (DCO) sensitivity gain. For verifying this trade-off relation between settling time and jitter, Verilog-A model of BBPLL is simulated with different values of filter co-efficients. As shown in Fig. $3$ settling time vs. jitter curve follows non-linear relationship, and that, jitter is reduced at the cost of increased settling time. This illustrates the need of adding lock time as a parameter to the commonly used FoM.
A. Settling Time

Considering decay constant from system transfer function, settling time for Type-2 PLL is approximately given as:

\[ t_s = \frac{5}{\xi \omega_n} \propto \frac{10}{K_{TDC} K_P K_{DCO}} \]  \hspace{1cm} (6)

Eqn. (6) indicates that with decreasing DCO gain and filter proportional gain, settling time increases linearly.

B. Jitter Equation

When TDC-based PLL locks to frequency corresponding to fractional value input to DCO, control word oscillates between \( \pm K_P K_{DCO} \). So, with lower DCO gain \( K_{DCO} \) and filter proportional gain \( K_P \), jitter reduces linearly for output frequencies corresponding to fractional control word:

\[ \Delta t = \Delta f \propto \frac{K_P K_{DCO}}{f_o^2} \]  \hspace{1cm} (7)

C. Settling Time vs Jitter Trade-Off

Behavioral simulation of TDC based PLL model with varying DCO gain, indicates linear trade-off between settling-time and jitter (i.e. jitter increases and lock time decreases by same percentage with varied \( K_{DCO} \)) following linear curve fitting equation \( \sigma t_s \), as shown in Fig. 5.

IV. TRADE-OFF ANALYSIS FOR HYBRID PLL WITH ADAPTIVE LOOP GAIN

Hybrid PLL, in Fig. 6 employs two different phase detector blocks for fast linear system response in transient state, and low jitter in settled state. Here, linear Phase-Frequency Detector (PFD) is activated in case of large input phase error, for fast coarse settling; and binary phase detector is activated for small phase error, to avoid the dead zone issue. Adaptive gain feature allows filter gain to be changed, according to input phase error magnitude.

A. Effect of varying DCO Gain

During loop transient in Hybrid PLL, linear PFD is active as error-detection block for major portion of settling time. This results in loop settling curve to follow linear response, as per Eqn. (6) (which represents system response for linear PLL system). So, in case of Hybrid PLL also, linear trade-off between settling time and jitter is observed in behavioral simulation with varied \( K_{DCO} \), as shown in Fig. 7(a).

B. Effect of varying filter constants, in binary phase detection mode

In Hybrid PLL, non-linear bang-bang phase detector is activated only when loop reaches near to locked state. Therefore, reducing loop filter gain in bang-bang phase detection mode, can reduce jitter without significant linear increase in settling time. This overall performance improvement is verified by simulating Hybrid PLL Verilog-A model, with varied filter coefficients in binary phase detection mode. Simulation results in Fig. 7(b) shows that jitter reduces with reduced filter gain (while binary phase detector is active in settled state), without significantly increasing settling time (since, lock time is mainly governed by loop parameters while PFD is active). So, this kind of PLL design, wherein all the specifications (Lock Time/Jitter/Power) could be simultaneously improved, can be benchmarked as having higher Figure of Merit.
V. PROPOSED FIGURE OF MERIT

PLL performance analysis for different PLL architectures, in Sec. IV shows inverse relation that settling time and jitter holds with loop gain. Considering lock time vs. jitter performance observed in linear PLL system, it is proposed to include settling time in Figure of Merit equation, in same ratio as jitter, as shown in Eqn. (8).

\[
FOM = 10\log \left( \frac{\sigma_t}{1s} \right)^2 \left( \frac{t_s}{1s} \right)^2 \left( \frac{P}{1mW} \right)
\]

(8)

VI. PLL PERFORMANCE COMPARISON

Table I uses results of existing PLL architectures (designed in 180nm-90nm technology, with output frequency in 0.5GHz-1.8GHz range), to compare performance benchmarking done with commonly used Figure of Merit versus proposed Figure of Merit in this work.

In Table I, performance comparison for 130nm/90nm designs, indicates that for PLL [3] [5] achieving lowest jitter at the cost of large settling time, existing FoM [1] proves as an inadequate benchmark by ignoring lock time performance degradation. Similarly, performance comparison for 180nm designs, indicates that PLL [10] having lowest settling time at the cost of increased jitter is benchmarked for having lowest performance with FoM defined in [1] (which does not considers reduced lock time as improved PLL performance parameter).

Proposed Figure of Merit, on the other hand, correctly marks PLL designs for their overall performance, by considering inverse relation existing between settling time and jitter (as indicated in Table I).

**TABLE I**

PERFORMANCE BENCHMARKING FOR PLL ARCHITECTURES

| Ref. | Tech. | Freq. (GHz) | Jitter (ps) | Power (mW) | FOM of PLL (Eqn. 1) | Lock Time (µs) | Proposed FOM |
|------|-------|-------------|------------|------------|---------------------|----------------|---------------|
| [3]  | 130   | 1.56        | 0.38       | 2.8        | -243.9              | 300            | -314.4        |
| [4]  | 130   | 1.35        | 3.7        | 16.5       | -216.5              | 3.84           | -324.4        |
| [5]  | 90    | 1.73        | 4.15       | 11.3       | -227.1              | 40             | -315          |
| [6]  | 90    | 0.64        | 4.9        | 3.8        | -220.4              | 4.67           | -327          |
| [7]  | 90    | 0.48        | 5.8        | 3          | -219.9              | 2              | -333          |
| [8]  | 180   | 1.2         | 3.5        | 18         | -216.6              | 5              | -322          |
| [9]  | 180   | 1.56        | 9.7        | 16.2       | -208.2              | 26             | -299          |
| [10] | 180   | 0.446       | 7.0        | 14.5       | -191.5              | 0.5            | -317.5        |

Fig. 8 shows performance of existing PLL designs, with consideration to lock time, along with output jitter and power dissipated by PLL system.

VII. CONCLUSION

In this work, with analysis and behavioral simulation of different PLL architectures, trade-off between settling time and jitter is shown. Since, most PLL designs are able to achieve low jitter only at the cost of increased settling time, therefore, it is proposed to include lock time also as performance parameter in Figure of Merit for PLL.

Based on analysis of linear PLL system, we have proposed a Figure of Merit for PLL, wherein settling time is considered in equal proportion as jitter, for deciding overall PLL performance.

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