Experimental Body-input Three-stage DC offset Calibration Scheme for Memristive Crossbar

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Abstract—Reading several ReRAMs simultaneously in a neuromorphic circuit increases power consumption and limits scalability. Applying small inference read pulses is a vain attempt when offset voltages of the read-out circuit are decisively more. This paper presents an experimental validation of a three-stage calibration scheme to calibrate the DC offset voltage across the rows of the memristive crossbar. The proposed method is based on biasing the body terminal of one of the differential pair MOSFETs of the buffer through a series of cascaded resistor banks arranged in three stages—coarse, fine and finer stages. The circuit is designed in a 130 nm CMOS technology, where the OxRAM-based binary memristors are built on top of it. A dedicated PCB and other auxiliary boards have been designed for testing the chip. Experimental results validate the presented approach, which is only limited by mismatch and electrical noise.

I. INTRODUCTION

Memristors evolved as a good choice of candidature for artificial synapses in neuromorphic circuits after HP labs proved the physical existence of Chua’s finding [1]–[4]. Oxide-based Random-Access Memory (OxRAM) slowly rose to one of the promising synapses in neuromorphic computing systems due to their low-switching energy and high endurance [5]–[8]. The binary OxRAM synapses in a crossbar architecture used in this work are first formed and then switched between Low Resistance State (LRS) and High Resistance State (HRS) by applying a controlled voltage via a series connected MOSFET [9]. To prevent sneak-path currents, a selector MOSFET is connected in series to the OxRAM, leading to the so-called—‘1T1R’ structure as shown in Fig. 1(a) [10].

The filament of the OxRAM is formed by applying a bias $V_{TS} = 4$ V, 10 μs pulse and gate bias $V_{GS} = 1$ V, with a recommended compliance forming current of about 1 μA. For a RESET operation, a bias of $V_{ST} = 3$ V, 100 ns pulse is applied by keeping the gate fully ON ($V_{GT} = VDD$). For a SET operation, a bias $V_{TS} = 2.4$ V, 100 ns pulse is applied along with the gate bias, $V_{GS} = 1.5$ V. For a read operation, a read voltage of $V_{TS}$ or $V_{Read} = 0.3$ V is applied with a gate bias, $V_{GS} = 3.8$ V. During inference operation, when read pulses are applied across several memristors, power dissipation becomes critical, which limits the scalability of the crossbar [11]. To overcome this, we need to apply small inference read pulses. Fig. 1(b) shows OxRAM currents for read voltage pulses less than 1 V when LRS$ = 13.7$ kΩ and HRS$ = 845.9$ kΩ. However, applying such small read pulses becomes non-trivial, when the offset voltage of the system ruins the measurement.

The rest of the paper is organized as follows: In Section II, the $N 	imes n$ 1T1R crossbar with calibration of DC offset voltage in each row is described. The three-stage substrate-based calibration scheme is also explained in this section. Section III presents the experimental setup of DC offset calibration scheme. Section IV depicts the experimental results of calibration scheme. Finally, conclusions are drawn in Section V.
II. N × n 1T1R CROSSBAR WITH CALIBRATION OF DC OFFSET VOLTAGE IN EACH ROW

Fig. 2 shows an N × n 1T1R memristive crossbar architecture with calibration of DC offset voltage in each row. Each row has its own pre-synaptic driver. Each pre-synaptic driver comprises an opamp, calibration circuit, pulse-shaping digital block and an I-pot. I-pots are digitally programmable current sources which, from a reference current can provide desired current with high precision, down to pA [16]. I-pots serve as current source biases for the opamps and are controlled by 14-bit control word. Opamps are P-MOSFET based differential two-stage opamps. Each column has its own post-synaptic driver. Each post-synaptic driver comprises an integrator and a comparator.

Fig. 3 shows the three-stage calibration scheme, pulse-shaping digital block and opamp across row1. A similar schematic exists in each row. The pulse-shaping digital block is used to set three possible biases through digital control. The three-stage (coarse, fine and finer) calibration scheme is a cascade of resistor ladders whose resistor combinations are chosen by selectively turning ON the P-MOSFET switches via decoders. One of the differential pair MOSFET’s body-voltage of the opamp is biased with the calibration range between \( V_{ref} - V_d \) and \( V_{ref} + V_d \) in order to compensate the offset across the rows, while the other MOSFET’s body-voltage is biased with \( Calibref_{1,2,...,N} \). \( V_{ref} \) is the calibration reference voltage and \( V_d \) is the calibration differential voltage. The calibration scheme is digitally controlled by a 12-bit control word. To serve this purpose, a 26×N-bit edge-triggered D-flip flop based shift register is designed for having full-digital control of the I-pots and calibration schemes of the N × n crossbar.

III. EXPERIMENTAL SETUP OF DC OFFSET CALIBRATION SCHEME

Fig. 4 shows the experimental setup of the DC offset calibration scheme. It mainly comprises the test PCB which includes the chip under test, a SPARTAN 6 driver board, a button board, a resistor plug-and-play board, a logic analyser and its digital pod. Calibration circuit or scheme is part of the circuits in ‘outer-ring’ of the chip designed using 130
nm CMOS technology, which has the OxRAMs integrated above it. The ‘outer-ring’ of the chip is packed in a 100-pin PGA package, which is connected through a PGA 196-ZIF socket mounted on the test PCB. Fig. 5 shows different previews of the chip packed in PGA100 package with its labelled layout. For testing calibration scheme, a dedicated PCB is made, which mainly comprises components like opamps, level-shifters (3.3 V to 4.8 V), ADC, linear voltage regulator, switches and digital components like decoders, inverters, etc. Opamps on PCB are either used as power supplies opamps or integrating opamps or as comparators. The main purpose of the PCB is to assure desired analog biases at specific terminals of the chip, which are controlled by switches and digital circuits. These switches and digital circuits are further controlled by the SPARTAN 6 driver board. The button board has dedicated buttons to perform OxRAM operations like FORM, SET, RESET, READ and to calibrate DC offset during READ. It also has jumper arrangements where one can choose the target synapse in a crossbar and also pick the input bit sequence for the calibration scheme. The button board and the SPARTAN 6 driver board are used together for two main purposes: (i) Target a synaptic 1T1R device in the crossbar and perform operations like FORM, SET, RESET and READ through a 3-bit control signal, \((A, B, C)\) and (ii) Set the 12-bit control word for calibration scheme and perform calibration of DC offset during a READ operation.

**IV. EXPERIMENTAL RESULTS OF CALIBRATION SCHEME**

This section shows various results of the three-stage calibration scheme implemented in a \(4 \times 4\) memristive crossbar. Fig. 6 shows a preview of the output screen when \(V_{\text{read}} = 0.33\) V. After forming the targeted OxRAM, a READ operation is performed when \(A=\text{OFF}\), \(B=\text{OFF}\) and \(C=\text{OFF}\). Here \((A, B, C)\) is the control signal that is
used to set specific OxRAM operation. \( \text{data}_{in} \) is the \( 26 \times 4 = 104 \)-bit control word, which are the control-bits for I-pots and calibration circuits of the opamps in the experimented \( 4 \times 4 \) crossbar. Frequency of \( \text{clock} \) input to shift-register is kept at 2 kHz. Once, the calibration scheme is biased with \( V_{\text{ref}} = 4.5 \) V, \( V_d = 15 \) mV and \( \text{Calibref}_{1,2,3,4} = 4.5 \) V, \( \text{data}_{in} \) is loaded into the shift-register. Following this, \( \text{Latch} \) is turned ON and the targeted row is calibrated by varying the 12-bit input calibration sequence using button-board.

Fig. 7 shows the comparison of experimental and simulation results when \( \text{row}_1 \) of the crossbar is calibrated for DC offset voltage during stage 1 calibration for \( V_{\text{Read}} = 0.33 \) V. These results are taken by averaging 100 million samples in order to filter out noise, whose standard-deviation is about 200 \( \mu \)V. The power dissipation during inference READ operation is about 0.8 \( \mu \)W for a \( 4 \times 4 \) crossbar when using a 50 mV read pulse whose DC offset voltage is finely calibrated. The zero-crossing region in Fig. 7 is targeted and DC offset voltages are calibrated during stage 2 and stage 3 calibration, whose results are shown in Fig. 8 and Fig. 9. Experimental results of the three-stage calibration scheme match simulation results.

V. CONCLUSIONS

The experimental results presented in this paper show that it is possible to reduce the DC offset of memristive-array read-out systems below 0.1mV. The proposed approach – based on the use of a bulk-input differential pair – is demonstrated by presented measurements, thus opening doors to increasing the scalability of memristive-based neuromorphic systems thanks to the use of lower pulse amplitudes with the subsequent benefits in terms of power dissipation.

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