Photonic circuits in which stateful components are coupled via guided electromagnetic fields are natural candidates for resource-efficient implementation of iterative stochastic algorithms based on propagation of information around a graph. Conversely, such message-passing algorithms suggest novel circuit architectures for signal processing and computation that are well matched to nanophotonic device physics. Here, we construct and analyze a quantum optical model of a photonic circuit for iterative decoding of a class of low-density parity-check (LDPC) codes called expander codes. Our circuit can be understood as an open quantum system whose autonomous dynamics map straightforwardly onto the subroutines of an LDPC decoding scheme, with several attractive features: it can operate in the ultra-low power regime of photonics in which quantum fluctuations become significant, it is robust to noise and component imperfections, it achieves comparable performance to known iterative algorithms for this class of codes, and it provides an instructive example of how nanophotonic cavity quantum electrodynamic components can enable useful new information technology even if the solid-state qubits on which they are based are heavily dephased and cannot support large-scale entanglement.

Keywords: coherent quantum control, photonic circuits, low density parity-check codes
1. Introduction

Recent advances in the realization of nanoscale optical devices have shown the potential for ultra-low-power integrated photonic circuits for classical information processing that would have significant advantages over electronic circuits in terms of heat generation and interconnect density [1, 2]. In parallel, theoretical and computational tools have been developed for modeling the dynamics of photonic devices that have switching energies in the deeply sub-femtojoule, few-photon regime and are thus subject to quantum fluctuations [3]. These developments present an opportunity to consider the conventional (as opposed to quantum entanglement-enhanced) computational potential of such quantum noise-limited systems and to begin to consider architectural approaches that naturally accommodate noisy, low-power components interacting via coherent signal fields.

An intriguing source of architectural guidance is the broad and growing field of iterative, graph-based algorithms used today for computational tasks such as error-correction, probabilistic inference, optimization, and signal processing [4]. Such algorithms, including variants of message-passing schemes such as belief propagation, have the flavor of nodes repeatedly exchanging information locally with their neighbors until global convergence. This picture invites an analogy to the dynamics of a network of photonic components, each of which has some internal degree of freedom (e.g., an ‘atomic’ state), coupled via continuous interaction with propagating coherent fields. Thus, photonic information processing systems could provide a native hardware platform for the implementation of iterative graph-based algorithms that are currently executed using electronic computers with incommensurate (though universal) circuit architectures that simulate message passing inefficiently.

Here, we develop an instance of this direct mapping of a graph-based algorithm to a photonic circuit design for a simple and practically useful task: iterative decoding of expander codes, a class of low-density parity-check (LDPC) error-correcting codes for communication over a noisy channel. We work in the setting of linear coding theory in which every codeword is required to satisfy a set of parity-check constraints, i.e., sums modulo 2 of subsets of its bits. The assignments (0 or 1) of the codeword bits and the values of their parity-check sums correspond to the states (|0⟩ or |1⟩) of a collection of two-state systems. Here, we have in mind that |0⟩ and |1⟩ ideally should correspond to orthogonal quantum states of an atom-like elementary physical degree of freedom, to facilitate ultra-low energy scales for switching, but our circuit does not require coherent superpositions or entanglement. For decoding a possibly corrupted channel output, we consider a simple iterative decoding procedure for the expander LDPC codes [5, 6]: flip any bit (i.e., 0 ↔ 1) that appears in more unsatisfied than satisfied parity-check constraints; repeat until no more flips occur. We map this decoding procedure onto a closed-loop feedback circuit: a simple sub-circuit is engineered to encode parity-check sum values in the state of an optical field, and another sub-circuit is designed to route feedback optical fields such that the states of certain components are flipped (i.e., |0⟩ ↔ |1⟩) at a rate that grows with the number of unsatisfied parity-check constraints.

The proposed circuit is autonomous, continuous-time and asynchronous. No external controller, measurement system or clock signal is required, so the circuit can be realized as a single photonic device whose only required inputs are stationary coherent optical fields that
drive the computational dynamics (i.e., supply power)\(^1\). This follows the spirit of the systems we have designed in previous work on autonomous quantum memories \([7, 8]\). In contrast to our earlier work, the decoding circuit in the present proposal is straightforwardly extensible to the long block lengths (thousands of bits) used in practical LDPC implementations, as it involves a simpler feedback circuit architecture\(^2\).

Our circuit requires a collection of two-state latch systems coupled to input and output field modes. Here we consider designs based on the attojoule nanophotonic relay proposed in \([9]\), which is based on ideas of cavity quantum electrodynamics (cavity QED), but any photonic system that functions as a latch potentially could be used in our circuit, e.g., \([10]\). Moreover, our scheme tolerates noisy components (e.g., spontaneous switching of a latch between the 0 and 1 states), can compensate for this noise with increased input optical power, and actually performs optimally (in terms of bits decoded per second) when the components ‘misbehave’ at some nonzero rate. The graceful change in performance with increasing component imperfection and with varying optical input power is important for the practical usefulness of such a circuit. In our circuit design there is no real distinction between power and signal, as the power carried by the optical signal fields drives all the computational dynamics of the components, and it will be shown in figure 9 that simply increasing the optical input power reduces the error correction latency with fixed hardware. Our circuit tolerates a wide range of input powers with a constant performance as measured by bits corrected per joule.

This paper is organized as follows: We first briefly review linear error-correcting codes and an iterative decoding scheme for expander LDPC codes. We then describe in an intuitive way the operating principles of our photonic circuit implementation of an iterative LDPC decoder. The subsequent section gives a more detailed picture of our circuit in terms of open quantum systems theory. We then present some numerical tests of our system and conclude with a discussion. The appendices describe circuit composition rules for open quantum systems, discuss the details of our numerical simulations, and derive some bounds for a parameter regime in which we expect our scheme to work.

2. Linear codes and iterative decoding

We briefly review and set up notation for block binary linear error-correcting codes and an iterative decoding procedure for expander LDPC codes.

2.1. Linear codes

We work with binary bits transmitted in blocks of length \(n\) through the binary symmetric channel (BSC) that with some fixed probability independently flips (i.e. \(0 \rightarrow 1, 1 \rightarrow 0\)) the transmitted bits. To protect from errors, the sender restricts the possible channel inputs to the set

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\(^1\) Note that signal processing devices that require only optical forms of power may be of practical interest for large-area fiber optic networks.

\(^2\) The circuits in our earlier work implement maximum likelihood (ML) decoders for small codes like the three-bit bit-flip code. ML decoding is, however, impractical for larger block lengths, as it requires either a circuit size or decoding time exponentially large in the block length. Iterative decoding algorithms such as the one discussed in this work have a larger error rate than ML decoders, but require only polynomial or even linear resources in the block length.
of codewords—a subset of all $2^n$ possible inputs. The decoder attempts to find the nearest codeword to the possibly corrupted output of the channel. Equivalently, the bits are stored in memory that accumulates errors with time; the sender/decoder attempt to minimize losses through redundancy in the encoded memory bits.

Linear codes require each codeword $x^n = (x_1, \ldots, x_n)$ to satisfy $m$ parity-check constraints. A parity-check constraint $c$ is a subset of the $n$ message bits whose sum is constrained to equal 0 modulo 2:

$$\sum_{j \in c} x_j = 0 \pmod{2}$$

A vector $x^n$ is a codeword if and only if it satisfies every constraint. The rate $R$ of the code is the ratio of the number of non-redundant bits to the total number of bits per transmission, $R = (n - m)/n$.

It is useful to think of a code as an undirected bipartite graph, the Tanner graph [11], whose $n$ ‘variable’ nodes correspond to the message bits and whose $m$ ‘check’ nodes correspond to the constraints. Edges connect variable nodes and the constraints that include them.

2.2. Linear $\supset$ LDPC $\supset$ expander codes

Low-density parity-check (LDPC) codes are linear codes introduced by Gallager in 1962 [12, 13] and are among the first-known, near-capacity achieving efficiently decodable codes. The parity-checks of a $(n, l, k)$ LDPC code all include $k$ bits, and each bit is included in $l$ parity checks (in the Tanner graph, each variable node has degree $l$ and each check node has degree $k$). The codes are ‘low-density’ because the total number of variable-check pairs is $ln$, linear in the block length $n$ (rather than quadratic in $n$ for a dense graph); the Tanner graph is sparse. The rate of the code is $R = (n - m)/n = (k - l)/k$.

Figure 1 shows the Tanner graph for a particular $(n = 8, l = 3, k = 4)$ LDPC code, where variable (check) nodes are drawn as circles (squares), and we have highlighted a particular parity-check constraint. This graph would look sparse for larger $n$.

LDPC codes shine because they can be decoded efficiently by iterative algorithms that have good performance in practice and in theory. These schemes include those in Gallager’s original work [13], as well as message-passing algorithms and belief propagation; for a theoretical analysis of their performance, see [14–17]. These schemes all have the flavor of variable and check nodes repeatedly exchanging information about the most likely codeword given the observed channel output and differ from each other in how that information is represented (e.g. binary or real-valued messages) and how new messages are computed from old.
Expander codes are a class of LDPC codes, introduced by Sipser and Spielman [5, 6], for which a particularly simple iterative decoding procedure exists and that are easy to make by using a random construction. Expander codes require the Tanner graph to be a good expander graph, meaning that the number of check nodes neighboring any small enough subset $V$ of the variable nodes grows fast enough linearly with $|V|$. For our purposes, it suffices to note that a randomly sampled bipartite graph with fixed variable and check node degree (a regular LDPC code) probably makes a good expander code [6].

2.3. Iterative decoding of expander codes

The iterative decoding procedure that is our focus in this work is the sequential decoder of Sipser and Spielman [6]. The variable bits are initially assigned to 0 or 1, equal to the observed output of the channel (we work with a binary symmetric channel that flips incoming bits with a probability of less than $1/2$). The initial assignment of the variables may fail to satisfy all parity-check constraints due to errors. The decoding procedure is as follows:

- Flip (i.e. $0 \leftrightarrow 1$) any variable that is included in more unsatisfied than satisfied constraints.
- Repeat until no more variables are flipped.

Each iteration reduces the total number of unsatisfied constraints, so the procedure terminates when either there are 0 unsatisfied constraints (successfully outputting a codeword) or it gets stuck and declares failure to decode. While this procedure could be applied to any binary linear code, [6] proves that for expander codes this procedure removes a constant fraction of errors and, if the initial fraction of errors is low enough, is guaranteed to succeed. For the expander LDPC codes, each variable participates in $k$ constraints, so we flip the variable’s assignment if the number of unsatisfied constraints is greater than $k/2$.

Importantly for our work, in [6]’s numerical experiments, it was found that permitting the algorithm to make some amount of backwards progress (sometimes increasing the total number of unsatisfied constraints) increased the probability of success. This suggests the procedure is robust to noise affecting the computation. In our approximate implementation of this iterative algorithm, described below, backwards progress is unavoidable and the hardware itself is noisy, so this robustness of the decoding procedure to noise is desirable.

This procedure is not technically a message-passing algorithm in the sense of [18], in that information flow from a check to a variable node (a possible ‘flip’ instruction) does not exclude information received by the check node from that variable node (the bit state). Nonetheless, it is convenient to discuss the error-correcting dynamics, as [6] does, in terms of variable nodes receiving ‘flip messages’ from check nodes.

3. A photonic decoding circuit: Overview

We give an intuitive description of the operation of our expander code decoder circuit before giving a more precise description in terms of open quantum systems in the section that follows.

3.1. The idea

Our circuit consists of a collection of two-state ($|0\rangle$ or $|1\rangle$) systems, one for each of $n$ variable and $m$ check nodes in the Tanner graph for an error-correcting code. Information exchange
between the variable and check systems is mediated by coherent fields interacting with these systems (e.g. a beam scattering from one atom-cavity system into another). There are two crucial interactions:

- Fields outgoing from a system can encode that system’s state (perform a measurement).
- Fields incoming to a system can drive that system into a desired state (apply a control).

These two interactions allow us to construct a closed-loop, autonomous measurement and feedback circuit that achieves:

- Parity-checks/Measurements: A field scattered (e.g. a beam reflected) from the set of all variable bit systems included in some parity-check constraint encodes their sum modulo 2. This field then drives the check system into the |satisfied⟩ or |unsatisfied⟩ states (|0⟩ or |1⟩, respectively).
- Error correction/Feedback: A field scattered from the set of all check systems that include a particular variable has an amplitude that increases with the number of unsatisfied checks involving that variable. This field then drives the variable system to flip between the |0⟩ and |1⟩ state at a rate proportional to the magnitude of the field amplitude. The more unsatisfied parity-checks, the faster the flipping occurs.

The time evolution of this circuit is modeled as a continuous time Markov jump process

\[ R_{\text{flip}} > 0 \text{; otherwise, set } R_{\text{flip}} = 0. \]

In our implementation, the value of \( R_{\text{flip}} \) scales with the number of unsatisfied constraints in a different way (and is never 0; see section 4.3.2), but we attain comparable empirical performance in simulation.

Finally, we note that our circuit is essentially classical in its operation, even though we utilize quantum stochastic differential equations (QSDEs) to describe the dynamics of the components and their interactions in order to obtain a circuit model that is valid in the ultra-low-power regime of significant quantum fluctuations (photon shot noise). Entanglement between different subsystems is insignificant and is not exploited, and thus does not need to be protected from interactions with the outside environment.

4. A photonic decoding circuit—construction

We briefly review open quantum systems connected into circuits, describe the photonic component subsystems that make up our circuit, and specify their interconnection to form our iterative decoder circuit. We give an intuitive description of our circuit’s dynamics and defer a more detailed description to appendices A and B.

3 This description follows from the open quantum systems dynamics treatment of our circuit. See sections 5.1 for details.
4.1. Open quantum systems and circuits

We work in the framework developed by Gough and James [19, 20] for modeling open quantum systems interacting via coherent fields [21–24]. The basic component model (shown in figure 11 of appendix A.1) comprises a system with internal degrees of freedom coupled to incoming and outgoing field modes. The system is parametrized by its Hamiltonian $H$, by the coupling of the external modes to the internal degrees of freedom ($n$ by 1 operator-valued vector $L$), and by the way the incoming external field modes scatter into outgoing external field modes ($n$ by $n$ operator-valued unitary matrix $S$). The density matrix $\rho$ for the system’s internal degrees of freedom evolves in time according to the master equation:

$$\dot{\rho}_t = -i[H, \rho_t] + \sum_{i=1}^{n} \left( L_i \rho_t L_i^\dagger - \frac{1}{2} \left\{ L_i^\dagger L_i, \rho_t \right\} \right).$$

where $L_i$ is the $i$th component of the external field mode coupling vector $L$. See appendix A for a more detailed discussion.

The Gough–James circuit algebra allows us to compute new $(S, L, H)$ triplets in terms of old for two systems connected in series, in parallel, or for one system self-connected through feedback. These composition rules are given in appendix A.2. A systematic, automated approach for specifying and simulating such circuits in software is presented in [25, 26].

4.2. Photonic circuit components

The basic component of our circuit—used to represent both variable and check node assignments ($\langle 0 \rangle$ and $\langle 1 \rangle$)—is a photonic latch, shown in figure 2, that behaves like the set-reset latch in electronics. There are several proposals for implementing latching behavior in nanophotonic circuits [9, 10, 27–29]. One such system, a coupled atom-cavity system [9], is shown in figure 2 [panel (b)]. Our circuit construction is defined without reference to a particular physical system and assumes that the latch system used implements the following protocol.

The latch has a discrete internal degree of freedom (e.g. an atomic state) coupled to two external field modes, labeled ‘set’ and ‘reset’. A signal incoming to the ‘set’ (‘reset’) input drives the latch into the $\langle 1 \rangle$ ($\langle 0 \rangle$) state. When neither the set nor reset input is powered, the latch maintains its current state. Usefully for us, driving both the set and reset inputs simultaneously—an undefined condition for the electronic set-reset latch—results in astable behavior, with the latch state repeatedly jumping between the $\langle 0 \rangle$ and $\langle 1 \rangle$ state with exponentially distributed jump times.

The latch routes two input channels (in$_1$ and in$_2$) into two output channels (out$_1$ and out$_2$). When the latch is in the $\langle 0 \rangle$ state, the outputs match the inputs (out$_{1,2} = \text{in}_{1,2}$); when the latch is in the $\langle 1 \rangle$ state, the outputs are switched (out$_{1,2} = \text{in}_{2,1}$).

In addition to the latch, our circuit uses beamsplitters with some fixed transmission and reflection coefficients. Proposals for integrated nanophotonic beamsplitting devices include [30, 31]. The Gough–James $(S, L, H)$ description of these components connected to each other and driven by coherent fields is provided in appendix B.
4.3. Circuit construction

We describe how the latches, beamsplitters, and coherent inputs are used to form our expander code decoding circuit. There are two kinds of interactions to implement between the variable and check systems: parity-check sums and feedback to ‘flip’ the variable nodes.

4.3.1. Parity checks. Figure 3 shows our parity-check sum construction. For each parity-check \( \mathbf{e} \) corresponding to the \( k \)-variable constraint \( \oplus_{i=1}^k x_{e(i)} = 0 \), there are \( k \) variable latch systems, \( Q_{e(1)}^\text{var}, \ldots, Q_{e(k)}^\text{var} \), and one check latch system \( Q^\text{check} \) (here \( \oplus \) denotes addition modulo 2). The current assignment (0 or 1) of the variables included in \( \mathbf{e} \) is represented by the states \( \left| 0 \right> \) or \( \left| 1 \right> \) of the variable latches; the check latch’s state is meant to represent the sum of these assignments modulo 2. As shown in figure 3(b), the variable latches share two common optical paths for their \( \text{in}_1 \) and \( \text{in}_2 \) inputs and outputs. An input field with amplitude \( \alpha \) is incident to input port \( \text{in}_1 \) of check latch \( Q_{e(1)}^\text{var} \). Subsequently, the two output ports of \( Q_{e(i)}^\text{var} \) connect to the two input ports of \( Q_{e(i+1)}^\text{var} \) for \( i < k \). The outputs of the final variable latch \( Q_{e(k)}^\text{var} \) connect to the set and reset ports of check latch \( Q^\text{check} \).

Each time a \( \left| 1 \right> \) state is encountered at a variable latch along the beam path, the latch switches the beam path between the upper and lower branches. If the output power of the final latch is in the upper (lower) branch, then the parity of the variable assignment is odd (even), and the SET (RESET) port of the check latch receives power, driving the check latch into the
unsatisfied |1
(unsatisfied) = |1) (satisfied) = |0) state. The rate at which the check latch is driven to the appropriate state is proportional to the input field power $\alpha$ in units of photons per second.

The check latch $Q_{\text{check}}^{\text{var}}(1)$ in turn routes fields that participate in the feedback circuit described in the next section.

### 4.3.2. Feedback to variables

Figure 4 shows our feedback to variables construction. For a variable $v$, let $v$ denote the $l$ parity-check constraints that include $v$: $v = \{ e : v \in e \}$. The current value (parity—0 or 1) of the each check in $v$ is represented by the state ($|0\rangle$ or $|1\rangle$) of latches $Q_{v(1)}^{\text{check}}, \ldots, Q_{v(l)}^{\text{check}}$. As shown in figure 4(c), the check latches share a common optical path. An input field with amplitude $\beta$ is incident to input port $in_1$ of latch $Q_{v(1)}^{\text{check}}$. Subsequently, for each check latch $Q_{v(i)}^{\text{check}}, 1 \leq i \leq l$, the second output is fed back into the second input of the same latch after passing through an attenuator (e.g. a beamsplitter) that dumps (e.g. reflects out of the beam path) a fraction $\gamma < 1$ of incident power and transmits a fraction $1 - \gamma$ of the power back into the beam path.

Each time an unsatisfied parity-check constraint state ($|1\rangle$ state) is encountered at a check latch along the beam path, the power reaching the next check latch in the path is attenuated by a factor of $\gamma$. The output of the final check latch in the path $Q_{v(l)}^{\text{check}}$ is routed to drive both the SET and RESET inputs of the variable latch $Q_{v}^{\text{var}}$, causing it to ‘flip’ between the $|0\rangle$ and $|1\rangle$ states.

Once a flip of variable $v$ occurs, the parity-check system discussed in the previous section updates the states of the check systems that include this variable, resulting in an updated value of the flipping rate for variable $v$. If the power in the measurement circuit used to perform the parity-check computation is low enough, the feedback circuit may induce multiple flips of the same variable before the measurement system reacts. We consider this situation in the numerical results in the section below.

The rate at which the variable latch $Q_{v}^{\text{var}}$ flips is proportional to the attenuated power outgoing from the final latch in the beam path:
If all parity constraints that include a variable $v$ are unsatisfied, the state of variable latch $Q_v$ flips with the maximum rate proportional to $|\beta|^2$. If all $l$ constraints are satisfied, the variable is flipped with non-zero rate proportional to $\gamma^l |\beta|^2$. Thus our circuit can induce errors. For $\gamma \ll 1$, a single induced error should be quickly corrected, since the rate for correcting it is a factor of $1/\gamma^l \gg 1$ larger than the rate for inducing it.

Our circuit corrects errors that are involved in $i$ parity-check violations on a timescale proportional to $1/\gamma^i$. The smaller we make the attenuation factor $\gamma$, the fewer induced errors there are, but the longer the decoding takes to complete. We derive some bounds on the maximum value of $\gamma$ in terms of the code parameters such that our procedure is likely to succeed in appendix C. We guess that the attenuation factor $\gamma$ should not be too small, since the decoding probability could increase when some induced errors are permitted, as observed in [6]. This intuition is consistent with our observations in the numerical results section below.

4.4. Complete circuit summary plots

Figure 5 shows both the measurement and feedback subcircuits for a fragment of our decoder circuit corresponding to a fragment of the Tanner graph of an error-correcting code. There is one such fragment for each of $nl$ edges in the Tanner graph of the code.

Figure 6 shows a portion of a simulated trajectory for a fragment of the code. The top panel shows the state (0) or (1)) of a latch corresponding to a variable bit (blue) and the three latches
Figure 5. Measurement and feedback circuit fragment (right) corresponding to fragment of Tanner graph (left).

Figure 6. Part of a trajectory of the decoding circuit for a fragment of an error-correcting code. (top panel, blue line) state of a latch corresponding to a variable bit (top panel, dark red lines) states of latches corresponding to parity-check constraints that include the blue variable bit. (bottom panel) the feedback power applied to the variable bit, inducing it to ‘flip’ state. On a log scale, this feedback power is proportional to the number of satisfied parity-check constraints that include this variable bit. See text for trajectory narration.
corresponding to the three parity-checks that include this bit (dark red). At time 0, an error causes the variable bit latch (blue) to flip state (perhaps the component malfunctioned or the feedback system induced the error). The three check latches corresponding to this bit then turn on (enter the unsatisfied \(|1\rangle\) state) after some exponentially distributed waiting time (the mean of the waiting time is set by the input probe power used to perform the parity-check sum computation). For each check latch that enters the unsatisfied \(|1\rangle\) state, the feedback power reaching of the variable bit grows by a factor of \(1/\gamma\), where \(\gamma\) is the attenuation constant. Around time 1.25, the feedback induces the bit to flip back to the \(|1\rangle\) state. After an additional random waiting time, the three latch systems return to the satisfied \(|0\rangle\) state. Note that the feedback power reaching the bit is never 0, but reaches a minimum when all parity-check constraints are satisfied.

4.5. Fan-out

Our decoder circuit requires each variable latch component to participate in multiple \((l)\) parity-check constraints, and requires each parity constraint latch component to feed back to multiple \((k)\) variables. Since the latch described in section 4.2 (and in greater detail in appendix B.3) can switch only a single pair of signal inputs, it is not on its own sufficient for our needs. We can augment our latch to achieve the desired fan-out (and avoid the difficulty of having multiple beam paths access a single structure in a planar circuit) by breaking up each latch into a set of subsystems, each responsible for routing a single in/out signal pair. The subsystems are yet more latches, but each routes only a single pair of in/out signals, corresponding to the latch description of section 4.2.

Figure 12 (in appendix D) shows the circuit for the augmented latch that routes multiple in/out signal pairs. This augmented latch is used implicitly in our circuit description above and is described in detail in appendix D. The idea is that a single ‘master’ latch receives the two set/reset inputs and then routes power to drive the ‘slave’ latches into a matching state. Distributing the master latch state to the slave latches requires another optical input with amplitude \(a_{\text{f-out}}\) (for fan-out).

The numerical results presented below in section 5 are done at infinite fan-out power (yellow optical line in figure 12) so that the effects of the extra fan-out components on decoding performance can be ignored. We consider the effect of finite fan-out power in section 5.5.

5. Numerical experiments

Table 1 lists the parameters used in our simulations. The spontaneous flip rate \(\eta\) quantifies component noise during the computation—all latches in our circuit independently flip \((|0\rangle \leftrightarrow |1\rangle)\) with rate \(\eta\).

5.1. Simulating quantum trajectories

Our circuit evolves according to the master equation (2). Rather than solve this equation for the density matrix \(\rho\) for our system, we sample multiple trajectories of the system wavefunction \(|\psi\rangle\) and average observed quantities over these trajectories. Simulation of quantum trajectories given a master equation in the form of (2) is computationally easier than integrating the master equation and is discussed in detail in [32]. One way to perform such simulations is to sample
exponentially distributed jump times for each component of the system \( L \) vector (rate for \( i \)th component is \( \psi_i \sim \left\langle L_i | L_j | \psi \right\rangle^2 \)), apply the nearest-in-time jump to the system wavefunction, and resample all of the jump times given the new wavefunction. In general, there is a smooth Hamiltonian evolution occurring between jumps as well, but our decoder circuit’s Hamiltonian is diagonal in the \( \{|0\}, |1\} \) state basis, and this basis is fixed by the components of \( L \) (the jump terms) so we can ignore the smooth evolution and treat the system as a continuous time Markov jump process.

We prefer the trajectory approach in part because we want to average over different random instances of the expander code (with different network connectivities each time) and because it is useful to examine the time evolution of individual trajectories for an intuitive view of the circuit.

### 5.2. Trajectories

We uniformly randomly sample 30 bits to corrupt from the initial all-0 codeword of length \( n = 1000 \) for a randomly sampled LDPC code with \( l = 5 \), \( k = 10 \), and track the remaining number of errors in time. The code is generated by randomly sampling a bipartite graph with 1000 variable nodes each with degree 5, and 500 check nodes each with degree 10. We take the feedback attenuation parameter \( \gamma = 0.01 \), set the feedback power to 1 (arbitrary units), the probe power to something much larger (\( 10^5 \)), set the rate for spontaneous component flips \( \eta = 0 \), and the fan-out power \( l |\alpha_{\ell-o}|^2 \) to \( \infty \) (thus ignoring the effects of fan-out; see section 4.5 for explanation). Figure 7 shows the number of errors remaining as a function of time averaged over 999 trajectories, and for three individual trajectories. 999 of 1000 trajectories decoded successfully (converged the all-0 codeword). The one that did not is not included in the average.

We point out two features of the trajectory simulations. One is that (e.g. the red trajectory in figure 7) the number of errors remaining sometimes increases in the course of a simulation.

### Table 1. Simulation parameters

| parameter          | symbol | notes                      |
|--------------------|--------|----------------------------|
| Block length       | \( n \) |                            |
| Checks per variable| \( l \) | \( m = nl/k \) parity-checks |
| Variables per check| \( k \) |                            |
| Probe amplitude    | \( \alpha_{pr} \) |                          |
| Feedback amplitude | \( \alpha_{fb} \) | power \( \sim \alpha l^2 \) |
| Fan-out amplitude  | \( \alpha_{\ell-o} \) |                        |
| Feedback power     | \( 0 < \gamma < 1 \) | rate to flip variable \( \alpha_{fb} \gamma \# \text{satisfied checks} \) |
| Spontaneous flip rate | \( \eta \) | all latches independently flip state with rate \( \eta \) |
As discussed in our circuit description in section 4.3.2, the circuit induces errors at some non-zero rate and then corrects the induced errors. Errors are most likely to be induced for variables that are involved in some, but not a majority of parity-check violations. When the attenuation constant $\gamma$ is too high (too little attenuation), the circuit may induce errors faster than they are corrected, resulting in a failure to decode. On the other hand, as $\gamma$ is decreased, the circuit corrects errors at a lower rate, suggesting an optimal value of $\gamma$ in terms of a performance vs. decoding time tradeoff. This tradeoff is considered in the next section.

Second, the empirical mean of 999 trajectories (black trace in figure 7) exhibits three shoulders (alternates between being locally convex and concave) in its decay toward 0. The shoulders are spaced approximately $1/\gamma = 100$ logarithmic time units apart, corresponding to the correction of errors that are involved in 5, 4 and 3 parity-check violations, respectively. The mean number of errors remaining first declines significantly at time $t \sim 10^0$, consistent with feedback at maximal rate (no attenuation) $|\alpha_{fb}|^2 = 1$ flipping variables all $l = 5$ of whose corresponding parity-check constraints are initially unsatisfied.

5.3. Performance vs. initial number of errors

We simulate our decoding circuit using the same code parameters as [6]: a $(n = 40000, l = 5, k = 10)$ expander code, generated by randomly sampling a bipartite graph with 40000 variable nodes, 20000 check nodes, and degrees 5 and 10 at the variable and check nodes, respectively. The performance of our decoder in simulation for these parameters is shown in figure 8. This performance (top panel) is somewhat better than that of [6]'s scheme and somewhat worse than their version of the scheme permitting some backwards progress—occasionally allowing the total number of parity constraint violations to increase.
We see in figure 8 (top) that the decoder’s performance in terms of block error rate appears to saturate as the attenuation parameter $\gamma$ decreases. At the same time, the median time to successfully decode grows as $\gamma$ decreases (bottom), since the rate to flip bits scales exponentially in $\gamma$ (equation (3)). Thus, we could set $\gamma$ to the highest achievable value for a given channel error probability, desired mean decoding time, and probability to decode successfully.

5.4. Performance vs. input power with noisy circuit components

We consider the decoder’s performance as a function of applied input power in terms of probability to decode, decoding rate (bits/s), and decoding energy (bits/J). Additionally, we set some non-zero rate $\eta$ at which the circuit components undergo spontaneous flips ($0 \leftrightarrow 1$). This noise affects both the variable and the check latches and in turn both the measurement and feedback parts of the circuit. Figure 9 shows our numerical results for fixed component noise rate $\eta$, LDPC code parameters, initial number of errors, and attenuation parameter $\gamma$ (see caption for parameter values).

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We use the median, rather than the mean, time because as the probability to successfully decode drops sharply around 1800 initial errors, the distribution of decoding times spreads out over orders of magnitude (see figure 8, bottom), with the mean dominated by the few longest trajectories. We imagine in actual use, we would operate some distance (in number of initial errors) below the point at which the decoder breaks down.
We see (top panel of figure 9) that to decode successfully most of the time, the feedback power needs to be large enough to overcome the errors induced by noise in the circuit components, but not much larger than the probe power. When the feedback power is much larger than the probe power, the probe circuit is too slow to turn off the feedback once an error is corrected and too slow to turn on the feedback for new errors (induced by either the feedback or spontaneous flips), so the feedback system may induce more errors than it corrects.

For the bottom panel of figure 9, we fixed the probe to feedback power ratio at 1 and plotted the mean decoding rate and energy vs. input power in bit/unit time, bit/unit energy, respectively. We defined the decoding rate as the reciprocal of the mean decoding time, conditioned on successfully decoding, and the decoding power as the decoding rate divided by

![Figure 9. Decoder performance with varying probe and feedback power in the presence of component noise. (top, grayscale) Fraction of trials that decoded all of the initial errors successfully vs. probe and feedback power. (top, red dashed line) fixed probe to feedback power ratio (ratio value 1). (bottom) section of top plot (marked by red dashed line) corresponding to a fixed probe to feedback power ratio. (bottom, magenta) mean decoding rate in bits/unit time. (bottom, blue) mean decoding energy (ratio of mean decoding rate and input power). Both performance measures are conditioned on successfully decoding all errors. See footnote for a time and energy estimate in J and s. Component spontaneous flip rate $\eta = 10^{-8}$. $\gamma = 0.01$. Fan-out amplitude $\alpha_{f-o} = \infty$. Expander LDPC code parameters: block length 40000, $l = 5$, $k = 10$, 1700 initial errors. We sampled 3000 trajectories per grayscale point.](image)
the input power. We see that for large enough input power, the decoding rate is proportional to the input power, while the energy cost per decoded bit is constant.

See footnote\textsuperscript{5} for a calculation of a fiducial time and energy budget for a nitrogen-vacancy latch. It is useful for comparison to imagine implementing the same scheme using classical latches from electronics and to consider its power requirements. This comparison is difficult to make directly; we discuss the relevant issues and make an estimate in\textsuperscript{6}.

\textsuperscript{5} These are in arbitrary time and energy units proportional to $s$ and $J$, since we did not give physical values for our simulation parameters. To compute a fiducial time and energy to decode, we reference the latch switching time estimated in [9] using the parameters of [34] for a gallium phosphide photonic resonator and diamond nitrogen-vacancy system: $\tau_{sw} \approx 7\mu s$ per switch at 1 pW set/reset input power. For 1700 initial errors in figure 8, we see (bottom panel) the time to decode scales as $1/\gamma^2$, suggesting that the time to correct errors that satisfy 2 out of 5 parity-check constraints dominates the total decoding time. The feedback power to correct these errors is attenuated by a factor of $\gamma^2$, so the mean time for switching them is $\tau_{sw}/\gamma^2$. Setting the feedback power to 1 pW, $\gamma = 10^{-2}$ (this is the highest value of $\gamma$ shown in figure 8 such that the decoder succeeds for most trajectories with 1700 initial errors), we estimate the time to decode to be $\sim \tau_{sw}/\gamma^2 = 7\mu s/(10^{-2})^2 = 70\text{ms}$, the energy to decode to be $7\text{s} \cdot (\text{input power}) = 70\text{ms} \cdot 1\text{pW} = 70\ \text{fJ per latch};$ The set/reset inputs of each latch in the circuit receive 1 pW input power, so this estimate gives the energy to decode per latch. There are 60,000 total latches in the decoder circuit for the parameters in figure 8 (40,000 variables, 20,000 checks), so the total energy to decode is $\sim (\text{energy per latch}) \cdot (\text{number of latches}) \approx 70\text{fJ} \cdot 60,000 \approx 4\text{nJ}$.

\textsuperscript{6} Several points make it difficult to port our scheme to one that uses classical SR NAND latches in place of the optical ones. Our implementation relies upon partial attenuation of optical power to control the latch switching rate, while a classical latch may have only one operating power. Thus it could be easier with classical latches to implement a hard thresholding feedback [see figure 4(a)] than our softer optical nonlinearity; this hard threshold would require additional circuit components to determine if a majority of parity-check constraints is violated (and possibly a clock). Moreover, the optical latches operate asynchronously and update their state at random times, thus providing a randomized update schedule for the decoding algorithm. Classical latches can be clocked or operate asynchronously; clocked, parallel operation was considered in [6], but in the asynchronous case it is not clear how the corresponding update schedule affects the decoder performance. Further, an implementation with classical latches in electronics would depend for its correctness on the details of how the latches function in the forbidden ‘SET low and RESET low’ regime exploited by our optical latches, or else the circuit must be modified with additional components to achieve the desired behavior. Setting these circuit architecture issues aside, we can at least estimate a lower bound for a power budget for an implementation that naïvely replaces each optical latch with a classical one. For the parameters in footnote\textsuperscript{5}, there are 1700 initial bit errors, and each bit node is connected to 5 parity-check nodes. In total, then, about 10,000 latches must switch their state at least once in the course of decoding. Approximating each classical latch as a single transistor and assuming an energy scale of $\sim 1\text{pJ per transistor switch}$, this yields a crude lower bound of 10nJ for decoding, slightly larger than the estimate in footnote\textsuperscript{5}. This budget does not consider the extra power required for circuit fan-out (an additional factor of 10 per bit node), electrical signal propagation losses, and the extra costs of any additional components required to make the classical version work (like clocks and counters, discussed above). Decoding time could be faster with a classical implementation; we use a switching time-scale of 7 microseconds for a nitrogen-vacancy system in footnote\textsuperscript{5}, while transistor switching times can be sub-nanosecond. This speed advantage would depend, however, on the implementation of the extra components (like counters) for the classical circuit. Direct comparison is again difficult, as the optical scheme corrects ‘easy’ errors (those for which every parity-check is violated) faster than harder errors due to optical power attenuation scaling discussed in section 4.3.2, while classical latches might use a single power level. A reasonable idea would be to correct the easy errors cheaply using an optical scheme and hand off the incomplete result to a faster, more energy-expensive classical circuit.
5.5. Performance vs. fan-out power

The previous numerical results were obtained for infinite fan-out amplitude $\alpha_{f-o}$, allowing us to ignore the impact on decoding performance of the extra fan-out latches described in section 4.5. Here, we consider varying the fan-out amplitude $\alpha_{f-o}$. Figure 10 shows our numerical results for fixed LDPC code parameters (same as for figures 8 and 9), fixed attenuation parameter $\gamma$, varying initial number of errors, and equal probe and feedback amplitudes $\alpha_{pr} = \alpha_{fb}$ (see caption for parameter values).

We see that for high fan-out power ($\alpha_{f-o}/\alpha_{fb}^2 \geq 10$) the decoder’s performance in terms of block error rate vs. initial number of errors appears to saturate to the infinite fan-out power curve in figure 8. For the case $|\alpha_{f-o}/\alpha_{fb}|^2 = 1 (=|\alpha_{f-o}/\alpha_{pr}|^2)$ there is a moderate reduction in performance (about 3%) in terms of maximum number of errors decoded with given block error probability. Decoder performance degrades dramatically for $|\alpha_{f-o}/\alpha_{pr}|^2 < 10^{-1}$.

Given the above observations, it is reasonable to set $\alpha_{f-o} = \alpha_{fb} = \alpha_{pr}$ in computing an energy budget for our circuit using actual physical components. This choice of $\alpha_{f-o}$ doubles the fiducial energy budget computed in footnote 5 for a gallium phosphide photonic resonator and diamond nitrogen-vacancy system.

6. Discussion

We have described a photonic circuit that implements an iterative decoding scheme for expander LDPC codes. This circuit consists of a collection of optical latching relays whose interactions via coherent fields map naturally onto the subroutines of the iterative decoder.

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7 We refer to the red curve in figure 8, corresponding to the attenuation parameter $\gamma = 10^{-2}$. The simulations for figure 8 used a higher probe amplitude ($\alpha_{pr} = 10^3$) than the finite fan-out power simulations for figure 10 ($\alpha_{pr} = 10$), leading to slightly better performance in this metric.
This circuit is autonomous—it is powered by the same optical signals that it acts upon to implement the decoding procedure, and it requires no external controller, measurement system, or clock signal. It operates robustly in the low-power limit in which quantum fluctuations of the optical fields are significant. The feedback-induced latch state fluctuations provide a natural source of randomness to drive the decoding algorithm. Crucially for the feasibility of such a system, our circuit’s performance, as measured by decoding time and error rate, can be tuned smoothly by varying the optical input power. Tuning the input power can be done without loss in efficiency, as our circuit decodes a constant number of bits per Joule at a rate linear in the input power. Thus, noise that acts on the circuit components and potentially disrupts the computation can be overcome by increasing input power until the circuit works.

Our construction highlights the computational utility of cavity QED-based nanophotonic components for ultra-low-power classical information processing, and points to the utility of the probabilistic graphical model framework in engineering autonomous optical systems that operate robustly in the quantum noise regime.

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Appendix A. Gough–James circuit algebra

We briefly review the Gough–James treatment of open quantum systems and circuits composed of such systems [19, 20]. We give sufficient detail for the reader to reproduce our numerical simulations.

A.1. Open quantum systems

In the Gough–James circuit algebra for modeling open quantum systems, a system coupled to \( n \) external fields is parametrized by a \((S, L, H)\) triplet, where the scattering matrix \( S \) is \( n \) by \( n \) unitary with operator-valued entries, the coupling vector \( L \) is \( n \) by 1 with operator-valued entries, and \( H \) is the system’s Hamiltonian. Figure 11 summarizes this picture. The density matrix \( \rho \) for the system’s internal degrees of freedom evolves in time according to the master equation [equation (2)]:

\[
\dot{\rho}_i = -i [H, \rho_i] + \sum_{j=1}^{n} \left( L_i \rho_j L_i^\dagger - \frac{1}{2} \left\{ L_i^\dagger L_i, \rho_i \right\} \right)
\] (A.1)

where \([A, B] = AB - BA\), \( \{A, B\} = AB + BA\), and \( \dagger \) denotes conjugation. The scattering matrix \( S \) does not appear in (2), but appears when we interconnect such systems below.

A.2. Circuits

The Gough–James circuit algebra allows us to compute new \((S, L, H)\) triplets in terms of old for two systems connected in series, in parallel, or for one system self-connected through feedback. We briefly state these circuit composition rules.
The series product takes two open quantum systems \( G_1(S_1, L_1, H_1), \) \( G_2(S_2, L_2, H_2) \) coupled to an equal number of external modes and returns the system \( G_2 \triangleleft G_1 \) obtained by feeding the outputs of \( G_1 \) into the inputs of \( G_2 \):

\[
G_2 \triangleleft G_1 = \left( S_2 S_1, S_2 L_1 + L_2, H_1 + H_2 + \imath \left( L_2^* S_2 L_1 \right) \right) \quad (A.2)
\]

The concatenation product takes two open quantum systems \( G_1 \) and \( G_2 \), coupled to \( n_1 \) and \( n_2 \) modes, respectively, and returns the system \( G_1 \boxplus G_2 \) obtained by considering the two systems as one system coupled to \( n_1 + n_2 \) modes and introducing no interactions between them:

\[
G_1 \boxplus G_2 = \left( \left( \begin{array}{cc}
S_2 & 0 \\
0 & S_1
\end{array} \right), \left( \begin{array}{c}
L_1 \\
L_2
\end{array} \right), H_1 + H_2 \right). \quad (A.3)
\]

The feedback product takes a single open quantum system coupled to \( n \) modes and returns the system \( [G]_{k\rightarrow l} \) obtained by feeding back the \( k \)th output mode to the \( l \)th input mode, coupled to \( n - 1 \) external modes. The form of this product is given in [19] (section 5) and in the notation used here in [25], appendix A.

### Appendix B. Components

We describe the components we need for our decoder circuit in terms of an \((S, L, H)\) triplet, focusing on an intuitive input–output picture.

#### B.1. Beamsplitter

To give an intuition for these systems and to specify the components we need, we first describe the beamsplitter as an open Markov quantum system. A 50/50 beamsplitter has two input and two output ports and is parametrized by:

\[
B = \left( \begin{array}{cc}
S = \frac{1}{\sqrt{2}} \left( \begin{array}{cc}
1 & 1 \\
-1 & 1
\end{array} \right), & L = \left( \begin{array}{c}
0 \\
0
\end{array} \right), & H = 0
\end{array} \right) \quad (B.1)
\]

By examining the scattering matrix, we see that for a field incident into input port 1, half the power is transmitted into output port 1 and half is reflected into output port 2 with a \( \pi \) phase shift. The beamsplitter has no internal degrees of freedom that concern us here, so \( L = 0 \) and \( H = 0 \). The scattering matrix for a beamsplitter that transmits a fraction \( \gamma < 1 \) of incident power—our attenuation component—is a 2 by 2 rotation matrix with angle \( \arccos \sqrt{\gamma} \).
B.2. Coherent input field

A coherent input field is modeled as a Weyl operator $W_{\vec{a}}$, which displaces $n$ vacuum inputs into coherent states $|\alpha_1\rangle$, ..., $|\alpha_n\rangle$ with amplitudes $\alpha_1$, ..., $\alpha_n$:

$$W_{\vec{a}} = \begin{pmatrix} S = I_{n \times n}, & L = \begin{pmatrix} \alpha_1 \\ \vdots \\ \alpha_n \end{pmatrix}, & H = 0 \end{pmatrix}$$  \hspace{1cm} (B.2)

For example, driving the beam splitter above with $|\alpha\rangle$ in the first input and $|\beta\rangle$ in the second input results in the series connection:

$$B \triangleleft W_{(\alpha, \beta)} = \begin{pmatrix} S = \frac{1}{\sqrt{2}} \begin{pmatrix} 1 & 1 \\ -1 & 1 \end{pmatrix}, & L = \frac{1}{\sqrt{2}} \begin{pmatrix} \alpha + \beta \\ -\alpha + \beta \end{pmatrix}, & H = 0 \end{pmatrix},$$  \hspace{1cm} (B.3)

resulting in the mixing of the two inputs in the two outputs, as we expect.

B.3. Latch

In terms of an $(S, L, H)$ triplet, the latch is given by the concatenation (parallel product) of two systems: $Q_{\text{set-reset}}$ accepts the set and reset inputs and drives the latch into the $|0\rangle$ or $|1\rangle$ state, and $Q_{\text{in-out}}$ routes the input fields $in_{1,2}$ into the output fields $out_{1,2}$. We have $Q = Q_{\text{set-reset}} \boxplus Q_{\text{in-out}}$, where

$$Q_{\text{set-reset}} = \begin{pmatrix} S_{\text{set-reset}} = \begin{pmatrix} \Pi_0 & -\sigma_{01} \\ -\sigma_{01} & \Pi_1 \end{pmatrix}, & L_{\text{set-reset}} = \begin{pmatrix} 0 \\ 0 \end{pmatrix}, & H = 0 \end{pmatrix},$$  \hspace{1cm} (B.4)

$$Q_{\text{in-out}} = \begin{pmatrix} S_{\text{in-out}} = \begin{pmatrix} \Pi_0 & -\Pi_1 \\ -\Pi_1 & \Pi_0 \end{pmatrix}, & L_{\text{in-out}} = \begin{pmatrix} 0 \\ 0 \end{pmatrix}, & H = 0 \end{pmatrix},$$  \hspace{1cm} (B.5)

where $\Pi_0 = |0\rangle \langle 0|$ and $\Pi_1 = |1\rangle \langle 1|$ are projection operators onto the $|0\rangle$ and $|1\rangle$ states and $\sigma_{01} = |0\rangle \langle 1|$. Conditional on the state of the latch, either $S_{\text{in-out}} = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}$ or $S_{\text{in-out}} = \begin{pmatrix} 0 & -1 \\ -1 & 0 \end{pmatrix}$, thus either switching or not switching the input fields. This is the same latch model as that used in our earlier work [7].

A possible physical system that achieves this desired behavior is shown in figure 2 and was first proposed in [9]. The $|0\rangle$ and $|1\rangle$ states are degenerate ground states of an atom in a cavity. Set, reset, and input fields are resonant with transitions to one of two excited states ($|e\rangle$ and $|s\rangle$), from which the atom then decays back into one of the ground states. In a regime of strong atom-cavity coupling, the limiting behavior of the switch system is obtained by using the QSDE limit theorem [33] to adiabatically eliminate the excited state dynamics. An alternate proposal for such a switch using a Kerr cavity is found in [10].
Appendix C. Bounds on nonlinearity of feedback

Consider a \((n, l, k)\) LDPC code, and suppose there is only one variable \(v\) that needs to be flipped to return to a codeword. This variable participates in \(l\) parity-check constraints, all of which are violated, so it flips at some maximal rate \(r\). These \(l\) parity-check constraints together include at most \(l(k-1)\) variables other than \(v\) (at most because they may have some in common), each of which is involved in least one parity-constraint violation, and so flips with a rate of at least \(ry^{l-1}\). The total rate for erroneously flipping any variable other than \(v\) is then

\[
R_{\text{err}} = l(k - 1) r y^{l-1}.
\]

In order to flip \(v\) before errors accumulate, we set \(r > R_{\text{err}}\) and find

\[
\gamma < \left( \frac{1}{l(k-1)} \right)^{\frac{1}{l}}.
\]

In our numerical tests we have used \(l = 5, k = 10\), yielding \(\gamma < 0.38\). Numerically, we found that our decoder mostly fails to decode already for \(\gamma = 0.1\) (see figure 8), but this is an upper bound assuming only total error.

Appendix D. Fan-in/Fan-out

As discussed in section 4.3, our circuit requires a latch component \(Q_{\text{var}}\) corresponding to variable bit \(v\) to participate in multiple \((l)\) parity-check constraints, and a latch \(Q_{\text{check}}\) corresponding to parity-check \(c\) to feed back to multiple \((k)\) variables. Since the latch described in section 4.2 and appendix B routes only two input and two output ports (in/out1, 2), it is insufficient for our needs: we need a latch that routes multiple in/out1, 2 signal pairs—switching each pair if and only if the latch state is \(|1\rangle\) (see upper panel of figure 12). We can augment our latch to achieve the desired fan-in/fan-out in two ways.

D.1. Routing multiple signals

One way is to simply add extra input/output ports to the latch system depicted in figure 2: we could have input pairs in/out1, 2 for \(i \in \{1, \ldots, N\}\) and the corresponding outputs (in addition to the two set/reset ports) for some integer \(N\), all coupled to the same latch state. This would be difficult to achieve in a nanophotonic system, if only due to constraints of geometry—it would be difficult to have multiple beam paths access a single structure in a planar circuit.

An alternate scheme is depicted in figure 12. The idea is to break up each latch into a set of \(N\) subsystems \(Q_{\text{route}}^{(1)}, \ldots, Q_{\text{route}}^{(N)}\), each responsible for routing a single in/out signal pair, and a single subsystem \(Q_{\text{sr}}\) responsible for accepting the set/reset inputs (see figure 12). Each of the \(N + 1\) subsystems is another latch, but one that routes only a single in/out signal pair and fits the description of section 4.2. The set/reset subsystem \(Q_{\text{sr}}\) routes power (in orange path in figure 12) to the set/reset ports of the \(N\) routing subsystems \(Q_{\text{route}}^{(i)}\), driving the state of each routing subsystem to match the state of the set/reset subsystem. Thus the \(N\) routing subsystems \(Q_{\text{route}}^{(i)}\) all mirror the overall system state, defined as the state of the set/reset subsystem \(Q_{\text{sr}}\). This construction introduces a delay in distributing the state of the set/reset subsystem to the \(N\) routing subsystems—due to both the waiting time for a routing subsystem to switch and
to the time for a signal to propagate around a circuit (we do not model the latter source of delay for this circuit). The construction also introduces extra circuit components that could be subject to noise (e.g., spontaneously changing their state). We thus need to use high-enough fanout power (proportional to $|\alpha_{\ell_0}|^2$, in the orange path in figure 12) to make this construction useful.

D.2. Accepting multiple set/reset inputs

We note that we can use a similar construction to make a latch system that accepts multiple set/reset inputs in addition to routing multiple in/out signal pairs; though such a system does not appear in our decoder circuit, it may be useful for other purposes. When there are multiple set/reset input pairs for a device, these inputs lose their interpretation as ‘set’ and ‘reset’ for the electronic latch. We can instead associate each set/reset pair with an internal state and define an overall state as the sum modulo 2 of these internal states, so that changing any of the internal states changes the overall state. This behavior could be useful if we are interested in having a circuit component with multiple ‘flip’ control inputs.

The idea is to break up the set/reset latch subsystem described above into a set of $M$ subsystems $Q_{sr}^{(j)}$, $j \in \{1, \ldots, M\}$, each of which accepts only a single set of set/reset inputs. The overall system state is then defined as the sum modulo 2 of the set/reset subsystems, so flipping the state of any of them changes the overall state. The sum modulo 2 is performed as for the parity-check circuit described in section 4.3.1 and shown in figure 3(b). The probe beam path [black path in figure 3(b)] would now access each of the $Q_{sr}^{(j)}$ subsystems in sequence before driving the set or reset port of each of the $Q_{route}^{(j)}$ subsystems, as described in the previous subsection (orange path in figure 12).
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