Improved performance of InSe field-effect transistors by channel encapsulation

Guangda Liang¹, Yiming Wang¹, Lin Han¹, Zai-Xing Yang¹,², Qian Xin¹,²,⁶, Zakhar R Kudrynskyi³, Zakhar D Kovalyuk⁴, Amalia Patanè³ and Aimin Song¹,⁵,⁶

¹Center of Nanoelectronics and School of Microelectronics, Shandong University, Jinan 250100, People’s Republic of China
²Shenzhen Research Institute of Shandong University, Shenzhen, 518057, People’s Republic of China
³School of Physics and Astronomy, University of Nottingham, Nottingham NG7 2RD, United Kingdom
⁴Institute for Problems of Materials Science, The National Academy of Sciences of Ukraine, Chernivtsi Branch, Chernivtsi 58001, Ukraine
⁵School of Electrical and Electronic Engineering, University of Manchester, Manchester M13 9PL, United Kingdom

E-mail: xinq@sdu.edu.cn and A.Song@manchester.ac.uk

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Abstract

Due to the high electron mobility and photo-responsivity, InSe is considered as an excellent candidate for next generation electronics and optoelectronics. In particular, in contrast to many high-mobility two-dimensional (2D) materials, such as phosphorene, InSe is more resilient to oxidation in air. Nevertheless, its implementation in future applications requires encapsulation techniques to prevent the adsorption of gas molecules on its surface. In this work, we use a common lithography resist, poly(methyl methacrylate) (PMMA) to encapsulate InSe-based field-effect transistors (FETs). The encapsulation of InSe by PMMA improves the electrical stability of the FETs under a gate bias stress, and increases both the drain current and electron mobility. These findings indicate the effectiveness of the PMMA encapsulation method, which could be applied to other 2D materials.

Keywords: InSe, 2D semiconductor, bias stress, PMMA encapsulation

(Some figures may appear in colour only in the online journal)

1. Introduction

The isolation of graphene and other two-dimensional (2D) materials has raised expectations for a revolution in electronics and optoelectronics [1–3]. However, graphene has a zero band gap, which prevents its use in many applications. Thus, continuous efforts have turned to explore other 2D materials with a band gap, such as transitional metal dichalcogenides [4–6], black phosphorus [7, 8], and III–VI group semiconductors [9, 10]. Among the III–VI semiconductors, InSe has emerged as a promising material due to its direct band gap over a range of layer thicknesses and light in plane electron effective mass \( m_{\text{InSe}}^* = 0.14m_0 \) [11]. High performance few-layered InSe photodetectors were reported by Tamalampudi et al demonstrating a responsivity that is four orders of magnitude higher than that of MoS2 and graphene phototransistors [12]. Also, Feng et al have reported multi-layer InSe field-effect transistors (FETs) on SiO2/Si substrate, reaching field-effect mobilities of 162 cm² V⁻¹ s⁻¹ at room temperature [13]. These mobilities can be further increased up...
to 1055 cm² V⁻¹ s⁻¹ by using poly(methyl methacrylate) (PMMA)/Al₂O₃ as dielectric layer rather than SiO₂ due to a significant reduction of carrier scattering by surface charged impurities and polar phonon scattering [14]. Although layered InSe exhibits outstanding optical and electrical properties [12, 15, 16], and better resilience to oxidation under ambient conditions than many other 2D materials, the electrical stability and performance of InSe-based devices can be affected by the exposure and interaction of the InSe surface to chemical species in air, such as water or oxygen [17]. For example, Balakrishnan et al have shown that the oxidation of InSe surface in air can be induced by both thermal and photo annealing, which converts a few surface layers of InSe into In₂O₃, thus forming an InSe/In₂O₃ heterostructure [18]. On the other hand, Feng et al have demonstrated that InSe-based FETs become unstable under a gate bias stress due to the absorption (desorption) of oxygen and water on the InSe surface [19]. Thus, the development of techniques for improving the stability in air of InSe-based devices is critical to future applications.

PMMA is an ideal encapsulation dielectric to isolate the channel of FETs from air. Being readily available as a standard electron-beam lithography resist of high purity, it can be dissolved easily into organics and can be used to form thin films by a simple spin-coating process [4, 20]. Furthermore, PMMA has been used to modify the surface states of semiconductors, resulting in improved performances, as shown by Bao et al who have used PMMA to encapsulate the channel of MoS₂-based FETs, thus increasing the carrier mobility [4]. In this work, we use PMMA as the channel encapsulation to improve the performance of InSe-based FETs. The electrical stability of InSe FETs is investigated in response to a constant gate bias stress (±40 V) for 300 s under ambient conditions. The encapsulation of InSe by PMMA enables the fabrication of FETs with higher mobility and significantly improved electrical stability. This work offers a convenient method to improve the mobility and stability of 2D-material-based devices.

2. Methods and results

We use InSe-based FETs with and without encapsulation of the InSe layer by PMMA, as shown in figures 1(a) and (b). The InSe layers are prepared from bulk Bridgman-grown rhombohedral γ-InSe by mechanical exfoliation using adhesive tape and deposited on SiO₂/μ-Si substrates for the fabrication of InSe FETs. The primitive unit cell of γ-InSe contains three layers, each consisting of four closely packed, covalently bonded, atomic sheets in the sequence Se–In–In–Se; within each layer plane, atoms form hexagons (figure 1(c)) [21]. The source and drain electrodes, Ti/Au (10/40 nm), are defined by shadow masks and deposited by electron-beam evaporation. For the channel encapsulation, 200 nm PMMA (950 K, 4.5 wt%) is spin-coated onto the FETs and baked at 110 °C for 2 h. A typical optical image of the unencapsulated InSe FET is shown in the right part of figure 1(c). This has a channel length \( L = 50 \mu m \) and width \( W = 45 \mu m \). The corresponding thickness \( t \) of the InSe layer is approximately \( t = 40 nm \), as measured by atomic-force microscopy (figure 1(d)).

The electrical performance of the fabricated back-gated FETs is characterized with a standard electrical probe station and an Agilent 2902A semiconductor analyzer. As shown by the transfer and output characteristics in figures 2(a) and (b), the InSe FET shows n-type behavior. For transfer characteristics, as shown in figure 2(a), the \( V_GS \) sweep takes 16 s (0.75 V/step), from \( V_GS = -30 \) to +30 V at \( V_DS \) of 0.1 V, and another 16 s for the sweep back from \( V_GS = +30 \) to -30 V. Following the encapsulation of InSe by PMMA, the on current increases from 2.0 to 3.4 \( \mu A \) at \( V_GS = +30 \) V, and the width of the hysteresis loop decreases from 8.2 to 4.0 V. For the output characteristics, the current \( I_DS \) is measured for \( V_DS \) swept from 0 to +30 V while stepping \( V_GS \) from \( -30 \) to +30 V in increments of 12 V, as shown in figure 2(b). The \( I_DS-V_DS \) curves indicate that fairly good ohmic contacts form between InSe and the Ti source/drain electrodes (Ti has a work function of 4.3 eV, slightly smaller than that of InSe around 4.6 eV) [9, 13]. The field-effect mobility of the InSe FETs can be extracted from the transfer curve by the equation [14, 21, 22]:

\[
\mu = \frac{L}{W} \frac{1}{C_I} \frac{dI_D}{dV_G},
\]

where \( C_I \) is the capacitance of SiO₂ with a thickness of 300 nm per unit area (1.15 × 10⁻⁸ F cm⁻²) [23]. We find that with PMMA encapsulation, the electron mobility increases from 186 to 220 cm² V⁻¹ s⁻¹. A similar improvement is measured on other FETs in which the InSe layer thickness ranges from 20 to 70 nm. As shown in figure 2(c), with PMMA encapsulation, all the InSe FETs reveal an improved mobility. In particular, the mobility increases as the layer thickness of InSe increases from 20 to 30 nm, and decreases as the InSe thickness increases from 30 to 70 nm, consistent with a previous report [14]. For thinner layered InSe, the interaction distance between charged impurities on the
substrate and free carriers in InSe is smaller, which enhances carrier scattering and reduces the mobility. For thicker InSe layers, because the source and drain electrodes are contacted only directly to the top InSe layer, electron transport into the bottom layers involves additional interlayer resistors, resulting in a lower mobility of the FETs.

The electrical stability of the as-fabricated FETs is investigated by applying a constant gate bias stress ($\pm 40$ V) for 300 s. The transfer characteristic curves are measured immediately after the bias stress at $V_{DS} = 1$ V and at regular time intervals. For the unencapsulated FET, after applying a gate bias stress of $-40$ V, the drain current increases from 26 to 30 $\mu$A at $V_{GS} = +30$ V, and the threshold voltage shifts in the negative direction ($\Delta V_{th} = -7.4$ V), as shown in figure 3(a). After applying a gate bias stress of 40 V, the drain current decreases from 25 to 13 $\mu$A at $V_{GS} = +30$ V, and the threshold voltage increases ($\Delta V_{th} = 4.3$ V), as shown in figure 3(b). For the PMMA encapsulated FET, after applying a gate bias stress of $-40$ V, the drain current increases from 31 to 34 $\mu$A at $V_{GS} = +30$ V, and the threshold voltage reduces ($\Delta V_{th} = -3.5$ V), as shown in figure 3(c). On the other hand, for a gate bias stress of $+40$ V, the drain current decreases from 30 to 20 $\mu$A at $V_{GS} = +30$ V, and the threshold voltage increases ($\Delta V_{th} = 2.5$ V), as shown in figure 3(d). Figures 3(e) and (f) compare the changes of the threshold voltage and mobility for each measurement with the values of the pre-biased devices. The PMMA encapsulated FET shows much smaller shifts of the threshold voltage for both positive and negative gate bias stress than those for the
FET without the encapsulation. Also, after PMMA encapsulation, the mobility is less sensitive to the gate bias stress, as shown in figure 3(f). Without PMMA encapsulation, the mobility decreases by 22.3% from 76 to 59 cm² V⁻¹ s⁻¹ after a positive gate bias stress, and increases by 14.4% from 76 to 87 cm² V⁻¹ s⁻¹ after a negative gate bias stress. With PMMA encapsulation, the mobility decreases by 13.0% from 100 to 87 cm² V⁻¹ s⁻¹ after a positive gate bias stress, and increases by 5.0% from 100 to 105 cm² V⁻¹ s⁻¹ after a negative gate bias stress. As such, our results demonstrate an improved stability of InSe FETs by using PMMA for the encapsulation.

3. Discussion

To discuss the results, we consider the energy band diagram in figure 4. Under the ideal condition, without gate bias stress, electron accumulation forms at each Ti/InSe interface because the electron affinity of InSe (≈4.5 eV) is higher than the work function of Ti (≈4.3 eV) [25], as shown in figure 4(a). However, under ambient condition, the InSe channel surface is subject to the adsorption of water and oxygen molecules in air [26–29]. For example, Bickley et al. studied photoadsorption at rutile surface, indicating that the adsorption oxygen could capture electrons from the rutile surface and form negatively charged species (O₂⁻) through the reaction:

\[ \text{O}_2(e) + e^- \rightarrow \text{O}_2^-(s), \tag{2} \]

where O₂⁻(s) donates the adsorbed oxygen on the surface and O₂(e) donates the neutral oxygen in gas form [26]. Such adsorption of oxygen has also been observed in IGZO [28–30] and MoS₂ [31] devices. Lopes et al. investigated the performance of IGZO TFT with water vapor exposure. The drain current exhibited an apparent increase after water vapor exposure [29]. Fuh et al. further studied the effect and summarized the reaction as:

\[ \text{H}_2\text{O}(g) \rightarrow \text{H}_2\text{O}^+(s) + e^-, \tag{3} \]

where H₂O⁺(s) donates the adsorbed water molecule and H₂O(g) donates the neutral water molecule [28], meaning that an adsorbed water molecule can be positively charged on the channel surface by releasing an electron.

Here, such adsorption/desorption of oxygen and water is also expected to occur on the InSe channel, while the contact region is not affected by such adsorption/desorption[32]. Under ambient conditions, pristine defects and dangling bonds on the surface of InSe can facilitate absorption of oxygen or water from air, thus forming charged species that affect the band bending and the electrical transport [29, 33]. With a positive gate bias stress, the increase of electron concentration facilitates the adsorption of oxygen and desorption of water, resulting in a more negative surface and hence an increase of electrons depletion in the InSe channel. In this case, the electrons have to traverse a higher channel-depletion-induced barrier during the transport process, as shown in figure 4(b), causing a decline of drain current and a positive shift of threshold voltage. On the other hand, with a negative gate bias stress, the decrease of electron concentration in the FET facilitates desorption of oxygen and adsorption of water, resulting in a release of electrons from oxygen and water. As a result, the channel depletion-induced barrier decreases, making the transport of electrons easier, as shown in figure 4(c). This causes the increase of drain current and the negative shift of threshold voltage. By using PMMA to isolate InSe from air, the surface states of InSe channel is reduced, resulting in reduced scattering and increased mobility. Furthermore, owing to the isolation from water or oxygen in ambient air, InSe FETs become more stable under both positive and negative bias stresses as observed in figures 3(e) and (f).

4. Conclusion

In conclusion, PMMA has been used for the channel encapsulation to improve the performance of back-gated InSe FETs in air. A number of devices with InSe channel of different thicknesses have been fabricated. All devices showed increased mobility as well as bias-stress stability after the encapsulation. The effect can be explained by the isolation of InSe channel surface from adsorption of oxygen and water in air. Our study may have implications for a better design of functional nanodevices based on 2D layered materials for a wide range of device structures.

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**ORCID iDs**

Qian Xin @ https://orcid.org/0000-0003-4605-5894  
Aimin Song @ https://orcid.org/0000-0001-6550-518X

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