Optimization techniques for p-GTO thyristor design

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Abstract. A new type of semiconductor power device was devised in the early '90s as an alternative to the classic Gate Turn-Off (GTO) thyristor. Because the low-doped n-base was replaced by a low-doped p-base, it was called the p-GTO. Its main advantage is a higher possible control voltage when the device is switched off, leading to the possibility of a higher blocking anode current (IATO) and a lower turn-off time. The studies and techniques employed with the help of SILVACO-TCAD simulation software Athena and Atlas show that the p-GTO has higher breakdown voltages compared with its classic counterpart and similar on-state voltage (VT) and switching characteristics when replacing the GTO in the same circuit. Specific circuit improvements, like an affordable higher turn-off gate voltage, will drive the p-GTO into even faster switching operation.

1. Introduction
The GTO thyristor is a p-n-p-n structure which can be switched-on and blocked with positive and respective negative signals applied on the gate, without reversing the voltage applied between anode and cathode [1,2]. The GTO thyristor is usually used as power electronic switch controlled by signals applied on the gate [3]. To improve the parameters of such devices by design means optimising toward the ideal electronic switch which has: null on-resistance, infinite off-resistance, sensibility for the control signal applied on the gate, noise immunity, compact device, high operating frequency (low switching times on-off), high reliability. The most important GTO thyristor performances are the maximum voltage and current and turn-off dynamic characteristics. They are function of device vertical structure parameters like thickness and doping of the semiconductor layers, surface geometry and thermal parameters. The geometrical configuration of gate-cathode architecture is very important to ensure a high rate of gate current evacuation in the turn-off process. The lifetime of the mobile electric charge carriers has a very important role to reduce the blocking time and affect the main device parameters. The thermal parameters of the case influence the thyristor switched power and the semiconductor chip temperature variations influence the device reliability.

2. Fabrication process
The main process (figure 1) starts with the anode (A) realised on boron doped with 10^{18} cm^{-3} concentration silicon wafer. Epitaxially growth of n-base of 2 microns silicon layer doped with phosphorous 10^{16} cm^{-3} concentration is followed by p-base 23 microns epitaxially growth of silicon layer doped with boron 10^{14} cm^{-3} concentration, connected to gate (G). The cathode (K) is processed by 0.2 microns epitaxially growth of silicon layer high doped with boron 10^{19} cm^{-3} concentration. The
The cathode-gate junction is configured by lithographic process and anisotropic etching of 0.2 microns windows in the 0.2 microns-thick epitaxially growth silicon layer highly doped with boron of $10^{19}$ cm$^{-3}$ concentration. Same thickness silicon dioxide is deposited by chemical vapour deposition technique and lithographic patterned and by etching configured to fill the hole resulting by silicon anisotropic etching. The next process step is the 0.1 microns aluminium layer deposition, lithographic patterned and etching configuration of cathode and gate electrodes.

3. The gate-cathode (GK) junction optimization

Because the p-GTO has a low doped p-n junction at the cathode side (unlike the classic GTO) [4], with the help of Athena and Atlas TCAD and simulation software tools of SILVACO [5,6], the structure configuration was optimized on the GK-junction in order to minimize the electric field value at the surface of the junction and in the overall structure, in order to maximize the maximum applicable voltage on the Gate (reverse voltage) and on the Anode (direct voltage) with respect to the Cathode (usually as reference voltage of zero value). First step of process simulator begins with mesh definition [7]:

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LINE X LOC=0.00 SPAC=0.1
LINE X LOC=0.4 SPAC=0.01
LINE X LOC=0.6 SPAC=0.01
LINE X LOC=1.00 SPAC=0.05
LINE Y LOC=0.0 SPAC=0.02
LINE Y LOC=0.2 SPAC=0.05
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to refine the high doping gradient junctions, figure 1:

**Figure 1.** Implantation under the gate area (upper right) of the p-GTO thyristor reduces the value of the electric field. SILVACO Tonyplot [8] output.
For the sake of comparison, it was considered a classic GTO thyristor, with a p+n-pn+ structure and a p-GTO with p+np-n+ structure in which the concentration of the lightly-doped n-, respectively p- bases was the same ($10^{13}$ cm$^{-3}$ as in SILVACO simulation examples) – figure 2.

Two methods were employed to minimize the electric field and so to maximize the breakdown voltage at the GK junction:
- p-doping implant (Boron dose $4 \times 10^{12}$ cm$^{-2}$) was added under the gate contact area, lowering the value of the electric field in that area - figure 2,
- positive bevel of an optimum angle of $45^\circ$ at the gate-cathode junction (figure 1), decreasing the value of the electric field at the junction surface. Figure 1 shows a negative bevel at the GK junction since the upper side of the junction respectively the cathode is higher doped than the gate. The technological feasibility of the bevel is needed to achieve this optimisation, usually achieved by special technical processes.

![Figure 2. SILVACO Tonyplot output of doping profiles regions from right to left a) GTO thyristor: p+n-pn+ and b) p-GTO thyristor: p+np-n+.

4. Comparative results regarding the maximum voltage at the gate-cathode junction

Whereas the maximum (breakdown) voltage of the gate-cathode junction of the comparative classic GTO was obtained 9 volts, the corresponding voltage in the case of the p-GTO was 14.5 volts, which represents an increase of more than 50% in value. Also, in the figures can be observed that the rising of the leakage current is slower in the case of the p-GTO, which usually indicates a better designed junction.
After gate-cathode junction optimization (described above) of the p-GTO structure, the obtained value of the breakdown voltage of the gate-cathode junction was 27 V in the case a positive 45° bevel angle, compared with about 14 V in the cases of negative 45° or vertical 90° angles.

5. **Comparative results regarding the anode to cathode maximum voltage**

Also, in the case of the $V_{AK}$ maximum voltage, a better result was obtained in the case of the p-GTO compared to the classic GTO: 340 vs. 240 volts, figure 3 a) and b). Since the doping of the high-resistive base of the devices was the same, this gain is due entirely to the novel structure of the p-GTO.

6. **Comparative results about the switching characteristics**

To properly compare the switching behaviour of the p-GTO versus the classic GTO thyristor, in both cases was used the very same circuit and simulation procedure provided in the power examples of SILVACO TCAD software. The only modification was to increase the anode inductance from 2.2 μH to 4 μH, because the old value was giving some minor oscillations on the descending front of the anode voltage, increasing too much the computation time of the simulation.
Figure 4. The turn-off current characteristic from which the turn-off times can be measured.

The initial value of the current to be switched off is 400 Amps. The turn-off time is similar in both cases: 6.4 $\mu$s for the GTO ($t_s = 2.3 \, \mu s + t_f = 4.1 \, \mu s$) and 6.7 $\mu$s for the p-GTO ($t_s = 2.3 \, \mu s + t_f = 4.4 \, \mu s$). Considering supplementary that in fact for the p-GTO a larger turn-off control voltage can be applied on the gate terminal, the conclusion is that the new p-GTO device exhibits superior switching characteristics compared with the classic GTO. Recent works [9,10] show that implementation of similar devices on Silicon Carbide (SiC) translates into lowering the turn-off times up to 10 times.

Also, in the simulation was computed the static operating point of the devices, i.e., the anode current $I_{AT} = 400A$ and the on-state voltage $V_T$. In both cases the obtained value was $V_T = 1.5$ volts.

7. Conclusions
The p-GTO (gate-turn-off) thyristor has a p-type low-doped base, in comparison with its classic counterpart, which has a n-type low-doped base. As shown in this work, design optimization techniques applied with SILVACO TCAD simulation tools lead to improved static and dynamic characteristics of the p-GTO thyristors. The main advantages are augmented breakdown voltages of the power device, improving the main anode-to-cathode maximum voltage and the cathode-to-gate breakdown voltage, leading to the possibility of faster turn-off switching.

8. References
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