RISC-NN: Use RISC, NOT CISC as Neural Network Hardware Infrastructure

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Abstract

Neural Networks (NN) have been proven to be powerful tools to analyze Big Data. However, traditional CPUs cannot achieve the desired performance and/or energy efficiency for NN applications. Therefore, numerous NN accelerators have been used or designed to meet these goals. These accelerators all fall into three categories: GPGPUs, ASIC NN Accelerators and CISC NN Accelerators. GPGPUs achieve general purpose and high computing throughput, but cannot provide desired energy efficiency because their stream architecture cannot achieve efficient data reuse required by NN applications. ASIC NN Accelerators achieve best performance or energy efficiency through advanced data reuse optimization, however, they only support limited NN use cases. CISC NN Accelerators aim to achieve both general purpose and high energy efficiency by decomposing NN applications into multiple relatively simple matrix or vector CISC instructions. Though CISC NN Accelerators can achieve considerable smaller memory footprint than GPGPU thus improve energy efficiency; they still fail to provide same level of data reuse optimization achieved by ASIC NN Accelerators because of the inherited poor programmability of their CISC architecture.

We argue that, for NN Accelerators, RISC is a better design choice than CISC, as is the case with general purpose processors. We propose RISC-NN, a novel many-core RISC-based NN accelerator that achieves high expressiveness and high parallelism and features strong programability and low control-hardware costs. We show that, RISC-NN can implement all the necessary instructions of state-of-the-art CISC NN Accelerators; in the meantime, RISC-NN manages to achieve advanced optimization such as multiple-level data reuse and support for Sparse NN applications which previously only existed in ASIC NN Accelerators. Experiment results show that, RISC-NN achieves on average 11.88× performance efficiency compared with state-of-the-art Nvidia TITAN Xp GPGPU for various NN applications. RISC-NN also achieves on average 1.29×, 8.37× and 21.71× performance efficiency over CISC-based TPU in CNN, MLP and LSTM applications, respectively. Finally, RISC-NN can achieve additional 26.05% performance improvement and 33.13% energy reduction after applying pruning for Sparse NN applications.

Key Words: RISC, Neural Networks Accelerators, CISC, Many-Core

1 Introduction

The world now has entered the Big Data Era with millions of terabytes of data generated each day. Such a huge amount of data, together with the computing power enabled by advanced processing technologies, has spurred a wave of powerful neural network (NN) applications that play major roles in visual recognition \cite{30}, voice recognition \cite{29}, autonomous vehicle \cite{11} and smart advertisement campaign \cite{7}. Unfortunately, traditional CPU/GPGPU platforms cannot achieve the desired performance and/or energy efficiency when running neural network applications \cite{14}. Therefore, it is a natural evolution to create specialized NN accelerators. As a matter of fact, NN applications are ideal for implementing in accelerators because most of the NN applications are composed of multiple relatively simple matrix or vector operations \cite{33,28} that can be efficiently implemented in hardware.

A straightforward solution in this respect is to design a CISC (Complex Instruction Set Computers) NN accelerator with specialized ISAs for vector and/or matrix operations. This is exactly the design solution of prior arts used
in two state-of-the-art NN accelerators, TPU [28] and Cambricon [33]. Both accelerators use a simple centralized control logic to decode the CISC instructions and then drive large arithmetic logic arrays. This design solution largely reduces the area and/or energy used by control logics—for example, the control logic of TPU takes about 2% of the total chip area. As a result, these accelerators can (1) achieve higher performance by implementing more arithmetic logics in the spare area and (2) achieve higher energy efficiency by decreasing the portion of energy used by control logics.

We argue, however, that, though well-motivated, these CISC NN accelerators inherit some shortcomings of CISC, specifically a lack of instruction-level parallelism, and poor programmability. The former causing shortcoming results from underutilization of execution units, which in turn lowers the performance and energy efficiency of CISC NN accelerators. The latter shortcoming results in performance penalties and energy inefficiency in CISC NN accelerators when executing important NN applications like CNN and Sparse NN. Since these shortcomings are intrinsic, they cannot be easily solved within the CISC architecture.

In this paper, we aim to overcome the aforementioned problems using RISC-NN, a novel many-core NN accelerator that combines the merits of RISC (Reduced Instruction Set Computers) and dataflow architecture. We show that, compared with CISC NN accelerators, RISC-NN has the following merits:

- **High Expressiveness.** As will be shown in Section 5.1, RISC-NN supports all the necessary CISC instructions of two state-of-the-art CISC NN accelerators [28][33]. Thus, it is at least as expressive as CISC NN accelerators.
- **High Parallelism.** As will be shown in Section 3, RISC-NN maximizes performance by exploiting parallelism at the task, ExeBlock and instruction levels.
- **Strong Programmability.** As will be shown in Sections 5.2&5.4 for applications such as CNN and Sparse NN, RISC-NN manages to implement state-of-the-art optimizations which previously were only available in ASIC NN Accelerators [16][50]. This fact proves that RISC-NN offers unprecedentedly strong programmability among all the NN accelerators.
- **Low Control Hardware Cost.** As will be shown in Section 5.3, we can minimize the control hardware cost by carefully choosing features such as Very-RISC ISA, SIMD and decoupling data movement and computation.

In summary, we believe that using RISC instead of CISC as the hardware infrastructure for NN applications is the right way to go.

The rest of the paper is organized as follows. Section 2 discusses the shortcomings of state-of-the-art NN accelerators and proposes design principles of RISC-NN. Section 3 presents the design of RISC-NN. Sections 4&5 present the experiment methodology and results. Section 6 discusses some additional topics. Section 7 concludes the paper.

2 Motivation

In this section, we first summarize state-of-the-art NN accelerators, and then presents the conclusion which motivates our proposed RISC-NN architecture.

2.1 Shortcomings of State-of-the-Art NN Accelerators

Many architectures have been proposed in order to accelerate NN applications. Yet, they all fall into three categories: GPGPUs, Special Purpose NN Accelerators and CISC General Purpose NN Accelerators.

2.1.1 GPGPUs.

GPGPUs [9] are the most widely used NN accelerators, due to their strong parallelism in processing of vector and matrix. Also, additional support has been provided to make GPGPUs more capable to accelerate NN applications—take Nvidia GPGPUs for example: on software side, cuDNN, a special deep NN library has been introduced; on hardware side, mixed precision calculation unit has been introduced to reduce the calculation overhead of NN applications. On the other hand, however, being a stream accelerator, GPGPU cannot provide fine-grained data sharing among its computing cores. As a result, data reuse can only happen in shared cache and global memory, and this introduces non-trivial excessive energy consumption.

Note that, very recently, Nvidia also has integrated Tensor Cores, which are specialized in tensor operations, in their Volta and Turing architecture. The notion and architecture of Tensor Cores is largely the same with TPU [28], which will be discussed in detail in Section 2.1.3.

2.1.2 ASIC NN Accelerators.

ASIC NN Accelerators [10][13][17][18][19][22][25][32][34][35][37][39][40][41][42][44][45][48] are special-purpose accelerators tailored for one or few NN applications, and they achieve high performance and/or energy efficiency by utilizing the intrinsic characterizations of the target NN applications. For example:

- **ASIC NN Accelerators for CNN applications** [16][32][34] maximize the data reuse of CNN. As a result, they decrease the off-chip/on-chip memory traffic and achieve high energy efficiency.
- **ASIC NN Accelerators for Sparse NN applications** [10][17][22][50] choose to take advantage of the ineffectual neurons in Sparse NN by not transferring or computing...
them. This also largely reduces energy consumption and boosts performance.

### 2.1.3 CISC NN Accelerators.

Designers also come up with more general NN Accelerators which support various NN applications and achieve better performance and/or higher energy efficiency than GPGPUs. Interestingly, the field of these general NN Accelerators is dominated by CISC architectures. Two state-of-the-art commercial ones (TPU \[^{28}\] and Cambricon \[^{33}\]) are both CISC. Such a design choice is motivated by the fact that most NN applications can be factorized into multiple simple matrix and/or vector operations. As a result, it is a straightforward task to implement these operations in CISC instructions. Since the instructions of CISC NN accelerators are relatively few and simple (compared to those in CISC general-purpose processors), their control hardware is in fact quite lightweight: in TPU, the control logic only takes up just 2% of the chip area. However, these CISC NN accelerators still inherit the other two drawbacks of CISC architecture:

- **Poor Instruction-Level Parallelism.** The designers of CISC NN accelerators have striven to improve their instruction-level parallelism. For example, both TPU and Cambricon enable instruction pipelining, and Cambricon even achieves out-of-order execution. However, to our best knowledge, all CISC NN accelerators fall short in another fundamental aspect: the ability to share execution units among multiple instructions. That is, for TPU and Cambricon, a single instruction occupies a whole execution unit (e.g., the Matrix Multiply Unit of TPU and the Vector/Matrix Func. Units of Cambricon). This incurs considerable underuse of execution units when executed instructions cannot fully use the execution unit. For example, more than half of the MACs of TPU are unused in CNN1 applications \[^{28}\]. Finally, such a drawback causes a nontrivial performance and energy efficiency overhead for CISC NN accelerators.

- **Poor Programmability.** It is hard, if not impossible, for CISC NN accelerators to achieve the same advanced optimization achieved in ASIC NN Accelerators. We take CNN and Sparse NN applications as examples:
  - **CNN.** CISC NN accelerators cannot fulfill all these data reuse techniques in ASIC NN accelerators because the reused data are usually across multiple CISC instructions, and it is hard to specify complex data reuse among different CISC instructions.
  - **Sparse NN.** In order to efficiently decompose NN applications into simple and regular CISC instructions, CISC NN Accelerators require these applications to be regular. This is not the case for Sparse NN. As a result, CISC NN Accelerators could only treat Sparse NN applications as regular dense ones and thus are incapable of benefitting from the computation and memory traffic benefits of Sparse NN.

### 2.1.4 RISC-Based NN Accelerators

Several researches \[^{20}\] \[^{21}\] study the possibility of using existing RISC cores to accelerate NN applications. The main focus of these researches is for embedded systems which has a tight power budget. The RISC cores used (e.g., PULP) are usually light-weighted and tightly-coupled (e.g., shared instruction and/or data cache \[^{21}\]). Such an approach works well in small scale system but also has scalability issues. On the other hand, many schemes of RISC-NN (e.g., Distributed Control, Dataflow and Data Stationary) are proposed to enhance the scalability of the accelerator. We believe these core RISC-NN ideas are the keys to scale up future RISC-based accelerators.

### 2.2 Our Proposal: RISC-NN

We can see that the drawbacks of CISC NN Accelerators mentioned in Section \[^{21}\] are fundamental and cannot be easily overcame within CISC architecture. Here we propose RISC-NN, a many-core RISC accelerator that overcomes these drawbacks without sacrificing performance and energy efficiency. Before we describe RISC-NN architecture in detail, we first introduce the techniques used in RISC-NN and the reasons of using them:

- **Distributed Control** (Section \[^{33}\]). Unlike CISC NN accelerators that use a centralized control scheme, RISC-NN uses a distributed control scheme in which each PE has its own control unit and can make most of the control decisions independently. With this capability, we can enable fine-grained control and data reuse, which are important to achieving desired programmability.

- **Very-RISC ISA** (Section \[^{32}\]). We acknowledge that having a independent control unit for every PE may considerably increase the control overhead for the chip area and energy efficiency. To counteract such control overhead, we use a very simple RISC ISA in every PE, one with only 11 instructions and two different addressing modes. Yet, this ISA is flexible enough to represent and optimize state-of-the-art NN applications.

- **Decoupling Execution and Data Transmission** (Section \[^{34}\]). In RISC-NN, the data transmission (e.g., memory load and storage) is completely decoupled from execution (i.e., calculation). That is, all the data needed are preloaded into the PE’s local memory prior to the execution; therefore, the execution will not be
suspended by memory accesses. Such a design boosts the utilization of execution components (i.e., MACs) and simplifies the control hardware.

- **SIMD** (Section 3.8). Most NN applications will be executed with identical instructions for multiple times. In order to take advantage of such an application feature, each PE uses a SIMD (single instruction multiple data) architecture to reduce the control energy overhead per operation and thus improve energy efficiency.

- **Multi-Level Parallelism.** To achieve high utilization of execution units, we exploit task-level, exeblock-level and instruction-level parallelism (Sections 3.1, 3.4 and 3.6 respectively) in RISC-NN.

- **Replacing Large RFs with SRAMs** (Sections 3.5). It is well-known that a large RF (register file) takes a considerable amount of power and energy [16]. Here we replace the large RF with a number of SRAMs and use hardware and software mechanisms to guarantee that this SRAM-based approach can achieve performance similar to that of the RF-based approach.

- **Dataflow** (Section 3.1). To reduce off-chip memory data transmission, we use an exeBlock-level dataflow technique to enable inter-PE data reuse across exeBlocks.

- **Data Stationary** (Section 3.11). To further reduce data movement, we allow multiple exeBlocks on the same PE to share the same piece of physical data. This technique is sometimes referred as data stationary [16].

## 3 RISC-NN Architecture

In this section, we introduce in detail the architecture of RISC-NN with an emphasis on how we improve the accelerator’s performance, efficiency and flexibility.

### 3.1 Overview

Figure 1 shows the overall architecture of RISC-NN. To reduce hardware complexity and achieve good scalability, RISC-NN adopts a simple tiled architecture that consists of many homogeneous PEs, several memory controllers with caches and In-DRAM Table Loader modules (see Section 3.9) in their front end. RISC-NN talks to the host in two ways: control messages, which uploads the control information to PEs through a simple Control Interface; and memory DMA, which transfers large amount of data (e.g., input data and instructions, output data) between host and DRAMs of RISC-NN. Three sets of NoCs connect the components: (1) the Memory NoC, a MESH network that transfers data and instructions between the off-chip DRAM and the PEs; (2) the Inter-PE NoC, a MESH network that transfers data among different PEs; and (3) the Control NoC, a tree-like network that connects the PEs with the Control Interface.

Before introducing the detailed PE architecture, we first introduce the execution model of RISC-NN. As is shown in Figure 2 multiple applications can run on RISC-NN at the same time. Each application consists of a sequence of consective tasks, and each task consists of multiple execution blocks (i.e., ExeBlocks) that are organized in a DataFlow manner. ExeBlocks are then mapped into the PE arrays, with each PE containing multiple ExeBlocks. The code for each ExeBlock consists of up to four consective Execution Stages, which we describe below:

- **LD (Load) Stage.** This stage loads data from the off-chip DRAM memory to the in-PE Operand RAM Module. Once the associated task is enabled, an ExeBlock can execute its LD Stage.

- **CAL (Calculation) Stage.** This stage does all the calculation. An ExeBlock can execute its CAL Stage only when the following two conditions are met: first, its LD Stage (if it exists) has already finished; second, it has received all the necessary data from its predecessor ExeBlocks (i.e., finishing actication step, see Section 3.4).

- **FLOW (Flow) Stage.** This stage transfers data from the current ExeBlock to its successor.

- **ST (Store) Stage.** This stage transfers data from the in-PE Operand RAM Module to the off-chip DRAM memory. As will be discussed in Section 3.9 in order to support complex activation/classifier functions, this stage can also do memory-side table lookup.

In the beginning of an application, the host first uploads the instructions and data onto the DRAM through DMA. It then sends control messages to initialize the corresponding ExeBlocks on the PEs. After that, as will be discussed in detail in section 3.4, the PEs will automatically finish rest of the application execution such as instruction loading, task
Table 1: Very-RISC ISA of RISC-NN. All instructions have the same format: [OP F0, F1, F2, CTRL], in which OP is 4-bit instruction type and F0—F2 are three 16-bit operand fields. And CTRL is a 12-bit control field which has a 8-bit Sparse PC Inc sub-field to support Sparse NN applications (see Section 3.4) and a 4-bit In-DRAM Lookup Type sub-field to support complex activation/classifier functions (see Section 3.9). Each ExecutionStage has its own sub-instruction set. OPM is the abbreviation of Operand Memory of the PE. DRAM refers to off-chip DRAM main memory. LD_Base and ST_Base refer to the Load Base Address and Store Base Address of corresponding tasks, respectively.

| OP   | Main Function         |
|------|-----------------------|
| LD   | OPM[F0]=DRAM[LD_Base+F1,F2] |
| ADD  | OPM[F2]=OPM[F0]+OPM[F1] |
| SUB  | OPM[F2]=OPM[F0]-OPM[F1] |
| MUL  | OPM[F2]=OPM[F0]*OPM[F1] |
| MAX  | OPM[F2]=MAX(OPM[F0],OPM[F1]) |
| MIN  | OPM[F2]=MIN(OPM[F0],OPM[F1]) |
| MADD | OPM[F2]=(OPM[F0]*OPM[F1])+OPM[F2] |
| PREREAD0 | OPM[PrdRead Data Reg] = OPM[F0] |
| PREREAD1 | OPM[PrdRead Data Reg] = OPM[F1] |
| FLOW Stage |
| COPY | PE[F2],OPM[F1]=OPM[F0] |
| ST   | DRAM[ST_Base+F1,F2]=OPM[F0] |

enabling, execution, etc., and store the final results in the DRAM for host to read back through DMA.

3.2 Very-RISC ISA

As discussed in Section 2.2, the ISA of RISC-NN should be expressive enough to represent and optimize state-of-the-art NN applications but also simple enough to incur minimal area and power/energy overhead. We have designed a Very-RISC ISA to achieve such a goal.

Table 1 summarizes RISC-NN ISA, which includes just 11 fixed-length instructions. All instructions have the same format: [OP F0, F1, F2, CTRL], in which OP is 4-bit instruction type field, F0—F2 are three 16-bit operand fields and CTRL is a 12-bit control field with a 8-bit Sparse PC Inc sub-field to support Sparse NN applications (see Section 3.4) and a 4-bit In-DRAM Lookup Type sub-field to support complex activation/classifier functions (see Section 3.9). Each instruction only belongs to one ExecutionStage. The ISA contains only two addressing modes:

- **Direct PE Addressing Mode.** For all the in-PE data, we use a simple direct addressing mode: one 16-bit field representing the data’s absolute address inside the Operand RAM Module of the PE. If the instruction has a remote PE address (i.e., COPY instruction), then another 16-bit field represents the remote PE number.
- **Base-Plus-Offset DRAM Addressing Mode.** To access data in the off-chip DRAM, we use a base-plus-offset addressing mode in which the DRAM address of a piece of data is the sum of the following two components: (1) a pre-stored 32-bit base address of the corresponding task and (2) a 32-bit offset address represented by two 16-bit fields of the instruction (i.e., F1&F2).

Here we describe in detail the individual instructions:

- **LD and ST Instructions.** These two instructions are in charge of transferring data between the DRAM and the PE’s local Operand Memory. They adopt the Direct PE Addressing and Base-Plus-Offset DRAM Addressing Modes. Note that LD and SD instructions use different pre-stored base addresses (i.e., LD_Base and ST_Base). As discussed in Section 3.11, we can use ST and LD instructions to conveniently share data between different tasks or applications. Section 3.9 also shows that, with non-zero In-DRAM Lookup Type bits in CTRL field, ST supports complex activation/classifier functions.

- **CAL Instructions.** There are eight CAL instructions. All of them use the Direct PE Addressing Mode since they can only visit the data in the PE’s local Operand Memory. Six out of eight instructions (i.e., ADD, SUB, MUL, MAX, MIN, MADD) are calculation-style instructions. The rest, the PREREADS, are used to avoid Operand RAM Module access conflicts (see Section 3.7).

- **FLOW Instruction.** The COPY instruction transfers data between the Operand RAM Modules of source and destination PEs. It enables data sharing among ExeBlocks of the PEs in a dataflow style.

3.3 Overall Architecture of PE

We carefully designed the PE architecture of RISC-NN based on its execution model. As shown in Figure 3, RISC-NN PE consists of the following modules:

- **Control Unit.** This is the central control logic of the PE. It receives and records the control information of the corresponding ExeBlocks and tasks and manages the operations of Execution Units and the Instruction
3.4 Management of ExeBlocks

The instructions on a PE are managed by the Control Unit at the granularity of ExeBlock. As shown in Figure 3, an ExeBlock Info Recorder in the Control Unit records all the necessary information of its ExeBlocks. An ExeBlock is then managed in a multi-step/stage manner. Figure 4 summarizes the order of steps and stages of an ExeBlock. Here we introduce in detail the steps and stages:

- **Initialization Step.** This step initializes a new ExeBlock. It specifies the following information of the ExeBlock:
  - Priority, which records its scheduling priority.
  - Task ID, which records the corresponding Task ID of the corresponding task.
  - #Predecessor, which records the number of predecessor ExeBlocks.
  - Stage Starting PCs, each of which records the starting PC of the corresponding ExeBlock Stage.
  - Stage Ending PCs, each of which records the ending PC of corresponding ExeBlock Stage. If the Starting and Ending PCs of an ExeBlock Stage are the same, it means the ExeBlock does not have this stage.
  - Inst DRAM Address, which records the starting DRAM address of ExeBlock instructions.
  - Successor ExeBlocks, which points to all the successor ExeBlocks of current ExeBlock. In our current implementation, each ExeBlock has up to 3 successors.
  - Sparse Execution, this bit indicates if this ExeBlock is used for a Sparse NN application or not.

- **Instruction Loading Step.** When Instruction Loader is not busy, it finds the ExeBlock with the highest priority among the ones whose instructions have not been loaded yet and then loads the instructions from the corresponding Inst DRAM Address into the corresponding location of the Instruction RAM Module. Note that, we store all the instructions of an ExeBlock consecutively in the Instruction RAM Module. As a result we can load them at once in a DMA manner.

- **Sparse PC Inc Update Step.** Only ExeBlocks with Sparse Execution have this step. At the beginning of each Sparse NN task, the Control Interface sends a sparse vector to each ExeBlock. For each ExeBlock, the bits of its sparse vector is the same with its instruction count, with each bit indicating if the instruction should be executed in the upcoming task. Instruction Loader takes the sparse vector and translates it into Sparse PC Inc of each individual instruction, which is the PC increment to the next valid instruction, and write such information to the Inst RAM Module.

- **Task-Enabling Step.** Control Interface enables the task by broadcasting a task-enabling message to all the PEs. An ExeBlock must have its corresponding task enabled to start its Execution Step.

- **Activation Step.** At the end of the FLOW Stage of an Execution Step, an ExeBlock sends activation requests to all its successor ExeBlocks, indicating that all the necessary data have been transferred. The Activation Step finishes only when the ExeBlock successfully collects activation requests from all its predecessors.

- **Execution Step.** This is the main step, which executes the instructions of the ExeBlock. As mentioned in Section 3.1, this step contains four consecutive stages: LD, CAL, FLOW and ST. Note the following:
  - An ExeBlock can start Execution Step only when Instruction Loading and Task-Enabling Steps have finished.
  - A stage of Execution Step can start only when all its previous stages were executed or do not exist.
  - In order to collect all the necessary data, the CAL stage of Execution Step can start only when the Activation Step has finished.

- **Reset Step.** After the Execution Step, the Control Unit resets the status of the ExeBlock before its termination. Such an operation is necessary for the reuse of an ExeBlock (see Section 3.11).

As shown in Figure 5 such a multi-step/stage management method overlaps the steps and stages of different ExeBlocks. This in turn helps maximize the utilization of the PE execution units, especially CAL Units. This is important because improving the utilization of CAL Units is the key to improving the performance and energy efficiency of the whole RISC-NN.

3.5 Instruction and Operand RAM Modules

This section discusses the hardware structures used to store instructions and operands (i.e., data) in RISC-NN.
These are the Operand and Instruction RAM Modules, respectively.

Instruction RAM Module. As shown in Figure 6 (c), the Instruction RAM Module consists of multiple (8 in our experiment) single-port SRAM banks. Each bank can only be occupied by a single Execution Unit at any time.

Operand RAM Module. One important reason for why general-purpose architectures (e.g., GPU and CPU) are not energy efficient enough is that they extensively use large, power-hungry RFs. To improve energy efficiency, we replace the RF with a low-cost Operand RAM Module, which can be conceptually viewed as a large multi-write-multi-read SRAM. The Operand RAM Module consists of multiple (16 in our experiment) 1-write-1-read SRAM banks, each of which can serve at most one write and one read at the same time. As shown in Figure 6 (a), three out of five read ports (Ports 0–2) are used by the CAL Unit. These three ports have the highest priority and must be served at the same time. The ports of ST and Flow Units have a lower priority. As a result, CAL Instructions can always be served without stalling (i.e., ack always be 1'b1), but ST and Flow Instructions may have to wait because of the bank conflicts. To avoid the conflict of CAL Unit read ports, we map input operands of a CAL instruction to be distributed in different banks during compilation. As we discuss in Section 3.7, if there are conflicts remain in a CAL Instruction, we use two pre-read instructions (i.e., PREREAD0/1) to resolve them.

3.6 Four-Stage CAL Unit Pipeline

When compared to a conventional five stage RISC pipeline, the pipeline of the CAL Unit has several differences:

- There is no need to have one separate Instruction Decode stage because the ISA is ultra simple and thus decoding takes a very short time.
- the Memory Access stage can also be omitted since there is no memory access in the CAL Unit.
- One extra Operand RAM Read (READ) stage is needed to get access to the data in Operand RAM Module.

Therefore, as shown in Figure 7, the CAL Unit uses a short four-stage (FETCH, READ, EXE and Writeback) pipeline.

As is mentioned in Section 3.4 all the instructions are stored consecutively in Instruction RAM Module. Therefore, for regular (non-sparse) NN applications, the pipeline just increases its current PC by 1 to fetch the next instruction. For sparse NN applications, the pipeline uses the value of Sparse PC Inc (see Sections 3.2 & 3.4) in control field of current instruction to get the next instruction.

3.7 Resolving Data Hazard and Operand Conflicts

Though we omit memory accesses and jump instructions, there are still two more situations in the CAL Unit needing special attention: (1) Operand RAM Conflict, in which two or more operands of an instruction come from the same Operand RAM bank so they cannot be read at the same time and (2) Read-After-Write Data Hazard, in which an instruction uses the result of the instruction right before it.

Resolving Operand RAM Conflict. As is shown in Table 1 and Figure 7 we have two pre-read instructions (i.e., PREREAD0/1) which read the data from Operand RAM into OP0/1-PreRead Data Reg and store the corresponding Operand RAM addresses in OP0/1-PreRead Addr Reg. If the compiler detects Operand RAM Conflict in one instruction, it injects pre-read instruction(s) up front. At READ stage, if CAL Unit detects that the address of an OP (i.e., OP0) is the same with its pre-read address register (i.e.,
Each cache slice has 4 ways and 64-byte block size, and is connected to an edge memory NoC router. 1.887GHz, which results in a peak performance of 1.932TOPS (1 DDR4 2400MHz Controller with 1MB write-back policy front-end cache, which is distributed into 8 slices. SIMD-8, 16-bit MAC Unit; 8-bank Instruction RAM Module, with each bank using a single 64bit*512 single port RAM; 85-bit width Control NoC Router; 128-bit data width Memory & Inter-PE NoC Routers.

Table 2: RISC-NN Simulation Parameters

| #PEs  | Memory Subsystem         | PE | Host Access | Frequency |
|-------|--------------------------|----|-------------|-----------|
| 64    | 1 DDR4 2400MHz Controller with 1MB write-back policy front-end cache, which is distributed into 8 slices. Each cache slice has 4 ways and 64-byte block size, and is connected to an edge memory NoC router. | SIMD-8, 16-bit MAC Unit; 8-bank Instruction RAM Module, with each bank using a single 64bit*512 single port RAM; 16-bit Operand RAM Module, with each bank using a single 128bit*128 1W1R RAM; 85-bit width Control NoC Router; 128-bit data width Memory & Inter-PE NoC Routers. | PCIe3.1 [4]; 5mW/Gb/lane | 1.887GHz, which results in a peak performance of 1.932TOPS (1.887G × 64 × 8 × 2, a MAC unit delivers 20Ps per cycle) |

Figure 8: ExeBlock Reuse and Sharing. OP0-PreRead Addr Reg), it will bypass reading Operand RAM and use pre-read data (i.e., from OP0-PreRead Data Reg) instead. Note that, data in pre-read address & data registers are one-time only—once used, they will be invalidated.

Resolving Read-After-Write Data Hazard. As is shown in Figure [7] at EXE stage, CAL Unit compares the address of each operand (i.e., OP0/1/2 Addr Reg) with the address of result in previous cycle (i.e., Result Addr Reg). If any of them match, CAL Unit then uses the result of previous cycle, which is stored in Result Data Reg.

3.8 SIMD

Most NN applications are static and need to be executed multiple times (this feature is sometimes referred as a Single-Graph Multiple Flow [49]). Therefore they are a perfect match for SIMD [6] execution. As a result, our RISC-NN also adopts SIMD (SIMD-8 in our experiment) to improve performance and reduce control overhead.

3.9 Supporting Complex Activation & Classifier Functions

For design complexity and hard-ware cost considerations, we choose to keep the ISA of RISC-NN simple, which does not support complex activation/classifier functions. Instead, we rely on table lookup [14] to implement these complex functions. We also have the following two observations:

- For 16-bit accuracy (i.e., accuracy of RISC-NN), we need a table of $2^{16}$ entries to achieve full accuracy lookup. This corresponds to 128KB of memory space, which might be too large for on-chip SRAM but is trivial for off-chip memory.
- These functions are usually used at the very end of the layer computation and comprise a very small fraction of the overall computation.

Based on the above observations, we choose to store the lookup tables of complex functions in the DRAM with each table taking only 128KB of DRAM space. As is discussed in Section 3.2, each ST instruction has 4-bit In-DRAM Lookup Type in its CTRL field. Non-zero value of this type means there is a complex function lookup associated with the stored value. In that case, the memory controller first uses In-DRAM Table Loader (See Figure [1]) to look up the function value in corresponding In-DRAM table and then store this value into DRAM/cache instead.

3.10 Cache Architecture

Although RISC-NN strives to reduce memory access by utilizing intra-PE and inter-PE data reuse, sometimes there are still considerable amount of memory accesses to large shared global data structures (such as feature map in CNN). To enhance the performance and energy efficiency of these memory accesses, we introduce a cache module as the front-end of memory controller. This is a write-back cache which accommodates all the LD and ST requests, but bypasses all the instruction loading requests.

3.11 Data Reuse and Sharing

As shown in Figure [8] RISC-NN supports various data reuse and sharing mechanisms that are important to improving its performance and energy efficiency. We describe these mechanisms below:

- ExeBlock Reuse. Tasks A1 and A2 share the same ExeBlocks. As a result, the instructions of the ExeBlocks only need to be loaded once at the beginning of Task A1.
- Inter-ExeBlock Data Reuse. ExeBlock-0 and ExeBlock-2 of Task A1 can get access to the

![Diagram](image-url)
same operand in index \(0x07\) of PE0’s Operand RAM Module.

- **Inter-Task Data Reuse.** Both ExeBlock-2 of Task A1 and ExeBlock-0 of Task A2 can get access to the operand in index \(0x11\) of PE0’s Operand RAM Module.

- **Inter-PE Data Sharing.** During FLOW Stage, ExeBlock-0 copies the operand in index \(0x11\) of PE0’s Operand RAM Module to index \(0x15\) of PE1’s Operand RAM Module. Since ExeBlock-0 is a predecessor of ExeBlock-3, it has to send a network message to activate ExeBlock-3 at the end of its FLOW Stage.

- **In-Memory/Cache Data Sharing.** Though it is best to share data through Inter-ExeBlock Data Reuse and Inter-Task Data Reuse, sometimes the amount of data that needs to be shared exceeds the capacity of the Operand RAM Module. In this case, we need to share data through the main memory/cache. As shown in the figure, by assigning a different LD Base Addr and ST Base Addr, Tasks A1 and A2 manage to share data by storing to and loading from the same memory address \(0x20008000\).

### 3.12 Programming Model

Figure 9 shows the programming model for RISC-NN:

- **User Inputs**, which includes:
  - **Definition of ExeBlock Classes.** As will be discussed in Section 5.2, a typical RISC-NN task comprises of multiple ExeBlocks with only few identical styles. A programmer needs to first provide the definition of the different ExeBlocks styles (a.k.a., ExeBlock Classes) which, just like ExeBlocks, are composed of RISC-NN instructions. Yet, their operation fields are address parameters instead of hardware physical addresses.
  - **Execution Graph.** It consists of the instances of ExeBlocks Classes and the graph defining the relationship of the ExeBlock Instances. In ExeBlock Instances, the address parameters are replaced by logical (hardware irrelevant) addresses. The programmer also needs to assign a logical PE id to each ExeBlock Instance.

Note that, the data sharing is defined in Execution Graph. For example, if the instructions of two ExeBlock Instances will access the same operand data (e.g., \(0x07\) in ExeBlocks-0&1 of Figure 8), the programmer needs to first assign the same logical PE id to both ExeBlock Instances to make sure the compiler will map them to the same physical PE. Then for the data-sharing instructions, the logical addresses of corresponding operands should be the same.

- **Translator Responsibility.** We use a simple C++-based translator to handle the user inputs and maps them to the RISC-NN hardware. Its responsibility includes:
  - Mapping ExeBlocks to physical PEs. The compiler optimizes the load-balancing among PE by considering the available resources of different PEs (i.e., current ExeBlock count, available entries in Instruction/Operand RAM Modules, etc.).
  - Mapping logical in-PE addresses to physical entries in Operand RAM Module. Here the compiler also balances the occupancy among the banks of each Operand RAM Module to reduce the chance of Operand RAM conflict (Section 5.7).
  - Mapping logical DRAM addresses to physical DRAM addresses.

### 4 Experiment Methodology

Table 3 summarizes the parameters of a default RISC-NN system. To evaluate the effectiveness of RISC-NN, we use an in-house cycle-accurate simulator with Ramulator [29] as its memory subsystem. We also implement the design in Verilog and synthesize it using Synopsys Design Compiler with TSMC 12nm GP standard VT library. We then do
Table 4: Supported and unnecessary CISC NN accelerator instructions in the PE array of RISC-NN.

| TPU [28] | Cambricon [33] |
|-----------|----------------|
| Implementable | Read_Host_Memory, VLOAD, VSTORE, MLOAD, MSTORE, MMV, VMM, MMC, OP, MAM, MSM, MMC, OP, VGT, VE, VAND, VOR, VNOT, SC, SL |
| Unnecessary | Activate (complex), Read_Weights, Matrix Multiply, Convolve, Activate (simple), Jump, cond. branch, VEXP, VDV, VLOG, RV |

Table 5: Implementation Details of Instructions from CISC NN Accelerators on RISC-NN

| Size | LD Insts | CAL Insts | COPY Insts | ST Insts | Exec-Blocks | OP RAM Entries |
|------|----------|-----------|------------|----------|-------------|----------------|
| MMM  | 64x64    | 192       | 4906       | 4928     | 4096        | 255            |
| MMR  | 64x64    | 4160      | 4096       | 525      | 64          | 255            |
| MMS  | 64x64    | 4160      | 4096       | 0        | 64          | 8256           |
| MAM  | 64x64    | 8192      | 4096       | 0        | 64          | 8256           |
| OP   | 64x64    | 128       | 4096       | 896      | 4096        | 127            |
| VGMT  | 1024     | 2048      | 1024       | 0        | 1024        | 64             |
| VMV  | 1024     | 2048      | 1024       | 0        | 1024        | 64             |

Table 6: Static Program Analysis of Different CNN Implementations of AlexNet_CONV2 on RISC-NN

| Layers          | LD Insts | CAL Insts | COPY Insts | ST Insts | Exec-Blocks | OP RAM Entries | Max Insts |
|-----------------|----------|-----------|------------|----------|-------------|----------------|-----------|
| No Reuse        | 1056     | 6400      | 0          | 256      | 64          | 13056          | 8         |
| Conv Reuse      | 2976     | 6400      | 15200      | 256      | 256         | 13056          | 8         |
| Filter Reuse    | 6681     | 6400      | 1575       | 256      | 120         | 8256           | 8         |
| Hmap Reuse      | 6681     | 6400      | 1575       | 256      | 120         | 8256           | 8         |
| All Reuse       | 1136     | 6400      | 8400       | 256      | 254         | 8256           | 8         |

Table 7: Best Performance’s Instances number of Different CNN Implementations on RISC-NN

| Layers          | No Reuse | Conv Reuse | Filter Reuse | Hmap Reuse | All Reuse |
|-----------------|----------|------------|--------------|------------|-----------|
| CoogLeNet_CONV1 | 3        | 4          | 2            | 6          | 6         |
| CoogLeNet_CONV-5a | 4       | 4          | 7            | 8          | 8         |
| VGGM_CONV4     | 1        | 2          | 1            | 3          | 8         |
| VGGM_CONV9     | 3        | 7          | 3            | 8          | 8         |
| VGGM_CONV11    | 1        | 8          | 1            | 8          | 8         |
| AlexNet_CONV2  | 3        | 6          | 4            | 8          | 8         |
| AlexNet_CONV3  | 4        | 6          | 5            | 8          | 8         |
| ResNet_CONV2_2 | 1        | 3          | 2            | 6          | 8         |
| Average        | 2.5      | 5          | 3.75         | 6.88       | 7.75      |

5 Experiment Results

5.1 Implementing ISAs of CISC NN Accelerators in RISC-NN

Table 4 summarizes the implementability of all the CISC instructions of TPU [28] and Cambricon [33] on RISC-NN. We can see the following:

- **RISC-NN** can implement most of these instructions.
- **RISC-NN** can achieve the same behavior of two control instructions (i.e., jump and conditional branch) through inter-task management (either through host or control interface). Therefore these two instructions are not necessary for **RISC-NN**.
- Five CISC instructions (complex activate, VEXP, VDV, VLOG and RV), which are mainly used for complex activation functions and classifiers, are unimplementable with **RISC-NN** ISAs. Instead, as is discussed in Section 3.9, **RISC-NN** uses an alternate solution which implements these functions as In-DRAM lookup tables.

Table 5 shows the implementation details of several Cambricon [33] CISC instructions on RISC-NN. We can see that, all these implementations have quite a high ratio of memory instructions (LD and ST) to CAL instructions. As we will show in Section 5.2, this phenomenon indicates that these instructions have poor data reuse within the PE array and thus are not well optimized.

We acknowledge **RISC-NN** has a higher code size overhead than **CISC** accelerators [28, 33, 36, 38]. However, as will be shown in the rest of the section, the benefits of **RISC** clearly outweigh its code size overhead. Additionally, such overhead can be largely offset by two countermeasures: (1) When **RISC-NN** executes the same application for multiple times (common case for cloud-based **NN** accelerators [28]), the instructions need to be loaded only once and reused.

As is shown in Table 3, we measure the performance of **RISC-NN** using layers/operators of multiple **NN** inference applications, including classical **CNN** models (GoogLeNet [46], AlexNet [31] and VGG16 [43]) and other **NN** models (ResNet50 [24], Transformer [47], a sentiment analysis model based **CNN** [27] and seq2seq [12] from MLPerf [1]). Table 3 shows the detail of these **NN** benchmarks. Table 5 also shows the compress rates of AlexNet and VGG16 layers [23], as we will use these layers as examples to show effectiveness of **RISC-NN** for Sparse **NN** applications.

We compare energy consumption of **RISC-NN** with state-of-the-art NVIDIA Titan Xp GPGPU [5]. To get accurate energy consumption of each **NN** layer/operator, we use Caffe2 time [8] or Tensorflow timeline [5] to get execution time, and measure power consumption using Nvidia-smi [2]. Finally, GPGPU energy consumption is product of the measured execution time and power consumption.

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5.2 Optimizing CNN in RISC-NN

To show the flexibility and programmability of RISC-NN, we analyze in detail of some typical CNN 2D convolution layers (see Table 3). As is shown in Figure 10 following the category mechanism proposed by Chen et al., we evaluate five CNN implementations with different data reuse mechanisms on RISC-NN. No Reuse is the baseline scheme that has no data reuse, while Filter Reuse and Ifmap Reuse reuse the whole filters and input feature map chunks (both at the granularity of 2D filter size), respectively. These three implementations have only one task (i.e., Task-Main), which loops itself multiple times. Meanwhile, Conv Reuse introduces more complex partial inter-PE data sharing of the filters and input feature maps to further reduce off-chip memory traffic. To fulfill such data sharing, Conv Reuse needs the assistance of a single-run preprocess task (i.e., Task-Prepare). All Reuse combines all the aforementioned reuse techniques together. Note that, Conv Reuse and All Reuse, which were implemented in a recent ASIC CNN accelerator, cannot be achieved in CISC-NN accelerators. This fact indicates that RISC-NN achieves higher programmability than CISC-NN accelerators.
5.2.1 Static Analysis of CNN Implementations.

Table 6 shows the static program statistics of all the CNN implementations of AlexNet_CONV2:

- All implementations have the same number of CAL instructions.
- No Reuse has the highest number of LD instructions because of its lack of data reuse. Conv Reuse, Filter Reuse and Ifmap Reuse all substantially reduce the number of LD instructions. All Reuse, as the combination of all the reuse schemes, achieves the fewest LD instructions and thus the lightest memory read traffic.
- The implementations with reuse mechanisms all use COPY instructions to reuse on-chip data among the ExeBlocks (either intra-PE or inter-PE).
- Filter Reuse, Ifmap Reuse and All Reuse also reduce the number of Operand RAM entries used by each task. As is shown in Table 6, RISC-NN has enough Instruction and Operand RAM Module capacity to incorporate multiple instances of all the CNN implementation (8 in all five CNN implementations of AlexNet_CONV2). Running multiple instances can increase ExeBlock-level parallelism and thus improve the performance. We evaluate the performance impact of running multiple instances in Section 5.2.2.

5.2.2 Performance of CNN Implementations.

Figure 11 shows the performance of RISC-NN in terms of MAC utilization under different CNN implementations with single instance—All Reuse achieves an average MAC unit utilization of 22.91%, remarkably surpassing the results of others (2.12%, 5.21%, 2.30% and 7.96% respectively for No Reuse, Conv Reuse, Filter Reuse and Ifmap Reuse).

Due to conflicts of shared resources, such as NOCs and offchip-Memory, having more instances does not necessarily lead to higher performance. Table 6 shows the instances number of the best MAC unit utilization for five different CNN implementations. The performance of All Reuse keeps increasing as its number of instances increases to about 8; however, this is not the case for other implementations—No Reuse, Conv Reuse, Filter Reuse and Ifmap Reuse achieve their peak performance with an instance number of on average 2.5, 5, 3.75 and 6.88, respectively, and adopting more instances beyond these sweet spots hurts the performance. As is shown in Figure 12 for the multi-instance situation, the best MAC unit utilization of All Reuse (on average 74.43%) is at least more than 2 times higher than the other implementations.

5.2.3 Memory and NoC Traffic of CNN Implementations.

Figures 13 and 14 present the memory and NoC traffic of different CNN implementations with single instance. We can see that, as expected, All Reuse has the least memory traffic—only on average $\frac{1}{35}$, $\frac{1}{13}$, $\frac{1}{3}$ and $\frac{1}{6}$ of No Reuse, Conv Reuse, Filter Reuse and Ifmap Reuse, respectively. Note that, Filter Reuse has considerably more memory ac-
cesses than Ifmap Reuse because the filters of a CNN application usually have a smaller memory footprint than its input feature maps. This is also the reason why DaDian-Nao [15] and TPU [23] use large on-chip memories to make input feature maps stay on-chip. Cow Reuse has less memory traffic than Filter Reuse because it also partially reduces the access to off-chip feature maps.

On the NoC traffic side, Memory NoC traffic is proportional to the Off-Chip Memory traffic shown in Figure 13 and the Control NoC traffic takes a quite small portion of all NoC traffic (less than 8% for all implementations). While No Reuse has no Inter-PE NoC traffic since it has no inter-PE data sharing, all the other implementations have a significant amount of Inter-PE traffic to realize their unique inter-PE data-sharing pattern using COPY instructions. An interesting phenomenon is that there is a mismatch of off-chip memory traffic and memory NoC traffic in Ifmap Reuse—compared to All Reuse, Ifmap Reuse has nearly on average 9.39× more Memory NoC traffic but only on average 5.82× more off-chip memory traffic. This happens because the memory request of Ifmap Reuse, the majority of which is input feature map information, achieves a high hit rate (at least 91.92%) in the front-end cache of the memory controller.

5.2.4 Energy Efficiency of CNN Implementations.

Figure 15 shows the normalized energy consumption of all the CNN implementations. We can see that, consistent with NoC and off-chip memory traffic statistics, No Reuse consumes the highest energy while All Reuse consumes the lowest energy.

5.3 Performance Efficiency Over State-of-the-Art GPGPU and CISC NN Accelerator

We compare performance efficiency (in terms of TOPS/W) of RISC-NN with state-of-the-art Nvidia Titan Xp GPGPU and TPU [28].

RISC-NN VS. GPGPU. Since Titan uses 32-bit accuracy instead of 16-bit (the accuracy of RISC-NN implementation), to ensure fair comparison, we also provide extrapolated performance efficiency results of the GPGPU with 16-bit accuracy. As a stream processor, the major part of GPGPU energy is consumed during data movement and such energy is proportional to the number of data moved, therefore we extrapolate that 16-bit accuracy GPGPU has roughly half the energy consumption of its 32-bit counterpart. We can see that, RISC-NN achieves on average 11.88× and 5.94× higher energy performance efficiency over Nvidia Titan Xp with 32-bit and 16-bit accuracy, respectively.

RISC-NN VS. TPU. There were limited performance/power details provided in CISC-NN processors (i.e., Cambricon and TPU). As the best efforts, we compare the average reported MAC unit utilization and performance efficiency of different types of NN applications (i.e., CNN and MLP) in RISC-NN and TPU [23]. As is shown in Figure 17(a), RISC-NN manages to achieve 72.62%, 69.44% and 26.66% MAC unit utilization for CNN, MLP and LSTM; while TPU achieves respectively 54.40% (with high variability), 11.96% and only 3.53% for CNN, MLP and LSTM. This indicates that, compared with CISC NN accelerators, RISC-NN manages to better utilize its hardware resources. As a result of better hardware utilization, RISC-NN also achieves better performance efficiency than TPU with the same 16-bit accuracy—as is shown in Figure 17(b), RISC-NN achieves on average 1.29×, 8.37× and 21.71× performance efficiency over TPU for CNN, MLP and LSTM, respectively.

5.4 Sparse NN Optimization

Here we use five Sparse CNN layers [23] as an example to show how RISC-NN takes advantage of the sparsity. As is shown in Figure 18, the compiler first identifies ineffective weights of filters and generates corresponding sparse vector to record the unnecessary instructions in next task. Then, as is discussed in Section 3.4 Instruction Loader takes the sparse vector and translates it into Sparse PC Inc in Instruction RAM. Finally, CAL Unit skips unnecessary instructions according to information of Sparse PC Inc in each instruction.

As is shown in Figure 19 this approach boosts the performance by on average 20.06%, as a result of skipping unnecessary instructions. It also reduces energy consumption by on average 33.13% because of reduction in calculation and accesses to Instruction and Operand RAMs.

5.5 Area Overhead of RISC-NN

The total area of RISC-NN is 14.42mm², and a single RISC-NN PE takes 0.15mm². Figure 20 and 21 show the area breakdowns of the whole RISC-NN and a single PE, respectively. We can see that, PE array consumes the majority (67%) of the whole chip area while cache takes only 16%; in the meantime, the area of a single PE is dominated by Operand RAM Module. Such an architecture with small shared cache and large in-PE memory is in line with our design principle of maximizing the data sharing within PEs and reducing transmission overhead of accessing remote data (see Section 5.11).

5.6 Impact of SIMD on Energy Efficiency

Using a high SIMD count in RISC-NN not only reduces the area overhead of the control hardware, but also increase energy efficiency. Figure 22 shows the normalized energy
efficiency (in terms of nJ/op) of the All Reuse implementation of AlexNet_CONV2 under different SIMD counts. We can conclude that, the energy overhead of the control hardware diminishes as the SIMD count increases. With SIMD-64, the control energy only takes 0.8% of the total energy consumption. Overall, we can achieve a reasonable control energy overall with SIMD-8.

5.7 Energy Efficiency Scalability

As the number of PE increases in RISC-NN, the energy efficiency of its components should stay largely the same, except for the NOC which on average requires more hops to finish a single request. Without loss of generality, we assume the number of hops and energy consumption per NOC request increase as the square root of PE counts. We then project the energy efficiency of RISC-NN at different scales. As is shown in Figure 23 when running All Reuse applications, the energy efficiency of RISC-NN scales well—even with the extreme scale of 4096 PEs, it energy efficiency is still just 23.1% higher than that of the default 64-PE version, thanks to the optimizations of All Reuse which keeps the data movement minimal.

6 Discussion

6.1 Use Scenarios for RISC-NN

Currently RISC-NN can be used either as a library-based NN accelerator or as an energy-efficient alternative to FPGA-based NN accelerator, but our ultimate goal is to make it an automatic end platform for high-level NN frameworks:

- **As a Library-Based NN Accelerator.** As is discussed in Section 3.12 the current version of RISC-NN uses a semi-automatic programming model which still needs some effort from programmers to generate performance and energy efficient implementations. Though not ideal, this is an acceptable overhead given the fact that only a few NN applications will be used by a certain customer and applications themselves are not changed frequently. As a result, RISC-NN service providers can develop libraries of typical NN applications for end users to use. Such library-based use scenarios are widely adopted in NN accelerators [20,21,23] and proven to be successful.

- **As an Energy Efficient Alternative to FPGA-based NN Accelerators.** In previous sections, we prove that RISC-NN has achieved high flexibility in NN optimization implementation, similar to FPGA-based approaches. Meanwhile, RISC-NN can achieve significantly better energy efficiency, making it an energy efficient alternative to FPGA-based approaches.

- **As an Automatic End Platform for High-Level NN Framework.** Our future work is to develop a compiler to automatically translate the codes of high-level NN frameworks (e.g., PyTorch and Tensorflow) into optimized instructions for RISC-NN. Given the static nature of NN applications and the rich prior research of RISC compiler optimizations, we believe such a goal is achievable.

6.2 Hardware Design Space Exploration

Though RISC-NN is mainly designed to support cloud-based NN acceleration which has a strict performance and energy efficiency requirement, we believe it can also fit into other markets with some design adaptions.

Without loss of generality, we discuss how to adapt RISC-NN to fit the requirements of IoT (Internet-of-Things) NN applications, which have a strict power/area budget to meet the target performance. Table 8 shows the details of such an adaption (i.e., IoT RISC-NN). Compared with RISC-NN, IoT RISC-NN manages to achieve similar energy efficiency but reduce 78.6% of the PE area by slashing the number of RAM banks, router buffer depth and concurrency. This comes at a cost of reduction in available performance—IoT RISC-NN only achieves 7% of MAC Unit Utilization with AlexNet_CONV2 compared with 81% in RISC-NN. Yet, IoT RISC-NN still achieves a performance of 135.2GOPS which is well above the performance requirements of typical IoT NN applications.
7 Conclusions

We believe RISC is a better design choice for NN accelerators over CISC. To prove our concept, we propose a many-core RISC NN accelerator (i.e., RISC-NN) with a 11-instruction Very-RISC ISA and other carefully selected design solutions such as distributed control, dataflow and SIMD.

We show that RISC-NN can realize all the necessary instructions of state-of-the-art CISC NN Accelerators [28,33]. As proof of its superior programmability, our experiments show that RISC-NN can realize the advanced CNN optimizations and optimization for Sparse NN, both of which previously were only available in ASIC NN Accelerators [16,50]. For a variety of NN applications, RISC-NN achieves on average 11.88× performance efficiency over state-of-the-art Nvidia Titan Xp GPGPU. It also achieves on average 1.29×, 8.37× and 21.71× performance efficiency over CISC-based TPU in CNN, MLP and LSTM applications. Finally, by applying pruning optimization, RISC-NN achieves additional on average 26.06% performance improvement and 33.13% energy reduction for Sparse NN applications.

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