Virtualizing Deep Neural Networks
for Memory-Efficient Neural Network Design

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Abstract
The most widely used machine learning frameworks require users to carefully tune their memory usage so that the deep neural network (DNN) fits into the DRAM capacity of a GPU. This restriction hampers a researcher’s flexibility to study different machine learning algorithms, forcing them to either use a less desirable network architecture or parallelize the processing across multiple GPUs. We propose a runtime memory manager that virtualizes the memory usage of DNNs such that both GPU and CPU memory can simultaneously be utilized for training larger DNNs. Our virtualized DNN (vDNN) reduces the average memory usage of AlexNet by 61% and OverFeat by 83%, a significant reduction in memory requirements of DNNs. Similar experiments on VGG-16, one of the deepest and memory hungry DNNs to date, demonstrate the memory-efficiency of our proposal. vDNN enables VGG-16 with batch size 256 (requiring 28 GB of memory) to be trained on a single NVIDIA K40 GPU card containing 12 GB of memory, with 22% performance loss compared to a hypothetical GPU with enough memory to hold the entire DNN.

1. Introduction
Deep neural networks (DNNs) have been successfully deployed in various application domains such as computer vision (Krizhevsky et al., 2012), speech recognition (Graves & Schmidhuber, 2005), and natural language processing (Collobert et al., 2011) thanks to their superior performance compared to traditional state-of-the-art approaches. Such proliferation of deep learning techniques has led several software frameworks to be developed in recent years to analyze and facilitate the design of neural networks (Tensorflow, 2016; Torch, 2016; Theano, 2016; Caffe, 2016). The list of available frameworks continue to expand with developers constantly adding more features and improving computational efficiency to foster research in the area of deep learning. Due to the tremendous compute horsepower offered by graphics processing units (GPUs), these frameworks provide strong backend support for GPU software libraries such as cuDNN (NVIDIA, 2016b) and Neon (Nervana, 2016). In fact, almost every group today involved in training neural networks is deploying GPUs for accelerated deep learning (Bahrampour et al., 2016).

While these popular machine learning (ML) frameworks facilitate the study of DNNs, a major limitation of the use of these frameworks is that the DRAM capacity limits of the GPU(s) in the system eventually limit the size of the neural network that can be trained. To work around the memory capacity bottleneck, ML practitioners must either use less desirable DNN architectures (e.g., smaller number of layers, smaller batch sizes, less performant but more memory-efficient convolutional algorithms) or parallelize the DNN across multiple GPUs (Krizhevsky, 2014). Figure 1 highlights how the memory consumption trends of the ImageNet (ImageNet, 2016) winning DNNs have evolved over time. AlexNet (Krizhevsky et al., 2012), for instance, only contained 5 convolutional layers with 2 fully-connected layers and required “mere” 1.1 GB of memory allocation for training, which is well below the 12 GB memory capacity of the state-of-the-art NVIDIA K40. The more recent VGG-16 (Simonyan & Zisserman, 2015), on the other hand, contains 16 convolutional layers and 3 fully-connected layers, incurring a total of 28 GB of memory usage for batch size 256. Because a single GPU can only accommodate a batch size of 64 for VGG-16, training with batch 256 requires parallelization across multiple GPUs or the network must be sequentially executed.
multiple times with the smaller batch 64. With the most recent ImageNet winning network adopting more than a hundred convolutional layers (He et al., 2015), the trend in deep learning research is to move towards larger and deeper neural network designs (Wired, 2016; Szegedy et al., 2014; Simonyan & Zisserman, 2015). As a result, alleviating the rigid physical memory limitations of GPUs is becoming increasingly important.

In this paper, we propose virtualized Deep Neural Network (vDNN), a runtime memory management solution that virtualizes the memory usage of deep neural networks across both GPU and CPU memories. Our vDNN allows ML practitioners to deploy larger and deeper networks beyond the physical capacity of available GPUs, enabling them to focus more on their algorithms while the system architecture and runtime system transparently manage the allocation, placement, movement, and release of their data. The motivation behind vDNN is based on the following three key observations: 1) DNNs trained via stochastic gradient-descent (SGD) are designed and structured with multiple layers (LeCun et al., 1998); 2) the training of these neural networks involves a series of layer-wise computations, the order of which is statically fixed and repeated for millions to billions of iterations throughout the entire training process; and 3) even though the GPU can, at any given time, only process a single layer’s computation (due to the layer-wise computational characteristics of SGD-based DNN training), popular ML frameworks adopt a network-wide memory allocation policy. In other words, existing memory management schemes overprovision the memory allocations to accommodate the usage of the entire network layers, even though the GPU is only using a subset of this allocation for the layer-wise requirements. We observe that such memory underutilization issue becomes more severe for deeper networks, leading to 58% to 69% of allocated memory being unused at all at any given time (Figure 1). The goal of vDNN is to conservatively allocate GPU memory for the immediate usage of a given layer’s computation so that the maximum and average memory usage is drastically reduced, allowing researchers to train larger networks. To achieve this goal, vDNN exploits the data dependencies of allocated data structures, particularly the intermediate feature maps that account for the majority of memory usage (Section 2.3), and either releases or moves these intermediate data between GPU and CPU memory. Specifically, vDNN either 1) aggressively releases these feature maps from the GPU memory if no further reuse exists, or 2) offloads (and later prefetches) to (from) CPU memory if further reuse does exist but is not immediately required. By exploiting the inter-layer memory access and reuse patterns of DNNs, our vDNN memory manager intelligently overlaps the normal DNN computations with the offload/prefetch/release operations, effectively virtualizing the memory usage of DNNs with little to no performance loss. The operations of vDNN are completely transparent to programmers and enable them to train larger and deeper neural networks that consume memory well beyond the limits of physical memory of GPUs today. The key contributions of our work are summarized below:

- We qualitatively and quantitatively analyze the memory access characteristics of DNNs and their effect on the GPU memory system. To the best of our knowledge, our work is the first that provides an in-depth characterization study on the memory access characteristics of DNNs from an architectural perspective.

- We identify the key limitations of current ML frameworks’ memory management policies as they require the network-wide memory usage of the target DNN application to monolithically fit within the physical capacity of the GPU. We quantitatively analyze the memory inefficiencies of these frameworks.

- We propose, implement, and evaluate a novel runtime memory manager called vDNN that virtualizes the memory usage of neural networks across CPU and GPU memories with little to no loss in performance.

2. Background and Motivation

This section provides an overview of modern DNNs, the memory management policies of current ML frameworks, and their key limitations that motivate this work.

2.1. DNN Architecture

Convolutional neural networks are one of the most popular ML algorithms for high accuracy computer vision tasks. While other types of network architectures are
also gaining tractions (e.g., recurrent neural networks for natural language processing), all of these DNN architectures are trained using a backward propagation algorithm (LeCun et al., 1998) via stochastic gradient-descent (SGD). For clarity of exposition and owing to their popularity, the rest of this paper assumes the linear, feedforward style convolutional neural networks commonly seen in AlexNet, OverFeat, and VGG. However, the key intuitions of our work are equally applicable to any DNN that exhibits layer-wise computational characteristics and trained via SGD, detailed later in this section.

DNNs are designed using a combination of multiple types of layers, which are broadly categorized as convolutional layers (CONV), activation layers (ACTV), pooling layers (POOL), and fully-connected layers (FC). A neural network is structured as a sequence of multiple instances of these layers. DNNs for computer vision tasks in particular are broadly structured into the following two modules: 1) the feature extraction layers that detect distinguishable features across input images, and 2) the classification layers that analyze the extracted features and classify the image into a given image category. Feature extraction layers are generally designed using CONV/ACTV/POOL layers and are positioned as the initial part of the DNN. The classification layers are built upon the FC layers and are found at the end of the DNN computation sequence. The general trend in deep learning is to design the network with a large number of feature extraction layers so that a deep hierarchy of features are trained for robust image classification (Szegedy et al., 2014; Simonyan & Zisserman, 2015; He et al., 2015).

2.2. DNN Training vs. Inference

A neural network needs to be trained before it can be deployed for an inference or classification task. Training entails learning and updating the weights of the layers of a neural network by performing the operations of forward and backward propagation algorithms (LeCun et al., 1998). The direction of traversal, as well as the mathematical operations that must be performed, differ for forward and backward propagation.

Forward Propagation. Forward propagation is performed from the first (input) layer to the last (output) layer, whereas backward propagation is performed in the opposite direction (last to first layer), from right to left in Figure 2. Intuitively, forward propagation traverses the network layer-wise and performs the aforementioned feature extraction and classification tasks on a given input, leading to an image classification. During forward propagation, each layer applies a mathematical operation to its input feature maps (X) and stores the results as output feature maps (Y). For linear feedforward DNNs, the resulting Y of layer \( (n-1) \) is used as the input X by layer \( (n) \). The computation flow of forward propagation is therefore a serialized process, meaning layer \( (n) \) can initiate its layer’s operation only when the preceding layer \( (n-1) \) is finished with its computation and forwarded its Y to layer \( (n) \)’s X. The GPU can therefore only process a single layer’s computation at any given time due to such inter-layer data dependency. As a result, the minimum, per layer memory allocations required are solely determined by the layer’s input-output relationships and its mathematical function\(^1\). For instance, a CONV layer using the most memory-efficient convolutional algorithm (e.g., implicit GEMM in cuDNN (NVIDIA, 2016b)) requires three data structures, the input/output feature maps (X and Y) and the weights of the layer (W) for forward propagation. Employing a fast-fourier-transform (FFT) based algorithm however requires an additional workspace (WS) buffer to manage transformed maps.

Backward Propagation. For DNNs that are not fully trained, however, the inferred image category might not be correct. At the end of forward propagation, a loss function is used to derive the magnitude of the inference error. Specifically, the gradient of the loss function is derived with respect to the rightmost layer \( (N) \)’s output:

\[
\frac{\partial \text{Loss}}{\partial Y_{(N)}}
\]

\(^1\) Popular activation functions (sigmoid/tanh/ReLU) can be refactored into an in-place algorithm using element-wise computation. Both Caffe and Torch leverage this in-place memory optimization for the activation layers and only allocate memory space for Y and dY for forward (Y) and backward (both Y and dY) propagation (Chintala, S., 2015). This paper adopts this in-place optimization for both baseline and vDNN.
The value in Equation 1 is forwarded to the last layer $Y_{(N)}$ as its input gradient maps $(dY)$, and the output gradient maps $(dX)$ are derived based on the chain rule (LeCun et al., 1998):

$$\frac{\partial \text{Loss}}{\partial X_{(N)}} = \frac{\partial \text{Loss}}{\partial Y_{(N)}} \cdot \frac{\partial Y_{(N)}}{\partial X_{(N)}} \tag{2}$$

Because the output $dX$ $(\frac{\partial \text{Loss}}{\partial Y_{(N)}})$ is the product of the input $dY$ $(\frac{\partial \text{Loss}}{\partial Y_{(N)}})$ with $\frac{\partial Y_{(N)}}{\partial X_{(N)}}$, deriving the value of $dX$ for layer $l_{(N)}$ generally requires memory for both its input/output gradient maps $(dY$ and $dX$) and also the input/output feature maps ($X$ and $Y$) for this layer. The calculated $dX$ of layer $l_{(N)}$ is then passed on to the preceding layer $l_{(N-1)}$ to be used as $dY$ for layer $l_{(N-1)}$’s $dX$ derivation. This chain rule is similarly used to derive the gradients of the weights.

Similar to forward propagation, backward propagation is also performed layer-wise to the respective incoming gradient maps, $dY$s. Once backward propagation reaches the leftmost first layer, the weights are adjusted using the weight gradients so that the prediction error is reduced for the next classification task. Hence, training a network involves both forward and backward propagation, which are repeated for millions to billions of iterations. Because of the stochastic nature of SGD-based backward propagation, the network input is generally batched with multiple images (e.g., 128 and 256 images for best performing AlexNet and VGG-16), which helps network convergence.

2.3. Motivation: Memory-Efficient DNN Design

To aid the design and deployment of neural networks, a variety of ML frameworks have been developed in recent years, including Caffe, Torch, TensorFlow, and Theano (Bahrampour et al., 2016). The rich set of features offered by these frameworks coupled with their ability to accelerate the training and inference process using GPUs greatly simplifies the process of implementing neural networks. Despite their flexibility, however, popular machine learning frameworks suffer from severe limitations in the way they allocate and manage memory.

To illustrate the shortcomings of ML frameworks in managing memory, consider the example shown in Figure 2. When implemented using an existing ML framework, the memory required across all of the layers of the neural network is first allocated on the GPU before it starts computing. One of the reasons why such network-wide memory allocation strategy is used is because of the layer-wise gradient updates of backward propagation (property of the chain rule, Section 2.2): each layer’s feature maps ($X$) are later reused during its own backward propagation pass, so all $X$s must be stored in GPU memory until backward computation is completed. Figure 3 shows the amount of memory used for feature maps and its growing significance as network become deeper. The baseline network-wide memory allocation policy is extremely wasteful as computations in a neural network are performed layer-wise. Figure 4 shows the per layer memory usage of VGG-16 during forward propagation, which provides the following key observations. First, the intermediate feature maps and workspace (left axis) incur an order of magnitude higher memory usage compared to the weights (right axis) of each layer. Second, most of these intermediate data structures are concentrated on the feature extraction layers and are less significant for later classifier layers. Third, the weights, while smaller in size compared to these intermediate data, are mostly concentrated on the classifier layers due to their full connectivity. Lastly, the per layer memory usage is much smaller than the memory size allocated by the baseline pol-
icy, showing significant opportunities for memory savings with a fine-grained, layer-wise memory management policy which we detail in Section 3.

3. Virtualized DNNs

The design objective of our virtualized DNN (vDNN) memory manager is to virtualize the memory usage of DNNs, using both GPU and CPU memory, while minimizing its impact on performance. vDNN is completely transparent to the programmer as the allocation, placement, movement, and release of data is seamlessly orchestrated by the system architecture and the runtime system. Such abstraction enables ML practitioners to focus more on their machine learning algorithm and not have to worry about the low level details of GPU memory management. vDNN primarily optimizes the memory usage of the feature extraction layers (CONV/ACTV/POOL) as the majority of memory usage is concentrated on these layers, accounting for 81% of memory usage on AlexNet and 96% on VGG-16 (256). More specifically, we target the feature maps of these feature extraction layers as these intermediate data structures account for the majority of GPU memory usage (Figure 3 and Figure 4). The intuitions of vDNN can also be applied to weights and to the classification layers, but with less of a memory saving benefit.

3.1. Design Principle

As discussed in Section 2.3, the minimum memory requirement per individual layer is substantially smaller than what is actually provisioned with the baseline, network-wide memory allocation policy. vDNN adopts a sliding-window based, layer-wise memory management strategy in which the runtime memory manager conservatively allocates memory from its memory pool for the immediate usage of the layer that is currently being processed by the GPU. Intermediate data structures that are not needed by the currently processing layer are targeted for memory release to reduce memory usage.

Forward Propagation. As shown in Figure 5, a given layer_{(n)}’s forward computation is not dependent on any of the preceding layer’s Xs. For inference-only DNNs, all these Xs can safely be released from the memory pool as the data structures are not reused anymore. For DNN training, blindly releasing the preceding Xs is not an option because all Xs (which also becomes the Ys) are still needed during backward propagation. However, the large numbers of Xs that get allocated for deep networks will camp inside GPU memory without being reused until reaching its backward computation. Given that the latency between the completion of the layer_{(n)}’s forward propagation and the start of the same layer_{(n)}’s backward propagation is on the order of milliseconds to seconds (e.g., more than 100 ms and 2500 ms for the first layer of AlexNet and VGG-16 (64), respectively), tackling these Xs for memory optimization is crucial for efficient utilization of GPU memory. vDNN therefore conditionally offloads these intermediate Xs to CPU-side host memory via the system interconnect (e.g., PCIe, NVLINK) if they are targeted for memory release. Section 3.3 details the vDNN memory transfer policy that decides which layers will offload its X. Once the offload operation is complete, vDNN releases the offloaded X from the memory pool to reduce GPU memory usage.

Backward Propagation. Similar to forward propagation, vDNN aggressively releases data structures that are not needed for training the remaining layers’ backward computation. During layer_{(n)}’s backward propagation, layer_{(n+1)}’s Y and dY are no longer required because the GPU has already completed the gradient updates for this layer (Figure 6). Again, by leveraging the layer-wise DNN backward propagation, vDNN immediately frees up a layer’s Y and dY once this layer’s backward computation is complete. X and dX are not released as the the preceding layer’s backward propagation will be needing these values for gradient derivation. If a layer has offloaded its X to host memory, vDNN should guarantee that the offloaded data is copied back to GPU memory before the gradient update is initiated. Naively copying back the data on-demand will serialize the backward computation behind the memory copying operation of X. The vDNN memory manager therefore launches a prefetch operation for layer_{(n)}’s offloaded feature maps, which is overlapped with layer_{(m)}’s backward computation, with n < m, so that prefetching is launched before its actual usage, hiding prefetching latency.

3.2. Core Operations And Its Design

We prototype vDNN as a layer on top of cuDNN (NVIDIA, 2016b). vDNN employs two separate CUDA streams to overlap normal DNN computations with the memory
Virtualizing Deep Neural Networks for Memory-Efficient Neural Network Design

Figure 6. DNN execution flow during backward propagation. The figure assumes that layer\textsubscript{(2)} is currently being processed by the GPU. Data associated with the arrows marked with black \(X\)s can safely be released because they will not be reused during the training of this input image batch.

allocation, movement, and release operations of vDNN. \textit{streamcompute} is the CUDA stream that interfaces to the cuDNN handle and sequences all the layer’s forward and backward computations. \textit{streammemory} manages the three key components of vDNN; the memory allocation/release, offload, and prefetch.

Memory Allocation/Release. The CUDA library currently only supports \textit{synchronous} memory (de)allocations, meaning that any calls to \textit{cudaMalloc}() or \textit{cudaFree}() will enforce an additional synchronization across all the GPUs within a node. To safely enable vDNN memory operations while not fall into the pitfalls of synchronous CUDA APIs, we employ the open-source \textit{asynchronous} memory allocation/release APIs distributed by NVIDIA (NVIDIA, 2016a). When the program launches, the vDNN memory manager is allocated with a memory pool that is sized to the physical GPU memory capacity. Whenever vDNN allocates (and releases) data structures, the underlying memory manager will reserve (and free) memory regions from this memory pool without having to call \textit{cudaMalloc}() or \textit{cudaFree}().

Memory Offload. Offloading input feature maps during forward propagation is one of the key enablers of vDNN’s memory savings. When a layer is chosen for offloading, our memory manager first allocates a pinned host-side memory region using \textit{cudaMallocHost}(). \textit{streammemory} then launches a non-blocking memory transfer of this layer’s \(X\) to the pinned memory via PCIe using \textit{cudaMemcpyAsync}(), overlapping it with the same layer’s normal forward computation. The current implementation of vDNN synchronizes \textit{streamcompute} and \textit{streammemory} at the end of each layer’s forward computation if \textit{streammemory} has offloaded its feature maps. This approach guarantees that the offloaded data is safely released from the memory pool before the next layer begins forward computation, maximizing the memory saving benefits of vDNN offloading. Because the Xs of CONV and POOL layers are read-only data structures, overlapping layer\textsubscript{(n)}’s offload operation with the same layer’s forward propagation does not create any correctness issues. ACTV layers are already refactored into an in-place algorithm and only use \(Y\) and \(dY\) for gradient updates, obviating the need for memory offloading (Section 2.2). Figure 7 provides a high level overview of vDNN’s offload operation. Here, the baseline system is able to immediately launch layer\textsubscript{(2)}’s forward computation once layer\textsubscript{(1)} is complete. The execution of layer\textsubscript{(2)} is stalled for vDNN, because \textit{streamcompute} must wait until the offloading of \textit{streammemory} is complete, blocking layer\textsubscript{(2)}’s computation. The computation of layer\textsubscript{(3)} is not delayed however because the offload latency for layer\textsubscript{(2)} is completely hidden inside the same layer’s forward computation.

Memory Prefetch. Similar to memory offloads, prefetching the offloaded Xs back to GPU memory is implemented using \textit{cudaMemcpyAsync}() to overlap data transfers with the computations of backward propagation. However \textit{streammemory} launches prefetch operations in the reverse order relative to the offload operations from forward propagation (Figure 7). As mentioned in Section 3.1, the general rule of prefetching is to overlap the memory copy operation of layer\textsubscript{(n)}’s offloaded data with layer\textsubscript{(m)}’s backward computation, with layer ID \(m\) always being higher than \(n\) to maximize the benefit of both prefetching and latency hiding. In other words, when the GPU starts the backward propagation of layer\textsubscript{(m)}, the vDNN memory manager determines the best layer to prefetch among the preceding layers (as \(n < m\)).

If the distance between the prefetched layer\textsubscript{(n)} and overlapping layer\textsubscript{(m)} is too far away, the memory saving benefit of vDNN offloading will be reduced because the reuse...
Virtualizing Deep Neural Networks for Memory-Efficient Neural Network Design

Figure 8. Pseudo code explaining how vDNN finds layers to prefetch. Notice how the search operation is only up to the next closest CONV layer (line 14), guaranteeing that the prefetched X will not end up being used too far away in the future as it restricts the prefetch layer to be within the search window of layers.

time of this prefetched data will be distant in the future. In other words, prefetching data too early in time will again suboptimally utilize GPU memory as the prefetched data will once again camp inside the GPU memory without immediate usage. We carefully designed the vDNN prefetch algorithm to avoid this pitfall and balance the memory saving benefits of offloading with the timeliness of prefetching. Figure 8 is a pseudo-code of the vDNN prefetch algorithm that determines the best candidate layer for prefetching. Before stream\text{\_compute} starts a layer’s backward computation, vDNN first searches for a potential layer that requires prefetching of its X. If the search operation is successful (line 11), the layer ID to be prefetched is returned by find\_prefetch\_layer routine and is used to launch its prefetch operation via stream\_memory. Similar to offloading, vDNN synchronizes stream\_compute and stream\_memory so that the next layer’s backward computation is stalled until the prefetch operation is finalized. Consequently, any prefetch operation launched during layer\(_n\)’s backward computation is guaranteed to be ready before layer\(_{n-1}\)’s computation. This benefit of course comes at the cost of a potential performance loss when the prefetch latency is longer than the overlapped computation, which we quantitatively detail in Section 5.3.

3.3. vDNN Memory Transfer Policy

Determining the best layers to offload/prefetch their feature maps is a multi-dimensional optimization problem that must consider: 1) physical GPU memory size, 2) the convolutional algorithms used and the overall layer-wise memory usage, and 3) the network-wide performance. The first two factors determine whether we are able to train the network at all (which we refer to as trainability of a network), while the last factor decides overall training productivity. If vDNN were to use the most memory-efficient convolutional algorithm for all layers (e.g., implicit GEMM in cuDNN (NVIDIA, 2016b) which does not require any WS) while also having all layers offload/prefetch, the GPU memory usage will be the lowest. Performance will likely suffer, however, compared to a baseline with the fastest convolutional algorithms adopted for each layer; the performance loss primarily comes from 1) the additional latency possibly incurred due to offload/prefetch, and 2) the performance difference between memory-optimal implicit GEMM and the performance-optimal convolutional algorithm. Going with the fastest convolutional algorithm, without any offload/prefetch, will result in the highest possible performance, but the potential memory overheads for the faster algorithm’s workspace and the cumulative Xs that camp inside the GPU memory will likely overflow the GPU memory budget. Given that optimizing the layer-wise memory usage and its performance is in itself a multi-dimensional optimization problem, selecting the most optimal hyperparameters across the entire network is non-trivial. We therefore adopt the following heuristic-based memory transfer policies that narrow the parameter choices and simplify the optimization problem, while still performing robustly in practice.

Static vDNN. The feature extraction layers are mostly composed of CONV and ACTV layers with intermittent POOL layers that downsize the dimensionality of the feature maps. More than 70% to 80% of the (forward/backward) computation time however is spent on the CONV layers for deep neural networks. We therefore evaluate two static vDNN memory transfer options that exploit this computational characteristic. The first option we explore is to have the vDNN memory manager offload all of the Xs of all the layers. This policy, vDNN\text{\_all}, is our most memory-efficient solution as all Xs are offloaded and released from the GPU, drastically reducing device memory usage. The second vDNN policy is to only offload Xs for the CONV layers and leave the remaining layers’ Xs resident inside GPU memory (vDNN\text{\_conv}). The vDNN\text{\_conv} policy is based on the observation that CONV layers have a much longer computation latency than ACTV/POOL layers, being more likely to hide the latency of offload/prefetch. Not surprisingly the performance of vDNN\text{\_conv} is generally higher than vDNN\text{\_all}. But vDNN\text{\_all} has the advantage of consuming the least GPU memory, significantly enhancing the trainability of a DNN. We later evaluate the trainability, memory usage, and performance of these two static policies with the memory-optimal and performance-optimal convolutional algorithms.

Dynamic vDNN. While static vDNN is simple and easy to implement, it does not account for the system architectural components that determine the trainability and overall performance of a DNN (e.g., maximum compute FLOPs and memory bandwidth, memory size, effective PCIe band-
width, etc). For DNNs that comfortably fit within a given GPU memory capacity, neither \texttt{vDNN\textsubscript{all}} nor \texttt{vDNN\textsubscript{conv}} is optimal as the best approach is to have all the memory allocations resident in GPU without any offloading and employ the fastest possible convolutional algorithm. Large and deep networks, on the other hand, might not have the luxury of using faster convolutional algorithms. So being able to fit such network on the GPU is the best optimization \texttt{vDNN} could make. We therefore develop a dynamic \texttt{vDNN} policy that automatically determines the offloading layers and the convolutional algorithms employed, at runtime, to balance the trainability and performance of a DNN. Dynamic \texttt{vDNN} augments this profiling stage with a number of additional profiling passes that are required for training. NVIDIA’s cuDNN provides a runtime API that experiments with all available convolution algorithms for a given layer, evaluating each algorithm’s performance and its memory usage. Current ML frameworks leverage this API to undergo an intial profiling stage to determine the best algorithms to deploy for each CONV layer for best performance. The overhead of such profiling is on the order of a few tens of seconds, which is negligible relative to the days to weeks required for DNN training. Our dynamic \texttt{vDNN} augments this profiling stage with a number of additional profiling passes to select the best layers to offload and the best per layer algorithm. Once the baseline profile stage is completed and the fastest possible convolutional algorithms are derived for all CONV layers, dynamic \texttt{vDNN} employs the following additional profiling passes:

1. First, the static \texttt{vDNN\textsubscript{all}} is tested for a single training pass with all CONV layers using the memory-optimal, no-WS incurred algorithm. Because this configuration uses the least memory, this initial pass determines if the target DNN can be trained at all.

2. If \texttt{vDNN\textsubscript{all}} passed, another training phase is launched with all CONV layers employing the fastest algorithms but without any offloading. Such a configuration, if it passes successfully, will be adopted for the rest of the full training procedure as it provides the highest performance while guaranteeing trainability. If this profiling phase fails due to memory over-subscription, two additional training passes are tested with the same fastest algorithms, but with \texttt{vDNN} offloading enabled for both \texttt{vDNN\textsubscript{conv}} and \texttt{vDNN\textsubscript{all}} respectively. If successful, \texttt{vDNN} employs the succeeded configuration for the rest of training. If both \texttt{vDNN\textsubscript{conv}} and \texttt{vDNN\textsubscript{all}} fails, we move on to the next profiling pass below to further reduce memory usage.

3. The last phase is based on a greedy algorithm that tries to locally reduce a layer’s memory usage, seeking a global optimum state for the given GPU system, in terms of trainability and performance. When traversing through each layer, the \texttt{vDNN} first calculates whether using the fastest algorithm will overflow the GPU memory budget. If so, then the given layer’s convolutional algorithm will be locally downgraded into a less performant but more memory-efficient one, until it reaches the memory-optimal implicit GEMM. This greedy-based approach first tries \texttt{vDNN\textsubscript{conv}} with each CONV layer initially using its own performance-optimal algorithm. If \texttt{vDNN\textsubscript{conv}} fails, then another training pass is launched with the more memory-efficient \texttt{vDNN\textsubscript{all}}. If \texttt{vDNN\textsubscript{all}} also fails with this greedy algorithm, then \texttt{vDNN} resorts back to the very first \texttt{vDNN\textsubscript{all}} solution, with the memory-optimal, no-WS algorithms applied across the entire network.

While other possible settings might better balance performance and trainability, we find that our dynamic \texttt{vDNN} performs competitively without having to exhaustively search for globally optimal parameter selections.

4. Methodology

4.1. \texttt{vDNN} Memory Manager

We implemented a host-side memory manager that interacts with the latest and fastest version of cuDNN 4.0 (NVIDIA, 2016b), which serves as the GPU backend to accelerate DNN layer computations. All the layers that constitute a DNN’s feature extraction layer (CONV/ACTV/POOL) have been implemented using cuDNN, and the execution of each layer is orchestrated using two CUDA streams, \texttt{stream\textsubscript{compute}} and \texttt{stream\textsubscript{memory}} as discussed in Section 3.2. The classification layers remain unchanged and use the same cuBLAS routines as Torch. Our \texttt{vDNN} API interface closely resembles that of Torch and Caffe, providing the high level abstractions of the target DNN architecture and each of its layer compositions.

While there are subtle differences between Torch, Caffe, and Theano’s memory allocation scheme, prior work quantitatively demonstrated that all three frameworks exhibit comparable performance and memory requirements (Bahrampour et al., 2016). We therefore choose Torch’s memory management policy as the baseline scheme to compare against \texttt{vDNN} given its widespread deployment across both academia and industry (e.g., Facebook and Google DeepMind). This baseline memory allocation scheme is based on the network-wide allocation policy discussed in Section 2.3. However, we improve this baseline policy using the following strategy to reduce memory consumption during the backward propagation phase (S. Gross and M. Wilber, 2016; Chen et al., 2015): rather than allocating separate \texttt{dY} and \texttt{dX} for individual
layers, we only allocate a single data structure for each of these and reuse them after each layer’s backward computation is complete (Figure 2).

4.2. GPU Node Topology

To evaluate the performance-memory consumption trade-offs of the proposed vDNN framework, we conducted experiments on NVIDIA’s K40 GPU which provides the highest computational throughput (single precision throughput of 5 TFLOPS), memory bandwidth (max 288 GB/sec), and memory capacity (12 GB) in the family of Kepler GPUs. The GPU card communicates with the host-side memory via a PCIe switch (gen3) which provides a maximum 16 GB/sec memory transfer bandwidth.

4.3. DNN Benchmarks

Conventional DNNs. First, we evaluate existing, state-of-the-art DNNs: AlexNet (Krizhevsky et al., 2012), OverFeat (Sermanet et al., 2013), and four different batch sizes for VGG-16 (the deepest configuration with 16 CONV and 3 FC layers) (Simonyan & Zisserman, 2015). The network configurations of these existing DNNs are identical to the reference models maintained by the developers at Facebook (Chintala, S., 2016). While the memory usage of AlexNet and OverFeat is already below the 12 GB memory capacity of K40 (Figure 3), we use it to evaluate the performance regression on these networks with vDNN. VGG-16 is one of the largest and deepest DNN architecture to date, requiring substantial memory capacity for trainability (using up to 28 GB of memory when trained with the best performing batch size of 256). We use VGG-16 as a representative, future-looking DNN architecture that stresses the memory capacity limits of today’s GPUs.

Very Deep Networks. To highlight vDNN’s effectiveness in training very deep networks, we collected a second set of benchmarks by extending the number of CONV layers of VGG, from 16 CONV layers to 516 CONV layers. The original VGG network features a homogeneous architecture that only uses \(3 \times 3\) convolutions (with stride 1 and pad 1) and \(2 \times 2\) pooling operations (with stride 2), from the first to the last feature extraction layer. The feature extraction layers are conceptually divided into five groups of CONV layers, separated by the intermediate POOL layers. The only difference among these CONV layer groups is that the number of output feature maps grows from 64 to 512, from the first to the last layer group. Simonyan and Zisserman (Simonyan & Zisserman, 2015) studied the effect of layer depth on classification accuracy by incrementally adding more CONV layers to each of these layer groups, going from 8 CONV layers to 16 CONV layers. We follow similar measures to deepen the layer depth of VGG by gradually adding 100 more CONV layers to VGG-16, resulting in VGG-116/216/316/416/516 network configurations. For each addition of 100 CONV layers, we add 20 more CONV layers to each of the five CONV layer groups. The added CONV layers have the same number of output feature maps that are employed for that layer group. We use these five VGG-like networks to perform a case study on vDNN’s effectiveness on training very deep networks that require much more memory.

5. Results

This section evaluates the effect of vDNN on GPU memory usage, network trainability, off-chip memory bandwidth utilization, and overall performance. The static vDNN\(_{all}\) and vDNN\(_{conv}\) policies are denoted as \(\text{all}\) and \(\text{conv}\) in all the figures discussed in this section and are each evaluated with both memory-optimal and performance-optimal (denoted as \(m\) and \(p\)) convolutional algorithms across the network. The baseline memory manager (base) is similarly evaluated with both memory-optimal and performance-optimal algorithms. The algorithms are dynamically chosen for vDNN\(_{dyn}\) (denoted as \(\text{dyn}\)) as discussed in Section 3.3. Memory management policies that fail in training the network, due to memory oversubscription, are marked with (×).

5.1. GPU Memory Usage

Because vDNN adopts a layer-wise memory allocation policy, the GPU memory usage during forward/backward propagation will fluctuate depending on the memory offloading policy chosen and the convolutional algorithm employed for a given layer (Figure 4). We therefore discuss both the maximum and average memory usage as shown in Figure 9. The maximum memory usage corresponds to the largest memory allocated across the entire run, which decides whether the target DNN application can be trained at all. The average memory on the other hand reflects how much memory has been used on average, and conversely, freed up during forward/backward propagation. The smaller the average memory usage becomes, the more likely vDNN will have headroom to improve performance by: 1) employing performance-efficient convolutional algorithms that may require larger workspace, and 2) reducing the total number of offload layers and prevent potential performance drops due to offloading (Figure 7).

Because the baseline network-wide memory manager provisions the memory allocations to accommodate the entire network usage, the maximum and average memory usage are identical. The baseline policy therefore is not able to train networks like VGG-16 with batch 128 and 256, which require more than the physically available 12 GB of memory. Our vDNN enhances the trainability of a network by significantly reducing its memory requirements. Overall,
the memory-optimal \( \nuDNN\text{all}(m) \) shows both the smallest average and maximum memory usage as it always offloads a layer’s input feature maps while using the most memory-efficient algorithms. As a result, \( \nuDNN\text{all} \) exhibits the highest offload traffic being sent to host memory, reaching up to 16 GB of GPU memory savings for VGG-16 (256) (Figure 10). Such aggressive offloading significantly improves memory efficiency and achieves an average 69% and 92% reduction on the maximum and average memory usage of the networks shown in Figure 9. When employed with the performance-optimal algorithm, the average memory savings of \( \nuDNN\text{all} \) are slightly reduced to 50% and 85% for the maximum and average memory usage. Because \( \nuDNN\text{conv} \) only offloads the feature maps for the CONV layers, its memory savings is not as high as \( \nuDNN\text{all} \). However, \( \nuDNN\text{conv} \) still reduces the maximum and average memory usage by 39% and 72% on average, even when the performance-optimal algorithms are employed.

\( \nuDNN\text{dyn} \) allocates the largest memory space among the three \( \nuDNN \) policies, reducing the maximum and average memory consumption by 37% and 64% on average compared to baseline. This is because \( \nuDNN\text{dyn} \) tries to balance its memory usage and performance, seeking to fit the network within GPU memory capacity while still optimizing performance by minimizing the number of offload layers and employing the fastest possible convolutional algorithms. The static \( \nuDNN\text{all} \) and \( \nuDNN\text{conv} \), on the other hand, do not consider the overall performance when the offloaded layers are chosen. For instance, VGG-16 (128) trained with memory-optimal \( \nuDNN\text{all} \) only uses up to 4.8 GB out of the 12 GB of available memory. This configuration leads to a 49% performance loss (Section 5.3) as \( \nuDNN\text{all} \) fails to exploit the remaining 7.2 GB of the memory for performance optimizations. \( \nuDNN\text{dyn} \) tries to bridge this gap by dynamically deriving the offload layers as well as the best convolutional algorithms to employ. We further discusses \( \nuDNN \)'s impact on performance in detail at Section 5.3.

5.2. Impact on Memory System

While \( \nuDNN \) helps virtualize DNN’s memory usage, it does come at the cost of adding more read (offload) and write (prefetch) traffic to the GPU memory subsystem, potentially interfering with the normal cuDNN operations that train the network. Because the additional memory traffic \( \nuDNN \) introduces can be up to the bandwidth of the PCIe bus (maximum of 16 GB/sec for gen3), its effect on overall performance will be determined by the normal cuDNN operation’s memory bandwidth intensity. Figure 11 shows the baseline’s maximum DRAM bandwidth utilization for VGG-16, which is measured separately for each CONV.
layer’s forward and backward propagation\(^2\). Feature extraction layers rarely saturate the peak memory bandwidth of 288 GB/sec, providing more than enough headroom for \(v\text{DNN}\)’s offload/prefetch traffic. Even if a hypothetical, future convolutional algorithm were to completely saturate the off-chip DRAM bandwidth, \(v\text{DNN}\)’s additional traffic will approximately incur up to a worst-case (16/288) = 5.5% performance overheads, which we believe is reasonable given the benefit of virtualized memory.

### 5.3. Performance

Figure 12 summarizes the performance of the static/dynamic \(v\text{DNN}\) compared to the baseline. For a conservative evaluation, we only compare the latencies incurred in the feature extraction layers because the classifier layers are executed identically for the baseline and \(v\text{DNN}\). Because the baseline policy requires more than 12 GB of memory allocations for VGG-16 (128) and VGG-16 (256) (15 GB and 28 GB respectively), it is impossible to train these two networks on a single GPU card. We therefore establish an oracular baseline that removes the memory capacity bottlenecks of these two networks for a conservative evaluation. The performance of this oracular baseline is estimated by configuring all CONV layers with the fastest algorithms and evaluating the latencies of each layer individually. The latencies are later accumulated altogether to estimate overall performance. Overall, \(v\text{DNN}_{\text{all}}\) and \(v\text{DNN}_{\text{conv}}\) with memory-optimal algorithms exhibit an average 46% and 43% performance loss (maximum 59% and 56% degradation) compared to baseline, an expected result as the memory manager put no effort into balancing memory usage and overall performance. The dynamic \(v\text{DNN}_{\text{dyn}}\) does much better in terms of balancing memory efficiency and overall throughput, closing the performance gap between the static \(v\text{DNN}\) and baseline and reaching 95% of baseline’s throughput (worst case 78% of the oracular baseline, for VGG-16 (256)).

### 5.4. Case Study: Training Very Deep Networks

Our scalable, memory-efficient \(v\text{DNN}\) solution provides ML practitioners with the ability to train deep networks, such as those studied in (Szegedy et al., 2014; Simonyan & Zisserman, 2015; He et al., 2015). To highlight \(v\text{DNN}\)’s effectiveness and scalability in training very deep networks, we perform a case study on five VGG-like networks that contain hundreds of CONV layers. Figure 13 shows the maximum memory usage of the baseline and \(v\text{DNN}_{\text{dyn}}\) for these very deep neural networks. As the number of CONV layers increases from 16 to 516, the baseline memory requirements monotonically increase by 16 times (from 4.9 GB to 80.6 GB), even with a small batch size of 32. Thanks to its layer-wise memory allocation policy, \(v\text{DNN}_{\text{dyn}}\) significantly reduces the memory usage of all five networks, only using up to 5.8 GB of memory even for most memory hungry VGG-516. \(v\text{DNN}_{\text{dyn}}\) also provided 99% of the throughput for all five networks.

### 6. Related Work

There have been a variety of proposals aiming to reduce the memory requirements of neural networks. A popular approach explored by researchers is to remove redundancies in the network architecture. Network pruning techniques (Hanson & Pratt, 1989; LeCun et al., 1990; Hassibi & Stork, 1993) where small weight connections are removed from the network are examples of this ap-
proach. Network pruning results in fewer weights, leading to a reduction in memory consumption. Recent work by Song et al. (Han et al., 2015b) show that leveraging pruning while training can significantly reduce memory requirements for weights without any loss in classification accuracy.

Another redundancy mitigating approach uses quantization to reduce the number of bits required to represent the weights of a network. Vanhoucke et al. (Vanhoucke et al., 2011) use reduced precision representations of weights and activations to mitigate the memory requirements of networks. The authors in (Han et al., 2015a) employ a weight sharing approach where the weights of the network are binned into clusters and represented using the cluster centroids. A variety of compression techniques have also been explored by researchers (Gong et al., 2014) to reduce the memory requirements of neural networks.

Although these prior studies reduce DNN memory requirements, they fall short in several respects. First, weights only account for a small fraction of the overall memory consumption in state-of-the-art deep neural networks, as shown in Figure 3. Thus, proposals that optimize memory requirements of weights, while beneficial in terms of memory bandwidth utilization and energy-efficiency, provide only limited opportunity for memory capacity savings. Second, using reduced precision occasionally results in loss of classification accuracy unless carefully tuned for the given architecture and task. Our proposal targets memory consumptions of the most dominant data structures in deep networks, the intermediate feature maps, providing substantial memory saving benefits.

7. Discussion and Future Work

While this paper highlights the memory saving benefits of vDNN using linear, feedforward style DNNs, the intuition of vDNN is equally applicable to other network topologies, such as those in GoogLeNet (Szegedy et al., 2014), ResNet (He et al., 2015), and recurrent neural networks (RNNs) (Graves & Schmidhuber, 2005). The inception module in GoogLeNet for instance contains one-to-many (fork) and many-to-one (join) inter-layer communication patterns, affecting the order in which the vDNN offload/prefetch/release operations are launched. However, since the training of these networks is still performed layer-wise using the backpropagation algorithm, the memory saving benefits of vDNN are retained. RNNs have inter-layer connections that form a directed cycle, distinguishing them from feedforward networks. The computation flow of these RNNs, however, are similar to feedforward networks once they are unrolled in their time sequences.

8. Conclusion

Existing machine learning frameworks require users to carefully manage their GPU memory usage so that the overall network-wide memory requirements are within the physically available GPU memory. We propose and evaluate virtualized DNN, a scalable, memory-efficient runtime memory manager that virtualizes the memory usage of a network across both CPU and GPU memories. Our virtualized DNN solution reduces the average memory usage of AlexNet by 61% and OverFeat by 83%, substantially improving the memory-efficiency of DNNs. Similar experiments to VGG-16 result in an average 60% reduction in memory usage at a cost of 22% performance penalty compared to an oracular baseline with infinite memory. We also study the scalability of vDNN to extremely deep neural networks, demonstrating that vDNN can train networks with hundreds of convolutional layers, as long as their per layer memory usage fits within a GPU memory budget.

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