Brian2Loihi: An emulator for the neuromorphic chip Loihi using the spiking neural network simulator Brian

Carlo Michaelis\textsuperscript{1,2,*}, Andrew B. Lehr\textsuperscript{1,2,*}, Winfried Oed\textsuperscript{1,2,*}, and Christian Tetzlaff\textsuperscript{1,2}

\textsuperscript{1}Department of Computational Neuroscience, University of Göttingen, Germany
\textsuperscript{2}Bernstein Center for Computational Neuroscience, University of Göttingen, Germany
\textsuperscript{*}These authors contributed equally.

Abstract

Developing intelligent neuromorphic solutions remains a challenging endeavour. It requires a solid conceptual understanding of the hardware’s fundamental building blocks. Beyond this, accessible and user-friendly prototyping is crucial to speed up the design pipeline. We developed an open source Loihi emulator based on the neural network simulator Brian that can easily be incorporated into existing simulation workflows. We demonstrate errorless Loihi emulation in software for a single neuron and for a recurrently connected spiking neural network. On-chip learning is also reviewed and implemented, with reasonable discrepancy due to stochastic rounding. This work provides a coherent presentation of Loihi’s computational unit and introduces a new, easy-to-use Loihi prototyping package with the aim to help streamline conceptualisation and deployment of new algorithms.

1 Introduction

Neuromorphic computing offers exciting new computational structures. Decentralised units inspired by neurons are implemented in hardware (reviewed by Rajendran et al., 2019; Schuman et al., 2017; Young et al., 2019). These can be connected up to one another, stimulated with inputs, and the resulting activity patterns can be read out from the chip as output. A variety of algorithms and applications have been developed in recent years, including robotic control (DeWolf et al., 2020; DeWolf et al., 2016; Michaelis et al., 2020; Stagsted et al., 2020), spiking variants of deep learning algorithms, attractor networks, nearest-neighbor or graph search algorithms (reviewed by Davies et al., 2021). Moreover, neuromorphic hardware may provide a suitable substrate for performing large scale simulations of the brain (S. Furber, 2016; Thakur et al., 2018). Neuromorphic chips specialised for particular computational tasks can either be provided as a neuromorphic computing cluster or be integrated into existing systems, akin to graphics processing units (GPU) in modern computers (Davies et al., 2021; S. B. Furber et al., 2014). With the right ideas, networks of spiking units implemented in neuromorphic hardware can provide the basis for powerful and efficient computation. Nevertheless, the development of new algorithms for spiking neural networks, applicable to neuromorphic hardware, is a challenge (Bouvier et al., 2019; Grünig & Bohte, 2014; Pfeiffer & Pfeil, 2018).

At this point, without much background knowledge of neuromorphic hardware, one can get started programming using the various software development kits available (e.g., Brüderle et al., 2011; Lin et al., 2018; Michaelis, 2020; E. Müller, Mauch, et al., 2020; E. Müller, Schmitt, et al., 2020; Rhodes et al., 2018; Rueckauer et al., 2021; Sawada et al., 2016; Spilger et al., 2020). Emulators for neuromorphic hardware
(S. B. Furber et al., 2014; Luo et al., 2018; Petrovici et al., 2014; Valancius et al., 2020) running on a standard computer or field programmable gate arrays (FPGA), make it possible to develop neuromorphic network architectures without even needing access to a neuromorphic chip (see e.g. NengoLoihi\(^1\) and Dynap-SE\(^2\)). This can speed up prototyping as the initialisation of networks, i.e. distributing neurons and synapses, as well as the readout of the system’s state variables on neuromorphic chips takes some time. At the same time emulators transparently contain the main functionalities of the hardware in code and therefore provide insights into how it works. With this understanding, algorithms can be intelligently designed and complex network structures implemented.

In the following, we introduce an emulator for the digital neuromorphic chip Loihi (Davies et al., 2018) based on the widely used spiking neural network simulator Brian (Stimberg et al., 2019). We first dissect an individual computational unit from Loihi. The basic building block is a spiking unit inspired by a current based leaky integrate and fire (LIF) neuron model (see Gerstner et al., 2014). Connections between these units can be plastic, enabling the implementation of diverse on-chip learning rules. Analysing the computational unit allows us to create an exact emulation of the Loihi hardware on the computer. We extend this to a spiking neural network model and demonstrate that both Loihi and Brian implementations match perfectly. This exact match means one can do prototyping directly on the computer using Brian only, which adds another emulator in addition to the existing simulation backend in the Nengo Loihi library. This increases both availability and simplicity of algorithm design for Loihi, especially for those who are already used to working with Brian. In particular for the computational neuroscience community, this facilitates the translation of neuroscientific models to neuromorphic hardware. Finally, we review and implement synaptic plasticity and show that while individual weights show small deviations due to stochastic rounding, the statistics of a learning rule are preserved. Our aim is to facilitate the development of neuromorphic algorithms by delivering an open source emulator package that can easily be incorporated into existing workflows. In the process we provide a solid understanding of what the hardware computes, laying the appropriate foundation to design precise algorithms from the ground up.

2 Loihi’s computational unit and its implementation

Developing a Loihi emulator requires precise understanding of how Loihi works. And to understand how something works, it is useful to “take it apart and put it back together again”. While we will not physically take the Loihi chip apart, we can inspect the components of its computational units with “pen and paper”. Then, by implementing each component on a computer we will test that, when put back together, the parts act like we expect them to. In the following we highlight how spiking units on Loihi approximate a variant of the well-known LIF model using first order Euler numerical integration with integer precision. This understanding enables us to emulate Loihi’s spiking units on the computer in a way that is straightforward to use and easy to understand. For a better intuition of how the various parameters on Loihi interact, we refer readers to our neuron design tool\(^3\) for Loihi. Readers familiar with Davies et al. (2018) and numerical implementations of LIF neurons may prefer to skip to Section 2.3.

2.1 Loihi’s neuron model: a recap

The basic computational unit on Loihi is inspired by a spiking neuron (Davies et al., 2018). Loihi uses a variant of the leaky integrate and fire neuron model (Gerstner et al., 2014) (see Appendix 7.1). Each

\(^1\)https://www.nengo.ai/nengo-loihi/

\(^2\)https://code.ino.uzh.ch/vigit/NICE-workshop-2021

\(^3\)anonymized
unit $i$ of Loihi implements the dynamics of the voltage $v_i$

$$\frac{dv_i}{dt} = -\frac{1}{\tau_v} v_i(t) + I_i(t) - v_i^{th} \sigma_i(t),$$

(1)

where the first term controls the voltage decay, the second term is the input to the unit, and the third term resets the voltage to zero after a spike by subtracting the threshold. A spike is generated if $v_i > v_i^{th}$ and transmitted to other units to which unit $i$ is connected. In particular, $v_i$ models the voltage across the membrane of a neuron, $\tau_v$ is the time constant for the voltage decay, $I_i$ is an input variable, $v_i^{th}$ is the threshold voltage to spike, and $\sigma(t)$ is the so-called spike train which is meant to indicate whether the unit spiked at time $t$. For each unit $i$, $\sigma_i(t)$ can be written as a sum of Dirac delta distributions

$$\sigma_i(t) = \sum_k \delta(t - t_{i,k}),$$

(2)

where $t_{i,k}$ denotes the time of the $k$-th spike of unit $i$. Note that $\sigma_i$ is not a function, but instead defines a distribution (i.e. generalised function), and is only meaningful under an integral sign. It is to be understood as the linear functional $\langle \sigma_i, f \rangle := \int \sigma_i(t) f(t) \, dt = \sum_k f(t_{i,k})$ for arbitrary, everywhere-defined function $f$ (see Corollary 1 in Appendix 7.1.2).

Input to a unit can come from user defined external stimulation or from other units implemented on chip. Davies et al. (2018) describe the behavior of the input $I(t)$ with

$$I_i(t) = \sum_j J_{ij} (\alpha_I * \sigma_j)(t) + I_i^{bias},$$

(3)

where $J_{ij}$ is the weight from unit $j$ to $i$, $I_i^{bias}$ is a constant bias input, and the spike train $\sigma_j$ of unit $j$ is convolved with the synaptic filter impulse response $\alpha_I$, given by

$$\alpha_I(t) = \exp \left( -\frac{t}{\tau_I} \right) H(t),$$

(4)

where $\tau_I$ is the time constant of the synaptic response and $H(t)$ the unit step function. Note that $\alpha_I(t)$ is defined differently here than in Davies et al. (2018) (see Appendix 7.1.3 for details). The convolution from Equation 3 is a notational convenience for defining the synaptic input induced by an incoming spike train, simply summing over the time-shifted synaptic response functions, namely $\langle \sigma_i * f \rangle(t) = \langle \sigma_i, \tau_I f \rangle = \sum_k f(t - t_{i,k})$, where $\tau_I f(x) = f(x - t_I)$ and $\tilde{f}(x) = f(-x)$ (see Appendix 7.1.2).

### 2.2 Implementing Loihi’s spiking unit in software

From the theoretical model on which Loihi is based, we can derive the set of operations each unit implements with a few simple steps. Using a first order approximation for the differential equations gives the update equations for the voltage and synaptic input described in the Loihi documentation. Combined with a few other details regarding Loihi’s integer precision and the order of operations, we will have all we need to implement a Loihi spiking unit in software.

#### Synaptic input

From Equation 3 we see that the synaptic input can be written as a sum of exponentially decaying functions with amplitude $J_{ij}$ beginning at the time of each spike $t_{j,k}$ (see Appendix 7.1.2). In particular we have

$$I_i(t) = \sum_j J_{ij} \sum_k \exp \left( \frac{t_{j,k} - t}{\tau_I} \right) H(t - t_{j,k}) + I_i^{bias},$$

(5)
To understand the behavior of the synaptic input it is helpful to consider the effect of one spike arriving at a single synapse. Simplifying Equation 5 to just one neuron that receives just one input spike at time $t_1 = 0$, for $t \geq 0$ we get

$$I(t) = J \cdot \exp \left( -\frac{t}{\tau_I} \right)$$

and for $t < 0$, $I(t) = 0$. Each spike induces a step increase in the current which decays exponentially with time constant $\tau_I$. Taking the derivative of both sides with respect to $t$ gives

$$\frac{dI}{dt} = -\frac{1}{\tau_I} \cdot I(t), \quad I(0) = J.$$ (7)

Applying the forward Euler method to the differential equation for $\Delta t = 1$ and $t \geq 0$, $t \in \mathbb{N}$ we get

$$I[t] = I[t - 1] - \frac{1}{\tau_I} \cdot I[t - 1] + J \cdot s[t],$$ (9)

where $s[t]$ is zero unless there is an incoming spike on the synapse, in which case it is one. Here, $s[0] = 1$ and $s[t] = 0$ for $t > 0$. With this we have simply incorporated the initial condition into the update equation. Note that we have switched from a continuous (e.g. $I(t)$) to discrete (e.g. $I[t]$) time formulation, where $\Delta t = 1$ and $t$ is unitless.

Loihi has a decay value $\delta^I$, which is inversely proportional to $\tau_I$, namely $\delta^I = 2^{12}/\tau_I$. Swapping $\tau_I$ by $\delta^I$ reveals

$$I[t] = I[t - 1] \cdot (2^{12} - \delta^I) \cdot 2^{-12} + J \cdot s[t].$$ (10)

The weight $J$ is defined via the mantissa $\tilde{w}_{ij}$ and exponent $\Theta$ (see Section 3.1) such that the equation describing the synaptic input becomes (with indices)

$$I_i[t] = I_i[t - 1] \cdot (2^{12} - \delta^I) \cdot 2^{-12} + 2^{6+\Theta} \cdot \sum_j (\tilde{w}_{ij} \cdot s_j[t]),$$ (11)

where $s_j[t] \in \{0, 1\}$ is the spike state of the $j^{th}$ input neuron. Please note that Equation 11 is identical to the Loihi documentation.

From this we can conclude that the implementation of synaptic input on Loihi is equivalent to evolving the LIF synaptic input differential equation with the forward Euler numerical integration method (see Figure 1A1).

Voltage

It is straightforward to perform the same analysis as above for the voltage equation. We consider the subthreshold voltage dynamics for a single neuron and can therefore ignore the reset term $v_i^{th}(t)$ from Equation 1, leaving us with

$$\frac{dv}{dt} = -\frac{1}{\tau_v} v(t) + I(t).$$ (12)

Applying forward Euler gives

$$v[t] = v[t - 1] - \frac{v[t - 1]}{\tau_v} + I[t].$$ (13)

Again, to compare with the Loihi documentation we need to swap the time constant $\tau_v$ by a voltage decay parameter, $\delta^v$, which is inversely proportional to the time constant, the same as above for synaptic input. Plugging in $\tau_v = 2^{12}/\delta^v$ leads to

$$v[t] = v[t - 1] \cdot (2^{12} - \delta^v) \cdot 2^{-12} + I[t].$$ (14)
By introducing a bias term, the voltage update becomes

\[ v_i[t] = v_i[t-1] \cdot (2^{12} - \delta^u) \cdot 2^{-12} + I_i[t] + I_{i}^{\text{bias}}. \]  

Equation 15 agrees with the Loihi documentation. Like the synaptic input, the voltage implementation on Loihi is equivalent to updating the LIF voltage differential equation using forward Euler numerical integration (see Figure 1A2).

**Integer precision**

Loihi uses integer precision. So the mathematical operations in the update equations above are to be understood in terms of integer arithmetic. In particular, for the synaptic input and voltage equations the emulator uses round away from zero, which can be defined as

\[ x_{\text{round}} := \text{sign}(x) \cdot \lceil|x| \rceil. \]  

where \( \lceil \cdot \rceil \) is the ceiling function and \( \text{sign}(\cdot) \) the sign function.

### 2.3 Summary

We now have all of the pieces required to understand and emulate a spiking unit from Loihi. Evolving the differential equations for the current-based LIF model with the forward Euler method and using the appropriate rounding (see Section 2.2) and update schedule (see Section 4.1 and Appendix 7.2.1) is enough to exactly reproduce Loihi’s behavior. This procedure is summarized in Algorithm 1 and an exact match between Loihi and an implementation for a single unit in Brian is shown in Figure 1A. Please note that during the refractory period Loihi uses the voltage trace to count elapsed time (see Figure 1A2, Appendix 7.2.2), while in the emulator the voltage is simply clamped to zero.
Algorithm 1: Loihi single neuron emulator

**Result:** Simulate one Loihi unit with one input synapse for \( t_{\text{max}} \) time steps and read out state variables \((I, v)\) and spikes \((\sigma)\).

1. Define round away from zero
   \[ \text{rnd}(\cdot) := \text{sign}(\cdot)[1:] \]

2. Define input spike train
   \[ S_t = \{0, 1\} \forall t \in \mathbb{N} \mid t \leq t_{\text{max}} \]

3. Define synaptic weight
   \[ J := 2^{6+\Theta} \cdot \tilde{w}, \Theta \in [-8, 7], \tilde{w} \in [-256, 255] \]

4. Define threshold
   \[ v_{\text{th}} := v_{\text{mant}} \cdot 2^6, v_{\text{mant}} \in [0, 131071] \]

5. Define voltage and current decay
   \[ \tau_v = 2^{12}/\delta_v, \delta_v \in [0, 4096] \]
   \[ \tau_I = 2^{12}/\delta_I, \delta_I \in [0, 4096] \]

6. Initialise variables
   \[ I_t, v_t, \sigma_t = 0 \forall t \in \mathbb{N} \mid t \leq t_{\text{max}} \]

7. Loop over simulation steps
   
   for \( t \) from 1 to \( t_{\text{max}} \) do
     # Spike input
     \[ s \leftarrow S_t \]
     # Spike input
     \[ I_t \leftarrow I_{t-1} - \text{rnd}(\frac{1}{\tau_I}I_{t-1}) + J \cdot s \]
     # Update and read voltage
     \[ v_t \leftarrow v_{t-1} - \text{rnd}(\frac{1}{\tau_v}v_{t-1}) + I_t \]
     # Check threshold
     if \( v > v_{\text{th}} \) then
       # Read spike
       \[ \sigma_t \leftarrow 1 \]
       # Reset voltage
       \[ v_t \leftarrow 0 \]
     end
   end
Figure 1: A Input trace of a single synapse and voltage trace of a neuron. The emulator matches Loihi in both cases perfectly. Note that Loihi uses the voltage register to count refractory time, which results in a functionally irrelevant difference after a spike, e.g. time step 17 in A2 (see Appendix 7.2.2). B Network simulation with 400 excitatory (indices 100 – 500) and 100 inhibitory (indices 0 – 100) neurons. The network is driven by noise from an input population of 40 Poisson spike generators with a connection probability of 0.05. All spikes match exactly between the emulator and Loihi for all time steps. The figure shows the last 400 time steps from a simulation with 100 000 time steps.

3 Network and plasticity

We now have a working implementation of Loihi’s spiking unit. In the next step, we need to connect these units up into networks. And if the network should be able to learn online, connections between units should be plastic. In this section we review how weights are defined on Loihi and how learning rules are applied. This includes the calculation of pre- and post-synaptic traces. Based on this, we outline how these features are implemented in the emulator.

3.1 Synaptic weights

The synaptic weight consists of two parts, a weight mantissa $\tilde{w}$ and a weight exponent $\Theta$ and is of the form $\tilde{w} \cdot 2^{6+\Theta}$. However, in practice the calculation of the synaptic weight depends on bit shifts and its precision depends on a few parameters (see below). The weight exponent is a value between $-8$ and $7$ that scales the weight mantissa exponentially. Depending on the sign mode of the weight (excitatory, inhibitory, or mixed), the mantissa is an integer in the range $\tilde{w} \in [0, 255]$, $\tilde{w} \in [-255, 0]$, or $\tilde{w} \in [-256, 254]$, respectively. The possible values of the mantissa depend on the number of bits available for storing the weight and whether the sign mode is mixed or not. In particular, precision is defined as
2^{n_s}, with

\[ n_s = 8 - (n_{wb} - \sigma_{\text{mixed}}). \]  \hspace{1cm} (17)

This can intuitively be understood with a few examples. If the weight bits for the weight mantissa are set to the default value of \( n_{wb} = 8 \) bits, it can store 256 values between 0 and 255, i.e. the precision is then \( 2^8 - (8 - 0) = 2^0 = 1 \). If \( n_{wb} = 6 \) bits is chosen, we instead have a precision of \( 2^{8 - (6 - 0)} = 2^2 = 4 \) meaning there are 64 possible values for the weight mantissa, \( \tilde{w} \in \{0, 4, 8, 16, \ldots, 252\} \). If the sign mode is \textit{mixed}, i.e. \( \sigma_{\text{mixed}} = 1 \), one bit is used to store the sign, which reduces the precision. Mixed mode enables both positive and negative weights, with weight mantissa between \(-256 \) and 254. Assuming \( n_{wb} = 8 \) in mixed mode, precision is \( 2^8 - (8 - 1) = 2^1 = 2 \) and \( \tilde{w} \in \{-256, -254, \ldots, -4, -2, 0, 2, 4, \ldots, 254\} \).

### 3.1.1 Weight initialisation

While the user can define an arbitrary weight mantissa within the allowed range, during initialisation the value is rounded, given the precision, to the next possible value towards zero. This is achieved via bit shifting, that is the weight mantissa is shifted by

\[ \tilde{w}^{\text{shifted}} = (\tilde{w} \gg n_s) \ll n_s, \]  \hspace{1cm} (18)

where \( \gg \) and \( \ll \) are a right and left shift respectively. Afterwards the weight exponent is used to scale the weight according to

\[ J^{\text{scaled}} = \tilde{w}^{\text{shifted}} \cdot 2^{6 + \Theta}. \]  \hspace{1cm} (19)

This value cannot be greater than 21 bits and is clipped if it exceeds this limit. Note that this only happens in one case for \( \tilde{w} = -256 \) and \( \Theta = 7 \). Finally the scaled value \( J^{\text{scaled}} \) is shifted again according to

\[ J = (J^{\text{scaled}} \gg 6) \ll 6, \]  \hspace{1cm} (20)

where \( J \) is the final weight.

We provide a table with all 4096 possible weights depending on the mantissa and the exponent in a Jupyter notebook\(^4\). These values are provided for all three sign modes.

### 3.1.2 Plastic synapses

In the case of a static synapse, the initialised weight remains the same as long as the chip/emulator is running. Thus static synapses are fully described by the details above. For plastic synapses, the weight can change over time. This requires a method to ensure that changes to the weight adhere to its precision.

For plastic synapses, stochastic rounding is applied to the mantissa during each weight update. Whether the weight mantissa is rounded up or down depends on its proximity to the nearest possible values above and below, i.e.

\[ \text{RS}_{2^n_s}(x) = \begin{cases} 
\text{sign}(x) \cdot \lfloor |x| 2^{n_s/2} \rfloor, & \text{with probability } (2^{n_s} - (|x| - \lfloor |x| 2^{n_s/2} \rfloor)) / 2^{n_s} \\
\text{sign}(x) \cdot \lfloor |x| 2^{n_s} + 2^{n_s/2} \rfloor, & \text{with probability } (|x| - \lfloor |x| 2^{n_s/2} \rfloor) / 2^{n_s} 
\end{cases} \]  \hspace{1cm} (21)

where \( \lfloor \cdot \rfloor_{2^n_s} \) denotes rounding down to the nearest multiple of \( 2^n_s \). After the mantissa is rounded, it is scaled by the weight exponent and the right/left bit shifting is applied to the result to compute the actual weight \( J \). How this is realised in the emulator is shown in Code Listing 3.

To test that our implementation of the weight update for plastic synapses matches Loihi for each possible number of weight bits, we compared the progression of the weights over time for a simple learning rule. The analysis is described in detail in Appendix 7.3.

\(^4\)anonymized
### 3.2 Pre- and post-synaptic traces

Pre- and post-synaptic traces are used for defining learning rules. **Loihi** provides two pre-synaptic traces $x_1$, $x_2$ and three post-synaptic traces $y_1$, $y_2$, $y_3$. Pre-synaptic traces are increased by a constant value $\hat{x}_i$, for $i \in \{1, 2\}$, if the pre-synaptic neuron spikes. The post-synaptic traces are increased by $\hat{y}_j$ for $j \in \{1, 2, 3\}$, accordingly. So-called dependency factors are available, indicating events like $x_0 = 1$ if the pre-synaptic neuron spikes or $y_0 = 1$ if the post-synaptic neuron spikes. These factors can be combined with the trace variables by addition, subtraction, or multiplication.

A simple spike-time dependent plasticity (STDP) rule with an asymmetric learning window would, for example, look like $dw = x_1 \cdot y_0 - y_1 \cdot x_0$. This rule leads to a positive change in the weight ($dw > 0$) if the pre-synaptic neuron fires shortly before the post-synaptic neuron (i.e. positive trace $x_1 > 0$ when $y_0 = 1$) and to a negative change ($dw < 0$) if the post-synaptic neuron fires shortly before the pre-synaptic neuron (i.e. positive trace $y_1 > 0$ when $x_0 = 1$). Thus, the time window in which changes may occur depends on the shape of the traces (i.e. impulse strength $\hat{x}_i$, $\hat{y}_j$; and decay $\tau_{x_i}$, $\tau_{y_j}$, see below).

For a sequence of spikes $s[t] \in \{0, 1\}$, a trace is defined as

$$x_i[t] = \alpha \cdot x_i[t-1] + \hat{x}_i \cdot s[t],$$

(22)

where $\alpha$ is a decay factor (see Davies et al., 2018). This equation holds for presynaptic ($x_i$) and postsynaptic ($y_i$) traces. However, in practice, on **Loihi** one does not set $\alpha$ directly but instead decay time constants $\tau_{x_i}$ and $\tau_{y_j}$.

In the implementation of the emulator we again assume a first order approximation for synaptic traces, akin to synaptic input and voltage. Under this assumption for the exponential decay, in Equation 22 we replace $\alpha$ by

$$\alpha(\tau_{x_i}) = 1 - \frac{1}{\tau_{x_i}}.$$  

(23)

Using this approximation gives reasonable results across a number of different $\tau_{x_i}$ and $\tau_{y_j}$ values (see Figure 4). While this essentially suffices, it could be improved by introducing an additional parameter, e.g. $\beta$, and optimising $\alpha(\tau_{x_i}, \beta)$.

Note that we have integer precision again. But different from the round away from zero applied in the neuron model, here stochastic rounding is used. Since traces are positive values between 0 and 127 with precision 1, the definition above in Equation 21 simplifies to the following

$$RS_{1,\geq 0}(x) = \begin{cases} 
[x] & \text{with probability } 1 - (x - [x]) \\
[x] + 1 & \text{with probability } x - [x]
\end{cases}$$

(24)

Since this rounding procedure is probabilistic and the details of the random number generator are unknown, rounding introduces discrepancies when emulating **Loihi** on the computer. Further improvements are possible if more details of the chip’s rounding mechanism were to be considered.

### 3.3 Summary

At this point we are able to connect neurons with synapses and build networks of neurons (see Figure 1B). It was shown how the weights are handled, depending on the user defined number of weight bits or the sign mode. In addition, using the dynamics of the pre- and post synaptic traces, we can now define learning rules. Note that different from the neuron model, the synaptic traces cannot be reproduced exactly since the details of the random number generator, used for stochastic rounding, are unknown. However, Figure 2 shows that the synaptic traces emulated in **Brian** are very close to the original ones in **Loihi** and that the behavior of a standard asymmetric STDP rule can be reproduced with the emulator.
4 Loihi emulator based on Brian

Here we provide an overview over the emulator package and show some examples and results. This enables straightforward emulation of the basic features from Loihi as a sandbox for experimenters. Note that we have explicitly not included routing and mapping restrictions, like limitations for the number of neurons or the amount of synapses, as these depend on constraints such as the number of used Loihi chips.

4.1 The package

The emulator package is available on PyPI\(^5\) and can be installed using the pip package manager. The emulator does not provide all functionality of the Loihi chip and software, but the main important aspects. An overview over all provided features is given in Table 1 in the appendix. It contains six classes that extend the corresponding Brian classes. The classes are briefly introduced in the following. Further details can be taken from the code\(^6\).

Network

The LoihiNetwork class extends the Brian Network class. It provides the same attributes as the original Brian class. The main difference is that it initializes the default clock, the integration methods and updates the schedule when a Network instance is created. Note that it is necessary to make explicitly use of the LoihiNetwork. It is not possible to use Brian’s magic network.

Voltage and synaptic input are evolved with the forward Euler integration method, which was introduced in Section 2.2. Additionally a state updater was defined for the pre- and post-synaptic traces.

The default network update schedule for the computational order of the variables from Brian do not match the order of the computation on Loihi. The Brian update schedule is therefore altered when initialising the LoihiNetwork, more details are given in Appendix 7.2.1.

Neuron group

The LoihiNeuronGroup extends Brian’s NeuronGroup class. Parameters of the LoihiNeuronGroup class are mostly different from the Brian class and are related to Loihi. When an instance is created, the given parameters are first checked to match requirements from Loihi. Finally, the differential equations to describe the neural system are shown in Code Listing 1. Since Brian does not provide a round away from zero functionality, we need to define it manually as an equation.

Synapses

The LoihiSynapses class extends the Synapses class from Brian. Again, most of the Brian parameters are not supported and instead Loihi parameters are available. When instantiating a LoihiSynapses object, the needed pre- and post-synaptic traces are included as equations (shown in Code Listing 2) as theoretically introduced in Section 3.2. Moreover, it is verified that the defined learning rule matches the

---

\(^5\)https://pypi.org/project/brian2-loihi/
\(^6\)anonymized
lif_equations = '''
    rnd_v = sign(v) * ceil(abs(v * tau_v)) : 1
    rnd_I = sign(I) * ceil(abs(I * tau_I)) : 1
    dv / dt = - rnd_v / ms + I / ms: 1 (unless refractory)
    dI / dt = - rnd_I / ms : 1
'''

Code Listing 1: Neuron model equations of the voltage and the synaptic input for Brian. It contains a round away from zero rounding.

x1decay_equations = '''
    x1_new = x1 * (1 - (1.0 / tau_x1)) : 1
    x1_int = int(x1_new) : 1
    x1_frac = x1_new - x1_int : 1
    x1_add_or_not = int(x1_frac > rand()) : 1 (constant over dt)
    x1_rnd = x1_int + x1_add_or_not : 1
    dx1 / dt = x1_rnd / ms : 1 (clock-driven)
'''

Code Listing 2: Synaptic decay equation for Brian. Only the decay for x1 is shown, the decay for x2, y1, y2, y3 is applied analogously. It contains an approximation of the exponential decay and stochastic rounding.

available variables and operations supported by Loihi. The equations for the weight update is shown in Code Listing 3.

Since we have no access to the underlying mechanism and we cannot reproduce the pseudo-stochastic mechanisms exactly, we have to find a stochastic rounding that matches Loihi in distribution. Note that on Loihi the same network configuration leads to reproducible results (i.e. same rounding). Thus to compare the behavior of Loihi and the emulator, we simulate over a number of network settings and compare the distribution of the traces. Figure 2B shows the match between the distributions. Note that with this, our implementation is always slightly different from the Loihi simulation, due to slight differences in rounding. In Figure 2C we show that these variations are constant and not diverging. In addition, Figure 2D shows that the principle behavior of a learning rule is preserved.

State monitor & Spike monitor

The LoihiStateMonitor class extends the StateMonitor class from Brian, while the LoihiSpikeMonitor class extends the SpikeMonitor class. Both classes support the most important parameters from their subclasses and update the schedule for the timing of the probes. This schedule update avoids shifts in the monitored variables, compared to Loihi.

Spike generator group

The LoihiSpikeGeneratorGroup extends the SpikeGeneratorGroup class from Brian. This class only reduces the available parameters to avoid that users unintentionally change variables which would cause an unwanted emulation behavior.
weight_equations = `'`

```plaintext
u0 = 1 : 1
u1 = int(t/ms % 2**1 == 0) : 1
...
```

```plaintext
u9 = int(t/ms % 2**9 == 0) : 1
```

```plaintext
dw_rounded = int(sign(dw)*ceil(abs(dw))) : 1
quotient = int(dw_rounded / precision) : 1
remainder = abs(dw_rounded) % precision : 1
prob = remainder / precision : 1
add_or_not = sign(dw_rounded) + int(prob > rand()) : 1 (constant over dt)
```

```plaintext
dw_rounded_to_precision = (quotient + add_or_not) * precision : 1
w_updated = w * dw_rounded_to_precision : 1
w_clipped = clip(w_updated, w_low, w_high) : 1
```

```plaintext
dw/dt = w_clipped / ms : 1 (clock-driven)
```

```plaintext
w_act_scaled = w_clipped * 2**(6 + w_exp) : 1
w_act_scaled_shifted = int(floor(w_act_scaled / 2**6)) * 2**6 : 1
w_act_clipped = clip(w_act_scaled_shifted, -limit, limit) : 1
```

```plaintext
dx0/dt = 0 / ms : 1 (clock-driven)
dy0/dt = 0 / ms : 1 (clock-driven)
```

```plaintext
`
```

**Code Listing 3:** Weight equations for Brian. The first part creates variables that allow terms of the plasticity rule to be evaluated only at the $2^k$ time step. $dw$ contains the user defined learning rule. The updated weight mantissa is adapted depending on the number of weight bits, which determines the precision. The weight mantissa is rounded with stochastic rounding. After clipping, the weight mantissa is updated and the actual weight is calculated.

### 4.2 Results

To demonstrate that the Loihi emulator works as expected, we provide three examples covering a single neuron, a recurrently connected spiking neural network, and the application of a learning rule. All three examples are available as jupyter notebooks.

#### Neuron model

In a first test, we simulated a single neuron. The neuron receives randomly timed excitatory and inhibitory input spikes. Figure 1A1 shows the synaptic responses induced by the input spikes for the simulation using the Loihi chip and the Brian emulator. The corresponding voltage traces are shown in Figure 1A2. As expected, the synaptic input as well as the voltage match perfectly between both hardware types.

#### Network

In a second approach we applied a recurrently connected network of 400 excitatory and 100 inhibitory neurons with log-normal weights. The network gets noisy background input from 40 Poisson generators that are connected to the network with a probability of 0.65. As already shown by others, this setup leads to a highly chaotic behavior (Brunel, 2000; London et al., 2010; Sompolinsky et al., 1988; Van Vreeswijk & Sompolinsky, 1996). Despite the chaotic dynamics, spikes, voltages and synaptic inputs match perfectly.
Figure 2: Comparing a STDP learning rule performed with the emulator and with Loihi. A Sketch showing the setup. B Synaptic trace for many trials showing the arithmetic mean and standard deviation. The inset shows the same data in a logarithmic scale. Note that every data point smaller than $10^0$ shows the probability of rounding values between 0 and 1 up or down. C Relative difference $|\tilde{w}_L - \tilde{w}_B|/\tilde{w}_{\text{max}}$ for the plastic weight between the emulator, $\tilde{w}_B$, and the Loihi implementation, $\tilde{w}_L$, for 50 simulations, $\tilde{w}_{\text{max}} = 255$. D STDP weight change in respect to pre- and post-synaptic spike times, data shown for time steps $0 - 2000$ for visualisation purposes.

for all neurons and over the whole time. The spiking pattern of the network is shown in Figure 1B. All yellow (Brian) and blue (Loihi) dots match perfectly.

Learning

In the last experiment, we applied a simple STDP learning rule, as introduced in Equation 25, at a single plastic synapse. The experiment is sketched in Figure 2A. One spike generator, denoted input, has a plastic connection to a neuron with a very low weight ($\tilde{w} = 128, \Theta = -6$), such that it has a negligible effect on the post-synaptic neuron. Another spike generator, denoted noise, has a large but static weight ($\tilde{w} = 254, \Theta = 0$) to reliably induce post-synaptic spikes. Figure 2B compares the distribution of traces between the emulator and Loihi. For this 400 trials were simulated.

We chose an asymmetric learning window for the STDP rule. The learning rule uses one pre-synaptic trace $x_1 (\hat{x}_1 = 120, \tau_{x_1} = 8)$ and one post-synaptic trace $y_1 (\hat{y}_1 = 120, \tau_{y_1} = 8)$. In addition the dependency factors $x_0 \in 0, 1$ and $y_0 \in 0, 1$ are used, which indicate a pre- and post-synaptic spike respectively. Using these components, the learning rule is defined as

$$dw = 2^{-2} \cdot x_1 \cdot y_0 - 2^{-2} \cdot x_0 \cdot y_1.$$  

(25)
Due to the stochastic rounding of the traces, differences in the weight changes occur, which are shown in Figure 2C. Fortunately, the differences in the weight changes remain on a constant level and do not diverge, even over long simulation times, e.g. 100,000 steps. Despite these variations, the STDP learning window of the emulator reproduces the behavior of the Loihi learning window, as shown in Figure 2D.

5 Discussion

This study was motivated by two goals. We hope to simplify the transfer of models to Loihi and therefore developed a Loihi emulator for Brian, featuring many functionalities of the Loihi chip. In the process of developing the emulator, we aimed to provide a deeper understanding of the functionality of the neuromorphic research chip Loihi by analysing its neuron and synapse model, as well as synaptic plasticity.

We hope that the analysis of Loihi’s spiking units has provided some insight into how Loihi computes. With the numerical integration method, numerical precision and related rounding method, as well as the update schedule, we were able to walk from the LIF neuron model down to the computations performed. For neurons and networks without plasticity we are able to emulate Loihi without error. Analysing and implementing synaptic plasticity showed that, due to stochastic rounding, it is not possible to exactly replicate trial by trial behavior when it comes to learning. However, on average the weight changes induced by a learning rule are preserved.

The main benefit of the Brian2Loihi emulator lies in lowering the hurdle for the experimenter. Especially in neuroscience, many scientists are accustomed to neuron simulators and in particular Brian is widely used. The emulator can be used for simple and fast prototyping, making a deep dive into new software frameworks and hardware systems unnecessary. In addition, hardware specific complications, like distributing neurons to cores, or constraints like potential limits on the number of available neurons or synapses, or on the speed or size of read-out, do not occur in the emulator. While this will surely improve with new generations of hardware and software in the upcoming years, they can already be ignored by using the emulator.

At this point it is important to note that not all Loihi features are included in the emulator, yet. In particular, the homeostasis mechanism, rewards, and tags for the learning rule are not included. In Table 1 we provide a comparison of all functionalities from Loihi with those available in the current state of the emulator. Development of this emulator is an open source project and we expect improvements and additions with time.

An important vision for the future is to flexibly connect front-end development environments (e.g. Brian, NEST, Keras, TensorFlow) with various back-ends, like neuromorphic platforms (e.g. Loihi, SpiNNaker, BrainScaleS, Dynap-SE) or emulators for these platforms. PyNN (Davison et al., 2009) is such an approach to unify different front-ends and back-ends in a more general way. Nengo (Bekolay et al., 2014), as another approach, does not provide the use of other simulators, but allows several back-ends and focuses on higher level applications (DeWolf et al., 2020). NxTF (Rueckauer et al., 2021) is an API and compiler aimed at simplifying the efficient deployment of deep convolutional spiking neural networks on Loihi using an interface derived from Keras. We think that ideally, one could continue to work in their preferred front-end environment while a package maps their code to existing chips or computer-based emulators of these chips. We expect an interface along these lines will play an important role in the future of neuromorphic computing and want to contribute to this development with our Brian2Loihi emulator.

At least for now, with an emulator at hand, it is easier to prototype network models and assess whether
an implementation on Loihi is worth considering. When getting started with neuromorphic hardware, to e.g. scale up models or speed up simulations, researchers familiar with Brian can directly deploy models prepared with the emulator. We hope that with this, others may find a smooth entry into the quickly emerging field of neuromorphic computing.

6 Acknowledgements

The work received funds by the Intel Corporation via a gift without restrictions. ABL currently holds a Natural Sciences and Engineering Research Council of Canada PGSD-3 scholarship. We would like to thank Jonas Neuhöfer, Sebastian Schmitt, Andreas Wild, and Terrence C. Stewart for valuable discussions and input.
7 Appendix

7.1 Loihi neuron model

Computational units on Loihi communicate via spikes. They can be connected up to form networks, each unit both sending and receiving spikes from some subset of the other units. Like neurons in the brain, a unit emits a spike if its internal variable reaches a certain threshold. The spike is then transmitted to all units with a direct incoming connection from the one that spiked. This induces a change in the receiving units’ internal variable. At every time step, the internal variable of all units’ decays towards zero, counteracting any input received. And after spiking, the internal variable is reset to zero. In terms of the brain, each computational unit on Loihi implements a simple model of a spiking neuron, in particular a variant of the leaky integrate and fire neuron model, which is based on a simple resistor-capacitor (RC) circuit. Readers are encouraged to consult the first chapter of Gerstner et al. (2014) for a more detailed treatment.

7.1.1 Voltage

We refer to the standard leaky integrate and fire neuron, as it is defined in Gerstner et al. (2014). In this model, the difference in electric potential between the interior and the exterior of a neuron, the so-called membrane potential, evolves according to

$$\tau_v \frac{dv}{dt} = -[v(t) - v_{rest}] + RI(t),$$

(26)

where $v$ is the voltage across the membrane, $\tau_v$ is the membrane time constant of the neuron, $v_{rest}$ is the resting potential, $I$ is the input current and $R$ is the resistance of the membrane. Whenever the membrane potential reaches threshold $v^{th}_i$ it is reset to $v_{rest}$.

Davies et al. (2018) present the following variant of the standard LIF model which forms the basis for Loihi’s computational units

$$\frac{dv_i}{dt} = -\frac{1}{\tau_v}v_i(t) + I_i(t) - v^{th}_i \sigma_i(t),$$

(27)

where $v$ is the voltage across the membrane, $\tau_v$ is the time constant for voltage decay, $I$ is in this case an input variable, $v^{th}_i$ is the threshold voltage to spike, and $\sigma(t)$ indicates whether the neuron fired a spike at time $t$.

There are a few differences that are worth noting. In the Loihi variant, the resting potential is zero. The membrane time constant $\tau_v$ applies only to the voltage decay and not to the input variable $I$. In effect, the resistance and the time constant are implicit in the input variable $I$ as connection weight.

Further, resetting after a spike is included directly in the differential equation. The final term subtracts the threshold voltage $v^{th}_i$ at the time of a spike. This is a matter of notation and can be written as such, or with a separate reset condition $v_i \to 0$ applied at the time of each spike, as in Gerstner et al. (2014).

7.1.2 Derivation of synaptic response

To keep this paper self-contained, here we derive the synaptic response of a Loihi unit to an incoming spike train. For the reader’s convenience, we repeat the definition from Equation 3 in the main text here
and then with a few steps obtain the result from Equation 5.

**Definition.** The synaptic response is given by

\[
I_i(t) = \sum_j J_{ij}(\alpha_i * \sigma_j)(t) + I_i^{\text{bias}},
\]

(28)

where \(J_{ij}\) is the weight from unit \(j\) to \(i\), \(I_i^{\text{bias}}\) is a constant bias input, and the spike train \(\sigma_j\) of unit \(j\) is convolved with the synaptic filter impulse response \(\alpha_i\), given by

\[
\alpha_i(t) = \exp\left(-\frac{t}{\tau_i}\right) H(t),
\]

(29)

where \(\tau_i\) is the time constant of the synaptic response and \(H(t)\) the unit step function. Note we define \(\alpha_i(t)\) differently here than in Davies et al. (2018) (see Appendix 7.1.3 for details).

**Definition.** The unit step function \(H : \mathbb{R} \to \mathbb{R}\) is given by

\[
H(x) = \begin{cases} 
1 & , x \geq 0 \\
0 & , x < 0 
\end{cases}
\]

(30)

**Definition.** The Dirac delta \(\delta \in \mathcal{S}'(\mathbb{R})\), with \(\delta : \mathcal{S}(\mathbb{R}) \to \mathbb{C}\), \(\varphi \mapsto \langle \delta, \varphi \rangle\) where

\[
(\delta, \varphi) := \int_{-\infty}^{\infty} \delta(x)\varphi(x) \, dx := \varphi(0)
\]

(31)

for all Schwartz functions \(\varphi \in \mathcal{S}(\mathbb{R})\). Here we extend the definition such that \(\delta : f \to f(0)\) for arbitrary, everywhere-defined \(f : \mathbb{R} \to \mathbb{R}\).

**Definition.** We define the translation of \(\delta\) by \(a\), denoted \(\delta_a\), as the distribution \(\tau_a\delta : \mathcal{S}(\mathbb{R}) \to \mathbb{C}\) with

\[
\tau_a\delta(\varphi) := \langle \delta_a, \varphi \rangle = \int_{-\infty}^{\infty} \delta(x - a)\varphi(x) \, dx
\]

(32)

and again extend this notion to arbitrary, everywhere-defined \(f : \mathbb{R} \to \mathbb{R}\).

**Lemma 1.** (translation property) \(\tau_a\delta(f) = f(a)\), for \(a \in \mathbb{R}\) and \(f : \mathbb{R} \to \mathbb{R}\).

**Proof.** Let \(f : \mathbb{R} \to \mathbb{R}\). Then

\[
\tau_a\delta(f) = \int_{-\infty}^{\infty} \delta(x - a)f(x) \, dx = \int_{-\infty}^{\infty} \delta(x)f(x + a) \, dx = f(0 + a) = f(a)
\]

(33) \(\blacksquare\)

**Corollary 1.** As a sum of Dirac deltas, \(\sigma_i\) can be understood as the following linear functional

\[
\sigma_i := \sum_k \tau_{t_{i,k}} \delta : \varphi \mapsto \mathbb{C},
\]

(34)

with

\[
(\sigma_i, \varphi) := \sum_k \delta_{t_{i,k}}(\varphi) = \sum_k \delta_{t_{i,k}}(\varphi) = \sum_k \varphi(t_{i,k}), \quad \varphi \in \mathcal{S}(\mathbb{R}),
\]

(35)

and again we extend this notion to the space of tempered distributions to \(\sigma_i\) for arbitrary, everywhere-defined \(f\).

**Definition.** The convolution between the Dirac delta distribution and a function is to be understood in the following sense

\[
(\delta * f)(x) := \langle \delta, \tau_x f \rangle = \int_{-\infty}^{\infty} \delta(y)f(x - y) \, dy = \int_{-\infty}^{\infty} \delta(x - y)f(y) \, dy
\]

(36)
where $\tilde{f}(x) = f(-x)$.

**Lemma 2.** $(\delta * f)(x) = f(x)$.

**Proof.** Using $\delta(x) = \delta(-x)$ (E) and the translation property of the Dirac delta function (T) from Lemma 1 we have

\[
(\delta * f)(x) := \int_{-\infty}^{\infty} \delta(x-y)f(y)\,dy = \int_{-\infty}^{\infty} \delta(y-x)f(y)\,dy = \tau_x \delta(f) = f(x).
\] (37)

\[\blacksquare\]

**Claim.** The synaptic input $I_i(t)$ for unit $i$ is given by

\[I_i(t) = \sum_j J_{ij} \sum_k \exp \left( \frac{t_{j,k} - t}{\tau_I} \right) H(t - t_{j,k}) + I_i^{\text{bias}}.\] (44)

**Proof.** Applying the definition of convolution (D), linearity of the integral operator (L), the translation property of the Dirac delta function (T), and using that $\delta(x) = \delta(-x)$ (E) we have

\[
(\alpha I * \sigma_j)(t) \overset{D}{=} \int_{-\infty}^{\infty} \alpha_I(s) \sigma_j(t - s)\,ds
\]
\[
= \int_{-\infty}^{\infty} \alpha_I(s) \sum_k \delta(t - t_{j,k} - s)\,ds
\]
\[
\overset{E}{=} \sum_k \int_{-\infty}^{\infty} \alpha_I(s) \delta(t - t_{j,k} - s)\,ds
\]
\[
\overset{L}{=} \sum_k \int_{-\infty}^{\infty} \alpha_I(s) \delta(s - (t - t_{j,k}))\,ds
\]
\[
\overset{T}{=} \sum_k \tau_t - t_{j,k} \delta(\alpha_I)
\]
\[
\overset{E}{=} \sum_k \alpha_I(t - t_{j,k})
\] (43)

With this, we can write the synaptic input (Equation 3) as

\[I_i(t) = \sum_j J_{ij} \sum_k \exp \left( \frac{t_{j,k} - t}{\tau_I} \right) H(t - t_{j,k}) + I_i^{\text{bias}}.\] (45)

\[\blacksquare\]

We see the input can be written as a sum of exponentially decaying functions with amplitude $J_{ij}$ beginning at the time of each spike $t_{j,k}$.

### 7.1.3 Definition of the synaptic filter impulse response

Davies et al. (2018) defined the *synaptic filter impulse response* as

\[\alpha_{I,\text{orig}}(t) = \frac{1}{\tau_I} \exp \left( -\frac{t}{\tau_I} \right) H(t).\] (46)

Note that we have omitted the factor of $1/\tau_I$ in our definition, in particular we defined

\[\alpha_I(t) = \exp \left( -\frac{t}{\tau_I} \right) H(t).\] (47)
We prefer this formulation as the results obtained match exactly with the Loihi documentation. If, however, the factor of $1/\tau_I$ is included, the factor is carried through to Equation 10. Namely it becomes

$$I[t] = I[t-1] \cdot (2^{12} - \delta_I) \cdot 2^{-12} + \frac{J}{\tau_I} \cdot s[t]$$

(48)

where we see there is an extra factor of $1/\tau_I$ multiplied by the weight $J$. The definition from Davies et al. (2018) and the NxSDK documentation can be reconciled by replacing this extra factor of $1/\tau_I$ with a static factor $2^{6}$ and then considering the weight to be $J = \tilde{w} \cdot 2^{6}$ instead of $J = \tilde{w} \cdot 2^{6+\Theta}$.

### 7.2 Miscellaneous implementational details

#### 7.2.1 Brian state update schedule

In Brian the network class is the main class of a simulation. All containing objects like neurons, synapses, monitors, poisson generators, are added to that network object. Each of these objects have a when attribute. The network class decides in which order containing objects are updated depending on their when attribute. For this decision a schedule is defined, given as a string list. The default schedule is ['start', 'groups', 'thresholds', 'synapses', 'resets', 'end'].

We observed that Loihi implements a schedule where first the synapses are updated and afterwards the neuron groups. In Brian the evaluation is performed in opposite order, which results in a shift between Loihi and the emulator. We therefore changed the Brian schedule to ['start', 'synapses', 'groups', 'thresholds', 'resets', 'end'], i.e. the synapse update is pulled in front of groups.

Additionally the time when the synaptic monitor is evaluated is different in Loihi. For the emulator, we also needed to adjust these. This is done by changing the monitors when flag from the default start to synapses for the synaptic input and all pre- and post-synaptic trace variables. For probing the voltage and weight the when attribute was changed to end. The same holds for probing spikes with the spike monitor. Moreover, the poisson generators when flag has to be changed from the default thresholds to start to ensure Poisson spikes are given at the beginning of the current time step and are propagated through the simulation schedule.

#### 7.2.2 Voltage memory used to count refractory time

Note that Loihi sets the voltage of a neuron to a non zero value if the neuron has spiked. The memory for storing the voltage is used for counting while the neuron is in refractory state. This causes a deviation between the emulator and Loihi for the voltage, which is only due to technical reasons and has no functional effect.
7.3 Plastic weight update with stochastic rounding

If the weight is updated by a learning rule, the weight mantissa needs to be updated according to the given precision, as described in Section 3.1.2. The precision is determined by the available number of bits, which can be chosen by the user, and in addition depends on the sign mode. To test the implementation in the emulator, we compared its behavior to Loihi for each possible number of weight bits. In particular, for an excitatory plastic synapse we increased the weight mantissa by one at each time step (via learning rule \( dw = u_0 \)) and measured the actual weight after the update (i.e. rounding and shifting). Our expectation was that for stochastic rounding to the nearest \( 2^{n_s} \), the average number of time steps required until a weight change takes place should be equal to \( 2^{n_s} \). This is because the probability of rounding up from a given weight mantissa, e.g. \( \tilde{w} := k \cdot 2^{n_s} \), when 1 is added can be calculated from Equation 21 as

\[
\frac{(|w| - |\tilde{w}| \cdot 2^{n_s})}{2^{n_s}} = \frac{((k \cdot 2^{n_s} + 1) + k \cdot 2^{n_s})}{k \cdot 2^{n_s}} = \frac{1}{2^{n_s}}.
\]

As expected, the results match Loihi’s behavior nicely, as seen in Figure 3, confirming the validity of our implementation.

![Figure 3: Distribution of the weight change for different number of weight bits. The weight mantissa is increased by 1 in every time step. Due to stochastic rounding, this change may then be rounded up or down. Shown is the distribution of the number of time steps until a weight change occurs. For each number of weight bits, 8000 weight changes were sampled for Loihi and the emulator. The emulator implementation matches Loihi well.](image-url)
7.4 Pre- and post-synaptic decay deviations

Figure 4: Deviations of the synaptic traces between Loihi and the emulator. A Synaptic traces for different synaptic time constants $\tau$. Averaged over 100 trials each. The inlay shows the traces in a logarithmic scale. Blue indicates the trace from Loihi, yellow the trace from the emulator. B Mean signed deviation for different synaptic time constants $\tau$ over 100 trials each. For low $\tau$ values, the emulator is slightly below the Loihi reference, whereas it lies slightly above the Loihi traces for higher values.
### 7.5 Emulator features

| Loihi                          | Emulator          |
|-------------------------------|-------------------|
| neurons                       |                   |
| current impulse/decay         | ✓                 |
| voltage impulse/decay         | ✓                 |
| bias input                    | (✓)               |
| homeostasis (threshold adaption) | -                |
| random noise for current      | -                 |
| random noise for voltage      | (✓)               |
| multi-compartment neurons     | (✓)               |
| connections                   |                   |
| weight mantissa/exponent      | ✓                 |
| weight precision              | ✓                 |
| synaptic delay                | ✓                 |
| box-synapse                   | -                 |
| learning                      |                   |
| presynaptic spike             | ✓                 |
| 1<sup>st</sup> presynaptic trace | ✓            |
| 2<sup>nd</sup> presynaptic trace | ✓         |
| postsynaptic spike            | ✓                 |
| 1<sup>st</sup> postsynaptic trace | ✓           |
| 2<sup>nd</sup> postsynaptic trace | ✓         |
| 3<sup>rd</sup> postsynaptic trace | ✓         |
| synaptic weight as variable   | ✓                 |
| reward spike                  | -                 |
| reward trace                  | -                 |
| tag                           | -                 |
| plastic synaptic delay        | -                 |
| learning epoch                | (✓)               |
| probes                        |                   |
| probe variables               | ✓                 |
| probing conditions            | (✓)               |

**Table 1:** Features of Loihi compared with the emulator (version 0.5.2). Check marks in brackets are not fully supported or can manually be included using core Brian functionality.
References

Bekolay, T., Bergstra, J., Hunsberger, E., DeWolf, T., Stewart, T., Rasmussen, D., Choo, X., Voelker, A., & Eliasmith, C. (2014). Nengo: A python tool for building large-scale functional brain models. *Frontiers in Neuroinformatics*, 7(48), 1–13. https://doi.org/10.3389/fninf.2013.00048

Bouvier, M., Valentin, A., Mesquida, T., Rummens, F., Reyboz, M., Vianello, E., & Beigne, E. (2019). Spiking neural networks hardware implementations and challenges: A survey. *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, 15(2), 1–35.

Brüderle, D., Petrovici, M. A., Vogginger, B., Ehrlich, M., Pfiefl, T., Milner, S., Grübl, A., Wendt, K., Müller, E., Schwartz, M.-O., et al. (2011). A comprehensive workflow for general-purpose neural modeling with highly configurable neuromorphic hardware systems. *Biological cybernetics*, 104(4), 263–296.

Brunel, N. (2000). Dynamics of networks of randomly connected excitatory and inhibitory spiking neurons. *Journal of Physiology-Paris*, 94(5-6), 445–463.

Davies, M., Srinivasa, N., Lin, T., Chinya, G., Cao, Y., Choday, S. H., Dimou, G., Joshi, P., Imam, N., Jain, S., Liao, Y., Lin, C., Lines, A., Liu, R., Mathaikutty, D., McCoy, S., Paul, A., Tse, J., Venkatakrishnan, G., ... Wang, H. (2018). Loihi: A neuromorphic manycore processor with on-chip learning. *IEEE Micro*, 38(1), 82–99. https://doi.org/10.1109/MM.2018.112130359

Davies, M., Wild, A., Orchard, G., Sandamirskaya, Y., Guerra, G. A. F., Joshi, P., Plank, P., & Risbod, S. R. (2021). Advancing neuromorphic computing with Loihi: A survey of results and outlook. *Proceedings of the IEEE*.

Davison, A. P., Brüderle, D., Eppler, J. M., Kremkow, J., Muller, E., Pecevski, D., Perrinet, L., & Yger, P. (2009). PyNN: a common interface for neuronal network simulators. *Frontiers in neuroinformatics*, 2, 1.

DeWolf, T., Jaworski, P., & Eliasmith, C. (2020). Nengo and low-power AI hardware for robust, embedded neurorobotics. *Frontiers in neurorobotics*, 14.

DeWolf, T., Stewart, T. C., Slotine, J.-J., & Eliasmith, C. (2016). A spiking neural model of adaptive arm control. *Proceedings of the Royal Society B: Biological Sciences*, 283(1843), 20162134.

Furber, S. (2016). Large-scale neuromorphic computing systems. *Journal of neural engineering*, 13(5), 051001.

Furber, S. B., Galluppi, F., Temple, S., & Plana, L. A. (2014). The spinnaker project. *Proceedings of the IEEE*, 102(5), 652–665.

Gerstner, W., Kistler, W. M., Naud, R., & Paninski, L. (2014). *Neuronal dynamics: From single neurons to networks and models of cognition*. Cambridge University Press.

Grüning, A., & Bohte, S. M. (2014). Spiking neural networks: Principles and challenges. *ESANN*.

Lin, C.-K., Wild, A., Chinya, G. N., Cao, Y., Davies, M., Lavery, D. M., & Wang, H. (2018). Programming spiking neural networks on Intel’s Loihi. *Computer*, 51(3), 52–61.

London, M., Roth, A., Beeren, L., Häusser, M., & Latham, P. E. (2010). Sensitivity to perturbations in vivo implies high noise and suggests rate coding in cortex. *Nature*, 466(7302), 123–127.

Luo, T., Wang, X., Qu, C., Lee, M. K. F., Tang, W. T., Wong, W.-F., & Goh, R. S. M. (2018). An FPGA-based hardware emulator for neuromorphic chip with RRAM. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 39(2), 438–450.

Michaelis, C. (2020). Pelenet: A reservoir computing framework for loihi. *arXiv preprint arXiv:2011.12338*.

Michaelis, C., Lehr, A. B., & Tetzlaff, C. (2020). Robust trajectory generation for robotic control on the neuromorphic research chip loihi. *Frontiers in neurorobotics*, 14.

Müller, E., Mauch, C., Spilger, P., Breitwieser, O. J., Klähn, J., Stöckel, D., Wunderlich, T., & Schemmel, J. (2020). Extending BrainScaleS OS for BrainScaleS-2. *arXiv preprint arXiv:2003.13750*.

23
Müller, E., Schmitt, S., Mauch, C., Billaudelle, S., Grübl, A., Güttler, M., Husmann, D., Ilmberger, J., Jeltsch, S., Kaiser, J., et al. (2020). The operating system of the neuromorphic BrainScaleS-1 system. arXiv preprint arXiv:2003.13749.

Petrovici, M. A., Vogginger, B., Müller, P., Breitwieser, O., Lundqvist, M., Muller, L., Ehrlich, M., Destexhe, A., Lansner, A., Schüffny, R., et al. (2014). Characterization and compensation of network-level anomalies in mixed-signal neuromorphic modeling platforms. PloS one, 9(10), e108590.

Pfeiffer, M., & Pfeil, T. (2018). Deep learning with spiking neurons: Opportunities and challenges. Frontiers in neuroscience, 12, 774.

Rajendran, B., Sebastian, A., Schmuker, M., Srinivasa, N., & Eleftheriou, E. (2019). Low-power neuromorphic hardware for signal processing applications: A review of architectural and system-level design approaches. IEEE Signal Processing Magazine, 36(6), 97–110.

Rhodes, O., Bogdan, P. A., Brenninkmeijer, C., Davidson, S., Fellows, D., Gait, A., Lester, D. R., Mikaitis, M., Plana, L. A., Rowley, A. G., et al. (2018). sPyNNaker: a software package for running PyNN simulations on SpiNNaker. Frontiers in neuroscience, 12, 816.

Rueckauer, B., Bybee, C., Goetttsche, R., Singh, Y., Mishra, J., & Wild, A. (2021). NxTF: An API and Compiler for Deep Spiking Neural Networks on Intel Loihi. arXiv preprint arXiv:2101.04261.

Sawada, J., Akopyan, F., Cassidy, A. S., Taba, B., Debole, M. V., Datta, P., Alvarez-Icaza, R., Amir, A., Arthur, J. V., Andreopoulos, A., et al. (2016). Truenorth ecosystem for brain-inspired computing: Scalable systems, software, and applications. SC’16: Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis, 130–141.

Schuman, C. D., Potok, T. E., Patton, R. M., Birdwell, J. D., Dean, M. E., Rose, G. S., & Plank, J. S. (2017). A survey of neuromorphic computing and neural networks in hardware. arXiv preprint arXiv:1705.06963.

Sompolinsky, H., Crisanti, A., & Sommers, H.-J. (1988). Chaos in random neural networks. Physical review letters, 61(3), 259.

Spilger, P., Müller, E., Emmel, A., Leibfried, A., Mauch, C., Pehle, C., Weis, J., Breitwieser, O., Billaudelle, S., Schmitt, S., et al. (2020). Hxtorch: Pytorch for brainscales-2. Iot streams for data-driven predictive maintenance and iot, edge, and mobile for embedded machine learning (pp. 189–200). Springer.

Stagsted, R., Vitale, A., Binz, J., Bonde Larsen, L., Sandamirskaya, Y., et al. (2020). Towards neuromorphic control: A spiking neural network based pid controller for uav.

Stimberg, M., Brette, R., & Goodman, D. F. (2019). Brian 2, an intuitive and efficient neural simulator (F. K. Skinner, Ed.). eLife, 8, e47314. https://doi.org/10.7554/eLife.47314

Thakur, C. S., Molin, J. L., Cauwenberghs, G., Indiveri, G., Kumar, K., Qiao, N., Schemmel, J., Wang, R., Chicca, E., Olson Hasler, J., et al. (2018). Large-scale neuromorphic spiking array processors: A quest to mimic the brain. Frontiers in neuroscience, 12, 891.

Valancius, S., Richter, E., Purdy, R., Rockowitz, K., Inouye, M., Mack, J., Kumbhare, N., Fair, K., Mixter, J., & Akoglu, A. (2020). FPGA based emulation environment for neuromorphic architectures. Van Vreeswijk, C., & Sompolinsky, H. (1996). Chaos in neuronal networks with balanced excitatory and inhibitory activity. Science, 274(5293), 1724–1726.

Young, A. R., Dean, M. E., Plank, J. S., & Rose, G. S. (2019). A review of spiking neuromorphic hardware communication systems. IEEE Access, 7, 135606–135620.