Performance Analysis of CMOS Circuits using Shielded Channel Dual Gate Stack Silicon on Nothing Junctionless Transistor

S.C. Wagaj, S.C. Patil

Abstract: In this paper it has been demonstrated that a shielded channel made by varying the side gate length in silicon-on-nothing junctionless transistor not only improves the short channel effect but also improve the performance of CMOS circuits of this device. The proposed device shielded channel dual gate stack silicon on nothing junctionless transistor (SCDGSSONJLT) drain induced barrier lowering (DIBL), cut-off frequency and subthreshold slope are improved by 20%, 39% and 20% respectively over the single material gate silicon on insulator junctionless transistor (SMG SOJLT). The proposed device CMOS inverter fall time $T_f$ (pS) and noise margin improves by 50% and 10% compare to shielded channel silicon on insulator junctionless transistor (SCSOJLT). It has been observed that circuit simulation of CMOS inverter, NAND and NOR of proposed device. The static power dissipation in the case of proposed SCDGSSONJLT device are reduced by 45%, 81% and 83% respectively over the SMGSOJLTJLT. Thus, significant improvement in DIBL, cut-off frequency, propagation delay and static power dissipation at low power supply voltage shows that the proposed device is more suitable for low power CMOS circuits.

Keywords: Shielded channel, junctionless transistor, dual gate stack, silicon on nothing, NAND gate, NOR gate.

I. INTRODUCTION

This International technological road map for semiconductor nanoscale with junction transistor’s shallow junction formation is very challenging in fabrication. Author colinge et.al have introduced junctionless transistor with uniform doping of source, channel and drain region [1]. The electric field perpendicular to the channel is significantly very low in junctionless transistor means mobility degradation is very less [2][3]. However, in junctionless transistor improving the current driving capability and gate control on channel potential are the challenges in this device. To overcome the short channel effect problem related with nanoscale junctionless transistor, double gate junctionless transistor can be considered [4][8].

It has been observed that bulk planner junctionless transistor [6] and junctionless double gate transistor are having low leakage current due to high channel doping. Moreover, due to high channel doping the mobility reduces due to ionization scattering and subsequently results in lower transconductance [6][7]. To overcome these challenges, many authors have introducing solutions such as junctionless nanowire transistor with a dual material gate [8], dual material gate junctionless transistor with high-k spacer [9], dual material gate silicon on nothing junctionless transistor [10], dual material double gate junctionless transistor considering fringing field [11], charge plasma based transistor with induced graded channel [12], gate-all-around junctionless transistor [13], non-uniformly doped symmetric double gate junctionless transistor [14], have been proposed. Among these junctionless transistor and architecture, dual material double gate junctionless transistor is best candidate for CMOS logic circuits [15]. However, it has been observed that

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dual material double gate with high-k spacer leads to an increase in gate capacitance and decrease in cut-off frequency [9]. Along with increases in device parameter fluctuations limits the scalability of junctionless transistors is the short channel effect. DIBL effect problem and excess parasitic capacitance arrive in SOI MOSFET due to charge accumulated in the thick buried layer. Air is insulating layer dielectric constant is unity. Buried oxide layer is removed by air and a structure is proposed as silicon-on-nothing MOSFET. Parasitic capacitance values between source/drain and substrate are induced in the silicon on nothing (SON) structure, and therefore a higher circuit speed can be expected with SON device [10]. Due to double layer gate stack design the output characteristics are improved. The drain bias variations and enhanced and the gate control on the channel charge is increased. The channel length of the proposed work 20nm [17], to reduce device gate leakage current and low off state current requirements the high-k dielectric is considered as an alternative to SiO₂. The concept of double layer gate stack and silicon on nothing has been studied on various device architecture such as dual material double gate layer stack SON MOSFET [18], dual material double gate SON MOSFET [19]. High-k gate stack properties in SON MOSFET, dual material double layer gate stack junctionless transistor [20]. Amin s and Sarin R.K. et.al demonstrate doping less dual material and gate stack architecture of junctionless transistor with high-k spacer and misaligned double gate JLT [21][22]. Although the concept of double layer gate stack SON has been widely studied on various device architectures, the effect of two layer gate stack and SON junctionless transistor for CMOS circuit has not been reported in earlier literature to the best of my knowledge. In our earlier work shielded channel junctionless transistor was proposed by reducing the short channel effects. Here the reduced DIBL effect was observed by varying side gate length and increased ON current due to workfunction difference of side gate [15].

In this paper, we demonstrate the CMOS circuit implementation using N and P channel SCDGGSSONJLT. A comparison of SCDGGSSONJLT with SMG SOI JLT and SCNOJLT is performed. Performance parameters such as static power dissipation, propagation delay, noise margin, rise and fall time of CMOS inverter, NAND and NOR are thoroughly investigated. For the simulation COGENDA TCAD tool is used.

This paper is arranged as follows. Section II consist device structure and their dimensions used for simulation are presented. The methodology is also highlighted. The result and discussion are given in section III. Conclusion is presented in section IV.

II. DEVICE STRUCTURE AND SIMULATION

Six different types of MOSFETs are used to implement CMOS circuits in this paper: namely, p- and n-channel SCDGGSSONJLT and p- and n-channel SMGSOIJLT and p- and n- channel SCNOIJLT. The schematic device structure of the SCDGGSSONJLT is shown in Figure 1. Performance analysis for CMOS inverters is done for three different channel length 20nm, 30nm and 40nm as per the international technology roadmap for semiconductors (ITRS) [19]. The parameters considered for the simulation are main gate 4.77eV, side gate 4.5eV, channel donor doping N_D=0.4x10¹⁸ cm⁻³, channel thickness t_s=10nm, gate oxide thickness 3nm (1nm SiO₂ and 2nm HfO₂), substrate doping N_A=1x10¹⁶ cm⁻³ respectively. A buried oxide thickness (t bó) is of 10nm (two oxide layer 2nm each and air thickness 6nm). Table 1 Device parameters used in simulation summarizes device parameters used in simulation.

Table1: Device parameters used in simulation

| Sr. No. | Parameters                       | Smgsoijlt | Scsoijlt | Scdgsoijlt |
|--------|---------------------------------|-----------|----------|------------|
| 1      | Main Channel length (nm)        | 20        | 20       | 20         |
| 2      | Side gate channel length (nm)   | -         | 10       | 10         |
| 3      | Work function of main gate (eV) | 4.9       | 4.9      | 4.9        |
| 4      | Work function of Side gate (eV) | -         | 4.17     | 4.17       |
| 5      | Channel thickness (nm)          | 10        | 10       | 10         |
| 6      | Channel doping density N (cm⁻³) | 0.4x10¹⁴  | 0.4x10¹⁴ | 0.4x10¹⁴   |
| 7      | Buried oxide (nm)               | 10        | 10       | SiO₂-2 Air-6 SiO₂-2 |
| 8      | P-sub (nm)                      | 20        | 20       | 20         |
| 9      | Gate oxide (nm)                 | 3         | 3        | HfO₂- 2 SiO₂-1 |
| 10     | Equivalent gate oxide thickness (nm) | 3     | 3        | 1.312      |

Genius uses the Kane’s model [23] to calculate the carrier generation by band-band tunnelling G_BB. The expression for the generation rate of for electrons and holes is as shown in equation 1

\[ G_{BB} = A_{BTBT} \cdot \frac{E^2}{E_g} \cdot \exp\left(\frac{-B_{BTBT} \cdot E_g^{3/2}}{E}\right) \]  

(1)

Where- E is the magnitude of electrical field; E_g is the bandgap of the material, A_BTTB and B_BTTB are empirical fitting parameters.

The default values for silicon are:

A_BTTB = 3.500000E+21
B_BTTB = 2.250000E+07

Lombardi Surface Mobility Model

The Lombardi mobility model [24] is an empirical mobility model shown in equation 2. The mobility model consist three different components as like surface roughnes, phonon scattering and doping dependent mobility model. Bulk mobility model in Lombardi mobility model is similar to masetti’s model.
\[
\mu_b = \mu_0 \exp\left( -\frac{P}{N_{tot}} \right) + \frac{\mu_{\text{max}} - \mu_0}{1 + \left( \frac{N_{tot}}{C_r} \right)^\alpha} - \frac{\mu_1}{1 + \left( \frac{C_r}{N_{tot}} \right)^\beta}
\]  

(2)

\[
\alpha = 0.680, \beta = 2.0, \xi = 2.5, \mu_0 = 52.2 \text{cm}^2/\text{V.s}, \\
\mu_1 = 1417 \text{cm}^2/\text{V.s}, C_s = 3.43 \times 10^{20} \text{cm}^{-3}, C_r = 9.68 \times 10^{16} \text{cm}^{-3}
\]

Carrier recombination, generation model, Fermi Dirac statics and impact ionization models and Lombardi mobility model in COGENDA TCAD. The quantum confinement model also have been incorporated in the simulation.

III. MODEL CALIBRATION

To ensure the validity of results, initially calibration of simulation models is done with reference to simulation result of MOSFET characteristics presented in [9] and n-channel JLT [5]. Thus the model characteristic is shown in Figure 2. and Figure 3. There is good agreement of COGENDA TCAD simulated and simulated result of different researchers is evident in these figures.

IV. RESULTS AND DISCUSSIONS

1.1 Performance comparison of SCDGSSONJLT and SCSOIJLT

SCDGSSONJLT’s subthreshold slope, drain induced barrier lowering (DIBL) and cut-off frequency are improved by 20%, 20% and 39% respectively over the single material gate silicon on insulator junctionless transistor (SMG SOI JLT). The \(I_D-V_{DS}\) characteristics are shown in Figure 4. Figure 4 compares the transfer characteristics of n channel and p channel SCDGSSONJLT with SCSOIJLT. The main reason for this improvement is, reduction of the effective gate oxide thickness of thickness of n type SCDGSSONJLT due to dual gate stack design (1.312nm). Output characteristics of n and p channel SCDGSSONJLT enhanced compare to SCSOIJLT at a fixed \(V_{SGS}=1.5\text{V}\), work function main gate=4.9eV, side gate=4.17eV, \(N_D=0.4 \times 10^{18} \text{cm}^{-3}\).

The electric field in the channel increase due to side gate biasing. Due to high electric field in the channel velocity of electron increases. The ON state current of SCSOIJLT is lower due to high doping density. In presence of the effect of using high-k/SiO\(_2\) gate-stack architecture on the transfer characteristics of SCDGSSONJLT and SCSOIJLT. The advantage of gate stack in terms of increased \(I_{ON}\). ON current of SCDGSSONJLT is 45.4\(\mu\text{A}\) and for SCSOIJLT is 14.1\(\mu\text{A}\) at \(V_{GS}=V_{DS}=1\text{V}\).

Figure 4. \(I_D\) vs \(V_{DS}\) characteristics of shielded channel JLT and proposed n-channel and p-channel SCDGSSONJLT at different \(V_{GS}\) values

The electric field in the channel increase due to side gate biasing. Due to high electric field in the channel velocity of electron increases. The ON state current of SCSOIJLT is lower due to high doping density. In presence of the effect of using high-k/SiO\(_2\) gate-stack architecture on the transfer characteristics of SCDGSSONJLT and SCSOIJLT. The advantage of gate stack in terms of increased \(I_{ON}\). ON current of SCDGSSONJLT is 45.4\(\mu\text{A}\) and for SCSOIJLT is 14.1\(\mu\text{A}\) at \(V_{GS}=V_{DS}=1\text{V}\).
Figure 5 shows that comparison of gate to drain capacitance $C_{gd}$ and gate capacitance $C_{gg}$ for n & p channel as a function of the gate-to-source voltage $V_{GS}$ between SCDGSSONJLT and SCSOIJLT. The gate capacitance $C_{gg}$ consist of the series combination of gate to channel capacitance and gate oxide capacitance.

Capacitance components $C_{gg}$, $C_{gs}$ and $C_{gd}$ have the relationship

$$C_{gg} = C_{gs} + C_{gd} \quad (3)$$

Gate oxide capacitance $C_{ox}$ can be evaluate as $^{[25]}$

$$C_{ox} = \frac{2\pi\varepsilon_{0}L_{g}}{\ln\left(1 + \frac{1}{R_{g}}\right)} \quad (4)$$

### Table 2: Delay and static power dissipation of inverters

| $L_G$ (nm) | $V_{DS} = 1V$ | $V_{DS} = 0.5V$ | $V_{DS} = 1V$ | $V_{DS} = 0.5V$ |
|-----------|---------------|-----------------|---------------|-----------------|
|           | $P_{static}$ (W) | $\tau_p$ (pS) | $P_{static}$ (W) | $\tau_p$ (pS) | $P_{static}$ (W) | $\tau_p$ (pS) | $P_{static}$ (W) | $\tau_p$ (pS) |
| 20        | 7.82x10^{-10} | 10 | 2.01x10^{-10} | 50 | 2.34x10^{-10} | 10 | 1.89x10^{-11} | 70 |
| 30        | 3.37x10^{-11} | 19 | 1.10x10^{-11} | 20 | 1.34x10^{-10} | 20 | 1.47x10^{-11} | 70 |
| 40        | 3.21x10^{-12} | 24 | 1.26x10^{-12} | 20 | 1.43x10^{-11} | 30 | 2.78x10^{-12} | 110 |

In transient response gate capacitance role is very important. It is observed that $C_{gd}$ for the SCDGSSONJLT are lower than that for SCSOIJLT. In linear region 0.275fF capacitance at $V_{GS}=0.08V$ and $V_{DS}=1V$ for SCDGSSONJLT and 0.117fF capacitance at $V_{GS}=0.08V$ and $V_{DS}=1V$ for SCSOIJLT and in saturation region 0.2fF capacitance at $V_{GS}=V_{DS}=1V$ of SCDGSSONJLT and 0.1fF capacitance at $V_{GS}=V_{DS}=1V$ of SCSOIJLT.

![Performance Analysis of CMOS Circuits using Shielded Channel Dual Gate Stack Silicon on Nothing Junctionless Transistor](image-url)
Figure 6. Comparison of static power dissipation of a) CMOS inverter, b) NAND gate and c) NOR gate circuit based on SCSOIJLT and proposed SCDGSSON junctionless transistor at various channel lengths.

All the capacitances are simulated as simulation mode AC sweep at a frequency of 1MHz. The SCDGSSONJLT has highest $C_{gg}$ compared with SCSOIJLT. This is attributed to high-k gate stack.

Figure 6 shows the plot between static power dissipation v/s physical gate length for $V_{DS}=1V$ (LHS) and $V_{DS}=0.5V$ (RHS) for inverter, NOR and NAND gate. The channel length consider for this simulation are 20nm, 30nm and 40nm and side gate length is 10nm which is constant for SCDGSSONJLT and SCSOIJLT. It has been observed that OFF current of MOSFET as well as static power dissipation decreases due to high-k gate stack.

Figure 7. Comparison of propagation delay of a) CMOS inverter, b) NAND gate and c) NOR gate circuit based on SCSOIJLT and proposed SCDGSSON junctionless transistor at various channel lengths.

Table 2 summarize CMOS inverter $P_{static}$ and $\tau_p$ values for $V_{DS}=0.5V$ and 1V. At $V_{DD}=0.5V$ and channel length 30nm, 40nm of SCDGSSONJLT inverter static power dissipations are 11pW.

| Side gate length (nm) | Rise Time, $T_r$ (pS) | Fall time $T_f$ (pS) | Improvement |
|-----------------------|-----------------------|----------------------|-------------|
| Inverter-1 SCDGSSONJLT | Inverter-2 SCSOIJLT | Improvement | Inverter-1 SCDGSSONJLT | Inverter-2 SCSOIJLT | Improvement |
| 10 | 105 | 150 | 30% | 95 | 180 | 47% |
| 20 | 105 | 130 | 19% | 130 | 110 | NIL |
| 30 | 140 | 119 | NIL | 100 | 118 | 15% |
| 40 | 140 | 140 | NIL | 190 | 130 | NIL |
1.26pW respectively, and SCSOIJLT inverter static power is 14.7pW. The static power dissipation of SCDGSSONJLT NOR gate is 3.55pW at $V_{DD}=0.5V$ and channel length of 40nm. The static power dissipation is 5.55pW for SCSOIJLT NOR gate. Static power dissipation of SCDGSSONJLT is minimum due to high phonon scattering below threshold voltage. Figure 7 shows the graph between propagation delay v/s physical channel length of SCDGSSONJLT and SCSOIJLT inverter, NAND and NOR gate. Propagation delay of SCDGSSONJLT is minimum as compared to SCDOIJLT. The delay time $\tau_d$ is defined as $\tau_d = (\tau_r + \tau_f)/2$, where the rise time $\tau_r$ and the fall time $\tau_f$ are extracted at $V_{out} = V_{dd}/2$. Device aspect ratio of SCDGSSONJLT device is 50 because channel length is 20nm and width is 1μm. When Channel length increases then propagation delay of inverter SCDGSSOJLT decreases and propagation delay of SCDGSSONJLT reduces by 20% as compared to SCSOIJLT. Propagation delay of SCSOIJLT is 110ps and proposed SCDGSSONJLT is 20ps at $V_{DS}=0.5V$ at channel length 40nm. SCDGSSONJLT NOR gate propagation delay is improved by 22%, 45% and 52% over the SCSOIJLT at channel length 20, 30 and 40nm respectively at $V_{DS}=0.5V$. Proposed SCDGSSONJLT is best candidate for low power CMOS circuit.

Figure 7 shows the graph between propagation delay v/s physical channel length of SCDGSSONJLT and SCSOIJLT inverter, NAND and NOR gate.

Figure 8. Transient response of CMOS inverter a) proposed SCDGSSONJLT b) SCSOIJLT at different side gate length.

Figure 8 a and b shows that the transient response of CMOS inverter SCDGSSONJLT and SCDOIJLT, it is useful for different side gate length calculation of propagation delay ($\tau_p$). Propagation delay indicates that time require by CMOS inverter to switch from OFF state to ON state. When propagation delay increases then lower will be the speed of device. It has been observed that SCDGSSONJLT exhibits smallest propagation delay of 20pS and SCSOIJLT has larger propagation delay that is 30pS. Voltage overshoot and undershoot effect leads in the transient response due to $C_{gd}$. In SCDOIJLT the undershoot peak arises due to the larger $C_{gd}$. Table 3 summarizes transient response inverters for different side gate lengths at $V_{DS}=1V$. SCDGSSONJLT and SCDOIJLT inverters rise time ($\tau_r$) and fall time ($\tau_f$) are calculated from transient characteristics at a different side gate channel length as shown in table 3.
Table-4 Device parameters for different channel length

| Channel length (nm) | $V_{DS}$(V) | SCDGSSONJLT n-type | SCDGSSONJLT p-type | SMGSOIJLT n-type | SMGSOIJLT p-type |
|---------------------|-------------|-------------------|-------------------|-----------------|-----------------|
|                     | $I_{ON}$(μA) | $V_T$(mV)        | $I_{ON}$(μA)      | $V_T$(mV)       | $I_{ON}$(μA)   | $V_T$(mV)       |
| 20                  | 1           | 45.4             | 410               | -               | -              | -               |
| 20                  | 0.05        | 11.7             | 680               | -               | -              | 51.3            | 380             | 23              | 1030            |
| 30                  | 1           | 78.4             | 430               | 17.1            | 1150           | 71.9            | 430             | 59.2            | 950             |
| 30                  | 0.05        | 36.6             | 550               | 4.8             | 1500           | 20.3            | 570             | 17.7            | 1040            |
| 40                  | 1           | 74.3             | 510               | 17              | 1140           | 79.4            | 350             | 54.7            | 980             |
| 40                  | 0.05        | 34.6             | 780               | 4.7             | 1210           | 31.9            | 400             | 12.9            | 1040            |

Channel potential shift away from main channel length. The current driving capability decreases then rise time increases from 10ps to 20ps and side gate length increases from 30nm to 40nm then drain current is remains constant means rise time remains constant. It is observe in $\tau_c$ for SCDGSSONJLT is lower than that of SCOSOI JLT at side gate length of 20, 30 and 40nm. It has been observed that rise time of both inverter remains constant. Figure 10 shows that voltage transfer curve (VTC) of CMOS inverter with SCDGSSONJLT is approximately similar to CMOS inverter with SCOSOI JLT having the same effective channel length i.e. L=20nm. Figure 10 shows that noise margin is calculated from butterfly graph of voltage transfer characteristics. The noise margin defined as maximum acceptable noise voltage in input that will not change the output voltage. It has been observed that the higher noise margin is in SCDGSSONJLT inverter as compared to SCOSOI JLT inverter at same effective channel length. Thus, SCDGSSONJLT CMOS circuit is more suitable for digital application such as memory design which is affect on read and write margin as compared with SCOSOI JLT CMOS circuit. Noise Margin at low state (NM_1) of SCDGSSONJLT is 0.39V and SCOSOI JLT is 0.34V. Noise Margin at high state (NM_2) of SCDGSSONJLT is 0.32V and SCOSOI JLT is 0.39V where NM_1 and NM_2 are calculated using following equation. Noise margin at channel length 30nm is 0.36V in high state and 0.37V in low state.

$NM_1 = V_{OH_{min}} - V_{IH_{min}}$

$NM_2 = V_{OL_{max}} - V_{IL_{max}}$

1.2 Comparison of SCDGSSONJLT and SMGSOIJLT

Multi material gate junctionless transistor improves the performance as compared to single material gate junctionless transistor. The different researchers demonstrates that multi material gate junctionless transistor is best candidate for CMOS design compare to single material gate junctionless transistor [9] [16]. In this section multi material gate SCDGSSONJLT’s CMOS circuits logical performance compared with single material gate junctionless transistor. Figure 9a shows a graph between subthreshold slope (SS) and physical gate length and Figure 9b shows the graph between DIBL and physical gate length for PMOS and NMOS. The DIBL is calculated from equation 5.

$$DIBL = \frac{V_{T_{LIN}} - V_{T_{SAT}}}{0.95}$$  \hspace{1cm} (5)

Where $V_{T_{LIN}}$ is threshold voltage at $V_{DS}=0.05$V and $V_{T_{SAT}}$ as a threshold voltage at $V_{DS}=1$V and the poly gate work function is 4.77eV and n poly gate is 4.1eV. It can be seen that due to side gate biasing, the DIBL and SS are reduced for SCDGSSONJLT as compared to SMG SOI JLT NMOS and PMOS devices. It has been observed that n-channel SCDGSSONJLT, the DIBL and SS are 40mV/V and 90 mV/decade and for SMGSOIJLT DIBL and SS are 50mV/V and 90mV/decade. The P-channel SCDGSSONJLT DIBL is -70mV/V and for SMGSOIJLT is -60mV/V at channel length 40nm. The sub-threshold current, $I_{sub}$ can be expressed in terms of $V_{T_{SAT}}$ and SS as shown in equation 6 [26].

$$I_{sub} = I_0 \times 10^{(V_{T_{SAT}}/SS)}$$  \hspace{1cm} (6)

$I_0$ is the drain current at $V_{GS}=V_{T_{LIN}}$ and SS can be expressed as...
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\[ SS = \frac{KT}{q} \ln \left(1 + \frac{1}{C_{ox1}} \frac{C_{si} \times C_{ox2}}{C_{si} + C_{ox2}}\right) \]  

Figure 10. VTCs of CMOS inverter a) SCSOI b) proposed SCDGSSON junctionless transistor

Figure 11. VTC for SCDGSSONJLT and SCSOIJLT for channel length 20nm

Figure 12. Comparison of propagation delay of CMOS inverter, NAND gate and NOR gate circuit based on SMG SOI and proposed SCDGSSON junctionless transistor at various channel length.

Figure 13. Comparison of static power dissipation of CMOS inverter, NAND gate and NOR gate circuit based on SMG SOI and proposed SCDGSSON junctionless transistor at various channel length.

\[ C_{ox1} \text{ is gate capacitance and } C_{ox2} \text{ is buried oxide capacitance and } C_{si} \text{ is body channel capacitance } C_{si} = \frac{\varepsilon_{si}}{t_{si}}. \]
Figure 13. shows the comparison of static power dissipation of CMOS NAND and NOR and Inverter gate circuits of SMG SOI JLT and proposed SCDGSSONJLT. The significant reduction in both $P_{\text{static}}$ and $\tau_p$ at minimum supply voltage observe the suitability of the proposed SCDGSSONJLT for low power CMOS logic circuits. At $V_{DS}=0.5V$, the SCDGSSONJLT inverter static power dissipation is 0.6nW and that of SMGSOIJLT inverter is 4.7nW. The SCDGSSONJLT NOR gate static power dissipation is 1.73 nW and that of SMGSOIJLT is 4nW at channel length 20nm. The static power dissipation of SCDGSSONJLT NAND gate is 1.35 nW, and that of SMGSOIJLT is 1.78nW at channel length 30nm. It has been observed that SCDGSSONJLT logic gate has good performance at low power. Table 4 summarize the ON current and threshold voltage of n and p channel of SCDGSSONJLT and SMGSOIJLT. It has been observed that 44% maximum ON current of SCDGSSONJLT as compared to SMGSOIJLT at channel length 30nm. Maximum $\sigma V_{th}$ of n channel SCDGSSONJLT is 370mV and SMGSOIJLT is 380mV. Average threshold voltage for SCDGSSONJLT is 560mV and it is suitable for low power device at $V_{DS}=0.5V$. For SMGSOIJLT average threshold voltage is 386mV. The hole density and electric field distribution in the middle of the channel when device operated in the off-state. When device is in the off-state, the channel region to be almost completely depleted, the bulk conduction of holes is reduced. The hole mobility hovers around 40 cm$^2$/Vs in p-type silicon for high doping concentration. The threshold voltage of p-type SCDGSSONJLT increases.

Where, $C_{gs}$ is gate capacitance and $g_m$ is transconductance. Due to higher current conductivity of SCDGSSONJLT at side gate length 40nm, the cut-off frequency $f_t$ is maximum than that of SMG SOI JLT and SCDGSSONJLT at side gate lengths of 10nm, 20nm and 30nm. The value of $f_t$ for SMGSOIJLT, SCDGSSONJLT are 300 GHz, 700 GHz respectively at $V_{GS}=0.6V$ and $V_{DS}=1V$ respectively. The value of SCDGSSONJLT increases due to dual gate stack gate material and in silicon on nothing technique no charge is accumulate in air. It has been observed that SCDGSSONJLT cut off frequency is improved as compared to SMGSOIJLT by 54%.

V. CONCLUSION

- The proposed device SCDGSSONJLT performs better than SMG SOI JLT. The subthreshold slope, DIBL, and cut-off frequency are improved by 20%, 20% and 39% respectively over the SMG SOI JLT.
- Three CMOS circuits have been proposed namely, Inverter, NAND and NOR gate
- The proposed device CMOS inverter fall time $T_f$ (pS) and noise margin are improved by 50% and 10% respectively, as compared to SMG SOI JLT
- The static power dissipation in proposed SCDGSSONJLT device is reduced by 45% , 81% and 83% respectively over the SMGSOIJLT at $V_{DS}=0.5V$.
- The improvement in Propagation delay of SCDGSSONJLT NOR gate at 20nm, 30nm and 40nm is 40%, 50% and 40% respectively, as compared to SCSONJLT.
- Although the lower gate capacitance in junctionless SCDGSSONJLT suppresses the undershoot effect in the circuit, the Cut off frequency of SCDGSSONJLT improves by 54% compared to SMGSOIJLT.

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