Simulink implementation of three-phase PWM rectifier using five-level cascaded H-bridge MLI configuration

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Abstract. Ability of multilevel inverters (MLI) to operate with matured medium power electronic devices has enhanced their prominence for active front converters in various applications such as drive control, battery energy storage systems and PV/Grid integrated systems. In short, Active front end (AFE) converters are regenerative rectifiers incorporated to, simultaneously regulate dc-link voltage and ensure unity power factor at source terminals. Realizing the significance of MLI based active front end converter, this paper presents Simulink implementation of MLI based active front end converter, using most popular classical MLI i.e., cascaded H-bridge. Imposing level shifted and phase shifted carrier arrangements, implementation PWM for CHB is demonstrated and MATLAB simulation results for both open loop and closed systems are presented.

1. Introduction
Rectifier converts ac voltage to dc voltage and it allows current to flow only in one direction. We can use diodes or thyristors in a rectifier circuit. For controlled energy flow we use thyristors instead of diodes in rectifier. Electrical system is negatively affected by the generation of harmonics which are produced by the converters and this can be reduced by using active filters, passive filters and by power factor correction method. IGBT (Insulated gate bipolar transistor) is used in power factor correction method as it is a controlled power switch. As the name PFC itself indicates improvement in power factor. Boost and Vienna rectifiers cannot perform regeneration. VSR’s-Voltage source rectifiers and CSR’s-Current source rectifiers are Active front ends which operates with a high power-factor. Regenerative rectifier circuit has source, rectifier circuit, capacitor, load and a feedback which helps for power regeneration. Regeneration is the major requirement for cranes, downhill conveyors etc., as they need reversal of energy flow during the operation. These are two regenerative rectifiers and it is nothing but the inverter working with reverse power flow. Multilevel inverter is a device which produces desired output voltage level from the multiple input dc voltages and finds its application in static VAR generation, flexible ac transmission systems, adjustable speed drives. This paper further
explains the concept of PWM rectifier and further presents its control and implementation with five-level cascaded H-bridge multilevel inverter.

2. PWM Regenerative Rectifier

For the control of dc-link voltage in 3-phase VSR’s we require a feedback control loop. The difference between \( V_o \) and \( V_{oref} \) is named as error signal “e”. The error signal “e” should generate a sinusoidal waveform with the same frequency as that of the mains supply and this error signal is used to produce Pulse width modulated pattern and controls rectifier in two different ways. They are Voltage source-voltage controlled PWM rectifier and Voltage source-current controlled PWM rectifier. Among these the more stable one is Voltage source-current controlled PWM rectifier and the circuit diagram of it is as shown in the figure1.

![Voltage source-current controlled PWM rectifier](image)

**Figure 1.** Voltage source-current controlled PWM rectifier.

Instantaneous phase currents are forced to form a sinusoidal reference by multiplying I with a sinusoidal function which is of same phase and frequency. Magnitude of current reference template, \( I^* = G_c e = G_c (V_{oref}-V_o) \). The controller \( G_c \) may be P, PI or other controller. Feedback control loop can produce instability on the voltage \( V_o \) and that can be avoided by following the relation given below and this should be followed during the design of the rectifier.

\[
\Gamma \leq \left( \frac{C \cdot V_o}{3K_v L_s} \right) \\
\Gamma \leq \left( \frac{K_p V_x \cos \phi}{2 R K_i + L_s K_i} \right)
\]

Where

- \( C = \) value of dc-link capacitor
- \( V_o = \) value of dc-link voltage
- \( V_x = \) value of rms voltage supply
- \( R = \) value of resistance at input side
- \( L = \) value of inductance at input side
- \( \cos \phi = \) value of input power factor
- \( \Gamma = \) value of input current
- \( K_p = \) value of proportional gain
- \( K_i = \) value of integral gain

Dc capacitor voltage will be equal to \( V_{oref} \) of rectifier for all load conditions when these two stability limits are satisfied. Power flows from ac side to dc side in rectifier and power flows from dc side to ac side in inverter. This method of giving dc-link voltage as reference command and finally extracting switching pulses to control the converter is called as voltage-oriented control (VOC).

This paper presents the importance of PWM Regenerative rectifiers which can also deliver the energy from line side to supply side. PWM regenerative rectifiers improves power factor and reduces input
harmonics. Importance is given to VSR’s and CSR’s which range power from a few kilowatts to megawatts. Many of the applications need input supply with reduced harmonics which gives efficient output. PWM regenerative rectifier operates in closed loop while multilevel inverter operates in open loop. Multilevel inverter is preferable than two level inverters because of its reduced harmonic distortion. The outcomes of regenerative rectifiers are improvement of power factor, reduced harmonics, reduced reactive components. The outcome of multilevel inverter is reduction in total harmonic distortion.

3. Multilevel inverters
Inverter converts fixed dc voltage into ac voltage with variable magnitude and frequency. We use two-level and multilevel inverters for high power medium voltage applications. Pulse width modulation is used in inverters to reduce harmonic content in output voltage, which compares reference(sinusoidal) wave and carrier(triangular) wave. A pulse is generated when carrier wave is less than reference wave. We prefer multilevel inverter than two-level inverter for high power medium voltage applications because of reduced device rating, minimum harmonic distortion and better voltage waveform [2]. The most popular Classical Multilevel inverters (MLI’s) are [1-7]:
1. Diode clamped MLI
2. Flying capacitors MLI
3. Cascaded H-bridge MLI

3.1. Cascaded H-Bridge Multilevel Inverter
The most popular inverter used for high power medium voltage drives is CHB multilevel inverter. CHB multilevel inverter requires isolated dc supplies for each h-bridge and each h-bridge consists of four MOSFET switches with anti-parallel diodes. CHB MLI is the combination of many H-bridge cells as shown in the figure2.

![Figure2. Three-phase five-level CHB inverter.](image-url)
Further, the operation of CHB and its corresponding switching states including redundancies is shown in Table 1.

**Table 1.** Operating states of five-level CHB inverter.

| Output Voltage | Switching State |
|----------------|-----------------|
| $v_{AN}$       | $S_{11}$ | $S_{31}$ | $S_{12}$ | $S_{32}$ | $v_{H1}$ | $v_{H2}$ |
| $2E$           | 1       | 0       | 1       | 0       | $E$     | $E$      |
| $E$            | 1       | 0       | 0       | 0       | $E$     | 0        |
|                | 1       | 1       | 1       | 0       | 0       | $E$      |
|                | 0       | 0       | 1       | 0       | 0       | $E$      |
| 0              | 0       | 0       | 0       | 0       | 0       | 0        |
| $-E$           | 0       | 1       | 1       | 1       | $E$    | $-E$     |
|                | 1       | 1       | 0       | 0       | 0       | 0        |
|                | 1       | 1       | 1       | 0       | 0       | 0        |
|                | 1       | 0       | 0       | 1       | $-E$   | $E$      |
|                | 0       | 1       | 1       | 0       | $E$    | $-E$     |
| $-2E$          | 0       | 1       | 0       | 1       | $-E$   | $-E$     |

Carrier based PWM schemes in CHB MLI are

1. Phase-shifted PWM
2. Level-shifted PWM

**Phase-shifted PWM:** In a phase shifted PWM we require (m-1) triangular carriers for ‘m’ voltage levels. For example, for five-level inverter which have five voltage levels we require 4 triangular carriers. We need a transportation delay for phase shifting of carrier waves while performing MATLAB simulation.

The transportation delay angle is calculated as

$\alpha = 1 / (4 \times \text{switching frequency})$

The following table shows respective output voltages when respective switches conducts.

**Output voltage, $v_{AN} = v_{H1} - v_{H2}$**

Each triangular wave should have same amplitude and frequency and the phase shift between any two adjacent carrier waves is given as $\mu = 360\text{deg}/(m-1)$. Phase shifted PWM for cascaded h-bridge inverter is as shown in the Figure 3(a).

**Level-shifted PWM:** Level shifted PWM can be achieved by any of the dispositions. There are 3 types of dispositions namely In-phase disposition (IPD), Alternative phase opposite disposition (APOD) and phase opposite disposition (POD). We will get same output for any of these three dispositions. Level shifted PWM for CHB inverter is as shown in the figure 3(b) and 3(c).

The sinusoidal reference wave and carrier wave are compared and given to relational operator and that is connected to switch. The switching sequence must form U-shape for both types of carrier
modulations. Device switching frequency and device conduction period is same for all devices in case of phase shifted modulation.
Figure 3. (a) Phase shifted PWM (b) Level shifted PWM & (c) Types of phase dispositions in level shifted PWM.

While in level shifted modulation both conduction period and switching frequency will be different. Line to line voltage total harmonic distortion is good in phase shifted PWM and it is better in level shifted PWM. Imposing a carrier frequency of 2kHz, open loop performance of phase voltage of five-level CHB obtained using PSPWM and LSPWM are shown in figure 4(a) and (b).

Figure 4. Phase voltage Performance of Five-level CHB with (a) PSPWM (b) LSPWM.

4. CHB based active rectifier: simulation results

Simulation results are obtained imposing VOC. However, as the dc-link involves two capacitors phase, cluster and individual voltage balancing is used. Individual voltage balancing controller ensures
that each capacitor tracks its reference voltage and cluster voltage balancer, minimizes the difference in dc-link voltage between capacitors of each phase. Further the output of cluster and individual voltage balancing controller are added to the current template generate from the output current controller or outer voltage loop. The Simulink implementation of the controller for phase-a is shown in figure-5, Where ‘n’ is number cascaded modules, Vdc is the reference the dc link voltage of each dc-link capacitor, Ia is the actual (measured) current of phase-a, Vdc1a and Vdc2a are the sensed instantaneous voltage of the capacitors in dc-link phase-a of five-level cascaded H-bridge MLI [4-5].

![Figure 5. Extraction of modulating signal (for phase-a).](image)

**Table 2.** Shows the simulation parameters.

| Parameter                  | Value  |
|----------------------------|--------|
| Phase-voltage (peak)       | 155 V  |
| Supply frequency           | 50 Hz  |
| Coupling inductance (Lac)  | 5 mH   |
| dc-link capacitance (C)    | 3000 µf|
| Sample time (Ts)           | 5e-6 sec|
| Reference voltage for each dc-link | 100 V |
| Switching frequency (fsw)  | 2 kHz. |

| PI Parameters              | Kp     | Ki    |
|----------------------------|--------|-------|
| Kp and Ki values           |        |
| Inner loop                 | 50     | 1     |
| outer loop                 | 20     | 2     |
|                            | 0.5    | 25    |

However, it is to be noted that total dc-link voltage in each phase can never be less than the supply phase peak voltage. Thus, the modulation index (ma) of the converter can never be greater than unity and can be defined as

\[ ma = \frac{V_m}{n*V_{dc}} \]

where \( V_m \) = supply phase peak, \( n \) = dc-link capacitors per phase and \( V_{dc} \) = reference dc-link voltage for each capacitor. Further, Imposing the simulation parameters given in Table2, the obtained simulation results are presented in figure 6, 7 and 8.

Results presented in figure 6, 7 and 8 prove the ability of CHB to operate as active rectifier, regulating dc-link voltages. It is to be noted that results are extracted considering PSPWM technique. The extraction of unity power factor and regulation of dc-link voltage of capacitors to the
reference voltage validate the satisfactory performance of the developed five-level CHB based active rectifier.

**Figure 6.** Source voltages, source currents, UPF.

**Figure 7.** DC-link voltage regulation.
Figure 8. Output voltage of CHB in closed loop (a) Five-level ph-voltage (b) Nine-level line-voltage.

5. Conclusion

This paper promoted the significance of MLI based active rectifier and elevated the limitations of conventional PWM regenerative rectifier. The efficacy of the MLI is proved by simulating a five-level CHB and investigating its open and closed loop performance.

6. References

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