Cryogenic Controller for Electrostatically Controlled Quantum Dots in 22-nm Quantum SoC

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ABSTRACT We present a fully integrated cryogenic controller for electrostatically controlled quantum dots (QDs) implemented in a commercial 22-nm fully depleted silicon-on-insulator CMOS process and operating in a quantum regime. The QDs are realized in local well areas of transistors separated by tunnel barriers controlled by voltages applied to gate terminals. The QD arrays (QDA) are co-located with the control circuitry inside each quantum experiment cell, with a total of 28 of such cells comprising this system-on-chip (SoC). The QDA structure is controlled by small capacitive digital-to-analog converters (CDACs) and its quantum state is measured by a single-electron detector. The SoC operates at a cryogenic temperature of 3.4 K. The occupied area of each QDA is 0.7 × 0.4 μm², while each QD occupies only 20 × 80 nm². The low power and miniaturized area of these circuits are an important step on the way for integration of a large quantum core with millions of QDs, required for practical quantum computers. The performance and functionality of the CDAC are validated in a loop-back mode with the detector sensing the CDAC-compelled electron tunneling from the quantum point contact (QPC) node into the quantum structure. The position of the injected charge inside the QDA is intended to be controlled through the CDAC codes and programmable pulse width. Quantum effects are shown by an experimental characterization of charge injection and quantization into the QDA consisting of three coupled QDs. The charge can be transferred to a QD and sensed at the QPC, and this process is controlled by the relevant voltages and CDACs.

INDEX TERMS Capacitive DAC (CDAC), charge qubits, cryo-CMOS, fully depleted silicon-on-insulator (FD-SOI), imposer, position-based qubits, quantum computer (QC), quantum dot (QD), single-electron detector, single-electron injector.

I. INTRODUCTION

QUANTUM computing is a new paradigm that utilizes the fundamental principles of quantum mechanics, such as superposition, interference, and entanglement [1], [2]. The range of complex problems from mathematics, chemistry, and material science that could be solved with quantum computing is far beyond the reach of today’s most powerful supercomputers. The potential is thus immense. Quantum
bits (qubits), basic units of quantum information, operate at a molecular/atomic level. They are extremely fragile and difficult to manipulate and read out. Some quantum computer (QC) technologies, such as those based on trapped ions and photons, do not require the equipment to be cryogenically cooled [3], [4], but the majority of qubits must operate under extremely low (cryogenic) temperatures in order to preserve their coherent superposition state. Due to the above requirements, existing commercial implementations of QCs are bulky and expensive (mainly due to the required auxiliary cooling equipment), can utilize only a relatively small number of entangled qubits, and cannot be reliably scaled up and reproduced in mass production due to difficulties with maintaining their quantum states but also due to cooling and control/detect connectivity issues [5], [6], [7], [8].

To address these challenges, we propose to leverage the unprecedented scalability of contemporary CMOS technology. Just like with a small IC chip, where a single nanometer-scale transistor can be reliably replicated billions of times to build a digital or mixed-signal processor, a new position-based charge qubit structure [7], [8], [9], [10], realized as a CMOS-compatible coupled quantum dot array (QDA), can be reliably replicated thousands (perhaps, millions) of times to construct a single-chip quantum processor operating at $\sim 4$ K where the cooling requirements are modest.

There are several approaches toward the physical realization of QCs, with those most notable based on superconducting [11], photonic [12], ion traps [13], and semiconductor qubits [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31] (see our discussion on state-of-the-art in qubits in [7]). Superconducting quantum computing is the most prevalent in industry, as a result of the quality of qubits and maturity of the technology, and is currently deployed for commercial applications [32]. Superconducting qubits and higher quality spin qubits are placed inside the deepest stage of a dilution refrigerator, at 20 mK or so temperature [see Fig. 1(c)] and under a very stringent thermal budget of $20 \mu$W that prohibits large-scale integration with their control electronic circuitry [5], [33], [34]. For example, in [35], a 60-mK current-biased heterojunction bipolar transistor is placed at the same cryogenic stage as its interfacing qubit, but the following amplification and readout circuitry still resides at the room temperature. Although a good step toward a full cryogenic readout of qubits, such an arrangement currently consumes a large space and makes this approach hardly scalable due to the allocation of one or two control lines for each qubit. The semiconductor-based quantum computing, specifically using commercial CMOS technologies, is a relatively recent approach and very promising as it provides potential for the integration of qubits with their control and readout circuits on a single chip [see Fig. 1(a)]. This can be advantageous for the realization of a large-scale QC capable of solving practical problems.

The use of standard CMOS operating at the 4-K cryogenic temperature of liquid helium (“cryo-CMOS”), rather than conventionally at the room temperature, was first proposed in [5] and [6] for the arrangement where the control electronics reside at the 4-K thermal stage within a dilution refrigerator (thermal budget $\sim 1.5$ W), while the actual qubits are at the deepest 20-mK stage. A collection of interfacing wires now has to traverse a subsequently shorter distance of $< 1$ m across the modest temperature change of 4 K [see Fig. 1(c)]. Since then, a number of publications on the cryo-CMOS interface circuits for the control and readout of qubits have been reported [32], [33], [37], [38], [39], [40], [41], [42]. However, a more important challenge is the implementation of qubits and quantum gates in standard CMOS processes to facilitate tight monolithic integration with their control electronics. This requires significant breakthroughs to drastically increase the operational temperature of qubits (“hot qubits”) and reduce power consumption of the control/detect circuitry while simultaneously improving the qubit performance in terms of uniformity and fidelity. The very recent publications in [43] and [44] present a quantum readout circuitry that works at cryogenic temperature but still exhibits high power consumption per qubit, which makes it difficult to scale for a higher number of qubits. In other very recent publications [45], [46], RF-reflectometry-based...
readout circuitry is presented that relies on a multiplexing technique to cover the output data of all associated qubits due to the large needed area for the readout circuitry alone.

Solid-state qubits based on quantum dots (QDs) are the most compatible structures for an implementation using silicon technology. A number of structures for such qubits have been recently reported [17], [18], [19], [20], [21]. Furthermore, a few quantum gates have been developed, mostly limited to simple two-qubit gates [16], [27], [29]. However, these qubits and quantum gates have been implemented using special processes (e.g., isotopically enriched silicon, Si28) which are not yet compatible with standard CMOS. As a result, they cannot be scaled up to levels envisioned by the potential of CMOS technology without incurring substantial fabrication investments. Furthermore, some other recent works have proved the feasibility of qubits operating above 1 K (the mentioned hot qubits) [27], [28], [29], which is promising for the future of CMOS quantum computing.

In this article, we offer a vision of a position-based charge qubit structure intended to operate at 4 K and fully integrated with its interfacing circuitry using a volume-production 22-nm fully depleted silicon-on-insulator (FD-SOI) CMOS process that has unique benefits for quantum operation [31], [47], [48], [49]. In contrast to bulk CMOS, FD-SOI provides a thin semiconductor layer isolated vertically from the substrate by a 20-nm buried oxide (BOX) layer. Therefore, a quantum particle can be strictly confined inside the 5-nm thin semiconductor film where it precisely follows the gate control, and is isolated from the substrate impurities to further increase its decoherence time. This opens up new possibilities for charge qubits that were popular but then abandoned over a decade ago [14], [15].

It is noteworthy that hybrid qubits [50], [51], [52], i.e., those combining the quantum charge and spin information, have the potential to combine the benefits of both types of qubits, i.e., fidelity of spin qubits with the speed and convenience of control/readout of charge qubits [48], [53]. However, in this article, we focus on the prospects of charge qubits and their interfacing circuits, most notably a reset transistor and capacitive DAC (CDAC) for injecting individual electrons into the qubit structure and then controlling their movement, as well as a single-electron readout path for detecting a quantum state of the qubit structure.

The remainder of this article is organized as follows. Section II presents a brief overview of CMOS position-based charge qubits. Section III describes specifications and detailed implementation of the interface circuitry. Section IV discusses the measurement setup and experimental results of the interface circuitry.

II. OVERVIEW OF QDA STRUCTURE FOR CHARGE QUBITS

The QD-based qubits can be constructed based on the spin (e.g., up/down polarization) [17], [20], [21], [26] or charge (e.g., electron’s position within a double QD) [14], [15], [31] of the carriers. When looked in isolation, the spin qubits appear more advantageous than the charge qubits, mainly due to longer decoherence times. However, several other performance metrics should be considered for large-scale integration [47], [48], [49], [54]. The weak interactions of the spin qubits with their environment, which is beneficial to their long decoherence times, make interqubit operations challenging. The charge qubits, however, can achieve stronger coupling to each other, enabling the realization of quantum gates through arrays of QDs [7], [10], [24], [55], as shown in Fig. 2.

A linear arrangement of QDs (i.e., quantum shift register, Fig. 2) allows the individual electrons to travel within the structure [7], [8]. For example, once the electron is injected into a QD, it can be transported to a neighbor QD through a \( \pi \) phase shift [56]. It can then be transported to the next QD through another \( \pi \) phase shift. We can thus construct a 1-D topological array of QDs that move around an electron in its entirety (for \( \pi \) phase shifts) or transfer around part of its wavefunction \( \Psi \) (for phase shifts other than \( \pi \)). For example, \( \pi/2 \) implements a Hadamard gate \( (H) \). Other single-qubit gates (e.g., \( R(\phi) \) rotation) can be obtained by adjusting the pulse duration of the imposer’s voltage.

The next step required to realize a QC involves the quantum entanglement of multiple qubits. This entails theoretical developments, simulations, and measurements of the entanglement dynamics in a multiqubit system [8]. Two arrays of QDs can be “joined” at certain QD nodes such that their respective electrons can electrostatically interact (i.e., two QDs at the middle of the quantum structure in Fig. 2). If wavefunctions \( \Psi \) of each of the electrons in the top and bottom arrays start to overlap, then their common quantum state will, under certain circumstances, entangle [8].

Our work is based on position-based charge qubits [8] that utilize a DRAM-like low-power electrostatic gate control, thus enabling the scaling to higher qubit counts. The physical structure of the qubits and their control circuitry have been designed in “22FDX” FD-SOI process technology from GlobalFoundries. As illustrated in Fig. 3, a gap between the two gates in two adjacent gates, which is below 100 nm,
forms a physical trap for electrons inside the quantum core. Such a small physical distance enables the dynamic control of electrons by properly adjusting $V_{\text{gate}}$, as described in [8]. This can provide the single electron with the energy required to move between two QDs in a quantum core when sufficiently high $V_{\text{gate}}$ is applied. If the potential energy applied to an electron is greater than $E_c = e^2/(2C)$, where $C$ is the total equivalent capacitance of the QD, then the electron can tunnel into the QD. For example, a capacitance of 10 aF (112 aF for the terminal QD when connected to the detector) exhibits the single-electron charging energy of 8 meV (0.7 meV), which is larger than the thermal energy of a single electron at 4 K, i.e., $kT = 0.34$ meV, where $k$ is Boltzmann’s constant and $T$ is the absolute temperature in kelvin. The higher single-electron potential charge energy prevents the electron from tunneling into the QD caused by thermal excitation [36].

III. QUBIT INTERFACE CIRCUITRY

A. TOP-LEVEL ARCHITECTURE

Fig. 4 presents the structure of the CMOS position-based charge qubit incorporating two electrostatically coupled QDAs [8], [47], [49], with schematics of nearby interfacing circuitry: reset, control, single-electron injector, and detector. It belongs to a quantum processor implemented in 22-nm FD-SOI CMOS and operating at a cryogenic temperature of ~4 K [54].

We can perform the charge qubit readout using simple charge sensors integrated with the qubit structure as shown in Fig. 4 [49]. The readout of spin qubits, on the other hand, is much more complicated and requires the presence of a magnetic field and a spin-to-charge conversion [33].

We can control the charge qubits electrostatically using gate pulses which can be generated with microvolt and picosecond-level accuracy using CMOS circuits [47], [49], [54], which consume > 2 orders-of-magnitude lower power than for controlling spin qubits [33], [39]. However, for the control of spin qubits, a magnetic field is also required.

The currently estimated decoherence time in our system is > 50 ns [56], which is 2–3 orders of magnitude shorter than that of the spin-based qubits. However, the cut-off frequency ($f_T$) of the used process technology is in the hundreds of GHz, allowing the realization of quantum gate flip operations < 50 ps, which is 2–3 orders of magnitude faster than with the spin counterparts. In further support of the process capabilities, Elsayed et al. [57] and Åberg et al. [58] disclosed the measurement results of digital and mixed-signal circuits, also implemented in the same 22-nm FD-SOI, indicating that the circuits can be functionally faster than 50 ps, i.e., equivalent to 20-GHz operating speed. This suggests roughly the same number of over 1000 gate operations per useful decoherence time. Therefore, despite their apparent imperfections when examined in isolation, the charge qubits generally appear as an attractive choice for integrated large-scale quantum computing systems [7], [8], [10].

As shown in Fig. 4, a distance of 20 μm between the quantum structure and the interface circuitry allows to mitigate the effect of noise originating from the circuit switching activities in the detector path. The first source follower (SF) together with a reset switch of the detector path are located adjacent to the last QD (realized as a quantum point contact (QPC) [59], [60]). This helps minimize the loading capacitance, which impacts the readout charge-to-voltage ($Q$-to-$V$) conversion gain. To minimize the impact of supply-line noise, the preamplifier (preamp) and correlated-double-sampling (CDS) detector are powered from a charge stored on the $C_{\text{float}}$ capacitor, which is isolated from the external supply lines by “SW float” switches during the measurement.

Electrons are injected into the QDA row through the injector interfaces (i.e., “quantum inject CDAC” in Fig. 4). Once an electron is in the first QD, its subsequent position (i.e., quantum state) is controlled by a sequence of gate pulses (i.e., $V_{\text{imp}}(t)$). A QD passes the electron carrying the quantum information from the main quantum cell to the QPC [47] which performs the $Q$-to-$V$ conversion.

The reset action which can be conducted by “quantum reset CDAC” in Fig. 4 performs two functions: first, it defines the reference voltage for the quantum cell and, second, it sets the bias voltage for the detector. The minimum size “$M_{\text{reset}}$” MOS transistor performs a subthreshold reset that minimizes the channel charge-sharing injection while ensuring a low OFF-state leakage current that keeps the quantum electron confined in the QPC during the detection.

Fig. 5 shows the interface circuitry to the string of quantum devices from Fig. 4. Injectors and imposers generate narrow pulses from a set of clock waveforms with a precisely controllable amplitude, and these pulses are used to set
the potential in the quantum row, inject a single electron, and set imposing phases, respectively. Following the reset, a single electron is injected from the QPC node into the quantum row with a precisely timed/leveled pulse \( V_{\text{inj}}(t) \), and its quantum state is subsequently modified with a set of imposer pulses having a precise pulse width, baseline, and amplitude \( V_{\text{imp}}(t) \) [with reference to Fig. 5(b)]. The detector samples and amplifies the voltage difference at QPC before and after the imposing phase, and sends this amplified voltage off the chip. A binary-weighted CDAC followed by a capacitive attenuation is used to generate a digitally programmable pulse amplitude to control the QDs inside the quantum core. The precharge switch sets the pulse baseline to a bias voltage \( V_{\text{pre}} \), which is supplied from an off-chip bias generator.

The layout of the proposed system exhibits sufficient separation between the QDs and the active FETs of the single-electron readout and CDACs to minimize the effect of electrical disturbance and local heating on the QDs. The CDAC’s active FETs are more than 120 \( \mu \)m away from the QDs. Furthermore, the single-electron readout’s FETs are over 20 \( \mu \)m away from QDs.
In the presented design, the CDAC capacitors as well as CDAC resolution are overdesigned, which had to be done conservatively due to the lack of (even approximate) models. However, in the next generations targeting the 1 million physical qubits or so, we should be able to reduce the CDAC’s resolution and its capacitor size to reduce the total power consumption and area. The required number of detectors can be much smaller than the number of qubits since they are engaged only at the end of the quantum experiment (thus, their duty cycle can be much smaller than 1). Note that in any charge-qubit system, the operation is at baseband, thus avoiding any need for the RF upconversion needed by spin qubits. The baseband frequency is naturally much lower, e.g., events at < 1 GHz. As a result, the control of qubits can be realized using the mixed-signal circuitry, which consumes 2–3 orders-of-magnitude lower power compared to the RF circuits required for the spin qubits.

B. IMPOSER AND INJECTOR TOPOLOGY

1) CIRCUIT IMPLEMENTATION

In order to control the quantum states, the CDAC must ensure to cover all the required functionality, such as: precharge, reset, as well as single-electron injection, extraction, and transfer. An additional important design consideration for CDAC is that the quantum structures require many controlling signals that are all needed to be routed into a very small space, as shown in Fig. 6. Power consumption and $kT/C$ noise are yet another challenging design considerations of the CDAC capacitor array.

Fig. 7 shows the top-level diagram of the 8-bit binary-weighted CDAC architecture with 255 identical weight units. The CDAC is composed of several building blocks, including the clock gating, capacitor array, precharge (pedestal setting), and pulse shaping filter. The capacitors in the binary-weighted array are divided into unit cells (UCs), with the UC’s details shown on the left side of Fig. 7. The cell is composed of logic gates that are designed to drive the light capacitive divider (i.e., $C_{u1}$ and $\sum C_{u3}$). Note that a “parasitic” capacitor $C_{u2}$ is intentionally placed inside each UC to compensate for the charge injection and clock feed-through at the CDAC output (node N1). This results in a reduction of the over- and under-shooting on node N1, which is very important for the proper operation of QD. As shown in Fig. 8(a) and (b), the falling edge injects a small compensating charge into N1 while the negated clock input ramps with a 5-ps delay in the opposite direction. This results in a reduction of the voltage ripple [49].

To maintain the low dynamic power consumption, clock-gating circuits are provisioned to feed the 2-GHz clock only to the enabled CDAC units. As shown in Fig. 8(c), first, the voltage on N1 is precharged to the desired dc level. Then, the CDAC is activated to establish the pedestal of the QD energy barrier levels. It is necessary to slow down the clock transitions at N2, inside the UCs, in order to avoid glitches at the output of the CDAC. These glitches could cause errors in the energy level of the injected electron during the quantum experiment. The extra AND gate can reduce these glitches and make the signal transitions at N2 much smoother. The fast transients at $V_{out}$ are reduced by the 11-stage RC pulse-shaping filter. This helps lowering the high-frequency noise components of the output CDAC pulses, thus stabilizing the energy levels of QD electrons. It should be noted that at the time of design, the characterization of polysilicon resistors (without salicide) had not been validated to ensure its resistivity at the cryogenic temperature of 4 K [38], [39]. Therefore, $R_c$ is implemented with the lowest metal layer, Metal1 (M1), in the form of long traces with 50-nm width, but which still meets the DRC rules. On the other hand, all the CDAC’s capacitors are designed using higher metal layers with a density of 5.08 fF/µm². The CDAC output voltage is periodically added to the pedestal $V_{pre}$ as

$$V_{out}(D) = \frac{D \cdot C_{u1}}{C_{out} + 255C_{u1}} V_{DD} \quad (1)$$

where $C_{out}$ is the total fixed capacitance at the CDAC’s output node N1, including from the 11-stage filter that becomes effective after its settling of a few time constants. As a result, $C_{out}$ can be calculated as $11C_c + 255C_{u3}$. Equation (1) is a simplified formula and does not include the parasitics capacitance of the CDAC switches. By taking into account the extracted parameters shown on the left side of Fig. 7, the CDAC’s full-scale range from the pedestal is $V_{out}(D = 255) \approx 70$ mV. The step size is therefore $V_{out,LSB} \approx 273 \mu$V. The bias for the precharge switch $V_{pre}$ is supplied from an off-chip reference. Long-channel MOS transistors are employed by the CDAC in the precharge switch so as to help reduce the leakage current at the output of the CDAC.

Fig. 9(a) shows the UC layout with metals layers M1 and M3 exposed. The net names and capacitors are annotated to match with Fig. 7. The laterally coupled M3 lines between nodes N1 and N2 give rise to $C_{u1}$. The charge injection compensation is enabled by $C_{u2}$ which is coupled between the inverter output (on M1) and N1 (a single finger on M3) as highlighted by the red box. The 0.8-V rail-to-rail negative clock signal should be weakly coupled for the proper compensation. Fig. 9(b) shows the UC layout on the left side where the lateral coupling between M3 and M4 gives rise to $C_{u3}$. The floor-plan of the capacitor array is shown on the right side. The “tall and skinny” floorplan makes the integration of the array of CDACs seamless as each layout.
FIGURE 7. Detailed schematic of CDAC functioning as a part of the imposer, injector, and reset device for the quantum experiment. Note that resistors $R_C$ are made of metal M1 (adapted from [49]).

FIGURE 8. Signal activity outputs for CDAC for (a) no negative edge clock, (b) active negative clock edge, and (c) precharge voltage add to the CDAC output.

FIGURE 9. Layout structure of (a) compact CDAC unit-cell fragment showing charge-injection compensation and (b) whole CDAC UC and its floor plan.

cell is stacked in a tile and placed next to the quantum core. The common lines between the CDACs, such as $V_{DD}$, GND, clk, and $V_{pre}$ are routed along the CDAC array.

2) NOISE AND REQUIRED SPECIFICATIONS FOR QDS

The thermal noise of CDAC circuits, appearing in the form of $kT/C$ noise, should be maintained at a sufficiently low level to prevent disturbing the Coulomb blockade operations in the QDA. We can derive the equivalent total noise at the output of CDAC (i.e., at N1) by adding the noise contributed by each switch-cap circuit of Fig. 7. It can be shown that the output noise power caused by the $i$th switching bit of $D$ can be derived as

$$v_{noise}^2(b_i) = \left(\frac{2^i \cdot C_{u1}}{2^i \cdot C_{u1} + C_{o1}'}\right)^2 \cdot \frac{kT}{C_{o1}'}$$

(2)

where $C_{o1}' \approx C_{o1} + 255C_{u1}$ now incorporates the static (fixed) as well as dynamically switched capacitors at the output node. Equation (2) estimates the noise based on the voltage division of the two series capacitors: $C_{u1}$ in the $i$th UC and the total shunt capacitance lumped at the output node. Assuming uncorrelated noise contributions from the switch-cap units, we can estimate the total noise power by means of accumulating the noise power contributions from each $b_i$ switch-cap from (2) and its precharged noise power. As a result, the total noise power can be described as

$$v_{noise}^2 = v_{noise}^2\text{(precharge)} + \sum_{i=0}^{7} v_{noise}^2(b_i).$$

(3)

By taking into account its equivalent values, (3) can be simplified. We note that the total noise is dominated by the precharge switch as shown in the following:

$$v_{noise}^2 \approx \frac{kT}{C_{o1}'} \left(1 + 128 \frac{C_{u1}}{C_{o1}'}\right)$$

(4)

For the unit capacitor $C_{u1} = 0.135\,\text{fF}$, $C_{o1}' = 392\,\text{fF}$, we calculate the total noise at $T = 4\,\text{K}$ at the level of $12\,\mu\text{V}_{\text{rms}}$ or $4.3\%$ of the LSB.

The key specifications of the CDAC for the designed system are summarized in Table 1. They are derived from physical equations and COMSOL multiphysics modeling of the QDA structure [8], [56]. To achieve the required signal-to-noise ratio compared with the $kT/q$ thermal energy of an electron, the resolution of the voltage step at the tunnel junction between QDs should be finer than $300\,\mu\text{V}$ at $4\,\text{K}$.

| Speed (GHz) | Voltage Range (mV) | LSB (mV) | Overshoot (mV) | Jitter (ps-peak) |
|-------------|---------------------|----------|----------------|------------------|
| 2           | 70                  | 0.3      | 0.3            | 5                |

TABLE 1. Key Specifications of the CDAC.
Yet, the capacitive division between $C_{\text{ox}}$ (gate oxide capacitance) and $C_t$ (tunnel junction capacitance) necessitates the voltage levels presented at the imposer gates to be $\sim 10 \times$ larger. Consequently, the target resolution of CDAC should be set below $300 \mu V \times 10 = 3 \text{ mV}$. On the other hand, to cover the increase in mismatch and model inaccuracies at $4 \text{ K}$, an extra margin of $10 \times$ was considered; therefore, the CDAC step size was eventually set at $300 \mu V$.

In our QDA system, the decoherence time is evaluated to be more than $50 \text{ ns}$. The key CDAC function is to shuttle an electron between multiple QDs well within the decoherence time. Therefore, we set the CDAC sampling period to $0.5 \text{ ns}$. For larger QDA structures, this sampling period should be reduced. Any timing error or jitter noise at the CDAC output can result in the accumulation of error in the equivalent injected energy into the QD and, consequently, can disturb the electron’s quantum state. The equivalent area under the CDAC output pulses is proportional to the injected energy into the QD. Excluding the effect of the voltage noise and the ripples caused by CDAC output pulses, the error in the injected electron’s energy is restricted by the timing errors (i.e., jitter) of the pulses. Minimum pulse duration of the CDAC output signal is designed to be $0.5 \text{ ns}$. As a result, the timing error should be at least $10^2$ times smaller, yielding the specification level of $5 \text{ ps}$.

### C. READOUT PATH

1) CIRCUIT IMPLEMENTATION

Fig. 10(a) illustrates the readout circuitry for detecting the quantum state of the QDA structure. The detector chain performs as a single-electron detection to determine a net gain or loss of an individual electron within a timing period set by $S_0$ and $S_1$ pulses from the QPC interface node. The designed system consists of a double source follower $M_{3,4}$, a preamp, and a switched-capacitor correlated double sampler (CDS). The size of $M_3$ was minimized for higher $Q$-to-V gain, but such a choice increases the flicker noise from the device. However, this is effectively mitigated by the CDS arrangement that samples the signal twice with the narrowly separated $S_0$ and $S_1$ pulses, just before and after the electron is expected to be injected into or received from the QPC well (labeled as “QPC” in Fig. 4). The total capacitance at the QPC node is effectively reduced by means of a double-bootstrapped SF (i.e., $M_{3,4}$) which largely neutralizes the $C_{s\text{g}}$ and $C_{g\text{d}}$ parasitic capacitances of the front-end $M_3$ SF device. A negative supply voltage is used to allow both the front and back gates of $M_3$ to be biased at the ground level, which is the condition to minimize the gate leakage current [49].

Considering the elementary charge of an electron, $q = 1.6 \times 10^{-19} \text{ C}$, the parasitic capacitance at node QPC should be minimized to increase the voltage swing. The voltage swing of $V_{\text{q, SF}}$ at the SF input caused by a single electron can be given by

$$V_{\text{q, SF}} \approx \frac{q}{C_{\text{SET}} + C_{\text{DD, M\text{-reset}}} + C_{\text{GS}} + (1 - G_{\text{SF}}) \cdot C_{\text{GD}}} \quad (5)$$

where $C_{\text{SET}}$ is the capacitance of the single-electron transistor (SET) in the QDA, with reference to Fig. 4, that is seen by the SF input, $C_{\text{DD, M\text{-reset}}}$ is the parasitic capacitance at the drain of $M_{\text{reset}}$, and $G_{\text{SF}}$ is the voltage gain of the SF. $C_{\text{GS}}$ and $C_{\text{GD}}$ are the gate-to-source and the gate-to-drain capacitances of the input transistor ($M_3$), respectively. Using a detailed layout extraction, the total parasitic capacitance at the QPC node (see Fig. 2) is estimated at $C_{\text{QPC}} \approx 112 \text{ aF}$ and, therefore, the voltage swing is around $1.4 \text{ mV}$.

The preamp of 6-dB extrapolated gain drives the sampling capacitors $C_{\text{S1,2}}$ of the CDS detector. As shown in Fig. 10(b), pulse $S_0$ is asserted to sample the initial level of preamp output to $C_{\text{S1}}$. Then, after a delay of $T_D$, $S_1$ is asserted to sample the preamp output to $C_{\text{S2}}$. The difference of voltages stored on $C_{\text{S1}}$ and $C_{\text{S2}}$ is amplified during $S_2$ with a gain of $C_{\text{S1,2}}/C_{\text{F}}$. The differential output at nodes $\text{OUT}_{\text{ND}}$ and $\text{OUT}_{\text{PD}}$ is fed to the final-stage analog buffer driving the off-chip detector components depicted in Fig. 10(c). The equivalent linear model of the signal path is shown in Fig. 11. The transfer function of SF and its preamp exhibits a second-order low-pass filtering (LPF), i.e., $H_{\text{LPF}} = H_{\text{SF}} \cdot H_{\text{preamp}}$, which can be derived as

$$H_{\text{LPF}}(\omega) = \frac{G_{\text{SF}} \cdot G_{\text{preamp}}}{(1 + j \frac{\omega}{2\pi f_{\text{SF}}}) \cdot (1 + j \frac{\omega}{2\pi f_{\text{preamp}}})} \quad (6)$$

where $H_{\text{LPF}}(\omega)$ is the frequency response of the LPF, $G_{\text{SF}}$ is the voltage gain of the SF, $G_{\text{preamp}}$ is the voltage gain of the preamp, $f_{\text{SF}}$ is the cutoff frequency of the SF, and $f_{\text{preamp}}$ is the cutoff frequency of the preamp.

FIGURE 10. Detailed schematic of (a) CDS topology, (b) timing diagram of control signal for CDS, and (c) output buffer with an off-chip load (adapted from [49]).
where $G_{\text{preamp}}$ is the dc gain of the preamp, $f_{S\text{F}}$ and $f_{\text{preamp}}$ are the equivalent dominant poles of the SF and preamp, respectively. They are, respectively, estimated at 10 and 1.5 GHz based on SPICE simulations. The CDS detector functions as a first-order high-pass filter, whose transfer function can be derived as

$$|V_{\text{out,CDS}}(f)| = G_{\text{CDS}} \cdot 2|\text{sinc}(\pi f T_3)|$$

$$\times \sum_{n=-\infty}^{n=\infty} |V_{\text{in,CDS}}(f - nf_3)| \cdot |\sin(\pi T_D(f - nf_3))|$$

(7)

where $T_D$ is the delay between $S_0$ and $S_1$, $T_3$ is the sampling period of $S_0$ and $S_1$, and $f_3 = 1/T_3$ is the sampling frequency. Based on the transfer function, the dominant pole of the CDS is calculated at $(1/6T_D)$, having a maximum value at 67 MHz when considering the minimum delay $T_D$ of 2.5 ns. The total equivalent noise of the signal path takes into account the combined noise contributed from SF, preamp, and CDS detector.

2) CIRCUIT SIMULATION

To be able to drive the long routing lines to the off-chip resistive load, a relatively large size of input devices and higher bias current are adopted. This also helps to minimize the thermal and flicker noise at the output buffer circuitry of Fig. 10(c). It should be noted that the input-referred (or, in our case, “electron-referred”) noise contributed by the output buffer will be attenuated by the gain of the preceding amplification stages, i.e., preamp and the CDS. Therefore, the contribution of the output buffer to the in-band noise of the signal path can be negligible. The major in-band noise contributor of the readout path is the SF, preamp, and sampling noise of the CDS detector. By means of the low-pass filtering effect of SF and preamp, and the high-pass filtering effect of the CDS detector, the in-band noise can be minimized by optimizing the gain and bandwidth of the SF and preamp.

Fig. 12 shows a simulated gain breakdown of the readout path revealing the relative gains of individual blocks across different input voltage steps. It was done at 70 K, which is the lowest temperature supported by the PDK, although the results there are unreliable as they are beyond the normally calibrated temperature range of $-40 \degree C$ to $+125 \degree C$. A 1.5 kΩ resistor is used as a load for the output buffer. Thus, the obtained total simulated gain for a single-electron step of 1.4 mV is 39 (V/V), whereas the gain based on a single-electron measurement at 4 K is 70 (presented later in Section IV-D). The gain of the output buffer decreases at higher input voltage steps due to compression.

Fig. 13 shows the transient noise simulation of the complete readout path for 0.2 ms after the QPC was reset (by momentarily applying 800 mV to $V_{\text{reset1}}$ and 0 V to $V_{\text{reset2}}$ with reference to Fig. 10) and then left floating undisturbed. The simulation is performed at the lowest temperature supported by the process PDK (70 K) while the load resistance of 1.5 kΩ is considered with $T_D$ of 2.5 ns, and the CDS rate of 50 MHz (i.e., separation of $S_0$ and $S_1$ in Fig. 10 and $1/T_3$ in (7)). Due to the presence of associated noise, the output signal shows a random variation with a zero mean, as shown in Fig. 13. Fig. 14 illustrates the corresponding power spectrum density (PSD) at the output buffer and preamp. The preamp exhibits a low-pass characteristic with lower than $-110$ dBV in-band noise. Thanks to the discrete sampling nature of the CDS chain, the PSD noise characteristic at the output shows the effect of sinc function in the frequency domain, where the notches repeat at 50 MHz (i.e., the sampling rate of $S_0$ and $S_1$ in Fig. 10).

IV. EXPERIMENTAL RESULTS

A. TEST SETUP OF THE CHIP

The quantum system-on-chip (SoC) is implemented in 22-nm FD-SOI CMOS. The chip die occupies 3 × 3 mm².
Its micrograph is shown in Fig. 15(a). Fig. 15(b) shows a zoomed-in portion that indicates the locations of the fully integrated quantum core along with its control electronics. This includes the quantum execution cell, device exclusion area, low-noise preamp, CDS, and output buffer. The CDAC occupies $3.5 \times 45 \, \mu m^2$ and consumes 0.27 mW in dynamic power running at a 2-GHz system clock. The single-electron detector occupies $40 \times 25 \, \mu m^2$ and consumes only 1 mW at a 150-MHz sampling frequency, including its output driver [49]. The digital processor part was described in [53] and [54].

The cryogenic test apparatus with the detailed measurement setup is illustrated in Fig. 16. The fabricated chip is mounted on the “Alpha” test printed-circuit board (PCB) inside the cryogenic chamber, which is cooled down to < 4 K. Small decoupling capacitors are used on the test board to decrease noise and ripple from the digital activities. Other parts of the controlling circuits and components are placed outside the chamber at room temperature, which helps the system to decrease the power dissipation in order to maintain the chip at < 4 K. The test PCB is connected to a first-side connector (FSC) board at the edge outside the cryo-cooler through a wire ribbon which carries supplies and I/O signals. The cryoflex board contributes to the thermal isolation between the cryo-part of the chamber that is at ~4 K, and the outer part of the chamber, adjacent to the room temperature which is at 70 K, due to the higher thermal resistivity of the wires on the flex connection. The air-side connector (ASC) board is responsible for the connection between the FSC board in the intermediate section of the chamber at 70 K to the room temperature environment. To allow extensive programmability of the measurement setup, an FPGA Mezzanine card (FMC) is used for the communication between the device under test, the off-chip components, e.g., ADCs, power supply management, and connections to measurement equipment outside, i.e., FPGA, PC, high-frequency RF signal generator, and a high-frequency oscilloscope. This allows direct automated testing from the PC. In addition, to have a real-time temperature monitoring in the cryo-cooler near the chip and intermediate section inside the chamber, various temperature sensors are embedded on the corresponding PCBs at different sections of the test chamber.

### TABLE 2. Key specifications for the detector chain.

| Sampling rate (MHz) | Min. gain (V/V) | Input-referred noise (mV$_{rms}$) |
|---------------------|-----------------|----------------------------------|
| 50                  | 30              | 0.35                             |

**B. CHARACTERIZATION OF THE DETECTOR**

We start the measurements with a characterization of the single-electron detector. Fig. 17 shows the probability density function (pdf) of the detector’s sampled output voltage over 10,000 trials at 3.4 and 70 K, for measurements and simulations, respectively, while the QPC input is kept undisturbed. The total measurement time span is 0.2 ms, i.e., 10,000 trials × (1/50 MHz). The measured standard deviation of the detector output noise ($\sigma_{out}$) at 3.4 K is 18 mV$_{rms}$. Note that with the estimated detector gain of 70 (V/V) measured at ~4 K (presented later in Section IV-D), the input-referred noise is estimated to be 0.257 mV$_{rms}$. To compare this with the system simulations in Section III-C.2, Fig. 17 superimposes the pdf of the simulated output noise $\sigma_{out}$ of 39 mV$_{rms}$ at 70 K based on Fig. 13 with the gain of 40 (see Fig. 12). The equivalent simulated input-referred noise is estimated as 0.97 mV$_{rms}$. Despite the gaps between the simulation and measurement, both values of input-referred noise satisfy the required specifications of the detector path as they are lower than the voltage swing at QPC caused by a single electron (i.e., 1.4 mV). Table 2 summarizes the key specifications for the detector chain.

### C. CHARACTERIZATION OF THE CDAC

In this section, we describe the loop-back configuration to characterize the CDAC and its driving capability to the single-electron device. The proposed “loop-back” measurement method is shown in Fig. 18. We take advantage of the presence of a nearby single-electron detector with CDS to capture the difference in the QPC potential developed between $S_0$ and $S_1$ pulses. To start with, the reset device momentarily presets the QPC potential. An electron is then injected via tunneling from the QPC node into the first QD (QD1). This yields a net loss of charge, thus a positive quantum change in voltage. This is measured by the detector before and after the injection event ($S_0$ and $S_1$, respectively) so as to capture the potential net charge loss. This operation, however, depends on the reset switch transistor $V_{reset}$ staying under the subthreshold operational regime. If not, then $V_{reset2}$ will pull the

1. This is conceptually similar to the loop-back modes in radio transceivers for testing and calibrating entire chains.
QPC node and any information associated with the electron injection will be lost. Consequently, when the gate and source of $M_{\text{reset}}$ are swept over a suitable range, there will be a set of $V_{\text{pre,reset1}}$ and $V_{\text{pre,reset2}}$ voltages when the $M_{\text{reset}}$ transistor just barely turns on, i.e., when $V_{\text{gs}} = V_{\text{pre,reset1}} - V_{\text{pre,reset2}}$ is right at the strict neighborhood of the threshold voltage, $V_{\text{th}}$. This will ensure the subsequent electron injection from node QPC into the QD structure. If $V_{\text{GS}} > V_{\text{th}}$, then node QPC will be ac-grounded during the quantum experiment and detection. If $V_{\text{GS}} < V_{\text{th}}$, then node QPC will simply not get reset. Lowering $V_{\text{gs}}$ after the reset by means of the CDAC will help $M_{\text{reset}}$ to stay below $V_{\text{th}}$ during the electron injection and detection phases. There is a gap between these two regions which is proportional to the voltage swing at the CDAC output controlled by CDAC code [see (1)]. With reference to Fig. 18(b), increasing the CDAC code will lower $V_{\text{reset1}}(t)$ after the reset phase of the experiment, which helps $M_{\text{reset}}$ to stay in the subthreshold region for the wider equivalent voltage range of $V_{\text{pre,reset1}}$ and $V_{\text{pre,reset2}}$, as a result, larger acceptable voltage range of $V_{\text{pre,reset1}}$ and $V_{\text{pre,reset2}}$. This can ensure the subsequent electron injection from node QPC into the QD structure. Increasing the acceptable voltage range of $V_{\text{pre,reset1}}$ and $V_{\text{pre,reset2}}$ results in a wider voltage gap in Fig. 19 for higher CDAC codes [49].

Fig. 19 plots the measurement results of applying the control pulses of Fig. 18(b). The heat color indicates the detector’s output voltage. The very high $V_{\text{pre,reset1}}$ (x-axis) and very low $V_{\text{pre,reset2}}$ (y-axis) values maintain the voltage at the QPC, so the CDS contributions will be close to zero. If $V_{\text{pre,reset1,2}}$ are set appropriately, as stated above, the detected voltage change (red area in Fig. 19) will correspond to an electron loss due to the tunneling from QPC to QD1. The red gap area in Fig. 19 is changing from 20 to 114 mV, which corresponds to the output voltage step of $V_{\text{reset1}}(t)$ due to the CDAC [49].

Fig. 20(a) shows the voltage gap observed in Fig. 19, which corresponds to (1), versus the CDAC code, $D$. The
INL and DNL nonlinearities of the CDAC transfer function [Fig. 20(a)] are plotted in Fig. 20(b). Despite the DNL of 10 LSB, the system works as intended in the manual/experimental mode of operation, which merely requires precise pulse transitions between two semistatic voltage levels. We plan to substantially improve it in future versions to take advantage of algorithmic searches for the optimal reset, injector, and imposer voltages [49].

To verify the above loop-back configuration via an alternative method, a direct measurement is performed by means of a comparator that is embedded inside the quantum core, as shown in Fig. 18(a). To estimate the CDAC output, $V_{\text{ref}}$ was swept through an off-chip 16-bit DAC (mounted on the FMC board) from 0 V to a level causing flipping of the output bit. This comparator triggering point corresponds to the output voltage of CDAC. Fig. 21(a) plots the resulting transfer function of the CDAC, while the corresponding DNL and INL are shown in Fig. 21(b). It can be observed that the measured CDAC output voltage range of around 75 mV matches with the estimation from (1). Unfortunately, due to the limitations of the measurements at a cryogenic temperature, the nonlinearities observed in Fig. 21(b) may come from the comparator offset in conjunction with the noise from the off-chip DAC.
D. CONTROL AND MEASUREMENTS OF CHARGE QUANTIZATION IN THE QUANTUM DOT ARRAY STRUCTURE

The value of 70 V/V for the total gain of the whole detector path at 4 K was used earlier in the system calculations. We now disclose the applied methodology to estimate this gain. Fig. 22 plots the control signal waveforms for quantum experiments using the loop-back method. In this measurement, the CDAC was initially reset to bring the pedestal operating voltage to all its internal nodes. In the next phase, the injection of a single electron into the system starts by triggering the $V_{\text{inj1}}$ pulse to the QPC. The imposing of the injected single electron in the QPC is carried out by applying $V_{\text{imp}}$. Two samples (i.e., $S_0$ and $S_1$) are collected from the output of the amplifier, which are then fed into the CDS. For this experiment, the CDAC code was set to 80 and the $V_{\text{pre, imp}}$ pedestal voltage, which is the precharge voltage of the imposing CDAC, is swept and the average output voltage of the output buffer is shown in Fig. 23. This shows the distinctly quantized voltage gap at the output of the output buffer. Higher values of the CDAC code produce higher quantization levels. The shown voltage gap of around 100 mV is the smallest. Thus, we attribute the injection of a single electron to this quantized voltage gap. As mentioned in Section III-C.1, the total equivalent capacitance at the QPC is $\sim 112$ aF, resulting in the input voltage swing $\sim 1.4$ mV for the single-electron injection at QPC. Considering the voltage step in Fig. 23 is around 100 mV, the measured gain of the whole detector system is estimated to be $\sim 70$ V/V.

The aim of the next part of this section is to present the experimental characterization of charge injection and quantization into a quantum array consisting of three coupled QDs. While the main focus of this article is on the quantum control circuitry, in this section, we aim to have a quick demonstration of the observed charge quantization, signature behavior of QDs, and its control by the interface circuitry. The goal is to show: 1) the charge can be transferred to a QD and sensed at the QPC and 2) the process is controlled by the relevant voltages and CDACs.

The methodology of the specific quantum injection test is as follows. The test quantum cell consists of a QDA made of three QDs shown in Fig. 24(a). The edge left and right dots are connected to the floating QPC #1 and #3 through a potential energy barrier controlled by the dc voltage applied at the terminals IU2/3/4/5. Specifically, the terminals IU2 and IU5 are directly responsible for charge injection from QPCs to dots QD1 and QD3, respectively. QPC1 and QPC3 are connected to the gates of the sensing SF transistors for a single electron readout. The differential voltage measurement...
is taken from CDS amplifiers of Fig. 10 labeled as buffer output #1 and #3 in Fig. 24(a). The experiment is controlled by specific logic signals activating differential measurements and pulses at the imposer terminals IU2/3/4/5. The experiment is initiated by a pulse S0 [of 9-ns duration, as shown in Fig. 24(b) and (c)] in the amplifiers of channel #3 and #1, while the experiment is ended with a pulse S1 (of 9-ns duration) leading to the charging of the sampling capacitors in the CDS of Fig. 10.

The experiment shown in Fig. 24(b) corresponds to the injector terminals IU2–IU5 staying idle (CDAC code = 0) and the electrical field in the structure defined by the dc voltages applied at the terminals IU2/3/4/5 (\(V_{imp} = 0.1\) mV and 0.2 mV). This is the main calibration test. In this test, the QDs QD1 and QD3 stay isolated from the sea of electrons in the QPCs by high potential energy barriers at IU2 and IU5. One expects that the differential measurement in both channels returns (approximately) zero as no charge can be injected into QD1 and QD3 from QPC1 and QPC3. Fig. 25 shows the sweep of voltages \(V_{reset1}\) and \(V_{reset2}\) of the reset (also called precharge) devices. For a given pair of \(V_{reset1}\) and \(V_{reset2}\), the output voltages at the differential voltage detectors buffer outputs are measured. The experiment is repeated 2000 times to obtain the measurement statistics in the form of histograms. The peak of the histogram is coded in a color scale and presented as a heatmap. Indeed, in this calibration test, we measure (effectively) no voltage change at the QPCs. We conclude that the injectors isolate the QD from the QPCs properly.

The test of charge injection is carried out by applying the signal sequence shown in Fig. 24(c) when the injector terminals IU2 and IU5 are pulsed. In the example shown in Fig. 26, a CDAC code of 50 is applied corresponding to a voltage increment of \(50 \cdot \Delta V_{max}/255 = 19.6\) mV (\(\Delta V_{max} = 100\) mV is the maximum pulse range). This voltage pulse is enough to decrease the potential energy barrier from the QPCs to the QDs QD1 and QD3. The heatmap
of the injection test reveals the charge transfer region visible as a blue stripe in Fig. 26. The intensity of the blue color shows the amount of charge injected in the QDs.

The charge injection and charge quantization are controlled by the reset device voltages and the imposer voltages, which are the combination of the dc level $V_{\text{imp}}$ and the CDAC code. The next experiment demonstrates that the combination of the dc levels $V_{\text{imp}}$ and $V_{\text{reset1}}$ controls the charge transfer and the CDAC code controls the amount of charge injected. The heatmap of the charge sensed at the QPC in the plane spanned by $V_{\text{reset1}}$ and the CDAC code is shown in Fig. 27. The color of the heatmap encodes the average voltages sensed on the QPC. The figure presents multiple variations of the heatmap investigating the influence of other experiment parameters, namely, the dc level $V_{\text{imp}}$ held on the injectors and imposers and the delay before the reset phase and the beginning of the experiment. The ‘drain’ voltage of the reset devices was fixed at $V_{\text{reset2}} = -300$ mV.

A number of important features are demonstrated in Fig. 27. First, the dc imposer level $V_{\text{imp}}$ affects the injection as expected. With $V_{\text{imp}}$ increasing, the voltage $V_{\text{reset1}}$ must also be raised to match the Fermi level of the QPC with the energy levels of the QDA. Second, the amount of the injected charge is clearly controlled by the CDAC code and $V_{\text{imp}}$. In particular, we highlight that the CDAC code is responsible for the coupling between the QPC and the QDA as it controls the height of the potential barriers isolating the QDA from the QPC. Applying a larger CDAC codes allows more charge to be injected, as is expected. Third, the average voltages sensed on the QPC (which is proportional to the charge moved to the QDA during the experiment) appear to have quantized increments. As a final note, the result of the experiment does not depend on auxiliary parameters of digital control such as the delay between the reset phase and the beginning of the experiment.

V. CONCLUSION

This article described classical circuitry, monolithically integrated with QDA, that is capable of performing rudimentary operations of reading and setting the QDA quantum states at $\sim 4$ K. The QDA structure intends to house position-based charge qubits that could be massively scaled in the chosen commercial 22-nm FD-SOI process technology. The proposed classical circuitry contains injector and detector sub-blocks that are connected to the QPC node, which is an interface between the quantum and classical domains. The injector circuitry transfers a single electron from the QPC node to the QD structure, while the detector block observes the event. A reset transistor is being used to set and reset the energy level of the QDA. A CDAC is being used for the injector, imposer, and reset device, which must feature very low noise, power consumption, and area. The proposed system is verified through practical experiments. Further characterization of the CDAC has been performed through a loopback configuration with an assistance of the single-electron detector. This, as a result, confirms the functionality of the detector, reset device, and the quantum tunneling into the QD structure.

The proposed system achieves a $0.257$-mV$_{\text{rms}}$ readout noise at $3.4$ K with merely hundreds of microwatts consumed. While the quantum experiments are in progress, it was shown that the injection of charge occurs only when pulses of correct amplitude are applied at the injector terminals when proper precharge voltages $V_{\text{reset1}}$ and $V_{\text{reset2}}$
are selected, which is consistent with the Coulomb blockade effect. While the main focus of this article is on the QDA control circuitry, we demonstrated that charge quantization was observed, signature behavior of QDs, and it was controlled by the interface circuitry, particularly, the combination of $V_{\text{reset}}$, $V_{\text{imp}}$, and CDAC. At the same time, it did not depend on auxiliary parameters of the experiment, as demonstrated by the calibration tests.

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