Robust Qubit Mapping Algorithm via Double-Source Optimal Routing on Large Quantum Circuits

CHIN-YI CHENG, Department of Electrical Engineering, National Taiwan University, Taiwan (R.O.C.)
CHIEN-YI YANG, Department of Computer Science and Engineering, University of California San Diego, USA
YI-HSIANG KUO, Graduate Institute of Electronics Engineering, National Taiwan University, Taiwan (R.O.C.)
REN-CHU WANG, College of Computing, The Georgia Institute of Technology, USA
HAO-CHUNG CHENG, Department of Electrical Engineering and Graduate Institute of Communication Engineering, National Taiwan University, Taiwan (R.O.C.)

Qubit Mapping is a critical aspect of implementing quantum circuits on real hardware devices. Currently, the existing algorithms for qubit mapping encounter difficulties when dealing with larger circuit sizes involving hundreds of qubits. In this paper, we introduce an innovative qubit mapping algorithm, Duostra, tailored to address the challenge of implementing large-scale quantum circuits on real hardware devices with limited connectivity. Duostra operates by efficiently determining optimal paths for double-qubit gates and inserting SWAP gates accordingly to implement the double-qubit operations on real devices. Together with two heuristic scheduling algorithms, the Limitedly-Exhaustive (LE) Search and the Shortest-Path (SP) Estimation, it yields results of good quality within a reasonable runtime, thereby striving toward achieving quantum advantage. Experimental results showcase our algorithm’s superiority, especially for large circuits beyond the NISQ era. For example, on large circuits with more than 50 qubits, we can reduce the mapping cost on an average 21.75% over the virtual best results among QMAP, t\ket, Qiskit and SABRE. Besides, for mid-size circuits such as the SABRE-large benchmark, we improve the mapping costs by 4.5%, 5.2%, 16.3%, 20.7%, and 25.7%, when compared to QMAP, TOQM, t\ket, Qiskit, and SABRE, respectively.

CCS Concepts: • Computer systems organization → Quantum computing; • Hardware → Physical synthesis.

Additional Key Words and Phrases: Quantum Compilation, Qubit Mapping, Scalability, Local Optimal Solution.
INTRODUCTION

The ultimate goal of quantum computing is to outperform the classical algorithms exponentially in solving real-world intractable problems [1], including Quantum Communication [2], Quantum Cryptography [3], and Quantum Machine Learning [4], etc. Recent progress in quantum computing devices has sparked hope for this dream to become a reality. For instance, IBM Condor has reached a milestone of 1,121 qubits, tripling its previous generation, Osprey, from the previous year. This is only about $1/2$ of the 2048 qubits needed for the Quantum Fourier Transform (QFT) to break the RSA-1024 encryption [5, 6], and approximately $1/30$ of the $255 \times 6$ qubits required for the discrete logarithms over elliptic curves (e.g., Curve25519) to solve the Bitcoin encryption [7].

However, the dream of achieving the quantum advantage can be seriously deferred by the “connectivity constraints” of modern quantum computing devices. Taking the *ibmq_washington* quantum computer of which the topology is shown in Fig. 1 as an example, each of its qubits (i.e. a vertex in the graph) is connected to at most three adjacent qubits. Therefore, when a quantum algorithm involves a quantum operation between two non-adjacent qubits, say qubits 0 and 126 at the extreme, we will need a long sequence of swap operations to bring the computation to a pair of adjacent qubits, say qubits 61 and 62. This will significantly increase the demand for the number of qubits and, even worse, lead to a much longer execution time for the quantum circuit. Therefore, intelligently mapping the quantum circuit to the physical qubits, known as the “qubit mapping problem,” will be one of the most crucial steps in achieving the quantum advantage.

The qubit mapping problem involves an initial placement of the logical qubits to the physical ones, and subsequent SWAP insertions to bring the computations of multiple qubit gates to adjacent qubits. The objective is to improve the circuit fidelity. Common approaches include reducing the number of SWAPs and thus optimizing the execution time of the quantum circuit and mitigating the error of each gate and qubit. Siraichi *et al.* [9] have shown qubit mapping to be an NP-complete problem.

Earlier algorithms [10–19] attempted to minimize the number of additional SWAP gates with the mapping of qubits to the Linear Nearest Neighbor (LNN) structure. Booth *et al.* [20] even
transformed the mapping into a mathematical problem and utilized solvers to obtain feasible results. However, modern quantum computing devices in the NISQ era are mostly in lattice structures, which offer higher routing flexibility than the LNN structure. Therefore, the aforementioned approaches could only achieve sub-optimal solutions for the qubit mapping problem.

To realize the qubit mapping on the NISQ devices, Siraichi et al. [9] introduced a straightforward heuristic approach that worked on the lattice structure of the earlier generations of the IBM quantum computers. de Almeida et al. [21] relied on the matrix cost to solve CNOT mappings on IBM QX device. However, as the qubit interaction of these early-day machines is unidirectional, their algorithms are not suitable for modern quantum devices that pose bidirectional qubit interactions. There were studies focusing on reducing depth overheads besides the number of SWAP gates. Venturelli et al. [22] used exhaustive-search temporal planners to schedule gates. Zulehner et al. [23, 24] and Matsuo et al. [25] then proposed a multi-step approach with a depth-based layer partitioning and A* as the underlying search algorithm. Additionally, Peham et al. [26] explored the sub-architectures of the quantum devices in order to devise a suitable initial placement strategy for the qubit mapping problem. Notably, [23] and [26] have been integrated into the QMAP framework [27], which delivered high-quality results for relatively small quantum circuits (less than 50 qubits). However, when applied to larger circuits, QMAP will suffer in lengthier program runtime and thus the mapping outcomes are not as effective.

To counter the solution quality problems of the above-mentioned heuristic-based methods, several researchers proposed methodologies that rendered the exact solution for the optimal result with respect to the number of inserted SWAPs. In addition to the straightforward heuristic approach, Siraichi et al. [9] also presented an exhaustive computation based on the dynamic programming algorithm. However, it comes with the complexity of $O((Q!)^2)$, where $Q$ is the number of qubits, and thus is not applicable for larger quantum circuits. Some other exact-solution approaches formulated the qubit mapping problem into a satisfiability problem. Wille et al. et al. [16, 32] utilized the Satisfiability Modulo Theories (SMT) solver together with the pseudo-Boolean optimizer to minimize the inserted SWAP gates. Tan and Cong [33] constructed a gate-dependency graph and guaranteed optimality for objectives either in circuit depths or SWAP counts via an SMT solver named OLSQ. Their follow-up works, namely OLSQ-GA [34] and OLSQ2 [35], claimed to enlarge the scalability to 54 qubits. Moreover, Molavi et al. [36] utilized maximum satisfiability (MaxSAT) to minimize the mapping cost. However, these exact methods, although being able to achieve optimality for small circuits, are inferior to the heuristic methods in large circuits. It is often that they will abort on large circuits due to the complex exhausting search process.

Another technique to improve the solution quality of the qubit mapping is to define the timing model for distinct gate types so that the mapping cost can better approximate the execution time of the quantum circuit on the real device. Consequently, the optimal qubit mapping solution can ensure the better fidelity of the quantum computation. Deng et al. [37] proposed a timing model for super-conducting devices that defined the timing costs of the single-qubit, double-qubit, and SWAP gates to be 1, 2, and 6 units, respectively. The mapping cost is therefore calculated based on these

\[ \text{SWAP-based BidiREctional heuristic search algorithm} \]
timing costs. They further introduced the concept of lock time for the busy qubits and presented it as the CODAR\(^2\) algorithm to optimize the total circuit execution time. On the other hand, Zhang et al. in [38] adopted a similar timing model\(^3\) and devised an improved algorithm, Time-Optimal Qubit Mapping (TOQM), with estimated cost to achieve better results for the mapping. Lao et al. [39] proposed a Qmap\(^4\) algorithm for Surface-17, a 17-qubit quantum computer. To accommodate the specific controlling mechanism of this device, they imposed frequency constraints into mapping costs and minimized the execution time by exhaustive search on the potential routings. However, their runtime complexity can be as high as \(O(g\sqrt{n}4^{\sqrt{n}})\), where \(g\) and \(n\) are numbers of gates and qubits respectively. Although the above-mentioned algorithms claimed to achieve optimal mapping solutions, the runtime of these algorithms was very long due to the fact that they needed to calculate the costs of all the potential swapping candidates in each iteration when selecting a SWAP. Consequently, they could only handle mapping problems up to 50 qubits, which is much smaller than the number of required qubits for achieving quantum advantage.

This paper introduces a robust qubit mapping framework designed for large circuits with hundreds of qubits and beyond. Our key contributions are two-fold:

1. While many previous approaches such as [37], [38], and [39] have exponential or sub-exponential complexities in finding the optimal SWAP insertion sequence, we propose a qubit mapping framework that decomposes the optimization flow into three components: an \(O(n)\) initial mapping strategy, an \(O(n \log n)\) Duostra router that can guarantee the optimal mapping solution for a given double-qubit gate, and a heuristic scheduler that can either exploit a limited-depth exhaustive search or a shortest-path estimation. The overall algorithm strikes a good balance that it can obtain the near-optimal solution for smaller circuits as well as scale up to handle very large-scale circuits.

2. Unlike other previous algorithms that optimize the mapping solutions by considering static costs derived from the device topologies (e.g. SABRE), our proposed Duostra algorithm dynamically computes the “occupied time” (defined in section 3.2.1) during the finding of the routing paths. It can not only ensure the qubit mapping optimality for a double-qubit gate, but also update the coupling constraints for the other double-qubit gates so that the scheduler can further optimize the mapping for the subsequent routing paths.

The experimental results indicate that in the mid-size test cases within the SABRE-large test suite [28], our approach achieves an average cost improvement by 4.5%, 5.2%, 16.3%, 20.7%, and 25.7%, when compared to QMAP, TOQM, t\(|ket\rangle\), Qiskit, and SABRE, respectively. Additionally, those results are generated within a runtime of 5 minutes. Regarding scalability, Duostra surpasses IBM Qiskit, QMAP, t\(|ket\rangle\), and SABRE on mapping cost for most large quantum circuits, including Galois Field (GF), inst, classical Electronic Design Automation (EDA) benchmark circuits [40], adder, and qugan. Our framework exhibits an average improvement of 21.75% over the best results among IBM Qiskit, QMAP, t\(|ket\rangle\), and SABRE across 39 large circuits (i.e. qubits > 50), with nearly the shortest runtime. Furthermore, our method can handle problem sizes up to 11,969-qubit QFT within 3 hours (with time complexity \(O(n^{2.8})\), where \(n\) denotes the numbers of qubits). In summary, our proposed qubit mapping framework offers a solution for large-scale quantum circuits by efficiently implementing local-optimal quantum algorithms on a non-fully connected quantum device.

The rest of the paper is organized as follows. We first explain the qubit mapping problem in Section 2. The proposed framework is detailed in Section 3, and specifically the proof for the optimality of the Duostra algorithm is provided in Section 4. We present the experiment results in...
Section 5, and conclude the paper in Section 6. The source code\(^5\) of our method is embedded in the tool Qsyn [41].

### 2 QUBIT MAPPING PROBLEM

The qubit mapping problem is to schedule the operations of a quantum circuit and then assign them to the qubits of a quantum computer with a given topology (e.g. Fig. 1). The circuit is composed of gates from a quantum cell library (e.g. Clifford+T library). However, we need to insert additional SWAP gates to bring the inputs, which are logically connected but physically apart, of a double-qubit gate to the adjacent qubits. This is because the computation of a double-qubit gate can only be applied on adjacent qubits on the actual hardware device (called "coupling constraint"), and the topology of the physical device often limits its qubits to interact with only a small number of adjacent neighbors (e.g. 1 to 3 for ibmq_washington quantum computer as shown in Fig. 1).

Taking Fig. 2 as an example of the qubit mapping problem, we denote the logical qubits (i.e. the qubits for a quantum circuit) in lowercase as \(q_0\) to \(q_6\) in Fig. 2a, and the physical qubits (i.e. the qubits on the actual device) in uppercase as \(Q_0\) to \(Q_7\) in Fig. 2b. Let’s assume that after the initial mapping, the inputs of the double-qubit gate \(G_5\), that is, \(q_1\) and \(q_2\), are mapped to two non-adjacent physical qubits, \(Q_1\) and \(Q_6\) (explained later in Section 3.1 for details). We can insert SWAPs along a path, for example, \(Q_2, Q_3, Q_4, Q_5, Q_6\), to bring these two inputs to adjacency. Clearly, there is another path \(Q_2, Q_1, Q_0, Q_7, Q_6\) to resolve the coupling constraint of \(G_5\). By choosing one of these two paths, we will employ different numbers of SWAPs and thus relocate the inputs of the subsequent double-qubit gates \(G_6\) and \(G_7\) to different physical qubits. This will lead to different execution time of the circuit and therefore different error probabilities.

A SWAP is composed of three consecutive CX gates, where the middle CX possesses opposite control and target qubits with respect to the other two CX gates. The insertion of the SWAP gates greatly increases the gate counts and execution time of the quantum circuit. Therefore, the objective

\(^5\)https://github.com/DVLab-NTU/qsyn
\(^6\)Without loss of generality, we assume there are only single- and double-qubit gates in the quantum cell library.
of the qubit mapping problem is to optimize the scheduling and mapping of the logical cells to the physical qubits and thus minimize the gate counts, execution time, and the resulting computing errors.

To illustrate our qubit mapping framework in the next section, we first introduce four definitions to facilitate the design of the qubit mapping algorithm:

**Definition 2.1 (Dependency Graph (DepG)).** A graph that describes the computational dependency of the double-qubit gates in the quantum circuit. For the qubit mapping problem, since the single-qubit gates will never violate the coupling constraints, we only need to consider the double-qubit gates for SWAP insertions to bring their input qubits to the adjacencies. In a Dependency Graph, an edge \( \text{Gate}_i \rightarrow \text{Gate}_j \) means that \( \text{Gate}_j \) depends on \( \text{Gate}_i \). A gate can be executed only after all of its parents are executed.

Take Fig. 2a as an example, the gate \( \text{G}_4 \) operates on two qubits, \( q_1 \) and \( q_2 \). It can only be executed after all the previous gates (i.e. \( \text{G}_1 \) and \( \text{G}_3 \)) are executed. We say \( \text{G}_4 \) depends on \( \text{G}_1 \) and \( \text{G}_3 \), and add edges from \( \text{G}_1 \) and \( \text{G}_3 \) to \( \text{G}_4 \) to build a directed acyclic graph (DAG), called Dependency Graph as shown in Fig. 2c.

**Definition 2.2 (Device Graph (DevG)).** An undirected graph \( \text{DevG} = (V, E) \) represents the topology of a real quantum computing device, where \( V \) denotes the physical qubits and \( E \) is the set of edges corresponding to the connectivity among physical qubits. A pair of qubits can be involved in the double-qubit operation only if there is a direct connection between these two qubits. In the qubit mapping problem, if a double-qubit operation is mapped to two non-adjacent physical qubits, we need to find a path between these two qubits on DevG to perform SWAPs.

**Definition 2.3 (Waitlist).** Similar to the “front layer” concept in [28], Waitlist is a list of gates that are ready for execution. That is, gates in a Waitlist are those without any unexecuted parents in the Dependency Graph.

For example, in Fig. 2, if \( \text{G}_2 \) and \( \text{G}_3 \) were executed, then \( \text{G}_1 \) is the only gate in the Waitlist. Since gates should be executed following the Dependency Graph, gates in the Waitlist are the only candidates when scheduling for the next execution.

**Definition 2.4 (Ideal Circuit Cost and Mapping Cost).** CODAR [37] notes that the execution time of single-qubit and double-qubit gates is different. To simplify calculations, Deng et al. introduce a model in which single-qubit gates occupy one unit of time and double-qubit gates occupy two units. Using this model, we compute two metrics: Ideal Circuit Cost and Mapping Cost. The Ideal Circuit Cost is derived from the logical circuit before SWAP operations, providing an indication of the circuit’s inherent complexity and its performance on a fully connected quantum device. In contrast, Mapping Cost is calculated based on the physical circuit with SWAP insertions taking up six units each. Mapping Cost reflects the time needed for quantum devices to execute the physical circuit. Our subsequent research aims to minimize the Mapping Cost.

### 3 THE PROPOSED QUBIT MAPPING FRAMEWORK AND ALGORITHM

Our proposed qubit mapping framework is shown in Fig. 3. Unlike previous studies which treat the qubit mapping problem as a whole, we propose a framework that decomposes the problem into two manageable subproblems – routing, and scheduling. We start by quickly placing the circuit inputs to certain physical qubits, called initial placement, and from there, we have the first set of gates in the Waitlist. While the Router can efficiently suggest a routing path that minimizes the execution time of a double-qubit gate on a real device, the Scheduler now only needs to consider the order of the gates for execution in the Waitlist. This framework offers flexibility in choosing
specific scheduling and routing heuristics with different metrics for different quantum circuits. Below we present our design of algorithms.

### 3.1 Initial Placement

The initial placement step assigns the circuit inputs to specific physical qubits. In our framework, we employ a depth-first search (DFS) strategy for the initial placement. The primary objective of the DFS placement is to ensure that the two input qubits required by each gate are situated in close proximity to each other.

![Fig. 3. Our qubit mapping framework](image)

| qubit | adjacency list |
|-------|----------------|
| $q_0$ | $q_1$ $q_6$   |
| $q_1$ | $q_0$ $q_4$ $q_2$ |
| $q_2$ | $q_1$         |
| $q_3$ | $q_4$ $q_6$   |
| $q_4$ | $q_3$ $q_1$   |
| $q_5$ | $q_6$         |
| $q_6$ | $q_5$ $q_3$ $q_0$ |

(a) Adjacency lists of the circuit in Fig. 2a

![Fig. 4. An example of the initial placement strategy for the circuit in Fig. 2](image)

This strategy attempts to first sort the logical qubits in a depth-first-search (DFS) order and then map them to the physical qubits according to the DFS order on the Device Graph. Algorithm 1 shows the procedure of sorting the logical qubits in the DFS order on the quantum circuit. Let’s use the circuit on Fig. 2a again as an example. Assume the list of the double-qubit gates (i.e. DQG) are initialized to $G_1$, $G_2$, $G_3$, $G_4$, $G_5$, $G_6$, $G_7$. We will first pick $G_1$ (Line 3) and one of its inputs $q_3$ (Line 4) to call the **DFS_RECUR** subroutine (Line 5). In the subroutine, $q_3$ will be added to DFS (Lines 11-14) and, $q_4$, the first qubit on the adjacency list of $q_3$, will be passed to the recursive call (Line 17). Continuing with this pre-order traversal procedure, we can derive the DFS order of the logical qubits as \{q_3, q_4, q_1, q_0, q_6, q_5, q_2\}. On the other hand, the DFS order of the physical qubits in Fig. 2b can be easily computed as \{Q_0, Q_1, Q_2, Q_3, Q_4, Q_5, Q_6, Q_7\}. Therefore, the initial qubit mapping will be \{(q_3, Q_0), (q_4, Q_1), (q_1, Q_2), (q_0, Q_3), (q_6, Q_4), (q_5, Q_5), (q_2, Q_6), ( , Q_7)\}, as shown in Fig. 4b.
Note that with this approach, the inputs of the first three double-qubit gates $G_1, G_2, G_3$, and even the fourth double-qubit gate $G_4$, will be placed in adjacency (i.e. $(Q_0, Q_1), (Q_5, Q_4), (Q_3, Q_2)$, and $(Q_2, Q_1)$). Therefore, no SWAP insertion is needed. However, for the next double-qubit gate $G_5$, although its inputs seem next to each other in the circuit (i.e. $q_1$ and $q_2$), they are apart in terms of the physical qubits (i.e. $Q_2$ and $Q_6$) and thus a sequence of SWAP insertions will be performed.

Clearly, the closeness of the inputs of the subsequent double-qubit gates (i.e. $G_6$ and $G_7$) will be affected by the SWAP insertions of $G_5$. Therefore, it is impossible for the initial placement strategy to ensure the overall optimality of the qubit mapping problem. Our observation indicates that initial placement tends to play a more pivotal role in shallow circuits, where the qubits interact only with a limited number of others. However, as the circuit complexity grows, the influence of the initial placement is confined to the first few “layers” before swapping paths disturbing the initial placement, and thus the routing and scheduling strategies begin to exert a more dominant influence on the final outcome. We examine our speculation in Section 5.2.

**Algorithm 1 DFS_TRAVERSAL**

```
1: procedure DFS_TRAVERSAL(DQG)  \text{> $DQG$ denote the list of double-qubit gates}
2:     $DFS = \emptyset$
3:     for gate $\in DQG$ do
4:         for $q \in$ gate do
5:             DFS_RECUR($q, DFS$)  \text{> $q$ is the input qubit}
6:         end for
7:     end for
8:     return DFS
9: end procedure
10: procedure DFS_RECUR($q, DFS$)
11:     if $q$ is visited then
12:         return
13:     end if
14:     $q \rightarrow$ setVisited()
15:     $DFS \leftarrow q$
16:     for $q' \in q.\text{adj\_list}$ do
17:         DFS_RECUR($q', DFS$)
18:     end for
19: end procedure
```

### 3.2 Routing: Duostra (Dual-source Dijkstra)

In this paper, we present a novel routing algorithm called Duostra (Dual-source Dijkstra) for handling a double-qubit gate that operates on physically distant qubits. The algorithm outputs an optimal routing path and provides a SWAP sequence that efficiently brings the two involved qubits, of a double-qubit gate, adjacent to each other. Additionally, we demonstrate that the time complexity of this algorithm is $O(n \log n)$, where $n$ represents the number of qubits in the quantum device.

In the following, we first introduce two important terminologies, “occupied time” and “routing path”, for our routing algorithm. We then describe the main novelty of the routing procedure and present the details of the algorithm in the end.
3.2.1 Terminologies.

**Definition 3.1 (Occupied Time).** We have adopted the concept introduced in [37] to define the notion of “occupied time” for a qubit. When a physical qubit is involved in an operation, such as SWAP or CX, it is considered occupied. If an operation is carried out on a physical qubit \( Q_n \) from time \( t_0 \) to \( t_1 \), we define the occupied time of \( Q_n \) as the finishing time of that operation, denoted as \( Q_n.ocep = t_1 \). This means that the qubit cannot be assigned to another operation until time \( t_1 \).

We further extend the concept of occupied time to the edge of the Device Graph. Let \( e(i, j) \) be an edge that connects two adjacent qubits \( Q_i \) and \( Q_j \) on \( DevG \). Applying a SWAP gate on this edge will swap the logical qubits that \( Q_i \) and \( Q_j \) applied on. We then calculate the occupied time for the edge with or without applying SWAP by:

\[
e(i, j)_{\text{swap}.ocep} = \max(Q_i.ocep, Q_j.ocep) + \tau_{\text{swap}} \quad \text{with SWAP} \quad (1)
\]

\[
e(i, j).ocep = \max(Q_i.ocep, Q_j.ocep) \quad \text{without SWAP} \quad (2)
\]

where \( Q_i.ocep, Q_j.ocep \) and \( \tau_{\text{swap}} \) represent the occupied time of \( Q_i \), occupied time of \( Q_j \), and the operating time for a SWAP gate (i.e. 6 units as defined in [37]).

**Definition 3.2 (Routing Path).** In the context of a source qubit \( Q_s \) and a distant target qubit \( Q_t \), we represent the routing path \( RP(s, t) \) as a pathway from \( Q_s \) to \( Q_t \), which involves a sequence of SWAP operations applied along the edges of this path.

Let \( Q_1, Q_2, ..., Q_n \) be the \( n \) qubits between \( Q_s \) and \( Q_t \) along the routing path \( RP(s, t) \). In other words, \( Q_i \) and \( Q_{i+1} \) for \( i \) between 1 and \( n-1 \), and \( Q_n \) and \( Q_t \) are all adjacent. With Eq. (1), we can recursively calculate the occupied time of a routing path as

\[
RP(s, t).ocep = \max(RP(s, n), e(n, t)_{\text{swap}.ocep})
\]

\[
= \max(\max(RP(s, n-1), e(n-1, n)_{\text{swap}.ocep}), e(n, t)_{\text{swap}.ocep}) = ..., \]

where \( e(n-1, n) \) and \( e(n, t) \) are adjacent edges between \( Q_{n-1} \) and \( Q_n \), and \( Q_n \) and \( Q_t \), respectively.

During the computation of the occupied time for a routing path, the occupied time of the qubits along that path is updated accordingly.

To illustrate this concept, we proceed with the example outlined in Section 3.1. After initial mapping, we can execute the single-qubit gates (i.e. H, Z, S, X, T) and the two-qubit gates G1, G2, G3, and G4 without the need of SWAP insertions. The occupied time for the physical qubits after the executions is illustrated in Fig. 5a and according to the dependency graph in Fig. 2c, we have the double-qubits gates G5 and G6 on the Waitlist. Let’s assume we pick G6 for the next execution. Since its inputs are now placed on two non-adjacent qubits \( Q_0 \) and \( Q_4 \), we need to find a routing path to bring them to adjacency.

If we choose \( Q_0 \) as the source and \( Q_4 \) as the target, we observe that the SWAPs can be performed along two distinct paths: \((Q_0, Q_1, Q_2, Q_3, Q_4)\) or \((Q_0, Q_7, Q_6, Q_5, Q_4)\). The occupied time for both of these routing paths and their corresponding qubits is calculated as in Fig. 5b. Upon analysis, we find that the occupied time of the path \((Q_0, Q_1, Q_2, Q_3, Q_4)\) (i.e., 29) is greater than that of the path \((Q_0, Q_7, Q_6, Q_5, Q_4)\) (i.e., 27). As a result, in our efforts to optimize the execution time of the quantum circuit, we can disregard the former path for future considerations. In general, when dealing with a source qubit \( Q_s \) and a target qubit \( Q_t \), their optimal routing path is denoted as \( RP_{opt}(s, t) \). For this specific example, \( RP_{opt}(0, 4) = 27 \).

It is important to note that if we interchange the roles of the source and target qubits for \( Q_0 \) and \( Q_4 \), the occupied time for the routing path and qubits will differ. In Fig. 5c, we present the calculation of the occupied time for the routing paths and qubits when taking \( Q_4 \) as the source.
and $Q_0$ as the target. Notably, $RP_{opt}(4, 0)$ is found to be 28, which is larger than $RP_{opt}(0, 4)$ (i.e. 27). Therefore, choosing $Q_0$ as the source and $Q_3$ as the target proves to be the more favorable routing path.

Furthermore, if we treat both $Q_0$ and $Q_4$ as sources and search for two routing paths ($Q_0$ to $Q_4$ and $Q_4$ to $Q_0$) between them, we can observe that when both routing paths converge at the edge
e(5, 6), an optimal routing path with a minimal occupied time of 15 is achieved (Fig. 5d). In simpler terms, by swapping the logical qubits on Q₀ to Q₅ and on Q₄ to Q₁, we can bring the computation of the double-qubit gate to a pair of adjacent qubits and attain the most optimal qubit mapping for it. This leads us to the dual-source routing algorithm, named “Duostra,” as depicted below:

Given a double-qubit gate that operates on two physically remote qubits (i.e. the sources) Q₀ and Q₅, the Duostra algorithm aims to find a pair of adjacent qubits (i.e. the targets) Q₀ and Q₅ on the Device Graph in such a way that the maximum of \( R_{\text{opt}}(s₀, t₀) \cdot \text{ocp} \) and \( R_{\text{opt}}(s₁, t₁) \cdot \text{ocp} \) can be minimized. That is:

\[
\min_{e \in E} (\max(\text{\#1}, \text{\#2}, \text{\#3})).
\]

\[\text{(3)}\]

3.2.2 The novelty of Duostra algorithm. The Duostra algorithm is a modified version of the classic shortest-path finding algorithm, i.e. the Dijkstra’s algorithm [42], with the key differences in traversing the search tree from dual sources and dynamically updating the availability of nodes (i.e. the occupied time of the physical qubits) during the search. Let’s continue the qubit mapping for the previous example. After we apply SWAPs between (Q₀, Q₇), (Q₇, Q₅) and (Q₅, Q₄), the double-qubit gate G6 can now be executed on the adjacent physical qubits (Q₀, Q₅). At the same time, the inputs of the other double-qubit gate G5 are thereby swapped to Q₇ and Q₂, and the occupied time of the physical qubits are then updated as depicted in Fig. 6a.

Note that if we apply the traditional shortest path approach to resolve the coupling constraint of G5, it is intuitive that we will execute a SWAP between Q₀ and Q₇, and another SWAP between Q₁ and Q₂. This will lead to the occupied time 21 as a result.

However, if we perform the Duostra algorithm, as shown in Fig. 6b, by considering and dynamically updating the occupied time of the qubits on the routing path, we will keep one of the sources unmoved on Q₇, and swap the other source from Q₂ to Q₀. This will generate the optimal mapping with the occupied time 17.

To further elucidate the differences above, let’s compare the number of SWAPs executed on the edges by the Duostra and the traditional Shortest-Path (SP) algorithms as in Fig. 7. The result on the benchmark circuit cm42a_207 shows that the SWAP operations by the SP algorithm are not applied uniformly. It has the standard deviation 67.00 and the maximum number 178. On the other hand, Duostra renders a much balanced distribution of the SWAP operations. Its standard deviation is 35.26 and the maximum number is 112. This discrepancy suggests that Duostra tends to choose the routing path with smaller occupied time and thus yield more balanced and parallel results. It can thereby reduce the mapping cost.

3.2.3 Detailed description of the algorithm. We present the pseudo-code of the Duostra algorithm in Algorithm 2 below. To begin, we initialize a priority queue, PQ, and mark all vertices \( v \in V \) as unseen and unvisited. The input sources of the routing problem, \( s₀ \) and \( s₁ \), are then marked as seen and visited. For each vertex \( v \), we utilize a field \( v\cdot \text{source} \) to indicate its routing source. As there are only two possible routing sources, \( s₀ \) and \( s₁ \), we set the routing sources of \( s₀ \) and \( s₁ \) as themselves (Lines 2 and 3). Subsequently, we add all the adjacent vertices of \( s₀ \) and \( s₁ \) to PQ, updating their occupied time, marking them as seen, and recording their sources as either \( s₀ \) or \( s₁ \) (Lines 5 and 6).

Next, we proceed iteratively by selecting the vertex with the smallest occupied time, \( m \), from PQ and marking it as visited (Lines 8 and 9). If there exists an adjacent vertex \( v \) of \( m \) that has been visited and is routed from the other source different from \( m\cdot \text{source} \) (Line 10, i.e. \( v\cdot \text{source} \neq m\cdot \text{source} \)), then we conclude the procedure and establish an optimal routing solution. This solution includes the optimal routing path from \( m\cdot \text{source} \) to \( m \) (i.e. \( R_{\text{opt}}(m\cdot \text{source}, m) \)), the optimal routing path

\[\text{We increment the occupied time for Q}_₅ \text{and Q}_₇ \text{by 2 due to the execution of the CX gate.}\]
Fig. 7. Heat graphs of SWAP counts for each edge between different routers on benchmark cm42a_207 and device ibmq_guadalupe. Both of them are normalized to the same gradients.

Algorithm 2 Duostra (Dual-source Dijkstra)

1: procedure DUOstra(Graph, s₀, s₁)
2:   s₀.source ← s₀
3:   s₁.source ← s₁
4:   PQ ← priority queue
5:   pushUnseenNeighbors(PQ, s₀)
6:   pushUnseenNeighbors(PQ, s₁)
7: while PQ is not empty do
8:   m ← nodeWithLowestCost(PQ)  \(\triangleright\) Cost is the occupied time of the vertex
9:   m.visited ← True
10: if \(\exists\) visited neighbor v s.t. m.source \(\neq\) v.source then
11:   RP(m.source, m) ← backtrace(m)
12:   RP(v.source, v) ← backtrace(v)
13: return \(\langle path_{s₀}, path_{s₁} \rangle\)
14: end if
15: pushUnseenNeighbors(PQ, m)
16: end while
17: end procedure
18: procedure pushUnseenNeighbors(PQ, m)
19:   for v ∈ Neighbor(m) and v.unseen do
20:     v.source ← m.source
21:     v.seen ← True
22:     PQ.push(v)
23:   end for
24: end procedure

from v.source to v (i.e. \(R_{opt}(v.source, v)\)), and the edge \(e(m, v)\) (see Section 4 for the proof of the optimality of the Duostra algorithm). Otherwise, we add all the unseen neighbors of m to PQ and continue with the iteration. Since the Duostra algorithm can be viewed as a Dual-source Dijkstra algorithm with dynamic occupied time as the cost function, the algorithm has the time complexity \(O(n \log n)\), where n represents the number of physical qubits.
It is noteworthy that there is no need to maintain separate priority queues for the search trees originating from the dual sources $s_0$ and $s_1$. Instead, all seen vertices can be recorded in a single priority queue, irrespective of whether their sources are $s_0$ or $s_1$. As we define the cost of a seen vertex $v$ in the priority queue as the occupied time of the optimal routing path from $v.source$ to $v$, the top vertex in the priority queue, with the lowest cost, represents the earliest qubit that can be operated using a SWAP gate.

Furthermore, once a vertex is pushed into the priority queue, its cost remains unchanged. As a result, we can ensure that when the two search trees from $s_0$ and $s_1$ converge at a pair of adjacent physical qubits, they will indeed form the optimal routing path with the smallest occupied time. This is because if there were an alternative sequence that could be completed earlier, it would have been visited from the priority queue and halted the search process earlier. The proof of the optimality of the priority queue is provided in Section 4.1.

3.3 Scheduling: Limitedly-Exhaustive (LE) Search and Shortest-Path (SP) Estimation

Given a quantum circuit, the scheduler plays a crucial role in determining the optimal execution sequence of the gates on the quantum computing device, with the objective of optimizing the total execution time or achieving other specific goals. It is important to note that, at any given moment, we have the flexibility to select any gate from the Waitlist for the subsequent execution and then employ the Duostra algorithm to find the most optimal routing path.

Once a gate is executed and SWAPs are performed, the occupied times of the relevant qubits are updated, and the subsequent gates on the Dependency Graph are added to the Waitlist. This procedure refers to the scheduler routine, as shown in Fig. 3. Since different execution orders can lead to varying total execution time, to attain the global optimum of the scheduling problem, we must consider all possible execution sequences of the gates (i.e., different gate selections from the Waitlist). However, this exhaustive enumeration proves to be an intractable task [9], even for relatively small-scale quantum circuits.

In this paper, we propose two heuristic approaches that adopt different subsets of the execution sequences at each step when choosing the gate to route for subsequent execution. These heuristic methods provide practical and effective strategies for addressing the scheduling problem in the context of quantum circuits.

3.3.1 Limitedly-Exhaustive (LE) Search. As exhaustively enumerating all possible gate sequences on the Dependency Graph proves to be exponentially costly, we introduce a Limitedly-Exhaustive Search approach to constrain the search depth for each decision. In this method, the user specifies a depth limit $d$, and the search process focuses on exhaustively exploring all depth-$d$ sequences originating from any gate in the Waitlist. For each of these depth-$d$ sequences, the Duostra routing algorithm is utilized to calculate their corresponding occupied time.

The scheduler then proceeds to select the sequence with the minimal occupied time, determining its corresponding gate in the Waitlist for execution. Subsequently, the Waitlist is updated, and the process is repeated for the subsequent depth-$d$ sequences. To illustrate, if the depth limit is set to 2, the Limitedly-Exhaustive Search will first enumerate all the gates in the Waitlist, finding the optimal routing path for each gate using Duostra, and updating the corresponding occupied time and Waitlists accordingly. Next, for each gate in the previous iteration and its updated Waitlist, the gates in the updated Waitlist are enumerated, and the above process is repeated again. Finally, the gate that results in the smallest occupied time among these depth-2 sequences will be selected for execution, and the Limitedly-Exhaustive search process will be restarted. This approach offers an efficient strategy to tackle the scheduling problem by limiting the search depth while reducing computational complexity.
3.3.2 Shortest-Path (SP) Estimation. While the Limitedly-Exhaustive (LE) Search heuristic may provide an approximation close to the global optimum solution when employing a large search depth $d$, its practical applicability remains limited due to the extensive calculations involved in the path enumeration. Consequently, it can only be effectively applied to small-scale designs. To address this challenge and being inspired by Li et al. [28], we propose an alternative heuristic approach that considers the concept of the shortest path [43] between the physical qubits of the gate.

The SP-Estimation goes through all the gates in the Waitlist and selects the one with the minimal value of this equation:

$$
\max(g_i.Q_i,ocp, g_i.Q_j,ocp) + c \cdot SP(g_i.Q_i, g_i.Q_j),
$$

where $g_i$ is a double-qubit gate from the Waitlist, $g_i.Q_i$ and $g_i.Q_j$ denote its current qubit assignments, $SP(g_i.Q_i, g_i.Q_j)$ indicates the shortest path between these qubits, and $c$ is a constant factor to take the execution time of the shortest path into consideration. In our implementation, we set $c$ to be 1.

After selecting a gate with a minimal value of Eq. (4) from the Waitlist, we employ the Duostra algorithm to calculate the occupied time of the circuit, and then continue with the updated Waitlist.

It is essential to emphasize a significant difference between the Duostra routing path and the shortest-path routing path. If we were to directly choose the shortest path as the routing path, collisions may occur where the route conflicts with the swaps of another gate. This situation would force us to pause the swapping procedure, leading to a prolongation of the execution time. On the contrary, the Duostra algorithm takes into account the occupied time of each qubit, allowing it to avoid busy routes and efficiently achieve the optimal path for the gate. This distinction is critical in optimizing the overall Mapping Cost (c.f. Section 2.4) of the quantum circuit, see experiments in Section 5.5. Therefore, given the shortest path, we still need to rely on the Duostra router to produce the local optimal result.

The time complexities of the LE Search approaches and the SP Estimation are $O(N^2n)$ and $O(N(W + R))$, respectively. Here, $N$ represents the number of gates in the circuits, $W$ is the number of gates in the Waitlist, $R$ stands for the time complexity of the router, and $n$ indicates the number of qubits.

In summary, the LE Search approach explores all possible gate sequences up to a specified depth $d$. It has the capability to close in on global optimum solutions for smaller designs when the depth $d$ is set sufficiently large. Conversely, the SP Estimation approach prioritizes better scalability, even if it may sacrifice some performance. As a result, the SP Estimation approach can be effectively applied to larger circuits, thus paving the way toward achieving quantum advantage.

### 4 PROOF OF DUOSTRA OPTIMALITY

We design the Duostra Algorithm by capitalizing on the property of local optimality in order to strike a balance between the mapping cost and the program runtime for large circuits. Given a double-qubit gate whose control bit is not adjacent to its target bit, Duostra Algorithm can generate a SWAP sequence with minimum Mapping Cost. We will prove the Duostra Optimality as follows.

In our model, physical qubits are represented as vertices, and given a vertex $v_i$, the parent $v_{p_i}$ of $v_i$ is the vertex adjacent to $v_i$ with the smallest occupied time. In other words, $v_{p_i}$ is the previous vertex of $v_i$ in the routing path. Thus, according to Eq. (1), the occupied time of $v_i$ under the condition of the swap edge $e(v_i,v_{p_i})_{swap}$ can be calculated as:

$$
v_i.ocp|_{e(v_i,v_{p_i})_{swap}} = \max(v_i.ocp, v_{p_i}.ocp) + \tau_{swap}.
$$

In our Duostra Algorithm as presented in Algorithm 2, the vertices are categorized into three types: visited ($t$), seen ($s$), and unseen vertices ($u$). Both seen and unseen vertices are all unvisited.
We call the control and the target bits of the double-qubit gate the routing sources. At first, we mark the routing sources as visited, and their adjacent vertices as seen. During each iteration of the algorithm, we select a vertex from the set of seen vertices and mark it as visited. Following this, the unseen vertices connected to the chosen visited vertex are then labeled as seen.

**Lemma 4.1.** The seen set contains the unvisited vertex with the minimum occupied time

We prove lemma 4.1 as follows. Since an unseen vertex \( u_j \) must be connected to the seen set \( S \) by at least one edge, let the seen vertex connect through this edge be \( s_{arb} \), and we can calculate \( u_j.ocp \) after applying the SWAP gate by Eq. (5) as

\[
    u_j.ocp|_{e(u_j,s_{arb})_{swap}} = max(u_j.ocp,s_{arb}.ocp) + \tau_{swap}
\]

Based on Eq. (6), we observe that as long as there is one edge between \( u_j \) and the seen set, it would lead to \( u_j.ocp|_{e(u_j,s_{arb})_{swap}} > s_{arb}.ocp \). Therefore, since the occupied time of any seen vertex \( (s_{arb}.ocp) \) is greater than or equal to the minimum occupied time of all the seen vertices, the occupied time of an unseen vertex will inevitably be greater than the vertex with the smallest occupied time in the seen set.

We can turn to prove the Duostra Optimality with lemma 4.1. In the routing problem, our objective is to find the best edge \( e^* \) between the best adjacent pair, \( v_0^* \) and \( v_1^* \), which minimizes the objective function, defined in Eq. (3),

\[
    e(v_0^*,v_1^*)_{swap} = max(RP(r_0,v_0^*).ocp,RP(r_1,v_1^*).ocp),
\]

where \( r_0 \) and \( r_1 \) are the given routing sources. To minimize the objective function, we compare the occupied time of all the seen vertices generated by the two routing paths and select the vertex with the minimum occupied time. This vertex will prolong one of the routing paths. Therefore, by iteratively searching for the optimal solution, we come to the Duostra Optimality.

**Lemma 4.2 (Duostra Optimality).** The first edge where the two routing paths converge is the solution \( e^* \), which has the smallest occupied time.

We prove the lemma 4.2 by contradiction. Suppose Duostra Algorithm identifies a sub-optimal edge \( e^- \) with two vertices, \( v_0^- \) and \( v_1^- \), then the occupied time of \( e(v_0^-,v_1^-)_{swap} \) will be:

\[
    e(v_0^-,v_1^-)_{swap} = max(RP(s_0,v_0^-).ocp,RP(s_1,v_1^-).ocp) > max(RP(s_0,v_0^*).ocp,RP(s_1,v_1^*).ocp).
\]

Because we only prolong the routing paths by selecting a vertex with the minimum occupied time, the sub-optimal solution \( e^- \) with the bigger occupied time must be found after the optimal solution \( e^* \). As a result, Duostra Algorithm finds the optimal solution given a double-qubit gate, thus ensuring efficient and effective qubit mapping in quantum circuits.

## 5 EXPERIMENTAL RESULTS

In this section, we first present our experiment setup and an experiment to testify to the significance of initial placement. Following that, we respectively demonstrate experiments on mid-size circuits to showcase our robustness on both Mapping Cost and runtime, on large circuits to witness the scalabilities, and on extra-large circuits to prove our readiness for future quantum advantage. We conducted all experiments on a 13th Gen Intel® Core™ i9-13900K with a total of 126G memory.

### 5.1 Experiment Setup

#### 5.1.1 Compared Methods

We adopt four existing tools for the comparison in our experiments, namely QMAP [27], TOQM [38], t|ket⟩ [44], and IBM Qiskit [45] (version 1.0.1) with default and SABRE mappers. For QMAP and TOQM, we use their heuristic versions because the exact versions...
are impractical for our experiments, as it takes them over a day to generate the mapping results. On the other hand, to ensure the fair comparison of the qubit mapping results, we set the optimization level of Qiskit to 0 so that it will not perform additional circuit optimization. Other than these four tools, we also implement a baseline version of our framework by replacing the Duostra router with a shortest-path router, which directly takes the shortest path as the swap path.

5.1.2 Addressing the connectivity challenges across the NISQ era and beyond. Our proposed qubit mapping framework is not limited to specific devices in NISQ era. However, based on current knowledge, maintaining a low average node degree in superconducting quantum devices, typically less than three, is crucial to minimize frequency collisions and crosstalk errors [46]. For example, IBM’s 433-qubit Osprey proposed in 2022 and the 1121-qubit Condor unveiled in 2023 adhere to the heavy-hexagon topology. Therefore, we opt for the heavy-hexagon structure in our experiment setup to align with the current understanding of the connectivity issues, although our research is not confined to the hexagon topology.

Looking ahead to the era beyond NISQ, if the qubit fidelity improves sufficiently, we can directly address the qubit mapping problem when executing the quantum circuits on the quantum devices. Therefore, our algorithm can continue to prevail. However, if the quantum error correction codes (QECC) are needed, we can view the quantum error correction as an amalgamation of the correction code circuit and the underlying logical circuit and handle the qubit mapping problem as if on a larger interconnected circuit. It will still be important to determine the optimal routing path of any two-qubit gates under the QECC mechanism, and we believe that our robust qubit mapping strategy on large-scale circuits will become imperative.

5.1.3 Target Topologies. Our experiments are based on the architectures of a series of IBMQ machines including the 16-qubit Guadalupe, 27-qubit Kolkata, 65-qubit Brooklyn, 127-qubit Washington, 433-qubit Osprey and 1121-qubit Condor. Furthermore, to emulate devices beyond 1121-qubit, we adopt the heavy-hex pattern from the existing IBM machines [47] and extrapolate the topology up to a remarkable 11,969-qubit, allowing us to assess the scalability of our algorithm thoroughly. These emulated devices are 2,129, 3,457, 5,105, 7,073, 9,361, and 11,969 physical qubits.

There are two limitations, imposed by the characteristics of the IBMQ machines, to our experiments. First, with the designated qubit counts of the machines, we have to select the smallest available device that can accommodate the size of the circuit. For example, for the circuit with 256 logical qubits, we will map it to the topology with 433 physical qubits. Second, since IBMQ does not support control-rotation and Toffoli gates, we have to decompose these complex gates into their fundamentally-equivalent counterparts, as depicted in Fig. 8.

5.1.4 Benchmarks. To assess the different superior aspects of our framework, including performance, scalability, and futurism, we employ distinct sets of benchmarks in our evaluations.

Firstly, for the performance assessment, we focus on the circuits that are big enough so that the optimum solution can not be acquired by the exact approach such as OLSQ2 [35], and are smaller
Fig. 9. Mapping result on all benchmarks in QMAP [27]. With the ideal cost growth, the improvement of Duostra grows.

enough so that the compared methods (c.f. Section 5.1.1) can all generate meaningful results with heuristics. The chosen benchmark consists of circuits proposed in SABRE-large [28], along with its extended form as presented by Wille et al. (QMAP8) [27]. These circuits constitute a subset9 of RevLib [49] and have been decomposed into single- and double-qubit gates. They are up to 185,000 gates and are no more than 16 qubits.

Secondly, for our scalability experiments, we either concentrate on the circuits with the scalable and repeatable architectures, such as Quantum Fourier Transform (QFT), Galois Field (GF), and Inst, or on the benchmark that contains large oracle circuits such as ISCAS’85 [40]. The QFT circuits are generated using the method outlined in [1], and Galois Field and Inst circuits are respectively sourced from [50] and [51]. ISCAS’85, on the other hand, is a collection of classical EDA circuits [40]. To prepare the quantum version of the ISCAS’85 benchmark, we initially transform the circuits into XOR-Majority Graph (XMG) form utilizing the ABC tool [52]. This transformation enables a direct mapping from the traditional AND, OR, and NOT gates to the X, CX, and Toffoli gates in a quantum circuit. Subsequently, we decompose the Toffoli gates into a combination of single- and double-qubit gates as Fig. 8a.

Lastly, to explore the futurism of quantum computing beyond the NISQ era, we conduct experiments on the emulated large-scale quantum circuits as mentioned in Section 5.1.3.

5.2 Experiments on Initial Placement
As mentioned in Section 3.1, to testify to the impact of initial placement on the qubit mapping problem, we compare with the QMAP method, which incorporates an adaptive initial placement heuristic for better mapping results [26], on various sizes of circuits. The experimental results agree with our speculations – As the circuit depth increases along with its gate count, the Mapping Cost introduced by the scheduling and routing procedures starts to dominate the overall cost. Therefore, the impact of the initial placement becomes insignificant.

8https://github.com/cda-tum/mqt-qmap/tree/main/examples
9Our focus for performance evaluation is on circuits with Ideal Circuit Costs (c.f. Definition 2.4) surpassing 500. For those with Ideal Circuit Cost smaller than 500, since it is often that their optimum mapping results can be achieved by exact methods, we will skip them for performance comparison and yet include them in the initial placement experiments (Section 5.2).
Table 1. Performance on the SABRE-large benchmark, with QMAP as the baseline. The cost improvement is calculated as $\Delta(\%) = \frac{\text{Cost}_{\text{QMAP}} - \text{Cost}_{\text{other tool}}}{\text{Cost}_{\text{QMAP}}}$. Duostra LE is the only approach outperforming the baseline QMAP on average.

| Circuit   | #Gate | Ideal | QMAP [27] | Qiskit [45] | TOQM [38] | t(ket) [44] | SABRE [28] | Duostra LE |
|-----------|-------|-------|-----------|-------------|-----------|------------|------------|------------|
| cm82a     | 650   | 571   | 1485      | 1803 -21.4  | 1554 -4.7 | 1488 -0.2  | 1806 -21.6 | 1495 -0.7  |
| rd53_251  | 1291  | 1203  | 3154      | 3712 -17.7  | 3348 -6.2 | 3536 -5.1  | 3814 -20.9 | 3192 -1.2  |
| cm42a     | 1776  | 1574  | 4515      | 5128 -13.6  | 4472 1.0  | 4850 -7.4  | 5426 -20.2 | 4245 6.0   |
| pm1_249   | 1776  | 1574  | 4515      | 5140 -13.8  | 4472 1.0  | 4850 -7.4  | 5426 -20.2 | 4245 6.0   |
| sqtr8_260 | 3009  | 2779  | 8078      | 9211 -14.0  | 7863 2.7  | 8902 -10.2 | 9420 -16.6 | 7561 6.4   |
| z4_268    | 3073  | 2756  | 7993      | 9165 -17.6  | 7887 -1.2 | 8651 -11.0 | 9576 -22.9 | 7441 4.5   |
| adrt4_197 | 3439  | 3088  | 8643      | 10372 -20.0 | 8859 -2.5 | 9721 -12.5 | 10627 -23.0 | 8225 4.3   |
| rd73_252  | 5321  | 4829  | 13350     | 15817 -18.5 | 13869 -3.9 | 17884 -34.0 | 16865 -26.3 | 12895 3.4   |
| cycle10   | 6050  | 5662  | 15897     | 18682 -17.5 | 15880 0.1  | 18997 -19.5 | 19193 -20.7 | 15321 3.6   |
| sqrt_7    | 7630  | 6367  | 18950     | 21086 -11.4 | 18049 4.7  | 22035 -16.5 | 23136 -12.6 | 17621 6.9   |
| ham15     | 8763  | 8092  | 22387     | 26201 -17.0 | 23048 -3.0 | 26644 -19.0 | 27367 -22.3 | 21652 3.3   |
| dc2_222   | 9462  | 8759  | 25256     | 28756 -13.9 | 24603 2.6  | 28357 -12.2 | 29886 -18.3 | 23775 5.9   |
| sqp_258   | 10223 | 9176  | 26850     | 30296 -12.8 | 26502 -1.2 | 29694 -9.6  | 32079 -10.6 | 24496 8.8   |
| ine_237   | 10619 | 9790  | 28281     | 31963 -13.0 | 27256 3.6  | 30512 -7.9  | 33075 -17.0 | 26500 6.3   |
| cm85a     | 11414 | 10630 | 30715     | 35076 -14.0 | 30157 1.8  | 35617 -16.0 | 36385 -18.5 | 29076 5.3   |
| rd84_253  | 13658 | 12176 | 35847     | 40567 -13.1 | 34876 2.8  | 40122 -11.8 | 42543 -18.6 | 33019 8.0   |
| root_255  | 17139 | 14799 | 43604     | 49606 -13.8 | 42833 2.8  | 47990 -10.1 | 52463 -20.3 | 40671 6.7   |
| mlt4_245  | 18852 | 17258 | 49755     | 57379 -15.3 | 49990 1.5  | 55144 -10.8 | 59263 -19.1 | 47199 5.1   |
| urf2_277  | 20112 | 19698 | 55709     | 62833 -19.0 | 59989 -7.7 | 65785 -1.9  | 69352 -24.5 | 55126 1.0   |
| life_287  | 2445  | 20867 | 60676     | 68673 -12.6 | 58932 3.3  | 65319 -7.1  | 71679 -17.6 | 56546 7.3   |
| 9symnl    | 34881 | 32048 | 94360     | 106104 -12.5| 90976 3.6  | 100672 -6.7 | 111521 -18.2 | 86165 8.2   |
| dist_223  | 38046 | 32968 | 79097     | 110229 -13.5| 95964 1.6  | 107263 -10.5| 116529 -20.0| 90288 7.0   |
| uff1_278  | 54766 | 53256 | 152057    | 183630 -20.8| 160414 -5.5 | 185152 -21.8| 194702 -28.1| 147585 2.9   |
| hwb8_113  | 69380 | 64758 | 175618    | 210658 -20.0| 183657 -4.6 | 204096 -4.8 | 220665 -25.7| 172757 1.7   |
| urf1_149  | 184864| 172518| 413994    | 534114 -22.4| 460686 -12.8| 497711 -20.7| 572947 -38.4| 437037 -5.6   |

Average Cost Improvement: -16.2 -0.70 -11.8 -21.2 4.5

For smaller circuits whose Ideal Circuit Costs (c.f. Definition 2.4) are smaller than 500, QMAP’s effort in exploring better initial placement pays back as it exhibits superior performance over the Duostra LE Search and TOQM. However, as the Ideal Circuit Cost grows, Duostra turns around and outperforms QMAP (Fig. 9).

It is noteworthy that achieving optimal qubit mapping results on small circuits (Ideal Circuit Cost < 500) is not our focus in this paper because the exact solution naturally overshadows heuristic approaches for circuits of this size. Thus, the value of heuristic-based methods shines through when the exact solution is not feasible. As indicated in Fig. 9, our approach prevails as the circuit size increases, which is our main contribution.

5.3 Performance Evaluation on Mid-Size Circuits

To evaluate the performance of various heuristics algorithms of different tools, we conduct experiments on the mid-size circuits adopted from the SABRE-large test suite [28] and its extended set in [27]. Note that we filter out the small circuits whose Ideal Circuit Costs are smaller than 500 because their optimum mapping solutions can be attained within one day by the exact approaches such as OLSQ [34, 35]. The selected circuits are of sizes up to 185,000 gates and less than 16 qubits. Consequently, all the compared tools can finish the qubit mapping task for every circuit within one minute, allowing the full exploitation of the heuristic algorithms of the tools.

The experimental results are presented in Table 1. Columns 2 and 3 list the number of gates and the Ideal Circuit Costs of the benchmark circuits, respectively. We choose QMAP [27] as the baseline method (note: marked with “*”) because it performs fairly well on these testcases. Columns 5 to 12 in the table report the Mapping Costs and the comparison with QMAP of IBM Qiskit, TOQM, t(ket),...
Fig. 10. Performance on the extended benchmark provided by QMAP [27]. Only the circuits with the Initial Circuit Cost greater than 500 are included in the experiment. We select QMAP’s result selected as the baseline. The indices are sorted by the relative improvements of the Duostra LE search. Duostra LE search outperforms the others in most cases.

and SABRE. The table indicate that on average, IBM Qiskit, \( t\ket{ket} \), and SABRE exhibit inferior performance compared to QMAP by 16.2%, 11.8% and 21.2% while TOQM demonstrates relatively competitive results with only 0.7% difference on average.

The qubit mapping results of our algorithm are listed in the last two columns. For the mid-size circuits, we employ the LE Search approach with the depth set to 4. It shows that we can outperform QMAP for the average of 4% as we win 22 of the 25 testcases.

We further conduct the experiments on the extended set of the benchmark circuits [27]. As shown in Fig. 10, our algorithm can top the other tools on 70.0% (42/60) of the cases and improve over QMAP for the average of 4% in Mapping Costs.

5.4 Scalability Experiment on Large Circuits

To assess the scalability of our algorithm, we conducted experiments on circuits with scalable and repeatable architectures, including Quantum Fourier Transform (QFT), Galois Field (GF) [50], and Inst [51]. We implemented the QFT circuits for 65, 127, 433, 1121, and 2129 qubits, and decomposed them into circuits with basic single- and double-qubit gates [1]. In addition, we included large oracle circuits such as ISCAS’85 [40] and a benchmark suited for the NISQ era [53].

The results are outlined in Table 2. The columns "Cir. #Q" and "Top. #Q" stand for the numbers of qubits for the benchmark circuits and the target topologies of the hardware devices (i.e. IBMQ machines). We compared our mapping results with QMAP [27], Qiskit [45], \( t\ket{ket} \) [44], and SABRE [28]. For the method TOQM [38] included in the mid-size circuit experiments, it failed to execute.
Table 2. Performance on various large benchmarks. The highlighted results represent the best one among QMAP, Qiskit, t(fket), and SABRE. The cost improvement is calculated based on the best results among the counterparts ($\Delta(\%) = \frac{Cost_{best} - Cost_{our}}{Cost_{our}}$). TLE stands for exceeding the time limit one day. Duostra SP estimation outperforms the others in most cases.

| Circuit   | Top.  | QMAP [27] | Qiskit [45] | t(fket) [44] | SABRE [28] | Duostra SP |
|-----------|-------|-----------|-------------|--------------|-------------|------------|
|           | #Q    | Cost     | Time        | Cost         | Time        | Cost       | Time       | Δ(%)    |
| QFT       | 4212  | 5,369     | 113.7       | 1,556        | 2.50        | 9,898      | 0.49       | 23.97   |
|           | 6246  | 25,243    | 3.864       | 16,156       | 7.91        | 28,644     | 7.239      | 67.22   |
|           | 48    | 1,867     | 0.238       | 5,029         | 1.896       | 4,267      | 0.063      | 0.533   |
|           | 46    | 1,194     | 0.183       | 776           | 0.323       | 1,223      | 2.471      | 3.083   |
|           | 64    | 877       | 0.106       | 441           | 0.104       | 849        | 2.948      | 4.032   |
|           | 49    | 634       | 0.069       | 442           | 0.096       | 456        | 9.176      | 418     |
|           |       |           |             |              |             |            |            |         |
| ICAS’85   | 1773  | 2129      | 73,368      | 349           | 13,787      | 1.720      | 13,121     | 1.885   |
|           | 1380  | 2129      | 92,227      | 440           | 167,765     | 62847      | 11,769     | 0.103   |
|           | 991   | 1121      | 50,894      | 143           | 245,659     | 4011       | 41,505     | 0.794   |
|           | 840   | 1121      | 15,947      | 189           | 197,737     | 2553       | 31,431     | 0.863   |
|           | 660   | 1121      | 20,045      | 70.83         | 131,372     | 885.6      | 15,164     | 0.385   |
|           | 255   | 433       | 10,313      | 4.580         | 12,874      | 7.829      | 20,506     | 29.01   |
|           | 202   | 433       | 6,807       | 9.198         | 7,919       | 6.041      | 14,673     | 23.20   |
|           | 188   | 433       | 6,587       | 4.715         | 8,821       | 5.972      | 11,755     | 12.41   |
|           | 172   | 433       | 7,322       | 5.527         | 9,269       | 6.58       | 17,287     | 18.97   |
|           | 433   | 433       | 14,559      | 6.788         | 16,228      | 42.95      | 39,906     | 150.3   |
|           | 118   | 433       | 5,048       | 1.757         | 4,717       | 2.899      | 5,542      | 3.599   |
|           | 64    | 65        | 1,747       | 0.066         | 2,492       | 0.831      | 2,682      | 1.725   |
|           | 31    | 65        | 1,346       | 0.065         | 1,935       | 0.745      | 1,166      | 0.791   |
|           | 341   | 433       | 9,664       | 0.729         | 11,258      | 7.823      | 22,894     | 15.04   |
|           | 129   | 433       | 3,516       | 1.058         | 3,750       | 2.965      | 8,317      | 2.754   |
|           | 67    | 127       | 1,622       | 0.069         | 1,851       | 0.452      | 1,622      | 1.569   |
|           | 39    | 65        | 1,051       | 0.042         | 1,694       | 0.305      | 883        | 0.408   |
|           | 400   | 433       | 11,362      | 2.274         | 18,879      | 6.80       | 22,442     | 469.7   |
|           | 350   | 433       | 11,362      | 2.274         | 18,879      | 6.80       | 22,442     | 469.7   |
|           | 75    | 127       | 36,413      | 2.419         | 42,943      | 10.35      | 43,254     | 11.50   |
|           | 45    | 65        | 10,845      | 0.365         | 13,787      | 7.120      | 13,121     | 1.885   |

Average Cost Improvement: 21.75%
better on qugan and some smaller ISCAS’85 benchmarks, and SABRE frequently produced the better results, particularly standing out for the QFT cases.

In short, the experimental results demonstrate the scalability and superiority of our qubit mapping framework for larger scale circuits. For the QFT cases that we lost to SABRE, it is likely due to the specifically repetitive patterns of the circuits. Our future work aims to enhance the Duostra Scheduler to identify and prioritize such patterns. We also plan to incorporate an automatic scheduler that can identify the suitable search depth, thereby striking a balance between solution quality and program runtime.

5.5 Exploring the Futurism on Extra-Large Circuits

To explore the futurism of quantum computing beyond the NISQ era, we conduct the qubit mapping experiments on QFT circuits up to 11,969 qubits. The target topologies are the emulated devices as described in Section 5.1.3. We choose the “Shortest path” approach (i.e. Shortest-Path router + SP Estimation scheduler) as the baseline comparison with “Duostra” to demonstrate the effect of when considering the occupied time during the routing path selection. The selection of QFT circuits is attributed to its scalability potential and reputation as one of the most resource-demanding test sets, primarily due to the requirement for every qubit within the QFT to interact with all other qubits.

As depicted in Fig. 12, the Mapping Cost associated with the Duostra router is consistently less than half of the cost generated by the Shortest Path router. Conversely, the runtime of the Shortest Path router is around two-thirds of that of Duostra. To facilitate a clearer and yet fair comparison, we multiply the cost and runtime values and plot them on Fig. 12c. The trend line of Duostra consistently appears lower, indicating that Duostra outperforms its counterpart considering both solution quality and efficiency as the circuit size increases. This leads us to conclude that, when compared to a simple approach like the Shortest Path router, which merely inserts SWAP gates to solve the problem, the Duostra Router’s incorporation of additional information, such as the occupied time, contributes to its ability to generate superior results.

6 CONCLUSION

In this paper, we introduce a pioneering framework designed to address the qubit mapping challenge in large-scale quantum algorithms. Our framework encompasses an innovative Duostra router that can efficiently generate optimal routing paths for SWAP insertions on double-qubit gates, and a flexible scheduler that offers two heuristic scheduling algorithms, the Limitedly-Exhaustive (LE)
Search and the Shortest-Path (SP) Estimation, for smaller- and larger-size circuits, respectively. The experimental results on various sets of benchmarks demonstrate the superiority of our framework on the qubit mapping problems. For instance, for the mid-size circuits (i.e. SABRE benchmark), we improve the Mapping Costs by 4.5%, 5.2%, 16.3%, 20.7% and 25.7%, when compared to QMAP, TOQM, t(ket), Qiskit and SABRE, respectively. For the large benchmarks whose numbers of qubits exceed 50, our framework can achieve on the average 21.75% improvements over the virtual best results among QMAP, t(ket), Qiskit and SABRE. We also conduct experiments on extra-large QFT circuits up to 11,969 qubits. The results showcase our scalability to tackle the qubit mapping challenges for the quantum advantage.

Looking into the future, we plan to enhance our framework for broader applicability and more novel techniques. For example, fidelity issue is an inevitable factor for the practical quantum computation. Several studies have attempted to address the qubit and gate errors for the mapping problems [54–61], and some others have focused on scheduling gates to reduce the crosstalk errors [62–65]. In the near future, we will incorporate some of the error models and error correction circuits into our framework in order to answer the fault-tolerant qubit mapping problems.

On the other hand, several recent researches have explored innovated ideas to address the qubit mapping problems, including investigations into the potential of quantum teleportation [66], reinforcement learning techniques [67], and gate commutation and circuit transformation [68–71]. However, scalability still remains a challenge for these methods due to their computational requirements. We plan to explore ways to integrate insights from these studies into our framework.
as the future work, aiming to achieve even greater efficiency and accuracy in qubit mapping for a broader range of quantum computing applications.

ACKNOWLEDGEMENT
This work was partially supported by National Science and Technology Council of Taiwan under Grant NSTC 113-2119-M-002-024.

H.-C. Cheng is supported by the Young Scholar Fellowship (Einstein Program) of the National Science and Technology Council, Taiwan (R.O.C.) under Grants No. NSTC 112-2636-E-002-009, No. NSTC 113-2119-M-007-006, No. NSTC 113-2119-M-001-006, No. NSTC 113-2124-M-002-003, No. NSTC 113-2628-E-002-029, by the Yushan Young Scholar Program of the Ministry of Education, Taiwan (R.O.C.) under Grants No. NTU-112V1904-4 and No. NTU-113V1904-5 and by the research project "Pioneering Research in Forefront Quantum Computing, Learning and Engineering” of National Taiwan University under Grant No. NTU-CC-112L893405 and NTU-CC-113L891605.

H.-C. Cheng acknowledges the support from the “Center for Advanced Computing and Imaging in Biomedicine (NTU-113L900702)” through The Featured Areas Research Center Program within the framework of the Higher Education Sprout Project by the Ministry of Education (MOE) in Taiwan.

REFERENCES
[1] Michael A. Nielsen and Isaac L. Chuang. *Quantum Computation and Quantum Information: 10th Anniversary Edition*. Cambridge University Press, 2010.
[2] Sumeet Khatri and Mark M Wilde. Principles of quantum communication theory: A modern approach. *arXiv preprint arXiv:2011.04672*, 2020.
[3] Chi-Yuan Chen, Guo-Jyun Zeng, Fang-jhu Lin, Yao-Hsin Chou, and Han-Chieh Chao. Quantum cryptography and its applications over the internet. *IEEE Network*, 29(5):64–69, September 2015.
[4] Srinivasan Arunachalam and Ronald De Wolf. Guest column: A survey of quantum learning theory. *SIGACT News*, 48(2):41–67, June 2017.
[5] Peter W. Shor. Algorithms for quantum computation: discrete logarithms and factoring. In *Proc. Annual Symposium on Foundations of Computer Science*, pages 124–134, 1994.
[6] Peter W. Shor. Polynomial-time algorithms for prime factorization and discrete logarithms on a quantum computer. *SIAM Journal on Computing*, 26(5):1484–1509, 1997.
[7] John Proos and Christof Zalka. Shor’s discrete logarithm quantum algorithm for elliptic curves. *Quantum Information & Computation*, 3(4):317–344, July 2003.
[8] IBM. IBM quantum, 2021.
[9] Marcos Yukio Siraichi, Vinicius Fernandes dos Santos, Caroline Collange, and Fernando Magno Quintão Pereira. Qubit allocation. In *Proc. International Symposium on Code Generation and Optimization*, pages 113–125, 2018.
[10] Dmitri Maslov, Sean M Falconer, and Michele Mosca. Quantum circuit placement. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 27(4):752–763, 2008.
[11] Mehdi Saeedi, Robert Wille, and Rolf Drechsler. Synthesis of quantum circuits for linear nearest neighbor architectures. *Quantum Information Processing*, 10(3):355–377, 2011.
[12] Amlan Chakrabarti, Susmita Sur-Kolay, and Ayan Chaudhury. Linear nearest neighbor synthesis of reversible circuits by graph partitioning. *arXiv preprint arXiv:1112.0564*, 2011.
[13] Alireza Shafaei, Mehdi Saeedi, and Massoud Pedram. Optimization of quantum circuits for interaction distance in linear nearest neighbor architectures. In *Proc. ACM/IEEE Design Automation Conference (DAC)*, pages 1–6, 2013.
[14] Alireza Shafaei, Mehdi Saeedi, and Massoud Pedram. Qubit placement to minimize communication overhead in 2D quantum architectures. In *Proc. IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)*, pages 495–500, 2014.
[15] Robert Wille, Aaron Lye, and Rolf Drechsler. Optimal SWAP gate insertion for nearest neighbor quantum circuits. In *Proc. IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)*, pages 489–494, 2014.
[16] Robert Wille, Aaron Lye, and Rolf Drechsler. Exact reordering of circuit lines for nearest neighbor quantum architectures. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 33(12):1818–1831, December 2014.
[17] Aaron Lye, Robert Wille, and Rolf Drechsler. Determining the minimal number of swap gates for multi-dimensional nearest neighbor quantum circuits. In *Proc. IEEE Asia and South Pacific Design Automation Conference*, pages 178–183, 2015.
Abtin Molavi, Amanda Xu, Martin Diges, Lauren Pick, Swamit Tannu, and Aws Albarghouthi. Qubit mapping and Tom Peham, Lukas Burgholzer, and Robert Wille. On optimal subarchitectures for quantum circuit mapping.

Alwin Zulehner, Alexandru Paler, and Robert Wille. An efficient methodology for mapping quantum circuits to the IBM QX architectures. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 38(7):1226–1236, 2018.

Alwin Zulehner and Robert Wille. Compiling SU(4) quantum circuits to IBM QX architectures. In *Proceedings of the 24th Asia and South Pacific Design Automation Conference*, pages 185–190, January 2019.

Atsushi Matsuo, Wakakii Hattori, and Shigeru Yamashita. Reducing the overhead of mapping quantum circuits to IBM Q system. In 2019 IEEE International Symposium on Circuits and Systems (ISCAS), pages 1–5, May 2019.

Tom Peham, Lukas Burgholzer, and Robert Wille. On optimal subarchitectures for quantum circuit mapping. *ACM Transactions on Quantum Computing*, 4(4):1–20, 2023.

Robert Wille and Lukas Burgholzer. MQT QMAP: efficient quantum circuit mapping. In *Proceedings of the 2023 International Symposium on Physical Design*, pages 198–204, 2023.

Gushu Li, Yufei Ding, and Yuan Xie. Tackling the qubit mapping problem for NISQ-era quantum devices. In *Proc. International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, pages 1001–1014, 2019.

Pengcheng Zhu, Zhijin Guan, and Xueyun Cheng. A dynamic look-ahead heuristic for the qubit mapping problem of NISQ computers. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 39(12):4721–4735, December 2020.

Hui Jiang, Yuxin Deng, and Ming Xu. Quantum circuit transformation based on Tabu search. *arXiv preprint arXiv:2011.04672*, August 2021.

Gian Giacomo Guerreschi and Jongsoo Park. Two-step approach to scheduling quantum circuits. *Quantum Science and Technology*, 3(4):045003, 2018.

Robert Wille, Lukas Burgholzer, and Alwin Zulehner. Mapping quantum circuits to IBM QX architectures using the minimal number of SWAP and H operations. In *Proceedings of the 56th Annual Design Automation Conference 2019*, pages 1–6, 2019.

Bochen Tan and Jason Cong. Optimal layout synthesis for quantum computing. In *Proceedings of the 39th International Conference on Computer-Aided Design (ICCAD)*, pages 1–9, 2020.

Bochen Tan and Jason Cong. Optimal qubit mapping with simultaneous gate absorption. In 2021 *IEEE/ACM International Conference On Computer-Aided Design (ICCAD)*, pages 1–8, November 2021.

Wen-Hsuan Lin, Jason Kimko, Bochen Tan, Nikolaj Bjerner, and Jason Cong. Scalable optimal layout synthesis for NISQ quantum processors. In 2023 60th ACM/IEEE Design Automation Conference (DAC), pages 1–6, 2023.

Abtin Molavi, Amanda Xu, Martin Diges, Lauren Pick, Swamit Tannu, and Aws Albarghouthi. Qubit mapping and routing via MaxSAT. In 2022 55th IEEE/ACM International Symposium on Microarchitecture (MICRO), pages 1078–1091, October 2022.

Haowei Deng, Yu Zhang, and Quanxi Li. Codar: A contextual duration-aware qubit mapping for various NISQ devices. In *Proc. ACM/IEEE Design Automation Conference (DAC)*, pages 1–6, 2020.

Chi Zhang, Ari B Hayes, Longfei Qiu, Yuwei Jin, Yanhao Chen, and Eddy Z Zhang. Time-optimal qubit mapping. In *Proc. ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, pages 360–374, 2021.

Lingling Lao, Hans Van Someren, Imran Ashraf, and Carmen G. Almudever. Timing and resource-aware mapping of quantum circuits to superconducting processors. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 41(2):359–371, February 2022.

Franc Brglez. A neutral netlist of 10 combinational benchmark circuits and a target translator in Fortran. In *Proc. International Symposium on Circuits and Systems*, 1985, 1985.
Pranav Mundada, Gengyan Zhang, Thomas Hazard, and Andrew Houck. Suppression of qubit crosstalk in a tunable superconducting circuit. *Physical Review Applied*, 12(5):054023, November 2019.
[63] Prakash Murali, David C. Mckay, Margaret Martonosi, and Ali Javadi-Abhari. Software mitigation of crosstalk on noisy intermediate-scale quantum computers. In Proceedings of the Twenty-Fifth International Conference on Architectural Support for Programming Languages and Operating Systems, pages 1001–1016, March 2020.

[64] Yongshan Ding, Pranav Gokhale, Sophia Fuhui Lin, Richard Rines, Thomas Propson, and Frederic T. Chong. Systematic crosstalk mitigation for superconducting qubits via frequency-aware compilation. In 2020 53rd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), pages 201–214, October 2020.

[65] Yasuhiro Ohkura, Takahiko Satoh, and Rodney Van Meter. Simultaneous execution of quantum circuits on current and near-future NISQ systems. IEEE Transactions on Quantum Engineering, 3:1–10, 2022.

[66] Stefan Hillmich, Alwin Zulehner, and Robert Wille. Exploiting quantum teleportation in quantum circuit mapping. In Proceedings of the 26th Asia and South Pacific Design Automation Conference, pages 792–797, January 2021.

[67] Matteo G. Pozzi, Steven J. Herbert, Akash Sengupta, and Robert D. Mullins. Using reinforcement learning to perform qubit routing in quantum compilers. ACM Transactions on Quantum Computing, 3(2):1–25, June 2022.

[68] Andrew M. Childs, Eddie Schoute, and Cem M. Unsal. Circuit transformations for quantum architectures. In Conference on the Theory of Quantum Computation, Communication and Cryptography (TQC), 2019.

[69] Toshinari Itoko, Rudy Raymond, Takashi Imamichi, and Atsushi Matsuo. Quantum circuit compilers using gate commutation rules. In Proceedings of the 24th Asia and South Pacific Design Automation Conference, pages 191–196, January 2019.

[70] Toshinari Itoko, Rudy Raymond, Takashi Imamichi, and Atsushi Matsuo. Optimization of quantum circuit mapping using gate transformation and commutation. Integration, 70:43–50, January 2020.

[71] Ji Liu, Feiyi Li, and Huiyang Zhou. Not all SWAPs have the same cost: a case for optimization-aware qubit routing. In 2022 IEEE International Symposium on High-Performance Computer Architecture (HPCA), pages 709–725, April 2022.