Estimation of residual carrier density near the Dirac point in graphene through quantum capacitance measurement

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ABSTRACT

We discuss the residual carrier density ($n^*$) near the Dirac point (DP) in graphene estimated by quantum capacitance ($C_Q$) and conductivity ($\sigma$) measurements. The $C_Q$ at the DP has a finite value and is independent of the temperature. A similar behavior is also observed for the conductivity at the DP, because their origin is residual carriers induced externally by charged impurities. The $n^*$ extracted from $C_Q$, however, is often smaller than that from $\sigma$, suggesting that the mobility in the puddle region is lower than that in the linear region. The $C_Q$ measurement should be employed for estimating $n^*$ quantitatively.

The extraction of the quantum capacitance ($C_Q$) through capacitance measurements of graphene provides direct information on the density of states (DOS) of graphene because it is regarded as the energy cost of inducing carriers in graphene and is directly related as $C_V = e^2DOS$. In the field-effect transistor (FET) structure, $C_Q$ is introduced in series with the geometrical capacitance ($C_{G}$) in the equivalent circuit ($1/C = 1/C_{G} + 1/C_Q$). The experimentally determined $C_Q$ value near the Dirac point (DP) is, however, larger than that expected from the ideal DOS of graphene. This indicates that mobile carriers should exist near the DP in graphene FETs. The origin of these residual mobile carriers at the DP is still under the debate. The temperature-independent resistivity at the DP of graphene FETs fabricated on SiO2 substrates suggests that the carriers are induced externally from charged impurities on/in the SiO2 substrates. In fact, the temperature-dependent resistivity due to the intrinsic thermal excitation of carriers is observed for suspended graphene and graphene on h-BN substrates as the charged impurity densities are reduced. These charged impurities not only induce mobile carriers around the DP but also degrade the carrier mobility ($\mu$) in the on-state of graphene FETs, thus, the quantitative estimation of the residual (mobile) carrier density ($n^*$) is quite important. The region around the DP may be understood intuitively by the electron-hole puddle state, which was demonstrated by scanning the single-electron transistor probe. Furthermore, the relationship between $n_{imp}$ and $n^*$ has been predicted theoretically. However, the quantitative comparison between them is limited. In addition, although the dominant scattering mechanism affecting $\mu$ in back-gated graphene FETs is considered to be the Coulomb scattering by charged impurities, the scattering mechanism in top-gated graphene FETs is not yet clear.

In this study, dual-gated (top- and back-gated) graphene FETs were fabricated to estimate $n^*$ through $C_Q$ measurements. Then, the dominant scattering source in graphene FETs with the high-k top-gate insulator is also discussed from the temperature dependence of the FET mobility.

Monolayer graphene was transferred by the mechanical exfoliation of Kish graphite onto ~90 nm SiO2/n+-Si substrates (0.01 Å/cm). The SiO2/Si substrates were annealed at 1000 °C for 5 min in an 100% O2 gas flow to remove the residual resist. Then, the D band was not detected in the Raman measurement through the Y2O3 layer, which suggests that no noticeable defects were formed during the deposition. The top-gate electrode (Ni/Au) was also patterned by electron-beam lithography. Finally, the device was annealed at 300 °C for 30 s in a 0.1% O2 gas flow before electrical measurements were conducted in a vacuum probe station. An optical micrograph of a dual-gated graphene FET with an Y2O3 top-gate insulator is shown in (a). The leakage current as a function of $V_{BG}$ when $I_{SO}$ is $5\times10^{-10}$ µA for $V_{BG} = 0$ V at 297 K. (c) $I_{SO}$ as a function of $V_{BG}$ for different $V_{AC}$ at 297 K. (d) $C_{Q}$ as a function of $V_{BG}$ for different $V_{AC}$ at a frequency of 1 MHz at 297 K. (e) The equivalent circuit of the dual-gated device.
optical microscopy image of the typical dual-gated FET is shown in Fig. 1(a). To avoid macroscopically inhomogeneous channel potentials due to the charge transfer from the source and drain contacts, 16 the distance between the top gate and the source (drain) electrodes was designed to be longer than ~2 μm.

Here, we should mention about the reason why Y2O3 was chosen for the top-gate insulator. The oxidation ability of Y is the highest among high-k materials and also higher than that of C based on the standard Gibbs free energy changes for oxidation. Therefore, it is expected that Y2O3 could be obtained at the relatively low oxidation temperature and is thermodynamically stable on graphene. The electrical characteristics of the thin Y2O3 films are critical in this study. The leakage current between the top-gate and source (drain) electrodes was kept low (<2 pA and three orders lower than Isd, as shown in Fig. 1(b). This low leakage current was achieved by optimizing Pd, during the metallic Y deposition. Figure 1(c) shows Isd as a function of top-gate voltage (VTG) for different VBG. The top gate controls the graphene channel just below the top-gate electrode, while the back gate (the n-Si substrate) changes the carrier density (n) over the entire area of the graphene channel. Therefore, when the Fermi level (EF) was initially placed deeply in the valence band by VTG = -20 V and then VG = -1 V, Isd was larger than the currents observed for other VG values because the resistance of the access region between the top-gate and source (drain) electrodes was kept low (μ-type). On the other hand, the total capacitance (CTot) between the source and top-gate electrodes for the same device was measured as a function of VTG for different VBG, as shown in Fig. 1(d). The equivalent circuit of the dual-gated FET is shown in Fig. 1(c), where VB, Cpara, and Cpara, are the channel voltage, the parasitic capacitances for the top gate and back gate, respectively. The large dependence of CTot on VTG (that is, VTG) directly indicates a large contribution of C to Ctotah, because C is independent of EF.

Contrary to the I-V characteristics, the C-V characteristic is shifted in parallel with changes in VBG because the capacitance in graphene was modulated just below the top-gate electrode. The slight variation in the minimum Ctotah could be due to the depletion layer formation in the Si substrate (~5×10¹² cm⁻²). To confirm this, all C-V curves in Fig. 1(d) were superimposed, except for the VBG = ±30 V cases, as shown in Fig. 2(a). It is clear that all of the curves are consistent, suggesting that the parasitic capacitance has no VTG dependence and that the linear dispersion is retained under the external electric field, unlike in the bilayer case. 15

The hysteresis in C-V curves is also a measure of the qualities of both the oxide layer and the graphene/oxide interface. The hysteresis is defined as ΔVhyst = Vbφ – Vdφ for the VTG sweep, where Vbφ is the Dirac point voltage. The inset in Fig. 2(a) shows ΔVhyst as a function of temperature for a VTG range of ±2 V. The room temperature data is only shown for VTG = ±1 V. The ΔVhyst is negligible for VTG = ±1 V and -0.1 V for VTG = ±2 V at room temperature. The fact that ΔVhyst was suppressed by lowering the measurement temperature may suggest the orientation polarization of water molecules. 14,18,19 Therefore, the present Y2O3 serves quite well as the top-gate insulator.

Systematic shifts in the DP as a function of VBG are evident in the I-V and C-V measurements, as shown in Figs. 1(c) and (d). The DP voltages obtained for the VTG sweeps in both measurements are plotted as a function of VBG in Fig. 2(b). The DP is controlled by the relative ratio of capacitative couplings between top and back gates with graphene. Therefore, the slope in Fig. 2(b) corresponds to Cgd/Cgd. Both lines have the same slope, indicating that both top and back gates capacitively control the dual-gated FET very consistently in I-V and C-V measurements. Because Cgd is estimated to be 0.039 μF/cm² for 88-nm-thick SiO2, Cgd can be calculated to be 0.76 μF/cm². This method is very useful because Cgd can be determined without the information on the dielectric constant and thickness of Y2O3 on graphene. The precise and independent determination of these two quantities for the very limited area of graphene includes large amount of ambiguity.

Next, let us estimate CG. Figure 3(a) shows the measured capacitance between the source and top gate electrodes, CG, as a function of VTG at VBG = 0 V. The equivalent circuit in Fig. 1(e) can be reduced to that in the inset of Fig. 3(a) due to VBG = 0 V. Because Cgd is 0.76 μF/cm² as mentioned above, CG is an only fitting parameter to extract CG. Therefore, the CG value at VTG = ±2 V was adjusted by the fitting of CG. The dotted lines in Fig. 3(a) are the fitted curves, assuming CG = 0.19 μF/cm².

![FIG 2](color online) (a) Ctot as a function of VTG at VBG, where the C-V curves for VBG = ±20 V in Fig. 1(d) are superimposed relative to the DP of C-V curve at VBG = 0 V for both the transverse and vertical axes. The inset is the temperature dependence of ΔVhyst for the sweeping range of VTG = ±2 V. The room temperature data is only shown for ΔVhyst = ±1 V. Both data is obtained for VBG = 0 V. (b) The DP voltage for the VTG sweep as a function of VBG. The solid circles and solid boxes indicate the DPs obtained by I-V and C-V measurements in Figs. 1(c) and (d), respectively. The linear functions obtained by the fitting are shown in the figure.

![FIG 3](color online) (a) Ctot as a function of VTG at VBG. The solid circles are experimental data; the dotted lines are curves fitted by CG = 0.19 μF/cm². The inset shows the equivalent circuit for VBG = ±30 V, where CG is in parallel with C and CG. (b) CG extracted based on the fitting in (a). The theoretically predicted CG is shown by red dotted lines. The right vertical axis indicates the DOS. The inset shows the minimum CG as a function of temperature for a different sample.
The dominant source for $C_{para}$ could be the capacitance between the topgate and source electrodes. The experimental results are reproduced well, except near the DP. Based on this fitting, $C_Q$ is experimentally estimated as a function of $E_p$, as shown in Fig. 3(b). $E_p$ is indeed the charging energy and is expressed as $E_p=-eV_{ch}$. When the serial capacitance is described as $1/C' = 1/C_{203} + 1/C_Q$ and $V_{TG}'$ is defined as $V_{TG}' = V_{TG} - V_p$, $V_{ch}$ can be expressed as $V_{ch} = V_{TG}' - \int V_{TG}' C'/G_{203}dV_{TG}'$. Thus, the experimentally estimated $C_Q$ can be compared to the theoretical $C_Q (=2\varepsilon_0\varepsilon_{Si}/\pi \alpha^2)$, where $\varepsilon_{Si}$ is the Fermi velocity ($1 \times 10^6$ cm/s) and $h$ is the Planck’s constant. The experimentally estimated $C_Q$ is in good agreement with the theoretical $C_Q$ for $|E_p| > -0.15$ eV.

On the other hand, a large deviation from theory is evident near the DP, suggesting that more carriers exist than theoretically predicted. To elucidate whether these carriers are induced by the charged impurities or by the thermal excitation, the temperature dependence of the minimum $C_Q$ was measured. As shown in the inset of Fig. 3(b), almost no temperature dependence of the minimum $C_Q$ is observed. Thus, the residual carrier density $n$ near the DP is induced by charged impurities\(^3,4\) and is calculated to be $3.6 \times 10^{13}$ cm\(^{-2}\), using $E_p = h\nu_F \sqrt{\pi e/n}$, as indicated by the arrow in Fig. 3(b). It should be noted that the minimum $C_Q$ value in the inset is different from that in the main figure, since these data were obtained from a different sample.

The residual carrier density $n$ near the DP is usually discussed from the $\sigma - n$ relationship because $n$ is referred as the carrier density in the so-called puddle transport.\(^7\) No comparison between $n_{LF}$ and $n_{CF}$, however, has been performed in the same graphene FET. In fact, it should be considered that the conductance is determined by not only the residual carriers but also the carrier mobility. Therefore, the four-probe dual-gated graphene FET was fabricated to remove the contribution of the contact resistance, as shown in Fig. 4(a). $n_{CF}$ was determined to be $1.25 \times 10^{12}$ cm\(^{-2}\) from the intersect (solid circle) of the two dotted lines in Fig. 4(b), while $n_{CF}$ for the same FET was determined to be $3.8 \times 10^{11}$ cm\(^{-2}\) from the $C_Q - E_p$ relation, which was obtained in the same manner for Fig. 3(b). The value of $n_{CF}$ is also indicated in Fig. 4(b) as an open circle. The $n_{CF}$ is larger than $n_{CF}$. It should be noted that $n_{CF}$ for seven different samples measured in this work lie in the range of $1.9 - 5.4 \times 10^{11}$ cm\(^{-2}\) and are always smaller than $n_{LF}$. In the analysis of the $I$-$V$ measurements, the simple two-band model\(^2\), in which the same and constant mobility values for electron and hole are assumed for all carrier densities, was employed for explaining the conductivity ($\sigma$ - $n$ relation. On the other hand, $n_{CF}$ is directly determined from the $C'V$ measurement, where the contribution of the scattering problem is excluded. Thus, the fact that $n_{CF}$ is larger than $n_{CF}$ suggests that the electron and hole mobilities in the puddle-edge region are lower than those in the linear $\sigma$ - $n$ region, as shown schematically in the inset of Fig. 4(b). Here, $n_{CF, TG}$ in Fig. 4(b) indicates the residual carrier density for back-gated FET device determined by the $I$-$V$ measurement, which is smaller than $n_{CF}$. It is evident that the deposition process of Y$_2$O$_3$ top-gate insulator on graphene affects $n_{CF}$. Therefore, the $C_Q$ measurement is necessary for estimating $n$ quantitatively and independently of the sample quality.

Finally, let us discuss the carrier scattering in the case of high-$k$ gate stack graphene FETs. There is a debate regarding whether high-$k$ dielectric materials on graphene improve the mobility due to a screening of the scattering potential from charged impurities on/in SiO$_2$ substrates.\(^2\)\(^4\) Moreover, the remote phonon scattering due to the polar high-$k$ oxide with a low phonon energy may become the dominant scattering source rather than the Coulomb scattering by charged impurities.\(^2\)\(^5\) In the remote phonon scattering, the mobility should be considerably suppressed and is strongly dependent on the temperature. To obtain more information on the scattering mechanism, the four-probe dual-gated FET, as shown in Fig. 4(a), was investigated. The $\sigma$ - $n$ relation in Y$_2$O$_3$ top-gated devices is linear at the high $n$ region as shown in Fig. 4(b). It should be noted that this $\sigma$ - $n$ curve was obtained by changing $V_{BG}$ because the top gate cannot electrostatically control the channel region between the top gate and the voltage probe. Figure 4(c) shows the resistivity at the DP and the electron mobility at $n = 3 \times 10^{12}$ cm\(^{-2}\) in the linear $\sigma$ - $n$ region, as functions of the measurement temperature. Although the very weak temperature dependence of the resistivity at the DP is observed in the high temperature region ($T > 200$ K) possibly due to the remote phonon scattering from Y$_2$O$_3$ topgate or SiO$_2$ substrate,\(^2\)\(^6\) it did not show the temperature dependence at low temperature. The very weak temperature dependence of the mobility also agrees with that reported previously for the graphene FET with the HfO$_2$ top gate,\(^6\) since the main origin seems to be the Coulomb scattering due to the charged impurity on/in Y$_2$O$_3$ and SiO$_2$. These results indicate that the remote phonon scattering is not dominant but that the Coulomb scattering by charged impurities is still the main limiting factor. This is consistent with that for the minimum $C_Q$ (Fig. 3(b) inset). Moreover, the carrier
mobility in the dual-gated graphene FETs is generally lower than those of typical back-gated graphene FETs without the top gate,\textsuperscript{10} as is seen from the comparison of slopes in the $\sigma$ - $n$ relations in Fig. 4(b). This suggests that the improvement of the top gate stack formation on graphene may improve the mobility of dual-gated graphene FETs.

In summary, we performed C-V and I-V measurements on the same dual-gated graphene FET. Both the minimum $C_Q$ and the resistivity at the DP have shown nearly zero temperature dependence, indicating that carriers are induced by charged impurities. Moreover, it has been found experimentally that $n_{C,V}$ is often smaller than $n_{I,V}$. This fact has been discussed from the viewpoint that the carrier mobility in the edge of the puddle region is lower than that in linear conductivity region. Thus, it is concluded that the $C_Q$ measurement should be employed for estimating $n'$ quantitatively. In addition, a relatively weak temperature dependence of the mobility and the linear $\sigma$ - $n$ relation suggest that the dominant scattering source in the high-$k$ top-gated FETs used in this study is the Coulomb scattering by charged impurities.

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