A ZVT Auxiliary Circuit for High Step-Up Multi-Input Converters with Diode-Capacitor Multiplier

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Received: November 2020 Revised: January 2021 Accepted: March 2021

ABSTRACT:
In this paper, a Zero-Voltage Transition (ZVT) non-isolated high step-up multi-input DC-DC converters is proposed which employs an auxiliary cell and diode-capacitor multiplier. The auxiliary cell has only one switch and is suitable for high step converters with diode-capacitor multiplier. In the proposed converter, all semiconductor devices operate under fully soft switching condition. The main switches turn on and turn off under Zero Voltage Switching (ZVS) condition whereas the auxiliary switch turns on under Zero Current Switching (ZCS) condition and turns off under zero Voltage and Zero Current Switching (ZVZCS) condition. Also, ZCS condition at turn-off is provided for all diodes to eliminate reverse recovery issue. The structure of the proposed converter includes two boost cells, one diode-capacitor multiplier cell, and one ZVT auxiliary circuit. Soft switching conditions for all main switches are provided by only one auxiliary circuit. The proposed converter has high step-up conversion gain without any coupled inductor. Soft switching conditions, continuous current of input sources, high efficiency, expansion capability of input sources, returning the energy of the auxiliary circuit to the diode-capacitor multiplier and low-voltage stress on switches are the main advantages of the proposed converter. The steady-state analysis of the converter and operation modes are discussed. A 160-W prototype of the proposed converter is designed and implemented. Experimental results confirm that the theoretical and the efficiency of the proposed converter reaches 96.4% at the nominal load.

KEYWORDS: Soft Switching, Zero Voltage Transition, High Step-Up Conversion, Multi-Input Converter.

1. INTRODUCTION
Nowadays, due to energy shortage and environmental contamination, renewable energy such as photovoltaic (PV) cells, wind turbines, and fuel cells are employed increasingly[1]. Among renewable sources, photovoltaic systems are expected to play a main role in future energy production[2].

Renewable energy systems generate low voltage output and environmental conditions affect their output voltage [3]. Accordingly, step-up converters with high efficiency is required to increase the low voltage of PV panels to a suitable DC bus voltage of inverters or other applications [4]. High step-up conversion can be obtained by cascaded method [5], coupled inductor[6], switched capacitor [7], diode-capacitor multiplier [8] or their combination [9]. By applying these methods, the problem of extreme duty cycles in traditional boost converters is solved. Many high step-up methods have been comprehensively reviewed and classified in [10]. Each technique has advantages and disadvantages. For instance, using a coupled inductor makes high step-up conversion ratio[6] but switch voltage stress is increased due to the existence of the leakage inductance. Also, pulsating input current of this technique makes it not suitable for PV power generation system[11]. Based on the categorization offered in [10], voltage multiplier circuits such as diode-capacitor multiplier are suitable for low power renewable energy applications because of high-voltage conversion ratio, low normalized voltage stress, low cost and transformer less.

Simultaneous receiving energy from different input sources ensures the continuity of energy supply. When using multi-input converter instead of multiple converters, many advantages such as low component count, reduced volume and cost, higher flexibility, the possibility of easier control, and better management of energy sources are obtained[12]. Multi-input converters are generally classified into two categories, including isolated and non-isolated multi-input converters [13]. In recent years, numerous isolated and non-isolated multi-
input converters with different structures for various applications have been presented [12, 14-21]. Although, isolated converters have obtained high voltage conversion ratio by using a transformer, volume, weight, losses, and ripple of input current are increased due to usage of the transformer[21]. Therefore, in systems or applications that isolation is not needed such as PV systems, non-isolated converters are more appropriate. In [20], non-isolated multi-input high step-up DC-DC converter based on diode-capacitor voltage multiplier is suggested. Although, low voltage stress on semiconductor devices and continuous input currents have been obtained for this converter, due to hard switching, the efficiency of this topology is low. An extendable high step-up multi-input converter is proposed in [14]. Although, low voltage stress on semiconductor devices and simple control have been obtained for this converter, due to hard switching, the efficiency of this topologies is low. In [15], a three-level multi-input converter with input sources grouping is proposed which independent operation of grouped input sources is not feasible. An extendable multi-input multi-output boost converter is proposed in [19]. Although, the input inductor of this converter is shared for all inputs, to reduce the count of the component and volume, the input sources cannot power up the load simultaneously. Also due to discontinuous input currents of this converter, it is not suitable for renewable energy sources. In [22], a multi-input DC-DC converter is presented based on traditional boost converter. However, four switches are employed which would increase the cost and size. In [23], a bidirectional multi input multi output buck-boost converter is presented. Six switches and two inductors are used for only two input sources of this converter and soft switching conditions are not provided for switches. A multi-input converter based on SEPIC topology is suggested in [24] which one of the inputs has the bidirectional operation for connecting to a battery and the other inputs are unidirectional. However, two isolated gate drivers are needed.

Soft switching techniques can be applied to improve efficiency and reduce Electromagnetic Interference (EMI) of the converters[8, 13, 16-18], [25]. In [16], a dual-input converter with zero voltage transition for main switches is proposed. Despite soft switching conditions is provided for main switches, the auxiliary switch operates under hard switching conditions. In this converter, input sources cannot power up the load independently because the series combination of sources is applied. Also, the cost of implementation is reduced due to the low number of switches used. A multi-port converter with zero voltage transition based on coupled inductor is presented in [17]. In this converter, only three switches are applied for three port so that all the input sources are controlled independently by using a separate switch. In [18], a high step-up three port converter similar to [17] based on coupled inductor is suggested. In this converter, two coupled inductors, five switches and two active clamp circuits have been used to increase voltage gain and provide soft switching conditions. Although, five power switches are used for only three port of this converter, the converter power density is low. In [26], a fully soft switched interleaved boost converter with zero voltage transition for main switches is proposed. Although, soft switching conditions is provided for all switches and diodes, the voltage stresses of semiconductor devices are high.

In this paper, a fully soft switched high step-up multi-input DC-DC converter based on the diode-capacitor multiplier technique is proposed. One soft switching auxiliary cell is applied for all input cells which decreases the number of components. The main switches are turned on and turned off at ZVS and the auxiliary switch is turned on at ZCS and turned off at ZVZCS. High step-up gain, high efficiency, continuous input currents, low voltage stress of switches and expandable input ports are benefits of the proposed converter.

This paper is organized as follows: Dual-input structure of the proposed converter is introduced in Section 2. In Section 3, design procedure along with an example are explained. In Section 4, simulation and experimental results are provided. In Section 5, performance comparison is expressed and conclusions are presented in Section 6.

2. DUAL-INPUT STRUCTURE OF THE PROPOSED CONVERTER

2.1. Circuit Configuration

Fig. 1 shows the dual-input configuration of the proposed converter. The proposed converter consists of two input boost cells, one stage diode-capacitor multiplier, and one soft switching auxiliary circuit, generally. Also, the number of diode-capacitor multiplier stages and input sources can be expanded as needed. \( V_{in1}, L_1, S_1, \) and \( D_1 \) are the first boost cell components, \( V_{in2}, L_2, S_2, \) and \( D_2 \) are the second boost cell components and \( D_3, D_4, C_1, \) and \( C_2 \) formed a diode-capacitor multiplier stage. Also, the auxiliary circuit consists of \( C_a, L_{a1}, L_{a2}, D_5, D_6, S_a, \) and \( C_o \) shown in the dashed block to provide ZVS conditions for the main switches.

![Fig. 1. Dual-input configuration of the proposed converter.](image-url)
In addition, as the number of inputs expands, the auxiliary circuit provides soft switching conditions for all switches of input boost cells. The energy received by the soft switching cell is returned to the capacitors of the diode-capacitor multiplier and finally is returned to the output. The control of the main switches S₁ and S₂ is like 180° phase interleaved structure. By controlling the duty cycle of the main switches, the power absorbed from the input sources can be controlled and the maximum absorbable power in PV systems can be achieved.

2.2. Operating Principle

Fig. 2 shows the main theoretical waveforms of the proposed converter during the one switching period Tₛ. There are eighteen total modes for a single switching period. However, due to the symmetrical operation of the proposed converter, only the nine leading modes in a half switching period are analyzed and the other nine modes are similar. To simplify the steady-state analysis, some conditions and assumptions are made in the following:

1.- All the components are ideal (without the effects of parasitic parameters).
2.- The proposed converter is operated in Continuous-Conduction Mode (CCM) to have a smooth current with minimum current ripple.
3.- The voltages across the capacitances of C₁, C₂ and Cₒ are considered as a constant over one switching period because the capacitances are assumed to be large enough.
4.- The main switches are 180° phase-shift interleaved switching and the duty cycle of them is larger than 50%.

The equivalent circuits for each mode are demonstrated in Fig. 3. The detailed circuit analysis over one switching period is presented as follows. It is assumed that before t₀, S₁ and S₂ are ON and L₁ and L₂ are being charged by the input sources. Also, all diodes are OFF and the capacitor Cₒ is supplying the load.

Mode 1 \( t₀ \text{ to } t₁ \): At \( t₀ \), the switch \( S₁ \) is turned off and the capacitor \( C₅ \) begins to charge through the diode \( D₅ \). The equivalent circuit is shown in Fig. 3. The voltage value of the capacitor \( C₅ \) is determined as follows:

\[
V_{C₅}(t) = \frac{I_{in₁}}{C₅} \cdot (t - t₀) \tag{1}
\]

At \( t₁ \), the voltage of \( C₅ \) reaches \( V_{C₅}(t₁) \) and diodes \( D₅ \) and \( D₁₀ \) are turned on. \( V_{C₅}(t₁) \) can be calculated according to the following equation, where \( V_{C₅}(t₀) \) is the voltage value of \( C₅ \) at the beginning of this mode.

\[
V_{C₅}(t₁) = V_{C₂} + V_{Cₐ}(t₀) \tag{2}
\]

Mode 2 \( t₁ \text{ to } t₂ \): When the voltage of \( C₇ \) reaches \( V_{C₇}(t₁) \), this mode starts and diodes \( D₇ \), \( D₇ \) and \( D₁₀ \) are turned on and capacitors \( C₁ \) and \( C₂ \) are charged linearly with input current \( I_{in₁} \). At \( t₂ \), the capacitor voltage \( C₇ \) reaches zero and the capacitor voltage \( Cₐ \) equals \( V_{C₉} \) and this mode ends. The important equations in this mode are as follows:

\[
V_{C₇}(t) = \frac{I_{in₁}}{C₅+Cₐ} \cdot (t - t₁) + V_{C₉}(t₁) \tag{3}
\]

\[
V_{Cₐ}(t) = \frac{I_{in₁}}{C₅+Cₐ} \cdot (t - t₁) + V_{Cₐ}(t₀) \tag{4}
\]

Fig. 2. Key waveforms of the proposed converter.

The required time for the charge of \( C₇ \), and providing the turning off under zero voltage conditions of the main switches is equal to the sum of the times of the first and second mode, which are obtained from (1) to (4) as follows:

\[
\Delta t₁₂ = t₂ - t₀ = \frac{C₆}{I_{in₁}} (V_{C₇} + V_{C₉}(t₀)) - \frac{C₅+Cₐ}{I_{in₁}} (V_{Cₐ}(t₀)) \tag{5}
\]

Mode 3 \( t₂ \text{ to } t₃ \): When the voltage of \( C₇ \) reaches \( V_{C₉} \), this mode starts and diodes \( D₇ \) and \( D₉ \) are turned on and capacitors \( C₉ \) and \( C₂ \) are charged with input current \( I_{in₁} \). By turning on \( D₇ \), the capacitor \( C₂ \) is charged to the output voltage of the first boost cell, which can be determined as follows:
Also due to the symmetry in the circuit, $V_{C1}$ can be similarly obtained as follows:

$$V_{C1} = \frac{V_{in1}}{1-D_{eff1}}$$  \hspace{1cm} (7)

Also, due to the conduction of $D_1$, the capacitor $C_1$ is connected in series with the output voltage of the first boost cell ($V_{C2}$) and the output voltage is equal to the sum of $V_{C1}$ and $V_{C2}$.

**Mode 4 [t3-14]**: This mode starts when the switch $S_1$ is turned on to discharge $C_5$ and turn on the switch $S_1$ at ZVS. When the switch $S_1$ is turned on, a resonance starts between $C_a$ and $L_{a1}$ through the path of $D_1$, $D_5$, $L_{a1}$, $C_a$, $S_1$, and until $I_{DS} = I_{D2} = I_{L3}$, conduction of diodes $D_1$ and $D_5$ is continued and capacitors $C_1$ and $C_2$ is charged. Given that the current increase is resonant form, the switch, diodes $D_1$, $D_3$, and $D_5$ turn on at ZCS and the diodes $D_1$ and $D_3$ turn off at ZCS. This mode ends with establishing the relationship $I_{DS} = I_{D5} = I_{L1}$ and turning off diodes $D_1$ and $D_3$. The resonant equations of this mode are as follows:

$$I_{L1}(t) = V_{C2} \sqrt{\frac{C_a}{L_{a1}}} \sin(\omega_1(t - t_3))$$  \hspace{1cm} (8)

$$V_{CA}(t) = V_{C2} (1 - \cos(\omega_1(t - t_3)))$$  \hspace{1cm} (9)

where $\omega_1 = \frac{1}{\sqrt{L_{a1}C_a}}$

Since the value of $L_{a2}$ is chosen to be much larger than $L_{a1}$, the presence of $L_{a2}$ in the resonant equations of modes 4 to 7 can be ignored.

**Mode 5 [t14-15]**: When $I_{DS} = I_{D7} = I_{L3}$, the diodes $D_1$ and $D_3$ turn off and this mode begins. In this mode, a new resonance is started between $C_a$, $L_{a1}$, and $C_a$ which causes the discharge of $C_a$. At $t_5$, the voltage $V_{C3}$ reaches zero and the body diodes $S_1$ and $S_2$ turn on. The resonance equations in this mode are as follows:

$$I_{L1}(t) = A \sin(\omega_2(t - t_4)) + B \cos(\omega_2(t - t_4)) + I_{L1} \frac{C_{eq}}{C_a}$$  \hspace{1cm} (10)

where $A = \left( V_{CA} - V_{CA}(t_4) \right) \frac{C_{eq}}{L_{a1}}$,

$$B = I_{L1} \left( 1 - \frac{C_{eq}}{C_a} \right)$$

$$\frac{dV_{CA}(t)}{dt} = \frac{1}{C_a} I_{L1}(t)$$  \hspace{1cm} (11)

Also, $V_{CA}(t_5)$ and $I_{L1}(t_5)$ are the value of the capacitor voltage $C_a$ and the value of the inductor current $L_{a1}$ at the beginning of this mode, respectively.

**Mode 6 [t15-16]**: At $t_5$, the body diodes of $S_1$ and $S_2$ turn on and a new resonance starts between $C_a$ and $L_{a1}$. At $t_6$, the body diodes of $S_1$ and $S_2$ turn off under ZCS condition, and this mode ends. When the body diode of $S_1$ is on, the voltage across the switch $S_1$ is zero which is an appropriate time to turn on the switch $S_1$ under ZVS condition. The equations of this mode are as follows:

$$I_{L1}(t) = \left( V_{CA}(t) \right) \frac{C_a}{L_{a1}} \sin(\omega_1(t - t_5))$$

$$+ I_{L1}(t_5) \cos(\omega_1(t - t_5))$$  \hspace{1cm} (13)

$$V_{CA}(t) = \frac{1}{C_a} \int_{t_5}^{t} I_{L1}(t) + V_{CA}(t_5)$$

$$= \left( \frac{\omega_1}{C_a} I_{L1}(t_5) \right) \sin(\omega_1(t - t_5)) + V_{CA}(t_5) \cos(\omega_1(t - t_5))$$  \hspace{1cm} (14)

Where, $\omega_1 = \frac{1}{\sqrt{L_{a1}C_a}}$

Also, $V_{CA}(t_5)$ and $I_{L1}(t_5)$ are the value of the capacitor voltage $C_a$ and the value of the inductor current $L_{a1}$ at the beginning of this mode, respectively.

**Mode 7 [t16-17]**: In this mode, the resonance of the previous mode continues and $I_{sa}$ reaches zero at $t_7$. By reaching $I_{sa}$ to zero, $S_a$ can be turned off under ZCS condition. To provide ZVS turn-on condition of $S_1$ and ZCS turn-off condition of $S_a$, the auxiliary switch should not be turned off earlier than the total of the fourth to seventh mode times.

**Mode 8 [t17-18]**: In this mode, a new resonance starts between $C_a$ and $L_{a2}$ and the energy stored in $C_a$ transfers to $L_{a2}$. After half period of this resonance, $I_{L2}$ reaches zero and $D_8$ turns off at ZCS and the resonance is finished at $t_8$. Also, both the main switches are turned on and $I_{L1}$ and $I_{L2}$ are increased linearly by the input sources. The defining equations of this mode are as follows:

$$I_{L2}(t) = V_{CA}(t) \frac{C_a}{L_{a2}} \sin(\omega_3(t - t_7))$$  \hspace{1cm} (15)
\[ V_{ca}(t) = V_{ca}(t_2) \cos(\omega_3(t - t_2)) \] (16)

Where, \[ \omega_3 = \frac{1}{\sqrt{L_0C_0}} \]

Also, \( V_{ca}(t_2) \) is the value of capacitor voltage \( C_a \) at the beginning of this mode. The duration of this mode is achieved \( \pi \sqrt{L_0C_0} \) from the relations (15) and (16). The resonance in this mode is ended before turning off the other main switch.

**Mode 9 [t8- t9]:** During this mode, both the main switches \( S_1 \) and \( S_2 \) are ON and \( L_1 \) and \( L_2 \) are energized by the two input sources, independently. Also, all diodes are off and \( C_O \) supplies the load.

### 3. DESIGN PROCEDURE

According to previously described circuit characteristics, the design guide of the proposed converter containing voltage gain, input current relationships, main element design, auxiliary circuit design, and selections of power switches and diodes are explained. Also, the converter parameters are calculated through an example. The specifications of the example are presented in Table 1:

| Parameters                  | Symbol | Values  |
|-----------------------------|--------|---------|
| First input dc voltage      | \( V_{in1} \) | 48V     |
| Second input dc voltage     | \( V_{in2} \) | 36V     |
| Output dc voltage           | \( V_{out} \) | 320 V   |
| Maximum output power        | \( P_{out} \) | 160 W   |
| Switching frequency         | \( f_{sw} \) | 50 kHz  |

### 3.1. Voltage Gain

The voltage gain of the proposed converter can be determined by a volt-second balance of the inductors \( L_1 \) and \( L_2 \) as follows:

\[ V_{in1}D_{eff1} \cdot T_S = (V_o - V_{C1} - V_{in1})(1 - D_{eff1}) \cdot T_S \] (17)

\[ V_{in2}D_{eff2} \cdot T_S = (V_o - V_{C2} - V_{in2})(1 - D_{eff2}) \cdot T_S \] (18)
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where:
\[ D_{\text{eff}1} = D_1 + \frac{1}{75} \Delta t_{4-6} \]

\[ \frac{1}{2} + \frac{1}{75} [\Delta t_7] \leq D_{\text{eff}1} \leq 1 - \frac{1}{75} [\Delta t_{1-2}] \quad (19) \]

\[ D_{\text{eff}2} = D_2 + \frac{1}{75} \Delta t_{13-15} \]

\[ \frac{1}{2} + \frac{1}{75} [\Delta t_{16}] \leq D_{\text{eff}2} \leq 1 - \frac{1}{75} [\Delta t_{10-11}] \quad (20) \]

\[ V_{\text{out}} = \frac{V_{\text{in}1}}{1-D_{\text{eff}1}} + \frac{V_{\text{in}2}}{1-D_{\text{eff}2}} \quad (21) \]

According to (21) and the mentioned characteristics of the design example with the same power distribution of inputs, \( D_{\text{eff}1} = D_{\text{eff}2} \approx 0.74 \) is obtained.

3.2. Relationships of the Input Currents

By applying the ampere-second balance for \( C_1 \) and \( C_2 \), the relationships of the input currents can be obtained where \( I_{L1}, I_{L2} \) and \( I_o \) are the average currents of the input inductors \( L_1, L_2 \) and the output current, respectively.

\[ (I_{L1} - I_o)(1 - D_{\text{eff}1})T_S = I_o \cdot D_{\text{eff}1} \cdot T_S \quad (22) \]

\[ (I_{L2} - I_o)(1 - D_{\text{eff}2})T_S = I_o \cdot D_{\text{eff}2} \cdot T_S \quad (23) \]

According to (22) and (23) can be expressed as:

\[ I_{\text{in}1} = I_{L1} \approx \frac{I_o}{1-D_{\text{eff}1}} \quad (24) \]

\[ I_{\text{in}2} = I_{L2} \approx \frac{I_o}{1-D_{\text{eff}2}} \quad (25) \]

According to (24) and (25) it can be concluded that by adjusting the duty cycle of the main switches, the input currents of the proposed converter can be controlled to track the maximum power point for two PV panels independently in PV system. The current auto-balance capability is obtained in the proposed converter by \( D_{\text{eff}1} = D_{\text{eff}2} \). Assuming \( D_{\text{eff}1} = D_{\text{eff}2} \approx 0.74 \) in the design example, \( I_{\text{in}1} \) and \( I_{\text{in}2} \) are calculated 1.9 A.

3.3. Considerations on Main Elements

Since the main structure of the proposed converter is formed from the combination of two conventional boost converters and their output summation, the design of the boost cell elements is similar to the regular boost converter. Also, input current ripple and output voltage ripple can be calculated like a regular boost converter [27]. The input currents for designing the boost cell elements are determined by (24) and (25). The multiplier capacitors \( C_1 \) and \( C_2 \) that are like the output capacitors of the boost cells can be obtained as follows:

\[ C_1 = C_2 \geq \frac{I_{\text{in}1,\text{max}} \cdot tf}{V_{\text{in}1}} \quad (26) \]

Where, \( \Delta V_{\text{C}1,2} \) is the capacitor voltage ripple and \( f_s \) is switching frequency. According to (26), \( C_1 = C_2 = 2.2 \mu F \) are chosen for the design example.

3.4. Considerations on Auxiliary Circuit

The snubber capacitor of both the main switches is \( C_s \) and can be calculated like other snubber capacitor based on the maximum current of both switches as follows:

\[ C_s \geq \max \left\{ \left( \frac{I_{\text{in}1,\text{max}} \cdot tf}{V_{\text{in}1}} \right), \left( \frac{I_{\text{in}2,\text{max}} \cdot tf}{V_{\text{in}2}} \right) \right\} \quad (27) \]

Where, \( tf \) is fall time of switches. A 3.3nF capacitor is chosen as snubber capacitor for the design example. The capacitance value of \( C_s \) must be chosen larger than the capacitance value of \( C_s \), so that the voltage \( V_{\text{C}1} \) changes much faster than \( V_{\text{C}2} \) in the fifth mode. Therefore, \( C_{\text{eq}} \) and \( \omega_2 \) in mode 5, can be rewritten as:

\[ C_{\text{eq}} \equiv C_s \quad (28) \]

\[ \omega_2 = \frac{1}{\sqrt{L_a C_s}} \quad (29) \]

Also, considering that the resonance period in the fifth mode should be selected much smaller than the switching period, it can be written as:

\[ \frac{2\pi}{\omega_2} \leq \frac{1}{5f_w} \quad (30) \]

Substituting (29) into (30), the following equation is concluded for the value of the inductor \( L_a \):

\[ L_a \leq \frac{1}{(10f_w)^2 C_s} \quad (31) \]

On the other hand, the maximum amount of resonant current in the fourth mode which is determined by (8) must be greater than \( I_{L1} \) so that the capacitor \( C_s \) in the fifth mode can be completely discharged. So:

\[ V_{\text{C}2} \cdot \sqrt{\frac{C_s}{L_a}} \geq 2 \cdot (I_{\text{in}1}) \quad (32) \]

By substituting (6) and (24) to (32) one can conclude:

\[ \sqrt{\frac{L_a}{C_a}} \leq \frac{V_{\text{in}1,\text{min}}}{2I_o} \quad (33) \]
According to (31) and (33), the appropriate value for the inductor $L_{a1}$ and the capacitor $C_a$ are selected $5\mu H$ and $15nF$, respectively. Since the auxiliary circuit and its components are used to provide soft switching conditions for both main switches, the maximum current of $L_{a1}$ is determined based on the maximum current at both switching times $t_5$ and $t_{11}$; Therefore, from (10) and (28), the maximum current $I_{a1}$ is obtained as follows:

$$I_{La1,max} \equiv \max \left\{ \left( \frac{V_{C2}}{L_{a1}} + I_{L1} \right), \left( \frac{V_{C1}}{L_{a1}} + I_{L2} \right) \right\} \tag{34}$$

Also considering that the resonance between $L_{a2}$ and $C_a$ in the eighth mode must be completed before turning on the main switch, consequently, $\frac{\pi}{\omega_3} \leq \left( D_{1,2,min} - \frac{1}{2} \right) \cdot T$ which by substituting $\omega_3 = \frac{1}{\sqrt{L_{a2}C_a}}$ the following equation can be obtained:

$$\sqrt{L_{a2}C_a} \leq \frac{(D_{1,2,min} - \frac{1}{2})}{\pi f_{sw}} \tag{35}$$

According to (35), the maximum value of the resonance inductor $L_{a2}$ can be determined which should be selected larger than $L_a$ so that the polarity of $V_{Ca}$ in the sixth and seventh modes remain positive and $I_{a1}$ can become zero and the auxiliary switch is turned off at ZCS. In this case, an appropriate value for the inductor $L_{a2}$ can be $20\mu H$.

The maximum current of $L_{a2}$ is determined based on the maximum amount of current in both the seventh and sixteenth modes; Therefore, $I_{La2,max}$ is obtained as follows:

$$I_{La2,max} \equiv \max \left\{ \left( V_{Ca}(t_7) \frac{C_a}{L_{a2}} \right), \left( V_{Ca}(t_{16}) \frac{C_a}{L_{a2}} \right) \right\} \tag{36}$$

The duty cycle of the main switches should be larger than 50% for a high step-up converter, certainly. Also, to establish ZCS condition for the auxiliary switch, the pulse gate of the auxiliary switch should not be removed before its current reaches zero. The minimum time required for the auxiliary switch to be ON ($\Delta t_a$) is equal to the sum of the duration of the fourth to seventh modes, which according to the selected values for $L_{a1} = 5\mu H$, $L_{a2} = 20\mu H$ and $C_a = 15nF$, $\Delta t_a$ is obtained $0.6\mu s$.

### 3.5. Selections of Power Switches and Diodes

The voltage and current stresses of switches and diodes are listed in Table 2. As can be seen, the main switches voltage stress is lower than the output voltage of the proposed converter. The current stress of the main switches is determined in the second and eleventh modes and is equal to the sum of the input currents. The current stress of the auxiliary switch and diode $D_9$ is determined at $t_3$ or $t_{14}$ and is equal to the maximum of $I_{La1}$ and can be calculated by (34). The current stress of diode $D_8$ is equal to the maximum of $I_{La2}$, which occurs in the eighth mode and is calculated by (36). The current stress of diodes $D_9$ and $D_{10}$ is equal $I_{La2}$ and $I_{a1}$, respectively, which occurs in the second and eleventh modes. According to the voltage and current stress of semiconductor components listed in Table 2, characteristics of the design example and the selected values of the auxiliary circuit IRFP460 and MUR460 are selected for power switches and diodes, respectively.

### 4. SIMULATION AND EXPERIMENT OF THE PROPOSED CONVERTER

The proposed converter is modeled in the simulation software (ORCAD) and a prototype is implemented based on the example design of section 4 to validate the theoretical analysis and the performance of the proposed converter at the 50 kHz switching frequency for main switches. Since the auxiliary circuit is employed to provide the soft switching conditions for both main switches, the switching frequency of the auxiliary circuit is twice the switching frequency of the main switches. The specifications of the prototype listed in Table 1 and the values of the circuit components are listed in Table 3. Also, the photograph of the implemented prototype is shown in Fig. 5.

![Prototype photograph of the proposed converter.](image-url)
According to Fig. 6, the main switch $S_1$ is turned off under ZVS condition by the snubber capacitor and ZVS turn-on is attained by turning on the body diode of the main switch $S_1$. Similarly, according to Fig. 7, ZVS turn-off and ZVS turn-on are achieved for the main switch $S_2$. The voltage and current waveforms of the auxiliary switch $S_a$ are shown in Fig. 8. According to Fig. 8, ZCS turn-on and ZVZCS turn-off of the auxiliary switch $S_a$ are attained by the resonant inductor $L_a$. According to the experimental results, $dv/dt$ is reduced by providing soft switching conditions and there is no unwanted high frequency oscillation which improves EMC (Electromagnetic compatibility) performance of the proposed converter.

Also, the parasitic ringing in the auxiliary switch voltage waveform shown in Fig. 8 is due to the resonance of the converter inductors and the parasitic capacitors of the power devices. The voltage and current waveforms of the main switch $S_1$ are shown in Fig. 6 and the voltage and current waveforms of the main switch $S_2$ are shown in Fig. 7.

### Table 2. Current and Voltages stresses of the Semiconductor Devices.

| Voltages stresses | Value | Current stresses | Value |
|-------------------|-------|------------------|-------|
| $V_{S1}$          | $V_{in1}$ divided by $1 - D_{eff1}$ | $I_{S1}$ | $I_o$ divided by $1 - D_{eff1}$ plus $I_o$ divided by $1 - D_{eff2}$ |
| $V_{S2}$          | $V_{in2}$ divided by $1 - D_{eff2}$ | $I_{S2}$ | $I_o$ divided by $1 - D_{eff1}$ plus $I_o$ divided by $1 - D_{eff2}$ |
| $V_{Sa}$          | $\max\left\{\frac{V_{in1} + V_{in2}}{1 - D_{eff1}, 1 - D_{eff2}}\right\}$ | $I_{Sa}$ | $\max\left\{\frac{V_{c2}}{C \sqrt{L_{a1} + I_{L1}}} + \frac{V_{c1}}{C \sqrt{L_{a2} + I_{L2}}}\right\}$ |
| $V_{D1}$          | $V_0$ | $I_{D1}$ | $I_o$ divided by $1 - D_{eff1}$ |
| $V_{D2}$          | $V_0$ | $I_{D2}$ | $I_o$ divided by $1 - D_{eff2}$ |
| $V_{D3}$          | $V_0$ divided by $1 - D_{eff2}$ | $I_{D3}$ | $I_o$ divided by $1 - D_{eff1}$ |
| $V_{D4}$          | $V_0$ divided by $1 - D_{eff1}$ | $I_{D4}$ | $I_o$ divided by $1 - D_{eff2}$ |
| $V_{D5}$          | $V_{in2}$ divided by $1 - D_{eff2}$ | $I_{D5}$ | $\frac{V_{c2}}{C \sqrt{L_{a1} + I_{L1}}}$ |
| $V_{D6}$          | $V_{in1}$ divided by $1 - D_{eff1}$ | $I_{D6}$ | $\frac{V_{c1}}{C \sqrt{L_{a2} + I_{L2}}}$ |
| $V_{D7}$          | $\max\left\{\frac{V_{in1} + V_{in2}}{1 - D_{eff1}, 1 - D_{eff2}}\right\}$ | $I_{D7}$ | $\max\left\{\frac{V_{c2}}{C \sqrt{L_{a1} + I_{L1}}} + \frac{V_{c1}}{C \sqrt{L_{a2} + I_{L2}}}\right\}$ |
| $V_{D8}$          | $\max\left\{\frac{V_{in1} + V_{in2}}{1 - D_{eff1}, 1 - D_{eff2}}\right\}$ | $I_{D8}$ | $\max\left\{\frac{V_{ca(t_c)}}{C \sqrt{L_{a1}} + \frac{V_{ca(t_{L2})}}{C \sqrt{L_{a2}}}\right\}$ |
| $V_{D9}$          | $V_0$ | $I_{D9}$ | $I_o$ divided by $1 - D_{eff2}$ |
| $V_{D10}$         | $V_0$ | $I_{D10}$ | $I_o$ divided by $1 - D_{eff1}$ |

### Table 3. Circuit parameters.

| Parameters             | Symbol | Values     |
|------------------------|--------|------------|
| Input inductors        | $L_i, L_2$ | 0.6 mH     |
| Capacitors of Diode-Capacitor Multiplier | $C_i, C_2$ | 2.2 μF     |
| Output capacitor       | $C_o$ | 22 μF      |
| Auxiliary inductor 1   | $L_{a1}$ | 5 μH       |
| Auxiliary inductor 2   | $L_{a2}$ | 20 μH      |
| Snubber capacitor      | $C_s$ | 3.3 nF     |
| Auxiliary capacitor    | $C_a$ | 15 nF      |
| Main power switches    | $S_1, S_2$ | IRFP460   |
| Auxiliary power switch | $S_a$ | IRFP460    |
| Power diodes           | $D_1-D_{10}$ | MUR460    |
Table 4 presents the power losses of the proposed converter components in two different modes of hard switching and soft switching based on the relationship between the losses of each component [28]. In this table, the main parameters of each component such as $R_{DS}$ of switches have been extracted from the data sheets. The efficiency curves of the proposed converter and its hard switching counterpart are depicted in Fig. 9 with $V_{in1}=48$ V and $V_{in2}=36$ V. The maximum efficiency of the proposed converter is realized at the nominal load about 96.4% which shows that soft switching conditions effectively improve the efficiency of the proposed converter.

The losses of the main and auxiliary elements (w)

| Type of losses | Soft switching (Auxiliary circuit) | Hard switching (RCD Snubber) |
|----------------|-----------------------------------|-------------------------------|
| $\frac{1}{2} \times C_{oss-Sa} \times (V_{sa})^2 \times f$ | 1.52 | ----- |
| $\frac{1}{2} \times C_{oss-S1,2} \times (V_{s1,2})^2 \times f$ | ----- | 6.54 |
| Switching losses of main switches $V_{s,off} \times f$ | ----- | 1.99 |
| $\frac{2}{2} \times (t_{on} + t_{off}) \times I_{on}$ | ----- | ----- |
| Conduction losses of $D_1$ $[V_f \times (I_{avg})]$ | 0.84 | ----- |
| Conduction losses of main switches $R_{DS(on)-S1} \times (I_{rms-S1})^2$ | 2.49 | 2.49 |
| Conduction loss of auxiliary switch $R_{DS(on)-S2} \times (I_{rms-S2})^2$ | 0.27 | ----- |
| Conduction losses of $D_2$ $[V_f \times (I_{avg})]$ | 0.8 | 0.8 |
| Total losses (w) | 5.92 | 11.82 |
| Efficiency | 96.4% | 93.1% |
5. PERFORMANCE COMPARISON

To show the performance of the proposed converter, the proposed converter and the other multi-input high step-up converters are compared. To have a similar condition, all converters are considered with just two inputs. Voltage gain, number of components, soft switching conditions and main switch voltage stress are listed in Table 5 for comparison. In this table, the gain of the proposed converter is written for the worst case which $D_{\text{eff}}$ is estimated to D. Based on the comparison, the proposed converter has advantages such as high efficiency, fully soft switching, low switch voltage stress and non-pulsating input currents. The voltage gain of [29] and [30] is higher than the proposed converter but [29] suffers from pulsating input currents and [30] has the high input current ripple. In [12], the switches operate under hard switching conditions, which causes more losses and electromagnetic emission. In [21], the voltage gain is higher than the proposed converter but the leakage inductance of the coupled inductors causes voltage spikes across the switch. [31] has higher voltage gain and lower voltage stress of switches than the proposed converter. input currents of [31] are pulsating with a high number of capacitors. In [32], the number of switches is high leading to increased size and cost.

Table 5. Comparison of the proposed converter with other multi-input step-up converters.

| Feature         | Voltage Gain | Number of | Soft switching | Input current | Main switch voltage stress |
|-----------------|--------------|-----------|----------------|---------------|---------------------------|
|                 |              | S D I C   |                |               |                           |
| [29]            | $\frac{1}{D} - \frac{D^2}{1-D}$ | 2 2 2 2 | Hard Hard - - | Pulsating | $V_o + \frac{DV_i}{1-D}$ |
| [30]            | $\frac{3}{1-D}$ | 2 4 2 5 | Hard Hard - - | Nonpulsating | $V_o/2$ |
| [12]            | $\frac{2}{1-D}$ | 2 3 2 4 | Hard Hard - - | Nonpulsating | $V_o/2$ |
| [21]            | $\frac{4n}{1-D}$ | 2 4 2 5 | ZCS ZCS - - | Nonpulsating | $nV_o/2$ |
| [31]            | $\frac{2 + 2n + nD}{1-D}$ | 3 8 8 1 | ZC Hard - - | Pulsating | $V_o$ |
| [32]            | $\frac{6n}{D}$ | 6 4 2 6 1 | ZVS ZVS - - | Nonpulsating | $V_o/3$ |
| Proposed        | $\frac{2}{1-D}$ | 3 4 5 - | ZVS ZVS ZC ZVZ C | Nonpulsating | $V_o/2$ |

Abbreviations: C: capacitor; D: diode; L: inductor; CI: Coupled Inductors; n: turn ratio; S: switch; ZC: zero current; ZV: zero voltage.

6. THE INPUT EXPANSION OF THE PROPOSED CONVERTER

The expansion capability of input sources is a significant property for multi-input converters. The proposed converter with two input can be extended for multi-input applications, as exposed in Fig. 4. Like the design procedure provided in section 3, static gain and relationships of input currents can be obtained as follows:

$$V_{\text{out}} = \frac{V_{in1}}{1-D_{\text{eff1}}} + \frac{V_{in2}}{1-D_{\text{eff2}}} + \ldots + \frac{V_{in_n}}{1-D_{\text{effn}}}$$  (37)
Fig. 9. N-Input version of the proposed converter.

In addition to three and more inputs version as a future work, the proposed auxiliary circuit can be applied and examined for other multi-input converters in which diode-capacitor multipliers are used.

7. CONCLUSION
A dual-input high step-up dc-dc converter is proposed. The auxiliary circuit is employed to achieve the soft-switching conditions for all semiconductor elements. Consequently, the switching losses can be reduced and reverse recovery losses can be eliminated. The proposed structure has high step-up conversion ratio without any coupled inductor or transformer. According to the theoretical, simulation and experimental results, the main switches voltage stress is lower than the output voltage and are turned on and turned off under ZVS condition. The auxiliary switch is turned on under ZCS condition and turned off under ZVZCS conditions. The efficiency of the proposed converter is improved by about 4% in comparison to its hard switching counterpart and makes it suitable for high-voltage applications. Input sources expansion capability and continuous input current (non-pulsating) are other advantages of the proposed converter.

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