A Study of Micro-crack on Surface Mount IC Package

Antonio Sumagpang Jr.1*, Frederick Ray Gomez1 and Edwin Graycochea Jr.1

1New Product Development and Introduction, STMicroelectronics, Inc., Calamba City, Laguna, 4027, Philippines.

ABSTRACT

In integrated circuit (IC) manufacturing industry, package micro-crack and other crack-related flaws are common defect frequently encountered in trim and form process of a surface mount IC package. This paper focused on the prevention of the micro-crack occurrence as it affected the assembly yield performance of the device in focus. Process mapping and defect concentration diagram were done to isolate the location of the defect and the processes involved. Containment and corrective actions were employed to fully narrow down the defect occurrence. Finally, a 99% improvement on defect parts per million (ppm) reduction was observed after implementation of all corrective actions.

Keywords: Micro-crack; trim and form; end-of-line; surface mount; assembly.

1. INTRODUCTION

Package micro-crack has been a chronic problem encountered at trim and form process causing mis-clip on the leaded surface mount integrated circuit (IC) package and resulting to low yield of lots at assembly manufacturing. Challenges really exist especially with new and continuous semiconductor technology trends and breakthroughs. Micro-crack and other package
crack-related defect is defined as a region of material with crack and/or parts missing from a body. The region may or may not progress completely through the component. Actual photos in Fig. 1 shows the signature of micro-crack and/or package crack found on affected units. The photos were taken on a single unit to show the defect on different sides of the unit. This paper focused on the study and mitigation of such assembly defect.

2. LITERATURE REVIEW AND PROBLEM IDENTIFICATION

Process flow for specific end-of-line (EOL) assembly processes in Fig. 2 is used to check if the defect is machine or process related. Worthy to note that assembly manufacturing process flow varies with the product and the technology [1-4]. With new and continuous technology breakthroughs and trends, challenges in IC assembly manufacturing are inevitable [5-8].

Data recovered in assembly yield and issues monitoring given in Fig. 3 indicates significant failure for assembly EOL processes in a span of several months [9]. High level of defect parts per million (ppm) occurrence was documented during this timeline, affecting the assembly yield performance.

Processing history of top 10 affected lots where traced to check if the defects came from a specific mold machine. Fig. 4 shows the defect occurrence coming from 3 different mold machines.
Fig. 4. Top ten assembly lots affected with high number of package crack occurrence

Based on the graph, Mold Machine 1 has the greatest contribution. This is because Mold Machine 1 is dedicated to the device in focus while the Mold Machines 2 and 3 are used on other packages. With this, analysis would focus on the succeeding processes, particularly at trim and form process since lasermarking is unlikely to cause such defect.

3. METHODOLOGY

The device was divided to four quadrants as illustrated in Fig. 5. Tabulation of defect occurrence was made based on the location of package crack per quadrant.

Problem definition tree was established in Fig. 6, identifying the quadrant for further investigation of the micro-crack defect.

The defect signatures were captured during the singulation stage at the trim and form process. Fig. 7 shows the detailed process mapping of the assembly reject.

50 reject units were retrieved for further analysis. Each unit was examined to check variation of the defect considering the signature and location on the affected unit. Criteria for rejects are governed by internal assembly design rules and work instructions [10-11].

Fig. 5. Defect concentration diagram
4. RESULTS AND DISCUSSION

Containment and corrective actions were employed focusing on the trim and form processes and including the molding process. One critical improvement action is to unplug the dispenser hose if epoxy dripping is encountered, to stop the dripping while the machine is under repair. Table 1 enumerates some of the key actions.

Since the problem still existed after the corrective actions were done, an additional electro-pneumatic circuit illustrated in Fig. 8 was recommended.

From the containment action of unplugging the dispenser from the main valve to release the pressure inside the syringe, the circuit was designed to automatically disconnect the dispenser hose from the main valve and release the pressure inside the syringe. This improvement successfully prevented the epoxy dripping.

Large scale validation was done with additional control valve installed. A 99% improvement was achieved for the micro-crack and other package cracks parts per million (ppm) level reduction as shown in Fig. 9. Actual ppm numbers are intentionally not shown due to confidentiality purposes.

Assembly yield performance stabilized after the implementation, optimization, and sustainability of all improvement actions.
Table 1. Improvement actions

| Tasks | Remarks                      |
|-------|------------------------------|
| 1     | Replacement of 5/3 way valve | Problem still exist          |
| 2     | Replacement of PCB W COMP PPD2 board | Problem still exist |
| 3     | Replacement of PCB W COMP PSD - PMC E2 | Problem still exist |
| 4     | Limit hold vacuum maximum setting of 15 millibars | Problem still exist |
| 5     | Optimized dispenser parameter of epoxy viscosity set to require epoxy viscosity specification | Problem still exist |

Fig. 8. Corrective action on epoxy dripping

Fig. 9. Defect ppm level performance improvement
5. CONCLUSION AND RECOMMENDATIONS

Micro-crack defect occurrence was successfully captured at the EOL trim and form process. Containment and corrective actions were done, eventually resulting to the improvement and stabilizing of the assembly yield performance. A 99% improvement in the ppm level reduction was achieved after implementation of all key actions.

It is imperative that improvement and corrective actions be sustained by understanding the wear and tear of the material and equipment involved, for periodic parts replacements and maintenance. Moreover, performance and time analysis must be conducted because corrective and improvement actions are time dependent.

ACKNOWLEDGEMENT

The authors are thankful to the New Product Development & Introduction (NPD-I) team and the Management Team (MT) for the usual great support provided.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Doering R, Nishi Y. Handbook of semiconductor manufacturing technology. 2nd ed., CRC Press, USA; 2007.
2. May GS, Spanos CJ. Fundamentals of semiconductor manufacturing and process control. 1st ed., Wiley-IEEE Press, USA; 2006.
3. Nenni D, McLellan P. Fabless: The transformation of the semiconductor industry. Create Space Independent Publishing Platform, USA; 2014.
4. Harper C. Electronic packaging and interconnection handbook. 4th ed., McGraw-Hill Education, USA; 2004.
5. Liu Y, Irving S, Luk T, Kinzer D. Trends of power electronic packaging and modeling. 10th Electronics Packaging Technology Conference, Singapore; 2008.
6. Sumagpang A, Rada A. A systematic approach in optimizing critical processes of high density and high complexity new scalable device in MAT29 risk production using state-of-the-art platforms. Presented at the 22nd ASEMEP Technical Symposium, Philippines; 2012.
7. Xian TS, Nantha kumar P. Dicing die attach challenges at multi die stack packages. 35th IEEE/CPMT International Electronics Manufacturing Technology Conference, Malaysia; 2012.
8. Tsukada Y, Kobayashi K, Nishimura H. Trend of semiconductor packaging, high density and low cost. 4th International Symposium on Electronic Materials and Packaging, Taiwan; 2002.
9. Sumagpang Jr A, Gomez FR. Specialized singulation punch design for package chip-out elimination. Journal of Engineering Research and Reports. 2019;5(2):1-7.
10. STMicroelectronics. Assembly and EWS design rules for wire bond Interconnect dice. rev. 2019:54.
11. STMicroelectronics. Process work instruction for singulation. Rev. 53; 2020.

© 2020 Sumagpang et al.; This is an Open Access article distributed under the terms of the Creative Commons Attribution License (http://creativecommons.org/licenses/by/4.0), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Peer-review history:
The peer review history for this paper can be accessed here:
http://www.sdiarticle4.com/review-history/56861