HyGain: High Performance, Energy-Efficient Hybrid Gain Cell based Cache Hierarchy

Sarabjeet Singh*†
University of Utah
USA
sarab@cs.utah.edu

Neelam Surana*‡
Ceremorphic
India
neelam.surana@alumni.iitgn.ac.in

Pranjali Jain‡
University of California, Santa Barbara
USA
pranjali.jain@alumni.iitgn.ac.in

Joycee Mekie
Department of Electrical Engineering,
Indian Institute of Technology,
Gandhinagar
India
joycee@iitgn.ac.in

Manu Awasthi
Ashoka University
India
manu.awasthi@ashoka.edu.ac.in

ABSTRACT
In this paper, we propose a “full-stack” solution to designing high capacity and low latency on-chip cache hierarchies by starting at the circuit level of the hardware design stack. First, we propose a novel Gain Cell (GC) design using FDSOI. The GC has several desirable characteristics, including ~50% higher storage density and ~50% lower dynamic energy as compared to the traditional 6T SRAM, even after accounting for peripheral circuit overheads. We also exploit back-gate bias to increase retention time to 1.12 ms (~60× of eDRAM) which, combined with optimizations like staggered refresh, makes it an ideal candidate to architect all levels of on-chip caches. We show that compared to 6T SRAM, for a given area budget, GC based caches, on average, provide 29% and 36% increase in IPC for single- and multi-programmed workloads, respectively on contemporary workloads including SPEC CPU 2017. We also observe dynamic energy savings of 42% and 34% for single- and multi-programmed workloads, respectively.

We utilize the inherent properties of the proposed GC, including decoupled read and write bitlines to devise optimizations to save precharge energy and architect GC caches with better energy and performance characteristics. Finally, in a quest to utilize the best of all worlds, we combine GC with STT-RAM to create hybrid hierarchies. We show that a hybrid hierarchy with GC caches at L1 and L2, and an LLC split between GC and STT-RAM, with asymmetric write optimization enabled, is able to provide a 54% benefit in energy-delay product (EDP) as compared to an all-SRAM design, and 13% as compared to an all-GC cache hierarchy, averaged across multi-programmed workloads.

KEYWORDS
Cache Memory, Emerging Memories, Gain Cell

INTRODUCTION
With the [51] increasing number of cores on-chip [33], additional memory is needed to feed these cores. Emerging workloads have become significantly memory intensive and have large working set sizes [54, 73]. These factors have necessitated the need for high capacity, low latency, on-chip caches.

Several research efforts have been made to increase capacity and contain latency of on-chip caches, which has led to ever-increasing cache capacities and deeper cache hierarchies [54]. However, the memory technology, which makes up the bulk of on-chip caches, has remained unchanged. On-chip caches, at almost all levels of the memory hierarchy, have been devised using 6T SRAM. Even though SRAM suffers from low areal density, high leakage power and high dynamic energy requirements compared to other memory technologies [16, 68, 85], the latency superiority of SRAM, and its compatibility with logic fabrication technology has made it indispensable for creating low-latency caches.

Recently, a number of alternative memory technologies have started to emerge, and have been evaluated for use in caches. Contenders for SRAM replacement include non-volatile memory technologies like Spin-Transfer Torque RAM (STT-RAM) [75, 77, 88] and Phase Change Memory (PCM) [56], as well as volatile ones like embedded DRAM (eDRAM) [16].

In addition to providing data non-volatility, both STT-RAM and PCM provide 3-4× density benefits over 6T SRAM [56, 77], making them attractive candidates for high capacity caches. However, there are drawbacks inherent to both technologies, including higher write energy (up to ~5× that of SRAM) and access latencies (~1.5× read, 5× write latency for STT-RAM, PCM is worse) [56, 77]. In most cases, the drawbacks outweigh the benefits, rendering these technologies suitable for use only in last-level caches, where both capacities and access latencies are expected to be higher. eDRAM has also been evaluated as a candidate for architecting caches [16, 86]. It has found adoption in multiple recent products, including IBM’s Power series [84], Intel’s Haswell [32] and Microsoft’s Xbox 360 [11], again as a technology for LLCs. Since eDRAM is a DRAM variant, it provides higher density compared to SRAM and has favorable
Table 1: Comparison of various memory technologies for on-die caches. Limitations of each technology in bold.

| Total Transistors | SRAM | STT-RAM [37] | PCM[56] | 1T1C eDRAM[5] | 2T GC[76] | 3T GC [30] | 4T GC [28] | Proposed |
|-------------------|------|-------------|---------|--------------|---------|---------|---------|---------|
| Area (um²)        | 0.64 | 0.16        | 0.16    | 0.16         | 0.24   | 0.38    | 0.54    | 0.24    |
| Data Storage      | Latch | Magnetization | Phase | Capacitor   | MOS     | MOS     | MOS    | MOS     |
| Read/Write Time   | Short/Short | Short/Long | Short/Long | Short/Short | Short/Short | Short/Long | Short/Long | Short/Short |
| Leakage/Yield     | High/High | Low/High | Low/High | Low/Low | Low/Low | Low/High | Low/High | Low/High |
| Retention Time    | - | - | - | 20 us | 20 us | 20 us | 1.6 ms | 1.12 ms |
| Destructive Read/ Decoupled Bitline | No/No | No/Yes | No/Yes | Yes/No | No/Yes | No/Yes | No/Yes | No/Yes |

Figure 1: eDRAM LLC energy breakdown.

access latency profiles [16] as compared to NVMs. However, the traditional 1T1C eDRAM cells suffer from low Data Retention Times (DRTs) of 20 - 50 µs [16], requiring frequent refreshes in many eDRAM based design. These refreshes begin to show significant energy consumption as the data from an eDRAM row has to be read and written back [16, 86], making addressing refresh operations as the primary challenge in designing eDRAM caches. The energy consumption breakdown of dynamic and refresh energies for single programmed SPEC CPU2017 and PARSEC workloads in an eDRAM LLC (simulation parameters are listed in Section 7) is shown in Figure 1. As can be observed, refresh energy is many times higher than dynamic energy, which makes optimizing refresh operations an essential consideration for designing eDRAM based caches.

Apart from energy overheads, an eDRAM row, and hence a portion of the cache, is unavailable for the duration of the refresh period, leading to performance overheads. To counter the shortcomings of traditional eDRAM, another eDRAM variant, Gain Cell (GC) has been proposed [30, 76], which has multiple advantages over 1T1C eDRAM. These include a cheaper, logic-compatible fabrication process and the absence of a dedicated capacitor per cell; GCs use the transistor’s parasitic capacitance for data storage. Finally, GCs provide non-destructive reads [16] and decoupled read/write bitlines, resulting in lower access latency and energy consumption [76].

Despite these advantages, traditional 2T and 3T GCs have not found adoption widespread since they suffer from low DRTs, hence requiring frequent refreshes. While 4T GCs with higher DRTs have been proposed [28], they suffer from higher write energies and lower density, making them unattractive as 1T1C eDRAM replacements. In any case, the presence of refresh makes existing GCs useless at any level of cache, other than LLCs [16].

As a result, even though each one of these technologies has its pros and cons, they cannot be used as a drop-in replacement for SRAM caches, especially for levels closer to the CPU. However, in the presence of a suitable SRAM replacement, many of their pros can be combined to architect high capacity caches that have similar latency profiles as that of an SRAM based hierarchy. In this paper, we attempt such a design, starting from ground up. First, we propose a novel FDSOI MOSFET [1] based 2T Gain Cell, which provides high storage density, low access latencies, and a high DRT. This makes the cell amenable for use at all levels of the cache hierarchy. Even after accounting for peripheral circuitry overheads, compared to 6T SRAM, the proposed GC array offers a 50% reduction in read/write energies, 50% reduction in the area while keeping access latency unchanged. It exhibits low leakage energy and has modest refresh requirements. A comparison of advantages of the proposed GC over competing memory technologies for caches is presented in Table 1. The main contributions of this work are summarized below:

- We propose a novel, FDSOI based 2T Gain Cell, specifically for use in on-chip caches, and exploit its back-gate bias feature to reduce leakage power by 99% and increase retention time by ~60×, compared to conventional GC and eDRAM, reducing the need for frequent refreshes. We combine this already large refresh window with optimizations like staggered refresh, to design practically refresh-free GC caches. As a result, proposed GCs can be used at all levels of the cache hierarchy.

- We show that GC based sub-arrays exhibit 2× area advantage and similar latency characteristics as compared to SRAM, even after accounting for overheads of peripheral circuits. This helps architect higher capacity caches within the same area and latency budgets. As a result, for single-programmed workloads, iso-area caches architectured using proposed GCs at all levels of the hierarchy exhibit a 42% reduction in dynamic energy and a 29% increase in IPC as compared to SRAM. Multi-programmed workloads exhibit similar behavior. We further show that the proposed GC scales well at smaller technology nodes, and retains its advantages over SRAM.

- We utilize the inherent decoupling in the read and write bitlines in proposed GCs to save precharge energy between consecutive writes, and clubbing up to 70% writes with reads, thereby improving performance and reducing dynamic energy consumption by 13%, as compared to GC based caches lacking this optimization. We also explore optimizations like no-refresh policy, where a line is invalidated if it is not accessed during its DRT period, and show that this can be used
as an effective mechanism to eliminate refreshes in caches closer to the CPU without performance penalties.

- Finally, to create high capacity, low latency caches, we evaluate several hybrid cache hierarchies by incorporating emerging technologies like STT-RAM with GCs to design caches that can provide up to 4× higher capacity, compared to iso-area SRAM caches. For multi-core workloads, hybrid caches architected with GCs, combined with asymmetric writes optimization, can provide 43% performance and 44% energy benefits as compared to iso-area SRAM caches.

The remainder of this paper is organized as follows. We provide the circuit level implementation details for proposed GC in Section 2 and details of the architectural implementations of GC caches in Section 3. Section 4 presents the experimental evaluation setup, while Section 5 analyses the energy and performance implications of the implementations. Section 6 proposes optimizations by exploiting intrinsic properties of GC, while Section 7 evaluates hybrid cache hierarchies. Sections 8 discusses the scalability of GC at lower technology nodes and provides an assessment of the no-refresh policy. Finally, we discuss related work in Section 9 and conclude in Section 10.

2 BACK-GATE BIASED GAIN CELL

Gain Cells have started gaining traction owing to their logic-compatible fabrication process, small area footprint, and low energy requirements [28, 30, 76, 79]. GCs have been fabricated and tested in FinFET [72], bulk [10], and FDSOI [28] processes. However, these proposals still suffer from low DRT leading to enormous refresh energy, as shown in Table 1. Earlier, FDSOI devices have been fabricated in 12 nm [4] and are expected to scale down, considering their advantages of higher DRT over FinFET [19, 38]. We implement an n-type 2T GC on an FDSOI device [1, 65] and exploit its back-gate bias feature to lower the leakage current, thus improving the DRT.

2.1 Using Back-gate Biased FDSOI to increase DRT

Data retention time (DRT) of a transistor is directly linked with the leakage current of the transistor in the OFF condition. The leakage current (I_{OFF}) in turn, exponentially depends on the threshold voltage (V_{TH}) of the transistor. In the recent past, with technology scaling, leakage has prohibitively increased in bulk-MOSFETs necessitating significant manufacturing efforts and additional fabrication steps to control the leakage current. Silicon-on-Insulator (SOI) technology offers a promising solution to deal with leakage current due to an additional handle to control the threshold voltage using its back-gate biasing. The junction leakage currents are significantly reduced in a fully-depleted SOI (FDSOI) as an oxide layer removes the p-n junction from the substrate, and has been used in a few commercial offerings, including IBM’s POWER 8 [26]. Due to this oxide layer, the substrate works as a second gate or the back-gate [71], and can be biased to change the threshold voltage of the FDSOI transistor which, in turn, exponentially reduces the leakage current [13, 24, 61, 81, 89, 90], and increases the DRT of the transistor.

We have implemented the n-type transistor using STMicroelectronics 28-nm FDSOI technology and simulated it using Cadence Virtuoso. Figure 2(a) captures the effect of back-gate biasing (V_{bg}) on threshold voltage, when V_{bg} is varied between −2V to 2V. Figure 2(b) shows the exponential dependence of I_{OFF} on V_{bg}, and as V_{bg} becomes more negative, the leakage current exponentially drops by almost four orders of magnitude, up to 10 pA/µm. Figure 2(b) also shows the improvement on I_{ON} (on-current) when V_{bg} is positive. Improvement in I_{ON} makes the transistor operate faster, thus reducing delay. Thus, back-gate biasing can be used both to improve performance (latency) and reduce leakage. The schematic of the proposed FDSOI based Gain Cell is shown in Figure 3a. During hold condition, -V_{DD} is applied to the back-gate bias of the device, which reduces the leakage from W1, improving DRT.

2.2 Overheads of back-gate biasing

Leveraging back-gate bias for DRT improvement leads to the reduction of ON current of n-type FDSOI, as depicted in Figure 2(b), and hence, higher cell access latency. To capture the best of both worlds, we apply zero back-gate bias during read and write operations, and -V_{DD} during the hold condition. This can be implemented with the circuit proposed in [20].

Figure 4 shows the layouts of SRAM and proposed 2T GC. To implement back-gate bias, a single contact can be shared across all the cells of a row in an array (as shown in Figure 4(b)). This keeps the area overhead minimal. Since the back-gate oxide thickness is quite large (~20 nm), back-gate carries only 5% of the front-gate capacitance, which keeps switching power overhead less than 5%, while increasing DRT. Additionally, since V_{bg} and row-signal

![Figure 2: The effect of back-gate bias voltage on (a) Threshold Voltage (V_{TH}) (b) Leakage Current (I_{OFF}) and On-state (I_{ON}) in n-type FDSOI transistor.](image-url)

![Figure 3: Schematic diagram of the memory cell.](image-url)
Singh and Surana, et al.  

(WWL) switching happens in parallel, delay of back-gate is overshadowed by WWL’s delay. Hence, back-gate bias causes no latency penalty, negligible area penalty, and has only ~5% of the switching power overhead.

Figure 4: Layout of (a) 6T SRAM Cell (b) Proposed 2T Gain Cell (all cells in a row share a single back-gate, layout shows 2 GCs with shared B-G).

Figure 5: 10K, Monte-Carlo waveforms of 1 and 0 decay (a) Traditional 2T Gain Cell (b) Proposed 2T Gain Cell.

Figure 6: Leakage Power of 6T SRAM, Traditional GC & Proposed GC

2.3 Working of Back-Gate Biased Gain Cell  
(BGB-GC)

Figure 3(a) shows the schematic of the proposed n-type 2T GC. GC has decoupled read and write operations and has non-destructive reads, unlike 1T1C eDRAM. The input signals for these operations are illustrated in Table 2. Working of proposed 2T GC is similar to conventional 2T GC, except that we use back-gate bias during hold condition.

2.3.1 Write Operation. Write Bitline (WBL) is shared across an entire column in an array and has a large capacitance. Write Wordline (WWL) runs along the row in the array. To write to the cell, data is first transferred to WBL, and then a row-signal (WWL) is used to transfer data to the Q node.

2.3.2 Read Operation. For a read operation, Read Bitline (RBL), which is a shared signal across the column, is first precharged to $V_{DD}$. Then, to read data, RBL is kept floating. Active low signal to Read Wordline (RWL) is used to read the data. If data stored in Q is 1, RBL discharges; otherwise it remains at $V_{DD}$, which is sensed by a sense amplifier. During the read operation, energy is consumed in the switching of RBL and RWL. Most importantly, read operation in GC is non-destructive, since RBL is decoupled from the Q node [76].

2.3.3 Hold Condition. Periods where the cell is neither read nor written to is known as the hold condition. This is important since the cell still needs to retain data during this period, unlike SRAM where data is retained due to cross-coupled inverters shown in Figure 3b. The charge in Q node leaks from W1 over time, necessitating refresh operations for data restoration, before the DRT window closes.

2.4 BGB-GC comparison with 6T SRAM

2.4.1 Data Retention Time (DRT). The proposed GC uses back-gate bias voltage of $-V_{DD}$ during hold operation, leading to reduction in leakage current from the W1 transistor, improving DRT. To quantify DRTs, we performed Monte Carlo simulations considering the standard 6-σ local and 1-σ global process variations. Figure 5 shows the data degradation of conventional and proposed 2T GC, for 10K M-C simulations. DRT is measured at a point where the data can be read without error. Typically, $V_{DD}/3$ is a sufficient margin to read data properly, and we consider the worst-case DRT as the refresh interval, making these results more pessimistic than usual. For conventional 2T GC [76], DRT obtained is 19 $\mu$s by considering 100% yield (Figure 5(a)), which is consistent with [28]. For the proposed GC, the data decay has significantly slowed down, as seen from Figure 5(b). We note that the worst-case DRT obtained for the proposed GC improves to 1.12 ms, which is ~60× higher than the case when no back-gate bias is applied. This is first such GC proposal built with 2 transistors leading to significant gains in DRT over existing GC designs, except 4T GC designs [28] where a similar DRT is achieved at the cost of increased area and latency.

2.4.2 Leakage Power. Since the proposed 2T GC has a smaller number of leakage paths compared to SRAM (schematic in Figure 3), it inherently has lower leakage power. Additionally, we have used back-gate bias to further reduce the leakage current significantly. We compare the leakage power of 6T SRAM, GC without back-gate bias, and proposed GC with back-gate bias in Figure 6. We show that proposed GC has ~99% reduction in leakage power as compared to 6T SRAM.

2.4.3 Area. Figure 4 compares the layout of the 6T SRAM cell and 2T GC at 28 nm technology. SRAM cell takes 0.64 $\mu$m$^2$, whereas the proposed GC takes 0.24 $\mu$m$^2$, which is 40% of the SRAM cell.

Table 2: Working of the Proposed Gain Cell

| Operation | WBL | WWL | Back-gate(bg) | RBL | RWL |
|-----------|-----|-----|---------------|-----|-----|
| Read      | Data $V_{DD}$ $0$ | 0 | $V_{DD}$ (floating) | 0 |
| Write     | Data $V_{DD}$ $0$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ |

2.3 Working of Back-Gate Biased Gain Cell  
(BGB-GC)

Figure 3(a) shows the schematic of the proposed n-type 2T GC. GC has decoupled read and write operations and has non-destructive reads, unlike 1T1C eDRAM. The input signals for these operations are illustrated in Table 2. Working of proposed 2T GC is similar to conventional 2T GC, except that we use back-gate bias during hold condition.

2.3.1 Write Operation. Write Bitline (WBL) is shared across an entire column in an array and has a large capacitance. Write Wordline (WWL) runs along the row in the array. To write to the cell, data is first transferred to WBL, and then a row-signal (WWL) is used to transfer data to the Q node.

2.3.2 Read Operation. For a read operation, Read Bitline (RBL), which is a shared signal across the column, is first precharged to $V_{DD}$. Then, to read data, RBL is kept floating. Active low signal to Read Wordline (RWL) is used to read the data. If data stored in Q is 1, RBL discharges; otherwise it remains at $V_{DD}$, which is sensed by a sense amplifier. During the read operation, energy is consumed in the switching of RBL and RWL. Most importantly, read operation in GC is non-destructive, since RBL is decoupled from the Q node [76].

2.3.3 Hold Condition. Periods where the cell is neither read nor written to is known as the hold condition. This is important since the cell still needs to retain data during this period, unlike SRAM where data is retained due to cross-coupled inverters shown in Figure 3b. The charge in Q node leaks from W1 over time, necessitating refresh operations for data restoration, before the DRT window closes.

2.4 BGB-GC comparison with 6T SRAM

2.4.1 Data Retention Time (DRT). The proposed GC uses back-gate bias voltage of $-V_{DD}$ during hold operation, leading to reduction in leakage current from the W1 transistor, improving DRT. To quantify DRTs, we performed Monte Carlo simulations considering the standard 6-σ local and 1-σ global process variations. Figure 5 shows the data degradation of conventional and proposed 2T GC, for 10K M-C simulations. DRT is measured at a point where the data can be read without error. Typically, $V_{DD}/3$ is a sufficient margin to read data properly, and we consider the worst-case DRT as the refresh interval, making these results more pessimistic than usual. For conventional 2T GC [76], DRT obtained is 19 $\mu$s by considering 100% yield (Figure 5(a)), which is consistent with [28]. For the proposed GC, the data decay has significantly slowed down, as seen from Figure 5(b). We note that the worst-case DRT obtained for the proposed GC improves to 1.12 ms, which is ~60× higher than the case when no back-gate bias is applied. This is first such GC proposal built with 2 transistors leading to significant gains in DRT over existing GC designs, except 4T GC designs [28] where a similar DRT is achieved at the cost of increased area and latency.

2.4.2 Leakage Power. Since the proposed 2T GC has a smaller number of leakage paths compared to SRAM (schematic in Figure 3), it inherently has lower leakage power. Additionally, we have used back-gate bias to further reduce the leakage current significantly. We compare the leakage power of 6T SRAM, GC without back-gate bias, and proposed GC with back-gate bias in Figure 6. We show that proposed GC has ~99% reduction in leakage power as compared to 6T SRAM.

2.4.3 Area. Figure 4 compares the layout of the 6T SRAM cell and 2T GC at 28 nm technology. SRAM cell takes 0.64 $\mu$m$^2$, whereas the proposed GC takes 0.24 $\mu$m$^2$, which is 40% of the SRAM cell.
The smaller size of the proposed GC allows for much higher density for the same area.

At the cell level, the proposed GC takes only 0.4× area compared to the 6T SRAM cell. Layout of the SRAM cell is drawn in a very efficient way and have area efficiency of 80%-90%[40, 68, 85]. Considering this, at the cache level, GC can have ~2× capacity as compared to SRAM cache. Even though GC has 2.5× benefits at the cell level, at the cache level, it reduces to 2.0× due to peripheral circuitry overhead. In the rest of the paper, for the iso-area comparison, we have considered 2× capacity of GC compared to the SRAM.

3 ARCHITECTING GAIN CELLS FOR CACHES

First, we describe the sub-array construction of proposed GCs, and the mechanism by which it maps to various cache configurations. Then we compare the architectural benefits of GCs over SRAM.

GCs are arranged as sub-arrays, in a typical row-column fashion. A cache can then be mapped to multiple sub-arrays, as dictated by its capacity. From an extensive design space exploration, we conclude that the sweet spot for minimum latency and peripheral circuitry overheads lie at a sub-array size of 256×512 bits, or 16 KB. Hence, GC caches can be architected such that each way, across all cache sets, maps to one sub-array. As a result, looking up a cacheline (64B) is the same as looking up a row of this sub-array, as shown in the Figure 7. In cases where combined size of a way is >16 KB, we keep adding sub-arrays, until all the sets have been accounted for. For example, the right hand side of Figure 7 depicts a cache where one way is mapped to two 256×512 sub-arrays.

However, this prohibits mapping of any cache configuration where the combined capacity for one way is smaller than 16 KB, as illustrated in the left half of Figure 7. For these caches, we keep the design choice of mapping an entire way to one sub-array, while reducing the size of the sub-array. For example, in the case of a 64KB, 16-way cache, an entire way (4KB) is mapped to a 64×512 bit sub-array. This ensures that a 64 B cacheline lookup is not spread across multiple sub-arrays.

Figure 8 shows the block diagram of the proposed GC cache. Compared to SRAM cache, GC has additional refresh counters at each level of cache. As per concurrent refresh, the refresh counter will generate signal to refresh the same row in all subarrays at the same time. BGB signal is generated along with RWL and WWL signals while performing refresh (no extra delay penalty). For staggering the refresh across different rows, the counter times out after every DRT/N time (N is number of rows in subarray).

Next, we compare and contrast the architecture level characteristics of on-chip caches devised using SRAM and GCs. We extract SRAM and GC energy and latency parameters using an enhanced CACTI [62] model and present these results in Table 3. These results were also validated using SPICE simulations using ST-microelectronics 28-nm FDSOI CMOS technology. We observe that for every cache level, the dynamic read and write energies for a GC cache are reduced by at least 50%, as compared to an SRAM one. This is because the proposed GC requires just one bitline per read or write access, thereby reducing a significant fraction of the dynamic energy consumed in switching of bitlines and word lines [52, 78].

Figure 9: Latency comparison of proposed GC and conventional SRAM caches

Additionally, owing to decoded read and write like 8-T SRAM[68] operations, GC has slightly lower access latencies as compared to SRAM, allowing for similar cycle time access as that of a SRAM cache, for a given processor frequency. Another trait of GC is high density, which enables us to fit a similar capacity cache in half the area. Additionally, in a given area budget, we can implement a higher capacity cache by increasing associativity. As shown in Figure 9, iso-area access latencies of GC based caches at all levels of
the hierarchy are similar to SRAM caches, with additional benefit of GC caches having twice the capacity. Doubling the capacity of an SRAM based cache increases the area by 2.0×. Not only that, it also increases access latency of caches by at least 30%. As a result, GC based caches allow twice the capacity in the same latency and area budget, for every level of cache.

3.1 GC Based Cache Proposals

Using these observations, we propose the use of GCs at various levels of caches, from all on-chip caches architected using GCs (ALL-GC) to just last-level cache (LLC-GC) or L1 cache (L1-GC) being GC, and compare with the baseline case where all caches are implemented with SRAM (ALL-SRAM). Since GCs provide excellent density benefits over SRAM, we examine the energy and performance implications of GC over SRAM for both iso (cache) capacity and iso-area. For iso-capacity (-CAP), SRAM and GC caches are compared with the same cache size, which indicates lower on-chip area usage by GC caches. While in the case of iso-area (-AREA), the GC caches are doubled in capacity by increasing their associativity, while retaining latency characteristics. We maintain the tag array in SRAM; only the data arrays are replaced with GCs.

3.2 Handling Refresh in Gain Cell Caches

One of the biggest challenges in GC caches is the need to refresh. In addition to adding energy overheads, the cache is made unavailable for access during refresh operations, which adversely affects performance. We use a staggered, concurrent refresh mechanism [47] to reduce unavailability of GC cache.

As explained earlier in this section, one way of the cache is mapped to a row in the GC sub-array. Refreshing one row of the sub-array takes 3 ns. We refresh one row in a sub-array at a time and iterate over all the rows in a round-robin fashion in the course of the 1.12 ms refresh window, which is the DRT of an individual cell.

A refresh is done by reading the sub-array in the first 1.5 ns of the refresh window. Data is written back to the row in the second half of the window. As a result, the sub-array is available for write in the first half and a read in the second half. This is made possible due to the presence of separate read and write bitlines. This optimization increases the availability of the sub-array and hence, the associated way – it is now unavailable only for 1.5 ns every 4.375 μs. Since the tags are maintained in SRAM, the cache can still be accessed to check for hits/misses.

We carry out a detailed analysis of performance and energy implications of this refresh policy, in Section 5.3, and conclude that the performance overheads are minimal, since a tiny fraction (0.003%) of cache accesses happen concurrently with refresh, leading to a worst-case 1.7% reduction in performance, as compared to the SRAM baseline.

4 EVALUATION METHODOLOGY

We evaluate our proposed architectures by using an 8-core system with configuration listed in Table 4, simulated using Sniper [15]. This configuration is used as the baseline for evaluation (ALL-SRAM). For iso-area GC caches (-AREA), cache capacity is doubled by doubling associativity. We test our proposals against 25 benchmarks from the SPEC CPU2017 [73] and PARSEC [14] suites and study energy and performance implications in Sections 5.1 and 5.2, respectively. These workloads, listed in Table 5, are simulated for 2 billion instructions each, after a 500 million warmup period. Additionally, to include variations in the application behavior and test against multi-programmed workloads, we divide the workloads in six sets, each consisting of 8 benchmarks, which represents: memory-intensive applications (MEM_HIGH), applications with average memory access (MEM_MED), applications with sparse memory access (MEM_LOW), and three random mixes of 8-workloads (mix1-3). This classification is done based on memory accesses per kilo instructions to caches - higher accesses means more memory intensive. Also, we create six homogeneous multi-programmed workloads (8x*) - 8 copies of the same benchmark, each per core.

Table 4: System Configuration (ALL-SRAM)

| Processor | 8-core, 3.4GHz, x86_64 ISA, 19-stage OOO |
|-----------|----------------------------------------|
| Decode/ Rename/ Fetch Width | 4/4/4 fixed, 4, 6 instructions per cycle |
| Issue/ Dispatch/ Commit width | 4, 6, 4 fixed p-ops per cycle |
| ROB/Branch misprediction penalty | 168 entries/cycles penalty |
| L1-LLC-1D cache | 32 KB, 8-way & 2 cycles. 64B line |
| L2 cache | 256 KB, 8-way & 5 cycles. 64B line |
| L3 cache | Shared 8 MB, 6-way & 10 cycles. 64B line |
| Main Memory | 406MB DDR3, 100 ns access, Read/Write Energy per 64B (nJ) = 41,654.4 |

Table 5: Workloads

| Single-Programmed | Multi-Programmed |
|-------------------|------------------|
| SPEC CPU2017      | MEM_HIGH         |
| parfait_r, gcc_r  | castellanSSN_r, mixl_r, streamcluster, gcc_r, canneal, osmtpg_r, facesim, perlbench_r |
| bwaves_r, mcf_r   |                                |
| cannealSSN_r, parset_r |                |
| povray_r, bm_r    |                                |
| omnetpp_r, sifir_r |                                |
| xalancbmk_r, cam4_r |                                |
| deepjeng_r, imgick_r |                                |
| nab_r, toms_r, xz_r |                                |
| PARSEC            | MEM_LOW          |
| canneal, decip_r  | raytrace, parset_r, fluidanimate, nab_r, dedup, imgick_r, toms_r, dedup, bm_r, freqmine |
| facesim, ferret   |                                |
| fluidanimate, freqmine |                           |
| raytrace, streamcluster |                          |
| mixl              | MEM_MED          |
| parfait_r, ferret_r, parset_r, canneal, osmtpg_r, cam4_r, deepjeng_r, imgick_r, nab_r, streamcluster |                                |
| mixl              |                                |
| mixl              |                                |
| mixl              |                                |
| mixl              |                                |

5 EVALUATION OF GC CACHES

In this section, we quantify the benefits of various GC based architectures and compare them with SRAM based caches. The evaluation includes a study of memory subsystem energy, performance, and the impact of refresh operations.

5.1 Energy Analysis

While most emerging memory technologies exacerbate energy requirements of the memory subsystem [16, 49, 91, 92], GCs, on the contrary, provide significant energy savings over SRAM. In comparison with the baseline SRAM, at the array level, proposed GC design consumes ~46% less energy per read and 40-50% less energy per write, as shown in Table 3.

The ALL-SRAM case, where all levels of caches are assumed to be SRAM, is used as the baseline. We first study ALL-GC-CAP, where we replace all SRAM caches with the same capacity GC caches (iso-capacity). Next, we evaluate iso-area GC caches with configuration listed in Table 4.
double capacity. For this, we evaluate three configurations: (a) L1-GC-AREA, where we replace L1 cache in ALL-SRAM with a double capacity GC cache, (b) LLC-GC-AREA, where we replace last-level cache in ALL-SRAM with double capacity GC, and (c) ALL-GC-AREA, where we replace all levels of caches in ALL-SRAM with double capacity, iso-area GCs.

Figure 10 compares the dynamic energy consumed by the memory subsystem in proposed architectures, for both single and multi-programmed workloads. We calculate the dynamic energy consumption of caches and main memory by taking the product of the total number of accesses to each level with the energy consumption per access using the per bit cache access energy (mentioned in Table 3). Access energies of main memory are obtained from [3] and are presented in Table 4. We observe that any cache hierarchy devised using GCs exhibits savings in dynamic energy. In L1-GC-AREA, where only the L1 is architected using proposed GCs, results in a 36% reduction in dynamic energy, averaged across all the single programmed benchmarks. The LLC-GC-AREA configuration, which replaces the SRAM LLC with a double capacity GC cache, also exhibits a 4% average reduction in dynamic energy. Similar results are obtained for multi-programmed workloads as well. For the memory-intensive mix (MEM-HIGH), the energy savings of L1-GC-AREA and LLC-GC-AREA stand at 25% and 9%, respectively.

Finally, using GC for all levels of the cache increases these gains tremendously. On average, across the single programmed workloads, ALL-GC-AREA achieves 42% (34% in the case of multi-programmed) reduction in dynamic energy consumption as compared to the ALL-SRAM baseline. Even in cases where the area density benefits of proposed GCs are not being utilized, i.e., in the sub-optimal configurations of ALL-GC-CAP, where all SRAM caches are replaced with equal capacity GC caches, we observe an average reduction in the dynamic energy of 34% and 28% for single and multi-programmed workloads respectively.

Compared to the baseline, applications like streamcluster and mcf_r, that have large number of memory accesses, achieve up to 80% reduction in dynamic energy for iso-area GC LLCs (LLC-GC-AREA). Increasing LLC capacity allows the working set of these applications to reside in the cache, reducing the number of off-chip accesses substantially (by ~99%). Reduced off-chip accesses reduce the high off-chip dynamic energy, resulting in massive energy savings. Additionally, in a large, many-core CPU running at a low voltage, leakage from on-chip caches contributes substantially to the chip’s power draw [7]. Proposed GC, with a large savings of 99.3% in leakage energy, as depicted in Figure 6, helps reduce these costs substantially.

5.2 System Performance

Figure 11 illustrates the system performance in terms of instructions per cycle (IPC) for various proposals, using single and multi-programmed workloads. We observe that the performance difference between iso-capacity SRAM caches (ALL-SRAM) and GC caches (ALL-GC-CAP) is negligible - 0.1% drop in IPC for GC caches on average, with respect to ALL-SRAM. All GC based iso-area caches (ALL-GC-AREA) exhibit performance gains as compared to the baseline. Average performance increase of 29% and 36% is observed across single and multi-programmed workloads, respectively. In the case of multi-programmed workloads, memory-intensive workloads tend to benefit most. We observe a 27% performance increase for MEM_HIGH workloads mix, as compared to the baseline. We verified our results on an aggressive processor configuration, with better prefetcher, replacement policy and DRAM access latency [35, 63, 74], and observed similar benefits (<4% IPC drop from above reported benefits).

Applications like streamcluster, canneal, and mcf_r have working set sizes that exceed the capacity of baseline SRAM caches. Hence, when the LLC size is doubled (LLC-GC-AREA), they see large performance improvements (>200%) as working sets can reside on caches. While, many applications like cactuBSSN_r and gcc_r have working sets that reside in the on-chip memory and leverage larger cache size to fit working sets in the L1 cache. As a result, they achieve significant performance improvements in L1-GC-AREA implementation (drop-in accesses to next level caches by >90%) but not in LLC-GC-AREA. On average, L1-GC-AREA and LLC-GC-AREA achieve IPC improvements of 13% and 15%, respectively.

5.3 Impact of Refresh

Regular GC based caches are required to refresh cells at regular intervals. Unfortunately, this has adverse effects on both energy and performance. 1T1C eDRAM and traditional 2T, and 3T GCs can have huge refresh energy overheads, accounting for up to 97% of total LLC energy, as was observed in the experimental results presented in Figure 1.

However, for caches designed using the proposed GC, owing to high DRTs and staggered refresh mechanisms, we observe that the refresh energy consumption is minimal, assuming the most pessimistic scenarios. For experiments carried out with an all GC based cache subsystem (ALL-GC-AREA), which should exhibit the worst case refresh energy consumption profile, we observe that on average, across all single programmed benchmarks, refresh energy contributes <3% (6%, at max for ferret) of the total energy consumption of all caches. We illustrate these observations in Figure 12. For this worst case, we show that refresh energy has an insignificant
Singh and Surana, et al.

Figure 11: System performance for single & multi-programmed (IPC is added across all cores) workloads. Normalized against ALL-SRAM.

Figure 12: Percentage of accesses to the cache which arrive when the cacheline is being refreshed (y1-axis). Breakup of energy consumption of caches, normalized to total energy (Dynamic + Refresh) (y2-axis). Configuration used is ALL-GC-AREA.

correction: But do the refresh operations not affect performance adversely, as demonstrated from ALL-GC-CAP results from Section 5.2. This is evidenced by the fact that caches spend only 0.008% of the time on refresh, on average. Our experiments show that, on average, ~0.003% of accesses to caches were made during refresh interval throughout the entire simulation (Figure 12, y1-axis).

6 ASYMMETRIC WRITES

To read/write a value in a 6T SRAM cell, the bitlines first have to be precharged to \( V_{DD} \). Then, wordlines are turned on to access the cell value. On a read, both bitlines are precharged to high (\( V_{DD} \)) while on a write, one bitline is driven to high and other to low \([68, 85]\). In proposed GC, we have separate bitlines for read (RBL) and write (WBL), as depicted in Figure 3a. Due to this decoupling, there is no need to precharge the WBL to \( V_{DD} \) before every access, unlike in SRAM where the bit lines are pre-charged to \( V_{DD} \) before every write. To perform a write, the WBL is precharged to high or low, depending on the value to be written. For instance, to write a 0, WBL will initially be connected to ground to establish the voltage difference to drain the charge in the cell to 0. Thus, if WBL was already set to 0, driving it again to 0 would require no energy. Such cases arise when the consecutive writes by WBL are the same, i.e., 0 \( \rightarrow \) 0 or 1 \( \rightarrow \) 1 transitions. In these cases, the second write will have a 0.48 – 0.67 \times lower energy consumption as compared to a similar transition in 6T SRAM, as depicted in Table 3.

We quantify the overall dynamic energy savings due to such asymmetric writes by calculating the number of dissimilar bits between two consecutive writes. Dissimilar bit writes are serviced normally, while writes with similar bits are serviced with reduced energy. The reduced energy parameters for caches, extracted from CACTI, are depicted in Table 3. We perform this experiment with ALL-GC-AREA configuration and present our results in Figure 13. On y1-axis, we present the ratio of dissimilar bit writes to total bit writes, for each cache. Lower ratio implies that a lot of the data being written is similar to the value of the WBL, and hence can be written with lower write energy. Accordingly, we calculate the overall dynamic energy consumption (cache + main memory) and compare it with baseline ALL-SRAM and ALL-GC-AREA proposals on y2-axis. We observe that most bits ~76%, averaged across all levels of caches, in write data are similar to the write bitline’s value. SPEC CPU2017 workloads rarely have writes which are larger than 8Bytes \([73]\). The rest of the cacheline is re-written with the same value. This is true for all data caches, with L1D exhibiting as high as 94% similarity, averaged across all benchmarks. Even in cases, where the initial access was a miss, and the existing cacheline has to be replaced with a new one being brought in, we observe significant data similarity between the new and the old lines. For instance, L1 I-cache, which only experiences writes as insertions of new cachelines, observes a 55% data similarity between the old and new lines. As a result, we observe a 13% reduction in dynamic energy consumption, with respect to ALL-GC-AREA, and 50% compared to baseline SRAM-based cache subsystem (ALL-SRAM). Applications with higher write ratios \([73]\) tend to save more energy, for example, parest_r, omnetpp_r, xalancbmk_r, and povray_r. Therefore, we show that, because of its inherent structure, GC can take advantage of write similarity in data to further save on dynamic energy.

Additionally, due to decoupled bitlines, reads and writes to the same sub-array can be done in parallel. We use this property to overlap writes with simultaneously occurring reads to the same sub-array. We note that 40% of all writes could be overlapped with some reads, represented by line-graph Overlaps in Figure 14. Most of the overlaps happen in L1-D cache, as L2 and L3 caches have more sub-arrays and experience a smaller number of writes than L1. By hiding the latency of these writes, we observe a \( \sim \)2% increase in IPC compared to ALL-GC-AREA, presented by GainbyOverlaps in Figure 14. To further take advantage of decoupled bitlines, smart...
cacheline placement policies or buffering can be used, which can potentially increase the number of overlaps. However, we do not pursue these optimizations due to the lack of substantial returns on either performance or energy.

7 HYBRID CACHE HIERARCHY

A growing body of research has proposed either eDRAM or STT-RAM as a replacement for LLCs [16–8, 18, 39, 45, 53, 69, 75, 77, 88]). In this section, we build on prior work to evaluate hybrid cache hierarchies, in an effort to build efficient SRAM “free” on-chip caches.

First, we compare proposed GC based caches with other, state-of-the-art memory technologies. We consider the architectures, where L1 and L2 caches are kept as GC and use either eDRAM or STT-RAM in LLC, namely “GC-GC-eDRAM” and “GC-GC-STTRAM” respectively. STT-RAM parameters were taken from [53], while parameters for eDRAM are obtained from CACTI simulations, and are listed in Table 6. In our experiments, we consider state-of-the-art refresh-optimized eDRAM [6] which achieves ~20× reductions in the number of refreshes over regular eDRAM at 2%-3% area overhead.

We compare these technologies with ALL-SRAM and present “GC-GC-Hybrid” results in the sweet spot of high performance and low energy.

Table 6: LLC parameters for different technologies

| Technology     | eDRAM 32MB | STTRAM 32MB | Hybrid 8MB STTRAM
|----------------|------------|-------------|------------------|
| Read Latency (ns) | 5.13 (18) | 25 (89)    | 2.93 (10) 26 (89)|
| Write Latency (ns) | 5.13 (18) | 60 (204)   | 2.93 (10) 60 (204) |
| Read/Write Energy / bit (pJ) | 5.3/6.32 | 3.5/7.85 | 3.61/8.52 3.5/7.85 |
| Refresh Interval Period (10^21 rec) | 1.125ms | - | 1.125ms 1.125ms |

As expected, the energy consumption of hybrid design is very close to that of ALL-SRAM. It helps it achieve 2.3% (4% for multi-core) improvement in IPC over ALL-GC-AREA, which makes a case for an eDRAM-based LLC. However, eDRAM has large refresh overheads. Even the refresh-optimized eDRAM [6] (GC-GC-eDRAM) results in 21% (12% for multi-core) more total energy consumption than ALL-GC-AREA. Traditional eDRAM results in much worse energy overheads ~ 6.8× higher energy consumption as compared to ALL-GC-AREA.

STT-RAM, with the same 2× density benefits over GC, suffers from much longer access latencies, which have been enumerated in Table 1. As a result, configurations with STT-RAM LLC experienced a performance drop of 7% with respect to ALL-GC-AREA, even though the number of off-chip requests actually dropped significantly by 13%. However, in realistic cases (multi-core runs) that take advantage of larger LLC, GC-GC-STTRAM performs slightly better than ALL-GC-AREA. Consequently, with smaller off-chip accesses, energy consumption reduces by 5%, compared to ALL-GC-AREA, concluding that STT-RAM LLC would be a better design.

In an effort to get the best of all worlds: utilize higher density of STT-RAM, and low latency of GC, we propose hybrid LLC designs of GC and STT-RAM. We selected STT-RAM to avoid the high energy overheads imposed by eDRAM. We carried out a design space exploration for the optimal size partitioning between GC and STT-RAM, while maintaining the area budget as SRAM, and found that equal-area (8 MB GC, 16 MB STT-RAM) distribution resulted in the sweet spot of high performance and low energy. The parameters of this organization are listed in Table 6. The ways of each set of the hybrid cache are split between GC and STT-RAM cachelines, in the ratio of capacity. On a cache lookup, tags of both GC and STT-RAM ways are read and compared. If there is a hit in one of the GC ways, a read or write is carried out. On a miss in GC ways, but a hit in STT-RAM way, the cacheline is moved to the LRU position in the GC ways. Since GC ways tend to have “hot” data, in order to exploit temporal locality, the evicted cacheline from GC way is moved to the LRU position of the STT-RAM ways. In case of a miss in both GC and STT-RAM ways, the cacheline is fetched from the next level and placed in the LRU position of STT-RAM ways. The proposed hybrid cache architecture can be further optimized via novel replacement policies and prefetchers, which we leave for future work [9, 46]. With L1 and L2 cache as GC, and a hybrid LLC, we evaluate the architecture, results of which are compiled in orange bars of Figures 15 & 16, under “GC-GC-Hybrid”.

As expected, the energy consumption of hybrid design is very close to that of ALL-GC AREA: within 2%, on average, across both single and multi-core benchmarks. More importantly, the increased LLC accesses, due to larger cache, are performed with lower latency.
latencies of GC. As a result, we observe 5% improvement in IPC over ALL-GC-AREA baseline, averaged across multi-core simulations. Compared to the traditional SRAM hierarchy, our proposal shows 24% better performance with 42% less energy consumption (43% better with 36% less energy, in case of multi-core). These designs can be further optimized by exploiting decoupled bitline optimizations proposed previously, resulting in an extra 13% savings in energy, as discussed in Section 6, leading to overall 50% (44% in case of multi-core) saving in energy as compared to ALL-SRAM. In conclusion, while GC works best for L1 and L2 caches, real environments require large-capacity LLC with low latency, which can be addressed with our proposed GC-STTRAM hybrid LLC design. In the hybrid design, we move the recently accessed cachelines to the GC part of hybrid LLC, thus serving them with lower latency, if locality exists.

In summary, we present Energy-Delay Product (EDP) results of various architectures in Figure 17. As can be observed, for both single and multi-programmed workloads, any GC based hierarchy does better than the baseline SRAM one. The most favorable design point is obtained by utilizing the benefits of asymmetric write-optimized GC caches at all levels, and a hybrid STT-RAM - GC LLC. This architecture achieves an EDP which is 0.46× of the baseline SRAM one.

8 SCALABILITY OF PROPOSED CACHES

As the technology scales down, transistors become leakier with smaller storage capacitances, resulting in smaller DRTs, exacerbating the refresh problem. This means that at lower technology nodes, GC based caches, due to a large number of refreshes, could perform worse than traditional SRAM based caches. To understand scalability characteristics of proposed GCs, we carry out experiments to characterize the energy consumption of proposed GC with technology scaling.

We carry out our analysis for 28, 22, 14, 10, and 7 nm technology nodes. Generally, leakage current and device capacitance are inversely proportional to technology node [2, 85]. So, scaling down to the next technology node would result in DRT reduction by ~50%. Additionally, cell access energies also decrease by ~50% as we move to lower technology [85]. Considering these trends, we simulate ALL-SRAM and ALL-GC-AREA configurations and calculate dynamic and refresh energy consumptions. At each technology node, we normalize ALL-GC-AREA’s energy consumption (dynamic + refresh) compared to ALL-SRAM’s energy consumption (dynamic) and present the results in Figure 18. Due to space constraints, we present only 15 benchmarks, 5 each from different memory intensity groups listed in Table 5. The first five benchmarks are from MEM_HIGH, followed by MEM_MED and MEM_LOW.

We observe that as we move to lower technology nodes, the contribution of refresh energy increases considerably. At 7 nm, the energy consumption of GC based caches (ALL-GC-AREA) is almost comparable to SRAM based caches (ALL-SRAM). Therefore, at 7 nm or lower, proposed GC, due to refresh, can perform worse than SRAM. Many techniques [6, 7, 80, 86] have been explored to reduce refreshes if it becomes a problem. We propose to reduce the refresh energy by increasing the back-gate bias voltage. Figure 2 shows reduction in leakage current with increasing back-gate bias voltage in a negative direction. This increases the cell’s DRT, which decreases refresh frequency and hence, energy. In Figure 19, for three technology nodes, we show that the actual DRT of rows can
be much higher than the worst case, for which we have to design refresh mechanisms. A potential solution to avoid that could be to use architectural solutions like RAIDR [55] and implement separate refresh intervals for different rows based on their actual DRTs. This can be achieved by dividing the rows into DRT bins and applying a different refresh interval for each bin, leading to a reduction in the number of refresh operations.

8.1 Refresh Free Hybrid Cache Hierarchy

Another key solution which reduces the effect of refresh is a No Refresh Policy (NRP), where rather than refreshing a cacheline, we invalidate the data if the line has not been touched after a refresh operation has been performed, but before it reaches its DRT. The key observation here is that if a row is accessed, the countdown for its DRT is reset, starting the refresh window from that point. NRP can further be optimized by taking advantage of the high number of writes in caches to reduce such invalidations (similar to [27]). To invalidate GC cachelines, a dedicated, on-chip refresh controller, which generates a pulse at given intervals would be required [7, 31].

We propose to maintain a 5-bit (programmable) saturating counter for every cacheline, which is incremented every 132\textsuperscript{th} epoch of the refresh interval. Once the counter saturates, the cacheline is invalidated. If the cacheline was dirty, it is written back to the next level of the hierarchy. In case of a write to the cacheline, the counter is reset to 0. We implement this policy at 28nm and calculate the number of times a cacheline was invalidated due to DRT expiration and present the percentage of cache read misses due to such invalidations on the y1-axis of Figure 20 and the performance impact of these invalidations on the y2-axis. We observe that NRP in L1 and L2 caches does not cause many misses (<1%), and exhibits similar performance as compared to GC with refreshes - on average, <0.1% and ~1% drop in IPC, for single and multi-programmed workloads respectively. However, extending NRP to LLC generates ~12% new misses due to invalidations. It, therefore, results in 23% (36% for multi-programmed workloads) drop in IPC (as seen from Figure 20) as a miss in LLC results in a request to the main memory. Also, while invalidating, we writeback dirty cachelines. This has negligible (<10MB/s) bandwidth impact on L1 and L2 bandwidth, but results in an average memory bandwidth usage of ~110MB/s across multi-core workloads, which is small but may be unacceptable in many cases. Although NRP doesn’t generate many new writebacks because it preemptively invalidates cachelines which would otherwise have been dirty evictions. NRP can altogether remove refreshes, and hence refresh energy, from L1 and L2 caches, while L3 cache would still need to be periodically refreshed. However, implementing L3 with STT-RAM does not need not refresh. As a result, we conclude that a hybrid cache hierarchy, where the L1 & L2 comprise of proposed GC, and LLC is made from STTRAM-GC hybrid is the lowest energy, highest performance on-chip cache hierarchy with refresh-free L1 and L2 caches.

9 RELATED WORK

**Emerging Memory Technologies for Caches:** Due to scalability and energy issues of traditional SRAM, several studies have been carried out to evaluate emerging memory technologies for caches. STT-RAM, owing to its low leakage energy and density benefits, has been viewed as a promising candidate. However, it suffers from inherent weaknesses - high write latency and write energy. There have been many proposals to alleviate these shortcomings [8, 18, 34, 37, 45, 69, 70, 75, 82, 93].

Another potential replacement for SRAM are eDRAMs, which offer high density, low leakage, similar access latencies, and low dynamic energies. However, eDRAM requires refresh operations to preserve data integrity [36]. As cache size increases, each refresh requires more energy, and more lines need to be refreshed; thus, refresh can potentially become the main source of eDRAM power dissipation. Many studies have been carried out to amortize this effect [7, 16, 31, 56, 80, 86, 87]. For instance, [6] showed that the DRTs of cells in large eDRAM modules exhibit spatial correlations, and exploit this behavior to reduce refresh energy. In contrast, the proposed GC already has insignificant refresh overheads.

**Gain Cell:** Many circuit and array level architectures have been proposed for GCs [10, 21–23, 28–30, 42, 48, 76]. The biggest advantage of the GC is its logic compatible fabrication process - only transistors are used for designing the cell and, therefore, can use the same fabrication process as the processor. Transistor’s parasitic
we demonstrate that a no-refresh policy, where GC based cache lines are invalidated than refreshed, can be a viable implementation for removing refreshes in GC caches closer to the CPU. Finally, we show that proposed GC, in conjunction with emerging memory technologies like STT-RAM can be used to architect SRAM-free cache hierarchies with a much superior energy-delay product as compared to SRAM caches.

REFERENCES

[1] [n. d.]. FDSOI 28 nm Technology. http://www.st.com/bi/content/st_com/en/about/innovation--technology/FD-SOI.html.
[2] [n. d.]. ITRS Scaling. http://www-inst.eecs.berkeley.edu/~ee130/sp06/chp7.pdf.
[3] [n. d.]. Micron Technical Note TN-41-01. http://www.micron.com/products/support/power-calc/
[4] 2018. 12FDX. https://www.globalfoundries.com/technology-solutions/sram/12fdx/
[5] James W Adkisson, Ramachandra Divakaruni, Jeffrey P Gambino, and Jack A Mandelman. 2002. Embedded DRAM on silicon-on-insulator substrate. US Patent 6,350,653.
[6] Aditya Agrawal, Amin Ansari, and Josep Torrellas. 2014. Mosaic: Exploiting the spatial locality of process variation to reduce refresh energy in on-chip eDRAM modules. In Proceedings of the 20th International Symposium on High Performance Computer Architecture (HPCA).
[7] Aditya Agrawal, Prabhat Jain, Amin Ansari, and Josep Torrellas. 2013. Refriment: Intelligent Refresh to Minimize Power in On-chip Multiprocessor Cache Hierarchies. In Proceedings of 19th International Symposium on High Performance Computer Architecture (HPCA).
[8] Junwhan Ahn, Sungjoo Yoo, and Kyoung Choi. 2014. DASCA: Dead write prediction assisted STT-RAM cache architecture. In Proceedings of 20th International Symposium on High Performance Computer Architecture (HPCA).
[9] Junwhan Ahn, Sungjoo Yoo, and Kyoung Choi. 2015. Prediction hybrid cache: An energy-efficient STT-RAM cache architecture. IEEE Trans. Comput. (2015).
[10] Yoshiyuki Ando. 2003. Capacitorless DRAM gain cell. US Patent 6,560,142.
[11] Jeff Andrews and Nick Baker. 2006. Xbox 360 system architecture. IEEE micro 26, 2 (2006), 25–37.
[12] Angelos Areilakis, Fredrik Dahlgren, and Per Stenstrom. 2015. Hycomp: A Hybrid Cache Compression Method for Selection of Data-type-specific Compression Methods. In Proceedings of the 46th International Symposium on Microarchitecture (MICRO).
[13] E. Ashena and M. H. Chowdhury. 2018. A New Power Gating Circuit Design Approach Using Double-Gate FDSOI. IEEE Transactions on Circuits and Systems II: Express Briefs 65, 8 (2018), 1074–1078.
[14] Christian Biema, Sanjeev Kumar, Jaswinder Pal Singh, and Kai Li. 2008. The PARSEC Benchmark Suite: Characterization and Architectural Implications. In Proceedings of 17th International conference on Parallel Architectures and Compilation Techniques (PACT).
[15] Trevor E Carlson, Wim Heirman, and Lieven Eeckhout. 2002. Embedded DRAM on silicon-on-insulator substrate. US Patent 6,350,653.
[16] Christian Biema, Sanjeev Kumar, Jaswinder Pal Singh, and Kai Li. 2008. The PARSEC Benchmark Suite: Characterization and Architectural Implications. In Proceedings of 17th International conference on Parallel Architectures and Compilation Techniques (PACT).
[17] Trevor E Carlson, Wim Heirman, and Lieven Eeckhout. 2011. Sniper: Exploring the Level of Abstraction for Scalable and Accurate Parallel Multi-core Simulation. In Proceedings of International Conference for High Performance Computing, Networking, Storage and Analysis (SC).
[18] Mu-Tien Chang, Paul Rosenfeld, Shih-Lien Lu, and Bruce Jacob. 2013. Technology comparison for large last-level caches (LLCs): low-leakage SRAM, low write-energy STT-RAM, and refresh-optimized eDRAM. In Proceedings of 19th International Symposium on High Performance Computer Architecture (HPCA).
[19] M. Chaudhuri. 2009. Pseudo-LIFO: The Foundation of a New Family of Replacement Policies for Last-level Caches. In Proceedings of the 42nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO).
[20] Xunchao Chen, Navid Koshshavai, Jian Zhou, Dan Huang, Ronald F DeMara, Jun Wang, Wujie Wen, and Yiran Chen. 2016. AOS: Adaptive Overwrite Scheme for Energy-Efficient MLC STT-RAM cache. In Proceedings of the 53rd ACM/EDAC/IEEE Design Automation Conference (ICM).
Kangwoog Cheng, Ali Khakifirooz, Kern Rim, and Ramachandra Divakaruni. 2015. Method and Structure For Forming a Localized SOI finFET. US Patent 8,987,823.

[20] H. S. Vangara and A. J. Martin. 2015. 1.1V to 1.3V 3.5 Power Switch Architecture for Controlling Body Bias of SRAM Array in 28nm UTBB CMOS FDSOI. In 2016 29th International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems (VLSID). 179–184.

[21] Keun-Wook Choe, Gyung-Ho Kang, and Jongsun Park. 2015. A refresh-less eDRAM macro with embedded voltage reference and selective read for an area and power efficient Viterbi decoder. IEEE Journal of Solid-State Circuits 50, 10 (2015), 2451–2462.

[22] Ki Chai Chun, Pulkit Jain, Hae-Ko Kim, and Chris H Kim. 2012. A 667 MHz Logic-Compatible Embedded DRAM Featuring an Asymmetric 2T Gain Cell for High Speed On-die Caches. IEEE Journal of Solid-State Circuits 47, 2 (2012), 547–559.

[23] Ki Chai Chun, Pulkit Jain, Jung Hwa Lee, and Chris H Kim. 2011. A 3T Gain Cell Embedded DRAM Utilizing Preferential Boosting for High Density and Low Power on-die Caches. IEEE Journal of Solid-State Circuits 46, 6 (2011), 1495–1505.

[24] S. Cleve, M. Saligane, F. Abouzeid, M. Cochet, J. Daveau, C. Bottoni, D. Bol, J. De-Vos, D. Zamora, B. Coeffic, D. Soussan, D. Croain, M. Naceur, P. Schamberger, P. Roche, and D. Sylvester. 2015. 8.4 A 0.33V/40C Process/Technology Closed-Loop Compensation SoC Embedding all-Digital Clock Multiplier and DC-DC converter exploiting FDSOI 20nm back-gate biasing. In 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers. 1–3.

[25] Krzysztof Flautner, Nam Sung Kim, Steve Martin, David Blaauw, and Trevor Mudge. 2002. Drowsy caches: simple techniques for reducing leakage power. In Proceedings 29th Annual International Symposium on Computer Architecture (ISCA).

[26] Eric J Fluhler, Joshua Friedrich, Daniel Dreps, Victor Zuybom, Gregory Still, Christoph Gonzalez, Allen Hall, David Hogenhalm, Frank Maligiolo, Ryan Nett, et al. 2014. 5.1 POWERS TM: A 12-Core Server-Class Processor in 32nm SOI with 7.6 Th/s off-chip Bandwidth. In Proceedings of the 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC).

[27] Mrinmoy Ghosh and Hsien-Hsin S Lee. 2007. Smart Refresh: An enhanced memory controller design for reducing energy in conventional and 3D die-stacked DRAMs. In Proceedings of the 40th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO).

[28] R. Giterman, A. Fish, A. Burg, and A. Teman. 2018. A 4-Transistor nMOS-Only NVMSA Architecture. In Proceedings of the 18th ACM Great Lakes symposium on VLSI. IEEE, 243–253.

[29] Per Hammarlund, Alberto J Martinez, and Erik Hallnor. 2015. Exploring the cache design space for large scale CMPs. In 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers (ISSCC). 1–3.

[30] SH Kang and C Park. 2017. MRAM: Enabling a sustainable device for pervasive system architectures and applications. In Proceedings of the IEEE International Conference on Computer-Driven Devices Meeting (ICDDM).

[31] E. Karl, Z. Guo, J. W. Conary, J. L. Miller, Y. N. S. Nalam, D. Kim, J. Keane, U. Bhattacharyya, and K. Zhang. 2015. 17.1 A 0.6V 1.5GHz 84MHz SRAM design in 14nm FinFET CMOS technology. In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers. 1–3.

[32] Stefanos Kaxiras, Zhigang Hu, and Margaret Martonosi. 2001. Cache decay, exploiting generational behavior to reduce cache leakage power. In Proceedings 28th International Symposium on Computer Architecture (ISCA).

[33] Amit Kazarminsky, Adam Teman, Noa Edri, and Alexander Fish. 2017. A 0.65×/500-mHz integrated dynamic and static ram for error tolerant applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems 25, 9 (2017), 2411–2418.

[34] S. Khan, A. R. Alamdeeb, C. Wilkerson, O. Mutlu, and D. A. Jimenez. 2014. Improving Cache Performance Using Read-Write Partitioning. In Proceedings of the 26th International Symposium on High Performance Computer Architecture (HPCA).

[35] Samira Manani Khan, Yingsong Tian, and Daniel A Jimenez. 2010. Sampling Dead Block Prediction for Last-Level Caches. In Proceedings of the 43rd International Symposium on Microarchitecture (MICRO).

[36] Navid Khoshavi, Xunchao Chen, Jun Wang, and Ronald F DeMara. 2016. Read-timed sram and edram cache hierarchies for throughput and energy enhancement. arXiv preprint arXiv:1607.08086 (2016).

[37] Namhyung Kim, Junwah Ahn, Kiyoung Choi, Daniel Sanchez, Donghoon Yoo, and Soojong Ryu. 2018. Benzene: an energy-efficient distributed hybrid cache architecture for manycore systems. ACM Transactions on Architecture and Code Optimization (TACO).

[38] Toshiaki Kikihata, Paul Parries, David R Hanson, Hoki Kim, John Golz, Gregory Fredeman, Raj Rajekuvakum, John Griesemer, Norman Robson, Alberto Cestero, et al. 2005. An 800-MHz embedded DRAM with a concurrent refresh mode. IEEE Journal of Solid-State Circuits 40, 6 (2005), 1377–1387.

[39] Wolfgang K Krautschneider and Werner M Klingsenberg. 1994. Process for the Manufacture of a High Density Cell Array of Gain Memory Cells. US Patent 5,308,783.

[40] Emre Kültürsuy, Mahmut Kandemir, Anand Sivasubramaniam, and Onur Mutlu. 2013. Evaluating STT-RAM as an energy-efficient main memory alternative. In Proceedings of International Symposium on Performance Analysis of Systems and Software (ISPASS).

[41] An-Chow Lai, Cem Fide, and Babak Falsafi. 2001. Dead-block prediction & dead-block correlating prefetchers. In Proceedings 26th Annual International Symposium on Computer Architecture (ISCA).

[42] Donghyuk Lee, Yoonhong Kang, and C Park. 2017. MRAM: Enabling a sustainable device for pervasive system architectures and applications. In Proceedings of the IEEE International Conference on Computer-Driven Devices Meeting (ICDDM).

[43] Leslie Lamport. 1986. TEX: A Document Preparation System. Addison-Wesley, Reading, MA.

[44] Raman Manikantan, Kaushik Rajan, and Ramaswamy Govindarajan. 2012. Probability-based eviction and flush decisions forapproximate storage applications. In Proceedings of the 19th International Symposium on High Performance Computer Architecture (HPCA).

[45] K Lee, R Chao, K Yaman, VB Naik, H Yang, J Kwon, NL Chung, SH Jang, B Behin-Aein, HJ Lim, et al. 2018. 22-nm FD-SOI Embedded MRAM Technology for Low-Power Automotive-Grade I/MCU Applications. In Proceedings of the IEEE International Electron Devices Meeting (IEDM).

[46] Junmin Lin, Yu Chen, Wenlong Li, Aamer Jaleel, and Zhizhong Tang. 2009. Underbody biasing for SOI Based SRAM Bitcell Circuit Designs with Different Back-Gate Biasing. US Patent 5,308,783.

[47] Sparsh Mittal and Jeffrey S Vetter. 2016. A survey of architectural approaches for effective Viterbi decoder. IEEE Journal of Solid-State Circuits 50, 10 (2015), 2500–2511.

[48] Wolfgang H Klingsenberg and Werner M Klingsenberg. 1994. Process for the Manufacture of a High Density Cell Array of Gain Memory Cells. US Patent 5,308,783.

[49] Prasanth Mangalagiri, Karthik Sarpwati, Aditya Yanamandra, Vijay Krishna Narayanan, Yuan Xie, Mary Jane Irwin, and Osama Awadil Karim. 2008. A low-power phase change memory based hybrid cache architecture. In Proceedings of the 18th ACM Great Lakes symposium on VLSI. ACM, 395–398.

[50] R Manikantan, Kaushik Rajan, and Ramaswamy Govindarajan. 2011. NuCache: An efficient multicore cache organization based on next-use distance. In Proceedings of the IEEE 17th International Symposium on High Performance Computer Architecture. IEEE, 243–253.

[51] Raman Malinkan, Kaushik Rajan, and Ramaswamy Govindarajan. 2012. Probabilistic shared cache management (PriSM). In 2012 39th Annual International Symposium on Computer Architecture (ISCA).

[52] Pascal Meinerzhagen, Adam Teman, Alexander Fish, and Andreas Burg. 2013. Impact of body biasing on the retention time of gain-cell memories. The Journal of Engineering 2013, 8 (2013), 19–22.

[53] Srinath Mittal and Jeffrey S Vetter. 2016. A survey of architectural approaches for data compression in cache and main memory systems. IEEE Transactions on Parallel and Distributed Systems 27, 5 (2016), 1524–1536.

[54] M. U. Mohammed, A. Nizam, and M. H. Chowdhury. 2018. Double-Gate FD-SOI Based SRAM Bitcell Circuit Designs with Different Back-Gate Biasing

[55] R. Colin Johnson. 2018. FinFETs + FD-SOI Proposition: May Save Power. https://www.eetimes.com/document.asp?doc_id=1327035/.
Configurations. In 2018 IEEE Nanotechnology Symposium (ANTS). 1–4.

Naveen Muralimanohar, Rajeev Balasubramonian, and Norman P Jouppi. 2009. Cache 6.0: A Tool to Model Large Caches. HP laboratories (2009), 22–31.

Kyle J Nesbit and James E Smith. 2004. Data cache prefetching using a global history buffer. In 10th International Symposium on High Performance Computer Architecture (HPCA’04).

Biswaaban panda, André Szencz. 2016. Dictionary Sharing: An Efficient Cache Compression Scheme for Compressed Caches. In Proceedings of the 49th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO).

Nicolas Planes, Olivier Weber, V Barral, S Haenidler, D Noblet, D Croain, M Biocat, P-O Ssoonzas, X Feredispil, A Croz, et al. 2012. 20nm FDSOI technology platform for high-speed low-voltage digital applications. In Proceedings of the 2012 Symposium on VLSI technology (VLSIT).

Moinuddin K. Qureshi, Aamer Jaleel, Yule N. Patt, Simon C. Steele, and Joel Emer. 2007. Adaptive Insertion Policies for High Performance Caching. In Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA).

Moinuddin K. Qureshi, Daniel N. Lynch, Onur Mutlu, and Yule N. Patt. 2006. A Case for MLP-Aware Cache Replacement. In Proceedings of the 53rd Annual International Symposium on Computer Architecture (ISCA).

Jan M Rabaey, Ananthu P Chandrakasan, and Borisivoj Nikolic. 2002. Digital Integrated Circuits. Vol. 2. Prentice hall Englewood Cliffs.

Mitchelle Rasquinha, Dhvruv Choudhary, Subho Chatterjee, Saibal Mukhopadhyay, and Sudhakar Yalamanchili. 2010. An Energy Efficient Cache Design Using Spin Torque Transfer Switch (STT) RAM. In Proceedings of the 16th International Symposium on Low Power Electronics and Design (ISLPED).

Mohammad Hossein Samavatian, Hamed Abbasitabar, Mohammad Arjomand, and Hamid Sarbari-azad. 2014. An Efficient STT-RAM Last Level Cache Architecture for GPUs. In Proceedings of the 51st Annual Design Automation Conference (DAC).

Manuel Sellier. 2018. FDSOI: How Body Bias Creates Unique Differentiation. https://blog.globalfoundries.com/id-soi-body-bias-creates-unique-differentiation/.

Amir Shalom, Robert Giterman, and Adam Terman. 2018. High Density GC-eDRAM Design in 16nm FinFET. In Proceedings of the 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS).

Sarabjeet Singh and Manu Awasthi. 2019. Memory Centric Characterization and Analysis of SPEC CPU2017 Suite. In Proceedings of the 2019 ACM/SPEC International Conference on Performance Engineering.

Alun Jay Smith. 1982. Cache memories. ACM Computing Surveys (CSUR) (1982).

Clintom W Smullen, Vidhyabhusan Mohan, Anurag Nigam, Sudhana Gurumurthi, and Mirea R Stan. 2011. Relaxing Non-Volatility for Fast and Energy-Efficient STT-RAM Caches. In Proceedings of 17th High Performance Computer Architecture (HPCA).

Dinesh Somasekhar, Yibin Ye, Paolo Aseron, Shih-lien Lu, Muhammad M Khel-lah, Jason Howard, Greg Rohi, Tanay Karkik, Shekhar Borkar, Vivek K De, et al. 2009. 2 GHz 2 MB 2T gain cell memory macro with 128 GB/byte/sec bandwidth in a 65 nm logic process technology. IEEE Journal of Solid-State Circuits 44, 1 (2009), 174–185.

Guangyu Sun, Xiangyu Dong, Yuan Xie, Jian Li, and Yiran Chen. 2009. A durable and energy efficient main memory using phase change memory technology. In Proceedings of the 36th Annual International Symposium on Computer Architecture (ISCA).

N. Surana and J. Mekie. 2018. Energy Efficient Single-Ended 6-T SRAM for Multimedia Applications. IEEE Transactions on Circuits and Systems II: Express Briefs (2018).

A. Teman, P. Meinerzhagen, R. Giterman, A. Fish, and A. Burg. 2014. Replica Technique for Adaptive Refresh Timing of Gain-Cell-Embedded DRAM. IEEE Transactions on Circuits and Systems II: Express Briefs 61, 4 (2014), 259–263.

Fengbin Tu, Weiwei Wu, Shouyi Yin, Leibo Liu, and Shaojun Wei. 2018. RANA: Towards Efficient Neural Acceleration with Refresh Optimized embedded DRAM. In Proceedings of the 45th Annual International Symposium on Computer Architecture (ISCA).

A. A. Vatanjou, E. Late, T. Ytterdal, and S. Aunet. 2016. Ultra-Low Voltage Adders in 28 nm FDSOI Exploring Poly-Biasing for Device Sizing. In 2016 IEEE Nordic Circuits and Systems Conference (NORCAS). 1–4.

Zhe Wang, Daniel A Jimenez, Cong Xu, Guangyuan Sun, and Yuan Xie. 2014. Adaptive Placement and Migration Policy for an STT-RAM Based Hybrid Cache. In Proceedings of the 20th International Symposium on High Performance Computer Architecture (HPCA).

Zhe Wang, Samira M. Khan, and Daniel A. Jiménez. 2012. Improving Writeback Efficiency with Decoupled Last-Write Prediction. In Proceedings of the 39th Annual International Symposium on Computer Architecture (ISCA).

James Warnock, Brian Curran, John Badar, Gregory Fredeman, Donald Plass, Vien Chan, Sean Carey, Gerald Salem, Friedrich Schroeder, Frank Malgoglo, et al. 2015. 4.1 22nm next-generation ibm system z microprocessor. In Proceedings of the 2015 IEEE International Solid-State Circuits Conference-(ISSCC) Digest of Technical Papers.