Partition Consistency:
A Case Study in Modeling Systems with Weak Memory Consistency and Proving Correctness of their Implementations

Steven Cheng, Lisa Higham, Jalal Kawash
University of Calgary
stevechy@gmail.com,\{higham,jkawash\}@ucalgary.ca

Abstract

Multiprocess systems, including grid systems, multiprocessors and multicore computers, incorporate a variety of specialized hardware and software mechanisms, which speed computation, but result in complex memory behavior. As a consequence, the possible outcomes of a concurrent program can be unexpected. A memory consistency model is a description of the behaviour of such a system. Abstract memory consistency models aim to capture the concrete implementations and architectures. Therefore, formal specification of the implementation or architecture is necessary, and proofs of correspondence between the abstract and the concrete models are required.

This paper provides a case study of this process. We specify a new model, partition consistency, that generalizes many existing consistency models. A concrete message-passing network model is also specified. Implementations of partition consistency on this network model are then presented and proved correct. A middle level of abstraction is utilized to facilitate the proofs. All three levels of abstraction are specified using the same framework. The paper aims to illustrate a general methodology and techniques for specifying memory consistency models and proving the correctness of their implementations.

Keywords: weak memory consistency models, distributed-shared memory, sequential consistency, processor consistency, correctness of distributed implementations, partial-order broadcast.
1 Introduction

Multiprocess systems including networks, grid systems, multiprocessors and multicore computers, incorporate a variety of specialized hardware and software mechanisms such as replicated memory, multi-level caches, write-buffers, multiple buses, and complex support for message passing. These features help speed computation by hiding latency and avoiding bottlenecks when accessing shared memory. An unfortunate consequence is that the possible outcomes of concurrent programs can be unexpected. Because the processes’ views of the current state of memory at any moment do not completely agree, the execution of a concurrent program may not be sequentially consistent.

Sequential consistency is important. It can be efficiently implemented in the absence of data-races; it supports platform independent code; it is easier to reason about sequential consistency than weaker models. Nonetheless, real systems typically deviate from implementing sequential consistency, resulting in complex memory behavior.

It is therefore necessary to formally and precisely specify what computations can arise on a given system. Such a specification is a memory consistency model. A concrete or low-level memory consistency model would describe possible outcomes in terms of the behavior of the actual system due to its hardware and software architecture. For example, consider a system where each process has a write-buffer. The behaviour of each store($x, ν$) instruction could be separated into a sequence of low-level events: first the value $ν$ for location $x$ is recorded in the local write-buffer, later, the pair $(x, ν)$ is removed from the write-buffer and the shared memory location $x$ is updated to contain $ν$. Similarly, the behaviour of each load($x$) instruction could be separated into the events: consult the write-buffer for a pending store to location $x$; if one exists, return the associated value; otherwise fetch the value of location $x$ from main memory and return that value. Such an operational specification in term of the events that occur in the system when an instruction is executed is a good way to capture exactly what can arise when a concurrent program is executed. A programmer, however, should be spared having to deal with the architectural details; she should be able to reason about her program in terms of the instructions of the program, rather than low level events. An abstract memory consistency model aims to provide such a non-operational specification of the behaviors of concrete architectures and systems. How can we be sure that such an abstract model is correct? What is required is a specification of both the abstract model and the concrete architecture and a proof of their equivalence.

This paper provides a case study of this process. We introduce a new general class of memory consistency models, called partition consistency, which captures different degrees of consistency between various sets of shared variables, as is common in distributed and multiprocessor environments. Sequential consistency [43], Goodman’s processor consistency [5], and the pipelined random-access machine [46] are all instances of partition consistency. The definition of partition consistency is a natural extension of sequential consistency. Implementations of partition consistency on the message-passing network model are presented and proved correct. In contrast to the high-level partition consistency definition, the message passing network is modelled at the level of message sends and receives combined with operations on local memory. It requires several partial orders to capture the relationships between message operations and local memory operations. Although partition consistency is an over-simplification, it is non-trivial and it captures some essential properties of actual implementations.

Our implementations and their proofs of correctness are facilitated by a middle level of abstraction, which generalizes a totally ordered broadcast model to a partially ordered one. Thus we introduce three levels of abstraction: the abstract partition consistency model, the intermediate partial-order broadcast model, and the concrete message-passing network model. The same framework is used to define the memory consistency model of each level. So the intermediate partial-order broadcast model is first the target of the implementation of the specified partition consistency model. Next, the same partial-order broadcast abstraction serves as the specified model, which is implemented on the target message-passing network model. We define the fast-read/slow-write and fast-write/slow-read implementations of partition consis-
tency on the partial-order broadcast model. Next we give two implementations of partial-order broadcast (one token-based and one timestamp-based) on message-passing networks. This results in four compositions of transformations; each implements partition consistency on message-passing networks.

Proofs of correctness of implementations of shared memory models on multiprocessors or networks typically involve a great deal of tedious but essential detail, and are thus prone to imprecision and error. Layering the implementation on levels that are defined using a common framework helps to overcome these problems by allowing us to focus on only part of the proof obligation at each level. We also introduce a diagrammatic notation that provides a visual representation of logical statements and inferences. The precision and conciseness of mathematical logic aids in avoiding some potential ambiguities of consistency proofs, while its representation in diagram format helps keep our intuitions aligned with the proof. This notation helped us uncover errors in our initial implementations and our attempted proofs.

Partition consistency is of independent interest because it supports different consistency guarantees for different partitions of variables. Itanium [39] and Java [49], for example, exhibit differing degrees of consistency depending on how variables are declared. Similarly, abstract consistency models are typically defined by partitioning operations into classes, where processes have different levels of agreement on the order of operations in each class. For example, Sequential consistency (SC) [43] requires complete agreement on all operations; pipelined random-access machine (P-RAM) [46] requires agreement on the write operations by any individual process; in addition to P-RAM, processor consistency (PC-G) [5] requires agreement on the operations on the same variables. SC, P-RAM, and PC-G are all special cases of partition consistency. This paper provides implementations of any instance of the partition consistency class on message-passing networks with multi-threaded nodes.

Some of the authors have used earlier versions of this framework in previous research. For example, it was used to expose problems with the Java specifications when applied to long-lived programs [34], to provide a simple abstract definition for TSO [31], to study the Intel Itanium memory consistency model [32], and to compare Itanium with the SPARC models [28].

Organization of the rest of the paper:

Section 2 discusses related research on modeling and proof techniques as applied to weak memory consistency models. Section 3 provides the framework and the three levels of abstraction used in this paper, by defining the memory consistency of each level. The setup for transformations and their proofs of correctness is given in Section 4. The implementations of partition consistency on partial-order broadcast and their proofs of correctness are given in Section 5. Section 6 (respectively, 7) provides the token (respectively, timestamp) implementation of partial-order broadcast on the message-passing network model, and the proof that the implementation is correct. Section 8 concludes by summarizing the paper and discussing future directions.

2 Related Work

Research concerning systems with weak memory consistency proceeds in several directions. In the following we look at those directions that are related to our work. We first review some formalisms used to specify given systems focusing on the ones that closely resemble our framework. There is a proliferation of abstract memory consistency models aimed at capturing those relaxations of sequential consistency that are common in real systems. We concentrate the next part of our review on the subset of these that are instances of partition consistency. Our work implements partition consistency on the message-passing network model, so we next discuss its relationship to the large body of research concerned with how to make algorithms that are correct for sequentially consistent machines remain correct when run on systems with weaker memory consistency guarantees. The principal goal of this paper is to demonstrate (through the case study of
partition consistency) one strategy for proving the correctness of an implementation of an abstract memory consistency model on a concrete operational model. While an abstract memory consistency model is often used to provide a non-operational model of a multiprocess system, a proof of the correctness of the proposed model is less common. Our final review section discusses other instances of this activity, and related proof techniques.

2.1 Formalisms for modelling systems

There are several formalisms used to specify concurrent systems — the most common types are based on process algebras and automata theory. Process algebras start with a basic set of processes, then combine them into larger systems using various algebraic operators. Communicating sequential processes (CSP) [37] and the calculus of communicating systems (CCS) [50] are classic examples.

In the input-output automata (IOA) language [48], processes are specified as automata that communicate by action synchronization. Actions are designated as input, output, or internal, where each input action is jointly performed with all matching output actions. Actions in IOA are automata transitions that can arbitrarily modify local state. Their effect on local state is specified in an imperative language that is essentially pseudocode. This can make IOA useful for reasoning about algorithms written in imperative programming languages. The input/output matching is similar to CCS, and the fact that more than two processes can participate in a communication action is similar to CSP.

The temporal logic of actions, TLA [45], specifies automata using a mathematical language. It avoids programming languages, making it attractive to hardware designers. TLA also provides many tools for reasoning about automata in general, and can be used with IOA [51].

Another approach is to regard a system as a collection of processes, where each process produces a sequence of instructions invocations (program order). A memory consistency model is a set of partial order constraints on the collection of all instructions of the system. (The model will specify what subsets of program order must be maintained by which processes (their “views”), and to what degree processes’ views must agree.) This is the approach used in this paper; it is defined in Section 3. It is most similar to that used by Steinke and Nutt [59], who observed that all of the models that they were aware of from the literature could be expressed in terms of the existence of serial views that extend certain partial orders.

2.2 Memory consistency models

There is a large body of literature examining various memory consistency models. Steinke and Nutt [59] re-specified several models including Goodman’s processor consistency, sequential consistency, pipelined random-access, and causal consistency in terms of processes’ views, and proved that their definitions are equivalent to those in the literature. Then, they used their partial order definitions to compare the relative strengths of models. Specifically, they arranged 12 models into a lattice, with SC being the strongest model. This research demonstrated a definitional style that is general enough to capture the models in the literature and to facilitate their comparisons. We now informally describe some specific memory consistency models. It is straightforward to recast each using the partial order formalism of Steinke and Nutt as adapted in Section 3.

Sequential consistency is a strong memory consistency model introduced by Lamport [43]; it requires agreement between all system processes on a single view of the all the operations of all processes. This view agrees with the order in which the instructions producing these operations appear in their programs, called program order. An even stronger model, atomic objects as defined by Lamport and by Lynch [47], and linearizability, defined by Herlihy and Wing [27] requires agreement on global timing of operations in addition to sequential consistency.
Lipton and Sandberg [46] introduced a much weaker consistency model than sequential consistency, the pipelined random-access machine (P-RAM) memory model. P-RAM is an example of distributed-shared memory (DSM). It requires a process’s view to include its own operations and all other processes’ writes. The view of a process must be consistent with program order. However, P-RAM allows processes to disagree on the order of two writes performed by two different processes. As a result, P-RAM is so weak that it cannot support a solution to mutual exclusion with only read/write variables [35].

Coherence requires that processes agree on the ordering of operations on each object separately, but not on how the operations on different objects interleave. Coherence is also too weak to support mutual exclusion with only read/write variables [33]. Coherence is a memory consistency model that captures a property that we might expect from any multiprocessing system. Nevertheless, some language memory models, such as Java, are incomparable to coherence.

Goodman’s version of processor consistency (PC-G) [25], as formalized by Ahamad et. al. [5], strengthens P-RAM by adding coherence to it. PC-G executions must simultaneously satisfy both P-RAM and coherence. PC-G is weaker than SC, but it supports mutual exclusion with only read/write variables [35]. Hence, PC-G is one of the few weak models that can be used to implement SC with only read/write variables [36]. Other versions of processor consistency exist, and these versions are incomparable [60].

In this paper, we introduce partition consistency, which defines a family of memory consistency models inspired by PC-G, P-RAM, and SC. Each of these three models is a special case of partition consistency.

In addition to such abstract memory consistency models, the literature contains formalizations of the memory consistency models implemented by concrete multiprocessor machines. Higham, Jackson, and Kawash explore memory consistency models for SPARC [31] and Itanium [29, 30] multiprocessors, including the TSO model, which is claimed to be the consistency model of Intel x86 multiprocessors. The consistency model for Alpha processors is described in the Alpha manual [20] and is formally defined and investigated by Attiya and Friedman [7]. The PowerPC consistency model is formalized by Corella, Stone, and Barton [17]. Sarkar, Sewell, Alglave, Maranget and Williams [55] also aim at faithfully representing the memory model of POWER multiprocessors. This research defines an abstract machine that implements the model, and provides programmers with a high level explanation of how the memory model is implemented by POWER multiprocessors. A large number of manually coded and automatically generated litmus tests are run on various POWER processors to provide confidence that the hardware behaves as the memory model predicts. The Intel architecture developer manual provides some description of an x86 memory model [19], which is also clarified in an Intel whitepaper [18]. Owens, Sarkar, Sewell, Nardelli, Ridge, Baribant, Myreen, and Alglave studied the memory consistency model of the x86 architecture [57, 56, 52].

It is important to study the behavior of highly used programming languages when there is more than one thread of execution and to formalize the resulting memory models. The Java memory model was the subject of a few studies (for instance, see [49], [6], and [34]). The C++ memory model was studied by Boehm and Adve [12] and recently formalized by Batty, Owens, Sarkar, Sewell, and Weber [11]. The partition consistency model is simpler than the models arising from such languages; our focus in this paper is on proving the correctness of implementations of a model.

2.3 Implementations of sequential consistency on systems with weaker memory consistency guarantees

Many researches have address the question of how to ensure that a program that is correct under sequential consistency remains correct and efficient under a weaker consistency model.

Attiya and Welch provide DSM implementations for sequential consistency and linearizability[8], and they examine the difference in these implementations in terms of message delay. Building on Lipton and Sandberg’s lower bound on sequential consistency [46], Attiya and Welch establish that it is more expensive to implement linearizability than it is to implement SC. Cholvi, Fernandez, Jimenez, and Raynal [16]
improve the best-case performance given by Attiya and Welch by showing that sometimes a read can be guaranteed not to incur any message delay. Cholvi et al. present a sequentially consistent DSM protocol that ensures fast writes, but not all reads can be fast. Their implementation uses a single circulated token to synchronize the processors’ copies of memory.

In this paper, we generalize Attiya and Welch’s total-order broadcast algorithm [8] to a partial-order one, allowing us to implement a class of weak memory consistency models. Since our focus is weak memory consistency, our generalization is based on their implementation for SC, rather than linearizability. Brzezinski and Szychowiai [14] provide a DSM implementation for PC-G and prove its correctness. It statically assigns a master node to each variable to ensure coherence. In contrast, our implementations use a timestamp protocol or circulating tokens and is fully distributed.

Agrawal, Choy, Leong and Singh created the Maya DSM [4] to experiment with weak memory consistency models. Amza, Cox, Dwarkadas, Keleher, Lu, Rajamony, Yu, and Zwaenepoel implemented the weak memory consistency model release consistency in their Treadmarks DSM [40]. Adve introduced data-race-free (DRF) programs [2, 3]. DRF programs have that property that there are no data races in any sequentially consistent execution, which can be achieved by insertion of appropriate synchronization instructions. DRF programs are guaranteed to yield sequentially consistent computations on several weak models including release consistency [23, 22].

Shasta and Snir [58] implement sequential consistency on MIMD machines such as the NYU Ultracomputer and IBM RP3. In such machines, a packet-switched network connects processors to multi-ported memory modules that can be simultaneously accessed. Their goal is to gain efficiency by exploiting potential simultaneous accesses to memory. To ensure that sequential consistency is not violated, control instructions are added to delay accesses until the previous one by the same processor is completed, and synchronization code (locks) are used to deal with cases when some memory accesses need to have stronger atomicity than the word-level atomicity provided by the machine. For efficiency, it is important to use these constructs only when necessary. Analysis of interdependence of processes is used to minimize their use. By doing this analysis of a program before it is executed, they show that their implementation “requires far less locking than database control theory would lead one to expect”. Their proofs are primarily set-theoretic in structure. In this paper, we similarly implement sequentially consistency (and other models) but on a message-passing platform.

Kuperstein, Vechev and Yahav [41] developed an algorithm and its implementation (Fender) that infers where memory fences are needed to maintain correctness. Fender takes as input a finite state program, a safety specification and a memory model described by a transition system. For each state, Fender computes an avoid formula that captures all the ways to prevent an execution from reaching the state. Once transitions to invalid states are identified, provided they can be avoided by local fences, such fences can be inserted to ensure that the invalid states are not reachable. This approach is distinctly different from the approach of this paper. It uses an operational definition of the memory consistency model, and a state-based notion of safety, whereas we use a partial-order definition of computations and a predicate on computations to define safety. Our techniques, however, do not provide an automated way to infer where and what kind of synchronization is required.

The CheckFence tool of Burckhardt, Alur, and Martin [15] is another tool to ensure that programs remain correct when executed under weak memory models. It takes as input a program written in a subset of C and an axiomatic memory model, and determine if there is an execution that violates its specification. CheckFence works by combining the axiomatic memory model definition with a compiled version of input program to to form a boolean satisfiability problem. It then calls a SAT solver to find violating executions for finite unrolling of the program. Like Fender, the advantage of CheckFence is that much of the work of checking correctness is automated. It does not, however, directly shed much light on how to fix a program that does permit executions that violate the specification.

Alglave and Maranget [55] provide a class of memory models that can be instantiated to produce se-
quential consistency, Sparc-TSO and a model based on Power processors. They provide theorems on barrier placement needed to regain sequential consistency and a tool called diy to automatically generate litmus tests that detect relaxations of SC. They use a specification style that is similar to what we use in this paper.

Huseynov’s Distributed Shared Memory webpage [38] tracks the available academic and commercial DSM implementations.

In contrast with all of these papers, this paper is concerned with developing techniques to prove that a given (weak) abstract memory consistency model is a correct abstraction of a given architecture.

2.4 Proofs of correctness of concurrent systems

There are several methods to prove the correctness of programs. Hoare established a logic-based approach, which proceeds by showing that a program satisfies specified post-conditions given that its satisfies specified pre-conditions (see Backhouse [10]). Owicki and Gries extended Hoare’s logic to apply to multiprocessor systems (see Feijen and van Gasteren [21]). Reynolds generalized Hoare’s logic to separation logic [54], which facilitates proofs of programs because it allows reasoning about parts of memory independent of the entire global state. Concurrent separation logic [13] combines these two extensions. It is aimed at reasoning about concurrent programs and their shared mutable data structures.

CCS [50] and π-calculus [1] establish correctness proofs by simulating one automaton with another. Proofs proceed by showing that the properties of a simulation imply the specifications. In these approaches, a system execution is a sequence of events. Lamport’s temporal logic of actions (TLA) [45] works similarly except that an execution in TLA is a sequence of states. Lamport’s system executions framework [44] uses a collection of events together with a happens-before partial order and a can-causally-affect relation, where some general axioms for system executions are satisfied. A proof of correctness is constructed by defining a mapping of sets of events to an abstract new event. This mapping induces a happens-before order and a can-causally-affect relation on the set of new abstract events. Hence, a new abstract (high-level) set of system executions are produced from a set of concrete (low-level) system executions. The proof is completed by showing that these high-level executions satisfy the specification. These high-level and low-level descriptions use the same mathematical language, allowing the abstraction process to be applied repeatedly. Lamport’s system executions framework cannot be easily adapted to weak memory consistency models. To more naturally capture weak memory consistency models, we typically use more than one partial order in addition to agreement properties on these orders.

Lamport’s system executions framework does not specify how these executions are generated. Gischer [24] and Pratt [53] address this problem. The execution of an entire program is described as a collection of partially-ordered sets. These posets are generated by applying process algebra operations, such as sequential and parallel compositions, to smaller programs. Thus, a set of posets that represent all system executions can be recursively constructed. Then, simulation techniques are used to prove that the system executions match the specifications.

Many proofs of shared-memory algorithms assume Herlihy and Wing’s strong consistency model, linearizability [27]. A particularly useful and powerful property of linearizability is its locality: proving separately that the implementation of each object in the system is linearizable implies the correctness of the whole system implementation. Usually weak memory consistency models do not have such a locality property, complicating proofs of correctness.

Aspinal and Sevcik use a partial order formalism to represent the Java Memory Model (JMM) [6] in order to prove that data-race-free programs produce sequentially consistent executions on the Java Virtual Machine. The partial order constraints of JMM are used to produce a sequentially consistent total order. Our partial order modeling shares similarity with theirs, but our low-level partial order constraints are used to produce computations that satisfy the partial order constraints of (the high-level) partition consistency, rather than a single total order.
3 Definitions and Models

An operation consists of an operation invocation and an operation response often involving shared objects. We use completed operation to emphasize that an invocation is paired with a response. A thread generates a sequence of operation invocations in a sequence called program order. A process consists of a finite collection of threads. A multiprogram is a finite collection of processes.

A computation of the multiprogram is formed by arbitrarily completing each operation invocation, in each individual thread sequence, with a response, creating a collection of sequences of completed operations. Program order on operation invocations is naturally extended to define program order on the set of completed operations of a computation. That is, a computation consists of a set of sequences of operations, one sequence of operations for each thread of each process. We denote this unrestricted set of computations of a multiprogram \( C(P) \) that could actually result from the execution of the multiprogram depends upon the distributed system’s architecture. A memory consistency model is a predicate defined on the set of all possible computations of a multiprogram; it filters these computations to include only those that could arise on the architecture being modeled. The subset of \( C(P) \) that satisfies the memory consistency predicate, MC, is denoted \( C(P, MC) \).

We use the following notation, terminology and conventions for the rest of the paper. For a computation \( C \) of a multiprogram \( P \), \( O_C \) denotes all the operations of \( C \). A completed operation \( OPER \) with input \( u \) that returns a value \( v \) is denoted \( OPER(u)_v \). For a set of operations \( O \), \( O|\text{wrets}(S) \) denotes the subset of all write operations to variables in \( S \); if \( S \) is all the variables, we write \( O|\text{wrets} \); \( O|P \) denotes the subset of all operations by process \( p \in P \). The program order relation on \( O_C \), denoted \( PORDER \), is the partial order formed by the union of the individual thread program orders\(^1\). For all these notations we omit the subscript \( C \) when it is obvious. When we need the individual program order for a particular process or thread \( p \), we write \( PORDER_p \). The style \( \text{pred}[\text{args}] \) is used to denote a predicate. Given relations \( \rightarrow^R, \rightarrow^T \), and a set \( A \), define extension and agreement predicates on relations by:

- \( \text{Extends}[A, \rightarrow^R, \rightarrow^T] \equiv \forall a_1, a_2 \in A : a_1 \rightarrow^R a_2 \implies a_1 \rightarrow^T a_2 \)
- \( \text{Agree}[A, \rightarrow^R, \rightarrow^T] \equiv \forall a_1, a_2 \in A : (a_1 \rightarrow^R a_2) \iff (a_1 \rightarrow^T a_2) \).

Given a total order on a finite set, there is only one sequence of all the elements of the set that realizes that total order. Therefore, we sometimes overload the term total order for a finite set \( A \): it refers to either the set of ordered pairs \( (A, \rightarrow^T) \) in the order, or the sequence, which we denote by \( T \), that realizes that total order. The notation \( \{ x_a : a \in A \} \) specifies a collection of items \( x_a \), exactly one for each \( a \in A \).

The most common shared objects for this paper are variables with the sequential specification [27]: a sequence of \texttt{read} and \texttt{write} operations on a variable \( x \) is valid if each \texttt{read}(\( x \)) returns the value written by the most recent preceding \texttt{write}(\( x, \cdot \)) in the sequence (or the initial value if no such \texttt{write} exists). Other shared objects will be defined later as needed. Any sequence of operations on a collection of objects is valid if, for each object, the subsequence of operations on that object is valid.

The technical results of this paper concern three memory consistency models, called the partition consistency model, the partial-order broadcast model, and the network model. We use these terms to describe the abstract machine that delivers the consistency guarantees, but when we need to emphasize that these models are actually predicates on computations, or when we need to denote them within other notation, we use the abbreviated predicate forms, PC, POB, and NW respectively.

\textbf{The partition consistency model} defines a class of abstract memory consistency models that is designed to capture processes that communicate by reading and writing shared variables. It requires each process to

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\(^1\)Since \( p \) could be multithreaded, \( (O_C|p, \text{wrets}) \) is not necessarily a total order.
“see” its own operations in addition to all other processes’ writes in a valid total order. This order must extend program order. In addition, the views of all processes may be required to agree on the ordering of some specified subsets of operations. More formally, let $K = \{V_1, \ldots, V_m\}$ be a partition of a subset of the set $V$ of shared variables.

**Definition 3.1.** \(PC(K) \equiv \exists \langle \text{valid total order } (O_C | p \cup O_C | \text{wrt}_{\text{wts}}, \frac{\text{L}_p}{\text{L}_q}) : p \in P \rangle \) satisfying $(\forall p \in P : \text{Extends}[O_C | p \cup O_C | \text{wrt}, \frac{\text{L}_p}{\text{L}_q}, \frac{\text{pro}_{\text{wts}}}{\text{pro}_{\text{wts}}}], (\forall p, q \in P, i \in [1, m] : \text{Agree}[O_C | \text{wrt}(V_i), \frac{\text{L}_p}{\text{L}_q}, \frac{\text{L}_q}{\text{L}_q}))].$

Different instantiations of $K$ yield different memory consistency models including several well-known models. For example, Sequential Consistency requires that all processes agree on a single valid total order that extends program order. Thus, SC is $PC(\{V\})$. In the pipelined random-access model every process “sees” all the writes of each other process in program order, but different processes can interleave these sequences differently, so there is no additional agreement beyond program order on the write operations. Thus, P-RAM is $PC(\emptyset$). Goodman’s Processor Consistency requires that, in addition to P-RAM, for each shared variable, processes agree on the order of all operations to that variable. Thus PC-G is $PC(\{\{v \} \mid v \in V\}$.

A variable is a single-writer variable if it can be written by only one process, otherwise it is a multi-writer variable. The multi-writer variable subset of $V$ is denoted $V_{\text{multi-wrtrs}}$. If $\{x\} \in K$ and $x$ is a single-writer variable, then the Agree property for the set $\{x\}$ holds automatically because write operations on $x$ are totally ordered by program order, and program order is preserved by the Extends property. Thus $\{x\}$ can be removed from $K$ while maintaining $PC(K)$. Because implementations spend resources to maintain the consistency of each set in $K$, removing $\{x\}$ from $K$ could reduce partition maintenance overhead in an implementation. This motivates two new natural instantiations of partition consistency,

- **WeakPC-G** $\equiv PC(G)$ where the partition $G$ is given by $G = \{\{v\} \mid v \in V_{\text{multi-wrtrs}}\}$, and
- **WeakSC** $\equiv PC(\{V_{\text{multi-wrtrs}}\}).$

By the previous observation, WeakPC-G is equivalent to PC-G; however WeakSC is strictly weaker than SC though still stronger than PC-G. Our preliminary investigation suggests that, for many programs, WeakSC is equivalent to SC. Yet, in our implementation, it can be substantially more efficient than SC.

The message-passing network model captures a concrete reliable, message-passing asynchronous network of multi-threaded processes. Each process has a set of locally shared variables, which threads within that process use to communicate with each other. The accesses to locally shared variables are sequentially consistent$^2$. Threads of distinct processes communicate by sending and receiving messages, where messages from a sender to a receiver are received in the order sent.

This intuition of a network is formalized as follows. The shared objects are variables (shared between threads of the same process) and messages (shared between different processes). Messages have distinct identifiers, and support the operations $\text{send}(s, d, m)$ and the receive $\text{recv}^{\text{recv}}(s, d, m)$, where $s, d, m$ are the source, destination, and message contents respectively. A sequence of message operations is valid if it contains at most one send and at most one recv of any message. We assume that for each local variable of a process, each write to that variable is distinct. (If this is not the case, the process can add sequence numbers to make them so.) Define the following relations on the set $O_C$ of operations of a computation $C$:

**Message causality:** (a message is received after it is sent)

\[
\text{x \rightarrow y} \equiv \text{MessageOrder}_{\text{recv}} \quad \iff \quad x, y \in O_C \land x = \text{send}(s, d, m) \land y = \text{recv}^{\text{recv}}(s, d, m)
\]

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$^2$Weakening this assumption of “local sequential consistency” is possible. It only requires some additional thread synchronization. Since this would add complication local to each process without otherwise changing the results of this paper, we do not include this option in the rest of this paper.
FIFO channel causality: (two messages sent in program order to the same receiver are received in that order)

\[ x \xrightarrow{\text{FifoChannel}_C} y \overset{\text{def}}{=} x, y \in O_C \land x = \text{RECV}(s, d, m) \land y = \text{RECV}(s, d, m') \land \text{SEND}(s, d, m) \overset{\text{prog}}{\rightarrow} \text{SEND}(s, d, m') \]

Writes-into causality for variables: (a value read from a variable must have been previously written to it)

\[ x \xrightarrow{\text{WritesInto}_C} y \overset{\text{def}}{=} x, y \in O_C \land x = \text{WRITE}(w, z) \land y = \text{READ}(w) \]

Happens-before: (operations happen in an order that observes the message, FIFO channel, and writes-into causalities)

\[ \overset{\text{HappensBefore}_C}{\text{HappensBefore}_C} \overset{\text{def}}{=} \left( \overset{\text{prog}}{\rightarrow} \right) \cup \overset{\text{MessageOrder}_C}{\rightarrow} \cup \overset{\text{FifoChannel}_C}{\rightarrow} \cup \overset{\text{WritesInto}_C}{\rightarrow} \]

The definition \( \overset{\text{HappensBefore}_C}{\text{HappensBefore}_C} \) is inspired by Lamport’s happens-before [42], but that definition considers sequential processes that communicate only by message passing. This definition adds shared memory communication between threads and is designed to incorporate weak consistency.

**Definition 3.2.** \( \text{NW}[C] \overset{\text{def}}{=} \exists \{ \text{valid total order } (O_C[p], \overset{\text{Lp}}{\rightarrow}) : p \in P \} \) satisfying \((\forall p \in P : \text{Extends}(O_C[p], \overset{\text{Lp}}{\rightarrow}, \overset{\text{HappensBefore}_C}{\rightarrow}) \land (\text{RECV}(s, d, m) \in O_C \text{ if and only if } \text{SEND}(s, d, m) \in O_C). \)

This definition captures what we would expect of a reliable message-passing network that has FIFO channels between each pair of processors. It requires that each process’s view of its own operations is consistent with \( \overset{\text{HappensBefore}_C}{\text{HappensBefore}_C} \) order. Thus, if two operations by threads of process \( p \) are causally ordered, and even if the intermediate operations that cause that ordering are not visible to \( p \), there must be a valid view of all \( p \)’s operations that does not conflict with that causal ordering. (Without this property, the model could, for example, allow a computation where process \( p \) receives \( m1 \) from \( q \), then does some local computation, then sends \( m2 \) to \( q \), and process \( q \) receives \( m2 \) from \( p \), then does some local computation, then sends \( m1 \) to \( p \). Since such a computation could not occur on a network, it should fail to satisfy the NW memory consistency predicate.) The last conjunct ensures that the received messages are exactly those that are sent.

Any instance of the partition consistency could be constructed directly on the message-passing network model. We obtain cleaner proofs and better abstraction, however, by introducing an intermediate level that isolates the fact that processes broadcast write updates and apply them locally without the details of how broadcasting is managed.

The partial-order broadcast model is designed to capture a collection of multithreaded processes, where threads within each process communicate through shared variables, and updates are communicated between distinct processes using a one-to-all \( \text{BCAST} \) and a corresponding \( \text{DELIVER} \). Every process delivers updates in an order that extends the program order of the corresponding broadcasts. Furthermore, updates can be labeled. Processes agree on the delivery order of all updates with the same label; such agreement is not required for differently labeled updates.

The formal definition of this model uses variables (shared between threads of the same process) and update objects (shared between different processes). Each update object is unique and supports the operation \( \text{BCAST}(u, l) \) (broadcast update \( u \) with label \( l \) to all) and the operation \( \overset{\text{DELIVER}}{\rightarrow}_{u,l} \) (deliver the update \( u \)). For unlabeled updates, the label has the null value, denoted \( \perp \). The delivery order of unlabeled updates is not constrained beyond program order. A sequence of \( \text{BCAST} \) and \( \text{DELIVER} \) operations is valid if 1) no \( \text{DELIVER} \) precedes its corresponding \( \text{BCAST} \) (This restriction does not require the corresponding \( \text{BCAST} \) to be in the valid order), and, 2) no specific \( \text{DELIVER} \) occurs more than once. Define the deliver relation (a partial order) on the set \( O_C \) of operations of a computation \( C \) of the partial-order broadcast model by:

\[ x \overset{\text{delOrder}_C}{\rightarrow} y \overset{\text{def}}{=} x, y \in O_C \land x = \overset{\text{DELIVER}}{\rightarrow}_{u_1,l_1} \land y = \overset{\text{DELIVER}}{\rightarrow}_{u_2,l_2} \land \text{BCAST}(u_1, l_1) \overset{\text{prog}}{\rightarrow} \text{BCAST}(u_2, l_2). \]

Let \( O_C[\text{delivers}(l)] \) denote the set of all \( \text{DELIVER} \) operations returning an update with label \( l \neq \perp \).
Definition 3.3. \( \text{POB}(L)[C] \triangleq \exists \langle \text{valid total order } (O_C | p, \overset{L_p}{\longrightarrow}) : p \in P \rangle \) satisfying
\( (\forall p \in P : \text{Extends}(O_C | p, \overset{\text{prog}}{\longrightarrow}, \cup \overset{\text{delOrder}}{\longrightarrow})) \) and \( (\forall p, q \in P, l \in L : \text{Agree}(O_C | \text{delivers}(l), \overset{L_p}{\longrightarrow}, \overset{L_q}{\longrightarrow})) \) and
\( \forall p(\text{BCAST}(m, l) \in O_C \text{ if and only if } \text{DELIVER}(m, l) \in O_C | p) \).

This definition captures what we described as the intermediate partial-order broadcast model. It requires that each process’s view of its own operations is a valid sequence that extends the program order of its own threads and delivers message according to the program order of the corresponding broadcasts. It also requires agreement between process’s views of delivers of updates with the same label. The last conjunct ensures that every process delivers exactly the updates that were broadcast.

4 Setup for Transformations and Proofs

4.1 Transformations setup

We implement any partition consistency model \( S \) on a network model \( N \) indirectly. We first implement \( S \) on a partial-order broadcast model \( T \) and then implement \( T \) on \( N \). For each of these two steps we provide two different implementations, and prove each one is correct. All four of the resulting proofs have similar structure and notation, which is described in this section.

All our implementations transform code for a specified model to code for a target model. For clarity, SMALL CAPS font is used to denote specification level operations; Teletype is used to denote target level operations. To emphasize that a component belongs to the target level its name is sometimes annotated with a “hat” as in \( \hat{\text{name}} \).

4.2 Proofs setup and structure

Our transformations convert some specified multiprogram into a target multiprogram. To prove correctness, we must show the possible computations of these two multiprograms that can arise from their respective memory consistency models, have the same “outcome”. We make this precise as follows. Let \( \tau(P) \) denote a transformation of multiprogram \( P \). The possible computations of multiprogram \( P \) (respectively, \( \tau(P) \)) on the specified (respectively, target) memory consistent model \( MC \) (respectively, \( \hat{MC} \)) is the set \( C(P, MC) \) (respectively, \( \hat{C}(\tau(P), \hat{MC}) \)). But \( \tau(P) \) transforms specified operation invocations that require a response into subroutines that return a response. So these returned responses can be used to interpret each computation in \( C(\tau(P), \hat{MC}) \) as a computation of \( P \). We need to show that each such interpreted computation could have arisen in the specified model. That is, we must show that the interpretation of any computation in \( C(\tau(P), \hat{MC}) \) is in \( C(P, MC) \). If this is satisfied for any \( P \), we say that \( \tau(\cdot) \) correctly implements \( MC \) on \( \hat{MC} \). Figure 1 depicts this proof obligation.

\[
\begin{align*}
P \quad \text{generates} \quad & \Rightarrow \hat{C}(\tau(P), \hat{MC}) \quad \text{interpret} \quad \Rightarrow \quad I \quad \text{show} \quad \supseteq \quad \text{I} \\
\tau(\tau(P)) \quad \text{generates} \quad & \Rightarrow \hat{C}(\tau(P), \hat{MC})
\end{align*}
\]

Figure 1: Proof obligation for establishing correctness of transformations.

Each of our memory consistency models in Section 3 is defined by requiring that for every computation there is a collection of sequences of its operations such that

- each sequence is valid,
• each sequence extends some partial orders, and
• the set of sequences together satisfy some agreement constraints.

So we show that a computation $C$ satisfies a memory consistency model $MC$ by constructing such a collection of sequences that jointly satisfy the $MC$’s constraints. Any such collection is said to witness that $C$ satisfies $MC$, and is informally referred to as a collection of witness sequences. More formally, we use the predicate $\text{Witnesses}[A, C, MC]$ to assert that the collection of sequences $A$ witnesses that $C$ satisfies $MC$.

Let $P$ be a specified program and $\tau(P)$ be a transformation of that program. All our proofs have the following structure:

Assume: $\hat{C} \in C(\tau(P), \hat{MC})$. Let $C \in C(P)$ be the interpretation of $\hat{C}$.

Build: Choose any collection of sequences $\hat{A}$ such that $\text{Witnesses}[\hat{A}, \hat{C}, \hat{MC}]$. Use $\hat{A}$ to construct a corresponding collection of sequences $A$ for the operations in $C$.

Verify: Show that $\text{Witnesses}[A, C, MC]$.

In this paper, we consider only finite computations of the specified system that are completed in the target system. For long-lived computations, we would need to consider computations that arise when a multiprogram is part way through its execution and extensions of such computations as the multiprogram continues to execute. Furthermore, the transformed multiprogram could be in a state where some processes are part way through executing the transformation of their current operation invocation. Such an operation invocation is incomplete. For example, a process could have sent some but not all messages required in the transformation of its current operation invocation, and messages sent by a process could be received by some recipients but not by others. The problem of incomplete operations is taken care of by generalizing the technique used to show that a computation is linearizable as introduced by Herlihy and Wing [27]. That is, in the Assume step, we are allowed to adjust the computation $\hat{C}$ so that every operation in the adjusted computation is complete before proceeding with the Build step that extracts the sequences $\hat{A}$, and uses them to construct the witness sequences $A$. This is done as follows. For every incomplete operation in $\hat{C}$, either all its steps are erased or remaining steps are added so that it is complete. Such adding or erasing of steps could also change the operations of other processes since they may be receiving and acting on messages sent by operations that were incomplete. So the steps of these operations are also either erased or completed. To take care of the problem that the multiprogram is long-lived, we must also show that the witness sequences constructed for a computation, say $C$, of the system are not messed up by the witness sequences that are constructed for an extension of that computation, say $C'$, as the system continues to execute. This is done by showing that the collection $A$ of sequences that are constructed to establish $\text{Witnesses}[A, C, MC]$, are each prefixes of the corresponding collection $A'$ of sequences that are constructed to establish $\text{Witnesses}[A', C', MC]$. For the proofs in this paper, these two tasks are straightforward, but add considerable notational overhead. We leave it to the reader to observe that the results hold for long-lived computations but consider only finite computations with only completed transformations in this paper.

Proof diagrams

When designing and debugging our proofs, we frequently used diagrams to record partial orders and various relationships between them. Because these diagrams could be formalized and used to help make our proofs more precise and concise, we adopt this diagrammatic notation here. The notation use in these diagrams is as follows. Let $a, b, c$ and $d$ be operations; and $A$ and $B$ be set of operations. Edges in a diagram represent boolean expressions and a diagram is interpreted as the conjunction of these expressions. The basic building blocks are:
Multiple edges are disjunctive; eg. $a \xRightarrow{E} b$ asserts $(a \xRightarrow{D} b$ or $a \xRightarrow{E} b$). The position of an arrow and its label are not significant; eg. $a \xRightarrow{L} b$ and $b \xRightarrow{L} a$ are equivalent. Notice that for sets $A$ and $B$, the notation is similar to Lamport’s system executions [44].

5 Implementing Partition Consistency on the Partial-Order Broadcast Model

Partition consistency models processes that interact by reading and writing globally shared variables that have only weak consistency guarantees. Recall that an instance of partition consistency has a partition $K$ of some of the variables and requires strong agreement within but not between sets of $K$. Our task is to transform each specified process $p$ of such a system into a target process $\hat{p}$ for the partial-order broadcast model, where inter-process communication is via the partial order broadcast primitive. Our implementation is a generalization of the way that totally ordered broadcast is used to implement sequential consistency [9]. The predicate $\text{PC}(K)$ for partition consistency ensures agreement on the ordering of writes to all variables within the same class of the partition $K$; the consistency predicate $\text{POB}(L(K))$ satisfied by the partial-order broadcast model is used to implement this agreement by enforcing agreement on the deliveries of updates with the same label.

We achieve our implementation by:

- creating a label for each class in partition $K$; that is, $L(K) = \{i : V_i \in K\}$;
- mapping each $p$ to a thread $\hat{p}.m$ in the partial-order broadcast model; and
- augmenting each $\hat{p}.m$ with a companion delivery thread $\hat{p}.d$.

There are two variants of the transformation. The pseudo-code for the slow-write/fast-read variant (SWFR) is shown in Figure 2.

The main thread, $\hat{p}.m$, is derived from $p$ by replacing each $\text{READ}$ and each $\text{WRITE}$ to a shared variable with a subroutine call. The transformation of a $\text{READ}$ simply returns the value stored in $\hat{p}$’s local memory. The transformation of a $\text{WRITE}$ creates a $\text{bcast}$ operation to be delivered to each target process. It has a label corresponding to the partition class of the variable being written, if it exists. The delivery thread, $\hat{p}.d$, manages the delivery operations and maintains synchronization with $\hat{p}.m$ via locally shared variables. It repeatedly applies updates to the local memory it shares with $\hat{p}.m$. The procedure $\text{WaitWritesComplete}$ causes $\hat{p}.m$ to wait until $\hat{p}.d$ has applied all the writes previously broadcast by $\hat{p}.m$.

Under the $\text{SWFR}_\text{PC}(K)_{\text{POB}(L(K))}$ transformation, each process has at most one outstanding local write, since every write must be applied locally before the subroutine completes. Every write contains a wait, making these writes “slow”. An alternative is to move the $\text{WaitWritesComplete}$ call from the end of the $\text{WRITE}$ to the beginning of the $\text{READ}$. This gives us a fast-write/slow-read ($\text{FWSR}_\text{PC}(K)_{\text{POB}(L(K))}$) implementation.

5.1 Correctness of the $\text{SWFR}_\text{PC}(K)_{\text{POB}(L(K))}$ and $\text{FWSR}_\text{PC}(K)_{\text{POB}(L(K))}$ implementations

The proofs of correctness of $\text{SWFR}_\text{PC}(K)_{\text{POB}(L(K))}$ and $\text{FWSR}_\text{PC}(K)_{\text{POB}(L(K))}$ are very similar; they differ in only one step. This step can be treated generically, so we present one proof for both implementations. Let $\text{WR}_\text{PC}(K)_{\text{POB}(L(K))}$ refer to either
1. Transformation’s local target variables

| Memory[\tilde{p}].x | \forall x \in V, local replica variable, initial value is the initial value of x |
|---------------------|------------------------------------------------------------------|
| writes-processed    | local variable, counts messages broadcast by \( p \) that are also delivered by \( p \), initially 0 |
| writes-requested    | local variable, counts locally broadcast messages, initially 0 |

2. Transforming specification processes

Transformation of process \( p \) to thread \( \tilde{p}.m \):

```plaintext
SWFR_{\text{POB}(L(K))}^{\text{PC}(K)}(\text{READ}_p(x)) \quad SWFR_{\text{POB}(L(K))}^{\text{PC}(K)}(\text{WRITE}_p(x,v)) \quad \text{WaitWritesComplete()}
```

1. \text{return} Memory[\tilde{p}].x
2. \text{writes-requested} \leftarrow \text{writes-requested} + 1
3. \text{if} \exists V_i \in K: x \in V_i
4. \text{then bcast}([x,v,\tilde{p}],i) \text{ else bcast}([x,v,\tilde{p}],\bot)
5. \text{WaitWritesComplete()}
6. \text{while} \text{writes-processed} < \text{writes-requested}
7. \text{do skip}

3. New target threads

\( \forall p \in P \), new thread \( \tilde{p}.d \).

\( \tilde{d} : \)

9. \text{while} TRUE
10. \text{do} \text{ApplyWrite()}
11. \text{update,} l \leftarrow \text{deliver()}
12. \{ \text{update has form } [x,v,\text{source}] \}
13. \text{let} [x,v,\text{source}] = \text{update}
14. \text{Memory}[\tilde{p}].x \leftarrow v
15. \text{if} \text{source} = p
16. \text{then} \text{writes-processed} \leftarrow \text{writes-processed} + 1

---

Figure 2: Implementation of Partition Consistency on the Partial-Order Broadcast Model

Implementation.

**Theorem 5.1.** Let \( P \) be any multiprogram where each process in \( P \) is a single-threaded program that accesses read/write variables from a set \( V \), and let \( K = \{V_1, \ldots, V_k\} \) be any partition of a subset of \( V \). Then \( \text{WR}_{\text{POB}(L(K))}^{\text{PC}(K)}(P) \) correctly implements \( \text{PC}(K) \) on \( \text{POB}(L(K)) \), for all such \( P \).

**Proof.**

Assume: Let \( \tilde{C} \) be a computation in \( C(\text{WR}_{\text{POB}(L(K))}^{\text{PC}(K)}(P), \text{POB}(L(K))) \) and let \( C \) be the interpretation of \( \tilde{C} \). Let \( \hat{O} \) denote the set of operations \( O_C \). To show \( \text{PC}(K)[C] \) we construct witness sequences that satisfy the requirements of Definition 3.1.

Build: Choose a collection of witness sequences \( \langle (\hat{O}[\tilde{p}, \xrightarrow{\text{wrts}} \tilde{L}_\hat{p}]) : \tilde{p} \in \text{WR}_{\text{POB}(L(K))}^{\text{PC}(K)}(P) \rangle \). That is, Witnesses\(\{\tilde{L}_\hat{p} : \forall \tilde{p} \in \hat{P}, \tilde{C}, \text{POB}(L(K))\}\).

Construct a corresponding set of sequences \( \langle (O_C|p \cup O_C|\text{wrts}, \xrightarrow{\text{wrts}}) : p \in P \rangle \) as follows:
1. For each read or write operation \( o \) on a “local replica” variable we associate it with a specification level operation as follows:

(a) The transformation sets up a one-to-one correspondence between the set of read operations of the POB(\( L(K) \)) system, and the read operations of the PC(\( K \)) system. Specifically, \( \text{read}(\text{Memory}[p],x) \) in the implementation must have come from the transformation of a unique corresponding specification level \( \text{READ}(x) \in O_C[p] \).

(b) The transformation sets up, for each \( \hat{p} \), a one-to-one correspondence between the set of write operations in \( \hat{O}|\hat{p} \) of the POB(\( L(K) \)) system, and the write operations of the PC(\( K \)) system. More precisely, every \( \text{write}(\text{Memory}[p],x,v) \) must have a \( o_d = \text{DELIVER}(\hat{p},x,v) \) in the same ApplyWrite() call. This deliver operation \( o_d \) must have a corresponding \( \text{BCAST}(m) \), which can only have occurred in the transformation of some unique corresponding specification level write \( \text{WR}^{\text{PC}(K)}_{\text{POB}(L(K))}(\text{write}(x,v)) \).

2. For each sequence \( \hat{L}_p \), build the sequence \( \text{Short}(\hat{L}_p) \) by removing all of operations that are applied to the broadcast object, and the local variable \( \text{writes-processed} \) and the local variable \( \text{writes-requested} \). This leaves only the read and write operations on the “local replica” variables in local memory.

3. For each \( \hat{L}_p \), build a sequence \( L_p \) by replacing each read (respectively, write) operation in \( \text{Short}(\hat{L}_p) \) with the associated specification level read (respectively, write) operation defined in step 1.

4. Notice that each sequence \( L_p \) contains exactly the operations in \( O_C[p \cup O_C]|\text{wrt} \). These sequences induce the corresponding total orders \( \langle (O_C[p \cup O_C]|\text{wrt}, L_p) : p \in P \rangle \).

**Verify:** We need to prove that \( \text{Witnesses}[[\{L_p : \forall p \in P\}, C, \text{PC}(K)] \) holds for the orders \( \langle (O_C[p \cup O_C]|\text{wrt}, L_p) : p \in P \rangle \) constructed in the Build step.

First observe that removing from any valid sequence all operations related to specific objects preserves validity. Hence each \( \text{Short}(\hat{L}_p) \) is valid since \( \hat{L}_p \) is valid. Then replacing each read and write with the corresponding read and write respectively also clearly preserves validity. We conclude that the total orders \( (O_C[p \cup O_C]|\text{wrt}, L_p) \) are valid. The following two lemmas establish the remainder of the proof:

| Constraint | Lemma |
|------------|-------|
| \( \forall p, q \in P, i \in [1,k] : \text{Agree}(O_C[wrt](V_i), L_p, L_q) \) | Lemma 5.3 |

Therefore, \( \text{PC}(K)[C] \) as required.

**Lemma 5.2.** \( \forall p \in P : \text{Extends}[[O|p \cup O]|\text{wrt}, L_p, \text{prog}_C] \).

**Proof:** Let \( o_1 \xrightarrow{\text{prog}} o_2 \) where \( o_1, o_2 \in O|p \cup O\). PC(\( K \)) only has read/write variable objects, so there are four cases for \( o_1, o_2 \). Notice that if \( o_1 \) or \( o_2 \) is a \( \text{READ} \) then \( o_1, o_2 \in O|p \).

**Case 1: read, read**

Let \( o_1 = \frac{\text{READ}(x)}{u} \) and \( o_2 = \frac{\text{READ}(y)}{u} \).

\[
\text{WR}^{\text{PC}(K)}_{\text{POB}(L(K))}(\text{READ}(x)) \xrightarrow{\text{prog}_p} \text{WR}^{\text{PC}(K)}_{\text{POB}(L(K))}(\text{READ}(y)) \Rightarrow \frac{\text{read}(x)}{u} \xrightarrow{\text{prog}_p} \frac{\text{read}(y)}{u} \Rightarrow \frac{\text{READ}(x)}{u} \xrightarrow{\text{prog}_p} \frac{\text{READ}(y)}{u} \Rightarrow o_1 \xrightarrow{L_p} o_2.
\]

**Case 2: read, write**

Let \( o_1 = \frac{\text{READ}(x)}{u} \) and \( o_2 = \text{WRITE}(y,w) \). We have:
1. By definition of validity of update objects (since `bcast` and `deliver` are both in $O|p$).

**Case 3: write, write**

Let $o_1 = \text{WRITE}(x, v)$ and $o_2 = \text{WRITE}(y, w)$. Suppose $o_1, o_2 \in O|q$. Then:

**Case 4: write, read** Let $o_1 = \text{WRITE}(x, v)$ and $o_2 = \frac{\text{READ}(y)}{w}$. Then:
1. By validity of \( \tilde{L}_p \).

2. Both fast-write and slow-write transformations call \text{WaitWritesComplete} between any write and subsequent read by the same process.

3. \( c_2 \geq c_1 \) and \text{writes}-\text{processed} is increased every time it is set. If a value greater than \( c_1 \) is read from \text{writes}-\text{processed}, it must have been written after \text{write}(\text{writes}-\text{processed}, c_1).

Thus in all cases we have \( o_1 \xrightarrow{L_p} L_q \rightarrow o_2 \). Therefore \( L_p \rightarrow \xrightarrow{\text{prog}} \).

Case 4 exemplifies how the proofs for both \( \text{SWFR}_{\text{POB}}^{PC} \) and \( \text{FWSR}_{\text{POB}}^{PC} \) are unified. The only property needed is that there is a \text{WaitWritesComplete} between the \text{bcast} and the \( \text{READ}() \). Both \( \text{SWFR}_{\text{POB}}^{PC} \) and \( \text{FWSR}_{\text{POB}}^{PC} \) satisfy this property and so one proof suffices for the correctness of both implementations.

**Lemma 5.3.** \( \forall p, q \in P, i \in [1, k] : \text{Agree}[O|\text{wrt}(V_i), \xrightarrow{L_p, L_q}] \).  

**Proof.** Let \( \text{write}_1, \text{write}_2 \in O|\text{wrt}(V_i) \) for some \( i \). Then the transformation \( \text{WR}_{\text{POB}(L(K))}^{PC}(\text{write}_i) \) \( (i \in \{1, 2\}) \) of each of these contains a corresponding broadcast \( \text{bcast}(\text{msg}_i, l) \) where the label \( l \) is the same for each. For every process \( p \), \( \tilde{L}_p \) contains a \text{deliver} followed by a \text{write} corresponding to each of these \text{bcast}'s. Let \( w_{1p}, w_{1q}, w_{2p}, w_{2q} \) be these corresponding writes in \( O_C \) for two processes \( p \) and \( q \) and suppose wlog that \( w_{1p} \xrightarrow{\text{msg}_u_1} w_{2p} \). Then \( \xrightarrow{\text{deliver()}L_p} w_{1q}, w_{2q} \) which implies \( \xrightarrow{\text{deliver()}L_q} w_{1q}, w_{2q} \) because POB(L(K)) requires that deliveries of messages with the same label must agree. Hence, \text{write}_1 \xrightarrow{L_p} \text{write}_2 \) and \text{write}_1 \xrightarrow{L_q} \text{write}_2 \) by the construction of \( L_p \) and \( L_q \) from \( \tilde{L}_p \) and \( \tilde{L}_q \) respectively. \[ \Box \]
6 Implementing The Partial-Order Broadcast Model on the Message-Passing Network Model Using Tokens

The partial-order broadcast model is very similar to the message-passing network model. The read and write operations are on local variables in both models, so they are mapped by the transformation with the identity function. That is, \( \text{read}(x) \) (respectively, \( \text{write}(x,v) \)) is mapped to \( \text{read}(x) \) (respectively, \( \text{write}(x,v) \)). We need only specify how to implement \( \text{bcast} \) and \( \text{deliver} \) by sending and receiving messages. The processes in \( P \) are numbered starting at 0, and organized into a virtual ring such that \( \text{next}(p) = (p + 1) \mod |P| \). A token is created for each label \( l \in L \), and for each token, a thread is created on each process to manage it.

The broadcast of a labeled update requires that all processes agree on the delivery order of all updates with the same label. To ensure this, the transformation of a \( \text{bcast} \) of a labeled update has the process acquire the appropriate token for that label by synchronizing with its token thread, \( \text{send} \) a message containing the update information to each process, and wait for acknowledgments from all the processes before completing. Since unlabeled updates only require that program order is maintained, unlabeled messages are sent (with \( \text{send} \)) to every other process without acquiring a token.

To avoid deadlock this transformation requires that \( \text{bcasts} \) and \( \text{delivers} \) are invoked by separate threads. Each call to \( \text{PassToken} \) manages one acquisition and subsequent release of a token. It returns only after handshaking with \( \text{ProtectedBcast} \) to determine that the token is no longer needed and can be released. \((\text{pattern}) \mapsto \text{recv()}\) is pseudo-code that blocks until a message matching \( \text{pattern} \) is received and stored in the appropriate pattern variables.

6.1 Correctness of \( \text{TKN}^{\text{POB}(L)}_{\text{NW}} \) transformation

Theorem 6.1. Let \( P \) be a multiprogram that uses \( \text{reads}, \text{writes}, \text{bcasts}, \) and \( \text{delivers} \) where each process has two threads; one that calls \( \text{deliver} \) but not \( \text{bcast} \) and one that calls \( \text{bcast} \) but not \( \text{deliver} \). Then \( \text{TKN}^{\text{POB}(L)}_{\text{NW}}(P) \) correctly implements \( \text{POB}(L) \) on \( \text{NW} \), for any label set \( L \) and any such \( P \).

Proof.

Assume: Let \( \hat{C} \) be a computation in \( C \left( \text{TKN}^{\text{POB}(L)}_{\text{NW}}(P), \text{NW} \right) \) and let \( C \) be the interpretation of \( \hat{C} \). Let \( \hat{O} \) denote the set of operations \( O_{\hat{C}} \). To show \( \text{POB}(L)[C] \) we construct witness sequences that satisfy the requirements of Definition 3.3.

Build: Choose some collection of witness sequences \( \{ (\hat{O}[\hat{p}], \frac{L_{\hat{p}}}{\hat{p}}) : \hat{p} \in \text{TKN}^{\text{POB}(L)}_{\text{NW}}(P) \} \). That is, Witnesses\(\{L_{\hat{p}} : \forall \hat{p} \in \text{TKN}^{\text{POB}(L)}_{\text{NW}}(P) \}, \hat{C}, \text{NW} \). Recall that \( L_{\hat{p}} \) denotes the sequence induced by the total order \( L_{\hat{p}} \). We now construct \( \{ (O[C[p], \frac{L_{p}}{p}) : p \in P \} \) from \( \{ (O[\hat{p}], \frac{L_{\hat{p}}}{\hat{p}}) : \hat{p} \in \text{TKN}^{\text{POB}(L)}_{\text{NW}}(P) \} \) as follows. For each \( \hat{p} \), first create the sequence \( \text{Short}(L_{\hat{p}}) \) from \( L_{\hat{p}} \) by removing:

- all operations on the handshake variables needToken\([l] \) and doorOpen\([l] \) for all \( l \in L \).
- all send operations except the first send of a bcast\(() \) that is in \( L_{\hat{p}} \).
- all recv operations except the recv of a deliver.

Observe that each operation remaining in \( \text{Short}(L_{\hat{p}}) \) is a target level operation that was produced from the transformation of some specification level operation, rather than by a thread created by the transformation.
TKN_{NW}^{POB(L)} Implementation;
Code for each process \( p \in P \).

1. Transformation’s local target variables

- \( needToken[l] \) for each \( l \in L \); handshake boolean variable, initially \( TRUE \)
- \( doorOpen[l] \) for each \( l \in L \); handshake boolean variable, initially \( TRUE \)

\( \bar{x} \) \quad \forall x \in V \), replica of local variable, initial value is the initial value of \( x \).

2. Transforming specification threads

Transformation of thread \( p.m \) to \( \hat{p}.m \) and \( p.d \) to \( \hat{p}.d \):

- \( \text{TKN}_{NW}^{POB(L)}(\text{BCAST}(u, l)) \)
  - if \( l \neq \bot \)
  - then \( \text{ProtectedBcast}(u, l) \)
  - else \( \text{bcastop}(u, l) \)
- \( \text{bcastop}(u, l) \)
  - while \( \neg doorOpen[l] \) skip
  - \( \text{bcastop}(u, l) \)
  - \( \text{doorOpen}[l] \) \( \leftarrow \) FALSE
  - \( \text{needToken}[l] \) \( \leftarrow \) FALSE

3. New target threads

One new token thread \( \hat{p} \). TokenThread\(_l \), \( \forall l \in L \):

- \( \text{PassToken}_{\hat{p}}(l) \)
  - if \( \hat{p} = 0 \)
  - then \( \text{send}(\hat{p}, \text{next}(\hat{p}), [\text{TOKEN, BCASTGROUPTOKEN}]) \)
  - loop
  - \( \text{do PassToken}_{\hat{p}}(l) \)

\( \text{PassToken}_{\hat{p}}(l) \)
- if \( \text{needToken}[l] \)
- then \( \text{doorOpen}[l] \) \( \leftarrow \) TRUE
- while \( \text{needToken}[l] \) skip
- \( \text{send}(p, \text{next}(p), [\text{TOKEN, BCASTGROUPTOKEN}]) \)

Figure 3: Token implementation of Partial-Order Broadcast on the Message-Passing Network Model

Now convert each \( \text{Short}(\hat{L}_p) \) to a new sequence \( L_p \) of specification level operations by replacing each target level operations with the specification level operations that produced it. More precisely:
Verify: The read and write operations in \( \hat{L}_p \) are valid. Thus the subset that remains in Short(\( \hat{L}_p \)) remains valid because it consists of exactly the subset of these operations that are applied to local variables, and projecting a valid sequence onto all the operations applied to a subset of objects preserves validity. Each read (respectively, write) in Short(\( \hat{L}_p \)) is replaced with the corresponding read (respectively, write) in the construction of \( L_p \), so for each \( p \), all read and write operations are valid. To see that the bcast and deliver operations are also valid we must confirm that for each \( L_p \), 1) no deliver precedes its corresponding \( \text{bcast} \) and, 2) no specific deliver occurs more than once. Sequence \( \hat{L}_p \) (and thus Short(\( \hat{L}_p \))) is valid, so no recv precedes its corresponding send and no message is received more than once, ensuring properties 1 and 2 after mapping from Short(\( \hat{L}_p \)) to \( L_p \).

The following table shows the properties we prove to verify the constraints of Definition 3.3:

| Constraint | Lemma |
|------------|-------|
| \( \forall p \in P : (O_C|p, L_p \rightharpoonup) \) is a valid total order | By construction of \( L_p \) as proved above |
| \( \forall p \in P : \text{Extends}[O_C|p, L_p \rightharpoonup_{\text{prog}_p}] \) | Lemma 6.2 |
| \( \forall p \in P : \text{Extends}[O_C|p, L_p \rightharpoonup_{\text{delOrder}_C}] \) | Lemma 6.3 |
| \( \forall p, q \in P, l \in L : \text{Agree}[O_C|\text{delivers}(l), L_p \rightharpoonup, L_q \rightharpoonup] \) | Lemma 6.6 |
| \( \forall p \in P : (\text{bcast}(m, l) \in O_C \text{ if and only if } \text{DELIVER}(l)_{m,l} \in O_C|p) \) | by construction of \( L_p \) and the network model. |

**Lemma 6.2.** \( \forall p \in P : \text{Extends}[O_C|p, L_p \rightharpoonup_{\text{prog}_p}] \)

**Proof.** Let \( o_1, o_2 \in O_C|p \) such that \( o_1 \rightharpoonup_{\text{prog}_p} o_2 \). Let \( \text{TS}_{\text{NW}}^{\text{POB}(L)}(o) \circ 1 \) denote the operation in the transformation of \( o \) to the transformation of \( o \) when Short(\( \hat{L}_p \)) is converted to \( L_p \).

\[
\begin{array}{c}
\text{TKN}_{\text{NW}}^{\text{POB}(L)}(o_1) \rightharpoonup_{\text{prog}} \text{TKN}_{\text{NW}}^{\text{POB}(L)}(o_2) \\
\text{TKN}_{\text{NW}}^{\text{POB}(L)}(o_1) \circ \text{TKN}_{\text{NW}}^{\text{POB}(L)}(o_2) \\
\end{array}
\]

1. \( \text{Extends}[O_C|\hat{p}_1, L_p \rightharpoonup_{\text{prog}}] \)

**Lemma 6.3.** \( \forall p \in P : \text{Extends}[O_C|p, L_p \rightharpoonup_{\text{delOrder}_C}] \)

19
Proof. Let \( o_1, o_2 \in O \setminus P \) such that \( o_1 \xrightarrow{\text{DelOrder}} o_2 \). Then \( o_1 = \frac{\text{Deliver}(\cdot)}{u_1,l_1} \), \( o_2 = \frac{\text{Deliver}(\cdot)}{u_2,l_2} \) and \( \text{BCAST}(u_1,l_1) \xrightarrow{\text{prog}} \text{BCAST}(u_2,l_2) \) for some process \( s \in P \).

\[
\begin{align*}
\text{BCAST}(u_1,l_1) & \quad \xrightarrow{\text{prog}} \quad \text{BCAST}(u_2,l_2) \\
\text{TKN}_{\text{POB}(L)} & \quad \xrightarrow{\text{MessageOrder}} \quad \text{TKN}_{\text{POB}(L)} \\
\text{TKN}_{\text{NW}}(\text{BCAST}(u_1,l_1), \text{send}(\hat{s}, \hat{p}, m_1)) & \quad \xrightarrow{\text{prog}_2} \quad \text{TKN}_{\text{NW}}(\text{BCAST}(u_2,l_2), \text{send}(\hat{s}, \hat{p}, m_2)) \\
\text{TKN}_{\text{NW}}(\text{BCAST}(u_1,l_1), \text{recv}(\hat{s}, \hat{p}, m_1)) & \quad \xrightarrow{\text{MessageOrder}} \quad \text{TKN}_{\text{NW}}(\text{BCAST}(u_2,l_2), \text{recv}(\hat{s}, \hat{p}, m_2)) \\
\text{TKN}_{\text{NW}}(\text{BCAST}(u_1,l_1), \text{recv}(\hat{s}, \hat{p}, m_1)) & \quad \xrightarrow{\text{DELIVER}(\cdot)} \quad \text{L}_{\hat{p}} \\
\text{TKN}_{\text{NW}}(\text{BCAST}(u_2,l_2), \text{recv}(\hat{s}, \hat{p}, m_2)) & \quad \xrightarrow{\text{MessageOrder}} \quad \text{TKN}_{\text{NW}}(\text{BCAST}(u_2,l_2), \text{recv}(\hat{s}, \hat{p}, m_2)) \\
\text{DELIVER}(\cdot) & \quad \xrightarrow{u_1,l_1} \quad \text{L}_{\hat{p}} \\
\end{align*}
\]

The next two results are sublemmas that provide the pieces for our last requirement, Lemma 6.6. Informally, the first shows that the messages sent by a \text{BCAST} are all received (and acknowledged) before the \text{BCAST} completes. The second ensures that an \text{BCAST} of an update with label \( l \) by process \( p \) is implemented while \( \hat{p} \) holds the token for label \( l \). These two facts together with the circulation of the token from process to process, combine to establish that all processes receive the update messages with label \( l \) in the same order.

**Lemma 6.4.** Each \text{recv} operation that corresponds to a specification level \text{Deliver} operation is ordered by \text{HappensBefore} order between the invocation and the response of the \text{BCAST} operation that matches this \text{DELIVER}.

**Proof.** Let \( \text{recv}(\cdot) \xrightarrow{\text{prog}} \text{send}(\hat{p}, \hat{q}, [\text{ACK}]) \) correspond to some deliver \( \text{Deliver}(\cdot) \), and let \( \text{BCAST}(u, l) \) be the matching \text{BCAST}. Consider the send \( \text{send}(\hat{p}, \hat{q}, [\text{ACK}]) \) that is sent after this receive.

\[
\begin{align*}
\text{recv}(\cdot) & \quad \xrightarrow{\text{prog}} \quad \text{send}(\hat{p}, \hat{q}, [\text{ACK}]) \\
\text{send}(\hat{p}, \hat{q}, [\text{MESSAGE}, u, l]) & \quad \xrightarrow{\text{MessageOrder}} \quad \text{recv}(\cdot) \\
\text{BCAST}(u, l), \text{bcastop} & \quad \xrightarrow{\text{prog}} \quad \text{recv}(\cdot)
\end{align*}
\]

The Lemma follows because \text{HappensBefore} order extends \text{prog} and \text{MessageOrder}.

**Lemma 6.5.** For each \( l \in L \), let \( B_l = \{ \text{TKN}_{\text{NW}}(\text{BCAST}(u, l)), \text{bcastop} : \text{BCAST}(u, l) \in O_C \} \). Then \( (B_l, \text{HappensBefore}) \) is a total order.

**Proof.** Informally, for any label \( l \), the main thread \( \hat{p} \_\text{main} \) and the token thread for label \( l \), \( \hat{p} \_\text{token}_{l} \), handshake via the \( \text{needToken}[l] \) and \( \text{doorOpen}[l] \) variables. This ensures that a \text{BCAST} of an update with label \( l \) by process \( p \) is implemented while \( \hat{p} \) holds that token.

More precisely:
Lemma 6.6. \( \forall p, q \in P, l \in L : \text{Agree}[O_{C}|\text{delivers}(l), \xrightarrow{L_p}, \xrightarrow{L_q}] \).

Proof. Let \( \text{DELIVER}(u_1, l), \text{DELIVER}(u_2, l) \in O_C \) and let \( \text{BCAST}(u_1, l), \text{BCAST}(u_2, l) \) be, respectively, the \( \text{BCAST} \) operations that match these \( \text{DELIVER} \) operations. Consider the method calls \( \text{bcst}-1 = TKN_{NW}^{\text{POB}(L)}(\text{BCAST}(u_1, l)), \text{bcst} \) and \( \text{bcst}-2 = TKN_{NW}^{\text{POB}(L)}(\text{BCAST}(u_2, l)), \text{bcst} \) of the implementation of these \( \text{BCAST} \)s.

By Lemma 6.5, assume, without loss of generality, that \( \text{bcst}-1 \xrightarrow{\text{HappensBefore}} \text{bcst}-2 \).

Then for any process \( q \):
1. By Lemma 6.4. Since this holds for every process \( q \), all processes agree on the order of \( \text{DELIVER}(u_1, l) \) and \( \text{DELIVER}(u_2, l) \). □

7 Implementing The Partial-Order Broadcast Model on the Message-Passing Network Model Using Timestamps

The \( TS_{\text{POB}}(L) \) implementation (Figures 4 and 5) uses timestamps to enforce agreement on the order of deliveries of updates with the same label. It generalizes Attiya and Welch’s implementation of totally ordered broadcast [9].

READ and WRITE operations are mapped by the identity transformation to the network model. The operations \( \text{BCAST} \) and \( \text{DELIVER} \) are implemented by \( \text{send}(\text{source}, \text{destination}, \text{message}) \) and \( \text{recv}() \) operations. No new threads need to be added in this implementation.

By the definition of \( \text{POB}(L) \), the implementation must ensure that all processes agree on the deliver order of messages with the same label. This is achieved using timestamps. Each process has \(|L| \) priority queues, one for each message label. For unlabeled messages, it has one fifo-queue for each process. For priority-queues, we denote the enqueue and dequeue operations by \( \text{priority-enQ} \) and \( \text{extractmin} \) respectively. For fifo-queues, we denote the enqueue and dequeue operations by \( \text{fifo-enQ} \) and \( \text{fifo-deQ} \) respectively.

Labeled messages are handled as follows. Messages with the same label are \( \text{priority-enQ} \)ed into the same priority-queue. \( \text{extractmin} \) removes the message with the minimum (timestamp, process id) pair. To ensure that all processes \( \text{DELIVER} \) messages with the same label in the same order, the implementation guarantees that no message is dequeued by \( \text{extractmin} \) before all messages with a smaller or equal timestamp have been received and \( \text{priority-enQ} \)ed. Processes keep their timestamps up to date by adopting the largest timestamp of any received message and sending their updated timestamp to all other processes.

Unlabeled messages are handled slightly differently. They are \( \text{fifo-enQ} \)ed into the fifo-queue for the sending process, but timestamps are not used for \( \text{fifo-deQ} \)ing because agreement of delivery order is not required for unlabeled messages.

The definition of \( \text{POB}(L) \) also requires that each process delivers messages in an order that extends the program order of the corresponding \( \text{BCASTs} \). This is not automatically enforced because messages are spread across multiple priority-queues and fifo-queues. So the implementation uses counters. A message is only delivered by a process if its counter value is 1 bigger than the counter value of the last delivered message from the same source.

Observe that the \( \text{DELIVER} \) transformation does the heavy lifting in this implementation. In order to avoid race conditions and more complicated synchronization, this implementation requires that for each process, at most one thread performs \( \text{DELIVER} \). Priority-queues and fifo-queues can be constructed from just variables because each queue is accessed by only one thread.

In Figures 4 and 5, messages are designated as one of three types: LOCAL-BROADCAST-REQUEST, TS-UPDATE, ORD-MSG. Depending on type, a message can contain a timestamp, counter, sender id (denoted \( m.src \)) as well as the label and value for the requested update.
1. Transformation’s local target variables

**local-counter**
- Last broadcast counter value

**counter**\([1..|P|]\)
- Array of last received counter values, one for each process, initially all 0

\(T[1..|P|]\)
- Array of last received timestamp values, one for each process, initially all 0

**priority**\([1..|L|]\)
- Array of priority-queues for messages, one for each label \(l \in L\), initially all empty

**fifo**\([1..|P|]\)
- Array of fifo-queues for unlabelled messages, one for each process, initially all empty

\(\tilde{x}\)
- Element of the set of operations

2. Transformation specification threads

Transformation of thread \(p.m\) to \(\tilde{p}.m\) and \(p.d\) to \(\tilde{p}.d\):

\[
\begin{align*}
TS^{\text{POB}(L)}_{\text{NW}}(\text{READ}(x)) &= \text{return } \tilde{x} \\
TS^{\text{POB}(L)}_{\text{NW}}(\text{WRITE}(x,v)) &= \tilde{x} \leftarrow v \\
TS^{\text{POB}(L)}_{\text{NW}}(\text{BCAST}(\text{update},l)) &= \text{send}(\tilde{p},\tilde{p},[\text{LOCAL-BROADCAST-REQUEST}])
\end{align*}
\]

3. New target threads

No new target threads for this implementation.

---

**Figure 4:** Timestamp Implementation of Partial-Order Broadcast on the Message-Passing Network Model

### 7.1 Correctness of the \(TS^{\text{POB}}_{\text{NW}}\) implementation

**Theorem 7.1.** Let \(P\) be any multiprogram that uses \textsc{reads}, \textsc{writes}, \textsc{bcasts}, and \textsc{delivers} such that at most one thread in each process calls \textsc{deliver}. Then \(TS^{\text{POB}(L)}_{\text{NW}}(P)\) correctly implements \(\text{POB}(L)\) on \(\text{NW}\), for any label set \(L\) and any such \(P\).

**Proof.**

**Assume:** Let \(\tilde{C}\) be a computation in \(\tilde{C}(TS^{\text{POB}(L)}_{\text{NW}}(P),\text{NW})\) and let \(C\) be the interpretation of \(\tilde{C}\). Let \(\tilde{O}\) denote the set of operations \(O_{\tilde{C}}\). To show \(\text{POB}(L)[C]\), we construct witness sequences that satisfy the
CanExtract(priorityQ)
28 if priority-isempty(priorityQ)
29 then return FALSE
30 else qe ← peek-min(priorityQ)
31 return (qe.counter = counter[qe.src] + 1)
\(\land (\forall \hat{q} \in \hat{P} : qe.ts \leq T[\hat{q}])\)

CanDequeue(fifoQ)
31 if isempty(fifoQ)
32 then return FALSE
33 else qe ← peek-head(fifoQ)
34 return (qe.counter = counter[qe.src] + 1)

ProcessQueueElement(queue-element, l, \hat{source})
25 if l \neq \bot
26 then priority-enQ(priorityQ[l], queue-element)
27 else fifo-enQ(fifoQ[\hat{source}], queue-element)

FifoBroadcast(message)
12 for \(\hat{q} \in \hat{P} \setminus \{\hat{p}\}\)
13 do send(\(\hat{p}, \hat{q}, message\))

Figure 5: Auxiliary Functions for the Timestamp Implementation

requirements of Definition 3.3.

**Build:** Choose a collection of witness sequences \(\langle (\hat{O}|\hat{p}, \hat{L}_p) : \hat{p} \in TS_{NW}^{\text{POB}(L)}(P) \rangle\). That is,

Witnesses\(\{\hat{L}_p : \forall \hat{p} \in \hat{P}, \hat{C}, NW\}\). Recall that we use \(\hat{L}_p\) to denote the sequence induced by \((\hat{O}|\hat{p}, \hat{L}_p)\).

Construct the sequence \(\text{Short}(\hat{L}_p)\) from \(\hat{L}_p\) by removing:

1. all the operations on the \(T\), counter, and local-counter variables.
2. all send and recv operations except the send of a \([\text{LOCAL-BROADCAST-REQUEST}]\).
3. all operations on priority-queues and fifo-queues except extractmin and fifo-deQ operations.

The operations remaining in \(\text{Short}(\hat{L}_p)\) are reads, writes, sends, extractmins and fifo-deqs. Each such operation, \(\text{op}\), was produced from a transformation of some unique specification level operation, denoted \(\text{lift}(\text{op})\), of the main thread. Specifically:

\[
\begin{align*}
\text{lift}(\text{read}(x)) &= \text{READ}(x) \\
\text{lift}(\text{write}(x, v)) &= \text{WRITE}(x, v) \\
\text{lift}(\text{send}(s, d, \text{LOCAL-BROADCAST-REQUEST}, \text{update}, l)) &= \text{BCAST}(\text{update}, l) \\
\text{lift}(\text{extractmin}(\text{priorityQ}[l])) &= \text{DELIVER}(l) \\
\text{lift}(\text{fifo-deQ}(\text{fifoQ}[m])) &= \text{DELIVER}(l) \quad (\text{where } \bot \text{ denotes an unlabelled update}).
\end{align*}
\]
For a sequence $S$, Lift$(S)$ denotes the sequence formed by applying lift$(\cdot)$ to each operation in $S$. Define the sequence $L_p$ to be Lift$(\text{Short}(\vec{L}_p))$.

**Verify:** We now complete the proof by showing that the sequences $\langle L_p : p \in P \rangle$ just constructed are witness sequences for POB$(L)[C]$. We do this by verifying the constraints of Definition 3.3.

| Constraint of Definition 3.3 | Lemma |
|-------------------------------|-------|
| $\forall p \in P : (O_C[p, L_p])$ is a valid total order | Lemma 7.7 |
| $\forall p \in P : \text{Extends}[O_C[p, L_p], p_{\text{pos}}]$ | Lemma 7.6 |
| $\forall p \in P : \text{Extends}[O_C[p, L_p], \text{delOrd}_C]$ | Lemma 7.8 |
| $\forall p, q \in P, l \in L : \text{Agree}[O_C[\text{delivers}(l), L_p, L_q]]$ | Lemma 7.9 |
| $\forall p \in P : (\text{bcast}(m, l) \in O_C$ if and only if $\frac{\text{DE|\text{L}l}}{m, l} \in O_C[p])$ | Lemma 7.5 |

Several parts of the following proofs are the same for labeled and unlabeled updates. When this is the case, we use "queue" to mean any priority-queue or fifo-queue. We use $\text{enQ}$ to denote either a priority-$\text{enQ}$ applied to $\text{priorityQ}[l]$ for some label $l$, or a fifo-$\text{enQ}$ applied to fifoQ$[\hat{p}]$ for some process $\hat{p}$. Similarly, $\text{deQ}$ denotes either an $\text{extractmin}$ or a fifo-$\text{deQ}$. A subscript on a local variable indicates which process owns that variable. For example, $T_p[q]$ denotes $\hat{p}$'s variable $T[q]$. Similarly, a subscript on an operation indicates which process applied the operation. For example, priority-$\text{enQ}_p(\text{priorityQ}, m)$ denotes that this priority-$\text{enQ}$ was applied by $\hat{p}$.

We begin with three sublemmas that capture the essential properties of timestamps. We rely on these lemmas later.

**Lemma 7.2.** For all processes $\hat{p}$ and $\hat{r}$, the writes to $T_{\hat{p}}[\hat{r}]$ taken in program order have strictly increasing values.

**Proof.** $T_{\hat{p}}[\hat{p}]$ changes value only in Line 15 where it is incremented, and Line 26 where it is boosted to a bigger value. Therefore $T_{\hat{p}}[\hat{p}]$ never decreases.

For $\hat{r} \neq \hat{p}$, $\hat{p}$ writes a new value $t$ to $T_{\hat{p}}[\hat{r}]$ only in Lines 21 and 23 because $\hat{p}$ received a TS-UPDATE or ORD-MSG message from $\hat{r}$ with timestamp $t$. So consider the timestamps in TS-UPDATE and ORD-MSG messages sent by $\hat{r}$ to $\hat{p}$. We have just seen that $T_{\hat{p}}[\hat{r}]$ does not decrease, so, given the increment in Line 15, any ORD-MSG sent by $\hat{r}$ to $\hat{p}$ (Line 19) contains a strictly bigger timestamp than that of any previous message sent by $\hat{r}$ to $\hat{p}$. Similarly, given the increase in Line 26, any TS-UPDATE message sent by $\hat{r}$ (Line 27) contains a strictly bigger timestamp than that of any previous message sent by $\hat{r}$ to $\hat{p}$. Since messages are received in fifo order, these messages that $\hat{p}$ receives from $\hat{r}$ have increasing timestamps, confirming that each of $\hat{p}$'s writes to $T_{\hat{p}}[\hat{r}]$ writes a bigger value than was previously written.

**Lemma 7.3.** If $m_1$ and $m_2$ are ORD-MSG messages with labels $g$ and $h$ ($h \neq \bot$) and queue-elements $qe_1$ and $qe_2$ respectively such that $qe_1.ts \leq qe_2.ts$ then for all $\hat{p} \in \hat{P}$, $\text{enQ}_{\hat{p}}(\text{queue}_g, qe_1) \xrightarrow{\text{exQ}_{\hat{p}}(\text{priorityQ}[h])} \text{extractmin}_{\hat{p}}(\text{priorityQ}[h])$.

**Proof.** For a process $\hat{p}$ in $\hat{P}$ to execute $\text{extractmin}_{\hat{p}}(\text{priorityQ}[h])$, CanExtract$\hat{p}(\text{priorityQ}[h])$ must have returned TRUE, implying $T_{\hat{p}}[\hat{q}] \geq qe_2.ts$ for every process $\hat{q}$, and hence, for $qe_1.src$. By Lemma 7.2, each write to $T_{\hat{p}}[qe_1.src]$ is an increasing value, so $T_{\hat{p}}[qe_1.src] \geq qe_2.ts$ remains true.

Notice that each $\text{enQ}_{\hat{p}}(\text{queue}_g, qe_1)$ is called from either Line 18 or Line 24, and each is preceded by a write of $qe_1.ts$ to $T_{\hat{p}}[qe_1.src]$ (Lines 15 and 23). Thus:
Lemma 7.4. If any process \( \text{enQ} q \) a queue-element with timestamp \( ts \), then for all processes \( \hat{q} \) and \( \hat{r} \) eventually the value for \( T_{\hat{q}r} \) becomes and remains at least \( ts \).

Proof. By Lemma 7.2, \( T_{\hat{q}r} \) never decreases, so it suffices to show that it eventually takes on a value equal to at least \( ts \).

A queue-element, say \( qe = [u, ts, c, p] \), can be \text{enQ} ed by process \( \hat{p} \) in line 18 or by process \( \hat{q} \neq \hat{p} \) in line 24 of HandleMessage. Even in the second case, however, \( qe \) was previously \text{enQ} ed by process \( \hat{p} \) in line 18. Process \( \hat{p} \) \text{enQ} s \( qe \) as a consequence of its own \text{LocalBroad} castRequest and incremented \( T_{\hat{p}p} \) to equal \( ts \) in Line 15. It then broadcasts \( qe \) to every other process. For each other process \( \hat{r} \), when \( \hat{r} \) receives \( qe \), if \( T_{\hat{r}r} \) is smaller than \( ts \), then it is boosted in Line 26 to equal \( ts \). Thus, for every \( r \), \( T_{\hat{r}r} \) is eventually at least as big as \( ts \). Furthermore, \( \hat{r} \) \text{FifoBroad} casts every change of \( T_{\hat{r}r} \) via either an \text{ORD-MSG} at Line 19 or a \text{TS-UPDATE} message at Line 27, which upon receipt, by each other process \( \hat{q} \), causes \( \hat{q} \) to set \( T_{\hat{q}r} \) to the received value (Lines 21 and 23). It follows that for all processes \( \hat{q}, \hat{r} \in \hat{P} \), eventually \( \hat{q} \)’s value for \( T_{\hat{q}r} \) is at least \( ts \).

Lemma 7.5. \text{BCAST}(update, l) \in O_C if and only if \( \frac{\text{DELIVER}(l)}{\text{update}, l} \in O_C|p, \forall p \).

Proof. Each transformation of a \( \text{BCAST}(update, l) \) by process \( p \) generates a unique \text{LOCAL-BROADCAST-REQUEST} by \( \hat{p} \), the transformation of \( p \). Each \text{LOCAL-BROADCAST-REQUEST} results in the preparation of a \text{queue-element}, say \( \eta \), (Line 17) that contains \( update \), and which is a parameter in the call by \( \hat{p} \) to \text{ProcessQueueElement} (Line 18). This call results in an \text{enQ} to \text{priorityQ}[\eta] if \( l \neq \bot \) (Line 10) or to \text{fifoQ}[\hat{p}] if \( l = \bot \) (Line 11).

Process \( \hat{p} \) next sends a copy of \( \eta \) to every other process (Line 19) in HandleMessage. Therefore, each \( \text{BCAST}(update, l) \) by process \( p \) results in an \text{enQ} of \( \eta \) at \( \hat{p} \), and also results in an \text{enQ} of \( \eta \) at every other remote process:

\[ \text{send}(\hat{p}, \hat{q}, [\text{LOCAL-BROADCAST-REQUEST}]) \]
Because these are the only two ways anything is enqced, (a call to ProcessQueueElement from Line 18 or from Line 24) there is a 1-1 correspondence between the set of all bcast operations by all processes in the specification level, and the set of all enqqs for each process, $\hat{p}$ in the implementation. Therefore, each process eventually enqqs the same set of queue-elements. Furthermore, each deq operation by $\hat{p}$ corresponds to exactly one deliver operation by $p$ (see the code for deliver). Since only enqqs messages can be deqced, it only remains to show that every queue-element, say $\eta$, that is enqced is eventually deqced.

By Lemma 7.4, for all processes $\hat{q}, \hat{r} \in \hat{P}$, eventually $T_{\hat{q}}[\hat{r}]$ becomes and remains greater than or equal to $\eta.ts$.

Therefore, eventually every priority-enqced queue-element with label $l \neq \bot$ will forever satisfy the timestamp part of the CanExtract predicate. Furthermore, if some $\text{priorityQ}[l]$ contains an queue-element that satisfies this timestamp part of CanExtract, then the highest priority queue-element in priorityQ[l] does, because priority decreases with increasing timestamp.

We now show that eventually $\eta$ will also forever satisfy the counter part of the CanExtract or CanDequeue requirement. Let $S_{\hat{p}}$ be the set of queue-elements, $\gamma$, in $\hat{p}$’s collection of queues, such that either 1) $\gamma$ has label $l \neq \bot$, has highest priority in priorityQ[l], and satisfies the timestamp part of the CanExtract requirement, or 2) $\gamma$ has no label and is at the head of its fifoQ. We just established that this set cannot remain empty. Let $qe_{\hat{p}} \in S_{\hat{p}}$ be the queue-element in $S_{\hat{p}}$ with the least $(ts, source)$ pair when it is not empty.

Since source sends messages in order of increasing timestamp, and channels are fifo, unlabeled queue-elements from source enter fifoQ[source] in order of increasing timestamp. Also, each priorityQ is ordered by increasing timestamp. So every other message from source with timestamp smaller than ts must have been delivered, implying counter[source] + 1 must be equal to $qe_{\hat{p}}.counter$. Therefore, either $qe_{\hat{p}}$ has a label $l \neq \bot$ and satisfies CanExtract or $qe_{\hat{p}}$ has label $\bot$ and satisfies CanDequeue.

Thus, provided only a finite number of messages are bcast (or, in longlived computations, given a weak fairness constraint) every queue-element that is enqced will eventually be deqced. Therefore, bcast($m, l$) $\in O_C$ if and only if bcast($m, l$) $\in O_C$ for every process $p$. □

**Lemma 7.6.** $\forall p \in P : \text{Extends}[O[p, \overrightarrow{L_p}, \overrightarrow{prog}]]$

**Proof.** Let $o_1, o_2 \in O[p]$ such that $o_1 \xrightarrow{\text{prog}} o_2$. For $o \in \{o_1, o_2\}$, $T_{\text{Prog}}(o) \cdot \text{op}$ denotes the operation in the transformation of $o$ so that lift($T_{\text{Prog}}(o) \cdot \text{op}$) = $o$.

1. Extends[O[\hat{p}, \overrightarrow{L_p}, \overrightarrow{prog}]] by the definition of the network model. □

**Lemma 7.7.** $\forall p \in P : (O[p, \overrightarrow{L_p})$ is a valid total order.
Proof. $\vec{L}_{\vec{p}}$ is valid. Hence, the modified $\vec{L}_{\vec{p}}$ after step 1, formed by removing all operations on some subsets of objects, is valid. After step 2, the sequence remains valid because removing some send and recv operations maintains the required validity property: a sequence of message operations is valid if it contains at most one send and recv of any message. After step 3, the subsequence of Short($\vec{L}_{\vec{p}}$) consisting of variables and network operations is valid. However, the subsequence of Short($\vec{L}_{\vec{p}}$) consisting of queue operations contains only deQ operations and is not valid. We now show that validity is restored in $L_p = \text{Lift}(\text{Short}(\vec{L}_{\vec{p}}))$.

The subsequence of $L_p$ consisting of only variables is valid since lift() is essentially an identity map for operations on variables. It remains to show validity for bcast$_p$ and deliver$_p$ operations. Recall that a sequence of bcast$_p$ and deliver$_p$ operations is valid if

1. deliver$_p$ does not precede its corresponding bcast$_p$, and
2. no specific deliver$_p$ occurs more than once.

The proof of Lemma 7.5 showed that each update is delivered exactly once in each $L_p$, establishing (2). Let send($\hat{p}, \hat{p}, \text{LOCAL-BROADCAST-REQUEST, } u, l$) and deQ$_p(\text{queue}_l)$ be operations in $O_{|^\vec{p}}$. The next diagram establishes (1).

1. By definition of network model Extends[$O|p$, \text{HappensBefore} $\vec{L}_{\vec{p}}$, $\vec{HappensBefore}$, $\vec{prog}$ $\cup$ $\vec{MessageOrder}$] and Extends[$O|p$, $\vec{L}_{\vec{p}}$, \text{HappensBefore}$].
2. By construction $L_p$, from definition of lift.

\[ \text{Lemma 7.8.} \quad \forall p \in P : \text{Extends}[O|p, L_p, \text{delOrder}_C] \]

Proof. Let $o_1, o_2 \in O|p$ such that $o_1 \text{ delOrder} o_2$. Then, by definition of delOrder, $o_1 = \text{deliver}_p(u_1, l_1)$ and there is a process $q$ such that bcast$_q(u_1, l_1) \text{ prog} \text{ bcast}_q(u_2, l_2)$. 

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If label is the queue-element at the head of deQ, then TRUE, where send(q, q', [LOCAL-BROADCAST-REQUEST, ] u_1, l_1) and send(q, q', [LOCAL-BROADCAST-REQUEST, ] u_2, l_2) to MessageOrder.

Each process’ counter[src] starts at 0 and is incremented by 1 if and only if a message from [src] is deQed (see line 11 of DELIVER()). Since x_1 < x_2, p must deQ u_1 before u_2:

1. \text{Extends}[O][\hat{p}, p, [\text{DELIVER}_{u_1,l_1}, \text{DELIVER}_{u_2,l_2}, \text{DEQ}_{u_1,l_1}, \text{DEQ}_{u_2,l_2}]].

This proves that \text{Extends}[O][p, L_p, l_p, deQ_{u_1,l_1}, deQ_{u_2,l_2}].
Lemma 7.9. \( \forall p, q \in P, l \in L : \text{Agree}[O_{\text{delivers}(l)}, \xrightarrow{L_p}, \xrightarrow{L_q}] \)

Proof. For each process \( p \) there is a one-to-one correspondence between the set of \( \text{deliver}() \)s by process \( p \) of updates with label \( l \) and the set of \( \text{extractmin}() \)s by process \( \hat{p} \) of queue-elements from \( \text{priorityQ}[l] \). Let \( qe_1 = [u_1, ts_1, t, \hat{q}] \) and \( qe_2 = [u_2, ts_2, t, \hat{r}] \) be two such queue-elements with label \( l \), where \( (ts_1, q) < (ts_2, r) \). Then \( ts_1 \leq ts_2 \), so by Lemma 7.3, for all \( \hat{p} \in \hat{P} \), \( \text{priority-enQ}_{\hat{p}}(\text{priorityQ}[l], qe_1) \xrightarrow{\text{prog}} \text{extractmin}_{\hat{p}}(\text{priorityQ}[l], qe_2) \). Therefore, by the definition of the priority queue (queue-elements are ordered lexicographically by (timestamp, source) pair):

\[
\begin{array}{ccc}
\text{extractmin}_{\hat{p}}(\text{priorityQ}[l]) & \xrightarrow{\text{prog}} & \text{extractmin}_{\hat{p}}(\text{priorityQ}[l]) \\
qe_1 & \text{prog} & qe_2 \\
\end{array}
\]

\[
\begin{array}{ccc}
\text{extractmin}_{\hat{p}}(\text{priorityQ}[l]) & \xrightarrow{\text{prog}} & \text{extractmin}_{\hat{p}}(\text{priorityQ}[l]) \\
qe_1 & \text{prog} & qe_2 \\
\end{array}
\]

Hence, for each label \( l \), and all processes \( p, q \), the orders \( (O_{\text{delivers}(l)}, \xrightarrow{L_p}) \) and \( (O_{\text{delivers}(l)}, \xrightarrow{L_q}) \) agree. \( \square \)

8 Summary, Open Questions and Future Work

This paper introduced partition consistency, a parameterized memory consistency model, from which other known models can be instantiated. Four implementations of partition consistency on a message-passing network of multithreaded nodes were also developed and proved correct. All implementations are structured with a middle-level of abstraction which serves to modularize the implementations and simplify our proofs. The implementations are based on Attiya and Welch’s slow-write/fast-read and fast-write/slow-read methods [9]. Both the token-based and queue-based variants are achieved by extending Attiya and Welch’s total order broadcast [9] to a partial order broadcast.

All four implementations were proven correct using a unified framework. Such unified descriptions of memory consistency models at different levels of abstraction and the associated proof techniques provide more confidence in proofs that are otherwise tedious, lengthy and ad hoc.

Our proofs assume that the specification-level computations always terminate. Extending these proofs to long-lived computations is not involved but tedious. It would be useful to have a general technique to “reduce” the long-lived case to finite cases. We also suggest that the framework, the proof set-up and the diagrammatic proof descriptions used in this paper could be used to establish the correctness of other memory consistency models for various multiprocess machines, or networks or languages (for example, C++).

Let us call a correct implementation \textit{exact} if every computation of the specification level is an interpretation of some computation of the target level. Our implementations in this paper are correct but not exact; there are computations that satisfy partition consistency that could not happen in our implementations. For example, abstract memory consistency models such as P-RAM and PC-G allow a kind of cyclic causality, such as the computation:
This computation contains a cycle. The first process must read the value written by the second process before writing but the second process must read the value written by the first process before writing. This problem can be overcome by adding a causality constraint to the memory consistency definitions. Our implementations prohibit such cyclic computations. Hence, our implementations are stronger than the memory consistency models they implement — the specifications allow such computations, but our implementations do not. Though this computation may seem impossible in actual implementations, it could conceivably be possible if there is a prediction system in place. Our proof method could still be used with such a system.

As a second example, consider the computation:

\[
p: \quad \text{read} (x), \quad \text{write} (y, 2) \quad q: \quad \text{read} (y), \quad \text{write} (x, 1)
\]

This computation is possible in a P-RAM implementation that broadcasts to itself, provided there is no guarantee that a process applies its own write before any other process applies that write. The first process broadcasts \text{write} (x, 1) which is received and applied by the second process. The second process then broadcasts \text{write} (x, 2) and \text{write} (y, 3). The first process receives \text{write} (x, 2) before its own \text{write} (x, 1) and so overwrites the 2 with a 1, even though \text{write} (x, 1) “caused” \text{write} (x, 2). This computation also could not happen in the implementations in this paper. This shows that our implementations are not exact, and that the simplest causality constraint added to the memory consistency definition is insufficient to make it exact. Whether or not there is a simple strengthening of the partition consistency predicate to make our current implementations exact remains a question for future research.

A related issue to exactness is optimality. We believe that our implementations use minimal synchronization in the following sense. For every synchronization that is added by the transformation, there exists a program whose transformation would create computations that do not satisfy partition consistency if that synchronization is removed. Confirming this intuition is beyond the scope of this paper.

Since the transformations in this paper are general, they are not optimal for all programs. Transforming individual programs may lead to more efficient implementations. Hence, another approach that we have not followed but is pursued by others (see Section 2) aims to determine for each program what synchronization is necessary and sufficient to preserve correctness on the target machine.

A different direction that could complement this research is the assessment of the performance gains of partition consistency instantiations over sequential consistency. Our preliminary experiments on Westgrid’s 128 node “matrix” cluster [26] are inconclusive. But some of these instantiations, and particularly the weak sequential consistency model, show a potential to outperform sequential consistency. This complementary study will be the subject of future work.

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