A Survey of Aging Monitors and Reconfiguration Techniques

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Abstract

CMOS technology scaling makes aging effects an important concern for the design and fabrication of integrated circuits. Aging deterioration reduces the useful life of a circuit, making it fail earlier. This deterioration can affect all portions of a circuit and impacts its performance and reliability. Contemporary literature shows solutions to monitor and mitigate aging using hardware and software monitoring mechanisms and reconfiguration techniques. The goal of this review of the state-of-the-art is to identify existing monitoring and reconfiguration solutions for aging. This survey evaluates the aging research, focusing the years from 2012 to 2019, and proposes a classification for monitors and reconfiguration techniques. Results show that the most common monitor type used for aging detection is to monitor timing errors, and the most common reconfiguration technique used to deal with aging is voltage scaling. Furthermore, most of the literature contributions are in the digital field, using hardware solutions for monitoring aging in circuits. There are few literature contributions in the analog area, being the scope of this survey in the digital domain. By scrutinizing these solutions, this survey points directions for further research and development of aging monitors and reconfiguration techniques.

Index Terms

Aging monitors, reconfiguration techniques, survey.

I. INTRODUCTION

With the scaling of CMOS technology circuit reliability issues become increasingly relevant for the design of integrated circuits. Among these issues, circuit aging is getting critical, as it inevitably affects all circuits. The literature shows an increase in the number of papers related to aging between 2000 to 2020 [1], [2], [3]. This trend is due to the development of ultra-deep submicron technologies, where reliability became crucial [4].

Aging is the deterioration of circuit performance over time [5], which can reduce the useful life of a circuit. This deterioration can increase circuit delay and affect all portions of a System-on-Chip (SoC), analog circuit, digital logic, and memory. One important factor that accelerates aging is power. The increase of power in modern circuits increases the temperature and makes these circuits susceptible to effects like bias temperature instability (BTI) and hot carrier injection (HCI) [6].

One solution to deal with aging effects is to add design safety margins to the circuit, such as clock margins. These margins ensure correct operation even in the presence of aging effects once they are designed according to worst-case conditions. However, these margins decrease performance, as they increase the clock period. The literature presents other solutions to mitigate aging, allowing to extend the lifetime of chips. These solutions monitor parameters that indicate aging effects. The monitored parameters include temperature, frequency variation, delay variation, among others. Decision methods, as threshold voltage analysis, evaluate whether the monitored parameters have an appropriate range of values. Activation mechanisms, such as voltage and frequency adaptations, bring the circuit back to the safe parameters if these do not meet predefined constraints.

The goal of this review is to study existing solutions for monitoring aging effects in circuits and dealing with them. This study seeks to answer two questions: (i) what solutions the literature presents for aging monitoring? and (ii) what solutions the literature presents for circuit reconfiguration? This work surveys the literature from 2012 to 2019, while works [7], [8], [9] map aging monitors since 1998. Thus, this survey fills the gap related to aging surveys, covering the most recent works.

The literature review considered three main search terms:

- Integrated Circuits: this category limits the search to the area of integrated circuits. The search string presents the terms used to reference this area, like VLSI, system, and architectures;
Monitoring and Self-reconfigurable Circuits: this category includes the monitoring area and the problems induced by aging, as Negative-Bias Temperature Instability (NBTI);

Aging: this category limits the research by aging problems.

The Scopus abstract and citation database (https://www.scopus.com) was the start point of the research. After that, the review researched in IEEE (https://ieeexplore.ieee.org) and ACM (https://www.acm.org) databases. Finally, the research focused on Google Scholar (https://scholar.google.com) database. The review considered journals and conference papers published since 2014.

This survey is organized as follows. Section II presents basic definitions to the understanding of this work. Section III presents a review of other surveys available in the literature. Section IV presents the proposed classification for the reviewed papers. Section V discusses comparatively the reviewed works. Section VI presents in detail the literature survey. Section VII concludes this survey.

II. BASIC DEFINITIONS

This section provides definitions required for the understanding of this survey.

**Definition 1.** Critical path: is the purely combinational path with the most significant delay between any two registers or primary I/O ports in a design.

**Definition 2.** Soft-errors: errors that can occur in a circuit when it is exposed to radiation, like cosmic rays and neutrons particles. Single-event upset (SEU) is an example of soft-error, when the exposition to radiation can generate a change in the memory elements values, generating erroneous outputs [10].

Important effects are considered in the aging research: NBTI (Definition 3), PBTI (Definition 4), HCI (Definition 5).

**Definition 3.** NBTI – Negative Bias Temperature Instability: increase in the threshold voltage and consequently decrease drain current and transconductance of a transistor [11]. It occurs in PMOS transistors and is caused by circuit aging.

**Definition 4.** PBTI – Positive Bias Temperature Instability: similar to NBTI, but in NMOS transistors. Since the introduction of the high-K gate dielectrics and metal gates transistors, the effect of PBTI becomes comparable to the NBTI one.

**Definition 5.** HCI – Hot-Carrier Injection: consists of a voltage drop that produces a large electric field in the region near to the drain of a transistor in saturation mode. It can result in the change of transistor characteristics such as the threshold voltage [12]. According to Novak et al., from Intel, [13], tri-gate technologies as 14nm can help to mitigate HCI effects together with body bias adjust techniques.

Classic test approaches are adopted for aging monitoring and reconfiguration techniques: DfT (Definition 6), BIST (Definition 7), ATPG (Definition 8).

**Definition 6.** DfT – Design for Testability: a set of techniques used to improve circuit testability by increasing controllability and observability in the design [14].

**Definition 7.** BIST – Built-in Self-Test: a mechanism that tests the circuit itself, verifying all or a portion of the internal functionality of the design [14]. The hardware and/or the software is built into integrated circuits allowing them to test their operation. The main advantage of BIST is the ability to test internal circuits having no direct connections to external pins or external testers. In addition, BIST allows testing in the field.

**Definition 8.** ATPG – Automatic Test Pattern Generation: a method that finds an input sequence (called test vectors) that enables automatic test equipment (ATE) to distinguish between the correct circuit behavior and the faulty circuit behavior caused by defects.

III. PREVIOUS AGING SURVEYS

Rahimipour et al. [7] review on-chip monitors for temperature, soft-errors (Definition 2), and critical paths (Definition 1), covering the period 1998-2011 (21 works). Figure 1(a) presents their classification divided in: monitors for...
high temperature induced problems; monitors for soft-errors; monitors for critical paths; and collaborative monitors, which combines the previously mentioned class of monitors. Soft-errors detects change caused in memory elements due radiation. Thermal monitors identify problems induced by high temperatures. Critical path delay monitors detect changes in the critical path, as delay increases. Collaborative monitors are a combination of more than one class of monitors. Figure 1(b) summarizes the monitor types and also informs cause, effect, and control action for each effect.

Khoshavi et al. [8] review the period 2004-2015 (30 works). Their work analyzes aging monitors and also aging models and techniques for aging mitigation. Aging models are used to predict the degradation of the circuit due to aging. Mitigation techniques are used to deal with aging effects and ensure correct behavior of the circuit under these effects. Besides, their work proposes a taxonomy to classify the aging mitigation techniques, shown in Figure 2. Worst-case design techniques add safety margins to the circuit characteristics, like frequency and supply voltage, at design-time. Design time aging-aware balancing focuses on balancing circuit delay to reduce aging effects. Dynamic adaptation techniques are online approaches to tune the design under aging during circuit operation. Adaptive resource management techniques mitigate the aging effects either through the management of idle time (Idle-Time Leveraging schemes, also called ITL schemes), power management and task scheduling (controlled resource wearout), or availability of expendable resources (spatial redundancy).

Kochte et al. [9] review the period 2007-2017 (14 works). Their work analyses self-test, self-checking, and self-diagnosis online techniques for self-awareness. Online techniques include aging monitors. Figure 3 shows the classification for self-test and self-checking, which contains non-concurrent and concurrent approaches. Non-concurrent approaches regard self-testing methods, including classic methods, as BIST, and techniques like suspending the circuit operation to execute the test. Concurrent approaches are self-checking methods executed during the circuit operation, which includes aging monitors.

IV. PROPOSED CLASSIFICATION OF AGING MONITORS AND RECONFIGURATION TECHNIQUES

Our proposed classification extends the taxonomy of previous work [7], [8], [9], considering parameters included in the state-of-the-art and features of the circuits monitored by them. Thus, this work proposes the following set of parameters for aging monitors classification:

![Fig. 1. Monitors types and control actions. Adapted from [7].](image)
Fig. 2. Taxonomy of aging mitigation techniques. Adapted from [8].

Fig. 3. Self-test and self-checking circuits classification. Adapted from [9].

- **Temperature**: a temperature monitor detects aging effects by measuring the variation in the temperature of the circuit. Temperature variations cause aging effects as NBTI and PBTI;
- **Critical path**: critical path monitors can be used to identify timing errors due to wrong transitions, SEU, or delay increase on circuit paths. These errors are detectable by comparing a circuit path controlled by the system clock and the same path controlled by a delayed clock [15];
- **Clock frequency**: clock frequency monitors measure the frequency variation of a clock circuit under aging. This type of monitor uses a reference frequency to identify a change in the circuit operating frequency;
- **Workload**: workload monitors measure the workload of a circuit to identify the stress level. Similar to the CPU load measure.
- **Circuit state**: circuit state monitors consider the state of the entire system. For example, some techniques use the BIST circuit output to evaluate aging effects;
- **Voltage**: Voltage monitors analyze the threshold voltage of the circuit. Aging effects as NBTI can change the threshold voltage of transistors.

Table I presents the aging monitors addressed in this survey and compares with those covered by previous works. Note that the Table does not include survey [8] because it does not consider aging monitors. Our work addresses eight monitors types, including monitors not covered by previous works.

This work adopts the following classification of reconfiguration techniques:

- **Dynamic voltage scaling**: Dynamic Voltage Scaling (DVS) is a power management technique where the voltage used in a component increases or decreases, according to some criteria [16]. An example of an approach to manage power dissipation is the adoption of a closed-loop control technique where the voltage is a knob to
meet the power goal [17].

- **Dynamic frequency scaling**: Dynamic frequency scaling (DFS) is a technique similar to DVS, but applied to the circuit frequency. Similarly, if the circuit needs a boost in performance, the frequency is increased. If the circuit or application can tolerate lower performance, the frequency may be decreased to allow power savings;

- **Aging compensation**: Aging compensation is a technique that enables the circuit to alleviate aging effects. For example, some circuits activate extra devices, in parallel to the main circuit, to increase the driving strength of an output driver, compensating the degradation due to HCI and BTI effects [18];

- **Body-bias adaptive**: Body-bias adaptive (BBA) is a technique that allows tuning the transistor threshold voltage [19]. This technique helps to mitigate and compensate for the NBTI impact in the circuit;

- **Workload reduction**: Workload reduction is a series of software approaches to reduce the workload system by introducing, for instance, no operation (NOP) instructions during the system operation.

Table II compares reconfiguration approaches covered by the previous works, and the ones addressed in this survey. The Table does not include survey [9] because it does not address reconfiguration techniques. Also, note that this survey does not address three types of reconfiguration techniques (clock throttling, backward recovering and computational sprinting) that were covered in the previous surveys because these techniques were not adopted in the research papers from 2012 to 2019. Our work addresses five reconfiguration approaches, including two types not covered by previous works.

### Table II

|                             | [7] | [8] | This Survey |
|-----------------------------|-----|-----|-------------|
| Dynamic Voltage Scaling     | A   | A   | A           |
| Dynamic Frequency Scaling   | A   | A   | A           |
| Aging Compensation          | NA  | A   | A           |
| Body Bias Adaptive          | NA  | NA  | A           |
| Workload Reduction          | NA  | NA  | A           |
| Clock Throttling            | A   | NA  | NA          |
| Backward Recovering         | A   | NA  | NA          |
| Computational Sprinting     | NA  | A   | NA          |

### V. Discussion Related to the State-of-the-Art

This Section brings a summary of the presented techniques, remarks, and insights about how to deal with aging. Also, this Section answers the research questions presented in the Introduction Section. The classified state-of-the-art works are described in Section VI.
About industry, most applications rely on sensors built in SoCs that allow measuring variations in such parameters as the circuit ages. These sensors are commonly distributed across the die and accessible through DfT infrastructure or as peripherals to CPUs. The most common sensor consists of a set of ring oscillators that control asynchronous counters. These counters provide an overview of how the overall speed of the circuit is being impacted by aging [20].

A. Summary and remarks of the literature review

Table III summarizes the reviewed works. The “Overall Monitoring” column means monitoring the entire circuit, not just the critical paths using, for example, the voltage or the current. The “Monitor Insertion Strategy” column corresponds to approaches that use some strategy to insert the monitors, such as statistical methods, and not based only on critical paths. The “Structure Reuse” column shows designs that use structures available in the circuit for monitoring aging effects. In these cases, only DfT structures are reused. The “Metastability Concern” column contains works concerned with metastability issues.

Circuits monitoring the overall system may present a low area overhead, once one mechanism can be applied for the entire design. This approach may be better in terms of area overhead when compared to solutions focusing on inserting monitors in all critical paths. However, designs that use methods to select paths to insert monitor are also promising in terms of area overhead reduction. The reuse of DfT structures is a promising strategy to choose paths, once test insertion overhead is already present in the circuit. This allows reducing the impact of aging monitors on area.

A ”no” in the first column (Overall Monitoring) means that only part of the system is monitored. This means that specialized mechanisms may be required for different parts of the system. Particularly, works with a ”no” in the second and/or third columns in Table III (Monitor Insertion Strategy and Structure Reuse) can present a significant overhead in the system. Nevertheless, these solutions may be useful for detecting aging and could be combined with path selection strategies to reduce the system overhead, making their use feasible.

Metastability is a concern present in only two works. It is an important issue, once its effects may propagate through designs, reducing circuit reliability, making them fail even in the absence of aging effects. Metastability can also be an issue to systems with more than one clock domain, due to the clock synchronization between domains. Thus, these two works have an advantage compared to other approaches since they use the same circuitry to deal with both aging and metastability effects.

A feature that can be observed is that voltage and frequency scaling are reconfiguration techniques associated mostly with critical path monitors, once it is possible to control the circuit speed by these two parameters. Similarly, body bias adjustment is associated with voltage monitors, once this reconfiguration technique changes the threshold voltage for compensating aging effects.

B. Remarks about aging monitors

Figure 4 and Table IV present the answer to the first research question of this survey, “What solutions the literature presents for aging monitoring?”. The Figure shows the monitor types covered by this survey. The most common monitor type used for aging detection are timing error monitors, which is present in 36.58% of the reviewed papers. The second most common monitor type used for aging detection is temperature monitor, which is present in 27% of the papers.

C. Remarks about reconfiguration techniques

This Section answers the second research question of this survey: “What solutions the literature presents for circuit reconfiguration?”. Figure 5 and Table V present the reconfiguration techniques covered in this survey. According to the Table, voltage scaling is the most adopted reconfiguration technique, present in 50% of the papers about reconfiguration techniques. The second most common reconfiguration technique used for aging detection is frequency scaling, which is present in 28.57% of the papers.
## TABLE III
**Summary of the Literature Review.**

| Overall Monitoring | Monitor Insertion Strategy | Structure Reuse | Metastability Concern |
|--------------------|---------------------------|----------------|----------------------|
| [21], 2015         | yes                       | no             | no                   |
| [22], 2017         | yes                       | no             | no                   |
| [23], 2017         | yes                       | no             | no                   |
| [24], 2017         | yes                       | no             | no                   |
| [25], 2015         | yes                       | no             | no                   |
| [26], 2016         | yes                       | no             | no                   |
| [18], 2014         | yes                       | no             | no                   |
| [27], 2016         | yes                       | no             | no                   |
| [28], 2019         | yes                       | no             | no                   |
| [29], 2015         | no                        | no             | yes                  |
| [30], 2017         | no                        | no             | no                   |
| [31], 2018         | no                        | no             | yes                  |
| [32], 2016         | no                        | no             | no                   |
| [33], 2015         | yes                       | no             | no                   |
| [34], 2017         | no                        | no             | no                   |
| [35], 2014         | no                        | no             | no                   |
| [36], 2017         | no                        | no             | no                   |
| [37], 2014         | no                        | yes            | no                   |
| [38], 2014         | no                        | yes            | no                   |
| [39], 2018         | no                        | no             | no                   |
| [40], 2017         | no                        | yes            | no                   |
| [41], 2015         | no                        | yes            | no                   |
| [42], 2019         | yes                       | no             | no                   |
| [43], 2019         | yes                       | yes            | no                   |
| [44], 2018         | no                        | no             | no                   |
| [45], 2012         | no                        | yes            | no                   |
| [46], 2014         | no                        | yes            | no                   |
| [47], 2014         | no                        | yes            | no                   |
| [48], 2015         | yes                       | no             | no                   |
| [49], 2016         | yes                       | no             | no                   |
| [50], 2014         | no                        | no             | no                   |
| [51], 2014         | no                        | yes            | no                   |
| [52], 2015         | yes                       | no             | no                   |
| [53], 2017         | yes                       | no             | no                   |
| [54], 2015         | yes                       | no             | yes                  |
| [55], 2015         | yes                       | no             | yes                  |
| [56], 2019         | yes                       | no             | no                   |
| [57], 2017         | yes                       | no             | yes                  |
| [58], 2015         | yes                       | no             | no                   |
| [59], 2015         | yes                       | no             | no                   |
| [60], 2018         | yes                       | no             | no                   |

### VI. Literature Review

This Section describes the papers related to aging monitors and reconfiguration techniques covering the years from 2012 to 2019. The subsections are grouped by monitoring approaches, according to the classification proposed in Section IV for aging monitors. When a paper also presents a reconfiguration technique, it is described together, in the same paragraph.
A. Temperature Monitors

NBTI, PBTI, and HCI are aging effects accelerated by temperature increase in chips. System workload affects power dissipation, which has a direct impact on the temperature. Thus, monitoring temperature helps to deal with
these effects. Some sensors use ring-oscillators to capture the aging effects caused by temperature increase. This kind of sensor provides an indirect measurement of temperature, and can be considered a temperature monitor.

Igarashi et al. [21] propose an aging monitor implemented with ring-oscillator (RO) to measures BTI and AC hot-carrier-injection (AC-HCI). The monitor consists of a symmetric RO (SRO) and an asymmetric RO (ASRO). ASRO is an RO composed of standard cells of different drives, while SRO is implemented only by standard cells with the same driving strength. With these two types of RO, it is possible to separate NBTF and PBTI effects for analyses by observing them under DC stress conditions. Also, the speed degradation caused by AC-HCI can be detected because unbalanced delay with a long/short transition in ASRO has high sensitivity against AC-HCI under AC stress. A dynamic voltage and frequency scaling (DVFS) technique controlled by software is used to change the supply voltage and clock activity dynamically and reconfigure the circuit. A test chip, including both SRO and ASRO using NAND2 standard cells, was implemented in a 16 nm Fin-FET bulk CMOS technology. Results show that $V_{th}$ shift due to PBTI measured from frequency degradation is 2mV, which is still 1/10 of NBTF in Fin-FET technology, and that is possible to reduce the BTI guard bands in 45% at the nominal frequency operation.

Majerus et al. [22] use ROs to measure changes in transistor and resistor parameters as a function of the stress caused by aging. The result is a data-driven aging model that provides information that can be used to ensure system reliability.

Sengupta and Sapatnekar [23] present two methods that use sensors implemented with ROs to detect the delay shifts in circuits as a result of BTI and HCI effects. The first method uses a pre-silicon analysis of the circuit to compute calibration factors that can translate the delay shifts in the ROs with a delay estimate of 1% of the real values. The second method uses an analysis where sensor measurements are combined with infrequent online delay measurements to reduce the circuit guard bands and allows 8% lower delay guard banding overheads compared to the conventional methods.

Kim et al. [24] propose a new test structure of RO that helps to measure the stress duty cycle (SDC) of the HCI. SDC is the ratio between the stress caused by the aging effect and the circuit cycle time [61]. The structure is composed of a NAND gate that has the function of enabling the oscillator mode and inverters. VDD and GND bias of the HCI stress inverter are set up in a complementary way during the stress, making the device not suffering from BTI aging. Also, a buffer is designed as a compensator for the signal falling by as much as $V_{th}$. Results demonstrated that HCI SDC increases with frequency, but the maximum duty cycle was much less than 2%.

Shakya et al. [25] propose an NBTI sensor that uses two ROs, one without circuit influence used as a reference and other to evaluate the degradation circuit under stress, and compare the output of both. This approach gives the manufacturer the exact control over the yield and accuracy of the sensors, which not occurs with ad hoc approaches that determine parameters such as the decision threshold.

Miyake et al. [26] propose an aging-tolerant monitor that analyzes frequencies of more than one RO. Thus, it is possible to derive the values for temperature and voltage from the frequencies using multiple regression analysis. Besides, three techniques to select the RO types are proposed to improve the accuracy of the measurement. The method was validated with simulations in 180 nm, 90 nm, and 45 nm CMOS technologies. In the 180 nm technology, temperature accuracy is about 0.99°C, and voltage accuracy is about 4.17 mV. Also, the authors fabricated test chips with 180 nm CMOS technology to confirm its feasibility.

Kumar [18] presents an aging compensation technique for a CMOS transistor output driver. It contains an aging compensation cell which monitors the degradation in the ON current ($I_{ON}$) of output driver due to the HCI and BTI effect. Based on this degradation, the aging compensation cell generates compensation codes for PMOS and NMOS transistors drivers. These aging compensation codes turn on devices in parallel to the main driver, increasing the drive strength of output, which compensates the degradation in NMOS and PMOS driver due to HCI and BTI effects. The design was implemented in 40 nm CMOS process by using 1.8V thick-oxide devices. Results show that by using the proposed aging compensation technique, the impact of aging on output driver reduces by 70% after ten years of operation.

Ali et al. [27] use IJTAG to manage temperature health monitors on the chip. The temperature health monitors are based on a Wheatstone bridge, which is composed of four resistors, one operational amplifier, one filter, and one analog to digital converter. Results show that the proposed solution can be used to manage and control instruments to ensure the reliable operation of the chip over its lifetime. According to the authors, the proposed method can reduce the overall time spent on the test, once there is no off-chip interface, and the system clock can be used instead of the test clock.
Rathore et al. [28] propose to use temperature and NBTI sensors to implement a task mapping strategy to manycore systems, called LifeGuard. LifeGuard considers performance and aging as parameters to perform task mapping, and is based on reinforcement learning. At each tile of the network-on-chip (NoC), an NBTI and a thermal sensor are added and used to perform the task mapping. As a benefit, LifeGuard prevents the rapid aging of cores that map a more significant number of tasks. Also, it improves the aggregate safe operating frequency of the system. Experimental results using a 256-core system showed that LifeGuard improved the health of the cores for 57% when compared to the HiMap strategy [62], and 74% when compared to the Hayat [63]. Also, LifeGuard shows a better system performance.

B. Critical Path Monitors

Contemporary literature presents monitors that capture timing errors on the critical paths of circuits (Definition 1). This technique contains extra components that capture the memory register output of the critical paths and its processed data. A comparison between these data is executed to identify if a timing error occurred.

Savanur et al. [29] present a BIST (Definition 7) approach to detect aging effects on the circuit during test mode. The BIST circuitry uses two identical buffer chains and a logic block to compare the output of these chains. If there is a difference between the outputs of the chains, an error caused by aging is detected. The approach needs extra components, which are a D flip-flop, a NAND gate, an AND gate, and two buffers. HSPICE simulations on 45 nm and 65 nm were performed to extract results. This paper focuses only on the NBTI aging factor, and results show that the solution can detect minimal stress levels in the presence of process variations and that the aging detection depends on the time that a path of the circuit keeps at logic level zero.

Sai et al. [30] present a Parity Check Circuit (PPC) for monitoring delay-faults and compare it with the Canary flip-flop approach [64]. Unlike the Canary flip-flop approach, PPC can monitor more than one logic path simultaneously, which allows reducing the number of sensors. PPC is implemented using a multiple-input XOR gate, a delay element (DE), a matched delay element (MD), a flip-flop, a shadow flip-flop, and a 2-input XOR gate. The multiple-input XOR gate is responsible for computing the data parity, and the MD is responsible for adding a delay to the clock signal to compensate delay produced by the multiple-input XOR gate. The PPC was validated in a 32 bit MIPS processor using a 65 nm technology. Results indicate that the use of the circuit reduces area overhead by 66% and power by 33% when compared to the Canary flip-flop approach.

Sai et al. [31] propose a metastability-free aging sensor called Differential Multiple Error Detection Sensor (DMEDS). The sensor monitors multiple paths concurrently. It is composed of a Multiple Detection Unit (MDU) and a stability checker, which allows monitoring two or more critical paths simultaneously. Any transition in the data active the MDU output signal that is captured by the stability checker, signaling a delay fault. The stability checker checks the stability of the delayed signal while the clock is high. DMEDS was designed at transistor level using a 32 nm technology and applied to a 32-bit MIPS processor to monitor ten paths concurrently. Results show that using DMEDS for monitoring ten paths can save 197.1% and 97.1% in area overhead when compared to Razor [15] and Canary [64], respectively.

Copetti et al. [32] propose a hardware-based technique able to increase ICs lifetime. The technique is based on a sensor able to monitor IC aging and to adjust its power supply voltage to minimize NBTI effects, increasing the circuit lifetime. The approach is composed of: (i) an aging sensor, which contains a delay element and the stability checker; (ii) an actuator, which contains a counter and a decoder block; and (iii) a flip-flop inserted at the critical path output. The flip-flop output of the critical path passes through the delay element and the stability checker while the clock signal is high, analyzing data transitions. If a transition while the clock is high occurs, it means that the delay of the circuit increased, changing the output of the stability checker and indicating a timing violation. Also, the actuator receives the signal from the stability checker and increases its counter, allowing the decoder to adjust the power supply. Experimental results obtained by simulations demonstrate that the technique increases the circuit lifetime by 150%.

Sadeghi-Kohan et al. [33] propose a self-adjusting age monitoring method to pipeline circuits, which allows detecting progressive changes in the timing of a circuit. The output of the critical paths are captured using an age monitoring clock (that occurs before the system clock), and this captured data is compared with the same output but captured at the rising edge of the system clock. The circuit used to adjust the age monitoring clock has an age indicator counter that counts RO pulses to adjust the clock phase and is initialized with the core process
characteristic. As the core ages, the age indicator counter is incremented, causing a more extended clock phase shift, and shorter slack time. The monitors are designed targeting low hardware overhead and accuracy in reported timing changes.

In another work, Sadeghi-Kohan et al. [34] use a similar strategy to monitor paths of a circuit and to detect its continuous age growth. This approach can provide the aging rate and the aging state of the circuit. The proposed strategy uses a clock generator to feed the register responsible for capturing the data before the system clock. Results show an area overhead of 2.13%, a power overhead of 0.69%, and a low-performance overhead. Yi et al. [35] present a scan-based on-line monitoring that monitors aging during system operation and gives an alarm if the system detects aging effects. This work inserts an extra scan chain that captures early the functional data (at the opposite edge of the system clock) within a given guard-band interval during system operation. After that, the extra scan chain output is compared to the original scan chain output, which allows detecting violations. The scan-chain scheme contains two scan-chains, one with conventional scan cells (SC scan-chain) and the other one with the early capture scan cells (ECSC scan-chain). The SC flip-flops capture the data at the clock rising edge, while the ECSC flip-flops capture the data at the clock falling edge. The modified scan chain uses an XOR gate to compare the captured data.

Jung [36] presents an aging level estimating flip-flop that exploits the frequency guard band of a device to estimate the aging level with a small power overhead, called performance estimation flip-flop (PEFF). The PEFF has five elements: i) a scan flip-flop; ii) a shadow latch; iii) a sampling time indicator; iv) a logic block to controls the input of the performance result cell (PERC); v) the PERC. The shadow-latch is used to sample the data earlier than the functional flip-flop. Results show a reduction in monitoring time, and the power consumption is reduced by 50% when compared to the Yi et al. [35].

Vazquez-Hernandez [37] proposes a solution for error prediction using an aging sensor based on the Error-Detection Sequential (EDS) circuit [65]. The EDS has a decoder module to monitors the critical paths. When one of the paths is activated, the decoder active the EDS to allow detect errors. The methodology for path selection uses statistical static timing analysis. Results show that the EDS can reduce power overhead form 102% to 6% and area overhead from 69% to 22% when compared to [5] and [35], considering the circuit characteristics as the number of gates and buffers.

Chandra [38] proposes the SlackProbe monitor. This approach inserts timing monitors at endpoints and intermediate nodes of the circuit paths. If a monitor is inserted at an intermediate node, an AND gate is used as delay matching, and a transition detector is connected to the intermediate node with a minimum size inverter. If a signal transition at the intermediate node occurs, it arrives at the transition detector through the delay chain, and the signal is compared with the incoming clock edge. If the transition is close to its required arrival time, a corresponding signal transition arrives at the transition detector input after the clock edge. This transition triggers the transition detector and flags a signal indicating a delay failure. The monitor inserted at the intermediate node is capable of monitoring the delay of all critical paths passing through it, and its output can be used for mitigating failures due to aging (based on hardware or software). The results show that SlackProbe can achieve up to 16x reduction in the total number of monitors.

Masuda and Hashimoto [39] propose an error prediction adaptive voltage scaling (EP-AVS) and a mean time to failure aware (MTTF-aware) design methodology for EP-AVS circuits. The EP-AVS has a main circuit plus a timing error predictive flip-flop (TEP-FF) and a voltage control unit. The TEP-FF has a flip-flop, delay buffers, and a comparator implemented with an XOR gate. Also, TEP-FF works with the main flip-flop. When the timing margin is gradually decreasing, a timing error occurs at the TEP-FF before the main flip-flop captures a wrong value due to the delay buffer. This wrong value produces an error prediction signal, which allows the voltage control logic to provide a higher supply voltage and reduce the circuit delay. Evaluation results show that the proposed EP-AVS design methodology achieves a 20.8% voltage reduction while satisfying the target MTTF.

Vijayan et al. [40] propose an aging monitor based on hardware and software. The system is composed of representative flip-flops (RFF) that are selected in an offline phase and connected to the monitoring hardware. The aging effect consists of two phases: i) stress phase, where the transistor is under the aging effect; ii) recovery phase, where the transistor is recovering from the stress phase. A switching event in the RFF corresponds to the recovery phase of the corresponding flip-flop group, which is captured to report the recovery event to the software. The representative flip-flops are observed by a switching-event detector to perform the capture operation, which is composed of an XOR gate and a shadow flip-flop that generates a pulse at its output when a logic transition
occurs in the corresponding flip-flop. The output of the switching-event detector is encoded using a priority encoder. In a determined clock cycle, the output of the priority encoder indicates the index of the flip-flop that switches its state in that particular clock cycle. If two representative flip-flops change their states at the same time, the priority encoder ensures a valid output. The critical-flag register (CFF) keeps the criticality word to represent the recovery/aging state of the corresponding representative flip-flop. This paper uses a software subroutine to mitigate aging by inserting NOPs instructions, which allows a relaxation on BTI stress, reducing the workload. Results show that area and power overheads imposed by the monitoring hardware are less than 0.25% for a Leon3 processor and Fabscalar processor.

Saliva et al. [41] propose monitors based on delay elements called pre-error flip-flops. The approaches are composed of a shadow flip-flop that stores delayed data, and is works in parallel to the regular flip-flop. The approach compares the two flip-flop outputs, and a pre-error signal is generated to predict the occurrence of timing errors. Each monitor uses different delay approaches. The first approach is the buffer delay, where buffers produce the delay. The second is the passive delay, where a resistor generates the delay. The last is the master delay, where master-slave latches replace the regular flip-flop, and the slave latch outputs feed the shadow flip-flop to generate the delay. Results show that the detection window of the in-situ monitors with passive delay is less deviant than the buffer and master delay ones with $V_{dd}$ decrease. However, using a passive element in a digital circuit is not common. The in-situ monitor with buffer delay is a better choice because it uses standard cells in its implementation.

Di Natale et al. [42] propose a hidden-delay-fault sensor that can be used to detect small delay faults. The sensor allows the circuit to operate at the nominal frequency, and it is inserted in a critical path. The monitor works by sampling a signal in both clock edges. After that, the monitor compares the two samples using an XOR gate and stores the result on the next falling edge of the clock using a shadow flip-flop. Result extraction is performed using a classic scan chain. The authors propose that the sensor can be used during the lifetime of the circuit to identify timing violations in short paths caused by aging. Also, the authors mention that it is possible to use the sensor combined with reconfiguration techniques such as DVFS. The paper does not present results.

Wang et al. [43] uses a timing margin detector (TMD) to monitor aging and capture delay behavior. Also, the output detector is used in a machine learning engine based on a support vector machine (SVM) to predict aging. The TMD is used to capture late transitions. It is composed of two D flip-flops, and by an OR gate at the flip-flops output. Results show that it is possible to obtain a 97.40% of accuracy in aging prediction, with 4.14% area overhead on average.

Rohbani and Miremadi [44] propose an aging sensor combined with the flip-flops of the design that monitors the critical path output before the rising edge of the clock signal. This signal follows the system clock by an adjusted delay of about 10% to 20% of the clock period. When the clock is at logic level one, the sensor is activated. Any change in the input signal during the period where the sensor clock is at logic level one and the system clock is at level logic level zero represents a delay extension of the critical path due to aging effects. Results show that the precision of the proposed sensor is about 2.7 higher, with almost 33% less area overhead compared with state-of-the-art aging sensors. Furthermore, the presented sensor can detect and correct 50% of the Single Event Upsets (SEUs), which lead to a bit-flip in the flip-flops. Besides, the SEU detection circuitry can reduce Bias Temperature Instability (BTI) by balancing the duty cycle of the flip-flop with negligible extra overhead.

Pachito et al. [45] propose an aging-aware power supply or frequency reconfiguration approach that uses global and local sensors. Global sensors perform periodic or on-demand delay monitoring, while local sensors predict errors locally. Both allow adjusting frequency or power supply voltage. Results show that performance and power can be improved by, respectively, increasing the frequency and reducing the voltage while still preventing errors. In other work, Semio et al. [46], [47] propose improvements in the global and local sensors cited previously. The global sensor was improved to detect Negative-bias temperature instability (NBTI) and Positive-bias temperature instability (PBTI), while the local sensor was improved to tolerate delay-faults.

Cho et al. [48] examine the effectiveness of the aging-aware Adaptive Voltage Scaling (AVS) for logic circuit blocks using a Tunable Replica Circuit (TRC) aging monitors. The TRC is calibrated off-line, based on the critical paths and on-line monitoring of the operational conditions of the circuit, as temperature variations. The Power Management Unit (PMU) communicates with the TRC periodically. The PMU tunes the Voltage Regulator Module (VRM) when the TRC detects an aging delay degradation until the TRC detects the correct behavior based on the clock. Simulation results in a 22 nm High-K/Metal-Gate Tri-Gate CMOS process show a 7% power reduction with the removal of the guard-bands of a conventional fixed $V_{cc}$. 
Ding et al. [49] propose a delay amplified digital (DAD) aging sensor circuit composed of a delay sensor and a signal amplification circuit. It uses a reference delay circuit designed according to the monitored combinational logic circuit. The delay sensor is used to detect aging effects, while a timing multiplier circuit eliminates the effects on the environment, improving the aging sensor data accuracy. A digital sample module uses nine T flip-flops to count the number of falling-edge during the amplified enable pulse. Using the parameters of TSMC 65 nm CMOS technology, the DAD sensor circuit is designed and simulated using SPECTRE.

Li and Seok [50] propose a technique to pipeline circuits that enables accurate of aging monitoring even under environmental variations. The technique scales the supply voltage for a temperature-insensitive delay and reconfigures the target paths into ring oscillators. The oscillation periods are measured and compared to pre-aging measurements to estimate the delay degradation caused by aging. Also, the technique presents a new register implementation, that has an area overhead of 12 transistors when compared to a standard flip-flop, and a relatively low delay overhead, once it adds a small amount of load between the path from input to output. The technique adds a feedback network between the input and output registers of target paths, which can present a small portion of the total oscillation period, making little impact on monitoring accuracy. The area overhead of feedback network can be minimized by sharing feedback paths among multiple target paths, as like the counter. The counter is used to measure the periods of the ring oscillator operation. Results show that the technique achieves highly-accurate monitoring with an error of 15.5% across the temperature variations in self-test phases from 0°C to 80°C, exhibiting more than 30 times improvement in accuracy as compared to the conventional technique operating at the nominal supply voltage.

Jang et al. [51] propose a aging sensor that detects failures caused by BTI and HCI. This aging sensor is based on timing warning windows to detect a guardband violation of sequential circuits and generates a warning right before circuit failures occur. It monitors the moment when the critical path delays of the logic exceed a standard value, which guarantees a correct circuit operation. The aging sensor is composed by: i) a guardband generator; ii) a path delay monitor; iii) a hold circuit; iv) a signal that controls the aging sensor. The circuit was implemented in 110 nm, and results show that the aging sensor achieves a good aging failure prediction with low overhead.

Table VI summarizes the reviewed path delay monitors. Most of the monitors use delay elements and comparison mechanism to detect timing errors. Also, most of the approaches monitor just the critical paths without monitoring other system elements.

C. Clock Frequency Monitors

Aging can affect clock frequency and decreases system performance. Thus, clock frequency monitoring is a way to detect aging in a design.

Wang et al. [52] present a sensor for reliability analysis of digital circuits using standard-cells called Radic. The Authors also propose a low-cost built-in aging adaption system based on the Radic sensor to perform in-field aging adaption. Radic allows frequency, aging, and metastability measurements. Also, the sensor is designed to obtain the frequency difference between the waveform under test and a reference frequency by measuring how much clock cycles the wave under test is faster or slower than the reference frequency. A stable external source such as automatic test equipment, or a waveform generator, or an internal source such as a phase-locked loop (PLL) can generate the reference frequency. An m-bit timer stores the length of the measurement window by counting the number of clock cycles of the reference frequency. The Radic-based aging monitor system is inserted into a Freescale IP and an ITC’99 b19 benchmark. Results show that the system reduces the fixed aging guardband by 80%. A comparison between the original design and the design with the proposed adaption system shows an area reduction of about 1.02% to 3.16% in most cases. Power is also reduced, as the design can be synthesized using smaller drive strength.

Kfloglu et al. [53] propose an aging sensor based on RO that uses two identical aging paths. Both paths can be either equally sensitive to BTI or modulated to be more sensitive to aging effects. Using DC biased with opposite polarity inputs, both paths have the PBTI and NBTI effects stressed alternatively at every other stage. Unlike a conventional RO based aging sensor, a control loop logic links all stressed devices into one measuring RO loop which its output is the frequency degraded due to the aging. Also, the control loop logic links all non-stressed devices are linked into a second RO loop, which the output is the reference frequency. The frequency delta between aging frequency and reference frequency is used to monitors aging.
D. Circuit State and Workload Monitors

It is possible to detect aging by monitoring the whole system instead of just critical paths. The circuit state and its workload are metrics that can be monitored and provide insightful information. For example, they can indicate stress levels that will increase the aging effects impact.

Koneru et al. [54] reuse the design for testability (DfT – Definition 6) infrastructure to perform a fine-grain workload-induced stress monitoring for accurate aging prediction. A multiple-input signature register (MISR) is used to capture the workload effect on the circuit. An aging prediction software, based on support vector machine (SVM) learning technique, performs aging mitigation. The DfT controller, implemented as a finite-state machine (FSM), periodically switches the circuit into scan mode to capture the circuit state. After capturing the state, the contents of the scan chains are then shifted out to the MISR. The scan-chains are modified to keep its value during the aging monitoring phase, which overwrites the state of the flip-flops and not allow the circuit to return to normal operation until completing the shift to MISR. The Authors conducted experiments on two open-source processor benchmarks, namely OpenRISC 1200 and Leon3, and on four ISCAS’89 benchmarks, to evaluate the accuracy of the proposed technique. Simulation results show that the proposed approach can accurately predict workload-induced aging trends. In a similar work, Firouzi et al. [55] reuse the BIST structure to predict the fine-grained circuit-delay degradation with minimal area and performance overhead and high accuracy.

Khan and Kundu [56] propose a system-level reliability management scheme (SRM) that dynamically adjusts the operating frequency and supply voltage according to the system aging. The proposal allows continuous runtime adjustments based on parameters such as actual room temperature and power supply tolerance. The SRM communicates with the voltage and frequency control registers to enable frequency and voltage reconfiguration. It is implemented in software and assumes a Virtual Machine Monitor (VMM) running underneath the OS software stack, which is primarily used to enter and exit the SRM. The SRM software enables carefully crafted functional stress tests or built-in self-test control to identify degradation at a component granularity and provides adjustments for sustained performance levels at the target reliability. The software allows the system to adapt to the aging effects and invokes aging device management at determined periods. The results show that the device can operate near
peak frequency throughout product life. Also, the approach ensures protection against failure due to insufficient lifetime guardband and no system downtime or change.

Sadi et al. [57] presents a framework for designing lifetime-reliable system-on-chip (SoC) with reconfiguration capability to deal with aging effects. The proposed flow uses a BIST (Definition 7), and a machine learning linear regression predictor software to activate aging countermeasures. The aging status of the chip is monitored at regular intervals by the BIST hardware. Based on the observations, proactive adaptation methods are taken to counteract the reliability degradation effect. The framework allows testing patterns from SoC’s existing BIST hardware, collect the response, and tune the linear regression software. A gate-overlap and path-delay-aware algorithm selects a minimum set of patterns, which activate the target paths used as features of the linear regression predictor. The seeds of the selected patterns are stored in on-chip memory and applied at the BIST hardware at multiple test clock frequencies when required. The corresponding responses of these patterns are collected in a separate response storage flip-flop chain. The software-implemented machine learning classifier is trained with the collected multiple-frequency responses, and the trained predictor accurately predicts the state of aging degradation at runtime. The paths to be monitored by the BIST hardware are selected at the design time based on timing analysis. The adaptive methods used in this approach are frequency scaling, voltage scaling, and adaptive body biasing. Simulation results show that the proposed technique allows accurate and fine-grained in-field aging prediction, with a precision that can reach 94%.

Baranowski et al. [58] present a method for aging rate prediction, which is based on workload monitoring and linear regression machine learning technique. The monitoring technique enables the on-line prediction of the degradation rate caused by the currently running application. The degradation rate monitoring system is composed of a workload monitor and a temperature sensor. The linear regression machine learning technique is used to find the representative critical gates that are monitored. Results show that this method delivers sufficient accuracy at an area overhead of 4.2%, which decreases with the size of the monitored circuit.

E. Voltage Monitors

Circuit voltage can also be use to monitor aging effects. Similar to what happens in clock frequency variations, as the circuit ages, negative effects will be observed, such as timing errors and path delay extension.

Narang and Srivastava [59] propose an approach that uses an inverter chain and counter-based technique to detect the variation in the threshold voltage. A voltage sensing methodology is used to monitor the circuit’s voltage variation. This variation can be fed to an Adaptive Body Bias (ABB) circuit to mitigate the effects of NBTI. The approach uses a counter to determine the total path delay. The path delay feeds an inverter connected to an amplifier. The amplifier output pass trough a voltage to current converter, which feeds a logarithmic amplifier. The output of this logarithmic amplifier feeds an exponential function generator that passes through a subtractor circuit that is used to detect a change in the threshold voltage due to the NBTI effect. The circuit was validated in a set of circuits such as 32-bit OR gate, 64-input OR gate, and 32-bit comparator in 32 nm technology. The simulation results show that this methodology is efficient as it reduces the delay to a large extent with minimal increase in power.

Xiaojin et al. [60] propose a digital on-chip detector that uses the circuit output voltage phase to detect aging. The approach consists of duplicating the circuit, generating two circuits: a reference circuit and an aging stressed circuit. The output of both is compared using an XNOR gate. If a pulse occurs in the XNOR output, aging is detected. Also, the XNOR output pass trough time to digital converter to facilitate the circuit state analyses and verification. The authors claim that the aging detecting circuit can be applied in adaptive systems to mitigate the aging, but do not present a solution in this work. The validation was made by a chip implementation and by simulation. The chip demonstrates results close to the simulated regarding aging time.

VII. Conclusion

This Section concludes the aging monitors and reconfiguration techniques survey, providing insights for future research and development. Table VII presents the implementation methods.

Most of the literature contributions are in the digital area, specifically using hardware solutions for monitoring aging in circuits. Few works use software approaches for aging monitoring. Most software applications act on reconfiguring the circuit after aging detection. We observed works using learning methods (software) for taking proactive actions, detecting events related to aging before they occur. These learning-based methods can point out
We believe that solutions based on system-wide monitoring parameters such as temperature, voltage, and frequency will be more prevalent once they do not depend on a specific parameter. Summarizing, current techniques heavily rely on timing error monitors for detecting aging and use voltage scaling to compensate the effects in integrated circuits. We believe that new solutions are required due to the fact that as technology nodes advance, it becomes harder to identify critical paths of a circuit. This limitation not only makes the task of defining where to place timing error monitors more challenging, but can also require an increase in the number of monitors, inducing larger area and power overheads. Furthermore, with the availability of different sensors, such as frequency and temperature, in industrial SoCs, we believe there is a gap to be filled in aging detection algorithms. Especially with emerging artificial intelligence capabilities, algorithms can analyze the data of the available sensors and configure the SoC to counter aging effects.

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