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Abstract: We investigate the monolithic integration of RF antennas onto a silicon-based integrated microwave photonics (IMWP) chip for short-range millimeter-wave (mmW) communication. The unification of antenna with photonics integrated circuits (PICs) reduces system loss for high data rate communication by eliminating parasitic interconnects. This integration of electronics (antenna) with photonics will be a key milestone leading to increased bandwidth capability and ubiquitous wireless links for emerging applications such as 5G, Internet of Things (IoT), autonomous vehicles, high data rate point-to-point communication, and wireless sensors. Through simulation above 20 GHz, we compare the transmission of three on-chip antenna structures designed in a commercial silicon photonics (SiPh) process and consider them for both inter and intra-chip communication. Results provide insight on the transmission gain variations relative to the antenna orientation from their distinct radiation pattern. The folded monopole structure provides superior gain, smaller footprint with layout flexibility, and good transmission spectrum. The analysis supports the idea of a monolithic mmW transmitter integrated with on-chip antennas on IMWP chip.

Index Terms: Integrated microwave photonics, photonics integrated circuits, antenna-on-chip, optical beamforming, silicon photonics, millimeter wave.

1. Introduction

The unparalleled surge in wireless data traffic witnessed over the last decade along with the rise of disruptive technologies such as 5G, autonomous vehicles, IoT, and virtual reality has compelled researchers to look for ways to increase wireless data rates. This insatiable demand for data has mobilized research effort towards using spectrum rich millimeter-wave (mmW) frequency bands [1]. Wireless communication at high frequencies leads to superior data rates [2]. The staggering wide spectrum (nearly 20 GHz) availability at mmW frequency bands is revolutionary in terms of delivering high-speed data communication considering that all of the world’s cellphone currently operate in less than 1 GHz of allocated spectrum [3]. Thus, there is strong impetus towards developing mmW wireless communication systems driven by the need for spectrum availability, increased bandwidth capability, and high data rate among other motivations.
To reap the real benefits of mmW communications, integration is essential as it reduces size, weight, and power budgets. Fig. 1(a) depicts the schematic of an electronics integrated circuit (EIC) based mmW beamforming system transmitting in one direction considering transmitter generated pulse arriving at the same time at the antenna elements. Introducing time delays in the feed tilts the transmitted pulse (Fig. 1(b)) allowing to steer the beam in the desired direction. Small wavelength at mmW frequencies allows for compact implementation of large number of antennas to synthesize highly spatial beam with high gain. The performance of these antenna arrays is strongly influenced by the beamforming network that connects the antennas with the transmitter or receiver [4]. Though mmW signal suffer from higher attenuation owing to free space path loss, diffraction and atmospheric conditions, the phased array antenna (PAA) with beamforming capacity neutralizes this propagation loss by spatial focusing [3], [5]. The path loss characteristics at mmW frequencies is equivalent to those at conventional cellular frequency bands if transmitting and receiving antennas are used to produce array gain [5].

Significant breakthroughs in electronic mmW systems have occurred in areas of communications [6], remote sensing [7], and sensors [8]. Despite this, the EIC approach for mmW beamforming and beam steering has severe drawbacks such as bandwidth limitation, large propagation loss, limited tunability, weak electromagnetic interference (EMI) immunity, and distortion [4], [9]. The two types of EIC based mmW beamforming and beam steering approaches are: 1) classical phase shifter [10], [11], which although efficient for narrow band PAA systems, have large insertion loss and beam squint phenomena at wider bandwidth operation [12]; 2) True time delay (TTD) [12], [13] approach, which overcomes bandwidth and distortion limitations, but alternatively suffers from frequency dependent insertion loss and inefficient scaling leading to increased power and chip real estate [4]. Using amplifiers to address this insertion loss problem leads to higher power consumption and system non-linearity. Although, all these problems are not unmanageable, the overheads in terms of development cost and complexity are significant.

A promising way to alleviate these fundamental limitations in electronic mmW systems is to adopt Microwave Photonics (MWP) [14]–[16], a discipline that combines RF engineering and optoelectronics. MWP shifts the signal generation, processing, distribution, and remote antenna tasks from radio domain to photonic domain, thereby accessing abundant bandwidth and ultra-low attenuation. Moreover, the loss is almost frequency independent. The photonics TTD beamforming allows for ultra-wide instantaneous bandwidth, delay tunability, EMI immunity, high frequency operation, and capability to scale for large arrays without beam squint problem [4]. A typical MWP system includes a modulator for electrical-to-optical (E/O) conversion, a photodetector converting signal from the optical to the electrical (O/E) domain, and an optical processing unit in between. The MWP beamforming system (Fig. 2(a)) replaces the electronic beamformer (Fig. 1(b)) with optical beamforming network along with E/O and O/E convertors. The bandwidth of MWP technique is limited only by the electro-optic modulator and photodetector.

The tremendous potential of conventional MWP and its widespread use in emerging technologies is limited by its cost, reliability issues, and size due to utilization of discrete components [17]. The ongoing parallel advancements in photonic integrated circuits (PICs) [18]–[20] helps MWP...
build monolithic systems with reduced footprint, cost, and inter-element coupling losses. This convergence of PICs and MWP into integrated microwave photonics (IMWP) [17], [21] is a natural and obvious step forward for implementing monolithic photonics solutions, as IMWP miniaturization and ultra-bandwidth characteristics make their use economical viable. A number of IMWP based functionalities have been demonstrated in [17], [21], [22]. Monolithic implementation of photonic front-end combining optical true time delay (OTTD) beamforming, photodetector, and antenna array is one of the ultimate challenges for IMWP designers and motivation of this paper. Fig. 2(b) shows the block diagram representation of such system. An attractive application of such monolithic system (Fig. 2(b)) is short-range chip to chip/module to module high-speed wireless interconnection in a portable device. Another envisioned application includes range extension of wireless personal area networks (WPAN) and last mile access solutions [23].

The on-chip unification of photonics and RF wireless components is a significant step in the continuous effort of system designers to extend the advantages of silicon integration to higher frequencies. An antenna integrated into an IMWP chip will reduce electrical power loss by averting the frequency dependent off-chip parasitic interconnects between the photodetector and the antenna. In addition, the on-chip antenna will eliminate the need for a matching network to transform the system impedance to 50 Ω [24]. Therefore, antenna impedance becomes one of the design parameters that further provides design flexibility. In addition, the frequency independent TTD approach coupled with miniaturized optical components in IMWP allows for a natural tuning of array parameters towards high frequency beamforming for next-generation architectures [4]. Development of a complete Si-based IMWP wireless front-ends (with on-chip antenna) will lead to breakthrough application of integrated photonics in next-generation technologies like 5G, wireless sensors, airborne and autonomous vehicles, short reach high frequency communication, and in-house broadband communication. Previously, we demonstrated a proof of concept 15 GHz monopole on-chip antenna design in a commercial silicon photonics (SiPh) process [25].

In this work, we propose a monolithic integration of an optical beamforming network, photodetector, and antenna array in a silicon-based IMWP chip. Section 2 presents a brief overview and comparison of the optical beamforming networks to be used in the envisioned short-range mmW IMWP transmitter. The section ends with the power budget analysis of three popular beamforming techniques with respect to the proposed IMWP chip. In Section 3, prominent antenna-on-chip (AoC) configurations found in the research literature are discussed followed by the detailed design, simulation, and analysis of three proposed on-chip antenna topologies on the SiPh platform. Subsequently, a comprehensive simulation of inter-chip and intra-chip communication is presented for all three designed AoC topologies. Finally, Section 4 concludes the paper.

2. Proposed IMWP mmW Transmitter

2.1 Integrated Optical Beamforming Overview

In general, integrated optical beamforming network can be realized using 1) OTTD or 2) phase shift (PS) approach. Being frequency dependent, optical PS approach is not immune to distortion
in broadband communication, but it exhibits tolerance to beam squint effect as long as fractional bandwidth of the transmitted signal is small, the scanning angle is small, and the number of antenna array elements is not too high. Also, PS has the merit of more straightforward implementation [26].

On the other hand, integrated optical beamforming network based on OTTD completely mitigates the beam squint effect and offers scalability by allowing more array elements [4], [26]. OTTD eliminates the bandwidth constraint by providing frequency independent time delay between the antenna elements [4]. Thus far, several integrated OTTD schemes have been implemented based on photonic crystals waveguides [27], [28], waveguide Bragg grating [29], [30], Blass matrix based optical switches [31], switchable waveguide delay matrices [32], [33], optical ring resonators (ORR) [34], [35], and arrayed waveguide grating (AWG) [36], [37]. Out of these, switchable waveguide delay and ORR are suited for monolithic implementation on silicon on an insulator (SOI) platform; therefore they have been aggressively researched in the last decade. The switchable waveguide delay based integrated OTTD approach induces delay by changing the path length. It utilizes switch elements connected between waveguides with varying length, where the optical path is selected by changing the state of the switches. Such integrated OTTDs have merits of reconfigurability, broadband performance, and fabrication robustness besides discrete delay tuning [32]. The achievable delay is proportional to the waveguide length and limited by waveguide loss and the device size. The length difference of the waveguide dictates the resolution. In general, they exhibit a tradeoff between beam angle resolution and complexity. In integrated AWG feedback loop with loopback delay lines of varying length in between, the optical delay line becomes wavelength selective [36], [37]. Here, the wavelength tuning of optical carrier results in the path (and therefore delay) selection. The unique advantages of AWG loops are 1) footprint reduction 2) fabrication tolerance 3) remote tuning of optical delays with wavelength and 4) low insertion loss [36].

The second scheme based on ORR provides an extremely compact and effective implementation of continuous tunable group delay. However, single ORR suffers from the narrow bandwidth owing to fixed delay bandwidth product. The bandwidth can be enhanced by cascading multiple ORRs but with the sacrifice of chip real estate and complex trimming. Therefore, an inherent tradeoff exists between bandwidth, delay response flatness, delay tuning range, and the total number of rings [35]. A combination of ORR and switchable waveguide delay lines have also been realized showcasing large delays and continuous tuning capability [38]. Table 1 compares the performance of the switchable, ORR and AWG based integrated optical beamformer networks.

### 2.2 Power Budget for the Proposed IMWP Transmitter

A conceptual integrated SiPh based mmW beamforming transmitter chip including photodetector and antenna elements is shown in Fig. 3. The optical carrier, modulated by the RF signal is fed to the IMWP chip, which includes beamforming network, photodetector (PD) and antenna array. Mach-Zehnder modulator (MZM) is preferred for modulation for its large modulation bandwidth, low
driving voltage, and low chirp. The grating coupler based coupling loss at the interface of the chip for channeling light into the chip is considered to be 3.1 dB [39]. The insertion loss associated with ORR utilizing 1 x 4 beamformer network (illustrated using simplified diagram in Fig. 3(a)) is reported to be 9.2 dB [34]. The ORR based beamforming network can be generalized to larger structures, for example 1 x 8 and 1 x 16, where the total number of rings depends on 1) the required delay tuning range per delay element 2) the required delay ripple (corresponding phase response accuracy) and the optical bandwidth. However, increasing the number of rings adds to the tuning complexity of the structure. Recently demonstrated Mach-Zehnder interferometer (MZI) based switchable waveguide delay line for photonic beamforming network exhibits \(\sim 0.38 \text{ dB}\) insertion loss for an MZI switch [33]. Considering three switches in each delay line (diagrammatically represented in the Fig. 3(b)), the total loss in each delay line is 1.14 dB. Taking into account the 1 x 4 power splitter and waveguide propagation loss, the average total insertion loss for an optical delay line is \(\sim 10 \text{ dB}\). Similarly, Fig. 3(c) depicts the proposed beamforming network based on AWG-loop. As shown in Fig. 3(d), the 4 x 4 symmetric AWG is used as both wavelength multiplexer and demultiplexer. The shown structure is topologically equivalent to two AWGs in series with a delay element in between. For the power analysis, the insertion loss of an AWG-loop is taken as \(\sim 4 \text{ dB}\) [36], [37], with 2.5 dB loss due to the demultiplexer [40], accounting for total insertion loss of the beamformer network of \(\sim 6.5\) excluding coupling loss. Taking into account the input laser power of 16 dBm, the input coupling loss of 3.1 dB, the total MZM loss of 9 dB [41], the EDFA gain of 13 dB, propagation losses and the insertion loss of the different beamforming arrangement, the power budget is shown in Table 2.
TABLE 2

Optical Power Budget

| Parameter                                      | Optical Power     |
|------------------------------------------------|-------------------|
| Laser [dBm]                                    | 16                |
| MZM and Modulation loss [dB]                   | −9                |
| EDFA gain [dB]                                 | 13                |
| Propagation loss between EDFA and SiPh chip [dB] | −6                |
| Coupling loss (Vertical fiber to grating coupler) [dB] | −3.1              |
| Beamformer network loss [dB]                   | ORR, Switchable, AWG |
| Input power at PD [dBm]                        | ORR, Switchable, AWG |
| Estimated PD sensitivity (for antenna gain of -1 dBi and antenna separation of 0.5 cm) [dBm] | −5.22          |
| Power margin [dB]                              | ORR, 6.92 Switchable, 6.12 AWG, 9.62 |

For a bit-error-rate (BER) of $10^{-12}$, the electrical signal-to-noise ratio (SNR) required is 23 dB [42]. Considering an electrical noise floor of -61 dBm, the received signal power should be $−38$ dBm. The noise floor is calculated using the (1) shown below for a bandwidth (B) of 1 GHz, Boltzmann’s constant ($k = 1.38 \times 10^{-23}$ Joules/K), temperature ($T = 300$ Kelvin), and equivalent resistance ($r = 50$ Ω).

$$P_n \text{ (dBm)} = 10 \log_{10} \left( 4kTB r \right) + 30 \quad (1)$$

Using the Friis transmission formula below, the estimated transmitted power can be calculated as below:

$$P_t = \frac{P_r G_t G_r \lambda^2}{(4\pi S)^2} \quad (2)$$

Here, $P_t$ is the average RF power at the receiving antenna in units of dBm. $P_r$ is the average RF power of the transmitting antenna in dBm. $G_t$ is the transmitting antenna gain in dBi. $G_r$ is the receiving antenna gain in dBi. $\lambda$ is the wavelength of the transmitted RF signal in meters. Finally, $S$ is the distance between the antennas in meters. The average optical power at the input of the on-chip SiPh photodetector, $P_{opt}$, in units of Watts (W) relates to the electrical RF power at the input of the antenna, $P_{ei}$, in units of Watts through the responsivity, $R$, in units of A/W, and the antenna impedance, $Z$, in Ohms at DC following this equation,

$$P_{opt} = \frac{1}{R} \cdot \sqrt{\frac{P_{ei}}{Z}} \quad (3)$$

We assumed a responsivity $R$ of 1.09 A/W for a SiPh PD exhibiting bandwidth of 42.5 GHz [43]. For an RF signal with a frequency of 22 GHz transmitted over a distance $S$ of 0.5 cm and using (3) in conjunction with the (2), the required transmitted RF power and gain of the antenna is $−23$ dBm and $−1$ dBi, respectively, considering received RF signal of $−38$ dBm and a PD sensitivity of $−5.22$ dBm. Here, PD sensitivity corresponds to the minimum signal power required at the input.
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Fig. 4. Power margin for the ORR, switch-based, and AWG beamformer network along with the required transmitter/receiver antenna gain versus the PD sensitivity.

of the PD for a BER of $10^{-12}$. The analysis shown here assumes an impedance matching between PD and antenna.

The corresponding power margins for each proposed beamforming network are as indicated in Table 2. The antenna gain value calculated is aligned with the gain values obtained in the investigation discussed in the next section. The simulated gain values for all three antenna structures are better than $-1$ dBi.

Relative to the envisioned systems in Fig. 3, the calculation shown in Table 2 considers single on-chip antenna system at the transmitter and receiver side. Antenna array beamforming systems increase the directivity and gain, thereby further improving the minimum detectable signal. With further simplification in the beamforming design, losses can be reduced leading to an efficient complete IMWP chip with better power margins.

Assuming an antenna separation of 0.5 cm, the required gain for transmitter and receiver antennas and power margin of the three beamforming network configurations are plotted with respect to PD sensitivity values in Fig. 4. Assuming a given antenna separation and considering (2) and (3), both PD sensitivity and antenna gains are interdependent. When computing one, we assume the other appropriately to satisfy power margins. For the PD-antenna integration in SiPh, important consideration includes area, gain, data rate, responsivity, and optical power needed for transmission. The data rate is limited by the bandwidth of the PD and the antenna. Optimizing on-chip peaking inductor can extend the bandwidth and responsivity of the PD [43]. Antenna bandwidth can be increased by using high frequency of operation and by using wider band structures.

3. On-Chip Antennas in Si Photonics

3.1 Antenna On-Chip Overview

The monolithic inclusion of antenna with other on-chip components on a conventional RF front-end design has been a lingering issue since the last two decades [24]. This ultimate goal allows for the realization of reliable, cost-effective, and low profile wireless front-end modules. On-chip antenna topologies for inter-chip and intra-chip communications have been investigated in [24], [44], [45]. In 2002, [46] demonstrated the intra-chip wireless communication between an integrated transmitter and receiver via on-chip dipole antennas. Following this, the authors in [47]–[49]...
investigated the feasibility of inter-chip wireless transmission among on-chip metallic antennas in various arrangements such as zigzag, meander, loop, and dipole. Further, [50] reported radiation characteristics of interesting antenna topologies like an inverted-F and a quasi-Yagi. In [51], [52], the authors studied the intra-chip propagation mechanism for wireless chip area network and concluded that the surface waves were dominant propagation mechanism rather than the space wave over intra-chip channels. In [53], Zhang et al. also showed the bit error rate analysis of integrated antennas. Besides the above-mentioned seminal papers, in-depth reviews journals [24], [54] serve as excellent sources of scholarship by highlighting potentials, challenges, future directions, and applications of up to date on-chip antenna research.

Though emerging mmW frequencies affords highly integrable antenna on-chip (AoC) solutions, the resulting AoC structures suffer from poor radiation efficiency and low gain [24], [55]. This is due to the low resistive Si substrate used in some complementary metal-oxide-semiconductor (CMOS) technology processes that lead to high losses [56]. Further, at mmW frequencies, bulk silicon is electrically thick leading AoC to couple significant power into surface modes in the silicon rather than through free space [57]. Therefore, it is difficult to match AoC performance with off-chip antennas since the latter exhibits higher bandwidth, efficiency, and directivity [24], [55]. Other solutions such as micromachining [58], Si lens [24], ground planes [24], dummy metal tiling [59], and artificial magnetic conductors (AMC) [24] are useful to some extent but makes the AoC design complex and costly besides creating new limitations. SiPh with high substrate resistivity allows for improved efficiency and gain for AoC as well as leading to a less complex design.

3.2 Antenna Design

SiPh compatibility with conventional CMOS foundry process makes it suitable for many applications. The targeted AoC in SiPh must provide superior gain, efficiency, and smaller chip real estate. Out of many antenna designs studied and investigated [3], [24], [44], we choose three AoC configurations namely the Meander monopole, the Folded monopole, and the Quasi-Yagi. We selected the meander monopole antenna for its small footprint and omnidirectional radiation pattern. The omnidirectional pattern is advantageous for intra-chip communication where efficient transmission is needed in various directions on the chip instead of a specific direction. The folded monopole is quite flexible in placement having a low profile, and is relatively simple to design and fabricate, while the quasi-Yagi is chosen for its directivity at the cost of larger antenna size. Other popular antenna structures include loop, slot, and microstrip, but they were not considered due to large size, multi-metal layer requirement, and the complexity.

The fabrication layer stack for a conventional SiPh process is shown in Fig. 5(a). The unavailability of multiple metal layers in the conventional SiPh process inhibits the development of complex antenna topologies. These constraints played a key role in selecting the antenna topologies. The AoC structures discussed in this paper were designed and optimized using ANSYS High Frequency Structure Simulator (HFSS). For a fair comparison of antenna performance, the three antennas are simulated using the same SiPh chip area. The predominant research in mmW has been carried at 24 GHz and 60 GHz frequency bands. Also, in 2019, the International Telecommunication Union's (ITU) has identified 24 GHz for terrestrial 5G [60]. As such, the antenna resonant frequency in this research is set close to 24 GHz. Specifically, it is set at 22 GHz due to superior simulated antenna parameters for the given chip area. Though mmW frequency starts at 30 GHz, with some researchers considering 24 GHz as mmW, the behavior and general consideration for 22 GHz is sufficiently close to 24 GHz to be considered in that category for the purpose of our discussion.

3.2.1 Meander Monopole Antenna: The layout of the meander monopole antenna in a standard SiPh process (Fig. 5(a)) with corresponding dimensions is shown in Fig. 5(b). At the input side of the meander monopole, a ground plane is included (shown in Fig. 5(b) in black). The envisioned interconnection scheme of antennas, PD and beamforming network is also shown in Fig. 5(b) inset. The simulation discussed here considers the antenna structure only without PD and beamforming network. The antenna is housed on a chip with length, width, and the coordinate axis as represented in Fig. 5(c). The meandering structure is formed by continuous periodic
Fig. 5. (a) A typical SiPh SOI process layer stack with layer description and an aluminum metal layer (M1) on top (b) Structural view of the meander monopole antenna with detailed dimensions along with an intended integration with PD and beamforming network as shown in the inset (c) Die area of the meander antenna layout with length and width (d) Simulated $S_{11}$ characteristics with resonance of greater than 20 dB. (e) Simulated antenna gain and radiation pattern.

Folding of the single metal (aluminum) layer with a thickness of 500 nm lying 2.2 μm over the buried oxide (Box). Thus, the layout results in lower resonance frequency compared to a straight monopole with same longitudinal length since meandering structure would lead to larger effective antenna length. The larger antenna length corresponds to lower antenna resonance frequency. The meander monopole uniform radiation pattern in the z-y plane and small size compared to the ones by dipole and straight monopole antennas making it compact and suitable for intra-chip wireless communication. The quarter-wave monopole is one half of the size of a dipole antenna and is designed by calculating the antenna length using the effective wavelength, $\lambda_{\text{eff}} = \lambda_0 / \sqrt{\varepsilon_r}$, where $\lambda_0$ is the resonance in free space and $\varepsilon_r$ is the relative permittivity of the oxide cladding below the metal layer which is 3.9. With the quarter wavelength obtained using the effective wavelength $\lambda_{\text{eff}}$, the resonance is optimized by varying the longitudinal length of the antenna. The meandering is then done for a more compact footprint. Further, the antenna structure is optimized for gain and a strong resonance at 22 GHz by tuning the length, pitch, and width of the antenna as per the design methodology reported in [61]. The resulting resonance ($S_{11}$) is $-24$ dB (Fig. 5(d)) at 22 GHz and the simulated gain obtained is $-0.80$ dBi (Fig. 5(e)). The antenna exhibits a typical radiation pattern behavior as expected from a monopole antenna with minimal gain along the axis (x-axis) and maximum gain orthogonal (y and z) to antenna axis.

3.2.2 Folded Monopole Antenna: The second antenna with its structural dimensions is illustrated in Fig. 6(a). Its footprint is slightly larger than the meander antenna discussed above. The antenna sits on a chip with an overall area of 3 mm × 4 mm and corresponding coordinate axis shown in Fig. 6(b). The antenna performance is optimized by varying the length, width and spacing of the antenna arms. This antenna has a resonance ($S_{11}$) value of $-12$ dB (Fig. 6(c)) inferior to the meander antenna. Folded monopole unique flexibility in terms of placement and directed radiation pattern (shown in Fig. 6(d)) makes it useful for directional communication for inter-chip
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Fig. 6. (a) Top view (X-Y plane) of the folded monopole layout with structural dimensions. (b) Chip length, width, and coordinate axis description along with antenna layout. (c) Simulated $S_{11}$ response of folded monopole AoC showing resonance better than 10 dB d) Antenna gain and radiation pattern representation.

and intra-chip environments. Its simulated gain is 1.29 dBi, better than mender monopole and quasi-Yagi antenna.

3.2.3 Quasi Yagi Antenna: Planar Yagi antenna is one of the popular configurations in antenna theory due to its suitability for a wide range of applications such as imaging arrays, phased arrays, and wireless communication systems. Here, we use a quasi-Yagi antenna with a simple CPW feed, thereby, alleviating the complicated feeding network [62]. The complete skeleton of the proposed antenna with chip dimensions and cross-section are illustrated in Fig. 7(a) and 7(b). The quasi-Yagi occupies a significant footprint compared to the meander and the folded monopole antennas. As illustrated in Fig. 7(b), this antenna consists of one director element for focusing the beam, a driver element, and a ground plane acting as a reflector. The starting point of designing this antenna involves setting the length of the driver element to be approximately half of $\lambda_{eff}$ and the length of the director to be in the order of 0.45 $\lambda_{eff}$ as per [63]. The distance between the director and driver should be kept between 0.1 and 0.2 $\lambda_{eff}$. After simulating the antenna using ANSYS HFFS based on the full-wave finite element method, the antenna dimensional parameters were optimized for resonance at 22 GHz. The gain was tuned by varying the width of the reflector. Fig. 7(c) shows the resonance behavior of the antenna and Fig. 7(d) exhibits the radiation pattern with gain of the antenna as $-0.40$ dBi.

The distinctive point of the proposed quasi-Yagi antenna is its simplicity of the feeding structure. The resulting resonance is not as broad as expected and gain is also nominal. Further optimization in terms of efficiency, gain and distortion is possible with the inclusion of an AMC or ground plane in the design [64], [59]. Table 3 summarizes the simulation results of the above antenna topologies along with the required PD input power values for simulated antenna gains. The PD input power for each antenna is calculated using (2) and (3) and considering $S$ as 0.5 cm and $R$ as 1.09 A/W.
3.2.4 Challenges in AoC Design: The on-chip antenna environment give rise to unique challenges that adversely affects AoC performance. Most of these problems arise due to the substrate [44]. Firstly, the substrate high permittivity forces antenna to preferentially radiate into the substrate instead of into the air. Secondly, thicker substrate leads to surface modes causing power loss. A substrate thicker than one tenth of a free space wavelength will support substantial surface waves [57]. And finally, design rule check (DRC) issues associated with the metal density, metal via design, and metal thickness shifts the performance parameters of the design [24]. In addition, the fabrication process variations leading to changes in resistivity, layer thickness, and height change antenna performance.

### TABLE 3
Summary of Antenna Results

| Parameter                        | Meander monopole | Folded monopole | Quasi-Yagi |
|----------------------------------|------------------|-----------------|------------|
| S11 resonance (at 22 GHz)       | -24              | -11.5           | -19        |
| Antenna Gain (dBi)               | -0.80            | 1.29            | -0.40      |
| Required input power at PD (dBm)| -5.3             | -7.52           | -5.83      |
3.3 Inter-Chip Communication

Inter-chip communication, typically undertaken for a distance range starting from 5 mm [65] is investigated using the arrangement of the on-chip antennas illustrated in Fig. 8, where \( S \) is the separation distance in mm between the antennas. Fig. 8(a), 8(b), and 8(c) show the relative placement of the meander, folded monopole, and quasi-Yagi antenna chips for inter-chip simulation using HFSS. The structural dimensions of the chips are the same as discussed in the previous subsections. Note that all on-chip antennas are placed in the far field of each other. The far-field boundary starts from the distance of \( 2D^2/\lambda_{\text{eff}} \) [66], where \( D \) is the maximum antenna length and \( \lambda_{\text{eff}} \) is effective wavelength. For meander monopole, at 22 GHz, the far field distance is 1.16 mm (\( \lambda_0 \) at 22 GHz is 13.6 mm which makes \( \lambda_{\text{eff}} \) equals 6.88 mm, thereby giving \( 2D^2/\lambda_{\text{eff}} = 1.16 \text{ mm} \)). In our simulation, the minimum separation of two antennas is set to 3 mm to make sure all antennas are placed in their far field. The resulting simulated transmission coefficient (S21) between the antennas with respect to separation is plotted in Fig. 8(d). From this plot, we see that the performance of the meander monopole and the folded monopole follows the same trend, whereas the quasi-Yagi antenna exhibits inferior performance. During the analysis, the chips were aligned in the direction of maximum gain.

The required transmission coefficient (S21) for the inter-chip communication can be calculated using the following equations:

\[
S_{21} = P_L (dB) + G_t (dB) + G_r (dB)
\]

Where the path loss \( P_L \) is defined as

\[
P_L (dB) = 20 \log \left( \frac{\lambda}{4\pi S} \right)
\]

For PD sensitivity of \(-5.22 \text{ dBm}\), antenna transmission gain \( G_t \) and receiver gain \( G_r \) of \(-1 \text{ dBi}\), and separation \( S \) of 0.5 cm, the required \( S21 \) comes to be \(-15.28 \text{ dB}\).
3.4 Intra-Chip Communication

The rapid advancement in Si-based PICs and their compatibility with the ubiquitous CMOS technology supports research effort towards electric-photonics integration. With frequency spectrum moving up towards mmW range, photonics systems with their abundant bandwidth, low loss, and compatibility with mature and reliable CMOS technology platform makes this co-integration proposition appealing. With increased data rates, the line parasitic becomes significant, thereby limiting the data rates on a wireline between electrical and photonics blocks on the same hybrid chip. One potential flexible and versatile solution is the use of high-speed wireless intra-chip communication between the electrical and photonic module with the help of RF antennas. These intra-chip communication links are generally for distances ranging from 5 to 20 mm. At mmW frequencies, antennas have more bandwidth and smaller size thereby making case for intra-chip communication.

The antenna arrangement for investigating intra-chip communication using meander monopole antenna is depicted in Fig. 9. The chip area for intra-chip communication simulation is increased and taken to be 9 mm × 9 mm to accommodate antenna on every side of the chip. We get valuable insight into the antenna transmission behavior in all directions by adding more than two antennas on the chip. The corresponding separation among antennas on the same chip is shown in Fig. 9(a). All these antennas are in the far field region. Each on-chip antenna is numbered and simulated using HFSS to calculate the transmission coefficients. The corresponding transmission coefficients are plotted in Fig. 9(b). As required, the maximum transmission gain (S31, S32, S21, S24, S41, S34) of meander monopole antenna coincides with its corresponding resonance (S11) dip. Due to the symmetrical arrangement of meander antenna on the chip, the transmission characteristics values (S21, S34) (S31, S24) and (S32, S41) are same as seen from Fig. 9(b). The transmission gain (S31, S24) is better than (S32, S41) and (S21, S34) due to the shape of the radiation pattern,
which is dominant towards the direction orthogonal to the antenna axis. The S-parameter simulation results presented in Fig. 9(b) can further be validated by observing the electric field distribution variation across the chip structure. In Fig. 9(c), the magnitude of the electric field distribution is investigated when only one antenna (Ant 3 in Fig. 9(a)) is excited at 22 GHz. As seen, the lower magnitude of the electric field distribution can be noticed at the position of antenna Ant 4 compared to the electric field magnitude at antennas Ant 1 and Ant 2. This is also observed in the transmission gain $S(34)$ in Fig. 9(b) which is less than $S(31)$ and $S(32)$. The field distribution depends on the antenna’s geometry and the operating frequency, but as well the material used. The maximum transmission gain ($S31, S24$) for the meander monopole antenna is $-12$ dB.

In the same fashion, the intra-chip layout arrangement, S-parameter simulation results, and electric field distribution for folded monopoles are shown in Fig. 10. This type of antenna provides better gain than the meander monopole with transmission value $S(23)$ equals to $-9$ dB. In this intra-chip configuration, transmission gain $S(24)$ and $S(12)$ have the lowest value at the resonance frequency due to their orientation with respect to each other. Fig. 10(c) shows that the electric field magnitude is high at the antennas Ant 1 and Ant 3 when antenna Ant 4 is excited at the resonant frequency while antenna Ant 2 receives lower electric field confirming low values shown by $S(24)$ and $S(12)$. Furthermore, Fig. 10(d) highlights low and high intensity regions on the chip when antenna Ant 2 is excited. Though folded monopole exhibits maximum transmission coefficient, in contrast to meander, all antennas do not show maximum gain at return loss minimum and transmission coefficient varies due to asymmetry in placement.

Same trend is visible in the quasi-Yagi antenna based intra-chip communication presented in Fig. 11(a). The peak transmission gain $S(13)$ in quasi-Yagi case as seen from Fig. 11(b) is $-14$ dB.
Fig. 11. Intra-chip communication configuration using quasi-Yagi antenna with (a) structural information (b) transmission and return loss plot (c) electric filed distribution when only Ant 1 is excited.

and electric field distribution is shown in Fig. 11(c). Lastly, one critical observing point in reference to the folded monopole and quasi-Yagi antenna is that their resonance frequency varies in contrast to the resonance value of same antennas in inter-chip communication. In both theses antennas, during intra-chip communication, $S_{11}$ decreases slightly compared to the $S_{11}$ values of Fig. 6 (c) and 7 (c). This is due to reflections from chip edges and interference phenomenon between multiple signal components [3], [44]. The high transmission gain values observed here from the simulation validate that intra-chip communication is possible. When realizing on-chip arrays, the chip footprint will increase as each array antenna element needs to be at half wavelength distance from the adjacent antenna element. As an estimate for implementing a four-element linear array using meander monopole antenna at 22 GHz, the length of the chip needs to be 11 mm (1.1 cm) and width of approximately 3 mm.

4. Conclusion
We proposed and analyzed three SiPh based on-chip antenna topologies namely the meander, quasi-Yagi, and folded monopole. We considered them to be monolithically integrated with optical TTD beamformer and PD, thereby enabling an optical processing unit capable of generating bandwidth enhanced mmW signal. Simulation results of inter and intra-chip communication attests the superior performance of folded monopole in terms of gain (1.29 dBi) over meander and quasi-Yagi, whereas the meander monopole antenna exhibits best resonance based on the $S_{11}$ return loss below $-20$ dB. The chip footprint of both folded monopole and meander is comparable and better than quasi-Yagi. The symmetrical placement of meander antenna promises efficient intra-chip communication with small variation in transmission characteristics. Feasibility of incorporating on-chip
antenna with OTTD beamforming network on a single chip has been corroborated through optical power budget analysis. This potential monolithic integration of complete IMWP based broadband mmW transmitter chip improves data rate, saves cost and chip area by eliminating parasitic. Thus Si-based IMWP wireless chip will provide effective solution in near future technologies like 5G, airborne and autonomous vehicles, home IoT, and short-reach high frequency wireless communication.

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