Multi-bit MRAM storage cells utilizing serially connected perpendicular magnetic tunnel junctions

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Serial connection of multiple memory cells using perpendicular magnetic tunnel junctions (pMTJ) is proposed as a way to increase magnetic random access memory (MRAM) storage density. Multi-bit storage element is designed using pMTJs fabricated on a single wafer stack, with a serial connections realized using top-to-bottom vias. Tunneling magnetoresistance effect above 130 %, current induced magnetization switching in zero external magnetic field and stability diagram analysis of single, two-bit and three-bit cells are presented together with thermal stability. The proposed design is easy to manufacture and can lead to increase capacity of future MRAM devices.

I. INTRODUCTION

Spin transfer torque magnetoresistive random access memories (STT-MRAM) have numerous advantages over existing storage technologies, including theoretically unlimited endurance, high read and write speeds and ionizing-cosmic-radiation resistance.1,2 However, state-of-the-art memories have limited capacity due to the fact, that current density needed to switch a cell (typically made of a single magnetic tunnel junction) requires relatively large transistors.3 Such an obstacle can be overcome using the architecture that incorporates multibit cell driven by a single transistor.

To date, very few practical implementations of multi-bit MRAM cells have been presented.4,5 This is mainly due to the fact, that efforts were made to produce a single storage element capable of being stable in more than two states, or to produce multiple storage elements on the top of each other.6–8 Both of these approaches are very challenging for the process of manufacture.

In this work an alternative approach is proposed – perpendicular magnetic tunnel junctions (pMTJ) are connected electrically in series and a multi-state behaviour is observed, that leads to a multi-bit storage capability. Theoretical explanation as well as experimental results (including working three-bit cell) are presented. In addition, such an approach can be implemented to design and fabricate an artificial synapse for neuromorphic computing scheme.9–11

II. PRINCIPLES OF OPERATION

The discussed pMTJs consist of a top free layer (FL), MgO tunnel barrier and a bottom reference layer (RL), which is magnetically pinned to the synthetic ferromagnet (SyF). In the proposed serial connection of pMTJs in a storage cell, the top contact of the first element is connected to the bottom contact of the next element (head-to-tail), as shown in the inset of Fig. 1. This results in the charge current flowing through all the cells involved in the same direction. Connections can be made using metallization and vias or any other suitable technique.

The behaviour of the presented arrangement of storage elements can be predicted by analysing characteristics of two pMTJs connected (Fig. 1). If both elements are in the parallel (P) state, the lowest resistance is observed (1). When a positive voltage is applied (which corresponds to the current flow that favours anti-parallel (AP) state), the current increases, until it reaches critical value, which results in the current induced magnetization switching (CIMS) (2). As one of the elements switches to the AP state, with constant voltage applied, the current decreases. This prevents the remaining element of the cell from switching, as the current drops below the critical value. By further increasing the voltage, the critical current is reached again, and the second pMTJ switches to the AP state (3).

By reversing the current polarization, the switching to the P state is achieved. In this case, as soon as the critical current is reached, one of the elements switches to the P state (4). With constant voltage applied, the current rises above the critical value, causing the other element to switch to P state.

The above mechanism works also for more than two elements, and similar reasoning can be carried out. For the serial pMTJs connection utilizing the presented mechanism, \( N + 1 \) stable resistance states would be observed for \( N \) elements connected, resulting in storage ability of \( \log_2(N + 1) \) bits. This is because there is no possibility to individually determine states of all incorporated storage elements, as ideally they are characterized by the same resistance - only the number of elements in P and AP state may be determined, based on the two-point resistance measurement.

The storage cell capable of storing two bits of data would, therefore, consist of three serially connected storage elements. The predicted resistance vs. voltage characteristics of such a storage cell are presented in Fig. 2. Voltages for writing different states, as well as reading the cell can be defined based on the characteristics obtained for a single pMTJ. Note, that in the proposed cell configuration, writing smaller bit value

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II. EXPERIMENT

Multilayer of the following structure: buffer / Co(0.5)-Pt(0.2) based SyF / W(0.25) / CoFeB(1) / MgO(0.89) / CoFeB(1.3) / W(0.3) / CoFeB(0.5) / MgO(0.75) / capping layers (thickness in nm) patterned into pillars of around 130 nm diameter were used as pMTJ basic cell. The details of the deposition and fabrication processes are presented in Refs. [16–18]. Elements were equipped 100 × 100 µm² Al(20)/Au(30) contact pads that enable both individual pMTJ characterization as well as measurement of the elements connected in series forming a multi-bit cell. The schematics of the multilayer stack, fabricated pMTJ pillar and a micrograph of a two-bit (three pMTJs in series) cell are presented in Fig. 3. In order to determine an ability of a single element to act as a memory device, two types of characterization were performed: a stability diagram [17] and thermal stability [16] measurements.

The stability diagram was determined as follows: pMTJ resistance (R) versus voltage pulse amplitude (V_p) measurements were repeated with different external magnetic field (H) applied. Voltage pulse length was set to 10 ms. Each point on the stability diagram corresponds to the transition from the P to AP state or AP to P state, depending on the initial magnetization configuration. The thermal stability was determined from the R vs. H measurement repeated around hundred times with a fixed sweep rate of around 80 A/(m s).

IV. RESULTS AND DISCUSSION

A. Single pMTJ characterization

An example of the R(V_p) loop and the stability diagram are presented in Fig. 4. The TMR ratio of 135 % and resistance area (RA) product of 21.6 Ωμm² were measured. These values, however, are influenced by series resistance of vias and contacts, which could not be eliminated due to two-wire measurement; in fact, the TMR ratio of the element is higher [19]. In the absence of an external magnetic field, the P to AP transition occurs for the voltage of around 0.25 V (corresponding to the critical current density of 2.00 MA/cm²), whereas, the AP
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FIG. 4. a) Representative $R$-$V$ loop of a single pMTJ, with switching voltages from P to AP (red) and from AP to P (blue) marked using big squares, measured without external magnetic field. b) A stability diagram with marked regions where P, AP or both of the states are stable.

to P switching is measured for $V_p = -0.15$ V (corresponding to $J_{crt} = -0.54$ MA/cm$^2$). Multiple $R(H)$ measurements allowed to obtain the switching probability versus H using the analysis described in Ref. [16] with the following equation

$$P(\tau) = 1 - \exp\left[-\frac{\tau}{\tau_0} \exp\left\{-\Delta \left(1 - \frac{|H - H_s|}{H_{eff}^k}\right)\right\}\right]\quad(1)$$

In Eq. (1) \( \tau \) denotes the magnetic field step duration (in this study \( \tau = 1 \) s), \( \tau_0 \) the inverse of the attempt frequency (in this work assumed to be 1 ns), \( \Delta \) the thermal stability, \( H_s \) shift field and \( H_{eff}^k \) denotes the effective magnetic anisotropy field.

FIG. 5. a) Representative $R$-$H$ loop. b) Calculated switching probability (black points) and theoretical fit based on Eq. (1)

The best fit of Eq. (1) to the experimental switching probability resulted in \( \Delta = 60 \), which, together with a capability of the pMTJ of being stable in both P and AP states in the absence of an external magnetic field proves that the cell is suitable to be used as a memory device.

B. Two-bit storage cell

Next, we move on to the two-bit cell consisting of three pMTJs connected in series. $R(V_p)$ measurement of such a system is presented in Fig. 6a - initially two-bit cell is in the low resistance state. Application of the positive voltage of around 0.37 V (corresponding to a single pMTJ switching from P to AP state) results in the transition to higher resistance state, which is denoted as “01”. Further increase of voltage to around 0.67 V causes a second pMTJ transition to a higher resistance state - thus “10” state is written. Finally, after application of 0.80 V, all three pMTJs are in the AP state, which is denoted as “11” state. Negative voltage of −1.15 V switches all pMTJs back to P state. The behaviour described in Sec. II was confirmed – four stable states can be defined and binary numbers can be assigned to them:

- all elements in AP state - 11
- one element in P state and two in AP state - 10
- two elements in AP state and one in P state - 01
- all elements in P state - 00

By repeating $R$-$V$ measurement of two-bit cell around hundred times and calculating switching voltages distributions, writing voltages of particular states, as well as a region safe for reading the storage cell can be defined (Fig. 6b).

The principle of operation, involving the current decreasing below the critical current after one element switching into AP state, was confirmed (Fig. 7). Due to non-ideal manufacturing
process, critical currents of all incorporated elements are non-

C. Three-bit storage cell

Finally, the proof-of-concept of three-bit cell consisting of
seven pMTJs connected in series is presented. As predicted,
the cell exhibited eight stable states (Fig. 8). Due to non-
ideal fabrication process it was noted, that regions for writ-
ing voltages of some of the states are very narrow because of
variation of the switching voltage (related with the switching
current distribution). It is believed, that the behaviour is due
to very similar critical currents of all incorporated elements.
Also switching to "000" state was not ideal in the case, and
needs further investigation. Nonetheless, the proposed archi-
tecture is valid for a multiple pMTJ that form multi-bit mem-
ory cell.

V. SUMMARY

In summary, we showed that multi-bit memory cell can
be successfully implemented using serially connected pMTJs.
State-of-the-art multilayer structure characterized by TMR of
135 % and RA of 21.6 Ωμm² was used to design two- and
three-bit MRAM cells. The developed method of fabrication
and driving multi-bit non-volatile storage elements is a signif-
icannt improvement in MRAM technology, as it allows to store
more data using the same area of the memory. This may be
achieved by driving a multi-bit storage cell using a single tran-
sistor rated for the same current, as a single storage element

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