An analysis of the eddy effect in through-silicon vias based on Cu and CNT bundles: the impact on crosstalk and power

Chopali Chanchal Sahu1 · Shubham Anand1 · Manoj Kumar Majumder1

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Abstract
The performance of three-dimensional integrated circuits primarily depends on the filler material used in the through-silicon vias (TSVs). The most widely used filler material is Cu, but it faces severe reliability issues due to the skin effect and problems related to electromigration at high frequencies. Therefore, single- and multiwalled carbon nanotube (SWCNT and MWCNT) bundles have recently emerged as suitable filler materials for TSVs. Additionally, at high frequencies, electromagnetic forces induce eddy currents that adversely affect the overall performance of TSVs. This paper demonstrates for the first time the impact of eddy currents on TSVs based on Cu as well as SWCNT and MWCNT bundles. An accurate RLGC circuit model is proposed by considering the eddy effect at the depletion layer, neighboring TSVs and in the silicon substrate region. The resulting closed-form expressions for the TSV parasitic parameters are verified against previous experimental data obtained at an operating frequency of 2 GHz. Good agreement between the experimental and analytical data for the resistance and inductance is observed, revealing a difference of approximately 8.02% and 4.95%, respectively. The equivalent circuit parameters are modeled at the 7-nm technology node using a three-line driver-via-load setup. For the proposed setup, the crosstalk-induced delay, the peak noise voltage, and the power dissipation are analyzed with and without consideration of the eddy effect. Irrespective of the TSV height, the MWCNT bundle design demonstrates substantially lower crosstalk delay, peak noise, and power dissipation in comparison with the TSVs based on Cu or SWCNT bundles. The overall difference when including the eddy effect is approximately 16.55%, 2.45%, and 0.27% for the crosstalk delay, noise voltage, and power dissipation, respectively. Furthermore, to demonstrate the complexity of the model at smaller technology nodes, a comprehensive study is performed at the 5-nm and 7-nm technology nodes. It is observed that the delay without the eddy effect at the 5-nm technology node is higher on average by 3.4-fold for Cu, whereas for the TSVs based on MWCNT bundles it is only 2.6-fold higher.

Keywords Crosstalk-induced delay · Peak noise · Power dissipation · Eddy effect · Skin effect · Single-walled CNTs (SWCNTs) · Multiwalled CNTs (MWCNTs) · Circuit-level approach

1 Introduction

Recently, the through-silicon vias (TSVs) in three-dimensional integrated circuits have attracted extensive attention due to their higher packaging density and bandwidth [1, 2], low latency [3], and homogeneous and heterogeneous integration [4, 5]. Mostly, copper (Cu) is used as the filler material in TSVs due to its better conductivity and compatibility with the via-last TSV fabrication process [6]. However, challenges due to fabrication limitations in accomplishing physical vapor deposition (PVD) and seed layer deposition for Cu-based TSVs have driven researchers to introduce carbon nanotubes (CNTs) as an alternative filler material. CNTs are hollow cylindrical structures made
up of graphene sheets rolled up concentrically at a specific angle [7]. Two types of CNTs, viz. single- (SWCNT) and multiwalled CNTs (MWCNT), are generally preferred as filler materials. Their negligible electromigration and thermal stability, and unique electrical and mechanical properties give CNTs an edge over other TSV filler materials for use in nanotechnology [8]. However, the performance of TSVs at the nanometer level is affected by several deep-submicron effects such as short-channel effects including the reverse short-channel effect, poly depletion and the surface charge centroid effect, the narrow-channel effect, the reverse narrow-channel effect, the leakage current effect, the drain-induced barrier lowering effect, and the hot carrier effect. At smaller technology nodes, the physical dimensions of TSVs are reduced, which improves the device density and operating frequency of such ICs. However, the diffusion of metal from the TSV to the silicon substrate increases as the channel length is reduced. Due to this reduced channel length, the channel electric field becomes more significant, which is the primary reason for the hot carrier effect. The charge carriers can then gain sufficient kinetic energy to break the barrier between the TSV and the silicon substrate. Some negative short-channel effects include the drain-induced barrier lowering, velocity saturation, and quantum confinement [9]. Usually, the threshold voltage reduces with the channel length due to such short-channel effects. In the reverse short-channel effect, the threshold voltage increases for a reduced channel length due to the nonuniform doping profile used in device manufacturing at the deep-submicron level. However, this higher threshold requires a higher gate voltage [10]. Thus, severe challenges are introduced in TSVs when moving towards smaller technology nodes. Furthermore, at smaller technology nodes, the eddy resistance plays a key role in the high-frequency modeling of TSVs. According to Faraday’s law of induction and Lenz’s law [11, 12], the eddy current is circulatory in nature because it opposes the change in the magnetic field. Hence, an eddy resistance occurs at high frequency.

In general, most state-of-the-art experimental evidence [13–22] describes equivalent RLGC models for cylindrical-shaped TSVs. Previously, researchers [13, 14] reported a comparative study on the propagation delay of TSVs with different filler materials such as Cu or SWCNT and MWCNT bundles but neglecting the eddy effect in the depletion layer and neighboring TSVs. Later, Kim et al. [15] presented a compact alternating-current (AC) model of a TSV including the via bump, redistribution layers, and skin effect. That analysis was based on an eye diagram using the method described in Ref. [16]. However, the impact of the eddy effect has been ignored in TSV modeling. Some researchers [17, 18] have proposed comprehensive models for TSVs based on SWCNT bundles, describing a significant improvement in the delay and power performance. However, those authors did not carry out high-frequency analysis. Later, Su et al. [19] proposed an equivalent model of MWCNT-based TSV that considered the eddy effect only in the substrate region. Lu et al. [20] demonstrated a pi equivalent electrical model of the Cu-based TSV with consideration of eddy currents and the proximity effect at high frequencies. However, those authors restricted their research to the impact of the eddy effect on only the power loss of the TSV. Later, Liao et al. [21] demonstrated the crosstalk-induced delay by considering the proximity effect in a shielded paired TSV. However, the impact of the eddy effect was restricted to only the silicon substrate. Recently, researchers [22] demonstrated the delay and power dissipation for differently shaped TSVs while considering the skin effect at high frequency. However, the mutual inductance, eddy resistance, and depletion capacitance were ignored. Therefore, current state-of-the-art research [13–22] fails to enable a comprehensive analysis of the eddy effect for TSVs at high frequencies, hence a detailed investigation is required to clarify the eddy resistance of TSVs.

This study demonstrates, for the first time, electrical modeling of TSVs with consideration of the eddy effect at high frequencies. To demonstrate this effect, a closed-form expression is derived for the eddy resistance in the depletion region, silicon substrate, and neighboring TSVs. In addition, the metal oxide semiconductor (MOS) effect is also considered during the RLGC modeling of the TSV. Furthermore, the liner and the depletion layers are used to provide isolation to the TSV from the silicon substrate. Similarly, intermetal dielectric (IMD) and underfilled layers are included to isolate the bump from the silicon substrate and to prevent coupling between the bumps, respectively. This paper analyzes the crosstalk and power performance using a three-line parallel driver-via-load (DVL) setup, wherein via lines with Cu, SWCNT, and MWCNT bundles as filler material are modeled. The model primarily considers the impact of the eddy effect at the 7-nm technology node [23]. The main reason behind choosing this node is that it provides higher device density, improved power savings, and better performance. A unique setup with 20 distributed pi-type networks is used for the electrical circuit model. A pi-type distributed network is considered instead of L- or T-type networks due to performance accuracy considerations [24, 25]. Thereafter, to demonstrate the complexity of the model at lower technology nodes, a comprehensive analysis of the crosstalk and power is also performed at the 5-nm technology node.

This manuscript is organized into the following sections: Sect. 1 sheds light on the recent state-of-art research scenario and summarizes the modeling of cylindrical-shaped TSVs, taking into account the impact of the eddy resistance. Section 2 introduces the electrical equivalent model for the TSVs based on Cu, and SWCNT or MWCNT bundles (number of shells ,n= 10) with and without consideration
of the eddy resistance. A detailed analytical expression is derived to model the eddy resistance in the silicon substrate, depletion region, and neighboring TSVs. Based on the proposed model, Sect. 3 describes a comprehensive study of the impact of the eddy resistance on the crosstalk noise, delay, and power dissipation, considering different heights and frequencies. Finally, Sect. 4 briefly concludes this work with a summary.

2 The TSV model and eddy resistance

This section describes the cylindrical-shaped TSV structure and its physical parameters when using the different filler materials, viz. Cu, and SWCNT or MWCNT bundles. Furthermore, a closed-form expression is derived for the eddy resistance in the depletion region, the silicon substrate, and the neighboring TSVs. A novel equivalent electrical model for the cylindrical TSV is then proposed with consideration of the eddy resistance.

2.1 The structure and physical parameters of the TSV

This subsection provides a detailed description of the structure of the TSV and quantitative values for several of its parameters that will be used in the equivalent RLGC model. Figure 1a and b show the physical configuration and a top cross-sectional view of the cylindrical TSV, respectively. The TSV is surrounded by an insulating layer such as a liner (usually SiO₂) as well as depletion layers to provide direct-current (DC) isolation and prevent leakage between the TSV and the substrate. Usually, copper is used as a filler material in the TSV and the bump. A cylindrical-shaped pillar bump is used to provide a contact between the TSVs and different functional blocks of the die. In general, an IMD and under-filled layer are used to isolate the bump from the substrate and to reduce the cross-coupling between the bumps, respectively. Lossy silicon material is considered as the substrate, whereas the depletion region consists of lossless silicon to reduce the leakage. Silica-filled anhydride resin polymers are used in the underfilled layer to prevent coupling between the bumps.

The physical parameters of the cylindrical TSVs designed at the 7- and 5-nm technology nodes [26] are presented in Fig. 1 and Table 1. The number of CNTs in a bundle is primarily calculated using the cross-sectional area of the TSV and the diameter of the CNTs, as discussed below.

2.2 The Cu-based TSV model

This subsection describes the Cu-based TSV modeling with consideration of the eddy effect in the silicon substrate, depletion region, and neighboring TSVs. Firstly, a closed-form expression for the eddy resistance in the silicon substrate is derived by using the physical dimensions of the TSV as shown in Fig. 1. The equivalent RLGC circuit model of the three-line TSV at high frequency is presented in Fig. 2. Whenever a high-frequency current passes through the TSV, it generates a varying magnetic field. Thus, the magnetic vector potential \( \vec{A} \) is calculated by using the Maxwell equation [28, 29] as

\[
\nabla^2 \vec{A} = j \omega \mu_0 \sigma_{\text{Si, eff}} \vec{A},
\]

Table 1 The physical dimensions of the cylindrical-shaped TSV at the 7- and 5-nm technology nodes

| Physical parameter | Symbol | Physical dimension at each technology node |
|--------------------|--------|------------------------------------------|
| TSV pitch (nm)*    | \( p_{\text{via}} \) | 23             13 |
| TSV diameter (nm)**| \( d_{\text{tsv}} \) | 10.5          6 |
| Aspect ratio       | \( d_{\text{tsv}}/h_{\text{tsv}} \) | 2.4          2.4 |
| TSV height (nm)    | \( h_{\text{tsv}} \) | 60             60 |
| Oxide thickness (nm)*** | \( t_{\text{liner}} \) | 1.05          0.6 |
| Depletion width (nm) | \( t_{\text{dep}} \) | 1.65          1.20 |
| Bump diameter (nm) | \( d_{\text{bump}} \) | 22.26         13.44 |
| Bump height (nm)   | \( h_{\text{bump}} \) | 3.71          2.24 |
| IMD layer height (nm) | \( h_{\text{IMD}} \) | 1.05          0.6 |

* The via pitch, i.e., the center-to-center distance between adjacent TSVs [26]
** The TSV pitch \( p_{\text{via}} \) should be equal to or greater than twice the TSV diameter \( d_{\text{tsv}} \) to avoid misalignment [27], thus \( p_{\text{via}} \geq 2d_{\text{tsv}} \)
*** The oxide thickness \( t_{\text{liner}} \) is assumed to be \( d_{\text{tsv}}/10 \) [14]
where \( \sigma_{\text{Si,eff}} = \sigma_{\text{Si}} + j\omega\mu_{\text{Si}} \) is the effective conductivity of the silicon substrate and \( \omega \) is the angular frequency. Assuming that the magnetic vector potential has only a \( z \)-directional component but varies in the radial direction \( r \) of the TSV, the variation in the \( \phi \) and \( z \) directions will be zero in the cylindrical coordinate system. Therefore, \( \partial A_z / \partial z = 0, \partial A_z / \partial \phi = 0 \) \[30\]. Equation (1) can thus be simplified to

\[
\frac{\partial^2}{\partial r^2} A_z(r) + \frac{1}{r} \frac{\partial}{\partial r} A_z(r) + k_s^2 A_z(r) = 0, \tag{2}
\]

where \( k_s = \left(j\omega\mu_{\text{Si}}\sigma_{\text{Si,eff}}\right)^{1/2} \). Using the solution of the Bessel function, Eq. (2) can be simplified to

\[
A^{\text{sub}}_z(r) = c_1 H_0^{(1)}(k_s r) + c_2 H_0^{(2)}(k_s r), a_1 \leq r \leq b_1 \tag{3}
\]

where \( c_1 \) and \( c_2 \) are arbitrary constants, \( a_1 = r_{\text{TSV}} + t_{\text{liner}} + t_{\text{dep}}, \) and \( b_1 = [p_{\text{via}} - (r_{\text{TSV}} + t_{\text{liner}} + t_{\text{dep}})] \). It is assumed that the total current \( I \) is passing through the TSV. Hence, Ampere’s law can be used to obtain the magnetic vector potential in the depletion and insulating layers as

\[
A^{\text{ins}}_z(r) = -\frac{\mu I}{2\pi} \ln(r) + c_3, \tag{4}
\]

where \( r_{\text{TSV}} \leq r \leq a_1 \) or \( b_1 \leq r \leq (p_{\text{via}} - r_{\text{TSV}}) \). Applying the boundary condition in the TSV as in Eq. (5) to Eq. (8) yields

\[
A^{\text{ins}}_z(r) \bigg|_{r=a_1} = A^{\text{sub}}_z(r) \bigg|_{r=a_1}, \tag{5}
\]

\[
\frac{\partial}{\partial r} A^{\text{ins}}_z(r) \bigg|_{r=a_1} = \frac{\partial}{\partial r} A^{\text{sub}}_z(r) \bigg|_{r=a_1}, \tag{6}
\]

\[
A^{\text{ins}}_z(r) \bigg|_{r=b_1} = A^{\text{sub}}_z(r) \bigg|_{r=b_1}, \tag{7}
\]

\[
\frac{\partial}{\partial r} A^{\text{ins}}_z(r) \bigg|_{r=b_1} = \frac{\partial}{\partial r} A^{\text{sub}}_z(r) \bigg|_{r=b_1}. \tag{8}
\]

Now, \( c_1 \) and \( c_2 \) can be obtained after solving the above expressions as follows:

\[
c_1 = \frac{\mu_0 H_{\text{ref}} I}{2\pi k_s} \times \frac{m^2(a_1, b_1)}{u}, \tag{9}
\]

\[
c_2 = \frac{\mu_0 H_{\text{ref}} I}{2\pi k_s} \times \frac{m^1(b_1, a_1)}{u}, \tag{10}
\]

where

\[
u = \left\{ H_1^1(k_s a_1) \times H_1^2(k_s b_1) \right\} - \left\{ H_1^1(k_s b_1) \times H_1^2(k_s a_1) \right\}. \tag{11}
\]
\[ mp(r_1, r_2) = \frac{1}{r_1} H^{(0)}(k r_1) - \frac{1}{r_2} H^{(0)}(k r_2). \]  

(12)

The electric current density in the substrate is \( J_z^{\text{sub}}(r) \), which can be derived from Eqs. (3), (9), and (10) as

\[ J_z^{\text{sub}}(r) = -j \omega \mu_S \sigma_{\text{Si,eff}} \times A_z^{\text{sub}}(r), a_1 \leq r \leq b_1. \]  

(13)

Hence, the eddy resistance in the substrate \( (r'_{e,\text{sub}}') \) can be obtained by using Eq. (13) and can be expressed per unit height (p.u.h.) as

\[ r'_{e,\text{sub}} = \frac{1}{\sigma_{\text{Si,eff}}} [J_z^{\text{sub}}(b_1) - J_z^{\text{sub}}(a_1)]. \]  

(14)

where \( h = h_{\text{tsv}} - 2h_{\text{IMD}} \) for the calculation of the eddy resistance over the total height. In the same way, the eddy resistance in the depletion region \( (r'_{e,\text{dep}}') \) and the neighboring TSVs \( (r'_{e,\text{TSV}}') \) can be obtained by using the limits of the radius and the material as \( (r_{\text{TSV}} + t_{\text{liner}}) \leq r \leq (r_{\text{TSV}} + t_{\text{liner}} + t_{\text{dep}}) \) and \( (r_{\text{TSV}} + t_{\text{liner}} + t_{\text{dep}}) \leq r \leq (p_{\text{via}} + (r_{\text{TSV}} + t_{\text{liner}} + t_{\text{dep}})) \), respectively. Values of the conductivity of \( \sigma_{\text{Si,dep}} = 1.56 \times 10^{-3} \, \text{S/m} \) in the depleted silicon region and \( \sigma_{\text{Si}} = 100 \, \text{S/m} \) for the silicon substrate are considered herein.

As shown in Fig. 2, the other parasitic parameters of the TSV can be obtained by using its physical dimensions. First, the total capacitance \( (C_{\text{uimd}}) \) is a parallel combination of the underfill \( (C_{\text{uf}}) \) and IMD capacitances \( (C_{\text{imd}}) \). \( C_{\text{uf}} \) occurs between pairs of bumps due to the presence of the underfilled layer made of silica-filled anhydride resin polymer. However, \( C_{\text{imd}} \) occurs between pairs of TSVs due to the presence of the IMD layer [31]. \( C_{\text{uf}} \) and \( C_{\text{imd}} \) can be modeled as parallel-wire capacitances thus [15]:

\[ C_{\text{imd}} = \frac{\pi \times \varepsilon_{\text{IMD}} \times h_{\text{IMD}}}{\cosh^{-1} \left( \frac{p_{\text{via}}}{d_{\text{bump}}} \right)}, \]  

(15)

\[ C_{\text{uf}} = \frac{\pi \times \varepsilon_{\text{uf}} \times h_{\text{bump}}}{\cosh^{-1} \left( \frac{p_{\text{via}}}{d_{\text{bump}}} \right)}, \]  

(16)

\[ C_{\text{uimd}} = C_{\text{uf}} + C_{\text{imd}}. \]  

(17)

A capacitance corresponding to the silicon substrate \( (c'_{\text{sub}}') \) occurs between the TSVs due to the presence of the conductive silicon substrate. \( c'_{\text{sub}} \) p.u.h. can be derived using the parallel-wire capacitance model [32] as

\[ c'_{\text{sub}} = \begin{cases} \frac{2 \pi \times \varepsilon_{\text{Si}}}{\cosh^{-1} \left( \frac{\rho_{\text{via}}}{2 \left( t_{\text{via}} + t_{\text{liner}} + t_{\text{dep}} \right)} \right) - 1}, \end{cases} \]  

(18)

where the height is considered to be \( h = h_{\text{tsv}} - 2h_{\text{IMD}} \). In addition, the substrate conductance \( g'_{\text{sub}} \) occurs between pairs of TSVs due to the lossy characteristics of the silicon substrate. \( g'_{\text{sub}} \) can be obtained by using the relationship between \( c'_{\text{sub}} \) and \( g'_{\text{sub}} \) as discussed in ref. [15]. The liner capacitance \( c'_{\text{liner}} \) occurs between the TSV and depletion layer due to the presence of the oxide layer [15]. In addition, the depletion capacitance \( c'_{\text{dep}} \) occurs between the TSVs surrounded by the oxide layer and the Si substrate in the presence of the depletion layer [32]. \( c'_{\text{liner}} \) and \( c'_{\text{dep}} \) p.u.h. can be derived by applying the coaxial-wire capacitance model.

The bump capacitance \( c'_{b} \) occurs between the silicon substrate and the bump due to the presence of the IMD layer. The bump capacitance p.u.h. can be expressed by using the parallel-plate capacitor model [15] as

\[ c'_{b} = \frac{\varepsilon_{\text{IMD}} \times 2 \left( \frac{d_{\text{bump}}}{2} \right)^2 - \left( \frac{d_{\text{bump}}}{2} + t_{\text{liner}} + t_{\text{dep}} \right)^2}{h_{\text{IMD}}}. \]  

(19)

Moreover, the total resistance of the circuit \( r'_{t} \) in Fig. 2 is a series combination of the TSV resistance \( r'_{\text{tsv}} \) and the bump resistance \( r'_{b} \):

\[ r'_{t} = r'_{\text{tsv}} + r'_{b}. \]  

(20)

where \( r'_{\text{tsv}} \) and \( r'_{b} \) are obtained using the DC and AC components of the resistance p.u.h. Here, the AC component of the resistance primarily considers the skin effect of the TSV [15]. On the other hand, the total inductance \( l'_{t} \) is a series combination of the bump inductance \( l'_{b} \) and the TSV inductance \( l'_{\text{tsv}} \) [15]. The inductance occurs due to the magnetic field produced by the current passing through the TSV.

To verify the accuracy of the proposed model, the quantitative values of the via parasitics are validated against the experimental results provided by Savidis et al. [33], who extracted electromagnetic solutions for the resistance and inductance for a Cu-based cylindrical-shaped TSV using a three-dimensional (3D) numerical simulation tool. For verification of the closed-form expression, the quantitative values of the via resistance and inductance are calculated at the given technology in Ref. [33] and compared with the simulated data in Fig. 3a and b, respectively.

To enable a comparison with the experimental results, values of the TSV diameter \( (d_{\text{tsv}}) \) in the range from 5 to 60 µm are considered, with aspect ratios of 0.5, 1, 3, 5, 7, and 9. The via resistance and inductance are calculated at an operating frequency of 2 GHz and shown in Fig. 3. Good agreement is observed between the experimental results and the calculated values of the resistance and inductance. The maximum difference between the analytical and experimental values of the TSV resistance and inductance is only 8.02% and 4.95%, respectively.
2.3 The CNT-based TSV model

This subsection presents the equivalent electrical model and the techniques used to calculate the parasitics for the TSVs based on the SWCNT then MWCNT bundles. The modeling of the via parasitics primarily depends on the number of conducting channels in each SWCNT present in a bundle. The total number of SWCNTs \( N_{\text{CNT}} \) in a bundle is calculated using the radius of each SWCNT \( r_{\text{CNT}} \), the radius of the TSV \( r_{\text{via}} \), and the van der Waals distance \( \delta \approx 0.34 \text{ nm} \) between adjacent SWCNTs. \( N_{\text{CNT}} \) can be represented as

\[
N_{\text{CNT}} = \frac{2\pi r_{\text{via}}^2}{\sqrt{3(2r_{\text{CNT}} + \delta)^2}}.
\]  

(21)

The number of conducting channels in a MWCNT is a function of the shell diameter [34]. All the SWCNTs in a bundle have either metallic or semiconductor nature depending on their chirality, whereas MWCNTs are always metallic. For the metallic SWCNTs in a bundle, the average number of conducting channels for an SWCNT of a particular diameter is

\[
N_i(D_i) \approx \left\{ \begin{array}{ll} k_1 D_i + k_2, & D_i > d_t/T \\ \frac{2}{3} D_i \leq d_t/T, \end{array} \right.
\]  

(22)

where \( D_i \) is the diameter of the \( i \)-th shell of the MWCNT (or SWCNT) and \( k_1 \) and \( k_2 \) takes values of \( 2.04 \times 10^{-4} \text{ nm}^{-1} \) and 0.425, respectively. The quantitative value of \( d_t \) is determined from the thermal energy of the electrons and the gap between the two subbands, which is equivalent to 1300 nm.k at \( T = 300 \text{ K} \). For \( D_i > 4.3 \text{ nm} \), the average number of conducting channels is proportional to the shell diameter. Therefore, the total number of conducting channels in a bundle can be calculated by taking the sum of the conducting channel of each SWCNT/ MWCNT in a bundle as

\[
N_{\text{channel}} = \sum_{i=1}^{n} N_i.
\]  

(23)

The conduction mechanism in a CNT is ballistic due to the long mean free path (mfp) in the range of micrometers. The diameter following mfp can be expressed as

\[
\lambda_{\text{mfp},i} = \frac{1000}{\left( \frac{D_i}{T} \right)^2 - 2}.
\]  

(24)

Thus, the total number of conducting channels can be expressed as

\[
N_{\text{Total}} = N_{\text{channel}} \times N_{\text{CNT}}.
\]  

(25)

The electrical equivalent RLGC model of the CNT bundle-based TSV considering the eddy resistance is shown in Fig. 4. Each CNT in a bundle contributes broadly three types of resistance: (1) the scattering resistance \( r'_{\text{bundle}} \) that occurs due to the fact that the nanotube is longer than the mfp of the electron, (2) the quantum resistance \( R_q \) due to the quantum confinement of the electrons and depending on the \( N_{\text{channel}} \) of each SWCNT/ MWCNT in a bundle, and (3) the resistance corresponding to the imperfect contact between the metal and the nanotube \( R_{\text{mc}} \) with an approximate value of 3.2 k\( \Omega \), arising
due to the fabrication process [34–37]. Thus, the equivalent scattering and quantum resistances can be expressed as

$$R_{\text{fix}} = \frac{R_q}{N_{\text{Total}}} + R_{\text{mc}}, \quad \text{where } R_q = \frac{h}{2e^2} \approx 12.9 \, \text{kΩ}, \quad (26)$$

$$\frac{l}{B_{\text{bundle}}} = \left( \sum_{i=1}^{n} (R_q / 2N_i N_{\text{Ambipolar}}) \right)^{-1} \times N_{\text{CNT}}, \quad (27)$$

where $h$ and $e$ denote Planck’s constant and the electron charge, respectively. The equivalent RLGC model of the CNT bundle includes two types of capacitance: (1) the quantum capacitance ($c_{q,\text{bundle}}$) arising due to the finite electronic states in a quantum wire and (2) the electrostatic capacitance ($c_{E,\text{bundle}}$) that is due to the potential difference between the CNT bundle and the ground plane. $c_{q,\text{bundle}}$ and $c_{E,\text{bundle}}$ in p.u.h. can be expressed as

$$c_{q,\text{bundle}} = c_q \times 2N_{\text{Total}} \quad \text{where } c_q = \frac{2e^2}{h v_f}, \quad (28)$$

$$c_{E,\text{bundle}} = \frac{2\pi \varepsilon_0 \varepsilon_f}{\cosh^{-1} \left( d_{\text{out}}^2 + h_{\text{mc}}^2 / 2c_{\text{CNT}}^2 \right)}. \quad (29)$$

where $d_{\text{out}}^\text{CNT}$ and $v_f$ represent the outer shell diameter of the SWCNT/MWCNT and the Fermi velocity ($\approx 8 \times 10^5 \, \text{m/s}$), respectively. Similarly, the equivalent bundle inductance ($l'_{\text{Bundle}}$) of the TSV is a combination of two types of inductance: (1) the kinetic inductance ($l'_{k}$) associated with the kinetic energy of the electrons in each conducting channel of the CNT and (2) the magnetic inductance ($l'_{m}$) due to the magnetic field induced by the current flowing through the nanotube [37]. Thus, $l'_{\text{Bundle}}$ can be primarily expressed as

$$l'_{\text{Bundle}} = \frac{l'_{k}}{2N_{\text{Total}}} + l'_{m}, \quad (30)$$

where

$$l'_{k} = \frac{h}{2e^2 v_f} \quad \text{and } l'_{m} = \frac{\mu}{2\pi} \ln \left( \frac{y}{c_{\text{CNT}}^\text{out}} \right). \quad (31)$$

Fig. 4 An equivalent RLGC circuit model of the CNT-based C-TSV with consideration of the eddy effect
when considering TSVs based on Cu or CNT bundles are summarized in Table 2 for different via heights and operating frequencies. Note that the quantitative values of the parasitic parameters are smaller for the MWCNT bundles compared with the Cu TSV, irrespective of the via height. As shown in Table 2, the eddy resistance in the neighboring TSV $R_{\text{e}_{\text{tsv}}}$ has a great impact at high frequencies due to the eddy effect and the skin effect.

Table 2 The values of the parasitic parameters for the C-TSVs based on Cu and the SWCNT or MWCNT bundles for different via heights and operating frequencies

| TSV height (nm) | Parameter value for C-TSV at an operating frequency (in GHz) of Cu-based TSV | SWCNT-bundle-based TSV | MWCNT-bundle-based TSV |
|-----------------|---------------------------------------------------------------------------------|------------------------|------------------------|
|                 | $R_{\text{eq}}$ (Ω) | $R_{\text{e}_{\text{tsv}}}$ (μΩ) | $R_{\text{e}_{\text{dep}}}$ (kΩ) | $L_{\text{eq}}$ (H) | $C_{\text{eq}}$ (aF) | $C_{\text{sub}}$ (aF) | $G_{\text{sub}}$ (μS) |
| 30              | 6.0545 | 0.1341 | 4.1485 | 7.0100 | 18.3451 | 1.1050 | 9.6004 |
| 60              | 11.9543 | 0.2681 | 6.0963 | 9.1326 | 31.1581 | 19.9230 | 60.2460 |
| 90              | 17.8542 | 0.4023 | 13.0700 | 9.1326 | 43.9697 | 31.8680 | 60.2460 |
| 120             | 23.7541 | 0.5364 | 15.7310 | 9.3683 | 56.7836 | 42.7450 | 40.6090 |

$R_{\text{eq}} = \left\{ \begin{array}{ll} R_{\text{cu}} + R_{\text{e}_{\text{sub}}}, & \text{for Cu-based TSV} \\ R_{\text{bundle}} + R_{\text{e}_{\text{sub}}}, & \text{for CNT-based TSV} \end{array} \right.$

$C_{\text{eq}} = \left\{ \begin{array}{l} C_{\text{b}} + \frac{1}{2} \left( \frac{C_{\text{sub}} \times C_{\text{eq}}}{C_{\text{eq}} + C_{\text{sub}}} \right), \text{for Cu-based TSV} \\ C_{\text{b}} + \frac{1}{2} \left( \frac{C_{\text{b}} \times C_{\text{eq}}}{C_{\text{eq}} + C_{\text{b}}} \right), \text{for CNT-based TSV} \end{array} \right.$

$L_{\text{eq}} = \left\{ \begin{array}{l} L_{\text{cu}}, \text{for Cu-based TSV} \\ L_{\text{bundle}}, \text{for CNT-based TSV} \end{array} \right.$
3 Performance analysis

This section illustrates the impact of the eddy current on the crosstalk-induced delay, peak noise, and power dissipation using the *RLGC* model proposed for the TSV at the 7-nm technology node. A three-line DVL setup (Fig. 5) is used for the circuit-level simulations of the TSV with 20 distributed pi networks using industry-standard software (Synopsys HSPICE version 2020). Each via line represents the *RLGC* model of the TSV as shown in Figs. 2 and 4. The vias are driven by a field-effect transistor (FET) instead of a complementary metal–oxide–semiconductor (CMOS) driver at the 7-nm technology node. However, several challenges are introduced when scaling down the technology, such as the closer proximity of the TSVs and the ultrahigh-resolution lithography requirements. With an increase in the TSV density, the impact of the cross-coupling capacitance becomes more severe and isolating them from one another becomes a challenging task. As a result, the performance of the overall system degrades [38].

On the other hand, the physical dimensions at lower technology node require a complex, costly fabrication process and require ultrahigh-resolution lithography [39]. Although CMOS performs well down to the 28-nm technology node, below this it shrinks in such a way that short channel-effects become uncontrollable. As a result, the gate is unable to control the leakage path. In the case of a FET driver, good control of the gate on the leakage path is obtained at lower technology node, hence FETS can be used as suitable drivers. In Fig. 5, each via line is terminated with a load capacitor $C_{load}$ of 200 aF. Using the setup illustrated in Fig. 5, the subsequent sections analyze the overall reliability of the TSV in terms of the crosstalk-induced delay, peak voltage, and power dissipation for different operating frequencies and via heights.

### 3.1 The crosstalk delay analysis

This subsection presents an analysis of the crosstalk-induced delay of the C-TSV with consideration of the eddy effect in terms of the dynamic crosstalk delay, applying the DVL setup shown in Fig. 5. The transmission line introduces some delay when the signal passes through it. In this situation, one of the transmission lines can act as an aggressor while the other can act as a victim. The dynamic crosstalk delay phenomena is introduced when all the signals provided to the aggressor and victim lines are in the same or the opposite switching state at the same time. However, in the case of out-of-phase crosstalk delay, all the signals exhibit the opposite switching transition from each other [40]. Furthermore, this out-of-phase crosstalk delay represents the worst case due to the higher Miller capacitive factor (MCF) between the vias [25]. Hence, this work considers the opposite switching transition state in the calculation of the crosstalk delay, e.g., where the aggressor line switches from high to low and the victim from low to high. Figure 6 shows the crosstalk delay of the TSVs based on Cu and the SWCNT or MWCNT bundles for via heights of $a$ $h_{TSV} = 30$ nm, $b$ $h_{TSV} = 60$ nm, $c$ $h_{TSV} = 90$ nm, and $d$ $h_{TSV} = 120$ nm.
due to the fact that the impact of the eddy current is greater at high frequencies, revealing that the eddy resistance in the neighboring TSV $R_{e_{t_{sv}}}$ rises with frequency, as also seen in Table 2. Additionally, it can also be observed that the crosstalk-induced delay increases with the TSV height and the operating frequency. This occurs due to the higher values of the parasitics as the via height or frequency is increased, as also shown in Table 2.

Additionally, Fig. 7 presents the rate of change in the crosstalk delay for different operating frequencies with respect to the delay obtained at 20 GHz, with and without considering the eddy effect, for $h_{TSV} = 120$ nm.

The percentage change in the crosstalk delay of the TSVs based on a Cu, and the b SWCNT or c MWCNT bundles for different operating frequencies with respect to the delay obtained at 20 GHz, with and without considering the eddy effect, for $h_{TSV} = 120$ nm is shown in Fig. 7. Note that the percentage change in the delay is greater at higher frequencies due to the corresponding increase in the delay. However, the rate of change of the crosstalk delay without consideration of the eddy effect is more severe than the variation in the delay when including the eddy effect. The percentage difference in the crosstalk delay when comparing the results obtained with versus without consideration of the eddy effect is 21.14%, 31.63%, 35.77%, and 38.35% at a frequency of 120, 200, 300, and 500 GHz, respectively, for the Cu-based TSV. Similarly, these differences in the delay for the TSV based on SWCNT bundles are 15.57%, 16.12%, 26.18%, and 27.04%, respectively, while the differences in the delay for the TSV based on the MWCNT bundle are 1.66%, 18.08%, 21.17%, and 25.29%, respectively. It can be observed that this difference in the rate of change in the delay improves when considering the TSV based on the MWCNT bundles. The average percentage change in the delay when including the eddy effect is 31.73%, 21.23%, and 16.55% for the TSVs based on Cu and the SWCNT and MWCNT bundles, respectively.

The percentage increment in the crosstalk-induced delay of the C-TSV at the 5-nm technology node with respect to the 7-nm technology is presented in Table 3 for various frequencies. It has been observed that the delay without the eddy effect increases on average by 3.4 times for Cu but only 2.6 times for the MWCNT-bundle-based TSV. However, the increment in the delay when including the eddy effect is reduced to 1.4 times for Cu, whereas for the MWCNT-bundle-based TSVs it is encouragingly reduced to 0.9 times. Therefore, it can be concluded that the MWCNT-bundle-based TSV demonstrates an improved delay compared with Cu at lower technology nodes.

### 3.2 Peak noise

This subsection discusses the impact of the eddy effect on the peak noise of the TSV. Conceptually, noise coupling takes place in the region of the substrate whenever fast signal transition occurs within the TSV. This coupling mechanism is similar to the noise coupling that takes place into the substrate through the source/drain junctions of a transistor. However, due to the greater dielectric area, the dielectric capacitance of the TSV is larger than the source/drain junction capacitance. TSV-related substrate noise coupling is therefore one of the primary noise injection

### Table 3 The percentage increment in the crosstalk-induced delay for the 5-nm technology node with respect to the 7-nm technology node at different frequencies

| Frequency (GHz) | Increase in delay for the 5-nm technology node with respect to the 7-nm technology node |
|-----------------|----------------------------------------------------------------------------------------|
|                 | Without eddy effect | With eddy effect |
|                 | Cu-based TSV | SWCNT-bundle-based TSV | MWCNT-bundle-based TSV | Cu-based TSV | SWCNT-bundle-based TSV | MWCNT-bundle-based TSV |
| 20              | 3.8×          | 3.4×              | 2.8×              | 1.7×          | 1.3×              | 0.9×              |
| 200             | 3.3×          | 2.8×              | 2.6×              | 1.3×          | 1.1×              | 0.8×              |
| 500             | 3.1×          | 2.8×              | 2.5×              | 1.3×          | 1.1×              | 0.9×              |
The peak noise of the TSVs based on Cu and the SWCNT or MWCNT bundles for via heights of \( h_{\text{TSV}} = 30 \) nm, \( h_{\text{TSV}} = 60 \) nm, \( h_{\text{TSV}} = 90 \) nm, and \( h_{\text{TSV}} = 120 \) nm.

Fig. 8 The peak noise of the TSVs based on Cu and the SWCNT or MWCNT bundles for via heights of \( a \) \( h_{\text{TSV}} = 30 \) nm, \( b \) \( h_{\text{TSV}} = 60 \) nm, \( c \) \( h_{\text{TSV}} = 90 \) nm, and \( d \) \( h_{\text{TSV}} = 120 \) nm.

Fig. 9 The percentage change in the peak noise of the TSVs based on \( a \) Cu, \( b \) SWCNT bundles, and \( c \) MWCNT bundles for different frequencies with respect to that obtained at 20 GHz, with and without considering the eddy effect, at \( h_{\text{TSV}} = 120 \) nm.

Mechanisms in 3D integrated circuits [41]. Peak noise is observed when the aggressor line is supplied with an in-phase signal while the victim line is grounded. This results in the formation of unintentional peaks that are observed on the victim line, which is responsible for faults in digital circuits [42]. Figure 8 shows the peak noise voltage of the TSVs based on Cu and SWCNT or MWCNT bundles, and with and without consideration of the eddy effect, for different TSV heights and frequencies. From Fig. 8, it can be observed that the peak noise voltage in the TSV based on MWCNT bundles is lesser as compared with those based on the SWCNT bundles or Cu due to the reduced coupling factor. Note also that the peak noise when including the eddy effect is considerably lower than that without considering it. Additionally, the peak noise is greater for higher TSVs and operating frequencies. The reason behind this finding is the higher parasitic values, which increase with the height and frequency as observed from Table 2.

Additionally, Fig. 9 shows the rate of change in the peak noise voltage for different frequencies with respect to the delay obtained at 20 GHz. This percentage change is calculated for the TSVs based on Cu and SWCNT or MWCNT bundles, with and without consideration of the eddy effect, at \( h_{\text{TSV}} = 120 \) nm, as shown in Fig. 9. Note that the percentage change in the noise voltage is considerably greater at higher frequencies due to the rise in the noise voltage with increasing frequency. However, the rate of change of the noise voltage when considering the eddy effect is more severe than without its consideration. The percentage difference in the peak noise voltage when calculated with versus without consideration of the eddy effect is 3.38%, 2.83%, 2.65%, and 2.45% at frequencies of 120, 200, 300, and 500 GHz, respectively, for the Cu-based TSV. Similarly, these differences in the peak noise voltage for the TSV based on SWCNT bundles are 3.04%, 2.64%, 2.61%, and 2.32%, while those for the TSV based on MWCNT bundles are 2.84%, 2.59%, 2.24%, and 2.05%, respectively. Note that the difference in the rate of change of the noise voltage improves when using the TSV based on MWCNT bundles. The average percentage change in the noise voltage when including the eddy effect is 2.83%, 2.65%, and 2.45% for the TSVs based on Cu and the SWCNT MWCNT bundles, respectively.

### 3.3 The Power Dissipation Analysis

This subsection demonstrates the impact of the eddy resistance on the dynamic power dissipation. The power dissipation is obtained by providing an in-phase signal either from low to high or from high to low through the coupled TSVs. Figure 10 shows the power dissipation of the TSVs based on Cu and the SWCNT or MWCNT bundles obtained with and without consideration of the eddy effect for different TSV heights and frequencies. Note that the TSVs based on
without consideration of the eddy effect at different frequencies with respect to that obtained at 20 GHz, with and without consideration of the eddy effect, as shown in Fig. 10. Additionally, the power consumption increases for higher TSVs and operating frequencies. The reason behind this finding is the higher quantitative values of the parasitics, which increase for higher TSVs and frequencies as seen in Table 2.

Furthermore, Fig. 11 presents the rate of change of the power dissipation for different frequencies with respect to that obtained at 20 GHz for a TSV height of 120 nm. This percentage change is calculated for the TSVs based on SWCNT and MWCNT bundles, with and without consideration of the eddy effect, as shown in Fig. 11. It is seen that the percentage change in the power dissipation is greater at higher frequencies. However, the rate of change of the power dissipation when considering the eddy effect is more severe than without its consideration. The percentage differences in the power dissipation when obtained with versus without consideration of the eddy effect is 0.17%, 0.43%, 0.6%, and 0.77% at frequencies of 120, 200, 300, and 500 GHz, respectively, for the Cu-based TSV. Similarly, these differences in the power dissipation are 0.08%, 0.35%, 0.52%, and 0.69%, respectively, for the TSV based on the SWCNT bundles, and 0.18%, 0.25%, 0.34%, and 0.31%, respectively, for the TSVs based on MWCNT bundles. Note that this difference in the rate of change of the power dissipation improves when using the TSV based on MWCNT bundles. The average percentage change in the power dissipation when including the eddy effect is 0.4925%, 0.41%, and 0.27% for the TSVs based on Cu and SWCNT or MWCNT bundles, respectively.

The percentage reduction in the peak noise voltage and the dynamic power dissipation of the C-TSV at the 5-nm technology node with respect to the 7-nm technology node is summarized in Tables 4 and 5, respectively, at various frequencies. Note that the peak noise and dynamic power dissipation without consideration of the eddy effect are reduced by approximately 7.24% and 35.2%, respectively, for the Cu-based TSV. In contrast, for the TSV based on the MWCNT bundles, it is reduced by 7.54% and 37.69%, respectively. However, the reduction in the peak noise voltage and dynamic power dissipation when including the eddy effect is 7.96% and 35.4%, respectively, for the Cu-based TSV, whereas for the TSV based on MWCNT bundles, it is encouragingly 8.24% and 37.79%, respectively. It can thus be concluded that the TSV based on MWCNT bundles demonstrates improved peak noise and dynamic power dissipation characteristics compared with Cu at this smaller technology node.
To analyze the static power dissipation of the TSV at the Deep Sub Micron (DSM) level, results for the 10-nm, 7-nm, and 5-nm technology nodes are shown in Fig. 12. Note that the static power dissipation increases as the technology is scaled down because of an increase in the leakage current $I_{\text{leakage}}$ [43], as shown in Eq. (32).

\[ P_{\text{static}} = I_{\text{leakage}} \times V_{DD}, \]  

(32)

where $V_{DD}$ is the supply voltage to the TSV and $I_{\text{leakage}}$ is the leakage current due to movement of charge carriers from the TSV to the silicon substrate. Furthermore, the liner and depletion layers are used to isolate the TSV to reduce the leakage current. However, the thicknesses of the liner and depletion layers are reduced when scaling down the technology, as revealed by Table 1. Hence, the leakage current increases substantially at smaller technology nodes. It can thus be concluded that an increase in the leakage current is a primary challenge when scaling down such technology.

**Table 4** The percentage reduction in the peak noise at the 5-nm technology node with respect to the 7-nm technology node at different frequencies

| Frequency (GHz) | The percentage (%) decrease in the peak noise for the 5-nm technology node with respect to the 7-nm technology node |
|-----------------|----------------------------------------------------------------------------------------------------------------|
|                 | Without consideration of the eddy effect | With consideration of the eddy effect |
| Cu-based TSV | SWCNT-bundle-based TSV | MWCNT-bundle-based TSV | Cu-based TSV | SWCNT-bundle-based TSV | MWCNT-bundle-based TSV |
| 20            | 5.82            | 5.69            | 5.65            | 7.06            | 7.18            | 7.04            |
| 200           | 7.87            | 8.23            | 8.34            | 8.40            | 8.63            | 8.92            |
| 500           | 8.03            | 8.31            | 8.64            | 8.43            | 8.50            | 8.77            |

**Table 5** The percentage reduction in the dynamic power dissipation for the 5-nm technology node with respect to the 7-nm technology node at different frequencies

| Frequency (GHz) | The percentage (%) decrease in the dynamic power dissipation for the 5-nm technology node with respect to the 7-nm technology node |
|-----------------|----------------------------------------------------------------------------------------------------------------|
|                 | Without consideration of the eddy effect | With consideration of the eddy effect |
| Cu-based TSV | SWCNT-bundle-based TSV | MWCNT-bundle-based TSV | Cu-based TSV | SWCNT-bundle-based TSV | MWCNT-bundle-based TSV |
| 20            | 36.00            | 37.21            | 38.53            | 36.27            | 37.28            | 38.91            |
| 200           | 35.06            | 36.29            | 37.60            | 35.20            | 36.35            | 37.61            |
| 500           | 34.53            | 36.24            | 36.93            | 34.72            | 35.85            | 36.85            |

Fig. 12 The static power dissipation of the TSV at diverse technology nodes.
4 Conclusions

A novel pi-type equivalent RLGC model for TSVs based on Cu and SWCNT or MWCNT bundles and considering the eddy effect at high frequencies at the 7-nm technology node is proposed herein. A closed-form expression for the eddy resistance is derived for the depletion region and the substrate and in the neighboring TSV. Furthermore, the performance of the TSV is analyzed in terms of the crosstalk delay, peak noise, and power dissipation with consideration of the eddy effect at high frequencies. The results reveal that the impact of the high-frequency eddy current is substantially lesser in the case of the TSV based on MWCNT bundles as compared with those based on Cu or SWCNT bundles. The overall difference is approximately 16.55%, 2.45%, and 0.27% for the crosstalk delay, noise voltage, and power dissipation, respectively.

References

1. Schaller, R.R.: Moore’s law: past, present, and future. IEEE Spectr. 34(6), 52–59 (1997)
2. Zhang C. and Sun G.: Fabrication cost analysis for 2D, 2.5D, and 3D IC designs. In: Proceedings of IEEE International 3D Systems Integration Conference (3DIC), pp. 1–4, Osaka, Japan (2012)
3. Kaushik, B. K., Kumar, V. R., Majumder, M. K., Alam, A.: Through Silicon Vias: Materials, Models, Design, and Performance (1st ed.), CRC Press, ISBN: 9781498745529 (2016)
4. Davis, W. R., et al.: Demystifying 3D ICs: the pros and cons of going vertical. IEEE Des. Test Comput. 22(6), 498–510 (2005)
5. Noia, B. and Chakrabarty, K.: Pre-bond probing of TSVs in 3D stacked ICs, in Proceedings of the International Test Conference (ITC ‘11), pp. 1–10, Anaheim, California, USA (2011)
6. Kannan, S., Gupta, A., Kim, B. C., Mohammed, F., Ahn, B.: Analysis of carbon nanotube based through silicon vias, in Proceedings of the IEEE 60th Electronic Components and Technology Conference (ECTC ’10), pp. 51–57, Las Vegas, Nev, USA (2010)
7. Kaushik, B. K., & Majumder, M. K.: Carbon Nanotube Based VLSI Interconnects. Springer Briefs Appl. Sci. Technol. (2015)
8. Alam, A., Majumder, M. K., Kumari, A., Kumar, V. R. and Kaushik, B. K.: Performance analysis of single- and multi-walled carbon nanotube based through silicon vias. 2015 IEEE 65th Electronic Components and Technology Conference (ECTC), pp. 1834–1839 (2015)
9. Gaynor, B. D., and Hassoun, S.: Simulation Methodology and Evaluation of Through Silicon Via (TSV)-FinFET Noise Coupling in 3-D Integrated Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 23(8), pp. 1499–1507, (2015)
10. Kunikyo, T., Mitsu, K., et al.: Reverse short-channel effect due to lateral diffusion of point-defect induced by source/drain ion implantation. IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. 13(4), 507–514 (1994)
11. Khan, A.A.: A novel apparatus to study Faraday’s laws of electromagnetic induction. IEEE Trans. Educ. 29(1), 30–31 (1986)
12. Hillmann, S., Schulze, M.H., and Heuer, H.: High-Frequency Eddy Current Techniques, In: Ida N., Meyendorf N. (eds) Handbook of Advanced NonDestructive Evaluation. Springer, ISBN: 9783319300504, Cham (2018)
13. Ismail, D.Y., Khellah, M., Karnik, T., De, V.: Analytical Model for the Propagation Delay of Through Silicon Vias, 9th International Symposium on Quality Electronic Design, pp. 553–556, San Jose, CA, USA (2008)
14. Xu, C., Li, H., Suaya, R., Banerjee, K.: Compact AC modeling and performance analysis of through-silicon vias in 3-D ICs. IEEE Trans. Electron Devices 57(12), 3405–3417 (2010)
15. Kim, J., et al.: High-frequency scalable electrical model and analysis of a through silicon via (TSV). IEEE Trans. Compon. Packag. Manuf. Technol. 1(2), 181–195 (2011)
16. Lim, S. K.: Design for High Performance, Low Power, and Reliable 3D Integrated Circuits, Springer New York, pp. 537 – 560, ISBN:9781441995421 (2012)
17. Goyal, T., Majumder, M. K., Kaushik, B. K.: Propagation delay and power dissipation for different aspect ratio of single-walled carbon nanotubebundled TSV. J. Semicond., 36(6), (2015)
18. Qian, L., Xia, Y., Liang, G.: Study on crosstalk characteristic of carbon nanotube through silicon vias for three dimensional integration. Microelectron. J. 46(7), 572–580 (2015)
19. Su, Jinrong, Chen, Xinwei, Han, Liping: Transmission characteristics of multi-walled carbon nanotube-based through-silicon vias considering temperature effects. IEEE Trans. Compon. Packag. Manuf. Technol. 6(10), 203–211 (2017)
20. Lu, Q., Zhu, Z., Yang, Y., Ding, R., Li, Y.: High-frequency electrical model of through-silicon vias for 3-D integrated circuits considering Eddy current and proximity effects. IEEE Trans. Compon. Packag. Manuf. Technol. 7(12), 2036–2044 (2017)
21. Liao, C., Zhu, Z., Lu, Q., Liu, X., Yang, Y.: Wideband electromagnetic model and analysis of shielded-pair through-silicon vias. IEEE Trans. Compon. Packag. Manuf. Technol. 8(3), 473–481 (2018)
22. Chandrakar, S., Gupta, D., Majumder, M. K.: Role of Through Silicon Via in 3D Integration: Impact on Delay and Power. J. Circuits, Syst. Computers (2020)
23. Gharavi Hamedani, S., Moaiyeri, M.H.: Impacts of process and temperature variations on the crosstalk effects in sub-10 nm multilayer graphene nanoribbon interconnects. IEEE Trans. Device Mater. Reliab. 19(4), 630–641 (2019)
24. Kumbhare, V.R., Paltani, P.P., Majumder, M.K.: Impact of interconnect spacing on crosstalk for multi-layered graphene nanoribbon. IETE J. Res., 1–10 (2019)
25. Kumbhare, V. R., Paltani, P. P., & Majumder, M. K.: Analysis of top- and side-contact MLGNR interconnects: impact on crosstalk, stability, and electromigration. J. Comput. Electron. (2020)
26. Hamedani, S. G., & Moaiyeri, M. H.: Impacts of process and temperature variations on the crosstalk effects in sub-10nm multilayer graphene nanoribbon interconnects. IEEE Trans. Device Mater. Reliab., 1–1 (2019)
27. Ahmed, M.A., Mohapatra, S., Chrzanowska-Jeske, M.: TSV- and delay-aware 3D-IC floorplanning. Analog. Integr. Circ. Sig. Process, 87, 235–248 (2016)
28. Ramo, S., Whinnery, J. R., Duzer, T. V.: Fields and Waves in Communication Electronics, Wiley-India, ISBN:9780471585510, (1994)
29. Niknejad, A.M., Meyer, R.G.: Analysis of eddy-current losses over conductive substrates with applications to monolithic inductors and transformers. IEEE Trans. Microw. Theory Tech. 49(1), 166–176 (2001)
30. Liang, F., Wang, G., Zhao, D., Wang, B.: Wideband impedance model for coaxial through-silicon vias in 3-D integration. IEEE Trans. Electron Devices 60(8), 2498–2504 (2013)
31. Cheng, D. K.: Fundamentals of Engineering Electromagnetics, Reading, Mass: Addison-Wesley Pub. Co., ISBN:978-0201566116 (1992)
32. Su, J., Wang, F., Zhang, W.: Capacitance expressions and electrical characterization of tapered through-silicon vias for 3D ICs. IEEE Trans. Compon. Packag. Manuf. Technol. 5(10), 1488–1496 (2015)
33. Savidis, I., Friedman, E.G.: Closed-form expressions of 3-D via resistance, inductance, and capacitance. IEEE Trans. Electron Devices 56(9), 1873–1881 (2009)
34. Naeemi, A., Meindl, J.D.: Performance modeling for single and multiwall carbon nanotubes as signal and power interconnects in gigascale systems. IEEE Trans. Electron Devices 55(10), 2574–2582 (2008)
35. Satio, R., Dresselhaus, G., Desselhaus, S.: Physical Properties of Carbon Nanotubes. Imperial College Press, London, UK (1998)
36. Saraswat, K.C.: 3-D ICs: motivation, performance analysis, technology and applications. in: Proc.2010 17th IEEE International Symposium on Physical and Failure Analysis of Integrated Circuits (IPFA) IEEE, pp. 1–6, Singapore, (2010)
37. Sarto, M.S., Tamburrano, A.: Single-conductor transmission-line model of multiwall carbon nanotubes. IEEE Trans. Nanotechnol. 9(1), 82–92 (2010)
38. Peng, Y., Song, T., Petranovic, D., Lim, S.K.: Silicon effect-aware full-chip extraction and mitigation of TSV-to-TSV coupling. IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. 33(12), 1900–1913 (2014)
39. Kumbhare, V. R., Paltani, P. P. and Majumder, M. K.: Analysis of top- and side-contact MLGNR interconnects: impact on crosstalk, stability, and electromigration. J. Comput. Electron. 19, (2020)
40. Kumbhare, V. R., Paltani, P. P., Majumder, M. K.: Impact of Interconnect Spacing on Crosstalk for Multi-layered Graphene Nanoribbon. IETE J. Res. (2019)
41. Kumbhare, V.R., Paltani, P.P., Majumder, M.K.: Novel Approach for Improved Signal Integrity and Power Dissipation Using MLGNR Interconnects VLSI Design and Test. Springer, Singapore (2019)
42. Ahmad, W., Chen, Q., Zheng, L., Tenhunen, H.: Modeling of peak-to-peak switching noise along a vertical chain of power distribution TSV pairs in a 3D stack of ICs interconnected through TSVs: pp. 1–6, NORCHIP (2010).
43. Valarmathy, M., Preetha, R.: Performance evaluation of static power reduction techniques in nano-scale CMOS circuits. JCR 7(5), 1225–1231 (2020)

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