GraphCage: Cache Aware Graph Processing on GPUs

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ABSTRACT

Efficient Graph processing is challenging because of the irregularity of graph algorithms. Using GPUs to accelerate irregular graph algorithms is even more difficult to be efficient, since GPU’s highly structured SIMT architecture is not a natural fit for irregular applications. With lots of previous efforts spent on subtly mapping graph algorithms onto the GPU, the performance of graph processing on GPUs is still highly memory-latency bound, leading to low utilization of compute resources. Random memory accesses generated by the sparse graph data structure are the major causes of this significant memory access latency. Simply applying the conventional cache blocking technique proposed for matrix computation have limited benefit due to the significant overhead on the GPU.

We propose GraphCage, a cache centric optimization framework for highly efficient graph processing on GPUs. We first present a throughput-oriented cache blocking scheme (TOCAB) in both push and pull directions. Comparing with conventional cache blocking which suffers repeated accesses when processing large graphs on GPUs, TOCAB is specifically optimized for the GPU architecture to reduce this overhead and improve memory access efficiency. To integrate our scheme into state-of-the-art implementations without significant overhead, we coordinate TOCAB with load balancing strategies by considering the sparsity of subgraphs. To enable cache blocking for traversal-based algorithms, we consider the benefit and overhead in different iterations with different working set sizes, and apply TOCAB for topology-driven accesses to partial sums, which improves memory access efficiency. We also coordinate our optimization with state-of-the-art load balancing. For traversal-based graph algorithms, we propose to leverage the last level cache (LLC) in the GPU to improve locality. Meanwhile, the graph representation is based on CSR to save global memory space.

KEYWORDS

graph processing, GPU, cache, data locality

1 INTRODUCTION

Analytics and knowledge extraction on graph data structures have become areas of great interest in today’s large-scale datacenters, as social network analysis and machine learning applications have received considerable attention. Many software systems [25, 26, 28, 48] have been developed for this application domain. Graph algorithms are usually embarrassingly parallel, which makes massively parallel accelerators (e.g. GPUs) possible candidates to speedup them. However, efficient graph processing on GPUs is challenging because 1) graph algorithms are irregular and 2) GPUs have highly structured architecture. It is difficult to avoid inefficiency when mapping irregular algorithms to a structured architecture. Specifically there are four major problems for GPU graph processing: (1) low work efficiency, (2) high synchronization overhead, (3) load imbalance and (4) poor data locality.

Lots of previous work have contributed to alleviate the effects of the first three problems, but the poor locality problem has got little attention on GPUs. This is because 1) with thousands of threads running simultaneously, GPUs have relatively much smaller cache capacity per thread compared to CPUs, which makes cache oriented optimization techniques less effective on GPUs, 2) GPU memory hierarchy is quite different from that of CPU, which makes CPU cache optimization techniques not directly applicable to the GPU, 3) GPU L2 cache is usually used as a global synchronization point instead of holding the working set, and GPU programmers tend to use scratchpad for locality issues, and 4) it is hard to capture locality from random accesses in graph algorithms. Fortunately, recent GPUs have shown a trend of including larger caches on chip, making cache oriented optimization a more important role in achieving highly efficient graph processing on GPUs.

In this work, we focus on improving cache performance for graph processing on GPUs. Graph algorithms have poor cache utilization on GPUs due to the random memory accesses to the vertex values. When the graph is large enough, random accesses cause frequent cache misses and long memory access latency. Cache blocking is an optimization technique to improve locality by partitioning a data structure into small blocks such that each block can fit in cache. CuSha [19] is a GPU graph processing framework that uses the idea of cache blocking. It partitions input graphs into shards to fit into the GPU shared memory. This approach leverages fast shared memory in GPUs, but limited by shared memory size it produces too many subgraphs which leads to non-trivial overhead. Meanwhile, CuSha uses a COO-like graph representation that requires roughly 2.5 × global memory space than the typical CSR format. To overcome the limitations, we propose to leverage the last level cache (LLC) in the GPU to improve locality. Meanwhile, the graph representation is based on CSR to save global memory space.

However, naively applying cache blocking on LLC can bring a large volume of inefficient memory accesses on the GPU. In this paper, we design a static cache blocking scheme for both pull and push directions. Our scheme replaces sparse accesses to the global sums with dense accesses to partial sums, which improves memory access efficiency. We also coordinate our optimization with state-of-the-art load balancing. For traversal-based graph algorithms, we consider the iterations in different phases according to their dynamic change of the working set size, and apply our cache blocking
scheme for topology-driven kernels in pull direction. We implement a graph processing framework GraphCage that integrates our proposed optimizations. We evaluate GraphCage on a recent NVIDIA GPU with diverse real-world graphs. Experimental results show that GraphCage achieves speedup of 2× over hand optimized implementations, and 4× over the implementations in state-of-the-art GPU graph processing frameworks Gunrock. Compared to a previous GPU graph partitioning framework, CuSha, GraphCage achieves better performance with less memory consumption.

This paper makes the following contributions:

- We investigate the cache performance of state-of-the-art graph algorithms on GPUs and observe poor cache utilization caused by random memory accesses.
- We propose GraphCage, a cache aware optimization framework for efficient GPU graph processing. The core is a static cache blocking scheme specialized for the GPU.
- We apply our cache optimization with load balancing, and enable it for traversal-based algorithms, to achieve high performance for different applications.
- We measure GraphCage on the NVIDIA GPU and show superior performance over state-of-the-art implementations.

The rest of the paper is organized as follows: Section 2 introduces the background and explains our motivation. The GraphCage design is described in Section 3. We present the evaluation in Section 4. Section 5 summarizes related works and Section 6 concludes.

## 2 BACKGROUND AND MOTIVATION

Recently people have intensively investigated many graph algorithms on various platforms, and proposed plenty of parallel strategies and optimization techniques to make them as fast as possible. Meanwhile, many graph processing frameworks and libraries have been developed to improve the performance and programmability of graph applications targeting CPUs [1, 32, 39, 40, 42] and GPUs [14, 44, 47], by generalizing these proposed optimizations. In this section, we first summarize these strategies and optimizations. We then point out that there is still room for performance improvement even if these sophisticated optimizations have been applied. Finally we briefly introduce cache blocking, and show its limitations when applied to GPU graph processing.

### 2.1 Graph Processing on GPUs

Efficient graph processing on GPUs is notoriously difficult. There has been considerable recent effort in improving the performance of various graphs algorithms on both CPUs and GPUs. Generally, there are four key issues that affect the performance most: 1) work efficiency [2, 15, 17, 27, 31, 43], 2) load balancing [12, 24, 30, 41], 3) synchronization overhead [7, 30], and 4) data locality [4, 5, 9, 46]. Both algorithm-level and architecture-oriented optimization techniques have been proposed targeting one or several of these issues. In this section, we briefly summarize these methods and explain how they are applied on GPUs. We use Fig. 1 as an example to illustrate the basic ideas. Fig. 1 (a) is a directed graph whose CSR format is shown in Fig. 1 (b).

We use vertex-centric model [38] in this work. There are two kinds of graph algorithms: 1) All-active: all the vertices are active in every iteration, i.e. PageRank. 2) Partial-active: only some of the vertices are active in each iteration and the active vertex set is changing during the execution, i.e. BFS. The algorithm converges when the active vertex set is empty. Many graph traversal based algorithms are partial-active, and the frontier queue in the graph traversal is the active vertex set. Optimizations used for all-active and partial-active algorithms may be different because the active vertex set could substantially change the program characteristics.

**Work Efficiency.** It is important to improve work efficiency on a parallel machine (especially on a massively parallel processor) to take advantage of its compute capability. Work efficiency highly depends on how the threads are mapped to the tasks. On GPUs, usually two mapping strategies are utilized: **topology-driven** or **data-driven**, to map the work to the threads [31]. As shown in Fig. 2 (a), the topology-driven scheme assigns a thread to each vertex in the graph, and in each iteration, the thread stays idle or processes a vertex depending on whether its corresponding vertex is active or not. It is straightforward to implement the topology-driven scheme on GPU with no extra data structure. By contrast, the data-driven scheme maintains an active vertex queue which holds the vertices to be processed during a certain iteration. In this iteration, threads are created in proportion to the size of the queue. Each thread is responsible for processing a certain amount of vertices in the queue and no thread is idle, as shown in Fig. 2 (b). Therefore, the data-driven scheme is generally more work-efficient than the topology-driven one when a small portion of the vertices are active, but it needs extra overhead to maintain the queue. Mapping strategies usually work with the **direction optimization** [2] technique to improve work efficiency. Graph algorithms can be implemented in either pull or push direction. Fig. 1 (c) illustrates the traversal order when performing breadth first search (BFS) on the graph in Fig. 1 (a). In level 2 we apply push direction with either a frontier queue (Fig. 1 (d)) or a status array (Fig. 1 (e)). In level 3 pull direction is used (Fig. 1 (f)). This hybrid method dynamically changes the direction to maximize work efficiency for each iteration (level).

**Load Balancing.** Since vertices have different amount of edges to be processed by the corresponding threads, load imbalance becomes an important issue for vertex-centric graph processing, particularly when the input is a scale-free graph in which neighbor sizes of vertices can differ by orders of magnitude. Hong et al. [17]...
proposed a Virtual Warp Centric (VWC) method for BFS to map warps rather than threads to vertices. Since the edges of a vertex are stored continuously, this approach can not only balance the work inside the warp, but also lead to coalesced memory accesses, which improves bandwidth efficiency. As an extension, Merrill et al. [30] proposed a hierarchical load balancing strategy Thread+warp+CTA (TWC) which maps the workload of a single vertex to a thread, a warp, or a thread block, according to the size of its neighbor list. At the fine-grained level, all the neighbor list offsets in the same thread block are loaded on chip, then the threads in the block cooperatively process per-edge operations. At the coarse-grained level, per-block and per-warp schemes are utilized to handle the extreme cases: (1) neighbor lists larger than a thread block; (2) neighbor lists larger than a warp but smaller than a thread block respectively. Fig. 2 (c) shows a load balanced data-driven mapping, where each thread is assigned to process an edge. In this way, the TWC approach can handle vertices with different sizes of neighbor lists. Enterprise [24] further improves TWC with inter-block load balancing for handling extremely high-degree vertices (hub vertices) using the entire grid.

Synchronization overhead. Updating vertex values in parallel may cause conflicts, which requires atomic operations to guarantee correctness. Usually, pull-style operations do not need atomics since vertex values are accumulated by individual threads separately. However, conflicts happen for push-style operations as different threads could write to the same vertex value concurrently. Therefore, for those all-active algorithms, such as PR, pull is usually faster than push as it requires no atomic operation. But when we apply fine-grained load balancing scheme, such as TWC, to pull-style algorithms, conflicts occur among cooperative threads in the thread block, and thus it brings in atomic operations. This leads to significant synchronization overhead which is not acceptable. So usually we only apply coarse-grained load balancing in pull direction. On the contrary, TWC works well for push-style operations as synchronization can not be avoided no matter what strategy is used. Besides, maintaining the frontier queue in partial-active algorithms also requires synchronization [30].

Data locality. Most of the above mentioned optimizations have been incorporated in state-of-the-art graph processing frameworks such as Gunrock [44]. Therefore, graph applications written within the Gunrock framework can achieve excellent performance close to that of hand-optimized implementations. By contrast, CuSha [19] is a framework mainly focusing on partitioning the input graph into shards and therefore can coalesce memory accesses and make good use of the scratchpad. This method is very similar to the propagation blocking technique used in CPU graph algorithms [5, 9]. CuSha can also improve performance compared to non-partitioned implementations. However, since the subgraph size is confined by the size of scratchpad in each SM, each subgraph is small and there are too many blocks generated. This leads to non-trivial overhead on merging partial results of subgraphs.

2.2 Performance Bottleneck on GPUs

The parallel strategies and optimization techniques introduced above have substantially improved the performance of graph processing on GPUs [44]. However, the GPU hardware is still poorly utilized. We conduct a characterization on the GPU using hand optimized PageRank. We observe low hardware utilization, including both the compute units and memory bandwidth. This result indicates that the performance is still limited by memory access latency, even if state-of-the-art optimizations are applied.

The inefficiency of the memory hierarchy is due to the large volume of the input data and the irregular memory access pattern of the data. When executed on a GPU, this large volume of irregular memory accesses can not be coalesced. They are translated into a huge amount of load and store transactions in the memory hierarchy. Demand-fetched caches in GPUs have very limited capacity and are impossible to hold this huge amount of data on chip [18]. This causes the cache thrashing problem [10], leading to a large number of DRAM accesses. Therefore graph algorithms exhibit very poor temporal and spatial locality, although there is plenty of potential data reuses exist in these algorithms [4]. Software managed local memory (or scratchpad) is also not capable to capture the data reuses for these random accesses. On the other hand, since most of the memory requests are sent to DRAM and cause significant memory access latency, the SM pipelines are often

Algorithm 1 PageRank in pull direction

1. procedure Pull(G(V,E))
2. for each vertex \( u \in V \) in parallel do
3. contributions[\( u \)] ← rank[\( u \)]/out_degree[\( u \)]
4. for each vertex \( dst \in V \) in parallel do
5. sum ← 0
6. for each incoming neighbor src of vertex \( dst \) do
7. sum ← sum + contributions[src]
8. sums[\( dst \)] ← sum
9. for each vertex \( u \in V \) in parallel do
10. rank[\( u \)] ← (1-d)/|V| + d ∗ sums[\( u \)]

Algorithm 2 PageRank in push direction

1. procedure Push(G(V,E))
2. for each vertex \( u \in V \) in parallel do
3. contributions[\( u \)] ← rank[\( u \)] / out_degree[\( u \)]
4. for each vertex \( src \in V \) in parallel do
5. contribution ← contributions[src]
6. for each outgoing neighbor \( dst \) of vertex \( src \) do
7. atomicAdd(sums[\( dst \)], contribution)
8. for each vertex \( u \in V \) in parallel do
9. rank[\( u \)] ← (1-d)/|V| + d ∗ sums[\( u \)]
Algorithm 3 Shortest Path Calculation in Betweenness Centrality

1: procedure BC_FORWARD(G(V,E))
2: for each vertex src ∈ Qcurr in parallel do
3:   for each outgoing neighbor dst of vertex src do
4:     if atomicCAS(δ[dst], ∞, δ[src] + 1) = ∞ then
5:       Qnext.push(dst)
6:     if δ[dst] = δ[src] + 1 then
7:       atomicAdd(σ[dst], σ[src])

 stalled waiting for the return of memory requests, which leads to inefficiency of the compute units as well.

To understand the performance bottleneck more specifically, we use PageRank (PR) as an example. PR [36] is a graph algorithm for ranking a website based on the score (rank) of the sites that link to it. PR is iterative; at each iteration, it updates the score of each vertex using the weighted sum of its neighbors' scores and degrees. PR can be implemented in either pull or push direction. Algorithm 1 shows one iteration of pull-based PR (PR-pull), while Algorithm 2 is in push style (PR-push). For each destination vertex, PR-pull gathers contributions from all the incoming neighbors (line 6 & 7) and accumulate them to sums (line 8). On the contrary, PR-push scatters the contribution of each source vertex to all its outgoing neighbors (line 6). Therefore, when implemented in parallel, atomic operations are required (line 7).

For both algorithms, lines from 4 to 7 are the most important, which consume most of the execution time. PR-pull avoids atomic operations, and the sum of incoming contributions will have high locality. But the random memory accesses to the contributions of source vertices (line 7 in Algorithm 1) could have low locality and become the major performance limiter. PR-push requires atomic operations, and therefore is usually slower than PR-pull. In push style, the outgoing contribution will have high locality, but reading (and writing) its neighbors’ sums (destination vertices) could have low locality (line 7 in Algorithm 2), which also causes significant memory latency and limits overall performance.

We use another example, Betweenness Centrality (BC) [29], to show the characteristics of traversal based algorithms such as BFS and SSSP. BC is commonly used in social network analysis to measure the influence a vertex has on a graph. It calculates a betweenness score for each vertex in a graph based on shortest paths. For every pair of vertices in a connected graph there exists at least one shortest path between them. A vertex’s betweenness centrality score is related to the fraction of shortest paths between all vertices that pass through the vertex. A push style data-driven shortest path calculation kernel in BC is shown in Algorithm 3, where δ is the depth and σ is the number of shortest paths for each vertex. The parallel for loop in Line 2 assigns one thread to each element in the frontier queue such that only active vertices in each iteration are traversed. The atomic Compare and Swap (CAS) operation in Line 4 is used to prevent multiple insertions of the same vertex into Qnext. Since this kernel is in push style, it requires atomic to update σ (line 7). In this kernel, random accesses to δ and σ of the destination vertices cause cache thrashing.

2.3 Cache Blocking

Although random accesses can not be avoided anyway, there is still plenty of room for performance improvement if we can make good use of caches by reordering the memory accesses. Cache blocking [8, 33] is such a reordering technique proposed to improve cache performance for dense linear algebra and other applications. By partitioning the graph into small blocks, the range of vertex values in each subgraph is reduced significantly such that the corresponding arrays data for vertex values are small enough to reside in cache, therefore improving the locality [5]. Cache blocking can be done in 1D or 2D, and can be applied to either push or pull direction. Although cache blocking can significantly improve performance for dense matrix computation, naively applying cache blocking to graph processing on GPUs is much less effective. Take PR-pull as an example. Cache blocking for PR-pull divides the adjacency matrix into column blocks. This will improve the locality of reading the neighbors’ contributions (line 7 in Algorithm 1), as the source vertex id (the index of the contributions array) is restricted in the partition, and therefore the corresponding vertex values can fit in cache. But column blocking results in repeated accesses to sums (line 8 in Algorithm 1) for each block. In another word, cache blocking reduces accesses to one data structure at the cost of increasing accesses to another data structure.

Actually, in each subgraph, the number of edges is much fewer than that in the original graph. Many destination vertices may not have edge in a given subgraph since source vertices of this subgraph are restricted in a small range. For these vertices, accessing sums is useless. However, for GPU implementations, even if there is only one thread in a warp has updated sums, there will be a memory write request generated for this update. This memory access pattern is inefficient spatially. When the graph is not very large and it is partitioned into only several subgraphs, these inefficient memory accesses may not be a problem. But when a graph is large enough to have tens of subgraphs or more, this overhead becomes non-trivial and cache blockin achieves only marginal performance improvement or could even lead to slowdowns.

3 GRAPHCAGE DESIGN

In this section, we describe our GraphCage design in a progressive way. We first propose a throughput-oriented cache blocking (TOCAB) scheme which is orchestrated specifically for the GPU architecture. TOCAB is applicable for both pull and push style algorithms. We then integrate TOCAB with load balancing to achieve high performance. Finally, we enable cache blocking for traversal based algorithms by considering the change of working set size.

3.1 Throughput Oriented Cache Blocking

As aforementioned, conventional cache blocking for CPUs is much less effective for GPUs. To enable efficient cache blocking on GPUs, we propose Throughput Oriented Cache Blocking (TOCAB) that is designed for the GPU architecture. At the beginning, we have several design choices to make. First, although modern GPUs have multiple levels of caches with different types (e.g. read-only cache and software managed scratchpad memory), in this work our cache blocking scheme mainly focuses on the last-level cache (LLC), i.e. the L2 cache in most of the modern GPU architectures. This is
reasonable because 1) scratchpads or read-only caches are level-one caches with relatively small capacities, which severely limits the block size of cache blocking; 2) the latency and bandwidth between the LLC and DRAM is typically the performance bottleneck and we are committed to reduce the overall number of DRAM accesses. Note that scratchpad and read-only caches are also useful and we will discuss how to leverage them for locality later.

Second, we apply one dimensional (1D) instead of two dimensional (2D) blocking. This is because 1) transforming the CSR data structure is easier for 1D blocking, which means less preprocessing overhead; 2) 2D blocking partitions the graph on both source and destination vertices, which may generate too many small blocks in total. Smaller blocks result in fewer data reuses to capture and less parallelism for the GPU to exploit, while more blocks lead to more overhead for merging the partial results of each block. When there are too many blocks, the overhead may outweigh the benefit of cache blocking and therefore leads to limited performance improvement or even slowdown. In this case, the block size is actually a tradeoff between locality benefit and blocking overhead. To obtain a scalable block size, we decide to use 1D blocking.

Third, we choose to use static blocking instead of dynamic blocking. Static blocking divides the graph into subgraphs before the execution of the algorithm, and therefore incurs less runtime overhead. By contrary, dynamic blocking [5, 20] uses intermediate buffers to hold the data at runtime, and the data is dynamically distributed into different buffers so that each buffer can fit in cache. The intermediate data is processed separately and then the partial results are accumulated. Dynamic blocking requires no or little modification on the original CSR data structure, but needs a huge memory space for the intermediate buffers. In addition to consuming more memory, dynamic blocking performs additional load and store instructions in order to insert data into the buffers and read data back from the buffers. Note that preprocessing can be applied to reduce this runtime overhead of dynamic blocking, which is a tradeoff between static and dynamic overhead. Anyway, preprocessing (static overhead) is necessary to ensure high performance for both static and dynamic approaches. We choose static blocking to reduce as much dynamic overhead as possible, because 1) most of graph algorithms are iterative and take a large number of iterations, making a case for additional preprocessing time; 2) preprocessing cost is small compared to the significant performance gains; 3) the partitioned graphs can also be reused across multiple graph applications, further amortizing the preprocessing cost; 4) the dynamic operations are simpler after the graph is statically blocked, making it easier to implement on GPUs for different graph applications.

Algorithm 4 Subgraph Processing in pull-style PageRank

1. procedure Pull($G_{sub}^T(V_{sub} \cup E_{sub})$
2. for each vertex $dst_{local} \in V_{sub}$ in parallel do
3. \hspace{1cm} $sum \leftarrow 0$
4. \hspace{1cm} for each incoming neighbor $src$ of $dst_{local}$ do
5. \hspace{1cm} \hspace{1cm} $sum \leftarrow sum + contributions[src]$
6. \hspace{1cm} for each outgoing neighbor $dst$ of $src_{local}$ do
7. \hspace{1cm} \hspace{1cm} $partial sums[dst_{local}] \leftarrow sum$

Algorithm 5 Subgraph Processing in push-style PageRank

1. procedure Push($G_{sub}(V_{sub} \cup E_{sub})$
2. for each vertex $src_{local} \in V_{sub}$ in parallel do
3. \hspace{1cm} $src_{global} = id_map[src_{local}]$
4. \hspace{1cm} contribution $\leftarrow contributions[src_{global}]$
5. \hspace{1cm} for each outgoing neighbor $dst$ of $src_{local}$ do
6. \hspace{1cm} \hspace{1cm} atomicAdd($sums[dst]$, contribution)

Based on these design choices, TOCAB can be divided into three phases. First, the original CSR data structure is modified to store the subgraphs, i.e. the preprocessing phase. Second, each subgraph is processed sequentially, i.e. the subgraph processing phase. Third, the partial results of all subgraphs are reduced to the final results, i.e. the post-processing (reduction) phase. We describe each phase in details as follows.

In the preprocessing phase, we partition the graph into subgraphs so that the vertex values in each subgraph can fit in cache. One technique is to store the subgraphs each as their own graph, which is known as blocked CSR (as shown in Fig. 3). For each subgraph, it has its own CSR data structures (e.g. rowptr and colidx). Computationally, it is easy to generate blocked CSR for each subgraph. For pull model, we do column blocking which takes each edge in the graph and classifies it to the subgraph which its source vertex belongs to. For push model, destination vertex is used instead of source vertex, and therefore we apply row blocking. Note that the code for column blocking (pull) can be reused for row blocking (push), since the input graph of the push model is just the transpose graph of that used in the pull model. This means the same preprocessing code works for both pull and push models with no modification.

However, blocked CSR is not enough to achieve high performance. As mentioned, for pull model, the gain of cache blocking for the low-locality access stream (contributions) comes at the expense of the high-locality access stream (sums). It is critical to reduce the overhead of repeatedly accessing sums. Since only a small portion of destination vertices have incoming edges in each subgraph, to improve efficiency, we ignore the destination vertices with no edges and assign each destination vertices with at least one edge a local-ID. We keep a mapping of this local-IDs in the subgraph to the global-IDs used in the original graph, so that we can always find the global-ID of a vertex when we need to accumulate its partial results. We keep a partial_sums array for each subgraph. The partial results are not directly written into sums, but stored in partial_sums. After all the subgraphs are processed, all the partial_sums are reduced to get the correct sums. Since we use local-IDs instead of global-IDs for destination
vertices, the partial_sums accessed by destination vertices in a given subgraph are stored contiguously in memory regardless of their global-IDs. This is particularly important for GPUs as we can have coalesced memory accesses for the partial_sums. Fig. 4 illustrate how the graph in Fig. 1 is partitioned into two subgraphs and the global-IDs are mapped to local-IDs for the destination vertices.

With this global to local ID transformation, the subgraph processing phase requires little modification on the original pull or push operations. Algorithm 4 and 5 show the operations to process a subgraph in pull and push style respectively. In Algorithm 4, destination vertices use local-ID so that accesses to partial_sums are coalesced (line 6). In Algorithm 5, accesses to contributions use global-ID (line 4), and thus we use the id_map to convert local-IDs into global-IDs (line 3). Since we confine the destination vertices in a small range, the atomic operations on partial_sums happen in the cache (line 6), which substantially speedup the entire phase.

In the accumulation phase, only the pull-style implementation needs to reduce the partial results, because in push direction the contributions are already accumulated into partial_sums as shown in Algorithm 4 line 6. We use a GPU friendly approach for accumulation, as shown in Fig. 5. Since we use local-IDs in the partial results, we need to find the global IDs and accumulate the values to the global results (sums). If different partial results are assigned to different threads, the write accesses will be inefficient, because the global IDs are not consecutive. Our strategy is to divide vertices into equal sized ranges (e.g. 1024), and assign the work of accumulating global results in each range to a thread block. A thread block is responsible to collect data from the specific range of all the subgraphs, and accumulate them in the shared memory. When all the partial results are reduced, the final results of this range are written back to the corresponding position of global memory. In this case, most of the read and write operations happen in the shared memory, while the reads from (partial_sums) and writes to (sums) the global memory are fully coalesced.

![Figure 4: Example of how the graph is partitioned into two subgraphs using source vertices in pull direction. Only vertices that have incoming edges are assigned local-IDs.](image)

![Figure 5: Accumulating partial_sums into sums. $R_j$ is the jth range. $k$ is the range width.](image)

### 3.2 Coordinated Locality and Load Balancing

TOCAB improves memory access efficiency so that we have a cache blocking scheme that works efficiently on GPUs. To achieve high performance, we must integrate TOCAB with other optimization techniques. When we apply TOCAB with load balancing techniques, we find that cache blocking actually affect the load balancing strategy. As aforementioned, for PR-push it is easy to apply fine-grained load balancing, since atomic operations are not avoidable in push direction. However, we only apply coarse-grained load balancing (e.g. VWC) in pull direction to avoid atomics. Our experiment (not shown in the paper) finds that VWC works well for dense-frontier algorithms (e.g PR and SpMV) when the average degree is large (e.g. $d > 16$), because the memory accesses are consecutive and coalesced, and the SIMD lanes are computationally efficient as most of the threads in a warp are working. However, when we partition the graphs into small subgraphs, we find that VWC no longer improves performance when applied to each subgraph. In fact, the average degree of vertices in the subgraphs is smaller than that in the original graph. Table 1 lists the degree distribution of LiveJournal before and after partitioning. In subgraphs more than 90% of the vertices have less than 8 edges and only %3.5 of the vertices have 16 or more edges. Since VWC gets each warp to process one vertex and most of the SIMD lanes in a warp are idle in this case, making VWC inefficient.

To coordinate cache blocking with load balancing, we apply different load balancing strategies in different directions. For the push-style case, whether or not the inner loop is parallelized, atomics are required. So we simply apply TWC in push direction. However, for the pull pattern, parallelizing the inner loop leads to synchronization overhead [15]. VWC is also not suitable due to its low SIMD efficiency. Therefore, we only apply coarse-grained load balancing.

| degree | Original Graph | Subgraphs |
|--------|----------------|-----------|
| 0–7    | 76.7%          | 90.7%     |
| 8–15   | 11.7%          | 5.8%      |
| 16–31  | 7.3%           | 2.3%      |
| 32–    | 4.3%           | 1.2%      |

Table 1: Degree distribution of the original graph (LiveJournal) and subgraphs.
3.3 Work Efficient Cache Optimization

We have discussed our approach for all-active graph algorithms such as PR. However, there are many partial-active graph algorithms, for example, traversal based graph algorithms, such as BFS, BC and SSSP. These algorithms have different characteristics. In each iteration the operator may update the values of only a small subset of vertices. For example, in the first iteration of BFS, only the neighbors of the source vertex have their values updated. Therefore data-driven mapping with a frontier queue is used to avoid unnecessary updates. These differences introduce two extra issues when considering cache blocking: 1) the maintenance of the frontier; 2) the change of working set size.

For a data-driven implementation, when a graph is partitioned into subgraphs, extra operations are required to synchronize the frontier queue, which could be expensive. Another approach is to use topology-driven mapping with status arrays instead of queues, as shown in Fig. 1 (e). Array front is used to show whether the vertices are in the current frontier or not. Array next is used to label the vertices in the frontier of the next level. When we partition the graph, we assign each subgraph a local array. During each iteration, the subgraph processes its vertex array. This is a similar approach used for the partial_sum in PR. So we can perform the reduction of partial results and next in the same kernel.

Since the frontier size is changing in different iterations, the size of the working set is also changing at runtime. At the beginning, there is only one active vertex, the source, in the frontier. And then the queue gets larger as more and more vertices are pushed into the frontier. After several iterations, the queue shrinks until it is empty. The working set size is proportional to the total degree of vertices in the frontier. When the frontier is small, the working set can possibly fit in cache. It is only when the frontier is large enough that cache blocking becomes beneficial.

As direction optimization [2] divides an algorithm into different phases, we also use this hybrid method to enable cache blocking for traversal based algorithms. Take BC as an example. Algorithm 3 is split into three phases: push-pull-push. In the two push phases, the working set is usually smaller than the cache size, which means cache blocking may not be necessary. So we only apply TOCAB in the pull direction. Since the push kernel uses data-driven mapping to achieve work efficiency, this choice also avoids maintaining the frontier queue locally. For the pull kernel, applying TOCAB is the same as PR except updating next array. There are some iterations that run in push direction but have a working set larger than the cache capacity. Our experiment shows that these large push kernels are rare (usually one in each graph). Since the total graph size is confined by the memory size, the assumption is reasonable.

Finally we have a full solution for different kinds of graph algorithms. We integrate the optimizations into a unified framework, GraphCage. Programmers only write basic pull and push kernels to describe the operators for a specific algorithm, and GraphCage can apply cache optimizations to achieve high performance.

4 EVALUATION

We evaluate performance of GraphCage on NVIDIA GTX 1080Ti with CUDA 9.1. The GPU has 3584 cores with boost clock of 1.6GHz. It has a 2.75 MB L2 cache and 11GB DDR5X memory with 484 GB/s bandwidth. We use gcc and nvcc with the -O3 optimization option for compilation along with -arch=sm_61 when compiling for the GPU. We execute all the benchmarks 10 times and collect the average execution time to avoid system noise. Timing is only performed on the computation part of each program.

We select our datasets from the UF Sparse Matrix Collection [13], the SNAP dataset Collection [23], and the Koblenz Network Collection [21] which are all publicly available. Size, density, topology and application domains vary among these graphs. Note that graph layout has a tremendous impact on the locality of the vertex value accesses [5]. In another word, some graphs can benefit from locality optimizations, while some others may not, depending on their data layouts. The fact is that, for some graphs (e.g. social networks), their topologies make it difficult to find a good layout for high locality. Meanwhile, for some situations the time spent on transforming the graph into a locality-friendly layout is not warranted [5]. Therefore, our proposed method is useful in these cases. Our experiment mainly shows the performance improvement on graphs with poor locality, while we also show the performance effect on those graphs with good locality (Hollywood) to indicate that GraphCage only causes trivial slowdown.

In this paper, we use two graph algorithms, i.e. PageRank (PR) and Betweenness Centrality (BC) as graph benchmarks. PR is non-traversal based and all the vertices in every iteration are active, while BC is a traversal based algorithm whose active vertex set (frontier queue) changes in each iteration during the execution. We also include sparse matrix vector multiplication (SpMV) [6] as another benchmark since most of graph algorithms can be mapped to generalized SpMV operations [42].

4.1 Performance Speedup

We first show PR performance improvement by comparing GraphCage with hand-optimized implementations. The baseline (Base) is a
We then apply Virtual-Warp Centric (VWC) [17] method on the base line, which is the second implementation. CB is the naive implementation of conventional cache blocking. We only implement cache blocking for PR. We also implement both PR-pull and PR-push in GraphCage. We run all the PR implementations until they converge with the same condition. Fig. 6 illustrates the performance speedups normalized to the baseline. On average, GraphCage significantly outperforms other implementations. VWC can consistently improve performance with an averaged speedup of 66% because of coalesced memory accesses. But it has little effect on temporal locality. CB works well for relatively small graphs with poor locality. For large graphs, such as Wiki-link and Twitter, it brings very limited benefit. For Hollywood, however, neither CB and GraphCage are able to get too much speedup, since this graph already has a layout with good locality. But GraphCage can substantially improve performance for large graphs, due to a better overhead control of our proposed TOCAB scheme. Since our cache blocking approach works well with load balancing, GraphCage consistently outperforms VWC (2× faster on average) except Hollywood which has a good layout that can benefit a lot from VWC, but not from locality optimizations. GC-pull and GC-push get similar average speedups, but have some difference for specific graphs. This is because GC-push has more overhead on atomic operations but its load balancing scheme is better than GC-pull.

We also evaluate the performance of SpMV and BC. Fig. 7 shows the speedups of SpMV implementations over the baseline. We can still observe consistent performance improvement for VWC and GraphCage. Compared to the baseline, VWC achieves more speedup (2.3× on average) for SpMV than PR because not only the column indices but also the matrix values are coalesced. The matrix values have no reuse opportunity, and could pollute the last level cache by replacing useful data. Therefore, GC-pull is less effective for SpMV compared to VWC. Since the effect of load balancing for SpMV is more significant than that for PR, we can observe better performance for GC-push than GC-pull, since fine-grained load balancing is applied to GC-push, but not GC-pull. On average, GC-push achieves 82% performance improvement over VWC.

Fig. 8 illustrates BC performance normalized to the baseline. Since we only applied TOCAB to the pull kernels, we have only one implementation for BC in GraphCage. The baseline is still a naive implementation, but we apply TWC in the second implementation since TWC works better than VWC for BC. We can still observe consistent improvement for TWC and GraphCage with averaged speedup of 2.8× and 4.1×. A special issue here is that for large-diameter graphs, Wiki2007 and Wiki-link, GraphCage has limited improvement over TWC. This is because there are lots of iterations in these graphs have only one vertex in the frontier, For these iterations, GraphCage does not bring any benefit. Time spent on these iterations makes the improvement on other iterations less significant. However, we can still observe an average speedup of 46% for GraphCage compared to TWC.

### 4.2 Cache and Memory Efficiency

To relate the total performance improvement to the cache behavior, we conduct experiments on cache miss rates and memory efficiency. Fig. 9 shows the L2 cache miss rates for all the implementations in Fig. 6. It is quite clear that Base and TWC suffer tremendous cache misses with up to about 80% miss rate. In this case, the L2 cache is definitely poorly used and it could become a bottleneck in
4.3 Sensitivity to Subgraph Size

We vary the subgraph size to determine its impact on GraphCage’s performance. When the subgraphs are small enough to keep the vertex values reside in the cache, the memory efficiency is high, since most of the vertex value accesses hit in the cache instead of going to the DRAM. However, if the subgraphs are too small, there will be numerous subgraphs, which brings more overhead on merging the partial results of the subgraphs. Thus the performance will not be good. On the other hand, when the subgraph size becomes too large, the vertex values data no longer fit in the cache, and the memory efficiency drops increasingly. Therefore, the subgraph size is a trade-off between locality benefits and the overhead of partitioning. For our platform, we select a subgraph size of 256 vertices, since it makes a good trade-off and achieves best performance.

4.4 Comparing with Other Frameworks

We compare GraphCage with the state-of-the-art GPU graph processing framework Gunrock [44], and another graph partitioning framework on GPUs, CuSha [19]. The averaged execution time of one PageRank iteration is listed in Table 3. We use the runtime of one iteration instead of runtime of convergence because CuSha uses a different convergence condition. We can observe that GraphCage substantially outperforms Gunrock for all the graphs with poor locality, especially those graphs with large average degrees which have great potential to enjoy locality optimizations. On average, GC-pull and GC-push achieve 4.0× and 3.6× speedup over Gunrock for our tested graphs, respectively. Since there is no cache blocking technique applied in Gunrock to improve cache performance, this dramatic improvement is expected. For CuSha, however, it partitions graphs into Shards to fit into the shared memory, which also improves performance for LiveJ, Kron21 and Orkut. It is extremely inefficient for the two wiki graphs which have large diameters. This issue could be caused by the difference of convergence condition. However, GraphCage is still faster or as fast as CuSha for other graphs, because of the overhead of relatively small partitions in CuSha. Table 4 lists the number of partitions in GraphCage and CuSha. Last but not least, CuSha fails to run
Table 3: Averaged execution time (ns) of one PageRank iteration. GraphCage significantly outperforms prior work.

|                      | Subgraphs | Shards |
|----------------------|-----------|--------|
| LiveJ                | 19        | 789    |
| Wiki2007             | 14        | 1162   |
| Flickr               | 9         | 750    |
| Wiki-link            | 47        | 1978   |
| Hollywood            | 5         | 743    |
| Kron21               | 8         | 1366   |
| Orkut                | 12        | 1952   |
| Twitter              | 82        | 3467   |

Table 4: Comparing the number of subgraphs in GraphCage and the number of Shards in CuSha. Since GraphCage tiles the data for the L2 cache, it has much fewer partitions.

Twitter on GTX 1080Ti because it requires more global memory than the GPU provides. This is also very important as global memory in GPUs is scarce resource and GraphCage can provide more stable performance with less global memory requirement than CuSha. We also compare GraphCage with other available implementations. For example, we compare SpMV with cuSPARSE [34] and nvGRAPH [35]. GraphCage also significantly outperforms these commercial libraries.

5 RELATED WORK

There are plenty of previous work on dynamic cache blocking targeting push-style graph processing on CPUs. Beamer et al. [4] proposed Propagation Blocking (PB) [5] for PageRank. They split the computation into two phases, binning and accumulation. In the binning phase, intermediate data is distributed into different buffers (bins) whose sizes can fit in the cache. And then buffers are processed sequentially in the accumulation phase to merge the results. Similar approach is used to improve the performance of SpMV kernel in graph analytics applications [9]. milk is a language extension on OpenMP [20]. It automatically collects indirect memory accesses at runtime in order to improve locality. Comparing to these dynamic schemes on CPUs, our design use static cache blocking to reduce runtime overhead as much as possible.

Zhang et al. propose CSR segmenting [46], an efficient 1D static cache blocking technique for multicore CPUs. CSR segmenting partitions a graph into segments, each of which can fit in the cache. They also propose a merge phase to accumulate the partial partitions a graph into segments, each of which can fit in the cache. And then buffers are processed sequentially in the accumulation phase to merge the results. Similar approach is used to improve the performance of SpMV kernel in graph analytics applications [9]. milk is a language extension on OpenMP [20]. It automatically collects indirect memory accesses at runtime in order to improve locality. Comparing to these dynamic schemes on CPUs, our design use static cache blocking to reduce runtime overhead as much as possible.

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6 CONCLUSION

Data locality is a key performance issue for graph processing. In this paper, we point out that there is a chance to improve locality as well as performance of GPU graph processing by leveraging the last level cache. We first propose a throughput oriented cache blocking (TOCAB) approach for the GPU architecture which improves memory access efficiency compared to naively applying conventional cache blocking scheme. Then we coordinate our cache blocking scheme with state-of-the-art load balancing scheme with awareness of the sparsity of subgraphs. Finally we apply our scheme to traversal based graph algorithm by considering both the benefit and overhead of cache blocking. These optimization techniques are integrated into our graph processing framework, i.e. GraphCage, to support various graph applications. Experimental results show that...
GraphCage can significantly improve performance over previous best-performing implementations and state-of-the-art graph processing frameworks such as Gunrock and CuSha, with less memory space requirement than CuSha. With the continuous increasing of GPU last level cache size, our proposed approach will be more effective and important for graph processing on GPUs in the future.

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