CAMAC based 4-channel 12-bit Digitizer

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Abstract. With the development in Fusion research a large number of diagnostics are being used to understand the complex behaviour of plasma. During discharge, several diagnostics demand high sampling rate and high bit resolution to acquire data for rapid changes in plasma parameters. For the requirements of such fast diagnostics, a 4-channel simultaneous sampling, high-speed, 12-bit CAMAC digitizer has been designed and developed which has several important features for application in CAMAC based nuclear instrumentation. The module has independent ADC per channel for simultaneous sampling and digitization, and 512 Ksamples RAM per channel for on-board storage. The digitizer has been designed for event based acquisition and the acquisition window gives post-trigger as well as pre-trigger (software selectable) data that is useful for analysis. It is a transient digitizer and can be operated either in pre/post trigger mode or in burst mode. The record mode and the active memory size are selected through software commands to satisfy the current application. The module can be used to acquire data at high sampling rate for short time discharge e.g. 512 ms at 1MSPS. The module can also be used for long time discharge at low sampling rate e.g. 512 seconds at 1KSPS. This paper describes the design of digitizer module, development of VHDL code for hardware logic, Graphical User Interface (GUI) and important features of module from application point of view. The digitizer has CPLD based hardware logic, which provides flexibility in configuring the module for different sampling rates and different pre/post trigger samples through GUI. The digitizer can be operated with either internal (for testing/acquisition) or external (synchronized acquisition) clock and trigger. The digitizer has differential inputs with bipolar input range ±5V and it is being used with sampling rate of 1 MSamples Per Second (MSPS) per channel but it also supports higher sampling rate up to 3MSPS per channel. A user-friendly GUI has been developed in LabView as well as LabWindows/CVI application software for acquisition through developed hardware.

1. Introduction
The time duration of tokamak discharge has been prolonged in accordance with the development of fusion research. In the next generation tokamak like SST-1 and ITER [1] the discharge time of the order of 1000 sec. is planned. At the same time demand for more no. of acquisition channels from different diagnostics is increasing. A CAMAC Digitizer module has been designed and developed to acquire data at sampling rate up to 3MSPS with 12-bit ADC resolution and on-board RAM per channel for long-time discharge. With the use of this digitizer module, more number of channels can be accommodated per CAMAC crate. The module has dedicated ADC per channel for simultaneous sampling and digitization. The module has several important features for application in CAMAC based nuclear instrumentation.
2. Hardware description

This high-speed 12-bit CAMAC digitizer module is designed to cater the acquisition requirements of fast plasma diagnostics, which demand high sampling rate to acquire data for rapid changes in plasma parameters. The designed digitizer has CPLD based hardware logic for design flexibility and four independent acquisition channels with software selectable sampling rate up to 1MS/s per channel, 512 KSamples RAM per channel for on-board storage and selectable acquisition window size. The digitizer can be operated with internal or external clock as well as trigger and the different clock frequency are available on the board, which can be selected through software CAMAC command. The hardware design of module is presented as block diagram in figure 1. The block diagram shows how various elements are connected to various buses for achieving the following described functions:

- CAMAC access to program various registers
- Transfer of data from ADC to memory (SRAM)
- Transfer of data from memory to CAMAC backplane (Dataway)
- Clock Generation
- Control Logic Generation

![Figure 1. Block Diagram of 4-channel CAMAC Digitizer.](image)

2.1. Clock Generator

A crystal-based clock generator is used to generate the on-board clock (TTL level internal clock). A 10 MHz crystal is used to give the basic clock of 10 MHz. The crystal-based circuit provides the most stable clock. To synchronize the operation with other sub-systems, there is a provision for TTL level external clock through front panel LEMO connector. The basic clock is divided in to different frequency clock through the CPLD based logic circuit. Present module VHDL code supports 4 different frequency clocks for sampling rate (1 MHz, 500 KHz, 250 KHz and 125 KHz) but through external clock we may go for any sampling rate value up to 3MSPS. The clock can also be distributed to all modules in the CAMAC crate through CAMAC Dataway. Either internal or external clock can be used for digitization through software selection.

2.2. Analog Circuit

An Instrumentation amplifier is used to interface the differential input to the ADC (Analog to Digital Converter). Instrumentation amplifier provides very high input impedance. Also an attenuator circuit, with buffering, is also used in between instrumentation amplifier and ADC to provide suitable range to ADC input. Hence this unit makes the input signal compatible to ADC input requirement.
2.3. ADC and On-board memory (SRAM)
A dedicated 12-bit ADC has been used for each channel for high-speed simultaneous sampling. A 512K sample (16-bit sample) SRAM (Static Random Access Memory) in each channel is used for on-board data storage. The local RAM allows data from different channels to be archived without costly computer supervision. Depending upon the requirement, the memory can be segmented to enhance read operation. The usable memory size is programmable (512K, 256K, 128K and 64K). The ADC output goes to SRAM through buffer. Another buffer is used for CAMAC Read lines interface with SRAM.

2.4. Module Operation Control Logic Circuits
Module Operation Control logic circuits are configured in the CPLD (Complex Programmable Logic Device) to control proper module functioning. CPLD device provides the design flexibility and saves the component space on the board. It also provides the flexibility for various hardware settings through software e.g. Sampling rate selection, Pre/Post trigger samples, internal/external clock and trigger etc. The hardware logic circuit has been developed with VHDL code and CPLD as target device. The circuit controlling commands are either issued by computer or generated by circuit itself [2]. Various Control signals are generated from CPLD for different components e.g. sampling clock, memory read/write, and buffer enable etc.

2.5. CAMAC Interface Circuits
These are the interfacing circuits between digitizers and CAMAC backplane (Dataway). These include read and write line buffers, CAMAC control/Acknowledgement signal generation circuits etc. We have used CPLD as reconfigurable device to perform the desired hardware logic function through VHDL code.

3. Functional sequence of module operation
The proper operation of module is governed by a set of CAMAC Function commands. Figure 2 shows the functional sequence of module operation. CAMAC Function Commands are used to reset the circuit, to configure sampling clock rate, to select type of clock and trigger (internal or external), to select pre/post trigger data, to read data from module etc.

![Figure 2. Functional Sequence of CAMAC Digitizer](image-url)
With Start (powering on), first of all, the module digital logic circuit gets reset through command (CAMAC command) and various hardware settings (configuring module), like selection of sampling rate, pre trigger samples etc.; are done through CAMAC commands. The designed module is a transient digitizer, which has been designed to operate in either Burst mode or Pre/Post Trigger Mode [3]. Both modes require a trigger to synchronize the acquisition. The mode is selected through software. The concept adopted here to develop the transient digitizer is Circular Buffering of memory. In RUN state module digitizes the input channel and stores the data in RAM. The RAM address counter is running in circular manner and overwriting the old sample. On receipt of the trigger the digitizer writes number of samples in memory as selected by post trigger sample count. The remaining samples (post trigger samples subtracted from usable memory size) will be latest pre-trigger samples. If we stop memory address counter at this place, then while reading data from memory we will get pre-trigger samples first followed by post trigger samples in array. Present module VHDL code supports 4 different Pre trigger samples selection (256, 512, 1K and 2K samples).

4. Graphical User Interface
A user-friendly GUI has been developed with LabView as well as LabWindows/CVI application software for acquisition through developed hardware. This provides a convenient display of acquired data for all channels with zoom facility. The digitizer has CPLD based hardware logic, which provides flexibility in selection of different sampling rate and pre/post trigger samples through GUI.

5. Results & Discussion
The developed module has been tested in CAMAC data acquisition system with precise test and measurement equipments. The testing has been performed with GUI developed in LabVIEW as well as LabWindows/CVI application software. We have found no phase shift between channels. We have configured the module through software commands for different pre/post trigger samples and then verified the plotted acquired data for these exact pre/post trigger numbers. We have tested the DC performance as well as AC performance of digitizer with utility developed in LabVIEW software that includes time domain plots, histograms, and the FFT analysis. We have found the results quite satisfactory and close to ADC specifications. Figure 3 and figure 4 show pre/post trigger acquisition and simultaneous sampling acquisition respectively.

6. Conclusion
The main aim, of this work, was to develop a multi-channel, simultaneous-sampling 12-bit digitizer to cater the data acquisition needs of several plasma diagnostics. The module provides the flexible, cost
effective solution for CAMAC modular instrumentation. Full programmability of this digitizer with on-board memory per channel in single width CAMAC module offers versatile solutions for many applications in CAMAC based nuclear instrumentation. The module can be configured for other feasible requirements by modifying VHDL code. Similarly the Graphical User Interface can be modified for advanced acquisition and data analysis requirements.

References
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