Discovering Multi-Hardware Mobile Models via Architecture Search

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Abstract. Developing efficient models for mobile phones or other on-device deployments has been a popular topic in both industry and academia. In such scenarios, it is often convenient to deploy the same model on a diverse set of hardware devices owned by different end users to minimize the costs of development, deployment and maintenance. Despite the importance, designing a single neural network that can perform well on multiple devices is difficult as each device has its own specialty and restrictions: A model optimized for one device may not perform well on another. While most existing work proposes different models optimized for each single hardware, this paper is the first which explores the problem of finding a single model that performs well on multiple hardware. Specifically, we leverage architecture search to help us find the best model, where given a set of diverse hardware to optimize for, we first introduce a multi-hardware search space that is compatible with all examined hardware. Then, to measure the performance of a neural network over multiple hardware, we propose metrics that can characterize the overall latency performance in an average case and worst case scenario. With the multi-hardware search space and new metrics applied to Pixel4 CPU, GPU, DSP and EdgeTPU, we found models that perform on par or better than state-of-the-art (SOTA) models on each of our target accelerators and generalize well on many un-targeted hardware. Comparing with single-hardware searches, multi-hardware search gives a better trade-off between computation cost and model performance.

Keywords: multi-hardware, mobile models, neural architecture search

1 Introduction

Developing efficient on-device neural networks has become an important topic in computer vision with many real-world applications. Having models that can be fully deployed on device not only enables fast, real-time results, but also avoids exposing personal data to public servers.

Given the resource constraints of a portable device, such as latency, energy and memory footprint, on-device models need to be fast and small. While the
number of multiply-and-add operations (MAdds) and the number of parameters have been widely used to optimize efficient models \cite{18,11,35,27,31}, recent research has shown that improvements on theoretical MAdds or number of parameters do not always translate into better latency on real hardware, and can actually be counterproductive in some cases \cite{30,26}. Thus, optimizing directly on latency measurements becomes important when we want to find a fast model on device \cite{14,3}.

Unlike MAdds or the number of parameters, latency is highly dependent on hardware (and its associated software). A neural network optimized for a specific hardware platform may perform sub-optimally on a different one in terms of inference efficiency. This brings about challenges when practitioners try to decide which neural network to adopt, especially when the models are to be deployed on many different types of hardware, such as across the Android ecosystem which covers a wide variety of different phones.

Having a single neural network that runs effectively across diverse hardware platforms would be the most favorable choice for applications, as it is the simplest solution to eliminate major concerns of the developers, and will likely have significant impact in maintaining the quality of the model regardless of their underlying hardware. For example, since different models have different accuracy and failure modes, if one application has to use different models on different hardware, it requires the application to manually fine-tune user-visible components (such as a score threshold to determine whether to give a user an action suggestion) that interact with the model, increasing overall cost and complexity. Having a single model is also beneficial for run time scheduling where an application may choose to move the inference from one hardware to another as a function of dynamic workload.

This paper represents the first effort to explore the problem of finding a single model that works well across multiple hardware platforms. To achieve this goal, we first introduce the concept of multi-hardware search space which is compatible for all examined hardware platforms. Then, two multi-hardware metrics are

Fig. 1: Average and worst case performance of our proposed models comparing with SOTA models, where our multi-hardware models, Multi-MAX and Multi-AVG, achieve better results than SOTA models on overall metrics. See Section 5.2 for details of the metrics on the x-axis.

This paper represents the first effort to explore the problem of finding a single model that works well across multiple hardware platforms. To achieve this goal, we first introduce the concept of multi-hardware search space which is compatible for all examined hardware platforms. Then, two multi-hardware metrics are
proposed to measure average and worst case performance of a model in multiple deployment scenarios. To demonstrate the effectiveness of our methodology, we examine all five hardware on a Pixel 4 phone as a case study: CPU floating point and 8 bit quantized (uint8), mobile GPU, Qualcomm’s DSP and Google’s EdgeTPU. By leveraging multi-hardware architecture search, we find models that work on par or better than each of the SOTA models on CPU uint8, GPU, DSP, EdgeTPU, and rank the second among six SOTA models on CPU float while the top model cannot run on certain other accelerators at all. As shown in Fig. 1, the new multi-hardware models give the best results on both proposed multi-hardware metrics. More analysis will be given in Section 6.3.

2 Related Work

Designing efficient neural networks has been a popular research topic in the past years. MobileNets [15, 25, 14], SqueezeNets [18, 11] and ShuffleNets [33, 22] are just a few examples. Various techniques have been proposed to make models efficient, such as new efficient operations [29, 17, 33] and architecture pruning [12, 31, 32].

As the divergence of hardware has been taken into consideration, researchers began to explore hardware-aware models. NetAdapt [30] uses empirical latency tables of the target hardware to greedily adapt a model to its highest accuracy under a target latency constraint. MnasNet [26] also uses latency tables, but applies reinforcement learning to do hardware-aware architecture search. FBNet [28] and ChamNet [8] find the best architecture for targeted hardware by incorporating latency table and resource predictive models in architecture search respectively. MoGA [7] optimizes a model for GPU. Once-for-all [4] proposes a pre-trained super-model where different sub-models can be extracted for different hardware.

Many success of hardware-aware designs leverage the technique of neural architecture search (NAS) [34, 35, 32, 26, 3] as the unpredictable hardware performance of a model makes it challenging to optimize models by hand. This technique uses reinforcement learning [34], evolutionary search [24], differentiable search [20, 21] or other algorithms [10] to find the best neural architecture according to a predefined reward function which incorporates both accuracy and application constraints. TuNAS [3], as one of the most recent efficient NAS techniques, will be adopted in this paper to accomplish our goal. Like ProxylessNAS [5], TuNAS uses a weight sharing model in combination with a reinforcement learning controller. In addition, TuNAS uses other optimizations, such as operation and filter warm-up, to make it work reliably across multiple large search spaces.

3 Challenges of Finding A Single Model for Multiple Hardware

While it is highly desired to have a single model for multiple hardware, designing such model has many challenges.
3.1 Different Devices Prefer Different Design Choices

Due to the unique design of each hardware, their specialties are usually different, which may yield different directions of optimization. To demonstrate this, we take the MobilenetV3 Large minimalistic model \cite{1} and run per layer profiling on CPU (uint8) and DSP (Qualcomm 855 Hexagon) to get the latency percentage of each layer over the whole model (Fig. 2). On CPU, a larger fraction of the model’s total latency comes from the earlier layers of the network, while on DSP, a larger fraction of the total latency comes from the later layers. Therefore, when optimizing on CPU, one may focus mainly on the early layers, while later layers may gain more attention when optimizing for DSP.

![Fig. 2: Per layer profiling of MobileNetV3 minimalistic on Pixel4 CPU uint8 and DSP. The leftmost is the input layer while the output layer is on the right.](image)

3.2 Different Supporting Levels of the Same Operation

While new operations and model blocks have been proposing to improve accuracy and latency trade-offs \cite{16,33,15,14}, not all of them are equally efficient on different hardware. For example, the depthwise separable convolution that was proposed in MobileNet \cite{15} to replace the regular convolution reduces MAdds and makes model inference more efficient on CPU. However, a decrease in MAdds does not always lead to a decrease in on-device latency, especially for accelerators which have been optimized specifically to handle large number of computations as long as they follow certain pattern \cite{6}. For example, \cite{13} indicates that EdgeTPU favors regular convolution over depthwise separable convolution in certain layers of the model as the former can utilize the hardware resources better and gives better latency-accuracy trade-offs. This makes it hard to manually decide what operation to use at which layer if we want to have a single model that works well on both CPU and EdgeTPU.

3.3 Different Latency Relationships Among Different Models

It is well known that a model has different latencies when running on different hardware, but is the relationship similar for all models? That is, if a model runs $2 \times$ faster than another on one hardware, 1) will it still run faster on another hardware? 2) if faster, will it still be $2 \times$ faster? To answer this questions, we take four mobile models, MobileNetV1 \cite{15}, MobileNetV2 \cite{25}, MobileNet EdgeTPU \cite{13}, ProxylessNAS mobile \cite{5}, and benchmark them on different hardware to
see whether the latency ratio among them are the same. Fig. 3 shows the results, where the latency ratio among different hardware are obviously different for each model. Furthermore, while EdgeTPU runs MobileNet-EdgeTPU model faster than ProxylessNAS-Mobile, CPU executes ProxylessNAS-Mobile faster than MobileNet-EdgeTPU.

Fig. 3: Latency of different models on different hardware in Pixel4 phone.

4 Problem Formulation

The divergence of hardware mentioned above makes it extremely hard to manually handcraft a single model to accommodate the traits of all examined hardware. Specifically, we want to answer the following questions: Which part of the neural network should we optimize? Which operation should be used in which layer of the neural network? How do we balance the performance for each hardware? How do we know a model is better than another in a multi-hardware optimization?

In this paper, we leverage neural architecture search to solve above questions, where we propose a multi-hardware search space that is supported by all examined hardware and two metrics to measure the overall latency performance over multiple hardware to determine which model is better in multi-hardware optimization.

Let $\mathcal{H} = \{H_1, H_2, ..., H_N\}$ be the set of hardware we want to optimize for. For $0 < i \leq N$, $S_i$ denotes the set of neural network architectures that $H_i$ can support, i.e., the entire network can fully run on this hardware without falling back to another slower hardware. Then, a multi-hardware search space, denoted as $S^\mathcal{H}$, is a set of neural network architectures that belongs to the intersection of supported architectures of the set of examined hardware. Mathematically,

$$S^\mathcal{H} \subseteq S_1 \cap S_2 \cap \cdots \cap S_N.$$  \hfill (1)

Note that, we allow the multi-hardware search space to be a subset of instead of equal to the intersection of all supported architectures, by taking into account the practical size limit for efficient architecture search.

In order to find a single model optimized for multiple hardware, we need metrics to determine what is a better model. Without loss of generality, we examine models’ accuracy and latency to compare different models, as the Pareto optimal on these two metrics has been broadly used in single-hardware architecture optimizations \cite{283115}. Specifically, model $a$ is better than model $b$ in single-hardware optimization iff
\[ L_a < L_b \text{ when } A_a \approx A_b, \quad (2) \]

where \((L_a, A_a)\) and \((L_b, A_b)\) are the (latency, accuracy) measurements of model \(a\) and \(b\) on the examined single hardware, respectively.

When considering multi-hardware optimization, the biggest challenge is how to compare models given their latency measurements on various hardware. Let \(L_a = \{L_{a,1}, L_{a,2}, \ldots, L_{a,N}\}\) denote the latency of model \(a\) on \(H\). Similarly for model \(b\). We need some overall metric function \(f^H(\cdot)\) such that, if

\[ f^H(L_a) < f^H(L_b) \text{ when } A_a \approx A_b, \quad (3) \]

we say that model \(a\) is better than model \(b\).

As shown in Section 3.3, latency on different hardware may have different scales, thus \(L_{a,i}\) needs to be normalized before any calculation. In this paper, we propose two intuitive metrics to measure the average and worst case performance of a model on multiple hardware. Specifically, the normalized average latency over \(H\) is defined as

\[ f^H_{\text{avg}}(L_a) \equiv \frac{1}{N} \sum_{i=1}^{N} \frac{L_{a,i}}{C_i}, \quad (4) \]

and the normalized max latency over \(H\) is defined as

\[ f^H_{\text{max}}(L_a) \equiv \max_i \left( \frac{L_{a,i}}{C_i} \right), \quad (5) \]

where \(C = \{C_1, C_2, \ldots, C_N\}\) are normalization factors. While there are many ways of choosing \(C\), we discuss two common cases as follows.

1. \(C\) can be chosen as the latency of a reference model on \(H\) to represent the latency scaling relationship among hardware. In addition, if the normalized average latency of a model is 0.5, it implies that, on average, the model runs in half of the time of the reference model.

2. On top of the natural latency scaling difference among hardware, one can further re-weight \(C\) with the importance of each hardware in \(H\). An extreme case would be to set all norm factors to be \(\infty\) except one \(C_1 = 1\). Then \(f^H(L_a) = L_{a,1}\), which regresses the problem to a single hardware optimization.

Remark: This paper mainly focuses on mobile models as cross device application is the most common use case of multi-hardware models. However, the methodology introduced here can be easily generalized to discover multi-hardware server sized models when needed.

5 A Case Study on Finding a Multi-Hardware Model for Pixel4 via NAS

With the essential concepts defined above, we use a case study to demonstrate how to find multi-hardware model via architecture search. Here, we consider all 5 hardware inside a Pixel4 phone: CPU float, CPU uint8, GPU (Qualcomm Adreno 640), DSP (Qualcomm Snapdragon 855), EdgeTPU (Google). We choose this set of hardware because
1. it covers various types of hardware from different manufacturers;
2. the obtained multi-hardware model will perform well on all hardware on Pixel4, so that even when an application chooses to move its inference from one hardware to another, it does not introduce too much performance degradation.

Among the various architecture search schemes, we use the latest one, TuNAS [3], in this paper, while others can also be adopted for the same purpose.

5.1 Multi-Hardware Search Space

As Pixel CPU float is one of the target hardware, we start constructing the search space from MobilenetV3 Large model which was obtained by optimizing for this single hardware [14]. We make the following adjustments to guarantee that the multi-hardware search space is both exclusive enough so that each searched operation is supported by all examined hardware, and inclusive enough so that it searches over a variety of effective (and supportive) operations for each examined hardware.

- Do not include Squeeze and Excite (SE) [16] as it is not supported in EdgeTPU. Table 1 shows that, while SE is well supported by CPU float, it introduces large overhead on DSP and is not supported by EdgeTPU at all.
- Do not include H-swish activation [14] due to the same reason as SE above. Replace it with ReLU activation.
- Adjust all filter sizes to be integer multiples of 32 instead of 8 as recommended for accelerating on DSP [2].
- Include fused inverted bottleneck, which replaces the expansion 1x1 convolution and depthwise conv in regular inverted bottleneck [25] with a single regular convolution, in search as it has been proven to be efficient on EdgeTPU [13].

Table 1: How much slower the model would be when adding SE blocks.

|                | CPU float | CPU uint8 | DSP   | EdgeTPU               |
|----------------|-----------|-----------|-------|-----------------------|
| Mobilenet V2   | 25.2ms    | 11.7ms    | 4.08ms| 2.32ms                |
| Mobilenet V2 with SE | 27.2ms | 14.3ms    | 5.61ms| not supported         |
| Increased %    | 7.9%      | 22.2%     | 37.5% | -                     |

With these adjustments, our multi-hardware search space can be summarized as follows:

- It is based on MobilenetV3 Large model’s blocks without SE nor h-swish.
- Filter sizes are adjusted to be integer multiples of 32.
- Search over number of repeated blocks per stage from {1, 2, 3, 4}, where stage is defined as a sequence of consecutive layers that share the same output resolution and filter size [263].
- Search over input and output filter sizes in the main body (excluding the first layer and model head). Possible change ratios w.r.t. the centered model are {0.5, 0.625, 0.75, 1.0, 1.25, 1.5, 2.0}.
Each block can choose either regular inverted bottleneck or fused inverted bottleneck. 
Search over expansion ratio from $\{1, 2, 3, 4, 5, 6\}$. 
Search over kernel sizes 3x3 and 5x5 for convolutions.

Note that we decide not to search the input/output filter sizes in the model head because in early experiments we found that, the RL controller was biased towards using large numbers of filters in the model head which blew up the model size but with marginal accuracy improvement. One can achieve a similar effect by restricting the filter size change in a smaller range on these last layers, or consider adding an explicit constraint on the number of parameters into the search algorithm.

5.2 Mobilenet Normalized Average and Max Metrics

Given we are optimizing for mobile models, we choose to use MobilenetV1 as our reference model to calculate the overall metrics, i.e., use its latency on the examined hardware as the normalization factors $C$ in equation (4) and (5). More specific reasons to choose this reference model are:

- it has been around for a few years and yet is still widely used;
- it is publicly available in multiple formats (TFLite, Caffe, etc.) for ML researchers to run benchmarks with;
- it is simple enough that it can run on a wide variety of hardware.

We do not have a particular preference on having better performance on some of the optimized hardware, so no extra re-weights were assigned to these normalization factors.

The reward function used in architecture search needs to be adjusted with these new metrics too. In TuNAS, single hardware search maximizes the following reward function [3]:

$$ r(\alpha) = A(\alpha) + \beta \left| \frac{L(\alpha)}{L_0} - 1 \right|, $$

where $\alpha$ represents an architecture, $r(\cdot)$, $A(\cdot)$ and $L(\cdot)$ are reward, accuracy and latency of the architecture, respectively. $|\cdot|$ is absolute function. $L_0$ denotes latency target. $\beta < 0$ is an application-specific constant.

To search for multi-hardware models, the reward function becomes

$$ r_{\text{avg}}(\alpha) = A(\alpha) + \beta \left| f^H_{\text{avg}}(\alpha) - 1 \right| = A(\alpha) + \beta \left| \frac{1}{N} \sum_{i=1}^{N} \frac{L_i(\alpha)}{C_i} - 1 \right|, $$

when optimizing for average performance; and

$$ r_{\text{max}}(\alpha) = A(\alpha) + \beta \left| f^H_{\text{max}}(\alpha) - 1 \right| = A(\alpha) + \beta \left| \max_i \frac{L_i(\alpha)}{C_i} - 1 \right|, $$

when optimizing for worst case performance. Note that when optimizing for average performance, the reward function implies a prior that the searched architecture should, on average, have latency close to that of the reference model MobilenetV1.
6 Experiments

6.1 Experimental Setup

Latency benchmarks: In this paper, 3 phones with totally 10 different hardware will be used in either searching for the multi-hardware model or evaluating the model on unsearched hardware. The driver’s versions for these phones are: Pixel4 uses QQ1B.200205.003; Pixel3 uses QQ1A.200205.002; MediaTek Dimensity 1000 5G uses QP1A.190711.020.

The delegates used for accelerators are: GPU’s latency was obtained from Jet delegate using OpenCL; DSP’s latency was from Hexagon delegate which directly calls the Qualcomm’s binary with less overhead than Android NNAPI; EdgeTPU’s latency and APU’s latency were obtained by using NNAPI delegate.

TF-Lite models with single-thread and batch size of 1 were used to get all benchmarking results. When getting CPU’s latency, only the large cores were used. When benchmarking on CPU uint8, DSP, EdgeTPU and APU, where quantized models are needed, fake quantization was applied \(^1\). Cost models: As required by TuNAS, each searched hardware, Pixel4 CPU float/uint8, GPU, DSP and EdgeTPU, needs a cost model (a linear model between architecture encoding and its latency) trained before search to reduce search overhead. 9K pairs of (architecture, latency) data were used to train the cost model for each hardware, except for EdgeTPU where we used 20K to achieve the similar quality.

While we always use real time benchmarks to evaluate baseline models and the newly searched models, when generating data for training cost models, we obtained CPU latency from a latency table and EdgeTPU latency from a highly correlated simulator \(^2\), to expedite the process. DSP and GPU cost models’ training data was still obtained from real time benchmarks. \(^3\) Architecture search and training: We used ImageNet data \(^9\) to search, train and evaluate. Input resolution is 224×224 and ResNet data preprocessing was used. Cloud TPU v2-32 was used in both search and standalone model training, where per core batch size is 128.

For standalone model training, we used the same hyper-parameters with the TuNAS paper for classification \(^3\), where 0.25 was set as the dropout rate when training models for 360 epochs to get the test accuracy.

For architecture search, we increased the search length as it showed some benefits when optimizing DSP and TPU. Specifically, 1) per core learning rate was halved from 0.0825 to 0.04125; 2) the warmup time where only shared model

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\(^1\) In order to have consistency across multiple hardware, accuracy in this paper is always measured on the float model.

\(^2\) The simulator is highly correlated with real device in the sense that model A runs faster than model B on simulator iff A runs faster than B on real device. Latency number on simulator is usually smaller than that on real device.

\(^3\) Unless specified ‘simulator’ in the text, all latency reported in this paper is real time benchmarks.
weights are trained without updating RL controller was increased from 25% to 50%; 3) we searched for 360 epochs instead of 90 epochs.

6.2 Re-Implement Baseline Models

To make fair comparison, we re-implemented the baseline models in our training setup so that they use the same hyper-parameters with our new multi-hardware models. Table 2 lists the re-implemented accuracy v.s. published accuracy, where Mobilenet models’ published accuracy was from [1] and ProxylessNAS-mobile (PNAS-M)’s published accuracy was from [5]. When scaling down the model (width multiplier = 0.75), we shrunk the filter sizes uniformly, while MobilenetV2 and MobilenetV3 variations keep the last layer unchanged when shrinking the other filters.

Table 2: Top-1 ImageNet accuracy (%) of published number v.s. our re-implemented baseline models in TuNAS. ‘MN’ is short for ‘mobilenet’, ‘MNV3L’ denotes ‘mobilenet v3 large’. ‘-’ means no published accuracy.

| Model     | Width Multiplier | MNV1 | MNV2 | MNV3L | MNV3Lmin | PNAS-M |
|-----------|------------------|------|------|-------|----------|--------|
| Published | 0.75             | 0.75 | 1.0  | 0.75  | 1.0      | 0.75   | 1.0    |
| Ours      |                  | 68.4 | 70.9 | 69.8  | 73.3     | 75.3   | 72.3   | 69.5   |
|           | 1.0              | 73.3 | 73.3 | 73.1  | 75.3     | 69.5   | 72.6   | 74.9   |

While our re-implementation yield similar (slightly better) accuracy as the published numbers for MobiletV3 and ProxylessNAS-Mobile, it has significant gain on MobilenetV1 (2.7%) and MobilenetV2 (1.4%). This is consistent with the results in [3]. The gain on MobilenetV2 with width multiplier 0.75 is less than that with 1.0 multiplier because of the different scaling scheme used in re-implementation mentioned above. Unless specified otherwise, all numbers of baseline models reported in this paper come from these re-implemented models.

6.3 Multi-Hardware Models for Pixel4

We conducted two multi-hardware architecture searches using TuNAS to find models that perform well on all hardware in Pixel4, regarding average performance and worst case performance, respectively. Both of them use the same multi-hardware search space proposed in Section 5.1. Reward functions used in these two searches were equation (7) and (8) respectively. $\beta$ is set to -0.07.

Figure 4 shows the accuracy-latency pareto curves of the obtained multi-hardware models compared with (re-implemented) baseline models. ‘Multi-MAX’ and ‘Multi-AVG’ models are the results from searching over average metric and max metric, respectively. Each model has three points in the plot denoting the performance for width multiplier 0.75, 1 and 1.25.

On CPU float, except MobilenetV3 Large model, which is particularly optimized for this single hardware, our multi-hardware models performs the best among all other baseline models. MobilenetV3 Large is too much optimized for
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Fig. 4: Accuracy-latency trade-offs of multi-hardware model v.s. baseline models on each optimized hardware. The horizontal axis is end-to-end real time latency benchmarks in milliseconds and the vertical axis is test accuracy.

CPU, such that this model is not supported in EdgeTPU. On all other hardware, our multi-hardware models achieve SOTA trade-off between accuracy and latency.

More specifically, on CPU and GPU, multi-hardware models perform similarly with MobilenetV3 Large min, however they are much better than this baseline model on EdgeTPU and DSP. After updating MobilenetV1’s accuracy with the better hyper-parameters, we found that this is the best baseline model on DSP as it contains all merits optimized on this hardware. However, our multi-hardware models still perform better as MobilenetV1 does not perform well enough when scaling up and it has much worse performance on all other hardware. Lastly but not the least, our multi-hardware models give better results than Mobilenet-EdgeTPU which particularly optimized for single-hardware EdgeTPU, on both EdgeTPU and other hardware.

Fig. 1 in Introduction shows the overall performance where the normalization factors were taken as the latency of MobilenetV1 on examined hardware as shown in Table 3. As expected, the multi-hardware models are better than all baseline models in both average and worst case performance. Note that in Table 3, EdgeTPU simulator latency, instead of real time latency, is used as the norm factor in search reward functions because we used simulator to generate the large number of benchmarks for training the EdgeTPU cost model.

Table 3: Latency of reference model MobilenetV1 on examined hardware.

| Pixel4 hardware | CPU float | CPU uint8 | GPU | DSP | EdgeTPU | EdgeTPU simulator |
|-----------------|-----------|-----------|-----|-----|---------|-------------------|
| MobilenetV1     | 36.8ms    | 12.9ms    | 4.82ms | 3.06ms | 2.38ms | 1.06ms |

Numerically, we compare multi-hardware models with baseline models on similar accuracy range in Table 4. Multi-MAX model runs the fastest on all examined hardware except on CPU float where it still ranks the second, while its
accuracy is only 0.4% lower than the second highest number in baseline models achieved by MobilenetV2 and MobilenetV3 Large. The top accuracy is achieved by Mobilenet-EdgeTPU, which is only 0.4% higher than Multi-AVG model but its latency on CPU float is almost \(2\times\) slower and MAdds is \(2.29\times\) more. While MobilenetV3 Large achieves the best CPU float latency, it is not supported on EdgeTPU, and runs 18% slower than Multi-AVG on DSP while also 0.5% lower on accuracy. MobilenetV2 is 0.5% lower on accuracy than Multi-AVG and runs also slower on all examined hardware: 25% slower on CPU float and 30% slower on DSP.

Table 4: Performance of multi-hardware models comparing with baseline models on Pixel4 phone. ‘wm’ is short for ‘width multiplier’. ‘\(\times\)’ means that the model is not supported on that hardware. ‘MN-Norm’ is the mobilenet normalized metrics proposed in Section 5.2 where lower is better. Top-1 item within each column has been marked bold.

| Model    | wm | Accu (%) | Params (M) | MAdds (M) | CPU float | uint8 | GPU | DSP | EdgeTPU | MN-Norm |
|----------|-----|----------|------------|-----------|-----------|-------|-----|-----|---------|---------|
| MNV1     | 1.25| 75.1     | 6.25       | 883       | 54.7      | 18.2  | 7.12| 3.72| 2.84    | 1.36 1.49|
| MNV2     | 1.25| 75.3     | 5.01       | 487       | 38.8      | 16.6  | 5.74| 4.97| 2.93    | 1.28 1.62|
| MNV3L    | 1.0 | 75.3     | 5.45       | 217       | 20.3      | 13.2  | 5.61| 4.51| \(\times\) | \(\times\) |
| MNV3Lmin | 1.25| 74.9     | 5.73       | 346       | 27.7      | 12.6  | 4.56| 3.81| 2.58    | 1.00 1.25|
| PNAS-M   | 1.0 | 74.9     | 4.05       | 321       | 27.6      | 14.8  | 5.92| 3.90| 3.09    | 1.14 1.30|
| MN-TPU   | 1.0 | 76.2     | 4.05       | 991       | 59.3      | 19.4  | 7.52| 4.29| 2.67    | 1.44 1.61|
| Multi-AVG| 1.0 | 75.8     | 4.91       | 433       | 31.0      | 13.9  | 5.40| 3.81| 2.40    | 1.06 1.25|
| Multi-MAX| 1.0 | 74.9     | 4.39       | 349       | 25.2      | 11.7  | 4.47| 3.38| 2.22    | 0.91 1.10|

Fig. 5: Accuracy-latency trade-offs of multi-hardware models v.s. baseline models on un-searched hardware.

4 ProxylessNAS-Mobile only has two data points on MediaTek hardware as the model with width multiplier 1.25 is not fully supported by this hardware.
To show how multi-hardware models generalize on un-searched hardware, we evaluate their performance on various hardware of Pixel3 and MediaTek phones in Fig. 5. Similar to Pixel4 results in Fig. 4, multi-hardware models give best results on Pixel3 GPU and DSP and the second best result on CPU float. Unlike the results on Pixel4 CPU uint8, multi-hardware models are only the second best on Pixel3 CPU uint8. This is because that Pixel3 CPU float and uint8 are close hardware, while Pixel4 CPU uint8 has been particularly accelerated and performs much different from CPU float. Above observation demonstrates that one may only need to pick representative hardware to optimize, as the multi-hardware model will most likely to have similar performance on closely related hardware, such as the same type of chips with different versions.

MediaTek Dimensity 1000 5G is a completely different type of hardware which uses APU accelerator. However, our multi-hardware models still achieve the best results. This implies the good generalization of multi-hardware models when a diverse enough set of hardware are considered in the optimization.

Fig. 6 shows the visualization of the multi-hardware models. The number inside each grey box is the output filter size (number of channels) for that stage, which is applied to each of the colored blocks inside. For example, in Fig. 6(a) second to left grey box, ‘dwbottleneck 3x3 / 96.0’ indicates an inverted bottleneck block where the kernel size of depthwise convolution is 3x3, the filter size of the expanded layer is 96 and the output filter size is 32. ‘skip’ denotes an identity operation. The $\times 2$ strides on resolution are taken at the same places as the centered model MobilenetV3: at the beginning of 1st, 2nd, 3rd, 4th, 6th stages respectively.
Both of the multi-hardware models have light early layers and heavy later layers, 5x5 kernels also appear later in the network. This indicates that multi-hardware models tend to move the computation to later layers where accelerators may gain more computation advantage. In addition, the observation that fused inverted bottlenecks are not chosen for multi-hardware models indicates that, operations only effective on a small subset of examined hardware are not preferable for multi-hardware optimization.

6.4 Multi-Hardware Search v.s. Single-Hardware Search

To show the effectiveness of multi-hardware search comparing with single-hardware search, we conduct single-hardware search, by using reward function in equation [9], for each optimized hardware on the same multi-hardware search space with the multi-hardware search. The results are shown in Table 5. As expected, the best performance on CPU uint8, GPU and DSP was obtained from searching for corresponding hardware. Since the multi-hardware search space does not contain SE and h-swish which are particularly effectively on CPU float, Single-CPU float model searched on this search space only gives sub-optimal performance. Single-DSP model gives similar or even better results on EdgeTPU than Single-EdgeTPU indicates the high correlation between DSP and EdgeTPU. By checking the overall latency metrics, Single-CPU uint8 model (highlighted in yellow) gives the best results in all single-hardware models.

Table 5: Performance of single-hardware models. ‘Single-DSP’ is the searched model only optimized for DSP. Top-1 item within each column is marked bold.

| Model            | Accu (%) | CPU float | uint8 | GPU | DSP | EdgeTPU MN-Norm | Avg  | Max |
|------------------|----------|-----------|-------|-----|-----|-----------------|------|-----|
| Single-CPU float | 76.5     | 39.6      | 18.0  | 6.23| 4.52| 3.32            | 1.33 | 1.48|
| Single-CPU uint8 | 76.2     | 38.6      | 13.9  | 5.85| 3.71| 2.55            | 1.13 | 1.21|
| Single-GPU       | 76.0     | 33.6      | 15.6  | 5.46| 4.10| 2.68            | 1.15 | 1.34|
| Single-DSP       | 76.3     | 46.7      | 15.6  | 6.88| 3.42| 2.44            | 1.21 | 1.43|
| Single-EdgeTPU   | 76.0     | 44.0      | 15.4  | 6.03| 3.98| 2.47            | 1.20 | 1.30|

Table 6: Compare computation cost and performance of multi-hardware search and single-hardware search. One unit of search cost is ~90 hours of Cloud TPU v2-32 usage.

| Model               | Search Cost | Accu (%) | CPU float | uint8 | GPU | DSP | EdgeTPU MN-Norm | Avg  | Max |
|---------------------|-------------|----------|-----------|-------|-----|-----|-----------------|------|-----|
| Single-Hardware     | 5×          | 76.2     | 38.6      | 13.9  | 5.85| 3.71| 2.55            | 1.13 | 1.21|
| Multi-Hardware      | 1×          | 75.8     | 31.0      | 13.9  | 5.40| 3.81| 2.40            | 1.06 | 1.25|

Taking the best single-hardware search results and comparing with the multi-hardware model (we take Multi-AVG here as they have similar accuracy) in Table 6, we can see that the best single-hardware model performs on par, or even slightly better than multi-hardware model on normalized max metric. However,
which hardware would give the best model is unknown until we get all single-hardware models. Therefore, though single-hardware search might get slightly better results than multi-hardware search, its computation cost is $N \times \text{that needed for multi-hardware search}$, which scales linearly with the number of hardware one wants to optimize on.

7 Conclusions

In this paper, we explored the question of finding a single model that works well on multiple hardware, where a general methodology was proposed and demonstrated by a case study on Pixel4 hardware. Specifically, the concept of multi-hardware search space that is compatible with all examined hardware has been introduced, as well as the normalized average and max metrics to compare models’ multi-hardware performance. The multi-hardware models found in our experiments give SOTA performance on majority of the examined hardware, as well as closely correlated un-searched hardware. Comparing with single-hardware searches which have to be applied on each target hardware separately, multi-hardware search gives comparable overall performance in a single search/train session.

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