Efficient Approaches for Designing Fault Tolerant Reversible Carry Look-Ahead and Carry-Skip Adders

Md. Saiful Islam, Muhammad Mahbubur Rahman, Zerina Begum, and Mohd. Zulfiquar Hafiz

Abstract—Combinational or Classical logic circuits dissipate heat for every bit of information that is lost. Information is lost when the input vector cannot be recovered from its corresponding output vector. Reversible logic circuit implements only the functions having one-to-one mapping between its input and output vectors and therefore naturally takes care of heating. Reversible logic design becomes one of the promising research directions in low power dissipating circuit design in the past few years and has found its application in low power CMOS design, digital signal processing and nanotechnology. This paper presents the efficient approaches for designing fault tolerant reversible fast adders that implement carry look-ahead and carry-skip logic. The proposed high speed reversible adders include MIG gates for the realization of its basic building block. The MIG gate is universal and parity preserving. It allows any fault that affects no more than a single signal readily detectable at the circuit’s primary outputs. It has also been demonstrated that the proposed design offers less hardware complexity and is efficient in terms of gate count, garbage outputs and constant inputs than the existing counterparts.

Index Terms—Carry Look-Ahead Adder, Carry-Skip Adder, Fault Tolerance, Parity-Preserving Reversible Gate, Reversible Logic

I. INTRODUCTION

Reversible circuits dissipate heat in the amount of $kT\ln 2$ Joule for every bit of information that is lost irrespective of their implementation technologies, where $k$ is the Boltzmann constant and $T$ is the operating temperature [1]. Information is lost when the circuit implements nonbijective functions. Therefore in irreversible logic circuit the input vector cannot be recovered from its output vectors. Reversible logic circuit by definition realizes only those functions having one-to-one mapping between its input and output assignments. Hence in reversible circuits no information is lost. According to [2] zero energy dissipation would be possible only if the network consists of reversible gates. Thus reversibility will become an essential property in future circuit design.

Reversible logic imposes many design constraints that need to be either ensured or optimized for implementing any particular Boolean functions. Firstly, in reversible logic circuit the number of inputs must be equal to the number of outputs. Secondly, for each input pattern there must be a unique output pattern. Thirdly, each output will be used only once, that is, no fan out is allowed. Finally, the resulting circuit must be acyclic [3]-[5]. Any reversible logic design should minimize the followings [6]:

- **Garbages**: outputs that are not used as primary outputs are termed as garbages
- **Constants**: constants are the input lines that are either set to zero(0) or one (1) in the circuit’s input side
- **Gate Count**: number of gates used to realize the system
- **Hardware Complexity**: refers to the number of basic gates (NOT, AND and EXOR gate) used to synthesize the given function

Parity checking is one of the widely used mechanisms for detecting single level fault in communication and many other systems. It is believed that if the parity of the input data is maintained throughout the computation, no intermediate checking would be required [7], [8]. Therefore, parity preserving reversible circuits will be the future design trends towards the development of fault tolerant reversible systems in nanotechnology. And a gating network will be parity preserving if its individual gate is parity preserving [7]. Thus, we need parity preserving reversible logic gates to construct parity preserving reversible circuits. This paper presents the efficient approaches for designing fault tolerant reversible carry look-ahead and carry-skip adders. To design the basic building block of both carry look-ahead adder (CLA) and carry-skip adder (CSA) we have used IG gate proposed in [9], [10]. The IG gate is parity preserving and complete. Finally, this paper presents a 16-bit high speed fault tolerant reversible adder that is efficient in terms of gate count, garbage outputs, constant inputs and hardware complexity.

The rest of the paper is organized as follows: section II presents reversible logic and some basic reversible logic gates, section III presents parity preserving reversible logic gates, section IV presents the efficient approaches for designing CLA and CSA, section V evaluates proposed designs in terms of gate count, hardware complexity,
garbages and constant inputs; and finally section VI concludes the paper.

II. REVERSIBLE LOGIC GATES

A gate that implements any bijective function involving \( n \) inputs and \( n \) outputs is called an \( n \times n \) reversible logic gate. There exist many reversible gates in the literature. Among them 2*2 Feynman gate [11] (shown in Fig. 1), 3*3 Fredkin gate [12] (shown in Fig. 2), 3*3 Toffoli gate [13] (shown in Fig. 3) and 3*3 Peres gate [14] (shown in Fig. 4) are the most referred. Feynman (FG), Fredkin (FRG) and Peres (PG) gates are one through \( n \) gates, that is, one of its output lines is identical to one of its input lines. On the other hand, Toffoli gate is two through, that is, two of its outputs are identical to two of its inputs. It can be easily verified that all of these gates are reversible. Each gate has an equal number of input and output lines. For each input combination there is a unique output combination.

\[
\begin{array}{c|c|c|c|c|c}
A & B & P & Q & R & C \\
---&---&---&---&---&---
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 1 & 1 & 0 \\
1 & 0 & 1 & 1 & 1 & 1 \\
1 & 1 & 1 & 1 & 1 & 1 \\
\end{array}
\]

Fig. 1. 2*2 Feynman gate.

\[
\begin{array}{c|c|c|c|c|c|c}
A & B & C & P & Q & R & 0 \\
---&---&---&---&---&---&---
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 1 & 0 & 1 & 0 \\
1 & 0 & 1 & 1 & 0 & 1 & 1 \\
1 & 1 & 1 & 1 & 0 & 0 & 1 \\
\end{array}
\]

Fig. 2. 3*3 Fredkin gate

\[
\begin{array}{c|c|c|c|c|c|c}
A & B & C & Q & P & R & 0 \\
---&---&---&---&---&---&---
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 1 & 1 & 0 \\
1 & 0 & 1 & 1 & 0 & 0 & 1 \\
1 & 1 & 1 & 1 & 0 & 0 & 1 \\
\end{array}
\]

Fig. 3. 3*3 Toffoli gate.

\[
\begin{array}{c|c|c|c|c|c|c}
A & B & C & P & Q & R & 0 \\
---&---&---&---&---&---&---
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 0 & 1 & 0 \\
1 & 0 & 1 & 0 & 0 & 0 & 1 \\
1 & 1 & 1 & 0 & 0 & 1 & 0 \\
\end{array}
\]

Fig. 4. 3*3 Peres gate.

III. PARITY PRESERVING REVERSIBLE GATES

A reversible gate will be parity preserving if the parity of the inputs matches the parity of the outputs. Mathematically, a reversible gate having \( n \) input lines and \( n \) output lines will be parity preserving if and only if:

\[ I_1 \oplus I_2 \oplus \ldots \oplus I_n \leftrightarrow O_1 \oplus O_2 \oplus \ldots \oplus O_n \]

where \( I_i \) and \( O_j \) are the input and output lines. Not all of the gates presented in section II are parity preserving. Only Fredkin gate is parity preserving and it can be easily verified by examining its truth table. That is, Fredkin gate maintains \( A \oplus B \oplus C \leftrightarrow P \oplus Q \oplus R \). It can also be said that the Fredkin gate is zero preserving (once preserving as well) and therefore conservative [15]. Other parity preserving reversible logic gates are 3*3 Feynman Double gate [7] (shown in Fig. 5), 3*3 New Fault Tolerant gate [16] (shown in Fig. 6) and newly proposed 4*4 IG gate [9], [10] (shown in Fig. 7). Feynman Double gate can be as used as the fault tolerant copying gate when it’s B and C input lines are set to constants.

\[
\begin{array}{c|c|c|c|c|c|c}
A & B & C & P & Q & R & 0 \\
---&---&---&---&---&---&---
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 1 & 1 & 0 \\
1 & 0 & 1 & 0 & 0 & 1 & 1 \\
1 & 1 & 1 & 0 & 0 & 0 & 1 \\
\end{array}
\]

Fig. 5. 3*3 Feynman Double gate.

\[
\begin{array}{c|c|c|c|c|c|c}
A & B & C & P & Q & R & 0 \\
---&---&---&---&---&---&---
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 0 & 1 & 0 \\
1 & 0 & 1 & 0 & 0 & 0 & 1 \\
1 & 1 & 1 & 0 & 0 & 1 & 0 \\
\end{array}
\]

Fig. 6. 3*3 New Fault Tolerant gate

\[
\begin{array}{c|c|c|c|c|c|c}
A & B & C & P & Q & R & 0 \\
---&---&---&---&---&---&---
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 1 & 1 & 0 \\
1 & 0 & 1 & 0 & 0 & 1 & 1 \\
1 & 1 & 1 & 0 & 0 & 0 & 1 \\
\end{array}
\]

Fig. 7. 4*4 IG gate

\[
\begin{array}{c|c|c|c|c|c|c}
A & B & C & P & Q & R & 0 \\
---&---&---&---&---&---&---
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 0 & 1 & 0 \\
1 & 0 & 1 & 0 & 0 & 0 & 1 \\
1 & 1 & 1 & 0 & 0 & 1 & 0 \\
\end{array}
\]

Fig. 8. 4*4 MIG gate

The first three output lines of IG gate produce the same output as PG gate. The fourth one can be considered as garbage if we wish to replace PG by IG. It is mainly introduced for preserving the parity. The fourth output line of IG gate can also be minimized to reduce the hardware complexity as follows:

\[ BD \oplus B'(A \oplus D) \leftrightarrow AB' \oplus D \]

The modified version of IG is depicted in Fig. 8.

IV. SYNTHESIS OF FAULT TOLERANT REVERSIBLE CLA AND CSA

The basic building block of many complex computational systems is the full adder (FA). Both CLA and CSA include full adders. Realization of the efficient reversible full adder circuit given in [3]-[5] includes two 3*3 Peres gates. The
A. Ripple Carry Adder

The most straightforward realization of a final stage adder for two \(n\)-bit operands is ripple carry adder. The RCA requires \(n\) full adders (FAs). The carry out of the \(i\)th FA is connected to the carry in of the \((i+1)\)th FA. The Fig. 12 shows a reversible logic implementation of an \(n\)-bit final stage fault tolerant ripple carry adder.

B. Carry Look-Ahead Adder

The main idea behind carry look-ahead addition is an attempt to generate all incoming carries in parallel and avoid waiting until the correct carry propagates from the stage (FA) of the adder where it has been generated. The Fig. 13 shows a reversible logic implementation of a 2-bit fault tolerant carry look-ahead adder.

C. Carry-Skip Adder

A carry-skip adder reduces the carry-propagation time by skipping over groups of consecutive adder stages. The carry-skip adder is usually comparable in speed to the carry look-ahead technique, but it requires less chip area and consumes less power. The Fig. 14 shows a reversible logic implementation of a 4-bit fault tolerant carry skip adder.

D. Proposal for a Novel 16-bit Fault Tolerant Reversible Adder

This paper proposes a 16-bit high speed adder that includes four fixed-size blocks, each of size 4, shown in Fig. 15. Each block is a 4-bit ripple carry adder and block carry in is skipped using carry skip logic. Therefore, each block can be operated in parallel and will thereby reduce the overall delay.

V. Evaluation Of The Proposed Designs

The presented adder circuits can be evaluated in terms of hardware complexity, gate count, constant inputs and garbage outputs produced. Evaluation of the proposed circuit can be comprehended easily with the help of the comparative results given in Table I.

A. Hardware Complexity

One of the main factors of a circuit is its hardware complexity. It can be proved that the proposed adder circuits are better than the existing approaches in terms of hardware complexity. Let

\[
\alpha = \text{A two input EXOR gate calculation} \\
\beta = \text{A two input AND gate calculation} \\
\delta = \text{A NOT gate calculation} \\
T = \text{Total logical calculation}
\]

The FTFA and RCA given in [9], [10] have total logical calculation \(T=8\alpha+6\beta+2\delta\) and \(T=32\alpha+24\beta+8\delta\) respectively. The FTFA given in [15] has total logical calculation \(T=16\alpha+16\beta+4\delta\). The presented FTFA and RCA have total logical calculation \(T=6\alpha+4\beta+2\delta\) and \(T=24\alpha+16\beta+8\delta\) respectively. Therefore, we can say that the presented FTFA and RCA is better than the design given in [9], [10] and [15] in terms of hardware complexity. The CSA with fanout given in [15] has total logical calculation \(T=40\alpha+80\beta+20\delta\). The presented CSA without fanout has total logical calculation \(T=8\alpha+6\beta+2\delta\) and \(T=32\alpha+24\beta+8\delta\) respectively.

B. Gate Count

The presented FTFA and RCA, and the design given in [9], [10] require the same number of reversible gates. The FTFA given in [15] requires 4 reversible gates. Hence the presented FTFA is better than the design given in [15] in terms of gate count. The presented CSA requires 14 reversible gates whereas the CSA given in [15] requires 20 reversible gates. Therefore, we can say that the presented CSA is better than the design given in [15] in terms of gate count. The proposed CLA and HSA require 19 and 56 reversible gates respectively.

C. Garbage Outputs

Garbage output refers to the output of the reversible gate that is not used as a primary output or as input to other gates. One of the other major constraints in designing a reversible
logic circuit is to lessen number of garbage outputs [5]. The presented FTFA and RCA, and the design given in [9], [10] and [15] produce same number garbage outputs. The presented CSA produces 19 garbage outputs whereas the design given in [15] produces 16 garbage outputs only. This is because the presented designs do not allow fanout. Fanout is strictly prohibited in reversible logic design. The proposed CLA and HSA produce 28 and 76 garbage outputs respectively.

**D. Constant Inputs**

Number of constant inputs is one of the other main factors in designing a reversible logic circuit. The input that is added to an $n\times k$ function to make it reversible is called constant input [5]. The presented FTFA and RCA, and the design given in [9], [10] and [15] require the same number constant inputs. The presented CSA requires 15 constant inputs whereas the design given in [15] produces 11 constant inputs only. This is because the presented designs do not allow fanout. Fanout is strictly prohibited in reversible logic design. The proposed CLA and HSA require 26 and 60 constant inputs respectively.

**VI. Conclusion**

This paper presents the efficient approaches for designing fault tolerant reversible carry look-ahead and carry-skip adders. The proposed designs are optimized in terms of gate count, garbage outputs, constant inputs and hardware complexity. Finally a novel design of 16-bit high speed fault tolerant reversible adder is proposed. It has also been demonstrated that the proposed designs offer less hardware complexity and are efficient in terms of gate count, garbage outputs and constant inputs.

**References**

[1] R. Landauer, “Irreversibility and heat generation in the computing process”, IBM J. Research and Development, vol. 5, pp. 183-191, 1961.
[2] C. H. Bennet, “Logical reversibility of computation”, IBM J. Research and Development, vol. 17, no. 6, pp. 525-532, 1973.
[3] M. S. Islam, M. R. Islam, M. R. Karim, A. A. Mahmud and H. M. H. Babu, “Variable block carry skip logic using reversible gates”, In Proc. of 10th International Symposium on Integrated Circuits, Devices & Systems, Singapore, pp 9-12, 8-10 September, 2004.
[4] M. S. Islam, M. R. Islam, M. R. Karim, A. A. M. and H. M. H. Babu, “Minimization of adder circuits and variable block carry skip logic using reversible gates”, In Proc. of 7th International Conference on Computer and Information Technology, Dhaka, Bangladesh, 26-28 December, 2004, pp. 378-383.
[5] M. S. Islam and M. R. Islam, " Minimization of reversible adder circuits", Asian Journal of Information Technology, vol. 4, no. 12, pp. 1146-1151, 2005.
[6] M. S. Islam, M. M. Rahman, Z. Begum and M. Z. Hafiz, "Low cost quantum realization of reversible multiplier circuit", Information Technology Journal, vol. 8, no. 2, pp.208-213, 2009.
[7] B. Parhimi, “Fault tolerant reversible circuits”, in Proceedings of 40th Asimolar Conf. Signals, Systems, and Computers, Pacific Grove, CA, pp. 1726-1729, October 2006.
[8] R. K. James, Shahana T. K., K. P. Jacob and S. Sasi, “Fault Tolerant Error Coding and Detection using Reversible Gates”, IEEE TENCON, pp. 1-4, 2007.
[9] M. S. Islam, M. M. Rahman, Z. Begum, M. Z. Hafiz and A. A. Mahmud, “Synthesis of fault tolerant reversible logic circuits”, In Proc. IEEE International Conference on Testing and Diagnosis, Chengdu, China, 28-29 April, 2009.
[10] M. S. Islam and Z. Begum, "Reversible logic synthesis of fault tolerant carry skip BCD adder", Bangladesh Academy of Science Journal, vol. 32, no.2, pp. 193-200, 2008.
[11] F. Feynman, “Quantum mechanical computers”, Optical News, vol. 11, 1985, pp. 11-20.
[12] E. Fredkin and T. Toffoli, “Conservative logic”, Intl. Journal of Theoretical Physics, pp. 219-233, 1982.
[13] T. Toffoli, “Reversible computing”, In Automata, Languages and Programming, Springer-Verlag, pp. 632-644, 1980.
[14] A. Peres, “Reversible logic and quantum computers”, Physical Review: A, vol. 32, no. 6, pp. 3266-3276, 1985.
[15] J. W. Bruce, M. A. Thornton, L. Shivakumarahia, P.S. Kokate, X. Li, “Efficient adder circuits based on a conservative reversible logic gates”, In Proceedings of IEEE Computer Society Annual Symposium on VLSI, Pittsburg, PA, pp. 83-88, 2002.
[16] M. Haighparast and K. Navi, “A novel fault tolerant reversible gate for nanotechnology based systems”, Am. J. of App. Sci., vol. 5, no.5, pp. 519-523, 2008.
**TABLE I** COMPARATIVE EXPERIMENTAL RESULT OF DIFFERENT FAULT TOLERANT REVERSIBLE ADDER CIRCUITS

| Design       | Gate Count | Hardware Complexity | Constant Inputs | Garbage Outputs |
|--------------|------------|---------------------|-----------------|-----------------|
| 1-bit FTFA   | 2 MIG      | 6α+4β+2δ             | 2               | 3               |
| 1-bit FTFA [9][10] | 2 IG       | 8α+6β+2δ             | 2               | 3               |
| 1-bit FTFA [15] | 4 FRG      | 8α+16β+4δ            | 8               | 12              |
| 4-bit RCA    | 8 MIG      | 24α+16β+8δ           | 8               | 12              |
| 4-bit RCA [9][10] | 8 IG       | 32α+24β+8δ           | 8               | 12              |
| 4-bit RCA [15] | 16 FRG     | 32α+64β+16δ          | 8               | 12              |
| 2-bit CLA    | 4 MIG+10 F2G+5 NFT = 19 | 47α+23β+9δ          | 26              | 28              |
| 4-bit CSA    | 8 MIG + 4NFT +2 F2G=14 | 40α+28β+12δ         | 15              | 19              |
| 4-bit CSA [15] | 20 FRG     | 40α+80β+20δ          | 11              | 16              |
| 16-bit HSA   | 32 MIG+16NFT+8F2G = 56 | 320α+112β+48δ       | 60              | 76              |

Fig. 12. Reversible logic implementation of fault tolerant n-bit ripple carry adder.

Fig. 13. Reversible logic implementation of 2-bit fault tolerant carry look-ahead adder. The realization requires 19 parity preserving reversible gates of which are 5 NFTs, 10 F2Gs and 8 MIGs. It needs 26 constant inputs and produces 28 garbage outputs.

Fig. 13 presents a reversible logic implementation of a 2-bit fault tolerant carry look-ahead adder. The realization requires 19 parity preserving reversible gates of which are 5 NFTs, 10 F2Gs and 8 MIGs. It needs 26 constant inputs and produces 28 garbage outputs.
Fig. 14 presents an efficient reversible logic implementation of a 4-bit fault tolerant carry skip adder. The realization requires 14 parity preserving reversible gates of which are 4 NFTs, 2 F2Gs and 8 MIGs. It needs 15 constant inputs and produces 19 garbage outputs. The proposed CSA is better than the CSA presented in [15] in terms of gate count and hardware complexity. The proposed design requires more garbages than the design given in [15]. This is because fanout are not allowed in the proposed design since it is strictly prohibited in reversible logic design. The 16-bit high speed fault tolerant reversible adder is realized by dividing it into four fixed-sized blocks. Each block implements carry skip logic to skip block carry in for the next block. To realize the block 4-bit RCA is proposed instead of 4-bit CLA because CLA is more costly than CSA in terms of gate count. The fault tolerant CSA offers less hardware complexity than CLA too.