I/O Lower Bounds for Auto-tuning of Convolutions in CNNs

Technical Report

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Abstract
Convolution is the most time-consuming part in the computation of convolutional neural networks (CNNs), which have achieved great successes in numerous practical applications. Due to the complex data dependency and the increase in the amount of model samples, the convolution suffers from high overhead on data movement (i.e., memory access). This work provides comprehensive analysis and methodologies to minimize the communication for the convolution in CNNs. With an in-depth analysis of the recent I/O complexity theory under the red-blue game model, we develop a general I/O lower bound theory for a composite algorithm which consists of several different sub-computations. Based on the proposed theory, we establish the data movement lower bound results for two main convolution algorithms in CNNs, namely the direct convolution and Winograd algorithm, which represents the direct and indirect implementations of a convolution respectively. Next, derived from I/O lower bound results, we design the near I/O-optimal dataflow strategies for the two main convolution algorithms by fully exploiting the data reuse. Furthermore, in order to push the envelope of performance of the near I/O-optimal dataflow strategies further, an aggressive design of auto-tuning based on I/O lower bounds, is proposed to search an optimal parameter configuration for the direct convolution and Winograd algorithm on GPU, such as the number of threads and the size of shared memory used in each thread block. Finally, experiment evaluation results on the direct convolution and Winograd algorithm show that our dataflow strategies with the auto-tuning approach can achieve about 3.32× performance speedup on average over cuDNN. In addition, compared with TVM, which represents the state-of-the-art technique for auto-tuning, not only our auto-tuning method based on I/O lower bounds can find the optimal parameter configuration faster, but also our solution has higher performance than the optimal solution provided by TVM.

Keywords: I/O lower bounds, red-blue pebble game, dataflow design, auto-tuning, convolutional neural network.

1 Introduction
Convolutional neural networks (CNNs) are commonly applied to numerous computer vision and machine learning applications, which have achieved great successes because the complex layer structures could produce high-quality results based on a large number of data. Specifically, the convolution layer is an important structure in many state-of-the-art modern CNN models, such as MobileNet [14], ResNet [29], ShuffleNet [34], SqueezeNet [15], VggNet [27] and so on. The wide adoption of convolution and its huge cost have led to a high demand to optimize convolution operations for high performance. From the hardware perspective, GPUs have been demonstrated to be able to provide tremendous computation power for accelerating convolution operations [31]. Furthermore, many specific accelerators for convolutions in CNNs are designed based on field-programmable gate arrays (FPGA) and application-specific integrated circuits (ASIC).

For convolution operations in CNNs, multiple convolution algorithms have been developed and classified into two categories: direct and indirect approaches. Typical direct and indirect representatives are the direct convolution and Winograd convolution algorithms respectively, each of which involves a large amount of memory accesses due to the complex computational workflow and massive data in convolution operations. For example, all inputs and weights are typically stored in the off-chip memory of CNN accelerators, such as NVIDIA cuDNN [9] and AMD MIOpen [20]. During computation, partial inputs and weights are loaded from the off-chip memory into the on-chip buffer to produce portions of outputs. Meanwhile, each processor could use its own registers to read some inputs and weights which have been in the on-chip buffer. Consequently, the frequent data movement in the memory hierarchy commonly dominates the energy consumption in convolution operations [6]. Therefore, optimizing the data

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transmission in convolutions is the key for improving the performance of convolutions.

To minimize data movement, the most works focus on how to reduce the model size, such as quantifying weights [36]. On the other hand, another effective way for reducing communication is to increase data reuse based on the dataflow design. In recent years, a variety of dataflow approaches have been proposed [7, 18, 25], most of which mainly focus on the computation efficiency. However, the data movement of convolutions has not been taken a full account. This work would try to consider the communication-optimal strategies for different convolution algorithms based on the I/O lower bound analysis.

Since I/O lower bound analysis is important for evaluating the optimality of a proposed algorithmic solution, it is widely concerned to establish appropriate lower bounds of the data movement of application codes [19, 30]. Under the red-blue pebble game model [17] for data transmission in memory hierarchy, past work on I/O lower bounds has found bounds for specific algorithms, such as matrix-matrix multiplication and FFT. As the recent methodology mainly focuses on the workflow’s specific properties which do not translate across different computational patterns, the recent lower bound theory seems hard to be applied to arbitrary computations such as convolutions, in which different sub-computations involve different computational patterns. How to establish a systematic I/O lower bound theory for convolutions based on the red-blue pebble game model is a big challenge[32]. Even if the lower bounds could be obtained, the theoretical minimum of I/O complexity is not easy to directly yield an efficient dataflow strategy. There is a very large space to explore. How to determine the dataflow with the help of I/O lower bound is another challenge.

To solve the above challenges, this work considers to quantify the contribution of each sub-computation to the total computation, and then generalizes the recent I/O lower bound theory to establish I/O lower bound results for convolutions under the red-blue pebble game model. Next, through a deeper investigation of the highest order term in the lower bound results, we determine which data reuse should be fully exploited, and propose I/O-optimal dataflow strategy for maximizing such data reuse to minimize the memory access in convolutions. Furthermore, by comparing the lower bound result with I/O cost of our dataflow strategy, the optimality condition for implementation of convolutions is deduced. Based on the optimality condition, a fine-grained auto-tuning optimization is designed to effective find the optimal implementation with high performance.

In this work, we make the following key contributions.

- Develop a general I/O lower bound theory for an arbitrary composite algorithm which involves different sub-computations and different computational patterns, under the red-blue pebble game model.
- Establish I/O lower bound results for two typical representatives of direct and indirect convolution algorithms, which are the direct convolution and Winograd convolution algorithms.
- Design near I/O-optimal dataflow strategies respectively for the direct convolution and Winograd convolution algorithms.
- Propose an auto-tuning engine to achieve excellent implementations of our dataflow strategies.

## 2 Background

### 2.1 Red-blue Pebble Game

The red-blue pebble game is a two-level memory access model which is proposed by Hong & Kung. This model is suitable for small-fast and large-slow memory structures and our theoretical analysis of lower bound is based on it. Red and blue pebbles represent fast storage and slow storage, respectively. The fast storage is limited, thus the number of red pebbles is small. The slow storage is unlimited, and there is no limit to the number of blue pebbles. The game is played on a directed acyclic graph (DAG), and DAG describes the operation of the algorithm. Furthermore, the rules of a red-blue pebble game are as follows:

- (Load) A red pebble may be placed on any vertex that has a blue pebble.
- (Store) A blue pebble may be placed on any vertex that has a red pebble.
- (Compute) If all the immediate predecessors of a vertex have red pebbles, a red pebble may be placed on such vertex.
- (Free) A pebble no matter red or blue may be removed from any vertex.

Let $G(V, E)$ be a DAG, which describes an algorithm. $V$ is the vertex set representing operations of algorithm, and $E$ is the edge set representing the dependency of two operations. A partition on $G$ is called an $S$-partition, if the following four properties hold.

- Property 1: $V$ is partitioned into $h$ subsets $V_1, V_2, \ldots, V_h$ such that $V_i$’s are disjoint but their union is $V$.
- Property 2: There is a dominator set $D_i$ for each $V_i$ that contains at most $S$ vertices. A dominator set $D_i$ for $V_i$ is a set of nodes in $V$ such that any path from an input of $G$ to a node in $V_i$ contains some nodes in $D_i$.
- Property 3: There is a minimum set $M_i$ for each $V_i$ that contains at most $S$ vertices. The minimum set of $V_i$ is defined to be the set of vertices in $V_i$ that do not have any successor vertex belonging to $V_i$.
- Property 4: No cyclic dependence is among $V_1, \ldots, V_h$.

Let $P(S)$ be the minimum number of subsets that any $S$-partition of a DAG must have. The following theorem describes the communication lower bound based on the $S$-partition model (for the proof, refer to [17]).
**Theorem 2.1.** Any complete calculation of a red-blue pebble game on DAG $G = (V, E)$ with at most $S$ red pebbles needs the minimum I/O time $Q$ such that

$$Q \geq S \cdot (P(2S) - 1).$$

(1)

2.2 Direct Convolution

![Figure 1. Direct Convolution.](image)

Figure 1 illustrates a direct convolution. We have an input image of size $W_in \times H_in \times C_in$ and $C_out$ kernels of weights, producing a $W_out \times H_out \times C_out$ output image. For the convolution, the channels of input image $C_{in}$ is the number of channels in each kernel, and the channels of output image $C_{out}$ is equal to the number of kernels, and each channel of output image is a $H_{out} \times W_{out}$ matrix. The kernel is a $W_{ker} \times H_{ker} \times C_{in}$ tensor. Each output is computed by an inner product between a kernel tensor and a sliding input tensor with the size of $W_{ker} \times H_{ker} \times C_{in}$ from an input image by using a sliding window. The stride size $\mu$ is the position difference between two adjacent sliding windows.

2.3 Winograd Algorithm

Winograd algorithm for convolution is shown in Figure 2. This algorithm changes the characteristics of time-domain convolution calculations, and reduces the number of multiplication operations between input images and kernels through mathematical transformation. In order to perform the mathematical transformation, several parameter matrices are introduced. Matrix $A$, $B$ and $L$ are three transformation matrices for output images, input images and kernels respectively. Furthermore, as Winograd algorithm requires $W_{ker} = H_{ker}$, we denote $r$ as $W_{ker}$ or $H_{ker}$ briefly. Winograd algorithm can calculate multiple output results at once. Here, we denote $F(e \times e, r \times r)$ as a calculation process to deduce $\epsilon^2$ outputs in winograd algorithm. Theoretically, the value of $\epsilon$ is arbitrary, but in practice $\epsilon$ usually is chosen as 2, 3 or 4. To compute every $\epsilon^2$ outputs at a fixed channel of an output image, $F(e \times e, r \times r)$ requires a sliding input tensor with the size of $(e + r - 1) \times (e + r - 1) \times C_{in}$ from input images using a sliding window and a kernel tensor with the size of $e \times e \times C_{in}$. Then the input tensor and kernel are transformed by $B$ and $L$ into $P$ and $J$ which have the same size of $(e + r - 1) \times (e + r - 1) \times C_{in}$. Next, the corresponding element product of $P$ and $J$ results in a new $(e+r-1)\times(\epsilon+r-1)\times C_{in}$ tensor $\Lambda$, and the summation of elements in $\Lambda$ along channel direction generates a $(e+r-1)\times(e+r-1)$ matrix $\Pi$. Finally, $\Pi$ is transformed by $A$ into a $e \times e$ matrix which are $e^2$ outputs.

![Figure 2. Winograd Algorithm.](image)

Figure 2. Winograd Algorithm.

3 Motivation

In this section, we elaborate specific challenges that need to be addressed in order to build I/O lower bound theory and design I/O optimal dataflow implementations, and present our basic idea to address these challenges.

3.1 Challenges for I/O Lower Bounds Building

![Figure 3. Different Patterns for Winograd Algorithm.](image)

Figure 3. Different Patterns for Winograd Algorithm.

Since the lower bound analysis is important for evaluating the optimality of a proposed algorithmic solution, and often yields new insights in algorithm optimization for achieving better performance, it is widely concerned to establish appropriate I/O lower bounds of the data movement of a numerical method on a hierarchical memory system. In real application, most numerical algorithms, such as convolutions, are typically constructed from a number of sub-computations. For instance, Winograd algorithm has 4 sub-computations, which involve 4 different patterns (Figure 3): (1) transformed matrix multiplication, (2) element-wise multiplication, (3) element-wise addition, (4) transformed matrix multiplication. Although the red-blue pebble game model has been proposed for many years, it is still difficult to use this model to establish I/O lower bounds of composite algorithms which involve several different kinds of computational patterns [13]. It is
not even possible to deduce a suitable I/O lower bound of the DAG only focusing on each sub-computation of the composite codes, due to the following two main reasons. Firstly, at the beginning of the red-blue pebble game, all DAG vertices without predecessors have blue pebbles, and all vertices without successors would get blue pebbles at the end of the game. Based on this assumption, the calculation for each sub-DAG will require at least one load operation for each input and one store operation for each output. However, when the red-blue pebble game is played on the full DAG, the data could pass from a previous sub-computation to a later one directly through fast memory. Secondly, when a composite computation is assigned into several sub-computations, the total DAG is partitioned into several relevant sub-graphs. Under a common constraint that previous sub-computation must be totally finished before the later sub-computation starts, the partition way of the total DAG usually impacts the data movement complexity due to the limited size of fast memory. The two reasons above describe the essential difficulties to develop the general I/O lower bound theory for any composite algorithm. To get around these difficulties, the red-blue-white pebble game model has been proposed recently to analyze composite algorithms, which uses some restrictions on models [13].

3.2 Challenges for Optimal Implementations

If I/O lower bound can be obtained, it often provides some insights for the algorithm design. For instance, I/O lower bound can tell us which data should be reused in the on-chip memory prior to the others (see Section 5). When we know which data has higher reuse priority, another challenge is designing the optimal implementation to maximize such data reuse. For the implementation design of convolutions, the combinatorial choices of memory access, threading pattern, specific input shape and layout create a huge configuration space, such as loop tiling, ordering, unrolling, and so on. For 4 sub-computations in Winograd algorithm, the size configuration space is usually larger than $10^6$. This fact indicates that it is hard to manually design an efficient implementation for a convolution. Although NVIDIA proposes excellent implementations for different convolution algorithms in cuDNN library [10], these implementations mainly focus on general optimization on GPUs. Directly using the convolution API in cuDNN sometimes can not satisfy the real-time demand of inference applications. Recently, auto-tuning methods have been proposed for the fine-grained optimization of convolutions. The common way is to adopt a predefined cost model to guide the search, but building an accurate cost model is difficult due to the increasing complexity of modern hardware. As the state-of-the-art framework for auto-tuning convolutions, TVM proposes a new auto-tuning method based on ML-model [5]. However, it still needs a large search cost due to the huge search space.

3.3 Basic Idea

In this work, we explore the red-blue pebble game. The analysis on each sub-computation could not accurately estimate the data movement complexity, which is because the contribution of each sub-computation to total computation is ignored. Through the quantification of such contribution, all sub-computations can be viewed as a whole, which provides an opportunity to build I/O lower bound of composite algorithms.

Besides, to addresses the challenges for algorithm optimization, this work combines both the coarse-grained design and fine-grained optimization for convolutions. Based on the lower bound analysis, we propose a coarse-grained dataflow design by fully exploiting the data reuse and minimizing the off-chip memory access. With comparing the I/O volume of the dataflow with the lower bound, we discover the optimality condition for I/O optimal design. Using this optimality condition, our fine-grained optimization is to reduce the size of search space and proposing an effective parallel searching method to find the optimal implementation, which leads to an auto-tuning engine.

4 Lower Bound Theory

4.1 Red-Blue Pebble Game Re-exploration

4.1.1 Basic Idea. In order to build I/O lower bounds of convolutions, we revisit the red-blue pebble game in fine-grained. First of all, it is not easy for a composite code to deduce the value of $P(S)$ indeed, while we could try to estimate a valid lower bound of $P(S)$. Denote $P_S$ as the set containing all possible options of S-partitions for DAG $G(V, E)$, and each element in $P_S$ represents one S-partition of $G(V, E)$. Let

\[
H(S) = \min_{\{V_1, \ldots, V_n\} \in P_S} \max_{1 \leq i \leq k} |V_i|.
\]

According the definition of $P(S)$ in Section 2.1, we have $P(S) \geq H(S)$. This fact, together with Equations (1) and (2), implies that the I/O time $Q$ satisfies

\[
Q \geq S \cdot (P(2S) - 1) \geq S \cdot (H(2S) - 1).
\]

Hence, we only need to estimate $H(2S)$ instead of $P(2S)$. Secondly, from Equation (2), $H(S)$ depends on the value of $\max_{1 \leq i \leq k} |V_i|$, which means that the fine-grained analysis on $V_i$ is the key. Thirdly, if we can find out the relationship between $V_i$ and all sub-computations of $G(V, E)$, it would become possible to estimate the number of vertices in $V_i$. Before deducing the upper bound of $|V_i|$, we formalize the notation of multi-step partition of a DAG.

Definition 4.1. Assume that a DAG $G(V, E)$ is decomposed into $n$ sub-DAGs $G_1(U_1, E_1), G_2(U_2, E_2), \ldots, G_n(U_n, E_n)$ where $G_i(U_i, E_i)$ is corresponding to a sub-computation. \{G_1(U_1, E_1), G_2(U_2, E_2), \ldots, G_n(U_n, E_n)\} is called as a multi-step partition of $G(V, E)$,
if and only if any input vertex of $G_j(U_j, E_j)$ must be an output vertex of $G_{j-1}(U_{j-1}, E_{j-1})$, and the internal vertex sets of all $U_j$’s are disjoint from each other.

It is clear that any sequence of sub-computations can be represented as a multi-step partition of the DAG for the total computation. Assume that $\{G_1(U_1, E_1), \cdots, G_n(U_n, E_n)\}$ is a multi-step partition of $G(V, E)$. If we are able to estimate all the upper bounds of $|V_i \cap U_j|$ ($j = 1, 2, \cdots, n$) by using Property 2 and Property 3 in the definition of S-partition, it is possible to obtain the maximum of $|V_i|$.

In the following, we study the feasibility on the derivation of the upper bound of $|V_i|$ based on recursive analysis. For some $j$-th sub-computation, assume that the upper bound of $|V_i \cap U_j|$ has been obtained successfully. The next problem is how to estimate $|V_i \cap U_{j+1}|$. Since $|V_i \cap U_j|$ seems not to be associated with the upper bound of $|V_i \cap U_{j+1}|$, we have to focus on how the output set of $U_j$ affects the $(j+1)$-th sub-computation. Denote $\bar{O}_j$ as the output set of $U_j$, and $D_i$ as a dominator set of $V_i$. Further, we apply a new concept of vertex generation to determine the vertices in $\bar{O}_j$ which are associated with $D_i$ and $V_i$.

**Definition 4.2.** In a DAG $G(V, E)$, a vertex set $U$ can generate another vertex set $U'$, if and only if every path from an input of $V$ to a vertex in $U'$ contains some vertex in $U$. Furthermore, $\Theta(U)$ represents a set containing all vertices which can be generated by $U$.

It is obvious that the dominator set $D_i$ can generate $V_i$. Furthermore, $\Theta(D_i) \cap V_i \cap \bar{O}_j$ determines the vertices in $\bar{O}_j$ which are associated with $D_i$ and $V_i$. $|\Theta(D_i) \cap V_i \cap \bar{O}_j|$ could be used to deduce the upper bound of $|V_i \cap U_{j+1}|$, because that all inputs of $V_i \cap U_{j+1}$ are included in $\Theta(D_i) \cap V_i \cap \bar{O}_j$.

In conclusion, if we can deduce the upper bounds of $|V_i \cap U_j|$ and $|\Theta(D_i) \cap V_i \cap \bar{O}_j|$, it is easy to obtain $|V_i \cap U_{j+1}|$ and $|\Theta(D_i) \cap V_i \cap \bar{O}_{j+1}|$ by using $|\Theta(D_i) \cap V_i \cap \bar{O}_{j+1}|$ as the inputs for $V_i \cap U_{j+1}$. Based on recursive analysis, all upper bounds of $|V_i \cap U_{j+1}| (j = 1, 2, \cdots, n)$ can be established, which would lead to the upper bound of $|V_i|$.

After the feasibility analysis above on the derivation of the upper bound of $|V_i|$, we use a simple example to show the intuition of how to obtain the the upper bound of $|V_i|$. Assume DAG $G(U, E)$ of a composite algorithm has two sub-computations $(G(U, E) = G_1(U_1, E_1) + G_2(U_2, E_2))$. Denote $k^2$ as the number of vertices in the dominator $D_i$ of $V_i$. According to the definition of S-partition, we have $|D_i| = k^2 \leq S$, and divide $k^2$ into $k^1 + k^1$ such that $k^1$ is the number of input vertices for $V_i \cap U_i$ and $k^2$ is the number of a part of input vertices for $V_i \cap U_2$. For any integer $k$, find two functions $\varphi_j(k)$ and $\psi_j(k)$, where $\varphi_j(k)$ represents the maximum of vertices in $U_j$ generated by using $k$ input vertices, and $\psi_j(k)$ represents the maximum of vertices in $\bar{O}_j$ generated by using $k$ input vertices. Hence, $|\Theta(D_i) \cap V_i \cap U_i|$ is not larger than $\varphi_j(k^1)$, and at most $\psi_j(k^2)$ vertices are generated as the inputs for $V_i \cap U_2$. Hence, there are at most $k^2_j + \psi_j(k^2)$ input vertices for $V_i \cap U_2$. Further, $|\Theta(D_i) \cap V_i \cap U_2| \leq \varphi_2(k^2_j + \psi_j(k^2))$ is valid. Hence, we have

$$|V_i| \leq |D_i|| + |\Theta(D_i) \cap V_i \cap U_1| + |\Theta(D_i) \cap V_i \cap U_2| \leq S + \varphi_2(k^2_j + \psi(k^2_j)) \leq S + \max_{k_1 + k_2 \leq S} (\varphi_1(k_1) + \varphi_2(k_2 + \psi(k_1))).$$

Letting $T(S) = S + \max_{k_1 + k_2 \leq S} (\varphi_1(k_1) + \varphi_2(k_2 + \psi(k_1)))$, we achieve $|V_i| \leq T(S)$.

According to the discussion above, we deduce the general I/O lower bound result of any composite code by three steps. Firstly, find two functions which can determine the numbers of vertices generated by $D_i$ in $V_i \cap U_j$ and $V_i \cap \bar{O}_j$ respectively (Section 4.1.2). Secondly, deduce the upper bound of $|V_i|$ by using the upper bounds of the two functions (Section 4.1.3). Finally, establish general I/O lower bound result by substituting the upper bound of $|V_i|$ into Equations (2) and (3) (Section 4.1.4).

### 4.1.2 Two Maximum Vertex Generation Functions.

For any integer $k$ and a vertex set $U$ with any dominator set $D$ satisfying $|D \cap U_j| + |\Theta(D) \cap \bar{O}_{j-1}| \leq k$, define two vertex generation functions for the $j$-th sub-computation, as follows

$$\varphi_j(U, k) = |\Theta(D) \cap U \cap U_j| \text{ and } \psi_j(U, k) = |\Theta(D) \cap U \cap \bar{O}_j|.$$

Here, $\varphi_j$ and $\psi_j$ represent the numbers of vertices generated by $D$ in two sub-graphs $U \cap U_j$ and $U \cap \bar{O}_j$ respectively. Furthermore, for any given $k$ and the $j$-th sub-computation, we define maximum vertex generation functions as

$$\varphi_j(k) = \max_{U \cap U_j \cap \bar{O}_j} \varphi_j(U, k) \text{ and } \psi_j(k) = \max_{U \cap U_j \cap \bar{O}_j} \psi_j(U, k).$$

It is clear that $\varphi_j$ and $\psi_j$ provide the upper bound estimation on the number of vertices in $U_j$ and $\bar{O}_j$, which can be generated by a vertex $D$ satisfying $|D \cap U_j| + |\Theta(D) \cap \bar{O}_{j-1}| \leq k$.

With maximum vertex generation functions $\varphi_j$ and $\psi_j$, it becomes possible to estimate $|V_i \cap U_j| (j = 1, \cdots, n)$ one by one.

### 4.1.3 Estimation of Upper Bound of $|V_i|$.

The analysis in Section 4.1.1 inspires us that I/O lower bound establishment is equivalent to finding the upper bound of $|V_i|$. Further, two kinds of maximum vertex generation functions $\varphi_j$ and $\psi_j$ in Section 4.1.2, provide us a powerful tool to respectively estimate the numbers of vertices in $V_i \cap U_j$ and $V_i \cap \bar{O}_j$, which are generated by any dominator $D_i$ of $V_i$. In the following, we try to deduce the upper bound of $|V_i|$.

First of all, we deduce two auxiliary results. Let $\bar{O}_j$ be the subset of $\bar{O}_j$ such that for any $v \in \bar{O}_j$, any path from the input set of $V$ to $v$ has at least one vertex which belongs in $U'_{k=1}(D_i \cap U_k)$.

**Lemma 4.3.** $\bar{O}_j \cup (D_i \cap U_{j+1})$ is a dominator set of $\bar{O}_{j+1}$.
Proof. For each \( v \in \overline{O}_j \), denote \( P \) as any path from the input set of \( V \) to the vertex \( v \). In order to prove Lemma 4.3, we need to prove that the path \( P \) has a vertex which belongs in \( \overline{O}_j \cup (D_i \cup U_{j+1}) \).

On one hand, if all vertices in \( P \) belong in \( U_{j+1} \), by the definition of \( D_{j+1} \), there must exist a vertex \( u \in D_i \cup U_{j+1} \) on path \( P \) such that \( u \in \overline{O}_j \). On the other hand, if there is a vertex \( v \notin U_{j+1} \) on the path \( P \), \( P \) belongs in \( U_k \) \( (1 \leq k \leq j) \). Hence, the path \( P \) would be joint with \( \overline{O}_j \) which is the output set of \( U_j \). Let \( w \) be one vertex in \( P \cap \overline{O}_j \). If the sub-path of \( P \) from \( w \) to \( v \) has a vertex \( u \in D_i \), then we have \( u \in D_i \cup U_{j+1} \), similar to the discussion above. Otherwise, if the sub-path of \( P \) from \( w \) to \( v \) has no vertex in \( D_i \), then it is clear that \( w \) must belong in \( \overline{O}_j \). In fact, when the sub-path of \( P \) from \( w \) to \( v \) has no vertex in \( D_i \), any path from the input set of \( V \) to \( w \) must has a vertex in \( D_i \). Furthermore, since \( w \in \overline{O}_j \), any path from the input set of \( V \) to \( w \) must has non vertex in \( D_i \cup U_k \) \( (k \geq j + 1) \). Therefore, on each path from the input set of \( V \) to \( w \), any vertex in \( D_i \) must belong in \( U_{j+1} \cap (D_i \cup U_k) \). Hence, we have \( w \in \overline{O}_j \). In conclusion, Lemma 4.3 is valid. \( \Box \)

With a similar discussion in the proof above, we can find out a dominator set of \( V_i \cup U_{j+1} \).

**Lemma 4.4.** \( \overline{O}_j \cup (D_i \cup U_{j+1}) \) is also a dominator of \( V_i \cup U_{j+1} \).

By Lemma 4.3 and Lemma 4.4, we can obtain an upper bound of \( |V_i| \), which is important for I/O complexity analysis under the red-blue pebble game model.

**Theorem 4.5.** Assume that \( \{G_1(U_1, E_1), \ldots, G_n(U_n, E_n)\} \) is a multi-step partition of a DAG \( G(V, E) \). For any \( S \)-partition \( \{V_1, \ldots, V_h\} \) of \( G(V, E) \), \( |V_i| \) has an upper bound

\[
T(S) = S + \max_{\sum_{j=1}^{h} k_j \leq S} \left( \phi_1(k_1) + \phi_2(k_2) + \phi_3(k_3) + \cdots + \phi_h(k_h) \right)
\]

(5)

where \( |\overline{O}_j| \leq \phi_j(k_{j-1} + \phi_{j-1}(k_{j-2} + \cdots + \phi_1(k_1))) \), \( (6) \)

is valid for any integer \( j \in [1, n] \) by using the mathematical induction. When \( j = 1 \), it is obvious that \( D_i \cup U_1 \) is a dominator set of \( \overline{O}_i \). Since \( |D_i \cup U_1| = k_1 \), we have \( |\overline{O}_i| \leq \phi_1(k_1) \).

This implies that the inequality (6) is valid for \( j = 1 \). Assume that the inequality (6) is valid for \( j \geq 1 \). We need to prove that the result is also valid for \( j + 1 \). In fact, by Lemma 4.3, \( \overline{O}_j \cup (D_i \cup U_{j+1}) \) is a dominator set of \( \overline{O}_{j+1} \). Furthermore, using the assumption above, we have

\[
|\overline{O}_{j+1}| \leq |D_i \cup U_{j+1}| + |\overline{O}_j| \leq k_{j+1} + \phi_2(k_2 + \phi_{j-1}(k_{j-2} + \cdots + \phi_1(k_1)))\,
\]

(7)

Furthermore, the definition of \( \phi_j \) leads to

\[
|\overline{O}_{j+1}| \leq \phi_{j+1}(k_{j+1} + \phi_j(k_2 + \phi_{j-1}(k_{j-2} + \cdots + \phi_1(k_1))))\,
\]

(8)

Thus, the inequality (6) is valid for \( j + 1 \).

Next, by the inequality (6), we can further check that the inequality (7) is always valid. According to Lemma 4.4, \( \overline{O}_j \cup (D_i \cup U_{j+1}) \) is also a dominator set of \( \Theta(D_i) \cap V_i \cup U_{j+1} \). Hence, we have

\[
|\Theta(D_i) \cap V_i \cup U_i| \leq \phi_1(|D_i \cup U_i|) \leq \phi_1(k_1)\,
\]

(9)

and

\[
|\Theta(D_i) \cap V_i \cup U_{j+1}| \leq \phi_j+1(|\overline{O}_j \cup (D_i \cup U_{j+1}))| \leq \phi_{j+1}(k_{j+1} + \phi_j(k_2 + \phi_{j-1}(k_{j-2} + \cdots + \phi_1(k_1))))\.
\]

(10)

Finally, since \( V = U_{j+1}, V_i = U_{j+1}(V_i \cup U_i) \) is valid. As each vertex of \( D_i \) can possibly be a vertex in \( V_i \), we have

\[
|V_i| \leq S + |\Theta(D_i) \cap V_i \cup U_i| + |\Theta(D_i) \cap V_i \cap U_i| + \cdots + |\Theta(D_i) \cap V_i \cup U_{n-1}|\,
\]

which together with (9) and (10), implies that \( |V_i| \leq P(T(S)) \) is valid. \( \Box \)

### 4.1.4 I/O Lower Bound Result For Composite Codes.

**Theorem 4.6.** Assume that a DAG \( G(V, E) \) describes an algorithm with \( n \) steps. All sub-computations in \( n \) steps are corresponding to a multi-step partition of the DAG. Given a fast memory of size \( S \), to finish the algorithm, the minimum number \( Q \) of I/O operations between the fast memory and the slow memory satisfies

\[
Q \geq S \cdot \left( \frac{|V|}{T(2S)} - 1 \right).
\]

(11)

**Proof.** Based on Equations (2) and (3), we have

\[
Q \geq S \cdot \left( \frac{\min_{V_1, \ldots, V_h \in \mathcal{P}_S} |V|}{\max_{1 \leq i \leq h} |V_i|} - 1 \right).
\]

(12)

For any \( \{V_1, \ldots, V_h\} \in \mathcal{P}_S \), Theorem 4.5 directly leads to \( \max_{1 \leq i \leq h} |V_i| \leq T(2S) \), which, together with Equation (12), implies that \( Q \geq S \cdot (|V|/T(2S) - 1) \) is valid. \( \Box \)

Theorem 4.6 concludes how the I/O lower bound of any composite algorithm depends on the upper bounds of \( \phi_j \) and \( \psi_j \). It not only gives a general theoretical result, but also presents a lower bound proof method which is to estimate \( \phi_j \) and \( \psi_j \) one by one. In addition, although Equation (11) is similar to Equation (1), it is easier to obtain \( T \) for a composite code.

### 4.2 I/O Lower Bounds for Direct Convolution

Figure 4 shows a DAG \( G(V, E) \) of the direct convolution. It is clear that the direct convolution consists of two steps. The first step is to generate a lot of product terms by using inputs in the input images and kernels. In DAG \( G(V, E) \), we call the product vertices as the vertices which are corresponding to the product terms generated by the first step in the direct convolution. Denote \( I_i \) as the \( i \)-th sliding input tensor with the size of \( W_{ker} \times H_{ker} \times C_{in} \) from an input image by using a sliding window. Let \( K_j \) be the \( j \)-th kernel whose size is also \( W_{ker} \times H_{ker} \times C_{in} \). For each \( I_i \) and \( K_j \), the first step generates
Proof. For a summation tree with \( k \) input vertices, the summation of the first two vertices would generate the first output vertex. Furthermore, we continue the process above. After the \((k - 2)\)-th internal vertex is added with the \( k \)-th input vertex, the final output would be generated. Hence, there are \((k - 2)\) internal vertices and 1 output vertex on a summation tree. \( \square \)

Based on the summation tree structure, we can calculate the total number of internal and output vertices in the DAG of a direct convolution.

**Lemma 4.8.** In a DAG of any direct convolution, the total number of internal and output vertices is

\[
|V_{\text{inter}} \cup V_{\text{out}}| = (2W_{ker}H_{ker}C_{in} - 1)W_{out}H_{out}C_{out}.
\]

**Proof.** It is obvious that the DAG of a direct convolution has \( W_{out}H_{out}C_{out} \) output vertices. Each output is the summation of the corresponding element product of \( I_i \) and \( K_j \), where \( I_i \) is the \( i \)-th sliding input tensor and \( K_j \) is the \( j \)-th kernel. \( I_i \) and \( K_j \) have the same dimension of \( W_{ker} \times H_{ker} \times C_{in} \).

Firstly, the two tensors \( I_i \) and \( K_j \) are associated with two input vertex sets. Secondly, after executing the corresponding element product of \( I_i \) and \( K_j \), we can obtain \( W_{ker}H_{ker}C_{in} \) product vertices which are \( W_{ker}H_{ker}C_{in} \) of the outputs of \( G_i(U_i, E_i) \). Thirdly, Lemma 4.7 indicates that, in order to sum \( W_{ker}H_{ker}C_{in} \) internal results based on the summation tree, the second step would generate another \( W_{ker}H_{ker}C_{in} - 2 \) internal vertices and 1 output vertex. Consequently, one output vertex depends on \( 2W_{ker}H_{ker}C_{in} - 2 \) internal vertices.

Since each output vertex is generated independently, no internal vertex would be shared by two different summation trees. Hence, the total number of internal and output vertices in DAG is 

\[
(2W_{ker}H_{ker}C_{in} - 1)W_{out}H_{out}C_{out}.
\]

For any two tensors \( a \) and \( b \) with the same dimension, denote \( a \odot b \) as the summation of all corresponding element products of \( a \) and \( b \). By this notation, the \( i \)-th output vertex \( O'_i \) in the \( j \)-th output channel can be represented as \( O'_i = I_i \odot K_j \) (Figure 4). Before estimating the upper bound \( T(S) \), we denote \( R \) as the maximum reuse number of each input (element) in an input image by different sliding windows, whose value is

\[
R = \frac{W_{ker}H_{ker}}{\mu^2},
\]

where \( \mu \) is the stride size. We will see that the \( T(S) \) relies on \( R \).

**Lemma 4.9.** In a direct convolution, \( \psi_1 = \varphi_1 \) is valid for the first step. Furthermore, for any positive integer \( h_1, \varphi_1(h_1) \leq 2\sqrt{Rh_1} \).

**Proof.** Let \( U \) be any vertex set whose dominator set \( D \) and minimum set \( M \) contain at most \( S \) vertices. Suppose \( |D \cap U_i| \leq h_1 \). In order to estimate \( \varphi_1 \) and \( \psi_1 \), we consider how many vertices in \( U \cap U_i \) can be generated by \( D \cap U_i \). Since \( G_i(U_i, E_i) \) has no internal vertices, all vertices generated by \( D \cap U_i \), can be used as the inputs of \( G_2(V_2, E_2) \). Hence, \( \psi_1 = \varphi_1 \) is valid.

Since \( |M| \leq S \) and the internal vertex sets of different summation trees are disjoint from each other, \( U \) can have nonempty intersections with internal vertex sets at most \( S \) summation trees, and each intersection has at least one distinct vertex in the minimum set. For any \( \tilde{O} = \{O_{i_1}^1, O_{i_2}^2, \ldots, O_{i_S}^S\} \) with \( S \) output vertices, each vertex can be formed by \( O_{i_0}^\mu = I_{i_0} \odot K_{j_0} \) (Figure 4). Without loss of generality, we assume that each \( I_i \) in the set \( I^1 = \{I_{i_1}, I_{i_2}, \ldots, I_{i_S}\} \) has at least \( \sqrt{Rh_1} \) entries in \( D \cap U_i \), while each \( I_r \) in the reset \( I^2 = \{I_{r+1}, I_{r+2}, \ldots, I_{i_S}\} \) has at most \( \sqrt{Rh_1} \) entries in \( D \cap U_i \).

On one hand, for the set \( I^1 = \{I_{i_1}, I_{i_2}, \ldots, I_{i_S}\} \), we can prove that \( k_0 \leq \sqrt{Rh_1} \). In the following, we verify this fact by reductio ad absurdum. Assume that \( k_0 > \sqrt{Rh_1} \). Since each \( I_i \in I^1 \) has at least \( \sqrt{R}S \) entries in \( D \cap U_i \), the set \( I^1 \) involves at least \( k_0 \sqrt{R}S \) vertices belonging to \( D \cap U_i \), while some of these vertices may be the same. As each input vertices can be reused at most \( R \) times, there exist at least \( k_0 \sqrt{R}S / R \) independent vertices in \( D \cap U_i \), and \( k_0 \sqrt{R}S / R > h_1 \), which

**Figure 4.** DAG of Direct Convolution.
contradicts with the fact \(|D \cap U_1| \leq h_1\). Thus, the assumption is not valid, and \(k_0 \leq \sqrt{R_h^1}\) is valid. Due to \(|D| \leq S, \bigcup_{k=1}^{h_0} K_k\) involves no more than \(S\) vertices in \(D\). Hence, the vertices in \(D \cap \bigcup_{k=1}^{h_0} K_k\) and \(D \cap \bigcup_{k=1}^{h_0} K_k^i\) can generate at most \(S \sqrt{R_h^1}\) products for \(O_{ik}^i (k = 1, 2, \ldots, k_0)\). On the other hand, for the set \(I^2 = \{l_{k1+1}, l_{k2+2}, \ldots, l_{k_0}\}\), since each \(l_i\) in \(I^2\) has at most \(\sqrt{R_h^1}\) entries in \(D\), at most \(S \sqrt{R_h^1}\) products can be formed by the vertices in \(D \cap \bigcup_{k=1}^{h_0} K_k\) and \(D \cap \bigcup_{k=1}^{h_0} K_k^i\).

In conclusion, \(D \cap U_1\) can generate at most \(2S \sqrt{R_h^1}\) in \(U \cap U_1\). This means that \(\varphi(h_1) \leq 2S \sqrt{R_h^1}\) is valid.

Lemma 4.10. In a direct convolution, for any positive integer \(h_2, \varphi_2(h_2) \leq h_2 - 1\).

Proof. Assume that a vertex set \(U\) has a dominator set \(D\) and a minimum set \(M\) satisfying \(|D \cap U_1| + |\Theta(D) \cap U_1| \leq h_2, |D| \leq S\) and \(|M| \leq S\). To deduce the upper bound of \(\varphi_2\), we only need to consider the vertices in \(U \cap U_2\) which can be formed by \(D \cap U_2\) and \(\Theta(D) \cap U_1\). As \(|D \cap U_2| + |\Theta(D) \cap U_1| \leq h_2\), at most \(h_2\) vertices would be the inputs of summation trees. By Lemma 4.7, such \(h_2\) vertices can generate at most \(h_2 - 1\) internal vertices in the intersections of \(V_1\) with \(S\) summation trees. Therefore, we get \(\varphi_2(h_2) \leq h_2 - 1\).

Lemma 4.9 and Lemma 4.10 lead to an estimation of \(T(S)\) directly.

Lemma 4.11. For a direct convolution, \(T(S) \leq 4S \sqrt{RS} + S - 1\).

Proof. By the definition of \(T\), we deduce

\[
T(S) \leq S \max_{k_1, k_2 \leq S} \{2S \sqrt{R_{k1}^1} + (k_2 + 2S \sqrt{R_{k1}^1} - 1)\} \leq 4S \sqrt{RS} - 1,
\]

where the final equality holds if and only if \(k_1 = S\) and \(k_2 = 0\).

Theorem 4.12. The I/O lower bound of a direct convolution (DC) is

\[
Q_{\text{lower \ DC}} = \Omega \left( \frac{W_{ker} H_{ker} C_{in} W_{out} H_{out} C_{out}}{4 \sqrt{RS}} \right).
\]  

(14)

Proof. By Theorem 4.6, Lemma 4.8 and Lemma 4.11, we have

\[
Q \geq \frac{2W_{ker} H_{ker} C_{in}^2 - 1}{8 \sqrt{2RS} + 2} - \frac{1}{S},
\]

which implies that (14) is valid.

It is worth mentioning that the derived lower bound is in the form of \(\Omega\) instead of a precise value. It provides the asymptotic relation between the data movement and the fast memory capacity when the problem scale is large enough.

4.3 I/O Lower Bounds for Winograd Algorithm

In Winograd algorithm, since the size of three transformation matrices \(A, B\) and \(L\) is small, we assume that they can be always stored in fast storage, and their volume can be ignored compared with the size \(S\) of the fast memory. Furthermore, as Winograd algorithm requires \(W_{ker} = H_{ker}\), we denote \(r\) as \(W_{ker}\) or \(H_{ker}\) briefly. As mentioned in Section 2.3, Winograd algorithm decomposes the output matrix on each given channel of a output image into several sub-domains whose size is \(e \times e\). Every output on each subdomain are calculated simultaneously using \(F(e, r)\). Figure 5 is a DAG \(G(V, E)\) of Winograd algorithm which consists four steps. In Figure 5, the red vertices represent the elements of three transformation matrices which would not involve any I/O procedure. The first step is a tensor conversion process. Using a sliding window, a sliding input tensor \(I_i\) with the size of \((e + r - 1) \times (e + r - 1) \times C_{in}\) is chosen from an input image, where is a positive integer. The first step transforms \(I_i\) into \(P_i\) by multiplying the transformation matrix \(B\) with the \((e + r - 1) \times (e + r - 1)\) matrix of \(I_i\) at each fixed channel. The size of \(P_i\) is also \((e + r - 1) \times (e + r - 1) \times C_{in}\). Similarly, by using \(L\) and the \(k\)-th kernel \(K_k\), another tensor \(J_k\) can be formed with the size of \((e + r - 1) \times (e + r - 1) \times C_{in}\). The second step is to execute the element-wise multiplication of \(P_i\) with \(J_k\), which results in a new tensor \(L_{i,k}\). The third step is to sum the elements of \(L_{i,k}\) along the channel direction through the summation tree. A \((e + r - 1) \times (e + r - 1)\) matrix \(S_{i,k}\) is obtained. The final step is to use the matrix \(A\) to transfer \(S_{i,k}\) into a \(e \times e\) matrix which would be \(e^2\) outputs on the \(i\)-th sub-domain at the \(k\)-th channel of an output image. It is worth mentioning that both the tensor conversion of the first step and the matrix conversion of the fourth step can be realized through a linear combination tree (Figure 5).

Similar to the summation tree, a linear combination tree is a sub-DAG with the tree structure in which the in-degree of internal and output vertices is at most two. All inputs of linear combination tree are multiplied with different coefficients respectively at first, and then summed together to the only one output.
Lemma 4.13. A linear combination tree with $k$ input vertices involves $2k - 2$ internal vertices and 1 output.

Proof. For a linear combination process with $k$ inputs, all inputs are multiplied respectively by different coefficients that are always stored at fast memory. This multiplication could result in $k$ internal vertices. Furthermore, $k$ internal vertices are summed together through a summation tree. From Lemma 4.7, another $k$ internal vertices and 1 output node are formed. Hence, the linear combination tree has $2k - 2$ internal vertices and 1 output.

Lemma 4.14. In a DAG of any winograd algorithm, the total number of internal and output vertices is

$$|\text{inter} \cup \text{out}| = O\left(\frac{2W_{\text{out}}H_{\text{out}}C_{\text{out}}(e + r - 1)^4}{e^2}\right).$$

Proof. A winograd algorithm has $W_{\text{out}}H_{\text{out}}C_{\text{out}}$ output vertices. Every $e^2$ outputs are calculated at once by using a $(e+r-1) \times (e+r-1) \times C_{\text{in}}$ input tensor $I_i$ and a $r \times r \times C_{\text{in}}$ kernel $K_k$. At the first step, $I_i$ and $K_k$ generate $P_i$ and $J_k$ respectively. $P_i$ and $J_k$ have the same dimension of $(e+r-1) \times (e+r-1) \times C_{\text{in}}$. Each vertex in $P_i$ is formed through a linear combination tree with $(e+r-1)^2$ inputs from the input matrix at some channel of $I_i$. By Lemma 4.13, $(2(e+r-1)^2 - 1)(e+r-1)^2 C_{\text{in}}$ vertices are generated. Similarly, each vertex in $J_k$ is formed through a linear combination tree with $r^2$ weights in $K_k$, which involves $(2r^2 - 1)(e+r-1)^2C_{\text{in}}$ vertices. In the second step, the corresponding element-wise multiplication of $P_i \odot J_k$ forms $(e+r-1)^3C_{\text{in}}$ vertices further. The third step is to add the elements in $A_{i,k}$ $(A_{i,k} = P_i \odot J_k)$ along the channel direction to deduce a matrix $\Pi_{i,k}$, which would generate $(C_{\text{in}} - 1)(e+r-1)^2$ vertices through $(e+r-1)^2$ different summation trees (by Lemma 4.7). Finally, the fourth step is to obtain $e^2$ outputs on the $i$-th sub-domain at the $k$-th channel of an output image. Since each vertex from the $e^2$ outputs is generated through a linear combination tree with the inputs of all $(e+r-1)^2$ elements in $\Pi_{i,k}$. By Lemma 4.13 again, the fourth step involves $(2(e+r-1)^2 - 1)(e+r-1)^2$ vertices. Since each $e^2$ output vertices are generated independently, the total number of internal and output vertices in DAG is $O(2W_{\text{out}}H_{\text{out}}C_{\text{out}}(e + r - 1)^4/e^2)$.

Let $\{G_1(U_1, E_1), G_2(U_2, E_2), G_3(U_3, E_3), G_4(U_4, E_4)\}$ be the multi-step partition of $G(V, E)$. Since $P_i$ and $J_k$ are obtained independently, we further divide the sub-DAG $G_1(U_1, E_1)$ into two small DAGs $G_{1,2}(U_{1,2}, E_{1,2})$ and $G_{1,3}(U_{1,3}, E_{1,3})$ where $G_{1,1}$ and $G_{1,2}$ are corresponding to the generation process of $P_i$ and $J_k$ respectively. As $r = e \pm 1$ is satisfied in Winograd algorithm, we can assume that $1/2 \leq r/e \leq 2$ in our estimation for $\varphi_i$ and $\psi_j$ ($1 \leq i \leq 4$).

Lemma 4.15. In Winograd algorithm, for any positive integer $h_1$, $\varphi_i(h_1) \leq \frac{6h_1(e + r - 1)^4}{e^r}$ and $\psi_j(h_1) \leq \frac{3h_1(e + r - 1)^2}{e^r}.$

Proof. Let $U$ be any vertex set whose dominator set $D$ and minimum set $M$ contain at most $S$ vertices. Assume that $|D \cap U_1| \leq h_1$. In order to estimate $\varphi_i$ and $\psi_j$, we consider the vertices in $U \cap U_1$ generated by $D \cap U_1$ and $D \cap U_2$ respectively. Denote $k_1 = |D \cap U_1|$ and $k_2 = |D \cap U_1|$ respectively. As $U_1, U_2$ is disjoint with $U_1, U_2$, we get $k_1 + k_2 \leq h_1. $ On one hand, in sub-DAG $G_1$, every $(e + r - 1)^2$ vertices in $D \cap U_1$ are used as the inputs of $(e + r - 1)^2$ linear combination trees. By Lemma 13, with $(e + r - 1)^2$ inputs, each linear combination tree can generate $2(e + r - 1)^2 - 2$ internal vertices and 1 output. Hence, every $(e + r - 1)^2$ vertices from $D \cap U_1$ would form at most $(e + r - 1)^2 - 2(e + r - 1)^2 - 2$ internal vertices and $(e + r - 1)^2$ outputs. Furthermore, since the reuse number of each input vertex is $(e + r - 1)^2/e^2$, $D \cap U_1$ can generate at most $2k_1(e + r - 1)^4/e^2$ vertices in which there are $k_1(e + r - 1)^2$ vertices in the output set of $G_1, G_1$. On the other hand, in sub-DAG $G_1$, every $r^2$ vertices in $D \cap U_2$ are used as the inputs of $(e + r - 1)^2$ combination trees, while any vertex in $D \cap U_2$ would not be reused. Similar to the discussion above, it is clear that $D \cap U_2$ could generate at most $2k_2(e + r - 1)^4/e^2$ vertices in which $k_2(e + r - 1)^2$ vertices are in the output set of $G_1, G_1$. Since $1/2 \leq r/e \leq 2$, we have $\varphi_i(h_1) \leq \max_{k_1, k_2 \leq h_1}(2(e + r - 1)^4(k_1^2 + k_2^2) \leq 6h_1(e + r - 1)^4(\frac{k_1}{e^2} + \frac{k_2}{r^2}) \leq \frac{3h_1(e + r - 1)^2}{e^r}$.

Lemma 4.16. In Winograd algorithm, $\psi_j = \varphi_j$ is valid for the second step. Furthermore, for any positive integer $h_2$, $\psi_j(h_2) \leq h_2 \sqrt{h_2} + (e + r - 1)^2 S \frac{\sqrt{h_2}}{e^2}.$

Proof. In the sub-DAG $G_2(U_2, E_2)$, there is no internal vertices. Hence, $\psi_j = \varphi_j$ is valid. Assume that a vertex set $U$ has a dominator set $D$ and a minimum set $M$ satisfying $|D \cap U_2| + |\Theta(D) \cap \Omega_1| \leq h_2$, $|D| \leq S$ and $|M| \leq S$. Since $M$ has no more than $S$ vertices, $U$ can have nonempty intersections with internal vertex sets of at most $S$ different linear combination trees of the fourth step. We note that every $(e + r - 1)^2$ outputs of summation trees in the third step, would be used as inputs of $e^2$ combination trees. Due to $|M| \leq S$ again, $U$ must intersect with at most $S(e + r - 1)^2/e^2$ independent summation trees of the third step. To estimate the upper bound of $\varphi_j$, we only need to consider the vertices in $U \cap U_2$ which are generated by $D \cap U_2$ and $\Theta(D) \cap \Omega_1$ for at most $S(e + r - 1)^2/e^2$ disjoint summation trees in the third step. Similar to the proof of Lemma 4.9, we can deduce that $\varphi_j(h_2) \leq h_2 \sqrt{h_2} + (e + r - 1)^2 S \sqrt{h_2}/e^2$. □
Lemma 4.17. In Winograd algorithm, for any positive integer \( h_3, \varphi_3(h_3) \leq h_3 - 1 \) and \( \psi_3(h_3) \leq \min\{ h_3/2, S(e + r - 1)^2/e^2 \} \).

Proof. By Lemma 4.7, it is clear that \( \varphi_3(h_3) \leq h_3 - 1 \). Based on the discussion in the proof of Lemma 4.16, for any \( U \) whose minimum set has at most \( S \) vertices, \( U \) must have nonempty intersections with internal vertex sets of at most \( S(e + r - 1)^2/e^2 \) independent summation trees of the third step. Hence, \( \psi_3(h_3) \leq S(e + r - 1)^2/e^2 \) is valid for any \( h_3 \geq 1 \). Furthermore, In the third step, none of the input and internal vertices in one summation tree appears as a vertex in another. Hence, at least two vertices in fast memory are needed to form one output vertex of a summation tree. This means \( \psi(h_3) \leq h_3/2 \). Consequently, \( \psi(h_3) \leq \min\{ h_3/2, S(e + r - 1)^2/e^2 \} \) is valid.

Lemma 4.18. In Winograd algorithm, for any positive integer \( h_4, \varphi_4(h_4) \leq \min\{ (2h_4 - 1)e^2, (2(e + r - 1)^2 - 1)S \} \).

Proof. Let \( U \) be any vertex set whose dominator set \( D \) and minimum set \( M \) satisfy \(|D \cup U_t| + \theta(D) \leq h_4, |D| \leq S \) and \(|M| \leq S \). Since each input of \( U_t \) is used as an input for \( e^2 \) linear combination trees, Lemma 4.13 leads to \( \varphi_4(h_4) \leq e^2(2h_4 - 1) \). In the fourth step, each linear combination tree has \( (e + r - 1)^2 \) inputs, and at most \( S \) linear combination trees have nonempty intersections with internal vertex sets of \( U \). By Lemma 4.13, we have \( \varphi_4(h_4) \leq (2(e + r - 1)^2 - 1)S \).

Based on the upper bounds of \( \varphi_i \) and \( \psi_i \) \( (1 \leq i \leq 4) \), it is easy to estimate \( T \) for Winograd algorithm.

Lemma 4.19. For Winograd algorithm,
\[
T(S) = O \left( \frac{(e + r - 1)^3}{er} S \sqrt{S} + \frac{6(e + r - 1)^2}{e^2} S \right). \quad (17)
\]

Proof. Set \( h(k_1, k_2) = k_2 + 3k_1(e + r - 1)^2/er \) for any integer \( k_1 \) and \( k_2 \). Denote \( T_1 \) and \( T_2 \) as \( T_1(k_1) = 6k_1(e + r - 1)^2/er \) and \( T_2(k_1, k_2) = h(k_1, k_2) \sqrt{h(k_1, k_2)} + \left( \frac{e + r - 1}{e^2} \right)^2 S \sqrt{h(k_1, k_2)} \).

By Lemma 4.15 - Lemma 4.18, we can deduce
\[
T(S) \leq S + T_1(S) + T_2(S, 0) + (e + r - 1)^2 \left( \frac{1}{e^2} + 2 \right) S. \quad (18)
\]

Therefore, it is easy to check that \( T_2(S, 0) \leq 2 \left( \frac{e + r - 1}{er} \right)^3 S \sqrt{S} \).

In conclusion, the equation (4.19) is valid.

So far, the lower bound of I/O complexity of Winograd algorithm can be established.

Theorem 4.20. The communication lower bound of Winograd algorithm (WA) is
\[
Q_{lower \ WA} = \Omega \left( \frac{W_{out}H_{out}C_{out}C_{in}(e + r - 1)r}{e \sqrt{S}} \right). \quad (19)
\]

Proof. By Theorem 4.6, Lemma 4.14 and Lemma 4.19, we have
\[
Q \geq S \cdot \left( \frac{2W_{out}H_{out}C_{out}C_{in}(e + r - 1)^4}{e^2T(S)} - 1 \right),
\]
which implies that (19) is valid.

5 Near I/O-Optimal Strategy

5.1 Methodology for Near I/O-Optimal Strategy

In the proposed general I/O lower bound theory, the highest order term in I/O lower bound result (11) must be determined by some \( \varphi_i \) due to the definition (5) of \( T \). Specifically, for the direct convolution, the maximum vertex generation function \( \varphi_2 \) for the last step determines the highest order term in I/O lower bound (Equation (14)). For Winograd algorithm, the highest order term in I/O lower bound (Equation (19)) comes from \( \varphi_3 \) for the third step, rather than \( \varphi_2 \) for the last step. As the highest order term in I/O lower bound result represents the main part of I/O number, the related \( \varphi_i \) points to the major process which involves the most I/O operations.

By the function \( \varphi_i \), which determines the highest order term in I/O lower bound result of a composite algorithm, we are able to find which data should be fully reused in the on-chip memory, and minimize the number of I/O operations during the \( i \)-th step of the composite algorithm. In detail, for the direct convolution, \( \varphi_2 \) which determines the highest order term in Equation (14), indicates that minimizing the number of I/O operations needs to maximize the output data reuse. For Winograd algorithm, \( \varphi_3 \) inspires us to maximize the data reuse of two temporary arrays which are involved during the third step.

After determining which data reuse should be exploited, the dataflow strategy can be designed to maximize the reuse of such data. In the following, we propose different schedules for the direct and Winograd convolutions by maximizing the reuse of output data and two temporary arrays respectively.

5.2 Dataflow Design for Direct Convolution

![Figure 6. I/O Optimal Dataflow for Direct Convolution.](image)

For the direct convolution, the highest order term in I/O lower bound (Equation (14)) comes from \( \varphi_2 \) for the last step.
φ₂ indicates that the output data reuse should be fully exploited, which implies that we need to use the least inputs to produce the most outputs. Hence, the dataflow design should assign most of the effective on-chip memory to portions of outputs. Figure 6 shows a sub-block of the output image with the dimension of \( x \times y \times z \). Based on the fundamental principle above, to reach the minimum off-chip memory access, we tend to choose \( xyz \approx S/N_p \) where \( N_p \) is the total number of active processors.

To compute the output sub-block \( x \times y \times z \), we need the inputs in the corresponding \( x' \times y' \) locations from all input channels (the yellow sub-block in an input image) and \( z \) kernels associated with the partial output channels (the yellow kernels), as shown in Figure 6. Since the on-chip memory is limited and tends to be used for storing the most outputs, it is necessary to load the required inputs and kernels by a series of stages, rather than at a time. During each stage, a portion of inputs \( x' \times y' \times \alpha \) (the black sub-block) and the corresponding weights \( H_{ker} \times W_{ker} \times \alpha \) of \( z \) kernels are loaded to the on-chip memory (Figure 6). Since each input of the \( i \)-th channel only can be reused by the weights of the \( i \)-th channel, rather than other channels. In order to put the larger output sub-block in the limited on-chip memory, we set \( \alpha = 1 \), which indicates that our dataflow design is to load a \( x' \times y' \) tile with a fixed channel index firstly and then slide the tile along the channel direction.

After loading a \( x' \times y' \) input tile and the corresponding weights of \( z \) kernels into the on-chip memory, a partial sum can be performed on the output sub-block. To update the whole output sub-block, we continuously slide the \( x' \times y' \) input tile along the channel direction, and load the corresponding inputs and weights (in the yellow blocks), and perform partial updates. Consequently, updating each output sub-block only needs to load the required inputs and weights from the off-chip memory to on-chip memory exactly once. Meanwhile, different output sub-blocks are updated by \( N_p \) processors in parallel.

In our dataflow design, there are \( (W_{out}H_{out}C_{out})/(xyz) \) output sub-blocks in total. To update each sub-block, we need \( x'y'C_{in} \) inputs from an input image and \( W_{ker}H_{ker}C_{in}z \) weights from \( z \) kernels. As \( R = W_{ker}H_{ker}/\mu^2 \), \( x' \approx \mu x \) and \( y' \approx \mu y \), the I/O volume for reading data is

\[
Q_{DC}^{reading} \approx \frac{H_{out}W_{out}C_{out}}{xyz} \left( H_{ker}W_{ker}C_{in}(z + \frac{xy}{R}) \right) \\
\geq H_{out}W_{out}C_{out}H_{ker}W_{ker}C_{in} \left( 2 \sqrt{\frac{1}{Rxyz}} \right), \tag{20}
\]

where the final equality holds if and only if \( xy = Rz \). By the fact \( R = W_{ker}H_{ker}/\mu^2 \), \( x' = \mu x \) and \( y' = \mu y \) again, the requirement of \( xy = Rz \) leads to \( x'y' = zW_{ker}H_{ker} \), which determines the optimal size of each \( x' \times y' \) tile. Further, the I/O volume for storing outputs is \( W_{out}H_{out}C_{out} \). When we choose \( xyz \approx S/N_p \) and \( xy = Rz \), the total I/O volume is

\[
Q_{DC} \approx \frac{2H_{out}W_{out}C_{out}H_{ker}W_{ker}C_{in}}{\sqrt{RS}/N_p} + H_{out}W_{out}C_{out}. \tag{21}
\]

If \( N_p = 1 \) and \( \frac{H_{ker}W_{ker}C_{in}}{\sqrt{R}} \gg 1 \) which is easily satisfied in CNN applications due to \( S \) usually being equal to or less than KB level, \( Q_{DC} \) reaches the I/O lower bound (Theorem 4.12). This fact indicates that, sequentially executing the dataflow and assigning most of the effective on-chip memory to the outputs can reach the minimum off-chip memory access. Otherwise, if we perform the dataflow in parallel, The equation (21) means that fully utilizing the on-chip memory owned by each processor to produce the partial sum could maximize the output data reuse and reduce the data transmission in the memory hierarchy.

In order to view the proposed dataflow at a high level, we conclude the details of this design as follows:

- The input data reuse is fully considered. In fact, one input is reused by weights of \( z \) kernels, and one weight is reused by \( x \times y \) outputs. On the other hand, one input is also reused by at most \( R \) sliding windows on each \( x' \times y' \) tile.
- The output data reuse is fully exploited. In fact, the partial sum can always stay in the on-chip memory during the update process, and they are just written back to the off-chip memory only once. To make sure the larger output sub-block can be loaded in the on-chip memory, the optimal tiling is designed to slide the \( x' \times y' \) tile along the channel direction, which reveals that the loading of inputs along the width and height directions should be considered prior to the channel direction.
- In order to achieve the I/O lower bound, the \( x \times y \times z \) output sub-block needs to satisfy \( xy = Rz \), which is called as the optimality condition in this work. Under this condition, \( x'y' = zW_{ker}H_{ker} \), which determines the optimal size of each input tile.

5.3 Dataflow Design for Winograd Algorithm

**Figure 7. I/O Optimal Dataflow for Winograd Algorithm.**
Similar to the analysis in the dataflow design for direct convolution, \( p_3 \) determining the highest order term in I/O lower bound of Winograd algorithm (Equation (19)), leads us to maximize the data reuse of temporary arrays involved during the third step.

To compute each \( x \times y \times z \) output sub-block, Winograd algorithm needs to partition further sub-block into \( xy/e^2 \) smaller sub-blocks each of which has the size of \( e \times e \times z \). Each \( e \times e \times z \) small sub-block is computed by using the corresponding \((e+r-1) \times (e+r-1)\) locations from all input channels of the input images (i.e., the yellow block in the input image) and \( z \) kernels associated with the parallel output channels (Figure 7), which are loaded into on-chip memory by a series of stages due to the limited on-chip memory. Based on the same discussion in the dataflow design, each stage loads a \((e+r-1) \times (e+r-1)\) input tile at an input channel (which means \( \alpha = 1 \)) and the corresponding \( r^2 \) weights at the same channel of a kernel, and then produce a partial sum \( \Lambda \) (Figure 7). We allocate two \((e+r-1) \times (e+r-1)\) temporary arrays in the on-chip memory for the summation of all partial sums along the channel direction. The first array is used to save the last summation result, and the second one is for the generation of a new partial sum. When a new partial sum is created in the second array, it would be added to the first array. After collecting all partial sums along the channel direction, the \((e+r-1) \times (e+r-1)\) summation matrix \( \Pi \) naturally generates in the first array (Figure 7), which would be multiplied with a transform matrix to deduce \( e \times e \) outputs in the same channel of the small output sub-block.

To complete the update of each small sub-block with the size of \( e \times e \times z \), each processor continuously loads the required inputs and weights (the red blocks in Figure 7), and performs partial updates. In order to exploit the parallelism of the computation of \( x \times y \times z \) outputs, every \( e^2 \) outputs rely on two \((e+r-1) \times (e+r-1)\) temporary arrays at a time. To maximize the data reuse of temporary arrays, we should use the most on-chip memory to store the \( 2xyz/e^2 \) required temporary arrays. Hence, our design chooses \( 2 \frac{(e+r-1)^2}{e^2} xyz \approx S/N_p \).

In the dataflow above, an output image is divided into \((W_{out}H_{out}C_{out})/(xyz)\) sub-blocks. For each sub-block, we need to load \( x'y'C_{in} \) inputs from an input image and \( zr^2C_{in} \) weights from \( z \) kernels. As \( \mu = 1 \) is only valid in Winograd algorithm, we have \( x' \approx x \) and \( y' \approx y \). The I/O volume for reading data can be estimated as follows

\[
Q_{WA \text{ reading}} \approx \frac{H_{out}W_{out}C_{out}}{xyz} (xyC_{in} + zr^2C_{in}) 
\geq H_{out}W_{out}C_{out}C_{in} \left( 2 - \frac{r}{\sqrt{xyz}} \right),
\]

where the final equality holds if and only if \( xy = r^2z \). Due to \( R = r^2 \) in Winograd algorithm, \( xy = r^2z \) leads to \( xy = Rz \), which is similar to the optimality condition for the dataflow of direct convolution. In addition, the I/O volume for writing outputs is \( W_{out}H_{out}C_{out} \). As \( 2 \frac{(e+r-1)^2}{e^2} xyz \approx S/N_p \), the total I/O volume is

\[
Q_{WA} \approx 2H_{out}W_{out}C_{out}C_{in}r(e + r - 1) \frac{e\sqrt{S/N_p}}{e} + H_{out}W_{out}C_{out}.
\]

As the proposed dataflow is similar to our design for the direct convolution, we just list two specific details in this design as follows:

- The dataflow design of direct convolution mainly focuses on the output data reuse, while the dataflow design of Winograd algorithm is to exploit the data reuse of temporary arrays and combine input data reuse in the best way. In addition, each \((e+r-1)^2\) inputs are reused by weights of \( z \) kernels, and each \( r^2 \) weights are reused by \( e^2 \) outputs.
- The parallelism of the computation of \( x \times y \times z \) outputs is fully considered. The update of every \( e \times e \) tiles at an output channel is performed in parallel. To achieve a high parallelism and data reuse, the most on-chip memory is for loading the temporary arrays.

6 Auto-Tuning for Implementation

6.1 Auto-Tuning Engine

The dataflow design above just provides a coarse-grained strategies to minimize the off-chip memory access. In order to achieve an optimal implementation, fine-grained computational schedule and memory access schedule are still needed. In this section, we mainly consider the optimal implementation on accelerators, such as GPU. Similar optimization can be used for other hardware backends.

![Figure 8. Auto-tuning Engine.](image)

For a given coarse-grained schedule, we define the configuration as a group of key performance parameters, including specific input shape and layout, number of threads in each thread block, tiling size, the shared memory size allocated to each thread block. Each configuration provides the description of an implementation way. All possible configurations constitute a configuration space whose size usually is over billions. In order to rapidly find the optimal choice in the huge space, we built an auto-tuning engine based on the learning-based cost modeling method. Figure 8 shows the overview of our auto-tuning engine, which consists of three
main components: a template manager that measures the execution time of any given configuration, and a cost model that predicts the cost of any given configuration, and a configuration explorer that searches promising new configurations.

**Template Manager:** In the low-level implementation, the proposed dataflow schedules are described as a template. Template manager is in charge of all schedule template, and generates various configurations for each template.

**Cost Model:** We use XGBoost method [4] to train a gradient tree boosting model as the cost model to predict the runtime of any configuration. The model is trained using measurement data, which is consisted of a configuration and its execution time. During the auto-tuning process, the cost model would be updated periodically as the configuration explorer finds more configurations and updates the training dataset.

**Configuration Explorer:** During the configuration searching, the configuration explorer uses the trained cost model to predict the cost of any configuration, and searches the potential optimal configuration in the search space. Although the cost model could reduce the time to evaluate configurations, the searching process is still expensive due to a huge search space with over billions of size.

### 6.2 Searching Based on Optimality Condition

In order to improve the search efficiency, we construct a searching domain based on the optimality condition, which is helpful for significantly reducing the size of search space. Besides, we use a heuristic method to rapidly search promising configurations.

**Searching Domain:** Table 1 presents the searching domain. According to the dataflow design, the tile is loaded into on-chip memory as a whole, which implies that $xyz \leq S_b$. $S_b$ is the shared memory size for each block. Furtermore, the optimality condition $xy = Rz$ leads to $z \leq \sqrt{S_b/R}$ and $xy \leq \sqrt{S_bR}$. In order to achieve a high level parallelism, at least two thread blocks are guaranteed to concurrently run on one streaming multiprocessor (SM), resulting in $S_b \leq S_{sm}/2$.

| Parameters     | Definition and Constrains            |
|----------------|---------------------------------------|
| $H_{in}, W_{in}, C_{in}$ | Input shape                           |
| $H_{out}, W_{out}, C_{out}$ | Output shape                          |
| $H_{ker}, W_{ker}$ | Kernel shape                          |
| CHW, CWH, HWC | Layout                                |
| $S_{sm}$ | Shared memory size of SM             |
| $S_b$ | Shared memory size for each block     |
| $x, y, z$ | Tile size which are the factor of $H_{out}, W_{out}, C_{out}$, $xyz \leq S_b$, $z \leq \sqrt{S_b/R}$ and $xy \leq \sqrt{S_bR}$ |
| $N_{ct}, N_{ct}, N_{ct}$ | Thread numbers which are the factor of $x, y, z$ |

**Searching Process:** To find many promising configurations, the configuration explorer performs a searching process to select configurations from the searching domain. At the beginning of the searching process, $n_s$ random configurations are chosen as initial guesses. During each searching step, the configuration explorer randomly walks from each initial guesses to its nearby configuration in the searching domain. Each random walk tends to converge on a configuration that has lower predicted costs. Consequently, the $n_s$ parallel random walks generate $n_t$ promising configurations, which are saved as the initial guesses for the next searching step. Until all predicted costs of the $n_t$ selected configurations are lower than a threshold, they are outputted as a solution.

### 6.3 Auto-tuning Process

The proposed auto-tuning engine searches the optimal implementation iteratively. Each iteration consists of three stages: (1) **Model Training** that trains the cost model, (2) **Configuration Searching** that applies the cost modal to select multiple promising configurations, (3) **Dataset Updating** that measures the new configurations and updates the dataset. Until the measurement runtime of the selected configurations does not decrease for hundreds of iterations, the auto-tuning process would end. The parallel strategy corresponding the best selected configuration is the implementation of our near-optimal I/O dataflow.

### 7 Evaluation

In this section, we evaluate our proposed I/O optimal dataflow designs for the direct convolution and Winograd algorithm respectively. We first evaluate the optimal dataflow implementations derived from the proposed auto-tuning engine, and then compare the speeds of different automation searching methods, and finally demonstrate our implementation can achieve performance speedup in end-to-end cases. Our evaluation is mainly performed in the NVIDIA 1080Ti and V100 GPUs.

To evaluate our work from a broad scale, we use synthetic convolution cases with different $W_{ker}$ $H_{ker}$ and the stride $\mu$. On the one hand, in cuDNN library, the direct implementation of convolutions mainly has two approaches: direct convolution and image2col method [16], where the direct convolution occasionally fails for some different input shapes, and the image2col method are usually better than the direct convolution. In order to present the superior of our implementations, we compare with the best one of two direct implementations in cuDNN. On the other hand, the indirect implementation of convolutions in cuDNN mainly is Winograd algorithm. The following evaluation compares the runtime of different convolution kernels of ours and cuDNN, where CUDA-9.0 and cuDNN-7.0.3 are used.

To evaluate the auto-tuning engine, we first compare the searching performance of our proposed searching method with different searching strategies in TVM, which represents the state-of-the-art technique for auto-tuning a convolution
operation, and then compare our searched implementation with the optimal solution provided by TVM.

7.1 Performance Comparison with cuDNN

![Figure 9](image_url)

**Figure 9.** Performance Comparison of Dataflow Design over cuDNN for Direct Convolution and Winograd Algorithm on 1080Ti GPU. For all convolutions, $H_{\text{ker}} \times W_{\text{ker}} = 3 \times 3$ and $C_{\text{in}} = 256$.

Figure 9 shows the performance comparison on the implementations of the direct convolution and Winograd algorithm respectively. We can find that our I/O optimal dataflow implementations can achieve 3.32× performance speedup on average. We have three important observations from the results.

Firstly, the benefit from the dataflow is consistent as the $H_{\text{in}}$ and $W_{\text{in}}$ increase, and our methodology can have significant performance improvement. This mainly owes to the design of exploiting input and output data reuse. I/O dataflow design maximizes the data reuse of the $x' \times y'$ tile at a given channel. When $H_{\text{in}}$ and $W_{\text{in}}$ become larger, the more data reuse can be achieved.

Secondly, when $C_{\text{out}}$ is small, the dataflow contribution is always higher for the direct convolution. Conversely, when $C_{\text{out}}$ is large, the benefit from the dataflow is always higher for Winograd algorithm.

Third, on the whole, the dataflow benefits decrease as the stride $\mu$ increase. This is because the motivation of I/O dataflow design is to minimize the off-chip memory access. When the stride $\mu$ is larger, more off-chip memory accesses gradually become independent with each other.

Furthermore, Figure 10 shows the batched convolution test. It is clear that, compared with scaling the batch size of cuDNN, our I/O optimal dataflow still achieves 1.51× performance speedup on average. On the one hand, For a given batch-size, when $H_{\text{in}}$ and $W_{\text{in}}$ increases, the performance improvement from our dataflow design gradually becomes apparent. On the other hand, when $H_{\text{in}}$ and $W_{\text{in}}$ are small, the dataflow contribution is small. However, when $H_{\text{in}}$ and $W_{\text{in}}$ become larger, the convolution needs more I/O operations, and the benefit from the dataflow becomes greater. When $H_{\text{in}}$ and $W_{\text{in}}$ are 112, the speedup becomes larger with the batch size increasing.

![Figure 10](image_url)

**Figure 10.** Performance Comparison of Dataflow Design over cuDNN for Batched Direct Convolution Test on 1080Ti GPU.

7.2 Performance Comparison with TVM

![Figure 11](image_url)

**Figure 11.** Comparison of Different Automation Methods.

Table 2 presents the detail information about configuration space, the number of iterations and the best solution’s runtime of the auto-tuning engine and TVM during searching the optimal implementations of different convolution layers in AlexNet on V100 GPU. We have three important observations from the experiment results. Firstly, the constraints for the templates and the proposed searching domain can successfully reduce the size of configuration space to about 20% – 50% for the direct convolution and 50% for Winograd algorithm. The compression ratio for Winograd algorithm is not small, because the size of original configuration space is small (see the space size in TVM) and the
flexibility for implementation design is limited essentially. Secondly, the proposed auto-tuning engine finds the final solution faster than TVM, thanks to the proposed searching domain. Thirdly, the final configuration found by the auto-tuning engine usually has a shorter runtime than the best solution in TVM. The three facts above demonstrate that the auto-tuning engine has the strong scaling efficiency for searching optimal configuration.

Figure 11 shows the comparison of different automation methods for searching an optimal direct convolution implementation of the conv1 in Table 2 on V100 GPU. The ML-based model in TVM starts with no training data and uses the collected data to improve itself. The X-axis is the number of iterative steps and the Y-axis is the floating-point arithmetic efficiency in GFlops. From Figure 11, we observe a similar trend for all automation methods. During the iterations, each automation method gradually finds the better configuration with higher floating-point arithmetic efficiency. It should be noted that the proposed auto-tuning engine is able to find better configurations much faster than the others. This mainly owes to two reasons. On the one hand, the I/O optimality condition is used to prune configuration search space, which leads to the proposed searching domain. On the other hand, the parallel searching method effectively improves the searching process in the searching domain.

7.3 Performance Comparison on CNN Models

The modern CNN models introduce many layer structures, such as convolution layer. More specifically, the convolution layer is important and popular in many state-of-the-art CNN models such as ResNet [29], VggNet, SqueezeNet [15] and so on. In the following, we demonstrate that our proposed auto-tuning engine can help for accelerating CNN inference.

Figure 12 shows the performance comparison of the dataflow design and cuDNN on different CNN models. For SqueezeNet, Vgg-19, ResNet-18, ResNet-34 and Inception-v3, our optimal implementation can achieve 2.67×, 1.09×, 1.02×, 1.09× and 1.23× performance speedup respectively compared with using cuDNN. The performance benefits come from two aspects. The different kinds of convolutions take up the main part of CNN models. Besides, for each convolution layer, the proposed auto-tuning engine could find a better implementation than cuDNN.

7.4 Sensitivity for GPU Architecture

To demonstrate the scalability on GPU architecture, we evaluate the proposed dataflow with auto-tuning engine on Pascal and Maxwell architectures. We use one kind of Pascal architecture: GTX Titan X. Figure 13 shows the evaluation results on the above two architectures. The proposed dataflow is much faster than cuDNN. Compared with the solution of TVM, for the direct convolution, the improvement of our implementation on these architectures can achieve about 1.05× and 1.27× respectively. For Winograd algorithm, the speedups of our dataflow are 1.12× and 1.01× respectively on these architectures.
In addition, we compare the dataflow design with MIopen library on AMD GFX906 platform (Pre-Wukong GPU), and use ROCm-2.9 and MIopen-2.1 in this evaluation. On average, the performance improvement is up to 2.86x and 1.10x for direct convolution and Winograd algorithm respectively. Besides, compared with the solution of TVM, our optimal implementation achieves 1.21x speedup for the direct convolution and 1.03x speedup for Winograd algorithm. We find that our optimal implementation is well ported to different architectures and achieve a consistent performance speedup.

8 Related Work

The red-blue pebble game is widely used in theory analysis of communication lower bound to guide optimal communication strategy. After Hong & Kung established the I/O complexity theory [17], Savage developed the notion of S-span to derive Hong-Kung style lower bounds [23]. Kwasniewski et al. provided a new proof of I/O complexity of matrix-matrix multiplication and designed a parallel algorithm to reach its lower bound [21]. Although the red-blue pebble game model has been proposed for many years [1–3, 12, 24, 28], it is still difficult to use this model to establish I/O lower bounds of composite algorithms which involve several different kinds of computational patterns [13]. To get around the essential difficulties, the lower bound of composite algorithms was considered by modifying the red-blue pebble game model into a red-blue-white pebble game model [13], which uses some restrictions on models, such as the limitation of disallowing re-computation of values on the DAG. However, such restrictions seem inappropriate for the lower bound analysis of some convolution algorithms. For example, Winograd algorithm allows re-computation of values to decrease the number of I/O operations. In order to solve the difficulties, this work at first establishes a general I/O lower bound theory for any composite algorithm based on the red-blue pebble game model without introducing the limitation of disallowing re-computation of values on the DAG.

For convolutions in DNN, Demmel et al. estimated the minimum memory access of direct convolution by solving an intricate optimization problem [11]. Furthermore, Chen et al. transformed the direct convolution into Matrix-matrix multiplication, and successfully deduced the lower bound of the off-chip communication of direct convolution in CNN accelerators [6]. However, our work is the first time to perform a systematic analysis of diverse convolution algorithms in deep learning by developing a general I/O lower bound theory for any composite algorithm. It is worth mentioning that the I/O lower bound in Equation (14) is equivalent to the I/O lower bounds of direct convolution in [6, 11], while our proposed result on direct convolution is the tighter lower bound with a more precise coefficient. Besides, the previous works [6, 11] mainly focus on the direct convolution, and seem not easy to adapt to Winograd algorithm. However, to the best our knowledge, this work at first establishes the I/O lower bound of Winograd algorithm.

To fully exploit the research efforts from convolution algorithm and micro-architecture optimizations, many software libraries, such as cuDNN, are launched to pack these optimizations together in order to reduce programming difficulty. However, due to the increasing demand on performance, directly using the software libraries sometimes is not satisfactory. In recent years, the convolution optimization is widely concerned. Some excellent implementations are proposed for different convolution algorithms [7, 18, 22, 25, 26]. However, most of the studies mainly focus on the optimization from experience[33]. In this work, we try to propose the I/O optimal dataflow based on the lower bound theoretical analysis. By comparing the I/O volume of the dataflow with the lower bound, we find the optimality condition for I/O optimal design. On the other hand, in the convolution optimization, the combinatorial choices of memory access, threading pattern, and novel hardware primitives creates a huge configuration space. A common way is to adopt a predefined cost model to guide the search, but building an accurate cost model is difficult due to the increasing complexity of modern hardware. To addresses these challenges, some searching strategies based on the learning-based cost models are proposed, in which TVM represents the state-of-the-art auto-tuning technique. However, it still needs a large search cost due to the huge search space. In this work, this work firstly considers to use the deduced optimality condition to fully reduce the size of search space, and proposes an effective parallel searching method to find the optimal implementation, which leads to an effective auto-tuning engine. Compared with TVM, it could faster find a better final solution.

9 Conclusion

In this paper, we have tackled the challenge of building I/O lower bound theory and designing I/O optimal dataflow implementations for convolutions. By fine-grain viewing the recent lower bound theory developed under the red-blue pebble game model, we fully consider the influence of sub-computations to each other, and propose a general I/O lower bound theory for composite algorithms. Based on the proposed theory, we establish the communication lower bound results for the typical representatives of direct and indirect convolution methods, which are the direct convolution and Winograd algorithm. Furthermore, for each approach, we design the I/O optimal dataflow strategy based on the lower bound analysis. By developing an auto-tuning engine for searching the optimal configuration, we push the envelope of performance of our dataflow designs further.
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References
[1] Alok Aggarwal and S. Vitter, Jeffrey. 1988. The Input/Output Complexity of Sorting and Related Problems. Commun. ACM 31, 9 (Sept. 1988), 1116–1127. https://doi.org/10.1145/48329.48535
[2] Grey Ballard, James Demmel, Olga Holtz, and Oded Schwartz. 2011. Minimizing Communication in Numerical Linear Algebra. SIAM J. Matrix Anal. Appl. 32, 3 (2011), 866–901. https://doi.org/10.1137/090769156
[3] Grey Ballard, James Demmel, Olga Holtz, and Oded Schwartz. 2013. Graph Expansion and Communication Costs of Fast Matrix Multiplication. J. ACM 59, 6, Article 32 (Jan. 2013), 23 pages. https://doi.org/10.1145/2395116.2395121
[4] Tianqi Chen and Carlos Guestrin. 2016. XGBoost: A Scalable Tree Boosting System. In Proceedings of the 22nd ACM SIGKDD International Conference on Knowledge Discovery and Data Mining (San Francisco, California, USA) (KDD ’16). Association for Computing Machinery, New York, NY, USA, 785–794. https://doi.org/10.1145/2939672.2939706
[5] Tianqi Chen, Thierry Moreau, Ziheng Jiang, Liammin Zheng, Eddie Yan, Haichen Shen, Meghan Cowan, Leyuan Wang, Yuwei Hu, Luis Ceze, Carlos Guestrin, and Arvind Krishnamurthy. 2018. TVM: An Automated End-to-End Optimizing Compiler for Deep Learning. In 13th USENIX Symposium on Operating Systems Design and Implementation (OSDI 18). USENIX Association, Carlsbad, CA, 578–594. https://www.usenix.org/conference/osdi18/presentation/chenn
[6] Xiaoming Chen, Yinhe Han, and Yu Wang. 2020. Communication Lower Bound in Convolution Accelerators. In 2020 IEEE International Symposium on High Performance Computer Architecture (HPCA). 529–541. https://doi.org/10.1109/HPCA47549.2020.00050
[7] Yu-Hsin Chen, Joel Emer, and Vivienne Sze. 2016. Eyriiss: A Spatial Architecture for Energy-Efficient Dataflow for Convolutional Neural Networks. SIGARCH Comput. Archit. News 44, 3 (June 2016), 367–379. https://doi.org/10.1145/3007787.3001177
[8] Yu Cheng, Duo Wang, Pan Zhou, and Tao Zhang. 2017. A Survey of Model Compression and Acceleration for Deep Neural Networks. CoRR abs/1710.09282 (2017). http://arxiv.org/abs/1710.09282
[9] Sharan Chetlur, Cliff Woolley, Philippe Vandermersch, Jonathan Cohen, John Tran, Bryan Catanzaro, and Evan Shelhamer. 2014. cuDNN: Efficient Primitives for Deep Learning. CoRR abs/1410.0759 (2014). arXiv:1410.0759 http://arxiv.org/abs/1410.0759
[10] Jee W. Choi, Amik Singh, and Richard W. Vuduc. 2010. Model-Driven Autotuning of Sparse Matrix-Vector Multiply on GPUs. SIGPLAN Not. 45, 5 (Jan. 2010), 115–126. https://doi.org/10.1145/1837853.1693471
[11] James Demmel and Grace Dinh. 2018. Communication-Optimal Convolutional Neural Nets. CoRR abs/1802.06905 (2018). http://arxiv.org/abs/1802.06905
[12] James Demmel, Laura Grigori, Mark Hoemmen, and Julien Langou. 2012. Communication-optimal Parallel and Sequential QR and LU Factorizations. SIAM Journal on Scientific Computing 34, 1 (2012), A206–A239. https://doi.org/10.1137/080713992
[13] Venmugil Elango, Fabrice Bastello, Louis-Noël Pouchet, J. Ramanujam, and P. Sadayappan. 2014. On Characterizing the Data Movement Complexity of Computational DAGs for Parallel Execution. In Proceedings of the 26th ACM Symposium on Parallelism in Algorithms and Architectures (Prague, Czech Republic) (SPAA ’14). Association for Computing Machinery, New York, NY, USA, 296–306. https://doi.org/10.1145/2621669.2621694
[14] Andrew G. Howard, Menglong Zhu, Bo Chen, Dmitry Kalenichenko, Weijun Wang, Tobias Weyand, Marco Andreetto, and Hartwig Adam. 2017. MobileNets: Efficient Convolutional Neural Networks for Mobile Vision Applications. CoRR abs/1704.04861 (2017). http://arxiv.org/abs/1704.04861
[15] Forrest N. Iandola, Matthew W. Moskewicz, Khalid Ashraf, Song Han, William J. Dally, and Kurt Keutzer. 2016. SqueezeNet: AlexNet-level accuracy with 50x fewer parameters and <1MB model size. CoRR abs/1602.07360 (2016). http://arxiv.org/abs/1602.07360
[16] Yangqing Jia. 2014. Learning semantic image representations at a large scale. Ph.D. Dissertation. UC Berkeley. https://escholarship.org/uc/item/64c2v6sn
[17] Hong Jia-Wei and H. T. Kung. 1981. I/O Complexity: The Red-Blue Pebble Game. In Proceedings of the Thirteenth Annual ACM Symposium on Theory of Computing (Milwaukee, Wisconsin, USA) (STOC ’81). Association for Computing Machinery, New York, NY, USA, 326–333. https://doi.org/10.1145/800706.802486
[18] Jihyuck Jo, Suchang Kim, and In-Cheol Park. 2018. Energy-Efficient Convolution Architecture Based on Rescheduled Dataflow. IEEE Transactions on Circuits and Systems I: Regular Papers 65, 12 (2018), 4196–4207. https://doi.org/10.1109/TCASI.2018.2840092
[19] Xiao Jiajun and Peng Jiean. 2019. Trade-offs between computation, communication, and synchronization in stencil-collective alternate update. CCF Transactions on High Performance Computing 1 (07 2019). https://doi.org/10.1007/s42514-019-00011-x
[20] Jehandad Khan, Paul Fultz, Artem Tamazov, Daniel Lowell, Chao Liu, Michael Meleasa, Murali Nathendramad, Kamil Nasyrov, Ilya Perminov, Tejas Shah, Vasilii Filippov, Jing Zhang, Jing Zhou, Bragadeesh Natarajan, and Mayank Daga. 2019. MIOpen: An Open Source Library For Deep Learning Primitives. CoRR abs/1910.00078 (2019). http://arxiv.org/abs/1910.00078
[21] Grzegorz Kwasniewski, Marko Kabić, Maciej Besta, Joost VandeVondele, Raffaele Solcà, and Torsten Hoefler. 2019. Red-Blue Pebbling Revisited: Near Optimal Parallel Matrix-Matrix Multiplication. In Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis (Denver, Colorado) (SC ’19). Association for Computing Machinery, New York, NY, USA, Article 24, 22 pages. https://doi.org/10.1145/3295500.3356181
[22] Maurice Peemen, Arnaud A. A. Setio, Bart Mesman, and Henk Corstjens. 2013. Memory-centric accelerator design for Convolutional Neural Networks. In 2013 IEEE 13th International Conference on Computer Design (ICCD). 13–19. https://doi.org/10.1109/ICCD.2013.6657019
[23] John E. Savage. 1995. Extending the Hong-Kung Model to Memory Hierarchies. In Proceedings of the First Annual International Conference on Computing and Combinatorics (COCOON ’95). Springer-Verlag, Berlin, Heidelberg, 270–281.
[24] John E. Savage. 1997. Models of Computation: Exploring the Power of Computing (1st ed.). Addison-Wesley Longman Publishing Co., Inc., USA.
[25] Nimish Shah, Paragkumar Chaudhari, and Kuruvilla Varghese. 2018. Runtime Programmable and Memory Bandwidth Optimized FPGA-Based Coprocessor for Deep Convolutional Neural Network. IEEE Transactions on Neural Networks and Learning Systems 29, 12 (2018), 5922–5934. https://doi.org/10.1109/TNNLS.2018.2815085
[26] Runbin Shi, Zheng Xu, Zhihao Sun, Maurice Peemen, Ang Li, Henk Corporaal, and Di Wu. 2015. A Locality Aware Convolutional Neural Networks Accelerator. In Proceedings of the 2015 Euromicro Conference
on Digital System Design (DSD ‘15). IEEE Computer Society, USA, 591–598. https://doi.org/10.1109/DSD.2015.70

[27] Karen Simonyan and Andrew Zisserman. 2015. Very Deep Convolutional Networks for Large-Scale Image Recognition. http://arxiv.org/abs/1409.1556

[28] Edgar Solomonik, Aydın Buluç, and James Demmel. 2013. Minimizing Communication in All-Pairs Shortest Paths. In 2013 IEEE 27th International Symposium on Parallel and Distributed Processing. 548–559. https://doi.org/10.1109/IPDPS.2013.111

[29] Christian Szegedy, Sergey Ioffe, and Vincent Vanhoucke. 2016. Inception-v4, Inception-ResNet and the Impact of Residual Connections on Learning. CoRR abs/1602.07261 (2016). http://arxiv.org/abs/1602.07261

[30] Junmin Xiao, Shigang Li, Baodong Wu, He Zhang, Kun Li, Erlin Yao, Yunquan Zhang, and Guangming Tan. 2018. Communication-Avoiding for Dynamical Core of Atmospheric General Circulation Model. In Proceedings of the 47th International Conference on Parallel Processing (Eugene, OR, USA) (ICPP 2018). Association for Computing Machinery, New York, NY, USA, Article 12, 10 pages. https://doi.org/10.1145/3225058.3225140

[31] Da Yan, Wei Wang, and Xiaowen Chu. 2020. Optimizing Batched Winograd Convolution on GPUs. In Proceedings of the 25th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (San Diego, California) (PPoPP ’20). Association for Computing Machinery, New York, NY, USA, 32–44. https://doi.org/10.1145/3332466.3374520

[32] Xiaoyang Zhang, Junmin Xiao, and Guangming Tan. 2020. Communication Lower Bounds of Convolutions in CNNs. In Proceedings of the 32nd ACM Symposium on Parallelism in Algorithms and Architectures (Virtual Event, USA) (SPAA ’20). Association for Computing Machinery, New York, NY, USA, 591–593. https://doi.org/10.1145/3350755.3400267

[33] Xiaoyang Zhang, Junmin Xiao, Xiaobin Zhang, Zhongze Hu, Hongrui Zhu, Zhongbo Tian, and Guangming Tan. 2019. Tensor Layout Optimization of Convolution for Inference on Digital Signal Processor. 184–193. https://doi.org/10.1109/ISPAD-Cloud-SustainCom-SocialCom48970.2019.00036

[34] Xiaoyu Zhang, Xinyu Zhou, Mengxiao Lin, and Jian Sun. 2018. ShuffleNet: An Extremely Efficient Convolutional Neural Network for Mobile Devices. In 2018 IEEE/CVF Conference on Computer Vision and Pattern Recognition. 6848–6856. https://doi.org/10.1109/CVPR.2018.00716

[35] Jie Zhao and Peng Di. 2020. Optimizing the Memory Hierarchy by Compositing Automatic Transformations on Computations and Data. In 2020 53rd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO). 427–441. https://doi.org/10.1109/MICRO50266.2020.00044

[36] Aojun Zhou, Anbang Yao, Yiwen Guo, Lin Xu, and Yurong Chen. 2017. Incremental Network Quantization: Towards Lossless CNNs with Low-Precision Weights. CoRR abs/1702.03044 (2017). http://arxiv.org/abs/1702.03044