10-bit rapid single flux quantum digital-to-analog converter for ac voltage standard

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Abstract. Digital-to-analog (D/A) converters based on rapid single flux quantum (RSFQ) technology are under development for ac voltage standard applications. We present design and test results on a prototype 10-bit version integrated on a single chip. The 10-bit chip includes over 6000 Josephson junctions and consumes a bias current exceeding 1 A. To reduce the effects of the high bias current on circuit operation, a custom design method was employed in part and large circuit blocks were divided into smaller ones. The 10-bit chips were fabricated and tested at low speed. The test results suggested that our design approach could manage large bias currents on the order of 1 A per chip.

1. Introduction
A digital-to-analog (D/A) converters based on rapid single flux quantum (RSFQ) technology enables synthesis of arbitrary waveforms with fundamental accuracy [1]-[3]. Our goal is to develop RSFQ D/A converter systems for establishing a new generation of ac voltage standards based on the Josephson effect [4]. The first step to achieving an ac Josephson voltage standard is accurate characterization of the thermal voltage converters that are the principal devices used to set the present ac voltage standards. For this purpose, an RSFQ D/A converter is required to generate sufficiently high voltages on the order of 100 mV zero-to-peak. Previously, we successfully demonstrated operation of the key subsystems, a pulse-number multiplier (PNM) [5], a pulse distributor (PD) [4] and voltage multipliers (VMs) [6].

This paper presents design and test results of 10-bit RSFQ D/A converters in which all the subsystems are integrated on a single chip. The single-chip 10-bit D/A converter is a prototype that provides all functions required for ac voltage standards although the output voltage level is insufficient to use for practical applications. The 10-bit chip including more than 6000 Josephson junctions consumes bias currents exceeding 1 A in total. The key to such a large-scale circuit is how to manage the high bias current on the order of 1 A per chip.

2. 10-bit RSFQ D/A converter
The RSFQ D/A converter consists of three main subsystems, PNM, PD and VM. The operation principle and system design concept are presented in detail in [4]. Figure 1 shows a block diagram of a 10-bit RSFQ D/A converter chip including auxiliary circuits for testing. Dc-to-sfq converters for probe signal inputs and sfq-to-dc converters for monitor signal outputs are added between the subsystems for testing the separate circuit blocks. A prescaler (PRSC), a cascade of 10 T flip-flops, is used to test the
PNM operation. This prototype D/A converter has all the necessary functions for synthesis of arbitrary waveforms with definable rms values, while the maximum output voltage, 20 mV, is still insufficiently low for practical applications.

![Block diagram of a 10-bit RSFQ D/A converter chip.](image1)

2.1. Standard-cell-based design

The first version of the 10-bit D/A converter was implemented using our standard cell library on a 1.6 kA cm\(^{-2}\) Nb junction technology [7]. The subsystem blocks were constructed by simply connecting the standard cells. Figure 2 shows an example of a 1-bit slice of PD consisting of Josephson transmission lines (JTLs), splitters (SPs), pulse switches (PSWs) and a nondestructive readout (NDRO). The whole D/A converter was divided into six blocks each of which had a separate bias line as listed in Table 1. The VM block was the largest one consuming a bias current of 0.9 A and including 5331 junctions. The total bias current was 1.07 A and the number of junctions was 6524 for the overall chip.

![Standard-cell-based implementation of a 1-bit slice of PD.](image2)
Table 1. Circuit blocks in the first version of the 10-bit RSFQ D/A converter.

| Circuit block | Bias current (mA) | Num. of JJs | Description                                      |
|---------------|-------------------|-------------|-------------------------------------------------|
| I/O           | 28                | 175         | Dc-to-sfq and sfq-to-dc converters               |
| PNM           | 25                | 168         | PNM core                                        |
| PNM-RO        | 1.2               | 8           | Ring oscillator in PNM                          |
| PD            | 92                | 668         | 10-bit PD                                       |
| VM            | 902               | 5331        | 10-bit VM                                       |
| PRSC          | 24                | 173         | Prescaler and sfq-to-dc converters              |
| **Total**     | **1072**          | **6524**    |                                                 |

The circuits were fabricated and tested at low speed. Numerous routines were run but we could not obtain an operating chip even if wafer parameters such as the junction critical current density, the sheet resistance and the pattern shifts were sufficiently close to target values. Typical results were as follows: when only the I/O block was fed with a bias current and the other blocks were not, the I/O circuits, dc-to-sfq and sfq-to-dc converters, seemed to work correctly; the bias margins of the I/O circuits rapidly decreased with increase of the bias current for a large circuit block, the VM or PD block. Thus, we could not operate the whole circuit at the appropriate bias points. We have concluded that the main cause for the imperfect circuit operation was magnetic fields induced by the bias currents [8][9].

2.2. Improved design

Although a standard-cell-based design is a reliable and powerful method for developing large-scale digital circuits, this approach inherently implies hardware overhead. Standard cells generally have buffer junctions at input and output ports for direct connection with each other. Such buffer junctions, which dose not contribute to logic functions, consumes bias currents and increases delays in signal propagation between the cells. In the second design, we tried removing the buffer junctions to reduce the bias current. Removing the buffer junctions generally causes reduction of operating margins for the circuit parameters, so that the redesigned circuits were carefully optimized. If the margins did not reach sufficient values, typically +/-25%, the removed junction was put back in the circuit. To minimize the design cost, we applied the custom design approach only to portions which included much redundancy. For the same reason, standard cells with complicated functions such as TFF, DFFC and NDRO were unchanged and used as they were in the original form. Figure 3 shows new implementation of a 1-bit slice of PD, which has slightly smaller operating margins than those for the standard-cell-based implementation in figure 2. Table 2 summarizes the bias currents and the number of junctions for the second version. The bias current of the PD block, the second largest block in the first design, was significantly reduced because the original PD in figure 2 included a lot of JTLs only for interconnection.

![Figure 3. Custom-designed implementation of a 1-bit slice of PD.](image-url)
While PD was efficiently improved by removing the junctions, it was difficult to reduce the bias current for VM, the largest block, because VM includes almost no redundant junction. We therefore divided the VM block into two parts in order to reduce the effects of the magnetic fields induced by the high bias current. As a result, the largest bias current decreased to 450 mA for the second design. In addition, the bias lines from bonding pads to the VM blocks were laid out so as to be sandwiched with grounded Nb layers for shielding the induced magnetic field.

| Circuit block | Bias current (mA) | Num. of JJs | Description |
|---------------|-------------------|-------------|-------------|
| I/O           | 16                | 121         | Dc-to-sfq and sfq-to-dc converters |
| PNM           | 27                | 185         | PNM core    |
| PNM-RO        | 0.88              | 6           | Ring oscillator in PNM |
| PD            | 52                | 462         | 10-bit PD   |
| VM1           | 443               | 2624        | VM (10th bit) |
| VM2           | 449               | 2655        | VM (1st - 9th bits) |
| PRSC          | 19                | 142         | Prescaler and sfq-to-dc converters |
| Total         | 1007              | 6195        |             |

A mask layout for the second version consisted of four 5-mm chips including the 10-bit D/A converter (figure 4), test circuits for the PNM and PD subsystems, and a parametric test chip. After screening wafers by parametric tests, we successfully tested individual PNM and PD at low speed. Figure 5 shows experimental waveforms of a 10-bit PD. The experimental bias margins were typically +/- 18% for PNM and +/-25% for PD.

Unfortunately, we found a mistake in the layout of the 10-bit D/A converter when we proceeded to test the 10-bit chips. The error we made was only one but serious: a confluence buffer in the EOP line between PNM and PD (see figure 1) was placed in a wrong direction, so that we could test only two functions of the subsystems: PNM’s TR generation and PD’s TR transmission. Figure 6 shows operation of PNM and PD integrated in the 10-bit D/A converter, which confirms the generation of 1024 SFQ pulses at each RIN input and the transmission of them. When the bias currents for the other blocks were set to the designed value, the PNM bias margin for the TR generation was +/-16% and the PD bias margin for the TR transmission was +/-36%. The results suggests that the effect of the large bias current is negligible for the second version. The third version of the 10-bit D/A converter in
which the confluence buffer direction was corrected was already designed, and will be fabricated and tested shortly.

Figure 5. Operation of a stand-alone 10-bit PD.

Figure 6. Operation of PNM in a 10-bit D/A converter. Only the TR generation and the TR transmission were tested.

3. Conclusion
10-bit RSFQ D/A converters were designed, fabricated and tested, which is a prototype with all the necessary functions for ac voltage standard applications. Based on unsuccessful results on the first version, the chip design was improved by reducing the bias currents for circuit blocks. While correct operations of newly designed subsystems were confirmed, complete testing of the whole 10-bit D/A converter was not available because of a careless mistake in layout. Partial test results on the 10-bit chip suggested that the effects of the bias-current-induced magnetic field were sufficiently suppressed for the improved version.

References
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