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Experimental realization of a Coulomb blockade refrigerator

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We present an experimental realization of a Coulomb blockade refrigerator (CBR) based on a single-electron transistor (SET). In the present structure, the SET island is interrupted by a superconducting inclusion to permit charge transport while preventing heat flow. At certain values of the bias and gate voltages, the current through the SET cools one of the junctions. The measurements follow the theoretical model down to \( \sim 80 \, \text{mK} \), which was the base temperature of the current measurements. The observed cooling increases rapidly with decreasing temperature, in agreement with the theory, reaching about a 15 mK drop at the base temperature. The CBR appears as a promising electronic cooler at temperatures well below 100 mK.

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Over the past several decades, there has been continuous growth of research dedicated to thermoelectrics in a variety of nanostructures (see Refs. [1–3] and references therein) and, in particular, to electronic microrefrigerators [4,5]. The first quantum dot refrigerator (QDR) for cryogenic temperatures was proposed by Edwards in 1993 [6,7]. In the QDR discrete energy levels of the dot are tuned to cool the electronic Fermi-Dirac distribution of a small reservoir. Soon afterwards, it was demonstrated in a different device [8] that the electrons can be cooled down below the phonon temperature of the lattice. These cooling effects have been observed in several different systems, such as a normal metal-insulator-superconductor (NIS) tunnel junction [8–10] and with improved performance in a related SINIS device with a double junction configuration [11,12]. Also, the exact realization of the above mentioned QDR was shown later in a two-dimensional (2D) electron gas [13]. All of these devices, which are able to cool down on-chip electronic systems to subkelvin temperatures, have potential scientific and commercial applications, especially when size, weight, and ease of operation become important. Examples of possible applications are microbolometers, discussed in Ref. [14]. Recently, several implemented coolers on a Si\(_n\)N\(_n\) membrane [15] with a transition-edge sensor for high-resolution x-ray spectroscopy [16] have been demonstrated. These refrigerators work most of the time in the temperature range of 300–100 mK. They perform suboptimally at lower temperatures, due to several reasons, including excess quasiparticle population in a superconductor [17,18], leakage of the junctions [19], and a low electron-electron scattering rate [13].

In this Rapid Communication, we present an experimental realization of a type of cooler that has been recently proposed by some of the authors [20]. A Coulomb blockade refrigerator (CBR) is based on thermal transport through a fully normal single-electron transistor (SET) [21]. The relative temperature drop is expected to increase when the base temperature is lowered, which we verify here experimentally down to 80 mK. This feature makes the CBR suited for temperatures below 100 mK, and could be used in cascade coolers as the last stage, for example, in combination with a superconducting refrigerator [22]. Here we want to emphasize the most important feature of the CBR. In contrast to the NIS cooler, the operating point can be optimized by the bias and the gate voltages at any given temperature. For example, at a base temperature of 20 mK, which is possible to achieve with standard dilution refrigerators, a temperature of \( \sim 5 \, \text{mK} \) can be reached by the CBR assuming no extra heat leaks.

Figure 1 shows the principle of the operation of the cooler. The SET has two NIN tunnel junctions with tunneling resistances \( R_{T,k} \) each, formed between two normal metal (N) electrodes separated by a thin insulator (I) layer. We define the order of the junctions as \( k = 1, 2 \), where 1 is the “cold” junction and 2 is the “hot” junction. Our cooler is biased by voltage \( V \) transporting electrons through the SET, first to the island through the “hot” junction, then out of the island through the “cold” junction. When the SET island has \( n \) excess electrons, the electrostatic energy is \( E = E_c(n-n_g)^2 \), where \( E_c = e^2/2C_\Sigma \) is the charging energy, and \( C_\Sigma \) is the total capacitance of the SET island. The electrostatic energy is controlled by tuning the gate position \( n_g \equiv -C_gV_g/e \), where \( C_g \) and \( V_g \) are the gate capacitance and voltage, respectively. For simplicity, we define the two extreme gate values that will be used later: (i) gate closed \( (n_g = 0) \) and (ii) gate open position \( (n_g = 0.5) \).

In this experiment, we focus on the low-temperature regime, where the number of excess electrons on the island is restricted to \( n = 0 \) or 1. An electron that tunnels into the island through junction 2 changes \( \Delta E_2 = eV/2 + E_c(1-2n_g) \). Similarly, an electron that tunnels out of the island through junction 1 changes \( n \) from 1 to 0 for an energy cost \( \Delta E_1 = eV/2 - E_c(1-2n_g) \). The tunneling electrons distribute the energy evenly to their respective heat baths formed by the junction electrodes with typically about \( 10^9 \) free electrons in each. The energy \( \Delta E_2 \) is added to the heat bath of junction 2 at a temperature \( T_2 \), heating that junction, while the energy \( \Delta E_1 \) is removed from the junction 1 heat bath at a temperature \( T_1 \), cooling that junction. At the optimum point of \( n_g \) and \( V \), where \( \Delta E_1 = 2k_BT_1 \), the cooling power of the junction 1 is given by [20]

\[
\dot{Q}_{\text{opt}} \approx 0.31 \frac{(k_BT_1)^2}{e^2R_{T,1}}.
\]
Next we consider the conditions to observe a temperature drop in the CBR. As presented in Fig. 1(b), substrate phonons exchange heat with electrons via electron-phonon coupling

\[ Q_{e-ph} = \Sigma_k \left( T_k^f - T_k^p \right) \]

where \( \Sigma \) is a constant specific to the electrode material, \( T_k^f \) is the volume of that electrode, \( T_k^p \) is the temperature of the phonons, and \( T_p \) is the temperature of the phonon bath. Since \( Q_{e-ph} \) is proportional to the electrode volume, the CBR junction electrodes need to be small, as well as thermally insulated to prevent heat leaks from outside and between each other, as indicated in Fig. 1(b) by the S parts. Finally one needs temperature probes to measure \( T_1 \) and \( T_2 \). To realize the CBR, we make use of several different types of high-quality Al junctions, all contacting Cu, compatible with cofabrication of other metallic structures [15,16,22].

In the following, we describe the present realization of the proof-of-concept CBR that is shown in a scanning electron micrograph (SEM) in Figs. 2(a) and 2(b). The device is made by electron beam lithography and a three-angle shadow evaporation technique [23]. First, a 20 nm layer of Al forms the superconducting inclusion, outer leads, fingers for the NIS temperature probes, and Al “dots” [see the inset in Fig. 2(b)]. Next, a 25 nm layer of Cu, evaporated at a different angle, creates normal metal parts that form clean contacts to the superconducting inclusion from one side and to Al “dots” on the other side. Short Cu intermediate leads that are connected to the outer leads are formed at this step as well. In situ thermal oxidation followed after the second metal evaporation to form a thin Al₂O₃ layer over Al to provide the insulator for tunnel junctions. In the last evaporation step, 25 nm thick Cu electrodes form tunnel junctions for the SET, for the NIS probes, and connections to the intermediate leads. Connections to the outer leads are assumed to be transparent junctions between two Cu layers, which are, however, slightly oxidized in between. Underneath all of the leads, except for the gate electrode, we use a ground plane made out of 50 nm of copper covered by 50 nm of Al₂O₃. Here, the ground plane serves the purpose of reducing the leakage current in the subgap region of the NIS thermometer [24,25], and suppresses voltage noise in general.

The SET junctions are made by the laterally proximized tunnel junction technique [26], where the small Al “dots” (100 nm × 100 nm) are in direct contact with a bigger volume of normal metal Cu that suppresses the superconductivity by the inverse proximity effect [27–29]. The inset in Fig. 2(b) shows the lateral junction with an Al “dot” (colored blue) that is connected on the left side by the NIN tunnel junction to the island to be cooled, and to the SET island through a clean NN contact on the right side. Two fully normal NIN tunnel junctions of the SET were made intentionally unequal in resistance, functioning as thermally insulated junctions for the SET to the NIS thermometer [24,25], and suppresses voltage noise in general.

Next, we present the measurement data that characterize the SET and the NIS temperature probes. We conduct our experiments in a ⁴He dilution refrigerator at a bath temperature \( T_{bath} \). In Fig. 3(a), the measured current voltage characteristic (\( I-V \)) of the SET is shown as blue dots. The dots appear as vertical lines due to the gate voltage sweep recorded at each bias voltage point. The slope in the gate open position is constant around zero bias, demonstrating the absence of a superconducting gap, meaning that the SET junction electrodes are normal. The theoretical model used in the inset and in the main panel is based on the theory of sequential single-electron tunneling [21]. The fit to the \( I-V \) curve gives values \( E_c = 78 \mu eV \) for the charging energy, and the tunneling resistances are \( R_{T,1} = 103 \, k\Omega \) and \( R_{T,2} = 448 \, k\Omega \).
define the base temperature of the bath as well as on the bias and gate voltages. We measured temperature probes. The observed cooling depends on the voltage is swept over a few gate periods, at constant current bias electrostatic potential of the island. At each bias point, the gate in Fig. 2(a). The voltage bias is applied to the right lead of the SET and at the same time the gate voltage is used to tune the in Fig. 2(a). The lower inset shows the measured full calibration obtained from the $I$-$V$ curves in the main panel for bias currents of 1, 3, and 14 pA (shown as black, blue, and purple dots from bottom to top, respectively).

In Fig. 3(b), we characterize the NIS thermometer probe by measuring the temperature sweep of its $I$-$V$. The curves are well separated for different temperatures. The solid gray line in Fig. 3(b) indicates 3 pA, which we have chosen as a biasing current for the temperature probe. This value is in the temperature sensitive region, not influenced by the Andreev current leakage [30–32] that appears as a constant slope at low temperature sensitive region, not influenced by the Andreev current leakage [30–32] that appears as a constant slope at low temperature sensitive region, not influenced by the Andreev current leakage [30–32] that appears as a constant slope at low temperature sensitive region, not influenced by the Andreev

The experimental setup to test CBR performance is shown in Fig. 2(a). The voltage bias is applied to the right lead of the SET and at the same time the gate voltage is used to tune the electrostatic potential of the island. At each bias point, the gate voltage is swept over a few gate periods, at constant current bias for temperature probes. The observed cooling depends on the bath temperature as well as on the bias and gate voltages. We define the base temperature $T_{e,0}$ as the electronic temperature observed at the gate closed position, meaning zero current through the SET; here no cooling or heating takes place at the junctions. The temperature traces obtained by the NIS thermometer at different bath temperatures are presented in Fig. 4. The measured thermal voltages across the NIS probes and the outer leads are converted into temperature with a calibration [8,14,33,34] [see the upper inset in Fig. 3(b)] with respect to the bath temperature of the dilution refrigerator. The measurement data shown in the left column [Figs. 4(a)–4(c)] and in the right column [Figs. 4(d)–4(f)] were obtained at base temperatures of 111 and 83 mK, respectively. Both columns from top to bottom present the temperature traces of junction 1 [shown in Figs. 4(a) and 4(d)] and of junction 2 [shown in Figs. 4(b) and 4(e)], and the current through the SET [shown in Figs. 4(c) and 4(f)] during the gate voltage sweep. The cooling $\Delta T$ appears as a dip below $T_{e,0}$ indicated by the dashed lines, and the signal above the line indicates heating. The solid red lines shown in all the panels present the theoretical model to be described. We measured similar temperature traces at various bath temperatures. At each bath temperature, the drop $\Delta T$ was averaged over repeated gate sweeps and the standard deviation was calculated. The result is shown in Fig. 5(a) for three different voltage bias values indicated by orange circles, blue squares, and red triangles. The error bars are $\pm 2\sigma$ confidence intervals estimated from the observed scatter.

Next, we describe the theoretical model presented by the lines in Figs. 4 and 5. The electron temperatures $T_1$ and $T_2$ are obtained as a solution to the steady state heat balance equation $Q_{SET}+Q_{e-ph}=0$ for both junctions $k=1, 2$, where $Q_{SET}$ is the heat flow through the junctions based on a sequential single-electron tunneling model and cotunneling [20]. We estimate that in the present structure at $T_{e,0}=83$ mK the temperature drop is reduced by 11% due to cotunneling. We assume $T_p=T_{e,0}$ in the expression of electron-phonon coupling $Q_{e-ph}$. The volume of the cooled island is approximately $\Omega \equiv 5 \times 10^{-21}$ m$^3$. We obtain a fit $\Sigma=4 \times 10^8$ W K$^{-5}$/m$^{-3}$ by assuming that at the gate open position the heat flow through the junctions is equal to Joule heating, $Q_{SET}=IV/4$, distributed equally among the four electrodes of the SET.

The observed cooling increases rapidly, in agreement with the theory towards low temperatures, giving a maximum value of $\Delta T=15 \pm 1.15$ mK for a bias voltage of 60 $\mu$eV at
FIG. 5. (Color online) (a) Observed cooling \(\Delta T\) (see the inset for definition) for three different voltage bias values over the temperature range from 200 down to 80 mK. The data sets obtained by averaging over all realizations within a \(\pm 5 \mu\text{eV}\) range are shown for mean bias values of 60 \(\mu\text{eV}\) (orange circles), 40 \(\mu\text{eV}\) (blue squares), and 20 \(\mu\text{eV}\) (red triangles), from top to bottom. The error bars are calculated as a standard deviation for the data. The theoretical predictions of \(\Delta T\) for the three voltage bias values (60, 40, and 20 \(\mu\text{eV}\)) are shown as orange, blue, and red solid lines, respectively. The dashed lines show predictions for a CBR with tunneling resistances that are ten times higher than in the present experiment. As a reference, we show the dashed-dotted red line (20 \(\mu\text{eV}\)), which is identical to the one that is shown in Fig. 5(a) as a red curve, with \(R_{T,k}\) values obtained from the experiment. To reach lower electronic temperatures in the present configuration, one can thus benefit from higher tunneling resistances of the junctions and lower bias voltages. The higher tunneling resistances thus would decrease the cooling power [see Eq. (1)], but on the other hand, cooling required to reach lower electronic temperatures is significantly smaller as well.

In conclusion, we have shown the experimental realization and demonstrated the proof-of-concept performance of a Coulomb blockade refrigerator. The present realization of the device measured down to 80 mK demonstrates about a 15% temperature drop which increases rapidly towards lower temperatures.

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