Aquarium: Cassiopea and Alewife Languages

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Abstract
This technical report describes two of the domain specific languages used in the Aquarium kernel code synthesis project. It presents the language cores in terms of abstract syntax. Cassiopea is a machine description language for describing the semantics of processor instruction sets. Alewife is a specification language that can be used to write machine-independent specifications for assembly-level instruction blocks. An Alewife specification can be used to verify and synthesize code for any machine described in Cassiopea, given a machine-specific translation for abstractions used in the specification. This article does not include an introduction to either the Aquarium system or the use of the languages. In addition to this version of the article being a draft, the Aquarium project and the languages are work in progress. This article cannot currently be considered either final or complete.

1 Introduction
The goal of the Aquarium project is to synthesize the machine-dependent parts of an operating system. This has the potential to greatly reduce the amount of work needed to port an operating system to a new machine architecture. It also potentially reduces the depth of knowledge needed to do that work – currently an OS port requires deep expert knowledge of both the OS and the new machine architecture – and with luck the overall amount of time involved as well.

This document does not discuss either code synthesis or OS porting in any detail. It is intended as a supplement to other project publications, which should in general be read first. While this document includes discussions of and rationales for language features (as well as absence of language features) these discussions assume familiarity with the surrounding context.

The two languages described in this document are Cassiopea\(^1\), which is a register-transfer-list-style machine description language used for writing down the semantics of processor instruction sets, and Alewife, which is a specification or modeling language used for writing down machine-independent specifications for assembly language code blocks to be synthesized.

Cassiopea also includes material for writing machine-dependent specifications (this is the target for the Alewife translator), a concept of mapping modules used by the Alewife translator, and a simple representation of basic blocks in assembly language. These are described in this document.

This document does not, however, describe any of the other languages or file formats used in the Aquarium project or any of the Aquarium tools.

The document is structured with six parts:

- The Cassiopea language and abstract syntax (Sec. 3)
- Cassiopea types (Section 4)
- Cassiopea semantics (Section 5)
- The Alewife language and abstract syntax (Section 6)
- Alewife types and semantics (Section 7)
- Alewife translation to Cassiopea (Section 8)

2 Notation
In the abstract syntax, type judgments, and semantics judgments we use italics for metavariables (e.g., \(v\)) and for words corresponding to types in the abstract syntax (e.g., declaration). We use typewriter font for words that correspond to language keywords. The notation \(\overline{a_i}\) means “a sequence of one or more \(a\), each to be referred to elsewhere as \(a\).” If there are no references outside the overbar, the subscript may be left off. Epsilon (\(\epsilon\)) appearing in syntax represents an empty production. The notation “...” represents a string literal with arbitrary contents.

Bitvectors (machine integers) may be any width greater than zero. Bitvector constants are represented as 0b\(C\), which can be thought of as an explicit sequence of zeros and ones. The number of bits in a bitvector constant (that is, the number of digits) gives its type. Thus, 0b00 and 0b0000 are different. In the concrete syntax, bitvector constants whose size is a multiple of 4 can also be written in the form 0x\(C\). These are desugared in the parser and not shown further in this document.

\(^1\)Cassiopea is named for a jellyfish that features symbiotic photosynthetic algae, which is for some reason spelled without the customary ‘i’.
The Cassiopea and Alewife syntax should be considered disjoint. Some elements are the same in each, but these are specified separately regardless. They use the same metavariables as well, which should not be mixed; any language construct in a judgment should be all Cassiopea or all Alewife. In a few places mixing is needed, in which case the translation defined in Section 8 is applied to allow inserting Alewife fragments into Cassiopea terms. The Alewife rules in Section 7 do use the same environments as the Cassiopea rules. These should be construed as holding only Cassiopea elements. Further details can be found in Section 7.

3 Cassiopea Overview

This section covers the abstract syntax for Cassiopea.

Cassiopea is a register-transfer-list style language: it models instructions as non-Turing-complete procedures that update a machine state. Its executable semantics are covered in Section 5.

We model the machine from the assembly-language programmer’s perspective. In particular, we do not treat memory as a huge block of address space but instead treat it in small chunks passed in from somewhere else. We model both control registers and general-purpose registers as well as other machine state such as whether interrupts are enabled.

Furthermore we must allow assembler labels, which have addresses, but those addresses are not resolved until after programs are compiled and linked and must be treated as abstract.

Notation. We use the following metavariables:

- \( x, y, z \) Program variables (binders)
- \( r \) Registers (abstract)
- \( C \) Integer constants (written in decimal)
- \( \theta b C \) Bitvector constants (written in binary)
- \( \tau \) Types
- \( v \) Values
- \( e \) Expressions
- \( S \) Statements
- \( i, j \) Rule-level integers

(Other constructions are referred to with longer names.)

A number of constructions are lists written out in longhand (with a null case and a cons case) – these are written out in longhand so that typing and semantic judgments can be applied explicitly to each case, in order to, for example, propagate environment updates correctly.

Identifiers and Variables. Identifiers are divided syntactically into seven categories:

- \( x_{\text{mem}} \) are identifiers bound to memory regions, which are second-class.
- \( x_{\text{func}} \) are identifiers bound to functions, which are second-class.
- \( x_{\text{proc}} \) are identifiers bound to procedures, which are second-class.
- \( x_{\text{op}} \) are identifiers bound to instructions ("operations"), which are akin to procedures but distinguished from them.
- \( x_{\tau} \) are identifiers for type aliases, which are bound to base types in declarations.
- \( x_{\text{module}} \) are the names of "modules", which are used to select among many possible groups of lowering elements.
- Other identifiers \( x \) are used for other things, and should be assumed to not range over the above elements.

Note that all identifiers live in the same namespace, and rebinding or shadowing them is not allowed. All these identifiers can be thought of as variables, in the sense that they are names that stand for other things. All of them are immutable once defined, including the ordinary variables \( x \) that contain plain values.

Types. Types are divided syntactically into base types (integers, booleans, strings, bitvectors, etc.) and others (memory regions and functions). User functions may handle only base types. Furthermore, memory regions and functions are second-class for reasons discussed below and are excluded in various places in the syntax and the typing rules.

We use index typing to capture the bit width of values.

Registers. Registers are represented in the specification with the metavariable \( r \), which stands for the underlying abstract identity of a register. Declaring a register, e.g., with

\[
\text{letstate } x : C \text{ reg as shown in Figure 2, allocates a fresh register } r \text{ and binds the variable } x \text{ to it. A subsequent declaration of the form let } y : C \text{ reg } = x \text{ creates another variable } y \text{ that refers to the same underlying register. One might think of registers as numbered internally. We use the form letstate control } x : C \text{ reg to declare specific control registers, which are treated differently by the framing rules. The additional keyword dontgate inhibits state gating for the register; this should be used for flags registers and anything similar that is implicitly used by all ordinary code.}
\]

Some registers have associated with them a text form, which is declared separately and is the form an assembler expects to parse. The Capstan uses this to extract an assembly program from aquarium’s internal representation. It is referred to by attaching the suffix .txt to the/a register variable. As some registers are not directly addressable by the assembler (e.g., they might be subfields of some larger addressable unit or nonaddressable internal state), not all registers have a text form. This is not readily checked statically, at least not without introducing specific additional machinery, so invalid .txt references fail at assembly code extraction time.

The type of a register is \( C \text{ reg } \), which is a register that holds a \( C \)-bit bitvector. The bitvector value in question can be updated by assigning a new value; this is a statement \( (e_1 := e_2) \) and can only happen in places where statements are allowed. The construction "\( e \) reads a register."
This restriction could be relaxed if we wanted to model various historic machines. Thus a memory region of type 32 bit 4 len 32 ref has 4 32-bit values in it, which can be addressed at byte offsets 0, 4, 8, and 12. These values can of course be changed, like values in registers.

Memory regions are named with identifiers. These names, and memory regions themselves, are not first-class; variables are not allowed to range over them. Also note that memory regions are a property of programs (and thus are declared in specifications) and not a property of the machine as a whole.

**Pointers.** A pointer literal has the form \((x_{\text{mem}}, C)\), in which \(x_{\text{mem}}\) is the region name and \(C\) is the offset, shown in Figure 1. Because memory regions are second-class, \(x_{\text{mem}}\) must be specifically one of the available declared memory regions. Pointer literals exist in the abstract syntax, but are not allowed in the concrete syntax except in specifications. The only way to get a pointer value is to look up a label (discussed immediately below) or have it provided in a register as part of the initial machine state.

A pointer literal is treated as a bitvector of the same width, so one can appear in a register or in memory. However, we enforce a restriction (not captured in the semantics rules so far) that no value in the initial machine state, whether in a register or in memory, is a pointer unless required to be so by the precondition part of the specification. All other values are restricted to be plain bitvector values.

Addition and subtraction are allowed on pointers and they change the offset, but other bitvector operations (e.g., multiply) are disallowed and fail. Similarly, attempting to fetch from or store to a plain bitvector that is not a pointer fails. Note however that we do not statically distinguish

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The reader will note that the semantics rules for machines and declarations do not provide initial values for registers. Instead, executions are defined in terms of some initial register state (and also some memory state), which is required to have the right registers to match the machine definition. This allows reasoning about the execution of programs and program fragments in terms of many or all possible initial states. These issues are discussed further below.

**Memory.** A memory region has the type \(C_1\) bit \(C_2\) len \(C_3\) ref, shown in Figure 1. This refers to a memory region that has \(C_2\) cells, each of which stores a bitvector of width \(C_1\). This memory region is addressed with pointers of width \(C_3\). Note that we assume byte-addressed machines, and for the purposes of both this specification and our implementation, we assume bytes are 8 bits wide. (This restriction could be relaxed if we wanted to model various historic machines.) Thus a memory region of type 32 bit 4 len 32 ref has 4 32-bit values in it, which can be addressed at byte offsets 0, 4, 8, and 12. These values can of course be changed, like values in registers.

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pointers and plain bitvectors. (We could have used flow-sensitive typing to reason about when registers and memory cells contain pointers and when they do not; but this adds substantial complexity and for our problem domain does not provide significant value.) Instead, we step to failure at runtime. This can be seen in the semantics rules.

Fetching from a pointer takes the form \texttt{fetch} (e, C). Storing to a pointer takes the form \texttt{store} (e, C). The extra constant C specifies the width of the cell pointed to. (This is not an offset.) Because we do not check pointers statically, we do not know the memory region being pointed to and cannot look up its cell size; thus we need the width explicitly for typing. It is checked at runtime.

**Labels.** As mentioned above, the term “label” means an assembler label or linker symbol. These have addresses (or depending on how one looks at them, they are addresses) and those addresses are constants, but the constants are not known at assembly time, so we must model them abstractly.

When one declares a memory region, one may attach a label to it, which is an additional identifier. This identifier is created as a variable of type \texttt{C label} in Figure 1. The value is a pointer to the first entry in the region, and a single type subsumption rule allows this value to be accessed and placed in an ordinary register or variable of suitable bitvector type. The intended mechanism is that for each machine the preferred instruction on that machine for loading assembler symbols into a register can be defined to take an operand of type \texttt{C label}, and then its value can be assigned to the destination register. This type restriction on the operand is sufficient to synthesize programs that use labels correctly.

**Code Positions and Branching.** Cassiopea code blocks may contain branches, either forward within the block (branching backwards is forbidden) or to a single external assembler label outside the block. This model is sufficient for our block-oriented synthesis approach; more complex control flow can be handled with multiple blocks.

Consequently, a branch may either go to the external assembler label (which terminates execution of the current block) or skip zero or more instructions. We model branch targets as an 8-bit skip count. In Figure 2, the statement \texttt{BRANCH(0bC)} skips 0bC instructions; \texttt{BRANCH(0xff)} jumps to the external label. This statement may be used to define both conditional and unconditional branch instructions. Such instructions should be defined to take an operand of type \texttt{8 bit} to choose the branch destination. This magic number should then be printed to the output assembly text using the built-in function \texttt{text1label}, which replaces it with a valid assembler label, either the selected external label string or a scratch label attached to the proper destination instruction.

Specifications do not need to be directly concerned with internal branches, which occur or not as needed. However, external branches are part of a block’s specification; typically the purpose of a block with an external branch is to test some condition and then either branch away or fall through to the next block. It is thus necessary to be able both to name the external label to use and to specify the conditions when it should be reached. For this purpose a predicate \texttt{branchto} is provided. It may appear in the postcondition and governs the exit path from the block: if forced to true, the block branches to the external assembler label, and if false, the block falls through from its last instruction. The concrete syntax is \texttt{branchto(dest)} which also sets the assembler label used to dest. It is not valid to name more than one such assembler label.

Note that the assembler labels used in branching are, though also assembler labels, a separate mechanism unrelated to the labels attached to memory regions; they are code labels rather than data labels and inherently work differently.

Also note that the implementation is slightly more complicated than the description given above and the rules given in the semantics section. In the implementation, the magic number that triggers an external branch is not 255 but the number l such that l added to the instruction number of the branch adds to 99. This detail affects only intermediate synthesis results in the internal format; the extracted assembly code is the same.

**Register Sets.** Register sets are second-class elements intended to exist only as literals and only as the result of lowering machine-independent specifications that cannot directly talk about specific registers. Currently they do not exist in the implementation. Register sets are not allowed to be operands to instructions to avoid state explosions when synthesizing. This restriction is currently not captured in the abstract syntax or typing rules.

**Functions and Procedures.** Functions, defined with \texttt{def} in Figure 2, are pure functions whose bodies are expressions. They produce values. They can access registers and memory, and can fail, but cannot update anything. Procedures, defined with \texttt{proc}, are on the other hand impure and their bodies are statements. They do not produce values, but they may update the machine state. They are otherwise similar, and are intended to be used to abstract out common chunks of functionality shared among multiple instructions in machine descriptions. Functions can also be used for state hiding in specifications.

Functions and procedures are second-class; they may be called only by their own name and may not be bound to variables or passed around. Furthermore, they are only allowed to handle base types: higher-order functions are explicitly not supported.

**Operations.** Operations (defined with \texttt{def op} in Figure 2) are essentially instructions, and we refer to these interchangeably. An operation takes zero or more operands and transforms the machine state as defined by one or more statements. Operands are currently defined as expressions, but are restricted as follows:
This restriction affects what the synthesizer tries to generate; a broader set of expressions may be accepted for verification or concrete execution and simply evaluated in place.

There is an important distinction between "operations" and "instructions". Operations are the units in which Cassiopea reasons about machine operations and the units in which Cassiopea generates programs and code fragments, but they do not necessarily need to be single instructions. The text output to the assembler is arbitrary and can be computed on the fly based on the operand value. On some platforms the assembler defines so-called "synthetic instructions" that are potentially multiple real instructions. This facility takes that a step further by allowing the writer of the machine description to define their own synthetics.

Other Constructs. $e[C]$ and $e[C_1, C_2]$ in Figure 1 extract a single bit and a slice, respectively, from a bitvector. The offsets are constants; a shift can be used beforehand if variable offsets are needed. The width of the slice must be constant for static typing.

Machines, Lowering, Specifications, and Programs.
A machine is the full description of a machine architecture; it includes declarations (including types, constants, registers, functions and procedures) and also instructions, shown in Figure 3. This is typically a standalone file but may be a set of files referenced via `include`.

A (single) lowering is a collection of declarations used to instantiate elements in Alewife translations, shown in Figure 3. These are placed into a module, with multiple modules per file, so that the lowerings associated with multiple related Alewife specifications can be kept together. The `import` directive enables sharing common elements in one module across multiple specifications. The modules used to lower a specification are selected using the `lower-with` declaration in Alewide.

A spec (specification) is a precondition and postcondition, which are boolean expressions, along with optional permission to destroy additional registers (the frame), shown in Figure 3. Cassiopea specifications are produced by compiling Alewide specifications. Note that a module can also contain frame declarations; these are added to any provided in the Alewide specification. A code block is permitted to destroy any register that is either explicitly listed in the frame declarations or mentioned in the postcondition, while it may read any register mentioned in the precondition and any control register. This restriction is currently not adequately captured in the semantics rules.

A program is a sequence of instruction invocations, shown in Figure 3.

Built-in Functions. Here is a partial list of the built-in functions in Cassiopea.

- `empty (int C → C reg set)` produces an empty register set of the requested bit size.
- `hex (C bit → string)` prints numbers in hexadecimal.
- `bin (C bit → string)` prints numbers in binary.
As already mentioned, bitvector constants whose size is a multiple of 4 can also be written in the form desugared in the parser and not shown in the abstract syntax. The concrete syntax is ML-style. There are also a few things the operator precedence and most of the rest of the abstract syntax. The operator precedence and most of the rest of the abstract syntax. The operator precedence and most of the rest of the abstract syntax. The operator precedence and most of the rest of the abstract syntax. The operator precedence and most of the rest of the abstract syntax.

* dec (C bit → string) prints numbers in decimal.
* lbl (C label → string) prints labels (it returns the label identifier as a string). This is for data labels attached to memory locations.
* textlabel (8 bit → string) prints branch offsets as assembler labels. This is for code labels, as described above.
* format (string → string ... → string) formats strings. The first argument is a format string; the remainder of the arguments are substituted into the format string where a dollar sign appears followed by the contents of the format string.
* bv_to_len (int C_1 → C_2 bit → C_1 bit) returns a new bitvector of size C_1 with the same value up to the ability of the new size to represent that value.
* bv_to_uint (C_1 bit → int) converts a bitvector to unsigned int.
* uint_to_bv (int C_1 → C_2 → int C_1) converts an unsigned int C_1 into a bitvector of size C_1.
* isptr (C bit → bool) tests at runtime if a bitvector value is a pointer or not.

Note that some of these functions have their own typing rules, some of which are polymorphic in bitvector size. We have not complicated the typing rules presented by including all of these as special cases.

**Concrete Syntax.** We do not describe the concrete syntax in detail here; however, it does not stray very far from the abstract syntax. The operator precedence and most of the operator spellings are taken from C but most of the rest of the concrete syntax is ML-style. There are also a few things desugared in the parser and not shown in the abstract syntax. As already mentioned, bitvector constants whose size is a multiple of 4 can also be written in the form \(0x\text{C}\). Syntax of the form \(e.\text{hex}, e.\text{bin}\), and \(e.\text{dec}\) is converted to the built-in functions \(\text{hex}, \text{bin}, \text{dec}\) respectively. These print either integers or bitvectors as strings in hexadecimal, binary, or decimal respectively. The syntax \(x.\text{lb1}\) is similarly converted to the built-in function \(\text{lb1}\). This produces the label (that is, the identifier naming the label) as a string. Further the concrete syntax supports include files via an include directive, which is useful for sharing common elements.

### 4 Cassiopea Static Typing

This section describes the Cassiopea type system.

**Environments.** The type system uses two environments: \(\Delta\) maps type alias names to the types they represent, and \(\Gamma\) maps variables to the types assigned to them. Recall from the syntax that only base types may have alias names, so alias names can be treated as base types.

**Well-Formedness.** Since types include alias names, we need to check that a proposed alias name is actually a type name. At the same time we insist that the widths of bitvectors be greater than zero. The judgment for this has the form \(\Delta \vdash_{\text{w}} \tau\), shown in Figure 4. There is an intended invariant that only well-formed types may be entered into the variable typing environment \(\Gamma\), so that types taken out of it do not need to be checked for well-formedness again.

In a typing environment comprised of \(\Delta\) mapping user-defined type names (type aliases) to types and \(\Gamma\) mapping program binders (variables) to types, we say that a type is well formed when all type names are well-formed and all indices are of type int and nonzero.

**Expressions.** Expressions produce values that have types. Because types appear explicitly in some expressions (e.g., \(1\text{et}\)), we need both environments, so the form of an expression typing judgment is \(\Delta, \Gamma \vdash e : \tau\), shown in Figure 5. This means that we conclude \(e\) has type \(\tau\). Note that the \(\cdot\text{txt}\) form is restricted to registers; it is specifically for extracting the assembly text form of a register. We have not written out a
There is no rule (either in the typing or in the semantics) that allows taking a subrange of a memory region as a new smaller region. We have not needed this for our use cases, and keeping the set of possible regions fixed simplifies a number of things.

**Statements.** Statements do not produce values. We still need both environments, though, so the form of a typing separate rule for each unary and binary operator. The types of operators are as shown in Figure 6. Note that the bitvector operators are polymorphic in bit size.

Arguably the right hand argument of the shift operators should be allowed to be a different width. There is one rule for pointer literals that covers both the expression and the value form. There is no rule (either in the typing or in the

![Type Well-Formedness](image_url)

**Figure 4.** Cassiopea type well-formedness.

![Expression Typing](image_url)

**Figure 5.** Cassiopea typing rules for expressions.
The description is well typed and provides the environment on the machine, there is no specific machine state to refer to; machine state (registers or memory), because when defining they may not use the expression forms that refer to machine state. This notionally includes the built-in function describing the built-in type aliases. (Currently there are none.)

Declarations. Declarations update the environment. The form of a typing judgment for a declaration is \( \Delta, \Gamma \vdash \text{decl} \vdash \Delta', \Gamma' \), and a judgment for a list of declarations has the same form, shown in Figure 8. This means that the declaration (or list) is well typed and produces the new environment on the right. One can think of the \( \vdash \) as the tail and head of an arrow with the element transforming the environments labeling the body.

We impose an additional syntactic restriction on declarations found in a machine description (as opposed to the additional declarations that may appear in a specification): they may not use the expression forms that refer to machine state (registers or memory), because when defining the machine, there is no specific machine state to refer to; any references need to be quantified. (That in turn is not allowed to avoid needing to send these quantifiers to the SMT solver.)

Machines. A machine is some declarations followed by some defops, so the typing rule is just sequencing, shown in Figure 9. But there is a wrinkle: the initial environment for the machine is not an input. \( \Delta_{\text{builtin}} \) is the (fixed) environment describing the built-in type aliases. (Currently there are none.) \( \Gamma_{\text{builtin}} \) is the environment describing the types of built-in variables. This notionally includes the built-in functions. (But as mentioned earlier some of them actually have their own typing rules.) The form of a typing judgment for a machine is \( \vdash \text{machine} \vdash \Delta, \Gamma \). This means that the machine description is well typed and provides the environment on
(Declaration Typing)

\[
\begin{array}{c}
\Delta, \Gamma \vdash e \triangleright \Delta, \Gamma \\
\hline
\Delta, \Gamma \vdash \text{decl} \triangleright \Delta', \Gamma' \\
\hline
\Delta, \Gamma \vdash \text{decls} \triangleright \Delta'', \Gamma''
\end{array}
\]

\[
\begin{array}{c}
\Delta \vdash \text{type } x_r : \tau_{\text{base}} \triangleright \Delta', \Gamma \\
\hline
\Delta \vdash x : \tau_{\text{base}} \triangleright \Delta', \Gamma \\
\hline
\Delta \vdash x : \tau_{\text{base}} \triangleright \Delta', \Gamma
\end{array}
\]

\[
\begin{array}{c}
\Delta \vdash \text{let } x : \tau_{\text{base}} \triangleright \Delta', \Gamma \\
\hline
\Delta \vdash x : \tau_{\text{base}} \triangleright \Delta', \Gamma
\end{array}
\]

\[
\begin{array}{c}
\Delta \vdash x : \tau_{\text{base}} \triangleright \Delta', \Gamma \\
\hline
\Delta \vdash \text{let } x : \tau_{\text{base}} \triangleright \Delta', \Gamma
\end{array}
\]

\[
\begin{array}{c}
\Delta \vdash \text{proc } x_{\text{proc}} : \tau_{\text{base}} \triangleright () \\
\hline
\Delta \vdash x_{\text{proc}} \triangleright () = S \triangleright \Delta, \Gamma''
\end{array}
\]

\[
\begin{array}{c}
\Delta \vdash \text{C reg } x \notin \Delta, \Gamma \\
\hline
\Delta \vdash \text{letstate } x : \text{C reg} \triangleright \Delta, \Gamma'
\end{array}
\]

\[
\begin{array}{c}
\Delta \vdash \text{C reg } x \notin \Delta, \Gamma \\
\hline
\Delta \vdash \text{letstate control } x : \text{C reg} \triangleright \Delta, \Gamma'
\end{array}
\]

\[
\begin{array}{c}
\Delta \vdash \text{C reg } x \notin \Delta, \Gamma \\
\hline
\Delta \vdash \text{letstate control dountgate } x : \text{C reg} \triangleright \Delta, \Gamma''
\end{array}
\]

\[
\begin{array}{c}
\Delta \vdash \text{C bit } C_1 \text{ bit } C_2 \text{ len } C_3 \text{ ref } x_{\text{mem}} \notin \Delta, \Gamma \\
\hline
\Delta \vdash \text{letstate } x_{\text{mem}} : \text{C bit } C_1 \text{ bit } C_2 \text{ len } C_3 \text{ ref} \triangleright \Delta, \Gamma''
\end{array}
\]

\[
\begin{array}{c}
\Delta \vdash \text{C bit } C_1 \text{ bit } C_2 \text{ len } C_3 \text{ ref } x_{\text{mem}} \notin \Delta, \Gamma \\
\hline
\Delta \vdash \text{letstate } x_{\text{mem}} : \text{C bit } C_1 \text{ bit } C_2 \text{ len } C_3 \text{ ref} \triangleright \Delta, \Gamma''
\end{array}
\]

\[
\begin{array}{c}
\Delta \vdash \text{defop } \triangleright \Delta', \Gamma' \\
\hline
\Delta \vdash \text{defops } \triangleright \Delta'', \Gamma''
\end{array}
\]

\[
\begin{array}{c}
\Delta \vdash \text{e } \triangleright \Delta, \Gamma \\
\hline
\Delta \vdash \text{e } \triangleright \Delta, \Gamma
\end{array}
\]

\[
\begin{array}{c}
\Delta \vdash \text{defop } \text{xop} \{ \text{txt} = e, \text{sem} = S \} \triangleright \Delta, \Gamma' \\
\hline
\Delta \vdash \text{defop } \text{xop} \{ \text{txt} = e, \text{sem} = S \} \triangleright \Delta, \Gamma''
\end{array}
\]

**Figure 8.** Cassiopea typing rules for declarations.

The right for use of other constructs that depend on the machine. (Specs and programs are only valid relative to a given machine.)

**Specifications.** For specifications we need two helper rules, shown in Figure 9: one that applies an additional list of declarations to a machine, which has the same form as the judgment on a machine; and one that says that a frame (modifies list) is well typed, which has the form \( \Delta, \Gamma \vdash \text{frames} \).

This lets us write the real rule, which has the form \( \text{machine } \vdash \text{spec} \) and means that the specification is well typed under the machine description.
5 Cassiopea Semantics

This section defines the semantics of Cassiopea.

Environment. The execution environment $\Lambda$ maps Cassiopea variables $x$ to values $v$. For labels on memory regions, each label maps to a pointer that points to the base (offset 0) of the region associated with the label. However, we take advantage of the polymorphism and dynamic typing of paper rules to also store the following in the same environment:

- $x_{func}$ (function names) map to pairs $\{\overline{x}, e\}$, which give the list of argument names and the body for functions.
- $x_{proc}$ (procedure names) map to pairs $\{\overline{x}, e, S\}$, which give the list of argument names and the body for procedures.
- $x_{op}$ (operation/instruction names) map to triples $\{\overline{x}, e, S\}$, which give the list of argument names, the expression for the text form, and the body for operations.
- $r_{txt}$ (the form for the text version of a register) maps to a value.
- The word EXTBRANCH maps to a branch state, which must be either ext or -. This reports whether, after executing a program, it branched to the external label or not.

Since identifiers are not allowed to overlap in well-typed programs, and register identities are not strings at all, and EXTBRANCH is reserved, this usage creates no conflicts.

Note that $x_{mem}$, $x_{r}$, and $x_{module}$ do not appear in $\Lambda$ as these require no translation/lookup at runtime.
(Expression Semantics)

| Rule | Description |
|------|-------------|
| \( \Lambda(x) = v \) | \( \Lambda \vdash (\rho, \sigma, e) \Downarrow r \) \( \Lambda(r.\text{txt}) = v \) \( \Lambda \vdash (\rho, \sigma, e.\text{txt}) \Downarrow v \) \( \Lambda \vdash (\rho, \sigma, e) \Downarrow r \) \text{ if } \text{txt} \notin \Lambda |
| \( \forall i, \Lambda \vdash (\rho, \sigma, e_i) \Downarrow v_i \) \( \Lambda(x_{\text{func}}) = \{x_i, e\} \) \( \Lambda[x_i \mapsto v_i] \vdash (\rho, \sigma, e) \Downarrow \hat{v} \) |
| \( \Lambda \vdash (\rho, \sigma, \text{unop } e) \Downarrow \hat{v}_2 \) \( \Lambda \vdash (\rho, \sigma, \text{binop } e_2) \Downarrow \hat{v}_3 \) \( \Lambda \vdash (\rho, \sigma, \text{if } e_2) \Downarrow \hat{v}_2 \) \( \Lambda \vdash (\rho, \sigma, \text{let } \tau_{\text{true }} = e_1 \text{ in } e_2) \Downarrow \hat{v}_2 \) |
| \( \Lambda \vdash (\rho, \sigma, e[C_i]) \Downarrow b_{C_i} \) \( \Lambda \vdash (\rho, \sigma, e[\ldots]) \Downarrow \text{fail} \) \( \Lambda \vdash (\rho, e[C_i], C_j] \Downarrow b_{C_i} \ldots b_{C_j} \) |
| \( \Lambda \vdash (\rho, \sigma, e[C_i]) \Downarrow b_{C_i} \) \( \Lambda \vdash (\rho, e[C_i], C_j] \Downarrow \text{false} \) \( \Lambda \vdash (\rho, \sigma, \text{true}) \Downarrow \hat{v}_1 \) \( \Lambda \vdash (\rho, \sigma, \text{false}) \Downarrow \hat{v}_f \) |
| \( \Lambda \vdash (\rho, \sigma, e[\ldots] \Downarrow \hat{v}_2 \) \( \Lambda \vdash (\rho, \sigma, \text{if } e \text{ then } e_1 \text{ else } e_2) \Downarrow \hat{v}_f \) |
| \( \Lambda \vdash (\rho, \sigma, \text{true}) \Downarrow \hat{v}_1 \) \( \Lambda \vdash (\rho, \sigma, \text{false}) \Downarrow \hat{v}_f \) |
| \( \Lambda \vdash (\rho, \sigma, e[C_i]) \Downarrow \hat{v}_2 \) \( \Lambda \vdash (\rho, \sigma, \text{true}) \Downarrow \hat{v}_1 \) \( \Lambda \vdash (\rho, \sigma, \text{false}) \Downarrow \hat{v}_f \) |
| \( \Lambda \vdash (\rho, \sigma, e[C_i]) \Downarrow \hat{v}_2 \) \( \Lambda \vdash (\rho, \sigma, \text{false}) \Downarrow \hat{v}_f \) |
| \( \Lambda \vdash (\rho, \sigma, \text{true}) \Downarrow \hat{v}_1 \) \( \Lambda \vdash (\rho, \sigma, \text{false}) \Downarrow \hat{v}_f \) |
| \( \Lambda \vdash (\rho, \sigma, \text{true}) \Downarrow \hat{v}_1 \) \( \Lambda \vdash (\rho, \sigma, \text{false}) \Downarrow \hat{v}_f \) |
| \( \Lambda \vdash (\rho, \sigma, \text{true}) \Downarrow \hat{v}_1 \) \( \Lambda \vdash (\rho, \sigma, \text{false}) \Downarrow \hat{v}_f \) |

Figure 10. Cassiopea semantics for expressions.
**Machine State.** In addition to the execution environment, we also need a representation of machine state. We define two stores, one for registers and one for memory. The register store ρ maps registers r to values v. The memory store σ is more complicated: it maps pairs (x_mem, C) (that is, pointer literals) to pairs (v, C), where v is the value stored at that location and C is the bit width. The bit widths of memory regions are invariant, both across the region when they are declared and also over time. They are used to check the access widths appearing in fetch and store operations. Also note that new entries cannot be created in either the register store or the memory store, as real hardware does not permit such actions. The values stored in registers and memory regions are restricted by the typing rules to bitvectors (whether constants or pointers) of the appropriate width.

Notice that stepping through the declarations does not initialize the machine state. We want to reason about executions over ranges of possible starting machine states; so instead we provide a judgment that uses the typing environment to restricts the stores to forms consistent with the declarations. This is discussed further below.

**Expressions.** We describe expressions with a large-step operational semantics, shown in Figure 10. The form of an expression semantic judgment is: \( \Lambda \vdash (\rho, \sigma, e) \Downarrow v \), which means that given the environment \( \Lambda \) and the machine state \( \rho, \sigma \), the expression \( e \) evaluates to the value \( v \). Expressions may refer to the machine state, but not modify it. Expressions can fail; in addition to the explicit failure cases seen, some of the operators and built-in functions can fail. For example, as mentioned earlier, attempting bitvector arithmetic other than addition and subtraction on pointers will fail. Furthermore, division by zero fails.

Note that we currently do not statically check (in the typing rules) that the .txt form is present for every register or that it is defined for registers on which it is used. Thus we have an explicit failure rule for when no matching declaration has been seen. We also have failure rules for bad fetch operations: if the length annotation is wrong, if the pointer is not in the machine state (this covers both unaligned accesses and out of bounds accesses), or if the value used is not a pointer. Similarly, we have failure rules for when bit indexing/slicing a pointer. We do not, conversely, need explicit failure checks or rules for the bit indexes in the bit extraction/slicing constructs as they are statically checked.

Also note that we include in the semantics the obvious failure propagation rules for when subexpressions fail. We do not show these explicitly as they are not particularly interesting or informative; however, note that the && and || logical operators short-cut left to right.

**Statements.** Unlike expressions, statements can change machine state. Thus, the form of a machine state semantics judgment (also large step) is \( \Lambda \vdash (\rho, \sigma, S) \Downarrow (\rho', \sigma', S', \xi) \), shown in Figure 11. This means that the statement \( S \) evaluates to the irreducible statement \( S' \) (which must be either skip or crash) and in the course of doing so changes the machine state from \( \rho, \sigma \) to \( \rho', \sigma' \), and produces a branching state \( \xi \), which can be either an 8-bit bitvector, the reserved value ext, or a dot (·). As with expressions, statements can fail. Explicit failure rules are shown for bad stores (corresponding to the cases for bad fetches) and for a failed assertions. We also similarly include, but do not show, the obvious failure propagation rules for cases where sub-statements, or expressions within statements, fail.

**Declarations.** The semantics for declarations have judgments of the form \( \Lambda, (\rho, \sigma) \vdash decl \Rightarrow \Lambda' \), shown in Figure 12. This means that the given declaration updates \( \Lambda \) as shown. As stated above, we do not initialize the machine state while handling declarations; this instead allows us to work with arbitrary (or universally quantified) machine states afterwards. However, because the let-binding declaration evaluates an expression, it potentially needs access to a machine state. Consequently we write the rules so they accept a machine state as input, but do not update it. In the case of machine descriptions, where there is no machine state, we pass empty environments; let declarations in machine descriptions are not allowed to reference machine state. In the case of the additional declarations that accompany a specification, we pass in the initial machine state; this allows values from the initial machine state to be globally bound so they can be referred to in the postcondition.

We give first the rules for a list of declarations, then the rules for the various declarations, then the rules for a list of operation definitions and a rule for a single operation definition. Note that several of the declarations do not update \( \Lambda \), and nothing is placed in \( \Lambda \) for memory regions. For registers, only the mapping of the identifier to its underlying register \( r \) is entered; nothing for \( r \) is inserted.

**Machines.** As with the typing rules, the semantics rule for a whole machine description integrates the initial environment and gives a judgment of the form \( \vdash machine \Rightarrow \Lambda' \), shown in Figure 13. We also include a comparable form that includes additional declarations, as it will be used below.

**Programs.** Instructions update the machine state, and we chose to represent programs as lists of instructions rather than having dummy instruction forms for skip and sequence. Consequently the form of the judgments is slightly different, and there are several of them, shown in Figure 14.

First, we can execute an individual instruction using the form \( \Lambda \vdash (\rho, \sigma, \text{inst}) \rightarrow (\rho', \sigma', \xi) \), meaning that the instruction executes and updates the machine state \( \rho, \sigma \) to \( \rho', \sigma' \), producing the branching state \( \xi \). Then, a list of instructions executes using the form \( \Lambda \vdash (\rho, \sigma, \text{insts}, \xi) \rightarrow (\rho', \sigma', \text{insts}', \xi') \), which means that the list steps to a new list and updates both the machine state and the branching state. When the instruction list runs out, these reduce to a shorter form via a judgment of the form \( \Lambda \vdash (\rho, \sigma, \text{insts}, \xi) \rightarrow (\rho', \sigma') \), which discards the instructions and branching state and produces
which means that a machine with the initial state $$\rho, \sigma$$ to the way assembly languages normally work. Noted that there are two versions of the judgment for in-

clusions of the form $$\Gamma \vdash (\Gamma, \Delta \vdash \mathit{crash} \cdot)$$.
(Declaration Semantics)

\[
\begin{align*}
\Lambda, (\rho, \sigma) &\vdash e \triangleright \Lambda' \\
\Lambda, (\rho, \sigma) &\vdash \text{decl} \triangleright \Lambda' \\
\Lambda, (\rho, \sigma) &\vdash \text{decls} \triangleright \Lambda''
\end{align*}
\]

Figure 12. Cassiopea semantics for declarations.

(Machine Semantics)

\[
\begin{align*}
\Lambda_{\text{builtin}} (\{\}, \{\}) &\vdash \text{decls} \triangleright \Lambda \\
\Lambda &\vdash \text{defops} \triangleright \Lambda' \\
\Lambda &\vdash \text{decls; defops} \triangleright \Lambda'
\end{align*}
\]

Figure 13. Cassiopea semantics for machines.

The intended behavior is that a program that fails during execution (that is, the body of one of its instructions steps to crash) enters a state where no postcondition can evaluate to true. We have decided for the moment that working this explicitly into the formalism would result in a lot of complication and obscurcation without providing any useful information.

Specifications. For specifications we need three judgments, shown in Figure 15: the first two state what the reg-modify and mem-modify clauses mean, respectively (they are properties on initial and final register and memory states), and the last one says what it means for a program to satisfy a specification. Note that the reg-modify and mem-modify rules as shown are slightly misleading, because the register and pointer list provided in the input specification is implicitly augmented with all registers and pointers mentioned in the postcondition before it gets to this point.

Machine State Validity. As discussed above, we do not initialize the machine state while processing declarations. Instead we treat the starting machine state as an input (e.g., in the final judgment about programs) or quantify it universally as in the specification judgment. This requires that we have a predicate to reject machine states that do not match the machine description. The validity judgment has the form \(\Delta, \Gamma, \Lambda \vdash \rho\), shown in Figure 16, and correspondingly for \(\sigma\) (except without \(\Lambda\)) and then for \(\rho, \sigma\) (both stores at once). This means that the given stores match the given environments.
(Program Semantics)
\begin{align*}
\Lambda(x_{op}) &= \{ [ ] , _- , S \} \quad \Lambda \vdash (\rho , \sigma , S) \Downarrow (\rho' , \sigma' , \text{skip}, \xi) \\
\Lambda \vdash (\rho , \sigma , x_{op}) \rightarrow (\rho' , \sigma' , \xi) \\
\forall i , \Lambda \vdash (\rho , \sigma , e_i) \Downarrow v_i \\
\Lambda(x_{op}) &= \{ \overline{x_i} , _- , S \} \quad \Lambda' = \Lambda[\forall i , x_i \mapsto v_i] \quad \Lambda' \vdash (\rho , \sigma , S) \Downarrow (\rho' , \sigma' , \text{skip}, \xi) \\
\Lambda \vdash (\rho , \sigma , x_{op} \overline{e_i}) \rightarrow (\rho' , \sigma' , \xi)
\end{align*}

\[ \vdash \text{machine} \triangleright \Lambda \quad \Lambda \vdash (\rho , \sigma , \text{program}, \cdot) \rightarrow^* (\rho' , \sigma' , \epsilon , \xi) \]

Figure 14. Cassiopea semantics for programs.

(Specification Semantics)
\begin{align*}
\forall i , \Lambda \vdash (\rho , \sigma , x_{reg_i}) \Downarrow r_i \quad \forall r \not\in \{ r_i \} , \rho(r) = \rho'(r) \\
\Lambda , \rho , \sigma , \rho' , \sigma' \vdash \text{reg-modify} : \overline{x_{reg}} \\
\forall i , \Lambda \vdash (\rho , \sigma , (x_{mem}, e_i)) \Downarrow (x_{mem}, C_i) \quad \forall x_{mem} , C , (x_{mem}, C) \not\in \{ (x_{mem}, C_i) \} , \sigma((x_{mem}, C)) = \sigma'((x_{mem}, C)) \\
\Lambda , \rho , \sigma , \rho' , \sigma' \vdash \text{mem-modify} : (x_{mem}, e_i) \\
\Lambda , \rho , \sigma , \rho' , \sigma' \vdash \text{frame} \\
\Lambda , \rho , \sigma , \rho' , \sigma' \vdash \text{frames} \\
\vdash \text{machine} , \text{decls} \triangleright \Delta , \Gamma \\
\vdash \text{machine} \triangleright \Lambda \\
\forall \rho , \sigma , (\Delta , \Gamma , \Lambda \vdash \rho , \sigma) \implies \\
(\forall (x_{mem}, C_1) \text{ bit} C_2 \text{ len} C_3 \text{ ref} \implies \\
(\forall i \in \{ 0 , C_1 / 8 , \ldots , (C_1 - 1) * C_1 / 8 \} , \exists v , \sigma(x_{mem}, i) = (v , C_i) \land \Delta , \Gamma \vdash \rho : C_1 \text{ bit}) \\
(\forall i \not\in \{ 0 , C_1 / 8 , \ldots , (C_1 - 1) * C_1 / 8 \} , \Delta \vdash (\rho , \sigma , (x_{mem}, i)) \Downarrow \text{fail}) \\
\Delta , \Gamma \vdash \sigma
\]

Figure 15. Cassiopea semantics for specifications.

(Machine State Validity)
\begin{align*}
(\forall x , \Delta , \Gamma \vdash x : C \text{ reg} \land \Lambda(x) = r) & \iff (\exists v , \rho(r) = v \land \Delta , \Gamma \vdash v : C \text{ bit}) \\
\Delta , \Gamma , \Lambda \vdash \rho \\
\forall x_{mem} , \Delta , \Gamma \vdash x_{mem} : C_1 \text{ bit} C_2 \text{ len} C_3 \text{ ref} \iff \\
(\forall i \in \{ 0 , C_1 / 8 , \ldots , (C_1 - 1) * C_1 / 8 \} , \exists v , \sigma(x_{mem}, i) = (v , C_i) \land \Delta , \Gamma \vdash v : C_1 \text{ bit}) \land \\
(\forall i \not\in \{ 0 , C_1 / 8 , \ldots , (C_1 - 1) * C_1 / 8 \} , \Delta \vdash (\rho , \sigma , (x_{mem}, i)) \Downarrow \text{fail}) \\
\Delta , \Gamma \vdash \sigma
\end{align*}

\[ \Delta , \Gamma , \Lambda \vdash \rho \quad \Delta , \Gamma \vdash \sigma \]

Figure 16. Cassiopea machine state validity.
We use this with the typing environments that come from both the machine description and the additional declarations arising from a specification. In the case of registers we need access to $\Lambda$ to handle the names of registers. We do not use the $\Lambda$ generated from the additional declarations in a specification; this avoids circularity. This is acceptable, because specifications are not allowed to define new registers. For memory regions we need to enumerate the valid offsets for the region (note the literal 8 that hardwires 8-bit bytes) and check the cell width.

**Branching.** To handle branching, we allow statements to produce a branching state, which indicates the number of instructions to skip over. Normally this is $\cdot$, which means none and has no effect; however, when an instruction body produces something else we use it to branch. A nonzero bitvector results in skipping the indicated number of instructions; the out-of-band additional value $\text{ext}$ causes a branch to the external label. The magic number used to select the external label appears only in one of the statement rules; beyond that point we use $\text{ext}$ explicitly.

The program rule in Figure 15 inserts the branch state produced by the program into $\Lambda$, where it provides a value for the branch to predicate found in the postcondition. This allows specifications to enforce the external branching behavior.

### 6 Alewife Overview

This section describes Alewife, our specification language for writing abstracted machine-independent specifications of low-level code.

Alewife specifications are abstractions of machine-level Cassiopea specifications; we say that Cassiopea constructs are *lifted* into Alewife and Alewife constructs are *lowered* into Cassiopea. Alewife is only for specifications, so there are no statements, no updates, and no notion of instructions or programs. We refer to the single synthesis problem in one Alewife specification as a *block*.

**Notation.** We use the following metavariables:

- $x, y, z$: Program variables (binders)
- $r$: Registers (abstract)
- $C$: Integer constants (written in decimal)
- $\text{0bC}$: Bitvector constants (written in binary)
- $N$: Symbolic integer constants
- $\tau$: Types
- $v$: Values
- $e$: Expressions
- $i, j$: Rule-level integers

(Other constructions are referred to with longer names.)

As noted previously, Alewife types and expressions should be considered distinct from Cassiopea ones (even where they correspond directly). We use the same letters in the hopes that this will cause less confusion (even in the definition of the translation) than picking an entirely different set of letters for Alewife.

**Identifiers and Variables.** In Alewife there are five syntactic categories of identifiers: As in Cassiopea, $x_{\text{mem}}$ name memory regions, $x_{\text{func}}$ name functions, and $x_i$ are type aliases. $x_{\text{module}}$ name Cassiopea lowering modules, which are used to instantiate the abstract elements and conduct Alewife–Cassiopea translation for synthesis. Other $x$ are ordinary variables that range over other things, and may be presumed to not range over the above reserved categories. All variables are immutable, in the sense that their values do not change once bound.

**Symbolic Constants.** In Alewife symbolic constants $N$ are permitted to occur in some places where only integer constants are allowed in the corresponding Cassiopea constructions. In particular, the bit sizes associated with types (and the lengths of memory regions, which are functionally similar) may be given as symbolic values $x$ instead of integer constants. These must be bound to integer constants either directly in the Alewife spec, in the Cassiopea lowering, or by the Cassiopea machine description. This allows the concrete sizes of bitvectors to vary depending on the machine architecture.

**Types.** As in Cassiopea, Alewife types are divided syntactically into base types and others, shown in Figure 17. The chief difference from Cassiopea is that bit widths (and the lengths of memory regions) can be symbolic constants.
This functions as a form of import, and allows an Alewife
require it is possible to
do not currently define or implement such a check. Note that
machine description or Cassiopea lowerings. However, we
file to be checked on its own separately from any particular
cription. In this case, the type is given, but not the value.
second form declares elements in the ordinary way, while
argument of fetch can be a symbolic size.
most expressions, shown in Figure 17. Note that the width
spond directly to the values in Cassiopea as do operators and
progression of values through machine registers, only before

distinguished from plain bitvectors (Alewife Symbolic Constants)
\[ N := C | x \]

(Alewife Types)
\[ \tau := \tau_{base} | \tau_{mem} | \tau_{func} \]
\[ \tau_{base} := \text{int} | \text{bool} | x_r \]
\[ \tau_{reg} := N \text{ reg} | N \text{ label} \]
\[ \tau_{mem} := N_1 \text{ bit} N_2 \text{ len} N_3 \text{ ref} \]
\[ \tau_{func} := \tau_{base} \rightarrow \tau_{base} \]

(Alewife Values)
\[ v := \text{true} | \text{false} | C | \text{0b} C | (x_{mem}, C) \]
\[ | \text{fail} \]

(Alewife Operators)
\[ \text{unop := } - | \text{b-} | \neg | \text{bnot} \]
\[ \text{binop := } = | \neq | + | - | * | / | < | \leq | > | \geq \]
\[ | \& \& | || | @ \]
\[ | \gg | \ggg | \ll | \land | \lor | \lnot | \lnot \lnot | \bior | \bxor \]
\[ b+ | b- | \text{b+} | \text{b/} \]
\[ b< | b<= | b> | b>= \]
\[ \text{bs}< | \text{bs<=} | \text{bs>} | \text{bs>=} \]
\[ \cup | \cap | \subseteq | \setminus \]

(Alewife Expressions)
\[ e := v | x \]
\[ | x_{func} (\overline{\tau}) \]
\[ | \text{unop } e \]
\[ | e_1 \text{ binop } e_2 \]
\[ | e[C] | e[C_1, C_2] \]
\[ | \text{let } x : \tau_{base} = e_1 \text{ in } e_2 \]
\[ | \text{if } e_1 \text{ then } e_2 \text{ else } e_3 \]
\[ | (x_{mem}, e) \]
\[ | \text{\textbackslash } e | \text{fetch}(e, N) \]
\[ | \text{branchto} \]
\[ | \{x_1, \ldots, x_k\} \]
\[ | \| e \| | e_1 \in e_2 \]

However, an additional difference is that pointers (ptr) are
distinguished from plain bitvectors (vec). This is reasonably
possible in Alewife, because it need not reason about the
progression of values through machine registers, only before
and after states. Strings and unit are also absent, as they are
not needed for specifications.

Values and Expressions. The values in Alewife cor-
respond directly to the values in Cassiopea as do operators and
most expressions, shown in Figure 17. Note that the width
argument of fetch can be a symbolic size.

Declarations and Frames. Alewife declarations come in
two forms: require and provide, shown in Figure 18. The
second form declares elements in the ordinary way, while
the first form declares an element that must be provided
by the Cassiopea lowerings or the Cassiopea machine de-
scription. In this case, the type is given, but not the value.
This functions as a form of import, and allows an Alewife
file to be checked on its own separately from any particular
machine description or Cassiopea lowerings. However, we
do not currently define or implement such a check. Note that
it is possible to require functions that implicitly depend
on machine state or that depend on machine state on some
machines and not others. Such functions can also depend on
constants or other elements that are not visible in the Alewife
specification at all. The lower-with declarations specify all
lowering modules that are used to compile this Alewife spec-
ification into a Cassiopea specification. The module name
\( x_{\text{module}} \) is used to look up the Cassiopea lowering module
to apply. The region declarations declare memory regions,
like the memory-typed letstate declarations in Cassiopea.
(These are implicitly always provide, because, for memory
regions, the corresponding require declaration would be
entirely equivalent, requiring duplication in the Cassiopea
lowering.) Note that the parameters of the region can be
symbolic constants if abstraction is needed.

Frame declarations in Alewife, annotated with reg-modify and mem-modify, are exactly the same as in
Cassiopea. Because Alewife files are machine-independent,
the registers mentioned must be abstract and concretized
via the Cassiopea lowerings.

Block-lets. While Alewife expressions include let-
bindings, the scope of those let-bindings is conventional:
it lasts until the end of the expression. To refer to values taken from the initial state (that is, the machine state of which the precondition must be true), we need a way to bind these values so their scope extends to the postcondition. The block-lets serve this purpose in Alewife, shown in Figure 18, much like the additional declarations seen in Cassiopea specs can. These are found within a block (because a block corresponds to a synthesis problem, it is meaningful to associate before and after machine states with it), and the scope is the entire block.

Specifications. A full specification starts with a preamble of declarations, shown in Figure 18. It also includes block-lets and the pre- and post-conditions for the block. Common declarations can be shared with include.

7 Alewife Typing and Semantics

We do not provide (or implement) a full typechecking pass for Alewife. Instead, when we lower to Cassiopea, we allow the Cassiopea typechecker to reject invalid results, which might be caused by invalid Alewife input or by bad/mismatched Cassiopea lowering definitions. The rules provided here are for doing scans over the declarations sufficient to make the translation to Cassiopea work and no more.

Environments. We retain the Cassiopea typing environments, $\Delta, \Gamma$. We add an additional environment $\Sigma$, which maps identifiers to integer constants. This is a projection of the Cassiopea execution environment $\Lambda$: it holds mappings only for variables defined as integer constants and excludes everything else. We include a separate set of rules for extracting these integer constants without doing a full Cassiopea execution. (Among other things, this avoids involving machine state or the machine state stores.)

Translation. The translation (lowering) from Alewife to Cassiopea, defined in the next section, appears cross-recursively in the rules in this section. Because $\Delta, \Gamma$ are Cassiopea environments, they map identifiers to Cassiopea types, not Alewife ones. This means Alewife types must be lowered on the fly to update them correctly.

Integer Constant Extraction. The integer constant extraction rules do a simple pass over Cassiopea declarations to extract the variables defined as integer constants, shown in Figure 19. These populate a substitution environment $\Sigma$ that we use for lowering Alewife types containing symbolic constants. These rules are judgments of the form $\Sigma, decls \vdash e$ or $\Sigma, decls \vdash \Sigma'$, plus one of the form $\Sigma, decls \vdash \Sigma', \Sigma$, shown in Figure 20. These mean that the declaration or declarations update the type environment (and integer constant environment) as shown. Note that there is a special-case rule for provide value for when the value is an integer constant; this enters the constant into $\Sigma$. The integer constants are in turn used when lowering the types of memory regions, which can be seen in the last two rules.

Block-lets. The rules for block-lets are effectively the same as the rules for declarations, shown in Figure 21. The ways in which block-lets are special mostly do not apply here. Note however that even though we pass through $\Sigma$ (for consistency of the form of the rules) there is no rule
for loading integer constants into $\Sigma$ from block-lets. Integer constants used in types and defined in the Alewife specification should be defined with $\text{provide value}$; block-lets are intended to provide access to machine state.

**Specifications.** The rule for the semantics of an entire specification is large and complex. The conclusion is that a given machine, lowering module, and Alewife specification produce a final translation output $\Omega$. The rules work by nondeterministically taking fixpoints over all the material included. $\text{decls}$ is the combination of all declarations found both in the initial specification and all the included lowering modules, and $\text{frames}$ is the combination of all frame information (part of the declarations in Alewife; separated in Cassiopea). Similarly, the final set of environments $\Gamma, \Delta, \Sigma$ represent fixpoints produced by processing all the declarations.

In Figure 22, the first premise expands the Alewife specification as we will need to work with the components. The next two premises generate initial environments: the Cassiopea typing environments induced by the machine description, and its integer constants, and then we require that these are included in the final environments. In the fifth and sixth premises, we then require that the result of processing the declarations from the specification appears in the final environments, and that the translation of these to Cassiopea is included in the final declarations and frame rules. Then for every lowering module requested by the specification, we require that it be provided in the input modules list and that its components appear in the final declarations and frame rules. This is followed by two more rules to ensure that these results are represented in the final environments. Later, we include the block-let material in the final environments, include its lowered form in the final declaration list (block-lets lower to declarations), bind the lowerings of the pre- and postconditions, and define the output.

The fixpoint-based evaluation strategy for declarations is required, because the Alewife declarations rely on the Cassiopea lowering file (most notably for resolving symbolic constants), but the Cassiopea lowering file is in turn also specifically allowed to refer to objects declared by the Alewife specification, such as memory regions. In the implementation this circularity is resolved by lifting both the Cassiopea and Alewife declarations (and block-lets) into a common representation and topologically sorting them based on identifier references. (Genuinely circular references among identifiers are prohibited.) From this point, they can be handled in order in a more conventional way.

**Complete Output.** Note that the output includes the declarations from the Cassiopea lowering modules (each $\text{decls}_{\text{lower}}$). Apart from symbolic constants, we do not substitute the definitions of the lowering elements, as that would greatly complicate things, especially with functions; instead we include the definitions and let the translation refer to them. In fact, because of the declaration ordering issues, in the implementation the lowering declarations and translated Alewife declarations can be arbitrarily interleaved in the output.

Note furthermore that it would not be sufficient to include only the lowering declarations explicitly imported with $\text{require}$ declarations, as those may refer freely to other things declared in the lowering module that the Alewife specification itself may have no cognizance of whatsoever.
(Alewife Declaration Typing)

\[
\begin{align*}
\Delta, \Gamma, \Sigma \vdash \text{decl} & \triangleright \Delta', \Gamma', \Sigma' \\
\Delta', \Gamma', \Sigma \vdash \text{decls} & \triangleright \Delta'', \Gamma'', \Sigma''
\end{align*}
\]

\[
\begin{align*}
\Delta \vdash \mathcal{A} \text{C} \left[ t_{\text{base}} \right] = \tau & \quad \Gamma(x) = \tau \\
\Delta, \Gamma, \Sigma \vdash \text{require type} x : t_{\text{base}} & \triangleright \Delta, \Gamma, \Sigma
\end{align*}
\]

\[
\begin{align*}
\Delta, \Gamma, \Sigma \vdash \mathcal{A} \text{C} \left[ \tau_{\text{func}} \right] = \tau & \quad \Gamma(x_{\text{func}}) = \tau \\
\Delta, \Gamma, \Sigma \vdash \text{require func} x_{\text{func}} : \tau_{\text{func}} & \triangleright \Delta, \Gamma, \Sigma
\end{align*}
\]

\[
\begin{align*}
\Delta, \Gamma, \Sigma \vdash \mathcal{A} \text{C} \left[ r \right] = \tau' & \quad \Delta \vdash \tau' = \Delta \left[ x \mapsto r' \right] \\
\Delta, \Gamma, \Sigma \vdash \text{provide type} x : \tau & \triangleright \Delta, \Gamma, \Sigma
\end{align*}
\]

\[
\begin{align*}
\Delta, \Gamma, \Sigma \vdash \mathcal{A} \text{C} \left[ t_{\text{base}} \right] = \tau & \quad \Delta \vdash \tau \quad e \neq C \\
\Delta, \Gamma, \Sigma \vdash \mathcal{A} \text{C} \left[ e \right] = \tau' & \quad \Gamma = \Gamma \left[ x \mapsto \tau' \right] \\
\Delta, \Gamma, \Sigma \vdash \mathcal{A} \text{C} \left[ e \right] = \tau' & \quad \Gamma = \Gamma \left[ x_{\text{func}} \mapsto (x_{i} : \tau_{i} \mapsto \tau) \right]
\end{align*}
\]

\[
\begin{align*}
\Delta, \Gamma, \Sigma \vdash \text{region} x_{\text{mem}} : N_{1} \text{bit } N_{2} \text{ len } N_{3} \text{ ref} & \triangleright \Delta, \Gamma, \Sigma \\
\Delta, \Gamma, \Sigma \vdash \mathcal{A} \text{C} \left[ N_{1} \text{ bit } N_{2} \text{ len } N_{3} \text{ ref} \right] & = C_{1} \text{ bit } C_{2} \text{ len } C_{3} \text{ ref} \quad \Delta \vdash \text{label} C_{3} \text{ ref} \\
\Delta, \Gamma, \Sigma \vdash \mathcal{A} \text{C} \left[ \text{C}_3 \text{ label} \right] & = \text{C}_3 \text{ label} \\
\Delta, \Gamma, \Sigma \vdash \text{region} x_{\text{mem}} : N_{1} \text{ bit } N_{2} \text{ len } N_{3} \text{ ref with } x > \Delta, \Gamma, \Sigma \\
\Delta, \Gamma, \Sigma \vdash \text{lower-with} x_{\text{module}} & \triangleright \Delta, \Gamma, \Sigma \\
\Delta, \Gamma, \Sigma \vdash \mathcal{A} \text{C} \left[ \text{reg-modify} : x_{i} \right] & = \text{reg-modify} : x_{i} \\
\Delta, \Gamma \vdash \text{reg-modify} : x_{i} & \triangleright \Delta, \Gamma, \Sigma \\
\Delta, \Gamma, \Sigma \vdash \mathcal{A} \text{C} \left[ \text{mem-modify} : (x_{\text{mem}}, e_{i}) \right] & = \text{mem-modify} : (x_{\text{mem}}, e_{i}) \\
\Delta, \Gamma, \Sigma \vdash \text{mem-modify} : (x_{\text{mem}}, e_{i}) & \triangleright \Delta, \Gamma, \Sigma
\end{align*}
\]

Figure 20. Alewife typing rules for declaration.

8 Lowering Alewife

The semantics of an Alewife specification depend on material taken from a Cassiopea mapping and machine description. This does not preclude defining a semantics for Alewife in terms of that material or even some abstracted concept of what any such Cassiopea material might be. However, doing so is complicated (as can be seen from the material in the previous section, which does not even attempt to handle expression evaluation) and not necessarily rewarding or illuminating.

So instead, we write only enough typing rules to prepare material for writing a translation (lowering) to Cassiopea, and then apply the Cassiopea typing (and, implicitly, semantics) to the lowered material. That material goes into the Cassiopea typing environments \( \Delta, \Gamma \), and as discussed in the previous section, we also maintain an additional environment \( \Sigma \) of integer constants used for substituting symbolic constants in types.

This section defines the translation \( \mathcal{A} \text{C} \left[ a \right] \) defines the Cassiopea lowering of an Alewife element \( a \). We make the
translation polymorphic over the various kinds of element; that is, \( \mathcal{AC}[e] \) is the translation of a type (shown in Figure 23), \( \mathcal{AC}[a] \) is the translation of an expression, etc. Some of the translation rules rely on the environments; these are written \( \Delta, \Gamma, \Sigma \vdash \mathcal{AC}[a] \) (shown in Figure 24).

Some of the translation rules produce \( \bot \). If these are reached, the translation fails; this can happen if the Alewife spec was malformed and, potentially, if the mapping module failed to declare elements that were expected of it or declared them in an incompatible or inconsistent way. The rules in the previous section exclude some of these cases, but we are not (yet) prepared to argue that they rule out all translation-time failures.

Notice that the translations for require declarations are empty, because the declarations from the mapping module are output along with the translated Alewife specification.
First, we presented a machine modeling language named Alewife that allows stating abstract specifications for blocks of assembly code, such that these abstract specifications can be used used to describe the semantics of many different processor ISAs at the assembly language level. Then, we presented a specification language named Alewife – Cassiopea translation.
be lowered to concrete specifications and used for synthesis and verification against Cassiopea machine descriptions.

We note that this is work in progress, and does not yet present a final or complete view of either the Aquarium system or the languages presented.