Study on the Impact of Lead Sidewall Solder Coverage and Corner Lead Size on Joint Reliability

Jefferson Talledo

1STMicroelectronics, Inc., Calamba City, 4027, Laguna, Philippines.

Author’s contribution

The sole author designed, analysed, interpreted and prepared the manuscript.

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ABSTRACT

Solder joint reliability is very important to ensure that an integrated circuit (IC) semiconductor package is functional within its intended life span as the solder joint establishes electrical connection between the IC and the printed circuit board (PCB). Solder fatigue failure or crack under thermal cycling is one of the common problems with board-mounted packages. There are several factors or package characteristics that have impact on solder fatigue life like package size and material properties of the package components. This paper presents a thermo-mechanical modeling of a leadframe-based semiconductor package to study the impact of lead sidewall solder coverage and corner lead size on the solder joint reliability. Finite element analysis (FEA) technique was used to calculate the solder life considering 50% and 100% package lead sidewall solder coverage as well as smaller and larger critical corner leads of the package. The results of the analysis showed that higher lead sidewall solder coverage and larger lead could significantly increase solder life. Therefore, ensuring lead sidewall solder wettability to have higher solder coverage is beneficial. The study also reveals that packages with side wettable flanks are not only enabling high speed automated optical inspection required for the automotive industry, but they are also providing improved solder joint reliability.

Keywords: Lead sidewall wetting; corner lead; solder joint reliability; thermal cycling; finite element modeling; wettable flank.
1. INTRODUCTION

A semiconductor package is usually mounted to the PCB (printed circuit board) using solder material to establish electrical and mechanical connection. Board-level solder joint reliability is very important especially for critical applications. The amount of solder or fillet on the lead sidewall or the solder coverage after reflow could vary as illustrated in Fig. 1. In automotive applications requiring higher lead count solutions or devices utilized in safety or mission critical applications, the need for consistent fillet formation, detectable using high speed automated optical inspection is now the automotive industry’s stated requirement. This led to the development of leadframe packages with side wettable flanks [1]. The wettable flank process was developed to resolve the issue of side lead wetting of leadless packaging for automotive and other commercial component manufacturers. This provides a visual indicator of solderability and lowers the inspection time [2].

For a board-mounted semiconductor package, the common failure is solder joint crack after thermal cycling as shown in Fig. 2. Solder joint crack could not be avoided after a certain number of thermal cycles, but it should not be an issue if the required number of cycles is achieved before the solder joint connection fails.

![Fig. 1. Schematic of a semiconductor package with different lead sidewall solder coverage](image1)

![Fig. 2. Solder joint crack after certain number of thermal cycles](image2)
Solder joint reliability in bottom terminated component depends on both the board properties as well as component characteristics such as the die size and mold compound especially to its coefficient of thermal expansion (CTE) as shown in Quad Flat No-Lead (QFN) packages. Thermal cycle profile also has an influence on the board level solder joint reliability [3]. While some believe that voids will act as stress concentrators, reducing the solder joint fatigue life, voids located in the bulk of the solder do not affect thermo-mechanical fatigue life of the solder joint [4]. Solutions to improve solder joint reliability include the optimization of PCB design with cavity and compliant layer to make it less rigid [5], use of smaller package size, smaller die size, bigger pad size, thinner PCB, higher mold compound CTE, higher solder standoff, and extra soldering at the center pad to help enhance the fatigue life [6].

In ball grid array (BGA) packages, factors such as BGA array, underfill choices and BGA depopulation can impact the board level reliability. Addition of redundant or dummy BGAs or minimizing BGA depopulation area can significantly improve the solder joint reliability [7]. Solder joint microstructure can also have influence on the thermal cycling reliability of BGA packages [8]. The evaluation on the use of joint reinforced solder paste (JRP) has shown that the epoxy resin component of the developed JRP material can improve the solder joint reliability [9]. Another solution to improve solder joint reliability during thermal cycling is to use the corner lead solder joint as mechanical reinforcement only (no electrical connection to the PCB) as shown in Fig. 3. So even if the corner solder joint cracks completely, the electrical connection needed by the device to function is still working.

With the automotive industry’s requirement to have consistent fillet formation being addressed using packages with side wettable flanks, it is also important to study its impact to the solder joint reliability. From the several factors or package characteristics with impact on solder fatigue life, the current study focuses on the lead sidewall coverage or fillet and corner lead size for a specific multi-row QFN package that has active corner leads. The goal of this study is to analyze the impact of the solder coverage (% of lead side wall height) as well as the corner lead size on solder joint life of the QFN package considered.

2. SOLDER JOINT RELIABILITY MODELING

Several studies on board-level solder joint reliability uses finite element analysis (FEA) technique [3, 5-6, 10, 12-16]. This computer simulation has become popular with solder joint reliability modeling because it enables faster evaluation of design options before the actual semiconductor package is built. It is also very useful in narrowing down available package design choices so that only those with expected better solder joint reliability would be built. The prediction of solder life is based on life prediction equation developed from actual experiments as well as the solder constitutive model for a certain solder material used.

![Fig. 3. Bottom view of the package (multi-row QFN) showing the corner lead](image)
Constitutive models describe the material responses to various loading conditions and provide the stress–strain relationship of the material. For solder, there are different constitutive models commonly used in the microelectronics industry. One previous study [10] implemented four different models including elastic-plastic (EP), elastic-creep (Creep), elastic-plastic-creep (EPC) and viscoplastic Anand’s (Anand) models in modeling and simulation to investigate solder constitutive model effect on solder fatigue life and stress-strain response. Based on fatigue life prediction, it was shown that Creep, EPC and Anand models are suitable for thermal cycling simulations.

However, for SAC solders (e.g. SAC 305, SAC405, and SAC387), the hyperbolic sine creep equation is commonly used to model the solder’s temperature and time-dependent creep behavior. It is defined as [10,11]:

\[
\dot{\varepsilon}_c = C_1 \frac{G}{T} \left[ \sinh \left( \frac{\sigma}{G} \right) \right]^n \exp \left[ -\frac{C_4}{kT} \right]
\] (1)

When using ANSYS FEA software in doing the analysis, the creep strain rate is simplified and rewritten as:

\[
\dot{\varepsilon}_c = C_1 \left[ \sinh \left( C_2 \sigma \right) \right] G \exp \left[ -\frac{C_4}{kT} \right]
\] (2)

Table 1 gives the input for ANSYS hyperbolic sine creep model used in this study.

The fatigue life prediction could either be based on strain or strain energy. However, Che et al. [12] showed that the energy-based fatigue model resulted in accurate and reasonable fatigue life prediction compared to strain-based fatigue model. And in order to reduce the stress concentration effect, the volume-averaging method is typically used in parameter extraction from simulation results for solder fatigue life prediction [13]:

\[
W_{cr} = \frac{\sum (W_{cri} V_i)}{\sum V_i}
\] (3)

Once the accumulated strain energy density per cycle \(W_{cr}\) is obtained from the model, the characteristic life, \(N_f\) (63.2% accumulative failure), can be calculated by the following correlation for SnAgCu(SAC) solders [14]:

\[
N_f = 345 W_{cr}^{(1.02)}
\] (4)

The fatigue correlation above, which is also known as Schubert’s correlation model, has been found to have good prediction accuracy for BGA (ball grid array) laminate-based packages but not for leadframe-based packages like QFN (quad flat no lead). Another study [15] showed that a different fatigue correlation model would work well with solder fatigue life prediction for QFNs:

\[
N_f = 741.37 W_{cr}^{(-0.3902)}
\] (5)

In this study, a finite element modeling was conducted to analyze the impact of lead sidewall solder coverage and the corner lead size on solder joint reliability. Fig. 4. shows the finite element model used for the solder joint reliability modeling with the solder coverage and corner lead size varied. A quarter symmetry model was used to reduce the computation time as the actual QFN package analyzed was also symmetric in both X and Y axis. Details of the solder fillet around the lead sidewall were included. Table 2. summarizes the package versions being considered in the solder joint reliability modeling study. Three thermal cycles were simulated since this is the number of cycles in which the accumulated strain energy density or plastic work accumulation is already stable, and the change becomes minimal [16].

After the three thermal cycles, the average accumulated strain energy density or plastic work accumulation per cycle was extracted from the results and solder fatigue life was calculated using equation (5). The solder life calculation results for all the package versions were then normalized against the solder life of package Version 1 (smaller corner lead, with 50% lead sidewall solder coverage).

### Table 1. Constants for Sn-3.8Ag-0.7Cu Solder [11]

| \(C_1\) | \(C_2\) | \(C_3\) | \(C_4\) |
|---|---|---|---|
| 3.2e4 | 0.037 | 5.1 | 6524.7 |

65
3. RESULTS AND DISCUSSION

The creep strain energy density result of the critical solder joint after three thermal cycles is shown in Fig. 5. The critical solder joint is the active joint that is expected to fail earlier than the other electrically connected joints. The volume-averaged technique was implemented to get the accumulated creep strain energy density per cycle for the solder material interface layer. Based on the results (Fig. 5), the critical solder joint turns out to be the active corner joint.

From the accumulated strain energy density per cycle obtained and the characteristic life calculation using the fatigue life prediction equation established for QFN solder joint [15], normalized results are now shown in Fig. 6. Results indicate that higher lead sidewall solder coverage results in higher solder joint life. Increasing the corner lead size also increases the solder life significantly. This implies that to increase the solder joint reliability, it is important to ensure higher lead sidewall solder coverage and increase the lead size if still possible. It can be observed that increasing the lead sidewall solder coverage from 50% to 100% results in about 30% to 50% increase in solder life considering both the smaller and the larger corner leads. It appears that having higher solder coverage provides more resistance against solder crack.

The results of the current study agree with the actual results of a related study [6] on QFN-8x88 revealing that the package with solder fillet has 227 longer cycles than the case without solder fillet. The same study also showed that when both the lead and land length are increased, the fatigue life is enhanced, mainly due to increase in lead length. The crack initiated takes longer time to propagate through the failure interface. The current results are further supported by analysis and experimentation [17] indicating that increased fatigue life under power cycling can be attained by fabricating solder joints with large fillets and low standoff heights. If fillets are formed, this will be a benefit for solder joint reliability [18].

| Package Version | Corner Lead Size | Sidewall Solder Coverage |
|-----------------|------------------|--------------------------|
| Version 1       | Smaller          | 50%                      |
| Version 2       | Smaller          | 100%                     |
| Version 3       | Larger           | 50%                      |
| Version 4       | Larger           | 100%                     |
4. CONCLUSION

The study shows that higher solder life is achieved when using higher sidewall solder coverage. Larger lead also provides increase in solder life. The increase in lead sidewall solder coverage and lead size resulting in larger solder connection increases the resistance of the package against solder crack failure. Results also reveal that packages with side wettable flanks, which allow higher lead sidewall solder coverage, would be beneficial not only in enabling high speed automated optical inspection but also in providing improved solder joint reliability. It is also demonstrated that board-level solder reliability modeling using finite element analysis (FEA) is very useful in quickly analyzing different factors or package characteristics that affect solder joint reliability performance assessment. Future solder joint reliability study on actual multi-row QFN package built with different sidewall solder coverage and lead size could be further explored.

DISCLAIMER

The products used for this research are commonly and predominantly use products in our
area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

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COMPETING INTERESTS

Author has declared that no competing interests exist.

REFERENCES

1. Mangrum MA. Side Wettable Flanks for Leadless Automotive Packaging. Amkor Technology, Inc; 2020.
2. Natronix/SPEL. QFN Wettable Flank Packaging. Available: http://www.natronix.net/
3. Serebreni M, McCluskey P, Ferris T, et al. Modeling the influence of mold compound and temperature profile on board level reliability of single die qfn packages. 19th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE); 2018.
4. Ribas M, Sarkar S. Effect of Voids on Thermo-mechanical Reliability of Solder Joints. Proceedings of SMTA International; 2017.
5. Xu L, Zhou S, Lu J. Optimization of PCB board to improve thermomechanical reliability of lead-free ball joint. IEEE 19th International Conference on Electronic Packaging Technology; 2018.
6. Tee TY, Ng HS, Yap D, Zhong Z. Comprehensive board-level solder joint reliability modeling and testing of QFN and PowerQFN packages. Microelectronics Reliability; 2003.
7. Dhandapani K, Zheng J, Roggemann B, Hsu M. Improving solder joint reliability for PoP packages in current mobile ecosystem. IEEE 68th Electronic Components and Technology Conference; 2018.
8. Sun X, Li W, Chen M. Influence of the BGA solder joint microstructure on the thermal cycling reliability. 20th International Conference on Electronic Packaging Technology (ICEPT); 2019.
9. Yamaguchi A, Fukuhara Y, Behr A, Hino H, et al. The Influence of Resin Coverage on Reliability for Solder Joints Formed by One-Pass Reflow Using Resin Reinforced Low Temperature Solder Paste. IEEE 67th Electronic Components and Technology Conference; 2017.
10. Che FX, Pang HLJ, Zhu WH, Sun W, Sun AYS. Modeling constitutive model effect on reliability of lead-free solder joints. IEEE 7th International Conference on Electronics Packaging Technology; 2006.
11. Pang HLJ, Xiong BS, Low TH. Creep and fatigue characterization of lead-free 95.5sn-3.8ag-0.7cu solder. Proc 54th Electronic Components and Technology Conference; 2004.
12. Che FX, Pang HLJ. Thermal Fatigue Reliability Analysis for PBGA with Sn-3.8Ag-0.7Cu Solder Joints. Proc 6th Electronic Packaging Technology Conference; 2004.
13. Che FX, Pang HLJ, Xiong BS, Xu LH, Low TH. Lead-Free Solder Joint Reliability Characterization for PBGA, PQFP and TSSOP Assemblies. Proc 55th Electronic Components and Technology Conference; 2005.
14. Schubert A, Dudek R, Auerswald E, Gollhardt A, Michel B, Reichl H. Fatigue Life Models for SnAgCu and SnPb Solder Joints Evaluated by Experiments and Simulation. Proc 53rd Electronic Components and Technology Conference; 2003.
15. Sun W, Zhu WH, et al. Study on the board-level smt assembly and solder joint reliability of different qfn packages. Proc 8th Int. Conf. on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems, Euro Sim E; 2007.
16. Fan X, Pei M, Bhatti PK. Effect of finite element modeling techniques on solder joint fatigue life prediction of flip-chip bga packages. Electronic Components and Technology Conference; 2006.
17. Charles HK Jr, Clatterbaugh GV. Solder joint reliability — design implications from finite element modeling and experimental testing. ASME Journal of Electronic Packaging; 1990.

18. Recommendations for printed circuit board assembly of infineon qfn packages. Infineon Technologies AG; 2012.

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