Planar Josephson Junctions Templated by Nanowire Shadowing

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More and more materials, with a growing variety of properties, are built into electronic devices. This is motivated both by increased device performance and by the studies of materials themselves. An important type of device is a Josephson junction based on the proximity effect between a quantum material and a superconductor, useful for fundamental research as well as for quantum and other technologies. When both junction contacts are placed on the same surface, such as a two-dimensional material, the junction is called “planar”. One outstanding challenge is that not all materials are amenable to the standard planar junction fabrication. The device quality, rather than the intrinsic characteristics, may be defining the results. Here, we introduce a technique in which nanowires are placed on the surface and act as a shadow mask for the superconductor. The advantages are that the smallest dimension is determined by the nanowire diameter and does not require lithography, and that the junction is not exposed to chemicals such as etchants. We demonstrate this method with an InAs quantum well, using two superconductors - Al and Sn, and two semiconductor nanowires - InAs and InSb. The junctions exhibit critical current levels consistent with transparent interfaces and uniform width. We show that the template nanowire can be operated as a self-aligned electrostatic gate. Beyond single junctions, we create SQUIDs with two gate-tunable junctions. We suggest that our method can be used for a large variety of quantum materials including van der Waals layers, topological insulators, Weyl semimetals and future materials for which proximity effect devices is a promising research avenue.

Broad Context

In the rapidly advancing field of quantum technologies, some of the breakthroughs are based on the better understood materials, such as silicon and aluminum [1, 2]. However, unresolved challenges with quantum control, coherence times, and scalability make it relevant to explore new materials for quantum devices [3]. In parallel, the development of quantum materials takes advantage of quantum devices as a way of exploring the materials properties and discovering exotic quantum states.

Previous Work: Super-Semi Planar Junctions

One prominent direction is the search and validation of Majorana zero modes in topological superconductors [4]. Among several approaches, planar junctions based on semiconductor quantum wells have been proposed as hosts for Majorana zero modes [5]. Experimental claims of topological superconductivity have been made in InAs and HgTe junctions [6–8]. The possibility of entering the π-junction state at large magnetic fields have been experimentally explored [8–10]. Edge state transport was detected using Josephson interference [11, 12]. Super-semi junctions were also explored as a platform for transmon-like superconducting qubits [13].

Previous Work: Shadowing

Nanowires and nanoflakes have been used to shadow nanowires, for making in situ Josephson junctions, superconducting islands, and normal-superconductor junctions [14–16]. Patterned membranes have also been used as shadow masks [17, 18]. Finally, fabricated tall walls were used for shadow deposition of metals onto selective-area-grown structures [19, 20]. Vanadium oxide nanowires were used as etch templates to produce metallic wires [21].

Superconductor-semiconductor planar junctions to two-dimensional electron gas (2DEGs) were defined by selective etching of the superconducting layer [22–28]. Anodic oxidation method has been developed as one alternative to etching [29]. Though high quality junctions were demonstrated, a concern with this is that the weak link is directly exposed to potentially degrading chemical, thermal or mechanical processing. The requirement for selective etching of metal on semiconductor also limits material choices.

Motivation and Approach

We are motivated by extending the concept of shadowing by nanoscale objects to planar junctions. In our approach, nanowires act as shadow masks protecting part
FIG. 1. The nanowire shadow mask method. (a) A mother chip with nanowires (top) and a 2DEG chip (bottom) are aligned to make contact with each other. (b) After contact, nanowires adhere to the 2DEG chip due to van der Waals interaction. (c) A thin layer of superconductor, Al or Sn, is evaporated onto the 2DEG with nanowires acting as shadow masks. Gray arrows indicate the flux of superconductor. (d) Optical microscope image of a dummy chip after nanowire transfer. Nanowires were grown in square patterns which got imprinted to this chip. (e) Scanning electron microscope (SEM) image of a practice GaAs chip after Al evaporation. The white arrow indicates a nanowire. The black arrows indicate masked areas with nanowires removed by ultrasound. (f) Cross-section high-angle annular dark-field (HAADF) image of a junction shows Al thin film interrupted by the shadowing InSb nanowire on an InAs 2DEG. The layer structure of the quantum well as well as other materials are labeled.

of the surface from superconductor deposition. The key steps of creating a clean interface and the junction along the critical dimension can be performed in situ or ex situ, and can be extended to a variety of materials of interest. The advantages are in avoiding chemical processing of the bulk of the weak link and realizing dimensions that are challenging with liftoff.

List of Results

We deposit InAs and InSb nanowires onto shallow InAs quantum wells, and use wires as shadow masks during the deposition of Al and Sn superconductors. The nanowires are used as self-aligned gates which allows for gate-tunable supercurrents. The product of switching current and normal resistance, $I_{sw}R_N$, is 0.4 mV for Al Josephson junctions (JJs), and 0.86 mV for Sn JJs. Both of these values are higher than their corresponding superconducting gaps, suggesting high transparency interfaces. We fabricate single Josephson junctions and dc-SQUIDs using this method. While this manuscript is dedicated to the introduction of the nanowire shadow planar junction technique, in simultaneous manuscripts we report how the technique allows us to study the anomalously large second-order Josephson effects [30, 31] as well as missing Shapiro steps, a Majorana signature, in the trivial regime near zero magnetic field [32].

Future Relevance

The concept of making planar junctions using nanoscale objects can be taken beyond superconductor-semiconductor structures, and beyond nanowires. One interesting direction to explore is whether junctions can be made using van der Waals materials as weak links. Many important quantum materials are synthesized as bulk crystals rather than thin films, which complicates device fabrication. Dispersal of nanowires on the surface of a 3D crystal can take care of defining the critical dimension. Other objects, such as nanoflakes, nanonetworks or nanocubes, can be used as shadow masks.
FIG. 2. Al-InAs-Al Josephson junction device (JJ-1). (a) Schematic diagram (top) and SEM image (bottom) of a device similar to JJ-1. The nanowire is contacted by the Ti/Au electrode to function as a self-aligned gate. (b) Differential resistance \(dV/dI\), bottom as a function of the bias current \(I\) and the gate voltage \(V_g\). Top: switching current \(I_{sw}\), black and the \(I_{sw}R_N\) product (red) extracted from data in the bottom. (c) Differential conductance \(dI/dV\) as a function of the bias voltage \(V\) and \(V_g\). White arrows indicate the first and second multiple Andreev reflections using \(\Delta = 0.21\) meV.

The remaining density becomes smaller and smaller.

For our first generation of devices, which use InSb nanowires, the contact between the two chips is made inside an MBE vacuum cluster. This allows, in principle, to not break vacuum between the 2DEG growth, nanowire transfer and superconductor deposition. In our case, the quantum well was grown earlier and stored outside. To remove the native oxide, atomic hydrogen cleaning is performed prior to superconductor deposition. For our second generation of devices, which use HfO\(_2\)-covered InAs nanowires, the contact is made in air to increase the efficiency without sacrificing the cleanliness of the super-semi interface.

The scanning electron microscope (SEM) image of a practice GaAs chip with nanowires coated with 10 nm of Al is shown in Fig. 1(c). Here, nanowires are removed by ultrasound after superconductor deposition revealing the shadow. However, for planar junctions we keep the wires in place, for two reasons. First, we use nanowires as markers of where the shadowed regions are, since the superconductor film is thin and difficult to resolve under microscope. Second, we use nanowires as self-aligned gates, see Fig. 2.

The cross-section scanning transmission electron microscope (STEM) image of a planar junction is shown in Fig. 1(f). This image is reproduced in the schematic panel (c). Al layer is capped \textit{in situ} with evaporated aluminum oxide or oxidized in the load-lock chamber to prevent dewetting. The InSb nanowire is not in electrical contact with the 2DEG due to the native oxide on the nanowire’s surface: the planar junction structure consists of two Al contacts on the left and right and the quantum well. The Al film is smooth and the contacts are sharply defined. The gap of 140 nm between the left and right Al layers is determined by the nanowire width. The top and the right facets of the hexagonal nanowire are also coated with Al but that layer is not in contact with the 2DEG. The thicknesses of InGaAs/InAs/InGaAs layers are 10/5/10 nm. A 10 nm layer of Al is deposited onto the quantum well substrate cooled to 80 K.

**Figure 2: Al/2DEG Josephson Junction**

The final step in the junction fabrication is an etch step. As can be seen in Fig. 1(e) the superconductor fully surrounds the nanowire shadow. But a junction requires two separate superconducting contacts. As Fig. 2(a) illustrates, we etch away the areas colored pink, while the superconductor and the quantum well is left in the gray/metallic area.

We leave the nanowire in place to be used as a self-aligned electrostatic gate. In order to do this, we choose InAs nanowires which are coated with hafnium oxide while still standing (prior to step shown in Fig. 1(a)). We use InAs in order to make sure that the nanowire itself is conducting as required for the gate effect. The reason for a hafnium oxide coat is to protect the nanowire during the wet etching step. It also acts as a dielectric layer between the nanowire gate and the quantum well. A Ti/Au contact is made to the nanowire in order to actuate the gate. Hafnium oxide is removed in the contact area by argon-ion milling. The nanowire is suspended in between the Ti/Au contact and the Al/2DEG junction. Note that the Al layer on top of the nanowire is removed during the wet etch step in the suspended segment. Transport data in the main text are taken from devices that use HfO\(_2\)-covered InAs nanowires. Devices using InSb wires, without hafnium oxide and without the gate contact, are presented in supplementary materials 35.

We present a gate-tunable Josephson supercurrent trace in Fig. 2(b). Measurements are performed in a dilution refrigerator at temperatures of 50 mK. Supercurrent can be fully suppressed by the gate voltage near zero. Though non-superconducting current cannot be pinched off, likely due to parallel conduction in the quantum well.
Figure 3: Al/2DEG SQUIDs

Next, we fabricate gate-tunable superconducting quantum interference devices (SQUIDs). Fig. 3(a) shows SQUID-1 consisting two Al-InAs-Al planar junctions, JJ_a and JJ_b, connected in parallel. The two nanowires have landed nearby during the transfer step. For this figure we define the “off” state where \( I_{sw} \) is zero, and the “on” state where \( I_{sw} \) is above 1 \( \mu \)A. However, the critical current is continuously tunable with gates similar to Fig. 2(a). We note that junctions are still conducting in the “off” state even though supercurrent vanishes. When the magnetic field is applied in the out-of-plane direction, Fraunhofer-like modulation of \( I_{sw} \) in the two junctions show similar periodicity (Fig. 3(b),(c)), as expected for junctions with the same nominal geometry. The effective length (\( L_{eff} \), along the direction of the current) of the junction can be calculated with \( L_{eff} = \Phi_0/WB_0 \), where \( \Phi_0 = h/2e \) is the magnetic flux quantum, \( W = 5 \) \( \mu \)m is the junction width, \( B_0 = 0.28 \) mT is the modulation period. We get \( L_{eff} = 1.5 \) \( \mu \)m. This value is an order of magnitude larger than the typical geometric length (\( L \)) of these junctions. This difference likely indicates large London penetration depth (\( \lambda_L \)). With \( L_{eff} = L + 2\lambda_L \), we estimate \( \lambda_L \) close to 700 nm. The large difference between \( L_{eff} \) and \( L \) is also reported in other systems [39]. This junction length significantly exceeding the geometric length should be taken into account when estimating system size for planar junction topological superconductivity attempts, it may be too large to enter the single mode regime [5,7].

When both junctions are in the “on” state, an extra high-frequency modulation of the switching current due to SQUID interference arises [Fig. 3(d),(3(f))]. SQUID-1 area \( S = \Phi_0/B_0' = 1.33 \times 10^3 \) \( \mu \)m\(^2\), where \( B_0' = 1.55 \) \( \mu \)T is SQUID modulation period. This area is consistent with the designed enclosed area which is \( 1.28 \times 10^3 \) \( \mu \)m\(^2\).

Figure 4: Sn/2DEG Devices

The nanowire shadow-mask technique comes with a degree of flexibility in materials combinations. For instance,
FIG. 4. Sn/2DEG SQUID (SQUID-2) and Josephson junction (JJ-2) at 1.1 K. (a) Optical microscope image of SQUID-2. Two shadow nanowires are indicated by arrows. Junctions are underneath nanowires. (b) $dV/dI$ as function of the current ($I$) and the magnetic field ($B$) in SQUID-2. (c) SQUID modulation in a narrower magnetic field range. (d) $dV/dI$ as a function of $I$ and $B$ in JJ-2. The yellow dotted line highlights a kink in $I_{sw}$ studied in [30]. (e) Zero-field $dV/dI$ relation in JJ-2. (f) Zero-field $dI/dV$ as function of the voltage ($V$) in JJ-2. Dashed lines are positions of multiple Andreev reflections with indices labeled for $\Delta = 0.57$ meV. A series resistance of 1.4 $\Omega$ and a field offset of -0.26 mT are used for recalibrating data in panel (d-f).

one constraint of wet etching is that not every metal can be selectively etched on a semiconductor. Nanowire shadow-removing the need for wet etching in the weak link.

To demonstrate this flexibility, we use another superconductor, Sn (Fig. 4). Sn has a higher critical temperature than Al (3.7 K in Sn vs 1.2 K in Al), thus a larger superconducting gap, and stronger spin-orbital coupling compared to Al. Sn has been used to demonstrate hard gap, parity preserving transport, and field resilience in nanowire superconductor-semiconductor devices [16]. These properties make Sn a promising material for realizing topological superconductors in hybrid devices. At the same time, despite our efforts, selective etching of Sn on InAs or InSb has been a challenge.

Sn is deposited onto InAs 2DEGs covered with InAs nanowires in the same setup that is used for Al deposition. The substrate is cooled to 80K for Sn deposition. Sn is capped with a layer of evaporated aluminum oxide. Two Sn/2DEG devices, SQUID-2 and JJ-2 are presented in Fig. 4. Measurements are made at a temperature of 1.1 K, which is much higher than the measurement temperature for Al devices. The measurement at 50 mK gives similar $I_{sw}$ and $I_{sw}R_N$ [35]. Sn devices are based on InAs nanowires, but the wires were not used as gates, for simplicity. Compared to Al/InAs, a different wet etch recipe is used to remove Sn and InAs outside the junction (see supplementary materials [35]).

SQUID-2 shows similar behavior to the Al/2DEG SQUID-1 while the switching current is several times larger [Figs. 4(a)-4(c)]. The Sn/2DEG single junction device, JJ-2, also behaves similarly to its Al counterpart with a larger switching current [Fig. 4(d)].

The $I_{sw}R_N$ product can be deduced from $dV/dI$ versus $I$ in Fig. 4(c). With $I_{sw} = 9$ $\mu$A, $R_N = 95$ $\Omega$, we get an $I_{sw}R_N$ product of 0.86 mV. This is larger than the typical gap of Sn which is 0.6 meV [16]. $I_{sw}R_N$ exceeding the gap is consistent with our findings from Al/2DEG nanowire shadow junctions.

The induced gap of Sn can be deduced from MAR peaks in the differential conductance [$dI/dV$, Fig. 4(f)]. We estimate $\Delta = 0.57$ meV. Vertical dashed lines in Fig. 4(f) show calculated positions of MAR peaks with indices labeled. Similar gap sizes are observed at 50 mK and in two other devices (Fig. S17). Note that, like in Al devices, not all peaks fit the the MAR series at higher indices ($\geq 5$).

The Fraunhofer-like pattern shows kinks near half period [Figs. 3(b), 3(c), Fig. 3(d)], more and stronger examples in supplementary materials [33]. The Al SQUID oscillation also shows kinks. These observations can be explained by a strong second-harmonic component in the current-phase relation. A detailed study is presented in a separate manuscript [30, 31]. The inversion-symmetric character of magnetic flux diffraction patterns, more clearly seen in supplementary materials [35], can be explained by self-field effects.

Conclusions

We introduce a method for fabricating planar Josephson junctions using nanowires as both shadow masks and self-aligned electrostatic gates. We fabricate and characterize single junctions and SQUIDs based on Al and Sn as superconducting materials. The weak link is a 2DEG in the shallow InAs quantum well. $I_{sw}R_N$s of about 0.4 mV and 0.86 mV are observed in Al and Sn junctions, re-
spectively, both larger than their superconducting gaps. Our studies are split in three manuscripts, this technique paper being the first. In the second, we observe deviations from a sinusoidal current-phase relation in oscillations of $I_{sw}$ in single junctions and SQUIDs. The deviations are related to a large second-order Josephson harmonic [30]. In the third manuscript, the Shapiro step measurement is performed, showing that a series of odd Shapiro steps are missing which is related to several different origins [32].

Data Availability

Curated library of data extending beyond what is presented in the paper, as well as simulation and data processing code are available at [40].

Duration and Volume of Study

This study proceeded over three periods. The first period was between September 2016 to January 2017. We proved the concept of the nanowire shadowing with dummy chips.

The second period was between August 2018 to June 2019, including sample preparation, device fabrication and measurements. We explored the first-generation devices (Al, InSb nanowire, without gates). More than 7 devices on 1 chip are measured during 2 cooldowns in a dilution refrigerator, producing about 8900 datasets.

The third period was between March 2021 to February 2022. We explored the second-generation devices, (Al or Sn, InAs/HfO$_2$ nanowire, with self-aligned nanowire gates). 62 devices on 6 chips are measured during 8 cooldowns in dilution refrigerators, producing about 5700 datasets.

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Supplementary Materials: Planar Josephson Junctions Defined by Nanowire Shadowing

I. Author Contributions

A.-H.C and M.H. grew InAs nanowires. M.P., J.S.L., C.D., A.M., S.D.H., J.T.D., and C.J.P grew quantum wells and superconducting films with nanowire shadowing. S.T. performed STEM study. P.Z., A.Z., B.Z., S.M., and H.W. fabricated devices. P.Z., L.J, V.V.d.S, and A.Z. performed measurements. P.Z. and S.M.F. wrote the manuscript with inputs from all authors. S.M.F. directed the project.

II. Device information

TABLE S1. Information of devices discussed in this manuscript. JJ-1, JJ-2, SQUID-1, and SQUID-2 are discussed in the main text. The rest are discussed in supplementary materials.

| Chip name | JJ-#   | SQUID-# | Chip reference | Wafer | Description                        |
|-----------|--------|---------|----------------|-------|------------------------------------|
| Al-chip-1 | S3-S8  | -       | 2019 2DEG      | SH180919 | SH180919 QW + InSb NWs            |
| Al-chip-2 | S0-S11 | -       | 20210329 Al InAs 2DEG | MP738 | MP728 QW + NW637 InAs NWs         |
| Al-chip-3 | 1, S1-S2 | 1 | 20210924 Al InAs 2DEG | MP738 | MP728 QW + NW637 InAs NWs         |
| Sn-chip-1 | S12-S16 | S1  | 20210907 Sn InAs 2DEG | MP739 | MP728 QW+ NW637 InAs NWs          |
| Sn-chip-2 | 2, S17-S20 | 2, S2 | 20211009 Sn InAs 2DEG | MP739 | MP728 QW + NW637 InAs NWs         |

III. Full Methods

Layer structure of SH180919 used in Al-Chip-1

| Layer structure of SH180919 used in Al-Chip-1 |
|-----------------------------------------------|
| 10 nm In$_{0.75}$Ga$_{0.25}$As                  |
| 5 nm InAs                                       |
| 10 nm In$_{0.75}$Ga$_{0.25}$As                  |
| 10 nm In$_{0.35}$Al$_{0.65}$As                  |
| Si delta doping layer $n_{\text{sheet}}$ 2.5x10^{11}/cm$^2$ |
| 100 nm In$_{0.75}$Al$_{0.25}$As                 |
| 5x (2.5 nm In$_{0.75}$Al$_{0.25}$As – 2.5 nm In$_{0.35}$Ga$_{0.65}$As) |
| 50nm each of In$_{x}$Al$_{1-x}$As x starting from 0.53 to 0.81 to 0.75 in steps of 0.02 |
| 5x (2.5 nm In$_{0.525}$Al$_{0.475}$As – 2.5 nm In$_{0.525}$Ga$_{0.475}$As) |
| 500 nm In$_{0.65}$Al$_{0.35}$As                  |
| Semi-Insulating InP (001) substrate             |

Layer structure of MP728 used in Al-Chip-2,3 & Sn-Chip-1,2

| Layer structure of MP728 used in Al-Chip-2,3 & Sn-Chip-1,2 |
|-----------------------------------------------------------|
| 10.72 nm In$_{0.75}$Ga$_{0.25}$As                        |
| 4.54 nm InAs                                             |
| 10.72 nm In$_{0.75}$Ga$_{0.25}$As                        |
| 25 nm In$_{0.525}$Al$_{0.475}$As                         |
| 20x (3 nm In$_{0.75}$Al$_{0.25}$As – 2 nm In$_{0.525}$Ga$_{0.475}$As) |
| 2x (25 nm In$_{0.525}$Al$_{0.475}$As – 1 nm In$_{0.525}$Ga$_{0.475}$As) each x starting from 0.525 to 0.825 to 0.75 in steps of 0.025 |
| 20x (4 nm In$_{0.525}$Al$_{0.475}$As – 1 nm In$_{0.525}$Ga$_{0.475}$As) |
| Semi-Insulating InP (001) substrate                     |

FIG. S1. Layer structures of quantum well samples used in this manuscript.

2DEG growth. The InAs quantum wells are grown by molecular beam epitaxy (MBE) similar to work reported in [25, 33]. The layer structures of the quantum well samples are depicted in Fig. S1. For SH180919, the mobility on a calibration sample, without the nanowire and superconductor, was estimated to be approximately 25,000 cm$^2$/Vs at a sheet carrier density of $1 \times 10^{12}$ cm$^{-2}$. This corresponds to an electron mean free path of approximately 400 nm. For a similar calibration of MP728, the mobility was measured to be 20,000 cm$^2$/Vs at a sheet carrier density of $4.6 \times 10^{11}$ cm$^{-2}$, corresponding to an electron mean free path of approximately 200 nm. Electron mobility and density in the underlying 2DEG are expected to change after nanowires are brought in contact with the 2DEG surface and superconductors are evaporated.
Nanowire growth (InAs). The InAs nanowires were grown by MBE using the gold assisted VLS mechanism. The samples were prepared as follow. InAs substrates (111)B and (001) were wet deoxidized using NH$_4$OH during 5 min then rinsed in DI water. Gold colloids were immediately deposited after deoxidation on the substrates and samples were introduced to the MBE chamber. After an annealing step at 500 °C under As vapour, nanowires were grown at 420 °C by opening the In shutter. After 75 min of growth, the In shutter was closed and the sample cooled down to room temperature under vacuum. InAs wires under those conditions (BEP V/III ratio 20 and In flux 5 × 10$^{-7}$ Torr) exhibit 60 nm diameter, have a reduced tapered and measure above 4 μm in length. Once removed from the MBE chamber, the samples were introduced to an ALD system for HfO$_2$ deposition (120 °C, 150 cycles, about 5 nm).

Superconducting layer. The InAs quantum wells were removed from UHV post growth of the quantum well and were put face down, i.e. “smashed”, on the surface of their corresponding InAs nanowire chips (for devices with InSb nanowires, the smash was performed in an MBE machine in prior to the hydrogen cleaning step described below). This smashing of the two surfaces, leads to part of the nanowires being transferred to the quantum well chip due to electrostatic attraction. It was observed that smashing the two chips such that the quantum well chip was facing down lead to less debris from the smash being left behind on the same chip. Since this same quantum well chip, now with the nanowires, would be used for superconductor evacuation and subsequent device fabrication, maintaining optimum cleanliness would be beneficial.

While this process of smashing the chips could in principle be carried out without breaking UHV, execution of the same remains a part of future work. Advantages of conducting this process in UHV include preventing the oxidation of the surface of the quantum well while also enabling the growth of the nanowires in UHV (in a separate run) or pre-cleaning of the nanowire chip with atomic hydrogen upon insertion in UHV, prior to smashing.

The nanowire+quantum well “smashed” chip was then re-introduced in UHV for subsequent surface preparation, evaporation of superconductor and passivation. Atomic hydrogen cleaning was performed at a substrate temperature of about 475-480 °C, as measured by a thermocouple, under constant rotation, at a chamber pressure of 5 × 10$^{-9}$ Torr of primarily hydrogen. The samples once cooled to room temperature were moved to a neighboring UHV chamber equipped with a cryogenic sample stage operating at about 80 K (cooled with liquid nitrogen) and effusion cells of aluminum and tin. The samples were then pre-cooled for over an hour in direct contact with the cryogenic sample stage at 80 K, before evaporation of aluminum or tin was started. Typical nominal growth rates of about 10 nm/hr were used for evaporation of the superconducting films of 10 nm thickness at oblique incidence. Al-Chip-1 was immediately moved out of vacuum to oxidize the Al film. Al-Chip-2,3, and Sn-Chip-1,2, were immediately coated with a protective layer of electron-beam evaporated AlOx (nominally 3 nm), before the samples could warm up to room temperature. Further details of this process are described in Ref. [16].

Device fabrication (Al/2DEG). First, the chip is pre-patterned with coordinate markers by e-beam lithography (EBL), e-beam evaporation of Ti/Au, and lift-off. Second, optical-microscope images of nanowires are taken for device designing. Third, gate electrodes are made by EBL, Al etching (CD26 developer:water 1:20 for 2 min, or Transene C for 10 s), Ar ion milling to remove HfO$_x$ (500 V, 25 mA for 60 s in a Plassys system), and then 10/120 nm Ti/Au by e-beam evaporation. At last, mesa of Josephson junctions and SQUIDs are made by EBL using negative tone resistor ma-N 2403, followed by Al etching and InAs etching (water:1M citric acid:38% H$_3$PO$_4$ :H$_2$O$_2$ 220:55:3:3 for 8 min, with agitation). Etch with the Al etchant again to avoid undercuts after 2DEG etching. The ratios of solutions are in volume. EBL resists are “baked” in a vacuum chamber for 8 hours or longer at room temperature to avoid heating.

Device fabrication (Sn/2DEG). The fabrication of Sn/2DEG devices is similar to that of Al/2DEG. In some devices, a 10/100 nm Ti/Au layer is deposited over the leads to short possible discontinuities in the Sn film and avoid cracks due to wire bonding. This Ti/Au layer is made by EBL, Ar ion milling of Al$_2$O$_3$ (250 V, 15 mA for 90 s in a Plassys system), and e-beam evaporation. The Sn layer is etched by first developing in ma-N 525 for 3 min to remove unexposed ma-N 2403 and Al$_2$O$_3$, then etching in 36.5%-38% HCl:water 1:1000 for 10 s. We find the etching rate of Sn in the diluted HCl solution difficult to control. Large undercuts of several μm under the resist may happen. We carefully check the result under an optical microscope after etching for every 5 s to avoid possible undercuts.

IV. Uncertainty in the $I_{sw} R_N$ product

$I_{sw} R_N$ is widely used for characterizing a Josephson junction. We find it is sensitive to the method we use for extracting parameters. For example, in the top-middle part (near 150 mV, 10 μA) of Fig. 2(b) bottom panel, there are red tilted lines which is due to a background increasing linearly against the current. This background may be a result of the gating effect from the source-drain voltage. The larger the current bias, the larger the $R_N$ extracted. This explains the discontinuity in the $I_{sw} R_N$ curve at $V_g$ = 100 and 200 mV because here $R_N$ is extracted at the largest current bias in each vertical line. In the Sn device, we also observe that $R_N$ increases by about 15% between 35 μA and 80 μA, in both positive and negative sides [Fig. 2(e)]. This may be due to the heating effect at large currents.
We take $R_N = 95 \, \Omega$ which is the value near the switching current around $\pm 30 \, \mu A$ to minimize the uncertainty caused by heating.

V. Series resistance and multiple switching currents

Devices are mostly designed to be 2-terminal with long leads on chips. We bond 4 wires to each 2-terminal device to perform 4-terminal measurements, with every two wires sharing one lead. This may lead to a series resistance and multiple superconducting switching currents if a lead has non-superconducting regime besides the junction. Breaks in the superconducting film may be caused by unexpected masking nanowires on leads, scratches on the surface, or damage made by wire bonding. We have observed series resistance and multiple switching currents in both Al and Sn devices. In Al devices these issues are very rare (Fig. S8). The Al film seems to be less fragile against scratches and wire bonding comparing to the Sn film. Another property of Sn that may contribute to these issues is that Sn has two common phases, one of which is not superconducting. To suppress the series resistance and extra superconducting switchings in Sn devices, we either make four-terminal leads on the chip or short long leads by a Ti/Au layer (Fig. S11).

VI. Magnetic field offset

Numerical offsets are applied to the magnetic field so that $I_{sw}$ always maximizes at “zero” magnetic field. The offset is typically of the order of hundreds $\mu T$. It may be due to fluxes trapped in devices or the magnet itself.

Comment on data in Figure 4 - Sn/InAs junctions. Devices in this batch are hysteretic about the magnetic field. The field is scanned from negative to positive in Fig. 4(d). The left part of the oscillation is stretched while the right part of the oscillation is squeezed (For details, see Fig. S18). The hysteretic behavior may be caused by fluxes trapped in junctions. Non-linear behavior of a magnet at mT range may also lead to a hysteresis. However, we do not observe such a strong hysteretic behavior about the magnetic field in Al devices in the same fridge (Fig. S9). Optimization to the device design such as avoiding sharp kinks in a path can be made in future works to avoid possible vortex accumulation.

VII. Supplementary data from Al/2DEG devices at 50 mK

![FIG. S2. Optical microscope image of JJ-1 (Al/2DEG) which is discussed in the main text. The vertical bright gray path is the Al/2DEG mesa. The yellow lead is the Ti/Au electrode contacting the nanowire which is a dark line on the top of the mesa. The rest is wet etched.](image_url)
FIG. S3. V-I curves at different gate voltages in JJ-1. Data are extracted from Fig. 2b).

FIG. S4. Fraunhofer diffraction patterns of JJ-1 (Al/2DEG) at a variety of gate voltages which are noted at the top of each panel. The field is shifted by -0.23 mT in all panels so that $I_{sw}$ maximizes at zero field.
FIG. S5. Characterization of device JJ-S1 (Al/2DEG) which is similar to JJ-1 in the main text. (a) Differential resistance as a function of the current and the magnetic field. The superconducting switching current $I_{sw}$ undergoes a Fraunhofer-like oscillation. Kinks appear in the oscillation at the half period. The gate voltage $V_g = 400$ mV. (b) Differential conductance as a function of the bias voltage and the gate voltage. Horizontal resonances are due to multiple Andreev reflections. (c) Differential resistance as a function of the current and the gate voltage (bottom). Extracted $I_{sw}$ and $I_{sw}R_N$ as a function of the gate voltage (top). $I_{sw}R_N$ saturated near 0.3 mV. The field is offset by a value of about -0.2 mT so that the zero field is where the switching current maximizes.

FIG. S6. Characterization of device JJ-S2 (Al/2DEG) which is similar to JJ-1 in the main text. (a) Differential resistance as a function of the current and the magnetic field. The superconducting switching current $I_{sw}$ undergoes a Fraunhofer-like oscillation. Kinks appear in the oscillation at the half period. The gate voltage $V_g = 400$ mV. (b) Differential conductance as a function of the bias voltage and the gate voltage. Horizontal resonances are due to multiple Andreev reflections. (c) Differential resistance as a function of the current and the gate voltage (bottom). Extracted $I_{sw}$ and $I_{sw}R_N$ as a function of the gate voltage (top). $I_{sw}R_N$ saturated near 0.35 mV. The field is offset by a value of about -0.2 mT so that the zero field is where the switching current maximizes.
FIG. S7. Data from multiple devices on Al-chip-1. (a) SEM of a typical device on this chip. The dark stripe through the mesa is over-dosed m-a-N 2403 resist residue. The designed dose in this area is accidentally doubled. The mask wire on this chip are bare InSb nanowires. They get etched by the 2DEG etchant. On newer chips we use InAs nanowires covered by HfO$_x$ protecting layer to avoid etching so that nanowires can be connect by Ti/Au electrodes next to the mesa. (b-g) Fraunhofer diffraction patterns in JJ-S3, JJ-S4,..., JJ-S8, respectively. Offsets ($< 0.5$ mT) are applied to the field so that $I_{sw}$ maximizes at zero field.

FIG. S8. Data from multiple devices on Al-chip-2. (a) SEM of a typical device. The mask nanowires are InAs coated with HfO$_x$ protecting layer. These nanowires are resistant to the 2DEG etchant. No gate electrodes are made on this chip. (b) SEM of a device showing a rare event that the nanowire is accidentally moved during the fabrication. The arrow shows the junction which is a bright thin line across the mesa. (c) SEM of device JJ-S9. Directions of vertical and horizontal in-plane magnetic fields are labeled. (d-f) Fraunhofer diffraction patterns in JJ-S9, JJ-S10, JJ-S11, respectively. JJ-S10 manifests extra superconducting switchings which may be due to breaks of Al film in the leads. Offsets ($\leq 0.2$ mT) are applied to the field so that $I_{sw}$ maximizes at zero field.
FIG. S9. The differential resistance $dV/dI$ in JJ-S9 shows no obvious hysteresis against the field or the current. The scan direction of the field and the current is indicated by arrows on the top and left, respectively. Original magnetic field without an offset is shown.

FIG. S10. (a-g) Diffraction patterns of JJ-S9 in a variety of vertical in-plane magnetic fields $B_{//,v}$ [Fig. S8(c)]. The out-of-plane field where $I_{sw}$ maximizes shifts as $B_{//,v}$ increases, indicating a small misalignment between the field and device plane. The current is scanned from negative to positive. (h) Similar as (g) but the current is scanned from positive to negative. $I_{sw}$ shows strong hysteresis in the presence of an in-plane field.
VIII. Supplementary data for Sn/2DEG devices at 50 mK and 1.1 (or 1.2) K

FIG. S11. Optical microscope image of Sn/2DEG devices in the main text. Both devices are on Sn-chip-2. (a) SQUID-2. This panel duplicates Fig. 4(a). (b) JJ-2 which is indicated by the yellow arrow.

FIG. S12. V-I curve in JJ-2. The right panel shows zoomed-in regime of the left panel. The sweep direction is indicated by black arrows on the right.
FIG. S13. Data from multiple devices on Sn-chip-1 which is not shown in the main text. $T = 1.2$ K. (a-e) Single Josephson junction devices JJ-S12, JJ-S13, ..., JJ-S16. The measurement is performed with a locin-in amplifier. The AC excitation is 100 nA, the frequency is either 77.77 Hz or 88.77 Hz for different measurements. The ac signal is accidentally damped by 15% due to the grounding and filters. (f-g) $dV/dI$ in SQUID-S1 measured by the DC method. JJ-S13 and SQUID-S1 are measured by the 4-terminal method. Other devices are measured by the 2-terminal method with an ac probe resistance of 3.4 kΩ (smaller than the dc resistance due to the damping). The resistance below $I_{sw}$ may be larger than the probe resistance due to non-superconducting parts in device leads and bonding pads. We suppress the on-chip series resistance by covering leads with a layer of Ti/Au or making four leads instead of two on Sn-chip-2 (Fig. S11,S15,S16).

FIG. S14. (a-e) Similar to Fig. S13(a-e) except that the temperature $T = 50$ mK. Extra superconducting switches are clear at this temperature. They may be due to non-superconducting parts in leads or pads of devices. We suppress extra superconducting switches by covering leads with a layer of Ti/Au or making four leads instead of two on Sn-chip-2 (Fig. S11,S15,S16).
FIG. S15. Data from multiple devices on Sn-chip-2. $T = 1.1$ K. (a) JJ-S17, (b) JJ-S18, (c) JJ-2, (d) JJ-S19, (e) JJ-S20, (f) SQUID-2, (g) SQUID-S2. All devices are measured with dc signal and the 4-terminal method.

FIG. S16. Similar to Fig. S15 at 50 mK.
FIG. S17. Differential resistance $dV/dI$ versus current $I$ (top panels) and differential conductance $dI/dV$ versus voltage $V$ (bottom panels) for devices (a,b) JJ-S17, (c,d) JJ-2, and (e,f) JJ-S20, at zero field. The switching current $I_{sw}$ and the normal resistance $R_N$ at 1.1 K are similar to those at 50 mK. The $(I_{sw}, I_{sw} R_N)$ extracted from (a,c,e) are (6.4 $\mu$A, 0.90 mV), (9.0 $\mu$A, 0.86 mV) , and (4.0 $\mu$A, 0.54 mV), respectively. In panel (a), $R_N$ keeps increasing above 25 $\mu$A, which may be due to the heating effect. We take $R_N = 140 \Omega$ which is the value near the jump at 25 $\mu$A in (a). The vertical dashed lines in (b,d,f) are calculated multiple Andreev reflection voltages at $\pm 2\Delta/ie$, with $\Delta = 0.57$ meV for all three panels and $i = 1, 2, 3, 4$. Fields are shifted (see Figs. S15,S16) so that the zero field is where the switching current maximizes. A series resistance of 1.4 $\Omega$ is subtracted from (c, d).

FIG. S18. The differential resistance $dV/dI$ in JJ-2 shows no obvious hysteresis about the current but obvious hysteresis about the field. The scan direction of the field and the current bias is indicated by arrows on the top and left, respectively.