Achieving Real-Time Execution of Transformer-based Large-scale Models on Mobile with Compiler-aware Neural Architecture Optimization

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Abstract

Pre-trained large-scale language models have increasingly demonstrated high accuracy on many natural language processing (NLP) tasks. However, the limited weight storage and computational speed on hardware platforms have impeded the popularity of pre-trained models, especially in the era of edge computing. In this paper, we seek to find the best model structure of BERT for a given computation size to match specific devices. We propose the first compiler-aware neural architecture optimization framework (called CANAO). CANAO can guarantee the identified model to meet both resource and real-time specifications of mobile devices, thus achieving real-time execution of large transformer-based models like BERT variants. We evaluate our model on several NLP tasks, achieving competitive results on well-known benchmarks with lower latency on mobile devices. Specifically, our model is 5.2× faster on CPU and 4.1× faster on GPU with 0.5-2% accuracy loss compared with BERT\textsubscript{BASE}. Our overall framework achieves up to 7.8× speedup compared with TensorFlow-Lite with only minor accuracy loss.

1 Introduction

Transformer-based self-supervised models have demonstrated their high efficacy in learning universal language representations from large-scale unlabeled data, and have been fine-tuned to adapt to various downstream Natural Language Processing (NLP) tasks. Representative efforts, such as BERT (Devlin et al. 2018), XLNet (Yang et al. 2019), RoBERTa (Liu et al. 2019), GPT-2 (Radford et al. 2019), MobileBERT (Sun et al. 2020), and DistilBERT (Sanh et al. 2019), have substantially advanced the state-of-the-art across a wide spectrum of tasks, including text classification, natural language inference, and question answering.

These models are extremely deep and large, consisting of hundreds (or even thousands) of layers and hundreds of millions of parameters (e.g., 12 transformer blocks with 109M parameters and 24 transformer blocks with 340M for BERT\textsubscript{BASE} (Devlin et al. 2018) and BERT\textsubscript{LARGE} (Devlin et al. 2018), respectively). This fact severely challenges their wide deployment on resource-limited edge devices, such as varied mobile phones.

However, with the increasing popularity of mobile AI applications and the concerns of information security and privacy, it has the demands to execute such models on the edge devices. Therefore, how to accommodate the large and extremely deep models, such as BERT, to edge device becomes an imminent problem. Furthermore, when it comes to edge computing, it commonly has a real-time requirement, making the problem even challenging.

Over the past year, more compact models have been introduced to reduce BERT model size while maintaining the accuracy for multiple downstream NLP tasks. For example, MobileBERT has 4.3× smaller model size over BERT\textsubscript{BASE} with small accuracy loss (Sun et al. 2020); however, it has over 2,000 computation layers, the same as BERT\textsubscript{LARGE}. Such a compact model significantly reduces memory requirement; however, we observe that a large number of model layers introduces considerable execution overhead, thus obstructing the latency reduction.

Table 1 validates our above analysis. Specifically, MobileBERT has much fewer FLOPs (5.3×) but many more layers compared to VGG-16 (Simonyan and Zisserman 2014). The deep layers introduce a large number of intermediate results (e.g. MobileBERT contains over 1G intermediate results), which need to be swapped out to the main memory. However, mobile GPU has longer latency to read/write data from the main memory. As a result, with 5.3× fewer FLOPs, the speed of MobileBERT is even 6.2× slower than VGG-16.

The large model depth (e.g., BERT\textsubscript{LARGE} and MobileBERT) not only affects inference latency but also brings challenges in compiling models to mobile devices. To the best of our knowledge, only TensorFlow-Lite (TFLite) (TensorFlow 2017) supports deploying BERT models on mobile CPU (not on mobile GPU), while no other frameworks can even support BERT models on mobile CPU.

The above observations clearly demonstrate that the compiler-agnostic network architecture design can be hardly beneficial since the compiler will generate codes with high latency or even cannot generate the code to run on mobile devices. However, almost all network architecture design works (a.k.a. neural architecture search, NAS) assume a general compiler and assume that the identified network architecture can be compiled to the mobile device, including recent hardware-aware NAS. This may be true for shallow
convolutional neural networks, but for the deep transformer-based models, we claim that the compiler optimizations have to be involved in the neural architecture optimization loop.

In this paper, we propose the first Compiler-Aware Neural Architecture Optimization framework (called CANAO) to search for the large transformer-based models like BERT and its variants on mobile devices. CANAO for the first time involves the compiler optimizations in the NAS loop, aiming to co-optimize the model accuracy and computation resource usage, such that the resultant architectures can be compiled to target mobile devices for real-time execution.

We focus our study on the impact of model depth (and width) on the accuracy and compiler optimizations. We rely on an empirical study to evaluate these impacts by testing both the model accuracy and performance on the real mobile devices with our compiler optimizations.

We involve the compiler optimization into the NAS search loop, in which our latency reward is from the compiler optimized model. The latency information together with the model accuracy from the training stage will feedback to the controller to improve the prediction of neural architectures.

This paper makes several major contributions as follows:

- It advances a compiler-aware neural architecture optimization framework to search for a desirable architecture for BERT models to achieve a good balance between accuracy and latency.
- It proposes a highly effective layer fusion method to reduce intermediate results to achieve better performance on both mobile CPU and GPU.
- It evaluates CANAO on multiple BERT variants, and compares with a state-of-the-art framework, TFLite, proving CANAO outperforms TFLite by up to 7.8× speedup. Particularly, CANAO is the first framework supporting BERT execution on both mobile CPU and GPU.

Evaluation results show that our models CANAOBERT and CANAOBERT with NAS can achieve significantly lower latency with minor accuracy loss. Specifically, our model (executed on CANAO) is 5.2× faster on CPU and 4.1× faster on GPU with 0.5%-2% accuracy loss compared with BERTBASE. These results demonstrate that CANAO can achieve real-time execution of large transformer-based models on an off-the-shelf mobile phone.

## 2 Related Works and Motivation

### Language Model Compression

**General DNN compression techniques** can also be used for language models. There are three main directions for compressing DNN models: weight pruning, knowledge distillation, and quantization.

**Model pruning** identifies and removes redundant or less important weights. There are typically two types of pruning: non-structured pruning (Han, Mao, and Dally 2015) and structured pruning (Wen et al. 2016). Non-structured pruning usually results in higher compression rates. However, it incurs overhead in both weight storage and computation due to its introduced irregularity. Structured pruning overcomes the limitation of non-structured pruning by maintaining a more regular model structure. However, it usually leads to a more severe accuracy degradation with the same compression rate, due to its coarser pruning granularity. It is worth noting that although model pruning has shown its efficacy on other DNN models, it cannot achieve as a high compression rate on transformer-based language models as on VGG-16 (Simonyan and Zisserman 2014) or ResNet-18 (He et al. 2015). For example, existing effort achieves up to 2× compression rate with a 1-2% drop in accuracy/F1 for all the downstream tasks (Guo et al. 2019).

**Knowledge distillation** is another compression technique, where a compact model (called student model), is generated by distilling the knowledge from a larger model (called teacher model). The student model is trained to imitate the behavior produced by the large teacher model. It is widely used in various compact transformer-based language models, for example, DistilBERT (Sanh et al. 2019) manages to reduce half of the layers by applying knowledge distillation to BERT during pre-training; TinyBERT (Jiao et al. 2019) distills BERT in both pre-training and fine-tuning process; MobileBERT (Sun et al. 2020) uses knowledge distillation in the pre-training stage while maintaining the same depth as BERTLARGE.

**Quantization** has become a popular optimization method for embedded deployment. It quantizes the weights or activations of a model into lower-bit representations (Ganesh et al. 2020). Take int8 as an example, it uses 8-bit integers instead of 32-bit floating-point numbers, and integer math instead of floating-point math. This helps reduce both memory and computing requirements, fitting models on low-power controllers and FPGAs, and is orthogonal to this work.

### Neural Architecture Search

With the development of AI democratization, automatic machine learning (AutoML) has been a hot research area in the past few years. NAS, an engine in AutoML, aims to automatically explore the optimal and efficient architecture design for a particular application. Recently, the multi-objective NAS is proposed to take network efficiency into consideration during the NAS process.
DNN Inference Frameworks on Mobile Devices  Mobile computing becomes more and more powerful due to the rapid progress of mobile processors, e.g. Snapdragon 865 (Qualcomm 2019). Multiple state-of-the-art inference frameworks spring up on mobile devices. TVM (Chen et al. 2018), TFLite (TensorFlow 2017), Alibaba Mobile Neural Network (MNN) (Alibaba 2020), and PyTorch Mobile (PyTorch 2019) are representative ones. TVM is a compiler-assisted inference framework on varied devices. TFLite, MNN, and PyTorch are dedicated counterparts running on mobile devices. These frameworks mainly focus on CNN accelerations. TFLite is the only exception; however, it supports BERT on mobile CPU only (no mobile GPU support). To the best of our knowledge, CANAO is the first optimized end-to-end acceleration framework to run various BERT models on both mobile CPUs and GPUs.

Motivation & Problem Definition  Current transformer-based language models have hundreds of millions of parameters. Many of them are extremely deep, leading to high inference latency on edge devices. Take BERT (BERTBASE) as an example. Its high memory and computation cost makes it hard to be deployed on edge devices with limited resource. MobileBERT addresses this issue by designing a new model based on BERTLARGE and distilling it to a small one with the size of 23% of BERTBASE. However, MobileBERT’s layer count remains the same as BERTLARGE (over 1,000 computation layers). As a result, although MobileBERT has much fewer FLOPs (19%) compared to VGG-16 (Simonyan and Zisserman 2014), it still runs 6.2× slower than VGG-16 on mobile, far from real-time execution. Other compact models (e.g., DistilBERT and TinyBERT) remove over half number of layers compared to BERTBASE by using knowledge distillation. These efforts raise a few open questions:

- Does BERT really need more layers? Under similar FLOPs, which type of models show higher accuracy on downstream tasks, wider ones or deeper ones?
- If deeper models are preferred, how can we accelerate the inference to achieve real-time execution?

### 3 Compiler-aware Neural Architecture Optimization Framework (CANAO)

#### 3.1 CANAO Overview

Although the hardware-aware NAS has been proposed to optimize network architectures with the awareness of latency; however, there is still a missing link between neural network search and compiler optimization. For instance, all the existing hardware-aware NAS: MnasNet (Tan et al. 2018), FBNet (Wu et al. 2019), ProxylessNAS (Cai, Zhu, and Han 2018) assumes a general, non-optimized compiler. It may be fine for computer vision applications with shallow layers, but for the network with hundreds of layers, the inference latency can easily exceed the target without the optimization of the compiler, rendering the hardware-aware NAS useless. In this work, we involve the compiler optimizations in the NAS search loop, and propose the first compiler-aware neural architecture optimization framework (called CANAO). CANAO can guarantee the identified model to meet both resource and real-time specifications of mobile devices, thus achieving real-time execution of large transformer-based models like BERT variants while maintaining accuracy.

CANAO consists of two processes: training and compiler code generation (as shown in Fig. 1). The training process consists of a controller for predicting/generating the model hyperparameters (i.e., network architecture), and a trainer to train the predicted model and (quickly) evaluate its accuracy by fine-tuning the model to downstream tasks. The compiler code generation process takes the predicted model and returns execution information (e.g. latency, number of fused layers, CPU/GPU utilization). The execution information together with the model accuracy from the training process will be feedback to the controller to improve the prediction of neural architectures. After the compiler-aware NAS, the generated codes by our optimized compiler will be deployed for mobile CPU/GPU executions.

For the training process, we use the controller to generate architectural hyperparameters of neural networks. We find that the number of layers in BERT models plays a major role in model accuracy, which should be determined firstly while searching the optimized model architecture. Then, the layer size can be optimized by considering both the model accuracy and inference latency. Thus, we divide the training process into two phases: 1) The determination of the number of transformer blocks; 2) The optimization of size for each layer. Accuracy and latency are set as reward signals to feedback to the controller. The controller maximizes the expected reward to find the desirable architecture.

The compiler code generation process is composed of three steps: First, it generates a computational graph from the generated model by NAS controller and applies multiple optimizations on this graph. Second, it employs a novel compiler-based layer fusion optimization to further improve execution performance. This is the key to achieve better hardware efficiency. Third, it employs code generation and optimization to generate and further optimize the inference code. The generated inference code is tested on mobile devices. According to the feedback from the device side, the controller makes a better tradeoff between model accuracy and
and hardware efficiency (e.g., latency).

### 3.2 Model Depth Exploration

As mentioned in Section 2, the extremely deep and large size of current Transformer-based language models make them hard to be implemented on edge devices. To understand the impact of model size and depth on NLP tasks, we conduct the following explorations: We use BERT as the prototype model to build four groups of models with four different levels of FLOPs to study the impact of model depth/size on accuracy. As shown in Table 2, these levels are 22GFLOPs, 10GFLOPs, 8GFLOPs, and 6GFLOPs, respectively. Two models with the same FLOPs but different model architectures are included in each group to explore the impact of the model depth on accuracy. - one is a relatively deep-and-narrow model, and the other is a relatively shallow-and-wide model. In the second column of Table 2, L, H, A stand for transformer blocks, hidden layer size, attention head number, respectively. The third column shows the number of computation layers for each model. Columns 4 ∼ 6 show the accuracy tested on three GLUE tasks: MRPC, STS-B, and RTE (see in Section 4.1).

From the results of the first three groups, with FLOPs 22G, 10G, and 8G, we can see that a larger model size (with higher FLOPs) can increase the model accuracy. Then, we compare the two models with different architectures in each group. We can find that under the same FLOPs, the deep-and-narrow models consistently achieve higher accuracy than the shallow-and-wide models, with accuracy improvements up to 6%. More interestingly, we design two 6G models, make them deeper than the two 8G models and compare the accuracy. We can see that, even with smaller model size, the two 6G models achieve higher model accuracy than the 8G models, respectively, on all tasks except for STS-B. This further demonstrates that the depth of the model is the primary factor to model accuracy. The relatively deep-and-narrow models generally have higher accuracy than shallow-and-wide models under the same amount of computation. This is the answer for the first question in Section 2. More layers are indeed needed to achieve higher accuracy for the Transformer-based language models.

However, the model depth cannot be increased arbitrarily, for two reasons: 1) As the model goes deeper, the growth of accuracy will saturate, analogous to the trend of classification accuracy of ResNet models (He et al. 2016); 2) Limited by the latency requirement and storage on edge devices, we have to trade-off the model width to increase the model depth. This will reduce the number of attention heads, which is proportional to the model width. If the number of the attention head is less than or the hidden layer size is smaller than a threshold, a noticeable accuracy degradation will occur (Michel, Levy, and Neubig 2019; Sun et al. 2020).

Thus, a proper layer number is essential to model accuracy and should be determined prior to other optimizations.

### 3.3 Compiler-aware NAS

To better implement BERT on mobile devices, we propose a compiler-aware NAS scheme in our framework. Unlike MnasNet (Tan et al. 2018), which directly uses the model inference latency as the reward, we involve the compiler optimization into the NAS search loop and our latency reward is from the compiler optimized model. This takes our NAS scheme one step further, allowing us to search for better models that take compiler optimization results into account.

In our NAS scheme, a fast searching process is ensured by the following two aspects: 1) the smaller search space; 2) quick evaluation of accuracy and latency reward.

**Smaller search space:** In BERT, the width of the attention head for each layer is set to 64, so we only need to search for the size of hidden layer in multiples of 64. This also matches the hardware parallelism degree enabled by compiler-generated codes. According to the previous works (Michel, Levy, and Neubig 2019; Sun et al. 2020), the accuracy will decrease when hidden layer size is smaller than 256. Thus, we set the lower bound of hidden layer size to 256. As a result, our search space is significantly reduced.

**The quick evaluation of accuracy and latency reward:** It is usually very costly to complete a full training process to get the final model accuracy for each NAS step. To overcome this issue, we only train the model for a certain number of epochs and use the early-stage accuracy as the accuracy reward to reflect the overall model accuracy. This can significantly reduce the time of each searching step.

On the other hand, the latency reward can also be obtained quickly. To get the latency reward of the compiler-optimized model, the compiler takes the predicted model architecture in the current searching step and examines the optimized model inference latency based on generated compiler-optimized execution code. The time costs of the compiler code generation process are mainly contributed by computation graph optimization, LP fusion, and polyhedral code generation (as introduced in Section 3.4). Note that the compiler code generation process is independent of the training process since it only requires the architecture of the current predicted model and does not need the accuracy. Thus, the compiler code generation process can be executed with the training process in parallel. In general, our compiler code generation process is much faster than the training process. The time costs of the compiler code generation process can be completely hidden by the training time (no extra time cost to be compiler-aware). Moreover, if the latency of the compiler-optimized model cannot satisfy the design target, the lengthy training process will be terminated early to speed

**Table 2:** Accuracy of BERT variants with different depth and width levels. The models are distilled from BERTLARGE (Turc et al. 2019) with layer drop to match the FLOPs.

| FLOPs  | Model layer configuration | Layer count | MRPC | STS-B | RTE |
|--------|----------------------------|-------------|------|-------|-----|
| 22G    | L-12-H-768-A-12           | 1,172       | 91.83| 89.40 | 66.43|
|        | L-7-H-1024-A-16           | 702         | 88.61| 87.72 | 64.15|
| 10G    | L-12-H-512-A-8            | 1,172       | 89.70| 88.06 | 66.78|
|        | L-6-H-768-A-12            | 608         | 87.81| 88.02 | 63.90|
| 8G     | L-10-H-512-A-8            | 984         | 87.86| 87.52 | 63.89|
|        | L-5-H-768-A-12            | 514         | 83.85| 86.71 | 57.76|
| 6G     | L-24-H-256-A-4            | 2,300       | 88.80| 83.83 | 66.24|
|        | L-6-H-512-A-8             | 608         | 85.17| 85.82 | 61.37|
up the NAS time. Putting all together, CANAO achieves compiler-aware NAS with a fast searching process.

**Two searching phases:** Our search space includes the number of layers, hidden layer size, and intermediate embedding size of the feedforward layers. The corresponding hyperparameters will be generated by the controller during the search process. As discussed in Section [3.2], the number of layers should be determined prior to other optimizations. Thus, the controller will conduct two searching phases: 1) The determination of the number of transformer blocks; 2) The optimization of layer size. As mentioned before, appropriately increasing the number of model layers can improve model accuracy, but will saturate when it exceeds a certain limit. So, our framework can search for a desirable model that achieves a good balance between accuracy and latency, preventing from searching the architecture manually.

**Controller implementation:** Our controller is implemented as a recurrent neural network. The recurrent network can be trained with a policy gradient method to maximize the expected reward of the sampled architectures. The accuracy and latency are used as the reward signal to feedback to the controller, which is trained by using the reinforcement learning method to explore the architecture. The reward signal is calculated by taking accuracy $A$, latency $L$ as components. $rL$ is a required latency set as the threshold. The reward function is defined as follows:

$$ R = \begin{cases} \frac{r_L - L}{r_L} - 1 & L > rL \\ (A - b) + \frac{L}{rL} & L \leq rL \end{cases} $$

When $L > rL$, the performance of the resultant system cannot satisfy the timing specification. In this case, we return a negative reward to controller without training the sampled architecture. When $L \leq rL$, the latency and accuracy are summed up as the reward. $b$ is a baseline function, which is an exponential moving average of the previous architecture accuracy. The controller maximizes the expected reward by:

$$ C(\theta_c) = E_{P(a_{1:T}; \theta_c)}[R] $$

where $\theta_c$ is the parameter of the controller, $a_{1:T}$ is the list of actions that the controller predicts.

We use the REINFORCE rule to iteratively update $\theta_c$ during training (Zoph and Le 2016).

$$ \nabla_{\theta_c} C(\theta_c) = \sum_{t=1}^{T} E_P(a_{1:T}; \theta_c) \left[ \nabla_{\theta} \log P(a_t|a_{(t-1)}; \theta_c) R \right] $$

### 3.4 Compiler Optimizations

This section briefly introduces our key layer fusion compiler optimizations that optimize the latency reward for the feedback. It offers us multiple optimizing opportunities, e.g., reducing intermediate results, and eliminating unnecessary computations by analyzing the computation pattern.

**Lightweight Polynomial-based Layer Fusion (LP-Fusion)** We identify all fusion candidates in a model based on two kinds of properties in the polynomial calculation: *computation laws* (i.e., associative, commutative, and distributive) and *data access patterns*.

### 4 Experiments

**Models and datasets.** We test CANAO on three mainstream BERT models: BERT_{BASE} (Devlin et al. 2018), DistilBERT (Sanh et al. 2019), and MobileBERT (Sun et al. 2020). For pre-training, we use the same corpus as the original BERT model: BooksCorpus (Zhu et al. 2015) and English Wikipedia datasets (Devlin et al. 2018). We fine-tune the pre-trained models on GLUE benchmark (Wang et al. 2018), a comprehensive collection of natural language understanding tasks covering three NLP task categories: single-sentence tasks, paraphrase similarity matching tasks, and inference tasks. Specifically, for single-sentence tasks, we consider the Corpus of Linguistic Acceptability (CoLA) (Warstadt, Singh, and Bowman 2018). For paraphrase similarity matching tasks, we consider the Microsoft Research Paraphrase Corpus (MRPC) (Dolan and Brockett 2005) and the Semantic Textual Similarity Benchmark (STS-B) (Cer et al. 2017). For inference tasks, we consider the Recognizing Textual Entailment datasets (RTE) (Wang et al. 2018).

**Evaluation setup.** Our training is executed on GPU-AI (Bridges GPU Artificial Intelligence) nodes on the Extreme Science and Engineering Discovery Environment (XSEDE) (Towns et al. 2014). We use two node types: Volta 32 – NVIDIA DGX-2 enterprise research AI system tightly coupling 16 NVIDIA Tesla V100 (Volta) GPUs with 32 GB of GPU memory each, connected by NVLink and NVSwitch; Volta 16 – nine HPE Apollo 6500 servers, each

| Model               | MRPC | STS-B | RTE | CoLA | Latency CPU/GPU |
|---------------------|------|-------|-----|------|-----------------|
| BERT_{BASE}         | 88.9 | 85.8  | 66.4| 52.1 | 257/186         |
| DistilBERT          | 85.0 | -     | 65.5| 51.3 | 145/133         |
| MobileBERT          | 88.8 | 84.4  | 66.2| 50.5 | 73/69           |
| CANAOBERT w/o distill | 84.9 | 81.6  | 63.8| 45.7 | 60/54           |
| CANAOBERT           | 88.5 | 83.8  | 65.8| 49.7 | 60/54           |
| CANAOBERT with NAS  | 88.4 | 83.5  | 65.6| 49.2 | 49/45           |

Table 3: Evaluation results on GLUE benchmark. MRPC, STS-B, RTE, and CoLA columns show accuracy, and the last column shows inference latency on mobile CPU and GPU (with a unit of ms). All models are optimized with layer fusion and code generation (i.e., they already run faster than their TFLite implementation) with a fixed sequence length of 128. MobileBERT and CANAOBERT are trained with knowledge distillation, while CANAOBERT w/o distill. is trained directly from a deep-narrow structure.

Fig. 2 shows multiple examples we identified in BERT (these operators commonly exist in other transformer-based large models as well). Because of the large number of fusion candidates, we set two constraints: (i) only explore the opportunities offered specifically because of the above properties, and (ii) only consider two cost metrics in the fusion, which are enlarging the overall computation to improve the CPU/GPU utilization and reducing the memory access to improve the memory performance.
with 8 NVIDIA Tesla V100 GPUs with 16 GB of GPU memory each, connected by NVLink 2.0. We also use an 8 NVIDIA Quadro RTX 6000 GPU server with 24 GB of GPU memory each for training. We conduct the experiments using HuggingFace Transformer toolkit (Wolf et al. 2019).

We evaluate CANAO on a Samsung Galaxy S20 cell phone with Qualcomm Snapdragon 865 which consists of a Qualcomm Kryo 585 Octa-core CPU and a Qualcomm Adreno 650 GPU. We use a Samsung Galaxy S10 with a Qualcomm Snapdragon 855 that consists of a Kryo 485 Octa-core CPU and an Adreno 640 GPU, and an Honor Magic 2 with a Kirin 980 that consists of an ARM Octa-core CPU and a Mali-G76 GPU for portability evaluation. For each model, we run CANAO and TF Lite 100 times with 8 threads on CPU and all pipelines on GPU. Multiple runs do not vary severely, so we only report the average time for readability. We tune all runs to their best configurations, e.g., we apply the same hardware configuration for all runs, and use 16-bit float point for all GPU runs. The evaluated BERT models (including DistilBERT, BERT\textsubscript{BASE}, and MobileBERT) are trained with English Wikipedia and BooksCorpus with a fixed sequence length of 128.

### 4.2 Accuracy and Latency Results

We compare the accuracy and latency of six models: BERT\textsubscript{BASE}, MobileBERT, DistilBERT, CANAOBERT w/o distillation, CANAOBERT, and CANAOBERT with NAS. We apply layer fusion to all BERT variants to show the effectiveness of compiler-aware model optimization.

CANAOBERT w/o distillation is directly trained with a 28-transformer block deep-and-narrow structure; CANAOBERT is derived from further distilling from a teacher model. Note that CANAOBERT uses the same distillation method as MobileBERT. For CANAOBERT with NAS, 200 training epochs are used for the overall NAS. The models are evaluated on four downstream tasks: MRPC, STS-B, RTE, and CoLA. Accuracy and latency results are shown in Table 3 with the optimizations of our proposed layer fusion. We can see that CANAOBERT improves accuracy by 3-4% compared to CANAOBERT w/o distillation under the same latency. All of our three models can achieve notably lower latency compared to BERT\textsubscript{BASE}, DistilBERT, and MobileBERT.

By further applying our compiler-aware NAS, which is our CANAOBERT with NAS model, we manage to significantly reduce latency compared to BERT\textsubscript{BASE}, DistilBERT, and MobileBERT on both CPU and GPU. Compared with BERT\textsubscript{BASE}, our model is 5.2× faster on CPU and 4.1× faster on GPU with 0.5-2% accuracy loss. Compared with MobileBERT, our model is 1.49× faster on CPU and 1.53× faster on GPU with only 0.4-1% accuracy decrease.

### 4.3 Effectiveness of Compiler Optimizations

This section demonstrates the effectiveness of compiler optimizations, especially the proposed layer fusion. We compare with a state-of-the-art framework, TF Lite. The models utilized for comparison have already gone through compiler-aware NAS discussed in Section 5.3. As the models are already optimized and fixed in the comparison, we can demonstrate the efficacy of our compiler optimizations.

Table 4 shows inference latency comparison results. The
fully optimized CANAO framework can achieve up to $2.0 \times$ speedup on CPU, and $2.4 \times$ on GPU, over TFLite’s CPU execution. Notably, comparing to BERT$_{BASE}$ on TFLite, CANAO (CANAOBERT with NAS on GPU) can achieve up to $7.8 \times$ speedup. Without compiler optimizations, our baseline implementation runs slightly better than TFLite on CPU, because TFLite is already optimized for BERT models. Without compiler optimizations, GPU performance is unusually worse than CPU (only $0.6 \times$ speedup for CANAOBERT over TFLite on CPU). This is because extremely deep layers generate many intermediate data, while mobile GPU memory performs worse than CPU due to its smaller and simpler cache hierarchy. Our LP-Fusion reduces intermediate results, thus significantly improving the GPU utilization and inference performance.

We also validate LP-Fusion’s high efficacy and CANAO’s good portability. Please refer to supplementary materials.

### 5 Conclusion

This paper presents a compiler-aware neural architecture optimization framework, CANAO to search for the best BERT structure for mobile devices. CANAO guarantees the identified model to meet both resource and real-time specifications of mobile devices, achieving real-time execution of large transformer-based models (like BERT and its variants). CANAO achieves up to $7.8 \times$ speedup over TFLite. CANAOBERT model generated from the CANAO outperforms both BERT$_{BASE}$ and MobileBERT with small accuracy loss on popular NLP downstream tasks.

### Ethics Statement

CANAO is the first software solution achieving real-time execution of BERT (and its variants) on mobile devices without accuracy compromise. The ethical aspects and future societal consequences of this research are highly application-dependent. This research has several positive impacts: First, CANAO enables a wide spectrum of machine learning applications built on transformer-based self-supervised models on mobile devices that have to run on the cloud previously, such as text classification, natural language inference, question answering, etc. Second, data privacy—a key aspect of many machine learning applications has been significantly enhanced because CANAO supports model executions on the edge locally without requiring users to share their personal data with service providers. The negative consequences introduced by this research include increasing the possibility of misusing machine learning techniques due to the low-cost and easy-accessible nature of mobile AI. Furthermore, we should be cautious of AI system failures that could lead to wrong decisions, thus jeopardizing the safety of the public and individuals. All experiments in our work are based on public datasets, and our approach does not leverage biases in the data.

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