Advance in the development of wideband resistive voltage dividers

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Abstract. The advance in the development of a set of resistive dividers is described. The frequency range is 50 Hz to 100 kHz and the voltage, from 4 V to 1024 V. It was used a special design for reducing the stray capacitances and to limit the temperature, especially for the highest voltages. Tests on frequency response, ratio and phase, are shown in this paper.

Keywords. Power meter, power quality, harmonics.

1. Introduction

The objective of this work is to scale the input voltage for a wideband wattmeter, which is a joint project of the National Metrology Institutes of Brazil, Argentina and Uruguay; Instituto Nacional de Metrologia, Qualidade e Tecnologia (INMETRO) in Brazil, Instituto Nacional de Tecnologia Industrial (INTI) in Argentina, and Administración Nacional de Usinas y Trasmisiones Eléctricas (UTE) in Uruguay\textsuperscript{[1][2]}. Its goal is to construct three reference systems for measuring electric power, one for each institute, which will allow the calibration of harmonic power measuring devices. Harmonics are generated by nonlinear loads in power networks. Customer nonlinear loads, such as switched-mode power supplies, can generate harmonics up to 100 kHz\textsuperscript{[3]}. This project will contribute to provide calibration services in measuring ranges still not covered by these institutes.

UTE is in charge of the voltage dividers. The wattmeter has nine input voltage ranges, from 4 V to 1024 V, and the wattmeter digitizer requires a rated voltage of 0.8 V. So, the ratios of the voltage dividers go from 4:0.8 to 1024:0.8.

Several proposals were presented for voltage dividers\textsuperscript{[4]-[6]} but they have limited bandwidth compared to the requirement of our project, and employ complex capacitor networks for compensation systems. The progress of our design and construction of a set of resistive dividers was presented in previous papers\textsuperscript{[7][8]}. Stray capacitances and nonlinearity are the major problems in high-frequency resistive dividers. A specially designed shield was proposed to reduce the influence of both effects. It reduces the transversal electric field, reducing in this way the capacitance between the resistors and surrounding electrodes. It also reduces the dielectric losses. High electric fields through insulation material cause power losses that vary with frequency and field intensity in a nonlinear way. The components that contribute more to these losses are the dielectric materials of the resistor’s cover and
Figure 1. Resistors without cover.

The printed circuit board (PCB). To avoid this, naked resistors (Vishay Z-Foil type), as shown in Figure 1, mounted in PTFE PCB were used. In the following sections, the progress of this construction is described and test results based on the step-up method are shown.

2. Description

The basic characteristics of the dividers are shown in Table 1. The design has two arms in separated cases. The input arms have different values according to the voltage, to get a rated current of 4 mA. The output arms have appropriate values so that the output impedance is 200 Ω for all dividers. Each arm is enclosed in a cylindrical shield, which allows calibrations as a divider, with both arms connected together, or separately as single resistors. The first configuration was used for the step-up test, and the second for ac-dc tests based on thermal converters.

| Input voltage (V) | Ratio | Input resistance (kΩ) |
|-------------------|-------|-----------------------|
| 1024              | 1280  | 256                   |
| 512               | 640   | 128                   |
| 256               | 320   | 64                    |
| 128               | 160   | 32                    |
| 64                | 80    | 16                    |
| 32                | 40    | 8                     |
| 16                | 20    | 4                     |
| 8                 | 10    | 2                     |
| 4                 | 5     | 1                     |

A photograph of a complete set is shown in Figure 2. The dividers from 4-V to 32-V can be seen on the lower part of Figure 2. Due to their low power dissipation and reduced length, small cases are enough. On the contrary, in the upper part of Figure 2 (on the right side) are the three units from 64 V to 256 V, with larger cases. To reduce the temperature rise of the higher voltage dividers, the input resistor is formed by three parallel arms of ten series individual resistors. The 512-V and 1024-V units (on the left side of Figure 2), have an additional forced-air cooling system with a special design for the air flux [9].

The dividers for voltages greater than or equal to 64 V have internal shielding for reducing the influence of stray capacitances and extending the bandwidth. The main cause of errors is at the input arm because its value is much higher than the output arm. So, their stray capacitances and dielectric losses are greater. For this project, we proposed a new shielding technique for nulling radial electric
fields at the input resistor surface [10]. Two symmetrical cone-shaped electrostatic shields are installed at each end of the resistor. One cone is connected to the resistor high potential end, and the other, to ground. In this way, the displacement current though the capacitance between both cones goes from the input terminal to ground, without passing though the resistor; and few radial currents exist at the resistor surface, as shown in the electric potential and field simulation of Figure 3. Holes were done in the cones for cooling purposes (Figure 4).
3. Tests

For power applications, it is necessary to measure ratio as well as phase errors. Because of that, step-up calibration method was chosen. The 4-V divider is absolute calibrated, from 1 kHz up to 100 kHz, against a ferrite-core inductive voltage divider (IVD), and from 50 Hz to 5 kHz, against a binary inductive voltage divider (BIVD) [11]. Some frequency bandwidth can be measured by both methods. From this first step, the 8-V unit is compared to the 4-V and so on.

The high frequency IVD has a ferrite core and twelve sectors of ten turns each, with rope winding type (Figure 5, left). Ten sectors are connected in series, so that several ratios can be achieved. In particular, the ratio 5:1 corresponding to the 4-V unit can be obtained with 10 sectors at the input and 2 sectors at the output, or 5 sectors at input and 1 sector at the output. Both configurations have similar performance. This device can be self-calibrated comparing the voltage of the 11th auxiliary sector against each one of the main winding, as shown in Figure 6.

The comparator is a battery-powered digitizer [12], controlled by an algorithm based on IFFT (Interpolated Fast Fourier Transform). It computes the values of ratio and phase of both signals, and then calculates the differences between them. Everything runs on LABVIEW®. One digitizer (channel A) measures the voltage of the auxiliary sector for phase reference, and the subtraction of both channels (B-A) measures the voltage difference between each IVD sector and the auxiliary sector. An external shield acts as a guard reducing the effect of stray capacitances. It is driven by a resistive divider with the same ratios than the IVD (Figure 5, right). The LOW input of channel A is connected to the guard but, as the digitizers have independent floating inputs, this connection does not affect the LOW potential of channel B.

![Figure 5. Reference inductive divider (left) and auxiliary resistive divider (right).](image)

![Figure 6. Self-calibration circuit of the IVD.](image)
The setting 5:1 has an expanded uncertainty between $20 \times 10^{-6}$ in ratio and 20 µrad in phase shift at 10 kHz, and $60 \times 10^{-6}$ and 60 µrad at 100 kHz, as Table 2 shows. At lower frequencies the uncertainties are few parts in $10^6$ in ratio and few microradian in phase, because of the use of other 24-bit digitizer and the BIVD.

Table 2. Expanded calibration uncertainty of the IVD in the ratio 5:1.

| Frequency (kHz) | Ratio error $\times 10^{-6}$ | Phase shift (µrad) |
|-----------------|-------------------------------|-------------------|
| 10              | 20                            | 20                |
| 30              | 30                            | 30                |
| 50              | 30                            | 30                |
| 70              | 50                            | 50                |
| 100             | 60                            | 60                |

For the step-up procedure, two adjacent dividers are compared (see Figure 7). They have binary ratios, so that when the lower ratio divider has 0.8 V at its output, the other has 0.4 V. To compare them, the previously described digitizers were used, but in the ratio 2:1. The method of substitution was chosen. Channel A was used only as reference, always at the same voltage $V_a$, while channel B receives voltages $V_b$ successively, from the two dividers (UUT) to be compared. As an example, to compare the 128-V divider against the 64-V one, another auxiliary 64-V unit is used at channel A. With 64 V of the ac voltage source, when the 64-V UUT is connected, $V_a = 0.8$ V and $V_b = 0.8$ V, but with the 128-V UUT, $V_b = 0.4$ V. Subtracting both fractional measurement results, the 128-V UUT is calibrated against the 64-V one. In this way, only the linearity error in ratio 2:1 of channel B affects the measurement. All other error sources vanished. Linearity calibration of channel B was done using the previously described IVD and BIVD, and errors lower than $30 \times 10^{-6}$ in ratio and 30 µrad in phase at 100 kHz were found, with expanded uncertainty of $30 \times 10^{-6}$ in ratio and 30 µrad in phase.

Figure 7. Circuit for the step-up calibration

Up to the 64-V step, the ratio errors and phase shift were lower than the project requirements, but at the 128-V step, the phase shift increased. Table 3 shows the frequency dependence of this divider. Regarding to the ratio error, it is practically constant, so that no significant dependence on the frequency was detected. The variations are inside the uncertainty of the measurement, and the average value corresponds with the dc ratio, meaning that dielectric losses were effectively controlled. On the contrary, the variation of the phase displacement shows a typical influence of a non-compensated stray capacitance. Its linear dependence to positive values, as Figure 8 shows, is compatible with a capacitor of 0.11 pF in parallel with the input arm. The conic shields reduce the electric fields around the resistor, but these shields cannot avoid the electric filed inside the resistors. Its effect is equivalent to a parallel capacitance of 0.37 pF for each one of the 30 resistors included in the input arm. This time constant
(3.5 ns) can be compensated adding a capacitor in parallel with the output arm, or adjusting the position of the resistor inside the cone shields. Moving the resistor to the output side, the capacitance to ground is increased and the capacitance to the input potential is reduced, shifting the phase to negative values. Although both methods compensate the positive phase displacement, they also have some influence on the ratio. The capacitor can have significant dielectric losses that can produce negative ratio errors. On the other hand, moving the shield to the output side adds a second time constant that also modifies the ratio to negative values. For different dividers, different methods were chosen. Up to the 256-V unit, the adjust was made moving the resistor. For the 512-V and 1024-V, capacitors in parallel with the output arm were included. In case of the 256-V unit, the original phase displacement of 2340 µrad at 100 kHz was reduced to 30 µrad. For the 512-V and 1024-V units, the phase shifts without adjust were 7600 µrad and 27 000 µrad, respectively. Adding a capacitor to the low resistive arm, reductions around 30 times were obtained, as Table 4 shows.

Table 3. Frequency response of the 128-V divider without adjustment.

| Frequency (kHz) | Ratio error ×10^{-6} | Phase shift (µrad) |
|----------------|-------------------|------------------|
| 1              | -15               | 19               |
| 10             | -18               | 235              |
| 30             | -21               | 703              |
| 50             | -23               | 1172             |
| 70             | -19               | 1636             |
| 100            | -21               | 2340             |

![Figure 8. Phase shift of the 128-V divider without adjustment.](image)

The input capacitance of the wattmeter’s digitizer [13] connected to the divider output also produces a phase shift, because of the 200-Ω output impedance. A capacitance of 10 pF leads to an angle around 1 mrad at 100 kHz, however since it depends on the specific value of capacitance, it was proposed to correct it by software in the wattmeter calculation program. A single time constant is enough for this correction and, even with 10% of uncertainty it satisfies the project requirements. It should be noted that the current resistor-shunts [14] together with the input wattmeter capacitance also add phase displacements. In this case, the angle varies according to the shunt value leading to different time constants, which should be also corrected.
Table 4. Phase displacement at 100 kHz determined by the step-up method calibration.

| Divider | Phase shift (µrad) |
|---------|-------------------|
| 8-V     | -84               |
| 16-V    | -48               |
| 32-V    | -52               |
| 64-V    | -236              |
| 128-V   | 30                |
| 256-V   | 70                |
| 512-V   | -326              |
| 1024-V  | -577              |

The expanded uncertainties of the calibration (see Table 5) depend on several factors, but the main ones are the digitizers, the divider taken as standard in the step-up comparison (lower ratio) and the stability of the adjustment. The uncertainty of step-up procedure increases with the divider ratio, nevertheless the uncertainties obtained are adequate for the project. Below 10 kHz, the uncertainties are lower, of some parts in $10^{-5}$.

Table 5. Expanded uncertainty of the dividers calibration in ratio ($\times 10^{-6}$) and phase (µrad).

| Divider | 10 kHz | 100 kHz |
|---------|--------|---------|
| 4-V     | 36     | 67      |
| 8-V     | 47     | 73      |
| 16-V    | 56     | 79      |
| 32-V    | 63     | 85      |
| 64-V    | 70     | 90      |
| 128-V   | 76     | 95      |
| 256-V   | 82     | 99      |
| 512-V   | 87     | 300     |
| 1024-V  | 92     | 600     |

4. Conclusions
Three sets of voltage dividers with input voltages from 4 V to 1024 V and an output voltage of 0.8 V were constructed to operate up to 100 kHz. They have a simple construction and only the higher voltage dividers need some adjust. The maximum expanded uncertainty, associated with the ratio errors and phase displacement as a function of frequency are below $10^{-5}$ for the ratio, and from 67 µrad to 600 µrad for phase displacement depending on the ratio, in the whole frequency range.

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