Read/Write Margin Enhanced 10T SRAM for Low Voltage Application

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Abstract: The static random access memory (SRAM) is indispensable for high performance applications. With technology scaling, the device size as well as the operation supply voltage (VDD) is reduced. However, with the supply voltage decreasing, the performance of the conventional 6T SRAM is deteriorated seriously. In this letter, a symmetrical 10T SRAM with dramatically improved read stability and write ability is proposed. The simulation results indicate that, compared with the conventional 6T SRAM, the read static noise margin (RSNM) and write margin (WM) of the proposed 10T SRAM achieve 2.43× and 4.51× improvement, respectively, at a 0.8V supply voltage in SMIC 65 nm technology. As a result, lower failure probability in access operations is expected. Moreover, the minimum supply voltage (VDDmin) of the proposed 10T SRAM achieves ~0.32× compared with that of conventional 6T cell. Additionally, it also shows a better tolerance to the varying process variations.

Keywords: SRAM, Low voltage, SNM, VDDmin, Process variations, Failure probability

Classification: Integrated circuits

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1 Introduction

Recently, with the development of mobile internet applications, the need for embedded processor is growing. SRAM, as a critical module of it, occupies most of area, and determines main performance and power consumption [1]. Meanwhile, owing to the progress of the semiconductor techniques, the dimension of transistors as well as the supply voltage is scaling. Although supply voltage scaling has been proved to be the most effective method for energy saving [1-6], it will seriously deteriorate the read stability and write ability of the memory cell. Moreover, due to the process variations existing, the performance described above will be further deteriorated in low voltage, also in the future process nodes, which will result in the failure probability
of read or write operations increasing [2, 6-10]. Thus, the trade-off between performance and power should be considered.

The conventional 6T SRAM, as shown in Fig. 1(a), is common utilized in industrial production [6]. During a read operation, the read disturbance will occur at the node “0” due to the voltage drop between the driver transistor and access transistor [1, 6, 9-11]. An effective workaround for this problem is increasing β ratio \( \frac{W/L}{P/L} \) [12] or increasing the tipping point of the cross-couple inverters. However, this strategy will weaken the write ability. Moreover, with the effect of process variations, the robustness of SRAM cell will be exacerbated, and the \( V_{DD_{min}} \) will be further limited [1-2, 6-7, 9].

To improve the write margin and read stability for conventional 6T SRAM, different types SRAM cell topologies as well as assist circuit has been proposed [1-3, 6-13]. Decoupling the storage nodes with bit-line or lowering the voltage drop between the driver and access transistors is the efficient way to enhance read stability [11]. And, cutting the feedback loop, boosting word-line (WL) voltage and decreasing the supply voltage of cross-couple inverters can increase write margins[1,3-4, 13]. However, the previous techniques only improve one of the write margin and read stability, or the single-port, read/write, them generally degrade the speed of operation and makes the sense amplifier faced a challenge [1, 3, 6, 12-13]. Moreover, considering the stability for unselected cells, the techniques, WL voltage boosted or feedback cut, are unfit. Additional, extra complicated assist circuits will increase the difficulty for SRAM design [8].

In this letter, a novel symmetrical 10T SRAM cell is proposed to improve write margin and read stability simultaneously. During the read operation, the connecting transistors, between driver and pull-up transistors, will be working in the near-threshold region after discharging of the bit-line. Therefore, the disturbance on storage node “0” will be suppressed. And, during the write operation, the voltage of bit-lines can provide the working voltage of the cross-couple inverters by the switching transistors [2]. It weakens the trip-point of one side inverter. As a result, the write ability will be significantly enhanced. Additionally, the proposed 10T SRAM can work at a lower \( V_{DD_{min}} \) compared with the conventional 6T SRAM.

The remainder of this letter is constructed as follows. The proposed 10T SRAM is presented in section 2. And, the analysis and comparison of the proposed and related SRAMs based on the simulation results are given in section 3. In the end, the conclusion of this paper is given in section 4.

2 The design of the proposed 10T SRAM

The diagram of the proposed 10T SRAM is shown in Fig. 1(b). Two connecting-PMOSs, PCL and PCR, are added between pull-up and driver transistors [11]. And, two switching-PMOSs, PSL and PSR, are placed between the bit-lines and pull-up transistors. Furthermore, the additional PMOSs are controlled by the other word-line signal, AWL. Table. I gives the level of key signals for different operation, and, L and H present the low and
During the standby, WL and AWL are kept low logic level, the connecting-PMOSs and switching-PMOSs are activated. Thus, the cells are powered by the bit-lines. Under this condition, the stability of the proposed 10T SRAM resembles that of the conventional 6T SRAM. During the access operation, the WL and AWL are set to high and low logic level, respectively, for the row selected cell. Contrary, for the row unselected cell, the WL and AWL are set to low and high logic level, respectively.

Fig. 1. Schemes and waveform, (a) Conventional 6T, (b) Proposed 10T, and (c) DC sweep waveform.

Table I. Signals of the proposed 10T SRAM cell under different operations.

| Operation      | Standby | Read | Write |
|----------------|---------|------|-------|
| Signal         | WL | AWL | WL | AWL | WL | AWL |
| Row-selected   | L  | L   | H  | L   | H  | L   |
| Row-unselected | L  | L   | L  | H   | L  | H   |

During a read operation, both BL and BLB are pre-charged to high logic level initially. Assuming that the storage node Q and QB of the selected cell are low and high logic level, respectively, the BL will be discharged though PGL, PCL and PDL when WL and AWL are activated. Due to the PCL existing, when the q node is discharged to near the threshold voltage of it, it will work in the near-threshold region. As a result, the storage node, Q, will be isolated from BL, and will almost keep low logic level state, as shown in Fig. 1(c). Thus, the proposed 10T SRAM can avoid the read disturbance effectively.

Assuming that the storage node Q and QB of the selected cell are high and low logic level, respectively, the BL and BLB are pre-set to low and high logic level initially for a write operation. When WL and AWL are activated, because of the left inverter powered by the BL, the PUL is hard to maintain the high logic level for the nodes, q and Q. Moreover, the trip point of the left inverter (invL) is decreased and the right inverter (invR) is kept unchanged, which is effective to improve the write ability.
Additionally, during a write operation, the row half-selected cells keep a fake read operation. As mentioned above, they are more reliable than the conventional 6T SRAM due to the high ability against the read disturbance. Moreover, for the column half-selected cells, the AWL is temporarily set to high logic level. Although, the cross-couple inverters are temporarily floating, the storage nodes are further isolated by the conducting-PMOSs. Thus, it relieves the influences from the leakage current. As a result, the proposed 10T is more reliable than the conventional 6T SRAM, as well as the 8T SRAM proposed in [2].

3 Characterization based on the simulation

To present the superiority of the proposed 10T, the stability, process variation tolerance, error rate, $V_{DD_{min}}$ and operation speed are characterized, compared with the conventional 6T, 8T in [2] and 8T in [11] cell. Considering the fairness of comparison, the access, pull-up and driver transistors have the same dimension for cells, respectively, in different schemes as Table.II shown.

| Device     | Conv 6T (W/L)   | Prop 10T (W/L)  |
|------------|-----------------|-----------------|
| Pull-up    | 120nm/65nm      | 120nm/65nm      |
| Access     | 120nm/75nm      | 120nm/75nm      |
| Driver     | 135nm/65nm      | 135nm/65nm      |
| Switching  |                | 120nm/65nm      |
| Connecting |                | 120nm/65nm      |

Fig. 2. Simulation results of HSNM, (a) VTCs of different cells at 0.8V VDD, and (b) HSNMs versus VDD.

According to [14], the stability of SRAM cell is determined by the static noise margin (SNM), which is defined as the maximal tolerated voltage noise before the states of SRAM cell changing, and estimated by butterfly curves. During the standby, hold SNM (HSNM) of different cells is shown in Fig.
2(a). As it shown, the HSNMs of the different cells are similarly about 0.320V under the condition of 0.8V supply voltage, 125°C and SS corner. Moreover, the HSNM is decreasing with supply voltage changing from 1.2V to 0.2V, as Fig. 2(b) shown.

During the read operation, the read SNM (RSNM) of different cells is presented in Fig. 3(a). In the proposed 10T SRAM, one of the connecting-PMOSs will work in the near-threshold region when the voltage of its source is small enough as mentioned above. As a result, the disturbance on the low logic storage node of the proposed 10T SRAM is significantly smaller than that of the other referenced cells. And, simulation results show that, the RSNM of the proposed 10T SRAM is 301mV, which is 2.43× as that of conventional 6T SRAM. Moreover, as Fig. 3(b) shown, the RNSM of the proposed 10T SRAM will get 2.51 and 6.03 times compared that of conventional 6T SRAM at 1.2V and 0.3V supply voltage, respectively. Thus, it indicates a better tolerance of the read disturbance, especially at a low supply voltage.

The write SNM (WSNM) as a criterion is common used to measuring
write margin (WM), lower WSNM indicates poorer write ability. Considering the structure of the proposed 10T SRAM, the BL voltage, which will result in Q and QB flip, is used as a criterion of WM [15]. As Fig. 4(a) shows, under the condition of 25°C and SF corner, the WM of different cells is reducing with the scaling of supply voltage, and the WM of the proposed 10T cell achieves 2.35× and 12.52× improvement at 1.2V and 0.6V supply voltage, respectively, compared with that of conventional 6T cell. Thus, the stronger ability for write operation of the proposed 10T SRAM is presented, especially at a low voltage.

Additionally, during access operation, the row half-selected cells remain a pseudo read operation. Thus, RSNM will be as a metric to evaluate the stability of them [2]. Fig. 4(b) gives the 1000 times Monte Carlo (MC) simulations under 25°C and FS corner, compared with conventional 6T cell, the average RSNM of the proposed 10T cell gets 2.60× and 4.09× improvement at 1.2V and 0.3V supply voltage, respectively. That is to say the immunity of disturbance for the row half-selected cell used proposed 10T cell is better than that used conventional 6T cell.

Table III. Comparisons of WM and RSNM with different corners. (A: Conv 6T; B: Prop 10T)

| Corner | WM (mV) | RSNM (mV) |
|--------|---------|-----------|
|        | TT      | FF        | SS   | FS   | SF   | TT      | FF        | SS   | FS   | SF   |
| WM (mV)| A       | 302.6     | 330.7 | 274.6| 412.5| 186.1   | B       | 502.0     | 498.6| 503.7| 436.6| 584.2 |
|        | Ratio   | B/A       | 1.659| 1.508| 1.834| 1.058   | 3.139   |
| RSNM (mV)| A     | 190.2     | 170.4 | 203.8| 139.4| 232.5   | B       | 395.9     | 356.2| 424.3| 360.4| 386.4 |
|        | Ratio   | B/A       | 2.081| 2.090| 2.082| 2.585   | 1.662   |

Fig. 5. Comparisons of DRT versus different voltages for the column half-selected cell during write operation.
Moreover, during access operation, the high logic store nodes of the column half-selected cells remain floating. As a result, the data will be upset due to the discharging, especially at a write operation. Thus, the date retention time (DRT) during floating period is critical for stability. Fig. 5 gives the comparison of the DRT between the 8T cell in [2] and the proposed 10T cell. As shown, the mean and minimum of DRT of the proposed cell are 51.57 s and 6.53 s, which are \( \times1.5 \times \) and \( \times1.0 \times \) compared with those of 8T cell in [2] at 0.5 V, respectively. Moreover, the maximum write time of the proposed 10T cell obtained by the 1000 times MC simulations is 35.3 ns. And, assume that the floating time need for the unselected cell on the same column is the same as the maximum write time. Nonetheless, the DRT of the proposed 10T cell is far larger than the floating time during a write operation. Hence, the floating mechanism has not significant influence for the data-hold stability.

Beyond stability, the tolerance of process variation is also an important criterion for the SRAM design [1]. Fig. 6 gives the 1000 times MC simulations under different cases for different operation, (a) SS for standby, (b) FS for read and (c) SF for write, respectively, at 1.0 V supply voltage and 25°C. The similar mean \( (\mu) \), standard deviation \( (\sigma) \) and \( \mu/\sigma \) of HSNM among different SRAM cells imply similar stability during standby, as Fig. 6(a)
shown. Accordingly, as Fig. 6(b) shown, those of the RSNM for the proposed 10T cell achieve 2.59×, 0.69× and 3.77×, respectively, compared with those of conventional 6T cell. Additionally, those of WM achieve 3.14×, 0.58× and 5.43×, respectively, as Fig. 6(c) shown. Furthermore, as Table. III shown, the variations of RSNM and WM between extreme corners are 68.1mV [i.e. (424.3-356.2)mV] and 147.6mV [i.e. (584.2-436.6)mV] in proposed 10T cell compared to 93.1mV [i.e. (232.5-139.4)mV] and 226.4mV [i.e. (412.5-186.1)mV] in conventional 6T cell. Therefore, it is shown that the proposed 10T SRAM shows better process variation tolerance.

![Fig. 7.](image)

**Fig. 7.** Comparisons of failure probability versus VDD, (a) Read failure, and (b) Write failure.

| Table IV. | VDD$_{\text{min}}$ of different cells. (A:Conv 6T; B:8T in [2]; C:8T in [11]; D:Prop 10T) |
|-----------|----------------------------------|
|           | A                      | B        | C        | D        | D/A       |
| VDD$_{\text{read min}}$(V) | 1.027                  | 1.007      | 0.371   | 0.370    | 36.03%    |
| VDD$_{\text{write min}}$(V) | 1.166                  | ↓0.200     | ↑1.200   | ↓0.200   | ↓17.15%   |
| VDD$_{\text{min}}$(V) | 1.166                  | 1.007      | ↑1.200   | 0.370    | 31.73%    |

As mentioned above, the stability is decreased with scaling supply voltage. Thus, the failure rate is closely related to the supply voltage. The failure rate is expressed as $P_{\text{Fail}}$. For standby and read operation, the $P_{\text{Fail}}$ is determined by the SNM<$V_{\text{Thermal}}$, where the $V_{\text{Thermal}}$ is the thermal voltage which is 26mV at normal temperature, and for write operation, the $P_{\text{Fail}}$ is determined by the WM<$0 [1, 6, 7, 9]. Due to retention stability is typically stronger compared to read data stability [6], this paper just concerns the read and write operation. Fig. 7 is the failure probabilities versus supply voltage. As can be seen, the read as well as write failure probability of the proposed 10T cell is orders of magnitude smaller compared that of conventional 6T cell. In addition, according to [1,6,7,9], the VDD$_{\text{min}}$ is defined as the minimum supply voltage at which the target yield can be achieved, and determined by max{$VDD_{\text{hold min}},VDD_{\text{read min}},VDD_{\text{write min}}$}, where
the VDD\textsubscript{hold\_min}, VDD\textsubscript{read\_min}, and VDD\textsubscript{write\_min} are the minimum VDD in standby, read, and write operation, respectively. Additionally, due to VDD\textsubscript{hold\_min} is much lower than VDD\textsubscript{read\_min} and VDD\textsubscript{write\_min} \cite{6}, the Table IV gives the VDD\textsubscript{min} of different SRAM cells determined by VDD\textsubscript{read\_min} and VDD\textsubscript{write\_min}, assuming the P\textsubscript{Fail\_is} is 10^{-5}. As shown, the VDD\textsubscript{min} of proposed 10T cell is the lowest one, and achieves \sim 0.32x compared that of conventional 6T cell. Although, the cell in \cite{11} and in \cite{2} have an aggressive VDD\textsubscript{read\_min} and VDD\textsubscript{write\_min}, respectively, the proposed 10T cell is more competitive in ultra low voltage.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{fig8.png}
\caption{Transient waveforms at 1.2V voltage, (a) Read operation, and (b) Write operation.}
\end{figure}

\begin{table}[h]
\centering
\caption{Read delay with 100mV difference at different voltages. (A:8T in \cite{11}; B:Prop 10T (ZWL=0V); C:Prop 10T (ZWL=-0.3V)}
\label{tab:VReadDelay}
\begin{tabular}{cccccc}
\hline
VDD (V) & A (ns) & B (ns) & C (ns) & C/A & C/B \\
\hline
1.2 & 1.423 & 1.436 & 0.423 & 0.297 & 0.295 \\
1.1 & 2.626 & 2.650 & 0.599 & 0.228 & 0.226 \\
1.0 & 5.583 & 5.632 & 0.907 & 0.162 & 0.161 \\
0.9 & 14.084 & 14.201 & 1.490 & 0.106 & 0.105 \\
0.8 & 42.201 & 42.572 & 2.724 & 0.065 & 0.064 \\
\hline
\end{tabular}
\end{table}

Lastly, due to the trade-off existing between the speed and margin, the speed of proposed 10 cell is deteriorated compared with conventional 6T cell. Nonetheless, with almost the same read speed, the write speed of proposed 10T cell is better than that of 8T in \cite{11}, as Fig. 8 shown. Additionally, for speed considering, the negative voltage of ZWL signal can be used. As Table V shown, when the ZWL is -0.3V, the read speed of proposed 10T can be improved significantly, with voltage scaling.

\section{Conclusion}

In this paper, a novel 10T SRAM cell with read/write margin enhanced is proposed for ultra low supply voltage. Simulation results show that the
proposed 10T achieves $2.43 \times$ read stability and $4.51 \times$ write ability compared that of conventional 6T cell at 0.8V supply voltage. Meanwhile, it is shown that the proposed 10T cell has better process variation tolerance as well as more competitive supply voltage range.

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