Two-step switching scheme for SAR ADC with high energy efficiency

Chenggao Zhang¹ · Shubin Liu¹ · Zhangming Zhu¹

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Abstract

The paper presents two high energy-efficiency switching schemes for the successive approximation register (SAR) analogue-to-digital converter (ADC). The first scheme is a part of the second one. The new switching schemes achieves no switching energy consumption in the first three comparison, and need no reset energy. Thus, compared with the conventional SAR architecture, 99.23 and 99.42% reduction in switching energy is achieved respectively. Moreover, the total scheme achieves an 86.7% reduction in unit capacitor number by its special architecture.

Keywords SAR ADC · Energy-efficiency switching scheme · Reset energy · Capacitor saving

1 Introduction

Successive approximation register (SAR) analogue-to-digital converter (ADC) is a popular candidate for medium-precision and medium-speed ADC used in wireless sensor networks and medical instrumentation applications. Compared with other kinds of ADCs, it has advantages such as high-energy efficiency, switching feature and being amenable to CMOS process scaling. In SAR ADC with capacitor DACs, the energy consumption during the capacitor switching plays a leading role in the overall power consumption. Therefore, a variety of switching schemes have been proposed to reduce the power consumption [1–5]. The tri-level switching scheme [1], monotonic scheme [2], modified merged capacitor switching (MCS) scheme [3] and novel energy-efficient capacitor switching scheme [4] achieve 81.2, 87.5, 93.7 and 98.8% reductions in average switching energy, respectively, compared with the conventional conversion scheme [2]. However, in some presented switching scheme, the reset energy is nonnegligible, even higher than the switching energy (Fig. 4(5)). Thus, it is indispensable to take both the switching energy and the reset energy into consideration.

In this letter, a new two-step switching scheme is proposed, while its first step switching scheme can also be an energy-efficient switching scheme solely. The proposed two-step scheme and its first step scheme achieve 99.42 and 99.23% reduction in average switching energy, respectively, and have no reset energy consumption. Moreover, 86.7 and 75% reduction in unit capacitor number over the conventional scheme are also achieved.

2 Energy analyses

For most of the switching energy is consumed in the first several bit cycles, it is a key point to reduce the switching energy of the first several bit cycles to zero. Analyze the switching energy as follows:

In every bit cycle, the bottom voltage of some capacitors is changed, while the others remain unchanged. The switching energy of these two kinds of capacitors is

\[ E_i = V_i C_i [(V_i - V_y) - (V_i - V_x)] \]  

\[ E_j = V_{ij} C_j [(V_{ij} - V_y) - (V_{ij} - V_x)] \]

The subscript “i” represents the quantities of the unchanged capacitors, while “j” represents the changed capacitors. The subscript “y” represents the quantities after the switching, and “x” represents the quantities before the switching.
Given:

\[ V_y - V_x = \sum_{j} \frac{C_j \Delta V_j}{C_{\text{tot}}} \] (3)

In most instances, the voltage change quantity on the bottom plate of every \( C_j \) is the same, so:

\[ \Delta V = \Delta V_j \] (4)
\[ k = \sum_{j} \frac{C_j}{C_{\text{tot}}} \] (5)
\[ E_i = -kV_iC_i \Delta V \] (6)
\[ E_j = V_{sj}C_j \Delta V(1 - k) \] (7)
\[ E = \sum_{i} E_i + \sum_{j} E_j \] (8)
\[ E = \Delta V \left( \sum_{j} V_{sj}C_j(1 - k) - \sum_{i} V_iC_i k \right) \] (9)

There are several ways to let \( E = 0 \).

### 2.1 The first way

If the bottom plates of all the capacitors are set to the same voltage (for any \( i, j \); \( V_i = V_{sj} \)):

\[ E = V_i \Delta V \left( \sum_{j} C_j(1 - k) - \sum_{i} C_i k \right) \] (10)
\[ \sum_{i} C_i k = \sum_{i} C_i \sum_{j} \frac{C_j}{C_{\text{tot}}} = \frac{1}{C_{\text{tot}}} \sum_{i} C_i \sum_{j} C_j \] (11)
\[ \sum_{j} C_j(1 - k) = \sum_{j} C_j \sum_{i} \frac{C_i}{C_{\text{tot}}} = \frac{1}{C_{\text{tot}}} \sum_{i} C_i \sum_{j} C_j = \sum_{i} C_i k \] (12)

Plug (11), (12) into (10):

\[ E = 0 \]

### 2.2 The second way

If the bottom plate voltage of all the capacitors are changed and changed in the same quantity (\( \sum_{j} C_j = C_{\text{tot}}, \sum_{i} C_i = 0, \ k = 1 \)). It is easy to get \( E = 0 \).

### 2.3 The third way

If:

\[ \sum_{j} V_{sj}C_j(1 - k) = \sum_{i} V_iC_i k \] (13)

It is easy to get \( E = 0 \), but it is difficult to find a special voltage distribution [6].

### 2.4 The fourth way

In some cases, we can get a negative \( E \), so it’s seems that the zero switching energy consumption can be achieved by \( E_P + E_N = 0 \) (\( E_P \) is the energy consumption of P-DAC, and \( E_N \) is the energy consumption of N-DAC). But, a special voltage distribution should be applied [6].

### 3 Proposed switching scheme

Figure 1 shows the proposed switching scheme of an 8-bit SAR ADC. The scheme adopts a two-step architecture that each step decides 4 bits.

#### 3.1 The first step

The first part of the proposed architecture is equivalent to an independent 4-bit SAR ADC as shown in Fig. 2. The MSB capacitor 2C split into two capacitor (C, C) because of the MSB-split structure. In the end of the sampling phase, the input singles are sampled onto the top plates of the DAC, while the bottom plates of LSB sub-arrays are set to GND, and the MSB sub-arrays are set to \( V_{cm} \), where \( V_{cm} \) equals to half of the voltage reference \( V_{\text{ref}} \). ‘1’, ‘1/2’ and ‘0’ represent the voltage reference \( V_{\text{ref}}, V_{cm}, \) and ground (GND). After sampling, we can get the MSB (D1) directly by comparing the inputs without any switching. Based on the MSB (D1), the voltage of all the bottom-plates of the lower input referred capacitor array are increased by \( V_{cm} \), being changed to [\( V_{\text{ref}}, V_{\text{ref}}, V_{cm}, V_{cm} \)]. The other capacitor array remain unchanged. Thus, the MSB-1(D2) is obtained, and no switching energy is consumed in this operation due...
to “the first way”. During the third bit cycle, if D2 and D1 are not equal, the side with \([V_{cm}, V_{cm}, GND, GND]\) is changed to \([V_{cm}, V_{cm}, V_{cm}, V_{cm}]\), while the other side remain unchanged. If D2 is equal to D1, the side with \([V_{cm}, V_{cm}, GND, GND]\) is changed to \([GND, GND, GND, GND]\). Due to “the second way”, this operation consumes zero switching energy. So far, there is no switching energy consumption in the first three bit-cycles with the proposed scheme.

In the following bit cycles, a single-side switching method is applied. As shown in Fig. 1, the side with \([V_{cm}, V_{cm}, V_{cm}, V_{cm}]\) or \([GND, GND, GND, GND]\) is always unchanged, and the other side capacitor array switch with only two reference voltages, following the scheme proposed by [3].

### 3.2 The second step

During the first step, after the first two switching cycles, only one of the two capacitor DACs keep working in the rest bit cycles, and the other one always remain unchanged. Based on this factor, a new scheme is proposed, as shown in Fig. 3, to reduce the number of unit capacitor. The second part capacitor array includes a 4-bit MSB-split capacitor array and a redundant capacitor \(C_{rest}\). During the first step, all the plates of the second part capacitor array
are set to $V_{cm}$. When the first step is complete, connect the second part capacitor array with the DAC that worked in the first step, turn off $S1$, $S2$, $S3$ and turn on $S4$, as shown in Fig. 3 for example. Then, we can get the last 4 bits by the scheme proposed by [3]. The number of Crest can be get by the following equations [7].

$$C_{tot} = C_{rest} + C_{MSB} + C_{LSB}$$  \hspace{1cm} (14)

$$\frac{1}{2} V_{ref} \frac{C_{MSB}}{C_{tot}} = \frac{1}{2^{N/2}} V_{ref}$$  \hspace{1cm} (15)

$$C_{MSB} = C_{LSB}$$  \hspace{1cm} (16)

$$\frac{1}{2} V_{ref} \frac{C}{C_{tot}} = \frac{1}{2^{N-1}} V_{ref}$$  \hspace{1cm} (17)

C is the unit capacitor; N is the total bit of the ADC.

Compared with the symmetrical architecture, the proposed one only need one capacitor-based DAC in the second part, which achieves nearly 50% reduction in the unit capacitor number. S1–S5 will affect the accuracy of the ADC in two respects.

The first respect, the switch is made up of MOSFET, so it’s inevitable to introduce stray capacitance in the DAC, and effect the upper plate voltage of the capacitor array DAC.

$$\Delta V_{DAC1_{real}} = \Delta V_{DAC1} \frac{1}{1 + (C_{S5} + C_{S1})/C_{all1}}$$  \hspace{1cm} (18)

$$\Delta V_{DAC2_{real}} = \Delta V_{DAC2} \frac{1}{1 + (C_{S3} + C_{S4})/C_{all2}}$$  \hspace{1cm} (19)

$\Delta V_{DAC1_{real}}$ and $\Delta V_{DAC2_{real}}$ are the real upper plate voltage change of the capacitor array DAC, and $\Delta V_{DAC1}$, $\Delta V_{DAC1}$ are the theoretical value. $C_{Sx}$ is the stray capacitance of switch. $C_{all}$ is the total capacitance of the capacitor array. In the second step, both plates of C1 are floating, so the effect on C1 can be ignored. Minish the array of the switching tube can decrease the stray
capacitance. If necessary, a digital calibration could be introduced.

The second respect, when the switches move, the leak current will affect the DAC’s voltage. Using the transmission gate with both N-MOS and P-MOS and choosing a reasonable aspect ratio could minimize the leak current.

4 Reset energy

After the second step, the first and second part capacitor array is separated by turning off S4. It consume no energy to reset all the bottom plates of the second part capacitor array to $V_{cm}$ due to “the first way”. However, it will result in a huge energy consumption if we reset the first part capacitor array to the original state in the next moment. To reduce the reset energy, we use a scheme shown in Fig. 4. Figure 4(1) shows a capacitor array of the first part, which
we cannot make sure the voltage distribution on its bottom plates. Turn off S5 and all the switches between the bottom plates and the reference voltage, and short the MSB and LSB respectively [8]. Then, the MSB is changed to $V_{cm}$ while the LSB is changed to Gnd. Due to “the second way”, this operation draw no energy from the reference voltage. Next, the MSB and LSB sample the input respectively. When the sampling is finished, S5 is turned on, and a new SAR cycle begins. Since both the up-plate voltage of the MSB and LSB is $V_{in}$, there is no charge redistribution in this operation, which means there is no energy consumption. From the above, the reset energy is reduced to zero theoretically.

5 Simulation

The behavioural simulations for the case of 10 bit ADC were performed in MATLAB to compare the two proposed schemes with several existing ones. A comparison of average energy consumption is shown in Fig. 5 and 6 and summarized in Table 1. Without consideration of the PART 2, the average switching energy of a 10 bit SAR ADC with the switching scheme proposed in PART 1 is 10.54$CV_{ref}^2$, which achieves a 99.23% reduction over the conventional architecture. When both the two proposed parts are applied, the average switching energy is only 7.91$CV_{ref}^2$. Besides the switching energy saving, both the two proposed scheme have no reset energy while (Fig. 4(5)) consume a huge energy in resetting. In the respect of unit capacitor saving, the number of unit capacitor used in the two proposed scheme is 512 and 272 respectively, which is 4096 in the conventional architecture, achieving 75 and 86.7% reduction.

6 Conclusion

Two energy-efficient and area-efficient switching scheme is presented in this paper. The switching energy is reduced by 99.23 and 99.42% respectively, while no reset energy is consumed. The number of unit capacitor is reduced by 75 and 86.7%. Therefore, it is applicable to use the proposed schemes in the biomedical area.

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References

1. Yuan, C., & Lam, Y. (2012). Low-energy and area-efficient tri-level switching scheme for SAR ADC. *Electronics Letters*, 48(9), 482–483.
2. Liu, C.-C., Chang, S.-J., Huang, G.-Y., & Lin, Y.-Z. (2010). A 10 bit 50 MS/s SAR ADC with a monotonic capacitor switching procedure. *IEEE Journal of Solid-State Circuits*, 45(4), 731–740.
3. Zhu, Z., Xiao, Y., & Song, X. (2013). Vcm-based monotonic capacitor switching scheme for SAR ADC. *Electronics Letters*, 49(5), 327–329.
4. Tong, X., & Zhang, Y. (2015). 98.8% switching energy reduction in SAR ADC for bioelectronics application. *Electronics Letters*, 51(14), 1052–1054.
5. Huang, G.-Y., Chang, S.-J., Liu, C. C., & Lin, Y.-Z. (2013). 10-bit 30-MS/s SAR ADC using a switchback switching method. *IEEE Transactions on Very Large Scale Integration Systems*, 21(3), 584–588.
6. Osipovl, Dmitry, & Paull, Steffen. (2016). Two advanced energy-back SAR ADC architectures with 99.21 and 99.37% reduction in switching energy. *Analog Integrated Circuits and Signal Processing*, 87(1), 925–1030.
7. Gao, Ji, Guo, Wei, & Zhu, Zhangming. (2016). Energy-efficient common-mode voltage switching scheme for SAR ADCs. *Analog Integrated Circuits and Signal Processing*, 89, 499–506.
8. Liu, S., Shen, Y., & Zhu, Z. (2016). A 12-bit 10 MS/s SAR ADC with high linearity and energy-efficient switching. *IEEE Transactions on Circuits and Systems I-Regular Papers, 63*(10), 1616–1627.

9. Zhu, Z.-M., & Liang, Y.-H. (2015). A 0.6-V 38-nW 9.4-ENOB 20-kS/s SAR ADC in 0.18-CMOS for medical implant devices. *IEEE Transactions on Circuits and Systems I-Regular Papers, 62*(9), 2167–2176.

10. Zhu, Y., Chan, C.-H., Chio, U.-F., et al. (2010). A 10-bit 100-MS/s reference free SAR ADC in 90 nm CMOS. *IEEE Journal of Solid-State Circuits, 45*(6), 1111–1121.

Chenggao Zhang now is currently working toward the Ph.D. degree at the school of microelectronics, Xidian University, Xi’an, China. His research interests include nanoscale CMOS ADC and low power analog front end (AFE) integrated circuits design.

Shubin Liu received the B.S. and Ph.D. degree in microelectronics from Xidian University, Xi’an, China, in 2007 and 2014. His current interests include high-resolution high-speed data converters, SAR ADC and mixed-signal VLSIs.

Zhangming Zhu received the M.S. and Ph.D. degree in microelectronics from Xidian University, Xi’an, People’s Republic of China, in 2001 and 2004, respectively. He is currently a professor with the school of microelectronics, Xidian University, Xi’an, China. His research interests include CMOS data converters and AFE, low power mixed-signal integrated circuits design, green-power ICs, and 3D-ICs based TSV.