Design and Implementation of Hybrid Asymmetric 15-Level Cascaded Modified H-Bridge Multilevel Inverter (CMHB-MLI) to reduce the Total Harmonics Distortion

K B Bhaskar¹ A Vijayaprabhu² R Kumaresan³ E Kokila⁴
¹,³,⁴Department of Electrical and Electronics Engineering, Adhi College of Engineering and Technology, India
²Assistant Professor, Department of Electronics and Communication, Sri Venkateswara College of Engineering and Technology, India

jaibhaskar15@gmail.com¹, Vijayabrabhu85@gmail.com²

Abstract. This new cascaded modified H-bridge asymmetrical multilevel inverter (CMHB-MLI) module proposes a 15 levels with three unequal dc sources and 10 switches. The design approaches with preferable advantage with greater quality comparatively to similar modules with minimum number of semiconductor switches utilizing lower switching frequency and less dc sources. Opposite phase disposition pulse width modulation (OPD-PWM) switching technique is utilized for controlling the Semiconductor switches in CMHB-MLI. In asymmetrical topology the input source are designed with unequal magnitude is done deliberately with binary nature of voltages such as 10Vdc, 20Vdc and 40Vdc. In asymmetrical designing of MLI produces a number of different output levels with the similar number of power semiconductor switches. The results are designed using MATLAB and hardware implementation validates improved quality performance with lower total harmonics distortion without utilizing any filtering circuit in the output with reduced switching stress.

Key words – Asymmetric, Hybrid, CMHB-MLI, opposite phase disposition pulse width modulation (OPD-PWM), Total harmonic distortion.

1. Introduction
In the past decades, multilevel inverters had a great attention towards cost effective systems with wider range of applications mainly in the areas of power quality improvement devices, flexible AC transmission systems, larger motor drives and green energy converters[1]–[3]. The anxiety to ozone layer depletion caused by burning of fossil fuels for electricity generation leads to usage of natural available green resources such as photovoltaic, wind, geothermal etc., to improve the efficiency of the system and cost cutting a power electronic conversion switching technology is a valid requirement towards power generation from solar and wind[4]–[6].

Compared to the conventional inverter, MLIs have numerous advantages that produces common mode voltage with reducing switching stress by drawing lowering input current with low distortion, MLIs can operate at lower switching frequencies and achieves higher efficiency with lower
switching stress[7], [8], By proper PWM technique selective harmonics can be eliminated which can be resulted in lower total harmonic distortion in the output waveforms without usage of any filter[9]–[12].

In general, the MLI are classified as Neutral point diode clamped (NPDC), Flying capacitor (FC) and Cascaded H-Bridge (CHB). In NPDC multilevel inverter makes use of diodes which transfers minimum amount of voltage leads to drawback of producing a maximum output voltage is half of the input voltage[13]–[16]. In FC multilevel inverter approaches to more number of capacitors are connected in series which causes switching redundancy impact to reduction in voltage level and voltage balancing is difficult thereby produces half output compared to the input voltage[17]–[19]. CHB multilevel inverter avoiding usage of bulky transformer, clamping diodes and capacitor which required in NPDC and FC and each cell in an H-bridge produces three different voltages like zero, positive DC and Negative DC voltages, the main advantage of multilevel inverteris that it requires less components[20]–[23].

Making concern of the vital factor of MLI design approach for high voltage applications will generate increased stress on output H-bridge therefore it is necessary to build a new topology which will make stress even to all the switches[24]–[27].

The proposed asymmetric CMHB-MLI aims to achieve lowering switching stress to the switches by designing a proper pulse dispositioning scheme and achieves lower total harmonics distortion with greater efficiency at the output voltage level and cost efficient, and also targeted to produce 15 level with less number of switches.

The paper proceeds with, section II describes the symmetrical and asymmetrical cascaded H Bridge multilevel inverter and analysis of conduction and switching losses, section III elaborates the proposed CMHB-MLI circuit description with switching state analysis with the analysis of operating modes of converter, section IV validates the simulation and hardware results and section V concludes the proposed CMHB-MLI continued with the references.

2. Symmetrical and Asymmetrical Cascaded H Bridge Multilevel Inverter
In symmetrical MLI with ‘n’ equal dc voltage offer $2n+1$ distinct voltage level at the phase output. Since the required number of devices depends on output voltage level, the problem such as increasing inverter size, cost, and installation area and control complexity should be avoided.

To overcome the above mentioned problem an asymmetrical MLI is approached for providing a large number of output voltage levels without increasing the number of bridges, a method of choosing non identical DC input sources is referred as binary configuration. The topology can achieve $2^{n+1}-1$ distinct voltage levels with ‘n’ cascaded H-bridges, this approach gets better performance in terms of levels than symmetrical MLI topology with the same number of switching components and DC buses. However, high variability in the consequent DC voltage magnitudes leads to charge balance problem as well as the higher voltage stress. The general representation for Asymmetrical model as,
2.1 Conduction loss

Usually losses will be calculated in two types conduction and switching loss. First conduction loss, developed to multilevel inverter is the instantaneous conduction losses of a transistor, the losses that occur during the power device is the on-state and conducting current, therefore, power dissipation during conduction is computed by multiplying on state saturation voltage and on state saturation current and it is given as.

\[ p(t) = V(t) \times I(t) \]  \hspace{1cm} (1)

In the equation 1, \( V(t) \) represents on state saturation voltage and \( I(t) \) is the load current, and the instantaneous conduction losses of semiconductor switches \( P_{cs}(t) \) is given in equation 2.

\[ P_{cs}(t) = [V_s + R_s i^{\beta(t)}] i(t) \]  \hspace{1cm} (2)

The average conduction loss of main circuit is represented in equation 3 as,

\[ P_{c,Mc} = \frac{1}{\pi} \int_{0}^{\pi} [N_s(t) + P_{cs}(t)] d\omega(t) \]  \hspace{1cm} (3)

The output current of auxiliary circuit to be sinusoidal as \( i(t) = I_m \sin \omega t \) and conduction losses of auxiliary circuit can be calculated as below.

\[ P_{c,A} = \frac{1}{\pi} \int_{0}^{\pi} [x(t)V_{\omega,j} + x(t)R_{\omega,j} i(t)] i(t) d\omega t \]

\[ = \frac{1}{\pi} \int_{0}^{\pi} 2P_{cs}(t) d\omega t \]

\[ = \frac{2}{\pi} [V_s + R_s i^{\beta(t)}] i(t) d\omega t \]
2.2 Switching losses

Switching loss is the power dissipation during turn-on and turn-off switching transitions, the switching loss can be determined by plotting the voltage and current waveform in controllable switch during the switching transition and multiplying the waveforms point by point to get an instantaneous power waveform, and the energy loss during turn-off of a switch by using linear approximation can be expressed as,

\[
P_{sw} = 2\pi \left[ 2V_{TH}I_{M} + R_{TH}I_{M}^{\beta} \int_{0}^{\pi} \sin^{\beta+1} \omega t \, d\omega \right]
\]  
\(\text{(4)}\)

\[E_{\text{off}}, k = \int_{0}^{t_{\text{off}}} V(t)I(t) \, dt
\]
\(\text{(5)}\)

\[= \int_{0}^{t_{\text{off}}} \left( \frac{V_{\text{off}}}{t_{\text{off}}} t \left( -\frac{I}{t_{\text{off}}} (t - t_{\text{off}}) \right) \right) \, dt
\]
\(\text{(6)}\)

\[E_{\text{off}}, k = \frac{V_{\text{off}}, k, I_{t_{\text{off}}}}{6}
\]
\(\text{(7)}\)

Similarly

\[E_{\text{on}}, k = \int_{0}^{t_{\text{on}}} V(t)I(t) \, dt
\]
\(\text{(8)}\)

\[= \int_{0}^{t_{\text{on}}} \left( \frac{V_{\text{on}}}{t_{\text{on}}} t \left( -\frac{I}{t_{\text{on}}} (t - t_{\text{on}}) \right) \right) \, dt
\]
\(\text{(9)}\)

Average switching losses can be calculated by using equation 10.

\[P_{sw} = 2f \left[ \sum_{k=1}^{N_{\text{switch}}} \left( \sum_{i=1}^{N_{\text{on}, k}} E_{\text{on}, k, i} + \sum_{i=1}^{N_{\text{off}, k}} E_{\text{off}, k, i} \right) \right]
\]
\(\text{(10)}\)

And the Total power losses will be estimated as the combination of conduction losses, auxiliary switch conduction loss and average switching loss will be expressed in the equation 11.

\[P_{loss} = P_{c, M_c} + P_{c, A_c} + P_{sw}
\]
\(\text{(11)}\)

3. Structure of the proposed CMHB-MLI

The proposed CMHB-MLI is shown in the Fig. 2, is a cascaded unit of 15 level inverter, for its dc-dc converter section that consists of number n semiconductor section, it is capable of producing n+1 voltage levels according to different switching states. With the operation of the H-bridge, a total of 2n+3 voltage level can be produced.
Figure 2. Proposed CMHB-Multilevel inverter topology

3.1 Circuit Description and state analysis
Figure 3. Working states for the Proposed CMHB-Multilevel inverter topology. (a) maximum positive output voltage (+Vdc) (b) +6Vdc/7 (c) +5Vdc/7 (d) +4Vdc/7 (e) +3Vdc/7 (f) +2Vdc/7 (g) +Vdc/7

Table 1. Switching States for the Proposed Inverter

| output voltage | M1 | M2 | M3 | M4 | M5 | M6 | A1&A 4 | A2&A 3 |
|----------------|----|----|----|----|----|----|--------|--------|
| 70             | 1  | 0  | 1  | 0  | 1  | 0  | 1      | 0      |
| 60             | 1  | 0  | 1  | 0  | 0  | 1  | 1      | 0      |
| 50             | 1  | 0  | 0  | 1  | 1  | 0  | 1      | 0      |
| 40             | 1  | 0  | 0  | 1  | 0  | 1  | 1      | 0      |
| 30             | 0  | 1  | 1  | 0  | 1  | 0  | 1      | 0      |
| 20             | 0  | 1  | 1  | 0  | 0  | 1  | 1      | 0      |
| 10             | 0  | 0  | 1  | 0  | 1  | 0  | 1      | 0      |
| 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0      | 0      |
| -10            | 1  | 0  | 1  | 0  | 1  | 0  | 0      | 1      |
| -20            | 1  | 0  | 0  | 1  | 0  | 1  | 0      | 1      |
| -30            | 1  | 0  | 0  | 1  | 1  | 0  | 0      | 1      |
| -40            | 0  | 1  | 1  | 0  | 0  | 1  | 0      | 1      |
| -50            | 0  | 1  | 1  | 0  | 1  | 0  | 0      | 1      |
| -60            | 0  | 1  | 0  | 1  | 0  | 1  | 0      | 1      |
| -70            | 0  | 1  | 0  | 1  | 1  | 0  | 0      | 1      |
3.2 Operating modes of the proposed 15 level CMHB Multilevel inverter

The positive staircase output produced by the proposed switching pattern is explained from maximum positive voltage (Vdc) to zero level, the voltage level obtained is Vdc, 6Vdc/7, 5Vdc/7, 4Vdc/7, 3Vdc/7, 2Vdc/7 and Vdc produces the positive output is explained below.

(i) When MOSFET switch M1, M3, M5 is turned ON, and switches in H-bridge A1 and A4 is at on position, and the switch M2, M4, M6, A2 AND A3 is at OFF position the current flows through from the source and produces a maximum positive output voltage of (Vdc) of the load.

(ii) When the MOSFET switch M1, M3, M6 is turned ON, and switches in H-bridge A1 and A4 is at on position, and the switches M2, M3, M5 is at OFF position the current flows through from the positive potential and produces a positive output voltage of (6Vdc/7) at the load.

(iii) When the MOSFET switch M1, M4, M5 is turned ON, and switches in H-bridge A1 and A4 is at on position, and the switches M2, M3, M6 is at OFF position the current flows through from the positive potential and produces a positive output voltage of (5Vdc/7) at the load.

(iv) When the MOSFET switch M1, M4, M6 is turned ON, and switches in H-bridge A1 and A4 is at on position, and the switches M2, M3, M5 is at OFF position the current flows through from the positive potential and produces a positive output voltage of (4Vdc/7) at the load.

(v) When the MOSFET switch M2, M3, M6 is turned ON, and switches in H-bridge A1 and A4 is at on position, and the switches M1, M4, M5 is at OFF position the current flows through from the positive potential and produces a positive output voltage of (3Vdc/7) at the load.

(vi) When the MOSFET switch M2, M3, M6 is turned ON, and switches in H-bridge A1 and A4 is at on position, and the switches M1, M4, M5 is at OFF position the current flows through from the positive potential and produces a positive output voltage of (2Vdc/7) at the load.

(vii) When the MOSFET switch M2, M4, M5 is turned ON, and switches in H-bridge A1 and A4 is at on position, and the switches M1, M3, M6 is at OFF position the current flows through from the positive potential and produces a positive output voltage of (Vdc/7) at the load.

Similar to the positive staircase output obtained by different switching pattern, negative staircase output voltage from -Vdc/7, -2Vdc/7, -3Vdc/7, -4Vdc/7, -5Vdc/7, -6Vdc/7 and -Vdc also can be obtained by reversing the pattern of switching at each level and 15-level output is obtained.
4. Simulation and Hardware Results
Figure 7. PWM current

Figure 8. PWM technique
In the above figure, we calculated the THD value in a 15-level inverter, which was 7.69%.

### Table 2 Comparison

| PARAMETERS     | EXISTING SYSTEM | PROPOSED SYSTEM |
|----------------|-----------------|-----------------|
| Levels         | 5               | 15              |
| No of source   | 2               | 3               |
| No of switch   | 8               | 10              |
| THD value      | 9.78            | 7.699           |

Figure 9. Total harmonic distortion
In the above figure, we calculated the THD value in a 15-level inverter, which was 7.69%.
5. Conclusion
In this paper an asymmetric improved cascaded modified H-bridge asymmetrical multilevel inverter (CMHB-MLI) is proposed and generates a output voltage of 15 level, compared with the existing system with five level asymmetrical multilevel inverter the percentage of number of switches is reduced to 10, The analysis for total harmonic distortion (THD) in proposed CMHB-MLI by using Opposite phase disposition pulse width modulation (OPD-PWM) switching technique at lower frequency of (50 Hz) is
7.699% which is comparatively 40% less than existing system thereby reduces the switching stress and quality of the output improved without output filter, The experimental output is verified by using MATLAB/SIMULINK and hardware implementation.

References:
[1] C. H. Hsieh, T. J. Liang, S. M. Chen, and S. W. Tsai, “Design and Implementation of a Novel Multilevel DC-AC Inverter,” IEEE Trans. Ind. Appl., 2016, doi: 10.1109/TIA.2016.2527622.
[2] K.B. Bhaskar and T.S.Sivakumar 'Impimentation of 11 level cascaded multilevel inverter using level shifting pulse with modulation technique with different loads', International journal of electrical engineering(IPASJ),volume 2,issue 10 Nov 2014
[3] L. Wang, Q. H. Wu, and W. Tang, “Novel Cascaded Switched-Diode Multilevel Inverter for Renewable Energy Integration,” IEEE Trans. Energy Convers., 2017, doi: 10.1109/TEC.2017.2710352.
[4] N. Prabaharan and K. Palanisamy, “A Single Phase Grid Connected Hybrid Multilevel Inverter for Interfacing Photo-voltaic System,” 2016, doi: 10.1016/j.egypro.2016.11.281.
[5] Bhaskar, K. B., &Alagumariappan, P. (2020). Energy Channeling Led Driver Technology to achieve Flicker Free Operation with Zeta Converter for Power Quality Improvement. International Journal of Automation and Smart Technology, 10(1), 401-407.
[6] S. Sudha Letha, T. Thakur, and J. Kumar, “Harmonic elimination of a photo-voltaic based cascaded H-bridge multilevel inverter using PSO (particle swarm optimization) for induction motor drive,” Energy, 2016, doi: 10.1016/j.energy.2016.04.033.
[7] Paramasivam A., Bhaskar K.B., Madhanakkumar N., Vanchinathan C. (2020) Analysis of an Enhanced Positive Output Super-Lift Luo Converter for Renewable Energy Applications. In: Siano P., Jamuna K. (eds) Advances in Smart Grid Technology. Lecture Notes in Electrical Engineering, vol 687. Springer, Singapore. https://doi.org/10.1007/978-981-15-7245-6_11
[8] J. W. Dixon, “Multilevel converters,” in Power Electronic Converters and Systems: Frontiers and Applications, 2016.
[9] L. K. Haw, M. S. A. Dahidah, and H. A. F. Almurib, “SHE-PWM cascaded multilevel inverter with adjustable DC voltage levels control for STATCOM applications,” IEEE Trans. Power Electron., 2014, doi: 10.1109/TPEL.2014.2306455.
[10] Alagumariappan, Paramasivam, Najumnissa Jamal Dewan, GughanNarasimhanMuthukrishnan, Bhaskar K. Bojji Raju, Ramzan Ali Arshad Bilal, and VijayalakshmiSankaran. 2020. "Intelligent Plant Disease Identification System Using Machine Learning" Engineering Proceedings 2, no. 1: 49. https://doi.org/10.3390/ecsa-7-08160
[11] S. T. Meraj, A. Ahmed, L. K. Haw, A. Arif, and A. Masaoud, “DSP Based Implementation of SHE-PWM for Cross-Switched Multilevel Inverter,” 2019, doi: 10.1109/CSPAS.2019.8695981.
[12] S. Bhadra and H. Patangia, “A comparison based harmonic elimination method with digital control of fundamental amplitude,” 2013, doi: 10.1109/ICIInfS.2013.6731991.
[13] A. Prayag and S. Bodkhe, “A comparative analysis of classical three phase multilevel (five level) inverter topologies,” 2017, doi: 10.1109/ICEPEICES.2016.7853567.
[14] I. H. Shanono, N. R. H. Abdullah, and A. Muhammad, “A Survey of Multilevel Voltage Source Inverter Topologies, Controls, and Applications,” Int. J. Power Electron. Drive Syst., 2018, doi: 10.11591/ipeds.v9.i3.pp1186-1201.
[15] X. Jiang and M. L. Doumbia, “Comparative Study of Grid-Connected Multilevel Inverters for
[13] High Power Photovoltaic Systems,” 2019, doi: 10.1109/SEGE.2019.8859784.

[16] I. H. Shanono, N. R. H. Abdullah, and A. Muhammad, “A survey of multilevel voltage source inverter topologies, controls and applications,” International Journal of Power Electronics and Drive Systems. 2018, doi: 10.11591/iypeds.v9n3.pp1186-1201.

[17] M. S. Manoharan, A. Ahmed, H. W. Kim, and J. H. Park, “A single-source photovoltaic power conditioning system using asymmetric cascaded multilevel inverter,” 2015, doi: 10.1109/ICPE.2015.7167761.

[18] A. Chen, D. Shao, C. Du, and C. Zhang, “High-frequency DC link flyback single phase inverter for grid-connected photovoltaic system,” 2010, doi: 10.1109/PEDG.2010.5545796.

[19] K. H. Law, W. P. Q. Ng, and W. K. Wong, “Flyback cascaded multilevel inverter based SHE-PWM control for STATCOM applications,” Int. J. Power Electron. Drive Syst., 2017, doi: 10.11591/ijpeds.v8i1.pp1186-1201.

[20] A. Nami, F. Zare, A. Ghosh, and F. Blaabjerg, “A hybrid cascade converter topology with series-connected symmetrical and asymmetrical diode-clamped H-bridge cells,” IEEE Trans. Power Electron., 2011, doi: 10.1109/TPEL.2009.2031115.

[21] Y. He, P. Liu, J. Liu, and Z. Wang, “A design method of hybrid cascade multilevel structure for active power filter application in moderate-voltage grid,” 2010, doi: 10.1109/IPEC.2010.5542339.

[22] S. Mariethoz and A. Rufer, “New configurations for the three-phase asymmetrical multilevel inverter,” 2004, doi: 10.1109/ias.2004.1348509.

[23] Y. Suresh and A. K. Panda, “Investigation on hybrid cascaded multilevel inverter with reduced dc sources,” Renewable and Sustainable Energy Reviews. 2013, doi: 10.1016/j.rser.2013.04.027.

[24] F. Khoucha, S. M. Lagoun, K. Marouani, A. Kheloui, and M. E. H. Benbouzid, “Hybrid cascaded H-bridge multilevel-inverter induction-motor-drive direct torque control for automotive applications,” IEEE Trans. Ind. Electron., 2010, doi: 10.1109/TIE.2009.2037105.

[25] Z. Du, L. M. Tolbert, and J. N. Chiasson, “Active harmonic elimination for multilevel converters,” IEEE Trans. Power Electron., 2006, doi: 10.1109/TPEL.2005.869757.

[26] J. Napolis et al., “Selective harmonic mitigation technique for cascaded H-bridge converters with nonequal DC link voltages,” IEEE Trans. Ind. Electron., 2013, doi: 10.1109/TIE.2012.2192896.

[27] D. A. Ruiz-Caballero, R. M. Ramos-Astudillo, S. A. Mussa, and M. L. Heldwein, “Symmetrical hybrid multilevel DCAC converters with reduced number of insulated DC supplies,” IEEE Trans. Ind. Electron., 2010, doi: 10.1109/TIE.2009.2036636.