Low-voltage linear bootstraped sampling switch with a-InGaZnO TFTs

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This letter presents a novel linear bootstraped sampling switch using amorphous indium-gallium-zinc-oxide thin-film transistors, which is designed using all enhancement n-type transistors. The switch is simulated at a low supply voltage and a small transistor channel length of 2 V and 2 μm, respectively. The simulation results across the process corners have shown a maximum variation of 2.2% in the off-resistance of the switch. Moreover, the worst-case signal-to-noise and distortion-ratio, spurious-free-dynamic-range, and total-harmonic distortion across the process corners have been observed as 66, 70 and –68 dB, respectively, at a sampling frequency of 50 kHz. This circuit finds potential applications in implementing an analogue-to-digital converter with oxide thin-film transistors technology, which is an essential block in flexible sensing systems.

Introduction: Amorphous oxide thin-film transistor (TFT) technology empowers low-cost flexible and transparent electronics due to its compatibility with low-temperature fabrication techniques [1–4]. As a result, this technology helps to implement wearable electronics with unobtrusiveness, which is difficult to achieve with standard complementary-metal-oxide semiconductor (CMOS) technology, where the circuits are fabricated on rigid substrates due to the high-temperature fabrication process. Moreover, oxide TFT technology enables circuit fabrication on an insulator substrate, eliminating the body-bias effect, and body-related parasitics. However, low intrinsic mobility, large device parasitics, high operating voltages [5, 6], and scarcity of amorphous p-type oxide TFTs [7–9] are the major bottlenecks of the oxide technology in the system-level implementation of practical importance.

A sampling switch is an integral part of the analogue-to-digital converter, which is an important functional block in flexible sensing systems. The work done on sampling switches is scarce with oxide TFT technology. Though many other works have been reported on amplifiers [10], ring oscillators [11], logic gates [12], and DC–DC converters [13] with this technology, sampling switch has not been explored. Moreover, the reported circuits operate with a minimum supply voltage and a reliable device channel length of 6 V and 10 μm, respectively, which results in high power consumption and ample active-area occupancy.

Besides, the power supply voltage and channel length scaling degrade the circuit performance with oxide TFT technology [14].

A sampling switch with only a single n-type pass transistor limits the maximum amplitude of the input analogue signal due to the inherent threshold voltage (V_DD) drop of the transistor. Moreover, its large signal on-resistance (R_ON) is a function of the input signal amplitude, which leads to non-linear errors [15]. Many bootstrapped sampling switches have been reported in CMOS technology with bi-polar (p- and n-type) transistors to address the limitations faced by the pass transistor switches [9]. However, these designs cannot be adapted directly in amorphous oxide TFT technology as the amorphous p-type oxide TFTs are still under active investigation [7–9]. Therefore, to mitigate the limitations of n-type pass transistor switches with amorphous oxide TFT technology, this work proposes a linear bootstrapped sampling switch, which operates at a low supply voltage and a small device channel length of 2 V and 2 μm, respectively. The switch is designed using all enhancement n-type TFTs. Moreover, it employs a voltage booster to boost the gate voltages of intermediate n-type transistors in the circuit, making R_ON almost constant over the full-scale range of the input analogue signal.

Proposed Sampling Switch: The large signal ON-resistance (R_ON) of the n-type pass transistor is defined in Equation (1) considering a negligible voltage drop across the transistor.

\[
R_{ON} = \frac{1}{\mu_{OX} \left( \frac{W}{L} \right) (V_{GS} - V_{TH})} \tag{1}
\]

Here, \( \mu_{OX}, C_{OX}, \frac{W}{L}, \) and \( V_{GS} \) are the mobility, oxide capacitance, aspect ratio and the gate-to-source voltage of the transistor, respectively. It should be noted that \( V_{GS} \) is the function of the amplitude of the input analogue signal \( V_{IN} \). Therefore, if the gate of the n-type pass transistor switch is controlled by a sampling clock signal (clk), which oscillates between the power supply voltage (V_DD) and 0 V, Equation (1) is modified as Equation (2).

\[
R_{ON} = \frac{1}{\mu_{OX} \left( \frac{W}{L} \right) (V_{DD} - V_{GS} - V_{TH})} \tag{2}
\]

As a result, \( R_{ON} \) strongly depends on the amplitude of \( V_{IN} \). Moreover, the inherent \( V_{TH} \) drop of the n-type pass transistor switch restrains the full-scale amplitude (0 V to V_DD) of \( V_{IN} \).

The schematic of the proposed bootstrapped sampling switch with only n-type transistors is shown in Figure 1. In the switch, the clock at the gate of the transistor M1 is bootstrapped to a voltage \( V_{DD} + V_{TH} \) using a capacitor \( C_{OX1} \) and transistors M2–M7 to make \( V_{GS} \) of M1 independent of \( V_{DD} \). A rail-to-rail pseudo-CMOS bootstrapped inverter (I2 and I3) [12] is used to generate clk from clk signal. The switch also employs a clock booster [16] comprises of transistors M8–M9 and capacitors C1–C2, to generate signals oscillating between \( V_{DD} \) and \( 2V_{DD} \) at nodes N1 and N2 from clk and clk respectively. In addition, a clock booster for driving the gate of transistor M5 is proposed, which employs two rail-to-rail pseudo-CMOS bootstrapped inverters (I2 and I3) [12], a transistor M10 and a capacitor C3. It should be noted that the two inverters (I2 and I3) take their power supply voltages from nodes N2 and N3 as shown in Figure 1.

The operation of the proposed sampling switch is explained using following two phases:

Phase-I: The equivalent circuit of the sampling switch with signals at nodes N1 and N2 are shown in Figure 2(a). In this phase, clk makes a transition from \( V_{DD} \) to 0 V. As a result, transistors M3, M7 and M10 are turned ON and the output of the inverters (I2 and I3) will be at logic 0 (=0 V). The voltage at node N1 (=2VDD) is applied to the gate of the transistors M4, which charges capacitor \( C_{OX1} \) to \( V_{DD} \) without any \( V_{TH} \) drop. Moreover, transistor M7 pulls the gate of M1–M2 to 0 V, to turn them OFF in the current phase. Since the output of I3 is at 0 V, transistor M5 is also turned OFF. Thus, the load capacitor \( C_{OX1} \) is isolated from \( V_{IN} \). In addition, transistor M10 charges C3 to a voltage equal to \( V_{DD} - V_{TH1}/2 \).

Phase-II: The equivalent circuit of the sampling switch with signals at nodes N1 and N2 are shown in Figure 2(b). In this phase, clk makes a transition from 0 V to \( V_{DD} \). As a result, all the transistors marked with grey colour are turned OFF. Since the input to the inverters I2 and I3 is 0 V, their output will be at their power supply voltages. Therefore, output of I2 is equal to the voltage at node N2 (=2V_DD), which charges node N3 to a voltage equal to \( V_{DD} - V_{TH2}/2 \). Since I3 takes its power
supply voltage from node $N3$, its output will be $3V_{DD} - V_{HLM10}$ and the gate voltage of transistor $M5$ is boosted in the current phase. As a result, transistor $M5$ is turned ON and it initially passes $V_{DD}$ at the gates of $M1$-$M2$ to turn them ON. Since transistor $M2$ is turned ON, it charges $C_{IN}$ to a voltage $V_{DD} + V_{DD}$, and finally, transistor $M5$ passes complete $V_{DD}$ to the gate of $M1$-$M2$ without any $V_{DD}$ drop. As a result, $V_{G5}$ of $M1$ will be a constant voltage ($=V_{DD}$) and $R_{ON}$ will be almost constant over the complete amplitude range of $V_{IN}$, which can ensure the desired performance without using wider transistor. Moreover, the maximum amplitude of $V_{IN}$ can be as high as $V_{DD}$.

Thus, the proposed linear sampling switch mitigates the limitations of n-type pass transistor switch with oxide TFT technology.

**Results and Discussions:** The proposed sampling switch is designed using oxide TFT models from PragmatIC [20]. The TFTs employed in the circuit has a channel length of $2\mu m$ and $V_{TH}$ of around 0.6 V. The switch is simulated at a $V_{DD}$ of 2 V, a sampling frequency of 50 kHz and an input signal frequency of 10 kHz with full-scale range (0 V to $V_{DD}$). The value of load capacitor $C_{L}$ is kept at 10 pF for all the simulations.

The gate voltages of transistors $M1$ ($V_{GSM1}$) and $M5$ ($V_{GSM5}$) were obtained from the transient simulations and they are shown in Figure 3. It is observed from the figure that $V_{GSM1}$ is boosted to a voltage close to 5 V when clk is at logic ‘1’ ($=V_{DD}$), which is 0.4 V less than the expected result of $3V_{DD} - V_{HLM10}$. This voltage drop of 0.4 is accounted for the parasitics at node $N2$, which degrades $V_{GSM1}$. However, $V_{GSM5}$ is large enough to pass the voltage $V_{DD}$ to $V_{GSM5}$ as can be seen from Figure 3. As a result, $V_{GSM1}$ is made almost independent of the amplitude of $V_{IN}$. In addition, the maximum amplitude of $V_{IN}$ can be as high as $V_{DD}$. The red arrow in the figure highlights the transient gate voltages when clk is at $V_{DD}$. Besides, it also shows that $C_{L}$ is correctly tracking the input analogue signal.

The transient simulations were performed by sweeping the input amplitude of $V_{IN}$ from 0 to 2 V (full-scale range) in a step size of 0.1 V. The obtained value of $R_{ON}$ from simulations is shown in Figure 4(a).

The figure shows $R_{ON}$ values at different process corners (slow, fast and typical). In order to study the percentage variations in $R_{ON}$, $\Delta R_{ON}$ is calculated using Equation (3) and it is shown in Figure 4(b).

$$\Delta R_{ON} = \frac{R_{ON,\text{min}} - R_{ON,\text{max}}}{R_{ON,\text{average}}}$$

It is observed from the figure that variations up to 2.2% in $R_{ON}$ have been observed when the simulations were performed at different process corners. It should be noted that the observed percentage variations in $R_{ON}$ is very low considering the large device parasitics of the oxide TFTs.

The spectrum of the output signal is obtained for 1024 FFT bins from transient simulations. At a sampling frequency of 50 kHz, the proposed sampling switch has shown signal-to-noise-and-distortion-ratio (SNDR), spurious-free-dynamic-range (SFDR) and total-harmonic-distortion (THD) of 72, 74.3 and $-72.3\, dB$, respectively, under typical conditions. Moreover, these dynamic parameters were obtained at different process corners and the result is shown in Figure 5. It is observed from the figure that in the worst-case, the proposed switch has shown SNDR, SFDR and THD better than 66, 70 and $-68\, dB$, which shows the ability of the proposed switch to drive the ADC with a maximum resolution of 10 bits. The dynamic parameters were also obtained at different frequencies of $V_{IN}$ and the results are summarised in Figure 6. It is observed from the figure that the performance of the switch degrades as the frequency of $V_{IN}$ increases due to the dominance of parasitics at different nodes of the circuits. However, the switch can still drive an ADC with a maximum resolution of 9 bits in the worst case with 10 pF load. It should be noted that with oxide TFT technology, the state of the art work has reported Nyquist ADCs not exceeding 7 bits and at a sampling frequency in tens and hundred of hertz [21]. However, by employing the proposed sampling switch, the resolution and speed of the ADC with amorphous oxide TFT technology can be improved.

**Conclusion:** A linear low-voltage sampling switch with oxide TFT technology is proposed for the first time in this letter, which is capable of working with a small device channel length of 2 $\mu m$. The sampling switch has shown a worst-case SNDR, SFDR and THD of 66, 70 and
Fig. 5 Dynamic parameters of the proposed sampling switch at different process corners

Fig. 6 Dynamic parameters of the proposed sampling switch at different frequencies of VIN

−68 dB, respectively, at a sampling frequency of 50 kHz and supply voltage of 2 V across process corners. In addition, a maximum 2.2% variation in RON over full-scale input signal range has been observed, which is very low with oxide TFT technology. Therefore, the proposed circuit can help to improve the figure-of-merit of the ADC at low operating voltages.

Acknowledgements: This work is supported by early career research grant with project ref. ECR/2017/000931, SPF/2021/000018, EP/P02839X/1 and IISER Bhopal. This work uses the oxide TFT models provided by PragmatiC for designing and simulating the proposed switch.

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Received: 4 February 2021 Accepted: 6 April 2021 doi: 10.1049/ell2.12203