260 GHz spatially combined transmitter with a V-band distributed OOK modulator

Jung-Dong Park

Graduate of School of Engineering, University of California, Berkeley, 2108 Allston Way, Berkeley, CA 94704, USA. Currently in Qualcomm, San-Jose, CA 95110, USA.
a) jungdong@eecs.berkeley.edu

Abstract: A 260 GHz on-off keying (OOK) transmitter (Tx) is presented with distributed switches in V-band fundamental signal path in 65 nm CMOS. Aiming at OOK modulation operating up to 20 Gb/s, distributed switches are integrated in the driving chain to suppress transient ringing from a LC tank in the PA where the modulated input directly switches the Tx output without information distortion. The spatially combined transmitter with on-chip antenna demonstrates up to 14 Gb/s of modulation speed with +5 dBm of equivalent isotropically radiated power (EIRP) at \( f_r = 246 \text{GHz} \).

Keywords: transmitter, OOK modulation, spatial-power combining, CMOS

Classification: Microwave and millimeter wave devices, circuits, and systems

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1 Introduction

Realization of a fully integrated THz transmitter (Tx) beyond the device cut-off frequency (\( f_T \)) and maximum oscillation frequency (\( f_{\text{max}} \)) is challenging to meet the required Tx power and high data rate modulation in ultrafast communication. When radiation frequency is higher than \( f_{\text{max}} \), the THz output can be generated by a frequency multiplier [1]. The efficiency of the antenna radiation and the frequency multiplier are the main key factors to implement ultra high speed wireless transceiver under this restriction.
For the on-chip planar antenna, the dimension shrinks to the RF pad size which may also result in the antenna efficiency improvement; its loss becomes comparable to the signal loss through the pads and the package. Therefore it is quite appealing approach to use the spatial power-combining by integrating multiple transmitters with on-chip antennas to overcome the shortage of the output power at this regime [2, 3]. However, the frequency multiplier involves more critical issues. When the modulated band-pass waveform like M-PSK signal is passing through the multiplier, the Tx output suffers from the nonlinear AM-AM and AM-PM distortions as well as PM-PM distortion from the frequency (phase) multiplications [4]. Therefore it requires a complex digital pre-distortion at the base-band which might seriously deteriorate achievable data rate eventually. Especially in the line-of-sight “cm” range wireless link, it can be shown that the required $e_b/N_0$ of OOK is comparable to that of QPSK [3].

This paper describes a transmitter design with distributed OOK modulator used in a 260 GHz transceiver [5] in detail. By utilizing a quadrupler with quadruple-push harmonic generator driven by class-D<sup>-1</sup> PA, the fast OOK modulation is achieved at V-band while the modulated Tx output signal spectrum is preserved after the multiplier. In order to serve this switching functionality among the amplifier with LC tank circuit, a distributed switching structure is introduced.

2 Transmitter design

Fig. 1 shows a spatially power combined 260 GHz transmitter with the distributed OOK modulator at V-band [3]. Two Tx blocks are integrated together with on-chip antenna array. Each block consists of a quadrupler, distributed OOK switches, a driving chain, and a hybrid for IQ signal generation.

2.1 V-band distributed OOK modulator

Class-D<sup>-1</sup> power amplifier (PA) is used in the driving chain. The LC tank used in the PA and driving amplifier (DA) causes a transient signal ringing which mainly limits the modulation speed of the transmitter. Considering the drain efficiency of the power amplifier (PA) as well as OOK modulation rate, the D<sup>-1</sup> PA tank has moderate quality factor around 3. The designed non-coherent OOK modulator is aiming at data rate $R_b$ up to 20 Gb/s which switches the ‘On’ and ‘Off’ status about three periods of the 65 GHz fundamental signal.

![Block diagram of the spatially power combined 260 GHz transmitter.](image-url)
From this reason single series-switch between DA and PA could not provide fast enough settling of the damping signal. In order to resolve this transient ringing issue from the tank, a 2nd parallel switch (M3) is introduced at the output of the $D^{-1}$ PA tank. Fig. 2 presents the structure of the distributed OOK modulator. Class-A driver stage is used to provide $+7 \text{dBm}$ of driving amplitude for the optimal switching of the PA device (M1, M2). Since the first OOK modulator is a series switch, the impedance seen at the input of the modulator is varying depending on the status of the modulating switch pair (M4, M5). The dummy load is placed in parallel to mask the switching action by using the complementary switch pair (M6, M7) penetrating dummy load to the preceding stages. From harmonic balanced (HB) simulation, the isolation between ‘On’ and ‘Off’ of the distributed OOK modulator is larger than 45 dB with insertion loss less than 7 dB including single to differential input balun with loss of 4 as shown in Fig. 3-(a).

Implemented with the distributed OOK modulator, high speed data distribution was another limiting factor for high speed data modulation. The residual delay from the CMOS repeater should be minimized to track switching signal synchronization. The circuit was designed to have less than fan-out of 2 to achieve the speed requirement. Fig. 3-(b) presents the modulated signal with \( R_b = 20 \text{Gb/s} \) in transient simulation. Input clock pulse distortion caused by the limited bandwidth is minimized by carefully placing buffers throughout the routing trace. There is a small ripple shown at the beginning of the transition which was well suppressed with distributed switch up to 20 Gb/s. Simulated output power of the designed PA including 2nd switch is $+13 \text{dBm}$ with $+7 \text{dBm}$ of input driving power at “on” state.

![Fig. 2. Circuit diagram of the distributed non-coherent OOK modulator with $D^{-1}$ PA.](image)

![Fig. 3. (a) Simulated isolation and thru for the designed distributed non-coherent OOK modulator. (b) 20 Gb/s OOK modulated output of the power amplifier.](image)
2.2 Frequency quadrupler

The transmitter quadrupler generates 260 GHz 4th harmonic output from 65 GHz input. The quadrupler utilizes a quadrature-push clamping circuit driven by the balanced IQ quadrature fundamental signals as shown in Fig. 4. The gate bias is provided by the center tap of the transformer. Owing to the push-push clamping structure, all the odd harmonics are cancelled out including the strong fundamental driving signals. Thus bulky and lossy fundamental signal rejection circuit is unnecessary. Only $n \cdot 4^{th}$ ($n = 0, 1, 2, \cdots$) harmonics are delivered at output load.

The balanced I/Q quadrature signals are routed with CPS T-line with $Z_0 = 92 \Omega$ and the controlled series inductor $L_{gM}$ is realized with more separated CPS line where conjugated matching is achieved in a simple form of the LC matching network. The gate DC bias is fed from the center tap of the output transformer in the preceding PA. 20 µm of the NMOS width ($W$) is chosen to optimize conversion loss around $+13$ dBm of IQ driving power. Since the load is the half-width Microstrip-line Leaky Wave Antennas (MLWA) with one of the edges shorted to ground [6], the output matching network is DC-blocked with the microstrip-coupled line. With $P_{in} = +13$ dBm input signals applied to each I and Q push-push pair (total $+16$ dBm), the 4th harmonic component is stronger than the 2nd harmonic if IQ phase mismatch is smaller than 10° as shown in Fig. 5-(a). Fig 5-(b) shows the conversion loss (CL) as a function of the driving input power.

When 2nd modulation switch M3 in Fig. 2 is “ON”, there is 15 dB of input power reduction which causes more than 15 dB of increase in the conversion loss.

![Fig. 4. 260 GHz quadrupler with the quadruple-push harmonic structure.](image)

![Fig. 5. Simulated (a) 4th/2nd harmonic ratio and 4th harmonic power as a function of I/Q phase mismatch, (b) conversion loss as a function of the total input power.](image)
2.3 Spatial-power combining with TRx dual antenna

Two sets of on-chip TRx dual MLWA is integrated to serve as a spatial power combiner. As a unit antenna element, a half-width leaky wave antenna is concurrently matched to the Rx and Tx, relieving aperture size restriction due to the chip area constraint while obviating the need for an explicit TR switch. By arraying four antenna elements, the designed TRx dual antenna-array achieves +4.9 dBi of maximum antenna gain at 245 GHz with more than 30 GHz of matching bandwidth. The expected maximum EIRP is +6.8 dBm at 245 GHz.

3 Measurement

Fig. 6 presents implemented transmitter in 65 nm TSMC CMOS process. The in-situ OOK modulator is characterized using a V-band horn antenna, a down-converter, and a spectrum analyzer. Weakly radiating V-band fundamental signal is measured while the transmitter is operating. The spectral line of the PRBS output has sinc²(f) envelope having spectral line spacing at \(m \cdot \Delta f = m \cdot R_b/(2^{27}-1)\) Hz \((m = 1, 2, 3 \cdots)\) from the on-chip interleaved PRBS \((2^{27}-1)\) with CML logic. Fig. 7 shows measured spectral line spacing at the fundamental signal with 14 Gb/s of modulation data-rate in the transmitter. Owing to the pseudo random characteristic which repeats with \(2^{27}-1\) bits in the integrated PRBS generator, the spectrum shows 111 MHz of the periodic spectral line spacing \((\Delta f)\). Using a power-meter, WR-3.4 horn antenna, and a waveguide transition, we measured +5 dBm of maximum EIRP.

Fig. 6. Microphotograph of the fabricated Tx block unit (925 \times 420 \mu m^2).

Fig. 7. (a) Setup for the modulated in-situ fundamental signal spectrum, (b) Measured spectral spacing at the fundamental signal with 14 Gb/s of modulation.
at 246 GHz. Fig. 8 shows a comparison between the measured EIRP and the simulated one. Table I presents the performance summary of the Tx with power consumption contribution from each block.

| Technology                        | 65 nm CMOS                             |
|-----------------------------------|----------------------------------------|
| On-chip half-width MLW antenna    | Gain = +4.9 dBi, BW > 30 GHz           |
| V-band OOK modulator              | Modulation Rate = 14 Gb/s,             |
|                                   | On/off isolation = 45 dB               |
| 260 GHz Quadrupler                | Conversion loss = 16 dB, P_{DC} = 2 mW |
| V-band driving stages (D^{-1} PA+DA) | Max. output = +13 dBm with D^{-1} PA |
|                                   | Drain efficiency = 29%, P_{DC} = 116 mW |
| EIRP                              | +5 dBm at 246 GHz                      |
| Total DC power                    | 688 mW                                 |

Fig. 8. Simulated and measured EIRP of the transmitter.

Table 1. Performance summary

4 Conclusion

A 260 GHz CMOS transmitter was demonstrated upto 14 Gb/s of modulation speed with proposed distributed OOK modulator. The spatially power combined transmitter achieved +5 dBm of EIRP at 246 GHz with power consumption of 688 mW.

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