Steady-state analysis and design of phase-controlled class-D ZVS inverter

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Abstract: This paper proposes an analysis and design method of the phase-controlled class-D Zero-Voltage Switching (ZVS) inverter. To derive the ZVS region diagram, a steady-state waveform of the phase-controlled class-D inverter is analytically derived. This analysis introduces an expression of an anti-parallel diode behavior and multiple-harmonic analysis. By developing a ZVS region diagram at the fixed phase shift and drawing power contour lines over the region diagram, a parameter region, in which sufficient power can be obtained with achieving the ZVS, are also determined. The analysis and design method of this paper were verified through circuit experiments and by collating the quantitative values obtained from the experiment and analysis.

Key Words: zero-voltage switching, class-D inverter, anti-parallel diode, phase-controlled, harmonic component

1. Introduction

The resonant inverters [1–13] have broad applications ranging from wireless power transfer [3–5], RF power supply [6–8], induction heating [9–11], and power amplifiers for communication [12, 13]. Frequency modulation control, which includes an LLC converter, is an effective means to control the output power in resonant inverters and converters. However, a fixed frequency control is required for use in wireless power transfer and RF power supply. Phase control is used to adjust the output power by changing the phase of the driving signal from a pair of inverters.

One of the major resonant inverters, which achieves high power-conversion efficiency, is the class-E inverter [14–18]. The class-E inverter requires a highly voltage-resistant switching device because the maximum switch voltage can be as high as 3.5-times of the input voltage. By contrast, the maximum switch voltage for the class-D inverter is the equivalent of the input voltage and thus the cost of the switch device remains low. From the above reason, this paper focuses on the class-D inverter with phase control.
The Zero-Voltage Switching (ZVS) achievement is an important issue for resonant-inverter designs. Generally, it is required for high-frequency resonant inverters to achieve the ZVS in the entire control range. The designers would like to ensure the design conditions such as the ZVS theoretically at the inverter-design step. The circuit performances are generally comprehended by the entire-region search, which means that many trials-and-errors with high computation cost are necessary for inverter designs. In this sense, it is a hard task for designers to ensure keeping the conditions such as the ZVS in the entire control range.

The performance visualization algorithm on parameter spaces was presented in [19]. The key technique in [19] is that the circuit performance in the entire parameter space can be comprehended by just tracking the special conditions for dividing the circuit performances. One of the cutting-edge design methods is to apply a heuristic optimization algorithm [20–22] for converter designs. By applying the heuristic optimization algorithm, it is possible to obtain a proper parameter set, which achieves multiple design conditions. In this design approach, however, it is possible to obtain just the optimization ‘point.’ The designer cannot comprehend the relationship between the circuit parameter and performance intuitively on parameter spaces. The performance visualizations in [19] are, on the other hand, achieved by solving the algebraic equations successively. The computation cost for solving the algebraic equations is much lower than that for heuristic-optimization calculations. Therefore, the designers can comprehend circuit performance on parameter spaces easily with low computation cost by adopting the performance-visualization algorithm in [19]. From these visualization diagrams, it is possible to ensure that the inverter keeps the conditions in the entire control range theoretically. The performance visualizations in [19] were, however, done with full-numerical computations with transient-analysis waveform. Therefore, a problem with the computation cost still remains.

One of the solutions to this problem is to use the steady-state analytical waveform formula in stead of the numerical transient-analysis waveform. The steady-state analysis expression greatly reduces the calculation amounts compared with numerical transient analysis. The fundamental harmonic analysis was previously used for resonant circuits with an assumption of a pure sinusoidal output current [23–25]. The impedance in the phase-controlled class-D inverter varies as observed from each inverter, and likewise, the waveform of the current owing through resonant circuit varies and the switch voltage becomes asymmetrical between a pair of inverters. At the same time, harmonic components are included in the output current because the resonant frequencies of the resonant filters vary acceding to phase shift. Therefore, a multiple-harmonic analysis [26–28] needs to be conducted. Conventional analyses assume that the ZVS is achieved by turning on the anti-parallel diode while the switch remains off [29–31]. However, an anti-parallel diode, which occasionally turns on, turns off again before the switch is turned on [16–18]. Additionally, the phase-controlled class-D inverter has asymmetrical behavior characteristics owing to the phase shift, and the behavior of the switch for each inverter needs to be considered. A steady-state analysis expression that accurately expresses the switching state of each inverter and takes harmonic components into account does not exist for the phase-controlled class-D inverter. By achieving the expression of these behavior waveforms at high precision, waveforms are recreated under various states, thus enabling an understanding of the switching state correctly.

This paper proposes an analysis and design method of the phase-controlled class-D ZVS inverter. To visualize the ZVS region on the parameter space, a steady-state waveform of the phase-controlled class-D inverter is analytically derived. Waveforms at any phase shifts can be expressed accurately because this analysis introduces an expression of an anti-parallel diode behavior and multiple-harmonic analysis. Circuit parameters that serve as a boundary condition between a ZVS and a non-ZVS at a given phase shift is derived by using the obtained waveform formula, to graphically represent the ZVS region. The ZVS region diagram are developed for various phase shifts within the range of 0 to $\pi$. By changing the phase shift, developing a ZVS region diagram, and drawing power contour lines over the region diagram, a parameter region, in which sufficient power can be obtained with achieving the ZVS, are also determined. By using an analysis formula, these diagrams can be developed quickly with low computation cost, and an inverter can then be designed within a short period of time. The proposed analysis and design of this paper were verified through a circuit experiment and by collating
the quantitative values obtained from the experiment and analysis.

2. Operation principle

Figure 1 shows a circuit topology of the phase-controlled class-D inverter, which connects the class-D inverters in parallel. Each class-D inverter consists of an input voltage \( V_I \), two switch devices \( S_{1j}, S_{2j} \), shunt capacitances \( C_{S1j}, C_{S2j} \), a series resonant filter \( L_{rj} - C_{rj} \), and load resistance \( R \), where \( j = 1 \) and 2 are the inverter labels.

Figure 2 shows example waveforms of the phase-controlled class-D inverter, where \( \theta = \omega t = 2\pi ft \) is the angular time and \( f \) is the operating frequency of the inverter. The high- and low-side switches of each inverter switch in an alternating manner. At this point, the dead time in which both switches are turned off is defined. The duty ratio \( D \) of each inverter is fixed at the same level, but a phase shift \( \phi \) is provided between inverters for the output-power control. The behavior of each inverter becomes asymmetrical owing to the phase shift. For this reason, the switching behavior of each inverter also varies. For example, the switch voltage on one side satisfies the ZVS, but that of the other side may not, as indicated by the waveforms for the switch voltages as shown in Fig. 2.

The fundamental frequency component of the bottom-switch voltage is extracted using a series resonant filter, and an ac current is generated. The resonant currents \( i_1 \) and \( i_2 \) gain a phase shift based on the phase shift of the gate-drive signals \( D_{r1} \) and \( D_{r2} \) driving \( S_1 \) and \( S_2 \). Because the output voltage is a sum of \( i_1 \) and \( i_2 \), the phase-controlled class-D inverter can adjust the output power using the phase shift. The impedance in the phase-controlled class-D inverter varies as observed from each inverter. Therefore, the waveforms of \( i_1 \) and \( i_2 \) are different, and the currents that flow through the resonant filters may contain harmonic components. Likewise, the switch voltage becomes asymmetrical between a pair of inverters.

Figure 3 shows example waveforms for the bottom-switch voltage and the bottom-switch current of the phase-controlled class-D inverter. Now it is considered that the switch \( S_{1j} \) is turned off at \( \theta = \theta_{0j} \) and turned on at \( \theta = 2\pi + (j - 1)\phi \). Switching behaviors can be classified into three different patterns, as shown in the Fig. 3. In Fig. 3(a), the switch turns on while the switch voltage does not reach zero during the period in which the switch is in the off-state, which is defined as “Pattern 1”. In Fig. 3(b), the switch voltage reaches zero during the period in which the switch is in the off-state. When the switch voltage drops to zero at \( \theta = \theta_{1j} \), the anti-parallel diode turns on. The switch also turns on during the anti-parallel diode is in the on-state, which is defined as “Pattern 2”. In Fig. 3(c), the anti-parallel diode switches off again at \( \theta = \theta_{2j} \) before the switch turns on, which is defined as “Pattern 3”. It can be stated that, only (b) achieves the ZVS among (a)–(c) in Fig. 3. The switch voltages between the bottom switch and the top one have symmetry, namely \( v_{S2j}(\theta) = 1 - v_{S1j}(\theta) = v_{S1j}(\theta + \pi) \).

3. Analytical expressions of steady-state waveforms

3.1 Assumptions

The analysis of the phase-controlled class-D inverter presented in this paper is based on the following assumptions.

1. All the passive components work as linear components, which have no parasitic element.

2. The MOSFETs and anti-parallel diodes work as ideal switches. Therefore, zero-switching time,
zero on-resistance, and infinite off-resistance are assumed.

3. The switches $S_{11}$ and $S_{21}$ turn on at $\theta = 0$ and $\theta = \pi$, respectively, with a duty ratio $D$ as shown in Fig. 2, where $0 < D < 0.5$. In addition, the class-D inverters 1 and 2 are driven with a phase shift of $\phi$ in the range of $0 < \phi < \pi$, namely $\theta_{ij} = \pi(1 + 2D) + (j - 1)\phi$.

4. In order to obtain zero output power, the component values of the class-D inverters 1 are the same as those of inverter 2.

3.2 Parameters
In this analysis, the following parameters are defined.

1. $Q = \omega L_{rj}/R$: The loaded $Q$ factor.

2. $A = \omega_{oj}/\omega = 1/(2\pi f \sqrt{L_{rj} C_{rj}})$: The ratio of the resonant frequency to the operating frequency.

3. $B = C_{rj}/C_S$: The ratio of the resonant capacitance to the shunt capacitance.

3.3 Expression of the output current
Because of the asymmetric operation of the phase-controlled class-D inverter, $N$ harmonic-components are considered at the currents flowing through the resonant circuits as
\[ \frac{R_{ij}}{V_I}(\theta) = \sum_{k=1}^{N} (a_{kj} \cos(k\theta) + b_{kj} \sin(k\theta)), \quad \text{for } j = 1 \text{ and } 2. \] (1)

Because the output current is the sum of \( i_1 \) and \( i_2 \), we have

\[ \frac{R_{i_s}}{V_I}(\theta) = \sum_{k=1}^{N} [(a_{k1} + a_{k2}) \cos(k\theta) + (b_{k1} + b_{k2}) \sin(k\theta)]. \] (2)

### 3.4 Switch voltage waveform

While the switch is off, switch voltage occurs due to the current flowing through the shunt capacitance connected in parallel. The normalized switch voltage is expressed as

\[
\frac{v_{S1j}(\theta)}{V_I} = -A^2 BQ \int_{\theta_0}^{\theta} \frac{R_{i_{Cj}}}{V_I} d\theta = -A^2 BQ \int_{\theta_0}^{\theta} \sum_{k=1}^{N} (a_{kj} \cos(k\theta) + b_{kj} \sin(k\theta)) d\theta, \tag{3}
\]

\[
\begin{cases}
0, & \text{for } (j-1)\phi < \theta < (j-1)\phi + 2\pi D \\
-A^2 BQ \sum_{k=1}^{N} \frac{1}{k} (f_{kj}(k\theta) - f_{kj}(k(j-1)\phi + 2\pi D)), & \text{for } (j-1)\phi + 2\pi D \leq \theta < \theta_{1j} - \pi \\
1, & \text{for } \theta_{1j} - \pi \leq \theta < \theta_{2j} - \pi \\
1 - A^2 BQ \sum_{k=1}^{N} \frac{1}{k} (f_{kj}(k\theta) - f_{kj}(k\theta_{2j})), & \text{for } \theta_{2j} - \pi \leq \theta < \pi + (j-1)\phi \\
1, & \text{for } \pi + (j-1)\phi \leq \theta < \pi + (j-1)\phi + 2\pi D \\
1 - A^2 BQ \sum_{k=1}^{N} \frac{1}{k} (f_{kj}(k\theta) - f_{kj}(k(j-1)\phi + 2\pi D)), & \text{for } \pi + (j-1)\phi + 2\pi D \leq \theta < \theta_{1j} \\
0, & \text{for } \theta_{1j} \leq \theta < \theta_{2j} \\
-A^2 BQ \sum_{k=1}^{N} \frac{1}{k} (f_{kj}(k\theta) - f_{kj}(k\theta_{2j})), & \text{for } \theta_{2j} \leq \theta < 2\pi + (j-1)\phi
\end{cases}
\]

where \( f_{kj}(\theta) \) is

\[ f_{kj}(\theta') = a_{kj} \sin(\theta') - b_{kj} \cos(\theta'). \] (4)

Note that the above equations are independent of the switching patterns for substituting \( \theta_{1j} = \theta_{2j} = 2\pi + (j-1)\phi \) for Pattern 1 and \( \theta_{2j} = 2\pi + (j-1)\phi \) for Pattern 2.

Applying the Fourier series expansion to \( v_{Sj} \) in Eq. (3), we have analysis expression of the normalized switch voltage, which is defined in the range of \( 0 \leq \theta < 2\pi \) as

\[
\frac{v_{S1j}}{V_I} = \sum_{k=1}^{N} (c_{kj} \cos(k\theta) + d_{kj} \sin(k\theta)). \tag{5}
\]

The resulting equations of \( c_{kj} \) and \( d_{kj} \), which are the function of \( a_{kj}, b_{kj}, \theta_{1j}, \) and \( \theta_{2j} \), are given in Appendix.

### 3.5 Equivalent circuit

By using the normalized switch voltage equation in Eq. (5) and defined parameters, a dimensionless equivalent circuit model can be established. Figure 4 shows the equivalent circuit model of the phase-controlled class-D inverter.

By applying KVL to the loops in the equivalent circuit model in Fig. 4, we obtain the another expressions of the switch voltage as
\[
\frac{v_{Sj}}{V_t} = Q \frac{d}{d\theta} \frac{R_{ij}}{V_t} + A^2 Q \int_0^{2\pi} \frac{R_{ij}}{V_t} d\theta + \frac{R}{V_t} (i_1 + i_2)
\]
\[
= \sum_{k=1}^{N} \left\{ \left( a_{k1} + a_{k2} \right) + \left( kQ - \frac{A^2 Q}{k} \right) b_{kj} \right\} \cos(k\theta) + \left[ b_{k1} + b_{k2} \right] - \left( kQ - \frac{A^2 Q}{k} \right) a_{kj} \right\} \sin(k\theta) \right\}.
\]

Comparing the coefficients between Eqs. (5) and (6), we have

\[
Q \text{ loop}_1 \quad 1/AQ \quad 1/AQ \quad Q
\]
\[
\begin{align*}
\frac{v_{Sj}}{V_t} & = \sum_{k=1}^{N} \left\{ \left( a_{k1} + a_{k2} \right) + \left( kQ - \frac{A^2 Q}{k} \right) b_{kj} \right\} \cos(k\theta) + \left[ b_{k1} + b_{k2} \right] - \left( kQ - \frac{A^2 Q}{k} \right) a_{kj} \right\} \sin(k\theta) \right\}.
\end{align*}
\]

**Fig. 4.** Equivalent model of the phase-controlled the class-D inverter.

\[
c_{kj} = (a_{k1} + a_{k2}) + \left( kQ - \frac{A^2 Q}{k} \right) b_{kj}
\]

and

\[
d_{kj} = (b_{k1} + b_{k2}) - \left( kQ - \frac{A^2 Q}{k} \right) a_{kj}
\]

Because of \( j = 1 \) and \( 2 \) and \( k = 1, 2, \cdots, N \), we have \( 4 \times N \) relationships in Eqs. (7) and (8).

### 3.6 Derivation of switching pattern and current coefficients

Additionally, \( \theta_{ij} \) and \( \theta_{2j} \) should be determined for obtaining the waveforms. For that, it is necessary to comprehend the relationships among \( \theta_{1j}, \theta_{2j} \), and the switching patterns, which can be expressed as:

\[
\theta_{1j} = \theta_{2j} = 2\pi + (j-1)\phi \quad \text{in Pattern 1}
\]

\[
\begin{align*}
\left\{ \frac{v_{Sj}}{V_t}(\theta_{1j}) = 1 - A^2 BQ \sum_{k=1}^{N} \frac{1}{k} (f_{kj}(k\theta_{1j}) - f_{kj}(k(j - 1)\phi + 2\pi D)) = 0, \quad \text{in Pattern 2} \right. \\
\theta_{2j} = 2\pi + (j-1)\phi,
\end{align*}
\]

and

\[
\begin{align*}
\left\{ \frac{v_{Sj}}{V_t}(\theta_{1j}) = 1 - A^2 BQ \sum_{k=1}^{N} \frac{1}{k} (f_{kj}(k\theta_{1j}) - f_{kj}(k(j - 1)\phi + 2\pi D)) = 0, \quad \text{in Pattern 3} \right. \\
\frac{R_i D_{1j}}{V_t}(\theta_{2j}) = \sum_{k=1}^{N} (a_{kj} \sin(k\theta_{2j}) + b_{kj} \cos(k\theta_{2j})) = 0.
\end{align*}
\]

By solving \((4N+4)\) equations, namely Eqs. (7), (8) and the above relationships simultaneously, \((4N+4)\) unknown variables, which are the current coefficients \( a_{kj} \) and \( b_{kj} \) and the anti-parallel-diodes switching instants \( \theta_{1j} \) and \( \theta_{2j} \) can be fixed uniquely. In this paper, Newton’s method is applied for solving the algebraic equations.

For obtaining the final waveforms, however, some iterative calculations are necessary in order to determine the switching pattern. Figure 5 shows a flowchart for determining the switching patterns of each inverter. First, the waveforms are derived with assumption that both bottom-switch voltage waveforms are in Pattern 1. When \( v_{S1j} \) under the assumption of Pattern 1 become negative in the range of \( 0 < \theta < 2\pi \), the switch \( S_{1j} \) is re-assumed to work in Pattern 2 and the waveforms are newly
obtained with the updated assumption. If both \( v_{S1j} \) and \( v_{S2j} \) always positive, the waveforms are the final solutions. In the next step, when the newly obtained switch-voltage waveform assumed as Pattern 2 satisfies \( i_{D1j} > 0 \) at \( \theta = 2\pi + (j - 1)\phi \), the switch \( S_{1j} \) is considered to be in Pattern 3. With the above calculations, it is possible to finalize the switching patterns of each inverter and to derive the correct waveforms.

The above calculations are mandatory because the Newton’s method is used in order to derive the coefficient values. If we don’t follow the flowchart in Fig. 5, there are cases that Newton’s method is diverged.

3.7 Harmonic-component number

Obviously, the accuracy of the waveforms increases as the increase in the harmonic-component number \( N \). The computation cost, however, also increases as the increase in \( N \). Therefore, it is necessary to determine the proper value of \( N \). For example, the waveforms are drawn at fixed \( N \). Waveforms for \( N = \infty \) is obtained from PSpice simulations. Figure 6 shows the resonant-current waveforms for \( A = 0.94, B = 3.0, D = 0.4 \) and \( Q = 10 \) at fixed \( \phi \). It is seen from Fig. 6(a) that the waveforms are independent of \( N \) for \( \phi = 0 \). This is because a pair of inverters work with symmetry and high \( Q \) characteristics can be obtained. In Fig. 6(b), however, the waveforms of \( i_{2R_L}/V_I \) strongly depends on \( N \). This means the sufficient harmonic components are included in the resonant current. Additionally, it is also seen that the waveforms with \( N = 5 \) almost the same as that with \( N = \infty \). In this paper, \( N = 5 \) is adopted for waveform derivations.
4. ZVS region, output power and power-conversion efficiency

4.1 ZVS region

This paper aims to design the phase-controlled class-D inverter that satisfies the ZVS condition at any phase shift. By deriving the parameters that form the boundary of a switching state, the ZVS region is visualized over the parameter space.

The waveform that forms a boundary between the ZVS and the non-ZVS can be expressed specifically, as shown in Figs. 3(d) and (e). Patterns 1 and 3 are in the non-ZVS state, and the ZVS region can be represented graphically by calculating the boundary between Patterns 1 and 2 and between Patterns 2 and 3. Figure 3(d) shows the waveform that forms the boundary between Patterns 1 and 2. In this state, the switch voltage reaches zero at the instant that the switch is turns on, namely

\[ \frac{v_{S1}}{V_I}(2\pi) = 0, \]

or

\[ \frac{v_{S2}}{V_I}(\phi) = 0. \]

By contrast, Fig. 3(e) shows the waveform that forms the boundary between Patterns 2 and 3. In this state, the current \( i_{D1} \) that flowing through an anti-parallel diode become zero at switch turn-on instant, namely

\[ \frac{R i_{D1}}{V_I}(2\pi) = 0, \]

or

\[ \frac{R i_{D2}}{V_I}(\phi) = 0. \]

Figure 7 shows the set of parameter \( A \) and \( B \) that satisfies conditions Eqs. (12)–(15) for \( \phi = \pi/6 \). As shown in the Fig. 7, the ZVS region can be visualized by drawing a boundary line over the parameter space. Additionally, it is seen from Fig. 7 the boundary for inverter 2 forms a narrower ZVS region than the boundary at inverter 1. In other words, when the ZVS region for the inverter 2 are obtained, the region forms the ZVS regions for both the inverters 1 and 2. It can be confirmed that the ZVS region of inverter 2 is always equal to or narrower than that of inverter 1 for all the phase shift.

This paper treats parameters \( A \) and \( B \) as the design parameters and draws the ZVS region over parameter spaces \( A \) and \( B \). At this point, the phase shift is adjusted from 0 to 180 degrees by 1 degree increments, and a region diagram is developed each time. Each region diagram can be derived quickly because a steady-state analysis formula obtained on the previous section is used. Figure 8(a) shows the ZVS region for fixed phase shift in parameter spaces \( A \) and \( B \). By overlapping the ZVS from every phase shift, the common region becomes the parameter at which ZVS can be achieved at any phase shifts. Figure 8(b) shows the ultimately calculated region for parameters \( A \) and \( B \) that achieves the ZVS. Note that the ZVS region diagrams are formulated with dimensionless parameters. The figure is useful for various design specifications because Fig. 7 and 8 do not depend on the design specifications.

4.2 Output power

The output power \( P_o \) is expressed as

\[ \frac{R P_o}{V_I^2} = \frac{1}{2\pi} \int_0^{2\pi} \left\{ \sum_{k=1}^{N} \left[ (a_{k1} + a_{k2}) \cos(k\theta) + (b_{k1} + b_{k2}) \sin(k\theta) \right] \right\}^2 d\theta \]

\[ = \frac{1}{2\pi} \sum_{k=1}^{N} \pi \left[ (a_{k1} + a_{k2})^2 + (b_{k1} + b_{k2})^2 \right]. \]

By solving

\[ \frac{R P_o}{V_I^2} - \frac{R P_{oc}}{V_I^2} = 0, \]

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Fig. 7. \( B \) as a function of \( A \) for satisfying Eqs. (12)–(15) on the parameter space \( A \) and \( B \).

Fig. 8. ZVS region on the parameter space \( A \) and \( B \). (a) Boundary of the ZVS or non-ZVS regions for fixed phase shift. (b) ZVS region for satisfying any phase shift.

Fig. 9. ZVS region and the maximum output power on the parameter space \( A \) and \( B \).

The contour lines of the output power for the fixed \( \phi \) can be drawn over the parameter space. Where, \( P_{\text{or}} \) is the rated output power. Figure 9 overlaps the output-power contour lines for fixed \( \phi = 0 \) and the ZVS region. It is seen Fig. 9 that the output power is sensitive to parameter \( A \). The contour lines in Fig. 9 agrees with the intuition that the power increases as the resonant frequency reaches closer to the operating frequency.
4.3 Output power-loss analysis and power-conversion efficiency

Figure 10 shows equivalent circuit of the phase-controlled class-D inverter for power-loss analysis. This paper considers the power losses in on-resistances \( r_{Sj} \) of the MOSFET, equivalent series resistance (ESRs) of the shunt capacitance \( r_{C_{Sj}} \), and series resonant filter \( r_{LC_{j}} \), and antiparallel diodes of the MOSFETs. The power losses in the ESRs of the shunt capacitance and the resonant filter are obtained from

\[
\frac{R_{PC_{Sj}}}{V_{I}^{2}} = \frac{r_{C_{Sj}}}{R} \frac{1}{2\pi} \int_{0}^{2\pi} \left( \frac{R_{i_{j}}}{V_{I}} \right)^{2} d\theta \\
= \frac{r_{C_{Sj}}}{2\pi R} \left[ \int_{0}^{\theta_{1}} \sum_{k=1}^{N} (a_{kj} \cos(k\theta) + b_{kj} \sin(k\theta)) \right]^{2} d\theta \\
+ \int_{\theta_{2}}^{2\pi} \sum_{k=1}^{N} (a_{kj} \cos(k\theta) + b_{kj} \sin(k\theta))^{2} d\theta, \tag{18}
\]

and

\[
\frac{R_{PLC_{j}}}{V_{I}^{2}} = \frac{r_{LC_{j}}}{R} \frac{1}{2\pi} \int_{0}^{2\pi} \left( \frac{R_{i_{j}}}{V_{I}} \right)^{2} d\theta \\
= \frac{r_{LC_{j}}}{2\pi R} \sum_{k=1}^{N} \pi(a_{kj}^{2} + b_{kj}^{2})^{2}, \tag{19}
\]

respectively. Additionally, power losses in the MOSFET should be considered. By considering waveform symmetry between the bottom and top switches, the condition loss in the MOSFET on-resistance is

\[
\frac{R_{PS_{j}}}{V_{I}^{2}} = \frac{r_{Sj}}{R} \frac{1}{2\pi} \int_{0}^{2\pi} \left( \frac{R_{i_{j}}}{V_{I}} \right)^{2} d\theta \\
= \frac{r_{Sj}}{2\pi R} \int_{0}^{2\pi} \left[ \sum_{k=1}^{N} (a_{kj} \cos(k\theta) + b_{kj} \sin(k\theta)) \right]^{2} d\theta. \tag{20}
\]

In Pattern 1 and 3, the switching losses occur, which are expressed as

\[
\frac{R_{PSW_{j}}}{V_{I}^{2}} = \frac{1}{2} \frac{1}{A^{2}BQ} \left[ \frac{v_{S1j}(2\pi + (j - 1)\phi)}{V_{I}} \right]^{2} \frac{1}{2\pi} \\
= \frac{1}{4\pi A^{2}BQ} \left[ -A^{2}BQ \sum_{k=1}^{N} \frac{1}{k} (f_{kj}((2\pi + (j - 1)\phi)k) - f_{kj}(k\theta_{2j})) \right]^{2} \\
= \frac{A^{2}BQ}{4\pi} \sum_{k=1}^{N} \frac{1}{k} \left[ b_{kj} \cos(k\theta_{2j}) - b_{kj}^{2} - a_{kj}^{2} - a_{kj}^{2} \sin(k\theta_{2j})) \right], \tag{21}
\]

Finally, the power losses in antiparallel diode, which occur in Pattern 2 and 3, are expressed as The power loss in antiparallel diode is expressed as

\[
\frac{R_{PD_{j}}}{V_{I}^{2}} = \frac{V_{d}}{V_{I}} \frac{1}{2\pi} \int_{0}^{2\pi} \frac{R_{i_{D}}}{V_{I}} d\theta \\
= \frac{V_{d}}{2\pi V_{I}} \left\{ \sum_{k=1}^{N} \frac{1}{k} \left[ a_{kj} \sin(k\theta_{2j}) - \sin(k\theta_{1j})) + b_{kj} \cos(k\theta_{1j}) - \cos(k\theta_{2j})) \right] \right\}, \tag{22}
\]

where \( V_{d} \) is the forward voltage of the antiparallel diode. From Eqs. (20)–(22), total power loss of the phase-controlled class-D inverter is

\[
P_{loss} = \sum_{j=1}^{2} (P_{CS_{j}} + P_{LC_{j}} + P_{S_{j}} + P_{SW_{j}} + P_{D_{j}}). \tag{23}
\]
The power-conversion efficiency can be obtained analytically from

\[ \eta = \frac{P_o}{P_o + P_{loss}}. \]  

(24)

5. Experiment results

This section shows experimental measurements for confirming the validities of the analytical expressions. The fundamental specifications of the designed inverters are operating frequency \( f = 1 \) MHz, duty ratio \( D = 0.4 \), load resistance \( R = 25 \) Ω, and loaded quality factor \( Q = 10 \).

5.1 Validity of analytical expressions

Figure 11 shows the experimental and analytical waveforms for the several phase-controlled class-D inverter for fixed \( A \) and \( B \). The design parameters are marked in Fig. 7. It is seen from Fig. 11 that all the experimental waveforms agreed with the analytical predictions. Additionally, each experimental switch voltage showed the predicted switching pattern. For example, it is predicted from Fig. 7 that switch voltages of the inverters 1 and 2 for \( A = 0.96 \) and \( B = 3.5 \) are in Patterns 2 and 3, respectively. This is because the parameter is located at the right-hand side of the boundary line between Patterns 2 and 3 for \( v_{S22} \) and at the left-hand side of the boundary line for \( v_{S12} \). It can be confirmed from Fig. 11(b) that the experimental waveforms showed the predicted switching pattern correctly. The results in Fig. 11 showed the validity of the analysis formula and the ZVS region diagram.
5.2 Design of the phase-controlled ZVS class-D inverter

The phase-controlled class-D ZVS inverter was designed and implemented. The output power varies from 0 to 50 W, and the ZVS is achieved at any output powers. From Fig. 9, $A = 0.94$ and $B = 2.1$ are selected in order to satisfy the ZVS condition at any phase shifts and to obtain the large output power. From the selected parameters and the specifications, the component values are calculated as given in Table I. Because of $R_{cp}/V_{L}^2 = 0.15$, the input voltage needs at least $V_I = 91.3$ V to achieve 50 W of output power at $\phi = 0$. From the analysis formula, the maximum current flowing through the switch can be estimated as 1.96 A. From the maximum switch voltage, which is the same as the input voltage, and the maximum switch current, IRF510 MOSFET was selected as the switching device. Table II gives the characteristics of IRF510 MOSFETs, which were obtained from the datasheet.

Figure 12 shows experimental and analytical waveforms at $\phi = 0$, $\phi = \pi/6$, and $\phi = \pi$. The experimental waveforms were measured using a Tektronix MDO4054-3 oscilloscope, and current waveforms were measured using a Tektronix TCP2020 current probe. Figure 12 shows that all the switch voltages achieved the ZVS regardless of the phase shift. Based on these results, the ZVS region diagram drawn in the Fig. 12 was validated.

| Table I. | Design value of the phase-controlled class-D inverter. |
|----------|-----------------------------------------------------|
|          | Analytical | Measured | Difference |
| $V_I$    | 91.3 V     | 91.3 V   | 0.00%      |
| $R$      | 25 $\Omega$| 25 $\Omega$| 0.00%      |
| $f$      | 1 MHz      | 1 MHz    | 0.00%      |
| $D$      | 0.4        | 0.4*     | —          |
| $C_{S1}$ | 0.24 nF    | 0.24 nF  | 0.00%      |
| $C_{S2}$ | 0.24 nF    | 0.25 nF  | 0.03%      |
| $C_{r1}$ | 0.73 nF    | 0.70 nF  | 0.04%      |
| $C_{r2}$ | 0.73 nF    | 0.70 nF  | 0.04%      |
| $L_{r1}$ | 39.0 $\mu$H| 38.1 $\mu$H | 2.31%   |
| $L_{r2}$ | 39.0 $\mu$H| 38.2 $\mu$H | 2.05%   |

The measured duty ratio is the duty ratio of the function generator of Tektronix AFG3022, whose signal was the input signal of the MOSFET driver.

| Table II. | Characteristics of IRF510 MOSFET. |
|-----------|----------------------------------|
| Maximum Drain-Source voltage $V_{dsmax}$ | 100 V |
| Maximum Drain-Source current $I_{dsmax}$ | 5.6 A |
| On-resistance $r_s$ | 0.56 $\Omega$ |
Fig. 13. Output power and power-conversion efficiency as a function of the phase shift for $A = 0.94$ and $B = 2.1$.

Figure 13 shows the output power and power-conversion efficiency as a function of phase shift $\phi$. For measuring the power conversion efficiency, the output voltage $V_o$ was measured by Tektronix MDO4054-3 oscilloscope. Additionally, the input voltage $V_I$ and input current $I_I$ were measured by the Iwatsu VOAC7523 digital multimeter. The output power could be adjusted from 49.8 W to 0 with phase shift from 0 to $\pi$ with keeping ZVS. These measurement results showed the validity and effectiveness of the proposed design method.

It is seen from Fig. 13 that the experimental results agreed with the theoretical predictions quantitatively in terms of the output power and power-conversion efficiency. Figure 13(b) showed the validity and accuracy of the power-loss analysis. In the experimental measurements, the power-conversion efficiency was 97.1% at 49.8 W and 1 MHz output.

6. Conclusion

This paper has proposed an analysis and design method of the phase-controlled class-D inverter. To derive the ZVS region diagram, the steady-state waveform of the phase-controlled class-D inverter is analytically derived. Waveforms at any phase shifts can be expressed accurately because this analysis introduces an expression of an anti-parallel diode behavior and multiple-harmonic analysis. The circuit parameters that satisfies the boundary condition between the ZVS and the non-ZVS at a given phase shift are derived by using the obtained waveform formula, to graphically represent the ZVS region. The validities of the analysis formula and design method proposed in this paper were verified through the experiments and by collating the quantitative values obtained from the experiments and analysis.

Appendix

The resulting equations of $c_{kj}$ and $d_{kj}$ in Eq. (5) are expressed as

$$c_{kj} = \frac{1}{\pi} \left\{ \frac{1}{k} \left[ 1 - (-1)^k \sin(k\theta_{1j}) \right] + A^2 B Q \left[ \sum_{k=1, m \neq k}^{N} (F_j + G_j) - \frac{b_{kj}}{2k} T_j + \sum_{m=1}^{N} M_j + U_j \right] \right\}$$

(A-1)

and

$$d_{kj} = \frac{1}{\pi} \left\{ \frac{1}{k} \left[ (-1)^k \cos(k\theta_{1j}) - 1 \right] + A^2 B Q \left[ \sum_{k=1, m \neq k}^{N} (H_j + K_j) + \frac{a_{kj}}{2k} T_j + \sum_{m=1}^{N} O_j + W_j \right] \right\}$$

(A-2)
where

\[ T_j = \theta_{1j} - \theta_{2j} + \pi + (j - 1)\phi - 2\pi D + (j - 1)\phi, \quad (A-3) \]

\[ F_j = \frac{[1 + (-1)^{m+k}]}{2m^2 + k} \begin{bmatrix} \cos((m + k)(2\pi D + (j - 1)\phi)) \\ \cos((m + k)\theta_{1j}) \\ \cos((m + k)\theta_{2j}) \\ \cos((m + k)(j - 1)\phi) \\ \sin((m + k)(2\pi D + (j - 1)\phi)) \\ \sin((m + k)\theta_{1j}) \\ \sin((m + k)\theta_{2j}) \\ \sin((m + k)(j - 1)\phi) \end{bmatrix}^T \begin{bmatrix} a_{mj} \\ -a_{mj} \\ a_{mj} \\ -a_{mj} \\ b_{mj} \\ -b_{mj} \\ b_{mj} \\ -b_{mj} \end{bmatrix}, \quad (A-4) \]

\[ G_j = \frac{[1 + (-1)^{m-k}]}{2m^2 - k} \begin{bmatrix} \cos((m - k)(2\pi D + (j - 1)\phi)) \\ \cos((m - k)\theta_{1j}) \\ \cos((m - k)\theta_{2j}) \\ \cos((m - k)(j - 1)\phi) \\ \sin((m - k)(2\pi D + (j - 1)\phi)) \\ \sin((m - k)\theta_{1j}) \\ \sin((m - k)\theta_{2j}) \\ \sin((m - k)(j - 1)\phi) \end{bmatrix}^T \begin{bmatrix} a_{mj} \\ -a_{mj} \\ a_{mj} \\ -a_{mj} \\ b_{mj} \\ -b_{mj} \\ b_{mj} \\ -b_{mj} \end{bmatrix}, \quad (A-5) \]

\[ H_j = \frac{[1 + (-1)^{m+k}]}{2m^2 + k} \begin{bmatrix} \sin((m + k)(2\pi D + (j - 1)\phi)) \\ \sin((m + k)\theta_{1j}) \\ \sin((m + k)\theta_{2j}) \\ \sin((m + k)(j - 1)\phi) \\ \cos((m + k)(2\pi D + (j - 1)\phi)) \\ \cos((m + k)\theta_{1j}) \\ \cos((m + k)\theta_{2j}) \\ \cos((m + k)(j - 1)\phi) \end{bmatrix}^T \begin{bmatrix} a_{mj} \\ -a_{mj} \\ a_{mj} \\ -a_{mj} \\ b_{mj} \\ -b_{mj} \\ b_{mj} \\ -b_{mj} \end{bmatrix}, \quad (A-6) \]

\[ K_j = \frac{[1 + (-1)^{m-k}]}{2m^2 - k} \begin{bmatrix} \sin((m - k)(2\pi D + (j - 1)\phi)) \\ \sin((m - k)\theta_{1j}) \\ \sin((m - k)\theta_{2j}) \\ \sin((m - k)(j - 1)\phi) \\ \cos((m - k)(2\pi D + (j - 1)\phi)) \\ \cos((m - k)\theta_{1j}) \\ \cos((m - k)\theta_{2j}) \\ \cos((m - k)(j - 1)\phi) \end{bmatrix}^T \begin{bmatrix} a_{mj} \\ -a_{mj} \\ a_{mj} \\ -a_{mj} \\ b_{mj} \\ -b_{mj} \\ b_{mj} \\ -b_{mj} \end{bmatrix}, \quad (A-7) \]

\[ M_j = \frac{1}{k} \begin{bmatrix} ((-1)^m + (-1)^k) \sin(k\theta_{1j}) \\ (1 + (-1)^{m+k}) \sin(k(2\pi D + (j - 1)\phi)) \\ (1 + (-1)^{m+k}) \sin(k(j - 1)\phi) \end{bmatrix}^T \begin{bmatrix} -a_{mj} \\ a_{mj} \\ -a_{mj}\theta_{2j} \\ a_{mj}\theta_{2j} \end{bmatrix}, \quad (A-8) \]

\[ O_j = \frac{1}{k} \begin{bmatrix} ((-1)^m + (-1)^k) \cos(k\theta_{1j}) \\ (1 + (-1)^{m+k}) \cos(k(2\pi D + (j - 1)\phi)) \\ (1 + (-1)^{m+k}) \cos(k(j - 1)\phi) \end{bmatrix}^T \begin{bmatrix} a_{mj} \\ -a_{mj} \\ a_{mj}\theta_{2j} \\ -a_{mj}\theta_{2j} \end{bmatrix}, \quad (A-9) \]
\[
U_j = \frac{1}{2k^2} \begin{bmatrix}
\cos(2k(2\pi D + (j-1)\phi)) & a_{mj} \\
\cos(2k\theta_1j) & -a_{mj} \\
\cos(2k\theta_2j) & a_{mj} \\
\cos(2k(j-1)\phi) & -a_{mj} \\
\sin(2k(2\pi D + (j-1)\phi)) & b_{mj} \\
\sin(2k\theta_1j) & -b_{mj} \\
\sin(2k\theta_2j) & b_{mj} \\
\sin(2k(j-1)\phi) & -b_{mj}
\end{bmatrix}^T, \quad (A-10)
\]

and

\[
W_j = \frac{1}{2k^2} \begin{bmatrix}
\sin(2k(2\pi D + (j-1)\phi)) & a_{mj} \\
\sin(2k\theta_1j) & -a_{mj} \\
\sin(2k\theta_2j) & a_{mj} \\
\sin(2k(j-1)\phi) & -a_{mj} \\
\cos(2k(2\pi D + (j-1)\phi)) & b_{mj} \\
\cos(2k\theta_1j) & -b_{mj} \\
\cos(2k\theta_2j) & b_{mj} \\
\cos(2k(j-1)\phi) & -b_{mj}
\end{bmatrix}^T. \quad (A-11)
\]

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