A high efficient CTLE for 12.5 Gbps receiver of JESD204B standard

Gang Chen¹,², Min Gong¹, Dongbing Fu², and Junan Zhang³

¹ School of Physical Science and Technology, University of Sichuan, Chendu 610064, China
² Science and Technology on Analog Integrated Circuit Laboratory, Chongqing 400060, China
³ School of Electrical and Electronic Engineering, Chongqing University of Technology, Chongqing 400054, China

Abstract: A 12.5 Gbps continuous-time linear equalizer circuit (CTLE) constructed with two stage equalizer, three stages of limiting amplifier and designed in 55 nm CMOS technology for high speed serial interface of JESD204B standard is presented. Beside using degeneration RC pair to compensate low pass response of the channel and high frequency signal loss, the first equalizer also utilizes inductive shunt peaking technology to further extend the bandwidth of input signals. The proposed circuit was simulated with post layout parasitic extraction and achieves around 20 ps peak-to-peak jitter, 1.08 V voltage swing and a data rate of 12.5 Gbps through 10-inch FR-4 PCB trace with the characteristic of low equalization power consumption.

Keywords: SerDes, CTLE, high speed serial link, electrical channel attenuation, internal symbol interference (ISI), BER, equalizer

Classification: Integrated circuits

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1 Introduction

Wire-line communication speed between two devices increases rapidly as the fabricating technology process scaling. The JESD204B serial link interface has been widely integrated in high speed analog to digital converter (ADC) and digital to analog converter (DAC) due to its low cost and high bandwidth. However, the signal frequency-dependent insertion loss in serial link channels has become the major limiter as skin effect, dielectric loss and coupling loss existing in the communication channels, causing intersymbol interference (ISI) which is the bottleneck for high speed-rate and long distance communication. In order to maximize the channel bandwidth utilization rate and improve the performance of transmission system, equalization technologies such as decision feedback equalizer (DFE) [3, 4, 7, 9] and continuous-time equalizer (CTLE) [2, 5, 6, 8, 10] have been utilized to compensate the non-ideal characteristic in the receiver side. The equalizer can compensate the useful frequency component in the Nyquist frequency range, and restrain ISI even with channel conditions and process-voltage-temperature variations.

The frequency response of a CTLE is essentially a continuous-time high-pass filter which amplifies the high frequency signal component around Nyquist frequency of transmitted signal, opposing to low pass response of channel. Thus, CTLE can restrain pre-cursor and post-cursor efficiently and potentially suppress the high-frequency noise of subsequent stages. Unlike linear equalization, a DFE eliminates the ISI by taking the quantized previous input values and utilizing the decision to substrate the input signal with proper weighting. However, a DFE has the potential to propagate error if noise is large enough for quantized output to be wrong. Also, owing to the feedback equalization structure, the DFE cannot cancel pre-cursor ISI. One of the key design challenges in DFE implementation is closing the feedback loop within a timing margin of 1 bit period or unit interval (UI). Therefore, A CTLE is more preferable when error requirement and power consumption is stringent in the serial communication system.

This paper presents a 12.5 Gb/s continuous-time linear equalizer applied in the standard of JESD204B receiver to compensate the channel signal loss at the front of...
CDR (clock and data recovery) circuit. To improve the performance of equalization, RC-degeneration pair and inductive peaking technology is used in the circuit which results in low power consumption.

2 CTLE architecture and implementation

The propose of the CTLE focuses on 12.5 Gbps data rate communication over 10-inch FR4 backplane PCB trace, which is used to compensate high frequency signal loss with low power consumption. The low pass channel constructs with three parts, the PCB trace, wire banding and electric static discharge (ESD) circuit which contributes parasitic capacitance and additional resistance to the channel and attenuates the quality of high frequency signals. By constructing the channel model, the signal loss of our target channel is 19 dB at 12.5 Gbps after simulation. The proposed CTLE is designed to obtain larger than 19 dB equalizing gain at 12.5 Gbps. Fig. 1 shows the overall structure of the proposed CTLE. It has two stages of linear equalizer, three stages of limiting amplifiers and a DC feedback path which provides a DC bias voltage to the first stage equalizer. The first equalizer in the front-end uses RC-degeneration zero peaking and inductive shunt peaking technologies to expand the high frequency response compared with ordinary structure. The second equalizer only uses degeneration RC pair to provide more gain boost at higher frequency. The capacitors connected between the output of EQ1 and the input of EQ2 forms Miller capacitors, cancel out some gate parasitic capacitor of EQ2 and reduce the capacitance load of the first stage equalizer.

2.1 The first stage equalizer

Continuous-time equalizer usually is used to implement a transfer function that is opposite to the lossy channel response function. Fig. 2 shows the first stage equalizer used in the CTLE circuit. The gain of conventional equalizer without inductor is

$$A_E = \frac{g_m R_L}{sC_L R_L + 1} \cdot \frac{g_m (sC_d R_D + 1)}{sC_d R_D + 1 + g_m R_D}$$

(1)

As can be seen from The Eq. (1), there are a zero and two poles in the equation. If let the zero equals to $1/C_L R_L$, the pole can be canceled out, and the new pole becomes $(1 + g_m R_D)/R_c C_D$. Comparing with original pole $1/C_L R_L$, the bandwidth increases $1 + g_m R_D$, and the low frequency gain decreases to $g_m R_L/(1 + g_m R_D)$. 

![Proposed CTLE structure](image)
However, because the work frequency of proposed CTLE is above 12 GHz, the zero point $z = 1/C_d R_D$ cannot simply equals to $1/C_L R_L$. As for the equalizer presenting in this work, the zero point has been putted in the front as shown in the Fig. 3, where the dash curve shows the ideal response and the red curve shows the realistic response. The frequency response curve increases after the zero point until the effect of zero canceled out by dominant pole, and then the second pole let the curve decrease. The gain expression can be rewritten to Eq. (2)

$$A_E = \frac{g_m R_L}{1 + g_m R_D} \cdot \frac{s + 1}{\frac{s}{p_1} \left(1 + \frac{s}{p_1}\right) \left(1 + \frac{s}{p_2}\right)}$$

(2)

where $g_m R_L/(1 + g_m R_D)$ is the DC gain, $z = 1/C_d R_D$ is zero point, the dominant pole is $p_1 = (1 + g_m R_D)/R_D C_D$ and $p_2 = 1/C_L R_L$ is second pole. The ratio $p_1/z$ is gain factor, representing the degree of correction of signal spectrum by equalizer contract to DC gain. In the implementation, $C_d$, $R_D$ and bias current are adjustable to compact with different lane speed, so as to ensure the flexibility of the circuit. The product of DC gain, gain factor and second pole equals to $g_m/C_L$ that is the CMOS process cut off frequency, extending the second pole at the expense of degenerating the other two.

The equalizer EQ1 has also used inductive shunt peaking to increase bandwidth. The gain is proportion to $g_m R_L$ for purely resistive load. When added a
capacitance load, the frequency gain will decrease as the frequency increase, since the capacitive impedance reduces as frequency increasing. However, cascading a inductor with resistor load introduces a zero point, compensating the capacitance impedance reduction. The overall impedance keep unchanged over a wide range of Nyquist frequency compared to the original RC network. At the view of time domain, the inductor delays the current flowing from resistor, making more current charge the capacitor, reducing rise time. Because a faster rise time means a larger useful bandwidth, selecting suitable inductor value can increase the bandwidth.

Fig. 4 shows the small signal analysis of single stage common-source amplifier. The bandwidth of circuit in Fig. 4(a) is \( \omega_1 = \frac{1}{RC} \), before compensating. After using the inductor shunt peaking technology, the impedance of circuit Fig. 4(d) can be written as

\[
Z(s)_d = (R + sL) || \left( \frac{1}{sC} \right) = \frac{R L}{s^2 L C + s R C + 1} \tag{3}
\]

Then, Adding two factors \( m = \frac{RC}{L/R} \), \( \tau = L/R \) and normalizing \( |Z(j\omega)| \) to R, the impedance value associated with the frequency becomes

\[
\frac{|Z(j\omega)|}{R} = \sqrt{\frac{(\omega R)^2 + 1}{(1 - \omega^2 \tau^2 m^2 + (\omega R m)^2}} \tag{4}
\]

Therefor,

\[
\frac{\omega_2}{\omega_1} = \sqrt{\left( -\frac{m^2}{2} + m + 1 \right) + \sqrt{\left( -\frac{m^2}{2} + m + 1 \right) + m^2}} \tag{5}
\]
Using the numeric analysis, the maximum value of Eq. (5) can be acquired when $m = \sqrt{2} = 1.414$, the bandwidth is 1.85 larger than the bandwidth before compensation without any power consumption by just adding a inductor into the circuit. However, when $m$ equals $\sqrt{2}$, the frequency response has a 20% peak value. Increasing the value of $m$ to seek the desirable bandwidth rather than maximizing bandwidth, a specific selection is that the impedance equals $R$ at the bandwidth without compensation. After calculation, $m = 2$ and bandwidth equals $\omega = \omega_1\sqrt{1 + \sqrt{5}} \approx 1.8\omega_1$ which is closed to the maximum value of Eq. (5) and the peak value reduces to 3%.

2.2 The second equalizer and limiting amplifier

Fig. 5(a) shows the second equalizer used in the proposed CTLE, which only utilizes source degenerated resistor and capacitor pair to compensate high frequency loss.

After processed by the equalizers, the signal is amplified by three subsequence cascade limiting amplifiers to provide compatible digital signal levels for the following processing, typically source coupled logic (SCL) levels. The structure of limiting amplifier used in the proposed CTLE is shown in the Fig. 5(b), which has the property of higher operation speed, low power consumption, easier design and smaller area and slightly higher input sensitivity.

3 Experimental results

The proposed CTLE circuit shown in Fig. 7, which is implemented in 55 nm CMOS process with 6 metal layers and 1.2 V supply voltage, occupying a area of 0.384 mm$^2$. Fig. 6 shows the simulation result of signal eye diagram transmitting in the nodes of channel and CTLE with typical condition. Fig. 6(a) to Fig. 6(c) shows the eye diagram at the nodes, which are the output 12.5 Gbps DC balanced signal from TX driver near PCB trace front-end, the end of PCB trace before package, and the input of first stage equalizer after banding wire. The jitter is increased from minimum value of 0.2 ps to 32 ps, and the voltage swing is decreased from 266 mV to 84 mV. Thus, due to the low-pass frequency response characteristic of channel,
constructed with PCB trace, package and wire banding, the signal loss is very significantly. After the signal passing through the proposed CTLE, the eye diagram of signal is gradually opening and noise is restrained, as it is shown from Fig. 6(d) to Fig. 6(g) at the internal nodes of CTLE. The jitter is reduced from 16 ps to 5 ps and the voltage swing is increased from 200 mV to 1080 mV when signal pass through EQ1, EQ2 and three cascade limiting amplifiers (LA). After post layout

Fig. 6. The simulation result of eye diagram from TX output to CTLE output with 10-inch PCB trace.

Fig. 7. The layout of proposed CTLE.
simulation with worst corner and 1 V voltage, the proposed CTLE still can achieve a peak-to-peak jitter of 20 ps.

Table I gives the performance of the proposed equalizer and lists with previously reported equalizers operating at around 12 Gbps. The proposed work has better power efficiency than [3, 8, 9], at the expensive of large area by adding inductors into the first stage equalizer to reduce power consumption.

| Table I. Comparison with recent designs |
|----------------------------------------|
| Technology (CMOS) | 110 nm | 65 nm | 110 nm | 55 nm |
| Filter type | CTLE | CTLE + 1-tap DFE | CTLE + 2-tap DFE | CTLE (EQ1+EQ2) |
| Data rate | 10 Gb/s | 21 Gb/s | 11.5 Gb/s | 12.5 Gb/s |
| Boosting gain (dB) | 20 | 11.7 | 21.7 | 19 |
| Core area (mm²) | 0.0156 | 0.04 | 0.014 | 0.384 |
| Supply voltage (V) | 1.2 | 1.2 | 1.3 | 1.2 |
| Power (mW) | 23.2 | 48 | 38 | 14.4 |

4 Conclusion

This work presents a CTLE circuit used in 12.5-Gb/s data rate JESD204B standard interface, with the property of low power, high bandwidth and easily implementation. The CTLE uses a equalizer with RC-degeneration and inductive shunt peaking technology at the front of input. The second stage equalizer provides additional high frequency gain booting for the input signal which only uses RC-degeneration pair. The simulation results demonstrate successfully transmission of 12.5-Gb/s data rate over 10-inch FR-4 PCB trace.