Feedback compensated 10 kW solid-state pulsed power amplifier at 352 MHz for particle accelerators

Cite as: Rev. Sci. Instrum. 90, 104707 (2019); https://doi.org/10.1063/1.5110981
Submitted: 22 May 2019. Accepted: 26 August 2019. Published Online: 17 October 2019

L. Hoang Duc, M. Jobs, T. Lofnes, R. Ruber, J. Olsson, and D. Dancila

ARTICLES YOU MAY BE INTERESTED IN

Pulse-width variation of power supply for evaluating quasi-steady state of magneto-plasma-dynamic thruster operation
Review of Scientific Instruments 90, 104706 (2019); https://doi.org/10.1063/1.5088084

Load sensitive stable current source for complex precision pulsed electroplating
Review of Scientific Instruments 90, 104704 (2019); https://doi.org/10.1063/1.5113790

Insulation improvement of an all-solid pulse forming line with film dielectric
Review of Scientific Instruments 90, 104705 (2019); https://doi.org/10.1063/1.5115178
Feedback compensated 10 kW solid-state pulsed power amplifier at 352 MHz for particle accelerators

L. Hoang Duc, M. Jobs, T. Lofnes, R. Ruber, J. Olsson, and D. Dancila

AFFILIATIONS
1 Angstrom Laboratory, Division of Solid-State Electronics, 751-21 Uppsala, Sweden
2 Angstrom Laboratory, Department of Physics and Astronomy, 751-20 Uppsala, Sweden

ABSTRACT
This paper presents the first results of an in-house developed low-level radio frequency (LLRF) system and a 10 kW solid state power amplifier (SSPA). The design approach for the SSPA is based on eight resonant single-ended kilowatt modules combined using a planar Gysel combiner. Each of the single-ended modules is based on a two-stepped impedance resonant matching, allowing for harmonic suppression, simple design for massive production, and high-performance design. A design methodology to tune SSPA modules for optimum combining efficiency is presented thoroughly in the time domain. We characterize the power droop due to capacitor banks in the time domain. In open loop of compensation, it is about 1 kW within the pulse of peak value 10 kW and a duration of 3.5 ms. This may lead to the beam instability of the accelerator as particles are not provided with the same energy during the pulse. By incorporating our LLRF system, it is demonstrated that the objective of amplitude and phase stability is satisfied, as required in the European Spallation Source proton accelerator. The presented design also offers the advantages of compact form factor, low complexity, and better performance. In closed loop compensation, the variation of amplitude (pulse droop) is measured on the order of 20 W, which is equivalent to 0.2% at 10 kW peak output power.

I. INTRODUCTION
Radio frequency (RF) vacuum tubes, i.e., klystrons, tetrodes, and Inductive Output Tubes (IOTs), are used to power particle accelerators operated in the frequency range from megahertz to gigahertz. The continuous innovation of solid-state technology allows foreseeing the replacement of these vacuum tubes in the frequency range up to around 2 GHz. The main driver for the adoption of the solid-state technology is the higher reliability of solid state devices operated at two or three orders of magnitude lower voltage supply than vacuum tubes. Solid-state-power-amplifier based power sources have an inherent high degree of modularity and have proven to operate with superior performance regarding high efficiency, i.e., 75%, better linearity, lower harmonics, cost effectiveness, and simple start-up procedures. Klystrons remain advantageous for megawatt level applications, while solid-state technology has already been a mainstream technology of choice for midpower range applications of several hundreds of kilowatt. The synchrotron SOLEIL pioneered the development of solid state power amplifiers (SSPAs) at 352 MHz for its boost and storage ring amplifiers. Those amplifiers are based on a combination of 330 W modules to deliver up to 190 kW in continuous wave (CW) mode. After the initial successful deployment at SOLEIL, many accelerator facilities have carried out research on SSPAs for their accelerators. Jacob et al. in collaboration with ELTA/SOLEIL developed 150 kW SSPAs as a replacement of klystron transmitter for their booster system operated in CW at the European Synchrotron Radiation Facility (ESRF). The SSPA-based power source, consisting of two 75-kW towers with an overall efficiency of 59%, is composed of individual modules of 650 W with 68% in efficiency. It is reported during 1000 h of test without any degradation. Another replacement of klystrons by SSPAs was made for the booster synchrotron of the Swiss Light Source (SLS), which
The system is composed of 65 kW power amplifiers operated with 53% efficiency by combining 108 of 650 W modules. In addition, it is noted that the efficiency of the system was optimized at higher levels than 50% by changing bias voltages at each of the modules independently. The solid state technology is not only increasingly present in research accelerator laboratories, but it is also growing in the industry (see an exhaustive review in Ref. 12 and references therein). Therefore, it is needed to foresee the development of the next-generation power sources, which will be implemented using the latest solid-state technology and high power low loss combination strategies possible.

Recently, we have proposed an innovative design approach, introducing single-ended modules at the kilowatt level. This design is based on a resonant stepped-impedance matching network, which is a compact design with less complexity, dedicated for mass production. The design approach opens up a new perspective toward kilowatt-level amplifiers with comparable power handling capability, output power, and efficiency, i.e., 71%, as in push-pull configurations. In addition, we have realized a low loss Gysel planar combiner at the 10 kW level, which allows us to reduce significantly the dimension of the combiner as well as the whole design system without any compromise of combining efficiency performance.

When developing solid-state power amplifiers for particle accelerators, one often raised question is related to the stability and flatness of the power source during the pulse duration. This is especially relevant for the next generation particle accelerators, i.e., the European Spallation Source (ESS) proton accelerator, comprising 26 stations of 400 kW for driving superconducting cavities. In this paper, we introduce a 10 kW system that is suitable for scaling up in power and reaching the nominal 400 kW required for the operation of ESS linear accelerator (LINAC), and thus, it must fulfill strict requirements in terms of amplitude and phase. In order to demonstrate the adequacy of the proposed 10 kW amplifier and scaling up, we characterized the presented system in the time domain, under the specifications of ESS. The use of capacitor banks inherently causes power droop within the pulse (see Refs. 16 and 17). During operation, the power droop leads to inherent instabilities in the operation of the LINAC, as the extremely stable accelerating voltage gradient generated in superconducting cavities is disturbed by the power droop. To supply the required energy to the accelerated particles, a feedback control loop is implemented, which allows stabilizing the amplitude and phase disturbances of the RF power supplied in order to establish a constant field gradient in the superconducting cavities (see Fig. 1).

We have therefore implemented in-house several building blocks such as the feedback low level RF (LLRF) control system and a 10 kW power amplifier to demonstrate the adequate operation and potential for scaling up in power, i.e., a 400 kW power amplifier for powering ESS superconducting cavities.

This paper is organized as follows: Section II introduces the architecture of the LLRF control system. In Sec. III, the design architecture of the 10 kW system is presented. The tuning of each amplifier is implemented toward optimizing in amplitude and phase at a 1.25 kW output power level. In Sec. IV, the 10 kW system is fully characterized in the time domain. Section V shows the droop compensation and an improvement of amplitude variations using LLRF. Section VI concludes this paper.

II. AN ARCHITECTURE OF FEEDBACK CONTROL LOOP

It is important to fully evaluate our design approach of the SSPA-based power source under ESS requirements regarding amplitude and phase variations. In this regard, the LLRF is realized on a field-programmable gate array (FPGA) technology at the heart of the control system for the presented 10 kW system, as shown in Fig. 1. A reference signal from the output coupler is used as a feedback signal. The feedback signal is fed to the LLRF system, allowing for compensating the droop of the pulsed RF signal caused by capacitor banks and correcting other disturbances caused by cavities detuning, phase and amplitude variations, etc.

In this paper, we present the test of the 10 kW power station using the feedback loop, as to assess the amplitude variations and the droop. A comparison with and without feedback is realized in Sec. V.

The architecture of the LLRF system is described (see Fig. 2). The digital LLRF system is realized on the PXIe architecture.
(PXIe-1085 from National Instruments) incorporating the FlexRIO FPGA module, two Analog-to-Digital Converters (ADCs) at 250 MSPS, and two high-resolution high speed Digital-to-Analog Converters (DACs) at 500 MSPS. The RF signal from the cavity is routed to the digital down converter (DDC) block to convert into in-phase and quadrature (IQ) components. The down-converted IQ signals are filtered using configurable decimation filters, allowing for reducing the sampling rate from 250 MSPS down to 10 MSPS (see Fig. 2). A phase shift or time delay is added to the IQ components in order for compensating the loop delay. The time delay or phase shift algorithm on the FPGA is based on rotating the I and Q components according to the following equations:

\[ I_\text{r} = I \cos(\delta \phi) - Q \sin(\delta \phi), \]  
\[ Q_\text{r} = I \sin(\delta \phi) + Q \cos(\delta \phi), \]  

where the time delay \( \delta t \) is converted to a phase delay \( \delta \phi = \omega \delta t \), and \( I_\text{r} \) and \( Q_\text{r} \) are the phase-shifted signals. The rotated I- and Q-part of the cavity is then fed to the LLRF (Proportional-Integral) PI-controller, allowing for correcting the amplitude and phase of the cavity. The PI-controller is used to drive the output to the predefined values of the amplitude and the phase toward a set-point. The predicted values are either a single set-point or a table of set-point values. In this block, it consists of two independent PI-controller cores, in which one is for the amplitude and one is for the phase. Note that the feed forward (FF) table is used only in the case of beam loading. The output from PI-controllers is then digitally mixed and then converted back to the RF analog signal to drive the cavity field using a dual 500 MSPS DAC combined to a 1 GSPS DAC. The LLRF controllers are implemented on the FlexRIO NI-5782 FPGA module programmed using Labview.

III. 10 kW SOLID STATE AMPLIFIER

A. The architecture of 10 kW SSPA system

In this section, the 10 kW SSPA system is presented (see Fig. 3). The presented system consists of two-stage driver power amplifiers (PAs), an 8-way quarter-wavelength divider, 8 single-ended kilowatt modules, an 8-way Gysel combiner, DC power supplies, capacitor banks, switches, and Arduino-based monitoring circuits. The first-stage driver PA 1 (ZHL-100W-52 from Minicircuits) amplifies an RF pulse from a R&S SMBV100A signal generator with a gain of 50 dB. The amplified signal is then fed to the second-stage driver PA 2, which is of single-ended architecture as the same as described in Ref. 13. The driver amplifier is operated in class AB at a lower drain voltage of 35 V, driving a peak output power of about 200 W. At the output of the second stage, a circulator (VDB-1078A from Valvo) is added for protection. The output pulsed RF from the driver stage is divided by using a resonant divider before feeding the 8 SSPA modules. Each of the modules is driven about 25 W in order to deliver 1.25 kW peak RF power. An eight-68-mF-capacitor bank allows for supplying the energy during the pulse and the power supply (63 V-90 A) and then provides a recharge current to 8 SSPA modules during the silence of the pulse. A Gysel-based combiner is used for the combination of eight 1.25 kW modules to obtain a total peak output power up to 10 kW as described in Ref. 14. The designs of the
The 10 kW system is designed to fit the 19-inch rack with 4 SSPA modules on the top and 4 SSPA modules at the bottom. The system incorporates Arduino-based circuits to monitor the current, drain voltage, and heat-sink plate temperature of each module during high power operation. The 24-channel analogous data from circuits are digitized by an Atmega-328P microcontroller (Arduino), allowing to compute the drain efficiency in the time domain. The prototype of 10 kW amplifier system is designed to fit a 19-inch standard rack and a height of 9-rack units (40 cm) (see Fig. 4).

**B. Design of 1250 W SSPA module**

The SSPA-based system was built around individual modules, which were based on the push-pull architecture allowing for high power handling capability, harmonics suppression, easier input/output matching, and wide-band performance while providing a simple amplifier design. This is a new approach in kilowatt power amplifier design, presently dominated by the push-pull configuration (see Fig. 5). In the presented system, each of the individual modules has resonant stepped-impedance matching networks in the single-ended architecture at the kilowatt-level (see Ref. 13). The input and output matching networks are stepped-impedance resonators at 352 MHz. The single-ended SSPA module is built around BLF188XR and realized on the RO3003 substrate with dielectric constant $\epsilon_r = 3$, loss tangent $\tan \delta = 0.0012$, substrate thickness of 0.76 mm, conductor thickness of 35 $\mu$m, as in Fig. 5 biased at a low quiescent current of 80 mA and a drain voltage of 50 V in deep class AB operation. The design is demonstrated to have superior performance in terms of efficiency up to 71%, output power of maximum 1.3 kW pulsed at ESS specifications, and very good stability in amplitude and phase, as shown in Ref. 16. The design approach opens up a new route to kilowatt power amplifier design with good performance and stability.
new perspective toward kilowatt-level amplifiers which require compact design, repeatability for mass production, less complexity with comparable power handling capability, output power, and efficiency as in the push-pull configuration.

According to Ref. 15, the loaded Q of the cavity is about 1.75 × 10^5, setting the cavity bandwidth at about 2 kHz. The amplifier bandwidth should be 10 times greater than the cavity bandwidth, which is about 200 kHz, for tuning and regulation delay. Due to the extremely narrow bandwidth of the amplifier, the single-ended architecture has been adopted and its feasibility and performance at the kilowatt-level have been demonstrated. As strictly required in Ref. 15, a time domain measurement setup is used in order to fully characterize the kilowatt single-ended module’s performance such as pulse droop along the pulse, efficiency over the pulse, average envelope pulse amplitude and phase, pulse drain voltage waveform, pulse drain current waveform, pulse to pulse stabilities in amplitude and phase, etc. The presented module features outstanding characteristics of pulse-to-pulse (P2P) stabilities of −80 dB in amplitude and 0.05° in phase as delivering 1.25 kW output power at the 1.5 dB compression point with more than 70% in drain efficiency (see Ref. 16). Thanks to the resonating matching networks, we achieve such a low level of harmonics at 1.25 kW output power: 2nd at −25 dBc, 3rd at −35 dBc, 4th at −44 dBc, and 5th below −60 dBc.
C. Variation measurements in amplitude and phase

As previously mentioned, all of the modules are biased in deep class AB operation at $V_{ds} = 50$ V. All of the modules are fully characterized using the measurement setup, as published in Ref. 16. Due to the tolerance of the Laterally-diffused metal-oxide semiconductor (LDMOS) transistors, manufacturing, and passive components, there are some variations in the values of power gain and phase shift among individual kilowatt modules. As analyzed in Refs. 19 and 20, the variability in the gain and phase shift results in imperfect summation of power, hence a reduction in combining efficiency. Such variations should be kept within some limits so that the combination loss does not increase above a minimum acceptable value. In the presented 10 kW system, the tolerances are quantified within 0.5 dB for the gain and within $5^\circ$ for the phase shift among individual single-ended amplifiers to ensure the best performance of combining efficiency above 90%. Modules are fine-tuned by moving the position of the matched capacitors toward the transistor. The input reflection of the modules are also tuned to critically match 50 $\Omega$ and optimized below $-15$ dB for reducing power combining loss.

The gain characteristic of 8 modules is presented in Fig. 6. There is deviation among gain curves at a low output power range. The tolerance for the gain curves is kept in the order of 0.5 dB at the high output power ranging from 900 W to 1250 W. As described previously in Ref. 13, the position of the matched capacitors close to the drain of the transistor results in significant changes of gain, drain current, and phase as well as efficiency due to the use of stepped impedance resonators. Variation of the efficiency and phase shift among the modules are presented (see Figs. 7 and 8). The phase imbalance is on the order of $8^\circ$ in the range of 1000W–1100 W, while it is tuned perfectly within $5^\circ$ in the range of 1100 W–1250 W. Such imbalance can be compensated by using the variable length coaxial cables and the variability in phase among ports of the combiner. The imbalances in amplitude among the kilowatt modules are presented in the time domain, as shown in Fig. 9.

D. Design of quarter-wavelength divider

In this section, the 8-way divider is based on the quarter-wave transmission-line impedance transformer. The transformer is a coaxial transmission line which is formed by a circular inner conductor and a square outer trough. The characteristic impedance of the transmission lines can be deduced by the following formula:

$$Z_0 = 138 \log_{10} \left(1.079 \frac{d}{D}\right) \Omega,$$

(3)

where D is the diameter of the outer conductor and d is the diameter of the inner circular conductor. In this design, four outputs are mounted on one end of the trough, while four other outputs are mounted on the other end of the trough (see Fig. 11). The input port of the splitter is mounted at the center of the trough. The distance between the input port and the output ports is equivalent to a quarter-wavelength of 352 MHz. The impedance seen at the common point of 4 output ports is 12.5 $\Omega$, and the impedance seen at the input is 100 $\Omega$. The characteristic impedance of quarter-wave transformers is then chosen on the order of 37.5 $\Omega$, allowing for best matching. In the design of divider, $D = 26$ mm for aluminum square tubes and $d = 15$ mm for brass circular tubes, as shown in Fig. 11. The topology is then simulated using Keysight ADS software (see Fig. 12). At 352 MHz, the insertion loss is measured as low as 0.05 dB. The input return loss is measured on the order of about 25 dB. The mutual coupling among output ports is measured about 8.33 dB. The low mutual coupling of the
divider can be solved by adding circulators at each of the output ports.

### E. Design of 8:1 Gysel-based power combiner

In this section, a compact 8-way combiner is developed on the TMM3 substrate.14 The presented combiner is based on the Gysel architecture22 addressing technical challenge as being realized on planar technology in a mechanically compact unit, i.e., heat dissipation at high power during mismatch. The combiner allows for power summation of SSPA modules to produce a final output signal on the order of 10 kW. The 8-way combiner is provided, composed of a two dimensional layered assembly including the output layer and the common layer. The layered assembly allows degrees of freedom in selecting the interlayer transmission line impedances for best optimization of the combiner, i.e., board-to-board coupling, amplitude balance, and phase balance. Two layers are stacked over each other with the interconnecting points at the 8 input ports. The stack arrangement results in a high power compact assembly suitable for the 352 MHz operating frequency of interest where the long wavelength leads to a bulky structure. The dummy loads are electrically connected to associated transmission line termination at respective input ports. The dummy loads are carried by the common layer and mounted to the aluminum casing. Each of the layer boards carries cut-out slots enabling high power operation with the inherent ventilation capability of the layered approach. The mutual coupling among transmission lines in the common layer is compensated by adding weakly coupled stubs located on the order of $\lambda/8$ from the floating common point. Further insightful design can be found in Ref. 14. Low power measurement results are provided in Table I. The insertion loss is as low as $-0.2$ dB. The maximum amplitude among ports is measured in the order of 0.15 dB. The imbalance in phase of the presented combiner is kept within 4°, thanks to adding the coupling stubs. The phase variations can be compensated by choosing the suitable SSPA modules with phase deviation as inputs of the combiner, hence minimizing the power combining loss of the whole system without adding the variable coaxial cables between the power amplifier stage and the combiner. According to analysis in Ref. 23, the combining efficiency is computed on the order of 98%.

### IV. TESTING OF THE 10 kW SYSTEM

The 10 kW system is characterized using a test setup described in Fig. 13. A measurement setup is used to characterize the presented system as in Fig. 3. The overall loss in cables and the divider/combiner stage of the 10 kW system is on the order of 0.72 dB in which 0.4 dB is the input loss and 0.32 dB is the output loss. High power tests are performed (see Fig. 14). The measured input power/output power characteristic is plotted in the blue curve, while the red curve shows the theoretical input power/output power characteristic of the system. The theoretical curve is defined as the summation of 8 SSPA modules. The system is driven with 154 W of input power to produce a final output of 10 kW. Each of the modules is calculated to deliver in the order of 1355 W. As shown in Fig. 15, the 1.5 dB compression point of the system is measured approximately 10.5 kW (70.21 dBm). As mentioned in Sec. III C, the perfect

---

**FIG. 14**. The presented system is driven about 180 W of input power to obtain 10 kW of output power. The figure shows the input power/output power characteristic of the 10 kW system with the measured results (blue curve) and theoretical results (red curve).

**FIG. 15**. The 1.5 dB compression point of the presented system is on the order of 10.5 kW output power. The red curve shows the theoretical power gain of SSPAs, while the blue curve shows the measured power gain of SSPAs.

**FIG. 16**. The combination loss is reduced, thanks to the higher homogeneity in amplitude and phase among the eight SSPA modules at high power levels.
imbalance in the amplitude and the phase among modules in the range of 1100 W–1250 W lead to a significant reduction in combining loss (see Fig. 16). The combination loss is computed in the order of 0.105 dB at the output power of 10 kW, equivalent to 267 W. Time domain measurements are implemented using the monitoring circuits and a high-speed oscilloscope RTO-1024 [see Figs. 17(a) and 17(b)]. The voltage drop is about 1 V during the pulse. The power supply then recharges the capacitor during the off period of the pulse [see Fig. 17(a)]. The drain current waveforms among the SSPA modules are shown in Fig. 17(b). The droop over the pulse is measured in the order of 1.5 A. The spread in the current waveforms is observed with a maximum current of 40 A drawn by module 2 and a minimum current of 35 A drawn by module 8. The DC power consumption of the 10 kW system is presented in the time domain. As shown in Fig. 18, the DC power droop during the pulse measured in the order of 1 kW, which is equivalent to 7% of the average DC power. The droop over the RF pulse is measured about 0.354 dB or approximately 834 W. The average efficiency of the 10 kW system is computed on the order of 72% as shown in Fig. 19. The 10 kW system is tested at 10 kW output power during 4 h of operation. The RF system performance and temperature characteristic of the combiner are measured over time. There is an increase in the combiner’s temperature due to heat dissipation of the external dummy loads on the common layer as described in Sec. III E. The temperature of the combiner stays constant at 35 °C with the ambient temperature of 25 °C (see Fig. 20). There are no performance degradation, heating, or arcing of the system during the measurements. The cooldown rate is also measured with RF off, as shown in Fig. 20. This implies that no active cooling is needed, thanks to the extremely low insertion loss of the combiner.

V. COMPENSATING 10 kW SSPA SYSTEM WITH THE PXIE-BASED LOW LEVEL RADIO FREQUENCY (LLRF) SYSTEM

In this section, the presented 10 kW system is tested using the LLRF for compensating the droop within the pulse due to the use of capacitor banks. The block diagram of the experimental setup is presented (see Fig. 2). A reference signal from the output coupler (see Fig. 2) is used as a feedback signal. The feedback signal is fed to the LLRF system, allowing for compensating the flattop of the RF pulsed signal. A 0 dBm limiter is added to protect the inputs of the ADC parts. The calibration is first implemented using the LLRF system in which the PI-controller loops are bypassed. The output of the LLRF system is used to drive the 10 kW system and compare when using signal generator SMBV-100A, as described in Sec. III A. The droop within the pulse is in the order of 0.356 dB (see Fig. 21). The measured droop in is an agreement with the result achieved in
Sec. III C. The open-loop test allows for evaluating the linearity of the 10 kW system, thus preventing the system from instability as running with feedback loops. The PI-controller loops are activated, allowing for compensating the droop within the pulse (see Fig. 21). The amplitude variation is measured approximately 20 W during the pulse, which is equivalent to 0.2%. The overshoot in the beginning of the pulse can be significantly reduced by adjusting proportional and integral terms of the PI-controller core for phase. The overall processing time of the system is in the order of 6 μs. The system is operated without any instability during 4 h of operation.

VI. CONCLUSION

A modular and scalable 10 kW solid-state based RF system is successfully developed and characterized extensively in the time domain under ESS specifications (3.5 ms pulse width and 14 Hz repetition rate). In the presented 10 kW system, the single-ended design approach toward compactness, high stability, high efficiency, and easy repeatability is validated at the kilowatt level, each of the power amplifier modules delivering up to about 1.3 kW output power. The combination of 8 modules is demonstrated. For reducing the combining loss, all of the modules are tuned optimally within an acceptable variation of 0.5 dB in gain and 5° in phase. The Gysel-quarter-wavelength based combiner is realized on planar technology with a layer-by-layer approach, allowing for higher compactness as compared to other quarter-wavelength designs. The layer-by-layer design approach of the combiner makes it realizable to integrate in the presented 10 kW system on 4U rack units. The combining efficiency of the combiner is measured to be on the order of 98%. The inherent phase variations among modules can be reduced significantly by choosing the appropriate input ports of the combiner, thus improving the overall combining efficiency without adding any variable coaxial cables between the power amplifier stage and the combiner stage. The presented system is measured at 72% within the pulse in drain efficiency at 10 kW of output power. The overall efficiency is reduced 1% due to the use of the combiner. To the best of our knowledge, the presented system is by far the best in terms of compactness, efficiency at 10 kW of output power. Furthermore, the droop caused by capacitor banks is characterized 0.356 dB within the pulse in the time domain. For the first time, the droop-and-overshoot compensation is implemented at 10 kW of output power using an in-house LLRF system, thus improving the overall stability of the system suitable for ESS particle accelerator requirements within 0.1% in amplitude and 0.5° in phase. In conclusion, the proposed system meets the strict requirements by ESS and is an excellent candidate for the scale in power up to a 400 kW solid-state based power station to be deployed for the ESS particle accelerator.

ACKNOWLEDGMENTS

The authors would like to thank FREIA and ESS for financial support of this work. We gratefully acknowledge the support from the Eurostars programme for the project ENERF, E11654.

REFERENCES

1. C. Beard, Nucl. Instrum. Methods Phys. Res., Sect. A 557, 276–279 (2006).
2. M. D. Giacomo, in Particle Accelerator Conference (PAC09), May 2009, Vancouver, Canada (JACoW, Geneva, Switzerland, 2009), p. 757.
3. P. Marchand, T. Ruan, F. Ribeiro, and R. Lopes, Phys. Rev. Spec. Top.—Accel. Beams 10, 112001 (2007).
4. G. Gautier, J. Jacob, M. L. Langlois, and J. M. Mercier, in Proceedings of the 2nd International Particle Accelerator Conference, IPAC 2011, San Sebastian, Spain, September 4–9, edited by C. Petit-Jean-Genaz (EPS-AG, Geneva, Switzerland, 2011), Vol. CI10904, pp. 71–73.

5. L. F. M. Gaspar, M. Pedrozzi, and T. Garvey, Nucl. Instum. Methods Phys. Res., Sect. A 637, 18–24 (2011).

6. M. Gaspar and T. Garvey, IEEE Trans. Nucl. Sci. 63, 699–706 (2016).

7. A. Jain, D. K. Sharma, A. K. Gupta, and P. R. Hannurkar, Rev. Sci. Instrum. 79, 014702 (2008).

8. A. Jain, P. R. Hannurkar, D. K. Sharma, A. K. Gupta, A. K. Tiwari, M. Lad, R. Kumar, P. D. Gupta, and S. K. Pathak, Int. J. Microwave Wireless Technol. 4, 595–603 (2012).

9. A. Jain, P. Hannurkar, D. Sharma, A. Gupta, A. Tiwari, M. Lad, R. Kumar, M. Badapanda, and P. Gupta, Nucl. Instum. Methods Phys. Res., Sect. A 676, 74–83 (2012).

10. A. Jain, D. K. Sharma, A. K. Gupta, M. R. Lad, P. R. Hannurkar, and S. K. Pathak, Rev. Sci. Instrum. 85, 024707 (2014).

11. J. K. Mishra, B. Ramarao, M. M. Pande, and P. Singh, Nucl. Instum. Methods Phys. Res., Sect. A 764, 247–256 (2014).

12. P. Marchand, in Proceedings of the 8th International Particle Accelerator Conference (IPAC 2017), Copenhagen, Denmark, May 14–19 (JACoW, Geneva, Switzerland, 2017), p. WEPME012.

13. L. Haapala, A. Eriksson, L. H. Duc, and D. Dancila, Electron. Lett. 52(18), 1552–1554 (2016).

14. M. Jobs, D. Dancila, J. Eriksson, and R. Ruber, IEEE Trans. Compon., Packag., Manuf. Technol. 8, 851–857 (2018).

15. S. Pegg, Technical Report No. ESS-2013-001, European Spallation Source, European Spallation Source, April 2007.

16. L. H. Duc, A. Bhattacharyya, V. Goryashko, R. Ruber, A. Rydberg, J. Olsson, and D. Dancila, Microwave Opt. Technol. Lett. 60, 163–171 (2018).

17. P. Mohania, A. Mahawar, P. Shrivastava, and P. D. Gupta, Rev. Sci. Instrum. 84, 094703 (2013).

18. L. H. Duc, M. Holmberg, A. Hjort, A. Rydberg, and D. Dancila, in Swedish Microwave Days, Linköping, 2016.

19. M. S. Gupta, IEEE Trans. Microwave Theory Tech. 40, 1031–1034 (1992).

20. R. A. York, IEEE Trans. Microwave Theory Tech. 49, 1477–1482 (2001).

21. Y. A. Omar and C. F. Miller, IEEE Trans. Commun. 71, 81–89 (1992).

22. U. H. Gysel, in IEEE-MTT-S International Microwave Symposium (IEEE, 1975), pp. 116–118.

23. R. L. Ernst, R. L. Camisa, and A. Presser, in IEEE MTT-S International Microwave Symposium Digest (IEEE, 1977), pp. 174–177.

24. D. Dancila, A. Rydberg, A. Eriksson, V. Goryashko, L. Haapala, R. Ruber, R. Wedberg, R. Yogi, and V. Ziemann, in Proceedings of the 5th International Particle Accelerator Conference (IPAC 2014), Dresden, Germany, June 15–20, 2014 (CERN, Geneva, Switzerland, 2014), p. WEPME012.