An Optimized Parallel Failure-less Aho-Corasick Algorithm for DNA Sequence Matching

D.R.V.L.B Thambawita  
Department of Computer Science and Technology  
Uva Wellassa University  
Badulla, Sri Lanka  
Email: vlbthambawita@gmail.com

Roshan G. Ragel and Dhammike Elkaduwe  
Department of Computer Engineering  
University of Peradeniya  
Peradeniya, Sri Lanka  
Email: [ragelrg, dhammika.elkaduwe]@gmail.com

Abstract—The Aho-Corasick algorithm is a multiple patterns searching algorithm running sequentially in various applications like network intrusion detection and bioinformatics for finding several input strings within a given large input string. The parallel version of the Aho-Corasick algorithm is called as Parallel Failure-less Aho-Corasick algorithm because it doesn't need failure links like in the original Aho-Corasick algorithm. In this research, we implemented an application specific parallel failure links like in the original Aho-Corasick algorithm. The parallel version of the Aho-Corasick algorithm is called as Parallel Failure-less Aho-Corasick algorithm on the general purpose graphic processing unit by applying several cache optimization techniques for matching DNA sequences. Our parallel Aho-Corasick algorithm shows better performance than the available parallel Aho-Corasick algorithm library due to its simplicity and optimized cache memory usage of graphic processing units for matching DNA sequences.

key words- Aho-Corasick, GPGPU, DNA sequence matching

I. INTRODUCTION

The Aho-Corasick algorithm is used for finding multiple patterns (strings) within a given large input string. This was invented by Alfred V. Aho and Margaret J. Corasick [1]. Therefore, this algorithm is used widely in many applications like plagiarism detection, intrusion detection, digital forensic, text mining and bioinformatics. The Aho-Corasick algorithm is executed one time for finding all occurrences of known patterns within the given input string. However, the main drawback of the original Aho-Corasick algorithm, which is based on sequential processing logic is the performance. The solution for the issue about the performance was introduced by Lin et al. [2] [3] by introducing a parallel version of the Aho-Corasick algorithm called Parallel Failure-less Aho-Corasick (PFAC) algorithm which runs on GPGPUs.

The original PFAC was introduced as the general purpose library for any kind of applications, which are based on finding multiple patterns within the given large input. However, our implementation is designed especially for DNA sequence matching and compared with the usage of the original PFAC for DNA sequence matching. Within our PFAC implementation, we concentrated on cache optimizations of GPGPU and application specific modifications for achieving better performance than original PFAC for DNA sequence matching.

II. RELATED WORK

The Aho-Corasick algorithm was invented by Aho, Alfred V. and Corasick, Margaret J. on 1975 as an article “Efficient String Matching: An Aid to Bibliographic Search” [1]. They have introduced a new mechanism for searching multiple patterns within a given large input text. It shows good performance for multiple pattern searching among other traditional multiple pattern matching algorithm.

Dimopoulos et al. [4] have discussed a modification to the serial Aho-Corasick algorithm for gaining memory efficiency to detect intrusions. They implemented a split Aho-Corasick algorithm with domain specific characteristics of intrusion detection for minimizing the memory usage of the finite state machine of the algorithm. As the domain specific characters, they observed that most patterns are subset of 256 characters, out of these 256 characters some are used almost in every states while other characters are used infrequently, and split finite state machines have smaller memory sizes according to the domain than the large finite state machine. The modified algorithm has been run on a Field-Programmable Gate Array (FPGA) chip as an improved version of the Aho-Corasick algorithm with the point of view of the memory usage.

The speed-up of Aho-Corasick pattern matching machines by rearranging states has been done by Nishimura et al. [5]. They have rearranged the states of the finite state machines for improving the memory access via cache memory. After constructing the basic goto graph, all the states of the graph have been rearranged according to the breadth-first order. Then all the memory accesses were more cache friendly and the performance gain is 55%.

The PFAC was introduced by Lin et al. [2]. PFAC has been run on a graphic processing units without failure links. They have run failure links less Aho-Corasick algorithm using thousand of threads of the GPGPU. Then it shows big performance improvement over the original serial Aho-Corasick algorithm. They published the second paper [4] of improving the PFAC by introducing a hash function method.

Kouzinopoulos et al. have done a survey about the performance of some selected string matching algorithm on GPGPU [6]. They have selected the Naive, Knuth-Morris-Pratt, Boyer-Moore and Quick-search on-line exact string matching algorithms as the test cases. However, the graphic card used for testing these algorithm was basic general graphic card called NVIDIA GTX 280. Therefore, they failed to show actual performance gain of these algorithm on the high end GPGPU.
like tesla series.

III. AHO-CORASICK ALGORITHM

As we mentioned, Alfred V. Aho and Margaret J. Corasick [1] introduced the Aho-Corasick algorithm. They have discussed basic two steps for using this algorithm like (1). constructing a finite state pattern matching machine from the keywords and (2.) matching the input using the constructed finite state machine.

Let us look at an example; assume that patterns AC, ACG, CTGT and TG should be searched within the given text. As the first step, the finite state machine should be constructed using the given patterns. For constructing a finite state machine, they have used three functions called goto (g), failure (f) and output. First, goto graph should be constructed for finding the goto function. This goto graph of the above example input patterns is given in Fig. 1.

The pattern AC will be matched in state 2, ACG in state 3, CTGT in state 7 and TG in state 9 as shown in Fig. 1. This graph represents the goto function. Next step is constructing failure function from the goto function. This failure function should be calculated for all the states of the goto graph as mentioned in the original Aho-Corasick article [1]. The complete finite state machine with failure links of the above example is given in Fig. 2. Some nodes are marked with red color to identify output nodes.

The complete finite state machine is now available as in Fig. 2. It is easy to understand the processing phase of the Aho-Corasick algorithm by an example. Let’s consider an input text with a text string $S = s_1,s_2,s_3,...,s_n$. The processing phase starts with the first state from the transition graph and the first character from the input text. First, it checks that the current input character of the input text has a transition from the current state of the finite state machine. Simply, it executes the goto function. If the goto function returns a new state, the current state of the input transition table is a new state while the current input character is the next character of the input. Assume that the goto function failed, then the processing phase will check the failure function (f) for finding the next state for the current input character. If the finite state machine reached to the output nodes, it will return matched patterns of the current state of the finite state machine. All of the above steps will be continued until the process reaches to the final character of the input text.

IV. WHAT IS THE PFAC ALGORITHM?

Within this section, we are discussing Parallel Failure-less Aho-Corasick Algorithm (PFAC) implemented by Lin C.H. et al. [2] [3]. It works as same as the Aho-Corasick algorithm. However, PFAC runs on GPGPUs without failure links. PFAC doesn’t use these failure links to backtrack the next starting point and sub patterns. It uses a parallel execution technique using parallel threads of GPGPUs. Then, it doesn’t need any failure link for identifying the next start point because each character of the input has its own thread for running a finite state machine. However, normally PFAC can detect only the longest patterns and it does not detect sub-patterns of the large patterns.

This failure-less machine runs parallel on a GPGPU. When the machine is run parallel on the GPGPU, each and every letter of the input text pass into the transition machine by it’s own thread. As the result, every letter is searched in parallel individually. This mechanism can be identified by Fig. 3.

PFAC algorithm has been used as the reference point of our research. We have developed our own application specific PFAC source code for matching DNA sequences because original PFAC was developed for general purposes. The development process of our application specific PFAC will be discussed in the next section.
### V. Designing and Implementation of the Application Specific PFAC for DNA Sequence Matching

Within this section, we are discussing how the new application specific PFAC algorithm was developed and features of that algorithm. Our own application specific PFAC algorithm was developed with some differences from the original PFAC algorithm. However, our implementation has been limited into an application specific algorithm like bioinformatics DNA matching as a factor for gaining better performance than the general purpose original PFAC algorithm.

#### A. Designing application specific PFAC algorithm for DNA sequence matching

To develop an application specific PFAC algorithm, the following main steps were followed:

- Developing a data structure for the input patterns’ finite state machine.
- Read data from input text and run with the finite state machine.
- Managing memory types of the system for gaining better performance.

When the input pattern’s finite state machine data structure was created, only four characters were considered because the bioinformatics algorithms of DNA matching are using mainly a specific number of letters like A, T, C and G. Therefore, $4 \times N$ 2D array was created to store all the input patterns where $N$ is the maximum number of states that can be handled by the program. A sample data structure (transition table) for storing sample input patterns can be seen at Table 1.

|   | A   | T   | C   | G   |
|---|-----|-----|-----|-----|
| 0 | 1.0 | 0.0 | 0.0 | 0.0 |
| 1 | 2.0 | 0.0 | 0.0 | 0.0 |
| 2 | 3.0 | 0.0 | 0.0 | 0.0 |
| 3 | 0.0 | 4.0 | 0.0 | 0.0 |
| 4 | 0.0 | 11.0| 5.0 | 0.0 |
| 5 | 0.0 | 0.0 | 0.0 | 6.1 |
| 6 | 7.0 | 0.0 | 0.0 | 0.0 |
| 7 | 0.0 | 0.0 | 8.0 | 0.0 |
| 8 | 0.0 | 0.0 | 0.0 | 9.0 |
| 9 | 0.0 | 0.0 | 10.0| 0.0 |
| 10| 0.0 | 0.0 | 11.2| 0.0 |
| 11| 0.0 | 0.0 | 0.0 | 12.3|
| 12| 0.0 | 0.0 | 0.0 | 0.0 |

#### B. Implementation of our application specific PFAC on GPGPU

The main method of our application specific PFAC for loading input patterns into the transitions table can be seen in Fig. 4. It has three input arguments for parsing pattern file name, pointing next state of the int array and pointing the matched pattern ID array.

```c
int readPatternsFromFileToTransitionTable(
    char *patternFile,
    unsigned int *nextState,
    unsigned int *matchedPatternId)
{
    ...
}
```

Fig. 4. Method for loading patterns into the transition table

```c
char * readTextFromFile(
    char *inputFile,
    int* inputText_size_p){
    ...
}
```

Fig. 5. Reading input text file into a buffer

According to the above method, the method readTextFromFile takes two arguments for input text file name and an integer pointer to store input file size. Finally, a char pointer which has all the characters of the input text file is passed as the return value.

Now, all the required data to run PFAC algorithm are ready within the memory of the host machine. Therefore, those data have to be passed into the device memory before launching a kernel in the device. The cudaMemcpy() function has been used for copying data from the host to device as well as the device to the host in the final stage.
Then, the kernel can be launched by passing the relevant parameters. Only one kernel is launched in our PFAC. It creates 256 threads per block. The number of blocks is defined according to the input text file size. If one dimension grid is considered, then the number of blocks per dimension may exceed the maximum number of blocks per dimension limit of the device for large input size. Therefore, a two dimension grid was created when the input has more characters. Deciding about dimensions of the grid is an automated process. As a requirement, the number of threads that is equal to the number of characters within the input text are created within the GPGPU for running our application specific PFAC algorithm. Finally within the kernel, character by character search is done using an individual thread using the transition table of the input patterns.

The kernel function takes mainly five parameters. The nextState and matchedPatternId are memory locations that were allocated previously to store the information about the transition table. Then, it takes main input called inputText which has to be searched. The output is the integer array which has been used to store output data after finding a match. Our implementation of PFAC uses the 1D array instead of 2D arrays. Therefore, the pitch is taken as an input parameter to determine the rows of arrays. It means the pitch size is equal to the row size of the transition table. In our case, this value is equal to the four (4).

C. Managing memory types to gain better performance

The GPGPU is a device with several memory types. Global, shared, L1 cache, L2 cache, texture and constant memories are names to identify those various memory types. However, the usage of these memory types is different while some of the memory types are out of control from the user. Therefore, it is very important to handle these memory types according to the requirement.

Initially, all the data structures (input text data, transition table arrays) are transferred into the main global memory. Then those data structures are step by step migrated to special memory locations for testing the performance of each memory types. The first test was run using only global memory. Then two arrays of transition table called nextState and matchedPatternId are transferred into the texture memory location. Within another test, the input text also transferred into the shared memory. As the first step of testing, all the test cases run for different input patterns with large input text. As the second step, input data has been changed for measuring the performance for various input text.

VI. EXPERIMENTAL SETUP

Our main workstation has Intel(R) Core(TM) i7-6700K 4.00GHz CPU with 32GB RAM. The main GPGPU was 6GB NVIDIA Tesla C2075. Table II is used to tabulate cache information about our GPGPU because cache optimizations are discussed under this research.

| Cache size | Cache line size | Description |
|------------|----------------|-------------|
| L1 cache   | 48KB/16KB      | 128bytes    |
|            |                | can be disable by using -Xptxas-dlcmemcg compile flag |
| Shared memory | 16KB/48KB       | 128bytes    |
|            |                | can be used manually |
| L2 cache   | 768KB          | 128bytes/32bytes |
|            |                | Unified cache |

Our PFAC implementation and original PFAC implementation were tested for various patterns and inputs. Information about these test cases is tabulated in Table III and IV.

VII. RESULTS AND DISCUSSION

First, it is required to identify performance difference between memory types of the GPGPU for our application specific PFAC. Then, the cache configurations of the Fermi GPGPU was changed to identify the effects for the performance. Finally, our PFAC implementation and the original PFAC were tested for identifying the performance gap.

The first experiment of our application specific PFAC algorithm was done with only global memory. Then, shared memory and texture memory have been added into the algorithm gradually. The configurations of the GPGPU was unchanged. The test result of these tests is depicted in Fig. 6.

According to the result set in Fig. 6 it is clear that global memory to the GPGPU is the slowest memory as they mentioned in their official document. However, if the data structures are cache friendly then it is possible to gain considerable performance benefits. Within this test, array merge technique has been used to increase the spatial locality of the cache accesses. Then, shared memory is applied into the accesses of input text pattern array. It improves the temporal locality of the cache accesses. Then, slight performance improvement could be gained from the global memory input text array compared
the shared memory input text array. This performance gain is common for both cases which have two arrays for the transition table or one merge array for the transition table. As the next step, texture memory has been applied to the memory accesses of the transition table. Then, transition table memory accesses were via the texture memory of the GPGPU. This increases the spatial locality and temporal locality of the memory accesses of the transition table because texture memory loads all the adjacent memory locations to the texture cache. The texture cache has a 2D spatial locality. Using this texture memory, it could be achieved better performance gain than the previous shared memory technique. However, the final test uses both shared memory and texture memory. At last, merged arrays with shared memory and texture memory shows the best performance among all other techniques. Then, same tests like the above cases were done for the PFAC with shared memory because it shows the best performance among the tested methods. This modified PFAC accesses the input text via shared memory. In the previous basic PFAC, the input text is accessed via global memory only. The results of the PFAC with shared memory option are graphed in Fig. 7.

The shared memory of the GPGPU has been used in this experiment as the technique of optimizing memory access. As the results in Fig. 4, the PFAC with two array transition table shows better performance when it has the large L1 cache (48KB) than other options. The reason behind this story is reducing the cache replacements over the time. However, disabled L1 cache shows better performance if the input pattern set size is very large. This effect is occurring when the pattern size is large because L1 cache has to be replaced cache lines frequently time by time more compared with small input patterns. The number of cache lines within the L1 and the L2 cache is the main reason for this performance gain. The PFAC with one array transition table and shared memory shows a pattern which is similar to the pattern of the previous experiment of the basic PFAC. Therefore, the reason behind this is the same as the above of giving different execution time for different cache options of basic PFAC with only global memory. The texture memory has been used in next experiment for analysing the effect of cache memory options of the GPGPU within the PFAC algorithm. The modified PFAC uses the shared memory for the input text while the texture memory is used for the transition table of storing the input pattern set. The result set is shown in the Fig. 8. According to Fig. 8, It is clear that there are no any clear differences between the 16KB L1 cache and 48KB L1 cache while the texture memory is used. The reason behind this effect is, the texture cache is completely different hardware cache located in each streaming multiprocessor of the GPGPU. The texture cache is designed especially for managing the 2D spatial locality. Therefore, it is well suited for the transition table of the modified PFAC algorithm. However, disabled L1 cache shows poor performance in the two array transition table and the one array transition table compared with enabled L1 cache because it is disabled the L1 cache completely. As the result, only shared memory is available for the usage within L1 cache location. The process cannot use the L1 cache for its own caching purpose. This introduces some performance losses.
Fig. 9. Performance comparison between the original PFAC vs our PFAC implementation.

A test has been done for checking the performance gap between the original PFAC and our PFAC implementation. The worst case and best case of our PFAC implementation were selected for comparing with available PFAC implementation. The results of this test are graphed in Fig. 9.

According to the result sets in Fig. 9, it is clear that our PFAC implementation has better performance than the available PFAC. The worst case of our PFAC implementation also is showing better performance than the available PFAC for large pattern sets. Reasons for this performance gap is different data structures which are more cache friendly and easy to handle compared with the data structures of the original PFAC because our PFAC implementation is application specific like DNA pattern matching. If we compare the available PFAC and the best case of our PFAC implementations then a large gap between performances can be seen. For the largest data set, it is around 3X. The main reason behind this story is cache-friendly memory arrangements for running application specific PFAC compared with the original PFAC.

In all the previous tests, the variable factor was input patterns. As the next step, the input size of input has been changed for various sizes. However, data sets were changed only for identifying the effects of changing input data sets rather than changing the input pattern sets. Within this tests, all the cache parameters have not been changed one by one because the effect of cache options of the GPGPU has been tested in the above tests which were done for various input patterns. Therefore, only the worst case, best case and original available PFAC have been selected as the test cases for changing input data. Then comparison between the available PFAC and our PFAC implementation was done with various input data files as mentioned in Table V. The results of the experiment are graphed in Fig. 10.

Above tests were done for clarifying that our PFAC implementation has better performance while the input data are changed. According to the result sets in Fig. 10, our implementation has better performance for all the test input data in the worst case and the best case. The best case of our PFAC implementation has better performance for all the cases while it is 3X faster than the original PFAC for the largest data set which was used in our experiments.

VIII. CONCLUSION

Our PFAC implementation with basic memory arrangement also shows better performance than the original PFAC. The original PFAC is better than our basic PFAC implementation when the input pattern size is small. The main reason behind this is, the original PFAC uses the texture memory of the GPGPU if the input pattern size is very small. They handle the texture memory automatically without enabling it all the time because they could not show better performance for large data with texture memory.

However, our PFAC implementation with all the possible cache optimization techniques shows the better performance than the original PFAC in all the time. Our best PFAC implementation uses the texture memory for handling the input data while shared memory for handling the input pattern. It is showing best performance among all the PFAC implementation because it has cache friendly data structures and access patterns.

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