Synapses play a critical role in memory, learning, and cognition. Their main functions include converting presynaptic voltage spikes to postsynaptic currents, as well as scaling the input signal. Several brain-inspired architectures have been proposed to emulate the behavior of biological synapses. While these are useful to explore the properties of nervous systems, the challenge of making biocompatible and flexible circuits with biologically plausible time constants and tunable gain remains. Here, a physically flexible organic log-domain integrator synaptic circuit is shown to address this challenge. In particular, the circuit is fabricated using organic-based materials that are electrically active, offer flexibility and biocompatibility, as well as time constants (critical in learning neural codes and encoding spatiotemporal patterns) that are biologically plausible. Using a 10 nF synaptic capacitor, the time constant reached 126 and 221 ms before and during bending, respectively. The flexible synaptic circuit is characterized before and during bending, followed with studies on the effects of weighting voltage, synaptic capacitance, and disparity in presynaptic signals on the time constant.

1. Introduction

Since the early 1990s disadvantages of conventional von Neumann computing architectures, including time-multiplexed serial processing, explicit programming, and high power consumption, have driven the development of biologically inspired electronic circuits to emulate sensory processing systems and spiking neural networks, known as neuromorphic engineering.[1–3] Neuromorphic architectures are characterized by distributed, event-driven processing mechanisms that are massively parallel, resilient against failure or damage, and which consume comparably low energy (1–10 fJ per synapse).[4–6] Neuromorphic computing mainly relies on collections of processing units, called neurons, consisting of synapses and somas. Their main function is to integrate the synapse-weighted input signals and to produce an all-or-none event (a somatic spike) as soon as this integral exceeds a spiking threshold, which is then propagated to other neurons.[7–10]

The synaptic circuits in these architectures play a vital role in the learning and memory formation mechanism.[11] Their main function is to convert the presynaptic voltage spike to a postsynaptic current, and to weight, or scale, the input signal. Furthermore, these synaptic circuits are considered crucial elements for future intelligent brain–machine interfaces (BMI) to bridge the gap between biological and artificial neural systems.[12,13] Silicon-based technologies are currently the dominant realization methods to implement brain-like computing systems.[14–16] The silicon technology offers ultra-fast operational speeds (≥ GHz) and high-density devices, with mature fabrication processes that are precise and well understood.[17] However, silicon-based implementations are expensive and complex, and crucially suffer from lack of biocompatibility, flexibility, and large area coverage. Organic electronics and materials are an alternative to conventional electronics that can be integrated with low-temperature processes with relatively low-priced equipment over a large area. Further advantages include ambipolar semiconducting behavior, physical flexibility, stretchability, and biocompatibility.[18–20]

Early proposals to emulate synaptic functions relied on multi-element electric circuits.[21] Since the announcement of a fabrication of a “memristor,”[22] there has been a great interest to employ these two-terminal inorganic or organic devices to emulate the function and the efficiency of biological synapses in a compact and simple form.[23–25] However, they present a limited number of tunable parameters, typically ON/OFF resistance or discharge rates.[26] Multi-element synaptic circuits provide more flexibility at the cost of lower density.[27] Despite the complexity of these circuits, compared to a single memristive device, multi-element synapse circuits offer control over individual parameters, provide continuously tunable weight, and enable the emulation of biophysically realistic synaptic temporal dynamics.[28–31]

One of the main characteristics of an ideal neuromorphic mechanism is having a biologically plausible time constant (in excess of tens of milliseconds) to process real-world sensory signals efficiently and interact with the environment in real time.[32–34] Log-domain subthreshold circuits with large capacitors faithfully provide biologically plausible temporal dynamics.[35–37] Several log-domain synaptic circuits have been proposed.[38] In particular, the log-domain integrator (LDI)
synapse introduced by Merolla and Boahen in 2004 is a linear filter that lets the synapse integrate the contribution of action potentials from multiple sources linearly. The main drawback of the silicon-based circuit is that long time constants require significant silicon area, for the capacitor, which in turn reduces the number of synapses that can be integrated on a single die. Organic materials are characterized by intrinsically slower charge carrier mechanisms compared with inorganic materials; therefore, the switching speeds of organic devices is limited below MHz or even kHz. Integrating organic materials and LDI synapse architecture seems to offer an ideal synaptic circuit with a plausible time constant and a linear behavior.

In here, we demonstrate a physically flexible spiking LDI synapse fabricated using organic electronics on a flexible plastic substrate. The circuit is fabricated using complimentary p- and n-type organic materials. Following the fabrication, the organic field-effect transistors (OFETs) and the LDI synapses are characterized and compared before and during bending. We demonstrate that the synaptic circuit converts presynaptic voltage spikes to postsynaptic current. We also show that the magnitude of the postsynaptic current is proportional to the synaptic strength, adjusted via the weighing voltage \( V_W \). The time constant of LDI synaptic circuits is experimentally estimated and compared while flat and under strain. The strain shifted the threshold voltage \( (V_T) \) of the p- and n-type OFETs by 0.63 and 1.01 V, respectively. The estimated time constant with a 10 nF synaptic capacitor reached 126 and 221 ms before and during bending. Finally, the effect of disparity in capacitance, presynaptic signal, and weighting voltage are studied on the time constant under neutral and strain conditions.

2. Materials and Methods

2.1. Device Structure

The main elements of the LDI synaptic circuit are p- and n-type OFETs. Figure 1 shows the device stack with photographs of the flexible chip and both types of OFETs. The OFET structure is top-contact bottom-gate, consisting of the following layers: Polyimide (PI) substrate, Cr/Ag gate, Parylene diX-SR as gate dielectric, active layers of Dinaphtho[2,3-b:2′,3′-f][thieno][3,2-b] thiophene (DNTT), and \( N,N′\text{-bis(n-octyl)}\text{-x,y,di}c\text{yanoperylene-3,4,9,10-bis(dicarboximide)} \) (PDI-8CN2, also referred to as N1200) for p- and n-type OFETs, respectively, and Au as source and drain. The channel length and width are the same for both types of OFETs, at 100 and 1000 μm, respectively.

2.2. Characterization of Organic Transistors

The output and transconductance characteristics of individual OFETs and the entire LDI synaptic circuits are examined before (flat) and during bending to elucidate the effects of stress and compare their electrical properties. The bending radius is 4.5 inches (114.3 mm), and Figure 2 demonstrates the laboratory test setup, including individual micromanipulators used to directly contact individual circuit nodes (e.g., \( V_{DD}, I_{Syn}, \) or GND).

Figures 3 and 4 present representative examples of p- and n-type OFETs characterization results, shown with neutral and strain status with solid and dashed lines, respectively. Table 1 presents the OFETs’ characterization results in flat and bent conditions.

Bending shifts the threshold voltage \( (V_T) \) of the p- and n-type OFETs by 0.63 and 1.01 V toward more positive values and increases the mobility \( (μ) \) by 0.03 and 0.002 cm\(^2\) V\(^{-1}\) s\(^{-1}\), respectively. The carrier mobility of the n-type device is lower than the p-type, which decreases the switching speed of the device. The OFF current of p-type device remains constant before and during bending, 1.54 × 10\(^{-10}\) A at 20 V, while bending decreases the OFF current of n-type device by 2.4 nA at −30 V.

2.2.1. The Mechanisms of Hysteresis

Figures 3b and 4b show that \( I_D \) depends on \( V_{GS}' \)s sweep direction, known as the “hysteresis” phenomenon. Such reversible electrical bistabilities are often observed in OFETs. A variety of effects have been identified as causes, including charge trapping at the interface of the semiconductor and the dielectric, the dielectric polarization, injection of charges from the semiconductor/gate to the dielectric bulk, moving ions in the...
dielectric, and slow reaction of moving charge carriers,[42,43] While
hysteresis has been used as the basis of memory devices,[44]
generally it is seen as a negative effect with adverse effects on
the electrical circuits. As discussed later, it is likely one of the
culprits of subtle but noticeable changes in our synaptic circuit,
for instance affecting the time constant. Possible fabrication
strategies aiming to minimize hysteresis include replacing the
gate electrode, reducing the dielectric thickness, and adding
self-assembled monolayers (SAMs).[45]

2.3. Log-Domain Integrator Synapse

The electrical neural signals are transmitted through synapses
between individual neurons in the brain. A human nervous
system consists of $\approx 10^{16}$ synapses that permit the signals to
be transferred between neurons. There are two types of bio-
logical synapses, electrical and chemical. Chemical synapses
tend to transmit more complicated signals than electrical ones.
Chemical synapses convert the electrical activities of a presyn-
aptic neuron to the release of a chemical known as a neuro-
transmitter. Neurotransmitters bind to receptors, mechanical
elements in post-synaptic neurons, and initiate electrical
activities that may either be inhibitory or excitatory. Chemical
synapses play a critical role in the formation of memory; there-
fore, there has been a considerable research effort focusing on
emulating the synaptic functions.[46]

While several examples demonstrating functional perfor-
mances have been introduced in the literature, the log-domain
integrator (LDI) synaptic circuit represents a biologically real-
istic current-mode model of a chemical synapse.[21]

Figure 2 illustrates the LDI circuit schematic. It consists of
three p-type, one n-type OFET, and a capacitor. In order for the
circuit to function properly as a log-domain integrating circuits,
all of the p-type OFETs need to operate in the subthreshold
regime (otherwise the circuit works as a nonlinear and power-
hungry reset-and-discharge synapse). However, the intrinsic
characteristics of n-type OFETs (higher OFF current and lower
mobility than p-type OFET) make subthreshold operation
more challenging.[47] The OFF current of the n-type $M_{\text{pre}}$ OFET
(which acts as a switch turning the synaptic circuit ON or OFF)
is greater than the OFF current of p-type OFETs by approxi-
ately one order of magnitude ($6.92 \times 10^{-9}$ A compared with
$1.54 \times 10^{-10}$ A). Biasing p-type $M_{\tau}$ OFET in a $V_{GS}$ that produces
an $I_D$ greater than the OFF current of n-type $M_{\text{pre}}$ OFETs allows
for $M_{\text{pre}}$ to turn the circuit off, and the LDI synapse operates
appropriately, as will be demonstrated in Section 3.1. Assuming
all the p-type OFETs are working in a subthreshold regime, the

Figure 2. a) The characterization setup before (flat) and b) during bending, with individual micromanipulators used to access individual circuit nodes clearly visible.

Figure 3. a) Output and b) transconductance curves of the p-type organic transistor before (flat, solid line) and during (bent, dashed line) bending to a radius of 4.5 inches (114.3 mm), shown in Figure 2.
LDI synaptic behavior can be described as follows: a square pulse signal, which represents the presynaptic voltage spike, activates $M_{\text{pre}}$. When the $M_{\text{pre}}$ is ON, the gate voltage of $M_{\text{syn}}$ decreases with a rate set by $I_{\text{pre}}-I_{\text{s}}$ and the synaptic current ($I_{\text{syn}}$) increases following an exponential profile. At the onset of each presynaptic pulse, the capacitor discharges, and the $I_{\text{syn}}$ decreases exponentially. When the input voltage pulse ends, the $M_{\text{pre}}$ is turned OFF, the capacitor $C_{\text{syn}}$ is linearly recharged to $V_{\text{DD}}$ by the constant current through $M_{\text{s}}$, and the current through $M_{\text{syn}}$ decreases back to its leakage current levels. The parameter $V_{W}$ biases the gate of $M_{W}$ and sets the maximum efficacy of the synapse (i.e., the synaptic weight). The $M_{f}$ transistor needs to be biased to produce a current that compensates for the leakage current of the n-type $M_{\text{pre}}$ to charge the synaptic capacitor $C_{\text{syn}}$.

Figure 5b shows a photograph of the fabricated organic synapse. Individual OFETs are connected through 30-nm Au tracks immediately after source/drain deposition. A non-circuit-integrated commercial capacitor is deployed to expedite the fabrication and characterization process, as an integrated organic capacitor (part of our future efforts) would dramatically increase the complexity of the fabrication.

3. Results

3.1. Synaptic Circuit Characterization

As mentioned, one of the functions of a synapse is to weight, or scale, the presynaptic input signal via synaptic weights. Figure 6 illustrates the step response of the organic LDI synapse to a square wave with a cycle duration of 4 s, alternating between $-10$ and 10 V, to turn OFF and ON $M_{\text{pre}}$ based on the n-type OFET characterization results. The circuit’s response has been plotted for three synaptic weights ($V_{W}$) to demonstrate the circuit’s functionality in either signal attenuation or amplification. $M_{f}$ needs to produce a current greater than the OFF current of n-type $M_{\text{pre}}$ OFET, while $V_{\text{DS}}$ of $M_{f}$ is a value less than 1 V. Therefore, 9 V is applied to the gate of $M_{f}$ with $V_{\text{DD}} = 15$ V to compensate the leakage current of $M_{\text{pre}}$ when presynaptic voltage is $-10$ V. Table 2 summarized the experimental values.

The synaptic weight parameter $V_{W}$ modulates the height of the circuit’s response, namely the magnitude of the saturated synaptic current $I_{\text{syn}}$. Specifically, applying smaller $V_{W}$ values decreases $V_{\text{syn}}$, consequently elevating the peak of the output synaptic current ($M_{W}$ is a p-type OFET and the source of $M_{W}$ is connected to $V_{\text{DD}}$). Applying lower $V_{W}$ means smaller $V_{\text{GS}}$ ($V_{W} - V_{\text{syn}}$). If we consider that $V_{\text{syn}}$ is almost constant with a value close to $V_{\text{DD}}$, then $V_{\text{GS}}$ of $M_{W}$ depends only of $V_{W}$. Hence smaller $V_{W}$ means higher $I_{W}$. Consequently, $C_{\text{syn}}$ can recharge more and $V_{\text{GS}}$ of $M_{\text{syn}}$ varies more and produce taller peaks of $I_{\text{syn}}$. During the step input, while $M_{\text{pre}}$ is ON, $M_{f}$ produces a current that is approximately constant. As soon as the pre-synaptic voltage is turned to $-10$ V, $I_{f}$ starts charging $C_{\text{syn}}$, eventually turning off both $M_{\text{syn}}$ and $M_{s}$. The threshold voltage of p-type OFETs is a nonzero value in the characterizations; therefore, the $M_{\text{syn}}$ is not turned OFF, and $I_{\text{syn}}$ is biased to a constant value greater than zero. Either applying a voltage less than $V_{\text{GS}}$ to the source electrode of $M_{\text{syn}}$ or fabricating a p-type OFET with a threshold voltage close to 0–V will remove the bias from the result.

Ideally, the synaptic currents need to reach the same steady-state value with different $V_{\text{GS}}$; however, Figure 6 shows the $I_{\text{syn}}$ is marginally different at the end of the cycle ($t < 3$ s). Weighting voltages stimulate hysteresis mechanisms and lead to a discrepancy in the steady-state values.

3.2. Time Constant

Only the spikes that exhibit time constants comparable to the neuron’s membrane potential allow leaky integrate-and-fire
neurons to recognize the difference between temporal input spikes patterns.\cite{39} As such, synaptic circuits with time constants of milliseconds or seconds are critical. Silicon synaptic circuits have shown the same time constants as this study, but with smaller capacitors in the range of pico to femtofarads—partially due to the superior inorganic semiconducting technologies, such as carrier mobilities, lower OFF currents, and matching threshold voltages of p- and n-type devices. Moreover, organic semiconducting technology is relatively new compared with mature inorganic electronics. Therefore, further improvement in the fabrication of this study, regarding materials, deposition, and patterning methods, will yield organic synaptic circuits with a large time constant using smaller capacitors. Finally, organic materials naturally offer biocompatibility and flexibility, which are difficult or impossible for silicon technologies.

3.2.1. Experimental Time Constant

The governing equations of the LDI synaptic circuit are only valid when all p-type OFETs are operating in subthreshold regimes. However, because our p-type OFETs operate in a weak- and moderate-inversion regime, resulting in a quasi-linear circuit operation, the standard equations cannot be used directly to extract the circuit’s time constant.

LDI synaptic circuit implements a first-order low-pass filter; therefore, the time constant can be extracted from circuit’s step response.\cite{28} Regardless of the transistors’ operating regime, Figure 6 shows that the organic LDI synapse still works similarly to a first-order low-pass filter (the non-ideal behavior of the circuit seen as a difference in OFF currents, is likely caused by the hysteresis effect, which also contributes to a slight shift to the current over time). The time constant can be experimentally estimated through the circuit’s step response. Various methods exist to estimate the time constant of a first-order system.\cite{48–51} Indiveri et al. fitted the experimental data with an exponential equation to estimate the time constant.\cite{39} Equation (I) presents the exponential relationship between the synaptic current and the time constant. The fitting parameters are estimated using a particle swarm optimization algorithm.

\[
I_{syn} = \begin{cases} 
    a + b \times e^{-\frac{t}{\tau}} & \text{charge phase} \\
    c \times e^{-\frac{t}{\tau}} & \text{discharge phase}
\end{cases}
\]  

3.2.2. The Effects of Synaptic Capacitance on the Time Constant

The time constant is nonlinearly proportional to the synaptic capacitance when the p-type OFETs are not operating in the subthreshold regime.\cite{52} Two capacitors, 4.7 and 10–nF, are deployed to show the effects of synaptic capacitance on the time constant. In order for let \( M_L \) produces a current greater than the

| \( V_W \) [V] | \( C_{syn} \) [nF] | Presynaptic signal period/width [s] | \( V_c \) [V] | \( V_{DD} \) [V] |
|---|---|---|---|---|
| 9, 10, 11 | 10 | 4/2 | 9 | 15 |

Figure 5. a) Circuit diagram of the implemented organic log-domain integrator synapse. b) Photograph of an entire chip, with multiple organic circuits, with a zoomed view of a single log-domain integrator synapse on a Polyimide substrate shown above.

Figure 6. Step response of the log-domain integrator synapse for three different values of \( V_W \).
leakage current of $M_{\text{pre}}$ when presynaptic voltage is $-10 \text{ V}$, 9 V is applied to the gate electrode with $V_{\text{DD}} = 15 \text{ V}$. A square wave alternated between ±10 V with two different time periods—1 and 2 s—to simulate presynaptic voltage spikes. Table 3 shows a summary of the experimental parameters. The time constant is estimated for a captured cycle; therefore, presynaptic stimulations determine the number of estimated time constants in an experiment. In this experiment, 18 cycles are captured to estimate time constants. Whisker plots display patterns of estimated time constants in experiments.

Figures 7 and 8 show the Box plots of estimated time constants based on Section 3.2.1 for 4.7 and 10 nF synaptic capacitances. The time constant has been estimated for two periods of presynaptic signals for every synaptic capacitance. The time constant is independent of presynaptic signal periods and remained relatively unchanged for different periods of presynaptic signals before bending; however, during bending, the time constant increased due to the shifts in the threshold voltages. Also, the figures show disparities in medians and average values of time constants for the same conditions at the same synaptic capacitance for different presynaptic signal periods. This is likely due to three factors. First, the hysteresis mechanisms affect the value of the time constant during the captured periods. Second, the time constant estimation is intrinsically an error-prone process. Finally, the system is not precisely a first-order low-pass filter but a higher-order system with the first-order dynamics as the leading dynamic.

Tables 4 and 5 summarize the statistical information presented in Figures 7 and 8, respectively.

Figures S1 to S4, Supporting Information, demonstrate the synaptic current ($I_{\text{syn}}$) for the experiments shown in Section 3.2.2.

### Table 3. Experimental parameters discussed in Section 3.2.2.

| $V_{\text{W}}$ [V] | $C_{\text{syn}}$ [nF] | Presynaptic signal period/width [s] | $V_{\text{f}}$ [V] | $V_{\text{DD}}$ [V] |
|------------------|------------------|-----------------------------------|-----------------|-----------------|
| 10               | 4.7, -10         | 2/1, 1/0.5                         | 9               | 15              |

The weighting voltage and presynaptic signals have no role in determining the time constant; however, they do affect the saturation level of synaptic current. Two different weighing voltages ($V_{\text{W}}$ of 9.5 V, 9.8 V) and square wave shape presynaptic signal with two different time periods—2 and 4 s—have been applied to the LDI synaptic circuit. The experimental parameters are similar to the experiments discussed in Section 3.2.2 except the capacitance is constant (10 nF), and the weighing voltage and the periods of the presynaptic signal are varied. Table 6 summarizes the experimental parameters. In this experiment, 18 cycles are captured to estimate time constants. Whisker plots are deployed to show the statistical information regarding the experiment. Figures S5 and S6, Supporting Information show the synaptic currents with respect to time according to the parameters in the Table 6 before and during bending. Figures 9 and 10 present the box plots of experimentally estimated time constants according to Section 3.2.1 for 10 nF synaptic capacitance with presynaptic periods of 2 and 4 s and two weighing voltages. It can be seen that the time constant is independent of weighing voltage and period of the presynaptic signal, with noticeable changes between flat and bent devices. However, the results show disparities in the results for different weighing voltages. Also, the time constants need to be the same as what is shown in Figure 8 to show the independency of time constant from periods of presynaptic signals. The negligible disparity is mainly due to three reasons: 1) the hysteresis mechanisms that affect the time constants in a period of time, 2) the time constant extraction method that estimates the

### Table 4. Statistical information graphically shown in Figure 7 for $C_{\text{syn}} = 4.7 \text{ nF}$ discussed in Section 3.2.1 to study the effect of synaptic capacitance and pre-synaptic signal periods.

| Condition | $\text{Period}_{\text{pre}}$ [s] | Min [s] | Max [s] | Median [s] | Mean [s] |
|-----------|------------------|--------|--------|-----------|---------|
| Flat      | 2                | 67.15  | 70.58  | 68.21     | 68.50   |
| Bent      | 2                | 91.67  | 105.19 | 97.08     | 97.28   |
| Flat      | 1                | 66.45  | 68.21  | 67.03     | 67.08   |
| Bent      | 1                | 79.55  | 97.28  | 89.25     | 89.15   |

The weighting voltage and presynaptic signals have no role in determining the time constant; however, they do affect the saturation level of synaptic current. Two different weighing voltages ($V_{\text{W}}$ of 9.5 V, 9.8 V) and square wave shape presynaptic signal with two different time periods—2 and 4 s—have been applied to the LDI synaptic circuit. The experimental parameters are similar to the experiments discussed in Section 3.2.2 except the capacitance is constant (10 nF), and the weighing voltage and the periods of the presynaptic signal are varied. Table 6 summarizes the experimental parameters. In this experiment, 18 cycles are captured to estimate time constants. Whisker plots are deployed to show the statistical information regarding the experiment. Figures S5 and S6, Supporting Information show the synaptic currents with respect to time according to the parameters in the Table 6 before and during bending. Figures 9 and 10 present the box plots of experimentally estimated time constants according to Section 3.2.1 for 10 nF synaptic capacitance with presynaptic periods of 2 and 4 s and two weighing voltages. It can be seen that the time constant is independent of weighing voltage and period of the presynaptic signal, with noticeable changes between flat and bent devices. However, the results show disparities in the results for different weighing voltages. Also, the time constants need to be the same as what is shown in Figure 8 to show the independency of time constant from periods of presynaptic signals. The negligible disparity is mainly due to three reasons: 1) the hysteresis mechanisms that affect the time constants in a period of time, 2) the time constant extraction method that estimates the
parameter is intrinsically susceptible to error, and 3) the higher-order dynamics that affect the response. The threshold voltage shift caused an increase in the mean value of the time constant during bending. The statistical information regarding Figures 9 and 10 have been summarized in Table 7.

### 4. Conclusion

Synapses have two critical roles in neuromorphic systems, as individual interfaces with biological elements and forming abilities such as learning, memory, and cognition. Organic synaptic circuits offer advantages over silicon-based ones, including biocompatibility, flexibility, and large area covering. More importantly, the charge carrier mobilities of organic materials are slower than inorganic semiconductors, resulting in more plausible time constants. Furthermore, compared with individual devices used to emulate artificial synapses (e.g., two-terminal memristive devices), the multi-element synaptic circuits provide for a greater synaptic control, for instance via a continuously tunable weight or time constants.

There are two functions of a synapse. The first one is to convert presynaptic voltage spikes onto postsynaptic current. The second one is to scale, up or down, the magnitude of post-synaptic current according to so-called “synaptic weight” (which is adjusted during learning or training). We have demonstrated that our organic spiking synapse performs both of these functions, including the effects of synaptic weighting voltage $V_W$ and its effects on the postsynaptic current $I_{syn}$. This paper presents a biologically realistic current-mode model, linear charge and discharge, flexible organic log-domain integrator synapse consisting of three p-type, one n-type OFETs, and a capacitor. We also show that the time constant, estimated via fitting circuits step response, can reach 126 and 221 ms before and during bending when a 10 nF capacitor is deployed. We acknowledge large time constants can only be achieved using large capacitors. However, future improvements in individual device performance should lead to more practical, all-integrated solutions. The upgrades consist of 1) shrinking the dielectric thickness in the level of sub-100 nm to reduce the operating voltage, 2) lowering the OFF current to the level of pico-amps, and 3) pushing threshold voltages toward zero for both p-type and n-type OFETs to remove any biases in the synaptic current. While these current results are not ready to be interfaced with biological systems, the research outcome opens the door to more biologically plausible time constant and biocompatible synaptic circuits, as well as networks of fully organic spiking neurons.

### 5. Experimental Section

Materials and Methods: Dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT), as the p-type organic semiconductor, and N,N′-bis(n-octyl)-x:y,dicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI8-CN2, also referred to as N1200), as the n-type semiconductor were obtained from Sigma-Aldrich and Polyerra, respectively. Parylene diX-SR was purchased from Specialty Coating Systems Inc and grown using a chemical vapor deposition (CVD) process with SCS LabCoater 3 (PDS 2010). Chromium (Cr) rods, gold (Au), and silver (Ag) pellets were obtained from Kurt J. Lesker Company (KJLC). A NANO 36 thermal evaporation thin film deposition system by KJLC was exploited to deposit gate, source, drain, and active layers. An HP 4155A performed the $I$–$V$ measurements. The flexible Polyimide substrates—50 μm thick, precleaned, 75 × 50mm—are obtained from DuPont de Nemours, Incorporation. A National Instrument USB-6343 Data Acquisition Card and a ThorLabs

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### Table 5. Statistical information graphically shown in Figure 8 for $C_{syn} = 10$ nF and $V_{DD} = 10$ V.

| Condition | Period$_{presyn}$ [s] | Min [s] | Max [s] | Median [s] | Mean [s] |
|-----------|-----------------------|--------|--------|-----------|---------|
| Flat      | 2                     | 121.01 | 123.18 | 122.97    | 122.91  |
| Bent      | 2                     | 157.45 | 221.84 | 191.14    | 189.33  |
| Flat      | 1                     | 107.15 | 109.71 | 108.40    | 108.42  |
| Bent      | 1                     | 105.17 | 169.02 | 144.90    | 140.85  |

---

### Table 6. Experimental parameters shown in Section 3.2.3.

| $V_{DD}$ [V] | $C_{syn}$ [nF] | Presynaptic signal period/width [s] | $V_{I}$ [V] | $V_{DD}$ [V] |
|--------------|----------------|-----------------------------------|-------------|-------------|
| 9.5, 9.8     | 10             | 4/2, 2/1                           | 9           | 15          |

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Figure 9. Box plots of the estimated time constant for the log-domain integrator synapse with $C_{syn} = 10$ nF and Period$_{presyn} = 2$ s discussed in Section 3.2.1 to study the effect of weighting voltage and presynaptic signal period.

Figure 10. Box plots of the estimated time constant for the log-domain integrator synapse with $C_{syn} = 10$ nF and Period$_{presyn} = 4$ s discussed in Section 3.2.1 to study the effect of weighting voltage and presynaptic signal period.
Au was deposited as drain/source electrodes at the rate of 1.2 Å s⁻¹ of DNTT. The access to gate electrodes was obtained through the C during the deposition process. The temperature of the substrate was 60°C.

The data that support the findings of this study are available from the corresponding author upon reasonable request.

**Data Availability Statement**

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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**Conflict of Interest**

The authors declare no conflict of interest.

**Keywords**

neuromorphics, organic neuromorphics, flexible organic synaptic circuit, log-domain integrator synapse, biologically plausible time constant

**Supporting Information**

Supporting Information is available from the Wiley Online Library or from the author.

**Table 7. Statistical information regarding Figures 9 and 10 for C_{syn} = 10 nF.**

| V_{app} [V] | Condition | Period_{pre syn} [s] | Min [s] | Max [s] | Median [s] | Mean [s] |
|------------|-----------|----------------------|---------|---------|------------|---------|
| 9.5        | Flat      | 2                    | 122.46  | 126.38  | 124.23     | 124.12  |
| 9.5        | Bent      | 2                    | 155.40  | 179.64  | 167.66     | 167.43  |
| 9.8        | Flat      | 2                    | 115.98  | 121.09  | 119.07     | 118.84  |
| 9.8        | Bent      | 2                    | 158.64  | 198.24  | 170.57     | 174.02  |
| 9.5        | Flat      | 4                    | 119.99  | 125.01  | 122.16     | 122.25  |
| 9.5        | Bent      | 4                    | 172.68  | 185.13  | 177.82     | 178.73  |
| 9.8        | Flat      | 4                    | 121.86  | 125.29  | 123.92     | 123.71  |
| 9.8        | Bent      | 4                    | 160.99  | 207.77  | 180.75     | 182.49  |

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