Carry Select Adder Implementation using Asynchronous Fine Grain Power Gated Logic

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Abstract: This paper presents a low power logic family, called asynchronous fine-grain power-gated logic (AFPL). Each pipeline stage is comprised of the logic function called efficient charge recovery logic (ECRL) gates and a handshake controller. ECRL gates have negligible leakage power dissipation. By incorporating partial charge reuse (PCR) mechanism the energy dissipation required to complete the evaluation of an ECRL gate can be reduced. Moreover, AFPL-PCR adopts a C-label, in its handshake controllers. To mitigate the hardware overhead of the AFPL circuit, circuit simplification techniques have been developed.

Keywords: AFPL circuits, CSLA adders, PCR mechanism, ECRL logic gates.

1. Introduction

As the feature size continues to shrink and the transistor density increases, power dissipation has become an important concern in nanoscale CMOS VLSI design. As several features like threshold voltage, gate oxide thickness and channel length continue to shrink, leakage dissipation is becoming a significant contributor to the total power dissipation. Various techniques for reducing leakage loss have been proposed at the circuit level and also at the process technology levels. At the circuit level, transistor stacking, dual threshold CMOS, reverse body biasing, and channel length continue to shrink, leakage dissipation is becoming a significant contributor to the total power dissipation. Various techniques for reducing leakage loss have been proposed at the circuit level and also at the process technology levels. At the circuit level, transistor stacking, dual threshold CMOS, reverse body biasing, and power gating are the leakage reduction techniques. Power gating technique is highly efficient for leakage reduction. In general, power gating increase the resistance of leakage paths by inserting sleep transistors which are the power gating transistors used necessary. In the idle (sleep) mode, the sleep transistors are turned off and thus the leakage current is highly reduced; in the active mode the pull-up and pull-down networks are reconnected to power supply rails. For synchronous circuits, power gating can be implemented using the fine-grain which is at gate level or coarse-grain manner. The fine-grain power gating can considerably reduce leakage dissipation at run time when compared with coarse-grain power gating approach. A coarse-grain power-gated synchronous system has the following disadvantages: 1) it needs a complex power network 2) it requires wake-up current control to prevent ground bounce noise; 3) it has longer wake-up latency; and 4) it needs rigorous static and dynamic IR drop analysis.

Asynchronous circuits employ local handshaking protocol for transferring data, so they are data-driven type and becomes active only when doing work. That is, asynchronous circuits do not switch when inactive. Asynchronous circuits in inactive mode suffer leakage dissipation. Several techniques have been proposed recently for power gating to reduce the static power of asynchronous circuits.

Asynchronous circuits can be power-gated at the gate level of granularity. Method proposed was asynchronous adiabatic logic (AAL) for gate level. Each stage consists of a gate called as adiabatic, which implements the logic function of this stage, and a block called control and regeneration (C&R). When the control and regeneration block detects that the incoming input to the gate becomes a valid data, then the output of the C&R block transits to HIGH level, and the logic gate can acquire power; when the C&R block detects that the data input to the gate becomes empty, then the output of the block transits to LOW, and the adiabatic gate is not powered and remains idle. Unidirectional control signal (i.e., the output of the C&R block) accomplishes the synchronization between neighboring stages in rather than bidirectional handshake signals, so an asynchronous adiabatic logic circuit whose pipeline stages have diverse propagation delay may result in data values propagating along the pipeline stages to be overridden by its succeeding data token.

AFPL can achieve fine-grain power gating to tolerate static power dissipation without excess hardware overhead. The partial charge reuse (PCR) mechanism is combined with AFPL method to reduce the energy required to complete the evaluation of a logic block.

2. Literature Survey

AFPL can be combined with a mechanism called partial charge reuse (PCR). When AFPL incorporates this mechanism which is denoted by AFPL PCR, and that without PCR as AFPL w/o PCR. Fig. 1 shows the structure of the AFPL pipelines. In AFPL w/o PCR (without PCR) [see Fig.1(a)], a pipeline stage, denoted by Si, comprises of logic gate called efficient charge recovery logic gates Gi(ECRL) and a handshake controller Hi. In AFPL-PCR [see Fig.1(b)], denoted by Si, which is a pipeline stage, has an additional unit, the PCR unit PCri, which controls charge reuse between other pipeline stages Sj and Sk.
Figure 1: AFPL pipelines. (a) AFPL w/o PCR pipeline. (b) AFPL-PCR pipeline

There are two main differences between AFPL PCR and AFPL without PCR. First, AFPL-PCR employs the PCR unit PCR\(_{i+1}\) to control charge reuse between S\(_i\) and S\(_{i+2}\), which are the pipeline stages. Second, HC, the handshake controller in AFPL-PCR employs an enhanced C-element, which is called C\(^*\)-element to control the power node Vp\(_i\) of the ECRL gates. The enhanced element C\(^*\)-element has the advantage that an ECRL gate can discharge early if its outputs are no longer required, without waiting for next empty token to arrive at this stage. As shown in the Fig.1(b), in the PCR\(_{i+1}\) unit, transistor M2 is used as a diode, that allows the current to flow only in a direction from Vp\(_i\) to Vp\(_{i+2}\), and transistor M1 shown in the figure is used as a switch, which is turned on when charge reuse is activated.

In order to evaluate the effectiveness of the proposed AFPL, we have employed AFPL w/o PCR(AFPL without PCR) and AFPL-PCR to implement an eight-bit five-stage pipelined Kogge–Stone adder for performance comparison. Eight-bit five-stage pipelined Kogge–Stone adder is simulated using VHDL in Xilinx ISE Design Suite 8.1. Power consumption comparison is done for AFPL w/o PCR(AFPL without PCR) and AFPL-PCR mechanism. The AFPL w/o PCR (AFPL without PCR) implementation can reduce power dissipation by 19.1%–32.0%, and the AFPL-PCR implementation can reduce power dissipation by 30.6%–55.3%.

3. AFPL-PCR implementation of an Eight-Bit Five-Stage Pipelined Kogge–Stone adder

The Kogge Stone(KS) adder is a parallel prefix carry look ahead adder. It generates the carry signals of the adder circuit within O(log n) time, and is widely the fastest adder design. It is one of the common design for high-performance adders in industry. But it has large area. In this implementation, all ECRL gates in the same pipeline stage share a common handshake controller to mitigate the hardware overhead. The logic blocks of the Kogge–Stone adder consist of 83 ECRL gates (508 transistors); the handshake controllers and PCR units of the Kogge–Stone adder consist of 14 logic gates (83 transistors). That is, the handshake controllers and PCR units account for 14% of the total transistor count.

![Simulated result without using PCR mechanism](image)

Figure 3: Simulated result without using PCR mechanism
Figure 3 shows the power consumption for eight-bit five-stage pipelined Kogge–Stone adder without using PCR mechanism. The power rating has been estimated using Xilinx ISE 8.1 and the total estimated power consumption was found to be 819 mw.

![Figure 3: Power Consumption for Kogge–Stone Adder](image)

**Power Consumption Summary**
- Power at 1.80V: 391 mW
- Power at 3.30V: 27 mW

**Logic Utilization**
- Number of '1's: 44 out of 15,824, 1%
- Number of Flip Flops: 51 out of 35,524, 1%

**Power Distribution**
- Number of '1's: 45 out of 6,912, 1%
- Number of '0's containing '1's: 6 out of 4,206, 1%
- Number of '0's containing '0's: 8 out of 5,446, 1%

The total estimated power consumption was 819 mw.

**Conclusion**
- The total power consumption for the eight-bit five-stage pipelined Kogge–Stone adder without using PCR mechanism is 819 mw.

Figure 4 shows the power consumption for eight-bit five-stage pipelined Kogge–Stone adder using PCR mechanism. The power rating has been estimated using Xilinx ISE 8.1 and the total estimated power consumption was found to be 711 mw. In Kogge-stone adder, carries are generated fast by computing carries in parallel at the cost of increased area.

![Figure 4: Simulated Result Using PCR Mechanism](image)

**Power Consumption Summary**
- Power at 1.80V: 93 mW
- Power at 3.30V: 27 mW

**Logic Utilization**
- Number of '1's: 47 out of 35,524, 1%
- Number of Flip Flops: 11
- Number of '1's: 1 out of 29
- Number of '0's: 1 out of 29

The total equivalent gate count for design is 4,837.

**Additional Notes**
- Power Consumption: 1,304
- Peak Memory Usage: 192 KB

4. **Delay, Area and Power Evaluation of 16bit Conventional Carry Select Adder (CSLA)**

Carry Select Adder (CSLA) is used in many data processing systems which is the fastest adders to perform arithmetic functions faster. This method uses a simple and more efficient gate level modification to reduce the area and power of the CSLA. The proposed method has reduced area and power as compared to the regular SQRT CSLA adder with a slight increase in the delay. In this work the performance of proposed designs is evaluated in terms of delay, area, power, and their products by hand with the logical effort and using custom design and the layout of circuit in 0.18- m CMOS process technology. From the result it is(8,5),(989,986) clear that the proposed structure is better than the regular SQRT CSLA. The delay, area and power evaluation methodology considers all gates made up of AND, OR, and Inverter, each having delay and area equal to 1 unit. After that add the number of gates in the longest path of a logic system that is contributing the maximum delay. The area is evaluated by counting the total number of AOI (AND OR inverter) logic gates required for each logic block.

![Figure 5: Conventional Carry Select Adder (CSLA)](image)

**Power Consumption Summary**
- Power at 1.80V: 167 mW
- Power at 3.30V: 27 mW

**Logic Utilization**
- Number of '1's: 69, 125
- Number of '0's: 8, 15
- Number of '0's: 0
- Number of '1's: 0

**Conclusion**
- The total power consumption for the 16-bit conventional CSLA is 194 mw.

![Figure 6: Conventional Adder](image)

**Conclusion**
- The proposed structure is better than the regular SQRT CSLA.
5. Delay, Area and Power Evaluation Methodology of regular 16-b SQRT CSLA

The structure of 16-b regular SQRT CSLA is shown in the Fig. 7. It has five groups of different size RCA.

![Figure 7: Regular 16-b SQRT CSLA](image)

6. Delay, Area and Power Evaluation of Modified 16-b SQRT CSLA

The structure of the proposed 16-b SQRT CSLA adder using BEC (Binary to Excess-1 Converter) logic for RCA (Ripple carry adder) with carry input of the adder $c_{in}=1$ to optimize the area and power is shown in the Fig. 9.

![Figure 8: Regular 16-b SQRT CSLA](image)

![Figure 9: Modified 16-b SQRT CSLA](image)
Figure 10: Modified 16-b SQRT CSLA (a) area, (b) power, (c) time.

The proposed modified SQRT CSLA adder saves 113 gate areas than the regular SQRT CSLA adder, with only 11 increases in gate delays.

7. Inferences

KS-ADDER:

Timing Summary:

Speed Grade: -7

Minimum period: 3.589ns (Maximum Frequency: 278.66MHz)
Minimum input arrival time before clock: 35.960ns
Maximum output required time after clock: 34.270ns
Maximum combinational path delay: 42.892ns

CSA ADDER:

Timing Summary:

Speed Grade: -7

Minimum period: No path found
Minimum input arrival time before clock: 15.675ns
Maximum output required time after clock: 11.254ns
Maximum combinational path delay: 17.672ns

8. Conclusion

This paper has proposed the AFPL. In the AFPL circuit, the logic blocks become active only when performing useful computations, and the idle logic blocks were not powered and have negligible leakage power dissipation. The AFPL circuit employs ECRL logics to construct its logic blocks to avoid the occurrence of the short-circuit current from VDD.

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to the ground, and to eliminate the requirement for additional standalone pipeline latches.

The PCR mechanism can be incorporated in the AFPL circuit to form the AFPL-PCR circuit. The AFPL-PCR pipeline uses the enhanced C*-element in its handshake controllers (HC) such that an ECRL logic gate in the AFPL-PCR pipeline can enter the sleep mode early to reduce the leakage dissipation once the output has been received by the downstream pipeline stage. For the AFPL-PCR implementation of an eight-bit five-stage pipelined Kogge–Stone adder, power consumption is less than that without using PCR.

A method is proposed in this paper to reduce the area and power of SQRT CSLA architecture. The reduced number of gates of this work offers the greater advantage in the reduction of area and also the total power. The compared results shows that the modified SQRT CSLA adder has a slightly larger delay, but the area and power of the 16-b modified SQRT CSLA are significantly reduced. The modified CSLA architecture is therefore, low area, low power, simple and efficient for VLSI hardware implementation. Also it has lower power consumption than kogge stone adder.

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