A HIERARCHICALLY BLOCKED JACOBI SVD ALGORITHM
FOR SINGLE AND MULTIPLE GRAPHICS PROCESSING UNITS∗

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Abstract. We present a hierarchically blocked one-sided Jacobi algorithm for the singular value decomposition (SVD), targeting both single and multiple graphics processing units (GPUs). The blocking structure reflects the levels of GPU’s memory hierarchy. The algorithm may outperform MAGMA’s \texttt{dgesvd}, while retaining high relative accuracy. To this end, we developed a family of parallel pivot strategies on GPU’s shared address space, but applicable also to inter-GPU communication. Unlike common hybrid approaches, our algorithm in a single GPU setting needs a CPU for the controlling purposes only, while utilizing GPU’s resources to the fullest extent permitted by the hardware. When required by the problem size, the algorithm, in principle, scales to an arbitrary number of GPU nodes. The scalability is demonstrated by more than twofold speedup for sufficiently large matrices on a Tesla S2050 system with four GPUs vs. a single Fermi card.

Key words. Jacobi (H)SVD, parallel pivot strategies, graphics processing units

AMS subject classifications. 65Y05, 65Y10, 65F15

1. Introduction. Graphics processing units have become a widely accepted tool of parallel scientific computing, but many of the established algorithms still need to be redesigned with massive parallelism in mind. Instead of multiple CPU cores, which are fully capable of simultaneously processing different operations, GPUs are essentially limited to many concurrent instructions of the same kind—a paradigm known as SIMT (single-instruction, multiple-threads) parallelism.

SIMT type of parallelism is not the only reason for the redesign. Modern CPU algorithms rely on (mostly automatic) multi-level cache management for speedup. GPUs instead offer a complex memory hierarchy, with different access speeds and patterns, and both automatically and programmatically managed caches. Even more so than in the CPU world, a (less) careful hardware-adapted blocking of a GPU algorithm is the key technique by which considerable speedups are gained (or lost).

After the introductory paper [26], here we present a family of the full block [19] and block-oriented [19] one-sided Jacobi-type algorithms for the ordinary (SVD) and the hyperbolic singular value decomposition (HSVD) of a matrix, targeting both a single and the multiple GPUs. The blocking of our algorithm follows the levels of the GPU memory hierarchy; namely, the innermost level of blocking tries to maximize the amount of computation done inside the fastest (and smallest) memory of the registers and manual caches. The GPU’s global RAM and caches are considered by the mid-level, while inter-GPU communication and synchronization are among the issues addressed by the outermost level of blocking.

At each blocking level an instance of either the block-oriented or the full block Jacobi (H)SVD is run, orthogonalizing a sequence of pivot submatrices by the conceptually same algorithm at the lower level. Thus the overall structure of the algorithm is hierarchical (or recursive) in nature, and ready to fit not only the current GPUs, but also various other memory and communication hierarchies, provided that efficient, hardware-tuned implementations at each level are available.

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The Jacobi method is an easy and elegant way to find the eigenvalues and eigenvectors of a symmetric matrix. In 1958 Hestenes [20] developed the one-sided Jacobi SVD method, an implicit orthogonalization of a factor of a symmetric positive definite matrix. But, after discovery of the QR algorithm in 1961/62 by Francis and Kublanovskaya, the Jacobi algorithm seemed to have no future, at least in the sequential processing world, due to its perceived slowness [15]. However, a new hope for the algorithm has been found in its amenability to parallelization, in its proven high relative accuracy [9], and finally in the emergence of the fast Jacobi SVD implementation in LAPACK, due to Drmač and Veselić [13, 14].

In the beginning of the 1970s Sameh in [29] developed two strategies for parallel execution of the Jacobi method on Illiac IV. The first of those, the modulus strategy, is still in use, and it is one of the very rare parallel strategies for which a proof of convergence exists [24].

In the mid 1980s, Brent and Luk designed another parallel strategy [3], known by the names of its creators. The same authors, together with Van Loan [4], described several parallel one-sided Jacobi and Kogbetliantz (also known as “the two-sided Jacobi”) algorithms. The parallel block Kogbetliantz method is developed in [36].

In 1987 Eberlein [15] proposed two strategies, a round-robin strategy, and another one that depends on the parity of a sweep. A new efficient recursive divide-exchange parallel strategy, specially designed for the hypercube topologies (and, consequently, matrices of order $2^n$) is given in [16]. This strategy is later refined by Mantharam and Eberlein in [25] to block-recursive (BR) strategy.

Two papers by Luk and Park [23, 24] published in 1989 established equivalence between numerous strategies, showing that if one of them is convergent, all the strategies are convergent. In the same year Shroff and Schreiber [30] showed convergence for a family of strategies called the wavefront ordering, and discussed the parallel orderings weakly equivalent to the wavefront ordering, and thus convergent.

One of the first attempts of a parallel SVD on a GPU is a hybrid one, by Lahabar and Narayanan [22]. It is based on the Golub–Reinsch algorithm, with bidiagonalization and updating of the singular vectors performed on a GPU, while the rest of the bidiagonal QR algorithm is computed on a CPU. In MAGMA1, a GPU library of the LAPACK-style routines, dgesvd algorithm is also hybrid, with bidiagonalization (DGEBRD) parallelized on a GPU [35], while for the bidiagonal QR, LAPACK routine DBDSQR is used. We are unaware of any multi-GPU SVD implementations.

In two of our previous papers [33, 32] we discussed the parallel one-sided Jacobi algorithms for the hyperbolic SVD with two and three levels of blocking, respectively. The outermost level is mapped to a ring of CPUs which communicate according to a slightly modified modulus strategy, while the inner two (in the three-level case) are sequential and correspond to the “fast” (L1) and “slow” (L2 and higher) cache levels.

At first glance a choice of the parallel strategy might seem as a technical detail, but our tests at the outermost level have shown that the modified modulus strategy can be two times faster than the round-robin strategy. That motivated us to explore if and how even faster, yet still accurate strategies could be constructed. We present here a class of parallel strategies designed around a conceptually simple but computationally difficult notion of a metric on a set of strategies of the same order. These new strategies can be regarded as generalizations of the Mantharam–Eberlein BR strategy to all even matrix orders, outperforming the Brent and Luk and modified modulus strategies in our GPU algorithm.

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1 Matrix Algebra on GPU and Multicore Architectures, http://icl.utk.edu/magma/
However, a parallel strategy alone is not sufficient to achieve decent GPU performance. The standard routines that constitute a block Jacobi algorithm, like the Gram matrix formation, the Cholesky (or the QR) factorization, and the pointwise one-sided Jacobi algorithm itself had to be mapped to the fast, but in many ways limited shared memory of a GPU, and to the peculiar way the computational threads are grouped and synchronized. Even the primitives that are usually taken for granted, like the numerically robust calculation of a vector’s 2-norm, present a challenge on a SIMT architecture. Combined with the problems immanent to the block Jacobi algorithms, whether sequential or parallel, like the reliable convergence criterion, a successful design of the Jacobi-type GPU (H)SVD is far from trivial.

In this paper we show that such GPU-centric design is possible and that the Jacobi-type algorithms for a single and the multiple GPUs compare favorably to the present state-of-the-art in the GPU assisted computation of the (H)SVD. Since all computational work is offloaded to a GPU, we need no significant CPU ↔ GPU communication nor complex synchronization of their tasks. This facilitates scaling to a large number of GPUs, while keeping their load in balance and communication simple and predictive. While many questions remain open, we believe that the algorithms presented here are the valuable choice to consider when computing the (H)SVD on the GPUs.

The paper is organized as follows. In Section 2 a brief summary of the one-sided Jacobi-type (H)SVD block algorithms is given. In Section 3 new parallel Jacobi strategies—nearest to row-cyclic and to column-cyclic are developed. The main part of the paper is Section 4, where a detailed implementation of a single-GPU Jacobi (H)SVD algorithm is described. In Section 5, a proof-of-concept implementation on multiple GPUs is presented. In Section 6, results of the numerical testing are commented. Two appendices complete the paper with a parallel, numerically stable procedure for computing 2-norm of a vector, and some considerations about the Jacobi rotation formulas.

2. Jacobi-type SVD algorithm. Suppose that a matrix $G \in \mathbb{F}^{m \times n}$, where $\mathbb{F}$ denotes real ($\mathbb{R}$) or complex ($\mathbb{C}$) field, is given. Without loss of generality, we may assume that $m \geq n$. If not, instead of $G$, the algorithm will transform $G^*$. If $m \gg n$, or if the column rank of $G$ is less than $n$, then the first step of the SVD is to preprocess $G$ by the QR factorization with column pivoting [11] and possibly row pivoting or row presorting,

$$G = P_r Q R P_c = P_r Q \begin{bmatrix} R_0 \\ 0 \end{bmatrix} P_c,$$

where $Q$ is unitary, $R_0 \in \mathbb{F}^{k \times n}$ is upper trapezoidal with the full row rank $k$, while $P_r$ and $P_c$ are permutations. If $k < n$, then $R_0$ should be factored by the LQ factorization,

$$R_0 = P_r' L Q' P_c' = P_r' [L_0 \ 0] Q' P_c'.$$

Finally, $L_0 \in \mathbb{F}^{k \times k}$ is a lower triangular matrix of full rank. From the SVD of $L_0$, by (2.1) and (2.2), it is easy to compute the SVD of $G$. Thus, we can assume that the initial $G$ is square and of full rank $n$.

The one-sided Jacobi SVD algorithm for $G$ can be viewed as the implicit two-sided Jacobi algorithm which diagonalizes either $G^*G$ or $GG^*$. Let, e.g., $H := G^*G$. Stepwise, a pair of pivot columns $g_p$ and $g_q$ of $G$ are orthogonalized by applying a
single Jacobi plane rotation $\hat{V}_{pq}$, which diagonalizes a $2 \times 2$ pivot matrix $\hat{H}_{pq}$,

\begin{equation}
\hat{H}_{pq} = \begin{bmatrix}
\hat{h}_{pp} & \hat{h}_{pq} \\
\hat{h}_{qp} & \hat{h}_{qq}
\end{bmatrix} = \begin{bmatrix}
g_p g_p & g_p g_q \\
g_q g_p & g_q g_q
\end{bmatrix} = \begin{bmatrix}
g_p^* \\
g_q^*
\end{bmatrix} \begin{bmatrix}
g_p & g_q
\end{bmatrix},
\end{equation}

such that

\begin{equation}
\hat{V}_{pq}^* \hat{H}_{pq} \hat{V}_{pq} = \text{diag}(\hat{\lambda}_p, \hat{\lambda}_q).
\end{equation}

When the diagonalization process converges (numerically), we have $V = \prod \hat{V}$,

$$\Lambda = V^* H = (V^* G^*) (G V), \quad \Lambda = \text{diag}(\lambda_1, \lambda_2, \ldots, \lambda_n),$$

i.e., a resulting matrix $G V$ has orthogonal columns, and can be written as

\begin{equation}
G V = U \Sigma,
\end{equation}

where $U$ is unitary and $\Sigma = (\Lambda)^{1/2}$ is a diagonal matrix of the column norms of $G V$.

A matrix $U$ of the left singular vectors results from scaling the columns of $G V$ by $(\Lambda)^{-1/2}$, so only the right singular vectors $V$ have to be obtained, either by accumulation of the Jacobi rotations applied to $G$, or by solving a linear system (2.5) for $V$, with the initial $G$ preserved. The system (2.5) is usually triangular, since $G$ is either preprocessed in such a form, or already given as a Cholesky factor in an eigenproblem computation. Solving (2.5) is therefore faster than accumulation of $V$, but it needs more memory and may be less accurate if $G$ is not well-conditioned (see [12]).

The one-sided approach is better suited for parallelization than the two-sided one, since it can simultaneously process disjoint pairs of columns. This is still not enough to make a respectful parallel algorithm. In the presence of a memory hierarchy, the columns of $G$ and $V$ should be grouped together into block-columns,

\begin{equation}
G = \begin{bmatrix}
G_1 \\
G_2 \\
\vdots \\
G_b
\end{bmatrix}, \quad V = \begin{bmatrix}
V_1 \\
V_2 \\
\vdots \\
V_b
\end{bmatrix}.
\end{equation}

In order to balance the workload, the block-columns should be (almost) equally sized.

Usually, a parallel task processes two block-columns, i.e., a single pivot block-pair, either by forming a $2 \times 2$ pivot block-matrix $H_{pq}$ and its Cholesky factor $R_{pq}$,

\begin{equation}
H_{pq} = \begin{bmatrix}
G_1^* G_p & G_1^* G_q \\
G_2^* G_p & G_2^* G_q
\end{bmatrix} = \begin{bmatrix}
G_p^* \\
G_q^*
\end{bmatrix} \begin{bmatrix}
G_p & G_q
\end{bmatrix}, \quad (P^*) H_{pq} (P) = R_{pq}^* R_{pq},
\end{equation}

or by shortening the block-columns $[G_p \ G_q]$ directly, by the QR factorization,

\begin{equation}
[G_p \ G_q] (P) = Q_{pq} \begin{bmatrix}
R_{pq} \\
0
\end{bmatrix}.
\end{equation}

The diagonal pivoting in the Cholesky, or analogously, the column pivoting in the QR factorization should be employed, if possible (see [33] for further discussion, involving also the hyperbolic SVD case). Either way, a new, square pivot factor $R_{pq}$ is obtained. Note that a unitary matrix $Q_{pq}$ in the QR factorization does not have to be formed.

A variant of the Jacobi algorithm is then applied to $R_{pq}$. The following variants are advisable: block-oriented (see [18]), when the communication (or memory access) overhead between the tasks is negligible, and full block (see [19]) otherwise.
• Block-oriented: all the pivot pairs of $R_{pq}$ are transformed (at most) once, i.e.,
$$R'_{pq} = R_{pq} \tilde{V}_{pq},$$
with $\tilde{V}_{pq}$ being a product of the rotations applied in a sweep.

• Full block: $R_{pq}$ is fully orthogonalized, i.e., $R_{pq} V_{pq} = U_{pq} \Sigma_{pq}$.

Especially in the full block case, width of the block-columns should be chosen such that the pivot factors saturate, without being evicted from the fast local memory (e.g., the private caches) of a processing unit to which a subset of the block-columns is assigned. This also makes efficient blocking of the shortening operations possible.

Having computed $V'_{pq} = \tilde{V}_{pq}$ from the first, or $V'_{pq} = V_{pq}$ from the second variant, the original block-columns are updated,

$$(2.9) \quad [G'_p, G'_q] = [G_p, G_q] V'_{pq}, \quad [V'_p, V'_q] = [V_p, V_q] V'_{pq},$$

and (at least) one of the updated block-columns of $G$ (and $V$) is replaced by a block-column from another task. A completion of this exchange is a necessary synchronization point for the otherwise concurrent tasks.

The same blocking principle may be applied recursively, acting on $R_{pq}$. The recurrence terminates at the pointwise (non-blocked) Jacobi algorithm. In that way a hierarchical (or multi-level) blocking algorithm is created, with each blocking level corresponding to a distinct communication/memory domain (see [32]).

In the case of a multi-GPU system, we identify access to the global memory (RAM) of a GPU as slow compared to the shared memory and register access, and data exchange with another GPU as slow compared to access to the local RAM. This suggests the two-level blocking for a single-GPU algorithm, and the three-level for a multi-GPU one. Moreover, the latencies on every memory level are much higher than the speed of computation, so we adopt the full block variant at each of the levels.

Similar ideas hold also for the hyperbolic SVD (HSVD). If $G \in \mathbb{F}^{m \times n}$, $m \geq n$, and $\text{rank}(G) = \text{rank}(G J G^*)$, where $J = \text{diag}(\pm 1)$, then the HSVD of $G$ is (see [38])

$$(2.10) \quad G = U \begin{bmatrix} \Sigma & 0 \\ 0 & \end{bmatrix} V^*, \quad \Sigma = \text{diag}(\sigma_1, \ldots, \sigma_m), \quad \sigma_1 \geq \sigma_2 \geq \cdots \sigma_n \geq 0,$$

$U$ is a unitary matrix of order $m$, while $V$ is $J$-unitary, (i.e., $V^* J V = J$) of order $n$. The HSVD in (2.10) can be computed either by orthogonalization of the columns of $G^*$ by trigonometric rotations [10], or the columns of $G$ by hyperbolic rotations [37].

A diagonalization method for the symmetric definite (or indefinite) matrices requires only the partial SVD (or HSVD), i.e., the matrix $V$ is not needed. With the former algorithm, the eigenvector matrix $U$ should be accumulated, but with the latter, it is easily obtainable by scaling the columns of the final $G$. Thus, the hyperbolic algorithm is advantageous for the eigenproblem applications, as shown in [33].

In the sequel we assume $\mathbb{F} = \mathbb{R}$, but everything, save the computation of the Jacobi rotations and the hardware-imposed block sizes, remains also valid for $\mathbb{F} = \mathbb{C}$.

3. Parallel pivot strategies. In each step of the classical, two-sided Jacobi (eigenvalue) algorithm, the pivot strategy seeks and annihilates an off-diagonal element $h_{pq}$ with the largest magnitude. In the sequential one-sided algorithms this approach has a prohibitive overhead, since the scalar products of all columns have to be recomputed. In the parallel case there is an additional problem of finding $\lfloor n/2 \rfloor$ independent (their indices pairwise disjoint) off-diagonal elements with large magnitudes. Therefore, a cyclic pivot strategy—a repetitive, fixed order of annihilation of all off-diagonal elements of $H$—is more appropriate for the one-sided algorithms.
More precisely, a cyclic Jacobi strategy is a sequence of pivot pairs (pivots),

\[(p_k, q_k) \mid 1 \leq k \leq \tau, \quad \tau = \frac{n(n - 1)}{2},\]

where \((p_k, q_k)\) are taken from the strictly upper (or lower) triangle of the matrix. This sequence is traversed in cycles (also known as sweeps), until convergence criteria are met. Assuming that no repetitions of pivots occur, every pair of indices appears in the strategy exactly once. If a prescribed subset of \(f\) pivots is processed \(c > 1\) times in every cycle (i.e., \(\tau = n(n - 1)/2 + cf\)), the strategy is called quasi-cyclic.

A cyclic Jacobi strategy is perfectly parallel (p-strategy) if it simultaneously annihilates as many elements of \(H\) as possible, i.e., if for

\[t = \left\lfloor \frac{n}{2} \right\rfloor, \quad 1 \leq s \leq \begin{cases} n - 1, & n \text{ even}, \\ n, & n \text{ odd}, \end{cases}\]

exactly \(t\) independent pivots can be simultaneously processed in each of the \(s\) parallel steps (p-steps). As the p-strategies for an even \(n\) admit more parallelism within a p-step than those for \(n - 1\), with the same number of p-steps, we assume \(n\) to be even.

Besides the standard terminology of equivalent, shift-equivalent and weakly equivalent strategies [30], here we add a definition of a p-strategy closest to a given sequential strategy. The motivation was to explore whether a heuristic based on such a notion could prove valuable in producing fast p-strategies from the well-known row- and column-cyclic sequential strategies. The numerical testing (see Section 6) strongly supports an affirmative answer.

Let \(\mathcal{O}\) be a fixed cyclic Jacobi strategy. Then, for each possible pair of indices \((p, q)\) exists an index \(k\) such that \((p, q) = (p_k, q_k) \in \mathcal{O}\). For any cyclic strategy \(\mathcal{O}'\), and for each \((p'_k, q'_k) \in \mathcal{O}'\), there is \((p_{\ell(k)}, q_{\ell(k)}) \in \mathcal{O}\), such that

\[(p'_k, q'_k) = (p_{\ell(k)}, q_{\ell(k)}).\]

This induces \(I_\mathcal{O}\), a one-to-one mapping from the set of all cyclic Jacobi strategies on matrices of order \(n\) to the symmetric group \(\text{Sym}(\tau)\), as

\[I_\mathcal{O}(\mathcal{O}') = (\ell(1), \ell(2), \ldots, \ell(k), \ldots, \ell(\tau)) \in \text{Sym}(\tau),\]

with \(\ell(k)\) defined as in (3.1).

**Definition 3.1.** For any two cyclic Jacobi strategies, \(\mathcal{O}_1\) and \(\mathcal{O}_2\), we say \(\mathcal{O}_1\) is closer to \(\mathcal{O}\) than \(\mathcal{O}_2\), and denote that by \(\mathcal{O}_1 \preceq \mathcal{O}_2\), if \(I_\mathcal{O}(\mathcal{O}_1) \preceq I_\mathcal{O}(\mathcal{O}_2)\), where \(\preceq\) stands for the lexicographic ordering of permutations.

Similarly, the relation “strictly closer with respect to \(\mathcal{O}\)” could be defined and denoted by \(\prec\). Now, take \(\mathcal{O} \in \{\mathcal{R}_n, \mathcal{C}_n\}\), where \(\mathcal{R}_n\) and \(\mathcal{C}_n\) are row- and column-cyclic Jacobi strategies, respectively. Then there exists a unique p-strategy \(\mathcal{R}_n\) (resp. \(\mathcal{C}_n\)) that is closest to \(\mathcal{R}_n\) (resp. \(\mathcal{C}_n\)), since \(\preceq\) is a total order.

Interpreted in the graph-theoretical setting, a task of finding the closest p-strategy amounts to a recursive application of an algorithm for generating all maximal independent sets (MIS) in lexicographic order (e.g., [21]). Let \(G\) be a simple, connected graph with the vertices enumerated from 1 to \(\tau\), representing pivots from a prescribed \(\mathcal{O}\), and the edges denoting that two pivots collide (share an index). Note that \(|\text{MIS}(G)| \leq n\). Then a MIS(G) with \(n\) vertices is an admissible p-step, and vice versa. The same holds for a graph \(G' = G \setminus S\), where \(S\) is any admissible p-step.
Any permutation of the pivots in a p-step generates an equivalent (called step-equivalent) p-strategy, so the vertices in each MIS can be assumed to be sorted in ascending order. With a routine next_lex, returning the lexicographically next MIS with \( n \) vertices (or \( \emptyset \) if no such sets are left), Alg. 3.1 always produces \( \mathcal{O}^\parallel \), the p-strategy closest to \( \emptyset \). Note that, at the suitable recursion depths, next_lex could prepare further candidates in parallel with the rest of the search, and the parallel searches could also be launched (or possibly canceled) on the waiting candidates.

Algorithm 3.1: MIS-based generation of the p-strategy \( \mathcal{O}^\parallel \) closest to \( \emptyset \).

\[
\text{Description: Input: a graph } G \text{ induced by } \emptyset. \text{ Output: } \mathcal{O}^\parallel (\text{initially } \emptyset). \\
\text{boolean gen_strat(in } G) \\
\begin{align*}
\text{begin} \\
\text{if } G = \emptyset \text{ then return } \text{true}; \\
\text{begin loop} \\
\text{ } S \leftarrow \text{next_lex}(G); \\
\text{if } S = \emptyset \text{ then return } \text{false}; \\
\text{append } S \text{ to } \mathcal{O}^\parallel; \\
\text{if } \text{gen_strat}(G \setminus S) \text{ then return } \text{true}; \\
\text{remove } S \text{ from the back of } \mathcal{O}^\parallel; \\
\text{end loop}; \\
\text{end} \\
\end{align*}
\]

Alg. 3.1, however optimized, might still not be feasible even for the off-line strategy generation, with \( n \) sufficiently large. However, there are two remedies: first, no large sizes are needed due to the multi-level blocking; and second, we show in the sequel that it might suffice to generate \( \mathcal{R}^\parallel_n \) (or \( \mathcal{C}^\parallel_n \)) only for \( n = 2o \), with \( o \) odd.

**Lemma 3.2.** For all \( n \), \( S_n^{(1)} = ((2k - 1, 2k) \mid 1 \leq k \leq n/2) \) is the first p-step of \( \mathcal{R}^\parallel_n \) and \( \mathcal{C}^\parallel_n \).

**Proof.** \( S_n^{(1)} \) is an admissible p-step; e.g., Brent and Luk strategy starts with it, and we show that the same is true for any p-strategy closer to \( \mathcal{R}^\parallel_n \) or \( \mathcal{C}^\parallel_n \).

The first pivot in \( \mathcal{R}^\parallel_n \) and \( \mathcal{C}^\parallel_n \) is \((1, 2)\), i.e., \((2k - 1, 2k)\) for \( k = 1 \). After skipping over all colliding pivots in \( \mathcal{R}^\parallel_n \) or \( \mathcal{C}^\parallel_n \) (those that contain index 1 or 2), the first one that remains is \((3, 4)\), i.e., \((2k - 1, 2k)\) for \( k = 2 \). Inductively, after selecting a pivot \((2\ell - 1, 2\ell)\) and skipping over all pivots that contain \( 2k - 1 \) or \( 2k \), for all \( 1 \leq k \leq \ell < n/2 \), the first remaining pivot is \((2\ell' - 1, 2\ell')\) for \( \ell' = \ell + 1 \).

As an immediate consequence of Lemma 3.2, a matrix of order \( 2n \) can be regarded as a block matrix of order \( n \) with \( 2 \times 2 \) blocks, where the off-diagonal blocks are yet to be annihilated after the first p-step. Once we have \( \mathcal{O}^\parallel_n \), it is easy to construct the closest block p-strategy \( \mathcal{O}^\parallel_{2n} \), since each pivot of \( \mathcal{O}^\parallel_n \) corresponds uniquely to an off-diagonal block. A p-step of \( \mathcal{O}^\parallel_n \) is expanded to two successive p-steps of \( \mathcal{O}^\parallel_{2n} \). The expansion procedure is given by Alg. 3.2 and illustrated, for \( n = 6 \) and \( \mathcal{O} = \mathcal{R} \), with Fig. 3.1. Note that a pivot of \( \mathcal{O}^\parallel_n \) contributes two pairs, \((\mathcal{N}W, \mathcal{SE})\) and either \((\mathcal{NE}, \mathcal{SW})\) or \((\mathcal{SW}, \mathcal{NE})\), of independent and locally closest pivots in its corresponding block.

It's trivial to show that, with \( \mathcal{O}^\parallel_n \) given, a p-strategy \( \mathcal{O}^\parallel_{2n} \) generated by Alg. 3.2 is indeed the closest block p-strategy; any other such \( S^{\parallel}_{2n} \prec \mathcal{O}^\parallel_{2n} \) would induce, by the block-to-pivot correspondence, a strategy \( S_n \prec \mathcal{O}^\parallel_n \), which is impossible. Moreover, we have verified that, for \( n \leq 18 \) and both \( \mathcal{R} \) and \( \mathcal{C} \) strategies, \( \mathcal{O}^\parallel_{2n} = \mathcal{O}^\parallel_{2n} \), and although
**Algorithm 3.2**: Expansion of $O^\|_n$ to $\tilde{O}^\|_{2n}$ for $O \in \{R, C\}$.

**Description**: Input: $O^\|_n$, $O \in \{R, C\}$. Output: $\tilde{O}^\|_{2n}$. $S_m^{(i)}$: $j$-th $p$-step of $O^\|_m$ (or $\tilde{O}^\|_m$).

$S_{2n}^{(1)} \leftarrow \{(2k-1,2k) | 1 \leq k \leq n\}$;

for $i \leftarrow 2$ to $2n - 2$ do
  // construct $S_{2n}^{(i)}$
  $S_{2n}^{(i)} = \emptyset$;
  foreach $(p, q) \in S_n^{(i)}$ do
    if even$(i)$ then
      $NW = (2p - 1, 2q - 1)$; $SE = (2p, 2q)$; append $(NW, SE)$ to $S_{2n}^{(i)}$;
    else
      $NE = (2p - 1, 2q)$; $SW = (2p, 2q - 1)$;
      if $O = R$ then append $(NE, SW)$ to $S_{2n}^{(i)}$ else append $(SW, NE)$ to $S_{2n}^{(i)}$;
  end if
  end foreach
end for

**Fig. 3.1**: Expansion of $R^\|_6$ to $R^\|_{12}$, according to Alg. 3.2. From left to right: the black disks represent the odd $p$-steps, while the black squares stand for the even $p$-steps.

lacking a rigorous proof, claim that the same holds for all even $n$. Therefore, as a tentative corollary, to construct $O^\|_m$, for $O \in \{R, C\}$ and $m = 2^k a$, with $k > 1$ and $a$ odd, it would suffice to construct $O^\|_n$, $n = 2a$, and apply, $k - 1$ times, Alg. 3.2.

For example, a three-level blocking algorithm for 4 GPUs and a matrix of order $15 \cdot 1024$ requires $O^\|_8$, $O^\|_{240}$, and $O^\|_{32}$ strategies. To find $O^\|_{240}$, it suffices to construct $O^\|_{30}$, and expand (i.e., duplicate) 3 times, since $240 = 2^3 \cdot 2 \cdot 15$. Thus, the $O^\|_m$ strategies should be pretabulated once, for the small, computationally feasible orders
The strategies just described progress from the diagonal of a matrix outwards. However, if the magnitudes of the off-diagonal elements in the final sweeps of the two-sided Jacobi method are depicted, a typical picture [14, page 1349] shows that the magnitudes rise towards the ridge on the diagonal. That motivates us to annihilate the near-diagonal elements last, which is easily done by reverting $\tilde{\mathcal{R}}_n^\parallel$ and $\tilde{\mathcal{C}}_n^\parallel$. A reverse of the strategy $\mathcal{O}$ is a strategy $\hat{\mathcal{O}}$, given by

$$\hat{\mathcal{O}} := \{(p_{\tau-k+1}, q_{\tau-k+1}) \mid 1 \leq k \leq \tau, \quad (p_k, q_k) \in \mathcal{O}\}.$$ 

Thus, $\mathcal{R}_n^\parallel$ and $\mathcal{S}_n^\parallel$ progress inwards, ending with $\hat{\mathcal{S}}_n^{(1)}$ reversed. We tentatively denote the reverses of both $\mathcal{R}_n^\parallel$ and $\tilde{\mathcal{R}}_n^\parallel$ (resp. $\mathcal{C}_n^\parallel$ and $\tilde{\mathcal{C}}_n^\parallel$) by the same symbol.

For $m = 2^k$, both $\mathcal{R}_m^\parallel$ and $\mathcal{C}_m^\parallel$ can be generated efficiently by Alg. 3.1, since no backtracking occurs. In this special case it holds that $\mathcal{R}_m^\parallel = \tilde{\mathcal{R}}_m^\parallel$, $\mathcal{C}_m^\parallel = \tilde{\mathcal{C}}_m^\parallel$, and $\mathcal{R}_m^\parallel$ is step-equivalent to $\mathcal{C}_m^\parallel$. The former claims are verified for $k \leq 14$.

The respective reverses, $\mathcal{R}_m^\parallel$ and $\mathcal{S}_m^\parallel$, operate in the same block-recursive fashion (preserved by Alg. 3.2) of the Mantharam–Eberlein BR strategy [25], i.e., processing first the off-diagonal block, and then simultaneously the diagonal blocks of a matrix. It follows that all three strategies are step-equivalent. Thus, $\mathcal{R}_m^\parallel$ and $\mathcal{S}_m^\parallel$ can be regarded as the generalizations of the BR strategy to an arbitrary even order $n$, albeit lacking a simple communication pattern. Conversely, for the power-of-two orders, $\mathcal{R}_m^\parallel$ and $\mathcal{S}_m^\parallel$ might be replaced by the BR strategy with a hypercube-based communication.

4. A single-GPU algorithm. In this section we describe the two-level blocked Jacobi (H)SVD algorithm for a single GPU. The algorithm is designed and implemented with NVIDIA CUDA [6] technology, but is also applicable to OpenCL, and—at least conceptually—to the other massively parallel accelerator platforms.

We assume that the following CUDA operations are correctly rounded, as per IEEE 754-2008 standard [27]: $+\, -\, \times\, /\, \sqrt{x}, \ fma(x, y, z) = x \cdot y + z$, and $\text{rcp}(x) = 1/x$. Under that assumption, the algorithm may work in any floating-point precision available, but is tested in double precision only, on Fermi and Kepler GPU architectures.

The algorithm performs all computation on a GPU, and consists of 3 kernels:

1. $\text{initV}$ – initialization of $V^{(-T)}$ to $I$ (if the full SVD is requested);
2. $\text{pStep}$ – invoked once for each p-step in a block-sweep;
3. $\text{Sigma}$ – a final singular value extraction ($\sigma_i = \|g_i\|_2$).

The CPU is responsible only for the main control flow, i.e., kernel invocations and testing of the stopping criterion. Besides a simple statistics from each $\text{pStep}$ call, there is no other CPU $\leftrightarrow$ GPU data transfer. We assume that input factor $G$ is preloaded onto a GPU. We keep $J$ partitioned as $J = \text{diag}(I, -I)$ and represent it with a parameter $n_+$, where $n_+$ denotes the number of positive signs in $J$. The output data remaining on the GPU are $G' = U\Sigma$ (overwrites $G$), $\Sigma$, and (optionally) $V^{(-T)}$.

Data layout (i.e., array order) is column-major (as in Fortran), to be compatible with (cu)BLAS and other numerical libraries, like MAGMA. We write one-based array indices in parentheses, and zero-based ones in square brackets.

The matrices $G$ and $V$ are partitioned into $b = n/16$ block-columns, as in (2.6). To simplify the algorithm, $n$ must be divisible by 16 and $b$ must be even. Otherwise, if $n$ is not divisible by 32, $G$ has to be bordered as in [26, eq. (4.1)]. The reason lies in the hardware constraints on the GPU shared memory configurations and a fixed warp size (32 threads), as explained in the sequel.
We focus on pStep kernel, since the other two are straightforward. An execution grid for pStep comprises b/2 thread blocks, i.e., one thread block per a pivot block-pair. Each 2-dimensional thread block is assigned \(32 \times 16 = 512\) threads, and 16 kB of the GPU shared memory. That imposes a theoretical limit of 3 thread blocks per a multiprocessor, 100% occupancy on a Fermi, and 75% occupancy on a Kepler GPU.

A chosen block p-strategy \(S_b\) is preloaded in the constant or global GPU memory in a form of an \(O(1)\) lookup table \(S_b\). A thread block \(b\) in a pStep invocation \(s\) during a block-sweep \(r\) obtains from \(S_b\) the indices \(p\) and \(q\), \(1 \leq p < q \leq b\), of the block-columns \(t\) is about to process. In other words, a mapping \((r,s,t) \mapsto (p,q) \in S_b\) establishes a correspondence between the thread blocks and the pivot block-pairs.

A thread block behavior is uniquely determined by the block indices \(p\) and \(q\), since the thread blocks in every pStep invocation are mutually independent. Computation in a thread block proceeds in the three major phases:

1. **factorize** – shortens the pivot block-pair \([G_p \ G_q]\), according to (2.7) or (2.8), into a triangular factor \(R_{pq}\) of order 32, and initializes \(V'_{pq} = I_{32}\);
2. **orthogonalize** – orthogonalizes \(R_{pq}\) by the block-oriented or the full block variant of the Jacobi (H)SVD algorithm, accumulating the applied rotations into \(V'_{pq}\);
3. **postmultiply** – postmultiplies \([G_p \ G_q]\), and optionally \([V_p \ V_q]\), by \(V'_{pq}\), according to (2.9).

The matrices \(R_{pq}\) and \(V'_{pq}\) reside in the shared memory, and together occupy 16 kB. The entire allocated shared memory may also be regarded as a single \(64 \times 32\) double precision matrix, named \(G_{pq}\), of which \(R_{pq}\) aliases the lower, and \(V'_{pq}\) the upper half.

There is no shared memory configuration that can hold two square double precision matrices of order that is a larger multiple of the warp size than 32. It is therefore optimal to use the smallest shared memory configuration (16 kB), leaving the highest amount (48 kB) of the L1 cache available. Also, since \(R_{pq}\) and \(V'_{pq}\) have to be preserved between the phases, all phases need to be completed in the same kernel invocation. That creates a heavy register pressure, which is the sole reason why only one thread block (instead of 3) can be active on a multiprocessor.

In the complex case \((F = C)\), the shared memory configuration would be 48 kB (suboptimal, 16 kB unutilized) or 32 kB, for a Fermi or a Kepler GPU, respectively.

We present two approaches for factorize. The Cholesky factorization of the Gram matrix \(H_{pq}\), as in (2.7), is described in Subsection 4.1 in two subphases, and the QR factorization (2.8) is discussed in Subsection 4.2.

### 4.1. The Cholesky factorization

The first subphase of factorize loads the successive \(64 \times 32\) chunks of \([G_p \ G_q]\) into \(G_{pq}\). For a thread with the Cartesian indices \([x,y]\) in our thread block, \(x\) is its lane ID, and \(y\) its warp ID. Let \(y' = y + 16\) onwards. After a chunk is loaded, a thread \([x,y]\) then updates \(H_{pq}[x,y]\) and \(H_{pq}[x,y']\) (kept in its registers and being initially 0),

\[
H_{pq}[x,y] += G_{pq}[; , x]^{T} G_{pq}[; , y], \quad H_{pq}[x,y'] += G_{pq}[; , x]^{T} G_{pq}[; , y'].
\]

Finally, when all the chunks are processed, \(H_{pq}\) is written into \(R_{pq}\), and \(V'_{pq}\) is set to \(I_{32}\). Note that data in the GPU RAM are accessed only once. No symmetrization is needed for \(H_{pq}\), since only its lower triangle is taken as input for the Cholesky factorization. For details of this subphase see Alg. 4.1.

On a Kepler GPU, with 8 bytes wide shared memory banks, each thread in a warp can access a different bank. Due to column-major data layout, each of 32 consecutive (modulo 64) rows of \(G_{pq}\) belongs to a separate bank. Therefore, the modular row
Algorithm 4.1: Device function that computes the Gram matrix $H_{pq}$.

**Description:** Input: $[G_p \ G_q]$. Output: $H_{pq}$. Thread ID: $[x, y]$.

```plaintext
x' = x + 32; \quad y' = y + 16; \quad h_{x'y'} = h_{x'y'} = 0; \quad // H_{pq} elements kept in registers
for (i = x; i < n; i += 64) \quad // process the next chunk of $[G_p \ G_q]$
    \begin{cases}
        G_{pq}[x, y] = G_p[i, y]; & \quad G_{pq}[x, y'] = G_q[i, y]; \quad // load the first 32 chunk rows
        G_{pq}[x', y] = G_p[i', y]; & \quad G_{pq}[x', y'] = G_q[i', y]; \quad // load the remaining chunk rows
    \end{cases}
end if
\_syncthreads(); \quad // ensure the shared memory writes have taken effect
\_unrolled for (j = 0; j < 64; ++j) \quad // compute the partial dot-products
    \begin{cases}
        j' = (x + j) \mod 64; & \quad // modular row addressing avoids bank conflicts
        g_{j'x} = G_{pq}[j', x]; \quad g_{j'y} = G_{pq}[j', y]; \quad g_{j'y'} = G_{pq}[j', y'];
        h_{xy} = fma(g_{j'x}, g_{j'y}, h_{xy}); \quad // update $H_{pq}[x, y]$
        h_{xy'} = fma(g_{j'x}, g_{j'y'}, h_{xy'}); \quad // update $H_{pq}[x, y']$
    \end{cases}
end for
\_syncthreads(); \quad // ensure that $G_{pq}$ is free to be overwritten
\_unrolled for R_{pq}[x, y] = h_{xy}; \quad R_{pq}[x, y'] = h_{xy'}; \quad // store (unsymmetrized) $H_{pq}$ to $R_{pq}$
\_syncthreads(); \quad // ensure the shared memory writes have taken effect
```

Addressing of Alg. 4.1 guarantees bank-conflict-free operation on a Kepler GPU, and generates 2-way bank conflicts on a Fermi GPU, with 4 bytes wide banks.

The next subphase consists of the in-place, forward-looking Cholesky factorization of $H_{pq}$ without pivoting, i.e., $H_{pq} = L_{pq}L_{pq}^T$. The factorization proceeds columnwise to avoid bank conflicts. After the factorization, the upper triangle of $R_{pq}$ is set to $L_{pq}^T$, and the strict lower triangle to zero. This transposition is the only part of the entire algorithm that necessarily incurs the bank conflicts. The factorization has 32 steps. A step $k$, for $0 \leq k < 32$, transforms $H_{pq}[k: k]$ in 2 or 3 stages:

(a) Compute $L_{pq}[k: k]$, overwriting $H_{pq}[k: k]$ (see Fig. 4.1(a)). Only one warp is active. A thread $[x, y]$ performs the following:
   - If $x = y = k$, then $L_{pq}[k, k] = \sqrt{H_{pq}[k, k]}$;
   - else, if $x > y = k$, then $L_{pq}[x, k] = H_{pq}[x, k] / \sqrt{H_{pq}[k, k]}$;
   - else, a thread is dormant, i.e., does nothing.

(b) Update at most 16 subsequent columns of $H_{pq}$. Let $j = (k + 1) + y$. If $x \geq j$ and $j < 32$, then $H_{pq}[x, j] = fma(-L_{pq}[x, k], L_{pq}[j, k], H_{pq}[x, j])$, else do nothing (see Fig. 4.1(b)).

(c) If there are more columns remaining, let $j' = (k + 1) + y'$. If $x \geq j'$ and $j' < 32$, then $H_{pq}[x, j'] = fma(-L_{pq}[x, k], L_{pq}[j', k], H_{pq}[x, j'])$, else do nothing (see Fig. 4.1(c)).

After each stage, a thread-block-wide synchronization (\_syncthreads) is necessary.

4.2. The QR factorization. When the input matrix $G$ is badly scaled, the QR factorization (2.8) is required at all blocking levels, since the input columns of too large (resp. too small) norm could cause overflow (resp. underflow) while forming the Gram matrices. If the QR factorization employs the Householder reflectors, the

\[2\text{Could possibly be faster if implemented as } L_{pq}[x, k] = H_{pq}[x, k] \star \text{rsqrt}(H_{pq}[k, k]).\]
column norm computations should be carried out carefully, as detailed in Appendix A.

The tall-and-skinny in-GPU QR factorization is described in [2]. It is applicable when a single QR factorization per a p-step is to be performed on a GPU, e.g., in the shortening phase of a multi-GPU algorithm. On the shared memory blocking level, each thread block has to perform its own QR factorization. Therefore, an algorithm for the batched tall-and-skinny QRs is needed in that case.

Ideally, such an algorithm should access the GPU RAM as few times as possible, and be comparable in speed to the Cholesky factorization approach. We show that the algorithm can be made to access $[G_p \ G_q]$ exactly once, but the latter remains difficult to accomplish.

Let $A^{(0)}_0$ and $A^{(0)}_1$ be the $32 \times 32$ matrices that alias the lower and the upper half of $G_{pq}$, i.e., $R_{pq}$ and $V_{pq}'$, respectively. The first $32 \times 32$ chunk of $[G_p \ G_q]$ is loaded into $A^{(0)}_0$ and factorized as $A^{(0)}_0 = G^{(0)}_0 R^{(0)}_0$. The factorization is performed by 31 successive applications of the Householder reflectors, in a pattern similar to Fig. 4.1(b,c). A reflector is simultaneously computed in all active warps before the update, but is not preserved, and $Q^{(0)}_0$ is not (explicitly or implicitly) formed.

More precisely, for $0 \leq k < 31$, a Householder reflector annihilating the subdiagonal of a column $k$, $H_k = I_{32} - \tau_k w_k w_k^T$, where $w_k = [0 \ 1 \ v_k]^T$ ($0$ is a vector of $k$ zeros), is represented in a thread with the row index $x$ by $\tau_k$ and $w_k[x]$.

When the reflector is found, a warp $y$ transforms $A^{(0)}_0[x, \ell]$ for $\ell = k + y$. Let $z_\ell$ be a scalar product $z_\ell = w_\ell^T A^{(0)}_0[:, \ell]$, computed by warp-level shared memory reduction (on Fermi), or by warp shuffle reduction (on Kepler). Then,

$$A^{(0)}_0[x, \ell]' = \text{fma}(-\tau_\ell \ast z_\ell, w_\ell[x], A^{(0)}_0[x, \ell]).$$

The transformation is then repeated for $\ell' = k + y'$.

After $R^{(0)}_0$ is formed, the second chunk of $[G_p \ G_q]$ is loaded into $A^{(0)}_1$ and similarly factored as $A^{(0)}_1 = Q^{(0)}_1 R^{(0)}_1$.

The factors $R^{(0)}_0$ and $R^{(0)}_1$ are combined into $R^{(1)}_0$ by a “peel-off” procedure illustrated with Fig. 4.2. The procedure peels off one by one (super)diagonal of $R^{(0)}_1$ by the independent Givens rotations, until (after 32 stages) $R^{(0)}_1$ is reduced to a zero matrix. In a stage $k$, a row $x$ of $R^{(0)}_0$ and a row $x - k$ of $R^{(0)}_1$ are transformed by a rotation determined from $R^{(0)}_0[x, x]$ and $R^{(0)}_1[x - k, x]$ such to annihilate the latter. This is the main conceptual difference from the tall-and-skinny QR, described e.g. in [7, 8], where the combining is performed by the structure-aware Householder reflectors. The Givens rotations are chosen to avoid the expensive column norm computations.
Each remaining chunk of \([G_p, G_q]\) is loaded into \(A_1^{(i)}\), factored as \(A_1^{(i)} = Q_1^{(i)} R_1^{(i)}\), and combined with \(R_0^{(i)}\) to obtain \(R_0^{(i+1)}\). After the final \(R_{pq} = R_{0/(n/32-1)}\) is formed, \(V_{pq}'\) is set to \(I_{32}\).

Unfortunately, this approach is not recommendable when efficiency matters. For example, on matrices of order \(3072\), the QR factorization is \(12–15\) times slower than the Cholesky factorization, depending on the column norm computation algorithm.

### 4.3. The orthogonalization

In this phase, the inner pointwise Jacobi (H)SVD algorithm is run on \(R_{pq}\). A constant memory parameter \(M_s\), representing the maximal number of inner sweeps, decides whether the block-oriented \((M_s = 1)\) or the full block variant \((M_s > 1, \text{usually} M_s = 30)\) should be performed.

The inner p-strategy \(S'_{32}\) is encoded into a constant memory lookup table \(S'_{32}\). In principle, \(S'\) need not belong to the same p-strategy equivalence class as \(S\).

In each p-step \(s\) of an inner sweep \(r\), warp \(y\) is assigned a pivot pair \((p, q) = S'_{32}(r, s)[y]\), i.e., a pair of columns \([g_p, g_q]\) of \(R_{pq}\), and a pair of columns \([v_p, v_q]\) of \(V_{pq}'\). Then, the following subphases are executed:

1. The \(2 \times 2\) pivot matrix \(\hat{H}_{pq}\) from (2.3) is computed. As explained in Subsection 4.3.1, three dot products (for \(\hat{h}_{pq}, \hat{h}_{pp}, \text{and} \hat{h}_{qq}\)) are needed when the rotation formulas from [11] are not used. The elements \(g_p[x], g_q[x], v_p[x], \text{and} v_q[x]\) are preloaded into registers of a thread with lane ID \(x\), so, e.g., \(V_{pq}'\) may be overwritten as a scratch space for warp-level reductions on Fermi GPUs.

2. The relative orthogonality criterion for \(g_p\) and \(g_q\) is fulfilled if

\[
|\hat{h}_{pq}| < c(\varepsilon) \sqrt{\hat{h}_{pp} \hat{h}_{qq}} = c(\varepsilon) \|g_p\|_2 \|g_q\|_2,
\]

where \(c(\varepsilon) = \varepsilon \sqrt{n}\), and \(n\) is the matrix order (here, \(n = 32\)). If \(g_p\) and \(g_q\) are relatively orthogonal, then set an indicator \(\rho_s\), which determines whether a rotation should be applied, to \(\rho_s = 0\) and go to subphase 5, else set \(\rho_s = 1\).

3. Compute \(\alpha_s = (\Sigma \rho_s)/32\), a thread-block-wide number of warps about to perform the rotations, as \(-\_\_\_\_s\_syncthreads_count(\rho_s)/32\). Since the pointwise Jacobi process stops if no rotations occurred in a sweep, we have to increase a per-sweep counter of rotations, \(A_r\), by \(\alpha_s\).

4. Let the pivot indices \(p\) and \(q\) correspond to columns \(k\) and \(\ell\), respectively, of the input factor \(G\). If \(k \leq n_+ < \ell\), then compute \(\tilde{V}_{pq}\) from (2.4) as a hyperbolic rotation (4.2), else as a trigonometric one (4.1), according to Subsection 4.3.1. If \(c \varphi \neq 1\), then set \(\rho'_s = 1\) (a proper rotation), else leave \(\rho'_s = 0\) to indicate that the rotation is nearly identity.
5. If the rotation is trigonometric, find the new diagonal elements, $\hat{h}'_{pp}$ and $\hat{h}'_{qq}$,

$$
\hat{h}'_{pp} = \text{fma}(\tan \varphi, \hat{h}_{pq}, \hat{h}_{pp}), \quad \hat{h}'_{qq} = \text{fma}(-\tan \varphi, \hat{h}_{pq}, \hat{h}_{qq}).
$$

If $\rho = 0$ (i.e., $\hat{V}_{pq}$ is identity), take $\hat{h}'_{pp} = \hat{h}_{pp}$ and $\hat{h}'_{qq} = \hat{h}_{qq}$. To keep the eigenvalues sorted decreasingly \[19\], if $\hat{h}'_{pp} < \hat{h}'_{qq}$ when $\ell \leq n_+$, set $P_2 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$, else $P_2 = I_2$. Define

$$
\hat{V}'_{pq} = \hat{V}_{pq}P_2.
$$

The eigenvalue order tends to eventually stabilize, thus no swapping is usually needed in the last few sweeps \[26\]. If the rotation is hyperbolic, set $\hat{V}'_{pq} = \hat{V}_{pq}$, i.e., keep $J$ partitioned. An unpartitioned $J$ could lead to slower convergence \[31\].

6. Apply, per thread, $\hat{V}'_{pq}$ to $[g_p[x] \ g_q[x]]$ and $[v_p[x] \ v_q[x]]$ from the right, and store the new values into shared memory.

7. Compute $b_s = (\Sigma \rho'_s)/32$, similarly to subphase 3, and increase a per-sweep counter of proper rotations $B_r$ by $b_s$. This concludes the actions of one p-step.

After sweep $r$ finishes, update $B$, a total number of proper rotations in the thread block, by $B_r$. If $A_r = 0$, or $r = M_s$, thread $[0, 0]$ atomically adds $B$ to a global rotation counter $B$, mapped from the CPU memory. More details about a GPU-wide stopping criterion can be found in Subsection 4.5. This ends orthogonalize phase.

### 4.3.1. The Jacobi rotations.

The numerically stable, state-of-the-art procedure of computing the trigonometric Jacobi rotations is described in \[11\]. The procedure relies on computing the column norms reliably, as described in Appendix A.

The rest of the computation from \[11\] is straightforward to implement. Since the entire shared memory per a thread block is occupied, storing and updating the column scales, as in \[1\], is not possible without changing the shared memory configuration and reducing the L1 cache. The memory traffic that would thus be incurred over-weights the two additional multiplications by a cosine per a GPU thread. Therefore, rotations in the following form ($\text{fma}$ followed by a multiplication, if $\cos \varphi \neq 1$) are chosen,

$$
\begin{bmatrix}
g'_p \\
g'_q
\end{bmatrix} = \cos \varphi \begin{bmatrix}
g_p \\
g_q
\end{bmatrix} \begin{bmatrix}
1 & \tan \varphi \\
-\tan \varphi & 1
\end{bmatrix}.
$$

Together with DRDSSQ, we call such a procedure DDRJAC. The hyperbolic rotations may be computed similarly to the trigonometric ones, as in \[11\], in the form

$$
\begin{bmatrix}
g'_p \\
g'_q
\end{bmatrix} = \cosh \varphi \begin{bmatrix}
g_p \\
g_q
\end{bmatrix} \begin{bmatrix}
1 & \tanh \varphi \\
\tanh \varphi & 1
\end{bmatrix}.
$$

On a Fermi GPU (matrix order 6144), DDRJAC is only 14% slower than a simple procedure we discuss in the sequel. However, protection from the input columns of too large (or too small) norm that DDRJAC offers has to be complemented by the QR factorization at all blocking levels, which is extremely expensive.

Assume instead that the Gram matrix formation, the ordinary scalar products, and the induced norm computations never overflow. Using only correctly rounded arithmetic, $\cos \varphi$ and $\tan \varphi$ of (4.1), or $\cosh \varphi$ and $\tanh \varphi$ of (4.2), may be computed...
as in (4.3)–(4.6) (an adapted version of the Rutishauser formulas [28]):

\begin{align}
\text{(4.3)} & \quad h = \hat{h}_{qq} - t \cdot \hat{h}_{pp}; \quad \text{ct } 2\varphi = t \cdot \frac{h}{2\hat{h}_{pq}}; \\
\text{(4.4)} & \quad |\text{ct } \varphi| = |\text{ct } 2\varphi| + \sqrt{\text{fma}(\text{ct } 2\varphi, \text{ct } 2\varphi, t)}; \\
\text{(4.5)} & \quad t_n = \text{sgn}(\text{ct } 2\varphi) \cdot \text{rcp}(|\text{ct } \varphi|); \\
\text{(4.6)} & \quad \text{cs}_1 \varphi = \text{rcp}\left(\sqrt{\text{fma}(t \cdot t_n \varphi, t_n \varphi, 1)}\right); \quad \text{cs}_2 \varphi = \frac{|\text{ct } \varphi|}{\sqrt{\text{fma}(|\text{ct } \varphi|, |\text{ct } \varphi|, t)}}.
\end{align}

For \( t = 1 \), (4.3)–(4.6) produce the parameters of a trigonometric (ct = cot, \( t_n = \tan \), cs = cos) and \( t = -1 \) a hyperbolic (ct = coth, \( t_n = \tanh \), cs = cosh) rotation. If, numerically, \(|\text{ct } 2\varphi| = 1\), it is substituted by 5/4 (see [37]).

If \(|\cot 2\varphi| < \sqrt{\varepsilon}\), then \(\sqrt{\text{fma}(\cot 2\varphi, \cot 2\varphi, 1)} = 1\), and (4.4) in the trigonometric case simplifies to \(|\cot \varphi| = \cot 2\varphi + 1\). If \(|\cot 2\varphi| \geq \sqrt{2/\varepsilon}\), then (barring an overflow) \(\sqrt{\text{fma}(\cot 2\varphi, \cot 2\varphi, t)} = |\cot 2\varphi|\), with (4.4) and (4.6) simplifying to \(|\cot \varphi| = 2 \cdot |\cot 2\varphi|\) and \(\text{cs}_2 \varphi = 1\), respectively. These simplifications avoid taking square roots and a possible overflow of \(\cot^2 \varphi\), at a price of at most 3 floating-point comparisons. If \(|\cot 2\varphi| \leq \nu/4\), then \(t_n\) is normalized.

In (4.6) there are two mathematically (but not numerically) equivalent expressions, \(\text{cs}_1 \varphi\) and \(\text{cs}_2 \varphi\), which compute a cosine. By a similar analysis as above, \(|\cot \varphi| \geq \sqrt{2/\varepsilon}\) implies \(\text{cs}_2 \varphi = 1\), \(t_n \varphi \leq \sqrt{\varepsilon/2}\), and therefore \(\text{cs}_1 \varphi = 1\). Testing that condition also avoids an overflow of \(\cot^2 \varphi\). Motivated by the preliminary results described in Appendix B, we have chosen \(\text{cs}_2 \varphi\) formula for our implementation.

### 4.4 The postmultiplication

This phase postmultiplies \([G_p \ G_q]\) and, optionally, \([V_p' \ V_q']\) by \(V_{pq}'\) only if the rotation counter from orthogonalize is non-zero, i.e., \(V_{pq}' \neq I_{32}\). Let \(A_{pq}\) alias the first half of \(G_{pq}\) (i.e., \(R_{pq}\)). The procedure, detailed in Alg. 4.2, is based on the Cannon parallel matrix multiplication algorithm [5].

**Algorithm 4.2:** Device function for Cannon-like postmultiplication by \(V_{pq}'\).

**Description:** Input: \([A_p \ A_q], A \in \{G, V\}\). Output: \([A_p' \ A_q'] = [A_p \ A_q] V_{pq}'.

for \(i = x; i < n; i += 32\)  // multiply the next chunk of \([A_p \ A_q]\) by \(V_{pq}\)
    \(A_{pq}[x,y] = A_p[i,y]; \quad A_{pq}[x,y] = A_q[i,y];\) // load the RAM chunk into \(A_{pq}\)
    __syncthreads();  // ensure the shared memory writes have taken effect
    \(a_{xy} = a_{xy'} = 0;\)  // \([A_p' \ A_q']\) elements kept in registers
    \(j = (y + x) \mod 32; \quad j' = (y' + x) \mod 32;\) // initial skew modulo 32
unrolled for \((k = 0; k < 32; ++k)\)  // multiply-and-cyclic-shift
    \(a_{xy} = \text{fma}(A_{pq}[x,j], V_{pq}[j,y], a_{xy});\)  // update \(A_p[i,y]\)
    \(a_{xy'} = \text{fma}(A_{pq}[x,j'], V_{pq}[j',y'], a_{xy'});\)  // update \(A_q[i,y]\)
    \(j = (j + 1) \mod 32; \quad j' = (j' + 1) \mod 32;\) // cyclic shift modulo 32
endfor
    __syncthreads();  // ensure that \(A_{pq}\) is free to be overwritten
    \(A_p'[i,y] = a_{xy}; \quad A_q'[i,y] = a_{xy'};\) // store the product in the RAM chunk
endfor

Finally, Fig. 4.3 summarizes the entire pStep kernel, from a perspective of the shared memory state transitions per a thread block. The GPU RAM is accessed by one read (when no rotations occur), or by two reads and one write per element of \(G\).
(and, optionally, at most one read and write per element of $V$), with all operations fully coalesced. The only additional global memory traffic are the atomic reductions necessary for the convergence criterion in orthogonalize.

![Diagram](image)

**Fig. 4.3.** An overview of pStep kernel per a thread block, the full block variant. Each subfigure depicts a state of the shared memory, a computation subphase performed, and data transfer in or out of the GPU RAM. Subfigures (a)–(d) illustrate factorize with the Cholesky factorization, (e) and (f) belong to orthogonalize, and (g) and (h) to postmultiply phase.

4.5. A GPU-wide convergence criterion. Contrary to the pointwise Jacobi algorithm, which is considered to converge when no rotations have been performed in a sweep, stopping of the block algorithms for large inputs is more complicated than observing no rotations in a block sweep. There has to be an additional, more relaxed stopping criterion at the block level (motivated in the sequel), while keeping the one at the inner ($32 \times 32$) level unchanged.

The columns of a block pivot pair should be relatively orthogonal after completion of a pStep call, but they may have departed from orthogonality, since (see [19, 33])

1. the accumulated rotations are not perfectly ($J$-)orthogonal, and
2. the postmultiplication introduces rounding errors.

Independently from that, when subject again to factorize (and its rounding errors), even the numerically orthogonal columns may result in the shortened ones that fail the relative orthogonality criterion.

If an orthogonality failure results from the first two causes, the ensuing rotations might be justified. However, if the failure is caused only by the rounding errors of the factorization process, the spurious rotations needlessly spoil the overall convergence.

To overcome this problem, we devised a simple heuristics to avoid excessive block sweeps with just a few rotations. We expect these rotations not to be proper, i.e., to have very small angles. Let $B$ be a counter in the CPU RAM, mapped to the GPU RAM. The counter is reset at the beginning of each block sweep, and is updated from the pStep calls as described in Subsection 4.3. At the end of a block sweep, $B$ contains the total number of proper rotations in that sweep. If $B = 0$, or the maximal number...
of block sweeps has been reached without convergence, the process stops.

This heuristics may skip over a relatively small number of legitimate rotations, but nevertheless produces reasonable relative errors in the computed singular values (see Section 6). A reliable way of telling (or avoiding) the exact cause of the orthogonality failures is strongly needed in that respect.

5. A multi-GPU algorithm. In this Section we apply the same blocking principles one level up the hierarchy, to the case of multiple GPUs. As a proof-of-concept, the algorithm is developed on a 4-GPU Tesla S2050 system, and implemented as a single CPU process with 4 threads, where a thread 0, . . . , 3 controls the same-numbered GPU. Were the GPUs connected to multiple machines, on each machine the setup could be similar, with a CPU process and an adequate number of threads. Multiple processes on different machines could communicate via the CUDA-optimized MPI subsystem. Except replacing the inter-GPU communication APIs, the algorithm would stay the same.

Each of g GPUs holds a block pivot pair with a total of $n = n/g$ columns. For simplicity, we assume $n \mod g = 0$. After an outer block step, a single block-column on a GPU $i$ is sent to a GPU $j$, and replaced by the one received from a GPU $k$, where $j$ may or may not be equal to $k$, according to a block-column mapping $S^p_{2g}$ (i.e., a p-strategy $S^p_{2g}$ with communication rules). For example, in our test system with $g = 4$, a GPU $i$ communicates with a GPU $j$, $j = i \oplus 1$, faster than with the others. We maximized the amount of fast exchanges within an outer block sweep for $S^p_{8}$ (equivalent to Mantharam–Eberlein BR on a two-dimensional hypercube) to 3, by carefully choosing which block pivot pair is assigned to which GPU in each block step. The result is a block-column mapping shown in Fig. 5.1.

![Fig. 5.1](image-url) The block-column mapping in a single block sweep of a p-strategy equivalent to Mantharam–Eberlein BR to GPUs 0, . . . , 3. The fast (F) communications for column exchanges between GPU peers are denoted by dashed curves, and the slow (S) exchanges by solid lines. Two-speed communication is defined on the top left subfigure. The (logical) column swaps needed to maintain $p < q$ are shown by an asterisk.

Besides two outer block-columns of $G$ (and, optionally, $V$), stored in $G_A$ and $V_A$ regions of the GPU RAM, respectively, an additional buffer space of the same size, $G_B$ and $V_B$, has to be allocated to facilitate the BLAS 3-style matrix multiplications and
the full-duplex asynchronous communication between GPUs. Also, for the shortening and the single-GPU Jacobi phases, two \( n \times n \) matrices, \( X \) and \( Y \), are needed. With a small auxiliary space \( \text{AUX} \) for the final singular value extraction, the total memory requirements are at most \( m \times 5n \) double elements per GPU.

In an outer block step the following operations are performed (see Fig. 5.2):

1. Form the Gram matrix \( G^T_A G_A \) in \( X \) by \texttt{cublasDsyrk};
2. Factorize \( G^T_A G_A = R^T R \) by the Cholesky factorization (we chose hybrid MAGMA’s \texttt{dpotrf_gpu}, and this is the only place where a CPU is used for computation, which may be circumvented by a GPU-only implementation);
3. If accumulation of a product \( \hat{V} \) of the Jacobi rotations is desired (case (acc.)), call a full SVD single-GPU Jacobi variant (full block, block-oriented or hybrid one) from Section 4 on \( X \), storing \( \hat{V} \) in \( Y \), else
4. Copy \( R \) from \( X \) to \( Y \), call a partial SVD single-GPU Jacobi variant on \( Y \), and solve a triangular linear system \( R\hat{V} = \hat{U}\hat{\Sigma} \) for \( \hat{V} \) by \texttt{cublasDtrsm}, with the original \( R \) in \( X \) and \( \hat{V} \) overwriting \( \hat{U}\hat{\Sigma} \) in \( Y \) (case (solve));
5. Postmultiply \( G_A \) and \( V_A \) by \( \hat{V} \) in separate CUDA streams by \texttt{cublasDgemms}, storing the updated block-columns in \( G_B \) and \( V_B \);
6. Ensure that all GPUs have completed the local updates by a device-wide \texttt{cudaDeviceSynchronize}, followed by a process-wide thread synchronization (wait on a common barrier, use \texttt{MPI_Barrier} in the multi-process case);
7. Start, via CUDA streams, the asynchronous sends of one block-column from \( G_B \) and the corresponding one from \( V_B \) to another GPU, and start the asynchronous copies of the other column of \( G_B \) and the corresponding one of \( V_B \) to either the first or the second block-column of \( G_A \) and \( V_A \), according to the block-column mapping rules for transition to the subsequent block step;
8. Wait for the outstanding asynchronous operations to finish by the same synchronization procedure as in (4), after which a block step is completed.

At the end of an outer block sweep, the threads (or processes) +-reduce their local numbers \( \Sigma_B \) of proper rotations (cf. Subsection 4.5) performed in all block steps in that sweep. If the result is 0, or the limit on the number block sweeps has been reached, the iteration stops and the final singular values are extracted.

The full block variant of phases (2a) and (2b) usually has 30 sweeps limit for both the inner blocking and the pointwise, shared-memory Jacobi level. The block variant has both limits set to 1. Between them many hybrid variants may be interpolated.

Observe that phase (4) forces all GPUs to wait for the slowest one, in terms of execution of phase (2a) or (2b). The full block variant exhibits the largest differences in running times between GPUs, depending on how orthogonal the block-columns are. Although, by itself, is the fastest choice for a single-GPU algorithm (see Section 6), the full block variant may be up to 35% slower in a multi-GPU algorithm than the block-oriented one, which has a predictable, balanced running time on all GPUs.

A reasonable hybrid variant might try to keep the running times balanced. A CPU thread that first completes the full block variant of (2a) or (2b) informs immediately other threads, before proceeding to phase (4). The other threads then stop their inner block sweeps loops in (2a) or (2b) when the running iteration is finished.

The wall execution times of such an approach may be even lower than the block-oriented variant, but on the average are 10% higher. Moreover, both the full block and its hybrid variant induce larger relative errors in \( \Sigma \) than the block-oriented variant. Such effect may be partially explained, as in Section 6, by the same reasons valid for the single-GPU case (more rotations applied), but the larger differences in the
multi-GPU case require further attention. We therefore focused on the block-oriented multi-GPU variant for the numerical tests.

\[ \begin{align*} G_A & \quad V_A \quad G_B \quad V_B \quad G_{\Lambda}^T \quad G_{\Gamma}^T \\ \text{receive} & \quad \text{or} & \quad \text{send} & \quad \text{or} & \quad \text{or} & \quad \text{or} & \quad \text{or} \\ \text{one column locally} & \quad \text{or} & \quad \text{one column remotely} & \quad \text{synchronize (4, 6)} \\ \end{align*} \]

Fig. 5.2. Schematics of a GPU’s memory organization and the outer block step phases. Operations with the same number may be performed concurrently, in streams, if the hardware allows.

6. Numerical testing. In this section we define the testing data, describe the hardware, and present the speed and accuracy results for both the single-GPU and the multi-GPU implementations. By these results we also confirm our Jacobi p-strategies (\( G^4 \) and \( G^8 \)) from Section 3 as a fast and reliable choice for the Jacobi algorithms on the various parallel architectures.

Let \( \text{norm} \) and \( \text{unif} \) be double precision pseudorandom number generators, such that \( \text{norm}(\mu, \sigma) \) returns the non-zero samples from normal distribution \( N(\mu, \sigma) \), and \( \text{unif}(S) \) returns the samples from the continuous uniform distribution \( U \) over \( S \). We have generated the following pseudorandom spectra, for \( k = 1, \ldots, 16 \):

1. \( \Lambda_k^{(1)}(1:16) = 0.5; \quad \Lambda_k^{(1)}(17:1024k) = \text{norm}(0, 0.1) \),
2. \( \Lambda_k^{(2)} = 1 + \Lambda_k^{(1)} \) (verified to be greater than zero),
3. \( \Lambda_k^{(3)}(1:1024k) = \text{unif}((-10k, 10k) \setminus [-10^{-7}, 10^{-7}]) \),
4. \( \Lambda_k^{(4)}(1:1024k) = \text{unif}(10^{-7}, 10k) \).

These arrays have been casted to Fortran’s quadruple precision type, and denoted by \( \Lambda_k^{(1)} \) to \( \Lambda_k^{(4)} \). By a modified LAPACK xLAGSY routine, working in quadruple precision, a set of symmetric matrices \( A_k^{(j)} = U_k^{(j)} \Lambda_k^{(j)} [U_k^{(j)}]^T \) has been generated, for \( j = 1, \ldots, 4 \), by pre- and post-multiplying \( \Lambda_k^{(j)} \) with a product \( U_k^{(j)} \) of the random Householder reflectors. The matrices \( A_k^{(j)} \) have then been factored by the symmetric indefinite factorization with the complete pivoting [34] in quadruple precision:

\[
P_k^{(j)} A_k^{(j)} [P_k^{(j)}]^T = \tilde{G}_k^{(j)} Q_k^{(j)} [Q_k^{(j)}]^T J_k^{(j)} \hat{Q}_k^{(j)} [Q_k^{(j)}]^T \hat{G}_k^{(j)} [G_k^{(j)}]^T = G_k^{(j)} J_k^{(j)} [G_k^{(j)}]^T.
\]

The inner permutation \( Q_k^{(j)} \) brings \( J_k^{(j)} \) into \( J_k^{(j)} = \text{diag}(I, -I) \) form. For \( j \in \{2, 4\} \) the symmetric indefinite factorization is equivalent to the Cholesky factorization with diagonal pivoting and \( Q = I \). Finally, \( G_k^{(j)} \) have been rounded back to double precision, and stored as the input factors \( G_k^{(j)} \), along with \( \Lambda_k^{(j)} \) and \( J_k^{(j)} \).

Since one of the important applications of the (H)SVD is the eigensystem computation of the symmetric (in)definite matrices, the procedure just described has been designed to minimize, as much as it is computationally feasible, the effect of the
rounding errors in the factorization part. We have, therefore, measured the relative errors of the computed $\Sigma^2 J$ (from $G = U\Sigma V^T$) vs. the given $\Lambda$, i.e.,

$$\max_{i=1,\ldots,n} \left| \frac{f(\sigma_i)^2 j_i - \lambda_i}{|\lambda_i|} \right|.$$ 

The NVIDIA graphics testing hardware, with accompanying CPUs, consists of:

A. Tesla C2070 (Fermi) GPU and Intel Core i7–950 CPU (4 cores),
B. Tesla K20c (Kepler) GPU and Intel Core i7–4820K CPU (4 cores),
C. Tesla S2050 (Fermi) 4 GPUs and two Intel Xeon E5620 CPUs ($2 \times 4$ cores).

The software used is CUDA 5.5 (nvcc and cuBLAS) under 64-bit Windows and Linux, and MAGMA 1.3.0 (with sequential and parallel Intel MKL 11.1) under 64-bit Linux.

As shown in Table 6.1, the sequential Jacobi algorithm $\text{DGESVJ}$, with parallel MKL BLAS 1 operations, on machine C runs approximately 16 times slower than a single-GPU (Fermi) algorithm for the large enough inputs.

| $k$ | $\text{DGESVJ}/\mathbb{R}^\parallel$ |  $\text{DGESVJ}/\mathbb{R}^{\parallel}$ | $\text{DGESVJ}/\mathbb{R}^{\parallel}$ | $\text{DGESVJ}/\mathbb{R}^{\parallel}$ |
|-----|---------------------------------|---------------------------------|---------------------------------|---------------------------------|
| 1   | 5.57                           | 12.34                          | 14.89                          | 16.49                          |
| 2   | 8.61                           | 13.47                          | 15.45                          | 16.46                          |
| 3   | 11.75                          | 13.62                          | 15.62                          | 16.19                          |
| 4   | 11.83                          | 13.58                          | 16.14                          | 16.00                          |

In Table 6.2 the differences in the execution times of the $\mathbb{R}^{\parallel}$ p-strategy on Fermi and Kepler are given. There are three main reasons, outlined in Section 4, why the Kepler implementation is much faster than the Fermi one. In order of importance:

(i) 8-byte wide shared memory banks on Kepler vs. 4-byte wide on Fermi—the profiler reports 99.8% shared memory efficiency on Kepler vs. 49.8% on Fermi,
(ii) warp shuffle reductions, i.e., without shared memory, on Kepler, and
(iii) no register spillage on Kepler, due to the larger register file.

The other profiler metrics are also encouraging: the global memory loads and stores are more than 99% efficient, and the warp execution efficiency on Fermi is about 96.5%, which confirms that the presented algorithms are almost perfectly parallel.

| $k$ | Kepler [s] | Fermi [s] | $K/F$ [%] |
|-----|-------------|-----------|-----------|
| 1   | 1.413099    | 2.376498  | 59.5      |
| 2   | 7.260334    | 12.43532  | 57.9      |
| 3   | 22.980686   | 35.783290 | 64.2      |
| 4   | 46.357804   | 84.466500 | 54.9      |
| 5   | 95.828870   | 160.38259 | 59.8      |
| 6   | 154.643361  | 261.91793 | 59.0      |
| 7   | 246.114488  | 403.15079 | 61.0      |
| 8   | 346.689433  | 621.34177 | 55.8      |

| $k$ | Kepler [s] | Fermi [s] | $K/F$ [%] |
|-----|-------------|-----------|-----------|
| 9   | 506.36598   | 850.27953 | 59.6      |
| 10  | 682.57710   | 1153.33795| 59.2      |
| 11  | 904.21222   | 1545.45154| 58.5      |
| 12  | 1148.88198  | 1970.59157| 58.3      |
| 13  | 1439.39178  | 2500.93110| 57.6      |
| 14  | 1809.88820  | 3158.11696| 57.3      |
| 15  | 2196.75547  | 3820.55174| 57.5      |
| 16  | 2625.64259  | 4662.74870| 56.3      |
Even though the instruction and thread block execution partial orders may vary across the hardware architectures, the presented algorithms are observably deterministic. Combined with a strong IEEE floating-point standard adherence of both Fermi and Kepler, that ensures the numerical results on one architecture are bitwise identical to the results on the other. This numerical reproducibility property should likewise be preserved on any future, standards-compliant hardware.

We proceed by showing that \( R \| \) and \( C \| \) p-strategies are superior in terms of speed to \( R \| , C \| \), the Brent and Luk (\( B \)), and modified modulus (\( M \)) strategies, in both a definite and an indefinite case. By abuse of notation, we write \( R_b \| \) for the block-oriented variant (otherwise, we measure the full block variant), and \( R_{16} \| \) for the 4-GPU implementation. Fig. 6.1 depicts the wall time ratios of the other strategies vs. \( R \| \). Except \( B \) and \( C \| \), the other strategies are consistently about 14–21\% slower than \( R \| \), while \( C \| \) is almost equally fast as \( R \| \). Therefore, we further tested for speed only \( R \| \).

The standard counter-example that shows nonconvergence of the Brent and Luk strategy for matrices of even orders (first constructed by Hansen in [17], and later used in [24]), is actually not a counter-example in the usual diagonalization procedure which skips rotations with the very small angles, because there is no need for the diagonalization of an already diagonal matrix of order 2. On the contrary, the usual algorithm will diagonalize this matrix in only one (second) step of the first sweep.

However, this still does not mean that no serious issues exist regarding convergence of \( B \). Fig. 6.1 indicates that a further investigation into the causes of the extremely slow convergence (approaching 30 block sweeps) of \( B \) may be justified.

The block-oriented variant has more block sweeps and, while slightly faster for the smaller matrices, is about 7\% slower for the larger matrices than the full block variant. It may be more accurate in certain cases (see Fig. 6.2), due to considerably smaller total number of rotations performed, as shown in Table 6.3. Strategies \( M \) and \( B \) are far less accurate than the new p-strategies.

MAGMA’s \texttt{dgesvd} routine was tested with a sequential (seq.) and a parallel (par.) (4 threads) MKL library on machine A. The relative accuracy is identical in both cases. Compared with the single-GPU Fermi algorithm, MAGMA (seq.) is 1.5–3 times
Fig. 6.2. The relative accuracy of the various parallel Jacobi strategies on a single GPU. The test spectra for the left graph are $\Lambda^{(2)}_k$, and for the right graph are $\Lambda^{(1)}_k$.

Table 6.3
The number of block sweeps and the average ratios (with small variance) of the total number of rotations of the full block vs. the block-oriented variant, per 4 spectrum types on a single GPU.

| Spectrum type | 1   | 2   | 3   | 4   |
|---------------|-----|-----|-----|-----|
| average ratio of the number of rotations $\mathcal{R}_b^\parallel/\mathcal{R}_b^{b}$ | 2.29 | 2.10 | 2.30 | 2.08 |
| range of the number of block sweeps $\mathcal{R}_b^\parallel$ | 8–12 | 8–9 | 8–11 | 7–9 |
| range of the number of block sweeps $\mathcal{R}_b^{b}$ | 10–14 | 9–12 | 9–14 | 9–12 |

slower, and MAGMA (par.) is up to 2 times faster. On the other hand, MAGMA (par.) is, on average, 30%, and for the larger matrix sizes, more than 45% slower than the block-oriented 4-GPU Fermi (solve) implementation. The (acc.) implementation is about 35% slower than (solve) (see Fig. 6.3), and only marginally more accurate (see Fig. 6.4). For the matrix orders at least 4096, the fastest Jacobi implementation on 4 GPUs is about 2.7 times faster than the fastest one on 1 GPU.

MAGMA’s accuracy is comparable to a single-GPU algorithm for the well-conditioned test matrices, and better than a multi-GPU algorithm, but in the (separately tested) case of matrices with badly scaled columns ($\kappa_2 \approx 10^{12}$), the relative errors of MAGMA could be more than 20 times worse than the Jacobi ones.

Unlike MAGMA, the Jacobi GPU algorithms are perfectly scalable to an arbitrary number of GPUs, when the matrix order is a growing function of the number of assigned GPUs. That makes the Jacobi-type algorithms readily applicable on the contemporary large-scale parallel computing machinery, which needs to leverage the potential of a substantial amount of numerical accelerators.

Conclusions. In this paper we developed a set of new parallel Jacobi strategies, both faster and more accurate than the widely used ones. The new strategies may be seen as a generalization of Mantharam–Eberlein block-recursive strategy [25] to all even matrix orders. These new strategies are combined with the multi-level blocking and parallelization techniques explored in [18, 19, 33, 32, 26], to deliver the Jacobi-type (H)SVD algorithms for the graphics processing unit(s), competitive with the leading
hybrid (CPU + GPU) alternatives, like MAGMA. The new algorithms are carefully designed to use CPU primarily as a controlling unit. To this end, a collection of auxiliary shared-memory routines for concurrent formation of the Gram matrices, the Cholesky and QR factorizations, and numerically robust vector 2-norm computations are proposed. The numerical results confirm that in the massively parallel GPU case the Jacobi-type methods retain all the known advantages [13, 14], while exhibiting noteworthy speed.

Appendix A. Parallel norm computation. An essential prerequisite for computing the Householder reflectors and the Jacobi rotations [11] is obtaining the column norms (effectively, the sums of squares) reliably, avoiding possible underflows and overflows of an ordinary scalar product. However, a strictly sequential nature of LAPACK’s DLASSQ is unsuitable for parallel processing. Therefore, we propose an alternate procedure, DRDSSQ, based on the parallel reduction concept.
Let $\mu$ be the smallest and $\nu$ the largest positive normalized floating-point number, $\varepsilon$ the maximal relative roundoff error ($\varepsilon = 2^{-53}$ for double with rounding to nearest), $\gamma = 1 - \varepsilon$, $\delta = 1 + \varepsilon$, and $x$ a vector of length $n$, with no special values ($\pm \infty$, NaNs) for its components. A floating-point approximation of an exact quantity $\xi$ is denoted by $\text{rn}(\xi)$, or $\text{rz}(\xi)$, or $\text{ru}(\xi)$, for rounding to nearest, to $+\infty$, or to 0, respectively.

Find $M := \max_i |x_i|$. If $M = 0$, $x$ is a zero vector. Else, there exists the smallest non-zero $|x_i|$, which can be computed as $m := \min_i |x'_i|$, where $x'_i = x_i$ for $|x_i| > 0$, and $x'_i = \nu$ otherwise. Provided enough workspace for holding, or another technique for exchanging the partial results (such as the warp shuffle primitives of the Kepler GPU architecture), $M$ and $m$ could be found by a parallel min/max-reduction of $x$.

If the floating-point subnormals and infinity are supported, inexpensive, and safe to compute with (i.e., no exceptions are raised, or the non-stop exception handling is in effect), a sum of $x^2$ might also be computed. If the sum does not overflow, and a satisfactory accuracy is found to be maintained (e.g., the underflows could not have happened if $\text{rn}(m^2) \geq \mu$), DDRSSQ stops here.

Otherwise, note that the depth of a reduction tree for the summation of $x^2$ is $\lceil \lg n \rceil$, and at each tree level (the first one being level 0) at most $\delta$ relative error is accumulated. Inductively, it follows that if, for some $s = 2^\ell$,

$$2^{\lfloor \lg n \rfloor} (sM)^2 \delta^{(1+\lfloor \lg n \rfloor)} \leq \nu,$$

then the sum of $(sx_i)^2$ cannot overflow. Also, if $(sm)^2 \gamma \geq \mu$, for some $s = 2^k$, then no $(sx_i)^2$ can underflow. If some $j$ could be substituted for both $k$ and $\ell$, it would define a scaling factor that simultaneously protects from the potential overflows and underflows. When the range of values of $x$ does not permit a single scaling, the independent scalings of too large and too small values of $x$ should be performed.

Such a scaling of $x_i$ by $s$ in the binary floating-point arithmetic introduces no rounding errors and amounts to a fast integer addition of the exponents of $x_i$ and $s$. Instead of the scale factors themselves, only their exponents need to be stored and manipulated as machine integers. For clarity, the scales remain written herein as the integer powers of 2. A pair $(s, y)$ thus represents a number with the same precision as $y$, but with the exponent equal to a sum of the exponents of $s$ and $y$.

As motivated above, define the safe, inclusive bounds $\hat{\mu}$ (lower) and $\hat{\nu}$ (upper) for the values of $x$ for which no overflow nor underflow can happen, as

$$\hat{\mu} = \sqrt{\mu/\gamma}, \quad \delta_n = 2^{\lfloor \lg n \rfloor} \delta^{(1+\lfloor \lg n \rfloor)} \quad \hat{\nu} = \sqrt{\nu/\delta_n}.$$

Consider the following computations over a partition of the set of values of $x$:

- if $[m, M] \cap [\hat{\mu}, \hat{\nu}] \neq \emptyset$, set $s_\ell = 1 = 2^0$ (no scaling needed), and compute

$$\sigma^2 = \sum_{i=1}^n \tilde{x}_i^2, \quad \tilde{x}_i = \begin{cases} x_i, & \hat{\mu} \leq |x_i| \leq \hat{\nu}, \\ 0, & \text{otherwise}, \end{cases}$$

- if $M > \hat{\nu}$, take the largest $s$ such that $sM \leq \hat{\nu}$, denote it by $s_2$, and compute

$$\sigma^2 = \sum_{i=1}^n (s_2 \tilde{x}_i)^2, \quad \tilde{x}_i = \begin{cases} x_i, & |x_i| > \hat{\nu}, \\ 0, & \text{otherwise}, \end{cases}$$

- if $m < \hat{\mu}$, take the smallest $s$ such that $sm \geq \hat{\mu}$, denote it by $s_0$, and compute

$$\sigma^2 = \sum_{i=1}^n (s_0 \tilde{x}_i)^2, \quad \tilde{x}_i = \begin{cases} x_i, & |x_i| < \hat{\mu}, \\ 0, & \text{otherwise}. \end{cases}$$
From $m$, $M$, $\tilde{\mu}$, $\tilde{\nu}$ it is known in advance which partial sums are necessarily 0, and the procedure should be simplified accordingly. If, e.g., $m \geq \tilde{\mu}$, then $\sigma_2^2 = 0$.

A C/C++ implementation of finding $s_0 = 2^k$ or $s_2 = 2^\ell$ is remarkably simple. An expression $y = \text{frexp}(x, \&e)$ breaks $x$ into $0.5 \leq y < 1$ and $e$ such that $2^e = x$. Let $f = m$, $t = r\mu(\tilde{\mu})$, $j = k$ for $s_0$, or $f = M$, $t = r\nu(\tilde{\nu})$, $j = \ell$ for $s_2$. Also, let $f = \text{frexp}(f, \&fe)$ and $t = \text{frexp}(t, \&te)$. Then $j$ is returned by a code fragment:

$$j = (f \leq t) ? (te - fe) + (fy < ty) : (te - fe) - (fy > ty).$$

If there are more than one non-zero partial sum of squares, such $(s_{i-2}^2, \sigma_i^2)$ are expressed in a common form, $(\hat{s}_{i-2}^2, \hat{\sigma}_i^2)$, where $0.5 \leq \hat{\sigma}_i^2 < 2$, and the scales’ exponents remain even. Let $(s_{i-2}^2, \sigma_i^2) = (2^j, 2^m y)$, where $y$ is a significand of $\sigma_i^2$. Since $\sigma_i^2$ is normalized by construction, $1 \leq y < 2$. Define $m' = -(m \mod 2)$ and $j' = j + m - m'$. Then $m' \in \{-1, 0\}$, $j'$ remains even, and $(\hat{s}_{i-2}^2, \hat{\sigma}_i^2) = (2^{j'}, 2^m y)$.

The common form makes ordering the $(\hat{s}_{i-2}^2, \hat{\sigma}_i^2)$ pairs by their magnitudes equivalent to ordering them lexicographically. A summation from the smallest to the largest pair in such an order gives the final $(s^{-2}, \sigma^2)$ result. A smaller addend is rescaled to match the scale of a larger one. Let $(s_{i+2}^2, \sigma_i^2) = (\hat{s}_{i-2}^2, \hat{\sigma}_i^2) + (\bar{s}_{i-2}^2, \bar{\sigma}_i^2)$, and $(\bar{s}_{i-2}^2, \bar{\sigma}_i^2) \leq (\bar{s}_{i-2}^2, \bar{\sigma}_i^2)$. Then $s_{i+2}^2 = \hat{s}_{i-2}^2 + \bar{s}_{i-2}^2$, and $\sigma_i^2 = \bar{s}_{i-2}^2 \bar{\sigma}_i^2 + \hat{s}_{i-2}^2 \hat{\sigma}_i^2$.

If one more addition is needed, $(s_{i+2}^2, \sigma_i^2)$ has to be brought into the common form $(\hat{s}_{i-2}^2, \hat{\sigma}_i^2)$ and compared with the remaining addend. However, both $(\hat{s}_{i-2}^2, \hat{\sigma}_i^2)$ and $(\bar{s}_{i-2}^2, \bar{\sigma}_i^2)$ have to be computed only when $n \mu^2 \approx \varepsilon \nu^2$. Such large $n$ seldom occurs.

The result of DrDSSQ is $(s^{-2}, \sigma^2)$, and the norm of $x$ is $||x||_2 = \sqrt{\sigma^2} / s$. If $||x||_2$ overflows or underflows for $x$ a column of $G$, the input factor should be initially rescaled. A procedure similar to DrDSSQ is implementable wherever parallel reduction is a choice (e.g., with MPI_Allreduce operation).

**Appendix B. A choice of the rotation formulas.** In the block Jacobi algorithms, it is vital to preserve $(J)$-orthogonality of the accumulated $V^{-T}$. In the hyperbolic case, perturbation of the hyperbolic singular values also depends on the condition number of $V$ [19, Proposition 4.4]. A simple attempt would be to try to compute each rotation as $(J)$-orthogonal as possible, without sacrificing performance.

Departure from a single rotation’s $(J)$-orthogonality should be checked in a sufficiently high (e.g., 128-bit quadruple) precision, as $d_t = |(\cos^2 \varphi + \sin^2 \varphi) - 1|$, or as $d_h = |(\cosh \varphi - \sinh \varphi)(\cosh \varphi + \sinh \varphi) - 1|$, with $\sin \varphi = \cos \varphi \cdot \tan \varphi$, or $\sinh \varphi = \cosh \varphi \cdot \tanh \varphi$. For each binary exponent $-53 \leq e \leq 53$ we generated, on a CPU, $2^{24}$ uniformly distributed pseudorandom 52-bit integers $\tilde{m}_i$, to form $|c_t 2^\varphi|_i$ with the exponent $e$ and the non-implied bits of the significand equal to $\tilde{m}_i$. From $|c_t 2^\varphi|_i$ and (4.4)–(4.6) we computed $(\ln \varphi)_i$, $(\cosh_1 \varphi)_i$, and $(\cosh_2 \varphi)_i$ in double precision. In Fortran’s quadruple arithmetic the corresponding $d_t$ and $d_h$ were then found and averaged, over all tested exponents. The results are summarized in Table B.1.

**Table B.1**

|                | trigonometric rotations | hyperbolic rotations |
|----------------|------------------------|----------------------|
| $d_t$ with $\cos \varphi$ | 8.270887 · 10^{-17} | 8.335956 · 10^{-17} |
| $d_t$ with $\cos_2 \varphi$ | 7.575893 · 10^{-17} | 6.586691 · 10^{-17} |

Table B.1 indicates that $\cosh_2 \varphi$ induces, on average, more $J$-orthogonal hyperbolic rotations than $\cosh_1 \varphi$. In the trigonometric case it’s the opposite, but with a far
smaller difference. Orthogonality of the final $V$ was comparable in the tests for both trigonometric versions, often slightly better (by a fraction of the order of magnitude) using $\cos^2 \varphi$. Therefore, $\cos^2 \varphi$ formulas were chosen for a full-scale testing.

If $\text{rsqrt}(x) = 1/\sqrt{x}$ were correctly rounded in CUDA, $\cos \varphi$ could be written as

\begin{equation}
\cos' \varphi = \text{rsqrt}(\text{fma}(t \cdot \tan \varphi, \tan \varphi, 1)).
\end{equation}

With (B.1) and a correctly rounded-to-nearest $\text{rsqrt}$ prototype CUDA implementation there was a further improvement of orthogonality of $V^{(-T)}$. Although (B.1) has only one iterative operation ($\text{rsqrt}$) instead of two ($\text{rcp}$ and $\sqrt{x}$), and thus has a potential to be faster than (4.6), we omitted (B.1) from the testing due to a slowdown of about 1% that we expect to vanish with the subsequent implementations of $\text{rsqrt}$.

It is still far from conclusive which formulas from (4.6) or (B.1), and for which ranges of $\cos^2 2\varphi$, should be used. However, $\cos^2 \varphi$ or $\cos'_1 \varphi$ formulas might be an alternative to the established $\cos_1 \varphi$ ones. A deeper analysis is left for future work.

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