Non-volatile multilevel resistive switching memory cell: A transition metal oxide-based circuit

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Abstract—We study the resistive switching (RS) mechanism as way to obtain multi-level memory cell (MLC) devices. In a MLC more than one bit of information can be stored in each cell. Here we identify one of the main conceptual difficulties that prevented the implementation of RS-based MLCs. We present a method to overcome these difficulties and to implement a 6-bit MLC device with a manganite-based RS device. This is done by precisely setting the remnant resistance of the RS-device to an arbitrary value. Our MLC system demonstrates that transition metal oxide non-volatile memories may compete with the currently available MLCs.

Index Terms—Multilevel cell, Resistive switching, Non-volatile memory, ReRAM.

I. INTRODUCTION

During the last decade, the development of non-volatile electronic memories based on the resistive switching (RS) effect in transition metal oxides made a huge progress, becoming one of the promising candidates to substitute the standard technologies in a near future. RS refers to the reversible change of the resistance of a nanometer-sized media by the application of electrical pulses [1]–[6].

Though immediately after the discovery of the reversible RS effect in transition metal oxides its application for multi-level cell memories (MLC) was envisioned [7]–[11], reports so far chiefly focused on single-level cell (SLC) devices [1]. [3]. Unlike SLC, which can only store one-bit per cell, MLC memories may store multiple bits in a single cell [12]. MLCs of up to 4 bits (16 levels) are currently available based on both, standard Flash [13] and phase-change [14] technologies.

This work was partially supported by CONICET, ANPCyT, UNSAM, DuPont and Fundación Balseiro. M. J. S., M. J. R. and P. L. are members of CONICET.

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Fig. 1. Experimental Results. Random memory level sequence stored in the 6-bit MLC. The plot presents the memory states during 50 readings (at 10 Hz) for each stored value. For a 6-bit MLC, the working memory range is divided into 64 levels (as indicated in the inset).
coded in the MLC. In principle, a perfect knowledge of the function \( f \) should allow for this, but in practice the function is not known. Yet, any reasonable form of \( f \) would allow to tune any arbitrary current state by applying a sequence of pulses of decreasing intensity, following a simple “zero-finding” algorithm as in standard control circuit. Nevertheless, the requirement of a threshold current difficult the fine tuning, as small corrections beneath \( |I_{th}| \) have no effect. In practice, the dead-zone introduced by relatively large values of \( |I_{th}| \) prevents a straightforward implementation of RS-device as MLC memories with a large number of levels. Below we shall demonstrate how this conceptual problem can be overcome, and exhibit the implementation of a 64-level MLC.

**II. IMPLEMENTATION**

We adopt a manganite-based RS-device, made by depositing silver contacts on a sintered pellet of \( \text{La}_{0.325}\text{Pr}_{0.3}\text{Ca}_{0.375}\text{MnO}_3 \) (LPCMO) \([15]\). A RS-device is defined between the pulsed Ag/LPCMO and a second non-pulsed contact. A third electrode (earth) is required in a minimal 3-contact configuration setup.

A requirement for our MLC is that the RS-device operates in bipolar RS mode \([1]–[3]\), i.e., depending on the pulse polarity the remnant resistance either increases or decreases.

It is now well established that the mechanism behind bipolar RS is the redistribution of oxygen vacancies, within the nanometer-scale region of the sample in contact with the electrodes \([2]\). In the case of LPCMO, the oxygen vacancies significantly increase its resistivity because the electrical transport relies on the double-exchange mechanism mediated by the oxygen atoms \([16]\).

Pulsing an electrical current through the contact will produce a large electric field at the interface due to the high resistivity of the Ag/LPCMO Schottky barrier. If the pulse is strong enough, it will enable the migration oxygen ions across the barrier, modifying the concentration of vacancies and, hence, changing the interface resistance. The ionic migration remains always near the interface and does not penetrate deep into the bulk, since the much larger conductivity there prevents the development of high electric fields. Thus, the RS effect remains confined to a nanometer-sized region near the interface, as schematically depicted in Fig. \( \PageIndex{2} \).

We now introduce a practical implementation of an RS-based MLC that produced the results shown in Fig. \( \PageIndex{1} \). We used an Ag/LPCMO interface and off-the-shelf electronic components. The block diagram of the concept is presented in Fig. \( \PageIndex{3} \) and the schematics and technical details are included in the Appendix. We envisage an implementation of an RS-based MLC memory chip where the storage core is a set of many RS-units with a single common control circuit. The common control would set each of the individual RS-units, one at a time, thus resembling the concept of the refresh logic circuit in the DRAMs. In this work we demonstrate the implementation of the control circuit with a single RS memory unit.

Key to our MLC implementation is to adopt a discrete-time algorithm that overcomes the problems discussed above \([17]\), and which we describe next. The required memory state \( K_i \) is coded in terms of a \( V_{IN} \), while \( V_{OUT} \) indicates the actual stored value (Fig. \( \PageIndex{3} \)). The system iteratively applies pulses \( I_{pulse} \) of a strength that is an estimate of the required value to set the target state \( V_{IN} \), eventually converging to it. This discrete-time feedback loop continuously cycles between 2 stages; “probe” and “correct”. In probe stage the switch connects the RS-device to the current source \( I_0 \) in order to sense the remnant resistance. In the correct stage, the switch connects the RS-device to a pulse generator that applies a corrective pulse \( I_{pulse} \), of a strength that is obtained from the difference between the delayed \( V_{OUT} \) and the target value \( V_{IN} \) as follows,

\[
I_{\text{pulse}}[k] = K_P e[k] + K_I \sum_{i=0}^{k} e[i],
\]

where the error signal \( e[k] = V_{OUT}[k-1] - V_{IN}[k] \) is the change required in the output voltage and \( I_{\text{pulse}}[k] \) := \( I_{\text{pulse}}(k f_{\text{CLK}}) \), being \( f_{\text{CLK}} \) the frequency of the system clock and \( k \) an integer. \( K_P \) and \( K_I \) are generic proportional and integral constants respectively with \( \frac{1}{V} \) unit, being \( A \) and \( V \) the electric current and voltage units. The first term of the equation represents a proportional estimator. The second term prevents the system to get stuck in a condition where \( |I_{\text{pulse}}| < |I_{th}| \). In fact, for low \( e[k] \) a pulse of strength \( K_P e[k-1] \) would lay below the threshold, thus not producing any further change
in the state of the system. The magnitude of the second term linearly increases in time, thus making \( I_{\text{pulse}} \) to eventually overcome the threshold and correct the output voltage in the desired direction.

Notice that even if this approach resembles a standard proportional-integral (PI) control loop with dead-zone, there are substantial differences. First, the remnant resistance read-

proportional-integral (PI) control loop with dead-zone, there

overcome the threshold and correct the output voltage in the

The unit of \( u_1 \) is \( \frac{1}{\Omega} \). When a negative signal exceeds the

threshold \( I_{\text{pulse}}[k] < -I_{th} \), \( R_{rem} \) decreases as a linear function of \( I_{\text{pulse}}[k] \) with slope \( \frac{1}{\Omega} \). For a positive signal greater than \( I_{th} \), \( R_{rem} \) increases with slope \( \frac{1}{\Omega} u_1 \). For the sake of stability analysis Eq. (3) is simplified as:

\[
c[k] = V \sum_{j=-\infty}^{k} \text{NL} \left( I_{\text{pulse}}[j] \right).
\]  

In this way, the analysis is not considering any instability when sensing \( R_{rem} \) with \( I_0 \). Indeed, our actual implementation did not present any critical issue at this level (see the Appendix). From now on, unit-step sequence is considered as input signal \([18]\). The steady-state error for the system with \( K_f = 0 \) (just proportional control) and \( u_1 = 1/A^{-1} \) is \( e_s = \lim_{k \to \infty} e[k] = \frac{I_{th}}{K_P} \), then the steady-state response is \( c_s = 1 - \frac{I_{th}}{K_P} \). In fact, Fig. 5(a) shows that the system converges to the required set-point only for \( I_{th} = 0 \). The system arrives to this condition because when \( |e[k]| \leq \frac{I_{th}}{K_P} \) the excitation of the RS-device is \( |I_{th}| \leq I_{th} \), i.e. lower than the minimum voltage required to produce a change in \( R_{rem} \). A proportional control that enters into this condition, remains there indefinitely. The integral term in Eq. (2) that turns the system into a PI control, avoids the problem; when continuously integrated, \( e[k] \) makes \( I_{\text{pulse}}[k] \) to eventually overcome the threshold \( |I_{th}| \). See Fig. 5(b) and (c).

III. STABILITY ANALYSIS

A. Discrete-Time Model

The study of the system stability is based on the discrete-time model presented in Fig. 4. In the z-domain, Eq. (1) becomes

\[
I_{\text{pulse}}(z) = E(z) \left( K_P + \frac{K_f}{1 - z^{-1}} \right).
\]  

The resulting \( R_{rem} \) after these corrective pulses is probed by connecting the RS-device to the bias current source \((I_0)\), obtaining the output signal \( c[k](C(z) \text{ in } z\text{-domain}). In the next cycle, it will be compared to the reference input \( r[k+1] \) generating the error signal \( e[k+1] \). This fact implies the 1-cycle delay \( z^{-1} \).

Central to the present proposal is the following equation, a discrete-time model for the RS-device:

\[
\begin{align*}
R_{rem}[k] &= R_0 + R_1 \sum_{j=-\infty}^{k} \text{NL} \left( I_{\text{pulse}}[j] \right), \quad R_{rem}[k] - R_{rem}[k-1] = R_1 \text{NL} \left( I_{\text{pulse}}[k] \right),)
\end{align*}
\]  

where \( R_0 \) and \( R_1 \), having resistance units, are offset and a proportionality factor respectively. NL is a non-linear function that has to be defined on the basis of the general behavior of a RS-device operating in bipolar mode. In this model the \( R_{rem} \) is calculated by integrating the writing pulses after being weighted by the NL function. In this way, we model the possible change of the device resistance after the \( k \)-th pulse as \( \Delta R_{rem}[k] = R_{rem}[k] - R_{rem}[k-1] = R_1 \text{NL} \left( I_{\text{pulse}}[k] \right) \).

A concrete implementation of NL is presented below

\[
\text{NL}[k] = \begin{cases}
\left( I_{\text{pulse}}[k] + I_{th} \right) \frac{1}{A} & \text{if } I_{\text{pulse}}[k] < -I_{th} \\
0 & \text{if } -I_{th} < I_{\text{pulse}}[k] < I_{th} \\
\left( I_{\text{pulse}}[k] - I_{th} \right) u_1 & \text{if } I_{\text{pulse}}[k] > I_{th}.
\end{cases}
\]  

B. Analysis without NL

We begin by considering the simplified situation where the stability is analyzed by removing the nonlinearities introduced by \( \text{NL}[k] \) \((u_1 = 1/A^{-1} \text{ and } I_{th} = 0) \). The transfer function of the system is

\[
\frac{C(z)}{R(z)} = \frac{K_P K_f}{1+ \left( K_P + K_f \right) z^{-1} + \left( K_P - K_f \right) z^{-2}}.
\]

For \( K_f = 0.25 A^{-1} \) (typical value) the system is critically damped when \( K_P = 0.75 A^{-1} \), and remains stable for \( K_P < 1.875 A^{-1} \). Increasing \( K_I \) moves the location of the poles following \(|z| = 1\), arriving to \( z = -1 \) when \( K_I = 4 A^{-1} \), where the system becomes unstable for any \( K_P \) (see Fig. 5(m)).

C. Analysis with NL

Although the introduction of nonlinearities in Eq. (4) does not allow to study the system analytically, as in the previous section, its response might be numerically simulated. In fact, simulations where performed in the k-space by solving Eq. 5, after substituting \( I_{\text{pulse}}[k] \) (Eq. 1) and \( \text{NL}[k] \) (Eq. 4). For the computation of \( e[k] \), we assigned \( V_{OUT}[k] = e[k] \) and the unitary step function at the input (ie. \( V_{IN}[k \geq 0] = 1 V \)).

Fig. 5(d-f) shows this simulated response of the system for three sets \{\( K_P, K_I \)\} corresponding to representative position of the poles of the equivalent system without nonlinearities.

Fig. 5(g-i) shows the effect of introducing the threshold \((I_{th} \neq 0)\) for the same set \{\( K_P, K_I \)\}. The system response is qualitatively the same with the addition of periods where \( e[k] \) is “frozen” because \( |I_{\text{pulse}}[k]| \leq |I_{th}| \), while the integral term is growing. Fig. 5(j-l) shows the effect of further introducing asymmetry into the nonlinear function \( u_1 \neq 1/A^{-1} \). The effect that this nonlinearity introduces when \( u_1 < 1/A^{-1} \) is equivalent to reducing the gain of the system for \( I_{\text{pulse}}[k] > 0 \) (see Eq.
In fact, Fig. 5(j) evidences a clear difference between the system speed when \( c[k] \) is increasing as compared to the speed when \( c[k] \) is decreasing. The case for \( u_1 > 1 A^{-1} \) is equivalent to a case where \( u_1 \rightarrow u_1^{-1} \) and \( K_P \rightarrow K_P u_1^{-1} \).

Simulations also show a change in the stability limit as reported in the following table:

| \( I_{th} (A) \) | \( u_1 (\frac{1}{A}) \) | stability limit \( (K_I = 0.25) \) |
|---------------|----------------|------------------|
| 0             | 1               | \( K_P = 1.875 \) |
| 0.1           | 1               | \( K_P = 1.969 \) |
| 0.1           | 0.1             | \( K_P = 11.181 \) |

Summarizing, the simulations show that the system stability is not compromised after the introduction of nonlinearities, even if in some conditions, the system might require a considerably higher number of cycles to stabilize.

IV. RESULTS

Two tests were done to evaluate the performance of the MLC memory. Experimental results for the memory retention test are presented in Fig. 6. We emphasize that the relatively slow operation speed of our memory MLC would be dramatically improved upon device miniaturization and integration. For simplicity, we sampled a random subset of 16 out of 64 different voltages uniformly distributed along the operative range (Fig. 5(a)). Each write and read cycle had a duration of 13 seconds. In the first 5 s the WR signal was active and a memory value was SET. After a memory value was SET, we observed a small relaxation of a memory value was SET. After a memory value was SET, the WR signal was active and the memory state stored in \( V_{OUT} \) remained essentially stable afterwards. Thus, for the sake of performing a large number measurements, we only monitored the memory retentivity during the 5 time-constants (ie, 8 seconds) that immediately followed the SET. Within that period, the WR signal was inactive, and the memory state stored in \( V_{OUT} \) was probed every 0.1 s (ie, the memory was read out 80 times).

In Fig. 6(b) we present the histogram of the last read value of the memory in each cycle (ie, last value of blue sections). The horizontal bars denote the \( \Delta R \) intervals corresponding to a 16, 32 and 64 level devices. The location of the bars are chosen so to minimize the error probability (ie, area of histogram outside the interval).

The finite dispersion of the histogram is the main limitation for implementing a high number of memory levels. To easily visualize the retentivity performance of the memory for increasing number of levels, we indicate with horizontal bars the sequence of input values that is randomly chosen on the grid. During the readings indicated with blue bars, no pulses were applied to the RS-device, resulting in a drift. (b) Histogram of the last read value of the memory in each cycle (ie, last value of blue sections). The horizontal bars denote the \( \Delta R \) intervals corresponding to a 16, 32 and 64 level devices. The location of the bars are chosen so to minimize the error probability (ie, area of histogram outside the interval).

The observed values correspond to the remnant resistance of the memory cell, after reading it 80 times at a 10 Hz rate, following the SET. The histogram is constructed from a sequence of 460 memory state recordings.

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C102 and R109 introduce a time constant of \( f \) in the timing diagram. In this proof-of-concept implementation, Fig. 7. Simplified circuit of the proposed implementation with its corresponding components. It compares the output of the “sample and hold” (S&H) against the input signal divided by 2, and associated components. It demonstrates for large number of bits.

V. CONCLUSIONS
In conclusion, we have introduced a feedback algorithm to precisely set the remnant resistance of a RS-device to an arbitrary desired value within the device working range. This overcomes the conceptual problem of fine tuning a resistance value in non-volatile RS-devices for MLC applications, due to the presence of a threshold current behavior. The feedback configuration is intrinsically time-discrete, since it is based on read / write sequences. The overhead in the writing time introduced in this feedback system may be a limitation for its utilization as primary memory in a computer system, but it can easily compete with actual speed of the current mass storage devices (flash memories). The applicability of the concept to implement an n-bit MLC memory was successfully demonstrated for \( n = 4, 5 \) and 6, with an LPCMO-based circuit; which clearly illustrates the critical trade-off between BER, number of memory levels and (power and area) overhead of the control circuitry.

APPENDIX
SCHEMATICS AND TECHNICAL DETAILS OF THE CIRCUIT
Fig. 7 shows a simplified circuit of our implementation. The “estimator” circuit (see Fig. 6 and Fig. 4) is implemented by IC100D, IC101A and the high-current buffer A3 (and associated components). It compares the output of the “sample and hold” (S&H) against the input signal divided by 2, and then computes the PI function. \( K_P \) and \( K_I \) are set by means of P101 and P100 respectively.

During the “correct” state, corrective pulses are applied to the RS-devices (LPCMO), by closing S1 during \( f_{WR} = 120 \)\( \mu \)s. C102 and R109 introduce a time constant of \( \approx 13 \mu \)s, reducing the rise time of the pulses in order to avoid overshoots. In the “probe” state, IC103B closes first and \( t_{RD} = 0.25 \)ms after, IC103A. Also, S4 clamps the inverting input of A3 to \( V+ \). The timing of the circuit is generated by a timing circuit based on the master clock CLCK (see Fig. 7). A current \( I_0 \approx 1 \)mA flows though the LPCMO (\( V+ = 7.5 \)V, \( V- = -7.5 \)V). The voltage drop at the switching interface of the RS-device (ranging 20-50 mV) is amplified by the instrumentation amplifier A1 (gain=21), eventually setting the voltage at the output of the S&H. Both interfaces of the RS-device behave complementary (i.e., when one interface reduces its resistance, the other increases), then the total drop across the device is \( \approx 70 \) mV and quite insensitive to the state, and therefore, \( I_0 \).

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