Exploring the Impact of Affine Loop Transformations in Qubit Allocation

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Abstract
Most quantum compiler transformations and qubit allocation techniques to date are either peep-hole focused or rely on sliding windows that depend on a number of external parameters. Thus, global optimization criteria are still lacking. In this paper we explore the synergies and impact of affine loop transformations in the context of qubit allocation and mapping. We conduct an extensive evaluation spanning 8 quantum circuits taken from the literature, 3 distinct coupling graphs, 4 affine transformations (including the Pluto dependence distance minimization and Feautrier’s minimum latency algorithms), and 4 qubit allocators. Our results demonstrate that affine transformations using global optimization criteria can cooperate effectively in several scenarios with quantum qubit mapping algorithms to reduce the circuit depth, size and allocation time.

Keywords: affine compilation, polyhedral model, quantum computing, qubit allocation

1 Introduction
The field of Quantum Computing (QC) has made tremendous advances in the last two decades at the hardware (e.g. ion trap and superconducting QC), algorithmic (QFT [7, 18, 19, 34], Grover’s Search [14, 33, 43], Shor’s algorithm [10, 45, 51, 60, 61], and software levels [21, 52, 58]). Known quantum algorithms already provide us with a glimpse of their expected exceptional complexity. Thus, it is imperative for a programming language to be a vehicle for algorithmic specification rather than an obstacle in the path to progress. To address and bridge the semantic gap between algorithm specification and quantum architectures, several languages, compilers and frameworks have been proposed. Examples of these are ProjectQ [67], Scaffold and the ScaffCC compiler [40], Quipper [30], Microsoft’s Q# DSL [68] and SIMD approaches such as [36], or approaches focused on safe uncomputation such as SILQ [11].

Ultimately, the high-level programming language produces a stream of quantum assembly operations [12, 21], at which point Qubit Allocation, a technique akin to classic register allocation [15, 56], is applied to find a space-time mapping of the quantum gate operations in the program to the quantum device. Qubit allocation techniques typically decompose the input program into (network) layers, and generally suffer from limitations such as approximating the global solution from local optima [37], use relative small sliding windows [48], leverage random initial mappings [37, 62], or incur in high time and space complexity due to exponentially large search spaces [35, 81].

The main goal of this work is to explore and understand potential synergistic interactions between affine loop transformations and qubit allocation techniques in order to find scenarios where the power of a global optimization criteria can effectively improve the quality of the qubit allocation. Our evaluation shows that even state-of-the-art allocators such as sabre [48] can improve by as much as 34% with classical polyhedral loop transformations, while other techniques less computationally demanding (i.e. wpm [62]) can improve by up to 60%.

In summary, this paper makes the following contributions: i) We conduct an extensive study to understand the interactions of affine loop transformations with qubit allocation techniques. Our evaluation encompasses 8 quantum circuits, 4 allocators, 3 topologies and 3 affine transformations in addition to the pass through code generation mode. ii) Inspired in the Omega calculator [41] and ISCC’s [76] notation, we introduce a simple domain specific language based on polyhedral abstractions to enable the description, manipulation and composition of quantum circuits. iii) We discuss how the polyhedral model can be used as an efficient intermediate representation for the optimization of affine quantum circuits. In particular, we highlight how we can use it to represent quantum networks.

The rest of this paper is organized as follows. Sec.2 recaps the necessary quantum terminology and background. In particular, we briefly recap several quantum allocators recently introduced, and which we use in our evaluation. Sec.3 revises the polyhedral background while introducing a simple domain-specific language for affine quantum circuits. Sec.4 discusses our extensive evaluation, general results, individual analyses and scalability tests. We conclude this paper with the related work (Sec.5) and the final remarks in Sec.6.

1sabre’s average improvement over jku for large circuits is 14%, reported in [48]
2 Background in Quantum Computing

Qubits Quantum bits are the basic unit of information of quantum programs, and are the analogs of classical bits. However, unlike their classical counterpart, which can only take the values in the set \{0,1\}, qubit values take the form of linear combinations of two basis states (\{0\} and \{1\}).

Gates and Measurement Are the elementary operations applied to qubits. Their role is to evolve the state of qubits. More generally, quantum gates can be seen as unitary matrix operations applied to vectors representing quantum states. Current quantum technologies utilize gate operations with 1 and up to 3 qubits. An example of a single qubit operation is the NOT (X) gate, which negates the state of a single qubit. An example of a two-qubit gate is the CNOT (Controlled-NOT or CX) operation, which reverses the state of the second qubit operand when the first one is 1. An example of a 3-qubit gate is the CCNOT (Controlled-Controlled-NOT), which utilizes two control and one target qubits. In terms of classical computing the control-qubits are read-only while the target qubit is effectively updated. Quantum gates are akin to assembly code in classical computing.

Coupling Graphs A quantum processor can be conceptually conceived as a graph/network where the vertices are the qubits, and the edges the communication links between them. Computational steps (gates) performed in the network are synchronized in time. Qubits serve as inputs and outputs to each quantum operation. A current limitation of quantum computing technology, is that multi-qubit gates can only be applied to qubits directly connected by a link [44, 80].

Quantum Circuits Quantum programs can be graphically represented in the form of circuits [71]. We show an example of a simple circuit obtained from the Revlib online repository [59] in Fig.1. The x-axis signifies time, while the y-axis are the qubits available in the quantum processor. It uses 6 qubits, 5 NOT gates (left-most), and 5 CNOT gates. Each NOT gate is synchronized with the control qubit of a CNOT gate. Operations on the same qubit lane, from left-to-right execute one-after another, and embody classic data-flow input/output dependences.

![Figure 1. parity_247 circuit](59)

The actual semantics of the specific gate determine if the state of a qubit \(q_i\) is read, written, or both. The depth of a quantum circuit is the maximum number of gates scheduled on any single qubit lane, whereas the total number of gates is the circuit size. The quantum circuit ultimately defines the unitary evolution of the input (initial) state into the final/output state.

Qubit Allocation Is the space-time mapping (assignment) of quantum operations to qubits in the coupling graph, and is very similar in spirit to the classical register allocation problem. Recently several qubit allocators have been proposed. We briefly summarize a few of the most relevant techniques. The ibm-mapper [37] (available in Qiskit) divides the input into a sequence of layers using disjoint sets of qubits; qubits within layers are mapped by minimizing the sum of squared distances among vertices, and potentially inserting SWAP operations. In addition, each distance term is scaled by a factor \(1 + r\), where \(r\) is a random number between 0 and 1. The algorithm defaults to one gate per layer if a valid mapping is not found. wpm [62] is a heuristic that finds first an initial allocation maximizing the number of control dependences, followed by a second pass which completes any remaining ordering constraint, potentially inserting SWAP operations. Sirachi et al. [62] also proposed an exact solution to the qubit allocation problem as a dynamic program with state memoization, and showing that it leads to a \(O(|Q|!)\) \cdot |Q| \cdot |D|\), where \(Q\) is the set of (physical) qubits, and \(D\) the list of dependences. The heuristic proposed (wpm) was shown to achieve \(O(|Q| \cdot lg(|Q|)) + \sum |E| + |D| + |D| \cdot (|Q| + |E|)). jku [81] uses the circuit size as the main optimizing metric, decomposing the input network into layers, and attempting to minimize the number of gates within each layer. To avoid falling into local optima, jku uses an A* search algorithm [35], a family of graph traversal algorithms known to incur in \(O(b^d)\) space complexity, where \(b\) is the branching factor in a tree and \(d\) its depth. The heuristic used to drive the search attempts to convert the mapping of each layer into the subsequent one by inserting SWAP operations. sabre [48] is an efficient algorithm with \(O(N^{2.5}g)\) time complexity that attempts to minimize both the circuit depth and size, usually exploring a trade-off between them. As previous techniques, it divides the input program into layers, but performs two additional passes (a back-traversal and a second forward traversal) to improve the initial (random) mapping.

(De)Coherence One of the main challenges facing QC is the decoherence problem, where the state of a qubit decays over time. Each quantum gate has a specific decoherence time, which for state-of-the-art quantum machines using superconducting technology is approx. 100 \(\mu\)s [58]. In addition, gate operations can also introduce errors at rates varying between \(O(10^{-3})\) for single-qubit gates and \(O(10^{-2})\) for two-qubit gates. The execution time of a quantum circuit results from the aggregated time needed to run all the gates along the circuit’s depth. Thus, minimizing this metric is one of the main optimizing criteria. Likewise, minimizing the total number of operations in circuits also equates to reducing the compounded error.

3 The Polyhedral Model in Quantum Computing

In this section we quickly revise the 4 polyhedral abstractions in the context of (affine) quantum circuits. We then
describe a simple domain-specific language heavily inspired in the Omega Calculator [41] and ISCC [76] notation. However, unlike its predecessors, one of its main goals is to facilitate and capture the identity schedule of the quantum circuit. We explain how the circuit structure and dependences are mapped to the polyhedral abstractions, and quickly recap well-known affine loop transformations previously proposed.

3.1 Polyhedral Abstractions

Polyhedral compilers focus on fragments of programs that exhibit static control parts (SCoPs)[24–26]. From these, four abstractions are extracted: iteration domains, access functions, dependence polyhedra and scattering/scheduling functions [31].

Iteration Domains: Each syntactic statement S is associated to the set of points $D^S$ in $\mathbb{Z}^+$ comprised by the dynamic instances of the statement. In the context of QC, an iteration domain can group several operations of the same type or of different ones, but that behave in the same fashion. Consider for instance the parity_247 circuit shown in Fig.1, which can be represented with two iteration domains, $D^{S1} = \{[i] : 0 \leq i < N\}$ and $D^{S2} = \{[i] : 0 \leq i < N\}$, one for the NOT operations, and another for the CNOTs; where $N$ is an unknown but fixed value that parameterizes the circuit. We also note that several techniques have been developed to model and extend the applicability of the polyhedral model to different forms of irregular computations [6, 72, 73]. The remaining three abstractions are essentially functions applied to the iteration domains.

Program schedules: The execution order of statement instances is defined in the polyhedral model with the program schedule, a transformation matrix or an affine map that assigns to each statement instance an execution date. Schedules can be seen as multi-dimensional time-stamps $\Theta^S(\vec{x}) = \langle \theta^S_1, \theta^S_2, \ldots, \theta^S_d \rangle$, $\vec{x} \in D^S$, where $\theta^S_i$ is a one-dimensional affine function, and $d$ is the number of dimensions in $\Theta^S$. Schedules can be lexicographically compared, and are used in the polyhedral scanning process [9] to generate the loop structure that will visit each statement instance in the order established by the schedule $\Theta^S$. Continuing with our ongoing example, the execution order of parity_247 circuit can be represented with the schedules $\Theta^{S1}(i) = (0, i)$, $\Theta^{S2}(i) = (1, i)$. We note, however, that for this circuit loop fusion can be legally applied. In this case, another potential schedule could be $\Theta^{S1}(i) = (0, i, 0)$, $\Theta^{S2}(i) = (0, i, 1)$.

Access Relations: Are an abstraction that permit to model memory accesses. Access relations map points in an iteration domain to a data-space. The motivation is two-fold. First, to later be able to identify program statements accessing the same memory location. Second, to update the array subscript functions post-transformation. The construction of access relations in quantum computing differs in two fundamental ways from its classical counterpart. First, in classical computing the usage of multi-dimensional arrays is the norm, whereas the current practice in quantum computing is to operate on a single, large, one-dimensional array that represents a quantum register. The second difference involves what constitutes a read and write access. In effect, in classical computing, where polyhedral compilation has been predominantly applied to imperative programming languages such as C/C++ and Fortran, there is, practically always, a single write reference and zero or more read references. This is not the case in quantum computing, where the program’s state evolves as specific entries of the registers are input to gate operations. Moreover, the type of gate determines if a specific register entry is read or updated. We make this distinction for two reasons: First, some gates take control argument, which do not modify the contents of a register entry. Second, every gate operation performing a write also reads the input register entry, i.e. the same entry is both read and written. Resuming our example, if we assume that the top qubit has index 0, increasing downwards, then statement S2 would have three access relations, a read and write relation $\{[i] \rightarrow [0]\}$ for the target qubit, and a read-only relation $\{[i] \rightarrow [i + 1]\}$ for the control qubit.

Dependence Polyhedra embody the semantic orderings of the program. Every program dependence in a SCoP is represented by one or more dependence polyhedra $D^{R \rightarrow S}$. These polyhedra define the ordering among points $\vec{r}^R$ and $\vec{g}^S$ from the iteration domains $D^R$ and $D^S$, respectively. This critical pass is necessary to perform aggressive loop optimizations, and compute reordering transformations via one or more integer linear problems (ILPs), which must preserve the legality of the transformations applied. Essentially every scheduling technique [3, 20, 23, 28, 70] embeds the program semantic constraints in the form of dependence polyhedra (possibly linearized by the application of the Farkas Lemma) into one or more ILP systems. These polyhedra are usually extracted with “classical” data-flow dependence analysis [24].

(Paramaterized) Affine Quantum Circuits (PAQCs)

We define PAQCs as a subclass of quantum programs that can be expressed with affine relations, or a union of them. We have two requirements: First, the instances of gate operations to be groupable by an affine expression; Second, the indices of qubits being accessed to be representable via affine functions.

3.2 AXL: A simple Domain-Specific Language for Parameterized Affine Quantum Circuits

Enter AXL, a declarative language with operations that enable the specification, manipulation and composition of quantum circuits. AXL’s syntax is simple and straightforward. AXL provides 4 datatypes: gate, circ (constant circuits), statement circuits (our link to the polyhedral abstractions) and
### Table 1. Quantum Gates

| Gate         | Description              | No.Inputs | No.Outputs | Integer Map Representation                                      |
|--------------|--------------------------|-----------|------------|-----------------------------------------------------------------|
| X(r_{w0})    | Pauli-X (NOT) gate       | 1         | 1          | S[x] → q[|r_{w0}(x)|]                                         |
| Y(r_{w0})    | Pauli-Y gate             | 1         | 1          | S[x] → q[|r_{w0}(x)|]                                         |
| Z(r_{w0})    | Pauli-Z gate             | 1         | 1          | S[x] → q[|r_{w0}(x)|]                                         |
| H(r_{w0})    | Hadamard (H) gate        | 1         | 1          | S[x] → q[|r_{w0}(x)|]                                         |
| Measure(r_{w1}, r_{w2}) | Measure qubit to classical bit | 1 | 2 | S[x] → q[r_{w1}(x)]; S[x] → c[w_{2}(x)] |
| CNOT(r_{1}, r_{w2})   | Controlled-NOT (CX)     | 2         | 1          | S[x] → q[r_{1}(x)]; S[x] → q[r_{w2}(x)]                       |
| CXY(r_{1}, r_{w2})   | Controlled-Y            | 2         | 1          | S[x] → q[r_{1}(x)]; S[x] → q[r_{w2}(x)]                       |
| CZ(r_{1}, r_{w2})     | Controlled-Z            | 2         | 1          | S[x] → q[r_{1}(x)]; S[x] → q[r_{w2}(x)]                       |
| Swap(r_{w0}, r_{w1})  | Exchange state           | 2         | 2          | S[x] → q[r_{w0}(x)]; S[x] → q[r_{w2}(x)]                       |
| Toffoli(r_{x}, r_{z}, r_{w}) | Controlled-Controlled-Not | 2 | 1 | S[x] → q[r_{x}(x)]; S[x] → q[r_{z}(x)]; S[x] → q[r_{w3}(x)] |

Parameterized Affine Quantum Circuits (PAQC) A unique capability of AXL is to represent affine quantum circuits in a parameterized fashion, that is, circuits can be modeled with symbolic values representing arbitrary, unknown, constant values. PAQCs are built by defining an iteration domain for the circuit and by attaching a circuit body to it. The circuit body can be: i) a basic gate; ii) a fixed, possibly composite expression of type $circ$; or iii) a parameterized, variable expression. The last of these body types, leverages the full power of the polyhedral model to represent individual instances of the computation. PAQCs are implemented in AXL via the statement type, making parameterized and variable sized quantum circuits first class citizens in our language.

We show in Table 1 a subset of the gates supported by AXL. The arguments to each gate represent indices in an implicit one-dimensional space; depending on the type of the gate, some arguments are either read-only (i.e. any $r_{i}$ argument), read-write (arguments $r_{w}$) or write-only (arguments $w_{i}$). These semantics allow us to determine the number of input and output relations, which we show in the third and fourth columns. The last column shows the extracted access relations for each of the accessed register entries, modeled as a single affine relation mapping points of the iteration domain to the data-space of the quantum register (register $q$) or of the classical register (register $c$). We follow the same naming convention to indicate when an access function is of type read, read-write or write. We note here that, although we list the main quantum gate operations, these can be quickly added into the AXL language under the category defined by the number of qubits, and the access type to each of its arguments.

#### Gate Call Relations

In classical (scientific) computing, where multi-dimensional arrays are pervasive in imperative programming languages, each array reference is either read or written. This naturally follows the semantics of languages with explicit assignment operations; only the reference on the left-hand-side is written, while any array or scalar variable on the right-hand-side is read-only (except when passed to some function with side-effects). In our DSL, quantum programs operate in an implicit 1-dimensional data-space.
While there is no inherent limitation in AXL to represent registers in a multi-dimensional space, most quantum technologies have assumed this so far. Thus, we add a new abstraction representing quantum gate calls. These are very similar in spirit to classical access relations that map points in iteration domains to the various data spaces of the program. While quantum gates are effectively functions that could change the state of a register, they do come equipped with domain semantics that must be correctly mapped. More precisely, each quantum gate operation has a set of read and write index sets that establish the register entries accessed in each of these modes. Later, during the polyhedral scanning process (phase-1 of code generation) these relations are used to produce the exact quantum gate operation specified by the end-user.

**Program Assembly** We define Program Assembly as the process of constructing the final circuit schedule establishing the complete ordering among statement circuit instances in a single SCoP. It takes place at the start of the transformation and code generation process (see codegen clause in Fig 2). Building the final schedule happens in two phases. First, when defining circuit statements, a local identity schedule is created. For instance, in the same example, the local schedule \( \Theta = (i) \) is created for statements S1-S3 (Lines 3-5 in the same figure). AXL will then split S1 into sub-statements S11 and S12, effectively making each gate its own statement. The usage of the (+) operator for S1 will introduce a suffix scalar dimension, producing the schedules \( \Theta^{S11} = (i, 0) \) and \( \Theta^{S12} = (i, 1) \). The second phase of program assembly synchronizes statement circuits in a similar fashion, but with the distinction of inserting scalar dimensions as prefixes. For example, the local schedules of S2 and S3 will be modified to \( \Theta^{S2} = (0, i) \) and \( \Theta^{S3} = (1, i) \). Along the process, multiple scalar dimensions might be added to faithfully represent the ordering among various circuit patterns, which can be controlled by proper parenthesization.

### 3.3 Transformations

We next recap two well known formulations that have been extensively used at the heart of several scheduling algorithms, the Feautrier minimum latency schedules [25, 26], and the minimization of the maximal dependence distance used in the Pluto compiler [13]. In particular, Pluto has been extremely successfully in generalizing the tileability of imperfectly nested loops and using the aforementioned cost function to produce high-quality transformations. Similarly, the Feautrier algorithm has been used in [42] and is still the fallback scheduling strategy in ISL [75].

**The Pluto Algorithm** The Pluto Tiling Hyper-plane algorithm [13], was introduced as a general greedy algorithm to find affine transformations to make a program tileable. At its core, it uses a cost function that bounds and minimizes the distance among statements in dependence relations. As

```
1  // Plutomin (min.fusion) heuristic:
2  // Loop fission
3  for (int c1 = 1; c1 <= 8; c1 += 1) {
4    X[c1];
5  }
6  for (int c1 = 1; c1 <= 8; c1 += 1) {
7    CX[c1][0];
8  }
9  // **********************************
10  // Plutomax (max.fusion) heuristic:
11  // Loop fusion
12  for (int c0 = 1; c0 <= 8; c0 += 1) {
13    X[c0];
14    CX[c0][0];
15  }
```

**Figure 3.** Generated loop structure for circuit parity_247 using Pluto’s Minfuse and Maxfuse loop fusion heuristics

we don’t apply loop tiling to quantum programs, we only recap Pluto’s main cost function formulation below:

\[
\begin{align*}
\delta_e(\bar{x}) &= \phi_S(\bar{x}) - \phi_S(h_e(\bar{x})), \quad \bar{x} \in P_e \\
\phi_S(\bar{x}) - \phi_S(h_e(\bar{x})) &\leq v(\bar{p}), \quad \bar{x} \in P_e, \forall e \in E \\
v(\bar{p}) &= u.\bar{p} + w \\
v(\bar{p}) - \delta_e(\bar{x}) &\geq 0, \quad \bar{x} \in P_e, \forall e \in E \\
\end{align*}
\]

The above equations essentially perform the following: i) define the constraints to satisfy a dependence edge \( e \) of the dependence set \( E \), for every point \( \bar{x} \) in the dependence polyhedron \( P_e \); ii) introduce an affine function \( v \) on the vector of program parameters, \( \bar{p} \); iii) bound the distance between the target and source of the dependence via a function \( v(\bar{p}) \); iv) minimize the \( u \) coefficients that bound the dependence distance (NOTE: we omit here the application of the Farkas Lemma).

The rest of Pluto’s algorithm proceeds level-by-level, from the outermost to the innermost, finding one-dimensional affine transforms for all statements in the program. By default, splitters (scalar dimensions) are only introduced by the algorithm when no solutions are found for a new hyperplane. However, doing this whenever is legal, produces loop structures maximally distributed. We show in Fig 3 the result of applying both heuristics, labelled as Plutomin and Plutomax; to the AXL implementation of the parity_247 circuit.

**The Feautrier Scheduling Algorithm** Feautrier’s seminal papers [25, 26] on one-dimensional and multi-dimensional affine schedules have been a common test for several applications and domains. The main property of Feautrier’s
Table 2. Geometric Mean Circuit Depth and Added Gates across topologies, loop transformations and qubit allocators

| Topology x Transformation | Circuit Depth (No.Gates) | No. of Added Gates |
|---------------------------|--------------------------|--------------------|
|                           | jku          | ibm     | sabre    | wpm    | jku      | ibm      | sabre    | wpm    |
| multi-ring x base         | 204.79       | 314.63  | 208.17   | 358.02  | 317.25   | 568.47   | 290.30   | 723.47  |
| multi-ring x feautrier     | 211.31       | 311.54  | 203.04   | 358.47  | 327.48   | 556.27   | 275.04   | 747.09  |
| multi-ring x plutomin      | 203.85       | 312.80  | 204.96   | 367.19  | 316.87   | 562.75   | 269.52   | 769.92  |
| multi-ring x plutomax      | 206.43       | 309.15  | 205.16   | 356.87  | 321.21   | 550.15   | 284.55   | 735.11  |
| grid x base               | 162.31       | 228.26  | 169.33   | 307.15  | 225.17   | 419.21   | 203.31   | 584.08  |
| grid x feautrier           | 167.22       | 225.93  | 169.20   | 302.71  | 225.12   | 425.11   | 208.55   | 626.09  |
| grid x plutomin            | 161.93       | 228.69  | 165.52   | 308.05  | 224.40   | 415.32   | 223.36   | 590.60  |
| grid x plutomax            | 161.61       | 228.71  | 170.60   | 298.12  | 224.40   | 415.32   | 223.36   | 590.60  |
| tiled x base               | 191.55       | 250.30  | 198.37   | 319.59  | 336.20   | 469.53   | 298.63   | 570.72  |
| tiled x feautrier          | 196.23       | 254.10  | 192.31   | 321.07  | 344.30   | 473.35   | 294.37   | 385.64  |
| tiled x plutomin           | 190.22       | 249.75  | 188.44   | 315.98  | 330.93   | 473.35   | 286.59   | 382.62  |
| tiled x plutomax           | 195.73       | 246.92  | 194.65   | 329.98  | 333.47   | 461.80   | 287.61   | 379.69  |

scheduling approach is to greedily satisfy as many dependences as early as possible, going from the outermost (linear) dimension to the innermost. This greedy approach produces schedules with the minimum number of dimensions. More importantly, this approach yields the maximum freedom to reorder operations in the innermost loop dimensions.

4 Experimental Evaluation

We have implemented the AXL language, and the analyses and transformations described in Section 3 as a source-to-source compiler toolchain using the Integer Set Library [75]. Quantum circuits are written and compiled with AXL to produce the loop structure, which is then post-processed to construct a compilable C-program. This is then compiled into an executable binary to finally generate the stream of quantum assembly operations, targeting either the ProjectQ [67] compiler or OpenQASM 2.0 [21]. In particular, the results shown here are obtained with QASM files. The AXL benchmarks were compiled on an 8-core AMD Ryzen 7 2700X - 2.1GHz with 105GB DRAM, 32KB L1, 512KB L2 and 8MB L3 cache.

The overall goal of our experimental evaluation is to demonstrate that even “classical” high-level loop transformations, i.e. not yet tailored to the quantum computing domain, can synergistically work with back-end compiler optimization such as Qubit Allocation. Thus, our goal is to determine where (in which experimental configurations), why (interactions of loop transformations with the qubit allocator) and when (in some specific stage of a circuit) can impact the qubit allocation result, either for good (improved quality, i.e. shallower circuits) or bad (bigger circuits).

**Testbed and Protocol:** We use the Enfield compiler [1, 2], which implements several qubit allocation techniques. In particular, we consider four of the qubit allocation algorithms covered in Sec.2: sabre [48], jku [81], wpm [62], and ibm [37]. Enfield allows to collect statistics such as allocation time, circuit depth (no. of gates in critical path), circuit size (total no. of gates) among many others. The methodology we follow is the same as that of sabre [48] when comparing against jku, while wpm and jku compare against the ibm mapper in their respective publications. As context, the jku paper reported a 23% improvement (no. of elementary gates added) w.r.t. to ibm, while sabre reports an average improvement of 14% over jku, considering their qft and large benchmark categories.

We use the circuit depth and size as primary quality metrics, which vary with the allocator due to the number of quantum SWAP and REVERSE operations introduced to advance the program state, usually between adjacent layers. Each of these operations is implemented with elementary gates. Each SWAP is implemented with 3 CNOT, while each reverse operation requires 4 Hadamard (H) and 1 CNOT gates.

Our experimental testbed consists of the eight quantum circuits listen in Table 3, which were taken from the literature \(^2\). We generate four different variants for each benchmark: pass-through mode performing only code generation (base); the transformed code obtained by applying the Feautrier scheduling algorithm (feautrier) [25, 26]; and the two well known Pluto’s fusion heuristics, maximal loop fusion (plutomax) and maximal loop distribution (plutomin). We note that the base variant, while only involving code generation, can already be considered an optimized program, as the polyhedral scanning process will produce minimal control overhead that can vastly differ from hand-written loop-based code [9]. The latter two variants represent ends of the classical locality spectrum. Although Enfield already repeats the allocation process 10 times and report their arithmetic mean. We also include error bars showing the standard deviation.

\(^2\) Please refer to the Appendix for a larger AXL example and circuit diagrams.
Table 3. Quantum Circuits Evaluated with Default Parameters

| Benchmark Name   | Source | No. Statements | No. Polyhedral Dependencies | Parameters | No. Qubits | No. QASM ops | Output Lines |
|------------------|--------|----------------|-----------------------------|------------|------------|-------------|--------------|
| adder-maj-uma    | [22]   | 3              | 11                          | N=9        | 20         | 55          | 13-15        |
| cuccaro-adder-6bit | [22]  | 6              | 50                          | N=6        | 14         | 46          | 26-36        |
| sum5             | [69]   | 7              | 41                          | N=5        | 11         | 36          | 22-32        |
| init-G5          | [69]   | 8              | 33                          | N=5        | 11         | 35          | 24-34        |
| cheung           | [17]   | 1              | 3                           | N=6        | 18         | 21          | 5            |
| pipelined-swap   | [27]   | 13             | 28                          | N=6        | 14         | 75          | 37-43        |
| cnt3-5_179       | [79]   | 2              | 14                          | N=5        | 19         | 30          | 14-20        |
| rd84_142         | [79]   | 3              | 36                          | M=2, N=4   | 15         | 28          | 16-32        |

Evaluated Topologies: Just as in classical computing the underlying architecture (e.g. multi-core CPU, many-core CPU, GPUs, etc) can have a substantial impact on the program’s performance, in quantum computing the quality of the resulting qubit allocation can depend of the underlying architecture (topology). We thus evaluate three coupling graphs with the same number of qubits (36), and slightly vary the graph’s connectivity to produce different properties. The three coupling graphs used are shown in Fig.4, and include a 6x6 grid (grid), a graph with three doubly-linked concentric rings (multi-ring), and a four 3x3 tiled array of qubits (tiled). All graphs have the same diameter (10), but differ in their bisection bandwidth, which is 6 for multi-ring and grid, and only 2 for tiled. In addition, having more qubits with higher degree enhances the architectural parallelism. For instance, if a given qubit has degree d, then completing an update (write) on this qubit can enable up to d – 1 gate-to-gate dependencies. For multi-ring, tiled and grid the number of gates with degree 3 or greater are 8, 24 and 32, respectively. This design decision differs from the IBM QX20 (Tokyo) coupling graph, which varies over time, and which typically has several qubits with degree 5 or 6.

Figure 4. Evaluated coupling graphs (topologies)

TL;DR: Overall, we observe that quantum qubit allocation algorithms and quantum programs can benefit from the power of global cost functions offered by polyhedral optimization techniques. Our evaluation shows that even the most advanced allocators (jku and sabre) can improve up to 34%, while achieving 60% on wpm. We also observe and confirm general trends such as allocation variability due to the inherent data- and pipelined- parallelism, distance among qubit operands, or the hardware parallelism available.

General Trends We summarize in Tab.2 the geometric mean of the circuit depth (no.gates) and number of added gates across all combinations of topologies, affine transformations and qubit allocators. The first trend to observe is that the depth of the circuit tends to increase with with lower architectural parallelism (e.g. no. of qubits with degree 3 or greater), as expected. Next, we observe than even the state-of-the-art allocators, jku and sabre, can greatly benefit from affine transformations. In particular, we observe up to a 10% gap of added gates (max Δtransform/max(added)) due to loop transformations in the [grid,jku], [grid,sabre] and [tiled,sabre] configurations. In regard to jku, this qubit allocator produces the shortest circuits (depth-wise) in all three topologies when used in combination with plutomin, and producing its worst circuit depth when combining it with feautrier. This trend is nearly the same for sabre. Lastly, we don’t observe any obvious trend involving the ibm allocator.

In regard to the number of gates added by each allocator (last 4 columns), we observe that this metric also correlates with the architectural parallelism of the topologies used. We also observe that an overall increase of gate count does not necessarily correlate with better circuit depth. This phenomenon can be seen when comparing the [grid,jku] and [grid, sabre] with {multi-ring,jku} and {multi-ring, sabre}.

Individual Analysis with Default Parameters We next dissect the behavior of our eight quantum circuits, and show the achieved circuit depth in Fig.5. For each circuit, we cluster the results by topology × allocator. Each bar represents the mean of 10 repetitions, and include their corresponding standard deviation. In addition, each cluster is also tagged with the highest percentual variation between the highest and lowest depth ((depthmax − depthmin)/depthmax) among the loop transformation for the same topology and allocator. In general, we expect lower variation for the grid topology than for the multi-ring and tiled topologies.

Turning our attention to the pipelined-swap circuit. This benchmark represents the swap between two distant qubits
Appendix for circuit diagram). Each CNOT operation being added to the operations on two adjacent qubits. The interesting result here is that WPM, which typically produces lower quality mappings, consistently produces shallower circuits. We also observe up to a 23% gap for Sabre on the multi-ring topology yielded by the Feautrier transformation.

The cheung circuit exhibits N-way data-parallelism, N being the number of pipelined CCNOT (Controlled-Controlled NOT) gates found at the bottom of the circuit. The first CCNOT of each qubit can be mapped to a distinct qubit to maximize parallelism and reduce the circuit depth. Intuitively, both the Feautrier and Plutomin should yield the highest benefit in terms of circuit depth, since maximizing the number of satisfied dependences per schedule dimension equates to minimizing the maximal-dependence distance. The circuit’s depth drastically increases with quality of the qubit allocator. This is due to the fact that the control qubits for each operation start the closest and separate as the state evolves. This, in turn, requires more swaps operations to make the qubit operands adjacent.

The arithmetic adder using the majority and unmajority circuit pattern, adder-maj-uma, exhibits a highly serial form in its steady-state. The only opportunities for reordering transformations arise from the potential fusion/distribution of the CNOT operations with the sequence of CCNOTs following later. In general terms, we expect the Plutomax to have the highest impact on the circuit depth. The same observations hold for the cuccaro-adder-6bit adder, which differs from the former in the degree of data-parallelism. This translates to much shallower circuits, roughly half the depth of the adder-maj-uma counterparts. It also differs in that base and Plutomin typically achieve the best circuit depth due to the already available parallelism. All four qubit allocators also benefit from the higher scheduling and placement flexibility of cuccaro-adder-6bit due to the lower number of CCNOTs (3-operand gates) as well as the presence of CNOT and NOT gates.

Benchmarks sum5 and initG5 [69] share similar properties. As both exhibit distinct and noticeable parallel and
serial phases. For instance, sum5’s initial and init-G5 ending phase offer a lot of reordering freedom in the scheduling and placement of the CNOT operations. In contrast, the middle and ending phases of sum5 and initial and middle ones of init-G5 are mostly serial with stints of pipelined parallelism. In addition, the large and varying separation between the gate operands induce a higher number of required SWAP operations. These combination of factors make harder the prediction of the most suitable affine transformation, making the outcome highly variable w.r.t to the coupling graph and the qubit allocator. So the overall topological trends remain.

Circuit cnt3-5_179 also shares some similar features with circuit cuccaro-adder-6bit. They both have a mix of data- and pipelined parallelism, with short constant distance (3 or lower) among the gate operands. These traits contrast with benchmark rd84_142 which exhibits much larger, but constant separation (5). cnt3-5_179 benefits from a slighter higher degree of data parallelism (left-most CNOTs). Given the combination of characteristics, we expect plutomax to
FIGURE 7. Impact of problem size scaling on circuit depth for cheung circuit on topologies grid (top), multi-ring (middle) and tiled (bottom)

FIGURE 8. Impact of problem size scaling on circuit depth for pipelined-swap circuit on topologies grid (top), multi-ring (middle) and tiled (bottom)

be more beneficial for rd84_142, while feautrier and plutomin to perform best (or close to) for cnt3_5_179, as loop fission will effectively isolate the parallel operations from the more serial/pipelined ones. Empirically, both of these observations and hypotheses hold.
Impact on Circuit Size Next, we show in Fig.6 the gap in circuit size for four of the previous circuits. The analysis and justification is as before, revolving around the variability in data- and pipelined parallelism, specific properties of the circuits such as the distance between its qubit operands (fixed-short, fixed-large or variable), and the underlying topology. In particular, we highlight that wpm effectively detected that the pipelined-swap was a swap circuit in itself, unlike all other allocators, which still attempted to optimize the circuit. We also observe circuit gaps ($\Delta_{\text{transform}} / \text{max(added)}$) of up to 26% even for jku, on sum5.

Impact of Circuit Scaling To complement our study, we perform a scaling evaluation of circuits pipelined-swap and cheung. We focus on these benchmarks due to their high regularity and lack of singleton quantum statements that require more specific scheduling. We vary the SCoP parameter $N \in \{2, 12\}$. Beyond this, the quantum register size is exceeded. To judge the overall scaling behavior, the last four bar clusters in each figure show the arithmetic mean of each allocator varying the loop transformation. We note that pipelined-swap using jku on the grid topology only scaled up to $N=6$ (14 qubits), at which point each run started taking above an hour to complete. Furthermore, at $N=10$, memory was being exhausted in our benchmarking server. The time limit was also exceeded for the base variant of pipelined-swap using jku on the other two topologies, for $N \geq 8$. A consequence of the $A*$ search used by jku. Next, we center our attention on the cheung benchmark, which only utilizes CCNOT gates. This trait makes it fare best on topologies with higher number of vertices with degree 3 or higher, i.e. tiled (24) and grid (32). The impact of this requirement is notorious on the multi-ring (8) graph, which for $N=4$ requires a total of 8 (4 producing and 4 consuming) gates. Past this point the number of swaps operations introduced by the wpm allocator nearly doubles for every increment of 2 on N. Given these resource restrictions, we now refine our first assessment on this circuit, and expect the feautrier transformation to fare best, as it was conceived as a minimum latency, resource conscious transformation. Equivalently, we also now expect plutomax to induce typically higher circuit depth. The intuition here (in classical loop transformation terms) is that the plutomax heuristic would amount to an outer parallel loop and an inner serial loop, while the feautrier transformation would make the outer loop serial, thereby exposing more inner parallelism. The general effect of this trade-off for most qubit allocators is to expose earlier the gate-to-gate dependences. In particular, this is most beneficial when the allocator makes local decisions using sliding windows.

Changing our focus to the pipelined-swap circuit, we first note that, unlike the previous benchmark, this one only consists of CNOT gates. Thus, the number of vertices with degree 3 or higher is not a limiting factor. This provides more freedom to the qubit allocators. In general, the jku allocator produces the circuits with the shallowest depth, outperforming sabre in every topology. Nonetheless, we highlight that wpm in tandem with plutomax yields results comparable, and at times better, than sabre. This is relevant because wpm is $10 \times$ faster than sabre and $10 \times$ to $15 \times$ faster than jku. The much improved circuit depth w.r.t to wpm’s impact on other benchmarks is due to a specific feature of pipelined-swap. If we divide the circuit into four quadrants, the north-east (NE), north-west (NW), south-east (SE) and south-west (SW), and consider them as the four statements to schedule, we can notice that the NW and SW statements converge in the middle of the circuit. This means that the underlying qubit allocator would benefit from finding those operations, the ones in the middle of the four quadrants, concentrated into a small window of operations. That is precisely the effect of using plutomax, and leads up to a 60% circuit depth improvement when using wpm on the tiled topology.

5 Related Work
Modeling affine quantum circuits shares some similarities with polyhedral process networks (PPN) [54, 74], independent processes that communicate with unbounded FIFOs. However, most of their work has focused on translating serial programs into parallel hardware. Polyhedral and affine transformations have also successfully targeted several architectures, among them CPUs [38, 49], GPUs [8, 32, 47, 77], and FPGAs [4, 57]. Functional languages have been proposed as viable candidates for the specification of quantum programs: [46] introduced a statically typed functional DSL; [5] introduced the QML language focused on allowing the specification of reversible and irreversible quantum computations and combining it with first order strict linear logic. The Scaffold language and the ScaffCC compiler [39, 40] allow for a modular organization of quantum programs, and are equipped with control-flow constructs that allow to manipulate quantum gates. Loke, Wang and Chen [16, 50] developed the Qcompiler and OptQC, which focused on the optimization of circuits by determining permutation matrices that minimized the number of required swap gates. Their algorithm used simulated annealing to determine near optimal number of swap gates. Svore et al. developed Q# [68], a DSL with a rich type system, modular definitions, reversible operations, control-flow constructs and qubit management. Similarly, quantum instructions sets [63] and assembly languages such as OpenQASM [21] and cQASM [12] (the common Quantum Assembly language) have also been proposed. Qiskit [37] is an open sourced quantum toolkit, available as a Python package, which enables users to write programs with OpenQASM and run them in the IBM Quantum Experience [58], a cloud service. These efforts embody important software building blocks that new quantum compiler
infrastructures can build upon to develop more scalable and high-level frameworks. RevKit [64, 65] has also been used to support fully automatic synthesis of quantum circuits [66], Quipper [29, 30], an embedded quantum programming language for circuit specification developed by Green et al., introduced several features such as ancilla scope and reuse, classical to quantum circuit lifting for automatic generation of application specific oracles, basic data types, boxed/procedural definition and reversing operators for defined circuits. LIQUi> [78], a DSL for quantum computing, proposed language features such as static typing, opaque types for qubit and kets representation, and introspection functionality that uses Microsoft’s F# language and .NET support. [55] introduced QWIRE, a language designed for the specification of quantum circuits with strong type system and safe properties for well defined circuits. In QWIRE, circuits are first-class citizens, and provides boxing and unboxing functionality that enables the composition of circuits. In addition, it also leverages dynamic lifting to convert a quantum circuit to its classical equivalent. Lastly, efforts to produce more robust quantum program mappings for NISQ (Noisy Intermediate-Scale Quantum) architectures by exploiting calibration parameters, scalability and routing options are also being explored [53].

6 Conclusion and Future Directions

In this paper we have introduced the first polyhedral quantum specification language and compiler, AXL. We have demonstrated how off-the-shelf polyhedral analyses and transformations from the classical HPC world can be applied and beneficial to quantum computing. We have found that even not-yet-tailored transformations can improve state-of-the-art qubit allocators such as jku and sabre by as much as 36%, and others such as wpm by 60%. Clearly, much work remains. An obvious follow up is to devise different model-driven optimizations that embed parallelism constraints, as well as considering the underlying machine topology.

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Appendix A
Due to space constraints and for better viewing, we include the set of evaluated circuits in this appendix. The set of circuit benchmarks evaluated in our work are summarized in Tab.3. These should be viewed as small computational building blocks used in larger applications, in similar spirit to modern and classic computational kernels such as DGEMM.

Here we quickly summarize their overall role/goal:

- sum5,init-G: Sub-circuits used in [69] corresponding to the computation of initial values and sum of an adder. The circuits do not use ancillary qubits, and have depth $O(n)$. The corresponding circuit diagrams shown in Fig.10.

- pipelined-swap: Performs a qubit SWAP operation between two qubits 2N lanes apart. We show in Fig.9 its implementation in AXI, and its circuit diagram in Fig.11.

- cnt3–5–179: A 5 digit binary coded ternary counter with count control input (cnt) [79]. Circuit diagram shown in Fig.12.
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Figure 10. init-G₅ and sum5 circuits

Figure 11. pipelined-swap[27]

Figure 12. cnt3–5.179 and cheung circuits

Figure 13. rd84_142[79]

```plaintext
param N;
statement S1a, S1b, S1c;
statement S2a, S2b, S2c;
statement S3;
statement S4a, S4b, S4c;
statement S5a, S5b, S5c;
S1a := {i: 0<=i<N (%) # CNOT(i, i+1) };   
S1b := {i: 0<=i<N (%) # CNOT(i+1, i) }; 
S1c := {i: 0<=i<N (%) # CNOT(i, i+1) };   
S2a := {i: 0<=i<N (%) # CNOT(2*N-i+1, 2*N-i) }; 
S2b := {i: 0<=i<N (%) # CNOT(2*N-i, 2*N-i+1) };  
S2c := {i: 0<=i<N (%) # CNOT(2*N-i+1, 2*N-i) };  
S3 := {i: i = N (%) # CNOT(i, i+1) (+) #CNOT(i+1, i) (+) #CNOT(i, i+1) };  
S4a := {i: 0<=i<N (%) # CNOT(N-i-1, N-i) };  
S4b := {i: 0<=i<N (%) # CNOT(N-i, N-i-1) };  
S4c := {i: 0<=i<N (%) # CNOT(N-i-1, N-i) };  
S5a := {i: 0<i <= N (%) # CNOT(N+i+1, N+i) };  
S5b := {i: 0<i <= N (%) # CNOT(N+i, N+i+1) };  
S5c := {i: 0<i <= N (%) # CNOT(N+i+1, N+i) };  
codegen { S1a (+) S1b (+) S1c (+) S2a (+) 
S2b (+) S2c (+) S3 (+) S4a (+) S4b (+) 
S4c (+) S5a (+) S5b (+) S5c } with { N=6};
```

- cheung: sub-circuit used in computing the $\tilde{d}$ component of the Elliptic Curve Discrete Logarithm problem (ECDLP) [17]. Circuit diagram shown in Fig.12.
• \texttt{rd84_142}: Counts the number of ones in the input\cite{79}. Circuit diagram shown in Fig.13.

• \texttt{adder-maj-uma}: is a ripple-carry adder using the in-place “MAJority” (MAJ) and “UnMajority and Add” (UMA) patterns \cite{22}. Circuit diagram shown in Fig.14.

• \texttt{cuccaro-adder-6bit}: Depth optimized ripple-carry adder of depth $2n + 4$, with $2n - 1$ time slices and $5$ CNOT time-slices \cite{22}. Circuit diagram shown in Fig.14.

\textbf{Figure 14.} \texttt{adder-maj-uma} and \texttt{cuccaro-adder-6bit} circuits