CASCADED H-BRIDGE MULTILEVEL INVERTER BASED DSTATCOM FOR POWER QUALITY IMPROVEMENT

Jagdish Kayasth¹ and R.P. Hasabe²

¹,² Department of Electrical Engineering, WCE, Sangli

Abstract- This paper investigates the compensation of reactive power and harmonics in distribution network by using the cascaded H-bridge 5 level inverter based DSTATCOM. The CHB MLI has many advantages such as less no. of components which suppress the switching losses and also harmonics. DSTATCOM is used to mitigate the voltage sag problem by maintaining the voltage profile flat and reduce the THD in nonlinear network. It also improves the power factor. The reference compensating current for DSTATCOM is generated using synchronous rotating reference frame (SRF). The capacitor DC link voltage of H-bridge is regulated by Proportional-Integral controller. The 1kv distribution system is consider for shunt compensation. CHB performance is carried out by level shift PWM and phase shift PWM techniques. The simulation result are obtained through MATLAB.

Keywords-DSTATCOM, Synchronous rotating reference frame, CHB multilevel inverter, Phase shift PWM, Level shift PWM, PI Controller

I. INTRODUCTION

Power quality is often defined as the grid's ability to supply a stable and clean power supply. In other words, power is always available, has a pure harmonics-free sinusoidal wave shape, and is always within frequency and voltage tolerances. However, with increasing and varying energy demands from various industries, many loads regularly causes disturbances on the grid, making frequent deviations from ideal conditions.

In Electric network especially distribution, have large no. of nonlinear loads, which affect the quality of power significantly. Apart from nonlinear loads, events like motor starting, unusual faults, and capacitor switch could also affect power quality. Power quality problem is defined as any manifested problem in voltage and current or frequency deviations that result in mal operation or failure of customer equipment. Voltage swells and sags are among the many power quality problems to face in the industrial processes. Voltage sags are more severe. Due to presence of reactance Most of the AC loads are consuming reactive power. Consumption of reactive power causes poor voltage quality. A reliable and fast control over the transmission parameters is offered using the FACTS devices, i.e. Voltage, phase angle between the sending end and receiving end voltages and line impedance. Alternatively the custom power is for low voltage, and achieving the good quality and reliability of supply.

Custom power devices are nearly equal to the FACTS. Most widely known custom power devices are UPQC, DSTATCOM, DVR among them DSTATCOM is very well known. [5]. DSTATCOM can exchange both active and reactive power with the distribution network by varying the phase angle and amplitude of the inverter voltage with respect to line terminal voltage.

A multilevel inverter can reduce the device voltage and the output harmonics by increasing the number of levels of output voltage. There are many types of multilevel inverters: Diode clamped, cascaded H-bridge (CHB), flying capacitor. Among these topologies, CHB inverters are being widely used because of their simplicity and modularity. The installation of cascaded H-bridge converters for DSTATCOM applications leads to reduced injection of harmonics and low cost. This paper investigates a DSTATCOM with a PI controller based CHB multilevel inverter for the reactive power and harmonics mitigation of the nonlinear loads.
II. DESIGN OF CHB BASED DSTATCOM

The DSTATCOM (Distribution Static Compensator) is a voltage source inverter based that is used for mitigation of voltage sags. It is Connected (usually shunt) to the distribution network via a coupling transformer. The DSTATCOM continuously generate variable inductive or capacitive shunt compensation up to its maximum MVA rating. The DSTATCOM, with respect to reference ac signal continuously checks the line waveform, and further, it can provide lagging or leading reactive current compensation to reduce the voltage fluctuations. The major components of a DSTATCOM are shown in Fig. (1). It consists of an inverter module (Cascaded), dc capacitor, a transformer to match the line voltage and inverter output, and a PWM control strategy. [6]

![Fig.1 Components of DSTATCOM](image_url)

Cascaded H-bridge (CHB) multilevel inverter is popular converter topologies used in high-power medium-voltage (MV) application. It consist of a units of single-phase H-bridge cells. The H-bridge cells are normally connected in cascade to obtain medium-voltage and low harmonic distortion operation. The inverter requires a no. of isolated dc supply to feed each H-bridge power cell. The number of voltage levels in a CHB inverter can be determine by

\[ m = (2H + 1) \]

The voltage level \( m \) is always an odd number for the CHB inverter while in other multilevel topologies such as diode-clamped inverters, it can be either an even or odd number. Where H is the number of H-bridge cells per phase leg.

The voltage source converter (VSC) converts the dc voltage across the capacitor into a set of three-phase ac output voltages. These voltages are in phase and coupled with the ac system through coupling transformer. Effective adjustment of the magnitude and phase of the DSTATCOM output voltages allows efficient control over active and reactive power exchanges between the ac system and DSTATCOM. [1]

The Voltage source converter connected in shunt to the ac system provides a multifunctional topology which can be used for following distinct purposes:
I. Voltage regulation and compensation of reactive power;
2. Elimination of current harmonics.
3. Correction of power factor.

The controller operate the inverter in such a way that phase angle between the line voltage (\( V_L \)) and the inverter voltage (\( V_i \)) is dynamically adjusted so that the DSTATCOM absorbs or generates the required VAR at the point of common coupling. If \( V_i \) equals to \( V_L \), the reactive power is zero and the DSTATCOM does not generate or absorb reactive power. If \( V_L \) is greater than \( V_i \), the system ‘sees’ an inductive reactance connected at its terminal and the DSTATCOM ‘sees’ the system as a capacitive reactance. Then the current flows from the ac system to the DSTATCOM, resulting absorbing inductive reactive power by device.

When \( V_i \) is greater than \( V_L \), the DSTATCOM ‘sees’ an inductive reactance connected at its terminal. Hence, the system ‘sees’ the DSTATCOM as a capacitive reactance. The current, I, flows through the coupling inductor from the DSTATCOM to the ac system, and the device generates capacitive reactive power.
A. Design of Five level CHB

The cascaded H-bridge multilevel inverter consist series connected multiple units of H-bridge cells to produce high ac voltages. A typical five-level CHB inverter configuration is shown in Fig. Y where two H-bridge cells powered by two isolated dc supplies of equal voltage $E$, are placed in each phase. The dc supplies are normally obtained by multipulse diode rectifiers. By switching the switches in proper conduction, different level of phase voltages can be obtained. Some voltage levels can be obtained by more than one switching state. The switching state redundancy is a common phenomenon in multilevel converters. It provides a great flexibility for switching pattern design.

![Fig. 2 Five-level cascaded H-bridge inverter.](image)

B. PWM for CHB

The PWM techniques for CHB inverter can be generally classified into two categories are

1. Phase Shifted Carrier PWM

2. Level Shifted Carrier PWM

1. Phase Shifted Carrier PWM (PSCPWM):
   - A multilevel inverter with $m$ voltage levels requires $(m - 1)$ triangular carriers. In the phase-shifted multicarrier modulation all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by
   \[
   \phi_c = \frac{360^\circ}{(m - 1)}
   \]

![Fig. 3 Phase shift PWM](image)

2. Level Shifted Carrier PWM (LSCPWM):
   - Similar to the phase-shifted modulation, an $m$-level CHB inverter using level-shifted multicarrier modulation scheme requires $(m - 1)$ triangular carriers, all having the same frequency and amplitude. The $(m - 1)$ triangular carriers are vertically disposed such that the bands they occupy are contiguous.

![Fig. 4 Level shift PWM](image)
III. CONTROL ALGORITHMS

SRF theory is actually transformation of currents in rotating synchronously $d$–$q$ frame called as Park’s transformation. This transformation is implemented using transformation angle ($\theta$). Fig. (Z) Shows the structure of this theory. Inputs $i_{La}$, $i_{Lb}$, and $i_{Lc}$ and $Va$, $Vb$, and $Vc$ are sensed and are fed to controller. PLL (phase-locked loop) is used to processed voltage signals to generate unit voltage templates (sine and cosine signals). Three phase current signals are transformed d–q frame and by using inverse transform d–q frame is transformed to abc ($i_{sa}$, $i_{sb}$, and $i_{sc}$), frame called as reverse Park’s transformation. Further to generate DSTATCOM’S switching signals the abc frame is fed to PWM technique employing hysteresis loop. Controller for DSTATCOM is shown below.

![Fig. 5. Block diagram of the reference current extraction using SRF theory.]

IV. MATLAB/SIMULINK MODELING AND SIMULATION RESULTS

The Simulink model of the proposed Cascaded H-Bridge multilevel inverter based DSTATCOM is simulated in MATLAB. The parameters implemented in this simulation are source voltage of 1 kv, 50hz AC supply, DC bus capacitance 10000e-6 F, Inverter series inductance 3mH, Source resistance and inductance 0.1ohm and 0.9mH respectively. Load resistance and inductance are 60 ohms and 30mH respectively. The Simulink Block diagrams are shown below.

![Fig. 6 Simulation Diagram of Proposed Topology]

The Simulink power circuit model of DSTATCOM consist of source block, non-linear load, control block, APF block and measurement block. The 3–phase cascaded H-Bridge of 5 level output voltage (phase) is simulated in Simulink model to achieve the compensation. A 5 level output of inverter is shown in Fig (7)
Fig. 7 five level output

Fig. 8 shows the three phase source currents without DSTATCOM. It is clear that without DSTATCOM the source current has distortion.

Fig. 8 Source current before compensation

Fig. 9 shows the harmonic spectrum of Source current without DSTATCOM. The THD of source current without DSTACOM is 30.46%.

Fig. 9 THD in source current before compensation

Fig. 10 shows the three phase source currents with DSTATCOM. It is clear that with DSTATCOM the source current has less distortion and it’s nearly sinusoidal.

Fig. 10 Source current after compensation
Fig.11 shows the harmonic spectrum of Source current with DSTATCOM. The THD of source current without DSTACOM is 2.64%.

![Fig.11 THD in source current after compensation](image)

Fig.11 THD in source current after compensation

Fig.12 shows the waveform for voltage sag generated during 0.4 to 0.6 sec. Voltage dips to 25% normal value.

![Fig.12 Voltage sag before Compensation](image)

Fig.12 Voltage sag before Compensation

Fig.13 shows the waveform for compensation of voltage sag using DSTATCOM.

![Fig.13 Voltage sag after Compensation](image)

Fig.13 Voltage sag after Compensation

IV. CONCLUSION

The paper presents five Level H bridge Cascaded Multi Level Inverter as DSTATCOM. The proposed theories are able to generate the pulses for the MLI to give the output of 5 level voltage. Hence with this techniques the harmonic compensation is done for the nonlinear load system. Results shown that the THD for the source current is 30.46% before the compensation and it is reduced to the 2.64% after compensation, in permissible limit as per IEEE 519 Standard.
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