Investigating the Impact of Self-Heating Effects on some Thermal and Electrical Characteristics of Dielectric Pocket Gate-all-around (DPGAA) MOSFETs

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Abstract
The dielectric pocket gate-all-around (DPGAA) MOSFET is being considered the best suited candidate for ULSI electronic chips because of excellent electrostatic control over the channel. However, the phenomena of self-heating and hot carrier injection (HCI) severely affect the performance of the device, and make the behaviour of the DPGAA FET very unpredictable. In the present article, a comprehensive investigation under the influence of self-heating effects has been done for the variation in the lattice and carrier temperature against spacer length, ambient temperature, device length, and thermal contact resistance including ON and Off currents with gate bias voltage (VGS). In order to analyse the SHEs, the hydrodynamic (HD) and thermodynamic (TD) transport models have been used for three-dimensional (3D) electrothermal (ET) simulation. The Lucky (hot carrier injection) model has been used to study the HCI degradation in DPGAA MOSFET using Sentaurus 3D TCAD simulator.

Keywords HCI · Electro-thermal (ET) effects · Thermal contact resistance · Ambient temperature · Phonons · Optical mode · Acoustic mode

1 Introduction
Under the arena of nanoscale CMOS technology, the gate-all-around (GAA) MOSFET is one of the most promising devices. The published reports [1] claimed that the device could have excellent channel control, better subthreshold characteristics, large packing density, and short channel effects (SCEs) immunity [2]. Moreover, according to IRDS 2017 edition report, the CMOS structure has the feasibility to be downscaled below 22 nm [3]. Reports say that the GAA CMOS Technology node shall reach 3 nm by 2022, and one of the leading fabrication industries has proposed adopting the GAA structure for their upcoming CMOS Technology node [4]. For further improvement in the device performance, dielectric pockets (DPs) have been introduced in the channel region at the drain-channel and source-channel interface. The DP MOSFET is getting a lot of attention as a potential architecture due to restrained SCEs and minimized Off-current [5, 6]. The Off-current (Ioff) gets reduced as the DP acts as a diffusion stopper and impedes the path of punch through [7].

Although downscaling of the device increases the number of transistors per unit area on a chip, the chip suffers from high power dissipation and self-heating problem with the passage of time [8, 9]. The shrinkage in device dimensions results in unbalanced scaling of dimensional parameters and supply voltage which causes a high electric field (~1MV/cm) near the channel-drain junction. This high electric field energizes the charge carriers to higher energy levels whence they become hot carriers. Accumulated hot carriers in the channel give rise to self-heating problem in the gadget [10–14]. The heating effect severely deteriorates the performance of the device owing to mobility reduction, increased gate leakage current, down fall in drain saturation current [15]. Moreover, the degradation in device performance also comes from electrothermal (ET) issues due to variation in ambient temperature, injection of hot-carrier, etc. [16].
Some researchers have investigated self-heating effect (SHE) in silicon-based GAA MOSFETs [17–26]. Park et al. [17] studied the ET effects and degradation of drain current in GAA MOSFETs with vertically stacked multiple silicon-based nanowire channels. Shin et al. [18] developed an ultrafast high-resolution thermo-reflectance (TR) imaging technique for investigating the increase in local surface temperature and high-resolution measurements by heating and cooling at constant time. Further, Kompala et al. [19] investigated the device performance degradation by the ET conductivity problem owing to the lower thermal conductivity of gate oxide, spacer region material, and higher thermal contact resistance (Rth). Pala et al. [20] studied the effect of self-heating with quantum confinement effects (QCEs) in the Nano-electronic device. Asheghi et al. [21] calculated the degradation in thermal conductivity due to the phonon-boundary scattering in terms of a simple mathematical model. It revealed the excessive drain current degradation due to SHEs in Silicon-based GAA MOSFETs. A. Kumar et al. [22] depicted that SHE and HCI severally degrade the performance of DGAA MOS due to high gate leakage current. S. Banchhor et al. [23] analysed that SHE causes zero temperature coefficient (ZTC) bias-point instability in SOI-FINFETs. I. Myeong et al. [24] reveal the effect of air gap/spacer for changing the thermal property of VFET. To date, the influence of ambient temperature (T_A), Drain voltage (V_DS), and device parameters such as spacer length, spacer conductivity, device length, and thermal contact resistance on carrier temperature, lattice temperature, along with hot carrier injection (HCI) induced degradation of DPGAA FET has not been investigated in detail.

The present work is dedicated to discuss the comprehensive study of variation in lattice temperature (T_L) and carrier temperature (T_C) against ambient temperature (T_A), drain-to-source voltage (V_DS), and different device geometries of the DPGAA MOSFET. The work also includes the study of hot carrier injection (HCI) in the device. All the mentioned works has been carried out using electrothermal (ET) simulation. The entire manuscript is organized as: Section II covers the device structure and methodology. Section III describes the results and discussion, and finally section IV sums-up the work.

2 Device Structure and Simulation Methodology

The 3D schematic diagram of DPGAA MOSFET for simulation on Sentaurus device simulator is shown in Fig. 1. In this structure, the silicon-based nanowire channel region is wrapped around by a thin oxide layer and contact metal (Tungsten Nitride) with a work function (\(\phi_{M} \)) of 4.7 eV [27]. Molybdenum (Mo) is used as a source/drain contact metal. All other physical parameters of the DPGAA MOSFET architecture for simulations are listed in Table 1, and the thermal parameters used for electrothermal (ET) simulations are listed in Table 2.

The Hydrodynamic (HD) and Thermodynamic (TH) transport models have been coupled for the purpose of simulation. The HD model [28] acquires the electrothermal (ET) characteristics of carrier transport along with the carrier temperature (T_c) effect. The lattice temperature (T_L) variation has been obtained by solving the Poisson’s equation of lattice heat flow. The density gradient model is applied for solving the quantum confinement effects (QCEs) of the charge carriers in the channel region. For the electrothermal (ET) simulation, the temperature-dependent thermal conductivity (TC) model [28] is applied for silicon TC dependence on channel film thickness. The Lombardi (CVT), Philips unified mobility, and high field saturation models have been used to simulate temperature, carrier concentration, and carrier-to-carrier scattering dependent carrier mobility. The constant thermal contact resistance value at an isothermal ambient temperature of 300 K has been used for thermal boundary conditions of device terminals. Figure 2a and Fig. 2b show the calibrated transfer characteristics for appropriate models and simulation data validation.

3 Results and Discussion

3.1 Effect on Lattice and Carrier Temperature

The onset of self-heating occurs when the nearly free conduction band electrons in the channel region are accelerated by the electric field because of rise in the drain voltage (V_DS). The electrons (carriers) gain energy from the field and consequently, carrier temperature (T_C) increases. The carriers lose energy by inelastically scattering with the lattice phonons, where the carriers with energies below 50 meV scatter mainly with acoustic phonons, whereas, those with higher energy scatter strongly with the optical modes [29]. Such scattering events result in transfer of energies (heat) to the crystal lattice, and hence carrier temperature (T_C) is found much higher than the lattice temperature (T_L) (i.e., T_C > T_L). In Fig. 3, the variations of the maximum lattice temperature (T_{L,max}) and carrier temperature (T_{C,max}) against V_{DS} for V_{GS} = 1 are shown. It be observed that T_{C,max} and T_{L,max} increase gradually up to 0.1 V of V_DS owing to low-field transport (LFT) mechanism. On the other hand, for V_{DS} from 0.1 V to 1 V, T_{L,max} and T_{C,max} could be seen rising from 303 K to 398 K and 360 K to 2664 K because of high-field transport (HFT) mechanism. It may be noted that enhancement in carrier temperature results in phonon emission, where a significant portion of the generated phonons correspond to optical modes (low group velocity) or acoustic modes. Figure 4 deals with the changes in T_{L,max}...
and $T_{C_{\text{max}}}$ against change in spacer lengths ($L_{\text{SP}}$) at $V_{\text{DS}} = V_{\text{GS}} = 1$ V. The expansion in spacer length ($L_{\text{SP}}$) at fixed channel length extended the space between side contacts with the channel. It produced two effects (a) the induced electric field gets reduced along the channel length at the same value of $V_{\text{DS}}$ and diminished the carrier energy, as a result of which $T_{C_{\text{max}}}$ got reduced. (b) The heat dissipation path extended for the channel from cooling sinks (metallic contacts of D/S) and caused the increase in $T_{L_{\text{max}}}$. As per Fig. 4, against the variation of $L_{\text{SP}}$ from 10 nm to 30 nm, the $T_{L_{\text{max}}}$ rises from 333 K to 398 K (~16% increase), and conversely $T_{C_{\text{max}}}$ falls from 3131 K to 2664 K (~15% decrease). Figure 5 displays the contour plots of (a) lattice temperature and (b) electron temperature in silicon nanowire along device length (nm) at $V_{\text{GS}} = V_{\text{DS}} = 1$ V. Hot carriers (high energy carriers) moving from the source undergo heavy scattering near the drain side and give their energy in the form of phonons to the lattice. Consequently, there is increase in lattice temperature ($T_{L}$) near the drain region locally. Note that, the area of maximum lattice temperature ($T_{L_{\text{max}}}$) is known as a ‘Hotspot’, where the density of optical phonons is the maximum. The variations in $T_{L}$ and $T_{C}$ against the device length for the fixed values of $V_{\text{DS}}$ and $V_{\text{GS}}$ at 1 V are demonstrated in Fig. 6. It is already mentioned earlier that near the channel-drain interface, the energy of carriers gets sufficiently high owing to high electric field which make them hot. In Fig. 6, it can be easily observed that the electron temperature ($T_{C}$) near the channel-drain interface ($\approx 55$ nm) reaches the peak value which is near 2500 K. Note that, in the course of journey from source to drain, the carriers gain energy, and at the same time they also got scattered with lattice ions which results in generation of phonons. Therefore, an increase in lattice and carrier temperature may be observed in the plot. When the hot carriers enter the drain region, due to reduced mean free path length, there is a surge in electron-lattice scattering events resulting in a steep increment in lattice.

### Table 1: Device parameters used for DPGAA MOSFET simulation

| Sl. No. | Parameter                        | Symbol | Value       |
|--------|----------------------------------|--------|-------------|
| 1      | Channel Length                   | $L_{\text{C}}$ | 20 nm       |
| 2      | Source/Drain Doping              | $N_{\text{D}}$ | $10^{20}$ cm$^{-3}$ |
| 3      | Channel doping                   | $N_{\text{A}}$ | $10^{15}$ cm$^{-3}$ |
| 4      | Oxide thickness                  | $t_{\text{ox}}$ | 2 nm        |
| 5      | Channel thickness                | $t_{\text{id}}$ | 10 nm       |
| 6      | Dielectric pocket length         | $D_{\text{PL}}$ | 4 nm        |
| 7      | Dielectric pocket thickness      | $D_{\text{PD}}$ | 4 nm        |
| 8      | Spacer Length                    | $L_{\text{SP}}$ | 10–30 nm    |
| 9      | Source/Drain Contact Length      | $L_{\text{SC}/L_{\text{DC}}}$ | 5 nm        |
| 11     | Thermal Contact Resistance [16]  | $R_{th}$ | $1 \times 10^{-5}$–$1 \times 10^{-4}$ cm$^2$K$^{-1}$W$^{-1}$ |
| 12     | Gate-to-source voltage           | $V_{\text{GS}}$ | 0–1 V       |
| 13     | Drain-to-source voltage          | $V_{\text{DS}}$ | 0–1.2 V     |
temperature as obvious from the fig. 6. At the same time, it can be seen that the carriers lose their energy through scattering and their temperature starts decreasing from the channel-drain interface. Near the metallic contact, the lattice temperature again starts decreasing due to heat dissipation through the metallic contact.

3.2 Output and Transfer Characteristics under SHE

Figure 7 shows the behaviour of output characteristics of the DPGAA MOSFET versus $V_{DS}$ with SHE and without SHE for different $V_{GS}$. Self-heating causes the carrier mobility to degrade in the channel near the drain side due to populated hot carriers scattering, which result in the downfall of drain saturation current with the increase of $V_{DS}$ at a particular value of $V_{GS}$. As per Fig. 7, the drain saturation current decreases due to SHE by approximately 8% in DPGAA MOSFET at $V_{GS} = 1$ V. The next figure (Fig. 8) depicts the transfer characteristics of DPGAA versus $V_{GS}$ with SHE and without SHE at $V_{DS} = 0.75$ V. It depicts that the on-state current of DPGAA degrades with SHE on increasing value of $V_{GS}$, where the impact of SHE is staring at 0.75 gate bias. The degradation of electron mobility and electron velocity along device length (nm) at $V_{GS}=V_{DS} = 1$ V is shown in Fig. 9. The electron mobility degrades by approximately 50% from source-channel to drain-channel interface. However, the electron velocity increases suddenly with a significant peak value ($1.37 \times 10^8$ cm/s) in the channel region and tends to decrease near the drain and channel interface in the drain region.

3.3 SHE Variations Due to Thermal Contact Resistances ($R_{th}$)

Thermal contact resistance ($R_{th}$) plays a vital role in the heat transfer mechanism of the device. The low value of $R_{th}$ provides a fast thermal conducting path for heat flow from the
device through source and drain contacts. Figure 10 & Fig. 11 depict the increase in Lattice and carrier temperature for higher values of thermal contact resistances ($R_{th}$), respectively. According to Fig. 10, when $R_{th}$ varies from $1 \times 10^{-5}$ cm$^2$K$^{-1}$ to $1 \times 10^{-4}$ cm$^2$K$^{-1}$, lattice temperature ($T_L$) increases from 332 K to 472 K (~42% increase). On the other hand, in Fig. 11, the electron temperature ($T_C$) can be seen increasing with an increase in $R_{th}$ near the source and drain contacts, but the ‘hotspot’ carrier temperature $T_{C_{max}}$ seems independent against the variation in $R_{th}$. The variation of maximum lattice temperature ($T_{L_{max}}$) with thermal conductivity of spacers for various values of $R_{th}$ is plotted in Fig. 12. It has been observed that if the thermal conductivity of spacers increases from 0.14 W/K-cm to 0.185 W/K-cm, the $T_{L_{max}}$ gets reduced by around ~5.1% for $R_{th} = 5 \times 10^{-5}$ cm$^2$K$^{-1}$. Obviously, the thermal conductivity of spacers may play important role in fighting with self-heating effects. Figure 13 shows the variation of the drain current versus $R_{th}$ for various types of gate insulators. The drain current decreases from 39.8 $\mu$A to 25.3 $\mu$A (~36.4% decrease) for Al$_2$O$_3$, 38.9 $\mu$A to 24.6 $\mu$A (~36.8% decrease) for Si$_3$N$_4$ and 35.5 $\mu$A to 22.3 $\mu$A (~37.2% decrease) for SiO$_2$, respectively, which claims the scope of high K-dielectric (Al$_2$O$_3$) material to get the high drain current.

3.4 Gate Leakage Current under HCl Degradation

This section is dedicated to discuss the gate leakage current ($I_G$) under hot carrier injection with SHE for the DPGAA MOSFET. The hot carrier injection model (LUCKY) [30] is used in the ET simulation of the device. It is used to extract the significant values of the carriers injected into the gate oxide near the ‘hotspot’ region. Because of the presence of a strong vertical electric field in the channel region, the significant tunnelling current occurs through the gate oxide near the ‘hotspot’ region. These injected carriers break the ionic bonds of the gate oxide and create a tunnel, as a result of which gate leakage current ($I_G$) enhances and the drain saturation current ($I_{ON}$-current) degrades in the device [31]. In Fig. 14, the variation of the gate leakage current versus spacer length ($L_{sp}$) is plotted. Against the variation of spacer length from 10 nm to 30 nm, the gate leakage current ($I_G$) decreases from 13.5 nA to 4.8 nA (~64.5% decrease). It is explained earlier that the considerable spacer length reduces the carrier temperature ($T_C$) and hence causes a reduction in leakage current.
3.5 Effect of Ambient Temperature ($T_A$) Variations

The ambient temperature ($T_A$) is one of the crucial factors of SHE degradation [14]. Here, ET simulation has been used to investigate the SHE in DPGAA MOSFETs to analyse the impact of $T_A$. Figure 15 demonstrates the variation of the maximum lattice temperature ($hotspot$ temperature) ($T_{L_{\text{max}}}$) versus ambient temperature ($T_A$) for the various values of $R_{th}$. The $T_{L_{\text{max}}}$ increases from 398 K to 494 K (~24.1% increase) with the rise in $T_A$ from 300 K to 400 K for $R_{th} = 5 \times 10^{-5} \text{cm}^2 \text{K} \text{W}^{-1}$. The variation of the drain current ($I_D$) against ambient temperature ($T_A$) for the various values of $R_{th}$ is plotted in Fig. 16. Increasing $T_A$ from 300 K to 400 K, the $I_D$ decreases from 37.8 μA to 35 μA (~7.5% decrease) because the lateral electric field degrades the carrier mobility at $R_{th} = 5 \times 10^{-5} \text{cm}^2 \text{K} \text{W}^{-1}$. Figure 17 demonstrates the cutline plot of the variation in lattice temperature ($T_L$) versus device length (nm) for increasing $T_A$ values (300 K to 400 K in a step of 20 K). The drain lattice temperature ($T_L$) is higher than the channel and source regions because the high electric field enhances the scattering in the drain region. However, the $T_L$ increases with an increase in $T_A$.

4 Conclusion

The SHEs and HCI degradation in dielectric pocket gate-all-around (DPGAA) MOSFET has been discussed using ET simulation. Under the SHE, it is observed that the drain saturation current of DPGAA degrades by 8%. The $Off$-state
Fig. 9 Cutline plot of variation of electron mobility and electron velocity versus device length (nm).

Fig. 10 Cutline plot of the variation of lattice temperature ($T_L$) versus device length (nm) for various value of $R_{th}$.

Fig. 11 Cutline plot of the variation of electron temperature ($T_e$) versus device length (nm) for various value of $R_{th}$. 
Fig. 12 Variation of maximum lattice temperature ($T_{L_{\text{max}}}$) versus changing thermal conductivity of spacer for various value of $R_{th}$

Fig. 13 Variation of the drain current versus increasing in $R_{th}$ for various types of gate oxide

Fig. 14 Variation of the gate leakage current versus increasing spacer length ($L_{SP}$)

Fig. 15 Variation of the maximum lattice temperature (peak of ‘Hot Spot’) ($T_{L_{\text{max}}}$) versus increasing ambient temperature ($T_{A}$) for the various value of $R_{th}$
current ($I_{OFF}$) of DPGAA is being reduced due to the Dielectric Pocket. Hence the $I_{ON}/I_{OFF}$ ratio of DPGAA is found to be improved significantly. However, SHE may be ameliorated when the carrier temperature gets reduced by 15% and lattice temperature increases by 16% against the increase in spacer length ($L_{SP}$) from 10 nm to 30 nm. It is further noted that the HCI gets diminished for a similar increment in spacer length as the gate leakage current is reduced by 64.5%. The self-heating effect gets intensified because of rise in lattice and carrier temperature by 42% with the rise of thermal contact resistance ($R_{th}$) from $1 \times 10^{-5}$ cm²K⁻¹ to $1 \times 10^{-4}$ cm²K⁻¹. Therefore, the significant spacer length ($L_{SP}$) with appropriate thermal contact resistance may be utilized to design a less prone device from self-heating and HCI degradation.
Author Contribution All authors have made substantial contributions to the conception and design, or acquisition of data, or analysis and interpretation of data; have been involved in drafting the manuscript or revising it critically for important intellectual content; and have given final approval of the version to be published. Each author has participated sufficiently in the work to take public responsibility for appropriate portions of the content. All authors read and approved the final manuscript.

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