Incorporation of CdCl₂ Surface Treatment into the CdS/ZnTe Hetero-Junction Solar Cell Device Structures for Efficiency Improvement

J. Olaidje I. Olusola

Abstract - p-ZnTe thin film semiconductors have been successfully used as an absorber material to n-CdS window layer by effectively optimising the ZnTe absorber layer thickness. In order to create a two-terminal hetero-junction diode from the n- and p- type materials, two ohmic electrical contacts are required. This was achieved by depositing n-CdS layers on glass/fluorine-doped tin oxide (FTO) conducting substrate and evaporating Au on p-ZnTe layer. The ZnTe layer was successfully electroplated on CdS thin film grown on glass/fluorine-doped tin oxide (FTO) conducting substrates. The device structures were subjected to heat treatment in air with and without CdCl₂ surface treatment using temperature of 400°C and duration of 10 minutes. The incorporation of the CdCl₂ treatment led to enhancement in the solar cell efficiency. Solar cells developed from glass/FTO/n-CdS/p-ZnTe/Au device structure gave an open circuit voltage (V_OC) of 450 mV, short circuit current density (J_SC) of 7.26 mA cm⁻² and fill factor-factor (FF) of 0.31 resulting in ~1.0% efficiency (η) for n-CdS/p-ZnTe heterostructure annealed ordinarily in air. After treating the top surface of n-CdS/p-ZnTe heterostructure with CdCl₂ solution, all the solar cell parameters improved with V_OC of 480 mV, J_SC of 24.0 mA cm⁻² and FF of 0.46 giving a total efficiency of ~5.3%. For the CdS/ZnTe heterostructures treated without and with CdCl₂ solution, the rectification factors (RF) observed from the I-V characteristics under dark condition for these devices are 10^11 and 10^12 respectively. Both devices show ideality factors (η) in excess of 2.0 and the reverse saturation currents are 79.4 and 0.16 nA for heterojunction structures without and with CdCl₂ treatment respectively. The improvement in the solar cell efficiency can be accredited to the integration of the CdCl₂ treatment in the p-n junction cells.

Keywords - Solar Cells, p-n Junction Diodes, n-CdS, Heterostructure, p-ZnTe, CdCl₂ surface treatment.

1 Introduction

ZnTe and CdS semiconductors have energy gaps of 2.26 and 2.42 eV respectively. Electrical conductivities of n- and p-type have been mostly reported for ZnTe and CdS binary compound – based semiconductors. Doping via extrinsic means has been employed by researchers to obtain CdS films with p-type electrical conductivity (Chernow, 1968; Sebastian, 1993). ZnTe films have been widely acknowledged to possess p-type electrical conduction. The difficulty encountered in getting n-ZnTe semiconductors without the support of extrinsic dopants such as aluminium are as a result of self-compensation (Mandel, 1964; Sato et al., 2000) and native defects present in the ZnTe layers (Fauzi et al., 2013). In our research work, we have successfully overcome this hurdle of achieving n-ZnTe thin films through intrinsic means (Olusola et al., 2016).

The interfacing of n-CdS and p-ZnTe to produce heterostructure compound have been used to fabricate opto – electronic devices such as light emitting diodes (Ota et al., 1972; 1974). Diodes having good device quality were also obtained from the n-CdS and p-ZnTe heterostructure by Aven and Cook (1961). Aven & Garwacki (1963) investigated the way in which CdS layers are formed on ZnTe films. A lot of studies have been carried out on the heterostructure combining CdS and ZnTe but limited researches have been conducted on the suitability of the combined structure for solar cell applications. The experimental investigations reported by Pfisterer and Shock (1982) was the first to show that the ZnTe and CdS heterostructure is a feasible material for use in solar cell development.

Using vacuum evaporation technique, the authors deposited ZnTe on CdS which was grown on silver coated glass substrate. After the investigations performed by Pfisterer and Shock (1982), fewer reports exist in the literature on the viability of ZnTe to serve as absorber layer to CdS; one likely reason for this could be as a result of the ZnTe wide bandgap. Pfisterer and Shock (1982) reported the current density of their fabricated solar cells to be 3 mAc⁻² while the current density measured for the fabricated solar cells in this work after treating the topmost surface of the solar cell structure with CdCl₂ solution was 24.0 mAc⁻². The enhancement in the device parameters after CdCl₂ treatment led to the improvement in the solar cell efficiency reported in this work.

As reported by Olusola et al., (2016), the inclusion of excess tellurium into ZnTe semiconductors can lead to bandgap grading of the material. Ota et al. (1974) reported that semiconductor diodes made from CdS and tellurium-rich ZnTe mono crystals have rectifying diode behaviour when measured in a dark environment. The remarks given by Ota et al., (1974) was the main cause why the first batch of semiconductor diodes made from single – sided rectifying p-n heterostructures were grown with a p-type tellurium – rich ZnTe films as a partner to n-CdS films (Olusola et al., 2016). The p-type tellurium – rich ZnTe films were deposited from an aqueous acidic electrolyte which contains 0.015 molar concentration of zinc sulphate heptahydrate and 10 ml of dissolved tellurium oxide. When the tellurium – rich ZnTe was interfaced with CdS and used in devices, good diodes were produced when measured under dark. However, poor solar cell performance was observed when the diodes were measured under AM 1.5 illuminations. Due to this, 0.045 molar concentration of Zn in the electrolytic bath was employed to carry out the experimental investigations reported in this work. It should be noted that the amount

*Corresponding Author
of tellurium in the bath was not altered to enable comparison. The increment in the Zn concentration from 0.015 M to 0.045 M is in agreement with Major and Durose (2013) report that zinc rich buffer layers can be used in obtaining solar cells with improved efficiency.

In this present work, we have demonstrated the successful growth of n-CdS/p-ZnTe heterostructures. Before using the developed structures for device fabrication, the top surface of the n-CdS/p-ZnTe heterostructure was first treated with CdCl₂ solution before heat – treatment in air; this sample was labelled P10_CC. This was compared with the heterostructure annealed ordinarily in air without surface treatment and the sample was labelled P10_HT. In this work, the effects of normal CdCl₂ treatment have been investigated on the glass/FTO/n-CdS/p-ZnTe heterostructure and the results are given in this paper.

2 EXPERIMENTAL DETAILS
The p-ZnTe was electropolated on glass/FTO/CdS thin film which was chemically annealed. 0.045 M of ZnSO₄.7H₂O and 10 ml of dissolved TeO₂ were mixed together in 1000 ml of glass beaker containing 800 ml of de-ionised water to prepare the electrolytic bath for ZnTe deposition. The deposition of ZnTe thin films with p-type electrical conductivity was achieved using a cathodic potential of 1600 mV. A detailed material characterisation of ZnTe semiconductors can be found in one of our recent publications (Olusola et al., 2016). Gold contacts with thickness and diameter of ~100 nm and 3 mm respectively was evaporated on the CdS/ZnTe device structure. A computerised RERA system was used in measuring the current-voltage characteristics of the heterostructure.

3 EFFECT OF CdCl₂ TREATMENT ON p-TYPE ZnTe MONOSTRUCTURE (GLASS/FTO/ZnTe)
The effects of treating glass/FTO/ZnTe mono-structure with CdCl₂ solution have been reported in one of our previously published paper (Olusola et al., 2018). We reported that treatment with CdCl₂ does not introduce extra phase to the ZnTe layer as revealed by the XRD measurements performed on glass/FTO/p-ZnTe mono-structure. It was also reported that the electrical conductivity type remains unchanged after applying CdCl₂ treatment to the top surface of glass/FTO/p-ZnTe. Details on the structural and electrical characterisation of the ZnTe mono layers can be found in (Olusola et al., 2018).

3.1 INVESTIGATION OF ELECTRONIC PARAMETERS ACQUIRED FROM GLASS/FTO/n-CdS/p-ZnTe/Au SOLAR CELL DEVICES
To acquire parameters needed to describe the behaviour of solar cell, the cells must be measured in both dark and light conditions. Figures 1 and 2 illustrate the log-linear and linear-linear current-voltage (I-V) characteristics of the measured cells respectively. Parameters obtainable from Figure 1 are: potential barrier height (Φₜ), quality or ideality factor (n), rectification factor (RF) and reverse saturation current (Iₛ). From Figure 2, electronic parameters such as the threshold voltage (𝑉ᵣ), shunt (𝑅ₛ) and series resistance (𝑅ₑ) can be acquired. The summary of electronic parameters taken under dark condition is given in Table 1.

As revealed in Table 1, rectification factor is better in sample P10_CC than sample P10_HT. The high series resistance observed in the diodes fabricated from heat-treated (HT) and CdCl₂ (CC) treated n-Cds/p-ZnTe heterostructure is a key challenge encountered in the p-n junction diodes fabrication. However, there was a significant reduction of the series resistance value from 40.00 kΩ to ~6.60 kΩ after CdCl₂ treatment. For solar cells with optimum performance to be produced, the series resistance should be very low while the shunt resistance must be very high with values going towards infinity. Series resistances are caused by resistance due to: the interconnections, electrical contacts and bulk resistance of the material. The central effect of large series resistance is the reduction of fill factor, open circuit voltage and slope of log-linear curve at the top forward bias area. This in turn increases the value of quality factor, n and decreases the efficiency of solar cell (Dharmadasa, 2013). However, large values of 𝑅ₑ observed in sample P10_HT under dark condition can greatly decrease the 𝑁ₒ values.

![Fig. 1: Log-linear dark current-voltage characteristics of solar cell devices obtained from glass/FTO/n-CdS/p-ZnTe heterostructure treated with and without CdCl₂.](image1)

![Fig. 2: Linear-linear dark current-voltage characteristics of solar cell devices obtained from glass/FTO/n-CdS/p-ZnTe heterostructure treated with and without CdCl₂.](image2)
As reported by Rohatgi et al. (1989), heat-treated CdZnTe layers with highest series resistance have lesser contents of tellurium when compared to the Cd and Zn contents combined. The high series resistance observed in the diodes reported in this work can be ascribed to the high concentration of Zn salts that are present in the electrolytic bath. Nevertheless, it is important to have a considerable amount of Zn salts in the bath so as to realise solar cells with good photo-voltaic effect when measured under light.

This barrier of large series resistance in the midst of high Zn concentration can be introduced by introducing extrinsic dopants like sodium (Park et al., 2011) and copper (John et al., 2005) to lower the ZnTe resistivity for better cell efficiency. The absence of such dopants in the present study may be the cause of having high series resistance in the diodes notwithstanding its photovoltaic behaviour.

Significant reduction in solar cells efficiency can be caused by the presence of low \( R_{sh} \). Defects which arise from production and leakage of currents across the interface are the main causes of low \( R_{sh} \). The shunt resistance values observed in diodes with sample number P10_CC is far greater than the ones seen in sample P10_HT. The small value of \( R_{sh} \) in diode with sample number P10_HT signifies that some of the charge carriers generated via photon absorption are lost via leakage paths. This loss leads to a reduction in the solar cell short circuit current density and efficiency. (Olusola et al., 2016).

The current loss produces diode reverse saturation current (\( I_s \)). It is because of this that diodes which have low \( R_{sh} \) possess high \( I_s \) value considering the fact that low shunt resistance provides another route for photogenerated currents to flow. As given in Table 1, diode indicated as P10_HT with low \( R_{sh} \) of \(-0.2 \) MΩ has a high \( I_s \) of 56.2 nA while diode indicated as P10_CC with high \( R_{sh} \) of \(-3.7 \) MΩ has a low \( I_s \) of 0.1 nA. The obtained results reveal that treatment of the CdS/ZnTe heterostructure with CdCl\(_2\) assist in the reduction of leakage paths through which electrons and holes can pass through.

The potential barrier height is another important diode parameter which is dependent on \( I_s \). It is also a determining factor of the solar cell \( V_{oc} \) and diode turn-on voltage (\( V_t \)). The \( V_t \) differs from one material to another (Kabra et al., 2014; Olusola et al., 2014; Olusola et al., 2015), and it is the smallest voltage needed for a diode to be turned on (Sze & Ng, 2007).

The experimental results presented in this work reveal that the \( V_t \) (Table 1) and \( V_{oc} \) (Table 2) can be influenced by chemical treatment. After CdCl\(_2\) treatment, the diodes \( V_t \) change from 0.2 V to 0.7 V while the solar cell \( V_{oc} \) slightly improved from 450 mV to 480 mV. This enhancement in \( V_t \) and \( V_{oc} \) after CdCl\(_2\) treatment can be attributed to the declined value in \( I_s \) and increased \( \phi_b \) seen in sample P10_CC when compared to sample P10_HT. As reported by Jones et al., (2009) and Messina et al., (2008); decrease in open-circuit voltage can be as a result of increase in the reverse saturation current. The high values of ideality factor obtained in both diodes is an indication of the presence of interfacial charges and defects in the fabricated devices (Naby et al., 1993).

The CdS/ZnTe solar cell I-V characteristics measured under illumination is illustrated in Figure 3 while Table 2 reveals the solar cell parameters. As given in Table 1, the extreme decrease of \( R_s \) of both diodes under illumination state when compared to the dark state is an indication of the photo-conductivity of the material and enhanced photovoltaic activity of the devices.

### Table 1. Summary of diodes and solar cells parameters acquired from n-CdS/p-ZnTe combined structures under different treatment conditions.

| Treatment Status | Diode (Solar cell measured under dark) Parameters | Solar Cell Light Parameters |
|------------------|--------------------------------------------------|-----------------------------|
|                  | \( \text{Sample Name} \) | \( I_s \) (nA) | \( R_{sh} \) (MΩ) | \( \phi_b \) (eV) | \( R_{sh} \) (kΩ) | \( V_t \) (V) | \( \eta \) (%) | \( R_{oc} \) (Ω) | \( R_{sc} \) (Ω) |
| HT-treated       | P10_HT | 3.13 | 56.2 | 10\(^{10}\) >0.72 | -0.2 | 40.0 | 0.20 | 1.0 | 4053 | 1592 |
| CC-treated       | P10_CC | 2.36 | 0.1 | 10\(^{22}\) >0.89 | -3.7 | -6.6 | 0.70 | 5.3 | 4246 | 255 |

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![Fig. 3: AM 1.5 illuminated current-voltage characteristics of solar cell devices obtained from glass/FTO/n-CdS/p-ZnTe heterostructure treated with and without CdCl\(_2\).](https://example.com/fig3.png)
Generally, as seen in Tables 1 and 2, improvement was observed in the diode and solar cell parameters obtained from CdCl2 – treated CdS/ZnTe heterostructure when compared to the structure heat-treated with no treatment. The cell efficiency gotten for solar cell devices indicated as P10_HT and P10_CC are ~1.0% and 5.3% respectively.

Elimination of certain defects at the cell back contact is a probable cause for the enhanced efficiency observed in CC-treated CdS/ZnTe heterostructure. Some of the likely defects removed are tellurium (Te) precipitates (Fernández, 2003; Jayatirtha et al., 1993) and stacking faults (Abbas et al., 2013). In a similar manner, Cl diffusion from the CdCl2 solution used for surface treatment into the CdS/ZnTe junction could assist in growth of the grains and passivation of grain boundaries (Dharmadasa, 2014).

4 CONCLUSION

p-ZnTe layers have been successfully used as a hetero-partner to n-CdS window layers to fabricate solar cells with the device architecture glass/FTO/n CdS/p ZnTe/Au. The device characterisation results presented in this paper revealed that CdCl2 annealed n-Cds/p-ZnTe heterostructure possess better device quality than ordinarily heat-treated n-Cds/p-ZnTe heterostructure. The overall experimental results obtained in the CdS/ZnTe hetero-junction device structures reveal that the CdS/ZnTe heterostructure is a viable material for diode and solar cell fabrication.

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COMPETING INTERESTS

The main author has declared that no competing interests exist. This manuscript is an excerpt of the PhD thesis prepared by O. I. Olusola. The PhD thesis of O. I. Olusola was submitted to the Sheffield Hallam University library.

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