Balanced Partitioning of Several Cache-Oblivious Algorithms

Yuan Tang
School of Computer Science, School of Software
Fudan University
Shanghai, P. R. China
yuantang@fudan.edu.cn

Weiguo Gao
School of Mathematical Sciences, School of Data Science
Fudan University
Shanghai, P. R. China
wggao@fudan.edu.cn

Abstract—Frigo et al. proposed an ideal cache model and a recursive technique to design sequential cache-efficient algorithms in a cache-oblivious fashion. Ballard et al. pointed out that it is a fundamental open problem to extend the technique to an arbitrary architecture. Ballard et al. raised another open question on how to parallelize Strassen’s algorithm exactly and efficiently on an arbitrary number of processors.

We propose a novel way of partitioning a cache-oblivious algorithm to achieve perfect strong scaling on an arbitrary number, even a prime number, of processors within a certain range in a shared-memory setting. Our approach is Processor-Aware but Cache-Oblivious (PACO). We demonstrate our approach on several important cache-oblivious algorithms, including LCS, 1D, GAP, classic rectangular matrix multiplication on a semiring, and Strassen’s algorithm. We discuss how to extend our approach to a distributed-memory architecture, or even a heterogeneous computing system. Hence, our work may provide a new perspective on the fundamental open problem of extending the recursive cache-oblivious technique to an arbitrary architecture. We provide an almost exact solution to the open problem on parallelizing Strassen. All our algorithms demonstrate better scalability or better overall parallel cache complexities than the best known algorithms. Preliminary experiments justify our theoretical prediction that the PACO algorithms can outperform significantly state-of-the-art Processor-Oblivious (PO) and Processor-Aware (PA) counterparts.

I. INTRODUCTION

Frigo et al. proposed an ideal cache model and a recursive technique to design sequential cache-efficient algorithms on a hierarchical architecture of caches in a cache-oblivious fashion [11]. That is, an algorithm does not specify any parameters on cache architecture such as number of cache levels, cache size of each level, or block transfer sizes between each pair of consecutive levels, but still can attain asymptotically optimal cache complexity on all levels of cache. Ballard et al. (Sect. 6.2 of [12]) pointed out that it is a fundamental open problem to extend the technique to an arbitrary architecture.

In the literature, there are two classes of extension. One is processor-oblivious (PO) and the other is processor-aware (PA). A PO approach does not use the knowledge of processor number, cache architecture [10], [13], [14], [15], [16], [17], [18], [19], [20], or network architecture [20]. An algorithm just exploits maximal parallelism and bounds its sequential cache complexity to be optimal, then relies on a runtime scheduler or folding mechanism [20] to yield a provably efficient solution on either a shared-memory or a distributed-memory architecture. The main benefits of the PO approach are easy-of-programming, simple and scalable to an arbitrary number of processors within a certain range. However, Frigo and Strumpen [1] pointed out that the communication complexity (cache miss in a shared-memory setting, and message bandwidth and latency in a distributed-memory setting) of a PO algorithm may not be as good as its PA counterpart. Though Blelloch et al. [15] show that if a PO algorithm has a poly-logarithmic depth, i.e. low-depth, it will have low cache complexity on a shared-memory architecture, we can see from Table I that a PA counterpart can still be better.

On the other hand, a PA approach [3], [8], [21], [22], [7] utilizes the knowledge of processor number, sometimes even the knowledge of cache / memory architecture, to provide a strong scaling [23], [24] algorithm in terms of both computation and communication. However, classic PA algorithms may not utilize all processors effectively unless the processor number matches well the structure of algorithm. For example, a straightforward implementation of the Communication-Avoiding Parallel Strassen (CAPS) algorithm by Ballard et al. [8] requires processor number \( p \) to be an exact power of 7. Lipshitz et al. [9] later improved the required processor number to a multiple of 7 with no large prime factors, i.e. \( p = m \cdot 7^x \), where \( 1 \leq m < 7 \) and \( 1 \leq x \) are integer numbers, by a hybrid of Strassen and classic matrix multiplication (MM) algorithms. This hybrid algorithm may still lose up to 1/7 of the available processors, which can nullify the performance advantage of Strassen in practice. So Ballard et al. (Sect. 6.5 of [8]) raised an open question if it is possible to run Strassen’s algorithm concurrently on an arbitrary number of processors, while still attaining the computation lower bound exactly and attaining the communication lower bound up to a constant factor.

Contributions (Table I): We propose a novel way of partitioning a cache-oblivious algorithm to achieve perfect strong scaling in a shared-memory setting based on a pruned BFS traversal of the algorithm’s divide-and-conquer tree. Our
TABLE I: Main results of this paper, comparing with typical prior works. “PO”: processor-oblivious; “PA”: processor-aware; “PACO”: Processor-Aware but Cache-Oblivious. “Q_1” : optimal sequential cache complexity; “T_p, Q_p” : notations for PO algorithms; “T_p^\sum, Q_p^\sum” : notations for PA and PACO algorithms; “Z” : cache size; “L” : cache line size; “epsilon” : small constant; “omega_0 = log_2 T”.

TABLE II: Acronyms & Notations

| General Acronyms | Description |
|------------------|-------------|
| LCS              | Longest Common Subsequence |
| MM               | Matrix Multiplication |
| RWS              | Randomized Work-Stealing |
| w.h.p.           | with high probability |
| PO               | Processor-Obscure |
| PA               | Processor-Aware |
| PACO             | Processor-Aware but Cache-Oblivious |

| Parameters | Description |
|------------|-------------|
| n, m, k    | Input sizes |
| c          | small constant |
| p          | Number of processors |
| Z          | cache size |
| L          | cache line size |

Complexity Notations for PO Alg.

| Notation | Description |
|----------|-------------|
| T_p      | total work |
| T_w_c    | work along critical path (time, span, depth) |
| T_p,s    | parallel running time on p processors |
| Q_p      | sequential cache complexity |
| Q_p,c    | overall cache complexity over p processors |

Complexity Notations for PACO Alg.

| Notation | Description |
|----------|-------------|
| T_p^\sum | work over p processors |
| T_w_c    | work along critical path |
| Q_p^\sum | overall cache complexity over p processors |
| Q_p,c    | overall cache complexity along critical path |

The approach uses processor number p, but no knowledge on cache architecture, hence is Processor-Aware but Cache-Oblivious (PACO). Our PACO approach does not assume any special property of p, e.g. factorizable into two or three roughly equal numbers or does not contain large prime factors, etc. so that it works for an arbitrary p within a certain range.

We demonstrate our approach on several important cache-oblivious algorithms, including longest common subsequence (LCS) (Sect. III-B), which is Dynamic Programming (DP) with constant dependency, 1D problem (Sect. III-C) and GAP problem (Sect. III-D), both of which are DP with more-than-constant dependencies, classic rectangular Matrix Multiplication on a semiring and Strassen’s algorithm (Sect. III-F), as well as comparison based sorting. In particular, our PACO Strassen’s algorithm attains both the computation and communication lower bounds on an arbitrary number of processors in a shared-memory setting. If translated to a distributed-memory setting, our PACO STRASSEN-CONST-PIECES algorithm attains the computation lower bound up to an arbitrarily small constant factor, attains the bandwidth lower bound up to a constant factor, and has an $O(\log p)$ latency bound. We also conjecture that this latency bound is tight up to a constant factor. Hence we provide an almost exact solution to the open problem [8] on paralleling Strassen.

Compared with classic PA approaches, our algorithms achieve perfect strong scaling on an arbitrary number, even a prime number, of processors within a certain range. So we argue that our approach is as scalable as classic PO approaches. We discuss how to possibly extend our approach to a distributed-memory setting, or even a heterogeneous computing system. Hence, our work may provide a new perspective on the fundamental open problem [12] on extending the recursive cache-oblivious [11] technique to an arbitrary architecture. Compared with classic PO approaches, our algorithms usually attain a better communication complexity, no matter the best PO counterpart has a poly-logarithmic (low-depth) [15] or super-linear [24, 26, 27] critical-path length. Our work may
not only initiate new ideas on designing provably efficient runtime scheduler, but also provide a new perspective on the fundamental open problem of extending a sequential cache-oblivious algorithm to an arbitrary architecture. Preliminary experiments show that our new algorithms outperform state-of-the-art PO and PA counterparts significantly in practice.

II. MODELS

We view a parallel computation as a Directed Acyclic Graph (DAG). Each vertex stands for a piece of computation with no parallel construct and each directed edge represents some data dependency between a pair of vertices. For simplicity, we count each arithmetic operation such as multiplication, addition, and comparison uniformly as an $O(1)$ operation. Our DAG considers only data dependency because any extra control dependency is artificial dependency, which can only hurt potential parallelism \cite{28, 29}. Our computation DAG is slightly different from the CDAG of \cite{12}. In a CDAG, each vertex stands for an input / intermediate / output argument, and each edge stands for a direct dependency. The difference is due to that CDAG counts the number of edges to bound communication cost, while our DAG calculates the computation and communication complexity of each task, i.e. a subset of vertices and edges of DAG, independently.

We adopt the ideal distributed cache model (Fig. 1) proposed by Frigo and Strumpen \cite{11} as our machine model. It is a two-level memory model. There are $p$ dedicated processors with identical computing power, each of which is equipped with a private ideal cache. An ideal cache is fully associative and is managed by an omniscient, i.e. off-line optimal, cache replacement policy that replaces the cache line whose next access is the farthest in future \cite{30}. The papers of \cite{11, 31} justify the ideal cache assumption. Each private cache is of size $Z$. All caches are connected by an arbitrarily large shared memory. Private caches exchange data with shared memory atomically in cache line of size $L$. A processor can only access data in its private cache. If a value is not present in the cache, the processor incurs a cache miss to bring the data from shared memory to its cache. We do not consider cache-coherence protocols because all algorithms considered in this paper do not have data race \cite{11} nor do we consider false sharing. All private caches are non-interfering, i.e. the number of cache misses incurred by one processor can be analyzed independently of the actions of other processors in

\footnote{Data race means that there are at least two processors accessing the same location of shared memory simultaneously, at least one of which are “write.”}

III. PACO ALGORITHM DESIGN AND ANALYSIS

General PACO algorithm: Based on the observation that the maximal speedup attainable on a $p$-processor system is usually $p$-fold so that excessive parallelism may not be necessary, we have a general PACO algorithm as follows. The algorithm traverses a $c$-way divide-and-conquer tree of a cache-oblivious algorithm in a pruned breadth-first (BFS) fashion, where $c$ is a small algorithm-specific constant. That is, it unfolds the tree depth by depth in a breadth-first fashion. As soon as it figures out that some depth has equal or more than $p$ nodes that have all inputs ready and have no data dependency among each other, it cuts off (prunes) up to $(c - 1) \cdot p$ of them and assigns to $p$ processors in a round-robin fashion. The rest of nodes will stay in the tree and go to more rounds of “pruned BFS” traversal. This procedure repeats until either all nodes are pruned, i.e. assigned to processors, or all nodes are of base-case (constant) size, in which case they will be assigned to all processors in a round-robin fashion. Fig. 2 shows a pruned BFS traversal of a binary tree, assuming $p = 3$. Labels indicate assigned (pruned) order.

Invariant: Assuming that each parent node is at least a constant factor larger than each of its child node in terms of computation and communication overheads (volume, surface area, or perimeter in geometry), we can see that the set of nodes assigned to each processor forms an (almost) geometrically decreasing sequence and that the top-level node(s) dominate.

Comparison with classic PO approaches: Classic PO approach usually recursively divides each and every node to base-case size to increase the “slackness” of an algorithm so that it has better processor utilization for a wider range of processor counts. This more slackness increases the potential deviations from its sequential execution order \cite{33, 34}, hence usually incurs more communication and synchronization overheads than a PA counterpart \cite{11}.

Fig. 1: ideal distributed cache model

Fig. 2: Pruned BFS Traversal of a Binary Tree ($p = 3$); Labels indicate assigned (pruned) order.
Comparison with classic PA approaches: Classic PA approach, on the other hand, may not fully utilize all processors from beginning to end unless the processor number matches well the structure of algorithm. For example, the CAPS algorithm for Strassen [8], [9] requires processor number \( p \) to be an exact power of 7 or at least be a multiple of 7 with no large prime factors.

A. Complexity counting:

We count the complexity bounds of a PACO algorithm as follows. If there is an independent partitioning procedure ahead of real execution as in the case of LCS (Sect. III-B), we will count them separately. We assume that any processor starts a task, i.e. a set of nodes of the divide-and-conquer tree, with an empty cache and flushes all data to lower-level memory when task finishes. We use notation \( Q_p^{\Sigma} \) to denote all data movements (cache misses) between upper-level private caches and lower-level shared memory summed up over all \( p \) processors in cache line of size \( L \), and notation \( Q_p^{\max} \) to denote the maximal data movements on any single processor, or along a critical path. Similarly, we have notations \( T_p^{\Sigma} \) and \( T_p^{\max} \) for the amount of computation summed up over all \( p \) processors and the maximal on any single processor, or along a critical path, respectively.

Perfect Strong Scaling Property: We give out a more formal and more strict definition of “Perfect Strong Scaling Property”, which was initiated by Ballard et al. [23], [24], as follows.

1) Optimal balanced computation: Firstly, the overall computation complexity \( (T_p^{\Sigma}) \) should be asymptotically optimal or match that of the best sequential algorithm of the same problem. Secondly, the computation complexity on any single processor \( (T_p^{\max}) \) should be \( O((1/p) T_p^{\Sigma}) \). We make one more restriction that the amount of computation assigned to different processors can differ by no more than an asymptotically smaller term, rather than a larger-than-1 multiplicative factor.

By the restriction, we make any imbalance of workloads, if any, among different processors diminishing when increasing problem size.

2) Optimal balanced communication: Firstly, the cache misses summed up over all processors \( (Q_p^{\Sigma}) \) throughout execution should be asymptotically optimal or match that of the best sequential algorithm of the same problem. Secondly, the maximal cache misses on any single processor \( (Q_p^{\max}) \) should be \( O((1/p) Q_p^{\Sigma}) \).

Discussions: The initial notion of “perfect strong scaling” in [23], [24] requires that an algorithm attains running time on \( p \) processors which is linear in \( 1/p \), including all communication costs. Our definition is more formal and more strict in three senses: Firstly, it requires that the overall computation and communication overheads of algorithm be asymptotically optimal or match that of the best sequential algorithm of the same problem; Secondly, it requires that any load imbalance among different processors, if any, can not be more than an asymptotically smaller term, rather than a larger-than-1 multiplicative factor; Thirdly, we require that the property be valid for an arbitrary number, even a prime number, of processors within a certain range. For example, Galil and Park [3] designed a sublinear \( T_p^{\max} = O(\sqrt{n} \log n) \) time (critical-path length) and \( T_p^{\Sigma} = O(n^4) \) overall work algorithm for the GAP problem [35]. Due to the sublinear time, the algorithm is perfect strong scaling according to [23], [24]. Due to the asymptotically more work than the optimal [13], [26], it is not according to our definition.

For computation and communication overheads, we count both overall and along a critical path to compare with both PO and PA counterparts. By convention, a PO algorithm usually counts its sequential communication complexity and critical-path length, then relies on a runtime scheduler, e.g. [33], [36], or a folding mechanism, e.g. [20], to yield an overall parallel computation and communication complexity: On the other hand, a PA algorithm, e.g. [8], [9], [21], [22], [7], usually calculates overheads along a critical path.

B. PACO LCS algorithm

Given two sequences \( S = \langle s_1, s_2, \ldots, s_m \rangle \) and \( T = \langle t_1, t_2, \ldots, t_n \rangle \), the LCS problem asks to compute the length of longest common subsequence \( \mathcal{L} \) of the two inputs by the recurrence of (1) [25].

\[
X_{i,j} = \begin{cases} 
0 & \text{if } i = 0 \lor j = 0 \\
X_{i-1,j-1} + 1 & \text{if } i, j > 0 \land s_i = t_j \\
\max \{X_{i,j-1}, X_{i-1,j} \} & \text{if } i, j > 0 \land s_i \neq t_j 
\end{cases}
\]

(1)

For simplicity, we assume that the two input sequences are of the same length, i.e. \( n = m \).

Lemma 1 (25): There is a sequential algorithm CO-LCS that computes the LCS recurrences of (1) in optimal \( O(n^2) \) work, using no temporary space, and \( O(n^2/(LZ) + n/L) \) cache misses in a cache-oblivious fashion.

Referring to Fig. 3, we design a two-phase PACO LCS algorithm as follows. Firstly, a partitioning phase divide-and-assign regions to \( p \) processors evenly as follows. Initially, the entire 2D square region is marked as “unassigned”. It then repeatedly makes a 2-way division on all unassigned sub-regions. As soon as it finds some anti-diagonal, i.e. all sub-regions on the same anti-diagonal have their center coordinates \((i,j)\) satisfying that \( i+j \) are equal, contains equal or more than \( p \) sub-regions, it assigns \( p \) of them to \( p \) processors in a round-robin fashion and stops any further division on them. If the sub-regions on an anti-diagonal are of constant size, it assigns all of them to \( p \) processors in a round-robin fashion. Figure 3 is an illustrative diagram, assuming \( p = 4 \); Labels of sub-regions denote the order they get assigned. For example, label-1 sub-regions are the firstly assigned sub-regions after two rounds of 2-way division; label-2 sub-regions require one more round of 2-way division, and so on. Secondly, the algorithm executes

\[\text{The subsequence does not have to be contiguous in the input sequences.}\]

\[\text{A similar recurrence applies to the “pairwise sequence alignment with affine gap cost” problem [37].}\]
sub-regions anti-diagonal by anti-diagonal along a time line. All sub-regions on the same anti-diagonal run simultaneously. Each sub-region is executed sequentially by the best sequential cache-oblivious algorithm \( \text{COP} \) (Lemma 1). Since each sub-region only depends on two of its neighboring regions, there is no need of global synchronization between consecutive anti-diagonals. In semantics, the data dependency between sub-regions can be specified by a dataflow operator like the \( \rightsquigarrow \) operator in the Nested Dataflow Model [29].

**Theorem 2:** The PACO LCS algorithm computes the LCS recurrences of \( \text{COP} \) in optimal \( T_p^{\text{max}} = O(n^2) \) work, \( T_p^{\text{max}} = O(n^2/p) \) time, using no temporary space, \( Q_p^{\text{max}} = O(\min\{n^2/(pLZ) + (n \log(pZ))/L, (n \log n)/L\}) \), assuming \( p = o(n) \) if does not count partitioning overheads.

**Proof:**

Our performance analyses consider only the execution phase, with partitioning overheads calculated separately in Corollary 3. The work and space complexities come from the fact that this algorithm calls the sequential algorithm (Lemma 1) to compute each assigned sub-region.

**Optimal balanced computation:** Clear from the partitioning phase because in each assignment the difference in work loads among processors can not be more than an asymptotically smaller term (normal assignment) or a small constant (base-case assignment).

**Optimal balanced communication:**

**Outline:** We firstly prove that the sub-regions assigned to each processor form an almost geometrically decreasing sequence in terms of area. Since we apply the sequential cache-oblivious algorithm (Lemma 1) to compute each sub-region and the sequential cache complexity is proportional to area, top-level sub-regions thus dominate. Summing up over all sub-regions on each and every processors then yields the bounds.

**More details:** We prove by induction that the sub-regions assigned to each processor form an almost geometrically decreasing sequence in terms of area. Referring to Fig. 3 the labels 1, 2, and 3 denote the order a sub-region gets assigned. To simplify analysis, we assume without loss of generality that the the first step of partitioning makes a \( p \)-way division on the entire region. Then by a recursive \( 2 \)-way divide-and-assign, except the top-level label-1 sub-regions, if each processor has \( q \) label-\( j \) sub-regions, there will be \( 2q \) label-\( (j+1) \) sub-regions on the same processor. The total area of all label-\( j \) and label-\( (j+1) \) sub-regions on each processor sum up to \( q(n/2^n)^2 \) and \( 2q(n/2^{j+1})^2 \), respectively. In conclusion, the sum of label-\( j \) areas is a factor of 2 larger than that of label-\( (j+1) \)’s, which then forms a geometrically decreasing sequence for all \( j \in [1, \log n] \). On the other hand, we can see that the sums of half-perimeters, which stands for the space requirement of sub-regions, of consecutively labelled sub-regions are identical.

Applying the sequential algorithm of Lemma 1 to compute each assigned sub-region, assuming that \( n/p > \epsilon \), where \( \epsilon \in (0, 1) \) is some small constant, the maximal cache misses on any single processor sums up to \( Q_{1,\text{co-LCS}}(n/p) + \sum_{i=2}^{\log n} \left( 2^{i-1}(p-1)Q_{1,\text{co-LCS}}(n/(2^{i-1}p)) + \sum_{j=i+1}^{\log n} 2^{j-1}(p-1) \right) \). Note that \( Q_{1,\text{co-LCS}}(n) = O(n^2/(LZ)) \) if \( 2n > \epsilon \) and \( O(n/L) \) if \( 2n \leq \epsilon \) by Lemma 24 which explains the first equation. The switching point \( j \) comes when \( 2n/(2^n/p) \leq \epsilon \), i.e., when the input array size is less than or equal \( \epsilon \), which solves to \( j = \log_2(2n/p) \). We may see \( j = \log_2(2n/p) \) to get the final bound. To complete the calculation, if we consider the case of \( n/p \leq \epsilon \), Equation (24) will reduce to \( Q_p^{\text{max}} = O(n/(pL) + (n \log(n))/L) = O((n \log n)/L) \), for \( p \geq 1 \) and \( n \geq 2 \), because the sums of half-perimeters of

- The input array of LCS are stored in align with anti-diagonal, so its total input size is \( 2n \).
sub-regions of consecutive labels are identical. Note that in this case we have \( \log n = O(\log(pZ)) \) so that we must take a \( \min \), rather than a \( \max \), over the two cases to yield an overall bound. Since this is the analysis for any single processor, it is then clear \( Q^\sum_p = pQ^\max_p \). This finalizes the proof for optimal balanced communication.

**Corollary 3:** The partitioning overheads of PACO LCS algorithm are \( O(p^2n) \). The overheads are asymptotically smaller than the computational loads assigned to any single processor if \( p = o(n^{1/3}) \).

**Proof:** The partitioning overheads are proportional to the number of leaves of the pruned binary tree of algorithm. According to the proof of optimal balanced communication of Theorem 2 except the top-level label-1 regions, if each processor has \( q \) label-\( j \) regions, there will be \( 2q \) label-(\( j + 1 \)) regions on the same processor. So we can bound the number of total leaves by \( p[n + \sum_{j=0}^{\log_2 n} j(p-1)] = O(p^2n) \). Compared with the computational loads assigned to any processor, which is \( O(n^2/p) \), it is asymptotically smaller if \( p = o(n^{1/3}) \).

A Nested Parallel, which has a series-parallel DAG, algorithm scheduled by a Randomized Work-Stealing (RWS) scheduler such as Cilk will yield \( O(pT_{\infty}) \) steals \( \Omega \) with high probability, which are its partitioning overheads. The PO LCS algorithm \( \Omega \) will then have a partitioning overheads of \( O(pT_{\infty}) = O(pn\log_23) \), which is asymptotically larger than ours if \( p = o(n^{3−1}) = o(n^{0.58}) \). Compared with the PA LCS \( \Omega \) that has an \( O(p^2) \) overheads, our overheads are larger due to more sub-regions generated. We leave an efficient parallelization of PACO LCS algorithm’s partitioning phase to future research.

**Corollary 4:** The PACO LCS algorithm can achieve perfect strong scaling if \( n/p = \Omega(Z\log(pZ)) \), if does not count partitioning overheads.

**Proof:** The PACO LCS algorithm has memory-dependent bound of \( Q^\sum_p = O(n^2/(LZ)) + (pn\log(pZ))/L \) if \( n/p > \epsilon Z \) and memory-independent bound of \( Q^\sum_p = O((pn\log n)/L) \) if \( n/p \leq \epsilon Z \). It is then clear that perfect strong scaling comes when the memory dependent bound holds and its second term be subsumed by the first term.

**Discussions:** The classic PO and cache-efficient LCS algorithm \( \Omega, \Omega \) has a critical-path length of \( O(n^{1.5}\log 3) \), which induces a parallel cache complexity of \( Q_p = O(n^2/(LZ)) + (pn\log_3 3L)/L \) with high probability when scheduled by an RWS scheduler \( \Omega, \Omega, \Omega \). This bound is asymptotically larger than ours. Moreover, our bound is deterministic. Later Frigo and Strumpen \( \Omega \) improved the bound to \( Q_p = O(n^2/(LZ) + \sqrt{pn^{3.58}}) \) by using a concave function and Jensen’s Inequality. We can see that if \( \sqrt{p^{0.5}\log(pZ)} = o(n^{0.78}) \), which is usually true on any given machine whose \( p \) and \( Z \) are constants with respect to problem size \( n \), our bound can still be asymptotically smaller. Cole and Ramachandran \( \Omega \) later pointed out that Frigo and Strumpen’s method may omit the overheads of usurpation, i.e. synchronization at the join point of a fork-join (also known as nested parallel) algorithm. They gave a refined overall cache bound of \( O(n^2/(LZ) + \sqrt{pn^{3.58}} + pn^{1.58}) \) for finding LCS sequence, more than just the length, if approximating \( \log_23 \approx 1.58 \). On the other hand, Chowdhury and Ramachandran \( \Omega \) designed cache-efficient LCS algorithms for several different models, including D-CMP, S-CMP, and Multicore. Their D-CMP model is exactly the ideal distributed cache model \( \Omega \) adopted by our paper. Their LCS algorithm on the D-CMP model makes a \( w \)-way divide-and-assign at the top level of recursion then switches to the sequential \( 2 \)-way divide and conquer (Lemma \( \Omega \) for the rest of computation. The bound claimed in their paper considers only the case when \( n/p > \epsilon Z \). If we consider both branches, their bound will then be \( Q^\max_p = O(n^2/(pLZ)) \) and \( Q^\sum_p = O(n^2/(LZ)) \) if \( n/p > \epsilon Z \); and \( Q^\max_p = O(n/L) \) and \( Q^\sum_p = O(pm/L) \) if \( n/p \leq \epsilon Z \). If \( \epsilon Z < n/p < \epsilon Z \log(pZ) \) or if \( n/p \leq \epsilon Z \), their bound will be a logarithmic factor smaller than ours in either case; otherwise, the two bounds are identical. The difference is because their algorithm derives less number of independent sub-regions. Their algorithm’s critical-path length is \( (2p-1)n^2/p^2 + o(n^2/p^2) = 2n^2/p + o(n^2/p) \), which is larger than our \( n^2/p + o(n^2/p) \) by a small constant factor of \( 2 \). In practice, constant factor matters. Our preliminary experimental results (see our online full version) show that their algorithm’s real performance is not as good as ours.

**C. PACO 1D algorithm**

Given a real-valued function \( w(\cdot, \cdot) \), which can be computed with no memory access in \( O(1) \) time, and initial value \( D(0) \), compute

\[
D[j] = \min_{0 \leq i < j} \{ D[i] + w(i, j) \} \quad \text{for } 1 \leq j \leq n \quad (2)
\]

This problem was called the least weight subsequence (LWS) problem by Hirschberg and Larmore \( \Omega \). We will call it \( 1D \) problem following the convention of Galil and Park \( \Omega \) since it is a 1D simplification of the more complicated GAP problem (Sec. \( \Omega \)). Its applications include, but is not limited to, the optimum paragraph formation and finding a minimum height B-tree.

**Lemma 5 \( \Omega \):** There is a sequential external-updating function \( \text{co-1D}_\text{C} \) that computes a rectangular quadrant of \( 1D \) problem in optimal \( O(n^2) \) work, using no temporary space, and \( O(n^2/(LZ) + n/L) \) cache misses in a cache-oblivious fashion.

Referring to Fig. \( \Omega \) we can see that the geometric shape of total work of computing \( 1D \) problem is an equilateral right triangle (triangle in short). The output of algorithm overlaps the input and is marked by the top shaded row. The sequential algorithm \( \Omega \), as well as a straightforward cache-oblivious parallelization (COP), recursively divides the work into three or four quadrants depending on shape and schedules their execution according to the data dependencies in granularity of quadrants. For convenience, we mark the top-left quadrant of each recursion by \( (0, 0) \), top-right \( (0, 1) \), bottom-left \( (1, 0) \), and bottom-right \( (1, 1) \). A triangular quadrant is a \( 1D \) computation by only cells within the same quadrant, i.e. a self-updating function, while a squared quadrant denotes an update.
of region by cells from a disjoint quadrant, i.e. an external-updating function. The cache-oblivious (both sequential and parallel) algorithm [26] firstly invokes itself recursively on the \((0, 0)\) quadrant, then updates the output of \((0, 1)\) by the results of \((0, 0)\), finally recursively computes the \((1, 1)\), whose output overlaps that of \((0, 1)\).

Our PACO 1D algorithm only changes the partitioning and parallelization of the squared \((0, 1)\) quadrant of each recursion as follows. Initially the top-level square is associated with a list of all \(p\) processors. It then divides the square along a longer dimension into two halves by the ratio of \([p/2] : [p/2]\). In the mean time, it splits the processor list by the same ratio and hands down the resulting two lists to the two halves respectively. If a rectangle has two equal-sized dimensions, division can be on an arbitrary one to break tie. If a division is on the \(y\) axis (Fig. 4), the algorithm will allocate temporary space to break dependency since the two resulting rectangles update the same output region. In this case, the two resulting rectangles will merge the results concurrently after both of them have finished local computation. The divide-and-conquer procedure of each squared \((0, 1)\) quadrant of each recursion repeats until each derived rectangle is associated with a list of only one \((1)\) processor, specifying on which the computation of rectangle will be executed sequentially. The partitioning and parallelization of squared quadrant will apply recursively to the triangular \((0, 0)\) and \((1, 1)\) quadrants of every recursions until base cases. A base case will be executed sequentially on an arbitrary processor. Fig. 4 shows a diagram assuming \(p = 3\) and Fig. 6 is the pseudo-code. In Fig. 6 COP-1D\(\square\) denotes the self-updating function, COP-1D\(\square\) the parallel external-updating function, and CO-1D\(\square\) the sequential external-updating function.

**Theorem 6:** The PACO 1D algorithm computes the 1D recurrence of \((2)\) in optimal \(T_p^\text{max} = O(n^2/p)\) work, \(T_p^\text{max} = O(n^2/p)\) time, using \(O(p^{1/2}n \log n)\) temporary space, \(Q_p^\text{opt} = O(n/2^k) = O(n^2/p)\) \((pL \log Z)/L, (p^{1/2}n \log n)/L)\) and \(Q_p^\text{max} = O(n/2^k) = O(n^{1/2}(pLZ)/L, (n \log n)/(p^{1/2}L))\), assuming \(p = o(n)\). The perfect strong scaling range is \(n = \Omega(Z\sqrt{p}\log Z)\).

**Proof:** The work and time complexity bounds follow from that the algorithm always evenly partitions the square of each and every recursions among \(p\) processors until base cases. Chowdhury and Ramachandran [26] (Lemma 5) showed that the sequential external-updating function incurs \(O(n^2/(pLZ) + n/\log Z)\) cache misses on a square of dimensions \(n\)-by-\(n\), which indicates that the cache complexity is proportional to the area, i.e. \(O(n^2)\), if its space requirement \(2n\) is larger than cache size \(Z\), otherwise proportional to the half-perimeter, i.e. \(O(n)\). Note that the space requirement of an external-updating function is the half-perimeter of square. The width along \(x\) axis (Fig. 4) stands for the output region and the length along \(y\) axis for the input. So we just need to count the areas and half-perimeters of the rectangles assigned to each processor to bound the \(Q_p^\text{opt}\) and \(Q_p^\text{max}\). Since the partitioning always divides a rectangle with \(p'\) processors into two halves by the ratio of \([p'/2] : [p'/2]\), the area ratio of any final rectangle derived from an initial squared \((0, 1)\) quadrant is clearly \(1/p\).

Applying the conclusion recursively to all triangles of every recursions yields an \(O(n^2/p)\) total area on each processor. We take two steps to bound the half-perimeter of each rectangle as follows. First, we prove the bound by assuming that \(p\) is a power of two. Secondly, we prove that the resulting cache complexity will not differ by a small constant factor when removing the assumption. The initial half-perimeter of an \(n\)-by-\(n\) square is \(2n\), and we use notation \(S_p^+\) to denote the overall increase of half-perimeters after \([\log_2 p]\) rounds of 2-way division.

1) If \(p\) is a power of two: In this case, the algorithm cuts the initial square alternatively on the two dimensions into two equal-sized halves. So the division doubles the initial half-perimeter of \(2n\) every two rounds. That is, \(S_p^+ = \sum_{i=0}^{[\log_2 p]} p (2n \cdot 2^i) \leq 4p^{1/2}n = O(p^{1/2}n)\).

The overall half-perimeter is then \(2n + S_p^+ = O(p^{1/2}n)\) and the half-perimeter of each rectangle will be \(O(n/p^{1/2})\) because all final rectangles are of the same shape and size.

2) If \(p\) is not a power of two: This time the algorithm may cut a rectangle into two slightly unequal-sized halves. For simplicity of analysis, we assume that it follows the same partitioning order on every dimensions as in the case of rounding \(p\) up to the next power of two. We can then bound any dimension of any final rectangle to be no more than a small constant factor away from that in the case of rounding \(p\) to the next power of two. We take an arbitrary dimension of length \(n\) as an example. In the worst case, the dimension gets cut through a series of uneven right-halves (uneven left-halves are similar and symmetric) and will have size \(n, [p/2], \ldots, p/2\) \(\ldots, n\cdot \prod_{j=0}^{[\log_2 p]} \frac{2^{j+1} - 1}{2^j + 1} = \Theta(n^{1/2})\), which is asymptotically the same as cutting through a series of even divisions. The number \([\log_2 p]\) is because the algorithm cuts alternatively on the two dimensions and total rounds of cutting is \([\log_2 p]\).

The equation holds because \(\prod_{j=0}^{[\log_2 p]} \frac{2^{j+1} - 1}{2^j + 1} = \Theta(2^{-x})\) and \(\forall j \in [0, x], \frac{2^{2j+1} + 1}{2^{2j+1} + 1} \leq \frac{2^{2j+1} + 1}{2^{2j+1} + 1} \leq \frac{2^{2j+1} + 1}{2^{2j+1} + 1}, \) so \(\prod_{j=0}^{[\log_2 p]} \frac{2^{j+1} - 1}{2^j + 1} = \prod_{j=0}^{[\log_2 p]} \frac{2^{j+1} - 1}{2^j + 1} = \Theta(2^{-x/2})\), where \(x = [\log_2 p]\).

Combining the above two cases, we conclude that the area and half-perimeter of each final rectangle of the top recursion is \(O(n^2/p)\) and \(O(n/p^{1/2})\) respectively. Applying Lemma 5 will yield a cache complexity of \(O(n^2/(pLZ) + \sum (p^{1/2}L))\) for each top-level rectangle assigned to each processor. Note that when the algorithm cuts a rectangle on the \(y\) axis into two halves, it will merge the results after the two halves have finished their local computation. Since the merge is just one row of a rectangle and can be fully parallelized among the processor list of the parent rectangle as shown by lines 17–18 in Fig. 6, we can charge its overheads to the two
halves without affecting asymptotically on either computation or communication bounds. From the algorithm, we can see that going down one more level of recursion will double the number of rectangles assigned to each processor, shrinks the corresponding total area by a factor of 2, and keeps the same total half-perimeter. So if \( n > \epsilon Z \), where \( \epsilon \) is some small constant, \( Q_{p}^{max} = O((n/2)[/p(LZ)] + 2 \cdot (n/4)^2[/p(LZ)]) + \cdots + Z[L] + Z[L] + \cdots = O(n^2[/p(LZ)] + (Z \log Z)/L). \)

If \( n \leq \epsilon Z \), \( Q_{p}^{max} = O(n(2p^1/2L) + 2 \cdot (4p^1/2L)) + \cdots \) = \( O((n \log n)/(p^2/L)) \). \( Q_{p}^{max} = O(n^2[/p(LZ)] + (pZ \log Z)/L, (p^2/n \log n)/L)) \). The overall temporary space is the sum of half-perimeters over all derived rectangles, which is \( O(p^1/2n \log n) \).

The perfect strong scaling range comes when \( n > \epsilon Z \) and the second term of \( Q_{p}^{max} \), i.e. \( O(pZ \log Z/L) \) is subsumed by the first term, i.e. \( O(n^2/(LZ)) \).

Note that the partitioning overheads of PACO 1D algorithm is proportional to the number of rectangles assigned to each and every processors, so is charged to computational loads.

**Discussion:** The PO 1D algorithm developed by Chowdhury and Ramachandran [26] has a sequential cache complexity of \( O(n^2/(LZ) + n/L) \) with a depth of \( O(n \log n) \). So a straightforward scheduling by a Randomized Work-Stealing (RWS) scheduler will yield a parallel cache complexity of \( O(n^2/(LZ) + (p \log n)Z)/L \), which is asymptotically larger than our bound. Blelloch and Gu [4] improved the depth to \( O(n) \) by allocating \( O(p^2/n) \) total temporary space from an arbitrarily large system’s stack. Their algorithm’s parallel cache complexity, assuming an RWS scheduler, is \( O(n^2/(LZ) + (pZ)/L) \), which is still asymptotically larger than ours in both the case \( n > \epsilon Z \) and \( n \leq \epsilon Z \). Galil and Park [5] developed a sublinear \( O(\sqrt{n} \log n) \)-depth 1D algorithm, which requires a sub-optimal \( O(p^1/3n^{3/2}) \) total space and \( O(n^2/L) \) sequential cache complexity. This bound is the largest of all above algorithms.

**D. PACO GAP algorithm**

Given \( w, w', s_i, j \), which can be computed in \( O(1) \) time with no memory access, and \( D_{0,0} = 0 \), compute

\[
D_{i,j} = \min \left\{ \begin{array}{ll}
D_{i-1,j-1} + s_i & \text{min}_{0 \leq q < j} \{D_{i,q} + w(q,j)\} \\
D_{i-1,j} & \text{min}_{0 \leq q < i} \{D_{i,q} + w'(p,i)\}
\end{array} \right. \tag{3}
\]

for \( 0 \leq i \leq m \) and \( 0 \leq j \leq n \). We assume that \( m \) and \( n \) are equal to simplify discussion. This is the problem of computing edit distance when allowing gaps of insertions and deletions [35]. We will call it GAP problem following the convention of Galil and Park [5]. Its applications include, but is not limited to, molecular biology, geology, and speech recognition.

GAP problem is actually a 2D version of 1D problem (Sect. III-C). Similarly, the cache-oblivious algorithms, both sequential and a straightforward parallel version, designed by Chowdhury and Ramachandran [13, 25] follow a similar recursive divide-and-conquer pattern to their 1D algorithm and separate the updates to any quadrant to one self-updating function and one external-updating function. The geometric shape of the work of a self-updating function is a 3D triangular analogue, while that of an external-updating function is a 3D cube. The right part of Fig. 5 shows such a 3D triangular analogue on the top and a 3D cube at bottom.

Similar to the case in 1D, our PACO GAP algorithm only changes the partitioning of external-updating function as follows. It always partitions the work of a 3D cube of dimensions \( n \times n \times n \) into \( p \times n \times n \times n/p \) cuboids, so that each function updates a disjoint output region independently and simultaneously. The same partitioning and parallelizing pattern then applies recursively to every self-updating functions of every recursion, i.e. 3D triangular analogues, until base cases. A base case is assigned to an arbitrary processor.

**Theorem 7:** The PACO GAP algorithm computes the GAP recurrences of (3) in optimal \( O(n^2) \) work, \( O(n^3/p) \) time, using no temporary space, \( Q_{p}^{max} = O(n^3/(LZ) + (n^2 \log n)/L) \), \( Q_{p}^{max} = O(n^3/(LZ) + (n^2 \log n)/L, (n^2 \log n)/L) \) and \( Q_{p}^{max} = O(n^3/(LZ) + (n^2 \log n)/L, (n^2 \log n)/L) \), assuming \( p = o(n) \). The perfect strong scaling range is \( n = \Omega(Z \log Z) \).

**Proof:** Similar to that of Theorem 6 hence omitted.

**Discussion:** The PO GAP algorithm designed by Chowdhury and Ramachandran [26] has a sequential cache complexity of \( O(n^3/(L \sqrt{Z}) + n^2/L) \) and a depth of \( O(n^{log_{2}3}) \), using no temporary space. So scheduling by a Randomized Work-Stealing (RWS) scheduler will yield a parallel cache complexity of \( O(n^3/(L \sqrt{Z}) + n^2/L \cdot \log_{2}(Z) \cdot \log_{2}(\sqrt{Z})) \) with the same \( O(n^{log_{2}3}) \) depth by observing that one GAP algorithm’s external-updating function of dimension \( n \) can be decomposed into \( n \) independent invocations of 1D algorithm’s external-updating function, i.e. a 3D cube can be decomposed into a set of independent 2D squares, and by allocating \( O(p^{1/2}n^2) \) total temporary space from an arbitrarily large system’s stack. Their algorithm’s parallel cache complexity, assuming an RWS scheduler, is \( O(n^3/(LZ) + n^2/L \cdot \log_{2}(Z) \cdot \log_{2}(\sqrt{Z})) \), which can be slightly smaller than ours if \( p = o((n^{0.415} \log_{2}(\sqrt{Z}))/Z) \), where \( 0.415 \approx 2 - \log_{2}3 \). This is because our algorithm always partitions a 3D cube evenly and recursively until base cases so incurs deviations from the sequential execution order until base cases, while Blelloch and Gu’s counts the sequential cache misses so there is no deviation when the sum of input and output of a quadrant fits in cache. Galil and Park [5] developed a sublinear \( O(\sqrt{n} \log n) \)-depth 1D algorithm, which has a sub-optimal \( O(n^2) \) work, \( O(p^1/3n^{3}) \) temporary space, and \( O(n^2/L) \) sequential cache miss complexity. This bound is the largest of all above algorithms.

**E. PACO MM algorithm**

This section considers the general rectangular MM of multiplying an \( n \times k \) matrix \( A \) with an \( k \times m \) matrix \( B \), i.e. \( C = A \otimes B \), on a closed semi-ring \( SR = (S, \oplus, \otimes, 0, 1) \), where \( n, m, k \) are arbitrary positive integers.
PACO-MM($C, A, B, \{P\}, \text{res}_p, \text{base}$)

```text
// Compute $C = A \times B$ on processor list $\{P\}$
// initial $n\_rounds = \lfloor \log_2 \text{np} \rfloor$, $\text{res}_p = 2^{n\_rounds} - \text{np}$
// np is the number of real processors
// initial $\{P\} = \{p_0, p_1, \ldots, p_{\text{np}-1}, \ldots, p_{2^{n\_rounds}} \}$
// for proc. $p_i, 0 \leq i < \text{np}$, are real, $i \geq \text{np}$ are virtual
1 if ($|\{P\}| = 1$ and $p_i \in P < \text{np}$) or base)
   // exec seq. MM on $p_i$
2 exec($p_i$, CO-MM($C, A, B$))
   // return free processor(s) list to scheduler
3 return $\{p_i\}$
4 if $|\{P\}| = 1$
   // Adjust the processor list
5 $n\_rounds = \lfloor \log_2 (\text{np} / \text{res}_p) \rfloor$
6 // get the index of first processor of $\{P\}$
7 $i = P, \text{start}$
8 start$_i = (i - \text{np}) \cdot 2^{n\_rounds}$
9 end$_i = (i + 1 - \text{np}) \cdot 2^{n\_rounds}$
10 // re-compute $\text{res}_p$ and $\{P\}$
11 $\{P\} = \{p_{\text{start}_i}, p_{\text{end}_i}\}$
12 $\text{res}_p = \text{np} \cdot 2^{n\_rounds} - \text{np}$
// split $\{P\}$ evenly. Note that $|\{P\}| \equiv 2^x$
13 $\{\{P_1\}, \{P_2\}\} = \text{split}(\{P\})$
14 if cut on $X / X$ is the length
15 // split matrices $A$ and $C$ evenly
16 $(A_1, A_2) = \text{split}(A) ; (C_1, C_2) = \text{split}(C)$
17 base = base-size($C_1, A_1, B$) or base-size($C_2, A_2, B$)
// $\{P_1\}$ and $\{P_2\}$ are real
18 spawn
19 $\{P'_1\} = \text{PACO-MM}($$C_1, A_1, B, \{P_1\}, \text{res}_p, \text{base}$)
20 $\{P'_2\} = \text{PACO-MM}($$C_2, A_2, B, \{P_2\}, \text{res}_p, \text{base}$)
21 sync
22 $\{P^p\} = \text{merge}(\{P'_1\}, \{P'_2\})$
23 if cut on $Y / Y$ is the width
24 $(B_1, B_2) = \text{split}(B) ; (C_1, C_2) = \text{split}(C)$
25 base = base-size($C_1, A, B_1$) or base-size($C_2, A, B_2$)
26 spawn
27 $\{P'_1\} = \text{PACO-MM}($$C_1, A_1, B_1, \{P_1\}, \text{res}_p, \text{base}$)
28 $\{P'_2\} = \text{PACO-MM}($$C_2, A_2, B_2, \{P_2\}, \text{res}_p, \text{base}$)
29 sync
30 $\{P^p\} = \text{merge}(\{P'_1\}, \{P'_2\})$
31 if cut on $Z / Z$ is the height
32 $(A_1, A_2) = \text{split}(A) ; (B_1, B_2) = \text{split}(B)$
33 base = base-size($C_1, A, B_1$) or base-size($C_2, A, B_2$)
34 $D = \text{alloc(sizeof}(C))$
35 spawn
36 $\{P'_1\} = \text{PACO-MM}($$C, A_1, B_1, \{P_1\}, \text{res}_p, \text{base}$)
37 $\{P'_2\} = \text{PACO-MM}($$D, A_2, B_2, \{P_2\}, \text{res}_p, \text{base}$)
38 sync
39 $\{P^p\} = \text{merge}(\{P'_1\}, \{P'_2\})$
40 parallel for ($\{P'\}$) // Exec parallel adds on $\{P'\}$
41 $C = C + D$
42 free($D$)
43 return $\{P^p\}$
```

Fig. 8: Pseudo-code of PACO MM-1-Piece algorithm

PACO-MM-1-Piece($C, A, B, \{P\}$)

```text
// Compute $C = A \times B$ on processor list $\{P\}$
1 if $|\{P\}| = 1$
   // exec seq. MM on processor $p_i \in \{P\}$
2 $p_i \in \{P\}$
3 exec($p_i$, CO-MM($C, A, B$))
4 return
5 $|\{P_1\}| = \lfloor |\{P\}|/2 \rfloor, |\{P_2\}| = \lceil |\{P\}|/2 \rceil$
6 if cut on $X / X$ is the length
7 // split matrices $A$ and $C$ according to
8 // the ratio of $|\{P_1\}| : |\{P_2\}|$
9 $(A_1, A_2) = \text{split}(A) ; (C_1, C_2) = \text{split}(C)$
10 spawn PACO-MM-1-Piece($C_1, A_1, B, \{P_1\}$)
11 PACO-MM-1-Piece($C_2, A_2, B, \{P_2\}$)
12 sync
13 if cut on $Y / Y$ is the width
14 // split matrices $B$ and $C$ according to
15 // the ratio of $|\{P_1\}| : |\{P_2\}|$
16 $(B_1, B_2) = \text{split}(B) ; (C_1, C_2) = \text{split}(C)$
17 spawn PACO-MM-1-Piece($C_1, A, B_1, P_1$)
18 PACO-MM-1-Piece($C_2, A, B_2, P_2$)
19 sync
20 parallel for ($\{P\}$) // Exec parallel adds on $\{P\}$
21 $C = C + D$
22 free($D$)
23 return
```

Fig. 8: Pseudo-code of PACO MM-1-Piece algorithm

We can view the computation DAG of a general MM as a rectangular cuboid of size $n \times m \times k$, where the two side faces stand for the input matrices $A$ and $B$, and the bottom face stands for the output matrix $C$, respectively. To perform a given multiplication, a processor must access to the entries of $A$, $B$, and $C$, corresponding to the projections onto the $n \times k$, $k \times m$, and $n \times m$ faces of the initial cuboid, respectively.

Frigo et al. (11) proposed a sequential cache-oblivious MM algorithm by making a recursive 2-way divide-and-conquer on the longest dimension of the cuboid until base cases. So the initial cuboid is computed by a depth-first (DFS) traversal of the recursion tree.

**Lemma 8 (17):** There is a sequential algorithm CO-MM that multiplies an $n$-by-$k$ matrix with an $k$-by-$m$ matrix in optimal $O(nmk)$ work, with $Q_1 = O(1 + (nm + nk + mk) / L + nmk / (L\sqrt{Z}))$ cache misses in a cache-oblivious fashion.
By contrast, we reduce a parallel MM algorithm to a pruned breadth-first (BFS) partitioning of the initial cuboid among $p$ processors as follows. The initial cuboid is marked as “unassigned” and has output matrix $C$ as its bottom face. Then it repeatedly makes an even 2-way division on the longest dimension of all unassigned cuboids to derive twice the number of smaller cuboids depth by depth. That is, depth-0 has only one unassigned cuboid, depth-1 will have two, depth-2 will have four, and so on. If a division is on the height of a cuboid, the algorithm will allocate a temporary space of the same size as its bottom face for output of the upper cuboid. The corresponding lower cuboid reuses their parent’s bottom face for output. By allocating temporary space, all derived cuboids of the same depth can run concurrently. This stands by the observation that all multiplications are independent of each other, serialization is only necessary when combining the intermediate results by addition. As soon as some depth contains equal or more than $p$ unassigned cuboids, exact $p$ of them will be assigned to $p$ processors in a round-robin fashion. The rest of cuboids, if any, will go to the next round of division. This procedure repeats until all cuboids on the same depth are of base (constant) sizes, in which case all of them will be assigned in a round-robin fashion.

Figure 2 is an illustration of the algorithm when $p = 3$. After two rounds of 2-way division, we have four (4 > $p = 3$) depth-2 unassigned cuboids, three of which will then be assigned to $p = 3$ processors in a round-robin fashion. The algorithm then repeats the divide-and-assign on the remaining one (1) unassigned cuboid until all unassigned cuboids are of base (constant) sizes, in which case all of them will be assigned in a round-robin fashion. The following Theorem 9 bounds the algorithm’s performance.

**Theorem 9:** The PACO MM algorithm multiplies an $n$-by-$k$ matrix $A$ with an $k$-by-$m$ matrix $B$ in optimal $T_p^\Sigma = O(nmk)$ work, optimal $T_p^{\text{max}} = O(nmk/p)$ time, using $O(\min\{pmk, \sqrt{pnmk^2}, p^{1/3}(nmk)^{2/3}\})$ temporary space, $Q_p^\Sigma = O(nmk/(L\sqrt{Z})) + (nm + nk + mk + \min\{pmk, \sqrt{pnmk^2}, p^{1/3}(nmk)^{2/3}\})/L$ and $Q_p^{\text{max}} = (1/p)Q_p^\Sigma$, assuming $n \geq m \geq k$ and $p = o(n + m + k)$.

**Proof:** Optimal balanced computation: A cuboid gets assigned either because the number of unassigned cuboids of the same depth are equal or more than $p$, in which case exact $p$ of them will be assigned, or because all cuboids are of base (constant) size, in which case there will be no more than $2p$ of them and all of them will be assigned to $p$ processors in a round-robin fashion. In the first case, the difference between assigned cuboids will be no more than one face, i.e. an asymptotically smaller term, due to an even 2-way division; while in the second case, the difference between assignments will be no more than a constant.

**Optimal balanced communication:**

**Outline:** From the proof of Lemma 8 (Theorem 2.1 of [11]), the sequential cache-oblivious MM algorithm CO-MM incurs $O(nmk/(L\sqrt{Z}))$ cache misses, i.e. proportional to the volume of cuboid, if its surface area $nm + nk + nk > \epsilon Z$, and $O((nm + mk + nk)/L)$ cache misses, i.e. proportional to the surface area, otherwise, where $\epsilon \in (0, 1)$ is some small constant. We prove that for all $i \in [1, p]$, the cuboids assigned to processor-$i$ form a geometrically decreasing sequence in terms of both volume and surface area. It is then clear that the top-level, i.e. largest, cuboid on each processor dominates in either cases. Since the reduction of a pair of upper and lower cuboids derived from a cut on height by addition is asymptotically cheaper than the corresponding upper and lower cuboids’ multiplications, i.e. one face of a cuboid versus its volume, plus that the reduction by addition can be fully parallelized, we can charge all reduction overheads (work, time, caching) to all real processors that are involved in computing the upper and lower cuboid’s multiplication without affecting overall complexities asymptotically. It then boils down to bound the volume and surface area of the largest cuboid on each processor to yield the final bounds. To be convenient, we denote that the initial cuboid has volume $V = nmk$ and surface area $S = (nm + mk + nk)$ and assume without loss of generality that $n \geq m \geq k$ in the rest of proof.

**More details:** We prove that the cuboids assigned to any single processor form a geometrically decreasing sequence in terms of both volume and surface area as follows. By the 2-way divide-and-assign, as soon as some depth contains equal or more than $p$ cuboids, exactly $p$ of them will be assigned in a round-robin fashion. The number of rest unassigned cuboids, if any, will be less than $p$, and will go to more rounds of 2-way division before they can be assigned. It is clear that no processor will have more than one cuboid of the same depth, i.e. the same non-constant volume. This finalizes the proof of geometrical decrease in volume. Since the algorithm always cut a cuboid on the longest dimension into two equally sized halves, we can see that the surface area of a child cuboid is no more than $(2/3)$ of that of its parent but larger than $(1/2)$ fraction. That is, without loss of generality if we assume that a parent cuboid is $n' \times k' \times m'$ and has surface area
\(S' = (n'm' + n'k' + m'k')\), assuming \(n' \geq m' \geq k'\), we have 
\[(1/2)S' \leq ((n'/2) \cdot m' + (n'/2) \cdot k' + m' \cdot k') \leq (2/3)S'.\] 
This finalizes the proof of geometrical decrease in surface area.

We then bound the volume and surface area of the largest cuboid on each processor as follows. Each processor has its largest cuboid assigned after \([\log_2 p]\) rounds of 2-way division. Since each round decreases the volume of a cuboid by a factor of 2, it is then clear that the volume of largest cuboid on each processor is \(V/(2^{[\log_2 p]})) \in (V/(2p), V/p)\), where \(V\) is the volume of initial cuboid. To bound the surface area, we adapt the proof on communication cost of CARMA (Communication-Avoiding Recursive MAtrix Multiplication) algorithm by Demmel et al. (Sect. II C of [7]). The main difference is that their proof assumes that processor number \(p > nm/k\), whereas our algorithm and proof work for an arbitrary number of processors, even when \(p\) by itself is a large prime number. We use notation \(S_p^+\) to denote the overall increase of surface area after \([\log_2 p]\) rounds of 2-way division.

1) If \(p \leq n/m\), the 2-way division cuts only on dimension \(n\) (recall we assume \(n \geq m \geq k\)), the smallest face \(m \times k\) gets doubled on every cut.

\[S_p^+ = \sum_{i=0}^{\log_2 p-1} (m \cdot 2^i) = O(pmk) \quad (4)\]

2) If \(n/m < p \leq nm/k^2\), the division has two phases. The first phase of \(\log_2(n/m)\) rounds cut only on dimension \(n\) and increase the total surface area by \(\sum_{i=0}^{\log_2(n/m)-1} (m \cdot 2^i) = O(nk)\) and increase the number of cuboids to \(n/m\).

After the first phase, the sizes of dimension \(n\) and \(m\) of any cuboid are within a factor 2 of each other. So the second phase of \(\log_2 p - \log_2(n/m) = \log_2(pm/k)\) rounds cut into all \(n/m\) cuboids’ dimensions \(n\) and \(m\) alternatively and doubles the smallest face \(m \times k\) every two rounds.

\[S_p^+ = O(nk) + \sum_{i=0}^{\log_2(pmk/n)} ((n/m) (m \cdot 2^i)) \quad (5)\]

\[= O(nk) + O(\sqrt{pmk^2}) = O(\sqrt{pmk^2}) \quad (6)\]

In (5), the second term dominates because \(p > n/m\) in this case.

3) If \(nm/k^2 < p\), the division has three phases. The first phase cuts only on dimension \(n\) for \(\log_2(n/m)\) rounds and increase the surface area by \(O(nk)\), as well as increasing the total number of cuboids to \(n/m\). The second phase cuts on \(n/m\) cuboids’ dimension \(n\) and \(m\) alternatively for \(2 \log_2(m/k)\) rounds and increase the surface area by \(\sum_{i=0}^{\log_2(m/k)} ((n/m)(m \cdot 2^i)) = O(nm)\), as well as increasing the total number of cuboids to \(nm/k^2\).

After the second phase, all cuboids’ three dimensions are within a factor of 2 of each other. So the third phase of \(\log_2(p - \log_2(nm/k^2)) = \log_2(pk^2/(nm))\) rounds cut into all \(nm/k^2\) cuboids’ three dimensions alternatively and double the smallest face \(k \times k\) every three rounds.

\[S_p^+ = O(nm) + \sum_{i=0}^{(1/3) \log_2(pk^2/(nm))} ((nm/k^2)(k^2 \cdot 2^i)) \quad (7)\]

\[= O(nm) + O(p^{1/3}(nmk^2/3)) = O(p^{1/3}(nmk^2/3)) \quad (8)\]

In (8), the second term dominates because \(p > nm/k^2\) in this case.

Combining the three cases by taking a min, a single largest cuboid’s surface area is then \(O((1/p) \cdot (S + S_p^+)) = O((1/p) \cdot (nm + nk + k + \min\{pmk, \sqrt{pmk^2}, p^{1/3}(nmk^2/3))\})\) The temporary space complexity is then at most \(S_p^+\). This finalizes the bound on largest cuboid’s surface area. The bounds of theorem then follow.

Though PACO MM algorithm of Theorem 9 is optimal in a shared-memory setting, it can have up to \(O(\log(nmk))\) cuboids on each processor so that its latency bound in a distributed-memory setting can be large. So we simplify the algorithm to PACO MM-1-PIECE algorithm as follows. The algorithm is almost identical to PACO MM algorithm except that each time it cuts a cuboid on its longest dimension into two slightly unequal-sized halves as shown in Fig. 8. That is, if a cuboid is associated with a list of \(p\) processors, the algorithm will partition the cuboid on its longest dimension into two halves by the ratio of \([p/2] : [p/2]\). In the mean time, it splits the processor list by the same ratio. The algorithm then repeats on the left and right halves concurrently and recursively until each cuboid is associated with a list of only one (1) processor, which specifies its assignment. To simplify analyses, we assume that the partitioning on each dimension follows exactly the same order as in PACO MM algorithm. This assumption can be realized by associating the initial real cuboid with a same-sized virtual cuboid. Each time the virtual cuboid employs PACO MM algorithm to pick a dimension to cut and the real cuboid will then cut on the same dimension but into two unequal-sized halves. Corollary 10 then bounds the algorithm’s performance.

Corollary 10: The PACO MM-1-PIECE algorithm multiplies an \(n\)-by-\(k\) matrix \(A\) with an \(k\)-by-\(m\) matrix \(L\), by having only one cuboid on each processor, in optimal \(T_p^{\min} = O(nmk/p)\) time, using \(O(\min\{pmk, \sqrt{pmk^2}, p^{1/3}(nmk^2/3))\})\) temporary space, with an \(Q_p^{\min} = O(nmk/(L\sqrt{Z}) + (nm + nk + k + \min\{pmk, \sqrt{pmk^2}, p^{1/3}(nmk^2/3)))/L)\) and \(Q_p^{\max} = (1/p)Q_p^{\min}, \text{assuming } n \geq m \geq k\) and \(p = o(n + m + k)\).

Proof: Since a real and virtual cuboid always cut on the same dimension at each and every division points and the partitioning of virtual cuboid follows the same partitioning order of PACO MM algorithm for the first \([\log_2 p]\) rounds, we just need to bound any dimension of any final real cuboid to be no more than a small constant factor away from that of corresponding virtual cuboid. The volume and surface area
of any final real cuboid will then also be within a constant factor of those of corresponding virtual cuboid, i.e. the largest cuboid of PACO MM algorithm. Without loss of generality, we take dimension \( n \) as an example. In the worst case, the dimension gets cut through a series of right halves and will have size \( n \cdot \left(\frac{1}{2}\right)^{\log_2 p} \cdot \left(\frac{1}{2}\right) \cdots (2/3) = n \cdot \prod_{i=1}^{\log_2 p} \left(\left(2^i + 1\right)/(2^{i+1} + 1)\right) = \Theta(n/p) \), which is asymptotically the same as cutting through a series of equal-sized halves. Similarly, we can bound the size of a dimension that gets cut through a series of left halves. If the cuts on dimension \( n \) interleave with two other dimensions, since the real cuboid follows exactly the same division order as the virtual cuboid, the difference on any dimension after \( x \) cuts, where \( 0 \leq x \leq \log_2 p \), will not be larger than a small constant factor. This completes the proof.

**Corollary 11:** The PACO MM algorithm and PACO MM-1-PIECE algorithm achieve perfect strong scaling if \( p = O((mnk)/Z^3/2) \).

**Proof:** The perfect strong scaling range comes when the memory-independent bound of \( Q_p^\Sigma = O((nm + nk + mk + \min\{pnmk, \sqrt{pnmk^2}, \sqrt{p(2^m)^3}\})/L) \) is subsumed by the memory-dependent bound of \( Q_p = O(mnk/(LVZ)) \).

**Discussions:** A straightforward depth-\( O(n) \) MM \([25]\) has overall parallel cache misses of \( O(n^3/(LVZ) + pn(Z/L)) \) with high probability when scheduled by a Randomized Work-Steuiling (RWS) scheduler \([33], [36], [38]\). Frigo and Strumpen \([1]\) refined it to \( O(n^3/(LVZ) + p^1/3n^2/L + pn) \) by using concave function and Jensen’s Inequality. They also pointed out that a static scheduling, i.e. PA scheduling, of a square MM can yield asymptotically less cache misses. Blumofe et al. \([32]\) designed a PO MM with an \( O(2^n/3) \) critical-path length, and bounded \([38]\) its sequential cache misses to be asymptotically optimal on DAG-consistent distributed shared memory maintained by the Backer coherence protocol. Cole and Ramachandran \([2], [6]\) proved an \( O(n^3/(LVZ) + (p \log p)^{1/3} \cdot n^2/L + p \log p) \) overall parallel cache complexity for a resource-oblivious algorithm scheduled by a centralized scheduler. Chowdhury et al. \([17]\) proposed a Multicore-Oblivious (MO) algorithm on a hierarchical multi-level caching multicore (HM) model and a network-oblivious (NO) algorithm on the D-BSP model with similar bounds. Assuming \( n = m = k \), our bounds are asymptotically tighter than all above PO bounds because all PO bounds include a non-constant critical-path length in their second term, which is eliminated by our PA approach.

Classic PA algorithms include 2D \([8], [40]\), 3D \([41]\), or 2.5D \([21]\). These algorithms assume a square MM and require that processor number \( p \) be factorizable into two or three roughly equal numbers. Aggarwal et al. \([42]\) proved a lower bound as well as a matching 3D square MM algorithm on their shared-memory LPRAM model. Irony et al. \([43]\) proved a lower bound for 2D and 3D square MM algorithms on a distributed-memory model. McColl and Tiskin \([44]\) provided a similar 3D square MM algorithm on their BSPRAM model. Solomonik and Demmel \([21]\) coined a 2.5D square MM algorithm, which can change its partitioning of computational DAG as well as processor grid according to the availability of memory to achieve optimal communication complexity on a distributed-memory model. Demmel et al. \([27]\) proved the lower bound as well as the first communication-optimal algorithm for all dimensions of rectangular MM. Their proof assumes that processor number \( p \) is an exact power of 2 and their algorithm is efficient by the proof if all prime factors of \( p \) can be bounded by a small constant. By contrast, our algorithm and proof work for an arbitrary number of processors, even when \( p \) per se is a large prime number. Our algorithm matches the lower bound proved in \([27]\).

1) **Extension to a Distributed-Memory Computing System:** One of the reasons that we choose a PA approach is that PA algorithms are more portable to both shared-memory and distributed-memory computing systems. Though Network-Oblivious (NO) algorithms by Bilardi et al. \([20]\) and Chowdhury et al. \([17]\) are efficient on the D-BSP model, provided there is a provably efficient folding mechanism. Such a folding mechanism is not available in practice. There are at least two ways to port a PACO algorithm to a distributed-memory computing system as follows.

1) If assuming that each processor has an arbitrarily large local disk besides a local memory of size \( Z \) a PACO algorithm’s communication can be separated into two phases. The first phase will be an inter-processor message passing, the bandwidth of which will be the memory-independent communication bound proved for a PACO algorithm. In the case of PACO MM-1-PIECE algorithm, the latency bound will be \( O(\log p) \). For each cuboid, the read of two side faces, i.e. sub-matrices of \( A \) and \( B \) requires only \( O(1) \) messages by a proper packing / unpacking. The \( O(\log p) \) latency comes from writing intermediate results back to \( C \) because in the worst case all cuts are on the height of initial cuboid, hence requires \( O(\log p) \) rounds for reduction.

2) The second phase will be a local sequential computation, which will incur only sequential cache misses between local memory / disk pair. The local bandwidth of this phase will be the memory-dependent or memory-independent bound of each PACO algorithm, depending on the relative size of surface area of cuboid with respect to the local memory size \( Z \).

2) If assuming a distributed-memory model as in \([27]\), i.e. each processor has only one local memory of size \( Z \) with no local disk, then the bandwidth bound will still be the same as the communication bound proved for each PACO algorithm. Take the PACO MM-1-PIECE algorithm as an example, the latency bound will be a

5 This assumption can be valid by the virtual memory (VM) system (Chap. 9 of [45]). A user’s program can only access VM, which usually resides on a local disk. VM system will bring data to physical memory when user accesses it. A 32-bit system usually has a \( 2^{40} \)-byte VM, while a 64-bit system usually has a VM of size \( 2^{64} \) or \( 2^{48} \) bytes, all of which are usually much larger than corresponding physical memory size.
factor of \( Z \) lower than the bandwidth bound as follows. The number of messages to compute a cuboid will be \( \min(V'/V_Z) \cdot \log p \), where \( V' \) is the volume of cuboid, which is \( O(nmk/p) \), and \( V_Z \) is the largest volume of a cuboid that has an \( O(Z) \) surface area, which stands for the largest amount of multiplications that can be done by having \( O(Z) \) elements. So \( \min(V'/V_Z) \) accounts for the minimal number of messages for reading sub-matrices of \( A \) and \( B \), and \( \log p \) is for writing back to \( C \). According to Loomis-Whitney Inequality [7], [46], the largest volume that a cuboid with a surface area of \( O(Z) \) can have is \( O(Z^{3/2}) \), i.e., when the cuboid is a cube. So the number of messages reduce to \( O(nmk/(pZ^{3/2}) \cdot \log p) \). The latency bound of CARMA [7] is different from this bound because they assume matrices \( A \), \( B \), and \( C \) are stored distributedly among \( p \) processors’ memory, hence not every intermediate results have to be written back to \( C \).

2) Extension to Heterogeneous Computing System: The heterogeneous computing system considered in this section makes following modifications to the ideal distributed cache model. It has \( p \) processors, each of which can have a different but fixed throughput. In the case of MM, it means that if we execute the same-sized MM sequentially on every computing cores, the throughput, say FLOPS (Floating Point Operations Per Second), of all cores can be normalized to \( t_1 : t_2 : \cdots : t_p \). For simplicity, we assume that this throughput ratio is fixed and does not change on different problem sizes. Without loss of generality, we assume that the throughput ratio is in a monotonically non-decreasing order. That is, \( t_i = 1, \forall i, j \in [1, p] \), we have \( t_i \leq t_j \) if \( i \leq j \), where \( t_i, t_j \geq 1 \) are arbitrary real numbers.

We construct our PACO HETERO-MM algorithm based on the 2-way divide-and-conquer procedure of PACO MM algorithm as follows. The intuition is to assign cuboids to processors proportional to their throughput ratio, plus that all cuboids assigned to any processor still keep a geometrically decreasing sequence in terms of both volume and surface area. Firstly, we normalize the throughput ratio to fraction ratio of \( f_1 : f_2 : \cdots : f_p \), where \( f_i = t_i \sum_{j=1}^{p} t_j \). Each fraction number \( f_i \), where \( i \in [1, p] \), indicates the fraction of total computational loads to be assigned to processor-\( i \). Secondly, we still perform a similar recursive 2-way divide-and-conquer procedure to that of PACO MM algorithm. In addition, we associate each cuboid with a real number to indicate its fraction of total computational loads. For example, the initial cuboid of \( n \times m \times k \) will have a fraction number 1, a cuboid of \( n' \times m' \times k' \) will have a fraction number of \( f' = \frac{n'm'k'}{nmk} \), and so on. Thirdly, in the recursive 2-way divide-and-conquer, whenever a cuboid’s fraction number \( f' \) is less than or equal to some processor’s remaining ratio \( f_i \), we make an assignment and adjust the processor’s remaining ratio by \( f' \), i.e., \( f_i = f_i - f' \). This recursive procedure repeats until all remaining cuboids are of constant sizes, in which case they will be assigned to all processors in a round-robin fashion.

By the modification, it’s not hard to check that the amount of computation and communication assigned to every processors should be proportional to their throughput ratio, hence the running time on every processors are identical. As a consequence, the algorithm will reach an ideal speedup.

**Corollary 12:** The PACO HETERO-MM algorithm multiplies an \( n \)-by-\( k \) matrix \( A \) with an \( k \)-by-\( m \) matrix \( B \) on a heterogeneous computing system with \( p \) processors of throughput ratio \( t_1 : t_2 : \cdots : t_p \), where \( t_1 = 1 \) and \( t_i \geq t_1 \), for \( 1 \leq i \leq p \). In optimal \( \mathcal{T}_{\Sigma} = O(nmk) \) work, with an \( O(\ell \Sigma) \) speedup with respect to a sequential execution on processor-1, where \( \ell \Sigma = \sum_{j=1}^{p} t_j \).

**Discussions:** Our model for heterogeneous computing systems is simpler than that in Ballard et al. [47]. Their model considers four parameters, i.e. \( \beta_i \) (inverse bandwidth), \( \alpha_i \) (latency), \( M_i \) (local memory size), and \( \gamma_i \) (flops per second), for \( 1 \leq i \leq p \). We simplify it to just throughput ratio because we feel that the parameters \( \alpha_i \), \( \beta_i \), and \( \gamma_i \) are closely related in any real system and are usually proportional to each other in an algorithm’s complexity bound. They develop a heterogenous algorithm for square MM, and our PACO HETERO-MM algorithm works for a rectangular MM of all dimensions. The same scheme extends to heterogeneous Strassen as well.

Beaumont et al. [48], [49] proposed 2D and 3D approximate algorithms for partitioning square MM on a heterogeneous computing system, with a proof that an exact partitioning is NP-Complete. Their method is Non-Rectangular Partitioning and has a better approximate ratio than the Rectangular Partitioning proposed by Nagamochi and Abe [50].

**F. PACO Strassen’s algorithm**

Assuming the existence of an inverse operation of addition, Strassen’s algorithm [51] is a 2-way divide-and-conquer algorithm that recursively reduces 1 multiplication of two \( n \)-by-\( n \) matrices to 7 multiplications of two \( n/2 \)-by-\( n/2 \) matrices plus a constant number of matrix additions and subtractions on a ring as follows.

\[
C = \begin{bmatrix} C_{00} & C_{01} \\ C_{10} & C_{11} \end{bmatrix}, A = \begin{bmatrix} A_{00} & A_{01} \\ A_{10} & A_{11} \end{bmatrix}, B = \begin{bmatrix} B_{00} & B_{01} \\ B_{10} & B_{11} \end{bmatrix}
\]

\[
S_1 = A_{00} \oplus A_{11}, S_2 = A_{10} \oplus A_{11}, S_3 = A_{00}, S_4 = A_{11}, S_5 = A_{00} \oplus A_{01}, S_6 = A_{10} \oplus A_{00},
\]

\[
S_7 = A_{01} \oplus A_{11}, T_1 = B_{00} \oplus B_{11}, T_2 = B_{00}, T_3 = B_{01} \oplus B_{11}, T_4 = B_{10} \oplus B_{00}, T_5 = B_{11},
\]

\[
T_6 = B_{00} \oplus B_{01}, T_7 = B_{10} \oplus B_{11}, M_r = S_r \oplus T_r, 1 \leq r \leq 7
\]

\[
C_{00} = M_1 \oplus M_4 \oplus M_5 \oplus M_7, C_{01} = M_3 \oplus M_5, C_{10} = M_2 \oplus M_4, C_{11} = M_1 \oplus M_2 \oplus M_3 \oplus M_6
\]

We can view the computation of Strassen’s algorithm as a cube of dimensions \( n \)-by-\( n \)-by-\( n \), where the two side faces stand for the input matrices \( A \) and \( B \), and the bottom face stands for the output matrix \( C \), respectively. Our PACO STRASSEN’S algorithm is then a pruned BFS traversal of a 7-way divide-and-conquer tree as follows. Each node of tree stands for a matrix multiplication, which is also called a cube in our description, and the seven children nodes of it are the seven (7) derived smaller-scale cubes. All intermediate matrices, i.e. \( S, T, \) and \( M \), are held in temporary space so that
all derived nodes of the same depth can run concurrently. As soon as some depth contains equal or more than \( p \) unassigned nodes, exact \( p \) of them will be pruned and assigned to \( p \) processors in a round-robin fashion. The rest of nodes, if any, will go to the next round of division. This procedure repeats until all nodes on the same depth are of base (constant) sizes, in which case all of them will be pruned and assigned in a round-robin fashion. An assigned node stops any further parallel divide-and-conquer and will be executed by the cache-oblivious sequential Strassen’s algorithm \([11]\) on the assigned processor. The entire procedure is similar to that shown in Fig. 2 except that it is now a 7-ry tree.

**Theorem 13:** The PACO STRASSEN’s algorithm multiplies two \( n \)-by-\( n \) matrices in optimal \( T_p^\sum = O(n^{\omega_0}) \) work, optimal \( T_p^{\max} = O(n^{\omega_0}/p) \) time, using \( O(p^{0.29}n^2) \) temporary space, \( Q_p^\sum = O(n^{\omega_0}/(LZ^{\omega_0/2} + n^2/(L^3/\omega_0 - 1))) \), and \( Q_p^{\max} = (1/p)Q_p^\sum \), where \( \omega_0 = \log_2 7 \) and \( 0.29 \approx 1 - \log_7 4 \), assuming \( p = o(n) \). The perfect strong scaling range is \( n = \Omega(Z) \).

**Proof:** The conclusion of optimal balanced computation is clear from the algorithm, and the property of optimal balanced communication follows by showing that the sequence of cubes, i.e. multiplications, assigned to each processor forms an almost geometrically decreasing sequence in terms of volume, i.e. \( O(n^{\omega_0}) \), and surface area, i.e. \( O(n^2) \), up to a constant factor of 6, and that the cache complexity of cache-oblivious sequential Strassen’s algorithm \([11]\) is proportional to the volume when the sizes of input and output, i.e. \( 3n^2 \), is larger than the cache size \( Z \), and proportional to the surface area otherwise. So the overheads of top-level nodes dominate on each processor. The overheads of constant number of matrix additions and subtractions of each node can be charged to corresponding multiplications. The temporary space before the first assignment of \( p \) nodes is \( 3 \cdot 7 \cdot n^2 \cdot \sum_{i=0}^{\log_7 p} (7/2)^2 = O(p\log_7(7/4)/n^2) \approx O(p^{0.29}n^2) \), where \( 3 \cdot 7 \cdot n^2 \) is the temporary space for top-level recursion (to hold \( S, T \), and \( M \)) and the \( \sum \) is to accumulate over \( \log_7 p \) recursion levels before the first assignment. Since it is pruned BFS traversal, later space requirement after the first assignment will be dominated. The perfect strong scaling range comes when the memory-dependent bound dominates.

From PACO STRASSEN’s algorithm, we can see that after first \( i_1 = \lceil \log_7 p \rceil \) rounds of 7-way branching, each processor will be assigned up to 6 same-sized cubes, and will get the next assignment after another \( i_2 - i_1 = \lceil \log_7 (p/(7^{\lceil \log_7 p \rceil} - p)) \rceil \) rounds of 7-way branching, and so on. If we denote the number of rounds that yields the \( j \)-th assignment by \( i_j \), which we call \( j \)-th super-round, we make the following changes. The new algorithm will stop parallel divide-and-conquer after \( \gamma \) super-rounds, where \( \gamma \) is some constant to be determined later. If there are still unassigned cubes, the algorithm assigns all of them to \( p \) processors in a round-robin fashion. Ignoring constant, the maximal possible difference in computational loads among different processors is

\[
\sum_{j=1}^{\lfloor \log_7 (n/2^j) \rfloor} (n/2^j)^{-\omega_0} - \sum_{j=1}^{\lfloor \log_7 (n/2^j) \rfloor} (n/2^j)^{-\omega_0} = \sum_{j=1}^{\lfloor \log_7 (n/2^j) \rfloor} (n/2^j)^{-\omega_0} + (n/2^j)^{-\omega_0} \leq 1 - \frac{(n/2^j)^{-\omega_0}}{(n/2^j)^{-\omega_0}} = 1 - \frac{(n/2^j)^{-\omega_0}}{(n/2^j)^{-\omega_0}} \leq 1 - \frac{2^{\gamma - 1}}{2^{\gamma - 1 + 1}}.
\]

The last inequality is because each super-round contains at least one round of 7-way branching. We can see that \( f_{\text{comp}} \) can be made arbitrarily close to 0 with the increase of \( \gamma \). A similar conclusion applies to difference in cache complexity as well. Note that \( \gamma \) depends on processor number \( p \), but is independent of problem size \( n \). These changes make our improved PACO STRASSEN-CONST-Pieces algorithm (Corollary [14]).

**Corollary 14:** The PACO STRASSEN-CONST-Pieces algorithm multiplies two \( n \)-by-\( n \) matrices by having only constant pieces of cubes on each processor, in optimal \( O(n^{\omega_0}) \) work, optimal \( O(n^{\omega_0}/p) \) time, using \( O(p^{0.29}n^2) \) temporary space, \( Q_p^\sum = O(n^{\omega_0}/(LZ^{\omega_0/2} + n^2/p^{2}/\omega_0 - 1)) \), and \( Q_p^{\max} = (1/p)Q_p^\sum \), where \( \omega_0 = \log_2 7 \) and \( 0.29 \approx 1 - \log_7 4 \), assuming \( p = o(n) \).

In practice, we can make \( \gamma \) a tuning parameter. For example, if \( \gamma = 8 \), the load imbalance among different processors, if any, will be less than 1%.

**Discussions:**

The load imbalance of PACO STRASSEN’s algorithm among different processors is an asymptotically smaller term, if any, so is optimal in a shared-memory setting; However, if translated to a distributed-memory setting, they may have an \( O(\log n) \) latency bound; By contrast, PACO STRASSEN-CONST-Pieces algorithm may have an arbitrarily small constant-factor difference, but reduces latency to \( O(\log p) \) in a distributed-memory setting. The partitioning overheads of both our new Strassen’s algorithms can be fully parallelized and charged to each and every derived cubes as in the case of PACO 1D algorithm (see Fig. 6 for an analogue).

**Open Problem on Parallelizing Strassen:** Ballard et al. \([8]\) developed a CAPS (Communication-Avoiding Parallel Strassen) algorithm based on interleaving of BFS/DFS steps on a distributed-memory model. Their algorithm assumes that processor number \( p \) is an exact power of 7. Lipshitz et al. \([9]\) later improved it to a multiple of 7 with no large prime factors, i.e. \( p = m \cdot 7^k \), where \( 1 \leq m < 7 \) and \( 1 \leq k \) are integers, by a hybrid of Strassen and classic \( O(n^3) \) MM algorithm. They raised an open question in their paper (Sect. 6.5 of \([8]\)) whether a parallel Strassen’s algorithm can run on an arbitrary number of processors, attains the computational lower bound exactly, and attains the communicational lower bound up to a constant factor.

If translated to a distributed-memory model, our PACO STRASSEN-CONST-Pieces algorithm is an almost exact solution to their open question, i.e. it runs concurrently on an arbitrary number of processors within a certain range, attains computational lower bound up to an arbitrarily small constant factor, attains bandwidth lower bound up to a constant factor, and attains the same \( O(\log p) \) latency bound as the CAPS algorithm. Moreover, our PACO STRASSEN-CONST-Pieces algorithm is pure Strassen. We further conjecture that this \( O(\log p) \) latency bound is tight up to a constant factor. Because in Strassen, each internal node of the 7-ry tree requires additional matrix additions and subtractions to construct new
input matrices to the next level of recursion so that an $O(1)$ message(s) per node along a critical path seems inevitable. A parallel Strassen requires at least an $\Omega(\log p)$ depth to derive $\Omega(p)$ cubes of multiplications. So the $O(\log p)$ latency bound should be tight up to a constant factor.

**More Related Works on Parallel Strassen:** McColl and Tiskin [44] developed a similar algorithm to the CAPS [8], [9] on their BSPRAM model. McColl and Tiskin’s algorithm is pure theoretical and ignores certain practical considerations such as what if $p$ is not a power of 7. Cole and Ramachandran [2], [6] bounded the overall parallel cache complexity of a resource-oblivious Strassen, which belongs to the PO class, to be $O(n^{\frac{20}{3}} + (p \log p)^{1/3} \cdot n^2/L + p \log p)$, which is asymptotically larger than all PA (including PACO) counterparts. Benson and Ballard [52] developed a code generation tool to automatically implement multiple sequential and shared-memory parallel variants of fast MM algorithms.

**G. PACO SORT algorithm**

This section considers comparison-based sorting (sorting in short) algorithm.

**Lemma 15 ([11]):** There is a SEQ-SAMPLE-SORT algorithm that sorts $n$ elements by comparison in optimal $O(n \log n)$ work, and $O((1 + (n/L)(1 + \log Z n))$ cache misses.

Based on the sequential sample sort [11] and the observation that the maximal speedup a parallel algorithm can attain on a $p$-processor system is $p$-fold if does not count the caching effect, we have a PACO SORT algorithm operating on an array $A$ (stored in contiguous locations) of length $n$ as follows. We discuss the differences of our algorithms from classic ones by the end of section.

1) Picking $p - 1$ pivots ($p_1, p_2, \ldots, p_{p-1}$) uniformly at random from the array as follows:

a) Pick $kp$ samples uniformly at random from the array, where $k$ is an over-sampling ratio to be determined later.

b) Sort the $kp$ samples with the SEQ-SAMPLE-SORT (Lemma [15]).

c) Pick every $k$-th sample as the final pivots.

2) Redistributing elements of array $A$ by the $p - 1$ pivots as follows.

a) Each processor works simultaneously on a sub-array of length $n/p + 1$ of $A$ and partitions it into $p$ partially ordered chunks by the $p - 1$ pivots. That is, after the partitioning, all elements of the $i$-th chunk on any processor must be between the $(i-1)$-th and the $i$-th pivots in sorted order, $\forall i \in [1, p]$. The $0$-th and $p$-th pivots are defined to be $-\infty$ and $+\infty$ respectively.

   This step can actually be performed by using a partial sequential quicksort [53] as follows. Any processor $i$ firstly partitions the $i$-th sub-array by the $[p/2]$-th pivot into two chunks such that all elements in the first chunk are less than or equal all elements in the second chunk. Then, each processor uses the $[p/4]$-th and $[3p/4]$-th pivots on the first and second chunk, respectively, and so on for up to $\lceil \log_2 p \rceil$ levels of recursion.

b) Calculating the exact position of every chunk for re-distribution as follows. After the first step, we have a $p$-by-$p$ matrix $[N]$, where each entry $n_{i,j}$ stands for the number of elements of the $j$-th chunk on processor-$i$, which will be re-distributed to processor-$j$. By invoking a sequential prefix sum algorithm on every column of the matrix $[N]$ simultaneously, we get each chunk’s destined position for re-distribution.

c) Performing a parallel matrix transposition like the one in Blelloch et al. [15], [54] to redistribute every chunk. That is, every processor will send $(2 - 1)$ chunks to other $(p-1)$ processors by an all-to-all communication.

3) Sorting locally, i.e. sequentially, on each processor by the SEQ-SAMPLE-SORT (Lemma [15]).

**Theorem 16:** The PACO SORT algorithm sorts an array of $n$ elements by comparison in optimal $T_{p} = O(n \log n)$ work, $T_{p}^{\max} = O((1 + (1 + \epsilon)n/p \cdot \log n)$ for an arbitrarily small $\epsilon \in (0, 1)$ with high probability, using $O(p^2)$ temporary space, $Q_{p} = O((n/L) \log Z(n/p))$, and $Q_{p}^{\max} = (1/p)Q_{p} = O((n/pL) \log Z(n/p))$, assuming $p \in O(\sqrt{n/\ln n})$.

**Proof:** Optimal balanced computation: By choosing an appropriate over-sampling ratio $k > \frac{2(e+1)}{\ln n} \ln n$, where $c > 1$ and $0 < \epsilon < 1$ are some small constants, we can prove that the number of elements on each processor after re-distribution is no more than $(1 + \epsilon)n/p$ with probability $1 - n^{-c}$, i.e. with high probability. The following proof adapts mostly from that of Theorem B.4. of [54]. If we look at any particular element $i$ and its distance $I$ to the next pivot in sorted order. If $I \geq (1 + \epsilon)n/p$ elements, where $0 < \epsilon < 1$ is some small constant, there must be fewer than $k$ samples selected from these $(1 + \epsilon)n/p$ elements in sorted order. That is, $Pr[I \geq (1 + \epsilon)n/p] \leq Pr[Y_i < k]$, where $Pr$ denotes the probability of some event and $Y_i$ denotes the number of samples picked from these $(1 + \epsilon)n/p$ elements. Since the algorithm samples uniformly at random, each element has the same probability of $(kp/n)$ to be chosen. By lower-tail Chernoff bound, $Pr[Y_i < k] = Pr[Y_i \leq (1 - \delta)\mu] \leq e^{-\delta^2/2}$, where $\mu = (1 + \epsilon)k$ is the expected number of samples from $(1 + \epsilon)n/p$ elements and $\delta = (\epsilon/(e + 1), 1)$ is a small variable to make the first equation of $Pr[Y_i < k] = Pr[Y_i \leq (1 - \delta)\mu]$ holds. Since this is the upper bound for any single element to be within a balanced chunk. For all elements to be within a balanced chunk, the probability is then no more than $n e^{-\delta^2/2}$. To have a high probability bound, we make $n e^{-\delta^2/2} \leq n^{-c}$, where $c \geq 1$ is some constant. Solving the inequality, we have the over-sampling ratio of $k \geq \frac{2(e+1)}{\ln n} \ln n/(1 + (1 + \epsilon)\delta^2) > \frac{2(e+1)}{\ln n} \ln n$. Since $c \geq 1$ and $0 < \epsilon < 1$ are some small constants, we conclude that $k \in O(\ln n)$.

The overall work of this algorithm sums up to the optimal $O(kp \log kp) + O(n \log p) + O(p^2) + O(n) + O(n \log (n/p)) = O(n \log n)$, where $k = O(\log n)$ and assuming $p \in O(\sqrt{n})$. In the equation, $O(kp \log kp)$ is the work for sorting samples, $O(n \log p)$ is the work of using $(p - 1)$ pivots to partition the
array, $O(p^2)$ is the work of prefix sum on $[N]$, $O(n)$ is the work for redistribution, and $O(n \log(n/p))$ is the overall work of final sequential sorting on every processors.

The time complexity is $O(kp \log kp) + O(n/p \log p) + O(p) + O((1 + \epsilon) n/p \cdot \log n) = O((1 + \epsilon) n/p \log n)$ for any arbitrarily small constant $0 < \epsilon < 1$ with high probability. The $O(p^2)$ temporary space is used for storing matrix $[N]$ and computing the prefix sums.

**Optimal balanced communication:**

1) The parallel cache complexity of selecting pivots and using the pivots to partition each sub-array of $n/p$ elements into $p$ chunks is $O((kp/L) \log_M(kp) + (n/(pL)) \log_Z(p))$ along the critical path and $O((kp/L) \log_M(kp) + (n/L) \log_Z(p))$ in summation.

2) The parallel cache complexity of prefix sum and redistribution is $O(n/(pL) + p)$ along the critical path and $O(n/L + O(p))$ in summation.

3) The parallel cache complexity of the final sequential sorting on each processor is $O((n/pL) \log_Z(n/p))$ along the critical path and $O((n/L) \log_M(n/p))$ in summation.

Summing up over all above overheads, we have the final parallel cache complexity of $O^\text{max} = O((n/(pL)) \log_Z(n/p))$ along the critical path and $O^p = O((n/L) \log_Z(n/p))$ in summation, assuming $p \in O(\sqrt{n} / \ln n)$.

Note that the overall parallel cache complexity ($O^p$) of PACO SORT algorithm is actually smaller than the best sequential cache bound of SEQ-SAMPLE-SORT (Lemma 15) because we have $p$ caches in the parallel setting and all procedures of sampling, partitioning and sequential sorting after re-distribution are concurrent on $p$ caches.

**Discussions:** Our algorithm is a variant of parallel sample sorting algorithm. Parallel sample sorting algorithm has been studied in both PA [54] and PO fashions [15]. Cole and Ramachandran [10] developed a resource-oblivious, which also belongs to the PO class, sorting which interleaves the partitioning of a sample sort with merging, hence has only an $O(\log n \log \log n)$ critical-path length.

There are several key differences of our algorithm from the PO algorithm in [15]. Firstly, we use $(p - 1)$ pivots instead of $O(\sqrt{n})$ pivots. Secondly, we call the sequential sample sort (Lemma 15) to sort on each processor after re-distribution, rather than a recursive low-depth one. As a consequence, all PO algorithms [10, 15] incur more cache misses than the best sequential cache bound, though they all have a poly-logarithmic, i.e. low-depth critical-path length. By contrast, our PACO SORT algorithm incurs less. As we can see from the experimental data in Sect. IV, our algorithm does outperform the PO counterpart implemented in PBBS [55] significantly.

The main difference of our algorithm from the PA version in [54] is that the early distributed-memory version calls a standard sequential radix sort after re-distribution for an empirical efficiency, while we call the sequential sample sort (Lemma 15) for an emphasis on optimal balanced communication. Putze et al. [56]’s MCSTL utilizes atomic operations for an in-place parallel quicksort with dynamic load-balance.

**IV. PRELIMINARY EXPERIMENTAL RESULTS**

We implement our PACO algorithms and compare them on a 72-core machine and a 24-core machine (Table III).

| Name                  | 72-core machine | 24-core machine |
|-----------------------|-----------------|-----------------|
| OS                    | CentOS 7.1 x86_64 | CentOS 7 x86_64 |
| CPU                   | Intel Xeon      | Intel Xeon      |
| # cores / socket      | 18              | 12              |
| Dual Precision        | 16              | 16              |
| FLOPs / cycle         | 37 KB           | 32 KB           |
| # dcache / core       | 256 KB          | 256 KB          |
| # cache / core        | 44 MB           | 36 MB           |
| Memory                | 128 GB          | 152 GB          |

**TABLE III: Experimental Machines**

**Overview of Performance Comparison:** Since the focus of this paper is to provide a new partitioning and scheduling mechanism of cache-oblivious algorithm, we request that all algorithms of the same problem call the same kernel function(s) to compute sequentially base cases. For example, when comparing PACO MM algorithm with Intel MKL or PO counterpart, we call MKL’s sequential dgemm and daxpy subroutines for base-case matrix multiplications and additions, respectively. By this way, the only difference between peer algorithms is how they partition and schedule tasks. We include all partitioning and scheduling overheads in final running time. To avoid averaging noise, we measure “running time” as a min of at least three independent runs. We calculate speedup by “(running time peer alg. / running time PACO) − 1) × 100%”.

**A. MM**

| Rmax/Rpeak | PACO | MKL | CO2 |
|------------|------|-----|-----|
| Mean       | 82.6%| 75.1%| 37.8%|
| Median     | 84.0%| 78.4%| 39.3%|

**TABLE IV: Rmax/Rpeak of MM algorithms. “CO2” is the PO depth-α MM algorithm based on 2-way divide-and-conquer with a base-case size of 64 [1]. “Mean” and “Median” is the mean and median Rmax/Rpeak of all data.**

We firstly compare PACO MM-1-PIECE algorithm (Corollary 10) with Intel MKL’s parallel dgemm on the 72-core machine. Figure 7A shows speedup distribution along problem sizes. Problem size is calculated as $n \times m \times k$ for an $n$-by-$k$ matrix multiplying an $k$-by-$m$ matrix, where $n, m, k$ iterate independently from 8,000 to 44,000 with a step size 4,000. So there are multiple points of the same $x$-value. From the
Fig. 9: Speedup of PACO MM-1-Piece algorithm over Intel MKL’s dgemm on 72-core machine.

Fig. 10: Performance of PACO MM-1-Piece algorithm on 24-core machine.

figures, though PACO MM-1-Piece algorithm outperforms MKL in majority of cases, the mean and median of speedup is just 3.4% and 3.5%, respectively. Figure ?? shows that this 72-core machine has 4 sockets, each of which has 18 cores. Profiling shows that the 18 cores on 0-th socket are actually 3 times faster than the other 54 cores on other 3 sockets, though all these cores have the same clock frequency and cache parameters. By 3 times faster, we mean that the 18 cores on 0-th socket takes only 1/3 of time of other 54 cores when we compute same-sized MM sequentially on every core. Because the focus of this paper is algorithm, rather than systems or computer architecture, instead of figuring out the reason of machine’s heterogeneity, we simply switch to a heterogeneous version with the new results shown in Fig. 9b. Now we can see that the mean and median of speedup ratio raises to 48.6% and 48.8%, respectively. To reduce the overheads of reduction of intermediate results, our heterogeneous MM is slightly different from PACO Hetero-MM algorithm in Sect. ??, but is similar to the rectangular partitioning by Nagamochi and Abe [50]. The algorithm structure is similar to PACO MM-1-Piece algorithm and has following changes. We view the recursive divide-and-assign procedure as a binary tree, where each leaf stands for a processor’s throughput and each internal node stands for the summation of its left and right child’s throughput. We divide the initial cuboid starting from the root of tree by a recursive procedure until each derived cuboid reaches a leaf. At each internal node, we cut a cuboid on its longest dimension by the ratio of the node’s left and right child’s throughput. By the change, each processor will get only one cuboid instead of a sequence.

Figure 10a shows the performance comparison of PACO MM-1-Piece algorithm with MKL’s parallel dgemm on the 24-core system, with a mean speedup of 11.1% and median of 6.4%. Problem size is calculated as $n \times m \times k$ for an $n$-by-$k$ matrix multiplying an $k$-by-$m$ matrix, where $n, m, k$ iterate independently from 8,000 to 44,000 with a step size of 4,000.
So there are multiple points of the same $x$-value. Figure 11 show the frequencies of PACO MM-1-Piece algorithm’s speedup over MKL and PO counterparts. “CO2” in the figure stands for the PO depth-$n$ MM algorithm based on 2-way divide-and-conquer [14] with a base-case size of 64. We select this base-case size by several manual trials to give the CO2 algorithm a reasonably good performance on the machine, though we do not attempt to make a thorough searching because tuning is not the focus of this paper. Recent research by Leiserson et al. [57] actually justifies our conclusion by showing that a well-tuned PO MM algorithm achieves about 40% of machine’s peak performance. Actually one concern on the PO approach is that its implementation may require to choose a proper base-case size, i.e. when to stop partitioning and parallelizing the algorithm, to balance communication, synchronization and processor utilization. If a base-case size is too small, it increases “slackness” of algorithm and allows better processor utilization for a wider range of processor counts, but at the cost of more deviations from its sequential execution order [33], [24], hence more communication and synchronization overheads. On the other hand, if a base-case size is too large, a base-case task may not fit in some upper-level cache(s) of each processor, hence it may not be cache-efficient, and the load imbalance among processors may be larger, in other words, some processor may be under-utilized. By contrast, our approach does not need to tune. Figure 11(b) shows the percentages of theoretical peak performance ($R_{peak}/R_{max}$) that PACO MM-1-Piece algorithm has attained. Table IV lists different algorithm’s mean and median of $R_{max}/R_{peak}$ side-by-side. The $R_{max}$ is calculated by “$2 \times n \times m \times k/time_{in\_second}$” because we are computing $C = C + A \times B$ so there are $nmk$ multiplications and $nmk$ additions. The $R_{peak}$ is calculated by “$24 \times (2.3 \cdot 10^9) \times 16$” because this machine has 24 cores, each of which is 2.3 GHz, which means $2.3 \cdot 10^9$ cycles per second, and each core can perform 16 dual precision floating point operations per cycle.

B. LCS and Sorting

We experiment PACO LCS algorithm and PACO SORT algorithm with PO and PA counterparts on the 24-core machine as shown in Fig. 12. The PO LCS counterpart is the classic 2-way divide-and-conquer algorithm [25] with a base-case size of 256 elements while the PA is the $p$-way divide-and-conquer by Chowdhury and Ramachandran [3]. We select this base-case size by several manual trials to give the PO algorithm a reasonably good performance on the machine, though we do not attempt to make a thorough searching because tuning is not the focus of this paper.

The mean and median speedups of PACO LCS algorithm over the PO is 71.2% and 54.4%, respectively, and over the PA is 86.3% and 88.3%, respectively. The PO Sorting counterpart is the low-depth sorting algorithm [15] implemented in the Problem Based Benchmark Suite (PBBS) [55]. We directly use the default oversampling ratio and other parameters implemented in PBBS without any tuning. The mean and median speedup of PACO SORT algorithm over it is 9.3% and 9.1%, respectively.

V. CONCLUDING REMARKS

More Related Works: Andreev and Räcke [58] partitions a graph into several equal-sized components while minimizing the capacity of edges between different components. They did not consider minimizing computation and communication

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1. A 64 base-case size means that the algorithm stops cutting a dimension when it is less than or equal 64 and a cuboid will be a base case when none of its three dimensions can be cut.

2. By Fused Multiply Add FMA3 instruction

3. A 256 base-case size means that the algorithm stops cutting a dimension when it is less than or equal $16 = \sqrt{256}$ and a square will be a base case when none of its two dimensions can be cut.
(a) PACO LCS algorithm’s speedup over PO and PA counterparts.

(b) PACO SORT algorithm’s speedup over PBBS.

Fig. 12: Experiments on LCS and Sorting algorithms on the 24-core machine.

along a critical path so that their solution may not be a perfect strong scaling one.

Conclusions: This paper proposes a general PACO algorithm based on the observation that the maximal speedup attainable on a p-processor system is usually p-folds so that excessive parallelism may not be necessary. Our methodology is to partition computation and communication evenly and recursively among p processors by a pruned BFS traversal of a cache-oblivious algorithm’s divide-and-conquer tree. Each processor will have balanced computational and communication overheads, usually forming in a geometrically decreasing sequence. We apply the idea to several important cache-oblivious algorithms, including LCS, which is Dynamic Programming (DP) with constant dependencies, 1D and GAP, both of which are DP with more-than-constant dependencies, classic rectangular MM on a semiring and Strassen’s algorithm, as well as comparison based sorting. Compared with classic PA counterparts, our algorithms achieve perfect strong scaling on an arbitrary number, even a prime number, of processors within a certain range. Compared with classic PO counterparts, our algorithms usually have better communication complexities. Our PACO STRASSEN-CONST-PIECES algorithm provides an almost exact solution to the open question on parallelizing Strassen’s algorithm efficiently and exactly on an arbitrary number of processors. Our preliminary experimental results confirm the theoretical predictions. Our methodology may provide a new perspective on the fundamental open problem of extending a sequential cache-oblivious algorithm to an arbitrary architecture. We leave an efficient parallelization of PACO LCS algorithm’s partitioning phase to future research.

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