Solution-processed organic field-effect transistors based on dinaphthothienothiophene precursor with chemically modified electrodes

Takashi Nagase¹², Souichiro Abe¹, Takashi Kobayashi¹², Yu Kimura³, Azusa Hamaguchi¹, Yoshinori Ikeda³ and Hiroyoshi Naito¹²

¹Department of Physics and Electronics, Osaka Prefecture University, Sakai 599-8531, Japan
²The Research Institute for Molecular Electronic Devices (RIMED), Osaka Prefecture University, Sakai 599-8531, Japan
³Electronics Materials Development Project, Teijin Limited, Hino, Tokyo 191-8512, Japan

E-mail: nagase@pe.osakafu-u.ac.jp, yos.ikeda@teijin.co.jp, naito@pe.osakafu-u.ac.jp

Abstract. Bottom-gate organic field-effect transistors (OFETs) based on a soluble precursor of dinaphtho[2,3-b:2’,3’-f]thieno[3,2-b]thiophene (DNTT) with bottom-contact source-drain electrodes chemically modified with pentafluorobenzenethiol (PFBT) have been fabricated. The preparation of DNTT films using CYTOP overcoat layers allows the solution processing of bottom-gate/bottom-contact DNTT FETs with good electrical contacts between the PFBT-treated Au electrodes and the DNTT molecules. The DNTT FETs processed using CYTOP overcoat layers exhibit the field-effect mobilities of up to 0.37 cm² V⁻¹ s⁻¹. High maximum mobility of 0.29 cm² V⁻¹ s⁻¹ has been achieved in solution-processed DNTT FETs with channel length of 5 μm.

1. Introduction
In recent years, a highly π-extended small-molecule semiconductor, dinaphtho[2,3-b:2’,3’-f]thieno[3,2-b]thiophene (DNTT) [1], has attracted considerable interest as a promising channel material for high-performance organic field-effect transistors (OFETs). OFETs with vacuum-deposited DNTT thin films exhibit high field-effect mobilities of up to 2.9 cm² V⁻¹ s⁻¹ and good air stability because the DNTT enables thin-film formation with excellent microstructures and has a high ionization potential (5.4 eV) [1 - 3]. Recent interest has also been directed towards the development of highmobility solution-processable OFETs. However, DNTT molecules show low solubility in organic solvents, even when long alkyl chains are attached to the molecules [4]. A DNTT precursor, 5,14-N-phenylmaleimide dinaphtho[2,3-b:2’,3’-f]thieno[3,2-b]thiophene (Fig. 1), can be dissolved in organic solvents (e.g., chloroform, dichlorobenzene, or dimethylacetamide) at room temperature because of its low crystallinity, and can be converted into DNTT by thermal annealing through the elimination of N-phenylmaleimide [5]. We have recently demonstrated the solution processing of high-performance bottom-gate/top-contact DNTT FETs through vertical phase separation that appeared in solution-processed blend films of the DNTT precursor and an insulating polymer [5 - 7].
For application of OFETs to organic integrated circuits, the development of bottom-gate/bottom-contact DNTT FETs is desirable since fine-pattering techniques, such as photolithography and ink-jet printing, can be applied to the fabrication of source-drain electrodes with narrow spacing. It is widely known that the field-effect mobility of bottom-gate/bottom-contact OFETs depends sensitively on a charge injection barrier formed at the source electrode/organic semiconductor interface as compared with that of bottom-gate/top-contact OFETs [8 - 10]. The chemical modification of Au source-drain electrodes with a thiolated self-assembled monolayer (SAM) of pentafluorobenzenethiol (PFBT) has been found to increase the work function of Au electrodes (~4.8 eV) to 5.2-5.5 eV [11, 12]. This leads to the enhancement in the field-effect mobility of bottom-gate/bottom-contact short-channel OFETs with vacuum-deposited alkylated DNTT thin films as a result of the decrease in the hole injection barrier (contact resistance) at the Au electrode/DNTT interface [13]. However, we observed that the solution processing of DNTT films on substrates with PFBT-treated Au electrodes does not allow forming continuum films at boundaries between the substrate and the PFBT-treated electrodes.

In this study, we develop a simple technique for fabricating bottom-gate/bottom-contact OFETs based on the DNTT precursor with PFBT-treated source-drain electrodes by using an overcoat layer of CYTOP. The DNTT FETs processed using CYTOP overcoat layers exhibit higher electrical performances as compared with those of devices processed without using CYTOP overcoat layers. Solution-processed DNTT FETs exhibit high field-effect mobilities of up to 0.37 cm²V⁻¹s⁻¹.

2. Experimental

Figure 1 shows the schematic diagram of a bottom-gate/bottom-contact DNTT FET device processed using the DNTT precursor. Au source-drain electrodes (40 nm) with thin Cr adhesion layers (2 nm) were fabricated by vacuum evaporation through a metal shadow mask on a heavily doped Si wafer with a SiO₂ layer (300 nm), which were used as the gate electrode and the gate insulator, respectively. The substrates with Cr/Au electrodes were washed sequentially with acetone and 2-propanol in ultrasonic baths and were then cleaned with O₂ plasma to remove organic contaminants. The surfaces of Au electrodes were chemically modified with the SAM of PFBT (Tokyo Chemical Industry Co., Ltd.) to reduce a hole injection barrier caused by the potential difference between the work function of Au (~4.8 eV) and the ionization potential of DNTT (5.4 eV). To form the SAMs on Au surfaces, the substrates were immersed in a ~50 mM ethanol solution of PFBT overnight at room temperature in a capped bottle. After removing the substrates from the PFBT solution, they were ultrasonically washed in fresh ethanol to remove any excess layers. A 0.2 wt% chloroform solution of the DNTT precursor, which was synthesized in our laboratory [5], was drop cast on the substrates and dried in ambient air. Then, an amorphous fluoropolymer solution of CYTOP (CTL-809M, Asahi Glass Co., Ltd) was spin-coated on the DNTT precursor films and subsequently annealed at 200 °C for 5 min in air to convert DNTT precursor into DNTT. We also fabricated OFETs with DNTT films on substrates having PFBT-treated Cr/Au electrodes (2 nm/40 nm) without using CYTOP overcoat layers for comparison. The channel length (L) and width (W) of these FET devices were 350 μm and 2 mm, respectively.

![Figure 1](image-url)

**Figure 1.** Chemical structure of organic materials and the schematic diagram of a bottom-gate/bottom-contact OFET processed using the DNTT precursor and the CYTOP overcoat layer.
To investigate the dependence of field-effect mobilities on channel length, we fabricated bottom-gate/bottom-contact DNTT FETs with $L_s$ ranging from 250 to 5 μm and a fixed $W$ of 1.5 mm using photolithographically-defined Cr/Au source-drain electrodes on Si/SiO$_2$ substrates, where the surfaces of SiO$_2$ gate insulators were treated with a SAM of phenethyltrichlorosilane (PETS) (Gelest, Inc.) to suppress hysteresis behavior for the forward and reverse scans of the gate voltage often reported for $p$-type OFETs with SiO$_2$ insulators [14, 15]. The substrates were immersed in a ~50 mM toluene solution of PETS overnight after PFBT treatment of Au electrodes to form the PETS SAMs on SiO$_2$ surfaces.

The current-voltage characteristics of OFET devices were measured in a nitrogen-filled glove box or vacuum using source meters (Keithley 6430, 2635, and 2400) at room temperature.

3. Results and discussion

Figures 2(a) and 2(b) show the polarized optical micrographs of regions around the edges of PFBT-treated Au electrodes in DNTT FETs fabricated without and with CYTOP overcoat layer, respectively. Solution-processing DNTT FETs with PFBT-treated Au electrodes without using CYTOP layers causes needle-like crystals around the electrode edges, whereas firm forming with CYTOP layers suppresses the formation of needle-like crystals. The typical gate voltage ($V_G$)-drain current ($I_D$) (transfer) and drain voltage ($V_D$)-$I_D$ (output) characteristics of both DNTT FETs are shown in Figs. 2(c) and 2(d), respectively. It is found that the drain current of devices is remarkably increased using CYTOP overcoat layers, indicating better connectivity between DNTT molecules and PFBT-treated electrodes in devices with CYTOP overcoat layers.

The field-effect mobility ($\mu$) was determined in the saturation regime from the slope of $|I_D|^{1/2} - V_G$ curve in the low $V_G$ region using the standard FET equation: $I_D = (W/2L)\mu C(V_G - V_th)^2$, where $C$ is the capacitance per unit area for the gate insulator and $V_th$ is the threshold voltage. The maximum field-effect mobility of PFBT-treated devices with CYTOP layers was 0.37 cm$^2$ V$^{-1}$ s$^{-1}$, which is much higher than that of PFBT-treated devices without CYTOP layers (0.03 cm$^2$ V$^{-1}$ s$^{-1}$) and that of non-treated devices with CYTOP layers (0.04 cm$^2$ V$^{-1}$ s$^{-1}$). The average mobility was 0.17 cm$^2$ V$^{-1}$ s$^{-1}$, which is comparable to or higher than the mobilities of bottom-gate/top-contact devices fabricated on non-treated SiO$_2$ gate insulators (0.085–0.13 cm$^2$ V$^{-1}$ s$^{-1}$ [5]). These results clearly indicate that the PFBT treatment effectively works to reduces hole injection barriers at the Au source electrode/DNTT semiconductor interfaces.

The exact reason for the formation of needle-like crystals for DNTT FETs without CYTOP layers

![Figure 2](image_url)

Figure 2. Polarized optical micrographs of regions around the PFBT-treated Au electrodes in bottom-gate/bottom-contact OFETs based on the DNTT precursor fabricated (a) without and (b) with CYTOP overcoat layers. (c) Transfer and (d) output characteristics of both DNTT FETs without and with CYTOP overcoat layers. The channel length of devices was 350 μm.
is unclear at present. However, the enhancement in the growth of highly crystalline films on low energy surfaces reported for solution-processed OFETs [16] could be responsible for the formation of needle-like crystals because PFBT-treated Au electrodes have high hydrophobicity (its water contact angles was ~85°) [17]. In fact, it has been found that PFBT-treated Au electrodes induce the crystallization of a soluble small-molecule semiconductor and the growth of crystalline films extends into the channel region [18]. We consider that the confinement of DNTT molecules between the substrate and the CYTOP overcoat layer would facilitate two-dimensional crystal growth of DNTT films during thermal annealing.

Figures 3(a) and 3(b) show the representative transfer and output characteristics of solution-processed DNTT FETs using CYTOP overcoat layers with different channel lengths, respectively. In these devices, PFBT and PETS were employed for SAM treatment of the Au electrodes and the SiO₂ insulator, respectively. The devices exhibit good transistor performances with high on/off ratios of over 10⁵ and small hysteresis in the transfer characteristics between the forward and backward scans of the gate voltage. The hysteresis behavior of p-type OFETs with SiO₂ gate insulators is believed to be caused by long-lifetime trapping of electrons by hydroxyl (OH) groups existed at the SiO₂ surfaces [14,
and therefore the observed small hysteresis in our devices can be attributed to the termination of the OH groups with PETS SAMs.

The dependence of field-effect mobilities on channel length of devices is shown in Fig. 4. It is found that the field-effect mobility of solution-processed bottom-gate/bottom-contact DNTT FETs tends to increase as the channel length is reduced from 250 to 100 μm. Such behavior can be understood by the decrease in the boundaries of crystalline DNTT domains between source-drain electrodes as shown in the polarized optical micrographs of channel regions (Fig. 5), since it can reduce frequent carrier trapping at the domain boundaries between source-drain electrodes.

We also see from Fig. 4 that the field-effect mobility gradually decreases as the channel length is reduced from 100 to 5 μm. This is likely caused by the influence of contact resistance, and the decrease in the total resistance of devices associated with the reduction of channel length is restricted in case of the presence of high contact resistance, which leads to the apparent decrease in the field-effect mobility in short-channel devices [19]. However, the solution-processed DNTT FETs with channel length of 5 μm achieved a high field-effect mobility of 0.29 cm²V⁻¹s⁻¹ at maximum. It has been observed that the field-effect mobility of solution-processed DNTT FETs depends on the film annealing temperature and time [5]. The contact resistances of OFETs are also known to be reduced by the increase in the gate voltage. The optimization of film processing processes and the use of thinner gate insulators, such as SAM-treated oxidized Al (AlOₓ) insulators [2, 3], can therefore lead to further improvement in the field-effect mobilities of solution-processed DNTT FETs.

Figure 4. Channel length-dependence of the field-effect mobility of solution-processed bottom-gate/bottom-contact DNTT FETs.

Figure 5. Polarized optical micrographs of the channel region of solution-processed DNTT FETs with channel lengths of (a) 200 μm, (b) 100 μm, (c) 50 μm, and (d) 10 μm.
4. Conclusions
We have examined the solution processing of bottom-gate DNTT FETs based on the DNTT precursor with bottom-contact source-drain electrodes chemically modified with fluorinated PFBT SAMs and investigated their electrical performances. It is found that the use of CYTOP overcoat layers in forming DNTT films allows fabricating bottom-gate/bottom-contact DNTT FETs with high field-effect mobilities of up to 0.37 cm²V⁻¹s⁻¹. The field-effect mobility tends to increase with reducing channel length and the devices with channel length of 5 μm exhibit a field-effect mobility of 0.29 cm²V⁻¹s⁻¹ at maximum.

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