Abstract

With the high demand of the portable electronic products, Low- power design of VLSI circuits & Power dissipation has been recognized as a challenging technology in the recent years. PLA (Programming logic array) is one of the important off shelf part in the industrial application. This paper describes the new design of PLA using power gating structure sleep transistor at circuit level implementation for the low power applications. The important part of the power gating design i. e. header and footer switch selection is also describes in the paper. The simulating results of the proposed architecture of the new PLA is shown and compared with the conventional PLA. This paper clearly shows the optimization in the reduction of power dissipation in the new design implementation of the PLA. The transient response of the power gates structure of PLA is also illustrate in the paper by using TINA-PRO software.

References

- Abdullah A, Fallah F, and Pedram M, (Jan 2007) "A robust power gating structure
and power mode transition strategy for MTCMOS design; IEEE Trans. Very large Scale integration, vol 15, No 1, pp. 80-89.
  - Howard D., Shi K (2006), "Sleep Transistor design and implementation simple concepts yet challenges to be optimum," proc. VLSI-DAT, pp. 1-4.
  - C. Chrisim Gnana suji, S. Maragatharaj, "Performance analysis of power gating in low power VLSI circuits," Proc. Of ICSCCN, pp. 689-694, 2011 IEEE.
  - Changbo Long and L. He, "Distributed sleep transistor network for power reduction," IEEE Trans. Very large scale integer, vol. 12, no. 9, pp. 937-946, Sep 2004.
  - Designing Low-Power Circuits: Practical Recipes by Luca Benini Giovanni De Micheli Enrico Macii.
  - J. P. Uyemura, Introduction to VLSI Circuits and Systems. New York: Wiley, 2002.
  - C. Long, J. Xiong, and L. He, "On optimal physical synthesis of sleep transistors," in Proc. ISPD, 2004, pp. 156-161.
  - Chang H, Lee C, and Sapatnekar S. S, (2005) "Full-chip analysis of leakage power under process variations, including spatial correlations," in Proc. Des. Autom. Coni (DAC), pp. 523-528.
  - Pradeep Singla and Naveen Kr. Malik, "A cost-effective design of reversible programmable logic array," International Journal of Computer applications Vol. 41(15), pp. 41-46, 2012.
  - S. Mutoh et al., "1-V power supply high speed digital circuits technology with multithreshold voltage CMOS," JSSC, vol. SC-30, pp. 847-854, Aug. 1995.
  - Umea Normal et al., "A low power high speed adders using MTCMOS Technique," International journal of computational engineering & Management, vol. 13, pp. 65-69, July 2011.

Index Terms

Computer Science
Integrated Circuits

Keywords

Low Power Design  Sleep Transistor  Header  Footer  Power Gating  Tina-Pro  Pla
