Study of Cluster Test of Complex Circuits

Zhiwei Li 1, Zhongliang Pan 2
1 Guangzhou Civil Aviation College, Guangzhou, China
2 South China Normal University, Guangzhou, China

Abstract. Cluster test of complex circuits is very difficult. The paper uses boundary scan test technology, different test algorithm, and test method for performing output operations on the boundary scanning units at each end of the interconnect network, and does a lot of test and analysis, effectively solves the problems of cluster test of complex circuits, and gives high fault resolution.

Key words: Complex Circuits; Boundary Scan Test; Test Algorithm; Cluster Test.

1. Introduction
For the testing of complex circuits, it is possible to use boundary scan test technology [1, 2], and IEEE has developed a series of test standards (1149.1, 1149.4, 1149.6, and 1149.7) [3-6]. The cluster structure circuit is shown in figure 1. Cluster structure circuit is that the chips that have boundary scan test (BST) function surround the chips or other components that do not have BST function, so that these chips or components can be tested by BST method. The application of cluster test can greatly improve the testability of the complex circuits, can test the interconnection of the circuits without BST function, and in some cases can even test whether the main function of chips without BST function in these circuits is normal.

2. Analysis of common faults in cluster structure circuits
In the circuit board manufacturing process, may cause open circuit, short circuit or sluggish fault. Some boards may have only one type of fault, while others may have multiple faults. In the cluster test, the fault situation will be more complicated, and the following three common fault types are analyzed [2].
2.1. Open circuit fault
For an open circuit fault, the interconnect pin is suspended. In the cluster structure, it is possible for the interconnect pin of one BST chip, or for two BST chips simultaneously.

In the test process, the following three situations may occur: case 1, if the interconnect pin of the BST chip for input operation is open, the value of the input pin will not be affected by its serial test vector, and the value captured by the boundary scanning unit depends on the chip technology; In case 2, if the interconnection pin of the BST chip for output operation is open, the value of the input pin will not be affected by the serial test vector, and the value captured by the boundary scanning unit depends on the joint decision of the BST chip for input operation and the structure without BST function. In case 3, if both BST chips have an open circuit failure, the result will be similar to case 1.

2.2. Sluggish fault
Sluggish fault can be divided into sluggish ‘1’ and sluggish ‘0’. In general, an open circuit fault can also be classified as a sluggish fault, because in most cases the value captured by the boundary scanning unit is a logic ‘0’ or ‘1’. In this paper, uses the method in which the boundary scan units at both ends of the interconnection network were used for output to do the cluster test [7], and can better distinguish the open circuit fault from the sluggish fault.

2.3. Short circuit fault
Short circuit fault is caused by two or more signal lines being bridged together. In fault detection, short circuit fault judgment is more complicated. In boundary scan test, short circuit fault mainly refers to the bridge between the adjacent signal lines. For the bridge between signal lines and power supply or ground, it can be classified as sluggish fault.

When a network with an output of logic ‘0’ and a network with an output of logic ‘1’ are short-circuited, the final output signal depends on whose driving ability is stronger. The short circuit fault includes ‘or’ short circuit (logic ‘1’ driving ability is stronger), ‘And’ short circuit (logic ‘0’ driving ability is stronger), ‘Weak’ short circuit (uncertain final logic value after short circuit). After the actual test in this paper, it is found that the short circuit of the output pin of EP1C3T144 is ‘or’ short circuit, the short circuit of the output pin of EPM7064AET44 is ‘and’ short circuit, the output pin short circuit of SN74LVTH182512 is ‘and’ short circuit.

3. Test method
In this paper, different testing algorithms are combined and the method in which the boundary scan units at both ends of the interconnection network were used for output is used to complete the cluster test of complex circuits.

3.1. Test algorithms
The test algorithm is a method to optimize the test vector, it is only a macro description of how each network should be assigned. The actual test data moving into the boundary scan units is more complex.

The walking ‘1’ algorithm is the most basic and practical one, which can cover a wide range of fault types. However, it has a disadvantage that its parallel test vector (PTV) is equal to the number of networks to be tested, which results in a longer test time. Each PTV only gives ‘1’ to only a network, which takes a long time to test, so some optimization algorithms appear, such as minimum weight algorithm, binary counting sequence algorithm, modified binary counting sequence algorithm, counting compensation algorithm, etc [2,8-10]. In this paper, comprehensively analyzed these test algorithms, the walking "1" algorithm and the modified binary counting sequence algorithm were used to test the experimental circuit board.
3.2. Test process
The test process of the upper computer is shown in figure 2. Because it uses the method in which the boundary scan units at both ends of the interconnection network were used for output, there are two sets of test vector matrix and two sets of response vector matrix for each test.

\[ \text{Netlist and BSDL files} \]
\[ \text{Obtain the information of the interconnect pin corresponding to the boundary scanning unit and the instruction information} \]
\[ \text{Test algorithm setup, two sets of test vector matrix generation} \]
\[ \text{Matrix 1 sent out?} \]
\[ \text{Y} \]
\[ \text{Matrix 2 sent out?} \]
\[ \text{Y} \]
\[ \text{two sets of test response matrix} \]

\[ \text{Open circuit, sluggish, short circuit fault detection, location, display} \]

**Figure 2.** Test process

4. Test experiment

4.1. Structure of the experimental circuit
The cluster structure and the boundary scan link of the experimental circuit board are shown in figure 3. U1 (EP1C3T144), U2 (EPM7064AE) and U3 (SN74LVTH182512) have the function of boundary scan test. U3 is a dedicated boundary scan test chip. However, the test link needs to pass through U2, so in the cluster test, relevant boundary scanning units of U2 should be bypassed.

\[ \text{U1 EP1C3T144} \]
\[ \text{U2 EPM7064AE} \]
\[ \text{U3 SN74LVTH182512} \]

**Figure 3.** The cluster structure and the boundary scan link of the experimental circuit board

4.2. Cluster test experiment
The fault diagnosis of cluster test is not accurate enough, which is caused by the part of cluster structure without BST function. It is impossible to predict the test results from BSDL files and netlist files alone, which makes the diagnosis of fault types more difficult. This is inevitable, only we can determine the logical functions that do not have BST function part artificially, so as to improve the effect of identify the fault. The cluster structure fault set on the experimental circuit board is shown in figure 4.
Table 1 shows the test results using the walking ‘1’ algorithm, and table 2 shows the test results using the modified binary counting sequence algorithm.

**Table 1.** Used the walking ‘1’ algorithm to test the fault in cluster structure

| Response matrix 1 | Response matrix 2 | Fault and location                          |
|-------------------|-------------------|---------------------------------------------|
| 000000010         | 001000010         | Open circuit: C1_3; C2_3*; C2_1*; C2_8*;    |
| 010000010         | 011000010         | Sluggish 0: C1_1*; C2_1*; C1_8*; C2_8*;     |
| 000000010         | 001000010         | Sluggish 1: C1_7*; C2_7*;                   |
| 000101100         | 001000010         | Short circuit: C2_4; C2_6;                  |
| 000010100         | 001010010         |                                             |
| 000101100         | 001000010         |                                             |
| 000000010         | 001000010         |                                             |
| 000000010         | 001000010         |                                             |

*’* means the location is a high probability.

**Table 2.** Used the modified binary counting sequence algorithm to test the fault in cluster structure

| Response matrix 1 | Response matrix 2 | Fault and location                          |
|-------------------|-------------------|---------------------------------------------|
| 000000010         | 001000010         | Open circuit: C1_3; C2_3*; C2_1*; C2_8*;    |
| 000111110         | 001111110         | Sluggish 0: C1_1*; C2_1*; C1_8*; C2_8*;     |
| 010101110         | 011000010         | Sluggish 1: C1_7*; C2_7*;                   |
| 000010100         | 001010010         | Short circuit: C2_4; C2_6;                  |

*’* means the location is a high probability.

In the test, the method in which the boundary scan units at both ends of the interconnection network were used for output is used, so there are two sets of response vector matrix. It can be seen from the diagnosis results that the fault judgment of the two test algorithms is the same. In contrast, the modified binary counting sequence algorithm has more advantages in test time.

According to the test results, the short circuit fault can be diagnosed. But due the part of cluster structure without BST function, adopted the method in which the boundary scan units at both ends of the interconnection network were used for output, the sluggish failure and open failure of individual position although not confirmed, but suspected fault location are given, and the location is the actual fault location, just the types of faults need to be further judgment, simply by artificial judgement at this time, it can be confirmed immediately.
5. Conclusion
Boundary scan test method is an effective technique for complex circuit testing, which provides an ideal solution for complex circuit testing. Through the experiment, the method in which the boundary scan units at both ends of the interconnection network were used for output is used to test the complex circuit cluster, with the good test algorithm, can find the fault location better.

Acknowledgments
This work was financially supported by Guangzhou Science and Technology Plan Project (201904010107), Guangdong Natural Science Foundation Project (2019A1515010793), Guangdong Science and Technology Plan Project (2016B090918071).

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