1 Overview

Cyber-physical systems (CPS) are integrations of computation with physical processes, where computing machineries monitor and interact with the physical world via sensors and actuators. In such a system, the reading of a sensor represents measurements of a physical quantity, and the values are often reals ranged over bounded intervals. The implementation of control laws is based on nonlinear numerical computations over the received sensor values. Synthesizing controllers fulfilling features within CPS brings a huge challenge to the research community in formal methods, as most of the work in automatic controller synthesis (LTL synthesis) is designed to handle specifications having inputs within the Boolean domain [10, 14, 7, 3].

In this report, we present a novel approach that addresses the above challenge to synthesize controllers for CPS. Our core methodology, called numerical LTL synthesis, extends LTL synthesis [12] by using inputs or outputs in real numbers and by allowing predicates of polynomial constraints to be defined within an LTL formula as a specification. The synthesis algorithm is based on an interplay between an LTL synthesis engine that handles the pseudo-Boolean structure, together with a nonlinear constraint validity checker that tests the (in)feasibility of a (counter-)strategy. The methodology is integrated within the CPS research framework Ptolemy II [8] via the development of an LTL synthesis module G4LTL [1] and a validity checker JBernstein [4]. Although we only target the theory of nonlinear real arithmetic, the use of pseudo-Boolean synthesis framework also allows an easy extension to embed a richer set of theories, making the technique applicable to a much broader audience.

2 Numerical LTL Synthesis

2.1 Understanding Numerical LTL Synthesis

We use an example to illustrate key ingredients of numerical LTL synthesis, including the specification methodology and the algorithmic interplay between the pseudo-Boolean LTL synthesizer and the theory solver.

**Specification.** Consider a reactive system where in each reactive cycle, sensor readings are updated. In this system, two variables \(x, y \in [0, 4] \cap \mathbb{R}\) are used to store the sensor values in each cycle. The system has two clients Client1 and Client2. Client1 issues a request when \(x + y > 3\) holds, while Client2 issues a request when \(x^2 + y^2 < \frac{7}{2}\) holds. Our goal is to design a controller that grants a client in the next round
whenever he requests. However, as the resource is unique, it is disallowed to grant the resource simultaneously to two clients in each cycle. When we use two Boolean variables grant1, grant2 to represent the issuing of the resource in each round, we can describe the specification of a correct controller formally using the following “extended” LTL formula, where $G$, $F$ and $X$ are temporal operators \[1\] representing “always,” “eventually” and “next”:

$$G(x+y > 3 \rightarrow Xgrant1) \land G(x^2 + y^2 < \frac{7}{2} \rightarrow Xgrant2) \land G(\neg (grant1 \land grant2)) \quad (1)$$

Pseudo-Boolean specification synthesis. The implemented numerical LTL synthesis algorithm interleaves between the pseudo-Boolean level and the theory level. First, rewrite $x+y > 3$ and $x^2 + y^2 < \frac{7}{2}$ as predicates req1 and req2. View req1 and req2 as independent input variables, then we have created the following pseudo-Boolean specification:

$$G(req1 \rightarrow Xgrant1) \land G(req2 \rightarrow Xgrant2) \land G(\neg (grant1 \land grant2)) \quad (2)$$

In the original specification, valuations of $x+y > 3$ and $x^2 + y^2 < \frac{7}{2}$ are inter-related, but req1 and req2 in the new specification are independent input variables. Therefore, the pseudo-Boolean specification overapproximates the capability of the environment.

When an LTL synthesis engine analyzes Eq. 2, it reports the unrealizability of the specification. The counter-strategy (i.e., reason of unrealizability) can be understood by a simple input pattern \(true, true\), as when both req1 and req2 are true, a controller needs to assign grant1 and grant2 to be true in the next round. This violates the third conjuncted invariance condition $G(\neg (grant1 \land grant2))$.

Counter-strategy validation (theory level). Given a counter-strategy on the pseudo-Boolean level, one needs to check whether such a strategy is indeed possible. In this example, it is equivalent to check whether it is possible to have $x+y > 3$ and $x^2 + y^2 < \frac{7}{2}$ true simultaneously, given $x, y \in [0, 4]$. We use a validity checker to examine the negated constraint $\forall x, y \in [0, 4] : \neg (x+y > 3 \land x^2 + y^2 < \frac{7}{2})$, or equivalently:

$$\forall x, y \in [0, 4] : x+y > 3 \land x^2 + y^2 \geq \frac{7}{2} \quad (3)$$

Such an assume-guarantee style constraint can be checked automatically by the solver JBernstein. In this example, JBernstein returns true, implying that this counter-strategy is spurious. If all pseudo-Boolean input patterns in the counter-strategy are realizable on the theory level, then the counter-strategy is genuine.

Specification refinement and resynthesis (pseudo-Boolean level). As the input pattern \(true, true\) can never appear, the subsequent step on the pseudo-Boolean level is to perform specification refinement. To rule out \(true, true\), one adds an assumption $G(\neg (req1 \land req2))$ to the original specification:

$$G(\neg (req1 \land req2)) \rightarrow (G(req1 \rightarrow Xgrant1) \land G(req2 \rightarrow Xgrant2) \land G(\neg (grant1 \land grant2))) \quad (4)$$

By posing this assumption and re-running the LTL synthesis engine, the engine reports the existence of a solution: if any one of req1 ($x+y > 3$) and req2 ($x^2 + y^2 < \frac{7}{2}$) is true, grant the corresponding client in the next round.
2.2 Workflow

The whole workflow for numerical LTL synthesis is illustrated in Fig. 1. The input of the workflow contains LTL(Th), the extended LTL formula where Th is the underlying theory. For the presented example, Th is the theory of nonlinear real arithmetic. The workflow first creates the pseudo-Boolean specification via the Abstract module, then the pseudo-Boolean specification is fed into the LTL controller synthesis engine. If the engine finds a controller $M_{ctrl}$, then the workflow stops and reports realizability. Otherwise, the workflow generates $M_{env}$, the counter-strategy for the environment to act as a spoiler.

Given $M_{env}$, the Extract module extracts a compact strategy that uses fewer pseudo-Boolean input valuations whose validity are not proven on the theory level. It then passes these unproven input valuations $S$ to the theory checker. In the previous example, the Extract module generates a counter-strategy that only uses $(req1, req2) = (\text{true}, \text{true})$, and $S = \{(\text{true}, \text{true})\}$. Given $S$, the theory checker checks whether any element in $S$ is not realizable. If all of them are realizable, then the counter-strategy is genuine and the workflow stops by reporting the unrealizability of the specification. Otherwise, whenever the theory checker detects one input combination $s_{in}$ that is not realizable, $s_{in}$ is used to refine the pseudo-Boolean specification. The refinement is demonstrated in the Refine module, and the refined specification is fed again to the LTL synthesis engine. For the set $S_{\text{proven}}$ of pseudo-Boolean input combinations that are proven to be realizable by the theory checker, it is stored within the Memorize module as elements in $S_{\text{checked}}$ (initially, $S_{\text{checked}} = \emptyset$), so that later in the input extraction process, module Extract does not place any element inside $S_{\text{checked}}$ and avoids duplicate checking on the theory level.

1LTL synthesis is known to be determined: If one cannot find a controller $M_{ctrl}$ realizing the LTL specification, there exists a counter-strategy $M_{env}$ for the environment.
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Our proposed algorithm can be viewed as analogous to the counter-example guided abstraction refinement (CEGAR) techniques \cite{6} applied in program verification. An intuitive method to replace the above procedure is to check whether all possible input combinations are possible within the theory level. However, this can be overly expensive, as given $n$ pseudo-Boolean input variables, one needs to perform validity checking of nonlinear constraints for $2^n$ times. Our counter-example guided technique is superior, as demonstrated in the previous example, it is sufficient to trigger the validity checking once rather than four times. Also, given the infeasibility of a certain input vector on the pseudo-Boolean level, it is impossible to have a counter-strategy that reuses this input vector, as this makes the specification trivially true. Together with the use of the Memorize module, the workflow guarantees that every input vector on the pseudo-Boolean level is checked for its validity at most once.

2.3 Duality between Inputs and Outputs

Clearly, the above problem formulation and workflow are simplified, as they only consider output variables within the Boolean domain. The methodology can be naturally extended so that the every output variable is also replaced by a polynomial constraint. In this way, even if a controller $M_{\text{ctrl}}$ is successfully synthesized on the pseudo-Boolean level, one still needs to check whether every output of $M_{\text{ctrl}}$ is realizable, similar to the above input validation process for counter-strategies. For pseudo-Boolean outputs, the refinement of un-realizability is to add new constraints as guarantees in the pseudo-Boolean specification. E.g., let $\text{grant1}$ and $\text{grant2}$ be output predicates on the pseudo-Boolean level. If we derive that $\text{grant1}$ and $\text{grant2}$ can not appear true simultaneously as a fact from the theory level, add $G(\neg(\text{grant1} \land \text{grant2}))$ to refine the pseudo-Boolean specification.

3 Towards an Optimized Implementation in Ptolemy II

In this section, we outline how we integrate the presented numerical LTL synthesis technique into Ptolemy II. Ptolemy II is an open source CPS research framework which is implemented in Java and supports easy installation and execution in most operating systems. To achieve seamless integration, the accomplishment of this work involves the development of two independent modules G4LTL and JBernstein.

3.1 G4LTL

G4LTL is the engine that performs (pseudo-Boolean) LTL synthesis. G4LTL implements two (incomplete) algorithms for synthesizing controllers. The first algorithm translates the corresponding Büchi automaton of a given specification to a Büchi game and generates the controller via Büchi game solving. The second algorithm parses the Büchi automaton of the negated specification, constructs a safety game via bounded unroll, and generates the controller via safety game solving. Ptolemy II uses actor-oriented programming techniques, and each actor can be viewed as a function that takes input tokens and produces output tokens. The engine is designed to allow the environment to start the first move; i.e., no output is generated if no input is provided. G4LTL uses two Java-based libraries LTL2Buchi \cite{9} and JDD \cite{2}, where LTL2Buchi is used for converting an LTL specification into its corresponding Büchi automaton, and JDD is used for solving safety and Büchi games symbolically.

\[2\] Here we pose a restriction on each polynomial constraint such that it can not be mixed with both input and output variables. Without the restriction, in the implementation one needs an analysis tool for exists-forall formulas.

\[3\] This read-input-produce-output view is common within the signals and systems community.
Assume that the operator always comes once for a while
ASSUME ALWAYS (EVENTUALLY (operator))

Whenever the error sign is raised,
## ALWAYS (error -> (stop UNTIL operator))

Rewrite <->, as it is not supported by LTL2Buchi
## ALWAYS (stop -> (!grant1 && !grant2 && !grant3) )
## ALWAYS (!grant1 && !grant2 && !grant3) -> stop

## Rewrite <->, as it is not supported by LTL2Buchi
ALWAYS (stop -> (!grant1 && !grant2 && !grant3) )
ALWAYS (stop UNTIL operator)

ALWAYS (req1 -> EVENTUALLY grant1)
ALWAYS (req2 -> EVENTUALLY grant2)
ALWAYS (req3 -> EVENTUALLY grant3)
ALWAYS (!grant1 || !grant2)
ALWAYS (!grant2 || !grant3)
ALWAYS (!grant1 || !grant3)

INPUT error, operator, req1, req2, req3
OUTPUT stop, grant1, grant2, grant3

## Newly translated specification
ASSUME ALWAYS (EVENTUALLY (operator))

ALWAYS (error -> (!sig1 && !sig2) UNTIL operator)
ALWAYS (req1 -> EVENTUALLY (!sig1 && sig2))
ALWAYS (req2 -> EVENTUALLY (sig1 && !sig2))
ALWAYS (req3 -> EVENTUALLY (sig1 && sig2))

INPUT error, operator, req1, req2, req3
OUTPUT sig1, sig2

Figure 2: An example for specifying a controller with error handling capabilities (above), and the translated specification by G4LTL (below).

G4LTL also implements a new feature to automatically rewrite an LTL specification before synthesis (as a preprocessing step), so that the use of variables can be reduced. This idea was sketched in our earlier technical report [5], and G4LTL is the first tool that realizes this feature for LTL synthesis. The workflow first synthesizes a controller realizing the rewritten specification (thus the synthesis speed can be exponentially faster than doing synthesis on the original specification), followed by automatically producing the signal multiplexer that translates a signal to the original one. The idea is illustrated in the example in Figure 2. For the specification above, G4LTL automatically detects that one can re-encode the output signals, as only 4 output combinations \{(1,0,0,0),(0,1,0,0),(0,0,1,0),(0,0,0,1)\} are possible. Therefore, it is sufficient to perform synthesis with two output variables. The system integrated with the synthesized modules is shown in Figure 3 where model1 is an FSMActor realizing the translated specification, and OutMultiplexer performs signal translation. The integration into Ptolemy II makes the visualization and simulation easy. In this model, once when links are established, within the simulation the light signal demonstrates whether a certain variable is set to true. In Figure 3, although an error appears, as the operator is also present, the controller can still grant the third client by setting variable grant3 to be true.
3.2 JBernstein

JBernstein is the engine that handles the validation of (counter-)strategies. JBernstein implements the validity checking process via the use of Bernstein polynomials. The process contains three steps: range transformation, basis transformation, and subspace refinement to recursively derive more precise bounds. As during the design process, we were unable to use software packages like GNU Multiple Precision Arithmetic Library in C or C++ which can guarantee precision by representing every rational number with two integer values (e.g., represent $\frac{1}{3}$ by $(1, 3)$), JBernstein uses double but conservatively estimates the maximum possible error due to the use of double. In this way, JBernstein only proves or disproves the validity on a strengthened property (by considering errors) and can also return unknown. We have used JBernstein to evaluate examples within the NASA PVS benchmark suite. JBernstein outperforms existing tools on complicated examples, while the strengthening is still precise enough to provide answer for all problems.

3.3 Integration

Constructing pseudo-Boolean game graphs only once. Our presented algorithm is based on an assumption where we view the synthesis engine and the validity checker as two black boxes. In the implementation, the algorithm can be further improved as we have full control to modify the LTL synthesis engine. Recall in each refinement step caused by the spurious counter-strategy, the algorithm removes
the ability of the environment by disallowing some input combinations. It is equivalent to the removal of environment edges in the generated game for the original pseudo-Boolean specification. Therefore, during the integration process, one can modify the internal data structure for games in G4LTL that marks an edge to be present or absent (due to the removal). This process avoids the repeated construction of game arenas from pseudo-Boolean LTL specifications.

**Implementing the Extract module.** The counter-strategy generation process within the pseudo-Boolean LTL synthesis engine plays an important role for numerical LTL synthesis. To apply CEGAR techniques, the engine needs to generate a strategy that minimizes the use of input assignments that are not checked on the theory level (otherwise, the validation can be overly time-consuming). In the presented counter-strategy, a state may have multiple outgoing edges. If only one edge is chosen for every state in the counter-strategy, it is still a counter-strategy. Therefore, the Extract module first tries to pick for every state in $M_{env}$ an edge whose input element is in $S_{checked}$. If this is possible, then the counter-strategy is genuine. Otherwise, perform a greedy-based approach to cover every state with an edge while maintaining the least use of input assignments that are not checked on the theory level. For the example presented in this paper, G4LTL is able to identify a counter-strategy (from the generated arena) that merely uses $(req1, req2) = (true, true)$.

**Using the tool.** To use numerical LTL synthesis in Ptolemy II, currently a user must provide the pseudo-Boolean specification (for G4LTL), together with polynomial constraint template where each abstract variable is set to true (for JBernstein; JBernstein will automatically parse the template and concretize based on the actual input variable assignment). The output (whenever a controller exists) is automatically created as an FSMActor component in a design canvas. One can open and see the concrete implementation, link it with other components to complete the design, or even use the code-generation framework within Ptolemy II to deploy the synthesized module as executable C program on dedicated platforms in cyber-physical systems.

Figure 4 shows a Synchronous Dataflow (SDF) model describing the scenario presented in this paper, together with the synthesized controller (named model1). The Purse actor is used to generate reactive runs, and the value of sensor Sensor:X and Sensor:Y are generated at random with a uniform distribution. After data processing, the value of $X + Y > 3$ is fed into the input port req1 of the synthesized FSMActor, while $X^2 + Y^2 < 3.5$ is fed into the input port req2. Inputs and outputs from the FSMActor are connected to a console to show the result of simulation. The FSMActor starts with state 5. Whenever an input (true, true) is provided, the specification holds and the execution moves to state 0. State 7 means that there is a pending grant to be issued for client 2; all outgoing edges (except the one to state 0) set grant2 to true. Analogously, state 9 implies a pending grant to be issued for client 1.

**Another example with 3 sensors.** Consider another example where two clients make their requests based on the reading of three sensor values $x_0, x_1, x_2$ ranging within $[0, 4]$. Client 1 requests when $x_0 + x_1 + x_2 > 3$, while client 2 requests when $(x_0)^2 + (x_1)^2 + (x_2)^2 < 4$. The solver detects that there exists a genuine counter-strategy by assigning $(x_0, x_1, x_2)$ to be $(0.314453125, 1, 1.6875)$. Under this assignment, $x_0 + x_1 + x_2 = 3.001953125 > 3$ and $(x_0)^2 + (x_1)^2 + (x_2)^2 = 3.946537017822265625 < 4$.

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4The use of CEGAR is an attempt to reduce the number of checks in for the theory solver, as validity checking for nonlinear constraints over reals is very time consuming. However, for the un-optimized method the cost of reducing checks for the theory solver is transferred to the check of realizability for pseudo-Boolean LTL specifications, as every refinement requires to trigger the LTL synthesis engine once.
4 Concluding Remarks and Discussion

**Availability.** Currently the tool is within the development version\(^5\) of Ptolemy II and is still under active development. Part of the features will be made public in the release of Ptolemy II version 9.0. Users can also download separately G4LTL and JBernstein to experiment the counter-example guided synthesis process manually.

**Contribution.** We conclude this report by summarizing our main contributions.

- The proposition of numerical LTL synthesis as a novel way to synthesize controllers for cyber-physical systems.
- The proposition of a CEGAR-based algorithm for numerical LTL synthesis, which involves the interplay between an LTL synthesizer and a (nonlinear real arithmetic) theory checker.

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\(^5\)Visit [http://chess.eecs.berkeley.edu/ptexternal/](http://chess.eecs.berkeley.edu/ptexternal/) to download the experimental version and follow the instructions to execute examples demonstrated in this paper.

\(^6\)The G4LTL module in Ptolemy II only employs the basic synthesis engine without optimization. The fortiss institute has developed an alternative (academic free) version that contains techniques presented in this paper and the synthesis speed is much faster.
• An implementation within the component-based design tool Ptolemy II that makes both normal and numerical LTL synthesis within the formal method community more approachable to a broader audience.

Discussion. LTL synthesis has been criticized concerning its practicability for two reasons.

1. It is very difficult to describe the system specification in full.
2. For full LTL synthesis, existing technologies commonly fails to scale with more than 10 input and 10 output variables.

Nevertheless, within the context of block-based languages such as Ptolemy II, one can discover that a system is hardly monolithic but rather composed by several blocks. Each block should be functionally isolated and implements a very specific feature. It turns out that it is highly uncommon to have the number of input and output ports within a block to be excessively high. Therefore, complete specification on the block level should be considered as possible. We believe that understanding the feasibility on block-based languages while probing further in numerical aspects of control will make synthesis techniques very useful to the CPS community.

For subsequent work, we plan to extend the technique to use it within the project iCyPhy (industrial cyber-physical systems) to synthesize over-voltage protection units for electric power systems.

Capturing system dynamics. For the previous workflow, the validity checking only checks whether a certain pseudo-Boolean input combination is possible on the theory level. For system dynamics captured by an equational system, checking if a counter-strategy is valid also involves a checking whether two (or more) consecutive pseudo-Boolean input valuations are realizable in the theory level.

We also plan to adapt the technique called relational abstraction. Given a time frame $\delta$, relational abstraction enables to create a sound approximation concerning relations between inputs for time $t$ and $t + \delta$, for all time $t$. With relational abstraction, our counter-strategy validation process also needs to examine whether all consecutive pseudo-Boolean inputs in the counter-strategy is realizable by being contained inside the relational abstraction. If it is impossible to have $in_1$ and $in_2$ as two consecutive pseudo-Boolean inputs, then in the refinement process, one does not add a state invariant (as in Figure 1) but an invariant similar in the following form

$G \neg (in_1 \rightarrow Xin_2) \quad (5)$

to act as an assumption on the environment.

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$^7$Observe Fig. 3, where for the FSMActor model1, using 5 inputs already occupies the left edge of the block completely.

$^8$iCyPhy: [http://www.icyphy.org/](http://www.icyphy.org/)
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