Design for Delay Fault Testability of 2-Rail Logic Circuits

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SUMMARY  This paper presents a scan design for delay fault testability of 2-rail logic circuits. The flip flops used in the scan design are based on master-slave ones. The proposed scan design provides complete fault coverage in delay fault testing of 2-rail logic circuits. In two-pattern testing with the proposed scan design, initial vectors are set using the set-reset operation, and the scan-in operation for initial vectors is not required. Hence, the test application time is reduced to about half that of the enhanced scan design. Because the additional function is only the set-reset operation of the slave latch, the area overhead is small. The evaluation shows that the differences in the area overhead of the proposed scan design from those of the standard scan design and the enhanced scan design are 2.1 and −14.5 percent on average, respectively.

key words: 2-rail logic circuits, design for testability, delay fault testing, scan design, set-reset operation

1. Introduction

As technology advances into the deep-submicron regime, designs are becoming increasingly more sensitive to various noise sources [1], [2]. Excessive noise causes performance degradation and signal integrity problems [3]. It corrupts the system-level data integrity. It also significantly affects the timing performance. Two-rail logic circuits (TRLCs) are expected to ensure the data integrity of today’s deep submicron devices [4]. Although TRLC offers strong error detection during normal operation, a chip including TRLCs needs off-line test as conventional commercial chips after manufacturing. This paper targets the off-line test of a chip including TRLCs.

The area of a TRLC is about twice as large as that of the single-rail logic circuit. It has a bad influence on the test costs. Therefore, test cost reduction of TRLCs is more important than that of single-rail logic circuits. It is now widely accepted that stuck-at fault testing can no longer satisfactorily test the functionality of fabricated integrated circuits in nanometer technologies. Unfortunately, traditional functional at-speed testing suffers from huge amount of test development costs, and limited effectiveness. Furthermore, limited test access to internal registers makes application of at-speed functional tests impractical.

Scan-based testing can significantly improve the controllability and observability, and thus it is a practical approach for large-sized complicated circuits fabricated in nanometer technologies. Some previous works related to the scan based delay fault testing are shown as follows. Broadside testing, skewed-load testing, and enhanced scan testing are well-known scan based delay fault testing techniques [5], [6]. The broad-side and skewed-load testing use the standard scan design, and thus the area overheads for those methods are not high. However, fault coverage is low because those methods permit the application of only strongly limited test patterns to circuit under test (CUT). The enhanced scan design achieves complete fault coverage [5]. However, the scan flip flop for the scan design requires additional redundant latches. These additional latches give bad influence on the area overhead. These works do not focus on TRLCs but single-rail circuits. No previous scan design has focused on TRLCs. Sparmann et al. researched the testability of unate gate network [7], [8]. Since TRLCs are unate, their results are applicable to TRLCs. However, they showed no concrete DFT architecture.

This paper presents a scan design for delay fault testability of TRLCs. The flip flops used in the scan design are based on master-slave ones. Conventional scan designs for single-rail logic circuits, such as the standard scan design and the enhanced scan design, can be applied to 2-rail logic circuits. But the proposed scan design, which focuses on 2-rail logic circuits, achieves complete delay fault coverage unlike standard scan-based delay fault testing, and lower area overhead than the enhanced scan design. The rest of this paper is organized as follows. Section 2 briefly explains the definition of TRLCs and the delay fault testing. Section 3 presents the detail of the proposed scan design. Section 4 evaluates the proposed scan design. Finally, Sect. 5 concludes this paper.

2. Preliminaries

In preparation for the later discussions, some notations and definitions will be presented first. In a 2-rail logic, a variable \( x \) is represented by a pair of signals \( (x_0, x_1) \). Thus 1-bit data of a 2-rail logic is represented 2-bit data shown as follows.

\[
x = 0 \iff (x_0, x_1) = (0, 1)
\]

\[
x = 1 \iff (x_0, x_1) = (1, 0)
\]

Figure 1 shows the basic gate expression of 2-rail logic functions. Especially, logic negation of 2-rail logic circuits

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3. Proposed Scan Design

This section describes the detail of the proposed scan design with delay fault testability for TRLCs. In two-pattern testing with the proposed scan design, the initial vectors are set using the set-reset operation. It reduces both the test application time and area overhead compared with the conventional enhanced scan design.

3.1 Overview of the Proposed DFT

Figure 2 illustrates a typical self-checking TRLC with the proposed DFT. The circuit consists of a 2-rail logic combinational block labeled TRL Logic, flip flops, and an error checker circuit E. The TRL Logic has the primary inputs, $x_0, x_1, \cdots, x_{0(n-1)}x_1(n-1)$, the primary outputs, $f_0, f_1, \cdots, f_{0(m-1)}f_1(m-1)$, the pseudo inputs, $z_0, z_1, \cdots, z_{0(n-1)}z_1(n-1)$, and the pseudo outputs, $y_0, y_1, \cdots, y_{0(n-1)}y_1(n-1)$. The pseudo inputs $z_0, z_1$ are connected to the outputs of $FF_0, FF_1$. The pseudo outputs $y_0, y_1$ are connected to the inputs of $FF_0, FF_1$. The error checker circuit E has the inputs connected to the outputs of $FF_0, FF_1$ and the primary output set $f_0, f_1$. In this figure, the input lines from the primary output set $f_0, f_1$ are left out for the convenience of space. It has an output line $Err$. The output $Err$ is activated if a fault occurs. The input $Scan In$ is the scan input, and the output $Scan Out$ is the scan output. The inputs $S_0$ and $S_1$ control the output value of slave latch of each $FF_i$.

3.2 Architecture of Proposed Scan Design

Figure 3 illustrates the detail of the proposed scan design. In this figure, the proposed flip flops, $FF_{00}, FF_{10}, \cdots, FF_{0n}, FF_{1n}, \cdots, FF_{0(n-1)}, FF_{1(n-1)}$ are arranged vertically. The flip flop $FF_i$ consists of the master latch $L_{M_i}$ and the slave latch $L_{S_i}$. The inputs $S_0$ and $S_1$ are set-reset inputs. Unlike normal set-reset inputs, the inputs control only the values of slave latches. The values of master latches are independent of the inputs. The inputs are not connected to the master latches, but connected to the slave latches.

The detail of the slave latch with the set and reset function is shown in Fig. 4(a). The value of the output of the slave latch is controlled using the set-reset operation when it is opened. The latch comprises two 2-input NAND gates and two CMOS switches. The NAND gate $G_0$ has two inputs, $S_0$ and $D$. The output is connected to an input of $G_1$. The other input of $G_1$ is $S_1$. The output of $G_1$ is $Q$. The clock signal $Clk$ controls the CMOS switches. When $Clk = 1$, $S_0 = 1$, $S_1 = 1$, the latch is closed. When $Clk = 0$, the latch is opened. When the latch is opened, assigning $S_1 = 0$ makes $Q = 1$. Assigning $S_0 = 0$ and $S_1 = 1$ makes $Q = 0$. These two operations are used to set the initial vector all-0 or all-1 in the delay fault test sequence. Setting $S_0 = 1$ and $S_1 = 1$ connects the input $D$ to the output $Q$, directly.

3.3 Delay Fault Testing in Proposed Scan Design

Here, delay fault testing with the proposed scan design is

![Fig. 1](image1)

![Fig. 2](image2)

![Fig. 3](image3)

![Fig. 4](image4)
explained. We explain the sequence from the scan-in operation of a test pattern to the scan-out operation of the test response. There are two types of path delay faults, one is a rising path delay fault for a rising transition at the input and the other is a falling path delay fault for a falling transition at the input. The delay fault test sequence of testing of rising path delay fault is divided into the following three steps.

**Step 1** The transitional vector is scanned in through scan input `Scan In`, and set $S_0 = 0$ and $S_1 = 1$ to set the slave latches all-0.

**Step 2** Set $S_0 = 1$ and $S_1 = 1$ to apply the value stored in the master latch. The operation launches transitions to CUT.

**Step 3** One clock later, the test response is captured. After that, it is retrieved with scan-out operation.

Figure 5 shows the timing chart for $n = 2$. In case of the testing of falling path delay fault, $S_0 = 1$ and $S_1 = 0$ to set the slave latches all-1 in the last 0.5 cycles of Step 1 instead of $S_0 = 0$ and $S_1 = 1$. Since the number of flip flops is $2n$, the scan-in and scan-out operations (Step 1 and Step 3) require $2n$ clock cycles. Step 2 requires 2 clock cycles.
Therefore, the test application time $TAT_{SR}$ is calculated by the following formula:

$$TAT_{SR} = TPSR (2n + 2) + 2n,$$  \((1)\)

where $TP_{SR}$ is the number of the test patterns for the proposed scan design. This formula is the same as that of the broad-side testing and the skewed-load testing. However the number of test patterns is different. Thus, the test application time is different from each other.

The test application time of the enhanced scan design $TAT_{enh}$ is calculated by the following formula:

$$TAT_{enh} = TPSR (4n + 1) + 2n.$$ \((2)\)

The required time for applying a test pattern of the proposed scan design is about the half of that of the enhanced scan design. It is because the proposed scan design does not require scan-in operation of the initial vectors. It gives good influence on the test application time. However, the constraint that the proposed scan design allow only all-0 and all-1 vectors may give bad influence on the number of test patterns $TP_{SR}$. They are evaluated in Sect. 4.

4. Evaluation

It is proved that the two-pattern testing of TRLCs with only all-0 and all-1 initial vectors achieves complete fault coverage [8]. Here, we evaluate the area overhead, the fault coverage, and the test application time.

No scan design for TRLCs has been proposed. For the reference of the evaluation, the area of the proposed flip flop is compared with those of the standard scan design and the enhanced scan design. In addition, the area overhead of TRLCs applied the proposed scan design is compared with those applied the standard scan design and the enhanced scan design. In this evaluation, the standard scan flip flop and the enhanced scan flip flop are comprised of master and slave latches like the proposed scan flip flop. The area overhead of the scan flip flop is calculated by the formula, $100.0 \times (AR_{eval,FF}/AR_{norm,FF} - 1)$, where $AR_{eval,FF}$ is the area of the evaluated scan flip flop, and $AR_{norm,FF}$ is that of the normal flip flop. The area overhead of the scan flip flop is calculated by the formula, $100.0 \times (AR_{eval,2rc}/AR_{norm,2rc} - 1)$, where $AR_{eval,2rc}$ is the area of TRLCs with the evaluated scan design, and $AR_{norm,2rc}$ is the area of TRLCs with no scan design. Note that in this formula, the area of circuits includes the error checker circuit E. Each flip flop is implemented by the standard cells of Rohm 0.35 $\mu m$ design rule. Table 1 shows the evaluation result of the area overhead of the flip flops. The AR and AO columns show the area of each flip flop and the area overhead, respectively.

Table 2 shows the evaluation result of the area overhead of the scan designs. In this evaluation, ISCAS 89 benchmark circuits are used. The circuits column shows the name of each benchmark circuit. The column Normal AR shows the area of circuits with normal flip flops, i.e., applied no scan design. The columns Std. scan, Enh. scan, SR scan show the area and area overhead of circuits applied the standard scan design, the enhanced scan design, and the proposed scan design, respectively. In these columns, the sub-column AR shows the area, and the sub-column AO shows the area overhead. The area overhead of the standard scan design, the enhanced scan design, and the proposed scan design are 12.5%, 29.1%, and 14.6% on average, respectively. The difference of area overhead between the proposed scan design and the standard one is 2.1 percent point on average. The difference of that between the proposed scan design and the enhanced one is 14.5 percent point.

The difference of area overhead between the proposed scan design and the standard scan design is due to the difference of the structure of the slave latches of each scan flip flop. The structure of the slave latch of the proposed scan flip flop is shown in Fig. 4 (a). The structure of the standard scan flip flop is shown in Fig. 4 (b). The normal latch has two inverters, while the slave latch for the proposed scan design has two NAND gates. Therefore, the difference is the same as the difference of area between two NAND gates and two inverter gates. On the other hand, the difference of area between the enhanced scan flip flop and the standard scan flip flop is just a standard latch.

Therefore, the difference between the proposed scan flip flop and the enhanced scan flip flop is calculated by $D_{E-S} - D_{SR-S}$, where $D_{E-S}$ is the difference of the area between the enhanced scan flip flop and the standard scan flip flop, and $D_{SR-S}$ is the difference of the area between the
The test application time of the proposed scan design is reduced by (1 − RTP/TPenh) × 100.0. According to the table, the number of test patterns for the proposed scan design is 42.6% of that of the enhanced scan design. Therefore, the test application time is reduced to about half that of the enhanced scan design. Because the additional function is only the set-reset operation of the slave latch, the area overhead is small. The evaluation shows that the difference of the area overhead of the proposed scan design from those of the standard scan design and the enhanced scan design are 2.1 and −14.5 percent point on average, respectively.

5. Conclusion

This paper has presented a scan design for delay fault testability of 2-rail logic circuits. The proposed scan design provides complete fault coverage in delay fault testing of 2-rail logic circuits. In two-pattern testing with the proposed scan design, the initial vectors are set using the set-reset operation, and the scan-in operation of initial vectors is not required. Therefore, the test application time is reduced to about half of that of the enhanced scan design.

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Table 3 Comparison of fault coverage between the standard scan design and the proposed scan design.

| circuits | #RP | #SP | TATSR | TATenh | FC |
|----------|-----|-----|-------|--------|----|
| b06      | 336 | 335 | 336   | 99.7   | 100.0 |
| b07      | 76,896 | 68,912 | 76,896 | 90.8   | 100.0 |
| b08      | 7,730 | 5,976 | 7,730 | 77.3   | 100.0 |
| b09      | 4,708 | 4,214 | 4,708 | 89.5   | 100.0 |
| b10      | 2,718 | 2,693 | 2,718 | 99.1   | 100.0 |

Table 4 Comparison of number of test pattern and test application time between the enhanced scan design and the proposed scan design.

| circuits | #TP | TPenh | RTP | TATenh | TATSR | RTAT |
|----------|-----|-------|-----|--------|-------|------|
| b06      | 28  | 27    | -3.6| 1,054 | 558   | 47.1 |
| s5378    | 483 | 549   | 13.7| 346,669| 197,998| 42.9 |
| s55932   | 447 | 555   | 24.2| 3,093,567| 1,922,646| 37.9 |
| Average  | -   | 11.4  | -   | -      | -     | -    |
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