Energy-Proportional Data Center Network Architecture

Through OS, Switch and Laser Co-design

Think Green - Turn Off The Lights

Haiyang Han*, Nikos Terzenidis†, Dimitris Syrivelis‡, Arash F. Beldachi§, George T. Kanellos§, Yigit Demir¶, Jie Gu*, Srikant Kandula†, Nikos Pleros†, Fabián Bustamante* and Nikos Hardavellas*

*CS & ECE, Northwestern University
{haidang.han@u.northwestern.edu, jgu, fabianb, nikos}@northwestern.edu

†Aristotle University of Thessaloniki, Greece
{nterzeni, npleros}@csd.auth.gr
dimitriss@nvidia.com

‡NVIDIA, Israel
{gt.kanellos, Arash.Beldachi}@bristol.ac.uk

§Google
yigit@u.northwestern.edu

∥Microsoft Research
srikanth@microsoft.com

Abstract—Optical interconnects are already the dominant technology in large-scale data center networks. However, the high optical loss of many optical components coupled with the low efficiency of laser sources result in high aggregate power requirements for the thousands of optical transceivers used by these networks. As optical interconnects stay always on even as traffic demands ebb and flow, most of this power is wasted. We present LC5DC, a data center network system architecture in which the operating system, the switch, and the optical components are co-designed to achieve energy proportionality.

LC5DC capitalizes on the path divergence of data center networks to turn on and off redundant paths according to traffic demand, while maintaining full connectivity. Turning off redundant paths allows the optical transceivers and their electronic drivers to power down and save energy. Turning full connectivity hides the laser turn-on delay. At the node layer, intercepting send requests within the OS allows for the NIC’s laser turn-on delay to be fully overlapped with TCP/IP packet processing, and thus egress links can remain powered off until needed with zero performance penalty.

We demonstrate the feasibility of LC5DC by i) implementing the necessary modifications in the Linux kernel and device drivers, ii) implementing a 10Gbit/s FPGA switch, and iii) performing physical experiments with optical devices and circuit simulations. Our results on university data center traces and models of Facebook and Microsoft data center traffic show that LC5DC saves on average 60% of the optical transceivers power (68% max) at the cost of 6% higher packet delay.

I. INTRODUCTION

Optical interconnects have emerged as a promising solution to meet the growing demand for high-bandwidth, low-latency, and energy-efficient communication in data centers [1], [31], [48]. A significant fraction of the energy consumption in these networks can be attributed to the laser sources and laser drivers. As we argue, most of this energy is wasted.

For example, a typical 64-port switch with 220 W peak power draws on average 140 W [4] and employs 10G SFP+ optical transceivers at 1 W per port. With this configuration the switch consumes a third of its power on optical transceivers. QSFP (40G) transceivers consume as much as 3.5× more power, raising the power ceiling even further. However, most of the laser energy is wasted. Unlike traditional interconnects that expend most of their energy only during packet transmission, optical interconnects are always on and consume power, even during periods of inactivity. In reality, the interconnect often stays idle for long periods: compute-intensive workloads underutilize the interconnect (common in scientific and many analytic workloads), and servers in data centers often stay idle or exhibit load imbalances (data centers are typically 20–30% utilized [6], [7]).

The natural solution is to turn off the transceiver of an idle link to save energy, and turn it back on when packets arrive to facilitate communication [32]. A naive implementation of this “laser gating”, though, risks exposing multiple laser turn-on delays to the end application as a packet typically crosses multiple links to reach its destination, significantly increasing packet latency and lowering performance.

We propose to hide the laser turn-on delay by capitalizing on the path diversity of modern data center interconnects. To service high levels of traffic across a large number of nodes, data centers typically exploit scalable network topologies. For example, full-optical Clos networks are widely deployed in Facebook [48], Google [51] and Microsoft [31] data centers, and flattened butterfly topologies have been proposed as a cost-efficient alternative by Google [1]. All these topologies provide path diversity, i.e., there are multiple paths between any source-destination pair. Instead of turning off links arbitrarily and severing end-to-end paths, which exposes the laser turn-on delay, we propose to turn off only redundant links when utilization is low, and turn them on again when the aggregate workload needs more bandwidth. Maintaining full connectivity removes the laser turn-on latency from the critical path and results in minimal performance degradation.

We also propose to control the server-to-ToR (Top of the Rack) switch links by intercepting socket write calls at the OS level and raising a signal to the Network Interface Card (NIC) lasers to turn on. The TCP/IP processing latency is high enough that allows for ample time to notify the server NIC of the impending traffic. By the time the data are ready to be sent, the laser is already on and locked at the appropriate frequency, thereby allowing the node to save energy with zero
performance penalty.

The main idea of laser gating is not new. Such techniques have been proposed before for on-chip interconnects [19]–[22]. An earlier study capitalizing on path diversity for laser control in on-chip interconnects [20] was extended to data centers but only as a conceptual study; no evaluation was performed on traffic similar to modern large-scale data centers (only a university data center traffic trace was used), and the feasibility of the technique was not proven or discussed. After all, the latency to perform network control plane changes has been previously shown to be in the ms scale [27], which could render such a technique useless, and the latency to perform link retraining for Clock and Data Recovery (CDR) can be prohibitively high.

In this paper we aim to set the record straight. We evaluate laser gating on multi-stage data center networks with a Clos architecture similar to the one found in modern hyperscale data centers [31], [48], [51] using traffic patterns that closely approximate real-world traffic [31], [36], [48]. We demonstrate that control plane changes can be performed in a matter of ns by implementing LC\$\text{DC}$ on a $6 \times 6$ 10.8 Gbit/s switch on an FPGA. We implement a device driver on a modern Linux operating system and kernel changes that intercept socket write calls to raise a signal and alert the NIC of imminent outgoing traffic. We measure the latency of the TCP/IP processing and show that the NIC has ample time to turn on its transceiver while the outgoing packet is being prepared. Finally, through a combination of physical experiments and analog SPICE simulations of laser driver circuit models, we show that optical transceivers and their electronic drivers can be turned on at μs scales. Collectively, these results demonstrate that laser power gating at the data center scale is indeed feasible, and can be driven by the OS and network switch layers. We then estimate the energy savings that can be achieved on a variety of scenarios through simulations and technology projections.

More specifically, our contributions are:

- We propose LC\$\text{DC}$ (Laser Control for Data Centers), a data center network system architecture in which the operating system, the switch, and the optical components are co-designed to achieve energy proportionality.
- We demonstrate the feasibility of employing LC\$\text{DC}$ at servers and global switches through modifications in the Linux kernel and device drivers, switch design on FPGA boards, physical experiments with optical devices, and analog circuit simulations.
- We develop a data center traffic generator that models the traffic exhibited at Facebook and Microsoft. We show that our traffic generator produces CDFs of flow size and flow intervals that closely match real-world traffic.
- We evaluate LC\$\text{DC}$ on models of Facebook and Microsoft data center traffic, as well as traffic traces from a university data center. LC\$\text{DC}$ saves on average 60% of the optical transceiver power (68% max) at the cost of 6% higher packet delay.
- As servers and cooling, electrical and mechanical systems become increasingly more energy efficient, we project that the network will command a larger fraction of the overall data center energy consumption. We estimate the potential savings of LC\$\text{DC}$ on a hypothetical future datacenter that applies multiple server-level energy optimizations. We find that LC\$\text{DC}$ can save 12% and 21% of the data center energy on average when deactivating transceivers or transceivers and switch PHY and NIC electronics, respectively, even for cases where the server utilization approaches 70%.

II. Motivation

Power and energy efficiency have been at the forefront of research in circuits and computer architecture for at least 15 years [11], [25], [52]. Innovations in these fields coupled with technological advances in materials, semiconductor processes and packaging yield lower-power devices at each technology node [9], [34], [40], [55]. The end result is the rapidly increasing energy efficiency of server components, including memory, storage, processors, and ultimately the servers themselves. Simultaneously, the high power demands of modern data centers has pushed data center operators to drastically reduce power inefficiencies. As a result, modern state-of-the-art data centers reduced the power overhead for cooling, electrical and mechanical systems from more than 2 × a decade ago to only 6% today [24], [30], [42]. As servers deliver increasingly higher performance per Watt, and data center overheads are aggressively eliminated, their contribution to the overall data center power consumption drops, exposing other components that have not yet received similar attention [32]. Data center networks are one of these components, and its relative power consumption rises as innovations in other sectors reduce the power draw of other data center components.

Figure 1 shows the breakdown of data center power as various optimizations are applied on servers. For generality, we carry out the same study across various network designs from the literature: a Clos Facebook site [48], a Flattened Butterfly interconnect by Google [1], and three Fat-Tree networks derived from [28] that are either readily available using off-the-shelf components (Fat-Tree 1), or require board and chassis engineering for higher efficiency and lower cost (Fat-Tree 2), or require board, chassis and new ASIC design (Fat-Tree 3). All designs are modeled using the exact component counts and connectivity described in their respective publications. Figure 1 breaks down the data center power into:

- Server systems
- Switch ASIC and CPU chips (28 W per switch) [28]
- Switch network card (NIC) electronics (10 W) [1]
- Switch PHY chips that implement the Layer 1 protocol exposed by the switch (0.8 W, one PHY per port) [28]
- Optical transceivers on switch and NIC card ports, assuming 1 W for 10G SFP+, 2.4 W for 40G QSFP [28]

The figure excludes the overhead for cooling, electrical and mechanical systems within the data center, as the additional overhead these systems impose is proportional to the power draw of the server, storage and networking equipment. We note that modern hyperscale data centers often achieve Power
Usage Effectiveness (PUE) of 1.06 [24, 30, 42] and report a comprehensive trailing twelve-month PUE of 1.10 [30] across all large-scale data centers, in all seasons, including all sources of overhead. Thus, the additional overhead of large-scale data centers nowadays represents a relatively small fraction of their overall energy consumption.

Most readers would be familiar with the left-most stacked bar for each network, where 92–95% of the power is consumed by the servers and only 5–8% goes to the interconnect. However, this assumes that all servers run at 100% utilization and draw peak power all the time. In reality, servers are typically only 20–30% utilized [6, 7]. Thus, their contribution to data center power is lower, and the relative importance of other components grows. The second stacked bar shows this effect assuming typical servers circa 2013 [26].

The third bar shows the effect of 30% server utilization on a best-of-class modern server that is nearly energy-proportional: the Lenovo Think System SR665, which currently has the highest performance per Watt as measured by an audited SPECpower benchmark [53]. This server expends 58% of its power at 30% utilization (compared to 70% for the 2013 server [6]). The fourth bar continues that trend and models a fully energy-proportional server at 30% utilization [6, 7, 26] at which point it consumes 40% of its peak power. On average, a data center with fully energy-proportional servers at 30% utilization seems to spend about 86% of its energy on the servers and the remaining 14% on the network.

The following bars apply successively more optimizations on the server components (and if applicable the switch and NIC electronics) to account for the transition from 7 nm to 1.5 nm CMOS technology following IRDS projections [10, 34]; the use of modern memory technology (e.g., Micron’s 3D hybrid memory cube, HMC) [10, 46]; the introduction of 16-die-stacked 3D NAND Flash for solid-state drives [3, 55]; and the employment of specialized computing which is modeled after the Catapult project [47] in Microsoft that deployed FPGAs in production data centers to off-load computations from conventional general-purpose processors.

Finally, the last two bars show the impact of applying various recent technologies such as DRAM refresh reduction [39], DRAM idle power-off [56], memory disaggregation [44], and near-memory processing [38]. We model the impact of these optimizations by employing them only on the appropriate components, following the typical power profile of data-center-class servers [26] and switches [4, 28].

As Figure 1 indicates, with each optimization the relative power consumption of servers drops, to the point where the network becomes a major component. Our projections indicate that, unless something is done, the thousands of transceivers employed in a data center network will account for 20% of the data center power consumption on average across network designs, after these series of optimizations are applied on the servers. Moreover, the combined switch PHY chips, server NIC electronics and transceivers will account for as much as 46% of the data center power. Thus, we argue it is time to start optimizing the network not only for latency, bandwidth and cost, but also for power and energy efficiency.

It is important to note that the optimizations we model in this study are carefully selected to be conservative and readily available, and they are solidly backed by experimental characterization of existing products. The technology projections conform to the roadmap that the semiconductor industry collectively sets every year since 1993 [10, 34], the memory and SSD devices are already commercially available [16, 45, 46, 55], nearly full-energy-proportional servers are commercially available today [53], and some data centers already deploy specialized computing (e.g., Microsoft’s Catapult [47], Google’s Tensor Processing Units [35]).
To capture a wider range or projections, we also include two more sophisticated energy-efficiency optimizations that have been in active development in industry for more than a decade, and while they are not mainstream products yet, they are in advanced stages of development. These optimizations include near-memory processing [38] and disaggregation [44]. There is a large number of much more aggressive optimizations that we explicitly chose not to include, as their ability to scale up to production at reasonable cost is unknown, or they are not a good fit for hypercale data centers, or simply because they are not commercially available yet, despite their high potential (e.g., STT-RAM, PCM, near-threshold-voltage processors, spintronics, neuromorphic processors, and chip-and board-level photonics).

III. LCSDC ARCHITECTURE

We propose LCSDC to minimize the amount of power spent on optical transceivers employed in switches and server NIC cards by turning them off when they are not needed. Moreover, we can extend the design of LCSDC to also put the switch PHY chips and the server NIC electronics into a low-power state at the same time that the laser is switched off. While we do not study this extension in this paper, it can address as much as 46% of the projected data center power consumption (Figure 1), even after accounting for the CMOS scaling of the PHY and NIC electronics.

To minimize the performance impact of waiting for the lasers to turn on, LCSDC deactivates only redundant links, while maintaining full network connectivity. As there is always a path connecting any pair of nodes, packets can still reach their destination while links are active. LCSDC monitors the interconnect traffic and turns off links when the utilization is low to save energy, and activates additional links when the utilization is high to increase performance.

A. LCSDC Operation at the Switch Level

LCSDC is applicable to any network topology with path diversity. In this paper we evaluate it in a network similar to a site in the Facebook data center [48]. Figure 2 presents the network design. Each rack has 48 nodes which connect to a Rack Switch (RSW). 32 RSW’s form an Cluster and connect to 4 Cluster Switches (CSW). 4 Clusters (16 CSWs) connect to 4 “Fat Cat” Routers (FC) to form a site. The RSWs have 48 10G (downlink) input-output ports and 4 10G uplinks to CSW intermediate routers (12:1 oversubscription). In turn, the CSW’s provide 4 40G uplinks to FC switches (2:1 oversubscription). Each set of CSWs within a cluster and the FCs are connected on a ring formed by 8 10G links and sixteen 10G links respectively, for load balancing.

LCSDC controls each tier independently. Each RSW has 4 uplinks to connect to all the CSWs in its cluster (path divergence). Each one of these uplinks defines a Stage. When we say that stage k is active, we mean that links 1 through k are active. Initially only one stage per RSW is active. LCSDC on each switch estimates network traffic by monitoring the buffer depth (buffer utilization, aka queue backlog) of its active links, which is an accurate and lightweight method [12]. When a buffer’s depth exceeds a tunable threshold (high watermark), the RSW turns on an additional stage to provide higher bandwidth and minimize queueing delay. The switch sends a control message through the already active stages to the corresponding CSW informing it of the new stage activation, and once its transceiver is active and has received an acknowledgement from the CSW that the receiving side is active, it starts using the additional link.

The newly activated stage turns off when the RSW that activated it becomes underutilized, i.e., its buffer utilization falls below a low watermark. In that case, LCSDC realizes that the additional bandwidth provided by the redundant link is not necessary, and should turn it off. The RSW stops receiving outgoing messages in this port, serves all the packets in its buffers, and then notifies the corresponding CSW with a stage turn-off message which deactivates the last activated stage. Once the CSW acknowledges the link deactivation, RSW turns off its transceiver too. Link activation and deactivation at CSWs and FCs is performed similarly.

LCSDC adaptively routes traffic through only the active stages which achieves load balancing, turns on lasers on the side and hides their turn-on delay, and avoids unnecessary link activation which maximizes the energy savings.

B. LCSDC Switch Architecture

Figure 3 shows the architecture of the LCSDC switch. LCSDC is a combined input-output queued switch (CIOQ) [13]. At the input, buffering relies on the hardware queues of RGMII MAC, while at the output the design features one RAM-based queue per physical port. The LCSDC datapath is 64-bit wide and adds a single annotation...
1) Dataplane Pipeline Stages: The Ethernet frames are pulled from RGMII MAC queues that drive the physical interfaces using a round robin arbiter. Besides the physical input ports, the switch features a virtual port that interfaces a 2-port memory to the arbiter. The memory is pre-programmed with all flavors of control packets that are forwarded to other switches to initiate LC₅DC stage changes. The arbiter polls the virtual port out-of-order to prioritize the forwarding of generated control packets.

In the next pipeline stage the processing differs depending on whether the packet is LC₅DC control or not. The LC₅DC control packet is an ethernet frame where bytes 13-14 form the LC₅DC Ethernet type (0x9100). The next 8 bytes contain the senderID (4 B), the stageID (2 B), and the TTL (2 B). The packet is then padded to the minimum ethernet frame size. The stageID denotes the LC₅DC stage to be enabled and the possible values are deployment-wide agreed. The TTL designates the number of switching layers that the control packet may flow through before it is discarded. This approach simplifies the distribution scheme by allowing control packets to get forwarded from all output ports of each switch without worrying for endless loops. Accordingly, the control packet processing checks the stageID and sends the appropriate notification to the LC₅DC stage enabling component, updates the TTL and drops the packet (if zero) or propagates it for forwarding. Finally, the senderID designates the control packet sender, so it is used to determine if the packet was generated in the local switch. If it was, it is directly forwarded to the scheduler because the stage transition process is initiated before control packet generation.

The non-local packets initiate a Content Addressable Memory (CAM) lookup to match the packet destination Ethernet MAC address with a logical port, which is a deployment-unique identifier of the destination switch where the packet recipient is attached. This switch addressing scheme is internal to LC₅DC and has to be configured by the control plane (Section III-B2). For multicast support, special logical port identifiers are programmed by the control plane for each multicast tree. Accordingly, the logical port identifier is pushed to the packet annotation space and a multicast bit is set when needed before the packet propagates to the scheduler pipeline stage.

The scheduler load-balances the incoming traffic over the available output physical port queues based on the packet destination and the LC₅DC stage that is enabled. As the provided packet destination is a logical port, the scheduler has access to a series of binary CAM tables, one per LC₅DC stage, to determine the physical output port options. These CAM tables take the logical port as input and provide a binary map at the output where all the possible physical ports that may be used for this destination, based on the enabled LC₅DC stage, are one-hot encoded. The scheduler uses each time a single CAM that corresponds to the currently enabled stage. A simple weighted scheduling algorithm chooses the output queue with the minimum backlog from the ones that belong to the given map. In case of multicast packets, the scheduler places a copy to all output queues of the encoded map, which is encoded accordingly to implement the multicast. This step
concludes the LCSDC datapath operation.

Moreover, three peripheral components orchestrate the LCSDC stage transitions. First, the queue backlog monitor component inspects all the output queue backlogs. When a backlog exceeds an administrator defined high watermark, the stage up trigger is sent in parallel to the other two components: i) the stage enable component and ii) the stage enable control message generator. The former immediately drives the electronics to enable the next stage and when it receives a stage ready signal it enables the CAM stage table that corresponds to the currently active output ports. The latter activates the virtual input port so that the arbiter pulls the proper control packet to notify the rest of the deployment for the state change. If the backlogs become low, the backlog monitor sends to the stage enable component the stage down trigger, which immediately enables the appropriate CAM table while it requests the shutdown of specific physical ports.

2) LCSDC Control Plane: The LCSDC switch requires control plane support that has overview of the whole network deployment and device topology in order to provide the required forwarding information on all CAM tables, the thresholds on the backlog monitors and the programming of the control packets for the underlying switch fabrics. For this particular purpose the current design features an Altera Avalon bus interface that connects the aforementioned components to the Altera NIOS processor, a softcore processor solution that is provided by the FPGA platform we use. Therefore, low-level software-based control plane support can be realized on each switch, which can then be integrated with data center network orchestration tools like OpenStack Neutron according to the SDN paradigm.

C. OS and Device Driver Design for Node-Level LCSDC

In addition to controlling the redundant links, LCSDC independently controls the transceivers on each server’s NIC card, by using a modified network card device driver which is controlled by the system as a kernel module. LCSDC intercepts the Linux sendmsg() system call and replaces it with our version of sendmsg() by modifying the system call table at driver module initialization. Upon a user-level socket_write() call, the driver signals its laser to turn on and then invokes the original sendmsg() function. While the laser turns on, the payload goes through the TCP/IP stack processing. By the time the driver-specific transmit function is called to transmit over the fiber, sufficient time has elapsed for the laser to be fully operational and transmit the data. Changes to the Linux driver and kernel module is minimal at around 200 lines of code.

IV. FEASIBILITY STUDY

A. Feasibility at the Device Level

1) Optical Transceiver Turn-on Delay: The datacom transceiver modules that are largely deployed in current data center implementations mainly rely on SFP+ modules for up to 10Gbit/s link bandwidths and QSFP modules, which is a quadruple form of SFP+, for link bandwidths in the range of 40Gbit/s to 100Gbit/s. The simplest SFP+ form of transceiver is shown in Figure 4a and comprises a transmitter side which includes a laser component followed by the laser driver circuitry, and a receiver side that includes a photodetector followed by the pre-amplifier, also called trans-impedance amplifier (TIA), and the post-amplifier. Optional additional circuitry may include a CDR (clock and data recovery) circuit in both transceiver sides.

In such transceiver configurations, the transmitter turn on/off timings are denoted as TxDisable assert time / Tx_negate assert time and are defined in the SFP+ multisource agreement (MSA) [50]. The MSA specifies that the transmitter turn on/off timings are 100µs and 1 ms respectively, while the receiver turn on/off times denoted as Rx_LOS assert delay / Rx_LOS negate delay are 100µs each. However, the MSAs have set the timing boundaries well beyond any safety margins of stable operation in order to fully relax the design and cost requirements of the transceivers [50]. In fact, though both optical and electrical components comprising the transceivers allow for significantly faster operations, this has never been a design objective for commercial manufacturers of Datacom transceiver modules, and hence they are not optimized for it.

This becomes evident for transceivers in the SFP+ form-factor that are deployed in PON (Passive Optical Network) applications, such as the 10GE-PON SFP+ transceivers. For these transceivers, the necessity for burst operation has led to their commercial implementations exhibiting turn on/off times of 512 ns each [18], [23], [33]. These transceivers retain all other Datacom SFP+ specifications, such as power consumption, bit rate, etc, and thus demonstrate that transceiver for Datacom applications (e.g., data centers) can also be implemented with equally fast µs-scale turn on/off timings.

To provide further evidence that the optical components can be turned on/off at such high speed, we set an experimental
setup of a manufactured VCSEL device and a simulation model of the electrical circuitry to assess the minimum timings required for turning on/off such transceivers. Figure 4b shows the experimental setup that reveals the turn on/off timings for the optical components. We have chosen the 22 GHz VCSEL laser of [37] as the optical source, since VCSELs are typical laser sources for Datacom transceivers. We consider the non-return-to-zero (NRZ) direct modulation bandwidth as the laser turn on/off frequency. A pseudo-random binary sequence with a word length of $2^7 - 1$ and a bit rate of 35 Gbit/s was generated from a commercial pattern generator. The output of the pattern generator was a single-ended NRZ signal with a swing of 650 mV peak-to-peak, while a bias tee superimposed this data signal on a DC bias current of 12.4 mA. This setup substitutes the laser driving circuitry of Figure 4a, and defines the electrical signal specs to be applied to the VCSEL through RF probes. The optical signal generated by the VCSEL was then pre-amplified through an erbium-doped fiber amplifier (EDFA) and launched to a Finisar XPDV3120R 70GHz photodetector with 3V bias. The electrical signal at the output of the PD was then captured by an Infinium sampling scope, revealing a clear eye-pattern for up to 35 Gbit/s as shown in Figure 4c. This implies that both transmitter and receiver optical components have the ability to be turned on/off at timing below 15 ps respectively.

The experiment above demonstrates that the turn on/off speed achievable by laser devices is well below the µs-scale that LC-SDC requires. The electrical integrated circuit for the receiver can also be sufficiently fast for LC-SDC application. An electrical circuit that even includes a burst mode CDR has been recently shown to exhibit optical power calibration in 12.5 ps and phase lock in 18.5 ps [49], both well below 1 µs. We emphasize that switching OFF links and their lasers does not modify the links; the link characteristics are the same when the link is powered up again. This makes the link amenable to clock phase caching, which was recently demonstrated to provide clock and data recovery times below 625 ps [5], [14], [15] on a real-time prototype with commercial transceivers, comfortably within the µs requirement of LC-SDC. This result was further validated against temperature variation and clock jitter [15], demonstrating its resilience and applicability to real-world scenarios.

To fully assess the lower possible boundaries of the transceiver timing specifications, the only remaining component in our device-level feasibility study, we derived a SPICE-based analog simulation model for the laser driver depicted in Figure 5a. In this configuration, we considered the RLC electrical circuit equivalent for the VCSEL as provided by Finisar in [29].

2) Electronic Circuit Simulation: We created a spice simulation in a 45nm CMOS technology following the specification provided from VCSEL laser model [29]. As shown in Figure 5a, the model contains simple lumped components for bonding pad $C_{PAD}$ (68.3 pF), distributed resistance components $R_{P1}$ (215Ω), $R_{P2}$ (147Ω), and $R_{J}$ (1690Ω) for mirror, and combined junction and oxide capacitance $C_{JOX}$ (34 pF). This simplified lumped model has been verified from DC to high frequency (25 GHz) to match well with measured responses from the physical VCSEL laser [29]. In our simulation, a small CMOS driver with transistor sizes of 10 µm was used to turn on and off the laser block. Simulation in Figure 5b shows that the laser junction voltage can be driven within 25 ns with a large signal magnitude using our small CMOS driver. This simulation shows that such a laser source can be power gated well within 100 ns or 1 µs time window.

**B. Feasibility at the Switch Level**

Similar to transceiver modules, commercially available switches do not allow for fast nanosecond-scale updates to port maps or rules. While technologically this should be feasible within a few processor cycles, commercial designs never had the incentive to optimize it to a few nanoseconds.

To demonstrate the feasibility of LC-SDC at the switch layer we implemented a prototype of the described LC-SDC pipeline architecture in Verilog as a 6×6 switch, with small-sized CAMs (100 entries each) and support for four LC-SDC stages (Figure 3). The design targets an Altera Stratix V GT platform where it achieves a clock rate of 169.32 MHz, providing a 10.8 Gbit/s backplane. The overall latency from the time a packet flit enters the pipeline until it is delivered to the output queues is 7 cycles (2 cycles for the logical port lookup, 2 for the stage out port map lookup, 2 for the scheduler, and 1 for placing at the output queue). The cycle count is expected to grow with the number of output ports because the scheduler checks all backlogs before queueing a packet.

Our design also demonstrates fast stage trigger generation. When the backlog monitor observes a threshold violation (checked on every cycle) it signals the stage enable component in the same cycle (<5.8 ns delay). When a control packet that initiates the stage change appears at the input, 2 cycles elapse before the proper flit is parsed (12.8 ns). As soon as the stage enable component receives the ready signal from the output ports, it enables the appropriate stage CAM lookup table on the next cycle so that the next packet (whenever it arrives) is forwarded according to the new stage.

Our FPGA prototype demonstrates that it is feasible to implement a fast LC-SDC switch with ns-scale latencies. ASIC implementations would be even faster than our FPGA implementation, but they are outside the scope of this paper.
C. Feasibility at the Node Level

Using our modified Linux network device driver we measured the latency between the hypothetical “laser turn on” command that the device driver will issue to the NIC transceiver, and the subsequent call to the device-specific transmit function that starts sending the bits through the physical link. To do this we took timestamps with our version of the `sendmsg()` system call and NIC device transmit function were invoked. Our test-bed consists of an Intel 82579LM Ethernet card and an Intel Core i5 2520M 2.5 GHz processor running Linux kernel 4.2.0 on Ubuntu 15.10. We measured a mean elapsed time of 3.2 µs over 100k samples on a completely idle system at runlevel 1 to minimize perturbations from other kernel services, `TCP_NODELAY` to eliminate small packet aggregation, and with hyper-threading, frequency governors, and all but one cores disabled to minimize perturbations due to thread migration or core frequency changes.

Our results corroborate independent measurements in literature of 3.7 µs for a packet to traverse the TCP/IP stack [41]. These results independently measured that it takes 950 ns for a process to send a message to the socket interface on a connection that has already been established. Evoking a socket write begins the TCP layer to initiate transmission, copy the application buffer into the transmit queue in kernel space and prepare a datagram for the IP layer (260 ns). Then the IP layer does routing, segmentation, processes the IP header, and eventually calls the network device driver (550 ns). The network device driver constructs the output packet queue entry and calls the precise hardware implementation of the NIC card to transmit the frame by passing a pointer to the packet descriptor (430 ns). This causes a control register write within the NIC to set up a DMA transfer to fetch the pointer, and when it completes control is handed to the NIC card (400 ns). Another 760 ns are consumed by the NIC to process the core register write, interpret the descriptor, and based on the descriptor initiate a DMA to fetch from main memory the data of the packet to transmit. Each 64-byte cache line access to memory takes an estimated 400 ns to propagate from the PCIe signal pins to memory and back. Thus, it takes a total of 3.75 µs for an application to launch a packet onto the fiber interface. Thus, the server’s NIC card will have ample time to turn on its laser and it will impose no laser turn-on delay to the sending process.

V. EXPERIMENTAL METHODOLOGY

We model the data center network in Figure 2 using the BookSim cycle-accurate network simulator [17] that we modified in-house. We faithfully model all traffic, including...
Fig. 8. Breakdown of partial network activation. The legend indicates the fraction of the network links that are on.

Fig. 9. LCsDC transceiver energy savings.

Fig. 10. Impact of LCsDC on packet latency.

the fraction of the time each link is deactivated. We set the high watermark at 75% buffer utilization for stage activation, and the low watermark at 22% buffer utilization for stage deactivation (experimentally determined to balance energy savings with network performance).

VI. EXPERIMENTAL RESULTS

A. Input Data

Figure 6 shows the data traffic injected into our simulated network. We created a traffic generator that produces traffic that closely approximates the network traffic originating from large-scale data centers in Facebook [48], Microsoft [31], [36], as well as in higher education settings [8]. Comparing the distribution of traffic from our generator with the large-scale data center traffic from published measurements [31], [36], [48], we confirm that they have similar CDFs, as is shown in Figure 7. We measure the Pearson r coefficient to be between 0.979–0.992 for the flow size CDF, and 0.894–0.998 for the flow interval CDF. Thus, our simulations are conducted under conditions that closely approximate real-world environments.

B. Results

Figure 8 shows the portion of the network that is activated during the execution of the traffic workload for each modelled traffic. Most traffic types exhibit sparse and bursty packet injection trends. Thus, LCsDC finds windows of low utilization to deactivate a link, and 87% of the time on average half of the network is deactivated, indicating the potential to achieve significant power savings. The Microsoft data center traffic presents the most challenges, but LCsDC still manages to turn off half of the network half the time.

As a result, LCsDC saves on average 60% of the optical transceivers’ energy (Figure 9). The lower energy savings relative to the time breakdown (Figure 8) are due to the fact that while a transceiver is in the process of turning on or off, the link is still considered deactivated, but we conservatively charge the full transceiver power consumption to the network. The energy savings come at the cost of 6% higher average
packet latency (Figure 10) as queueing in network buffers may slightly increase, which we argue can be largely absorbed by the application layer.

Following the analysis in Section II we estimate the data center energy savings of LC\textsuperscript{5}DC in Figure 11. We consider the data center to be at an average utilization of 30\%. Additionally we calculate the energy savings of LC\textsuperscript{5}DC in cloud servers, which are shown to typically have higher utilizations at 40\%-70\% [54]. Figures 11b and 11c show energy savings at 50\% and 70\% utilization, respectively. For data centers at 30\% utilization, assuming the data center servers are optimized for energy while maintaining high performance, LC\textsuperscript{5}DC can save 12\% of the data center energy by deactivating links when they are not needed. It is also possible to extend LC\textsuperscript{5}DC to deactivate or put into a sleep mode the switch PHY chips and the server NIC electronics whenever the corresponding link is deactivated. With that extension, LC\textsuperscript{5}DC’s data center energy savings can reach up to 27\% on average, even after accounting for the CMOS scaling of the switch PHY and NIC card electronics. While we do not directly explore turning off the switch PHY and NIC card electronics, it is a promising future direction for this work. For cloud servers with utilizations of 50\% and 70\%, LC\textsuperscript{5}DC can respectively save 13\% and 12\% of total data center energy by just turning off links. By deactivating the switch PHY and NIC card electronics, LC\textsuperscript{5}DC can respectively save 23\% and 21\% of total data center energy.

VII. RELATED WORK

Heller et. al propose ElasticTree [32], a power manager that dynamically adjusts the set of active links and switches to satisfy data center traffic while saving energy. However, ElasticTree cannot hide the high latency of rebooting a switch, and thus it is only applicable to large-grain traffic ebb and flow, while LC\textsuperscript{5}DC exerts very fine-grain control over link activations. Ananthanarayanan and Katz [2] present a switch design that estimates traffic to power down ports when possible. Unlike LC\textsuperscript{5}DC, it may send packets to sleeping ports and expose long delays to the application.

Laser gating has been proposed before for on-chip interconnects [19]–[22], which however do not present the complex-
We demonstrate LC5DC’s feasibility at all levels (electrical circuitry, optical devices, node-level architecture, and switch architecture) and show that it can save the majority of the network energy in a data center.

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