LETTER

Fully integrated receiver for free-space visible light communication

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Abstract A fully integrated visible light communication (VLC) receiver is presented in this paper. The proposed VLC receiver chip is designed for free-space communication. Utilizing a laser diode as light source, the measured -3dB bandwidth of receiver is 420MHz over 0.5m distance without lens. The integrated receiver is manufactured in an UMC 0.18μm CMOS process, and the chip area is 889 × 570 μm². This receiver chip can be used in VLC systems with the following advantages: suitable for VLC free-space channel, low requirements for focusing and alignment, low cost, low power-consumption, compatible with standard CMOS technology, and high integration-density.

key words: Visible light communication (VLC), receiver, avalanche photodiode (APD), free-space, CMOS
Classification: Integrated optoelectronics

1. Introduction

Simultaneously offering data communication and indoor illumination make VLC gain plenty of attention in the past few years [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13]. In the future, VLC has the potential to play a major part in smart home and next generation communication networks. It is a significant work to increase the achievable data rates and make it can be integrated within existing network infrastructures. The future of VLC systems depends on the ability to fabricate low cost transceiver components and to realize the promise of high data rates. Integrated high-speed solutions for the VLC source driver and receiver are required [14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26].

A research team in Japan proposed a VLC system based on phosphor LED transmitter and a CMOS camera receiver. Using on-off keying (OOK) modulation, the data-rate is 10-20Mbps [27]. Another 24Mbps VLC system based on ordinary phosphor white LED without pre-emphasis, a commercial silicon PIN photodiode (PD) and CMOS receiver is also presented [28]. Due to the limited communication bandwidth of phosphorescent LED, the achievable data-rate of VLC system is not fast enough. Due to the long photoluminescence lifetimes of the phosphor, the communication bandwidths of phosphor LED is only a few MHz. This is the bottleneck for high speed data communications. Based on μLED [14] and laser diode (LD) [29][30], which have much better modulation bandwidth than LED, the data-rate of integrated VLC system can be improved.

For the existing optical receivers, the area of detector is small, for the purpose of achieving higher communication speed. However, the receiver with small detector is not suitable for free-space VLC, mainly due to the low optical power density and high requirements for focusing and alignment. Therefore, we proposed a fully integrated VLC receiver with much larger avalanche photodiode (APD), which is more suitable for free-space VLC. We also measured and analyzed the trade-off relationship between the area and frequency response of APD. Based on the study of APD, we proposed a fully integrated VLC receiver with active inductor and post-equalization for frequency compensation of the large area APD.

This paper is organized as follows: Section 2.1 presents the trade-off relationship between the area and frequency response of APD, Section 2.2 presents the design of receiver circuits. Experimental results are reported and discussed in Section 3. Finally, conclusions are drawn in Section 4.

2. Design of the proposed VLC receiver

2.1 APD array

In this section, we measured and analyzed the frequency response characteristics of APDs.

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The structure of APD in this paper is shown in Fig. 1. Generally, there are mainly two kinds of APD structures for visible light detection. One is P+/N-well junction, and the other is N-well (or deep N-well)/P-substrate junction. The junction depth of N-well/P-sub is much deeper than P+/N-well. The response speed of P+/N-well APD is faster than N-well/P-sub APD. Therefore, we utilized the P+/N-well structure for the APD design.

Three APDs of different size are fabricated in UMC 0.18μm CMOS process, which is shown in Fig. 2. The dimensions of the three APDs are 75μm×75μm, 150μm×150μm and 300μm×300μm, respectively. The connection wires from every APD unit to output electrode are designed to be the same, in order to minimize the influence of electrode connection wire. The APD chip is packaged on a PCB using bonding wires as the DUT. Because the output photocurrent of APD is too weak to be measured directly with a testing instrument of 50Ω port. Therefore, a high-speed transimpedance amplifier (MAX3665) with 8kΩ gain is used for photocurrent amplification. The dimensions of the DUT are 5 cm×6 cm. The DUT is shown in Fig. 2. The chip capacitors on the DUT are used to filter off the high-frequency components of the DC power supply.

A LD (OSRAM PL TB450B) is used as the light source for measurement. The -3dB bandwidth of LD is more than 1GHz, which is enough for our experiment. The network analyzer (Agilent E5062A) is utilized for frequency response measurement. Fig. 4 shows the experiment results of frequency response. For the low-frequency band, larger area means higher frequency response value. The start frequency response value of 300μm×300μm APD is -5dB. The start frequency response value of 75μm×75μm APD is only -50dB, which is very close to the background noise of free-space VLC (approximately -60dB). Therefore, 75μm×75μm APD maybe not suitable for free-space VLC. The -3dB bandwidth of three APDs are 155MHz, 300MHz and 380MHz, respectively. Considering the response and bandwidth at the same time, we finally choose 150μm×150μm APD for the VLC receiver design.

2.2 Design of the receiver circuits
Utilizing the 150μm×150μm APD, we proposed a fully integrated VLC receiver with active inductor peaking and post-equalization.
Fig. 5 shows the block diagram of the proposed VLC receiver chip. The receiver is made up of APD, differential transimpedance amplifier (TIA), post-equalization (PEQ), limiting amplifier (LA) output buffer and DC-offset canceller. The dummy APD is covered by the top metal. The active APD is used to detect the visible light signal. Both the dummy APD and the active APD have the same size. The post-equalization is added to compensate for the bandwidth limitation of APD. Next, the detail of circuits is discussed.

The circuits of receiver are shown in Fig. 6. Active inductors are used instead of resistors as the drain loads, in order to improve the high frequency response. PEQ can decrease the response in the low-frequency region but increase the amplitude of the signal in the high-frequency region.

Fig. 7 shows the ac gain simulation results. The TIA with active inductors compensated for 10dB in the 0-300MHz band. The gain of PEQ is not more than 10dB. But the PEQ compensated for 20dB in the 0-300MHz band. For the whole receiver, the peak ac gain value is 75dB at 300MHz. The reason why we designed 300MHz as the peak point is that the -3dB bandwidth of 150μm×150μm APD is 300MHz. By this way, the VLC receiver can achieve better frequency compensation performance.

Fig. 8 shows the micrograph of the VLC receiver chip. The VLC receiver we propose was fabricated by UMC 0.18μm standard CMOS process, and the chip area is 889 × 570 μm². The DC power supply for the chip is 1.8 V. All pads and some large components are marked in the figure. The VLC receiver chip is packaged on a PCB using bonding wires. The dimensions of the DUT are 4.5 cm×4.5 cm. The experimental results are discussed in the next section.

3. Experiment results

Fig. 9 shows the experimental setup to measure the frequency response of the receiver.
The experimental setup is shown in Fig. 9. A LD (OSRAM PL TB450B) is driven by the Bias-T (Mini-Circuits ZFBT-4R2GW+), the DC bias voltage of LD is 4V. We used a network analyzer (Agilent E5062A) to measure the frequency response of the receiver. Port 1 of the network analyzer was connected to Bias-T. The output of receiver was connected to port 2 of the network analyzer. The output-power of the network analyzer is 0dBm.

The output-frequency of the RF signal generator is changed from 100MHz to 500MHz. The output waveform of different input frequency is shown in Fig. 12. Because of the free-space communication with no lens for focusing, the optical power is weak, the output signal voltage swing of receiver chip is relatively small. The peak to peak voltage of 100MHz waveform is 20.3mV, and the peak to peak voltage of 420MHz waveform is 14.2mV. The waveform of 420MHz is clear and stable, which means good communication performance under this frequency.

4. Conclusion

In this paper, the trade-off relationship between the area and frequency response of APD is analyzed. Based on the study of APD, we proposed a free-space VLC receiver with large area APD. Active inductor peaking and post-equalization technique are used for frequency compensation of the large area APD. Utilizing a LD as the light source, the measured -3dB bandwidth of receiver chip is 420MHz over 0.5m distance without lens. The VLC receiver we proposed is designed for free-space communication, and has the advantages of low cost, low power-consumption, compatible with standard CMOS technology, and high integration-density.

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