A Comprehensive Graphene FET Model for Circuit Design

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Abstract—During the last years, Graphene based Field Effect Transistors (GFET) have shown outstanding RF performance; therefore, they have attracted considerable attention from the electronic devices and circuits communities. At the same time, analytical models that predict the electrical characteristics of GFETs have evolved rapidly. These models, however, have a complexity level that can only be handled with the help of a circuit simulator. On the other hand, analog circuit designers require simple models that enable them to carry out fast hand-calculations, i.e., to create circuits using small-signal hybrid-π models, calculate figures of merit, estimate gains, pole-zero positions, etc. This paper presents a comprehensive GFET model that is simple enough for being used in hand-calculations during circuit design and at the same time it is accurate enough to capture the electrical characteristics of the devices in the operating regions of interest. Closed analytical expressions are provided for the drain current $I_D$, small-signal transconductance gain $g_m$, output resistance $r_o$, and parasitic capacitances $C_{gs}$ and $C_{gd}$. In addition, figures of merit such as intrinsic voltage gain $A_V$, transconductance efficiency $g_m/I_D$, and transit frequency $f_T$ are presented. The proposed model has been compared to a complete analytical model and also to measured data available in current literature. The results show that the proposed model follows closely to both the complete analytical model and the measured data; therefore, it can be successfully applied in the design of GFET analog circuits.

Index Terms—Graphene, FET, Analytic Model

I. INTRODUCTION

The reduction of dimensions in Silicon based transistors faces great challenges as dimensions approach atomic sizes and physical limits will be eventually reached. A great deal of research has focused during the last years in new materials that alleviate these limitations. One of these materials is Graphene [1], a two-dimensional structure with outstanding electrical characteristics such as very high electron mobilities in the order of 20000 cm$^2$V$^{-1}$s$^{-1}$ on silicon substrates [2]. The possibility of achieving such high electron mobilities, which are orders of magnitude higher than silicon based technologies, makes GFETs excellent candidates for replacing nanometer CMOS transistors in future high-speed analog electronic circuits [3].

Since the demonstration of the first GFET [4], the technology has evolved very fast. In just very few years it has been shown that de-embedded, intrinsic GFETs transit frequencies $f_T$ are comparable to or higher than those of similarly sized nanometer CMOS devices [5][6][7]. Actual measured $f_T$ is, in fact, much lower than CMOS, mainly due to the presence of interface and contact resistances. These resistances are a serious issue in GFET technology and therefore there are active research efforts on finding ways to reduce their impact. Latest research results have shown that contact resistances well bellow 100 $\Omega \mu m$ are possible; for instance, contact resistances as low as 20 $\Omega \mu m$ were measured for hydrogen intercalated graphene growth [8]. RF/Analog design uses solely the minimum width transistors of a technology. Minimum transistor sizes in RF applications are generally above 20 $\mu m$ - 30 $\mu m$, whereas in analog-baseband circuits the dimensions can be as large as hundreds of micrometers. Transistors with these widths would present small contact resistances with values similar to those of parasitic resistances on the metallic interconnection/vias in nanometer CMOS technologies. Their impact on the circuit performance would be the same as other parasitics, and therefore, they can be handled using the same circuit design techniques that are used in todays CMOS circuits.

Likewise, high transconductance gain $g_m$ values were also demonstrated [9][5]. In addition, it has been shown that the drain current in GFET transistors has a saturation region [10]. This is an important characteristic since it facilitates the use of the GFETs as voltage-controlled current sources, and consequently, the design of analog circuits in general. Until now, drain current saturation has been mainly observed in long gate GFET devices, and short-channel GFETs still present unsatisfying current saturation behavior. Nevertheless, it has been reported that the use of bilayer graphene can result in important current saturation improvements [11]. Likewise, lateral graphene heterostructures have also been suggested as a possible solution to enhance the current saturation [12].

Although GFET technology still faces technological challenges, projections of GFET vs. CMOS high-speed analog IC performance [13] have shown that GFET technology can potentially surpass CMOS in the near future provided that the
The development of GFET devices has been accompanied by the appearance of electrical models that can be used to describe the electrical characteristics of the device and also to simulate circuits [14][15][16][17][18][19]. Some of these initial models are physical models which do not have closed expressions and therefore require the use of numerical methods to find solutions. These models are very useful to explain the device physics; however, they are not suitable for implementation in analog circuit modeling languages such as SPICE or Verilog-A. Other models are compact analytical models which can be written in SPICE or Verilog-A and used to simulate circuits with EDA CAD tools. These models, however, are still very complex for being used during circuit design. Analog circuit designers make many decisions based on hand-calculations, and therefore require simple analytical expressions.

This paper introduces a comprehensive model which provides the circuit design community with simple mathematical expressions to analyze GFETs. The proposed model is based on hand-calculations, and therefore require simple analytical expressions.

An exhaustive study of the drain-source current using the drift equation for GFET transistors can be found in [19]. The result of this study shows that the drain-source current can be expressed as:

$$I_D = \mu W \frac{V_{DSI}^2}{L} \left[ |Q_{net}| + e n_{paddle} \right] dV$$  (1)

where \( \mu \) is the mobility, \( W \) the transistor width, \( L \) the transistor length, \( Q_{net} \) the net mobile charge density per unit area, \( e \) the elementary charge (\( 1.6 \times 10^{-19} \) As), \( n_{paddle} = \frac{\Delta^2}{\hbar^2 v_f^2} \), and \( V_{DSI} \) the internal drain-source voltage. The parameter \( \Delta \) represents the spacial inhomogeneity of the electrostatic potential, \( \hbar \) is the reduced Planck constant, and \( v_f \) is the Fermi velocity.

For simplicity, the integral in the numerator of (1) can be split and solved independently.

$$I_D = \mu W \frac{NUM}{DEN} = \mu W \frac{NUM_1 + NUM_2}{DEN}$$  (2)

where the first term in the numerator is:

$$NUM_1 = \beta \int_0^{V_{DSI}} \left[ \frac{-C_{TOP}}{2\beta} + \sqrt{C_{TOP}^2 + 4\beta |C_{TOP}(V_{GSI} - V) + eN_f|} \right]^2 dV$$  (3)

and the factor \( \beta = e^3/\pi (h v_f)^2 \). \( C_{TOP} \) is the top oxide capacitance, \( V \) the potential variation along the channel due to \( V_{DS} \) and \( N_f \) is a term that accounts for the net acceptor/donor doping. Since the graphene material does not have a bandgap, GFETs do not switch off completely like other FET devices. Instead, they show a minimum conduction point which is known as the Dirac point. The doping level set by \( N_f \) is responsible of shifting the Dirac point in a similar way than the intentional doping used to control the threshold voltage in MOS devices. In practice, the Dirac point is also affected by \( V_{DS} \); nevertheless, \( N_f \) sets an absolute offset which is biasing independent. Accordingly, it is possible to define a zero-bias threshold voltage for GFET devices as:

$$V_{TH,0} = eN_f/C_{TOP}$$  (4)

and the effective gate-source overdrive voltage as:

$$V_{eff} = V_{GSI} + V_{TH,0}$$  (5)

where \( V_{GSI} \) is the internal gate-source voltage. Accordingly, (3) can be rewritten as:

$$NUM_1 = \beta \int_0^{V_{DSI}} \left[ \frac{-C_{TOP}}{2\beta} + \sqrt{C_{TOP}^2 + 4\beta |C_{TOP}(V_{eff} - V)|} \right]^2 dV$$  (6)

Equation (6) is simplified by introducing the integration variable to \( z = C_{TOP}(V_{eff} - V) \). The integral has the following symbolic solution:

$$NUM_{1(z>0)} = -\frac{1}{32} \beta^2 C_{TOP} \left[ C_{TOP}^2 \left[ \frac{C_{TOP}^4}{32} + \frac{\beta^2 z^2}{2} + \frac{\beta C_{TOP}^2 z^2}{2} \right] \right]^{z_1}$$  (7)

$$NUM_{1(z<0)} = -\frac{1}{32} \beta^2 C_{TOP} \left[ C_{TOP}^2 \left[ \frac{C_{TOP}^4}{32} - \frac{\beta^2 z^2}{2} + \frac{\beta C_{TOP}^2 z^2}{2} \right] \right]^{z_1}$$  (8)

where \( z_1 = C_{TOP}V_{eff} \) and \( z_2 = C_{TOP}(V_{eff} - V_{DSI}) \). The second term of the numerator is given by:

$$NUM_2 = \int_0^{V_{DSI}} e n_{paddle} dV = e n_{paddle} V_{DSI}$$  (9)
The denominator in \( 7 \) can be expressed as:

\[
\operatorname{DEN} = L + \mu \left[ \int_{0}^{V_{DSi}} \frac{1}{v_{\text{SAT},AV}} dV \right] \tag{9}
\]

which can be simplified assuming an average \( v_{\text{SAT},AV} \) given by:

\[
v_{\text{SAT},AV} = \frac{\omega}{\sqrt{\pi \frac{Q_{\text{NET,AV}}}{e} + n_{\text{puddle}}}} \tag{10}
\]

where \( \omega \) is obtained from the surface phonon energy of the substrate \( h\omega \) and \( Q_{\text{NET,AV}} \) is the average charge given by:

\[
Q_{\text{NET,AV}} = \beta \left[ \frac{-C_{\text{TOP}}}{2\beta} + \sqrt{C_{\text{TOP}}^2 + 4\beta |C_{\text{TOP}}(V_{\text{eff}} - V_{DSi}/2)|} \right]^2 \tag{11}
\]

With the previous assumption, the denominator can be expressed as:

\[
\operatorname{DEN} = L + \frac{\mu}{v_{\text{SAT,AV}}} |V_{DSi}| \tag{12}
\]

The accuracy of the model has been successfully evaluated by its authors by comparing it against numeric models and measured data of different GFET devices built by different groups \[20\] \[21\] \[9\].

The whole model is very compact and perfectly suitable for building SPICE and Verilog-A models; and consequently, it is also suitable for circuit simulation purposes. While the model shows outstanding accuracy, it can be appreciated that it is still complicated to be used by analog circuit designers. The main problem is that it lacks a simple closed mathematical expression for the drain current like the one that is available for CMOS FET transistors (Shichman-Hodges model) \[22\] or like the collector current in bipolar transistors (Ebers-Moll model) \[23\]. A simple expression for the drain current is fundamental since the parameters for small-signal hybrid-\( \pi \) model and figures of merit are directly derived from this equation. The later ones represent the foundation of electronic circuit theory and are the main tools that analog circuit designers have in order to analyze circuit topologies and make design decisions. Therefore, it is of paramount importance to obtain a simplified expression for the GFET drain current.

III. SIMPLIFIED LARGE SIGNAL MODEL

The difficulty in finding a simple expression for the GFET drain current lies in the complexity of \( 7 \). Fortunately, the replacement of technology dependent parameters taken from the measured GFETs and physical constants unveils that there is a term that dominates and therefore \( 1 \) can be reduced to:

\[
\operatorname{NUM}_1 \simeq -\frac{1}{2} \frac{z^2}{C_{\text{TOP}} \times \text{sign}(z)} \tag{13}
\]

for \( z > 0 \) (typical case in analog design) can be expressed as:

\[
\operatorname{NUM}_1 \simeq C_{\text{TOP}} V_{DSi} \left( V_{\text{eff}} - \frac{V_{DSi}}{2} \right) \tag{14}
\]

For typical technology parameters \( \operatorname{NUM}_1 \gg \operatorname{NUM}_2 \). As a result, \( \operatorname{NUM}_2 \) can be disregarded and \( \operatorname{NUM} \simeq \operatorname{NUM}_1 \).

Expression \( 12 \) becomes complicated when \( v_{\text{SAT,AV}} \) is replaced by \( 10 \) and \( Q_{\text{NET,AV}} \) by \( 11 \). However, it can also be simplified under the assumption that \( V_{\text{eff}} \gg V_{DSi}/2 \), and \( n_{\text{puddle}} \ll \pi |Q_{\text{NET,AV}}|/e \). Under these conditions, \( |Q_{\text{NET,AV}}| \approx C_{\text{TOP}} (V_{\text{eff}} - V_{DSi}/2) \) and the denominator can be simplified to:

\[
\operatorname{DEN} \simeq L + \frac{\mu}{\omega} \sqrt{\frac{\pi C_{\text{TOP}}}{e} V_{DSi} V_{\text{eff}} - \frac{V_{DSi}}{2}} \tag{15}
\]

Finally, the GFET drain current is found by replacing \( 14 \) and \( 15 \) into \( 2 \):

\[
I_D \simeq \frac{\mu W C_{\text{TOP}} (V_{\text{eff}} - V_{DSi}/2)}{V_{DSi} + \frac{\mu}{\omega} \sqrt{\frac{\pi C_{\text{TOP}}}{e} V_{\text{eff}} - \frac{V_{DSi}}{2}}} \tag{16}
\]

which is a closed analytical expression that relates the main technology parameters and biasing conditions. Fig. 1, Fig. 2 and Fig. 3 show \( I_D \) vs. \( V_{DSi} \) plots for GFETs of 1 \( \mu \)m width and 440 nm, 1 \( \mu \)m, and 3 \( \mu \)m length respectively from \[20\]. \( I_D \) is calculated by using \( 16 \) and the complete model including fitting parameters from \[19\]. For these devices, \( N_f \) is approximately 0, and therefore \( V_{TH,0} \approx 0 \) V. The other parameters have the following values: \( C_{\text{TOP}} = 3.6 \times 10^{-3} \text{F/m}^2 \), \( \mu = 7000 \text{ cm}^2/\text{V} \cdot \text{s} \), and \( h\omega = 56 \text{ meV} \). \( V_{GSi} \) takes values from 0 V to 2 V in steps of 500 mV. It can be appreciated that the simplified model matches very well both the complete model and the measured data for \( V_{\text{eff}} > V_{DSi}/2 \). The plots show that both the first triode region and the saturation/negative resistance region are correctly modeled by
that there is strong dependence of short lengths in the GFET transport characteristics [24] [25]. This dependence can be analytically explained by (15) where it can be seen that $DEN \approx L$ only for $V_{DSi} \approx 0$. Once the gate and drain bias voltages increases, the value of $DEN$ departs from $L$ and increases quickly. For very short lengths and high electric fields, the current becomes independent of the channel length, something that has also been confirmed experimentally in [26]. Under these conditions, the drain current saturates, stops depending on $\mu$, and takes a value of approximately:

$$I_D \simeq \omega W \sqrt{\frac{C_{TOP}}{\pi}} \sqrt{V_{eff} - V_{DSi}/2} \quad (17)$$

IV. SMALL SIGNAL MODEL

While the large signal model in [16] encloses the physics of the device in a single expression, it is still too complex to be used in quantitative circuit analyses of the behavior of amplifier configurations. These analyses are normally performed by taking advantage of linear system theory in which a simplified small-signal representation of the transistor biased in the operating point is used. The small-signal representation, also called hybrid-\(\pi\) model, is shown in Fig. 5. The parameters $g_m$, $r_o$, $C_{gs}$, and $C_{gd}$ can be obtained by linearization of the large signal model. Naturally, the small-signal representation provides only limited information which is valid for small excursions from the operating point. However, it allows to calculate and estimate in an easy way small-signal dynamic linear behavior of gain, phase, poles, zeros, impulse response, etc. Large-signal behavior is non-linear and therefore its analysis requires the use of the complete model and a circuit simulator.

The derivation of small-signal parameters for the GFET transistor is presented in the following subsections.
Fig. 5. GFET Symbol and equivalent hybrid-π model for small-signal analysis.

Fig. 6. Transconductance \( g_m \) calculated using the complete and simplified model for the 440 nm length, 1 \( \mu \)m width GFET from \([20]\). \( N_f \approx 0 \), \( V_{TH,0} \approx 0 \) V, \( C_{TOP} = 3.6 \times 10^{-3} \text{F/m}^2 \), \( \mu = 7000 \text{cm}^2/\text{V·s} \), and \( h \omega = 56 \text{ meV} \).

A. Transconductance \( g_m \)

The expression for the transconductance gain can be directly derived from \([16]\):

\[
g_m = \left. \frac{\delta I_D}{\delta V_{GSi}} \right|_{V_{DSi},\text{const}}.
\]

\[
g_m = \left( \frac{I_D}{V_{eff} - V_{DSi}/2} \right) \left( 1 - \frac{I_D}{2 \pi W \omega} \right)
\times \left( \frac{\pi}{e \times C_{TOP}} \sqrt{\frac{V_{eff} - V_{DSi}/2}{V_{eff}}} \right)
\]

Fig. 6 shows \( g_m \) values calculated using (19) and the complete model. It can be seen that (19) follows closely the complete model in particular for \( V_{eff} > V_{DSi}/2 \). It is interesting to notice that \( g_m \) drops substantially at large \( V_{GSi} \) biasing voltages, mainly due to the effect of \( V_{SAT} \). Therefore, the best \( g_m \) performance is actually achieved at low \( V_{eff} \) voltages.

B. Output resistance \( r_o \)

The output resistance can be calculated as \( r_o = 1/g_0 \) where \( g_0 \) is the output conductance. An expression for \( g_0 \) can be directly derived from \([16]\):

\[
g_o = \frac{\delta I_D}{\delta V_{DSi}} \Big|_{V_{GSi},\text{const}}.
\]

\[
g_o = \frac{I_D}{V_{eff} - V_{DSi}/2} \left[ \frac{1}{2} + \frac{I_D}{\mu W C_{TOP}} \left( L + \frac{\mu}{e \times C_{TOP}} V_{eff}^{3/2} \right) \right]
\]

One important characteristic of the GFET device is that under some biasing conditions, \( g_0 \) becomes negative \([27][28]\). A negative \( g_0 \) makes the device unstable, and in general this region needs to be avoided in amplifier design. On the other hand, a negative \( g_0 \) is a very welcome asset when designing oscillators. The biasing conditions in which \( g_0 \) changes from positive to negative values can be found by making \( g_0 = 0 \) in \([21]\) and solving for \( V_{DS} \). The expression for this boundary condition is:

\[
V_{DS,\text{lim}} = \frac{-2L + \sqrt{4L \left( L + \frac{\mu}{e \times C_{TOP}} V_{eff}^{3/2} \right)}}{\mu \times \frac{\pi C_{TOP}}{e} \sqrt{V_{eff}}}
\]

Fig. 7 shows \( I_D vs. V_{DS} \) plots for different \( V_{GS} \) voltages. In addition, the plot shows the points in which \( g_0 = 0 \) \((r_o = \infty)\) which were found by using (22). It can be seen that (22) predicts very well the transition from positive to negative output resistance.

C. Total Channel Charge

The distributed gate capacitance in GFET devices is modeled as the series capacitance of \( C_{TOP} \) and the quantum capacitance \( C_q \) in the graphene channel \([15]\):

\[
C_q = C_q \times C_{TOP} \frac{C_q + C_{TOP}}{C_q}
\]

where the parameter \( C_q \) relates the distributed charge along the graphene channel and its potential \( V_{CH} \), which depends
strongly on both $V_{GS}$ and $V_{DS}$. The total charge stored in the gate capacitance can be found by considering that the charge of all capacitors is the same when they are connected in series. Accordingly, the total charge stored in the gate capacitance is equal to the total charge in the graphene channel $Q_{CH}$. The separation of the gate capacitance between Gate-Source capacitance and Gate-Drain capacitance can be done by taking partial derivatives of $Q_{CH}$. Consequently, it is beneficial to find a simple closed expression for $Q_{CH}$ which can be easily differentiated. $Q_{CH}$ can be expressed as [19]:

$$Q_{CH} = W \int_{0}^{L} (Q_{NET}(x) + e_{puddle}) \, dx \quad (24)$$

By changing the integration variable $dx$ to $dV$ and reordering the expression, $Q_{CH}$ becomes:

$$Q_{CH} = \frac{eW}{E_{AV}} \int_{0}^{V_{DSi}} \left( \frac{\beta}{\epsilon} |V_{CH}| V_{CH} + n_{puddle} \right) \, dV \quad (25)$$

where $E_{AV}$ is the average electric field which is given by:

$$E_{AV} \approx \frac{dV}{dx} \approx \frac{V_{DSi}}{L} \quad (26)$$

The integral in (25) is similar to that in (9) and therefore it is solved in the same way. Likewise, there is a quadratic term that dominates and therefore $Q_{CH}$ can be reduced to:

$$Q_{CH} \approx \frac{e \times W}{2E_{AV}} \left( - \frac{z_{2}^{2}}{C_{TOP} \times \epsilon} \right) \bigg|_{z_{1}}^{z_{2}} \quad (27)$$

which after replacing $z_{1}$ and $z_{2}$ becomes:

$$Q_{CH} \approx \frac{WC_{TOP}}{E_{AV}} V_{DSi} \left( V_{eff} - V_{DSi}/2 \right) \quad (28)$$

Finally, a simplified expression for $Q_{CH}$ is found by replacing (26) into (28):

$$Q_{CH} \approx C_{TOP} W L (V_{eff} - V_{DSi}/2) \quad (29)$$

### D. Gate-Source Capacitance $C_{gs}$

The small-signal gate-source capacitance can be calculated as:

$$C_{gs} = \frac{\delta Q_{CH}}{\delta V_{GSi}} \bigg|_{V_{DSi}, \text{const.}} \quad (30)$$

and

$$C_{gs} = C_{TOP} W L \quad (31)$$

Fig. 8 shows plots of $C_{gs}$ calculated using (31) and the complete model. It can be seen that for $V_{eff} > V_{DS}/2$, $C_{gs}$ approaches the value of the total oxide capacitance. For large $V_{eff}$ values the error is within 5%.

### E. Gate-Drain Capacitance $C_{gd}$

The small-signal gate-drain capacitance can be calculated as:

$$C_{gd} = -\frac{\delta Q_{CH}}{\delta V_{DSi}} \bigg|_{V_{GSi}, \text{const.}} \quad (32)$$

and

$$C_{gd} = \frac{C_{TOP} W L}{2} \quad (33)$$

Fig. 9 shows plots of $C_{gd}$ calculated using (33) and the complete model. In this case it is also possible to see that even though $C_{gd}$ values calculated with the complete model have valleys at different drain biasing conditions, their values are close to the value predicted by (33). For large $V_{DS}$ values the error is within 15%.

Fig. 10 shows $C_{gs}$, $C_{gd}$, and $I_{D}$ vs. $V_{GSi}$. It is interesting to see that despite the fact that the capacitances change for different biasing conditions, their values approximate very well the simplified model when enough $V_{GSi}$ and $V_{DSi}$ bias is present.
V. FIGURES OF MERIT

The extraction of small-signal parameters allows the calculation of figures of merit that can be used to make performance comparisons. The main figures of merit used to evaluate amplifying devices are: intrinsic voltage gain $A_V$, transconductance efficiency $g_m/I_D$, and transit frequency $f_T$. Expressions for these figures of merit are found in the following subsections.

A. Intrinsic Voltage Gain $A_V$

The intrinsic voltage gain estimates the low frequency voltage amplification capabilities of the device and can be calculated as:

$$A_V = g_m \times r_0$$  \hspace{1cm} (34)

$$A_V = \left[ 1 - \frac{I_{DSi}}{2W \omega} \sqrt{\frac{\pi}{eC_{TOP}} \sqrt{V_{eff} - V_{DSi}/2}} \right] \times \left[ 1 + \frac{I_{DSi}}{\mu WC_{TOP}} \left( \frac{L}{V_{DSi}^2} + \frac{\mu}{4W} \sqrt{\frac{\pi C_{TOP}}{e}} \right) \right]$$  \hspace{1cm} (35)

B. Transconductance Efficiency $g_m/I_D$

The $g_m/I_D$ relates the transconductance amplification capability of the device and the drain current that is required to produce it. Therefore, it is a measure of the power consumption efficiency of the amplifying device. The expression for $g_m/I_D$ can be directly obtained from (19):

$$\frac{g_m}{I_D} = \frac{1}{V_{eff} - V_{DSi}/2} \times \left( 1 - \frac{1}{2} \frac{I_D}{W \omega} \sqrt{\frac{\pi}{e \times C_{TOP}} \sqrt{V_{eff} - V_{DSi}/2}} \right)$$  \hspace{1cm} (36)

C. Transit Frequency $f_T$

The transit frequency estimates the frequency at which the current gain of the device drops to 1, and it is a measure of its high-speed and bandwidth capabilities. The transit frequency is defined as:

$$f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd})}$$  \hspace{1cm} (37)

$$f_T = \frac{1}{2\pi \left( \frac{\pi C_{TOP} W L}{2} \right)} \times \left( 1 - \frac{1}{I_D \sqrt{\frac{e \times C_{TOP}}{V_{eff} - V_{DSi}/2}}} \right)$$  \hspace{1cm} (38)

Fig. 11 shows plots of $f_T$ calculated using (38) and the complete model. It can be seen that there is very good matching for most biasing points, and disagreements start to become visible only when $V_{eff} < V_{DS}$.

VI. SUMMARY

A summary of the simplified GFET model is shown in Table I. The expressions in this table were used to extract small-signal hybrid-π model parameters and figures of merit typically used to compare the performance of transistors. The proposed model has been validated by comparing it against a complete analytical model and to measured data available in current literature. Whereas the complete analytical model hides the effects of physical parameters behind many separate
calculations, the proposed model provides a simple expression that enables direct identification of dominant physical parameters. In addition, the proposed GFET model is ready for use in circuit design in exactly the same way as the Shichman-Hodges and Ebers-Moll models are used for CMOS and bipolar circuit design respectively.

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