Single donor electronics and quantum functionalities with advanced CMOS technology

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Abstract
Recent progresses in quantum dots technology allow fundamental studies of single donors in various semiconductor nanostructures. For the prospect of applications figures of merits such as scalability, tunability, and operation at relatively large temperature are of prime importance. Beyond the case of actual dopant atoms in a host crystal, similar arguments hold for small enough quantum dots which behave as artificial atoms, for instance for single spin control and manipulation. In this context, this experimental review focuses on the silicon-on-insulator devices produced within microelectronics facilities with only very minor modifications to the current industrial CMOS process and tools. This is required for scalability and enabled by shallow trench or mesa isolation. It also paves the way for real integration with conventional circuits, as illustrated by a nanoscale device coupled to a CMOS circuit producing a radio-frequency drive on-chip. At the device level we emphasize the central role of electrostatics in etched silicon nanowire transistors, which allows to understand the characteristics in the full range from zero to room temperature.

Keywords: dopants, nanowires, CMOS

(Some figures may appear in colour only in the online journal)

1. Introduction

In 1965 Gordon E. Moore reported on the progress of the semiconductor industry and enunciated the trend that became its driving force until today \cite{1, 2}. Half a century later engineers face the most difficult challenges ever for developing the next generations of chips. Beyond the huge cost of fabrication facilities, a fundamental breakdown occurs when the atomic nature of matter makes the traditional transistor scaling irrelevant. While the technology node at which this will happen depends on the very fine details of each device, it is interesting to compare the critical dimensions with the size of the wavefunction of single dopant atoms. A crude approximation of the Bohr radius of dopants in silicon, derived from the hydrogen atom model, yields a value of $a_B = 3 \text{ nm}$. This is a realistic number for impurities weakly bounded to the host atom, like most dopants used in CMOS technology (e.g. As, P, B). Taking into account that the tail of the wavefunction extends over several $a_B$, this opens opportunities to use the quantum properties of these shallow donors or acceptors in actual devices produced today by the microelectronics facilities.
This experimental review focuses on this area of research where quantum dots are co-integrated in an advanced CMOS technology with only minor modifications to the integration process flow. We restrict ourselves to this particular case because for the perspective of applications standard CMOS processes are a key enabler for scalability. Large scale integration requires an efficient isolation scheme between devices, such as shallow trench or mesa isolations performed by etching. In addition it allows a direct re-use of all the devices necessary to design a fully functional technology platform such as periphery transistors, electrostatic discharge protection diodes and Field Effect Transistors. Furthermore it allows to co-integrate a quantum core together with conventional CMOS logic or analog circuits for driving or read-out.

Other fabrication methods for donor based devices or small quantum dots, which have been covered extensively in recent reviews, are only briefly summarized in the remaining of this introduction. The broad topic of single donor electronics has been covered, e.g. in [3], in a comprehensive review [4] as well as a recent special issue of *J. Phys.: Condens. Matter* [5]. Recent advances aiming at deterministic ion implantation have been covered e.g. in [6–8].

The most widely spread method for fabricating small quantum dots in the academic community is to use a bulk Si substrate and deposit top gates which create a 2D electron gas underneath (see figure 1). There is therefore no etching of the silicon layer, which is a striking difference with the devices produced within microelectronics facilities on which this review focuses. Built on a well established technique [10, 11], it has been very successful recently to couple quantum dots and build spin-based quantum bits featuring a long enough coherence time to allow for practical operations [9, 12–18]. This method is not compatible with large scale integration, but could be interesting for preserving carriers mobility and quantum coherence.

A radically different (and bottom-up) scheme is based on nanoscale patterning of H-passivated silicon surfaces with ultra-high vacuum scanning tunneling microscopes [19]. This technique has been applied to study dopant clusters [20, 21] and finally single-dopant devices [22], as illustrated in figure 2.

Unlike ion implantation, the method yields deterministic doping since single dopant atoms can be positionned in silicon with atomic precision. Subsequent encapsulation by silicon molecular beam epitaxy activates the dopant in a substitutional site. Devices are engineered with no dielectric interfaces and far away from surface states. The sharp transition from doped to undoped allows to tune the resistance of tunnel gaps over many orders of magnitude simply by engineering the device dimensions.

### 2. Silicon nanowire CMOS transistors

#### 2.1. Fully-depleted silicon-on-insulator (SOI) nanowire technology

Nowadays the industry of semiconductors relies on nanometer scale technologies enabling very high density and performances [23, 24]. The integration scheme developed at CEA-Leti for this ‘nano-CMOS’ era is shown in figure 3. Starting from a SOI substrate (typical thickness: 10–15 nm), nanowires are patterned using 193 nm deep-UV (DUV) lithography. Resist trimming is performed during etching to reach nanowire widths down to 5 nm. This is the most important part of the integration scheme that enables to
reach sub-10 nm width. The details of this process is shown in figure 4.

The smallest width obtained directly after DUV lithography is approximately 80 nm. The active stack consists of undoped Si, SiO2 dielectric layer and an organic bottom anti-reflective coating (BARC) layer patterned using 193 nm ArF resist. The thickness of the photoresist is adapted to have proper aspect ratio at the end of trimming. The nanowire etching is carried out using the trimmed resist/BARC as a mask. Therefore the final width of nanowires is determined mainly by the amount of trimmed resist.

We then define a metallic gate with high-k dielectric as gate oxide. For that purpose a high-k/metal gate stack with typically 2.3 nm of HISiON, 5 nm of TiN and 50 nm poly-Si is deposited. The pre-deposition cleaning step is adapted to form an interfacial SiO2 layer. At this point a gate down to 20 nm is patterned, again with DUV lithography, also followed by resist trimming and reactive ion etching. We use mesa isolation, therefore the gate covers the nanowire on three sides (trigate or Ω-gate geometry). A first set of offset spacers is then formed (made of silicon nitride, shown in blue in figure 3). Silicon epitaxy is then performed on source/drain areas to obtain raised source/drain. Low dose doping (LDD) is then performed. A second offset spacer consisting of TEOS liner and nitride spacer is then patterned. It is then followed by high dose doping (HDD) to define source/drain, and finally silicidation (with formation of NiPt silicide) for lower contact resistance. Tungsten contact to define source/drain, and finally silicidation (with formation of NiPt silicide) for lower contact resistance. Tungsten contact

2.2. Electrostatics and field-effect: simulations at 300 K

Because the integration scheme shown above is developed for industrial purposes, a comprehensive set of simulation tools are used to model the device properties. We have developed at CEA-INAC a k,p and tight-binding code to compute the structural, electronic, optical and transport properties of various kinds of nanostructures such as semiconductor nanocrystals, nanowires and carbon nanotubes [29].
Topical Review

quantum dots in silicon single-electron transistors obtained by disorder effects in constrictions [31]. Reference [32] gives a review of single electron devices in silicon around that period. In our devices the top gate controls the channel’s potential with a nearly ideal efficiency, i.e. in terms of lever-arm parameter \( \alpha = \frac{C_g}{C_\Sigma} \approx 1 \), where \( C_g \) is the gate capacitance and \( C_\Sigma \) is the sum of all capacitances connected to the channel. The key parameter for engineering field effect (FET) or single electron (SET) transistors at low temperature is the region below the spacers. Since it is low doped, it exhibits a very strong temperature and electric field dependence. When the right parameters are chosen it turns into a tunnel barrier at low temperature, resulting in a very reliable and controlled SET device [34], as shown schematically in figure 9. After the first peaks, very regular oscillations are recorded in the drain-source current versus front gate voltage, as expected for the orthodox model of Coulomb blockade. This is consistent with typical numbers for the gate capacitance of relatively large (≥20 nm) devices, of the order of \( C_g = 10–100 \) aF. This yields a peak spacing in voltage in the 1–10 mV range. In this first generation of devices (produced at LETI before 2010) the charging energy dominates completely the electrical transport properties: the peak spacing was found to be constant over up to 300 electrons added in the channel. This is generally not the case with 2DEG devices unless a sophisticated scheme of multiple gates is used to create a single dot [12].

In contrast with the geometric gate capacitance, the mesoscopic properties of the access regions are very rich, as shown in figure 10. They undergo a metal-insulator transition as the electric field (gate voltage) increases. As expected, not only the conductance varies strongly in this region, but also the dielectric constant. This has been studied in [35] by recording the source and drain capacitances over a large number of Coulomb diamonds. Not surprisingly, the conductance and dielectric constant were found to scale with the same parameter, namely the localization length \( \xi \) [36].

3.2. Use of the backgate: SET/FET dual behaviour

Silicon-on-insulator substrates provide an efficient way to preserve electrostatic integrity and prevent short-channel effects in ultra-scaled transistors. They provide in addition another gate electrode, either through a global (the whole substrate) or local gates in case of shallow trench isolation [25]. The benefits of having two gates acting on the channel has been used at NTT (figure 11) to investigate the vertical position (‘depth’) of isolated dopants [37]. This electrostatic detection is complementary with a conductance measurement through the device,
which they performed to estimate the 'horizontal' position by observing shifts in threshold voltage \[38, 39\]. The same technique of 2D mapping of the conductance versus front- and back- gates has been used by the same group to compare the properties of P-doped channels, with Indium and Boron \[40\].

The evolution of the \[I_d(V_g)\] characteristics at 300 K with the backgate voltage is shown in figure 12(a) for an NW-FDSOI transistor of channel thickness \[T_{Si} = 8 \text{ nm}\], an active width \[W = 40 \text{ nm}\] and a gate length \[L_g = 70 \text{ nm}\]. The small \[T_{Si}\] and relatively long \[L_g\] ensure good sub-threshold electrostatic control by the gate. Indeed we observe a sub-threshold slope of 70 mV/decade (measured with \[V_g = 1 \text{ mV}\]), at the state-of-the-art for a top-gate oxide thickness \[T_{BOX} = 5 \text{ nm}\], and close to the theoretical limit for thermally activated transport \[kT/\epsilon\].\ln(10) which yields 60 mV/decade for operation at 300 K. Figure 12(c) shows the variation of the linear conductance at

\[V_g = 1.6 \text{ V}\] above the threshold voltage. Using a positive back gate voltage \[V_{bg}\], we increase by 20% the normalized value of the ON-current, reaching 0.4 mA \(\mu\text{m}^{-1}\)\(V_{bg} = 39 \text{ V}\) and the source-drain bias \[V_d = 1 \text{ V}\], not shown). This is a high value for an etched Si-nanowire \[25, 26\]. Figure 12(a) shows that this gain is obtained without degrading the sub-threshold slope. Increasing \[V_{bg}\] leads to a decrease of the threshold voltage \(V_T\), plotted in figure 12(b). From the slope \(dV_b/dV_T\) we can obtain the ratio of the effective front gate and back gate capacitances \[38\]. We found a ratio of 40 which is not far from a crude estimation with planar capacitors: \(dV_{bg}/dV_T \approx T_{BOX}/T_{FOX} = 30\) (in these devices the buried oxide thickness \(T_{BOX}\) is 145 nm). The deviation from this model can be explained using a more realistic 3D model of capacitances. For practical applications much thinner BOX should be used to lower the applied \(V_{bg}\).

Working with industrial technology can restrict the choice of available wafers. Since we had no highly-doped 300nm SOI wafers to process, using the backgate at low temperature is more tricky since the background (P-type) doping is very low and freezing of carriers occurs near 50 K, resulting in a vanishingly small conductance. The trick \[28\] consists in shining red light from a LED right above the sample, in the cryostat, before and during a ramp in back-gate voltage \[V_{bg}\]. The absorption of photons in a semiconductor can in principle play the same role as temperature, in the sense that it can generate carriers, hence making the crystal conducting. The mechanism has not been studied in details yet in our devices, but clearly for the residual doping level of the wafer, the light from the LED at low temperature seems at least as efficient as the thermal activation at 300 K, since the back-gate operates well at room temperature without light (it shifts the threshold voltage according to the capacitance ratio between front
Despite the size, the loss of conductance is shown for comparison.

For comparison the FET characteristics at 300 K and $V_{bg} = 0$ V is shown on the same plot. It exhibits a subthreshold swing of 112 mV/decade, as a result of its short channel and relatively thicker $T_{Si}$.

The use of the back gate has proved to be crucial to engineer more complex situations, such as transport through corner states (section 5), studies of a single dopant [41] (section 7) or two dopants in series (section 8).

4. First electron/hole regime in CMOS quantum dots

The threshold voltage $V_T$ of transistors is usually defined as the gate voltage for which the band diagram is flat [2]. When the field-effect transistor turns into a single-electron transistor at low temperature, it is relevant to study the voltage at which the first oscillations are observed and whether it is related or not to some room temperature characteristics. Ideally one could expect the first Coulomb peak to occur exactly at $V_T$. Despite the very clean aspects of silicon technology, the material after processing remains fairly disordered. Mobility is low and that usually translates at low temperature in a loss of current at voltages below the threshold. In other words, usually the first electrons or holes observed as Coulomb peaks in the conductance are not observed at $V_T$ in Si CMOS quantum dots.

A consistent behaviour between 300 K and low temperature has been reported in 2012 for N-type devices [42]. In the latest generations of FDSOI nanowire transistors, small size devices can have such optimized access regions that N-type devices do not exhibit Coulomb blockade but instead show an excess current at low temperature compared to 300 K. Since P-type doping results in smaller conductivities, the situation remains different for these devices. We have been able to observe recently the occurrence of the first holes right at the threshold voltage, as shown in figure 14. This device has a width of 15 nm, a film thickness $T_{Si} = 11$ nm and a gate length $L_g = 25$ nm. Despite the size, the loss of conductance is relatively small at large negative voltage and the first peak occurs very near the threshold voltage at 300 K, indicated by the arrow. The finite bias Coulomb diamonds shown in the insert illustrate the small size of the sample, with a charging energy for the first peak of the order of 35 meV, i.e. of the same order than the one expected for a single dopant. Due to
the very small width and the ‘trigate’ or ‘Ω’ gate geometry there is a strong screening by the front gate. As a result the effect of the backgate is much smaller than expected from the front and back oxide ratio. Also the effect of corner states discussed in the next section is not visible here, because of the rounded shape of the wire when its cross section is too small.

5. Corner states in CMOS quasi-1D channels

As shown in figure 7, there is a higher density of carriers at the corners of the nanowire. This can be used to create quasi-one-dimensional channels in the edges, and study interaction between them [43–45]. For the devices studied in [44] the spacers are not long enough to provide carrier confinement along the source-drain axis. However we clearly observe quantum dots. This can be explained by introducing disorder in the simulations: as shown in figure 15, the introduction of realistic surface roughness and charges in the dielectrics (remote Coulomb scattering) induces charge localization. Figure 15 illustrates that in the case of no disorder: accumulation starts in two symmetric extended edge channels. Surface roughness and remote positive charges can be introduced in the gate stack. While the carriers are still confined along the top edges of the channel, the mesoscopic variability breaks the left/right symmetry. Near the threshold voltage, the positive charges in the gate dielectric produce a confinement potential for the electrons in the edge states responsible for the quantum dots observed in the experiment.

The couple of lines (A1; A2) in figure 16 are attributed to the addition of two electrons in the first corner state while (B1; B2; B3) are attributed to the addition of three electrons in the second edge state. Other higher energy lines are indicated by arrows above the onset. The edge states disappear by hybridization with the bulk conduction channel at positive backgate voltage. Dot A shows a larger charging energy than dot B. The inset shows the shift of the resonance for (A1; A2) and (B1; B2).

6. CMOS single atom transistor

Single Atom Transistors (SATs), in which transport occurs through the orbitals of a single dopant state, have been obtained with CMOS devices [46] (following pioneering work where the dopant’s wavefunction was hybridized with the surface channel [47]) as well as 2DEG devices [48] and more recently with STM-assisted lithography [22].

6.1. Dopants diffusion

The low temperature characteristics of our nanowire transistors rely heavily on the presence of spacers to ensure a resistive enough access region to the channel. We also realized samples without spacers. In this section we focus only on the shortest of those devices, for which the nominal gate length was 30 nm, the width 50 nm and the silicon thickness 20 nm. The characteristics of 8 such nominally identical samples are shown in figure 17.
The consequence of removing the spacer is a very overlapped structure, where dopants implanted right at the edge of the gate (see figure 18) have a good chance to diffuse below the gate, both during the implantation itself and during the activation annealing. The microelectronics industry knows very well how to predict the resulting doping gradient. Figure 18 shows the simulations of the doping concentration, both in a continuous approximation and with discrete arsenic dopants, represented by spheres of radius the Bohr radius. These simulations therefore predict some source and drain (with a large roughness) extending well below the gate and a few atoms ‘disconnected’ in the middle region. Of course, since this becomes a very mesoscopic situation, we expect very large variations. It should be noted that the interplay between a single impurity like a dopant and the channel of a SET has been studied extensively in the past. Interestingly a single, capacitively coupled impurity gives rise to complex signatures in the low bias conductance and stability diagram of the SET [33, 49–51], which should be ruled out before interpreting lines in the stability diagrams in terms of excited states. Resonant tunneling through a single impurity located below the spacers and in series with the SET island also gives rise to characteristic features both at zero and finite bias [27].

6.2. Resonant tunneling through dopant states

The conductance in the low $V_g$ range for a sample with a very degraded sub-threshold slope is shown in figure 19. The very flat and smooth current at 300 K is replaced by two bumps evolving into very sharp peaks at low temperature, with resonating feature. Note that there is more current at 43 mK than at 90 K for the first peak, and even more than at 300 K for the second one. Estimations of the couplings $\Gamma_s, \Gamma_d$ to the source and drain have been obtained. For the first peak thermally broadened resonant tunneling describes the data all the way to the lowest temperatures. This indicates an intrinsic width of the first peak of the order of 100 mK, in agreement with the temperature dependence of the peak. For the second peak a saturation below a few Kelvin is observed, and couplings $\Gamma_s = 26$ GHz and $\Gamma_d = 120$ GHz are found [46] by fitting the data with a Lorentzian curve (Breit–Wigner resonance) and from the overall conductance at saturation ($0.58 e^2/h$).
Figure 20. Finite bias spectroscopy at 4.2 K for the same sample as figure 19. The two peaks turn into diamonds which remain sharp up to high $V_g$. From [46]. Copyright 2010 Nature Publishing Group.

Figure 21. Left: colorized TEM micrograph of a CMOS nanowire transistor. The gate is wrapped around the nanowire thanks to overetching of the buried oxide (BOX). Right: Room temperature $I_{ds}(V_g)$ characteristics of a typical PMOS single-hole transistor device. From [63]. Copyright 2015 American Chemical Society.

The finite bias spectroscopy is shown in figure 20 at 4.2 K. The gate voltage in this 2D plot can be transformed in energy, referenced from the conduction band edge found before, using the lever arm parameters obtained very accurately at each resonance. For instance we extract $\alpha = 0.16$ from the slopes of the first diamond occuring at $V_{g0}$, the corresponding energy is $e\alpha(V_{g0} - V_f) = 108 \pm 10$ meV. This energy scale is shown on the top axis of figure 20. As we identify these peaks with dopant atoms in the channel, this energy is the ionization energy of the donors: going from the negative values of $V_g$ towards zero, we observed the $D^+ \rightarrow D^0$ transitions for each donor (ionized $\rightarrow$ neutral). For the second peak a lower $\alpha$ factor is found (0.104) The value for the first peak, 108 meV, is markedly larger than the well-known value for Arsenic atom in bulk silicon, calculated more than 50 years ago [52]. The estimation of the energy of the bottom of the conduction band from the threshold voltage in samples which close well is, in our opinion, the most reliable, at least compared to other methods using the activation energy. We also performed activation energy analysis and observed that it is correlated to the two first peaks we observed [46]. In other words transport at high temperature occurs through these dopants when the current below $V_f$ is anomalously high, whereas samples which close well at $V_f$ have no such dopants well centered in the channel, through which thermally activated resonant transport can occur.

Figure 22. Stability diagram of a PMOS single hole transistor showing the filling of the quantum dot with the first holes. From [63]. Copyright 2015 American Chemical Society.

Clearly one difficult problem with the extraction of the ionization energy comes from the estimation of the reference or zero energy level. Tomography of up to three dopants has been performed recently thanks to the backgate and comparisons with realistic simulations of the global electric field within the channel, taking into account not only the dielectrics (gate oxides) but also screening by the conducting source/drain (see [53] and references therein).

Recently the use of the backgate allowed to monitor the effect of the electric field on the wave function of a single phosphorus donor atom in a CMOS device [41].

7. CMOS single accepotor devices

The study of single acceptors (as well as small P-type quantum dots in the first holes regime) started soon after single donors. This was motivated by results on GaAs heterostructures to implement spin quantum bits [54–56]. Indeed localized spins are a natural way to build a quantum computing platform in a solid-state device [57, 58]. Very recently it gained even more interest because of the very long spin coherence time [17, 18, 59] obtained in isotopically purified $^{28}$Si. Even with natural silicon reduced hyperfine interaction with nuclear spins is a great advantage of hole systems in Si compared to III–V materials [60]. Just like for donors, single acceptor states have also been studied both with the STM technique [61]. P-doped CMOS devices have been investigated recently in view of their potential interest for spin manipulation and processing [62, 63].

The Landé $g$ factor has recently been measured in a Boron single-acceptor CMOS device [62]. Figure 21(a) shows the cross section of a CMOS nanowire quantum dot. Its transconductance characteristics measured at 300 K with small bias is shown in figure 21(b). It exhibits an excellent sub-threshold slope of 64 mV per decade, as a result of the excellent electrostatic control resulting from the gate wrapped around the wire. The gate length is 20nm, hence this quantum dot is among the smallest, although its fabrication is very well controlled. The stability diagram measured at 260 mK is shown in figure 22. It shows the addition of the first holes in the channel. The first resonance appears around $V_g = 580$ mV, slightly above the threshold voltage measured at 300 K. The evolution of the $g$ factor versus orientation of the magnetic field has been studied.
and revealed a strong anisotropy which could be used for fast spin manipulation through modulation of the $g$ tensor [63].

8. CMOS coupled atom transistor

8.1. Device geometry

As the signatures of single dopants are better understood, we now turn to more complex, multi-gate designs, and we make use of the back gate technique explained in section 3.2. Figure 23 shows a colorized scanning electron micrograph and a 3D sketch of a device featuring two gates facing each other. The behaviour of this device in the regime where 2D electron gases are formed below the front gates, i.e. for positive $V_{g1}$ and $V_{g2}$ is shown in figure 24. As expected a regular lattice is found, with current all along the horizontal and vertical lines as the two dots are in parallel (for dots in series current is expected only at the intersection of these lines, as we will observe in the next section). The period is in agreement with the expected overlap between gate(s) and nanowire, and coupling between the two dots exists as the rectangular lattice is distorted near the crossings.

Figure 23. (a) Colorized SEM micrograph of a 2-gate device. Note that the gates face each other and the spacers completely fill the gap between them. (b) 3D drawing of the same device with the spacers removed for clarity. A first low doping with phosphorus (red) was performed in all the nanowire prior to gate deposition, while heavy arsenic doping (blue) was used after the gate and spacers module to define the source and drain. From [64]. Copyright 2012 American Physical Society.

Figure 24. Current through the device above the threshold voltages of both front gates. The typical signature of two dots in parallel is obtained. The separation of the crossing points which affects the otherwise rectangular lattice shows the coupling between the two dots.

Figure 25. First current peaks detected for $V_{bg} = +4$ V, corresponding to the onset of the conduction band in the two channels below the top gates.

It is more interesting to look at lower front gate voltages, i.e. depleting the channels below the top gates, while increasing the back gate voltage. At $V_{bg} = +4$ V, the first resonance in the channel is observed. This marks the onset of the conduction bands for the two channels, labelled $E_1$ and $E_2$ in figure 25. Below these lines, for this back gate voltage no other peaks are visible at lower front gate voltages. Increasing the back gate further, some remarkable features appear, shown in figure 26, which is recorded with a DC bias $V_3 = 3$ mV, hence this couple of triangles suggests a double-dot system, which in our case is ‘simply’ a 2-donor system. From [64]. Copyright 2012 American Physical Society.

Figure 25. First current peaks detected for $V_{bg} = +4$ V, corresponding to the onset of the conduction band in the two channels below the top gates.

Figure 26. Current detected for $V_{bg} = +11.5$ V. As the back gate voltage has increased, more features below threshold (i.e. below the lines $E_1$ and $E_2$) are observed. First, anti-crossings with the line $P_1$ indicate that the dopant atom responsible for this new line interacts with the channel. Lower in $V_{g1}$ and $V_{g2}$ a remarkable double triangular feature appears. This plot is recorded with a dc bias $V_3 = 3$ mV, hence this couple of triangles suggests a double-dot system, which in our case is ‘simply’ a 2-donor system. From [64]. Copyright 2012 American Physical Society.
8.2. Dopant states in the sub-threshold regime

More detailed investigations of this region are shown in figure 27. First, the two isolated triple points are shown with no dc bias (ac lock-in technique only with a small $V_d$ in figure 27(a)). In figure 27(b) the position of these two points is indicated schematically by the red points. The 2D plot is with $V_d = 3$ mV, like in figure 26, but at larger resolution and with an applied parallel magnetic field of 2 T, which results in an almost complete suppression of the current inside the triangle: mostly only the base of the triangle remains visible. The main effect of the magnetic field is probably to suppress inelastic processes, which are responsible for the current inside the triangle. Indeed, for two donors in series, at first order we expect current only at the base as this corresponds to the energy for which the levels for each donor are aligned. This is in contrast with the more usual case of metallic coupled dots where there is a continuum in energy instead of a single level. Another characteristic feature of 2 coupled discrete levels is the fact that the on-peak current does not depend on the applied bias. In other words we expect a constant current whatever the bias applied, instead of a fixed conductance (current increasing with the bias). This is shown in figure 28: 3 cuts across the baseline of the triangle are shown, for 3 bias voltages. Between 0.5 and 16 mV the current increases by less than 40%, whereas the bias voltage increased by a factor 32.

Before analyzing the spectroscopy at higher $V_d$, we will illustrate the importance of a double-donor system to perform spectroscopy. Just like with double dots [65], this situation ‘isolates’ the system from the source and drain in the sense that the finite temperature or local density of states in the contacts will not impact the data. Figure 29 shows the Coulomb diamonds for the single donor state $P_3$ (this data was taken along the red line in figure 26). The density of lines and the roughly equal number of negative and positive differential conductance lines is not a simple image of the spectroscopy of this donor state: we mostly see the fluctuations of the local density of states, which are necessarily important in our system where the contacts are made by the exact same dopants that we study, but just at much higher concentration. Although doping gradients are extremely well controlled in microelectronics, such a situation is unavoidable due to the nature of the contacts in high density CMOS scaling.

8.3. Atomic spectroscopy

As the 2D plots at $V_d = 3$ mV were still very sharp, we increased the source-drain bias further, and sharp features were observed up to 25 meV, a remarkably high value for transport spectroscopy in a solid-state device. This is another consequence of dealing with dopants instead of ‘artificial atoms’ such as quantum dots. Some results are shown in figure 30(a) for $V_d = 16$ mV. At such bias the two triangles merge, as their separation in energy is approximately 4 meV. As inferred from figure 28, the baseline is well separated from any other line. The faint line, with a pronounced curvature, observed in the middle of the triangle cannot be attributed to an intrinsic excited state of the double-donor system, as it has...
As there is more than 55 years of intense theoretical and experimental research on dopant’s spectra in silicon, only a brief summary will be given here. The topics regained even more interest in view of the quantum control required for quantum bits, for instance by coupling with surface states [66]. The electronic excitation spectra of donor states in bulk silicon are well described by theory and precisely measured by optical spectroscopy. Donor states differ from a hydrogenic-like atom for two main reasons. Firstly, the ground state (1s) is 6-fold degenerate because of the six equivalent conduction band minima of silicon. Secondly the so-called central-cell correction lifts this degeneracy as the effective mass approximation fails to describe the lowest lying states for which the electron moves in a tight orbit close to the ion [52]. For P donors this correction is responsible for the rather large (11.63 meV) valley-orbit splitting between the lowest lying (ground) state (1s(A1)) and the next one (1s(T2)) [67, 68]. The energy spectrum for the bulk case is shown in the leftmost sketch of figure 32(a). In a confined geometry, when the dopant atom comes close to an interface, the spectrum changes. This is due to the fact that the charge is repelled away from the interface (this is the dielectric mismatch seen before), hence away from the central-cell position as well. As a result the central-cell correction is reduced and so is the valley-orbit splitting. Such calculations have been performed by Yann-Michel Niquet at INAC. We computed the electronic structure of phosphorus impurities embedded in a 20 nm thick Si film [69, 70] with a sp3d5s* tight-binding model [71]. Figure 32(b) shows an image of the wavefunction amplitude for the next level above the ground (lowest) state. As the wavefunction is pushed away from the interface it is also less centered on the dopant site, and therefore the central-cell correction responsible for the valley-orbit splitting is smaller.

The differences between the ground state and the first five excited states are plotted as a function of the distance \( z_{imp} \) between the impurity and the lower Si/SiO\(_2\) interface in figure 32(c). The dashed horizontal lines are the corresponding bulk limits, i.e. the 1s(T2) and 1s(E) splittings. Due to the lower symmetry of the film, the first excited state (red line) is no more degenerate and at significantly lower energy than in bulk for \( z_{imp} \) below the Bohr radius of the impurity (\( \approx 2.2 \) nm). The next excited states are well above the first excited state, showing that the 1s(A1), 1s(T2) and 1s(E) states are completely mixed up to \( z_{imp} \approx 7 \) nm where an approximate triplet/doublet structure becomes clearly identifiable. This behavior results from the deformation of the impurity wave functions by quantum confinement, which controls the mixings and splittings between the six conduction band valleys of silicon [52]. Figure 32(c) shows the excitation spectrum for the first five 1s excited states of a phosphorus donor as a function of \( Z_{imp} \), the distance between the phosphorus atom and an infinite planar Si/SiO\(_2\) interface. The simulation is performed with no electric field but the conclusions remain valid for moderate electric field of order 10–20 mV nm\(^{-1}\), as estimated in our sample for the applied gate and substrate bias. We can therefore account for the main experimental observations (valley-orbit splitting of \( \approx 10 \) meV) if we suppose that \( P_1 \) and \( P_2 \) are located approximately 3 nm above the buried interface.

Figure 30. (a) Transport spectroscopy of the \( P_1, P_2 \) double donor system: same data as for figure 27(b) but with \( V_{G0} = 16 \) mV. (b) Energy levels in the double donor system. Of particular importance are the green lines parallel to the triangle base, due to resonant tunneling when ground or excited states of \( P_1 \) and \( P_2 \) are aligned. From [64]. Copyright 2012 American Physical Society.

Figure 31. Left: Energy spectrum versus energy detuning \( \varepsilon \) between \( P_1 \) and \( P_2 \) states, for different \( V_d \). Beyond the ground state, the 1s(T2) and 1s(E) levels stand out around 10 meV. Right: These peaks are fitted by two Lorentzian lineshapes and a background inelastic contribution.

Figure 32. (a) Left: splitting of the six-fold degenerate 1s ground state calculated for a phosphorus dopant atom in bulk silicon. Right: spectrum calculated for a donor located 3 nm away from a Si/SiO\(_2\) interface. (b) Color plot of the wavefunction amplitude calculated for the next level above the lowest lying state around a phosphorus donor (in grey) located 1.3 nm above an infinite Si/SiO\(_2\) located at \( z = 0 \). The wave function is less centered around the donor hence the central-cell correction is smaller. (c) First five 1s excited states of a phosphorus donor as a function of \( Z_{imp} \) the distance between the phosphorus atom and an infinite planar Si/SiO\(_2\) interface. The simulation is performed without electric field. The dashed horizontal lines are the result for bulk case, i.e. the 1s(T2) and 1s(E) degenerate states. The first excited state (in red) is non degenerate. The thick grey line corresponds to our observation of an energy splitting of \( \approx 10 \) meV.

to be parallel to the base of the triangle. Another indication that this line has a different origin lies in the fact that this line is specific to a certain bias polarity: at \( V_d = -16 \) mV this line simply isn’t there. More interesting, a line parallel to the base is well visible further away. Figure 31 shows cuts across the triangle. By principle the size of the triangle is the applied \( V_d \). This allows to determine experimentally the position of this first line: it appears for an energy of 10.3 ± 0.5 meV. Again this line does not depend much on the bias: figure 31 shows that this peak is nearly the same with \( V_d = -16, -18 \) and \( -20 \) mV.
9. Electron pumping through two dopants in series

Electron pumping has been recently investigated in dopant based systems [72–76]. Hereafter we consider the same device as in section 8. The set of triple points shown for instance in figure 27 as a separation in energy, of the order of 4 meV, allows one to perform a pumping experiment, namely turning around each of these points.

Figure 33, left shows cuts along the base of the triangles (the gate voltage \( V_{g} \) is simply a linear combination of \( V_{g1} \) and \( V_{g2} \) allowing to pass through these bases). No bias is applied but RF signals dephased by \( 180^\circ \) are applied on the gates. Clear plateaus at the expected value \( I = e\nu \) and sign reversal are observed, as a result of quantized charge pumping. Note that the frequency, however, is very small.

Figure 33 shows the frequency behaviour for both polarities. There clearly start to be a deviation after a few MHz. The coupling between the dopants has been estimated to be of the order of 60 MHz. First, from the 4 meV energy separation between the triple points a crude electrostatic variation in 1/\( r_{ij} \) yields a distance between dopants \( r_{ij} \approx 30 \) nm, which is very consistent with the geometry of the sample. In addition, photon-assisted tunneling experiments (not shown) have been performed. A quantum interference pattern was clearly observed, allowing to extract this estimation of 60 MHz for the tunnel coupling between the dopants [77]. Finally, using an estimation of the current expected for this tunnel rate depending on the distance [78] (i.e. the tail of the wavefunctions, far from the dopant site), we find again between 30 and 35 nm.

More experiments were performed on this system for which the number of experimental parameters is large. The effect of the contour shape (dephasing and amplitude of the RF signals) was especially studied, and showed clear and spectacular effects. We have identified the crucial role of non-adiabatic processes which are responsible for the finite current observed outside the regions in which a triple point is enclosed, and where pumped current should be zero. Indeed at low frequency only adiabatic pumping occurs and current is measured only in the usual circular regions, as shown in the right panel of figure 34. At higher frequency striking features are observed, as shown in figure 35. A compact model involving a Landau–Zener transition when the two levels cross each other has been developed at RWTH [73]. It accounts for the spectacular features observed in figure 35.

Further developments are in progress in order to use this modeling to give some new insights on the determination of inelastic as well as elastic charge relaxation rates in ultra small systems such as dopant-based devices [79].

10. Ultra-scaled, high temperature CMOS SETs

Research for the 11 nm node (and below) of the microelectronics roadmap involves device dimensions below 10 nm [80]. At this scale Coulomb blockade arises quite naturally and can be favored and exploited by changing only a few ingredients in
the standard integration scheme. We realized nanowires with extremely small cross sections (3.4 nm in diameter and 10 nm in length for the device shown in figure 36), but relatively long offset spacers (25 nm) in order to realize non invasive source-drain. We also deposited a thick (7 nm) gate oxide to increase the confinement and Coulomb interaction for carriers. The effect on the transport characteristics is dramatic since an atomic-like characteristics is observed continuously from low up to room temperature for the first time (see figure 37), in a device made on 300nm wafers in a CMOS facility using state-of-the-art deep-UV lithography, hence without electron beam lithography [81]. This sample layout enhances the role of interactions already present in transistor scaling since more than a decade and visible even at 300 K as a decrease of the maximum drain current as the gate length shrinks. This is in contrast with more than 50 years of progress during which shorter gate length meant higher current. In our ultra-scaled device the intra-channel electron interaction plays the leading role to explain the transport characteristics of the device. The channel forms a silicon single artificial atom transistor. We take into account in simulations the unavoidable imperfections such as line edge roughness and remote Coulomb scattering in order to get a quantitative agreement with the data. However even simulations without disorder capture qualitatively the main features. The addition energies are in the range of 150 meV. The orbital excited state is several tens of meV above the ground state and the valley-orbit splitting is 5 meV, a large value for an artificial structure, almost as large as for dopants [64]. The potential landscape in the device was computed with a non-equilibrium Green’s functions solver in the effective mass approximation. The geometry was chosen as close as possible to the TEM pictures. Electron–phonon interactions and surface roughness disorder were taken into account (Gaussian profile with rms value 0.25 nm and correlation length 5.2 nm). Exchange-correlation effects were described with a local density approximation supplemented with a semi-classical model for the image charges self-energy corrections. A detailed comparison with the experimental results can be found in [81].

11. Opportunities and challenges of a fully CMOS integrated quantum circuit

The previous sections have shown that carriers and dopants can be controlled at the level of one unit in advanced CMOS devices, provided that low temperature operation is considered. Low temperature operation is not a big obstacle for certain applications such as metrology, detectors or quantum computation. It should also be considered as an option to reduce dramatically the standby and dynamical power of conventional CMOS logic circuits. Indeed it is possible to reduce drastically the drain ($V_d$) and threshold voltages (in the 10 mV range) and therefore also the dynamic consumption ($\propto V_d^2$), while preserving very low OFF-state current levels thanks to very steep sub-threshold slopes ($\approx 1$ meV/decade). A careful estimation of the trade-off between consumption of the cryogenic machine versus gain in processors dissipation should be done for each specific application.

The FDSOI route is particularly adapted for such low power circuits. A fine adjustment of the threshold voltage can be obtained on-chip using local back gates, thanks to shallow trench isolation [25, 82].

The clearest advantage of producing CMOS quantum devices such as our MOS-SETs is their ability to be co-integrated with standard low temperature CMOS peripheral devices and circuits. This includes advanced logic field-effect transistors, electrostatic discharge protection diodes.

**Figure 36.** Top: Transmission electron micrograph image of the cross-section of an ultra-scaled nanowire. The gate oxide is made thicker than usual. Bottom: Simulated structure ($L_g = 10$ nm, diameter 3.4 nm including surface roughness) with the silicon in red, SiO$_2$ in green, HfO$_2$ in blue, TiN gate in grey, Si$_3$N$_4$ otherwise. From [80]. Copyright 2015 American Chemical Society.

**Figure 37.** Five resonances are identified which correspond to the addition of 5 electrons in our artificial atom. From [80]. Copyright 2015 American Chemical Society.
Acknowledgments

CMOS circuits on real plex structures such as coupled quantum bits or conventional they are the best candidates for the integration of more complex advances programs since they share the goal of fabricating extremely well controlled nanostructures. CMOS-based single dopant devices can reach the same level of performances as efficient detectors for fast qubit readout [45, 84–87].

Figure A1. Schematics of the whole circuit designed and fabricated on 300nm Silicon-On-Insulator wafers. The nanowire with a small cross-section which exhibits Single-Electron transport at low temperature is on the right, with the channels turning into Coulomb islands at low temperature highlighted in green. The CMOS circuit driving the gates is made of several sub-circuits. A voltage controlled oscillator, monitored through a frequency divider, feeds a clock generator also based on ring-oscillators. This generator delivers two signals delayed and phase-shifted in such a way that they never overlap. These oscillating outputs RF1 and RF2 are further attenuated by capacitive dividers and added with external DC biases in order to tune the right working point independently on each gate. Two other input signals, not represented on this schematics, are the VDD and GND voltage supplies to the CMOS circuit.

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Appendix. Hybrid classical/quantum integration in CMOS

Silicon electron pumps developed within standard microelectronics processes [74–76, 88] make it possible to cointegrate silicon circuits and therefore generate the RF signals on-chip. We designed, fabricated and operated at cryogenic temperature a ring oscillators based circuit delivering non-overlapping square signals on two gates of a nanowire transistor [83].

A schematic diagram of the whole circuit is shown in figure A1. The quantum device, on the right side of the diagram, is made with a 25 nm wide, 11 nm thick nanowire and is covered by 30 gates of length 40nm in series, with a spacing $S_{GS} = 170$nm. The gate stack consists of $\sim 0.8$nm of SiO$_2$,$\sim 2$nm HISiON, 5nm of TiN and 50nm of polycrystalline silicon. After gate etching a single, self-aligned 12nm Si$_3$N$_4$ spacer is deposited. The back-end process follows with epitaxy for raised source/drain, doping and silicidation (NiPtSi). The nanowire is connected to the outside of the cryostat by 4 pads (in black): two for the Source and Drain and two others for the DC biases to be applied on the gates of the SET.

The circuit for generating RF signals onto these gates at low temperature is made with the same technology than the SET, but a width $2 \times 1 \mu$m and 60 nm long gates. All the transistors are fed with a unipolar voltage given by external pads GND and VDD. The circuit starts with a Voltage-Controlled Oscillator (VCO) made of 20 invertors and 1 NAND gate. A voltage controlled current source is inserted in the invertors with an NMOS transistor in footer configuration. The VCO is

12. Conclusions and perspectives

Although single-dopant electronics is at an early stage, it is a quickly growing field, thanks to its potential applications. This review illustrates that this research can benefit from the massive and continuous progresses of the microelectronics advanced programs since they share the goal of fabricating extremely well controlled nanostructures. CMOS-based single dopant devices can reach the same level of performances than those processed with non-CMOS schemes. Furthermore they are the best candidates for the integration of more complex structures such as coupled quantum bits or conventional CMOS circuits on real ‘quantum chips’.

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and peripheral (input/output) transistors. Moreover it is clear that beyond the proof-of-concept step, any quantum function (an electron pump, a logical qubit) should be addressed, controlled and read out on chip by classical components, like voltage controlled oscillators, current and voltage amplifiers and converters or multiplexers. These components have been developed already for cooled detectors, whether for ground or space applications. What is required is some adaptation to fulfill the requirements in terms of noise level or dissipation for building a non-invasive interface with the fragile quantum core. The freezout at low temperature of passive or active components should be carefully addressed too, but is not a big challenge to overcome.

An exemple is the co-integration of a two-output clock generator based on a voltage control oscillator with a MOS-SET electron pump [83]. This circuit detailed in appendix operates down to $\sim 2$ K. Our CMOS quantum devices can also benefit from an efficient 3D integration. As shown in this review controlling the vertical electric field by front and back gate voltage in FDSOI offers many opportunities such as coupling a surface channel or surface quantum dot with a dopant in the body of the silicon channel, or coupling two surface channels on the front and buried interfaces. Because the coupling of quantum bits beyond the first neighbours is a difficult task, adding a third dimension for coupling or addressing the qubits could be interesting for large scale integration of qubits. The confinement by trench isolation or dielectrics is also very beneficial for density and integration compared to electrostatic confinement which requires too many gates per bit. Finally the very good coupling of our quantum dots with their control gate enables radio-frequency reflectometry on gates to be used as efficient detectors for fast qubit readout [45, 84–87].
switched on or off with the OSC input and its frequency is tuned by the voltage applied on the VCO pad. Its amplitude is given by the supply voltage VDD. According to the simulations, the VCO has an output frequency ranging from 300 kHz (VCO = 0.2 V) to 1.8 GHz (VCO = 1 V) at 300 K. This clock signal is monitored with a frequency divider. It feeds a second, non-overlapping clock generator with two outputs. It is made of 5 buffers allowing to shift by 108 ps the two signals, ensuring that only one of the two outputs is in the high (VDD) state at any time. The two outputs RF1 and RF2 are attenuated by capacitive dividers in order to reach amplitudes down to 0.5, 5 or 100 mV. Finally bias tees is realized with 1 MΩ resistors made of polysilicon in order to add a DC bias to each RF output.

The global circuit layout is shown in figure A2 for the one delivering an amplitude of 500 μV, with detailed views of the ring oscillator and nanoscale device. Each of the three circuits integrated on a single chip uses 12 aluminium pads for external control (see figure A2(a)). The passive components of the circuits are the poly-Si resistors (red squares) and the capacitors for the dividers. These are made between two metal layers in the back-end process and use a 2 pF / 1 fF combination in order to reach the desired attenuation. The 2 pF capacitors occupy a large surface area of the circuit (empty cyan squares in figure A2(a)). The ring oscillators and frequency divider are located between pads 3 and 4 (see figures A2(a) and (b)). They use very wide dual-channel devices (W = 2 × 1 μm) with gate lengths 60 nm as shown in figure A2(c). The SET device is located near the oscillators and the output of the capacitance divider (figure A2(d)).

The frequency response of the VCO down to low temperature is shown in figure A3 in Log-Lin scale. The ring oscillator being fed by NMOS transistors whose output current is controlled by the voltage VCO, we should obtain a curve looking like the drain-source versus gate voltage characteristic of an N-MOSFET, as confirmed by simulations. This is indeed observed, not only at room temperature but also at lower temperature. The maximum slope (corresponding to the sub-threshold of the NMOS) is 90 mV/decade at 300 K. At lower temperature we find a small degradation of this factor, with a maximum slope of 33 mV/decade at 77 K instead of 23 and 10 to 20 mV/decade at 4.2 K instead of 1.3. Despite this, the general behaviour of the VCO is perfectly suitable for being used at low temperature to drive a nanoelectronic device.

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