Analog/Mixed-Signal Circuit Synthesis Enabled by the Advancements of Circuit Architectures and Machine Learning Algorithms

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Abstract— Analog mixed-signal (AMS) circuit architecture has evolved towards more digital friendly due to technology scaling and demand for higher flexibility/reconfigurability. Meanwhile, the design complexity and cost of AMS circuits has substantially increased due to the necessity of optimizing the circuit sizing, layout, and verification of a complex AMS circuit. On the other hand, machine learning (ML) algorithms have been under exponential growth over the past decade and actively exploited by the electronic design automation (EDA) community. This paper will identify the opportunities and challenges brought about by this trend and overview several emerging AMS design methodologies that are enabled by the recent evolution of AMS circuit architectures and machine learning algorithms. Specifically, we will focus on using neural-network-based surrogate models to expedite the circuit design parameter search and layout iterations. Lastly, we will demonstrate the rapid synthesis of several AMS circuit examples from specification to silicon prototype, with significantly reduced human intervention.

I. INTRODUCTION

In traditional circuit design, there are clear boundaries between the digital back-end, analog mixed-signal (AMS) and radio frequency (RF) front-end circuits. As we are approaching the limits of CMOS technology scaling in terms of device size and power efficiency, improving the performance of conventional AMS circuits becomes incredibly challenging and inefficient. Therefore, circuit designers resort to architectural and/or system-level re-thinking. Consequently, co-design and co-optimization across devices, circuits, and algorithm have spawned significant number of innovations in interfaces (i.e., AMS) design. Driven by the growing performance and efficiency requirement of communication and computing system, the boundaries between analog and digital domain are blurring (Fig. 1). As a result, AMS circuits, especially data converters, become crucial to various emerging systems that need to cross between analog and digital domains. In a nutshell, the industry demands AMS circuits across a wide specification range (i.e., performance, power and area). However, the high degrees of freedom for optimizing such circuits poses a great challenge to deliver optimized designs within a reasonable time frame.

In addition, the increasing design cost in advanced technology nodes further necessitates the reduction of time to market [1], motivating AMS circuit synthesis.

However, the complexity for AMS circuit synthesis is generally higher than digital circuit synthesis. For example, constrained by the accuracy requirement of both continuous amplitude and time, simulations of analog circuits take significantly longer than that of digital circuits. Moreover, since the primitive design unit is down to transistor level instead of discrete digital standard cells, the parameter space of analog circuits is enormous compared to its digital counterpart, which demands substantially more iterations to achieve an optimum design. In addition, AMS design phases, including behavior modeling, schematic design and layout, require close guidance by the analog circuit designers, further increasing the design time.

All those factors set a higher barrier for AMS circuit synthesis.

On the other hand, AMS circuit has gradually moved towards digital-intensive, analog-lite architectures to leverage the benefits of technology scaling maximally and achieve high flexibility and enhanced performance simultaneously. The digital-intensive AMS circuit architectures enable the possibility of leveraging digital design flow to synthesize complex AMS circuits like data converters, phase-locked loops, and digital transceivers. Meanwhile, the advancement of machine learning (ML) algorithms has been exploding over the past decade. Many algorithmic innovations have resulted in significantly improved accuracy for various modeling and classification tasks.

This shift in AMS circuit architecture along with the recent advances in ML algorithms has provided a new opportunity for AMS circuit synthesis with high dimensional optimization, despite the aforementioned difficulties for AMS design. Moreover, a recent move toward open-source circuit design, including EDA tools and IPs, can potentially facilitate AMS circuit synthesis. In this paper, we will broadly review the emerging architectures and ML algorithms suitable for AMS circuit synthesis. Several representative synthesis examples will be provided. Lastly, we will discuss a potential open-source design ecosystem enabled by AMS circuit synthesis.

The rest of this paper is organized as follows. Section II reviews the mostly digital AMS architectures and the associated
techniques that favor design automation, especially standard digital design tools and flows. Next section III discusses the new opportunities in rapid AMS circuit synthesis enabled by the deep learning algorithms, focusing on the NN-based surrogate model for circuit parameter search. Design examples are provided in section IV. Section V describes the vision on open-source AMS design, followed by section VI which concludes the paper.

II. DIGITAL-EMPowered AMS Architectures

The key motivation of pushing AMS circuits towards more digitally-intensive architecture stems from the fact that analog circuits cannot leverage the CMOS technology scaling intrinsically as much as the digital circuits, in terms of both circuit performance and design cost. Due to the limited benefits offered by the scaling, architecture innovation has been the main driver of AMS circuit/system performance improvement [2] and [3]. As the CMOS technology has advanced to 5nm and below, the short-channel transistors continue to favor mostly digital AMS architectures with performance and cost advantages [4].

To illustrate the recent evolution of AMS circuits, we roughly divide the AMS architectures into three categories, as shown in Fig. 2. Starting around year 2000, applying digital signal processing techniques to assist or relax the analog circuit design became an active area of research (Fig. 2(a)). Motivated by [5] circuit designers pushed the performance of data converters and clock, which aimed to replace most analog signal conditioning by digital signal processing (DSP), making the system highly flexible (Fig. 2(b)). However, depending on the application, extremely high-performance data converters and PLLs might diminish the overall system efficiency. In such scenario, keeping some analog conditioning in the system while approximating the analog behaviors with digital-like operations can be a promising alternative (Fig. 2(c)). In the rest of this section, we elaborate those three types of AMS architectures in the context of AMS circuit synthesis.

A. Digitally-Assisted AMS Design

A major challenge in an AMS design is the fundamental trade-off between the area of the device and its mismatch. Larger device provides better matching but also leads to higher cost and lower speed. As transistors have been scaled down to 65nm and smaller, digital signal processing can relax the matching requirement of analog circuits with decent power- and area-efficiency. In [6], digital calibration is used to relax the precision requirement of the residue amplifier in a pipeline analog-to-digital converter (ADC) for significant power and area saving. Likewise, [7] proposed a background calibration technique based on adaptive filters to compensate for the nonlinearity of analog circuits in the ADC. More comprehensive calibration techniques have enabled new regime of high-performance ADCs [8]. Similarly, advanced digital pre-distortion and noise shaping techniques have been developed for wideband and high dynamic range digital-to-analog converters (DACs) [9]–[11]. In addition to the performance enhancement, the above digital calibrations also reduce the analog complexity and ease the design automation.

B. Mostly Digital AMS Architectures

In parallel, designers have demonstrated mostly-digital architectures in the direct sampling receiver [12] and DAC-based transmitter [13] using high-performance data converters for superior system flexibility. Such architectures have also been broadly explored for various AMS component blocks to leverage the increasing digital signal processing capability in advanced nodes. One such example is the digital phase-locked loop (DPLL), which has attracted much attention lately [14]–[19]. By pushing the control processing unit into digital domain completely, DPLL shows impressive robustness against process, voltage and temperature (PVT) variations and intrinsically allows digital calibration algorithms to improve the performance. More importantly, DPLL can be synthesized using standard digital design flow thanks to its mostly digital architecture. Fully synthesized DPLLs have demonstrated a significantly reduced implementation overhead with performance close to that of analog PLLs [15], [20]. Similarly, digital low-dropout regulator (DLDO) was proposed for low-noise and low-supply voltage applications [21]. Digitally-intensive dual-rate hybrid DAC was used to achieve high-speed and high-resolution simultaneously [22]. Likewise, thanks to its minimum analog complexity among the ADC architectures, successive approximation register (SAR) topology has been widely adopted [23], [24]. Since SAR ADC performs the conversion sequentially, the conversion rate inevitably slows down, as shown in the speed and complexity trade-off in Fig. 3. Time interleaving technique is typically utilized [25] to boost up the rate.

C. Digital-like AMS Operations

Another ongoing trend in AMS design is to use digital gates to achieve or approximate the analog functionalities in order to advance the circuit performance and reduce the design cost. Consider time-based ADC as an example. In recent years, the trend to operate time-based ADC above GHz sample rate has increased significantly. The ADC usually consists of a voltage-to-time converter for encoding the voltage information into
time domain and a time-to-digital converter (TDC) for quantizing the time. The TDC is either a delay-line or a voltage-controlled oscillator [26]–[29] and can be implemented by inverters and flip-flops only. Due to the smaller size of the digital circuits, fewer routing parasitics are expected in time-based ADCs. Moreover, digital circuits can achieve fast speed in advanced technology nodes without consuming too much power. As a result, the delay line based TDCs in [30] and [31] have reached up to 5GS/s using a single channel, which was previously only possible using Flash ADC or excessive paralleling (i.e., time interleaving), incurring significant area and power overhead. Along the same line, a design automation flow for a mostly digital voltage-controlled oscillator (VCO)-based delta-sigma ADC has been proposed and demonstrated recently [32]. Custom library and flow were combined with the digital design flow and scaling benefits were shown by comparing different processes. Likewise, [33] proposed a complete design automation flow including logic synthesis, placement, and routing schemes for time-domain computing circuits. In similar manner, [15] utilized NAND gates to implement the current digital-to-analog converter (DAC) for a current-controlled ring oscillator. A digital-based operational amplifier [34] was proposed as well, blurring the boundary between analog and digital circuits. Furthermore, a synthesized switched-R-MOSFET-C analog filter was demonstrated using digital standard cells [35]. In addition to these baseband circuit blocks, [36] and [37] approximated the amplitude-varying (i.e., analog) impulse response of an RF filter with a constant amplitude but a time-varying binary (i.e., digital-like) impulse response, such that the frequency responses are similar within a certain band of interest. Based on the specifications, the impulse response of a target filter is first designed using standard digital filter design flows, such as the FDA tool in MATLAB, followed by the time approximation via pulse-width modulation (PWM). In principle, such digital-like or time approximated AMS circuits favor the digital EDA tools [38], however specialized algorithms may be needed [33], [39].

III. NN-ASSISTED AMS DESIGN

To achieve a complete AMS circuit synthesis, one cannot solely rely on the architecture innovation by incorporating mostly digital design. New design methodology for AMS circuits is essential to tackle the grand challenges posed by advanced technology nodes (16nm and below), which results from the following observations:

- The device dimension is more discrete, yielding less degree of freedom for circuit sizing.
- Layout design rule is more complicated and constrained and hence harder for manual design.
- The device model and the layout parasitic extraction are more complex, dramatically increasing the simulation time.

Consequently, it is extremely costly to design a close-to optimal AMS circuit. Therefore, AMS circuit synthesis with reduced design efforts and sufficiently good performance is highly desirable.

AMS synthesis cast a long research history with various approaches demonstrated in the past decades. The paper focuses on the model-based methods due to their fast evaluation speed, reusability, and low computational cost. In the early days, the designers coded all the circuit knowledge in a hierarchical fashion [40] and synthesized relatively small circuit blocks like amplifiers. Geometric programming was also proposed to cast the Op-Amp design into a convex optimization problem [41] and later utilized for automating the design of analog PLL [42] and pipeline ADC [43]. Other surrogate models such as support vector regression [44], [45], neural network (NN) [46], and Gaussian process model [47], [48] have been widely explored for reducing the computational costs and model preparation overhead. Among the approaches, the NN regression outperforms others since it has more tunable hyperparameters, enabling accurate modeling of circuits which exercise a sophisticated non-linear function [49], [50]. Therefore, NN has been deployed in many computer-aided design (CAD) tools. In the rest of this section, we elaborate on the use of NN-based surrogate model for AMS design.

A. NN-based Surrogate Model and Parameter Search

A surrogate model can replace the SPICE model to avoid expensive SPICE simulations, especially the post-layout simulations in advanced technology nodes (Fig. 4). A NN surrogate model was proposed to characterize the circuit’s metrics in [51], [52]. A single NN model was used to predict the metrics of a circuit as simple as a single-stage amplifier or as complex as a PLL [53]. Unfortunately, similar to other regression
With behavioral or functional models, the modules' metrics are called modules and models these modules using regression. Combining global optimization and sufficiently accurate NN relations between two modules. Since estimating system specifications, genetic algorithm using SPICE simulations at first, then train perform local optimization with SPICE simulations, removing the system properly when interactions among the modules problem occurs. The module linking graph (MLG) concept proper interface characterization, without which interface parameter values for further optimization using SPICE simulation requires many iterations, NN modeled are then related to the system specifications. NN herein plays the role of module-level characterization, without which interface the system is a directed graph containing the modules as the vertices and the direction of the edges shows the cause and effect relations between two modules. Since estimating system specification with MLG requires many iterations, NN modeled modules are used in [56] but only for global optimization. Combining global optimization and sufficiently accurate NN models accelerates the search process while delivering nearly optimal results. After global optimization, [56] proposed to perform local optimization with SPICE simulations, removing the least significant parameters based on their gradients. The algorithm, called MOHSENN, can rapidly synthesize various AMS circuits with comparable or even better performance than manual design from an experienced designer.

The idea of MLG was further explored in [57]. Referred to as circuit connectivity inspired NN (CCI-NN), the NN structure was customized according to the circuit connection. The method achieves higher accuracy compared to the conventional fully-connected network (Fig. 5) given the same number of training data. Alternately, CCI-NN requires less training data to achieve the same model accuracy as a fully-connected network. Also, the network only requires a single dataset generated from the system simulations and does not need multiple training dataset for the modules and behavioral or functional modeling between modules' metrics and systems' specifications. CCI-NN can inherently learn the module-to-system relations and model the interfaces among the modules better. [57] showed that for proper modeling of an 8-bit 20GS/s current-steering DAC, CCI-NN required at least four times less training data compared to the regression models using conventional fully-connected NN.

Fig. 5: Concept of CCI-NN.

Fig. 6: Transfer learning from schematic to layout models.
one input linear layer and one output linear layer to the trained model, and only trains the new layers with a few post-layout samples. For the first time, [58] efficiently incorporated the layout parasitic information into the circuit surrogate model. Proved by experiments, this modeling method can effectively reduce the required training samples for a layout-level circuit model while maintaining a high modeling accuracy.

With this highly-efficient approach, [39] has successfully demonstrated a layout-aware AMS design flow from specification to layout, using an AMS filter as the test vehicle. [59] took one step further and applied TL to train a silicon-level circuit model and design the circuit incorporating both layout- and silicon-level information. This way, the NN-based approach for sophisticated AMS design has been significantly enhanced. Details of those design examples will be discussed in the next section.

C. Verification

SPICE simulation plays an important role in the AMS circuit synthesis. For example, one would rely on accurate simulation results for validating the synthesized circuit. Unfortunately, AMS circuit simulations, especially transient simulations, are typically time-consuming because of the inherent complexity of the SPICE models and the required number of samples for FFT evaluation. To address these limitations, simulations of unsatisfactory designs can be terminated according to early-stage simulation results, which can potentially save a significant amount of machine computation time. Some physical and empirical formulas can quickly estimate the performance but lack high accuracy of judgment. [60] proposed a convolutional neural network (CNN) based early performance assertion scheme, named CEPA, for fast and accurate verification. CEPA takes a short duration of a transient waveform to predict the satisfaction of the target specifications, which are typically obtained in the frequency domain after long transient simulations. Trained with a few samples, the CNN can extract both human-recognizable and -unrecognizable features from the short transient waveform and use such features for performance prediction. Note that the learned features from the schematic simulations can be transferred to the post-layout model, with only a small number of training data from the post-layout simulation. As an application, CEPA can quickly narrow down the feasible design parameter space, which helps to sample the training data for the NN-based surrogate model and hence expedite the whole parameter search process.

IV. PROPOSED DESIGN FLOW AND EXAMPLES FOR AMS SYNTHESIS

A. Analog/Mixed-signal Parameter Search Engine

Fig. 8 shows the proposed design flow based on an open-source AMS circuit generator, called Analog/Mixed-Signal Parameter Search Engine (AMPSE) [61], [62]. First, AMPSE developers select promising circuit architectures from known good designs (KGD), break them into smaller modules, and parameterize the modules. Then, the developers make testbenches for characterizing each module and build MLG based on the connection between the modules. After the preparation, modeling and parameter search can be fully automated without human in the loop. NN serves as the surrogate model to represent the mapping between the design parameters and performance metrics. The model is trained with a dataset generated from the SPICE simulation, which is assisted by CEPA for reduced training efforts. Transfer learning is applied to incorporate post-layout information for improving the modeling accuracy. When the surrogate models of all the modules are prepared, they are used for global parameter search by connecting the models using MLG and applying gradient-based search algorithms. Thanks to the fast inference of NN, the search process is accelerated by orders of magnitude compared to the SPICE simulation based global search. AMPSE also suggests local optimization with SPICE model to fine-tune the circuit performance. Owing to the decent accuracy achieved by the surrogate model, the optimum design can be expected near the parameter candidates from the global search stage. Hence, the local optimization requires only a small number of iterations. For final verification, the SPICE simulation with the combined netlist is performed in the end. The whole AMPSE flow leverages both designer’s knowledge and the recent advancement in machine learning and optimization, demonstrating highly automated and fast AMS circuit generation with a wide specification range and high performance.
B. Example 1: SAR ADC

In this example, the design was a SAR ADC from [56]. As shown in Fig. 9, the ADC consists of four modules, i.e., track/hold and DAC, comparator, SAR logic, and a driver. There were 26 design parameters and 5 design specs. The objective was to satisfy all the specs while minimizing the power consumption. Fig. 10 shows the MLG of the SAR ADC, where the shared edges among modules represent the interface elements. AMPSE could generate around 500 different design candidates within 7 minutes which satisfied the specs. Fig. 11 shows the corresponding "banana" curve of the SAR ADC obtained by AMPSE. The plot depicts the possibility of the design outcomes for a given numbers of bits and sample rates. For a 6-bit 500 MS/s case, AMPSE reached similar performance as global search using the SPICE model while achieving almost 700 times faster search speed than the simulation-based method.

C. Example 2: Delta-Sigma and RF DACs

In [60], we demonstrated the design of delta-sigma DAC in 65nm CMOS technology. The capacitor delta-sigma DAC consists of one inverter-based driver, one capacitor, and associated digital circuits. We first utilized CEPA to rapidly explore the design parameter space of the DAC and locate the feasible region as the target design space. We then used NN to model the mapping between the design parameters and the performance metrics within this design space and applied TL with post-layout simulation results to improve the model. Finally, we applied gradient descent on the NN model to search for the best possible design parameter combinations given the specifications. The DAC layout was generated using a mixed-signal layout flow [60]. The fully synthesized delta-sigma DAC achieved a 81 dB SFDR and 8.8-bit ENOB for 10 MHz signal bandwidth.

We have also explored RF-DAC-based AMS filter using time-approximation filter (TAF) architecture [37]. The filter mainly consists of eight-channel time-interleaved RF DACs and a TAF pattern control circuits. We synthesized the control circuits using standard digital design flow and the DACs using a custom mixed-signal layout flow. The custom flow incorporated the designer’s insights, such as symmetry and dummy constraints, to ensure high performance. A top-level script then integrated the two parts. To derive a nearly optimum filter response for the TAF, the impulse response was first designed based on the mathematical analysis and then optimized with a coordinate descent algorithm. This hybrid approximation scheme significantly reduced the time approximation errors of TAF over a wide range of filter’s specifications.

D. Example 3: Silicon verified and enhanced VCO design

In the last design example, we demonstrated a “from specification to silicon” design of voltage-controlled oscillators [59]. After training the schematic-level VCO model, we generated the layout samples using the ALIGN layout automation tool [63] and developed the layout-level model via TL. With the layout-level model, we designed ten different VCOs via AMPSE, laid out and taped out the silicon chip in the 12nm FinFET technology. The fabricated VCOs were measured and evaluated in terms of oscillation frequency and power consumption at different control voltages. Compared to the layout-level design results, the silicon measurement results showed a 12% mean square variation. We then performed TL to tune the model using silicon-level samples (i.e., measurement data) and used the updated model to re-design the VCOs.

Thanks to the silicon-level circuit model, the design flow could accurately predict the real silicon performance and found the corresponding design parameters with a 3.9% mean square prediction error.

V. OPEN-SOURCE ECOSYSTEM FOR AMS DESIGN

Moving forward, the growing demands and design cost of AMS circuits continuously challenge circuit designers and EDA tool developers. Besides, it is well-known that AMS circuit design is a highly specialized research area, where experienced designers’ knowledge and intuition play a key role in successful designs. The shortage of design expertise becomes the bottleneck of the current design capacity of the industry. The recent DARPA Posh Open Source Hardware (POSH) program aims for an open-source hardware IP
ecosystem. The open-source environment is widely adopted in software and digital design. However, it is still a fresh concept in the AMS circuit community for its technology dependency, IP sensitivity, reliability requirement etc. In Fig. 12, we present a potential AMS circuit design ecosystem for sustainable and secure IP sharing, aiming to dramatically increase the AMS design capacity. The open-source AMS IP developers choose the silicon-proven circuit architectures and conduct the AMPSE flow to generate the surrogate models for a relatively large design parameter space. To avoid leaking out the confidential device model information, the developers should use the open-source predictive technology model (PTM) [64] instead of the commercial process design kit (PDK) model for all the shared designs. The parameterized netlist, associated testbenches, and the surrogate models are all shared on the cloud. The IP developers can also upload verified design netlists with fixed parameters as KGDs. The IP users follow the procedure to obtain the desired AMS design:

1) Download the target IP netlist from the cloud.
2) Replace the PTM model used in the netlist with the actual PDK model.
3) Apply TL to obtain an accurate surrogate circuit model.
4) Use the surrogate model to find the circuit parameters that satisfy their design specifications.

IP users can also be developers by uploading the silicon/post-layout verified designs to the cloud repository. The kick-off of the open-source ecosystem can potentially lower the cost of AMS circuit development and promote more research outcomes to commercial products. Moreover, it can enable more complex AMS system innovation and integration that a single organization can never achieve.

VI. CONCLUSION

As the technology scaling no longer leads to cost reduction and significant circuit performance improvement, AMS design automation has been gaining increasing attention from both industry and academia. This paper discussed the two main thrusts of current AMS circuit synthesis: (1) AMS circuit evolution towards mostly digital architecture and (2) ongoing application of machine learning algorithms inEDA tools. After reviewing the pros and cons of the state-of-the-art approaches, a complete AMS design flow based on NN surrogate model has been presented with examples.

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