Applications of the quantum algorithm for Monte Carlo simulation to pricing of financial derivatives have been discussed in previous papers. However, up to now, the pricing model discussed in such papers is Black-Scholes model, which is important but simple. Therefore, it is motivating to consider how to implement more complex models used in practice in financial institutions. In this paper, we then consider the local volatility (LV) model, in which the volatility of the underlying asset price depends on the price and time. We present two types of implementation. One is the register-per-RN way, which is adopted in most of previous papers. In this way, each of random numbers (RNs) required to generate a path of the asset price is generated on a separated register, so the required qubit number increases in proportion to the number of RNs. The other is the PRN-on-a-register way, which is proposed in the author’s previous work. In this way, a sequence of pseudo-random numbers (PRNs) generated on a register is used to generate paths of the asset price, so the required qubit number is reduced with a trade-off against circuit depth. We present circuit diagrams for these two implementations in detail and estimate required resources: qubit number and T-count.

I. INTRODUCTION

With recent advances of quantum computing technologies, researchers are beginning considering how to utilize them in industries. One major target is finance (see [1] for a review). Since financial institutions are performing enormous tasks of numerical calculation in their daily works, speed-up of such tasks by quantum computer can bring significant benefits to them. One of such tasks is pricing of financial derivatives. Financial derivatives, or simply derivatives, are contracts in which payoffs are determined in reference to the prices of underlying assets at some fixed times. Large banks typically have a huge number of derivatives written on various types of assets such as stock price, foreign exchange rate, interest rate, commodity and so on. Therefore, pricing of derivatives is an important issue for them.

In derivative pricing, we represent random movements of underlying asset prices using stochastic processes and calculate a derivative price as a expected value of the sum of payoffs discounted by the risk-free interest rate under some specific probability measure. In order to calculate the expected value, Monte Carlo simulation is often used. There are quantum algorithms for Monte Carlo simulation [5][6], which bring quadratic speed-up compared with that on classical computers and there already exists some works which discuss application of such quantum algorithms to derivative pricing [7][9]. However, in order to bring benefits to practice in finance, previous works have some room to be extended. That is, previous works consider the Black-Scholes (BS) model [10][11]. Although the BS model is the pioneering model for derivative pricing and still used in many situations in today’s financial firms, it is insufficient to consider only the BS model as an application target of Monte Carlo for practical business for some reasons. First, for various types of derivatives, market prices of derivatives are inconsistent with the BS model. This phenomenon is called volatility smile, which will be explained in Section 1. In order to precisely price derivatives taking into account volatility smiles, financial firms often use models which have more degree of freedom than the BS models. Second, the BS model is so simple that analytic formulae are available for the price of some types of derivatives in the model. In such cases, Monte Carlo simulation is not necessary. Actually, banks use Monte Carlo simulation mainly for complex models which can take into account volatility smiles. Although it is the natural first step to consider Monte Carlo in the BS model, the above points motivate us to consider how to apply quantum algorithms for Monte Carlo to the advanced models.

In this paper, we will focus on one of the advanced models, that is, the local volatility (LV) model [12]. The LV model, which we will describe later, is the model in which a volatility of an asset price depends on the price itself and time, so the BS model is included in this category as a special case. With degrees of freedom to adjust the function form of volatility, the LV model can make derivative prices consistent with volatility smiles. So this model is widely used to price derivatives, especially exotic derivatives, which have complex transaction terms such as early redemption, in many banks.

In order to price a derivative by Monte Carlo simulation, we generate paths, that is, random trajectories of time evolution of asset prices, then calculate the expectation value of the sum of discounted payoffs which arise in each path. Since we cannot generate continuous paths on computers, we usually consider evolutions on a discretized time grid, using a random number (RN) for each time step, which represents the stochastic evolution in the step. In this paper, we focus on how to implement such a time evolution in the LV model on quantum computers.

We can consider two ways to implement the time evolution. In this paper, we call them the register-per-RN way and the PRN-on-a-register way. The difference between them is how
to generate RNs required to generate a path. The register-per-RN is adopted in previous papers [7,9]. In this way, following the procedure described in, e.g., [13], one creates a superposition of bit strings which correspond to binary representations of possible values of a RN, where the probability amplitude of a each bit string is the square root of the possibility that the RN take the corresponding value. The point is that one register is used for one RN, so the required qubit number is proportional to the number of RNs used to generate a path. This can be problematic in terms of qubit number when many RNs are required. The number of RNs is equal to that of time steps times and that of underlying assets. The number of time steps can be large for derivatives with long maturity. Maturity can be as long as 30 years, so if we take time grid points monthly, the total number of time steps is 360. The number of underlying assets can be multiple, and furthermore, there are situations where we must simultaneously consider assets concerning different derivative contracts in a portfolio, for example, XVA [7]. Assuming that the number of asset is $O(10)$ and that of time steps is $O(100)$, the total number of RNs becomes $O(10^3 \times 10^4)$. If we use a register with $O(10)$ qubits for each RN, the total qubit number can be $O(10^5)$ easily. The current state-of-art quantum computers have only $O(10)$ qubits [15]. Even if we obtain large-scale fault-tolerant machines in the future, the large qubit overhead might be required to make a logical bit (see [16] as a review and references therein). Therefore, calculations which require the large number of qubits as above might be prohibitive even in the future. This situation is similar to credit portfolio risk measurement, which is described in [17].

We are then motivated to consider the PRN-on-a-register way, which is proposed in [17]. In this way, one does not create RNs on different register, but generates a sequence of pseudo-random number (PRN) on a register. At each time step, the PRN sequence is progressed and its value is used to evolve the asset price. Therefore, the required qubit number does not depend on the number of RNs and is largely reduced. The drawback is the circuit depth. Here, we define the circuit depth as the number of layers consisting of gates on distinct qubits that can be performed simultaneously, as T-depth used in [18, 19]. Since calculations to update the PRN is sequentially performed on a register, the circuit depth is now proportional to the number of RNs. Since in the fault-tolerant computation some kinds of gates, for example T-gates in the Clifford+T gate set, can take long time to be run [20, 21], the sequential run of such gates might be also prohibitive in terms of calculation time [22]. At any rate, in the current stage, where it is difficult to foresee the spec of future quantum computers, we believe that it is meaningful to consider the implementation which saves qubits but consumes depth as a limit.

When it comes to the LV model, the PRN-on-a-register way becomes more motivating, since its disadvantage on the circuit depth compared with the register-per-RN way is alleviated. In the LV model, the volatility varies over time steps depending on the asset price, so the calculation for the time evolution is necessarily stepwise [6]. Therefore, the PRN-on-a-register way and the register-per-RN way are equivalent with respect to this point, that is, the circuit depth is proportional to the time step number in both ways. This is different from the situation in credit portfolio risk management [22], where, in the register-per-RN way, a register is assigned to each random number which determine whether each obligor defaults or not and parallel processing on different registers reduces circuit depth.

In this paper, we design the quantum circuits in the above two way in the level of elementary arithmetic. In doing so, we follow the policies of the two ways to the extent possible. That is, not only with respect to RNs but also in other aspects, we try to reduce qubits accepting some additional procedures in the PRN-on-a-register way, and vice versa in the register-per-RN way. For example, in the PRN-on-a-register way, we have to intermediately output the information of the volatility used to evolve the asset price at each time step and clear it by the next step. Otherwise, we need a register to hold the information per step and the required qubit number becomes proportional to the number of time steps. It is nontrivial to implement such a procedure and we will present how to do this later. Note that such clearing procedure is unnecessary in the register-per-RN way.

We then estimate the resources to implement the proposed circuits. We focus on two metrics: qubit number and T-count. As mentioned above, we see that the qubit number in the PRN-on-a-register way is independent from the time step number and much less than the register-per-RN way. The T-count is proportional to the time step number in the both ways. We see that in some specific setting the both ways yield the T-counts of same order of magnitude, except that in the PRN-on-a-register way is larger by some $O(1)$ factor.

The rest of this paper is organized as follows. Section II and III are preliminary sections, the former and the latter briefly explain the LV model and the quantum algorithm for Monte Carlo simulation, respectively. In section IV, we present the circuit diagram in the two way. In section V, we estimate qubit number and T-count of the proposed circuits. Section VI gives a summary.

II. LV MODEL

In this paper, we consider only the single-asset case, since it is straightforward to extend the discussion in this paper to the multi-asset case.

---

2 In this paper, we consider arbitrage-free and complete markets, standard assumptions for derivative pricing, so the number of stochastic factors is equal to that of assets. For details, see [3,4].

3 XVA is the term which collectively represents various types of Value Adjustment on derivative prices, for example, credit value adjustment (CVA), price subtraction taking into account the default of the counterparty. In this paper, we ignore such technical issues. If you are interested, see [15].

4 In the multi-asset case, parallel computing over assets is possible in the register-per-RN way.
A. Pricing of Derivatives

Consider a party A involved in a derivative contract written on some asset. We let $S_t$ denote a stochastic process which represents the asset price at time $t$, which is set as $t = 0$ at the present. We assume that the payoffs arise at the multiple times $t^p_i, i = 1, 2, \ldots$ and the $i$-th payoff is given by $f^p_i(S_{t^p_i})$, where $f^p_i$ is some function which maps $\mathbb{R}$ to $\mathbb{R}$. The positive payoff means that A receives a money from the counterparty and the negative one means vice versa. For example, the case where A buys an European call option with the strike $K$ corresponds to

$$f^p_1(S_{t^p_1}) = \max \{ S_{t^p_1} - K, 0 \}$$

(1)

with a single payment date $t^p_1$. Note that this type of derivative contract is too simple to cover all trades in financial markets. For example, callable contracts, in which either of the parties has a right to terminate the contract at some times, are widely dealt in markets. We leave studies for such exotic derivatives for future works and, in this paper, consider only those which can be expressed in the above form.

Following the theory of arbitrage-free pricing, the price $V$ of the contract for A is given as follows [3,4] :

$$V = E \left[ \sum_i f^p_i(S_{t^{p_i}}) \right],$$

(2)

where $E[\cdot]$ represents the expectation value under some probability measure, the so-called risk-neutral measure. Here and hereafter, we assume that the risk-free interest rate is 0 for simplicity.

B. LV Model

In the LV model, the evolution of the asset price is modeled by the following stochastic differential equation (SDE)

$$dS_t = \sigma(t, S_t)dW_t$$

(3)

in the risk-neutral measure[4] $W_t$ is the Wiener process which drives $S_t$. $dX_t$ is the increment of a stochastic process $X_t$ over an infinitesimal time interval $dt$. The deterministic function $\sigma : [0, \infty) \times \mathbb{R} \rightarrow [0, \infty)$ is the local volatility. Note that the BS model corresponds to the case where

$$\sigma(t, S_t) = \sigma_{BS} S_t,$$

(4)

where $\sigma_{BS}$ is a positive constant, which we hereafter call a BS volatility.

The LV model was proposed to explain volatility smile. In order to describe this, let us define implied volatility first. In the BS model, a price of a European call option with strike $K$ and maturity $T$ at $t = 0$ is given by the following formula:

$$V_{\text{call,BS}}(T, K, S_0, \sigma_{BS}) = \Phi_{SN}(d_1)S_0 - \Phi_{SN}(d_2)K$$

$$d_1 = \frac{1}{\sigma_{BS} \sqrt{T}} \left[ \ln \left( \frac{S_0}{K} \right) + \frac{1}{2} \sigma_{BS}^2 T \right]$$

$$d_2 = d_1 - \sigma_{BS} \sqrt{T},$$

(5)

where $\Phi_{SN}$ is the cumulative distribution function of the standard normal distribution. We can price the option if we determine the BS volatility. Conversely, given the market price of the option $V_{\text{call,mkt}}(T, K)$, we can reversely calculate the BS volatility. That is, we can define the following function of $K$ and $T$:

$$\sigma_{TV}(T, K) :$$

$$\sigma_{TV}(T, K) \text{ s.t. } V_{\text{call,BS}}(T, K, S_0, \sigma_{TV}(T, K)) = V_{\text{call,mkt}}(T, K).$$

(6)

We call BS volatilities drawn back from the market option prices by [5] as implied volatilities.

If the market is described well by the BS model, implied volatilities $\sigma_{TV}(T, K)$ take a same value for any $K$ and $T$. Although this is the case for some markets, $\sigma_{TV}(T, K)$ varies depending on $K$ and $T$ in many markets. Especially, if $\sigma_{TV}(T, K)$ depends on $K$, it is said that we observe the volatility smile for the market.

Volatility smiles mean that possible scenarios of asset price evolution in the BS model do not match those which market participants consider. For example, if market participants think that extreme scenarios, big crashes or sharp rises, are more possible than the BS model predicts, the volatility smile arises. In fact, it is often said that the Black Monday, the big crash in the stock markets at 1987, was one of triggers of appearance of volatility smiles.

With the LV model, we can make European option prices given by the model consistent with any market prices, as long as there is no arbitrage in the market. This is intuitively apparent since we can expect that the degree of freedom of the local volatility $\sigma_t(S, t)$ as a two-dimensional function is available to reproduce the two-dimensional function $V_{\text{call,mkt}}(T, K)$. In fact, if we can get $V_{\text{call,mkt}}(T, K)$ as a function, that is, the market option prices for continuously infinite strikes and maturities, we can determine $\sigma(T, K)$ which reproduces $V_{\text{call,mkt}}(T, K)$ as follows[12]:

$$\sigma^2(T, K) = 2 \frac{d}{dK} V_{\text{call,mkt}}(T, K).$$

(7)

In reality, the market option prices are available only for several strikes and maturities. Therefore, in the practical business, we usually use a specific functional form of $\sigma(t, S)$ with degrees of freedom sufficient to reproduce several available market option prices. In this paper, we use the following form. First, we set the $n_t$ grid points in the time axis, $t_0 = 0 < t_1 < t_2 < \ldots < t_n$. Second, we set the $n_S$ grid points in the asset price axis for each time grid point, that is, $s_{i,1}, \ldots, s_{i,n_S}$ for $t_i$. Then, $\sigma(t, S)$ is set as follows:

$$\sigma(t, S) = a_{i,j} S + b_{i,j}; \text{ for } s_{i,j-1} \leq S < s_{i,j}, j = 1, \ldots, n_S + 1$$

(8)
for \( t_{i-1} \leq t < t_i \), where \( a_{i,j}, b_{i,j} \) are constants satisfying \( \sigma(t, S) > 0 \) for any \( t \) and \( S \) and \( s_{i,0} = -\infty, s_{i,n+1} = +\infty \). In other words, the two-dimensional space of \((t, S)\) is divided in the direction of \( t \) and in each region \( \sigma(t, S) \) is set to a function which is piecewise-linear with respect to \( S \). In this paper, we assume that \( a_{i,j}, b_{i,j} \) are preset to the value for which the option prices in the LV model, which we here write as \( V_{\text{call}}(T, K, S_0, \{a_{i,j}\}, \{b_{i,j}\}) \), match the market prices by some standard. For example, they can be set to

\[
\arg\min_{\{a_{i,j}\}, \{b_{i,j}\}} \sum_i \left[ V_{\text{call}}(T_i, K_i, S_0, \{a_{i,j}\}, \{b_{i,j}\}) - V_{\text{call,mkt}}(T_i, K_i) \right]^2,
\]

where \( (T_i, K_i) \)'s are several sets of maturity and strike for which the market option prices are available.

C. Monte Carlo simulation in the LV model

We here describe how to calculate the derivative price \([2]\) in the LV model by Monte Carlo simulation.

First, we have to discretize the time into sufficiently small meshes, since we can deal with the continuous time on neither classical nor quantum computers. For simplicity, we set the time grid points to the above \( t_i \)'s, those for the LV function. Then, the time evolution given by \([3]\) is approximated as follows:

\[
\Delta S_{t_i} := S_{t_{i-1}} - S_{t_i} \approx \sigma(t_i, S_{t_i}) \sqrt{\Delta t_i} w_i, \Delta t_i = t_{i+1} - t_i,
\]

where \( w_1, \ldots, w_n \) are independent standard normal random numbers (SNRs). Among various ways to discretize the SDE, we here adopt the Euler-Maruyama method \([23]\).

Even after time discretization, we cannot consider all of continuously infinite patterns of SNRs. One solution for this is discretized approximation of SNRs. We can choose the finite numbers of the grid points and assign probability to each point so that standard normal distribution is approximately reproduced. Now, the patterns of discretized SNRs are finite, so we can approximate \([2]\) as

\[
V \approx \sum_n p_n \sum_i f_i^{\text{pay}} \left( S_i^{(n)} \right),
\]

where \( p_n \) is the probability that the \( n \)-th pattern of values of SNRs are realized and \( S_i^{(n)} \) is the asset price at time \( t \) in the \( n \)-th pattern.

There are some possible ways to take patterns considered in \([11]\). In the register-per-RN way, we take all patterns. If we take \( N \) grids to discretize each of \( n_t \) SNRs, the number of possible patterns of SNRs is \( N^n_t \). Although this is exponentially large, quantum computers can take into account all patterns with a polynomial number of qubits by quantum superposition.

On the other hand, this cannot be adopted on classical computers, since the number of the SNRN patterns are exponentially large. Usually, Monte Carlo pricing on classical computers is done in the following way, which the PRN-on-a-register way is also based on. We consider sampled patterns of SNRs. That is, we generate finite but sufficiently many sample sets of \((w_1, \ldots, w_n)\) and use them to generate sample paths of the asset price which evolves according to \([10]\). We then approximate \([2]\) by the average of sums of payoffs in sample paths,

\[
V \approx \frac{1}{N_{\text{path}}} \sum_{n=1}^{N_{\text{path}}} \sum_i f_i^{\text{pay}} \left( S_i^{(n)} \right),
\]

where \( S_i^{(n)} \) is the value of the asset price at time \( t \) on the \( n \)-th sample path and \( N_{\text{path}} \) is the number of sample paths.

III. QUANTUM ALGORITHM FOR MONTE CARLO SIMULATION

A. outline of the algorithm

We here review the quantum algorithm for Monte Carlo simulation\([5, 6]\). It can be divided into the following steps. First, we create a superposition of possible values of a random number used to calculate a sample value of the integrand on a register. If multiple random numbers are necessary to calculate the integrand, one register is assigned per random number. As mentioned above, continuous random numbers must be approximated in some discretized way. Second, we calculate the integrand into another register, using the random numbers. Note that the results for many patterns of random numbers are simultaneously calculated in quantum parallelism. Third, by controlled rotation, the integrand value is reflected into the amplitude of the ancilla. Finally, amplitude estimation \([6, 24, 25]\) on the ancilla gives the expectation value of the integrand.

The quantum state is transformed as follows:

\[
|0\rangle |0\rangle |0\rangle \\
\rightarrow \sum_i \sqrt{p_i} |x_i\rangle |0\rangle |0\rangle \\
\rightarrow \sum_i \sqrt{p_i} |x_i\rangle |f(x_i)\rangle |0\rangle \\
\rightarrow \sum_i \sqrt{p_i} |x_i\rangle |f(x_i)\rangle \left( \sqrt{1 - f(x_i)} |0\rangle + \sqrt{f(x_i)} |1\rangle \right).
\]

Here, the first, second and third kets correspond to the random number registers, the integrand register and the ancilla, respectively. \( x_i \) represents the binary representation of values of random numbers in the \( i \)-th pattern and \( p_i \) is the probability that it realizes. \( f \) is the integrand and \( f(x_i) \) is its value for \( x_i \). Note that the probability to observe \( 1 \) on the ancilla is \( \sum_i p_i f(x_i) \), the integral value which we want. Although we do not explain how to estimate the probability amplitude in this paper, it is studied in many papers. For example, see \([6, 24, 25]\). Using such methods, we can estimate the integral with the statistical error which decays as \( O(N^{-1}) \), where \( N \) is the number of oracle calls. This decay rate is quadratically faster than that in the classical algorithm, \( O(N^{-1/2}) \).
B. the scheme using the PRN generator

We here briefly review the quantum way for Monte Carlo simulation using the PRN generator. The calculation flow for the current problem, the time evolution of asset price in the LV model, based on this way is described in Section IV B.

It is proposed in [12] in order to reduce the required qubits to generate RNs in the application of the quantum algorithm for Monte Carlo to extremely high-dimensional integrations. When it is necessary to generate many RNs to compute the integrand, the naive way, in which we assign a register to each RN and create a superposition of possible values, leads to the increase of qubit numbers in proportion to the number of RNs. In order to avoid this, we can adopt the following way. First, we prepare two registers, \( R_{\text{samp}} \) and \( R_{\text{PRN}} \). Then, we create a superposition of integers which specify the start point of the PRN sequence, on \( R_{\text{samp}} \). With the start point, we sequentially generate PRNs on \( R_{\text{PRN}} \). This is possible because a PRN sequence is a deterministic sequence whose recursion equation is explicitly given, and in [12] we gave the implementation of one of PRN generators on quantum circuits. Using the PRNs, we compute the integrand step by step, which corresponds to time evolution of the asset price and calculation of payoffs in this paper. Finally, the expectation value of the integrand is estimated by quantum amplitude estimation. In this way, since we need only \( R_{\text{samp}} \) and \( R_{\text{PRN}} \) to generate PRNs, the required qubit number is now independent from the number of RNs and much smaller than the naive way. The drawback is the increase of the circuit depth.

IV. CIRCUIT DESIGN

Now, we present quantum circuits for time evolution of an asset price in the LV model in the two ways: PRN-on-a-register and register-per-RN.

A. elementary gate

Before we present circuits, we here list up elementary gates we use.

- Adder: \(|x\rangle |y\rangle \rightarrow |x + y\rangle |y\rangle\)
- Controlled Adder:
  \(|c\rangle |x\rangle |y\rangle \rightarrow \begin{cases} |c\rangle |x + y\rangle |y\rangle & ; \text{for } c = 1 \\ |c\rangle |x\rangle |y\rangle & ; \text{for } c = 0 \end{cases}\)
- Multiplier: \(|x\rangle |y\rangle |z\rangle \rightarrow |x\rangle |y\rangle |z + xy\rangle\)
- Divider: \(|x\rangle |y\rangle |0\rangle \rightarrow |x\rangle |y\rangle |x/y\rangle\)

We here simply assume their existence. Actually, implementation of such elementary arithmetics are widely studied in previous works: see, for example, [26–46]. We will discuss the implementation in Section V A.

With these, we can construct other types of arithmetic we use. For example, subtraction \(|x\rangle |y\rangle \rightarrow |x - y\rangle |y\rangle\) can be done as addition by the method of 2’s complement. Comparison \(|x\rangle |y\rangle |z\rangle \rightarrow |x\rangle |y\rangle |z + (x > y)\rangle\) can be done as subtraction in 2’s complement method, since the most significant bit represents whether the result of subtraction is positive or negative. So a comparator is constructed as two adder, including uncomputation.

Note that the above multiplier uses two registers as operands and outputs the product into another register. Most of previously proposed multipliers are of this output-to-other type. On the other hand, we also need the self-update type of multiplier which updates either of input registers with the product, otherwise we have to add a register for each multiplication and qubit number explodes. Such a operation is realized by the following trick. When we want to multiply \( x \) by \( y \), given the two registers holding \( x \) and \( y \) and an ancilla register, we can do:

\[ |x\rangle |y\rangle |0\rangle \rightarrow |x\rangle |y\rangle |xy\rangle \rightarrow |xy\rangle |y\rangle |x\rangle \rightarrow |xy\rangle |y\rangle |0\rangle. \]  

Here, the first step is output-to-other multiplication. The second step is swap between the first and third registers, which is not necessary if we change our recognition on which of two registers is ancillary at every multiplication. The third step is the inverse operation of division.

B. the PRN-on-a-register way

1. calculation flow

We first present the calculation flow in the PRN-on-a-register way. We consider the flow until calculation of the sum of payoffs, which corresponds to from the first to the third line in (13), since the controlled rotation in the fourth line does not depend on the problem.

In the PRN-on-a-register way, PRNs are used for evolution of the asset price (10). More concretely, we preselect some sequence of pseudo standard normal random numbers (PSNRNs) and divide it into subsequences, then evolve the asset price using them.

Before we present the calculation flow, we explain some setups. We prepare the following register:

- \( R_{\text{samp}} \)
  This is a register where a superposition of integers which determine the start point of the PSNRN sequence. We write its qubit number as \( n_{\text{samp}} \). \( n_{\text{samp}} \) is the number of sample paths we generate.

- \( R_{\text{W}} \)
  This is a register where we sequentially generate PSNRNs.

- \( R_{\text{S}} \)
  This is a register where the value of the asset price is stored and which we update for each time step of the evolution, using \( R_{\text{W}} \).
• $R_{\text{payoff}}$

This is a register into which the payoffs determined by $R_S$ are added.

Note that we need some ancillary registers in addition to the above registers. We assume that the required calculation precision is $n_{\text{dig}}$-bit accuracy and $R_W, R_S, R_{\text{payoff}}$ and ancillary registers necessary to update them have $n_{\text{dig}}$ qubits.

We assume that the following gates are available to generate a sequence of PSNRNs.

• $P_W$

This progresses a PSNRN sequence by one step. In other words, it acts on $R_W$ and updates $x_i$ to $x_{i+1}$, where $x_i$ is the $i$-th element of the sequence: $|x_i\rangle \rightarrow |x_{i+1}\rangle$.

• $J_W$

This lets the PSNRN sequence jump to the starting point. That is, it is input an integer $i$ on a register and outputs $x_{i+n_t}$ into another register which is initially set to $|0\rangle$: $|i\rangle |0\rangle \rightarrow |i\rangle |x_{i+n_t}\rangle$. Remember that $n_t$, the number of time steps, is equal to the number of RNs used to generate one sample path.

The concrete implementation of these gates is discussed later.

Then, the calculation implementation is as follows:

1. Initialize all registers to $|0\rangle$ except $R_S$, which is initialized to $|S_{b_0}\rangle$.

2. Generate a equiprobable superposition of $|0\rangle, |1\rangle, ... , |N_{\text{samp}}-1\rangle$, that is, $\frac{1}{\sqrt{N_{\text{amp}}}} \sum_{i=0}^{N_{\text{amp}}-1} |i\rangle \text{PRN}$ on $R_{\text{amp}}$. This is done by operating a Hadamard gate to each of $n_{\text{amp}}$ qubits.

3. Operate $J_W$ to set $x_{i+n_t}$ to $R_W$, where $i$ is determined by the state of $R_{\text{amp}}$. These are the starting points of subsequences.

4. Perform the time evolution (10) using the value on $R_W$. $R_S$ is updated from $|S_{b_0}\rangle$ to $|S_{b}\rangle$.

5. Calculate the payoff at time $t_1$ and add into $R_{\text{payoff}}$.

6. Operate $P_{\text{PRN}}$ to update $R_W$ from $x_{i+n_t}$ to $x_{i+n_t+1}$.

7. Iterate operations similar to 4-6 for each time steps until the time reaches $t_n$.

8. Finally we obtain a superposition of states in which the value on $R_{\text{payoff}}$ is the sum of payoffs in each sample path. Estimate the expectation value of $R_{\text{payoff}}$ by methods like [6, 24]. This is an estimate for (12).

Here and hereafter, we assume that a payoff arises at each time step, for simplicity.

The flow of state transformation is as follows:

$$|0\rangle |0\rangle |S_{b_0}\rangle |0\rangle \rightarrow \frac{1}{\sqrt{N_{\text{amp}}}} \sum_{i=0}^{N_{\text{amp}}-1} |i\rangle |0\rangle |S_{b_0}\rangle |0\rangle \rightarrow \frac{1}{\sqrt{N_{\text{amp}}}} \sum_{i=0}^{N_{\text{amp}}-1} |i\rangle |S_{b_0}\rangle |0\rangle $$

$$\rightarrow \frac{1}{\sqrt{N_{\text{amp}}}} \sum_{i=0}^{N_{\text{amp}}-1} |i\rangle |S_{b_0}\rangle |0\rangle \rightarrow \frac{1}{\sqrt{N_{\text{amp}}}} \sum_{i=0}^{N_{\text{amp}}-1} |i\rangle |x_{i+n_t}\rangle |S_{b_0}\rangle |0\rangle $$

$$\rightarrow \frac{1}{\sqrt{N_{\text{amp}}}} \sum_{i=0}^{N_{\text{amp}}-1} |i\rangle |x_{i+n_t}\rangle |S_{b_0}\rangle |0\rangle \rightarrow \frac{1}{\sqrt{N_{\text{amp}}}} \sum_{i=0}^{N_{\text{amp}}-1} |i\rangle |x_{i+n_t}\rangle |S_{b_0}\rangle |0\rangle \rightarrow \frac{1}{\sqrt{N_{\text{amp}}}} \sum_{i=0}^{N_{\text{amp}}-1} |i\rangle |x_{i+n_t}\rangle |S_{b_0}\rangle |0\rangle $$

$$\rightarrow \frac{1}{\sqrt{N_{\text{amp}}}} \sum_{i=0}^{N_{\text{amp}}-1} |i\rangle |x_{i+n_t}\rangle |S_{b_0}\rangle |0\rangle \rightarrow \frac{1}{\sqrt{N_{\text{amp}}}} \sum_{i=0}^{N_{\text{amp}}-1} |i\rangle |x_{i+n_t}\rangle |S_{b_0}\rangle |0\rangle.$$  (15)

where the first, second, third and fourth kets correspond to $R_{\text{amp}}, R_W, R_S$ and $R_{\text{payoff}}$, respectively.

2. overview of the circuit

Schematically, the circuit which realizes the flow (15) is as shown in Figure [4]. In the figure, the gate $U_j$ corresponds to the $j$-th step of asset price evolution, that is, the $j$-th iteration of step 4-6 in the above calculation flow.

$U_j$ is implemented as shown in Figure [2]. $P_W$ is already explained and the gate Payoff, calculates $f_j^{\text{Pay}}(S_j)$ using $R_S$ and adds it into $R_{\text{payoff}}$. In addition to these, $U_j$ has gates $V_j^{(i)}, ..., V_j^{(n_s)}$, which update $R_S$.

The detail of $V_j^{(i)}$ is shown in Figure [3]. This gate (i) checks whether the asset price is in the $k$-th interval $[s_{j,k-1}, s_{j,k})$, (ii) if so, update $R_S$ using the LV in the interval, (iii) clears the intermediate output. It requires ancillary registers $R_{\text{count}}, R_Y$ and $R_g$. They have $\log_2 n_t$, $n_{\text{dig}}$ and 1 qubits respectively. At the start of $V_j^{(i)}$, $R_{\text{count}}$ takes $|j\rangle$ or $|j+1\rangle$ and the others take $|0\rangle$. Then the detailed calculation flow is:

1. If $R_{\text{count}}$ is $j$ and $R_S$ is in $[s_{j,k-1}, s_{j,k})$, flip $R_g$.

2. If $R_g$ is 1, update $R_S$ as

$$S_{t_j} \rightarrow S_{t_{j+1}} = S_{t_j} + (a_{j,k} S_{t_j} + b_{j,k}) \sqrt{\Delta t_j x_{i+n_t}}$$  (16)

using the value $x_{i+n_t}$ on $R_W$ and add 1 to $R_{\text{count}}$.

3. Calculate

$$S_{t_{j+1}} - b_{j,k} \sqrt{\Delta t_j x_{i+n_t}} \frac{1}{1 + a_{j,k} \sqrt{\Delta t_j x_{i+n_t}}}$$  (17)

into $R_S$, using the value on $R_S$ as $S_{t_{j+1}}$ and that on $R_W$ as $x_{i+n_t}$. 

$$$$
4. If $R_{\text{count}}$ is $j+1$ and $R_S$ is in $(s_{j,k-1}, s_{j,k})$, flip $R_g$. This uncomputes $R_g$.

5. Do the inverse operation of 3.

Let us explain the meaning of this flow. First, $R_{\text{count}}$ is necessary as an indicator of whether the $j$-th step of evolution has been already done or not. Without this, it is possible that the asset price is doubly updated in a time step. If and only if the $j$-th step has not been done, that is, $R_{\text{count}}$ is $j$ and the asset price is in $(s_{j,k-1}, s_{j,k})$, the update of the asset price with the LV function $a_{j,k}S + b_{j,k}$ is done. To do this conditional update, the check result is immediately output to $R_S$ and the gate corresponding to $R_S$ is operated on $R_g$ and the state is transformed from $|j⟩|$ to $|j+1⟩$ and all intermediate outputs on ancillary registers are cleared.

We here mention a restriction on the LV model so that it can be implemented in the PRN-on-a-register way. Note that through $V_1^{(j)}$, ..., $V_{n+1}^{(j)}$ the state is transformed from $|j⟩|S_{t_j}^{(i)}⟩$ to $(j+1)|S_{t_j}^{(i)}⟩$, where the first and second kets correspond to $R_{\text{count}}$ and $R_S$ respectively and other registers are omitted since they are unchanged. This means that the map from $S_{t_j}^{(i+1)}$ to $S_{t_j}^{(i)}$ must be one-to-one correspondence, since unitarity is violated if not. Actually, this is not so strong restriction. As shown in Appendix, if we set $a_{i,j}, b_{i,j}$ so that $\sigma(r_i, S)$ is continuous with respect to $S$ and we set $\Delta t_j$ is small enough that the increment $\Delta S_{t_j}$ is much smaller than $S_{t_j}$ itself, the above condition is satisfied.

This one-to-one correspondence lets Step 3 work. That is, since the map between $S_{t_j}^{(i)}$ and $S_{t_j}^{(i+1)}$ is one-to-one correspondence, the result of Step 3 is in $(s_{j,k-1}, s_{j,k})$ if and only if the value on $R_g$ before Step 3 is in the image of $(s_{j,k-1}, s_{j,k})$ under the map.

3. Implementation of respective gates

We now consider how to implement respective gates in the PRN-on-a-register way to the level of four arithmetic operations.

(i) $V_k^{(j)}$

Note that most parts of $V_k^{(j)}$ consist of only arithmetic operations, addition, subtraction, multiplication, division and comparison, which mentioned in Sec IVA.

For example, the gate $z ← z \oplus (x = j$ and $y \in I)$ can be divided to two parts. The first part is checking that the value on $R_{\text{count}}$ is equal to $j$ and this can be done by the multiple control Toffoli gate, which is studied in [19][48][54]. The second part is checking that the asset price is in a given interval, which can be constructed from two comparisons. Combining these, the gate $z ← z \oplus (x = j$ and $y \in I)$ in Figure 3 is constructed as shown in Figure 4. Note that the bitwise flips $X_{1}^{−n} \otimes \cdots \otimes X_{1}^{−j_{a−1}}$ are operated before the multi control Toffoli. Here, $j_a$ is the $a$-th digit of the binary representation of $j$, so the $a$-th qubit is flipped and if only if $j_a = 0$. This convert $|x⟩$ to $|1⟩...|1⟩$ if and only if $x = j$.

The operation $x ← x + (ax + by)$ in Figure 5 can be realized as follows:

\[
|x⟩|y⟩|0⟩ \rightarrow |x⟩|y⟩|1⟩
\]

\[
|x⟩|y⟩|1 + ay⟩ \rightarrow |(1 + ay)x⟩|y⟩|1 + ay⟩
\]

\[
|(1 + ay)x + by⟩|y⟩|1 + ay⟩ \rightarrow |((1 + ay)x + by)⟩|y⟩|0⟩
\]

where the third ket corresponds to an ancillary register. The first arrow is just setting a constant on a register. The second arrow is the multiplication by a constant $a$. The third arrow is the self-update multiplication, so it needs another ancillary register. The fourth arrow is again multiplication by a constant $b$ and the final arrow is uncomputation of the first and second arrows. Note that this is done under control by $R_g$. In order for this to be controlled, it is sufficient to control only the second, fourth and final arrows, since the third arrow becomes a multiplication by 1 without the second. Also note that multiplication by a $n$-bit constant $a$ or $b$ can be done by $n$ adders, that is, $n$ shift-and-add’s: $ax = \sum_{i=0}^{n-1} a_i 2^i x$, where $a_i$ is the $i$-th bit of $a$. This saves qubits compared with the case where we use a multiplier, which needs holding $a$ on an ancillary register.

The operation $x ← (x - by)/(1 + ay)$ in Figure 6 is done as follows:

\[
|x⟩|y⟩|0⟩|0⟩ \rightarrow |x⟩|y⟩|1⟩|0⟩
\]

\[
|x⟩|y⟩|1 + ay⟩|0⟩ \rightarrow |x - by⟩|y⟩|1 + ay⟩|0⟩
\]

\[
|x - by⟩|y⟩|1 + ay⟩|(x - by)/(1 + ay)⟩
\]

where the first, second, third and fourth kets are $R_S$, $R_W$, another ancillary register and $R_Y$, respectively. Here, the first and second arrows are same as (18), the third is the multiplication by a constant $-b$ and the final one is division. Here, we do not have to uncompute $R_S$ and the ancillary register, since the whole of this operation is uncomputed soon later in $V_{j,k}$.

(ii) $J_W, P_W$

In [17], implementation of PRN on quantum circuits is presented, using the PRN generator called PCG[49]. Note that this PRN generator generates uniform RNs. We now need PSNRNs, so we must transform uniform distribution to standard normal distribution. There are some method and we
adopt the inverse transform sampling. Schematically, \( J_\text{W} \) and \( P_\text{W} \) are implemented as shown in Figure 5. Here, \( J_{\text{PRN}} \) is the gate to let the PRN sequence jump to \( m_i + 1 \) and \( P_{\text{PRN}} \) is the gate to progress the PRN sequence by a step. They sequentially generate uniform RNs on the ancillary register \( R_{\text{PRN}} \) and they are transformed to PSNRN on \( R_\text{W} \).

Although we refer to [17] for the detail of implementation of the PRN generator, we here briefly explain. This generator is combination of linear congruential generator (LCG) and permutation of bit string. For LCG, update of the PRN sequence is done by

\[
x_{n+1} = ax_n + c \mod N,
\]

where \( a, N \) are positive integers and \( c \) is a nonnegative integer, and the initial value \( x_0 \) by

\[
x_n = a^n x_0 + \left( c\left( a^n - 1 \right) / a - 1 \right) \mod N, \quad \text{(21)}
\]

According to (20), we can construct the modular adder using 5 plain adders. Modular multiplication by a \( n \)-bit constant can be done as \( n \) modular shift-and-add’s. Modular division by a constant \( a - 1 \) can be done as modular multiplication by a constant integer \( \beta \) such that \( \beta(a - 1) = 1 \mod N \), if exists. Modular exponentiation \( a^\beta \mod N \) is computed as a sequence controlled modular multiplication. So, to summarize, we can perform (20) and (21) using only controlled adders. In (20), the state is transformed as

\[
|\chi\rangle |0\rangle |0\rangle \rightarrow |\chi\rangle |a x \mod N\rangle |0\rangle
\]

\[
\rightarrow |\chi\rangle |a x \mod N\rangle |c\rangle
\]

\[
\rightarrow |\chi\rangle |a x + c \mod N\rangle |c\rangle
\]

\[
\rightarrow |\chi\rangle |a x + c \mod N\rangle |0\rangle . \quad \text{(22)}
\]

In the circuit we are considering, the first and second registers are \( R_{\text{PRN}} \) and an ancillary register, which interchange their role at every step, and the third is another ancillary register. Each step corresponds to an elementary operation as follows. The first arrow is modular multiplication. The second arrow is the inverse modular multiplication by a constant such that \( a \alpha = 1 \mod N \) and this clearing step is necessary to avoid increase of ancillas. The third is just loading \( c \) on an ancillary register, the fourth is modular addition and the last is unloading. (21) progresses as follows:

\[
|\psi\rangle |0\rangle |0\rangle |0\rangle \rightarrow |\psi\rangle |a^\alpha \mod N\rangle |0\rangle |0\rangle
\]

\[
\rightarrow |\psi\rangle |a^\alpha \mod N\rangle |\left( x_0 + \frac{c}{a - 1} \right) a^\alpha \mod N\rangle |0\rangle
\]

\[
\rightarrow |\psi\rangle |a^\alpha \mod N\rangle |\left( x_0 + \frac{c}{a - 1} \right) a^\alpha - \left( c\left( a^n - 1 \right) / a - 1 \right) \mod N\rangle |\frac{c}{a - 1}\rangle
\]

\[
\rightarrow |\psi\rangle |0\rangle |\left( x_0 + \frac{c}{a - 1} \right) a^\alpha - \left( c\left( a^n - 1 \right) / a - 1 \right) \mod N\rangle |0\rangle , \quad \text{(23)}
\]

where the first, third, second and fourth registers are respectively \( R_{\text{amp}}, R_{\text{PRN}} \) and two ancillary registers. The first arrow is modular exponentiation, the second is modular multiplication, the third is loading, the fourth is modular addition and the last is uncomputation of the first and third.

We do not explain permutation: see (17) for the detail. We just make a comment that it is implemented by a simple circuit, for example, Xorshift is implemented as a sequence of CNOT.

We also need the gate to calculate \( \Phi_{\text{SN}}^{-1} \), the inverse function of CDF of standard normal distribution. There are some ways to calculate this efficiently and we here adopt the method in (50). In the method, \( \mathbb{R} \) is divided into some intervals and \( \Phi_{\text{SN}}^{-1} \) is approximated by a polynomial in each interval. We adopt the setting where the number of intervals is 10^9, and polynomials are cubic, which realizes the error smaller than 10^{-6}.

Here, we write the approximated inverse CDF as

\[
\Phi_{\text{SN}}^{-1}(x) \approx c_m 3x^3 + c_m 2x^2 + c_m 1x + c_m 0 \quad \text{(24)}
\]

for \( x_{\text{ICDF}}^{m-1} \leq x < x_{\text{ICDF}}^{m} \), \( m = 0, 1, ..., n_{\text{ICDF}} + 1 \), where \( x_{\text{ICDF}}^{m} < x_{\text{ICDF}}^{m+1} < ... < x_{\text{ICDF}}^{n_{\text{ICDF}}} \) are the end points of the intervals and \( n_{\text{ICDF}} \) is the number of the interval. Consider that \( x_{\text{ICDF}}^{-1} = +\infty \), \( x_{\text{ICDF}}^{n_{\text{ICDF}}+1} = -\infty \).

Such a piecewise cubic function can be implemented as shown in Figure 6. We here explain how it works. First, the sequence of comparators and “Load \( c_{m}\)'s” gates load \( c_{m}, c_{m}, ..., c_{m} \) into the register \( R_{g_{1}}, ..., R_{g_{3}} \) respectively as follows. The comparators compare the value of \( R_{\text{PRN}} \) and the grid points \( x_{\text{ICDF}}^{m} \) and flip \( R_{g} \) if \( x < x_{\text{ICDF}}^{m} \). If \( R_{g} \) is 1, the “Load \( c_{m}\)'s” gates are activated. They are actually collections of bitwise flips, that is, \( X \) gates. If \( x \geq x_{\text{ICDF}}^{-1} \), only “Load \( c_{m}\)'s” gate is performed and it loads \( c_{n_{\text{ICDF}}+1} = 1 \) and \( c_{n_{\text{ICDF}}+1} = 1 \). If \( x_{\text{ICDF}}^{-1} \leq x < x_{\text{ICDF}}^{1} \), “Load \( c_{m}\)'s” and “Load \( c_{m}\)'s” are performed. So, we set “Load \( c_{m}\)'s” so that it compensates flips done by “Load \( c_{n_{\text{ICDF}}+1}\)'s” and \( c_{n_{\text{ICDF}}+1} \) and \( c_{n_{\text{ICDF}}+1} \) are successfully loaded. The case where \( x \) is in another interval is similar. The point is that if \( x_{\text{ICDF}}^{m-1} \leq x < x_{\text{ICDF}}^{m} \), every other gates are activated. That is, the activated gates are “Load \( c_{m}\)'s” of \( m = M, M + 2, ..., n_{\text{ICDF}}, n_{\text{ICDF}} + 1 \) if \( n_{\text{ICDF}} - M \) is even and \( m = M, M + 2, ..., n_{\text{ICDF}} - 1, n_{\text{ICDF}} + 1 \) if \( n_{\text{ICDF}} - M \) is odd. This is because every comparator after the \( M \)-th one flips \( R_{g} \) and \( R_{g} \) takes 0 and 1 alternatingly. Considering this, the \( X \) gates in “Load \( c_{m}\)'s” are set as shown in Figure 7 so that \( c_{m}, c_{m}, ..., c_{m} \) for appropriate \( m \) are loaded after the sequence of all activated gates.

After load of coefficients, the cubic function is calculated in the Horner’s method

\[
\left( c_{m} x + c_{m} x + c_{m} x + c_{m} x + c_{m} x + c_{m} \right) \quad \text{(25)}
\]

This is done by the sequence of adders and multipliers in the latter half of the circuit in Figure 6.

(ii) Payoff

In this paper, we do not consider gates to calculate payoffs in detail, since the resource the gates require is same in both

6 if we include \( (-\infty, x_{0}^{\text{ICDF}}] \) and \( [x_{0}^{\text{ICDF}}, +\infty) \), it is 111
the PRN-on-a-register way and the register-per-RN way. We here make just a short comment. In many cases, a payoff can be expressed in the following form:

\[ f_i^{\text{pay}} = \min \{ \max \{ a_i S_t + b_i, f_i \}, c_i \}, \]  

(26)

where \( a_i, b_i, c_i, f_i \) are real constants, that is, a linear function of the asset price with the upper bound (cap) \( c_i \) and the lower bound (floor) \( f_i \). For example, a payoff in an European call option \( f \) corresponds to \( a_i = 1, b_i = -K, c_i = +\infty, f_i = 0 \). Payoffs expressed as (26) can be calculated easily by combination of comparators, adders and multipliers.

C. the register-per-RN way

1. calculation flow

Also for the register-per-RN way, we start from presenting the calculation flow, which is somewhat simpler than the PRN-on-a-register way. Again, we consider the flow until calculation of the payoff sum.

Before we present the calculation flow, we explain the required registers.

- \( R_w, i = 1, ..., n_t \)
  
  This is a register for the \( i \)-th SNRN. We need such a register per random number, so the total number is \( n_t \).

- \( R_s, i = 0, 1, ..., n_t \)
  
  This is a register where the value of the asset price at time \( t_i \) is held.

- \( R_{\text{payoff}}, i = 1, ..., n_t \)
  
  This is a register where the value of the sum of payoffs by \( t_i \) is held.

We again omit ancillary registers here and explain them later. Besides, we again assume that these and ancillary registers necessary to update them have \( n_{\text{dig}} \) qubits.

We here concretely define a superposition of SNRN values as the following state. In advance, we set the equally spaced \( N_{\text{SN}} + 1 \) points for discretization of the distribution \( x_{\text{SN},0} < x_{\text{SN},1} < ... < x_{\text{SN},N_{\text{SN}}} \), where \( x_{\text{SN},0} \) and \( x_{\text{SN},N_{\text{SN}}} \) are the upper and lower bounds of the distribution and set to, say, -4 and +4, respectively. We here assume \( N_{\text{SN}} = 2^{n_{\text{SN}}} \) for simplicity. Then, we define \( |SN\) as

\[ |SN\rangle = \sum_{i=0}^{N_{\text{SN}}-1} \sqrt{p_{\text{SN},i}} |i\rangle, \]  

(27)

where \( p_{\text{SN},i} = \int_{x_{\text{SN},i}}^{x_{\text{SN},i+1}} \phi_{\text{SN}}(x) dx \) and \( \phi_{\text{SN}}(x) \) is the probability density function of the standard normal distribution. We consider how to create such a state later. Since \( x_{\text{SN},i} \) can be easily calculated from the index \( i \) by a linear function, we identify \( i \) as \( x_{\text{SN},i} \).

Then, the calculation flow is as follows:

1. Initialize all registers to \( |0\rangle \) except \( R_{\text{SN}_0} \), which is initialized to \( |S_{t_0}\rangle \).

2. Generate superpositions of SNRNs on \( R_w, ..., R_{w_n} \).
   
   That is, set each of them to \( |SN\rangle \).

3. Perform the time evolution (10) using the value on \( R_{w_1} \) as \( w_1 \). The result is output to \( R_{s_1} \), as \( |S_{t_1}\rangle \).

4. Calculate the payoff at time \( t_1 \) using \( R_{s_1} \) and output the sum of it and the previous payoffs to \( R_{\text{payoff},1} \).

5. Iterate operations similar to 3-4 for each time step until the time reaches \( t_n \).

6. Finally we obtain a superposition of states in which the value on \( R_{\text{payoff},n} \) is the sum of payoffs for each pattern of values of SNRNs. Estimate the expectation value of \( R_{\text{payoff},n} \) to get (11).

The flow of state transformation is as follows. Writing only \( R_{w_1}, ..., R_{w_n}, R_{s_1}, ..., R_{s_n} \) and \( R_{\text{payoff},1}, ..., R_{\text{payoff},n} \),

\[
|0\rangle^{n_{\text{SN}}} |S_{t_0}\rangle |0\rangle^{n_{\text{SN}}} |0\rangle^{n_{\text{SN}}}
\]

\[
\rightarrow |SN\rangle^{n_{\text{SN}}} |S_{t_0}\rangle |0\rangle^{n_{\text{SN}}} |0\rangle^{n_{\text{SN}}}
\]

\[
\rightarrow \sum_{i=0}^{N_{\text{SN}}-1} \sqrt{p_{\text{SN},i}} |i\rangle |SN\rangle^{n_{\text{SN}}-1} |S_{t_0}\rangle |S_{t_1}(i)\rangle |0\rangle^{n_{\text{SN}}-1} |0\rangle^{n_{\text{SN}}}
\]

\[
\rightarrow \sum_{i=0}^{N_{\text{SN}}-1} \sqrt{p_{\text{SN},i}} |i\rangle |SN\rangle^{n_{\text{SN}}-1} |S_{t_0}\rangle |S_{t_1}(i)\rangle |0\rangle^{n_{\text{SN}}-1} |f_{t_1}^{\text{pay}}(S_{t_1}(i))\rangle |0\rangle^{n_{\text{SN}}-1}
\]

\[
\rightarrow \sum_{i=0}^{N_{\text{SN}}-1} \sqrt{p_{\text{SN},i}} |i\rangle \cdots |i_{n_{\text{SN}}}\rangle |S_{t_0}\rangle |S_{t_1}(i)\rangle \cdots |S_{t_{n_{\text{SN}}}}(i)\rangle |f_{t_1}^{\text{pay}}(S_{t_1}(i))\rangle \cdots |f_{t_{n_{\text{SN}}}^{\text{pay}}}(S_{t_{n_{\text{SN}}}(i), \cdots (i-1)}),
\]  

(28)
where \( S^{(g_{ij})} \) is the value of the asset price at time \( t_j \) evolved by \( w_1 = x_{SN,j}, \ldots, w_j = x_{SN,j} \).

2. Overview of the circuit

The outline of the circuit in the register-per-RN is as shown in Figure 8. First, \( SN \) is created on each \( R_W \) by the gate \( SN \), which is considered in detail later. After that, the gate \( U_j \) performs \( j \)-th step of asset price evolution and payoff calculation. For each evolution step, ancillary registers \( R_{R_j} \) and \( R_{LV,j} \), which have 1 and 2\( n_{dig} \) qubits respectively, are necessary. \( U_j \) is then implemented as Figure 9. In this gate, the sequence of comparators and “Load” gates set \( a_{jk}, b_{jk} \) in (8) into \( R_{LV,j} \) by the trick similar to that in the circuit in Figure 6. Then, the operation \( x \rightarrow x + (ax + by) \) updates the asset price according to (10). Since the register-per-RN way does not aim to uncompute ancillary qubits in order to reduce them, \( x \rightarrow x + (ax + by) \) can be done as follows:

\[
|x⟩ ⟨y| ⟨a| ⟨b| ⟨0| ⟨0| \rightarrow |x⟩ ⟨y| ⟨a| ⟨b| ⟨xy| ⟨x⟩ \\
\rightarrow |x⟩ ⟨y| ⟨a⟩ ⟨b| ⟨xy⟩ ⟨x⟩ \\
\rightarrow |x⟩ ⟨y| ⟨a⟩ ⟨b| ⟨xy⟩ ⟨x + axy⟩ \\
\rightarrow |x⟩ ⟨y| ⟨a⟩ ⟨b| ⟨xy⟩ ⟨x + axy + by⟩,
\]

where the first ket is \( R_{S_j} \), the second is \( R_{W_j} \), the third and fourth are \( R_{LV,j} \), the fifth is an ancillary register and the last is \( R_{S_j} \). So, this operation consists of copying a state and three multiplications. At the end of \( U_j \), the payoff is calculated using \( R_{S_j} \). Here, the “Payoff” gate performs the following operation

\[
|S^{(g_{ij})}\rangle \sum_{k=1}^{j} \delta_k^{pay}(S^{(g_{ij})}) |0\rangle \\
\rightarrow |S^{(g_{ij})}\rangle \sum_{k=1}^{j} \delta_k^{pay}(S^{(g_{ij})}) |\sum_{k=1}^{j} \delta_k^{pay}(S^{(g_{ij})})\rangle,
\]

where the first, second and third ket are \( R_{S_j} \), \( R_{payoff,j-1} \) and \( R_{payoff,j} \). This is done as copying \( R_{payoff,j-1} \) to \( R_{payoff,j} \) by calculation and addition of \( \delta_k^{pay}(S^{(g_{ij})}) \) to \( R_{payoff,j} \).

3. Implementation of the SN gate

Let us now consider implementation of the SN gate, which creates a superposition of SNR values. The outline was presented in 13. In addition to this, we here explain some details, which were not explicitly explained in 13.

We construct the state in the recursive way. We assume that we have already divided \( x_{SN,0} \) by equally-spaced \( 2^m + 1 \) points \( x_{SN,0} < x_{SN,1} < \ldots < x_{SN,2^m} = x_{SN,m} \) and created

\[
|SN_m\rangle = \sum_{i=0}^{2^m-1} \sqrt{p^{(m)}_{SN,i}} |i\rangle,
\]

where \( p^{(m)}_{SN,i} = \int_{x_{SN,i}}^{x_{SN,i+1}} \phi_{SN}(x)dx \). We also assume that we have a gate to efficiently compute \( \theta^{(m)}_i = \arccos \sqrt{f^{(m)}_i} \) with the input \( i \), where \( f^{(m)}_i \) is

\[
f^{(m)}_i = \frac{\int_{x_{SN,i}}^{x_{SN,i+1}} \phi_{SN}(x)dx}{\int_{x_{SN,m}}^{x_{SN,m+1}} \phi_{SN}(x)dx}.
\]

Then, the following state transformation is possible:

\[
|SN_m\rangle |0\rangle = \sum_{i=0}^{2^m-1} \sqrt{p^{(m)}_{SN,i}} |i\rangle |0\rangle \\
\rightarrow \sum_{i=0}^{2^m-1} \sqrt{p^{(m)}_{SN,i}} |i\rangle |\theta^{(m)}_i\rangle \\
\rightarrow \sum_{i=0}^{2^m-1} \sqrt{\int_{x_{SN,i}}^{x_{SN,i+1}} |\cos \theta^{(m)}_i| 1 + \sin \theta^{(m)}_i 1\rangle |\theta^{(m)}_i\rangle \\
= \sum_{i=0}^{2^m-1} \sqrt{\int_{x_{SN,i}}^{x_{SN,i+1}} |\theta^{(m)}_i\rangle \\
= |SN_{m+1}\rangle |0\rangle,
\]

where we use the gate to compute \( \theta^{(m)}_i \) at the first arrow and perform the controlled rotation at the second arrow. Repeating this until \( m = n_{dig} - 1 \), we get \( SN \).

However, as far as the authors know, neither 13 nor other papers present the gate to compute \( \theta^{(m)}_i \). Here, we propose a way to do this on the basis of a simple Taylor expansion.

Consider

\[
g(x, \delta) = \frac{1}{2} + \frac{1}{8} \delta x + \frac{1}{16} \delta^2 + O(\delta^3)
\]

by simple calculation. So, \( g(x, \delta) \) is well-approximated by a linear function of \( x \) for small \( \delta \). We can use this to compute \( f^{(m)}_i \), since

\[
f^{(m)}_i = g \left( \frac{x^{(m)}_{SN,i} - \Delta}{2m} \right) \Delta = x_{SN,N_{SN}} - x_{SN,0}.
\]

Given \( x_{SN,N_{SN}}, x_{SN,0} \) and \( m \) large enough that \( \Delta/2m \) is sufficiently small, this can be approximately seen as a linear function of \( i \), since \( x^{(m)}_{SN,i} = x_{SN,0} + \frac{\Delta}{2m} i \). Actually, we numerically confirmed that for \( m \geq 7 \) the above approximation gives error smaller than \( 10^{-5} \).

We then reach the circuit in Figure 10 for calculation of \( f^{(m)}_i \). For \( m \leq 6 \), as shown in Figure 10a, the sequence of comparators and “Load” gates set \( f^{(m)}_i \) to the output register \( R_{gen} \), using the trick similar to the circuit in Figure 6 again. Note
that comparators now check whether the input value \( i \) is equal to a given integer constant or not, so each of them is actually a combination of bitwise flips and a multi-controlled Toffoli gate, similar to that appeared in Figure 4. Also note that, if the input \( i \) is 1, “Load \( f^{(m)} \)” gates are activated for \( i \geq 1 \). Considering this point, each “Load” gate is set so that operations of it and the following gates are successfully compensated. For \( m \geq 7 \), the \( f^{(m)} \) is just a linear transformation, which is implemented as bitwise flips followed by a constant multiplier. Of course, according to required accuracy, the value of \( m \) where the two types of \( f^{(m)} \) are switched should be adjusted and the degree of the Taylor approximation for \( g(x, \delta) \) should be increased.

Using this \( f^{(m)} \) gate, the SN gate is constructed as Figure 11. First, we operate a Hadamard gate to the most significant bit in \( R_W \), to assign probability 1/2 to positive and negative halves of \( \{3\text{SNO}, 3\text{SN1}, 3\text{SN} \} \) respectively. Then, we operate the sequence of the gates \( U_m \) which corresponds to the \( m \)-th step of the above recursive calculation. \( U_m \) is constructed as a combination of the \( f^{(m)} \) gate, the gates to calculate square root and arc cosine and the controlled rotation gate \( R(\theta) \).

We here comment on implementation of arccos and square root. The implementation of the inverse trigonometric function based on the piecewise polynomial approximation is proposed in [51]. Although [51] considers not arccos but arccsin, these can be easily related as \( \arccos(x) = \frac{\pi}{2} - \arcsin(x) \). We adopt a setting with the polynomial degree 3 and 2 intervals, which leads to accuracy \( 10^{-5} [51] \). The circuit for square root is given in [52].

V. ESTIMATION OF REQUIRED RESOURCES

Then, let us estimate the machine resources required for the implementation in the PRN-on-a-register way and the register-RN way. We consider the two metrics, qubit number and T-count, as many papers do.

A. elementary gates

We first summarize the resources of the elementary gates which are necessary to construct the LV circuit. We here consider fixed-point arithmetic. Among various implementations proposed previously, we adopt one for each of the elementary gates and summarize their resources when operands are \( n \)-bit in Table I. Since we aim to estimate the orders of the above metrics, we take only the leading term with respect to \( n \) for required resources. For example, we approximate \( an + b \) as \( an \).

We make a comment on multiplication and the division. For these operation, we use modified versions of circuits proposed in [42] and [46]. This is because of the following reason. In order to store the strict value of the product of two \( n \)-bit numbers, original circuits use \( 2n \)-bits. This causes a problem in the situation where we have to sequentially perform multiplication as in the LV circuit, since the required qubit number doubles at every multiplication. Therefore, we have to truncate lower bits of product and keep the digit number constant. In order to do this, we modify the multiplier in [42]. We also construct the divider, which is dedicated to drawback of the modified multiplication. This is why the qubit number for divider in Table I is different from that in [42] [46]. We explain the details of the modified multiplier and divider in Appendix.

B. assumptions on registers

We assume the following points on qubit numbers of various registers, some of which have already been mentioned.

- Registers which store numerical numbers, \( R_W, R_S, R_{\text{payoff}}, R_{LV,j} \) etc., and ancillary registers concerning them have \( n_{\text{dig}} \) qubits. This is determined according to the required accuracy. We hereafter set \( n_{\text{dig}} = 16 \).
- \( R_{PRN} \) in Figure 5 exceptionally has \( n_{PRN} \) qubits, since this is set to so large a value that the PRN sequence has good statistical property, e.g. long period. [49] considers the PRN generators with 64 bits and we also use this value for \( n_{PRN} \) hereafter. Ancillary registers necessary for calculation of PRN sequence have \( n_{PRN} \) qubits too. Even if \( n_{PRN} > n_{\text{dig}} \), we use only \( n_{\text{dig}} \) qubits in \( R_{PRN} \) for transformation to PSNRN.
- \( R_{\text{amp}} \) has \( n_{\text{amp}} \) qubits.
- Other registers, e.g. \( R_{\text{ const}} \), have only several qubits and we neglect their contributions to the whole qubit number.

C. the PRN-on-a-register way

Then, let us consider the required resources in the PRN-on-a-register way.

1. qubit number

In Table II we summarize qubits necessary in each step in the circuit. Registers which hold some values throughout the circuit are as follows: \( R_{\text{amp}}, R_{S}, R_{\text{payoff}} \) and \( R_{PRN} \). Except these, the following parts in the circuit can consume qubit number most heavily.

- \( J_{PRN} \) and \( P_{PRN} \): \( 2n_{PRN} \) qubits
- \( \Phi_{SN}^{-1} \): \( 7n_{\text{dig}} \) qubits

Therefore, the total qubit number required in the PRN-on-a-register way is roughly

\[
n_{\text{amp}} + 2n_{\text{dig}} + n_{PRN} + \max(2n_{PRN}, 7n_{\text{dig}}) \tag{37}
\]

Let us comment on some technical points for obtaining Table II. We first make a supplementary explanation on the ancillary qubit number in \( V_k^{(j)} \). There are two parts which require...
Table I: Resources for various elementary gates. We here assume that operands are \( n \)-bit. We omit subleading terms with respect to \( n \).

| Gate              | Total | Qubits | Operand | Output | Ancilla | T-count | Reference |
|-------------------|-------|--------|---------|--------|---------|---------|-----------|
| Adder             | \( 2n \) | \( 2n \) | 0 (self-update) | 0 | 14\( n \) | \[27\][38][46] |
| Ctrl Adder        | \( 2n \) | \( 2n \) | 0 (self-update) | 0 | 21\( n \) | \[42\] |
| Modular Adder     | \( 2n \) | \( 2n \) | 0 (self-update) | 0 | 70\( n \) | \[26\][37][38][56] |
| Multiplier        | \( 3n \) | \( 2n \) | \( n \) | 0 | 21\( n \) | \[42\] |
| Diviser           | \( 5n \) | \( 2n \) | \( n \) | 2\( n \) | 35\( n \) | \[46\] |
| Multi Ctrl Toffoli| \( 2n \) | \( n \) | 1 | \( n \) | 8\( n \) | \[19\][46] |
| Square Root\( ^* \)| \( 4n \) | \( n \) | \( n \) | 2\( n \) | 14\( n \) | \[52\] |
| arccos            | 105   |        |        |        |         | 3.4 \times 10^{11} | \[51\] |

controlled rotation \( 2 \) (control and target) \( n \) \[22\][53][54] \( (\text{with accuracy of } 2^{-n}) \)

\( ^* \) Since we can construct the modular adder using 5 plain adders\[26\], we use 5 times the values of the adder for T-count.

\( ^b \) The circuit given in \[52\] takes a \( n \)-bit input and returns the \( n/2 \)-bit square root and the \( n/2 \)-bit remainder. In order to keep \( n \)-bit accuracy, we add \( n \) 0’s to the input and calculate the \( n \)-bit square root of the virtual \( 2n \)-bit input. We treat the \( n \) bits added to the input and the \( n \) bits where the remainder is output as ancillas.

\( ^c \) Since the value shown in \[51\] is Toffoli count, we simply multiply it by 7 for converting it to T-count.

Table II: Qubits necessary in each step in the PRN-on-a-register circuit. We neglect registers with only several qubits.

| Part                | Qubit | Note |
|---------------------|-------|------|
| Whole               |       |      |
| \( R_{\text{amp}} \) | \( n_{\text{amp}} \) |      |
| \( R_S \)           | \( n_{\text{dig}} \) |      |
| \( R_{\text{payoff}} \) | \( n_{\text{dig}} \) |      |
| \( R_{\text{PRN}} \) | \( n_{\text{PRN}} \) |      |
| \( J_{\text{PRN}} \) | ancilla | \( 2 n_{\text{PRN}} \) | To hold intermediate outputs; see \( 21 \) |
| \( \Phi^{-1}_{\text{SN}} \) | \( R_W \) | \( n_{\text{dig}} \) | \( 6 n_{\text{dig}} \) | To hold the coefficients of the polynomial and the intermediate outputs; see Figure \( 6 \) |
| \( V_{k}^{(j)} \)   | \( R_{W} \) | \( n_{\text{dig}} \) | \( 4 n_{\text{dig}} \) | For \( x \leftarrow x + (ax + b)y \) and \( z \leftarrow \frac{x + ay}{1 + ay} \); see the comment in the body text. |
| \( P_{\text{PRN}} \) | ancilla | \( 2 n_{\text{PRN}} \) | To hold intermediate outputs; see \( 22 \). |

ancillas in \( V_k^{(j)} \). First, \( x \leftarrow x + (ax + b)y \) needs the following ancillas: a \( n_{\text{dig}} \)-bit register to which 1 + \( ay \) is output, a \( n_{\text{dig}} \)-bit register to which the result is temporally output in the self-update multiplication and a \( 2 n_{\text{dig}} \)-bit register necessary for the inverse division to clear the input \( x \). Second, \( z \leftarrow \frac{x + ay}{1 + ay} \) needs the following: a \( n_{\text{dig}} \)-bit register to which 1 + \( ay \) is output and a \( 2 n_{\text{dig}} \)-bit register necessary for division. In total, \( 4 n_{\text{dig}} \) bits are sufficient.

We also comment on the ancilla number in \( \Phi^{-1}_{\text{SN}} \). As we can see from Figure \( 6 \), we need four registers to which coefficients are loaded and two registers for intermediate outputs. Therefore, \( 6 n_{\text{dig}} \) ancillas are necessary.

2. T-count

Since we are interested in only the leading contribution, we focus on multiplications, divisions and repeated additions. Besides, we do not consider the T-count of \( J_W \), which is used only once. For the parts in \( U_j \), which is used repeatedly, we specify T-counts as follows:

1. \( V_k^{(j)} \)

One \( V_k^{(j)} \) includes the following parts:

- \( x \leftarrow x + (ax + b)y \)

As we can see in \( 18 \), this includes one multiplication and one division, which come from one
self-update multiplication, and \(3n_{\text{dig}}\) controlled additions, which come from two controlled multiplications by constant and one inverse. In total, the T-count is \(119n_{\text{dig}}^2\).

- \(z \leftarrow \frac{z + x \cdot y}{1 + ay}\)  
  As we can see in \([19]\), this includes one division and \(2n_{\text{dig}}\) additions, which comes from two multiplications by constant. In total, the T-count is \(63n_{\text{dig}}^2\).
- Uncomputation of \(z \leftarrow \frac{z + x \cdot y}{1 + ay}\).  
  Similar to the above.

Therefore, the total T-count in one \(V^{(j)}_k\) is \(245n_{\text{dig}}^2\). Since \(V^{(j)}_k\) is used \(n_S + 1\) times, the total T-count in them is \(245n_{\text{dig}}^2n_S\) (only the leading term).

2. \(P_{\text{PRN}}\)

This includes two modular multiplications by constant, which coming from one self-update modular multiplication. These are decomposed into \(2n_{\text{PRN}}\) modular additions. So the T-count is roughly \(140n_{\text{PRN}}^2\).

3. \(\Phi^{-1}_{\text{SN}}\) and its inverse  
   Each of them includes \(2(n_{\text{ICDF}} + 1)\) additions (\(n_{\text{ICDF}} + 1\) comparisons) and five multiplications. So the T-count for each is roughly \(105n_{\text{dig}}^2 + 28n_{\text{dig}}n_{\text{ICDF}}\).

Summing up these and considering \(U_j\) is used in \(n_t\) times, the T-count in the whole circuit is roughly:

\[
(245n_{\text{dig}}^2n_S + 140n_{\text{PRN}}^2 + 210n_{\text{dig}}^2 + 56n_{\text{dig}}n_{\text{ICDF}})n_t. \tag{38}
\]

D. the register-per-RN way

Next, we consider the required resources in the register-per-RN way.

1. qubit number

In the register-per-RN way, registers shown in Table III are added per time step. Note that we do not uncompute ancillas. Summing up all registers, the qubit number necessary for one time step is roughly \(3n_{\text{dig}}^2 + 111n_{\text{dig}}\), and for the entire circuit it is \(3n_{\text{dig}}^2 + 111n_{\text{dig}}n_t\). \tag{39}

Note that the dominant part comes from the iterative calculation in the SN gates, which prepare superpositions of the values of the SNRNs.

2. T-count

Again, we focus on operations with large T-count. For each part in the circuit, we estimate the T-count as follows:

1. SN gate

The \(m\)-th iteration \(U_{\text{SN}}^m\) in the SN gate includes the following parts:

- square root, arccos, controlled rotation  
  T-counts are \(14n_{\text{dig}}\), \(3.4 \times 10^4\) and \(3n_{\text{dig}}\), respectively.
- \(f_j^{(m)}\)  
  For \(2 \leq m \leq 6\), we use \(2^m\) \(m\)-controlled Toffoli gates to check the value on \(R_{U_i}\) and load \(f_j^{(m)}\) which corresponds to the value. T-count for this is \(2^m(8m - 9)\). Summing this for \(m = 2, \ldots, 6\) leads to about 4000. Since this is much smaller than T-count for arccos in one iteration, we neglect this. For \(m \geq 7\), we do multiplication between a \(m\)-bit variable and a \(n_{\text{dig}}\)-bit constant, which is decomposed \(n_{\text{dig}}\) additions of \(m\)-bit. Then, T-count is \(14mn_{\text{dig}}\).

Summing up these and taking only dominant contributions, one SN gate has T-count of \((7n_{\text{dig}}^2 + 3.4 \times 10^4)n_{\text{dig}}\) roughly.

2. \(U_j\)

This includes \(2n_S\) additions (\(n_S\) comparisons) and three multiplications. So one \(U_j\) gates has T-count of \(63n_{\text{dig}}^2 + 28n_Sn_{\text{dig}}\) roughly.

In total, we can estimate T-count of the entire circuit in the register-per-RN way as:

\[
(7n_{\text{dig}}^2 + 63n_{\text{dig}} + 28n_S + 3.4 \times 10^4)n_{\text{dig}}n_t. \tag{40}
\]

E. comparison between two ways

We then compare resources necessary in two ways in Table IV. Naturally, qubit number is independent from \(n_t\) in the PRN-on-a-register way but proportional to \(n_t\) in the register-per-RN way and T-count is proportional to \(n_t\) in both ways. If we take a setting, which is typically necessary for practical use in derivative pricing\(^9\):

\[
\begin{align*}
n_{\text{samp}} &= 16, \\
n_{\text{dig}} &= 16, \\
n_{\text{PRN}} &= 64, \\
n_{\text{ICDF}} &= 109, \\
n_t &= 360, \\
n_S &= 5
\end{align*}
\tag{41}
\]

the values in Table IV becomes as Table V. The total T-count is of same order of magnitude in the both way but larger for

\(^9\) Here, we use \(8m - 9\), the accurate value of T-count of the \(m\)-controlled Toffoli gates\(^9\), since the approximation as \(8m\) is too crude for small \(m\).  
\(^{10}\) \(n_{\text{samp}} = 16\) corresponds to 65536 sample paths.
the PRN-on-a-register way by a factor 2 roughly. We here comment on the parts which consume T-count most heavily in each way. In the PRN-on-a-register way, there are two parts which contribute to T-count equally and dominantly. The first is the update of the asset price in $V^k(t)$. Note that additional operations for reduction of qubits, such as inverse division in self-update multiplication and drawing back the asset price to clear $R_t$, increase T-count compared with the register-per-RN way. The second is modular multiplications in update of the PRN sequence. Since the PRN generator requires the large bit number, say $n_{PRN} = 64$, in order to it keep good statistical properties such as long period, the T-count of operations for the PRN becomes large. On the other hand, in the register-per-RN way the dominant contribution to T-count comes from arccos’s in preparing SNRNs. Because not only an arccos itself is T-count consuming but also it is used in each iteration in the SN gate, the total T-count piles up.

### VI. SUMMARY

In this paper, we considered how to implement time evolution of the asset price in the LV model on quantum computers. Similar to other problems in finance, derivative pricing by Monte Carlo simulation requires a large number of random numbers, which is proportional to $n_t$, the number of time steps for asset price evolution, and this may cause difficulty in implementation. We then considered two ways of implementation: the PRN-on-a-register way and the register-per-RN way. In the former we sequentially generate pseudo random numbers on a register and use them to evolve the asset price. In the latter, standard normal random numbers necessary to time evolution are created as superpositions on separate registers. For both ways, we present the concrete quantum circuits in detail. For not only random number generation but also other aspects, we try to save qubit numbers permitting some additional procedures in the PRN-on-a-register way and do opposite in the register-per-RN way. We then give estimations of qubit number and T-count required in each way. In the PRN-on-a-register way, qubit number is kept constant against $n_t$. On the other hand, in the register-per-RN way qubit number is proportional to $n_t$. Each way has T-count consuming parts and the total T-counts for both ways are of same order of magnitude, expect the PRN-on-a-register way has the larger T-count by a factor about 2, in some specific setting.

Note that analyses of resources required for implementation of the LV model in this paper strongly depend on designs of elementary circuits for arithmetic. For example, in the register-per-RN way the dominant contribution to T-count comes from arccos’s in preparing SNRNs. If more efficient circuits are proposed and we replace the current choice with them, required resources may change.

Finally, we would like to notice that this study is not enough for application of quantum algorithm for Monte Carlo simulation to pricing in the LV model. Although we assumed that the LV function is given, in practice we have to calibrate the LV so that the model prices of European options fit to the market prices. Besides, we have not considered how to evaluate terms in exotic derivatives, for example, early exercise. In future works, we will consider such things and aim to present how to apply quantum computers in the whole process of exotic derivative pricing.

### Appendix A: Sufficient condition on $\sigma(t, S)$ in the PRN-on-a-register way

We here show that $\sigma(t, S)$ which is continuous with respect to $S$ and takes the form of (8) and sufficiently small $\Delta t_j$ lead to one-to-one correspondence between $S_{t_j}^{(i)}$ and $S_{t_{j+1}}^{(i)}$. We see
\( S^{(i)}_{j_{i+1}} \) as a function of \( S^{(i)}_j \) and define a function \( f \) by

\[
f(S) = S + \sigma(t_j, S) \sqrt{\Delta t_j w_j}
\]

for fixed \( w_j \) so that \( S^{(i)}_{j_{i+1}} = f(S^{(i)}_j) \) holds. Except for the grid points \( S = s_{j0} \ldots s_{jK} \), \( f(S) \) is differentiable and

\[
f'(S) = 1 + a_{jk} \sqrt{\Delta t_j w_j}; \quad \text{for } s_{j_{k-1}} < S < s_{jk}, k = 0, \ldots, n_S + 1.
\]

Since \( w_j \) is bounded in numerical computation, \( f'(S) \) is always positive expect the grid points for sufficiently small \( \Delta t_j \). Besides, if \( \sigma(t_j, S) \) is continuous with respect to \( S \) also at the grid points, so is \( f(S) \). Combining these, we find that \( f(S) \) is strictly increasing for small \( \Delta t_j \). Thus, the correspondence between \( S^{(i)}_j \) and \( S^{(i)}_{j_{i+1}} \) is one-to-one.

Small \( \Delta t_j \) is required from another perspective, too. The original dynamics of the asset price is given as the continuous-time evolution (3) and (10) is the discretized approximation of it. Therefore, in order for this approximation to be accurate, the increment of asset price should be sufficiently smaller than the asset price itself:

\[
|\sigma(t_j, S^{(i)}_{j_{i+1}}) \sqrt{\Delta t_j w_j}| \ll |S^{(i)}_{j_{i+1}}|\quad \text{if this condition is satisfied, } |a_{jk} \sqrt{\Delta t_j w_j}| \ll 1, \quad \text{so } f'(S) > 0 \text{ is met.}
\]

**Appendix B: Truncated multiplier and divider**

We here describe the modified version of multiplier and divider. We assume that we consider the fixed-point arithmetic with \( n_{\text{int}} \) bits in the integer part and \( n_{\text{frac}} \) bits in the fractional part, \( n = n_{\text{int}} + n_{\text{frac}} \) bits in total. We hereafter call such numbers \((n_{\text{int}}, n_{\text{frac}})\)-bit numbers. We want to keep this digit setting before and after multiplication. In order to do this, we adopt the following policy.

- We simply truncate the digits lower than the \( n_{\text{frac}} \)-th fractional digit in the product. This might cause numerical errors around and the \( n_{\text{frac}} \)-th fractional digit and such a tiny error might accumulate, but we simply neglect this concern.

- We assume the overflow from the \( n_{\text{int}} \)-bit integer part never occurs.

We then approximate the product as follows. Writing a number \( x \) in binary representation as \( x_{n_{\text{int}}-1}x_{n_{\text{int}}-2} \ldots x_0x_{-1} \ldots x_{-n_{\text{frac}}} \), where \( x_i \) is the \( i \)-th integer digit of \( x \) and \( x_{-j} \) is the \( j \)-th fractional digit of \( x \), we do

\[
xy = \sum_{i=-n_{\text{frac}}}^{n_{\text{int}}-1} x_i 2^i y \approx f^{\text{mul}}_{n_{\text{int}}, n_{\text{frac}}}(x) := \sum_{i=-n_{\text{frac}}}^{n_{\text{int}}-1} x_i 2^i \tilde{y}_i,
\]

where

\[
\tilde{y}_i = \begin{cases} y_{n_{\text{int}}-1} \ldots y_0 y_{-1} \ldots y_{-(n_{\text{frac}}-i)} & \text{for } i < 0 \\ y & \text{for } i \geq 0 \end{cases}
\]

This truncated multiplication is implemented as a circuit in Figure 12. Note that the circuit in Figure 12 actually calculates not \( f^{\text{mul}}_{n_{\text{int}}, n_{\text{frac}}}(x) \) but

\[
\sum_{i=0}^{n_{\text{int}}-1} x_i 2^i (y_{n_{\text{int}}-1-i} \ldots y_0 y_{-1} \ldots y_{-(n_{\text{frac}}-i)}) \].
\]

This is equal to \( f^{\text{mul}}_{n_{\text{int}}, n_{\text{frac}}}(x) \) if our assumption that the overflow from the \( n \)-bit integer part never occurs is satisfied.

We define the truncated division as the inverse of the truncated multiplication: \( z/y \approx f^{\text{div}}_{n_{\text{int}}, n_{\text{frac}}}(z) := \left(f^{\text{mul}}_{n_{\text{int}}, n_{\text{frac}}}ight)^{-1}(z) \). Given two \((n_{\text{int}}, n_{\text{frac}})\)-bit numbers \( y, z \) which satisfies \( z = f^{\text{mul}}_{n_{\text{int}}, n_{\text{frac}}}(x) \), we can find the \((n_{\text{int}}, n_{\text{frac}})\)-bit number \( x \) as follows:

1. Set \( i = n_{\text{int}} - 1, d = z \) and \( x = 0 \).
2. Update \( d \) with \( d - 2^i \tilde{y}_i \).
3. If \( d < 0 \), update \( d \) with \( d + 2^i \tilde{y}_i \) (\( d \) returns to the value before step 2) and set \( x_i = 0 \). If \( d \geq 0 \), set \( x_i = 1 \).
4. Decrement \( i \) by 1.
5. Repeat step 2-4 until \( i \) becomes \(-n_{\text{frac}} - 1 \) at step 4.
6. Output \( x \).

Note that \( 2^i \tilde{y}_i > \sum_{j=-n_{\text{frac}}}^{i-1} 2^j \tilde{y}_j \). This ensures that sequential subtractions by \( 2^i \tilde{y}_i \) and checking whether the difference is positive or negative lead to determining each digit of \( x \). The above procedure is implemented as the circuit in Figure 13. Note that we add dummy qubits which correspond to the \( 2n_{\text{int}} - 1 \)-th to \( n_{\text{int}} \)-th integer digits of \( z \). Also note that this circuit transforms the dividend register from \( |z \rangle \) to \( |0 \rangle \). If we want to reserve \( |z \rangle \), we can copy the state to another ancillary register by CNOT gates and use the copy as the dividend state. That is, we can do

\[
|z \rangle |0 \rangle |y \rangle \rightarrow |z \rangle |z \rangle |y \rangle |0 \rangle \rightarrow |z \rangle |0 \rangle |y \rangle |x \rangle.
\]

Despite the trick to truncate the digits, the structures of the circuits for truncated multiplication and division are similar to that in [42] and the restoring division circuit in [46] respectively. We therefore use the qubit number and T-count of the circuits in [42, 46] as those of our truncated arithmetic circuits. The exception is the qubit number of divider, for which
we use $5n$. This is larger than the value in [46] by $2n$, reflect-

\[11\] Actually, added qubits are not $2n$ but $n_{\text{req}} + n$, but we consider that $2n$ qubits are added for simplicity and conservativeness.

[1] R. Orus et al. "Quantum computing for finance: overview and prospects", Reviews in Physics 4, 100028 (2019)
[2] J. C. Hull, "Options, Futures, and Other Derivatives", Prentice Hall (2012)
[3] S. Shreve, "Stochastic Calculus for Finance I: The Binomial Asset Pricing Model", Springer (2004)
[4] S. Shreve, "Stochastic Calculus for Finance II: Continuous-Time Models", Springer (2004)
[5] A. Montanaro, Quantum speedup of Monte Carlo methods, Proc. Roy. Soc. Ser. A, 471, 2181 (2015)
[6] Y. Suzuki et. al., Amplitude Estimation without Phase Estimation, Quantum Information Processing, 19, 75 (2020)
[7] P. Rebentrost et. al., "Quantum computational finance: Monte Carlo pricing of financial derivatives", Phys. Rev. A 98, 022321 (2018)
[8] N. Stamatopoulos et al., "Option Pricing using Quantum Computers", arXiv:1905.02666
[9] S. Ramos-Calderer et al., "Quantum unary approach to option pricing", arXiv:1912.01618
[10] F. Black and M. Scholes, "The Pricing of Options and Corporate Liabilities", Journal of Political Economy 81, 637 (1973).
[11] R. C. Merton, "Theory of Rational Option Pricing", The Bell Journal of Economics and Management Science 4, 141 (1973)
[12] B. Dupire, "Pricing with a Smile", Risk, 7, 18-20 (1994)
[13] L. Grover et. al., Creating superpositions that correspond to efficiently integrable probability distributions, arXiv:quant-ph/0208112
[14] J. Gregory, "The xVA Challenge: Counterparty Credit Risk, Funding, Collateral and Capital", Wiley (2015)
[15] F. Arute et al., "Quantum supremacy using a programmable superconducting processor", Nature, 574, 505 (2019)
[16] E. T. Campbell et al., "Roads towards fault-tolerant universal quantum computation", Nature, 549, 172 (2017)
[17] K. Miyamoto and K. Shiobara, "Reduction of Qubits in Quantum Algorithm for Monte Carlo Simulation by Pseudo-random Number Generator", arXiv:1911.12469
[18] M. Amy et al., "A meet-in-the-middle algorithm for fast synthesis of depth-optimal quantum circuits", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 32(6): 818-830 (2013)
[19] P. Selinger, Phys. Rev. A 87, 042302 (2013)
[20] S. Bravyi and J. Haah, Magic-state distillation with low overhead, Phys. Rev. A 86, 052329 (2012)
[21] A. G. Fowler and C. Gilkey, "Low overhead quantum computation using lattice surgery", arXiv:1808.06709
[22] D. J. Egger et al., "Credit Risk Analysis using Quantum Computers", arXiv:1907.03044
[23] G. Maruyama, "On the Transition Probability Functions of the Markov Process", Rendiconti del Circolo Matematico di Palermo 4, 48 (1955)
[24] G. Bassard et. al., Quantum amplitude amplification and estimation, Contemporary Mathematics, 305, 53 (2002)
[25] K. Nakaji, "Faster Amplitude Estimation", arXiv:2003.02417

[26] V. Vedral et al., Quantum Networks for Elementary Arithmetic Operations, Phys. Rev. A 54, 147 (1996)
[27] D. Beckman et al., "Efficient networks for quantum factoring", Phys. Rev. A, 54, 1034 (1996)
[28] T. G. Draper, "Addition on a quantum computer", arXiv:quant-ph/0008033
[29] S. A. Cuccaro et al., "A new quantum ripple-carry addition circuit", The Eighth Workshop on Quantum Information Processing (2004)
[30] Y. Takahashi et al., "A linear-size quantum circuit for addition with no ancillary qubits", Quantum Information and Computation, 5(6), 440448 (2005)
[31] R. Van Meter et al., "Fast quantum modular exponentiation", Phys. Rev. A 71(5), 052320 (2005)
[32] T. G. Draper et al., "A logarithmic-depth quantum carry-lookahead adder", Quantum Information and Computation, 6(4), 351 (2006)
[33] Y. Takahashi et al., "Quantum addition circuits and unbounded fan-out", Quantum Information and Computation, 10(9&10), 0872 (2010)
[34] R. Portugal et al., "Reversible Karatsuba algorithm", Journal of Universal Computer Science, 12(5), 499 (2006)
[35] J. J. Alvarez-Sanchez et. al., "A quantum architecture for multiplying signed integers", Journal of Physics: Conference Series, 128(1), 012013 (2008)
[36] Y. Takahashi et al., "A fast quantum circuit for addition with few qubits", Quantum Information and Computation, 8(6), 636 (2008)
[37] H. Thapliyal, Mapping of subtractor and adder-subtractor circuits on reversible quantum gates, Transactions on Computational Science XXVI. 10, (2016)
[38] H. Thapliyal and N. Ranganathan, Design of Efficient Reversible Logic Based Binary and BCD Adder Circuits, J. Emerg. Technol. Comput. Syst. 9, 17, 1 (2013)
[39] C.-C. Lin et al., Qlib: Quantum module library, J. Emerg. Technol. Comput. Syst., 11, 1, pp. 7:17:20 (2014)
[40] H. M. H. Babu, Cost-efficient design of a quantum multiplier-accumulator unit, Quantum Information Processing, 16, 1, 30 (2016)
[41] H. V. Jayashree et al., Ancilla-input and garbage-output optimized design of a reversible quantum integer multiplier, The Journal of Supercomputing, 72, 4, 1477 (2016).
[42] E. Muñoz-Coreas and H. Thapliyal, "Quantum Circuit Design of a T-count Optimized Integer Multiplier", IEEE Transactions on Computers, 68, 5 (2019)
[43] A. Khosropour et al., "Quantum division circuit based on restoring division algorithm", Information Technology: New Generations (ITNG), 2011 Eighth International Conference on. IEEE, 2011, pp. 10371040.
[44] L. Jamal and H. M. H. Babu, Efficient approaches to design a reversible floating point divider, in 2013 IEEE International Symposium on Circuits and Systems (ISCAS2013), May 2013, pp. 30043007.
[45] S. V. Dibbo et al., An efficient design technique of a quantum divider circuit, in 2016 IEEE International Symposium on Circuits and Systems (ISCAS), May 2016, pp. 21022105.
[46] H. Thapliyal et al., "Quantum Circuit Designs of Integer Divi-
sion Optimizing T-count and T-depth”, IEEE Transactions on Emerging Topics in Computing (2019)
[47] M. Amy, D. Maslov, and M. Mosca, IEEE Trans. CAD 33(10), 1476 (2014)
[48] D. Maslov, "On the advantages of using relative phase Toffolis with an application to multiple control Toffoli optimization", Phys. Rev. A 93, 022311 (2016)
[49] M. E. ONeill, PCG: A Family of Simple Fast Space-Efficient Statistically Good Algorithms for Random Number Generation, Harvey Mudd College Computer Science Department Technical Report (2014); http://www.pcg-random.org/
[50] W. Hörmann and J. Leydold, "Continuous random variate generation by fast numerical inversion", ACM Transactions on Modeling and Computer Simulation 13(4):347, (2003)
[51] T. Haner et al., "Optimizing Quantum Circuits for Arithmetic", arXiv:1805.12445
[52] E. Muñoz-Coreas and H. Thapliyal, "T-count and Qubit Optimized Quantum Circuit Design of the Non-Restoring Square Root Algorithm", ACM Journal on Emerging Technologies in Computing Systems, 14, 3 (2018)
[53] V. Kliuchnikov et al., "Practical approximation of single-qubit unitaries by single-qubit quantum Clifford and T circuits", IEEE Transactions on Computers, 65, 1, 161 (2016)
[54] M. Amy et al., A meet-in-the-middle algorithm for fast synthesis of depth-optimal quantum circuits, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 32, 818 (2013).
Figure 1: The overview of the circuit for asset price evolution in the LV model in the PRN-on-a-register way. Here and hereafter, ancillary qubits are sometimes omitted for simple display.

Figure 2: The overview of the $U_j$, which performs the $j$-th step of asset price evolution, in the PRN-on-a-register way.
Figure 3: $V^{(j)}_k$, which updates $R_S$ if the asset price is in the $k$-th grid of the LV function. Here and hereafter, the wire going over a gate means that the corresponding register is not used in the operation of the gate. A formula at the center of a gate represents the operation the gate performs and '−1' means the inverse operation. A formula beside a wire and in a gate means the input or the output of the gate.
Figure 4: The gate which outputs whether $x = j$ and $y \in [\alpha, \beta]$ or not. The control by a register means the multiple control by qubits therein.
Figure 5: The circuits to generate PSNRN sequences.

(a) $J_w$, the gate to let the PSNRN sequence jump to the $i_{n+1}$ element.

(b) $P_w$, the gate to progress the PSNRN sequence by a step.
Figure 6: The gate to calculate the inverse CDF of standard normal distribution by piecewise polynomial approximation.
(a) The detail of the “Load $c_{m,i}$’s” gate.

(b) The detail of the “Load $c_{m,i}$” gate.

(c) The detail of the “Load $c_{m,i,k}$” gate.

Figure 7: Parts of the circuit in Figure 6. Here, $c_{m,i}$ means the $i$-th digit of $c_m$. Here, $c_{m,i,k}$ means the $k$-th digit of $c_{m,i}$.
Figure 8: The overview of the circuit for asset price evolution in the LV model in the register-per-RN way.
Figure 9: $U_j$, which performs the $j$-th step of asset price evolution, in the register-per-RN way.
(a) For $m \leq 6$.

(b) For $m \geq 7$.

Figure 10: Circuit to compute $f_i^{(m)}$. 
(a) The overview of SN gate.

(b) $U_{m}^{SN}$, the $m$-th step in the SN gate.

Figure 11: Implementation of the SN gate.
Figure 12: The circuit to perform truncated multiplication.
\[
\begin{align*}
|x_{n-1}\rangle &= |0\rangle \\
|a_1\rangle &= |0\rangle \\
|a_0\rangle &= |0\rangle \\
|x_{-1}\rangle &= |0\rangle \\
&\vdots \\
|x_{-n}\rangle &= |0\rangle \\
|y_{n-1}\rangle &= |0\rangle \\
&\vdots \\
|y_{-1}\rangle &= |0\rangle \\
&\vdots \\
|y_{-n}\rangle &= |0\rangle \\
|z_{2n-1}\rangle &= |0\rangle \\
&\vdots \\
|z_{n}\rangle &= |0\rangle \\
&\vdots \\
|z_{-n}\rangle &= |0\rangle \\
&\vdots \\
|z_{-2n}\rangle &= |0\rangle \\
&\vdots \\
|z_{-n}\rangle &= |0\rangle \\
&\vdots \\
|z_{-n-1}\rangle &= |0\rangle \\
&\vdots \\
|z_{-n-2}\rangle &= |0\rangle \\
&\vdots \\
&\vdots \\
|z_{-n-3}\rangle &= |0\rangle \\
&\vdots \\
|z_{-n-4}\rangle &= |0\rangle \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots \\
&\vdots 
é
\]

(a) The overview.

\[(a) The\ overview.\]

(b) The TruncDivPart gate. Note that in the 2’s complement method we can check whether a number is negative or not by seeing the most significant bit so we do not have to use an adder as a comparator.

Figure 13: The circuit for the truncated division.