Graphene-Silicon-On-Insulator (GSOI) Schottky Diode Photodetectors

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Graphene-silicon (GS) Schottky junctions have been demonstrated as an efficient architecture for photodetection. However, the response speed of such devices for free space light detection has so far been limited to 10’s-100’s of kHz for wavelength $\lambda > 500$nm. Here, we demonstrate graphene-silicon Schottky junction photodetectors fabricated on a silicon-on-insulator substrate (SOI) with response speeds approaching 1GHz, attributed to the reduction of the photo-active silicon layer thickness to 10$\mu$m and with it a suppression of speed-limiting diffusion currents. Graphene-silicon-on-insulator photodetectors (GSOI-PDs) exhibit a negligible influence of wavelength on response speed and only a modest compromise in responsivities compared to GS junctions fabricated on bulk silicon. Noise-equivalent-power (NEP) and specific detectivity ($D^*$) of GSOI photodetectors are 14.5pW and 7.83×10$^{10}$ cm Hz$^{1/2}$ W$^{-1}$, respectively, in ambient conditions. We further demonstrate that combining GSOI-PDs with micro-optical elements formed by modifying the surface topography enables engineering of the spectral and angular response.

Graphene is an appealing material to realize ultrafast and broadband photodetectors (PDs) due to its versatile electronic and optical properties such as high carrier mobility, ultrafast carrier dynamics and broadband optical absorption. However, graphene’s low mobility, ultrafast carrier dynamics and broadband electronic and optical properties such as high carrier mobilities and broadband photodetectors (PDs) due to its very fast and broadband absorption of light. However, graphene’s low optical absorption at optical wavelengths ($\sim 3\%$) and small photo-active area of devices are a bottleneck for photodetectors solely based on graphene. Photoresponsivities of graphene-based photodetectors based on metal-graphene-metal architectures (MGM) are typically below 10mA/W$^{-1}$ for visible (VIS) and near-infrared (NIR) wavelengths and the photoactive area is restricted to the periphery of the graphene contact. Various strategies have been exploited to enhance light absorption in graphene, e.g. by integrating graphene into optical microcavities or combining graphene with plasmonic nanostructures. More recently, graphene-silicon (GS) Schottky junction photodiodes have been demonstrated as an efficient platform for photodetection and photovoltaic applications. The co-integration of graphene with silicon technology allows the realization of a hybrid platform that is suitable for large scale fabrication due to the possible integration of graphene into back end-of-line (BEOL) complementary metal-oxide-semiconductor (CMOS) processing.

GS Schottky PDs exhibit a dual operating regime where both graphene and silicon act as active light absorbing materials for different wavelength ranges. Devices can show high responsivities on the order of hundreds of mA/W, comparable to commercial silicon photodiodes for wavelength ranges with photon energies above the silicon bandgap ($\lambda < 1.1\mu$m) which is facilitated by the high optical transmittance of graphene ($\sim 97.3\%$). Detection of light with energies below the silicon bandgap is enabled by the broadband absorption of graphene and responsivities reduce to a few mA/W$^{-1}$ or less for $\lambda > 1.1\mu$m. One important advantage of GS devices is their large photoactive area due to the vertical nature of the graphene-silicon junction as opposed to the lateral junction as in MGM photodetectors.

To date, the performance of GS PDs in terms of response speed remains far below that of MGM and commercial silicon photodetectors which exhibit cut-off frequencies (fc) on the order of GHz for free space light detection. Conversely, GS PDs demonstrated response speeds of 10’s-100’s of kHz for wavelengths $\lambda > 500$nm on the order of GHz for free space light detection. SOI wafers with a 10-300nm thick, lightly-doped (1-10 Ωcm) n-type silicon device layer (100) were employed to improve the response speed of GS devices is replacing commonly employed bulk silicon with a silicon-on-insulator (SOI) substrate. SOI, a thin silicon layer on top of a buried silicon oxide layer (BOX), is frequently used to implement CMOS electronics because of many advantages compared to their bulk silicon counterparts; SOI allows full dielectric isolation between neighboring devices, reduced leakage currents and reduced capacitive coupling, full depletion of the active silicon layer and 3-dimensional device architectures which makes SOI suitable for high speed and low power applications. SOI substrates additionally provide processing advantages since the BOX acts as a well-defined etch-stop and substrates can further be employed for micro-electromechanical-systems (MEMS).
to fabricate two sets of devices, a planar GSOI Schottky diode (GSOI-planar) and GSOI Schottky diode with a grating surface topography (GSOI-grating). The architecture of both device types is shown in Fig. 1. For the GSOI-planar device, graphene is transferred onto the flat (100) oriented silicon surface. For the GSOI-grating device, graphene is transferred onto an array of self-terminated V-grooves formed by anisotropic wet etching of silicon in KOH solution, exposing both the (100) and (111) silicon surfaces with an angle of 54.7° between them. To pattern the silicon surface of the GSOI-grating device, 100nm of SiO$_2$ were deposited on the silicon surface by inductively coupled plasma enhanced chemical vapor deposition (ICP-PECVD, Oxford Instruments). A grating structure consisting of an array of trenches (∼5.5µm wide) is patterned in the SiO$_2$ layer employing optical lithography and subsequent dry etching (reactive ion etching). This grating structure formed in the SiO$_2$ layer then serves as a hard mask for the anisotropic etching of silicon along the grating trenches carried out in 30wt% KOH solution at 80°C. As a result, 3µm deep (111)-self-terminated V-grooves are etched into the silicon surface. The substrate is then dipped in acetic acid to remove the KOH residues and the SiO$_2$ mask is completely removed by dry etching.

After the substrate fabrication for the GSOI-grating device, the device fabrication process is identical for both the GSOI-planar and GSOI-grating devices. The previously fabricated grating substrate and un-processed substrate (planar) are both coated with a 100nm thick silicon-dioxide (SiO$_2$) layer by ICP-PECVD (Oxford Instruments). Subsequently, two areas are opened in the SiO$_2$ layer for the formation of the GSOI junction and the metal-silicon contact. These areas are defined by optical lithography and the oxide layer in these areas is removed by wet etching in a buffer-oxide-etch (BOE) solution. In the case of the GSOI-grating device, the GSOI junction area corresponds to the previously patterned region. Right after the BOE of the oxide, contacts to the top silicon layer are fabricated by an additional lithography step followed by thermal evaporation of Au/Cr/Al (50nm/3nm/50nm) and lift-off. Aluminum is chosen as the metal contact to the silicon substrate as it forms an ohmic contact to silicon due to its low work function. The additional layers of Au/Cr on top of Al serve as protective layers for Al during subsequent BOE etching processes.

Commercially sourced graphene grown by chemical vapour deposition (CVD) on copper foil is spin coated with a 200nm thick poly-methyl-methacrylate (PMMA, 950K A4) layer before being etched in ammonium persulfate solution to remove the copper foil. The PMMA/graphene membrane is rinsed in de-ionised (DI) water twice before the final transfer to remove etchant and copper residues. The substrates are dipped in BOE for five seconds to remove any native oxide layer formed on the silicon area for the graphene-silicon junction window, before the wet transfer of CVD graphene. The substrates with the PMMA/graphene membrane are baked at 140°C for 5 minutes to enhance graphene adhesion to the substrate before removing the PMMA layer in an acetone bath. The shape of graphene is defined by optical lithography and subsequent O$_2$/Ar plasma etching (60s at 8W, Moorfield NanoETCH). A further optical lithography step is used to define the electrical contact to graphene and Au/Cr (50nm/3nm) are evaporated as contact metals with a following lift off step. Optical images of the finalized devices are shown in Fig. 1c,d. The quality of graphene on top of SiO$_2$ and on top of the silicon window is examined by Raman spectroscopy under 532nm laser excitation after completion of the device fabrication. Obtained Raman spectra (ESI) show a negligible D peak and a single Lorentzian 2D peak with a full width at half maximum (FWHM) below 35cm$^{-1}$, confirming the successful transfer of monolayer CVD-grown graphene.

The current density-voltage (J-V) characteristics of both the GSOI-planar and GSOI-grating devices are shown in Fig. 2. Devices were tested under dark conditions, at room temperature and in ambient atmosphere. Both device types exhibit a rectifying behavior with current on- to off-ratios ($I_{on}/I_{off}$, at ±2V), exceeding 10$^5$ and 10$^2$ for the GSOI-planar and the GSOI-grating device, respectively. It is notable that the GSOI-grating device exhibits an increased dark current density under reverse bias compared to the GSOI-planar device. The exact reason for this is unknown so far but we suspect that both the inhomogenous doping profile of graphene due to the patterned substrate as well as the differences in silicon surfaces in contact with graphene, (100) vs (111), will play a role. The J-V characteristic of an ideal diode can be described by the Shockley equation which allows the extraction of the ideality factor (n) and series resistance ($R_s$)

\[
I = A A^* T^2 \exp \left( \frac{-q\phi_B}{k_B T} \right) \left[ \exp \left( \frac{q(V - I R_S)}{n k_B T} \right) - 1 \right] \tag{1}
\]

Here, $A$ is the Schottky diode contact area, $A^*$ is the effective Richardson constant (112 A·cm$^{-2}$ K$^{-2}$) for n-type silicon) and $\phi_B$ is the Schottky barrier height (SBH) for a given voltage (V), $k_B$ is the Boltzmann constant, $q$ the electron charge, and $T$ is the temperature in Kelvin. The values of $n$ and $R_s$ obtained through fitting eq. (1) to the experimental data are 2.03 and 1.7kΩ for the SOI-planar device, respectively, and 5.23 and 1.21kΩ for the SOI-grating device, respectively. We intentionally employ a fit of eq. (1) over the whole bias voltage range despite deviations of the experimental data from ideal diode characteristics. This avoids vastly different results for $n$ and $R_s$ depending on which voltage region the experimental data has been fitted to. It further allows a fair compar-
FIG. 1: a) Schematic structure of the GSOI-planar device where graphene is transferred on the planar silicon (100) surface. b) Schematic structure of the GSOI-grating device where graphene is transferred on the structured silicon surface that consist of an array of V-grooves with (111) silicon facets separated by unpatterned planar (100) silicon lines of 3μm width. The V-grooves are 3μm deep and 5.5μm wide. c,d) Optical images of the fabricated devices. The active area of the GSOI-planar device is 4×4mm$^2$ and for the GSOI-grating is 0.5×0.5mm$^2$. Inset: Scanning electron micrograph (SEM) image of the grating structure formed by the V-grooves.

Subsequently, J-V measurements of both device types have been carried out under optical excitation at different wavelengths and varying optical powers. Fig. 2a) shows the J-V characteristics of the GSOI-planar device under illumination with $\lambda = 635$nm laser light at optical powers varying from $P = 2$nW...0.5mW (device area 4×4mm$^2$). As expected for a well-behaved photodiode, the forward current remains unchanged under illumination, however, the reverse current increases with increasing incident light powers due to generated photocurrents at the junction. The time dependent measurement of the current of the GSOI-planar device under intermittent illumination at a reverse bias of $V_b = 2$V (Fig. 2b)) shows that light powers as low as 500pW, corresponding to an intensity of $\sim 3$nW/cm$^2$, can be clearly detected. It demonstrates the high sensitivity of the GSOI-planar device due to the low dark current of $\sim 4$nA ($\sim 25$nA/cm$^2$). Fig. 2c) shows transient measurements conducted with different laser wavelengths at constant power ($P = 1$µW) when the device is operated at $V_b = 2$V reverse bias. The responsivity of the device is 0.23A/W, 0.26A/W and 0.029A/W for 520, 635 and 980nm laser light, respectively. Fig. 2d) demonstrates the bias voltage dependence of the photoresponse of the GSOI-planar device under $\lambda = 635$nm laser light illumination. Higher reverse biases increase the depletion width of the Schottky junction and increase the electric field in the deple-
tion region which facilitates separation of photogenerated carries[31, 42].

FIG. 3: Photoresponse of the GSOI-planar device in various conditions. a) J-V characteristics under different light powers (P = 2nW..0.5mW) at \( \lambda = 635 \text{nm} \) wavelength. b) Transient measurement under decreasing light powers (P = 10nW..0.5nW) at \( \lambda = 635 \text{nm} \) wavelength at \( V_b = 2V \) reverse bias. c) Photocurrent response of the device for different wavelengths at constant light power (P = 1 \( \mu W \)) under \( V_b = 2V \) reverse bias. d) Photocurrent response of the device at different reverse biases (\( V_b = 0..2V \)) at \( \lambda = 635 \text{nm} \) intermittent illumination (P = 1 \( \mu W \)).

Sensitivity is an important metric that represents the performance of a photodetector by quantifying the ultimate capability to detect weakest signals. Achieving high sensitivity requires both large responsivity R and low noise. Noise-equivalent-power (NEP) and specific detectivity (D*) quantify the detection limit of a photodetector and are defined as:

\[
\text{NEP} = \frac{\text{Noise}_{\text{RMS}}}{R} \quad \text{(2)} \quad D^* = \frac{\sqrt{A_d \Delta f}}{\text{NEP}} \quad \text{(3)}
\]

where NEP is the incident optical power that results in a signal-to-noise ratio (SNR) of one, R is the responsivity of the device at a given wavelength and bias conditions, \( A_d \) is the photoactive device area and \( \Delta f \) is the electrical bandwidth. The NEP is determined by the ratio of the root-mean-square (RMS) noise and responsivity R of the photodetector at a given wavelength. To extract NEP and \( D^* \), the time-dependent response of the GSOI-planar device has been recorded with 8 Hz sampling rate at bias voltages of \( V_b = 0 \) and 2V, respectively, under optical excitation at a wavelength of \( \lambda = 520 \text{nm} \), chopped at 0.5s intervals. Fig 3(h) shows the IV characteristics of the GSOI-planar device in the dark and under periodic optical excitation with decreasing optical power at a bias voltage of \( V_b = 0 \text{V} \). The RMS noise is extracted from the measurement in the dark, equating to 2.89pA. NEP and \( D^* \) of the GSOI-planar device are calculated to be 14.5pW and 7.83\( \times 10^{10} \) cm Hz\(^{1/2}\)W\(^{-1}\), respectively. Under an applied reverse bias of \( V_b = 2 \text{V} \), shown in Fig 4(h), the rise in the dark current leads to an increase in the RMS noise to 4.06pA. The NEP increases by \( \sim 20\% \) to 17.7pW and \( D^* \) decreases to 6.41\( \times 10^{10} \) cm Hz\(^{1/2}\)W\(^{-1}\), respectively. As such, a reduction of the photoactive silicon thickness from 500\( \mu \text{m} \) (bulk) to 10\( \mu \text{m} \) (SOI) leads to a \( \sim 10 \) times improved NEP for the GSOI-planar device due to reduced noise. We anticipate that a passivation/encapsulation of the graphene surface will improve the sensitivity of GSOI photodetectors further. Passivation will prevent the adsorption of e.g. H\(_2\)O and O\(_2\) from the ambient environment onto graphene and reduce electronic noise[49]. Additional sensitivity enhancement can be achieved through engineering of the graphene-silicon interface to further reduce dark currents[22, 31].

FIG. 4: Time dependent current of the GSOI-planar device under low light power in ambient condition. The device is intermittently illuminated with laser light of \( \lambda = 520 \text{nm} \) wavelength of sub-nanowatt intensity to characterize Noise\(_{\text{RMS}}\), NEP and \( D^* \) under different reverse bias voltages of a) \( V_b = 0 \text{V} \) and b) \( V_b = 2 \text{V} \).

The high-speed optical response of both devices has been evaluated for wavelengths ranging from the near UV to NIR employing a picosecond white light laser source (Fianium, pulse duration \( \tau_{\text{pulse}} < 80\)ps at all wavelengths) and optical bandpass filters (FWHM \( \leq 10 \text{nm} \)). The electrical response was recorded using a transimpedance preamplifier (Phillips Scientific 6954) and an oscilloscope (WaveJet 354-A) while the devices
were operated under zero bias conditions ($V_b = 0V$). The current response $I$ of the devices to the picosecond light pulses is shown in Figs.5(a,b) and has been fitted with a biexponential function

$$I = I_{\text{max}} \times (1 - e^{-\frac{t}{\tau_r}}) \times e^{-\frac{t}{\tau_f}}$$ (4)\

with $I_{\text{max}}$ the peak response, $\tau_r$ and $\tau_f$ the rise- and fall-times at which the response occurs. The rise- and fall-times of the GSOSI-grating device are $\tau_r < 4\text{ns}$ and $\tau_f \sim 10\text{-}15\text{ns}$ for all tested wavelengths ($\lambda = 420\text{-}900\text{nm}$) and are moreover almost constant for all wavelengths. The GSOSI-planar device exhibits slightly increased rise- and fall-times in the orders of $\tau_r \sim 10\text{ns}$ and $\tau_f \sim 20\text{-}70\text{ns}$, attributed to the larger average thickness of the active silicon layer of the GSOSI-planar device compared to the GSOSI-grating device with a patterned surface. Note that fall-times can be further decreased upon application of a bias voltage $V_b$ to facilitate extracting charge carriers out of the device; due to restrictions in our characterization setup this is not possible in present experiments.

The temporal response of a photodiode to an instant injection of excess carriers upon photon absorption depends mainly on three independent components which can be expressed[50] by

$$\tau_r = \sqrt{\tau_{\text{RC}}^2 + \tau_{\text{dr}}^2 + \tau_{\text{diff}}^2}$$ (5)\

with $\tau_r$ the overall 10% to 90% response time of the photodiode, $\tau_{\text{RC}}$ the resistor-capacitor (RC) time constant of the photodiode, $\tau_{\text{dr}}$ the electric-field driven drift time of the carriers in the depletion region and $\tau_{\text{diff}}$ the diffusion time of carriers in the non-depleted region of the substrate. The wavelength dependent optical absorption coefficient of silicon determines the penetration depth of incident light into the silicon substrate according to Beer-Lambert law[42]. Generally, light of shorter wavelengths has a shallow penetration depth while light of longer wavelengths can penetrate much deeper into the bulk of the silicon substrate. In other words, incident short wavelength light optically excites charge carriers in the silicon close to the substrate surface while long wavelength creates charge carriers deep within the silicon substrate. Considering a depletion region length $L_D$ of the Schottky junction for employed low doped silicon on the order of $1\text{-}2 \mu m$[31], this implies complete absorption of short wavelength light (e.g. $\lambda = 450\text{nm}$) within the depletion region while only $\sim 50\%$ and $\sim 15\%$ of light of $\lambda = 550\text{nm}$ and $\lambda = 700\text{nm}$ wavelengths, respectively, are absorbed within the depletion region. The light absorbed deeper within the silicon substrate, outside the depletion region length of the Schottky junction, thus creates charge carriers that contribute to the response by a diffusion process. The transit time for charge carriers within the depletion region for zero external bias condition depends on the depletion region length $L_D$ and the electric field $E$ due to the built in potential $V_{\text{bi}}$ of the Schottky junction and can be estimated by $\tau_{\text{dr}} = \frac{L_D}{\mu E} = \frac{L_D^2}{V_{\text{bi}}}$ to $\sim 82\text{ps}$ for holes and $\sim 26\text{ps}$ for electrons based on mobilities for holes and electrons of $\mu_p = 450\text{cm}^2\text{Vs}^{-1}$ and $\mu_n = 1400\text{cm}^2\text{Vs}^{-1}$, respectively. However, charge carriers contributing to diffusion currents from deep within the silicon substrate need to travel far longer distances. The required time for diffusion can be calculated via $\tau_{\text{diff}} = \frac{L_D^2}{D_{\text{p}}}$. In the case of a bulk silicon substrate, the diffusion length $L_D$ for holes is determined by the thickness of the active silicon layer. The diffusion coefficient $D_p = \mu_p \frac{kT}{\tau_p}$ can be evaluated from the mobility of holes ($\mu_p \sim 450\text{cm}^2\text{Vs}^{-1}$) in lowly n-doped silicon. Using a recombination time of $\tau_p = 2 \times 10^{-4}\text{s}$ for n-type silicon with a doping level of $N_d = 3.5\times 10^{14}\text{cm}^{-3}$, the diffusion length $L_D$ is calculated as $L_D = \sqrt{D_p \tau_p} = 480 \mu m$ which is comparable to the thickness of a standard silicon substrate.

In a straightforward manner, the necessary time $\tau_{\text{diff}}$ for a hole to diffuse $10\mu m$ and $480\mu m$, representative of employed SOI wafers and typically employed bulk silicon wafers with identical doping concentration of $N_d \sim 3.5\times 10^{14}\text{cm}^{-3}$, can be calculated as $\sim 42\text{ns}$ and $\sim 98\mu s$, respectively. As such we argue that the decrease of the

![FIG. 5: Time-resolved photoresponse of a) the GSOSI-grating and b) the GSOSI-planar device under illumination with a picosecond white light source at various wavelengths. Note change of scale of time-axis.](image-url)
active optical silicon layer thickness to 10µm in our devices based on SOI material and with it a reduction of speed limiting diffusion currents is the major reason for an increase of the operating speed of both the GSOI-planar and GSOI-grating device by more than two orders of magnitude compared to GS devices based on bulk silicon.

The argument of diffusion currents being the speed limiting component is further supported by comparing the 3-dB cut-off frequency ($f_c$) of our GSOI devices fabricated on SOI substrate with GS junction diodes fabricated on bulk silicon substrates in the literature, including our previous report (Fig.6) [31]. The corresponding cut-off frequencies of the GSOI-grating, GSOI-planar and reference devices are determined from the measured and reported rise times $\tau_r$ as $f_c = 0.34/\tau_r$ [51]. Fig.6 shows the cut-off frequency ($f_c$) vs photoactive device area for various wavelengths of our own devices and devices reported in the literature. It can be seen that despite an active area of our devices comparable to or greater than devices fabricated on bulk silicon, our devices fabricated on SOI substrate exhibit an increase in cut-off frequency of several orders of magnitude. It further demonstrates that the increase in cut-off frequency $f_c$ of our devices cannot be attributed to a simple decrease of the RC-time constant due to down scaling contact and junction areas. To the best of our knowledge, our graphene-silicon Schottky photodetectors on SOI substrate are the fastest to date for free space light detection, especially in the VIS and NIR wavelength range $\lambda > 500$nm.

![Image of diagram](image.png)

**FIG. 6:** Comparison of the 3dB cut-off frequency $f_c$ versus photoactive device area of our GSOI-photodetectors with GS Schottky photodetectors fabricated on bulk silicon photodiodes at various wavelengths.

The spectral response of the photodetectors on SOI substrate in comparison with a device fabricated on 500µm thick bulk n-type silicon with identical doping level is shown in Fig(7a). All three device types show similar responsivities for shorter wavelengths $\lambda < 450$nm since incident light in this wavelength range is totally absorbed within the first top 10µm of silicon. Light of longer wavelengths $\lambda > 450$nm can penetrate deeper into the silicon substrate due to the reduced absorption coefficient. For longer wavelengths, only part of the incident light is absorbed within the active top silicon layer of the SOI substrate and the remaining light power is transmitted into the BOX and silicon handle wafer where it does not contribute to the photoresponse. This is manifested in Fig(7b) as a reduced responsivity of the GSOI devices compared to GS devices fabricated on bulk silicon for longer wavelength light $\lambda > 900$nm. It is further noticeable that the spectral response of the GSOI-grating device is almost flat in the wavelength range $\sim 400$-800nm compared to both the GSOI-planar and bulk silicon device, easier recognizable in the plot of the spectral dependence of the responsivities for each device type normalized to their respective peak responsivities (Fig(7b)).

This flat spectral photoresponse of the GS-grating device can be attributed to the surface topography of the device. The V-grooves form micro-optical elements that allow direct transmission of incident light into the silicon substrate but also reflect light that is unused in planar devices back into the substrate [52-54]. Fig(7c,d) show the simulated electromagnetic power loss for a unit cell of the grating and planar device, respectively, for normal incident light (p-polarized) at a wavelength of $\lambda = 980$nm (ESI). The blue arrows are indicate the transmitted and reflected light paths. Light incident on the GSOI-grating device with 54.7° sloped facets will be partially transmitted into the silicon substrate after undergoing refraction. However, the reflected light component is directed towards the opposite facet and also partially absorbed by the substrate. Additionally, the active silicon layer of the SOI substrate of both the GSOI-grating and the GSOI-planar device forms an optical cavity where multiple reflections between the topmost air-silicon, silicon-BOX and BOX-handle silicon interfaces lead to optical interference effects. This is clearly visible in the zoom-in on the electromagnetic losses in the GSOI-planar device (Fig(7c)). The surface topography of the GSOI-grating device leads to greater electromagnetic power losses (absorption) within the active silicon layer compared to the GSOI-planar device and allows tailoring the spectral response of GS photodetectors. However, we note that optical absorption on its own does not fully describe the electrical responsivity. Optically excited charge carriers contribute to the photocurrent via diffusion and drift processes subject to electric fields in the formed junction which can be particularly complex, especially for the grating device.

Devices fabricated on SOI substrate are further sensitive to the angle of incident light. Fig(7f) shows a measurement of the angular dependence of the responsivity...
FIG. 7: Effect of substrate thickness, surface topography, and incident angle on the spectral response of GS Schottky photodiodes. a) Spectral responsivity of the GSOI-planar and -grating device and comparison with a GS Schottky diode fabricated on a ∼500 µm thick silicon substrate. b) Comparison of normalized responsivity of GSOI-planar, GSOI-grating and bulk GS diode. c,d) Simulated relative electromagnetic power loss density in the grating and planar device, respectively, for normal incidence light and at a wavelength of λ = 980 nm. Blue arrows indicate the light reflection and transmission, respectively. Zoom-in: Interference effects in the planar device. e) Angular dependence of the responsivity of the GSOI-planar and -grating device, respectively.

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