FPGA-based GEM detector signal acquisition for SXR spectroscopy system

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Abstract: The presented work is related to the Gas Electron Multiplier (GEM) detector soft X-ray spectroscopy system for tokamak applications. The used GEM detector has one-dimensional, 128 channel readout structure. The channels are connected to the radiation-hard electronics with configurable analog stage and fast ADCs, supporting speeds of 125 MSPS for each channel. The digitalized data is sent directly to the FPGAs using fast serial links. The preprocessing algorithms are implemented in the FPGAs, with the data buffering made in the on-board 2Gb DDR3 memory chips. After the algorithmic stage, the data is sent to the Intel Xeon-based PC for further postprocessing using PCI-Express link Gen 2. For connection of multiple FPGAs, PCI-Express switch 8-to-1 was designed. The whole system can support up to 2048 analog channels. The scope of the work is an FPGA-based implementation of the recorder of the raw signal from GEM detector. Since the system will work in a very challenging environment (neutron radiation, intense electro-magnetic fields), the registered signals from the GEM detector can be corrupted. In the case of the very intense hot plasma radiation (e.g. laser generated plasma), the registered signals can overlap. Therefore, it is valuable to register the raw signals from the GEM detector with high number of events during soft X-ray radiation. The signal analysis will have the direct impact on the implementation of photon energy computation algorithms. As the result, the system will produce energy spectra and topological distribution of soft X-ray radiation. The advanced software was developed in order to perform complex system startup and monitoring of hardware units. Using the array of two one-dimensional GEM detectors it will be possible to perform tomographic reconstruction of plasma impurities radiation in the SXR region.

Keywords: Computing (architecture, farms, GRID for recording, storage, archiving, and distribution of data); Modular electronics; Plasma diagnostics - charged-particle spectroscopy; Micropattern gaseous detectors (MSGC, GEM, THGEM, RETHGEM, MHSP, MICROPIC, MICROMEGAS, In-Grid, etc)

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1 Introduction

The presented work is related to the currently being developed measurement system for plasma soft X-ray (SXR) spectroscopy, for use in ITER-oriented tokamaks. As a sensor unit, the Gas-Electron-Multiplier (GEM) detector is used, with 128-channel, 1-dimensional readout board [1, 2]. The designed system contains FPGA units for signals preprocessing, fast interconnects to the PC system using PCI-Express Gen2 standard and multiple analog input channels. The system can work with up to 512 input channels per one PCI-Express slot.

The goal of the project is to produce two kinds of spectra:

- SXR energy spectrum
- SXR topological spectrum

of the observed tokamaks’ plasma.

One of the main difficulties is the intense plasma SXR radiation resulting in photon fluxes of $10^5$-$10^6$ counts/mm$^2$s (peak value). Therefore, special care must be taken for the algorithms development and overall system’s data processing speed.

The presented system is a second generation of the SXR measurement system designed by the Team. The first generation system is KX1 installed at JET (Culham, U.K.). Examples of final spectra are presented in figure 1, as a result of plasma shot at JET tokamak [2, 3].

2 System architecture

The system consists of several functional hardware blocks. The GEM detector is connected to the signal acquisition blocks (64 input channels each). This section includes Radiation Hard Analog Front-End Boards (AFEs) and Analog-Digital Converter Boards (ADBs). The blocks’
Figure 1. Example of energy and topological spectra. Result of a plasma shot at JET tokamak [4].

main features are signal shaping, long distance analogue signal transmission with user correction (in term of offsets, and signal gain) and finally conversion to the digital representation of the signal. The digitalized samples are transmitted to the backplane boards containing FPGAs with DDR3 memory for data preprocessing and fast PCI-Express Gen2 interface for computed values transmission to the PC. One backplane board can work with up to 64 input channels from GEM detector.

The backplane boards are connected to the PCI-Express Switch Gen3 8-to-1, installed in the high-performance mainframe PC. The preprocessed data is transmitted from the FPGA DDR3 memory to the PC using PCI-E links from each backplane board. Then, postprocessing software is run in order to compute the SXR spectra — energy and topology. The system architecture is presented in figure 2.

The mainframe PC contains also specialized control and diagnostics software (FCS). System setup is performed through PCI-Express links and USB configuration links. Details of the hardware components of the system are presented in following section [5].

3 System components

The main key components of the system in term of analog signal transmission from the GEM detector, are:

- Radiation Hard Analog Front-End Board (AFE);
- Analog-Digital Converter Board (ADB).

The boards of the first type will be located near the tokamak (directly in the port). Therefore, the electronic components installed there must be radiation hard. One AFE board can work with 16 analog input channels from the GEM detector. The boards contain transimpedance amplifiers and signal shaper circuits. The signal offset can be manually corrected from the PC resulting in the high dynamic input range of the ADC chip. This is necessary also because of significant parameters dispersion of the installed operational amplifiers. The boards also offer the analog signal integration


mode (not yet tested). The board outputs form signals using VHDCI cables with a differential analog transmission. Figure 3 presents the designed AFE board.

The second described board is an Analog-Digital Converter Board (ADB). These boards are installed in the separate rack with the distance of 1–2 m from the AFE boards. The connection is made with VHDCI cables. Each cable transmits 16 analog channels with control signals for the AFE boards. The ADB boards contains two stage amplification path for each channel:

- The single-ended variable-gain amplifier with independent gain correction;
- The second stage amplifier with offset correction and single-ended to differential signal conversion.

The input channels can work in two selectable modes: with AC or DC coupling.

All of the settings including gain, offset correction and coupling mode needs to be tuned in order to achieve the highest dynamic range of the signal, matching the ADC input range.
Figure 4. The Analog-Digital Converter Board (ADB) designed by the team.

The analogue signals are sampled by the ADCs with tuneable sampling frequency varying from 75 MHz to 125 MHz. Currently, the system works at 75 MHz. The digitalized samples are passed to the FPGAs on the backplane boards. The ADBs are installed in slots in backplane boards. Figure 4 presents the designed ADB board.

More details about the construction of the system can be also found in following publications [4, 6–8].

4 Developed FPGA Firmware for signal acquisition

The backplane board consists of Xilinx Artix7 FPGA with 2Gb DDR3 PC-800 memory. The communication with the PC system is done through implemented in the FPGA PCI-Express Gen2 link. For the slow control of the HDL components AXI4-Lite and Wishbone interfaces are used. PC is a master unit, which manages the interfaces through PCI-Express using memory-mapped access.

The developed advanced signal acquisition FPGA firmware consists of:

• Fast ADCs SERDES interfaces — provides hardware interface for a fast digital transmission from ADCs together with the clock synchronization in the FPGA;

• 64 channels raw signal recorder — the FPGA can register 40 samples of the raw signal directly from the ADCs on each channel simultaneously using 75 MHz sampling frequency;

• Timestamp generation for each event;

• Extensive data acquisition management block controlling:
  – Triggering unit — independent trigger for each input channel;
  – AXI Data Mover — management of the transmission between the raw signal recorder and DDR3 memory interface;

• AXI4-Stream standard was used for handling large data streams from the GEM detector.

The detailed implementation of the data path from the GEM detector to the PC is shown in figure 5. Currently the algorithm can register up to 100 000 events with event frequency of approximately 450 kHz in all channels. The speed can be significantly improved with the introduction of data
clustering and online charge computation in the FPGA. The final data processing speed should be sufficient for the target application.

For the extensive system configuration with automatic diagnostics, the FCS (FPGA Configuration Software) is used [9, 10].

After successful signals acquisition, the registered data is sent to the PC unit for further postprocessing, described in [11–13]. It is also planned to implement in the FPGA the DMA block for fast data transmission between the backplane DDR3 memory and PC.

The implemented firmware was verified in HDL simulation software under the scope of proper data processing. Data path containing signal input and algorithm blocks, AXI-Stream interface, AXI-DataMover and data transmission interface to the DDR3 memory was simulated and tested. As the test input signal, there was a 1 MHz digital pulse, simulating the response from the GEM detector, connected to each input channel.

The results of the tests determined the maximum throughput of the system in terms of data registration in the DDR3 memory. Figure 6 presents HDL code simulation of the implemented firmware.

5 Soft X-ray measurement system test stand

The developed measurement system needs an advanced test stand in order to correctly verify its functionality. Figure 7 presents the currently used test stand.

The test stand consists of:

- GEM detector with 1 dimensional, 256 channel readout board [14];
Figure 6. HDL simulation testbench of the implemented firmware in Xilinx Artx7 FPGA.

Figure 7. Currently used test bench for the signal acquisition of the SXR measurement system.

- $^{55}$Fe soft X-ray source (around 1 kHz events);
- Gas supply for the GEM detector: 70% Ar, 30% CO$_2$;
- Mainframe PC with the following specification: Intel Xeon CPU E5-2630v3 @ 2.40GHz, Intel S2600CW mainboard, DDR4 2133 (PC4 17000), PCI-Express Gen3 switch 8-to-1;
- Backplane board with one ADB and one AFE board — currently supporting 16 input channels.

The first tests were done with 16 input channels, using the special signal adapter allowing to inject analog signals to the AFE board. The signals can be standard sine or square waves. However,
it is also possible to provide fast, narrow analog pulses simulating the response of the GEM detector to soft X-ray radiation.

The signals generated from the function generation unit in shape of narrow pulses were used to verify:

- Proper signal transmission from the input connector on AFE board to the ADB board;
- Correct signal registration by ADCs with 75 MHz sampling frequency;
- Proper offset and gain correction;
- Proper channels alignment in the FPGA firmware;
- Correct signal registration in the FPGA memory;
- Correct HDL algorithms control from the PC unit;
- Verification of the developed FCS application for the control of the system and data download.

6 Summary

The presented FPGA-based SXR spectroscopy system is a complex, high-performance measurement system. Its main advantage is a high number of input channels, combined with a systems’ modularity. The paper presents the overall system architecture with the description of the designed key hardware components: AFE, ADB, FPGA backplane and PCI-E switch boards [4] and implemented advanced firmware for data registration and processing.

The developed FPGA firmware can register 40 samples of raw data from the 64 input channels and store them in the DDR3 memory. Memory upload to the postprocessing PC unit is done with the use of a PCI-Express link. Since the firmware design is complicated, intense simulations were done including data path and DDR3 memory verification. It was also possible to determine the overall system throughput in terms of data storage.

The complete test stand was designed including the GEM detector, an X-ray source and the measurement system including FPGA board and mainframe PC. In order to verify the prototype hardware, multiple tests were made with signal generator on 16 analogue input channels, simulating the response from the GEM detector.

Since the system is still under development, the next steps will include: the integration with Matlab postprocessing algorithms, the development of automatic system calibration algorithms, the integration of the high-voltage supply unit and registration of $^{55}$Fe signals from GEM detector. This will provide first energy and topology spectra.

Also, the charge computation algorithms are planned to be included in the FPGA in order to decrease the amount of the data sent to PC unit and to achieve the higher event processing speed.

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