Phase sequence interchange scheme for suppressing transient cross regulation on the compensator controlled and non-compensator controlled single-inductor dual-output buck converter

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Abstract
Single input multiple output (SIMO) buck converter is a good solution to enhance the area efficiency of the power management unit. Because the SIMO type buck converter uses only one inductor to buffer the transferred energy for the multiple output ports, it usually suffers from severe transient cross regulation in a continuous conduction mode. Most of the well-known approaches to suppress the transient cross regulation are either to create the additional free-wheeling loop or to refine the controller loop. The control logic is usually quite specific which may not apply to the other controller types controller.

A phase sequence interchange (PSI) scheme is proposed to mitigate the transient cross regulation without modifying the original control design. Compared to the other techniques, the proposed method can be easily applied, but not limited to the compensator-based control or the non-compensator-based control in the buck converter. This study starts with the illustration of the reason why the PSI can mitigate the transient cross regulation. Detail designs are then presented to implement the proposed scheme on both the compensator type and the non-compensator type controls. Experimental results show that the suppression of the cross regulation is comparable to the other state of the arts.

1 | INTRODUCTION

Switching type power converters are very common in the power management unit (PMU) to serve the integrated circuits. The converter of this type needs an inductor to buffer the transferred energy, but it inevitably occupies certain circuit area. This situation is even critical as the number of the converter increases within the PMU. Alternatively, a single-inductor multiple-output (SIMO) DC-DC converter is the right topology to save this problem. However, the output ports of this topology could suffer from cross regulation when the inductor current continues to feed different ports. Although the SIMO scheme shows its merits of low cost and area efficiency, the aforementioned drawback is the issue that designers should overcome.

Generally, the controller design of the SIMO converter is quite challenging because it needs to keep energy delivery balance among different output ports. To make the idea more feasible and easier to implement, the single-inductor dual-output (SIDO) buck converter still prevails because of its simpler control type and current feeding capability. The control strategies for the SIDO buck converter are similar to that of the SIMO type. The major issue of the energy distribution between the inductor and the output ports was thoroughly discussed in the following studies. The author in [1, 2] introduced time-multiplexing control to make the inductor deliver energy to each output port within a cycle time. Because energy delivery cycle is independent from one to the other, cross regulation is rarely found when the SIDO is operating in either the boundary conduction mode or the discontinuous conduction mode [3, 4]. However, if the inductor current increases to continuous conduction mode (CCM), energy distribution to each load cannot be isolated from each other, the SIDO may
encounter severe transient cross regulation. To solve this problem, the pseudocontinuous conduction mode (PCCM) was proposed [5]. The PCCM scheme is to use the additional freewheeling path to buffer the high current impact to the output port. Various controls based on this concept were proposed in recent years [6–15]. The common feature of the approaches of the literatures is to use a specific way to refine the control scheme with the expense of design complexity, and some of them could impact the control stability.

The other way to reduce the cross regulation is to reformat the circuit structure. For example, a topology synthesis methodology [16] is to synthesize the SIDO and Dual-Input Single-Output (DISO) structure to mitigate the cross regulation problem. A single coupled-inductor dual output with a soft-switching technique was proposed to improve the cross regulation [17]. A predictive control model was applied to the current control loop to reduce the cross regulation [18]. The proposed solutions are generally involved in changing the circuit structure, or in adding more circuit resources to achieve the goal. The similar kind of the approach may not be suitable for the area efficiency within the PMU.

From the aforementioned comparison, we can deduce several key points for implementing the SIDO buck converter inside the PMU: (1) The structure of SIDO should be simple for the circuit efficiency. (2) It should operate at fixed switching frequency for the ease of filter design. (3) Low cross regulation is expected under load transient. In order to reduce the impact of transient cross regulation, this study introduces a phase sequence interchange (PSI) concept by properly arranging the energy-feeding sequence to loads. The significance of the PSI scheme is its universal use in any type of the control within the SIDO converter irrespective of the compensator-based or non-compensator-based control.

The study organisation is arranged as follows: following the introduction, Section 2 illustrates the cause and the way to mitigate the transient cross regulation for a SIDO buck converter. In Section 3, the implementation of the PSI on the compensator-based SIDO buck converter is introduced. This section also demonstrates the stability analysis for the design of the voltage mode SIDO buck converter. In Section 4, the implementation of the PSI on the ripple-based SIDO buck converter is presented. This section describes how the PSI can avoid the voltage surge in the adaptive off-time (AFT) control. Section 5 demonstrates the experimental results to validate the effectiveness of the proposed method. Finally, Section 6 summarizes the features and contributions of the design.

2 | CAUSE OF TRANSIENT CROSS REGULATION AND ITS SUPPRESSION

2.1 | Operating principle of the SIDO buck converter

Transient cross regulation occurs on the load transient state. When one of the output ports is undergoing load transient, the other output ports would encounter voltage disturbance.

Figure 1 shows the simplified circuit topology of the SIDO buck converter. Figure 2(a) shows the duty cycle of each switch and the inductor current waveform of a SIDO buck converter operating at steady-state, respectively. To simplify the explanation, the alphabet A is used to represent the period when the energy is delivered to the output port A (phase A). Alphabet B indicates the period when energy is delivered to output port B (phase B). Note that the energy delivery sequence begins at phase A, then ends at phase B within a switching cycle. $T_{change}$ is the period of energy distribution from source to the phase A, and $T_r$ represents the total period of energy distribution from source to both phases A and B. $T_{change}$ is determined by the feedback signal from the preceding phase (phase A). $T_r$ is decided by the feedback signal from the latter phase (phase B).

Figure 2(b) shows the inductor current when the phase A load steps down. It can be seen that $T_{change}$ becomes shorter in response to the load decrease in phase A. During the same switching period ($T_s$), the charging period for phase B becomes longer due to the constant $T_r$. This phenomenon results in voltage rise at the output port B due to the excess energy flowing to phase B. On the other hand, Figure 2(c) shows the inductor current when the phase A load steps up, $T_{change}$ becomes longer and thus squeezes the charging period for phase B. The voltage drop at the output port B occurs because less energy is distributed to the phase B load.

Figure 3 shows the inductor current waveforms when the latter phase (phase B) is changing the load. It is obvious to see that the consequence is quite different from that of the case in Figure 2. When the phase B load steps-up or steps-down, Figure 3b,c shows that the $T_{change}$ remains the same. $T_r$ is the only one that should be corrected in response to the load change in phase B. As a result, there is no voltage disturbance in phase A. Transient cross regulation is not evident in this case.

2.2 | Phase sequence interchange

The aforementioned observation implies that the load feeding sequence is the key to affect transient cross regulation. Transient cross regulation is small as load transient occurs at the latter load feeding sequence. Whenever we find the phase load is stepping up at the preceding phase of the load feeding sequence, the load feeding sequence is exchanged such that the disturbed load will be fed at the last order. This mechanism is
named PSI. Figure 4 depicts the voltage-mode SIDO buck converter using the PSI scheme. Activation of PSI is determined by a signal selector, which is designed to judge whether the load is stepping up or not.

3 | IMPLEMENTATION OF THE PSI ON THE COMPENSATOR-BASED SIDO BUCK CONVERTER

Figure 5 demonstrates the flowchart to implement the PSI scheme in the compensator-based SIDO buck. Detail design is described as follows.

3.1 | Counter: A fixed saw-tooth

Assume 250 MHz clock frequency $f_{clk}$ is used, the switching frequency $f_{sw}$ of the SIDO buck system is determined at 1 MHz, the resolution is calculated as follows:

$$\text{Resolution} = \frac{f_{clk}}{f_{sw}} = 2^{n_{\text{counter}}} = \frac{250 \text{MHz}}{1 \text{MHz}} \approx 2^8$$  \hspace{1cm} (1)

An eight-bit counter is chosen to generate the fixed saw-tooth waveform, such that
In addition to an eight-bit counter, the structure also generates a 1 MHz switching frequency signal and a 1 MHz sampling frequency signal to trigger other digital blocks and ADCs, respectively.

3.2 Digital PWM algorithm

Digital PWM (DPWM) produces duty cycle signals to control the on/off time of the switches. As shown in Figure 5, it compares the signal DC from COMP with an eight-bit sawtooth counter and generates duty cycle.

3.3 PSI soft start mechanism

The output voltage may exceed the output voltage reference and result in malfunction of the PSI control when the converter starts up. To avoid the incorrect start-up transient, the PSI start-up mechanism shown in Figure 6 must be added.

De is the output of the digital error amplifier. De_z is the one-clock-delay signal of De. Signal error_De is the error between De and De_z. Whether error_De equals zero or not is the criterion for detecting the start-up condition. A four-bit counter is applied to ensure that the error_De remains zero and stays long enough to get ready for initiating the PSI mechanism.

3.4 Phase sequence determination

Phase sequence indicates power distribution priority for the phase loads. The signal sig_AB represents the triggering signal to distribute inductor energy to output nodes. When sig_AB is high (equals to 1), the inductor delivers energy to node A first, and then to node B. When sig_AB is low (equals to 0), it means that the inductor delivers energy to node B first, and then to node A. The logic flowchart of the phase sequence determination is shown in Figure 7. Sig_AB was set high by default. The status is dependent on the signal De_a and De_b, the output of the digital error amplifier. Signal ref_low indicates the lower band of the judge reference. When De_a is lower than ref_low, it means that phase A load is stepping-up, sig_AB is set low to activate the PSI. If De_b is lower than ref_low, it means phase B load is stepping-up and sig_AB is set to high. If both aforementioned conditions do not happen, sig_AB remains the same.
Feedback signal select

When PSI is activated, several control signals need to be rerouted. Figure 8 shows how the control signal is rearranged. The voltage error signals, $De_a$ and $De_b$, are transmitted to the corresponding compensator COMPA or COMPB according to Sig_AB. When Sig_AB is high, $De_a$ goes to COMPA, $De_b$ goes to COMPB. The duty cycle D from DPWM_a will be given to switch $S_3$, and its complement duty cycle 1-D will be given to switch $S_4$. The overall process will be opposite if Sig_AB is low.

Stability analysis

It is necessary to derive the small-signal model to portray the circuit characteristic in the frequency domain for assessing the stability of the whole circuit. The small signal analysis of the voltage-mode controlled SIDO buck converter in CCM is described as follows. To make the derivation clear, assumption of $D_1 = D_a$, $D_3 = D_b$, $D_4 = 1 - D_b$ is made to match the notations of Figure 4. The small-signal model of SIDO buck converter is shown in Figure 9, where $D_a$, $D_b$, and 1-$D_b$ are duty cycles of switches $S_1$, $S_3$, and $S_4$, respectively.

The voltage-mode controlled model of a SIDO buck converter is shown in Figure 10. All the referred transfer functions are shown in the appendix of Table A1. The SIDO buck converter has two output nodes. One output node is feedback into one compensator to generate the duty cycle $D_b$ to control the energy distribution. The other output node is feedback into the other compensator to decide duty cycle $D_a$ for the sake of total energy in need. $G_{com_a}(s)$ and $G_{com_b}(s)$ are the compensator transfer functions connecting the output voltage

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**FIGURE 7** Logic flowchart of the phase sequence determination

**FIGURE 8** Schematic of signal select implemented by FPGA

**FIGURE 9** Small signal equivalent circuit of the single-inductor dual-output buck converter

**FIGURE 10** Model of the voltage-mode single-inductor dual-output buck converter

| Component                  | Parameters |
|----------------------------|------------|
| $V_{in}$ (input voltage)   | 3.3 V      |
| $V_{out}/V_{ch}$ (output voltage) | 1.2 V/1.8 V |
| $I_{ss}/I_{ch}$ (load current) | 10–200 mA/10 mA |
| $f_w$ (switching frequency) | 1 MHz      |
| $C$ (output capacitance)   | 10 μF      |
| $H$ (inductance)           | 4.7 μH     |
and the control to output block in between to form a whole loop. There are three loops in the entire system:

\[
T_x = F_M \cdot G_{\text{comb}} \cdot G_{\text{dba}} \\
T_y = F_M \cdot G_{\text{comb}} \cdot G_{\text{dab}} \\
T_z = T_p \cdot T_Q = F_M^2 \cdot G_{\text{comb}} \cdot G_{\text{dab}} \cdot G_{\text{dbb}} \cdot G_{\text{dwa}}
\]

where \( F_M = \frac{1}{\omega_c} \) and \( V_{pp} \) is the amplitude of the ramp signal. The loop gains for output nodes:

\[
T_1 = T_x - \frac{T_z}{1 + T_y} \\
T_2 = T_y - \frac{T_z}{1 + T_x}
\]

Figure 10 shows that \( T_1 \) is the loop to control energy distribution to the output ports and \( T_2 \) is the loop to control the charging energy to the inductor. Generally, loop \( T_1 \) does not have conjugate poles to cause 180° phase shift that may impact the stability. Thus, a type II compensator is adequate. Regarding the loop \( T_2 \), the inductor and output capacitors generate conjugate poles which cause 180° phase shift. A type III compensator is needed to obtain sufficient phase margin. When PSI is implemented, light load conditions at both output ports need to be considered. The two zeros at low frequency are designated to eliminate the effect of conjugate poles. The transfer functions of the compensators are shown in Equations (7) and (8), respectively.

\[
G_c(s)_{\text{typeII}} = \frac{D_c(s)}{D_s(s)} = \frac{k_{\text{typeII}} \cdot \left(1 + \frac{s}{\omega_1}\right)}{s \cdot \left(1 + \frac{s}{\omega_p}\right)}
\]

\[
G_c(s)_{\text{typeIII}} = \frac{D_c(s)}{D_s(s)} = \frac{k_{\text{typeIII}} \cdot \left(1 + \frac{s}{\omega_1}\right) \cdot \left(1 + \frac{s}{\omega_2}\right)}{s \cdot \left(1 + \frac{s}{\omega_p}\right) \cdot \left(1 + \frac{s}{\omega_c}\right)}
\]

4 | IMPLEMENTATION OF THE PSI ON THE NON-COMPENSATOR-BASED SIDO BUCK CONVERTER

Figure 11 is the circuit diagram of a SIDO buck converter with the constant frequency ripple-based control. The inductor energy is controlled by MOSFETs denoted by \( S_p \) and \( S_o \), and the power distribution is controlled by MOSFETs denoted by \( S_1 \) and \( S_2 \). The switching control used in this architecture is the

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**FIGURE 11** Ripple-based single-inductor dual-output buck converter with constant frequency control
comparator combined with an AFT generator so as to achieve fast transient response and fixed switching frequency.

In the case of the SIDO buck converter, the off-time control is more intuitive as it is compared to the on-time control. Figure 12(a) shows that the inductor is charged until both \( V_{o1} \) and \( V_{o2} \) reach the required voltages at point 1 and point 2, then the off-time control is activated to discharge the inductor until voltage drops at point 3. On the other hand, the on-time control is shown in Figure 12(b). When the charging time (on-time control) of the inductor ends at point 5, \( V_{o2} \) may not reach the required voltage. This case usually happens when the phase 2 load is much heavier than the phase 1 load.

### 4.1 Operating principle of the off-time control

Due to the inherent parasitic resistances inside the power switch and the inductor, the constant off-time control would variate the switching frequency at different loading conditions. In order to fix the switching frequency, the off-time should be adaptively adjusted according to the on-time such that the overall switching period is fixed. As shown in Figure 11, the output voltages are controlled by the logic and an AFT generator to provide a complete switching cycle for \( S_p \) and \( S_o \) to charge or discharge the inductor. The detail design of the AFT can be referred to [19]. The operating principle is shown in Figure 13. When the inductor energy control switch \( S_p \) is turned on, the switch \( (S1) \) is turned on, the switch \( (S2) \) is turned off and the inductor current \( (I_L) \) rises. At this time, the inductor current flows through the output capacitor \( (C1) \), causing the phase 1 voltage \( (V_{o1}) \) to rise. When the voltage feedback signal \( (V_{ref1}) \) is greater than the phase 1 reference voltage signal \( (V_{ref2}) \), \( S1 \) is turned off and \( S2 \) is turned on, causing the phase 2 voltage \( (V_{o2}) \) to rise. When the voltage feedback signal \( (V_{ref2}) \) is greater than the phase 2 reference voltage signal \( (V_{ref2}) \), the switch \( S_p \) is turned off and \( S_o \) is turned on. At this time, the AFT starts to count the off-time for \( S_p \). During the off-time, the inductor current \( (I_L) \) decreases until the off-time ends. Following that, the switch \( S_p \) is turned on again to repeat the same operation process. Figure 13 shows that the energy (area \( E_{A1} \)) delivered to the phase 2 load is larger than the energy (area \( E_{A2} \)) delivered to the phase 1 load. In other words, the energy obtained at sequence of the latter is usually more than that of the former.

### 4.2 Voltage surge phenomenon

When the charging mode of the off-time control is used, one problem may happen when the phase 1 load is much heavier than the phase 2 load. The over-charged inductor would cause voltage surge at phase 2 load if the phase 2 load is arranged at the latter sequence of the energy distribution. The simulation waveform is shown in Figure 14.

To solve this problem, it is better to exchange the charging sequence between the phase 1 load and the phase 2 load. That is, the charging sequence always keeps the heavier phase load at the later order. Therefore, the PSI is the right choice to implement this idea. Figure 15 demonstrates that PSI has successfully prevented the voltage surge phenomenon from the case of Figure 14.

### 5 EXPERIMENTAL RESULT AND DISCUSSION

The control of the voltage mode SIDO buck converter was implemented by the TSMC0.18 \( \mu m \) manufacturing process. Before the buck converter was taped out, the functions of the PSI and voltage mode control were validated using the Altera DE2-70 FPGA. The schematic of the proposed circuit is depicted in Figure 16. To prevent the EMI noise induced by the large current in the power stage, the power stage and the
Signal wires need to be routed separately for isolation to be connected with the SMA headers. The components parameters are listed in Table 1, which is chosen in accordance with the tolerance of current, voltage and switching speed. The bandwidth and phase margin are designed according to the loop analysis to ensure a stable system.

**Figure 14** Voltage surge phenomena as phase 1 load current increased from 100 mA to 350 mA while phase 2 load current kept at 150 mA (V_{o1}, phase 1 voltage; V_{o2}, phase 2 voltage; I_L, inductor current)

**Figure 15** Phase sequence interchange was activated to exchange the energy distribution sequence as the phase 1 load current increased from 100 mA to 350 mA while the phase 2 load current was kept at 150 mA (V_{o1}, phase 1 voltage; V_{o2}, phase 2 voltage; I_L, inductor current)
the PSI signal turned from high to low. The transient cross regulation at the preceding phase ($V_{oa}$) was minor.

Table 2 shows the specification and cross regulation performance of the compensator-based SIDO buck converter. The definition of the performance index is the same as that was used in [20], that is, the performance index is defined as the voltage variation of the output voltage $b$ in response to the load current variation of the output current $a$. 

$$\xi_{a-b} = \frac{\Delta V_b}{I_a/\Delta I_a}$$

where $I_a$ is the rated load current and vice versa with $\xi_{b-a}$.

Based on the quantitative values calculated from the performance indices, the proposed PSI method provides comparable performances in cross regulation suppression. Although some performance indices provided from [8, 20] are less than those of the proposed work, their capacitances are 20× higher than that of this work. Compared with the similar specs of [13], the performance index of this work is less. Note that the proposed PSI control method does not change the original compensator design, which simplifies the circuit implementation compared to those of the counterparts.

The next test was conducted to verify the effectiveness of the PSI for mitigating the voltage surge in the ripple-based controlled SIDO. The circuit implementation was made according to the schematics in Figure 11. The testing scenario was to change the preceding phase load current ($I_{oa}$) in between 100 mA and 300 mA, when the latter phase load was kept at $I_{o2} = 200$ mA. Figure 19 shows when $I_{oa}$ stepped-up from 100 mA to 300 mA, the preceding phase current was already greater than the latter phase current $I_{o2}$ (200 mA). The
Table 2 Transient cross regulation comparison with the latest SIDO converter implementations

| Reference | [8] | [13] | [20] | This work |
|-----------|-----|------|------|-----------|
| Control method | MPVC | Multivariable | CCR | Voltage mode PSI |
| Input voltage | 20 V | 2.8–5 V | 10 V | 3.3 V |
| Output voltage | 8 V/12 V | 1 V/1.5 V | 3.3 V/5 V | 1.2 V/1.8 V |
| Switching frequency | 100 kHz | 500 kHz | 50 kHz | 1 MHz |
| Inductor value L | 100 μH | 5 μH | 100 μH | 10 μH |
| Capacitor value C | 100 μF | 10 μF | 470 μF | 4.7 μF |
| ∆Vb | 300 mV | 250 mV | 100 mV | 20 mV |
| ∆Va | 100 mV | 150 mV | 5 mV | 15 mV |

Performance index (cross)

\[ \xi_{\text{a-b}}, \xi_{\text{a-b}} = (\Delta V_a/V_a)/(\Delta I_a/I_a), \xi_{\text{a-b}} = (\Delta V_b/V_b)/(\Delta I_b/I_b) \] [20]

Note: Performance index (cross), \( \xi_{\text{a-b}} = (\Delta V_a/V_a)/(\Delta I_a/I_a) \) and \( \xi_{\text{a-b}} = (\Delta V_b/V_b)/(\Delta I_b/I_b) \) [20].

Abbreviation: SIDO, single-inductor dual-output.

Figure 19 Transient response of the output voltages and the inductor current when \( I_{o1} \) increased from 100 mA to 300 mA, but kept \( I_{o2} = 200 \) mA

PSI was enabled to exchange the charging phase sequence. When the \( V_{o2} \) was put at the preceding phase sequence, the \( V_{o2} \) did not have voltage surge at that moment. Figure 20 shows the other case when \( I_{o1} \) stepped-down from 300 mA to 100 mA. When \( I_{o1} = 100 \) mA, it was already smaller than \( I_{o2} = 200 \) mA. The PSI was enabled again. Therefore, we do not see the voltage surge at \( V_{o1} \).

In Figures 19 and 20, relatively high output voltage ripples can be found in the \( V_{o1} \) and \( V_{o2} \). The reason is that the ripple-based control needs to detect a ripple signal that should be in phase with the inductor current, and large enough to be stably compared with the voltage reference. One way to enlarge the feedback ripple signal is to increase the equivalent series resistance (\( R_{\text{ESR}} \)) of the output capacitor. The authors in [21] also stated that the \( R_{\text{ESR}} \) value should follow the rule of Equation (10) as shown below, such that the pulse bursting phenomenon does not happen.

\[ R_{\text{ESR}} C \geq T_{\text{on}}/2 \] (10)

where \( C \) is the output capacitance, \( T_{\text{on}} \) is the switching on period. Therefore, an electrolytic capacitor with high \( R_{\text{ESR}} \) is selected in this ripple-based control experiment. If one wants to reduce the large voltage ripple, using a smaller \( R_{\text{ESR}} \) capacitor, such as ceramic capacitor, is the most effective way. However, it might contradict Equation (10). To obtain the sawtooth signal that does not incur the pulse bursting phenomenon, several approaches such as using a differential circuit to feedback the capacitor output voltage [22] or acquiring the ripple part of the inductor current [23] are the solutions.
The PSI scheme also applies to the comparator type control. When the SIDO is operating in the ripple-based AFT control, the PSI mechanism avoids the voltage surge that may happen at the light load port. Table 3 shows that the proposed comparator controlled SIDO has the least load transient time compared to the other comparator controlled SIDO. The advantage of the ripple-based design is the prompt response of the non-linear control without bandwidth limitation, which speeds-up the load transient response.

### 6 CONCLUSION

The PSI scheme is proposed to suppress transient cross of a SIDO buck converter. The merit of the proposed scheme is its universal application to the comparator-based as well as the non-compassor-based controls. This study demonstrates the design flow of the compensator-based buck converter that is embedded with the PSI actuator. In addition, the rationale of using the PSI to avoid the transient voltage surge in the AFT mode ripple-based buck converter is explained in detail. The overall design concept was implemented to control the SIDO power stage. Both experimental results show that transient cross regulation is effectively suppressed by the proposed method and the performance is comparable to the other state of the arts.

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CONFLICT OF INTEREST
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REFERENCES
1. Tsai, C.H., Yang, C.H., Leng, C.W.: Design and implementation of a digitally controlled single-inductor dual-output (SIDO) buck converter. Int. J. Circuit Theory Appl. 42, 221–237 (2012)
2. Ma, D., et al.: Single-inductor multiple-output switching converters with time-multiplexing control in discontinuous conduction mode. IEEE J. Solid-State Circuits. 38(1), 89–100 (2003)
3. Kwon, D., Rincón-Mora, G.A.: Single-inductor multiple-output switching DC–DC converters. IEEE Trans. Circuits Syst. II Exp. Briefs. 56(8), 614–618 (2009)
4. Lee, A.T.L., Sin, J.K.O., Chan, P.C.H.: Scalability of quasi-hysteretic FSM-based digitally controlled single-inductor dual-string buck LED driver to multiple strings. IEEE Trans. Power Electron. 29(1), 501–513 (2014)
5. Ma, D., Ki, W.H., Tsui, C.Y.: A pseudo-CCM/DCM SIMO switching converter with freewheel switching. IEEE J. Solid-State Circuits. 38(6), 1007–1014 (2003)
6. Xu, W., et al.: A dual-mode single-inductor dual-output switching converter with small ripple. IEEE Trans. Power Electron. 25(3), 614–625 (2010)
7. Lin, K.Y., et al.: Modeling and design of feedback loops for a voltage-mode single-inductor dual-output buck converter. In: Proceedings of the IEEE PESC, pp. 3389–3395. Rhodes, Greece (2008)
8. Wang, B., et al.: Model predictive voltage control for single-inductor multiple-output DC–DC converter with reduced cross regulation. IEEE Trans. Ind. Electron. 63(7), 4187–4197 (2016)
9. Lee, Y.H., et al.: Interleaving energy-conservation mode (IECM) control in single-inductor dual-output (SIDO) step-down converters with 91% peak efficiency. IEEE J. Solid-State Circuits. 46(4), 904–915 (2011)
10. Chen, B.W., Chang-Chien, I.R.: Digitally controlled low cross-regulation single-inductor dual-output (SIDO) buck converter. In: Proceedings of the IEEE ISCAS, pp. 2497–2500. Lisbon, Portugal (2015)
11. Lee, Y.H., et al.: Minimized transient and steady-state cross regulation in 55-nm CMOS single-inductor dual-output (SIDO) step-down DC–DC converter. IEEE J. Solid-State Circuits. 46(11), 2488–2499 (2011)
12. Su, Y.P., et al.: CCM/GM relative skip energy control and bidirectional dynamic slope compensation in a single-inductor multiple-output DC–DC converter for wearable device power solution. IEEE Trans. Power Electron. 31(8), 5871–5884 (2016)
13. Dasika, J.D., et al.: Multivariable control of single-inductor dual-output buck converters. IEEE Trans. Power Electron. 29(4), 2061–2070 (2014)
14. Pizzutelli, A., Ghioni, M.: Novel control technique for single inductor multiple output converters operating in CCM with reduced cross regulation. In: Proceedings of the IEEE APEC, pp. 1502–1507. Austin, USA (2008)
15. Patra, P., Ghosh, J., Patra, A.: Control scheme for reduced cross-regulation in single-inductor multiple-output DC–DC converters. IEEE Trans. Ind. Electron. 60(11), 5095–5104 (2013)
16. Chen, G., et al.: Principle and topology synthesis of integrated single-input dual-output and dual-input single-output DC–DC converters. IEEE Trans. Ind. Electron. 65(5), 3815–3825 (2018)
17. Chen, G., et al.: Single coupled-inductor dual output soft-switching DC–DC converters with improved cross regulation and reduced components. IET Power Electron. 10(13), 1665–1678 (2017)
18. Shen, Z., et al.: Predictive digital current control of single-inductor multiple-output converters in CCM with low cross regulation. IEEE Trans. Power Electron. 27(4), 1917 (2012)
19. Ko, W.H., Chang-Chien, I.R.: Ripple-Based Control of Constant Frequency Single Inductor Dual Output (SIDO) Buck Converter. Masterthesis, National Cheng Kung University (2020)
20. Wang, Y., Xu, J., Yin, G.: Cross-regulation suppression and stability analysis of capacitor current ripple controlled SIDO/DCM buck converter. IEEE Trans. Ind. Electron. 66(3), 1770–1780 (2019)
21. Wang, J., Xu, J., Bao, B.: Analysis of pulse bursting phenomenon in constant-on-time-controlled buck converter. IEEE Trans. Ind. Electron. 58(12), 5406–5410 (2011)
22. Lee, Y.H., Wang, S.J., Chen, K.H.: Quadratic differential and integration technique in V2 control buck converter with small ESR capacitor. IEEE Trans. Power Electron. 25(4), 829–838 (2010)
23. Lee, S.H., et al.: 12.0A 0.518mm2 0.518mm2 0.518mm2 Multi-string buck LED driver to multiple output DC–DC converters. IEEE Trans. Ind. Electron. 59(5), 1007–1014 (2010)
24. Wu CH, Chen BW, Ko WH, Liu CW, Chang-Chien I.R.: Phase sequence interchange scheme for suppressing transient cross regulation on the compensator controlled and non-compensator controlled single-inductor dual-output buck converter. IET Circuits Devices Syst. 2021;1–13. https://doi.org/10.1049/ed2.12062

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TABLE A1 Transfer functions of Figure 10

\[
G_{vb} = \frac{\bar{v}_{ob}}{\bar{v}_{in}} = \frac{D_a(1 - D_b)R_{eqb}}{sL + r_L + D_b R_{eqa} + (1 - D_b)^2 R_{eqb}}
\]

\[
G_{da} = \frac{\bar{v}_{oa}}{d_a} = \frac{V_{in}D_b R_{eqa}}{sL + r_L + (1 - D_b)^2 R_{eqb} + D_b^2 R_{eqa}}
\]

\[
G_{da} = \frac{\bar{v}_{ob}}{d_a} = \frac{V_{in}(1 - D_b)R_{eqb}}{sL + r_L + D_b^2 R_{eqa} + (1 - D_b)^2 R_{eqb}}
\]

\[
G_{d_{ab}} = \frac{\bar{v}_{oa}}{d_b} = \frac{I_L R_{eqa} (1 - D_b) R_{eqb} + sL + r_L} {D_b R_{eqa} + (1 - D_b)^2 R_{eqb} + sL + r_L}
\]

\[
G_{d_{ab}} = \frac{\bar{v}_{ob}}{d_b} = \frac{V_{in}(1 - D_b)R_{eqb}}{sL + r_L + D_b^2 R_{eqa} + (1 - D_b)^2 R_{eqb}}
\]

\[
Z_{o1a} = \frac{\bar{i}_{oa}}{i_{o1}} = \frac{R_{eqb} [(1 - D_b)^2 R_{eqb} + sL + r_L]}{D_b R_{eqa} + (1 - D_b)^2 R_{eqb} + sL + r_L}
\]

\[
Z_{o2b} = \frac{\bar{i}_{ob}}{i_{o2}} = \frac{R_{eqa}(D_b^2 R_{eqa} + sL + r_L)}{D_b R_{eqa} + (1 - D_b)^2 R_{eqb} + sL + r_L}
\]

\[
Z_{o1b} = \frac{\bar{i}_{ob}}{i_{o1}} = \frac{-D_b(1 - D_b)R_{eqb}R_{eqb}}{D_b R_{eqa} + (1 - D_b)^2 R_{eqb} + sL + r_L}
\]

\[
Z_{o2a} = \frac{\bar{i}_{oa}}{i_{o2}} = \frac{-D_b(1 - D_b)R_{eqa}R_{eqb}}{D_b R_{eqa} + (1 - D_b)^2 R_{eqb} + sL + r_L}
\]