1. Introduction

Thin-film transistors (TFTs) with an oxide semiconductor channel, such as amorphous indium-gallium-zinc-oxide (a-IGZO), have attracted considerable attention as an alternative to amorphous silicon (a-Si) and low temperature polycrystalline silicon (LTPS) TFTs for high-resolution display technology. Although amorphous oxide semiconductors show considerably less threshold voltage ($V_{th}$) variation than poly-silicon, large-area processing and degradation effects can impede the characteristic parameters of a-IGZO TFTs, which manifests in an uneven brightness distribution across the display panel. Such $V_{th}$ variations are usually reduced by additional compensation circuits consisting of TFTs and capacitors. Herein, a new approach to compensate such variabilities is demonstrated: the integration of a programmable ferroelectric (FE) film in the gate stack of the TFT. This simplifies the complexity of the pixel cell and potentially minimizes the need for compensation circuits, which is crucial for transparent displays. To test this new approach, fully integrated FE-TFTs (i.e., with vias contacting a structured bottom gate electrode from the top) based on a-IGZO and FE hafnium-zirconium oxide (HZO) are developed. A single low-temperature post-fabrication treatment at 350 °C for 1 h in air is used to simultaneously crystallize the HZO film in the FE phase and to reduce the number of defects in the a-IGZO channel. The structural and electrical characterizations provide comprehensive guidance for the design of effective FE-TFT gate stacks and device geometries. An accurate control of the polarization state and linear switching between multiple intermediate states is shown by using programming pulses of various amplitudes and widths. Furthermore, a direct correlation between the channel length and the applied pulse width for programming is observed.
uneven brightness distribution across the display panel. In addition to intrinsic variabilities, aging of TFTs has to be taken into account, which, like degradation of organic light emitting diodes (OLEDs), causes further brightness deviations.

To compensate these fluctuations, elaborate compensation circuits have been suggested that require additional control signal lines, capacitors and transistors increasing the complexity and size or packing density of the pixel cell at the expense of resolution and/or transparency. Furthermore, for external compensation with driver ICs, additional elements for sensing and access to the driver TFT are needed within the pixel cell, besides increased effort for external sensing circuitry as well as data processing and storage capabilities.

Herein, a new approach to readjust and compensate device-to-device variabilities is suggested, namely the introduction of a programmable ferroelectric (FE) layer into the gate stack of the TFT. In the case of FE-TFTs, the polarization state of the FE layer is controlled by the polarity, amplitude, and width of a voltage pulse applied to the gate electrode. This polarization state controls accumulation or depletion of carriers in the semiconducting channel between the source and drain and can thus be used to compensate any deviations. This approach potentially simplifies the complexity of the pixel cell circuit and reduces the pixel size, which is important, for example, for transparent micro-displays.

FE-TFTs have been fabricated and discussed so far as artificial synapse, back end of line TFT, and non-volatile memory. For an effective compensation of the aforementioned device-to-device variabilities, an accurate control of the polarization state and analog/linear switching between multiple intermediate states is necessary. Although these requirements are very similar to the ones of analog synaptic devices that require analog weight updates, the devices reported in the literature use an unstructured bottom electrode as gate. Therefore, important device characteristics that depend on the geometry, for example the influence of the gate channel length on the programming characteristics, could not be addressed in detail. Herein, fully-integrated FE-TFT devices with optimized gate stack and various channel length were manufactured and characterized electrically as well as structurally.

The most widely studied FE materials are perovskites like lead zirconate titanate and barium titanate. Those require high film temperatures and the film composition: While HfO2-rich films are semi-crystalline after this thermal treatment (studied Hf-contents: x = 0.6). Consequently, the crystallization temperature increases with increasing HfO2 concentration. For films of 10 nm thickness, diffraction lines of the m-phase (cf. most pronounced diffraction line at 2θ = 28°) can be observed. In contrast, all 5 nm films (not shown in Figure 1) are amorphous after this thermal treatment (studied Hf-contents: x = 0.7 and x = 0.6). Consequently, the crystallization temperature increases with declining film thickness. This effect is well known and attributed to the increased surface to volume ratio of films having a thickness of only a few nm.

Under identical annealing conditions (isothermal and isochronal) the fraction of the monoclinic (m)-phase increases significantly with the film thickness and the amount of HfO2 (Figure 1). In the case of the 7 nm films, no diffraction lines attributed to the m-phase can be observed. For films of 10 nm thickness, diffraction lines of the m-phase (cf. most pronounced diffraction line at 2θ = 28° in Figure 1) appear for the film with the highest content of HfO2 (x = 0.7). For a thickness of 15 and 20 nm, also films with lower content of HfO2 (x < 0.7) exhibit diffraction lines of the m-phase.

### 2. Results and Discussion

The crystallinity of Hf,Zr1−xO2 films with different compositions was determined by GIXRD (Figure 1). The thermal budget of 350 °C for 1 h is sufficient to crystallize all tested films with a thickness of 10 nm and above. In the case of 7 nm films, a clear dependence can be observed between the crystallization temperature and the film composition: While HfO2-rich films have a large fraction of the amorphous phase, ZrO2-rich films are rather crystalline. Therefore, it can be deduced that the crystallization temperature increases with increasing HfO2 concentration. In contrast, all 5 nm films (not shown in Figure 1) are amorphous after this thermal treatment (studied Hf-contents: x = 0.7 and x = 0.6). Consequently, the crystallization temperature increases with declining film thickness. This effect is well known and attributed to the increased surface to volume ratio of films having a thickness of only a few nm.

In order to realize integrated FE-TFTs, it is highly desired to use one single post-fabrication heat treatment to simultaneously crystallize the HZO film in the FE phase and to reduce the number of point defects within the a-IGZO semiconductor. The latter requires temperatures not exceeding 300–350 °C to achieve the best results with respect to carrier mobility, current on-off ratio, and low Vth demands. In addition, a thermal treatment at such comparatively low temperatures is fully compatible to flexible- and glass substrates and minimizes the risk for inter-diffusion processes of metallic species at the interfaces between the a-IGZO channel and the metallic source and drain contacts, which are known to result in deteriorated TFT performance. Consequently, the maximum temperature to functionalize the HZO film is limited to 350 °C in the present processing scheme. Therefore, tailoring the HZO film to meet the thermal budget limitations defined by a-IGZO is highly desirable. This gives the possibility to integrate all necessary thermal treatments of the FE-TFT stack in one single step.

Herein, metal-ferroelectric-metal (MFM) capacitors are utilized to optimize HZO films (thickness and doping concentrations) with respect to the thermal budget of the TFT technology. In a second step, the most promising HZO films were integrated with the IGZO into metal-semiconductor-ferroelectric-metal (MSFM) structures. These test structures were used to find optimal thickness ratios of the semiconductor and FE, which give a good access to the FE material by the external electrical field. Finally, fully-integrated FE-TFT devices with the optimized gate stack and various channel length were manufactured and characterized.

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Figure 1. GIXRD pattern of metal-ferroelectric (FE)-metal (MFM) stacks annealed in a furnace-type oven at 350 °C for 1 h. The thicknesses of the FE Hf$\_x$Zr$_{1-x}$O$_2$ films is 7, 10, 15, and 20 nm. For each thickness, the following compositions were used: Hf$_{0.3}$Zr$_{0.7}$O$_2$ (blue pattern), Hf$_{0.5}$Zr$_{0.5}$O$_2$ (green pattern), Hf$_{0.6}$Zr$_{0.4}$O$_2$ (red pattern), and Hf$_{0.7}$Zr$_{0.3}$O$_2$ (black pattern). At the bottom of the figure, the positions of the diffraction lines of individual HfO$_2$ phases are shown. In addition, the positions of the TiN diffraction lines are added by dashed vertical lines. For the sake of clarity, only the low-angle parts of the XRD patterns are displayed.

Since the cubic (c), tetragonal (t), and orthorhombic (o) phases have reflection lines at similar 2θ angles, it is not straightforward to distinguish between these phases solely from the XRD pattern. Therefore, and to get a proper understanding of the ferroelectric film-properties, additional P–E-measurements were conducted (Figure 2).

All Hf$_x$Zr$_{1-x}$O$_2$ films of 5 nm thickness show linear (i.e., dielectric) P–E-characteristics in virgin state and after 10$^5$ wake-up cycles (data not shown). This is in good agreement with the amorphous nature of these films. Thicker films have nonlinear P–E-characteristics before and after wake-up cycling. Films with a surplus of ZrO$_2$ ($x = 0.3$) depict anti-ferroelectric (AFE)-like behavior in the virgin state (Figure 2). With increasing film thickness from 7 to 20 nm and increasing HfO$_2$ content the AFE behavior gradually decreases. It may therefore be concluded that ZrO$_2$ rich films of 10 nm and below crystallize preferentially in the AFE-like t-phase during annealing, whereas in the case of thicker films (15 and 20 nm) and/or HfO$_2$ rich films the FE o-phase and the paraelectric m-phase gradually replace the AFE-like t-phase. For pure ZrO$_2$ films it is well known that the t-phase is energetically preferred at small film thicknesses due to the surface energy effect.[43] Nevertheless, the AFE-like behavior can also be attributed to AFE-like domains present in the o-phase.[42]

During wake-up, the AFE-like behavior vanishes gradually with the number of field cycles (data not shown). After 10$^5$ cycles the FE hysteresis is fully developed. This can be explained either by an initial field induced phase transformation from a t-rich-state to an o-rich-state[43] with a subsequent stabilization of the o-phase and/or by ferroelastic switching of prior AFE-like domains of the o-phase.[42] Compared to the other studied stoichiometries, films with surplus of ZrO$_2$ have the highest fraction of AFE-like phases in the pristine state. As a consequence, the effect of wake-up cycling on the shape of the P–E-characteristics is the strongest for the films with $x = 0.3$.

Films with a ZrO$_2$ to HfO$_2$ ratio of 1:1 ($x = 0.5$) depict a partial AFE-like behavior in the virgin state only at 10 nm film thickness. With increasing film thickness, the AFE-like behavior (i.e., the t-phase and/or the non- FE domains of the o-phase) vanishes gradually. In case of the 10 nm film, wake-up cycling has a strong impact on the shape of the P–E-characteristics. For films thicker than 10 nm, the impact of the wake-up is rather small, due to the increased fraction of the paraelectric m-phase, which cannot be transferred to the o-phase via field cycling.[44]

Films with excess HfO$_2$ ($x > 0.5$) do not depict AFE-like characteristics in the virgin state, even at a small thickness of 10 nm. It can thus be deduced that the amount of the t-phase and/or the amount of AFE-like domains within the o-phase is small. Since the remanent polarization is comparatively small for HfO$_2$ rich films and further decreases with increasing HfO$_2$ content between 0.3 ≤ $x ≤ 0.5$, the fraction of the paraelectric m-phase seems to scale with the amount of HfO$_2$. As shown in the diffraction pattern in Figure 1, the fraction of the m-phase also increases as the film thickness grows. This is in good agreement with the decreasing remanent polarization observed with increasing film thickness, which is seen especially in case of the HfO$_2$ rich films in Figure 2.

Another important parameter of the Hf$_x$Zr$_{1-x}$O$_2$ films is the leakage current, which leads to a “cigar-like” hysteresis loop and, therefore, can be estimated qualitatively from the shape of the P–E-characteristic.[45] In particular after wake-up cycling (blue lines in Figure 2), a clear trend is visible: at the same field, the leakage increases with the film thickness and the ZrO$_2$ content. In addition, the breakdown field decreases with the film thickness (not shown here). For this reason, a maximum field of 2.6 MV cm$^{-1}$ was applied to measure the P–E characteristics for the 20 nm film, whereas, for all other films, a maximum field of 3.0 MV cm$^{-1}$ was used. Such a thickness-dependent film degradation was also observed for Hf$_{0.3}$Zr$_{0.7}$O$_2$ films before.[34] Reasons could be that thicker films have a lower proportion of the amorphous phase and/or consist of larger crystallites. Both
would facilitate the diffusion/field drift of the charge carriers along grain boundaries leading to increased leakage and dielectric breakdown. The composition dependent leakage increase can be explained by the weaker leakage characteristics of ZrO$_2$ as compared to HfO$_2$.[46]

The remanent polarization depends strongly on the film composition (Figure 3). In the case of 10 nm, the remanent polarization increases for increasing ZrO$_2$ content until $x = 0.5$ and decreases upon further increase. This dependence on composition can be attributed to the partial formation of the m-phase for HfO$_2$ rich films and to the partial formation of the t-phase and/or AFE-like o-domains for ZrO$_2$ rich films (Figures 2 and 3). Thus, the highest remanent polarization of about 20 $\mu$C cm$^{-2}$ is measured for $x = 0.5$, which is in good agreement with previous work using RTP annealing at high temperatures.[30]

Consequently, to achieve the largest share of FE domains (i.e., the highest remanent polarization), a HfO$_2$ to ZrO$_2$ ratio...
of 1:1 and a layer thickness of 10 nm is most promising for the annealing conditions used in the a-IGZO TFT technology. Therefore, the following investigations focus on the integration of the 10 nm Hf$_{0.5}$Zr$_{0.5}$O$_2$ film into a-IGZO TFT technology and the electrical characterization of corresponding FE-TFTs.

The interfaces between the Hf$_{0.5}$Zr$_{0.5}$O$_2$ (HZO) and the surrounding materials are of high importance for the stabilization of the FE phase. Different interface materials have been investigated, whereas the largest polarization could be observed for TiN. For this reason, the FE-TFTs studied here use a TiN bottom gate contacting the HZO. However, since also the top interface to the a-IGZO layer could negatively impact the polarizability of the FE film, an Al$_2$O$_3$ capping layer was placed in between the HZO and the oxide semiconductor. MFM test structures using this TiN/HZO/Al$_2$O$_3$/TiN stack show promising $P$–$E$ characteristics (Figure 4a). Nevertheless, in comparison with classic TiN/HZO/TiN stacks, they have rather asymmetric $P$–$E$ hysteresis loops, higher coercive voltage, and lower maximum remanent polarization values (Figure 4b). The first point can be explained by the asymmetric field distribution across the stack in the case of different interface layers surrounding the HZO.

For the targeted applications, the FE-TFTs must show FE plasticity (stable, partially switched polarization states) for programming at sub-coercive voltage conditions. The existence of these multi-state sub-loops has been directly observed for $P$–$E$ measurements of MFM test structures (Figure 4b). They are well controllable and range from approximately zero remanent polarization to the full loop. In addition to the targeted applications, this functionality is particularly important for ultra-dense memory applications and as multi-state weight cell or analogue synapses in neural network accelerators.

Figure 5 summarizes the $P$–$V$ and capacitance versus voltage ($C$–$V$) measurements for MSFM structures with a FE layer and a semiconductor layer of different thicknesses $t_{HZO}$ and $t_{IGZO}$. If the semiconductor is three times, that is, significantly thicker than the thickness of the ferroelectric, no wake-up effect is visible (cf. wake-up behavior in Figure 5a). Although the initial $P$–$V$ measurement yields a distinctly pronounced but strongly asymmetric hysteresis, the size of the hysteresis loop (memory window) decreases with each field cycle until it eventually disappears. The asymmetric hysteresis appears again, but only for the first few field cycles, if the voltage range is increased (subloop behavior in Figure 5b). A gradual voltage increase leads to a gradual increase of the negative remanent polarization ($P_{r-}$) and the positive coercive voltage ($+V_{c}$) (i.e., the asymmetric characteristics become more pronounced). The $C$–$V$ curves have similar characteristics like one would expect for non FE metal-insulator-semiconductor (MIS)-structures (Figure 5c). For small voltage ranges ($\leq \pm 3$ V), no difference between the forward and the backward sweep was seen. It thus can be concluded that the coercive field is not reached and charge-trapping is a weak mechanism. For larger voltage ranges ($\geq \pm 4$ V), a shift of the flatband voltage to the left and thus a
memory window (MW) of 0.7 V can be observed during the forward sweep (from 4 to −4 V). This can be explained by the FE switching of the HZO, which occurs at \(+V_c\). However, the shift cannot be reversed by the return sweep (−4 to 4 V). Also larger voltage ranges (±5 V) do not reverse the shift, since the dielectric breakdown occurs before the back switching. This means that once the FE material is programmed, it cannot be erased. This and the asymmetric hysteresis loops can be explained by the field distribution across the stack: due to the rather large thickness of the semiconductor, a larger fraction of the applied voltage drops across the semiconductor. If a negative window is applied to the gate (erase), this fraction is even larger due to the depletion zone formed in the IGZO. Thus, the coercive field to reverse (erase) the FE state of the HZO is not reached. In the case of a positive voltage (program), the semiconductor is in accumulation. Consequently, the fraction of the voltage dropping across the semiconductor is smaller and the field of the HZO is large enough to cause FE switching.

If the semiconductor and the FE have the same thickness (\(t_{\text{HZO}} = t_{\text{IGZO}}\)), a higher amount of the applied voltage drops across the FE (compared to the case of \(t_{\text{IGZO}} > t_{\text{HZO}}\)). The \(P–V\) measurements show small hysteresis loops with a weak wake-up effect (Figure 5d). Since the coercive field of the FE is close to the breakdown field of the stack, the dielectric breakdown occurs at a low number of field cycles. A distinct sub-loop behavior is not observed for increasing voltage ranges (Figure 5e). The characteristics of the \(C–V\) measurements are still similar to the characteristics expected for non FE MIS structures. However, a FE switching with a memory window of about 1.1 V can be observed between the forward sweep (measured from 4 to −4 V) and the backward sweep (measured from −4 to 4 V; Figure 5f). Although programming and erasing is possible for this stack, the field distribution is still not optimal.

If the FE material is thicker than the semiconductor (i.e., \(t_{\text{HZO}} > t_{\text{IGZO}}\)), an even higher fraction of the applied voltage drops over the HZO. The \(P–V\) characteristics are symmetric and the wake-up effect is more pronounced (Figure 5g). Also, the sub-loop behavior, observed for gradually increased voltage ranges, is promising (Figure 5h). The \(C–V\) curves show typical MFM characteristics with two maxima and a large memory window of about 1.8 V (Figure 5i).

The most promising results have been observed if the FE is significantly thicker than the semiconductor (\(t_{\text{HZO}} = 3\ t_{\text{IGZO}}\)). Corresponding structures show large, very symmetric \(P–V\) hysteresis loops with typical wake-up characteristics (Figure 5j) and promising sub-loop behavior (Figure 5k). Accordingly, FE-TFTs with appropriately optimized gate stacks are expected to have the best electrical properties.

A schematic drawing of our devices is illustrated in Figure 6a. FE-TFTs with various channel lengths (at a constant channel width of 50 μm) and IGZO thicknesses have been fabricated (Figure 6b). It is important to mention that the samples receive only a single annealing step at 350 °C for 1 h after the entire device has been formed. The cross sectional transmission electron microscope (TEM) image of the gate stack shows that the HZO is fully crystalline and the IGZO remains amorphous after applying the annealing scheme (Figure 6b). In addition, all layers are uniformly formed and the thin Al₂O₃ capping prevents inter-diffusion processes between the HZO and IGZO.

Figure 7a shows the transfer characteristics of typical FE-TFTs with different IGZO thicknesses. To prevent programming during the measurement, the sweep range of the gate voltage was limited to ±1 V. The IGZO thickness clearly influences the saturated drain current and the initial \(V_{\text{th}}\): with increasing IGZO thickness, the saturated drain current increases and both the initial \(V_{\text{th}}\) and the on voltage decrease (Figure 7b). The first observation can be attributed to the degradation of the charge carrier mobility for ultra-thin channel films due to the detrimental impact of the non-passivated and thus highly sensitive back channel interface on the semiconductor film.

Furthermore, the current on-off ratios depend on the IGZO thickness: a large ratio of 10⁶ (limited by the resolution of the
measurement equipment) was measured for 30 nm and a rather small ratio of $10^3$ for 5 nm.

Figure 8 shows the transfer characteristics of FE-TFTs after programming. Therefore, a programming pulse of a certain amplitude and width was applied to the gate contact while keeping the potential of the source and drain contacts at ground. Programming can be realized by increasing either the pulse amplitude (Figure 8a) and/or the pulse width (Figure 8b). The gradually increasing shift of $V_{th}$ to negative values is due to the gradually increasing remanent polarization ($P_r$) of the FE material as the amplitude and/or the width of the programming pulse increase. The distance between $V_{th}$ in pristine state and the maximum shifted $V_{th}$ reveals a maximum memory window of about 1 V if programming occurs via pulse-amplitude variation and about 0.5 V if programming occurs via pulse-width variation. The intermediate states in between the initial $V_{th}$ and maximum shifted $V_{th}$ can be controlled precisely.

The FE shifting in Figure 8 shows only weak deterioration of both the field-effect mobility (+3.4 %) and the subthreshold slope (from 65.3 mV dec$^{-1}$ until 103 mV dec$^{-1}$) in the case of increasing amplitudes at constant pulse width, whereas in the case of fixed amplitude and increasing pulse width the mobility decreases by 19% at slightly increasing subthreshold slope. The degeneration of subthreshold behavior, especially seen for extensive programming, points toward defect generation at the semiconductor-to-insulator interface. The contradictory development of the field effect mobilities in fixed-pulse width versus fixed-amplitude programming suggest a joint consideration of both mechanisms for a balanced optimization of programming without mobility alteration.

Figure 9 illustrate the influence of the device geometry (i.e., the gate channel length and IGZO film thickness) on the programming characteristics. The pulse width (i.e., the programming time) needed to shift $V_{th}$ by a certain level increases if the channel length increases and/or the IGZO thickness decreases.

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**Figure 5.** Polarization versus voltage (P–V) and capacitance versus voltage (C–V) measurements of metal-semiconductor-FE-metal (MSFM) gate stacks with various thicknesses of the FE and semiconductor layer (see schematic drawings). The P–V characteristics in the left and central column display the wake-up and sub-loop behavior, respectively. The C–V characteristics in the right column show the formation of a memory window (MW) due to the shift of the flatband voltage caused by the polarization switching of the FE.
Figure 6. Overview of our FE-TFTs. a) A schematic drawing of a typical fully-integrated device. b) Light microscopic top-view-images of FE-TFTs. The channel lengths decreases from 100 µm (top) to 3 µm (bottom). The width of the channel (50 µm) is constant. Source (S), drain (D), and gate (G) are contacted from the top. The cross-sectional transmission electron microscope (TEM) image provides a detailed view of the channel region. All devices received one post-fabrication temperature treatment at 350 °C for 1 h in air.

Figure 7. a) Transfer characteristics of not programmed FE-TFTs with various IGZO thicknesses and a channel length of 20 µm. The gate voltage was swept over a small range of ±1 V to prevent a programming. b) the drain current (extracted at $V_G = 1$ V) and the threshold voltage (extracted at $I_D = 10^{-9}$ A) are plotted as a function of the IGZO thickness.

Figure 8. Transfer characteristics of FE-TFTs (IGZO-thickness: 30 nm; HZO-thickness: 10 nm; channel length: 20 µm). Partial switching can be observed after applying a) a voltage pulse of increasing amplitude and constant width (200 ns) or b) a voltage pulse of increasing width and constant amplitude (5.5 V) to the gate contact. During readout, the gate voltage was swept within a small range of ±1 V to prevent programming.
(cf. Figure 9a,b). In order to program the device, the voltage applied to the gate contact must be effectively coupled to the HZO. Since the device does not have an additional top-gate contact, an accumulation layer must be formed in the semiconductor to couple the external field efficiently into the HZO. As a consequence, charge carriers (electrons in the case of programming) must drift to the interface IGZO/HZO. The duration of this process depends strongly on the device geometry. If the channel is longer, a higher number of electrons must drift over a longer distance to accumulate. In the case of an ultra-thin (i.e., 5 nm) IGZO body (Figure 9b), the mobility of the electrons is decreased due to the quantum size effect and the overall number of electrons in the semiconductor is reduced. In both cases, longer programming times are needed to form an accumulation layer.

Retention measurements after programming to different intermediate states show promising long time stability (Figure 10). During the measurement duration of 2 h, no significant shift of $V_{th}$ was observed. Extrapolation to 10 years reveals a polarization loss of about 20%.

Over all, the programming approach can compensate positive $V_{th}$ shifts typically observed in OLED driver TFTs under drain current stress, the typical operation regime. Accessing the drain and source contacts of the driver TFT by proper external biasing, if required by adding few components to the pixel circuit, and the gate via the data programming line enables programming access to the driver gate. The typical negative $V_{th}$ correction can be sensed by the driver IC as executed in common external compensation routes.[15,16] In contrast there is reduced need for external data storage or processing, as the compensation information is stored permanently in the driver TFT.

Erasing on the programmed $V_{th}$ states is investigated by applying a negative pulse to the bottom gate while keeping the potential of the source and drain contacts constant at ground level. Various pulse-widths (up to several seconds), pulse-amplitudes and device-geometries were tested, but an erase was not possible. Further ideas like elevated chuck temperatures, illumination with UV-light, and applying an additional electric field between source and drain to form a conductive channel were reviewed but did not improve the capability to erase the FE-TFTs. However, if the HZO is significantly thicker than the IGZO and $P–V$-characteristics are measured only between gate and source or gate and drain in a capacitor-like approach, switching in both directions is possible directly underneath the source and drain regions (Figure 11). This observation is in good agreement with the results obtained for the MSFM structures in Figure 5 and proofs that the voltage divider is not the reason for the limited erasure capability. A potential explanation for the impossible erasure is the absence of an inversion layer in the semiconductor when a negative potential is applied to the gate. The large band gap of a-IGZO which is typically about 3.4 eV hinders the strong inversion.

From the geometry-dependent programming time in Figure 9, one can conclude that the presence of an accumulation layer is a basic requirement to program the FE-TFTs. Without additional top-gate contact, the accumulation layer acts similarly like a top-gate and supports the efficient application of the electric field to the HZO. Since the mobility of the electrons ($\approx 10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) is comparatively high the accumulation layer is formed within a short time of about 100 ns to 100 μs depending on the device geometry (Figure 9). In contrast, the hole-mobility is significantly lower. Consequently, an
performance. All devices could be programmed by applying a positive pulse to the gate and having source and drain connected to ground. The programming time to shift \( V_{th} \) increases if the channel length increases and/or the IGZO thickness decreases. This result was attributed to the formation of an accumulation layer in the semiconductor, which is a prerequisite to efficiently apply the electric field to the HZO. Programming to intermediate states was realized precisely by using pulses of certain amplitude and width. The intermediate states showed promising retention characteristics with a polarization loss of 20% extrapolated for 10 years. For erasing, a negative pulse was applied to the bottom gate while keeping the potential applied to source and drain constant at ground. Various pulse widths (up to several seconds), pulse amplitudes and device geometries were tested, but an erasure was not possible. This was explained by the significantly lower mobility of the holes in the semiconductor, which prevents the formation of an inversion layer. Thus, the electric field cannot be efficiently applied to the HZO. However, directly underneath the source and drain, the programmed state could be erased. The use of an additional top-gate electrode could thus be promising to enable also an erasure of the channel region. FE-TFTs are expected to deliver a simple means to compensate positive \( V_{th} \) shifts in stressed display driver TFTs at minimum need for excess in-pixel components, sensing effort on the order of typical external compensation schemes and relaxed requirements for external data processing and storage.

4. Experimental Section

MFM and MSFM capacitors were fabricated on highly-boron doped 300 mm silicon wafers in CMOS compatible industry standard production tools. The TiN bottom electrode was deposited via atomic layer deposition (ALD) employing TiCl4 and NH3 precursors. The FE Hf\(_{0.7}Zr_{0.3}O_2\) layers were deposited at 300 °C by ALD. As precursors, HfCl4 and ZrCl4 were used together with \( \text{H}_2\text{O} \) as oxidizing reactant and Ar as purging gas. Different stoichiometries (ranging from \( \text{Hf}_{0.3}\text{Zr}_{0.7}O_2 \) to \( \text{Hf}_{0.5}\text{Zr}_{0.5}O_2 \)) were achieved by using various precursor cycling ratios. The film thickness, adjusted by the number of total deposition cycles, was varied between 5 and 20 nm and confirmed by spectroscopic ellipsometry. In case of the MSFM capacitors, the IGZO was deposited by RF magnetron sputtering from a ceramic target (In:Ga:Zn=1:1:3) with an argon to oxygen ratio of 33.3:1 and a working pressure of 1 mbar. The thickness of the oxide semiconductor was varied between 5 and 30 nm. Prior to semiconductor deposition, 2 nm of Al2O3 deposited by ALD using trimethyl aluminum and H2O were used to introduce an intermediate layer between \( \text{Hf}_{0.5}\text{Zr}_{0.5}O_2 \) and IGZO. The TiN top electrode was fabricated by magnetron sputtering at temperatures below 100 °C to avoid in-situ crystallization of the \( \text{Hf}_{0.5}\text{Zr}_{0.5}O_2 \) layers. The crystallization anneal was carried out at 350 °C in \( \text{N}_2 \) atmosphere within a furnace-type oven for 1 h to simulate the maximum thermal budget of the TFT process. Therefore, the wafers were introduced into a preheated chamber and pulled out after processing.

For the electrical characterization, Ti/Pt dots were patterned by applying shadow mask and electron beam evaporation. Subsequently, the TiN and optionally the IGZO layers between the dot-contacts were removed by wet etching using SC1 and diluted HCl to form individual MFM or MSFM capacitors.

The polarization versus field (P–E) measurements were performed with an Aixacct TF 3000 FE analyzer using a triangular waveform at a frequency of 1 kHz. Structural characteristics of the crystalline phases were concluded from X-ray powder diffraction experiments in a grazing incidence diffraction geometry (GIXRD) with a thin-film diffractometer. To avoid the Si 311 substrate reflection, all samples were mounted with

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**Figure 11.** I–V characteristics measured for FE-TFTs wired like a capacitor (i.e., the voltage for programming and erasing is applied to the gate contact, the source is grounded, the drain is floating). The occurrence of displacement current peaks in the first programming and erasing loop, respectively indicate a switching of the FE material in both directions. However, underneath the source and drain area the electric field cannot be efficiently applied to the HZO. Thus, directly underneath the source and drain, the programmed state could be erased. The use of an additional top-gate electrode could thus be promising to enable also an erasure of the channel region. FE-TFTs are expected to deliver a simple means to compensate positive \( V_{th} \) shifts in stressed display driver TFTs at minimum need for excess in-pixel components, sensing effort on the order of typical external compensation schemes and relaxed requirements for external data processing and storage.

3. Conclusion

All important steps necessary to develop fully-integrated FE-TFTs based on a-IGZO and FE Hf\(_x\)Zr\(_{1-x}\)O\(_2\) have been outlined. In a first step, the Hf\(_{0.5}\)Zr\(_{0.5}\)O\(_2\) film was optimized in a way that film crystallization within the FE phase is possible by using a single heating step at 350 °C for 1 h in conjunction with IGZO defect and contact annealing after the entire device has been formed. This low thermal budget prevents crystallization of the a-IGZO as well as a degradation of the channel by the source and drain metal contacts. In a second step, capacitor structures were used to test the integration of the most promising FE Hf\(_{0.5}\)Zr\(_{0.5}\)O\(_2\) film (Hf\(_{0.5}\)Zr\(_{0.5}\)O\(_2\), HZO) together with the a-IGZO in the gate stack. Due to the voltage divider, the HZO film must be significantly thicker than the IGZO to enable switching in both directions. Corresponding test structures show large and symmetric P–V hysteresis loops with promising sub-loop behavior. Based on these results, fully-integrated FE-TFTs with various channel lengths and IGZO thicknesses have been fabricated to investigate the influence of the device geometry on the writing
a 45° rotation between the [001] direction of the (100)-oriented silicon wafer and the diffusion plane.

The FE-TFTs were fabricated on silicon wafers covered by 100 nm SiO₂ to insulate the devices from the substrate. 50 nm of TiN was deposited by ALD and patterned via e-beam lithography and reactive ion etching to form bottom gate electrodes. As FE gate insulator, Hf₀.₅Zr₀.₅O₂ (HZO) of 10 nm thickness was deposited by ALD and covered by 2 nm ALD Al₂O₃. The IGZO channel layer being 5 to 30 nm in thickness was deposited by magnetron sputtering. The source and drain contacts consisting of Ti/Al/Ti stacks were deposited by electron-beam evaporation and patterned by lift-off technique. The contact opening to the bottom gate was achieved by using a dry etching process. Finally, the devices were annealed in air at a temperature of 350 °C for a duration of 1 h.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Research data are not shared.

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analog switching, ferroelectrics, hafnium zirconium oxide, thin-film transistors, threshold voltage variation, transparent displays, neuromorphic computing

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