Switched-On: Progress, Challenges, and Opportunities in Metal Halide Perovskite Transistors

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Field-effect transistors (FETs) are key elements in modern electronics and hence are attracting immense scientific and commercial attention. The recent emergence of metal halide perovskite materials and their tremendous success in the field of photovoltaics have triggered the exploration of their application in other (opto)electronic devices, including FETs and phototransistors. In this review, the current status of the field is discussed, the challenges are highlighted, and an outlook for the future perspectives of perovskite FETs is provided. First, attention is drawn to the device physics and the fundamental processes that influence these devices, including the role of ion migration and defects, effects of temperature, light, and measurement conditions. Next, the performance of perovskite transistors and phototransistors reported to date are surveyed and critically assessed. Finally, the key challenges that impede perovskite transistor progress are outlined and discussed. The insights gained from the study of other perovskite optoelectronic devices may be adopted to address these challenges and advance this exciting field of research closer to the industrial application are examined.

1. Introduction

Metal halide perovskites are a remarkable class of materials: they exhibit exceptional properties like high luminescence efficiency and low degree of energetic disorder, comparable to those of highly crystalline inorganic semiconductors like GaAs, but can be processed at a fraction of the cost by facile solution coating. Other favorable properties include high absorption coefficients,[2] low exciton binding energy[3] and high diffusion lengths.[4] The combination of these properties makes perovskite materials highly attractive for application in a wide range of optoelectronic devices, such as photovoltaic and light-emitting diodes, photonic devices and lasers, and potentially transistors and phototransistors.

The progress made in the field of perovskite photovoltaic devices is particularly impressive: since their first introduction in 2009,[5] the power conversion efficiency increased nearly six-fold, surpassing 25% at the time of writing.[6] Theoretical calculations predict that efficiencies up to 30% could be reached with further device optimization, making perovskite solar cells very promising among third-generation photovoltaic devices.[7] Similarly, significant advances have been made in the field of perovskite light-emitting diodes (LEDs) since their first demonstration in 2014:[8] the external quantum efficiency of perovskite LEDs has increased by an order of magnitude in only a few years, surpassing 20%.[9]

Lagging behind in both performance and reliability are the perovskite field-effect transistors (FETs),[10–16] with a significantly smaller number of reports describing the application of perovskite semiconductors in FETs in comparison to a large body of literature on perovskite solar cells or LEDs, in spite of the fact that the first manuscript on perovskite FETs preceded all reports on other applications.[12] Nevertheless, the high predicted charge carrier mobility and the ease of processing using scalable, cost-efficient manufacturing techniques, as demonstrated for large area solar cell modules[18] and other applications,[19] motivate and sustain the research on perovskite FETs. For example, ab initio calculations performed on methylammonium lead iodide (MAPbI3) predict charge carrier mobilities surpassing $\mu = 1000$ cm$^2$ V$^{-1}$ s$^{-1}$.[20,21] The origin of this high mobility is the low effective charge carrier mass ($m^*$), with theoretical[22] and experimental[23] results reporting both electron and hole $m^*$ to be $\approx 0.1m_0$, where $m_0$ is the free electron free mass. Supporting these theoretical predictions are optical-pump-terahertz-probe photoconductivity spectroscopy measurements that determined the free charge carrier mobility in a MAPbI3 single crystals to be in the range of 500 to 800 cm$^2$ V$^{-1}$ s$^{-1}$.[24–26] Despite these expectations, the performance of perovskite FETs reported to date is disappointingly low: mobility values vary from $10^{-3}$ cm$^2$ V$^{-1}$ s$^{-1}$ in non-optimized thin films to $\approx 50$ cm$^2$ V$^{-1}$ s$^{-1}$ in high quality...
single crystals.\textsuperscript{10,15,16,27–33} The analysis of these devices is complicated by ion migration,\textsuperscript{34} which screens the applied voltages and by charge carrier scattering at the interface with the dielectric layer. The obvious question to pose is whether perovskite FETs are indeed serious contenders for thin film electronic circuits that could potentially be integrated with the other types of perovskite optoelectronic devices, or is this an application that perovskites cannot address at competitive levels? To address this question, in this review, we survey the current progress made in the field of perovskite transistors and phototransistors, focusing on understanding the mechanism of charge transport, role of microstructure and grain boundaries, their operational and environmental stability and the development of mitigation strategies for these challenging issues. First, we discuss the physics of perovskite FETs, highlighting the influences of ion migration, defects, film composition and microstructure, as well as external factors such as light and temperature. Based on this information, we summarize the influence of measurements conditions on the resulting performance of the perovskite FETs. Next, we detail the current status in the field of both 2D and 3D perovskite transistors and phototransistors. Finally, we examine the key challenges that this technology is facing and discuss how the insights broadly gained in the field of perovskite optoelectronics can be exploited for the advancement of perovskite FETs.

2. Physics of Perovskite FETs

The crystal structure of the hybrid perovskites varies from 3D to 2D, depending on their composition. 3D perovskites adopt the general formula ABX\textsubscript{3} (Figure 1a), where A\textsuperscript{+} is the organic cation, B\textsuperscript{2+} is the metal cation and X\textsuperscript{–} is the halide anion. They form a crystal of corner-sharing [BX\textsubscript{6}]\textsuperscript{4–} octahedra, with several size restrictions being necessary to maintain the stability of the lattice (Figure 1a).\textsuperscript{35,36} 2D perovskites exhibit a layered structure and are described with the general formula of Ruddlesden–Popper phases R\textsubscript{2}A\textsubscript{n−1}B\textsubscript{n}X\textsubscript{3n+1}, where R\textsuperscript{+} is typically an organic cation larger than A\textsuperscript{+}, interleaving inorganic plate-like networks of [BX\textsubscript{6}]\textsuperscript{4–} octahedra. The variable n in the sum formula represents the number of inorganic two-dimensional [BX\textsubscript{6}]\textsuperscript{4–} octahedra sheets that are separated by the bulky organic cation. Figure 1a shows a Ruddlesden–Popper perovskite structure for n = 1.

A field-effect transistor is a three-terminal device that functions as a voltage controlled electrical switch. The source and drain electrodes come in direct contact with the semiconductor material and the gate electrode is separated by a dielectric layer from the semiconductor and the other electrodes and is used to control the current in the channel formed between the source and the drain electrodes. Four principal FET device architectures exist, depending on the order in which the layers are deposited (Figure 1b,c). All of these device architectures have been demonstrated for perovskite transistors; however, most commonly bottom gate structures based on silicon/silicon oxide (Si/SiO\textsubscript{2}) are utilized due to the simplicity of their fabrication. Top gate structures offer the benefit of solution processing and post-deposition modifications at the interface to the dielectric layer, where charge transport normally takes place. In perovskite FETs developed to date, the distance between the source and drain electrodes (channel length L) typically lies in the range of a few to several hundreds of micrometers and the

Figure 1. a) The unit cell of the ABX\textsubscript{3} metal halide perovskite crystal structure and below schematic representation of 3D and layered 2D perovskite solid state structures. b) Commonly employed bottom gate/bottom contact (BGBC) FET architecture with perovskite as semiconducting material. c) Other architectures for perovskite field-effect transistors.
channel width of the electrodes (W) ranges typically from several hundred micrometers to a few millimeters. The capacitance per unit area (C_d) of the dielectric layer determines the operating voltage range, with thin and/or high-k dielectric layers being required for low voltage operation at the commonly used 3.3 or 5 V levels of modern electronics. The transistor geometry and design, especially the overlaps of the electrodes will further influence the maximal possible operating frequency and power dissipation of the field-effect transistors (see Section 6).

Unipolar devices utilize either holes (p-channel) or electrons (n-channel) as major carrier type, while in ambipolar devices both charge carriers contribute to the channel current. A field-effect transistor can operate in different regimes. For simplicity, in the following, we will limit the discussion to devices of a single carrier type. Upon the application of a voltage between the source and gate electrodes (V_{GS}), once V_{GS} surpasses the threshold voltage (V_{th}), the charges accumulate at the semiconductor/dielectric interface and the overall charge carrier density is proportional to (V_{GS}-V_{th}). The sign of the applied gate voltage and nature of the injecting contact determine the majority charge carrier in the channel. The distribution of mobile charges within the channel between source and drain electrodes follows the voltage applied between source and drain (V_{DS}). Consequently, the total channel current I_{DS} from source to drain can be expressed via Equation (1):

\[ I_{DS} = \frac{W}{L} C_d \mu \left[ (V_{GS} - V_{th}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \]

where \( \mu \) is the electric field independent charge carrier mobility. For small source drain voltages with respect to the gate voltage (V_{DS} < V_{GS}) the term \( \frac{1}{2} V_{DS}^2 \) can be neglected, resulting in a linear relationship between the channel current and given V_{DS} (Figure 2a), typically referred to as the “saturation regime”. The channel current in this saturation regime can be expressed as:

\[ I_{DS} = \frac{W}{2L} \mu_{sat} C_d \cdot (V_{GS} - V_{th})^2 \]  

(3)

Based on Equation (3) the square root of the channel current depends linearly on the gate voltage, as can be seen in Figure 2b for sufficiently large values of V_{DS}. The charge carrier mobility in the saturation regime can therefore be extracted following Equation (4):

\[ \mu_{sat} = \frac{2L}{WC_d} \left( \frac{\partial I_{DS}}{\partial V_{GS}} \right)^{1/2} \]

(4)

For gate voltages below the threshold voltage, an insufficient concentration of mobile carriers is present, and the channel current is very low—the transistor is “off”. From the semilog plot of the channel current the onset voltage (V_{on}) can be derived and marks the point at which the channel current abruptly exceeds the off-current (Figure 2b). The subthreshold swing (S) characterizes the steepness of the channel current increase and is influenced by the capacitance of the dielectric layer and the trap density at the interface (Equation (5)).

\[ S = \frac{\partial V_{GS}}{\partial \log I_{DS}} \]

(5)

The semilog plot of I_{DS} further allows to directly extract the on/off-ratio for a given V_{GS} and V_{DS} as ratio between “on” and “off” current, which is typically given as expression in power of tens.

The development of the expressions shown above, and in particular for the charge carrier mobility in Equations (2) and (4) is based on the gradual channel approximation (for a complete derivation we refer to refs. [37,38]), which assumes the electric field of the gate electrode to be perpendicular to the charge transport direction and to be larger than the electric field caused by the source drain voltage.[39] These conditions are typically fulfilled for large channel lengths in the range of micrometers and a dielectric layer thicknesses of only a few hundred nanometers. Short channel devices, on the other hand, in combination with thick dielectric thicknesses no longer satisfy these conditions. Furthermore, the electrical contacts are assumed to be ideal and hence the contribution from contact resistance is ignored in the above mentioned equations. However, non-ideal behavior and deviation from these analytical equations is often observed in perovskite FETs and could potentially lead to overestimation or underestimation of the charge carrier mobility. We refer the readers to several other excellent reviews that outline these basics of field-effect transistors[37,38,40] and focus in the following on those physical features which are unique to perovskite materials and have a stark influence on the perovskite FET’s operation and performance.

2.1. Ionic Defects and Ion Migration: Impact on Perovskite FET Operation

The mixed ionic-electronic nature of perovskites makes ion migration an intrinsic property of perovskite semiconductors.[34,41]
Consequently, the application of an electric field across a perovskite layer will not only lead to the motion of holes and electrons, but also to a redistribution of mobile ions and ionic defects (vacancies and interstitials). Several experimental techniques such as photoluminescence mapping, x-ray photoemission mapping or Kelvin probe measurements have visualized lateral ionic migration in perovskite films upon the application of an external lateral field similar to that forming between the source and drain electrodes in field-effect transistors. Generally speaking, ion migration involves both anions (e.g., I\(^-\), Br\(^-\)) and cations (e.g., MA\(^+\), Pb\(^{2+}\)). However, it has been experimentally and theoretically shown that ion migration in 3D perovskites is dominated by the motion of anions, such as iodide, due to a lower activation energy and significantly higher diffusion coefficients as compared to the other mobile ion species, and typically occurs on a time-scale of seconds. While in recent years ion migration has been confirmed for lead-based 2D perovskites those 2D perovskites that are based on tin (Sn) seem to be less prone to ion migration and it remains unclear to which extent the low-dimensionality or differences in chemical composition, bonding strengths and formation energies for vacancies and interstitials are responsible for this effect.

Ion migration complicates device characterization by triggering variations in electric field within the device that are not accounted for in the graduate channel approximation adopted for FET analysis and mobility determination. These effects can lead to non-ideal current-voltage (I–V) characteristics which yield mobility under- or overestimation, as well as faster material and device degradation. Importantly, the electric fields within field-effect transistors may be significantly higher than the typical electrical fields generated in photovoltaic or light-emitting devices. For example, the electric field applied between the drain and source electrodes in perovskite FETs with a channel length of several micrometers is comparable to that of photovoltaic cells with an absorber thickness of several 100 nm and can reach values in the range of MV m\(^{-1}\).

However, with the simultaneous application of the gate-source voltage, the total electric field exceeds that commonly found in photovoltaic cells by at least one order of magnitude. Screening of the gate voltage is therefore the most detrimental effect introduced by ionic motion in perovskite FETs since it not only lowers the channel current and the effective mobile charge carrier density (and therefore charge carrier mobility) but it can also dramatically alter the shape of the transistor electrical characteristics.

Sirringhaus and co-workers distinguished three (I–III) main regimes in n-type MAPbI\(_3\) FET operation under continuous bias and attributed the non-ideal I–V shape of the output characteristics to the following processes (Figure 3a): I) in the forward sweep, at low source–drain voltage V\(_{DS}\) ion migration is negligible and hence the device exhibits near-ideal transistor characteristics typical to the linear regime. II) With increasing the bias, ion migration becomes substantial, causing negatively (positive for p-type channels) charged species to migrate towards the gate electrode and

![Figure 3. Output characteristics measured at room temperature under DC bias for TGB devices with similar thickness of Cytop dielectric and same channel width with a) MAPbI\(_3\) semiconductor and short channel (20 µm) and b) MAPbI\(_3\) long channel (100 µm) as well as for long channel (100 µm) devices with c) 5% rubidium (Rb) addition to Cs\(_{0.05}\)FA\(_{0.17}\)MA\(_{0.78}\)PbI\(_3\) and same material in (d) but treated with diethylether (Et\(_2\)O, Lewis base) prior to deposition of the dielectric. Reproduced under terms of the CC-BY license. Copyright 2020, The Authors, AIP Publishing.]
screen the applied gate voltage; consequently, the drain current $I_{DS}$ decreases and no saturation behavior is observed. III) Positively charged species will move into the bulk and towards the backchannel interface, where the associated space charge will allow the formation of a parallel electron conduction channel. In the reverse sweep, the current is mostly dominated by this second conduction channel. Due to the field-dependence of ion migration, longer channel lengths (with an effective lower electric field for the same operating voltage) exhibit a less significant hysteresis caused by ion migration (Figure 3b). This understanding of massive hysteresis in the output characteristics is supported by measurements of dual-gate perovskite FETs for which a positive bias applied to the back gate provides control over the ionic screening effects and lowers the influence of hysteresis caused by ion migration. A simple and efficient way to test for ion migration is to bias the transistor in the "on" state and follow the temporal evolution of the current. A decay in the channel current within seconds to minutes is typically attributed to screening effects of mobile ions. It was also found that following an initial decay, the channel current can also increase due to healing of vacancies upon ion migration and/or reduction in contact resistance.

Ion migration is closely interlinked with the defect chemistry of the perovskite layer. In metal halide perovskites iodide interstitials ($I_I^-$) and vacancies ($V_I$) possess very low formation energies, therefore these species dominate the defect physics. The role of grain boundaries in ion migration, where the crystal lattice is discontinued and possesses a high defect density, remains under intense debate. Abate and co-workers demonstrated that grain boundaries inhibit ion migration, while others reported that ion migration is facilitated through grain boundaries. Nevertheless, the research on perovskite FET indicates that for the same material system the deposition method, processing details and composition (and therefore the density and nature of ionic defects) determine to which extent ion migration and defect redistribution influence the device performance, temporal and temperature stability of the channel current and, consequently, the reliability of extracted charge transport parameters. Particularly, the incorporation of other A-site cations like formamidinium (FA$^+$), or Cs$^+$, the use of additives such as rubidium salts (Rb$^+$), or post processing treatments, have shown to control the ionic defect density in such a way that transistor operation with little hysteresis at room temperature can be achieved (see Figure 3c,d). Nevertheless, the overall measurement conditions still dramatically influence the impact of ion migration on the $I$–$V$ characteristics of perovskite FETs, as will be discussed in the following sections.

Several studies showed that electrolysis of the perovskite itself can occur, with oxidation of halides taking place at the anode and reduction of potential components like for example methylammonium at the cathode. The redistributed ions, and possible redox products, can further alter the optical and electronic properties of the remaining film, cause contact degradation (see Sections 3.3.2. and 5.4.), dope the contact area or change the trap distribution. Furthermore, ion migration can lead to microstructural changes and especially phase segregation in mixed halide systems. Ion migration has often been linked to the observation of hysteresis in the electrical characteristics of perovskite devices even beyond FETs. However, it is important to note that ionic migration occurs even in devices that exhibit little to no hysteresis. In the field of perovskite photovoltaics, many recent reports have shown that hysteresis can be significantly minimized (see also Section 5.1) through engineering of the interfaces between the perovskite active layer and the contact materials. In the vast majority of perovskite solar cells, a direct contact between the metal electrode and the perovskite material is avoided, an approach that so far has been underutilized in perovskite field-effect transistor research.

### 2.2. Effects of Composition and Microstructure

Tuning the composition of perovskite materials is a simple and effective method to control their optical and electronic properties. Unlike the field of perovskite solar cells, where many different compositions and microstructures have been explored and meticulously optimized, only relatively few have been intentionally implemented and investigated in perovskite FETs. Among these, MAPbI$_3$ is by far the most studied, and is a representative example for 3D metal halide perovskites in terms of some of the issues that can be encountered. For example, there appears to be a disagreement regarding the type of transport observed in MAPbI$_3$ FETs: while some groups found an ambipolar channel, with varying strengths of electron and hole transport, and even light emission, others demonstrate only unipolar p- or n-type transport, even for the same device geometry and the same contact material. This rather peculiar behavior could stem from the sensitivity to the stoichiometry of the precursors, with an excess/deficiency of methylammonium iodide (MAI) giving rise to n-doping/p-doping of the perovskite layer. Even when doping is not introduced intentionally, fractional accidental deviations in precursor stoichiometry can strongly impact on the electronic structure of the perovskite.

Fassl et al. demonstrated that such unintended variations can lead to either n- or p-type properties due to the accumulation of ionic defects at the film surface. Mativenga and co-authors reported that excess PbI$_2$ increases the channel current of n-type FETs, which might appear to contradict the aforementioned studies. However, it is possible that this discrepancy originates from the fact that the authors examined bottom gate architecture devices, and the introduced excess or deficiency is segregated to the surface of the samples, so the composition at the buried bottom interface with the substrate (i.e., the gate dielectric) is unknown. The impact of differences in the vertical composition of non-stoichiometric films could be elucidated in future studies by employing, for example, a dual-gate device configuration. Another aspect of perovskite composition that can play a role in the performance of perovskite FETs is the choice of A-site cation. Organic cations, such as MA$^+$ or FA$^+$ can be polarized, which will influence the evolution of the FET properties as a function of temperature (see Section 2.3) as well as the hysteresis in the $I$–$V$ characteristics of the devices.

The microstructure also plays an important role, as, for example in MAPbI$_3$ where the study of single crystals, polycrystalline films (with varying grain size), uniaxially aligned ribbons, nanoplatelets, nanowires, and quantum dots led to drastic differences in electronic
properties. The various microstructures can be accomplished via processing or post-processing steps, and are accompanied by different defect densities, for example at the surface or grain boundaries. The microstructure can also influence phase transitions, thus affecting the temperature-dependence of the FET properties. An important note is that the microstructure at the surface might vary from that at the bottom interface with the substrate – evident for example by scanning electron microscopy (SEM) – which leads to different performance of the same film in different FET device architectures.

2.3. Effect of Temperature

Early studies quickly realized that screening of the electronic transport by ionic migration, along with the structural fluctuations and dynamical disorder (rotations of the MA unit around its axis and PbX₆ octahedral distortions) make electrostatic gating of lead-based 3D perovskites non-trivial. These phenomena are thermally activated, and thus can be reduced and often even suppressed upon decreasing the temperature, resulting in several early studies reporting on the performance at 70–80 K. Recent advances in material and device engineering have led to more reliable transistor behavior, with low hysteresis and charge carrier mobilities >1 cm² V⁻¹ s⁻¹ at room temperature, which allowed investigations of temperature-related effects. Temperature dependent studies provide important details about the charge transport mechanism in perovskite materials, which remains elusive. When assessing the effects of temperature on electronic transport, the structural phase transitions occurring in some perovskites should be considered. MAPbI₃, for instance, exhibits an orthorhombic (γ-phase) below 165 K, forms a tetragonal structure (β-phase) between 163 and 327 K, and above this temperature, it crystallizes in a cubic unit cell (α-phase).

For 3D metal halide perovskites, most temperature dependent studies have been performed on MAPbI₃, with only few reports investigating other compositions, for example, polycrystalline films of MAPbBr₃ and CsPbBr₃. Among the different reports for MAPbI₃, an increase in charge carrier mobilities with decreasing temperature was observed consistently in the range of 300–160 K, resulting in a negative temperature coefficient, which is indicative of electron-phonon coupling being the major charge-carrier scattering mechanism (Figure 4). This behavior is remarkable considering the overall low charge carrier mobilities and stands

![Figure 4](https://example.com/four.png)

**Figure 4.** Temperature dependence of the charge carrier mobility for MAPbI₃, obtained by various groups: a) Electron mobility versus temperature for devices with large grains but differently treated gold bottom contacts. b) Temperature dependence of the electron mobility for transistors with small (0.25M) to large (0.75M) grain size. c) Temperature dependent electron mobility determined in the linear and saturation regime d) DFT simulations of the temperature dependence of the electron and hole mobilities. e) Temperature dependence of the electron mobility for microplatelets with different thicknesses and corresponding phase transition temperatures marked with arrows. f) Hole and electron mobility versus temperature around the phase transition temperature. Panel (a) and (b) reproduced under terms of the CC-BY license. Panel (c) adapted with permission. Panel (d) adapted under terms of the CC-BY license. Panel (e) adapted under terms of the CC-BY license. Panel (f) reproduced with permission.
in contrast to organic semiconductors or amorphous silicon that exhibit similar mobilities but thermally activated transport typical of disordered systems.[98–101] A particularly noteworthy work is that by Senanayak et al., who conducted temperature dependent measurements on polycrystalline films with different grain sizes, which are typically associated with different concentrations of ionic defects and identified three main regimes (I–III) of the temperature dependent electron mobility, determined from the saturation regime of the $I$–$V$ characteristics (see Figure 4a). In the “high” temperature regime (III) $240 \, \text{K} < T < 300 \, \text{K}$, a larger temperature coefficient was observed for films with smaller grains and high defect concentrations.[33] Dielectric loss spectroscopy measurements confirmed that charge transport in MAPbI$_3$ for $T > 240 \, \text{K}$ was mainly mediated by ion migration. A field-effect for defect-rich MAPbI$_3$ films could only be observed at low temperature, explaining the difficulty to establish electrostatic gating at room temperature in many of the early studies on perovskite FETs. In the second regime (II), the temperature dependence down to 160 K can be explained by the decrease in the polarization disorder of MA$^+$, supported by the changes in order determined by a combination of temperature dependent capacitance and Raman measurements.[33] A different mechanism determines the temperature dependence in the first regime (I) ($T < 160 \, \text{K}$) and seems to dominate at temperatures below the phase transition temperature to the orthorhombic phase. Since MA$^+$ has been shown to be fully ordered in the orthorhombic phase,[302,303] the temperature dependence of the electron mobility in this regime could be dominated by phonon scattering.

Other research groups observed a sudden increase in charge carrier mobility close to the phase transition from tetragonal to orthorhombic crystal phases.[27,33,98] Soci and co-workers studied the electron and hole mobilities extracted from the linear regime of polycrystalline MAPbI$_3$ transistors and revealed that both quantities were higher in the orthorhombic phase than the corresponding ones in the tetragonal phase. Their observations were supported by semi-classical Boltzman transport theory that, while predicting far higher absolute values, was qualitatively in agreement with the trend of increasing mobilities with temperature (see Figure 4d) and higher mobilities in the orthorhombic phase due to a lower effective mass of the charge carriers. A somewhat different trend was reported by Liu et al. recently studied the temperature dependence of the electrical properties in 2D (C$_6$H$_5$C$_2$H$_4$NH$_3$)$_2$SnI$_4$ (PEA$_2$SnI$_4$) films, a representative 2D perovskite, showed a completely different trend to those obtained in 3D perovskites. Measurements conducted on FETs with low contact resistance resulted in a thermally activated transport, namely a decrease in both electron and hole mobilities with decreasing temperature, which was attributed to the small crystallite size and polycrystalline nature of the films.[106] Similarly, early studies by Papa-vassiliou on large, millimeter sized PEA$_2$SnI$_4$ crystals revealed a decrease in conductivity with decreasing temperature, suggesting that the temperature activated transport might have an intrinsic origin.[107]

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2.4. Measurement Conditions: Why Establishing a Consensus for Perovskite FET Characterization Protocols Matters

The complexity of the dynamic processes occurring in perovskite materials, from ion migration, to polarization and defect healing, requires that a particular attention is paid to the measurement and biasing conditions selected for the characterization of a perovskite FETs (Figure 5). Typically, FETs are characterized in a continuous DC mode, with total measurement times in the range of seconds or even minutes.[37] In perovskite transistors, however, application of these biases for a long period of time can lead to ion migration, which, in turn, results in screening of the electric fields, contact degradation and, consequently, a temporal instability of the current during the electrical characterization. These effects can, in principle, be reduced if electrical characterization is performed very fast by utilizing high sweep rates. However, years of research on perovskite photovoltaics demonstrated that the electrical performance of a device can be underestimated by applying large sweep rates of several volts per second. Similarly, in FETs, high sweep rates might artificially provide larger values for charge carrier mobilities, particularly at higher temperatures, when dynamic effects play an important role.[30] Choosing the most appropriate sweep rate is not trivial, since it depends on many factors, including device structure and geometry, perovskite type, and more. To unify testing protocols and improve the reproducibility between different labs, we recommend that 1) the sweep rate is reported and 2) characterization at different rates is included. Furthermore, like with any FET, considering that the $I_{DS}$ covers a range of several orders of magnitude and requires different levels in absolute resolution, such a measurement demands very different integration times in the “off” and “on” state of the transistor for most commonly employed parameter analyzers. This, in turn, can lead to varying response times of the dynamic effects of perovskite FETs at each step of the measurement. Choosing an instrumental delay time that is sufficiently large to account for these differences in integration time for small and large channel currents is of utmost importance. The inclusion of the temporal stability of the channel current in the “on”-state (under applied bias) alongside with the measured output and transfer characteristics, similar to the maximum power point (MPP)[41] tracking, which is an established routine in the field of perovskite photovoltaics, will greatly enhance the reliability of the extracted transistor parameters and minimize the discrepancies in results obtained between different labs. We also recommend that the measured gate current, $I_{GS}$, is reported, as it can indicate charging and screening effects.

One approach to reduce the influence of gate potential screening by ion migration is the utilization of pulsed or AC modulated measurement routines. In this case, details on the timings (pulse width, frequency, and integration times) are necessary to allow reproducible measurement among different groups. The measurement history of the perovskite device will also influence its characteristics and should be taken into account for experimental design. Pre-biasing (particularly with the opposite voltage polarity) should be avoided in order to be able to judge the impact of ion migration and screening effects on the device performance correctly.

The fact that perovskite materials are photoactive in the visible range cannot be neglected when selecting the measurement conditions of perovskite FETs. In many perovskite compositions, the absorption of light leads to the generation of free charge carriers due to the very low exciton binding energy and high dielectric constants of these materials.[110] Perovskite FET have been shown to be very sensitive to light, with an increase in channel current by several orders of magnitude upon illumination and consequently typically higher charge carrier mobilities.[111,112] This property has triggered interest in the study of perovskite phototransistors, but should also be considered when regular FETs are characterized and transistor characterization should, therefore, be conducted exclusively in the dark to avoid the contribution of the photogenerated charge carriers to the channel current. Nevertheless, it is known that even exposure to light prior to characterization also influence the device properties. Light (even of low intensity) has been shown to effectively heal defects in perovskite materials and cause ion redistribution.[113,114] Prolonged illumination at high intensities can cause phase segregation[115] and material degradation.[116] Considering that illumination cannot be completely avoided, for example during contacting, illumination sources, times and intensities should be documented and kept identical between different measurements and different samples.

Figure 5. Summary of the various measurement conditions that may impact the electrical characteristics of a perovskite FET.
Another important experimental aspect that should be documented is related to the environment during fabrication, storage, and device characterization. Of particular importance is the presence of water and oxygen, since they alter the densities of traps and defects and can lead to degradation of perovskites. One alternative is an electrical characterization in vacuum, which is predominantly used for low temperature measurements. However, 3D as well as 2D perovskite materials have been shown to degrade under prolonged exposure to vacuum, changing composition and microstructure of the active layer. Another solution to reduce the impact of interaction with environmental species is device encapsulation. Top-gate dielectrics inherently offer this advantage and consequently some of the best perovskite transistors reported to date are based on this architecture.

3. Current Status in Perovskite Transistors and Phototransistors

In this section we will review the current status of research on perovskite transistors and phototransistors. First, progress in field-effect transistors will be described for 2D and 3D perovskites, followed by an assessment of the impact of the dielectric layer and source-drain electrodes on the device performance. Next, the state of research in perovskite phototransistors will be discussed, including those based on solely a perovskite active layer, as well as those that include a heterostructure in which a perovskite layer is interfacial with another material.

3.1. 2D Perovskite Field-Effect Transistors

2D hybrid perovskite FETs were first reported in 1999 by Kagan et al. and were based on a spin-coated (C₆H₅C₂H₄NH₃)₂SnI₄ (PEA₂SnI₄) perovskite layer deposited onto a doped Si substrate with a SiO₂ gate dielectric. These devices, with either top or bottom source and drain contacts made from Pt, Pd, or Au, yielded a maximum room temperature hole mobility of μₑ = 0.62 cm²V⁻¹s⁻¹ (Figure 6a). In 2001, the same group improved the mobilities to μₑ = 1.4 cm²V⁻¹s⁻¹, however, the large negative threshold voltage and non-negligible hysteresis in the I–V-curves remained staples of the first 2D perovskite transistors. Devices based on fluorinated analogues 2-, 3-, or 4-fluorophenethylammonium PEA have also been tested and it was found that the substitutions yielded changes in electronic structure and film morphology, resulting in charge carrier mobilities between μₑ = 0.2 and μₑ = 0.6 cm²V⁻¹s⁻¹ for the different cations. In 2002, melt processing of PEA₂SnI₄ onto a SiO₂/polyimide dielectric generated devices with mobilities reaching values of μₑ = 2.6 cm²V⁻¹s⁻¹, an improvement that was attributed to larger grain size resulting from the better control of crystallization via the new deposition method. Only two years later, the first thermally evaporated PEA₂SnI₄ perovskite FETs were successfully fabricated, and exhibited hole mobilities of μₑ = 0.78 cm²V⁻¹s⁻¹. After a relatively large time gap, a renewal of interest in perovskite transistors was sparked by the impressive progress made in perovskite optoelectronics, in particular in perovskite photovoltaics. As such, 2D perovskite FETs re-emerged in 2016 with the work of Adachi and collaborators, who fabricated PEA₂SnI₄ transistors in both coplanar and staggered architectures. These FETs operated as p-channels, similar to the examples described above, but the meticulous device engineering resulted in the elimination of the hysteresis and high a device performance. The maximum field-effect mobilities were tuned between μ₀ = 1.1 and 15 cm²V⁻¹s⁻¹ by tailoring the surface energy with self-assembled monolayer (SAM) treatments to enhance film crystallinity, by inserting an interlayer of MoOₓ to enhance injection and employing the fluoropolymer Cytop as gate dielectric to reduce the density of trap states at the semiconductor/dielectric interface (Figure 6b).

In vacuum deposited PEA₂SnI₄ transistors, however, the staggered architecture led to higher hole mobilities (μ₀ = 0.78 ± 0.24 cm²V⁻¹s⁻¹) than the coplanar architecture (μ₀ = 6.7 ± 1.8 x10⁻³ cm²V⁻¹s⁻¹) as a result of the better interface established between the evaporated Au and the perovskite active layer.

The first n-type 2D perovskite FET was demonstrated in 2016 by inserting a C₆₀ interlayer between the contact metal and the PEA₂SnI₄ film for a more efficient injection to the conduction band of the perovskite. A dependence on the work function of the source-drain contacts was observed, with Au/C₆₀ contacts yielding mobilities of μₑ = 0.9 cm²V⁻¹s⁻¹, Ag/C₆₀ electrodes resulting in μₑ = 1.4 cm²V⁻¹s⁻¹ and Al/C₆₀ in μₑ = 2.1 cm²V⁻¹s⁻¹ (Figure 6c). Similar to the case of p-channel FETs, electron transport was also found to be less efficient across the organic spacers, as systematically studied by Li et al. in FETs based on the Ruddlesden–Popper perovskite (C₆H₅NH₃)₂PbI₃ with n = 1, 2, or 3. The device properties depended on the number of conducting metal halide octahedral present between the organic cation layers and the electron mobilities evaluated at T = 77 K were tuned from μₑ = 2 x 10⁻⁶ to 1.25 cm²V⁻¹s⁻¹ by increasing the number of octahedral layers from n = 1 to n = 3. Perovskite FETs based on single crystals BA₂(MA)₃PbI₃ exposed electron mobilities ranging from μₑ = 0.087 to 0.75 cm²V⁻¹s⁻¹ at T = 150 K by varying the number of conducting octahedral layers from 2 to 5.

By increasing the device dimensions to very long channel lengths (L = 500 µm), the impact of contact resistance on the transistor performance was reduced substantially and electron and hole mobilities of μₑ = 4.6 cm²V⁻¹s⁻¹ and μ₀ = 26 cm²V⁻¹s⁻¹, respectively, have been demonstrated. These values approached those obtained in devices fabricated by laminating single crystals over substrates with SiO₂ dielectric and Au/MoOₓ contacts, that is, μₑ = 35 cm²V⁻¹s⁻¹ and μ₀ = 50 cm²V⁻¹s⁻¹. The elimination of grain boundaries suppressed the most effective oxidation channels, and hence resulted in a higher degree of
electrical stability – the mobility and threshold voltage remained unchanged over a test period of 1 hour; however, the yield from the production of these devices was below 1% due to the difficulty of establishing a good mechanical contact between the single crystals and the pre-defined bottom contacts.\[32\]

Since oxygen diffusion via grain boundaries represents the main source of degradation through conversion of Sn\(^{2+}\) into Sn\(^{4+}\),\[131\] and subsequent charge carrier trapping by the impurity cation,\[131,132\] later efforts focused on reducing this effect by altering the processing and structure of devices. Matsushima et al. annealed the films at \(T = 100^\circ\text{C}\) in a nitrogen atmosphere to generate larger grains, which resulted in devices that exhibited only a minimal change in drain current over time.\[133\] Further improvement in stability was achieved by encapsulating the devices with Cytop: these devices showed no change in the drain current during 5 h of exposure to air, whereas a six orders of magnitude decrease was observed in unencapsulated devices. The changes were reversible and the initial properties have been restored after an overnight storage in vacuum.\[121\]

The electrical performance of the 2D perovskite films is also very sensitive to its composition. For example, an excess of PEA in the perovskite precursor passivates grain boundaries,\[106,134\] while the presence of a Lewis base such as dimethyl sulfoxide (DMSO) catalyzes the passivation of the anti-site defects;\[134\] both result in transistors with superior properties.\[134\] Addition of metallic Sn to the precursor solution facilitates the reduction of oxidized Sn\(^{4+}\) back to Sn\(^{2+}\) via a comproportionation reaction.\[134\]

By replacing the PEA organic cation with 2-(3″′,4″′-dimethyl-2,2″′:5″′,2″′-quaterthiophen)-5-yl)ethan-l-ammonium (4Tm), Gao et al. observed that the mobility improved from \(\mu_h = 0.15 \text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}\) to \(\mu_h = 2.32 \text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}\).\[135\] Other stoichiometries studied include 2D perovskite PEA\(_2\)Bi\(_4\)Br\(_{9x}\), for which microplatelets were incorporated in p-type transistors with mobilities of \(\mu_h = 1.66 \times 10^{-5} \text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}\) in air.\[136\]

In summary, after more than a decade gap in the research on 2D perovskite FETs, the recent revival of interest has generated remarkable progress: both n-type and p-type transistors have been fabricated and characterized based on poly-crystalline films and single crystals with various contacts and...
dielectrics, as listed in Table 1. The continuous improvements in device performance as a result of a better understanding of the microscopic mechanism limiting charge injection and transport promise that this class of materials could become excellent candidates for cost-effective and high-quality transistors.

### Table 1. Summary of 2D perovskite FETs.

| Year | Perovskite composition | Active layer | Temp. | Geometry | Dielectric material | Contact material | $\mu_h$ [cm$^2$ V$^{-1}$ s$^{-1}$] | $\mu_e$ [cm$^2$ V$^{-1}$ s$^{-1}$] | Reference |
|------|------------------------|--------------|-------|----------|---------------------|-----------------|-------------------------------|-------------------------------|-----------|
| 1999 | PEA$_2$SnI$_4$         | pc, spin     | RT    | BGBC     | SiO$_2$             | Pd              | 0.62                          |                               | [17]      |
| 2001 | 2-FPEA$_2$SnI$_4$      | pc, spin     | RT    | BGBC     | SiO$_2$             | Pd              | 0.24                          |                               | [122]     |
| 2001 | 3-FPEA$_2$SnI$_4$      | pc, spin     | RT    | BGBC     | SiO$_2$             | Pd              | 0.51                          |                               | [122]     |
| 2001 | 4-FPEA$_2$SnI$_4$      | pc, spin     | RT    | BGBC     | SiO$_2$             | Pd              | 0.48                          |                               | [122]     |
| 2001 | PEA$_2$SnI$_4$         | pc, spin     | RT    | BGBC     | SiO$_2$             | Pd              | 1.4                           |                               | [122]     |
| 2002 | PEA$_2$SnI$_4$         | pc, spin     | RT    | BGBC     | polyimide           | Au              | 2.6                           |                               | [123]     |
| 2004 | PEA$_2$SnI$_4$         | pc, vacuum   | RT    | BGTC     | SiO$_2$/OTS         | Au              | 0.78                          |                               | [124]     |
| 2016 | PEA$_2$SnI$_4$         | pc, spin     | RT    | BGBC     | SiO$_2$             | Au              | 0.53 ± 0.24                   |                               | [120]     |
| 2016 | PEA$_2$SnI$_4$         | pc, spin     | RT    | BGBC     | SiO$_2$/NH$_3$I–SAM | Au              | 2.5 ± 0.7                     |                               | [120]     |
| 2016 | PEA$_2$SnI$_4$         | pc, spin     | RT    | BGCT     | SiO$_2$/NH$_3$I–SAM | Au/MoO$_x$      | 5.7 ± 0.8                     |                               | [120]     |
| 2016 | PEA$_2$SnI$_4$         | pc, spin     | RT    | BGCT     | SiO$_2$/NH$_3$I–SAM | Au/MoO$_x$      | 7.1 ± 0.4                     |                               | [120]     |
| 2016 | PEA$_2$SnI$_4$         | pc, spin     | RT    | TGTC     | Cytop               | Au/MoO$_x$      | 6.4 ± 1                       |                               | [120]     |
| 2016 | PEA$_2$SnI$_4$         | pc, spin     | RT    | TGTC     | Cytop               | Au/MoO$_x$      | 12 ± 1                        |                               | [120]     |
| 2016 | PEA$_2$SnI$_4$         | pc, spin     | RT    | TGTC     | Cytop               | Au/MoO$_x$      | (6.7 ± 1.8) × 10$^{-3}$       |                               | [130]     |
| 2016 | PEA$_2$SnI$_4$         | pc, vacuum   | RT    | BGTC     | SiO$_2$/OTS         | Au              | 0.78 ± 0.24                   |                               | [130]     |
| 2016 | PEA$_2$SnI$_4$         | pc, spin     | RT    | TGTC     | Cytop               | Au/C$_60$       | 0.6 ± 0.2                     |                               | [121]     |
| 2016 | PEA$_2$SnI$_4$         | pc, spin     | RT    | TGTC     | Cytop               | Ag/C$_60$       | 1.1 ± 0.2                     |                               | [121]     |
| 2016 | PEA$_2$SnI$_4$         | pc, spin     | RT    | TGTC     | Cytop               | Al/C$_60$       | 1.5 ± 0.3                     |                               | [121]     |
| 2017 | PEA$_2$SnI$_4$         | pc, spin     | RT    | TGTC     | Cytop               | Au/MoO$_x$      | 26                            |                               | [106]     |
| 2017 | PEA$_2$SnI$_4$         | pc, spin     | RT    | TGTC     | Cytop               | Al/C$_60$       | 4.6                           |                               | [106]     |
| 2018 | BA$_2$PbI$_4$          | microplate,  | 77 K  | BGBC     | SiO$_2$             | Ag              | 1.25                          |                               | [109]     |
|      |                       | slow evaporation |      |          |                     |                 |                               |                               |           |
| 2019 | PEA$_2$SnI$_4$         | pc, spin     | RT    | BGTC     | PVA/CL-PVP          | Au              | 0.3 ± 0.07                    |                               | [129]     |
| 2019 | PEA$_2$SnI$_4$         | sc, refrigeration | RT   | BGBC     | SiO$_2$             | Au/MoO$_x$      | 50                            |                               | [32]      |
| 2019 | PEA$_2$SnI$_4$         | sc, refrigeration | RT   | BGBC     | SiO$_2$             | Al/C$_60$       | 35.5                          |                               | [32]      |
| 2019 | PEA$_2$SnI$_4$         | pc, spin     | RT    | BGTC     | SiO$_2$             | Au/MoO$_x$      | 0.4 ± 0.19                    |                               | [133]     |
| 2019 | PEA$_2$SnI$_4$         | pc, spin     | RT    | BGTC     | SiO$_2$             | Au/MoO$_x$      | 7.9 ± 2.3                     |                               | [133]     |
| 2019 | PEA$_2$SnI$_4$         | pc, spin     | RT    | BGTC     | SiO$_2$             | Au              | 0.11                          |                               | [135]     |
| 2019 | 4TmSnI$_4$             | pc, spin     | RT    | BGTC     | SiO$_2$             | Au              | 1.78                          |                               | [135]     |
| 2020 | (BA)$_2$((MA)$_n$PbnI$_{3n}$)$_{n+1}$ | sc, solution cooling | 150 K | BGTC     | SiO$_2$             | Ca              | 0.5                           |                               | [108]     |
| 2020 | PEA$_2$SnI$_4$         | pc, spin     | RT    | BGTC     | SiO$_2$             | Au              | 0.21 ± 0.09                   |                               | [134]     |
| 2020 | PEA$_2$SnI$_4$         | pc, spin     | RT    | BGTC     | SiO$_2$             | Au              | 0.67 ± 0.13                   |                               | [134]     |
| 2020 | PEA$_2$SnI$_4$         | pc, spin     | RT    | BGTC     | SiO$_2$             | Au              | 2.53 ± 0.46                   |                               | [134]     |
| 2020 | PEA$_2$SnI$_4$         | pc, spin, O$_2$ | RT   | BGTC     | SiO$_2$             | Au              | 3.51 ± 0.6                    |                               | [134]     |
| 2020 | PEA$_2$BiAgBr$_3$      | microplate,  | RT    | BGBC     | SiO$_2$             |                 | 1.66 × 10$^{-3}$              |                               | [136]     |

Temp., measurement temperature; pc, polycrystalline; sc, single crystal or single crystalline film; spin, fabricated by spin-coating; vacuum, fabricated by thermal evaporation under reduced pressure; RT, room temperature; OTS, octadecyltrichlorosilane; PVA, poly(vinyl alcohol); CL-PVP, cross-linked poly(4-vinylphenol).

#### 3.2. 3D Perovskite Field-Effect Transistors

3D perovskites have rapidly attracted interest owing to their extraordinary optoelectronic properties. Implementing and controlling the electrostatic doping of perovskites with the use of FET structures, however, has proven to be more challenging...
due to the screening effects introduced by the mobile ions, as was detailed in Section 2.1.\cite{53}

3.2.1. 3D Hybrid Perovskite Field-Effect Transistors

The first 3D hybrid perovskite transistor was reported by Mei et al. in 2015 on CH$_3$NH$_3$PbI$_{3-x}$Cl$_x$ thin films. The FETs had bottom contacts consisting of Au treated with 2,3,5,6-tetrafluoro-4-(trifluoromethyl) benzenethiol (TTFB) SAM and a Cytop top gate dielectric. It functioned as an ambipolar transistor, with hole mobilities of $\mu_h = 1.3$ cm$^2$ V$^{-1}$ s$^{-1}$ and electron mobilities $\mu_e = 1$ cm$^2$ V$^{-1}$ s$^{-1}$ (Figure 7a).\cite{29} While the current-voltage characteristics were not ideal, mobilities were conservatively estimated and, remarkably, the devices operated at room temperature. The use of the inert gate dielectric Cytop created a semiconductor/dielectric interface with a small density of electronic traps, which was key in achieving this performance.\cite{128} With the gate dielectrics consisting of the most common dielectric, SiO$_2$, only a weak modulation of the source-drain current by the gate-source voltage was observed at room temperature in FETs with top Au contacts that were encapsulated in Poly(methyl methacrylate) (PMMA) (hole and electron mobilities in the order of 10$^{-4}$ cm$^2$ V$^{-1}$ s$^{-1}$), and transport was limited to low temperatures in unencapsulated devices.\cite{28} Field-effect mobilities in the order of 10$^{-2}$ cm$^2$ V$^{-1}$ s$^{-1}$ were obtained at $T = 77$ K in CH$_3$NH$_3$PbI$_3$ FETs with bottom Au contacts and SiO$_2$ dielectric. Notably, the balanced mobilities also lead to

Figure 7. a) First 3D perovskite FET had a TGBC configuration with Cytop dielectric. b) Devices in a similar configuration, but with improved film morphology by surface passivation. c) First Sn-based 3D perovskite FET had a TGBC configuration with PMMA/Al$_2$O$_3$ dielectric. Panel (a) adapted under terms of the CC-BY license.\cite{29} Copyright 2015, The Authors, Cambridge University Press. Panel (b) reproduced with permission.\cite{33} Copyright 2020, Springer Nature. Panel (c) adapted with permission.\cite{137} Copyright 2021, John Wiley and Sons.
the observation of light-emission.[27] High-frequency AC modulation of the applied bias reduced the ionic drift and cation polarization and yielded brighter and more uniform electroluminescence in perovskite light-emitting field-effect transistors (LEFETs), even at room temperature.[96] When using Al contacts in the same device geometry, Labram et al. obtained only n-type FETs, as expected based on the energy level alignments of the perovskite and electrode material.[35] The merit of this work is that it provided a series of careful temperature dependent measurements in transistor, capacitor and solar cell structures that univocally demonstrated that the perovskite layer is susceptible to polarization as a result of the ionic migration and alignment of the organic cation in the presence of an electric field. These events occur at spatial and time scales relevant to those of charge transport and, along with the structural fluctuations and dynamical disorder,[92] hamper the operation at and field. These events occur at spatial and time scales relevant to those of charge transport and, along with the structural fluctuations and dynamical disorder,[92] hamper the operation at and near room temperature in perovskite devices. While these early examples represent groundbreaking work in perovskite FET research, the low device yield, operational and environmental instabilities and non-idealities in current–voltage characteristics represent serious bottlenecks for both accessing the charge transport properties in these materials and for their transition to commercial thin film electronic circuits (see Section 6 for more details). In the following years, effort was focused on gaining a good fundamental understanding of the charge transport physics in perovskite FETs, both in the bulk of the perovskite layer and at device interfaces.

The stoichiometry, composition, grain distribution, and orientation with respect to the substrate, were all found to drastically impact the final device performance, despite the pre-existing widely accepted notion that the optoelectronic properties of these materials have a high resilience to defects.[138–140] Ji et al. showed that by varying the ratio of MA1·PbI2 in the precursor solution, the channel type can be modified from unipolar (p- or n-type) to ambipolar, with excess PbI2 promoting electron transport and MAI excess yielding hole transport.[141] Tang et al. observed a similar pattern for the hole mobility, which increased by over two orders of magnitude in samples with some PbI2 deficiency, but observed a concurrent 40% reduction in electron mobility.[73] Discrepancy between these results may be a consequence of the difference in processing techniques: Ji et al. fabricated the perovskite layers by spin-coating in ambient air (resulting in substantial oxygen exposure of the perovskite) while Tang et al. used thermal evaporation which occurred in vacuum. There is also evidence that the composition of perovskite precursor can have a substantial impact on device stability. For example, while the electron mobility of MAPbI3 FETs was highest when the ratio of MA1·PbI2 in the precursor was 6.5 (μe = 0.05 cm2 V–1 s–1), the current–voltage hysteresis was substantially reduced by changing the ratio to 4.5, albeit with the electron mobility dropping to μe = 0.02 cm2 V–1 s–1.[142] In a different report, however, the same group found that the precursor with a component ratio MA1·PbI2 of 1:1 exhibits the highest electron mobility of μe = 0.1 cm2 V–1 s–1,[143] underlining the importance of fine tuning the stoichiometry in achieving consistent device performance. By using a solvent combination of diethylsulfide and N,N-dimethylformamide (DMF) and increasing the MA concentration in the precursor solution, Jana et al. demonstrated MAPbI3 FETs with hole mobilities as high as μh = 23.2 cm2 V–1 s–1 when deposited on Si substrates and μh = 11.5 cm2 V–1 s–1 on kapton.[134] She et al. proposed a method for surface cleaning and passivation which exploited solvent polarities in a three-step process: solvent rinse to remove weakly bonded species from the surface, healing to eliminate surface organic halide vacancies, followed by subsequent cleaning from the residual ionic species introduced during step 2.[135] This approach led to a reduction in the concentration of ionic surface defects, and, consequently, the suppression of hysteresis in the current-voltage characteristics.

An electron mobility of μe = 4.2 cm2 V–1 s–1 was measured at 300 K (Figure 7b), increasing to μe = 10.6 cm2 V–1 s–1 at 80 K in devices with bare Cr contacts, while hole mobility reached μh = 2.1 cm2 V–1 s–1 at 300 K on PFBT treated Au contacts. Senanayak et al. showed that replacing PbI2 with Pb(Ac)2, where Ac = acetate, in the precursor mixture, resulted in better and more uniform substrate coverage, larger grain size, and lower surface roughness, along with a higher degree of conversion of the starting material into the final perovskite.[33] Further optimization of the perovskite film microstructure has been obtained by increasing the concentration of the Pb(Ac)2 precursor from 0.25 to 0.75 M, which promoted an increase in the grain size from 38 to 150 nm and, consequently, an enhancement in mobility from 0.2 ± 0.08 to 0.6 ± 0.2 cm2 V–1 s–1; both values were extracted at 100 K and only electron transport has been detected.[33]

Doping the perovskite film offers another strategy for tuning the morphological and electronic properties of the films. For example, small quantities of chlorine (Cl–) ions can be added to the MAPbI3 precursor from salts such as PbCl2 to enhance the morphology of the perovskite film.[145,146] The final Cl– content is typically below 3% and its effect is most notable in the enhancement of the grain size of polycrystalline perovskite films by slowing down the crystallization process upon its reaction with MAI to form a metastable MAPbCl3 phase and eliminate the excess CH3NH3+.[147] Following the success of MAPb1–xClx in room temperature perovskite FETs, the quality of the MAPb1–xClx film was later improved by a solvent annealing treatment with DMF vapor, which resulted in field effect mobilities of μh = 15.8 and μe = 15.7 cm2 V–1 s–1 for holes and electrons, respectively, upon removal of the preferential orientation unfavorable for charge transport, increasing grain size, and healing electronic traps located at grain boundaries by solvating unreacted PbI2 and MAI components.[74]

Following its common use in perovskite photovoltaics,[148] the metal cation Cs+ has been introduced into the MAPb1 perovskite composition, resulting in polycrystalline Cs5MA1–xPbI3 perovskite transistors with a four-fold increase in electron mobility compared to that of standard MAPb1 film, in spite of the reduction in the grain size.[149] This outcome is possibly due to the compact nature of the Cs5MA1–xPbI3 perovskite film, such that while the grains were smaller, they were also better connected to one another resulting in improved pathways for charge transport.[149]

In addition to MAPb1, other types of 3D perovskite have gained attention for transistor applications. In 2017, the first perovskite thin film transistor made from MAPbBr3 was fabricated. Using different metals for the source (Au) and drain (Al) electrodes, the transistor exhibited ambipolar transport with room temperature hole mobility of 5 cm2 V–1 s–1 and electron mobility of 3 cm2 V–1 s–1.[150] In 2019, Wang et al. optimized the
MAPbBr$_3$/Au interface using a PFBT treatment and achieved hole mobilities on the order of 10$^{-1}$ at 100 K.$^{[65]}$

Beginning in 2016, triple cation perovskites that combine Cs$^+$, MA$^+$, and HC(NH$_2$)$_2$$^+$ (FA$^+$) have risen to prominence. In 2017, the first FETs fabricated from Cs$_x$(MA$_{0.7}$FA$_{0.3}$)$_{1-x}$Pb(Br$_{0.7}$I$_{0.3}$)$_3$ demonstrated ambipolar transport at room temperature with a hole mobility of $\mu_h = 2.16$ cm$^2$ V$^{-1}$ s$^{-1}$ and an electron mobility of $\mu_e = 2.5$ cm$^2$ V$^{-1}$ s$^{-1}$ as well as a high environmental stability.$^{[153]}$ Subsequently, the performance of these devices was improved with the addition of the crosslinking polymer diethyl-(12-phosphonododecyl)phosphonate (DPP) in the precursor solution, increasing the room temperature hole and electron mobilities to $\mu_h = 4.02$ cm$^2$ V$^{-1}$ s$^{-1}$ and $\mu_e = 3.35$ cm$^2$ V$^{-1}$ s$^{-1}$, respectively.$^{[152]}$ A very exciting development has been the creation of hysteresis-free devices in DPP-doped perovskite FETs by depositing polyethyleneimine ethoxyliated (PEIE) onto the surface of the perovskite.$^{[152]}$ More recently, hysteresis-free devices with high electron mobility have been developed using a different version of the triple cation perovskite (Cs$_{0.2}$FA$_{0.6}$Pb(10$_{0.3}$Pb$_{0.7}$)$_2$) doped with Rb$^+$ to passivate traps in the perovskite bulk and reduce ion migration.$^{[52]}$ Vasilopoulos et al. used higher amounts of Rb$^+$ salts and reported only p-type operation for Rb$_{0.13}$(MAFA)$_{0.87}$PbI$_3$.$^{[153]}$

In 2019, the first transistor based on a low-bandgap mixed-lead–tin perovskite layer, that is, FAPb$_0.5$Sn$_0.5$I$_3$, was demonstrated (Figure 7c).$^{[111]}$ This device operated at room temperature with hole mobility $\mu_h = 0.007$ cm$^2$ V$^{-1}$ s$^{-1}$ and enhanced stability resulting from the reduction in tin-rich clusters. By adding a small amount of the 2D tin perovskite into the 3D formamidinium tin triiodide (FA$\times$SnI$_3$) perovskite, Loi and co-workers managed to reduce the inherent p-doping and enhance the crystallinity of the film, which yielded FET devices with hole mobilities of $\mu_h = 0.21$ cm$^2$ V$^{-1}$ s$^{-1}$ and on/off ratios of $10^5$ at $V_{th} = 2.8$ V.$^{[137]}$ To the best of our knowledge, this represents the first example of a 3D Sn-based perovskite FET, and consisted of bottom Au contacts, a PEFA$_{n-1}$Sn$_n$I$_{2n+1}$ semiconductor layer (with various compositions containing $n = 1, 4$, or 8), and a top gate dielectric consisting of a PMMA/Al$_2$O$_3$ double layer.

An important area of research is that dedicated to single crystal perovskite FETs: single crystals provide a window into intrinsic properties of the material in the absence of grain boundaries and with minimal structural defects; consequently they are expected to exhibit superior charge carrier mobilities and longer carrier diffusion lengths, compared to those of polycrystalline films.$^{[154]}$ Perovskite single crystals are grown using techniques such as crystal seeding and growth,$^{[72]}$ vapor-phase intercalation,$^{[155]}$ gradual solvent evaporation,$^{[156]}$ or anti-solvent vapor-assisted crystallization.$^{[80]}$ The first single crystal 3D MAPbI$_3$ transistors were fabricated in 2015 and demonstrated electron mobilities of $\mu_e = 2.5$ cm$^2$ V$^{-1}$ s$^{-1}$ at 77 K, an order of magnitude higher than the value reported for similar polycrystalline perovskite FETs operating at the same temperature.$^{[57,72]}$ Replacing Au contacts with graphene improved the low-temperature mobilities even further, to 4 cm$^2$ V$^{-1}$ s$^{-1}$.$^{[107]}$ Single crystals of varying thickness were fabricated and used in transistors that were operated in temperatures ranging from 77 K to room temperature in order to investigate the impact of perovskite crystal size on the occurrence of the temperature dependent phase transitions.$^{[10,158]}$ The study revealed that thinner crystals transitioned from the tetragonal to orthorhombic crystal phase at lower temperatures. Amassian and collaborators fabricated single crystal perovskite FETs using MAPbI$_3$, MAPbBr$_3$, and MAPbCl$_3$ crystals and observed ambipolar room temperature charge transport, with $\mu_h = 4.7$ and $\mu_e = 1.5$ cm$^2$ V$^{-1}$ s$^{-1}$ and on/off ratios up to $10^3$.$^{[94]}$ The mobility in MAPbBr$_3$ was later improved to 15 cm$^2$ V$^{-1}$ s$^{-1}$ upon treatment of the electrodes with PFBT.$^{[65]}$

### 3.2.2. 3D Inorganic Perovskite Field-Effect Transistors

Replacing the organic cations MA$^+$ or FA$^+$ by cesium (Cs$^+$) results in the formation of fully inorganic 3D halide perovskite materials: such substitutions have so far only been done on lead-based perovskites, that is, CsPbX$_3$ ($X = $ Cl, Br, I). These materials exhibit higher thermal stability and robustness against moisture-induced degradation as compared to organic cation containing halide perovskites.$^{[159–161]}$ Nevertheless, their processing is less straightforward than that of hybrid halide perovskites, especially in terms of formation of polycrystalline pinhole-free thin films.$^{[88]}$ As a result, at the time of writing, the integration of inorganic lead halide perovskites in field-effect transistors is limited to nanowires and microplatelets. Several groups have demonstrated that CsPbBr$_3$ platelets can be used as active layers in FETs. Hu et al. grew micrometer-scale cubic CsPbBr$_3$ platelets on pre-patterned ITO contacts via a chemical vapor phase (CVP) deposition (Figure 8a)$^{[162]}$ and incorporated them in TGBC FETs with PMMA dielectric. They observed current modulation by the gate-source voltage, but were not able to obtain a unipolar channel needed to evaluate device characteristics (Figure 8b). Huo et al. grew CsPbBr$_3$ platelets in a similar fashion on various substrates, including synthetic mica, Si/SiO$_2$, GaN, and FTO glass and graphene, resulting in squares of cubic CsPbBr$_3$ platelets of several hundred micrometer lengths and a thickness of ~150 nm.$^{[97]}$ FETs were fabricated by transferring the platelets onto pre-patterned Au contacts on Si/SiO$_2$. The hole mobilities in the linear regime reached $\mu_h = 0.32$ cm$^2$ V$^{-1}$ s$^{-1}$ at room-temperature, but the devices showed significant contact effects. Upon cooling, the authors observed an improved performance and reduction in hysteresis, with hole mobilities $\mu_h = 1.0$ cm$^2$ V$^{-1}$ s$^{-1}$. Recently, the same group was able to implement the CsPbBr$_3$ nanoplatelets grown on graphene in vertical field-effect transistors (VFET) that showed much improved contact behavior with an evaporated Ni/Au top contact, however no mobility values were reported.$^{[163]}$

Liu et al. grew CsPbBr$_3$ single crystals in the orthorhombic phase directly from a DMF solution.$^{[164]}$ The authors used silver particles as nucleation centers and were able to bridge two pre-patterned silver electrodes on Si/SiO$_2$ by utilizing capillary forces during the growth, while pressing a polydimethylsiloxane plate onto the solution during the crystal growth. The resulting FETs exhibited p-type transport characteristics with linear mobilities in the range of $\mu_h = 0.5–2.3$ cm$^2$ V$^{-1}$ s$^{-1}$ at 150 K.$^{[164]}$ Another study exploring charge transport in the orthorhombic phase of CsPbBr$_3$ was conducted by Zou et al.,...
who grew micrometer thick CsPbBr$_3$ platelets on Si/SiO$_2$ substrates under capillary forces by melting a polyethylene terephthalate layer below a glass cover.\cite{165} Following the evaporation of gold electrodes, the BGTC FETs exhibited ambipolar charge transport at room temperature with electron transport dominating, with a saturation mobility of $\mu_e = 0.19 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and a saturation hole mobility of $\mu_h = 0.02 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.\cite{165}

Meng et al. grew CsPbX$_3$ (X = Cl, Br, or I) nanowires (NW) by a vapor-liquid-solid (VLS) process in an argon/hydrogen gas stream of an evacuated tube furnace, in which melted Sn particles on Si/SiO$_2$ at 290–330 °C act as nucleation and growth centers for the perovskite nanowires (Figure 8c).\cite{166} The method led to the formation of nanowires several tens of micrometers in length and a diameter of 120–180 nm with a nanometer thin native oxide coating. CsPbBr$_3$ and CsPbCl$_3$ nanowires exhibited a cubic phase, while CsPbI$_3$ nanowires exhibited an orthorhombic phase, confirmed by electron diffraction. After a dry transfer onto the substrate surface and electrode evaporation (Ti, Au) all nanowire transistors exhibited p-type transport properties with a weak ambipolarity and on/off ratios in the range of $\approx 10^3$. The charge carrier mobility extracted in the linear regime increased from Cl to Br to I (Figure 8d), increasing from $\mu_h = 1.06$ to 2.17 to 3.05 cm$^2$ V$^{-1}$ s$^{-1}$, respectively.\cite{166} The authors hypothesized that the dominating p-type transport could either be caused by a high interface trap density for electrons at the native oxide layer of the nanowires or the incorporation of traces of the Sn catalyst and its oxidized species into the nanowires. A follow-up study on CsPbBr$_3$ nanowires was reported in 2020 by the same group, in which the VLS grown nanowires were coated with thermally evaporated MoO$_3$ to form a core shell structure. The molybdenum oxide caused strong p-doping of the CsPbBr$_3$ nanowires, resulting in an increase of the hole mobility and a shift of the threshold voltage towards positive voltages.\cite{167}

Table 2 summarizes the composition, deposition method, device structure and performance parameters of 3D perovskite FETs. To visualize the advances made in both 2D and 3D perovskite FETs, in Figure 9 we include the highest reported room-temperature field-effect mobilities as a function of time of publication, for devices of different architectures and compositions: in blue we include the values obtained in p-type and n-type channel 2D perovskite devices, while in green we show the results on p- and n-type 3D perovskite FETs. These numbers should be regarded with great care because many of them were generated from devices with non-ideal current-voltage characteristics, in which case the mobility extraction methods derived from the gradual channel approximation are not adequate.\cite{37} Nevertheless, the improvement in performance of perovskite FETs is obvious, in particular after the renewal interest sparked by the demonstrations of PVs and LEDs, which are also marked in an inset. Given the large variation in results between different groups, and taking into account the

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**Figure 8.** a) SEM image of a vapor-phase grown CsPbBr$_3$ nanoplate bridging two ITO electrodes. b) Output characteristics of a CsPbBr$_3$ nanoplate FET. Inset is the schematic of the FET. c) SEM images of different individual CsPbBr$_3$ NWs grown with the Sn catalytic seeds. d) Transfer characteristics of the typical single VLS-grown CsPbX$_3$ (X = Cl, Br, or I) NW FETs. Panel (a) and (b) adapted with permission.\cite{162} Copyright 2017, American Chemical Society. Panel (c) and (d) adapted with permission.\cite{166} Copyright 2019, American Chemical Society.
| Year   | Perovskite composition          | Active layer | Temp. | Geometry | Dielectric material | Contact material | $\mu_h$ [cm$^2$ V$^{-1}$ s$^{-1}$] | $\mu_e$ [cm$^2$ V$^{-1}$ s$^{-1}$] | Reference |
|--------|---------------------------------|--------------|-------|----------|---------------------|------------------|-------------------------------|-------------------------------|-----------|
| 2015   | MAPbI$_{3-x}$Cl$_x$             | pc, spin     | RT    | TGBC     | Cytop               | Au/TTFB          | 1.3                           | 1.0                           | [29]      |
| 2015   | MAPbI$_3$                       | pc, spin/anti solvent | 78 K  | BGBC     | SiO$_2$             | Ni/Au            | $2.1 \times 10^{-3}$           | $7.2 \times 10^{-3}$         | [27]      |
| 2015   | MAPbI$_3$                       | pc, spin/anti-solvent | 163 K | BGTC     | SiO$_2$             | Al               | $8 \times 10^{-3}$             |                               | [33]      |
| 2015   | MAPbI$_3$                       | microplate, seeding and growth | 77K   | BGBC     | SiO$_2$             | Au               | 2.5                           |                               | [72]      |
| 2016   | MAPbI$_3$                       | sc, blade coating | 78 K  | BGTC     | SiO$_2$             | Au               | $8 \times 10^{-5}$             |                               | [71]      |
| 2016   | MAPbI$_3$                       | sc, blade coating | RT    | BGTC     | SiO$_2$             | Au               | $8 \times 10^{-6}$             |                               | [71]      |
| 2016   | MAPbI$_3$                       | sc, blade coating | 163 K | BGTC     | SiO$_2$             | Au               | $3.2 \pm 0.7 \times 10^{-2}$   |                               | [71]      |
| 2016   | MAPbI$_3$                       | sc, blade coating | 78 K  | BGTC     | SiO$_2$             | Au               | $4.3 \pm 0.5 \times 10^{-2}$   |                               | [71]      |
| 2017   | MAPbBr$_3$                      | pc, spin     | RT    | TGBC     | SiO$_2$/OTS         | Au and Al        | 5                             | 3                             | [150]     |
| 2017   | MAPbI$_3$                       | pc, spin, thermal cycling | RT    | TGBC     | Cytop               | Au/PEIE          | 0.5                           |                               | [31]      |
| 2017   | MAPbI$_3$                       | pc, spin, thermal cycling | RT    | TGBC     | Cytop               | Au               | 0.1                           |                               | [31]      |
| 2017   | MAPbI$_3$                       | pc, spin     | RT    | TGBC     | Cytop               | Au               | $0.02 \pm 0.01$               |                               | [31]      |
| 2017   | Cs$_x$(MA$_{0.17}$FA$_{0.83}$)$_{1-x}$Pb(Br$_{0.17}$I$_{0.83}$)$_3$ | pc, spin | RT    | TGBC     | SiO$_2$             | Graphene         | ≈1                           |                               | [151]     |
| 2017   | MAPbI$_3$                       | microplate, vapor phase intercalation | 2 K   | BGBC     | SiO$_2$             | Graphene         |                               |                               | [157]     |
| 2017   | MAPbI$_3$                       | microplate, vapor phase intercalation | 160 K | BGBC     | SiO$_2$             | Graphene         |                               |                               | [157]     |
| 2017   | MAPbI$_{3-x}$Cl$_x$             | pc, spin     | RT    | BGBC     | Cytop/protein       | Au               | 0.04                          |                               | [86]      |
| 2017   | MAPbI$_3$                       | microplate, vapor phase intercalation | 80 K  | BGBC     | SiO$_2$             | Graphene         |                               |                               | [93]      |
| 2017   | MAPbI$_3$                       | pc, spin     | 202 K | BGTC     | PMMA                | Au               | 0.056                         |                               | [176]     |
| 2017   | MAPbI$_3$                       | pc, spin     | 202 K | BGTC     | PEMA                | Au               | 0.030                         |                               | [176]     |
| 2017   | MAPbI$_3$                       | pc, spin     | 202 K | BGTC     | PPhMA               | Au               | 0.40                          |                               | [176]     |
| 2017   | CsPbBr$_3$                      | microplate, van-der-Waals epitaxy | RT    | BGBC     | SiO$_2$             | Au               | 0.3                           |                               | [97]      |
| 2017   | CsPbBr$_3$                      | nanoplates, vapor deposition | RT    | TGBC     | PMMA                | ITO              | 0.26                          |                               | [162]     |
| 2018   | MAPbI$_3$                       | pc, deposition | RT    | BGTC     | SiO$_2$             | Au               | 3.55                          |                               | [73]      |
| 2018   | MAPbI$_3$                       | pc, vapor deposition | RT    | BGTC     | SiO$_2$             | Au/MoO$_x$       | 7.47                          |                               | [73]      |
| 2018   | MAPbI$_{3-x}$Cl$_x$             | pc, spin, solvent vapor | RT    | BGTC     | SiO$_2$             | Au               | $10 \pm 2.5$                  | $10 \pm 3.4$                 | [74]      |
| 2018   | MAPbCl$_3$                      | sc, injection/solvent evaporation | RT    | BGTC     | SiO$_2$             | Au               | $1.8 \pm 0.6$                 | $1.3 \pm 0.5$                | [94]      |
| 2018   | MAPbBr$_3$                      | sc, injection/solvent evaporation | RT    | BGTC     | SiO$_2$             | Au               | $1.9 \pm 0.7$                 | $1.1 \pm 0.4$                | [94]      |
| 2018   | MAPbCl$_3$                      | sc, injection/solvent evaporation | RT    | BGTC     | SiO$_2$             | Au               | $1.5 \pm 0.7$                 | $0.7 \pm 0.3$                | [94]      |
| 2018   | MAPbBr$_3$                      | sc, injection/solvent evaporation | RT    | BGTC     | SiO$_2$             | Au               | $2.1 \pm 0.9$                 | $0.27 \pm 0.04$              | [94]      |
| 2018   | MAPbCl$_3$                      | sc, injection/solvent evaporation | RT    | BGTC     | SiO$_2$             | Au               | $2.3 \pm 0.7$                 | $0.19 \pm 0.05$              | [94]      |
| 2018   | MAPbI$_3$                       | sc, injection/solvent evaporation | RT    | BGBC     | SiO$_2$             | Au               | $2.9 \pm 1.0$                 | $1.12 \pm 0.12$              | [94]      |
| 2019   | MAPbI$_3$                       | pc, spin, anti solvent | RT    | BGBC     | AlO$_x$             | IZO              | 0.05                          | $1.25 \times 10^{-4}$         | [141]     |
| 2019   | MAPbI$_3$                       | pc, spin     | RT    | BGBC     | AlO$_x$             | IZO              | 0.05                          |                               | [142]     |
| 2019   | MAPbI$_3$                       | pc, spin     | RT    | BGBC     | AlO$_x$             | IZO              | 0.01                          |                               | [149]     |
| 2019   | Cs$_x$(MA$_{0.17}$FA$_{0.83}$)$_{1-x}$Pb(Br$_{0.17}$I$_{0.83}$)$_3$ | pc, spin | RT    | BGBC     | AlO$_x$             | IZO              | 0.04                          |                               | [149]     |
| 2019   | MAPbBr$_3$                      | sc, antisolvent vapor | 80 K  | BGBC     | SiO$_2$             | Cr/Au/PFBT       | 15                            |                               | [65]      |
| 2019   | MAPbBr$_3$                      | pc, spin     | 100 K | BGBC     | SiO$_2$             | Cr/Au/PFBT       | $=1 \times 10^{-3}$           |                               | [65]      |
| Year  | Perovskite composition                      | Active layer | Temp. | Geometry | Dielectric material | Contact material | μh [cm² V⁻¹ s⁻¹] | μe [cm² V⁻¹ s⁻¹] | Reference |
|-------|---------------------------------------------|--------------|-------|----------|---------------------|-----------------|-----------------|-----------------|-----------|
| 2019  | MAPbBr₃                                     | pc, spin     | 220K  | BGBC     | SiO₂                | Cr/Au/PFBT      | ≈9 × 10⁻⁶       |                 | [65]       |
| 2019  | MAPbBr₃                                     | pc, spin     | 100K  | TGBc     | Cytop               | Cr/Au/PFBT      | ≈2 × 10⁻³       |                 | [65]       |
| 2019  | MAPbBr₃                                     | pc, spin     | 220K  | TGBc     | Cytop               | Cr/Au/PFBT      | ≈2 × 10⁻³       |                 | [65]       |
| 2019  | FAPb₀.₅Sn₀.₅I₃                             | pc, spin     | RT    | BGBC     | SiO₂                | Au              | 3 × 10⁻³        |                 | [111]      |
| 2019  | FA(Pb₀.₅Sn₀.₅)I₃, ZnI₃                    | pc, spin     | RT    | BGBC     | SiO₂                | Au              | 7 × 10⁻³        |                 | [111]      |
| 2019  | MAPbI₁                                     | pc, hot casting | RT | BGBC     | HfO₂                | Ti/Au           | 1 × 10⁻³        |                 | [174]      |
| 2019  | CsPbBr₃                                    | drop casting, refrigeration | RT | BGBC     | SiO₂                | Au              | 7 × 10⁻²        |                 | [182]      |
| 2019  | Cs⁺⁻Ag⁺PbBr₃                               | drop casting, refrigeration | RT | BCTC     | SiO₂                | Au              | 8 × 10⁻⁴        |                 | [182]      |
| 2019  | CsPbBr₃                                    | nanowire, VLS deposition | RT | BCTC     | SiO₂                | Au              | 2.17            |                 | [166]      |
| 2019  | CsPbI₃                                     | nanowire, VLS deposition | RT | BCTC     | SiO₂                | Au              | 3.05            |                 | [166]      |
| 2019  | CsPbClI₁                                   | nanowire, VLS deposition | RT | BCTC     | SiO₂                | Au              | 1.06            |                 | [166]      |
| 2020  | MAPbI₁                                     | pc, spin     | RT    | BGBC     | SiO₂                | AlOₓ             | 0.1             |                 | [143]      |
| 2020  | MAPbI₁                                     | pc, spin, anti solvent | RT | BCTC     | SiO₂/AlOₓ           | Ti/Au           | 18.8 ± 4.4      |                 | [144]      |
| 2020  | MAPbI₁                                     | pc, spin, anti solvent | RT | BCTC     | Kapton/AlOₓ         | Ti/Au           | 11.5            |                 | [144]      |
| 2020  | MAPbI₁                                     | pc, spin     | RT    | TGBC     | Cytop               | Cr              | 1.7 × 10⁻³      |                 | [33]       |
| 2020  | MAPbI₁                                     | pc, spin, C-H-C | RT | TGBC     | Cytop               | Cr              | 4.2             |                 | [33]       |
| 2020  | MAPbI₁                                     | pc, spin     | RT    | TGBC     | Cytop               | Au/PFBT         | 9 × 10⁻³        |                 | [33]       |
| 2020  | MAPbI₁                                     | pc, spin, C-H-C | RT | TGBC     | Cytop               | Au/PFBT         | 2.1             |                 | [33]       |
| 2020  | MAPbI₁                                     | Microplate, solvent intercalation, C-H-C | RT | BGCb     | SiO₂/Cytop          | Au              | 0.9             |                 | [33]       |
| 2020  | Csₓ(MₐₓAₓFₓAₓ)₀.₅₋ₓPbₓBrₓIₓ₋ₓ            | pc, spin, anti solvent | RT | TGCb     | Y₂O₃               | Y               | 2.19 ± 0.14     | 0.33 ± 0.13    | [152]      |
| 2020  | Csₓ(MₐₓAₓFₓAₓ)₀.₅₋ₓPbₓBrₓIₓ₋ₓ (with DPP) | pc, spin, anti solvent | RT | TGCb     | Y₂O₃               | Y               | 3.48 ± 0.30     | 3.17 ± 0.2      | [152]      |
| 2020  | Csₓ(MₐₓAₓFₓAₓ)₀.₅₋ₓPbₓBrₓIₓ₋ₓ (with DPP) | pc, spin, anti solvent, PEIE | RT | TGCb     | Y₂O₃               | Y               | 3.52 ± 0.22     | 3.25 ± 0.13    | [152]      |
| 2020  | FAₙ₋ₓMₐₓAₓBrₓ           | pc, spin     | RT    | TGCb     | Cytop               | Cr/Au           | 0.1 ± 0.03      |                 | [52]       |
| 2020  | Csₓ(MₐₓAₓFₓAₓ)₀.₅₋ₓPbₓBrₓIₓ₋ₓ            | pc, spin     | RT    | TGCb     | Cytop               | Cr/Au           | 0.3 ± 0.05      |                 | [52]       |
| 2020  | Csₓ(MₐₓAₓFₓAₓ)₀.₅₋ₓPbₓBrₓIₓ₋ₓ (with DPP) | pc, spin     | RT    | TGCb     | Cytop               | Cr/Au           | 3 × 10⁻³        |                 | [52]       |
| 2020  | (Csₓ₀.₂₋ₓRbx)₀.₇₀₊ₓMₐₓAₓBrₓ₀.₃₋ₓ         | pc, spin     | RT    | TGCb     | Cytop               | Cr/Au           | 1.2             |                 | [52]       |
| 2020  | FAₙ₋ₓMₐₓAₓBrₓ           | pc, spin     | RT    | TGCb     | Cytop               | Cr/Au           | 5 × 10⁻³        |                 | [52]       |
| 2020  | Faₙ₋ₓMₐₓAₓBrₓ           | pc, spin     | RT    | TGCb     | Cytop               | Cr/Au           | 0.02            |                 | [52]       |
| 2020  | (Csₓ₀.₂₋ₓRbx)₀.₇₀₊ₓMₐₓAₓBrₓ₀.₃₋ₓ         | pc, spin     | RT    | BGCb     | SiO₂                | Cr/Au           | 0.1             |                 | [52]       |
| 2020  | (Csₓ₀.₂₋ₓRbx)₀.₇₀₊ₓMₐₓAₓBrₓ₀.₃₋ₓ         | pc, spin     | RT    | BGCb     | SiO₂/2APTES         | Cr/Au           | 0.3             |                 | [52]       |
| 2020  | FAₙ₋ₓMₐₓAₓBrₓ           | pc, spin     | RT    | BGCb     | SiO₂                | Cr/Au           | 2 × 10⁻³        |                 | [52]       |
| 2020  | FAₙ₋ₓMₐₓAₓBrₓ           | pc, spin     | RT    | BGCb     | SiO₂                | Cr/Au           | 7 × 10⁻³        |                 | [52]       |
| 2020  | (Csₓ₀.₂₋ₓRbx)₀.₇₀₊ₓMₐₓAₓBrₓ₀.₃₋ₓ         | pc, spin     | RT    | TGCb     | Cytop               | Cr/Au           | 0.5             |                 | [52]       |
| 2020  | Rbₓ₁₅(MₐₓFₓAₓ)₀.₈₅₋ₓPbₓ           | sc, spin     | RT    | BGCb     | SiO₂                | Au              | 0.52 ± 0.05     |                 | [153]      |
| 2020  | MAPbI₁                                     | pc, vapor annealing | RT | BGCb     | SiO₂                | Au              | 2 × 10⁻³        |                 | [175]      |
| 2020  | MAPbI₁                                     | pc, vapor annealing | RT | BGCb     | SiO₂                | Au/4-fluorobenzethiol | 0.25          |                 | [175]      |
| 2020  | MAPbI₁                                     | pc, vapor annealing | RT | BCTC     | SiO₂                | Au              | 2.27            |                 | [175]      |
| 2020  | MAPbI₁                                     | pc, vapor annealing | RT | BCTC     | SiO₂                | Au/MoOₓ         | 5.28            |                 | [175]      |
fact that a detailed description of the measurement conditions is quite often missing, and in some cases, it was not clear if the analysis has been performed during the forward or reverse bias conditions, we will refrain from comparison between different materials and device types. It is also noteworthy that important device parameters beyond mobility (e.g., subthreshold swing, threshold voltage) are rarely reported, which makes it difficult to truly assess the quality of the devices.[30,65,72,94,168]

### 3.3. Impact of Dielectric and Electrode Materials on Perovskite FET Performance

The performance of a field-effect transistor is not only dependent on the quality of the semiconductor layer, but also the device architecture and the quality of the interfaces play a critical role in determining the final properties. Processes occurring at the dielectric-semiconductor and electrode-semiconductor interfaces represent an important consideration, and a high-quality perovskite layer alone does not guarantee a high performance. In this section, we review the dielectric and contact materials used in the fabrication of perovskite FETs and discuss their advantages and disadvantages.

#### 3.3.1. Dielectric Materials used in Perovskite FETs

Several different properties must be considered when selecting the dielectric materials for FETs. First, its thickness alongside its dielectric constant ($\varepsilon_r$) directly influence the operating voltages, which can be reduced by decreasing the dielectric thickness, and/or employing dielectric materials with high $\varepsilon_r$ (high-$k$ dielectrics).[169,170] The roughness and the chemical reactivity of the dielectric surface have direct implications on the interfacial trap densities at the perovskite/dielectric interface, where the device channel forms, and hence on the device properties.[171] Although less explored in the context of perovskite FETs, the coefficient of thermal expansion should also be scrutinized given that a severe mismatch in the thermal expansion properties of consecutive device layers has been found to induce performance degradation by means of interfacial microstrain.[100] Additional considerations such as processability or mechanical flexibility become increasingly important as they influence the adopted device geometry (top/bottom gate) and the circumstances under which the transistors can operate. As with many types of FETs, a commonly used dielectric in perovskite FET devices is $\text{SiO}_2$.[172] In addition, $\text{SiO}_2$ is extremely flat (with a roughness on the order of 0.1 nm) – an important trait for the formation of a high-quality interface with the semiconductor films.[173] Other metal oxide dielectrics have been incorporated in perovskite FETs, including several with high dielectric constants such as $\text{Y}_2\text{O}_3$ ($\varepsilon_r = 15$), $\text{HfO}_2$ ($\varepsilon_r = 25$), and $\text{Al}_2\text{O}_3$ ($\varepsilon_r = 9$ for), which promote transistor operation at lower voltages.[144,152,172,174,175]

Polymer dielectrics such as Cytop ($\varepsilon_r = 2.1$), or PMMA ($\varepsilon_r = 4.9$), bring several distinct advantages,[13,65,86,106,120,121,128,151,152] First, their interface with perovskite semiconductors typically yields lower trap densities due to the fact that they are more chemically inert than $\text{SiO}_2$, which, in turn leads to improved device performance.[130,120] Second, their mechanical flexibility opens the prospects for large area flexible device arrays. Third, they are deposited from a solution, and thus unlike $\text{SiO}_2$, are not restricted to functioning in bottom-gate FETs, and can be used to coat the surface of the perovskite film to form top-gate FETs, where they also serve as an encapsulation layer, prolonging the device lifetime and improving performance.[133] However, care should be taken when considering polymer dielectric for bottom gate devices, as it has been demonstrated that $\text{Pb}^{2+}$ in
the precursor can interact with the polymer (either through the electronegative oxygen or phenyl groups) hampering the formation of high quality films.\[156\]

3.3.2. Source-Drain Electrodes used in Perovskite FETs

A wide variety of contact materials has been tested in perovskite FET fabrication, including Ag, Al, InZnO (IZO), InSnO (ITO), Pd, Pt, Cr, Y, and graphene.\[27,103,109,152,177,178\] The most common choice remains Au, or Au chemically treated with SAMs.\[17,30,33,93,109,152,177,178\] 2D polycrystalline perovskite FETs made using Au contacts (no treatments or interlayers) demonstrated only p-type transport.\[120,130,135\] 3D perovskite devices based on MAPbI$_3$ and MAPbI$_3$.Cl$_x$ with untreated Au contacts have shown ambipolar transport,\[27,74\] but also pure n-type\[31,52\] and p-type devices were reported in similar device structures, highlighting the complexity of the FET operation and the fact that the simply selecting the electrode material based on energy level alignment does not guarantee efficient selective injection. Au has had a long reputation as a non-reactive metal, however there is recent evidence that suggests that hybrid perovskites can, in fact, react electrochemically (or thermochemically) with Au and create species like (MA)$_2$Au$_2$I$_6$ (for the case of MAPbI$_3$)\[79\] or AuBr$_3$ (with MAPbBr$_3$),\[65\] as will be discussed more in detail in Section 5.4. Y, Cr, IZO, ITO and graphene represent promising alternatives as robust contact materials, where such reactions do not occur.\[91,141-143,149,152,158,159\]

A solution to the Au interface reactivity problem is treatment with a SAM or insertion of an interlayer.\[65\] In addition to acting as a physical barrier to electrochemical degradation, these chemical functionalizations allow for the tuning of the injection barrier at the semiconductor/contact interface and, in some cases, assist with improving the perovskite film microstructure by modifying the surface energy.\[31,65,86\] The application of PEIE or PFBT to electrodes prior to MAPbI$_3$ precursor deposition has led to an increase in grain size, better mobility and a reduction in hysteresis.\[31,33,181\] The evaporation of an C$_{60}$ interlayer between the electrode metal and perovskite resulted in a transition from a p-type transport to a n-type transport in PEA$_2$SnI$_4$ FETs.\[121\] The MoO$_x$ interlayer also resulted in enhanced hole transport in both MAPbI$_3$ and PEA$_2$SnI$_4$ transistors.\[120,175\] The range of electrode and dielectric materials compatible with perovskite FET fabrication allows for substantial tuning of properties, even when the perovskite active layer remains the same. For example, by retaining the same BGTC architecture and changing the dielectric from SiO$_2$ to Al$_2$O$_3$ and the contact metal from Au to MoO$_x$, the mobility of the MAPbI$_3$ FETs was increased from 2.27 to 21.41 cm$^2$V$^{-1}$s$^{-1}$.\[175\]

3.4. Perovskite-Based Memory Transistors

Several examples demonstrating memory transistors that are based on metal halide perovskites have been reported recently, utilizing two different concepts for non-volatile storage. Hague et al. exploited ion migration in dendritic MAPbI$_3$ films to form high and low resistive states via gate voltage modulation. Switching ratios (high/low) in the range of 100 and retention times of 10$^4$ s were demonstrated, but the operating window for such devices remained relatively small.\[158\] Lee and co-workers utilized BA$_2$PbBr$_4$ perovskite coated with sputtered indium zinc tin oxide (IZTO) in memory transistors that can be switched from a high-resistance state to a low-resistance state following the application of a light pulse for several seconds.\[184\] The authors showed that both the wavelength and duration of the light exposure determine the achievable current ratio between the two states, which can be as high as 10$^6$. The devices could be erased electrically and showed retention of their low resistive state after illumination for more than 1000 s.\[184\]

A superior performance was achieved by Vasilopoulos et al. who utilized single crystalline Rb$_{0.15}$(MAFA)$_{0.85}$PbI$_3$ on top of an organic ternary blend layer as floating gate. Gate voltage dependent tunneling of holes from the perovskite into the fullerene-polyfluorene organic blend through the insulating polystyrene component enabled memory transistor operation with a wide operating voltage window and memory on/off ratios as high as 10$^7$. The devices exhibited good retention of their programmed state for up to 10$^6$ s.\[153\] Geda et al. investigated a blend of (PEA)$_2$PbBr$_4$(2,7-dioctyl[1]benzothieno[3,2-b]benzoannephenylene) (C$_{60}$-BTBT) for memory application. In this 2D Ruddlesden-Popper perovskite, the lead bromide layers separated by the insulating organic cations acted as floating gate and allowed effective trapping/de-trapping of holes depending on the applied gate voltage.\[185\] The authors demonstrated stable performance after over 10 000 read/write cycles with a high operating window. Retention times exceeded 55 000 s and the switching ratio were always above 10$^4$. These two examples of tunneling charge trapping memory devices exhibited switching times in the range of 50–200 ms that should be further improved to compete with state-of-the-art flash memory devices.

3.5. Perovskite-Based Phototransistors

With their unique optoelectronic properties and cost-effective processing, perovskites are well-suited to many optoelectronic applications.\[2,5,24\] A particularly exciting example is the phototransistor: similar to the case of photodiodes and photococonductors, in phototransistors light absorption generates excitons and trions in the perovskite layer, which dissociate in the presence of an external electric field, resulting in free charges that are collected at the electrodes as photocurrent.\[186,187\] In addition, phototransistors modulate the signal current via the gate-source voltage, allowing for a higher sensitivity compared to the two terminal photodetectors. In this section, we will summarize the most notable developments in perovskite phototransistors. For a recent review dedicated solely to perovskite phototransistors, we refer to the manuscript by Xie et al.\[188\] In addition to the figures of merit found in FETs, the phototransistors are also described in terms of properties that quantify their interaction with light, namely responsivity (R), detectivity (D*$^*$), and $t_{rise}$ and $t_{decay}$. The photoresponsivity, or responsivity (R), is defined as:

\[
R = \frac{I_{light} - I_{dark}}{P \times A}
\] (6)
where $I_{\text{light}}$ is the current under illumination, $I_{\text{dark}}$ is the current in the dark, $P$ is the intensity of the incident light, and $A$ is the active area of the device. The detectivity ($D^*$) is calculated from the expression:

$$D^* = \frac{R \times \sqrt{A}}{\sqrt{2 \times I_{\text{dark}} \times q}}$$

(7)

where $q$ represents the elementary charge. The time response of the phototransistors is captured by the values $t_{\text{rise}}$, defined as the time it takes for the current to increase from 10% to 90% of its maximum value under illumination, and $t_{\text{decay}}$, defined as the time it takes for the current to decrease from 90% to 10% of its maximum value.

3.5.1. Perovskite-Only Phototransistors

The first 2D perovskite phototransistor was fabricated in 2016 using PEA$_2$SnI$_4$ thin films and the characteristic responsivities were $R = 1.9 \times 10^4$ $\text{A W}^{-1}$ under 447 nm illumination with light power density of $5 \times 10^{-3}$ mW cm$^{-2}$, with a $t_{\text{rise}} = 0.45$ s (Figure 10a).\textsuperscript{[189]} By using the ferroelectric polymer poly(vinylidene fluoride-trifluoroethylene) as gate dielectric, Wang et al. exploited the change in dielectric polarization with the applied electric field and developed PEA$_2$SnI$_4$ phototransistors with $R = 14.57$ A W$^{-1}$, $D^* = 1.74 \times 10^{12}$ Jones, and a $t_{\text{rise}}$ ($t_{\text{decay}}$) of 50 ms (1.5 s) under 470 nm illumination with a light power density of $2.1 \times 10^{-3}$ mW cm$^{-2}$.[190] Zhu et al. further enhanced the performance of (PEA)$_2$SnI$_4$ by improving the microstructure of the perovskite through solvent engineering and demonstrated phototransistors with $R = 1.6 \times 10^3$ A W$^{-1}$, $D^* = 3.2 \times 10^{17}$ Jones under 532 nm light with light power density of 0.3 $\mu$W cm$^{-2}$ exceeding those of Si or InGaAs photodiodes.[191]

In 2020, a single crystal 2D perovskite phototransistor was made from (C$_4$H$_9$NH$_3$)$_2$(CH$_3$NH$_3$)$_2$Pb$_2$I$_7$ perovskite and this device displayed $R$ values ranging from $5.3 \times 10^{-3}$ to 1.29 A W$^{-1}$ as $V_{\text{GS}}$ was tuned from 0 to 100 V under 473 nm light with a light power density of 85.7 mW cm$^{-2}$.[108]

In 2015 Li et al. developed MAPbI$_3$ and MAPbI$_3$–xCl$_x$ 3D phototransistors with $t_{\text{rise}}$ and $t_{\text{decay}}$ times of 6.5 and 5.0 $\mu$s, respectively; these devices demonstrated a responsivity that...
could be tuned by 4 orders of magnitude with the application of a gate voltage (Figure 10b).\[28\] While the dark electron and hole mobility values of devices made from MAPbI$_3$Cl$_x$ were higher than those of MAPbI$_3$ devices, the responsivity was inferior ($R = 47$ A W$^{-1}$ compared to $R = 320$ A W$^{-1}$ under a light power density of 10 mW cm$^{-2}$).\[28\] This result was attributed to the higher dark current caused by a higher mobility of the MAPbI$_3$Cl$_x$. Similarly, single crystal MAPbI$_3$ phototransistors with an electron mobility of 2.5 cm$^2$ V$^{-1}$ s$^{-1}$ exhibited a lower responsivity of $R = 7$ A W$^{-1}$.[72] For comparison, the highest electron mobility value reported for thin films of MAPbI$_3$Cl$_x$ was 1.17 × 10$^{-4}$ cm$^2$ V$^{-1}$ s$^{-1}$.[28] However, in 2018, Cao et al. found that by fine tuning the preparation and temperature used for film annealing, MAPbI$_3$Cl$_x$ yielded an order of magnitude increase in mobility and responsivity, (with a maximum responsivity $R = 32$ A W$^{-1}$), accompanied by a faster temporal response, $t_{rise}$ (which improved from 335 to 42 ms) and $t_{decay}$ (which improved from 298 to 76 ms), as measured using a 405 nm illumination at a power density of 1 mW cm$^{-2}$.[192]

The charge carrier anisotropy present in MAPbI$_3$ also impacts the phototransistor performance, with two orders of magnitude difference in responsivity being observed between devices where the channel was parallel versus perpendicular to the long axis of the crystal obtained by directional growth (6.1 A W$^{-1}$ vs 0.047 A W$^{-1}$ respectively under white light of power density 0.5 mW cm$^{-2}$).[71] In 2020, Haque et al. reported on ambipolar BGBC MAPbI$_3$ phototransistors and characterized the photoresponse devices under p- and n-type operation.[196] $R = 0.36$ A W$^{-1}$ (0.22 A W$^{-1}$) respectively under white light of power density 0.5 mW cm$^{-2}$, $D^* = 3.1 × 10^{15}$ Jones (1.6 × 10$^{15}$ Jones), $t_{rise}$ = 100 ms (200 ms) and $t_{decay}$ = 100 ms (300 ms) were measured under white light intensities of 1.2 × 10$^{-4}$ W cm$^{-2}$ for p-type and n-type channels, respectively. Khorramshahi et al. developed phototransistors that operated in depletion mode and exhibited hole mobilities of 1.7 cm$^2$ V$^{-1}$ s$^{-1}$ and $R = 1.4 × 10^{-2}$ A W$^{-1}$ under white light with light power density of 80 mW cm$^{-2}$.[195]

These results exemplify the tremendous possibilities that lie ahead for the development of efficient phototransistors based on perovskite materials. While the performance demonstrated to date is promising, many challenges such as operational and environmental stability, high-yield, and large-scale fabrication remain to be overcome prior to the possibility of integrating perovskite phototransistors in industrial applications and significantly more research should be dedicated to resolving these outstanding issues.

### 3.5.2. Heterostructure Phototransistors

The photogain and dark current are strongly coupled, which makes the development of high-performance phototransistors extremely difficult. One strategy for resolving this challenge is to combine perovskites with other materials and create heterostructured phototransistors. In these multicomponent devices, each material serves a different functional purpose: light is absorbed through one material, the photogenerated charge carriers are then extracted into the second material (a process that is highly dependent on the energy level offset of the two materials and the properties of their interface) then the free charges are used to generate electrical signals modulated by the gate-source voltage of the transistor. Heterostructure transistors have been developed both in the form of composites (bulk heterojunctions) and bilayers, with the aim to enhance charge separation and collection and expand the wavelength range. Highly sensitive phototransistors have been demonstrated by blending perovskites with single-walled carbon nanotubes (SWNTs).[196] nitrogen-doped graphene quantum dots (NGQDs),[197] organic semiconductors,[198,199] or 2D semiconductors.[200] In 2017, a bulk heterojunction of MAPbI$_3$ and nitrogen doped graphene oxide to create phototransistors with $R = 1.92 × 10^4$ A W$^{-1}$ and $D^* = 2.71 × 10^{10}$ Jones measured under 660 nm illumination with a light power density of 2.4 × 10$^{-2}$ mW cm$^{-2}$.[197] In 2018, MAPbI$_3$ was used with MoS$_2$ in a bulk heterojunction to create phototransistors that when measured under 660 nm illumination with a light power density of 5.3 × 10$^{-7}$ W cm$^{-2}$ displayed $R$ values of 1.08 × 10$^4$ A W$^{-1}$ and a $D^*$ of 4.28 × 10$^{10}$.[200] These studies exemplify that the simple solution-processing of perovskite materials offers the possibility for their combination with a broad range of semiconductors in a bulk heterojunction architecture, thus serving as a potential route to enhance the performance of these devices.

In bilayer phototransistors, given the fact that the FET channel at the interface with the dielectric is only a few nm thick, the perovskite layer can either serve as a light absorbing medium, or as a charge transporting medium, but not both. Due to their high absorption coefficients, perovskites have been frequently used as the photoactive component in phototransistors, while the conductive channel was formed in the complementary material.[195,197,199,200–209] The results were remarkable; however, since the perovskite layer does not effectively participate in the electrostatic gating process, we consider that such phototransistor architectures should not be categorized as perovskite phototransistors. Unfortunately, many articles are elusive, in particular in their titles, which often leaves ambiguity as to the nature of the devices (perovskite vs heterostructure phototransistor) and the respective roles of the constituent layers. This language can be imprecise, and the field as a whole would benefit from clearer descriptions of the device architecture.

We will first focus on the few rare examples of heterostructured phototransistors where the perovskite layer is responsible for the transistor operation. In 2017, a phototransistor was made by layering quantum dots of PbSe on top of MAPbI$_3$, resulting in a $R$ of 1.2 A W$^{-1}$, $D^*$ of 3.3 × 10$^7$ Jones and a $t_{rise}$ ($t_{decay}$) of 2.5 ms (3 ms) under 300 nm light.[201] In 2019, FA$_{0.85}$Cs$_{0.15}$PbI$_3$ was used together with dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) to make a phototransistor with $R = 778$ A W$^{-1}$ under 450 nm at 4 × 10$^{-6}$ W cm$^{-2}$ with a $t_{rise}$ ($t_{decay}$) of 1.1 ms (2.0 ms).[211] Considering that very few examples of such devices exist, it is clear that many other absorbing materials can be explored in combination with perovskite layers to yield further improvements in the device performance of heterostructured perovskite phototransistors.

On the other hand, perovskites have been paired as light absorbing mediums with different materials in heterostructured phototransistors. A popular choice is graphene due to its high charge carrier mobility.[212] With graphene as charge...
transport medium and MAPbI₃ as light absorber; the resulting device showed a responsivity of \( R = 180 \, \text{A/W} \), a detectivity of \( D^* = 1.1 \times 10^{10} \, \text{Jones} \), and \( t_{\text{rise}} \) of 87 and 540 ms, respectively, when measured under 532 nm illumination at 2 mW cm⁻².[209] Phototransistors made of MAPbI₃ nanowires on top of a layer of graphene exhibited a \( R = 2.6 \times 10^{6} \, \text{A/W} \) at 633 nm with a light power density of \( 6.5 \times 10^{-5} \, \text{mW cm}^{-2} \), but the response times were longer, with \( t_{\text{rise}} \) of 55 s (75 s) – a change attributed to the non-uniform interface between the nanowires and the graphene.[201]

A dual halide perovskite, (MAPbBr$_3$I), was also used in combination with graphene and resulted in a phototransistor with \( R = 6 \times 10^{5} \, \text{A/W} \) under 1 nW 405 nm illumination as well as rise and decay times of 0.12 and 0.75 s, respectively.[208] A further improvement in responsivity was achieved by vapor depositing the perovskite layer on graphene; these devices exhibited \( R = 1.73 \times 10^{7} \, \text{A/W} \) and \( D^* = 2 \times 10^{15} \, \text{Jones} \) under white illumination with a light power density of \( 133 \times 10^{-9} \, \text{W cm}^{-2} \).[202] By transitioning to a trilayer phototransistor structure, where graphene was adjacent to the dielectric, MAPb$_{1−x}$Cl$_x$ was the light absorbing layer, and a poly(3-hexylthiophene) (P3HT) film was deposited between them to enhance exciton separation,[206] a responsivity of \( 4.3 \times 10^{9} \, \text{A/W} \) with 598 nm illumination at \( 1.4 \times 10^{-5} \, \text{mW cm}^{-2} \) was demonstrated, along with \( t_{\text{rise}} \) on the order of 1 s.[206] Graphene was also paired with 2D perovskites in heterostructure phototransistors. The 2D perovskite \((\text{BaI}_{2/3}\text{MA})_{1−x}\text{PbI}_{3+x}\text{Cl}_{x}\) was used with graphene as the charge transport layer and hexagonal boron nitride (hBN) to preserve the high mobilities of graphene and achieved a \( R = 1 \times 10^{5} \, \text{A/W} \), a \( D^* \) of \( 10^{13} \, \text{Jones} \) under \( 532 \, \text{nm illumination at a light power density of 0.8 mW cm}^{-2} \), and a \( t_{\text{decay}} \) of 189.8 ms.[207]

Organic semiconductors represent another choice of charge transporting materials in bilayer phototransistors where perovskites absorb the electromagnetic radiation. For example, using FA$_9$xCl$_x$PbI$_{3−x}$Br$_{0.5}$ and the polymer indacenodithiophene benzothiadiazole (C$_{31}$IDTBT) adjacent to a teflon dielectric,[193] resulted in devices with a gate-modulated photoresponse reaching values as high as \( R = 1.7 \times 10^{6} \, \text{A/W} \), \( D^* = 2.2 \times 10^{14} \) and \( R = 3.2 \times 10^{3} \, \text{A/W} \), \( D^* = 3.8 \times 10^{13} \, \text{Jones} \), respectively have been demonstrated (all values measured under light power densities of \( 7 \times 10^{-3} \, \text{mW cm}^{-2} \), see Figure 10c).

There are also other materials that show promise in bilayer devices; when transition metal dichalcogenides have been used as the carrier transport layer, the resulting device had \( R = 1.94 \times 10^{6} \, \text{A/W} \) and \( D^* = 1.29 \times 10^{12} \, \text{Jones} \) at 520 nm and a light power density of 0.17 mW cm⁻².[213] Another class of materials tested as charge carrier transport layer is represented by metal oxides. In 2019, a vertical heterojunction was made with SnO adjacent to the dielectric and MAPbI₃ as the optically active layer. The R of the resulting phototransistor was \( 1.83 \times 10^{5} \, \text{A/W} \) and the \( D^* \) was \( 2.1 \times 10^{11} \, \text{Jones} \) measured under 655 nm illumination of \( 1 \times 10^{-3} \, \text{mW cm}^{-2} \).[206] The \( t_{\text{rise}} \) and \( t_{\text{decay}} \) were 16.9 ms and 1.1 ms, respectively. It is noteworthy that while metal oxides are typically more stable than organic or perovskite materials, deposition of perovskite layers on certain metal oxides can lead to partial decomposition of the perovskite layer,[214,215] suggesting special care should be applied in investigating such heterostructures. Black Phosphorous has also been used with MAPbI$_{3−x}$Cl$_x$ to create phototransistors with \( R \) values as high as \( 2.0 \times 10^{9} \, \text{A/W} \) and \( D^* \) as high as \( 9 \times 10^{10} \, \text{Jones} \) when measured under visible light with a power density of \( 4 \times 10^{-4} \, \text{mW cm}^{-2} \) and \( t_{\text{rise}} \) and \( t_{\text{decay}} \) of 2.5 and 19.1 s, respectively.[203]

### 4. Comparison of Perovskite FET Mobility with Values Obtained by Other Methods

The charge carrier mobilities extracted from perovskite FET measurements are clearly inferior to those achieved by other methods. For example, in MAPbI₃ and its analogous MAPb$_{1−x}$Cl$_x$ – one of the most intensely studied perovskite systems – the highest reported field-effect mobility values are \( \mu_{\text{FET}} = 20 \, \text{cm}^{2}\text{V}^{-1}\text{s}^{-1} \) while values as high as \( \mu_{\text{THz}} = 800 \, \text{cm}^{2}\text{V}^{-1}\text{s}^{-1} \) were obtained by terahertz (THz) spectroscopy,[25] space charge limited current (SCLC),[154] and Hall effect measurements,[154] respectively. Such a significant difference cannot be explained solely by sample-to-sample variations or differences in material quality, raising fundamental questions regarding the origin for these noteworthy discrepancies. Possible causes include the fact that the different techniques probe different length scales within the semiconductor and encompass a wide range of charge density regimes. Certain method-specific assumptions that are required in cases where a direct access to mobility is not possible further complicate the analysis. The quality of contacts, which impacts the efficiency of charge injection and collection, and the presence of ion migration, which alters the electric field within the perovskite layer, are not accounted for in the models adopted for mobility determination, limiting the reliability of mobility values extracted from electrical measurements. These issues can indeed be avoided by employing non-contact methods such as optical pump terahertz and microwave conductivity, but unfortunately these techniques can only probe short-range conduction, and thus are not able to provide information which is applicable to device-relevant length scales.[26] FET characterization is one of the very few methods that provides direct access to the long-range charge carrier mobility, but only if ionic motion is correctly considered, either by characterization at low temperatures[27,28] or by eliminating the hysteresis,[32,24] and if the contact effects are minimized.[29,24,4,12] Therefore, as long as the FET operation follows the gradual channel approximation, which is at the basis of the models adopted for mobility calculations,[104,105,216] perovskite FETs allow the simultaneous determination of the charge carrier mobility and the nature of transport (p-or n-type) reliably and with high accuracy. This mobility value represents a lower limit since it reflects the surface properties, where the higher defect density compared to the bulk makes charge transport less efficient.

With FETs offering only the lower limit of mobility, it is important to identify the fundamental limits of mobility in perovskites materials. Their low effective masses, obtained both theoretically and experimentally[23,17,28] and from par with Si or GaAs. This, together with the characteristic low disorder suggested by the small Urbach tail energies[1,19,220] and low trap
densities[221] is consistent with that expectation of very high charge carrier mobilities based on the Drude’s model: \( \mu = \frac{q \tau}{m^*} \), where \( q \) is the elementary charge, \( \tau \) represents the carrier scattering time and \( m^* \) the effective mass. To estimate the value of \( \tau \) one has to consider the dominant scattering processes in perovskite materials. Since extrinsic effects such as impurities, and other sources of trapping disorder have been reduced by careful processing, as confirmed by the small disorder, charge scattering effects must be intrinsic in nature. Indeed, interaction with the lattice has been acknowledged as the dominating scattering process.[92] When accounting for the longitudinal optical (LO) phonon as the only type of scattering, a mobility of \( \mu = 200 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1} \) was predicted in MAPbI\(_3\), however scattering can also arise from acoustic phonons. Moreover, polaronic effects, lattice polarization, structural fluctuations and dynamic disorder due to organic cation rotation around its axis and PbX\(_2\) octahedral distortions will also contribute to a reduction in mobility, hence this value should be regarded as an upper limit for the long-range mobility.[26,92,223–225]

Space charge limited current (SCLC) measurements performed on perovskite single crystals approach this limit. While single crystals present the most pristine form of a material, in which transport is not limited by grain boundaries and other defects, SCLC mobility determination relies on the use of the Mott–Gurney law, which is based on the assumption of unipolar injection. The presence of both carrier types limits the validity of standard models and makes it necessary to invoke more complicated physics.[226] Unlike techniques like Hall effect, Seebeck effect, or FET measurements, SCLC cannot distinguish if electron, hole, or ambipolar transport occurs. While one may assume that by selecting a certain type of contact, it is possible to selectively inject only one of the two charge carrier types due to the formation of a large injection barrier for the other charge carrier type, in reality, this is not straightforward. For example, based on their energetics, MAPbI\(_3\) with Au contacts should exhibit exclusively p-type transport. However, many reports have shown that ambipolar, or even electron-only injection is possible in MAPbI\(_3\) FET devices with Au contacts.[31,33,72,74]

Clearly, the energy band diagram does not guarantee the injection of a certain carrier type, and complementary measurements are imperative to confirm that ambipolar transport does not occur in SCLC measurements. Otherwise, SCLC-derived mobilities might be overestimated due to the fact that both carrier types are present simultaneously and hence, the prerequisite of unipolar transport is not fulfilled.

Hall effect measurements have the advantage that they can univocally determine the mobility and the nature of the majority charge carrier (through the sign of the Hall voltage), but may also suffer from artefacts due to the poor signal to noise ratio, often characteristic to such measurements. The implementation of Faraday-induction corrected a.c. Hall measurements, coupled with a 4-point measurement to eliminate contact effects, resulted in a maximum single crystal bulk mobility between 1–10 cm\(^2\)V\(^{-1}\)s\(^{-1}\) in a rigorous study reported by Podzorov and collaborators. This value suggests that the results obtained in FETs (see Figure 9) have quite possibly reached the upper limits accessible in these devices.

5. Challenges in Perovskite FET Research and Insights from Perovskite Optoelectronics That Can Address Them

While the functionality of perovskite field-effect transistors differs from that of other perovskite optoelectronic devices such as light-emitting or photovoltaic diodes, they share several common challenges. This section will describe some of these challenges and discuss which insights can be adopted from optoelectronic perovskite devices to further advance the field of perovskite FETs.

5.1. Hysteresis

The presence of hysteresis in current–voltage measurements was largely underreported in the early days of perovskite research. For example, while the research on perovskite solar cells commenced with the seminal work by Miyasaka and coworkers in 2009,[9] anomalous hysteresis in PV devices was reported for the first time only in 2014.[41] Similarly, while the first perovskite light-emitting diodes were demonstrated in 2014,[8] only few studies investigated hysteresis in these devices,[227] and many recent works still do not report both scan directions.

Interestingly, hysteresis in perovskite FETs was observed—and reported—in some of the earlier studies examining the 2D perovskite structure PEA\(_2\)SnI\(_4\) in 2001[122] and 2004.[124] The authors speculated that the presence of ionic impurities in their perovskite films is responsible for the hysteretic behavior observed in the transfer curves of their devices. More recent studies of perovskite FETs based on the same perovskite composition also report on the existence of hysteresis in both the output and transfer characteristics.[120]

Several approaches were shown to be particularly effective in suppressing hysteresis in 2D perovskite FETs. Matsushima et al. found that the incorporation of a SAM containing ammonium iodide terminal groups (NH\(_3\)I–SAM) can eliminate the hysteresis in FETs, in which the NH\(_3\)I–SAM was used to modify the substrates on top of which the perovskite layer was deposited.[120] Considering that this effect was observed in both bottom and top gate devices, it is likely that the interfacial modification led to a better film formation, rather than passivation of the transistor channel (Figure 6b). Interestingly, when the same SAM was incorporated in n-type PEA\(_2\)SnI\(_4\) transistors, a small, but non-negligible, hysteresis was present in the output characteristics of the devices (Figure 6c).[121] It was suggested that the high density of electron traps in the perovskite films is responsible for the hysteresis and the inferior performance of the devices.

In another example, Gao et al. have demonstrated that by replacing the C\(_6\)H\(_5\)C\(_2\)H\(_4\)NH\(_3\)+ cation with a \( \pi \)-conjugated oligothiophene ligand, the hysteresis of the resultant 2D perovskite FETs was substantially reduced.[135] The authors speculated that this effect is associated with an improved film microstructure and a reduced trap density in the perovskite films, as well as an inhibited ion migration due to the large size of the organic cations.
The processing method of the perovskite layer also impacts hysteresis. For example, transistors based on thermally evaporated PEA3SnI5 perovskite exhibited a larger hysteresis than solution-processed devices accompanied by a lower FET performance. A similar trend was observed in thermally evaporated perovskite solar cells, whose performance currently lags behind that of solution-processed devices, and the observation of hysteresis in the former is far more frequent. Single crystalline transistors based on the same perovskite composition exhibited essentially no hysteresis, highlighting the importance of the microstructure of the perovskite active layer and in particular the role of grain boundaries. Zhu et al. have shown that by increasing the stoichiometry of PEAI to SnI2, the grain boundaries could be passivated by the excess PEAI, leading to an improved FET performance with a somewhat reduced hysteresis. Further reduction of hysteresis was achieved by exposure to trace amounts of oxygen, which passivates iodine vacancies in the perovskite layer and thus reduced the density of defects in the active layer. Li et al. explored the hysteresis in 2D perovskite FETs with different number of inorganic layers. By varying the ratio of the organic cations butylammonium (BA) and methylammonium (MA), the authors fabricated FETs using (BA)2(MA)n−1PbnI3+n perovskites with n = 1, 2, and 3. They found that while all their devices exhibited hysteresis, this was enhanced with increasing n. The larger hysteresis was associated with increased ionic motion for 2D perovskites with more inorganic layers. These results are in agreement with the large hysteresis often observed in 3D perovskite FETs. Unlike 2D perovskites, in which hysteresis is associated mostly with trapping/detrapping of charges at the interfaces or grain boundaries, ion migration (described in Section 2.1) in 3D perovskite FETs is a strong contributing factor to hysteresis in these devices. Such ion migration can be at least partly suppressed by characterizing the FET at low temperatures, which became relatively common in early works examining 3D perovskite FETs. For example, a study by Chin et al. showed that reducing the measurement temperature reduces hysteresis, however even when measuring at 78 K, a significant hysteresis was present in both the output and transfer curves of spin-coated MAPbI3 FETs. Similarly, large hysteresis was also observed in FETs based on MAPbI3 perovskite crystals blade-coated MAPbI3 perovskite films and microplate crystals even when measured at low temperatures (Figure 11). These observations suggest that while ionic motion plays an important role in affecting the hysteresis of the device, other factors such as trapping/de-trapping processes and the presence of surface dipoles also contribute to hysteresis in these devices, not unlike the situation in 2D perovskite FETs.

In fact, most current perovskite solar cells do not display hysteresis, owing to the meticulous optimization of both the quality of the perovskite layer, as well as the interfaces with other device layers, despite ion migration still being present in the devices. Similarly, optimization of the microstructure and interfaces in perovskite FETs has also been demonstrated to lead to a reduction in hysteresis. For instance, Sirringhaus and coworkers optimized the film morphology in MAPbI3 by employing surface treatments and demonstrated room temperature operation with essentially no hysteresis. Interestingly, the authors still observed hysteresis when the devices were measured at low temperature, which they assigned to the presence of traps at the interface to the dielectric, rather than ion migration. Later, the same group suggested that the hysteresis observed at low temperatures arises from the strong dipolar nature of the MA+ cation. Indeed, by replacing MA+ with FA+, which has a lower dipole moment, the hysteresis at low temperatures was almost eliminated. More importantly, they reported on a general approach to fabricate hysteresis-free perovskite FETs by incorporating small amounts of Cs or Rb in the perovskite composition and the treatment of perovskite layer with Lewis bases or acids.

Several more recent studies also reported on the elimination of hysteresis of perovskite FETs. Canicoba et al. fabricated MAPbI3 on a HfO2 dielectric using the hot casting method which results in large grain sizes, leading to transistors with negligible hysteresis. Kim et al. reported on hysteresis-free Cs0.05(MA0.17FA0.83)0.95Pb(Br0.17I0.83)3 transistors that have been cross-linked by adding DPP to the perovskite precursor solution, and passivating the perovskite layer by a thin layer of PEIE. In both these studies the absence of hysteresis was explained by the high-quality of the perovskite layer with a controlled microstructure and well passivated interfaces. She et al. recently developed a solvent-based surface passivation process that resulted not only in an increase in device performance, but also in the suppression of hysteresis for a broad range of perovskite compositions, demonstrating the great versatility of their approach.

Despite the progress made in the field of perovskite phototransistors (Section 3.5), only a few studies explored the
hysteresis of these devices in detail. Particularly noteworthy is the exceptional work by Sun et al., which characterized in detail the hysteresis of MAPbI3 phototransistors as it is influenced by the application of external voltages and modulation of monochromatic light. The authors demonstrated that the hysteresis is sensitive to the choice of excitation wavelength, thus opening the route to a potentially new family of photomemory devices.

5.2. Operational Stability

As with any field in its infancy, the current focus of the perovskite FET research is on increasing the device performance and detailed studies of FET operational stability are scarce. However, several studies discuss certain aspects of device instabilities that highlight the challenges that lie ahead. For example, Adachi and coworkers reported that biasing a thermally deposited PEA2SnI4 FET for 10 minutes at $V_{GS} = V_{DS} = -40$ V led to a reduction in channel current by approximately two orders of magnitude. This decrease was associated with ion accumulation at the dielectric/gate interface and could be reversed almost entirely by applying a positive bias of the same magnitude. The same group observed a significantly improved bias stability in single crystals of similar perovskite composition. The FET performance remained unchanged upon biasing the device at $V_{GS} = V_{DS} = -50$ V in vacuum for a period of 1 h.

Recently, Zhu et al. compared the bias stress stabilities of PEA2SnI4 solution-processed FETs fabricated with different Lewis bases under $V_{GS} = V_{SD} = -40$ V for 2000 s. Devices made using oxygen containing Lewis bases such as DMSO, N-Methyl-2-pyrrolidone (NMP), γ-butyrolactone (GBL) showed a 40% reduction in the source-drain current over this period of time, while those containing nitrogen containing bases, pyridine and acetonitrile, were stable, with the latter even resulting in an improvement by over 30%.

Even a smaller number of manuscripts focus on investigating the operation stability of 3D perovskite FETs. Senanayak et al. investigated the bias stability of optimized MAPbI3 FETs with PEIE modified Au electrodes biased with pulsed voltages of $V_{GS} = V_{DS} = 60$ V every 0.3 s for 30 min and observed essentially no change in device performance. The same group also demonstrated that optimized Rb-passivated CsFAMAPbI3-based perovskite FETs were more stable than reference MAPbI3 devices upon bias stress of $V_{GS} = V_{DS} = 60$ V for 10 h.

Promising results for enhancing the operational stability of perovskite FETs were recently reported by Kim et al., who have shown that the operational stability of perovskite FETs based on a mixed cation, mixed halide composition, Cs$_{0.05}$(MA$_{0.17}$FA$_{0.83}$)$_{0.95}$Pb(Br$_{0.17}$I$_{0.83}$)$_3$ can be enhanced by the addition of the hydrophobic cross-linker DPP and passivation by PEIE, with the performance of devices remaining unchanged after 80 000 s of a continuous bias stress (Figure 12a). Similarly, cycling stability test – where the device is repeatedly switched on and off for 50 000 cycles – has shown no sign of deterioration in performance (Figure 12b). Indeed, similar strategies based on the inclusion of stabilizing agents in the perovskite layer have been recently demonstrated for perovskite solar cells. For example, the inclusion of ionic liquids has been shown to dramatically increase device stability and should also be explored as a strategy for improving the operational stability of perovskite FETs.

5.3. Environmental Stability

As the field of perovskite photovoltaics matures and inches towards commercialization, the research community has gradually shifted its attention from being solely dedicated to increasing device performance, to investigating and mitigating its degradation. Unlike the remarkable advances made in enhancing the environmental stability of perovskite solar cells, few studies explored the stability of perovskite FETs in different environments. For example, Matsushima et al. compared the performance of single crystal PEA2SnI4 FETs in N$_2$ vacuum and mildly humid air. They observed that the mobility of an FET that was first measured in N$_2$ and later transferred to vacuum or air was halved, however it was speculated that this was caused by an unintentional shift of the perovskite crystal during the evacuation or refilling of the measurement chamber, rather than an interaction of the perovskite...
material with the environment. The FET performance in air (35% humidity) was found to be very stable—which the authors attributed to two factors. First, the single crystal exhibits a very low density of defects and grain boundaries, which are known to initiate the degradation upon exposure to either O₂ or H₂O. Second, the termination of the crystal surface by PEA makes it unlikely to oxidize.

Following this initial investigation, the same team investigated the stability of spin-coated PEA₂SnI₄ FETs in air in detail. By separately exploring the effects of exposure to humidity and oxygen, the authors found that while the former has little influence on the perovskite layer, the latter leads to a significant degradation of the perovskite structure with adverse effects on the film microstructure. It is noteworthy that exposure to trace amounts of oxygen was later shown to be beneficial to the performance of PEA₂SnI₄ FETs suggesting that the severe degradation observed by Matsushima et al. was most likely a result of a significantly increased oxygen concentration used in their experiments. Nevertheless, by reducing the density of grain boundaries in the polycrystalline perovskite film, the authors achieved not only significantly enhanced FET performance, but also improved stability upon measurement in air. Importantly, they also demonstrated that a simple encapsulation of the perovskite FET using Cytop can further enhance the device stability.

Gao et al. demonstrated that the environmental stability of the FETs can be significantly enhanced by using bulky linear π-conjugated oligothiophene cations (Figure 13). The authors obtained stable FET performance under vacuum conditions and only very minor degradation of performance upon storage in air without encapsulation for 30 days. This remarkable increase in device stability was associated with an intrinsic stabilization of the perovskite crystal, driven by intermolecular interactions between the conjugated cations, as well as their hydrophobic nature, which might limit the penetration of oxygen and humidity into the perovskite crystal.

The scarcity of detailed investigations of the environmental stability of perovskite FETs in spite of the overwhelming evidence that perovskite materials suffer from severe degradation upon exposure to oxygen and humidity represents a significant gap that should be urgently bridged for future integration into industrial applications. Significantly more research should be dedicated to tackling this key challenge, with many possible strategies that could be adopted from the fields of perovskite solar cells and light-emitting diodes, especially in the context of perovskite phototransistors, which will also suffer from light-induced degradation.

### 5.4. Electrode Degradation

Several studies performed on perovskite solar cells have demonstrated that ions from the perovskite layer may reach the electrodes causing device degradation. For example, in 2015, Kato et al. have shown that silver iodide (AgI) is formed at the interface with the electrodes in solar cells, resulting in decreased performance. Similarly, AgI formation was observed for lateral Ag electrodes deposited onto a perovskite layer by Li et al. These early examples suggest that chemical reactions may occur at the perovskite/metal interface and might also influence or deteriorate the device performance in perovskite FETs.

Unlike solar cells, that typically employ Ag electrodes, perovskite FETs very commonly use Au for source and drain contacts. It has been generally considered that Au is a stable electrode, resistant to environmental oxidation and metal–halide reactions, with degradation in perovskite solar cells that employ Au electrodes assigned to diffusion of Au into the active layer upon operation, rather than corrosion of the Au electrodes themselves. The identification of processes taking place at Au/perovskite interfaces in perovskite FETs is complicated by the difficulty to access these interfaces, especially after the devices have been biased. Wang et al. utilized a soft lamination method to deposit Au contacts on a MAPbBr₃ perovskite single crystal, which could be removed and investigated after biasing the device. It was demonstrated that an electrochemical reaction takes place at the interface between the positively biased Au contact and the perovskite, forming AuBr₃ confirmed by both X-ray photoemission spectroscopy (Figure 14a) and Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) (Figure 14b). The authors have also shown that it is possible to suppress such electrochemical reactions by inserting a buffer layer consisting of MoO₃ or PFBT, demonstrating the importance of interfacial engineering for further optimization of the performance and stability of perovskite FETs. While no similar investigations were performed on Au/MAPbI₃ perovskite FETs, a recent work by Kern et al. shows that electrochemical reactions can also occur at this interface.
5.5. Other Challenges

Reliable large-scale fabrication of perovskite FETs is a prerequisite for their application in modern electronics. Early work by Wang et al. has demonstrated that large arrays of independently addressable FETs can be fabricated by selectively nucleating and growing MAPbI$_3$ perovskite crystals on substrates pre-patterned with pairs of electrodes.[228] Recently, Zhu et al. fabricated over 1000 PEA$_2$SnI$_4$ FETs on a 4-inch wafer.[134] One hundred devices selected in random were measured and their performance was found to be rather uniform, with an average mobility of 3.16 ± 0.64 cm$^2$ V$^{-1}$ s$^{-1}$, demonstrating the potential of perovskite FETs for large-scale fabrication.

The issues of toxicity and environmental impact are of great concern to all possible applications of perovskites.[240] In the case of solution-processed perovskites, the use of toxic solvents hinders industrial-scale processing,[221] making it necessary to develop solvent-free deposition methods.[19,219] A possible route to a scalable fabrication of perovskite FETs might lie in the utilization of alternative methods for perovskite layer deposition. While most of the perovskite research activity is based on their solution processing, perovskite materials can be deposited also by thermal evaporation. Such deposition has several advantages over solution processing. First of all, it is solvent-free, which is beneficial in terms of both cost and environmental impact.[241] Second, thermally evaporated perovskites have been shown to crystallize without the need for thermal treatment,[242] which significantly simplifies processing and lowers the energy investment into the device fabrication. Additionally, it offers precise control over the layer thickness, which is not the case for solution-processed layers. Finally, thermal evaporation processes are well-established in many industrial applications, which can expedite the integration of perovskite FETs into mass produces electronic products.

While the high performance of 2D perovskite FETs that are based on tin, rather than lead, might appear to significantly reduce the environmental impact of these devices, some reports show that tin-based perovskites could be even more toxic than those based on lead.[243] Moreover, a recent study suggests that iodide is a key source of toxicity, the harmful effects of which will result in enhanced stability also of perovskite FETs. While most of the perovskite research activity is based on their solution processing, perovskite materials can be deposited also by thermal evaporation. Such deposition has several advantages over solution processing. First of all, it is solvent-free, which is beneficial in terms of both cost and environmental impact.[241] Second, thermally evaporated perovskites have been shown to crystallize without the need for thermal treatment,[242] which significantly simplifies processing and lowers the energy investment into the device fabrication. Additionally, it offers precise control over the layer thickness, which is not the case for solution-processed layers. Finally, thermal evaporation processes are well-established in many industrial applications, which can expedite the integration of perovskite FETs into mass produces electronic products.

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A special consideration should be devoted to understanding the role of perovskite layer microstructure in perovskite FETs. The lateral transport in these devices makes it necessary for charge carriers to cross multiple grain boundaries, so an optimized microstructure is of crucial importance. While many open questions remain regarding what influences the grain size of perovskite thin films, it has been shown that substrate surface energy and control over the pH value of the perovskite precursor solution are two factors that can be utilized for reducing the density of grain boundaries in perovskite layers.\cite{253-255} Importantly, one has to consider that crystallization on pre-patterned electrodes in bottom contact FETs, for example, will be starkly different to that on flat smooth surfaces such as extraction layers in solar cells. A structured metal contact surface could provide nucleation sites that will trigger crystallization and the growth of perovskite domains,\cite{256} so the exact geometry of these contacts will be instrumental in influencing the final perovskite active layer microstructure. This opens the opportunity for the development of novel strategies for the design of FET device structures with contacts that actively guide the perovskite crystallization to form the desired microstructure.

An alternative strategy to reduce the impact of grain boundaries is to examine the vertical device architecture for perovskite FETs. While only very few examples of such devices have been reported to date,\cite{257,257a} the implementation of perovskite FETs in a vertical device configuration makes it far more similar to the layered diode structures used in perovskite optoelectronics. Consequently, many of the existing optimization strategies of perovskite solar cells can be more easily transferred to vertical perovskite FETs.

The final strategy we would like to highlight is methodological in nature. As was mentioned in Section 2.4, the selected conditions for the measurement of perovskite FETs can greatly influence their performance. It is thus of critical importance that the methodology for the characterization and reporting of perovskite FET devices is standardized. Failing to do so would hinder the progress in the field, simply by the inability to reproduce literature results which serve as a starting point for future investigations. While the implementation of such a standard methodology might not immediately lead to better performing devices, it is good scientific practice and will – in the long term – result in further advances. The experience of the solar cell community, which was similarly plagued by these issues in its very early days, but progressed due to the adoption of standardized characterization (including the reporting of the scan speed, direction, environment, etc.) and presentation of statistically relevant data (i.e., histograms of device performance parameters instead of a single $I_f-V$ curve) has shown how valuable this can be in facilitating the progress in perovskite-based devices. Moreover, the immense focus on mobility as the sole figure of merit has led in many cases to incomplete reporting of other important device parameters, such as threshold and turn-on voltages, gate leakage current, on/off ratio and contact resistance. We strongly encourage researchers to be diligent in reporting the measurement conditions as well as the complete statistics of the performance parameters of their devices. Moreover, as mentioned earlier, the presence of ions in perovskites makes it necessary to report the temporal evolution of the device performance. In perovskite FETs, this can be achieved by tracking the channel current in the “on” state under applied bias, similar to the MPP tracking in perovskite solar cells. These measurements should be included together with transfer and output characteristics of the devices as standard practice.

6. Summary and Future Opportunities

Despite the fact that perovskite FETs were the very first reported electronic devices based on metal halide perovskites, they have not yet reached the level of maturity required by the market. Although progress has been made in recent years, perovskite FETs still need to overcome several challenges prior to commercialization.

The operation of perovskite FETs is complicated by their mixed ionic-electronic nature, the presence of defects, as well as external factors such as temperature and light. While the perovskite FETs included in many early reports suffered from non-ideal current-voltage characteristics, hysteresis and fast degradation, significant strides have been made both in understanding the origin of these phenomena and in the development of strategies for suppression, resulting in a number of examples of high-performance hysteresis-free perovskite FET devices. This positive development is also accompanied by an overall improvement of device performance, illustrated by the gradual increase in mobility and the emergence of perovskite-based FETs with novel functionalities such as memory.\cite{260,261} Still, many other challenges remain to be addressed, in particular, issues related to device stability, where significantly more research is required.

The steady improvements in mobility, fueled by a better understanding of the parameters that impact charge transport, suggest that perovskite FETs might be able to catch up with the other perovskite devices and become contenders for industrial applications in the form of thin-film transistor technologies. In spite of their very low hole and electron effective masses, perovskites will most likely never attain the high mobilities exceeding 1000 cm$^2$ V$^{-1}$ s$^{-1}$, which are characteristic to semiconductors like crystalline silicon, GaAs, or indium phosphide (InP), due to their soft nature, which makes the charges more susceptible to scattering. Nevertheless, alongside organic, carbon nanotube, and metal oxide semiconductors, perovskites could take advantage of the low-complexity processing and compatibility with arbitrary substrates and form factors to address applications where moderate charge carrier mobilities (<100 cm$^2$ V$^{-1}$ s$^{-1}$) are sufficient, and that are not possible or economically not feasible with traditional semiconductors.

We would like to emphasize, however, the true figure of merit deciding the type of application that a certain TFT technology can enable is not the mobility, but the transit frequency, $f_t$, which represents the maximum frequency at which the transistor can operate.\cite{258-261} A $f_t$ in the MHz range is necessary for wireless communication, displays, or RFID tags, while special applications like wireless transmitters and receivers used in military communications equipment or high-performance computer processors units require operation in the GHz range.\cite{259} A high mobility is indeed necessary in order to achieve high transit frequencies, but it is by no means sufficient. Other factors, such as the operating voltage, contact resistance, channel length and parasitic overlap between the gate and source/drain...
electrodes, often become more critical.[258–261] These properties have not yet been carefully explored in perovskite FETs. For example, only a handful of papers even report on the contact resistance value, while the parasitic effects due to contact overlap have never been addressed. The simultaneous reduction in contact resistance and channel length alongside mobility enhancement, all necessary for achieving a high $f_T$, is very difficult since these properties are interconnected: the channel resistance $R_{ch}$ is directly proportional with the channel length, $L$, while the contact resistance $R_c$ is independent on $L$, thus with reduction of $L$ the FET properties become dominated by $R_c$. In addition, with the increase in mobility, the channel resistance decreases, and hence the contacts become even more relevant.[219] Examining all manuscripts discussed in Tables 1 and 2, we found that the shortest channel length reported in perovskite FETs was $L = 2 \mu m$, with the vast majority focusing on $L > 30 \mu m$. This is at least one order of magnitude larger than the dimension needed for MHz operation given the current state of the art in terms of mobility. This tradeoff was necessary in order to minimize the impact of unoptimized contacts and to be able to access the material properties. Short channels also suffer from degradation due to Joule heating and a stronger polarization due to the presence of a higher electric field (therefore larger hysteresis). We hope that future work will expand the initial efforts mostly aimed at mobility enhancement and suppression of hysteresis to device design, targeted to address the other parameters that impact the operating frequency. Downscaling perovskite FETs will be challenging due to the fact that $L$, $\mu$, and $R_c$ parameters are all intertwined, but we believe that the design of efficient strategies for addressing this challenge should be the focus of the next phase in perovskite FET research in order to transition these devices to a real technology.

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Conflict of Interest

The authors declare no conflict of interest.

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