LTARS: analog readout front-end ASIC for versatile TPC-applications

T. Kishishita, S. Sumomozawa, T. Kosaka, T. Igarashi, K. Sakashita, M. Shoji, M.M. Tanaka, T. Hasegawa, K. Negishi, S. Narita, T. Nakamura and K. Miuchi

aKEK, High Energy Accelerator Research Organization, 1-1 Oho, Tsukuba, 3050801, Ibaraki, Japan
bIwate University, 4-3-5 Ueda, Morioka, 0208551, Iwate, Japan
cKobe University, 1-1 Nada-ku, Rokkodaicho, Kobe, 6570013, Hyogo, Japan

E-mail: kisisita@post.kek.jp

ABSTRACT: We designed a versatile analog front-end chip, called LTARS, for TPC-applications, primarily targeted at dual-phase liquid Ar-TPCs for neutrino experiments and negative-ion μ-TPCs for directional dark matter searches. Low-noise performance and wide dynamic range are two requirements for reading out the signals induced on the TPC readout channels. One of the development objectives is to establish the analog processing circuits under low temperature operation, which are designed on function block basis as reusable IPs (Intellectual Properties). The newly developed ASIC was implemented in the Silterra 180 nm CMOS technology and has 16 readout channels. We carried out the performance test at room temperature and the results showed an equivalent noise charge of $2695 \pm 71$ e$^-$ (rms) with a detector capacitance of 300 pF. The dynamic range was measured to be 20–100 fC in the low-gain mode and 200–1600 fC in the high-gain mode within 10% integral nonlinearity at room temperature. We also tested the performance at the liquid-Ar temperature and found a deterioration of the noise level with a longer shaper time. Based on these results, we also discuss a unique simulation methodology for future cold-electronics development. This method can be applicable to design the electronics used at low temperature.

KEYWORDS: CMOS readout of gaseous detectors; Dark Matter detectors (WIMPs, axions, etc.); Front-end electronics for detector readout; Neutrino detectors

1Corresponding author.
2Also at SOKENDAI, The Graduate University for Advanced Studies.
1 Introduction

In recent studies in particle and astro-particle physics, detectors with high-resolution positional imaging are often desired to explore new physics phenomena because the topological information can be utilized to discriminate the signature of the new physics phenomena from background events. These detectors require huge numbers of readout channels and advanced electronics play an important role in handling such large numbers of readout channels. To meet this need, we are developing front-end electronics for versatile applications of time projection chambers (TPCs) for a joint project called LTARS (Low Temperature Analog Readout System), located at KEK, Kobe, and Iwate Universities. We plan to use this readout system for the directional dark matter experiments [1, 2] and for the next-generation neutrino oscillation experiments [3].

TPC-based three-dimensional (3D) tracking detectors are thought to be one of the best detectors for the directional direct dark matter search experiments and several groups have developed prototype detectors [4, 5]. NEWAGE is one of these directional dark matter search experiments and has been leading in directional sensitivity [1]. One of the next steps needed to improve the sensitivity is to utilize a negative-ion drift gas, which enables full-volume fiducialization through 3D position reconstruction of the event vertex [6, 7]. These TPCs are called negative-ion (NI) $\mu$-TPCs and the detector concept is shown in the left of figure 1. In the NI $\mu$-TPCs, the ionized electrons are captured by the gas molecule immediately after ionization thereby generating negative ions. These ions are
drifted instead of the electrons in the NI $\mu$-TPCs. Some types of negative ion gases could contain more than one species of negative ion ($\text{SF}_6$ and $\text{SF}_5$ in figure 1). Each of these ions are drifted with different velocities. The arrival time difference provides information on drift length, or, the absolute position on the electric field direction. This new concept helps to improve the sensitivity by rejecting background events from the readout plane (indicated as MPGDs in figure 1) and the cathode plane; this was not possible with the self-triggering TPCs.

A large scale $O(10\text{kt})$ liquid argon time projection chamber (LAr-TPC) will be utilized as a 3D-tracking device for studies of next-generation neutrino oscillation, nucleon decay, and astrophysical neutrinos. Toward the realization of such a large-scale detector, a world-wide R&D effort on kiloton-scale LAr-TPC demonstrators is underway [8]. One approach to read out the ionized electron signals is to use a dual-phase LAr-TPC [9]. The detector concept is shown in the right of figure 1. In the dual-phase TPC, the ionized electrons are extracted from the liquid phase (indicated as LAr in figure 1) to the gas phase (GAr), and the extracted electrons are multiplied with a thick-GEM (Gas Electron Multiplier) and collected with a two-dimensional strip anode. The main advantage of the dual-phase readout is the high signal-to-noise ratio afforded by the gas multiplication. This enables a longer drift length because the signal is amplified even though some primary electrons are lost by impurities in the LAr. The high signal-to-noise ratio also benefits the physics sensitivity for the neutrino oscillation, nucleon decay, and astrophysical neutrino signals.

The signal timescale is much longer than that of electrons in typical gas TPCs, i.e., $\approx 10^{-2}\text{ cm/}\mu\text{s}$ for the NI $\mu$-TPCs and $\approx 10^{-1}\text{ cm/}\mu\text{s}$ for the LArTPCs, respectively. Therefore, the electronics has a lot of similarities, but is different from the standard electronics for the TPC. Additionally, a wide dynamic range together with a high signal-to-noise ratio is required for the readout electronics. In the case of the NI $\mu$-TPCs, typical signals are 3 fC for the minority species (indicated as $\text{SF}_5$ in figure 1) and 80 fC for the main species ($\text{SF}_6$) [11, 12]. On the other hand, the typical ionization signal in the LArTPCs is $\approx 10\text{ fC}$, assuming one order of magnitude of the thick-GEM gains, for a minimum ionization particle (MIP). The signal on one readout channel for events associated with electromagnetic or hadronic showers is about 50 times larger than 1 MIP signals. The detector capacitances seen from the ASIC input are both estimated as $\sim 300\text{ pF}$. A fine spatial resolution is
also necessary for both detectors, and it results in a huge number of readout channels as a whole
detector system. We also need to take the operating temperatures into consideration.

Whereas the readout electronics can be operated at room temperature (RT) in the NI$\mu$-TPC, the
front-end needs to be operated at $\approx -185$ °C for in the LArTPCs. This thermal constraint comes
from a practical issue that the analog front-end electronics must be located as close as possible to
the strip readout in order to minimize the detector capacitance.

To satisfy various requirements from both experiments, we have developed a series of readout
ASICs in a 180 nm CMOS technology. The circuits are designed on a function-block basis as
reusable components. In this paper, we report on the performance of a newly developed 16-channel
ASIC at RT and the functionality under the LAr temperature (LT) operation. We optimized the
transistor parameters of the previous prototype chip, taking special care in the layout to improve
low-noise characteristics [10]. One of the objectives of LTARS development was to generate cold-
electronics ‘know-how’ and to clarify issues for future system-integration, e.g., operating methods
of the ASICs at LT, and geometrical constrains on readout systems for a huge number of channels.
We describe the ASIC design in section 2, report on its performance at RT and LT in sections 3 and
4, respectively, discuss our simulation methodology for cold-electronics and future developments
in section 5, and conclude in section 6.

2 Architecture of the ASIC

2.1 Circuit properties

The physical layout of the readout ASIC implemented in the Silterra 180 nm CMOS technology is
shown in figure 2. Technological parameters and requirements for the ASIC are listed in table 1.
The chip includes 16 identical signal processing channels. The block diagram of each channel
is shown in figure 3. The TPC readout channel is connected to an input (AIN) of the charge-
sensitive amplifier (CSA) by an off-chip capacitor, while test pulses can be injected via an on-chip
AC-coupling capacitor $C_{tp} = 2$ pF. The CSA is based on a folded-cascode configuration with a
p-channel input transistor and a regulated-cascode configuration is implemented to improve the
open-loop gain for large detector capacitances. A transfer-gate type FET is employed for the CSA
DC-feedback component. Two distinct feedback capacitors are implemented for dynamic gain-
switching by using a metal-insulator-metal structure. The feedback capacitor is initially set at
$C_{t, HG} = 340$ fF. This state corresponds to a high-gain (HG) mode and it copes with a narrow range
signal of $< 80$ fC. The CSA output is fed into a discriminator to select the gain mode. Once the
amplitude of the CSA exceeds a certain threshold, which is given by a 6-bit DAC, a discriminator
followed by an RS-type flip-flop latches the switch on the additional feedback capacitance. This
state functions as a low-gain mode (LG) with a capacitance value of $C_{t, LG} = 6.22$ pF. As a result,
the overall voltage gain is more than 10 times smaller than that in the HG mode. After reading out
the analog output (AOUT) and the gain information (COMP_FBIN), the reset signal (RST) supplied
externally releases the latched signal and the overall circuit returns to the idle state. The influence
of the switching noise on the noise performance is negligible compared to the large input signals
required to switch on the LG mode. The dynamic-switching behaviors have been demonstrated in
the prototype chip, and this unique property makes the chip multi-purpose, not only for LAr-TPCs
but also NI $\mu$TPCs [10].
A CR-RC band-pass filter is composed of a pole-zero cancellation circuit (PZC) and a second-order integration low-pass filter. The capacitance and resistance values were selected to meet the equation of 
\[ C_{r, \ HG} \cdot R_{l} = C_{pz} \cdot R_{pz}, \quad \text{and} \quad C_{1} \cdot R_{1} = 4 \times C_{2} \cdot R_{2} \] (see figure 3). The transfer functions in the HG mode are described as

\[
T_{\text{CSA}} = -Q_{\text{in}} \cdot \frac{R_{l}}{(1 + sC_{r, \ HG} \cdot R_{l})} \cdot \frac{(1 + sC_{pz} \cdot R_{pz})}{R_{pz}},
\]

\[
T_{\text{CR}-\text{RC}} = -\frac{R_{l}}{(2sC_{2} \cdot R_{2} + 1)^{2}},
\]

\[
T_{\text{total}} = Q_{\text{in}} \cdot \frac{R_{l} \cdot R_{1}}{R_{pz}} \cdot \frac{1}{(2sC_{2} \cdot R_{2} + 1)^{2}}, \quad (2.1)
\]

where \( s \) denotes the complex angular frequency and \( Q_{\text{in}} \) is the input charges. The default shaping-time of the CR-RC filter is designed as 1 \( \mu \)s for the LArTPCs. This value can be switched to 4 \( \mu \)s for NI \( \mu \)TPCs via a 9-bit control register. This register is equipped in each channel, while also controlling the test pulse enable, monitor enable, and tuning voltage threshold. A reference current is injected to the IBIAS node via a potentiometer inserted between the ground and supply power. The current-mirror configuration generates an internal bias current of 100 \( \mu \)A that provides the proper bias current to each circuit block, e.g., 510 \( \mu \)A for the input FET in the CSA, at the current step of 10 \( \mu \)A.

Figure 2. Physical layout of the readout ASIC. The chip size is 2.5 mm\( \times \)5 mm.

3 Performance test results at room temperature

3.1 Experimental setup

The experimental setup and the dedicated printed circuit board (PCB) for performance testing are show in figure 4 left and right, respectively. The chip-mounted board (named SIRONEKO) shown on the left side of the right figure provides electrical connections between the ASIC. The semi-custom
Table 1. Technological parameters and requirements to the ASIC.

| Parameter                  | Value                        |
|----------------------------|------------------------------|
| Technology                 | Silterra 180 nm CMOS         |
| Chip size                  | 2.5×5 mm²                    |
| The number of channels     | 16                           |
| Supply power               | 1.8 V core/IO, max. 2.4 mW/ch|
| Fabrication options        | 6 metals, deep N-well, high-value poly res., MIM cap. |
| Detector type              | NIμ-TPC, LAr-TPC             |
| Minimum signal charge      | ≈3 fC, ≈10 fC               |
| Shaping time               | 4 µs, 1 µs                  |
| Operating condition        | room temperature, −185 °C    |
| Detector capacitance (Cdet) | ~300 pF                     |
| Dynamic range              | ±80 fC for narrow range, ±1600 fC for wide range |
| Voltage gain               | 10 mV/fC for narrow range, 0.5 mV/fC for wide range |
| ENC                        | 3000 e⁻ (S/N>20) for small signals, < 6.4 × 10⁴ e⁻ for large signals |

*: Estimated from the pad size of MPGDs.

Figure 3. Block diagram of the processing chain. Unlabeled substrates are connected to the supply powers.

FPGA board (named GoSHIK) is also shown on the right side. A bare die was directly mounted on the PCB, and optical light was shielded during the measurements. The GoSHIK board is an interface with a computer and provides the register control signals. This board includes 8-channel ADCs (AD9637) and 8-channel voltage/current DACs (LTC2656 and MAX5550). It provides a flexible bias setting to the ASIC, along with an easy-to-use pattern generation from the FPGA. We chose the Xilinx XC7A100T-2FGG676C [14], and data transfer is done via an Ethernet cable with the SiTCP protocol [15]. Test pulses are generated by a function generator (AFG-21025).
3.2 Analog waveforms and dynamic range

We first injected test pulses and checked the analog output with an oscilloscope. Figure 5 shows the waveforms in the different gain modes. The gain-switch and shaping time (1 µs) were fixed during the measurements. The waveforms were obtained without detector capacitance. Test pulses are shown in blue, which correspond to input charges of −40 fC in the HG mode and −1000 fC in the LG mode. The peaking times were measured as 1.2 µs and 1.0 µs, respectively. Although the pole and zero in the transfer function $T_{CSA}$ are not cancelled out in the LG mode (see eq. (2.1)), the overshoot was negligible at the analog output. The difference of the peaking times is not a major issue as long as the analog outputs are continuously sampled in parallel by ADCs, and the waveform is reconstructed in offline analysis.

![Figure 5. Analog outputs. The intervals on the vertical axis are 20 mV for input and 200 mV for output in the HG mode, and 500 mV for input and output in the LG mode. The intervals on the horizontal axis are 4 µs. All measurements were performed under the condition of $C_{det}=0$ pF.](image)

The dynamic range of a typical channel is shown in figure 6. Conversion gains were obtained by fitting a line through the minimum and maximum points of the required dynamic range. The measured values were 10.0 mV/fC for positive and 10.7 mV/fC for negative polarity in the HG mode, whereas in the LG mode, these values were 0.60 mV/fC and 0.65 mV/fC, respectively. The lower panels show the residuals between the data and fitting lines. Linearity is maintained with ±10% integral nonlinearity up to ±100 fC in the HG mode, while that extends to ±1600 fC in the...
Figure 6. Dynamic ranges of a typical readout channel in different gain modes. The lower panels show the residual between the data and linear functions. The baseline is subtracted from the peak pulse height.

Figure 7. Gain variation in the HG mode.

LG mode. The gain variation between the 16 channels is shown in figure 7. We confirmed that the variation is within 10%.

3.3 Equivalent noise charge

All the noise generated inside the amplifier is calculated as a quantity that is then converted into an equivalent noise charge (ENC), which is the noise generated at the input. The ENC is given by the following formula:

\[
\text{ENC (electron)} = \frac{V_{\text{noise, rms}} \text{ (mV)}}{\text{Conversion gain} \text{ (mV/fC)} \times 1.6 \times 10^{-4} \text{ (fC)}}.
\]
Figure 8 shows the detector capacitance $C_{\text{det}}$ versus the corresponding ENC values. For comparison, the simulation result is overlaid in the figure. To improve the noise performance, on-chip ESD protection diodes were not included in the analog inputs. The voltage noise is proportional to the detector capacitance, and the ENC in the HG mode was measured as $2695 \pm 71$ $e^-$ at $C_{\text{det}} = 300$ pF. By comparing our results with the simulation value of $2361$ $e^-$, we can confirm that the performance is very close to the simulation value, although there is about 13% offset at $C_{\text{det}} = 300$ pF. Possible causes of the noise offset are the bonding wire and PCB trace capacitance due to the mounting of the ASIC on the evaluation board and the ground bounce due to a single-supply configuration, i.e., 0/1.8 V. Based on these considerations, we expect to be able to improve the performance of the ASIC in the next experiment and design. The ENC in the LG mode was measured as $37200 \pm 330$ $e^-$ at $C_{\text{det}} = 300$ pF with a noise slope of $5.41$ $e^-/\text{pF}$. Since the expected value is $36913$ $e^-$, we concluded that the overall performance at RT are in agreement with the simulation models provided by the vendor. Moreover, the measured value is lower than the requirement of 64000 $e^-$ in the LG mode.

The typical ionization signal for 1 MIP in the LAr-TPC of 10 fC, corresponding to 94000 $e^-$, is expected based on recent studies at the large LAr-TPC demonstrators [8]. The ENC of 2700 $e^-$ achieves $S/N = 23$, and thus, the ASIC performance is considered to have reached the level of practical application if the RT performance can be kept at the LAr temperature. The data processing architecture in LArTPCs to handle the analog outputs from all channels is currently under discussion. Two options exist: either using external ADCs in parallel or on-chip ADCs combined with sparse readout. Since the number of readout channels is expected to be $O(10^5)$ for a $O(10 \text{kt})$ detector, it is desirable to reduce the number of feedthrough lines running from the inside to the outside of the LAr cryostat. From this perspective, we will consider a circuit that consists of both analog and digital processing parts by optimizing the deep Nwell option of the current 180 nm CMOS technology.

![Figure 8](image)

**Figure 8.** The equivalent noise charge (rms) as a function of detector capacitance. Data and simulation are shown in red and blue, respectively.
4 Measurements at the LAr temperature

4.1 Experimental setup

Figure 9 shows the experimental setup operated at the LAr temperature of $\approx -185^\circ$C. Since the feed-through terminal of the cryostat limits the number of cable connections, we chose direct immersion of the electronics in a Dewar vessel filled with liquid argon. To avoid thermal stress on the FPGA board, we separated the GoSHIK board from the ASIC, soaking only the SIRONEKO board in liquid argon. Supply powers, test pulses, and monitor lines were directly connected with ribbon cables. The bias voltages, which were tuned with trimmer potentiometers at RT, were also provided by external power supplies. The direct immersion approach provides an easy-to-access environment to the ASIC, although it subjects the ASIC and mounted components to harsh thermal and mechanical stresses. In this experiment, the temperature can be reduced to that of liquid argon instantaneously, removing any time restrictions.

![Figure 9. Experimental setup for the LAr temperature operation (left). Only the ASIC, i.e., the SIRONEKO board, was directly immersed in the LAr (right).](image)

4.2 Waveforms and dynamic range

In the LAr temperature, we confirmed that the circuit could not be operated under the same bias conditions as the RT environment. By optimizing the bias settings we succeeded in obtaining analog outputs; however, the conversion gain decreased and the noise level severely deteriorated. Such deterioration was not observed at RT in the Dewar. The baseline fluctuation was about 120 mV, while the peak height was about 530 mV for an input charge of 40 fC. Compared with the RT result, the gain decreased by about 40%. In order to specify the cause of this issue, we used the time-averaging function of the oscilloscope and compared the waveforms at the RT and with the simulation. The simulation methodology is discussed in the next section.

Figure 10 shows the time-averaged waveforms at RT and the LAr temperatures with an input charge of $-40 \text{ fC}$ and $C_{\text{det}} = 300 \text{ pF}$. Compared with the RT results, not only the conversion gain, but also the peaking time was clearly affected by the temperature; there was an increase of 60% in the peaking time. The conversion gain at LT was determined to be 6.6 mV/fC, while the peaking time was about 1.6 $\mu$s. This result was contrary to our expectations since the charge carrier mobility
in silicon generally increases with decreasing temperature, while the thermal noise decreases at the same time in the LT environment. Figure 11 shows the dynamic range at the LAr temperature.

![Waveform comparison](image1)

**Figure 10.** Time-averaged waveforms at RT and LT. Data and simulation are shown in red and blue, respectively.

![Dynamic range comparison](image2)

**Figure 11.** Comparison of the dynamic range in the HG mode with $C_{\text{det}} = 300$ pF.

## 5 Possible cause of the performance degradation and simulation methodology for cold-electronics

The analog performance at RT satisfied the requirements from the experiments, however, further optimization of the circuits and devices is clearly necessary for operation of circuits immersed in the LAr. In this section, we discuss possible causes of the performance degradation at LT and a unique simulation methodology for reliable cold electronics.
The gain and peaking time of the analog output are related to the operating points of the devices. It is generally known that the threshold voltage of the transistors increases as temperature is reduced, with a similar shifting-magnitude for n- and p-channel transistors, e.g., approximately 1 mV/K [16]. The SPICE parameters are supported at $-40^\circ C$ from the vendor; however, there are hurdles to extending this model down to the LAr temperature. Instead of modifying the individual transistor parameters, we attempt to utilize the body effect by changing the substrate voltage. The threshold voltage, $V_{th}$, of the transistor including the body effect is described with the Fermi potential of bulk silicon $\Phi_F$ with respect to the intrinsic Fermi level as

$$V_{th} = V_{th0} + \gamma \left( \sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F} \right),$$

(5.1)

where $V_{th0}$ is the threshold voltage of the transistor at RT, $V_{SB}$ is the source-bulk potential difference, and $\gamma$ is the body effect coefficient which typically lies in the range of 0.3 to 0.4 V\(^1/2\) [17]. Thus, it is possible to mimic the threshold voltages at LT, simply by changing $V_{SB}$ without considering process-dependent parameters. In the actual simulation, we separated the substrate nodes from the source voltages, applying the negative values from the source voltage $V_{BS,n}$ for n-channels and positive values of $V_{BS,p}$ for p-channels (see figure 13 as a schematic example).

The simulated waveforms with various $V_{SB}$ are shown in the left of figure 12. The top and bottom panels respectively show the outputs of the CSA and band-pass filter. As $V_{SB}$ increases, the baselines at the CSA and band-pass filter outputs linearly shift from the RT condition, while the rising edge of the CSA simultaneously becomes slower. On the other hand, the peaking time becomes longer and pulse height becomes lower. The threshold shift is estimated as 200 mV if we assume the LAr temperatures, and thus, the corresponding $V_{SB}$ is 0.88–1.35 V. Here we assumed $2\Phi_F =$0.8–0.9, and is temperature independent in this technology. We overlaid the simulation result of $V_{SB} = 1.2$ V in figure 10. For direct comparison, we optimized offsets in the baseline and peaking-times. While the gain and peaking-time shifts are close to the measurements, the overall breadth of the measurement at LT is wider than that of the simulation. Although there is still room for bias tuning, this is plausibly caused by a unity-gain buffer implemented on the PCB board.

The cause of the waveform shift was found to be due to the linear decrease of the transconductance $g_m$ of the input FET. The right of figure 12 shows $g_m$ as a function of $V_{SB}$. The rise time of the CSA ($t_{r,CSA}$) is given as

$$t_{r,CSA} = \frac{C_{det}}{g_m} + \frac{C_L}{\mu_0 \cdot g_m},$$

(5.2)

where $\mu_0 = \frac{C_f}{C_f + C_{det}}$ and $C_L$ is the load capacitance at the CSA output. We can see that the rise time of the CSA becomes larger as $g_m$ decreases. The peaking time and pulse height of the filter can be explained as a consequence of the slow rising edge of the CSA. The decrease of $g_m$ occurs due to the decrease of the internal bias current, which flows 100 µA at RT. The right side of figure 12 shows the internal bias current as a function of $V_{SB}$. As described in section 2, we used a diode- and current mirror- configurations as a bias generator. However, even if the IBIAS node is connected to the supply power, the internal current deviates as temperature decreases due to the higher threshold voltage in the simple diode-configuration. As a result, the nominal 510 µA for the input FET is not provided properly, and consequently, the $g_m$ deteriorates as temperature decreases.
To reduce the threshold shift at the LAr temperature, we considered two approaches. The first is to apply a forward bias voltage, e.g., 0.5 V, to the source substrate junction. The resulting forward current might be negligible at low temperature because of the decrease in the intrinsic carrier concentration. This approach requires additional power supplies for substrate biasing, however, it is easier to tune the bias current externally. The second approach uses a feedback-based current circuit proposed in [18]. Figure 13 shows a schematic of such bias circuit, based on the beta-multiplier. The addition of the resistor kills the closed loop gain, and the positive feedback system can be stable as long as its closed loop gain is less than one. The bottleneck of the circuit is that the gain of the loop increases as the size of resistor decreases. This pushes the feedback system closer to the instability. If the resistor, for example, is bonded out off-chip to set the current, it is likely that this bias circuit will oscillate, and thus, the circuit is basically self-biased with an on-chip resistor. For comparison, current output as a function of \( V_{SB} \) is overlaid in the right of figure 12 in a dashed line. We can see that the internal 100 \( \mu \)A is stably provided by this circuit.

\[ \text{Figure 12. (Left): simulation waveforms (top: CSA, bottom: shaper) with a typical process corner and different } V_{SB} \text{ values. The injected charge is 40 fC in the HG mode. The baseline offset is also caused by the threshold shift. (Right): the transconductance of the input transistor (top) and internal reference bias current (bottom) as a function of } V_{SB}. \]

6 Conclusion

We have newly developed the TPC readout chip in the 180 nm CMOS technology. The front-end ASIC is targeted at dual-phase LAr-TPCs for neutrino experiments and NI \( \mu \)-TPC for directional dark matter searches. We optimized the transistor parameters of the previous prototype chip, taking care in the layout for low-noise performance. The ENC reached 2695\( \pm \)71 e\(^-\) (rms) for a 300 pF detector capacitance with a noise slope of 3.09 e\(^-\)/pF at RT. The dynamic range and shaping times also satisfy the experimental requirements. In the LAr temperature testing, we have acquired the analog waveforms from the ASIC, however, the noise level unexpectedly deteriorated with a longer shaping time. By comparing our results with the SPICE simulation, this issue was found to be...
Unlabeled NMOS are W/L=50/2, and unlabeled PMOS are W/L=100/2 in unit of 180 nm.

**Figure 13.** Schematic of the improved bias circuit based on the beta-multiplier [18]. All substrate biases are separated from supply powers for the body-effect simulation.

caused by threshold voltage shifts of the transistors at LT. This work describes a unique simulation methodology for reliable cold electronics, which utilizes the body effect to mimic the threshold shifts. This method can be applicable to general cold electronics designs.

**Acknowledgments**

This work was supported by KAKENHI Grant-in-Aids (16H02189, 26104005, 17H01134, 18K03684, 19H05806), JSPS Bilateral Collaborations (Joint Research Projects and Seminars) program.

**References**

[1] T. Ikeda et al., *Results of a directional dark matter search from the NEWAGE experiment*, *J. Phys. Conf. Ser.* **1468** (2020) 012042.

[2] K. Miuchi et al., *CYGNUS*, *J. Phys. Conf. Ser.* **1468** (2020) 012044.

[3] A. Badertscher et al., *A possible future Long Baseline Neutrino and nucleon decay experiment with a 100 kton Liquid Argon TPC at Okinoshima using the J-PARC Neutrino Facility*, arXiv:0804.2111; DUNE collaboration, Long-Baseline Neutrino Facility (LBNF) and Deep Underground Neutrino Experiment (DUNE), arXiv:1601.02984.

[4] T. Tanimori et al., *Detecting the WIMP-wind via spin-dependent interactions*, *Phys. Lett. B* **578** (2004) 241 [astro-ph/0310638].

[5] F. Mayet et al., *A review of the discovery reach of directional Dark Matter detection*, *Phys. Rept.* **627** (2016) 1 [arXiv:1602.03781].
[6] D.P. Snowden-Ifft, *Discovery of multiple, ionization-created CS$_2$ anions and a new mode of operation for drift chambers*, Rev. Sci. Instrum. 85 (2014) 013303.

[7] T. Ikeda, *Development of a negative ion micro TPC detector with SF$_6$ gas for the directional dark matter search*, 2020 JINST 15 P07015 [arXiv:2004.09706].

[8] I. De Bonis et al., *Technical design report for large-scale neutrino detectors prototyping and phased performance assessment in view of a long-baseline oscillation experiment*, CERN-SPSC-2014-013 (2014) [SPSC-TDR-004].

[9] A. Badertscher et al., *Construction and operation of a double phase LAr large electron multiplier time projection chamber*, in the proceedings of the Nuclear Science Symposium, Medical Imaging Conference and 16th International Workshop on Room-Temperature Semiconductor X-Ray and Gamma-Ray Detectors (NSS/MIC 2008/RTSD 2008), October 19–25, Dresden, Germany (2008), arXiv:0811.3384.

[10] M. Nakazawa et al., *Prototype analog front-end for negative-ion gas and dual-phase liquid-Ar TPCs*, 2019 JINST 14 T01008.

[11] K. Miuchi, *Performance of the TPC with Micro Pixel Chamber Readout: micro-TPC*, IEEE Trans. Nucl. Sci. 50 (2003) 825.

[12] Y. Giomataris, Ph. Rebourgeard, J.P. Robert and G. Charpak, *MICROMEGAS: a high-granularity position-sensitive gaseous detector for high particle-flux environments*, Nucl. Instrum. Meth. A 376 (1996) 29.

[13] G. De Geronimo et al., *Front-end electronics for imaging detectors*, Nucl. Instrum. Meth. A 471 (2001) 192.

[14] https://www.xilinx.com/products/silicon-devices/fpga/artix-7.html

[15] T. Uchida, *Hardware-based TCP processor for gigabit ethernet*, IEEE Trans. Nucl. Sci. 55 (2008) 3.

[16] W.F. Clark et al., *Low temperature CMOS — A brief review*, IEEE Trans. Compon. Hybrids Mauf. Technol 15 (1992) 397.

[17] B. Razavi, *Design of analog CMOS integrated circuits*, McGrawHill, U.S.A. (2000).

[18] R.J. Baker, *CMOS circuit design, layout, and simulation*, Wiley, U.S.A. (2019).