Low-power Adaptive Integrate-and-Fire Neuron Circuit using Positive Feedback FET Co-integrated with CMOS

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ABSTRACT The most important aspect of an artificial neuron circuit is energy consumption. An analog neuron circuit has a critical problem in that the energy consumption in the steady-state due to a short-circuit current in the first inverter is quite large. In this study, we first demonstrated an adaptive neuron circuit with a dual-gate positive feedback field-effect transistor (FBFET) and fabricated a neuron circuit by co-integrating the FBFET and a complementary metal-oxide semiconductor (CMOS) in a chip. The fabricated FBFET has an extremely low sub-threshold slope of less than 0.5 mV/dec and a low off current. The threshold voltage of the FBFET can be precisely controlled by the second gate bias. By adjusting the second gate bias, it is possible to implement spike-frequency adaptive characteristics in the neuron circuit. Moreover, the proposed neuron circuit with the FBFET can significantly reduce the power dissipation. In the neuron circuit, a short-circuit current is suppressed by adopting the FBFET in the first inverter. In a modified inverter with the FBFET, more than 50% total energy consumption was reduced by the FBFET. We implemented the modified inverter in which the FBFET is connected in parallel with an N-channel metal-oxide semiconductor. Moreover, we utilized the neural frequency adaptation characteristics in the neuron circuit by adjusting the threshold voltage of the FBFET. Finally, we analyzed the fabricated FBFET neuron circuit operation and power consumption compared to a conventional CMOS neuron circuit.

INDEX TERMS Integrate-and-fire neuron circuit, low power, positive feedback field-effect transistor, short-circuit current, spike-frequency adaptation.

I. INTRODUCTION

Recently, neuromorphic devices inspired by biological networks, which can overcome the limits of the von-Neumann architecture, have been studied. One of the neural networks, the spiking neural network (SNN), has been researched as a third-generation neural network [1][2][3][4][5][6]. In an SNN, neuron circuits are the basic components of signal processing, which are biologically plausible artificial neuron models in which all signals are encoded by spikes based on the rate or spike timing dependency method [7][8]. Moreover, the synaptic weight is adjusted by the spike timing difference. Therefore, in an SNN, spike generation is the most important function, and numerous neurons that behave similarly to biological systems are required. To reduce the energy consumption of an SNN, it is most important to suppress the power dissipation in the neuron circuits. Therefore, various types of analog neuron circuits such as integrate-and-fire (I&F) neurons, conductance-based neurons, log domain neurons, and quadratic I&F neuron have been presented for implementing artificial neuron circuits [9][10][11][12][13][14]. An I&F neuron circuit was introduced to mimic biological neuron behavior, and the “Axon–Hillock” model proposed by Mead [15] is the most representative model of an I&F neuron circuit. Most of the conventional analog neuron circuits are constructed with a
membrane capacitor ($C_{\text{mem}}$) to integrate the input pulse. Moreover, the first inverter stage (INV1) that is connected to $C_{\text{mem}}$ accounts for the largest proportion of the power consumption, and has been called a starred inverter [16]. Because INV1 can spend a long time in a conductive state while the input voltage gradually passes through the switching voltage, during this period a short-circuit current ($I_{\text{sc}}$) flows from the power supply voltage ($V_{\text{dd}}$) node to ground. The energy is proportional to the switching time ($t_s$) of the input voltage, which is a very long period compared to in a digital circuit because $t_s$ is determined by the interval and number of input pulses. For a detailed explanation of the power dissipation in the above inverter, refer to [17][18]. Therefore, most of the energy is wasted during the period before inverter switching. A comparison of the energy consumption and number of transistors of different neuron circuits is summarized in Table I. In most studies, the energy consumption during the integration period before a spike is not considered, instead only that in the spiking period is focused on. However, actually, the energy consumption during integration can be higher than that during spiking. To reduce energy consumption, neuron circuits with various types of nonvolatile memories, such as resistive random-access memory, phase change materials, and insulator to metal transition devices are reported [19][20][21][22][23][24][25][26][27]. However, these devices have endurance problems for application in neuron circuits. In case of a neuron circuit, for etching the neuron fires, nonvolatile memories have to set and reset the state transition repeatedly; therefore, the endurance property is the most important characteristic. In addition, biological neurons present various behaviors such as adaptation, bursting, and resting [28][29][30]. Neural adaptation is a phenomenon in which the spike-frequency decreases over repetitive stimulations. Frequency adaption is a very essential characteristic that can reduce the energy consumption of neurons. Their energy consumption is proportional to frequency. Therefore, with a sufficiently trained SNN, if the frequency can be reduced by adaption, the energy consumption can be reduced proportional to the frequency. To implement an adaption model in a neuron circuit, spike-triggered adaptations have been studied [29][30].

### II. DUAL-GATE POSITIVE FBFET

Various types of steep-switching devices have been reported to overcome the limits of metal-oxide-semiconductor field-effect transistors, such as tunnel field-effect transistors, I-MOS, negative capacitance field-effect transistors, and IMT devices [31][32][33][34]. However, these devices are not able to replace the conventional CMOS owing to their low endurance, low on current, and high gate capacitance. Among the candidates for steep-slope devices, an FBFET is generating interest as a future low-power device owing to its excellent sub-threshold characteristics and high on/off ratio [35][36][37][38][39][40]. In a previous study, we investigated the operation mechanism and electrical characteristics of an FBFET [17]. In this study, we fabricated an FBFET with a conventional CMOS in a wafer by adding only one mask for the second gate (gate2) patterning and optimized the electrical characteristics of each device. The sub-threshold slope (SS) and on/off current ratio were improved by reducing the gate length, reducing the time of rapid thermal annealing, and increasing the temperature. The measured drain current ($I_d$)–first gate (gate1) voltage ($V_{G1}$).
curves based on the drain bias are shown in Fig. 1. As shown in Fig. 1, the tested FBFET has a super steep switching property with an SS of less than 0.5 mV/dec. Moreover, the FBFET can operate as both n-type and p-type FETs via its double control gates. When a fixed positive voltage is applied to gate2 and the gate1 voltage is swept, the FBFET operates as n-type FET, and conversely, if a negative voltage is applied to gate1 and the gate2 voltage is adjusted, it operates as a p-type FET. Fig. 2 presents the transfer characteristics at various $V_{G2}$. The depth of the potential well at the n-type floating body below gate2 is controlled by $V_{G2}$, making it possible to adjust $V_T$ precisely via the bias of gate2. $V_T$ increases linearly as $V_{G2}$ increases. By adjusting the gate2 bias, it is possible to implement spike-frequency adaptive characteristics. The $I_D$-drain voltage ($V_D$) curves based on $V_{G2}$ are shown in Fig. 3. The FBFET has an extremely low off current of approximately $10^{-14}$ A, high on/off current ratio of approximately $10^9$, and hysteresis voltage (~0.4 V). Therefore, owing to the excellent sub-threshold properties, the FBFET could be used effectively as a low-power application. However, because the FBFET turns off rapidly before the drain voltage drops to 0 V (Fig. 3), it would be difficult to utilize it as a logic application. Therefore, despite its very excellent switching characteristics, an FBFET has only been used as a memory device, and there are no reports on its use as a logic device.

III. FBFET INVERTER WITH CMOS

We developed an FBFET inverter with a CMOS that can reduce energy consumption. In a conventional analog inverter, if the input voltage passes gradually through the switching voltage, a linear current called short-circuit current ($I_{sc}$) or crowbar current flows from the power supply to ground. In addition, while the input voltage remains below the switching voltage, the N-channel metal-oxide semiconductor (NMOS) and the P-channel metal-oxide semiconductor (PMOS) operate in saturation and linear regions, respectively. Thus, during this period, the linear current continues to flow through the CMOS. Therefore, the
initially turns on and decreases the output voltage rapidly, the NMOS (N1) continuously drops the output voltage to ground, as shown in Fig. 6, which presents the measurement results of the modified inverter. The energy consumption of the conventional inverter is 838.6 pJ and 962.3 pJ at \( t_r = 50 \mu s \) and \( t_r = 100 \mu s \), respectively. In the proposed inverter, the energy consumption is 401 pJ and 412 pJ when the rising times are 50 \( \mu s \) and 100 \( \mu s \), respectively. As the rising time increases, the energy consumption slightly increases. This is because as the rising time increases, the duration of the leakage current flow in the NMOS (N1) increases. However, in the neuron circuit, the additional PMOS (P_{boost}) is connected with the FBFET inverter, as shown in Fig. 6(d). The inverter starts switching, and the PMOS plays the role of raising the input voltage to \( V_{dd} \). Therefore, the N1 leakage current time is reduced and becomes independent of the rising time. Finally, the power consumption of the proposed FBFET inverter with \( P_{boost} \) is 371 pJ at both rising times of 50 \( \mu s \) and 100 \( \mu s \). Therefore, the modified FBFET inverter can reduce the energy consumption by approximately 50%.

**IV. ADAPTIVE NEURON CIRCUIT WITH FBFET**

Fig. 7 shows the neuron circuit diagram and microscope image of a fabricated chip in which the FBFET is connected in parallel with the first inverter stage (INV1), and \( V_I \) of N1 is higher than that of the FBFET. In the FBFET, the source is grounded, the drain is connected to node1, and gate1 and gate2 are connected to \( C_{mem} \) and \( C_{adapt} \). If \( V_{mem} \) exceeds the \( V_T \) of the FBFET, the electron and hole concentrations in the

**FIGURE 6.** Measurement results of modified inverter with FBFET. After FBFET initially turns on and decreases output voltage rapidly, continuously \( V_{out} \) is fully discharged by NMOS.

**FIGURE 7.** Proposed neuron circuit diagram and microscope image of fabricated chip, where FBFET is connected in parallel with first inverter stage.

**FIGURE 8.** Measurement results of proposed neuron circuit (a) \( t_r = 50 \mu s \) and (b) \( t_r = 400 \mu s \). \( V_{adapt} \) maintains \( V_{out} \) because \( I_{leak} \) is suppressed by FBFET while \( C_{mem} \) is charged. Therefore, even though interval of input signal becomes longer and \( V_{mem} \) is gradually charged, energy consumption is not increased.
floating body and the drain current are abruptly increased. After the node1 voltage ($V_{\text{node1}}$) is dropped to approximately $V_{\text{dd}}$ by the FBFET, $V_{\text{mem}}$ is charged to $V_{\text{dd}}$ by $P_{\text{boost}}$. Thus, N1 with a high $V_T$ can be turned on, and it discharges node1 to ground. Finally, an output pulse is generated, and $C_{\text{mem}}$ is discharged. Moreover, whenever output spikes are generated, $C_{\text{adapt}}$ is charged and $V_{\text{adapt}}$ is increased, resulting in an increase in $V_T$ of the FBFET and spike-frequency decrease.

The measurement results of the conventional and FBFET neuron circuits are shown in Figs. 8 and 9, respectively. The input pulses are applied by the pulse generator, node1, and the output is recorded by an oscilloscope. Compared to the conventional neuron circuit, in the FBFET neuron circuit, $V_{\text{node1}}$ maintains $V_{\text{dd}}$ because $I_{\text{sc}}$ is suppressed by the FBFET and $C_{\text{mem}}$ is charged.

In the CMOS neuron circuit, $V_{\text{node1}}$ gradually decreases as $V_{\text{mem}}$ increases. During this period, $I_{\text{sc}}$ flows through the first inverter and most of the energy is wasted. Moreover, this period is increased as the input pulse interval increases or as the amplitude of the pulse decreases. The FBFET completely suppresses the $I_{\text{sc}}$ flow until switching occurs, and energy is only consumed at the moment of firing. Because the FBFET is turned on rapidly, INV1 switches very rapidly and the duration of the total current flow is significantly reduced (Fig. 8). In a previous study, we conducted circuit SPICE simulations and one-layer SNN simulations [17]. By conducting SPICE simulation, we calculate the power consumption per spike generation. The energy consumption per spike of the FBFET (at $V_{\text{dd}} = 1.5$ V, input pulse duration = 100 ns) is 120 fJ for 2 μs. The total energy of the neuron circuit is 8.83 pJ. In case of the conventional neuron circuit without an FBFET, the energy consumption per spike in INV1 is 12.4 pJ and that of the total circuit device is 18.79 pJ for 2 μs. The energy consumed by INV1 accounts for the largest percentage (66%) of the total energy. Most of the energy in INV1 is wasted before switching. In the proposed neuron circuit, the energy consumed by the first inverter is significantly reduced, resulting in a total energy reduction of 58%. Based on the SNN simulation, approximately 94% of the average power consumption of all output neurons is reduced [17]. The fabricated circuit has a gate length of 400 nm and a width of 1 μm; therefore, parasitic capacitors are very large and the delay time is long compared to those of a nanoscale circuit. Based on the measured characteristics, when the device scale was reduced, the current and parasitic capacitors were calculated. Therefore, we modeled the characteristics of the FBFET device and the extracted energy consumption using TCAD and SPICE. The measurement and SPICE simulation results of the spike-frequency adaptation are shown in Fig. 10. Moreover, whenever the action potentials are generated, $C_{\text{adapt}}$ is charged and $V_{\text{adapt}}$ is increased, resulting in $V_{G2}$ of the FBFET to increase. As the bias increases, both $V_T$ of the FBFET and the switching voltage of INV1 increase. Therefore, more input signals are needed for the neuron circuit to fire, and its spike-frequency is decreased. The delay time of the fabricated circuit is extremely long owing to the large parasitic capacitors; however, the simulated device has approximately 50-nm-scale gate length and width. Therefore, the spike pulse width is much smaller than the measurement result.

V. FABRICATION OF PROPOSED NEURON CIRCUIT

The fabrication process is CMOS-compatible and based on

![Fabrication process](image-url)
the standard CMOS process. The FBFET is co-integrated with a CMOS circuit, and the fabrication process is shown in Fig. 11. The difference from a CMOS process is that patterning of gate2 has to be added. Active patterning of the FBFET and the CMOS over a silicon-on-insulator wafer and p-type well implantation (BF2+ with a dose of 1 × 1013 cm−2) for the FBFET and the NMOS are performed to adjust the threshold voltage. Therefore, the body doping concentration of the FBFET is equal to that of the NMOS. Subsequently, for gate1 of the FBFET and the NMOS gate oxide, 8-nm-thick SiO2 is grown by dry oxidation at 960 °C and n+-doped poly-Si is deposited by low-pressure chemical vapor deposition. After the gate1 patterning, a potential N-well below gate2 and a lightly doped drain of the NMOS are formed by n-type implantation (as with a dose of 3 × 1013 cm−2), and the buffer oxide is removed by hydrogen fluoride (HF) wet etching. The SiO2 gate2 oxidation is performed to achieve 10-nm thickness by dry oxidation at 960 °C. This SiO2 not only serves as the oxide of gate2 but also separates gate1 and gate2. Subsequently, n+-doped poly-Si is deposited on gate2 of the FBFET and the sidewall spacer of the NMOS, and the gate2 patterning is conducted both for the FBFET and CMOS. The first and second poly-Si are used as the bottom and top plates of the capacitor, respectively. After source and drain implantation (BF2 for p-type, as for n-type with a dose of 5 × 1015 cm−2), rapid thermal annealing is conducted at 950 °C, with 5 s in an oxygen atmosphere for re-oxidation. Finally, tetraethoxysilane is deposited as the interlayer dielectric, and contact hole etching and pre-metal cleaning (dHF, 10 s) are conducted. Metal stacks (Ti/TiN/Al/TiN, 300/300/4000/300 Å) are deposited by metal sputtering. Metal patterning and inductively coupled plasma metal etching are performed. A mask layout and SEM image of the FBFET are shown in Fig. 12.

VI. DISCUSSIONS

We believe that the proposed neuron circuit and FBFET inverter are important advances for the development of artificial neuron circuits with new devices and for the application of an FBFET as logic device. Using a CMOS alone cannot prevent the short-circuit current, which is the most critical problem of analog circuits. In addition, although an FBFET has steep switching characteristics, owing to its critical problem as a logic device, it cannot replace a CMOS. Therefore, although FBFETs have been investigated as memory devices, there are few applications as logic devices. An FBFET and a CMOS should complement each other by taking advantage of their individual strengths. By integrating a CMOS and an FBFET into one chip to implement a neuron circuit, we can overcome the weaknesses of each device, dramatically reduce the energy dissipation, and imitate the biological characteristics of a neuron.

In addition, compared to non-volatile memories such as ReRAM and PCRAM, FBFET have superior endurance characteristics, since the electron movement mechanism is same as in conventional MOSFET. As shown in Fig. 13(a), there is no VT shift, when repeated DC voltage sweep measurements are performed more than 104 times. However, because the amount of electron accumulation in floating body is affected by temperature, the temperature sensitivity is slightly increased compared to MOSFET. As the temperature increases, the VT is decreased and the on current is increased as shown in Fig. 13(b).

We fabricated an adaptive I&F neuron circuit with an FBFET, which significantly reduces the energy dissipation of hardware neural networks and mimics spike-frequency adaptation. In the neuron circuit, the short-circuit current was dramatically suppressed by adopting an FBFET in the inverter. By conducting TCAD mixed-mode simulation of the device and the circuit, the energy consumption of the neuron circuit was investigated. In a single neuron circuit, when input pulses with microsecond durations were applied, approximately 58% energy dissipation was reduced by incorporating the FBFET. In a one-layer SNN simulation, approximately 94% average energy consumption of all output neurons was reduced. Finally, in the proposed neuron circuit, we confirmed from the measurement results that the short-circuit current is completely suppressed until the output spike is generated.

FIGURE 12. (a) Mask layout and (b) SEM image of FBFET. Gate1 and gate2 are overlapped and separated by 10-nm-thick oxide.

FIGURE 13. Measurement results of (a) repeated DC voltage sweep to over 104 times and (b) I-VT curve according to temperature.

VII. CONCLUSIONS

FBFET neurons are demonstrated for the first time and the FBFET successfully co-integrated with conventional CMOS. We not only manufactured steep switching devices, but full neuron circuit and verified the operation of neurons.
The short circuit current, which is the most critical problem of analog circuits is perfectly suppressed by incorporating FBFET in first inverter. The energy consumption of the proposed neuron circuit is independent of the membrane potential rising time and the energy consumption of the proposed FBFET inverter is 371 pJ at both rising times of 50 μs and 100 μs. Therefore, the FBFET inverter can reduce the energy consumption by approximately 50%. In a one-layer SNN simulation, approximately 94% average energy consumption of all output neurons was reduced.

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