Enabling Efficient RDMA-based Synchronous Mirroring of Persistent Memory Transactions

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Synchronous Mirroring (SM) is a standard approach to building highly-available and fault-tolerant enterprise storage systems. SM ensures strong data consistency by maintaining multiple exact data replicas and synchronously propagating every update to all of them. Such strong consistency provides fault tolerance guarantees and a simple programming model coveted by enterprise system designers. For current storage devices, SM comes at modest performance overheads. This is because performing both local and remote updates simultaneously is only marginally slower than performing just local updates, due to the relatively low performance of accesses to storage (e.g., hard drives, flash-based solid-state drives) in today's systems. However, emerging persistent memory (or storage class memory) and ultra-low-latency network technologies necessitate a careful re-evaluation of the existing SM techniques, as these technologies present fundamentally different latency characteristics compared to their traditional counterparts. In addition to that, existing low-latency network technologies, such as RDMA, provide durability guarantees and do not provide durability guarantees necessary for SM.

To evaluate the performance implications of RDMA-based SM, we developed a rigorous testing framework that is based on emulated persistent memory. Our testing framework makes use of two different tools: (i) a configurable microbenchmark and (ii) a modified version of the WHISPER benchmark suite, which comprises a set of common cloud applications, with support for SM over RDMA. Using this framework, we find that recently proposed RDMA primitives, such as remote commit, provide correctness guarantees, but do not take full advantage of the asynchronous nature of RDMA hardware. To this end, we propose new primitives enabling efficient and correct SM over RDMA, and use these primitives to develop two new techniques delivering high-performance SM of persistent memories. Overall, we find that our two SM designs outperform the remote commit based design by 1.8x and 2.9x, respectively.

1. Introduction

Enterprise applications require high-availability and durability guarantees. User data loss or service downtime can have significant economic impact or even lead to bankruptcy. For example, JournalSpace has been shut down due to a complete loss of the company's main database \([50]\). In August 2013, Amazon services stopped operating for a few minutes and the company lost millions of dollars in revenue \([19]\). In such situations, it is of essence for any company to ensure that they can keep serving their users by relying on a different copy of the user data. To provide such uninterruptible business continuity, most companies maintain multiple copies of data in different failure domains.

Synchronous Mirroring (SM) is one of the most widely used approaches to building highly-available storage systems for the enterprise. Technologies like RAID 1, EMC MirrorView/S \([18]\), VMware vSAN \([58]\), IBM Metro Mirror \([24]\), and NetApp SnapMirror \([46]\) provide synchronous mirroring over short distances to ensure high availability and disaster recovery. SM guarantees strong consistency of data by employing (at least) a pair of replica servers that host an exact copy of the application data. SM ensures that in the rare event of a failure, the application can rely on another active replica to continue seamless operation using the most recent version of the data. To provide such a guarantee, the underlying system has to propagate each data update synchronously to all of the replicas. Unlike more weakly-consistent systems, such as asynchronous mirroring (AM), SM (1) guarantees zero data loss; and (2) takes advantage of a simplified programming model, since the programmer does not need to worry about reading an out-of-date replica.

Existing enterprise systems prefer to provide SM instead of weakly-consistent techniques such as AM, even though the weakly-consistent techniques lower performance overheads \([15,24,46,56]\). This is because in existing systems, the additional overhead of performing SM in place of techniques such as AM is relatively small \([62]\). The small overhead is a result of the relatively small latency difference between a local update and a remote update today. In systems that use off-the-shelf magnetic hard disk drives (HDDs) and Ethernet controllers, waiting for a remote update via Ethernet does not take significantly longer than a local update to the HDD. While the relative cost of a remote update over Ethernet increases when the local system uses a solid-state drive consisting of NAND flash memory, prior work \([33]\) has proposed domain-specific operating systems and network stacks that greatly reduce the round-trip latency for a remote update. As a result, the additional overhead of SM over AM remains insignificant in systems with SSDs.

Unfortunately, persistent memory technologies such as PCM, MRAM, ReRAM, and Intel's 3D XPoint \([29,36,37,65]\) make it much more difficult to close the gap. These persistent memories are expected to replace traditional storage devices (HDDs/NAND flash based SSDs) in the near future \([13,48,53]\), and are orders of magnitude faster than current storage media (100,000X faster than HDDs and 1000X faster than SSDs \([53]\)). Since local updates will take much less time with storage class memory, remote SM updates will become even more expensive relative to local updates. Without significant innovation on the remote update latency, it will become increasingly more difficult to amortize and justify the additional overhead of SM over AM.

A promising approach to maintaining the viability of SM for persistent memory is to make use of high-performance networks such as Infiniband \([42]\), which are already becoming commonplace in modern datacenters \([47,68]\). Prior works \([15,53,59,67]\) have already proposed to combine fast Remote Direct Memory Access (RDMA) or Infiniband with the emerging memories to improve the efficiency of SM, but...
these works do not perform a detailed study of how these remote access protocols affect the latency trade-offs between the remote access, local access, and application performance.

Our goal is to understand the performance implications of using RDMA to provide SM for storage class memory, which we refer to as memory-level SM (SM henceforth), and propose new hardware primitives that will enable more efficient memory-level SM. RDMA requires a specialized RDMA-enabled Network Interface Card (RNIC). Applications access the local RNIC directly from user-space to schedule read and write commands to the remote RNICs. The end-to-end latency of RDMA operations depends on the complex interplay between the workload characteristics, processor architecture, and RNIC architecture. Finally, even though RNIC sits on the PCIe bus, it is capable of writing and reading from the CPU cache directly using Intel’s Data Direct Input Output (DDIO) technology [27]. However, because the CPU cache resides outside of the persistence domain [51], enforcing durability in RDMA-based SM is a challenge.

We develop a rigorous testing framework to evaluate memory-level SM using RDMA over an Infiniband network. Our workloads consist of (1) a configurable transaction microbenchmark and (2) applications from the WHISPER [44] benchmark suite that have been extended with support for SM over RDMA. Using our framework and workloads, we find that an SM design that uses the recently proposed remote commit (rcommit) primitive [54] is unable to take full advantage of the asynchronous nature of the RDMA hardware. We find that rcommit is an expensive primitive because it is overloaded to provide both ordering and durability of SM updates. And that significant performance gains can be made by developing separate primitives for ordering and durability and using only the appropriate primitive. Similar insight has been used to improve the performance of single-node persistent memory systems [44,48] and file systems [12].

Inspired by our analysis, we design a new set of RDMA hardware primitives (i.e., verbs): remote ordering fence, remote durability fence, remote write-through, and remote non-temporal writes. These new RDMA primitives aim to unleash the full potential of RDMA hardware and enable efficient memory-level SM. To showcase the new primitives, we propose two SM techniques, one based on ordered buffering, which leverages ordering, durability fences and remote write-through; and another one based on non-temporal writes and the implicit ordering guarantees provided by modern RDMA hardware.

We use our framework to evaluate the effectiveness of our new SM techniques. We find that the techniques provide much greater performance for memory-level SM than remote commit based SM. On average across our benchmarks, we find that our techniques improve the program execution time by 1.8x and 2.9x and the throughput by 1.9x and 3.4x, respectively. Thus, we argue that new primitives allowing for asynchronous updates, such as non-temporal remote writes, will be necessary for efficient SM over RDMA.

We make the following contributions in this work:

- We conduct a detailed study of RDMA-based synchronous mirroring of persistent memory using the existing remote commit verb. We find that remote commit verb does not take full advantage of the RDMA capabilities.
- We identify that remote commit is inefficient as it is overloaded to provide both ordering and durability of SM updates. And that by developing separate primitives for ordering and durability we can significantly reduce the overheads of SM.
- We propose a new set of hardware primitives that are key to performing SM efficiently: remote ordering fence, remote durability fence, remote write-through, and remote non-temporal writes.
- We use our new primitives to develop two new SM techniques that our techniques significantly outperform RDMA-based SM using the remote commit verb.
- We design and implement a benchmark suite comprising of an RDMA microbenchmark and a version of the WHISPER benchmark suite that has been extended for memory-level RDMA-based SM.

2. Background

2.1. Persistent Memories

The emerging non-volatile memory technologies (e.g., PCM [37] and Intel 3D XPoint [61]) provide DRAM-like performance combined with disk-like durability [13,37,48]. These new memory technologies can be used to store and manipulate persistent data directly in-memory. Such systems, referred to as persistent memory systems, have the potential to revolutionize how we manage persistent data and have sparked a wide variety of exciting research recently [2,3,11,13,30,34,38,45,49,55,57,60,63,64,66].

Persistent software running on persistent memory systems requires in-memory data to be recoverable across system failures. Ensuring recoverability requires programmers to have control over the order in which writes/updates reach the data in memory [12,48]. However, in the presence of system failures (power outages, application/kernel crashes, etc.) today’s systems do not provide any guarantees on the order in which writes reach persistent memory due to performance optimizations, like write back caching and memory controller reordering, which coalesce and reorder writes to persistent memory. For example, consider adding a new node to a persistent linked list in memory. The linked list can become inconsistent during an insertion operation if a power failure happens after the pointer to the new node has been persisted in memory, but the write that fills the new node with valid data did not persist in memory. The recovery process of the linked list would observe a node with garbage values. To ensure ordered updates, all the way to persistent memory, programmers have rely on a memory persistency model [48] and annotate their programs with appropriate low-level primitives, like Intel’s clwb [26] instruction.

2.2. Synchronous Mirroring

To guarantee high availability and durability of businesscritical and mission-critical data, system designers employ some form of data replication. SM is a commonly used replication strategy where multiple replicas are kept in sync by propagating every update to all the replicas simultaneously, and is a feature on many commercial storage platforms [13,24,40,58]. In this paper, we limit ourselves to studying a variant of SM that involves only two replicas. All the updates originate at the primary server and are propagated to both local media and to the replica. However, the insights gained from our work can be applied to a much broader class of replication strategies.
Storage-level SM has minimal performance overhead on the system, because storage write occupies significant portion of the latency of the entire persistent update operation (even the remote update) [39].

For memory-level SM, to perform a persistent update, along with issuing a write to local persistent memory (i), the DMA engine fetches the data from the cache (ii) and sends a write request to the replica over the network (iii). Upon receiving the request, the replica server performs a persistent memory write (iv) and then sends back an acknowledgement to the main server (v), completing the persistent update. Since local persistent memory writes are much faster than remote writes (100s of ns vs 1000s of us [53]), the overheads of memory-level SM (over a baseline of just local updates) are prohibitive. Storage-level SM (i.e., mirroring hard disks or SSDS) does not face the same problem because storage write occupies significant portion of the latency of the entire persistent update operation (even the remote update) [39]. To make memory-level SM feasible, system designers need to employ ultra-low latency networks. Next, we present an overview of RDMA, the ultra-low latency network protocol of choice in modern datacenters.

2.3. RDMA

Remote Direct Memory Access (RDMA) is a mechanism enabling a user-level program to directly access the memory of another computer, without interrupting the processors. There are several existing networks that provide support for RDMA, of which the two most widely used are InfiniBand [43] and an implementation using Converged Ethernet. InfiniBand (IB) [43] is a complete network stack consisting of specialized transport, network, link, and physical layers. IB is commonly used in high-performance computing environments and is now making inroads into datacenters. IB offers low-latency and high-throughput communication, as it is implemented entirely in hardware and allows for kernel bypass.

RDMA over InfiniBand requires special network gear, including a specialized switch, the links, and Host Channel Adapters (HCA) or RDMA Network Interface Card (RNIC). For many RDMA applications it is important that the network can guarantee reliable delivery, meaning packets should not be dropped at any point in time. The RNIC implements the entire network stack in hardware, allowing user-level programs to directly interact with the controller and request remote operations. In existing NIC implementation, the memory that is exposed to another server must be first registered with the RNIC [43]. A portion of main memory that has been registered is referred to as a memory region. During registration, the RNIC device driver pins the memory region in order to guarantee that this memory never gets swapped out from physical memory and thus is always accessible for RDMA operations. Registration also makes the virtual-to-physical address translation information (i.e., the page tables) accessible to the RNIC. A special copy of the page table entries that is designated for the RNIC is called Memory Translation Table (MTT). MTT entries reside in memory and are buffered in the HCA cache.

User applications initiate RDMA transfers by sending their requests directly to the RNIC using the verbs API. There are two categories of verbs: messaging verbs and memory verbs. These categories differ in terms of semantics and required inter-process synchronization. In this work, we limit our study to memory verbs due to their lower overheads. Memory verbs are called one-sided operations since the execution of the remote read and write operations does not involve the CPU on the target machine. The lack of CPU overhead at the responder makes one-sided verbs attractive; they provide the lowest latency and highest throughput among all verbs [32].

In this work, we use one-sided RDMA writes to implement synchronous mirroring.

RNICs have been designed to be compatible with commodity servers while, at the same time, providing a low-overhead hardware-software interface. RNIC connects with the rest of the server components using the PCIe bus, where the CPU communicates with the RNIC using PCIe commands. The RNIC uses the PCIe bus to DMA to and from local memory. Most recently, Intel introduced the Data Direct I/O Access (DDIO) [27] feature in its CPUs, allowing RNIC to read and write directly to the CPU cache, reducing the overhead of DMA controller invalidations, which used to be the key mechanism enabling coherent memory accesses in RDMA.

3. PM Transactions

In this work, we assume that the applications modifying persistent memory use a storage transactions [34, 44] for failure-atomicity. Figure 1 shows a typical transaction that uses undo logging to achieve failure-atomicity. Storage transactions do not provide concurrency control and programmers have to use a separate mechanism (e.g., locks) to achieve concurrency control. Next, we describe the guarantees provided by storage transactions and the primitives necessary to provide these guarantees.

Guarantee-1: Failure-atomicity This guarantee provided by the transaction system developer states that either all the updates from a transaction or none of the updates from a transaction are visible during recovery after a system failure. The typical way to achieve failure-atomicity is to employ some form of logging. For example, with undo logging (Fig 1), first a log entry (back up copy) of the data being modified is prepared, then the actual data is modified, and finally the log entry (back up copy) is invalidated to commit the transaction. If during the execution of the transaction a failure occurs, the log entry is used to roll back the partial updates and provide the illusion of failure-atomicity.

To achieve failure-atomicity, a primitive that provides ordering guarantees between different steps of a transaction is mandatory. Without such a primitive, failure-atomicity cannot be provided. For example, in the undo logging trans-
action, the programmer must have a way to ensure that the updates from the PrepareLogEntry step persist before any from MutateDataStructure persist. As long as such an ordering primitive is provided to the programmer, the programmer can develop software crash consistency mechanisms (not just undo/redo logging) to provide failure-atomicity. Henceforth, we refer to portions of a transaction between two successive ordering points as an epoch. So, a transaction may contain multiple epochs, all updates within on epoch may persist concurrently, however, updates from successive epochs must persist in order.

**Guarantee-2: Durability** While failure-atomicity provides a guarantee over what parts of a transaction may persist, the durability guarantee describes when a transaction must persist. The end of a transaction is considered a “durability point,” i.e., after the completion of the transaction, all the updates of the transaction must be persisted. The importance of a durability point is best understood in its contrast with an ordering point. A ordering point simply enforces the order in which two sets of updates (before and after the ordering point) must persist. It does not specify any constraints on when the sets of updates an be considered persisted, that is the responsibility of a durability point. A durability point, once executed past, guarantees that all prior updates have persisted.

**Primitive-1: Ordering Fence** The first primitive, necessary to achieve failure-atomicity, is one that provides ordering guarantees. We refer to a primitive that provides ordering guarantees as an ordering fence (sfence).

**Primitive-2: Durability Fence** The second primitive is one that provides durability guarantees. We refer to a primitive that provides durability guarantees as a durability fence (dfence).

It is important to note that while some architectural proposals [44,48] provide separate primitives to provide ordering an durability guarantees, some architectures overload the ordering and durability functionality on the same primitive (for example, sfence in x86. [35]).

4. Memory-level SM

4.1. SM over RDMA

In this paper, we assume a system implementing Intel’s recently proposed persistency model [26] to ensure local persistence of data. The key instruction introduced as part of this persistency model is the cache line write back (clwb) instruction, which writes back a cache line from the cache to the memory controller write queue. We further assume that the system has support for Asynchronous DRAM Refresh (ADR), mandatory on Intel platforms [28,51], which guarantees that all accepted writeback requests at the memory controller write queue will be drained to persistent memory in the event of a system failure [28,51]. Under this persistency model, two writes to addresses A and B are guaranteed to persist in order A << B, by using the following pseudo-assembly-code sequence:

strA; clwbA; sfence; strB;

The combination of clwb and sfence above ensures that the store to A becomes persistent (by reaching the write queue at the memory controller) before the store to B. And, this programming idiom can be used to provide more intuitive durability guarantees (e.g., transactions) to the regular programmers [14]. For processors which do not support the recently announced clwb instruction, it can be replaced with the more expensive clflush or clflushopt instructions to provide the same persistence guarantees albeit at degraded performance [26].

On top of achieving local persistence of data, to ensure memory-level SM, a programmer has to communicate two important pieces of information to the underlying replication system: (1) the dirty data that needs to be replicated and (2) specify the synchronization point in program where the replication of the identified dirty data has to be completed. For example, in storage-level SM, the file system captures all the necessary information and relays it to the replication system [67]. System calls like fwrite, fappend indicate the dirty data that needs to be replicated while those like fsync, msync specify the synchronization point in the program where the dirty data has to be replicated. Similarly, for memory-level SM, the memory persistency model employed helps capture this information.

For programs annotated with Intel’s persistency model, the clwb instruction (if unsupported, then clflushopt or clflush) identifies the dirty cachelines that need to be persisted and the sfence specifies the synchronization point by which the dirty cachelines have to be persisted. Based on such annotations, one could use RDMA writes to replicate dirty cachelines and enforce ordering and durability guarantees. Using one-sided - RDMA writes is a preferred way of synchronizing mirroring, as it only involves one server. Because of its one-sided nature, RDMA writes are cheaper in terms of latency and throughput compared to two-sided mechanisms, such as RPC. In the following section, we expand on why it is challenging to use one-sided - RDMA operations in SM.

4.2. Challenges in mirroring transactions over RDMA

While mirroring PM transactions, the replication system must be cognizant of the ordering and durability guarantees that must be provided within and at the end of the transaction respectively.

**Ordering challenges:** When mirroring using RDMA, there are many points in the path to the PM on the remote machine that can violate either the ordering or durability or both guarantees necessary to ensure the failure atomicity and durability of transactions. For example, successive RDMA writes may be placed in different Queue Pairs at the local NIC and may be processed in different order. Or, even if the writes reach the remote NIC in the correct order and are processed in the correct order, modern architectures employ DDIO which causes the writes to be written to the LLC of the remote machine. The LLC may then evict the corresponding cacheline in any order. So, any mechanism that replicates transactions must ensure that the writes to remote PM persist in the correct order.

**Durability challenges:** Durability guarantees are also not easily provided when replicating PM transactions over RDMA. When a durability fence is executed, the replication system must ensure that all the prior RDMA writes have been persisted in the remote PM. However, the path for an RDMA write from the local machine to the remote PM consists of many buffers and caches that can cause the request to be buffered at any point (even in the local machine) and not be completed. So, the replication system must deploy mechanisms which guarantee that upon the execution of dfence, the RDMA writes will in fact be persisted on a remote PM.
Both of these challenges stem from the fact that the acknowledgement to an RDMA write request (as shown in Figure 2) is sent before the PCIe write is posted let alone the write becoming persistent.

4.3. Key Goals of This Study

This work aims to understand the performance implications of using RDMA in SM of persistent memories. We would like to understand whether RDMA is well-suited for SM of persistent memories and, if not, identify key performance issues and propose new techniques and hardware primitives that will make SM over RDMA more efficient. The two key questions this paper aims to answer:

- What does it take to enforce ordering and durability guarantees in SM using the rcommit RDMA primitive? And, what is the performance impact of such a replication strategy?
- What are the other possible replication strategies? What primitives / hardware extensions do they require? And, how to reduce the performance overhead of SM using RDMA?

5. Replication Strategies

In this section, we describe several strategies to synchronously mirror the contents of persistent memories and we evaluate each of these designs in subsequent sections.

**NO Synchronous Mirroring (NO-SM):** NO-SM is a replication strategy where we do not perform any replication but just persist data locally. While no credible replication strategy can realistically match the performance of NO-SM, it provides a hypothetical upper bound on the possible performance and also helps us measure the costs introduced by various replication strategies. Table 1(a) shows the code of a sample transaction with two epochs implemented using Intel’s x86 extensions for PM programming (clwb and sfence).

**SM using Remote Commit (SM-RC):** Recently, there has been a push towards using single-sided RDMA verbs (like RDMA read() and write()) to avoid the overheads of interrupting the processor on the remote machine. These read() and write() requests are completely handled by the receiving NIC without ever interrupting the associated CPU. However, the challenge with using single-sided RDMA verbs for SM is that the completion of the write() verb does not provide any guarantees on whether the corresponding data persisted on the remote machine. Upon receiving a completion acknowledgement, the sender of the write() message is just guaranteed that the write command has been communicated to the remote NIC. The remote NIC may subsequently (at some future point) post a PCIe write command to write the corresponding data to the LLC of the attached processor (due to DDIO support). Current PCIe interface does not provide any mechanisms to query if a posted write command has been completed. Furthermore, even if the NIC can be assured that a posted PCIe write command is complete, the data has only been written to the LLC that is volatile and may lose its contents in the event of a system failure. To achieve persistence, the corresponding data has to be written back from the LLC to the memory controller.

One way to achieve the persistence of data written to the LLC is to have a “flusher” thread running on the dedicated core in the processor and periodically interrupt the thread and request it to flush the data from the LLC. However, that approach wastes valuable processor resources. Taley and Pinkerton [54] propose a single-sided RDMA verb called rcommit to tackle this problem. The completion acknowledgement of an rcommit message guarantees to the sender that all prior issued RDMA writes are complete and that they are written back to the memory controller and hence persistent. NICs that support the rcommit primitive receive as input the range of memory addresses to be flushed to the persistent memory and have to ensure that all cachelines that belong to the specified range reach the memory controller before sending a completion acknowledgement. Figure 2(a) shows how an rcommit writes back all the cachelines touched by prior writes from the cache hierarchy to the persistent memory controller. We discuss the implementation details of rcommit and how we model it in §6.

rcommit is both an ordering and durability primitive as the completion of an rcommit ensures that all prior RDMA writes are durable. That is, RDMA writes separated by an rcommit will necessarily persist in order. So, an rcommit is an overloaded primitive (like an sfence) that provides both ordering and durability guarantees. Table 1(b) shows the code a sample transaction with two epochs being replicated using the SM-RC approach. For each clwb encountered, an RDMA write is issued and at the end of every epoch (indicated by an sfence), an rcommit is issued, whether its for intra-transaction ordering guarantees or for the end of transaction durability guarantees.

**SM using Ordered Buffering (SM-OB):** In this design, we propose to decouple RDMA primitives for ordering and durability of remote writes. We introduce a new primitive called rofence, that ensures the ordering of remote writes, while a separate rdfence primitive ensures their durability. The rofence demarcates different epochs within a transac-
table 1: the code transformations necessary to implement various replication strategies discussed in this section.

| LOCAL | SM-RC | SM-OB | SM-DD |
|-------|-------|-------|-------|
| 1     | (a)   | (b)   | (d)   |
| 2     | LOCAL | SM-RC | SM-DD |
| 3     | LOCAL | SM-RC | SM-DD |
| 4     | Start Tx | Start Tx | Start Tx |
| 5     | St A; CLWB A; | St A; CLWB A; | St A; CLWB A; |
| 6     | RDMA Write A; | RDMA Write (WT) A; | RDMA Write (NT) A; |
| 7     | St B; CLWB B; | St B; CLWB B; | St B; CLWB B; |
| 8     | RDMA Write B; | RDMA Write (WT) B; | RDMA Write (NT) B; |
| 9     | SFENCE; RCOMMIT; | SFENCE; ROFENCE; | SFENCE; RCOMMIT; |
| 10    | St C; CLWB C; | St C; CLWB C; | St C; CLWB C; |
| 11    | RDMA Write C; | RDMA Write (WT) C; | RDMA Write (NT) C; |
| 12    | St D; CLWB D; | St D; CLWB D; | St D; CLWB D; |
| 13    | RDMA Write D; | RDMA Write (WT) D; | RDMA Write (NT) D; |
| 14    | SFENCE; ROFENCE; | SFENCE; ROFENCE; | SFENCE; ROFENCE; |
| 15    | $ $ $ | $ $ $ | $ $ $ |
| 16    | End Tx | End Tx | End Tx |

**Figure 3:** This figure depicts some of the new RDMA primitives proposed to enable and improve the performance of SM. (a) Depicts conventional RDMA writes and the new `rcommit` primitive used in SM-RC. (b) Depicts Write-Through writes (RDMA Write(WT)) that modify data in the LLC and then write back the data to the memory controller, a subsequent `rofence` forces them to completion (c) Depicts Non-Temporal writes (RDMA Write(NT)) that directly write data to the memory controller bypassing the LLC.

Our approach allows all writes in the same epoch to be processed concurrently while writes in different epochs will be persisted in order. While processing a write request, it is not enough for a remote NIC to simply post a PCIe command as that would result in the data being written to the LLC only. We introduce a new PCIe command to allow the data to not only be written to the LLC but also to be written back to memory controller. We refer to this new PCIe command as a Write-Through Write (Write (WT)).

Table 1(c) shows a sample transaction with two epochs being replicated using the SM-OB approach. For every clwb encountered, a RDMA write with Write-Through attribute is issued. Further, an `rofence` is issued at the end of each epoch within a transaction to achieve ordering guarantees while an `rofence` is issued at the end of the transaction to achieve durability guarantees.

**Discussion:** The main benefits of disabling DDIO for the purposes of SM are: (1) the RDMA writes are faster as they can now bypass the LLC and directly reach the persistent memory controller, (2) the overheads of `rofence`, like additional RDMA commands incurred, are completely eliminated, and
(3) designing the replication system is simpler as the designer is relieved of the burden of accurately identifying and placing the appropriate reference commands. However, the downsides of this approach are: (1) all the RDMA writes issued for SM are routed through a single QP (for ordering purposes), failing to take advantage of the parallelism provided by multiple QPs at the NIC, and (2) today’s computer systems have multiple timers, so disabling DDIO for the benefit of one application might hurt the performance of other applications. While the first concern is fundamental to this approach, the second can be eliminated by a feature that can enable/disable DDIO on a per application or on an per QP basis.

While SM-DD is implementable on certain select motherboards (which we unfortunately do not have access to), SM-RC and SM-OB are not feasible on current systems as they require support for new RDMA verbs and PCIe commands. To make a fair comparison of the different approaches, we develop an emulation methodology that we describe next and then present a comprehensive performance analysis of the different approaches.

6. Methodology

While SM for Persistent Memories is important, efficient mechanisms to enable SM are yet to be developed. The mechanisms that we are proposing in this paper need new primitives that are not available in today’s computing systems. To estimate the performance impact of our proposed techniques, we model the latencies of the necessary remote memory operations that are currently not available. To this end, we create a precise model of the last level cache (LLC) and the memory controller and investigate how local and remote operations interact with this model. We use this model to measure delays when interacting with the memory subsystem. We combine these delays with actual RDMA network traffic to gain insights and compare end-to-end performance of SM for Persistent Memories using techniques proposed in this paper (SM-OB and SM-DD) and the existing SM-RC proposal.

We first describe our model of the last level cache and the memory controller before discussing how we estimated the performance of our new primitives.

6.1. Modeling the LLC and the Memory Controller

Given a certain physical address, we can find the LLC cache set in which it will be stored using existing models for Intel processors [41]. On the remote side, we measure that 10% of each cache set in L3 is dedicated to DDIO traffic (2 out of the available 20 ways in the Xeon E5-2630 v3 processor in our test bed). Hence, assuming a least recently used (LRU) policy for DDIO traffic and the knowledge of physical addresses of the remote RDMA buffer, we can predict how each RDMA write will change the state of the remote cache and could potentially evict items from the LLC.

Assuming a system with DDIO support, items that are evicted from the LLC will end up in the memory controller queue before being written to the persistent memory. Since the memory controller is part of the persistent domain, we need to ensure that the items enter this queue in the correct order. In systems without DDIO support, the writes from the network (i.e., from PCIe) will directly enter the memory controller’s queue in the same order that they arrive.

Note that once the memory controller’s queue is full, the items cannot be inserted either from the LLC or the network. In this case, a back-pressure mechanism ensures that we can no longer send write requests to the remote server. Assuming a processor with a certain number of cache sets, our model takes four parameters as input: the latency of a PCIe write to the LLC (default - 200ns round-trip), the latency of a write from LLC to the memory controller’s queue (10ns), the size of the memory controller’s queue (64), and the latency of a write from the memory controller’s queue to the persistent memory (150ns). Once configured, our model can estimate the latency of a given memory write at a certain address with a given size.

6.2. Modeling Persistent Memory Primitives

We now describe the individual remote and local memory access operations and how we model them.

CacheWriteback (CLWB). The clwb instruction writes back dirty cachelines from the cache hierarchy to the memory controller. The instruction initiates a writeback and the programmers have to use a subsequent sfence to ensure the completion of all prior clwb instructions.

The clwb instruction is going to be available in the Skylake server micro-architecture. To model clwb, we rely on our model tag the cachelines that should be written to the memory controller’s queue eagerly. At each clwb, we calculate how many previously tagged cachelines have had time to have been eagerly sent to the memory controller. To model sfence, we calculate how many tagged cachelines still need to be written to the memory controller and return the necessary delay for these writes to be completed.

RemoteCommit (Rcommit). rcommit is a new RDMA verb being proposed in the RDMA standard to writeback the cachelines touched by all prior RDMA write operations from the LLC to the memory controller on the remote machine. The completion of an rcommit indicates that all prior RDMA writes have been persisted on the remote machine.

To estimate the latency of an rcommit, we treat is as being two separate operations performed in series. First, the round trip to the remote machine, that involves setting up the QP entry, draining it on the local NIC, receiving it on the remote NIC, issuing the appropriate PCIe command and finally sending a response back. Second, the actions performed on the remote machine, that is the write back operations. Hence, we model an rcommit as being two operations performed in series, a remote RDMA read (to estimate the latency of a round trip) and the price of draining the previously written cachelines that are still present in the LLC as estimated by our model. This also means that some RDMA write operations may observe increased latency if the target cache set and the memory controller’s queue are both full.

Remote Writes Write-Through (rntw) and Non-Temporal (rntw). rntw and rwtw are new RDMA primitives we introduce to write the cachelines directly to the memory controller instead of just writing them to the LLC. When an application issues these new RDMA verbs and it is received on the remote NIC, the remote NIC tags the cachelines associated with this write to be either directly sent to the memory controller bypassing the LLC (rntw) or written through from the LLC to the memory controller (rwtw) from the PCIe root complex.

To estimate the latency of an rntw or rwtw, we treat it as being two separate operations performed in series. First, the round trip to the remote machine, that involves setting up the queue pair entry, draining it on the local NIC, receiving it on the remote NIC, issuing the appropriate PCIe command and finally sending a response back. Second, the action performed on the remote machine. For the non-temporal write (rntw), we use our model to estimate the latency assuming no DDIO
support (i.e., writes directly go to the memory controller’s queue). For the write-through write (rwtw), we use the same estimation from our model as clwb.

**Remote Ordering Fence (rofence).** rofence defines ordering points within the execution of an application where the hardware must ensure that all prior issued RDMA writes or rwtw or rwtw are guaranteed to persist before any subsequent RDMA writes. The exact mechanism by which the hardware provides this guarantee is left up to the discretion of the hardware designer. One possible implementation is that the remote NIC receiving the RDMA write and rofence commands, places them in a single FIFO queue.

To estimate the latency of an rofence, we simply treat it as an RDMA write which incurs a standard round trip latency. The reason for this choice is that the rofence, like an RDMA write, simply notifies the remote NIC of certain action to be performed (the write for RDMA write, while the ordering specification in case of rofence) and does not actually force the completion of any action on the remote machine.

Such a queue introduces two sources of overheads: (1) it serializes the commands that are received from multiple independent threads/applications, (2) it does not allow any reordering of RDMA writes between successive rofence commands. Hardware designers may implement optimized versions of the queue that mitigates one or both of the overheads described. Note that rofence does not change the state of the LLC and/or the memory controller’s queue and hence need not to interact with our model.

**Remote Durability Fence (rdfence).** rdfence defines the durability points within the execution of an application where the hardware must ensure that all prior issued RDMA writes are guaranteed to persist before the completion of the rdfence command. Note that while persisting data due to an rdfence command, the hardware must still provide the ordering guarantees specified by any prior rofence commands.

To estimate the latency of rdfence command, we treat it as two separate serial operations, a round trip and draining writes to the persistent memory, similar to an rcommit command. The notable exception for rdfence is that the cachelines are eagerly written to the memory controller’s queue from the LLC, following the same mechanism as clwb. The latency of the writes to the persistent memory is hence estimated by our model similar to clwb.

### 6.3. Experimental Setup

To evaluate memory-level SM on RDMA, we build an RDMA test-bed based on Infiniband. Our test-bed assumes the following server configuration; an Intel Xeon E5-2630 v3 CPUs running at 2.4GHz and DDR4 memory. Our platform is based on Mellanox ConnectX-3 40Gbps RDMA network adapters. The IB platform is equipped with Infiniband SX6036 switch. A detailed summary of our platform is presented in Table 2.

**Platform disclaimers:** Our platform does not support the newly introduced clwb or clflushopt instructions, so we use the clflush instruction in our programs. The RDMA write verb, once completed on current hardware does not guarantee that the data has been persisted to the remote memory, instead, it just guarantees that a PCIe write for the data has been posted in the remote machine. This problem is already being addressed by the industry [53] and we expect future RNICs to close this vulnerability.

| **Table 2: RDMA platform** |
|-----------------------------|
| **Component** | **Platform** |
| CPU | Intel Xeon E5-2630 (2.4GHz) |
| Memory | DDR5 - 2400MHz (16x16GB DIMMs) |
| Network | Infiniband (40Gbps) |
| RNIC | Mellanox ConnectX-3 |
| Switch | SX6036 (w/FDR) |

### 7. Evaluation

To compare the performance of the different replication strategies, we instrument a microbenchmark and workloads from the WHISPER [44] with the primitives detailed in [5] and execute them on our test-bed with our model.

#### 7.1. Microbenchmarks

Our microbenchmark, **Transact**, executes 1M transactions, each of which is replicated. **Transact** allows configurable number of epochs per transaction and further, configurable number of writes per epoch. However, once configured, all the transactions have the same number of epochs per transactions and writes per epoch. We vary the number of writes per epoch from [1 ... 8] and the number of epochs per transaction from [1 ... 256]. The ranges were decided based on the analysis of persistent memory workloads presented by Nalli et al. [44], which showed that applications exhibit very few writes per epoch, but can exhibit hundreds of epochs per transaction. The addresses of writes within a transaction are randomly chosen.

Our goal with this study is to understand the suitability of different replication strategies to different kinds of transactions - small transactions, large transactions, ones with fewer epochs, etc. We evaluate Transact on the platform described in Section 6.3. Figure 4 shows the slowdowns incurred with different replication strategies over a baseline of NO-SM, where no replication is performed. The x-axis labels are of the form $e - w$, where $e$ represents the number of epochs per transaction and $w$ represents the number of writes per epoch used in Transact. For example, a configuration of 16 – 2 indicates that there are 16 epochs per transaction and 2 writes per epoch. We make three major observations from Figure 4.

**First, SM-RC incurs the highest performance overheads.** As Figure 4 shows, SM-RC incurs the highest slowdowns for all different Transact configurations, ranging from about 20x to over 55x. SM-RC uses expensive rcommit verbs to ensure ordering and durability guarantees and the frequent use of this primitive results in the high overheads. These overheads are highest for transactions with only 1 write per epoch and gradually reduce with increasing number of writes per epoch. This behavior is to be expected as higher number of writes per epoch allows the an expensive rcommit verb to be amortized over a larger number of asynchronous RDMA writes.

**Second, SM-OB and SM-DD consistently outperform SM-RC.** Both SM-OB and SM-DD outperform SM-RC for all Transact configurations by as much as 3.5x (for Transact 4-1). The main reason for the performance advantage of SM-OB and SM-DD is that they eliminate the use of blocking rcommit verbs to ensure intra-transaction ordering guarantees. The
performance difference is especially high when Transact has a low number of writes per epoch, due to a high ratio of rcommit verbs per write.

Third, SM-OB and SM-DD are suitable to different kinds of transactions. Controlling for the number of writes per epoch within a transaction, SM-OB performs better for transactions with higher number of epochs per transaction while SM-DD performs better for transactions with lower number of epochs per transaction. This trade-off in performance with SM-DD and SM-OB is to be expected as they optimize different aspects of SM. For example, SM-DD reduces the number of blocking ordering enforcement points than SM-OB by eliminating the need for rence primitive. However, SM-DD increases the latency of individual RDMA write operations by forcing each write to be written directly to the memory controller. Furthermore, SM-DD may cause frequent pauses to write processing at the remote NIC as it might cause the small write queue (64 entries, 4KB) at the memory controller to fill up while SM-OB allows the remote NIC to process more requests to buffer more writes in the LLC (up to 2MB as described in Section 6). For these reasons SM-DD is more efficient for small transactions while SM-OB is more efficient for larger transactions.

Discussion. With the optimized cache flush instructions (clflushopt and cwb), we expect the time to perform local flush operations to reduce significantly providing fewer opportunities to overlap remote RDMA writes and local flush operations resulting in higher performance overheads even for larger transactions. However, Transact is dominated by writes and real applications with less frequent write operations can expect lower overheads. Next, we analyze the overheads experienced with real applications from the WHISPER [44] benchmark suite.

7.2. WHISPER applications

In this subsection, we first present a quick overview of persistent memory applications from the WHISPER [44] benchmark suite and then show the overheads of employing memory-level SM for these workloads.

C-Tree is a multi-threaded benchmark that performs inserts and deletes on a persistent crit-bit tree data structure. This workload was initially released as part of NVML [25].

Echo mimics the behavior of a persistent key-value store. The benchmark consists of a master thread that manages the store and many client threads that send updates to the store.

Hashmap is a multi-threaded benchmark that performs inserts and deletes on a persistent crit-bit tree data structure. This workload was initially released as part of NVML [25].

YCSB and TPCC are two transaction processing workloads operating over N-store, a relational database management system designed from scratch for persistent memories.

Figure 4: Slowdowns seen due to SM of Transact with different replication strategies over a baseline of NO-SM. The x-axis labels are of the form \( e = w \), where \( e \) represents the number of epochs per transaction and \( w \) represents the number of writes per epoch used in Transact.

Figure 5: Changes in the execution time and throughput due to SM for different WHISPER workloads.

Next, we delve in the performance of different replication strategies for these workloads.

**SM-DD > SM-OB > SM-RC.** Figure 5 highlights the increased execution times and decreased throughputs for the WHISPER applications described above for various replication strategies. As with Section 7.1, the measurements presented for each platform are normalized over NO-SM. We draw two key observations. First, SM-RC, on average, increases execution time by 6.7x, while SM-OB and SM-DD increase execution times by only 3.8x and 2.3x, respectively. Hence, SM-OB and SM-DD outperform SM-RC by 1.8x and 2.9x, respectively. Second, SM-RC decreases throughput by 85%, while SM-OB and SM-DD decrease throughput by only 73% and 52%, respectively. SM-DD consistently performs best, while SM-RC performs worst.

**Workload characteristics.** The relative performance of SM-RC, SM-OB, and SM-DD are to be expected based on the characteristics of the workloads. These benchmarks have only a modest fraction of all the write instructions executed during the applications and update persistent data (about 5%) [44]. We expect that the performance degradation due to memory-level SM for different applications will be largely determined by the fraction of accesses to persistent data, with
applications having higher fractions of accesses to persistent data seeing more performance degradation. The rest of the write instructions in the application arise due to modifications to volatile data structures not necessary for crash consistency. Furthermore, the average number of writes per epoch for these workloads is only 1.4. A disproportionate number of epochs in most of the workloads modify only one cacheline worth of data. However, the average number of epochs per transaction vary significantly for the various workloads from about 10 (hashmap) to over 300 (echo). Based on the low number of writes per epoch in these workloads and our analysis of the microbenchmark Transact, we can expect SM-DD to perform best.

8. Related Work

In this section, we present a brief overview of the research most relevant to our work.

RDMA Applications. The use of RDMA has gained popularity as a communication mechanism in many distributed database systems and algorithms. In the context of join algorithms, the costs of large data transfers can be significantly reduced by interleaving compute and communication, and by avoiding intermediate copies through the use of one-sided memory operations [7]. These algorithms have been shown to scale to several thousands of cores and are able to achieve a high throughput [8]. RDMA is used in BatchDB as a low-latency communication mechanism to replicate data to multiple workload-specific replicas in order to maintain strict performance, data freshness, and consistency requirements [40]. Many distributed database systems have explored RDMA communication primitives as part of their query pipeline in order to speed up query response times [30, 52], while others have been re-designed from the ground up with RDMA in mind [6, 9]. Key-value storage systems make use of high-performance networks to enable low-latency access to remote data [16, 32].

Persistent memory systems. Emerging persistent memory technologies present a paradigm shift in storage technologies and have set off an assortment of research projects in the areas of persistent data structures [30, 45, 57], file systems [2, 13, 17, 60, 64, 66], transaction logging techniques [3, 11, 34, 38, 49, 63], and many more. Many recent works, both from academia and industry, have also sought to develop new programming models [26, 31, 44, 48] to program for persistent memory systems and have also developed architectural solutions to efficiently implement these models [31, 35, 44]. However, all of these works assume that data is “persistent” as soon as it reaches local persistent memory, as assumption that cannot be employed in large scale multi-node systems.

Replicating persistent memory data. Replicating data to ensure high-availability and high-durability is a widely used approach [11, 10, 14, 20, 22]. While many different replication techniques are used, synchronous mirroring (SM) is a common feature of enterprise storage solutions [18, 23, 24, 46, 58]. For conventional storage and network technologies, the strong consistency guarantees of SM comes at a very low performance cost [39]. However, with the emergence of persistent memory technologies a reevaluation of the costs of SM have to be reevaluated.

Recent proposals from the Storage Networking Industry Association (SNIA) [4, 53] indicate that both hardware manufacturers and software developers are looking to enable efficient remote persistent memory access over RDMA. Mojim [67] enables SM for persistent memories and most closely resembles the systems envisioned in our work. However, one major difference is that Mojim is designed to provide SM for file systems mounted on persistent memories and not designed to support the newer persistent memory programming interfaces [5]. Unlike the file systems, these newer interfaces expose a byte-addressable storage media to the programmers, resulting in fine-grain accesses (a few cachelines at a time [44]).

9. Conclusion

In this work we propose a set of new RDMA primitives that aim to improve the efficiency of persistent memory mirroring. On top of that, we propose two novel SM techniques that leverage the new primitives to unleash the full potential of modern RDMA hardware. The first technique is based on ordered buffering, while the other one uses non-temporal remote writes to ensure ordering and durability guarantees. We add the support for SM in the WHISPER benchmark suite and use a microbenchmark to evaluate the performance of our two proposals and compare them to a prior proposal based on the remote commit RDMA verb. We conclude that ordered buffering and non-temporal writes enable highly concurrent SM and outperform designs that use remote commit.

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