AN IMPROVED QUADRATURE VOLTAGE-CONTROLLED OSCILLATOR WITH THROUGH-SILICON-VIA INDUCTOR IN THREE-DIMENSIONAL INTEGRATED CIRCUITS

ABSTRACT

Low-power quadrature voltage-controlled oscillator (QVCO) design utilizing transformer-feedback and current-reuse techniques with increased frequency range is proposed in this paper. With increasing demand for QVCOs in on-chip applications, the conventional spiral inductor based approaches for QVCOs has become a major bottleneck due to their large size. To address this concern, we propose to replace the conventional spiral inductor based approaches with through-silicon-via (TSV) inductor based approach in three-dimensional integrated circuits (3D ICs). In addition, the proposed QVCO circuit can provide higher frequency range of operation compared with conventional designs. Experimental results show by replacing conventional spiral transformers with TSV transformers, up to 3.9x reduction in metal resource consumption. The proposed QVCOs achieves a phase noise of $-114 \text{ dBc/Hz} @ 1 \text{ MHz}$ and $-111.2 \text{ dBc/Hz} @ 1 \text{ MHz}$ at the carrier of 2.5 GHz for toroidal TSV transformed based-QVCO and vertical spiral transformer based-QVCO respectively. The power consumption is only 1.5 mW and 1.7 mW for toroidal TSV transformed based-QVCO and vertical spiral transformer based-QVCO respectively, under the supply voltage of 0.7 V.

Keywords On-chip oscillators · 3D ICs · Quadrature voltage-controlled oscillators · TSV inductors

1 Introduction

Voltage-controlled oscillator (VCO) is an essential component and extensively used for various on-chip applications i.e., phase-locked loops (PLLs) [1, 2, 3], clock distribution networks, signal generators, function generators, communication networks [4] etc. For all these applications, a VCO with low-power, low-noise, and low-resource consumption is desired because the VCO usually works at higher frequencies, and is the most power-hungry block as the power dissipation is proportional to the operating frequency [3, 4]. Hence, an efficient VCO design for these applications is required.

VCOs can be implemented in two ways: 1. Active VCO and 2. Passive VCO. Active VCOs do not contain passive inductor and hence these VCOs can be compact on-chip [5]. However, they do not perform well at higher frequencies due to high jitter associated with the transistors. The active VCOs also suffer from a severe frequency drift caused by the parasitic capacitors and resistors. Passive VCO works well at higher frequencies which most applications need and
also has low jitter compared with its active counterpart due to the reduced noise. Therefore, passive VCOs are more practical and attractive for various applications. In the rest of the paper, VCO refers to the passive VCO unless specified.

Inductors required for VCO can be implemented in various approaches: 1. Off-chip Inductor, 2. On-package inductor and 3. On-chip inductor. Off-chip inductor is bulky and is not practical for condensed integration \cite{6,7}. On-package inductor suffers from poor scalability \cite{8}. Therefore, current research focuses on implementing on-chip inductors effectively for various applications.

Conventional on-chip spiral inductors occupy huge metal routing resources which limits the number of inductors that can be implemented on-chip. The following works discuss about the implementation of conventional on-chip inductors and their metal resource consumption:

- On-chip DC-DC converters with a conventional spiral inductor designed in \cite{9} requires 78, 400\umu m^2 of metal area, equivalent to the area of 62K gates in 45\,nm technology.

- A 5\,GHz MIMO transceiver with 20 on-chip inductors implemented in \cite{10} occupies a huge area of 18\,mm^2.

- A variable bandwidth 3-4 GHz transceiver for Internet of Things (IoT) applications is proposed in \cite{11} has 10 optimized on-chip circular shape spiral inductors with an area of 5.6\,mm^2.

These on-chip planar inductors usually occupy large area, contributing to an increasing manufacture cost which is one of the main concerns for future ubiquitous applications. Therefore, compact on-chip inductors are needed for effective implementation of on-chip inductors for various applications.

On the other hand, three-dimensional integrated circuits (3D ICs) have become a promising alternative to keep Moore’s law since an extra dimension makes chip size smaller. This technology has gained popularity for high computing devices like large scale processors as well as for compact devices like mobile chips. While there are many challenges still exist in 3D IC practicality, a major one is related to TSVs because they are huge and they do not scale with logic gates. In addition, lot of dummy TSVs are needed to be inserted to satisfy minimum density rule due to chemical mechanical polishing purposes. For example, Tezzaron needs one TSV for every 250\,\umu m \times 250\,\umu m area \cite{12}. This further increases the overhead by TSVs. One way to address this problem is to make on-chip devices using TSVs and utilize them in on-chip applications.

In our previous works, we addressed the on-chip inductor metal resource consumption by replacing the conventional spiral inductor with TSV inductor for on-chip regulator and resonant clocking applications \cite{13,14,15,16,17,18,19,20}. For on-chip regulator applications \cite{13,14,15,16,17,18,19,20}, the inductor area reduced by upto 4.3x by replacing spiral inductor with TSV inductor for the same performance of the regulator. For resonant clocking applications \cite{15,16,17}, the inductor area reduced by upto 6.3x by replacing spiral inductor with TSV inductor for the same power reduction. Also, micro-channel shielding technique \cite{13,14} is proposed to make TSV inductors practical at high frequencies. For these applications, TSV inductors are effective in reducing the metal resource consumption.

VCO is another important component that is required for various on-chip applications. Conventionally on-chip VCO is designed by utilizing conventional spiral inductor which may not be efficient in utilizing the metal routing resources effectively. Towards this, we propose to use TSV inductors with novel coupling structures to enable efficient implementation of VCO. With these objectives, the main contributions of this work are as follows:

1. Quantitative analysis of the Quadrature voltage controlled oscillator (QVCO) is discussed in detail.

2. We propose to use novel transformer structures using TSV inductors to design QVCO. Compared with conventional spiral implementation, TSV inductor based transformers will better utilize the metal routing resources.

3. We design a low-supply QVCO with proposed TSV transformers. To author’s best knowledge, this paper is the first to design a TSV-based QVCO under a 0.7V supply.

The remainder of the paper is organized as follows: Section 2 reviews the background on VCO and TSV inductor design. A detailed description of QVCO design and the importance of transformer design on the performance of QVCO is given in Section 3. Novel TSV inductor structures to implement on-chip transformer for the design of QVCO is discussed in Section 4. Simulation results of this QVCO and the comparison with other works is presented in Section 5 and concluding remarks are given in Section 6.
2 Preliminaries

2.1 Basic VCO

VCO generates sinusoidal signals whose frequency is varied with the input voltage of the oscillator. This circuit is extensively used in the design of integrated circuits (ICs) for various applications that include function generators, clock generators, phase-locked loops, wireless transceivers etc. VCO is usually power hungry due to its higher frequency of operation and hence an efficient VCO design is required.

The circuit diagram of a basic VCO is shown in Figure 1. This circuit has three components: 1. LC tank, 2. NMOS cross-coupled pair and, 3. Constant current source. This circuit generates oscillations with the resonance frequency given by the equation (1) which is determined by the LC tank of this circuit when it is properly designed. Here \( L_{eq} \) and \( C_{eq} \) are the equivalent inductance and capacitance of the LC tank considering the parasitics of these components when implemented on-chip. The NMOS cross-coupled pair helps to achieve the phase shift of 360° across the loop at the resonance frequency and compensates for the series resistance of the inductor for the oscillations to sustain. Current source helps to lower the supply voltage sensitivity for stable operation. For the circuit to oscillate at the resonance frequency, the loop gain should be greater than 1 and can be achieved when \( R_L \geq \frac{g_m}{2} \) where \( R_L \) is the equivalent series resistance of the inductor and \( g_m \) is the transconductance of the NMOS transistor in the cross-coupled pair. Therefore, with proper sizing of the cross-coupled pair transistors and the input bias, this circuit generates oscillations with resonance frequency. For the VCO, the oscillation frequency is controlled by the input voltage \( V_c \). This property can be achieved by implementing a variable MOS capacitor with the input voltage.

\[
\omega_{osc} = \frac{1}{\sqrt{L_{eq}C_{eq}}} \tag{1}
\]

Another important aspect with the design of VCO is to meet the specifications for the given application. The important specifications correspond to the VCO design are center frequency \( f_c \), tuning frequency range \((f_{min} \text{ to } f_{max})\), VCO gain \( K_{VCO} \) and phase noise. Center frequency \( f_c \) and tuning frequency range \((f_{min} \text{ to } f_{max})\) are determined by the frequency standards for the protocol environment like mobile communications, PLL design etc. VCO gain \( K_{VCO} \) is determined by the control voltage sensitivity of the VCO and should be as small as possible in order to avoid stability issues. Phase noise \( \phi_{noise} \) is another important specification which is a measure of signal quality in the frequency domain that determines the frequency fluctuations in a signal and is usually measured at 1 MHz.

Since most of the current wireless communication systems like LTE and WiMAX [2] are employing quadrature modulation for up- and down-conversion, Quadrature VCOs (QVCOs) are developed by coupling two differential VCOs. Therefore, QVCO requires additional inductors and thus demands more metal resources for their on-chip implementation. Towards this, in this work we propose to use TSV inductor based QVCO for compact design with better efficiency.
2.2 On-chip Inductors

The major bottleneck for many applications that need inductors to fully integrate on-chip is the metal resource consumption especially by the conventional spiral inductor technique. Hence it is crucial to have a high-inductance density on-chip inductor with the desired quality factor Q. In our previous works, we tackled this challenge by designing TSV inductor that performs on-par with the conventional spiral inductor for on-chip regulator and resonant clock distribution network applications with the metal resource consumption reduced by upto 6x, which is a huge benefit for realizing more on-chip applications that need inductors.

![Three-turn toroidal TSV inductor](image)

A simple three-turn toroidal TSV inductor structure is shown in Figure 2. From the figure, we can see that the TSV inductor is buried in the substrate and hence the substrate losses are higher compared with the conventional spiral inductor. Our previous work \cite{14} shows that these losses are not significant for low-frequency range and can be reduced by using micro-channel etching technique at high frequencies to make them practical.

As discussed earlier, on-chip QVCO implementation demands huge metal resources and has become a tradeoff for many applications that require QVCO especially for LTE, WiMAX etc. In order to make QVCO designs more practical for on-chip implementation in 3D technology, we propose to utilize TSV inductor structures that require less metal resources compared with the conventional spiral inductor structures.

3 Transformer-feedback Current-reuse QVCO

In this section, we discuss about the design and analysis of QVCO for low power applications by combing two techniques: 1. Transformer feedback and, 2. Current reuse. We first discuss briefly about these techniques individually on the two-phase VCO and then we present a circuit topology for low-power QVCO that combines both these techniques.

![Circuit diagram of a TF-VCO](image)
The simple differential VCO circuit shown in Figure 1 cannot be used for the low supply voltage operation due to the limited voltage headroom by the tail current source and the active circuits. The simple differential VCO circuit can be modified by utilizing transformer as shown in the Figure 3 and this modified circuit is called two-phase transformer-feedback VCO (TF-VCO). With the two-phase TF-VCO, the output voltage can swing above the supply voltage $V_{dd}$ and below the ground potential. Also, the drain and source signals are in phase for this TF-VCO circuit [22]. Therefore, the oscillation amplitude range for this circuit is increased for the given supply voltage. In other words, we can reduce the supply voltage for the given oscillator specifications i.e., phase noise and oscillation amplitude and hence the power consumption can be reduced. Another advantage with this technique is the improved voltage sensitivity due to the transformer and hence the tail current supply is not required.

Current reuse VCO (CR-VCO) is another modified circuit of the differential LC-VCO circuit shown in Figure 4. With this circuit [23], the supply current is lowered by up to 50 %, which means that the power consumption of this VCO will be reduced to half compared with the conventional differential LC-VCO for the same supply voltage. This supply current reduction is achieved by turning on both PMOS and NMOS of the CR-VCO in the first cycle where the current flows from $V_{dd}$ to gnd through the inductor and in the second cycle both NMOS and PMOS are off and the current flows through the internal capacitances.

As discussed earlier, QVCO with low-power and low metal consumption is highly desired for many applications. In this work, QVCO is designed by combining both transformer-feedback and current-reuse techniques based on [24]. With this approach, power consumption is reduced significantly by reducing supply voltage and supply current but the inductor required to design this QVCO demands metal resources which we will address in Section 4 with the TSV based transformer design. The circuit diagram of the proposed QVCO is shown in Figure 5 can be divided into three blocks as shown in Figure 5:

1. Main block: It comprises of two identical differential CR-VCOs with two switching transistors for each. Hence, the minimum voltage headroom for this circuit is $2V_{DS}$. Two identical transformers (Transformer A and Transformer B) with cross-coupling between CR-VCOs is used to reduce supply voltage through positive feedback. The primary coil $L_{pa}$ ($L_{pb}$) serves as the inductor in the LC-tank and the secondary coils i.e., $L_{sa1}$ and $L_{sa2}$ ($L_{sb1}$ and $L_{sb2}$) senses the output nodes of the other identical CR-VCO and provide the injection current through cross-coupling. This cross-coupling action ensures that the oscillator outputs maintain quadrature phases. In addition, the series resistance of the inductors $L_{sa1}$ and $L_{sa2}$ suppresses the amplitude imbalance due to the difference in transconductance ($g_m$) of NMOS and PMOS transistors, hence no degenerate resistors are used.

2. Buffers: The outputs from the main block are fed into the buffer circuit because the core of QVCO has no driving ability. This can also isolate the parasitic resistors and capacitors from the LC-tank. These buffers consists of a ac-couple capacitor and an self-bias inverter. Therefore, no additional bias voltage is needed. PMOS and NMOS sizing of these buffers plays a crucial role in obtaining the proper QVCO output i.e., sinusoidal voltages. In our design, we design the buffer to have strong pull-up in order to accommodate the parasitic effects that our QVCO needs to drive.

3. Tuning arrays: Tuning arrays increase the frequency range of the QVCO by varying the center frequency. Tuning array circuit consists of a 2-bit differential binary-weighted swithed-capacitor array (SCAs) as shown
Figure 5: Topology of TC-QVCO with output buffers

In Figure 5, where $L_{eq}$ is the equivalent inductance seen between $V_o1$ and $V_o2$ (The coupling between primary and secondary coils should be considered). The equivalent capacitance to determine center frequency is $C_{Var}$ parallel to $C_{teq}$ where $C_{teq}$ is the equivalent capacitance of the tuning array. The center frequency is varied by varying $C_{teq}$ and voltage controlled tuning is achieved through $C_{Var}$. With this approach, the frequency range of operation of the VCO is increased. Different $C_{teq}$ is obtained by using NMOS switch with a control bit. Let us consider the Array ’0’ circuit: two capacitors are separated to each other if switch0 is low since the NMOS is OFF else the two capacitors will be in series and accordingly the equivalent capacitance can be $0$ or $C/2$. With our circuit, we can have a total of 3 values for $C_{teq}$ because of two arrays and the $C_{teq}$ can be $0$, $0.5C$ and $1.0C$ when the array control input is ‘00’, ‘01’ (‘10’) and ‘11’ respectively. We cascade two inverters for each array as shown in the tuning array circuit block to reduce the transient switching times. Also, two large resistors are utilized to isolate the noise from control bits.

To gain more insight on the operation of our QVCO, small signal analysis is performed and the small signal equivalent half circuit is shown in Figure 6 because of our QVCO symmetry. This half circuit corresponds to the left half of our QVCO and is obtained from the analysis based on [25]. In this circuit, $R$ and $C$ are equivalent resistance and capacitance of the LC tank parallel to the $\frac{k^2}{1-k^2}L_p$. The rest $(1-k^2)L_p$ inductance is the self inductance that is not part of the coupling and hence it is connected in series to the equivalent capacitance as shown in the Figure 6a. Also, the rest of the half circuit can be modeled with an ideal transformer and hence can be replaced by controlled sources as shown in Figure 6b.

To simplify our analysis, we assume that the transconductances $g_m$ of all transistors to be the same. This assumption is valid since we aim to size the transistors to behave the same way i.e, same transconductances in order to obtain identical outputs in terms of magnitude with desired phase differences between the outputs. With this assumption, the current
through the secondary coils i.e., $I_{SA}$ and $I_{SB}$ are same and is assumed to be $I_S$. From Figure 6, we can obtain output voltages using Kirchoff’s voltage and current laws. The non-coupling primary inductance $(1 - k^2) * L_p$ is negligible and the equation 2 is obtained using Kirchoff’s voltage law.

$$V_{o2} - V_{o1} + \left[ \left( V_{o1} - \frac{V_{o4}}{kN} \right) g_m + \left( \frac{I_S}{kN} + \frac{I_S}{kN} \right) \right] Z_{Tank} = 0$$  \hspace{2cm} (2)

where $Z_{Tank}$ is given by the equation 3 since it is a parallel RLC tank circuit.

$$\frac{1}{Z_{Tank}} = \frac{1}{R} + \frac{1}{j\omega k^2 L_p} + j\omega C$$  \hspace{2cm} (3)

The resonant frequency and the quality factor of this tank circuit are given in equations 4 and 5 respectively.

$$\omega_0 = \frac{1}{\sqrt{k^2 L_p C}}$$ \hspace{2cm} (4)

$$Q = \omega_0 R C = \frac{R}{\omega_0 k^2 L_p}$$ \hspace{2cm} (5)

The current $I_S$ can also be expressed using the transistor transconductance as shown in equation 6.

$$I_S = \left( V_{o3} - \frac{V_{o1}}{kN} \right) g_m$$ \hspace{2cm} (6)
QVCO produces four quadrature phase oscillations and each CR-VCO in Figure 5 produces out-of-phase outputs. Therefore, we can define the relation between the output voltages as shown in equation (7).

\[ V_{o1} = -V_{o2} = jV_{o3} = -jV_{o4} \] (7)

From equations (2), (3), (6) and (7), we obtain equations (8) and (9) by equating the real and imaginary parts. The minimum transconductance \( g_m \) required for proper oscillation of the QVCO is given in equation (8). By solving equation (9) and replacing \( g_m \) from equation (8), we obtain the oscillation frequency of the QVCO and is given in the equation (10).

\[ g_m = \frac{2}{R} \frac{(kN)^2}{(kN)^2 - 2} \] (8)

\[ \frac{3g_m}{kN} + \frac{2}{\omega k^2 L_p} - 2\omega C = 0 \] (9)

\[ \omega = \omega_0 \left[ \frac{3kN}{2Q \left( (kN)^2 - 2 \right)} + \left( \frac{3kN}{2Q \left( (kN)^2 - 2 \right)} \right)^2 + 1 \right] \] (10)

4 TSV Inductor Design

In this work, we assume a three-tier 3D process [20] for the rest of the paper. The parameters for the TSV inductor of this process is shown in Table 1. We use a total of 9 metal layers and the thickness of the metal interconnect layer is 30 µm including the inter-adhesive layer. The TSV inductor is designed such that its cross-section is close to square (TSV spacing equals TSV height) to achieve higher quality factor. The mentioned assumptions are for demonstration purposes only and the TSV inductor design is not limited to these assumptions.

| Parameter                  | Value   |
|----------------------------|---------|
| Substrate tier height      | 60 µm   |
| Substrate conductivity (σ) | 10 S/m  |
| TSV diameter               | 20 µm   |
| Liner thickness            | 0.5 µm  |
| Minimum TSV pitch          | 5 µm    |
| Inter-adhesive layer thickness | 2 µm |
| Total oxide layer between tiers | 30 µm |
| Top metal layer (M9) thickness | 1 µm |
| Top metal layer (M9) width | 24 µm   |
| M9-M8 via length           | 5 µm    |
| Metal layer (M8) thickness | 7 µm    |
| Metal layer (M8) width     | 24 µm   |
| M8-M7 via length           | 3 µm    |
| Metal layer (M7) thickness | 2 µm    |
| Metal layer (M7) width     | 24 µm   |

We implement TSV based 6-port transformer for our QVCO design in two ways based on the TSV inductor models discussed in [13]: 1. Toroidal TSV transformer and, 2. Vertical spiral TSV transformer. For these transformers, we need a total of three inductors i.e., one primary and two secondary coils. For our QVCO design shown in Figure 5, we implement two of these transformers that are identical. The TSV transformer structures are detailed in the rest of this section and the specifications with their characteristics are given in Section 5.1.

4.1 Toroidal TSV transformer

On-chip toroidal TSV transformer structure is shown in Figure 4. TSVs are connected to form a closed loop by using top metal layer and hence the inductor series resistance will be minimum. From the figure, we can see that there are total
of three inductors coupled to each other where the primary inductor is named as \( \text{ind}_1 \) and the other two secondary coils are named as \( \text{ind}_2 \) and \( \text{ind}_3 \). For the QVCO design, the primary coil requires higher inductance than the secondary coils. The secondary coils are tightly coupled to the primary coil with the structure shown in Figure 7 where adjacent turns corresponds to different coils. Also, the magnetic coupling between the secondary coils are minimum since they are not tightly coupled.

![Diagram of toroidal TSV transformer](image)

(a) cross-view

(b) side-view

Figure 7: Structure of toroidal TSV transformer

### 4.2 Vertical spiral TSV transformer

Vertical spiral TSV transformer structure is shown in Figure 8. TSVs are connected to form a closed loop by using top three metal layers and all the TSVs of the same inductor are aligned in a straight line. From the figure, we can see that there are total of three inductors coupled to each other where the primary inductor is named as \( \text{Main} \) and the other two secondary coils are named as \( \text{Sec}_1 \) and \( \text{Sec}_2 \). The secondary coils are placed close to the primary coil and the secondary coils are are on the opposite sides to the primary coil as shown in Figure 8. With this approach, magnetic coupling between primary coil to second coils is the possible maximum and between secondary coils is low.
5 Experimental Results

The center frequency of the QVCO is assumed to be 2.5 $GHz$. The capacitance $C_{var}$ ranges from 2.1 $pF$ to 6.3 $pF$ with the control voltage $V_c$ changes from 0.1V to 0.7V. Therefore, the primary coil of the transformer should be designed to achieve 3 $nH$ based on Equation 4, where the $C_{eq}$ is at 4.6 $pF$. To suppress the amplitude imbalance and maintain quadrature phases, secondary coils of the transformer is designed to achieve 0.4 $nH$ and $k$ is around 0.52. We implemented the transformer models in commercial full-wave simulation framework and followed the methodology discussed in [14] to design these inductors based on the specifications obtained. These inductors are embedded in QVCO design with their s-parameter model with the frequency range from 0 to 20 $GHz$ extracted from full-wave
simulator and we use 65 nm TSMC technology library to realize QVCO. For clarity, we show the design specifications of the QVCO in Table 2. These design specifications are obtained from industry and are slightly modified.

| Parameter               | Value or Range          |
|-------------------------|-------------------------|
| Supply voltage $V_{DD}$ | 0.7 V                   |
| Center frequency $f_c$  | 2.5 GHz                 |
| Control voltage $V_c$   | 0.1 V to 0.7 V          |
| Primary inductance $L_p$| 3 nH                    |
| Secondary inductance $L_s$| 0.4 nH                |
| Capacitance range $C_{var}$| 2.1 pF to 6.3 pF     |
| Rail-to-rail voltage $V_{out}-p$ | 350 mV             |
| Max voltage variation $\Delta V_{out}$ | 25 mV              |

5.1 TSV inductor design

Design parameters and the performance metrics for toroidal TSV transformer and vertical spiral TSV transformer to implement our QVCO are given in Table 3. $L_p$ and $L_s$ represents the primary coil and secondary coils inductance respectively. $R_{pdc}$ and $R_{sdc}$ represents the series DC resistance of primary coil and secondary coils respectively. $R_{pac}$ and $R_{sac}$ represents the series AC resistance of primary coil and secondary coils at frequency 2.5 GHz respectively. $k_{ps}$ and $k_{ss}$ represents the mutual coupling factor between primary coil-secondary coil and between secondary coils respectively. $Area$ represents the total metal resource consumption of the transformer. From the table, we can see that the DC resistance of the primary coil is higher for the vertical spiral transformer compared with the toroidal transformer since thin $M_7$ is used. However, with vertical spiral transformer, the metal resource consumption reduced by up to 18% compared with the Toroidal transformer. Also, although not shown, we also implemented conventional 2D spiral transformer to compare our TSV transformers and the metal resource consumption reduced by upto 3.2x and 3.9x times by replacing conventional 2D spiral transformer with the toroidal TSV transformer and vertical spiral TSV transformer respectively for the same inductance. Although not shown in the table, the parasitic capacitance will be higher for vertical spiral TSV based-transformer compared with the toroidal TSV based-transformer due to tight metal interconnects as shown in Figures 7 and 8.

| Parameter | Toroidal | Vertical spiral |
|-----------|----------|----------------|
| $L_p$ (nH) | 2.99     | 2.97           |
| $R_{pdc}$ (mΩ) | 300      | 488            |
| $R_{pac}$ (Ω) | 1.4      | 3.03           |
| $L_s$ (nH) | 0.38     | 0.36           |
| $R_{sdc}$ (mΩ) | 64       | 66             |
| $R_{sac}$ (Ω) | 0.35     | 0.38           |
| $k_{ps}$ | 0.52     | 0.54           |
| $k_{ss}$ | 0.15     | 0.29           |
| $Area$ (mm²) | 0.17     | 0.14           |

5.2 Performance of proposed QVCOs

We implemented two QVCO designs by using two different TSV transformers discussed in Section 5.1, i.e., Toroidal TSV based- and, Vertical spiral TSV based- transformers. The performance metrics of the proposed QVCOs are shown in Table 4. The freq range that the proposed VCOs can tune is around 1.4 GHz and the differences in this frequency range between toroidal TSV transformer based QVCO and vertical spiral TSV transformer based QVCO is due to their difference in parasitic capacitances. Since the parasitic capacitance will be higher for vertical spiral TSV based-transformer compared with the toroidal TSV based-transformer due to tight metal interconnects, the frequency range is reduced due to the similar transformer inductances. The phase noise $\phi_{phase}$ in the table is at 1 MHz frequency. From the table, we can see that the power consumption of the proposed QVCOs are different. This is because of the difference in series resistances of the transformers. However, to sustain oscillation, we need to ensure that the series resistance of primary inductor $R_L$ should be greater than $\frac{2}{g_m}$. The start-up time of the proposed QVCOs i.e., the time
required to reach steady state oscillations is around 50\text{ns}. The common benchmark for LC oscillators is Figure-of-Merit (FoM) [27] and is given by the equation (11) and the corresponding FoM values at 1\text{MHz} are given in the Table 4.

\[
\text{FoM} = -20 \log \left( \frac{\omega_0}{\Delta \omega} \right) + 10 \log(P_{mW}) + \phi_{noise}(\Delta \omega)
\]  

(11)

Table 4: QVCO Performance metrics

| Metric                  | Toroidal based- | Vertical spiral based- |
|-------------------------|-----------------|------------------------|
| Freq Range (GHz)        | 2 \sim 3.4      | 1.83 \sim 3.11         |
| \(\phi_{noise}\) (dBc/Hz) | -114            | -111.2                 |
| \(\Delta V_{out}\) (mV) | 19              | 20                     |
| Start-up time (\text{ns}) | 50              | 50                     |
| Power (mV)              | 1.5             | 1.7                    |
| FoM (dB)                | -180            | -177                   |

The phase noise \(\phi_{noise}\) vs. offset frequency \(f\) is shown in Figure 9. From the figure, we can see that the \(\phi_{noise}\) is almost identical for both the QVCO designs since they are different in terms of the transformer performance. \(\phi_{noise}\) is higher for vertical spiral TSV transformer based- QVCO compared with the toroidal TSV transformer due to their differences in quality factors as shown in Table 3 [28]. For example, at 1\text{MHz} frequency offset, the toroidal TSV based-QVCO has the \(\phi_{noise}\) of -114 \text{dBc/Hz}, almost 3dB lower compared with the vertical TSV based-QVCO.

The steady state quadrature output voltages of vertical spiral transformer based-QVCO is shown in Figure 10. The frequency of these output voltages are 2.5 GHz and the rail to rail voltage is around 350 mV for a 0.7 V supply. From the figure, we can see that the output voltages does not have same rail to rail voltage and this difference is due to the variations in transconductances of NMOS and PMOS transistors and in drain-source voltage of the transistors. However, the maximum voltage difference between the outputs is less than 20 mV and is well with in the limits of the design specifications.

Figure 9: Phase noise v.s. Frequency of proposed QVCOs

5.3 Comparison of proposed QVCO designs with other works

Table 5 summarizes the comparison of proposed QVCOs with other current QVCO designs. From the table, we can see that the proposed QVCO performance is on par with the other current QVCO designs. In terms of power consumption, proposed QVCOs are superior to other works except with the QVCO design in [31] but the die area and the frequency range is higher for the proposed design. In terms of die area, proposed QVCO design has the minimum die area and this is achieved through the proposed TSV transformer structure utilization to design QVCOs. In addition, proposed QVCO designs demonstrate relatively high phase noise. Although [29, 30, 31] used 3D solenoid inductor to implement QVCOs,
they use a single conventional TSV inductor based QVCOs instead of taking advantage of coupling mechanisms of the transformer designs.

6 Conclusion

In this article, we have demonstrated the effectiveness of TSV transformer structures in the QVCO designs in 3D ICs. We also proposed a novel QVCO that can be used to provide higher frequency range. Experimental results show by replacing conventional spiral transformers with TSV transformers, up to 3.9x reduction in metal resource consumption. The proposed QVCOs achieves a phase noise of $-114 \, \text{dBc/Hz}$ at $1 \, \text{MHz}$ and $-111.2 \, \text{dBc/Hz}$ at the carrier of $2.5 \, \text{GHz}$ for toroidal TSV transformed based-QVCO and vertical spiral transformer based-QVCO respectively. The power consumption is only 1.5 mW and 1.7 mW for toroidal TSV transformed based-QVCO and vertical spiral transformer based-QVCO respectively, under the supply voltage of 0.7 V. We have also discussed the comparison of our works with the current QVCO designs.

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