Simulations of resonant tunnelling through InAs/AlSb heterostructures for ULTRARAM™ memory

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Abstract
ULTRARAM™ is a III–V semiconductor memory technology which allows non-volatile logic switching at ultra-low energy (per unit area). This is achieved by exploiting triple-barrier resonant tunnelling (TBRT) through a series of InAs/AlSb heterojunctions specifically engineered for this purpose. Electrons tunnelling through the barriers at low bias are trapped in a floating gate, in which the presence or absence of charge defines the memory logic. Here, we report detailed non-equilibrium Green’s functions simulations of the InAs/AlSb TBRT heterostructure, which is the principal source of ULTRARAM™’s extraordinary performance benefits. The effects of variations to the heterostructure layer thickness are investigated for performance optimization, and for assessing growth and process tolerances for commercial implementation on 12″ Si wafers. Trade-offs between power, speed, logic disturbance and data retention time are identified. Importantly, most one monolayer alterations to the tunnelling region show the required characteristics for ULTRARAM™ memory operation, thus some tolerance in any future commercial fabrication process is identified.

Keywords: compound semiconductor, resonant tunnelling, non-volatile memory (NVM), non-volatile RAM (NVRAM), InAs/AlSb

1. Introduction
The development of a universal technology that replaces current memory types has long been a major objective in the semiconductor industry. A ‘universal memory’ should possess the speed of static random access memory, the non-volatility, low-cost and high-density of flash and endurance of dynamic random access memory. This necessitates a robust logic state which can nevertheless be easily changed with a small amount of energy. As the nature of these requirements appears antithetical, the widely accepted view is that universal memory is unfeasible [1] or almost impossible [2]. ULTRARAM™ is an emerging, floating-gate (FG) memory technology that utilises the unique band offsets of the 6.1 Å semiconductor family (InAs, AlSb and GaSb) [3]. In particular, the non-volatility of the memory is derived from the extraordinarily large conduction band (CB) offset of the InAs/AlSb heterojunction (2.1 eV), which plays a similar role to the semiconductor-oxide barriers used in flash memories [4]. However, in ULTRARAM™, multiple ultrathin InAs/AlSb layers are used to form a triple-barrier resonant tunnelling (TBRT) structure between the channel and the FG [5]. This reconciles the contradictory requirements of a universal memory, as the tunnelling structure provides a 2.1 eV energy barrier to retain memory logic, but allows resonant tunnelling
of electrons (i.e. transparent barriers) at program/erase (P/E) voltages less than 2.5 V, around 10 times lower than flash [6].

The remarkable performance characteristics of ULTRARAM™ are predicted by detailed simulations of quantum transport [7], and encouraging results have been demonstrated in single devices and 2 × 2 arrays at room temperature on GaAs substrates at 20 µm gate lengths [8], with implementation on Si substrates on-going [9]. Moreover, recent experimental results validate our previous simulation work, including the proposed half-voltage architecture for random access memory (RAM) applications [10]. Our previous theoretical investigations were for a specific layer thickness configuration of the triple-barrier InAs/AlSb tunnelling junction [7]. In practice, growth of these layers with exact monolayer (ML) precision is not straightforward. Indeed, thicknesses could be offset across the entire growth due to imprecise calibration, or vary across the wafer. This is of particular concern for the commercial development of ULTRARAM™, as it is vital that the InAs/AlSb heterostructures currently grown on 3° Si [9] be transferred onto 12° Si substrates in order to be cost-competitive. In this work, we present non-equilibrium Green’s function (NEGF) simulations of the ULTRARAM™ resonant tunnelling region, where layer thicknesses are varied to investigate the effect on the performance of the memory. Choices of layer alterations presented here are ±1 ML (i.e. one lattice constant, 6 Å). It is possible for alterations of 0.5 ML to occur; however, these have a smaller impact on the memory performance. Furthermore, the thinnest layer of the tunnelling region has a target thickness of just 2 MLs (12 Å), so an increase of 2 MLs would represent a doubling in thickness, whilst a decrease of 2 MLs removes the layer entirely.

2. Memory concept

Logic switching of the memory state in ULTRARAM™ is achieved via TBRT through the InAs/AlSb heterostructure. Under an applied bias of <2.5 V, electrons tunnel from the InAs channel, through the TBRT region and into the FG to produce logic 0 (P cycle). This is shown schematically in figure 1. Conversely, a reverse bias allows electrons to tunnel from the FG to the channel in the opposite direction. This depletes the FG, returning the device to logic 1 (E cycle). Electrons which tunnel into the FG are trapped there indefinitely by the 2.1 eV barriers become partially transparent and allow electrons to move across the tunnelling junction. The asymmetric double-well structure gives two resonant tunnelling energies. More importantly, this configuration increases the charge-blocking capability of the TBRT region compared to a conventional double-barrier structure, which is crucial for non-volatile memories [7, 15].

![Figure 1. Device schematic for ULTRARAM™ memory as fabricated in [8–10], with Al2O3 gate dielectric to prevent hole leakage currents (not to scale). Material layers are presented alongside with the TBRT region of particular interest to this work marked by a yellow arrow. Thicknesses of the TBRT layers are given in table 1.](image)

| Material | B1 | QW1 | B2 | QW2 | B3 |
|----------|----|-----|----|-----|----|
| InAs     | 18 | 30  | 12 | 24  | 18 |
| AlSb     | 18 | 24  | 12 | 24  | 18 |
| +1 ML QW1, QW2 | 18 | 36  | 12 | 30  | 18 |
| −1 ML QW1, QW2 | 18 | 24  | 12 | 18  | 18 |
| +1 ML B1, B2, B3 | 24 | 30  | 18 | 24  | 24 |
| −1 ML B1, B2, B3 | 12 | 30  | 6  | 24  | 12 |
| +1 ML B1, B3 | 24 | 30  | 12 | 24  | 24 |
| −1 ML B1, B3 | 12 | 30  | 12 | 24  | 12 |
| +1 ML B2 | 18 | 30  | 18 | 24  | 18 |
| −1 ML B2 | 18 | 30  | 6  | 24  | 18 |

Channel and FG thicknesses are fixed to 120 Å. InAs and AlSb material parameters can be found in the program database for nextnano. MSB and are fixed to experimental values [7, 13, 14].
3. Non-volatility

The ability of a memory to retain its logic state is important for memory performance in both RAM and mass storage applications [16]. It has been predicted that the intrinsic (300 K) storage time of electrons in the InAs/AlSb system exceeds the age of the universe [17]. However, this prediction is based on thermal excitation of electrons over the barrier potential. To investigate the non-volatility of ULTRARAM™ we must consider the effects of the TBRT structure on the transparency of the barriers. This is accomplished using NEGF simulations of the TBRT region at 300 K under zero applied bias. The simulation results detailed here are modelled using nextnano multi-scattering Büttiker (MSB) software, the details of which can be found in [7, 13]. Figure 2(a) shows the calculated CB edge (white) for the target TBRT structure, where the barriers and wells are labelled in accordance with table 1. The colour scale of the density of states (DOS) demonstrates the confinement energies of the QWs (QW1 and QW2). The transmission function, T, i.e. the likelihood of electrons leaving or entering the FG, is shown by the red line (log-scale). It is extremely small in the energy region below the barrier height; however, it possesses three distinct points of interest. The first is a transmission peak corresponding to the resonant state of the QW1 ground state, the second is the transmission peak for the QW2 ground state, and, finally, the largest transmission peak is for the second confined state of QW1. Note that for the target TBRT structure in figure 2, QW2 is too narrow to have a second confined QW state. The largest transmission peak of \(T = 0.04\) resides at an energy (\(E\)) of around 1.8 eV, which corresponds to an electron storage time of about \(10^{10}\) years at room temperature [17]. The lower energy (QW1 and QW2) transmission peaks are at \(T \sim 10^{-5}\), \(E = 0.29\) eV and at \(T \sim 10^{-5}\), \(E = 0.4\) eV, respectively. Although the peaks reside at a much lower energy, corresponding to millisecond storage times at room temperature for localization energies of that size [17], the probability of transmission is very low, making it unlikely that these peaks impact on the retention capability of the memory. Indeed, fabricated devices show stable memory retention exceeding 24 h at 300 K with little or no state decay [8, 10].

Monolayer alterations to the target structure are assessed by repeating the NEGF calculations under the same conditions for each of the alterations listed in table 1. The results for the transmission function are presented in figure 2(b). Alterations to the QW thicknesses shift the ground states of the QWs. A 1 ML reduction in QW thickness shifts the start of the QW1 transmission peak to a higher energy (solid red line, figure 2(b)) by around 100 meV, with similar transmission, such that it is coincident with the transmission peak associated with QW2 in the target structure. This is not unexpected as the QW width in both cases is the same. In the same way, the transmission peak associated with QW2 shifts to higher energy. The result would be an improvement in retention compared to the target structure. The converse argument can be made for increasing QW thicknesses by 1 ML (dotted red line, figure 2(b)), which would decrease retention. The transmission peak associated with QW2 becomes coincident with that of QW1 in the target structure, in both cases corresponding to a QW thickness of 30 Å, and the peak associated with QW1 moves to lower energy. The 1 ML increase also shifts the transmission peak associated with the second confined state of QW1 to lower energy, and introduces a new peak associated with the second confinement energy of QW2 at similar energy and transmission to the second confined state of QW1 in the target structure. Overall, with barriers at the target widths, the energies and magnitudes of the transmission peaks are closely associated with given QW widths, and somewhat independent of each other. If QW thicknesses are equal, the increased overlap interaction between the wells increases transmission by an order of magnitude, as shown in figure 2(b) (black dashed line).

Reducing the thickness of the barriers increases the transmission probabilities. A 1 ML thickness reduction of all barriers increases the transmission probability at the QW1 ground
state energy by about three orders of magnitude to \( T = 0.02 \), with a consequential detrimental impact on the non-volatility of the memory (solid blue line, figure 2(b)). Reducing the thickness of the central barrier (B2) results in greater separation between QW1 and QW2 peak energies as the energy splitting effect from the interaction of the two QW ground states due to the Pauli exclusion principle is increased [18]. This pushes the QW1 energy lower which could negatively impact retention, however the transmission remains relatively small (solid pink line, figure 2(b)). Unsurprisingly, increasing the barrier thicknesses has the opposite effect, and will result in improved retention capability of ULTRARAM™ if required (dotted blue, green and pink lines, figure 2(b)), with successive 1 ML increases in barrier thickness each delivering a reduction in QW peak transmission of about an order of magnitude. There will be a trade-off between the resonant-tunnelling current characteristics and the charge-blocking properties, so we cannot yet conclude that thickening the barriers is a superior design choice for the technology until the full extent of ULTRARAM™ retention properties have been investigated experimentally. Crucially, we find that the retention of the memory should not be detrimentally impacted by most 1 ML alterations, with the main retention concerns being the cases where thickness is reduced for all barriers. Fortunately, the latter scenario is experimentally relatively unlikely, as it represents a large change in percentage error in layer thickness for layers grown in close proximity to each other. This is a promising result regarding the commercial implementation of ULTRARAM™, but demonstrates that process and growth tolerances are of paramount importance.

4. Tunnelling current

The TBRT mechanism used to program (i.e. add electrons to the FG) for ULTRARAM™ memory devices is demonstrated in figure 3, where all calculations are again carried out using the nextnano MSB software package [13]. Resonant tunnelling occurs under the condition that the energy of electrons in the channel align with the available energies of the TBRT structure (i.e. the QW1 or QW2 ground state energies). This is measured as a current density through the barriers, as shown in figure 3(d), containing three distinct peaks. The DOS plots under applied bias reveal the resonant conditions of the large tunnelling currents (figures 3(a)–(c)) as labelled on the current density plot. The low-voltage peak (figure 3(a)) occurs when the electron energies from the contact align with the QW ground states, producing a broad peak. However, if we turn our attention to the device construction shown in figure 1, the channel is such that the contact is spatially separated from the gate stack, therefore resonant tunnelling directly from the contact (i.e. ballistic tunnelling that bypasses the InAs CB entirely) is not possible. We conclude that this is not part of the ULTRARAM™ tunnelling mechanism and is an artefact of the simulation construction. Indeed, experimental studies support this assertion [8–10, 19]. The peaks occurring at higher voltages are the expected resonant tunnelling peaks (figures 3(b) and (c)). As the TBRT region is under a large electric field, the sloping of the CB forms a triangular quantum potential well at the channel-B1 interface such that resonant tunnelling through the structure is a 2D-2D process with a concentrated DOS. Here, electrons occupy the triangular quasi-bound state due to inelastic scattering. Without the inclusion of inelastic scattering the device operates in an entirely different way whereby the current-density characteristic is entirely determined by the properties of the lead (contact), rather than by details of the CB in the device [20]. Two large tunnelling current density peaks emerge corresponding to alignment with the QW1 and QW2 ground states at \( V_{\text{TBRT}} = -1.06 \) V and \( V_{\text{TBRT}} = -1.28 \) V, respectively. Tunnelling through the QW2 state can occur despite the QW1 state residing at higher energy due to the wave-function overlap between the QWs, which can be seen in the DOS plots of figure 3(c).

When interpreting a resonant tunnelling current-density plot for the purposes of ULTRARAM™ memory there are important properties to consider. First, there is the magnitude of the current density peaks, which is directly related to the device switching speed [7], where larger current peaks improve performance. Second is the voltage (\( V_{\text{TBRT}} \)) at which the peak occurs; a high voltage will consume more power, whilst a very small voltage is more likely to have logic disturbances under readout biasing. Lastly, is the sharpness of the onset of the peaks; a significant tunnelling current away from the P/E peak voltage will also cause logic disturbances.

Figure 3. Simulations of the target TBRT junction for the memory (300 K) for tunnelling of the program cycle. (a) DOS of states for the ‘leads’ (contacts) under bias corresponding to the contact peak of the current density plot. (b) DOS (colour scale) plot for the tunnelling voltage of QW1 current density peak. (c) DOS (colour scale) plot for the tunnelling voltage of QW2 current density peak. (d) Current density plot of the TBRT region as a function of applied bias. Labelled peaks correspond to the resonant energy alignments of (a)–(c).
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However, a trade-off could be made with the retention cap-

magnitudes, which could degrade the speed of the memory.

Increasing barrier thicknesses reduces the current density by up to two orders of

thicknesses could serve as a valuable method in tuning the

performance. Moreover, this shift outweighs the increase in electric field
caused by thinning the structure. The converse applies when thickening the QWs. The magnitude of the current density
peaks is not significantly affected. Thus, changes to the QW thick-

nesses (figure 4(a)) shift their ground state energies such that

a reduction in thickness increases the required electric field for resonant tunnelling alignments (pink triangles, figure 4(a)).

Moreover, this shift outweighs the increase in electric field caused by thinning the structure. The converse applies when
thickening the QWs. The magnitude of the current density peaks is not significantly affected. Thus, changes to the QW thick-

nesses could serve as a valuable method in tuning the memory for operation at a desired voltage without hindering

performance.

Figure 4(b) presents the results of thickening barrier lay-

ers on the P cycle current density. Increasing barrier thick-

ness reduces the current density up to two orders of magnitude, which could degrade the speed of the memory.

However, a trade-off could be made with the retention cap-

ability such that speed is exchanged for more robust logic

retention as discussed in the previous section. It is worth noting that this speed reduction may be significant, but it is likely that ULTRARAM™ would still outperform current memory technologies as the tunnelling mechanism is intrinsically fast [7, 8, 21]. Increasing the thickness of the middle barrier (red dots, figure 4(b)) greatly reduces the tunnelling current from QW2 (compared to QW1) due to the reduction in wave-function overlap between the QWs, with the ground state of QW1 above the energy QW2 (similar to figure 3(c)).

Logic disturbances at low voltages within the architecture can be evaluated from the region below the peak, depicted by the orange shading in figure 4(b), where we ignore tunnelling from the contact for reasons previously discussed (labelled ‘off’). Increasing barrier thickness reduces the current density in the off region which could be used to reduce logic disturbance. However, it should be noted here that testing on fabricated devices retained robust logic states after 10^5 disturbance cycles [8, 10].

Reducing the barrier thicknesses increases the current den-

sities, as shown in figure 4(c). However, the maximum increase from these alterations is just over one order of magnitude, so switching speed benefits must be carefully weighed against other requirements of the memory. Decreasing the thickness of the outer barriers, B1 and B3, slightly increases the current-density (figure 4(c), green triangles), but broadens the peaks and produces a more gradual ramp to peak current (with omitted contact tunnelling i.e. the in the off region). This could negatively impact logic disturbance, both during readout and for the unique half-voltage RAM architecture [7, 10], as well as retention ability. Reducing the thickness of the middle bar-

rier causes energy splitting of the two QW ground states [18], which results in the QW1 peak moving to a lower voltage requirement and the QW2 peak moving to a higher voltage (figure 4(c), red dots). There are no obvious disadvantages to this configuration, and the energy shift in QW1 could be used for lower voltage memory operation using a single peak for the resonant-tunnelling current density. Reducing all barrier thicknesses results in a much broader current density relation, where it is likely that any gains in switching speed are outweighed by the degradation of other memory performance aspects. Most alterations possess desirable P cycle tunnelling characteristics for ULTRARAM™ operation, which is positive for the purposes of production wafer tolerances. The performance trade-offs in the design have been identified, however, decisions on this should be informed after a more extensive experimental investigation of the target design.

The simulations are repeated with a reversed tunnelling bias (V_{TBRT}) to investigate the erase cycle of the memory (remov-
electrons from the FG). The current-density peaks which move electrons out of the FG occur at energy alignments with the QW1 and QW2 ground states in a similar fashion to the P cycle. This is demonstrated in figures 5(a) and (b), where the QW DOS alignments in the target structure correspond to the peaks as labelled in the current density plot (figure 5(c), black squares). Increasing the barrier thicknesses reduces the magnitude of the current density peaks (figure 5(c)). Increasing the thickness of all the barriers or the outer barriers (figure 5(c) green and blue triangles, respectively) reduces

Figure 4. Nextnano MSB NEGF simulations (300 K) of TBRT current density for the program cycle for each of the alterations listed in table 1. Results are described in detail in the text. (a) 1 ML alterations to the QWs. (b) Increased barrier thicknesses. (c) Decreased barrier thicknesses.
Figure 5. Nextnano MSB NEGF simulations (300 K) for the erase cycle. Results are described in detail in the text. (a) DOS for the QW1 peak condition with FG-QW1 energy alignment for resonant tunnelling for the target structure. (b) DOS for the QW1 peak condition with FG-QW1 energy alignment for resonant tunnelling for the target structure. (c) TBRT current density for increased barrier thicknesses compared with the target structure, where peak labels correspond to the alignments in (a) and (b). (d) As in (c), but for decreased barrier thicknesses.

the contrast between peak current and off-current (orange shading), which could increase the cell logic disturbance rate. However, increased thickness of the middle barrier, B2, (red dots) reduces peak current magnitude, but improves peak-off current ratio which would reduce logic disturbance of the memory in a RAM array [7]. Reducing barrier thicknesses increases the tunnelling current at the peaks, as shown in figure 5(d). Reducing the outer barrier thickness makes little difference to the current-density relation, but shifts the peak current magnitude upwards by two orders (figure 5(d), green triangles). For the E cycle, the energy splitting from reducing the middle barrier thickness (figure 5(d), red dots) is less prominent, as biasing the structure in this direction moves the QW ground state energies further apart, thus reducing the interaction between them [18]. Moreover, reducing the thickness of the middle barrier (B2) gains an order of magnitude in QW1 peak current density and shifts it to a slightly lower voltage, whilst retaining similar off-currents as the target structure. Thus, the choice of reducing the middle barrier should be an improvement to the erase cycle tunnelling. However, these benefits should be carefully weighed against a potentially reduced retention capability and consequences of split P cycle tunnelling peaks, as previously discussed.

5. Conclusions

The InAs/AlSb TBRT region which forms the basis of the ULTRARAM™ memory concept has been investigated in detail using the nextnano.MSB software package (NEGF with Büttiker probe scattering) to determine memory performance characteristics. Monolayer alterations are made to the tunneling structure with the aim of realizing the optimum choice of layer structure whilst considering the growth tolerances required of a commercially-produced wafer. Transmission function calculations indicate that most monolayer alterations have a minimal effect on the retention capabilities. Thickening the barriers reduces low-energy transmission, improving retention, whilst the thinnest barrier configuration investigated allows 0.02 transmission at <300 meV, which could result in significant data (electron) losses. InAs QW widths can be engineered to alter the operation voltage for a specific purpose by shifting the ground state energies with little effect on the overall current density. Trade-offs in current-density and retention are realized by comparison of zero-bias transmission with P and E cycle current density simulations. A higher current density will allow for high-speed operation, but retention may suffer as a result. As the upper limit of ULTRARAM™’s speed and retention capabilities are still unknown (although early works show promising results [8–10]), it is not possible to conclude which trade-off is more desirable for a non-volatile RAM. However, a promising candidate from this work is the reduction in the middle barrier thickness, where the current density is increased with little change to the zero-bias transmission program and function shifted to a lower voltage due to the QW1-QW2 ground state energy-splitting interaction. Crucially, monolayer changes to the TBRT region retain the unique physical phenomena which ULTRARAM™ exploits for its superior performance metrics [7]. As such, transfer of the technology from 3′′′Si [9] to commercial 12″Si is a real possibility if growth tolerances can be kept within ±1 ML (one lattice constant).

Data availability

The data in the figures of this manuscript are openly available from Lancaster University data archive in [22].

The data that support the findings of this study are openly available at the following URL/DOI: https://doi.org/10.17635/lancaster/researchdata/467.

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