Fast Monte Carlo Estimation of Timing Yield: Importance Sampling with Stochastic Logical Effort (ISLE)

Alp Arslan Bayrakci  Alper Demir  Serdar Tasiran
Center for Advanced Design Technologies  College of Engineering  Koc University, Istanbul, Turkey

November 19, 2007

Abstract—In the nano era in integrated circuit fabrication technologies, the performance variability due to statistical process and circuit parameter variations is becoming more and more significant. Considerable effort has been expended in the EDA community during the past several years in trying to cope with the so-called statistical timing problem. Most of this effort has been aimed at generalizing the static timing analyzers to the statistical case. In this paper, we take a pragmatic approach in pursuit of making the Monte Carlo method for timing yield estimation practically feasible. The Monte Carlo method is widely used as a golden reference in assessing the accuracy of other timing yield estimation techniques. However, it is generally believed that it cannot be used in practice for estimating timing yield as it requires too many costly full circuit simulations for acceptable accuracy. In this paper, we present a novel approach to constructing an improved Monte Carlo estimator for timing yield which provides the same accuracy as the standard Monte Carlo estimator, but at a cost of much fewer full circuit simulations. This improved estimator is based on a novel combination of a variance reduction technique, importance sampling, and a stochastic generalization of the logical effort formalism for cheap but approximate delay estimation. The results we present demonstrate that our improved yield estimator achieves the same accuracy as the standard Monte Carlo estimator at a cost reduction reaching several orders of magnitude.

Keywords—logical effort, statistical variations, timing yield estimation and optimization, statistical timing analysis, Monte Carlo methods, variance reduction techniques, importance sampling.

I. INTRODUCTION

We address the problem of estimating timing yield for a circuit under statistical process parameter variations and environmental fluctuations by proposing a novel and improved Monte Carlo method based on transistor-level circuit simulations. In conventional Monte Carlo yield estimation, a number of samples in the parameter probability space are generated. The overall delay of the circuit for each sample point is determined by performing transistor-level timing simulations. An estimator for timing yield is obtained by considering the fraction of samples for which the timing constraint is satisfied. Because of the computational cost of determining circuit delay for each sample, the number of samples one has to work with is limited. This adversely affects the accuracy of the yield estimator; which has a large error for a small number of samples. This is a weakness of the conventional Monte Carlo method and has prevented it from finding widespread use for practical yield estimation.

The technique we propose aims to improve the accuracy of the yield estimates obtained from a given number of Monte Carlo simulations. Alternatively, our improved Monte Carlo estimator achieves the same accuracy as the standard Monte Carlo estimator, but at a cost of much fewer number of full circuit simulations. This is made possible by using a variance reduction technique called importance sampling that we combine in a novel manner with a stochastic generalization of the logical effort formalism originally proposed by Sutherland et. al [1]. Logical effort is a method for quickly estimating and optimizing the path delays in a circuit. We use the stochastic logical effort formalism to guide the generation and selection of sample points in the parameter probability space in a transistor-level simulation based Monte Carlo method for timing yield estimation.

Our approach is based on the premise that, given the magnitude of process parameter variations and the non-linear dependency of gate and circuit delay on these variations, the only sufficiently reliable and accurate method for determining circuit delay is detailed, transistor-level simulation. We believe that sufficient accuracy in yield estimation can not be obtained even by applying Monte Carlo simulations at a higher level, e.g. at the block level. Yield estimation techniques not based on Monte Carlo simulations operate by propagating probability density functions across the circuit. To make this process feasible, one is forced to use approximate gate delay models and delay propagation methods that may be too inaccurate when process parameter variations are large. We therefore believe that accurate determination of timing yield must have circuit simulation as its basis. We demonstrate in this paper that Monte Carlo simulation in conjunction with a novel variance reduction technique can serve as an accurate yet computationally viable yield estimation method.

In Section II, we provide background information and preliminaries on logical effort and its stochastic generalization, the Monte Carlo method for yield estimation and importance sampling. In Section III, we present our improved Monte Carlo yield estimator featuring significant error reduction through the use of the stochastic logical effort formalism to facilitate importance sampling. We also provide a precise, comparative error analysis for our proposed technique and the standard Monte Carlo estimator. Finally in Section IV, we present experimental results on several examples which demonstrate the efficiency and accuracy of our proposed yield estimator.

II. BACKGROUND

Section II-A provides an overview of the logical effort approach [1]. In Section II-B, we introduce two techniques for using logical effort as a method for approximating circuit delay in the presence of statistical variations. Section II-C reviews the standard Monte Carlo method for evaluating definite integrals, and Section II-D presents the importance sampling technique for variance reduction in Monte Carlo simulations. Finally, Section II-E describes the preliminaries in applying the standard Monte Carlo and importance sampling techniques to timing yield estimation.

A. Logical Effort

The logical effort formalism is a fast and efficient way of determining the delay of a path in a digital circuit. The path delay is simply the sum of the delays of the gates on the path, and the delay of a logic gate \( r \) is approximated as

\[
d_L^r = \tau d
\]

where \( d_L^r \) is the absolute delay of a gate measured in seconds, \( \tau \) is the delay of a parasitic-capacitance-free reference inverter driving another identical inverter, and \( d \) is the delay of the logic gate expressed in units of \( \tau \). The \( \tau \) factor in (1) models the gate delay and is given by

\[
d = (p + gh)
\]

where \( p \) represents the intrinsic (parasitic) delay, \( g \) is the logical effort, and \( h \) is the electrical effort or electrical fan-out. Logical effort \( g \) for a logic gate is defined as the (unitless) ratio of its (per) input capacitance to that of an inverter that delivers the same output current. Thus, logical effort \( g \) is a measure of the complexity of a gate. It depends only on the gate’s topology and is independent of the size and the loading of the gate. Parasitic delay \( p \) expresses the intrinsic delay of the gate due to its own internal parasitic capacitance, and it is largely independent of the sizes of the transistors in the gate. Parasitic delay \( p \), is also expressed in units of \( \tau \). The electrical effort \( h \) is the ratio of the load capacitance of the logic gate to the capacitance of a particular input [1].

B. Stochastic Logical Effort

Equations (1) and (2) provide a way of decomposing the effects of statistical parameter variations on gate delays. In a different context, Sutherland et. al [1] analyzed different semiconductor processes with varying supply voltages, and observed that almost all of the effect of process parameters and supply voltage on gate delay is captured by the reference inverter delay (\( \tau \) in (1)), even when the parameters vary over a large range spanning different fabrication processes. The logical effort \( g \) and the unitless parasitic delay \( p \) of a gate exhibit relatively little variation with process parameters and supply voltage. Exploiting this...
observation in the context of timing yield analysis, in [2] a stochastic logical effort (SLE) model was proposed where the delay of a gate was modeled as

\[ d_{s}^{LE} (X) = \tau (X) (p(X) + g(X) h) \]  

where \( X \) is a vector of random variables, each component of which represents a different statistical circuit or process parameter and \( \tau (X) \) is the reference inverter delay when the parameters are given by \( X \). As is apparent in this equation, in the stochastic logical effort approximation, all process and environmental variations are captured by the statistical variable \( \tau \) while \( g, p \) and therefore \( d \) are assumed to be independent of process parameters. If only inter-die variations are modeled, statistical parameters on the chip at all locations are perfectly correlated. In this case, using the stochastic characterization of \( \tau \) for the same reference inverter for all of the logic gates on the die captures this perfect statistical correlation among gates. We refer to the approximation given in (3) as first-degree stochastic logical effort (abbreviated as SLE.d1).

In this paper, we also investigate a further refinement of this approximation described by the following equation

\[ d_{s}^{LE} (X) = \tau (X) (p(X) + g(X) h) \]  

where the dependency of \( p \) and \( g \) on \( X \) is also modeled. We call this model second-degree stochastic logical effort (SLE.d2). As will become apparent later in the paper, SLE.d2 is more accurate but computationally more expensive.

In both versions of SLE, in order to compute the delay of a path \( \pi \) in a circuit, we simply add the delays of the gates on \( \pi \):

\[ d_{s}^{LE} (X) = \sum_{r=1}^{k} d_{s}^{LE} (X) \]  

Here \( d_{s}^{LE} (X) \) is the delay of the \( r \)-th gate on the path \( \pi \). \( d_{s}^{LE} (X) \) is computed by evaluating (3) for SLE.d1 and (4) for SLE.d2. For this evaluation, a full transistor-level simulation of the whole circuit containing the logic path is not necessary. However, the values of \( \tau (X) \) (for both SLE.d1 and for SLE.d2) and \( p(X) \) and \( g(X) \) (for SLE.d2) at a given \( X \) are needed. For the results we present in this paper, we compute these at a given \( X \) by running transistor-level circuit simulations on small test circuits which contain only the reference inverter (for \( \tau (X) \) or the gate under consideration (for \( p(X) \) and \( g(X) \))) together with a proper driver and load circuitry. We envision that the statistical characterizations (in the form of simple analytical formulas, a look-up table or a response surface model generated by running circuit simulations on appropriate test circuits) for these quantities could become part of the characterizations supplied with a standard-cell library. In this case, no circuit simulations will be needed when evaluating the SLE delay formulas for circuits that are built using gates from such a pre-characterized library.

C. The Monte Carlo Method

Monte Carlo (MC) techniques can be used to estimate the value of a definite, finite-dimensional integral of the form

\[ G = \int_{\Omega} g(X) f(X) dX \]  

where \( \Omega \) is a finite domain and \( f(X) \) is a probability density function (PDF) over \( X \), i.e., \( f(X) \geq 0 \) for all \( X \) and \( \int_{\Omega} f(X) dX = 1 \). MC estimation for the value of \( G \) is accomplished by drawing a set of independent samples \( X_1, X_2, \ldots, X_N \) from \( f(X) \) and by using

\[ G_N = \frac{1}{N} \sum_{i=1}^{N} g(X_i) \]  

The estimator \( G_N \) above is itself a random variable. Its mean is equal to the integral \( G \) that it is trying to estimate, i.e., \( E(G_N) = G \), making it an unbiased estimator. The variance of \( G_N \) is \( \text{Var}(G_N) = \sigma^2 / N \), where \( \sigma^2 \) is the variance of the random variable \( g(X) \) given by

\[ \sigma^2 = \int_{\Omega} g^2(X) f(X) dX - \bar{G}^2 \]  

The standard deviation of \( G_N \) can be used to assess its accuracy in estimating \( G \). If \( N \) is sufficiently large, due to the Central Limit Theorem, \( G_N \) has an approximate standard normal \( N(0,1) \) distribution. Hence,

\[ P(G - 1.96 \frac{\sigma}{\sqrt{N}} \leq G_N \leq G + 1.96 \frac{\sigma}{\sqrt{N}}) = 0.95 \]  

where \( P \) is the probability measure. The equation above means that \( G_N \) will be in the interval \( [G - 1.96 \frac{\sigma}{\sqrt{N}}, G + 1.96 \frac{\sigma}{\sqrt{N}}] \) with 95% confidence. Thus, one can use the error measure

\[ \text{Error} \approx \frac{2\sigma}{\sqrt{N}} \]  

in order to assess the accuracy of the estimator.

Several techniques exist for improving the accuracy of MC evaluation of finite integrals. In these techniques, one tries to construct an estimator with a reduced variance for a given, fixed number of samples, or equivalently, the improved estimator provides the same accuracy as the standard MC estimator but with considerably fewer number of samples. This is desirable because computing the value of \( g(X) \) is typically computationally or otherwise costly.

D. Importance Sampling

One MC variance reduction technique is importance sampling (IS) [3, 4]. IS improves upon the standard MC approach described above by drawing samples for \( X \) from another distribution \( f \). In (6) is first rewritten as below

\[ G = \int_{\Omega} \frac{g(X) f(X)}{f(X)} f(X) dX \]  

If \( X_1, X_2, \ldots, X_N \) are drawn from \( f \) instead of \( f \), the improved estimator \( G_N \) takes the form

\[ G_N = \frac{1}{N} \sum_{i=1}^{N} g(X_i) f(X_i) \]  

where the weighting factor \( f(X_i) / f(X) \) has been used in order to compensate for the use of samples drawn from the biased distribution \( f \). In order for the improved estimator above to be well-defined and unbiased, \( \tilde{f}(X) \) must be nonzero for every \( X \) for which \( f(X) g(X) \) is nonzero. We refer to this as the safety requirement. The ideal choice for the biasing distribution \( \tilde{f} \) is

\[ \tilde{f}_{\text{ideal}}(X) = \frac{f(X) / g(X)}{g(X)} \]  

which results in an exact estimator with variance zero with a single sample! However, \( \tilde{f}_{\text{ideal}} \) obviously can not be used in practice since the value of \( G \) is not known a priori. Instead, a practically realizable \( \tilde{f} \) that resembles \( \tilde{f}_{\text{ideal}} \) is used. The key to using IS in practical problems is the determination of an effective biasing distribution that results in significant variance reduction. We have identified one such biasing distribution by exploiting the SLE formalism that we use to construct an efficient and accurate estimator for the timing yield of digital circuits. This distribution will be described in Section III.

E. Monte Carlo Estimation of Timing Yield

A path \( \pi \) in a circuit \( C \) is a sequence of gates \( g_0, g_1, g_2, \ldots, g_n \), where \( g_0 \)'s inputs are primary inputs of the circuit, and \( g_n \)'s output is a primary output of the circuit. Given a circuit and values for the statistical parameters, a path is said to be critical if (i) it is sensitizable, and (ii) its delay is as large as the delays of other sensitzable paths. A path \( \pi \) is said to be statistically critical if it is a critical path of \( C \) for some possible assignment to process parameters. We denote by \( \Pi_{\text{crit}} \) the set of statistically critical paths. Then, the delay of a circuit is computed using

\[ d_{c}(X) = \max_{\pi \in \Pi_{\text{crit}}} d_{\pi}(X) \]  

where \( d_{c}(X) \) is the delay of the circuit and \( d_{\pi}(X) \) is the delay of path \( \pi \) when the circuit and process parameters are given by \( X \). A target delay \( T \) is specified for the circuit. Given a PDF \( f(X) \) for the statistical parameters, we would like to compute the fraction of circuits that satisfy \( d_{\pi}(X) \leq T \), i.e., the timing yield of the circuit. We define an indicator random variable \( I(T, X) \) for the entire circuit as follows: \( I(T, X) = 1 \) if the circuit delay exceeds the target, i.e., \( d_{c}(X) > T \), and \( I(T, X) = 0 \) otherwise. We then define the timing loss or simply loss with

\[ \text{Loss} = 1 - \text{Yield} = \int I(T, X) f(X) dX \]  

as the mean of the indicator random variable \( I(T, X) \) over the PDF \( f(X) \). Evaluation of the integral above is the timing yield (loss) estimation problem addressed in this paper.
In a straightforward application of the MC method to loss estimation, one would draw samples $X_1, X_2, \ldots, X_N$ from the statistical parameter space according to the PDF $f(X)$ and construct the loss estimator

$$\text{Loss}_N = \frac{1}{N} \sum_{i=1}^{N} I(T_c, X_i)$$

(16)

With the MC method, full circuit simulations (transistor-level SPICE simulations of the whole circuit containing the paths under consideration) must be performed for each sample point, $X_i$, in order to compute $d_c(X_i)$ and determine whether $I(T_c, X_i) = 1$ or 0. The MC method is widely used as a golden reference in the literature in assessing the accuracy and efficiency of timing yield estimation techniques. However, it is generally believed that it cannot be used in practice for estimating timing yield as it requires too many costly full circuit simulations for acceptable accuracy, even though there are some arguments to the contrary [5]. In the rest of this paper, the loss estimator in (16) is referred to as the standard MC (STD-MC) estimator.

Loss can also be estimated based on the SLE formalism, without performing any full circuit simulations. The delay of a circuit can be computed analytically based on the SLE formalism as follows

$$d^{\text{LE}}(X) = \max_{t \in \Pi} d^{\text{LE}}(X)$$

(17)

where $d^{\text{LE}}(X)$ is evaluated using the SLE formula in (5) and using SLE.d1 or SLE.d2. We define a new indicator random variable $I^{\text{LE}}(T_c, X)$, which takes the value 1 if the delay of a circuit computed analytically using the SLE equations exceeds the target delay $T_c$, i.e., $I^{\text{LE}}(T_c, X)$ is 1 if $d^{\text{LE}}(X) > T_c$, and 0 otherwise. The loss estimator based on this new indicator variable takes the form

$$\text{Loss}^{\text{LE}}_N = \frac{1}{N} \sum_{i=1}^{N} I^{\text{LE}}(T_c, X_i)$$

(18)

In computing $\text{Loss}^{\text{LE}}_N$, above, no full circuit simulations are performed. Only simple evaluations of the SLE delay formulas are needed, based on pre-characterizations of $f(X)$, $p(X)$ and $g(X)$ in (3) and (4). In contrast, the loss estimator in (16) requires $N$ full circuit simulations, one for every sample. The loss estimator in (18) will be referred to as the SLE-MC estimator in the rest of this paper.

The estimation of loss based on the STD-MC estimator in (16) will obviously be more accurate than the one based on the SLE-MC estimator in (18), but much more costly. We use the cheap SLE-MC estimator not by itself for yield estimation, but in a novel approach to constructing an IS-based loss estimator with reduced variance. This approach is called ISLE (Importance Sampling based on Stochastic Logical Effort) and provides the same accuracy as the STD-MC estimator but at a cost of much fewer number of full circuit simulations.

III. TIMING YIELD ESTIMATION WITH ISLE

The biasing distribution $f(X)$ used in ISLE is

$$\tilde{f}(X) = \frac{I^{\text{LE}}(T_c^e, X) f(X)}{\text{Loss}^{\text{LE}}_{\text{est}}}$$

(19)

This biasing distribution serves as a good approximation to the ideal but practically unrealizable biasing distribution for importance sampling, $f^{\text{ideal}}(X) / \text{Loss}^{\text{LE}}_{\text{est}}$. In (19) above, $T_c^e = (1 - \varepsilon) T_c$ and $\text{Loss}^{\text{LE}}_{\text{est}}$ is the loss computed by the SLE-MC estimator in (18) with the target delay set to $T_c^e$ instead of $T_c$, where $\varepsilon$ is a margin parameter which we explain below. The ISLE loss estimator is then constructed as follows

$$\text{Loss}^{\text{ISLE}}_N = \frac{1}{N} \sum_{i=1}^{N} I(T_c, X_i) \frac{I^{\text{LE}}(X_i)}{\text{Loss}^{\text{LE}}_{\text{est}}}$$

(20)

where the sample points $X_i$ must be drawn from $f(X)$ in (19) instead of $f(X)$. The margin parameter $\varepsilon$ was introduced above in order to guarantee that $f(X_i)$ is nonzero everywhere $I(T_c, X_i) f(X_i)$ is nonzero, i.e., $I^{\text{LE}}(T_c^e, X_i)$ must take the value 1 everywhere $I(T_c, X_i) = 1$. The margin parameter $\varepsilon$ must be large enough so that the indicator variables never assume the values $I^{\text{LE}}(T_c^e, X_i) = 0$ (the timing constraint $T_c^e$ is satisfied according to SLE) and $I(T_c, X_i) = 1$ (the actual circuit fails to satisfy the timing constraint) for any of the sample points. An automated and adaptive algorithm for the determination of the smallest value for the margin parameter $\varepsilon$ will be described in Section III-B.
The determination of an appropriate value of \( \epsilon \), the timing margin used by ISLE, is essential for the correctness, accuracy, and efficiency of the technique. On the one hand, \( \epsilon \) must be large enough to satisfy the correctness constraint that for every value of \( X \) that \( f(X) \) is non-zero, \( \epsilon \) is also non-zero. Since, \( f(X) \) is proportional to \( I(T_c, X) \), this translates to the safety requirement that \( I(T_c, X) = 1 \Rightarrow I(T_c, X) = 1 \). On the other hand, as can be seen in (25) and (30), the closest \( Loss^{LE, \epsilon} \) to \( Loss \) requires that \( \epsilon \) be kept small. Thus, to make ISLE accurate and efficient while preserving correctness, we must make \( \epsilon \) as small as possible without violating the safety requirement for any \( X \).

If SLE were a perfect approximation, a margin of \( \epsilon = 0 \) would satisfy the requirements above. However, as also demonstrated by our experimental results, stochastic SLE is inaccurate to an extent that is circuit and process parameter dependent. Therefore, the \( \epsilon \) margin must be determined separately for each different circuit and it must be checked that the resulting \( \epsilon \) satisfies \( I(T_c, X) = 1 \Rightarrow I(T_c, X) = 1 \).

This section presents ISLEXPLORER, an iterative heuristic algorithm for determining \( \epsilon \) (Algorithm 1) and estimating \( Loss^{LE, \epsilon} \). ISLEXPLORER interleaves steps of incrementing \( \epsilon \) and performing a number of full circuit simulations required to compute the ISLE estimator. When ISLEXPLORER terminates, a correct value of \( \epsilon \) is determined and all of the full circuit simulations required for computing the estimator \( Loss^{LE, \epsilon} \) (21) have been performed. ISLEXPLORER runs only a fixed number \( SafetyLimit \) of additional full circuit simulations beyond those needed for \( Loss^{LE, \epsilon} \) in order to ensure that the margin value \( \epsilon \) used is correct. As will become apparent below, the cost of the full circuit simulations are the dominant factor in the computational cost of ISLEXPLORER. Therefore, the computational cost of adaptively determining the margin parameter is a fixed number \( SafetyLimit \) full circuit simulations.

The intuition behind the operation of ISLEXPLORER is illustrated in Figure 1. The solid rectangle represents the two-dimensional parameter space. Every possible point in the rectangle corresponds a unique valuation of the parameters \( X \). The solid curve in Figure 1 consists of the points \( X \) for which the delay of the circuit is exactly \( T_c \). Outside the solid curve, circuit delay exceeds \( T_c \), i.e., \( I(T_c, X) = 0 \). Each dotted curve consists of points \( X \) for which \( d^{LE, \epsilon} (X) = T_c - \epsilon \) for a particular value of \( \epsilon \).

ISLEXPLORER considers \( NumFSamples \) samples generated from \( f(X) \) and computes \( \epsilon \) based on data it collects on these samples. ISLEXPLORER starts exploration with a negative initial value for the margin \( \epsilon_{\text{min}} \), gradually increases \( \epsilon \), ends exploration at \( \epsilon_{\text{end}} \) and determines \( \epsilon_{\text{min}} \) in the process. \( \epsilon_{\text{min}} \) is the smallest margin ISLEXPLORER can detect for which it can verify that the \( d^{LE, \epsilon} (X) = T_c - \epsilon_{\text{min}} \) curve lies completely inside the \( d^{LE, \epsilon} (X) = T_c \) curve. \( \epsilon_{\text{min}} \) is the value of \( \epsilon \) used by ISLEXPLORER for computing the ISLE estimator for timing loss (21). All circuit simulations required to compute the summation in (21) have already been performed when the \( \epsilon \) exploration is completed. At that point, to arrive at the value of the estimator \( Loss^{ISLE} \), all ISLEXPLORER needs is an estimate for the value of \( Loss^{ISLE, \epsilon_{\text{min}}} \) that is computed using the SLE-MC estimator in (18) as explained before. The computational cost of \( Loss^{LE, \epsilon_{\text{min}}} \) determination is unavoidable with ISLE and is not due to the adaptive determination of \( \epsilon \).

### Algorithm 1 ISLEXPLORER(\( MC\text{SimCapacity} \times \text{ExpectedMaxLoss}, T_c \))

1. \( NumFSamples \leftarrow \lfloor MC\text{SimCapacity} \times \text{ExpectedMaxLoss} \rfloor \)
2. Draw \( NumFSamples \) sample points \( \{X_1, X_2, X_3, \ldots, X_{NumFSamples}\} \) from \( f(X) \)
3. for \( i = 1 \) to \( NumFSamples \) do
4. \( X_i.\text{color} \leftarrow \text{BLACK} \)
5. end for
6. PointsInMargin \leftarrow 0
7. MC\text{LossCount} \leftarrow 0
8. while PointsInMargin \leq SafetyLimit do
9. EXPLORE \( (T_c, \epsilon, NumFSamples) \)
10. if PointsInMargin = 0 then
11. if (NewWhitePointsDiscovered) then
12. \( \epsilon_{\text{end}} \leftarrow \epsilon \)
13. LossPointsAt\( \epsilon_{\text{end}} \) \leftarrow MC\text{LossCount}
14. WhitePointsAt\( \epsilon_{\text{end}} \) \leftarrow WhitePoints
15. end if
16. end if
17. \( \epsilon \leftarrow \epsilon + \epsilon\text{-step} \)
18. end while
19. return \( \text{LossPointsAt}_{\epsilon_{\text{end}}} \times \text{WhitePointsAt}_{\epsilon_{\text{end}}} \times Loss^{LE, \epsilon_{\text{end}}} \)

B. ISLEXPLORER: The Margin Determination Algorithm

The determination of an appropriate value of \( \epsilon \), the timing margin used by ISLE, is essential for the correctness, accuracy, and efficiency of the technique.
At each iteration, ISLEEXPLORER increases the margin ε by ε-step. It then investigates (using the EXPLORE subroutine in Algorithm 2) the samples that fall between $d_E^T(X) = T_e - \epsilon$ and $d_E^T(X) = T_e - (\epsilon + \text{ε-step})$ and determines for each such sample $X$, whether $I(T_e, X) = 1$ is satisfied. The iterations continue until a value of margin $\epsilon_{\text{min}}$ is reached for which the number of samples $X$ that fall in a safety band defined by $d_E^T(T_e - \epsilon_{\text{end}}, X) = 1$ and $d_E^T(T_e - \epsilon_{\text{min}}, X) = 0$ (also $I(T_e, X) = 0$) reaches SafetyLimit, a user-given parameter.

ISLEEXPLORER uses the colors white and black to mark the status of samples $X$ generated from $f$. If $X$.color = Black, this indicates that a full circuit simulation has not been run for $X_i$. This is because for the values of the margin $\epsilon$ explored so far, $d_E^T(T_e, X)$ was found to be 0. If $X_i$.color = White, this indicates that an SL estimation and a full circuit simulation for $X_i$ has been performed and it has been determined whether the safety requirement is satisfied for $X_i$. White points do not need to be revisited when the value of $\epsilon$ increases, since the value of $I(T_e, X)$ and $d_E^T(T_e, X)$ do not change afterwards.

ISLEEXPLORER tries to obtain as accurate a delay estimate as possible while limiting the number of full circuit simulations to about $\text{MC} \times \text{SimCap}$, a parameter provided by the user. These $\approx \text{MC} \times \text{SimCap}$ samples are chosen among $\text{NumFSamples}$ samples generated from the distribution $f(x)$. The user also provides a rough estimate for an upper bound on the loss, $0 \leq \text{ExpectedMaxLoss} \leq 1$. From among $\text{NumFSamples}$ samples, we expect to run full circuit simulations for about $\text{ExpectedMaxLoss} \times \text{NumFSamples}$. Therefore, the algorithm selects $\text{NumFSamples}$ to be $(1/\text{ExpectedMaxLoss}) \times \text{MC} \times \text{SimCap}$. It should be noted that ISLEEXPLORER is a heuristic algorithm, and, as such, does not formally guarantee that the safety requirement is satisfied for all samples $X_i$. In order to keep the computational cost reasonable, instead of checking that the safety requirement is satisfied for all $\text{NumFSamples}$ samples $X_i$ (since this would require $\text{NumFSamples}$ full circuit simulations) ISLEEXPLORER considers margins larger than the minimum satisfactory $\epsilon_{\text{min}}$ and makes sure that for SafetyLimit samples $X_i$ that satisfy $T_e - \epsilon_{\text{min}} \leq d_E^T(X_i) \leq T_e - \epsilon_{\text{end}}$ (the points in the safety band) the safety requirement is not violated. This is done in order to build further confidence that the $\epsilon_{\text{min}}$ value arrived at is valid. In future work, we plan to investigate techniques that can formally ensure that the safety requirement is satisfied for importance sampling using the SLE approximation.

IV. RESULTS

A. Experimental Setup

We first explain the technical issues related to our experimental setup in order to help interpret our results better. We present results on two test circuits, InverterChain and GateChain shown in Figures 2 and 3. For both circuits, the timing loss is computed by comparing the delay between nodes 3 and 8 with the timing constraint. The precursor gates between nodes 1 and 3, and the postcursor gates between nodes 8 and 10 are placed in the circuit in order to realize a typical driver and load for the logic path under consideration. The gates used in these circuits are from Graham Petley’s 0.13μ library version 8.1 [6].

We consider three statistically varying process and circuit parameters [7]:
- Effective channel length $L_{eff}$ with a $3\sigma / \mu$ ratio of 15%.
- Supply voltage $V_{dd}$ with a $3\sigma / \mu$ ratio of 10%.
- Threshold voltage $V_{th}$ with a $3\sigma / \mu$ ratio of 10%.

These parameters are assumed to have Gaussian distributions, and are considered independent. We create three sets of statistical parameters from the above:
- OnePar: A one-parameter set consisting of $L_{eff}$.
- TwoPar: A two-parameter set consisting of $L_{eff}$ and $V_{dd}$.
- ThrPar: A three-parameter set consisting of $L_{eff}$, $V_{dd}$ and $V_{th}$.

For the results we report in this paper, we consider only inter-die correlations. In other words, the statistical parameters for all of the transistors in the circuit are fully correlated, and the variation in the parameters is location and transistor independent.

In order to empirically measure the error in the loss estimates obtained by the standard MC (STD-MC) estimator and our ISLE estimator, we perform 50 independent repetitions of the same experiment run. In our graphs and tables, experiment numbers 1 through 50 refer to these different runs. In each independent run, we compute the loss estimates using 1000 separate samples generated from $f$ in the parameter space. These 50 independent runs constitute samples of the loss estimator, and the variance and error of the loss estimator is computed over these 50 samples. For the STD-MC estimator, a reduced number of simulations are performed since most of the samples are discarded based on the evaluation of the SLE equations. The number of circuit simulations that are run for the ISLE estimator may be different in the 50 runs. In our tables and graphs, we report the average number of simulations over the 50 runs.

The loss value that is needed for computing the ISLE estimator in (19) and (21) is computed using the SLE-MC estimator in (18) using all of the 50000 sample points generated during the 50 runs.

We report and compare loss and error results for three estimators:
- the standard MC estimator: STD-MC,
- the ISLE estimator based on $f_{d1}$ and $f_{d2}$.
- the ISLE estimator based on SLE $d2$.

We report results for six different experiment configurations (combinations of a test circuit and a parameter set) in the next section on all of the six experiments we have run.

Figure 4 shows the graph of the loss estimator obtained with the STD-MC estimator and ISLE for all of the 50 experiment runs. The value of the ISLE estimator in each case is a lot closer to the mean than that of the STD-MC estimator. The variance reduction obtained by the ISLE estimator over STD-MC is thus apparent from this graph. We should note that for every loss estimate shown in Figure 4, 1000 transistor-level simulations are performed for STD-MC, but the average number of simulations for ISLE was only 213 over the 50 runs. Thus, if a normalization (to be explained below) is done considering that the errors for the two estimators are different, the Gain of ISLE over STD-MC is found to be 179, theoretically given by (30). Gain represents the ratio of the number of full circuit simulations required by the two approaches to achieve the same error.

As discussed before, the accuracy of the SLE approximation is key in order for it to facilitate IS for yield estimation. To gauge this accuracy, the scatter plots in Figures 5 and 6 show the errors in the loss estimates obtained with the SLE formulas versus delay computed with transistor-level circuit simulations. Figure 5 is for $SLE_{d1}$. Figure 6 is for $SLE_{d2}$. As seen in these plots, both versions of SLE formulas provide reliable delay estimates. However, $SLE_{d2}$ is more accurate, and hence it results in a bigger Gain as confirmed by the detailed results we present in the next section. This comes at the cost of having more pre-characterizations for parasitic delay $p$ and logical effort $g$ for all of the gates in the library, in addition to the reference inverter delay $\tau$.

Figure 7 confirms empirically that the $1/\sqrt{N}$ dependency of error on the number of MC samples is as expressed by (22) and (25) for the STD-MC and ISLE estimators, respectively. The significant reduction in variance that ISLE provides is also obvious in this graph. In this figure, a plot of loss error versus the number of full circuit simulations is shown for both estimators. The smooth curves in this plot were obtained using the theoretical error formulas. The two other curves were computed using data from the 50 runs, each of which explore...
sample set sizes ranging from 1 to 500. As explained before, full circuit simulations are performed at all of the sample points for the STD-MC estimator, but a reduced number of simulations are needed for the ISLE estimator. We observe the excellent match between the theoretical and experimental error curves in this plot.

C. Results

Table I presents results obtained from six experiments with the STD-MC estimator and our ISLE estimator based on both SLE.d1 and SLE.d2. The mean loss and loss error values are computed over 50 independent runs as explained before. The Gain value reported in the table represents the ratio of the number of full circuit simulations required by the STD-MC and SLE estimators to achieve the same error, theoretically given by (30). Gain here is computed using the experimental data for the loss errors and the actual number of circuit simulations reported in the table as follows:

\[ \text{Gain} = \frac{N_{MC} \cdot \text{Error}_{MC}^2}{N_{ISLE} \cdot \text{Error}_{ISLE}^2} \]

The second factor in the above formula is needed to perform a normalization required in order to make a correction for the difference in the errors achieved by the two estimators with the given number of simulations. The ratio of the squares of errors is used because of the \(1/\sqrt{N}\) dependency of error.

The results in Table I show that both versions of our ISLE yield estimator achieve significant cost reduction over the standard MC estimator for the same error, in the range from one to four orders of magnitude. As expected, ISLE based on SLE.d2 performs better, achieving two orders of magnitude cost reduction in the worst-case, whereas the cost reduction achieved by ISLE based on SLE.d1 goes down to 12 in the worst-case. The Gain data presented in Table I shows that ISLE performs better for the InverterChain circuit containing only inverters. This is due to the fact that the SLE delay formulas are more accurate for inverters because of their use in the SLE formalism as a delay reference. It should also be noted that the performance of ISLE improves considerably when only one statistical parameter is used, achieving a speed-up reaching three orders of magnitude. When more (two or three) statistical parameters are considered simultaneously, the performance degrades in comparison but still above a respectable two orders of magnitude speed-up with ISLE based on SLE.d2.

V. Conclusion

We have demonstrated in this paper that Monte Carlo simulation in conjunction with a novel variance reduction technique, Importance Sampling with Stochastic Logic Effort, can serve as an accurate yet computationally viable timing yield estimation method. Numerous other techniques for reducing the variance of Monte Carlo estimators have been proposed in the Monte Carlo simulation literature [3,8]. The stochastic logic effort formalism can be used to facilitate other techniques for variance reduction in Monte Carlo estimation, e.g., stratified sampling, control variables, multicanonical Monte Carlo method, etc. [4], which we intend to explore in future work.

REFERENCES

[1] I. Sutherland, B. Sproull, and D. Harris. Logical Effort: Designing Fast CMOS Circuits. Morgan Kaufmann, 1999.
[2] A. Demir and S. Tasiran. Statistical logical effort: Designing for timing yield on the back of an envelope. In ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), February 2006.
[3] Malvin H. Kalos and Paula A. Whitlock. Monte Carlo Methods, Volume 1, Basics. Wiley, 1986.
[4] P. Glasserman, P. Heidelberger, and P. Shahabuddin. Importance sampling and stratification for value-at-risk. In Proc. 6th Intl. Conference on Computational Finance, pages 7–24. MIT Press, May 28-31 1999.
[5] L. Schellnhuber. The count of Monte Carlo. In ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), February 2004.
[6] http://www.vlsitechnology.org/. Cell Library, Release 8.1.
[7] Y. Cao, H. Qiu, R. Wang, P. Friedberg, A. Vladimirescu, and J. Rahey. Yield optimization with energy-delay constraints in low-power digital circuits. In IEEE Conference on Electron Devices and Solid-State Circuits, December 2003.
[8] A. D. Sokal. Monte carlo methods in statistical mechanics: Foundations and new algorithms. In P. Cartier C. DeWitt-Morette and A. Folacci, editors, Functional Integration: Basics and Applications (1996 Cargèse summer school). Plenum, 1997.
### TABLE I

**EXPERIMENTAL RESULTS COMPARING STANDARD MC AND ISLE**

|                      | Mean Loss | Loss Error      | Number of Ckt. Simulations | Gain  |
|----------------------|-----------|-----------------|-----------------------------|-------|
|                      | SLE.d1    | SLE.d2 | STD-MC | SLE.d1    | SLE.d2 | STD-MC | SLE.d1 | SLE.d2 | STD-MC |
| Exp(InverterChain, OnePar) | 0.1394   | 0.1394 | 0.1395 | 1.15e-3  | 1.28e-3 | 2.35e-2 | 181    | 181    | 1000   | 2305  | 1866  |
| Exp(InverterChain, TwoPar) | 0.1481   | 0.1483 | 0.1482 | 8.15e-3  | 1.72e-3 | 1.87e-2 | 211    | 190    | 1000   | 25    | 624   |
| Exp(InverterChain, ThrPar) | 0.1535   | 0.1537 | 0.1538 | 8.72e-3  | 2.15e-3 | 2.03e-2 | 218    | 196    | 1000   | 25    | 457   |
| Exp(GateChain, OnePar)   | 0.1575   | 0.1575 | 0.1576 | 1.32e-3  | 1.33e-3 | 2.34e-2 | 199    | 199    | 1000   | 1589  | 1549  |
| Exp(GateChain, TwoPar)   | 0.1686   | 0.1684 | 0.1688 | 1.08e-2  | 2.81e-3 | 2.24e-2 | 248    | 211    | 1000   | 17    | 300   |
| Exp(GateChain, ThrPar)   | 0.1739   | 0.1741 | 0.1743 | 1.28e-2  | 2.80e-3 | 2.92e-2 | 259    | 217    | 1000   | 12    | 307   |