Identifying DC Faults in HVDC-VSC Systems for Integrating Large Offshore Wind - A Localized Protection Scheme

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Abstract—We propose a localized protection scheme based on rate of change of Running Autoregressive Smoothing Average (RASA) of fault limiting reactor voltage in VSC-HVDC systems. The paper addresses the issues of DC-fault identification, such as measurement quality, high impedance faults (HIFs) and external faults, when a localized protection scheme is employed. The scheme is validated to be selective, dependent and secure for DC fault identification in the presence of White Gaussian Noise (WGN) in measurement. The scheme operation is validated to be intact for High Impedance Faults (HIFs) and external faults. Finally, to validate the performance of our localized protection scheme, we perform a comparison with already existing ones in the literature.

Index Terms—HVDC, localized protection, fault identification, DC fault.

I. INTRODUCTION

NATIONAL and international ambitions to reduce the emission of greenhouse gases result in Renewable Energy Sources (RES) progressively replacing conventional generation based on fossil fuels [1], [2]. The North Sea countries have signed a political declaration and action plan that emphasizes their commitment to develop the necessary infrastructure for large scale offshore wind integration [3]. Representatives of Dutch, Danish and German Transmission System Operators (TSOs) have signed an agreement to develop the North Sea Wind Power Hub (NSWPH), an artificial energy island in the North Sea connecting up to 30GW wind power to the connected countries [4]. The island would be a large connection point of thousands of offshore wind turbines and would create an offshore network far out at sea. Additionally, in Europe, a large amount of offshore is expected to be built, where potential has been identified to an increase of on-and offshore wind power to 150 GW by 2030 [4].

For such a network, High Voltage Direct Current (HVDC) technology is the preferred solution to build a cost-effective power transmission. Due to the advancement of technology, IGBT based VSCs (voltage source converters) are replacing the thyristor based electromechanical converters in the HVDC transmission system but the protection aspect of the HVDC system has rather been the same, relying on the crude approach of blocking the converters in case of any fault inception. However, with the introduction of application of High Voltage solid state circuit breakers, the idea of multi-terminal VSC-HVDC configuration seems as valuable option for interconnecting different countries and integrating large offshore wind (e.g. four-terminal ±500 kV/3000 MW HVDC project in Zhangbei, China [5]). To facilitate secure integration of multi-terminal HVDC interconnections, system operators need to assess the system reliability under DC faults to guarantee the N-1 criterion. However, DC fault identification, interruption and isolation remain a challenge. This is due to:

- high rate of rise of current in DC. Since DC has no frequency, the impedance due to reactance is absent.
- no zero crossing of current in DC.
- sensitive power electronic switches of the converters prone to damage with their threshold rating only twice the full load rating [6].

Thus, there is a requirement of a protection scheme with the following attributes:

- Secure: Scheme operation intact for a transient occurring in the system. For eg. wind power output reduction.
- Dependent: Scheme giving a trip signal for a fault contingency in the system. For eg. relay allotted to identify DC faults, tripping for a fault $F_1$ in Fig. 1.
- Selective: Scheme operation intact for a fault outside the zone of a relay. For eg. relay allotted to identify DC faults, not tripping for fault $F_2$, $F_3$ and $F_4$ in Fig. 1.

A thorough overview is presented by authors in [7] on the challenges in protection of HVDC-VSC system. The primary protection employed in practical VSC-HVDC systems are travelling-wave based protection [8]-[9]. SIEMENS and ABB have been employing localised method enabled travelling wave protection in their respective products (SIMATIC-TDC series by SIEMENS; MACH3 series by ABB) [10]-[11] for conventional HVDC protection. However, the idea of a localised backup relay is a more robust approach to its communication-based counterpart. The reason is the travelling wave delay and data asynchronization for long transmission lines for communication-based...
Fig. 1: Offshore wind system with multiterminal VSC-HVDC configuration subjected to fault contingencies at different locations

The proposed algorithm takes the voltage of the fault limiting reactor into consideration [refer to Fig. 2]. This voltage is employed to realise RASA, expressed as:

$$V_i(n) = \frac{n}{k=m \sim n} v_t(k)$$

(2)

where $v_t(k)$ is the instantaneous value of $t^{th}$ node voltage at $k^{th}$ sample with a moving window of $(n-m)$. Once RASA
Fig. 2: Proposed Protection schematic

Fig. 3: (a) Zoomed $V(t)$[kV] vs t[s] (b) Zoomed $\phi(t)$[kV/s] vs t[s] for a fault $F_1$ of $R_f=200\Omega$ in Fig. 2.

for the fault limiting reactor voltage is evaluated, the rate of change of this voltage ($dV/dt$) is employed as the trigger signal to evaluate the decisive parameter $\phi_i(n)$. Fig. 3(a) shows the characteristics of RASA voltage ($V$) upon a fault contingency. The bus voltage collapses in case of a fault inception and hence $dV/dt$ is negative. Fig. 3(b) shows the variation of decisive parameter $\phi_i(n)$ with time. $\phi_i(n)$ is mathematically evaluated as:

$$\phi_i(n) = V_i(n) - V_i(n-d)$$  \hspace{1cm} (3)

where $d = b-a$ stands for the delay in samples to calculate the parameter, $\phi_i(n)$ [refer to Fig. 4]. The idea of employing $\phi_i(n)$ is different compared to other existing schemes [13]-[18]. The reason being the proposed scheme relying on a more specific fault characteristics (see Fig. 3(b)) than violation of a single static threshold keeping the security, dependability and selectivity of the proposed scheme intact.

To elaborate the algorithm proposed, the slope, $dV/dt$ is compared to slope threshold, $x$ (the analysis for $x$ is given in Section III). A window search from the instant (sample $a$) it violates the negative slope threshold, -$x$ to the instant (sample $b$) it violates the positive threshold, $x$ occurs (refer to Fig. 4). The window search from sample $a$ to sample $b$ includes evaluating condition defined as:

$$\min_{n=a}^{n=b} \phi_i(n) < -\phi_{thresh1}$$  \hspace{1cm} (4)

$\phi_{thresh1}$ is mathematically analysed in Section III. If equation (4) is satisfied, another window search from sample $b$ to sample $2b-a$ occurs. A trip signal is generated if the following final condition is violated:

$$\max_{n=b}^{n=2b-a} \phi_i(n) > \phi_{thresh2}$$  \hspace{1cm} (5)

$\phi_i(n)$ is subjected to a two-stage violation to give a trip signal as explained subsequently in Fig. 4. The parameters $x$, $\phi_{thresh1}$ and $\phi_{thresh2}$ have been mathematically elaborated in Section III.

III. MATHEMATICAL ANALYSIS OF THE THRESHOLD EMPLOYED

This section presents the mathematical analysis behind the derivation of decisive parameters i.e., $x$, $\phi_{thresh1}$ and $\phi_{thresh2}$. Fig. 6 shows the equivalent multiterminal VSC-HVDC circuit employed for the analysis. Upon inception of
a DC fault in a particular segment of the HVDC transmission system, the contribution from the wind farms and the DC capacitor of the faulty and healthy segment need to be analysed for the calculation of thresholds. The contribution is however limited by the inductance in the path of the fault where the rate of rise of current is inversely proportional to the inductance in the path [26].

Fig. 5 shows the current contribution upon a fault inception as shown in Fig. 6. Initially, contribution of \( I_{c3} \) in the fault current is very less in comparison to \( I_{c2} \). This can be explained with the idea suggested above [26] i.e., the rate of rise of current is limited due to larger value of inductance in path of fault for \( I_{c3} \). Hence, the contribution of other terminal capacitor is neglected for the initial sub-transient analysis ahead for \( x \), \( \varphi_{thresh1} \) and \( \varphi_{thresh2} \). The proposed mathematics gives an optimistic value of threshold employed. The threshold derived is not exact since contributions from various segments are neglected. Considering the faulty segment in Fig. 6;

\[
\nu_{c1}(t) = L_1 \frac{di_{L1}(t)}{dt} + \nu_{m1}(t) \quad (6)
\]

where \( \nu_{c1}(t) \) and \( \nu_{m1}(t) \) are the instantaneous voltages across the DC capacitor and across the fault limiting reactor; \( i_{L1}(t) \) is the instantaneous current across the fault limiting reactor. Also,

\[
\nu_{c1}(t) = \nu_{c1}(0^-) - \frac{\int i_{L1}(t)dt}{C_1} \quad (7)
\]

where \( \nu_{c1}(0^-) \) is the pre-fault voltage across the DC capacitor. The two equations can be re-arranged to the form,

\[
\nu_{m1}(t) = \nu_{c1}(0^-) - \frac{\int i_{L1}(t)dt}{C_1} - L_1 \frac{di_{L1}(t)}{dt} \quad (8)
\]

The parameter for fault identification has been already defined in section III as \( \varphi_{thresh1}, \varphi_{thresh2}, \varphi \).

1) Analysis of \( \varphi_{thresh1} \): \( \varphi_1(t) = \nu_{m1}(t) - \nu_{m1}(0^-) \quad (9) \)

where \( \nu_{m1}(t) \) and \( \nu_{m1}(0^-) \) are RASA voltages. Also, since pre-fault case refers to steady state DC operation for the HVDC transmission with DC link voltage maintained at a value,

\[
\nu_{m1}(0^-) = \nu_{c1}(0^-) = V_{m1}(0^-) = V_{c1}(0^-) \quad (10)
\]

Since the drop in the voltage is instantaneous,

\[
\varphi_1(t) = \frac{\nu_{c1}(0^-) + \nu_{m1}(t)}{2} - \nu_{c1}(0^-) \quad (11)
\]

\[
\varphi_1(t) = \frac{\nu_{m1}(t) - \nu_{c1}(0^-)}{2} \quad (12)
\]

Introducing \( \varphi_{thresh1} \) in the analysis,

\[
\varphi_{thresh1} = \nu_{thresh1} = \varphi_1(t)|_{min} \quad (13)
\]

The idea of analysis is to get the minimum permissible value for \( \varphi_{thresh1} \) that can work for a system with any possible contingency (pole-pole faults, pole-ground faults). Hence, the analysis should be studied for 100% cable length and maximum fault resistance scenario \( (R_f=200 \Omega) \) in the work) in a system.

\[
\varphi_{thresh1} = \frac{\nu_{m1}(0^-)}{2} - \frac{\nu_{c1}(0^-)}{2} \quad (14)
\]

\[
\varphi_{thresh1} = \frac{\nu_{c1}(0^-) - \frac{\int i_{L1}(t)dt}{C_1}|_{max} - L_1 \frac{di_{L1}(t)}{dt}|_{max} - \nu_{c1}(0^-)}{2} \quad (15)
\]

The current differential term can be neglected since its contribution is negligible in comparison to the second term of equation (15). This is because the current differential term is getting multiplied with \( L_1 \) whereas the current integral term is divided by \( C_1 \). This lower-bound value gets violated for a HIF as well as for a bolted fault in the HVDC-VSC system.

\[
\varphi_{thresh1} = -\frac{\int i_{L1}(t)dt}{2C_1} \quad (16)
\]

Realising the discrete analysis for the same, the threshold, \( \varphi_{thresh1} \) can be finally expressed as,

\[
\varphi_{thresh1} = -\frac{(b-a)\sum_{k=a}^{b} i_{L1}(k)}{2C_1} \quad (17)
\]

where \( (b-a) \) is the moving average window. The dependence of \( \varphi_{thresh1} \) on cable length and fault resistance is accounted with \( i_{L1}(k) \) in the analysis.

2) Analysis of \( \varphi_{thresh2} \): The threshold for the \( \varphi_{thresh2} \) has been defined as:

\[
\varphi_{thresh2} = -\eta \varphi_{thresh1} \quad (18)
\]

where \( \eta \) is defined as the damping variable for the RLC circuit shown in Fig 6. The idea of analysis is get the minimum permissible value for \( \varphi_{thresh2} \). Hence, the variation of \( \eta \) is analysed for 100% cable length and maximum fault resistance scenario for a system. \( \eta \) is expressed as:

\[
\eta = \frac{\beta rD}{rD + a R_f} \quad (19)
\]

where \( 0 < \{a, \beta\} \leq 1 \) are system dependent.
Fig. 6: Equivalent simplified multiterminal VSC-HVDC circuit employed to evaluate $\phi_{thresh}$

Fig. 7: A fault (F1) in Fig. 1(b) occurs at t=0.03s. For a fault impedance of 50$\Omega$, (a) $\phi_1(t)$ [kV/s] vs t[s] for $\sigma=0.1$, (b) ROTV$_1(t)$ [ratio] vs t[s] for $\sigma=0.1$, (c) ROCOV$_1(t)$ [kV/s] vs t[s] for $\sigma=0.1$, (d) $\phi_1(t)$ [kV/s] vs t[s] for $\sigma=0.3$, (e) ROTV$_1(t)$ [ratio] vs t[s] for $\sigma=0.3$, (f) ROCOV$_1(t)$ [kV/s] vs t[s] for $\sigma=0.3$, (g) $\phi_1(t)$ [kV/s] vs t[s] for $\sigma=0.5$, (h) ROTV$_1(t)$ [ratio] vs t[s] for $\sigma=0.5$, (i) ROCOV$_1(t)$ [kV/s] vs t[s] for $\sigma=0.5$
3) Analysis of \( x \): The slope of the RASA of fault limiting reactor voltage is analysed for 100% cable length and maximum fault resistance scenario for a system. The slope is defined as:

\[
\frac{dV}{dt} = \frac{V_{m1}(1) - V_{m1}(0)}{T_s}
\]

where \( n = 0 \) is the fault inception point in a system. The slope is further realised as:

\[
\frac{dV}{dt} = \frac{\nu_{m1}(1) + \nu_{m1}(0^-) - \nu_{m1}(0^+)}{2T_s}
\]

The slope threshold is defined in Section II as:

\[
x = \frac{dV}{dt} \mid _{\text{min}}
\]

The static slope threshold is implemented for maximum fault resistance in the system and hence is realised for its minimum value. Using equation (8) in the analysis,

\[
x = \frac{i_{\chi}(0)}{2C_1} \left[ 1 - \frac{L_1 C_1}{T_s^2} \right] - \frac{i_{\chi}(1)}{2C_1} \left[ 1 + \frac{L_1 C_1}{T_s^2} \right]
\]

where \( T_s \) is the sampling time of data acquisition.

IV. RESULTS

The test configuration explained in Fig. 1(b) has been implemented in RTDS, the software support system for RTDS. The control architecture employed is based on IEEE standards [27]-[28]. Bergeron transmission line model has been employed for the test configuration and the respective parameters are depicted in Table I. Based on equation (17) and (18), \( \varphi_{\text{thresh1}} \) and \( \varphi_{\text{thresh2}} \) are equal to -120kV/ms and 80kV/ms respectively for a sampling frequency of 20kHz. The threshold is calculated for a HIF of 200\( \Omega \) with the self-explanatory idea of the scheme working for fault resistances equal or lower to 200\( \Omega \).

TABLE I: Parameters implemented in RSCAD model

| Parameter                  | Value   |
|----------------------------|---------|
| DC-link Voltage (\( V_1 \)) | 700kV   |
| AC grid forming Voltage (\( N_{789} \)) | 220kV (peak) |
| Frequency of operation     | 50Hz    |
| DC-link Capacitor (\( C_1 \)) | 500\( \mu \)F |
| Fault Limiting Reactor     | 0.1H    |
| Sampling Frequency         | 20kHz   |
| Moving average window (n-m)|         |
| Delay (d)                  | 600e-6s |
| \( \varphi_{\text{thresh1}} \) | -120kV/ms |
| \( \varphi_{\text{thresh2}} \) | 80kV/ms  |
| \( x \)                    | 60kV/ms |
| \( a \)                    | 0.1     |
| \( \beta \)                | 0.7     |
| HVDC Tower type            | 1c/1g:735kV |
| Sub-conductor Radius       | 4.034cm |
| DC Resistance/km           | 0.0712 \( \Omega \) |
| Reactance/km               | 0.5mH   |
| Shunt Conductance          | 1e-11 \( \Omega \) |

Fig. 8: (a) \( V_1(t) \)[kV] vs t[s] for \( R_f=50\Omega \), (b) \( N_{789}(t) \)[kV] vs t[s] for \( R_f=50\Omega \), (c) \( \varphi_1(t) \)[kV] vs t[s] for \( R_f=50\Omega \), (d) \( V_1(t) \)[kV] vs t[s] for \( R_f=100\Omega \), (e) \( N_{789}(t) \)[kV] vs t[s] for \( R_f=100\Omega \), (f) \( \varphi_1(t) \)[kV] vs t[s] for \( R_f=100\Omega \)

A. Effect of White Gaussian Noise (WGN)

Fig. 7 shows the comparison of the proposed scheme with the existing acknowledged protection schemes i.e., ROTV and ROCOV in the presence of WGN. \( \sigma \) of the noise is varied from 0.1 to 0.5 to see how different schemes react to a fault inception in the presence of noise. A fault occurs at \( F_1 \) of Fig. 1(b) at \( t=0.03s \) and the response of different schemes for varying \( \sigma \) is shown in Table II.

When there is WGN in the signal measurement, it is very difficult to set a static threshold for the rate of change of any parameter, that can work well in identifying a fault despite the noise. Unlike the case of considering a static threshold for the rate of change of fault limiting reactor voltage to detect the fault contingency, considering rate of change of RASA fault limiting reactor voltage along with a decisive parameter, \( \varphi_1(n) \) make the scheme immune to this random noise up to \( \sigma \) of 0.5 in the signal measurement. The reason why RASA performs better than other schemes is that RASA averages over a window of samples and WGN has zero mean [29]. Hence, averaging the samples reduces the effect of noise in the measurement. However, since the algorithm takes various stages for a trip signal generation, noise as high as \( \sigma \) of 0.5 is not
affecting the operation of proposed scheme. Fig. 7(g) shows WGN making \( \phi_1(t) \) violate the positive threshold at \( t = 0.01s \). However, the scheme still gives no-trip signal for such variations.

B. Effect of Fault Resistance

The effect of varying fault resistance is shown in this subsection. Fig. 8 shows the effect of increasing fault resistance on the performance of the proposed algorithm. Fig. 8(a) shows steeper voltage collapse than in Fig. 8(d). This explains lesser voltage drop for higher fault resistance. The AC side grid forming voltage [refer VSC2 in Fig. 6] \( N_{789} \) is dependent on the DC voltage profile, \( v_{c1} \). Hence, Fig. 8(b),8(e) give the same conclusion of higher voltage drop on AC side as well for a lesser fault resistance. Fig. 8(c) shows \( \phi_1(t) \) for increasing fault resistance. The damping of the system increases with fault resistance which can be verified in Fig. 8(f).

The authors in [23] give a thorough comparison of performance of different schemes for high impedance faults. The proposed scheme works robustly in the presence of HIFs in the system. The different stages for trip signal [refer Fig. 4] mark their peculiarity for DC faults working well with HIFs as can be seen in Fig. 9. The scheme is tested for \( R_f \) up to 200Ω where the threshold has been derived for fault with \( R_f = 200Ω \) in section III. Decreasing the threshold further to make the same proposed scheme implementable for \( R_f > 200Ω \) can be one idea to make the same scheme work for higher fault impedances. However, there is always a trade-off between security and identification for HIFs in localised protection schemes.

C. Effect of fault on AC side

The effect of an external fault is realised to check the selectivity of the proposed algorithm as shown in Fig. 10. A comparison of the existing schemes for selectivity is done in [23]. The proposed work is validated to be secure for an external fault. A line to line fault occurs between \( N_7 \) and \( N_8 \) shown in Fig. 6. The fault represents the family of faults \( F_2 \), \( F_3 \) and \( F_4 \) shown in Fig. 1(b). Gaussian noise of \( \sigma = 0.4 \) is included for the analysis. \( \phi_1(t) \) is observed to not violate the threshold for any external fault in the system.

D. Detection Time

The maximum detection time is 2.2ms for a fault resistance \( (R_f) \) of 200Ω. The detection time is dependant on the value of DC link capacitor and Fault Limiting Reactor. Decreasing the value of DC link capacitor or/and value of Fault Limiting Reactor would decrease the detection time. However, the robustness in the presence of WGN would decrease as well.

V. Conclusion

The contribution of the proposed work has been to address the issue of measurement quality and HIFs for DC fault identification in VSC-HVDC systems. The work proposes a secure, selective and dependable protection scheme which is local in nature. The proposed protection algorithm takes Running Autoregressive Smoothing Average (RASA) of the fault limiting reactor voltage into consideration. The scheme is validated to be robust in the presence of White Gaussian Noise (WGN) up to standard deviation \( (\sigma) \) of 0.5. The scheme is also validated to work satisfactorily for HIFs of up to 200Ω. A comparative analysis of the existing acknowledged protection schemes (Rate of Change of Voltage (ROCOV), Rate of Transient Voltage (ROTV)) and the proposed work has been realised to justify the focus of the work. Further, the robustness of the scheme for external faults has been validated for selectivity. An offshore
wind VSC-HVDC system has been simulated in RSCAD, the software support system for Real Time Digital Simulator (RTDS). The proposed protection scheme is extremely robust and simple to implement for DC fault identification in HVDC systems. The scheme can also be implemented to MVDC shipboard power system. Future work will focus on an online fault identification method that gives the location of the DC fault in HVDC-VSC systems.

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