3DCAM: A Low Overhead Crosstalk Avoidance Mechanism for TSV-Based 3D ICs

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ABSTRACT

Three Dimensional Integrated Circuits (3D IC) offer lower power consumption, higher performance, higher bandwidth, and scalability over the conventional two dimensional ICs. Through-Silicon Via (TSV) is one of the fabrication mechanisms that connects stacked dies to each other. The large size of TSVs and the proximity between them lead to undesirable coupling capacitance. This interference causes mutual influences between adjacent TSVs and produces crosstalk noise. Furthermore, this effect threatens the reliability of data during traversal between layers. This paper proposes a mechanism that efficiently reduces crosstalk noise between TSVs with lower area overhead as compared to previous works. This mechanism revolves around the fact that retaining TSV value in current state can reduce coupling in some cases. To evaluate the mechanism, gem5 simulator is used for data extraction and several benchmarks are taken from the SPEC2006 suite. The simulation results show that the proposed mechanism reduces crosstalk noise with only 30% imposed TSV overhead while delay decreased up to 25.7% as compared to a recent related work.

Keywords Interconnection · TSV · 3D IC · 3D Integration · Crosstalk · NoC

1 Introduction

Technology node scaling in recent decades ushered in gate delay cut-off and rise of interconnection latency [1]. Hence, interconnects have become a major performance bottleneck of high performance System-on-Chips (SoC) and Integrated Circuits (IC) [23]. In addition, interconnections have become more susceptible to noises in particular crosstalk [23]. On the other hand, the advent of multi-core processors with ever increasing number of cores has highlighted the need for fast and reliable interconnections. One of the potential solutions to alleviate the interconnection delay problem is the three dimensional integration using Through-Silicon Vias (TSV). Vertical integration of IC dies using TSVs offers high density connections between adjacent dies. This technology also allows stacking of dies with nonidentical technologies such as CMOS with high density DRAM which can be used as a solution to mitigate memory wall problem [19]. Furthermore, the average and maximum distance between interconnect nodes of the 3D stacked ICs are greatly decreased which leads to significant delay, power, and area improvement. Despite of the TSV advantages, the adjacent, short and bounded TSVs are prone to TSV-to-TSV coupling and crosstalk noise which increases transmission time and power consumption, and more importantly, it threatens the signal integrity [17] [18].

*This work has been done while the authors were at Sharif University of Technology.
Figure 1: Overview of coupling characteristics in TSVs \[8\]; According to ITRS \[15\], it is predicted that the height of TSVs will reach to 20-50 µm and the via diameter will be 2-8 µm till 2018.

As demonstrated in Fig. 1, every TSV may be surrounded by neighbour TSVs which cause a big and undesirable coupling noise. This TSV-to-TSV coupling could be very challenging in 3D ICs due to the fact that TSVs are large and thick, thus the coupling between two adjacent TSVs can be huge. Moreover, the effective coupling capacitance between TSVs doubles when the aggressor and the victim signals switch in opposite directions\[18\].

Plenty of crosstalk minimization methods have been proposed in the literature of 2D design (e.g. \[5, 11, 12, 14, 26\]). However, these methods cannot be directly applied to alleviate TSV-to-TSV crosstalk noise, inasmuch as the TSVs are not placed in the same planar and are greatly affected by more than two aggressors \[27\]. Recent efforts in TSV-to-TSV crosstalk minimization including \[4, 17, 27\] are complex and impose significant area and TSV overhead. ShieldUS \[4\], by adding a crossbar, remaps data to TSVs in order to shield more active signals by the signals which predicted to have less transitions in the future. In addition to its complex decision-making circuit, the accuracy of its predictor is under question due to the fact that the signals may not have a regular pattern. 3DLAT \[27\] exploits less adjacent codes to limit maximum number of transitions in adjacent TSVs. Crosstalk Avoidance Codes (CAC) \[17\] is another coding scheme for TSV-to-TSV crosstalk minimization. These approaches also need a complex and large coder and also suffer from a considerable information redundancy overhead.

In this paper, we propose a TSV-to-TSV crosstalk minimization method, named 3DCAM, which can effectively reduce coupling noise between TSVs with a relatively low area and TSV overhead. In addition, the proposed method uses a small simple coder which reduces run-time performance overhead. In the case of a transition on a target signal, considering the target’s neighbours and their coupling effect, 3DCAM decides to whether retain target’s value or send its original transition. In the condition that coder decides to retain the value it informs the decoder through a control TSV. The simulation results show that 3DCAM can reduce the transmission delay up to 25.7% as compared to 3DLAT mechanism. 3DCAM imposes only 30% TSV overhead which is much less than the 3DLAT TSV overhead (which is 80% for \(\omega = 4\)).

The rest of this paper is structured as follows. In Section II, related works are reviewed. Section III describes the crosstalk model for TSVs based 3D ICs on which 3DCAM is built. In Section IV we present 3DCAM crosstalk avoidance mechanism. Section V explains the simulations and results and, finally, Section VI concludes the paper.

2 Related Work

In the context of Two Dimensional Network-on-Chips (2D NoC), there are plenty of works that target power consumption \[9, 10, 20\], reliability \[20\], security \[24\], or performance \[20\] of the interconnections. Particularly, crosstalk minimization methods can be classified in three categories: physical level, transistor level and, Register Transfer Level (RTL) techniques. Wire spacing \[1\], active and passive shielding \[26\], and buffer insertion \[2\] are examples of physical level techniques. \[14\] is a transistor level mechanism which reduces the crosstalk noise by skewing the simultaneous opposite transitions. Although this approach reduces the crosstalk, it requires timing adjustment between senders and receivers. Furthermore, this approach suffers from run-time management. The general idea behind RTL level techniques is to omit some undesirable transition patterns by using coding schemes. There are variety of works that focused on analytical aspect and coding concepts \[5, 25\]. Error detection codes and error correction codes \[12\], joint crosstalk avoidance mechanism \[25\], and CACs \[12\] are examples of these coding schemes.
Although the above approaches may cope with crosstalk in 2D ICs, they cannot be directly applied in 3D technologies because the additional dimension makes consequential differences in crosstalk problem analysis. Gathering the long and thick TSVs causes new reliability issues which have been studied recently [16, 22]. Several mechanisms have been proposed to make 3D ICs more reliable against crosstalk noise, e.g., [4, 6, 7, 17, 27]. The TSV-to-TSV capacitance and inductance coupling are two major threats to 3D IC reliability. Previous works have concentrated on these effects from two perspectives. [4, 17, 27] proposed capacitance-based mechanisms and [6, 7, 21] proposed inductance-based techniques to reduce crosstalk effects in 3D ICs.

Increasing TSV distances from each other, shielding TSVs, inserting buffers at the victim side, inserting buffers, decreasing driver size at the aggressor side, and increasing load at the wires are the mechanisms examined in [18] to mitigate TSVs crosstalk noise. According to their experiments, unlike 2D wires, increasing TSV distances is not an effective solution to TSV-to-TSV coupling problem and the other solutions either need high effort at post-design time or have negative impact on timing performance.

RTL mechanisms in 3D IC have been proposed and experimented recently. [17] proposed a coding scheme that reduces the maximum crosstalk about 28% based on their proposed crosstalk model. Two other mentionable mechanisms in 3D IC against crosstalk noise which have been studied recently are ShieldUS [4] and 3DLAT [27]. ShieldUS uses data with less transitions as the shield for the more active data. ShieldUS tries to minimize average transmission time with run-time mechanism that remaps data to TSVs in order to banish links with specific crosstalk pattern from others. The TSV overhead of this method is not considerable because it uses the same data as shield. But a large crossbar is required for bit shuffling which imposes considerable area overhead. This crossbar will get larger by increasing the number of bits to shuffle. Besides, this method needs the data to be highly regular, as this method tries to predict the activity of the signals.

The authors in [27] introduce use of less adjacent transition code along with transition signaling to minimize the number of transitions. Furthermore, 3DLAT reduces higher crosstalk class frequency. This scheme has a significant TSV overhead which is not negligible. According to the authors’ report, TSV overhead of 3DLAT is about 80% with ω = 4. This mechanism imposes more than 160% area overhead with ω = 2 for the same bitwidth. This method also suffers from significant area overhead which imposed by its complex coder.

### 3D Crosstalk Coupling Noise Model

In 2D integrated circuits, three neighbor wires affect each other and create coupling capacitance. The effective coupling capacitance which imposed on the victim (i.e. middle) wire is modeled by Eq. (1) [14].

\[
C_{e_{ff}} = C_{G} + C_{C} \left| \frac{\Delta V - \Delta V_{-1}}{V_{dd}} \right| + C_{C} \left| \frac{\Delta V - \Delta V_{+1}}{V_{dd}} \right|
\]  (1)
Figure 3: Layout of control TSVs for $3 \times N$ bus

Where $\Delta V$ is swing voltage on victim wire, $\Delta V_{-1}$ and $\Delta V_{+1}$ are the voltages that switch on neighbor wires and $V_{dd}$ is the supply voltage. In addition, $C_c$ is coupling capacitance that is imposed between the victim wire and its neighbors and, $C_G$ is the coupling capacitance between substrate and plate.

Based on the Eq. (1), we can model the transmission delay by the Eq. (2):

$$\tau = (1 + \rho \lambda) \pi_o$$

Where $\rho$ is the coupling coefficient of adjacent wires, $\lambda$ is the coupling capacitance to substrate capacitance ratio ($C_c/C_G$) and $\pi_o$ is the delay of a wire in the ideal channel, i.e., a channel without any coupling effect such as capacitance and inductance. For instance, when the both aggressors and the victim wire, switch in opposite directions a delay equal to $(1 + 4 \lambda) \pi_o$ will be imposed to the channel.

Similar to the 2D IC crosstalk model, we can drive a delay model for TSVs. Akin to previous studies [4, 17] and based on TSV’s inherent properties, a square model of 9 adjacent TSVs is considered. Fig. 2 depicts 9 neighbor TSVs from top view. We discuss the crosstalk effect on the victim TSV (specified by red in Fig. 2) and we model coupling capacitance noise that is emanated from its neighbor TSVs. Direct neighbors (i.e. north, south, west, and east) are closer to the victim, and thus their coupling capacitances are more destructive than the coupling effects of diagonal neighbors (i.e. northeast, northwest, southeast, and southwest). In order to model the effective capacitance on the victim TSV, we can extend the Eq. (1) to Eq. (3):

$$C_{eff} = C_G + \sum_{i=-2}^{2} C_{\alpha}|\frac{\Delta V_{I_0} - \Delta V_{I_{2i}}}{V_{dd}}|$$

$$+ \sum_{i=-1}^{2} C_{\beta}|\frac{\Delta V_{I_0} - \Delta V_{I_{2i-1}}}{V_{dd}}|$$

(3)

Where $C_{\alpha}$ represents coupling capacitance between a direct aggressor and the victim and $C_{\beta}$ is coupling capacitance between diagonal aggressor and the victim. Similar to 2D crosstalk delay model, based on Eq. (3) we can extend the Eq. (2) to model 3D TSVs as follows:

$$\tau = (1 + \rho_1 \lambda_1 + \rho_2 \lambda_2) \pi_o$$

(4)

Where $\rho_1$ is the coupling coefficient of the direct aggressors, $\lambda_1$ is the direct coupling capacitance to substrate capacitance ratio ($C_{\alpha}/C_G$), $\rho_2$ is the coupling coefficient of the diagonal aggressors, and $\lambda_2$ is the diagonal coupling capacitance to substrate capacitance ratio ($C_{\beta}/C_G$). $\rho_1$ and $\rho_2$ indicate how the changes in aggressors voltages affect the crosstalk on the victim. For instance, if a direct neighbor switches in opposite direction, $\rho_1$ would increase by two. In the worst case, all the neighbours switch from $V_{dd}$ to zero and the victim switches from zero to $V_{dd}$. In this case the
transmission delay would be \((1 + 8\lambda_1 + 8\lambda_2)\pi_o\).

\[
C_{\text{eff}} = \left[(C_\alpha + C_\beta) \times 8\right] + C_G
= [1.5C_\beta + C_\beta \times 8] + C_G
= 20 \times C_\beta + C_G \tag{5}
\]

As reported in [4, 27] the \(\lambda_1 = 5.54\) and \(\lambda_2 = 3.92\). For the sake of simplicity, we assume \(\lambda_1 = 1.5\lambda_2\) and consequently \(C_\alpha = 1.5C_\beta\), thus as Eq. (5) shows, we can classify crosstalk patterns in 40 distinct classes which represented in Table. 1. Indeed, patterns with higher class numbers have higher crosstalk noise and delay.

### 4 Proposed Mechanism

#### 4.1 Overview

As mentioned in Section 3, we have classified the patterns into 40 different classes based on their crosstalk effects. In this section, we propose 3DCAM mechanism which aims to minimize crosstalk effect on signal integrity and performance. To this end, we need to minimize the occurrences of higher crosstalk classes and maximize the occurrences of lower crosstalk classes. To accomplish which, we have to change the transition patterns on TSVs. As we know about the transmission line, one of the following conditions can occur to a single wire:

- \(0 \rightarrow 1\),
- \(1 \rightarrow 0\),
- \(0 \rightarrow 0\),
- \(1 \rightarrow 1\).

The motivation behind this work is the fact that retaining the previous value of a victim TSV can significantly affect the transmission’s crosstalk class.

Table 2 presents some examples, in which retaining the victim (middle) TSVs significantly reduces crosstalk class. The first column of this table is the incoming pattern in which the victim TSV could have transition and the second column shows the same pattern except that the victim’s transition is eliminated. The up and down arrows show zero to \(V_{dd}\) and \(V_{dd}\) to zero transitions respectively, and dashes (‘-‘) denote no transition on TSVs. The changes in crosstalk classes are represented in third column of this table. For instance, the first row of Table 2 shows the case that falls into crosstalk class of \(24C\) because the victim has three direct neighbors with opposite directions (\(C_{eff}\) increased by \(3 \times 2 \times 1.5C_\beta\)), a direct neighbor without transition (\(C_{eff}\) increased by \(1 \times 1 \times 1.5C_\beta\)), two diagonal neighbors with same direction transitions (impose no crosstalk) and two diagonal neighbors with no transitions (\(C_{eff}\) increased by \(2 \times 1 \times 1C_\beta\)). So the \(C_{eff}\) will be \(C_G + 12.5C_\beta\) and according to Table 1 the pattern falls into 24C class. By similar manner the crosstalk class after eliminating the victim’s transition would be 12C. As depicts in this table, the crosstalk minimization achieved by this simple modification is considerable.

#### 4.2 Control TSVs

In order to retain victim TSV’s value, 3DCAM should by some means inform the receiver side decoder that the victim’s transition has been eliminated. Thus, 3DCAM reserves some TSVs for this purpose. These control TSVs only switch
Table 2: Motivational Example

| Pattern | Pattern* | Crosstalk Reduction |
|---------|----------|---------------------|
| ↓ ↓ ↓ | ↓ ↓ ↓ | 5C → 19C |
| ↑ ↓ ↓ | ↑ – ↓ | 5C → 19C |

when the value of their corresponding victim TSVs are not valid (i.e. the 3DCAM eliminates their transitions). Fig. 5 demonstrates the layout of these control TSVs for a $3 \times N$ link. The middle TSVs of every $3 \times 3$ cluster (including overlapping ones) have a control TSV through which 3DCAM coder informs decoder that the value of the TSV is valid or not. Since the control TSVs may have coupling between themselves, we can repeat the technique and apply 3DCAM on them.

4.3 Switch Threshold

Retaining the victim’s value is not always beneficial to crosstalk class. In the cases that the original transitions are good enough, retaining the victim’s value may result in a worse crosstalk class. In addition, it has negative impact on control TSVs, considering the fact that retaining a value requires a transition in a control signal. Table 3 shows an example in which retaining the victim’s value leads to a worse crosstalk class and hence a worse transmission delay.

Table 3: Disruptive Retaining Example

| Pattern | Pattern* | Crosstalk Reduction |
|---------|----------|---------------------|
| ↓ ↓ ↓ | ↓ ↓ ↓ | 5C → 19C |

To address this issue, we introduce a parameter called Switch Threshold (ST). This parameter determines which patterns should be manipulated by 3DCAM. In the other words, 3DCAM retains the value of the victim TSV, only if the transitions of neighbour TSVs make a pattern which has a crosstalk class more than ST.

To find the optimal value for the ST parameter, we swept ST parameter from 0C to 39C and measured average transmission delay of several benchmarks. Fig. 6 depicts the results of this experiment. As this figure shows, the average delay is minimum when the ST is set to 20. These results are also consistent with the intuition, seeing that setting ST to 20 bisects the crosstalk classes.

4.4 CODEC Design

Fig. 4 and Fig. 5 illustrate the structure of 3DCAM coder and decoder. In order to send 9 bits of data ($D_0$ - $D_8$) from die $X$ to die $Y$, the data have to be delivered to the coder which has been placed in die $X$. After that, the coder evaluates the crosstalk class which will be imposed to the victim TSV ($I_0$). Then it checks whether the crosstalk class is greater
than the ST parameter, in which case, the coder eliminates the victim’s transition and flips the control bit. Next, the data and control bit are sent to the die \( Y \) through TSVs. At the die \( Y \), decoder receives the data and control signals. Then based on the control signal, the decoder determines the original value of the victim TSV. It is noteworthy that due to straightforward functionality of the 3DCAM coder and decoder, they can be implemented by simple circuits.

### 4.5 TSV Overhead

Because of the controlling mechanism, we have to reserve an extra TSV for each cluster including 9 TSVs. As a result, 3DCAM suffers from about 30% TSV overhead. Fig. 7 demonstrates the TSV overhead of proposed method, ShieldUS, and 3DLAT \((\omega = 4)\). As Fig. 7 depicts, the TSV overhead of 3DLAT is about 80% and ShieldUS imposed no TSV overhead to the circuit because it only shuffles and remaps the data. However, ShieldUS needs a considerable \( 9 \times 9 \) crossbar which is used to remap data to TSVs.

### 5 Evaluation

In this section, the proposed mechanism is evaluated and compared with two 3D crosstalk reduction schemes, 3DLAT [27] \((\omega = 4)\) and ShieldUS [4] \((\text{interval} = 100)\). Based on the crosstalk model that proposed in Section 3, we measured the amount of crosstalk reduction and average delay on real traces which are taken from SPEC2006 benchmark suite [13]. We used gem5 simulator [3] to capture the transitions of memory data bus of gcc, mcf, namd, soplex, h264, omnetpp, xalancbmk, perlbench2, bwaves, cactusADM, dealII, ibm, and aster benchmarks.

Without loss of generality, we assume that the TSVs are arranged in \( 3 \times N \) layout. Also, we suppose that the data bitwidth is 64 and thus we need eight \( 3 \times 3 \) TSV clusters for the data and three clusters for control lines.

#### 5.1 Delay Analysis

Fig. 8 demonstrates the transmission delay for several benchmarks from SPEC2006 suite. The delays are normalized to the case that no crosstalk minimization technique is used. As Fig. 8 represents, 3DCAM can reduce the transmission delay of benchmarks by 9% compared to the base uncoded case and in the best case 3DCAM could reduce transmission delay of soplex benchmark by 25.7% compared to 3DLAT method. Since 3DLAT \((\omega = 4)\) tries to code the input data in the manner that the coded output has no crosstalk class higher than 23C (based on our model), it can have a destructive effect on the transmissions time with lower crosstalk class. As the most transitions of soplex benchmark
fall into lower crosstalk classes, which is less than the average crosstalk class of 3DLAT coded outputs. 3DLAT even increases the transmission delay of this benchmark. ShieldUS also could not effectively reduce the delay of experimented benchmarks. Inasmuch as this method can only reduce transmission delay of benchmarks with highly regular data and signals.

5.2 Crosstalk Class Frequency Analysis

As the occurrence frequency of higher crosstalk classes directly affects the signal integrity and transmission time, the frequency of crosstalk classes is measured before and after applying the 3DCAM mechanism. Fig. 9 and Fig. 10 show the occurrence frequency of crosstalk classes before and after applying the 3DCAM mechanism, respectively. As these figures show, 3DCAM causes most of crosstalk patterns to fall into the left side of the chart. Namely it pushes the higher crosstalk classes to the lower crosstalk classes.

5.3 Area Overhead

As mentioned in Section 4, 3DCAM uses a simple coder which leads to less area overhead compared to all previous works. Table 3 demonstrates the coder and decoder area overhead of ShieldUS, 3DLAT, and 3DCAM mechanisms. For $3 \times 3$ TSV cluster in 3DLAT, the area of coder and decoder is $4264 \mu m^2$ due to its large comparators. We estimate
ShieldUS area overhead with the area of a $9 \times 9$ crossbar which is $218 \mu m^2$. Finally, the area of 3DCAM is $116 \mu m^2$. These mechanisms are implemented and synthesized with 45nm technology using Synopsys Design Compiler.

| Mechanism     | Area ($\mu m^2$) |
|---------------|------------------|
| ShieldUS (only) | 218              |
| 3DLAT         | 4264             |
| 3DCAM         | 116              |

6 Conclusion

In this paper, a crosstalk avoidance mechanism for TSV-to-TSV coupling capacitance is presented and a different crosstalk model has been discussed. The proposed mechanism decides about sending original data or retaining the TSV value in previous state based on a switch threshold (ST) parameter. 3DCAM reduces the frequency of higher crosstalk patterns which leads to reduce the interconnection delay. As compared to previous work, 3DCAM imposed negligible area overhead. GEM5 simulator is used to extract transitions of the data bus. We used real benchmarks taken from
With capacitance coupling effect. Second, presenting a probability model for each crosstalk classes in TSVs is another task for authors. Third, developing an analytical reliability model for TSV-to-TSV coupling effect in 3D ICs is going to be discussed in the future work.

In our future work, first, we plan to consider a comprehensive crosstalk model based on capacitance and inductance coupling effects. Since the inductive coupling effect will increase in the near future, it has to be considered in conjunction with capacitance coupling effect. Second, presenting a probability model for each crosstalk classes in TSVs is another task for authors. Third, developing an analytical reliability model for TSV-to-TSV coupling effect in 3D ICs is going to be discussed in the future work.

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References

[1] K. Agarwal, M. Agarwal, D. Sylvester, and D. Blaauw. Statistical interconnect metrics for physical-design optimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 25(7):1273–1288, 2006.

[2] C. J. Akl and M. a. Bayoumi. Reducing interconnect delay uncertainty via hybrid polarity repeater insertion. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 16(9):1230–1239, 2008.

[3] N. Binkert, B. Beckmann, G. Black, S. K. Reinhardt, A. Saidi, A. Basu, J. Hestness, D. R. Hower, T. Krishna, S. Sardashti, et al. The gem5 simulator. ACM SIGARCH Computer Architecture News, 39(2):1–7, 2011.

[4] Y. Y. Chang, Y. S. C. Huang, V. Narayanan, and C. T. King. ShieldUS: A novel design of dynamic shielding for eliminating 3D TSV crosstalk coupling noise. Proceedings of the Asia and South Pacific Design Automation Conference, ASP-DAC, pages 675–680, 2013.

[5] C. Duan, V. H. Cordero Calle, and S. P. Khatri. Efficient on-chip crosstalk avoidance CODEC design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 17(4):551–560, 2009.

[6] A. Eghbal, P. M. Yaghini, N. Bagherzadeh, and M. Khayamhasti. Tsv analytical fault tolerance assessment for 3d network-on-chip. Computers, IEEE Transactions on, PP(99):1–1, 2015.

[7] A. Eghbal, P. Yaghini, S. Yazdi, and N. Bagherzadeh. Tsv-to-tsv inductive coupling-aware coding scheme for 3d network-on-chip. In Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), 2014 IEEE International Symposium on, pages 92–97, Oct 2014.
[8] A. Engin and S. Narasimhan. Modeling of crosstalk in through silicon vias. *Electromagnetic Compatibility, IEEE Transactions on*, 55(1):149–158, Feb 2013.

[9] H. Farrokhbakht, H. M. Kamali, and S. Hessabi. Smart: A scalable mapping and routing technique for power-gating in noc routers. In *Proceedings of the Eleventh IEEE/ACM International Symposium on Networks-on-Chip, NOCS ’17*, pages 15:1–15:8, New York, NY, USA, 2017. ACM.

[10] H. Farrokhbakht, M. Taram, B. Khaleghi, and S. Hessabi. Toot: an efficient and scalable power-gating method for noc routers. In *2016 Tenth IEEE/ACM International Symposium on Networks-on-Chip (NOCS)*, pages 1–8, Aug 2016.

[11] A. Ganguly, P. Pande, and B. Belzer. Crosstalk-aware channel coding schemes for energy efficient and reliable noc interconnects. *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, 17(11):1626–1639, Nov 2009.

[12] A. Ganguly, P. P. Pande, B. Belzer, and C. Grecu. Design of low power & reliable networks on chip through joint crosstalk avoidance and multiple error correction coding. *Journal of Electronic Testing*, 24(1-3):67–81, 2008.

[13] J. L. Henning. Spec cpu2006 benchmark descriptions. *ACM SIGARCH Computer Architecture News*, 34(4):1–17, 2006.

[14] K. Hirose and H. Yasuura. A bus delay reduction technique considering crosstalk. In *Design, Automation and Test in Europe Conference and Exhibition 2000. Proceedings*, pages 441–445, 2000.

[15] S. Itr. ITRS 2012 Executive Summary. *ITRS*. [Online]. Available: http://www.itrs.net, 2012. Accessed: 2015-03-30.

[16] M. Jung, J. Mitra, D. Z. Pan, and S. K. Lim. Tsv stress-aware full-chip mechanical reliability analysis and optimization for 3d ic. *Commun. ACM*, 57(1):107–115, Jan. 2014.

[17] R. Kumar and S. P. Khatri. Crosstalk avoidance codes for 3d vlsi. In *Design, Automation Test in Europe Conference Exhibition (DATE)*, 2013, pages 1673–1678, March 2013.

[18] C. Liu, T. Song, J. Cho, J. Kim, J. Kim, and S. K. Lim. Full-chip tsv-to-tsv coupling analysis and optimization in 3d ic. In *Proceedings of the 48th Design Automation Conference*, DAC ’11, pages 783–788, New York, NY, USA, 2011. ACM.

[19] G. Loh. 3d-stacked memory architectures for multi-core processors. In *Computer Architecture, 2008. ISCA ’08. 35th International Symposium on*, pages 453–464, June 2008.

[20] R. Marculescu, U. Y. Ogras, L.-S. Peh, N. E. Jerger, and Y. Hoskote. Outstanding research problems in noc design: system, microarchitecture, and circuit perspectives. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 28(1):3–21, 2009.

[21] M. Motoyoshi. Through-silicon via (tsv). *Proceedings of the IEEE*, 97(1):43–48, Jan 2009.

[22] C. Okoro, J. W. Lau, F. Golshany, K. Hummler, and Y. S. Obeng. A detailed failure analysis examination of the effect of thermal cycling on Cu TSV reliability. *IEEE Transactions on Electron Devices*, 61(1):15–22, 2014.

[23] P. P. Pande, A. Ganguly, B. Feero, and C. Grecu. Applicability of energy efficient coding methodology to address signal integrity in 3D NoC fabrics. *Proceedings - IOLTS 2007 13th IEEE International On-Line Testing Symposium*, (Iolts):161–166, 2007.

[24] M. J. Sepúlveda, J. Diguet, M. Strum, and G. Gogniat. Noc-based protection for soc time-driven attacks. *IEEE Embedded Systems Letters*, 7(1):7–10, March 2015.

[25] S. R. Sridhara and N. R. Shanbhag. Coding for reliable on-chip buses: A class of fundamental bounds and practical codes. *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, 26(5):977–982, 2007.

[26] J. Z. J. Zhang and E. Friedman. Effect of shield insertion on reducing crosstalk noise between coupled interconnects. *2004 IEEE International Symposium on Circuits and Systems (IEEE Cat. No.04CH37512),* 2, 2004.

[27] Q. Zou, D. Niu, Y. Cao, and Y. Xie. 3dlat: Tsv-based 3d ics crosstalk minimization utilizing less adjacent transition code. *Proceedings of the Asia and South Pacific Design Automation Conference, ASP-DAC*, pages 762–767, 2014.