Highly Reliable Multiple-Valued One-Phase Signalling for an Asynchronous On-Chip Communication Link

Naoya ONIZAWA†a and Takahiro HANYU†b, Members

SUMMARY This paper presents highly reliable multiple-valued one-phase signalling for an asynchronous on-chip communication link under process, supply-voltage and temperature variations. New multiple-valued dual-rail encoding, where each code is represented by the minimum set of three values, makes it possible to perform asynchronous communication between modules with just two wires. Since an appropriate current level is individually assigned to the logic value, a sufficient dynamic range between adjacent current signals can be maintained in the proposed multiple-valued current-mode (MVCM) circuit, which improves the robustness against the process variation. Moreover, as the supply-voltage and the temperature variations in smaller dimensions of circuit elements are dominated as the common-mode variation, a local reference voltage signal according to the variations can be adaptively generated to compensate characteristic change of the MVCM-circuit component. As a result, the proposed asynchronous on-chip communication link is correctly operated in the operation range from 1.1 V to 1.4 V of the supply voltage and that from −50°C to 75°C under the process variation of 3σ. In fact, it is demonstrated by HSPICE simulation in a 0.13-μm CMOS process that the throughput of the proposed circuit is enhanced to 435% in comparison with that of the conventional 4-phase asynchronous communication circuit under a comparable energy dissipation.

key words: delay-insensitive, asynchronous circuits, multiple-valued current-mode (MVCM) circuits, Network-on-Chip (NoC), communication link

1. Introduction

With the recent technology node progress, many cores, such as processing cores, DSPs, and memories, are integrated on a single chip. Globally Asynchronous Locally Synchronously (GALS) [1], [2] Network-on-Chip (NoC) architecture [3] is one of the useful approaches for wide-bandwidth demands in large-scaled System-on-Chips (SoCs), and provides that multiple communications are simultaneously done over asynchronous routers and links between processing cores which are operated by different clock frequencies.

Although the asynchronous communication links have been proposed [4]–[8], a large number of wires and communication steps are required for an asynchronous handshake operation, where data is locally synchronized by using a request and an acknowledge signals. To reduce the overhead of the asynchronous operation, high-speed and wire-efficient asynchronous communication links based on one-phase signalling have been reported [9], [10]. In these links, the number of wires and communication steps are reduced to those in a synchronous communication link by utilizing multiple-valued encoding and multiple-valued current-mode (MVCM) circuits [11], [12]. However, variation effects, such as process, supply-voltage and temperature variations, have not been considered in the MVCM circuits, while in binary-CMOS circuits, the variation effects and their reduction techniques have been reported [13]–[15].

This paper presents highly reliable multiple-valued one-phase signalling for the asynchronous on-chip communication link under the process, the supply-voltage and the temperature variations. To implement a process-variation tolerant on-chip communication circuit, we propose two techniques to increase a dynamic range of the multi-level signal. First technique is a data-dependent multiple-valued encoding. In the proposed encoding, two kinds of request information with the data information is encoded by multiple-valued dual-rail codeword, and then is alternatively transmitted. Since the request information is encoded according to the data information, the request codeword is represented by the minimum set of three values, instead of four ones in the conventional independent multiple-valued encoding [9], [10], which increases the dynamic range of the multi-level signal. Second technique is a weighted current assignment of the logic value. In the multiple-valued one-phase signalling, an arrival of the asynchronous signals is recognized based on the request information. In the proposed current assignment, a large amount of current is assigned to the logic value in the request codeword in comparison with that in the data codeword, which increases current difference between two kinds of request information. Thus, the dynamic range of the multi-level signal in the request codeword is increased with respect to that in the conventional uniform current assignment. As a result, an enough dynamic range can be obtained for the correct asynchronous operation against the process variation.

The asynchronous on-chip communication circuits are designed by using supply-voltage and temperature-variation-aware MVCM-circuit components. To guarantee the characteristics of the MVCM-circuit components under the supply-voltage and the temperature variations, the MVCM-circuit components are controlled by reference voltage signals generated in reference voltage generators [16], where the MVCM-circuit components and the reference voltage generators are closely located. Since the supply-voltage and the temperature variations in smaller dimensions of circuit elements are dominated as the common-
mode variation, the reference voltage level can be adaptively changed to compensate the characteristic change of the MVCM-circuit components in accordance with the supply-voltage and the temperature variations.

As a result, the proposed asynchronous on-chip communication link is correctly operated in the operation range from 1.1 V to 1.4 V of the supply voltage and that from −50°C to 75°C under the process variation of 3σ. In fact, it is demonstrated by HSPICE simulation in a 0.13-μm CMOS process that the throughput of the proposed circuit is enhanced to 435% in comparison with that of the conventional 4-phase asynchronous communication circuit under a comparable energy dissipation.

2. Data-Dependent Multiple-Valued Dual-Rail Encoding

2.1 One-Phase Signalling

Figure 1 shows a channel model for the full-duplex asynchronous communication link based on the one-phase signalling. Although there is no difference between the two modules, for the purpose of explanation, one end is referred to as the primary and the other end as the secondary. It is assumed that the wires connected between the modules have bounded but unknown delays. In the one-phase signalling, A which includes data (Data_p) and request information (Req_p) is transmitted from the primary module, while B which includes data (Data_s) and request information (Req_s) is simultaneously transmitted from the secondary module. Then, C which includes both the data and the request information is returned to both the modules. Since the request information from the primary module can overlap with that from the secondary module, the handshaking can at best be completed within ‘one-way’ delay. In this sense, this protocol is called ‘one-phase signalling’.

2.2 Multiple-Valued Dual-Rail Encoding

The one-phase signalling is realized based on the multiple-valued dual-rail encoding shown in Table 1. The multiple-valued dual-rail codeword consists of data and request codeword. The data codeword signifies a logic value (0 or 1). The request codeword represents parity information (ODD or EVEN). In the conventional dual-rail encoding [9],[10], the data and the request information are independently encoded by the dual-rail codeword shown in Table 1 (a) and (b). In contrast, in the proposed data-dependent dual-rail encoding, the request information is encoded according to the data shown in Table 1 (c), while the data is encoded in a similar way as the conventional encoding.

Each module transmits the codeword represented by the sum of the data and the request codeword. The codeword transmitted from the primary and secondary modules are A(x_p, x'_p) and B(x_s, x'_s), respectively. The codeword C(x, x') is represented by the sum of two kinds of codeword A and B.

\[
A(x_p, x'_p) = (x_D, x'_D) + (x_R, x'_R)
\]
\[
B(x_s, x'_s) = (x_D, x'_D) + (x_R, x'_R)
\]
\[
C(x, x') = A(x_p, x'_p) + B(x_s, x'_s)
\]

Table 2 summarizes the three kinds of codeword in both the conventional and the proposed encoding. P-IN and S-IN are input data for the primary and the secondary interfaces, respectively. While P-REQ and S-REQ are request information for both the interfaces shown in Fig. 1.

The asynchronous communication based on the one-phase signalling is performed by detecting whether the mutual request information of the primary and the secondary modules is the same. The correspondence between the mutual request information can be detected by using the sum x + x' of the dual-rail codeword C. In the conventional dual-rail encoding, since the request information of EVEN is encoded by the dual-rail codeword (1,1) shown in Table 1 (b), x + x' becomes the maximum value of six when the mutual request information is EVEN.

In contrast, in the proposed dual-rail encoding, the request information of EVEN is encoded by the dual-rail codeword (0,1) or (1,0) according to the data information. Therefore, x + x' becomes the maximum value of four when the mutual request information is EVEN, while x + x' becomes the minimum value of two when the mutual request information is ODD. Otherwise, x + x' becomes an intermediate value of three. During the transition between ODD and EVEN, x + x' is monotonically increased or decreased between logic values of two and four. Therefore, the cor-

Table 1 Dual-rail codeword for (a) a logic value, (b) parity information in the conventional encoding and (c) parity information in the proposed encoding.

| Data     | (x_p, x'_p) |
|----------|-------------|
| “0”      | (0,1)       |
| “1”      | (1,0)       |

| Req      | (x_p, x'_p) |
|----------|-------------|
| EVEN     | (1,1)       |

| Req | Data     | (x_p, x'_p) |
|-----|----------|-------------|
| ODD | -        | (0,0)       |
| EVEN| “0”      | (0,1)       |
|     | “1”      | (1,0)       |
respondence between the mutual request information is performed by comparing \( x + x' \) with the logical threshold values 2.5 and 3.5. The data information is identified using a dual-rail codeword which is generated by subtracting own codeword \( A \) or \( B \) from the summed codeword \( C \) in each module.

Figure 2 shows a timing diagram of the one-phase signalling based on the proposed data-dependent dual-rail encoding. Initially, \( x + x' \) becomes the minimum value of two which means that the mutual request information is ODD. When the secondary module transmits the dual-rail codeword in the EVEN, \( x + x' \) becomes the intermediate value of three. Then, when the primary module transmits the dual-rail codeword of EVEN, \( x + x' \) becomes the maximum value of four that is detected by using the logical threshold value 3.5, which results in a completion of the asynchronous communication based on the one-phase signalling. In this way, the proposed dual-rail encoding makes it possible to reduce the maximum value of \( x + x' \) with maintaining the one-phase signalling for the asynchronous communication link.

3. Circuit Implementation Based on Weighted Current Assignment

The asynchronous communication link based on the multiple-valued dual-rail encoding is implemented by using the MVCM circuit. In this section, the overall structure of the proposed asynchronous communication interface based on a new current assignment of a logic value is described.

### 3.1 Overall Structure

Figure 3 shows a block diagram of the proposed asynchronous communication interfaces based on the multiple-valued dual-rail encoding. The structure is symmetric: both ends contain the same components; an encoder (EC), a state detector (SD), and a decoder (DC).

Figure 4 shows a circuit diagram of EC. The function of EC is to generate a multi-level dual-rail current signal corresponding to the multiple-valued dual-rail codeword shown in Table 2 (b). The input voltage signal \( P-IN \) (or \( S-IN \)) is converted to a dual-rail current signal \( (I_{xd}, I_{xd'}) \) corresponding to the dual-rail codeword of \( Data \), where logic values “0” and “1” of \( P-IN \) (or \( S-IN \)) assign to \( V_{SS} \) and \( V_{DD} \), respectively.

### Table 2

| Primary | Transmission lines | Secondary |
|---------|-------------------|-----------|
| P-REQ   | \( A(x_p, x'_p) \) | \( B(x_q, x'_q) \) | S-IN | S-REQ |
| ODD     | (0,1)             | (0,1)     | “0”  | ODD   |
| “0”     | (0,1)             | (1,0)     | “1”  | EVEN  |
| “1”     | (1,0)             | (0,1)     | “1”  | EVEN  |
| EVEN    | (2,1)             | (2,1)     | “1”  | EVEN  |
| “1”     | (2,1)             | (1,0)     | “0”  | EVEN  |

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### 3.6 Overall Structure

Figure 3 shows a block diagram of the proposed asynchronous communication interfaces based on the multiple-valued dual-rail encoding. The structure is symmetric: both ends contain the same components; an encoder (EC), a state detector (SD), and a decoder (DC).

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In contrast, a dual-rail current signal \((I_x, I_x')\) corresponding to the dual-rail codeword of Req is generated based on both the \(P-IN (S-IN)\) and \(P-REQ (S-REQ)\), where ODD and EVEN of \(P-REQ (S-REQ)\) assign to \(V_{SS}\) and \(V_{DD}\), respectively. Then, the \((I_{xd}, I_{xd'})\) and the \((I_{xr}, I_{xr'})\) are summed to generate \((I_{xp}, I_{xp'})\) by just wiring without any active devices because of Kirchoff’s Current Law. The dual-rail current signal \((I_x, I_x')\) is generated on the wires between the modules by the sum of \((I_{xp}, I_{xp'})\) and \((I_{xs}, I_{xs'})\), and then is returned to both the two modules.

Figure 5 shows a circuit diagram of SD which consists of current mirrors, I-V converters, voltage comparators and a C-element. The function of SD is to detect the correspondence between the mutual request information, such as ODD and EVEN. In the current mirror, the dual-rail current signal \((I_x, I_x')\) is copied to three kinds of dual-rail current signals. The two dual-rail current signals are summed to generate two current signals \(I_{xs',c}\), while the other one is used in DC. The two current signals \((I_{xs}, I_{xs'})\) are converted into the two voltage signals \(V_{xs, x'}\) by using two kinds of the I-V converters whose resistances are different. Then, the voltage signals \(V_{xs, x'}\) are compared with two logical threshold voltages \(V_{th25}\) and \(V_{th35}\), respectively in the voltage comparators which are designed by using a differential-pair circuit. The outputs \(TH25\) and \(TH35\) of the voltage comparators are inputs for the C-element. The C-element is a standard asynchronous storage element [17], whose output is low (high) when both inputs are low (high), and which otherwise holds its value. The output of the C-element is changed when the mutual request information is the same because \(x \neq x'\) becomes the maximum value of four or the minimum value of two.

Figure 6 shows a circuit diagram of DC. The current signals \(I_x\) and \(I_x'\) are used to decode Data in ODD and EVEN, respectively. As shown in Table 2 (b), there are the same two kinds of dual-rail codeword (1,1) or (2,2) in the ODD or EVEN, respectively when the mutual Data are different. To correctly decode Data, a current signal \(I_{IN}\) corresponding to a logic value of one is added to the \(I_x\) or \(I_x'\) according to the input data \(P-IN (S-IN)\) to distinguish the same dual-rail codeword (1,1) or (2,2) in both the interfaces. For example, when \(P-IN\) and \(S-IN\) are “1” and “0” in ODD, respectively, the dual-rail codeword (1,1) becomes (1,2) in DC of the primary interface, while one becomes (2,1) in DC of the secondary interface. Then, the summed current signals are converted into the voltage signals \(V_x\) and \(V_x'\) by using two kinds of I-V converters. The voltage signals \(V_x\) and \(V_x'\) are compared with two logical threshold voltages \(V_{ODD}\) and \(V_{EVEN}\) to generate \(OUT_{ODD}\) and \(OUT_{EVEN}\). The output data \(P-OUT (S-OUT)\) is selected by \(P-REQ (S-REQ)\) in a multiplexer.

### 3.2 Multi-Level Signal Detection Based on Weighted Current Assignment

Table 3 shows current assignments for the dual-rail codeword. In the conventional current assignment, two kinds of codeword for Data and Req assign to the same unit current \(I_u\). In sum, \(I_{ad} (I_{ad'})\) and \(I_{r} (I_{r'})\) are the same amount of current. Therefore, the current signal \(I_{xs',c}\) is changed in proportion to a logic value of the sum \(x + x'\) shown in Table 3 (a). \(V_{xs, x'}\) corresponding to \(I_{xs, x'}\) is compared with the logical threshold voltages \(V_{th25}\) and \(V_{th35}\) shown in Fig. 7 (a). The voltage level of \(V_{xs, x'}\) is limited by a supply voltage of 1.2 V, where the unit current \(I_u\) is 10 μA. Since the sum \(x + x'\) is just changed between logic values of two and four, \(I_{xs, x'}\) is also changed between 20 μA and 40 μA. Thus, each voltage swing \(\Delta V_{th25}\) and \(\Delta V_{th35}\) becomes small because an available voltage range of \(V_{xs, x'}\) is small, which may cause the wrong detection of the multi-level signal under the process variation.

To increase the available voltage range of \(V_{xs, x'}\), two kinds of codeword for Data and Req assign to the different amount of current. In the proposed weighted current assignment, the current signal \(I_{xs', c}\) is defined as Table 3 (b), where \(r\) is defined as a ratio of \(I_{xr} (I_{xr'})\) to \(I_{ad} (I_{ad'})\). When \(r\) is increased from one, the current signal \(I_{xs', c}\) corresponding...
to the logic value of three becomes large, while $I_{x+x'}$ corresponding to the logic values of one and two become small. Therefore, a range of $I_{x+x'}$ between two and four of $x + x'$ is increased in comparison with that in the conventional current assignment when $r$ is set to more than one. Figure 7 shows the characteristics of $V_{x+x'}$ when $r$ is four.

Moreover, an I-V converter with a reference voltage $V_{ref2}$ is used in the proposed SD. Since the resistance of the I-V converter becomes large at middle voltage level, the voltage swing of $V_{x+x'}$ becomes large at the logical threshold voltage levels $V_{th25}$ and $V_{th35}$. In contrast, in the conventional I-V converter, a gate of the I-V converter is connected to a ground. Thus, the resistance of the I-V converter becomes large at low voltage level, which leads to a small voltage swing of $V_{x+x'}$ at the logical threshold voltage levels $V_{th25}$ and $V_{th35}$. The characteristic of the I-V converter is described in details in Sect. 4.

As a result, each voltage swing $\Delta V_{th25}$ and $\Delta V_{th35}$ in SD based on the proposed weighted current assignment becomes large in comparison with that in SD based on conventional uniform current assignment, which improves the robustness against the process variation.

4. Multiple-Valued Current-Mode Circuit Components Based on Adaptive Reference Voltage Control

In this section, the MVCM-circuit components: the current source, the I-V converter and the voltage comparator are designed based on the adaptive reference voltage control for the robustness against the supply-voltage and the temperature variations. Each reference voltage generator is closely located at each MVCM-circuit component to compensate the characteristic change of the MVCM-circuit component. In the MVCM circuits, at most 2-bit information is superposed on a wire, while analog circuits use more than 6-bit information in general. Therefore, a few additional transistors are added to the MVCM-circuit components to roughly compensate the characteristics of the MVCM circuits for the correct operation.

In this paper, transient responses of the circuits due to the variations are not considered. The timing assumption of the proposed asynchronous circuit is almost the same as a quasi delay-insensitive (QDI) logic style [18]. Since the QDI logic style avoids any timing constraints with an only assumption, where the wires at a fan-out point must have roughly equal delay, the proposed asynchronous circuit is robust for the timing responses.

Figure 8 shows the proposed current source which is realized by a PMOS transistor $M1$ and an adaptive reference-voltage generator. The current $I_d$ is defined as
\[ I_a = \frac{\beta_1}{2}((V_{DD} - V_{ref1}) - |V_{thp}|)^2, \]  \hspace{1cm} (1)

where \( \beta_1 = \frac{W_i}{L_i} \mu_p C_{ox} \). \( \beta_i \) is the beta of the transistor \( M_i \) \( (1 \leq i \leq n) \). \( L_i \) and \( W_i \) are length and width of the transistor \( M_i \), respectively. \( C_{ox}, \mu_p \) and \( |V_{thp}| \) are the gate oxide capacitance per area, mobility and the threshold voltage of the PMOS transistor, respectively. Channel length modulation effect is ignored in the Eq. (1).

In the adaptive reference voltage generator, reference voltage \( V_{ref1} \) is generated for the current source. The reference voltage \( V_{ref1} \) is defined as

\[ V_{ref1} = V_{DD} - \sqrt{\beta_3 \beta_2 V_{refn} + \beta_3 V_{thn} - |V_{thp}|}, \]  \hspace{1cm} (2)

where \( \mu_n \) and \( V_{thn} \) are mobility and a threshold voltage of the NMOS transistor, respectively. As shown in the Eq. (2), \( V_{ref1} \) is positively proportional to \( V_{DD} \). Hence, \( (V_{DD} - V_{ref1}) \) becomes almost constant in the Eq. (1), which results in realization of the supply-voltage-tolerant current source.

Next, temperature dependence is considered in the current source. In the Eq. (1), \( \mu_p \) and \( |V_{thp}| \) have negative temperature coefficient. In the transistor in an active region, the current is strongly dependent on \( |V_{thp}| \). Therefore, the current \( I_a \) is positively proportional to temperature when the reference voltage \( V_{ref1} \) is constant.

To weaken temperature dependence of the current source, \( (V_{DD} - V_{ref1}) \) is required to change in negatively proportion to temperature for compensating the \( |V_{thp}| \) variation. In the proposed current source, the reference voltage \( V_{ref1} \) is dependent on \( V_{refn} \) and \( |V_{thp}| \) shown in the Eq. (2), while coefficient of \( \mu_p \) and \( \mu_n \) in \( \beta_2 \) and \( \beta_3 \), respectively are ignored. By adjusting the transistor sizes as \( \beta_2 > \beta_3 \), the reference voltage \( V_{ref1} \) is strongly dependent on \( |V_{thp}| \). The temperature dependence of \( V_{ref1} \) is approximately defined as

\[ \frac{\partial V_{ref1}}{\partial T} \approx \frac{-\partial |V_{thp}|}{\partial T}. \]  \hspace{1cm} (3)

Therefore, \( V_{ref1} \) is positively proportional to temperature because of negative temperature coefficient of \( |V_{thp}| \). Since \( (V_{DD} - V_{ref1} - |V_{thp}|) \) becomes almost constant in the Eq. (1) under the temperature variation, the proposed current source becomes weak dependence of temperature.

Figure 9 shows the circuit diagram of the proposed I-V converter. The proposed I-V converter is composed of a PMOS transistor \( M_1 \), the adaptive reference-voltage generator and a voltage-level shift circuit. The adaptive reference-voltage generator is the same as that used in the proposed current source. In a region of \( (V_{DD} - V_x) \ll 2(V_{DD} - V_{ref2} - |V_{thp}|) \), the voltage \( V_x \) is defined as

\[ V_x = V_{DD} - \frac{1}{\beta_1(V_{DD} - V_{ref2} - |V_{thp}|)} I_x \]  \hspace{1cm} (4)

\[ = V_{DD} - R_I I_x. \]  \hspace{1cm} (5)

Using the adaptive reference-voltage generator, the reference voltage \( V_{ref1} \) is adaptively changed in positively proportion to \( V_{DD} \) shown in the Eq. (2). Then, the reference voltage \( V_{ref1} \) is lowered to the reference voltage \( V_{ref2} \) using the voltage-level shift circuit which is composed of two NMOS transistors \( M_4 \) and \( M_5 \), because a low-voltage level is required for the I-V converter to operate the transistor \( M_1 \) in the linear region at high voltage level of \( V_x \). The reference voltage \( V_{ref2} \) is defined as

\[ V_{ref2} = V_{ref1} - \sqrt{\frac{\beta_3}{\beta_4} V_{refn} + \frac{\beta_3}{\beta_4} V_{thn} - V_{thn}}. \]  \hspace{1cm} (6)

As shown in the Eqs. (2) and (6), \( V_{ref2} \) is positively proportional to \( V_{DD} \). Therefore, the resistance \( R_I \) of the I-V converter becomes almost constant under the supply-voltage variation in the proposed I-V converter, because \( (V_{DD} - V_{ref2}) \) becomes almost constant in the Eq. (4).

On the other hand, a voltage level of \( V_x \) is shifted in accordance with \( V_{DD} \) variation shown in the Eq. (5). Moreover, the proposed I-V converter is sensitive to the temperature variation because \( V_{ref1} \) is positively proportional to temperature in the Eq. (3). The ratio \( \frac{\beta_3}{\beta_4} \) is set to about 1 to set \( V_{ref2} \) to low voltage level shown in Fig. 7. Therefore, temperature dependence of \( V_{ref2} \) is approximately defined as

\[ \frac{\partial V_{ref2}}{\partial T} \approx \frac{-\partial V_{ref1}}{\partial T}. \]  \hspace{1cm} (7)

Since \( V_x \) is dependent on only \( \beta_1 \) shown in the Eq. (4). \( V_x \) is negative proportional to temperature. The characteristic change due to the supply-voltage and the temperature variations are compensated in the comparator stage.

Figure 10 shows circuit diagram of the proposed voltage comparator. In the comparator, the converted voltage
V_t is compared with the logical threshold voltage V_T. The output voltage V_out in the comparator is determined as
\[ V_{out} = \begin{cases} 
\text{High} & (\text{if } V_t > V_T) \\
\text{Low} & (\text{if } V_t < V_T) 
\end{cases} \] (8)
The reference voltage V_ref2 is generated in the proposed I-V converter shown in Fig. 9. Since the transistors M1 and M2 are operated in the active region, the logical threshold voltage V_T is defined as
\[ V_T = V_{DD} - |V_{thp}| - \sqrt{K_3 - K_1}, \] (9)
where \( K_3 = \frac{\beta_3}{R_L} (V_{refn} - V_{thn})^2 \) and \( K_1 = \frac{\beta_1}{R_L} (V_{DD} - V_{ref2} - |V_{thp}|)^2 \). Since V_ref2 is positively proportional to V_DD shown in the Eqs. (2) and (6), V_T is also positively proportional to V_DD as same as the input voltage V_t shown in the Eq. (5) because \((V_{DD} - V_{ref2})\) in the K_1 becomes almost constant. Therefore, the comparison operation which recognizes the multi-level signal V_t can be correctly done under the supply-voltage variation in the proposed comparator.

In addition, V_T is temperature dependence because |V_thp|, V_thn and V_ref2 are changed in accordance with the temperature variation. By adjusting transistor sizes as \( \beta_3 > \beta_2 \) in the K_3, V_T is changed in negatively proportion to temperature because K_3 is positively proportional to temperature due to negative temperature coefficient of V_thn. Moreover, the transistor M1 is operated in the different regions due to the voltage level of V_ref2. When V_ref2 is increased in positively proportional to temperature, M1 is operated in the linear region, which becomes a large resistance of M1. Therefore, V_T is strongly changed in negatively proportion to temperature. As a result, the characteristic change of the resistance R_1 in the proposed I-V converter due to the temperature variation is compensated in the proposed comparator, which results in the correct comparison operation under the temperature variation.

5. Evaluation
In this section, we evaluate three types of the proposed asynchronous communication circuits with the conventional one[9],[10] based on the multiple-valued one-phase signalling shown in Table 4. The performances are evaluated by HSPICE simulation under a 0.13-μm CMOS technology. The wire length is set to 1 mm between the primary and the secondary interfaces shown in Fig. 11. The parameters of a wire are R_w = 94 Ω/mm, and C_w = 102 fF/mm. Normally, a condition of V_DD = 1.2 V and 25°C is used. In the proposed A circuit, the data-dependent multiple-valued dual-rail encoding is used. In the proposed B circuit, the weighted current assignment based on the data-dependent multiple-valued dual-rail encoding is used. In the proposed C circuit, the proposed B circuit components are designed based on the adaptive reference voltage control.

5.1 Performance Dependency on the Current Assignment
Figure 12 shows throughput and energy dissipation of the proposed B circuit based on the weighted current assignment according to the ratio r. When the ratio r is increased, ΔV_th25 and ΔV_th35 become large because of a large range of I_{x \rightarrow x'}, which results in a high-speed detection in the voltage comparators of SD. Moreover, since the dual-rail current signal(I_w, I_{x'}) on the wires in ODD of the request information becomes small shown in Table 3 at the large ratio r, power dissipation on the wires is reduced. On the other hand, when the ratio r is large, the small amount of current on the wires in ODD of the request information is required to copy to the large amount of current by using the current mirrors of SD for maintaining the speed of the I-V converter. As a result, the ratio r of four makes it possible to realize the highest throughput and the lowest energy dissipation. We select the ratio r of four for the proposed B and proposed C circuits.

5.2 Characteristics of the MVCM-Circuit Components under the Supply-Voltage and the Temperature Variations
Figure 13 shows the characteristics of the current sources when V_DD is changed from 1.0 V to 1.4 V at 25°C without and with the reference voltage generator, where 10 μA current signals are generated. In the current source without the reference voltage generator, since the current I_a is

| Table 4 | Four asynchronous communication circuits based on the multiple-valued one-phase signalling. |
| --- | --- |
| | Conventional | Proposed |
| | A | B | C |
| Data-dependent encoding | X | O | O |
| Weighted current assignment | X | X | O |
| Adaptive reference voltage control | X | X | O |

Fig. 11 Wire model.

Fig. 12 Throughput and energy dissipation when the ratio r is changed from one to five.
Fig. 13 Characteristics of current sources when $V_{DD}$ is changed from 1.0 V to 1.4 V at 25°C: (a) without and (b) with the reference voltage generator.

Fig. 14 Characteristics of current sources when temperature is changed from $-40^\circ$C to $125^\circ$C at $V_{DD} = 1.2$ V: (a) without and (b) with the reference voltage generator.

positively proportional to $V_{DD}$ squared shown in the Eq. (1), the amount of current is widely changed under the supply-voltage variation because of the constant reference voltage $V_{ref1}$, which results in the 30.5 $\mu$A current variation. In contrast, since the reference voltage $V_{ref1}$ is changed in positively proportion to $V_{DD}$, $(V_{DD} - V_{ref1})$ becomes almost constant in the proposed C current source with the reference voltage generator. Therefore, the amount of the current variation with the reference voltage generator becomes 0.7 $\mu$A and can be reduced to 2.3% in comparison with that without the reference voltage generator under the supply-voltage variation.

Figure 14 shows the characteristics of the current sources when temperature is changed from $-40^\circ$C to $125^\circ$C at $V_{DD} = 1.2$ V. In the current source without the reference voltage generator, the current $I_{c}$ is strongly changed depending on temperature, because the threshold voltage $|V_{thp}|$ has negative temperature coefficient in the Eq. (1). In contrast, in the current source with the reference voltage generator, the reference voltage $V_{ref1}$ is positively proportional to temperature by adjusting the $\beta$ ratio in the Eq. (3). Therefore, the current $I_{c}$ becomes weak dependence of temperature in the current source with the reference voltage generator. As a result, the amount of the current variation in the proposed C circuit becomes 0.2 $\mu$A and can be reduced to 4.1% in comparison with that without the reference voltage generator under the temperature variation.

Figure 15 shows the characteristics of the I-V converter with the constant logical threshold voltage $V_{th35}$ in SD of the proposed B circuit when $V_{DD}$ are 1.05 V, 1.2 V and 1.35 V at 25°C. In the I-V converter without the reference voltage generator, since the resistance $R_{1}$ is positively proportional to $V_{DD}$ shown in the Eq. (4), the characteristic of the I-V converter is greatly changed due to the supply-voltage variation. Therefore, cross-points between $V_{x} + x'$ and $V_{th35}$ at $V_{DD} = 1.05$ V and 1.35 V are widely changed from that at $V_{DD} = 1.2$ V. As a result, the multi-level signal $I_{x} + x'$ cannot be correctly recognized under the supply-voltage variation without the reference voltage generator.

Figure 16 shows the characteristics of the I-V converter with the reference voltage generator and the logical threshold voltage $V_{th35}$ in SD of the proposed C circuit when $V_{DD}$ are 1.05 V, 1.2 V and 1.35 V at 25°C. In the I-V converter with the reference voltage generator, $R_{1}$ of the I-V converter becomes almost constant using the reference voltage $V_{ref2}$ because $V_{ref2}$ is positively proportional to $V_{DD}$ shown in the Eqs. (2) and (6). In contrast, a voltage level of $V_{x} + x'$ is shifted in accordance with the $V_{DD}$ variation. To recognize the multi-level current signal $I_{x} + x'$ correctly, the logical threshold voltage $V_{th35}$ is changed in positively proportion to
Fig. 17 Characteristics of the I-V converter and the logical threshold voltage $V_T$ in SD of the proposed C circuit at $-40^\circ C$, $25^\circ C$ and $125^\circ C$ when $V_{DD}$ is 1.2 V.

$V_{DD}$. As a result, the multi-level current signal $I_{x+x'}$ can be recognized within at most 1.3 $\mu$A variation under the supply-voltage variation in SD of the proposed C circuit.

Figure 17 shows the characteristics of the I-V converter with the reference voltage generator and the logical threshold voltage $V_{th35}$ in SD of the proposed C circuit at $-40^\circ C$, $25^\circ C$ and $125^\circ C$ when $V_{DD}$ is 1.2 V. $V_{x+x'}$ is negatively proportional to temperature because the resistance $R_1$ of the I-V converter with the reference voltage generator is positively proportional to temperature shown in the Eq. (4). In contrast, $V_{th35}$ is also changed in negatively proportion to temperature to compensate the $R_1$ variation. As a result, the multi-level current $I_{x+x'}$ can be recognized within at most 1.3 $\mu$A variation under the temperature variation in SD of the proposed C circuit.

Table 5 summarizes shmoo plots of the conventional, the proposed A, the proposed B and the proposed C circuits under the supply-voltage and temperature variations. In the conventional, the proposed A and the proposed B circuits, where the reference voltage generators are not used, it is correctly operated under a small number of points around the supply voltage of 1.2 V because the multi-level current-signal cannot be correctly recognized. In contrast, the proposed C circuit can be correctly operated in the operation range from the supply voltage of 1.1 V to 1.4 V under the temperature range between $-50^\circ C$ and $75^\circ C$.

5.3 Performance Comparison

Table 6 shows the performances of the four asynchronous communication circuits based on the multiple-valued dual-rail encoding in a full-duplex channel. All circuits are evaluated under the process variation through Monte-Carlo simulations of 1000, where the process variation of 3$\sigma$ in the Silterra 0.13-$\mu$m CMOS technology is used. The supply-voltage is changed from 1.1 V to 1.3 V, while temperature is changed from $-25^\circ C$ to $75^\circ C$.

The conventional circuit is not correctly operated under the process variation because the voltage swing of a logic value on $V_{x+x'}$ becomes small due to the maximum value of six in $x+x'$. Although the maximum value in $x+x'$ is reduced to four, the proposed A circuit is not correctly operated under the process variation because the voltage swing of a logic value on $V_{x+x'}$ is not large enough. In contrast,
the proposed B circuit can be correctly operated under the process variation because the voltage swing of a logic value on $V_{重}$ is large enough. The throughput of the proposed B circuit is enhanced by 27% due to the high-speed detection of $V_{重}$ in SD, while the energy dissipation is reduced by 28% due to a small amount of current on the wires in ODD of the request information in comparison with those of the conventional circuit. To utilize the adaptive reference voltage control, the proposed C circuit can be correctly operated under the process, the supply-voltage and the temperature variations, while the energy dissipation is increased by 31% with respect to that of the proposed B circuit due to the additional circuits which are the reference voltage generators. As a result, the highly reliable asynchronous communication circuit is realized under the variations with maintaining the same energy dissipation of the conventional one.

The performance of the proposed circuit (proposed C) is evaluated with the traditional 4-phase asynchronous communication link based on CMOS circuit implementation [18] in a full-duplex channel as shown in Table 7. The robust proposed circuit makes it possible to enhance the throughput to 435% in comparison with that of the 4-phase circuit under a comparable energy dissipation.

### Table 7 Performance comparisons between traditional 4-phase and the proposed (proposed C) asynchronous communication circuits

| Circuit   | Throughput [Gbps/wire] | Energy [fJ/bit] | # wires | Robustness |
|-----------|------------------------|-----------------|---------|------------|
| 4-phase   | 0.168                  | 765             | 6       | O          |
| Proposed  | 0.730                  | 722             | 2       | O          |

6. Conclusion

The high-performance asynchronous communication link based on highly reliable multiple-valued one-phase signalling has been presented. The dynamic range of a logic value is enhanced by the proposed multiple-valued dual-rail encoding and the current assignment for robustness against the process variation. The characteristics of the MVMC-circuit components become robust against the supply-voltage and the temperature variations based on the adaptive reference voltage control. As a result, the proposed asynchronous communication circuit is correctly operated in the operation range from 1.1V to 1.4V of the supply voltage and that from −50°C to 75°C under the process variation. In fact, it is demonstrated by HSPICE simulation in a 0.13-µm CMOS that the throughput of the proposed circuit is enhanced to 435% in comparison with that of the conventional 4-phase asynchronous communication circuit under a comparable energy dissipation.

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References

[1] D.M. Chapiro, Globally-asynchronous locally-synchronous systmes, Ph.D. dissertation, Stanford University, Stanford, CA, Oct. 1984.
[2] D. Lattard, E. Beigne, P. Clermidy, Y. Durand, R. Lemaire, P. Vivet, and F. Berens, “A reconfigurable baseband platform based on an asynchronous network-on-chip,” IEEE J. Solid-State Circuits, vol.43, no.1, pp.223–235, Jan. 2008.
[3] L. Benini and G. De Micheli, “Networks on chips: A new SoC paradigm,” IEEE Trans. Comput., vol.35, no.1, pp.70–78, Jan. 2002.
[4] W.J. Bainbridge and S.B. Furber, “Delay insensitive system-on-chip interconnect using 1-of-4 data encoding,” Proc. 7th IEEE Int. Symp. Asynchronous Circuits and Systems, pp.74–82, March 2001.
[5] E. Nigussie, T. Lehtonen, S. Tuuna, J. Plosila, and J. Isoaho, “High-performance long NoC link using delay-insensitive current-mode signaling,” VLSI Design, vol.2007, Article ID 46514.
[6] E. Nigussie, T. Plosila, and J. Isoaho, “Current mode on-chip interconnect using level-encoded two-phase dual-rail encoding,” Proc. IEEE Int. Symp. Circuits and Systems, pp.649–652, May 2007.
[7] P.B. McGee, M.Y. Agyeekum, M.A. Mohamed, and S.M. Nowick, “A level-encoded transition signaling protocol for high-throughput asynchronous global communication,” Proc. 14th IEEE Int. Symp. Asynchronous Circuits and Systems, pp.116–127, April 2008.
[8] Y. Ohtake, N. Onizawa, and T. Hanyu, “High-performance asynchronous intra-chip communication link based on a multiple-valued current-mode single-track scheme,” Proc. IEEE Int. Symp. Circuits and Systems, pp.1000–1003, Taipie, Taiwan, May 2009.
[9] T. Takahashi and T. Hanyu, “Implementation of a high-speed asynchronous data-transfer chip based on multiple-valued current-signal multiplexing,” IEICE Trans. Electron., vol.E89-C, no.11, pp.1598–1604, Nov. 2006.
[10] K. Mizusawa, N. Onizawa, and T. Hanyu, “Power-aware asynchronous peer-to-peer duplex communication system based on multiple-valued one-phase signaling,” IEICE Trans. Electron., vol.E91-C, no.4, pp.581–588, April 2008.
[11] A. Mochizuki and T. Hanyu, “A 1.88 ns 54 × 54-bit multiplier in 0.18-µm CMOS based on multiple-valued differential-pair circuitry,” 2005 IEEE Symp. VLSI Circuits, Dig. Tech. Papers, pp.264–267, June 2005.
[12] N. Onizawa, T. Hanyu, and V.C. Gaudet, “High-throughput bit-serial LDPC decoder LSI based on multiple-valued asynchronous interleaving,” IEICE Trans. Electron., vol.E92-C, no.6, pp.867–874, June 2009.
[13] S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi, and V. De, “Parameter variation and impact on circuits and microarchitectures,” Proc. 40th IEEE/ACM Int. Design Automation Conference, pp.338–342, June 2003.
[14] R. Kumar and V. Kusun, “Impact of temperature fluctuations on circuit characteristics in 180 nm and 65 nm CMOS technologies,” Proc. IEEE Int. Symp. Circuits and Systems, pp.3858–3861, May 2006.
[15] B. Li, L.-S. Peh, and P. Patra, “Impact of process and temperature variations on network-on-chip design exploration,” Proc. 2nd ACM/IEEE Int. Symp. Network-on-Chip, pp.117–126, April 2008.
[16] N. Onizawa and T. Hanyu, “Robust multiple-valued current-mode circuit components based on adaptive reference-voltage control,” Proc. IEEE Int. Symp. Multiple-Valued Logic (ISMVL), pp.36–41, Okinawa, Japan, May 2009.
[17] M. Shams, J.C. Ebergen, and M.I. Elmasry, “Modeling and comparing CMOS implementations of the C-element,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol.6, no.4, pp.563–567, Dec. 1998.
[18] J. Sparso and S. Furber, Principles of Asynchronous Circuit Design, Kluwer Academic Publisher, pp.9–28, 2001.

Naoya Onizawa received the B.E., M.E. and D.E. degrees from Tohoku University, Sendai, Japan, in 2004, 2006 and 2009, respectively. He is currently a research associate in the Research Institute of Electrical Communication, Tohoku University. His main interests and activities are in the asynchronous circuit and data transfer scheme based on multiple-valued circuit technique, and their applications. Dr. Onizawa is a member of the IEEE.

Takahiro Hanyu received the B.E., M.E. and D.E. degrees in Electronic Engineering from Tohoku University, Sendai, Japan, in 1984, 1986 and 1989, respectively. He is currently a Professor in the Research Institute of Electrical Communication, Tohoku University. His general research interests include nonvolatile logic circuits and their applications to ultra-low-power and/or PVT-variation-free VLSI processors. He received the Outstanding Paper Award at IEEE International Symposium on Multiple-Valued Logic in 1986, the Distinctive Contribution Award at IEEE International Symposium on Multiple-Valued Logic in 1988, the Niwa Memorial Award in 1988, the Sakai Memorial Award from the Information Processing Society of Japan in 2000, the Judge’s Special Award at the 9th LSI Design of the Year from the Semiconductor Industry News of Japan in 2002, APEX Paper Award of Japanese Society of Applied Physics in 2009, the Excellent Paper Award of IEICE, Japan, in 2010, and Ichikawa Academic Award in 2010. Dr. Hanyu is a member of the IEEE.