High Bandwidth Memory on FPGAs: A Data Analytics Perspective

Kaan Kara†‡, Christoph Hagleitner‡, Dionyssios Diamantopoulos‡, Dimitris Syrivelis‡, Gustavo Alonso∗

∗† Systems Group, Department of Computer Science
ETH Zurich, Switzerland, firstname.lastname@inf.ethz.ch

‡ IBM Research
Zurich, Switzerland

Abstract—FPGA-based data processing in datacenters is increasing in popularity due to the demands of modern workloads and the ensuing necessity for specialization in hardware. Driven by this trend, vendors are rapidly adapting reconfigurable devices to suit data and compute intensive workloads. Inclusion of High Bandwidth Memory (HBM) in FPGA devices is a recent example. HBM promises overcoming the bandwidth bottleneck, faced often by FPGA-based accelerators due to their throughput oriented design. In this paper, we study the usage and benefits of HBM on FPGAs from a data analytics perspective. We consider three workloads that are often performed in analytics oriented designs into a columnar database (MonetDB) and show the trade-offs arising from the integration related to data movement and partitioning. In certain cases, FPGA+HBM based solutions are able to surpass the highest performance provided by either a 2-socket POWER9 system or a 14-core XeonE5 by up to 1.8x (selection), 12.9x (join), and 3.2x (SGD).

Index Terms—High Bandwidth Memory (HBM), FPGA, Database, Advanced Analytics

I. INTRODUCTION

Performing advanced data analytics efficiently in the datacenter is becoming more important, driven mainly by the exponentially increasing amount of data to be processed and by the rise of machine learning. Due to the stagnating performance of general purpose processors in recent years, specialized hardware solutions are being considered by major cloud providers as an alternative to achieve high performance and energy efficiency. Prominent examples include the development of the Tensor Processing Unit (TPU) by Google to accelerate deep learning [1], the usage of FPGAs by Microsoft in their datacenters to offload computation to the network [2] and perform low latency inference [3], the design of interconnects such as OpenCAPI [4] allowing easy integration of accelerators into systems, and FPGA instances being included in cloud offerings of AWS [5] and Baidu [6].

Thanks to their architectural flexibility, FPGAs are widely used for a variety of data processing tasks including machine learning [7–9], database query processing [10], [11], and networking [12]. One of the main bottlenecks faced by current FPGA designs is the bandwidth when accessing data to be consumed or produced. For throughput-optimized accelerators, that are often implemented on FPGAs, high bandwidth access to data is crucially important. For instance, recent work on FPGA-based data analytics on partitioning [11], linear model training [13], inference based on decision tree traversal [14], and regular expression matching [15] all mention the bandwidth to memory to be the bottleneck in performance. Because of this limitation, vendors have started offering FPGA devices with High Bandwidth Memory (HBM).

On Xilinx UltraScale+ devices [16], the HBM exposes a wide bus (8192-bits) to the FPGA fabric, via 32 256-bit AXI3 interfaces. When the logic is clocked at 400 MHz, this bus provides a theoretical peak bandwidth of 410 GB/s towards the HBM with a size of 8 GiB. While this is an improvement over existing systems such as PCIe-attached FPGA cards [17] with four DDR4 banks (72 GB/s max), or coherently-attached FPGAs as in Intel Xeon+FPGA [18] (20 GB/s max), the architecture raises questions about the usability of the bandwidth in a practical setting.

In this paper, we answer questions that arise regarding the usage of HBM on an FPGA from a data analytics perspective: (1) What are the characteristics of the workloads that benefit most from using the HBM on an FPGA? (2) How does the data partitioning and address space usage affect total usable bandwidth? (3) What does the system look like regarding computation and data movement with an HBM-enabled FPGA when integrating accelerators into a large-scale system such as a database? (4) What FPGA-related challenges such as timing closure and floorplanning arise when using the HBM?

To answer these questions, we implement three workloads often used in advanced analytics scenarios. The first is range selection, performing a scan of a data column and producing the indexes of values within the specified range. This represents a memory bound operation. The second is a relational join operation, commonly used in databases to match two tables on a given attribute. Joins can be both data and compute intensive, containing also many irregular access patterns [19]. The third workload involves training generalized linear models (GLM) using stochastic gradient descent [20], a commonly used model and optimization algorithm in machine learning. This represents a more compute intensive workload with iterative access to the data and frequent updates to its state, that is the model under training.

Our contributions are as follows:

- We present a system architecture enabling the design of accelerators taking advantage of the HBM on the FPGA while working as part of a database management system.
- We perform microbenchmarks showing under which circumstances the peak bandwidth of HBM can be achieved.
We design and integrate three acceleration solutions into the presented system architecture: range selection, join, and stochastic gradient descent; covering data analytics and in-database machine learning use cases.

We evaluate each accelerator solution in-depth showing how and when they benefit from the HBM and compare the resulting performance to high-end multi-core CPUs.

II. BACKGROUND

HBM architecture on Xilinx FPGAs. Figure 1 shows an overview of the HBM architecture on Xilinx UltraScale+ FPGAs, based on the documentation for the HBM IP Core [21]. There are 2 HBM stacks, each with 16 so-called pseudo memory channels that are connected to the FPGA with a 64-bit wide port. The HBM IP provided by Xilinx contains 16 memory controllers (each responsible for 2 pseudo channels) and a 32×32 crossbar. The IP converts the 64-bit wide port to a 256-bit wide port to a 256-bit wide one, to reduce the clock frequency requirements of the FPGA. Each 256-bit port is exposed to the FPGA fabric as an AXI3 port, in total 32 of them. The crossbar allows each of the AXI3 ports to access the entire address space, 8 GiB in total. When using the HBM IP, we leave most of the default configurations in the 2 stack configuration, apart from changing the traffic pattern to \textit{linear}, since the workloads of interest will access data in a sequential manner.

When utilizing the crossbar, any congestion on a particular memory channel reduces the effective bandwidth. For instance, if all AXI3 ports try to access the first channel (address space between 0 and 256 MiB), the effective bandwidth is \( \frac{1}{32} \) of the highest achievable one. We show this behavior later with the microbenchmarks.

The target platform is the Alpha Data ADM-PCIE-9H7 [22] (AD9H7) card attached to a POWER9 machine via OpenCAPI [4], as shown in Figure 1. The FPGA on AD9H7 is an engineering sample device (Xilinx XCVU37P-2E). On the FPGA, the control and CPU interfaces are implemented in SystemVerilog. The compute engines discussed later in Sections IV, V, and VI are implemented with Vivado HLS.

Evolution Setup. Our baseline CPU experiments are on a 2-socket POWER9 system, each socket with 22 cores at 3.9 GHz. As an x86 baseline, we use a single-socket Xeon Broadwell E5 with 14 cores [23] at 3.5 GHz. On POWER9, we use xlc 16 and compile with "-O3 -march=native". On XeonE5, we use gcc 5.4 and compile with "-O3 -march=native".

Microbenchmarking HBM on AD9H7. We perform microbenchmarks on the FPGA to get an understanding on the behavior of HBM. In particular, we focus on the bandwidth that can be achieved (1) depending on how many ports are utilized and (2) the address space accessed by each port. The infrastructure for performing these benchmarks are shown in Figure 1. Each AXI3 port that the HBM IP exposes is connected to a standalone traffic generator (TG), that can be controlled dynamically by the host. Each TG has 4 configuration parameters: (1) address, (2) size, (3) iterations, (4) read or write. With these parameters, we can generate traffic individually on each port, that is for instance heavy on sequential reads/writes to measure maximum bandwidth, or heavy on single short accesses to measure latency.

Figure 2 shows the read bandwidth measured depending on the number of ports used and address separation per port. The address separation is created by setting the offset of each traffic generator according to the following formula:

\[
\text{offset} = S \times 1 \text{ MiB} \times (TF_{id} - 1)
\]

where \( S = \{256, 192, 128, 64, 0\} \) and \( TF_{id} = [1, 32] \). In the ideal case, when the separation is 256 MiB, we measure 282 GB/s (300 MHz) and 190 GB/s (200 MHz) with 32 ports active. In the worst case, when the separation is 0 MiB (all ports access the same physical HBM channel), we measure 21 GB/s (300 MHz) and 14 GB/s (200 MHz) with 32 ports active. The experiment when repeated for writes yields very similar results to reads. The outcome of this benchmark shows the importance of ideally partitioning the data on the HBM to be consumed or produced by the compute engines on the FPGA. The highest bandwidth benefits can only be observed when each port accesses its own physical memory channel.

The reasons for not reaching the theoretical bandwidth of 410 GB/s are: (1) We perform the benchmark at highest 300 MHz for AXI3, whereas 400 MHz is required to reach the theoretical maximum. For scale-out architectures, meeting
data partitioning across the address space during runtime or (2) statically merging ports where a constant offset is applied to some ports to ensure ideal separation. We use a mix of these: The HBM-shim in Figure 3 uses static port merging for ideal stack partitioning; and otherwise runtime partitioning is utilized when possible. The shim merges 2 ports from the first and second stacks (ports 0 and 16, 1 and 17, etc.) to form a 512-bit AXI3 port, where a constant offset is applied always to the second port ensuring that there are no inter-stack accesses. The HBM-shim serves multiple purposes: It simplifies the HBM interface, ensures ideal separation across the two HBM stacks, and reduces the burden of controlling 32 parallel engines by half.

**Data Movement.** In our target system (in-memory DBMS), the data to be consumed resides in the main memory of the CPU. How to bring this data to the FPGA to be consumed by the CEs which are also attached to the HBM is one of the problems that the presented architecture aims to solve. A first alternative is to connect each CE both to the DMA (communicating with the CPU) and to one port on HBM. This however (1) creates a bandwidth imbalance and (2) requires arbitration when accessing the DMA by multiple CEs, complicating system architecture and leading to difficult routing. Instead, we choose a datamover based solution: Two dedicated datamovers are employed to move data between the CPU memory and the HBM. The datamovers occupy 2 of the 16 ports that the HBM-shim exposes. The remaining ports are usable by CEs, consuming/producing data via the HBM.

**Scale-Out Computation.** Any solution benefiting from the HBM should be a scale-out parallel one. Therefore, we attach multiple CEs to the HBM, each connected to a central control unit, that can asynchronously start/stop and monitor the CEs. The control unit is exposed to the CPU via a register read/write interface enabling asynchronous control by software: So, each CE can be started/stopped individually in parallel. Where necessary, synchronization among them (e.g., barriers) can be implemented via software.

### III. System Architecture

Figure 3 shows the architecture built on the target platform. Various compute engines (CE) on the FPGA take advantage of HBM and are integrated as operators into MonetDB. The design decisions behind this architecture are as follows:

**Simplifying HBM Interface.** HBM IP by default offers 32 AXI3 ports, each 256-bit wide (Section II). We showed the highest bandwidth can be reached only if the physical memory channels are accessed in parallel. This can be ensured (1) via timing is difficult, mainly due to Super-Logic-Region (SLR) crossings: All HBM ports are connected to SLR0, so any compute engine that cannot be placed at SLR0 has to cross SLRs. When implementing algorithms later, we found reaching 300 MHz reliably at high utilization is not possible, so we use 200 MHz for all the presented designs for the rest of the paper. This leads to the highest usable bandwidth of 190 GB/s in the ideally partitioned case. (2) Since our target FPGA is an engineering sample device, the HBM clock needs to be copped at 800 MHz rather than 900 MHz due to a silicon issue, leading to slight decrease in the available bandwidth.

**MonetDB.** a database management system (DBMS), is used as a baseline for the database workloads on the CPU and to integrate our FPGA-based accelerators. MonetDB [24] is a column-oriented in-memory database optimized for online analytical processing (OLAP). An HBM-enhanced acceleration system might improve such a DBMS in particular: (1) OLAP workloads tend to be read-heavy where data is scanned frequently to extract information via reduction operations such as selection or aggregation. (2) Column-oriented DBMS perform sequential access frequently and materialize their intermediate results heavily; in both cases, memory bandwidth plays an important role. (3) The query processing engine of the DBMS is optimized to work on data residing in main memory; compared to disk-optimized databases, this increases the potential of offloading tasks to accelerators. Recent work has focused on integrating FPGA-based accelerators to MonetDB to improve relational query processing [11], [15] and in-database machine learning [23], [26] via a user-defined-function (UDF) interface. In this work, we follow a similar approach, however focusing on the efficient usage of HBM, which to our knowledge is the first system to do so.

![Figure 3](image-url)
Data: int input[num_items], int lower, int upper
Result: uint result[num_items], uint num_matches
1 num_matches = 0
2 for i: 0 to num_items-1 do
3   if input[i] > lower and input[i] < upper then
4     result[num_matches++] = i;
5 end
6 end

Algorithm 1: Range selection algorithm, providing the indexes of items that are in the given range.

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AXI3 port bandwidth), this results in an internal buffer size of 64 KiB to store resulting indexes.

At the ingress pipeline, a DMA read module reads data from the HBM using the 512-bit AXI3 port and pushes it into a 512-bit wide FIFO. The FIFO is read by the Select Core, that internally has 16 parallel comparison and update units performing the selection (Algorithm 1, lines 3-5). The resulting indexes and number of matches can be written to on-chip memory (Block-RAM or Ultra-RAM) in parallel by the update units thanks to the spatial partitioning.

At the egress pipeline, the results stored in on-chip memory are read in parallel, a 512-bit line is constructed and written back to HBM via DMA Write. At this stage, since the number of matches from 16 individual units might differ, we append a dummy element to the line whenever necessary, when writing the results back. In the end, this causes some more data to be written than necessary; the same trick needs to be employed also on the CPU when utilizing SIMD instructions.

Evaluation. We use one bitstream with 14 selection engines utilizing all 14 AXI3 ports exposed by the HBM-shim (Figure 3). The number of engines used and the data placement are runtime decisions. Figure 3 shows the processing rate with strong/weak scaling, over the number of threads used. The selectivity is 0%, so no output is generated and the focus is on the data consumption rate. For the selection operator only we assume the input data is already in the HBM. This is reasonable for bandwidth sensitive operators, because the DBMS during the initial execution of a query brings the data from the disk: The first query takes much longer than subsequent ones, similar to bringing data to HBM for the first query, which in this case is more expensive than performing selection since OpenCAPI bandwidth is lower than HBM.

When input data is partitioned in an ideal way, such that the engines access data from their own physical memory channel, the selection can be performed at 154 GB/s with 14 engines: 11 GB/s per engine, where theoretical maximum is 12.8 GB/s. Even in the weak scaling case, when XeonE5 reaches its memory bandwidth, the FPGA can outperform XeonE5 by 2.7x (57 GB/s with 256 threads) and POWER9 by 1.6x (94 GB/s with 256 threads). When the data is not partitioned however, the advantage of HBM is diminished and processing rate with all 14 engines drops to 16 GB/s.

Figure 6 shows the effect of selectivity: With increased selectivity, more output is generated. The FPGA numbers with (copy) include the copying time of output data from the FPGA to the CPU.

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Algorithm 2: Naively partitioned hash join.

V. JOIN

In relational databases, joins are frequently performed especially in analytical settings. There is a large body of work optimizing join algorithms for CPUs [19], GPUs [27], and FPGAs [11]. In this work, we are interested to provide an end-to-end join implementation that can directly be used by the DBMS (MonetDB), while benefiting from HBM. Much of the related work on join optimization [19] focuses on finding the number of matching tuples, without materializing (writing back the resulting tuples), which can be expensive but necessary if the join is to be used in a DBMS. Therefore, we also include the materialization step in our implementation.

MonetDB by default uses a naively partitioned hash join implementation (Algorithm 2). The larger side of the join is partitioned across the number of threads to be used. The smaller side is used to create one hash table (line 5), that is used by all threads during probing (line 9). One drawback is that if the hash table does not fit the cache, the latency bound operation of probing the hash table becomes a bottleneck. More sophisticated algorithms such as radix join [28] perform high fanout radix partitioning to eliminate this problem, making sure the hash table fits the cache. Recently, Kara et al. [11] have shown that high fanout radix partitioning can be accelerated by an FPGA. But their method is useful only if the result of the partitioning is to be consumed by a CPU; so HBM does not provide an advantage for performing this operation, as the results need to be written back to CPU’s memory, making the CPU-FPGA interconnect the bottleneck. Furthermore, in many real world use cases or benchmarks emulating these (such as TPC-H [29]), one side of the join is usually much smaller because of a previously performed selection; so radix partitioning becomes less critical.

For these reasons and to also ensure seamless integration with MonetDB, we decide to implement the same hash join algorithm as used by MonetDB (Algorithm 2). This algorithm also fits well with the scale-out processing we look for to benefit as much as possible from the HBM.

FPGA Implementation. An overview for the implementation on the FPGA is shown in Figure 7. We aim to optimize the probing step as much as possible, since building the hash table takes a negligible time (uses the smaller side of the join). Also, parallelizing the build step with SIMD is not possible, since each new insertion depends on the previous one due to possible collisions. For this reason, the build step is not parallelized and processes items one after the other (a 16-to-1 multiplexer is inserted in Build module to reduce the 512-bit line). Since we would like to achieve maximum SIMD parallelism during probe, 16 replicas for the same hash table are created, using Ultra-RAM resources. This is necessary, because during probing each item will point to a different location in the hash table and we would like to obtain 16 probe results in parallel at the same clock cycle.

Once the build step is complete, the probe is started by the scheduler. DMA Read, Probe/Assemble, and DMA Write all work in a parallel dataflow fashion. Thanks to the 16 replicas of the hash tables created, 16 probes are performed in parallel. The results are assembled at the same rate. If the number of results produced by each of the 16 pipelines differ, a dummy element is added to the 512-bit line during the assemble step at the locations where fewer results are produced. The entire probe step can thus be performed with an initiation interval (II) of 1, able to consume and produce 512-bits per cycle. Since each join engine requires 2 AXI3 ports (reading/writing simultaneously), we employ 7 join engines in our system (Figure 5) and generate one bitstream, utilizing all HBM ports.

**Evaluation: Configurations.** Table I shows the processing rate (size of L divided by the runtime) for the end-to-end join, including the copying time of the results from the HBM to the CPU’s memory. For differing configurations we obtain
differing processing rates. The main factors affecting the processing rate are: (1) Loading L from CPU’s memory to the HBM and (2) necessity to handle collisions due to S not being unique. The first factor is less critical: The DBMS also has to load data from disk when a query is executed initially, so subsequent ones are much faster. As long as the larger side of the join fits the HBM, the same can be assumed also for the join on the FPGA. The second factor is more critical: If S contains non-unique items, collisions need to be handled during probing. Due to the non-deterministic nature of collision handling, II=1 cannot be upheld leading to reduced processing rate. So, only joins that have a unique S benefit from HBM fully, reaching 81 GB/s when using 7 engines. An advantage is that this is a frequent case in relational processing, especially for primary-foreign key joins that take place often in real world workloads and benchmarks.

**Evaluation: Scaling.** Figure 8a shows how the processing rate scales with increasing number of threads. For the CPU baselines, we use MonetDB and measure the time for the individual join operator within the DBMS. We observe that even for the worst case (when L needs to be loaded and S is not unique so collision handling is required), the FPGA outperforms both XeonE5 and POWER9 using 64 threads. For the ideal case when L is already in the HBM and S is unique, the FPGA can outperform the best rate of XeonE5 by 12.8x. This rate is achieved when L is written to the HBM such that all engines access their own physical memory channels to benefit most from the HBM. As shown in Sections II and IV if this is not done, the high bandwidth advantage is lost.

**Evaluation: Size of the smaller side (S).** In Figure 8b, we show the effect of increasing the size of S on the end-to-end join runtime. This causes a linear increase (log x-axis) for the runtime on the FPGA, whereas a sublinear increase on the CPU as long as S fits the cache. The main reason for this is our probe-optimized join implementation on the FPGA. Since we want to benefit from HBM as much as possible during probing, we replicate the hash table 16 times per engine (7 engines in total) using large amount of on-chip memory. This causes the hash table size to be limited to 8192 tuples (16 KiB). When the smaller side is larger than this, we have to repeatedly scan the entire L, causing the linear increase in Figure 8b. The FPGA outperforms the CPU when L is already in HBM and S is unique until S has 125,000 tuples. From a DBMS perspective this is acceptable: Query optimization and algorithm selection is performed regularly for each query [24]. The FPGA adds an attractive alternative join implementation to the DBMS, that is to be used whenever the smaller side has less than 125,000 tuples, frequent in analytics workloads.

### VI. STOCHASTIC GRADIENT DESCENT (SGD)

Performing machine learning (ML) within a DBMS is becoming increasingly important, with all major vendors now offering this functionality [30–32]. Since ML has different requirements than traditional analytics, recent work has focused on providing accelerators to perform in-database ML efficiently [13], [33], [34]. In this paper, we focus on training generalized linear models (e.g., linear/logistic regression) with SGD. Recent work shows the advantage of using FPGAs [9]. The SGD accelerator can be designed as a fully pipelined dataflow architecture, saturating the memory bandwidth (6.5 GB/s) on their target platform (Xeon+FPGA [18]). HBM has therefore a large potential for improving SGD with a scale-out architecture on the FPGA and provide an even more pronounced advantage over general purpose processors.

SGD is an optimization algorithm that minimizes problems
of the following form:

$$\min_{x \in \mathbb{R}^n} \left( \frac{1}{m} \sum_{i=1}^{m} J(\langle x, a_i \rangle, b_i) \right) + \lambda \|x\|^2_2$$

(1)

$$J = \begin{cases} \frac{1}{2} \| (\langle x, a_i \rangle - b_i ) \|^2_2 & \text{for Rigderg} \\ -b_i \log( h_x( a_i ) ) - (1 - b_i) \log(1 - h_x( a_i ) ) & \text{for Logreg} \end{cases}$$

where \((a_1, b_1), \ldots, (a_m, b_m) \in ([-1, 1]^n \times \mathbb{R})\) is a set of samples and \(J : \mathbb{R}^n \times \mathbb{R} \to [0, \infty)\) is a non-negative convex loss function. SGD is shown in Algorithm 3.

**FPGA Implementation.** We implement FPGA-based SGD following a similar architecture as related work \[9\], shown in Figure 9. The dataset is scanned \(N\) times (number of epochs) and forwarded to the compute modules. These modules (Dot, ScalarEngine, and Update) work in a parallel dataflow fashion, as illustrated in Figure 9 ensuring full utilization.

Unlike Kara et al. \[9\] we do not allow stale updates to the model that can happen due to the latency of the entire pipeline and read-after-write dependencies (between lines 4 and 7). We thus ensure high quality convergence, but have to accept a lower processing rate for low-dimensional datasets and lower minibatch sizes, since the entire pipeline as shown in Figure 9 cannot be filled in those cases. Nevertheless, considering the processing rate of only one engine, even in the worst case we match Kara et al. \[9\] (6.5 GB/s) and exceed it by 1.7x in the best case, thanks to the higher bandwidth we get from one HBM-shim port. We use one bitstream with 14 SGD engines in the system architecture (Figure 3); all engines capable of performing SGD in parallel, reading data from the HBM and writing the trained model back.

**Evaluation.** We evaluate the SGD implementation using the datasets listed in Table II considering the popular hyperparameter search use case occurring frequently in real world scenarios \[35\]: Multiple models are trained on the same dataset, however with differing hyperparameters, to find the best set that achieves the highest test score. This problem is trivially parallel, but requires many processors and is usually performed using entire clusters. Our goal is to show that 1 FPGA with an HBM can replace multiple CPUs for performing this work, in an in-database ML setting. SGD is an iterative algorithm: data is read multiple times; so the initial copy cost from the CPU to the FPGA is negligible (<1% of total runtime).

**Evaluation: Processing rate.** Figure 10a shows how the processing rate scales with the number of parallel jobs, for training the last layer of an InceptionV3 neural network \[36\] for a binary classification problem, using the IM dataset. There are 28 hyperparameter configurations to search, resulting in 28 training jobs, each can be performed in parallel. The plotted processing rate is calculated by dividing the total size of the consumed data (number of epochs \(\times\) dataset size) by the end-to-end runtime (including copying of the trained model to CPU’s memory). We observe that the FPGA scales until 14, since there are 14 engines, reaching 156 GB/s processing rate at the peak. When using 28 parallel threads, the XeonE5 can reach maximum 34 GB/s while POWER9 reaches 49 GB/s.

As in the microbenchmarks (Section II), how the data accessed is incredibly important for HBM performance: If there is only one copy of the dataset, it creates a bottleneck when accessing the HBM from 14 engines in parallel, diminishing the HBM advantage (Figure 10a): FPGA-nonreplicated rate stays at 12.8 GB/s and does not scale with the number of engines used. To utilize the HBM, we have to replicate the dataset such that each engine can access its own physical memory channel without utilizing the crossbar. The replication will not be possible if the dataset is larger than 512 MiB (the size of 2 physical memory channels on the HBM, exposed as an AXI3 port by the HBM-shim in Section III). However, in that case a blockwise scan approach can be followed \[37\]: A block of the dataset that fits 512 MiB is read for multiple epochs and then gets exchanged for the next block, and so

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**TABLE II: Datasets used during evaluation**

| Name   | # Samples | # Features | # Classes | Epochs | Size (MB) |
|--------|-----------|------------|-----------|--------|-----------|
| IM     | 41600     | 2048       | binary    | 10     | 340.8     |
| MNIST  | 50000     | 784        | 10        | 10     | 156.8     |
| AEA    | 32768     | 126        | binary    | 20     | 16.5      |
| SYN    | 262144    | 256        | regression| 10     | 268.435   |

**Execution flow:**

- **Input:** Samples and model
- **Output:** Model

- **Dataflow:**
  - DMA Read
  - DMA Write
  - On-Chip Memory
  - Scalar Engine
  - Dot
  - Update
  - Time

**Figure 9:** Overview of the engine for performing SGD. PARALLELISM equals 16, to be able consume and produce 16 32-bit floats at every cycle and to match the AXI3 port bandwidth.

**Figure 10:** SGD processing rate. FPGA-replicated shows when the dataset to be consumed is replicated so that each engine accesses it via its own physical memory channel on the HBM.
TABLE III: Consumption on XCVU37P-2E-FSVH2892

| Bitstream | #Engines | LUT | LUTRAM | FF | BRAM | URAM | DSP |
|-----------|----------|-----|--------|----|------|------|-----|
| Selection | 14       | 17.99% | 3.35%  | 17.97% | 26.53% | 23.33% | 0%  |
| Join      | 7        | 40.81% | 35.88% | 26.13% | 58.48% | 23.33% | 0%  |
| SGD       | 14       | 55.76% | 5.02%  | 47.29% | 55.95% | 46.66% | 38.78% |

Fig. 11: Logistic loss over time depending on the minibatch size. Dataset is \textit{IM}.

on. This reduces the IO complexity between the CPU and the FPGA while replication leads to high bandwidth from HBM.

**Evaluation: Effect of dimensionality.** In Figure 10b, we show how the processing rates across platforms and datasets differ. Lower dimensional datasets (AEA) lead to lower processing rate per engine because the SGD pipeline (Figure 7) cannot be kept at 100% utilization. The reason is that we keep the read-after-write (RAW) dependency (lines 4 and 7 in Algorithm 1) in SGD, causing bubbles during the processing if the dataset is low dimensional. In certain cases, the RAW dependency can be ignored in FPGA-based implementations [9], since SGD tends to be tolerant against constant stale updates. However, the tolerance is not guaranteed especially if the samples are ordered in a certain fashion, so we choose to respect the RAW dependency to get high quality convergence.

**Evaluation: Minibatch size.** Figure 11 shows the convergence over time for minibatch sizes used during SGD on the FPGA. Larger minibatch sizes increase pipeline utilization, leading to higher processing rate and therefore faster convergence. The goal here is to show that we can converge to the same loss, when increasing the minibatch size from 1 to 16, while achieving significant speedup. Accordingly, we use 16 in all SGD experiments both on the CPU and the FPGA (Figure 9).

VII. DISCUSSION AND RELATED WORK

**Discussion: Timing.** Although HBM offers obvious advantages for data analytics and machine learning as we have shown, there are major design challenges when implementing accelerators on HBM-based FPGAs. Since taking advantage of HBM requires a scale-out architecture, the designs are more likely to be constrained on the available resources (Table III). This entails the usage of multiple SLRs. However, on Xilinx FPGAs all HBM ports are located at SLR0. So, the AXI interfaces from the engines that are located in other SLRs need to be routed across SLRs to reach the HBM. This makes the timing closure challenging and requires careful floorplanning. The way we solved this issue to a certain extent is to first constrain one compute engine to be placed in just one SLR and second add AXI-interconnect modules with internal buffering in SLRs in between the compute engine and the HBM. For instance, for a compute engine placed in SLR2, we put two AXI-interconnect modules in SLR1 and SLR0 to ease routing. A possible solution to this problem might be hardened overlays that route signals in wide busses rather than bitwise routing. As FPGAs become more popular for high performance data processing, efficient data movement becomes critical. While HBM is a step in the right direction as we show in this work, more advancements on the device level are needed to make the development easier.

**Discussion: Data movement.** Coherent interconnects such as OpenCAPI [4] allow uniform memory management between CPUs and accelerators: Address spaces on the accelerator can be mapped by the OS and used natively. Due to the ongoing development of accelerator endpoints to enable this, for this work we used dedicated datamovers that need to be initiated separately by the software. In the presence of uniform memory management, the integration to the database can be easier: The main copy of data can be mapped to the accelerator memory, eliminating initial copies, making acceleration more interesting for data movement sensitive use cases such as the join.

**HBM on many-core processors** are becoming common thanks to 3D-stacking and chiplets. Prominent examples include processors such as Intel Knights Landing (KNL) [40], NVIDIA Titan V, and Google’s TPU. Recent work has focused on showing the usefulness of HBM on KNL for data processing workloads. KNL being an x86 many-core architecture offers easy portability for existing codebases and allows rapid testing of HBM-related ideas. Cheng et al. [41] focus on optimizing NUMA placement of hash tables on KNL to increase the utilization of the HBM and provide simulation results for hash join. Pohl et al. [42] focus on using the HBM on KNL for joins and find that the mode where HBM is directly addressed as opposed to the cache-mode results in the highest performance. Miao et al. [43] show how the HBM on KNL can be used to improve stream processing focusing on grouping operations, finding that sort-based algorithms fit HBM better than hash-based ones that require random access.

**Database acceleration with FPGAs** is a popular field, where recent surveys have been published [44], [45]. Inherent parallelism and capability of creating specialized processing pipelines make FPGAs a good target in cases such as sorting [46], joins [10], hashing [47], regular expression matching [15], high fanout data partitioning [11], compression [48], and grouping in the datapath [49]. Accelerator integration is a challenge that has been loosely addressed by systems such as doppioDB [25]. When considering end-to-end integration of FPGA-based accelerators, HBM might not be advantageous at all, especially if the accelerator relies on hybrid processing [11], so in this work we considered cases that can be performed completely on the FPGA, taking advantage of the HBM. Other workloads such as sorting and grouping might benefit from HBM just as well, following similar principles.

**In-database machine learning** is nowadays commonly per-
Recent work [13], [33], [34] has focused on improving these operations with FPGAs, with an additional benefit of an offload from the CPU, leaving the CPU better suited for processing database queries with low response times [20]. Mahajan et al. [35] propose a framework for FPGA accelerators to perform training with SGD and low-rank matrix factorization within PostgreSQL. Wang et al. [13] propose a fully specialized pipeline to take advantage of quantized datasets when training with SGD. Kara et al. [34] focus on training using column-stores and perform on-the-fly decompression/decryption on the FPGA. Thanks to the HBM, we are able to surpass their performance substantially at 156 GB/s, compared to 3.76 GB/s [33] and 15 GB/s [13] under same configurations (SGD with logistic regression and full precision input data). When implemented using the same principles, these works would likely benefit from HBM just as well, where resource consumption will be the determining factor to reach the target scale-out parallelism.

VIII. CONCLUSION

We show an end-to-end system with HBM-attached FPGA accelerators integrated into a main-memory database. Thanks to the HBM, even memory-bound algorithms such as range selection benefit from being implemented on the FPGA. Data intensive algorithms such as joins benefit under certain conditions, while offloading machine learning workloads such as SGD that access data iteratively provides consistent improvement compared to CPU-based solutions. For all workloads, we have shown the importance of data partitioning and address space usage in the HBM to utilize it to its full potential.

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