Abstract—Recurrent neural networks such as Long Short-Term Memories (LSTMs) learn temporal dependencies by keeping an internal state, making them ideal for time-series problems such as speech recognition. However, the output-to-input feedback creates distinctive memory bandwidth and scalability challenges in designing accelerators for RNNs. We present MUNTAIALA, an RNN accelerator architecture for LSTM inference with a silicon-measured energy-efficiency of 3.25TOP/s/W and performance of 30.53GOP/s in UMC 65nm technology. The scalable design of MUNTAIALA allows running large RNN models by combining multiple tiles in a systolic array. We keep all parameters stationary on every die in the array, drastically reducing the I/O communication to only loading new features and sharing partial results with other dies. For quantifying the overall system power, including I/O power, we built VAU DA MUNTAIALA, to the best of our knowledge, the first demonstration of a systolic multi-chip-on-PCB array of RNN accelerator. Our multi-die prototype performs LSTM inference with 192 hidden states in 330µs with a total system power of 9.0µW at 10MHz consuming 2.95µJ. Targeting the 8/16-bit quantization implemented in MUNTAIALA, we show a phoneme error rate (PER) drop of approximately 3% with respect to floating-point (FP) on a 3L-384NH-123NI LSTM network on the TIMIT dataset.

Index Terms—LSTM, neural network, recurrent neural network, deep learning, hardware, systolic, multi-chip, accelerator, Chipmunk.

I. INTRODUCTION

The availability of vast amounts of training data and computing power has enabled increasingly sophisticated machine learning (ML) algorithms, particularly models based on deep learning (DL), to excel in many tasks, such as image recognition [1], speech recognition [2], natural language processing [3], language translation [4], and autonomous gaming bots [5]. While a lot of DL research focuses on image processing, one particular time series problem has seen much interest in both industry and research: automatic speech recognition (ASR). The emerge of Deep Neural Network (DNN) for ASR has enabled novel speech-based user interfaces such as Amazon Alexa, Google Assistant, Apple Siri, Microsoft Cortana, and others. Recurrent neural networks (RNNs) are DL models that include an internal state allowing them to learn time-dependencies, making them an ideal candidate for learning tasks on time series, like ASR. Even though new time series oriented models based on, e.g., convolutional neural networks (CNNs) [6] or attention (e.g., Transformer [4]) have been proposed, RNNs, and especially LSTMs, were still 21% of all DL training workload of Google’s tensor processing units (TPUs) in their datacenters in 2019 [7]. Especially time series applications targeting medium to small Internet-Of-Things (IoT) devices with limited memory and compute resources have been mainly addressed by RNNs. In these scenarios, a part of the ASR alongside many other tasks (e.g., Keyword Spotting) is still primarily approached using two particular RNN types: Long Short-Term Memory (LSTM) and Gated Recurrent Units (GRUs).

The leading-edge accuracy of these methods has motivated a strong push toward embedded low-power accelerators to bring these advantages to energy-constrained products such as hearing aids or headphones [8]. As research has paid a lot of attention to CNNs, many specialized FPGA [9], [10] and ASIC [11]–[15] accelerators for low-power CNN inference have been proposed, which achieve energy-efficiency gains in the range of three orders of magnitude with respect to general-purpose architectures [16]. A significant contributor to this significant energy-efficiency gain comes from computing not in floating-point but rather in fixed-point numbers, which makes specialized training methods for minimizing an imposed accuracy loss an absolute requirement. While recent research shows that CNNs are very resilient towards accuracy loss even when using binary weights, there is less work available on quantizing RNNs, whose training process is less stable and more complex than for CNNs [17]. Additionally, the specialized architectural optimizations developed for accelerating CNN inference cannot directly be adopted to accelerate RNN inference. The additional challenges, such as the necessity of storing and regularly updating an internal
state, the densely connected layers with a low computation to memory-footprint ratio, ask for novel algorithmic and architectural solutions. State-of-the-art LSTM RNN models for ASR can contain up to multiple millions of parameters [17], making efficient data transfer and storage design a necessity. Typically, there are two possibilities: all parameters and internal states are either stored on-chip (e.g., SRAMs), which results in large dies dominated by SRAM, or stored off-chip in dense DRAM memories, whose content needs to be constantly (re-)loaded into the accelerator. The former approach of scaling the accelerator by arbitrarily increasing the die size is not cost-effective and ultimately infeasible due to decreasing yield. The second option implies slower and energy-inefficient state data access. Hence, performance and energy become dominated by the constant, high I/O activity toward external memory.

In this work, we present a solution based on the on-chip storage approach that allows scaling beyond a single die to keep the data local, readily accessible in a more energy-efficient way than with the constant weight reloading approach for bigger problem sizes. Building upon our recently presented energy-efficient LSTM accelerator called CHIPMUNK [18], this work presents the following contributions:

1) We introduce MUNTANIALA, an extension of CHIPMUNK for easier integration in a systolic array. The architecture of the MUNTANIALA chip-tile allows multiple tiles to work together in a multi-chip n x n array, while keeping all network parameters on-die local, and minimizing inter-die traffic, resulting in an ideal solution for the cost limited die scaling.

2) We present VAU DA MUNTANIALA, to the best of our knowledge, the first full-system demonstration of an exemplary systolic grid of 2 x 2 MUNTANIALA LSTM accelerator chips on an FPGA-controlled PCB, collaboratively performing LSTM inference with 192 hidden states (using tiny dies capable of storing only 96 hidden states each) with minimal total system power of 9.0 mW over 330µs at 10MHz, 1.2V core supply and 2.5V pad supply.

3) In contrast to most publications on accelerators that ignore I/O power, we measured the I/O and core power consumption of our prototypes, allowing us to make a complete power evaluation.

4) We have trained an LSTM network on the TIMIT dataset and studied the quantization losses for the chosen 8/16-bit quantization used for MUNTANIALA.

The next section Section II gives an overview of the related work. The following architecture Section IV starts with a short introduction to LSTM RNNs and then describes the single-die MUNTANIALA architecture and how it can be scaled systolically. Additionally, that section will describe our demonstrator PCB, called VAU DA MUNTANIALAS. Section V discusses all results, and Section VI concludes our work.

1Romansh for “marmot”.
2Romansh for “marmot burrow”.

II. RELATED WORK

A. DNN and RNN Acceleration

In general, the rather complex data dependencies encountered in RNN models make their acceleration more difficult than for feed-forward networks. Therefore, CPUs and GPUs have difficulties in exploiting the fine grained parallelism encountered in RNNs. Even though batching helps with the parallelism, the CPUs and GPUs remain very under-utilized [19].

Accelerators implemented on Field-Programmable Gate Array (FPGA) can be more effectively tailored to the requirements of the dataflow of RNNs and, therefore, can achieve a higher energy-efficiency and performance than CPU and GPU implementations.

The FPGA-based accelerator ESE from Han et al. [20] works directly on a precompressed parallelization-friendly RNN model. Their compression method is based on load-balance-aware pruning and compresses the LSTM model by a factor of 10x (without quantization). Wang et al. [21] apply another compression method based on block-circulant matrices on the model parameters and further reduce the computational complexity with the help of a Fast Fourier Transform algorithm. Cao et al. [22] introduce Bank-Balanced Sparsity (BBS) and apply it to the model parameters. Some recent work has been focusing more on the feature maps: The works of [23], [24] go a slightly different way and only compute inference on delta-updates, and [25] propose a hardware-friendly compression method to reduce the bandwidth requirements to transfer the feature maps. However, even with these advanced algorithm adaptations, which sometimes require specialized training methods, the maximum energy-efficiency achieved by FPGA-based accelerators is around 165 GOP/s/W [24].

However, this energy-efficiency is still too high for energy-constraint embedded IoT devices and highly efficient high-performance computing platforms. FPGAs are, in general, too power-hungry for low-power always-on application scenarios, which require power consumption on the other of a few mW.

In the last years, many specialized ASIC accelerators have been proposed for DNN and RNN inference [26–29]. These specialized accelerators achieve two orders of magnitude higher energy-efficiency than the previously presented FPGA-based accelerators. Many proposed accelerators, such as [30–32], include, in addition to specialized compute units, one or multiple microcontroller-style cores for dataflow control and computation. These heterogeneous systems usually focus on accelerating CNNs and fully-connected networks (FCN) instead of RNNs [33]. In contrast to our proposed MUNTANIALA design, where the non-linear activation functions are accelerated, these functions are performed on the cores and create a performance bottleneck. They are, therefore, not fully optimized for the complex dataflow dependencies coming with RNNs such as LSTMs. While accelerators such as EERA-ASR [34] and ELSA [26] make use of approximate compute units, the accelerator from Kadetotad et al. [28] applies an algorithmic parameter compression technique called hierarchical coarse-grain sparsity (HCGS), which allows reducing the weights by a factor of 16x while keeping the accuracy loss.
minimal. \cite{35} proposes a new model parameter compression scheme called compressed and balanced sparse row (CBSR) and shows improved throughput and energy efficiency over the compressed sparse column and rows (CSC and CSR) for an exemplary accelerator placed and routed in 65nm technology. In contrast, \cite{36} shows that up to 90% sparsity can be introduced to the recurrent hidden states without incurring any accuracy degradation on a set of tasks. Their accelerator shows an energy efficiency improvement by up to 5.2× when zero-skipping these sparse state computations. All these accelerators are mainly optimized for limited model sizes. Once the models get bigger than their on-chip storage capacity, they are all forced to reload their parameters, thereby creating an I/O bottleneck which is removed by our Muntaniala design, which, once all parameters are loaded, can work on multiple dies with local on-chip weights.

One way of scaling up the accelerator size is scaling the die size up to a complete wafer, such as the recently presented Cerebras CS-1 wafer-scale engine (WSE) \cite{37}. The Cerebras CS-1 WSE is the largest single die computing system produced so far and comes with benefits such as performance boost by order of magnitude due to the, e.g., lower on-chip communication cost in power and delays compared to on-board communication. However, the engineering effort and cost needed to produce such a wafer-scale engine are enormous and require not only highly advanced solutions for handling production imperfections but also highly advanced packaging and cooling solutions \cite{37}.

Another way to scale up computing systems can be achieved by combining multiple monolithic dies, also called chiplets, within a single package. Such systems, also called multi-chip-module (MCM), have not only been proposed for high-performance multi-core SoC architectures such as e.g. the works from Vivet et al. \cite{38} and Zaruba et al. \cite{39}, but also for DNN acceleration. Zimmer et al. \cite{40} and Shao et al. \cite{41} proposed to accelerate DNNs with an MCM containing 36 chiplets in a mesh-style network-on-chip (NoC) based communication system using ground-referenced signaling (GRS). Our MUNTANIALA prototype includes no advanced I/O interfaces, as no such interface IP blocks were available for the context of this research. Nevertheless, our design can be easily adapted to implement any form of MCM, or wafer-scale engine. Hyperdrive from Andri et al. \cite{42} implements a systolically scalable accelerator very similar to the MUNTANIALA. However, they accelerate only CNNs and implement resource-intensive FP16 arithmetic, while we focus on RNNs and work with fixed-point arithmetic. Additionally, we go one step further and provide not only single prototype results but evaluate the design from a fully fabricated demonstrator including a complete systolic array of 2 × 2 MUNTANIALA dies.

### B. Quantization

Since the rise in demand for DNN inference, many methods have focused on reducing the required numerical precision and in turn mitigate memory bandwidth pressure and compute complexity. With only minimal modifications, DNNs have been shown to run without accuracy loss using reduced bit-width floating-point formats such as IEEE’s half-precision (float16), Google’s “brain floating point” (bfloat16), and Nvidia’s 18-bit TensorFloat format—all of which have been implemented on a variety of platforms from microcontrollers to GPUs and application-specific processors \cite{43}, \cite{44}.

To further boost the energy-efficiency and performance, several methods have been proposed to enable 8-bit fixed-point inference with merely a calibration phase to optimize the value ranges of the activations and filter weights, with some extracting additional offsets, rescaling factors, or bit-shifts \cite{45}. This has drawn a lot of attention due to the efficiency gains and reduced memory bandwidth for hardware accelerators and its suitability for 4- or 8-way SIMD in processor-based devices. These methods have a very small impact of less than 2% on the accuracy for most feed-forward networks, although some recent networks such as in MobileNetV2 have been shown to be challenging for re-training-free approaches \cite{45}.

Higher-precision but more computational demanding quantization is based on retraining to adapt network weights to compensate for the quantization effect (quantization-aware training, QAT). This allows to attain almost identical accuracy even for MobileNetV2/V3 \cite{46}, \cite{47} and almost eliminates the small gap seen for most other networks when quantizing uniformly to 8-bit weights and 8-bit activations. Note that for most of these networks, the (re-)quantization is applied right before the convolutions or after the activations, performing by-pass/skip connections in full precision. Support for QAT is found in many common frameworks such as Keras/TensorFlow or PyTorch and is typically based on the straight-through estimator (STE).

Besides the common 8-bit QAT, a lot of efforts have been undertaken to further reduce the precision of weights and activations, even down to binary and ternary representations. While in initial efforts, the weights were quantized using STE as well, clear improvements have been shown when a method called incremental network quantization (INQ) \cite{48} was introduced, followed by moderate additional improvements using ADMM and RPR \cite{49}, \cite{50}. These methods can be applied to uniform quantization but also to power-of-two quantization levels. In contrast, some other methods like LQ-Nets \cite{51} and TTQ \cite{52} learn the quantization levels to further improve the accuracy at the expense of making their implementation very costly. The commonality of the quantization procedures is their resilience to extreme quantization with 2–3% accuracy loss for ternary weights and around 1% for 5-ary weights.

The feedback loop inherent to RNNs makes them particularly challenging to quantize. In \cite{53}, they propose a special flavor of STE to quantize weights, balancing their distribution for each layer before quantization during the forward pass and backpropagate the gradients as if there was no quantization. For the quantization of the activations, they perform normal STE, resulting in an overall accuracy drop of 3% for 4 bit weights and activations on the IMDB sentiment classification dataset. Xu et al. \cite{54} quantize the weights by choosing the nearest quantization level and alternatingly optimize the underlying full-precision weight and the quantization levels, showing an accuracy decrease from 92.5 to 95.2 perplexity per word (PPW) on the PTB dataset. Alom et al. \cite{55} show an accuracy decrease from 82.9% to 79.6% on the IMDB sentiment
III. Fundamental Concept: LSTM Networks

Standard Recurrent Neural Networks (RNNs) use a feedback of the hidden state \( h_t = (h_1, h_2, ..., h_{N_H}) \) with \( N_H \) elements to learn short-time dependencies over time \( t = 1, ..., T \) from an input state \( x_t = (x_1, x_2, ..., x_{N_I}) \) with \( N_I \) input features iteratively:

\[
h_t = \text{act}(W_{xl}x_t + W_{lh}h_{t-1} + b_h) \tag{1}
\]

where \( W_{kl} \) are weight matrices, \( b_l \) a bias vector whereas the subscripts \( k \) stand for the source state/gate (\( x_t \) or \( h_{t-1} \)) and the subscripts \( l \) for the target state/gate (\( h_t \)) to which the source state is contributing to. The activation function \( \text{act}(\cdot) \) used in RNNs is typically a non-linear function such as hyperbolic tangent or sigmoidal function.

Long Short-Term Memory (LSTM) neural networks [59], a special type of RNN, have an additional internal cell state \( c = (c_1, c_2, ..., c_{N_H}) \) which allows the network to capture not only short-term, but also long-term dependencies. Additionally, so-called gates control the information flow to and from the cell state. An LSTM network layer can be described as follows:

\[
i_t = \sigma(W_{ix}x_t + W_{ih}h_{t-1} + w_{ci} \odot c_{t-1} + b_i), \tag{2}
\]
\[
f_t = \sigma(W_{xf}x_t + W_{hf}h_{t-1} + w_{cf} \odot c_{t-1} + b_f), \tag{3}
\]
\[
c_t = \sigma(W_{xc}x_t + W_{hc}h_{t-1} + b_c), \tag{4}
\]
\[
o_t = \sigma(W_{xo}x_t + W_{ho}h_{t-1} + w_{co} \odot c_t + b_o), \tag{6}
\]
\[
h_t = o_t \odot \text{tanh}(c_t), \tag{7}
\]

with the input gate \( i \), forget gate \( f \), output gate \( o \), the helper cell candidate state \( \tilde{c}_t \) and the cell state \( c \), whereas the subscripts \( k \) stand for the source state/gate \( (x_t, h_{t-1}, c_{t-1}) \) and the subscripts \( l \) for the target state/gate \( (i_t, f_t, c_t, o_t) \) to which the source state is contributing to. \( \odot \) denotes element-wise multiplication. Again, \( W_{kl} \) are weight matrices, \( b \) are bias vectors, and the \( w_{kl} \) are peephole weight vectors. If the weight vectors \( w_{kl} \neq 0 \) the cell state is leaking information from the cell to the gates and the LSTM layer is called peephole LSTM [60]. However, if the peephole weight vectors \( w_{ix}, w_{xc}, w_{xo} \) and \( w_{ih}, w_{hc}, w_{ho} \) are all 0, the layer is called a vanilla LSTM.

This section gives an overview of LSTM networks and then introduces the functionality of a stand-alone MUNTANIALA accelerator. Afterwards, we describe multi-die systolic scaling, highlight the differences between MUNTANIALA and its predecessor CHIPMUNK and finally introduce our demonstrator called VAU DA MUNTANIALAS.

A. MUNTANIALA: LSTM Accelerator

MUNTANIALA accelerates the inference of peephole LSTM as described by Figure 3 in addition, it can also be configured to run the FCL output layer, often used in LSTM [61]. The core architecture of MUNTANIALA is derived from CHIPMUNK [18] and mainly differs in the I/O interfaces and, therefore, in the off-die interconnect for the accelerator’s systolic setup. A summary of these differences can be found later in this section.

1) Architecture Overview: A simplified block diagram of MUNTANIALA’s datapath and its LSTM units is shown in Figure 2. The main computational effort of an LSTM inference, as described in Section III, comes from the computation of the gates and the cell candidate in Equations (2) to (4) and (6) and
# hidden element loop
# NH LSTM Units working in parallel
for ih in range(0, NH):
    # Everything in this loop is mapped into a single LSTM Unit containing:
    # - 1 MAC unit
    # - 2 different activation functions
    # as 8-bit Look-Up table
    # input state contribution
    # matrix-vector multiplication
    # sequentially computed on MAC unit
    for nx in range(0, NX):
        g[ih] = w[ih, nx] * x[nx]
    # hidden state contribution
    # matrix-vector multiplication
    # sequentially computed on MAC unit
    for nh in range(0, NH):
        g[ih] += w[ih, nh] * h[nh]
    # cell state contribution (peephole)
    # element-wise vector multiplication
    # sequentially computed on MAC unit
    g[ih] += w[ih] * c[ih]
    # bias contribution
    # element-wise vector addition
    # sequentially computed on MAC unit
    g[ih] += b[ih]
    # non-linear activation function
    # 8-bit Look-Up tables
    # sequentially computed on 8-bit LUT
    g[ih] = activation( b[ih] )

Fig. 3. Pseudo-code for a gate or cell-candidate computation within a peephole LSTM layer.

2) Systolic Design: The architectural design of MUNITANIALA can be trivially scaled up to support a larger hidden cell size \(N_H\) per die, which implies increasing the on-chip memory and the number of computational LSTM Units. However, it is not cost-effective and ultimately infeasible (due to decreasing yield) to arbitrarily increase the die size. The MUNITANIALA design addresses this issue and provides a low-cost solution that scales in a systolic fashion by combining multiple fixed-size dies or chips on an interposer or a circuit board, respectively.

The main computational load of LSTM networks comes from the matrix-vector multiplications (see lines 6 – 14 in Figure 3), whose problem size scales quadratically with the hidden state’s size. Once the problem size gets too big to fit on a single die, the matrix-vector multiplication can be divided into many smaller multiplications by tiling the weights and vectors and distribute them accordingly on multiple dies, as shown in Figure 5. Following the quadratic problem size scaling of the matrix-vector multiplication, scaling the layer size up by \(N_H = n \times N_H_{MUNITANIALA}\) results in a systolic array of \(n \times n = n^2\) MUNITANIALA dies. By giving every tile at position \((i,j)\) the corresponding \(\frac{1}{n}\)-th tile of the matrix and the corresponding input state tile as in Figure 5, every die can compute a partial result which needs to be communicated to the next-right die which combines the received and its own partial result, see Figure 5. This reduction is performed until the rightmost dies receive the results from all other dies in its row, which performs the missing final element-wise activation function. For the next inference step, every hidden state tile needs to be distributed according to Figure 5. Figure 4 shows the typical sequences of computations in a systolic arrangement of \(2 \times 2\) MUNITANIALA dies. As shown, the non-rightmost dies (also called slaves) are stalled. Simultaneously, the rightmost dies (also called masters) are finishing their final computations, typically consisting of accumulations and activations.

Previously, we only considered scaling of a single LSTM
Fig. 4. The timeline shows the typical computational sequences in a systolic arrangement of $2 \times 2$ MUNTANIALA tiles. Note that the block sizes are not proportional to their processing time consumption.

Fig. 5. For accelerating an LSTM network bigger than the network that fits on a single MUNTANIALA die, multiple dies can be combined together [18]. Figures [5a] to [5c] show the necessary communication when scaling the size of a single LSTM layer. Figure [5d] shows how the dies need to be connected for creating multiple LSTM layers.

Another possibility are deeper networks by feeding the hidden states output of one LSTM layer as the input state to another LSTM layer. The MUNTANIALA design supports this layer stacking by connecting the corresponding data stream interfaces from multiple quadratic grids, as shown in Figure [5d]. An LSTM network of $l$ layers where each layer has a size of $n \times N_{H_{\text{MUNTANIALA}}}$ would require to combine $l$ grids of $n \times n$ dies, which would in total amount to $l \times n \times n$ dies.

Another possibility of computing multiple layers on fewer dies can be done by not loading the weights only once but reloading them for every layer or sub-tile of a layer. This means that for $l$ layers, each of size $n \times n$, $N_{H_{\text{MUNTANIALA}}}$, only $1 \times n \times n$ dies can be used. After the computation of the first layer, all internal gates $i_t$, $f_t$, $o_t$, and states $c_t$, $h_t$ need to be read out and stored externally. Before the computation of the new layer can start, new parameters (weights and biases) and the corresponding stored gates and states are loaded. Of course, this has a significant impact on the performance and latency of the complete inference and is, therefore, more reasonable for less latency-critical classifications.

### 3) Improvements: MUNTANIALA vs CHIPMUNK

The main improvement from MUNTANIALA on its predecessor, CHIPMUNK, is the new, more compact, and specialized usage of I/O pins. As shown in Table I, every data stream is accompanied by two signals, valid and ready, which together allow communicating via a basic and straightforward handshake protocol. The only exception is the output interface of MUNTANIALA, which has two ready signals: one for the handshake with other MUNTANIALA dies and one for the handshake with the external control unit, e.g., an FPGA. While CHIPMUNK has only two bundled data interfaces: one 8 bit input, and one 8 bit output data stream, MUNTANIALA instantiates an interface per transmission source:

- **network parameters** $p^{(i,j)}$ such as weights, biases, and new features are fed in from an external controller (e.g., FPGA, microcontroller, ...)
- **intermediate reduction results** $r^{(i,j)}$ are received from a neighboring accelerator
- **hidden states** $h^{(i,j)}$ for the next inference step are received from a different neighboring accelerator than the reduction results

The indices $i, j$ refer to the position of the receiving accelerator. The usage of three independent data sources allows multiple MUNTANIALA dies to be connected either on-silicon or on board-level directly, thus reducing design complexity, off-chip load, etc. The resulting simplified data stream handling is shown in Figure [7c]. However, as during any communication phase, only one input interface
is active (or one output interface), the maximum number of data transferred is reduced from 8 bit/cycle to 4 bit/cycle. Correspondingly, the bandwidth is reduced from 168MB/s to 79.5MB/s. Note that the MUNTANIALA prototype was designed as a proof of concept. For industrial implementation, not only the die size (and with it the hidden state size on a single MUNTANIALA die) could be scaled up further, but also the used interface could be changed. For example, the High-Bandwidth Interconnect (HBI) offers a high-bandwidth, low-power and low-latency interconnect and is a general standard for die-to-die communication and corresponding IPs are offered by, e.g., Synopsys [62], [63].

4) System I/O Scaling: Every stand-alone accelerator needs external memory to supply the parameters and input data. Therefore, the bandwidth and I/O requirements to such an external memory are an essential design aspect for targeting the integration of MUNTANIALA into an end-to-end system. From Table I it is visible that a single die requires 4 data plus two handshake pins for receiving all parameters and the input features from the environment. Additionally, every chip has 3 I/O pins, which help with the configuration and synchronization of the dies. They are controlled externally, signaling the accelerator, e.g., to store out the internal states, load new states, load new parameters, or similar, and can typically be shared over all dies within a systolic array.

An important point to notice is that the I/O for the parameter distribution can be time-multiplexed and be targeted by a simple chip select signal as shown in Figure 6b. Of course, this is better for systolic configurations that do not need to reload their weights often. Therefore, the minimal required I/O is limited by the number of dies in the input layer \( n_{\text{inp}} \) and the number of dies in the output layer \( n_{\text{out}} \). These are the minimal pins needed to feed the input features and write back the final results: \( \# I/O_{\text{clk, rst}} + \# I/O_{\text{config}} + n_{\text{inp}} \times (4 + 2) + n_{\text{out}} \times (4 + 2) \) pins. At the cost of some additional latency, time-multiplexing for the incoming and outgoing data could be introduced, resulting in a reduced minimum required I/O of \( \# I/O_{\text{clk, rst}} + \# I/O_{\text{config}} + 1 \times (4 + 2) + 1 \times (4 + 2) = 17 \) pins.

B. Vau da Muntaniala: Systolic Demonstrator

The aforementioned improvements of the MUNTANIALA interface allow a direct connection on a Printed Circuit Board (PCB) between the accelerator interfaces in a systolic grid without requiring additional off-chip components such as multiplexers. We built a demonstrator PCB, called VAU DA MUNTANIALAS to take more detailed measurements on the interaction of multiple MUNTANIALA dies.

This PCB is controlled using a simple Field Programmable Gate Array (FPGA). The Zynq-7000 system-on-chip (SoC) is active (or one output interface), the maximum number of data transferred is reduced from 8 bit/cycle to 4 bit/cycle. Correspondingly, the bandwidth is reduced from 168MB/s to 79.5MB/s. Note that the MUNTANIALA prototype was designed as a proof of concept. For industrial implementation, not only the die size (and with it the hidden state size on a single MUNTANIALA die) could be scaled up further, but also the used interface could be changed. For example, the High-Bandwidth Interconnect (HBI) offers a high-bandwidth, low-power and low-latency interconnect and is a general standard for die-to-die communication and corresponding IPs are offered by, e.g., Synopsys [62], [63].

4) System I/O Scaling: Every stand-alone accelerator needs external memory to supply the parameters and input data. Therefore, the bandwidth and I/O requirements to such an external memory are an essential design aspect for targeting
combines tightly coupled ARM cores with an FPGA. The FMC connector allows us to control our custom FMC card, i.e., our demonstrator PCB, with the Zynq FPGA. Figure 8 shows our custom FMC card including the grid of $2 \times 2$ MUNTANIALA LSTM accelerator chips, capable of collaboratively performing LSTM inference with 1 layer with a hidden state size of $2 \times N_{H_{MUNTANIALA}} = 192$. The four MUNTANIALA dies are interconnected as shown in Figure 6a.

1) FMC Card: As shown in Figure 8, the FMC card includes not only the four MUNTANIALA accelerators but also two DC/DC converters, multiple power measurement points, and an FPGA Mezzanine Card (FMC) connector. For more fine-grained control and evaluation, the PCB can also be powered from an external power supply. The four MUNTANIALA accelerators were arranged as an upside-down letter “L” to minimize the potential interference caused by unbalanced board connections. The clocks and resets of all accelerators could, if needed, be controlled individually. However, this was not necessary during our evaluation.

2) FPGA-Board Implementation: The processing system (PS) part of the Zynq reads parameters from the SD-Card. Over an AXI interconnect, the simple bare-metal implementation writes the parameters into the BRAM on the programmable logic (PL) part of the Zynq. Once all parameters are stored in the BRAM, the PS notifies a custom HDL controller over the same AXI interconnect. The controller is implementing the same basic handshaking protocol of MUNTANIALA as explained in Section IV-A3 and transfers the BRAM data over the FPGA’s programmable I/Os, which are connected to the corresponding FMC pins.

V. RESULTS

A. Evaluation - Quantization of LSTM

As part of this work, we show that 8 bit quantization of both the activations and the weights is possible for LSTMs for phoneme recognition. We combine the straight-through estimator (STE) for the activations, i.e. $y = \text{quant}(x)$ in the forward pass and $\delta x = \delta y$ in the backward pass where $\text{quant}$ maps $x$ to the closest quantization level, with incremental network quantization (INQ) \cite{48} for the weights. We perform uniform quantization for both, as learned quantization levels would require to decompress the values into a higher precision representation, leading to larger and less energy-efficient compute units. In turn, this excludes more recent quantization methods such as LQ-Nets or TTQ, whose gains are based on learning the quantization levels.

We first fully train the network in high precision before collecting value range statistics and beginning retraining with 255-level STE enabled for all post-activation feature maps and the input features of the network. After convergence, we set the 255 weight quantization levels uniformly across the value range of the weights and start applying INQ. We iteratively increase the share of quantized weights on a 40%, 60%, 80%, 90%, 100% schedule after convergence for the previous share, quantizing them from largest to smallest magnitude.

The feature extraction computes 40 MFCC features plus 1 energy signal on 25 ms of audio every 10 ms. Additionally, the derivatives are taken into account resulting in an input feature vector size of $N_X = 123$. The networks were trained with the Connectionist Temporal Classification (CTC) loss for all 62 phonemes. For the evaluation, the phonemes are merged to the typically used 39 phonemes \cite{64} and evaluated with a greedy decoder. Table [II] summarizes the hyperparameters and quantization schemes used to train the networks. Table [III] shows the achieved accuracy on various network sizes. The quantization only imposes a PER drop of approx. 3% on a network of the size 3L-384NH-123NI (similar to Graves et al. \cite{61}).

For the PyTorch implementation, we use the LSTM class. Therefore, the inference results from the quantized PyTorch network implementation and the Muntaniala accelerator can be slightly different, as our Look-Up tables implementation takes

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**TABLE II**

| Network size | Quantization | Quantization | PER |
|--------------|--------------|--------------|-----|
| L-NH-NI     | Weight       | Activation   |     |
| 3L-384NH-123NI | FP          | FP           | 26.7% |
| 3L-384NH-123NI | 8bit lin. INQ | 8bit STE   | 30.4% |

**TABLE III**

| Network size | Quantization | Quantization | PER |
|--------------|--------------|--------------|-----|
| L-NH-NI     | Weight       | Activation   |     |
| 3L-384NH-123NI | FP          | FP           | 26.7% |
| 3L-384NH-123NI | 8bit lin. INQ | 8bit STE   | 30.4% |
an 8bit input value. In contrast, the Pytorch implementation takes a full-precision input for the activation function. We report a mean squared error (MSE) of $2.965 \times 10^{-5} (\pm 3.691 \times 10^{-5})$ with a maximum squared error of $1.92 \times 10^{-4}$ for the $\tanh()$ and a MSE of $2.229 \times 10^{-5} (\pm 2.177 \times 10^{-5})$ with maximum squared error of $8.57 \times 10^{-5}$ for $\text{sigmoid}()$. These small errors confirm that the LUT activation error is not a major concern for the inference accuracy on the accelerator.

B. MUNTANIALA - LSTM Accelerator

The silicon prototype of a single MUNTANIALA tile as described in Section IV features an LSTM cell of the size $N_H = N_{\text{MUNTANIALA}} = 96$ and was fabricated in UMC 65nm technology. For minimizing leakage, high threshold voltage cells were used. The quadratic die of 1.57mm$^2$ containing a core of 0.93mm$^2$. In order to provide enough bandwidth to every LSTM Unit, the parameter memory is split up into $12 \times$ SRAM banks (a total of 84kB). Figure 9 shows the full operation range from 0.7V up to 1.275V achieving a performance of $30.53 \text{ GOP/s/W}$ in the high-performance operating point and an energy-efficiency of $3.28 \text{ TOP/s/W}$ in the high energy-efficiency operating point. Table LV shows the silicon measurement results (e.g., power, maximal frequency) of MUNTANIALA performed on our in-house Advantest SoCV93000 ASIC tester and compares them with other LSTM / RNN ASIC accelerator designs. Please note that the energy and power results in Table LV relate to core power only and excludes the I/O power.

For the technology node of 65nm MUNTANIALA is more energy-efficient than most other designs, with three exceptions. Firstly, Kadetotad et al. [28] make use of a Hierarchical Coarse-Grain Sparsity (HCGS) weight compression technique by propagating only nonzero weights to the MAC units, allowing them to achieve an energy-efficiency of 8.93 TOP/s/W. These kinds of compression and other sparsity exploiting approaches are orthogonal to the MUNTANIALA design and could be combined with the systolic approach in another work. Yin et al. [29] achieve a energy-efficiency of 5.09 TOP/s/W by using a reconfigurable unit capable of computing CNNs, FCs, and activations for RNNs. Their design follows a reloading procedure where the weights are loaded from an off-chip DRAM where the data are stored in a two-symbol Huffman coding compressed fashion. For running FC or RNN layers, they state a fully saturated I/O bandwidth. However, they lack giving any information on the power consumption caused by this high I/O activity. In contrast, our MUNTANIALA accelerator has a lower I/O activity than a design based on reloading weights (even in a compressed format). The 1-16bit weight configurable UNPU [51] achieves for 8bits an energy-efficiency of $5.32 \text{ TOP/s/W}$ on the FC layers which is comparable to MUNTANIALA. However, for really computing LSTM networks on their architecture, their on-die SIMD core will most likely become a performance bottleneck and as it computes the non-linear activation functions or element-wise multiplications.

To compare our design against other designs in a 40nm technology node, we scaled our 65nm silicon measurements down to 40nm technology [7]. Even with a very conservative scaling where the achieved frequency is kept the same as for the measured frequency in the low-power operating point in 65nm MUNTANIALA is approximately $1.4 \times$ more energy-efficient than the design proposed by Wu et al. [65].

On another aspect, these results are only applicable to tasks requiring reasonably small LSTM networks. Most of the various accelerator designs listed in Table LV have an on-chip SRAM memory size between 10-348kB. Once the task complexity and the corresponding network size increases, these accelerators are forced to reload all parameters, which cripples the throughput or results in heavily I/O-boundness and significantly degrades their energy-efficiency. In this scenario, the systolic design of MUNTANIALA shows its real advantages.

Even though some other works achieve comparable energy-efficiency, MUNTANIALA and CHIPMUNK are more area efficient than all accelerator designs in the same technology node of 65nm, and only Wu et al. [65] design in a more dense technology of 40nm is achieving a higher area efficiency.

FPGA accelerators such as [24] or ESE [20] exploit algorithmic compression and sparsity schemes. Nevertheless, they achieve 1-2 orders of magnitude lower energy efficiency than the ASIC implementations shown in Table HV for the 165 GOP/s/W [24] and 120 GOP/s/W [20] (results for the corresponding dense LSTM network).

To summarize, our MUNTANIALA is, in its stand-alone performance, the most area-efficient LSTM accelerator. Our architecture could benefit from efficiency improvements as achieved by accelerators exploiting algorithmic advancements such as the HCGS compression technique used by the most energy-efficient accelerator [28]. However our main focus and unique contribution is not on core efficiency, but on providing a solution of beyond-die-scaling to tackle larger networks.

C. VAU DA MUNTANIALAS - Systolic Array

Figures 10 and 11 show the power consumption during all phases of computation, as explained in Section IV-A1 and
| Publication       | Supported Networks | Type | Tech. [nm] | Area [mm²] | Memory SRAM [kB] | Quant. [bit] | Nr. of MAC | Voltage [V] | Freq. [MHz] | Power [mW] | Perf. [GOPs] | Energy Eff. [% TOPS/W] | Area Eff. [% GOPs/mm²] |
|------------------|--------------------|------|------------|------------|-----------------|--------------|------------|-------------|-------------|------------|--------------|--------------------------|-------------------------|
| ELSA [26]        | LSTM               | Si   | 65         | 2.62       | 106             | 8-11         | 772        | 1.1         | 322         | 20.4       | 27.0         | 1.32                      | 10.3                    |
| Laika [27]       | LSTM FC            | Si   | 65         | 1.03d      | 32              | 8 (32)       | 8          | 0.575e      | 0.25        | 0.005      | 0.004        | 0.822                    | -                       |
| Kadetodt et al. [28] | LSTM               | Si   | 65         | 7.74d      | 297             | 6,13         | 64         | 1.1         | 80          | 67.3       | 164.95       | 2.45                      | -                       |
| Kadetodt et al. [28] | LSTM               | Si   | 65         | 7.74d      | 297             | 6,13         | 64         | 0.68        | 8          | 1.85       | 24.6         | 8.93                     | -                       |
| OCEAN [30]       | GRU                | Si   | 65         | 10.15d     | 64              | 16           | 32         | 1.2         | 400         | 155.8      | 311.6        | 2.0                      | -                       |
| OCEAN [30]       | GRU                | Si   | 65         | 10.15d     | 64              | 16           | 32         | 0.8         | 20          | 6.6        | 15.58        | 2.36                     | -                       |
| Yin et al. [29]  | CNN FC RNN        | Si   | 65         | 14.4       | 348             | 8/16         | 512/256    | 1.2         | 200         | 386        | 409.6        | 1.06                     | 28.35                   |
| Yin et al. [29]  | CNN FC RNN        | Si   | 65         | 14.4       | 348             | 8/16         | 512/256    | 0.67        | 10          | 4          | 20.4         | 5.09                     | -                       |
| DNPU [32]        | CNN FC RNN        | Si   | 65         | 16.00d     | 256             | 1-16⁷        | -          | 1.1         | 200         | 297        | 891.2        | 2.5f                     | -                       |
| UnPU [31]        | CNN FC RNN        | Si   | 65         | 16.00d     | 256             | 1-16⁷        | -          | 0.63        | 5           | 3          | 22.28        | 5.32f                    | -                       |
| Wu et al. [65]   | LSTM               | P&R  | 40         | 0.45       | 88.5            | 8-16         | 12         | 1.1         | 200         | 6.16       | 24           | 3.89                     | 53.3                    |
| Wu et al. [66]   | BLSTM CNN Synth   |      | 40         | 1.40⁴      | 186             | 8-16         | 16         | 1.1         | 100         | 2.13       | 7.49         | 5.32                     | -                       |
| AIDA [67]        | CNN RNN           | Scaled[4] | 28⁸      | 44.50      | 6400            | 16          | -          | -           | 1000       | 7150.0     | 1474.0       | 0.206                    | -                       |
| iFPNA [68]       | CNN RNN           | Si   | 28         | 2.52d      | 84              | 4-16        | 348        | 1.16        | 125         | 39.4       | 48⁷          | -                        | -                       |
| iFPNA [68]       | CNN RNN           | Si   | 28         | 2.52d      | 84              | 4-16        | 348        | 0.63        | 30          | 3.1        | 11.52⁷       | 0.85                     | -                       |
| EERA-ASK [34]    | BWN LSTM          | Synth | 28        | 0.32d      | >56             | 2-16⁷       | 16         | 0.8         | 400         | 54.0       | 179.2        | 3.318                    | -                       |
| CHIPMUNK [18]    | LSTM               | Si   | 65         | 0.93       | 84              | 8 (16)      | 96         | 1.24        | 168         | 29.03      | 32.3         | 1.11                     | 34.4                    |
| CHIPMUNK [18]    | LSTM               | Si   | 65         | 0.93       | 84              | 8 (16)      | 96         | 0.75        | 20          | 1.24       | 3.08         | 3.08                     | -                       |
| This Work        | LSTM               | Si   | 65         | 0.93       | 84              | 8 (16)      | 96         | 1.275       | 159         | 30.36      | 30.53        | 1.01                     | 32.8                    |
| This Work        | LSTM               | Si   | 65         | 0.93       | 84              | 8 (16)      | 96         | 0.7         | 3.8        | 0.22       | 0.73         | 3.28                     | -                       |
| This Work        | LSTM               | Si   | 65         | 0.93       | 84              | 8 (16)      | 96         | 1.1         | 159         | 13.91      | 30.53        | 2.19                     | -                       |
| This Work        | LSTM               | Si   | 65         | 0.93       | 84              | 8 (16)      | 96         | 0.7         | 3.8        | 0.135      | 0.73         | 5.4                      | -                       |

*a* Peak performance.  
*b* To the best of our understanding.  
*c* Scaled, using the simple model \( \Phi = P(l_{new}/l_{old})(V_{dd,new}/V_{dd,old})^2 \).

*d* Die area as the core area is not available.  
*e* SRAM at 0.7V.  
*f* Design was first synthesized in 45nm and then scaled to 28nm, only 28nm results are available.  
*To the best of our knowledge this applies only to the FC part of RNN and not to the elementwise multiplication, or non-linear activations which are both performed on a SIMD core.  
*The numbers correspond for 8bit configuration.  
*The numbers correspond for 4bit configuration.

shown in Figure 3. Measurements were taken with a high-sensitivity current probe and a Keysight Oscilloscope. Due to size constraints, we use only a 1L-192NH-123NI subset of the fully trained 3L-384NH-123NI network. For the inference, preprocessed input features for samples from the TIMIT dataset were used. MUNTANIALA has separate I/O and core supply pads, each of which have dedicated test points on the demonstrator PCB VAU DA MUNTANIALAS. For every power measurement, we make use of these test points and measure I/O and core power for each chip individually (Figure 10), or for all chips at once (for Figure 11). The various computation and communication phases are highlighted according to the measured active handshakes.

Figure 10 shows the power traces for a MUNTANIALA accelerator at position (0,0) and (0,1), furthermore called slave S(0,0) and master M(0,1). In the first phase, every chip receives the new features by the FPGA. During the reduction phases (green), the output I/O pads of S(0,0) are driving the reduction input I/O pads of M(0,1) (see Figure 6a and section IV-A1). The reduction phases are repeated four times for each gate \( i_t, f_t, o_t \) and the cell candidate state \( \bar{c}_t \).

After the hidden state \( h_t \) computation, the chip at position M(1,1) distributes its partial state to M(0,1). After that M(0,1) distributes its own partial state to S(0,0) and S(1,0). These two hidden state distribution phases are highlighted in blue. After a last reduction round for the FCL, M(0,1) and M(1,1) write out their result back to the FPGA.

In general, the measurements reveal distinct power traces for computation and communication phases, respectively. Notably, the computation phases consume more energy than the I/O communication. In reduction phases (green), S(0,0) outputs partial results that are read by M(0,1), which is shown in our measurements by a power level difference. We measured the energy consumption of the I/O supply of S(0,0) and M(0,1) separately for the duration of the communication phases and report an driving costs of 27.8 \( \mu \text{J} / \text{bit} \) and a receiving cost of 4.7 \( \mu \text{J} / \text{bit} \). This behavior stems from the typically large inverters within the output pad drivers capable of driving high currents for the off-chip wiring. On the other hand, input pads still consume some energy as they have overvoltage protection and some smaller inverters to convert the incoming voltage level of 2.5V to the voltage level 1.2V of the CMOS cells in the...
Fig. 10. Power consumption trace for the core and I/O pads of a MUNTA\textsc{iala} accelerator at position (0,0) and at position (0,1) on the V\textsc{au da MUNTA\textsc{ialas}} demonstrator running at 10 MHz with external power supply of $V_{\text{core}} = 1.2V$, $V_{\text{pad}} = 2.5V$. The network is a 2L-192H-123NI where the input features are divided equally on the two columns.

Fig. 11. Total power consumption for the cores and I/O pads of all four MUNTA\textsc{ialas} on the V\textsc{au da MUNTA\textsc{ialas}} demonstrator running at 10 MHz with external power supply of $V_{\text{core}} = 1.2V$, $V_{\text{pad}} = 2.5V$. The network is a 2L-192H-123NI where the input features are divided equally on the two columns.

core. We note that the measurements of the I/O pad energy are consistent with other published measurements performed on PCBs [69].

Figure 11 shows the total power trace of all four MUNTA\textsc{ialas}. On average, we measure a total core power of 7.87 mW and total I/O power of 1.13 mW over a time of 330 $\mu$s, given a total average system power of 9.00 mW for the V\textsc{au da MUNTA\textsc{ialas}} FMC card computing a network of the size 1L-192NH-123NI at 10MHz, 1.2V core supply, and 2.5V pad supply. An inference on V\textsc{au da MUNTA\textsc{ialas}} consumes 2.97$\mu$J with the output $y_t$ computation and 2.74$\mu$J without the output $y_t$ computation. 11.9% and 12.5% respectively are consumed by the I/O, and 87.5% and 88.1% by the cores.

D. Systolic Array - System Energy Evaluation

For applications that are more demanding than keyword spotting, such as phoneme recognition, a bigger grid than $2 \times 2$ MUNTA\textsc{ialas} dies would be necessary. With the core and I/O power consumption on the V\textsc{au da MUNTA\textsc{ialas}} demonstrator measured in Section V-C, we estimate the overall power consumption for various systolic grid sizes in Table V. For simplicity reasons, we chose $N_I = N_H$ and skipped the configuration phase and the output computation, which depends on $N_O$. We stress that master dies are connected to slaves, other masters, and the FPGA at the same time. This leads to extreme wire lengths compared to normal slave-master wires. To keep our numbers comparable, we removed the energy consumption caused by the additional load of the longer wires to the FPGA. In a real-world scenario, the FPGA could be relocated on the same board and thus have vastly shorter wiring. The inference time is measured and scaled for each operation phase from RTL simulation measurements performed for a systolic grid of 1x1, 2x2 MUNTA\textsc{ialas} chips. The core power is extrapolated from the measurements performed on the demonstrator V\textsc{au da MUNTA\textsc{ialas}} (see Section V-C). The I/O power estimation considers the measured energy cost for driving and receiving data and leakage (see Section V-C) and considers toggling statistics for each interface based on a layer of the trained network.

Whenever the LSTM network fits completely onto one single die, the power is almost entirely dominated by the core (94.1% and 93.9%) because no communication for the reduction and hidden state redistribution is needed. On a systolic grid, these phases contribute to the I/O power. However, they consume less energy than naively reloading all parameters. Note that smaller systolic arrays lead to a higher contribution of the I/O to the total energy consumption, in the worst case up to 12.1%. Running inference on a network of the size 3L-384NH-123NI (similar to Graves et al. [61]) requires a grid of 48 MUNTA\textsc{ialas} dies. The inference takes 1.9ms consuming 193.8pJ at a frequency of 10MHz. If more performance is required, the MUNTA\textsc{ialas} dies could run with up to 159MHz leading to 122$\mu$s per inference. Note that the MUNTA\textsc{iala} prototype was designed as a proof of concept. For industrial implementation, the die size, and with it the hidden state size on a single MUNTA\textsc{iala} die, could be scaled up further before scaling multi-die.

VI. CONCLUSION

We have presented MUNTA\textsc{iala}, a systolically scalable hardware architecture for various types of LSTM neural networks, dramatically reducing the need for parameter reloading and therefore drastically minimizes I/O energy consumption.
Additionally, we presented Vau Da Muntanialas, to the best of our knowledge the first complete hardware demonstration of a multi-chip array for RNNs using our Muntaniala LSTM accelerator. Specifically, we combined four identical Muntaniala accelerators in a grid of 2×2 chips, performing LSTM inference with 192 hidden states in 330 µs with a core power of 7.87 mW and a I/O power of 1.13 mW consuming 2.95 µJ at 10 MHz. Our evaluation shows that running an inference on a 3L-384NH-123NI network (similar to Graves et al. [4]), a grid of 48 Muntaniala dies is needed which can perform inference in 122µs at a frequency of 159MHz, and 1.9ns consuming 193.8pJ at a frequency of 10MHz. We estimate the I/O contribution around 5.8%.

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Gianna Paulin received her B.Sc. and M.Sc. degrees in electrical engineering and information technology from the Swiss Federal Institute of Technology Zurich (ETH Zürich), Switzerland, where she started as a Ph.D. student with the Integrated Systems Laboratory at the beginning of 2019. Her main interests lay in reduced precision deep learning from the algorithmic and hardware acceleration aspect with a focus on time series applications and low power embedded systems.

Francesco Conti received the Ph.D. degree in electronic engineering from the University of Bologna, Italy, in 2016. He is currently an Assistant Professor in the DEI Department of the University of Bologna. From 2016 to 2020, he held a research grant in the DEI department of University of Bologna and a position as postdoctoral researcher at the Integrated Systems Laboratory of ETH Zürich in the Digital Systems group. His research focuses on the development of advanced deep learning based intelligence on top of ultra-low power, ultra-energy efficient programmable Systems-on-Chip – from both the hardware and software perspective. His work has resulted in more than 40 publications in international conferences and journals and has been awarded several times, including the 2020 IEEE TCAS-I Darlington Best Paper Award.

Lukas Cavigelli received the B.Sc., M.Sc., and Ph.D. degree in electrical engineering and information technology from ETH Zürich, Switzerland in 2012, 2014 and 2019, respectively. After spending a year as a Postdoc at ETH Zurich, he has joined Huawei’s Zurich Research Center in Spring 2020. His research interests include deep learning, computer vision, embedded systems, and low-power integrated circuit design. He has received the best paper award at the VLSI-SoC and the ICDSC conferences in 2013 and 2017, the best student paper award at the Security+Defense conference in 2016, and the Donald O. Pederson best paper award (IEEE TCAD) in 2019.

Luca Benini is the Chair of Digital Circuits and Systems at ETH Zürich and a Full Professor at the University of Bologna. He has served as Chief Architect for the Platform2012 in STMMicroelectronics, Grenoble. Dr. Benini’s research interests are in energy-efficient system and multi-core SoC design. He is also active in the area of energy-efficient smart sensors and sensor networks. He has published more than 1’000 papers in peer-reviewed international journals and conferences, four books and several book chapters. He is a Fellow of the ACM and of the IEEE and a member of the Academia Europaea.