LETTER

An ultra-fast and high-precision VCO frequency calibration technique for fractional-N frequency synthesizers

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Abstract A novel VCO auto frequency calibration (AFC) technique is presented in this paper. It provides ultra-fast and high-precision search for an optimum VCO discrete tuning curve among a group of frequency sub-bands in the PLL frequency synthesizer. The calibration circuit consists of a table of frequency (TOF) and a finite state machine (FSM). Asynchronous work of TOF and FSM makes it possible to realize ultra-fast and high-precision calibration simultaneously. TOF affords the high-precision of the calibration and FSM with a high-speed clock offers the ultra-fast search. A 2.8G-3.5GHz Fractional-N PLL incorporating the proposed calibration technique is implemented in 55nm CMOS process. The measured calibration time for a 5-bit capacitor bank is 90ns for a frequency resolution of 203KHz. Such small calibration time significantly reduces the effects of calibration time on the total lock time of the PLL.

key words: Automatic frequency calibration, frequency synthesizer, PLL, CMOS
Classification: Integrated circuits

1. Introduction

It is the basic requirement for a commercial transceiver to be compatible with multi-standard and multi-frequency in modern communication and broadcasting systems. This means that the PLL-based frequency synthesizer should support a wide frequency range. Meanwhile, the input voltage range of voltage-controlled oscillator (VCO) has been reduced as the supply voltage is scaled down by advanced CMOS technologies. Note that the LC-tuned VCO with small input voltage range uses a single tuning curve to cover wide frequency range, which inevitably leads to a large VCO tuning gain (Kvco, expressed in MHz/V) and thus degrade the PLL phase noise severely [1,2,3,4]. To overcome this problem, the most common approach is to employ multiple overlapped tuning curves in the VCO design, which are usually realized by a switched capacitor bank (cap bank) [5,6,7,8]. Fig.1 illustrates the difference between multiple tuning curves and single tuning curve. When dealing with the multiple tuning curves, a VCO auto frequency calibration (AFC) circuit used to find the optimum VCO sub-band is necessary. The time spent on AFC process will be added up to the PLL settling time. This would result in a longer locking process and a reduced data throughput. However, the settling time must be kept at a minimum value for many communication systems especially for frequency-hopping systems. To address this problem, this paper proposes a novel AFC technique with ultra-fast calibration time for integer and Fractional-N PLL synthesizer.

2. Previous AFC techniques

A variety of calibration techniques have been proposed during the last decades, which are mainly be categorized into closed-loop and open-loop calibration methods according to the PLL status during calibration. The open-loop calibration techniques can be further classified as either frequency comparison technique or period comparison technique.

2.1 Closed-loop AFC technique based on Vctrl monitoring

The closed-loop calibration method is shown in Fig.2. During the process of calibration, the loop of PLL remains closed and PLL works toward locking. The control voltage of VCO, Vctrl, is compared against a predefined voltage range (between Vref_high and Vref_low) after settled. The results of comparison will be sent to the
logic control unit that helps to detect the optimum VCO sub-band. If the settled value of $V_{ctrl}$ falls outside the predefined range, it is considered that the PLL does not lock properly, and the VCO sub-band will be adjusted by the logic control unit subsequently. The comparing and adjusting processes will be iterated until the settled value of $V_{ctrl}$ falls into the predefined range, which means that the PLL has locked. Closed-loop calibration techniques are inherently slow as $V_{ctrl}$ must be settled before it is compared by the reference voltage, and the total calibration time is directly correlated with times of comparison and the settle time of $V_{ctrl}$. As a result, the calibration time becomes very long. For example, the calibration time is 2 ms in [7,8].

![Fig. 2 Closed loop AFC technique block diagram](image)

2.2 Open-loop AFC technique based on frequency comparison

The loop of PLL is open while the open-loop calibration works, other than that, the physical quantity detected by calibration circuit is different between closed-loop calibration and open-loop calibration. Closed-loop calibration inspects the control voltage of VCO, while open-loop calibration detects the frequency of VCO. Furthermore, different ways to detect the frequency of VCO separate the open-loop calibration techniques into open-loop calibration based on frequency comparison and open-loop calibration based on period comparison.

Open-loop calibration based on frequency comparison is illustrated in Fig.3. $V_{ctrl}$ is fixed at a half $V_{DD}$ during the process of calibration. Two counters count $f_{REF}$ and $f_{DIV}$ in a certain time. Then, the digital comparator compares the result of counters to decide which is faster, and the logic control unit updates VCO sub-band for the next comparison subsequently. An algorithm embedded in the logic control unit will find the optimum sub-band based on several comparison results. In this approach, the uncertainty of the initial phase between two input signals of counters is the main limitation on the calibration precision. The counters must accumulate quantities of counts to guarantee certain calibration accuracy. Therefore, the calibration time may be longer with higher calibration accuracy. Typical calibration time with frequency comparison is dozens of us, such as 12.6us in [9] and 50us in [10].

![Fig. 3 Open loop AFC technique based on frequency comparison](image)

2.3 Open-loop AFC technique based on period comparison

Different from the frequency based comparison, the period comparison based open-loop calibration technique measures the frequency difference by comparing the periods of two signals. The structure is depicted in Fig.4. In this structure, the periods of $f_{REF}$ and $f_{DIV}$ are changed to voltages by a time-to-voltage converter (TVC). Subsequently, the voltages are compared to decide which input signal has a higher frequency. Then the comparison result will be sent to the logic control unit and processed as the same way as in the open-loop calibration based on frequency comparison. Compare to the open-loop calibration based on frequency comparison, this method only costs several clock cycles before comparing, which shorten the calibration time to several us. The calibration time with period comparison is reduced to several us or sometimes sub-us, such as 4us in [11] and 0.35us in [12] with inter-N PLL.

![Fig. 4 Open loop AFC technique based on period comparison](image)

The typical locking process of PLL, suppose its LC VCO has a 3-bit cap bank, based on closed-loop calibration and open-loop calibration as discussed above are illustrated in Fig.5 respectively. It is observed that the locking process begins with AFC circuit (corresponded to coarse tuning), and subsequent transitions to the loop of PLL locking to a target frequency (corresponded to fine tuning). As can be seen in Fig.5, the AFC calibration time $T_{cal}$ contributes significantly to the total lock time $T_{lock}$. Therefore, reducing $T_{cal}$ is a palpable design issue in the AFC technique. Another veiled design issue is the frequency resolution $f_{res}$ (the frequency-detection...
resolution of AFC circuit). The problem is that $f_{\text{res}}$ must be less than half of the frequency spacing $f_{\text{spacing}}$ between two adjacent sub-band tuning curves of VCO, otherwise, the frequency comparison result would not be precise enough to find the optimum sub-band which is closer to target frequency. During last decades, many works have been done to solve these two problems. Several papers use different algorithms embedded in logic control unit to reduce the calibration time and improve the accuracy of finding suited sub-band. Now, algorithms for finding suited sub-band in common use are linear search [11,13], binary search [9,10,14] and improved binary search [15,16,17]. Many other papers are focused on optimizing frequency comparison circuit to reduce the calibration time and improve $f_{\text{cal}}$. All the previous works use synchronous work method to calibrate the VCO frequency, which ensure AFC circuit’s robustness and veracity. However, it is difficult to realize a small frequency resolution and a short calibration time simultaneously in previous AFC techniques. The synchronous work method works as the AFC circuit does frequency compare, logic judge and sub-band changed step by step in timeline. Multiple frequency comparisons have been done during the process of calibration, thus the calibration time is strongly associated with the time costed by frequency comparison. As we know, the comparing time is negatively correlated to the precision of comparison namely the frequency resolution $f_{\text{res}}$. Therefore, frequency resolution $f_{\text{res}}$ is negatively correlated to the calibration time $T_{\text{cal}}$ in previous AFC circuits. To break the restriction between frequency resolution and calibration time, a novel AFC technique is proposed in this paper.

3. Proposed AFC circuit with fractional-N PLL

Fig.6 shows the block diagram of a Fractional-N PLL employed the proposed AFC circuit. The proposed AFC circuit is comprised of a table of frequency (TOF) and a finite state machine (FSM). The clocks of TOF and FSM are independent, which enables them to not only operate separately but also cooperate together to implement VCO frequency calibration. Generally, FSM or the circuit for searching optimum sub-band works synchronously with frequency comparison circuit or period comparison circuit in previous AFC techniques. It’s the underlying reason that frequency resolution conflict with calibration time. Therefore, asynchronous work of TOF and FSM is a major breakthrough in the proposed AFC technique. The asynchronous structure of proposed AFC circuit cuts off the connection between frequency resolution and calibration time, making it possible to improve the frequency resolution and reduce the calibration time simultaneously.

![Fig. 6 Block diagram of a PLL employed proposed AFC technique](image)

![Fig. 7 Detailed block diagram of the proposed AFC circuit](image)

![Fig. 8 Flowchart of the VCO frequency calibration process](image)

The detailed block diagram of proposed AFC circuit is depicted in Fig.7. The integrated procedure of the proposed frequency calibration technique is based on the flowchart in Fig.8. The intact procedure is separated into three parts including the operate procedure of TOF, the minimum error binary search process of FSM, and the PVT variation detection.

The TOF circuit starts upon a START signal, then, the loop of PLL breaks with the 5-bits sub-band of VCO set to 00000 and the input of loop filter (LPF) is fixed at half...
of $V_{DD}$. The frequency calculator consisting of a timer and a counter begins to record the center frequency of sub-band 00000. The process of frequency calculate will be repeated until all the center frequency of sub-bands 00000–11111 are recorded in the register group. An initialization complete signal is outputted afterwards and the operate procedure of TOF is over. The frequency resolution of frequency calculator is actually the same as the frequency resolution of the whole AFC circuit.

$$f_{\text{resolution}} = \frac{M \cdot f_{\text{REF}}}{K}$$  \hspace{1cm} (1)

As shown in Eq. (1), the frequency resolution is determined by $M$, $K$ and $f_{\text{REF}}$. $f_{\text{REF}}$ is usually limited by the design specification of PLL, thus, only $M$ and $K$ can be set to an arbitrary value. The value of $M$ should be appropriate since a small $M$ need a high speed counter, which will increase the difficulty of circuit design. On the other hand, the value of $K$ should be chosen according to the target frequency resolution. By choosing the proper values of $K$ and $M$, we can achieve a frequency resolution as low as several KHz. For example, if $M$ is 16 with $f_{\text{REF}} = 40$MHz and $K$ is $2^{16}$, then the frequency resolution is 9.8KHz. This is impossible without the new structure. Because in the previous AFC techniques, such a small frequency resolution with a large $K$ as $2^{16}$ means $2^{16}$ clock will be cost by the counter or the timer, which means approximate 1.64ms will be cost for a clock of 40MHz, this is unacceptable as the lock time of PLL is generally limited to 10–100us. However, such a huge time cost is acceptable in the proposed calibration circuit owing to the independence of TOF and FSM.

Once the table of frequency is ok, FSM begins to work upon a calibration enable signal from external. Only FSM works for each calibration after initialization of TOF. FSM searches the optimum sub-band of VCO according to the input fraction divide ratio $N.f$. As depicted in Fig.7, $N.f$ is transformed to a value $f_{\text{target}}$ which can be compared to the value of frequency saved in the register group directly. Once the input fraction divide ratio $N.f$ changed, FSM reads the center frequency of sub-bands from register group and compares it with $f_{\text{target}}$, the comparing results are used to find the optimum sub-band code with the minimum error binary search algorithm which is similar to the algorithm used in [15]. The detailed process of search is shown in Fig.8. In this way, there is no need to wait for the process of frequency comparison or period comparison, which makes the search time namely the calibration time only depends on the number of clock cycles cost in FSM and the clock of FSM. The number of clock cycles depends on the bits of cap tank and design of digital logic. The clock frequency of FSM is $f_{\text{VCO}}$ divide by $M$ instead of $f_{\text{REF}}$ as illustrated in Fig.7. A higher clock frequency of FSM means faster calibration time as the calibration time depends on FSM in the proposed AFC circuit. As a result, the calibration time can be as fast as dozens of ns with $M$ is 32 and $f_{\text{VCO}}$ is 2.8–3.5GHz in the proposed AFC circuit.

The last procedure of proposed frequency calibration technique is the PVT variation detection. The proposed AFC circuit will detect whether the PLL is locked after the optimum sub-band is found by the FSM. If the PLL is unlocked, it means that the table of frequency is wrong due to changed voltage or temperature. Then the unlocked signal can be used to reset TOF and a new table of frequency will be set up according to the changed environment. This step is used to provide a robust calibration in most cases unless the voltage and temperature vary too much within a few msec.

The proposed AFC circuit is applied to a 2.8–3.5GHz fraction PLL. The block diagram of the entire PLL is illustrated in Fig.6. In this design, the reference frequency $f_{\text{REF}}$ is chosen to be 26MHz. VCO is the most important circuit in a PLL and its phase noise greatly affects the overall PLL output noise performance. A Class-C topology has been employed to improve the phase noise for a given power efficiently [23,24,25,26], as depicted in Fig.10. This topology takes advantages of biasing the cross-coupled transistors in Class-C condition to generate more efficient oscillation currents and thereby costs lower power for the same phase noise level. To achieve a small $K_{\text{VCO}}$ and reduce the flicker noise up-conversion, a 5-bit switch cap tank is adopted for coarse frequency tuning while two varactors are used for fine frequency tuning. The objective of using two varactors is to decrease the difference between $K_{\text{VCO}}$ of high operate frequency and low operate frequency of VCO. The PFD
is based on RS flip-flop with dead zone control. The charge pump circuit employs source switch charge pump with improved output impedance [27,28,29] and LPF is a 2nd-order loop filter. The feedback divider is composed of a fixed divide-by-2 prescaler, a dual-modulus prescaler with division ratio of 4 or 5 and a pulse-swallow counter. The sigma-delta modulator is a 3rd-order 21-bit MASH-111 type.

4. Simulation result and measurement result

The proposed AFC circuit with a 2.8–3.5GHz Fraction-N PLL is implemented in a standard 55 nm CMOS process. A micrograph of the proposed circuit is shown in Fig. 11. The Fraction-N PLL with proposed AFC circuit is used in a receiver, the active area of the PLL is 0.562mm² while the AFC circuit is 0.042mm² (120um* 350um). The Fraction-N PLL with proposed AFC circuit consume 13.6mA from a 1.2 supply. The measured PLL output range is 2.8–3.5GHz. The PLL output is divided by 2 before test IO. Fig12 gives the measured phase noise of PLL while VCO oscillates at 3.12GHz. The phase noise is measured by an Agilent N9020A MXA signal analyzer.

![Fig. 11 Chip micrograph of proposed AFC circuit with fraction-N PLL](image)

Table I summarizes the performance of the proposed AFC circuit that is also compared with other published AFC circuits. In particular, the proposed AFC circuit can achieve a calibration time of 90ns that is much less than the other AFC circuits. Furthermore, the proposed AFC circuit can achieve frequency resolution as 203KHz by using a huge K=2^12 while other AFC circuits can only get several MHz. Therefore, the superiority of the proposed AFC circuit based on asynchronous mechanism is valid against other works. Compared to conventional AFC techniques, the proposed AFC circuit achieves high-precision since it costs long time during setting up the table of frequency(TOF), and achieves ultra-fast calibration as the calibration process can work without frequency detection once the TOF is ok. This is quite suitable for those high performance communication systems such as the frequency-hopping system, because PLL always works and the frequency or the sub-band of VCO changes continually in frequency-hopping system. On the other hand, the proposed AFC circuit is not suitable for low power communication systems, such as biomedical electronic system [30,31]. Because PLL may be turned off frequently for low power design, it requires long time to set up the TOF while PLL power on every time, and the set up time of TOF will be added to calibration time in such situation.
5. Conclusion

In this paper, an ultra-fast and high-precision VCO auto frequency calibration (AFC) circuit was presented with a Fraction-N PLL. The proposed AFC circuit is comprised of a table of frequency (TOF) and a finite state machine (FSM). Asynchronous work of TOF and FSM can achieve a calibration time of 90ns for a 5-bit cap bank with a frequency resolution of 203KHz. Such a AFC circuit is quite suitable for frequency-hopping systems.

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