Communication—Room Temperature Photoluminescence Characterization of Impact of Electrical Arcing on Silicon

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Corona discharge-based non-contact capacitance-voltage (C-V) measurement technique has been used for characterization of dielectrics on Si. For corona discharge generation, high voltage is applied to an electrode above dielectrics/Si sample. High voltage electrical discharge and arcing experiments were performed on Si wafers to investigate potential impact (or side effect) on electronic properties of Si wafers. Room temperature photoluminescence (RTPL) spectra from Si samples were measured before and after high voltage direct current (HVDC) discharge and Piezo ignition arcing experiments. Distinctive discharge and arcing footprints were observed in RTPL area maps suggesting modification of electronic properties.

A metal-oxide-semiconductor (MOS) structure is a critical part of a metal-oxide-semiconductor field effect transistor (MOSFET). The voltage (height of potential barrier in the channel) is controlled through the gate electrode on gate oxide (or dielectrics). MOSFET device characteristics are largely dependent on gate oxide or dielectrics. To characterize semiconductor materials and devices, a capacitance-voltage (C-V) measurement (or profiling) technique is frequently used. The applied voltage across the MOS structure is varied and the capacitance is measured. The change of capacitance is then plotted as a function of applied voltage to gain the characteristics of MOS structures, such as oxide thickness, oxide charges, contamination from mobile ions, interface trap density, doping profile and density of electrically active defects. Electrodes are essential parts of the C-V measurement technique.

For in-line monitoring of oxide (or dielectric) film quality, a corona discharge-based, non-contact C-V measurement technique has been introduced and used for years. This technique uses corona discharge in air to place an electric charge on a semiconductor wafer with a thin oxide film and uses the electric charge as an electrode. In order to generate corona discharge by ionization in air, high voltage (~5 kV) is applied to a metallic needle above the semiconductor wafer. Due to the presence of high voltage in close proximity to the semiconductor wafer surface, potential side effects, including material property modification and false interpretation of C-V measurement data often occur.

In this study, we have studied the impact of electrical arcing on Si with native oxide film, and use a room temperature photoluminescence (RTPL) technique to gain insight into potential side effects of corona discharge in close proximity to the Si sample.

Results and Discussion

650 nm and 830 nm laser beam excited RTPL maps for two Si samples, before and after HVDC discharge or Piezo ignition arcing experiments, are shown in Figs. 2 and 3. The RTPL mapping area is 5 mm × 5 mm in 100 μm intervals in X- and Y-directions (51 points × 51 points = 2601 points) were done for square Si samples, before and after the electrical arcing experiments using two different HV sources.

Experimental

A single side polished (SSP), 200 mm diameter p-Si(100) wafer was cleaved into ~50 mm × ~50 mm square pieces. The thickness and resistivity were ~725 μm and ~1–10 Ω·cm, respectively. Si samples from the identical wafer were used for electrical arcing experiments for consistency.

Two types of high voltage (HV) sources for electrical arcing experiments were prepared. They were a rectified high voltage direct current (HVDC) source from a step up transformer and a Piezo ignition driven HV pulse source. The HVDC source puts out ~2000 VDC and the Piezo HV device generates ~4000 V electric pulses. Figure 1 shows photographs of electrical arcing experiments on Si samples with native oxide using the two HV sources. Twenty (20) electrical arcing was randomly done on each Si sample in ~10 mm × ~10 mm area. A metal tip was placed ~2 mm above the Si square sample so that electrical arcing took place when HV is supplied. For the HVDC experiment, HVDC was supplied for ~1000 ms per point and electrical arcing lasted while the HVDC was on. For the Piezo ignition arcing experiment, electrical arcing lasted for a very short period (approximately 1 ms).

RTPL spectra in the wavelength range of 900~1400 nm were measured under 650 nm and 830 nm excitation using a thermoelectrically (TE) cooled spectrograph system (WaferMasters MPL-300). The RTPL system is designed for handling 200 mm and 300 mm diameter Si wafers for industrial applications. A specially designed sample stage capable of adapting ~50 mm × ~50 mm square samples was fabricated and placed on a 300 mm wafer stage. The excitation laser power at the wafer surface was fixed at 20 mW for 650 nm and 50 mW for 830 nm, respectively. The diameter of excitation spots on the Si surface is approximately 200 μm in diameter. The exposure time for RTPL measurements was fixed at 500 ms per point. We have tried to experimentally estimate the local increase of temperature under excitation of RTPL, but it was not successful due to fast heat diffusion through the Si sample and sample stage. We believe that the local heating at the Si surface should be less than 50 °C under both excitation wavelengths. RTPL mapping of 5 mm × 5 mm in 100 μm intervals in X- and Y-directions (51 points × 51 points = 2601 points) were done for square Si samples, before and after the electrical arcing experiments using two different HV sources.

Figure 1. Experimental configurations of (a) HVDC discharge and (b) Piezo ignition arcing onto Si samples.

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Figure 2. 650 nm and 830 nm excitation RTPL area mapping results before and after HVDC discharge (2000 VDC, \(\sim\)1000 ms) onto Si sample. (Mapping area: 5 mm \(\times\) 5 mm in 100 \(\mu\)m intervals).

Figure 3. 650 nm and 830 nm excitation RTPL area mapping results before and after Piezo ignition arcing (\(\sim\)4000 VDC, \(\sim\)1 ms) onto Si sample. (Mapping area: 5 mm \(\times\) 5 mm in 100 \(\mu\)m intervals).

spots per sample. General trends of excitation wavelength dependence of RTPL intensity was in good agreement as reported in previous publications.\(^6\)\(^-\)\(^9\) The 830 nm excited RTPL signal was stronger and had a higher signal-to-noise (S/N) ratio compared to the 650 nm excitation measurements due to its deeper probing depth and relative insensitivity to surface conditions.

The HVDC discharged Si sample did not show any noticeable footprints on the 650 nm excited RTPL map while the 830 nm excited RTPL map showed very distinctive conical footprints for five electrical discharge spots (Fig. 2), which corresponds a typical point-to-plane coronal discharge geometry.\(^10\)\(^,\)\(^11\) The overall RTPL intensity level increased from 985 counts to 1070 counts (approximately 8.6% increase) after the HVDC discharge experiment. On the other hand, the overall 830 nm excitation RTPL intensity level decreased from 6070 counts to 5995 counts (approximately 9.9% decrease) after HVDC discharge experiments. At the five discharge spots, approximately 15% increase of RTPL intensity were measured under 830 nm excitation. RTPL maps for the Si sample before the HVDC discharge experiment showed relatively uniform RTPL intensity across the mapping area. Thus, the conical spots in 830 nm excited RTPL map are from HVDC discharges on the Si sample. The 8.6% increase of average RTPL intensity under 650 nm excitation and the 9.9% decrease of average RTPL intensity under 830 nm excitation, after HVDC discharge experiments, may be due to charge deposition on the native oxide on the Si surface. Since the discharge time was relatively long (\(\sim\)1000 ms), enough charge was generated during HVDC discharge and there was possibly sufficient time for charge migration on the surface. Judging from the deeper probing depth of 830 nm, compared to 650 nm excitation, the conical spots observed in 830 nm excitation RTPL map indicate the HVDC electrical discharge impact into the Si material. This may explain the discrepancy of overall RTPL intensity increase (15% increase) under 650 nm excitation and overall RTPL intensity decrease (9.9% decrease) under 830 nm excitation.

The Piezo ignition arced Si sample showed very distinctive crater shaped footprints for four electrical arcing spots (Fig. 3) under 650 nm and 830 nm excitation RTPL maps. The overall 650 nm excitation RTPL intensity level was increased from 1056 counts to 1113 counts (approximately 5.4% increase) after the Piezo ignition experiment. On the other hand, the overall 830 nm excitation RTPL intensity level was decreased from 6086 counts to 5953 counts (approximately 9.8% decrease) after the Piezo ignition experiment. At the four discharge spots, approximately 20.7% decrease of RTPL intensity from 1994 counts to 1441 counts were measured under 650 nm excitation. Approximately 6.8% increase of RTPL intensity, from 6000 counts to 6410 counts, were measured under 830 nm excitation. The similar discrepancy of overall RTPL intensity increase under 650 nm excitation and overall RTPL intensity decrease under 830 nm excitation was observed. This discrepancy can be explained by the probing depth difference of the excitation wavelength and limitation of the depth of arcing impact from the surface. Due to the higher voltage pulse (\(\sim\)5000 V, \(\sim\)1 ms), the electrical impact was greater and time for charge distribution on
Si surface was limited. As a result, electrical impact was much more localized in-plane compared to the HVDC discharge experiment. The impact of Piezo ignition was also shallower. The crater shaped impact indicates that the HV momentary arcing was not spatially uniform on the Si surface. Doughnut shaped arcing may have been taken place. The shapes of all four arching spots are alike.

Corona discharge-based, non-contact C-V measurement and stress induced leakage current (SILC) measurement spots leave very distinctive measurement marks in RTPL wafer mapping, implying properties of MOS structures may have been altered during electrical measurements.6 Our experimental results also alert us that corona discharge based electrical measurements should be done carefully and interpretation of measured data should be done with caution. In short, a non-contact measurement technique does not guarantee non-destructive or non-invasive nature of results.

Summary
To study potential impact of electrical discharge and arcing on Si surface, high voltage electrical discharge and arcing experiments were performed on Si samples. RTPL spectra were measured before and after HVDC discharge and Piezo ignition arcing experiments. RTPL measurement results under different excitation wavelengths strongly suggest that there might be significant potential impact (or side effects) on the electronic properties of the Si surface and bulk when high voltage is applied, even in air. Distinctive discharge and arcing footprints were observed in RTPL area maps suggesting modification of electronic properties by exposure to HV (or high electrical field), resulting in ionization on the Si surface. The impact of different HV sources on the Si sample was found to be quite different. Although corona charge-based measurement does not cause electric arcing onto the Si surface, our experimental results and previously reported experimental results6 suggest that the corona discharge-based C-V and SILC measurement technique can affect the condition of the Si as indicated by changes in RTPL intensity after exposure to corona discharge and therefore must be used with great caution. Potential change of electronic properties of C-V and SILC measurement areas must be checked using RTPL measurements before interpreting the corona charge-based measurements. Corona charge deposition conditions need to be optimized not to cause electronic property change at or near the corona charge-based electrical measurement area.

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