A voltage-controlled topological-spin switch (vTOPSS) that uses a hybrid topological insulator-magnetic insulator multiferroic is presented that can implement Boolean logic operations with sub-10 aJ energy-per-bit and energy-delay product on the order of $10^{-27}$ Js. The device uses a topological insulator (TI), which has the highest efficiency of conversion of electric field to spin torque yet observed at room temperature, and a low-moment magnetic insulator (MI) that can respond rapidly to a given spin torque. We present the theory of operation of vTOPSS, develop analytic models of its performance metrics, elucidate performance scaling with dimensions and voltage, and benchmark vTOPSS against existing spin-based and CMOS devices. Compared to existing spin-based devices, such as all-spin logic and charge-spin logic, vTOPSS offers 100× lower energy dissipation and (40–100)× lower energy-delay product. With experimental advances and improved material properties, we show that the energy-delay product of vTOPSS can be lowered to $10^{-29}$ Js, competitive against existing CMOS technology. Finally, we establish that interconnect issues that dominate the performance in CMOS logic are relatively less significant for vTOPSS, implying that highly resistive materials can indeed be used to interconnect vTOPSS devices.

I. INTRODUCTION

Spin-based logic and memory devices use nanomagnets as digital spin capacitors to store and manipulate information [1]. Typically, spin-polarized electrical currents or magnetic fields are used to control the magnetization vector of nanomagnets while reading and writing information [2]. Compared to their charge-based counterparts, spin-based devices offer non-volatility of information and superior logical efficiency, i.e. fewer devices to implement a given Boolean function [3]. However, the majority of spin-based devices suffer from high energy dissipation resulting from a large electric current density on the order of $10^6$ A/cm$^2$ required to reorient the magnetization vector [4,5]. Such large current densities not only lead to excessive Joule heating in the device, but could cause electromigration issues in metallic interconnects [6]. At the same time, reversal of metallic ferromagnetic bodies using anti-damping spin-transfer torque (STT) proceeds on a timescale on the order of 100’s of picoseconds to a few nanoseconds [7]. As such, existing spin-based devices have an energy-delay product that is (1,000-10,000)× larger than that of their CMOS counterparts [8].

To harness the full potential of spintronics technology, it is imperative to develop methods for energy-efficient and fast manipulation of the magnetic order parameter. Actuation methods, such as voltage control of magnetic anisotropy and coercivity, use of magnetoelectric and exchange coupling in multiferroic/ferromagnetic heterostructures, and charge carrier density mediated ferromagnetism control, have been investigated [9,10]. Yet, these effects are generally weak at room temperature, which limits their practical use. For example, full 180° reversal of a ferromagnet via the magnetoelectric effect requires the assistance of electric currents or magnetic fields or can be accomplished using the resonant pulsed switching mode that requires precise pulse timing [11–14]. Magnetoelastic effects that are used to tune the magnetic properties of thin films via epitaxial strain or piezoelectric substrates are generally observed in small aspect ratio nanomagnets [15,16]. However, in high aspect ratio nanomagnets it is difficult to use strain effects to tune the magnetic properties.

A promising research direction is “topological spintronics” that has been driven by the demonstration of efficient room-temperature spin-charge conversion in heterostructures with a topological insulator (TI) interfacing a ferromagnetic (FM) metal [17]. The key property responsible for this advance is the combination of large spin-orbit coupling (SOC) strength and time-reversal symmetry that leads to the formation of helical Dirac surface states possessing an inherent spin-momentum locking [18–21].
The distinctive feature of TIs is that even without carriers near the chemical potential in bulk, the spin Hall conductivity can be finite and significantly larger than that of heavy metals such as Pd, Pt, W \cite{22, 24}.

Here, we utilize electric fields across a TI resulting in a coherent transport of spins across the material to generate a spin torque on the magnetization of an adjacent magnetic insulator (MI) layer \cite{25}. Unlike FM metal, there is no shunting of electric current in the MI layer and current is restricted to flow on the surface of the TI layer. Furthermore, the MI can induce a gap in the TI surface states, rendering the TI surface state insulating, which is (counterintuitively) beneficial to the device operation. The spin-based device, voltage-controlled topological-spin switch (vTOPSS), decouples the elements of a magnetoelectric material \cite{26}, allowing us to simultaneously optimize the choice of both TI and MI materials, thereby enabling ultra-low-energy computing.

One of the most important properties of the MI layer is its low damping \cite{27, 28} which is highly desirable in device applications where switching is realized through magnetization precession, as in vTOPSS. The remainder of this paper is organized as follows. In Section II, the physics of operation of vTOPSS is presented. In Section III, analytic models of performance metrics of vTOPSS are presented followed by benchmarking results against existing spin- and charge-based devices in Section IV. In Section V, implementation of universal Boolean logic gates and the logical efficiency of vTOPSS resulting from its innate polymorphism are highlighted. Section V summarizes the key findings of this work while also offering an outlook on future research directions.

II. PHYSICS OF OPERATION

The evolution of the wave functions of the full bands of the TI, under the influence of an electric field, produces coherent transport of spins across the material \cite{29}, which can be used to efficiently manipulate the magnetization state of an adjacent magnetic layer \cite{30}. The charge Hall conductivity and bulk dissipative charge currents vanish or are small in the TI, but the spin Hall conductivity is finite and can be much larger than that of a large-SOC metal \cite{31}. A TI has the highest efficiency of conversion of electric field to spin torque yet observed at room temperature \cite{32, 33}. Hybrid TI-MI structures decouple the constituent features of a multiferroic material, allowing independent optimization of both components of the response of magnetization to an electric field, i.e. generation of spin torque from the electric field and response of the magnetic moments to the spin torque.

The total Berry curvature of a full band measures the integrated correlation between spin and orbital degrees of freedom. For a so-called trivial insulator this correlation integrates to zero across the entire full band. Thus, if at one region of the Brillouin zone the wave functions of the band have spin and orbit correlated preferentially parallel, there will be another region of the zone in which the wave functions are correlated preferentially antiparallel. An example is the valence band in a trivial direct-gap semiconductor, such as GaAs, which is of p-orbital character, for which the wave functions near the valence maximum are heavy hole states, with spin and orbit degrees of freedom parallel, whereas at energies below the split-off energy the spin and orbit degrees of freedom are preferentially oriented antiparallel.

TIs differ from these trivial insulators in that this spin-orbit correlation does not integrate to zero. The spin-orbit correlation is described quantitatively by the Berry curvature of the band, and thus the electronic ground in a TI possesses a nonzero integrated Berry curvature. The spin Hall conductivity in the clean static limit, evaluated as the linear response of the spin current to an electric field using the Kubo approach, depends directly on the Berry curvature \cite{34}:

$$\sigma_{yx} = \frac{e\hbar}{V} \sum_k f_{nk} \Omega_{nk}^z,$$  \hspace{1cm} (1)

where $e$ is the elementary charge, $\hbar$ is the reduced Planck’s constant, $V$ is the volume of the system, $k$ is the crystal momentum, $n$ is a band index, and is $\Omega_{nk}^z$ is the Berry curvature:

$$\Omega_{nk}^z = 2 \sum_{n' \neq n'} \text{Im} \frac{\langle u_{nk}|j_y|u_{n'k}\rangle \langle u_{n'k}|u_z|u_{nk}\rangle}{(E_{nk} - E_{n'k})^2}.$$  \hspace{1cm} (2)

Here, the Fermi-Dirac function $f_{nk}$ ensures that the sum is over filled states, corresponding to all the filled bands at zero temperature. The spin current and velocity operators, $\hat{j}_i^s$ and $\hat{v}_i$, are

$$\hat{j}_i^s = \frac{\hbar}{2} \left( \hat{v}_i \sigma_j + \sigma_j \hat{v}_i \right), \quad \hbar \hat{v}_i = \nabla_k \hat{H},$$  \hspace{1cm} (3)

where $\sigma_j$ is the spin operator along direction $j$, and $\hat{H}$ is the Hamiltonian of the material. The current and velocity operators are evaluated between the states with Bloch functions $u_{nk}$ and $u_{n'k}$, and energy $E_{nk}$.

As the integrated Berry curvature of the full band does not vanish for a TI, and the spin Hall conductivity is directly related to the total Berry curvature of the filled states of the TI, even without any carriers near the chemical potential in bulk, the spin Hall conductivity does not vanish. This characteristic clearly identifies the spin current involved as non-dissipative until it encounters other regions, such as an interface. Here we take advantage of this localized effect to drive vTOPSS shown in Fig. 1.

The device relies on the accumulation of spins at an interface, originating from the voltage ($V_{in}$) applied to the TI. The spin Hall conductivity for a TI can be as large as (or larger than) that of a large SOC metal, but the dissipative longitudinal charge current will vanish for the TI. Thus, a TI provides the advantages of a large spin Hall conductivity, but without the intrinsic dissipation of a metallic material. The resulting spin current produced by the electric field on the TI generates a torque on the spin in the magnetic material through exchange coupling or anti-damping torque. In the case of effective exchange
coupling, the torque forces the magnetization to precess and eventually reverse. 

The spin-current density created by applying an electric field $E_{\text{TI}}$ is:

$$J_s = \sigma_{yz} E_{\text{TI}}.$$  \hspace{1cm} (4)

The resulting magnetization dynamics of the ferromagnetic insulator can be described using the Landau-Lifshitz-Gilbert-Slonczeewski equation in a macrospin limit [33]:

$$\frac{1}{\gamma} \frac{dm}{dt} = -\mu_0 m \times H_{\text{eff}} - \alpha \mu_0 m \times (m \times H_{\text{eff}}) - c_{\text{ex}} j_x m \times \dot{p} + j_y m \times (m \times \dot{p}),$$  \hspace{1cm} (5)

where $m$ is a unit vector in the magnetization direction, $\gamma = \gamma/(1 + \alpha^2)$, $\gamma$ is the gyromagnetic ratio, $\mu_0$ is the vacuum permeability, and $\alpha$ is the Gilbert damping coefficient. The last two terms describe a spin torque from a spin-current polarized in a direction $\vec{p}$, generally perpendicular to the electric field and in the plane of the TI/MI interface. $J_x = 2M_t m_{\text{MI}} j_x$, where $M_t$ is the magnetization of the MI layer, and $t_{\text{MI}}$ is its thickness. (We assume a thin ferromagnetic insulator with area in contact with the topological insulator $A_{\text{int}}$ and thickness $t_{\text{MI}}$.) The first spin-torque term describes the precession of the magnetization about the spin-polarization direction, with an exchange coupling parameter $c_{\text{ex}}$. (For an estimate of this parameter see Ref. [30].) This term is often referred to as a field-like interaction. The second spin-torque term characterizes the Slonczewski “anti-damping” torque, a torque that can oppose the dissipative term (the second term on the right hand side of the equation), leading to precessional magnetization dynamics and switching.

The effective field $H_{\text{eff}}$ characterizes the magnetic anisotropy of the free layer. For a uniaxial magnet with easy magnetization direction in the $y$-direction

$$H_{\text{eff}} = 2E_0 m_y / (\mu_0 M_s V_{\text{MI}}),$$  \hspace{1cm} (6)

where $E_0$ is the energy barrier to magnetization reversal and $V_{\text{MI}}$ is the volume of the MI layer. The magnetization switching mechanism depends on the orientation of the magnetic easy axis relative to the direction of spin-polarization $\vec{p}$. When the two are orthogonal, the switching can occur due to precession about the spin-polarization direction and be very fast (< 100 ps) [36-38]. However, typically precise electric pulse timing is required to ensure switching. When the spin-polarization is collinear with the easy-axis direction the switching is slower but the pulse time is not a critical parameter; in general, the write error rate decreases monotonically with either increasing pulse amplitude or duration [39]. The electric field polarity determines the sense of reversal, i.e. from $m_y = 1$ to $-1$ and vice-versa. The threshold spin current density for anti-damping spin-current switching follows from Eqn. (5), $J_{s,\text{th}} = 4\alpha E_0 / A_{\text{int}}$. The antidamping switching mechanism will be considered in the analysis presented in Sec. [11].

As shown in Fig. [1] the readout in vTOPSS is accomplished by exchange coupling a small section of the MI layer (storing information) to the free layer of a magnetic tunnel junction (MTJ), which could operate with sub-100 mV supply voltages ($V^+/V^-$) to generate sufficient output voltage ($V_{\text{out}}$) with intrinsic gain and the ability to fan-out. This separates the robust information storage aspect from the transduction within a hybrid magneto-electric device, allowing one to probe the magnetization without disturbing the state.

![FIG. 1. Copy/invert functions implemented using vTOPSS.](image)

In this section, analytic models of latency and energy

**III. PERFORMANCE MODELING**

In most spin-based devices, the operating speed is limited by the time it takes to reverse the magnetization of the metallic ferromagnetic layer, which is typically on the order of a nanosecond. Spin-based devices using spin-Hall effect in heavy metals, such as Pt, Pd, W, require large electric fields in the heavy metal to generate sufficient electric current to cause STT switching of nanomagnets. The spin-based device, vTOPSS, takes advantages of the unique properties of TI and MI material systems to achieve the following criteria for energy-efficient logic applications: (i) non-volatility of operational states, (ii) fully voltage-driven switching of the MI magnetization with voltages < 100 mV, (iii) absence of dissipative electric currents during the write process, and (iv) ultra-fast switching of the MI magnetization due to its low Gilbert damping.

In this section, analytic models of latency and energy
dissipation of vTOPSS are presented followed by a comparison of metrics against those of existing spin-based and charge-based devices. Analytic models are obtained for a uniaxial MI layer subject to anti-damping STT resulting from spin accumulation at the TI-MI interface when the TI is subject to an external electric field. Multidomain effects in the MI layer are neglected to arrive at closed form solutions of performance metrics that can provide insight into the device limits and opportunities.

A. Device Latency

To estimate vTOPSS latency, the rate of spin accumulation at the TI-MI interface must be calculated. For a given electric field ($E_{\text{TI}}$) and spin Hall conductivity ($\sigma_{\text{SHC}}$) of the TI layer, the accumulation rate of interface spins is given as

$$\frac{dn_{\text{spins}}}{dt} = \frac{\sigma_{\text{SHC}}}{\hbar/2} E_{\text{TI}} = \frac{\sigma_{\text{SHC}}}{\hbar/2} \frac{V_{\text{in}}}{W}, \quad (7)$$

where $V_{\text{in}}$ is the voltage applied across the TI layer, and $W$ is the width of the TI layer, measured along y-axis in Fig. 1. For a given efficiency, $\varepsilon$, of coupling of spins at the TI-MI interface and the magnetic moment of the MI layer, the following condition is satisfied:

$$N_{\text{spins,MI}} = \varepsilon n_{\text{spins}} A_{\text{int}}. \quad (8)$$

Here, $N_{\text{spins,MI}}$ is the total number of spins in the MI layer subject to spin torque due to the interface spin accumulation, and $A_{\text{int}}$ is the interface cross-sectional area. The total number of spins in a magnetic body is given as

$$N_{\text{spins,MI}} = \frac{M_{b}V_{\text{MI}}}{\mu_{B}} = \frac{2E_{b}}{\mu_{B}H_{K}}, \quad (9)$$

where $H_{K}$ is the anisotropy field of the MI layer, and $\mu_{B} = 9.3 \times 10^{-24}$ J/T is Bohr magneton. Assuming anti-damping switching of the MI layer in the ballistic limit ($J_{\text{MI}} \gg J_{\text{th}}$), the rate of spin accumulation at the interface will balance the rate of magnetization reversal of the MI layer. Here, $J_{\text{MI}}$ is the input spin current density in the MI layer, while $J_{\text{th}}$ is the threshold spin current density required for STT-induced magnetization reversal. In this case, the reversal time, $\tau$, of the MI layer is

$$\tau = \frac{N_{\text{spins,MI}}}{\varepsilon A_{\text{int}} dn_{\text{spins}}/dt}. \quad (10)$$

Considering that the TI and MI widths are identical and using Eqn. (7) and Eqn. (8), the above equation simplifies to

$$\tau = \frac{2E_{b}}{\mu_{B}H_{K} L \left( \frac{\sigma_{\text{SHC}}}{\hbar/2} \right) V_{\text{in}}}, \quad (11)$$

where $L$ is the length of the TI layer (measured along x-axis in Fig. 1). This equation shows that for fixed MI properties and switching voltage, the device latency is inversely proportional to the length scale. An increase in $L$ while fixing $E_{b}$ and $H_{K}$ values requires reducing the MI layer thickness. Therefore, the TI-MI interface area ($A_{\text{int}} = WL$) increases for the same volume of the MI layer, which increases the interface spin accumulation and the strength of STT acting on the MI layer.

The device delay can also be reduced by lowering the MI energy barrier, $E_{b}$; however, this comes at the cost of reduced thermal stability of the MI layer. An increase in $\sigma_{\text{SHC}}$ of the TI layer and the spin-coupling efficiency are particularly beneficial toward reducing the device latency. While the total latency of the device must include the time needed to charge/discharge the device capacitance (sum of interconnect and TI input capacitance), our analysis presented in Sec. III B shows that the dominant time constant is due to the rate of spin accumulation at the TI-MI interface.

Apart from the device geometry and material properties, a critical parameter affecting the device dynamics is the switching voltage, $V_{\text{in}}$. This voltage must be enough to ensure that the spin current input to the MI layer exceeds the critical spin current ($J_{\text{th}}$) for deterministic reversal. Lower-$\alpha$ MI materials are advantageous to reduce $J_{\text{th}}$ and permit low-power spin-based devices. The minimum switching voltage is found by considering

$$J_{\text{MI}} = J_{\text{th}} = d(N_{\text{spins,MI}}/A_{\text{int}})/dt.$$ Using Eqn. (7) and Eqn. (8), we obtain

$$V_{\text{in}}^{\text{min}} = \frac{2\alpha E_{b}}{\varepsilon L\sigma_{\text{SHC}}}. \quad (12)$$

Assuming $V_{\text{in}} = \xi V_{\text{in}}^{\text{min}}$ ($\xi > 1$) and substituting in Eqn. (11), we see that $\tau = \tau_{D}/(2\xi)$, where $\tau_{D} = 1/(\gamma H_{K} L)$ is the natural time scale for the dynamics of uniaxial nanomagnets subject to anti-damping torque. Considering $\alpha = 10^{-4}$, $E_{b} = 30kT$ ($kT = 25.8$ meV at room temperature), $\varepsilon = 0.1$, $L = 10$ nm, $\sigma_{\text{SHC}} = 1000h/2e\Omega$ cm$^{-1}$, $V_{\text{in}}^{\text{min}} \approx 0.75$ mV. For $V_{\text{in}} = 100$ mV, corresponding to $\xi = 133$, and $H_{K} = 0.1$ T, $\tau \approx 210$ ps.

B. Minimum read voltage and energy dissipation

In the vTOPSS device, the read unit is an MTJ stack coupled to the MI layer as depicted in Fig. 1. The read voltages are labeled as $V^{+}$ and $V^{-}$ and have the same magnitude but opposite polarity. That is, $V^{+} = V_{\text{read}}$ and $V^{-} = -V_{\text{read}}$, where $V_{\text{read}}$ is the magnitude of the voltage applied to the MTJ to read the magnetization state of the MI layer. The supply voltages are clocked such that the writing and reading of a given logic stage happen in concurrent cycles. The voltage generated at the output node $V_{\text{out}}$ of the $n^{th}$ stage drives the write unit of the $(n + 1)^{th}$ stage. The output voltage must meet the $V_{\text{in}}^{\text{min}}$ criterion in Eqn. (12).

The equivalent circuit model of vTOPSS is shown in Fig. 2. The interconnect is modeled as a lumped RC network with $R_{\text{int}}$ and $C_{\text{int}}$ representing the total interconnect resistance and capacitance, respectively. For a given interconnect length of $L_{\text{int}}$, $R_{\text{int}} = r_{\text{int}} L_{\text{int}}$ and $C_{\text{int}} = c_{\text{int}} L_{\text{int}}$, where $r_{\text{int}}$ and $c_{\text{int}}$ are the per-unit-length interconnect resistance and capacitance, respectively. The conductances of the parallel and anti-parallel
configuration of the free and fixed layer in the MTJ stack are denoted as $G_P$ and $G_{AP}$, respectively. These conductances are typically determined from the tunneling magnetoresistance (TMR) and resistance-area (RA) product measurements of the MTJ structure. TMR is given as $(G_P - G_{AP})/G_P$, while RA is given as $A_{MTJ}/(G_P + G_{AP})$, where $A_{MTJ}$ is the cross-sectional area of the MTJ stack. For all results reported in this paper, $A_{MTJ} = A_{int}$, unless otherwise specified.

The capacitance of the TI layer is $C_{TI}$, while the leakage of electric current through the TI is modeled using the leakage conductance $G_{TI}$. The TI capacitance is given as $C_{TI} = \epsilon_r \epsilon_0 A_{int}/W$ where $\epsilon_0 = 8.85 \times 10^{-12}$ F/m and $\epsilon_r$ is the static relative dielectric permittivity of the TI layer. For Bi$_2$Se$_3$, $\epsilon_r \approx 110$ [42]. The leakage conductance $G_{TI} = G_{sheet} L/W$, where $G_{sheet} = \epsilon n_\mu$ [43]. Here, $n_\mu$ and $\mu$ correspond to the density and the effective mobility of surface carriers, respectively.

The leakage in the TI layer results from the conductance of topologically trivial and non-trivial surface states as well as the bulk conductivity resulting from unavoidable self-doping effects [44]. Attempts to suppress bulk conductivity include thinning the TI layer until the surface contribution dominates or utilizing compensation doping to suppress free carriers in the bulk. For example, in Ref. [45], copper doping is used in Bi$_2$Se$_3$ films to fully suppress bulk states and decouple the surface states in samples as thin as 20 nm. A sheet resistance of $\approx 1000 \Omega/\square$ at room temperature (300 K) is experimentally measured in a 20-nm thick Bi$_2$Se$_3$ film, while the sheet resistance increases to 1400 $\Omega/\square$ and 3000 $\Omega/\square$ in film thicknesses of 10 nm and 2 nm, respectively in the same sample. More recently, sheet resistances on the order of 10’s of k$\Omega/\square$ have been experimentally achieved at room temperature in 5-60 nm thick Bi$_2$Se$_3$ films grown on insulating In$_2$Se$_3$/(Bi$_{0.5}$In$_{0.5}$)$_2$Se$_3$ buffer layer on sapphire substrates [46].

To obtain the energy dissipation of vTOPSS, Kirchoff’s laws are first solved in the circuit shown in Fig. 2, which gives the following time-domain response of output voltage:

$$V_{out}(t) = V_I \left(1 - e^{-\frac{t}{\tau_{eq}}} \right) + V_I e^{-\frac{t}{\tau_{eq}}},$$

(13a)

$$V_I = \frac{(G_P - G_{AP})V_{read}}{G_P + G_{AP} + R_{int} G_{TI} (G_P + G_{AP})},$$

(13b)

$$\tau_{eq} = \frac{(1 + R_{int} (G_P + G_{AP})) C_{out}}{G_P + G_{AP} + R_{int} G_{TI} (G_P + G_{AP})}.$$  

(13c)

Here, $V_I$ and $V_I$ are the final and initial voltages, respectively, at the output node. At the end of the read/write cycle, the voltage $V_{out}$ is reset to 0 V. Therefore, for all results presented in this paper, $V_I = 0$. The minimum read voltage required on the MTJ stack to ensure correct functionality is obtained by equating Eqn. [12] and Eqn. [13]. Assuming that the read pulse duration is significantly greater than $\tau_{eq}$, $V_{min}^{read}$ is given as

$$V_{min}^{read} = \frac{2 \alpha E_0}{\varepsilon L \sigma_{SHC}} \left[ \frac{(G_P + G_{AP})(1 + R_{int} G_{TI})}{G_P - G_{AP}} \right].$$  

(14)

In Fig. 3, the minimum read voltage ($V_{min}^{read}$) and the minimum input voltage ($V_{in}^{min}$) required for magnetization reversal are plotted as functions of the efficiency of spin coupling at TI-MI interface for various values of the spin Hall conductivity. The effect of TMR on $V_{min}^{read}$ is examined in the inset plot. Our results show that sub-20 mV input voltages corresponding to sub-50 mV read voltages will enable device functionality even when the coupling efficiency is as low as 10%. As expected, an improvement in coupling efficiency, spin Hall conductivity, and the TMR can lower the required supply voltage to only a few milli-volts. Such a low switching voltage to reverse the magnetization of magnetic materials is key toward enabling ultra-low-energy operation using vTOPSS.

The total energy dissipation consists of the energy required to charge and discharge the output node voltage, $V_{out}$, and the direct path conduction between $V^+$ and $V^-$. Assuming that the read phase lasts for a time duration of $\tau_{pulse}$, the energy supplied by the voltage $V^+$ is given by the following integral:

$$E_{read} = \int_0^{\tau_{pulse}} dt I_1(t) V^+ = \int_0^{\tau_{pulse}} dt (I_2(t) + I_3(t)) V^+, \quad (15)$$

where $I_j(t) (j = 1,2,3)$ denotes the electrical current flowing in the $j$th branches as shown in Fig. 2. $I_2(t) = G_{AP}(V_I(t) - V^-)$, and $I_3(t) = C_{out} dV_{out}(t)/dt + G_{TI} V_{out}(t)$. Here $C_{out} = C_{TI} + C_{int}$ is the net capacitive loading at the output node. By substituting $V_I(t)$ in terms of $V_{out}(t)$ and using Eqn. [13], the energy dissipation of the circuit is given per Eqn. [16]. The term $E_{read,1}$ in Eqn. [16] is dominated by the energy dissipation due to MTJ leakage, while $E_{read,2}$ is largely due to energy consumed in charging and discharging the output.
minimum read voltage with TMR for various ε values. For a TI length of 10 nm, read voltage of 50 mV, can be reduced by increasing the read voltage on the function of the read voltage. Simulation parameters are (copper/low-energy-delay product (EDP). For CMOS logic at the 2020 impact of device design on vTOPSS latency, energy, and efficiency. To ensure that the MI reversal delay is sub-1 ns, the area of the interface between the TI and MI layers must be increased. As shown in the inset plot of Fig. 4 by increasing the length of the TI layer to 100 nm, a delay of only a few 100 ps for vTOPSS is achievable. With all other parameters fixed, an increase in TMR increases the input voltage across the TI layer, reducing the latency of MI reversal. Another important material property is the spin Hall conductivity (σSHC) of the TI layer—an increase in σSHC increases the interface spins available to drive the MI magnetization, thereby reducing its delay.

FIG. 3. Minimum input and read voltages versus the spin coupling efficiency in vTOPSS for various values of the spin Hall conductivity of the TI layer (σSHC). Simulation parameters: α = 3 × 10⁻³, E₀ = 30kT, TMR = 1.4, L = 10 nm, W = 100 nm, RintG_TI ≪ 1. Inset plot shows the scaling of minimum read voltage with TMR for various RintG_TI product values. Note that the area of the MTJ and the RA product values do not affect the value of V_read and V_in.

IV. PERFORMANCE BENCHMARKING

To benchmark the performance of vTOPSS against CMOS and existing spin-based devices, we first study the impact of device design on vTOPSS latency, energy, and energy-delay product (EDP). For CMOS logic at the 2020 ITRS technology node, the effect of local interconnects (copper/low-κ) on the performance metrics is considered. We also identify a set of optimal material parameters of vTOPSS to achieve an EDP on the order of 10⁻²⁹ Js for it to be competitive against CMOS logic.

A. Energy and latency

Figure 4 shows the latency of vTOPSS plotted as a function of the read voltage. Simulation parameters are noted in the figure caption. The dominant time constant in vTOPSS is the magnetization reversal delay, which can be reduced by increasing the read voltage on the MTJ or by improving the efficiency of coupling of TI-MI spins. For a TI length of 10 nm, read voltage of 50 mV, and ε = 0.5, the latency of vTOPSS is ≈ 2 ns, while the latency reduces to ≈ 1 ns for perfect spin coupling efficiency. To ensure that the MI reversal delay is sub-1 ns, the area of the interface between the TI and MI layers must be increased. As shown in the inset plot of Fig. 4 by increasing the length of the TI layer to 100 nm, a delay of only a few 100 ps for vTOPSS is achievable. With all other parameters fixed, an increase in TMR increases the input voltage across the TI layer, reducing the latency of MI reversal. Another important material property is the spin Hall conductivity (σSHC) of the TI layer—an increase in σSHC increases the interface spins available to drive the MI magnetization, thereby reducing its delay.

Figure 5 shows the scaling of vTOPSS energy dissipation with the read voltage applied on the MTJ. As the read voltage reduces the energy dissipation also reduces. However, the energy dissipation of vTOPSS decreases linearly with V_read. At a read voltage of 50 mV, the energy dissipation of vTOPSS for infinite sheet resistance (gapped surface states and negligible bulk conductivity) is as low as 10 aJ. This energy dissipation increases by 12 × for Bi₂Se₃ thin films with a sheet resistance of 1 kΩ/□ measured at room temperature in Ref. [15]. Figure 6 shows the contribution of various terms in Eqn. (16) to the overall vTOPSS energy dissipation. In the best-case scenario with negligible TI conductance, the en-
energy dissipation is mainly dominated by the first term in Eqn. 16. This term signifies the importance of leakage through the MTJ stack and can be reduced by utilizing material systems with a much larger TMR ratio. As the leakage through the TI increases, energy dissipation begins to be dominated by the third term in Eqn. 16. Note that even if $G_{\text{TI}} \rightarrow 0$, the contribution of the third term in Eqn. 16 remains finite due to the presence of $G_{\text{AP}}$. Finally, the contribution of the second term in Eqn. 16 remains insignificant as long as $R_{\text{int}} G_{\text{TI}} < 1$. This condition is typically satisfied for local metallic interconnects considered for results in Fig. 4. The effect of interconnects on energy dissipation is further discussed in Sec. IV C.

B. Energy-delay product (EDP)

As shown in Figs. 3 and 4 there exists an energy-delay tradeoff in vTOPSS with respect to $V_{\text{read}}$. However, this trade-off in vTOPSS has a subtle difference when compared against CMOS technology. In CMOS logic, energy dissipation scales quadratically with the supply voltage ($E_{\text{CMOS}} \propto V_{DD}^2$). In vTOPSS, however, energy dissipation displays a linear dependence on the read voltage. This is because leakage through the TI conductance and the MTJ conductance dominate vTOPSS energy (see results and discussion related to Fig. 3). Since, $\tau_{\text{pulse}} \approx \tau \propto V_{\text{read}}^{-1}$ and $E_{\text{read}} \propto V_{\text{read}}$, a constant EDP with respect to $V_{\text{read}}$ is obtained in vTOPSS, if all other design parameters were kept the same. For the results reported in Fig. 3 the EDP increases from $1.2 \times 10^{-27}$ Js to $1.2 \times 10^{-26}$ Js as the sheet resistance of the TI layer reduces (or the TI conductance increases).

The EDP can be reduced by designing junctions that exhibit a large TMR—an increase in TMR at a fixed RA product value reduces both the switching delay and the energy dissipation. The scaling of EDP with TMR in vTOPSS can be expressed as $E_{\text{DP}} \propto 1/TMR^b$, where the exponent $b \geq 1$. At the same time, there exists an optimal value of RA product that minimizes the energy dissipation and the EDP of vTOPSS. As long as $\tau_{\text{eq}}$ is negligible compared to the MI reversal delay, an increase in RA product reduces the energy dissipation, resulting in a concomitant reduction in the EDP of the device. Note that the MI reversal delay is not affected by the RA product. For STT-MRAM applications, a large RA product is undesirable as it increases the voltage required to switch the magnetization state via current-induced spin torques [48]. In the case of vTOPSS technology, the MTJ...
cell is only used to generate a rather low output voltage that must be sufficient to switch the subsequent logic stage. As such, a large RA of the read unit on the MTJ stack may be beneficial to the design of vTOPSS.

As shown in Fig. 4, EDP initially decreases with an increase in RA product. With further increase in RA, EDP exhibits the reverse trend and begins to increase. For RA < RA_{opt} (optimal), the scaling of EDP with RA is expressed as EDP ∝ RA^{-1}. Beyond the optimal value RA_{opt}, unfortunately the delay associated with charging/discharging capacitive nodes becomes much larger than the MI reversal delay. The optimal value of RA depends on the material and geometry of the device. For the results shown in Fig. 7, RA_{opt} decreases with a reduction in $R_{\text{sheet}}$. Moreover, the EDP-RA contour becomes flatter around the optimal point as $R_{\text{sheet}}$ reduces. Results show that at a TMR of 600% and without any leakage through the TI, the optimal EDP of vTOPSS is around $2 \times 10^{-29}$ Js, which is comparable to the EDP of CMOS technology at the 2020 ITRS node (see discussion in Sec. IV D). For the same parameters, the energy dissipation and the delay of vTOPSS are 0.23 aJ and 55 ps, respectively, in typical MTJs. TMR increases with increasing RA product, which can be harnessed to improve the EDP of vTOPSS. In [49], it is shown that a TMR of 600% can be obtained with an RA product of $10^5 \Omega \cdot \mu m^2$ in CoFeB/MgO/CoFeB type MTJs by annealing the structure above 500°C.

### C. Interconnect considerations

To transmit information between vTOPSS logic, conventional CMOS-compatible metallic interconnects can be used. Additionally, highly resistive nanowires with effective resistivity ($\rho_{\text{eff}} \leq 100 \ \mu \Omega \cdot cm$) can also be used as the dominant component of delay is due to the MI reversal under the influence of anti-damping torque. As such, there exists a wide range of interconnect options, such as copper, ultra-scaled wires (wire width $\ll$ electron mean free path), doped semiconducting wires to design vTOPSS logic. The effect of interconnect resistivity on the the interconnect latency of vTOPSS for various interconnect lengths is shown in Fig. 8. Even for interconnect resistivity of 100 $\mu \Omega cm$, the delay associated with charging/discharging the output node is $\approx 30$ ps for interconnect length of 5 $\mu m$ and width of 10 nm (point labeled as “a” in Fig. 8). For wider interconnects, the effect of resistivity increase on the charging/discharging time constant is negligible. For comparison, the reversal delay of the MI layer is few 100’s of picoseconds and will dominate the overall latency of vTOPSS for interconnect length scales up to a few micrometers.

![FIG. 8. Effect of interconnect resistivity ($\rho_{\text{eff}}$), length ($L_{\text{int}}$), and width ($W_{\text{int}}$) on the charging/discharging time constant of the output node voltage. For comparison, the MI reversal delay is on the order of few 100’s of picoseconds. Simulation parameters are the same as those reported in the caption of Fig. 4](image)

### D. Comparison against existing logic devices

The model used for computing the performance metrics of CMOS technology comprise a minimum-sized CMOS inverter driving a similarly sized load through copper/low-$\kappa$ interconnect. Using the Elmore delay model, the delay of the CMOS circuit is given as

$$
\tau_{\text{CMOS}} = 0.69 R_S (C_S + C_L) + 0.69 (R_{\text{Source}} + r_{\text{int}} C_L) L_{\text{int}} + 0.38 r_{\text{int}} C_L L_{\text{int}}^2,
$$

where $R_S$ and $C_S$ are the source resistance and capacitance, respectively, $C_L$ is the load resistance (assumed equal to $C_S$). The energy dissipation of the CMOS circuit

![FIG. 7. EDP of vTOPSS versus the RA product of the MTJ for various values of $R_{\text{sheet}}$ of the TI layer at $\epsilon = 1$, TMR = 600%, $V_{\text{read}} = 50$ mV. An optimal RA product value exists that minimizes the EDP of the device. The inset shows the scaling of EDP with TMR for all other material parameters fixed. Inset shows the scaling of EDP with TMR for RA = $10^{-9} \ \Omega m^2$. Other simulation parameters are same as those reported in Fig. 4](image)
is given as

\[ E_{\text{CMOS}} = (C_S + C_L + c_{\text{int}}L_{\text{int}})V_{\text{DD}}^2, \]

where \( V_{\text{DD}} \) is the supply voltage.

CMOS device metrics are taken from the ITRS roadmap for the 2020 technology node (1/2 pitch of metal-1 = 18 nm). For a minimum-sized inverter, \( R_S \approx 78 \, \text{k}\Omega, \) \( C_S = 0.68 \, \text{fF/\mu m}, \) \( C_L = 0.38 \, \text{fF/\mu m}, \) \( \rho_{\text{eff}} = 25 \, \mu\Omega\text{cm}, \) \( c_{\text{int}} = 1.6 \, \text{pF/cm}, \) interconnect aspect ratio = 2 \([51]\). The delay of the CMOS circuit by omitting interconnect related delay is \( \approx 1.1 \) ps at an energy dissipation of 10 aJ/bit. This yields an EDP of \( 1.1 \times 10^{-29} \) Js. For an interconnect length of 100 nm, the delay of the CMOS circuit is 2.1 ps at an energy dissipation of 20 aJ/bit and EDP of \( 4.2 \times 10^{-29} \) Js.

Existing spin-based devices that are considered for comparison include all-spin logic (ASL) \([52]\), charge-spin logic (CSL) \([53]\), magnetoelectric spin-orbit (MESO) logic \([54]\). ASL uses filtering of electric current through a nanomagnet to generate spin-polarized current, which communicates spin information between input-output nanomagnets via a non-magnetic conductor (e.g., copper, aluminum) that serves as the interconnect. Unlike charge current, spin current is not conserved; therefore, the design of interconnects in ASL requires careful consideration \([55]\). On the other hand, CSL uses spin-Hall effect to convert electric current carrying information into spin polarized current, which is used to switch the state of an input nanomagnet. The orientation of the input nanomagnet is communicated to an output nanomagnet via their mutual magnetic dipolar coupling. The magnetization state of the output nanomagnet is read through an MTJ, which generates an output electric current with the polarity and amplitude dependent on the orientation of the output nanomagnet and the voltage applied on the MTJ. Since information is communicated via electric current, there is no loss of information in the interconnect. However, due to the flow of electrical current through a heavy metal layer with a high effective resistivity, CSL has a high Joule heating. The MESO device, recently proposed in \([54]\), uses magnetoelectric transduction to convert electrical current into spin current at the input side, while spin-orbit coupling is utilized at the output end for spin to charge transduction. That is, the input and output state variables are encoded in electrical current. Benchmarking activities have shown that magnetoelectric mediated spin devices have energy dissipation comparable to that of CMOS \([8]\).

Table 1 shows the performance metrics of vTOPSS in comparison to spin-based devices. The performance of vTOPSS exceeds that of existing spin-based devices. The energy dissipation of vTOPSS is \( 100 \times \) lower than that of ASL and CSL, while the delay of vTOPSS is \( (2-10) \times \) lower than that of ASL and CSL, respectively. The delay of vTOPSS is comparable to that of the MESO device and can be reduced further by utilizing MI layers with lower damping and/or MI switching via precessional dynamics. In terms of energy dissipation, vTOPSS performs slightly better than the MESO device. The energy dissipation can be further reduced through material optimization, particularly with a higher TMR and RA product of the MTJ used for sensing the state of the MI layer in vTOPSS.

V. UNIVERSAL BOOLEAN LOGIC IMPLEMENTATION

A complete set of two-input Boolean functions can be implemented using the schematic shown in Fig. 9. In this figure, \( V_A \) and \( V_B \) refer to primary signal inputs, while \( V_X \) denotes the tie-breaking input signal. To change the functionality between true and complementary outputs, the polarity of the supply voltage signals on the MTJ is swapped. To implement NAND gate, \( V_X \) is set to its negative value, while for NOR gate, \( V_X \) is set to its positive voltage. For XOR/XNOR functionality, one of the primary inputs is applied as a voltage signal on the TI, while the other primary input will serve as the supply voltage on the MTJ in the read unit. In the case of copy/invert functions, the tie-breaking signal \( V_X \) is set to 0 V. Alternatively, the schematic shown in Fig. 1 can be used for copy and invert Boolean operations. However, by using a generic layout as in Fig. 9 all 16 Boolean operations possible for two input signals can be implemented directly by permuting the polarities of MTJ supply and the control voltage. Another major advantage of vTOPSS is its ability to support logic locking \([56]\) and encryption at the device level by preventing optical based reverse engineering attacks \([59]\). The innate polymorphism of vTOPSS will enable runtime reconfigurability where the actual function to be implemented is determined on-the-fly using a key/control input. Exploring the resilience of vTOPSS against existing hardware attacks, prominently those based on the Boolean satisfiability test, will be investigated in future work.

The device layout corresponding to the universal logic gate is shown in Fig. 10, where the device area for a universal gate is \( 0.06 \, \mu m^2 \) assuming relatively large values of the cross-sectional areas of the TI-MI interface, MTJ, and the interconnect. The area can be reduced significantly by patterning narrower TI/MI layers and reducing the cross-sectional dimensions of the MTJ. The latter approach, in particular, is advantageous for reducing the device footprint without a negative impact on the device performance metrics.

VI. CONCLUSIONS

Computational electronics can, in principle, be realized using any state variable that is stable over device-relevant timescales, and with any low-loss communication mechanism between devices that allows fan-out. In this regard, storing and manipulating information in magnetic materials is promising. Magnetic materials have a large number of electron spins that are locked together by their exchange interaction such that the reorientation energy per spin to move the magnetization collectively can be on
TABLE I. Overview of performance metrics of various spin-based devices. Performance metrics of vTOPSS exceed those of existing spin-based technologies. ASL: All-spin logic, CSL: Charge-spin logic, MESO: Magnetoelectric spin orbit logic. The EDP of low-power CMOS technology at the 2020 ITRS technology node is \( \approx 4 \times 10^{-29} \) Js (see text for calculations). *indicates results for perpendicular magnetic anisotropy magnets, **total pulse width reported in [54]. #conservative estimate as it assumes areas of TI layer and the MTJ are equal to \((100 \times 100) \) nm\(^2\) and spacing between TI and MTJ = 50 nm. vTOPSS area is calculated for the device in Fig. 9.

| Metric                  | ASL [54] | CSL [57] | MESO [54] | vTOPSS (this work) |
|-------------------------|----------|----------|-----------|--------------------|
| Input/Output            | Voltage  | Electrical current | Electrical current | Voltage |
| Transduction            | \( V \rightarrow m \rightarrow I_{\text{spin}} \rightarrow m \) | \( I_{\text{elec}} \rightarrow m \rightarrow I_{\text{elec}} \) | \( I_{\text{elec}} \rightarrow m \rightarrow I_{\text{elec}} \) | \( V \rightarrow m \rightarrow V \) |
| Energy-per-bit          | 0.34 fJ(*) | 0.32 fJ | 27 aJ | 21 aJ |
| Switching delay         | 0.5 ns   | 1.5 ns   | 250 ps(***) | 200 ps |
| Energy-delay product    | \( 1.7 \times 10^{-26} \) Js | \( 4.8 \times 10^{-25} \) Js | \( 6.75 \times 10^{-27} \) Js | \( 4.2 \times 10^{-27} \) Js |
| Area                    | \( 3.8 \times 10^{-3} \) \( \mu \text{m}^2 \) | \( 1.6 \times 10^{-3} \) \( \mu \text{m}^2 \) | \( 1.4 \times 10^{-2} \) \( \mu \text{m}^2 \) | \((1-2) \times 10^{-2} \) \( \mu \text{m}^2 \)(#) |
| Fan-out                 | No       | Yes      | Yes       | Yes |

vTOPSS material parameters: \( A_{\text{int}} = A_{\text{MTJ}} = (100 \times 100) \) \( \mu \text{m}^2 \), \( \alpha = 3 \times 10^{-3} \), \( \sigma_{\text{SHC}} = 2000 \) \( h/e \) \( \Omega \) \( ^{-1} \) \( \text{cm} \) \(^{-1} \), \( E_b = 30kT \), \( H_K = 0.1 \) T, \( \kappa = 0.5 \), \( c_{\text{int}} = 1.6 \) \( \text{pF} / \text{cm} \), \( \rho_{\text{eff}} = 25 \) \( \mu \Omega \text{cm} \), \( TMR = 1.4 \), \( RA = 100 \) \( \Omega \mu \text{m}^2 \), interconnect length and width = 100 nm, \( G_{\text{TI}} = 0 \) (no leakage), \( V_{\text{read}} = 50 \) mV.

FIG. 9. All two-input Boolean logic functions can be implemented using the same device layout. The primary inputs are denoted as \( V_A \) and \( V_B \), while the signal \( V_X \) denotes the tie-breaking signal to change the Boolean functionality. To switch between inverting and non-inverting logic (different polarities of \( V_{\text{out}} \)), the polarity of the signals \( V^+ \) and \( V^- \) at the MTJ can be interchanged.

FIG. 10. Device layout for schematic shown in Fig. 9. Here, it is assumed that the cross-sectional area of the TI layer is \((100 \times 100) \) \( \mu \text{m}^2 \) and the spacing between adjacent TI layers is 50 nm. The MTJ cross-sectional area is the same as that of the TI-MI interface. The total area is \( \approx 0.06 \) \( \mu \text{m}^2 \).

the order of meV. Magnetization reversal solely through electric fields is critical toward paving the path for an ultra-low-energy computing substrate. The efficiency of voltage-spin conversion must be significantly higher to allow ultra-low-voltage operation to be competitive with CMOS technology.

In this paper, a voltage-controlled topological spin switch (vTOPSS) based on a hybrid topological insulator (TI)-magnetic insulator (MI) magneto-electric structure was presented. The device has the following important features: (i) innate polymorphism, i.e. it can implement all 16 two-input Boolean operations using the same layout, (ii) CMOS compatible (input/output variables are in voltage domain), (iii) extremely large intrinsic gain for charge-to-spin conversion owing to the ultra-high spin Hall conductivity of the TI material, (iv) ability to support fan-out, (v) sub-10 mV operation with energy-per-bit \(< 10 \) aJ/bit, (vi) ability to lower EDP on the order of \( 10^{-29} \) Js (competitive with CMOS), (vii) elimination of electrical current carrying wires as the operation is fully based on voltage-to-voltage conversion with transmission of information via capacitive charging/discharging of wires, (viii) ultra-low damping of the MI layer allows ultra-fast operation on the order of few 100’s of picoseconds via anti-damping spin torque.

We developed analytic models to quantify the performance of vTOPSS and benchmark the results against existing CMOS and spin-based devices. Our results conclusively show that at the current state-of-the-art material parameters, vTOPSS exceeds the performance of all-spin logic, charge-spin logic, and magnetoelectric spin-orbit logic. Improvements in material parameters and device design can readily facilitate sub-aJ energy-per-bit operation with an energy-delay product \( \sim 10^{-29} \) Js for vTOPSS to be competitive against CMOS devices at the 2020 ITRS technology node. Future work will address important issues pertinent to multi-domain effects in both uniaxial and biaxial magnetic insulators and effects of thermal stochasticity for sub-critical excitation.
Unlike CMOS, vTOPSS can also provide logic locking due to the uniform device-level layout that makes it virtually impossible to probe the functionality with reverse engineering hardware attacks. The ability of vTOPSS to thwart state-of-the-art Boolean SAT attacks is yet to be examined and will be considered in future work.

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[1] C. Chappert, A. Fert, and F. N. Van Dau, Nature Materials 6, 813 (2007).
[2] N. Locatelli, V. Cros, and J. Grollier, Nature Materials 13, 11 (2014).
[3] N. Kani and A. Naemi, in Proceedings of the 2014 IEEE/ACM International Symposium on Nanoscale Architectures (ACM, 2014) pp. 110–115.
[4] Y. Huai, AAPP Bulletin 18, 33 (2008).
[5] L. Liu, C.-F. Pai, Y. Li, H. Tseng, D. Ralph, and R. Buhrman, Science 336, 555 (2012).
[6] J. Katine and E. E. Fullerton, Journal of Magnetism and Magnetic Materials 320, 1217 (2008).
[7] D. E. Nikonov, G. I. Bourianoff, G. Rowlands, and I. N. Krivorotov, Journal of Applied Physics 107, 113910 (2010).
[8] D. E. Nikonov and I. A. Young, IEEE Journal on Exploratory Solid-State Computational Devices and Circuits 1, 3 (2015).
[9] Y.-H. Chu, L. W. Martin, M. B. Holcomb, M. Gajek, S.-J. Han, Q. He, N. Balké, C.-H. Yang, D. Lee, W. Hu, et al., Nature Materials 7, 478 (2008).
[10] C.-G. Duan, J. P. Velev, R. F. Sabirianov, Z. Zhu, J. Chu, S. S. Jaswal, and E. Y. Tsymbal, Phys. Rev. Lett. 101, 137201 (2008).
[11] T. Wu, A. Bur, P. Zhao, K. P. Mohanchandra, K. Wong, K. L. Wang, C. S. Lynch, and G. P. Carman, Applied Physics Letters 98, 012504 (2011).
[12] J.-M. Hu, T. Yang, J. Wang, H. Huang, J. Zhang, L.-Q. Chen, and C.-W. Nan, Nano letters 15, 616 (2015).
[13] R.-C. Peng, J.-M. Hu, K. Momeni, J.-J. Wang, L.-Q. Chen, and C.-W. Nan, Scientific Reports 6 (2016).
[14] N. Kani, J. T. Heron, and A. Naemi, IEEE Transactions on Magnetics (2017).
[15] N. Tiercelin, Y. Dusch, A. Klimov, S. Giordano, V. Preobrazhensky, and P. Pernod, Applied Physics Letters 99, 192507 (2011).
[16] N. Tiercelin, Y. Dusch, V. Preobrazhensky, and P. Pernod, Journal of Applied Physics 109, 07D726 (2011).
[17] A. Mellnik, J. Lee, A. Richardella, J. Grab, P. Mintun, M. H. Fischer, A. Vaezi, A. Manchon, E.-A. Kim, N. Samarth, et al., Nature 511, 449 (2014).
[18] A. A. Burkov and D. G. Hawthorn, Phys. Rev. Lett. 105, 066802 (2010).
[19] M. Z. Hasan and C. L. Kane, Rev. Mod. Phys. 82, 3045 (2010).
[20] A.A. Burkov and D. Hawthorn, Phys. Rev. Lett. 105, 066802 (2010).
[21] W. Witzczak-Krempa, G. Chen, Y. B. Kim, and L. Balents, Annu. Rev. Condens. Matter Phys. 5, 57 (2014).
[22] G.-Y. Guo, S. Murakami, T.-W. Chen, and N. Nagaosa, Phys. Rev. Lett. 100, 096401 (2008).
[23] A. Hoffmann, IEEE Transactions on Magnetics 49, 5172 (2013).
[24] N. H. D. Khang, Y. Ueda, and P. N. Hai, arXiv preprint arXiv:1709.07684 (2017).
[25] Y. Lv, J. Kally, D. Zhang, J. S. Lee, M. Jamaï, N. Samarth, and J.-P. Wang, arXiv preprint arXiv:1701.06505 (2017).
[26] M. Fiebig, Journal of Physics D: Applied Physics 38, R123 (2005).
[27] M. Wu and A. Hoffmann, Recent advances in magneticinsulators-From spintronics to microwave applications, Vol. 64 (Academic Press, 2013).
[28] B. Heinrich, C. Burrowes, E. Montoya, B. Kardasz, E. Girt, Y.-Y. Song, Y. Sun, and M. Wu, Phys. Rev. Lett. 107, 066604 (2011).
[29] C. Sahin and M. E. Flatté, Phys. Rev. Lett. 114, 107201 (2015).
[30] M. E. Flatté, AIP Advances 7, 055923 (2017) https://doi.org/10.1063/1.4975692.
[31] W. Witzczak-Krempa, G. Chen, Y. B. Kim, and L. Balents, Annual Review of Condensed Matter Physics 5, 57 (2014).
[32] A. R. Mellnik, J. S. Lee, A. Richardella, J. L. Grab, P. J. Mintun, M. H. Fischer, A. Vaezi, A. Manchon, E. A. Kim, N. Samarth, and D. C. Ralph, Nature 511, 449 (2014).
[33] Y. Fan, P. Upadhyaya, X. Kou, M. Lang, S. Takei, Z. Wang, J. Tang, L. He, L.-T. Chang, M. Montazeri, G. Yu, W. Jiang, T. Nie, R. N. Schwartz, Y. Tserkovnyak, and K. L. Wang, Nature 13, 699 (2014).
[34] G. Guo, S. Murakami, T.-W. Chen, and N. Nagaosa, Phys. Rev. Lett. 109, 096401 (2008).
[35] I. D. Mayergoyz, G. Bertotti, and C. Serpico, Nonlinear magnetization dynamics in nanosystems (Elsevier, 2009).
[36] A. D. Kent, B. Ozylirmaz, and E. del Barco, Applied Physics Letters 84, 3897 (2004).
[37] D. Pinna, C. A. Ryan, T. Ohki, and A. D. Kent, Phys. Rev. B 93, 184412 (2016).
[38] G. E. Rowlands, C. A. Ryan, L. Ye, L. Rehm, D. Pinna, A. D. Kent, and T. A. Ohki, ArXiv e-prints (2017), arXiv:1711.10575 [cond-mat.mes-hall].
[39] H. Liu, D. Bedau, J. Z. Sun, S. Mangin, E. E. Fullerton, J. A. Katine, and A. D. Kent, Journal of Magnetism and Magnetic Materials 358, 233 (2014).
[40] D. Bedau, H. Liu, J. Z. Sun, J. A. Katine, E. E. Fullerton,
While a lumped interconnect model provides a pessimistic value of interconnect latency, we choose this model for its simplicity and ease of analytic calculations. Moreover, for vTOPSS interconnect latency is significantly smaller than that associated with spin accumulation and reversal of the MI layer. Therefore, the error introduced due to a lumped model is negligible.

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S. Mangin, and A. D. Kent, Applied Physics Letters 97, 262502 (2010).

[41] While a lumped interconnect model provides a pessimistic value of interconnect latency, we choose this model for its simplicity and ease of analytic calculations. Moreover, for vTOPSS interconnect latency is significantly smaller than that associated with spin accumulation and reversal of the MI layer. Therefore, the error introduced due to a lumped model is negligible.

[42] R. Clasen, P. Grosse, A. Krost, F. Levy, S. Marenkin, W. Richter, N. Ringelstein, R. Schmechel, G. Weiser, H. Werheit, et al., Landolt-Bornstein, New Series, Group III 17 (1998).

[43] M. Brahlek, N. Koirala, N. Bansal, and S. Oh, Solid State Communications 215, 54 (2015).

[44] E. de Vries, S. Pezzini, M. Meijer, N. Koirala, M. Salehi, J. Moon, S. Oh, S. Wiedmann, and T. Banerjee, Phys. Rev. B 96, 045433 (2017).

[45] M. Brahlek, N. Koirala, M. Salehi, N. Bansal, and S. Oh, Phys. Rev. Lett. 113, 026801 (2014).

[46] M. Salehi, H. Shapourian, N. Koirala, M. J. Brahlek, J. Moon, and S. Oh, Nano Letters 16, 5528 (2016).

[47] S. Rakheja and A. Naeemi, IEEE Transactions on Electron Devices 57, 2711 (2010).

[48] S. Chatterjee, M. Rasquinha, S. Yalamanchili, and S. Mukhopadhyay, IEEE Transactions on Very Large Scale Integration (VLSI) Systems 19, 809 (2011).

[49] S. Ikeda, J. Hayakawa, Y. M. Lee, R. Sasaki, T. Meguro, F. Matsukura, and H. Ohno, Japanese Journal of Applied Physics 44, L1442 (2005).

[50] H. Bakoglu and J. D. Meindl, IEEE Transactions on Electron Devices 32, 903 (1985).

[51] L. Wilson, Semiconductor Industry Association (2013).

[52] B. Behin-Aein, D. Datta, S. Salahuddin, and S. Datta, Nature Nanotechnology 5, 266 (2010).

[53] S. Datta, S. Salahuddin, and B. Behin-Aein, Applied Physics Letters 101, 252411 (2012).

[54] S. Manipatruni, D. E. Nikonov, R. Ramesh, H. Li, and I. A. Young, arXiv preprint arXiv:1512.05428 (2015).

[55] S. Manipatruni, D. E. Nikonov, and I. A. Young, IEEE Transactions on Electron Devices 60, 3913 (2013).

[56] S. Manipatruni, D. E. Nikonov, and I. A. Young, Phys. Rev. App. 5, 014002 (2016).

[57] N. Rangarajan, A. Parthasarathy, N. Kani, and S. Rakheja, IEEE Transactions on Magnetics (2017).

[58] Y. Xie and A. Srivastava, in International Conference on Cryptographic Hardware and Embedded Systems (Springer, 2016) pp. 127–146.

[59] H. Wang, D. Forte, M. M. Tehranipoor, and Q. Shi, IEEE Design & Test 34, 63 (2017).