Metaplasticity in Multistate Memristor Synaptic Networks

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Abstract—Recent studies have shown that metaplastic synapses can retain information longer than simple binary synapses and are beneficial for continual learning. In this paper, we explore the multistate metaplastic synaptic characteristics in the context of high retention and reception of information. Inherent behavior of a memristor emulating the multistate synapse is employed to capture the metaplastic behavior. An integrated neural network study for learning and memory retention is performed by integrating the synapse in a $5 \times 3$ crossbar at the circuit level and $128 \times 128$ network at the architectural level. An on-device training circuitry ensures the dynamic learning in the network. In the $128 \times 128$ network, it is observed that the number of input patterns the multistate synapse can classify is $\approx 2.1x$ that of a simple binary synapse model, at a mean accuracy of $\geq 75\%$.

Keywords—Metaplasticity, Memristor, Multistate synapse

I. INTRODUCTION

Neural plasticity in the brain is the ability to learn and adapt to intrinsic or extrinsic stimuli by reorganizing the morphology, functions, or connectivity of its constituent synapses and neurons. Synaptic plasticity is a complex dynamic process that modulates and regulates network dynamics depending on external activity over multiple timescales. Metaplasticity refers to plasticity of the plasticity of synapses [1]. A metaplastic synaptic network enables a synapse to tune its level of plasticity depending on the pre-synaptic activity. This property is deemed crucial for high memory retention and learning capability in a synaptic network [2]. It is shown that simple binary synapses show high memory retention when the imposed activity is highly sparse. However, for moderately sparse neuronal activity, the interference between multiple stimuli can pose a challenge to achieve high memory retention and learning. Since binary synapses cannot concurrently learn new activity and retain knowledge of past activity, the synapse memory lifetime drops significantly [3]. To solve this issue, Fusi et al. [2] proposed a cascade model of synapse, in which synapses with binary efficacy have multiple metastates. Synapses exhibit varying degree of plasticity depending on their metaplastic state. This property enables a network of such synapses to retain knowledge of past activity and facilitate high plasticity to learn new activity. While the cascade synapse outperforms a simple binary synapse in response to moderately sparse activity, its memory retention for highly sparse activity is orders below that of a simple binary synapse. In [3], Leibold et al. proposed a variant of metaplastic synapse model, in which the metastates are serially connected and the probability to transit from one state to another is equally likely. This serial synaptic metaplasticity model, also referred to as multistate synapse, shows less degradation in memory lifetime for highly sparse activity and outperforms the cascade model in memory capacity [3]. In this paper, we focus on the multistate synaptic model. Previous research on metaplasticity focused on physical metaplastic behavior in memristor devices [4]–[6]. Most of the prior literature is concentrated on device level analysis considering only continuous synaptic efficacy with no network level realization. However, incorporating metaplastic synapses in a crossbar architecture can lead to compact and powerful neuromorphic architecture capable of high memory retention. Since edge devices encounter large amounts of streaming data, such architecture can immensely benefit their overall performance.

One of the early realizations of the binary metaplastic synapse was proposed by [3]. Since this model can retain previously learned information and maintain response to new information simultaneously, such a synaptic model can better capture all the information learned throughout its lifetime. Hence, it shows better resilience against catastrophic forgetting compared to binary synapses. In this research, we study this synaptic model at-scale in memristive neural accelerators. The main contributions of this paper are as follows:

- to emulate binary metaplastic synapses by exploiting inherent device properties of a memristor.
- to demonstrate the efficacy of metaplastic synapse in a $5 \times 3$ crossbar circuit architecture with on-device learning capability.
- to compare the performance of binary vs. metaplastic synapse in a two layer neural network emulating hardware constraints.

II. METAPLASTIC SYNAPTIC NETWORK MODEL

The multistate synapse is a relatively simple model where metaplasticity is modeled by serially connected metastates. The probability to transit from one state to the other is equal. Fig. 1 shows the metastates of the multistate synapse and their inter-transitions. The red and blue bubbles represent synaptic metastates with efficacy 1 and 0 respectively. The arrows show the transition direction, the red arrows correspond to potentiation and the blue arrows represent depression. As shown in Fig. 1, the synapse changes its efficacy only when it is in metalevel ($\eta$) 0; in all other cases it only changes the metalevel retaining its efficacy. Multistate model with n metalevels can exhibit $(2n-1)$ forgetting timescales which helps it to retain knowledge of past activity [3].
In [7] and [3], the authors investigate memory lifetime by imposing a specific pattern of activity to the network and observing how long the network can recollect the learned information. It is shown that complex synapses with metaplasticity can retain information longer than simple binary synapses when the neuron activity becomes less sparse. In this work, we explore how metaplasticity affects the accuracy of a synaptic network to detect all the patterns learned throughout its lifetime and its capability to learn new activity. We consider a simple feed forward network where $N_{in}$ input neurons are connected to $N_{out}$ output neurons through a network of sparse synapses. Random input patterns and corresponding output patterns of activity $f$ ($\%$ of bits are high) are generated and applied to a network with connectivity $C$, i.e. $C\%$ of the input and output neurons are connected to each other. Initially, the connected synapses have random efficacy and they are at their most plastic state. Similar to [3], we use McCulloch-Pitts neuron model at the output nodes. This neuron detects activity if the incoming signal is greater than its threshold, which is set based on the average input to an output neuron in the network. The incoming signal is greater than its threshold, which is set based on the average input to an output neuron in the network when the neuron activity becomes less sparse. In this work, we further investigate the effect of network connectivity $C$ and its capability to learn new activity. We consider a simple feed forward network where $f/\%$ of bits are high and $C/\%$ of the input and output neurons are connected to each other. Initially, the connected synapses have random efficacy and they are at their most plastic state. Similar to [3], we use McCulloch-Pitts neuron model at the output nodes. This neuron detects activity if the incoming signal is greater than its threshold, which is set based on the average input to an output neuron in the network when the neuron activity becomes less sparse. In this work, we further investigate the effect of network connectivity $C$ and its capability to learn new activity.

In Fig. 2(a) we see that the binary network outperforms both GD and multistate network in learning accuracy. The multistate network shows $\approx 91\%$ accuracy after encountering 100 patterns whereas for the binary network it is $\approx 99\%$. However, in Fig. 2(d) we see that the mean accuracy drops significantly slower in the multistate network than both GD and binary network. To compare the performance across networks we empirically set a threshold at 75% for the mean accuracy and observe the number of imposed patterns after which the mean accuracy goes below it. From Fig. 2(d) we see that the mean accuracy goes below the threshold after 20 patterns for the binary network whereas in multistate network it is 45 patterns. The loss in learning accuracy is significantly lower than the gain in mean accuracy. We also observe in Fig. 2(b) and (e) that with increasing network size the multistate network shows less degradation in learning accuracy and even higher mean accuracy as its memory capacity grows with size. We further investigate the effect of network connectivity $C$ and input activity $f$ on the mean accuracy of a multistate network (Fig. 2(c)). We notice a drop in the performance around $f=50\%$ due to rise in conflicting patterns, but it retains high performance for high and low connectivity. Overall, the simulation results indicate that the multistate synaptic model shows better accuracy in detecting patterns learned over lifetime accompanied by a degradation in learning ability compared to binary and it is particularly suitable for modeling large network of synapses.

In this work, we leverage device characteristics of memristor device to realize a multistate synapse. As presented in [8], the device under consideration shows gradual change in conductance during RESET. For modeling we assume this behavior during SET operation as well. To emulate the metastates, the memristor was trained with $15\mu$s pulses of 1.2V to potentiate or depress from one state to another. In this process, we get three states with high and low conductance which can represent different metastates. The correlation between the metastates and the memristor state variable ($w$) which is proportional to its conductance is shown in Fig. 1. In the ideal multistate model, change in metalevel incurs no change in synaptic efficacy. However, in the hardware emulation the conductance of the memristor varies across metastates. The device has to be programmed to ensure that the difference in conductance between the high and low efficacy states is substantial. In the modeled memristor, the lowest and highest resistive states were set to be 100k$\Omega$ and 10M$\Omega$ respectively and the ratio of conductance between high and low efficacy state at metalevel zero is $\approx 4.5$.

A modified Verilog-A memristor model proposed by [9] is employed to model the memristor. The device conductance changes as a function of the state variable, $w$, which is described in (1) and (2) where $D$ is the device thickness, and $G_{on}$ and $G_{off}$ define the memristor conductance limits. Here, the memristor model is tightened with a modified Z-window function (10) (see [3]).

$$G_{mem} = \frac{w}{D} \times G_{on} + (1 - \frac{w}{D}) \times G_{off}$$

(1)

$$\Delta w = \begin{cases} k_{off} \cdot \left( \frac{v(t)}{v_{off}} - 1 \right)^{\alpha_{off}} \cdot f_w(w), & 0 < v_{off} < v \\ 0, & v_{on} < v < v_{off} \\ k_{on} \cdot \left( \frac{v(t)}{v_{on}} - 1 \right)^{\alpha_{on}} \cdot f_w(w), & v < v_{on} < 0 \end{cases}$$

(2)

$$^1k_{off}, k_{on}, \alpha_{on}, \text{ and } \alpha_{off} \text{ are constants, and } v_{off} \text{ and } v_{on} \text{ are the memristor threshold voltage.}$$

$$^2\tau, \delta, \text{ and } p \text{ are constants to control the window function shape.}$$
Fig. 2. In (a) & (d): Learning and mean accuracy of $128 \times 128$ network developed using binary and multistate synapses. Here, H/W-Binary and H/W-Multistate refer to the network designed with hybrid CMOS/memristor circuitry in Cadence, while considering device non-idealities. Gradient shows the accuracy for network trained with gradient descent. In (b) & (e): Learning and mean accuracy of multistate networks as a function of the network size. In (c) & (f): Effect of network connectivity $C$ and input activity $f$ on the mean accuracy after presenting 100 patterns to a $128 \times 128$ network of multistate synapses and its hardware emulation respectively.

\[
f_w = \frac{1 - 4(\frac{w}{\eta} - \delta)^2}{e^{\tau(\frac{w}{\eta} - \delta)^p}}
\]

To account for device variability, a random Gaussian noise with standard deviation of 25% is induced for 100 cycles. The amount of noise considered is relatively higher than observed in actual devices to compensate for the suppression of variability due to the $Z$ window function.

IV. Metaplastic System Level Design

The multistate synaptic behavior is studied using the system architecture of a two layer neural network shown in Fig. 3. The sparse synaptic network is emulated by a crossbar consisting of the memristor model described in Fig. 1. The crossbar is initialized randomly maintaining connectivity $C$, setting the synapses with high and low efficacy to the most plastic metalevel ($\eta = 0$). We model the sparse connectivity by randomly setting crosspoints between the two neuronal layers to the lowest conductivity which are left untrained. A current comparator is chosen to model the McCulloch-Pitts neuron and we exploit its varying input resistance to improve the network performance. The input resistance of the neurons changes in the same direction as the column resistance which improves the networks ability to detect presynaptic activity and increases the mean accuracy. Inference is carried out simultaneously for all the columns. Since the synaptic columns are not grounded, if the inputs are directly connected to the output neuron, voltage drop across the current comparator will push current back into the input nodes with inactive presynaptic input. To prevent this, the inputs are connected to the crossbar through diodes. The programming scheme described in section III is executed using Ziksa to carry out the synaptic transitions. In this work, Ziksa is slightly modified by adding an extra transistor to the row trainer. This extra transistor holds the rows with inactive presynaptic input at $V_{DD}/2$ to reduce sneak current in the crossbar during training. The network is trained in two steps for the synapses to be potentiated and depressed, respectively. The training circuitry, current comparator and the error computing unit are shown in detail in Fig. 4.

V. Results and Analysis

The proposed architecture is evaluated through high level simulation of $128 \times 128$ networks ($f=25\%$, $C=25\%$) of binary and multistate memristive synapses with random Gaussian noise ($\sigma=0.25$). The simulation is carried out in MATLAB with implication of hardware constraints. Fig. 2(a) and (d) show the learning and mean accuracy for the hardware emulation of binary and multistate synapses while 100 random input patterns similar to Fig. 7 with activity $f$ are imposed on the network. We see that the mean accuracy for binary network drops below 75% after presenting 22 input patterns whereas for the multistate network this accuracy drop is observed after learning 47 patterns. Similar to the analysis in section II, the high mean accuracy comes at a cost of drop in the learning capability. The drop in the learning accuracy is higher in hardware emulation than its software counterpart due to the undesirable current through the low efficacy and pruned synapses. We further
explore the performance of the multistate network for different network connectivity (C) and input activity (f). As shown in Fig. 2(f), at C = 50%, the network mean accuracy drops with dense activity. When C = 40-60%, the percentage of connected and pruned synapses are comparable. Dense activity in this setting (f = 75-90%) results in significant current through the pruned synapses and the network shows poor performance which is observed in figure Fig. 2(f). We deduce that the hardware multistate network can differentiate patterns well when there is a considerable difference between the number of connected and pruned synapses, otherwise conflicting patterns and undesired current harshly affect the performance. In order to demonstrate the functionality of the proposed scheme, a multistate synaptic network with 5 input neurons and 3 output neurons is simulated in Cadence Virtuoso. Fig. 3 (left panel) shows a case scenario where four synapses in a crossbar column, denoted by w1-w4, have active presynaptic inputs and the error is positive. According to the learning rule, a potentiating pulse is applied to these synapses. w2, w3 and w4 have low initial efficacy, but they are in metalevel 0, 1 and 2, respectively. In Fig. 3 we see that only w2 changes its efficacy level due to potentiation, whereas w3 and w4 only transit to a lower metastate, w1, which has high initial efficacy at metalevel 0 transit to metalevel 1. The right panel of Fig. 3 shows the transitions of these potentiated weights when error is negative. Since w3 is in metalevel 0, it changes its efficacy level to low after the depression cycle while all the other weights retain their efficacy level with appropriate change in metastate. The power consumption of the proposed network is highly impacted by the input activity (f) and network connectivity (C). Considering connectivity C=50% in the implemented 5×3 crossbar network, we found the average power consumption to be 24.64μW (excluding the control circuitry) for 100 input and output patterns with activity f=75%. Low input activity (f) and low connectivity (C) is highly favorable for the proposed network. In such setting, the power consumption of the network is reduced since majority of the synaptic connections are pruned. It also enables the network to better utilize the metaplasticity of multistate synapses and show higher retention and learning capability.

VI. Conclusions

Metaplastic synapses can equip neural networks to better address catastrophic forgetting. This work investigates the performance of multistate synapses for retention and reception of information. It is demonstrated that the model shows slower decay in the mean accuracy than binary model, with moderate deterioration in learning accuracy. We then capture the characteristics of a multistate synapse in a memristive device through appropriate training method to map it to the metaplastic states. The inference and training procedure is validated by simulating a small scale crossbar network (5 ×3 size) in Cadence. Furthermore, high level emulation of the network shows that the number of patterns that the multistate memristive synaptic network can detect with ≤ 25% mean error is ≃ 2.1 times that of its binary counterpart.
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