I. INTRODUCTION

Within the last decade, single electron tunneling (SET) devices have been intensively investigated and have demonstrated their great potential for unique applications [1, 2]. For instance, SET transistors may be used as ultrasensitive electrometers of a minimal charge resolution of less than $10^{-5} e/\sqrt{Hz}$ at 10 Hz [3]. These rather simple SET devices consist of two ultrasmall tunnel junctions, characterized by parameters such as their tunnel resistance $R$ and their junction capacitance $C$, connected in series by a metallic island being capacitively coupled to a gate electrode with capacitance $C_G$.

In this paper, we present a study showing that a suitable forming gas annealing (FGA) process can be used to tune the junction properties of conventional Al-AlO$_x$-Al SET transistors in a controllable way. Recently, several groups have extensively studied the effects of thermal annealing on nm-scaled Nb-Al/AlO$_x$-Nb Josephson junctions with regard to the junction properties [4, 5, 6, 7]. However, adequate attention has so far not been paid to similar studies on tunnel devices comprising nm-scaled Al-AlO$_x$-Al junctions.

We had two motives in processing metallic SET transistor samples by FGA: Firstly, we aimed at investigating the influence of a thermal annealing procedure on the tunnel junctions with respect to $R$ and $C$. Here, the forming gas simply served as a protective atmosphere to prevent the unwanted excessive oxidation of the tunnel junctions. Secondly, forming gas annealing performed at the end of CMOS process lines in the semiconductor industry, is a traditional method for of healing process-induced defects by the passivation of electrically active traps in the Si/SiO$_2$ substrate material [8, 9, 10, 11].

Also, it is well known that the typical $1/f$-like excess charge noise, measured in the low-frequency regime of conventional SET transistors, is caused by the motion of background charges in the dielectric surroundings of the transistor islands (see, for example, [12, 13] and references therein). Hence, it was our special interest to study the effect of the FGA treatment on the noise behavior of our samples that were also prepared on Si/SiO$_2$ substrates.

II. EXPERIMENT

We prepared standard SET transistors by the conventional shadow evaporation technique on an Si substrate wafer with a thermally oxidized SiO$_2$ surface layer (300 nm thick). The three-layer mask was made of PMMA/Ge/copolymer. After patterning of the PMMA layer using e-beam exposure and a developing process, the pattern was transferred to the Ge layer by an etching process in a CF$_4$ plasma, followed by oxygen plasma etching of the copolymer layer creating the undercut for the following shadow evaporation. Next, two layers of aluminum were deposited by e-gun evaporation under different angles, and in situ oxidation of the bottom Al layer (200 Pa O$_2$, 10 min) between the evaporation steps formed the Al-AlO$_x$-Al tunnel junctions. Each of the sample chips carried eight transistors whose junction sizes were intentionally varied on each chip while the island dimensions were kept constant (Fig. 1).

The sample chips were annealed in an electrical furnace at a temperature of 200 °C or 400 °C in a forming gas atmosphere of 10% H$_2$ and 90% N$_2$ (by volume) at a total pressure $\approx$ 800 hPa. Before and between successive annealing cycles, the furnace chamber was flushed with forming gas and evacuated several times to minimize the amount of residual oxygen in the system that entered the system when it was opened to the air. Annealing time dependent resistance changes of the samples...
were traced by multimeter measurements under normal conditions, performed between successive annealing cycles. The low temperature characterization of the samples was performed in a top-loading dilution refrigerator at \( T = 25 \, \text{mK} \) and \( B = 1 \, \text{T} \) before and directly after FGA treatment \([13]\). All signal lines were equipped with Thermocoax cables about 1 m in length, serving as microwave frequency filters \([14]\), and a low-noise electronic setup, consisting of a symmetrical current or voltage bias and low-noise preamplifiers, was used for the measurements. Noise spectra were recorded using an HP 89410A spectrum analyzer. The total resistance value \( R_\Sigma \approx 2 R \) of a sample was given by the asymptotic differential resistance. The external impedance of the aluminum lines connected to the island was rather low, so the total capacitance \( C_\Sigma \) was derived by extrapolating the linear part of the “offset plot”, i.e. \( U_{\text{off}} \equiv U - IdU/dI \) versus \( U \), to zero voltage \([15, 16]\).

**III. RESULTS AND DISCUSSION**

All samples investigated survived the annealing treatment, as it was checked by multimeter measurements directly after FGA. In particular, even after annealing at \( 400 \, ^\circ\text{C} \) for 45 min, the SET transistors retained their typical gate modulation properties without any indication of qualitative degradation. Some samples were also inspected using an electron microscope before and after the FGA (Fig. 1), but no visible changes in their shape or surface morphology due to the annealing process were detected. However, distinct quantitative changes in the main electrical parameters of all samples occurred that are described in the following.

**A. Junction parameters after FGA at 200 °C**

A series of 27 transistor samples with junctions of different size \( (R_{\Sigma,0} \approx 100 \, \Omega - 800 \, \Omega, \; C_{\Sigma,0} \approx 1.1 \, \text{fF} - 0.25 \, \text{fF}) \) was exposed to FGA at a temperature of \( 200 \, ^\circ\text{C} \) for 15 min to 120 min. 16 transistor samples were characterized at \( 25 \, \text{mK} \) before and after the FGA. Unexpectedly, we observed a decrease of the sample resistance \( R_\Sigma \) during annealing. The typical behavior is demonstrated in Fig. 2, showing the relative resistance change \( \Delta R_\Sigma / R_{\Sigma,0} \equiv (R_\Sigma - R_{\Sigma,0}) / R_{\Sigma,0} \) versus the saturation of the resistance change after about 30 min. For all samples, we found a quite similar change of the saturated \( \Delta R_\Sigma / R_{\Sigma,0} \) of about \( 30 \% - 40 \% \). This behavior was reproduced for different sample chips and annealing runs.

We verified that the junctions retained pure tunnel contact behavior after the annealing treatments by making sure that all samples showed a distinct Coulomb blockade regime with a zero current state. Thus, we conclude that the resistance decrease is associated with a reduction of the effective barrier thickness. On the basis of a simple plate capacitor junction geometry where any change in the junction resistance is due to changes

![FIG. 1: SEM picture of a typical SET transistor after FGA at 400 °C for 45 min. No changes are seen in comparison with the picture before annealing. The areas of the tunnel junctions are about \( 80 \times 80 \, \text{nm}^2 \), the total initial island capacitance \( C_{\Sigma,0} \approx 500 \, \text{aF} \), and the total initial resistance \( R_{\Sigma,0} \approx 380 \, \text{kΩ} \).](image)

![FIG. 2: (a) Effect of decreasing sample resistances after FGA at 200 °C for different annealing times with the typical behavior of resistance saturation after 30 min of annealing. (b) Relative change \( \Delta R_\Sigma / R_{\Sigma,0} \) for several samples versus their initial resistance values \( R_{\Sigma,0} \). Resistance values are given in units of kΩ, and the shapes of the symbols correspond to individual transistor samples.](image)
in the tunnel barrier composition, and/or thickness, we calculated the tunnel resistance, assuming a rectangular energy barrier of height $\phi$ and thickness $s$ [4]. With $\phi = 1.9 \text{ eV} - 2.6 \text{ eV}$ for the thermally oxidized aluminum oxide barrier [8] [9] and with an initial thickness $s_0 = 0.7 \text{ nm} - 0.8 \text{ nm}$ (to fit the $R_{\Sigma,0}$ values), we estimated a barrier thickness change $\Delta s/s_0 = -4 \%$, corresponding to the saturated resistance change. In the plate capacitor model, this relative thickness change should be reflected by a similar relative capacitance increase of the junctions. Although the corresponding offset plots seemingly indicate no change in $C_\Sigma$ and, respectively, in $C$ (Fig. 3), we cannot rule out such a small change within the uncertainty due to data scattering.

In principle, finding a junction thickness decrease due to thermal annealing seems contrary to intuition and is in conflict with earlier results for thermal annealing effects on Nb-Al/AlO$_x$-Nb Josephson junctions [4] [5] [6] [7]. Here, it was found without exception that annealing treatments in the range from $T = 0 \text{ °C}$ to $350 \text{ °C}$ resulted in an increase in the normal state junction resistance, indicating an increase in thickness of the AlO$_x$ barriers. As in our case, the AlO$_x$ barriers were thermally oxidized but the materials and the deposition methods for the junction fabrication were different (sputtering in the case of the niobium junctions, but e-gun evaporation of the aluminum devices), which might lead to the differences in the annealing behaviors.

Although we have at present no direct method to investigate the microscopic changes in the barrier, we may speculate about the scenario during annealing: Firstly, in the presence of water, aluminum is known to form many hydroxides from Al$_2$O$_3$·H$_2$O (diaspore, AlO(OH)) to Al$_2$O$_3$·3H$_2$O (gibbsite, AlO(OH)$_3$) and substances of intermediate composition [20]. Although the initial pressure in our evaporation chamber was $\approx 10^{-5} \text{ Pa}$, a small residual water vapor content, and, thus, a deviation of the barrier composition from pure Al$_2$O$_3$ cannot be ruled out. The different hydroxide phases vary in crystalline structure, and dehydration temperatures of 145 °C and more are reported [20]. Even at moderate temperatures of 200 °C, the barrier morphology may therefore be affected by re-crystallization processes or changes in composition, possibly decreasing the effective barrier thickness. Although our data do not provide a clear indication about an associated increase in junction capacitance, even the case of $C \approx C_0$ and $R < R_0$ is possible if the mean barrier thickness is unchanged ($s \approx s_0$), but small sharp spikes form on the electrode surface (for instance due to re-crystallization processes). Such spikes, “pricking” into the barrier, could focus the current distribution on small areas with reduced barrier thickness and, due to the exponential dependence of the tunnel resistance on this parameter, reduce the total resistance.

Of course, in addition to the modifications of the barrier morphology, dehydration processes or changes in composition would affect the barrier height $\phi$ in an unpredictable way. Also, the relaxation of stress inside the layers might influence the interface morphology. We thus may state that our phenomenological observations are distinct and reproducible, but a detailed microscopic explanation is speculative at present.

### B. Junction parameters after FGA at 400 °C

14 transistors with the initial sample parameters $R_{\Sigma,0} \approx 80 \text{ k}\Omega - 410 \text{ k}\Omega$ and $C_{\Sigma,0} \approx 1.4 \text{ fF} - 0.4 \text{ fF}$ were exposed to FGA at a temperature of 400 °C. For all samples we found that the resistance values had approximatively doubled after 15 min, while after 45 min they were about three times $R_{\Sigma,0}$ (Fig. 4(a)). Again, this effect was independent of the initial resistance $R_{\Sigma,0}$ (Fig. 4(b)).

Also, the offset plots of these samples showed a significant increase in $U_{\text{off}}$ after the annealing (Fig. 5), reflecting a decrease of $C_\Sigma$. Assuming that $C_\Sigma = 2C_0 + C_S$, where $C_S \approx 20 \text{ aF} - 40 \text{ aF}$ is the stray capacitance of the 1 µm long transistor islands [14, 21], we estimated the mean capacitance $C$ of the junctions for each transistor [22]. Fig. 6 shows the relative decrease of the tunnel capacitance $\Delta C/C_0 = (C - C_0)/C_0$ versus $C_0$. After 15 min of annealing, the junction capacitances had decreased about 15 % - 20 %, and after 45 min about 20 % - 30 % from their initial values.

These results clearly indicate that the effective oxide barrier thickness increases as a result of the FGA treatment. In accordance with papers [4] [5] [6] [7], we attribute the annealing induced oxide barrier growth by the reaction with unbound oxygen, coming either from interstitial lattice sites in the proximity of the junctions and diffusion - thermally activated - towards the barrier, or directly from dissociation of aluminum hydroxides in the barrier. As described in the previous section, we estimated the relative increase in thickness corresponding to the change in resistance after 45 min, and found $\Delta s/s_0 \approx 9 \%$. Since
FIG. 4: Dependence of the relative sample resistance increase \( \Delta R / R_{\Sigma,0} \) on the annealing time (a) for FGA at 400 °C and versus the initial resistance \( R_{\Sigma,0} \) (b). Resistance values are given in units of kΩ, and the shapes of the symbols correspond to individual transistor samples.

FIG. 5: Offset plot for two different transistors before and after 15 min of FGA at 400 °C (\( T = 25 \) mK, \( B = 1 \) T). Clearly, the voltage offset \( U_{\text{off}} \) has increased after annealing.

FIG. 6: Reduction of the mean tunnel capacitance \( C \) for different transistors after 15 min and 45 min of FGA at 400 °C, represented as the relative change \( \Delta C / C_0 \), versus the initial values \( C_0 \).

this is significantly less than the value derived from the capacitance analysis, we conclude that the simple plate capacitor model for the tunnel junctions breaks down and that a non-uniform change of the barrier thickness has taken place along the junction cross section. In principle, such non-uniform changes may easily explain our findings due to the different functional dependence of tunnel resistance \( R \) and junction capacitance \( C \) on the distance between the tunneling electrodes. Nevertheless, our study does not enable us to make more precise statements about the microscopic changes in the barriers.

C. Low-frequency noise behavior

Si wafers with a thermally oxidized SiO\(_2\) surface layer are the most commonly used substrate material, not only for the preparation of SET devices but also in semiconductor industry. There, the CMOS devices are typically processed by FGA at 400 °C for about 30 min, since this treatment is especially suitable to heal defects in the Si/SiO\(_2\) interface (see, for instance, [8, 9, 10, 11] and reference therein). It is known that so-called interface charge traps are located at the Si/SiO\(_2\) interface, able to exchange carriers with the Si. FGA leads to a hydrogen passivation of these defects so that the interface density of states is typically reduced by one order of magnitude [8, 23] and the device performance is improved generally. Recently, it has been shown that an FGA process similar to that we carried out reduced the power of the low frequency \( 1/f \) noise in bipolar junction transistors by a factor of five, which indicates that the interface traps were effectively passivated by hydrogen [11].

Using our SET transistors prepared on such Si/SiO\(_2\) substrate as ultrasensitive electrometers, we tried to figure out the effects of FGA on the noise figures in the low frequency regime, i.e. in the range \( f = 1 \) Hz to 100
Hz. Before and after annealing at 200 °C and 400 °C, we found the typical 1/f-like noise power spectra, indicating the activities of independently switching noise sources in the dielectric surroundings of the transistor islands. By checking that the noise signal was proportional to the gain in the working point of each transistor, we could make sure that the noise sources were acting on the input of the electrometer, which justified the conversion of the measured noise signals into effective charge noise $Q_N(f)$ (see Fig. 7(a)). The annealing time dependence of the charge noise figures $Q_N$ at $f = 10$ Hz for a several transistors (after FGA at 200 °C and 400 °C) is demonstrated in Fig. 7(b). We generally found that the noise figures varied after thermal cycling between the different characterization runs, but the changes showed no monotonic trend. This is the usual behavior of SET devices when thermal cycling alters the potential “landscape” in which the charge traps are frozen in. Moreover, all values of $Q_N(10$ Hz) were found to be in the range between some $10^{-4}e/\sqrt{Hz}$ and some $10^{-3}e/\sqrt{Hz}$, which is the typical noise level for conventional SET transistors (see, e.g., [3, 4], and references therein).

Our experiments indicate that FGA processing has no significant effect on the level of the 1/f-like charge noise in SET transistors, which is in contrast to the recent experiments on the CMOS bipolar junction transistors [1]. The reason probably is that hydrogen passivation mainly affects noise sources in the Si/SiO$_2$ interface, which is 300 nm below the noise-sensing devices in our case, whereas the charge traps dominating the total noise in our SET devices are located closer to the transistor island, for instance on the substrate surface.

![Graph](attachment:image.png)

**FIG. 7:** (a) Typical 1/f-like charge noise spectra of a transistor before and after different durations of FGA at 400 °C ($T = 25$ mK, $B = 1$ T, $I = 50$ pA). (b) Annealing time dependence of the charge noise figures $Q_N$ at $f = 10$ Hz for several samples after FGA at 200 °C (open symbols) and 400 °C (solid symbols).

### IV. CONCLUSION

We investigated the effect of thermal annealing in a forming gas atmosphere on the properties of Al-AlO$_x$-Al SET transistors and found distinct and reproducible changes of the junction parameters. After annealing at $T = 200$ °C, the sample resistance $R_S$ decreased by about 30 % - 40 %, while the total capacitance $C_S$ remained nearly unchanged. After annealing at $T = 400$ °C, we found an increase in $R_S$, associated with a reduction of $C_S$. In both cases, the effects are attributed to changes in morphology, composition and/or effective thickness in the oxide barriers of the junctions, which are believed to be independent of the composition of the protective atmosphere. Moreover, the changes obtained appeared to be stable, i.e. within several weeks no degradation back to the initial sample values $R_{S,0}$ and $C_{S,0}$ was observed.

In addition, the influence of forming gas annealing on the noise properties of the transistors at low frequency was investigated. Here, we found no significant reduction of the noise level in the 1/f-regime due to potential hydrogen passivation of charge traps.

The good reproducibility of the observed effects suggests that a proper thermal annealing treatment may be used for safe post-process tuning of the junction parameters in SET devices. Firstly, annealing in a protective atmosphere at $T \approx 400$ °C may be used to increase the tunnel resistance $R$ in an easily controllable way, for instance to enhance SET effects in devices with insufficient $R_0 < R_K = \hbar/e^2 \approx 25.8$ kΩ. Secondly, annealing at $T \approx 200$ °C, causing a tunnel resistance drop of about 30 % - 40 %, might be useful to enhance the Josephson coupling energy $E_J \propto R^{-1}$ in the junctions of SET devices that should also offer superconducting properties (as, for instance, the Bloch transistor [4] but are on the borderline of their performance due to the initial sample parameters.
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