Creating a parameterized model of a CMOS transistor with a gate of enclosed layout

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Abstract. The method of creating a parameterized spice model of an N-channel transistor with a gate of enclosed layout is considered. Formulas and examples of engineering calculations for use of models in the computer-aided Design environment of Cadence Vitruoso are presented. Calculations are made for the CMOS technology with 180 nm design rules of the UMC.

1. Introduction
CMOS integrated circuits nowadays are widely used in many areas with high requirements for radiation resistance, such as high energy physics, nuclear physics and astrophysics. In these experiments, the ionizing radiation may cause various defects in the crystal lattice of the oxide layer of the integrated circuit, which may lead to leakage currents both between the drain and the source of a single transistor, and between the standing side by side transistors. At the same time, the work of a single block, or even the whole integrated circuit can be completely broken. As it is known, N-channel transistors are the most susceptible to this effect[2]. There are different methods to manage the leakage current, but the most common solution is the use of guard rings in combination with an enclosed layout topology of N-channel transistors. Guard rings are used to avoid current leakage between the placed near transistors, and an annular valve, are used to avoid between drain and source. However, it is difficult to fully use these types of transistors in a commercial CMOS technology. Primarily it is caused by poor development or even the lack of parametrized models needed for a full simulation of integrated circuits and the optimization on a range of parameters. This article is dedicated to one of the possible ways to create parametrized models or channel PCELL N-MOSFET ring to complete its technology library of CMOS technology with design rules 180 nm UMC company (Taiwan). The approval of the model is assumed to be done in CAD Virtuoso v.6.1.5 OA of Cadence company, which is used widely by authors in the last years.

2. N-channel enclosed layout transistor(ELT)
2.1. Gate enclosed topology
This model of the transistor [1,3] is able to operate, without an interruption at a total dose of 30 MRad thanks to the enclosed layout structure on the technological library of 240 nm. In Figure 1 there is shown such a ring structure taken however from an other technological library. Where: 1 - P-type guard ring, 2 - ring gate, 3 - drain 4 - source, 5 - symbol layer, 6 - a horizontally...
stretched transistor line, 7 - a vertical stretched transistor line, 8 - an enclosed gate stretching line.

Figure 1. Topological representation of N-channel ELT with minimal geometric dimensions for the 180nm technology of UMC company.

2.2. Model of ELT
In most cases, while describing the transistor with the enclosed topology, one resort to stating its length and width to the length and width of a standard transistor. In contrast to the ring one, standard transistor is well described in various literature and his model comes in standard technology libraries of all companies producing custom integrated circuits. For this reason, the most correct method is to construct a model based on the ELT standard transistor. The formula used to set the annular transistor to standard transistor shown in [2]:

\[
\frac{W}{L} = 4 \frac{2\alpha}{\ln \frac{d'}{d}} + 2K \frac{1 - \alpha}{2\ln \frac{1 + \alpha}{\alpha^2 + 2\alpha + 5}} + 3 \frac{d - d'}{L}
\]

when \(\alpha = 0.05\), \(K = 3.5\) (for channel length \(< 0.5\mu\)), \(d =\) inner diameter of the Gate, \(d' = d\) without the 45 Cut

With this formula, and the standard model of the transistor, we can work to characterize the standard transistor sufficiently.

3. Parametrized Cell
3.1. Parameterized CAD scheme in Virtuoso Cadence
In the CAD Virtuoso Cadence it is possible to use standard tools and specialized programming language SKILL to create Parametrization scheme(PCell). To creation Route of PCell consists of two steps: 1) Creation of a topological representation varies with the basic parameters of the transistor. 2) Creation of a schematic representation for the modeling of the transistor in the electrical circuits with the changes in the major parameters of the transistor.

3.2. Creation of ELT topology
To create a topological representation in addition to the standard software available in CAD, the formulas which will build and change the topology of future transistors are required. These formulas should consider not only the basic parameters of the transistor, and its compatibility with the physical implementation, such as the minimum possible distance between the various
layers and their compliance with the minimum step of the grid. The following are the formulas written in SKILL which build the ELT topology:

- Formula of Pcell vertical stretching according to the line 6 (Figure 1) and according to the horizontal line 7 (Figure 1). The formula takes into account the possible stretching speed and corresponds to the grid:
  \[
  fix\left(\frac{0.1(1-(L+1)E)}{1-E} + 0.56 + 2L - 2(L - 0.18) \right) * 100 * 0.01
  \]
  when
  \[
  E = exp\left(\frac{0.4L}{W - 0.5615509 * KL - 0.15}\right).
  \]

- Stretch gate formula. The formula corresponds to the grid:
  \[
  fix\left(\frac{L}{0.01}\right) * 0.01
  \]

- Formula of duplicate source contacts. The formula takes into account the possible gate tension and corresponds to the grid:
  Step duplication
  \[
  St_s = 0.5,
  \]
  the number of repetitions
  \[
  N_s = fix\left(2 \times \frac{0.1 * (1 - (L + 1)E)}{1 - E} + 0.72\right) + 0.5.
  \]

- Formula of duplicate contacts drain. Formula takes into account the possible gate tension and corresponds to the grid:
  Step duplication
  \[
  St_d = fix\left(100 \times \frac{0.1(1-(L+1)*E)}{1-E} - 0.04 - 0.5N_s \right) / N_s + 50) * 0.01,
  \]
  the number of repetitions
  \[
  N_d = fix\left(fix\left(100 \times \frac{0.1 * (1 - (L + 1) * E)}{1 - E} - 4\right) * 0.02\right).
  \]

3.3. Example of building ELT topology at different preset parameters
When the layout is changed, PCell varies submitted to the parameters. The built topologies are tested with DRC in Calibri software tool. Thus were built topologies for different parameters, they are depicted in Figure 2 and 3.

3.4. Create of ELT schematic
Inherently the ELT model of transistor is a CellView with the possibility of setting the three parameters: W, L, K. According to these parameters, the parameters of the standard N-channel transistor inside CellView and its topology.

The parameters of the transistor pleased inside CellView schematic vary according to the following formulas:
Figure 2. Constructed topology for W = 10 um, L = 0.18 um, K = 3.5.

Figure 3. Constructed topology for W = 10 um, L = 0.5 um, K = 4.

- The formula for calculating the perimeter of the source:
  \[ P_s = (0.4 \frac{1 - (pPar("L") + 1)Es}{1 - Es}) + 8pPar("L") + 2.66 \times 10^{-7} \]
  when
  \[ Es = \exp\left(\frac{0.4pPar("L")}{pPar("W") - 0.5615508536 \times pPar("K") \times pPar("L") - 0.15}\right). \]

- The formula for calculating the area of the source:
  \[ S_s = (0.139 \frac{1 - (pPar("L") + 1)Es}{1 - Es}) + 3.01pPar("L") + 0.2303 \times 10^{-13}. \]

- The formula for calculating the perimeter drain:
  \[ P_d = 0.4 \frac{1 - (pPar("L") + 1)Es}{1 - Es} \times 10^{-7}. \]

- The formula for calculating the area of the drain:
  \[ S_d = (0.1 \frac{1 - (pPar("L") + 1)Es}{1 - Es})^2 \times 10^{-13}. \]

4. Conclusion

Using standard Cadence CAD tools and mathematical calculations, there has been built a simple enclosed layout transistor PCell for the CMOS 180 nm UMC technology library.

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