Practical Floating Capacitance Multiplier Implementation with Commercially Available IC LT1228s

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Abstract: A practical realization of a tunable floating capacitance multiplier using commercially available integrated circuits, namely LT1228 is proposed. The synthetic capacitor utilizes only two IC LT1228s along with two passive components (one resistor and one capacitor). The capacitance multiplication factor is electronically controllable through the transconductance gain of the LT1228. The effects of non-ideal transfer gains and parasitic elements of the LT1228 on the circuit performance have been evaluated in detail. The applicability of the proposed floating capacitance multiplier as a second-order band-pass filter is also presented. The claimed theory is verified by several PSPICE simulations and experimental test results.

Keywords: capacitance multiplier; impedance simulation circuit; commercially available integrated circuit; electronically tunable

1 Introduction

It is well known that the capacitance multiplier is a significant electronic block in the fabrication of high capacitance values in integrated circuit (IC) technology [1]-[2]. This is due to the large-value capacitors requiring a large silicon area on the IC chip. To overcome this limiting problem, the capacitance multiplier circuit which performs the multiplication of small capacitance values can be very useful [3]-[4]. Therefore, the design of capacitance multiplier circuits becomes an essential research issue in the area of analog ICs. Over the years, there are various floating capacitance multiplier circuits reported by several researchers employing numerous versatile active elements [5]-[13]. However, careful observation of the topologies reported in these references reveals that they still suffer from one or more of the following restrictions:

1. They contain three or more active components [5]-[6], [10], [12], which enlarge the area on the chip, and relatively high power dissipation.
2. They need to employ more than two passive components [7], [9]-[10].
3. They are unavailable in commercial IC form [6]-[9], [11]-[12], which cannot be practically implemented using already existing readily available ICs.
4. They lack the electronic adjustability for the capacitance multiplying factor [7], [9]-[10]. The in-
ternal tuning feature would be desirable for modern mixed-signal systems.

5. They use different types of active components for their implementations [5], [12]-[13].

The attention aim of this work is, therefore, to design a floating and tunable capacitance multiplier using already existing commercially available ICs, namely LT1228 [14]. The LT1228 structure internally consists of an operational transconductance amplifier (OTA) and a current feedback operational amplifier (CFOA) in the same IC package. Thus, it may be noted that LT1228 has now become a popular commercial IC for designing several types of analog signal processing circuits and applications [15]-[20]. Two LT1228s and two passive components, i.e. one resistor and one capacitor, are employed in this design. The capacitance scaling factor of the simulated circuit can be altered through the tunable transconductance gains of the LT1228s and/or the resistor in the circuit. A careful non-ideality analysis for the proposed capacitance multiplier circuit is investigated in detail. The second-order RLC band-pass filter implemented with the proposed tunable active capacitance simulator is given as an application. To verify the workability of the proposed circuit, it has been simulated in the PSPICE program using macro-model of IC LT1228, and also experimentally tested in a laboratory using commercially available IC namely LT1228s.

2 Circuit description

2.1 Commercially available IC LT1228

The LT1228 is a commercially available IC manufactured by Linear Technology Corporation [14]. The LT1228 internal circuit, which has the properties of both the operational transconductance amplifier (OTA) and the current feedback operational amplifier (CFOA), is shown in Fig.1(a). The OTA provides an electronic gain control with a differential voltage-to-current converter, whose transconductance gain (\(g_m\)) depends on an external bias current, while the CFOA is implemented to drive load low-impedance loads with excellent linearity at high frequencies. The circuit representation block of the LT1228 and its equivalent circuit are given in Fig.1(b) and 1(c), respectively. In ideal operation, the function of the LT1228 can be described by the following matrix relation:

\[
\begin{bmatrix}
    i_p \\
    i_n \\
    i_z \\
    v_z \\
    v_o
\end{bmatrix} =
\begin{bmatrix}
    0 & 0 & 0 & 0 & 0 \\
    0 & 0 & 0 & 0 & 0 \\
    g_m & -g_m & 0 & 0 & 0 \\
    0 & 0 & 1 & 0 & 0 \\
    0 & 0 & 0 & R_{OL} & 0
\end{bmatrix}
\begin{bmatrix}
    v_p \\
    v_n \\
    v_z \\
    i_x \\
    i_o
\end{bmatrix}
\]

In equation (1), \(R_{OL}\) is the transresistance gain of the LT1228, which is ideally considered to be infinite. The \(g_m\)-parameter of this IC can be adaptable electronically with the help of the external bias current \(I_B\) and the expression is given by:

\[
g_m = 10I_B \tag{2}
\]

Figure 1: Commercially available IC LT1228: (a) package information; (b) electrical symbol; (c) equivalent circuit

2.2 Proposed floating capacitance multiplier design

The schematic diagram of the proposed floating capacitance multiplier circuit is given in Fig.2(a). It is composed of only two LT1228s, one resistor, and one capacitor. The equivalent circuit for the proposed capacitor implementation of Fig.2(a) is shown in Fig.2(b). Assuming that the matching condition of \(g_m = g_{m1} = g_{m2}\) is satisfied, routing circuit analysis shows that the equivalent
input impedance looking between ports \( v_1 \) and \( v_2 \) of the proposed circuit in Fig.2(a) can be obtained as:

\[
Z_{eq} = \frac{v_o}{i_m} = \left( \frac{v_2 - v_1}{i_1} \right) = \left( \frac{v_2 - v_1}{i_1} \right) = 1 + \frac{1}{sC_{eq} = s(g_m)R_C} \quad (3)
\]

It is obvious that the proposed circuit of Fig.2(a) implements a floating tunable lossless capacitance with equivalent capacitance being given by:

\[
C_{eq} = (g_m)C_1 = KC_1 \quad (4)
\]

where \( K = g_mR_1 \) represents the capacitance magnification factor. The relation in (4) reveals that the capacitance magnification with a large multiplication factor is easily feasible by appropriate choosing \( g_m \) and \( R_1 \).

Also from equation (2), the electronic tuning capability of the proposed design is evident through the bias currents of the LT1228s. It should be further noted here that two transconductance gains for this implementation need to be equal. This can be done easily by using simple current mirror to supply equal external bias currents to the two LT1228s.

![Figure 2: Proposed floating capacitance multiplier implementation: (a) circuit diagram; (b) ideal equivalent impedance](image)

2.3 Non-ideality performance analysis

Consider the non-ideal transfer gains of the LT1228, the characteristic of the LT1228 given in equation (1) can be re-described by the following matrix equation:

\[
\begin{bmatrix}
  i_p \\
  i_n \\
  i_z \\
  v_x \\
  v_o
\end{bmatrix}
= \begin{bmatrix}
  0 & 0 & 0 & 0 & 0 \\
  0 & 0 & 0 & 0 & 0 \\
  \alpha g_m & -\alpha g_m & 0 & 0 & 0 \\
  0 & 0 & \beta & 0 & 0 \\
  0 & 0 & 0 & R_{0k} & 0
\end{bmatrix}
\begin{bmatrix}
  v_p \\
  v_n \\
  v_z \\
  i_x \\
  i_o
\end{bmatrix}
\quad (5)
\]

In above equation, \( \alpha = (1 - \varepsilon_m) \) and \( \beta = (1 - \varepsilon_x) \), where \( |\varepsilon_m| << 1 \) and \( |\varepsilon_x| << 1 \) are the transconductance tracking error and the voltage transfer error, respectively. Therefore, an analysis of the simulator given Fig.2(a) with the consideration of these parasitic gains gives the following expression for the equivalent input impedance looking into port 1 and ground as:

\[
Z_{eq1} = \frac{v_1}{i_1} = \frac{1}{sC_{eq} = s(g_mR_1)} \quad (6)
\]

It is obvious that the parasitic gains \( \alpha \) and \( \beta \) directly deviate the value of the working capacitance \( C_{eq} \). To compensate for this, it can be governed by tuning the appropriate value for the \( g_mR_1 \) product. On the other hand, the non-ideal equivalent impedance looking into port 2 and ground can be approximately found as:

\[
Z_{eq2} = \frac{v_2}{i_2} = 1 + \frac{1}{sC_{eq2} + \frac{1}{R_{ex}}} \\
\quad (7)
\]

From equation (7), due to the LT1228 non-ideal gains, there is an extra undesired parallel resistance \( (R_{ex}) \) appearing in parallel with the non-ideal equivalent capacitance. The non-ideal equivalent circuit for this case can then be represented as in Fig.3, where \( C_{eq2} = (R_2C_2)(g_{m2}C_2) \) and \( R_{ex} = 1/(\beta_2-1)(g_{m2}C_2) \). Since a typical value of \( R_{ex} \) is of the order of hundreds of k\( \Omega \), the parasitic elements \( C_{eq2} \) and \( R_{ex} \) introduce an extra pole at low frequency, which restricts the operating frequency range of the circuit. This effect on the frequency response of \( Z_{eq2} \), will be shown in the following section.

![Figure 3: Non-ideal equivalent input impedance \( Z_{eq2} \)](image)
impedance values are theoretically equal to infinity. On the other hand, the parasitic resistance $R_i$ appears in series at terminal $x$. By considering $V_i = 0$, the impedance of the designed capacitor with the consideration of the parasitic element effects can be given by:

$$Z_{eq1} = \frac{V_1}{I_1} \bigg|_{v_{if} = 0} = \frac{1}{sC_{eq1}} = \frac{1}{s} \left[ \frac{g_m R C_i}{1 + \left( \frac{R_{z1}}{R_{zil}} \right)} - C_{eq1} \right]$$

where $R_{z1}, R_{z2}, R_{zil}$ and $C_{zj}$ ($j = 1, 2$) are the parasitic elements $R_{zj}, R_{zil}$ and $C_{zj}$ of the $j$-th LT1228, respectively. For practical realization, $R_{z1}$ and $R_{z2}$ are typically very large, yielding $R_{z1} \gg R_{zil}$ and $R_{z2} \gg 1$. Therefore, an equivalent capacitance $C_{eq1} \equiv (g_m R C_i - C_{eq1})$ is obtained from equation (8). It is further mentioned that there is not any additional parasitic pole and zero due to the parasitic elements, and the operating frequency limitation can be expressed as: $f \leq \min \{1/2\pi (g_m R C_i - C_{eq1})\}$.

![Figure 4: Practical LT1228 model with parasitic elements.](image)

By defining $V_i = 0$ and conducting relevant analyses, we can obtain the following expression for the non-ideal impedance seen between terminal 2 and ground as:

$$Z_{eq2} = \frac{V_2}{I_2} \bigg|_{v_{if} = 0} = \frac{1}{sC_{eq2}} = \frac{1}{s} \left[ \frac{g_m R C_i - C_{eq2}}{1 + \left( \frac{R_{z2}}{R_{zil}} \right)} \right]$$

where $R'_{z1} = R_{z1} / R_{z2}$, $R'_{z2}$ and $C_{z2} = C_{n} + C_{m} + C_{z2}$. In equation (9), the negative terms exhibit non-ideal behavior of the proposed capacitance simulator by introducing a parallel resistive effect. Since $R_{z1} \gg R_{z2}$ and $R'_{z2} \gg 1$, then equation (9) reduces to

$$Z'_{eq2} = \frac{1}{sC_{eq2}} = \frac{1}{s} \left[ \frac{g_m R C_i - C_{eq2}}{1 + \left( \frac{R_{z2}}{R_{zil}} \right)} \right]$$

The consideration of the above effect implies that in the frequency range of $f \leq \min \{1/2\pi (g_m R C_i - C_{eq2})\}$, and the inequality $g_m R C_i << C_{eq2}$, the simulator operates practically as an expected ideal capacitance multiplier.

### 3 Computer simulation validation

To verify our proposed design, the circuit in Fig.2(a) has been simulated in PSpice program using the macro-model parameters for the LT1228 provided by Linear Technology Corporation [14], with DC supply voltages of ±5 V. In simulations, the component values are taken as: $R_1 = 1 \text{k}\Omega$, $C_i = 50 \text{pF}$ and $I_i = I_{m1} = I_{m2} = 200 \mu\text{A}$. From equation (2), the transconductance gains are calculated as: $g_m = g_{m1} = g_{m2} = 2 \text{mA/V}$. Also, from the relation in (4), the capacitance multiplication factor, and the simulated equivalent capacitance are calculated as: $K = 2$ and $C_{eq} = 0.1 \text{nF}$, respectively. The simulation results for input signals $V_i$ and $i_{in}$ of the proposed capacitance multiplier are given in Fig.5, when a 1-MHz sinusoidal signal of an amplitude 50 mV (peak) was applied as an input signal. The phase difference between $V_i$ and $i_{in}$ was observed to be $86.77^\circ$ leading, as against the theoretical value of $90^\circ$. The corresponding frequency responses are also given in Fig.6. The total power consumption is measured to be 0.12 W when $V_i$ and $i_{in}$ are kept grounded.

![Figure 5: Simulation results for $V_i$ and $i_{in}$ of the proposed floating capacitance multiplier circuit in Fig.2(a).](image)

In order to evaluate the impact of the unwanted parasitic resistance $R_{ex}$, the frequency responses of the non-
ideal equivalent impedance $Z_{eq}$ ($Z_{eq} = v/i$) when $v_1 = 0$ are depicted in Fig.7. It is observed that, at low frequency range between 1 kHz and 20 kHz, $R_{eq}$ mainly causes drop of the magnitude response of the $Z_{eq}$ and also some deviates in phase response as depicted. However, some circuit techniques which reduce the parasitic impedance effects can be applied in the proposed capacitance multiplier circuit to improve the frequency performance [21]-[23].

Fig.9 shows the temperature analysis results of the proposed capacitance multiplier circuit in Fig.2(a), where the ambient temperature is changed from 0°C to 100°C in the step of 20°C. From Fig.9, the simulation results demonstrate that the magnitude response has deviated with a variation of -8% - +22% over the temperature range of 0°C to 100°C.

4 Experimental Evaluation

In the experimental evaluation, the availability of the proposed floating capacitance multiplier circuit in
Fig.2(a) has been verified in the laboratory using off-shelf IC’s LT1228 [14] under ±5V supply voltages. All experimental measurements were performed through Keysight EDU-X 1002G oscilloscope and HP4395A impedance analyzer. To perform the experimental test, the components used have been: $g_m = 2$ mA/V ($I_B = 200 \mu$A), $R_1 = 1$ kΩ, and $C_1 = 50$ pF, yielding $C_{eq} = 0.1$ nF. Fig.10 shows the measured input waveforms $v_{id}$ and $i_{in}$ of the proposed circuit in Fig.2(a), when the input signal is 100 mV peak-to-peak at 1 MHz. The phase shift between $v_{id}$ and $i_{in}$ obtained from this experiment is measured as 86.8°. The corresponding frequency responses of the equivalent input impedance $Z_{eq}$ are also represented in Fig.11. It appears from Figs.10 and 11 that the proposed circuit behaves as a lossless capacitor as expected.

So as to survey the electronic tunability of the capacitance multiplier circuit, the measured magnitude and phase responses with three different values of $g_m$ (i.e. $g_m = 0.5$ mA/V, 3 mA/V, and 5 mA/V) are shown in Fig.12. These results were obtained by taking $R_1 = 1$ kΩ and $C_1 = 50$ pF. This tuning process leads to obtain $K = 0.5$, 3 and 5 ($C_{eq} = 25$ pF, 0.15 nF, and 0.25 nF), respectively.

On the other hand, the magnitude-frequency responses of $Z_{eq}$ for different values of $R_1$ are depicted in Fig.13. In Fig.13, setting $g_m = 1$ mA/V and $C_i = 50$ pF, and different values for $R_1$ as 5 kΩ, 10 kΩ and 20 kΩ, results in the theoretical equivalent capacitances of $C_{eq} = 0.25$ nF, 0.5 nF, and 1 nF, respectively.

5 Illustrative application

In this section, illustrative applicability of the proposed floating capacitance multiplier given in Fig.2(a) has been considered. It may be utilized in the implementation of the second-order RLC voltage-mode band-pass (BP) filter as shown in Fig.14. The transfer function of the filter can be given by:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\left(\frac{R_{BP}}{L_{BP}}\right)^2 s}{s^2 + \left(\frac{R_{BP}}{L_{BP}}\right) s + \left(\frac{1}{L_{BP} C_{eq}}\right)}$$

(11)

The center frequency ($\omega_c$) and the quality factor (Q) are respectively expressed below:

$$\omega_c = 2\pi f_c = \frac{1}{\sqrt{L_{BP} C_{eq}}}$$

(12)

and

$$Q = \frac{\left(\frac{R_{BP}}{L_{BP}}\right)}{C_{eq}}$$

(13)

As an example for the circuit simulation, the following passive and active components were chosen as: $R_{BP} = 3.3$ kΩ, $L_{BP} = 1$ mH, and $C_{eq} = 0.1$ nF ($g_m = 2$ mA/V, $R_1 = 1$ kΩ).
Figure 12: Measured frequency responses of $Z_{eq}$ for different $g_m$: (a) $g_m = 0.5$ mA/V ($K = 0.5, C_{eq} = 25$ pF); (b) $g_m = 3$ mA/V ($K = 3, C_{eq} = 0.15$ nF); (c) $g_m = 5$ mA/V ($K = 5, C_{eq} = 0.25$ nF)
kΩ, and $C_1 = 50$ pF). The ideal and simulated frequency responses of the filter in Fig.14 are exhibited in Fig.15, in which the calculated and simulated values of $f_c$ are found to be 503 kHz and 509 kHz, respectively. The simulated frequency characteristics are in good agreement with the predicted responses, thereby confirming the practical utility of the proposed capacitance multiplier circuit. The corresponding frequency spectrum of the output voltage ($v_{out}$) of the BP filter is also recorded in Fig.16, where the total harmonic distortion (THD) values observed is well within 1.17%.

Finally, in order to inspect random deviations of the BP filter center frequency due to the process and mismatch variations, Monte-Carlo analysis simulation has been evaluated with the same given parameters that resulted in the frequency characteristic of Fig.15. The simulations were performed 200 times with a 5% Gaussian deviation of relevant $g_m$, $R_1$, and $C_1$. The histogram of the center frequency is shown in Fig.17. According to statistical analysis results, the mean value is at 522 kHz with a standard deviation of 9.4 kHz, corresponding to 1.8% deviation from the nominal value.
6 Conclusive Discussion

This work is an attempt to present a practical realization of the tunable floating capacitance multiplier circuit using a commercially available IC LT1228. The synthetic capacitance simulator is constructed with two LT1228s, one resistor, and one capacitor. The electronic tuning feature of the simulated floating capacitor can be achieved by means of external bias currents of the IC LT1228s. The communication further discusses a second-order RLC voltage-mode band-pass filter to validate the applicability of the proposed capacitor simulation. PSPICE simulation and experimental results of the commercially available IC LT1228 are also included to demonstrate the convincing characteristics of the proposed circuit and its practical significance.

Figure 17: Monte-Carlo analysis results showing the deviation in the standard deviations of the BP filter center frequency.

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8 Conflict of interest

The authors confirm that this article content has no conflict of interest.

9 References

1. S. Pennisi, “CMOS multiplier for grounded capacitors”, Electron. Lett., vol.38, no.15, pp.765-766, 2002. [https://doi.org/10.1049/el:20020517]
2. M. A. Al-Absi, E. S. Al-Suhaibani, and M. T. Abuelma’atti, “A new compact CMOS C multiplier”, Ana-

log Integr. Circ. Sig. Process., vol.90, no.3, pp.653-658, 2017. [https://doi.org/10.1007/s10470-016-0822-1]
3. W. Tangsrirat, “Resistorless tunable capacitance multiplier using single voltage differencing inverting buffered amplifier”, Rev. Roum. Des Sci. Techn.-Electrotechn. et Énerg, vol.62, no.1, pp.72-75, Jan-March 2017.
4. W. Tangsrirat, O. Channumsin, and J. Pimpol, “Electronically adjustable capacitance multiplier circuit with a single voltage differencing gain amplifier (VDGA)”, Informacie MDEM- J. Microelectron. Electron. Comp. Materials, vol.49, no.4, pp.211-217, 2019. [https://doi.org/10.33180/InfMDEM2019.403]
5. M. T. Ahmed, I. A. Khan, and N. Minhaj, “Novel electronically tunable C-multipliers”, Electron. Lett., vol.31, no.1, pp.9-11, Jan. 1995 [https://doi.org/10.1049/el:19950018]
6. M. T. Abuelma’atti and N. A. Tasadduq, “Electronically tunable capacitance multiplier and frequency-dependent negative-resistance simulator using the current-controlled current conveyor”, Microelectron. J., vol.30, no.9, pp.869-873, Sep.1999. [https://doi.org/10.1016/s0026-2692(99)00025-7]
7. P. V. A. Mohan, “Floating capacitance simulation using current conveyors”, J. Circuits Syst. Comput., vol.14, no.1, pp.123-128, 2005. [https://doi.org/10.1142/s0218126605002209]
8. O. Channumsin, and W. Tangsrirat, “Electronically tunable floating capacitance multiplier using FB-VDBAs”, Engineering Letters, vol. 24, no.3, pp.365-369, 2016.
9. H. Alpaslan, “DVCC-based floating capacitance multiplier design”, Turkish J. Electr. Eng. Comput. Sci., vol.25, no.2, pp.1334-1345, 2017. [https://doi.org/10.3906/elk-1509-112]
10. M. T. Abuelma’atti, Z. J. Khalifa, and S. K. Dhar, “New CFOA-based lossless floating inductor and capacitance/resistance multipliers for low frequency applications”, J. Active Passive Electron. Devices, vol.14, pp.229-237, 2019.
11. W. Tangsrirat and O. Channumsin, “Tunable floating capacitance multiplier using single fully balanced voltage differencing buffered amplifier”, J. Commun. Tech. Electron., vol.64, no.8, pp.797-803, Aug.2019. [https://doi.org/10.11134/s1064226919080163]
12. M. A. Al-Absi, A. A. Al-Khulaifi, “A new floating and tunable capacitance multiplier with large multiplication factor”, IEEE Access, vol.7, pp.120076-120081, Aug. 2019. [https://doi.org/10.1109/ACCESS.2019.2936800]
13. M. A. Al-Absi, M.T. Abulema’atti, “A tunable floating impedance multiplier”, Arab. J. Sci. Eng., vol.44,
14. Linear Technology, “100MHz current feedback amplifier with DC gain control”, LT1228 datasheet, 1994.
15. S. Siripongdee and W. Jaikla, “Universal filter using single commercially available IC: LT1228”, Proceedings of 2016 3rd International Conference on Mechatronics and Mechanical Engineering (ICMME-2016), October 21-23, Shanghai, China, p.14002, 2017.
16. A. Chaichana, S. Siripongdee, and W. Jaikla, “Electronically adjustable voltage-mode first-order all-pass filter using single commercially available IC”, Proceedings of IOP Conference Series: Materials Science and Engineering, January 19-22, Tokyo, Japan, p.012009, 2019.
17. N. Roongmuanpha, T. Suesut, W. Tangsrirat, “Electronically tunable triple-input single-output voltage-mode biquadratic filter implemented with single integrated circuit package”, Advances in Science, Technology and Engineering Systems Journal, vol.6, no.1, pp.1120-1127, 2021.
18. P. Moonmuang, N. Roongmuanpha, T. Pukkalanun, W. Tangsrirat, “On the realization of simulated lossy inductors using voltage differencing buffered amplifiers”, Proceedings of 2020 8th International Electrical Engineering Congress (IIECON), Chiang Mai, Thailand, 2020.
19. N. Roongmuanpha, W. Tangsrirat, “SITO current-mode multifunction biquad using readily available IC LT1228s”, Proceedings of The 6th International Conference on Engineering, Applied Sciences and Technology (ICEAST-2020), July 1-4, Thailand, pp. 108-111, 2020.
20. N. Roongmuanpha, T. Pukkalanun, W. Tangsrirat, “Practical realization of electronically adjustable universal filter using commercially available IC-based VDBA”, Engineering Review, vol.41, no.3, 2021.
21. A. Fabre and H. Barthelemy, “Composite second-generation current conveyor with reduced parasitic resistance”, Electron. Lett., vol.30, no.5, pp.377-378, Mar.1994.
22. F. Sequin and A. Fabre, “New second-generation current conveyor with reduced parasitic resistance and bandpass filter application”, IEEE Trans.