A Survey of Sobel Edge Detection VLSI Architectures

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Abstract. Edge detection is an essential process used to determine the object margins in most of the computer vision applications. Sobel edge detection algorithm, which is a simple method of edge detection, detects edges of various objects in an image. Real-time image applications need to be processed with large pixel data for a given time interval. So, Most of the VLSI architectures proposed for implementing sobel edge detection systems use FPGA, due to the parallel computing and reconfigurable feature. So, this paper introduces various VLSI architectures of sobel edge detection and compares the parameters like execution time, power dissipation with respect to similar input image size, different clock frequencies.

Keywords: Sobel Edge detection, VLSI architectures, FPGA, Power dissipation.

1. Introduction

The edge detection is an important method for computer vision. The change of image brightness is represented as an edge of an object. According to digital terminology, an edge is said to be the set of pixel values, which changes abruptly. The good detection of edges defines the good image processing for different applications. There are different types of edge detection depending on gradient calculation, filtering techniques etc.

The sobel edge detection technique is simple and preferred for implementing large set of images. Convolution is performed for the image pixel values with suitable kernel to obtain the gradients in horizontal and vertical directions. Comparing the pixel values of the image with their neighbouring pixel values is called as Conventional edge detection. The convolution calculation is involved in the Sobel operator by implementing it with appropriate kernels. The gray-scale image pixel values are taken as memory into the FPGA and the gradient computation is performed.

2. Sobel Edge Detection Algorithm

The edge detection process is generally performed using first and second order derivatives. The gradients are computed from the first order derivative. Sobel, Prewitt and Roberts operator are the various gradient operators. Laplacian and Gaussian come under the second order. Getting the edges using canny is a way to get the optimal edge detection.
For Edge discovery here we use the Sobel operator which is especially useful for the image processing and the edge calculation. In the sobel algorithm, edge calculation for the image operations is performed. It will be done by using the strength of the input image provided. \( G_x, G_y \) are the gradient values in the horizontal and vertical direction, which are obtained by performing convolution two 3x3 kernels, which is given in the figure 1 below.

\[
G = |G_x| + |G_y|
\]  

3. Literature Survey
Over the last few decades, so much research is going on based on developing hardware architectures for sobel edge detection. In 1994, Boo et al. [1] implemented sobel edge detector in hardware using VLSI technology by. In 2007, a Sobel edge detection architecture using FPGA was presented by T.A. Abbasi et al. [2] which is having the problem with complexity in time and space. Afterwards, architecture was proposed by S. Halder et al. [3], which saves the time and consumes smaller space when compared to [2].

In 2019, Hounghun Joe et al. had proposed the Stochastic computing method. This method uses Stochastic number computing which is of two types, uni-polar and bi-polar encoding. They had implemented the Stochastic computing using wire exchanging technique [21]. Zou Xiangxi et al. proposed the Sobel architecture in eight directions with FPGA pipeline processing architecture and parallel processing technology to improve processing speed [22]. Kun Zhang et al. implemented the various modules of enhanced sobel edge detection using FPGA [23].

Nazma Nausheen et al. proposed a simplified method of Traditional Sobel Edge Detection [24]. Baoshan You et al. used an efficient method, OpenCL, as a new scheme for the implementation [25]. Sobel Edge Detection system was designed using System Generator in [26, 28]. Yu Zheng et al. had implemented sobel IP core design using high level synthesize method and realized on Zynq FPGA kit [27].

An improvement of the edge detection implementation using chip statistics of which FPGA devices used for sobel algorithm is proposed in [29]. Jie Tian et al. developed a real-time edge detection system using FPGA and DDR2, which resulted in greater performance [30]. In [31], sobel edge detection is developed by calculating and comparing various parameters of image processing like Correlation, Peak Signal to Noise Ratio etc.

In 2014, Sanjay Singh et al. implemented Sobel operator using two parallel, pipelined processing elements and buffer memory architecture [32]. Girish Chap et al. developed edge detection technique on different FPGA devices and analyzed the results [33]. Sobel edge detection architecture had been proposed which include a dedicated hardware with a processor having the memory buffer [34]. In [35], Sobel edge detection technique was evaluated as a 2D spatial gradient of every image pixel using convolution and line scan edge detector.

Eng. Dina Alghurair et al. compared the cost analysis sobel edge detection algorithm development using different Xilinx FPGA device like Spartan and vertex families [36]. Ch. Spandana et
Prathyusha et al. worked on sobel edge detection for an image in noisy conditions implemented on ASIC board using Xilinx Platform Studio (XPS) [39].

Rajesh Mehra et al. designed an algorithm using pipelined architecture for sobel edge detection that is implemented for the serial image. The proposed design was implemented using a two dimensional filter which does the convolution of input image matrix using sobel filter [40]. Abdul Raouf Khalid et al. proposed the architecture for sobel algorithm using parallel adders and sequential comparators for different range of frequency applications, in which the parallel processing reduces the access time of image pixels placed in the memory [41]. A hardware ASIC architecture was presented for implementing real-time edge detection on FPGA considering Sobel algorithm on input images of size 1024x1024 [42]. Varun Sanduja et al. developed the parallel architecture of Sobel operator based edge detection using FPGA which reduces the complexity of the design and also reduces the processing time [43].

In 2011, Sudeep KC et al. implemented various edge detectors at a rate of 60 fps for a 720x480 input image and compared the gradient based and compass edge detection methods using FPGA [44]. I.Yasri et al. implemented the edge detection using FPGA technology to get high performance for image processing which is of low cost, reduction in time, flexibility and many others advantages [45]. The spatial and temporal parallelism of the FPGA is used for implementing image processing algorithms like sobel edge detection filters and an anisotropic diffusion filter [46].

Roberto Lopez Rosas et al. developed the sobel algorithm using Single Instruction Multiple Data (SIMD) architecture which consists of an arrangement of processing elements that carry out similar operation over dissimilar data. This architecture reduces the number of FPGA elements consumed by the sobel detection algorithm [17]. In [47], a new internal FPGA architecture was introduced to reduce the power dissipation and cost of edge detection system. Santanu Halder et al. proposed architecture for the generation of sobel edge detection of an image, using various blocks namely adder/divider block, subtractor block, and comparator block [3]. Vanishree et al. presented the Sobel edge detection algorithm with pipelined implementation using VGA (Video Graphics Array), which is the interface used to connect the FPGA for displaying the image having edges [48].

The sobel edge detection was implemented using combinational block architecture, which will make use of various FPGA features like parallelism, I/O Capabilities [49]. In [50], Sobel edge detector was developed with a combination of registers and block memory which compares the parameters like area and performance. The paper [51] describes the Sobel IP block development using Zynq TRD (Targeted Reference Design) with the help of Vivado HLS tool.

4. Sobel edge detection VLSI architectures

The Sobel edge detection VLSI architecture proposed in [21], uses stochastic computing methodology and developed for an ASIC made up of 45nm process. The adders, multipliers and multiplexers are based on stochastic computing, which reduces power consumed and resources utilized. Stochastic computing is the method derived from probability, which increases precision. Figure 2 below shows the VLSI architecture of sobel edge detection developed using stochastic computing.

In [18], the sobel edge detection architecture is improved by adding the convolution block for 45° and 135°, which contains buffers, adders, shifters etc is shown in figure 3 and 4 below. The architecture uses parallel adders, line buffers and no multipliers, which increases the performance and reduces the execution time. Abbasi et al. has proposed the hardware architecture for sobel edge detection using extra flip-flops, given in figure 5. The additional flip-flops are placed to increase the speed of operation [5].

Four different types of memories are proposed for sobel edge detection using external memory, buffers, block RAMs, registers. The first type of memory consists of input buffers and external memory. The second memory design is made up of buffers and registers. The third memory is based on block RAMs and fourth type of memory design includes block RAMs and registers. The proposed memory system is shown in figure 6 below [50].
Figure 2. Sobel edge detection architecture using stochastic computing

Figure 3. Sobel Edge Detection System

Figure 4. Convolution operation using parallel adders, buffers, shifters
Figure 5. Hardware architecture sobel edge detection using extra flip-flops

In [49], a processor block has been proposed to perform sobel edge detection which consists of adders, shifters and registers. The architecture of processor reuses the data with the help of two successive output rows, which optimizes the FPGA resources for sobel edge detection, which is shown in figure 7 below. The low power architecture of sobel edge detection system block given in figure 8 below consists of carry skip adders, sequential comparators and absolute difference calculation unit. This architecture utilizes less number of blocks when compared to conventional sobel edge detection systems [41].
Figure 7: Processor Architecture of Data Reuse
5. Comparison and Discussions

Table 1 and Table 2 shown below, compares various VLSI architectures of sobel edge detectors based on execution time and power dissipation with respect to different image sizes respectively. It is clearly observed from Table 1 that, for an input image of resolution 128x128, [48] proposes the hardware architecture for sobel edge detection technique that executes in 0.000012 ms time, which operates faster than remaining hardware architectures.

Table 1. Execution time of different sobel edge detection VLSI architectures

| Clock Frequency (MHz) | Image Size          | Execution Time (ms) |
|-----------------------|---------------------|---------------------|
| [24] 504.007          | 128x128             | 0.032               |
|                      | 512x512             | 0.052               |
| [33] 40               | 640X480             | 7.696               |
|                      | 48                  | 6.412               |
| [3] 190.840           | 512X512             | 1.28                |
|                      | 1024X768            | 3.84                |
| [48] ----             | 128X128             | 0.000012            |
| [49] ----             | 512X512             | 1.95                |
| [50] 142.82           | 320X320             | 5.67                |
|                      | 139.80              | 0.73                |
|                      | 123.20              | 0.84                |
|                      | 134.73              | 0.77                |

Figure 8. Low power architecture of sobel edge detection
It is observed from table 2, that with an image size of 512x512 and clock frequency of 329.75 MHz, the power dissipated for sobel edge detection system VLSI architectures [21] is less than that of other architectures.

| Power dissipation for various sobel edge detection VLSI architectures |
|-----------------|-----------------|-----------------|
| Clock Frequency (MHz) | Image Size | Power Dissipation (mW) |
| [21] | 329.75 | 512X512 | 1.29 |
| [40] | 148.133 | ---- | 103.13 |
| [41] | 300 | 640X480 | 27.31 |

6. Conclusion
This paper analyzes different VLSI architectures of Sobel edge detection systems. Most of the systems are implemented using FPGAs for gaining the advantage of parallel computation and only a few are implemented using ASIC, GPUs etc. The parameters such as execution time and power dissipation are compared with respected to similar input image size, but with varied clock frequencies.

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