Scaling Analysis of Nanowire Phase Change Memory

Jie Liu, Bin Yu Fellow IEEE, and M. P. Anantram

Abstract—This letter analyzes the scaling property of nanowire (NW) phase change memory (PCM) using analytic and numerical methods. The scaling scenarios of the three widely-used NW PCM operation schemes (constant electric field, voltage, and current) are studied and compared. It is shown that if the device size is downscaled by a factor of 1/k (k>1), the operation energy (current) will be reduced by more than k³ (k) times, and the operation speed will be increased by k² times. It is also shown that more than 90% of operation energy is wasted as thermal flux into substrate and electrodes. We predict that, if the wasted thermal flux is effectively reduced by heat confinement technologies, the energy consumed per RESET operation can be decreased from about 1 pJ to less than 100 fJ. It is shown that reducing NW aspect ratio (AR) helps decreasing PCM energy consumption. It is revealed that cross-cell thermal proximity disturbance is counter-intuitively alleviated by scaling, leading to a desirable scaling scenario.

Index Terms—Phase change memory, nanowire, device scaling, RESET current and energy, electro-thermal transport.

I. INTRODUCTION

THE non-volatile phase change memory (PCM) is promising to replace the flash memory [1]-[2]. As an alternative of the most popular thin film PCM, the novel nanowire (NW) and NW-like pore-shaped PCM researches are gaining momentum in recent years [3]-[9]. However, in these emerging researches, the NW radius, length, aspect ratio (AR), and operation scheme, which all exert significant impacts on device performance, are chosen largely at will and exhibit very large variance. To better understand and harness these influencing factors, and thereby to take advantage of the superior scalability of PCM technology, we present a unified scaling analysis of NW PCM performance by using both analytic and numerical methods. Our analysis reveals the promising scaling scenario by presenting the scaling laws of the crucial physical quantities which determine the PCM device performance. This work is inspired by the temperature scaling analysis in reference [10]. Our focus here is the diffusive transport region, in which the device dimension (tens of nm) is much larger than carrier mean free path ℓ_MFP (ℓ_MFP<1 nm [11]).

II. ANALYTIC SCALING ANALYSIS

NW PCM research is still at its early stage and the device operation schemes are diverse. To perform the RESET operations, the existing NW PCM work use either constant current [4]-[6] or constant voltage [7]-[9] pulses. Also, it was shown that the threshold switching of SET operations exhibit constant field scaling [6]-[7]. In this section, we will provide a general analysis and comparison of the scaling behaviors in the constant electric field, voltage and current operation schemes.

In the cylindrical coordinate as shown in Fig. 1, the governing equations of electro-thermal transport in NW PCM before and after isotropic scaling are

\[ \rho \mathbf{J}' = \mathbf{E}' = -\nabla \mathbf{V}' = -\nabla \mathbf{V} = \mathbf{E} \alpha = \rho \mathbf{J} \alpha \]  
\[ c \partial_t T - \kappa (r \partial_r T + \partial_z T) - \kappa \partial_z T - \rho \mathbf{J}'^2 \]  
\[ = c \partial_t T - \kappa (r \partial_r T + \partial_z T)k^2 - \kappa \partial_z T/k^2 - \rho \mathbf{J}'^2 \Sigma \alpha' k^2 \] (2)

where \( r'=r/k, \ z'=z/k \) (k>1), \( t'=t/k \). \( \alpha' \) is determined by how the electric field behaves with scaling in Eq. (1). \( \beta \) is chosen to keep Eq. (2) invariant after scaling. Here, we use the variables without (with) prime to denote quantities before (after) scaling. The meanings of the symbols are listed in Fig. 1 and Tab. 1. We observe that: (i) If electric field is kept constant in scaling (\( \mathbf{E}'=\mathbf{E} \)), Eq. (1) requires \( \alpha=1 \) and \( \mathbf{V}'=\mathbf{V}/k \); Eq. (2) is invariant if \( T'=Tk^2 \) and \( \beta=1/k^2 \). As typical pulse duration is long enough for temperature to reach its steady state, making the pulse width longer than \( t'=tlk^2 \) will not increase the temperature beyond \( T'=Tk^2 \) and the PCM cell can never be switched to the RESET state. (ii) If voltage is kept constant in scaling (\( \mathbf{V}'=\mathbf{V} \)), Eq. (1) requires \( \alpha=k \); Eq. (2) is invariant if \( T'=T \) and \( \beta=1/k^2 \). This indicates that the temperature amplitude does not change but the time required to reach the same amplitude is reduced by \( k^2 \) times [10]. (iii) If current is kept constant in scaling (\( I'=I, \ \mathbf{J}'=J/k^2 \)),

---

Fig. 1. Schematic NW PCM geometry (left) and default parameters used in the simulation (right) – specific heat capacity c, thermal conductivity \( \kappa \), electrical resistivity \( \rho \), Ge, Sb, Te (GST) melting point \( T_m \), GST latent heat \( L \), and thermal boundary resistance \( R_b \) at GST-Pt interface and GST-SiO₂ interface.

| Material | c (J/m²K) | \( \kappa \) (W/mK) | \( \rho \) (Ω·m) |
|----------|-----------|-----------------|--------|
| GST      | 1.30×10⁻⁶ | 0.46            | 4.16×10⁻⁴ |
| SiO₂     | 1.94×10⁻⁶ | 1.40            | 1×10⁻⁶   |
| Pt       | 2.84×10⁻⁶ | 71.6            | 1×10⁻⁷   |

| Parameter | Value |
|-----------|-------|
| \( R_b \) | 20 m²K/GW |
| \( T_m \) | 905 K |
| \( L \)  | 1.121 GJ/m³ |

---

Manuscript received June 7, 2011. This work is supported by the U.S. National Science Foundation under Grant Award Number 1006182.

Jie Liu and M. P. Anantram are with the Dept. of Electrical Engr., Univ. of Washington, Seattle, 98195, WA, USA (e-mail: lijie@uw.edu; anant@uw.edu). Bin Yu is with the College of Nanoscale Sci. & Engr., State Univ. of New York, Albany, NY, USA (email: byu@uamail.albany.edu).
Eq. (1) requires \( \alpha = k^2 \) and \( V = k^2 \); Eq. (2) is invariant if \( T' = k^2 T \) and \( \beta = 1/k^3 \). This means that the temperature amplitude becomes \( k^2 \) times larger than that before scaling even the pulse duration is reduced by \( k^3 \) times. Special attention should be paid to the sharply increase electric field \( E' = Ek^2 \), because this intensifies electro-migration, which limits the lifetime of device.

The scaling factors are summarized in Tab. I. We can see that, in all of the three cases, \( r \) is scaled by a factor of \( 1/k^2 \), indicating that the changing speed of \( T \) is \( k^2 \) times faster in the scaled PCM. So, the RESET speed will be increased by \( k^2 \) times. The SET speed, however, is largely determined by crystallization speed, instead of changing speed of \( T \). Therefore, although experiment has shown that SET time can be reduced from about 100 ns to less than 10 ns if PCM cell size is scaled from 500 nm to less than 50 nm [3], a microscopic theoretical analysis is required to quantitatively define the impact of scaling on SET speed. Since RESET and SET operations adopt the constant voltage [7] and constant field [12] scaling, the RESET and SET energy \( Q \) (current \( I \)) scaling factors are \( 1/k^3 \) (1/k) and \( 1/k^5 \) (1/k^2), as shown in Tab. I.

| Tab. I. Analytic Scaling Factors |
|---|
| \( r \) radius | \( 1/k \) | \( 1/k \) | \( 1/k \) | \( 1/k \) |
| \( l \) length | \( 1/k \) | \( 1/k \) | \( 1/k \) |
| \( R \) resistance | \( k \) | \( k \) | \( k \) |
| \( E \) electric field | \( 1/k \) | \( 1/k \) |
| \( V \) voltage | \( 1/k \) | \( 1/k \) |
| \( I \) current | \( 1/k^2 \) | \( 1/k \) |
| \( J \) current density | \( 1/k \) | \( k \) |
| \( T \) temperature | \( 1/k^2 \) | \( 1/k \) |
| \( t \) time | \( 1/k^2 \) | \( 1/k \) |
| \( P \) power | \( 1/k^3 \) | \( 1/k \) |
| \( Q \) energy | \( 1/k^3 \) | \( 1/k \) |

III. Numerical Scaling Analysis

The aforementioned analytic scaling analysis reveals the benefits of scaling to reduce energy consumption and to increase device operation speed. However, firstly it did not include the latent heat of melting; and secondly it scaled the thermal boundary resistance (TBR) \( R_{\text{in}} = \Delta T/kV T \) artificially to \( R_{\text{in}} = R_{\text{in}}/k \). Here, \( \Delta T \) means the temperature discontinuity (\( \Delta T > 0 \)) at material interface. To overcome these drawbacks and obtain a more accurate scaling analysis, we numerically solve the Laplace equation \( \nabla^2 V = 0 \) to obtain current density \( J = -\rho/\nabla V \). Then heat equation (Eq. (2)) is solved for temperature distribution by using the time dependent finite element method (TD-FEM). In solving Laplace’s equation, the Dirichlet boundary condition \( V_s \) and \( V_f \) are applied at top and bottom Pt surface, as shown in Fig. 1. In solving the heat equation, the Dirichlet boundary condition \( T = 300 \) K is imposed at top and bottom Pt surface. At \( r = 0 \) and at \( r = r_{\text{NW}} + r_{\text{cap}} \), the homogeneous Neumann boundary conditions are applied for both \( T \) and \( V \). The \( V_s \) and \( V_f \) are chosen so that the maximum value of \( T(R_{\text{NW}}, z, t) \) exceeds \( T_{\text{in}} \) because this ensures one cross-section of NW is melted within pulse duration time \( t_R \) and then quenched to amorphous state at \( r > r_k \) when the pulse is off.

By using the method outlined above and parameters shown in Fig. 1, the scaling behaviors of crucial physical quantities that determine NW PCM RESET performance are shown in Fig. 2-3. In these plots, \( r_{\text{NW}} = 40/k \) nm; \( l_{\text{NW}} = r_{\text{NW}} \times \text{AR} \) nm; and \( \Delta t' = 20/k^2 \) ns. The four components (radial heat loss into SiO2 substrate \( Q_{\text{rad}} \), axial heat loss into Pt electrodes \( Q_{\text{in}} \), energy used due to heat capacity \( Q_{\text{cap}} \), and energy used due to latent heat \( Q_{\text{lat}} \)) that determine RESET energy \( Q \) are plotted in Fig. 2-3 (c). Here, \( Q_{\text{rad}} (Q_{\text{in}}) \) is obtained by integrating the thermal flux at the GST-SiO2 (GST-Pt) interface. It is obvious that more than 90% of the RESET energy is wasted as thermal energy loss into substrate and electrodes. For example, for NW with \( r_{\text{NW}} = 20 \) nm (leftmost points of Fig. 2-3 with AR=1), \( Q = 0.64 \) pJ, which consists of \( Q_{\text{rad}} = 0.27 \) pJ, \( Q_{\text{in}} = 0.32 \) pJ, \( Q_{\text{cap}} = 0.04 \) pJ, and \( Q_{\text{lat}} = 0.01 \) pJ. Actually, only \( Q_{\text{cap}} + Q_{\text{lat}} \approx 50 \) fJ is necessary to achieve the RESET operations. The wasted \( Q_{\text{rad}} \) and \( Q_{\text{in}} \) consume 92% of \( Q \). So, confining heat during RESET operation has the potential to improve energy efficiency by one order of magnitude. To do this, one can either use substrate and electrodes with small effective \( \kappa \) or use materials which have large TBR with chalcogenides (see inserts of Fig. 2-3(c)). Our simulation reveals that if \( \kappa \) values of the Pt and SiO2 regions are decreased by 2 orders of magnitude, the RESET energy (current) can be reduced by 60%-70% (40%-50%).

To more clearly reveal the quantitative scaling relations, the numerical scaling factors are listed in Tab. II. From Fig. 2-3(b) and Tab. II, we can see that RESET operation adopts constant voltage scaling roughly. The numerical scaling factors of \( E, V, I, J, P, \) and \( Q \) are slightly smaller than the corresponding analytic scaling factors shown in Tab. I. So, Tab. I is a lower limit of the improvement in device performance during scaling. We have shown that in constant voltage scheme, \( T' = T \). This means that the thermal proximity effect is kept the same during scaling. However, this conclusion is based on \( R_{\text{in}} = R_{\text{in}}/k \). In the spatial scale of our interest (tens of nm), we expect \( R_{\text{in}}' \approx R_{\text{in}} \). So, downsizing will alleviate the thermal proximity disturbance.

Fig. 2-3 and Tab. II tell us that the above scaling conclusions are valid for various AR values. Fig. 4 reveals that decreasing the AR reduces the energy required but at the cost of increasing \( I \). As large \( I \) limits the cell selector size and, hence, the data density, we need to strike a balance between energy efficiency and data density to select an appropriate AR value.

In this work, \( \kappa \) and \( T_{\text{in}} \) are chosen to be the bulk values. In the nm-scale, \( \kappa (T_{\text{in}}) \) can be suppressed due to modified phonon dispersion (interfacial energy |4|)[9]. So, the scaling scenario will be even better than those listed in Tab. II and Fig. 2-3.

In our analysis, we have neglected barriers (Schottky or other barriers) at Pt-NW interface, which can modify heat dissipation leading to hot spots. The temperature dependence of resistivity is also neglected. These issues deserve future investigation.
than 90% of the operation energy is wasted as thermal flux into substrate and electrodes. If heat can be effectively confined, the energy consumed per RESET operation can be reduced from about 1 pJ to less than 100 fJ.

REFERENCES

[1] P. H. Wong, S. Rao, and S. Kim, etc., “Phase change memory”, Proc. of the IEEE, vol. 98, no. 12, pp. 2201-2227, 2010.
[2] G. W. Burr, M. J. Breitwisch, and M. Franceschini, et al., “Phase change memory technology,” J. Vac. Sci. & Tech. B, vol. 28, pp. 223–262, 2010.
[3] W. J. Wang, L. P. Shi, and R. Zhao, etc., “Fast phase transitions induced by picosecond electrical pulses on phase change memory cells”, Appl. Phys. Lett., vol. 93, pp. 043121, 2010.
[4] B. Yu, X. H. Sun, and S. Ju, etc., “Chalcogenide-nanowire-based phase change memory”, IEEE Trans. on Nanotechn., vol. 7, pp. 496-502, 2008.
[5] S. H. Lee, Y. Jung, and R. Agarwal, “Highly scalable non-volatile and ultra-low-power phase-change nanowire memory,” Nature. Nanotechn., vol. 2, pp. 626-630, 2007.
[6] S. H. Lee, Y. Jung, and R. Agarwal, “Highly scalable non-volatile and ultra-low-power phase-change nanowire memory,” Nature. Nanotechn., vol. 2, pp. 626-630, 2007.
[7] D. Yu, S. Brittman, and J. S. Lee, “Minimum voltage for threshold switching in nanoscale phase change memory,” Nano. Lett., vol. 8, pp. 3429-3433, 2008.
[8] S. Meister, D. T. Schoen, and M. A. Topinka, et al., “Void formation induced electrical switching in phase-change nanowires,” Nano. Lett., vol. 8, pp. 4562–4567, 2008.
[9] X. H. Sun, B. Yu, and G. Ng, et al., “Germanium antimonide phase change nanowires for memory applications,” IEEE Trans. on Electron Devices, vol. 55, pp. 3131–3135, 2008.
[10] S. Kim, and H. P. Wong, “Analysis of Temperature in Phase Change Memory Scaling,” IEEE Elect. Dev. Lett., vol. 28, pp. 697-699, 2007.
[11] J. Lee, Z. Li, and J. P. Reifenberg, et al., “Thermal conductivity anisotropy and grain structure in GeSbTe films,” J. Appl. Phys., vol. 109, pp. 084902, 2011.
[12] A. Pirovano, A. Lacaita, and A. Bonventi, et al., “Scaling analysis of phase-change memory technology,” IEEE Electron Devices Meeting, 2003.