PERFORMANCE EVALUATION OF SPWM TECHNIQUES FOR SINGLE-PHASE FIVE-LEVEL INVERTER

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https://doi.org/10.26782/jmcms.2019.12.00051

Abstract

In this, present a single-phase five-level inverter for high power applications. Whenever grid-connected system mainly focuses on maintaining less THD and less switching losses. The projected topology has a minimum number of switches as associated with existing topologies. In case, the inverter has a number of switches it produces high THD and switching loses similar more driving circuits are required. So in this proposed topology consider less number switches. Similarly, SPWM control technique is utilized to control the inverter. In SPWM techniques, level shifter modulation is implemented for proposed topology. With the help of Matlab software, the proposed topology is simulated and get results.

Keywords: DC-DC converter, SPWM, Five-level inverter, single-phase inverter.

I. Introduction

In present days usage and implementation of renewable energies are high. In India, the usage of renewable energies increases as compared to earlier years. To generate electric power from renewable sources like solar, wind, tidal and nuclear etc[II]. Whenever to generate power from solar dc boost converter is compulsory. To step up the energy from solar and give that energy to the inverter to run ac load like drives [VI]. The main role of invert is to change dc to ac power with the desired magnitude and frequency [XIII]. In inverters mainly five-level inverters are suitable for grid-connected applications. In generally five-level inverters are diode clamped, Flying capacitor and cascaded H-bridge this three are basic conventional five-level inverters. Out of this, the cascaded inverter is more suitable for grid-connected systems [IX]. The proposed topology also suitable for grid-connected applications. In projected topology contains only five switches for generating five levels [XII,IV].
In inverter total, five swathes are utilized, out of five switches three switches are functioned at high frequency and reaming switches are functioned at fundamental frequency [V,III,I]. In one switch contains around four diodes arranged like a bridge, those diodes are operated in both the direction of current flow. In this, controlling for switches, sinusoidal pulse with modulation technic is used, in that SPWM, Level-Shifted is implemented for controlling inverter. Here four carries and one sine wave is compared to produce the required pulse for each switch. For generating five-level output consider m-1 carriers [X]. In SPWM level-shifted five carrier modulation scheme has again classified into three types [VII-VIII]. Those are Phase Disposition (PD), Phase Opposite Disposition (POD) and Alternative Phase Opposite Disposition (APOD).

II. Simulation of the conventional boost converter

In power electronics converters are placed a vital role. In a conventional boost, the converter is considered for a step up the supply voltage. In boost converter input voltage is 115v, here input is simply dc voltage source is considered, otherwise, any renewable energy is considered like solar, wind, nuclear, tidal, etc. In this boost up the supply of 100v to 400v, converter output is given to the single-phase five-level inverter. In a boost, converter considers inductor, diode, capacitor, and switch. Fig.1 represents the conventional boost converter, inductor values, and capacitor values are taken as per the modelling of the boost converter.

\[
\begin{align*}
V_{in, min} & = \text{Minimum input voltage} \\
f_s & = \text{Switching frequency} \\
V_{out} & = \text{Initial output voltage} \\
\eta & = \text{Efficiency} \\
D & = \text{Duty cycle} \\
\Delta i & = \text{Input current} \\
\Delta v & = \text{Output voltage ripple} \\
I_{ripple} & = \text{Inductor ripple current}
\end{align*}
\]
Inductor and capacitor mathematical model is explained in equation 1 and 2. In this duty cycle is plays a very important role, the duty cycle varies from 0 to 1. In this 0.5 duty cycle is considered. Equation 3 and 4 explain the duty cycle and input current of the converter.

\[ L = \frac{V_{in}^* (V_{out} - V_{in})}{(\Delta t + f_s v_{out})} \]  
(1)

\[ C = \frac{I_s D}{f_s \Delta v} \]  
(2)

\[ D = 1 - \frac{V_{in_{lim}} \cdot \eta}{v_{out}} \]  
(3)

\[ \Delta i = I_{ripple} \cdot I_{out} \cdot \frac{v_{out}}{V_{in}} \]  
(4)

III. Projected single-phase five-level inverter

In generally five-level inverters are mostly used in grid-connected and drive applications. Similarly, with the help of five-level inverters to get near to sine waveform. The main basic topologies for five-level inverters are diode clamped, flying capacitor and cascaded H-bridge. Our proposed topology has very less number of switches as compare with existing topology’s and it produces minimum switching losses as well as less %THD. The projected topology is operated in five modes. Fig. 2 indicates the single-phase five-level inverter.

![Fig. 2 single-phase five-level inverter](image)

It contains two capacitors and five switches, out of five switches 1, 2 and 5 are functioned at high frequency and reaming two are functioned at low frequency. The working operation of interval switches for every stage differs within a definite time. The operating stages are divided as follows. Fig. 3 indicates the four modes of operation for the proposed inverter.

\[ Mode \ 1: 0 < \omega t \leq \theta_1, \quad \theta_2 < \omega t \leq \pi \]  
(5)

\[ Mode \ 2: \theta_1 < \omega t \leq \theta_2, \]  
(6)

\[ Mode \ 3: \pi < \omega t \leq \theta_3, \quad \theta < \omega t \leq 2\pi \]  
(7)

\[ Mode \ 4: \theta_3 < \omega t \leq \theta_4, \]  
(8)
Here high switching frequency means carrier frequency and low switching frequency means fundamental frequency. In this switch 5 contains four diodes, arranged as a bridge. Switch 1 and 2 in one leg and switch 3 and 4 are in another leg. In mode one, switch 5 and 4 are on, in this case, to get $V_o/2$ as output voltage. In mode two, switch 1 and 4 are on, in this case, to get $+V_o$ output voltage.

In mode three, switch 5 and 3 are on, in this case, to get $-V_o/2$ as output voltage. In mode four, switch 2 and 3 are on, in this case, to get $-V_o$ output voltage.

Table 1 explains the switching states operation for single-phase five-level inverter.

| S. No | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | Voltage ($V_o$) |
|-------|-------|-------|-------|-------|-------|-----------------|
| 1     | N     | Y     | N     | Y     | Y     | $+V_o/2$       |
| 2     | Y     | N     | N     | Y     | N     | $+V_o$         |
| 3     | Y (or) | N (or) | Y (or) | N (or) | N     | 0              |
| 4     | N     | N     | Y     | N     | Y     | $-V_o/2$       |
| 5     | N     | Y     | Y     | N     | N     | $-V_o$         |

Y→ Yes, N→ No
IV. Sinusoidal pulse with modulation

In sinusoidal pulse with modulation mainly to produce pulses for controlling switches. In this, mainly two waveforms are compared and generate a pulse for switching operation. Mostly sine and triangle waves compare and produce a pulse. Here, triangle frequency and sine frequency are different, triangle frequency greater than sine frequency. In this, mainly consider amplitude modulation and frequency modulation. The frequency modulation is $M_f = f_c / f_r$ and amplitude modulation is $M_a = V_r / V_C$. In SPWM mainly focus on phase-shifted modulation and level-shifted modulation techniques.

IV.i. Level-Shifted Multi carrier Modulation

In level-shifted triangles are compared with sine, in this m-1 triangles are consider for m-level inverter and those triangles are compared with single sing for producing pulsed. Here, four triangles are considered all triangles have equal magnitude and frequency.

![Fig. 4PD, POD, APOD Modulation scheme](image)

In the level-shifted arrangement of triangles are different, based on the technic scheme again level-shifted classified into three types, those are Phase Disposition (PD), Phase Opposite Disposition (POD) and Alternative Phase Opposite Disposition (APOD). Fig. 4 indicates the Level-Shifted Modulation.

In this, carrier waves contain 2k Hz frequency and 50 Hz fundamental frequency are considered. Hence, Frequency Modulation ratio, $M_f = (f_s / f_r)$. Individual carrier signal compared with a sine wave to produce pulses for inverter switches.
Fig. 5 Separate switching pulses for inverter switches

In fig. 5 represents the separate switching pulse for inverter switches. For pulse one, reference sine is associated with all four carrier waves to produce the required continues pulse for switch 5. For pulse two, reference sine is associated with carrier 2 and 4 to generate therequired pulse for switch 1. For pulse three, reference sine is associated with carrier 1 and 3 to generate therequired pulse for switch 2. For pulse four, reference sine is associated with carrier 1 and 2 to generate therequired pulse for switch 3. For pulse five, reference sine is associated with carrier 3 and 4 to generate therequired pulse for switch 5. Finally, fig. 6 signifies the Simulink model for single-phase five-level inverter using Level-Shifted control technique.

Fig. 6 Simulink model for single-phase five-level inverter with Level-Shifted technique

V. Results

In conventional boost convert the dc input voltage is considered 100v and to get 400v as an output of boost converter. Fig. 7 represent the boost output voltage and current. By applying 400v dc to the inverter to get stare case five-level ac output voltage. In this, 400V voltage and 9.38A current getting from the output side of the boost converter.
After getting ac output from the inverter, that output voltage is connected to the resistive load. Fig. 8 represents the load voltage and current. In this, to get 400V voltage and 1.66A current from the load side of the inverter.

In this clearly, observe the dc-bus voltage of the inverter at various loads. Here, 250Ω resistive load is considered. Fig. 9 indicates the DC-Bus voltage at 250Ω.
Table 2 represents the inverter DC-Bus voltage at variable load conditions. Here, the %THD for the inverter with varying modulation index was analysed. Fig. 10 indicates the graphical representation of DC-Bus voltage vs Load.

Table 2: Inverter DC-Bus voltage at variable load conditions

| DC-Bus Voltage | Load |
|---------------|------|
| 400.2         | 250Ω |
| 375.8         | 200Ω |
| 343.6         | 150Ω |
| 298.8         | 100Ω |
| 229.8         | 50Ω  |

Fig. 10: Graphical representation of DC-Bus voltage vs Load.

In the modulation index varying from 0.4 to 1.1, Fig. 11 shows the THD analysis for the proposed topology. Table 3 provides the %THD at different modulation index points. Fig. 12 displays the Graphical representation of Modulation index vs %THD.

Table 3: Inverter %THD at different modulation index points

| Modulation Index | %THD  |
|------------------|-------|
| 0.4              | 8.56% |
| 0.8              | 2.15% |
| 1                | 0.56% |
| 1.1              | 0.25% |

Fig. 11: THD analysis for the proposed topology.
Table 3 Inverter %THD at different modulation index points

| Modulation Index | %THD  |
|------------------|-------|
| 1                | 26.86 |
| 0.9              | 33.50 |
| 0.8              | 38.38 |
| 0.5              | 51.66 |
| 0.4              | 76.40 |

Fig. 12 Graphical representation of Modulation index vs %THD

The proposed topology get 22.86% THD at modulation index 1. Here, presents the different single-phase topologies THD with proposed topology. As compared to existing topologies proposed topology get less %THD. Table 4 represents the THD analysis for existing topologies and proposed topology similarly table 5 represents the judgment of switches requirement with an increasing number of levels as compared to existing topologies.

Table 4 THD analysis for existing topologies and proposed topology

| Reference | %THD |
|-----------|------|
| [6]       | 33.16|
| [7]       | 36.89|
| [8]       | 39.41|
| Proposed  | 26.26|
Table 5: Comparison of switches required with an increasing number of levels

| Reference | Five-level | Seven-level | Nine-level |
|-----------|------------|-------------|------------|
|           | Switches   | Switches    | Switches   |
| [1]       | 8          | 10          | 12         |
| [2]       | 6          | 8           | 10         |
| [3]       | 6          | 8           | 10         |
| [4]       | 6          | 8           | 10         |
| **Proposed** | **5**     | **6**       | **7**      |

VI. Conclusion

In this, present a single-phase five-level inverter with minimum switches. The projected topology contains only five switches to produce five-level output. In this sinusoidal pulse with modulation control scheme is used to control the inverter. In projected topology has so many advantages as compared to existing single-phase topologies. It can produce less THD and minimum switching losses. In this, the requirement of filter somewhat less as compared to existing topologies because of it produce less THD as output side. By utilizing this inverter to produces 26.86% THD as competed to existing topologies it is less. Similarly, it is suitable for high power applications.

Reference

I. E. Babaei, S. Laali, and Z. Bayat, “A single-phase cascaded fivelevel inverter based on a new basic unit with reduced number of power switches,” IEEE Transactions on Industrial Electronics, vol. 62, no. 2, pp. 922–929, 2015.

II. E. Najafi, and A. H. M. Yatim, “Design and Implementation of a New Fivelevel Inverter Topology,” IEEE Trans. Ind. Electron., vol. 59, no. 11, pp. 4148-4154, Nov. 2012.

III. E.Sambath1, S.P. Natarajan, C.R.Balamurugan, “Performance Evaluation of Five Carrier Based PWM Techniques for Single Phase Five Level H-Bridge Type FCMLI”, IOSR Journal of Engineering (IOSRJEN) ISSN: 2250-3021 Volume 2, Issue 7(July 2012), PP 82-90.

IV. Kennedy A. Aganah, Benozir Ahmed, and Aleck W. Leedy, “Single-Phase Fivelevel Inverter Topology for Distributed DC Sources”, 978-1-5090-1496-5/16/$31.00 c 2016 IEEE.
V. Krishna Kumar Gupta and Shailendra Jain, “A Novel Fivelevel Inverter Based on Switched DC Sources”, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 61, NO. 7, pp. 3269-3278, JULY 2014.

VI. Krishna Kumar Gupta, AlekhRanjan, Pallavee Bhatnagar, Lalit Kumar SahuSailendraJain, “Fivelevel inverter topologies with reduceddevicecount: A review,” Power Electronics, IEEE Transaction on, vol. III, pp. 135-150, Jan. 2015.

VII. M. Venkatesan, et al., “Comparative Study of Three Phase Grid Connected Photovoltaic Inverter Using PI and Fuzzy Logic Controller with Switching Losses Calculation,” International Journal of Power Electronics Drives Systems, vol.7, pp. 543-550, 2016.

VIII. M. Venkatesan, etc al., “Transient and Steady State Analysis of Modified Three Phase Fivelevel Inverter for Photovoltaic System,” International Journal of Power Electronics and Drive System (IJPEDS) Vol. 8, No. 1, pp. 31–39, March 2017

IX. Maha G. Elsheikh, Mahrous E. Ahmed, Emad Abdelkarem, Mohamed Orabi, “Single-phase Five-level inverter with less number of power elements,” 33rd International Telecommunications Energy Conference, IEEE transaction on, pp. 1-8, Oct 2011.

X. R. Naderi and A. Rahmati, “Phase-shifted carrier pwm technique for general cascaded inverters,” IEEE Transactions on Power Electronics, vol. 23, no. 3, pp. 1257–1269, 2008.

XI. Sharma, Neelam. "Analysis of Lactate Dehydrogenase & ATPase activity in fish, Gambusia affinis at different period of exposure to chlorpyrifos." International Journal 4.1 (2014): 98-100.

XII. Sung-Jun Park, Feel-Soon Kang, Man Hyung Lee, Cheul-U Kim, “A new single-phase five-level PWM inverter employing a deadbeat control scheme,” power electronics, IEEE transaction, vol. 18, no. 3, pp. 831-843, May 2003.

XIII. V.G. Agelidis, D.M. Baker, W.B. Lawrance, C. V. Nayar, “A Fivelevel PWM Inverter Topology for Photovoltaic Application,” Industrial Electronics, IEEE transaction symposium on, vol. II, pp. 589-594. 1997.