A monolithic 56 Gb/s silicon photonic pulse-amplitude modulation transmitter

CHI XIONG*, DOUGLAS M. GILL, JONATHAN E. PROESEL, JASON S. ORCUTT, WILFRIED HAENSCH, WILLIAM M.J. GREEN

1 IBM T.J. Watson Research Center, 1101 Kitchawan Road, Yorktown Heights, New York 10598, USA
*Corresponding author: cxiong@us.ibm.com

1. INTRODUCTION

Traditional optical interconnects, implemented using parallel multimode fiber coupled to vertical cavity surface emitting laser arrays, face modal dispersion-induced limitations in satisfying longer reach (>100 m) requirements within massively parallel data center and high-performance computing systems [1, 2]. On the other hand, silicon photonics links offer a scalable solution using wavelength division multiplexing, which can be implemented using compact single-mode silicon photonic modulators [3, 4] and on-chip Ge photodetectors [5]. As data centers require ever higher data rates, continued multiplexing of wavelengths can be limited by the cost and power consumption of the additional lasers. It is also increasingly challenging to increase the serial line rate of a non-return-to-zero (NRZ) link because the physical limitation of the electro-optic bandwidth of modulators and photodiodes. An alternative solution is to use multi-level signaling formats such as pulse-amplitude modulation (PAM-\(m\)), where multiple digital bits per symbol are encoded into \(m\) different signal amplitude levels. In PAM-4 modulation, two binary bits are encoded into four signal levels, which therefore doubles the data rate at the same symbol rate compared to conventional NRZ links.

The PAM-4 modulation format is receiving significant attention because of its relative ease of implementation compared to higher-order modulation. PAM-4 modulation has been explored with traditional electrical links [6-8] and directly modulated vertical cavity surface emitting lasers [9, 10]. In the case of directly modulated lasers, the PAM-4 signal applied to the laser is generated by summing two NRZ signals followed by amplification with a linear driver. A similar scheme using an electrically generated PAM-4 signal to drive the silicon photonic modulator has been demonstrated [11]. Recently it has been demonstrated that a PAM-4 optical waveform can be created by using a silicon photonic modulator with two electrode segments [12] and thus...
equivalently performing the digital-to-analog conversion (DAC) in the optical domain. Using the photonic DAC eliminates the power consumption associated with the electrical DAC circuits. On the receiver side, the PAM-4 signals can be decoded into two separate NRZ streams using an analog-to-digital converter (ADC). Using this approach, a recent demonstration has shown a bit-error rate of $10^{-12}$ at 25.6 Gbaud using a commercial chip with embedded $2^{31} - 1$ bit pseudo-random bit sequence (PRBS) generators and error checkers [13]. The driver circuits for these demonstrations, however, are implemented using discrete components or hybrid chips, and the parasitics from the packaging can severely degrade the RF signal quality and limit further scaling of data rate.

Here, we demonstrate a two-segment traveling-wave Mach-Zehnder modulator (MZM) silicon photonic PAM-4 transmitter having monolithically integrated current-mode CMOS driver circuits. Monolithic integration of the optical modulator side-by-side with CMOS driver circuits minimizes interconnect and packaging parasitics between the electronics and the photonic device, and allows for minimal performance degradation. In addition, monolithic integration facilitates precision electrical connections and helps, for example, to systematically design for and minimize synchronization issues between the differential drive signals into the two arms of the MZM. Furthermore, monolithic integration facilitates wafer level electro-optic testing, as well as minimizes packaging steps, which can reduce the overall cost. The reported PAM-4 modulator is optimized for high speed performance up to 28 Gbaud (56 Gb/s). We directly measure the bit-error rate of the PAM-4 signal using a standard commercial bit-error tester without post-processing and demonstrate error-free (BER < $10^{-12}$) PAM-4 transmission at 25 Gbaud with $2^7 - 1$ bit PRBS without forward-error correction.

2. DEVICE DESIGN AND CHARACTERIZATION

A. Design of the monolithic transmitter

The PAM-4 transmitter is designed and fabricated using IBM’s sub-100nm CMOS integrated nanophotonics technology, CMOS9WG [14]. This platform is targeted toward multi-channel short reach O-band (1310 nm) optical interconnects operating at up to 25 Gb/s symbol rates, with the optical components monolithically integrated into the front end CMOS electronics process with a manufacturable low-loss packaging technology [15, 16]. A micrograph of the monolithic PAM-4 transmitter is shown in Fig. 1. The same CMOS driver has recently enabled an error-free demonstration of a silicon photonic traveling-wave MZM transmitter up to 32 Gb/s [17]. The MZM’s phase shifter segments have balanced lengths and hence are insensitive to global temperature fluctuations. Each arm of the MZM is divided into two segments, with lengths of 1 mm and 2 mm respectively. Both segments are designed to operate in the traveling-wave mode, and make use of PN junction free carrier depletion-mode electro-optic phase shifters. The Most Significant Bit (MSB) data drives the 2 mm segment and the Least Significant Bit (LSB) drives the 1 mm segment, enabling electro-optic digital-to-analog conversion. Each traveling-wave electrode is terminated by a network of resistors which can be trimmed by focused-ion beam post-fabrication. In this prototype PAM-4 transmitter, this editable termination network provides flexibility to incrementally alter the termination impedance for better matching to the characteristic impedance of the transmission line, which is crucial for optimizing the PAM-4 waveform (see supplementary material). A fixed-value non-trimmed termination resistance can be realized by simply modifying the final metal mask, which is straightforward to implement once all transmission line parameters are finalized in a production-ready design.

The drivers for MSB and LSB data streams are identical and consist of a three-stage preamplifier followed by a nominal open drain driver. The circuit power supply voltage (VDD) is 1.2 V and the modulator termination resistors $R_{TERM}$ are terminated at 1.5 V termination power supply (AVTT). The top level circuit diagram is shown in Fig. 2(a). The three preamplifier stages are inductively-peaked current mode logic (CML) differential amplifiers and scale up $2 \times$ per stage to drive the open drain driver. With a 30 Ω termination impedance, single-ended output drive swing $V_{oc}$ of the CMOS driver is 1.08 $V_{pp}$ (2.16 $V_{pp}$ differentially). Fig. 2(b) shows transistor level circuit schematics of the three-stage predriver and the open drain driver for one MSM segment. As shown in the dashed box, the current bias circuit creates a bias current proportional to $1/R$, so that the voltage drop across all resistors is independent of process variations in sheet resistance. This allows us to maintain a constant voltage swing for CML stages. The current is set by VREF, which establishes the voltage drop across the reference resistor R. The nominal open drain driver’s output amplitude is designed to be adjustable using a three-bit digital control (TX_reg) to enable a PAM-4 waveform with equal spacing between each symbolic level. In addition, the reference voltage (VREF) can be used to finely adjust the output swing. Operating at 25 Gbaud, VREF of 0.5 V and maximum TX_reg setting of 7, the VDD supply draws 66 mA current and AVTT draws 36 mA, which amounts to a power consumption of 135 mW. Accordingly, the power consumption is 5.4 pJ/bit at 50 Gb/s and 4.8 pJ/bit at 56 Gb/s.

The traveling-wave MZM is designed for single mode operation at 1310 nm wavelength, and employs PN junction phase shifters embedded within a 145 nm thick silicon-on-insulator (SOI) waveguide layer. The buried oxide beneath the silicon waveguides is 2 μm thick. The phase shifter is based on an optically tunable input couplers and MZM phase control. Yellow squares are drawn around the CMOS drivers.

Fig. 1. Optical micrograph of the monolithically-integrated PAM-4 transmitter. Two directional couplers with thermooptically tunable phase shifters serve as input and output couplers for the Mach-Zehnder modulator. The layout of the silicon photonic waveguides is overlaid on top of the micrograph. The magnified waveguide sections in the inset show the thermally-tunable input couplers and MZM phase control.
Wafer-level testing results separately show that the propagation power consumption of the input and output thermo-optic phase shifters is 11.6 mW. This power consumption is not intrinsic to the device operation since in the newer generation of devices, additional thermo-optic phase shifters are embedded within these Zehnder interferometers. Thermo-optic phase shifters, which can be used to offset fabrication drift, are equipped with input/output RF probe pads. We measure the characteristic impedance of the loaded transmission line to be approximately 30 \( \Omega \) across the RF frequency range of interest.

The MZM has nominal 3 dB directional couplers at both the input and output, each designed using smaller tunable Mach-Zehnder interferometers. Thermo-optic phase shifters, which can be used to offset fabrication drift, are embedded within these directional couplers. In this experiment, the input thermo-optic phase shifter draws 6.5 mA at 1.72 V bias and the output thermo-optic phase shifter draws 1.5 mA at 0.31 V. Accordingly the total RF loss associated with the longer loaded transmission line. Following the rule of thumb that the transmission’s bandwidth needs to be at least 0.75 times the baud rate [20], the 21 GHz bandwidth is sufficient to support 28 Gbaud PAM-4 operation. The termination resistors have been trimmed to be 30 \( \Omega \) to match the characteristic impedance of the loaded transmission line to be approximately 30 \( \Omega \) across the RF frequency range of interest.

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Experimentally, to generate PAM-4 optical waveforms, the MSB and LSB data are drawn from the outputs of two non-return-to-zero (NRZ) PRBS pattern generators (Anritsu MP1800A and Centellax SSB16000J) which are triggered by the same external clock. A 1310 nm distributed feedback diode laser with 14 dBm optical output power is coupled onto the chip via a lensed fiber and an on-chip spot-size converter. The typical fiber-to-chip coupling loss per facet is 2.5 dB. An off-chip polarization controller is used to change the polarization of the launched light to transverse electric (TE). Two multi-contact RF probes are used to provide high-speed signals and power to the CMOS circuits. The bit sequences for MSB and LSB data are skewed with respect to each other to reach all possible transitions. High-speed optical signal-to-noise ratio and power measurements are made using an electrical spectrum analyzer.
While PAM-4 transmission doubles the data rate, it requires more power compared to a NRZ waveform at the same symbol rate to yield the same BER. In other words, the theoretical power penalty of a PAM-4 waveform compared to a NRZ waveform at the same symbol rate is $10\log_{10}3 = 4.8$ dB.

To quantify the performance of our PAM-4 transmitter against this theoretical prediction, BER measurements are performed on the PAM-4 transmitter and a reference single-segment Mach-Zehnder NRZ monolithic silicon photonic transmitter with 2.8 mm long phase shifters per arm [17]. We first compare the OMA needed to achieve error-free signaling of the PAM-4 and NRZ transmitters at a relatively lower data rate of 12.5 Gb/s. The BER of both transmitters are measured using a 40 Gb/s optical receiver (Discovery Semiconductor R411) and a bit error rate tester (Anritsu MP1800A). The optical power into the receiver is kept low to ensure linear operation and thus an accurate characterization of the multi-level PAM-4 eye diagrams. The measurement of the NRZ BER is straightforward. To measure the PAM-4 BER, however, we treat the three eye openings of the PAM-4 waveforms as three separate NRZ waveforms, and check the BER of the upper (BER$\text{upper}$), middle (BER$\text{mid}$) and lower eye (BER$\text{low}$) against programmed bit patterns: MSB $\lor$ LSB (Boolean OR AND between MSB and LSB), MSB $\lor$ LSB (Boolean OR between MSB and LSB) respectively. The aggregate BER of the PAM-4 waveform is then calculated as BER = $1/2 \cdot$ BER$\text{upper}$ + BER$\text{mid}$ + 1/2$ \cdot$ BER$\text{low}$. The BER of the upper and lower eye need to be divided by two because the two bits need to be equally distributed between the upper and lower eye for error checking assuming ‘1’ and ‘0’ bits occur with equal probability in the MSB and LSB streams [9]. Because the length of the programmable bit pattern is limited by the memory size of the error detector used, we focus on $2^7 - 1$ PRBS patterns in our experiments. The input MSB and LSB bit streams are phase skewed by half of a word length to ensure full decorrelation.

As shown in Fig.5(a), the OMA needed to achieve error-free operation (BER$<10^{-12}$) for the 12.5 Gb/s NRZ waveform and PAM4 waveform is -15.3 dBm and -9.8 dBm respectively. In other words, the PAM-4 transmitter shows a 5.5 dB power penalty compared to a NRZ waveform at the same symbol rate to yield the same BER. In other words, the theoretical power penalty of a PAM-4 waveform compared to a NRZ waveform at the same symbol rate is $10\log_{10}3 = 4.8$ dB.

C. Bit-error rate characterization

While PAM-4 transmission doubles the data rate, it requires more optical power to achieve the same eye openings (or signal to noise ratio) when compared with the NRZ transmission format. A figure of merit to quantify the transmitter performance is the optical modulation amplitude (OMA) needed to obtain error-free operation, which is usually defined as a bit-error rate (BER) less than $10^{-12}$. For the NRZ waveform the OMA is defined as the difference between the average power level $<1>$ and $<0>$. For PAM-4 waveform, we focus on the outer OMA (OMA$\text{outer}$), which is defined as the difference between the average power level $<11>$ and $<00>$. The three inner OMA values are given by the difference of high and low power for each eye: OMA$11$ = $P_{11} - P_{01}$, OMA$12$ = $P_{12} - P_{02}$, OMA$23$ = $P_{13} - P_{10}$. The inner OMA, which has the greatest effect on the BER, is defined as the minimum of OMA$11$, OMA$12$, and OMA$23$, i.e., OMA$\text{inner} = \min(\text{OMA}11, \text{OMA}12, \text{OMA}23)$. If the three eye openings have perfect equal distribution, OMA$\text{inner} = 1/3 \cdot$ OMA$\text{outer}$, i.e. the OMA$\text{outer}$ of the PAM-4 waveform will need to be three times the OMA$\text{outer}$ of a NRZ waveform at the same symbol rate to yield the same BER. In other words, the theoretical power penalty of a PAM-4 waveform compared to a NRZ waveform at the same symbol rate is $10\log_{10}3 = 4.8$ dB.

Fig. 4. Experimental PAM-4 waveforms at (a) 25 Gbaud (50 Gb/s) and (b) 28 Gbaud (56 Gb/s) measured with $2^{31} - 1$ bit PRBS. The extinction ratios between average power level $<11>$ and $<00>$ are measured to be approximately 6.0 dB for both data rates.

Eye diagrams at data rates of 25 and 28 Gbaud, shown in Fig. 4, are measured using a 30 GHz bandwidth digital sampling oscilloscope (Agilent DCA-86100D), with both MSB and LSB being driven with $2^{31} - 1$ PRBS patterns. Here the extinction ratio (ER) for the PAM-4 waveform is defined as the ratio of the average power level of data $<11>$ to the average power level $<00>$, $\text{ER} = 10\log_{10}(<11>/<00>)$. The ERs are approximately 6.0 dB at both symbol rates. The eyes show clear openings between all amplitude levels. The measured optical insertion loss of the PAM-4 modulator is 5.0 dB with the CMOS-supplied -0.8 V reverse bias applied to the PN junction phase shifters under PAM-4 operation.

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As shown in Fig.5(a), the OMA needed to achieve error-free operation (BER$<10^{-12}$) for the 12.5 Gb/s NRZ waveform and PAM4 waveform is -15.3 dBm and -9.8 dBm respectively. In other words, the PAM-4 transmitter shows a 5.5 dB power penalty compared to the NRZ transmitter running at the same symbol rate to achieve equivalent BER. This penalty is thus 0.7 dB greater than the theoretically predicted 4.8 dB power penalty. Part of the excess penalty likely originates from unequal eye openings, because the BER is determined by the smallest eye openings of the three eyes (OMA$\text{upper}$). Although the amplitude control of the driver circuit can precisely control the eye spacing, the adjustment is currently done manually which is subject to inaccuracy and drift. In Fig. 5(a), the eye with the smallest opening is the upper one, which is measured to have an OMA of 93 percent of 1/3 $\cdot$ OMA$\text{outer}$. As a result, a linearity penalty of 0.3 dB can be estimated. An output waveform tap and linearity feedback circuit can be implemented in the future to minimize the linearity penalty. The residual 0.4 dB excess penalty can be attributed to PAM-4 implementation penalties as it has been shown that multi-level formats are more susceptible to implementation imperfections including inter-symbol interference due to impedance mismatching, phase skew between MSB and LSB data streams, timing jitter, and so forth [9, 21].

Longer PRBS patterns have more low frequency spectral content and thus are interesting for characterizing the wide band response of the PAM-4 transmitter. As a result, we measure the
The BER of the PAM-4 transmitter using a $2^{23} - 1$ bit long PRBS pattern, which is the maximum programmable pattern length that can be stored within the 8 Mbit memory of the error detector. A modest additional power penalty of 0.3 dB is measured using $2^{23} - 1$ PRBS compared with $2^7 - 1$ PRBS.

The BER for the PAM-4 and NRZ transmitters, both running at 25 Gbaud, is measured using a similar high-speed electro-optic setup. However, achieving error-free operation at 25 Gbaud requires much higher optical power than needed at 12.5 Gbaud. To minimize the nonlinearity at the photoreceiver due to high input optical power, we keep the input optical power at the photoreceiver low while adding a low-noise 40 Gb/s RF amplifier (Picosecond labs 5882) after the photoreceiver to boost the RF signal into the error detector. This effectively improves the input sensitivity of the error detector while minimizing the receiver nonlinearity. As shown in Fig. 5(b), the PAM-4 transmitter operates error free (BER$<10^{-12}$) with an OMA greater than -5.8 dBm, with a $2^7 - 1$ PRBS pattern. This is the first demonstration of error-free operation of a silicon photonic PAM-4 transmitter at a data rate of 25 Gbaud. We also characterize the reference monolithic silicon photonic NRZ transmitter at 25 Gbaud, and obtain an error-free OMA sensitivity of -11.8 dBm. In other words, the PAM-4 transmitter exhibits a 6.0 dB power penalty relative to the NRZ transmitter at an equivalent BER, with both operating at 25 Gbaud. The excess power penalty compared to theory is 1.2 dB, of which 0.4 dB can be attributed to linearity penalty estimated from the smallest PAM-4 eye opening (middle eye) in Fig. 5(b). The remaining 0.8 dB penalty, which is 0.4 dB higher than that at 12.5 Gbaud, could be due to the increased impact of implementation imperfections such as impedance mismatching at 25 Gbaud.

3. CONCLUSION

In conclusion, we have demonstrated a monolithic silicon photonic PAM-4 transmitter in IBM CMOS9WG technology, operating up to 56 Gb/s (28 Gbaud). We directly measure the bit-error rate of the PAM-4 transmitter and compare the relative power penalty with a reference silicon photonic NRZ transmitter. The optimized traveling-wave modulators and monolithic integration of the CMOS drivers enable error-free operation (BER$<10^{-12}$) without forward-error correction at 50 Gb/s with an extinction ratio of 6.0 dB.

For PAM-4 waveform, the optimization of phase alignment between MSB and LSB is important to maximize the horizontal eye opening. In the current experiment, the phase alignment is adjusted using the phase setting in the pattern generators. In future implementation, we can take advantage of the fully monolithic platform to enable a complete on-chip signal distribution network including both the modulator driver and tunable RF delay line on chip [22]. To optimize the vertical eye opening, the monolithic CMOS drivers providing tunable output levels could be used with on-chip germanium power taps and integrated feedback circuitry to actively compensate for drift of the PAM-4 waveform linearity. In addition, the performance of the PAM-4 modulator can be further improved using phase shifter designs with maximized capacitance per unit volume. For example, interleaved junctions with highly scaled pitch have demonstrated smaller $V_T$ and smaller insertion loss [23, 24]. On a system level, PAM format can be combined with other available techniques for scaling aggregate bandwidth on the silicon photonics platform, including the use of parallel single mode fibers and wavelength division multiplexing, to enable ultrahigh data rate optical interconnects.

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See Supplement 1 for supporting content.

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