Towards Scalable, Energy-Efficient and Ultra-Fast Optical SRAM

Ramesh Kudalippallyalil,1, a) Sujith Chandran,1, a) Ajey P. Jacob,1, b) and Akhilesh Jaiswal1−b)
1Information Sciences Institute (ISI), University of Southern California (USC), Marina Del Rey, CA 90292

(Dated: 30 November 2021)

Optical static random access memory (O-SRAM) is one of the key components required for achieving the goal of ultra-fast, general-purpose optical computing. We propose and design a novel O-SRAM using fabrication-friendly photonics device components such as cross-coupled micro-ring resonators and photodiodes. Based on the chosen photonic components, the memory operates at a speed of 20 Gb/s and requires ultra-low static (switching) energy of ∼16.7 aJ/bit (∼1.04 pJ/bit) to store a single bit. The footprint of the bit cell is ∼2400 µm². The proposed O-SRAM can be configured in a 2D memory array by replicating the bit-cells along rows and columns for creating ultra-large scale on-chip optical memory sub-system. Such manufacturing-friendly, large-scale optical-SRAM could form the underlying memory backbone for photonics integrated circuits with wide applications in novel computing and networking.

The remarkable scalability of the electronic transistor has driven decades of improvements in power, performance and footprint metrics of digital computing systems1. However, the state-of-the-art electronic platforms fail to provide the required computing speed, throughput, and energy-efficiency, demanded by emerging class of data intensive applications such as artificial intelligence, machine learning2,3, extreme-scale simulations4, etc. As a result, use of optical state variable for memory, computing and interconnects4,5, has emerged as a promising alternative to the electronic charge-based computing platforms that are limited by slow and energy-expensive data access and lower electrical bus bandwidth6. There have been several demonstrations of large bandwidth memory-processor optical links7−10 reported in the past few years. However, high-speed, energy-efficient and compact photonic storage with true static random-access characteristics is still demanding to form the ultimate underlying memory sub-system for general-purpose optical computing. Various methods have been investigated for all-optical static random access memory (SRAM) cells, including semiconductor optical amplifier-Mach-Zehnder interferometer (SOA-MZI) configurations11−14, SOA-based ring lasers15, III-V photonic crystal cavities16 and optomechanical cavities17. SOA-MZI based optical SRAM bit cell reported in14 exhibit a speed of 10 Gbps, however, these devices are not compatible for large scale chip-level memory integration as it requires a large footprint in the order of mm². On the other hand, photonic crystal cavities16 and nano-optomechanical cavities18 can be integrated in a smaller optical footprint (∼100 µm²), but require major modifications to the existing foundry processes involving material or device integration aspects.

In this letter, we present a novel optical memory element based on cross-coupled optical devices - photodiodes (PDs) and microring resonator (MRR) modulators switches. Furthermore, the data can be selectively written or read to/from the optical memory element through another set of PDs and MRRs enabling random access functionality. This, in turn, leads to the construction of optical SRAM with striking functional similarities to electrical SRAMs, including complementary data storage and differential read-out of data18. Furthermore, the proposed optical-SRAM (O-SRAM) can be arranged in an array-like fashion for creating large-scale on-chip optical storage. Advantageously, the use of well-known optical devices makes our proposal amenable to large-scale manufacturing in the existing silicon photonics foundry process.

Fig. 1(a) shows the schematic layout of our proposed O-SRAM cell, where R1-R6 are MRR based active optical switches, D1-D4 are photodiodes (PDs) coupled to integrated optical waveguides, PS1-PS2 are optical power splitters, and A1-A8 are passive optical absorbers to reduce reflections from unwanted output ports. A block diagram representation of the O-SRAM is shown in Fig. 1(b) along with its truth table. The circuit is optically biased by an internal laser source (wavelength λbias) and electrically biased by a DC voltage source (Vbias). The MRR switches R1 and R2, and feedback photodiodes D1 and D2 form the internal optical latch. The optical outputs Q* and Q represents the present state of the memory. While, the other MRRs (R3-R6) and PDs (D3 and D4) constitute the read/write access circuit. The MRR switches are designed on a high speed p-n (carrier depletion) phase shifters. A detailed working of the circuit is discussed below. The O-SRAM bit-cells can be arranged in a 2D array fashion, as shown in Fig. 1(c), by replicating the bit-cells in rows and columns for creating large-scale optical memory sub-system. The rows share ‘wordline’ waveguides, while columns share BIT and BITE* waveguides.

As shown in Fig. 1(a), the internal bias laser (λbias) is coupled to a 50:50 power splitter (PS1) that feeds two identical MRR switches, R1 and R2, which in turn are controlled by the corresponding feedback photodiodes D1 and D2, respectively. The through-port of R1 (R2) drives D2 (D1). The drop ports of R1 and R2 represent the output states Q* and Q respectively. The ON state of D1 implies that R1 is resonant to the input light at λbias and transfers maximum optical power to its drop-port, resulting in a logic HIGH at Q*. This also implies that the light output at the through-port of R1 is insufficient to turn ON D2, causing R2 to be not in resonance with the incoming light. As a result, R2 delivers power to

---

a)Contributed equally to this work
b)Authors to whom correspondence should be addressed: ajey@isi.edu and ajkaiswal@isi.edu (Contributed equally to this work).
D1 and keeps the circuit in a stable state (Q* = HIGH and Q = LOW) by keeping R1 ON. This state continues as long as the electrical and optical bias signals are applied to the memory element allowing a static storage of optical data. Thus, the cross-coupled MRR-PD system (R1, D2 & R2, D1) forms an optical latch or optical storage unit constituting an optical SRAM bit cell. The read/write part of the O-SRAM cell (R3 and R5 controlled by D3 & R4 and R6 controlled by D4) remain OFF during the hold state unless the O-SRAM cell is accessed (or selected) for read/write operation by passing light through the ‘wordline’ waveguide. Note, the O-SRAM would be initialized by a write operation (described below) to ensure either Q = HIGH, Q* = LOW (digital 1) or Q = LOW, Q* = HIGH (digital 0). Thus, the condition that Q and Q* can simultaneously be HIGH or LOW is obviated (similar to electrical-SRAMs that have a metastable state but are never encountered in normal memory operations).

In order to read the state of the memory, a read/write laser is first enabled in the ‘wordline’ waveguide. This first drives D3 and D4 to the ON state; subsequently R3 and R4 are driven in resonant to λbit. Thus, the Q (input of R4) and Q* (input of R3) will transfer to the drop ports of R3 and R4, respectively. This differential (complementary) optical outputs are then transferred to BIT and BIT* waveguides (R5 and R6 are designed to be non-resonant to λbit irrespective of the switching voltage), which can then be fed to the peripheral sensing circuits for reading the stored data in the O-SRAM bit-cell.

To understand the memory write operation, assume the memory is initially in Q = LOW and Q* = HIGH state. This means that D2 is in OFF state and R2 is off-resonant to λbit, while D1 is in ON state and R1 is in resonant to λbit. In order to flip the memory output state, D2 needs to be triggered with an external optical signal. The write operation is initiated by activating D3-D4 photodiodes by enabling the READ/WRITE laser in the ‘wordline’. An external optical write pulse (at λwrite) is then applied at the BIT waveguide, reaching D2 through R6 (resonant to λwrite). This process turns ON D2 and subsequently drives R2 in resonance to λbit. The resonant R2, turns away the light feeding D1 from its through-port to the drop port. In other words, D1 turns OFF and makes R1 non-resonant to λwrite. This keeps D2 in ON state, leading to Q = HIGH and Q* = LOW, i.e., the state of the memory has switched as dictated by the write operation.

From the above discussion, it is clear that the write operation involves more numbers of MRRs and PDs compared to the read operation (twrite > tread), and thus the overall speed (or bandwidth) of the memory is specified in terms write speed. The operating speed of our proposed O-SRAM is limited by the bandwidths of MRRs (BW_MRR) and PDs (BW_PD) used in the circuit. In general, the MRR bandwidth is expressed using the empirical formula 1/BW_MRR = 1/BW_Q + 1/BW_RC where BW_Q = (2πτ_Q)−1 is a function of cavity photon life time τ_Q and BW_RC = (2πRC)−1 is a function of RC (= τ_RC) time constant of the phase shifter. At any operating λ and a given quality factor Q, τ_Q can be expressed as τ_Q = λQ/(2πc) where, c is the light speed in vacuum. The Q-factor is a critical design parameter of an MRR switch. The optical bandwidth BW_Q reduces as Q increases. On the other hand, the photon interaction with the injected/depleted carriers reduces as Q (τ_Q) reduces, and thus large bias voltage is required to switch the MRR between non-resonance to resonance. Thus, a moderate Q factor ~ 5000 – 7000 is preferred for our design, providing...
a BW ~ 30 GHz to 50 GHz at operating λ ~ 1270 nm. The phase shifter delay, τ_{RC}, is relatively smaller for carrier depletion (p-n) type phase-shifter compared to carrier injection (p-i-n) type phase-shifter\(^{20}\). This is because p-i-n devices take additional time delay to sweep out the injected carriers from the intrinsic (i-) region after removing the bias voltage across the junction.

We adapted the ring with SOI waveguide of 300 nm × 400 nm, ring radius = 10 µm. The waveguide loss, effective index versus bias voltage) and phase-shifter (p-n type) design parameters were adapted as reported in\(^{21}\) and designed our add-drop MRR switches near λ = 1270 nm. A schematic of the add-drop MRR switch driven by a PD is shown in Fig. 2(a). A detailed working principle of MRR switches/modulators can be found elsewhere\(^{20,22–24}\). We carefully designed the coupling coefficients (k₁₂) between the ring and bus waveguides for a desired optical switching response at operating wavelength λ, with the following assumptions: (1) the drop port extinction ratio, ER\(_{\text{dr}}\) = \(|P_{\text{dr}}^{\text{ON}} - P_{\text{dr}}^{\text{OFF}}|\) ≥ 3 dB (where \(P_{\text{dr}}^{\text{ON/OFF}}\) are the drop-port power for the ON and OFF states of MRR) for differential sensitivity between the BIT and BIT* outputs, (2) through-port extinction ratio, \(ER_{\text{th}} = |P_{\text{th}}^{\text{OFF}} - P_{\text{th}}^{\text{ON}}|\) ≥ 20 dB (where \(P_{\text{th}}^{\text{ON/OFF}}\) are the through-port power for the ON and OFF states of MRR) for better stability (either R1 or R2 is in ON state at any time during the memory operation), and (3) \(P_{\text{th}}^{\text{ON}}\) negligibly small to keep the corresponding PD in dark current mode (OFF state). Fig. 2(b) shows the transmission characteristics at the through-port (P\(_{\text{th}}\)) and drop-port (P\(_{\text{dr}}\)) of the MRR switch (R1-R4) for OFF (V\(_{\text{ps}}\) = 0 V) and ON (V\(_{\text{ps}}\) = -4 V) states of the phase shifter (V\(_{\text{ps}}\) is the reverse bias voltage across the p-n phase shifter). The resonance wavelength (λ\(_{\text{OFF}}\)) is shifted by ∆λ = 117 pm to λ\(_{\text{ON}}\) ~ 1270.06 nm, with \(ER_{\text{th}} = 23\) dB and \(ER_{\text{dr}} = 4.4\) dB. The Q factor (= \(\lambda_{\text{r}}/\Delta\lambda_{3\text{dB}}\), where \(\Delta\lambda_{3\text{dB}}\) is 3-dB band width) of the spectrum is ≈ 6500, which results in τ\(_{\text{th}}\) = 5 ps and BW\(_{\text{Q}}\) = 36 GHz. We choose the operating wavelength (λ\(_{\text{bit}}\) = 1270.08 nm) slightly above λ\(_{\text{r}}\) in order to have smooth transition at the output ports and also to satisfy the above conditions. The switching characteristics at λ\(_{\text{bit}}\) is shown in Fig. 2(c). The Q-limited rise time at the drop port and fall time at the through port are calculated to be τ\(_{\text{dr}}\) = 29.5 ps and τ\(_{\text{th}}\) = 14 ps, respectively. In this case, the RC limited electrical band width of the phase shifter (BW\(_{\text{RC}}\) ~ 150 GHz\(^{21}\)) is much higher than that of resonator (BW\(_{\text{Q}}\)). As discussed earlier, R1-R4 are identical MRRs of radii 10 µm operating at λ\(_{\text{bit}}\). Similarly, R5 and R6 are identical MRRs of radii 11.2 µm, designed to operate at resonant wavelength λ\(_{\text{write}}\) ~ 1269.7 nm.

Besides the bandwidth, it is also important to consider reverse saturation current I\(_{\text{r}}\) of the p-n phase shifter. For the given parameters in\(^{21}\), I\(_{\text{r}}\) is calculated to be ~ 4 – 10 nA. Since the MRR and PD are connected in series, one must choose a PD with the dark current I\(_{\text{dark}}\) << I\(_{\text{r}}\) in order to avoid the inadvertent switching of the MRR due to dark current while the corresponding PD is OFF. For D1-D4, we choose the Ge based photodiode\(^{25}\) with a low dark current of ~ 30 pA (< I\(_{\text{r}}\) for R1). Its responsivity R = 0.043 A/W and operating speed of ~ 14.5 GHz at λ ~ 1.27 µm.

We have simulated and verified the memory operations in *Lumerical Intrerconnect*. The simulated memory write operation at different data rates (5 Gbps, 18 Gbps and 20 Gbps) are shown in Fig. 3 (a)-(c) and corresponding eye-diagrams (calculated at Q output) in (d)-(f). The input non-return to zero (NRZ) write signal and the corresponding memory states (Q and Q* outputs) are shown for comparison. Note that, the outputs reach stable states within the pulse period when operating at low data rates, for example, at 5 Gbps as shown in Fig. 3 (a). The corresponding rise-time (10%-90%) and fall-time (90%-10%) are calculated as t\(_{\text{r}}\) ~ 46 ps and t\(_{\text{f}}\) ~ 43 ps, respectively. This means that, the maximum operating speed of the O-SRAM cell is expected to be 1/t\(_{\text{r}}\) ~ 22 Gbps. However, given the frequency response of the PD, at higher data rate the outputs of the photodiodes do not reach its maximum value and hence MRRs, that are driven by PDs, operate at slightly lower bias voltage, which in turn changes the operating conditions (i.e, ∆λ, ER\(_{\text{dr}}\), ER\(_{\text{th}}\), etc.). Thus, the actual operating speed of the memory is slightly lower than the calculated value of 1/t\(_{\text{r}}\) ~ 22 Gbps. Through simulations, we noticed that the output states (Q and Q*) are distinguishable with clear eye opening when the memory operates ≤ 20 Gbps (NRZ). This has been shown in Fig. 3(b) & (e) for 18 Gbps and (c) &
The reported switching speed and energy are based on simulation parameters from published literature for photodiodes and MRR modulators that have been optimized for telecommunication applications. The preliminary speed, required bias voltage and other metrics are, therefore limited by the reported device metrics. Significant improvements can be achieved by device optimization of MRRs and PDs designed specifically for memory storage.

Table I shows the comparison of performances of various optical SRAMs reported in the literature. The static energy consumption of our device is estimated as $V_{DD} \times (I_e + 3I_{dark}) \times t_{bit} \approx 2.5$ aJ/bit, where we assume only one of the PD is ON, and the remaining are OFF at any time during the static operation. Similarly, the static optical energy is calculated as the fraction of internal laser power ($P_{laser}$) to the memory speed. With the given PD parameters, we calculated the minimum optical input power to the PD (say D1) as $\approx 100$ nW which ensures the MRR (say R1) is in ON state. This corresponds to total internal laser power, $P_{laser} = 334$ nW, considering the power associated with 3-dB power splitter PS1 (refer Fig. 1) and the transfer function of MRR (R1 or R2) from Fig 2(b). Thus, the static optical energy consumption is $\sim 16.7$ aJ/bit. Since all six MRRs are involved in the write operations, the dynamic electrical energy consumption is $6 \times CV_{bias}^2/4 = 1.04$ pJ/bit, where $C = 45$ fF. Similarly, the dynamic optical energy is the sum of all three lasers involved in the operation, i.e., internal laser source, write/read enable laser, and write laser. This is calculated as $\sim 40$ aJ/bit. Note, the estimated power budget does not include energy needed for thermal detuning of the MRRs. In general, the MRR operating wavelength is detuned using thermal phase-shifters to compensate for any wavelength shift due to process variations. Such thermal detuning could be implemented on global (for all MRRs in a memory array) or local (for individual MRRs) level based on the scale and nature of process variations associated with specific manufacturing technology.

In conclusion, we have designed and simulated an O-SRAM cell using cross-coupled MRRs and PDs. The performance of the proposed memory is simulated based on published literature for MRR modulators and PDs. The operating speed and static (switching) energy consumption are estimated as 20 Gb/s and $\sim 16.7$ aJ/bit (1.04 pJ/bit, respectively). The overall footprint of the device is $\sim 2400 \mu m^2$. Finally, we would like to highlight some key prospects of our O-SRAM; 1) the proposed optical memory is amenable to large-scale manufacturing in existing silicon photonics foundry process without need of explicit material/process modifications, 2) since optical signals can travel long distances with minimal loss, the O-SRAM bit-cell can be replicated along rows and columns to create very-large scale, ultra-high speed memory arrays, 3) the functional similarity of proposed O-SRAM with electrical SRAM opens up new pathways to implement emerging paradigms of in-memory and near-memory computing, similar to their electrical counterparts, within large-scale optical memory arrays. Thus, the proposed O-SRAM bit-cell can be used to create ultra-fast, ultra-large scale on-chip memory system - a key component required for achieving the holy grail of general purpose optical computing.

ACKNOWLEDGMENTS

The authors would like to thank Dr. Michal Rakowski from GlobalFoundries for fruitful technical discussions. This work was supported in part by Mousetrap fund at University of Southern California.

AUTHOR DECLARATIONS

Conflict of Interest

The authors report no conflicts of interest.

DATA AVAILABILITY

The data that supports the findings of this study are available within the article.
A. A. Sawchuk and T. C. Strand, “Digital optical computing,” Proceedings of the IEEE 72, 758–779 (1984).

P. Ambs, “Optical computing: A 60-year adventure.” Advances in Optical Technologies (2010).

A. A. Sawchuk and T. C. Strand, “Digital optical computing,” Proceedings of the 1st conference on Computing frontiers (2010).

P. Maniotis, D. Fitsios, G. Kanellos, and N. Pleros, “Optical buffering for scalable shared-memory multiprocessors,” IEEE micro 25, 41–49 (2005).

D. Brunina, D. Liu, and K. Bergman, “An energy-efficient optically connected memory module for hybrid packet-and circuit-switched optical networks,” IEEE Journal of Selected Topics in Quantum Electronics 19, 3700407–3700407 (2012).

Y. Yin, R. Proietti, X. Ye, S. B. Yoo, and V. Akella, “Experimental demonstration of optical processor-memory interconnection,” in Proc. AIAI2010, 213–216, Beijing, China, Oct. 2010 (IET, 2010).

Y. Liu, R. McDougall, M. Hill, G. Maxwell, S. Zhang, R. Harmon, F. Huijskens, L. Rivers, H. Dorren, and A. Poustie, “Packaged and hybrid integrated all-optical flip-flop memory,” Electronics Letters 42, 1399–1400 (2006).

N. Pleros, D. Apostolopoulos, D. Petranonakis, C. Stamatiadis, and H. Avramidopoulos, “Optical static RAM cell,” IEEE Photonics Technology Letters 21, 73–75 (2008).

S. Pitr, C. Vagionas, T. Tekin, R. Broeke, G. Kanellos, and N. Pleros, “WDM-enabled optical RAM at 5 Gb/s using a monolithic inp flip-flop chip,” IEEE Photonics Journal 8, 1–7 (2016).

A. Tsakyridis, T. Alexoudi, A. Milion, N. Pleros, and C. Vagionas, “10 Gb/s optical random access memory (RAM) cell,” Optics Letters 44, 1821–1824 (2019).

B. Li, M. I. Memon, G. Mezosi, Z. Wang, M. Sorel, and S. Yu, “Optical static random access memory cell using an integrated semiconductor ring laser,” in 2009 International Conference on Photonics in Switching (IEEE, 2009) pp. 1–2.

T. Alexoudi, D. Fitsios, A. Bazin, P. Monnier, R. Raj, A. Milionu, G. T. Kanellos, N. Pleros, and F. Rainieri, “III–V-on-Si photonic crystal nanocavity laser technology for optical static random access memories,” IEEE Journal of Selected Topics in Quantum Electronics 22, 295–304 (2016).

B. Dong, H. Cai, Y. Gu, Z. Yang, Y. Jin, Y. Hao, D. Kwong, and A. Liu, “Nano-optomechanical static random access memory (SRAM),” in 2015 28th IEEE International Conference on Micro Electro Mechanical Systems (MEMS) (IEEE, 2015) pp. 49–52.

R. Mathur, M. Bhargava, S. Salahuddin, P. Schuddinck, J. Ryckaert, S. Annamalai, A. Gupta, Y. Chong, S. Sinha, B. Cline, et al., “Buried bitline for sub-5nm sram design,” in 2020 IEEE International Electron Devices Meeting (IEDM) (IEEE, 2020) pp. 20–22.

P. Dong, S. Liao, D. Feng, H. Liang, D. Zheng, R. Shaﬁhi, C.-C. Kung, W. Qian, G. Li, X. Zheng, et al., “Low V_{pp}, ultralow-energy, compact, high-speed silicon electro-optic modulator,” Optics Express 17, 22484–22490 (2009).

R. Soref and B. Bennett, “Electrooptical effects in silicon,” IEEE Journal of Quantum Electronics 23, 123–129 (1987).

J. Sun, R. Kumar, M. Sakib, J. B. Driscoll, H. Jayatilleka, and H. Rong, “A 128 Gb/s 444 silicon microring modulator with integrated thermo-optic resonance tuning,” Journal of Lightwave Technology 37, 110–115 (2019).

W. Bogaerts, P. De Heyn, T. Van Vaerenbergh, K. De Vos, S. Kumar Selvaraja, T. Claes, P. Dumon, P. Bienstman, D. Van Thourhout, and R. Baets, “Silicon microring resonators,” Laser & Photonics Reviews 6, 47–73 (2012).

G. T. Reed, G. Mashanovich, F. Y. Gardes, and D. Thomson, “Silicon optical modulators,” Nature Photonics 4, 518–526 (2010).

Q. Xu, B. Schmidt, S. Pradhan, and M. Lipson, “Micrometre-scale silicon electro-optic modulator,” Nature 435, 325–327 (2005).

M. de Cea, D. Van Orden, J. Fini, M. Wade, and R. J. Ram, “High-speed, zero-biased silicon-germanium photodetector,” APL Photonics 6, 041302 (2021).

K. Padmaraju and K. Bergman, “Resolving the thermal challenges for silicon microring resonator devices,” Nanophotonics 3, 269–281 (2014).