Design of CNTFET based Domino Wide OR Gates using Dual Chirality for Reducing Subthreshold Leakage Current

Vijay Kumar Magraiya1 · Tarun Kumar Gupta1 · Bharat Garg2

Received: 28 January 2021 / Accepted: 16 December 2021 / Published online: 14 January 2022
© The Author(s), under exclusive licence to Springer Nature B.V. 2021

Abstract
The leakage current is prime concern in the modern portable battery operated device. Therefore, various techniques using MOSFET and FinFET devices are presented and their performance is evaluated and compared. To further reduce the leakage current for improved battery backup in portable devices, new devices namely Carbon Nano Tube Field Effect transistors (CNTFETs) can be used for design of different digital circuits. In this paper, subthreshold leakage power of dual chiral CNTFET based domino circuit is investigated and also the results are compared with single chiral CNTFET domino circuits. For better performance, threshold voltage of CNTFET in critical path is varied by changing the diameter or chirality of carbon nanotube. The subthreshold leakage power saving is observed in dual chiral standard and LECTOR based domino circuits for OR2, OR4, OR8 & OR16 for low temperature (25 °C) and high temperature (110 °C) with low and high input ranges. For high temperature & high input ranges, the simulation results show power saving from 89.65—97.86% and from 91.85—99.76% when compared with single chiral standard and LECTOR based domino circuits, respectively.

Keywords CNTFET · Chirality · Subthreshold leakage · LECTOR

1 Introduction
Due to the scaling limit, conventional Complementary Metal Oxide Semiconductor (CMOS) and Fin- Field Effect transistors (FinFET) technology needs to be replaced with highly efficient Carbon Nano Tubes FETs (CNTFETs). The CNTFET based domino logic circuits can show drastic improvement in power consumption due to ballistic transport phenomenon of charge carriers in CNTFET. This section first presents various characteristics of CNTs followed by the discussion on subthreshold leakage (SL) current in CNTFETs.

1.1 CNTs and its Characteristics
The CNTs are of two types based on their structures namely Single Walled CNT (SWCNT) and Multi Walled CNT (MWCNT). The SWCNT is constructed from one atom thick graphene sheet rolled in cylindrical tube. When graphene sheet is rolled across three different axes SWCNT can be classified as zigzag (n,0), armchair (n, n) and chiral (n, m) as shown in Fig. 1. Equation of three different axes known as chiral vector ($\bar{C}$) [1–3] is defined by Eq. (1)

$$\bar{C} = n\bar{a}_1 + m\bar{a}_2$$

(1)

where n and m are integers, $\bar{a}_1$ and $\bar{a}_2$ are unit vectors.

For dual chirality, different threshold voltages are achieved by varying CNT diameters. The diameter of CNT reduces when threshold voltage of CNTFET increases. The diameter [1–3] of a carbon nanotube is given by Eq. (2).

$$d = \frac{a}{\pi} \sqrt{(n^2 + nm + m^2)}$$

(2)

where $a=0.246$ nm and n & m are chiral vector integers.

1.2 Subthreshold Leakage (SL) Current Characteristics
Figure 2(a) and (b) shows subthreshold current flow in n-type and p-type CNTFET transistors, respectively. In n-type CNTFET, when gate terminal is set to ‘0’, the transistor moves in OFF state and ideally no current flows from
source to drain. However, very small current flows between them due to short channel effects (SCEs). This current is known as SL current. On the other hand, in p-type CNTFET, when gate terminal is set to high to move transistor in OFF state, the SL current flows from source to drain.

The V-I characteristics of n-CNTFET and p-CNTFET is shown in Fig. 3(a) and Fig. 3(b), respectively. As shown in Fig. 3(a), in an n-CNTFET with high values of $n$ (chiral vector integer), when source voltage increases subthreshold current increases rapidly but after a point, the slope of subthreshold current reduces rapidly with the change in source voltage. When chiral vector integer $n$ reduces or in other words diameter of CNT reduces, subthreshold current also decreases. Further, reduction in chiral vector integer does not make remarkable difference in subthreshold current. As shown in Fig. 3(a), for $n = 13$ to $n = 7$ the magnitude of subthreshold current is almost same and fall on the same line.

As shown in Fig. 3(b), the subthreshold current increases gradually with source voltage in p-CNTFET. But in case of chiral vector integer $n = 19$ when source voltage increases beyond 0.8 V sudden breakdown occurs and large amount of subthreshold current flows. When CNT diameter reduces subthreshold current decreases by very small amount and cannot be distinguished, hence subthreshold current lines overlapped. Therefore, it is concluded that $n = 13$ or 11 are best suited values for SL reduction.

The paper is organized as follows. Section 2 provides literature review whereas Sect. 3 describes the proposed techniques. Results and discussion are given in Sect. 4. Finally, Sect. 5 concludes the paper.

## 2 Literature Review

The leakage current is prime concern for the design engineers and therefore significant attention is captured by the researchers across the globe. However, various reduction techniques are presented in the literature; the leakage is still...
high and motivated us to further work. This section summarizes different work done to reduce leakage current. A lector stacking technique for gate oxide and SL current reduction is presented in [4] where p- and n-type leakage control transistors (LCTs) are introduced between pull-up and pull-down network of domino circuit. In this circuit, each LCT gate is controlled by source terminal signal of other transistor. In this technique, either n-type or p-type transistor operates near its cut-off region for any combination of inputs which leads to higher resistance between supply and ground thus reducing leakage current. Moreover, in inverter circuit a footed-diode transistor is inserted between n-type transistor and ground which offers more resistive path between supply and ground to suppress leakage current at the inverter. Kao et al. [5] show different dual threshold voltage technique which reduces total leakage power. In [5], a domino circuit simulated on three circuit variants: first all transistors with low threshold voltage, second all the transistors with high threshold voltage and third dual threshold voltage with three different modes evaluation, precharge and standby. The results found that low threshold voltage design is faster than high threshold voltage.

Gupta et al. [6] enhance their previous work with dual threshold voltage technique and removed footed-diode transistor from inverter and analyzed in four different states CHIL (Clock high and inputs are low), CHIH (clock high and inputs are high), CLIL (clock low and inputs are low) and CLIH (clock low and inputs are high). It is shown that CHIH state is effective to suppress the leakage at low temperature and CHIL is ineffective. At high temperature CHIH is preferred for high fan-in and CLIL is preferred for low fan-in. Zhou et al. [7] show that for CMOS circuit, multi-threshold CMOS technology is an effective method to reduce subthreshold leakage power and satisfies requirements for design of low power and high performance designs. Garg et al. [8] proposes Foot Driven Stack Transistor Domino Logic (FDSTDL) for designing CMOS domino logic gates with reduced leakage power and better noise performance. Asyaei [9] presented a new leakage tolerant domino circuit that provides higher noise immunity with lower power consumption and without significant delay increment for wide fan-in gates. Further in [10], a new charging scheme is presented that reduces power consumption of dynamic circuit where dynamic node discharges frequently and suitable for large fan-in gates. All these works are contributed for CMOS technology, further many circuits proposed in FinFET technology node. Moradi et al. [11] proposed several logic circuits using FinFET device which is useful for reducing total leakage power. Magraiya et al. [12, 13] also presented circuits for reduction of SL power in FinFET domino circuits with the help of ONOFIC & ONOFIC pull-up approach and achieved SL reduction.

Further, some works are going on CNTFET devices are related to device level modification. According to Avshish Kumar et al. [14], single wall CNTFETs have clear advantage over MOSFETs particularly performance is improved related to on current with respect to dielectric constant and gate insulator thickness. Hence, thinner gate oxide and larger CNT improves the performance of CNTFETs. Further, Junctionless ballistic CNTFETs (JL-CNTFET) [15] is presented by Khalil Tamersit which mitigates ultra-scaling effects and enhances performance. Electrostatic doped Schottky barrier CNTFET (EDSBCNTFET) [16] is proposed by Amandeep Singh et al. for low power memory design by leakage power reduction and better stability. Another application of CNTFET for designed a high speed and low power unbalanced ternary multiplier is in [17]. Further, a ternary SRAM cells is presented in [18] for high speed and less variation in static noise margin application. Then, another ternary SRAM cell design using 17 CNTFET transistors for energy efficient and read disturb free application is presented in [19].
It is observed from the above research work that the existing leakage reduction techniques with CMOS & FinFET devices are still not minimizing the leakage current efficiently. Further there is very less analysis done on the leakage current of circuits with CNTFETs. Therefore, this paper presents new dual chiral CNTFET based domino circuits and provides a critical analysis to minimize leakage current.

3 Proposed CNTFET Domino Circuits

To address the aforementioned leakage current problem in the recent devices, new dual chiral CNTFET based two different standard and LECTOR domino OR circuits are proposed. To differentiate high threshold transistors from low threshold transistors thickness of tube is reduced as shown in Fig. 4(b) and Fig. 6(b).

3.1 Standard Domino CNTFET OR Gate

A generalized circuit diagram for 2-inputs standard footerless domino OR gate as shown in Fig. 4(a) has same threshold voltage or single chiral tubes whereas circuit in Fig. 4(b) shows proposed dual chiral footerless domino CNTFET circuit. In dual chiral, carbon nanotube diameters of clock transistor CN1, keeper transistor CN2 and inverter transistor CN4 are varied by changing the chiral vector. Due to this, carbon nanotube diameter reduces and drain current flow in the transistor also reduces.

The working of a dual chiral CNTFET domino circuit is same as standard domino circuit: when clock is low (clk = L), the high threshold precharge transistor CN1 is ON which charges the dynamic node; this is called precharge phase. During this precharge phase, output node goes low and high threshold CN2 transistor turns ON, maintaining the dynamic node in high state. Output of domino logic is independent of the inputs applied in the evaluation transistors, whereas only the leakage current is depends on the input vectors applied. On the other hand, when the clk = H, transistor CN1 is OFF and CN2 depends on the output of the domino circuit; this is called evaluation phase. Charging of dynamic node will depend on the input vectors applied and according to output node condition which will be low or high. Flow of subthreshold current is shown in Fig. 5 using dashed arrow for low and high inputs. The next subsection presents the LECTOR based dual chiral CNTFET domino circuits to minimize the leakage.

Fig. 4 2-input domino OR CNTFET (a) Standard gate (b) Proposed dual chiral gate
Fig. 5 SL current in proposed dual chiral domino OR CNTFET gate (a) low (b) high inputs

Fig. 6 Two input domino OR CNTFET gate based on (a) LECTOR (b) Proposed dual chiral
3.2 LECTOR Domino CNTFET OR Gate

In this section, the LECTOR based 2-input domino OR CNTFET both for single and dual chiral vector are shown in Fig. 6(a) and (b), respectively. Earlier Gupta et al. [6] have presented the same logic for domino logic in CMOS technology for reduction of subthreshold and gate oxide leakage currents. But in case of CNTFET, the SL is the dominant parameter of the total leakage current, hence the focus of this work is to investigate and reproduce the same logic in case of CNTFET. In Fig. 6(b), dual chiral carbon tubes are used with clock transistor CN1, keeper transistor CN2, inverter transistor CN5 and evaluation transistors CN7 & CN8.

The proposed dual chiral LECTOR domino CNTFET circuit effectively reduces SL power. In this technique, low threshold transistor CN4 and CN6 are leakage control transistors (LCTs) [4]. The proposed dual chiral LECTOR domino gate operates similarly to proposed dual chiral standard footerless CNTFET domino gate. In the proposed circuit, when clock is low (clk = L), the dynamic node is charged through the high threshold transistor CN1, and low threshold transistor CN4. This charging is

![Fig. 7 Flow of subthreshold current in proposed dual chiral LECTOR based CNTFET domino OR gate (a) low inputs (b) high inputs](image)

_table_1 APC of Standard and LECTOR domino OR gates with proposed chirality variation

| Active Power (nW) | No. of inputs | Single V_t (n = 19) | Dual V_t (n = 19 & 15) | Dual V_t (n = 19 & 13) | Dual V_t (n = 19 & 11) | Dual V_t (n = 19 & 9) | Dual V_t (n = 19 & 7) |
|------------------|---------------|---------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| **Standard**     |               |                     |                        |                        |                        |                        |                        |
| OR2              | 2.60          | 11.72               | 8.31                   | 7.04                   | 12.21                  | 5.40                   |
| OR4              | 13.45         | 10.76               | 10.10                  | 12.03                  | 10.31                  | 5.40                   |
| OR8              | 17.32         | 11.73               | 12.08                  | 10.75                  | 10.06                  | 6.60                   |
| OR16             | 23.84         | 25.15               | 17.03                  | 34.96                  | 10.95                  | 8.89                   |
| **LECTOR**       |               |                     |                        |                        |                        |                        |                        |
| OR2              | 24.95         | 12.30               | 11.82                  | 10.46                  | 6.81                   | 6.99                   |
| OR4              | 21.81         | 14.18               | 11.54                  | 1.37                   | 5.41                   | 5.81                   |
| OR8              | 22.09         | 17.82               | 12.46                  | 11.25                  | 24.16                  | 6.01                   |
| OR16             | 23.10         | 7.17                | 3.82                   | 9.98                   | 20.19                  | 12.05                  |

© Springer
independent of the input state of previous clock. Suppose the inputs are low before the clk = L, node N2 will be at low potential and low threshold transistor CN4 offers a very low resistance path for charging of the dynamic node. If inputs are high before clk = L, then node N2 potential is not sufficient to turn completely OFF the low potential transistor CN4 (operating near cut-off region). The resistance of CN4 will be less than its OFF resistance which allows charging of the dynamic node. This case is known as precharging phase and output is independent of inputs of the evaluation network, whereas only the leakage current is dependent.

Now, when clk = H or circuit is in standby mode known as evaluation phase. In this phase, output depends on the inputs. If all the inputs are low, the dynamic node will not be discharged by the evaluation network and the output of the inverter will be low and it turns ON the high threshold transistor CN2, the voltage at node N1 will turn ON the high threshold transistor CN5. But the voltage induced at node N2 will not enough to cut-off the transistor CN4, which will operate near the cut-off region, offering a high resistance path between V\text{dd} and ground, thus reducing SL current. When all or any one the input is high, the dynamic node will be discharged through the evaluation network. The transistor CN2 will turn OFF the voltage at node N1 and will operate the transistor CN6 near its cut-off region (offering high resistance). The potential at node N2 will turn ON the transistor CN4. Therefore, the introduction of low threshold LCTs increases the resistance between V\text{dd} and ground in addition with propagation delay of the domino circuit. Flow of subthreshold current in dual chiral LECTOR based OR CNTFET for low and high inputs are shown in Fig. 7(a) and Fig. 7(b) respectively. These circuits reduce the leakage current significantly and can be effectively employed for low power designs. The next section presents the efficacy of the proposed work with simulation results.

4 Results and Discussion

To evaluate the performance of the proposed technique, zig-zag (n,0) CNTFET based domino OR gates are designed for 2, 4, 8 and 16 inputs using single threshold voltage (single

| Table 2 | Delay of standard and LECTOR domino OR gates with proposed chirality variation |
|---------|----------------------------------|
|         | No. of inputs | Single V\text{t} (n=19) | Dual V\text{t} (n=19 & 15) | Dual V\text{t} (n=19 & 13) | Dual V\text{t} (n=19 & 11) | Dual V\text{t} (n=19 & 9) | Dual V\text{t} (n=19 & 7) |
| Standard | OR2         | 1.23                | 1.35                | 1.46                | 1.69                | 3.22                | 9.35                |
| OR4      | 1.11        | 1.27                | 1.39                | 1.68                | 3.38                | 10.25               |
| OR8      | 1.25        | 1.28                | 1.48                | 1.76                | 3.91                | 12.02               |
| OR16     | 1.08        | 1.36                | 1.56                | 8.71                | 4.61                | 15.05               |
| LECTOR   | OR2         | 4.37                | 4.11                | 4.15                | 4.79                | 8.86                | 28.38               |
| OR4      | 3.43        | 3.65                | 3.79                | 4.54                | 8.82                | 28.61               |
| OR8      | 3.16        | 3.50                | 3.76                | 4.67                | 9.26                | 30.84               |
| OR16     | 3.05        | 3.62                | 4.02                | 4.99                | 10.19               | 35.64               |

| Table 3 | PDP of standard and LECTOR domino OR gates with proposed chirality variation |
|---------|----------------------------------|
|         | No. of inputs | Single V\text{t} (n=19) | Dual V\text{t} (n=19 & 15) | Dual V\text{t} (n=19 & 13) | Dual V\text{t} (n=19 & 11) | Dual V\text{t} (n=19 & 9) | Dual V\text{t} (n=19 & 7) |
| Standard | OR2         | 3.20                | 15.82                | 12.11                | 11.91                | 39.28                | 50.50                |
| OR4      | 14.93       | 13.71                | 14.07                | 20.26                | 34.88                | 55.34                |
| OR8      | 21.63       | 15.00                | 17.84                | 18.91                | 39.37                | 79.30                |
| OR16     | 25.70       | 34.18                | 26.60                | 304.61               | 50.49                | 133.80               |
| LECTOR   | OR2         | 109.01              | 50.49                | 49.07                | 50.10                | 60.32                | 198.36               |
| OR4      | 74.72       | 51.69                | 43.75                | 6.23                 | 47.70                | 166.21               |
| OR8      | 69.78       | 62.32                | 46.80                | 52.55                | 223.65               | 185.33               |
| OR16     | 70.48       | 25.96                | 15.36                | 49.79                | 205.80               | 429.51               |
chiral) and dual threshold voltage (dual chiral) CNTFETs. Stanford CNTFET Model for 32 nm [20] is used for simulating the standard and LECTOR circuits for accurate estimation of active power, delay and subthreshold currents. All the existing and proposed circuits are simulated at Vdd = 0.9 V, 4 nm gate width for 2, 4, 8 and 16-input domino OR gates. For reasonable comparison, the sizing of the n-CNTFETs and p-CNTFETs are kept same in the existing and proposed circuits. Active power consumption (APC) and delay is measured by applying a clock period of 5 ns with 50% duty cycle and simulation runs for 100 ns. The APC and delay are compared with standard, LECTOR and proposed dual chiral random OR gates (2, 4, 8 and 16 inputs) for low and high inputs. Subthreshold current is measured at 0.9 V using DC analysis by varying supply from 0 to 0.9 dc voltage and setup the inputs either low or high. For single chiral circuits all the CNTFETs have equal diameters of chiral vector integer is (19, 0). For dual chiral some of the transistor diameters are changed in the circuit by changing the chiral integer n = 19 to 15, 13, 11, 9 and 7.

4.1 Power Consumption and Delay Analysis

The active power consumption and delay of the CNTFET domino circuits at 25 °C is shown in Table 1 and Table 2, respectively. The result shows that the APC in the CNTFET domino circuit is increased with number of inputs. For chiral vector integer n = 7, minimum APC is achieved when compared to other combinations of different chiral vectors. This is due to the fact that low chiral indices offer higher threshold voltages. Similarly, the delay is increased when chiral vector integer is varied from n = 19 to n = 7. Hence, we can see a trade-off between power and delay when the chiral indices vector of the CNTFET is varied.

Power delay product (PDP) of the standard and LECTOR based domino logic for single and dual Vt is shown in Table 3. It can be observed that the PDP is increased with the number of inputs and with the decreased chiral index vector for both standard and LECTOR based chiral index logic.

4.2 Subthreshold Leakage (SL) Power Consumption at Low Temperature (25 °C)

The SL power saving in proposed dual chiral standard footerless and LECTOR domino OR gates over the single chiral domino gates for both low and high inputs are shown in Table 4. The graphical representations of the same for low and high inputs are shown in Fig. 8 and Fig. 9 respectively. From Table 4, it is found that at low temperature for low inputs, dual chiral standard footerless CNTFET domino OR gates for chiral vector integer n = 19 & 15, SL power.
saving is from 90.36% to 92.54%. Whereas, for \( n = 19 \) & 13, SL power saving is from 94.8% to 95.96%. On the other hand, for \( n = 19 \) & 11, 19 & 9, and 19 & 7, SL power saving is in all three cases is almost same from 94.67% to 95.86%. From the results it is found that for chiral integer vector \( n = 19 \) & 13 maximum SL power saving is achieved, as shown in Fig. 8(a). Also from Table 4 it is found that at low temperature for low inputs, dual chiral LECTOR based CNTFET domino OR gates for chiral vector integer \( n = 19 \) & 15 maximum SL power saving is achieved, as shown in Fig. 8(a).

Similarly, for high input at low temperature, dual chiral standard footless CNTFET domino OR gates for chiral vector integer \( n = 19 \) & 15 SL power saving is 90.66%; for \( n = 19 \) & 13 SL power saving is 95.23%; while, for \( n = 19 \) & 11, SL power saving is 95.10%; On the other hand, for \( n = 19 \) & 9 and \( n = 19 \) & 7, SL power saving is in both two cases is same 95.09%. From the results it is found for chiral integer vector \( n = 19 \) & 15 maximum SL power saving is achieved, as shown in Fig. 8(a).

Also from Table 4 it is observed that at low temperature for high inputs, dual chiral LECTOR based CNTFET domino OR gates for chiral vector integer \( n = 19 \) & 15 SL power saving is 92.85%; for \( n = 19 \) & 13, SL power saving is 96.39%; while for \( n = 19 \) & 11 SL power saving is 96.30%. On the other hand, for \( n = 19 \) & 9 and \( n = 19 \) & 7 SL power saving is in both two cases is same 96.29%. From
the results it is found that for chiral integer vector \( n = 19 \) & 11 maximum SL power saving is achieved, as shown in Fig. 9(b).

### 4.3 SL Power Consumption at High Temperature (110°C)

SL power saving in proposed dual chiral standard footerless and LECTOR domino OR gates in comparison with single chiral domino gates for both low and high inputs are shown in Table 5. The graphical representations of the same for low and high inputs are shown in Fig. 10 and Fig. 11 respectively.

From Table 5 it is observed that at high temperature for low inputs, dual chiral standard footerless CNTFET domino OR gates for chiral vector integer \( n = 19 \) & 15 SL power saving is from 89.24% to 92.27%; for \( n = 19 \) & 13 SL power saving is from 97.81% to 98.4%. On the other hand, for \( n = 19 \) & 11 SL power saving is from 99.63% to 99.94% while for \( n = 19 \) & 9 and 19 & 7 SL power saving is in both cases is same from 99.63% to 99.73%. From the results maximum SL power saving is found for chiral integer vectors \( n = 19 \) & 9 and 19 & 7, as shown in Fig. 10(a).

Also from Table 5 it is found that at high temperature for low inputs, dual chiral LECTOR based CNTFET domino OR gates for chiral vector integer \( n = 19 \) & 15 SL power saving is from 27.5% to 92.77%; for \( n = 19 \) & 13 SL power saving is from 95.91% to 98.69%; for \( n = 19 \) & 11 SL power saving is from 99.62% to 99.76%. On the other hand, for \( n = 19 \) & 9 and 19 & 7 SL power saving is in both cases is same from 99.74% to 99.83%. From the results maximum SL power saving is found for chiral integer vectors \( n = 19 \) & 9 and 19 & 7 as shown in Fig. 10(b).

Similarly, for high input at high temperature, dual chiral standard footerless domino OR gates for chiral vector integer \( n = 19 \) & 15 SL power saving is 89.65%; for \( n = 19 \) & 13 SL power saving is 97.86%; for \( n = 19 \) & 11 SL power saving is 99.53%. On the other hand, for \( n = 19 \) & 9 and 19 & 7 SL power saving is in both cases is same 99.67%. From the results, the maximum SL power saving is found for chiral integer vectors \( n = 19 \) & 9 as shown in Fig. 11(a).

Also from Table 5 it is found that at high temperature for high inputs, dual chiral standard footerless CNTFET domino OR gates for chiral vector integer \( n = 19 \) & 15 SL power saving is 91.85%; for \( n = 19 \) & 13 SL power saving is 98.39%; for \( n = 19 \) & 11 SL power saving is 99.65%. On the other hand, for \( n = 19 \) & 9 SL power saving is 99.76%; and for \( n = 19 \) & 7 SL power saving is 99.75%. From the results it is found that for chiral integer vector \( n = 19 \) & 9 provides maximum SL power savings, as shown in Fig. 11(b).

| Sub-threshold leakage | Dual \( V_t \) (n = 19 & 15) | Dual \( V_t \) (n = 19 & 13) | Dual \( V_t \) (n = 19 & 11) | Dual \( V_t \) (n = 19 & 9) | Dual \( V_t \) (n = 19 & 7) |
|----------------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Low inputs OR2       | 89.24           | 97.81           | 99.49           | 99.63           | 99.63           |
|                      | 98.05           | 99.05           | 99.54           | 99.64           | 99.64           |
|                      | 99.66           | 99.66           | 99.66           | 99.66           | 99.66           |
|                      | 99.67           | 99.67           | 99.67           | 99.67           | 99.67           |
|                      | 99.68           | 99.68           | 99.68           | 99.68           | 99.68           |
|                      | 99.69           | 99.69           | 99.69           | 99.69           | 99.69           |
| High inputs OR2      | 89.65           | 97.86           | 99.53           | 99.53           | 99.53           |
|                      | 97.86           | 97.86           | 99.53           | 99.53           | 99.53           |
|                      | 97.86           | 97.86           | 99.53           | 99.53           | 99.53           |
|                      | 97.86           | 97.86           | 99.53           | 99.53           | 99.53           |
5 Conclusion

Dual chiral technique is a reliable technique to reduce sub-threshold leakage power (SLP) in CNTFET domino circuits. It is verified from the simulation results that the dual chiral CNTFET domino OR gates reduce SLP at both low and high temperatures. At 25 °C when inputs are low dual chiral standard footerless CNTFET domino subthreshold current is minimum for chiral vector integers \( n = 19 \) & \( 13 \) and achieve SLP reduction up to 95.96%; for dual chiral LECTOR based CNTFET domino subthreshold current is minimum for chiral vector integers \( n = 19 \) & \( 7 \) with SLP reduction up to 97.3%. At 25 °C, when inputs are high dual chiral standard footerless CNTFET domino subthreshold current is minimum for chiral vector integers \( n = 19 \) & \( 13 \) and achieve SLP reduction up to 95.23%; for dual chiral LECTOR based CNTFET domino subthreshold current is minimum for chiral vector integers \( n = 19 \) & \( 7 \) with SLP reduction up to 99.76%. Hence it is investigated that dual chiral CNTFET based circuits are worth like in CMOS technology and can be effectively utilized in designing of low power CNTFET circuits.
Acknowledgements I would like to express my deep and sincere gratitude to Head of Department Dr. Kavita Khare and Director MANIT Dr. N. S. Raghuvanshi, for their constant encouragement and valuable suggestions, which served as a source of inspiration for this work.

Data Availability Not applicable.

The authors have no relevant financial or non-financial interests to disclose.

The authors have no conflicts of interest to declare that are relevant to the content of this article.

All authors certify that they have no affiliations with or involvement in any organization or entity with any financial interest or non-financial interest in the subject matter or materials discussed in this manuscript.

The authors have no financial or proprietary interests in any material discussed in this article.

Declarations

Ethics Approval Not Applicable.

Consent to Participation and Publication The paper titled “Design of CNTFET based Domino Wide OR Gates using Dual Chirality for Reducing Subthreshold Leakage Current” is our original unpublished work and we are consent to participation and publication in the Silicon Journal.

Authors’ Agreement We the undersigned declare that the manuscript entitled “Design of CNTFET based Domino Wide OR Gates using Dual Chirality for Reducing Subthreshold Leakage Current” is original, has not been fully or partly published before and is not currently being considered for publication elsewhere.

We confirm that the manuscript has been read and approved by all named authors and that there are no other persons who satisfied the criteria for authorship but are not listed. We further confirm that the order of authors listed in the manuscript has been approved by all of us.

We understand that the Corresponding Author is the sole contact for the editorial process. The corresponding author “Vijay Kumar Magraiyia” is responsible for communicating with the other authors about process, submissions of revisions and final approval of proofs.

Corresponding Author: Vijay Kumar Magraiyia.

Highlights The major contributions of the paper are as follows:
1. A comprehensive analysis on the state-of-the-art leakage reduction techniques.
2. An analysis of the leakage reduction using CNTFET devices.
3. An improved leakage reduction technique using dual chiral CNTFET in standard footless and LECTOR based domino circuits.
4. The simulation results show subthreshold leakage current reduction upto 97.3% at 25 °C and 99.76% at 110 °C.

References

1. Qin L (2007) Determination of the chiral indices (n, m) of carbon nanotubes by electron diffraction. Phys Chem Chem Phys 9:31–48. https://doi.org/10.1039/b614121h
2. Patel PK, Malik MM, Gupta TK (2018) Reliable high-yield CNTFET-based 9T SRAM operating near threshold voltage region. J Comput Electron 17:774. https://doi.org/10.1007/s10825-017-1127-z
3. Ali, K, Chaudhary A R, Juanita, K. Roy, K. and De V. “Carbon Nanotube Field-Effect Transistors for High-Performance Digital Circuits-Transient Analysis, Parasitic, and Scalability” IEEE Transactions on Electron Devices 53(11)
4. Gupta TK, Khare K (2013) Lector with Footed-Diode Inverter: A Technique for Leakage Reduction in Domino Circuits. J Circuits System and Signal Processing 32:2707–2722
5. Kao JT, Chandrakasan AP (2000) Dual-threshold voltage techniques for low-power digital circuits. IEEE J Solid-State Circuits 35(7):1099–1018. https://doi.org/10.1109/4.848210
6. Gupta TK, Pandey AK, Meena OP (2017) Analysis and design of lector-based dual-Vt domino logic with reduced leakage current. Circuit World 43(3):97–104. https://doi.org/10.1108/CW-03-2017-0013
7. Zhou Q, Zhao X, Cai Y, Hong X (2009) An MTCMOS technology for low-power physical design. Integration 42(3):340–345. https://doi.org/10.1016/j.vlsi.2008.09.004
8. Garg S, Gupta TK (2018) Low power domino logic circuits in deep-submicron technology using CMOS. Eng Sci Technol Int J 21(4):625–638. https://doi.org/10.1016/j.jestech.2018.06.013
9. Asyaei M (2015) A new leakage-tolerant domino circuit using voltage-comparison for wide fan-in gates in deep-sub-micron. Integr VLSI J 51:61–71
10. Nasserian M, Kafi-Kangi M, Maymandi-Nejad M, Moradi F (2016) A low-power fast tag comparator by modifying charging scheme of wide fan-in dynamic OR gates. Integr VLSI J 52:129–141
11. Moradi F, Cao TV, Vatjelui EI, Peiravi A, Mahmoodi H, Wiland DT (2013) Domino logic designs for high-performance and leakage-tolerant applications. Integration 46(3):247–254. https://doi.org/10.1016/j.vlsi.2012.04.005
12. Magraiyia VK, Gupta TK (2019) ONOFIC pull-up approach in domino logic circuits using FinFET for subthreshold leakage reduction. Circuits Syst Signal Process 38:2564–2587. https://doi.org/10.1007/s00034-018-0980-8
13. Magraiyia VK, Gupta TK (2019) ONOFIC-based leakage reduction technique for FinFET domino circuits. Int J Circ Theor Appl 47:217–237. https://doi.org/10.1002/cta.2583
14. Kumar A, Huisan M, Khan A, Huisan M (2014) Effect of parametric variation on the performance of single wall carbon nanotube based field effect transistor. Physica E 64:178–182
15. Tamersit K (2020) Sub-10 nm junctionless carbon nanotube field-effect transistors with improved performance. AEU-Int J Electron Commun 124:153354
16. Singh A, Khosla M, Raj B (2017) Design and analysis of electrostatic doped Schottky barrier CNTFET based low power SRAM. AEU-Int J Electron Commun 80:67–72
17. Shrivastava Y, Gupta TK (2020) Design of low power high speed CNFET 1 trit unbalanced ternary multiplier. Int J Numeric Model 33(1)
18. Shrivastava Y, Gupta TK (2021) Design of high-speed low variation static noise margin ternary S-RAM cells”. IEEE Trans Device Mater Reliab 21(1):102–110
19. Shrivastava Y, Gupta TK (2021) Design of compact reliable energy efficient read disturb free 17T CNFET Ternary S-RAM cell. IEEE Trans Device Mater Reliab 21(4):508–817
20. Stanford University CNTFET model website. Stanford, CA [Online] Available: Stanford University; 2008 https://nano.stanford.edu/model.php?id=23

Publisher’s Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.