Reversible logic gate using adiabatic superconducting devices

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Reversible computing has been studied since Rolf Landauer advanced the argument that has come to be known as Landauer’s principle. This principle states that there is no minimum energy dissipation for logic operations in reversible computing, because it is not accompanied by reductions in information entropy. However, until now, no practical reversible logic gates have been demonstrated. One of the problems is that reversible logic gates must be built by using extremely energy-efficient logic devices. Another difficulty is that reversible logic gates must be both logically and physically reversible. Here we propose the first practical reversible logic gate using adiabatic superconducting devices and experimentally demonstrate the logical and physical reversibility of the gate. Additionally, we estimate the energy dissipation of the gate, and discuss the minimum energy dissipation required for reversible logic operations. It is expected that the results of this study will enable reversible computing to move from the theoretical stage into practical usage.

Energy efficiency has become the most important metric of advancement in modern computer design\(^1\). One of the most well-known theories regarding the fundamental energy limits in computation is Landauer’s principle\(^2\), where Rolf Landauer predicted that the erasure of 1-bit information generates heat of more than \(k_BT/2\), so that the entropy of the system does not decrease, where \(k_B\) is the Boltzmann constant and \(T\) is temperature. This principle imposed the Landauer bound of \(k_BT/2\) as the minimum energy dissipation on irreversible logic operations, such as AND and OR, because they erase 1-bit information at every logic operation. After long discussions and numerical analyses of this energy bound\(^3\), some very recent experimental demonstrations that confirmed its validity have been reported\(^4\). These results indicate that the Landauer bound limits the minimum energy dissipation in modern CMOS-based computers\(^5\), which perform irreversible logic operations. In order to go beyond this bound, Edward Fredkin established a theory of reversible computing\(^6\), where the entropy of information is conserved during computation to prevent the heat generation resulting from the entropy reduction. He introduced the Fredkin gate\(^7\) as a 3-in/3-out reversible logic gate, which is logically reversible\(^8\) because its inputs are uniquely determined from its outputs, thereby conserving the entropy during computation. As part of the effort to achieve practical reversible logic gates, several physical models and devices have been proposed\(^9\). However, no reversible logic operations have been experimentally demonstrated to date.

Thus, discussions on reversible computing remain theoretical, and the question as to whether reversible computing is achievable using practical logic devices has yet to be resolved.

In order to achieve reversible logic gates, an extremely energy-efficient logic device is first necessary because the energy dissipated by the erasure of information is of the order of \(k_BT\). The bit energy of conventional logic devices, including CMOS and energy-efficient superconductor logics\(^10\), is at least larger than \((1-0.001)k_BT\), which is too large to permit their use as reversible logic gates. In contrast, the adiabatic quantum-flux-parametron (AQFP) logic\(^11\)–\(^13\), which is an adiabatic superconducting logic device, is a good candidate for use as a building block of reversible logic gates because its bit energy can go below \(k_BT\) due to adiabatic switching operations\(^14\). Figure 1a shows the equivalent circuit of an AQFP buffer/NOT gate, which is based on the quantum-flux-parametron (QFP) gate invented by Eiichi Goto\(^15\)–\(^17\). The gate is composed of inductances, \(L_1\), \(L_2\), and \(L_q\) along with the Josephson junctions, \(J_1\) and \(J_2\). By applying magnetic fluxes to the gate using an ac excitation current, \(I_0\), either \(J_1\) or \(J_2\) will switch depending on the direction of the input current, \(I_{in}\). As a result, one single-flux-quantum (SFQ) is stored in the loop composed of either \(L_1\), \(L_q\) and \(J_1\) or \(L_2\), \(L_q\) and \(J_2\), generating an output current, \(I_{out}\) through a mutual inductance, \(M = k_BqL_qL_{out}\). During this switching event, the potential energy of the gate changes adiabatically or reversibly from a single-well to a double-well, without a sudden state transition\(^12\),\(^13\). This means that the switching energy can be much smaller than the energy barrier height, \(I_c\Phi_0\) which corresponds to energy dissipation during a non-adiabatic 2π-transition in a current-biased Josephson junction, where \(I_c\) is a critical current of Josephson junctions and \(\Phi_0\) is an SFQ.
the gate is injective and logically reversible by operating the function

\[ F(a, b, c) = (\text{MAJ}(a, b, c), \text{MAJ}(a, b, c), \text{MAJ}(a, b, c)) \]

(1)

Table I is the truth table of the RQFP gate. This table clearly shows that the gate is injective and logically reversible by operating the function two times: \( F(F(a, b, c)) = (a, b, c) \). Additionally, the RQFP gate is considered to be a primitive gate in reversible computing, because MAJ, NOT gates and constant inputs constitute a logical primitive. Because a 3-in MAJ gate and a 3-out SPL gate have the same circuit topologies, the topology of the RQFP gate is symmetrical. Data in the RQFP gate can propagate bi-directionally due to this symmetrical circuit topology, depending on the order of excitation. Specifically, if the SPL gates are excited earlier (excitation current, \( I_{\text{exc}} \)), the data propagates in the opposite direction. Therefore, the RQFP gate is physically reversible.

To demonstrate logical and physical reversibility of an RQFP gate, we conducted three kinds of experiments, \( x, \beta \), and \( y \). The block diagrams of these three experiments are shown in Fig. 2a, where \( a, b, \) and \( c \) are input ports and \( x, y, \) and \( z \) are output ports. In the

![Figure 1](image_url)
experiment α, we demonstrate logic operations of an RQFP gate. In β, two RQFP gates are serially connected to demonstrate logical reversibility. Specifically, if \( a = a', b = b' \) and \( c = c' \), the RQFP gate is injective and proven to be logically reversible. In γ, two RQFP gates are connected but one is physically mirrored to demonstrate physical reversibility. Specifically, if \( a = a', b = b' \) and \( c = c' \), data can propagate bi-directionally in an RQFP gate, and the gate is proven to be physically reversible. The RQFP gates were designed and fabricated using the Nb Josephson process, the AIST standard process (STP)\(^{29}\). Figure 2b is a microphotograph of the circuits used in experiment γ, where \( I_{x1}, I_{x2}, \) and \( I_{x3} \) are three-phase excitation currents. Here, it can be seen that two RQFP gates are serially connected but their physical layouts are horizontally mirrored. Figure 2c shows the measurement results of the experiments α, β, and γ, using trapezoidal excitation currents of 100 kHz at 4.2K. In the experiment α, the correct logic operations were confirmed for the RQFP gate. In β, the obtained outputs \( (a', b', \text{ and } c') \) corresponded to the inputs \( (a, b, \text{ and } c) \), which proves the logical reversibility of the RQFP gate. Similarly, the outputs corresponded to the inputs in γ, which proves its physical reversibility. These results confirm that the RQFP gate is logically and physically reversible, and that the RQFP gate is a practical reversible logic gate.

Next, we calculated energy dissipation of the RQFP gate by integrating the product of excitation currents and voltages over time using the Josephson circuit simulator, JSIM\(^{29}\). Figure 3a shows a block diagram for the simulation, where input and output buffers are inserted to avoid the interaction with input and output ports. Figure 3b provides the simulation results and shows the total energy dissipation per clock cycle, including an RQFP gate, input and output buffers, as a function of a rise/fall time of excitation currents. As can be seen in the figure, energy dissipation decreases almost linearly with an increase in the rise/fall time for all input patterns, which indicates that all gates operate adiabatically and reversibly during logic operations\(^{25,28}\). For a rise/fall time of 10,000 ps, the total energy dissipation of the RQFP gate and buffers composed of 69 AQFP gates reaches \( \sim 1 \times 10^{-20} \) J/cycle. The bit energy per AQFP gate is \( \sim 2 \times 10^{-21} \) J/cycle, which is much smaller than the barrier height, \( I_m \phi_B \sim 1.0 \times 10^{-10} \) J for \( I_c = 50 \) μA and around the same order of magnitude as the Landauer bound at 4.2 K, \( k_B T \ln 2 \sim 4.0 \times 10^{-20} \) J. These calculation results show that there is no minimum energy dissipation for reversible logic operations using the RQFP gates.

**Conclusions**

Based on the above results, we can conclude that the RQFP gate is the first practical reversible logic gate. It is clear that through the use of

![Figure 2](https://www.nature.com/scientificreports/images/2014/figure2.jpg)

**Figure 2** | Demonstration of logical and physical reversibility of the RQFP gate. (a) Block diagrams for experiments α, β, and γ. In α, three inputs \( (a, b, \text{ and } c) \) are externally applied and three outputs \( (x, y, \text{ and } z) \) are observed to confirm its logic operations. In β, two RQFP gates are serially connected to determine if the gate is injective. In γ, two RQFP gates are serially connected but one is mirrored to determine if data can propagate bi-directionally. (b) Micrograph of circuits for the experiment γ. Dc superconducting quantum interference devices (dc-SQUIDs) were used for readout of output ports \( (a', b', \text{ and } c') \), which detect output currents of buffer gates. One of the two RQFP gates is physically mirrored. (c) Measurement results, which were conducted at 4.2 K in liquid He. We used three-phase trapezoidal excitation currents of 100 kHz \( (I_{x1}, I_{x2}, \text{ and } I_{x3}) \). Input currents \( (a, b, \text{ and } c) \) were given by using a data-pattern generator. Output voltages were amplified by differential amplifiers.
Figure 3 | Energy dissipation of the RQFP gate. (a) Block diagram for simulation. Input and output buffers were inserted to avoid interaction with input and output ports. (b) Simulated energy dissipation, including an RQFP gate, input and output buffers. It was assumed that \( I_{\text{in}} = I_{\text{out}} \) and \( k_{\text{in}} = 0.1 \) for AQFP buffer gates, and that each wiring inductance is 10 pH for 3-in MAJ gates and 3-out SPL gates. For all input patterns, energy dissipation decreases almost linearly with an increase of a rise/fall time of excitation currents, which indicates that there is minimum energy dissipation for reversible logic operations using RQFP gates (see Supplementary Information for energy dissipation of irreversible logic gates). The inset shows the definition of an excitation current.

RQFP gates, detailed discussion and investigations on the energy efficiency of reversible computing will become possible. Although the energy dissipation of the RQFP gate was too small to measure in the slow-speed demonstration at 100 kHz, we expect that we will be able to measure it at a higher operation frequency (~1 GHz) in future work by using high-speed interface circuits and the superconducting resonator-based method. Also, in previous work, we have confirmed that calculation results of energy dissipation well agree with experimental results using superconducting resonators.

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Author contributions

N.T. designed circuits, carried out simulations and experiments, and wrote the paper. Y.Y. and N.T. supported theoretical aspects and supervised simulations and experiments. All authors discussed the results and commented on the manuscript.

Additional information

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