Reliable Resistive Switching Behaviour of Ag/Ta$_2$O$_5$/Al$_2$O$_3$/p$^{++}$-Si Memory Device

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Abstract. In this article, we demonstrate a resistive switching memory device based on a very simple bilayer structure of Ag/Ta$_2$O$_5$/Al$_2$O$_3$/p$^{++}$-Si. As compared to a single-layer based device of Ag/Ta$_2$O$_5$/p$^{++}$-Si, a uniform bistable resistive switching behaviour with on/off ratio over $10^4$ demonstrates that the Ag/Ta$_2$O$_5$/Al$_2$O$_3$/p$^{++}$-Si device could be a promising candidate for the memory device, in which the total resistance could also be adjusted by modifying the applied electric field. In the low voltage sweeping region, gradual increase and/or decrease in resistance can also be observed, indicating that an analog type of switching behaviour similar to the first demonstrated memristor device has also been observed in the newly made device. This study could open up new ways for the design of multi-functional devices which are promising for memory and neuromorphic computing applications.

1. Introduction
Memristive devices (i.e., memristor) have become the most promising nonvolatile memories due to low power consumption, fast speed and high integration density [1]. In memristors, two types of switching mechanisms, i.e., valence change memory (VCM) and electrochemical metallization (ECM) are involved [2]. The ECM mechanism is very promising owing to its excellent scalability, which enables the construction of large-scale computing systems [3]. The ECM-based memristor consists of an insulating layer between active electrode (e.g., Ag, Cu) and an inert metal (e.g., Pt, Ta). In contrast, an insulating layer is placed between the inert metal electrodes in VCM based memristor device. As compared to VCM, ECM based memristor is lower in reliability because of the mobility of the high ions in the dielectric layer[4].

Due to its outstanding scalability, which could make the development of large-scale computing structures, the ECM RRAM is highly promising. Great efforts were made to enhance the performance of ECM-based RRAM, for example, doping of cations in the dielectric layer [5], dielectric layer insertion (such as Al$_2$O$_3$ [7] and TiO$_x$ [8][9]), using active metal alloys [6]. In ECM-based memories, multilayer dielectrics are one of the interesting approaches to be adopted by researchers to enhance the switching performance. Besides other metal oxides, Ta$_2$O$_5$ has also been commonly used as a dielectric layer because of its porous structure. In this Ta$_2$O$_5$-based device, Ag$^+$ ions concentration could be increased due to porous structure, resulting in strongly Ag filament [7]. The device, however, could only repeat operations approximately 350 times [8]. We know that the resistive switching behaviour ECM based memristor is facing reliability issues due to random formation/rupture of
conductive filaments. However, the pores structure of dielectric layer could facilitate the accumulation of more Ag in the dielectric layer, which significantly decreased the on/off ratio.

In our current study, the Ta$_2$O$_5$-based memristors are prepared by inserting a thin layer of Al$_2$O$_3$, where Ag and p$^{++}$-Si are used as TE and BE, respectively. The Ta$_2$O$_5$-based memristor without Al$_2$O$_3$ thin layer exhibited small on/off ratio and poor performance. However, when an Al$_2$O$_3$ thin layer is inserted between the Ta$_2$O$_5$/p$^{++}$-Si interface, the device is a uniform digital switching with good performance can be achieved. Furthermore, the Ag/Ta$_2$O$_5$/Al$_2$O$_3$/p$^{++}$-Si device exhibits a reliable analog switching with corresponding synaptic behaviour. Our present results coincide the published observations in which analog switching behaviours can be obtained besides digital switching in filamentary memristors [9].

2. Experimental Details

The p$^{++}$-Si substrates (BE) were cleaned using a standard RCA method. After that Ta$_2$O$_5$ (100 nm) and Al$_2$O$_3$ (100 nm), thin layers were deposited on the p$^{++}$-Si substrate by a physical vapour deposition process using the Ta$_2$O$_5$ and Al$_2$O$_3$ targets and Ar sputtering gas (0.5 Pa of working pressure). A 200-nm-thick Ag top electrode (TE) was then deposited, realizing the Ag/Ta$_2$O$_5$/Al$_2$O$_3$/p$^{++}$-Si device structure. Meanwhile, a single-layered Ta$_2$O$_5$ was sandwiched between BE and TE to form a Ta$_2$O$_5$-based RRAM in order to compare the effect of Al$_2$O$_3$ film on the performance of the memristor device. The current-voltage (I-V) characteristics were measured using a power source (Keithley 2636B) that was hooked with a probe station at room temperature.

3. Results and Discussion

Figure 1(a) shows the current-voltage (I-V) characteristics of an Ag/Ta$_2$O$_5$/p$^{++}$-Si memory device operated under 5 mA compliance current. The I-V sweep is applied from 0 V → +4 V → -3 V → 0V. It shows a typical bipolar switching behaviour with SET and RESET states. It should be noted that a for a SET electroforming process is needed and RESET state is achieved when TE is negatively biased. For the digital type of switching, a suitable $I_{cc}$ requires to avoid the current overshoot and to tune the LRS state. If low $I_{cc}$ is applied, due to the formation of thin conductive filament, the performance of the device will not be uniform and reliable [10]. When we applied of 5 mA $I_{cc}$ to an Ag/Ta$_2$O$_5$/p$^{++}$-Si memory device, a small switching window of 10 is achieved, which is not quite suitable for practical device application [11]. Also, figure 1(b) and (c) show that the SET and REST voltage and the LRS and HRS states are distributed over a broad range, indicating a noticeable fluctuation in the switching parameters of the device. In order to control the Ag filament growth, an Al$_2$O$_3$ film is inserted in the Ag/Ta$_2$O$_5$/p$^{++}$-Si structure. An abrupt change is a resistance from HRS to LRS is realized with on/off ratio $10^4$, as shown in figure 1(d). A narrow distribution can also be observed in figure 1(e) and (f) for switching parameters fluctuation, indicating a better operational uniformity. Usually, an on/off resistance ratio of more than 10 is enough to accomplish the data storage with a low reading-error. It has been reported in many studies that above $10^6$ ratio has been providing a wide memory operating window [11].

For the understanding of physical processes from I-V characteristics, electron transport behaviour during the switching process is considered. So, the positive regions of the I-V curves in both kind of devices in the double logarithmic scale shown in figure 2(a) and (b). For the Ag/Ta$_2$O$_5$/p$^{++}$-Si memristor, a steep change in conductance with a slope $\sim$ 9 is followed by the linear I-V with slope $\sim$ 1.2. It indicates here that a conduction behaviour is dominated by Ohmic current due to thermally generated charge carriers at HRS. While at LRS, the fitting results show the liner behaviour with slope $\sim$ 1.3, indicating the Ohmic conduction. Such type of charge transport behaviour at HRS and LRS can only be realized from the formation/rupture of conducting filaments. For the Ag/Ta$_2$O$_5$/Al$_2$O$_3$/p$^{++}$-Si memory device, the charge transport behaviour can be explained by space charge limited conduction (SCLC), ECM, VCM mechanism. From the linear fitting results, three portions: the Ohmic region (I/V), the Child’s law region (I/V$^2$) and the steep current region [12] are exhibited at HRS indicating the conduction mechanism at HRS can be well explained by SCLC mechanism. In Ag/Ta$_2$O$_5$/Al$_2$O$_3$/p$^{++}$-Si memristor, at high voltage bias applied to the TE, Ag atoms are diffused in the dielectric layer and form an Ag conductive filament resulting in a sharp increase in current. Moreover,
it is known that if SCLC does not lead the conduction behaviour at HRS, then other conduction mechanisms (such as Poole–Frenkel emission and Ohmic conduction) are consecutively realized at the LRS. But, at LRS region, the Ohmic (I/V) conduction is dominated with a slope of 1.3. The different conduction behaviour at HRS and LRS indicates that the resistive switching behaviour of Ag/Ta2O5/Al2O3/p++-Si memristor is realized on the growth of Ag-filament [13].

![Figure 1](image1.png)

**Figure 1.** (a) I-V curves and (b) cumulative distribution of reset/set operating voltage and (c) HRS/LRS states in the Ag/Ta2O5/p++-Si memory device during 100 cycles; (d) I-V curves and (e) cumulative distribution of reset/set operating voltage and (f) HRS/LRS states in the Ag/Ta2O5/Al2O3/p++-Si memory device during 100 cycles.

![Figure 2](image2.png)

**Figure 2.** I-V curves of the positive region in both devices (a) Ag/Ta2O5/p++-Si and (b) Ag/Ta2O5/Al2O3/p++-Si plotted in double logarithmic scale.

In order to demonstrate the physical mechanism involved in both kinds of memory devices during the switching process, a physical model is presented in figure 3. Figure 3(a) and (e) show the structures of Ag/Ta2O5/p~+Si and Ag/Ta2O5/Al2O3/p~+Si memristors, respectively. Figure 3(b) illustrates, in Ag/Ta2O5/p~+Si memristor, Ag atoms are oxidized in Ag+ ions when TE is positively biased, and these Ag+ ions are reduced to Ag atoms again near BE due to thermally produced or through the p~+Si BE. The electric field spread across the dielectric layer between the electrode could result in the formation of multiple and weak Ag filaments. Figure 3(c) shows when of biased voltage is further increased, the Ag-filaments bridges the TE and the BE, the device achieved LRS from HRS.
Figure 3(d) shows that when the TE is biased negatively, high current is passed through the device and Ag-filaments ruptures by Joule heating effect due to high current. The fluctuation in switching behaviour might be caused by weak and multifilament from TE to BE.

![Figure 3. Formation/rupture of Ag conductive filament in Ag/Ta2O5/p++-Si and Ag/Ta2O5/Al2O3/p++-Si memristors. (a) Pristine Ag/Ta2O5/p++-Si device and (b, c) formation of Ag filaments (d) rupture of Ag filaments; (e) Pristine Ag/Ta2O5/Al2O3/p++-Si device and (f, g) growth of Ag-filaments (h) and dissolution of Ag filaments.](image)

Figure 3(f-h) shows when a TE of Ag/Ta2O5/Al2O3/p++-Si memristor is enough positively biased, Ag atoms can be diffused into the dielectric thin film and move towards the p++-Si BE resulting in the growth of a strong Ag filament. This is realized a stable and uniform switching. From figure 3(g), the growth of filament is from TE to BE and it much thicker in the Ta2O5 film as compared to Al2O3 thin film. When TE is enough negatively biased, the thinnest part of filaments in Al2O3 is broken at about -2.3 V with less risk of negative-SET when stressed voltage is further increased.

From Figure 4, it is observed that the resistance of memristor gradually increases or decreases under repetitive voltage bias in a DC mode. A continuous SET or RESET process can be realized when increasing voltage bias from 2.0 V to 4.0 V and from -1.8 V to -2.8 V applied, resulting in a gradual change of conductance. It is worth noting that this type of continuously decreasing or increasing in resistance between these multiple intermediate states is a typical characteristic of analog type switching. This kind of switching behaviour is distinct from sudden conductance change will be observed when the device is switched HRS to LRS under a non-identical sweeping bias. From these results, we can infer that the conductance of the device can be adjusted by modulating the applied electric field in Ag/Ta2O5/Al2O3/p++-Si memory devices. It is obvious that switching parameters are tightly concentrated and uniform as compared to those in Ag/Ta2O5/p++-Si memory devices, as shown in figure 1. Therefore, it can be assumed that these experimental results might result from the effective confinement of the filament formation/rupture in a bi-memristive-layer structure.

In a digital-type of switching, a high HRS/LRS ratio manifests the digital type of switching through the abruptly unbridged and bridged Ag CF filaments across the TE and BE. In contrast, repetitive sweeps under a voltage less than that of SET are not enough for the formation of Ag-filament to ultimately bridge electrodes. However, at low biased voltage, Ag atoms are diffused at the Ag/Ta2O5 interface, as shown in figure 3(f, g). Furthermore, when the TE is negatively biased, a decrease in the gap between TE and BE would be promoted the decrease in conductance of the device. It is expected that the gap between TE and BE will decrease and the cross-sectional size of Ag-CFs will also increase, resulting to a rise in the gradual increase in conductance, as shown in figure 4(a).
Figure 4. Analog switching characteristics of Ag/Ta$_2$O$_5$/Al$_2$O$_3$/p$^{++}$-Si memristor. (a) Continuous SET and (b) RESET processes non-identical consecutive sweeps using positive and negative biased voltages.

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5. Conclusion
In summary, we have demonstrated a reliable resistive switching behaviour in a simple Ag/Ta$_2$O$_5$/Al$_2$O$_3$/p$^{++}$-Si memory device compared to a Ta$_2$O$_3$-based memory device. The digital type of switching behaviour initiates from the bridged and unbridged of Ag-CFs. The analog type of switching characteristic can be obtained by the continuous growth and contraction of Ag filaments under the increasing electrical field only in Ag/Ta$_2$O$_5$/Al$_2$O$_3$/p$^{++}$-Si memory device. This simple memristor device has demonstrated its potential for nonvolatile memory and in artificial synapse applications as well in the near future.

6. References
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