22nm FDSOI SRAM single event upset simulation analysis

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Abstract. This article uses Sentaurus TCAD to establish the 3D device model of NMOS and PMOS under the 22nm FDSOI process, and establishes the 3D model of the 22nm FDSOI SRAM cell through this model. This model is used to numerically simulate the single event upset LET threshold of the 22nm FDSOI SRAM cell. The effects of different LET values and different incident conditions on the single event upset of a 22nm FDSOI SRAM cell are compared. The results show that whether the 22nm FDSOI SRAM cell is single event inversion depends on the transient current peak value generated after heavy ion incidence. For the 22nm FDSOI SRAM cell, the critical current peak value is about 0.011mA. Comparing the single event inversion thresholds at different incident positions, it is found that compared to the center of the channel, when a single event is incident on the channel-drain PN junction of an off-state N-type FDSOI device, the SRAM cell is more prone to single event inversion.

1. Introduction
With the continuous reduction of device node capacitance and power supply voltage, the single event effect caused by irradiation has become more and more obvious. With the continuous progress of CMOS device technology, the pulse width of transient disturbance caused by SEE has become larger and larger. The operating frequency of SET is getting higher and higher, and the number of errors caused by the SET effect is also increasing, far exceeding the influence of SEU on the circuit. At this time, SEU and SET will work together, making it more difficult for the circuit to work normally. Generally, SRAM circuits need to work in a large-dose irradiation environment for a long time, and they are particularly sensitive to SEU in the SEE effect. Especially under the trend of continuous development of circuits, the critical charge threshold of SRAM for SEU is significantly reduced, this will directly cause the radiation resistance of SRAM to become worse and worse.

When a radiant particle is incident on a node of the circuit and a single event upset (SEU) occurs, then transient voltage and current pulses will be generated, resulting in a 1-bit upset of the storage node of the SRAM cell. As the most promising device structure in the future, FDSOI has gradually replaced the traditional planar CMOS process in a smaller size. Therefore, it is necessary to discuss the sensitivity and stability of FDSOI-based SRAM cells to single-particle radiation.

This article will perform circuit simulation based on the Sentaurus software platform on the 4T-SRAM cell, and extract the single event upset (SEU) threshold of the SRAM cell.

2. SRAM memory cell single event upset mechanism and TCAD modeling

2.1. SRAM memory cell single event upset mechanism
The SRAM 6T unit circuit is shown in the figure. Among the six MOS, P1, P2, N1, and N2 are bistable circuits composed of two inverters to store a digital signal. N3 and N4 are control switches for
operating the unit, called select transistor. The gate of the select transistor is connected to the word line WL (word line) under the control of the row decoder, and the drain is connected to the bit line BL (bit line) or BLB (the opposite signal of BL). When information needs to be written to a certain cell, the WL of the cell is high, which turns on the select transistor. If write "1", BL is high level, BLB is low level, N1 is turned on, N2 is turned off, that is, Q is charged to high level and QB is discharged to low level, thus writing "1"; If write "0", BL is low level, BLB is high level, turn N1 off and N2 on, write "0" into the internal circuit. During the read operation, both the bit lines BL and BLB are precharged to high level, and then the word line of the unit is made high through the row decoder.

![Figure 1. Six-transistor SRAM.](image)

The single event upset effect refers to the effect that high-energy particles impact the storage circuit and cause the storage state to change. The single event flipping LET threshold is defined as the minimum LET value required to upset the device state. Therefore, the single event upset LET threshold is an important parameter to measure the ability of a circuit to withstand heavy ion radiation. SRAM is used as a storage unit, and the internal two pairs of cross-coupled inverters store "0" and "1" at two nodes respectively. Heavy ion radiation SRAM cells may cause storage errors and reverse the original stored values. The LET value corresponding to the storage state upset is just the single event upset threshold of the SRAM cell. The upset threshold of SRAM is mainly determined by two pairs of cross-coupled inverters.[1]

2.2. 22nm FDSOI SRAM cell TCAD modeling

In order to study the impact of single particle irradiation on SRAM cells, Sentaurus' hybrid circuit simulation function is needed. Sentaurus Device not only supports the modeling and simulation of a single device, but also supports mixed-mode circuit simulation. First, obtain the P-type and N-type FDSOI 3D device models required by the SRAM unit through Sentaurus modeling. Define the shape of the device through the Sentaurus Structure Editor, that is, the boundary conditions, structure, doping type, concentration and other information.

In this paper, the design of the structure parameters of the N-channel device is based on the 22 nm UTB FDSOI process in the literature [2]. The physical channel length is 28 nm, the gate oxide thickness is 1 nm, the top silicon film thickness is 6 nm, and the buried oxide layer (BOX) thickness is 20 nm. The device structure is built according to the TCAD simulation process described above.
Based on the accurate SPICE model provided by the process manufacturer, perform characteristic curve scanning simulation on the NMOS SPICE model that needs to build a three-dimensional device model, and obtain its IV characteristic curve as a standard parameter for process alignment. At the same time, use TCAD three-dimensional simulation software to compare with SPICE Model the same size NMOS device model for 3D device simulation, and obtain the IV characteristic curve under the 3D simulation condition. By repeatedly adjusting the process parameters of the 3D model, such as doping concentration, gate oxide thickness, etc., finally make the IV characteristic curve of the two fit well, that is, it is considered that the established three-dimensional device model is accurate and can reflect the device characteristics under actual process conditions. The results obtained after fitting are as follows.

![Device Model Calibration Results](image)

Figure 3. Device model calibration results (IdVg curve): (a) NMOS, (b) PMOS.

Since this article mainly discusses the impact of single event incident on the storage node of the SRAM cell, the word line is not enabled when the SRAM cell is in the storage state, that is, the level on the word line is zero, and the N3 and N4 transmission tubes are not turned off. Therefore, it is not used in the simulation. Consider the role of two transfer tubes. In order to more accurately describe the circuit changes under the single-event transient state of the device, a 4T SRAM cell is obtained through Sentaurus modeling.
3. SRAM memory cell single event upset effect simulation analysis

In this simulation, only the N-type SOI device in the SRAM cell is irradiated under the off-state condition. The heavy ion incident trajectory still adopts Gaussian distribution, the characteristic radius is 10nm, and the heavy ion incident time also adopts Gaussian distribution, and the incident depth is 1μm, observe the transient response and the effect on the storage state of the SRAM cell. Suppose that at the initial time of the simulation, the SRAM cell n0 node stores the logic "1", and the n1 node stores the logic "0".

3.1. The influence of different LET values on the single event upset of SRAM cells

First, the SEU upset threshold is simulated. Under the original condition that the storage node n0 is "1", heavy ions bombard the pull-down transistor and enter the center of the off-state FDSOI NMOS drain terminal. When the heavy ion upset threshold is reached, the n0 node will upset from "1" to "0". The figure below shows the node voltage node inversion of node n0 and node n1 when different LET values are selected for heavy ion incidence.

![Figure 5. Voltage reversal of n0 node and n1 node when different LET values are incident](image)

At the same time, it can be seen from the above figure that before the unit is turned over, with the increase of the LET value, the voltage fluctuations of the n0 and n1 nodes are more obvious, and the recovery time increases accordingly. After the cell reversal occurs, as the LET value increases, the time required for the voltage reversal of the n0 and n1 nodes is smaller.[5]

With the increase of the LET value, the peak value of the pulse current at point n0 increases rapidly, the voltage fluctuation becomes deeper and deeper, and the time required to reach the lowest point becomes longer and longer. This is because as the incident LET value of particles increases, more and more electron-hole pairs are generated after the incident, and it takes longer and longer for the drain of
the device to collect charges, which causes the time for the voltage to drop to the lowest point at n0 to be delayed. Rear. Under the condition of a small LET, the voltage at n0 point slowly returns to the initial logic voltage state after being reduced to a certain point. It can be considered that the SRAM does not have a single event upset at this time. But when LET increases to more than 2.9 MeV·cm²/mg, the voltage at n0 is reversed under the influence of the transient pulse current. Since the SRAM memory cell is a bistable circuit composed of two inverters, the drain voltage of the N2 transistor decreases, which will turn off the N1 tube, turn on the P1 tube, and the charging voltage of the drain terminal of the N1 transistor will rise, which will be positively fed back to the N2 and P2 tubes. The N2 transistor is turned on and the P2 transistor is turned off, and the storage logic value changes from high to low. It can be seen from Figure 5(a) that after the voltage at point n0 is reversed downward at a larger LET value (LET>2.9 MeV·cm²/mg), the circuit can no longer be restored to the original storage state, plus the feedback effect of the circuit Influe nce, the voltage at the node gradually stabilizes to a voltage of about 0V, and the voltage state at this time is stored in the circuit. Unless the write signal is valid, the 6T SRAM will always store the “0” state, that is, the so-called single event occurs. During the period from the occurrence of the rollover to the writing of the new data, all the data read from the SRAM cell is wrong.

3.2. The impact of different incident positions on the single event upset of the SRAM cell

It can be seen that when the incident energy of a single particle is 2.9 MeV·cm²/mg, the FDSOI NMOS irradiated by the single particle switches from the off state to the on state, the device is turned on, and the SRAM cell is flipped. As shown in the figure below, the more accurate upset threshold of the SRAM cell is between 2.8 MeV·cm²/mg and 2.9 MeV·cm²/mg. The figure below shows the curve of the n1 node voltage, the n0 node voltage and the n0 node current change with time when the incident energy of a single particle is 2.9 MeV·cm²/mg.

![Figure 6](image)

**Figure 6.** (a) The voltage inversion at node n0 and node n1 when single event incident occurs at critical time (b) NMOS gate and drain voltage and drain transient current during upset

The figure below is the curve of (a) the voltage inversion at node n0 and node n1 and the transient leakage current at node n0 with time when a single particle is incident on the junction of the channel and the drain.

It can be found from the figure that the SEAM unit starts to upset when the LET is 2.4 MeV·cm²/mg. The figure below shows the time-varying curve of the voltage at the n1 node, the voltage at the n0 node and the current at the n0 node when the incident energy of a single particle is 2.4 MeV·cm²/mg. It can be seen from the figure that at t = 21.4 ns, the voltage of node n0 is equal to the voltage of node n1. At this time, it is considered that the FDSOI NMOS irradiated by a single event changes from the off state to the on state, the device is turned on, and the SRAM cell is turned over.
It can be found that when a single particle is incident on the junction of the drain terminal and the channel, the SRAM upset threshold becomes smaller. This is because the sensitive position of the 22nm FDSOI device is located at the junction of the drain end of the device and the channel. By comparing the inverted LET threshold corresponding to different incident positions and the corresponding leakage current peak value. It can be seen that the peak current during single event inversion is about 0.011 mA.

4. Conclusions
Through the circuit simulation of single event irradiation on 22nm FDSOI SRAM, the research and analysis of SRAM cell flipping characteristics with different LET values and different incident positions are discussed: For 22nm FDSOI SRAM cell, whether single event upset (SEU) occurs depends on the peak value of transient current generated after heavy ion incidence. For different LET values and incident positions, the critical current peak value of the SRAM cell for single event inversion is basically the same, which is about 0.011mA. In other words, for the SRAM cell used in the simulation, the peak node current \( \geq 0.011 \text{mA} \) is one of the conditions for the SRAM cell to occur single event upset (SEU). Comparing and calculating the critical turnover LET thresholds for different incident positions, it is found that when a single particle is incident on the channel-drain P-N junction of the off-state N-type 22nm FDSOI, the SRAM cell is more prone to single event upset (SEU).

References
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