MSCCL: Microsoft Collective Communication Library

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Abstract

Machine learning models made up of millions or billions of parameters are often trained and served on large multi-GPU systems. As models grow in size and execute on more GPUs, the collective communications used in these applications becomes a bottleneck. Custom collective algorithms optimized for both particular network topologies and application specific communication patterns can alleviate this bottleneck and thus help these applications scale.

This paper introduces MSCCL, a system designed to make GPU communication programmable. MSCCL provides a data oriented domain specific language for writing custom collective communication algorithms and an optimizing compiler for lowering them to an executable form, which can be executed efficiently and flexibly in an interpreter based runtime. We used MSCCL to write novel collective implementations for AllReduce and AllToAll that are up to 48% and 20% faster than optimized vendor implementations, respectively. We also demonstrate how directly implementing an application specific collective called AllToNext in MSCCL results in a 14.5× speedup over the baseline.

1 Introduction

Recent trends in machine learning have increased the importance of efficient communication. First, machine learning models have been growing to hundreds of billions to trillions of parameters and beyond. At these sizes, models have to be partitioned across multiple GPUs because of both per-GPU memory constraints and parallelism required for both training and inference. This puts communication in the critical path for performance. At the same time, novel model architectures and partitioning schemes give rise to diverse communication patterns [14]. For instance, Mixture of Experts (MoE) models use the AllToAll collective, which has not been common in model and data parallelism. Finally, the hardware trends in GPU clusters have led to hierarchical and heterogeneous networks with modern cloud providers using bespoke hardware configurations to trade off between customization and efficiency.

These trends give rise to a need for flexible communication libraries that support the diverse collective primitives present in modern workloads, while providing optimized implementations of these primitives for various multi-GPU systems. NCCL (NVIDIA Collective Communication Library) [16], the current state-of-the-art library of communication kernels for NVIDIA GPU systems, provides hand-written implementations of some collective primitives. While they perform well with some system configurations and certain data sizes, we have found that they are often far from optimal. Furthermore, NCCL’s limited set of collectives does not cover the needs of all modern machine learning workloads.

This paper presents MSCCL, a language for specifying custom communication kernels in a declarative style, a compiler that automatically lowers a MSCCL programs into an optimized low-level representation, and a low-overhead runtime interpreter for efficiently executing these low-level representation. Together, MSCCL enables quick prototyping and customization of collective communication algorithms while matching, and many times beating, the performance of hand-written kernels. We have implemented and evaluated these ideas for communication with NVIDIA GPU systems, but they can naturally be extended to systems from other vendors.

The MSCCL language allows users to express communication patterns in a data-flow style. Rather than specify the program as a set of processes communicating through sends and receives, the language takes a chunk-oriented view: MSCCL programs specify the GPUs input chunks traverse from their sources to their destinations. Figure 1a gives an example of chunk-oriented AllToAll algorithm. In our experience chunk-oriented data-flow is a natural way of expressing collective algorithms, and we aim to demonstrate that in our case studies.

The MSCCL compiler lowers the chunk-oriented program into a per-GPU, process-oriented representation. In this translation, the compiler automatically infers low-level details involving scheduling, memory allocation and synchronization.
Peep-hole optimizations for instruction combining increase performance without complicating the frontend language, while a chunk subdivision optimization increases the amount of available parallelism.

The MSCCL runtime executes the process-oriented representation at each GPU in the network in a single kernel. The runtime hides the complexity of sending data over different types of links, such as NVLinks or PCIe for intra-node communication, InfiniBand (IB) for inter-node communication etc. Rather than re-implementing the runtime from scratch, MSCCL runtime is a carefully-architected version of NCCL with an execution engine that can execute MSCCL programs while reusing most of the facilities of NCCL. This makes integration of MSCCL runtime into existing ML frameworks such as PyTorch straightforward by changing NCCL repository pointer to MSCCL repository. Also, MSCCL is API compatible with NCCL which means that no changes in model are required and in the case where there is no MSCCL custom kernel for a given collective such as AllReduce, our runtime falls back on NCCL’s implementation. Lastly, MSCCL is open-source and it is being used for multiple internal models in a large enterprise company.

While MSCCL language is designed for ease of use and provides automatic scheduling, we provide language extensions that give full control of low-level scheduling details. Our case studies demonstrate how this can be used to further improve performance.

Our case studies focus on four scenarios that we identified as not being well-served by NCCL. For example, NCCL does not provide a dedicated algorithm for AllToAll, but it can be implemented using simple send operations. However, our custom MSCCL algorithm improves performance over NCCL on multiple nodes by up to 20%. Even when NCCL does include an algorithm MSCCL can help, as we demonstrate by implementing a single-node AllReduce algorithm that beats NCCL by up to 48% on some medium data sizes important for an industrial inference workload. We also implement a hierarchical AllReduce algorithm for multi-node training scenarios. Finally, we demonstrate the opportunity MSCCL offers for optimizing application specific communication patterns by implementing AllToNext, a collective version of a pipelined send. By allowing idle InfiniBand hardware to be utilized, this MSCCL program offers a massive 14.5× improvement over NCCL.

2 Overview

This section explains MSCCL system through a real-world scenario, where we used MSCCL to optimize a production training workload. Section 6 presents the detailed evaluation of this case study.

When training a state-of-the-art Mixture of Experts [14] model, the model engineers found through profiling that a significant percentage of time was spent in the AllToAll collective. The training was performed on a cluster of A100 GPUs, with each 8-GPU node interconnected with each other through InfiniBand (IB) links (see Figure 2). We found the performance of NCCL’s AllToAll to suffer due to many small cross-node InfiniBand sends/receives. We show how MSCCL can be used to quickly develop an alternate implementation of AllToAll optimized for this cluster.

**AllToAll Collective.** In the AllToAll collective, each rank simultaneously sends an input chunk to every other rank. The network consists of N nodes, each with G gpus. Each rank can be identified with a tuple (n, g) where 0 ≤ n < N is the node index and 0 ≤ g < G is the GPU index. For ease of exposition, we will use (n, g) to represent the integer n × G + g, which is useful to index into chunk buffers. The input buffer at each rank has N × G chunks. AllToAll requires input chunk (m, g) at rank (n, h) to be sent to index (n, h) of the output buffer at rank (m, g) for all 0 ≤ n, m < N and 0 ≤ g, h < G.

The default implementation of AllToAll in PyTorch sends each chunk independently using `ncclSends` and `ncclRecvs`. This requires (N − 1) × G IB send messages with very small sizes for each rank. This is prohibitively expensive for all but large input sizes, where the collective will be bandwidth constrained.

**Two-Step AllToAll Algorithm.** Figure 1a shows the MSCCL program for this algorithm. The basic idea behind the algorithm, as shown in Figure 1b, is to route an input chunk (n, g) at rank (m, i) to a scratch buffer at rank (m, g) at location (n, i). Then, transfer the G contiguous chunks (n, i) for all i using a single IB transfer from (m, g) to the output at rank (n, g). As shown in Figure 1b, there are N − 1 such IB sends from each rank. Although the total volume of data transferred is the same as NCCL’s AllToAll with MSCCL program, the number of messages are G times less with G times larger message sizes which translates to improvement for MSCCL program due to high latency of IB sends.

**Chunk-oriented program.** MSCCL program in Figure 1a defines this Two-Step AllToAll. The MSCCL DSL is embedded in Python for convenience. The key idea in MSCCL is to specify the collective algorithm with a chunk-oriented program. Such a program specifies how each chunk is routed from their source to their destination. In MSCCL, each chunk is represented by the buffer name, rank, and the index. For instance, at Line 8, c refers to the input chunk at rank (m, i) and index (n, g). This chunk is either routed directly to the output buffer for intra-node transfers at Line 10 or to the scratch buffer at rank (m, g) at Line 12. Finally, Line 15 creates a reference to G contiguous chunks and sends it to the output at rank (n, g) across the IB link at Line 16.
# $\text{N}$: number of nodes

# $\text{G}$: number of GPUs per node

```python
def alltoall(N, G):
    for n in range(N):
        for m in range(N):
            for i in range(G):
                # Coalesced IB send
                c = chunk('input', rank=(m,i), index=(n,g)).assign(c)
                if n == m:
                    chunk('output', rank=(n,g), index=(m,i)).assign(c)
                else:
                    chunk('scratch', rank=(m,g), index=(n,i)).assign(c)
```

Figure 1: Two-Step AllToAll algorithm for efficient inter-node IB transfers

Figure 2: Network topology of an A100 node. 8 GPUs are fully connected to each other through NVLinks to 6 NVSwitches (NVLinks shown for two GPUs). Every pair of GPUs shares a PCIe switch to 2 InfiniBand NICs for communication outside the node.

### Scheduling MSCCL program

Note that the program in Figure 1a only specifies how to route the chunks but not when or by which threadblock. The MSCCL compiler makes these decisions when it compiles the program into an intermediate representation called MSCCL-EF. The MSCCL runtime, running as a single kernel at each GPU, interprets this intermediate representation.

Figure 3 gives an overview of our system stack that lowers MSCCL program into the procedural MSCCL-EF format which precisely schedules the program. Specifically, the compiler lowers the chunk operations of the MSCCL program into instructions the runtime can execute. The compiler schedules the program by allocating threadblocks at each GPU and decides which and in what order these threadblocks execute the program’s instructions. This assignment honors the dependencies in the program. For instance, the IB send from $(m, g)$ to $(n, g)$ happens only after the $G$ intra-node sends that it depends on is finished. Different assignments result in different schedules. Similarly, using more threadblocks can result more parallelism but at the cost of GPU resources. The compiler uses a set of heuristics explained in Section 5 to make these choices.

## 3 MSCCL DSL

The MSCCL DSL is a chunk-oriented dataflow language that enables programmers to write a communication kernel by specifying how chunks are routed through GPUs. The MSCCL compiler automatically extracts parallelism from the dataflow program by scheduling operations onto parallel GPU threadblocks and maps it to procedural code (Section 5).

This abstraction allows programmers to express the parallel behavior of communication without explicitly writing parallel code. It also frees the programmer from explicitly scheduling individual send and receive operations for each GPU, allowing them to focus on the high-level algorithm.

In this section we explain how to write MSCCL programs, focusing on how chunk routing is specified. In Section 5.4 we discuss extensions to our DSL that let the user take control of scheduling decision to optimize their programs for performance.


### 3.1 State

The state of a MSCCL program is defined by a set of chunks and the buffer slots they are stored in. A buffer slot is a unique memory location defined by the triple (buffer, rank, index). By default every rank has three unique buffers: input, output and scratch. By design the input and output buffers have a fixed size according to the collective's interface, while the scratch buffer is unbounded and allocated according to the program.

The input/output buffers are divided by a set of chunks according to the collective's interface. For example, in an AllToAll among $N \times G$ GPUs, every GPU’s input buffer has $N \times G$ chunks. A user may define more chunks for the buffers but the number of chunks still needs to be compatible with what the interface requires. For example, for AllToAll, the buffers can have $2 \times N \times G$ chunks for better routing.

### 3.2 Program

MSCCL programs can be thought of as assigning and reducing chunks between buffer slots that are on different GPUs. Table 1 gives a description of each of the key MSCCL operations.

Chunks are accessed by calling $c1 = \text{chunk} \,(\text{buffer}, \, r1, \, \text{index}, \, \text{size}=1)$ which returns a reference to the chunk(s) stored on GPU $r1$ at specified index1 on the buffer. The buffer can either refer to the input, output, or scratch buffer. If the size is greater than 1, a reference to multiple chunks is returned.

#### Operations

Programmers can manipulate and copy chunks between buffer slots using two operations: assign and reduce. Specifically, $\text{c1.assign(buffer, r2, index2)}$ copies the chunk to GPU $r2$ at the specified buffer and index2, such that both slots contain a copy of the same chunk. If chunk refers to multiple chunks, assign will copy over each chunk starting at index. The assign operation returns a reference to the newly created chunk.

Two chunks can be reduced by calling $\text{c1.reduce(c2)}$ which creates a new chunk representing the reduction of these two chunks, and stores the result in chunk1’s location. For correctness, both chunk1 and chunk2 need to be the same size.

#### Validity

A valid MSCCL program only operates over chunks that exist. If the programmers accesses an uninitialized buffer slot that was never assigned to either at the start of the program or explicitly during the program, the compiler will terminate with an error. Additionally, the compiler will terminate with an error if programmer applies operations to a chunk that has been overwritten. A reduce operation always overwrites its caller with a new reduce chunk, while assign can potentially overwrite slots with a new copy of a chunk.

### 4 MSCCL Runtime

Once MSCCL compiles a program and generates a MSCCL-EF, the MSCCL runtime executes it efficiently. MSCCL runtime uses NCCL’s infrastructure for executing a MSCCL-EF. There are multiple components involved in the runtime which we will discuss in the following sections.

#### 4.1 MSCCL-EF

First, we will discuss MSCCL’s executable file format that MSCCL’s compiler generates and then we will discuss how MSCCL runtime digests a MSCCL-EF.

MSCCL-EF is a data structure as shown in Figure 4 which is stored on GPU memory and executed through an interpreter.

| Operation                                      | Description                                                                 |
|------------------------------------------------|-----------------------------------------------------------------------------|
| chunk(buffer, rank, index, size=1) → c         | Returns a reference to the chunk(s) at buffer slot (buffer, rank, index).   |
| c1.assign(buffer, rank, index) → c2            | Assigns the buffer slot (buffer, rank, index) to c1’s chunk, and returns    |
|                                               | a reference to the chunk at the buffer slot.                                |
| c1.reduce(c2) → c3                             | Reduces the chunks referenced by c1 and c2, creating a new chunk c3, and     |
|                                               | stores it at c1’s buffer location.                                          |

Table 1: MSCCL DSL operations.
written in CUDA. MSCCL-EF has a dedicated set of instructions for each GPU. Each GPU’s instructions are distributed among several threadblocks such that they are executed concurrently.

**Connection assumption.** Each threadblock in MSCCL-EF can make a send connection and a receive connection with at most one GPU. This is an invariant in the entire execution of a MSCCL-EF. In the MSCCL-EF example shown, GPU 0 has two threadblocks: threadblock 0 makes a send connection with GPU 8 and a receive connection with GPU 2, threadblock 1 makes a send connection with GPU 8 and a receive connection with GPU 1. This restriction simplifies the implementation of the MSCCL runtime as threadblocks do not need to synchronize with each other except to honor the dependencies in the MSCCL program.

**Instruction set.** Each threadblock has a linear set of instructions that are executed in-order. As described in previous sections, each MSCCL algorithm is described in terms of chunks and therefore, each MSCCL-EF specifies the number of equal chunks input and output buffers need to be divided by. Instructions are interpreted according to these chunks. Each instruction takes possibly 5 arguments: source buffer and chunk index (used for send instructions), destination buffer and chunk index (used for receive instructions), and count (the number of chunks the instruction uses, by default one). The buffers are possibly input (in), output (out), or scratch (sc) and chunk indices are with respect to number of chunks MSCCL-EF specifies. Below is the full list of instructions:

- `send(buffer,index)/recv(buffer,index)`: sends/receives from the given buffer and the chunk index to/from the remote GPU.
- `reduce(src_buf,src_ind,dst_buf,dst_ind)`: a pre-defined reduction operation is applied on the corresponding chunks and the result is store in the destination location.
- `copy(src_buf,src_ind,dst_buf,dst_ind)`: locally copies a chunk from a source location a destination location.
- `recvReduceCopySend(src_buf,src_ind,dst_buf,dst_ind)`: a fusion of multiple instructions; it receives a chunks, reduces it with source chunk, locally copies it to the destination location and then sends it to the remote GPU. We denote the instruction also by `rrcs`.
- `recvReduceCopy/rrc, recvReduceSend/rrs, recvCopySend/rcs`: are fusions of multiple instructions and their functionality can be interpreted from the name.

In all of these instructions, count is an argument and is assumed to be one. A count greater than one applies the same functionality but on count number of consecutive chunks.

**Cross-threadblock dependence.** Instructions within a threadblock execute sequentially, but instructions across threadblocks can execute out of order. MSCCL-EF can create an explicit order between two cross-threadblock instructions as shown in the example in Figure 4. For example, `recv(sc,0)` on threadblock 0 must occur before `send(sc,0)` on threadblock 1 to ensure that the chunk is fully received before it is sent. Note that one could have used `recvCopySend` instruction in threadblock 0 instead of the two instructions but for scheduling reasons, they may decide not to. Also, a threadblock may not have all the connection it needs due to the connection assumption described above.

### 4.2 Initialization

During the initialization of MSCCL runtime, the given MSCCL-EF is parsed and copied to the GPU memory. The runtime makes all of the connections listed for the threadblocks by using the building blocks of NCCL [16]. NCCL can make a connection between any pair of GPUs and the type of connection is dependent on the placement of the GPUs in the topology. There are three type of connections:

1. **Peer-to-peer:** this connection is made between two GPUs that are directly connected to each other through NVLinks/NVSwitch or PCI express. This is the fastest connection type and is only available within a node.
2. **Shared memory:** when a peer-to-peer connection is not available between two GPUs within a node, host memory is used as a shared buffer to exchange data between the GPUs.
3. **NIC/IB:** for a GPU pair that are across different nodes, the connection is made through a NIC/IB. If RDMA access is supported on the node, then the data transfer only happens through PCIe switches, otherwise it will need to go through host memory.

During initialization when a connection between a pair of GPUs is requested, NCCL goes through the above order of connection types and tries the next type only if the current one fails.

### 4.3 Connection Mechanism

Once a connection is initialized between two GPUs, it can be used during the runtime through a GPU kernel. Figure 5 shows how GPU 0 transfers chunk 1 from input buffer to chunk 0 from the output buffer on GPU 8 where the two are on two different nodes. As shown, threadblock 0 on GPU 0 initiates a send for chunk 1 which transfers data to the NIC’s memory for GPU 0 by the runtime using a simple CUDA `remote[tid]=input[tid]` instruction. The runtime will then use the NIC/IB connection to transfer the data to the other NIC’s remote memory for GPU 8 which is then copied
MSCCL executes a MSCCL-EF through an interpreter written in CUDA. First, the runtime will call the interpreter with as many threadblocks as MSCCL-EF specifies with cooperative kernel launch [7] which ensures that all threadblocks are running simultaneously. Note that MSCCL only compiles programs that use less than the number of streaming multiprocessors (SM) on the GPU, otherwise, the interpreter will fail. Once the kernel is launched, each threadblock will establish the connection specified in the MSCCL-EF.

After the connections are established, the interpreter will examine the input/output buffer sizes and read the number of chunks from MSCCL-EF to identify the number of 4MB tiles that each chunk needs to be divided into. The interpreter has an outermost loop that iterates through these tiles in-order. Inside the loop, the interpreter will read the instructions in the MSCCL-EF for the running threadblock one at a time and execute them by going through a chain of if and else commands to match the instruction type. Therefore, at the end of first iteration of the outermost loop, all the necessary data transfers are completed for the first tile of each chunk. In the next iteration, next tile of each chunk is transferred and so on.

Instructions within a threadblock are executed in the order they are listed in the MSCCL-EF. Before executing an instruction, the interpreter will check if there is a cross threadblock dependence and enforces an order in case there is. This enforcement is done through a spin-lock on a shared GPU memory location. Each threadblock has a dedicated GPU memory location for the spin-lock which is updated with the instruction number of the MSCCL-EF it is currently executing only when it satisfies a dependence. For example in Figure 4, only the first instructions of both threadblocks satisfy a dependence and as it can be seen, it is due to the chunks they are accessing (read after write accesses).

5 MSCCL Compiler

The steps the MSCCL compiler takes are summarized in Figure 6.

The MSCCL primitives in Table 1 implement a tracing frontend that records a directed acyclic graph (DAG) of operations on chunks, which we call the Chunk DAG. This is further lowered through an Instruction DAG into procedural code targeting the low-level MSCCL-EF language of our runtime. We first explain the tracing and lowering mechanisms that are essential to generating correct code, and then discuss optimizations that occur during the lowering.

5.1 Tracing

The MSCCL program is traced to build the Chunk DAG, which captures the global view of chunk movement in the
program. The graph is initialized with nodes to represent all chunks available in the input buffer as start nodes. The assign and reduce operations in Table 1 create new nodes recording the operation and its dependencies, and return references to the new node in the Chunk DAG. Each node in the Chunk DAG records:

- The operation of the node; reduce, assign, or a special start operation for the roots of the DAG.

- The edges capture the true dependences from chunk movements as well as false dependences from reusing a buffer slot.

The Chunk DAG in Figure 6 is the result of tracing a subset of the AllToAll program in Figure 1a. Operation dependencies are naturally captured when building the Chunk DAG and it exposes all the potential parallelism in the program.

### 5.2 Lowering

**Instruction generation.** The lowering of Chunk DAG happens in two steps: first into a Instruction DAG and then into a MSCCL-EF made up of instructions (see Section 4.1). Nodes in the Chunk DAG represents chunk operations which typically involves two different ranks. During instruction generation, we expand each chunk operation node into two rank instruction nodes (or a single instruction when the operation is local).

A chunk operation expands differently depending on whether it is local (ranks are the same) or remote (ranks are different). When an assign operation is a remote operation, it is expanded into a send and a receive instructions. Also when a reduce operation is remote, it is expanded into a send and a receiveReduceCopy instruction (see Section 4.1 for details of these instructions). For local operations only a single instruction is generated: a copy instruction for assign operation and a reduce instruction for a reduce operation.

When an operation is expanded into two instructions, they are connected by a communication edge, representing the dependency between two ranks where one rank sends a chunk to another. The original edges of the Chunk DAG are preserved as processing edges, representing the dependency within a rank when it needs to process one chunk before another.

Figure 6 shows the result of expanding the AllToAll Chunk DAG into an Instruction DAG.

**Threadblock assignment.** Each instruction in MSCCL-EF is assigned to a threadblock that will execute it. This assignment must at a minimum respect the rules that each threadblock can have at most one peer for receiving from and another for sending to (see the connection assumption in Section 4.1). Additionally for correctness, the assignment must not introduce deadlocks, which are possible due to the sequential execution order of instructions within a threadblock.

We have designed an automated routine to assign instructions to threadblocks, which employs two scheduling heuristics to minimize execution time. The high level steps of the routine are as follows:

1. **Create threadblocks:** scan through all instructions per GPU and create r threadblocks for every unique (send-peer, receive-peer) pair, so that every instruction maps to one threadblock. The multiple r is a hyperparameter that is set by the number of instances (see Section 5.3.2).

2. **Calculate dependency depth:** the number of hops a chunk must traverse is used to prioritize instructions that are likely to be enabled earlier.

3. **Calculate reverse dependency depth:** instructions that contribute to a chunk that has more hops remaining are prioritized.

4. **Sort instructions** into a global topological order with respect to their dependencies with a heap to prioritize nodes with a lower dependency depth first and a higher reverse dependency depth second.
5. **Assign instructions to threadblocks:** instructions are processed one by one in the topological order and assigned to their matching threadblock. If an instruction has multiple candidates (e.g., local copies can happen on any threadblock) then the one whose latest assigned instruction is earliest in the sorted order is chosen.

The sorting priorities calculated in steps 2 and 3 implement a heuristic that attempts to schedule operations in the order they will be enabled. This heuristic makes the rough assumption that number of hops equals time. Exploring more sophisticated cost models is left for future work.

Absence of deadlocks is guaranteed by scheduling instructions in a global topological order, which takes both send-receive and memory dependencies into account. Since instructions are appended into threadblocks, each of them will conform to the global topological order and thus the implicit dependencies introduced by their sequential executions cannot produce cycles.

As an alternative to automatic threadblock assignment, we describe ways for users to specify assignments manually in Section 5.4.

**Synchronization insertion.** Instructions have two kinds of dependencies: ones between a send and a receive, and ones due to repeated use of the same buffer slots (processing dependencies in Figure 6). While sends and receives implicitly synchronize, the second kind of dependencies may need additional synchronization.

Instructions within a threadblock are executed sequentially, and thus any dependencies between them are already satisfied and are filtered out. As MSCCL-EF supports synchronizing with up to one dependent instruction in another threadblock per instruction, any instructions with multiple dependencies remaining are split into a sequence of nop instructions containing the extra dependencies followed by the main instruction.

**5.3 Optimizations**

**5.3.1 Instruction Combining.**

The lowering from the Chunk DAG into instructions uses a subset of the available ones that doesn’t include the fused variants that combine a receive and a send (see Section 4.1). We have designed three peephole optimization passes that insert these fused instructions as appropriate. These passes execute right after instruction generation, before threadblock assignment.

**rcs** Rewrites a back-to-back receive and send on the same buffer slot into a fused receiveCopySend. For example, the following instructions:

- `recv(buffer, index)`
- `send(buffer, index)`

Would be rewritten into:

```
recvCopySend(buffer, index)
```

The rewrite is applied only if there is only the one send directly dependent on the receive. While it would be sound to select one in the case of multiple sends for the rewrite, this could delay the execution of the other sends.

**rrcs** A back-to-back pair of a receiveReduceCopy and a send instruction are rewritten into a receiveReduceCopySend. Like the previous optimization, this is only applied when the send is the only instruction depending on the receiveReduceCopy instruction.

**rrs** As a special case of the previous optimization, if the send also has only one dependent instruction, namely a paired receive on another rank, then the copy to local memory is unnecessary. In these cases a receiveReduceSend instruction can be used instead.

**5.3.2 Instances.**

An important aspect for performance of MSCCL programs is the amount of parallelism used for transfers. For example, our experience has shown that a single threadblock in an NVIDIA A100 GPU is not capable of saturating the bandwidth of an outgoing NVLink. This makes it often beneficial to break up a transfer into multiple smaller parallel transfers. While it is possible to rewrite the source MSCCL program to increase the number of chunks — thus making them smaller — and use more parallelism, it is somewhat cumbersome.

We have designed a general purpose procedure to replicate a program into multiple parallel instances. Given a program and a desired number of instances \( r \), the number of chunks in the collective is multiplied by \( r \). For each chunk \( c_i \) in the original program, chunks \( c_i, c_{i+1}, \ldots, c_{i+r-1} \) represent their subdivisions, occupying the same ranges in memory and following the same routing. All operations are similarly replicated, which increases the available parallelism by a factor of \( r \). During lowering, the automatic threadblock assignment routine will take advantage of the parallelism to place these operations onto separate threadblocks.

One subtlety that needs to be handled is that the new instances of the program are not necessarily fully independent when operations involve ranges of multiple contiguous chunks. Consider the following instructions:

```
1 chunk(0, 'a', 0, size=2).assign(1, 'b', 0)
2 chunk(1, 'b', 0, size=1).assign(2, 'c', 0)
```

With \( r = 2 \) these would effectively be turned into:

```
1 chunk(0, 'a', 0, size=2).assign(1, 'b', 0)
2 chunk(0, 'b', 0, size=2).assign(1, 'b', 0)
3 chunk(1, 'b', 0, size=1).assign(2, 'c', 0)
4 chunk(1, 'b', 1, size=1).assign(2, 'c', 1)
```
While the operations on lines 3 and 4 belong to separate instances, they are both dependent on the send on line 1, but not on the one on line 2. Due to this, the instances feature will redo dependency tracking after creating the new chunks and operations.

What value to choose for \( r \) is not obvious and we leave this as a hyperparameter for the user to control.

5.4 MSCCL Extensions

In this section we describe two extensions to MSCCL, both of which give the user control over how instructions are placed into threadblocks. Section 6 discusses how these extensions are used in our case studies.

Manual Threadblock Assignment For situations where the automatic threadblock assignment described in Section 5.2\(^1\), we allow users to specify threadblocks manually. This is accomplished with two additional optional parameters that can be given to the \texttt{assign} and \texttt{reduce} operations in Table 1:

\begin{verbatim}
c.assign(rank, buf, idx, sendtb, recvtb)
c.reduce(c2, sendtb, recvtb)
\end{verbatim}

The values given here directly replace the threadblocks indices that automatic assignment would infer. If these arguments are used in any operation, then they must currently be used in every operation, since MSCCL currently doesn’t support doing partial automatic threadblock assignment.

Channel Directives As an alternative to full manual thread-block assignment, we allow users to specify the channel the operation must be performed on. Since no two threadblocks on the same GPU with the same send or receive peer can use the same channel, this allows forcing operations to not be scheduled sequentially. These channel directives are respected by the automatic threadblock assignment when it considers candidate threadblocks. The channel are again specified with additional optional parameters:

\begin{verbatim}
c.assign(rank, buf, idx, ch)
c.reduce(c2, ch)
\end{verbatim}

We have used channel directives to ensure parallel sends over Infiniband while automatic threadblock assignment was sufficient for the rest of the program.

6 Evaluation

MSCCL is designed to allow programmers to quickly develop custom communication collectives and explore different scheduling strategies. To demonstrate the programmability of MSCCL, we use it to optimize two production scenarios: a single node inferencing scenario and a large-scale distributed training scenario. In both cases, we demonstrate the improvement of AllReduce and AllToAll respectively, and evaluate the end to end speedup these improvements for these scenarios. To additionally demonstrate the expressivity of MSCCL, we use MSCCL to optimize hierarchical AllReduce as well as build a novel collective we call AllToNext and its potential use case in optimizing pipeline parallelism.

All our algorithms required less than 30 lines of MSCCL code and took between 15 minutes to an hour to write, debug, and manually optimize.

Experimental Setup We tested our MSCCL generated programs on a cluster of NVIDIA A100 GPUs. GPUs are organized in a hierarchical fashion using heterogenous network links. Figure 2 shows the topology of a single node which contains 8 A100 GPUs and 6 NVSwitches. Each GPU is connected by 12 third-generation NVLinks to NVSwitches for a total of 600 GB/s bi-directional bandwidth. For communication outside the node, each pair of GPUs share a single PCIe Switch which connects to 2 HDR InfiniBand NICs, each running at 25 GB/s bandwidth. Depending on the collective, we use between 1 and 32 nodes. All experimental results are averaged over 50 iterations after a warmup period of 20 iterations.

Baselines When applicable, we compare our collectives against implementations provided by NCCL 2.8.4-1 [16]. This implementation uses the input buffer size to select among different algorithms for each collective [1].

6.1 Multi-Node AllToAll for Training

AllToAll is a MPI collective that transposes a buffer of data between GPUs such that chunk \( i \) on GPU \( j \) ends up on GPU \( i \) at index \( j \). Because each GPU exchanges data with every other GPU, AllToAll is a very communication intensive collective. In this section we analyze our two-step AllToAll algorithm described in Section 2 and Figure 1a. For this program, we used MSCCL’s default schedule with only 1 instance.

We compare the performance of our two-step AllToAll algorithm against two baselines: a handwritten CUDA implementation of the two-step algorithm and NCCL’s implementation running on 8, 16, and 32 A100 nodes. The handwritten two-step algorithm uses the same pattern of sends and receives as the MSCCL program by directly calling the send and receive primitives exposed by NCCL. Figure 7 plots the algorithmic bandwidth of our two baselines and the MSCCL AllToAll for a range of buffer sizes. We also compute the theoretical algorithmic bandwidth one can hope to achieve for AllToAll. If there \( N \) nodes, each GPU has to send \( (N - 1)/N \) of its input data across other nodes. Since there are as many IB links as there are GPUs per node, an AllToAll can achieve a maximum bandwidth of \( IB_{bw} \cdot N/(N - 1) \), where \( IB_{bw} \) is the theoretical bandwidth of each IB link.
Performance against handwritten. Despite implementing the same algorithm, the MSCCL version is significantly faster. For large buffer sizes (about 256MB or larger), MSCCL’s algorithmic bandwidth is up to 35% better on 32 nodes. The MSCCL implementation is superior because of scheduling decisions made by the MSCCL compiler that divides communication across multiple parallel threadblocks. Besides, the handwritten implementation needs CUDA synchronization and extra memory copy between the two steps to fit interface provided by NCCL primitives, while MSCCL could pipeline those steps well. The handwritten kernel required about 70 lines of code, including an explicit copy kernel that copied chunks from input to scratch buffer necessary for arranging chunks for the contiguous IB send. The MSCCL implementation does not differentiate between moving chunks between GPUs or within a GPU because it is seamlessly handled by the compiler and runtime, making our implementation more succinct.

Performance against NCCL. For large sizes our algorithm outperforms NCCL’s implementation and improves algorithmic bandwidth by 20%. For large buffer sizes (about 128MB or larger), the MSCCL implementation approaches the theoretical algorithmic bandwidth for the different number of nodes we ran on, shown as the red line in the figures.

6.2 Single-node AllReduce for Inferencing

This scenario involves serving a multi-billion parameter state-of-the-art language model on a node with 8 A100 GPUs. This scenario uses model parallelism to reduce the end-to-end user latency, and as such AllReduce is a key performance bottleneck. This workload used AllReduce on input buffer sizes ranging from 300KB to 20 MB. We optimized MSCCL algorithm for these buffer sizes.

6.2.1 Ring AllReduce.

Figure 7: Algorithmic bandwidth of MSCCL AllToAll on 8, 16, and 32 nodes of 8 A100 gpus.

Figure 8a shows our MSCCL Ring AllReduce program. For an AllReduce with r=8 ranks, the input buffer at each rank has r chunks. Each chunk traverses the ring twice starting from the corresponding rank - the first ring for the reduction and the second ring to copy the result to all ranks. Many libraries, including NCCL, implement their own highly optimized Ring AllReduce [16, 22].

MSCCL implementation. In MSCCL, we implemented the Ring AllReduce algorithm (see Figure 8a) and used the manual scheduling interface to explore different schedules and tuned the number of parallel instances needed to achieve good performance.

The best schedule we found divides a single logical ring into 8 threadblocks so that every chunk is processed in its own threadblock. We used MSCCL to automatically replicate our base rings 4 times, such that the algorithm uses 4 times the resources to process smaller chunks taking advantage of the multiple NVLink connections. It uses the LL128 communication protocol which enables, so that it’s primitives have slightly better latency at the expense of lower bandwidth utilization.

Performance Figure 8b, plots the performance of our two AllReduce algorithms against NCCL’s. From the range of 128KB to 32MB our MSCCL ring implementation outperforms NCCL, and is up to 48% at 2MB. Our implementation schedules the base ring among 8 threadblock and 8 channels, which is further parallelized across 4 instances, so that it uses a total of 32 channels and threadblocks for every GPU, while the NCCL implementation uses 24 channels. Forcing NCCL to use more channels resulted in decreased performance, while forcing our schedules to use 24 channels also resulted in lower performance. We found that dividing the base ring among multiple threadblocks, results in noticeable performance even if the amount of threadblocks and channels stays the same. For example, a schedule using 8 threadblocks
def ring_allreduce(R):
    for i in range(R):
        # Chunk i starts at rank i
        c = chunk('input', rank=i, index=i)
        # First ring: compute fully reduced chunk
        for r in range(1,R):
            r = chunk('input', rank=(i+r)%R, index=i)
            c = r.reduce(c, sendtb=i, recvtb=i, ch=i)
        # Second ring: broadcast fully reduced chunk
        for r in range(R-1,2*R-1):
            r = chunk('input', rank=(i+r)%R, index=i)
            c = r.assign(c, sendtb=i, recvtb=i, ch=i)

(a) MSCCL Ring AllReduce program.

(b) Algorithmic bandwidth of MSCCL Ring AllReduces on 8 A100 GPUs.

Figure 9: MSCCL Hierarchical AllReduce on two NDv2 nodes when compared with NCCL.

per ring instantiated 4 times outperforms a schedule using 1 threadblock per ring instantiated 32 times.

For buffer sizes greater than 32MB, our ring implementation’s algorithmic bandwidth levels out around 100 GB/s, which is to be expected because it relies on the LL128 primitives. NCCL performs better for these buffer sizes, but this range lies outside the needs of this specific workload. The ability to quickly prototype and optimize a collective for a specific workload — a range of input sizes on a given topology, is the key strength of MSCCL.

6.3 Hierarchical AllReduce

To show the flexibility of MSCCL we implemented a Hierarchical AllReduce and evaluate it on Azure NDv2 instances which have 8 V100 GPUs per node. Each node is connected with each other using IB. The ring AllReduce over 16 GPUs will make 30 IB traversals. To avoid this, the hierarchical version performs a intra-node ring to reduce all buffers within a node, makes two IB sends to share these buffers across nodes, and finally, each node performs the second ring to broadcast the reduced buffer. The MSCCL program is less than 30 lines of code and we elide it for space constraints. Figure 9 shows the performance improvement over NCCL.

6.4 AllToNext

The final case study we present is a collective to accelerate pipeline communication. In this collective involving N GPUs, where GPU $i$ sends a buffer of data to GPU $i+1$, with the last GPU sending nothing. This communication pattern exists in applications that process data in a pipelined fashion across multiple GPUs.

Similar to AllToAll, communication within a node utilize high bandwidth NVLinks while communication across node utilize InfiniBand, making cross node communication the bottleneck. If a single send is used only one of the eight available IB connections is utilized.

We used MSCCL to address this bottleneck with a custom collective called AllToNext. The key idea of AllToNext is to utilize all IB links in the node by using all GPUs within a node to cooperatively send data to the next GPU on another node so that all IB links are utilized. Because of our topology where pairs of GPU share two IB links via a single PCIe switch, one gpu in the node cannot utilize all the cross-node links. Figure 10 describes how AllToNext operates over a simplified 2-node pipeline of 6 GPUs, and a parameterized MSCCL program that implements it.

**Performance.** We used MSCCL to generate an AllToNext implementation operating over three nodes made up of 24
1. \texttt{def alltonext(N, G)}
2. \texttt{for n in range(N): # N nodes}
3. \texttt{for g in range(G): # G GPUs per node}
4. \texttt{if g != G-1: # direct intra-node send}
5. \texttt{c = chunk('input', rank=(n,g), index=0, sz=G)}
6. \texttt{chunk('output', rank=(n,g+1), index=0).assign(c)}
7. \texttt{continue}
8. \texttt{# last rank does not send anything}
9. \texttt{if n == N-1: continue}
10. \texttt{# use G IB links by routing through scatter/gather buffers}
11. \texttt{for i in range(G):}
12. \texttt{c = chunk('input', rank=(n,g), index=i)}
13. \texttt{if i == 0:}
14. \texttt{c = chunk('scratch', rank=(n,0), index=0).assign(c)}
15. \texttt{c = chunk('output', rank=(n+1,0), index=0).assign(c)}
16. \texttt{elif i == G-1:}
17. \texttt{c = chunk('scratch', rank=(n+1,i), index=i).assign(c)}
18. \texttt{c = chunk('output', rank=(n+1,0), index=i).assign(c)}
19. \texttt{else:}
20. \texttt{c = chunk('scratch', rank=(n,i), index=0).assign(c)}
21. \texttt{c = chunk('scratch', rank=(n+1,i), index=1).assign(c)}
22. \texttt{c = chunk('output', rank=(n+1,b), index=1).assign(c)}

(a) SCCLang AllToNext program parameterized for different number of nodes and local GPUs.

(b) Chunk routes for GPU 2 showing the cross-node send (lines 12-23) of AllToNext on 2 nodes of 3 local GPUs. Sends over NVLink are shown in blue, while sends over IB are shown in red.

Figure 10: AllToNext

7 Related Work

The message passing interface (MPI) [8] is a popular abstraction for communication primitives. Efficient algorithms for implementing these primitives is a long-studied research area [5, 18, 24], including optimized algorithms for specific architectures like mesh, hypercube, or fat-tree [2, 3, 20] and for clusters of shared-memory processors [19, 23, 25, 26]. Motivated by recent ML workloads, Horovod [21] implements collective primitives by using NCCL locally in node and MPI across nodes. Others such as BlueConnect [6] and PLink [15] exploit the hierarchical network topology of a cloud system or a data center to improve the performance of collective primitives. Recent work focuses on automatically generating new collective algorithms, either by packing trees [27] or using a constraint solver to generate pareto-optimal algorithms [4]. In contrast, this work focuses on a high-level language for specifying these algorithms and efficiently running them on state-of-the-art accelerators. Our hypothesis is that MSCCL will make it easy to not only generate new algorithms for MPI abstractions specialized to a particular topology and/or input sizes, but also specifying custom collectives, like AllToNext studied in this paper.

The chunk-oriented programming style of MSCCL is motivated by dataflow programming languages. The design of the language is particularly influenced by declarative coordination languages such as Linda [9] and Concurrent Collections [11]. Rather than use explicit tuples, MSCCL uses implicit chunk identifiers to coordinate multiple ranks. Cilk [13] also influenced the aspect of MSCCL where the deterministic semantics of the program is specified by the sequential semantics of the host language (Python for MSCCL and C/C++ for Cilk).

Recent works [10, 12, 17, 28] have shown the advantage of overlapping computation and communication when opti-
mizing distributed ML workloads. While our focus here is on specifying communication collectives, extending SCCLang to further specify the scheduling of computation is an interesting future work.

8 Conclusion

MSCCL is a declarative language embedded in Python for quickly prototyping and optimizing communication kernels. We have used MSCCL to generate efficient communication kernels for two production scenarios. To demonstrate the flexibility of MSCCL, the paper generates custom kernels for collectives not part of the standard MPI interface. We believe that this additional programmability will enable researchers to explore new collectives to optimize their ML workloads.

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