Electrostatically Doped Heterojunction TFET with Enhanced Driving Capabilities for Low Power Applications

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Abstract—This paper projects the enhanced drive current of a n-type electrostatically doped (ED) tunnel field-effect transistor (ED-TFET) based on heterojunction and band-gap engineering via TCAD 2-D device simulations. The homojunction ED-TFET device utilizes the electrostatic doping in order to create the source/drain region on an intrinsic silicon nanowire that also facilitates dynamic re-configurability. The ED-TFET offers good electrostatic control over the channel with reduced thermal budget and process complexity. However, device exhibits low ON current, therefore, in this work, we elaborate on interfacing of group III-V with group IV semiconductors for heterojunction. Incorporation of heterojunction and band gap engineering in the ED-TFET has improved drive current even at very low operating voltage. The comparison of various low band gap source region materials shows that germanium (Ge) source (Si-Si-Ge) ED-TFET provides steepest subthreshold swing (SS) of about 9.5 mV/dec, and higher ON-state drive current of 1.58 mA at \( V_{DS} = 1 \) V and 0.093 mA at \( V_{DS} = 0.5 \) V with same SS.

Keywords—Tunnel field effect transistor (TFETs), band-to-band tunneling (BTBT), electrostatic doping, heterojunction, band gap engineering, TCAD.

I. INTRODUCTION

Continuous downscaling of CMOS technology has significantly improved the performance, functionality, and packaging density, at the cost of rise in power dissipation and complex fabrication process of nanoscale CMOS devices. The rise in power dissipation is due to faster switching activities and subthreshold leakage. In this pursuit, small subthreshold swing SS (sub-KT/q) devices have acquired wider attention due to their efficient switching and very low subthreshold leakage. Among the emerging sub-KT/q devices, tunnel field-effect transistors (TFETs) have considered as the potential devices on account of their low SS, low leakage current and integration compatibility with CMOS process [1]–[3]. However, TFETs have comparatively low ON-state current as compared to their counterpart MOSFET devices due to poor band-to-band tunneling phenomenon (BTBT). The efficient tunneling in TFETs requires abruptly doped junctions which enforce complex fabrication process with high thermal budget requirements due to ion-implantation and thermal annealing techniques. Apart from steep doping requirements, these junctions restrain aggressive scaling and enhanced random dopant fluctuations (RDFs), as a result, these devices become susceptible to process variations related issues [4].

Therefore, before considering the potential merits of TFETs, issues related to steep doping requirements at drain/source junctions, process variability and complex fabrication process need to be addressed. In this line, an electrostatically doped (ED) TFET was proposed that attempted to address the aforementioned issues [5]. The ED-TFET employs an intrinsic silicon nanowire for the formation of a drain (D) – channel – source (S) structure without externally doped S/D regions. For making the \( p^+ \) and \( n^+ \) S/D regions, the polarity gate (PG) concept was employed in which appropriate bias at polarity gates were applied, as a result, desired level and type of carriers can be induced. This process of inducing carriers in an intrinsic silicon nanowire is referred as electrostatic doping [6]. The ED eliminates requirements of external doping, thereby yields, low thermal budget and simplified fabrication process. Further, intrinsic nature of silicon nanowire provides less susceptibility towards process parameter and temperature variations [5]. However, ED-TFET faces an inherent problem of poor ON current which makes it less suitable for main stream VLSI circuit applications.

The poor ON current issue of TFETs has been addressed through many ways in literature, such as, employing germanium (Ge) channel [7], strained silicon [8], and group III-V channel and heterojunction structure [9], [10]. Apart from that band gap engineering has also been explored for the selection of materials at drain and source sides for optimal drive current as well as \( I_{ON}/I_{OFF} \) ratio. Recently, many successful attempts have been made in order to fabricate such devices with hetero-junctions through epitaxial growth with vertical interface (or vertical hetero-structures) [12], [13]. Although all these approaches have yielded enhanced ON current in TFETs, yet the cost, fabrication complexity, and process variations issues still need to be addressed.

In this paper, poor ON current issue of the ED-TFET is explored through hetero-junction and band-gap engineering, while retaining it’s inherent merits of reduced thermal budget requirements, fabrication complexity, and less susceptibility to process variation. For ON current enhancement of this ED-TFET, we have explored interfacing of semiconductor materials (group III-V and group IV) with different combinations employing band gap engineering at source-channel as well as at drain-channel junctions. From the simulation results, it is confirmed that the combination of group III-V and group IV and also group IV (Si-Ge) materials for hetero source-channel interface may exhibit higher ON current as well as low OFF current.

II. DEVICE STRUCTURE AND SIMULATION PARAMETERS

Fig. 1 show the cross-sectional view of a silicon nanowire based ED-TFET structure [5]. In this device structure, drain (D) – channel – source (S) regions have been marked with three different materials, later combination of these materials for different regions have been optimized for enhanced ON current, low OFF current, and other performance parameters. The simulation parameters considered are as follows [5]: ultrathin silicon film thickness \( (t_{Si}) = 10 \) nm, equivalent oxide thickness (EOT) = 0.8 nm, channel length \( (L_g) = 50 \) nm, spacing between gate and source electrode \( L_{Gap,S} = 3 \) nm, and spacing between gate and drain electrode \( L_{Gap,D} = 15 \) nm. The metal control gate work function, \( WFE_{CG} \) of 4.5 eV of ED-TFET has been optimized to 4.3 eV. \( WFE_{CG}=4.3 \) eV causes a depletion...

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The interfacing of low and high band gap materials (group III-V and group IV semiconductor materials) results in heterojunctions in the ED-TFET; therefore, the ED-TFET has junction between two semiconductors instead of metallurgical junctions in conventional TFETs. The materials for drain–channel and source – channel heterojunctions were chosen according to their band gaps for higher ON current and low OFF current. The low band gap materials, such as Germanium (Ge), Silicon-Germanium (Si$_{0.3}$Ge$_{0.7}$), and Gallium Antimonide (GaSb) can be employed for source region, whereas, Indium Phosphide (InP) can be used as a high band gap material for drain and channel region.

The ED-TFET device is simulated using a 2-D device simulator, Atlas Silvaco V5.19.20 [14]. A nonlocal band-to-band tunneling model is used for the simulation of tunnel current. This inter band tunneling current in the TFET depends on the potential profile along the entire path connected by tunneling. Therefore, nonlocal models uses Wentzel-Kramer-Brillouin approximation method for estimating the tunneling probability along the tunneling path. The results are obtained through drift-diffusion current transport model where the poisson and carrier continuity equations are solved self consistently. Concentration dependent Shockley-Read-Hall (SRH) generation and recombination model is incorporated for transitions that occur in the presence of traps or defects. The tunneling model was first calibrated by reproducing the results reported in [16] in order to avoid the use of default parameters of the model for Ge. The fitted coefficients $A = 1.53 \times 10^{22} \text{cm}^{-3} \text{s}^{-1}$ and $B = 1.38 \times 10^{8} \text{V cm}^{-1}$ were used throughout in our simulation work.

### III. Band diagrams and Device Characteristics

Fig.2 (a) and (b) show the simulated carrier concentration of induced electrons and holes in the ED-TFETs with for different source materials (silicon and germanium) under OFF-state and ON-state along a horizontal cut-line at 1 nm below the Si/SiO$_2$ interface. The profile of both holes and electrons induced through electrostatic doping (i.e. appropriate PGs biases $V_{P2,1}=1.2$ V and $V_{P2,2}=1.2$ V), is similar with respect to conventionally doped TFETs except a sudden drop at nickel-silicide S/D contacts. It can be inferred that the induced carrier concentration is higher in case of germanium source ED-TFET due to low work function of Ge. In OFF state ($V_{CG}=0V$), the intrinsic channel under the control gate is depleted due to sufficient work function differences between metal (4.3 eV) and semiconductor, and therefore, causes almost no current. While under ON-state ($V_{CG}=1.2V$), intrinsic region under the control gate becomes $n^+$ having electron concentration of the order of $10^{19}$ cm$^{-3}$ and the device works on flat-band condition with almost zero resistance. This ensures formation of an abrupt n-p junction at source-channel interface necessary for tunneling of carriers from valence band (VB) of source to conduction band (CB) of channel.

Fig.2(a) and (b) show the valance band (VB) and conduction band (CB) energies of Si as well as Ge source ED-TFETs in OFF state as well as in the ON state. In OFF state, it can be seen that tunneling probability of electron from VB of source to CB of channel is low due to higher energy barrier width at source-channel junction of Si source ED-TFET in comparison with Ge source ED-TFET. Comparatively less tunneling width of Ge source ED-TFET is due to the low band gap of germanium with respect to Si which results in significant BTBT tunneling in OFF state also and hence higher OFF-state current. On application of positive gate bias (ON state), the CB and VB in the channel region gets aligned with CB and VB of drain region, causes the further reduction in tunneling width in case of Ge source ED-TFET, and thereby, increases the probability of electrons tunneling from VB of source to CB of channel. Therefore, Ge source ED-TFET has maximum number of overlapping energy states for both OFF and ON states, hence, higher current in both states as compared to Si ED-TFET.

In Fig.3 (a) and (b) show the transfer characteristics of ED-TFET with interfacing of semiconductor materials (group III-V and group IV) along with band gap engineering employed for heterojunctions at source-channel as well as at drain-channel junction with 4.5 eV control gate work function. From Fig.3 (a), one can observed that the ON current of ED-TFETs is increasing with the incorporation of low band gap materials like Germanium (Ge), Silicon-Germanium (Si$_{0.3}$Ge$_{0.7}$), and Gallium Antimonide (GaSb) as a source region material. The smaller source band-gap enables enhanced band-to-band tunneling rate, and therefore, high ON current but at the expense of large OFF current in comparison with silicon source. Amongst all low band gap materials in the source region, germanium offers high ON current with significantly low OFF current.

In Fig.3 (b), we have further optimized the ON and OFF state currents of ED-TFET with germanium source region by employing combinations of group III-V and IV materials (high band gap) to realize hetero drain-channel junction. Influence of large band gap materials than silicon (1.12 eV) like Indium Phosphide (1.35 eV) as drain and channel material is clearly visible on the device performance. Incorporation of high band gap materials in channel as well as in drain region helps in reduction of carrier recombination rate and in turn low $I_{OFF}$. In spite of that, it also results in an increase in energy barrier width at the drain and channel interface due to the increase in energy difference between conduction band edge of channel and valence band edge of drain which further decreases the reverse current, as a result, reduced ambipolar behavior.

Fig.5(a) show the comparison of transfer characteristics of ED-TFET with low band gap germanium source along with that of high band gap InP drain-channel region. It is confirmed that the ED-TFET

![Energy band diagrams](image-url)
Ge material to be a best low band gap source material having superior performance for TFETs based on Ge source have also revealed the potentiality of TFET with significant performance being the preferred hetero ED-TFET. Hence Si-Si-Ge ED-TFET has paramount boost in performance characteristics yet confirmed the potential benefit of incorporation of low and high band gap materials at drain as well as channel region, and (b) output characteristics of germanium source ED-TFET. Fig. 6 (a) shows the output characteristics of ED-TFET with (a) high band gap materials in drain and channel region in place of InP and GaAs at drain as well as channel region, and (b) output characteristics of germanium source ED-TFET with gate voltage variations at fixed $V_{DS} = 1V$.

Table-I shows the comparison of performance characteristics of heterojunction ED-TFETs, comprised of low band gap material (Ge) in source region and high band gap material (InP) in drain and channel regions. It can be seen that hetero ED-TFETs has superior performance in comparison with homo silicon ED-TFET. Therefore it confirmed the potential benefit of incorporation of low and high band gap materials along with interfacing of group III-V and IV materials for enhancing the performance of tunnel-FETs. Although InP-InP-Ge ED-TFET has paramount boost in performance characteristics yet the possible fabrication is need to be addressed. Hence Si-Si-Ge ED-TFET with significant performance is the preferred hetero ED-TFET in terms of reduced fabrication complexity. The experimental studies of TFETs based on Ge source have also revealed the potentiality of Ge material to be a best low band gap source material having superior performance at low operating voltages [16]. Further, Ge having small lattice mismatch (4%) with silicon in comparison with other low band gap materials, yields better interfacing with silicon [17]. The Si-Si-Ge ED-TFET outperforms when comparing the simulation results from the table with some recently developed hetero TFETs i.e., vertical InAs:Si nanowire heterojunction tunnel transistors ($I_{ON} \sim 2.4 \mu A$) [18] and $p^+ SiGe:Si$; $n^+ Si$ hetero TFET ($I_{ON} \sim 0.42 mA$) [19].

Fig. 7 (a) and (b) show the performance optimization of Si-Si-Ge ED-TFET comparing with Si-Si ED-TFET. Fig. 7 (a) show the $I_{ON}/I_{OFF}$ ratio and point SS with variation in control gate work function for both the devices. The optimum value of control gate work function is 4.3 eV at which both devices have better performance. Fig. 7 (b) show the $I_{ON}/I_{OFF}$ ratio and point SS of Si-Si-Ge ED-TFET with variation in thickness of germanium material in source region. It can be seen that both parameters are increasing as we decreases the thickness of germanium in source region. The thin epilayer of germanium is easier to fabricate and interface with silicon through direct epitaxy method [17]. Hence the optimum value of germanium thickness can be taken as 6 nm with less degradation in these parameters. This further added an advantage in having simpler fabrication process with lower manufacturing cost.

Fig. 7 (a) shows the transfer characteristics of silicon and germanium source ED-TFETs. Amongst all the low band gap materials, germanium ensures higher ON current of 1.58 mA with point SS of 9.5 mV/dec and $I_{ON}/I_{OFF}$ ratio $\sim 10^{13}$ in comparison with 0.0048 mA ON current, point SS of 7.5 mV/dec and $I_{ON}/I_{OFF}$ ratio $\sim 10^{15}$ of Si ED-TFET at 4.3 eV control gate work function. Fig. 7 (b) shows the output characteristics of ED-TFET with germanium source (Si-Si-Ge) for different values of $V_{GS}$. It can be inferred that in triode region as the drain voltage $V_{DS}$ increases the tunneling of carriers increases, and hence, $I_{ON}$ also increases. This establishes an exponential relationship with $I_{DS}$ due to drain induced barrier thinning [5]. With further increase in $V_{DS}$, the tunneling width becomes less reliant on it, hence, causes the saturation of the drain current. The output characteristic of (Si-Si-Ge) ED-TFET exhibits more exponential $I_{DS}-V_{DS}$ relationship, and thereby more linearity in the operation.

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\begin{array}{|c|c|c|}
\hline
\text{Parameters} & \text{Si-Si-Si} & \text{Si-Si-Ge} & \text{InP-InP-Ge} \\
\hline
I_{ON} \text{ mA}/\mu m & 0.0029 & 1.58 & 7 \\
\hline
I_{OFF} \text{ A}/\mu m & 7.00 \times 10^{-25} & 8.00 \times 10^{-10} & 7.47 \times 10^{-10} \\
\hline
\text{Point SS} \text{ mV/dec} & 10.1 & 9.5 & 8.5 \\
\hline
\end{array}
\]
ceptibility to process variations makes ED-TFET a potential device for its suitability for such applications, therefore, heterojunctions based source enables its potentiality for RF applications.

is evident that as gate bias increases from subthreshold to saturation the limiting value of \( g_m \) and unity gain frequency \( f_T \) have also improved for Ge source ED-TFET as compared to its counterpart Si source ED-TFET.

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