Comparisons of Soft Decision Decoding Algorithms Based LDPC Wireless Communication System

Yasmeen M. Hussein1, Ammar H. Mutlag 2, Basman M. Al-Nedawe3
1 & 2 Middle Technical University, Electrical Engineering Technical College, Baghdad, Iraq
3 Middle Technical University, Technical Institute of Baquba, Diyala, Iraq

Abstract. The Low Density Parity Check (LDPC) forward error correction code provides significant results that have been very close to Shannon limit. This paper compares the Bit Error Rate (BER) performance of soft decision decoding algorithms of LDPC codes on AWGN channel. Devising soft decision decoding algorithms which are good in BER performance requires a comparison of probabilistic, log domain and Min-Sum methods. Simulations are conducted with different parameters using MATLAB workspace to evaluate the LDPC system performance. Results have shown that Min-Sum has outperformed the algorithms of Log Domain and Prob. Domain with a considerable amount of the Signal to Noise Ratio (SNR). Finally, the optimal LDPC parameter values have been selected based on the achieved results which provide superior results.

1. Introduction

The communication device transmits data by a channel or transmitted media, like the wired or wireless, from source to the transmitter. The reliability of the data that has been obtained, is dependent upon the channel, as well as the external noise of the channel. This noise causes signal interference and errors in transmitted data. Based on the coding theorem, Shannon has shown that only in the case where the data rate has been less than that of the channel capacity can effective transmission be achieved. This theorem has shown that, as the length of the code goes to infinity, a set of the rate codes less than the capacity of the channel has the capability [1]. The detection and correction of the errors may be accomplished by adding the redundant symbols to original data referred to as the error correction and correction codes (ECCs). Without the ECCs data required to re-transmit in the case where it could detect an error in received data, the ECC has been referred to as the Forward Error Correction (FEC). Retransmission adds delay, expense and waste to the throughput of the device. For the long distance one-way communications like deep space or satellite communications [2], the ECCs are quite helpful. They have wireless networking apps and storage devices as well.

The Low Density Parity Check (LDPC) has been considered one of the most significant FEC forms. Gallager who is the first suggested these codes in 1962 [3]. Due to hardware complexity at the time, they were ignored for more than thirty years. It gained prominence, however, after MacKay and Neal formally re-introduced it in 1997[4]. It was shown that when designed optimally, LDPC codes can perform quite similarly to the Shannon Limit [5]. Any linear block code through its parity-check matrix can be represented. If this matrix is sparse, it only contains a small number of 1st per column or row, and the code is called a low-density parity-check code.

The LDPC codes recently attracted considerable research attention due to the reduced complexity of the implementation, higher efficiency of the Bit Error Rate (BER) at a lower value of the SNR and inherent code structure, supporting a high parallelism level. In the
applications of the high data rate like the WLAN Wi-Max, Digital Video Broadcasting (DVB-S2) and next-generation (5 G) applications [6] of the latest generation, LDPC codes have now become of increasing popularity and have been adopted. Many research studies on LDPC codes have been important. Researchers in [7] proposed decoding of the modified LDPC using the modulation of the Binary Phase Shift Keying (BPSK) that has been useful in optical fiber communications. Following the simulation, they have discovered that at 0.5 SNR, they had a BER near zero. Furthermore, in [8] the proposed standard masking matrix was introduced for Quasi-Cyclic LDPC (QC-LDPC) codes with a girth of a minimum of six. Then the irregular codes are built with the use of an enhanced finite field approach and the Progressive Edge-Growth (PEG) method, resulting in large girth and fewer short cycles. Simulations indicate that in the proposed codes, the lower error floor as well as the good waterfall performance have been found. In addition, the author in [9] used LDPC codes to enhance the knowledge hiding operation. Finally, in [10], the researcher identified the implementation of a common and embedded decoder to test the decoder. This hardware / software implementation technique gave the maximum flexibility for the hardware-based simulator framework to be improved and rapidly prototyped.

The purpose of this paper is to analyze the actions of an LDPC code-based on soft decision decoder communication mechanism represented by the Prob. Domain, Log Domain and Min-Sum Algorithms (MSA). These algorithms are used to display the potential of every one of the forms with a different number of the block length values (N), a number of 1s for each one of the columns (Wc), and iterations. The differences between all decoders will be observed in terms of the BER, complexity and delay time, to pick the best of them.

2. Low Density Parity Check (LDPC) Code

The LDPC code has been assumed with a matrix of the parity check $H = [H_{MxN}]$ has been viewed as an LDPC code, containing several 0s and only a limited amount of the 1s. The matrix of the parity search $H$ has N columns and M rows. Only regular LDPC codes have been considered. The regular LDPC codes’ characteristics are that every one of the columns has a constant "1" number (i.e. weight of the column) Every one of the rows has a constant "1" number (i.e. weight of the row), although every one of the rows has a constant "1" number (i.e. the weight of the row). The weight of the column is often not the same as the line weight. The code of the LDPC has been defined by the code of the LDPC (N, y, k), where N represents the repeated, utilize a different code-word term length, and j, k represents the LDPC code column and the weight of the row, respectively [11]. The LDPC code rate is $\frac{1-y}{k} = 1-\frac{M}{N}$. The regular, parity-check matrix of 8-bit code length is defined by

$$H = \begin{bmatrix} v_1 & v_2 & \cdots & v_x \\ 0 & 1 & 0 & 1 & 0 & 0 & 1 & 1 \\ 1 & 1 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 & 1 & 0 \end{bmatrix},$$

,where $x = 1, 2, \ldots N$ and $y = 1, 2, \ldots M$

Another $H$ matrix representation can be seen as the Tanner graph consists of check nodes sets and variable nodes that correspond to each $H$ matrix row and column, respectively, as shown in Figure 1 [12].
2.1. Encoder
The encoder utilizes the generator matrix for encoding information bits to producing code-word. Parity check matrix and generator are considered to be inter-related. With regards to standard form, parity check matrix will be provided as follows [13]:

\[ H = [A|I_{n-k}] \]  \hspace{1cm} (1)

and generator matrix is:

\[ G = [I_k|A^T] \]  \hspace{1cm} (2)

A codeword \( C \) will be generated as follows:

\[ C = UG. \]  \hspace{1cm} (3)

In which \( U \) represent block related to the information bits and \( G \) represent the generator matrix. Valid code-word should be verified as follows:

\[ HC^T = 0. \]  \hspace{1cm} (4)

where \((.)^T\) represents the transpose matrix. In the case when the result in (4) is non-zero, then \( C \) will be invalid, also the error correction procedure will be utilized in such condition.

2.2. Decoder
The decoder of parity check is iterative included two main categories, hard and soft decisions. The message-passing algorithm of the soft decision also known Sum-Product Algorithm (SPA) where the input of each received bit is represented by the probability of prior information received from the channel. Depending on the message structure between variable nodes and check nodes, SPA can be classified into: Probability Domain, Log Domain and Min-Sum SPA.

2.2.1. Prob. Domain
This algorithm applies real values of the likelihood in iterative planning to messages between the check nodes and the variable nodes. The following steps define the procedure [14].

Step 1: Messages from the variable nodes for checking nodes indicated as \( q_{x,y} \) will be initialized to probability \((p_1^0 \text{ and } p_1^1)\) values with the use of (5) and (6). This is achieved once for decoding of each received codeword

\[ q_{x,y}^1 = p_1^1 = \frac{1}{1 + e^{-2y_x/\sigma^2}} \]  \hspace{1cm} (5)

\[ q_{x,y}^0 = 1 - p_1^1 \]  \hspace{1cm} (6)
Where

\( p_i^0\) and \( p_i^1\) : The probabilities of codeword from the AWGN channel.

\( \sigma \) : The noise variance \((\sigma^2 = N_0/2)\).

\( q_{x,y} \) : Gathering of information from check nodes to corresponding variable nodes.

Step 2: Messages will be evaluated (variable node process) from the check nodes to the variable nodes [14].

\[
\bar{r}_{y,x}^0 = \frac{1}{2} \left[ 1 + \prod_{x' \in \text{row}[y]/[x]} (q_{x',y}^0 - q_{x',y}^1) \right]
\]

Step 3: Messages from the bit nodes for checking nodes will be determined (check node process).

\[
q_{y,x}^0 = \alpha_{x,y} p_i^0 \prod_{y' \in \text{col}[x]/[y]} \bar{r}_{y',x}^0
\]

\[
q_{y,x}^1 = \alpha_{x,y} p_i^1 \prod_{y' \in \text{col}[x]/[y]} \bar{r}_{y',x}^1
\]

Step 4: The extrinsic probability values of decoder output bits are computed and the hard decision is made according to \( Q_x \) value [14].

\[
Q_x^0 = \alpha_x \prod_{y \in \text{col}[x]} \bar{r}_{y,x}^0
\]

\[
Q_x^1 = \alpha_x \prod_{y \in \text{col}[x]} \bar{r}_{y,x}^1
\]

\[
\hat{C}_x = \begin{cases} 
1 & \text{if } Q_x^1 > 0.5 \\
0 & \text{Otherwise}
\end{cases}
\]

Step 5: Syndrome check.

\[
\hat{C}_i \times H^T = \delta
\]
If \( \hat{S} \) is a zero vector this indicates received code word will be correctly decoded. Or else, the decoding will continue through repeating the algorithm beginning from Step2 until arrived to the maximum number of iterations.

2.2.2. Log Domain.

With the exception of using log-likelihood ratios (LLR) instead of real probability, this algorithm is close to the probability domain in its calculation. Which is why, rather than \( q_{x,y} \) values \( L(q_{x,y}) \) values are utilized, which are computed as \( \pm \log \frac{q_{x,y}^k}{q_{x,y}^g} \). As same as \( r_{x,y} \) values replaced with \( L(r_{x,y}) \) \( \pm \log \frac{r_{x,y}^k}{r_{x,y}^g} \). Its process has described by the following steps [15].

**Step1**: Messages from the variable nodes for checking nodes indicated as \( L(q_{x,y}) \) will be initialized to LLR \( L(p_x) \) values with the use of (5) and (6). This is achieved once for decoding of each received codeword.

\[
L(p_x) = \log \frac{p_x^0}{p_x^1} = \frac{2}{\sigma^2} y_x
\]

\[
L(p_x) = L(q_{x,y})
\]

Where

\( y_x \) : The received data with AWGN.

**Step 2**: Messages to variable nodes from the check nodes will be computed as LLR (process of variable nodes).

\[
L(r_{y,x}) = 2 \tan^{-1} \left( \prod_{x' \in \text{row}[y]} \tanh \left( \frac{L(q_{x',y})}{2} \right) \right)
\]

Where

\( x' \in \text{row}[y] \) indicates indices \( x' \) \( (1 \leq x' \leq n) \) of all bits in \( y \) \( (1 \leq y \leq m) \) that have value one.

**Step3**: Messages from bit nodes for checking nodes will be estimated as LLR (check node process).

\[
L(q_{x,y}) = L(p_x) + \sum_{y' \in \text{col}[x]} L(r_{y,x})
\]

**Step4**: Extrinsic LLR values regarding decoder output bits have been estimated and the hard decision is made according to \( Q_x \) value [15].

\[
L(Q_x) = L(p_x) + \sum_{y' \in \text{col}[x]} L(r_{y,x})
\]

\[
\hat{c}_x = \begin{cases} 
1 & \text{if } Q_x^1 > 0.5 \\
0 & \text{Otherwise}
\end{cases}
\]
Step 5: Syndrome check.

\[ \hat{c}_x \times H^T = \hat{S} \]  

(19)

If \( \hat{S} \) is a zero vector this indicates received code word is correctly decoded. Or else, decoding will continue through algorithm starting from Step 2 until it arrived at the maximum number of iterations.

2.2.3. Min-Sum SPA

It is the most simplified decoding algorithms. To reduce the computational complexity in (21) of Log Domain step 2 it will modify as followed [16]:

\[ L(r_{y,x}) = \prod_{x' \in \text{raw}[y]} \text{sign}(L(q_{x',y})) \min(|L(q_{x',y})|) \]  

(20)

However, comparing to SPA decoder, the MSA decoder achieves higher BER. Thus, in terms of differentiated LDPC decoding, there is a trade-off between the efficiency and the complexity.

3. Design of the System

The LDPC architecture includes primarily 4 key blocks, transmitting random bits and then transmitting them via the AWGN channel and after that through the LDPC Decoder. Obtaining the performance of the simulation using MATLAB version 2019a work space as shown in Figure 2.

![Figure 2. The block diagram of system module.](image)

First, the source-generated binary bits are encoded with LDPC code to be transmitted with different (block length per frame, number of iterations per column (Wc) and number of iterations). The encoder receives a message which is represented by a number of the bits that need to be transmitted with a 250-bit length; the message will be multiplied by H matrix for the production of encoded message (i.e. code-word) with 500 bits length due to the code rate is set to 1/2. BPSK is used as a modulation technique for avoiding the distortions which are related to the binary ASK. The SNR ranges between -4 and 8 dB. Depending on the environment of the communication device, the channel will add a sound. In this study, the Additive White Gaussian Noise (AWGN) channel was considered with such a 0 mean and power spectral density relative to N0/2. The signal \( r_k \) obtained will be interpreted by:

\[ r_k = S_k + n_k \]  

(21)

Where

\( S_k \) : is transmitted signal
\( n_k \) : is AWGN channel.

The received signal \( r_k \) will enter to the decoder. The decoder is a means of interpreting and converting coded information through one of the decoding methods into a comprehensible
form. Three forms of soft decision decoders are used in this study, namely Prob. Domain, Log Domain and MSA. The most significant device module parameters are mentioned in table 1.

**Table 1.** The parameter of the system module.

| System parameters                    | Value                                                                 |
|---------------------------------------|----------------------------------------------------------------------|
| **Decoded methods of LDPC**           | Prob. Domain, Log Domain and MSA product                            |
| **Channel**                           | AWGN with N0/2                                                        |
| **Modulation**                        | BPSK                                                                 |
| **Number of bit per Column (Wc)**     | 3, 5, 9                                                              |
| **Number of iteration**               | 3: 2: 9                                                              |
| **Block length (No. of bit in frame)**| 150:100:450                                                           |
| **Number of information bit**         | 250                                                                  |

The simulation model can be represented by the flow chart.

```
Start

N = 400, M = 200, one PerCpl (W_{C}), N, iter

Create LDPC Matrix (H_{MXN})

Generate Random Data (Message)

Encoding Message Using LDPC

BPSK Modulation

AWGN Channel

NO

I <= No. of iteration

yes

Decoder Process

§ = 0

yes

Stop

```
4. Results and Discussion

To demonstrate the LDPC system instead of performance. The results are given in terms of the BER as a function of SNR. In this paper, three LDPC decoding algorithms with an SNR range from -4 to 8 dB are used. Different parameters are varied in all simulations, such as N from 150:100:450, Wc from 3:2:9 and iteration from 3:2:9.

First, to investigate the impact of increasing of iteration for each of the decoder types, a variety of iteration numbers from 3:2:9 are added with N and Wc values equal to 250 and 3, respectively. Performance of Prob. Domain, Log Domain, and MSA are explained in Figures 4, 5 and 6.
Figures 4, 5 and 6 indicated that the increase of the iterations would enhance the efficiency of the BER. However, with little improvement in the performance of the SNR, it will also increase the delay. Note, Prob. Domain, Log Domain and MSA achieve $10^{-4}$ BER for iteration 5 approximately at the same SNR, so that iteration 5 can be categorized with acceptable delay also as best iteration.

Next, to demonstrate the impact of the increase in the $W_c$ for every decoder with $N$ equal to 250, $W_c$ ranges from 3 to 9, iteration is 5, which is chosen from the previous section as the best iteration. The decoding efficiency of Prob. Domain, Log Domain and MSA is illustrated in figures 7, 8 and 9, respectively.

Figure 6. LDPC code performance using MSA.

Figure 7. LDPC code performance using the algorithm of Prob. Domain.
Figure 8. LDPC code performance using the algorithm of Log Domain.

Figure 9. LDPC code performance using MSA.

Show the result optimal BER is accomplished when \( W_c \) equals 3. In contrast, the worst BER is accomplished when \( W_c \) equals 9, which indicates that performance deterioration in the BER of LDPC for those algorithms will be induced when the number of 1s per column is increased. This is because the short cycles in the parity check matrix are formed. The Min-Sum have outperformed the algorithms of Log Domain and Prob. Domain with a considerable amount of the Signal to Noise Ratio (SNR).

Finally, from the two previous parts, \( W_c \) equals 3, iteration is 5; however, \( N \) ranges between 150 and 450; all 3 decoder types are implemented with the optimal parameters to illustrate the impact of the increase in the length of the block for every one of the decoder types. Figures 10, 11 and 12 clarify the results of Prob. Domain, Log Domain, and MSA.
It is quite clear from Figures 10, 11 and 12 that the increase in a block length enhances the efficiency of the proposed algorithm which is, predicated on Shannon’s theorem that when we
have sent accurately coded data via a noisy channel of communication, which has utilized the long block length values at rates that are lower than the channel power, the likelihood of error will reach 0. Therefore, the increase in the code length results in a low error likelihood.

It can be noted from previous results that when using Prob. Domain, Log Domain and MSA, the results indicate that similar performance is demonstrated. In comparison, they were increasing Log Domain, Prob. Domain and MSA iterations results in more delay time and higher complexity. However, the results would be more sufficient so that good results, delay, and complexity can be trade-offed.

5. Conclusion
In this paper, an LDPC code communication system with three types of soft decision decoders (Prob. Domain, Log Domain and MSA) is simulated to extract the AWGN channel performance. We used the LDPC Log Domain, Prob. Domain and MSA product System parameters and Value Decoded methods, with AWGN Channel of N0/2, Modulation BPSK, Number of bit per column (Wc) 3:9, Number of iteration 3: 2:7, Block length (Number of bit in frame) :150:100:550, Number of bit information 250. In our simulations, the results show that when the amount of iterations is increased, the performance of those algorithms are improved, there has been a disadvantage for increasing amount of iterations for decoding methods, the time of the decoding will increase. The BER performance of the LDPC is increased as well when the code's length is increased. The behaviors of Log Domain, Prob. domain and MSA algorithms are incredibly for the same block length. An additional important factor is that when the performance of the one per column is increased, the BER gets worse due to the structure of short cycles within the confirmation matrix and the difficulty of integrating those cycles.

References
[1] Ryan, William E., et al. "Optimal code rates for the Lorentzian channel: Shannon codes and LDPC codes." IEEE transactions on magnetics 40.6 (2004): 3559-3565.
[2] Moon, Todd K. Error correction coding: mathematical methods and algorithms. John Wiley & Sons, 2005.
[3] R. G. Gallager, “Low Density Parity Check Codes”, Number 21 in Research monograph series. MI Press, Cambridge, Mass, 1963.
[4] Kasai, Kenta, and Kohichi Sakaniwa. "Spatially-coupled MacKay-Neal codes and Hsu-anastasopoulos codes." IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences 94.11 (2011): 2161-2168.
[5] Mo, Elisa, and Pooi Yuen Kam. "Log-likelihood ratios for LDPC codes with pilot-symbol-assisted BPSK transmission over the noncoherent channel." 2009 IEEE Wireless Communications and Networking Conference. IEEE, 2009.
[6] Kadhim, Mohammed Aboud, and Mahmood Farhan Mosleh. "Design and implementation of mobile wimax baseband transceiver for different channel estimation algorithms." Journal of Engineering and Sustainable Development 18.1 (2014): 103-115.
[7] Hagenauer, Joachim, Elke Offer, and Lutz Papke. "Iterative decoding of binary block and convolutional codes." IEEE Transactions on information theory 42.2 (1996): 429-445.
[8] Parihar, Bhavinee U., and Y. A. Nafde. "Modified decoding algorithm of Low density parity check code using BPSK modulation." International Journal of Advanced Information Science and Technology 16.16 (2013).
[9] Zhao, Yunlong, Yi Fang, and Zhaojie Yang. "Interleaver design for small-coupling-length spatially coupled protograph LDPC-coded BICM systems over wireless fading channels." IEEE Access 8 (2020): 33500-33510.
[10] Mosleh, Mahmood F., Fadhil S. Hasan, and Ruaa M. Azeez. "Comparison between Different Decoding Algorithms for Low Density Parity Check." 2019 4th Scientific International Conference Najaf (SICN). IEEE, 2019.
[11] Roberts, Michaelraj Kingston, and Ramesh Jayabal. "A modified normalized Min-Sum decoding algorithm for irregular LDPC codes." International Journal of Engineering and Technology 5.6 (2014).
[12] Chaibi, Hasna. "Serial Genetic Algorithm Decoder for Low Density Parity Check Codes." International Journal of Communications, Network and System Sciences 8.09 (2015): 358.
[13] Kumar, A.: FPGE implementation of LDPC codes. PhD Thesis. National Institute of Technology, Rourkela (2013)
[14] Liu, Jingjing. Novel LDPC coding and decoding strategies: design, analysis, and algorithms. Diss. University of York, 2012.
[15] Nurellari, E.: LDPC coded OFDM and its application to DVB-T2, DVB-S2 and IEEE 802.16 e. PhD Thesis. Eastern Mediterranean University (EMU) (2012)
[16] L. Pepe, “FPGA Implementation Of An LDPC Decoder And Decoding Algorithm Performance,” Msc Thesis, University of Illinois at Chicago, 2013.