2D materials are promising to overcome the scaling limit of Si field-effect transistors (FETs). However, the insulator/2D channel interface severely degrades the performance of 2D FETs, and the origin of the degradation remains largely unexplored. Here, the full energy spectra of the interface state densities ($D_{it}$) are presented for both $n$- and $p$-MoS$_2$ FETs, based on the comprehensive and systematic studies, i.e., full range of channel thickness and various gate stack structures with $h$-BN as well as high-$k$ oxides. For $n$-MoS$_2$, $D_{it}$ around the mid-gap is drastically reduced to $5 \times 10^{11}$ cm$^{-2}$ eV$^{-1}$ for the heterostructure FET with $h$-BN from $5 \times 10^{12}$ cm$^{-2}$ eV$^{-1}$ for the high-$k$ top-gate. On the other hand, $D_{it}$ remains high, $\approx 10^{13}$ cm$^{-2}$ eV$^{-1}$, even for the heterostructure FET for $p$-MoS$_2$. The systematic study elucidates that the strain induced externally through the substrate surface roughness and high-$k$ deposition process is the origin for the interface degradation on conduction band side, while sulfur-vacancy-induced defect states dominate the interface degradation on valence band side. The present understanding of the interface properties provides the key to further improving the performance of 2D FETs.

1. Introduction

The electric field effect that enables modulation of the carrier density in a semiconductor channel is at the heart of the transistor. The gate controllability represented by the subthreshold swing (S.S.), that is, gate-voltage change needed to induce a drain-current change of one order of magnitude, is critical to achieve energy-efficient logic devices.\[3] Therefore, for Si metal-oxide-semiconductor field-effect transistors (MOSFETs), many dedicated researchers have developed interface analysis methods based on capacitance–voltage (C–V) measurements and have studied the SiO$_2$/Si interface properties in great detail such that they have become reliable and widely accepted.\[2–11] Here, the recent demonstration of a natural thin-body MoS$_2$ FET with an effective channel length of $\approx 3.9$ nm has facilitated research on 2D layered channels due to overcoming the scaling limit of $\approx 5$ nm for Si gate length.\[12] Although the dangling-bond-free surface of the layered channel is expected to ideally provide an electrically inert interface, there are many reports on the wide range of interface state densities ($D_{it}$) from $10^{11}$ to $10^{13}$ eV$^{-1}$ cm$^{-2}$ for high-$k$ top-gate $n$-MoS$_2$ FET in reality,\[13–30] which must be reduced to improve the device performance. To date, several physical origins for $D_{it}$ have been proposed, which are summarized in Figure 1a.

First, trap (I) represents the defects and impurities in the $n$-MoS$_2$ channel. Sulfur vacancies ($V_S$) with the high density of $\approx 10^{13}$ cm$^{-2}$ are widely recognized in mechanically exfoliated (ME) and chemically vapor deposited (CVD) MoS$_2$.\[31–37] Since physical vapor deposited MoS$_2$ dominantly includes antisite defects,\[33] the present study only focus on $V_S$ in ME and CVD MoS$_2$. $V_S$ introduces defects states in the bandgap, as shown in Figure 1b, which has been evaluated by density functional theory (DFT). CB and VB refer to the conduction and valence bands, respectively. Second, trap (II) represents the traps in the high-$k$ insulator. In general, the back SiO$_2$ oxide is formed by thermal oxidation by atomic layer deposition (ALD) at a relatively low temperature with well-controlled quality, which usually shows an extremely low trap site density inside ($\approx 10^{10}$ cm$^{-2}$). On the other hand, the top high-$k$ oxide is typically formed on the inert MoS$_2$ surface by atomic layer deposition (ALD) at a relatively low temperature with the aid of a buffer layer, which may introduce many traps inside. The traps close to the interface serve as quick traps while the traps inside the oxide serve as slow traps, as discussed in several reports.\[24,28,38] Third, trap (III) represents the strain in MoS$_2$ induced externally. One of the interesting properties of 2D materials is that they can be scaled down to atomic thickness. Strain is easily induced in a thin MoS$_2$ channel by both substrate surface roughness and/or the high-$k$ deposition process, resulting in Mo–S bond bending.\[35–37,39] Since the conduction and valence bands of MoS$_2$ are mainly composed of the energy splitting of the Mo $d$ orbital,\[40,41] the band tail states will be easily introduced, as schematically illustrated in Figure 1b. Although $V_S$ introduces lattice disorder strain around $V_S$ in the ideally flat MoS$_2$ layer, this strain has already been incorporated in the DFT calculation and is regarded as the origin in trap (I). The macroscopic strain introduced externally in the MoS$_2$ layer is considered here in trap (III).
The high-k/MoS2 interface properties are inherently complex because $D_n$ includes one or more types of traps and some origins might be related to each other. Most of the previous studies only focus on one specific gate stack with limited channel thickness ($t_{ch}$) for n-type MoS2. Therefore, a common understanding of the origin for the interface states has not yet been obtained. Although the energy distribution of $D_n$ is critical to reveal its origin from the comparison with the DFT calculation, a recent study indicated that the conventional C–V method for the $D_n$–energy relation developed for Si systems cannot be simply applied to the FET structure of 2D channels because the channel charging process due to the high channel resistance is more dominant than the electron capture/emission process by the interface trap.[25] In this study, in order to obtain the energy distribution of $D_n$, we performed the modeling of $I_D$–$V_{TG}$ characteristics[25,26] by considering the MoS2 channel carrier statistics through the quantum capacitance ($C_Q$) and its transport through the Drude model.[42] Based on the systematic investigation of over 100 devices for both n- and p- MoS2 with a wide thickness range of 1 layer (L) to bulk and various gate stack structures including a 2D heterostructure with h-BN as well as typical high-k top gate structure, the whole picture of high-k/MoS2 interface is discussed.

2. Results and Discussion

2.1. Interface States of MoS2 on the Conduction Band Side

A natural n-type MoS2 crystal was first studied, whose thin flakes were prepared by mechanical exfoliation. Figure 2a shows a schematic drawing of (i) the top-gate MoS2 FET on insulating quartz or SiO2/Si substrates. The quartz substrate with a surface roughness similar to SiO2 was used because the parasitic capacitance can be neglected. The typical drain/source current ($I_{DS}$)–top-gate voltage ($V_{TG}$) characteristics for 1L MoS2 can be found in Figure 2c. The two-terminal field-effect mobility ($\mu_{FE}$) are extracted to be $6.2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ under the conditions where the contribution of $C_Q$ is neglected and $C_{ox}$ for the $Y_2O_3$ buffer layer (1 nm) and the ALD-Al2O3 (10 nm) is estimated as $80 \text{ m}^2 \text{ V}^{-1} \text{ s}^{-1}$ at the accumulation in C–V. The hysteresis is relatively small. S.S. extracted at the current range of $10^{-12}$ to $10^{-10}$ A is mainly discussed in this paper and can be expressed as[1,25]

\[
S.S. = \ln 10 \frac{k_BT}{e} \frac{C_{ox} + C_{it}}{C_{ox}}
\]

where $k_B$, $T$, and $e$ are defined as the Boltzmann constant, temperature, and elementary charge, respectively. $C_{ox}$ is the oxide capacitance, and $C_{it}$ is the interface states capacitance ($C_{it} = e^2D_{it}$). S.S. is a simple and effective parameter to directly evaluate $D_{it}$ from 1L to bulk MoS2 with $t_{ch}$ << maximum depletion width ($W_{DM} = 48–55 \text{ nm}$).[25] $C_Q$ or depletion capacitance ($C_{D}$) decreases exponentially with the energy. At the deep subthreshold region, $C_Q(C_D) << C_p$, which make them negligible. This relation can be clearly seen in Figure S4b (Supporting Information).

Figure 2d summarizes S.S. as a function of $t_{ch}$ for a top-gate MoS2 FET on the quartz substrate. 1L MoS2 typically has a high S.S. level ($>230 \text{ mV dec}^{-1}$) with a large variation. $D_{it}$ is estimated to be $8 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. By increasing $t_{ch}$ over 20 nm, S.S. can be reduced as low as $80 \text{ mV dec}^{-1}$ with small variation, which corresponds to a $D_{it}$ of $9 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. The top-gate fabrication process is the same in principle from 1L to bulk, which means that trap (II), traps in the oxide, is unlikely the dominant origin for $D_{it}$ dependence. Instead, trap (I), the defects in MoS2, and/or trap (III), the strain in MoS2 induced externally, are the main origins for the high $D_{it}$ of atomically thin MoS2. In particular, as for trap (III), it mainly comes from the Mo–S bond bending. Therefore, the thick bulk MoS2 is robust to this effect, which accounts for the smaller S.S. with increasing the MoS2 thickness.

To clarify the importance of trap (III) and achieve low $D_{it}$ even for the 1L MoS2 channel toward the ultimately scaled device applications, the MoS2/h-BN/graphite heterostructure FET was prepared as shown schematically by (ii) in Figure 2a. The optical
image is also shown in Figure 2b. The details of the transfer process with negligible bubbles is explained in Figure S1 (Supporting Information).

The utilization of back-gate graphite can help with increasing $C_{ox}$ (0.23 $\mu$F cm$^{-2}$ with dielectric constant of 2.5 for h-BN) comparable to that for the high-k top gate by reducing the h-BN thickness to 9.5 nm, since the atomically flat surface of h-BN is guaranteed by the total thickness of graphite and h-BN (> 20 nm) (Figure S1, Supporting Information). Thus, S.S. for the 2D heterostructure FET can be compared with those for the high-k/MoS$_2$ FETs. Moreover, no high-k deposition is conducted on the MoS$_2$ channel to avoid any strain, which indicates that two origins for trap (III), that is, substrate surface roughness and high-k deposition, have been suppressed in the present 2D heterostructure FETs. The corresponding $I_{DS}$–back-gate voltage ($V_{BG}$) characteristics at room temperature (RT) in Figure 2c clearly show the improvement of S.S. ($\approx$75 mV dec$^{-1}$) with negligible hysteresis $\Delta V_{hys}$ = 7.3 mV, where the corresponding $D_{hi}$ is $\approx$4 × 10$^{11}$ cm$^{-2}$ eV$^{-1}$. The $\mu_{FE}$ values for two probe (2P) and four probe (4P) measurements are comparable ($\approx$70 cm$^2$ V$^{-1}$ s$^{-1}$) due to an ohmic contact by Ni (Figure S2, Supporting Information). More than 10 2D heterostructure FET devices were fabricated and showed smaller variation compared with high-k top-gate FET devices, as shown in Figure 2d. Since 1L MoS$_2$ flakes are ME from the same natural MoS$_2$ crystals for both high-k top gate and 2D heterostructure FETs, trap (I) is unlikely the main origin for the considerably low $D_{hi}$. Instead, the low $D_{hi}$ is most likely from the suppression of trap (III), which is achieved by forming the atomically flat surface and avoiding the high-k deposition process.

A nearly ideal MoS$_2$/h-BN interface is obtained by the 2D heterostructure formation. Here, it is interesting to reveal how the interface is degraded during the high-k deposition. Therefore, a 1-nm-thick Y$_2$O$_3$ buffer layer, 30-nm-thick ALD-Al$_2$O$_3$ and Al top-gate metal were sequentially deposited on a newly prepared 1L MoS$_2$ heterostructure FET device, as schematically shown by (iii) in Figure 2a. The degradation of S.S. by the top-gate deposition was monitored through the back interface by the back-gate sweep, as shown in Figure 3a. In this device, $C_{ox}$ of h-BN with the thickness of 8.1 nm is 0.27 $\mu$F cm$^{-2}$ and the thickness of graphite is 29 nm. S.S. = 70 mV dec$^{-1}$ before the top-gate deposition increases to $\approx$105 mV dec$^{-1}$ after the Y buffer layer deposition and finally to $\approx$130 mV dec$^{-1}$ after the subsequent ALD-Al$_2$O$_3$ process. The corresponding $D_{hi}$ values are $\approx$3.4 × 10$^{11}$, $\approx$1.3 × 10$^{12}$, and $\approx$1.9 × 10$^{12}$ cm$^{-2}$ eV$^{-1}$, respectively. The hysteresis also increases to 0.14 V. However, when S.S. was measured again before the Al top-gate deposition, S.S. unintentionally improved to $\approx$90 mV dec$^{-1}$, as shown in Figure S3 (Supporting Information). This result strongly indicates that the degradation of both $D_{hi}$ and hysteresis originates mainly from the strain induced by the high-k deposition process, not from the defect formation ($V_{JS}$) in MoS$_2$ during the deposition. It should be emphasized that the Y buffer layer is deposited under the Ar pressure of 10$^{-3}$ Pa to entirely suppress the deposition damage in this study.[15,46]

In the case of silicon-on-insulator, the top and back interfaces are still separated even for a 7-nm-thick Si channel.[47] On the other hand, for a 1L MoS$_2$, high-k top-gate deposition...
2.2. Energy Spectra of Interface States of n-MoS2

The interfacial properties discussed above are based on S.S. at the deep subthreshold region, which does not provide a precise energy level for \( D_\text{it} \) in the energy bandgap. Here, \( D_\text{it} \) is extracted as a function of energy from \( I-V \) characteristics\[^{45,46}\] by considering the carrier statistics through \( C_\text{Q} \) and its transport through the Drude model.\[^{42}\] An example of this simulation is shown in Figure S4 (Supporting Information). When the ideal \( I_{DS}-V_{TG} \) curve is calculated using \( C_\text{ox} \) and \( C_\text{Q} \) with a constant \( \mu \) value extracted experimentally, the ideal S.S. of 60 mV \( \text{dec}^{-1} \) can be obtained. The deviation between the ideal and experimental \( I_{DS}-V_{TG} \) can be considered as the contribution of electron traps to the interface states, that is, \( C_\text{it} \). By assuming the energy distribution of \( C_\text{it} \) as a fitting parameter, the energy distribution of \( D_\text{it} \) of n-MoS2 is estimated for high-k/1L-MoS2/SiO2 device with top-gate sweep and 1L-MoS2/h-BN device with back-gate sweep. On the other hand, for high-k/bulk MoS2/quartz, \( D_\text{it} \) is extracted as a function of energy from C–V characteristics by the Terman method.\[^{25}\] The \( D_\text{it} \)-energy distribution is shown in Figure 1c. The present analysis can quantitatively capture the bandtail-shaped \( D_\text{it} \), which cannot be obtained by the simple \( D_\text{e} \) estimation from S.S. Interestingly, the existence of mid-gap states is evident for high-k/1L-MoS2/SiO2 and 1L-MoS2/h-BN cases because a constant S.S. region exists below the current level of \( 10^{-11} \) A, as shown in the inset of Figure 2c. Although the mid-gap states are close to the energy for \( V_\text{S} \), the mid-gap and bandtail states are simultaneously reduced by improving the flatness of the substrate. To further emphasize the substrate flatness instead of \( V_\text{S} \) effect, Figure S5 (Supporting Information) shows that \( D_\text{e} \)-energy distribution for high-k/1L-MoS2/h-BN both from top-gate sweep is smaller than that for high-k/1L-MoS2/SiO2 in the whole measured energy range. It is evident that trap (I) is not the main origin for \( D_\text{it} \) in our devices, even though \( V_\text{S} \) induced defect states have been widely discussed as the origin for the degradation of the electrical properties for MoS2. As discussed in the previous section, the strain induced by high-k deposition is the dominant origin of the degradation. The interesting point here is that \( D_\text{it} \) near the CB edge for 1L-MoS2/h-BN is similar to that for high-k/1L-MoS2/SiO2 despite the lack of high-k deposition, which is much larger than that for high-k/bulk MoS2. This finding suggests that there is still much room for improvement. At present, the way to improve is not clear yet; the origin may not be the same since the CB minimum changes from the K point for a monolayer to the point on the \( K \rightarrow \Gamma \) line for the bulk material.\[^{48,49}\]

2.3. Electron Transport of n-MoS2

Having clarified the interfacial properties, the transport properties related to the interface states were studied through the...
temperature dependence for the high-k/MoS2/h-BN devices. Figure 4a shows the temperature dependence of $I_{DS}$–$V_{BG}$ characteristics before the top-gate deposition. The threshold voltage is shifted positively by lowering the temperatures. This is due to the temperature dependence of $C_Q$ of 1L MoS$_2$, as shown in Figure S4 (Supporting Information), which is further amplified by $D_{it}$. $S.S.$ also decreases by lowering the temperature at the range of 150–300 K. This is understood using Equation (1), which is the common case for a bulk Si MOSFET. However, $S.S.$ values remain almost constant at 50–150 K and start to increase at the temperature below 50 K. This result suggests the transition of the electron transport mechanism, that is, the occurrence of interface-states-related transport, such as nearest neighbor hopping (NNH) and variable range hopping (VRH).[34,50,51] Figure 4b shows $I_{DS}$–$V_{BG}$ characteristics after the top-gate deposition. The threshold voltage shifts positively more substantially by lowering the temperatures, which is due to the increased $D_{it}$. $S.S.$ is still proportional to the temperature at the range of 150–300 K. The solid circles indicate experimental data, while solid lines indicate the fittings. $E_A$, $E_h$ as a function of $I_{DS}$ before and after the top-gate deposition. Figure 4c shows the temperature dependence of $I_{DS}$ at different $V_{DS}$ values for an Al$_2$O$_3$/Y$_2$O$_3$/MoS$_2$/h-BN device. So far, the temperature dependence of $I_{DS}$ for the MoS$_2$ FET is explained by three terms, which are the conduction band transport by thermal activation (TA), and interface-states-related transport by NNH and VRH. Although some papers reported that VRH accounts for the observed temperature dependence of $I_{DS}$,[50,51] we found that NNH gives a reasonable fitting to experimental results at the low temperature, which can be shown by $I_{DS} = I_{TA}^{0} \exp(-E_a/k_BT) + I_{NNH}^{0}\exp(-E_h/k_BT)$, where $I_{TA}^{0}$, $I_{NNH}^{0}$ are pre-factors. $E_A$ and $E_h$ are the band activation energy and hopping energy, respectively.
in the plot of the temperature dependence of S.S. (Figure 4c). Figure 4e shows extracted $E_a$ and $E_h$ values as a function of $I_{DS}$ through the fitting in Figure 4d. $E_a$ and $E_h$ are also included for the devices before the top-gate deposition and after the $Y_2O_3$ deposition. $E_a$ remains almost unchanged before and after the top-gate deposition. This supports that the conduction band transport take place at high temperature. In contrast, $E_h$ decreases just after $Y_2O_3$ deposition and no further reduction is observed after $Al_2O_3$ deposition. The decrease in $E_h$ is due to the increase in $D_{it}$, as schematically shown in Figure 4f, and accounts for NNH transport at low temperatures at the subthreshold region, that is, the region of conductance fluctuation. The reduced $E_h$ after top-gate deposition could make the hopping path sensitive to Coulombic interactions from localized states. This is then supported by the time domain of $I_{DS}$ from another device, which shows a similar conductance fluctuation at 10 K, as shown in the insert of Figure 4b, and accounts for NNH transport at low temperatures at the subthreshold region, that is, the region of conductance fluctuation.

### 2.4. Interface States of MoS_2 on the Valence Band Side

Natural MoS_2 and CVD MoS_2 flakes usually show n-type behavior as discussed above. Although hole transport has been achieved using ionic gating,[55] the substrate dielectric effect[56] or a contact metal design,[57,58] these are either thermally unstable or complicated, which makes the investigation of interfacial properties difficult. Therefore, a niobium (Nb)-doped p-type MoS_2 crystal was studied here, since the substitution of Mo site by Nb (Nb Mo) is thermodynamically stable,[59] and uniformly dispersed in MoS_2 crystal, which has been confirmed by transmission electron microscopy.[60]

Figure 5a compares the Raman spectra of p-MoS_2 and n-MoS_2. Both types of MoS_2 flakes show sharp $E_{2g}$ and $A_{1g}$ peaks and no distinct difference from 1L to the bulk material,[61,62] which indicates that the effect of Nb substitution on the lattice phonon is negligible here. Back-gate p-MoS_2 FETs on the SiO_2/Si substrate were then fabricated by following the same procedure as n-MoS_2, as schematically shown in Figure 5b. Figure 5c shows $I_{DS}$–$V_{BG}$ characteristics of back-gate 4L p-MoS_2/SiO_2 FETs for both 2P and 4P measurements at 50 K. Figure 5d shows $I_{DS}$–$V_{BG}$ characteristics (circles) and fittings (lines) at $V_{DS} = 1 V$ and RT for a 4L p-MoS_2/h-BN/graphite heterostructure FET with the same structure shown in Figure 2a-ii.
hole $\mu_{FE}$ and current on-off ratio are 10.5 cm$^2$ V$^{-1}$ s$^{-1}$ and 10 for the 8-nm-thick $p$-MoS$_2$ and 2.5 cm$^2$ V$^{-1}$ s$^{-1}$ and $\approx 10^3$ for 4-nm-thick $p$-MoS$_2$, respectively. It is consistent with reported hole mobility.[60] Hole $\mu_{FE}$ is further degraded below 1 cm$^2$ V$^{-1}$ s$^{-1}$ for the thinner devices. The off current is dramatically decreased by decreasing $t_{ch}$ because the depletion layer width formed by the gate electrical field becomes close to $t_{ch}$.[25] Therefore, for $t_{ch} > W_{Dm}$, off-current remains high, which indicates the existence of unmodulated layers in thick $p$-MoS$_2$ and $W_{Dm}$ can be assumed as $= 7$ nm.Bulk acceptor impurity concentration ($N_A$), which comes from the substitution of the Mo site by Nb, is extracted from $W_{Dm}$ using the relation of $w_{Dm} = \sqrt{4 \mu_{m, ho} \tau (N_A / n)} / e \tau N_A$, where $n$ is the intrinsic density of states with the value of $\approx 3 \times 10^8$ cm$^{-3}$ and $\varepsilon_{MoS2}$ is the dielectric constant of bulk MoS$_2$ in the direction normal to the basal plane, which is 6.3.[63] The extracted $N_A$ is $= 2 \times 10^{19}$ cm$^{-3}$, which is consistent with previous Hall measurements.[60] In contrast, the natural $n$-MoS$_2$ crystal has bulk donor impurity concentration ($N_D$) of $= 2 \times 10^{17}$ cm$^{-3}$.[25]

There are two important phenomena observed in Nb-doped MoS$_2$ FETs: the $p$-type to $n$-type transition and asymmetry in electron and hole transport. The $p$-type to $n$-type transition can be understood by a surface electron accumulation effect. Recently, it was reported that $V_S$ of $\approx 10^{13}$ cm$^{-2}$ is introduced “at the surface” of bulk MoS$_2$ flake during mechanical exfoliation, and electrons accumulate at the surface.[64] Based on this report, the schematic to explain surface electron accumulation is shown in Figure 5d. For the bulk case, bulk $N_A$ is larger than surface $N_D$. By decreasing $t_{ch}$, the $p$-type bulk properties cannot be preserved when the surface $N_D$ becomes larger than bulk $N_A$. To support this idea, $V_{BG}$ values at the charge neutral point ($V_{CNP}$) are plotted as a function of $t_{ch}$ in Figure 5e. The CNP is defined as the point to change from hole to electron transport in ambipolar behavior (Figure 5c). Experimentally, the carrier density at CNP ($V_{CNP} \times C_{m/A}$) is determined by both the surface donor $N_D$ and bulk acceptor $N_A \times t_{ch}$. Here, $N_D$ ($cm$)$^{-2}$ is assumed as a constant to explain the accumulated electrons at the surface.[64] Therefore, the simple relation of $V_{CNP} \times C_{m/A} = -N_D + N_A t_{ch}$ can be obtained. Figure 5e shows $V_{CNP}$ is proportional to $t_{ch}$, which confirms the validity of this relation. Both $N_D$ and $N_A$ are calculated to be $8.5 \times 10^{12}$ cm$^{-2}$ and $2.7 \times 10^{19}$ cm$^{-3}$, respectively. $N_A$ estimated here is consistent to $N_A$ obtained from $W_{Dm}$. Although $N_D = 2.7 \times 10^{19}$ cm$^{-3}$ is a high doping concentration, it is not high enough to achieve $p$-type transport in 1L MoS$_2$ because $N_A \times 0.65 nm = 1.8 \times 10^{12}$ cm$^{-2}$ is much smaller than $N_D$. As a result, it is the surface doping effect that determines the carrier type at the atomically thin channel.

Another point is the asymmetry between electron and hole transport. Figure 5e shows the on-currents of both electrons and holes ($I_{DS}^{ON}$), which are defined as the current at $V_{BG} = +30$ V for electrons and at $V_{BG} = -30$ V for holes, respectively. Although the accurate definition should be $I_{DS}^{ON}$ at $V = |V_{BG} - V_{CNP}| = 30$ V, simple definition is used here since $V_{CNP}$ is not seen for thick $p$-MoS$_2$. The $I_{DS}^{ON}$ of electrons is relatively stable with respect to $t_{ch}$, while the $I_{DS}^{ON}$ of holes is degraded dramatically with decreasing $t_{ch}$ even if the $V_{CNP}$ shift is considered. For this $I_{DS}^{ON}$ reduction, the metal/$p$-MoS$_2$ contact effect is carefully investigated since the Schottky barrier at the contact might be the possible origin for the observed degraded hole transport. This is a quite important issue, since $D_{ch}$ cannot be simply extracted from $I_{DS}^{ON} - V_C$ if the modulation of the Schottky barrier by $V_C$ dominantly controls the drain current.[65,66] For $n$-MoS$_2$ with a Ni contact, we have already confirmed that the gate controls the high-$k$-$n$-MoS$_2$ interface, not the contact.[25] For $p$-MoS$_2$, the contact effect is discussed as follows.

First, a 4P 4.7 nm-thick $p$-MoS$_2$ FET on a SiO$_2$/Si substrate with Ni contact was fabricated to quantitatively investigate the contact effect. Figure 5f shows conductivity ($\sigma - V_{BG}$ characteristics for both the 2P and 4P measurements at 50 K. In general, the contact property becomes dominant at low temperature, since the thermionic-emission current is drastically reduced and the field emission current becomes dominant. In Figure 5f, it is clear that the discrepancy between $\sigma_{2P}$ and $\sigma_{4P}$ is quite small. This experiment proves that the contacts for both holes and electrons are reasonably transparent because the doping concentration for both $N_D$ and $N_A$ is high enough. Therefore, for the degraded hole transport observed in Figure 5e, the metal/MoS$_2$ contact is not the main origin but an interfacial issue. That is, $D_{ch}$ for $p$-MoS$_2$ can be extracted similarly with $n$-MoS$_2$.

To discuss the origin of $D_{ch}$ for the VB side according to the classification in Figure 1a, 4L-$p$-MoS$_2$/h-BN/graphite heterostructure FETs were fabricated for comparison, as shown in the inset of Figure 5g. The reason to select 4L is that it is almost the thinnest MoS$_2$ to show $p$-type conduction. Indeed, hole transport can still not be observed for 1L-$p$-MoS$_2$ heterostructure with h-BN, even though the S.S. for electrons is comparable with the $n$-MoS$_2$ heterostructure. As shown in Figure 5g, the S.S. for holes $= 590$ mV dec$^{-1}$ with $D_{ch} = 9.1 \times 10^{12}$ cm$^{-2}$ eV$^{-1}$, while it is $= 150$ mV dec$^{-1}$ with $D_{ch} = 1.1 \times 10^{13}$ cm$^{-2}$ eV$^{-1}$ for electrons. Based on the $I_{DS} - V_{BG}$ fitting shown by solid lines in Figure 5g, the energy spectra of $D_{ch}$ for the VB side are summarized in Figure 1c, where $D_{ch}$ for 4L-$p$-MoS$_2$/SiO$_2$/Si FET is also included. Interestingly, 4L-$p$-MoS$_2$ for both SiO$_2$/Si and h-BN/graphite substrates show almost equivalent energy spectra for $D_{ch}$ with a considerably high level over $10^{13}$ cm$^{-2}$ eV$^{-1}$ regardless of the substrate flatness. This suggests that both trap (II) and trap (III) are not the main origin because of the lack of high-$k$ deposition and the atomically flat surface of h-BN/graphite. Therefore, trap (I), that is, $V_S$ and/or $Nb_{Mo}$ are the most likely the cases for $p$-MoS$_2$, because the energy levels for both $V_S$ and $Nb_{Mo}$ are very close to the VB maximum,[58] as shown in Figure 1b.

Finally, let us discuss which defect is dominant, $V_S$ or $Nb_{Mo}$. A clue can be observed in Figure 5f as the abnormal conductance peaks at the hole side. Very similar abnormal conductance peaks have been reported even in the hole transport for a 1L “$n$-MoS$_2$” FET with ion gating,[67] where it is suggested to be due to defects states by $V_S$ close to VB. Figure 5e shows that the degradation of $I_{DS}^{ON}$ for holes as a function of $t_{ch}$ has the same tendency as the $V_{CNP}$ shift. Since the $V_{BG}$-$V_{CNP}$ shift has been suggested to be due to sulfur vacancy formation at the surface, the degradation of $I_{DS}^{ON}$ for holes could also have the same origin, that is, $V_S$. The mid-gap $V_S$ state on the CB side is localized, while the shallow $V_S$ state on the VB side is easily hybridized with valence band states, which will become more prominent in disulfur vacancies and even sulfur vacancy clusters.[68] This explains why the sulfur vacancy-induced transport is more prominent on the VB side (conductance peaks in Figure 5f) compared to its transport on the CB side (conductance fluctuation in Figure 4b). Although $Nb_{Mo}$ could also introduce shallow.
defect states on the VB side in p-type MoS$_2$, the density of $V_{i}$ ($\sim 10^{11}$ cm$^{-2}$)$^{[31]}$ is much larger than that of Nb$_{\text{MB}}$ ($\sim 10^{12}$ cm$^{-2}$) in atomically thin MoS$_2$, which indicates that $V_{S}$ could be the dominant origin of the degraded hole transport. To improve the hole transport at the subthreshold region, continued efforts to improve the crystallinity are required.

3. Conclusion

We successfully extracted the full energy spectra of $D_{0}$ from both n- and p-MoS$_2$ FETs. By fabricating the 2D heterostructure FET with h-BN, on the CB side, it is elucidated that the strain induced externally through the high-k deposition process is the dominant origin of the interface degradation which is further enhanced in response to the degree of initial surface roughness. Therefore, the strategy to obtain the sharp switching for n-MoS$_2$ FETs is to develop stress-free high-k deposition while maintaining the atomic flatness for the substrate surface. On the other hand, on the VB side, $V_{S}$-induced defect states dominate the interface degradation. To improve the hole transport, continued efforts to improve the crystallinity are required.

4. Experimental Section

Device Fabrication: n-MoS$_2$ flakes were ME from natural bulk MoS$_2$ crystals purchased from SPI Supplies, while p-MoS$_2$ flakes were obtained from Nb-doped bulk MoS$_2$ crystals purchased from HQ graphene. This Nb-doped MoS$_2$ crystals are grown by chemical vapor transport deposition process in a pyrolytic boron nitride (PBN) crucible in an Ar atmosphere with 1 Pa to form the buffer layer.$^{[45,46]}$ Al$_2$O$_3$ oxide layers with thicknesses of 10 or 30 nm were deposited via ALD, followed by the Al top-gate electrode formation. No annealing was conducted.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

N.F. was supported by a Grant-in-Aid for JSPS Research Fellows from the JSPS KAKENHI. This research was partly supported by The Canon Foundation, the JSPS Core-to-Core Program, A. Advanced Research Networks, the JSPS A3 Foresight Program, and JSPS KAKENHI Grant Numbers JP16H04343, JP19H00755, and 19K21956, Japan.

Conflict of Interest

The authors declare no conflict of interest.

Keywords

defect states, heterostructure, quantum capacitance, two-dimensional material

Received: June 4, 2019
Revised: August 20, 2019
Published online: September 30, 2019

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