PyCells for an Open Semiconductor Industry

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Abstract—In the modern semiconductor industry, automatic generation of parameterized and recurring layout structures plays an important role and should be present as a feature in Electronic Design Automation (EDA)-tools. Currently these layout generators are developed with a proprietary programming language and can be used with a specific EDA-tool. Therefore, the semiconductor companies find the development of the layout generators that can be used in all state of the art EDA-tools which support OpenAccess database appealing. The goal of this project is to develop computationally efficient layout generators with Python (PyCells), for ams AG technologies, that possess all the features of comprehensive layout generators.

Index Terms—PyCells, Semiconductor, OpenAccess

1 INTRODUCTION

The number of companies active in modern semiconductor business is increasing every day which raises the demand for cheaper EDA-tools. However, one of the main steps of designing an integrated circuit is drawing the physical structure, the layout. Thus the EDA-tools should have a feature for automatic generation of parametrized, recurring structures as pre-defined layouts in a library. The layout generators which are presently in use, are developed using a proprietary language, SKILL, and are only usable as a feature of a specific EDA-tool. On the other hand, the second major drawback of using the proprietary layout generators is the lack of interoperability characteristic. Consequently, the semiconductor manufacturers are not able to support their customers in an optimal way. Hence, the use of an open standard for an EDA database also allows chip designers to work on the same chip-design using tools, which often have more affordable prices, from different EDA vendors.

The aim of this project is developing interoperable layout generators with Python (PyCells), for H35, C35, and S35 technologies of ams AG, that can be used by any EDA-tool supporting OpenAccess database. The OpenAccess database will be further explained in the next section. For a certain set of parameters, PyCells should generate layouts identical to those generated by SKILL codes (PCells). Furthermore, extra interactive features such as stretching and auto-abutment are added to PyCells which are verified to be accurate and are optimized with respect to performance.

2 DEVELOPMENT

OpenAccess [OpenAccess] has been established as standard for storing design data in the semiconductor industry and builds the foundation for interoperability of EDA-tools. OpenAccess is a file based database and manages logical design data (schematics) as well as artwork data (layout) for manufacturing. The reference implementation for accessing design data within the database is written in C++. The company Ciranova (now acquired by Synopsys) developed a Python wrapper [PythonAPI] for the OpenAccess C++ class library with the goal to access and modify design data through Python. Additionally, they provide an integrated development environment [SynopsysPyCellStudio] that enables interactive development and debugging of Python code, while the effects on the design data are shown directly in a separate window of the GUI.

In our development, we have used Python API library to write Python codes which generate recurring layout structures based on a given set of parameters. Typical recurring structures are primitive devices that are used in integrated circuit design such as resistors, capacitors and transistors. The electrical properties of the mentioned devices are simplified to geometric dimensions (e.g. width and length) which serve as parameters for the Python scripts. The object oriented nature of Python matches very well with this task as shown in the following example:

A typical CMOS semiconductor process offers n-channel and p-channel transistors. Each of these transistor types can have multiple voltage ratings (e.g. 5V, 20V, 50V 120V), accordingly resulting in different layout structures. In general, transistors have similar gate, source and drain structures, yet they have different doping concentrations for the implant regions of the semiconductor material and different protection structures, which need to be reflected in the layout. Therefore, we have created a set of base classes in Python from which the more specific transistors inherit common structures, while adding only structures dedicated to the type of transistor. This approach reduces duplicate code and makes maintaining the scripts more intuitive when the number of devices increases. Finally the Python scripts are compiled to byte-code and stored inside the OpenAccess library. A plugin of the OpenAccess database ascertains loading the correct script when a parameter of the corresponding device is modified. In the next section, the development of PyCells is explained using a sample high voltage transistor.

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regions with different doping concentrations have to be created at the drain terminal of the transistor. (see Figure 4)

Similarly an n-well should be added to define the device body, followed by a p-implant layer on source and drain. Furthermore, the bulk connection of the pmos20t device is accomplished by a contact ring around the device which has to make the connection to the n-type isolation well, for which n-type implant and a shallow n-well are required. (see Figure 5)

Lastly, the overall device structures, such as definition layer for the thickness of the gate oxide, should be added to PyCell. The resulting layout for pmos20t is shown in Figure 6.

Figure 7 shows the layout generated for a transistor with 50V guard ring and multiplication factor of 2.

2.2 Optimization

The computation time plays a crucial role in designing integrated circuits. The complexity of the designs and the amount of operations necessary to generate layouts of high voltage devices or the large devices increase the computation
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3 STRETCHING

Along with the basic features such as specifying parameters for recurring structures, the Python API also offers more enhanced interactive features with the EDA-tool [PythonAPI]. Stretching, which is one of these features allows changing parameters of an instance interactively. This helps the engineer to fit instances of an analog design into the available space, without affecting the electrical properties of the instance. For example, the capacitance value of a capacitor depends to a large extent on its area. Therefore, the shape can be varied while maintaining a constant area. An example of stretching is shown for a rectangular capacitor in Figure 8:

\[ C \propto W \cdot L \]  

The electrical properties of resistors and transistors are proportional to the ratio of length and width:

\[ R \propto \frac{L}{W} \]  
\[ g_m \propto \frac{W}{L} \]

Therefore, one cannot simply fit them into a given shape without affecting the behavior of the design. One option is to allow the resistors to have bends (as shown in Figure 9) or to change the number of fingers of transistors (see Figure 10). Stretching the gate of a transistor to change its dimensions is also possible (see Figure 11).

The stretch handles appear as diamond shaped elements on the GUI, indicating the place where the user can click and drag the object in order to change its dimensions. These handles are stored as properties in the OpenAccess database and are defined within the Python source code. The stretch handles have to be associated to the shape and parameters of the layout. Stretching can be limited to minimum and maximum boundaries on both horizontal and vertical directions. Snap
resolution can be also be specified in definition of stretch handles, an example of which is shown below:

```python
stretchHandle(
    name = 'width_handle_left',
    shape = poly1GateShape,
    parameter = 'wtot',
    location = CENTER_LEFT,
    direction = EAST_WEST,
    stretchType = 'relative',
    minVal = 0.4,
    maxVal = 10000.0
)
```

The GUI of EDA-tool displays the stretch handles as small diamonds on layout, which can be dragged by the engineer graphically to change the value of parameters using mouse. By releasing the stretch handle, the Python code is automatically invoked and the layout structure is adapted according to the new values of parameters.

## 4 Abutment

Another advanced feature is auto-abutment which is used to make the layout more compact. In case of placing two instances next to each other, the layout can be adapted in a way that common structures are shared between the instances. This minimizes the layout area and two instances appear to be merged. Similar to stretching, auto-abutment is defined by additional properties associated with shapes in the OpenAccess database. In PyCells, abutment is defined for a graphical structure by the autoAbutment() function:

```python
autoAbutment(
    shape = drain,
    pinSize = self.w,
    directions = [WEST],
    abutClass = 'mos_drain',
    abut2PinEqual = [{'spacing': 0.0},
                    {'diffLeftStyle': 'DiffHalf'},
                    {'diffLeftStyle': 'DiffHalf'}],
    abut2PinBigger = [{'spacing': 0.0},
                     {'diffLeftStyle': 'DiffEdgeAbut'},
                     {'diffLeftStyle': 'DiffEdgeAbut'}],
    abut3PinBigger = [{'spacing': 0.0},
                     {'diffLeftStyle': 'DiffEdgeAbut'},
                     {'diffLeftStyle': 'DiffEdgeAbut'}],
    abut3PinEqual = [{'spacing': 0.0},
                    {'diffLeftStyle': 'ContactEdgeAbut2'}],
    abut2PinSmaller = [{'spacing': 0.0},
                       {'diffLeftStyle': 'DiffEdgeAbut'},
                       {'diffLeftStyle': 'DiffEdgeAbut'}],
    abut3PinSmaller = [{'spacing': 0.0},
                       {'diffLeftStyle': 'DiffEdgeAbut'},
                       {'diffLeftStyle': 'DiffEdgeAbut'}],
    noAbut = [{'spacing': 0.4}]
)
```

This function provides a variety of parameters to define which attributes are compatible with abutment. Only instances that have common layout structures can be merged. Furthermore, there are arguments of this function to specify different types of abutment, for example in cases where the instances have common structures but different dimensions. It is also important to take logical information of the design into account, as it is only allowed to merge structures which are logically connected (i.e. having the same net). The resulting layout can be further diminished, when the two instances are the only devices connected to the net. In this case, the structures between the two instances, that would allow connections to the net, can be omitted. The abutment process is shown in Figure 12, and Figure 13 depicts different cases of abutment.

In order to abut two transistors, the layout designer should drag one instance and place it such that the drain contacts overlap. Consequently the abutment feature of the PyCell will
be triggered and two instances will be merged. If one instance is relocated, each of the other instances will get its initial structure.

5 Verification

The last part of the project which is of utmost importance is verifying the PyCells. We have considered four processes in order to verify the accuracy of PyCells: Design Rule Check (DRC), Layout Versus Schematic (LVS), Schematic Driven Layout (SDL), and database Comparison (DBCOMP), as explained below.

5.1 Design Rule Check (DRC)

The semiconductor manufacturers define a set of design rules for every technology with which the layout of every design must comply. Therefore, all the layouts generated by PyCells with various parameters, are checked for design rule violations in order to ensure the design accuracy of them. A DRC verification software checks the layouts and highlights the violations of design rules, such as insufficient space between layers, overlapping layers, incorrect dimension of layers, etc. Some of these design rules are shown in Figure 14.

5.2 Layout versus Schematic (LVS)

The layout of a design should match with its schematic with respect to type, number of devices, connections and topological parameters. In this verification process, we ensure that the layout of a sample design which is generated by PyCells matches perfectly with its corresponding schematic. The LVS tool, first extracts the netlists of layout and schematic of a design according to design rules defined by semiconductor manufacturer. In these netlists, the devices used in design and their connections as well as topological parameters (such as area, perimeter, etc) are listed. The LVS tool compares these netlists and reports if the schematic and layout of the design match completely with respect to type and connection of devices as well as topology of them. It also reports the existence of fragmented nodes which appear if the connections are not identical in the front- and back-end of the design.

5.3 Schematic Driven Layout (SDL)

PyCell codes must include the definition of pins regarding type of connections, weak connection (by polysilicon) or strong connection (by metal), and also the definition of shapes requiring external connections. Having types of connections implemented in PyCells, the SDL Navigator tool can attain the schematic of a sample design and generate the layout of it by calling PyCells with respective parameters. After generation of the layout, SDL Navigator checks the connectivity features using flylines (the wire-like shapes which appear on layout and show the connections between the ports).

5.4 Database Comparison (DBCOMP)

The last verification step is to substantiate the main aim of this project, generating layouts with Python (PyCells) precisely similar to those generated with SKILL (PCells). This verification process is in GDSII level and is performed with the help of a regression test, by which the PCells and PyCells of identical devices with a same set of parameters are instanced in a layout, and then these instances are compared to be congruent.

6 Conclusion

Believing in what Richard Stallman has said "Proprietary software is an injustice", we have successfully developed the layout generators for an open semiconductor industry, giving the designers who use ams AG technologies, opportunity to work with any desired EDA-tools, to share their designs easily with others, and to receive the support they deserve. These PyCells are developed for all high and low voltage devices of ams AG technologies in order to enable the IC-designers to have advanced designs without having constraints because of missing parametrized layouts. Furthermore, by using these PyCells we have managed to reduce the computation time which is extremely important in semiconductor industry. The developed PyCells have passed all the verification tests and in practical use by customers. The PyCells are available free of charge to all Europractice members, currently more than 500 universities and more than 100 research institutes worldwide active in IC design are members of Europractice, and have free access to the technologies of ams AG including the PyCells.

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