Resistive switching of CuO nanofibers embedded into hollow channels of SiO₂ layer

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Abstract. In this work, we have formed CuO memristive array embedded into porous SiO₂ layer. Such an approach would create synaptic system on silicon substrate using standard integrated electronics operations. It also provides control over the geometric parameters of artificial synapses, which determines their synaptic weights. The results of synaptic behavior have shown that the value of synaptic weights and currents are dependent on the thickness of the CuO filled SiO₂ porous layer.

1. Introduction
Currently, researchers around the world are intensively studying systems that model the nervous system of living beings [1,2]. This interest in neuromorphic systems is related to their ability to solve ill-posed tasks, such as recognition of images in the external environment. It should be noted that this advantage is absent in the classical architecture of digital computers due to the sequential processing of arrays of data and commands [3].

In biological systems, neurons are interconnected through synapses, which may alter their strength to inhibit or facilitate communication between two neurons (synaptic depression or synaptic potency, respectively) [1]. This ability is called synaptic plasticity and is a key mechanism used by biological systems in the learning process [4].

To create artificial synapses, devices with high density, low power consumption and the possibility of obtaining them using the already developed technology of integrated electronics are required. This is due to the fact that the number of synapses in the real system is greater than the number of neurons by several orders of magnitude [5].

Earlier physical realisations of memristors fabricated on silicon substrates with metal–oxide–metal materials such as TiO₂ or ZnO are reported in literature [6,7]. The WO₃ and TiO₂ based neuromorphic devices are popular among the research fraternity [8,9].

Memristors with resistive switching, belonging to bipolar structures, significantly change the resistance under the action of an electric field. This allows to emulate neural activities called synaptic plasticity: an increase in resistance corresponds to depression, and a decrease corresponds to potentiation [1]. It is known that the synaptic plasticity of memristic structures is determined by their synaptic weight [10]. In turn, on the example of memristic cells based on CuO, it is found that the synaptic weight is determined by the structure and geometric parameters of the active element of the memristor device. Here it should be noted that CuO nanofiber memristor device is not practically explored for the
neuromorphic application. To solve the problems of the formation of memristic arrays on a crystal, and to provide them with the necessary geometry, this paper proposed the formation of memristic cells in the pores of the SiO2 layer located on a silicon wafer between the layers of electrically conductive crossbars.

2. Experiment

The formed samples are a multilayer structure placed on a silicon substrate. It contains an insulating layer of silicon oxide, the lower layer of copper bars, CuO filled porous layer of silicon oxide, the upper layer of aluminum bars. The scheme of arrays of memristic structures is shown in Fig. 1.

![Scheme of arrays of memristic structure](image)

Figure 1. Scheme of arrays of memristic structure

The route of manufacturing these structures was as follows. An insulating layer of silicon oxide was formed on the surface of the silicon substrate by thermal oxidation. On its surface by magnetron sputtering a layer of copper was applied by photolithography to form four bars with bonding pads. The width of each bar was 2 microns. Having previously protected the bonding pads, a layer of tetraethoxysilane of different thickness was applied to the surface of the bars by spin-coating [11]. To remove the organic component from the substrate, the plate was annealed in ambient atmosphere at a temperature of 500 °C for 1 hour. On the surface of the resulting layer, a layer of aluminum was applied by magnetron sputtering, which was converted into a porous oxide by anodizing under the conditions described in [12]. Pores were formed in accordance with using porous aluminum oxide as a solid mask by ion etching in the silicon oxide layer [13]. The porous oxide mask was removed in an aqueous solution of 3.5% H3PO4 with the addition of 45 g/l CrO3 at a temperature of 90 °C for 5 minutes. The pores of the oxide of silicon were filled with oxide of copper by electrochemical deposition. As an electrolyte, an aqueous solution of 0.5 g/l CuSO4 with the addition of 5 g CH3COONa·3H2O at room temperature was used, the voltage and pH were 2V and 7.1, respectively. The deposition process was carried out before the appearance of a solid copper oxide precipitate on the surface of SiO2, which was subsequently removed with a soft polisher. On the surface of a silicon oxide layer by magnetron sputtering was applied to the aluminum layer by photolithography in parallel copper rails formed four bars with bonding pads. The width of the bars was also 2 microns. Thus, an array of 16 memristic cells was obtained. The structure and composition of the obtained structure were investigated by atomic force microscopy (Solver P47, NT-MDT, Russia) and X-ray diffraction (X8 Advance, Bruker, Germany).

3. Results and discussion

In accordance with the above-mentioned route, after thermal annealing in the external environment, a number of samples with different thickness of the porous SiO2 layer covering copper bars (lower electrodes) and open areas of the silicon oxide film on the silicon plate were formed. To do this, a different amount of tetraethoxysilane solution was fed to a Si/SiO2/Cu substrate placed on a centrifuge. The rotation frequency was 3200 rpm. To control the thickness of the porous layer of SiO2 by local liquid etching, a step was formed in the layer, the height of which was measured by atomic force
microscopy. Figure 2 shows AFM image of the deposited SiO$_2$ film, as well as the dependence of its thickness on the amount of the solution supplied to the substrate.

Figure 2. AFM image of the deposited SiO$_2$ film (a) and the dependence of its thickness on the amount of the solution supplied to the substrate (b)

Figure 3a shows the surface of the film of the porous layer of SiO$_2$ after the process of plasma local etching through a solid mask of porous anodic aluminum oxide. It was found that the nanoscale pattern with regular through holes was completely transferred to the volume of the SiO$_2$ film. The completeness of the etching process of the porous SiO$_2$ layer to the desired depth was controlled through the establishment of the fact of occurrence of the electrochemical process of deposition of CuO because when at the insufficient depth the copper bars were coated with the dielectric SiO$_2$ layer and there was no electric current in the system. Figure 3b shows an image of the surface of the nanostructured film after electrochemical deposition into the pores of nanowires of CuO. Scanning of surface morphology of SiO$_2$ using AFM was conducted on plots located on the bottom copper bars. Uniform filling of all pores is observed for all film thicknesses. Figure 3c presents a characteristic X-ray diffraction pattern of the structure of Si/SiO$_2$/Cu/nf-CuO SiO$_2$. From the figure you can observe the presence of peaks of copper, copper oxide and silicon oxide. To measure the current-voltage characteristics of the fabricated structures, potentials were supplied between the lower (copper) and upper (aluminum) electrodes. Figure 4a shows the dependence graphs $I=f(V)$ for each of the sixteen memristors formed at the intersection of the upper and lower electrodes. The length of the nanofibers of SiO$_2$, filling the hollow channels of silicon oxide, was approximately ~ 300 nm. From the figure it can be observed that each memristor cell is characterized by two states of conductivity. The ratio of resistance in the low-resistance and high-resistance states is about 50. Almost identical characteristics indirectly confirms the high reproducibility of the complete filling and uniform filling of the nanofibers of copper oxide hollow channels of the porous layer of silicon oxide on the entire surface. This behavior is also typical for samples with other thicknesses of the porous SiO$_2$ layer.
Figure 3. AFM image of the surface of the film of the porous layer of SiO$_2$ after the process of plasma local etching (a), after electrochemical deposition into the pores of nanowires of CuO (b) and XRD spectra of this structure (c)

Figure 4. Current-voltage characteristics of sixteen memristors on porous SiO$_2$ (a), and between bars A and H in the samples with different porous layer thicknesses (b)

Figure 4b demonstrates the current-voltage characteristics measured between bars A and H in the samples with different porous layer thicknesses. With the increase in the thickness of the porous layer of silicon oxide, an increase in the value of the current is observed.

It is known that in biological systems, synaptic weights increase or decrease depending on the rate of change of electrical or chemical signals [10]. Similar behavior is also observed in the studied memristic cells. The correlation of the current values and the rate of voltage supply to the memristic cell was found. Figure 5 shows the current-voltage characteristics measured between bars A and H at different sweep rates. In this case, the kinetic dependence of the current can be considered as a synaptic weight. It has been established that memristors of this type have the highest synaptic weight at a supply rate of 50 to 100 V / s. Similar results were obtained for all sixteen meristate cells.

4. Conclusion
This paper presents a prototype of a memristic matrix based on silicon oxide on a silicon plate with addressing electrically conductive crossbars. The behavior of memristor properties of cells depending on the rate of voltage supply and the thickness of the porous layer of SiO$_2$ is studied. The results of synaptic behavior have shown that the value of synaptic weights and currents are dependent on the thickness of the CuO filled SiO$_2$ porous layer.
Figure 5. Current-voltage characteristics measured between bars A and H at different sweep rates

Such a structure can be the basis for creating arrays of artificial synapses for neuromorphic applications, implemented on silicon substrate using standard integrated electronics operations.

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