Monolithic Integrated AlGaN/GaN Power Converter Topologies on High-Voltage AlN/GaN Superlattice Buffer

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A high-voltage AlN/GaN superlattice (SL) buffer for monolithic AlGaN/GaN power circuits is experimentally compared with a step-graded AlGaN/GaN buffer. The SL as part of a 5.1 μm epitaxial stack withstands over 1.3 kV. Although the step-graded buffer is sufficient for low-side circuits, the operation voltage of monolithic topologies such as a half-bridge is limited: static negative back gating at −200 V depletes the lateral channel completely. Asymmetrical buffer leakage at a positive substrate voltage of +250 V limits the operation voltage further. The SL buffer mitigates both effects: a negative substrate voltage of −200 V reduced the lateral channel current only by 25%. However, this condition is not required for half-bridge operation on the SL, because low symmetrical vertical buffer leakage at substrate voltages of ±500 V allows operation of power topologies with positive substrate bias. High-electron-mobility transistors (HEMTs) on the graded buffer show excessive threshold voltage shift at negative substrate bias. On the SL buffer, the threshold voltage is shifted only +1 V from negative substrate biases, which allows monolithic high-voltage power topology operation. 98.8% efficient operation of a 6 × 4 mm² GaN-on-Si power integrated circuit with a monolithic half bridge, freewheeling diodes, and drivers is demonstrated on the SL.

1. Introduction
1.1. Background

Monolithic integration of complete power converter topologies, circuits, and sensors for highly efficient and compact power conversion applications is feasible in the lateral GaN-on-Si power semiconductor technology.[1,2] One-chip GaN power topologies for switched-mode converters such as H-bridges,[3] boost converters,[4] three-phase inverters,[5] driver and protection circuits,[6] half-bridges,[7–9] control and logic[10–13] were realized. Single discrete high-voltage GaN-on-Si power transistors for voltages up to 650 V are in mass production with proven reliability. Higher voltages for single transistors up to 1.2 kV have been demonstrated[14] and are also already partly commercialized. In contrast to this single power transistor devices, the operation of monolithic GaN power integrated circuits (ICs) with more than one high-voltage power transistors on conductive silicon substrate is still challenging. While a single high-voltage power transistor is typically operated with the conductive silicon substrate (or backside/bulk) tied to the source potential, in most power topologies such as a half bridge with two monolithically series-connected transistors, at least one of the transistors is at the mercy of substrate biasing effects because the common conductive silicon substrate prohibits a separate substrate-to-source termination of all integrated transistors.

1.2. Substrate- and Buffer-Related Challenges

Figure 1 shows the substrate biasing challenge. The cross section of a monolithic GaN-on-Si half bridge as part of a half-bridge direct current (DC)–DC buck converter shows two monolithically series-connected power high-electron-mobility transistors (HEMTs) on a single conductive silicon substrate. An AlGaN/GaN heterojunction above an isolating buffer layer forms a 2D electron gas (2DEG), which is used as conductive channel. Gate electrodes on the top-side of the channel (top-gates) enable control and depletion of the channel and thus switched-mode operation of the HEMTs. The top gate is typically less than 25 nm away from the channel and thus allows control of the channel with low gate-to-source voltages (typically below 7 V) and a high transconductance. In addition to the top gate, the conductive Si substrate is a second gate (back gate), separated by the isolating buffer layers by typically between 3 and 5 μm.
In single discrete transistors, it is possible to terminate the substrate to source, such that the substrate-to-source voltage is kept zero $V_{BS} = 0 \text{ V}$ all the time, and unintentional control of the channel current by the back gate is avoided. In a monolithic GaN-on-Si half bridge however, the substrate-to-source voltages of the two series-connected transistors (high-side and low-side transistors) are linked to the switch-node voltage $V_{SW}(t)$ by $V_{BS,\text{LS}}(t) = V_{BS,\text{HS}}(t) = V_{SW}(t)$. In a switched-mode converter, $V_{SW}(t)$ is a rectangular voltage signal between 0 V (GND) and the DC operation voltage $V_{DC}$. The dependent substrate voltages $V_{BS,\text{LS}}$ and $V_{BS,\text{HS}}$ now cover both positive and negative substrate voltages during operation, which possibly causes different substrate biasing effects during operation. Since the substrate voltages are now linked to the operation voltage of a converter, also the magnitude of the biasing effects depends on the operation voltage. As a result, while low-voltage monolithic circuits in the 100 V class are operable, especially high-voltage circuits require additional technological improvements for faultless circuit operation. Known back-gating effects are classified into static back-gating effects such as lateral channel current reduction at negative substrate bias,[15,16] including a current polarity dependence,[17] excessively increased static vertical leakage,[21] and dynamic effects such as cross-talk[19–21] and the threshold voltage shift.[28]

Advanced isolation techniques such as GaN-on-silicon-on-insulator (SOI)[20,29,30] or back surface isolation techniques[31] have been successfully realized and avoid the substrate biasing effects by local substrate-to-source termination of integrated devices. However, the improved isolation is realized in a trade-off with increased substrate capacitances (in case of additional thin buried oxides in GaN-on-SOI), increased thermal resistance from additional oxide layers, or the risk of silicon p–n-junction conduction. Another approach to reduce substrate biasing effects is to replace the conductive silicon carrier substrate by isolating substrates such as SiC,[32] GaN,[33] sapphire,[34] or other engineered substrates, which however results in higher fabrication cost compared with silicon. Instead of adding additional vertically isolating and conducting layers as in SOI, another approach is to improve the buffer and increase the thickness[35,36] of the buffer to mitigate substrate effects.

1.3. Approach and Outline

Despite the discussed approaches, the operation of monolithic integrated high-voltage power topologies in a pure GaN-on-Si technology, using only the GaN buffer as vertical isolator, and without additional vertical isolation techniques, is still desirable. A superlattice (SL) buffer is known to be superior in terms of vertical isolation compared with a graded buffer (GB), and thus a promising approach for GaN power ICs. Growth of GaN/AIN SLs on silicon substrates over AlGaN and AlN interlayers was demonstrated in the studies by Egawa and coworkers,[36,37] using as capping layers for the reduction of resistance in GaN HEMTs,[18] and then optimized for high-quality crack-free buffer layer structures,[19–22] increased breakdown voltage,[23,24] and switching and high-frequency transistors.[44,45] SL buffers enabled the reduction of on-resistance and trapping effects in GaN heterostructures for applications from 600 V up to 1.2 kV[14,46] and were combined with other advanced isolation techniques such as silicon-on-insulator.[47] SLs as engineered layers[48] are also used in other applications such as for optical devices.

This work first presents an AlN/GaN SL buffer epitaxy, which suppresses substrate biasing effects more effectively than a conventional step-graded buffer. Then, GaN-on-Si power devices for operation of monolithic high-voltage power converter topologies are characterized and compared. Next, a monolithic high-voltage GaN-on-Si half-bridge topology with integrated driver circuit, additional circuitry, and sensors is fabricated on both buffers. Finally, measurements of a DC–DC converter based on the monolithic half-bridge topology on both buffers are compared.

2. Results and Discussion

2.1. Epitaxy of SL and Step-Graded GaN Buffers

Figure 2 shows the fabricated vertical layer stacks of the step-graded AlGaN/GaN buffer (Figure 2a) and the AlN/GaN SL buffer (Figure 2b) and lists the thicknesses of the respective layers.

The SL and step-graded buffer structures were grown by metal organic chemical vapor deposition (MOCVD) in a Veeco K465i reactor on 800 μm-thick 4 in. highly conductive Si(111) substrates. Before the deposition of a 120 nm-thick AlN nucleation layer, the Si(111) substrates were cleaned in H₂ environment at a temperature of 1100 °C for 10 min to remove native oxide. For the step-graded buffer structure, three AlGaN layers were grown with decreasing Al content of 77%, 53%, and 29%, respectively, followed by a thick GaN layer with a thin AlN interlayer. For the SL buffer structure, 80 periods of AlN/GaN were deposited followed by a thick GaN layer with the same AlN interlayer. Part of the GaN buffer layer was doped with carbon up to $3 \times 10^{19} \text{ cm}^{-3}$ to ensure high vertical and lateral isolation. Finally, a thin AlGaN barrier and GaN cap layer were grown on both buffer structures to form a 2DEG for HEMT devices. The Al concentration of the barrier layer and the sheet resistance of the 2DEG is 22% and 24.5% and around 700 and 500 Ω·μm−1 for the GB and SL buffer, respectively. The growth conditions for both structures were optimized to
improve layer quality and vertical isolation and to reduce the internal strain build up during growth and the cooling down process at the end of the growth run.

### 2.2. Vertical and Lateral Voltage Isolation Capability

The lateral isolation between the ohmic contacts results from ion implantation, and the vertical isolation from the epitaxial buffer layer stack. Devices and test structures are processed on both buffer structures and are characterized and compared in the following.

**Figure 2.** Epitaxial layer stacks of a) step-graded AlGaN/GaN buffer and b) AlN/GaN SL buffer.

**Figure 3.** Shows measured vertical leakage currents between a top-side electrode and the substrate as a function of the substrate voltage. Measurements of 37 positions across the wafer show a low variation and a high reproducibility of the epitaxy. The measurement range is limited by the current compliance of the equipment and the discontinuity at zero due to reconfiguration of the wafer prober. Comparing the SL to the GB at equal vertical leakage current, the negative substrate voltage blocking capability is increased by around 300 V, and the positive substrate voltage blocking range increased by around 400 V. The observed asymmetry depending on the substrate bias polarity is further discussed in literature, for example, the studies by Zhang et al., Tang et al., and Borga et al. [18,49,50]

**Figure 4.** Shows the measured leakage currents of lateral isolation test structures between two ohmic contacts on grounded substrate as a function of the lateral voltage. Different lateral isolation distances between 1.5 and 10 μm are measured. Despite identical lateral isolation distances on the GB and the SL buffer, breakdown occurs earlier with the GB. For a lateral separation of 10 μm, the voltage blocking capability of the test structures was around 800 V on the GB and above 1300 V on the SL buffer. Based on the 5 μm layer structure, the SL buffer improved the lateral isolation on grounded substrate from 108 to 140 V μm⁻¹. From the 10 μm structure and the total buffer thicknesses from Figure 2, the isolation is at least 195 V μm⁻¹ (GB), and above 225 V μm⁻¹ (SL buffer), which is close to other state-of-the-art SL GaN buffers and the material limit. [35,44]

In addition to the test structures, normally on Schottky-gate GaN-on-Si HEMTs were processed on both buffer types. **Figure 5.** Shows the measured off-state drain current as a function of the off-state drain-to-source voltage for different gate-to-drain lengths between 1.5 and 13 μm. Compared with the measured isolation structures from Figure 4 without Schottky contacts, for the fully processed
devices with Schottky gates, the leakage current increases to above 10 µA mm\(^{-1}\) already at low drain-source voltages. The measured voltage blocking capability (at 100 µA mm\(^{-1}\)) of transistors on the GB is limited to around 700 V by leakage currents. On the GB (Figure 5a), the high-voltage device with \(L_{GD} = 9\) µm has a blocking voltage of 680 V, but increasing \(L_{GD}\) further to 13 µm already shows the saturation of the blocking voltage at around 700 V, which is an indication that the GB is limiting the voltage blocking capability.

On the SL buffer (Figure 5b), for \(L_{GD} = 9\) µm, already an increased blocking voltage of 860 V was measured, which then still further increases to above 1 kV when increasing \(L_{GD}\) to 13 µm. The measurement shows that the improved vertical isolation of the SL buffer (Figure 4b) forms an improved precondition for high-voltage devices. It should be mentioned that the total buffer thickness of the SL epitaxy is also increased by 24% compared with the GB (Figure 2). However, the increase in the voltage blocking capability of 46% is significantly higher and thus not explained only by the buffer thickness, but instead by the improved quality and isolation of the SL buffer.

2.3. Reduction of High-Voltage Substrate Biasing Effects

The improved vertical isolation of the SL buffer is also beneficial for IC operation: In addition to the increased blocking voltage capability, the improved vertical isolation of the SL buffer also significantly reduces substrate biasing effects. Furthermore, vertical substrate leakage is symmetrically suppressed up to high-positive substrate biasing voltages. Compared with the GB, this allows the operation of monolithic circuits with zero or positive substrate bias voltages only. Non-negative substrate bias voltages avoid the static channel current reduction and thus increased on-resistance and conduction losses from the static back-gating effect.

Figure 6 shows back-gated transfer characteristic measurements\(^{[23,51]}\) of a laterally conductive channel between two electrodes without a top-gate contact, using the conductive silicon substrate below the epitaxial layer stack as back gate instead. The test structure is part of a 1 x 1 mm\(^2\) cell layout and contains a 160 µm-wide top-gate-less 2DEG channel between two 700 µm separated ohmic contacts. The layout of the structure is shown in the study by Weiss et al.\(^{[24]}\). A voltage of 1 V is constantly applied between both electrodes, and both the lateral channel current and the vertical buffer leakage are measured. The substrate voltage sweep started at −500 V, and ramped up and then down again, indicated by arrows. As the GB has a reduced positive substrate voltage blocking capability, limited by vertical leakage, the voltage is only ramped to +300 V. Although the particular GB shows asymmetrical vertical leakage, Zhang et al.\(^{[18]}\) engineered an epistructure without SL but also nearly symmetrical vertical leakage. On the SL buffer, the measured vertical leakage is symmetrical, and at a positive substrate voltage of +300 V, still three orders of magnitude lower than on the GB. Therefore, the voltage was ramped up to +500 V.

For a negative substrate voltage of −200 V, the lateral channel current on the GB is already completely depleted (reduction by above 10\(^5\)). For the lateral channel structures on the SL buffer, however, at −200 V, the channel current is only reduced by 25%. A relation between the observed hysteresis in Figure 6 and charge trapping in the buffer layer stack is discussed for example in the studies by Kabouche et al., Weiss et al., and Chen et al.\(^{[14,24,52]}\). In addition to the back-gated transfer measurement of a gateless structure in Figure 6, also a fully processed GaN HEMT was measured for different substrate voltages.

Figure 6. Lateral channel current and lateral substrate leakage current for substrate bias voltages between −500 and +500 V. Back-gated transfer characteristic of top-gate-less device.
Figure 7 shows top-gated transfer measurements for different fixed substrate voltages between $-200$ and $+200$ V. The complete channel depletion at $-200$ V on the GB is visible, and also results in an effective threshold voltage shift (compared with zero substrate bias) between $-0.5$ and over $+2.5$ V. The vanishing channel current and high threshold voltage shift does not allow a reliable high-voltage design or operation of circuits which require a wide range of substrate biasing voltages, such as a monolithic half-bridge without other additional vertical isolation measures. The SL buffer shifts the threshold voltage only by $\pm 0.5$ V for a $-200$ to $+200$ V substrate voltage range. If only positive substrate bias voltages are used, which is possible on the SL due to the low symmetrical vertical leakage current, then a circuit design and operation with low threshold voltage shift and high-saturated channel currents are feasible.

2.4. Effect on C–V and I–V Characteristics at Zero Substrate Bias

The SL buffer not only improves device’s characteristics for monolithic integrated topologies, but also for single transistors with a substrate-to-source termination (zero substrate bias $V_{BS} = 0$ V). For discrete transistors, the switching performance is influenced by the device capacitances. Lower terminal capacitances result in reduced switching loss during hard-switching operation, and reduced switching time during resonant transitions. The device capacitances consist partly of the substrate capacitances between top electrodes and the substrate.

Figure 8 shows measured terminal capacitances of a high-voltage GaN HEMT on both buffers (gate width 1 mm).

However, the overall buffer thickness $T = 5.1 \mu m$ of the SL stack is 24% higher compared with the step-graded buffer with $T = 4.1 \mu m$, this increased thickness in itself should lead to a 20% reduction of substrate capacitances. However, the measured substrate capacitances are reduced even further by up to 32%. This is explained by the highly defective initial graded AlGaN/GaN layers of the step-graded buffer, resulting in a lower-effective substrate thickness for the step-graded buffer. Figure 8 also shows that the improved vertical epitaxial layer stack only marginally influences the on-resistance, extracted from the output characteristics. Figure 8 shows measurements of three HEMTs with different lateral geometries. The lateral scaling reduces the on-resistance for 100 V-class devices (1.5 $\mu$m gate-to-drain spacing) to 2 $\Omega$mm and the saturated drain current to above 0.8 A $\mu$m. Here, the increased saturated current on the SL buffer results mainly from a variation of the Al concentration and thickness of the barrier layer, and not from the improved buffer. Different voltage classes on the same IC are useful to combine high-voltage power converter topologies with low-voltage driver, logic and auxiliary circuits in an area-efficient way.

Figure 9 shows the measured substrate-to-drain capacitance $C_{BD}$ as a function of the off-state drain-source voltage up to 200 V for a range of substrate bias voltages up to $+200$ V. The measured substrate–voltage-dependent capacitance reduction for the GB is another direct indication for the strong back-gating effect using the GB, similar to the measured current reduction from Figure 6.

2.5. Processing of GaN-on-Si Power Integrated Topologies, Circuits, and Sensors

On the highly isolating vertical epitaxial buffers, the monolithic integration of high-voltage power topologies and circuits is possible. Figure 10 shows a simplified technology cross section
with multiple integrated devices. The process allows the integration of a variety of active and passive components. Figure 10 shows a Schottky diode, a low-voltage normally off transistor without source field plate, a high-voltage normally on transistor with source field plate, a resistive trace as linear temperature sensor, and a high-voltage normally off transistor with source field plate as well as an intrinsic freewheeling diode, which is realized by dotted Schottky contacts in the gate-to-drain region. Ion implantation is used for lateral isolation between devices. Furthermore, integrated inductors and transformers have been demonstrated monolithically integrated in the same technology. Integrated capacitors with limited capacitance density are also possible.

2.6. Monolithic Half Bridge and Driver IC Operation on SL Buffer

This work presents the fabrication and operation of a monolithic power stage in a single 6 × 4 mm² GaN power IC on the discussed SL buffer. Two large-area high-voltage half-bridge transistors (gate width of 204 mm) with intrinsic freewheeling Schottky diodes, a gate driver final stage, and temperature, current, and voltage sensors are monolithically integrated. In the previous work, a similar solution, but as a two-chip assembly, and on a GB is published. The IC and functionality are also described in more detail in the study by Moench et al. Figure 11 shows the diced GaN-on-Si power IC and labels the core devices and functionality. Around 60% of the total IC area is covered by two large-area power transistors, which are series connected to form a monolithic half bridge, as also shown in Figure 1. The circuit on a common conductive silicon substrate thus heavily relies on low substrate biasing effects during operation as previously discussed.

The ICs were assembled on ceramic power modules and operated in a DC–DC converter with an experimental setup similar to the one in the study by Moench et al. Figure 12 shows the measured efficiency of the DC–DC converter for input voltages up to 200 V and a DC output load current up to 2.5 A. The switching frequency is 65 kHz, the duty-cycle is 50%, and the dead time...
times are 40 ns. The integrated gate driver final stages were used to control the main power transistors and operated with a dual-input predriver circuit as the one shown in the study by Moench et al.\cite{58} Measurements of the monolithic power stage on both the step-graded and the SL buffer are compared in the following, with all other parameters (except the used highly resistive substrate biasing network) identical.

At an operation voltage of 100 V, the maximum measured efficiencies for both buffer types were comparably high (98.8\% for the SL, 98.4\% for the GB). At an increased operation voltage of 200 V, however, the SL enabled still high efficiency up to 98.5\%, whereas the efficiency of the GB reduced below 94\%. The measured efficiencies of this work’s monolithic half bridge and driver IC is compared with a discrete half-bridge operation from the study by Moench et al.\cite{17} with a similar IC layout, but diced into two ICs with separate substrate-to-source terminations. The measured maximum efficiencies at 100 and 200 V are comparably high, but this work shows a higher efficiency at light load (0.5 A). This is explained because the floating substrate termination in this work reduces the effective switch-node capacitance and thus also the switching loss, which contributes in a higher ratio to the total losses compared with high load operation where the conduction loss dominates.

The reduction of output capacitances for the floating substrate termination compared with separate substrate-to-source terminations is explained in the study by Moench et al.\cite{25} The increased power loss at higher operation voltages on the GB is assigned to back-gating effects and analyzed in more detail the following.

Figure 13 and 14 shows the measured switching waveforms at 200 V, 1 A for the step-graded buffer and SL buffer, respectively.

The GB has a limited positive substrate voltage blocking capability, as shown in Figure 6. To avoid excessive vertical leakage currents during operation, the highly resistive substrate biasing network, which was proposed in the study by Weiss et al.,\cite{59} was used to shift the average of the substrate voltage \( V_B \) to approximately \( \frac{1}{2} V_{DC} \). The measured transient \( V_B \) is also shown in Figure 13. The down-shifting of the substrate voltage by the highly resistive biasing network limits the maximum positive substrate-to-source voltage during operation (here to \( V_{BS,LS,OFF} = 160 \) V). However, due to the linkage of the substrate voltages, there is a compromise: The voltage difference (here 40 V) between the operation voltage \( V_{DC} \) and maximum positive substrate voltage (\( V_{BS,LS,OFF} \)) is also present as negative back-gating voltage during high-side conduction (here \( V_{BS,HS,ON} = -40 \) V).

From Figure 6 and 7, it is visible that the expected channel current is already statically reduced more than 50\%. On the GB with high-positive leakage current thus the operation voltage of monolithic power stages is limited by the trade-off between back-gated on-resistance increase and positive substrate leakage. It should be noted that only the high-side device is negatively backgated. The low-side device has a positive substrate voltage during the conduction phase. In Figure 13, significantly increased on-state voltage is thus only observed for the high-side device, visible as the discrepancy of above 10 V between the operation voltage of 200 V and switch-node voltage during the high-side conduction phase (approximately between 180 and 190 V, corresponding to an on-resistance increase to above 10 \( \Omega \), compared with the zero-bias on-resistance of below 0.1 \( \Omega \)). The dynamic on-resistance increase observed in Figure 13 is much higher than the static back-gating measurements from Figure 6 and 7. Thus, additional dynamic back-gating effects occur on the GB, which were further investigated in the study by Weiss et al.\cite{24}.

The monolithic converter on the SL shows high efficiencies also at 200 V operation and avoids negative back-gating effects. As the SL buffer has symmetrical and low vertical currents, the positive substrate voltage is not limited as for the GB. This allows to use another substrate biasing network which avoids negative back gating during conduction phases. Figure 14 shows the modified substrate biasing network, which was proposed in the study...
by Moench et al.[17] The average substrate voltage is higher (now approximately \( \frac{1}{2} V_{DC} \)) than for the circuit in Figure 13 and ensures a zero substrate-to-source voltage \( V_{BS,HS,ON} = 0 \) V during high-side conduction. This is possible because the buffer of the low-side device can withstand the increased positive substrate voltage of here to \( V_{BS,LS,OFF} = 200 \) V without excessive vertical leakage currents. Both substrate biasing networks are also discussed in more detail in the study by Moench et al.[17]

Compared with commercially available monolithic GaN-on-Si half bridges, which are available up to 100 V, and monolithic GaN-on-Si half bridges with drivers, which are available up to 80 V,[60] both using advanced vertical isolation techniques, and compared with state-of-the-art research results of monolithic GaN-on-Si power stages up to 200 V using GaN-on-SOI,[47] this work shows that the operation of power stages on a pure GaN-on-Si technology using only an improved buffer is also feasible with low substrate biasing effects and thus high power conversion efficiencies.

3. Conclusion

The AlN/GaN SL buffer improves the vertical isolation and reduces substrate biasing effects of HEMTs compared with a step-graded buffer. Based on the SL buffer and using the lateral GaN-on-Si integration platform, the fabrication and operation of a monolithic half-bridge with drivers, freewheeling diodes, and sensors demonstrate a universal building block for power converters on a single chip. Low symmetrical vertical leakage up to at least \( \pm 500 \) V substrate voltage and over 1 kV lateral off-state blocking voltage in single HEMTs provides sufficient voltage margin to also operate monolithically integrated power topologies with multiple power transistors referenced to different voltages on a single chip.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

gallium nitride, high-electron-mobility transistors, monolithic integrated circuits, power integrated circuits, semiconductor superlattices, substrates

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