Resource-efficient DNNs for Keyword Spotting using Neural Architecture Search and Quantization

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Abstract—This paper introduces neural architecture search (NAS) for the automatic discovery of small models for keyword spotting (KWS) in limited resource environments. We employ a differentiable NAS approach to optimize the structure of convolutional neural networks (CNNs) to maximize the classification accuracy while minimizing the number of operations per inference. Using NAS only, we were able to obtain a highly efficient model with 95.4% accuracy on the Google speech commands dataset with 494.8 kB of memory usage and 19.6 million operations. Additionally, weight quantization is used to reduce the memory consumption even further. We show that weight quantization to low bit-widths (e.g. 1 bit) can be used without substantial loss in accuracy. By increasing the number of input features from 10 MFCC to 20 MFCC we were able to increase the accuracy to 96.3% at 340.1 kB of memory usage and 27.1 million operations.

Index Terms—keyword spotting, neural architecture search, weight quantization

I. INTRODUCTION

Automatic speech recognition (ASR) is becoming an increasingly important technology for user interaction with everyday consumer devices. However, ASR systems are typically complex and computation-intensive, i.e. running ASR in always-on mode results in a steady high energy consumption. This is especially problematic for mobile devices whose batteries are drained quickly when running ASR permanently.

A common approach to this challenge is to run a low-cost keyword spotting (KWS) system that is listening permanently for a limited set of prespecified keywords. Upon detection of such a keyword, a full ASR system is triggered which then listens for a rich set of user commands.

The requirements of a KWS system are:

i. The system should be resource-efficient to mitigate the aforementioned energy problem,

ii. it should run in real-time, and

iii. it should be accurate to maintain a high user-experience.

In this paper, we aim to find efficient and small KWS models for limited resource environments. We make use of neural architecture search (NAS) — a popular technique to automate the design of deep neural network (DNN) architectures. A NAS algorithm tries to find the best performing neural network architecture within a given search space using some arbitrary search method. To obtain efficient DNN models we use the techniques from ProxylessNAS [1]. However, unlike ProxylessNAS [1] whose focus is on finding models for large-scale image classification tasks such as ImageNet, our focus lies on small-scale KWS tasks such as Google speech commands [2].

We quantize model weights during NAS by default to 8 bits to better compare to [3]. In [3], model weights are also quantized to 8 bits. Using NAS we obtain a model with 95.4% accuracy on the test set of the Google speech commands dataset [2] while using 494.8 kB of memory (for the storage of weights) and 19.6 million operations per inference. Once the efficient DNN architecture has been found, we compare different weight quantization schemes to show that the memory requirements can be reduced even further. Compressing the weights of this model to 1 bit allowed us to retain a test accuracy of 94.7% while only using 61.85 kB of memory and 19.6 million operations.

Furthermore, we show that the number of features extracted from the raw audio waveform has a substantial impact on the performance. By changing the number of extracted MFCC features from 10 to 20 we were able to find a model with a test accuracy of 96.3% using 340.1 kB of memory and 27.1 million operations.

The outline of the paper is as follows: Section II introduces the related work. In Section III we present our NAS configuration, the trade-off objective between accuracy and number of operations, and the weight quantization methods utilized in this paper. The experimental setup and the discussion of the results is shown in Section IV. Finally, Section V provides the conclusion. Code related to the paper is available online at [https://github.com/dapeter/nas-for-kws].

II. RELATED WORK

Popular NAS approaches use concepts such as reinforcement learning [4], gradient based methods [5] or even evolutionary methods [6] for exploring the search space. Recently, NAS techniques have also been used to find architectures that are specifically tailored to the underlying hardware [1], [7] by, for instance, additionally minimizing memory requirements, number of operations, or latency of the resulting model.
Therefore, NAS techniques are well-suited for finding DNNs that run on mobile phones or even embedded devices.

Conventional NAS algorithms require thousands of architectures to be trained to find the final architecture. Not only is this very time consuming but in some cases even infeasible, especially for large-scale tasks such as ImageNet or when computational resources are limited. Therefore, several proposals have been made to reduce the computational overhead. So called proxy tasks for reducing the search cost are training for fewer epochs, training on a smaller dataset or learning a smaller model that is then scaled up. As an example, \cite{8} searches for the best convolutional layer on the CIFAR-10 dataset which is then stacked and applied to the much larger ImageNet dataset. Many other NAS methods implement this technique with great success \cite{5,7,9,12}. Another approach, called EfficientNet \cite{13}, employs the NAS approach from \cite{7} to find a small baseline model which is subsequently scaled up. By scaling the three dimensions depth, width and resolution of the small baseline model, they obtain state-of-the-art performance.

Although model scaling and stacking achieves good performance, the convolutional layers optimized on the proxy task may not be optimal for the target task. Therefore, several approaches have been proposed to get rid of proxy tasks. Instead, architectures are directly trained on the target task and optimized for the hardware at hand. In \cite{1} an overparameterized network with multiple parallel candidate operations per layer is used as the base model. Every candidate operation is gated by a binary gate which either prunes or keeps the operation. During architecture search, the binary gates are then trained such that only one operation per layer remains and the targeted memory and latency requirements are met. This is extended in \cite{14} by using shared parameters among individual layers to avoid excessive parameter overhead during training.

In KWS, models using neural networks for keyword classification have become increasingly popular. They are not only easy to train, but they also achieve state-of-the-art performances on image and speech classification tasks. In \cite{3} several models from the literature \cite{15,16,17,18} are evaluated on the Google speech commands dataset \cite{2}. They compare their models in terms of accuracy, memory requirements and number of operations. To allow easy deployment on microcontrollers they train their models using 32 bit float numbers and quantize the weights after training to 8 bit fixed-point numbers. They argue that fixed point numbers have been shown to suffice to run neural networks with minimal loss in accuracy \cite{19,20,21}. We use the results from \cite{3} in our experiments as a baseline for our models.

In binarized neural networks (BNNs) the resolution of both weights and activations is reduced to binary values \{-1,1\} \cite{22} while still retaining state-of-the-art performance on image classification tasks such as MNIST, CIFAR-10 and SVHN. BNNs rely on the straight-through estimator (STE) \cite{23}, \cite{24} which approximates the gradient of non-differentiable or piecewise constant functions, such as quantizers, by the non-zero gradient of some other function. The STE was also used in \cite{22} to substitute the derivative of piecewise-constant functions. Another method for quantizing neural networks involves a Bayesian approach to learn weight distributions over discrete weights \cite{25}. The discrete-weight network is then obtained by selecting the most probable weights. For a comprehensive overview of resource-efficient methods for DNNs, we refer the interested reader to \cite{26}.

III. METHODS

A. Neural Architecture Search

We use convolutional neural networks (CNNs) for keyword classification. Our goal is to find well performing architectures for different computing regimes. To achieve this, we use the multi-objective NAS approach from \cite{1} called ProxylessNAS. In ProxylessNAS, hardware-aware optimization is performed by NAS to optimize the model accuracy and latency on different hardware platforms. However, we optimize for accuracy and number of operations and not for latency. By optimizing for number of operations, the model size is implicitly optimized as well. The trade-off between the accuracy and the number of operations is established by regularizing the architecture loss as explained in Section III-B.

ProxylessNAS constructs an overparameterized network with multiple parallel candidate operations per layer as the base model. A single operation is denoted by \( o_i \). Every operation is assigned a real-valued architecture parameter \( \alpha_i \). The \( N \) architecture parameters are transformed to probability values \( p_i \) by applying the softmax function

\[
p_i = \frac{\exp(\alpha_i)}{\sum_j \exp(\alpha_j)}. \tag{1}
\]

Every candidate operation is gated by a binary gate \( g_i \) which either prunes or keeps the operation. Only one gate per layer is active at a time. Gates are sampled randomly according to

\[
[g_1, g_2, \ldots, g_N] = \begin{cases} 
[1, 0, \ldots, 0] & \text{with prob. } p_1, \\
[0, 1, \ldots, 0] & \text{with prob. } p_2, \\
\ldots & \text{with prob. } p_N.
\end{cases}
\tag{2}
\]

Based on the binary gates and the layer input \( x \), the output of the mixed operation \( m^{\text{Binary}}_i \) (i.e. the output of the layer) is defined as

\[
m^{\text{Binary}}_i = \sum_{i=1}^{N} g_i \alpha_i(x). \tag{3}
\]

During architecture search, the training of the architecture parameters \( \alpha_i \) and the weight parameters of the operations \( o_i \) are performed in an alternating manner. When training weight parameters, the architecture parameters are frozen and binary gates are sampled according to (2). Weight parameters are then updated via standard gradient descent on the training set. When training architecture parameters, the weight parameters are frozen and the architecture parameters are updated on the validation set. Updating the architecture parameters via backpropagation requires computing \( \partial L / \partial \alpha_i \) which is not
defined due to the sampling in (2). ProxylessNAS proposes two methods for estimating the gradient. Method one estimates the gradient of $\partial L/\partial p_i$ as $\partial L/\partial g_i$. This estimation is an application of the STE explained in Section II-C. With this estimation, backpropagation can be used to compute $\partial L/\partial g_i$, since the gates $g_i$ are part of the computation graph and thus $\partial L/\partial g_i$ can be calculated using backpropagation. Method two utilizes REINFORCE \cite{27} to find the optimal binary gates that maximize a certain reward $R(\cdot)$. The reward $R(\cdot)$ is directly proportional to the model accuracy and inversely proportional to the number of operations of the model. We did not observe any benefits of using REINFORCE over the gradient based approach. Therefore, we use the gradient based approach in our experiments to approximate the gradient.

Our overparameterized network, shown in Table I, consist of three stages, (i) an input stage, (ii) an intermediate stage, and (iii) an output stage. Stages (i) and (iii) are fixed to a $5 \times 11$ convolution and a $1 \times 1$ convolution respectively. The network size is lower bounded by the size of stage (i) and stage (iii), which however is negligible regarding the overall model size. We apply batch normalization \cite{28} followed by the ReLU \cite{29} non-linearity as an activation function after the convolutions of stages (i) and (iii). We use mobile inverted bottleneck convolutions (MBCs) \cite{30} as our main building blocks in stage (ii).

Only convolutions from stage (ii) are optimized. MBCs have two learnable parameters, the expansion rate $e$ and the size $k$ of the quadratic $k \times k$ convolution kernel. MBCs consist of three separate convolutions, one $1 \times 1$ convolution followed by a depthwise-separable $3 \times 3$ convolution followed again by a $1 \times 1$ convolution. The first two convolutions use batch normalization and ReLU activation functions. The third convolution only uses batch normalization. The first and third $1 \times 1$ convolution change the number of feature maps by the expansion rate factor of $e$ and $1/e$ respectively. Stride (as stated in Table I) is only applied to the first convolution of each stage. The stride can be different along certain dimensions. Therefore it is parametrized by $(H, W)$, where $H$ is the stride along the height and $W$ is the stride along the width of a certain feature map.

During NAS, we allow MBCs with expansion rates $e \in \{1, 2, 3, 4, 5, 6\}$ and kernel sizes $k \in \{3, 5, 7\}$ for selection. We also include the zero operation. Therefore, our overparameterized network has $\#e : \#k + 1 = 19$ binary gates per layer. For blocks where the input feature map size is equal to the output feature map size we include skip connections. If a zero operation is selected as a block by NAS, the skip connection allows this particular layer to be skipped similar to \cite{1} resulting in an identity layer.

| Stage | Operation | Stride (H, W) | #Channels | #Layers |
|-------|-----------|--------------|-----------|---------|
| (i)   | Conv, $5 \times 11$ | 1, 2         | 72        | 1       |
| (ii)  | MBC[e], $|k| \times |k|$ or Identity | 2, 2       | 72       | 12      |
| (iii) | Conv, $1 \times 11$ | 1, 1         | 144       | 1       |

| Fully connected |

TABLE I: Three stage model used for the KWS task. Stages (i) and (iii) are fixed to a $5 \times 11$ convolution and a $1 \times 1$ convolution respectively. Stage (ii) convolutions are optimized.

where $\text{CE}_{\text{loss}}$ is the cross entropy loss, $\text{ops}_{\text{exp}}$ the expected number of operations, $\text{ops}_{\text{target}}$ the target number of operations and $\beta$ the regularization parameter. The expected number of operations $\text{ops}_{\text{exp}}$ is the overall number of operations expected to be used in the convolutions and in the fully connected layer based on the probabilities $p_i$ of the final network. For stages (i) and (iii) we simply sum the number of operations used in the convolutions and in the fully connected layer. For stage (ii) layers, the expected number of operations is defined as the weighted sum of the numbers of operations used in $o_i$ weighted by the probabilities $p_i$.

Establishing an accuracy/operations trade-off using (4) is usually achieved by fixing $\text{ops}_{\text{target}}$ and choosing $\beta$ such that the number of operations of the final architecture after NAS are close to $\text{ops}_{\text{target}}$. If $\text{ops}_{\text{target}}$ is close to $\text{ops}_{\text{exp}}$, the right term of (4) becomes one thus leaving the $\text{CE}_{\text{loss}}$ unchanged. However, if $\text{ops}_{\text{exp}}$ is larger or smaller than $\text{ops}_{\text{target}}$, the $\text{CE}_{\text{loss}}$ is scaled up or down respectively.

In our work, we focus on obtaining a wide variety of networks with a different number of operations, rather than reaching a certain number of target operations. Therefore, we keep $\text{ops}_{\text{target}}$ fixed while varying $\beta$. Varying $\beta$ while fixing $\text{ops}_{\text{target}}$ resulted in more diverse networks in terms of number of operations than fixing $\beta$ and varying $\text{ops}_{\text{target}}$.

C. Weight Quantization

Our goal is to find resource efficient models for limited resource environments. Therefore, we use weight quantization to reduce the model size in terms of memory consumption even further. Unless noted otherwise, we quantize our model weights to 8 bits during NAS. This allows us to compare our models to the quantized 8 bit models in \cite{31} while also reducing the model size substantially.

We perform quantization similar to \textit{quantize}$^e_k$ in \cite{31}. \textit{quantize}$^e_k$ takes a real-valued input $r_i \in [0, 1]$ and quantizes it to a $k$ bit number $r_o \in [0, 1]$. However, we want to quantize real-valued weights $w \in \mathbb{R}$ to $k$ bit weights $w_q \in [-1, 1]$. We achieve this by extending \textit{quantize}$^e_k$ to

$$w_q = 2 \cdot \left[ \frac{1}{2^k - 1} \min\left( \left[ 2^k - 1 \right] \frac{w + 1}{2} \right) \right]_0^1 - 1 \quad (5)$$

where $[x]^b_0$ is the clamping function

$$[x]^b_a = \max(a, \min(x, b)) \in [a, b]. \quad (6)$$
The real-valued weights are quantized to a set of discrete values \( \{q_1, q_2, \ldots, q_N\} \). The quantizer is uniform since the quantization steps \( q_{i+1} - q_i \) are equal. Non-uniform quantization is used by some methods by applying a linear quantization to the logarithm of the input \([32]\). Furthermore, our quantizer is a Mid-Rise type quantizer which means that the origin is not included in the set of discrete output values. In contrast, a Mid-Tread type quantizer includes the origin in the set of discrete output values.

We compare two techniques for quantization: bit-rounding as a post-processing step and quantization aware training using the STE. Both techniques use (5) to quantize the weights between +1 and -1.

Bit-rounding as a post-processing step is performed after training by simply quantizing the weights according to (5). The STE is used to quantize the weights during training. The STE approximates the gradient of functions that are non-differentiable or whose gradient is zero almost everywhere such as quantization functions. We apply the quantizer from (5) to quantize the weights during the forward pass. During backpropagation, the zero-gradient of the quantizer is replaced by the non-zero gradient of the linear function \( f(x) = x \), i.e., \( f'(x) = 1 \), which essentially passes the gradient through the quantizer. This allows us to train the network while simultaneously quantizing the weights.

Figure 1 illustrates weight quantization using the STE on a typical convolutional layer (without batch normalization). During the forward pass, the quantizer \( Q \) performs the quantization of the weight tensor \( W^l \) according to (5). During the backward pass, the STE replaces the derivative of the quantizer \( Q \) by the derivative of the identity function. In this way, the gradient can propagate back to \( W^l \).

Generally, we observe that quantization aware training with the STE performs better than bit-rounding as a post-processing step (cf. Section IV-D).

### IV. Experiments

#### A. Dataset

We use the first version of the Google speech commands dataset [2]. It consists of 65,000 1-second long audio files sampled with 16 bit at 16 kHz sampling frequency. Every audio file contains one utterance of an English word spoken by one person. In total there are 30 words spoken by thousands of people. The words are grouped into 30 different classes. We follow the procedure of [3] and use the following 10 classes "Yes", "No", "Up", "Down", "Left", "Right", "On", "Off", "Stop" and "Go" from the dataset. Likewise, we also include an "unknown" class which is a blend of randomly selected samples from the remaining 20 classes. Furthermore, a "silence" class is added. The "silence" class is artificially generated and consists of 1-second audio files containing a random slice of audio from a randomly selected noise sample provided by the Google Speech commands dataset. We made sure that the number of samples in the "unknown" class and in the "silence" class is equal to the average number of samples in all 30 classes to obtain equal class sizes. Our test set consists of the keyword samples from the test set and includes the same random selection of samples from the "unknown" and the "silence" class as used in [3] to make our results comparable.

#### B. Experimental Setup

We extract MFCC features from the raw audio streams before performing classification. Unless noted otherwise, we extract 10 MFCC features per 40ms frame. We use a stride length of 20ms which yields a total of 10×51 features per 1 second of audio.

We augment all training samples with a random time shift of up to 100ms. Furthermore, 80% of the training data is augmented with background noise. We use the noise samples from the Google speech commands dataset. It includes environmental sounds, speech, as well as white and pink noise. If a sample is augmented, it is first time shifted and then, in 80% of the cases, overlaid with a 1 second interval of a random noise sample. The desired signal and the noise signal are mixed in a \( (1 - \epsilon) : \epsilon \) ratio using \( \epsilon \sim U(0, 0.1) \).

Before actually performing the architecture search we pretrain the architecture blocks for 40 epochs at a learning rate of 0.05. During pretraining, architecture blocks are randomly sampled and trained on one batch of the training set. Sampling and training repeats until 40 epochs of training are passed. Optimization is performed with stochastic gradient descent using a mini-batch size of 100. After pretraining we perform an architecture search for 120 epochs with an initial learning rate of 0.2. The learning rate is decayed according to a cosine schedule [11].

An architecture is trained until convergence after selection by the NAS procedure to optimize the performance. We use the same hyperparameters as in the architecture search process.
Fig. 2: Test accuracy versus number of operations using multi-objective NAS for varying trade-offs $\beta$. The model size (i.e. memory used to store the weights in bytes) corresponds to the circle size. Numbers above circles represent the model size in bytes for some selected models.

TABLE II: Test accuracy, number of operations and memory requirements of three models obtained using NAS.

| Architecture          | Test Acc. (%) | Operations | Memory |
|-----------------------|---------------|------------|--------|
| Hello Edge DS-CNN [3] | 94.4          | 5.4 M      | 38.6 kB |
| Hello Edge DS-CNN [4] | 94.9          | 19.8 M     | 189.2 kB |
| Hello Edge DS-CNN [5] | 95.4          | 56.9 M     | 497.6 kB |
| Ours (Fig. 3c), $\omega = 0.75$ | 95.0 | 55.6 M | 397.8 kB |
| Ours (Fig. 3b), $\omega = 1.25$ | 98.4 | 19.6 M | 494.8 kB |
| Ours (Fig. 3a), $\omega = 1$ | 96.0 | 23.4 M | 554.0 kB |

C. Efficient Architecture Search

We search for architectures of different sizes by varying the regularization parameter $\beta \in \{0, 1, 2, 4, 8, 16\}$ to obtain a trade-off between the number of operations and accuracy. Furthermore, we kept $\text{ops}_{\text{target}}$ fixed at $20 \cdot 10^6$ during all experiments. By default, we perform quantization aware training using the STE during NAS to quantize the model weights to 8 bits.

Our models have the same number of channels across all layers except for the last $1 \times 1$ convolution where the number of feature maps is doubled with respect to the number of feature maps in the previous layers. We use networks with 72 channels in stage (i) and (ii) and 144 channels in stage (iii) as our base networks. To achieve more diversity, we employ a channel multiplier $\omega$ which scales the number of channels in each layer. We evaluated $\omega \in \{0.75, 1, 1.25\}$ and rounded the resulting number of channels to the closest multiple of 8 [30].

Figure 2 shows the test accuracy versus the number of operations for all models found using NAS. The model size (i.e. memory used to store weights in bytes) corresponds to the circle size. We observe a variety of models from different operation regimes.

We compare three of our models with depthwise-separable convolutional neural network (DS-CNN) models from [3] in Table II. Figure 3 (a), (b) and (c) provide the corresponding network topologies. Inverted bottleneck convolutions are denoted by $MBC[e, k\times k]$ with expansion rate $e$ and kernel size $k$. Expansion rates, kernel sizes and number of layers are determined by NAS. MFCC features at the input are processed first by a $5 \times 11$ convolution which reduces the width by a factor of 2 by means of a strided convolution. The first inverted bottleneck convolution then reduces the height and width by a factor of 2 by means of a strided convolution. The last stage contains a $1 \times 1$ convolution as well as global average pooling followed by a fully connected layer. Individual MBC blocks have skip connections if the output of the block has the same shape as the input of the block. Skip connections are drawn symbolically and are denoted by $\text{id}$. The output of the convolutions are three dimensional tensors, with dimensions $C \times H \times W$, where $C$ is the number of channels, $H$ is the height and $W$ is the width of the corresponding tensor.

DS-CNN models are currently among the best performing models. Still, NAS allows us to find models that match or even outperform the baseline while requiring substantially fewer operations.
Fig. 4: Test accuracy versus number of bits for two weight quantization methods evaluated on our second model from Table II for bit-widths in the range of \{1, 2, \ldots, 8\}. For every bit-width, the model is trained from scratch and quantized according to the quantization method. Results for STE (blue) are obtained by learning quantized weights during training. Results for post-processing quantization (red) are obtained by rounding the weights after training.

D. Weight Quantization

Reducing the model size in terms of memory consumption is not only possible by efficient architectures but also by efficient weight representations. Several methods are known, including weight pruning and weight quantization [26]. We apply weight quantization to reduce our model sizes even further.

We perform several tests where we quantize the weight tensors of our second model from Table II in the range of 8 bit to 1 bit. Note that our models use 8 bit weights by default. The activations are kept at full precision. We investigate the influence of weight quantization on the test accuracy. We compare two different methods for weight quantization as discussed in Section III-C:

- Quantization aware training using the STE.
- Quantization as a post-processing step by rounding parameters of a trained network to a prespecified parameter bit-width.

Figure 4 includes the results and compares the test accuracy of both methods for different bit-widths. We observe that the performance of the post-processing quantization method is only slightly worse than the STE for 8 bits to 5 bits. However, the performance drops rapidly when using fewer than 4 bits. Quantization using the STE on the other hand preserves the performance even for binary weight (1-bit) networks. We observe only a slight drop in performance of around 0.9% when going from 8 bit to 1 bit weights using the STE.

As we have seen, weight quantization using the STE can be employed successfully without any substantial loss in accuracy. Also, note that the training overhead introduced by the STE is only marginal. Training with the STE does not take much longer than conventional training. Post-processing quantization performed worse by comparison but has some advantages. It is easy to implement and it can be performed on arbitrary models without changing the model.

TABLE III: Test accuracy, number of operations and memory requirements (for storing weights) of models obtained by NAS using a different number of MFCCs as features.

| # MFCCs | Test Accuracy (%) | Operations | Memory |
|---------|-------------------|------------|--------|
| 10      | 94.9              | 10.9 M     | 258.8 kB |
| 20      | 96.3              | 27.1 M     | 340.1 kB |
| 30      | 96.2              | 41.4 M     | 348.2 kB |
| 40      | 96.6              | 54.7 M     | 344.7 kB |

E. Varying Number of MFCC Features

For the previous experiments we kept the number of MFCC features at 10 MFCCs. We have seen that using 10 MFCC features is sufficient for achieving a reasonable performance. Here, we aim to explore if using more than 10 MFCC features affects the performance, number of operations and memory requirements of the networks.

To compare performances we run 4 NAS experiments using 10, 20, 30 and 40 MFCCs respectively. As before we select $\beta \in \{0, 1, 2, 4, 8, 16\}$ and search for optimal architectures followed by retraining of the weights. The channel multiplier was kept at $\omega = 1$. In order to compare to the baseline, weight quantization to 8 bits using the STE is performed during training.

Figure 5 shows the results for using 10, 20, 30 and 40 MFCCs for several trade-offs $\beta$. We also provide a comparison of models found by NAS with $\beta = 8$ using 10, 20, 30 and 40 MFCCs in Table III.

We notice a definite improvement of using 20 MFCCs over 10 MFCCs. In particular, one model found by NAS uses 340.1 kB of memory, 27.1 million operations and achieves 96.3 % accuracy which outperforms [3] by a large margin. We include the model structure of this particular network in Figure 3d.

Using 30 MFCCs, we obtained the best performing network with a test accuracy of 96.7% using 1403.3 kB of memory and 155.3 million operations.
V. CONCLUSION

Resource efficient DNNs are the key components in modern keyword spotting (KWS) systems. We show that neural architecture search (NAS) can be used to obtain efficient convolutional neural networks (CNNs) without compromising classification accuracy. The CNN models obtained by NAS achieve state-of-the-art performance while being small enough to fit inside the memory of devices with limited resources such as a microcontroller. To make our results comparable, we performed NAS on the Google speech commands dataset. By using an accuracy/operations trade-off objective for NAS we obtained different models and compared them in terms of accuracy, memory and number of operations. We furthermore showed that weight quantization is a viable option to reduce the memory footprint for storing the CNN weights even further. Even 1 bit weights are sufficient for CNNs without severely degrading the accuracy. We also showed that changing the number of MFCC features can have a substantial impact on the performance of the models.

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