Towards “Zero-buffer” Datacenter Networks

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ABSTRACT

In this paper, we investigate the possibility of building a data center network (DCN) with simplified zero-buffer switches. It exposes a stringent requirement to the traffic control scheme to ensure perfect collision-free between packets. We find it is infeasible, if not impossible, to make a large-scale DCN completely zero buffering. We take a step back and propose Fastpod, a new data center architecture that enables zero buffering in pod scale, which can be expanded with buffered devices. With time synchronization, Fastpod avoids collisions by performing fine-grained centralized control on data packets and coordination-free scheduling on control packets. It leverages an optimistic sending mechanism to reduce the latency overhead induced by the centralized control.

Our preliminary simulation results indicate that Fastpod successfully meets the requirement of collision-free in the zero-buffer pod and maintains similar performance with conventional buffered DCN. It follows the trend of simplifying the network by pushing the functionalities to the edge. Fastpod explores an extreme end of the design spectrum and can be treated as a thought experiment to raise discussion in the community of data center networks.

1. INTRODUCTION

The data center network is the key infrastructure of cloud computing. With the rapid growth of large-scale cloud services, the traffic demands in DCN are doubling roughly every year [39]. However, with the slowdown of Moore’s Law [33], the dividends of each generation of CMOS technology on area reduction and power efficiency are gradually decreasing (10-30% compared to ~50% a decade ago) [34, 410], which leads to a deceleration in the capacity growth of data center switches. The gap between them results in high cost, high power, and low performance.

To continue the scaling of DCN, a natural way is to follow the trend of simplifying the network fabric by pushing the functionalities to the edge with smarter edge devices [46, 22, 16] (e.g. smartNIC, DPU [1], IPU [2]). Nowadays, DCNs are generally built from similar switching devices as the Internet with full functionalities. This introduces unnecessary switch complexities that stress the limited die size and power budget, thus constraining the scalability of switching capacity and radix.

In today’s switch chips, 50% of the total area is attributed to memory (lookup table and packet buffer), 20% to packet processing logic (forwarding and buffer management), and 30% to serial I/O (SerDes) [3, 12]. Recent proposals take the first step on this simplification trend by eliminating stages, logic, and tables with source routing techniques [28, 22] (i.e. “zero forwarding”) or system-switch architectures [46]. Except for the necessary I/O required to remain unchanged, the only complexity in the switch leaves to the packet buffer.

In this context, a natural question appears that “Can we build a simplest DCN with ‘zero-buffer’ switches?”. We refer it as a zero-buffer DCN though the smart edges offer the buffering functionality that can temporarily hold the packets before sending them to the network fabric. Note that simply shrinking the buffer size cannot fully mitigate the complexity. Except for the cost and power benefits, zero-buffer DCN also opens a door to achieve deterministic in-network latency. Ideally, once a packet is injected into the fabric, it can deterministically arrive at the receiver without any latency jitters, since there is no buffer and thus queuing (i.e. the dynamic latency) on the transmission path. Correspondingly, the potential congestion is required to be localized at the network edge. Otherwise, the packets will be dropped when facing collisions since there is no buffer to handle any input/output mismatches (i.e. many-to-one incast).

We find that it is infeasible to make a large-scale DCN (e.g. with 100K+ servers) completely zero buffering since it may require unrealistic computation capability or result in long collisions.
flow completion time (FCT) for short flows (§2). Hence we take one step back and turn to seek a compromising solution that could achieve zero buffering in a (relatively) small-scale pod and explore the possibility to expand it to a large-scale data center.

In this paper, we propose Fastpod, a new data center network architecture with zero-buffer switches. Servers buffer the traffic to be sent at the network edge. In Fastpod, all the traffic is explicitly controlled with time synchronization. Specifically, all the data transfers are centralized controlled by an arbiter to ensure collision-free between data packets (§3.1). To avoid collisions that involve control packets, Fastpod reserves gaps between data packets and controls the sending time of control packets so that they can be inserted into the gaps at the zero-buffer switches (§3.2). To mitigate the latency overhead induced by centralized control, Fastpod leverages an optimistic sending mechanism that allows the flows to be sent without scheduling when the egress link of the host is idle (§3.3).

Our preliminary simulation results indicate that Fastpod successfully meets the requirements of collision-free in the zero-buffer pod and maintains similar performance with conventional buffered DCN. To the best of our knowledge, Fastpod is the first architecture that enables server-to-server zero buffering with electrical packet switches in pod scale. With Fastpod, we seek to raise discussion in the community on whether or not current methods of building data center networks are worthy of complexity.

2. MOTIVATION

To motivate zero buffering DCN, we start this section by (re-)emphasizing its potential benefits and opportunities from three perspectives: cost, performance, and trend. Then we consider how to adapt conventional approaches to enable a zero-buffer DCN, as well as the limitations of those approaches. Except for zero buffering, the resulted solution is also required to be scalable and performant.

2.1 Why zero buffering?

CMOS dependency, cost and OAM^1. As the power and area gains become harder to sustain the historic doubling every generation [14][4][10], the CMOS-based electrical switches are gradually approaching the limits of free scaling. In modern switch chips, the memory as well as control logics of forwarding and buffering take about 50% of die size and power dissipation [3][12][8]. Simplifying the switch with zero buffering, along with zero forwarding, can be a promising direction to deal with this challenge.

This simplification can potentially reduce the CMOS process dependency of chip manufacturing, which means chips with the Nth generation process (e.g. 7nm) can achieve similar performance with those manufactured with the N+1th generation process (e.g. 5nm). In other words, with the same generation process, the simplified chips can save 50% die area and power consumption, which can dramatically reduce both the CAPEX and the OPEX of the data center networks. When the die size is kept unchanged, the total bandwidth offered by the chip can be doubled. In conventional DCN, more than 50% of total failures come from abnormal routing and buffering [19], which can be avoided in a simplified zero-buffer DCN so that greatly reduce the OAM costs.

Deterministic low latency: The end-to-end latency is often defined as the time a packet takes to traverse the network from the sender to the receiver, including both the propagation and switch latency. When it comes to closed environments like datacenters, the latency is dominated by the switch latency mainly contributed by buffering, routing algorithm, and arbitration. Deterministic low latency is a crucial performance requirement, especially for mission-critical and latency-sensitive applications where microseconds matter (e.g., financial networking) [41][44].

In a zero-buffer DCN, the end-to-end latency can be deterministically low. On the one hand, zero buffering means there won’t be dynamic latency, which is often contributed by the queueing delay in conventional buffered networks. On the other hand, the static processing latency at switch can also be reduced since the packet can bypass all the forwarding (i.e. table lookup) and buffering (i.e. queue schedule, enter/leave buffer) operations at switches of multiple network layers.

Future optical DCN: The design of zero-buffering DCN is a natural fit for cut-through switching fabrics and more importantly can be treated as an exploration for future generations of hybrid electrical/optical or all-optical DCNs [43][18][30][29][10], which are inherently zero buffering.

Small buffers vs zero buffer: Although there could be many opportunities to achieve zero buffering, readers may still wonder whether or not we really need zero buffer instead of a more modest goal with small buffers. We think the answer is yes, and argue that the concern does not lie in the size but the existence of the buffer.

On one hand, according to our switch chip vendor, it is surprising that the buffer management logic takes 2x more die area than that of the buffer itself. Simply shrinking the buffer size can not fully cope with the problem since the buffer management logic, the power of active RAM [12], and the static write/read latency are always there as long as the buffer exists. On the other hand, prior works (e.g. NDP [20], Homa [22]) have demonstrated that small buffers are crucial for statistical multiplexing to achieve high throughput in data center networks. However, as we will show in the following, with a properly designed scheduling mechanism, a zero-buffer DCN can achieve similar performance as the buffered ones, even without considering the potential bandwidth benefit from the chip simplification.

^1 Short for Operations, Administration and Management.
2.2 Strawman solutions

The key to enabling zero buffering is to eliminate congestion in switches, including temporary many-to-one port collision and long-term port congestion. This requires precise control on both packet scheduling and transmission path, which fails the conventional asynchronous congestion control along with load balancing methods for its coarse control granularity. In our opinion, since the traffic demands arrive dynamically, the only possible way to achieve zero buffering is to proactively control the sending behavior of each endpoint according to a global consensus, and thus any unscheduled operation outside the consensus will result in a collision. In this way, the synchronous schemes that allocate fine-grained network resources with clock synchronization are very promising.

Centralized scheduling approaches (e.g., Fastpass [35], datacenter TDMA [22]) rely on an arbiter with global information to allocate timeslot and transmission path for each flow, which can theoretically avoid collisions between scheduled data packets. However, the control packets (i.e., request and response messages) exchanged between the arbiter and hosts are sent in an unscheduled on-demand manner, which may collide with each other or with scheduled data packets, thus missing the requirement of zero buffering. Even this can be avoided by explicitly scheduling control packets (as we show later), the scalability is also constrained by the computation capability of the arbiter since it is required to compute schedules for all the (100K+) endpoints without sacrificing the throughput. Besides, short flows have to endure the scheduling latency overhead, especially under low traffic load.

Schedule-less approaches (e.g., RotorNet [30], Shool [38], Opera [29], Sirius [10]) preserve link resources for each pair of target nodes with circuit switches that are reconfigured according to a predefined static schedule in a round-robin manner, which eliminates the need for a centralized scheduler and inherently supports zero buffering. With a detour routing scheme (e.g., Valiant load balancing [13] [40]), they guarantee the worst-case network throughput across any traffic patterns. However, their scalability is limited by the flatten topology and the radix of (especially optical) circuit switches since they are required to connect all the servers to ensure end-to-end zero buffering. A potential extension is to leverage a multi-layer Clos network with low-radix to connect all the endpoints. This customization will result in high latency overhead due to long round-robin epochs. The length of an epoch is determined by the total node number, the node’s degree, and the length of each time slot. For example, consider a DCN containing 100K servers, each with 4 25Gbps channels. If a time slot is at least 64 bytes long, an epoch, i.e., the worst-case extra waiting time, will last for ~500us, which will dramatically increase the FCT of short flows.

2.3 Towards a feasible zero-buffering DCN

Based on the analysis above, it is infeasible to maintain all the switches zero buffering in a DCN with such a large scale. Since the challenge primarily comes from scalability, here we take one step back and turn to seek a compromising solution that could achieve zero buffering in a (relatively) small-scale pod, and explore the possibility to expand it to the large-scale data center with buffered devices. This way, the scope of servers that require precise control is limited within a pod, while the benefit of latency and cost from zero buffering is still kept for most of the traffic (i.e., intra-pod flows [37] [23] [11]) and switches, respectively.

3. DESIGN

Today’s data center often adopts a multi-layer Clos network as the topology. In the following, we take a pod from a k-port Fattree [5] as an example to show how Fastpod achieves zero buffering and low latency. We also provide a potential solution to expand our zero-buffer pod to the datacenter scale. The Fastpod’s architecture is shown in Fig. 1.

![Figure 1: FastPod architecture with k-port Fattree topology.](image-url)

3.1 Design overview

In Fastpod, servers are organized as several zero-buffer pods and their sending behavior is controlled by centralized arbiters, one for each pod. The switches inside the pod (i.e., the aggregation (Agg) and Top-of-Rack (ToR) switches) have no buffer and thus no buffer management logic. Besides, we use source routing to simplify these switches to be free of lookup tables and complex forwarding logic [28] [22]. We assume servers with smart edge devices use virtual output queues (VOQs) to queue packets from upper-layer applications. Each destination host has an assigned VOQ.

Every time the Fastpod agent at the host receives the traffic demand, it sends a request-to-send (RTS) message to the arbiter, specifying the destination and the number of bytes. The arbiter processes each RTS, performs scheduling, and sends the schedule (SCHD) message back to the sender, which contains the timeslot, destination, and path. The sender executes the scheduling result on the corresponding time slot. With all the demand information, the arbiter can obtain the schedule that yields the collision-free property for scheduled data packets [35]. The concrete scheduling process involves...
Collision at the receiver side. As shown in Fig. 2(b) the arbiter needs to send the SCHD packets to multiple hosts under the same ToR switch. These SCHDs may have the same destination as the scheduled data packets, which results in collision at the output port connected to the host if they arrive at the same time.

**Gap-filling mechanism.** The root cause of these problems is that control packets are sent in an unscheduled on-demand manner. To deal with these problems, we design a gap-filling mechanism to explicitly arrange the transfer of control packets so that they can be strictly staggered. As shown in Fig. 3 we divide one time slot into \(N - 1\) data slots so that there will be \(N\) gaps to be filled by the control packets, i.e. control slot.

As shown in Fig. 4, in each time slot, the sender sends its RTS at the \(i\)th control slot and keeps the \(j\)th gap empty for SCHD, where \(i\) and \(j\) are the sender’s and receiver’s relative number of all the hosts under the same ToR respectively. The arbiter sends SCHD to the host at a specific time so that the SCHD can fill the gap reserved by the sender. To reduce the overhead, we do not reserve the unselected gap. Therefore in the view of the host, a time slot comprises \(N - 1\) data packets and 2 control packets (one RTS and one SCHD). Note that with the scheduling results known by both the sender and arbiter, the position of two gaps can be determined locally without extra coordination. \(N\) is set as the number of hosts under a ToR, to ensure every host can communicate with the arbiter once per timeslot without collision. This way, the RTSs/SCHDs from/to those hosts are staggered.

In principle, the arbiter can fill the SCHD at the RTS gap to avoid collision, since at the receiver side the RTS has already been sent to the arbiter, leaving the control slot of RTS idle. However, the arbiter can only fill one gap with the SCHD when multiple hosts receive the traffic stream with the RTS gap at the same position (i.e. they are from different ToR but have the same relative number). This explains our two-gap design.

To ensure gaps with the different position will not overlap, we restrict that: 1) RTS and SCHD packets are with the same size and pack the upper layer packets into fixed-size cells (although we still call it as packet in the following paper); 2) the total size of the two control packets is smaller than the size of a single data packet. Besides, the host and arbiter need to adjust their sending time to compensate for the potential difference in fiber length [10].

### 3.3 Optimistic sending

Fastpod leverages a centralized control approach to avoid collisions between data packets. In a light load network, the
short flows need to bear the additional delay of communication with the arbiter, which could dramatically defer their completions. Inspired by Aeolus [21], we use an optimistic sending mechanism to allow flows sending before receiving the SCHD. Note that short flows of the incast cannot benefit from this mechanism. On the contrary, the conflicts between them are scheduled by the arbiter.

Sending with state judgment. When a new demand arrives, the host sends RTS for it to the arbiter as usual and tries to optimistically send it as unscheduled packets with a randomly chosen path. In principle, the new demand is allowed to be sent as long as its VOQ is empty (i.e. there is no traffic to the same destination as this demand), since the host has no information about the load condition of the whole network. With Fastpod’s slotted operation, the collision possibility is time slot dependent and can be inferred locally by the received scheduling result.

The demand is allowed to be optimistically sent until an SCHD is received after a time elapse of the RTT between the host and the arbiter, including the scheduling time at the arbiter. This implies two cases. If this demand has been scheduled, it should be sent according to the scheduling result. Otherwise, the link resources required by this demand may have been allocated to other demands, which could raise potential conflicts if the host insists to send. An SCHD received before that time provides no information about the current demand and thus the host can still be optimistic to send this demand, as long as the egress link is idle. When multiple demands compete, the earliest demand will get the chance to send.

Selective dropping at switches. The unscheduled packets may collide with other unscheduled or scheduled packets at the switch. The switch intentionally drops the unscheduled packets to ensure the reliability of the scheduled traffic.

Recovery with redundancy. Since the RTT between the arbiter and the host is often smaller than the host-to-host RTT, the sender can not obtain the acknowledgment information from the receiver before receiving the SCHD. At this time, to ensure reliable transmission, the sender resends all the unscheduled data after receiving the corresponding SCHD. Fastpod relies on the higher-layer protocol to perform de-redundancy.

3.4 Expansion to the data center scale

Two-round scheduling. To achieve scalability, we connect each pod with buffered core switches, and leverage a hybrid control scheme to deal with both intra- and inter-pod transfers. Specifically, the intra-pod traffic is synchronously scheduled by the arbiter of its pod, and the inter-pod traffic is asynchronously scheduled with two rounds by the arbiter of source pod and destination pod respectively. For inter-pod traffic, it is first sent to the core switches according to the schedule of the source-pod arbiter, which takes the destination pod as the matching target to perform timeslot allocation and chooses one of the core switches as the transit node. The core switch sends RTS for this traffic to the destination-pod arbiter, and then sends the traffic to the destination host as scheduled. In this way, the arbiter can constrain the scale of the scheduling problem to the number of servers in the pod, thereby converting a large-scale global scheduling task into two local ones. What’s more, through two rounds of scheduling, the property of collision-free in each pod is maintained.

Flow control of core switches. Acting as transit nodes, core switches temporarily buffer the inter-pod traffic until receiving the scheduling result. Each port of the core switch is connected to a Pod. Multiple core switches play the same role and are required to be load balanced. However, the core switches are independently selected by arbiters in different pods, which could result in queue buildup and buffer overflow. We use a backpressure flow control mechanism to restrict traffic through the core switch. When the total buffer of the core switch is about to overflow, all the ports are back pressured so that the pods are not allowed to transfer any traffic through this core switch. Besides, when the queue length of a output port is too long, back pressure is performed so that only the traffic to that pod is not allowed. The back-pressure signal informs all arbiters through the RTS packet. The RTS packet carries a list of destination pods for which the source pod is allowed to send data, and the arbiter of the source pod performs scheduling accordingly.

Arbiter customization. The arbiter needs to schedule intra-pod and inter-pod traffic at the same time, and maintain their fairness to prevent starvation. When there is only intra-pod
traffic, the rearrangeable non-blocking property of Clos network [14] allows the arbiter to perform timeslot allocation separately from path selection. However, when dealing with inter-pod traffic, both the core switch and the server participates in the scheduling, which breaks the property and thus requires further algorithm design.

We leave further optimization and simulation of inter-pod transfers as our future work.

4. DISCUSSION

**Time synchronization.** To avoid collision inside the zero-buffer pod, servers that belong to a pod are required to be precisely time-synchronized to enable Fastpod’s slotted operation. On the contrary, different pods can operate asynchronously since core switches have a buffer to absorb the time difference between pods. The core switches need to maintain clocks and times for all pods, so that they can send traffic at the right time to the corresponding pod. To absorb the synchronization error, we set a “guard band” between each time slot. Besides, we enlarge the control slot according to the synchronization error to enable successful gap filling of control packets. Note that this will incur negligible overhead since we only add three guard bands (i.e., one for the whole time slot and two for control slot) to a time slot of more than \(N - 1\) packets long.

Existing synchronization protocols [26, 24, 18] can achieve up to nanoseconds accuracy, but often require extra control messages. On the contrary, by leveraging Fastpod’s cyclic communication between the arbiter and all the hosts, the host can be synchronized with the arbiter. The basic idea is that our zero buffering fabric makes it possible to accurately and efficiently measure the one-way delay (OWD) between the arbiter and the host. Specifically, in each time slot, the arbiter will send an SCHD to each host with its local timestamp. After receiving the SCHD and obtaining the current timestamp, the host can adjust their relative time offset with the newly measured OWD by subtracting the OWD measured in the startup phase.

**Failure detection.** To detect failures, Fastpod relies on the fact that a server sends an RTS to the arbiter once every time slot, even if there is no traffic to send. The links that belong to the path between the arbiter and the servers can be detected as a failure if the RTS does not arrive on time. For the links above ToR, the host can report a flag in the RTS to the arbiter indicating whether or not it received the scheduled packets. The arbiter can use this information to compare with previously stored scheduling results to infer whether and where a failure occurs. To deal with arbiter failure, Fastpod leverages a backup arbiter with a similar mechanism with Fastpass [36].

5. EVALUATION

In this section, we will present our preliminary results for evaluating the performance of Fastpod compared to other state-of-the-art schemes in the pod scale. Our simulation is based on YAPS simulator [7] [11].

**Topology:** We simulate a pod of an 8-port FatTree topology. All links have 100Gbps capacity and the per-link propagation delay is 1 \(\mu s\). All the switches work in cut-through mode. For Fastpod, the switches have no buffer and the pod is controlled by an arbiter connected to all ToR switches.

**Workload:** We generate flows from a realistic workload distribution collected from a Microsoft cluster [11], using a Poisson arrival process for a specified target network load. This workload is highly skewed: most of the flows are small whereas most of the bytes lie in the long flows. All the flows follow an all-to-all communication pattern that the source and the destination of a flow are chosen randomly. We run 10,000 flows for each simulation setting.

**Schemes:** We compare Fastpod with DCTCP [7], pFabric [9] and Fastpass [35]. Their parameters are tuned according to suggestions of the original papers. We choose pFabric for comparison because it is widely used as a benchmark and its performance is believed to be near-optimal. Fastpod, each time slot consists of three 1500-byte data packets and two 64-byte control packets since each ToR connects to four hosts. In addition, we assume perfect time synchronization for Fastpod and Fastpass.

**Performance metrics:** We use slowdown of flow completion time [9, 32, 17] as the main performance metric. We also measure the goodput and packet latency for further analysis.

**Result analysis:** We start by examining if Fastpod achieves the collision-free property by checking the port occupation of each switch when disables the optimistic sending mechanism. We found that all the control packets are successfully inserted between adjacent data packets at a switch, indicating no collision occurs (not shown).

To show Fastpod’s ability of providing low-latency communication for latency-sensitive flows, Fig. 5(a) reports the 99th percentile FCT slowdown for short flows (flow size < 10KB) under varying loads. Fastpod delivers consistent lower tail FCT across all network loads, and its performance is similar, if not even better, to pFabric: the slowdown is never worse than 4 even at 100% network load. DCTCP and Fastpass have considerably higher slowdown than Fastpod and pFabric. Fastpod achieves this by pushing all the congestion to the host, so as to provide the lowest in-network latency without any queueing delay. This is an important result because it shows that Fastpod can achieve at least similar performance of a conventional buffered DCN at just a fraction of power and cost.

Fig. 5(b) shows the average goodput under varying network load. Fastpod achieves similar goodput as that of other schemes. This confirms that Fastpod’s precise control does not incur too much overhead. Note that with simplified switches, Fastpod can potentially provide more bandwidth than conventional DCNs so that achieves higher goodput.

Finally, we plot the cumulative distribution of in-network latency under an extreme 100% network load, as shown in Fig. 5(c). We measure this latency by the duration from
the packet’s leaving to its arrival at the servers. Since there is no buffer and thus no dynamic latency, Fastpod achieves deterministic in-network latency, while other schemes may encounter queuing at the switches. Comparing with those schemes, about 20% of Fastpod’s packets suffer from higher latency. This is because we require them to be always routed through two tiers of the topology, even if the nodes are under the same ToR. This ensures that all the packets belonging to the same time slot will arrive at the switch at the right time.

6. CONCLUSION AND FUTURE WORK

In this paper, we present Fastpod, a new data center network architecture with extremely simple switches. We remove the packet buffer along with the buffer management logic from the switches. The buffering functionality is pushed to the hosts. We present algorithms to enable collision-free property in pod scale, and mitigate the scheduling latency overhead. This paper shows a particular design to enable a zero-buffer data center network. We believe that Fastpod, or reducing the complexity of switches in general, is a promising direction to pursue for future data center networks.

In the next, we will further explore and optimize our preliminary solutions for inter-pod transfers, and demonstrate that while preserving all the properties of zero buffering, this expansion can generally maintain the performance. In addition, we will focus on implementing our solution using FPGAs in a real testbed environment to show its feasibility, and provide the cost analysis based on the implementation.

7. REFERENCES

[1] Data processing units (dpus). https://www.nvidia.com/en-us/networking/products/data-processing-unit/ Accessed June 26, 2020.
[2] Intel unveils infrastructure processing unit. https://www.intel.com/content/www/us/en/newsroom/news/infrastructure-processing-unit-data-center.html Accessed June 26, 2020.
[3] Programmable data plane at terabit speeds. https://opennetworking.org/wp-content/uploads/2020/12/p4_d2_2017_programmable_data_plane_at_terabit_speeds.pdf Accessed June 26, 2020.
[4] Tsmc reveals 6 nm process technology: 7 nm with higher transistor density. https://www.anandtech.com/show/14228/tsmc-reveals-6-nm-process-technology-7-nm-with-higher-transistor-density Accessed June 26, 2020.
[5] M. Al-Fares, A. Loukissas, and A. Vahdat. A scalable, commodity data center network architecture. ACM SIGCOMM, 2008.
[6] M. Alizadeh, T. Edsall, S. Dharmapurikar, R. Vaidyanathan, K. Chu, A. Fingerhut, V. T. Lam, F. Matus, R. Pan, N. Yadav, et al. Conga: Distributed congestion-aware load balancing for datacenters. In ACM SIGCOMM, 2014.
[7] M. Alizadeh, A. Greenberg, D. A. Maltz, J. Padhye, P. Patel, B. Prabhakar, S. Sengupta, and M. Sridharan. Data center tcp (dctcp). In ACM SIGCOMM, 2010.
[8] M. Alizadeh, A. Kabbani, T. Edsall, B. Prabhakar, and M. Yasuda. Less is more: Trading a little bandwidth for ultra-low latency in the data center. In UseNix Conference on Networked Systems Design and Implementation, 2012.
[9] M. Alizadeh, S. Yang, S. Sharif, S. Katti, N. McKeown, B. Prabhakar, and S. Shenker. pfabric: Minimal near-optimal datacenter transport. ACM SIGCOMM, 2013.
[10] H. Ballani, P. Costa, R. Behrendt, D. Cleherode, I. Haller, K. Joziwk, F. Karinou, S. Lange, K. Shi, B. Thomsen, et al. Sirius: A flat datacenter network with nanosecond optical switching. In ACM SIGCOMM, 2020.
[11] T. Benson, A. Akella, and D. A. Maltz. Network traffic characteristics of data centers in the wild. In ACM SIGCOMM, 2010.
[12] P. Bosshart, G. Gibb, H.-S. Kim, G. Varghese, N. McKeown, M. Izzard, F. Mujica, and M. Horowitz. Forwarding metamorphosis: Fast programmable match-action processing in hardware for sdn. ACM SIGCOMM, 2013.
[13] C.-S. Chang, D.-S. Lee, and Y.-S. Jou. Load balanced birkhoff–von neumann switches, part i: One-stage buffering. Computer Communications, 25(6):611–622, 2002.
[14] J. Duato, S. Yalamanchili, and L. Ni. Interconnection networks. Morgan Kaufmann, 2003.
[15] N. Farrington, G. Porter, S. Radhakrishnan, H. H. Bazzaz, V. Subramanya, Y. Fainman, G. Papen, and A. Vahdat. Helios: a hybrid electrical/optical switch architecture for modular data centers. In Proceedings of the ACM SIGCOMM 2010 Conference, pages 339–350, 2010.
[16] D. Firestone, A. Putnam, S. Mundkur, D. Chiu, A. Dabagh, M. Andrewartha, H. Angepat, V. Bhanu, A. Caulfield, E. Chung, et al. Azure accelerated networking: Smartnics in the public cloud. In USENIX NSDI, 2018.
[17] P. X. Gao, A. Narayani, G. Kumar, R. Agarwal, and S. Shenker. Phost: Distributed near-optimal datacenter transport over commodity network fabric. In ACM CoNEXT, 2015.
[18] Y. Geng, S. Liu, Z. Yin, A. Naik, B. Prabhakar, M. Rosenblum, and A. Vahdat. Exploiting a natural network effect for scalable, fine-grained clock synchronization. In USENIX NSDI, 2018.
[19] R. Govindan, I. Minei, M. Kallahalla, B. Koley, and A. Vahdat. Evolve or die: High-availability design principles drawn from google’s network infrastructure. In Proceedings of the 2016 ACM SIGCOMM Conference, pages 58–72, 2016.
[20] M. Handley, C. Raiciu, A. Agache, A. Voinescu, A. W. Moore, G. Antichi, and M. Wójcik. Re-architecting datacenter networks and stacks for low latency and high performance. In ACM SIGCOMM, 2017.
[21] S. Hu, W. Bai, G. Zeng, Z. Wang, B. Qiao, K. Chen, K. Tan, and Y. Wang. Aeolus: A building block for proactive transport in datacenters. In ACM SIGCOMM, 2020.
[22] X. Jin, N. Farrington, and J. Rexford. Your data center switch is trying too hard. In ACM SOSP, 2016.
[23] S. Kandula, S. Sengupta, A. Greenberg, P. Patel, and R. Chaiken. The nature of data center traffic: measurements & analysis. In ACM SIGCOMM, 2009.
[24] P. G. Kannan, R. Joshi, and M. C. Chan. Precise time-synchronization in the data-plane using programmable switching asics. In ACM SOSP, 2019.
[25] G. Kumar, N. Dukkipati, K. Jung, H. M. Wassel, X. Wu, B. Montazeri, Y. Wang, K. Springborn, C. Alfeld, M. Ryan, et al. Swift: Delay is simple and effective for congestion control in the datacenter. In ACM SIGCOMM, 2020.
[26] K. S. Lee, H. Wang, V. Shrivastav, and H. Weatherspoon. Globally synchronized time via datacenter networks. In ACM SIGCOMM, 2016.
[27] Y. Li, R. Miao, H. H. Liu, Y. Zhuang, F. Feng, L. Tang, Z. Cao, M. Zhang, F. Kelly, M. Alizadeh, et al. Hpccc: high precision congestion control. In ACM SIGCOMM, 2019.
[28] Y. Li, D. Wei, X. Chen, Z. Song, R. Wu, Y. Li, X. Jin, and W. Xu. Dumbnet: a smart data center network fabric with dumb switches. In ACM EuroSys, 2018.
[29] W. M. Mellette, R. Das, Y. Guo, R. McGuinness, A. C. Snoeren, and G. Porter. Expanding across time to deliver bandwidth efficiency and low latency. In USENIX NSDI, 2020.
[30] W. M. Mellette, R. McGuinness, A. Roy, A. Forencich, G. Papen, A. C. Snoeren, and G. Porter. Rotornet: A scalable, low-complexity, optical datacenter network. In ACM SIGCOMM, 2017.
[31] R. Mittal, V. T. Lam, N. Dukkipati, E. Blem, H. Wassel, M. Ghobadi, A. Vahdat, Y. Wang, D. Wetherall, and D. Zats. Timely: Rtt-based congestion control for the datacenter. ACM SIGCOMM, 2015.
[32] B. Montazeri, Y. Li, M. Alizadeh, and J. Ousterhout. Homa: A receiver-driven low-latency transport protocol using network priorities. In ACM SIGCOMM, 2018.
[33] G. E. Moore. Cramming more components onto integrated circuits. Proceedings of the IEEE, 86(1):82–85, 1998.
[34] S. K. Moore. Another step toward the end of moore’s law: Samsung and tsmc move to 5-nanometer manufacturing-[news]. IEEE Spectrum, 56(6):9–10, 2019.
[35] J. Perry, A. Ousterhout, H. Balakrishnan, D. Shah, and H. Fugal. Fastpass: a centralized” zero-queue” datacenter network. In ACM SIGCOMM, 2014.
[36] J. Perry, A. Ousterhout, H. Balakrishnan, D. Shah, and H. Fugal. Fastpass: A centralized” zero-queue” datacenter network. In ACM SIGCOMM, 2014.
[37] A. Roy, H. Zeng, J. Bagga, G. Porter, and A. C. Snoeren. Inside the social network’s (datacenter) network. In ACM SIGCOMM, 2015.
[38] V. Shrivastav, A. Valadarsky, H. Ballani, P. Costa, K. S. Lee, H. Wang, R. Agarwal, and H. Weatherspoon. Shoal: A network architecture for disaggregated racks. In USENIX NSDI, 2019.
[39] A. Singh, J. Ong, A. Agarwal, G. Anderson, A. Armistead, R. Bannon, S. Boving, G. Desai, B. Felderman, P. Germano, et al. Jupiter rising: A decade of clos topologies and centralized control in google’s datacenter network. ACM SIGCOMM, 2015.
[40] L. G. Valiant and G. J. Brebner. Universal schemes for parallel communication. In Proceedings of the thirteenth annual ACM symposium on Theory of computing, pages 263–277, 1981.
[41] B. Vamanan, J. Hasan, and T. Vijaykumar. Deadline-aware datacenter tcp (d2tcp). ACM SIGCOMM, 2012.
[42] B. C. Vattikonda, G. Porter, A. Vahdat, and A. C. Snoeren. Practical tdma for datacenter ethernet. In ACM EuroSys, 2012.
[43] G. Wang, D. G. Andersen, M. Kaminsky, K. Papagiannaki, T. E. Ng, M. Kozuch, and M. Ryan. c-through: Part-time optics in data centers. In Proceedings of the ACM SIGCOMM 2010 Conference, pages 327–338, 2010.
[44] C. Wilson, H. Ballani, T. Karagiannis, and A. Rowtron. Better never than late: Meeting deadlines in datacenter networks. ACM SIGCOMM, 2011.
[45] Y. Zhu, H. Eran, D. Firestone, C. Guo, M. Lipshteyn, Y. Liron, J. Padhye, S. Raindel, M. H. Yahia, and Z. Ming. Congestion control for large-scale rdma deployments. ACM SIGCOMM, 2015.
[46] N. Zilberman, G. Bracha, and G. Schzukin. Stardust: Divide and conquer in the data center network. In USENIX NSDI, 2019.
[47] N. Zilberman, A. W. Moore, and J. A. Crowcroft. From photons to big-data applications: terminating terabits. Philosophical Transactions of the Royal Society A: Mathematical, Physical and Engineering Sciences, 374(2062):20140445, 2016.