Robust Offset-Cancellation Sensing-Circuit-Based Spin-Transfer-Torque Nonvolatile Flip-Flop

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ABSTRACT Nonvolatile flip-flop (NV-FF) based systems can be effectively implemented in battery-limited internet of things (IoT) applications due to their zero standby power consumption and instant ON/OFF characteristics. Among various NV-FFs, spin-transfer-torque magnetic tunnel junction based NV-FFs are the most applicable due to their nonvolatility, high endurance, complementary metal-oxide-semiconductor (CMOS) compatibility, scalability, and rapid sensing and write speed due to its low resistance. However, they are subject to a degraded sensing margin for restoring operation with technology shrinks because of the increased process variation and reduced supply voltage. This paper proposes a novel NV-FF with a significantly superior offset-tolerance and reduction in read current ($I_{\text{read}}$) that produces read disturbance in comparison to state-of-the-art NV-FFs. Monte Carlo HSPICE simulation results based on industry-compatible 65-nm model parameters revealed that the proposed NV-FF can achieve a three-order improvement in the restore yield and a two-order reduction in the $I_{\text{read}}$ when compared with state-of-the-art NV-FFs.

INDEX TERMS Charge pump, magnetic tunnel junction (MTJ), nonvolatile flip-flop (NV-FF), offset-cancellation, process variation, read disturbance, restore yield, spin-transfer-torque (STT), standby power.

I. INTRODUCTION

Recently, nonvolatile flip-flop (NV-FF)-based systems (NV-System) have been regarded as a potential substitute for conventional volatile systems [1]–[10]. This is mainly because the NV-System enables 1) zero standby power consumption by switching OFF the power in standby mode, thereby saving power; 2) instant-ON from the power-down conditions, thereby improving user experience and saving power; 3) instant-OFF to the standby mode, thereby power saving and eliminating the need for external nonvolatile memory; and 4) the prevention of sudden power failures, thereby improving its reliability and resulting in cost/area saving, as large tantalum capacitors are not required.

Among a variety of NV-FF implementations, NV-FFs that employ spin-transfer-torque magnetic tunnel junctions (STT-MTJs) are the most applicable due to their characteristics of nonvolatility, high endurance, long retention times, complementary metal-oxide-semiconductor (CMOS) compatibility, scalability, and no area overhead as a result of stacking above the MOS transistor. The STT-MTJ based NV-FF has four operation modes. In the normal FF mode, it acts as a conventional volatile FF. In the backup mode, it stores the computing data in the STT-MTJs. In the standby mode, the power of the NV-system is completely switched OFF to achieve zero standby power. In the restore mode, it restores the stored data from the STT-MTJs to the FF core. Moreover, it should be noted that the design of the NV-FF should not degrade the performance of the normal FF mode, given that the normal FF mode operation is the predominant operation in the NV-System, whereas the restore and backup mode operations occur infrequently in internet of things (IoT) applications.

Although the STT-MTJ based NV-FFs demonstrate the abovementioned advantages, they are subject to a degraded sensing margin for restoring operations with technology shrinks because of the increased process variation and reduced supply voltage ($V_{\text{DD}}$). Moreover, this is exacerbated when $V_{\text{DD}}$ is further reduced until near-threshold voltage region for ultralow power IoT applications. The size-increase strategy typically employed for the conventionally used
merged latch and sensing circuit (MLS) structure (see Fig. 1(a)) to ensure tolerance to the process variation increases the parasitic capacitance of the slave latch, thus resulting in the performance degradation of the normal FF mode [3], [5], [10].

To overcome this problem, Ryu et al. [3] proposed a separated latch and sensing circuit (SLS) structure, as shown in Fig. 1(b). By adding a separate sensing circuit at the cost of the area overhead, the sensing circuit can be optimized without the degradation of the slave latch operation, thus leading to an improvement in the sensing margin of the restore mode and the performance of the normal FF mode. Song et al. [10] proposed an offset-cancellation sensing-circuit (OCSC)-based NV-FF, which is insensitive to the offset voltage due to the process variation. By employing the offset-cancellation technique in the sensing circuit, the sensing margin was improved, thereby resulting in the energy saving of the restore mode and area reduction. However, the abovementioned NV-FFs were still highly sensitive to the process variations.

This paper presents a novel NV-FF with a significantly higher offset-tolerance characteristic based on the SLS structure, in comparison with the state-of-the-art NV-FF [10]. The remainder of this paper is organized as follows. Section II describes the proposed NV-FF. Section III presents the simulation results and comparison, followed by the conclusions in Section IV.

II. PROPOSED NV-FF

Fig. 2 presents the circuit diagram of the proposed NV-FF. To independently optimize the sensing circuit and flip-flop core, the proposed NV-FF is based on the SLS structure. With respect to the sensing circuit, the only differences between the proposed NV-FF and state-of-the-art NV-FF [10] are 1) the inclusion of two NMOSs (NL2 and NR2), which are controlled by a supply voltage (VDDH) higher than the normal VDD and 2) reverse-connected MTJ A and MTJ B [11]. However, these differences significantly improve the effectiveness of offset cancellation and reduce the read disturbance in the restore mode. The requirement of VDDH may create design complexity when an extra power rail is needed. This paper gives a solution to generate the VDDH signal without extra power rail by using a simple charge pump, which will be described later.

The restore mode operation of the proposed NV-FF consists of the following four phases: precharge, offset-cancelling, re-precharge, and comparison. In the precharge phase (phase1, P1), the gate voltages of NL and NR reach VDD. Thus, the two capacitors (CSA_L, CSA_R) are precharged to VDD. In the offset-cancelling phase (phase2, P2), based on the diode-connected configuration, the precharged voltage VDD in CSA_L and CSA_R discharges and automatically stops discharging when the voltage reaches the threshold voltage (Vth) of NL and NR. Thus, in P2, CSA_L and CSA_R reflect the Vth of NL and NR, respectively, thus resulting in the offset cancellation. It should be noted that without NL2 and NR2, efficient offset cancellation cannot be achieved, given that the VOUT and VOUTB nodes are connected via MTJ A and MTJ B in P2. By adding NL2 and NR2 for isolation between the VOUT and VOUTB nodes in P2, the proposed NV-FF significantly improves the efficiency of the offset cancellation. In the re-precharge phase (phase3, P3), VOUT and VOUTB are precharged to GND, whereas CSA_L and CSA_R capture the Vth of NL and NR, respectively. In the comparison phase (phase4, P4), the stored data in the MTJs are first compared by the difference in resistance between MTJ A (RMTJ A) and MTJ B (RMTJ B), and then amplified by the positive feedback of the cross-coupled NL and NR. If RMTJ A is smaller than RMTJ B, VOUTB is charged more rapidly than VOUT. Given that VOUTB (VOUT) is connected to the left (right) plate of CSA_R (CSA_L), which is the cross-coupled NMOS structure, the voltage difference between VOUT and VOUTB is almost amplified to the rail-to-rail voltage (VOUTB ~ VDD, VOUT ~ GND). More details on the operation are presented in [10], [10].

![FIG 1. Block diagram of two representative NV-FF structures [3], [5], [10]: (a) Merged latch and sensing circuit (MLS) structure, and (b) Separated latch and sensing circuit (SLS) structure.](image-url)
given that the operation of the proposed NV-FF is the same as the operation of the state-of-the-art NV-FF; with the exception of the inclusion of switches NL2 and NR2. To restore correctly, the offset cancellation of NL and NR, in addition to the difference in resistance between $R_{MTJ_A} + R_{NL2}$ and $R_{MTJ_B} + R_{NR2}$, is critical, where $R_{NL2}$ ($R_{NR2}$) is the effective resistance of NL2 (NR2). To achieve insensitivity to the $V_{th}$ mismatch between NL2 and NR2, the gates of NL2 and NR2 are driven by $V_{DDH}$. Given that the drain current of NMOS is proportional to $(V_{GS} - V_{th})^2$, where $V_{GS}$ is the gate-source voltage; by increasing $V_{GS}$, the effect of the $V_{th}$ mismatch between NL2 and NR2 on the restore mode operation can be suppressed.

Fig. 3 shows the write operation of STT-MTJ [12]–[15]. Because the magnetization direction of the free layer can be changed by flowing a sufficient write current ($I_{write}$) larger than a critical switching current ($I_C$) while the magnetization direction of the pinned layer is fixed, low resistance ($R_L$) can be written by flowing $I_{write}$ from the top electrode (TE) to the bottom electrode (BE). Likewise, high resistance ($R_H$) can be written by flowing $I_{write}$ from the BE to the TE. However, because of the read current ($I_{read}$) that is the current flowing through MTJ_A and MTJ_B during the restore mode, an unintentional write operation can occur. This is known as read disturbance [16].

Fig. 4 shows the read disturbance scenarios in the restore mode in cases of normal-connected MTJs and reverse-connected MTJs. As mentioned earlier, if $R_{MTJ_A}$ and $R_{MTJ_B}$ are $R_L$ and $R_H$, $V_{OUTB}$ and $V_{OUT}$ nearly become $V_{DD}$ and GND, respectively. In the case of normal-connected MTJs (Fig. 4(a)), because the direction of $I_{read}$ is from the TE to the BE, only the MTJ_B of $R_H$ has the probability of causing a read disturbance. To avoid such a read disturbance, $I_{read}$ should be sufficiently lower than $I_C$. However, because $V_{OUT}$ is almost GND, a high $I_{read}$ ($\sim (V_{DD} - GND)/R_H$) is inevitable. In the case of reverse-connected MTJs (Fig. 4(b)), because the direction of $I_{read}$ is from the BE to the TE, only the MTJ_A of $R_L$ has the probability of causing a read disturbance. Because $V_{OUTB}$ is almost $V_{DD}$, $I_{read}$ can be...
FIGURE 4. Read disturbance scenarios in the restore mode in cases of a) Conventionally used normal-connected MTJs and b) Proposed reverse-connected MTJs.

significantly reduced ($\sim (V_{DD} - V_{DD})/R_L$), resulting in read disturbance prevention in the restore mode.

The backup mode operation of the proposed NV-FF has two scenarios that are determined by the computing data Q of the normal FF mode (refer to Fig. 2). When Q is 1 (0) and a write-enable (WE) is asserted, the write current flows from PWR (PWL), MTJ_B (MTJ_A), NR2 (NL2), NL2 (NR2), MTJ_A (MTJ_B), to NWL (NWR). Then, MTJ_A and MTJ_B are written as $R_H$ ($R_L$) and $R_L$ ($R_H$), respectively. Fig. 5 illustrates the operation when Q is 1.

FIGURE 5. Back-up mode operation of the proposed NV-FF when Q is 1.

III. SIMULATION RESULTS AND DISCUSSION

Fig. 6(a) presents the restore mode transient responses when there was no $V_{th}$ mismatch between NL and NR, and Fig. 6(b) presents the responses when there was a $V_{th}$ mismatch of 200 mV ($V_{th,NR} = V_{th,NL} + 200$ mV). In the simulation, the following industry-compatible 65-nm model parameters and the MTJ model based on [17] were used: $V_{DD} = 0.8$ V, $V_{DDH} = 1.5$ V, $R_{MTJ,A} = 3$ k$\Omega$ ($R_L$), $R_{MTJ,A} = 6$ k$\Omega$ ($R_H$), $C_{SA,L} = C_{SA,R} = 20$ fF, $W_{NL} = W_{NR} = W_{NL2} = W_{NR2} = W_{NB} = 1 \mu m$, and $W_{PT} = 2 \mu m$ are used; where W indicates the width of the corresponding transistor, as denoted by the subscript. A minimum length of 0.06 $\mu m$ was used for all the transistors. All other transistors that were not specified had minimum widths of 0.21 $\mu m$. Fig. 6(b) clearly reveals the advantage of the proposed NV-FF, in that the 200 mV $V_{th}$ mismatch in NR was entirely reflected by the $C_{SA,R}$, thereby successfully passing the restore operation; whereas the state-of-the-art NV-FF reflected almost zero, thereby failing.

Fig. 7(a)–(c) present the sensing pass/fail simulation results in the restore mode with respect to the (a) NL/NR $V_{th}$ mismatch; (b) tunnel magneto-resistance ratio (TMR), which is defined as $(R_H - R_L)/R_L \times 100$, when NL/NR $V_{th}$ mismatch is 50 mV; and (c) NL2/NR2 $V_{th}$ mismatch. Fig. 7(a) reveals that the proposed NV-FF exhibited a higher offset tolerance than the state-of-the-art NV-FF by a factor of 5. Due to the improved offset-tolerance characteristic, as can be seen from Fig. 7(b), the proposed NV-FF can restore correctly at a TMR of 20%; whereas the state-of-the-art NV-FF can restore correctly in TMR greater than 70%. Fig. 7(c) reveals that the proposed NV-FF was insensitive to the $V_{th}$ mismatch between NL2 and NR2 in accordance with an increase in the $V_{DDH}$, as mentioned previously. To ensure an effective restore operation under the severe conditions of a $V_{th}$ mismatch of 200 mV, $V_{DDH} = 1.5$ V was set. However, according to the target of the restoring yield and the reliability of the transistor, $V_{DDH}$ can be adjusted.

Fig. 8 presents the restore yield of the proposed NV-FF and the state-of-the-art NV-FF with respect to the capacitance of $C_{SA}$ ($= C_{SA,L} = C_{SA,R}$). The restore yield, which is defined as the number of restore pass results over total number of simulations in sigma, was obtained from a large number of...
FIGURE 6. Restore mode transient responses of proposed NV-FF and state-of-the-art NV-FF [10] in cases of (a) No $V_{th}$ mismatch and (b) 200 mV $V_{th}$ mismatch between NL and NR. For this simulation, $V_{DD} = 0.8$ V and $V_{DDH} = 1.5$ V were used.

FIGURE 7. Sensing pass/fail simulation results in restore mode with respect to (a) NL/NR $V_{th}$ mismatch, (b) Tunnel magneto-resistance ratio (TMR) when NL/NR $V_{th}$ mismatch is 50 mV, and (c) NL2/NR2 $V_{th}$ mismatch.

Monte Carlo simulations. The target restore yield of NV-FF was set to 4σ to guarantee a 96.88% yield when 1000 NV-FFs are assumed [10]. Given that $C_{SA}$ was used for the offset cancellation of NL and NR and the positive feedback operation of the cross-coupled NL and NR in the comparison phase, a larger $C_{SA}$ would improve the restore yield. The proposed NV-FF achieved a target restore yield of 4σ at $C_{SA} = 10$ fF; whereas the state-of-the-art NV-FF did not achieve the target store yield even at $C_{SA} = 20$ fF, due to the inefficient offset-cancellation characteristic. The increase in size of $W_{NL}$ and $W_{NR}$ improved the restore yield; however, it decreased after $C_{SA} = 10$ fF, due to the limited restore time when each phase time is set to 20 ns.

FIGURE 8. Restore yield of the proposed NV-FF and state-of-the-art NV-FF with respect to capacitance $C_{SA}$ ($= C_{SA,L} = C_{SA,R}$).

FIGURE 9. Restore yield of the proposed NV-FF with respect to $W_{NL2}$ ($= W_{NR2}$) and $V_{DDH}$.

Fig. 9 shows the restore yield of the proposed NV-FF with respective to $W_{NL2}$ ($= W_{NR2}$) and $V_{DDH}$. For this simulation, $C_{SA} = 20$ fF was used. Because the effect of the $V_{th}$ mismatch between NL2 and NR2 on the restore mode operation is suppressed as the width of NL2 and NR2 or $V_{DDH}$ increases, the restore yield increases with $W_{NL2} (= W_{NR2})$ and $V_{DDH}$. When $V_{DDH} = 1.5$ V is used, $W_{NL2} = W_{NR2} = 1.0 \mu m$ is sufficient to achieve the target restore yield of 4σ. When $V_{DDH} = 1.3$ V is used, $W_{NL2} = W_{NR2} = 2.0 \mu m$ is required.

FIGURE 10. Restore yield of the proposed NV-FF and a state-of-the-art NV-FF with respect to $W_{NL}$.

Fig. 10 shows the restore yield of the proposed NV-FF and a state-of-the-art NV-FF with respect to $W_{NL} (= W_{NR})$. For this simulation, $V_{DDH} = 1.5$ V was used. Unlike the state-of-the-art NV-FF, whose restore yield monotonically increases with $W_{NL}$ and $W_{NR}$, the proposed NV-FF has an optimal $W_{NL}$ and $W_{NR}$. When $W_{NL}$ and $W_{NR}$ are extremely small (e.g., $0.25 \mu m$), the effective resistances of NL and
NR become significantly high. Because this reduces the pull-down drive strength of the NL and NR, the voltage difference (ΔV) between V_{OUT} and V_{OUTB} becomes extremely small, as shown in Fig. 11(a), leading to a degradation in the restore yield. When W_{NL} and W_{NR} are extremely large (e.g., 10 µm) with the same value of C_{SA}, the capacitive coupling effect between V_{OUT} (V_{OUT}) and V_{G, NR} (V_{G, NL}) decrease because the coupling ratio depends on C_{SA, R} / (C_{SA, R} + C_{G, NR}) and C_{SA, L} / (C_{SA, L} + C_{G, NL}), where C_{G, NR} and C_{G, NL} are gate capacitances of NR and NL, respectively. This results in the weak positive feedback of cross-coupled NMOS, as shown in Fig. 11(b). The restore yield is also degraded. To improve the restore yield in extremely large values of W_{NL} and W_{NR}, C_{SA} should be also increased. In case of the proposed NV-FF, however, because of the superior offset-tolerance characteristic, large W_{NL} and W_{NR} values are not necessary. Thus, a much smaller C_{SA} can be used to achieve the target restore yield compared to the state-of-the-art NV-FF. The optimal W_{NL} and W_{NR} range of the proposed NV-FF is from 0.5 µm to 1 µm, as shown in Fig. 10. On the ground that a smaller W_{NL}, W_{NR}, and C_{SA} are possible in the proposed NV-FF compared to the state-of-the-art NV-FF and W_{NL2} = W_{NR2} = 1 µm is sufficient for achieving the same restore yield, the proposed NV-FF is expected to have a much smaller area than the state-of-the-art NV-FF.

Both the state-of-the-art and proposed NV-FFs have a cross-coupled NMOS structure. For this reason, V_{OUT} and V_{OUTB} cannot be the rail-to-rail voltage (V_{DD} or GND) after finishing the positive feedback of restore mode. Because the non-rail-to-rail voltages of V_{OUT} and V_{OUTB} generate static I_{read}, it can cause a read disturbance. When MTJA = R_L and MTJB = R_H, MTJB (MTJA) of state-of-the-art NV-FF (proposed NV-FF) has the probability of causing a read disturbance, as described in Section II and Fig. 4. Fig. 12 shows the I_{read} causing a read disturbance (proposed NV-FF: I_{read} flowing through MTJA, state-of-the-art NV-FF: I_{read} flowing through MTJB) with respect to NL/NR V_{th} mismatch. Fig. 12 clearly shows that the proposed NV-FF can reduce the I_{read} by almost two orders of magnitude compared to the state-of-the-art NV-FF, resulting in the prevention of read disturbance.

In the case of 65-nm process technology, the nominal V_{DD} is 1.2 V and the maximum allowable V_{DD} is 1.32 V, which is the value of the nominal V_{DD} multiplied by 1.1. Thus, a V_{DDH} of 1.5 V is not allowed to prevent gate oxide breakdown. There are two approaches to prevent this problem. The first approach is to reduce the V_{DDH} by increasing the width of NL2 and NR2. As shown in Fig. 9, a V_{DDH} of 1.3 V can be used by increasing the width of NL2 and NR2 to 2 µm. The second approach is to reduce the V_{DDH} by replacing the typical V_{th} NMOSs NL2 and NR2 with low V_{th} NMOSs because this reduces the effect of V_{th} variation in (V_{GS} – V_{th})^2. It should be noted that because both typical and low V_{th} NMOSs use the same gate oxide thickness, their allowable
voltage are the same to 1.32 V. Fig. 13 shows the restore yield of the proposed NV-FF with respect to \( W_{NL2} \) (= \( W_{NR2} \)) and \( V_{DDH} \) when NL2 and NR2 are low \( V\text{th} \) NMOSs. The figure shows that a \( V_{DDH} \) of 1.3 V can be used without increasing the width of NL2 and NR2. To minimize the area overhead, the second approach based on low \( V\text{th} \) NMOS for NL2 and NR2 is selected. Because the restore yields in cases of typical \( V\text{th} \) NL2 and NR2 with \( V_{DDH} = 1.5 \) V and low \( V\text{th} \) NL2 and NR2 with \( V_{DDH} = 1.3 \) V are almost the same, all the previous results using typical \( V\text{th} \) NL2 and NR2 with \( V_{DDH} = 1.5 \) V can be interpreted as results obtained using low \( V\text{th} \) NL2 and NR2 with \( V_{DDH} = 1.3 \) V.

Fig. 14 shows the restore yield of the proposed and state-of-the-art NV-FFs with respect to \( V_{DD} \). For this simulation, low \( V\text{th} \) NMOSs are used for NL2 and NR2 with \( V_{DDH} = 1.3 \) V. The figure shows that the state-of-the-art NV-FF requires a \( V_{DD} \) of 1.1 V to achieve the target restore yield of \( 4\sigma \), whereas the proposed NV-FF requires a \( V_{DD} \) of 0.8 V.

Fig. 15 shows the restore yield of the proposed and state-of-the-art NV-FFs with respect to the restore time. For simplicity, the simulation uses equal phase times for P1, P2, P3, and P4. As expected, the restore yields of both NV-FFs increase as the restore time increases. Note that the proposed NV-FF achieves the target restore yield at a restore time of 6 ns, whereas the restore yield of the state-of-the-art NV-FF is saturated to 2.7\( \sigma \) at a restore time of 40 ns.

Figs. 16 and 17 show the restore yield of the proposed and state-of-the-art NV-FFs with respect to temperature and process corner, respectively. The process corners are specified by two letters describing the NMOS and PMOS. S, T, and F stand for slow, typical, and fast corners, respectively. These results clearly verify that the proposed NV-FF outperforms the state-of-the-art NV-FF in terms of offset-tolerance characteristics regardless of the temperature and the process corner. It should be noted that when the temperature decreases to a value lower than 0 \( ^\circ \text{C} \) or the process corner is SS, because of significantly increased \( V\text{th} \) of switches, which are described as switch symbols in Fig. 2, the switches are not fully turned.
on, resulting in weak positive feedback and a degradation in restore yield. This can simply be overcome by replacing the typical $V_{th}$ switches to low $V_{th}$ switches, as shown in Figs. 16 and 17.

So far, the power rail of $V_{DDH}$ was assumed for the proposed NV-FF. Unless the power rail of $V_{DDH}$, which is for the purpose of operating not the proposed NV-FF but the other blocks, exists already in a target IoT application, however, using dual-rail supply only for the NV-FF in IoT application is not attractive because it may cause significant design complexity and power/area overhead. Fig. 18 shows a charge pump based solution that is capable of generating $V_{DDH}$ signal (P1,4_CP) without extra power rail of $V_{DDH}$. The operation of the charge pump is simple. When $V_{DD}$ signal P1,4 is low, the voltages of P1,4_CP and BOT_CP ($V_{P1,4_CP}$ and $V_{BOT_CP}$) are GND, and the voltage of TOP_CP ($V_{TOP_CP}$) is $V_{DD}$. When P1,4 signal changes from low (GND) to high ($V_{DD}$), $V_{BOT_CP}$ becomes $V_{DD}$, and then, by the capacitive coupling through C_CP, $V_{TOP_CP}$ and $V_{P1,4_CP}$ increase above $V_{DD}$. The increment of $V_{P1,4_CP}$ depends on the value of C_CP. Note that the body of two PMOSs, PCP1 and PCP2, is connected to the node TOP_CP, and a high $V_{th}$ PMOS is used for the PCP1 to maximize the increment of $V_{P1,4_CP}$. Fig. 19(a) shows the transient response of $V_{P1,4_CP}$ according to the value of C_CP. As expected, $V_{P1,4_CP}$ increases as the C_CP increases. It shows that C_CP of 6 fF is sufficient to achieve the target value of 1.3 V. $V_{th}$ variation of PCP1 can cause significant variation of $V_{P1,4_CP}$. Fig. 19(b) of 1000 sets of Monte Carlo simulations with minimum sized (width = 0.21 µm, length = 0.06 µm) PCP1 clearly
shows that $V_{P1,4\text{CP}}$ variation increases as time elapses, and at time $= 70$ ns, $V_{P1,4\text{CP}}$ variation becomes almost 140 mV. However, because the positive feedback occurs early in P3 (60.3 ∼ 60.5 ns) and after starting to the positive feedback $V_{OUTB}$ and $V_{OUT}$ are amplified correctly regardless of the value of $C_{CP}$. It also clearly shows that $C_{CP}$ of 6 fF, which corresponds to the pMOSCAP size of 6.0 $\mu$m/0.1 $\mu$m (W/L), is sufficient to achieve the target restore yield of $4\sigma$. Fig. 20 shows the restore yield of the proposed NVFF with charge pump according to the value of $C_{CP}$. It also clearly shows that $C_{CP}$ of 6 fF, which corresponds to the pMOSCAP size of 6.0 $\mu$m/0.1 $\mu$m (W/L), is sufficient to achieve the target restore yield of $4\sigma$.

**FIGURE 20.** Restore yield of the proposed NV-FF with charge pump according to the value of $C_{CP}$. For this simulation, low $V_{th}$ NMOSs are used for NL2 and NR2 without the use of $V_{DDH}$.

**FIGURE 21.** Example of the restore mode transient responses of $V_{OUT}$ and $V_{OUTB}$ (1000 sets of Monte Carlo simulations were conducted).

Table 1 summarizes and compares the performance of the proposed and state-of-the-art NV-FFs. Both NV-FFs use the SLS structure to optimize the sensing circuit without causing degradation in slave latch operation. The proposed NV-FF achieves the restore yield of $4.3\sigma$ at a restore time of 6 ns, whereas the restore yield of the state-of-the-art is saturated to $2.7\sigma$ at a restore time of 40 ns. The restore yield values of $2.7\sigma$ and $4.3\sigma$ are the same as the restore error rates of $3.5 \times 10^{-3}$ and $8.5 \times 10^{-6}$, respectively. Thus, by using the proposed NV-FF, a three-order improvement in the restore yield can be achieved. When the same restore time of 6 ns is applied, the restore energy of the proposed NV-FF is slightly lower than that of the state-of-the-art NV-FF even the energy consumed by the charge pump is included. It is due to the better offset-cancellation characteristic, leading to more rail-to-rail $V_{OUT}$ and $V_{OUTB}$ (as shown in Fig. 6), thereby reducing static current at P4. Even though [11], which is the first paper proposing the reverse-connected MTJ structure for embedded STT magnetic random access memory application, does not mention about the area overhead, the reverse-connected MTJ may cause the area overhead because one or two extra vias are required. However, its area overhead is negligible from the NV-FF area perspective. $I_{read}$ causing the read disturbance of the state-of-the-art NV-FF is 60.1 $\mu$A. The proposed NV-FF, however, significantly reduces the $I_{read}$ causing the read disturbance to 0.98 $\mu$A by employing the reverse-connected MTJ structure. Even though the write current of the proposed NV-FF is decreased from 58.5 $\mu$A to 53.9 $\mu$A because of the

| TABLE 1. Performance summary and comparison between state-of-the-art NV-FF [10] and proposed NV-FF. |
|---------------------------------------------------------------|
| FF Structure                      | State-of-the-art NV-FF [10] | Proposed NV-FF |
| $V_{DD}$ [V]                     | 0.8                        | 0.8            |
| $V_{DDH}$ [V]                     | N/A                        | 1.3            |
| Restore Yield [$\sigma$]          | 1.1 @ 6 ns$^5$              | 1.1 @ 6 ns$^5$ |
|                                  | 2.7 @ 40 ns                | 2.7 @ 40 ns    |
| Restore Time[$^3$] [ns]           | 40                         | 6              |
| Restore Energy [$^7$] [fJ]        | 107 @ 6 ns$^3$              | 104$^b$         |
|                                  | 536 @ 40 ns                | 536 @ 40 ns    |
| MTJ Structure                    | Normal-connected           | Reverse-connected$^5$ |
| $I_{read}$ causing Read Disturbance [$\mu$A] | 60.1                      | 0.98           |
| Write Current [$^{a}$] [$\mu$A]   | 58.5                       | 53.9           |
| C-Q Delay                        | Same to transmission-gate-based master-slave FF |

1) $C_{CP}$ is generated by charge pump with $C_{CP}$ of 6 fF.
2) Even though the state-of-the-art NV-FF has the restore yield of only 1.1$\sigma$ when restore time is 6 ns, this result is included in Table I for reference.
3) Equal phase times for P1, P2, P3, and P4 are used.
4) Energy consumed by the charge pump is included.
5) The reverse-connected MTJ structure may cause the area overhead because one or two extra vias are required. However, its area overhead is negligible from the NV-FF area perspective.
6) Width of PWL and PWR of 2 $\mu$m and width of NWL and NWR of 1 $\mu$m are used.
addition of NL2 and NR2, its write current is still enough when the write time of more than 10 ns is considered [5]. The clock-to-Q (C-Q) delays of both NV-FFs are the same as the transmission-gate-based master-slave FF because of the SLS structure.

Even though this paper focuses on the dynamic offset cancellation technique (offset capture and cancel), the offset voltage can also be alleviated by employing offset calibration techniques [18]–[20].

IV. CONCLUSION

This paper proposes a novel NV-FF with a significantly improved offset-tolerance characteristic due to the inclusion of two NMOSs (NL2 and NR2), to achieve isolation between the \( V_{OUT} \) and \( V_{OUTB} \) nodes in the offset-cancelling phase. To achieve insensitivity to the \( V_{TH} \) mismatch between NL2 and NR2, the gates of NL2 and NR2 were driven by \( V_{DDH} \). To avoid the overhead caused by the use of dual-rail supply, a charge pump based solution is proposed. In addition, the reverse-connected MTJ structure is used to reduce the read disturbance. The simulation results verify the effectiveness of the proposed NV-FF, which demonstrated a three-order improvement in the restore yield and a two-order reduction in the \( t_{read} \). Hence, the proposed NV-FF can be employed for the realization of zero standby power and instant ON/OFF NV-FF systems.

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