Abstract This paper presents a radiation-hardened flip-flop called MSIFF. The sensitive node-pairs between the master and slave latches are readjusted at layout-level. It obtains a high SEU tolerance with slight area and performance degradation. A test chip was irradiated with the static and dynamic test modes to validate the SEU tolerance of the proposed MSIFF. Experimental results demonstrate superior performance of the MSIFF over the conventional DICE and D flip-flop.

key words: Layout hardened design, Master-slave interleaving, DICE, Sensitive node-pairs, charge sharing
Classification: Integrated circuits

1. Introduction

Technology scaling has increased the vulnerability of flip-flops to single-event upset (SEU) [1]-[3]. Reduced nodal capacitance and supply voltage decrease the critical charge required to upset [4]-[7]. Close proximity of transistors results in charge sharing at multiple nodes [8]-[13]. Conventional redundant-based flip-flops, such as DICE and triple modular redundancy (TMR), are immune to SEU that only one node collects charge [14]. Charge sharing significantly increases SEU sensitivity of these redundant flip-flops by orders of magnitude. Some works have reported the conventional DICE flip-flop provides a very small advantage over unhardened flip-flop designs with technology scaling [15]-[17]. Therefore, it will be more challenging to mitigate SEU sensitivity at advanced CMOS technologies.

This paper presents a master-slave interleaved DICE flip-flop called MSIFF. We readjust the layout placement and separate the sensitive nodes by interleaving master-slave stage. A test chip was designed and fabricated in the commercial 65 nm bulk CMOS technology to estimate SEU sensitivity of the MSIFF. Heavy ion experimental data demonstrate it significantly improves SEU threshold and cross sections compared with the conventional DICE and D flip-flops.

2. Hardness mechanism of the MSIFF

The conventional DICE flip-flop considered in this paper is shown in Fig. 1. It is firstly described in [14] and widely used to harden the flip-flops. The conventional DICE flip-flop has several sensitive node pairs, such as node mn2 and mn4. It can be upset if any sensitive node-pair collect charge simultaneously. With technology scaling, the spacing between the sensitive nodes is also reduced. It leads to significant increase SEU sensitivity of the conventional DICE flip-flop.

Fig. 1. The schematic and layout of the DICE flip-flop considered in this paper.

To improve SEU tolerance of the DICE flip-flop, we readjust the sensitive nodes in the whole flip-flop. The sensitive nodes in the master latch are separated by the components of the slave latch, as shown in Fig. 2. This master-slave interleaving approach is similar with the double-DICE layout hardened approach described in [18]. However, we do not utilize an additional DICE latch but utilize the slave latch to separate the sensitive nodes. Therefore, the proposed MSIFF has a higher area efficiency. The interleaved master-slave stage effectively mitigates...
charge sharing between sensitive node-pairs. When an incident ion strikes the sensitive transistors, for example the PMOS transistors in node mn2, a column of electron-hole pairs are ionized along the incident track. The ionized carriers diffuse to the adjacent transistors and result in charge collection between the adjacent sensitive nodes, as shown in Fig. 3. For the conventional DICE flip-flop, the sensitive node-pairs will collect enough charge and lead to a SEU. For the proposed MSIFF, the increased node spacing effectively reduces the diffusion-collection due to the recombination process. Furthermore, the inserted components of the slave latch are also helpful to collect the additional carriers [19]. It will significantly decrease the ionized carrier density and prevent the diffusion-collection process. Therefore, the sensitive node-pairs will not collect enough charge simultaneously and SEU will not occur in the proposed MSIFF.

The bipolar amplification effect is another basic mechanism to cause charge collection [20]. The interleaved master-slave stage can also mitigate the bipolar amplification effect induced charge collection. The bipolar amplification effect is dominated by the well potential modulation. It is triggered when the well potential collapses. For the proposed MSIFF, the inserted components of the slave latch can maintain the well potential due to the additional source contacts [21]. It clamps the local well potential, preventing it from collapsing. Therefore, the interleaved master-slave stage can prevent the triggering of the bipolar amplification effect and mitigate the charge collection between sensitive node-pairs. Moreover, the MSIFF is also capable to mitigate SEU induced by the internal single-event transient (SET) [22]-[23]. SET pulses generated at the sensitive nodes may be captured and cause SEU if the latch is from transparent state to latched state. This SET-induced upset is dependent on the operating frequency. The generated SET pulse has a higher probability to be latched with the increase of the operating frequency. Therefore, it would become a key issue in high frequency circuits. Some works have reported the SET-induced upset increases SEU sensitivity of the conventional D flip-flop and the conventional DICE flip-flop with the increase of the operating frequency [24]. Because of the increased nodes spacing, the MSIFF prevents the sensitive node-pair collect charge simultaneously. SET pulse generated at a single node could not be latched and the SET-induced upset will not occur. Therefore, the MSIFF still has a high SEU tolerance with the increase of the operating frequency.

The proposed MSIFF has slight performance degradation because it only increases the metal interconnections. Based on the commercial 65nm CMOS technology, a side-by-side comparison of the area, delay and power of the conventional DICE flip-flop and the proposed MSIFF is shown in Table I. The MSIFF has the same layout area and setup time compared with the conventional DICE flip-flop. It only increases 7.4 % clk-to-q time and 5.4 % power.

### Table I. Comparison of area, delay and power of flip-flops

| Flip-flop | Area (um²) | Setup time (ps) | Clock to Q (ps) | Power (uW) |
|-----------|-----------|----------------|----------------|------------|
| DICE      | 23.4      | 38             | 203            | 6.29       |
| MSIFF     | 23.4      | 38             | 218            | 6.63       |

#### 3. Experimental setup

A test chip was designed and fabricated in the commercial 65nm CMOS technology. It contained the conventional D flip-flop, the conventional DICE flip-flop and the proposed MSIFF. The layout of the test chip is shown in Fig. 4. Each kind of flip-flops was consisted of a 4096 stage shift register chain with clock and data trees. All the signal (input, output and clock) pins of the test circuit were connected to FPGA. Error detection was implemented by FPGA and the error counts were exported to the computer by serial interface. The static test mode with solid 0 and solid 1 data patterns...
Heavy ion experiment was conducted at the HI-13 Tandem Accelerator in China Institute of Atomic Energy and the Heavy Ion Research Facility in Lanzhou (HIRFL) cyclotrons in Institute of Modern Physics, Chinese Academy of Sciences. The experiment setup is shown in Fig. 5. The characteristics of the three ions used in the test are listed in Table II. The incident ion dose rate was $1 \times 10^4$ ions/cm$^2$·s and the fluence was $1 \times 10^7$ ions/cm$^2$.

### 4. Experimental results

#### 4.1 Measured SEU cross sections

The measured SEU cross section is shown in Fig. 6. The conventional DICE flip-flop shows a small advantage in both solid 0 and solid 1 static test mode over the conventional D flip-flop at low LET. It only results in one order of magnitude decrease over the conventional D flip-flop at low LET. It shows a similar SEU sensitivity at high LET. Compared with the conventional D flip-flop, the conventional DICE flip-flop, the proposed MSIFF shows a superior SEU tolerance. The SEU cross section decreases three order of magnitude even when the LET is higher than 90 MeV·cm$^2$/mg. Measured results validate the master-slave interleaving approach effectively prevents charge collection simultaneously between sensitive node-pairs. It brings advantage to mitigate the intrinsic SEU sensitivity and significantly improve the SEU tolerance.

#### 4.2 Effect of the supply voltage

The supply voltage significantly impacts the SEU sensitivity of flip-flops [28]-[29]. The SEU cross sections with different supply voltages were also measured. We performed solid 0 static test mode with a range of the supply voltage from 1.0V to 1.2V. The incident ion is Ge. The measured SEU cross section is shown in Fig. 7. The SEU sensitivity has a slight change for the conventional D flip-flop while it shows an obvious increase for the conventional DICE flip-flop.
flop. The measured SEU cross-section at low supply voltage has only about 9% increase for the conventional D flip-flop and more than 3 times increase for the conventional DICE flip-flop. Note that the conventional DICE flip-flop shows a smaller advantage than the conventional D flip-flop at low supply voltage. The lower supply voltage enhances charge sharing between sensitive nodes. It does not influence the non-redundant flip-flops but significantly influence the redundant-based flip-flops. Therefore, the conventional DICE flip-flop shows more sensitivity to the supply voltage. Different from the conventional DICE flip-flop, the proposed MSIFF still shows a superior SEU tolerance with the decrease of the supply voltage.

4.3 Effect of the temperature
The temperature also significantly impacts the SEU sensitivity of flip-flops [30]-[31]. The SEU cross sections with different temperatures were also measured. We performed solid 0 static test mode with the room temperature (approximate 20°C) and the high temperature (approximate 75°C). The incident ion is Br and the measured SEU cross sections are shown in Fig. 8. An increased SEU sensitivity is observed for both the conventional D flip-flop and the conventional DICE flip-flop with the increase of the temperature. The cross sections at high temperature show about 35% and 38% higher than that at the room temperature, respectively. As expected, the change of the temperature does not influence the SEU sensitivity of the proposed MSIFF.

5. Conclusion
Technology scaling has increased the vulnerability of the redundant-based flip-flops. It is necessary to explore novel radiation hardened approaches to improve SEU tolerance. In this paper, we present a layout-based hardened flip-flop through interleaving sensitive node-pairs between the master and slave latches. This master-slave interleaving approach effectively prevents charge sharing and improves the SEU tolerance. The proposed flip-flop which is termed as MSIFF shows high area efficiency and slight performance degradation compared with the conventional DICE flip-flop. Heavy ion experiments demonstrate superior performance of the proposed MSIFF, especially for different supply voltage and temperatures. Moreover, the master-slave interleaving approach is convenient to apply to other redundant-based flip-flops. It will effectively improve the SEU tolerance for these flip-flops.

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