An efficient 70 GHz divide-by-4 CMOS frequency divider employing low threshold devices

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Introduction: High frequency communication systems rely on phase-locked loop (PLL) to generate a low-noise high-frequency signal carrier. PLL employ frequency dividers to close the loop between the high-frequency output signal and the lower-frequency precision frequency reference. In a common PLL the power consumption of a frequency divider is the second highest after the voltage controlled oscillator (VCO), since only these two components work at the highest frequency of the system. At mm-wave frequencies current mode logic (CML) frequency dividers often with inductive peaking were commonly used up to recently, when the possibility of low-power frequency division with compact true single phase clock (TSPC) frequency divider. The use of the lowest threshold PMOS devices resulted in self-resonance frequencies of 41.7, 56, and 60 GHz at supply voltages of 0.5, 0.8 and 0.9 V, respectively. Compared to a divider of the same architecture in the same technology, but with higher threshold voltage devices, this corresponds to improvements of 67%, 33% and 27%, respectively. Power consumptions of 26 and 355 µW were measured for a 20 GHz and a 70 GHz input signal for supply voltages of 0.5 and 0.9 V, respectively. The best knowledge of the authors, these results are the best reported to date for TSPC divider architecture, and they compete with state of the art for inductorless current-mode logic dividers.

Circuit implementation: The block diagram of the realized circuit is shown in Figure 1. It uses the same circuit architecture as our previous work, which utilized the fastest PMOS devices [1], with the goal comparing the results of the two device selection strategies. The circuit core is composed of two divide-by/2 stages, where the first stage utilize low-threshold PMOS devices. Such transistor flavour is seldom used in general digital circuits due to its non-negligible drain-source leakage. This leakage will set a lower limit on the operating frequency in a TSPC divider beyond what has been achieved with the small-signal-wisest fastest core transistors.

The idea to use a lower threshold, but slightly slower transistor over the fastest transistor type for large-signal circuits is presented with experimental verification for a compact divide-by/4 true single phase clock (TSPC) frequency divider. The use of the lowest threshold PMOS devices resulted in self-resonance frequencies of 41.7, 56, and 60 GHz at supply voltages of 0.5, 0.8 and 0.9 V, respectively. Compared to a divider of the same architecture in the same technology, but with higher threshold voltage devices, this corresponds to improvements of 67%, 33% and 27%, respectively. Power consumptions of 26 and 355 µW were measured for a 20 GHz and a 70 GHz input signal for supply voltages of 0.5 and 0.9 V, respectively. The best knowledge of the authors, these results are the best reported to date for TSPC divider architecture, and they compete with state of the art for inductorless current-mode logic dividers.

The division stages use DFFs where the inverted output are fed-back to the input terminal. As a result, the output toggles at every rising edge at their clock terminal. The operation principle together with the transistor level implementation are depicted in Figure 2. The divider was implemented in a fully depleted silicon on insulator (FD-SOI) technology, which allows forward backgate biasing to reduce the value of the threshold voltage of the transistors. This effect combined with the use of the lowest threshold PMOS transistor available, allowed to reach record high self-resonance frequencies, and mm-wave operation even at a supply voltage as low as 0.5 V. The transfer characteristics of the used transistors are depicted in Figure 3(a) and (b). The higher PMOS current of the low-threshold device in the middle of the range allows an operation point with higher overdrive voltage and thus higher current and transconductance for a given supply voltage compared to a higher threshold voltage transistor. The reduced threshold voltage increases the input voltage range, where the device functions as an amplifier and reduces ineffective regions, where it contributes only to the node capacitances. The effect of the threshold voltage on the operation point of a fed back CMOS inverter for a given supply is displayed schematically in Figure 3(c). The average voltages in the internal nodes of the divider will be set similarly due to the negative feedback. The operation point settles at the crossing of the transfer characteristic of NMOS and PMOS devices. Such effect is even more prominent at longer channel technologies, where velocity saturation is less pronounced and the device characteristic deviates less from the square-law model of long channel devices.

The peak transit frequency \( f_T \) of the different thin-oxide core transistors, which are typically reported in technology datasheets, are similar in value, and the improvement in the operating frequency range of the divider is obtained through the wider high frequency operation point range of a low-threshold voltage device, whose peak \( f_T \) was simulated to be 3% lower. The operation point dependence of \( f_T \) is shown in Figure 4 for typical \( V_{DS} \) values in a TSPC circuit. The low \( f_T \) operation point...
regions near and below the threshold voltage take a smaller part from the ideally rail-to-rail swing of the inner nodes for the lower threshold device. Since the large signal transconductance of a device—also called describing function [3]—can be expressed as the weighted sum of the transconductance at the operation points through which the input voltage trajectory travels in a period, a lower threshold, but otherwise similar device would provide a large-signal transconductance benefit for the same capacitive load. This increases the large-signal bandwidth of the stages, and the operating frequency will increase as a result.

The power consumption of a TSPC divider can be divided into two parts. The leakage current of the low-threshold devices provide a frequency independent component. At high frequencies the charge required to replenish the node capacitances up to the supply voltage in every period will dominate the power consumption. This component is proportional to the sum of the node capacitances and the frequency as well. A widely used figure-of-merit for frequency dividers are their power efficiency, which relates the operating frequency to its power consumption. In the case of a TSPC divider, it is independent of the input frequency if the leakage current is neglected.

The presented design was tailored for comparison with a circuit simultaneously optimized for power efficiency and maximum operating frequency. Even higher efficiencies are possible by using narrower transistors, though the benefits slowly diminish by the increasing weight of the wiring capacitances in the total node capacitances. Higher operational frequencies are possible if the effective width of transistors of the D-flipflop are increased, while the buffer of the D-flipflop is kept at the same size, and hence its capacitance will not change. Even though the wiring capacitances will increase almost linearly with the increased effective width, the capacitance of the buffer will weight less in the total capacitance of the most critical feedback node. On the other hand, this increase in the operating frequency will reduce the power efficiency.

**Experimental results:** The circuit was implemented in 22FDX®, a 22 nm FD-SOI technology from GLOBALFOUNDRIES. The chip micrograph is presented in Figure 5(c). In order to save chip area, three low-input-capacitance circuit prototypes [1] share the input signal pad and the backgate bias pads, where only their core supplies and outputs have dedicated pads. The other circuits have been disabled during the measurement. The dedicated supply pad for the divider core allowed direct measurement of the core current consumption. The layout of the divide-by-4 core is shown in Figure 5. The divide-by-2 core and the divide-by-4 circuit occupy only 1.56 and 3.45 μm² active area, respectively. The measurement setup is depicted in Figure 6 schematically. The circuit was measured on a wafer prober and was driven by a 70 GHz signal generator, while the output was observed with a spectrum analyzer. The average voltage of the input node was set by an external bias tee before the probe to save the area of an additional pad. The current consumption of the divider was measured through an in-loop precision resistance by a digital multimeter. The supply voltage of the core and the buffer was set to the same voltage in all measurements. The measured input reflection coefficient stayed below −18 dB up to 67 GHz, and therefore the input connection does not influence the effective input voltage and the operational frequency of the divider. The measured sensitivity curves—the relation of the minimum required input power for stable frequency division as a function of input frequency are shown in Figure 7. The post-layout simulation results are displayed with dotted curves. The different colors and markers indicate different backbias operation points. The first, green line corresponds to the common configuration for compact layouts, where the backgate of the NMOS and PMOS transistors are connected to VDD and VSS, respectively, for slight forward backgate bias without additional pins and wiring. The grounded backgate of both transistors provide the lowest leakage, and slowest operation, without additional circuit terminals. The PMOS backbias values were limited to −1 V by an antenna diode required by the design rules. A stronger PMOS backgate bias would have increased the operating frequency further. Division operation at 70 GHz has been measured in different operation points at a supply voltage of 0.8 V. Unfortunately no signal generator with sufficient power was available to measure the circuit performance at higher input frequencies. The frequencies where division with very small input power is achievable are called self-resonance frequencies. The measured phase noise values depicted in Figure 8. The operation points are marked with different colors, while the different input frequencies with different line styles. These values lay very close to the specified limit of the used
any degradation in the power efficiency. Self-resonance frequencies

The presented circuit has improved the highest self-resonance frequency in the same technology [1] by 28% to 59.5 GHz, while drawing 0.35 mW.

Conclusions: The benefits of low-threshold voltage devices over the point with 0.5 V supply voltage consuming only 0.1 mW.

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