ABSTRACT This paper presents a low-voltage low-power current-mode third-order low-pass filter (LPF) based on voltage second generation current conveyor (VCII). The VCII utilizes the bulk-driven MOS transistor technique to achieve a wide input voltage range at low supply voltage of 0.5 V. Also, the VCII operates in the subthreshold region to achieve nano-power consumption of 390 nW. A third-order low-pass filter that is presented as an application of the VCII can operate as both current- and transimpedance-mode filters. The filter consumes 2.73 $\mu$W and the total harmonic distortion (THD) is below 1% for sine-wave input signal below 350 nA$_{pp}$ @ 10 Hz. The post-layout simulation results based on TSMC 0.18 $\mu$m CMOS process are presented and confirm the futures of the filter.

INDEX TERMS Voltage second generation current conveyor, third-order low-pass filter, current-mode filter, low-voltage low-power, analog circuit.

I. INTRODUCTION

Recently, there is a gaining research interest for current-mode technique of the filter design. Compared with the voltage-mode counterparts the current-mode filters have been presented in the literature exhibiting improved performance [1]. There are several current-mode building blocks for realization high-order current-mode filters such as current differencing buffered amplifier (CDBA) [2], current-mirror [3] and current differencing transconductance amplifier (CDTA) [4], [5] available in literature. The developed filter topologies provide a higher maximum frequency of operation and a more accuracy of transfer function due to smaller parasitic parameters compared with the filters realized using voltage-mode op-amp configurations [6].

The high-order filter can be applied to biomedical systems devoted to applications in electroencephalograph (EEG), electromyographic (EMG), and electrocardiographic (ECG) systems. The frequency/amplitude ranges for EEG, EMG and ECG signals are respectively 0.05–60 Hz/15–100 $\mu$V, 10–200 Hz/0.1–5 mV and 0.05–250 Hz/100 $\mu$V–5 mV [7].

Since these signals attributes small amplitude and low frequency, high-order filters for applications to these systems should be designed to meet high dynamic range and low-power consumption. The analog low-pass filter is usually required to select the frequency range and eliminate out-of-band noise in the front-end of biomedical systems. The high-order filter based on the RLC prototype is usually required due to lower pass-band sensitivity compared with the cascade approach using biquads.

Voltage second generation current conveyor (VCII) was introduced in [8]–[10]. Conventional VCII has three terminals (y, x, and z), the first stage between y and x terminals is a current follower and cascaded by a voltage follower between x and z terminals as the second stage. This device is designed to obtain a low impedance voltage output node for avoiding an extra voltage buffer for application requiring a voltage output signal [11]. The required additional voltage buffer can lead to higher power consumption and a large chip area. A number of VCII structures have been reported recently in literature [11]–[18]. Unfortunately, these structures are designed by rather high supply voltage and high-power consumption such as ±1.65 V/330 $\mu$W in [11], ±0.9 V/120 $\mu$W in [12], ±1.65 V/320 $\mu$W in [13], ±0.9 V/664 $\mu$W in [16], ...
\[ \pm 0.45 \text{ V}/79.3 \text{ } \mu\text{W} \text{ in [18]. Therefore, these VCIIIs are not suitable for applications to ultra-low power analog signal processing. There are interesting applications of VCII available literature such as simulated inductor [15], universal filter [19]–[21], first-order all-pass filter [22], capacitance sensors [23], and full wave rectifier [24].}

In this work, a current-mode third-order low-pass filter based on voltage second generation current conveyor for bio-sensor applications is proposed. The proposed VCII is designed using bulk-driven (BD) MOS technique to provide wide input voltage range while the MOS operates in subthreshold region to obtain low-voltage low-power operation. The VCII is designed to work with voltage supply \( V_{DD} = 0.5 \text{ V} \) and power consumption is 390 nW. The proposed third-order filter was designed and simulated in the Cadence environment using a 0.18 \( \mu\text{m} \) CMOS process from TSMC. Post-layout Simulation results show that the filter offers a bandwidth (BW) of 250 Hz, and a power consumption of 2.73 \( \mu\text{W} \).

**II. PROPOSED CIRCUIT**

**A. 0.5 V VCII**

Fig. 1(a) shows the symbol of VCII and its equivalent circuit is shown in Fig. 1(b). The relation between the terminal voltages and current can be described by

\[
\begin{bmatrix}
i_x \\
\bar{i}_v \\
i_z
\end{bmatrix} =
\begin{bmatrix}
1/r_x & \beta & 0 \\
0 & r_x & 0 \\
\alpha & 0 & r_z
\end{bmatrix}
\begin{bmatrix}
v_x \\
\bar{i}_v \\
v_z
\end{bmatrix}
\]  
(1)

where \( \beta \) is the current gain and \( \alpha \) is the voltage gain of VCII (unity for the ideal case). It should be noted from (1) that the relation between \( x \) and \( y \) terminals is the current follower and the relation between \( z \) and \( x \) is the voltage follower, where \( r_y, r_x, \) and \( r_z \) are respectively the parasitic resistance at \( y, x, \) and \( z \) terminals.

Fig. 2 shows the proposed VCII that consists of two op-amps operating in unity gain feedback, firstly presented in [25], [26]. The first op-amp has two outputs and is created by transistors \( M_1-M_4 \) and \( M_9-M_{12} \) that ensure the unity gain current transfer \( I_x = I_y \). The second op-amp is created by \( M_3-M_7 \) and \( M_{13}-M_{15} \) that ensure the unity gain voltage transfer \( V_z = V_x \). The bias current \( I_B \) and transistor \( M_S \) set the currents of the VCII. For the first op-amp, transistor \( M_1, M_2 \) create non-tailed differential amplifier loaded by current mirrors \( M_9, M_{10} \), the second stage is created by transistor \( M_3 \) loaded by the current source \( M_{11} \). The bulk-drain terminals of \( M_3 \) and the bulk terminal of \( M_2 \) are connected together that creates a negative unity feedback connection. Transistors \( M_4, M_{12} \) create a copy of the current \( M_3, M_{11} \). The minimum voltage supply of this structure is:

\[ V_{DDmin} = \max (V_{SGM2} + V_{DSsatM10}) \]  
(2)

where \( V_{SG} \) and \( V_{DSsat} \) are the source-gate voltage and saturation voltage of the MOS transistor, respectively.

**B. PROPOSED FILTER**

Fig. 3 shows the doubly terminated RLC ladder third-order low-pass filter by \( R_E \) and \( R_L \) are connecting at the input and output ports respectively. Using KCL routine analysis the voltage and current relationship in several nodes can be written as:

\[
I_1 = I_{in} - \frac{V_1}{R_E} - I_2 
\]
(7)

\[
V_1 = \frac{I_1}{sC_1} 
\]
(8)

\[
I_2 = \frac{V_1 - V_2}{sL_2} 
\]
(9)

\[
V_3 = \frac{I_2 - I_{RL}}{sC_2} 
\]
(10)
\[ I_3 = I_2 - I_{RL} \] (11)

where \( I_{RL} = I_{out} \) and \( V_3 = V_{out} \). Using (7)-(9), signal flow graph of RLC low-pass filter can be shown in Fig. 4. It should be noted that three lossless integrators are required for realizing third-order low-pass filter.

**III. SIMULATION RESULTS**

The VCII was designed and verified in Cadence Analog Environment using 0.18 \( \mu \)m TSMC CMOS technology. The supply voltage was 0.5 V (\( V_{DD} = -V_{SS} = 0.25 \) V) and the bias current \( I_B \) was 20 nA. The transistors aspect ratio in \( \mu \)m/\( \mu \)m were for \( M_1, M_2, M_5, M_6, M_8 = 50/1 \), \( M_3, M_4, M_7 = 5 \times 50.1 \), \( M_9, M_{10}, M_{13}, M_{14} = 100/1 \), \( M_{11}, M_{12}, M_{15} = 5 \times 100.1 \). The layout of the VCII is shown in Fig. 6 with chip area 158 \( \mu \)m \( \times \) 140 \( \mu \)m.

Fig. 5 shows the proposed current-mode third-order low-pass filter using VCIIIs. The VCII1, VCII2, \( C_1 \) are worked as a first integrator while VCII3, VCII4, \( C_{L1} \) are worked as a second integrator and VCII5, VCII6, \( C_2 \) are worked as a third integrator. The inductor \( L_2 \) in the RLC prototype can be converted to the capacitor \( C_{L1} \) through the VCII and \( R \) by \( L_2 = C_{L1} R^2 \). The VCII3 is used to provide high-output impedance for current-mode circuit. Thus, the proposed current-mode filter offers low-input impedance and high-output impedance which is meet for current-mode circuit. From the property of VCII such as \( V_z = V_x \), node \( V_3 \) can also be used as output voltage terminal (\( V_{out} \)). In this case, the filter works as a transimpedance-mode filter which is meet a low-input impedance and a low-output impedance. The VCII7 can be vanished and the resistor \( R_L \) must be connected to ground if it works as a transimpedance-mode filter.
enjoys high output resistance $R_X = 16.1 \, \text{M} \Omega$ while the resistances $R_Y = R_Z = 5.63 \, \text{k} \Omega$. The value of these parasitic resistances of Y and Z terminals should be taken into account during the design of the applications. The voltage and current input-referred noises (IRN) of the VCII at Z and X node, respectively, are shown in Fig. 10. The voltage IRN is 500nV, while the current IRN is 0.481pA @ 1 kHz.

The performances of the VCII are presented in the Table 1 and compared to most recent VCIIIs presented in the literature [12], [13], [18], [22]. It is evident that the proposed structure has the lowest supply voltage, lowest power consumption with extended input voltage range $\pm 200 \, \text{mV}$ that make it suitable for bio-sensor applications. Also the efficient of the design and the low voltage operation capability are confirmed by the figure of merits $(V_{TH}/V_{DD}) \times 100 (%)$ and $(V_{in-max}/V_{DD}) \times 100 (%)$.
TABLE 1. Compassion between proposed VCII and others.

|                      | Proposed | CSSP [18] | IET [22] | 2020 | [12] 2019 | [13] 2020 |
|----------------------|----------|-----------|----------|------|----------|----------|
| Technology (µm)      | 0.18     | 0.18      | 0.18     | 0.15 | 0.35     |          |
| Voltage supply (V)   | 0.5      | 0.9       | 1.8      | 1.8  | 3.3      |          |
| Power consumption (nW)| 390     | 79 300    | 458 000  | 120 000 | 320 000  |          |
| Current gain β       | 0.999    | 0.987     | 1.017    | 0.996 | 0.987    |          |
| Voltage gain α       | 0.999    | 0.972     | 0.978    | 0.973 | 0.992    |          |
| DC linearity of current gain (nA) | ±190 | ±250000 | NA | ±500000 | NA |          |
| DC linearity of voltage gain (mV) | ±200 | ±60 | NA | ±800 | NA |          |
| Bandwidth of current gain (kHz) | 351.8 | 225 000 | NA | 165 000 | 22 400 |          |
| Bandwidth of voltage gain (kHz) | 74.3 | 49300 | NA | 55 000 | 220 000 |          |
| $g_t$ (kΩ)           | 5.63     | 2.7       | 0.0237   | 0.023 | 2E-6     |          |
| $r_t$ (MΩ)           | 16.1     | 0.1565    | 0.00068  | 522  | 0.37     |          |
| $r_e$ (kΩ)           | 5.63     | 0.0382    | 0.0237   | 0.16  | 2E-6     |          |
| Offset voltage (mV)  | 2*       | NA        | NA       | NA   | NA       |          |
| Offset current (nA)  | 1.75*    | 300       | NA       | NA   | NA       |          |
| Voltage IRN (mV/kHz) | 500 @ 1 kHz | 21.67 @ 10 MHz | NA | NA | 154 |          |
| Current IRN (µA/Hz)  | 0.481 @ 1 kHz | 4.96 @ 10 MHz | NA | NA | NA |          |
| Chip area (µm²)      | 22 120   | 509.6     | NA       | NA   | 75 155   |          |
| $V_{MM}/V_{DD}$<100 (%) | 100     | 55.5      | 27.7     | 33.3  | 21.2     |          |
| $V_{MM}/V_{DD}$>100 (%) | 80     | 6.6       | NA       | 88.8  | NA       |          |

* 3sigma

FIGURE 12. Frequency characteristics of the proposed filter with various $R$. 

The process, voltage and temperature (PVT) corners analysis were carried out with transistor corners: ss, sf, fs, ff, voltage supply corners ±10% of $V_{DD}$, and temperature corners −20 °C to 70 °C. The results of the frequency characteristics of the proposed filter with PVT corner analysis are shown in Fig. 14. The minimum $−3$ dB BW = 238.2 Hz and the maximum = 250 Hz. The minimums and maximum gain were around $−6.67$ dB and $−6.98$ dB, respectively.

The transient analysis of the filter is shown in Fig. 15. The input sine wave signal applied to the filter $IN = 50$ nA@ 10 Hz. The THD of the output signal is 0.09 %. The filter was tested for different peak-to-peak signal value is around 248.3 Hz with standard deviation around 1.93 Hz.

and with 100 Hz, the results of THD is shown in Fig. 16. The THD is below 1 % for input signal below 350 nA.

FIGURE 13. The histogram of the filter: a) gain and b) $−3$ dB bandwidth.
IV. CONCLUSION

This paper presents a third order low pass filter based on low-voltage low-power VCII. The VCII is capable to work with supply voltage of 0.5V while offering a wide input voltage range thanks to using the bulk-driven MOST technique operating in the subthreshold region. The filter can be operated as both current-mode and transimpedance-mode filters. The filter consumes 2.73 $\mu$W and the THD is below 1% for input signal below 350 nA$_{pp}$ @ 10Hz. Intensive postlayout simulation including MC and corner analysis confirm the performance of the filter.

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M. Kumngern et al.: 0.5 V Current-Mode LPF Based on VCII for Bio-Sensor Applications

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