Numerical approach for retention characteristics of double floating-gate memories

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We report on a numerical investigation in which memory characteristics of double floating-gate (DFG) structure were compared to those of the conventional single floating-gate structure, including an interference effect between two cells. We found that the advantage of the DFG structure is its longer retention time and the disadvantage is its smaller threshold voltage shift. We also provide an analytical form of charging energy including the interference effect.

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Floating-gate (FG) memories are widely used in computers because of their low cost and high density [1, 2]. FG memories have progressed rapidly through downsampling using state of the art technology. However, several problems have been arising as a result of the progress of down-scaling of the FG structure to the nanoscale region. In particular, the interference between FGs due to Coulomb interaction is emerging as one of the largest general problems have been arising as a result of the progress of down-scaling of the FG structure to the nanoscale region. In particular, the interference between FGs due to Coulomb interaction is emerging as one of the largest obstacles for FG memories [3, 4]. Stored charges in neighboring FGs interfere with one another, resulting in undesirable threshold voltage shifts in memory operations. In order to reduce this interference, complicated programming sequences are carried out in the current commercial FG arrays.

In the case of locally charged materials such as dielectric materials, it is evident that the electric dipoles exist stably within mutual strong Coulomb interaction. This leads us to consider whether we can construct an “artificial dipole” using a FG system. One of the candidates might be a stacked double floating-gate (DFG) structure [5], in which an additional FG exists between the FG and the control gate in the conventional FG array as shown in Fig. 1(a). Moreover, if the FG becomes as small as a quantum dot [6, 7], DFG can be used as a qubit [8], which is a basic element of a quantum computer [10]. There-

Quantum dot [7, 8], DFG can be used as a qubit [9], which might be a stacked double floating-gate (DFG) structure [5, 6], in which an additional FG exists between the FG and control gate, respectively (Fig. 1). Formulation.—We calculate transient behaviors of a cell where length $L$ and width $W$ of each FG and a distance between neighboring cells $X_D$ are set equal as $L = W = X_D = 23$ nm and the height of all FGs is $Z = 50$ nm for two cases of oxide thickness (Fig. 1(b)). (We obtain similar results for the $L = W = 11$ nm case.) We take dielectric constants and effective mass of Si and oxide SiO$_2$ as $\epsilon_{Si} = 11.7$, $\epsilon_{ox} = 3.9$, and $m_{Si} = 0.19$, $m_{ox} = 0.5$, respectively. The barrier height of SiO$_2$ is $\Phi_b = 2.9$ eV. The capacitances are defined by $C_A = \epsilon_{Si}LW/(T_{CG} + \gamma Z/2)$, $C_B = \epsilon_{Si}LW/(T_{ox2} + \gamma Z)$, $C_C = \epsilon_{Si}LW/(T_{ox1} + \gamma Z/2)$, $C_D = \epsilon_{Si}ZW/(X_D + \gamma L)$, $C_E = \epsilon_{Si}ZW/X_E$, $C_H = \epsilon_{Si}ZW/X_H$ and $C_K = \epsilon_{Si}ZW/X_K$ with $X_E = \sqrt{(X_D + \gamma L)^2 + (T_{ox1} + \gamma Z)^2})$, $X_H = \sqrt{(X_D + \gamma L)^2 + (T_{CG} + \gamma Z/2)^2}$ and $X_K = \sqrt{(X_D + \gamma L)^2 + (T_{ox2} + \gamma Z/2)^2}$ where $T_{ox1}$, $T_{ox2}$ and $T_{CG}$ are oxide thickness between lower FG and substrate, between two FGs, and between upper FG and control gate, respectively (Fig. 1). $\gamma = \epsilon_{ox}/\epsilon_{Si}$ is a penetration effect of small FGs [13]. Because we use SiO$_2$ for all tunneling barriers, equal EOT means that the total thickness of barriers is the same, namely, $T_{ox1}^{DFG} + T_{ox2}^{DFG} + T_{CG}^{DFG} = T_{ox1}^{SFG} + T_{CG}^{SFG}$.

Transient calculation is carried out as follows [11]. (i) For given initial charges $Q_{\alpha i}$, $Q_{\beta i}$ ($i = 1$ and $i = 2$ indicate left cell and right cell. $\alpha$ and $\beta$ indicate upper FG and lower FG, respectively), potential energies of FGs $V_{\alpha i}$, $V_{\beta i}$ ($i = 1, 2$) are obtained by solving the matrix equations: [11].

\begin{align}
Q_{\alpha i} &= C_A(V_{\alpha i} - V_{G1}) + C_B(V_{\alpha i} - V_{\beta i}) + C_D(V_{\alpha i} - V_{\alpha2}) + C_E(V_{\alpha i} - V_{\beta2}) + C_H(V_{\alpha i} - V_{G2}) \\
Q_{\beta i} &= C_B(V_{\beta i} - V_{\alpha i}) + C_C(V_{\beta i} - V_{sub}) + C_E(V_{\beta i} - V_{\alpha2}) + C_D(V_{\beta i} - V_{\beta2}) + C_K(V_{\beta i} - V_{sub}) \quad (1)
\end{align}

\begin{align}
V_{\alpha i} &= \bar{Q}_{\alpha i}/C_A + \bar{Q}_{\beta i}/C_B + \bar{Q}_{\alpha2}/C_D + \bar{Q}_{\beta2}/C_E + \bar{Q}_{G1}/C_H + \bar{Q}_{G2}/C_K \\
V_{\beta i} &= \bar{Q}_{\alpha i}/C_B + \bar{Q}_{\beta i}/C_C + \bar{Q}_{\alpha2}/C_D + \bar{Q}_{\beta2}/C_E + \bar{Q}_{sub}/C_K
\end{align}

FIG. 1: (a) Double floating-gate (DFG) structure. $T_{ox1}$, $T_{ox2}$ and $T_{CG}$ are oxide thickness between lower FG and substrate, between two FGs, and between upper FG and control gate, respectively. $q_{A1}$, $q_{B1}$, etc. are stored charges in those capacitances. (b) We consider two cases of device parameters.
(\(i = 2,1\) when \(i = 1,2\)). \(V_{\text{sub}}\) is a substrate bias and we set \(V_{\text{sub}} = 0\). (ii) Once potential energies of FGS are determined, electric field applied on each oxide is calculated as the difference of potential energies of FGS. For example, electric field between the stacked FGS is given by \(E_{\text{sub}} = (V_{\beta_i} - V_{\text{sub}})/T_{\text{oxi}}\). (iii) Current through each oxide is calculated by a direct tunneling model applied electric field \(E\) as \(J(E) = A E^2 \exp[-B(1 - (1 - ET_{\text{oxi}}/\Phi_b)^{3/2})/E]\) with \(A = e^4 m_{\text{si}}/(16\pi^2 h m_{\text{ox}} \Phi_b)\) and \(B = 4\sqrt{2} m_{\text{ox}} \Phi_b^{3/2} / (3he)\). (iv) Then, new charge distribution is obtained, namely, \(Q_{\beta_i} \Rightarrow Q_{\beta_i} + (J_{i} - J_{2i}) dt\) with the current that flows through the lowest tunneling oxide \(J_{i}\) and the middle tunneling oxide \(J_{2i}\) during time \(dt\). We repeat this calculation until charge distribution is stabilized by adjusting small time advance \(dt\). To determine stored charge and WRITE/ERASE process for a given gate voltage \(V_{\text{prg}}\), we start from trial charge \((10^{-6} \text{ C/cm}^2)\) and repeatedly apply \(V_{\text{prg}}\) and \(-V_{\text{prg}}\) a couple of times. The retention behavior is described under \(V_{\text{G}} = 0\), starting from the stored charges.

**Numerical results.**—First, we found that DFG is more stable when \(T_{\text{oxi}} = T_{\text{ox2}}\). For example, charge distribution of \(T_{\text{oxi}} = T_{\text{ox2}} = 5 \text{ nm DFG} \) begins to change later than that of \(T_{\text{oxi}} = 6 \text{ nm and } T_{\text{ox2}} = 4 \text{ nm DFG}\). Thus, we consider DFG with \(T_{\text{oxi}} = T_{\text{ox2}}\). This is because charge distribution begins to change through the thinnest tunneling oxide.

Figure 2(a) shows stored charges for programmed “00” states in case I. (We obtain a similar behavior for case II.) We define “0” state as a negative charge stored state (programmed state) such as \(Q_{\alpha} + Q_{\beta} < 0\) and “1” as a charge unstored state such as \(Q_{\alpha} + Q_{\beta} > 0\). For DFG, the upper FG stores negative charges similar to the FG of SFG, whereas the lower FG stores positive charges as if DFG constructs an “artificial electric dipole”. Figure 2(b) shows the threshold voltage shift \(\Delta V_{\text{th}}\) for DFG and SFG. For given charges \(Q_{\alpha}\) and \(Q_{\beta}\), \(\Delta V_{\text{th}}\) is obtained by Eqs. (11) as a gate voltage shift when \(E_{\text{prg}} = 0\). For “00” state, \(\Delta V_{\text{th}}\) is given when \(E_{1,1} = E_{1,2} = 0\) and, for “01” state, \(\Delta V_{\text{th}}\) is given only for the left cell when \(E_{1,1} = V_{\text{G}} = V_{\text{prg}}/2\). We can see that the magnitude of \(\Delta V_{\text{th}}\) of the DFG is one-fourth smaller than that of the SFG. This is because positive charge and negative charge cancel electric fields with each other and the electric field outside the dipole structure of DFG is weaker than that outside a single charge structure of SFG. This indicates that DFG is less appropriate for memories using multi-levels than SFG. In Figs. 2(c)(d), we show that the WRITE/ERASE speeds are almost the same in both structures. This is because the speed is mainly determined by the same \(T_{\text{oxi}}\). The peaks of DFG in the figures originate from different charges of \(Q_{\alpha}\) and \(Q_{\beta}\) and appear when the sign of \(Q_{\alpha} + Q_{\beta} \) is changed. Because the charge distribution in our model is symmetric for \(V_{\text{G}} > 0\) and \(V_{\text{G}} < 0\), the smaller memory window of DFG in Figs. 2(c)(d) corresponds to twice the \(\Delta V_{\text{th}}\) in Fig. 2(b).

Figures 3(a)(b) show retention characteristics, that is, transient degradations of \(\Delta V_{\text{th}}\) of DFG and SFG for “00” and “alone” states. We can see that \(\Delta V_{\text{th}}\) of DFG exceeds that of SFG at \(\sim 10^{10} \text{ sec for case I and at } \sim 10^6 \text{ sec for case II}\). Thus, retention time of DFG in “00” state is longer than that of SFG. The peak of DFG \(\Delta V_{\text{th}}\) appears when \(Q_{\alpha} + Q_{\beta} \) begins to decrease. Note that \(\Delta V_{\text{th}}\) of “alone” state starts from negative region. Thus, the interference between cells is effective for DFG. Programming voltage for “01” state is different from that for “00” state. In Fig. 3(c)(d), negative voltage is applied to store negative charge for DFG and SFG of \(V_{\text{G}} = 0\). These are results of the complicated electromagnetic fields produced by Coulomb interactions among FGS. In any case, \(\Delta V_{\text{th}}\) of “01” state in DFG become larger than those of SFG even in this thin \(T_{\text{oxi}} \leq 5\text{nm}\) region. (We have similar relation between DFG...
The charging energy of the system can be expressed by summing charging energy of all capacitors such as $U_{th} = \sum q_i^2/(2C_i) - \sum q_i V_i$ where $q_i$ shows charge of each capacitor and $V_i$ shows charge of capacitor that connects to gate voltage (see Fig. 1). By using Lagrange multipliers similar to Ref. 3, we have the charging energy of two DFGs as $U_{DFG} = U_1 + U_{II} - \sum_{i=1}^{2}(C_A V_{G_1} + C_H V_{G_1})/2$, where

$$U_1 = \frac{D_1 w_{g_1}^2 + D_2 w_{g_2}^2 + 2C_p w_{g_1} w_{g_2}}{2[D_1 D_2 - C_g^2]}$$

$$U_{II} = (C_{a_1} v_{g_1}^2 + C_{a_2} v_{g_2}^2 + 2C_D v_{g_1} v_{g_2})/(2\Delta)$$

with $v_{g_i} = C_A V_{G_1} + C_H V_{G_1} - q_i^{DFG}$ and

$$v_{g_i} = \left\{ \frac{C_D C_{E_1} + C_{a_1} C_{B_1}}{\Delta} \right\} v_{g_i} + \left\{ [C_D C_{B_1} + C_{a_1} C_{E_1}] / \Delta \right\} v_{g_i} - q_i^{DFG}$$

including $C_{a_1} = C_{a_1} + C_B + C_D + C_E + C_{H_1}$, $C_{B_1} = C_{B_1} + C_{G_1} + C_G + C_{E_1} + C_{K_1}$, $\Delta \equiv C_{a_1} C_{a_2} - C_D^2$, $D_1 \equiv C_{B_1} - C_{a_1} C_{B_1} + C_{a_1} C_{E_1} + 2C_D C_{E_1} C_{B_1}/\Delta$, and $D_2 \equiv C_{G_1} + C_{a_1} C_{B_1} + C_{a_1} C_{E_1} + C_{B_1} C_{B_1} + C_{E_1} C_{E_1} C_{B_1}/\Delta$. Note that $U_{DFG}$ has the same form as $U_{II}$ with capacitances replaced by those of SFG such as $C_{S_1}^2$, $C_{S_1}^2$ etc. For “00” state ($w_g = w_{g_1} = w_{g_2}$ and $v_g = v_{g_1} = v_{g_2}$), we have,

$$U_1 = w_{g_1}^2/(D - C_g), \quad U_{II} = v_{g_1}^2/(C_A - C_D)$$

For SFG, we have $U_{SFG} = v_{g_1}^2/(C_A - C_D) = (C_A + C_H) V_{G_1}^2$ where $C_{S_1}^2 = C_S^2 + C_{S_1}^2 + C_{D_1}^2 + C_{D_1}^2 + C_{I_1}^2$ and $v_g = (C_A + C_H) V_{G_1} - q_i^{SFG}$.

In summary, we numerically showed that interfering DFGs have a longer retention time than SFGs, although DFGs have the disadvantage of smaller threshold voltage shift and smaller memory window. Owing to the existence of additional FG, DFG shows unique transient characteristics, forming an artificial electric dipole.

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