Frequency Compensation of Three-Stage OTAs to Achieve Very Wide Capacitive Load Range

H. Aminzadeh¹, Member, IEEE, Andrea Ballo², Member, IEEE, and Alfio Dario Grasso², Senior Member, IEEE
¹Department of Electrical Engineering, Payame Noor University (PNU), Tehran, Iran
²Dipartimento di Ingegneria Elettrica Elettronica e Informatica (DIEEI), University of Catania, I-95125 Catania, Italy
Corresponding author: A.D. Grasso (e-mail: agrasso@dieei.unict.it).

ABSTRACT This paper proposes an optimal design approach for three-stage amplifiers driving an ultra-wide range of load capacitor. To this end, efficient state-of-the-art solutions have been combined to develop a power-efficient frequency compensation solution. High-speed feedback pathways relying on Miller capacitors and current buffers are implemented within the amplifier scheme to push the non-dominant poles to high frequencies for small to medium load capacitors. A small resistor is also shared between the two pathways to improve the stability regardless of the load capacitor. A serial R-C branch is then added to extend the lower limit of load drive capability to small load capacitors. Gain margin is, for the first time in literature, analytically evaluated and included in the design phase. A prototype of the proposed amplifier is fabricated in 65-nm CMOS process with active area of 0.0017 mm² and 1.15 pF total compensation capacitance. It can drive the load capacitor range from 200 pF to 100 nF, while drawing a quiescent current of 7.4 µA from a 1.2-V input voltage supply. A unity-gain frequency of 1.67 MHz was measured with an average slew-rate of 1.31 V/µs, when the proposed amplifier is wired in unity-gain configuration to drive a 500-pF load capacitor.

INDEX TERMS Amplifier; frequency compensation; local impedance attenuation; Miller compensation; quality factor; stability; wide load range.

I. INTRODUCTION
A large DC gain is a prerequisite for realizing operational transconductance amplifiers (OTAs) with high accuracy. A high DC gain is, however, difficult to achieve in nano-scale CMOS technologies, since scaling MOS devices decreases their intrinsic gain as well [1, 2]. In conventional CMOS technology, the DC gain of an amplifier could be readily increased by stacking more transistors in a cascode configuration. The reduced power supply of the integrated circuits (IC) in modern technology nodes, however, leaves little voltage headroom for stable operation of cascaded devices, rendering more convenient the use of cascaded gain-stages to construct multistage amplifier topologies for high-precision applications. Nonetheless, additional low-frequency poles in the voltage-gain transfer function of cascaded amplifiers complicate their stability in feedback configuration. Many frequency compensation techniques have thus been introduced [3-5], allowing the researchers to propose new design procedures depending on the application requirements [6-12]. Multistage OTAs are the fundamental block of many critical modules in an integrated system such as low-dropout linear regulator (LDO), voltage and current references, capacitive micro-electro-mechanical systems (MEMS) sensors, analog-to-digital and digital-to-analog converters, continuous-time and switched-capacitor filters, audio amplifiers, and finally active-matrix liquid crystal display (LCD) drivers [13-17].

The load capacitance, $C_L$, experiences significant changes by several orders of magnitude in some of these applications [13], implying that the OTA must remain stable over a wide range of capacitive loads [4, 18-24]. For many years, nested Miller compensation (NMC) was the classical scheme to design stable multistage amplifiers in feedback configuration [25, 26]. The right-half plane (RHP) zero associated with the Miller capacitance, together with the necessity of additional capacitors for compensating the inner gain stages of NMC amplifier, however, reduces its maximum bandwidth and leads to poor performance metrics [26]. Many variants of NMC amplifier have thus been proposed [27-33], along with some solutions for eliminating the Miller compensation capacitors altogether [20, 34, 35]. Despite looking attractive for a multistage
amplifier, removing the Miller capacitors comes with degraded power efficiency, since extra feedback loops and more biasing current would be required to compensate the inner gain-stages.

Alternatively, single-Miller compensation (SMC) resorts to the solutions which construct a stable multistage amplifier using one Miller capacitor, \( C_m \), only [33, 36]. In this category, cascode-Miller compensation topologies (Miller compensation employing current buffer) exhibit better power/area efficiency for those OTAs driving large capacitive loads, since the required \( C_m \) would be a function of \( \sqrt{C_L} \) rather than \( C_L \) in the classical Miller compensation [37-40]. Cascode-Miller compensation can be combined with local impedance attenuation (LIA), in the form of a serial \( RC \) branch, to extend the drivable load range of a three-stage OTA to small load capacitors [37]. Similar approaches demonstrated maximum efficiency for ultra-large capacitive loads but still show limited efficiency for small \( C_L \) [39, 41, 42].

In view of this shortcomings and in order to enable very wide capacitive load range with low quiescent power and small active area, this work introduces a compensation topology based on Hybrid Cascode frequency compensation, local Impedance attenuation and Resistor (HCIAR) for three-stage amplifiers and provides the analysis and design insights to drive light to heavy capacitive loads. The proposed OTA, in particular, is \( C_m \) compensated for small to medium load capacitors, becoming smoothly \( C_L \) compensated for large capacitive loads. As a result, the load capacitor range is extended to about 500x from 200 pF up to 100 nF using an overall compensation capacitor of 1.15 pF in 65-nm CMOS technology. In addition to analytical discussions, simulation and measurement results will be reported and compared with the prior art in the rest of this paper. The main contributions of this work are summarized below:

1. By combining the advantages of the compensation topologies introduced in [37] and [39], a novel compensation strategy is introduced exploiting also an additional compensation resistor in the main compensation path;
2. Gain margin is, for the first time in literature, analytically evaluated and included in the design phase;
3. A general design procedure to guarantee stability of the amplifier for both small and large load capacitors is introduced;
4. Experimental results show an outstanding 500x capacitive load driving range without reconfiguring the amplifier which, to the best of authors’ knowledge, is the highest reported in literature.

The paper is organized as follows. At first, Section II describes the conceptual block diagram, principles of operation and stability conditions of the proposed compensation strategy. Next, in Section III we discuss about the circuit implementation, large-signal operation and design guidelines of the amplifier. Simulation and measurement results are then presented in Section IV, where a comparison with the state-of-the-art is carried out. At last, conclusions are drawn in Section V. Some ancillary calculations and a comparison between the proposed solution and similar works in the literature are included in the Appendices.

II. HYBRID CASCODE FEEDFORWARD COMPENSATION WITH LOCAL IMPEDANCE ATTENUATION AND RESISTOR

A. AMPLIFIER DIAGRAM

Fig. 1 shows the proposed HCIAR amplifier diagram. It is composed of a differential first stage, a non-inverting second stage, and an inverting third stage with the equivalent transconductances \( g_m1, g_m2 \) and \( g_m3 \), respectively. Each stage output resistor and capacitor are also modeled by \( R_i \) and \( C_i \), where \( i = 1,2,3 \). As it will be shown in the next subsection, the feedforward stage \( g_{mf} \) has a negligible effect in the amplifier transfer function but is added to implement a class-AB output stage capable of driving \( C_L \) with increased charging/discharging rate [40].

![Figure 1: Conceptual block diagram of the proposed HCIAR amplifier.](image-url)

Frequency compensation is accomplished mainly by a single Miller capacitor which is equally split into two parts, \( C_m/2 \), to create a dual feedback network from the output to the first stage. Going forward, we will show that such arrangement yields larger non-dominant poles with smaller quality factor, \( Q \), in contrast to a single feedback configuration made by a monolithic \( C_m \). Superior stability margins are thus achieved compared to the prior SMC solutions [24, 37, 38, 40, 42].

What’s more, two current buffers with transconductance \( g_{mc} \) and input resistance \( 1/g_{mc} \) are cascaded with Miller capacitors to assist in feeding the output compensating current back to the first stage. The reduced input resistance \( 1/g_{mc} \) of the two current buffers lightens the loading effect of the Miller capacitors on the output terminal which leads to extended bandwidth. The described feedback pathways share a small compensation resistor denoted by \( R_c \), through which an extra left-half plane (LHP) zero is created and used for improving stability by introducing some phase lead to the external loop. Besides the above-mentioned...
components for frequency compensation, HCIAR includes a serial RC branch at the second stage output \((R_D \text{ and } C_D)\). Aimed at reducing the \(Q\)-factor of the non-dominant poles, the corresponding branch is meant for decreasing the lower limit of \(C_L\) by increasing the gain margin (\(GM\)) in the small load capacitors.

### B. TRANSFER FUNCTION

An estimation of OTA open-loop transfer function allows exploring its stability and bandwidth variations as a function of the load capacitor. Using the results reported in Appendix A and under the assumptions that:

1. the equivalent transconductance of all stages is much greater than their output conductance \((g_{m2}g_{m2}g_{mL} \ggg 1/R_i)\);
2. the nulling resistor \(R_C\) is much lower than \(R_D\) and both are much smaller than the output resistors \((R_C << R_D << R_i)\);
3. the compensation capacitors are much lower than the load capacitor and all are much larger than the parasitic capacitors \((C_i >> C_C, C_D >> C_i)\).

the simplified amplifier transfer function, using the methodology described in [43], can be expressed by

\[
A(s) \approx \frac{A_0 \left[1 + \frac{s}{\omega_0} \left[1 + \frac{s}{\omega_0} \left[1 + \frac{s}{\omega_0} \right] \right] \right]}{1 + \frac{s}{p_{-3dB} \left[1 + \frac{s}{Q\omega_0} \left[1 + \frac{s^2}{\omega_0^2} \left[1 + \frac{s}{p_4} \right] \right] \right]}} \tag{1}
\]

where

\[
A_0 = g_{m2}g_{mL}R_2 + g_{mL} \approx g_{m2}g_{mL}R_1R_3 \tag{2}
\]

is the DC gain and

\[
p_{-3dB} \approx \frac{1}{g_{m2}g_{mL}R_2R_3C_C + R_3C_L} \tag{3}
\]

is the magnitude of dominant pole frequency. The \(Q\)-factor and center frequency of standard second-order polynomial in the denominator of (1) are respectively expressed by

\[
\omega_0 = \sqrt{\frac{2g_{m2}g_{mL}R_D}{C_1C_L}} \tag{4}
\]

\[
Q = \frac{C_C}{2g_{m2}g_{mL}C_L} \tag{5}
\]

Finally, the magnitude of the remnant poles and zeros is given by

\[
p_4 = \frac{1}{R_D + \frac{C_L}{g_{m2}g_{mL}R_1C_C}}C_D \approx \frac{1}{R_D C_D} \tag{6}
\]

\[
p_5 = \frac{1 + \frac{2g_{mL}R_D C_2}{1 + 2g_{mL}R_D C_2}}{R_D C_2} \approx \frac{1}{R_D C_2} \tag{7}
\]

From (6) and (10) it is apparent that there is an inherent pole-zero cancellation due, as usual, to the serial RC branch at the second stage output.

Referring to (4) and (5), the following points can be stated.

1. Enlarging the load capacitor decreases the \(Q\)-factor of the pole pair, generating ultimately real poles.
2. The coefficient “2” in (4) and (5) is in favor of amplifier performance; originating from the parallel feedback loops in the proposed configuration, this factor moves the non-dominant poles to higher frequencies and reduces their \(Q\)-factor as compared to a single feedback loop.
3. The effect of \(R_D\) on both (4) and (5) is worth investigating. The \(Q\)-factor is now proportional to \(R_D\) rather than \(R_2\) in the absence of the RC circuit at the second stage output [37, 38], enabling to reduce \(Q\) via \(R_D\), without sacrificing the DC gain of the second stage. Too small \(R_D\) is, however, unsuitable since it moves \(\omega_0\) to low frequencies. Hence, its value should be tuned for an optimal location of the pole pair depending on the application requirements.

The first LHP zero, \(z_1\), depends on either \(R_C\) and \(R_D\), and can be used to counteract part of the negative phase shift caused by non-dominant poles. The second right-half plane (RHP) zero, \(z_2\), is inversely proportional to the parasitic \(C_i\). It is thus positioned well beyond the gain-bandwidth product (\(GBW\)) and can be pushed further to the higher frequencies by increasing \(R_C\). Besides, from the expressions of \(A_0\) and \(p_{-3dB}\) in (2) and (3), the \(GBW\) is given by

\[
GBW = \frac{g_{mL}C_C}{C_L + \frac{g_{m2}g_{mL}R_2R_3}{2g_{m2}g_{mL}C_L}} \tag{11}
\]

The above relation simplifies to the usual expression \(g_{mL}C_C\) for small to medium load capacitors (i.e., \(C_L \ll k_{m2}g_{mL}R_1R_2C_L\)), changing smoothly to \(g_{m2}g_{mL}R_1R_2R_3C_L\).
for heavy capacitive loads. The GBW is thus scaled down with $C_L$ for $C_L \gg g_{m2} g_a R_1 R_2 C_L$, which shows that the proposed amplifier is compensated by the load capacitor rather than by $C_L$ for large load capacitors.

Fig. 2 shows the pole-zero map of HCIAR amplifier, and the changes of its pole magnitudes with respect to $C_L$. The complex and conjugate $p_2$ and $p_3$ become real for higher $C_L$, while the dominant pole moves closer to the origin consistent with (3).

C. ANALYSIS OF STABILITY

The phase margin (PM) related to (1) is carried out in the eq. (33) in Appendix B, which allows finding the PM limits when $C_L$ tends to zero and infinity as

$$\lim_{C_L\to0} PM \approx \tan^{-1} \frac{R_P C_C}{g_m \left( R_C C_C + R_D C_D - \frac{C_1}{2 g_m g_a 2 g_m R_C R_D} \right)}$$

(12)

$$\lim_{C_L\to\infty} PM \approx \tan^{-1} \frac{R_P C_C}{g_m R_C C_D}$$

(13)

The limits in (12), (13) can be made positive and sufficiently large by properly sizing the contributing components from the compensation network. In particular, the stability of the OTA will be guaranteed for ultra-large load capacitors by adequately enlarging the PM limit in (13).

With reference to (36) in Appendix B, the $GM$ becomes negative by letting $C_L$ approach to zero. The closed-loop stability can thus be ensured only for the load capacitors larger than a threshold. Indeed, to get a positive $GM$ we must fulfill the condition

$$\frac{2 g_m}{g_m} \left[ 1 + \frac{g_m g_a 2 g_m R_D}{C_1 C_L} \left( \frac{R_P C_D^2 - \left( \frac{R_P R_D C_C}{R_C C_D + R_D C_D} \right)^2}{2 g_m g_a 2 g_m R_C R_D} \right) \right] > 1$$

(14)

which yields a minimum $C_L$ given by

$$C_{L,\min,GM} = \frac{g_m g_a 2 g_m R_D}{C_1 \left[ 1 - \frac{g_m}{2 g_m} \left( \frac{R_P R_D C_C}{R_C C_D + R_D C_D} \right)^2 \right] + \frac{C_1}{2 g_m g_a 2 g_m R_C R_D} \left( R_D C_2^2 \right)^2}$$

(15)

A more conservative choice of the minimum $C_L$ is according to the maximum tolerable $Q$-factor, $Q_{max}$, of complex and conjugate non-dominant poles, since decreasing $C_L$ increases accordingly the $Q$-factor as is evidenced by (5), thus yielding

$$C_{L,\min, Q} = \frac{g_m g_a 2 g_m R_D c^2}{2 g_m Q_{max}^2 C_1}$$

(16)

Both (15) and (16) indicate that the minimum capacitor of the proposed structure is dependent on $R_D$ rather than $R_2$ in the absence of the RC circuit at the output of the second stage. The serial RC branch thus lowered the minimum $C_L$ owing to the additional $GM$ recovered by this block at small capacitive loads. Moreover, the $GM$ is monotonically increasing by letting $C_L$ approach infinity according to (36)

$$\lim_{C_L\to\infty} GM \approx 20 \log \left( \frac{2 g_m C_L}{g_m g_a 2 g_m R_D R_C C_D} \right)$$

(17)

The above relation shows that the stability for the ultra-large load capacitors is affected only by the $PM$ and not the $GM$.

III. DESIGN CONSIDERATIONS

A. CIRCUIT IMPLEMENTATION

Fig. 3 illustrates a possible transistor-level representation of the HCIAR diagram in Fig. 1, where the original $g_m$-stages are implemented by their counterparts in dashed lines. It consists of an input folded-cascode stage, a current-mirror second stage with a positive gain factor for the negative feedback sign of the external loop, and a common-source third stage. The first stage is an inverting differential amplifier made up of $M_{1a}$–$M_{1b}$ as the input pMOS pair, $M_{3a}$–$M_{3b}$ and $M_{4a}$–$M_{4b}$ as cascode devices, $M_{5a}$–$M_{5b}$ as current mirror for fully-differential signal to single-ended conversion, and $M_{6}$, $M_{2a}$–$M_{2b}$ as biasing current sources. The second stage is made by $M_0$ as input device, $M_{7a}$–$M_{7b}$ as current mirror, and $M_8$ for bias generation. Transistor $M_{7c}$ is also exploited to increase the equivalent transconductance of the second stage [31, 37].

![FIGURE 3. Circuit implementation of the HClAR amplifier.](image-url)
The output stage is formed by $M_9$ and $M_{10}$ with rail-to-rail voltage levels for maximizing the OTA dynamic range in low-voltage environment. Push-pull operation is implemented through $M_{10}$ connected to the first stage output, whose transconducance is equivalent to $g_{mC}$.

The components used for frequency compensation are the serial $R_D$ and $C_D$, dual $C_C$ Miller capacitors, and $R_C$. Hybrid cascode Miller compensation has been implemented by the Miller capacitors coupling the left-hand side of $R_C$ and the source of common-gate $M_{3b}$ and $M_{4b}$ devices, through which the $g_{mC}$ stages in Fig. 1 are realized without any power overhead.

In the analysis carried out in Section II, it was assumed that the transconducance of transistors $M_{3b}$ and $M_{4b}$ is equal. Although perfect matching can be hardly met, being the two devices a $n$MOS and a $p$MOS transistor, respectively, it is worth noting that feasible mismatch percentages between the transconducance of these devices changes slightly the location of the poles and zeros derived in Section II. Detailed analysis of mismatch between the two feedback transistors is carried out in Appendix C, where it is shown that the location of the poles and zeros would be changed slightly by the mismatch between the transconductances of $M_{3b}$ and $M_{4b}$.

Contrary to the asymmetrical compensation network that can be made by the whole $C_C$ [37, 38], a balanced operation is resulted by the proposed arrangement during the rising and falling of the output voltage. Further comparison between the proposed work and similar solutions in the literature is left to Appendix D.

### B. LARGE-SIGNAL OPERATION

The setting response is impacted by the OTA large-signal operation and, in particular, its slew rate (SR) besides the small-signal performance metrics like the stability margins and the $GBW$. Defined as the highest changing rate of an output voltage, the SR depends on the maximum biasing currents available to charge and discharge the capacitors lumped at the different nodes of the circuit.

In Fig. 3, by denoting $I_{a1} = I_{C1} = I_{a2} = I_{L}$, and $I_{a3} = I_L$ as the maximum currents that can be delivered to charge/discharge the load capacitors, $C_{L1} = C_C/2 + C_C/2 = C_C$, $C_{L2} = C_D$, $C_{L3} = C_D + C_L$, of the first, second and third stage, respectively, and assuming that the load and compensation capacitors are much higher than the parasitics, the SR can be approximated as the minimum between the slew rate for the first, second and third stage, thus:

$$SR \approx \min \left( SR_1, SR_2, SR_3 \right) = \min \left( \frac{I_{a1}}{C_{L1}}, \frac{I_{a2}}{C_{L2}}, \frac{I_{a3}}{C_{L3}} \right)$$  \hspace{1cm} (18)

The overall $SR$ is likely limited by $SR_3$ for lighter $C_L$ becoming identical to $SR_1$ for the heavy load capacitor range. A push–pull output stage is formed by $M_{10}$ in Fig. 3, which helps to improve the large-signal operation by modestly increasing the output current for faster changing rate of the output. A slew-rate enhancer may be also added to temporarily boost the load current while driving ultra-large capacitive loads [24].

### C. NOISE ANALYSIS

The input-referred noise spectral density, $S_{n,in}$, of the proposed HIWAR amplifier is dominated by the first stage in Fig. 3, since the noise contribution of the last stages is divided by the gain factor of the former stages when referred to the input. The main noise components of the input stage are due to the flicker and the thermal noise of $M_{1b} - M_{1b}$, $M_{2b} - M_{2b} b$ and $M_{3b} - M_{3b}$. Consequently, the following input-referred noise spectral density is derived:

$$S_{n,in} \approx 2 \left[ S_{n,M_1} + \left( \frac{g_{m,M_2}}{g_{m,M_1}} \right)^2 S_{n,M_2} + \left( \frac{g_{m,M_3}}{g_{m,M_1}} \right)^2 S_{n,M_3} \right]$$  \hspace{1cm} (19)

where $g_{m,M_1}$ and $S_{n,M_i}$ are the transconducance and the noise spectral density of the $i$-th transistor, respectively. Splitting the Miller capacitor into equal parts and the serial current buffers effectively doubles $g_{mC}$ relative to single-Miller compensation solution. Less biasing current would be then required for prescribed stability margins by assuming unchanged $g_{mD}$ factors, enabling to lower the current of $M_{2b} - M_{2b}$ and $M_{3b} - M_{3b}$ and, eventually, their contribution on the input referred noise of the amplifier.

### D. DESIGN GUIDELINES

The proposed OTA can be designed in different ways depending on the load capacitor range, and nominal $GBW$ or noise requirements imposed by the application. In this section, we shall describe the main design considerations of HIWAR topology being useful for primitive hand calculations. For simplicity, we assume that $C_L$ is not affecting the $GBW$, thus this parameter can be expressed as $g_{mD} C_L$.

We also assume that the output resistors and capacitors are extracted initially by circuit simulation. Of course, these critical components can be revised/updated recursively when developing an iterative computer-aided design flow.

We start our design procedures by sizing the $RC$ circuit of the second stage output. The main purpose of this block is to overcome the parasitic pole generated by $R_2$ and $C_2$ and to move it to the high frequencies, as is evident from the analysis in Section II. At this purpose, $R_D$ and $C_D$ should be set such that the second stage output impedance approaches $R_0$ within the frequency range of concern, say between $0.1 \times GBW$ and $10 \times GBW$. After routine manipulations, these elements can be obtained as [42]

\[1\text{Note that this assumption is true if the nominal load capacitor is sufficiently small (usually up to hundreds of pF).}]}
\[ R_D = \min \left( \frac{0.1}{C_2 \times GBW}, \frac{1}{C_2 \times GBW} \right) \] (20)

\[ C_D = \max \left( \frac{100 \times C_2}{R_D \times GBW}, \frac{10}{R_D \times GBW} \right) \] (21)

The sizing of \( C_C \), on the other hand, should be according to the desired location of the non-dominant pole pair. Choosing \( \omega_0 \) equal to \( \beta \times GBW \) (where \( \beta \) may be nominally selected between 2 and 3 to allow enough \( GM \) and \( PM \) for the unity-gain OTA), \( GBW=g_{m2}/C_C \) can be combined with (4) to get

\[ \omega_0 = \beta \cdot GBW \Rightarrow C_C = \beta g_{m2} \sqrt{\frac{C_1 C_L}{2 g_{m2} g_{mL} R_D}} \] (22)

In addition to the center frequency of the pole pair, their \( Q \) factor also influences the time and frequency response of an OTA. Choosing \( Q = \sqrt{2} \) is convenient for many applications since it shapes the frequency response according to the Butterworth approximation with maximally flat band, hence

\[ Q = \frac{\sqrt{2}}{2} \Rightarrow \frac{g_{m2} g_{mL}}{g_{mL}} = \frac{C_1 C_L}{R_D C_C} \] (23)

Substituting \( g_{m2} g_{mL} \) from (23) into (22) gives

\[ g_{mL} \approx \frac{\beta}{\sqrt{2}} g_{mi} \] (24)

which simplifies (22) into

\[ C_C = \sqrt{\frac{g_{m2} C_1 C_L}{g_{m2} g_{mL} R_D}} \] (25)

The sizing of \( g_{mi} \) and, subsequently, \( g_{mL} \) in (24) and (25) is according to the nominal \( GBW \), thus

\[ g_{mL} \approx GBW \cdot C_C \] (26)

The transconductances \( g_{m2} \) and \( g_{mL} \) should then be evaluated such that (23) is fulfilled. Despite the usefulness of (23) as the starting point, simulations should be carried out to track the variations of \( GBW, PM \) and \( GM \) across the capacitive load range for the transconductance values to be optimized accordingly.

In the end, \( g_{mL} \) should be also set to

\[ g_{nf} = g_{nL} \] (27)

in order to maintain the balance of the last stage.

The resistor \( R_C \) is finally sized such that the first zero is positioned at the desired \( \alpha \times GBW \) location higher or lower than the \( GBW \) frequency [7], thus from (8) and (26) we get

\[ z_1 = \alpha \cdot GBW \Rightarrow R_C = \frac{R_D C_D}{\alpha g_{m2} R_D C_D - C_C} \] (28)

It is also important to check the frequency of the second RHP zero, \( z_2 \), after \( R_C \) being determined from (28), since its location also depends on \( R_C \) in the transfer function. Choosing \( |z_2| > 10 \times GBW \) as a safe margin to avoid the negative phase shift of \( z_2 \) deteriorating the frequency response, we get

\[ z_2 > 10 \cdot GBW \Rightarrow R_C > \frac{\frac{g_{m2}}{g_{mL}} \cdot C_C}{\frac{g_{m2}}{g_{mL}} \cdot C_C} \] (29)

After the analytical phase, simulation of the parasitic poles and zeros against the process, voltage and temperature (PVT) variations is required to fine tune the compensation elements for the increased robustness in presence of these inevitable changes. A prototype of HCIAR amplifier was implemented based on the above design procedures, and with the aid of an algorithm which optimizes the transistor aspect ratios for minimum silicon footprint and power consumption given the nominal \( GBW \), settling time, DC gain, dynamic range, and capacitor load range [44].

IV. VALIDATION RESULTS

A. SIMULATION RESULTS

Simulations were conducted in a standard 65-nm CMOS technology using MOS devices operating at 1.2-V power supply, in order to validate the HCIAR amplifier design. The design was optimized for minimum power consumption and maximum bandwidth over the load range of 200 pF and 100 nF. The amplifier occupies a total area of 0.0017 mm² with the current consumption of 7.4µA.

Table I summarizes the device aspect ratios while Table II reports the performance specifications for the nominal \( C_L \) of 500 pF, together with DC bias currents, \( g_m \) values, and output resistors.

The loop-gain frequency response is depicted in Fig. 4(a) for different load capacitors. In line from the limited \( SR \), originating from the limited quiescent current of the output stage, the OTA is found to be unconditionally stable with a minimum \( C_L \) of 200 pF, which is coherent with the analysis. The dominant pole is initially observed as a function of the Miller capacitance for small capacitive loads, becoming slowly a function of \( C_L \) for large load capacitors.

Fig. 4(b) shows the settling response of the unity-gain amplifier to the rising and falling edges of an input step voltage.

Fig. 5 shows the Monte-Carlo simulations results of the DC gain, UGF, and phase margin at \( C_L=500pF \). The average values of these parameters are 107.29 dB, 2.49 MHz, and 60.71° with a standard deviation of 0.16 dB, 0.05 MHz, 0.66°, validating the robustness of the proposed
amplifier against the local mismatches consistent with the performance parameters of different measured samples.

Figs. 6(a)-(b) report the OTA loop-gain and step response for a $C_L$ equal to 200 pF when taking into account the temperature variations (−25°C to 85°C) and supply voltage fluctuations (±5%) across the various process corners.

It can be observed that the OTA remains stable across the PVT corners, while the nominal and worst-case 0.1% positive/ negative settling time are 1.26/1.40 μs and 1.46/1.71 μs, respectively, according to Fig. 6(c).

The simulated PSRR+/ PSRR- are found as 181.7/188.6 dB at DC, dropping to 135.1/136.6 dB and 17.75/20.00 dB at 1 KHz and 1 MHz, respectively, for $C_L = 500$ pF. The DC CMRR is also obtained as 71.96 dB. Finally, the equivalent input noise is equal to 172 nV/√Hz at 100 kHz.

![Monte-Carlo simulation results of DC gain, UGF and PM](image)

**TABLE I. TRANSISTOR ASPECT RATIOS**

| Device | Value   | Device | Value   |
|--------|---------|--------|---------|
| $M_9$  | $2 \times 0.7 \mu / 2.1 \mu$ | $M_{7b}$ | $3 \times 0.4 \mu / 0.5 \mu$ |
| $M_{10a}$ | $2.5 \mu / 2.9 \mu$ | $M_{7b}$ | $0.4 \mu / 0.5 \mu$ |
| $M_{11a}$ | $3 \times 1.1 \mu / 3.9 \mu$ | $M_{7b}$ | $2 \times 0.3 \mu / 0.9 \mu$ |
| $M_{12a}$ | $2.2 \mu / 1.0 \mu$ | $M_{8}$ | $3 \times 0.7 \mu / 2.0 \mu$ |
| $M_{13a}$ | $3.1 \mu / 1.0 \mu$ | $M_{8}$ | $3.5 \mu / 0.2 \mu$ |
| $M_{14a}$ | $5.4 \mu / 0.8 \mu$ | $M_{10}$ | $3 \times 2.4 \mu / 0.2 \mu$ |
| $M_{5b}$ | $2.0 \mu / 0.2 \mu$ |

![Simulated response for different load capacitors: (a) open-loop gain and phase; (b) step response in unity-gain configuration.](image)

![Operation of the OTA in different process corners for $C_L = 500$ pF; (a) Loop-gain frequency response; (b) Step response; (c) 0.1% settling time.](image)
B. MEASUREMENT RESULTS

The proposed HCIAR amplifier was fabricated in a standard 65-nm process. Fig. 7(a) shows the chip micrograph incorporating the 0.0017-mm² layout of the amplifier.

The experimental setup is displayed in Fig. 7(b). It consists of a waveform generator (right-side) and two power supplies (left side). An oscilloscope, Tektronix TDS5054B, was also used to measure the input and output signals for transient response. Finally, setup configuration involves also a E5061B LF-RF network analyzer (ENA) provided by Keysight technologies, which was used to measure the amplifier response in the frequency domain.

Fig. 8 illustrates the loop-gain frequency responses for the $C_i$ range from 200 pF to 100 nF. The DC gain is extrapolated as around 107 dB, and the $GBW$ is 2.01 MHz and 0.03 MHz with a phase margin of 60.1° and 72.7° for 200 pF and 100 nF load capacitors, respectively.

Fig. 9 shows the settling response to a 400-mV input step voltage for the unity-gain OTA. The average SR is measured as 1.86 V/μs and 0.01 V/μs for 200 pF and 100 nF load capacitors, respectively.

![Fig. 7. (a) Chip micrograph of the circuit shown in Fig. 3; (b) experimental setup.](image)

![Fig. 8. Measured loop-gain for different capacitive loads from 200 pF to 100 nF.](image)

![Fig. 9. Measured large-signal step responses for the capacitive loads from 200 pF to 100 nF.](image)

Fig. 10 summarizes the $GBW$, $PM$ and settling time variations for different load capacitors. Overall, the settling response correlates well with simulation results, but a longer settling time was appreciated due to the loading effect of the experimental setup.

Performance parameters have been measured over 6 samples and a good stability is observed being the relative standard deviation lower than 5% in all cases unless for the offset voltage whose average value is 0.28 mV with a standard deviation of 7.24 mV.
B. COMPARISON

Table III presents the performance metrics of the proposed HCIAR amplifier and compares them with the results from some of the state-of-the-art OTAs.

The standard figures of merit, $\text{IFOM}_{\text{SA}} = \text{GBW} \times C_{\text{Lmax}}/I_{\text{DD}}$ and $\text{IFOM}_{\text{LA}} = \text{SR} \times C_{\text{Lmax}}/I_{\text{DD}}$, were used to characterize the small-signal and large-signal operations for the maximum load capacitance, while $\text{IFOM}_{\text{SA}} = \text{IFOM}_{\text{LA}}/\text{Area}$ and $\text{IFOM}_{\text{LA}} = \text{IFOM}_{\text{SA}}/\text{Area}$ were added to also take into account the silicon area.

With the aim of including in the comparison also the stable and drivable load capacitor range, the figures of merit $L_R-\text{IFOM}_{\text{SA}} = \text{IFOM}_{\text{SA}}/C_{\text{Lmin}}$ and $L_R-\text{IFOM}_{\text{LA}} = \text{IFOM}_{\text{LA}}/C_{\text{Lmin}}$ are then introduced. A lower total $C_C$ was achieved in [24] for comparable current consumptions (0.50 pF vs. 1.15 pF) but the minimum $C_C$ for stable operation is limited to 5 nF rather than 200 pF in the proposed implementation.

In the absence of Miller capacitor, the capacitor-less frequency compensation solution in [20], on the other hand, increases significantly the current consumption to maintain stability as compared to this work (185 $\mu$A vs. 7.4 $\mu$A). The measured DC gain was also limited to about 71 dB for heavy load mode. Similarly, the required current consumption of the design in [18] with a DC gain of 107 dB is comparatively high owing to the conventional Miller compensation solution applied (146 $\mu$A). A total compensation capacitance of 3.1 pF was also incorporated to stabilize the amplifier. Overall, the proposed OTA achieved the highest $L_R-\text{IFOM}_{\text{SA}} = \text{IFOM}_{\text{SA}}$ and $L_R-\text{IFOM}_{\text{LA}}$ among the OTAs listed in Table III, when taking into consideration the range of stable operation, active area, current consumption and small-signal and large-signal operations altogether.

\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline
Technology [nm] & 350 & 350 & 350 & 130 & 130 & 65  \\
Area [mm$^2$] & 0.016 & 0.003 & 0.0025 & 0.007 & 0.006 & 0.007  \\
$I_{\text{DD}}$ [µA] & 72 & 24.9 & 6.36 & 146 & 185 & 7.4  \\
$S_R$ [dB] & $>100$ & $>100$ & 113 & 107 & 71.25 & $-110$  \\
$C_C$ [pF] & 1–15 & 5–15 & 5–100 & 0.4–12 & 4.45–50 & 0.2–100  \\
$C_P$ [pF] & 2.6 & 1 & 0.5 & 3.1 & 1 & 1.15  \\
CMRR [dB] & N/A & N/A & N/A & N/A & N/A & N/A  \\
PSRR+PSRR− [dB] & 80 dB @ 1 kHz & N/A & N/A & N/A & N/A & N/A  \\
$C_{\text{max}}/C_{\text{min}}$ & 15 & 3 & 20 & 20 & 12.24 & 500  \\
$\text{GBW}$ (MHz) & 2.85–2.38 & 2.88–0.43 & 2.75–1.18 & 5.41–0.46 & 2.01–0.03  \\
$S_R$ [V/µs] & 0.59–0.22 & 0.76–0.3 & 0.36–0.045 & 0.92–0.14 & 0.49–0.04 & 1.86–0.01  \\
$P_M$ [°/µs] & 83–52 & 78–47 & 46–59 & $>48$ & 69–90 & 60–73  \\
$1\%$ $t_{\text{f}}$ [µs] & 1.28–4.49 & 0.63–0.93 & 2.05–7.7 & 0.33–9.75 & 0.57–4.62 & 1.15–91.3  \\
$\text{IFOM}_{\text{SA}}$ & 198 & 1433.7 & 6761 & 97 & 124.3 & 405.4  \\
$\text{IFOM}_{\text{LA}}$ & 45.8 & 180.7 & 707.6 & 11.51 & 10.81 & 135.1  \\
$\text{IFOM}_{\text{SA}}$ & 12'370 & 482.7 & 2'704'403 & 13'855 & 20'721 & 238'474  \\
$\text{IFOM}_{\text{LA}}$ & 2'865 & 60.8 & 283'019 & 1'644 & 1'801 & 79'491  \\
$L_R-\text{IFOM}_{\text{SA}}$ & 12.37 & 96.5 & 540.9 & 36.6 & 4.7 & 1'192.4  \\
$L_R-\text{IFOM}_{\text{LA}}$ & 2.86 & 12.1 & 56.6 & 4.1 & 0.4 & 397.5  \\
\hline
\end{tabular}
\caption{Comparison of the proposed amplifier with prior art}
\label{table:comparison}
\end{table}

* Simulated results (500pF load capacitor)

\begin{align}
\text{(1)} \quad \text{IFOM}_{\text{SA}} &= \frac{\text{GBW} \cdot C_{\text{Lmax}}}{I_{\text{DD}}} \frac{\text{MHz}}{\mu\text{A}} \\
\text{(2)} \quad \text{IFOM}_{\text{LA}} &= \frac{\text{SR} \cdot C_{\text{Lmax}}}{I_{\text{DD}}} \frac{\text{V}}{\mu\text{A} \cdot \mu\text{F}} \\
\text{(3)} \quad \text{IFOM}_{\text{SA}} &= \frac{\text{GBW} \cdot C_{\text{Lmax}}}{I_{\text{DD}}} \frac{\text{MHz}}{\mu\text{A} \cdot \mu\text{m}^2} \\
\text{(4)} \quad \text{IFOM}_{\text{LA}} &= \frac{\text{SR} \cdot C_{\text{Lmax}}}{I_{\text{DD}}} \frac{\text{V}}{\mu\text{A} \cdot \mu\text{m}^2} \\
\text{(5)} \quad L_R-\text{IFOM}_{\text{SA}} &= \frac{\text{GBW} \cdot C_{\text{Lmax}}}{I_{\text{DD}} \cdot \text{Area}} \frac{\text{MHz}}{\mu\text{A} \cdot \mu\text{m}^2} \\
\text{(6)} \quad \text{IFOM}_{\text{LA}} &= \frac{\text{SR} \cdot C_{\text{Lmax}}}{I_{\text{DD}} \cdot \text{Area}} \frac{\text{V}}{\mu\text{A} \cdot \mu\text{m}^2}
\end{align}
V. CONCLUSION
The stability of multistage OTAs is compromised by the wide range of capacitive loads is of concern. An efficient design methodology and, subsequently, high-performance frequency compensation solution were proposed in this work to improve the operation of three-stage amplifiers with ultra-wide load capacitor range. The proposed compensation network is comprised of identical compensation capacitors for cascode-Miller compensation, a small resistor for positive phase shift and enhanced stability, and a serial RC network for extending the drivable load range to small load capacitors. Verified by analysis, simulation and measurement results, the proposed OTA establishes an optimal stability/bandwidth trade-off over a very wide load capacitor range. The figures of merit related to power consumption, silicon area, and load capacitor range reveal superior performance metrics compared to the previous arts.

APPENDIX A. Simplification of the Amplifier Diagram
The transfer function of the circuit shown in Fig. 1 can be simplified by combining the parallel feedback pathways through identical $C_0/2$ and $g_{mc}$ stages in Fig. 11(a) and merging them in the form of a single $C_0$ in series with $g_{mc}$, as graphically depicted in Fig. 11(b). Indeed, in Fig. 11(a), $i_F$ can be expressed in terms of $v_i$ and the intermediate nodal voltage $v_O$ as

$$i_F = 2g_{mc} \left[ \frac{1}{g_{mc}} + \frac{1}{C_0 s} \right] v_O + 0.5 g_{sw} \left[ \frac{2}{C_0 s} \right] v_i$$

whereas in Fig. 11(b), $i_F$ can be written as

$$i_F = 2g_{mc} \left[ \frac{1}{g_{mc}} + \frac{1}{2C_0 s} \right] v_O + g_{sw} \left[ \frac{1}{2g_{mc} + C_0 s} \right] v_i$$

Both models induce the same $i_F$ in the output of the first stage, which proves that they are equivalent owing to the symmetry in the original configuration. Consequently, the HCIAR block diagram in Fig. 1 can be simplified as shown in Fig. 11(c) with $C_0$ in series with a $2g_{mc}$ stage.

APPENDIX B. Gain and Phase Margin Evaluation
Neglecting the pole-zero pair $z_3-p_3$, the phase margin of the transfer function (1) is expressed by the well-known expression

$$PM = 180^\circ - \tan^{-1} \left( \frac{GBW}{p_{z3b}} \right) - \tan^{-1} \left( \frac{GBW}{\omega_0 Q (1 - GBW^2/\omega_0^2)} \right)$$

$$+ \tan^{-1} \left( \frac{GBW}{\omega_2} \right) - \tan^{-1} \left( \frac{GBW}{p_4} \right) \approx$$

$$\approx \tan^{-1} \left( \frac{1}{GBW} \right) - \frac{1}{\omega_0 Q (1 - GBW^2/\omega_0^2)} + \frac{1}{z_1} + \frac{1}{z_2} + \frac{1}{p_4}$$

where the approximation holds assuming that $z_1$, $z_2$ and $p_4$ are located at frequencies higher than $GBW$ and recalling that $\tan(90^\circ - \alpha) = 1/\tan(\alpha)$ and that $\tan(\alpha + \beta + \chi) \approx \tan(\alpha) + \tan(\beta) + \tan(\chi) + \ldots$ for small $\beta$, $\chi$, $\ldots$ values. Substituting (3)-(11) into (32) yields (33) at the bottom of the page.

From the gain margin (GM) definition, it can be similarly found from (1) as

$$GM = -20 \log \left[ \frac{1 + (pX/\omega_0)^2}{1 + (pX/\omega_0)^2 + (pX/\omega_0 Q)^2} \right]$$

where $PX \approx \omega_0$ is the phase crossover frequency.
GM \approx 20\log \left( \frac{2g_{mc}}{g_{mi}} \left( 1 + \frac{C_L}{g_{mc}g_{ml}R_D R_C C_L} \right) \right) + 20\log \left( 1 + \frac{g_{mc}g_{ml}R_D R_C C_L}{R_g C_L} \left( \frac{R_g C_L}{R_C C_L + R_D R_D} \right)^2 - \left( \frac{C_L}{2g_{mc}g_{ml}R_D} \right)^2 \right) 

(36)

Considering that in general \sqrt{1+x^2} \approx 1 + 0.5x^2 and (1 + 0.5x^2)/(1 + 0.5y^2) \approx 1 + 0.5x^2 - 0.5y^2 for small x and y, eq. (34) can be approximated as

GM \approx 20\log \left( \frac{Q \cdot GBW}{2g_{mc}} \right) + 20\log \left( 1 + \alpha_i \left( \frac{1}{Z_i} + \frac{1}{Z_j} \right) \right) 

(35)

Substituting (3)-(11) in (35) yields (36) at the top of the page.

APPENDIX C. Mismatch between feedback transconductances

Being different type of devices with unequal aspect ratios, the inevitable mismatch between the transconductances of M\_3 and M\_4, which forms the parallel feedback pathways in Fig. 3 is a concern which requires further investigation.

Denoting with \( g_{mc1} \) and \( g_{mc2} \) the equivalent transconductances of these devices, respectively, the general form of the feedback current \( i_F \) in Fig. 11(a) is obtained as

\[ i_F = \left( g_{mc1} + g_{mc2} \right) \left( g_{mi} v_i + C_s v_o \right) \]

(37)

Let \( g_{mc1} = g_{mc} \) and \( g_{mc2} = g_{mc} + \Delta g_{mc} \), where \( \Delta g_{mc} \) models the effect of mismatch, we get

\[ i_F = \left[ \frac{1}{2g_{mc} + C_c s} \left( g_{mc} + \frac{g_{mc} + \Delta g_{mc}}{1 + \frac{2\Delta g_{mc}}{2g_{mc} + C_c s}} \right) \right] \left( g_{mi} v_i + C_s v_o \right) \]

(38)

With reference to the above result, Fig. 12 modifies the previously described amplifier model shown in Fig. 11(c). The two diagrams are analogous for the small mismatch errors between \( g_{mc1} \) and \( g_{mc2} \) when \( \Delta g_{mc} \ll 2g_{mc} + C_c s \), except that the original \( 2g_{mc} \) prior to the first stage output will be replaced by \( 2g_{mc} + \Delta g_{mc} \) in presence of mismatch.

By means of the modified amplifier model in Fig. 13, analysis of the transfer function reveals that the location of the poles and zeros is changed slightly by \( \Delta g_{mc} \). For instance, the \( Q \)-factor and the center frequency of the second and the third poles (Eqs. (4) and (5)) are modified to

\[ Q = \frac{1 + \frac{\Delta g_{mc}}{2g_{mc} C_c s}}{2g_{mc} C_c s} \]

(39)

FIGURE 12. Effect of the mismatch between \( g_{mc1} \) and \( g_{mc2} \).

APPENDIX D. Analytical comparison of the Proposed Work with other Solutions

The block diagram of an improved SMC [33], CLIA [37] and HCFC [39] compensation topologies is shown in Fig. 13. Their transfer function can be approximated by (1) but with the expression of natural frequency, quality factor and zeros summarized in Table IV. For analogous parasitic capacitors and transconductance values and depending on the gain factor \( g_{mc} R_D \) (or \( g_{mc} R_2 \)), SMC yields a natural frequency much lower than the rest, which is because of the advantage of cascode compensation over the classical Miller compensation.
Assuming equal values for $R_2$ and $R_D$, HCFC and HCIAR topologies have a value of $\omega_0$ which is higher by a factor of $\sqrt{2}$ and, at the same time, a value of $Q$ which is reduced by the same factor. This means that the amplifiers HCFC and HCIAR achieve the same stability margins with smaller compensation capacitance, and thus lead to $GBW$ and SR improvements.

To get similar performance of HCFC and HCIAR, CLIA amplifier must entail a doubled value of $g_{mC}$ which comes at higher power/area consumption.

However, from Table IV it is apparent that $\omega_0$ and $Q$ of HCFC is a function of $R_2$. This parameter cannot be set independently from $g_{mC}$ and, in turn, without changing the DC gain of the OTA. In the proposed HCIAR topology, like in CLIA, $\omega_0$ and $Q$ are a function of $R_D$, rather than $R_2$, which is a physical resistor that can be set according to the guidelines provided in Section III.D.

As a further advantage of the proposed scheme, the first LHP zero, $z_1$, depends on either $R_C$ and $R_D$ similar to improved SMC, and can be used to counteract partly the negative phase shift caused by non-dominant poles, thus allowing to increase $PM$ for equal $C_C$ or reduce $C_C$ for equal $PM$.

Therefore, we can conclude that HCIAR takes advantage of the benefits of SMC, CLIA and HCFC and introduces increased intrinsic performance by exploiting resistor $R_C$.

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Hamed Aminzadeh (’S05–’M10) received the M.S. and Ph.D. degrees in electronics engineering in 2008 and 2010, respectively. From 2010 to 2014, he was with the Delft University of Technology, the Netherlands, where he worked on low-voltage power regulation techniques for biomedical implanted devices. Since 2012, he has been also with Payame Noor University, Tehran, Iran, where he is currently an associate professor. His current research interests include modeling and optimization of analog circuits for low-voltage IoT and biomedical devices, and low-power digital-to-analog and digital-to-analog converters design for telecommunication applications. He has coauthored more than 50 papers on international journals and conference proceedings.

Andrea Ballo (’M20) was born in Catania, Italy, in 1990. He received the Laurea degree (summa cum laude) and the Ph.D. degree in electronic engineering from the University of Catania, Italy, in 2016 and 2020, respectively. From 2021 he is a research fellow and Adjunct Professor of electronic engineering at the University of Catania, Italy. His current research interests include low-voltage low-power analog and mixed electronics for energy harvesting circuit design and applications.

Alfio Dario Grasso (S’99–M’03–SM’15) was born in Catania, Italy, in 1978. He received the Laurea degree (summa cum laude) and the Ph.D. degree in electronic engineering from the University of Catania, Italy, in 2003 and 2006, respectively. From 2006 to 2011 he worked as a freelance engineer in the field of electronic systems. From 2009 to 2010 he was an Adjunct Professor of electronics at the University of Enna, Italy. In 2011 he became a Researcher (Assistant Professor) and in 2015 he was appointed an Associate Professor at the University of Catania. In 2017 he received the Italian National Scientific Qualification for the position of Full Professor. He teaches graduate courses on advanced VLSI digital design, microelectronics and basic electronics. Prof. Grasso is an Associate Editor at the IET Electronics Letters, at the Wiley International Journal of Circuits Theory and Applications and at the Journal of Circuits, Systems and Computers and is a member of the editorial board of MDPI Sensors. His current research interests include low-voltage low-power analog circuit design and analog and mixed signal processing for energy harvesting applications. He has coauthored more than 100 papers on referred international journals and conference proceedings.