Selective SHI irradiation for mesa type edge termination in semiconductor planar junction

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Abstract. A mesa type edge termination in planar junction structures has been devised by involving vibrational energy localisation in crystalline medium leading to atomic scale reordering of host atoms on the boundary of enclosed irradiated region. A fabrication process based on selective MeV ion beam irradiation on a square shaped planar abrupt p-n junction is presented to realize semiconductor junction structures with near ideal electrical characteristics. The experimental validation of the process provides compatibility with microelectronics and suits for Schottky diode structures employing silicon carbide (SiC).

1. Introduction
Planar semiconductor abrupt junction structure is the backbone of larger section of solid state devices and circuits without which electronics as a whole ceases in its present form. Planarity is an advantage to support continuous miniaturization of the electronic structure on one hand while associated edge effects tend to reduce operating capability and long term stability due to unavoidable design and fabrication related deficiencies [1]. Suppression of curvature effects associated with active region of junction region is a challenge in planar structures [2]. This problem becomes grim with continuous decreasing size of the structures. Mesa type edge termination of semiconductor junction has been considered an ideal way to suppress curvature and edge effects but it is limited to larger size of discrete structures [3,4]. A number of planar junction termination techniques have been developed but for partial improvement [5,6,7,8,9]. There is no mesa type junction termination techniques so far suggested for miniaturized planar junction structures. With the advancement in semiconductor technology and improved understanding in ion-solid interactions, localized modifications in the crystalline structures at nano level are suggested and experimentally shown to introduce for their further applications as junction edge termination [10,11]. This type of termination resembles with mesa and has been found compatible with microelectronics involving miniaturized planar structures.

Basic process of selective SHI irradiation and mechanism responsible for localized reordering of discrete system at nano level with modified electronic properties is explained in next section. Curvature effects in planar semiconductor junction structures and conventional approaches adopted for their suppression is presented in the followed section. Experimental results are presented thereafter on...
a model planar square shaped abrupt p-n junction to validate selective SHI irradiation in mesa type termination. The results are discussed with emphasis on selective SHI irradiation as viable planar junction termination technique suitable for SiC schottky diode.

2. Selective SHI irradiation and localized reordering
Interaction of swift heavy ions with crystalline semiconductor can be classified into two broad categories: blank exposure to the entire medium and selective exposure using thick metal mask. Blank exposure of MeV ion beams is usually carried out and reported in published literature for imparting common ion-fluence initiated modifications in different materials [9]. Employment of selective irradiation of few hundreds of MeV ion beam so that the exposed region is enclosed by protective mask of thick metal, results however, in hot and cold regions [12]. The very nature of electronic energy loss mechanism in the exposed region leaves the crystalline medium unchanged while the ions are implanted deep into the bulk. The energy transfer from the incident ions to the local atoms result in energy localization, which also traverse along the atomic high ways. The localized energy is finally dissipated at the interface of irradiated and masked regions of the medium and results in the modification of atomic arrangement within few tens of nano-meters. The reordering of atoms at the interface of closed exposed region has been experimentally shown in crystalline silicon using 200 MeV Ag+14 ion beam with a metal mask of nickel in the shape of a square mesh of 40 µm grid size. The reordered nanostructure having modified electronic properties isolate the exposed region with bulk material by encircling it in the lateral direction and therefore offers a mesa type edge termination [10, 12].

The swift heavy ions equipped with energy of hundreds of MeV interact with crystalline silicon atoms close to the surface and lose their energy through inelastic collision. The sudden impact of large energy results in localized excitation, which moves from atoms to atoms leaving no sign of structural modification to the exposed region of the silicon target. However any dislocation or defect present in the crystalline silicon is also swept away along with the moving localized energy packet. This way the silicon crystal becomes more clean from unwanted defects and dislocations which are invariably generated during crystal growth. The continuous exposure of the swift heavy ions to the enclosed silicon region using thick metal mask, initiates a region full of moving energy packets towards the boundary of the exposed region. At the interface of the exposed and un-exposed region, these energy packets release their localized energy, which is dissipated in terms of rearrangements of local atoms under the thick metal mask. The rearrangement of silicon atoms under the impact of large energy dissipation induces reordering of silicon atoms.

Balance in nonlinearity and discreteness in the system causes energy localization. Presence of defects and dislocations within a lattice is a known source of energy localization termed as Anderson localization. Nonlinear science provides theoretical proofs of energy localization even in perfect crystals; short range dynamics, Intrisic localized mode (ILM), Discrete Breathers, Solitary waves. Nonlinear periodic lattices occure in a large variety of systems, such as biological molecules, nonlinear optical waveguides, solid-state systems and Bose-Einstein Condensates. The underlying dynamics in these systems is dominated by the interplay tunneling between adjacent potential wells and non-linearity. A balance between these two effects can result in a self localised state: a lattice or discrete soliton. The discreteness of space is important in; solid state physics, photonic crystals, coupled optical wave guides, coupled Josephson junctions, Bose-Einstein condensates in optically induced lattices and micromechanical cantilever systems [11,13,14].

3. Planar junction
A planar p-n junction is a key electronic entity in the fabrication of integrated circuits. Using planar technology, each individual electronic component can be realized on the semiconductor wafer by processing individually selected regions. A p-n junction fabricated using planar process is always terminated at the surface of the semiconductor wafer where it is exposed to the outer environment.
Termination of a planar junction on the surface is therefore associated with a curvature in the diffused p-n junction geometry \([1,6]\). Secondly, the window through which a planar p-n junction is formed, introduces another curvature to the junction geometry \([2]\). The shape of the junction geometry on the semiconductor surface and the curvature associated with the metallurgical p-n junction inside the semiconductor, cause multidimensional effects which lead to higher leakages and reduced avalanche breakdown voltages in planar abrupt p-n junctions. However in case of linearly graded junction the electric field enhancement due to metallurgical junction curvature is not found to be crucial but its termination at the surface can not be avoided due to the planar process. The impurity profile is responsible for the realisation of abrupt and linearly graded junctions.

On the basis of symmetry, planar junctions are classified into three categories; plane junction, cylindrical junction and the spherical junction. A plane junction is the ideal form of a p-n junction having one dimensional doping profile on either side of the junction. This kind of a plane junction model is helpful to identify the limits of a practical p-n junction. A planar p-n junction formed by using a long rectangular window results in a cylindrical junction, while a junction formed through a sharp corner is modeled by a spherical junction. Electric field enhancement in a planar p-n junction with spherical symmetry is maximum, in comparison to cylindrical junction symmetry. A planar junction formed using a square or a rectangular window is associated with spherical symmetry at the corners, which is the deciding region for the entire junction characteristics. Square or rectangular geometries of the junction window are preferred in order to avoid semiconductor material wastage. However degradation in the reverse characteristics restricts such sharp corner geometries for planar junction formation. This is the reason that junction geometries with rounded corners are preferred for improved characteristics with less semiconductor area wastage \([2]\). The rounded corner structures provide junction breakdown in between spherical and cylindrical with less wastage of device material thus making it more economical.

In planar junctions, the edge region governs controlling of electrical characteristics of the device made therefrom, mainly due to localisation of maximum electric field in the region. Surface vicinity of the edge region further adds to the sensitivity of the device performance. At the early stages of device fabrication, when size of the devices used to be in cm or mm and no integrated circuit was introduced, mechanical or chemical bevelling was used to terminate the junction boundary at a suitable angle so that resulting electric field is not enhanced. However with the advent of IC technology and demand of miniaturized devices, planar technology restricts the use of bevelling techniques for junction edge termination. Here again, bevelling of the edge remained the limit for all possible edge terminations in planar technologies. Mesa etching has been a widely used edge termination for most of transit time device fabrications based on p-n junction and Schottky barrier \([3,4]\) as shown in figure-1 and figure-2 respectively.

![Fig-1 Mesa etching in IMPATT Diode fabrication [4]](image1)

![Fig-2 Mesa Schottky diode structures (a) Al and (b)Au metallisations [3]](image2)
4. Experimental

The experimental evidence of MeV ion irradiation induced reordering phenomena along the edges of exposed and virgin region of the targeted single crystalline silicon with modified electronic properties in terms of electronic band gap has immediate potentials for the edge termination in planar p-n junction structures. The reordered region can be used for isolating the edge region on the surface of a planar p-n junction in order to enhance its breakdown voltage as shown in figure-3. Also leakage current can be improved due to edge region isolation. Introduction of impurity for the junction formation therefore meets a sort of discontinuity around the edges. This eventually diminishes the multidimensional nature of the edge region, giving rise to a mesa type termination. Selective irradiation of MeV ion to the closed active device window provides a technique for edge effect termination without utilizing a significant chip area. Besides, selective MeV ion irradiation has potentials for dragging away defects and dislocations from the active region of the device. The implanted ions deep in to the bulk provide a shield to the surface active region from substrate.

![Fig.3 Schematics of selective irradiation of n-region of a semiconductor n-p junction](image)

**4.1 Planar p-n junction fabrication with MeV ion irradiation**

A sharp corner square window is the ideal layout for a planar p-n junction with negligible wastage of silicon material. However with these square geometries multidimensional edge effects become very prominent to degrade junction characteristics. A square geometry of a planar junction is therefore a worst shape from device behaviour point of view. Spherical symmetry associated with the sharp corner in a square geometry is advantageous to accurately estimating the breakdown voltage of the planar junction. Taking up the worst geometry of a planar junction in the shape of a square window provides two fold advantages; easy to monitor any improvement due to edge termination and accurate theoretical estimation of the breakdown characteristics. Besides, a square geometry planar junction provides a cost effective layout design in a production environment. A square of 2mm $\times$ 2mm size has been considered for the planar junction formation. A 9$\times$9 matrix of these squares with a pitch of 4.1 mm in x and y directions has been set for a 2” diameter silicon wafer.

**4.2 Process sequence**

Realisation of a p-n junction is the first process step for which a 2mm $\times$ 2mm square window in oxidized silicon surface is opened. Thermally grown oxide acts as a mask for defining the junction geometry. For a p-type of silicon substrate, phosphorous implantation is made through the window for n-type conversion leading to a step junction formation. Oxide thickness on silicon wafer is set about 1.0 $\mu$m sufficient to masking the underneath p-type silicon region. MeV ion irradiation of Ag$^{14+}$ is done on n-region of 2mm$\times$2mm through an aligned metal mask using a special jig for this purpose. After MeV ion irradiation metal mask is removed. As the bulk region of the silicon substrate is going to be blocked by the MeV ions, ohmic contact region for the p-type silicon and n-region of the junction are to be taken from the surface. A square annular window around the main junction with sufficient distance from the junction is required to be opened for p$^+$ region definition. Similarly a window for n$^+$ region on the main junction region is required for ohmic contact. Both the regions on p
and n– type silicon are realized by ion implantation using photoresist as a mask for selectivity. Metallisation on the p⁺ and n⁺ regions is done with smaller size contact regions. The fabrication process sequence is shown in figure-4.

Fig-4 Fabrication process flow of planar p-n junction with MeV ion irradiation
5. Results and discussion

A planar p-n junction is characterized by its I-V and C-V characteristics, which can be further used for estimating parameters such as substrate doping, leakage currents, on resistance, avalanche breakdown voltage. For the electrical characterization of the junction structure, wire was bonded on the wafer itself using conducting silver paste. A computer controlled test facility comprising of LCR meter and current source was employed for on line data acquisition for I-V and C-V measurements on virgin and irradiated devices. A frequency variation from 0.1 MHz to 1.0 MHz was used for C-V measurements. A typical silicon wafer carrying planar junction structure with and without irradiation is shown in figure-5. The reference of the devices on the wafer has been used for further analysis of the measured characteristics. The matrix of the device is 9×9 and if counted from the left upper corner the rows and columns will identify the location of the device on the wafer. The 5×5 matrix of the devices in the centre have been irradiated on this wafer. Device No. 55 is the centrally located and irradiated with 200 MeV Ag\(^{14}\) beam. Device No. 22 and 28 are located outside the irradiated region.

![Fig-5 A processed silicon wafer with planar junction structures. Diode No. 22 and 28 are virgin while diode No. 55 is 200 MeV Ag\(^{14}\) irradiated](image)

The circled region on the wafer shows the devices which have been irradiated using metal mask having 5×5 matrix of windows. The square grid around the centre region shows the p’ contact for the diode while centre square region shows the n’ contact pad. Dot of silver paste on the contact pads can be seen in the above figure. The device structures have also been diced using diamond saw for individual diode testing.

5.1 Forward I-V Characteristics

Forward I-V characteristics of the three devices out of which device No.-22 and device No.-28 are virgin while device No.-55 is 200 MeV Ag\(^{14}\) irradiated have been shown in figure-6 (a). The measured data has been taken up with an upper limit of 2.0 mA for the current source. The on voltage for the irradiated device is less than 1.0 volts while in case of virgin devices it is about 1.0 volt. The series resistance for the irradiated device is low than virgin devices. A 0.1 volt of incremental step was used for taking up the I-V data at room temperature in an open environment. The ln(J) versus forward voltage curves for virgin and irradiated p-n junction structures have been shown in figures-6(b) and 6(c). The curves clearly shows the G-R and diffusion dominated regimes with varying voltage. The
G-R region is narrowed down in case of irradiated device indicating removal of defects from the active region due to energy packet movement.

Fig-6 (a) Measured forward characteristics of fabricated planar p-n junction (b) Virgin diode (c) irradiated diode

5.2 Reverse I-V characteristics
The reverse characteristics of the devices have been measured for leakage currents and avalanche breakdown voltages. The virgin diodes have shown breakdown at 6.0 volts with leakage currents around 2.0 μA at 1.0 volt. The 200 MeV Ag$^{114}$ beam irradiated device has shown an improved leakage current with no breakdown at 6.0 volts. At 6.0 Volts leakage current can be found below 1.0 μA in case of irradiated diode. Characteristics of the three devices have been shown in figure-7 for the details of leakage currents. The device treated with selective 200 MeV Ag$^{114}$ beam shows marked improvements in the leakage and the breakdown voltage.

Fig-7 Measured I-V and C-V characteristics of irradiated and virgin diodes (a) reverse leakage currents (b) complete I-V Characteristics (c) C-V of virgin diode and (d) C-V of irradiated diode

The one sided abrupt planar junction of spherical symmetry with 0.1 μm radius of curvature shows breakdown voltage of 6.0 volts for a silicon substrate of 2-4 Ω cm resistivity. The virgin devices are in agreement with the theoretical limits of the breakdown voltage.

5.3 C-V Measurement
Measurement for the C-V of the fabricated planar junction devices have been performed using Agilent LCR meter 4284A connected to a computer through GPIB. The provision of frequency variation from 0.1 MHz to 1.0 MHz has been used in order to determine frequency influence on the device capacitance. Depletion and diffusion capacitances of the devices have been measured by
biasing the structures in reverse and forward mode respectively. The capacitance of forward biased p-n junction is due to excess minority carriers and therefore has relevance with the presence of defects. The C-V characteristics shown in figure-7(c) show a shooting behaviour in diffusion capacitance of virgin diode at typical frequency and forward voltage. However, no shooting behaviour is observed in case of irradiated diode C-V, as shown in figure-7(d).

5.4 Theoretical estimation of breakdown voltage

Theoretically avalanche breakdown voltage of an abrupt planar junction with either symmetry among spherical, cylindrical and plane, can be determined for a given uniform substrate doping and junction depth. In the case of under consideration, silicon substrate resistivity is of 2-4 $\Omega$ cm. The corresponding doping level can be determined using Irvin’s curve as shown in figure-8 (a). For a p-type silicon at room temperature a doping level of $4 \times 10^{15} \text{cm}^{-3}$ can be extracted from the Irvin’s curve for a p-type resistivity of 2-4 $\Omega$ cm. The coloured arrow has been put on the curves for clarity.

![Fig-8 (a) Resistivity vs. impurity concentration for p-type silicon](image1)
![Fig-8 (b) Avalanche breakdown voltage versus impurity concentration for one-sided abrupt doping profile with spherical junction geometries](image2)

The junction geometry considered in the present work is a square with sharp corners. Along the sharp corner doping diffusion follows the spherical symmetry in the formation of a p-n junction. Any p-n junction geometry associated with spherical symmetry is dominated by the spherical junction limits. Accordingly the breakdown voltage determined for the spherical junction of 0.1 junction depth and a substrate doping level of $4 \times 10^{15} \text{cm}^{-3}$ will be the breakdown for the p-n junction structure as a whole. From the computed data for one – sided abrupt silicon junction breakdown voltage of 6-7 volts is estimated for the given background doping. Coloured arrow on the curve given in figure-8 (b) shows the avalanche breakdown voltage of a spherical junction. The measurement of I-V characteristics of virgin devices has shown a breakdown voltage of around 6-7 volts, which coincides with the computed values. The improvement in the breakdown voltage and the leakage currents in case of irradiated devices is due to junction termination at its edges by reordered structures formed by the release of energy moving from the location of incident ion. The defects present in the silicon have been further flowed away by the energy wave towards the edges, resulting into diffusion capacitance without shooting up phenomenon.

Schottky diode is the special case of one sided abrupt p-n junction to require edge termination. Selective SHI irradiation has potential applications for introducing mesa type edge termination for Schottky barrier based structures employing materials like silicon carbide (SiC) and GaAs.

6. Conclusion
The measurement results of the fabricated planar abrupt p-n junction in p-type silicon with sharp corner geometry has demonstrated experimentally the usage of selective MeV ion irradiation for depositing large amount of energy on phonons through localization of vibrational energy and its further movement in the lateral direction to its release at the interfaces of virgin and irradiated silicon causing reordering in a narrow dimensions. The termination of the planar junction edges has been carriedout by the presence of reordered structures at and near the surface of the junction. A mesa type edge termination has been realized by the reordered structures. The technique is unique in its implementation as the incident ions are not in direct use for the modification of the material properties rather the energy released by them. A 8-10 times improvement in the breakdown voltage is due to elimination of the multidimensional effects. A sharp corner planar junction geometry is the worst case for the multidimensional effects based degradations in the breakdown characteristics. The improvement in the breakdown voltage from 6 volts to 50 volts has been a very effective usage of the reordered structures for junction termination. The movement of defects and disorder from the active region of silicon by the energy waves has been confirmed by the improved C-V. The technique can be utilized for producing high quality of single crystalline materials with a controlled treatment of few hundreds of MeV ions irradiation particularly in case of thin layers of materials.

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