Performance of capacitively coupled active pixel sensors in 180 nm HV-CMOS technology after irradiation to HL-LHC fluences

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ABSTRACT: In this ATLAS upgrade R&D project, we explore the concept of using a deep-submicron HV-CMOS process to produce a drop-in replacement for traditional radiation-hard silicon sensors. Such active sensors contain simple circuits, e.g. amplifiers and discriminators, but still require a traditional (pixel or strip) readout chip. This approach yields most advantages of MAPS (improved resolution, reduced cost and material budget, etc.), without the complication of full integration on a single chip. After outlining the basic design of the HV2FEI4 test ASIC, results after irradiation with X-rays to 862 Mrad and neutrons up to $10^{16} \ (1 \text{ MeV } n_{eq})/\text{cm}^2$ will be presented. Finally, a brief outlook on further development plans is given.

KEYWORDS: Radiation damage to electronic components; Radiation-hard detectors; Radiation damage to detector materials (solid state); Radiation-hard electronics

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1 Introduction

Future upgrades of the LHC (high luminosity LHC, HL-LHC) have direct impact on the requirements for future high energy physics particle detectors [1]. Especially tracker detectors used at HL-LHC experiments will suffer from significantly higher radiation doses. For this reason, currently installed silicon pixel and strip detectors in ATLAS will have to be replaced around 2018. Intense R&D effort is done to provide improved and ready-to-use sensor technologies for the replacement.

One very promising candidate is planar silicon sensors in deep sub-micron high voltage CMOS technology (AMS 180 nm high voltage CMOS process [2]). It evolved from the classic diode-based pixel sensor where an ionizing particle deposits charge in a reversedly biased diode structure. Here, the diode is formed by a deep n-well in a p-substrate. The reverse bias voltage in the order of 100 V creates a strong electric field. This causes effective charge collection by drift and the n-well acts as potential minimum for the electrons. The novelty of the HV-CMOS sensor is that despite the high voltage applied, the deep n-well also serves as substrate for PMOS transistors placed directly on the sensor chip. Additional p-wells inside the n-well host NMOS transistors and so the full range of CMOS logic is available. We refer to this concept as “smart diodes” and in the arrangement of a pixel matrix as “smart diode array” (SDA) [3].

The sensors investigated in this report are prototype pixel sensors designed for a hybrid detector using existing readout chips. Each pixel contains first stages of signal processing on the sensor: charge sensitive amplifier, comparator with possibility of local threshold adjustment and an output stage. Together with specific HV-CMOS process properties, this creates several advantages for the use as a tracking detector:
• With a substrate resistivity of about 20 Ω·cm and a maximum allowed bias voltage of 60 V, the depletion zone extends around 15 µm into the substrate. The expected charge collected by drift is therefore in the order of 1000 electrons. This relatively low signal can still be easily detected and readout thanks to the direct in-pixel amplification. The thin depletion zone allows for a very fast charge collection that in turn leads to low sensitivity to charge trapping at lattice defects. Since charge trapping is the main reason for sensor degradation by non-ionizing radiation, a high bulk radiation hardness can therefore be expected.

• Deep sub-micron CMOS electronics can be designed to be relatively resistant to ionizing radiation. Therefore high radiation hardness of the electronics is also given.

• Low “high voltage” compared to most current particle silicon sensors.

• On-sensor signal amplification makes it possible to use AC-coupling to the readout chip. Instead of the highly complex, mechanically sensitive and expensive bump bonding, the sensor chip can be simply glued onto the readout chip. This is referred to as “capacitively coupled pixel detector” (CCPD) [4, 5].

• Current prototypes are designed to be used with the existing ATLAS pixel readout chip FE-I4 [6]. No development of a new readout ASIC is needed and the advantages of SDA sensors can be combined with the advantages of a highly developed and well known readout chip.

• The very thin depletion zone allows for thinning of the sensor to 50 µm and below. Together with capacitive coupling this leads to low material budget compared to other hybrid detectors.

• The pixel size can be made smaller because there is no size restriction from metal bumps. From the electronics side, pixel sizes down to 20×20 µm² can be easily realized [4]. Smaller pixel size leads to smaller pixel capacitance and noise, better particle position detection and lower pile-up. The latter is especially important for high luminosity detectors.

• The pixel sensor can also be operated in “virtual strip detector”-mode. The sensor electronics interconnect pixels along one dimension and encode the position along the virtual strip in the signal height. Readout can thus be realized by existing analog or digital strip readout chips. Consequently, currently developed pixel chips present an alternative for future strip detector replacements.

• The HV-CMOS process is a standard electronic production process and therefore cheap and widely available compared to customized processes. This is an attractive feature for large-area detectors like the ATLAS strip detector.

In this publication first results obtained with prototype sensors irradiated to an integrated neutron flux of $10^{16} \left(1 \text{ MeV n_{eq}}\right)/\text{cm}^2$ and a total ionizing dose of 862 Mrad are presented.
Figure 1. Schematic of the sensor pixel electronics. The circles represent transistors implemented in a radiation hard design (enclosed transistors). The dashed circles represent transistors, which are implemented as standard transistors in the first generation prototype and as enclosed transistors in the radiation hard pixel type of the second generation prototype.

2 Prototype demonstrator chips

Two small-size prototypes to test the concept in 180 nm technology are currently available: HV2FEI4v1 (first generation) and HV2FEI4v2 (second generation). Both chips are geometrically equal. The first generation uses only standard CMOS elements for the pixel logic with no optimization for radiation hardness. The second generation comprises three pixel types, two of them with radiation hard electronic elements (e.g. circular transistors) partially implemented. The schematic shown in figure 1 gives more detail on this.

Figure 2 shows the front side of the HV2FEI4v1. It is $4.4 \times 2.2 \, \text{mm}^2$ large with a pixel size of $125 \times 33 \, \mu \text{m}^2$. The 1440 pixels are arranged in 24 rows and 60 columns. Wirebond pads for the pixel- and for the strip-readout sit on respective sides of the chip. The electronics power consumption is measured to be approximately 185 mW/cm².

To study bulk damage stemming from non-ionizing radiation, four chips of the first generation were neutron irradiated in the TRIGA reactor of the Jožef Stefan Institute in Ljubljana, Slovenia [7, 8]. Two of them were irradiated to $10^{15}$ and two to $10^{16} \left(1 \, \text{MeV n}_{\text{eq}}\right)/\text{cm}^2$ ($\pm 10\%$). For each of these fluxes one chip was finally assembled into a CCPD and successfully operated. A representative test setup is shown in figure 3. Results of operation after irradiation are given below.

One second generation chip was irradiated at the CERN X-ray irradiation facility to 862 Mrad to understand surface effects of ionizing radiation. It was used to extensively study the performance of the sensor electronics after irradiation. The main results are presented below.
Figure 2. Front side of the prototype demonstrator chip HV2FEI4v1.

Figure 3. A CCPD installed on a modified FE-I4 single chip card for testing. A UXiBo board is used for communication with the sensor chip. The FE-I4 is operated with a USBpix system. Most of the testing has been done in a climate chamber, including a $^{90}$Sr radioactive source.

3 Sub-pixel encoding

The ratio of the areas of a FE-I4 readout pixel ($250 \times 100 \, \mu m^2$) and of a HV2FEI4 sensor pixel is 3:1. To realize compatibility, the output signals of three sensor pixels are summed and connected to one readout pixel (see figure 4). Each of the three sensor pixels sends a current pulse with defined and constant amplitude when being hit by a particle. These three amplitudes are chosen in a way that the pixel position can be reconstructed from the summed amplitude. The FE-I4 readout pixel is able to measure the summed amplitude and converts it into time-over-threshold (ToT) information. In the end, the address of the firing sensor pixel can be reconstructed from the address and ToT information of the corresponding readout pixel.
Figure 4 shows the ToT histogram of one FE-I4 readout pixel after CCPD exposure to a $^{90}$Sr radioactive source. This CCPD comprised an unirradiated HV2FEI4v1 chip. There are clearly three distinct peaks visible, each of them corresponding to one of the three sensor pixels routed to the readout pixel. The concept of this so-called “sub-pixel encoding” is thus proven to work. However, we had to tune the three HV2FEI4 pixels and the FE-I4 pixel by hand to be able to show the encoding. This is due to the fact that no communication between the sensor control system and the readout system was implemented. There is ongoing effort to incorporate the custom sensor control (hard- and software) into the readout control. This will then provide automated tuning for the whole sensor area.

4 Particle detection after $10^{16}$ (1 MeV n$_{eq}$) / cm$^2$ neutron irradiation

Neutron irradiation causes mainly bulk damage in the silicon substrate. This is due to interaction of the neutrons with the lattice nuclei. In the early HV-CMOS R&D-phase radiation tolerance of up to $10^{15}$ (1 MeV n$_{eq}$) / cm$^2$ was shown. Sensors worked after irradiation even at room temperature, but with a somewhat increased noise level [3, 9]. HL-LHC silicon strip sensors will see an integrated particle flux of around $10^{15}$ (1 MeV n$_{eq}$) / cm$^2$. Fluxes at the level of the silicon pixel sensors will reach even higher values. Therefore we had HV2FEI4v1 sensors irradiated up to $10^{16}$ (1 MeV n$_{eq}$) / cm$^2$.

Test results show that the sensors are still operating after irradiation and particles from a $^{90}$Sr source have been detected. The CCPD was placed between the source and a scintillation counter. The latter was used for triggering. Figure 5 shows the occupancy plot of the FE-I4 region where the small demonstrator chip is glued onto. The FE-I4 detected no hits outside this region. In addition, the level-1 trigger distribution is shown. This histogram is filled with the measured time periods between a hit signal and its corresponding trigger. One distinct peak is visible on a flat background. This verifies that we really see mostly only particles stemming from the radioactive source. The
Figure 5. FE-I4 occupancy plot and its level-1 trigger distribution of a CCPD placed under a $^{90}$Sr radioactive source (see section 4 for detailed explanation and discussion).

sensor threshold was set to a global value where the noise occupancy was below $10^{-9}$ and some exceedingly noisy pixels were masked. Later measurements with only then available improved control software for the sensor showed that the optimum threshold level lies lower than the level used for the presented measurements. New measurements with the optimum threshold setting could not be conducted, since unfortunately the CCPD got damaged during manipulation for a planned test beam measurement. Further CCPDs with samples irradiated up to $10^{16}$ (1 MeV n$_{eq}$/cm$^2$) will only be available later this year.

The non-ideal threshold setting caused the sensor to most probably only detect the high energy tail of the Landau distribution. This assumption is reinforced by the very low event rate of the sensor (below 10 Hz for the whole sensor area compared to several hundred Hz for the same scintillator area). Future measurements will include a threshold tuning of the sensor chip as well as further investigation of threshold settings.

The occupancy plot shown was recorded at an ambient temperature of 22 °C in a light-tight climate chamber (error for temperature measurements 0.2 °C). The applied bias voltage was set to -20 V. Note that the sensor temperature was about 15 °C higher due to the power dissipated by the running readout chip (measured with an infra-red camera). This holds true also for section 4.1.

4.1 Temperature and bias voltage dependence

Further measurements have been conducted to investigate the behavior of particle detection depending on temperature and bias voltage. Figure 6 shows the absolute event rate of all active sensor pixels combined for the setup described above. The bias voltage was varied between 0 V and the limit defined by the foundry (–60 V). The measurements were done at two different ambient temperatures: 22 and 5 °C. We can not see saturation of the rate at high bias voltages at room temperature. This suggests that we have not yet reached the maximum charge collection efficiency. Also at 5 °C saturation is not seen albeit a tripled event rate. Further measurements at lower temperatures and higher bias voltages will be conducted to investigate a wider parameter range.
Figure 6. Event rate (detected particles per time unit) at different temperatures as a function of bias voltage for the HV2FEI4v1 after irradiation to $10^{16} \left(1 \text{ MeV n}_{\text{eq}}\right) / \text{cm}^2$. The absolute values of this measurement bear large errors (not shown) due to a lack of automated measuring method. The graph is only intended to give a first idea of the sensor’s behavior.

4.2 Leakage current

The leakage current driven by the bias voltage has been measured at different temperatures and with chips that received different integrated particle fluxes. Results are shown in figure 7. During these measurements neither the HV2FEI4 nor the FE-I4 were powered, hence no significant amount of electrical power was dissipated. Consequently, the measured ambient temperature represents the sensor’s temperature well. This was also confirmed by an infra-red camera measurement.

The maximum leakage current is drawn at a temperature of 22°C by the chip irradiated to $10^{16} \left(1 \text{ MeV n}_{\text{eq}}\right) / \text{cm}^2$. At $-60.0 \pm 0.1 \text{ V}$ the current reaches $-74 \pm 1 \mu\text{A}$. This corresponds to $1.25 \pm 0.02 \text{ mW/cm}^2$ for the active sensor area of 5.94 mm$^2$. The chip irradiated to only 1/10 the flux ($10^{15} \left(1 \text{ MeV n}_{\text{eq}}\right) / \text{cm}^2$) shows a leakage current about 13 times smaller. Currents drawn at 22°C are about 4 times larger than at 5°C, which translates into doubling the current approximately every 8.5°C. This behavior is in very good accordance with the theoretical behavior of a volume current (see [10]).

The leakage current for the unirradiated sensor is below 25 nA, which was the detection limit of the measurement setup used.

5 Performance of electronics after 862 Mrad

Performance of HV-CMOS sensor pixels is discussed in [3, 9, 12]: good signal-to-noise ratio and nearly 100% detection efficiency was shown. The most recent measurements on radiation hard pixel types were done on the HV2FEI4v2 chip during irradiation at the CERN X-ray facility. The most important results are briefly mentioned. A more complete discussion will be published elsewhere.
Before irradiation an optimum set of chip parameters was set and the preamplifier gains of different pixels were measured. The sensor was then irradiated to a total dose of just over 860 Mrad. At each step of 100 Mrad the chip was annealed for one hour at 70°C. The preamplifier gains dropped below 20% of their initial values after having finished the last step of irradiation. However, by re-optimizing the chip parameters we could restore the gains to about 90% of their initial value (see figure 8). At the same time, the average noise only doubled from 75 to 150 electrons [11].

This result is quite promising and even more so knowing that not the whole pixel electronics are implemented in a radiation hard way. Figure 1 shows that only some transistors are enclosed and therefore can be expected to be radiation hard. The rest is implemented as standard transistors. This leaves possibilities for further improvement open, leading to even more radiation hard future generations of this chip.

6 Summary and outlook

Performance of capacitively coupled active pixel sensors in 180 nm HV-CMOS technology has been investigated. Focus lied in characterizing prototype sensors that were irradiated to HL-LHC fluences. The first two prototype generation chips have been measured separately after irradiation to $10^{16} (1 \text{ MeV n_{eq}})/\text{cm}^2$ and 862 Mrad respectively. Non-ionizing irradiation was used to study bulk damage effects. Successful operation as capacitively coupled pixel detector after irradiation has been shown, even at room temperature. Saturation of the event rate at high bias voltages has not been observed which suggests that charge collection efficiency has not yet reached its highest possible value. Leakage current studies have been performed to confirm that the radiation damage from neutron irradiation really mainly affects the sensor substrate.
Irradiation with ionizing radiation (X-rays) was performed to study surface effects on the sensor electronics. Severe degradation of the preamplifier gains after irradiation has been measured. However, regular annealing during the irradiation process improved performance. Together with optimization of sensor chip parameters we were finally able to almost reach the initial gain values again. An increased noise level has been observed after irradiation. Under real conditions for large HEP experiments, sensors might run at low temperatures and therefore less annealing occurs. More detailed studies on the influence of annealing on pixel electronics will therefore be conducted.

Further measurements will include combined non-ionizing/ionizing radiation with protons to simulate conditions of HL-LHC operation as well as possible. Operational parameters of the sensor will be further optimized and the sensor performance studied in greater detail. Radiation hardness will be improved by optimizing the design of the next prototype generation. After the small-size prototypes an engineering run is planned to produce a cheap and radiation hard full reticle size chip. The ultimate goal is to provide a pixel detector that is suitable for HL-LHC detectors. Due to the flexibility of the sensor it also offers an alternative for the necessary replacement of the ATLAS silicon strip detector.

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