An ultra-wide range (0.01–240 Gbps) transmitter with latched AC-coupled driver and dummy data transient generator

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Abstract: This paper proposes an ultra-wide range transmitter with a latched AC-coupled driver (LACD) and a dummy data transient generator (DDTG). The LACD expands the low-frequency range by preventing the capacitor discharge issue of the high-speed AC-coupled driver and the DDTG enhances the high-frequency range by generating a dummy transient pattern to stabilize the power node fluctuation induced by the dense and sparse pattern dependency in the case of coding-less application. A 24-channel test chip designed with 40-nm CMOS technology achieved an ultra-wide frequency range (0.01–10 Gbps/channel) and ultra-wide bandwidth from 0.01 Gbps (0.01 Gbps × 1 channel) to 240 Gbps (10 Gbs × 24 channels) and a high area efficiency (0.0027 mm\(^2\)/Gbps/channel). At the data rates of 5 and 10 Gbps, the jitters with DDTG were 50% lower than attained without DDTG.

Keywords: ultra-wide frequency-range, ultra-wide bandwidth, transmitter, latched AC-coupled driver, dummy data transient generator, display interface

Classification: Integrated circuits

References

[1] B. Leibowitz, \textit{et al.}: “A 4.3 GB/s mobile memory interface with power-efficient bandwidth scaling,” IEEE J. Solid-State Circuits \textbf{45} (2010) 889. (DOI: 10.1109/JSSC.2010.2040230).

[2] VESA Embedded Display Port Standard Version1.3.

[3] “IEEE standard for low-voltage differential signals (LVDS) for scalable coherent interface (SCI),” 1596.3 SCI-LVDS Standard, IEEE Std. 1596.3-1996, 1994.

[4] H. Li, \textit{et al.}: “A 25 Gb/s 4.4 V-swing, AC-coupled ring modulator-based WDM transmitter with wavelength stabilization in 65 nm CMOS,” IEEE J. Solid-State Circuits \textbf{50} (2015) 3145 (DOI: 10.1109/JSSC.2015.2470524).

[5] G.-Y. Wei, \textit{et al.}: “A variable-frequency parallel I/O interface with adaptive power-supply regulation,” IEEE J. Solid-State Circuits \textbf{35} (2000) 1600 (DOI: 10.1109/4.881205).
1 Introduction

The consumer electronics products currently on the market demand higher speed data communication as the amount of digital data required increases year by year [1]. In particular, as the generation transitions from 4K2K to 8K4K, the amount of display data has become four times as great. In the case of uncompressed real-time 8K4K 120 Hz data, the total bandwidth of at least 160 Gbps is needed, as shown in Fig. 1(a). To cope with the rapid increase of the data rate, recent system-on-chips (SoCs) for video signal processing come with high-speed interface macros with Giga-bits per second (Gbps) class bandwidth per channel and scalable multiple channels such as an embedded display port (eDP) [2], high-speed low voltage differential signaling (LVDS) [3], and a high definition multimedia interface (HDMI). In these high-speed interface macros, the operational frequency range is becoming wider and wider to ensure interoperability with legacy devices (in other words, backward compatibility).

To achieve ultra-wide range operation for the 8K4K display interfaces, we have to extend both the low-speed and high-speed ranges. However, two critical issues specific to display interfaces, one on the low-speed side and one on the high-speed side, need to be overcome.

(1) Low-speed side

In display interfaces, a transmitter has to be connected with a high-voltage receiver. An AC-coupled driver is usually used as a power- and area-efficient level shifter. In this driver, a capacitor is inserted between the low-voltage pre-driver and
the high-voltage main driver [4]. Such a driver, however, cannot operate at low speed because of the capacitor discharge issue.

(2) High-speed side

In the many specifications for display interfaces, especially panel interfaces between timing controller and display driver as shown in Fig. 1(b), data is transmitted without coding (e.g., 8b10b) in a multi-channel configuration. The panel side chips usually require high-voltage operation, low-cost analog configuration, and smaller size in order to be mounted on many flexible printed circuits (FPCs). In other words, the panel side chips cannot utilize complex digital configuration using fine processes. Moreover, low latency is needed for real-time transmitting. Therefore, coding such as 8b10b is not suitable for the panel interfaces if the goal is to realize low-cost, high-data transmitting efficiency, low latency, and circuit simplicity at the panel side. In such coding-less applications, power node fluctuation induced by the dense and sparse pattern dependency create a bottleneck that prevents enhancing the speed.

Several excellent techniques have been proposed for wide-range operation [5, 6, 7, 8, 9, 10, 11]. These techniques focus on adaptive supply voltage control to achieve wide-range operation. However, they do not address the capacitor

Fig. 1. (a) Trends in operating frequency of display interface (qualitative illustration) and (b) a use case example of the transmitter for display interface.
discharge issue of high-speed AC-coupled drivers because they do not need to connect with a high-voltage receiver and they use a DC-coupled driver. Moreover, they do not have to address the pattern-dependent jitter issue because they use coding.

In response to these issues, we propose a wide-frequency-range transmitter suitable for display interfaces that uses a new driver and circuit for stabilization of power node fluctuation.

2 Concept of dual extension

Our strategy to realize operation in the ultra-wide frequency range is dual extension: that is, to extend both low frequency and high frequency, as shown in Fig. 2.

2.1 Low-speed extension (by latched AC-coupled driver)

Fig. 3(a) shows the conventional concept utilizing the AC-coupled driver. A capacitor \( C \) between a low-voltage pre-driver (Pre-Drv) and a high-voltage off-chip driver (Main-Drv) is used as a level shifter to drive the high-voltage driver while keeping both high-speed operation and high area efficiency. However, if the circuit is operating at a low rate or transmitting a burst signal representing data that does not change for a long time, the voltage at the COUT node changes gradually at a finite electrical discharge time \( T_{limt} \), as indicated in the figure. This occurs because the electrical charge stored in the capacitor \( C \) is lost little by little through the termination resistor \( R \). Therefore, in the conventional AC-coupled driver, coding (e.g., 8b10b) is required to guarantee data transition.

Our proposed concept, illustrated in Fig. 3(b), is to make a finite electrical discharge time \( T_{limt} \) infinite by eliminating discharge and maintaining amplitude after a capacitor \( C \) to ensure low-speed or a burst-signal operation, in addition to high-speed operation. To maintain the amplitude, the Latch & Limit is used. The latch prevents electrical discharge and maintains the polarity during no transition by flowing the small current. Though the latch current enlarges the amplitude, the limiter regulates the amplitude to be constant and not large.

\( T_{limt} \) with no data transition is proportional to \( C \times V(t)/I(t) \), where \( C \) is the capacitance between Pre-Drv and Main-Drv, \( I(t) \) is the leakage current through the termination resistor \( R \), and \( V(t) \) is the voltage after \( C \). Conventionally, \( T_{limt} \) has a finite value because \( I(t) \) leaks through \( R \) and \( V(t) \) is not constant. In the proposed concept, \( T_{limt} \) can be infinite because \( I(t) \) is 0 and \( V(t) \) is a constant given in the following equation (1), where \( a \) is a constant parameter:
2.2 High-speed extension (by dummy data transient generator)

Fig. 4 shows the simulation waveform of power node fluctuation caused by dense and sparse pattern dependency. The supply voltage variation is generated by dense and sparse pattern dependency because the data transition of the display interface is not guaranteed by coding. Suppressing the voltage variation is thus crucial for reducing jitter reduction and enhancing the speed characteristic.

\[
T_{lim} = \lim_{t \to \infty} \frac{V(t)}{I(t)} = \infty
\]  

Fig. 4. Simulation waveforms of power node fluctuation caused by dense and sparse pattern dependency.

In order to reduce the jitter caused by the pattern-dependency, we employ the Data Transient Generator (DTG) in [12]. In this paper, we call DTG a DDTG (Dummy Data Transient Generator).

3 Transmitter core design

Fig. 5 shows the proposed transmitter architecture to realize the dual extension concept with a newly developed LACD and DDTG. LACD is for the low-speed extension and DDTG is for the high-speed extension.
The transmitter contains 24 data Tx channels, an adaptive-bandwidth spread spectrum clock generator (AB-SSCG) [13], a clock tree (CK tree), and a bias generator (APNBG). N-bit parallel data is multiplexed to differential serial data. The data Tx includes the LACD, which consists of a latched AC-coupled pre-driver (LACPD) and a 3.3-V low voltage differential signaling (LVDS)/current mode logic (CML) hybrid driver (LCHD) in order to connect with a high voltage receiver efficiently. AB-SSCG and APNGB are shared for all 24 channels to reduce area and power.

3.1 Latched AC-coupled driver (LACPD)
A proposed circuit diagram for the LACPD is shown in Fig. 6(a). The LACPD consists of an AC-coupled level-shifter (C), a latch, a limiter, and initialization circuits. A simple structure including a current-steering cross-coupled latch and diode-type limiter serves to reduce the area and the parasitic capacitance of the high-speed data line. Waveforms for LACPD are shown in Fig. 6(b). The differential serial data (CINP and CINM) from MUX are input to each capacitor. If the last data transition in the data toggle phase occurs, the latch permits a small current to move the amplitude to the same direction as the last transition and maintain the electric charge of the capacitor during the next phase of no transition. The limiter regulates the amplitude to be constant and not large, even if a small latch current generates an amplitude in the emission direction. The upper limit and lower limit of the COUTP and COUTM are decided by PBIAS and NBIAS respectively. In the toggle phase, the latch acts as a positive feedback mechanism and duty corrector. As a result, the pattern-dependent jitter is small and high-speed characteristics are obtained. The initialization block has the role of setting the node of COUTP to low and the node of COUTM to high during the start-up sequence to fix the initial color for the panel on the receiver side. PBIAS and NBIAS are generated by an adaptive PBIAS and NBIAS generator (APNBG) and the amplitude is then decided. PBIAS and NBIAS are adaptively controlled according to the supply voltage to prevent
jitter due to the mismatch between the amplitude limit level and the data signal amplitude’s dependence on the supply voltage.

![Circuit Diagram](image)

**Fig. 6.** Proposed LACPD circuit diagram and waveform.

Fig. 7(a) and (b) respectively show the circuit simulation result of the conventional AC-coupled driver without LACPD and the proposed LACD in order to confirm the effectiveness of the proposed LACD. The data -rate is 5 Gbps and the data -pattern is 01 toggle pattern in this time. As shown in the Fig. 7(a), the voltage at the COUTP/M node in the conventional AC-coupled driver changes gradually because of the electrical discharge. However, the proposed LACD can prevent electrical discharge and maintain the polarity during no transition as indicated in the Fig. 7(b).

### 3.2 Dummy data transient generator (DDTG)

A dummy data transient generator (DDTG) suppresses jitter caused by disturbance of the supply voltage as a result of data pattern dependency when coding (e.g., 8b10b) cannot be applied.

Fig. 8(a) and (b) show a circuit diagram and timing chart for the DDTG. The DDTG generates additional data transients (TFF) during sparse periods of the data
streams (DTL) and moves the disturbance frequency near to half of the data rate to stabilize the supply voltage. The circuit and timing chart of the DDTG shown in Fig. 8 are essentially the same as the DTG in [12].

In the Fig. 8(a), the dummy AC-coupled pre-driver is the same structure as the LACPD with the normal path in order to realize the same current characteristics as the normal path. The dummy load is the same as the gate capacitance of the main driver (LCHD). The dummy load capacitance is formed in the same pattern as the gate of LCHD and is arranged near the normal path to reduce the mismatch between the dummy load capacitance and the LCHD gate capacitance. In addition to the capacitance, we consider the resistance between the dummy pre-driver and the dummy load by layout in order to make the slope of the waveform the same as that of the normal path. For the first time in this paper, we have designed the DDTG that can operate at 24 channels. The DTG in [12] was used for only 8 channels.

![Diagram](a) Conventional AC-coupled driver  
![Diagram](b) Proposed LACD

**Fig. 7.** Simulation results of conventional AC-coupled driver and proposed LACD.

![Diagram](a) Circuit Diagram  
![Diagram](b) Timing chart

**Fig. 8.** Dummy data transient generator (DDTG) circuit diagram and timing chart.
4 Experimental results

To determine the effectiveness of the transmitter concept, we fabricated a prototype chip in a 40-nm CMOS process with seven metal layers. The chip micrograph and layout are shown in Fig. 9. Tx includes 24-channel data Tx with LACD & DDTG, MUX, delay line, clock tree, BiasGen, and AB-SSCG circuit. The core area is 0.81 mm², with the latch circuit taking up about 280 um². Area overhead of the latch circuit is less than 1%.

The prototype chip with BGA package including bonding wire was evaluated using the evaluation board shown in Fig. 10. The prototype chip was connected to a display through a PCB line, connector, and cable. The transmitted eye pattern was probed between the chip and the connector by soldering a differential probe and using a high-speed oscilloscope.

Fig. 9. Chip micrograph and layout of the prototype chip.

Fig. 10. Experimental equipment.
The transmitted eye patterns measured at 0.01, 5, and 10 Gbps to confirm the frequency range are shown in Fig. 11. A total of 24 channels were operating simultaneously. The data rate indicates that successful wide-range operation was realized and the proposed LACD can keep the amplitude successfully when the frequency is very low thanks to LACPD.

![Eye patterns measured at 0.01, 5, and 10 Gbps](image)

Fig. 11. Measured eye patterns to confirm frequency range (x-axis: time; y-axis: voltage).

The transmitted eye patterns measured at 5 Gbps are shown in Fig. 12 (24 channels are operating). As shown, the broadening of the jitter distribution was improved. The jitter was reduced from 80 ps to 40 ps due to DDTG.

![Eye patterns measured at 5 Gbps](image)

Fig. 12. Eye patterns measured at 5 Gbps (x-axis: time; y-axis: voltage).

The transmitted eye patterns measured at 10 Gbps are shown in Fig. 13 (24 channels are operating). As shown, the broadening of the jitter distribution was also improved. The jitter was improved by 50% (from 60 ps to 30 ps) thanks to DDTG.

![Eye patterns measured at 10 Gbps](image)

Fig. 13. Measured eye patterns at 10 Gbps to confirm DDTG effectiveness (x-axis: time; y-axis: voltage).

The data-patterns in Figs. 11, 12, and 13 are test image pattern whose run-length is 10. We have also confirmed that the proposed transmitter can keep the
amplitude successfully in the case of DC operation by using continuous “1” and “0” pattern though we have already confirmed the very low frequency operation at 0.1 Gbps.

Table I. Performance summary

| Process                  | [6]  | [11] | This work |
|--------------------------|------|------|-----------|
| Supply Voltage           | 1.05 V | 1 V, 1.5 V | 1.1 V, 3.3 V |
| Max Termination Voltage  | 0 V (ground reference) | 1.5 V | 3.3 V |
| Driver Topology          | CML | CMOS (SST) | LVDS/CML hybrid |
| PreDriver Topology       | CMOS | CMOS | LACPD |
| Total channel number     | 16 | 2 | 24 |
| Frequency Range@channel (max freq ÷ min freq) | 5–15 Gbps (3x) | 7.5–8.5 Gbps (1.13x) | 0.01–10 Gbps (1000x) |
| Total bandwidth range (max freq ÷ min freq) | 5–240 Gbps (48x) | 7.5–17 Gbps (2.26x) | 0.01–240 Gbps (2400x) |
| Area Efficiency@channel (w/o PLL) (mm$^2$/Gbps) | - | 0.0076 | 0.0027 |
| Coding (ex.8B10B)        | required | required | Not required |
| Skew adjust function     | No | No | Yes |
| Voltage Stabilizer function for Data Dependent Noise | No | No | Yes (DDTG) |

The performance of the prototype test chip with LACD & DDTG is shown in Table I. It is clear that the test chip achieved an ultra-wide frequency range due to the proposed LACPD as pre-driver topology and DDTG as voltage stabilizer. The total bandwidth from 0.01 Gbps (0.01 Gbps × 1 channel) to 240 Gbps (10 Gbps × 24 channels) was achieved. The measured frequency range with the propose transmitter was 333 times wider than that of the [6].

The driver topology is an LVDS/CML hybrid so as to comply with various interface standards. The channel number is 24, which is large, because the chip needs to transmit 160 Gbps 8 K/4 K 120 Hz display data using a low-cost wire-bonding package and high insertion-loss transmission line.

The area efficiency was 0.0027 mm$^2$/Gbps (w/o PLL), which is very small, because bias circuit is shared between channels and the decoupling capacitor is minimized by using DDTG for data-dependent noise. Coding is obviously unnecessary due to DDTG, and the skew adjust function can be used for a clock-forwarded parallel interface such as LVDS.

5 Conclusion

An ultra-wide range transmitter with a latched AC-coupled driver (LACD) and a dummy data transient generator (DDTG) was proposed. The LACD solved the capacitor discharge issue of the AC-coupled driver and the DDTG solved the pattern-dependent induced jitter issue of the multichannel and coding-less interface. By combined usage of the LACD and DDTG, both the low- and high-frequency
ranges were expanded. A 24-channel test chip incorporating LACD and DDTG achieved an ultra-wide frequency-range (0.01–10 Gbps/channel), ultra-wide bandwidth from 0.01 Gbps (0.01 Gbps × 1 channel) to 240 Gbps (10 Gbps × 24 channels), and high area efficiency (0.0027 mm²/Gbps/channel). At the data rates of 5 and 10 Gbps, the jitters with DDTG were 50% lower than without DDTG. The proposed techniques are applicable to most transceivers with a wide-frequency-range.

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