PPT-Multicore: Performance Prediction of OpenMP applications using Reuse Profiles and Analytical Modeling

Atanu Barai · Yehia Arafa · Abdel-Hameed Badawy · Gopinath Chennupati · Nandakishore Santhi · Stephan Eidenbenz

Abstract We present PPT-Multicore, an analytical model embedded in the Performance Prediction Toolkit (PPT) to predict parallel application performance running on a multicore processor. PPT-Multicore builds upon our previous work towards a multicore cache model. We extract LLVM basic block labeled memory trace using an architecture-independent LLVM-based instrumentation tool only once in an application’s lifetime. The model uses the memory trace and other parameters from an instrumented sequentially executed binary. We use a probabilistic and computationally efficient reuse profile to predict the cache hit rates and runtimes of OpenMP programs’ parallel sections. We model Intel’s Broadwell, Haswell, and AMD’s Zen2 architectures and validate our framework using different applications from PolyBench and PARSEC benchmark suites. The results show that PPT-Multicore can predict cache hit rates with an overall average error rate of 1.23% while predicting the runtime with an error rate of 9.08%.

Keywords Performance Modeling · Parallel Application · Shared Cache · Reuse Distance Analysis · LLVM Basic Block · Multicore Processor

Atanu Barai
New Mexico State University. E-mail: atanu@nmsu.edu

Yehia Arafa
New Mexico State University. E-mail: yarafa@nmsu.edu

Abdel-Hameed Badawy
New Mexico State University. E-mail: badawy@nmsu.edu

Gopinath Chennupati
Los Alamos National Laboratory. E-mail: cgnath.dr@gmail.com

Nandakishore Santhi
Los Alamos National Laboratory. E-mail: nsanthi@lanl.gov

Stephan Eidenbenz
Los Alamos National Laboratory. E-mail: eidenben@lanl.gov
1 Introduction

Nowadays, with the emergence of Exascale computing, multicore processors with hundreds of cores, complicated memory hierarchy, instruction pipelining, branch prediction, and aggressive speculative execution have been a standard rather than an exception, from mobile devices to supercomputers. Such complicated designs come with several challenges [73], such as the efficient use of available computing cycles and the percentage of available memory utilization. Software designers have to fully leverage modern processors’ extensive computing power, especially the parallelization primitives. One of the critical factors determining a parallel application’s performance on a multicore is the data availability to the computing units. One way to measure an application’s data availability is through its cache utilization ability, which directly impacts runtime performance.

Modeling and simulation (ModSim) tools have been used to a great extent to help in understating the limiting factors and bottlenecks on applications’ performance. Co-design, which we define as modeling both hardware and software, helps tune an application’s performance. Most of the efforts in co-design have focused on getting simulation data from cycle-accurate dynamic instrumentation tools [31, 45, 80]. However, these simulations require a large number of runs and experimentation with many hardware configurations. Such configurations include variations in cache hierarchies, core counts, and problem sizes, all of which contribute to increasing design space complexity. Using cycle-accurate dynamic simulators to model and predict performance does not scale well and usually needs days, if not weeks and months, to produce output for large-scale applications. This slowdown is the huge bottleneck of the simulation tool. A co-design framework that is accurate in terms of prediction and scalable in terms of simulation time and core count is crucial in analyzing a multicore system’s performance.

In this paper, we introduce the PPT-Multicore. It combines and extends concepts from the Scalable Analytical Shared Memory Model (SASMM) [11] and the Performance Prediction Toolkit (PPT) [25]. PPT-Multicore is a performance model based on code analysis and reuse distance (the number of unique references between two references to the same address [57]) estimation methods. PPT is a parameterized co-design framework developed to predict application runtime at Los Alamos National Laboratory. PPT relies on a high event rate Parallel Discrete Event Simulation (PDES) engine named Simian [69], written in Python, Lua, and JavaScript. Simian allows mixing both entity and process-oriented simulation models and conservative, optimistic, or hybrid operation modes.

PPT-Multicore estimates the shared and private cache hit rates and overall runtime of parallel sections of an OpenMP [29] application running on a multicore architecture. The main building blocks of PPT-Multicore are the following: (i) We translate the parallel sections of the input OpenMP application to threaded version code using the Rose compiler [54]. (ii) We collect LLVM basic block [51] labeled memory trace of the parallel sections from a sequential execution of translated code. (iii) Using this memory trace, we explore different scheduling and interleaving strategies to mimic the behavior of multi-threaded programs on shared-memory multicore. We carry out these strategies at the basic block level. (iv) We mimic traces for the private and shared caches from the sequential trace and apply a probabilistic analytical method to measure the reuse distance profiles. Using these profiles, we estimate cache hit rates of the parallel sections of OpenMP.
applications. (v) We then pass the hit rates and other application-specific information such as the number of different arithmetic operations and the total memory operations to the PPT-Multicore Simian PDES model for runtime predictions.

To evaluate our tool, we compare the predicted cache hit rates with hit rates collected from real hardware using PAPI \[81\]. We also evaluate the predicted runtime by comparing it with timings from runs on real hardware. The results show that the model accurately predicts cache hit rates and runtimes across a large set of benchmark applications. Our model can predict cache hit rates with an overall average accuracy of 98.77%, while for runtime prediction, the accuracy is 90.92%.

The contributions of the paper can be summarized as follows:

– Vastly improved memory model for private and shared caches’ hit rate predictions on multicores
– Accurate runtime prediction of parallel sections of OpenMP applications
– Predicting the performance of OpenMP applications from the single thread execution trace of the application
– Showing the predictions for various core counts without having to rerun the application.

The rest of the paper is organised as follows: Section 2 briefly discusses the OpenMP execution model and introduces reuse distance theory for both single and multicore processors; Section 3 describes our modeling approach; In Section 4, we evaluate our model and describe the results; While Section 5 discusses relevant related works, and finally Section 6 concludes the paper.

2 Background

2.1 Fork Join Model: Execution of Parallel Application

In OpenMP shared-memory programming, a program exploits parallelism using the fork-join model. Program execution begins sequentially with only the primary thread. When it encounters a parallel region pragma, the primary thread forks a team of sub-threads. By default, the sub-threads execute the code in the parallel sections independently and can access all the variables declared in the primary thread before the fork. These variables are referred to as shared variables. A programmer can also specify private variables for each thread. When the threads complete a parallel section, they synchronize and join; the program execution continues with the primary thread.

2.2 Performance Modeling of Parallel Applications

Parallel applications exploit multicores with hundreds of cores. Thus, it is important that the programs can utilize all the hardware resources available to increase performance. We can obtain valuable insight into a parallel application’s performance on real hardware by developing their performance model. Based on HW/SW co-design, performance modeling helps improve the understanding of the applications’ behavior and modify for best performance. It also helps us study the impact
of advanced architectural designs and features on performance in multicores and manycores. Therefore, we can tune an application for the best performance. We can also suggest optimal hardware for a group of applications by simulating different hardware architectures’ performance. Thus, performance modeling plays a vital role in parallel program design.

On the other hand, performance modeling and evaluation are at the heart of modern parallel computer architecture research and development. Because of the growing complexity of modern processors, architects cannot design systems based only on intuition [38]. Rigorous performance evaluation methodologies are a crucial part of modern architecture research and development.

2.3 Reuse Distance

Reuse distance (D) of a memory address, is denoted as the number of unique memory references between two consecutive references to the same address. It is also known as the LRU stack distance [57]. If a memory address is accessed for the first time, the reuse distance D for that access is $\infty$. Table 1 shows an example of reuse distance calculation for a sample memory trace. For the access of address w at time 8, the RD value is 3 as there are three unique memory references from its previous access at time 3.

Reuse profile is the histogram of reuse distances for all memory references of a memory trace. Table 2 shows reuse profile for the example memory trace shown in Table 1. In the histogram, D sits on the X-axis while Frequency or probability of D ($P(D)$) sits on the Y-axis. Reuse distance analysis can be used to measure locality [35,90] which in turn can be used to predict the cache performance of that application [14,20,72] and make cache management policy decisions [37]. Furthermore, reuse distance analysis has also been used for parallel application performance prediction for compile-time optimizations or design space explorations [6,10,54,88]. We estimate cache misses based on the 3C model: compulsory, capacity, and conflict misses. For a fully associative cache with capacity C, a memory reference’s reuse distance will always trigger a cache miss if $D \geq C$. In the example shown in Table 1, 50% of memory references with RD value of $\infty$ will cause a compulsory cache miss. If we consider that cache size is four, then none of the memory references will cause a capacity cache miss. If we consider that cache size is four, then none of the memory references will cause a capacity cache miss.

Reuse distance analysis is robust and architecture-independent for sequential applications. Once the memory trace of an application is collected and a reuse

---

1 D and RD are used interchangeably

### Table 1 Reuse Distance Example

| Access Time | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|-------------|---|---|---|---|---|---|---|---|
| Memory Address | w | x | w | y | x | z | z | w |
| Reuse Distance | $\infty$ | $\infty$ | 1 | $\infty$ | 2 | $\infty$ | 0 | 3 |

### Table 2 Reuse Profile Example

| Reuse Distance | 0 | 1 | 2 | 3 | $\infty$ |
|----------------|---|---|---|---|-----------|
| Frequency/Count | 1 | 1 | 1 | 1 | 4 |
| $P(D)$          | 1/8 | 1/8 | 1/8 | 1/8 | 4/8 |
profile generated, we can compute different cache configurations’ performance. It saves a significant amount of time in cache performance analysis and design as we do not have to collect memory traces for different cache configurations. Previous attempts [12, 34, 78] demonstrated the use of memory traces for reuse profile calculations. These approaches use binary instrumentation tools to collect memory traces. The memory traces used in most of these attempts are significant in size and time-consuming to process, thereby unscalable. However, recent attempts from Chennupati et al. [22–24] demonstrated analytical models that scale with a small input run of a program. These attempts help predict the performance of an application on single-threaded programs. Similarly, we model the private and shared cache performance of multicore programs using reuse distance for multicore. We discuss Reuse Distance Analysis on Multicores in the next Section 2.4.

2.4 Reuse Distance Analysis on Multicore Processors

Most multicores have multiple cache hierarchies with private and shared caches. A core accesses its private cache while all the cores access the shared cache. Although the locality of references of a parallel program running on a multicore is somewhat architecture-specific, it largely depends on the application’s memory access characteristics. Two separate reuse profiles, a Private-stack (PRD) and Concurrent reuse profiles (CRD) are used to model private and shared caches [47] respectively. On a shared cache, memory references from different cores interleave with one another. Thus, we can interleave memory references from different cores on a single LRU stack to measure concurrent reuse profiles. This interleaving causes different types of interaction: dilation, overlap, and interception [85].

Table 3 shows the memory references from two cores. Reference u at time 4 has a CRD of two, while its PRD is 1. Here, the CRD is larger than the PRD, which shows dilation. On the other hand, data sharing reduces dilation. Reference u at time 9 has a CRD of three, although there are four memory references between the two consecutive memory references to u at times 4 and 9. This shows overlapping as x is accessed by both cores inside the reuse interval of u. For v at time 10, the reused data itself is shared. Thus, its CRD is two, which is less than its PRD.

Several recent works have focused on CRD profiles for predicting the performance of shared cache [21, 33, 76, 79, 89]. Recently, researchers attempted to use analytical model and sampling to speed up the performance prediction [13, 47, 68, 70, 71]. All these models require trace collection from parallel executions of the application for different thread counts. On the other hand, our model collects a trace once from a sequential run of the application. From the sequential trace, we predict the shared cache performance for different thread counts. This makes our model scalable in terms of core count.
3 Methodologies

**PPT-Multicore** is a parameterized tool for performance prediction of a parallel OpenMP code. We leverage reuse distance analysis to determine the Private-stack (PRD) and Concurrent reuse profiles of the parallel sections of a program. These reuse profiles are then used to determine the hit rates of different cache levels and, ultimately, the parallel sections’ runtime. Figure 1 shows the different steps of our model that include a) translating the OpenMP code to a threaded code and adding labels for shared variables in the threaded program, b) generating a basic block labeled memory trace from a sequential run and mimicking shared, and private memory traces from it, c) estimating private and concurrent reuse profiles and hit rates, and d) calculating the effective latency, throughput, and finally predicting runtime. In this section, We describe each of these steps in detail.

3.1 Static Code Translation

In the first step of **PPT-Multicore**, we convert the OpenMP application to an intermediate threaded code using the OpenMP translator in ROSE [54] compiler framework. In the translation process, the original code’s parallel sections are transformed into intermediate functions to be executed parallelly. The shared variables accessed by the parallel sections are also grouped in the intermediate code.

```
int main()
{
  int i, n, sum;
  n = 500;
  sum = 0;
  #pragma omp parallel for reduction(+: sum)
  for(i = 0; i < n; i++)
    sum = sum + i;
}
```

**Fig. 2** A simple OpenMP summation program
struct shared_struct {
    void * n_p;
    void * sum_p;
};

int main(int argc, char **argv) {
    int status = 0;
    XOMP_init(argc, argv);
    int i, n, sum;
    n = 500;
    sum = 0;
    struct shared_struct shared_var;
    shared_var.sum_p = ((void *) (&sum));
    shared_var.n_p = ((void *) (&n));
    XOMP_parallel_start (OUT_1_7285_, &shared_var);
    XOMP_parallel_end();
    XOMP_terminate(status);
}

static void OUT_1_7285_(void *s_data) {
    shared_var_trace0: {} // Label for shared variables
    int *n = (int *) (((struct shared_struct *) s_data)->n_p);
    int *sum = (int *) (((struct shared_struct *) s_data)->sum_p);
    other_trace1: {} // Label for rest of the program
    _p_sum = 0;
    long index, lower, upper;
    XOMP_loop_default(0, *n - 1, 1, &lower, &upper);
    for (index = lower; index <= upper; index += 1)
        _p_sum = _p_sum + index;
    XOMP_atomic_start();
    *sum = *sum + _p_sum;
    XOMP_atomic_end();
    XOMP_barrier();
}

Fig. 3 Example of how the code in figure 2 is translated to intermediate threaded code
using Rose compiler. Note how the parallel section in figure 2 has been converted to function
OUT_7285_. A structure of pointers to the shared variables is passed to the function. Labels
are added for identifying shared variables.

Tracking the memory references for the shared variables is difficult in the high-
level OpenMP code. Therefore, the translation is an important step to correctly
track the shared and private variables in the parallel regions. Thus, the translated
code helps to calculate PRD and CRD profiles efficiently. Furthermore, the names
of these intermediate functions corresponding to the parallel sections start with
‘OUT_’, making it easier to generate memory traces only for the parallel sections
of the program. We only need to instrument those intermediate functions that are
hard to complete in the high-level OpenMP code.

Figure 2 and 3 show a simple OpenMP program and its translated interme-
diate threaded code respectively. The translated code contains XOMP wrapper
functions generated from the Rose compiler. These wrapper functions call the
GNU OpenMP (GOMP) library functions internally when compiled with GCC.
The function named OUT_1_7285 corresponds to the OpenMP code’s parallel
section in the translated code. The private variables of the OpenMP parallel sec-
tions are translated as local variables of OUT_1_7285. As each thread under execution runs its copy of these functions, memory allocation for local variables is also done individually.

The translated functions in the threaded version of the code receive pointers’ structure as parameters (s.data in the example code) for the shared variables. These pointers point to the shared variables accessed by the functions. All members of these structures are assigned to locally declared pointers (line 21-22 in figure 3). Using a script, we put the assignment statements of shared variables under a label (see line 20 where shared_var_trace label is added). In the memory trace, all the references under the shared_var_trace label are grouped in the corresponding basic block label so that later we can identify the memory references for shared variables. We further discuss our trace construction approach in section 3.2.

3.2 Memory Trace Generation for Different Cache Hierarchies

In the second step of our model, we generate LLVM basic block labeled memory trace only for the translated threaded program’s parallel functions. Each of the LLVM basic blocks has a single entry and a single exit point of execution. We can obtain the basic blocks’ labels in an LLVM intermediate representation file. We use a modified version [22] of LLVM based instrumentation tool, Byfl [62] which can instrument the preferred functions (in this case, functions starting with OUT_) to generate the basic block labeled memory trace through sequential execution. We add the basic block labels in the memory trace in a way that all the memory addresses that are accessed as a result of executing the corresponding straight-line code of (BB_i) are grouped together.

Figure 3 shows an example of how the private and shared memory traces are constructed from the labeled basic block trace. We inspect the shared basic blocks from the identification of the basic block’s label name. For instance, we gather all the memory references under the shared label (shared_var_trace was added from the previous step). We then mimic the parallel section of the program’s memory access behavior while running on multiple cores using the basic block labeled memory trace and thus generate the private memory traces of each thread under execution.

The parallel sections of the OpenMP code are executed concurrently on different cores. Thus, each core has its copy of the parallel sections of the code. We mimic this behavior by making copies of each basic block’s memory references under the parallel sections. Our mimicking strategy tries to replicate the memory trace of an OpenMP program on multiple cores. For example, suppose the parallel program is using 4 cores. In that case, we make four copies of a basic block, we then add an offset to the memory addresses for each of the cores under execution except the core executing master thread. The offset is added to all memory references of a parallel region’s basic blocks except for the shared variables’ memory references. Some basic blocks (e.g. loop iterations) under the parallel region are executed multiple times. So, they appear multiple times in the labeled memory trace. After adding offsets in the same way, we distribute the memory references belonging to these basic blocks evenly among all the cores. We choose the offset so that the mimicked memory references do not match the original memory references produced in the sequential execution. This mimicking strategy helps to show that the memory references belong to different cores.
The corresponding core accesses the private caches (such as $L_1$) to perform thread-specific execution. Therefore, we employ the procedure described in Algorithm 1 to generate private traces for each core. From the traces, we calculate corresponding reuse profiles and hit-rates for private caches. It takes a list of all the basic blocks, the number of cores, the sequential memory trace, the references belonging to shared variables, and basic block counts as input. The basic block counts denote the number of times each basic block is executed during program execution. If the count for a basic block is less than the number of cores, each thread gets a basic block copy. Otherwise, we distribute the count evenly among the core by setting the $bb\_count\_per\_core$ variable. In the next step, we traverse the memory trace and check whether it is a memory reference or not by checking the trace’s entries. Suppose it is a memory reference and there is only one instance of the basic block in the memory trace it belongs to ($bb\_count\_per\_core[bb\_id]$ value is one). In that case, we make a copy of that reference for each core, add offset to the memory reference and assign it to each core. If the corresponding basic block has multiple instances in the memory trace ($bb\_count\_per\_core[bb\_id]$ value is greater
Algorithm 1 Private Memory Trace Generation

1: procedure gen_private_traces(bb_list, num_cores, trace, shared_var_refs, bb_counts)
2:     private_traces ← [[ ] * num_cores]
3:     bb_count_per_core ← [[ ] * num_cores]
4:     bb_done_count ← [[ ] * num_cores]
5:     for bb_id in bb_list do
6:         if bb_count[bb_id] < num_cores then
7:             bb_count_per_core[bb_id] ← 1
8:             ▷ Each core gets a copy of BB
9:         else
10:             bb_count_per_core[bb_id] ← bb_counts[bb_id] / num_cores
11:             ▷ Split BB instances to different cores
12:         end if
13:     end for
14:     for entry in trace do
15:         if entry is mem_address then
16:             address = strtoull(entry)
17:             if bb_count_per_core[current_bb_id] = 1 then
18:                 for core = 0; core < num_cores; core++ do
19:                     if address /∈ shared_var_refs then
20:                         private_traces[core].append(address + offset * core)
21:                         ▷ Add offset if the address is not for shared variable
22:                     else
23:                         end if
24:                 end for
25:             else
26:                 core ← bb_done_count[bb_id] / bb_count_per_core[bb_id]
27:                 if address /∈ shared_var_refs then
28:                     private_traces[core].append(address + offset * core)
29:                     ▷ Add offset if the address is not for shared variable
30:                 else
31:                     end if
32:             else if BB_START in entry then
33:                 current_bb_id ← entry.split(:)[2]
34:             else if BB_END in entry then
35:                 bb_done_count[bb_id] = bb_done_count[bb_id] + 1
36:             end if
37:         end if
38:     end for
39: end procedure

than one), we assign it to a particular core. Note that if the reference belongs to
the shared variables, then we do not add the offset. It is possible to perform the
distribution with chunk size, similar to OpenMP static scheduling with chunk size.
We find the list of basic blocks and corresponding counts using our LLVM based
offline code analysis tool.

The OpenMP library can perform different scheduling strategies (e.g., static,
dynamic, guided) while executing the code’s parallel sections. Recording memory
traces for each scheduling strategy is cumbersome and inefficient in terms of both
time and memory. Thus, in this work, we generate a trace similar to the OpenMP
scheduled traces. We use the recorded basic block labeled sequential trace to mimic
the interleaving of threads. Our mimicking strategy distributes the corresponding
memory trace equally among multiple threads under execution, similar to following
static scheduling in OpenMP. To further study the effect of scheduling strategies on
Algorithm 2 Interleave memory traces

1: procedure interleave_traces(num_cores, private_mem_traces, strategy)
2: \text{trace\_traverse\_done} \leftarrow \mathbb{[} \mathbb{]} \times \text{num\_cores}
3: \text{interleaved\_trace} \leftarrow \mathbb{[} \mathbb{]}
4: for core in range(num\_cores) do
5: \text{trace\_traverse\_done}[\text{core}] \leftarrow \text{false}
6: end for
7: core, i \leftarrow 0
8: while i < \text{num\_cores} do
9: if strategy == \text{uniform} then
10: \text{core} \leftarrow \text{randint}(0, \text{num\_traces} - 1) \quad \triangleright \text{Randomly choose core number}
11: else if strategy == \text{round\_robin} then
12: if core == \text{num\_traces} then
13: core \leftarrow 0
14: else
15: \text{core} \leftarrow \text{core} + 1 \quad \triangleright \text{Increase core number in round robin fashion}
16: end if
17: end if
18: if getline(line, private\_mem\_traces[\text{core}]) \neq -1 then
19: \text{interleaved\_trace} \text{appends line}
20: end if
21: else if trace\_traverse\_done[\text{core}] == false then
22: \text{trace\_traverse\_done}[\text{core}] \leftarrow \text{true}
23: i \leftarrow i + 1
24: end if
25: end if
26: end while
27: end procedure

memory reuse, we propose various interleaving and scheduling strategies, described in section 3.2.1.

To generate the shared memory trace, we take the private traces and interleave the memory references. We use both round-robin and uniform random scheduling to interleave the memory references. Similar traces can be generated with binary instrumentation tools such as Valgrind [59], memTrace [64] and Pin [58, 66]. However, we use an LLVM based tool to leverage the conceptual advantage of dealing with simple straight line basic blocks within a program. Valgrind’s Lackey tool runs the multi-threaded program sequentially per thread, where the interleaving of the threads is left to the operating system. Therefore the resultant memory trace happens to be multi-threaded.

On the other hand, with Pin, one has to collect the memory trace for a specific core count. Nonetheless, we cannot derive a basic block labeled trace from Pin instead of our LLVM instrumentation. We can generate both private and shared memory traces from basic block labeled sequential memory trace with our approach. Later we estimate the reuse profile for each trace once we have the memory traces that mimics the multicore execution.

3.2.1 Interleaving Strategies

To determine the OpenMP application’s shared cache performance, we employ multiple interleaving strategies to mimic the trace of shared memories. The shared trace is constructed as if all the threads in the application are executing concurrently and share the shared memory space (typically Last Level Cache). Algorithm
show a high-level implementation of our interleaving strategies. It takes private traces, interleaving strategy, and the number of cores as inputs and applies our interleaving strategies to generate shared traces for shared memory accesses. We assume that the master thread is being executed in core 0. We initiate an array `trace_traverse_done` with boolean value false. The size of the array is the same as the number of cores under consideration. This is to track if all the memory references of the corresponding private trace have been traversed or not. Here, we employ two interleaving strategies: round-robin and uniform-random (see lines 9
[17]). In case of uniform random interleaving, we randomly choose any of the private traces and check if all the references from the trace have been read. If not, then we pick a reference from the trace and append it to the interleaved trace. For round-robin interleaving, we take the first memory reference from core 0’s trace. Then we choose the next reference from the next core’s trace. We repeat the process until all memory references from all traces are read and appended to interleaved trace. As our model is flexible, it is possible to implement other interleaving strategies in our model.

3.3 Cache Model

We take the mimicked memory traces and cache configuration parameters as input and estimate the cache hit rates in this step. We use a reuse profile-based cache model to predict the cache hit rates. We further discuss the steps of our cache model as follows.

3.3.1 Reuse Profile Calculation

We build the Private-stack and the Concurrent reuse profiles of the program (P(D)) from our mimicked private and shared memory traces. The conventional methods of measuring the reuse profile are costly because of the enormous size of the memory traces. The previous work of PPT used a stack-based method to compute the reuse profiles of a program [5, 6, 22]. The stack-based method has a worst-case time complexity of \( O(N.M) \) for a trace of length \( N \) containing \( M \) distinct references. In this work, we use a more optimized tree-based approach [60] for calculating the reuse profiles from the memory trace, which has on average a time complexity of \( O(N.\log M) \).

3.3.2 Hit Rate Estimation

We measure private, and shared cache hit rates using an analytical memory model (SDCM) proposed by Brehob and Enbody [17]. SDCM was used before to predict the cache hit rates of CPUs [11, 22–24] and GPUs [5, 6] in PPT. Equation 1 shows the way to measure the conditional hit rate at a given reuse distance (\( P(h \mid D) \)).

\[
P(h \mid D) = \sum_{a=0}^{A-1} \binom{D}{a} \left( \frac{A}{B} \right)^a \left( \frac{B-A}{B} \right)^{(D-a)}
\]

where \( D \) denotes the reuse distance, \( A \) denotes cache associativity and \( B \) denotes cache size in terms of number of blocks (which is cache size over cache line size). Typically, Eq. 1 is used for an \( n \)-way associative cache. For a direct-mapped cache, conditional probability of hit is defined as
Finally, we calculate the approximated unconditional probability of a hit \( P(h) \) for the entire program using Eq. 3:

\[
P(h) = \sum_{i=0}^{N} P(D_i) \times P(h | D_i)
\]  

where, \( P(D_i) \) is the probability of \( i^{th} \) reuse distance \( (D) \) in a reuse distribution \( Pr(D) \). We further use these hit rates in the runtime prediction of the applications, which is beyond this paper’s scope.

### 3.4 Runtime Prediction

In our final step, we predict the runtime of the parallel application. In most cases, the benchmark kernels are within OpenMP parallel sections. When measuring parallel applications’ performance, usually, we are interested in the parallel kernels and do not care about the sequential initialization and cleanup phases of the benchmarks. We take the ideas used by Chennupati et al. in [22] to predict the runtimes of parallel sections of the benchmark applications. Chennupati et al. predicted the runtimes of a sequential application where we predict the parallel application’s runtimes.

Two main factors contribute to the runtime of a parallel application. Those are average time taken for the CPU operations \( (T_{CPU}) \) and average memory access time \( (T_{mem}) \). We use Byfl [62], an LLVM based application characterizing tool to get the number of CPU operations and the total memory required for the kernel execution. The parallel kernels’ reuse profile is used along with the total memory required to determine memory latency.

Therefore, the predicted runtime is measured using Eq. 4:

\[
T_{pred} = T_{mem} + T_{CPU}
\]

### 3.4.1 Runtime Prediction considering Contiguous Memory Access

If we assume that the available memory is contiguous, then the average memory access time is measured using equation 5:

\[
T_{cont-mem} = \frac{\delta_{avg} + (b - 1) \times \beta_{avg}}{b} \times total_{mem}
\]

where \( \delta_{avg} \), \( \beta_{avg} \), \( b \) and \( total_{mem} \) denote average latency, average reciprocal throughput, block size and the total memory (bytes) required by the program respectively. In the equation, we consider the average latency \( \delta_{avg} \) and throughput \( \beta_{avg} \) as per memory access, while we consider the block size \( b \) as word size assuming the available memory is contiguous. By dividing \( \delta_{avg} + (b - 1) \times \beta_{avg} \) by block size \( b \) we find average memory access time per byte. Multiplying this result with \( total_{mem} \) provides total memory access time of a program in contiguous memory setting.
The average latency and throughput of a program depend on the hit rates at different cache levels. The average latency of a program on a machine with a three-level cache can be calculated using equation\(6\):

\[
\delta_{avg} = P_{L_1}(h) \times \delta_{L_1} + (1 - P_{L_1}(h)) \left[ P_{L_2}(h) \times \delta_{L_2} + (1 - P_{L_2}(h)) \right] \times \left[ P_{L_3}(h) \times \delta_{L_3} + (1 - P_{L_3}(h)) \times \delta_{RAM} \right]
\]

where, \(\delta_{L_1}, \delta_{L_2}, \delta_{L_3}\), and \(\delta_{RAM}\) are latencies of L1, L2, L3 caches and RAM respectively; \(P_{L_1}(h), P_{L_2}(h)\) and \(P_{L_3}(h)\) are the probabilities of a hit for L1, L2 and L3 caches respectively.

Similarly, we measure the average throughput, \(\beta_{avg}\) using equation\(7\):

\[
\beta_{avg} = P_{L_1}(h) \times \beta_{L_1} + (1 - P_{L_1}(h)) \left[ P_{L_2}(h) \times \beta_{L_2} + (1 - P_{L_2}(h)) \right] \times \left[ P_{L_3}(h) \times \beta_{L_3} + (1 - P_{L_3}(h)) \times \beta_{RAM} \right]
\]

Using Byfl, we identify the number of CPU operations (ADD, SUB, DIV, etc.) in the parallel section. We divide those numbers by the number of cores and then measure \(T_{CPU}\), the time required for CPU operations for one core, using the hardware-specific instruction latencies and the operations count. We assume that the total workload is distributed among multiple cores evenly. Finally, the total runtime is predicted as \(T_{pred}\).

### 3.4.2 Runtime Prediction considering Non-contiguous Memory Access

In reality, the memory alignment is non-contiguous. Therefore, there will be gaps \((\upsilon)\) in between the required program data. As a result, the new block size \(b_{new} = b + \upsilon\) is used in equation\(5\) for determining non-contiguous memory access time. If the block size is large, the entire block may not be transferred from main memory to caches due to limiting factors such as cache size, data bus width, etc. Therefore, we model such memory access behavior as follows. Considering \(b_{new}^1, b_{new}^2, b_{new}^3, ..., b_{new}^i, ..., b_{new}^n\) are the blocks of data on main memory and \(C\) be the amount of data transferred to cache from main memory at any given time, the new block size \(b_{new}\) at a given cache size \((B)\) can be re-written as:

\[
b_{new} = \begin{cases} 
C & \text{if } b_{new}^i \leq C \\
\left( b_{new}^i \right) \times C & \text{if } S \geq b_{new}^i \geq C \\
S & \text{if } b_{new}^i \geq S
\end{cases}
\]

In case of the time taken for CPU operations, there is a large difference in the instruction latencies between DIV and the rest of the instructions. Moreover, the time required for CPU operations is dependent on program characteristics, where some applications are instruction latency dependent while others are throughput
Table 4 Benchmark applications used to verify our model. † and ♦ denote applications from PolyBench/OpenMP [65] and PARSEC [15] benchmark suites respectively. Last column shows the abbreviation of benchmark names which are used later to represent results.

| Application      | Description                                      | Domain                  | Input Size | Trace Size | Abbr. |
|------------------|--------------------------------------------------|-------------------------|------------|------------|-------|
| ADI†             | Alternating Direction Implicit method for 2D heat diffusion | Stencils                | 1k x 50    | 170GB      | adi   |
| ATAX†            | Matrix transpose and vector multiplication        | Linear Algebra          | 4k x 4k    | 14GB       | atx   |
| BICG†            | BICG sub kernel of BICGSTab linear solver        | Linear Algebra          | 4k x 4k    | 11GB       | bcg   |
| Blackcholes♦      | Black-Scholes partial differential equation       | Recognition, Mining and Synthesis | Options=64k, Runs=100 | 25GB    | blk   |
| Convolution-2D†   | 2D Convolution                                   | Stencils                | 4k x 4k    | 19GB       | c2d   |
| Covariance†       | Covariance computation                           | Datamining              | 1k x 1k    | 208GB      | cov   |
| Doitgen†          | Multiresolution analysis kernel                   | Linear Algebra          | 128x128x128 | 146GB     | dgn   |
| Durbin†           | Toeplitz system solver                            | Linear Algebra          | 4k         | 7.7GB      | dbn   |
| Gramschmidt†      | QR decomposition with modified Gram Schmidt      | Linear Algebra          | 512 x 512  | 64GB       | grm   |
| Jacobi†           | Jacobi iteration                                 | Stencils                | 4k x 4k    | 41GB       | jcb   |
| LU†              | LU decomposition without pivoting                | Linear Algebra          | 1k         | 179GB      | lu    |
| 2MM†             | Two matrix multiplication                         | Linear Algebra          | 512 x 512  | 115GB      | 2mm   |
| MVT†             | Matrix vector product and transpose               | Linear Algebra          | 4k         | 14GB       | mvt   |
| SYMM†            | Symmetric matrix-multiply                         | Linear Algebra          | 1024 x 1024 | 335GB     | smm   |

reliable. Thus, the time for the resultant CPU operations ($T_{CPU}$) can be written as:

$$T_{CPU} = \begin{cases} 
\delta_{in} + (N_{in} - N_{in,div} - 1) \times \beta_{in} + \\
\delta_{div} + (N_{in,div} - 1) \times \beta_{div} & : \text{throughput} \\
(N_{in} - N_{in,div} - 1) \times \delta_{in} + \\
(N_{in,div} - 1) \times \delta_{div} & : \text{latency}
\end{cases}$$

where $\delta_{in}, \delta_{div}, \beta_{in}, \beta_{div}$ are latencies and throughputs of instructions, ADD/SUB, MUL and DIV respectively, while $N_{in}$ and $N_{in,div}$ are the number of instructions.
4 Experiments and Results

In this section, we validate our model and present the results. Table 4 shows a list of the applications used for validation. We use various applications representing different domains from PolyBench [65] and PARSEC [15] benchmark suites. For PolyBench, we use the OpenMP implementation by Grauer-Gray et al. [40]. We choose these benchmark suites as they are widely used for validating performance models. We use the standard input sizes for all the benchmarks. The generated basic block labeled memory trace sizes are also shown for the input used for each application.

Our model validations are two-fold: 1) hit-rates and 2) runtimes. For the validations, we model three processor architectures listed in table 5. We disable both hardware prefetching and hyperthreading for these machines' architectures as we do not model those features in this work. We bind a single thread to run on a single core. For the experiments, we start the core count with 1 and increase it with a power of 2; therefore, we report hit rates and execution times for \{1, 2, 4, 8\} cores for all the benchmarks. For Xeon and EPYC processors, we also show the results for the 16 core configuration. We present the validation results of hit-rates in section 4.1 and runtimes in section 4.2.

4.1 Cache Hit Rate Verification

We validate the predicted hit-rates from our cache model against the PAPI [81] performance counters. Table 6 shows the PAPI events (equations) used to determine the cache hit rates on real hardware. We report hit-rates for varying numbers of cores \{1, 2, 4, 8\} for all the benchmarks across all the experimental architectures. While collecting the PAPI performance counters to calculate hit rates, we change the number of threads/cores using `OMP_NUM_THREADS` environment variable.

Most of the benchmark applications that we use have serial codes to initialize the data structures that are later accessed in parallel. Thus, the data that we access in parallel sections might already be in the cache due to their previous access to

Table 5 Target CPUs

| Processor           | Microarchitecture | Core Count | Freq.   | L1      | L2      | L3      |
|---------------------|-------------------|------------|---------|---------|---------|---------|
| Intel Core i7-5960X | Haswell           | 8          | 3.0 GHz | 32 KB   | 256 KB  | 20 MB   |
| Intel Xeon E5-2699 v4 | Broadwell       | 22         | 2.2 GHz | 32 KB   | 256 KB  | 55 MB   |
| AMD EPYC 7702P      | Zen 2             | 64         | 2.0 GHz | 2 MB    | 32 MB   | 256 MB  |

Table 6 PAPI events to measure cache hit rates on real machine

| Event               | PAPI events and equation used                                                                 |
|---------------------|-----------------------------------------------------------------------------------------------|
| L1 D-Cache Hit Rate | 1.0 - \((\text{PAPI}L1D\text{CM} / (\text{PAPI}LD\text{INS} + \text{PAPI}SR\text{INS}))\)   |
| L2 Cache Hit Rate   | 1.0 - \((\text{PAPI}L2D\text{CM} / (\text{PAPI}LD\text{INS} + \text{PAPI}SR\text{INS}))\)   |
| L3 Cache Hit Rate   | 1.0 - \((\text{PAPI}L3T\text{CM} / (\text{PAPI}LD\text{INS} + \text{PAPI}SR\text{INS}))\)   |
Fig. 5 Hit rate comparison on Intel Core i7-5960X caches for different core configurations. Note that we start the Y-axis at 0.7 on order to zoom in on the difference in performance.
Fig. 6 Hit rate comparison on Intel Xeon E5-2699 caches for different core configurations. Note that we start the Y-axis at 0.7 on order to zoom in on the difference in performance.
the applications’ initialization. This makes the cache warm cache (requested data is already in the cache). However, in our cache model, we assume the caches are cold (cache is empty when the first data is requested). To get around this issue, we add a large dummy array access to the code before starting the PAPI counters but after the program’s initialization. This way, we evict all the data loaded into the cache due to the initialization section’s execution. As a result, when the parallel kernels are executed, the cache acts as a cold cache.

Figure 5 compares the hit rates on Intel Core i7-5960X for each of the core configurations {1, 2, 4, and 8 cores}. We show the hit rates of the benchmarks for Intel Core i7-5960X in Figures 5(a)–5(d) respectively. For L1 cache our model’s average error rates are 0.99%, 0.84%, 0.92%, and 1.01% for the core configurations where 1.98%, 1.87%, 2.13%, and 2.03% are average error rates for L2 and 0.09%, 0.13%, and 0.15% are the average error rates for L3. The results for Xeon E5-2699 processor are shown in figure 6 for 1, 2, 4, 8 and, 16 core configurations. For Xeon’s L1 cache, our model’s average error rates are 1.43%, 1.31%, 1.41%, 1.56%, and 1.88% for the respective core configurations where 2.64%, 2.30%, 2.83%, 2.76% and 2.73% are average error rates for L2 and 0.05%, 0.07%, 0.09% and 0.20% are the average error rates for L3. The results show that our model predicts the hit rates of caches accurately with an overall average error rate of 1.23%.

The PAPI events listed in table 6 are not available on the AMD EPYC 7702P processor. Therefore, we can not verify the predicted cache hit rates for this CPU with real hardware.

As we mimic the memory traces of multi-threaded execution on different cache levels from single-threaded execution, we do not consider the effect of cache coherence in our model. Still, the experiments show promising results. Overall, our error rates for cache hit rate prediction are reasonable. However, we notice a slightly higher error rate for Gramschmidt and SYMM when predicting L2 cache hit rates on both processors irrespective of core count. On Core i7-5960X, the average error for Gramschmidt’s L2 hit rate prediction is 8.55%, where on Xeon E5-2699, it is 11.09%. For SYMM the error average rates are 6.94% and 9.04%.

4.2 Runtime Verification

We model the processors listed in table 5 inside PPT to predict runtimes of the benchmark applications. The previous implementation of PPT had parameterized models for single-core CPUs [23] and GPUs [4]. We added support for multicore modeling in PPT. PPT-Multicore takes the number of cores, clock frequency, cache sizes, line sizes, associativity, cache latencies, reciprocal throughput of different types of instructions (e.g., integer arithmetic, floating-point arithmetic), data bus

```python
1 tasklist = [{'iALU', n_iALU/num_cores}, ['fALU', n_fALU/num_cores], ['fDIV', n_fDIV/num_cores], ['MEM_ACCESS', reuse_dist_shared, probability_rd_shared, block_size, mem_in_bytes, data_bus_width, num_cores, reuse_dist_private_list, probability_rd_private_list]]
2 time = core.time_compute_multicore(tasklist)
```

Fig. 7 An example of tasklist passed to PPT
width, RAM bandwidth, and RAM latency as hardware parameter inputs. We take the hardware parameter values from the processor manufacturer’s website, Agner Fog’s instruction latency manual [39], and 7-CPU website [1].

Our model’s software parameters include the number of different types of integer arithmetic operations, floating-point arithmetic operations, block size, and total memory operations in bytes for the parallel section of the benchmarks. We use Byfl [62] to gather these data from the sequential run of benchmarks. To measure $T_{\text{pred}}$, we pass these data along with private and shared reuse profiles to PPT using a tasklist. An example tasklist looks like figure 7. In the tasklist, we divide the number of different ALU operations by the number of cores/threads to measure $T_{\text{CPU}}$ per core. We use the system clock to get runtimes of parallel sections on the real machine.

Figure 8 shows the runtime comparison between our model and the Intel Core I7-5960X processor. Runtimes are shown in seconds. The average error rates are 10.78%, 8.06%, 8.82%, and 13.63% for 1, 2, 4, and 8 core configurations respectively. On Xeon E5-2699 the error rates are 9.93%, 7.08%, 7.53%, 12.41%, and 16.72% as shown in figure 9. We compare the predicted runtimes for AMD EPYC 7702P in figure 10. The average error rates are 6.81%, 6.32%, 6.82%, 7.34%, and 10.86% for 1, 2, 4, 8, and 16 core configurations respectively. Overall we have an average error rate of $9.08\%$ for runtime prediction. As we do not model some modern CPU features like pipelining, speculative execution, branch prediction in the current PPT version, we notice higher error rates in runtime prediction. We also notice that some applications’ runtime does not scale with core count. In those cases, our model provides a high error rate. As an example, Jacobi has high
error for 8 core configuration (36.43%) as its runtime does not scale much from 4 (runtime 0.128s) to 8 (runtime 0.092s) core count on a Core i7 processor. On Xeon and EPYC, we also notice a similar result with Jacobi. Its runtimes are 0.111 seconds and 0.119 seconds for 8 and 16 core configurations on Xeon. On EPYC the runtime of Jacobi increases from 0.175s (8 core) to 0.194s (16 core) with increase of core count. As a result, we notice 55.60% and 58.62% error rates in Jacobi’s runtime prediction on Xeon and EPYC, respectively, for 16 core configurations. This behavior is expected as we divide the number of different CPU operations by core count when we pass the tasklist to PPT as shown in figure 7, which is later used for computing $T_{CPU}$ per core.

Fig. 9 OpenMP applications’ parallel sections’ runtime comparison on Intel Xeon E5-2699 with different core configurations
Fig. 10 OpenMP applications’ parallel sections’ runtime comparison on AMD EPYC 7702P with different core configurations.

5 Related Works

Recent works in performance modeling can be categorized into two approaches, analytical and simulation based. Analytical models like deduce mathematical equations to predict the performance. Analytical regression models has also been proposed by researchers for multicore performance modeling. Several groups also explored and benchmarked machine learning performance modeling. Although these models are fast, they are often less accurate than simulators. Although simulators are slower than analytical model, simulators such as Simics, SimpleScalar, SimCore, HASE, Barra, MSim, RSim, SimFlex, and Sniper have been proposed by the researchers for performance prediction and estimation at various levels of detail.
Simulators such as gem5 [16], MARSS [63], and the Structural Simulation Toolkit [67] aim to produce cycle-accurate predictions, which is time-consuming but important for concentrated design space explorations.

Alternatively, recent attempts in program analysis include COMPASS [53], Durango [19], CODES [27] which rely on Aspen [77]. Aspen performance modeling takes source code as input and generates the programs’ control flow graph while combining it with analytic modeling aspects.

On the other hand, reuse distance [57] analysis is a commonly used method for cache performance prediction [9,10,14,20,55,72], cache policy management [30,37,49], and program locality prediction [12,35,47,90]. Researchers have also used further parallelized graph algorithms to efficiently implement reuse distance analysis [60] and proposed analytical modeling and sampling techniques [22–24,75].

Recently, several research works on multicore and GPU reuse profile analysis has been also published [5,6,13,47,68,70,71,85].

Jiang et al. [47] introduced CRD profiles for multicores and provided a probabilistic model to estimate the CRD of each thread. They do not consider invalidation for data locality analysis of private caches.

Wu and Yeung [85] explored PRD and CRD profiles for performance prediction of loop-based parallel programs. They provided a detailed analysis of the effect of core count on PDR and CRD profiles. They also developed a model for predicting PRD and CRD profiles with core count scaling. The predict the CRD profile with about 90% accuracy. In other work [86], they studied the impact of core count and problem size scaling on the program locality’s predictability.

Sabarimuthu et al. [68] proposed a probabilistic method to calculate the CRD profile of threads sharing a cache and derived coherent reuse profile of each thread considering the effect of cache coherence. They derived the concurrent reuse distance (CRD) profile of each thread, sharing the cache with other threads from the respective thread’s private reuse profile.

In prior work to this paper, we et al. [11] proposed a probabilistic method to predict PRD and CRD profiles from single-threaded execution trace and introduced PPT-SASMM. Although PPT-SASMM can measure reuse profiles accurately, the implementation was slow. This paper takes the ideas of PPT-SASMM and re-implement it for performance improvement. Compared to PPT-SASMM, our private and shared cache trace generation is much faster. We also employ a tree-based algorithm to measure reuse profiles which makes our approach much faster [60].

Schuff et al. [71] explored reuse distance analysis for shared cache accounting inter-core cache sharing. They also studied PRD profiles considering invalidation-based cache-coherence. They further extended their work to accelerate CRD profile measurement by introducing sampling and parallelization [70].

Ding et al. [32] explored theories and techniques to measure program interaction on multicores and introduced a new footprint theory. They proposed a trace-based model that computes a set of per-thread metrics. They compute these metrics using a single pass over a concurrent execution of a parallel program. Using these metrics, they propose a scalable per-thread data-sharing model. They also propose an irregular thread interleaving model integrated with the data-sharing model.
Kaxiras et al. \cite{48} proposed statistical techniques from epidemiological screening and polygraph testing for coherence communication prediction in shared-memory multiprocessors.

Almost all of these approaches collect traces at different cache levels from parallel execution of the application. Our approach is different since we collect a trace only once from a sequential execution of the application. This makes our approach more scalable with core count.

6 Conclusion and Future Direction

We introduced PPT-Multicore which improves our previous approach for cache hit rate prediction of OpenMP program on multicores and adds runtime prediction of the parallel sections. Given an OpenMP parallelizable program and the modeled multicore parameters, PPT-Multicore can accurately predict the runtime of parallel sections. This prediction involves several intermediate results, including private and concurrent reuse profile prediction, latency and throughput of memory accesses, and finally, the runtimes. We validated our model using different benchmark applications from different domains with standard input sets on Intel Core i7-5960X, Intel Zeon E5-2699 v4, and AMD EPYC 7702P processors. The results show that our model can predict the hit rates at different cache levels accurately. Our runtime prediction is also promising, with an overall average error rate of 10.53%. We plan to model pipelining, speculative execution, prefetching, and other modern computer architecture features of multicores in the future.

Acknowledgements The authors would like to thank Dr. David Newsom for donating several machines to the PEARL laboratory at NMSU. Some of the experiments in this paper were run on the donated machines. This work is partially supported by Triad National Security, LLC subcontract #581326. This paper has been approved for unlimited public distribution under LA-UR-21-22749. Any opinions, findings, and/or conclusions expressed in this paper do not necessarily represent the views of the DOE or the U.S. Government.

References

1. 7-CPU: 7-Zip LZMA Benchmark. [https://www.7-cpu.com](https://www.7-cpu.com) (2021). [Online; accessed 4-Dec-2020]
2. Aarno, D., Engblom, J.: Software and System Development Using Virtual Platforms: Full-System Simulation with Wind River Simics. Morgan Kaufmann (2014)
3. Alexandrov, A., Ionescu, M.P., Schause, K.E., Scheiman, C.: LogGP: Incorporating Long Messages into the LogP Model for Parallel Computation. Journal of Parallel and Distributed Computing 44(1), 71–79 (1997)
4. Arafa, Y., Badawy, A.A., Chennupati, G., Santhi, N., Eidenbenz, S.: Ppt-gpu: Scalable gpu performance modeling. IEEE Computer Architecture Letters 18(1), 55–58 (2019)
5. Arafa, Y., Badawy, A.H., Chennupati, G., Barai, A., Santhi, N., Eidenbenz, S.: Fast, Accurate, and Scalable Memory Modeling of GPGPUs Using Reuse Profiles. In: Proceedings of the 34th ACM International Conference on Supercomputing, ICS ‘20. Association for Computing Machinery, New York, NY, USA (2020)
6. Arafa, Y., Chennupati, G., Barai, A.H.A., Santhi, N., Eidenbenz, S.: GPUs Cache Performance Estimation using Reuse Distance Analysis. In: 2019 IEEE 38th International Performance Computing and Communications Conference (IPCCC), pp. 1–8. IEEE, Piscataway, NJ, USA (2019)
7. Austin, T., Larson, E., Ernst, D.: SimpleScalar: An Infrastructure for Computer System Modeling. Computer 35(2), 59–67 (2002)
8. Badamo, M., Casarona, J., Zhao, M., Yeung, D.: Identifying Power-Efficient Multicore Cache Hierarchies via Reuse Distance Analysis. ACM Trans. Comput. Syst. 34(1) (2016)
9. Badawy, A.A., Yeung, D.: Guiding Locality Optimizations for Graph Computations via 
Reuse Distance Analysis. IEEE Computer Architecture Letters 16(2), 119–122 (2017)
10. Badawy, A.A., Yeung, D.: Optimizing locality in graph computations using reuse distance 
profiles. In: 2017 IEEE 36th International Performance Computing and Communications 
Conference (IPCCC), pp. 1–8 (2017)
11. Barai, A., Chennupati, G., Santhi, N., Badawy, A.H., Arafa, Y., Eidenbenz, S.: PPT-
SASMM: Scalable Analytical Shared Memory Model: Predicting the Performance of Mul-
ticore Caches from a Single-Threaded Execution Trace. In: The International Symposium on 
Memory Systems, MEMSYS 2020, p. 341–351. Association for Computing Machinery, 
New York, NY, USA (2020)
12. Berg, E., Hagersten, E.: StatCache: a probabilistic approach to efficient and accurate data 
locality analysis. In: IEEE International Symposium on - ISPASS Performance Analysis 
of Systems and Software, 2004, pp. 20–27. IEEE, IEEE, Piscataway, NJ, USA (2004)
13. Berg, E., Zeffer, H., Hagersten, E.: A Statistical Multithreaded Cache Model. In: 2006 
IEEE International Symposium on Performance Analysis of Systems and Software, pp. 
89–99. IEEE, Piscataway, NJ, USA (2006)
14. Beyls, K., D’Hollander, E.H.: Reuse Distance as a Metric for Cache Behavior. In: In Pro-
ceedings of the IASTED Conference on Parallel and Distributed Computing and Systems, 
pp. 617–662. IEEE, Piscataway, NJ, USA (2001)
15. Bienia, C.: Benchmarking Modern Multiprocessors. Ph.D. thesis, Princeton University 
(2011)
16. Binkert, N., Beckmann, B., Black, G., Reinhardt, S.K., Saidi, A., Basu, A., Hestness, J., 
Hower, D.R., Krishna, T., Sardashi, S., et al.: The gem5 Simulator. ACM SIGARCH 
computer architecture news 39(2), 1–7 (2011)
17. Brebesh, M., Embudy, R.: An analytical model of locality and caching. Tech. Rep. MSU-
CSE-99-31 (1999)
18. Carlson, T.E., Heirman, W., Eyerman, S., Hur, I., Ecekhouit, L.: An Evaluation of High-
Level Mechanistic Core Models. ACM Transactions on Architecture and Code Optimiza-
tion (TACO) (2014)
19. Carothers, C.D., Meredith, J.S., Blanco, M.P., Vetter, J.S., Mubarak, M., LaPre, J., Moore, 
S.: Durango: Scalable Synthetic Workload Generation for Extreme-Scale Application Per-
formance Modeling and Simulation. In: Proceedings of the 2017 ACM SIGSIM Conference 
on Principles of Advanced Discrete Simulation, SIGSIM-PADS ’17, p. 97–108. Association 
for Computing Machinery, New York, NY, USA (2017)
20. Cascaval, C., Padua, D.A.: Estimating Cache Misses and Locality Using Stack Distances. 
In: Proceedings of the 17th Annual International Conference on Supercomputing, ICS ’03, 
pp. 150–159. ACM, New York, NY, USA (2003)
21. Ceballos, G., Hagersten, E., Black-Schaffer, D.: Formalizing Data Locality in Task Parallel 
Applications. In: Algorithms and Architectures for Parallel Processing, pp. 43–61. Springer 
International Publishing, Cham (2016)
22. Chennupati, G., Santhi, N., Bird, R., Thulasidasan, S., Badawy, A.H.A., Misra, S., Ei-
denbenz, S.: A Scalable Analytical Memory Model for CPU Performance Prediction. In: S. 
Jarvis, S. Wright, S. Hammond (eds.) High Performance Computing Systems. Per-
formance Modeling, Benchmarking, and Simulation, pp. 114–135. Springer International 
Publishing, Cham (2018)
23. Chennupati, G., Santhi, N., Eidenbenz, S.: Scalable Performance Prediction of Codes with 
Memory Hierarchy and Pipelines. In: Proceedings of the 2019 ACM SIGSIM Conference 
on Principles of Advanced Discrete Simulation, SIGSIM-PADS ’19, p. 13–24. Association 
for Computing Machinery, New York, NY, USA (2019)
24. Chennupati, G., Santhi, N., Eidenbenz, S., Thulasidasan, S.: An Analytical Memory Hier-
archy Model for Performance Prediction. In: Proceedings of the 2017 Winter Simulation 
Conference, WSC ’17. IEEE Press, Piscataway, NJ, USA (2017)
25. Chennupati, G., Santhi, N., Eidenbenz, S., Zerr, R.J., Rosa, M., Zamora, R.J., Park, E.J., 
Nadiga, B.T., Liu, J., Ahmed, K., Obaida, M.A.: Performance Prediction Toolkit (PPT). 
Los Alamos National Laboratory (LANL) (2017c). https://github.com/lanl/PPT
26. Collange, S., Daumas, M., Defour, D., Parelo, D.: Barra: A Parallel Functional Simu-
lator for GPGPU. In: 2010 IEEE International Symposium on Modeling, Analysis and 
Simulation of Computer and Telecommunication Systems, pp. 351–360. IEEE (2010)
27. Cope, J., Liu, N., Lang, S., Carns, P., Carothers, C., Ross, R.: CODES: Enabling Co-
design of Multilayer Exascale Storage Architectures. In: In Proceedings of the Workshop on 
Emerging Supercomputing Technologies (2011)
28. Culler, D., Karp, R., Patterson, D., Sahay, A., Schauer, K.E., Santos, E., Subramonian, R., von Eicken, T.: LogP: Towards a Realistic Model of Parallel Computation. SIGPLAN Not. 28(7), 1–12 (1993)
29. Dagum, L., Menon, R.: OpenMP: An Industry-Standard API for Shared-Memory Programming. IEEE Comput. Sci. Eng. 5(1), 46–55 (1998)
30. Das, S., Aamodt, T.M., Daily, W.J.: Reuse Distance-Based Probabilistic Cache Replacement. ACM Trans. Archit. Code Optim. 12(4) (2015)
31. Davis, J.D., Landau, J., Ohlhot, R.: Maximizing CMP Throughput with Mediocre Cores. In: Proceedings of the 14th International Conference on Parallel Architectures and Compilation Techniques, PACT ’05, p. 51–62. IEEE Computer Society, USA (2005)
32. Ding, C., Chilimbi, T.: A Composable Model for Analyzing Locality of Multi-threaded Programs. Tech. Rep. MSR-TR-2009-107, Microsoft (2009)
33. Ding, C., Xiang, X., Bao, B., Luo, H., Luo, Y.W., Wang, X.L.: Performance Metrics and Models for Shared Cache. Journal of Computer Science and Technology 29(4), 692–712 (2014)
34. Ding, C., Zhong, Y.: Reuse Distance Analysis. Tech. rep., University of Rochester, Rochester, NY, USA (2001)
35. Ding, C., Zhong, Y.: Predicting Whole-program Locality Through Reuse Distance Analysis. SIGPLAN Not. 38(5), 245–257 (2003)
36. Dubach, C., Jones, T., O’Boyle, M.: Microarchitectural Design Space Exploration Using an Architecture-Centric Approach. In: 40th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO 2007), pp. 262–271 (2007)
37. Duong, N., Zhao, D., Kim, T., Cammarota, R., Valero, M., Veidenbaum, A.V.: Improving Cache Management Policies Using Dynamic Reuse Distances. In: Proceedings of IEEE/ACM International Symposium on Microarchitecture, MICRO-45, pp. 389–400. IEEE, Piscataway, NJ, USA (2012)
38. Eeckhout, L.: Computer Architecture Performance Evaluation Methods. Synthesis Lectures on Computer Architecture 5(1), 1–145 (2010)
39. Fog, A.: Instruction tables: Lists of instruction latencies, throughputs and micro-operation breakdowns for Intel, AMD and VIA CPUs (2016)
40. Grauer-Gray, S., Xu, L., Searles, R., Ayalamayajula, S., Cavazos, J.: Auto-tuning a High-Level Language Targeted to GPU Codes. In: 2012 Innovative Parallel Computing Conf. pp. 1–10. IEEE, Piscataway, NJ, USA (2012)
41. Haradavellas, N., Somogyi, S., Wenisch, T.F., Wunderlich, R.E., Chen, S., Kim, J., Falsafi, B., Hoe, J.C., Nowatzyk, A.G.: SimFlex: A Fast, Accurate, Flexible Full-System Simulation Framework for Performance Evaluation of Server Architecture. SIGMETRICS Perform. Eval. Rev. 31(4), 31–34 (2004)
42. Heywood, R.I.P., Howell, F.: HASE: A Flexible Toolset for Computer Architects. Computer J 38(10), 775–764 (1995)
43. Hill, M.D., Marty, M.R.: Amdahl’s Law in the Multicore Era. IEEE Computer 41, 33–38 (2008)
44. Hughes, C.J., Pai, V.S., Ranganathan, P., Adve, S.V.: Rsim: Simulating Shared-Memory Multiprocessors with ILP Processors. Computer 35(2), 40–49 (2002)
45. Huh, J., Burger, D., Keckler, S.W.: Exploring the Design Space of Future CMPs. In: Proceedings of the 2001 International Conference on Parallel Architectures and Compilation Techniques, PACT ’01, p. 199–210. IEEE Computer Society, USA (2001)
46. Ipek, E., McKee, S.A., Caruana, R., de Supinski, B.R., Schulz, M.: Efficiently Exploring Architectural Design Spaces via Predictive Modeling. In: Proceedings of the 12th International Conference on Architectural Support for Programming Languages and Operating Systems, ASPLOS XII, p. 195–206. Association for Computing Machinery, New York, NY, USA (2006)
47. Jiang, Y., Zhang, E.Z., Tian, K., Shen, X.: Is Reuse Distance Applicable to Data Locality Analysis on Chip Multiprocessors? In: Proceedings of the 19th Joint European Conference on Theory and Practice of Software, International Conference on Compiler Construction, CC10/ETAPS’10, pp. 264–282. Springer (2010)
48. Kaxiras, S., Young, C.: Coherence Communication Prediction in Shared-memory Multiprocessors. In: Proceedings Sixth International Symposium on High-Performance Computer Architecture. HPCA-6 (Cat. No. PR00530), pp. 156–167. IEEE, IEEE, Piscataway, NJ, USA (2000)
49. Keramidas, G., Petoumenos, P., Kaxiras, S.: Cache replacement based on reuse-distance prediction. In: 2007 25th International Conference on Computer Design, pp. 245–250. IEEE, NY, USA (2007)
50. Kise, K., Katagiri, T., Honda, H., Yuba, T.: The SimCore/Alpha Functional Simulator. In: Proceedings of the 2004 workshop on Computer architecture education: held in conjunction with the 31st International Symposium on Computer Architecture, pp. 24–es (2004)

51. Lattner, C., Adve, V.: LLVM: A Compilation Framework for Lifelong Program Analysis & Transformation. In: Proceedings of the International Symposium on Code Generation and Optimization: Feedback-directed and Runtime Optimization, CGO ’04, pp. 75–86. IEEE Computer Society, Washington, DC, USA (2004)

52. Lee, B.C., Collins, J., Wang, H., Brooks, D.: CPR: Composable performance regression for scalable multiprocessor models. In: 2008 41st IEEE/ACM International Symposium on Computer Architecture, pp. 270–281. IEEE (2008)

53. Lee, S., Meredith, J.S., Vetter, J.S.: COMPASS: A Framework for Automated Performance Modeling and Prediction. In: Proceedings of the 29th ACM on International Conference on Supercomputing, ICS ’15, p. 405–414. Association for Computing Machinery, New York, NY, USA (2015)

54. Liao, C., Quinlan, D.J., Panas, T., de Supinski, B.R.: A ROSE-Based OpenMP 3.0 Research Compiler Supporting Multiple Runtime Libraries. In: Proceedings of the 6th International Conference on Beyond Loop Level Parallelism in OpenMP: Accelerators, Tasking and More, IWOMP’10, pp. 15–28. Springer-Verlag, Berlin, Heidelberg (2010)

55. Maeda, R.K.V., Cai, Q., Xu, J., Wang, Z., Tian, Z.: Fast and Accurate Exploration of Multi-level Caches Using Hierarchical Reuse Distance. In: 2017 IEEE International Symposium on High Performance Computer Architecture (HPCA), pp. 145–156. IEEE, Piscataway, NJ, USA (2017)

56. Malakar, P., Balaprakash, P., Vishwanath, V., Morozov, V., Kumar, K.: Benchmarking Machine Learning Methods for Performance Modeling of Scientific Applications. In: 2018 IEEE/ACM Performance Modeling, Benchmarking and Simulation of High Performance Computer Systems (PMBS), pp. 33–44 (2018)

57. Mattson, R.L., Gecei, J., Slutz, D.R., Traiger, L.L.: Evaluation Techniques for Storage Hierarchies. IBM Syst. J. 9(2), 78–117 (1970)

58. McCurdy, C., Fischer, C.: Using Pin as a Memory Reference Generator for Multiprocessor Simulation. SIGARCH Comput. Archit. News 33(5), 39–44 (2005)

59. Nethercote, N., Seward, J.: Valgrind: A Framework for Heavyweight Dynamic Binary Instrumentation. SIGPLAN Not. 42(6), 89–100 (2007)

60. Niu, Q., Dinan, J., Lu, Q., Sudayappan, P.: PARDA: A Fast Parallel Reuse Distance Analysis Algorithm. In: Proceedings of the 2012 IEEE 26th International Parallel and Distributed Processing Symposium, IPDPS ’12, p. 1284–1294. IEEE Computer Society, USA (2012)

61. Obaida, M.A., Liu, J., Chemnupati, G., Santhi, N., Eidenbenz, S.: Parallel Application Performance Prediction Using Analysis Based Models and HPC Simulations. In: Proceedings of the 2018 ACM SIGSIM Conference on Principles of Advanced Discrete Simulation, SIGSIM-PADS ’18, p. 49–59. Association for Computing Machinery, New York, NY, USA (2018)

62. Pakin, S., McCormick, P.: Hardware-independent application characterization. In: 2013 IEEE International Symposium on Workload Characterization (ISWJC), pp. 111–112 (2013)

63. Patel, A., Afram, F., Chen, S., Ghose, K.: MARSS: A Full System Simulator for Multicore X86 CPUs. In: Proceedings of the 48th Design Automation Conference, DAC ’11, p. 1050–1055. Association for Computing Machinery, New York, NY, USA (2011)

64. Payer, M., Kravina, E., Gross, T.R.: Lightweight Memory Tracing. In: 2013 USENIX Annual Technical Conference (USENIX ATC 13), pp. 115–126. USENIX Association, San Jose, CA (2013)

65. Pouchet, L.N.: Polybench: The Polyhedral Benchmark Suite. URL: http://www.cs.ucla.edu/pouchet/software/polybench (2012)

66. Reddi, V.J., Settle, A., Connors, D.A., Cohn, R.S.: PIN: A Binary Instrumentation Tool for Computer Architecture Research and Education. In: Proceedings of the 2004 Workshop on Computer Architecture Education: Held in Conjunction with the 31st International Symposium on Computer Architecture, WCAE ’04, p. 22–es. Association for Computing Machinery, New York, NY, USA (2004)

67. Rodrigues, A.F., Hemmert, K.S., Barrett, B.W., Kersey, C., Oldfield, R., Weston, M., Risen, R., Cook, J., Rosenfeld, P., Cooper-Balis, E., Jacob, B.: The Structural Simulation Toolkit. SIGMETRICS Perform. Eval. Rev. 38(4), 37–42 (2011)
68. Sabarimuthu, J.M., Venkatesh, T.G.: Analytical Derivation of Concurrent Reuse Distance Profile for Multi-Threaded Application Running on Chip Multi-Processor. IEEE Transactions on Parallel and Distributed Systems 30(8), 1704–1721 (2019)

69. Santhi, N., Eidenbenz, S., Liu, J.: The Simian concept: Parallel Discrete Event Simulation with interpreted languages and just-in-time compilation. In: 2015 Winter Simulation Conference (WSC), pp. 3013–3024 (2015)

70. Schuff, D.L., Kulkarni, M., Pai, V.S.: Accelerating Multicore Reuse Distance Analysis with Sampling and Parallelization. In: Proceedings of the 19th International Conference on Parallel Architectures and Compilation Techniques, PACT ’10, p. 53–64. ACM (2010)

71. Schuff, D.L., Parsons, B.S., Pai, V.S.: Multicore-Aware Reuse Distance Analysis. In: Proceedings of the 2010 IEEE International Symposium on Parallel & Distributed Processing, Workshops and PhD Forum (IPDPSW), pp. 1–8. IEEE, Piscataway, NJ, USA (2010)

72. Sen, R., Wood, D.A.: Reuse-based Online Models for Caches. In: Proceedings of the ACM SIGMETRICS/International Conference on Measurement and Modeling of Computer Systems, SIGMETRICS ’13, pp. 279–292. ACM, New York, NY, USA (2013)

73. Shalf, J., Dosanjh, S., Morrison, J.: Exascale Computing Technology Challenges. In: J.M.L.M. Palma, M. Daydé, O. Marques, J.C. Lopes (eds.) High Performance Computing for Computational Science – VECPAR 2010, pp. 1–25. Springer Berlin Heidelberg, Berlin, Heidelberg (2011)

74. Sharkey, J., Ponomarev, D., Ghose, K.: Abstract M-SIM: A Flexible, Multithreaded Architectural Simulation Environment. Technical report, Department of Computer Science, State University of New York at Binghamton (2005)

75. Shen, X., Shaw, J., Meeker, B., Ding, C.: Locality Approximation Using Time. In: Proceedings of the 34th Annual ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages, POPL ’07, pp. 55–61. ACM, New York, NY, USA (2007)

76. Shi, X., Su, F., Peir, J.K., Xia, Y., Yang, Z.: Modeling and Stack Simulation of CMP Cache Capacity and Accessibility. IEEE Trans. Parallel Distrib. Syst. 20(12), 1752–1763 (2009)

77. Spafford, K.L., Vetter, J.S.: Aspen: A domain specific language for performance modeling. In: SC ’12: Proceedings of the International Conference on High Performance Computing, Networking, Storage and Analysis, pp. 1–11 (2012)

78. Van den Steen, S., Eyerman, S., De Pestel, S., Mechri, M., Carlson, T., Black-Schaffer, D., Hagersten, E., Eekhout, L.: Analytical Processor Performance and Power Modeling Using Micro-Architecture Independent Characteristics. IEEE TRANSACTIONS ON COMPUTERS 65(12), 3537–3551 (2016)

79. den Steen, S.V., Eekhout, L.: Modeling Superscalar Processor Memory-Level Parallelism. IEEE Computer Architecture Letters 17(1), 9–12 (2018)

80. Sun, G., Hughes, C.J., Kim, C., Zhao, J., Xu, C., Xie, Y., Chen, Y.K.: Moguls: A Model to Explore the Memory Hierarchy for Bandwidth Improvements. SIGARCH Comput. Archit. News 39(3), 377–388 (2011)

81. Terpstra, D., Jagode, H., You, H., Dongarra, J.: Collecting Performance Data with PAPI-C. In: Tools for High Performance Computing 2009, pp. 157–173. Springer (2010)

82. Thazhuthaveetil, M., Vaswani, K., Joseph, P.: Construction and use of linear regression models for processor performance analysis. In: Twelfth International Symposium on High-Performance Computer Architecture, pp. 99–108. IEEE Computer Society, Los Alamitos, CA, USA (2006)

83. Unat, D., Chan, C., Zhang, W., Williams, S., Bachan, J., Bell, J., Shalf, J.: ExaSAT: An Exascale Co-Design Tool for Performance Modeling. Int. J. High Perform. Comput. Appl. 29(2), 209–232 (2015)

84. Wu, M.J., Yeung, D.: Identifying Optimal Multicore Cache Hierarchies for Loop-Based Parallel Programs via Reuse Distance Analysis. In: Proceedings of the 2012 ACM SIGPLAN Workshop on Memory Systems Performance and Correctness, MSPC ’12, p. 2–11. Association for Computing Machinery, New York, NY, USA (2012)

85. Wu, M.J., Yeung, D.: Efficient Reuse Distance Analysis of Multicore Scaling for Loop-Based Parallel Programs. ACM Trans. Comput. Syst. 31(1), 1:1–1:37 (2013)

86. Wu, M.J., Zhao, M., Yeung, D.: Studying multicore processor scaling via reuse distance analysis. In: Proceedings of the 40th Annual International Symposium on Computer Architecture, ISCA ’13, p. 499–510. Association for Computing Machinery, New York, NY, USA (2013)

87. Wu, X., Taylor, V.: Performance Modeling of Hybrid MPI/OpenMP Scientific Applications on Large-Scale Multicore Supercomputers. J. Comput. Syst. Sci. 79(8), 1256–1268 (2013)
88. Zhao, M., Yeung, D.: Using Multicore Reuse Distance to Study Coherence Directories. ACM Trans. Comput. Syst. 35(2) (2017)
89. Zhong, Y., Dropsho, S.G., Shen, X., Studer, A., Ding, C.: Miss Rate Prediction Across Program Inputs and Cache Configurations. IEEE Transactions on Computers 56(3), 328–343 (2007)
90. Zhong, Y., Shen, X., Ding, C.: Program Locality Analysis Using Reuse Distance. ACM Trans. Program. Lang. Syst. 31(6), 20:1–20:39 (2009)