Recent progress in 3D integration technology

Mitumasa Koyanagi(a)
New Industry Creation Hatchery Center, Tohoku University,
6–6–01 Aza-Aoba, Aramaki, Aoba-ku, Sendai 980–8579, Japan
a) koyanagi@bmi.niche.tohoku.ac.jp

Abstract: 3D integration technology is the key for future LSIs with high-performance, low-power and multi-functionality. Especially, to mitigate various concerns caused by device scaling down to 10 nm or less, it is indispensable to introduce a new concept of heterogeneous 3D integration in which various kinds of materials, devices and technologies are integrated on a Si substrate. Future prospects of such a heterogeneous 3D integration technology has been discussed representing typical examples of heterogeneous 3D LSIs after the present situation of 3D integration technology is described.

Keywords: 3D integration, TSV, heterogeneous integration, 3D DRAM, 3D image sensor, 3D microprocessor

Classification: Integrated circuits

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1 Introduction

In high-density and high-performance large-scale integrations (LSIs), various concerns such as higher off-state and sub-threshold leakage, threshold voltage variability, and large signal delay by wiring have become more serious as transistor size continues on the path to scaling down toward 10 nm or less [1]. To overcome these concerns, it is indispensable to introduce a new concept of heterogeneous integration in which various kinds of materials, devices and technologies are integrated on a Si substrate. Such heterogeneous integration is easily realized by three-dimensional (3D) integration, which enables 3D heterogeneous stacking of different kinds of chips such as the compound semiconductor device chip, the photonic device chip and the spintronic device chip on CMOS chips. Heterogeneous 3D integration is indispensable for the future Internet of Things (IoT). IoT is expected to tremendously increase the connectedness of people and things as shown in Fig. 1 [2]. IoT has evolved from the convergence of 3D integration technologies, micro-electromechanical systems (MEMS) technologies, wireless technologies and the Internet. Low power consumption, small form factor, and multi-functionality are required for embedded devices for IoT, and heterogeneous 3D integration can address such issues. This article overviews these 3D integration technologies.

Fig. 1. Possible applications and services for Internet of Things (IoT)

2 Present situation of 3D integration technology

Various kinds of 3D devices or 3D LSIs have been proposed so far [3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16]. The first 3D LSI test chip having three device layers was fabricated using the poly-Si film which is re-crystallized by laser annealing [3]. Another 3D LSI fabrication process using a thinned-wafer transfer method was also proposed where a thinned LSI wafer is bonded to another LSI wafer after the silicon substrate is completely removed except for device areas [5]. However through-Si vias (TSVs) were not used in these 3D test chips. Then a 3D integration technology using through-Si vias (TSVs) suitable for the volume production has been proposed [6, 7, 8]. Several thinned LSI chips with TSVs and metal micro-bumps are vertically stacked in this 3D integration technology as shown in Fig. 2. The 3D integration technology is classified into three categories the via-first, via-middle and via-last by TSV fabrication process. The via-middle and back-via type
via-last methods are widely used to fabricate 3D LSIs. Several 3D LSI prototypes such as 3D-stacked DRAM, 3D-stacked image sensor and 3D-stacked microprocessor have been fabricated by these 3D integration technologies.

### 2.1 3D integration technology using TSVs

The 3D fabrication process flows for via-middle method is shown in Fig. 3 [17]. Deep trenches are formed by RIE (Reactive Ion Etching) after the transistor formation in the via-middle process. These deep trenches are filled with Cu by electroplating after forming the oxide liner, barrier metal layer and Cu seed layer inside trenches. Then the multilevel metallization layers are formed on the TSVs after Cu CMP (Chemical Mechanical Polishing). The LSI wafer with Cu-TSVs is temporarily bonded onto a support wafer after the formation of CuSn or CuSnAg microbumps, and then thinned from the backside by the mechanical grinding and CMP. After exposing the bottom of Cu-TSV and forming CuSn or CuSnAg on it, the support wafer is de-bonded from the thinned LSI wafer. Finally thinned chips with Cu-TSVs and metal microbumps are stacked on a Si interposer or organic substrate. A Si interposer is used to integrate several chips which are interconnected by the redistributed metal lines formed on it. A typical example of TSV fabricated by the via-middle process shown in Fig. 4 [18].

In the back-via process, Cu-TSVs are fabricated after the Si substrate thinning as shown in Fig. 5. Firstly the LSI wafer with metal microbumps is temporarily...
bonded onto a support wafer and then the deep trench is formed from the backside by RIE after thinning the Si substrate. After that, the interlayer dielectric under the first level metallization exposed at the bottom of deep trench is etched off by RIE to expose the first level metallization layer (M1) and then the oxide liner is deposited. This process step is followed by the selective etching of oxide liner at the bottom of deep trench to expose again the first level metallization layer (M1). Then the deep trench is filled with Cu by electroplating after the formation of barrier metal layer such as Ta layer and Cu seed layer. Metal microbumps are also formed on the Cu-TSV at the backside. Then the support wafer is de-bonded from the thinned LSI wafer and finally thinned chips with Cu-TSVs and metal microbumps are stacked on a Si interposer or organic substrate. A typical example of TSV fabricated by the back-via process is shown in Fig. 6 [17].

Fig. 4. Cross-sectional structure of CMOS chip with TSV (a) and SEM cross-sectional views of deep trench and Cu TSV formed by the via-middle process (b).

Fig. 5. 3D integration process flow by back-via process

Fig. 6. SEM cross-sectional views of deep trench and Cu TSV formed by the back-via process. ILD, inter-layer dielectric.
Several reliability issues have to be solved in both via-middle and back-via processes for the volume production of 3D LSIs. In the via-middle process, serious issue of Cu pop-up occurs in the BEOL process step since the Cu-TSVs are exposed to the thermal treatment at higher than 350°C [19, 20, 21]. A rapid crystal grain growth occurs in Cu of TSV at the annealing temperature higher than 350°C which causes the Cu protrusion upward in TSV as shown in Fig. 7(a). Such Cu pop-up gives rise to serious damages to lower level metallization layers and low-k interlayer dielectrics. Such a Cu pop-up is mitigated by forming the multilevel metallization layers after removing the Cu protrusion by CMP. However, it is recommended to fabricate Cu-TSVs after forming lower level metallization layers as shown in Fig. 7(b) in order to completely eliminate the influences of Cu pop-up [22]. In the back-via process, serious issue of Si “notch” occurs in the deep trench formation by RIE since the interlayer dielectric under the first level metallization is exposed after the deep Si trench etching. This exposed interlayer dielectric is charged up during over-etching and consequently the Si substrate around the bottom of deep trench is side-etched to cause Si “notch” as shown in Fig. 7(c). To minimize the notch, it is required to reduce the charge-up by employing the pulsed plasma etching which enhances the charge neutralization at the bottom of deep trench. Another difficult process step is the oxide liner removal at the bottom of deep trench. The oxide liner at the bottom of deep trench has to be selectively removed by RIE without damaging the oxide liner at the trench sidewall. Highly anisotropic plasma etching is necessary for the selective removal of the oxide liner at the bottom of deep trench. We could successfully fabricate the back-via-type Cu-TSV with no notch and excellent shape by using highly anisotropic pulsed plasma etching as shown in Fig. 7(d). The process temperature of back-via process has to be lower than that of via-middle process since the Cu-TSV is formed after temporary bonding to the support wafer using the adhesive the temperature tolerance of which is not high. This means that the oxide liner has to be deposited at lower temperature which gives rise to poorer step coverage for deep trench and poorer film quality. Therefore it is more difficult to fabricate Cu-TSV with smaller diameter and larger aspect ratio compared to the via-middle process. On the other hand, we have to be careful for Cu contamination from the Cu-TSV and the backside surface in the via-middle process since the process temperature is higher than that of back-via process [23, 24, 25]. Mechanical stress induced by Cu-TSVs

![Fig. 7. SEM cross-sectional views of TSVs fabricated by via-middle process and back-via process](image)
and metal microbumps, and crystal defects and crystal structure changes produced by thinning the Si substrate are also big concerns in 3D LSIs [26, 27]. Both tensile and compressive stresses are induced by Cu-TSVs and metal microbumps. These mechanical stresses cause significant changes in transistor current. The current change increases as the distance between the transistor and TSV or metal microbump is reduced. Therefore transistors should not be placed inside a specific area around a TSV or a metal microbump which is called a keep-out zone (KOZ) to minimize the current change by mechanical stresses [18]. Crystal defects and crystal structure changes produced by thinning the Si substrate decrease the minority carrier lifetime which causes the degradation in charge retention characteristics.

### 2.2 3D-stacked memories

The 3D integration technology has significantly progressed for these years. The 3D DRAM has contributed to such rapid progress of 3D integration technology [28, 29]. Initially the 3D DRAM has been fabricated aiming the mobile application as shown in Fig. 8. Specifications for such 3D DRAM have been standardized as a wide I/O DRAM with high data band width of 12.8 GBps and low power consumption of 83 mW [30, 31]. The next standardization of wide I/O-2 with the band width of 51.2 GBps has been discussed aiming to replace the LPDDR4. Another approach of 3D DRAM is targeted to the application to high-end systems.

![Fig. 8. 3D DRAM for mobile application, (a) 3D DRAM with 1 Gbit × 8 layers, (b) 2 Gb Mobile Wide-I/O DRAM with 4 × 128 I/Os](image)

Fig. 9 shows the configuration of 3D DRAM called HMC (Hybrid Memory Cube) which is used in a high-end system such as super-computer [32]. The bandwidths of the first generation HMC and the second generation HMC are 128 GBps and 160 GBps, respectively. A controller chip is stacked in HMC and failure bits and failure TSVs can be repaired by the controller chip. The 3D DRAM called HBM (High Bandwidth Memory) is also fabricated for high-end systems [33]. A cost/performance ratio is significantly improved in HMC and HBM since an extremely wide bandwidth can be achieved. The 3D stacked structure with TSVs is going to be employed in Flash memory as well. A 3D-stacked Flash memory is expected to produce a large market for a solid state disc (SSD).
2.3 3D-stacked CMOS image sensor

The 3D-stacked structure is also employed in a CMOS image sensor (CIS). A monolayer CIS chip with TSVs has been already in volume production [34]. Back-via type TSVs with large diameter are used in this CIS chip. A CIS with 3D structure has been also fabricated. Fig. 10 shows a back-illuminated stacked CIS (stacked BI-CIS) where a very thin BI-CIS chip is stacked on a logic chip. Cu-TSVs with different depths are used in this stacked BI-CIS [35, 36]. A 3D-stacked CIS with more layers is expected for the automobile application. A 3D image sensor system module for an advanced driving assistant system is shown in Fig. 11 where a pair of 3D-stacked CIS chip and several 3D-stacked multicore processors are integrated on a Si interposer. High performance image processing using stereo vision for image recognition and obstacle detection is indispensable to guarantee the safety in driving assistant system for automobile. A pair of 3D-stacked CIS chips is used to provide stereo vision images with high data rate of 10000 frames/s in this advanced driving assistant system [37]. A 3D-stacked CIS chip consists of CIS chip, analog chip (CDS), ADC chip, and interface circuit chip. Fig. 12 shows an X-ray CT (computed tomography) scan image of a fabricated 3D-stacked CIS chip [17, 38]. It is obvious in the X-ray CT scan image that the fabricated 3D-stacked CIS chip has a layered structure with four layers where TSVs with the diameter of 5 μm and the length of 50 μm are clearly observed. Excellent performance for block parallel operation to achieve a high frame rate of 10000 frames/s was confirmed in the fabricated 3D-stacked CIS chip.
2.4 3D-stacked microprocessor

3D-stacked multicore processors are used to process a huge number of data provided from a pair of 3D-stacked CIS chips with high speed and low power in the advanced driving assistant system. The parallel processing is indispensable to achieve the high speed and low power operation in multicore processors. The 3D-stacked structure is necessary for the high performance parallel processing. A prototype 3D-stacked dependable multicore processor has been fabricated by the 3D integration technology with the backside via to evaluate its fundamental characteristics [38, 39, 40]. The conceptual structure of this 3D-stacked multicore processor is illustrated in Fig. 13. One of core processors was used as a system-level supervisor processor (Sys-SVP) to control the self-test and self-repair function and to supervise the task allocation and scheduling among core processors. A circuit block diagram and a die photo of core processor fabricated by a standard 90-nm 1-Poly 9-Metal CMOS technology are shown in Fig. 14(a). The die size is $5 \times 5 \, \text{mm}^2$. Several new circuits specific for 3D-stacked multicore processor such as vertical system bus bridge, 3D shared memory controller and on-time self-test controller were added to standard circuits of conventional core processor. Approx-
approximately two thousands of TSVs per each core processor layer were assigned to form the system bus, memory bus and test bus including TSVs in I/O circuits. This core processor chip exhibited the performance of 350 Mips (Dhrystone 2.1) at a clock frequency of 200 MHz. BIST circuits, scan chains and test wrappers are embedded in each core processor. The system bus, memory bus and test bus are formed through stacked processor layers using TSVs in the 3D-stacked multicore processor as shown in Fig. 14(b). TSVs are tested by a boundary scan which extends from the upper die to the lower die. Failure TSVs are replaced by redundant TSVs when they are detected. Function of each die is tested through scan chains using BIST circuits. Input and outputs of test data are manipulated through test wrappers. One of core processors is used as a system-level supervisor processor (Sys-SVP) in the 3D-stacked multicore processor. The Sys-SVP supervises the total function of 3D-stacked multicore processor including the test function. When failure information is obtained, Sys-SVP replaces a failure block or chip by a redundant block or chip on time [41, 42]. A four-layer stacked multicore processor has been fabricated by the 3D integration technology with the backside via. Fig. 15 shows the X-ray CT scan image and SEM cross-sectional view of fabricated 3D-stacked multicore processor. It was confirmed that the fabricated prototype 3D-stacked multicore processor exhibited excellent characteristics.
Future prospects of 3D integration technology

More function and higher integration density are demanded for future LSIs. A new heterogeneous 3D integration technology is required to increase the functionality of future LSIs for IoT whereas monolithic 3D integration technology will be necessary for increasing the integration density.

A very attractive feature in 3D-LSI is the capability of heterogeneous integration. The different kinds of chips are integrated into one stacked chip in heterogeneous 3D integration. Such heterogeneous 3D integration can provide the possibility to achieve new functional LSIs. A super-chip is an example of heterogeneous 3D integration for IoT applications. A super-chip can be achieved by stacking various types of chips with different sizes, different devices, and different materials, as shown in Fig. 16 [43]. So far, several prototype super-chips have been fabricated by stacking microelectromechanical system (MEMS) chips, spin memory chips, and photonic device chips on CMOS chips. Fig. 17 shows a super-chip where a CMOS chip is stacked on an LSI wafer and then a pressure sensor MEMS chip is integrated onto a CMOS chip [44]. A self-assembly technique, described later, was

![configuration of a super-chip](image)

![photomicrograph of MEMS stacked on a CMOS chip](image)

Fig. 15. SEM cross-sectional view (left figure) and X-ray CT scan image of TSV array for 3D multicore processor (right figure). RDL, redistribution layer

Fig. 16. Configuration of a super-chip.

Fig. 17. Photomicrograph of MEMS stacked on a CMOS chip.
used to fabricate this super-chip. Fig. 18 shows a spin memory (spin transfer torque memory) chip stacked on a CMOS chip with static random-access memory and reconfigurable logic circuits where spin memory is used as a configuration memory for reconfigurable logic circuits [45]. As is clear in the I-V characteristic of Fig. 18(c), the magnetic tunneling junction (MTJ) showed an excellent switching behavior with high resistive state and low resistive state even after 3D stacking.

Fig. 19 shows a 3D optoelectronic LSI where an optoelectronic integrated circuit chip with Si photonic devices is stacked on CMOS chips [46]. The respective chip layers are vertically connected by both optical interconnections (TSPV, through-Si photonic via) and electrical interconnections (TSV, through-Si via). A Si optical waveguide with an oxide cladding layer is used as a TSPV. The Si-TSPV and Cu-TSV are simultaneously fabricated in a heterogeneous 3D integration process. We
confirmed that an optical signal is effectively guided by the TSPV. An optical grating coupler with a mirror was used to change the propagation direction of the optical signal. A high coupling efficiency of more than 80% in this optical grating coupler has been obtained [47]. Continuous propagation of optical signal from vertical TSPV to horizontal Si waveguide through the optical grating coupler has been confirmed.

We have developed a new heterogeneous 3D integration technology using self-assembly and electrostatic (SAE) temporary bonding to fabricate a super-chip as shown in Fig. 20 [48]. This new 3D integration technology has been named reconfigured wafer-to-wafer (RW2W) 3D integration technology [49]. First, more than several hundreds of known good dies (KGDs) are sorted from several device wafers and then simultaneously bonded, in a batch, with high alignment accuracy of 1 µm onto a carrier wafer using SAE temporary bonding. High alignment accuracy in SAE bonding is indispensable for forming a high density of electrical connections between the upper and lower chips. This carrier wafer, which consists of many KGDs, is called a reconfigured wafer, and it exhibits very high production yield because of the KGDs. Reconfigured wafers are stacked onto a target interposer wafer at the wafer level. More than several hundreds of super-chips with different configurations can be simultaneously fabricated on a 12-inch wafer with high production throughput and with low cost by using the RW2W integration technology. The surface tension of a liquid is utilized in self-assembly to simultaneously align many dies in parallel. Hydrophilic areas and hydrophobic areas are formed on the surface of a wafer or chip to obtain a high alignment accuracy. We have succeeded in simultaneously aligning five hundreds of chips with the average alignment accuracy of 0.5 µm within 0.1 sec. It is needed in the RW2W integration technology that many chips are temporarily bonded onto a carrier wafer after simultaneously aligning them by self-assembly. Then these bonded chips are simultaneously transferred to a support wafer after de-bonding. Therefore temporarily bonding and de-bonding are very important in the RW2W integration technology. We have developed an electrostatic temporary bonding and debonding method for our RW2W integration technology. Many chips are simultaneously bonded onto the electrostatic carrier (e-carrier) wafer by electrostatic force after the

![Fig. 20. Hybrid self-assembly using self-assembly and electrostatic (SAE) temporary bonding. CA, contact angle.](image-url)
simultaneous alignment by self-assembly and a high voltage with opposite polarity is applied to the electrodes for debonding chips in the SAE bonding.

To further increase the performance and packing density of 3D LSIs, it is necessary for increasing the wiring density and connectivity in the vertical direction by reducing the thickness of each layer as thin as possible. One of methods to do this is the 3D integration of SOI layers. An SOI device wafer is direct-bonded to the other thick device wafer with face-to-face through a silicon oxide or insulator layer and the silicon substrate of upper SOI wafer is completely removed. By repeating this sequence, many SOI layers can be stacked on the thick device wafer. Silicon substrate of each layer remains only in the device areas and hence vertical interconnections (vertical vias) to connect between the upper layer and lower layer are formed through insulator layers but not silicon substrates. Therefore a high density of vertical vias can be easily formed. A 3D-stacked SOI image sensor has been already fabricated using this technology as shown in Fig. 21(a) [21]. By evolving this technology it becomes possible to integrate semiconductor devices other than silicon such as compound semiconductor and germanium onto a silicon device wafer. Fig. 21(b) shows such a heterogeneous integration of InGaAs FET and Ge FET on a Si wafer [50]. Monolithic 3D integration technologies to fabricate transistors on a thin silicon layer formed on a silicon oxide or insulator have been proposed. A poly-crystalline silicon (poly-Si) layer with a large grain size or a single-crystalline silicon layer selectively grown by lateral solid phase epitaxial growth is used as a thin silicon layer. A 3D-stacked SRAM has been fabricated by the lateral solid phase epitaxial growth as shown in Fig. 22 [51]. 3D NAND Flash memories have been fabricated using poly-Si thin film transistors (TFTs) as memory transistors. The vertical poly-Si TFT is used as a memory transistor in the 3D NAND Flash memory, BICS, as shown in Fig. 23 [52]. The BICS is expected as a next generation high-density NAND Flash memory.

Fig. 21. SEM cross-sectional views of SOI 3-D LSI (a) and heterogeneous CMOS devices with InGaAs/Ge stacked structure (b)

Fig. 22. Monolithic 3-D LSI by lateral solid-phase crystal growth
4 Conclusions

This paper reviewed the present situation and future prospects of 3D integration technologies. Two kinds of 3D integration technologies, via-middle and back-via, were described discussing their reliability issues. In addition, 3D-stacked DRAMs, 3D-stacked CMOS image sensor and 3D-stacked microprocessor were described as typical examples of 3D LSIs fabricated by these 3D integration technologies. It was stated that a small production of 3D LSIs has started in 3D-DRAMs represented by the hybrid memory cube (HMC) and the high bandwidth memory (HBM). Furthermore heterogeneous 3D integration technologies and monolithic 3D integration technologies were described as future integration technologies to provide new functionality and to achieve higher integration density. A concept of 3D super-chip was represented and prototype super-chips were fabricated by stacking MEMS chip, spin memory chip, optoelectronic device chip on CMOS chips. A new heterogeneous 3D integration technology using self-assembly and electrostatic bonding were used to fabricate these 3D super-chips.

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Mitsumasa Koyanagi received the B.S. degree in electrical engineering from Muroran Institute of Technology, Japan in 1969 and the M.S. and Ph.D. degrees in electronic engineering from Tohoku University, Sendai, Japan, in 1971 and 1974, respectively. He joined the Central Research Laboratory, Hitachi Ltd. in 1974 where he worked on research and development of MOS memory device and process technology and invented a stacked capacitor DRAM memory cell which has been widely used in the DRAM production. In 1985, he joined the Xerox Palo Alto Research Center, California where he worked on research and development of sub-micron CMOS devices, poly-silicon thin film transistors and the design of analog/digital LSIs. In 1988 he joined the Research Center for Integrated Systems, Hiroshima University, as a professor where he worked on sub-0.1um devices, 3-D integration, and optical interconnection. Since 1994, he has been a professor in Department of Machine Intelligent and Systems Engineering, Department of Bioengineering and Robotics, and currently New Industry Creation Hatchery Center (NICHe), Tohoku University, Japan where his current interests are 3-D integration, optical interconnection, nano-CMOS devices, memory devices, parallel computer system, retinal prosthesis chip, brain-machine interface (BMI) and neural prosthesis chip. He has published more than 300 technical papers and given more than 100 invited talks. He was awarded IEEE Jun-ichi Nishizawa Medal in 2006, IEEE Cledo Brunetti Award in 1996, National Medal with Purple Ribbon in Japan in 2011, and Award of Ministry of Education, Culture, Sports, Science and Technology in 2001, JSAP (Japan Society of Applied Physics) Outstanding Achievement Award in 2015 Optoelectronic Technology Achievement Award in 2004, SSDM (Solid-State Devices and Materials) Award in 1994 and Okouchi Prize in 1990. He is an IEEE fellow and a Japanese Applied Physics Society fellow.