Control Hardware-in-the-loop for Voltage Controlled Inverters with Unbalanced and Non-linear Loads in Stand-alone Photovoltaic (PV) Islanded Microgrids

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Abstract—Unbalanced and nonlinear loads connected to micro-grids (MG) with local distributed energy resources (DERs) are two of the leading causes of power quality problems. Nonlinear loads introduce voltage and current harmonics, and single phase loads can cause voltage and current imbalances in a three phase network. This paper presents a hierarchical control scheme for voltage controlled photovoltaic (PV) inverters with unbalanced and nonlinear loads in micro-grids. The hierarchical control consists of primary control and voltage compensation control (VCC) and a DC voltage regulator (VR). The primary control scheme controls active and reactive power sharing and the VCC regulates the unbalanced voltage and harmonics distortion. The effectiveness of the scheme is verified using Opal-RT real-time simulation and experimentally using control hardware-in-the-loop. The voltage distortion at point of common coupling (PCC) decreased from 6.38 percent to 1.91 percent after compensation, while the unbalanced and harmonic load are shared proportionally among the DG units.

Index Terms—Unbalanced and harmonic compensation, distributed generations, PV islanded, voltage controlled inverters, microgrid

I. INTRODUCTION

In recent years, significant amount of renewable distributed energy resources (DERs) has been recently integrated into both bulk power transmission and distribution power systems to improve the sustainability of electric power systems. Unlike traditional grids, renewable distributed generations (DG) using PV energy source can be installed in every location and require little maintenance effort and also operate locally through power electronics interface converter [1], [2]. The increasing penetration of these inverter-based inertia-less DERs is rapidly changing the dynamics of large-scale power systems and causing several challenges such as inverse power flow, voltage deviation, and voltage fluctuation. To reduce the impact of high intermittent DER penetration, a micro grid (MG) is proposed [3], [7]. MG is a local grid that integrates multiple parallel DG units, energy storage and backup generators to improve reliability of power system operation [3], [8]. A MG can become isolated from the grid during faults, which is called islanding mode [4], [5].

PV-DGs in microgrids provide a clean and cost-effective solution for remote areas with no access to the utility grid such as, rural areas, marine, avionics and automotive. However, due to the intermittency of the PV systems, energy storage units are usually added to fulfill the immediate need for additional power to keep the system stable. However, integrating more PV units with the appropriate control could eliminate these storage units [6], [7].

The control structure for PV-DGs usually consists of a primary controller [5], [9]–[13]. This controller comprises of a power droop controller, virtual impedance and current and voltage controllers. Every DG unit should operate independently while in parallel without communication due to long distance between DGs. Therefore, the droop control approach has been implemented widely in order to control the active and reactive power among the inverters and generate inverter reference voltage and frequency for PV-DGs [5], [9], [10]. However, droop control is unable to share reactive power and harmonic current properly, thus virtual impedance is implemented to enhance the operation of multiple parallel DGs units [10], [14]–[16].

When PV-DGs feed unbalanced and nonlinear loads, the loads generate unbalanced voltage and voltage harmonic distortion respectively. They cause over voltage, overheating and deterioration of power quality on electrical equipment. Those power quality problems on power systems need to be improved. However, primary controllers are not enough to compensate for the power quality problems especially. Thus, to address these challenges, multiple micro grid control approaches are adopted to DG interface inverters in the literatures [3], [7], [12]–[14], [17]–[24].

Some work has been proposed to reduce unbalanced voltage and harmonics distortion using active power filters (APF) in [17], [18]. APFs inject compensating harmonic current in opposite phase to cancel voltage harmonics of the APF installation point. However, the initial and operational costs of the power-electronic-based active power filter are very high.

Some control methods regulate power quality problems and reduce harmonic distortion for sensitive load bus (SLB) under unbalanced and nonlinear loads [3], [14], [19]–[21], [25]. In [3], the authors discuss the negative and zero sequence current compensating controllers in islanded micro grids operating...
under unbalanced conditions but do not use negative sequences compensation of the PCC voltage to improve sharing of the unbalance voltage of the islanded micro grid. The approach presented in [19] is based on applying a secondary control to provide better voltage quality. Unbalanced harmonic compensation (UHC) is adopted to reduce unbalanced harmonic voltage at SLB. A hierarchical control scheme is proposed to improve power sharing and to perform voltage compensation of multi DERs micro grids including non-linear and unbalanced loads using radial basis function neural network-based harmonic power-flow calculations in [20]. Power sharing enhancement control method in [14] and also a fast harmonics suppression strategy in [21] have been proposed to improve current sharing and to compensate reactive, unbalance and harmonic power sharing problems in an islanded ac micro grid. Although power quality at the selected bus can be improved, unbalance of PCC voltage is not compensated to generate compensation reference in the compensation effort controller.

There are two types of PV-DGs that can be classified into current source inverters (CSI) and voltage source inverter (VSI) [6], [9], [11], [26]. CSIs are expected to inject maximum PV power into the grid or directly supply the loads. In [22], a voltage detection based harmonic compensator (HC) was proposed for CSIs based on the discrete Fourier transform (DFT) to better regulate the system harmonics. In [23], the authors presented a CSI under unbalanced and non-linear loads in a grid connected PV-MG. However, a PV-DG in the islanded mode is not capable of providing AC voltage and frequency regulation through CSI [7], [27]. In addition, a harmonic load compensation scheme in [24] is presented based on the voltage control method and a coordinated control of CSI and VSI units is proposed for reactive power sharing and voltage harmonics compensation in [12]. These literature [12], [22], [24] only considered harmonic compensation and not voltage unbalance.

In addition, while PV inverters can behave as voltage sources to supply unbalanced harmonic loads in islanded mode to regulate inverter output voltage, DC link voltage cannot be controlled by the PV inverter [4], [28]. If the generated power from the PV modules is higher than the demand power, a DC voltage regulator controller in [4] is applied to a dc/dc converter to avoid an increase in the DC link voltage by curtailing PV output power.

The impact of DC link voltage control combined with unbalanced distortion compensation based on voltage-source inverter has not been fully investigated in stand-alone systems. Therefore, this paper presents a complete control scheme combining voltage compensation controller with a DC voltage regulator controller under both unbalanced and nonlinear loads for voltage-controlled inverter based islanded PV systems with no storage units. The proposed hierarchical control includes primary controllers regulating inverter voltage and voltage compensating controllers (VCC). While droop control regulates the active and reactive power of the PV DGs considering their rated power capacities, virtual impedance is considered to achieve better power sharing of reactive, unbalance and harmonic powers in the primary level. The VCC is proposed to compensate negative sequences of fundamental and main harmonic voltage at PCC. Also a DC voltage regulator controller is adopted in power stage of the DG unit. The proposed control method is verified using Opal-RT real-time simulation of an IEEE-14 bus distribution system and experimentally using control hardware-in-the-loop.

The remaining parts of the paper are presented as follows: In Section II, the system description and proposed hierarchical control scheme, including the primary controller and the VCC, are presented. Section III is dedicated to present the simulation and experimental results and finally, this paper is concluded in Section IV.

II. SYSTEM DESCRIPTION AND PROPOSED HIERARCHICAL CONTROL SCHEME

Fig. 1: Single line diagram of the IEEE 14 node distribution system with parallel PV-DG units.

![Fig. 1: Single line diagram of the IEEE 14 node distribution system with parallel PV-DG units.](Image)

The power stage of the PV-DG and the proposed hierarchical control scheme block diagram are demonstrated in Fig. 2. The proposed hierarchical control consists of two control levels, the primary control level and the VCC level. The primary control as depicted in Fig. 2 comprises power droop controller, virtual impedance, and proportional resonant (PR) controllers. The power stage of each DG unit in Fig. 2 includes PV solar panels connected to a boost dc/dc converter feeding a voltage source inverter with a LC filter. The primary control is responsible for power sharing between DGs. Secondary control is for PCC voltage quality improvement. The DGs are feeding multiple loads, for example, unbalanced and nonlinear loads.

It is worth noting that the normal mode for triple harmonics is to be zero sequence. However, the unbalanced load will be added so 3rd harmonic compensation will be considered. In addition, the 5th, 7th and 11th harmonics (the main orders) of PCC voltage are considered. In addition, each DG unit has a different power rating. For facilitation, only DG1 details are...
shown in details in Fig. 2. The detailed control loops will be discussed in this section.

A. PV DC/DC Converter Controller

The boost dc/dc converter has a maximum power point tracking (MPPT) mode and a DC voltage regulator (VR) mode (i.e. PI controller).

1) MPPT mode: The controller uses incremental conductance technique to output maximum power of the PV array if the maximum PV power is equal to the demand power load. However the PV output power has to be curtailed in islanded mode to avoid an increase in the DC link voltage \(v_{dc}\) if the generated power from the PV modules is higher than the demand power load. In this case, the VR controller is activated to control the DC link voltage.

2) VR mode: As seen in Fig. 2, when the \(v_{dc}\) exceeds the reference of the DC link voltage \(v_{dc}^{*}\), the DC-DC converter control is able to automatically switch from the MPPT controller to the VR controller [3], [6]. In other words, the output power of the PV array is bounded between the maximum and curtailed power in the islanded mode. Finally, the VR controller generates a reference duty cycle \(D\) as shown in (1).

\[
k_{pdc} \text{ and } k_{ide} \text{ are the control parameters of the proportional integral (PI) of the DC link voltage, respectively.}
\]

\[
D = k_{pdc}(v_{dc}^{*} - v_{dc}) + k_{ide}\int(v_{dc}^{*} - v_{dc})dt \quad (1)
\]

B. Voltage Source Inverter Primary Controller

The detailed structure of one DG inverter primary controller is depicted in Fig. 2. The primary controllers share load power and in addition, adjust the frequency and amplitude of the DG output voltage reference.

1) Power Calculation: The three phase instantaneous active power \(p\) and reactive power \(q\) are calculated using output voltage \(v_{o\alpha\beta}\) and output current \(i_{o\alpha\beta}\) in \(\alpha\beta\) reference frame. The power equations are shown in (2) as

\[
p = \frac{3}{2}(v_{o\alpha}i_{o\alpha} + v_{o\beta}i_{o\beta})
\]

\[
q = \frac{3}{2}(v_{o\beta}i_{o\alpha} - v_{o\alpha}i_{o\beta}) \quad (2)
\]

\(p\) and \(q\) are passed through first order low pass filters (LPF) with 2 Hz cut-off frequency to extract fundamental positive sequence active \(P^+\) and reactive \(Q^+\) power respectively.
In addition, the ratio of power sharing among DGs are given in Table I. Power stage and Control Parameters

| System Parameter | Value (DG1/DG2) |
|------------------|----------------|
| Switching frequency, \( v_{m_p} \) | 10 kHz, 600 V, 370 rad/s |
| PV Power | 3000/6000 W |
| Power Control Parameter | Value (DG1/DG2) |
| \( m_p, n_p \) | 12e-4/6e-4, 1e-0.5e-3 |
| \( V_{ref}, W_{ref} \) | 120 rms V, 370 rad/s |
| \( U_{ref} H D_{ref} \) | 0.2%, 0.2% |
| \( R_{v}^1, R_{v}^2, L_{c}^1 \) | 0.3, 0.4/0.15/0.2 \( \Omega \) 0.5/0.25 H |

The second-order general integrator (SOGI) is designed to extract positive and negative sequences of fundamental and harmonic components for current from a distorted grid voltage in phase locked loop (PLL) algorithm and the detail of the SOGI is presented in [29], [30].

Virtual impedance comprises three impedance loops. Virtual positive sequence impedance (VPI) is designed to improve real and reactive power sharing. Virtual negative sequence impedance (VNI) is implemented to reduce effectiveness of fundamental negative sequence current among DGs. Finally, virtual variable harmonics impedance (VVHI) is also for sharing harmonic power properly among DG units. [14], [19].

Note that only the VPI loop has virtual inductance and resistance. VPI, VNI and VVHI loops in \( \alpha \beta \) reference frame are derived respectively in [5], [9] and [7].

In other words, \( P^+ \) and \( Q^+ \) are the average values of instantaneous active and reactive power.

2) Droop Control: The droop control strategy regulates the active and reactive power. In addition, it controls the power sharing between DGs based on each DG unit power rating and the total load demand without communication between DGs [5], [9], [10]. The droop control characteristics are defined as:

\[
W_{ref} = W^* - (P^+) m_p \\
V_{ref} = V^* - (Q^+) n_p
\]

where \( V^* \) and \( W^* \) represent the amplitude and frequency of the output phase voltage reference and \( m_p \) and \( n_p \) represent active and reactive power proportional coefficient respectively. In addition, the ratio of power sharing among DGs is given by:

\[
P^+_1 \quad P^+_2 \quad P^+_3 \\
P^+_i = \frac{m_{p_i}}{m_p} \\
Q^+_1 \quad Q^+_2 \quad Q^+_3 \\
Q^+_i = \frac{n_{p_i}}{n_p}
\]

where the number of suffixes demonstrate the number of each DG. It should be noted that DG units have different capacities so droop control parameters of the DG1 in Table I are doubled compared to the DG2 parameters in the present paper. Afterwards, the reference of the droop control (\( v_{ref} \)) in Fig. 2 is generated and transformed to \( \alpha \beta \) reference frame to inject for DG voltage controller.

3) Virtual Impedance Controller: The droop control is unable to share reactive power and harmonic current proportionally and therefore the virtual impedance method is implemented to improve the reactive power sharing better among DGs and also to share unbalanced and harmonic load current among DGs. [10], [14]–[16].

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The reference of the DG output voltage in $\alpha\beta$ frame ($V_{\alpha\beta}$) is provided by reference signals of the droop controller ($v_{\alpha\beta}$), the virtual impedance loop ($V_{vr-\alpha\beta}$) and the voltage compensation controller compensation ($V_c$). The reference of the DG output voltage is given as

$$V_{\alpha\beta}^* = v_{\alpha\beta} - V_{vr-\alpha\beta} + V_c. \quad (10)$$

Instantaneous output voltage ($v_{oabc}$) is measured and transformed to $\alpha\beta$ frame ($v_{o\alpha\beta}$). Then, $V_{\alpha\beta}^*$ is compared with $v_{o\alpha\beta}$. The error is received by PR voltage controller to generate the reference current ($i_{\alpha\beta}$). The LC filter inductor current ($i_{Labc}$) is transformed to $\alpha\beta$ frame ($i_{L\alpha\beta}$) and is compared with $i_{\alpha\beta}$ to be controlled by the current controller. The output of the controller transformed back to abc frame produces three phase voltage reference for the pulse width modulator (PWM) block. Finally, the PWM controls the switching of the inverter based on this reference.

### C. Voltage Compensating Controller (VCC)

Nonlinear and unbalanced loads introduce harmonics and unbalance into the system voltage and current. The proposed VCC controller compensates for unbalanced and harmonic voltage at PCC. Dq extraction block and the VCC are depicted in Fig. 2.

The load voltage ($V_{pcc}$) is extracted in the dq extraction block. Signs of +, -, and h representing positive and negative sequence of fundamental component and hth harmonic component, respectively. For example $v_{dq}^{-1}$ is negative sequence of fundamental voltage in $dq$ frame. The PLL block is used to detect voltage frequency and angular frequency ($w$) of the system. $w$ is multiplied by positive and negative sequence of the fundamental component and selected $h^{th}$ harmonic component gain which represent 1, -1, +h, -h respectively. The park transformation is used to transform the $V_{pcc}$ from abc to $dq$ frames. Then, second order (2$^{nd}$) low-pass filter is applied with a cutoff frequency of 5 Hz and damping ratio of 2.5 are used to extract positive and negative sequences of the PCC voltage fundamental and main harmonic components in Fig. 2

Extracted components are received by the VCC in Fig. 2 to reduce unbalanced voltage and harmonic distortion. The values of voltage unbalance factor ($VUF$) and positive and negative harmonic distortion indices ($HD^h$) are calculated in (11)

$$\%VUF = \frac{\sqrt{(V_{-1dq}^{-1})^2}}{\sqrt{(V_{+1dq}^{+1})^2}} \times 100 \quad (11)$$

$$\%HD^h = \frac{\sqrt{(V_h^{dq})^2}}{\sqrt{(V_{+1dq}^{+1})^2}} \times 100.$$
VUF_{ref} and HD_{ref}^h in Fig. 2 are the reference of VUF and h^{th} HD for the PCC voltage. The references are compared with VUF, HD^h. Note that if the unbalanced factor and harmonic references are less than PCC voltage distortion (VUF and HD^h), saturation block must be used to not affect the stability of the control system. The errors are fed to a PI controller to reduce voltage unbalanced and harmonic distortion. Then each output of the PI controller of the negative sequence of the fundamental component and selected h^{th} harmonic component is multiplied by V_{dq}^{-1} and V_{dq}^h respectively. Then, the signals are transformed from dq frame to αβ reference frame and added. The angular frequency generated by the active power controller is set to \( -W_{ref} \) and \( h^*W_{ref} \) for the negative sequence of the fundamental component and selected hth harmonic component, respectively. The references for voltage compensation (\( V_c \)) is generated as follows

\[
V_c = \left( \left( VUF_{ref} - VUF \right) . P1 . V_{dq}^{-1} \right) + \sum_{h=3,-5,+7,-11} \left( \left( HD_{ref}^h - HD^h \right) . P1 . V_{dq}^h \right) \frac{P_{o,i}^c}{\sum_{k}^n P_{o,k}^c} \tag{12}
\]

where \( n \) is the number of DGs. The ratio of \( DG_i \) rated power (\( P_{o,i}^c \)) and the total power of the DG units (\( \sum_k^n P_{o,k}^c \)) is needed to send the proper reference signal to all DG primary controllers considering their power capacities. \( V_c \) is transmitted to each primary local control to mitigate PCC distortion. In the control scheme, the VCC manages compensation of negative sequence of fundamental and main harmonic components.

To summarize the control system in Fig. 2, the PCC voltage (\( V_{pcc} \)) unbalanced and harmonic data are extracted by the dq extraction block to send PCC voltage information to the VCC. In addition, The VCC transmits compensation references of voltage unbalance and harmonic components to all DG primary controller to improve the PCC voltage quality. Primary local controllers receive the compensation voltage signal from the VCC and produce the reference voltage for DGs interface inverters.

### III. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the effectiveness of the proposed method, simulation and experimental results are presented using MATLAB/ Simulink and control hardware-in-the-loop (CHIL) respectively. The test system of the proposed islanded microgrid shown in Fig. 2 consists of two parallel connected PV-DG units unbalanced and nonlinear loads and connected to an IEEE 14 node distribution network. The DG2 unit is chosen to have double the power capacity of DG1. In addition, the
DG1 and DG2 current sharing.

Fig. 10: Output Voltage of PCC in experimental study before (a) and after (b) compensation and (c) DG1 and DG2 current sharing.

Fig. 11: The performance of DC link voltage and DG Power during Step Load.

Fig. 12: The performance of Power Sharing between DGs.

power stage and control parameters are listed in Table I. The effectiveness of the proposed control scheme is tested under unbalanced and nonlinear loads.

A. Simulation Results

This section presents the simulation results of the test system in Fig. 2 using MATLAB/ Simulink.

1) Performance of VCC: Fig. 3 and Fig. 4 depict the PCC output voltage and the frequency spectrum before and after compensation respectively. Fig. 3(a) shows the performance of the conventional micro-grid, with no the virtual impedance and the VCC controller. The PCC output voltage is unbalanced and highly distorted before compensation. In addition, the harmonic distortion (HD) is high especially, the main harmonic components (3rd, 5th, 7th, and 11th) as depicted in Fig. 3(a). Voltage quality of the PCC is improved after compensation as shown in Fig. 3(b). Furthermore, the total harmonic distortion (THD) is reduced as shown in Fig. 4(b) from 6.38% to 1.91%, which is less than 5% maximum THD in compliance with the IEEE-519 standards [15]. The voltage unbalanced factor (VUF) of PCC terminal was reduced from 5.8% to 0.2% with compensation.

2) Performance of VR controller: The performance of the VR controller was verified by applying a step drop in the load at 4 seconds. It can be seen from Fig. 5 that PV power reached to maximum power between 4 and 20 seconds operating at the MPPT mode. Then when the load is dropped at 20 seconds, the VR controller became active and the DC link voltage was regulated to 600 V by curtailing the PV-DG power. It should be noted that, only 4% of maximum output power of the PV array is curtailed in this case.

3) Performance of the load power sharing: Active and reactive power shared proportionally between different rated PV-DGs are presented after compensation as shown in Fig. 6 and Fig. 7 respectively and it should be noted that proper power sharing between DGs demonstrates the effectiveness of the droop controllers and the virtual impedance loop. Also output currents of DG1 and DG2 in Fig. 8 are presented to demonstrate sharing of unbalanced and harmonic load current properly among the DGs after compensation.

B. CHIL Experimental Validation

This section demonstrates the results of the CHIL real-time simulation of the proposed system and controllers and using OPAL-RT as shown in Fig. 9. The power stage including the DGs, inverters and loads are located in Mat-lab/Simulink. The proposed controllers are implemented using Compact Rio-9024 by National Instruments (NI) as the control hardware. The controller algorithm is coded in LabVIEW-FPGA. The experimental results of the CHIL simulation are shown in Fig. 10-12. It can be observed that the results in the experimental study also demonstrate a noticeable improvement in the power quality and sharing. Furthermore, the system is stable under load step change.
IV. CONCLUSION

A novel voltage controlled inverter for combined operation of the voltage compensation controller and the DC voltage regulator controllers is proposed in the PV islanded micro-grid. It has been shown that the voltage controlled compensation method can operate under unbalanced nonlinear loads in the islanded PV micro-grids. Fixing the DC link voltage is achieved by the DC voltage regulator controller. Moreover, simulation results verified the effectiveness of the proposed control method as the PCC voltage distortion is decreased by 70%, while the load power-sharing is achieved among the PV inverters. The effectiveness of the proposed control scheme is validated using Opal-RT real-time simulation of an IEEE-14 bus distribution system and experimentally using control hardware-in-the-loop. The complete simulation and experimental results are discussed.

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