Very large scale integration implementation of seizure detection system with on-chip support vector machine classifier

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Abstract
Epilepsy is one of the most common neurological disorders; it affects millions of people globally. Because of the risks to health that it causes, the study and analysis of epilepsy have been given considerable attention in the biomedical field. In a neurological diagnosis, an automated device for detecting seizures or epilepsy from an electroencephalogram (EEG) signal has a significant role. This research work proposes a very large scale integration implementation system for the automatic detection of seizures. Before classification, feature extraction was performed by discrete wavelet transform (DWT) and on-chip classification was performed by a linear support vector machine. The polyphase architecture of Daubechies fourth-order wavelet three-level DWT was used to minimize computational time. The systolic array architecture-based support vector machine classifier using parallel processing helps to minimize the computational complexity of the proposed method. This research work uses an open access EEG dataset. Hardware implementation was done on a field-programmable gate array (FPGA). Efficient results were produced compared with the existing system on chip (SoC) and FPGA seizure detection systems.

1 | INTRODUCTION

Epilepsy is a neurological disorder characterized by unpredictable seizures. Approximately 1%–2% of people globally experience seizures [1]. Recurrent seizures increase the danger of accidents and even death for patients [2]. A practical method is needed to identify epileptic seizures and to diagnose electroencephalogram (EEG) signals of epilepsy effectively by estimating temporal and spatial information from the brain [3]. Analyzing and diagnosing EEG epileptic seizure signals is time-consuming for physicians. Extricating normal or seizure EEG signals is difficult for the trained neurologist [4]. Hence, it is important to develop an automatic seizure detection system using machine learning (ML) in medical practice.

The ML approach is widely used in the automated detection of epileptic seizures. Previous studies primarily engaged in the feature extraction of seizure properties and classification of its activities. Several ML methods are widely employed in automatic epilepsy detection, such as multilayer perceptron (MLP) [5], dual-tree complex wavelet transforms (DTCWTs) [6, 7], artificial neural network (ANN) [8], and support vector machine (SVM) [9–18].

ANN, MLP, and DTCWT require extensive training and the feature extraction method leads to a complicated design approach. It was reported in Wang et al. [10] that SVM achieves better classification accuracy (ACC) than K-nearest-neighbor (KNN), linear discriminant analysis, naïve Bayesian, and logistic regression for epileptic EEG classification. Amid the classifiers, to achieve better ACC in EEG classification and use non-linear kernels that are easy for fixing boundaries of data points SVM is chosen as the best classifier to detect seizure EEG signals; various hardware implementations of SVM classification phase architectures have been proposed [19–25]. The systolic array architecture is based on an array of processing elements (PEs), which uses parallelism and pipelining techniques to enhance computing speed [19, 20]. In Hussain et al. [24], the proposed SVM classifier’s hardware implementations with the linear kernel classify the microarray dataset with two different architectures that depend on support vectors (SVs) and dimensions (D). In Wang et al. [25], the chip
implementation of the SVM classifier based on a Gaussian kernel yields efficient results. There are strong reasons for using an on-chip classifier for seizure detection in very large scale integration (VLSI) implementation: the kernel trick has two inputs in simple vector calculation, and additional coefficients are not needed.

The EEG signals contain noise and artifacts while recording, which lead to improper diagnosis of seizure signals. Preprocessing is done before classification, which eliminates power line noise and minimizes measuring artifacts such as eye blinking and muscle movement [26]. Generally, a high-pass filter (HPF), low-pass filter (LPF), and band-pass filter (BPF) are used to remove particular frequency ranges [27]. Feature extraction is an essential part of improving the classification performance of the SVM. Many types of features are there: time domain [28, 29], frequency domain [11, 14, 29], time-frequency domain (TFD) [15–17], and linear and non-linear features [18].

The nonstationary EEG signal was precisely represented by a discrete wavelet transform (DWT); it captures both frequency and time information [30], and its subbands have been represented to match the EEG signal's physiological frequency bands [31]. The Daubechies fourth-order (db4) wavelet has been applicable for finding changes in EEG signals with a smoothing feature [32]. Initially, the DWT filter's implementation has followed traditional methods such as convolution-based and lifting-based [33]. The polyphase structure uses fewer computations and reduces delay elements [34]; hence, polyphase-based db4 DWT architecture is selected and implemented to analyse a seizure diagnosis. Feature selection is also a key point of the classification of EEG signals, which reduces the classifier's computational complexity and improves the ACC of classification [35]. Statistical features, such as standard deviation, variance, and sample entropy, have been found to exhibit excellent performance in seizure detection [16, 17]. Still, this type of feature calculation in hardware implementation is complex and needs more resources.

Many works have been developed for automatic seizure detection based on EEG and ML software systems [5–10, 42]. Nevertheless, field-programmable gate array (FPGA) or system on chip (SoC)-based seizure detection systems are more comfortable and flexible for seizure patients to carry all the time [11–18]. In Yoo et al. [11], a novel algorithm was implemented to detect seizures using scalp EEG with on-chip linear SVM. Entropy and spectrum–aided features with a fully integrated SoC were used to suppress epileptic seizures effectively with the help of neural stimulation [12]. In Bin Altaf et al. [13] 16-channel SoC was been implemented for onset seizure detection and termination. Eight-channel patient-specific on-chip non-linear SVM (NLSVM) SoC improves the detection rate (DR) with less energy efficiency [14]. Seizure detection using DWT, sample entropy, and a threshold algorithm was implemented in FPGA, tested with the Bonn university dataset [15]. A three-class classification for epilepsy in FPGA using NLSVM with an on-chip training algorithm, such as modified sequential minimal optimization (SMO) was presented in Wang et al. [16]. Seizure detection using NLSVM, tested with two different publically available datasets, was presented in Feng et al. [17]. In Elhosary et al. [18] optimization techniques with SVM training algorithm (linear kernel and linear and non-linear combination features) were used to detect seizures with hardware implementation in FPGA and application-specific integrated circuits.

However, these works consume lots of resources or power; some papers have use an NLSVM classifier to achieve higher detection ACC. Still, it increases the hardware's complexity with complicated feature calculation circuits [11–18]. To address the shortcomings of these hardware implementations, on-chip linear SVM classifier, polyphase based DWT, and hardware-friendly features are selected to achieve better results in seizure detection. The proposed algorithms are implemented on the FPGA device and were tested using a freely available Bonn university dataset [36].

The main contributions of the proposed system are thus:

1. Linear kernels significantly reduce the computational complexity of SVM training and detection.
2. The polyphase structure increases FPGA's speed and reduces delay elements in the DWT structure.
3. The mean absolute value ( MAV) and maximum values are estimated from the feature extraction and are used to minimize the FPGA's overall computational complexity.
4. A customized SVM classifier implementation of FPGA is presented based on systolic array architectures. Such applications provide minimal versatility in modifying parameters and allow the entire system to reconfigure. In this analysis, hardware implementation tests for the training process are explicitly omitted.
5. A custom fixed-point arithmetic unit is proposed. The framework was implemented with the Verilog language.
6. The proposed system was found to be proficient compared with existing SoC [11–14] and FPGA approaches [15–18].

Sections 2–5 describe the EEG dataset from Bonn University, the hardware implementation of the proposed methodology, experimental results, and discussions on the classification model's performance evaluation and conclusion, respectively.

2 | EEG DATASET

The public available Bonn University database was used in this proposed research work to detect the seizure, inter-ictal, and healthy subjects with the help of EEG signals [36]. The dataset was composed of five subsets (A–E), each containing 100 single channel EEG segments with a length of 23.6 s. The sampling frequency of the epilepsy dataset is 173.61 Hz with a 12-bit resolution such that each segment is composed of 4096 points. The 128-channel amplifier system extracted all of the EEG signals with a common average reference. Sets A and B consisted of portions taken from surface EEG measurements performed on five healthy volunteers with eyes open (A) and
eyes closed (B), respectively. The intracranial EEG of five subjects are in Sets C–E for a presurgical diagnosis. Segments in Set D were recorded from the epileptogenic region. Sets C and D both contained activity at seizure-free periods, and Set E contained only seizure activity. The signals in E are therefore labeled +1, whereas the signals in A–D are labeled −1. This research work uses the whole dataset (A–E), to determine the proposed method’s ability to detect seizures and healthy signals. The implemented design for classification characteristics are thus: Set E (seizure) signals are in a positive class (+1 class), Sets A and B are healthy, and Sets C and D are interictal signals (negative class; −1 class). The Set E signal tested against the other sets (A–D) individually. The four different models are generated from the Bonn University dataset for testing and validation.

3 | METHODOLOGY

The proposed method was implemented in the software and hardware. EEG signals are collected from the Bonn university dataset; it is filtered with a BPF in the signal preprocessing module. A three-level db4 polyphase-based DWT generates four subbands from EEG signals, which is used to calculate the mean and maximum value. The offline proposed method was carried out by MATLAB version 19 software; it creates SVs, training coefficients (\(\alpha_i\)), the labels (\(y_i\)), and bias values (b). The parameters are made available to the on-chip classifier. Finally, classification of the seizure (E) or healthy (A–D) signals was done by the linear support vector machine (LSVM) classifier. Figure 1 shows the proposed seizure detection system.

3.1 | Signal preprocessing

Initially recorded EEG signals are in raw form and have unwanted noise, so preprocessing is vital to remove artifacts. Preprocessing improves the analysis of EEG signals before classification. The BPF was used to remove extra physiological artifacts ranging from 0.5 to 40 Hz [37]. The BPF is designed using the MATLAB Filter Design and Analysis Tool in third order to process EEG signals.

3.2 | Feature extraction

3.2.1 | Implementation of polyphase-based DWT

The filtered EEG signal is subjected to three-level polyphase-based DWT. The DWT generates detail coefficients (D1, D2, and D3) and the approximation coefficient (A3).

The three-level traditional DWT architecture is shown in Figure 2, which is used to decompose EEG signals into detail coefficients (D) and approximation coefficients (A). Each wavelet decomposition architecture level consists of a LPF and a HPF, which are represented by \(G(z)\) and \(H(z)\), respectively, as shown in Equations (1) and (2) [17, 38]:

\[
G(z) = b_0 + b_1 z^{-1} + b_2 z^{-2} + b_3 z^{-3}
\]

\[
H(z) = b_3 - b_2 z^{-1} + b_1 z^{-2} - b_0 z^{-3}
\]

where:

\[
b_0 = \left( \frac{1 + \sqrt{3}}{4\sqrt{2}} \right); b_1 = \left( \frac{3 + \sqrt{3}}{4\sqrt{2}} \right); b_2 = \left( \frac{3 \cdot \sqrt{3}}{4\sqrt{2}} \right); b_3 = \left( \frac{1 - \sqrt{3}}{4\sqrt{2}} \right)
\]

The traditional structure of the three-level wavelet architecture is shown in Figure 2. Significant memory is required because it has to implement the LPF and HPF architecture separately, which increases computational complexity as well as computations between input samples and filter coefficients [17, 34]. An improved architecture of polyphase DWT is shown in Figure 3. The architecture is implemented with the

![Flow diagram of epileptic seizure detection](image-url)
help of db4 three-level polyphase DWT. The registers are used to store the approximation coefficient value to carry out next-level decomposition.

Initially filtered signals are decomposed into approximation coefficient (A1) and detail coefficients (D1) with the help of the improved wavelet architecture. Afterward, the A1 coefficient is sent as an input again into the architecture and it generates the approximation coefficient (A2) and detail coefficient (D2) values. In the final step, A3, D3 decomposed values are generated from the A2 coefficient values. The three-level improved polyphase DWT structure is used to achieve LPF and HPF in one block. The implementation of a polyphase FIR filter has advantages in computational performance when it is used for the decimation of discrete-time signals.

The key benefit of the polyphase decimator (PPD) is that it works at a lower frequency than traditional filter architectures [15–17, 38]. In the PPD architecture, calculations between input samples and filter coefficients are performed after down-sampling, as shown in Figure 4. By adding down-sampling by a factor B (B = 2) to DWT architecture, it run B times faster than the usual filter [39].

LPF and HPF were implemented in one block with the help of a polyphase structure [33, 39], as depicted in Figure 4. The LPF \((G(z))\) and HPF \((H(z))\) are expressed as:

\[
G(z) = G_0(z) + z^{-1}G_1(z) = (h_0 + b_2z^{-2}) + z^{-1}(h_1 + b_3z^{-2})
\]

\[
H(z) = H_0(z) + z^{-1}H_1(z) = (b_3 + b_1z^{-2}) + z^{-1}(-b_2 - b_0z^{-2})
\]

where \(G_0(z), G_1(z), H_0(z),\) and \(H_1(z)\) are polyphase components of LPH and HPF.

3.2.2 Feature extraction

Seizure or healthy signals were classified by extracting transform domain features. The mav and maximum values from three-level DWT are estimated. These features are used to avoid computational and hardware complexity and memory requirements [15–17]. The mav [17] of each coefficient from DWT was calculated using Equation (5):

\[
mav = \frac{1}{N} \sum_{n=1}^{N} |d_n| \quad n = 1, 2, ..., N
\]

Hardware implementation of the mav circuit is shown in Figure 5. The various steps in estimating the mav are:

1. Set the number of datapoints points from each subband of DWT (N).
2. For each data point of the EEG signal, check whether it is positive or negative using the sign bit of input data \(d_n\).
3. Compute the accumulation of data points until N.

**FIGURE 2** Three-level wavelet architecture

**FIGURE 3** Three-level improved polyphase-discrete wavelet transform structure

**FIGURE 4** Polyphase based-discrete wavelet transform structure
(4) The accumulated values are multiplied with the parameter of \((1/N)\).
(5) Finally, the four MAV values are computed from the four coefficients (D1, D2, D3 and A3).

3.2.3 | Maximum value

Hardware implementation of the maximum value is depicted in Figure 6. It has the following steps:

(1) Set the number of datapoints points from each subband of DWT (N).
(2) For each data point of the EEG signal, check whether it is positive or negative using the sign bit of \(i\). If it is negative, avoid that datapoint.
(3) Positive values are compared with the current and previous values to find the maximum value using the comparator.
(4) In each clock cycle, the maximum value is stored in the register.
(5) The maximum value features are calculated from D1, D2, D3 and A3.

Equation (6) is used to calculate the maximum value.

Maximum value = \(\max\{d_n\}_{n=1}^N\)  \(\quad (6)\)

These calculations are used to find the maximum values of coefficients, so each signal it generates eight values such as features or dimensions. The features are sent as input to the LSVM classifier to identify the seizure signal.

3.3 | Support vector machine classifier

SVM is a standard supervised learning method used in biomedical applications for the diagnosis and treatment of disease. The training phase of classification was done with the help of MATLAB, which has parameters used in the on-chip SVM classifier implementation. SVM learns from training set \(\{x_i, y_i\}_1^N\), in which \(x_i \in \mathbb{R}^d\) is the number of features extracted, and \(y_i \in \{-1, +1\}\) is the \(x_i^d\) class label. N is the number of training data \([40]\).

Given the training dataset with labeled values:

\(\{x_i, y_i\} \ldots \{x_N, y_N\}\); \(x_i \in \mathbb{R}^d\) and \(y_i \in \{-1, +1\}\)  \(\quad (7)\)

The online SVM classification phase is an easy computation to find the unknown class label. A new unknown test data \((x_{\text{test}})\) label is found by Equation (9), based on the sign of the classification function. If a linear boundary cannot separate into two classes, a hyperplane must be created to perform linear separation in higher dimensions. The linear kernel used in the proposed hardware implementation method is shown in Equation (8):

\[K(x, x_i) = x_i^T x\]  \(\quad (8)\)

In the classification phase, the on-chip SVM classifier operates in Equation (9) to decide on which side of the hyperplane the test sample lies, as outlined in Equations (10) and (11), respectively \([40]\):

\[f(x) = \text{sign}\left(\sum_{i=0}^{N} y_i a_i K(x_i, x_{\text{test}}) + b\right)\]  \(\quad (9)\)

\[f(x) \geq 0 = x_{\text{test}} \in c_1\]  \(\quad (10)\)

\[f(x) < 0 = x_{\text{test}} \in c_{-1}\]  \(\quad (11)\)

where \(c_1, c_{-1}\) are the class labels of test data.

3.4 | On-chip SVM classifier

The proposed on-chip SVM classifier was implemented based on a systolic array architecture, which is used to compute and determine the sign of Equation (9). The PE is represented in a systolic array architecture to carry out the on-chip classification process \([24]\). The classification phase consists of three RAM blocks to store parameters, and then a classification blocks to find the test signal label value.

The single PE is used to carry the multiply and addition processes. Inputs \(A_i\) and \(B_i\) are multiplied and added to the previous output \((C_i)\) value. Initially, this \((C_{i-1})\) value is zero. Figure 7 illustrates the functionality of PE.
The three different RAM blocks are used to store training sSVs, their corresponding label values \((y_i)\), and their coefficients \((\alpha_i)\). The depth depends upon the number of SVs. The RAM widths of label values are one bit. The width of the remaining parameter RAM block is the same as the data width. The stored values are connected to a classifier to carry out the decision function of the input test signal. The on-chip classifier is shown in Figure 8, which has three different multipliers and is connected in a pipeline manner to perform classification phase computation.

Initially stored test features and SVs values are multiplied with the help of the systolic array architecture. Computation of the linear kernel is the most extensive and time-consuming operation, as shown in Equation (12):

\[
\text{Multiplier 1} = \sum_{i=0}^{SVs-1} \left( \sum_{j=0}^{D-1} x_{ij}U_j \right) \tag{12}
\]

where \(U_j\) is the test feature and \(X_{ij}\) is the matrix form of SVs. In this stage, linear kernel computation operation was done by the systolic array architecture. Figure 9 shows that the systolic array of a D-number of kernel PEs are available, where each PE has the role of receiving one SV \((x_{ij})\) feature from the local First In First Out in every clock cycle and has a separate test feature \((U_j)\). In this multiplier, for each clock cycle, one test vector was calculated in a pipelined manner.

Equation (12) is used to compute the linear kernel operation in a parallel manner and simultaneously carry out the process of test vector and SV multiplication per clock cycle. Consequently, to process one query vector, \(D + \) SV clock cycles are needed by the pipeline to finish the computation.

In Multiplier 2, the SV label values and training coefficients are multiplied using a scalar product. The stored offline values are simultaneously accessed from RAM. The SVs-1 clock cycle delay is required to start the Multiplier 2 operation for proper coordination between the two multipliers. The scalar product of Multiplier 2 is shown in Equation (13).

Computation of a single D is processed by Multiplier 3. In this multiplier stage, scalar product multiplication is carried out by the previous two multiplier results. The multiplication operation is carried out until the number of features (D) is extracted. The linear kernel operation of a single feature (D) is shown in Equation (14):

\[
\text{Multiplier 2} = y_i\alpha_i \tag{13}
\]

\[
\text{Multiplier 3} = \sum_{i=0}^{SVs-1} \left( \sum_{j=0}^{D-1} x_{ij}U_j \right) y_i\alpha_i \tag{14}
\]

D-PEs are used to complete the computation of Equation (14). In each clock cycle, a feature from one SV is sent to the corresponding PE, propagating the partial product to the next PE in the pipeline to the same SV. Here each PE has carried one SV result partially, and the final result gets from the last PE in a systolic array.

Identification of a test class label block is the most straightforward process in the entire classification operation; it is used to add and accumulate values from Multiplier 3 with bias values. The final aggregation result is given in Equation (15):

\[
\text{Classifier result} = \text{sign} \left( \sum_{i=0}^{SVs-1} \left( \sum_{j=0}^{D-1} x_{ij}U_j \right) y_i\alpha_i \right) + b \tag{15}
\]

This equation shows the accumulated result of the decision function, which decides the class label of the test vectors. The most significant bit is used to find the sign of the test vector and the class of the test signal.

4 | EXPERIMENTAL RESULTS AND DISCUSSION

Software- and hardware-related experiments were conducted on a personal computer with 8 GB memory and a 64-bit operating system. The proposed method was implemented...
on the FPGA using fixed-point arithmetic for faster testing and better performance. In this research, the implemented seizure design was evaluated and tested with the Bonn University EEG dataset with MATLAB version 19b software. The overall performance of this method, confusion matrix (CM), receiver operating characteristics (ROC), and boxplot are achieved from the software. The trained phase values are used in the hardware to classify seizure and healthy subjects.

Except for SVM training, all modules are implemented in hardware using Verilog language, synthesized and simulated using Xilinx with the Virtex 7 family. MATLAB version 19b carries out the software-based seizure detection process. The four different cases are used in this work to classify EEG signals. The different sizes of parameters are generated to help the online classification phase on an FPGA. The four cases have 500 instances of 8-dimensional features used in this method. After feature extraction, data normalization techniques were applied to the feature vectors to simplify the training process. Table 1 shows the number of SVs, and bias values generated from the offline SVM training phase.

The TFD features calculated from polyphase-based DWT are used for the training and testing set of the LSVM classifier. Four different classification problems are considered with the recorded EEG signals from the Bonn University dataset (Sets A–E).

To detect the seizure signals effectively from inter-ictal and healthy signals, four different cases are chosen and are included in numerous works in the literature [15–17]. Here, four two-class problems are considered that use various dataset combinations:

A. The sets of A and E perform the two-class classification. The output of this case is healthy or seizure.
B. Segments B and E are used and classified into two classes, such as healthy or seizures. Cases 1 and 2 lead to the isolation of healthy adults from epilepsy patients and the treatment of seizures.
C. EEG segments from Sets C and E are considered the two-class classification, which are classified as inter-ictal or seizure.
D. Sets D and E were chosen to distinguish EEG signals into inter-ictal and seizure. Cases 3 and 4 lead to the occurrence of seizures in controlled epilepsy monitoring.

In these four examples, training and testing feature vectors are 60% and 40%. Table 2 shows the distribution of the vector features chosen for training and testing purposes.

### 4.1 Performance assessment of classification model

The performance criteria for the four different cases determined by four statistical evaluation parameters, such as ACC, and specificity (SPE), sensitivity (SEN) or DR or recall (RL), precision (PR) and F1 score, are calculated as:

\[
ACC = \frac{TP + TN}{TP + TN + FP + FN} \times 100
\]

\[
SEN \ or \ DR \ or \ RL = \frac{TP}{TP + FN} \times 100
\]

\[
SPE = \frac{TN}{TP + FN} \times 100
\]

\[
PR = \frac{TP + FP}{TP}
\]

### Table 1 SVM model with support vectors and bias values

| SVM model | Number of SVs | Bias (b) |
|-----------|---------------|----------|
| Case 1 (E–A) | 10 | 2.8598 |
| Case 2 (E–B) | 10 | 2.6110 |
| Case 3 (E–C) | 11 | 4.2463 |
| Case 4 (E–D) | 34 | 1.9753 |

Abbreviations: SVs, support vectors; SVM, support vector machine.

### Table 2 Variation of training and testing feature vectors

| SVM model | Training | Seizure-free (inter-ictal) | Testing | Seizure | Seizure-free (inter-ictal) |
|-----------|----------|---------------------------|---------|--------|--------------------------|
| Case 3    | 60/100   | 60/100                   | 40/100  | 40/100 |
| Case 4    | 60/100   | 60/100                   | 40/100  | 40/100 |
| SVM model | Training | Seizure-free (normal)    | Testing | Seizure-free (normal) |
| Case 1    | 60/100   | 60/100                   | 40/100  | 40/100 |
| Case 2    | 60/100   | 60/100                   | 40/100  | 40/100 |

Abbreviation: SVM, support vector machine.
F1 score is the harmonic mean between PR and RL. The range for the F1 score is [0, 1]:

$$F_1 \text{ Score} = \frac{2 \times (PR \times RL)}{(PR + RL)} \quad (20)$$

where $TP$ is true positive, $FN$ is false negative, $FP$ is false positive, and $TN$ is true negative. $TP$ refers to cases in which seizure signals are accurately categorized, and $TN$ relates to conditions when seizure-free signals are correctly identified. $FN$ relates to instances when seizure signals are wrongly classified as seizure-free signals. $FP$ is the number of non-seizure signals defined as seizure by the proposed method.

The EEG epilepsy dataset was decomposed into D1, D2, D3, and A3 using polyphase-based DWT, from these coefficients max, and maximum statistical features are calculated to train and evaluate the proposed method. Figure 10 shows the boxplot of EEG dataset signals efficiently through its selected features. Seizure (Set E) signals have varied from normal (Set A–D) signals. The boxplots of the first and bottom of rectangular boxes are the 25th and 75th percentiles, respectively, with the median indicated inside the box compared with some existing SoC approaches.

The model was evaluated using ACC but also several evaluation indexes widely used in ML. The leading assessment indices are CM, ROC, and area under curve (AUC). These indices allow a more in-depth analysis of the performance of the classification model from a classification perspective [1].

The CM for the two EEG dataset categories, E-A, E-A, E-C, and E-D, with the linear SVM classifiers, are depicted in Figure 11. The horizontal and vertical directions of a CM indicate the actual and predicted classes, respectively. The L SVM classifier achieved higher numbers of correct classifications with a smaller number of feature vectors for all four models. The classification error occurred when the proposed design identified the normal signal into a seizure signal, or vice versa. The suggested approach has a high percentage of true positive and true negatives, as depicted on the main diagonal line, but it still prevents errors of false positives and true negatives, as shown by the off-diagonal rows.

To allow the ROC [41] curve to be drawn, the classifier must have a confidence value that is called positive or negative for each sample. If the ROC curve is above the diagonal, this indicates that the classification model has the predictive capability, and conversely, that there is no predictive capability. The optimal condition is that the ROC curve follows the y-axis; that is, the predictability is 100%.

The AUC [41] defines the average performance evaluation of the classifier and measures the performance based on the ROC. In general, the AUC value ranges between 0.5 for a random performance to 1 for accurate classification. Figure 12 shows the ROC curve of four cases with AUC values. Case 1–4 have AUC values of 1, 0.98, 0.992, 0.997, and 0.983, respectively. In each case, the proposed L SVM classifier model efficiently discriminates the seizure signals.

### 4.2 Comparison with prior SoC works

Table 3 compares the proposed research with previous works on the SVM-based SoC seizure detection method. The various approaches in Table 3 are mainly used for comparative purposes of DR or SEN used for four different cases. The
proposed design accomplishes a higher DR with the help of linear SVM and hardware-friendly low-dimensional features and on-chip classifiers. Seizure detection achieved better results with less hardware complexity circuits with low computational complexity.

The results in Table 3 clearly indicate that the proposed seizure detection based on FPGA is efficient compared with some existing SoC approaches.

### 4.3 | Comparison with previous FPGA work

Classification performance was improved in the analysis of the EEG signals by time-frequency features. The highest efficiency was obtained from Case 1, in which ACC, SEN, SPE, and DR for healthy and seizure groups are 100%. This implies a high degree of PR in classifying these two types of EEG signals. In Case 2, the average output indexes are 95%. In this case, EEG segments were falsely classified as healthy subject liable to seizure by the proposed method. The overall ACC of the classification between seizure and healthy signals when eyes were closed 95% is also acceptable. In Cases 3 and 4, DR or SEN achieves 100%, and the ACC value is 97.50% and 96.25% fair. In Wang et al. [15], only three sets were used, such as seizure (Set E) and non-seizure (Sets A and C) to detect seizures. The SEN, SPE, and ACC of the system are 97.2%, 94.5%, and 95.9%, respectively, and the computational complexity is high owing to implementation of sample entropy. The proposed method achieves better results in most cases with all performance metrics, but in Case 2, the DR is 95%. Wang et al. used the NLSVM classifier with maximum and standard deviation features to classify EEG signals with subsets A, D, and E selected to evaluate the performance of the system; it achieved an ACC of 94.2%. Still, the hardware complexity was high, but the proposed method uses only the LSVM classifier to achieve better results in efficiency for the four cases. Feng et al. also used the NLSVM classifier, like Wang et al. [16], and features calculated with complexity circuits. Hence, that increases the burden of the hardware device. However, this method only uses hardware-friendly features that were efficiently implemented using VLSI circuits and it achieves a better DR. In Elhosary et al. [18], an LSVM classifier with linear and non-linear features was used to detect seizures. In the proposed design, the focus is on efficiently classifying seizure signals using a low-dimensional feature vector with an on-chip LSVM classifier. The performance of the proposed hardware system was also verified using the two categories of EEG signals with four cases. The proposed method achieves better results compared with the previous seizure detection method shown in Table 4.

![Confusion matrices showing results of four cases of EEG classification](image-url)
**FIGURE 12** ROC curve and AUC values of four cases. AUC, area under curve; LSVM, linear support vector machine; ROC, receiver operating characteristics

**TABLE 3** Comparison with previous SoC based seizure detection works.

| References       | Yoo et al. [11]          | Chen et al. [12]           | Bin Altef et al. [14]          | Proposed research |
|------------------|--------------------------|---------------------------|--------------------------------|-------------------|
| Domain/filtering | Frequency domain/ BPF    | Time-frequency/fast Fourier transform | Frequency domain/ BPF        | Time-frequency/ DWT |
| Features         | Spectral energy          | Time-domain entropy and frequency spectrum | Spectral energy              | Mean absolute value and maximum |
| Classifier       | Linear                   | Linear least square       | Non-linear                    | Linear            |
| On-chip training | No                       | No                        | No                             | No                |
| Technology       | SoC (0.18 μm CMOS)       | SoC (0.18 μm CMOS)        | SoC (0.18 μm CMOS)            | FPGA (Xilinx Virtex 7) |
| Detection rate (or) sensitivity (%) | 84.4                     | 92                        | 95.1                           | Case 1–100       |
|                   |                          |                           |                                | Case 2–95        |
|                   |                          |                           |                                | Case 3–100       |
|                   |                          |                           |                                | Case 4–100       |

Abbreviations: BPF, band-pass filter; DWT, discrete wavelet transform; FPGA, field-programmable gate array; SoC, system on chip.
CONCLUSION

A VLSI architecture for automatic seizure detection was implemented with polyphase DWT-based feature extraction and an on-chip LSVM classifier. Three-level polyphase-based DWT was used to generate the coefficients (D1, D2, D3, and A3). mav and maximum values were calculated as features to minimize the computational complexity of the circuit and were used as the LSVM classifier input. The hardware systolic array architecture of the LSVM classifier uses parallelism within the kernels to speed the classification of EEG data. It is easy to change parameters in the SVM on-chip classifier efficiently for the device in a running state without disturbing other tasks. The proposed method incorporates four different cases detecting epileptic seizures in hardware implementation. The implemented classification method uses polyphase-based DWT (hardware-friendly features), and linear kernel and parallel processing techniques to minimize the computational complexity of the circuit. The designed system was tested on the Virtex 7 family on an FPGA platform and was evaluated using a public epilepsy dataset. Experimental results show that the proposed method produces efficient outcomes in terms of the overall classification of ACC, SPE, SEN, or DR compared with previous methods for the diagnosis of seizures. The outcome of this work will motivate researchers performing VLSI implementation for seizure detection. The proposed FPGA implementation of the LSVM classifier will also aid in the early detection of Alzheimer’s disease and Parkinson’s disease using EEG signals. Future work will include a real-time dataset and implementation of fuzzy SVM on the FPGA chip for an improved DR.

ACKNOWLEDGMENTS

The authors would like to thank their management, principal and head of the department for providing the facilities to carry out this research work, and also for their support and encouragement.

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| Table 4 | Comparison with previous FPGA based seizure detection works. |
|---------|-------------------------------------------------------------|
| Reference | System block | FPGA | Performance (%) |
| Wang et al. [15] | DWT + SampEn + classification | Virtex 6 | SEN 97.2 |
| | | | SPE 94.5 |
| | | | ACC 95.9 |
| Wang et al. [16] | DWT + FeatureExtraction + NLSVM | Virtex5 | ACC 94.2 |
| Feng et al. [17] | Feature extractor + NLSVM | Altera Cyclone II | DR 96.8 |
| Elhosary et al. [18] | Feature extractor + SMO + LSVM | Virtex 7 | SEN 96.77 |
| | | | SPE 90.34 |
| | | | ACC 90.36 |
| Proposed work | DWT + Feature extraction+SVM classification | Virtex 7 (hardware) MATLAB 2019b | Sets Case 1 Case 2 Case 3 Case 4 |
| | | | ACC 100 95 97.50 96.25 |
| | | | DR or SEN or RL 100 95 100 100 |
| | | | SPE 100 95 95.00 92.50 |
| | | | PR 100 95 93.2 95.24 |
| | | | F1 score 100 95 96.39 97.56 |

Abbreviations: ACC, accuracy; DR, detection rate; DWT, discrete wavelet transform; FPGA, field-programmable gate array; NLSVM, non-linear SVM; PR, precision; RL, recall; SEN, sensitivity; SVM, support vector machine; SPE, specificity; SMO, sequential minimal optimization
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How to cite this article: Shanmugam S, Dharmar S. Very large scale integration implementation of seizure detection system with on-chip support vector machine classifier. IET Circuits Devices Syst. 2021;1:1-12. https://doi.org/10.1049/cds.2012.12077