Implementation and analysis of Leakage Reduction Techniques in 6T SRAM cell

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Abstract. Leakage power dissipation is the dominating parameter while calculating in total power consumption of CMOS circuits specially in SRAM cells at 90 nm technology. In modern System on chips (SOCs), SRAM plays an important role because 70 to 80 percent area of any SOC is occupied by memory. So it is important to take care of leakage power dissipation and delay of memory based circuits. In this research paper, SRAM cell with hybrid Sleepy Keeper and Stack approach is proposed to optimize both the above parameters. SRAM cell using hybrid Sleepy Keeper and Stack approach leakage power consumption is 49.9 percent less and its dynamic power dissipation is 28% to 53% less as correlated to other implemented approaches. Read delay and power delay product of SRAM cell with hybrid Sleepy Keeper and Stack approach is less as compared to SRAM cell with Sleepy keeper and SRAM cell using Variable body biasing approach but these parameters value are more as correlated to conventional 6T SRAM cell and SRAM cell using stack approach.

1. Introduction
Nowadays, portable digital systems demand is increasing day by day so the need for device scaling and supply voltage scaling of the MOSFET is increasing [1]. Due to this reason in modern SOC design, the difference between the supply voltage and the threshold voltage of the transistor is very low. So the reduction in channel length of the MOSFET and threshold voltage leads to an increase in threshold current, Gate induced drain leakage (GIDL) drain induced barrier lowering (DIBL)[2]. When the CMOS circuit operates in idle condition leakage current flows when the transistor generally off. In a silicon chip, there are millions of transistors. Due to this reason, the overall leakage power consumption is comparable to dynamic power consumption. Leakage power dissipation increases also because of an increase in temperature. Thousands to billions of transistors are manufactured in a chip of SOC or a microprocessor so every transistor in the microprocessor chip contributes the leakage power dissipation[3]. This leakage power consumption will be huge so it is mandatory to minimize the leakage power consumption in VLSI chips. CMOS circuits static power dissipation purely depends on basic parameters like channel length, supply voltage Vdd, threshold voltage, temperature, and gate oxide thickness[4]. Stacking of PMOS and NMOS between supply voltage Vdd and ground can reduce the leakage power consumption in a high amount. Because the leakage power occurs in the circuits when the transistor is in the off state[5]. Circuit level techniques are essential to achieve good results because the device level voltage scaling techniques do not provide appropriate results. In this research paper we have used previously discussed and new approaches leakage power reduction in 6T SRAM topology, because portable devices' basic need is that primary memory should respond faster[6]. In this manner, SRAM has the advantage that its response is faster and it does not refresh periodically so SRAM is mainly used. In this research paper proposed leakage reduction technique based on SRAM cell operates with low power in standby mode and with high-speed in active mode.

2. Literature Survey

2.1 Conventional 6T SRAM Cell
The Schematic diagram of a conventional 6T SRAM cell is shown in figure 1. The 6T SRAM cell consists of six transistors. Two-pass transistors (NM2 and NM3), two pull up transistors (PM0 and PM1), and two pull-down transistors (NM0 and NM1). Word line (WL) controls the gate of the pass transistors. When the word line becomes high then only the read and write operations can perform. When the word line becomes low the SRAM operates in a hold state because there is no writing and reading operation performed. In this state the power is measured is called leakage or static power dissipation. Write driver is used for successful writing in the cell and it also monitors the presented data. Write enable of the write driver becomes off when the reading operation is to be done. The bit line (bl) and Bit line Bar (blb) have to be pre-charged before reading operation are to start this value should be at the same level of voltage.

In 6T SRAM cell due to voltage difference between nodes of pass transistor the capacitor at one end discharges. Capacitor discharging depends on the value stored at the output (q and q,b). Sense amplifier senses the difference of voltages BIT line and bit line bar and it also amplifies it. The bit line and bit line bar behave as output lines while reading operation[1].

2.2 SRAM Cell with Sleepy Stack Approach

Sleepy Stack approach is developed while combining the sleep transistor approach and forced stack approach. In the circuit given below, this combined approach is used in a 6T SRAM Cell. Sleep transistors behave as on switch while active mode and they act as off switch while sleep mode. The sleepy stack approach increases the speed in different ways. When the sleep transistor becomes switched on, then the current flow in the circuit. So, the switching speed increases in the circuit, and the overall delay decreases[7].

Fig: 1. Conventional 6T SRAM Cell
2.3 SRAM Cell with Sleepy Keeper Approach

We know that in conventional CMOS approach PMOS is not efficient to passing ground and NMOS is not efficient to passing Vdd so PMOS transistors are placed at so pull upside of the circuit because PMOS transistor is efficient to passing Vdd and NMOS transistors are placed at the pull downside of the circuit because the NMOS transistor is efficient to passing ground.
In a pull-up circuit, an extra transistor NMOS is connected in parallel with PMOS. PMOS is the only source of the supply voltage Vdd and the parallel NMOS transistor creates resistance it is also caused of leakage power reduction. Same as in the pull down circuit an extra transistor PMOS is connected in parallel with NMOS. NMOS is the only source in the pull down circuit that passes the ground and another PMOS transistor creates resistance in the circuit. This circuit has the disadvantage that its dynamic power dissipation is more as compare to the sleepy stack approach [8] [9].

2.4 SRAM Cell with Variable Body Biasing Approach

In this approach the leakage power dissipation can be reduced in two ways first is the variable body biasing method and the other one is the sleep transistor approach. In the first way variable body biasing approach two PMOS transistors parallelly connect at pull upside. In which to create a body biasing effect first PMOS transistor source is directly connected to the body of the second transistor. Same as at the pull downside two NMOS transistors are parallel connected in which to create a body biasing effect first NMOS transistor source is directly connected with the body of the next transistor. In the second way to create a sleep effect a separate NMOS transistor is connected with Vdd at pull upside and In the pull-down side, a PMOS transistor is connected with the ground[3].

![SRAM cell with Variable Body Biasing Approach](image)

3. Proposed Approach

3.1 SRAM Cell with Hybrid Sleepy Keeper and Stack Approach

This is the hybrid approach in which we have used a sleepy keeper and stack approach in a single 6t SRAM topology at pull upside and pull downside. Both the approaches advantage can get in a single circuit. The sleepy keeper and stack approach has the advantage that its delay is less as compared to
previous approaches. Its dynamic power and the leakage power dissipation are also less as compared to previously implemented approaches.

![SRAM cell with Hybrid Sleepy Keeper and Stack Approach](image)

**Fig.5: SRAM cell with Hybrid Sleepy Keeper and Stack Approach**

### 4. Simulation Results

In this paper all the reduction techniques are implemented on cadence virtuoso tool with 90nm technology node. Fig. 6 shows the leakage power of 6T SRAM cell with various leakage power reduction techniques with variation in supply voltages. It can be observed that leakage power is minimum with Hybrid Sleepy keeper and Stack technique as compared to other approach at 0.6V supply voltage.

![Leakage power vs supply voltage](image)

**Fig.6: Leakage power vs supply voltage**
Dynamic Power dissipation of 6T SRAM cell with power reduction techniques is shown in Fig. 7. It is worthy to note that Hybrid Sleepy keeper and Stack Approach results in minimum dynamic power dissipation at 0.6V supply voltage as compared to other approaches. Sleepy keeper approach also shows a similar trend as depicted in Fig. 7.

![Fig.7: Dynamic power dissipation vs supply voltage](image)

Read delay of 6T SRAM cell along with power reduction approaches is shown in Fig. 8. It can be seen that 6T SRAM cell has minimum delay as compared to 6T cell with other approaches at 1V supply voltage.

![Fig.8: Read Delay vs supply voltage](image)

Fig. 9 shows the power delay product with variation in supply voltages. It is evident that 6T SRAM cell has minimum power delay product at 1V supply voltage. Furthermore, power delay product with sleepy keeper approach becomes minimum as compared to other approaches at 0.6V supply voltages.
5. Conclusion

In this paper, a detailed analysis of the Conventional 6T SRAM cell and 6T SRAM cell with other power reduction approaches such as Sleepy Stack Approach, Sleepy Keeper Approach, Variable Body Biasing Approach, Hybrid Sleepy keeper and Stack Approach has been performed. Various parameters such as leakage power, dynamic power, read delay and power delay product are investigated. It has been observed that SRAM cell with Hybrid Sleepy keeper and Stack Approach provides the low leakage power consumption and Dynamic power consumption. Read delay and power delay product of SRAM cell with hybrid Sleepy Keeper and Stack approach is improved as compare to SRAM cell with Sleepy keeper and SRAM cell with Variable body biasing approach but these parameters value are high as correlated to conventional 6T SRAM cell and SRAM cell with Stack approach. Summarily SRAM cell with hybrid Sleepy Keeper and Stack approach have more advantage with small tradeoffs.

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