A system-level method for hardening phase-locked loop to single-event effects

Bin Liang, Xinyu Xu, Hengzhou Yuan, Jianjun Chen, Deng Luo, Yaqing Chi and Hanhan Sun

College of Computer, National University of Defense Technology, Changsha 410073, People’s Republic of China
E-mail: liangbin110@126.com and hhsun108@163.com

Abstract
To mitigate the sensitivity of the charge pump in a traditional Phase-Locked Loop (PLL), a single-event-hardened PLL architecture with a proportional and integral path is proposed. The phase margin of the PLL is kept at 58.16° due to the rational design and the output clock frequency ranges from 0.8 to 3.2 GHz. The circuit-level simulation results reveal that the sensitive volume of the hardened PLL decreases by 80% ~ 95%. The novel radiation-hardened PLL circuit was implemented in a 28 nm CMOS technology and irradiated with heavy ions with a linear energy transfer between 1.9 and 65.6 MeV·cm²·mg⁻¹. The proposed radiation-hardened PLL shows one order of single-event effects hardness level higher than the conventional PLL.

1. Introduction

A phase-locked loop (PLL) is a critical component of the electronic system, providing precise and multi-frequency clocks to the other functional blocks. PLL has been widely used in integrated circuits (ICs) in extreme space environments, such as frequency synthesis, clock recovery, high-speed interfaces, microprocessors, and frequency modulation/demodulation. The PLL compares the phase of the input clock and the feedback clock, tunes the voltage-controlled oscillator (VCO) and outputs a stable clock with the target frequency.

Due to the technology node advancement, the IC industry has entered the era of ultra-deep sub-micron technology. With the reduced feature size and the thinner gate oxygen layer, the effects of the total ionizing dose (TID) on ICs in space radiation environments become weaker and weaker, and the single-event effects (SEEs) become more and more significant. Killer electrons, which are trapped in Earth’s outer radiation belt, have been blamed for many spacecraft failures [1]. When traveling through silicon circuits, the ionizing particles create free carriers and the charges are efficiently collected in the high field present in a p/n junction depletion region. The transient currents through drift process and diffusion process disturb the circuit functionality [2, 3]. The killer electron particles even easily penetrate thick shielding and bury themselves in the insulation around sensitive satellite electronics [1]. After particle strikes on the devices in the PLL in the radiation environments, the single-event-induced charge collection by the sensitive nodes results in the variations of the PLL output clock. Although the PLL can modulate the changed clock through the feedback loop, problems such as data loss or processor malfunction may occur during the entire period. Once the single-event-induced clock perturbation exceeds the loop modulation capability, destructive failures such as PLL unlock will happen. An example of the frequency deviation and the phase shift of the PLL output clock following a single-event (SE) strike is shown in figure 1.

Various methods for hardening PLL to single-event transient (SET) have been proposed at the module level [4–6]. However, there are still few studies on the system-level hardening methods. In this paper, a SE-hardened PLL architecture with separate proportional and integral paths is proposed, according to the PLL systematic structure and the main sensitive paths to SET. The proposed radiation-hardened PLL circuit was designed in a 28 nm CMOS technology and verified by SET simulations. Finally, the prototype chip was silicified and tested in the heavy-ion experiments.
2. A system-level method for hardening PLL

2.1. Conventional PLL

The conventional PLL architecture is mainly composed of five parts: phase-frequency detector (PFD), charge pump (CP), low-pass filter (LPF), voltage-controlled oscillator (VCO), and feedback divider (FB-DIV), as shown in figure 2. The reference clock and the feedback-divided clock are sent into the PFD for phase comparison. According to the phase difference of the two clocks, the PFD outputs UP and DN signals with different widths to respectively control the charging and discharging switches of CP. The charging and discharging currents of the CP pass through the integral capacitance and proportional resistance of the following low-pass filter to generate the control voltage $V_c$ for tuning the VCO output frequency. After frequency division, the output clock signal of VCO generates the feedback-divided clock to compare with the reference clock in PFD and thus complete a cycle. PLL is a negative feedback system. Within the adjustable range of the system, the frequency and phase differences between the reference clock and the feedback-divided clock are being reduced and will be eventually fixed to lock the VCO output clock.

A particle strike on a sensitive node in CP will cause a transient current pulse on the output of CP, which will be transmitted to $R_1$ in the LPF block. Since the current pulse is quite fast and the integral capacitance $C_1$ in the LPF block can be seen as grounded, the transient current pulse can create a transient voltage drop across $R_1$ and a voltage disturbance $\Delta V_c$ on the node $V_c$. This disturbance can be transmitted to the VCO, which eventually results in the frequency deviations and phase shifts of the PLL output clock or even oscillating termination for a short time.

Recent studies reveal that CP is one of the most sensitive blocks to SEEs [7–10]. The pulsed laser radiation experiment from Vanderbilt University showed that the frequency deviations and phase shifts of the PLL output clock caused by the laser irradiation on the CP block is at least one order of magnitude higher than that of other blocks [8].

Radiation hardening by design (RHBD) has been proved to be an effective technique to harden the ICs against SEEs [9–12]. To improve the reliability of PLL in radiation environments, many module-level methods have been developed to mitigate the radiation sensitivity of PLL circuits. A typical example is that many years ago, Zhao et al reported the complementary current limiter (CCL) to harden the CP circuit, which effectively reduced the negative impacts of the particle strikes on CP [11]. However, there are still few reports on the system-level hardening and analyzing methods for PLL. Chung et al analyzed the response of SET in the PLL system through a mathematical model and investigated the influences of the PLL bandwidth on SET [10].
For the conventional PLL, the impact of the SEE-induced transient current \( I_{SET} \) on the intermediate node \( V_c \) between CP and LPF can be modeled, as shown in figure 3.

Regardless of \( C_2 \), the transfer function from the transient current to the tuning voltage \( V_c \) can be expressed as

\[
H(s) = \frac{V_c(s)}{I_{SET}} = \frac{R_1^2 + \frac{1}{C_1}}{s^2 + \left(\frac{2\pi K_{VCO}}{2\pi N} + \frac{2\pi K_{VCO}}{2\pi NC_1}\right)s + \frac{1}{C_1}} = \frac{R_1^2 + \frac{1}{C_1}}{s^2 + 2\omega_0s + \omega_0^2},
\]

where \( R_1 \) is the loop filter resistor, \( C_1 \) is the loop filter capacitance, \( I_{CP} \) is the CP current, \( K_{VCO} \) is the VCO gain, and \( N \) is the feedback divider ratio. Moreover, the system damping factor can be given as

\[
\zeta = \frac{R_1}{2\sqrt{\frac{I_{CP}K_{VCO}C_1}{2\pi N}}},
\]

and the system’s natural frequency is described as

\[
\omega_n = \sqrt{\frac{I_{CP}K_{VCO}}{2\pi NC_1}}.
\]

### 2.2. Proposed system-level method for hardening PLL

The research results of Zhao et al reported that in the system-level hardening for the conventional PLL, reducing \( R_1 \) in the proportional path can effectively suppress the influences of SEEs in the CP block on PLL. A reduction of 5 kΩ resistance led to a decrease of 180 mV in \( \Delta V_c \). A small \( R_1 \) has been proven as an effective RHBD method [13].

The proportional path where \( R_1 \) locates is the emphasis of SEE hardening in the PLL. As shown in figure 2, in the conventional PLL, the proportional path \( (R_1) \) and the integral path \( (1/C_1) \) share the CP output \( V_c \), which contributes to the fact that the current pulse induced by the SEEs in CP is converted to the voltage disturbance \( \Delta V_c \) to by \( R_1 \). The proportional path and the integral path can be separated and deployed with different CP blocks. By reducing the CP current in the proportional path, the gain and the sensitive area to SEEs can be decreased to achieve the system-level SEE hardening of the PLL circuit.

The SEE-hardened PLL architecture proposed in this paper is presented in figure 4. In this design, the proportional path is separated from the integral path, which is consistent with that in conventional architecture. An error current in the CP, which is produced by the frequency/phase error from the PFD block, flows through the \( C_1 \) and is integrated to generate the controlled voltage \( V_c \). The voltage-to-current (V2I) block is controlled by \( V_c \) and generates the current \( I_{INT} \) with a different magnitude. Meanwhile, the CP in the proportional path is engaged by the UP/DN signals from PFD and outputs the current \( I_{PROP} \) with a different magnitude. The current \( I_{INT} \) and \( I_{PROP} \) gather together on the node \( V_O \) which acts as the input stimulation of the current-controlled oscillator (CCO). The output clock frequency of the CCO block is linear with the input current.

According to the different frequency and phase information of the input reference clock and the feedback-divided clock, the PFD states (in figure 5) correspond to the CP (particularly \( \text{CP}_{PROP} \)) behavior they produce: 1) if the pulse widths of UP and DN signal are consistent, the current source motivated by the UP signal is turned off and that motivated by the DN signal is turned on, producing the basic current of the \( \text{CP}_{PROP} \) block when the PLL loop stabilizes; 2) if the UP pulse is wider than the DN pulse, the current source motivated by the UP signal is turned on, increasing the output current of the \( \text{CP}_{PROP} \) block; 3) if the UP pulse is narrower than the DN pulse, the current source motivated by the UP signal is turned off, decreasing the output current of the \( \text{CP}_{PROP} \) block. In the last two cases, the pulse widths of UP and DN signals finally become the same after the negative feedback in the PLL loop. As a result, the output current of the \( \text{CP}_{PROP} \) varies and adjusts the instantaneous frequency or phase of the CCO block, only when frequency or phase errors exist between the reference clock and the
feedback-divided clock. When the PLL is stable, the output current of the CP\textsubscript{PROP} is fixed at the basic current and does not regulate the CCO. This is the loop adjustment mechanism of the proportional path.

Since the proportional and integral paths are separate, a decent ratio of the loop current and capacitance contributes to the smaller size of the active devices in these blocks compared with the conventional PLL. Generally speaking, the smaller the gain of the proportional path is, the harder the PLL will be to the SEE. However, if the ratio \(I_{\text{PROP}}: I_{\text{INT}}\) is too small, the phase margin of the PLL loop will be insufficient and cause the degradation in the loop stability. Weighing the contradictory aspects, the ratio \(I_{\text{PROP}}: I_{\text{INT}}\) is chosen as \(1/2\) based on the simulation results of the system model. The phase margin is \(58.16^\circ\) accordingly, and the PLL loop is stable. Meanwhile, the circuit scale of the CP\textsubscript{PROP} block is about \(1/3\) of that of the CP in the conventional PLL. Thus, the sensitive area of the charge pump decreases by \(2/3\) compared with the conventional PLL. Note that in the conventional PLL, the resistor \(R_1\) can be replaced by the active devices to save layout area and reduce the device complexity [14], and these alternative active devices will also contribute to the sensitive volume to SEEs and directly reflect on the control voltage \(V_c\). These additional sensitive devices do not exist in the hardened PLL, so the SEE immunity of the PLL is further improved.

Redundancy is one of the important hardening approaches to reduce single-event error rates (SER) and has been implemented in various digital microelectronics [15]. In our design, the main digital parts include PFD, FB-DIV, band calibration block, and lock detector. To maintain the loop stability in radiation environments, we adopted the customized and radiation-hard flip-flops and latches based on the Dual Interlocked Cell (DICE) [16]. The master-slave interlocked structure with the data redundancy ensures that the latched bit value is tolerant against the SEEs. The employed DICE-topology designs were developed and proven robust [17, 18]. Besides, the unlock due to SEEs can be mitigated by radiation-hardened layout rules that optimize the space between N-type and P-type active areas, the space between active areas and substrate contacts, and so on. Those rules were followed in our previous works and also verified [4, 11, 19].
3. Simulation results

A common circuit model for simulating the single-event effects is a double-exponential, time-dependent current pulse [19–21]. This pulse can be given by:

\[ I(t) = \frac{Q}{\tau_a - \tau_b} \left( e^{-\frac{t}{\tau_a}} - e^{-\frac{t}{\tau_b}} \right), \]

where \( t \) is the time, \( Q \) is the charge, \( \tau_a \) and \( \tau_b \) are the time constants concerning the carrier lifetimes.

Based on the proposed method for hardening PLL to SEEs, the circuit was fabricated in a 28 nm CMOS technology. To get the precise time profile of the double-exponential current pulse in this technology, we created the 3D model of the transistors (shown in figure 7) by using TCAD and calibrated the characteristic I-V curve of the transistor model via the Hspice tool. Afterward, we delivered the simulations of the single-event strike at a linear energy transfer (LET) of 37 MeV·cm²/mg⁻¹. The peak of the current pulse is 750 μA, and the time constants were calibrated as \( \tau_a = 4 \) ps and \( \tau_b = 400 \) ps. To simplify the simulations, we used a pair of current pulses with the same amplitude and the opposite direction for the NMOS and PMOS transistors.

Figure 6. The V2I block in the hardened PLL does not introduce additional sensitive areas: (a) The VCO and its surrounding blocks in the conventional PLL; (b) The CCO and its surrounding blocks in the hardened PLL.

Figure 7. The 3D model of the transistors by TCAD.
The opposite current pulses were induced on the nodes $V_c$ and $V_O$ in the radiation-hardened PLL (figure 4) at different times, to investigate the SEE hardness of the proposed PLL circuit. The configuration of this PLL is summarized in table 1.

Figure 8 presents the simulated result of the positive single-event strike by the double-exponential current pulse on the $V_c$ node in the hardened PLL. The voltage of the $V_c$ node increases by 6.48 mV and the VCO frequency varies by 157.87 MHz. The recovery time of the PLL output frequency and phase is 3.61 $\mu$s. In contrast, the negative single-event strike on the $V_c$ node is illustrated in figure 9. The voltage of the $V_c$ node decreases by 6.41 mV and the VCO frequency varies by 165.68 MHz. The recovery time of the PLL output frequency is 3.64 $\mu$s.

The simulations of the opposite strikes by the same current pulse on the $V_O$ node have been also conducted, as shown in figure 10 and figure 11. For the positive single-event strike, the fluctuation of the VCO frequency is 75.71 MHz and the recovery time of the PLL output frequency is 0.32 $\mu$s, much faster than that of the strikes on the $V_c$ node. The phase recovery time is 3.28 $\mu$s. For the negative single-event strike on the $V_O$ node, the variation

![Figure 8. A positive single-event strike on the $V_c$ node in the hardened PLL.](image)

![Figure 9. A negative single-event strike on the $V_c$ node in the hardened PLL.](image)

| Table 1. Configuration of PLL. |
|-------------------------------|
| Parameters                    | Values |
| Reference clock frequency (MHz) | 25     |
| Feedback divider ratio        | 40     |
| VCO frequency (GHz)           | 1      |
| C1 (pF)                       | 54     |
| IINT (\(\mu\)A)               | 2.6    |
| IPROP (\(\mu\)A)              | 1.3    |
| Bandwith of PLL loop (MHz)    | 1      |

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The fluctuation of the VCO frequency is 80.44 MHz. The recovery times of the PLL output frequency and phase are 0.39 \( \mu \)s and 3.46 \( \mu \)s, respectively.

We also simulated the single-event strikes on the node \( V_C \) in a conventional PLL with the same configurations for comparison. The deviations in the VCO frequency are shown in table 2.

Simulation results reveal that the proposed radiation-hardened PLL possesses a higher level of SET hardness compared to the conventional PLL. The deviations of the VCO frequency due to the strikes on node \( V_C \) decreased by 80% \( \sim \) 90%, while the reductions of approximately 95% were seen in the frequency deviations due to the strikes on node \( V_o \). The hardness improvement significantly results from a smaller integral gain, which limits the impacts of the high-frequency perturbation on the PLL loop due to SEEs. Besides, it also benefits from the reduced sensitive area in the charge pump in both proportional and integral paths. The probability of particle strike drops by nearly half. However, this can only be proven in the experiments rather than in the simulations.
4. Measurements and analysis

The radiation-hardened PLL described above has been manufactured in a 28 nm CMOS technology. The layout of the PLL is shown in figure 12. The total designed area is 297.85 $\mu$m (width) $\times$ 199.97 $\mu$m (height).

4.1. PLL characterization

Figure 13 presents the closed-loop phase noise of the hardened PLL VCO operating at 3.2 GHz. The phase noise was measured to be $-101.89 \text{dBc/Hz}$ at an offset frequency of 100 kHz, and $-104.4 \text{dBc/Hz}$ at an offset frequency of 1 MHz. The integrated jitter (from 10 kHz to 100 MHz) was measured to be 3.87 ps (RMS).

For comparison, the phase noise measurements of the conventional PLL with the same configurations are shown in figure 14. The phase noise was measured to be $-102.55 \text{dBc/Hz}$ at an offset frequency of 100 kHz, and $-103.26 \text{dBc/Hz}$ at an offset frequency of 1 MHz. The integrated jitter (from 10 kHz to 100 MHz) was measured to be 3.75 ps (RMS). No obvious differences were observed in the noise measurements.

The characterization of the conventional and the hardened PLL at room temperature are summarized in table 3. The jitter performances are not extremely degraded and the power consumption is slightly lower by the hardened design when compared to the conventional PLL. Indeed, the system-level hardened architecture significantly reduces the SEE cross-section of the PLL design and therefore improves performance in radiation environments.

4.2. Radiation tests

The single-event strike in space radiation environments is hard to model. At the moment, the terrestrial experimental method, which is the most proximate to the single-event strike, is to use a particle accelerator to accelerate several particles and strike the targets [22–24]. Heavy ion experiments were performed in the Heavy Ion Accelerator Laboratory of the Institute of Modern Physics, Lanzhou Chinese Academy of Sciences and the
As shown in Table 4, five kinds of heavy ions with different LET values were used. Due to the limited beam time, the fluence was $1 \times 10^7$ ions cm$^{-2}$.

During each heavy-ion experiment, the output waveform of the radiation-hardened PLL is captured by an oscilloscope, where the periodical trigger is used to set the SEE trigger condition: the period of the PLL output clock after stabilizing is defined as $T_t$, and its redundancy, $\Delta T_t$, represents the periodical trigger condition. In the process, the real-time clock period is calculated in the oscilloscope. Once $T_{fo} < T_t - \Delta T_t$ or $T_{fo} > T_t + \Delta T_t$, the trigger condition is met and one single event is recorded. The oscilloscope automatically records the clock waveforms within 500 ns before and after the trigger. During the experiment, the VCO was set to oscillate at 3.2 GHz and observed on the oscilloscope after dividing by 4. The sampling rate of the oscilloscope is 20 GSa/s.

With $\Delta T_t = 100$ ps, the trigger condition for this experiment is $T_{fo} < 1.15$ ns or $T_{fo} > 1.35$ ns.

For comparison, the conventional PLL with the same configurations was also tested for SEEs in the heavy ion facility. In Figure 15, the measured cross-section for transients is plotted as the function of LET. For both PLL designs, the cross-section increases with the LETs. At a LET of 65.6 MeV cm$^2$ mg$^{-1}$, the cross-sections of the conventional and the hardened PLL are $8 \times 10^{-6}$ cm$^2$ and $2 \times 10^{-7}$ cm$^2$, respectively. In addition, there is no unlock in the proposed PLL for all single events. The SEE hardness of the radiation-hardened PLL is at least one order higher than that of the conventional PLL.
5. Conclusion

In this paper, a radiation-hardened PLL circuit is presented with a system-level hardening against SEEs in a 28 nm CMOS technology. The most sensitive block to SEEs in a conventional PLL has been analyzed and identified as the proportional path in the loop filter. Based on the previous studies, a radiation-hardened PLL is designed by separately proportional path and integral path. The sensitive volume of the charge pump is much smaller while reducing the integral gain, to mitigate the SEE vulnerability of the PLL circuit. In the simulations of the single-event strike by a double-exponential current pulse, the deviations of the VCO frequency decreased by 80% ~ 90% when striking the node $V_c$, and dropped by approximately 95% when striking the node $V_o$, in the radiation-hardened PLL. Both radiation-hardened PLL and conventional PLL were tested while subjected to heavy ions with a LET up to 65.6 MeV·cm$^{-2}$·mg$^{-1}$. The proposed radiation-hardened PLL shows one order of SEE hardness level higher than the conventional PLL.

Acknowledgments

This research was supported by the National Natural Science Foundation of China (No. 62104257 and No. 61974163). This research was supported by Pre-research project of University of national defense science and technology (ZK21–34). This research was supported by National Defense Science and Technology Key Laboratory fund (WDZC20215250110).

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

ORCID iDs

Hanhan Sun  https://orcid.org/0000-0002-0653-1385

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