Abstract: This study proposes a capacitive feedback transimpedance amplifier (CF-TIA) using a transistor in the direct current (DC) feedback loop for high DC dynamic range. In some applications, the background DC input can vary widely from the minimum to the maximum, and TIA have to sense the target signal even on the top of the maximum DC input. In a conventional CF-TIA, however, the allowable DC input is constrained by the value of the resistor in the DC feedback loop. To allow a fairly high DC input, the resistor is set to a very low value. This causes the thermal noise current to increase significantly. The increased thermal noise is always present even in the minimum DC input, thus degrading the overall noise performance. The circuit proposed herein overcomes this shortcoming by using the transistor instead of the resistor. The adverse effect of the parasitic capacitance of the transistor on system stability is compensated for as well. Then, the analyses of the overall frequency response and design parameters, including the cut-off frequency and attenuation ratio associated with system stability, are presented for the proposed circuit. In addition, in order to cope with the problem that stability is dependent on the amount of DC input, a simple method for ensuring system stability regardless of DC component value is introduced. The presented analyses and the method are generalized for all CF-TIA applications.

Keywords: capacitive feedback; transimpedance; high dynamic DC; system stability; transistor

1. Introduction

Precision instrumentation systems, such as optical receivers [1], electrical sensors [2–5], emerging biosensors [6–8] photodetectors [9–11], and other current-output measurement systems, often contain a transimpedance amplifier (TIA). An operational amplifier (op-amp) with negative feedback is typically used in a TIA. The most typical TIA topology is a resistive feedback TIA (RF-TIA), which is simple and easy to analyze as the feedback resistor directly matches the transimpedance gain. In [3,4,6,7,12–15], a capacitive feedback TIA (CF-TIA) has been proposed to reduce the thermal noise generated by the feedback resistor, as well as overcome difficulties in the integration of high resistance in complementary metal-oxide-semiconductor (CMOS) chips.

The basic topology of the CF-TIA is composed of an integrator and a cascaded differentiator, as shown in Figure 1. The DC feedback loop is typically inserted in the first stage integrator. It provides a DC path to prevent saturation of the integrator’s feedback capacitor \(C_f\) and simultaneously to bias the op-amp. The conventional DC feedback loop consists of an non-inverting integrator to filter the DC components on the feedback path and a resistor \(R_{dc}\) to drain the DC components from the input node. Although a high value of \(R_{dc}\) is preferred to reduce the thermal noise currents of \(R_{dc}\), it limits the maximum allowable DC input with the output voltage range of the op-amp, as in [6,7]. The voltage drop across \(R_{dc}\) with the DC input should be less than the op-amp output voltage range which is usually slightly less than the op-amp supply voltage. The higher the allowable DC input, the lower the value of \(R_{dc}\).
In some applications such as optical sensors, the DC input varies according to the amount of background light. While the normal DC input from the ambient light is typically low, the maximum feasible value of the DC input can be fairly high when intense light is directly incident on the sensors. The TIA has to sense the weak target signal on top of the expected maximum value of the DC input in the worst case scenario. However, to allow for high DC input, the value of $R_{dc}$ should be very low, causing the thermal noise to increase significantly. To make matters worse, increased thermal noise is always present even at normal or low DC inputs, degrading overall system performance. In this study, to overcome the shortcomings of the conventional CF-TIA, a new topology that replaces $R_{dc}$ with the transistor in the feedback loop is introduced. The method of discharging DC inputs using the transistor in the DC feedback loop is one of the widely used methods in various circuits, but it has not yet been used and analyzed for CF-TIA. With the transistor, the high DC can flow with a much smaller voltage drop across the base-emitter (gate-drain) compared to the significant voltage drop that occurs when a resistor is used. The thermal noise of the resistor is then replaced by the shot noise of the transistor.

Actually, when assuming a constant DC input, the shot noise is larger than the thermal noise. However, if the DC dynamic range, i.e., the range from the minimum to maximum DC, is significant, the proposed topology has the benefits in the overall noise. The shot noise of the proposed topology varies with the amount of the DC input. In normal cases, DC inputs are much less than the maximum value, so the proposed topology can exhibit lower noise than conventional topology that always shows the worst thermal noise to cope with maximum DC inputs. The advantage in terms of the noise is more distinct compared to the CMOS implementation of the conventional CF-TIA where the thermal noise and shot noise coexist for the pseudo-resistor [6,7]. For the CMOS implementation, the proposed topology shows the lower noise than the conventional topology by the amount of thermal noise even for the maximum DC input.

The proposed circuit includes a method for compensating for the adverse effect of the parasitic capacitance of the transistor on system stability. The overall frequency response and design parameters, such as the cut-off frequency and attenuation ratio associated with the system stability, are presented and analyzed for the proposed topology. Moreover, the inclusion of an additional capacitor to the DC feedback loop for ensuring system stability regardless of the DC input value is discussed. Through simulations and experiments, the proposed CF-TIA scheme is validated. In this study, the circuit is implemented with discrete components, but the frequency response model and stability analysis presented are generalized to be applicable to all CF-TIA applications and CMOS chip designs.
2. CF-TIA with DC Feedback Path Using Transistor

This section investigates and analyzes the proposed CF-TIA using a transistor in the DC feedback loop shown in Figure 2. The transistor $T_{dc}$ serves as a variable current sink that pulls the average DC input $I_{dc}$ from the signal path under a steady state condition. Note that the high current can flow from the collector (drain) to the emitter (gate) with only a low base-emitter (gate-drain) voltage.

![Proposed DC feedback loop with transistor](image)

**Figure 2.** Capacitive Feedback Transimpedance Amplifier with the proposed DC feedback loop with a transistor.

First, the fundamental performance of the CF-TIA is presented. The achievable bandwidth of the CF-TIA or the upper cutoff frequency, $f_H$, is limited by the gain-bandwidth product of the op-amp $f_{GBWP}$ and the ratio between $C_f$ and $C_{in}$ as follows [6,7]:

$$f_H \leq f_{GBWP} \cdot \frac{C_f}{C_{in} + C_f}, \quad (1)$$

where $C_{in} = C_s + C_{i,op} + C_{\mu} + C_{\mu,c}$ is the total capacitance at the TIA input including the sensor capacitance $C_s$, the input capacitance of the op-amp $C_{i,op}$ (encapsulating the differential and common mode capacitance), the base-collector (gate-drain) parasitic capacitance of the transistor $C_{\mu}$, and the capacitor $C_{\mu,c}$ to compensate the effect of $C_{\mu}$.

Following this, the overall flat gain of the generic CF-TIA can be described as follows:

$$\frac{v_o}{i_{in}} = \frac{C_d R_d}{C_f}, \quad (2)$$

where $C_d$ and $R_d$ constitute the second differentiator, $i_{in}$ is the input current, and $v_o$ is the output voltage of the CF-TIA. Because the gain of the differentiator increases with the frequency until it is rolled off by the open-loop gain of the op-amp, the product of $C_d$ and $R_d$ is constrained as follows:

$$C_d R_d \leq \frac{f_{GBWP}}{2\pi f_{H}}, \quad (3)$$

Note that while both a bipolar junction transistor (BJT) and a field-effect transistor (FET) can be used as $T_{dc}$, the FET shows a higher parasitic capacitance $C_{\mu}$ than that of the BJT, resulting in a reduced bandwidth as in (1). Thus, we use the BJT for $T_{dc}$ here. Then, in order for $T_{dc}$ to be in an active mode,
the appropriate emitter voltage $V_E$ must be set such that the collector-emitter voltage is greater than 0.7 V. Moreover, to compensate for the influence of $C_p$ on system stability, the inverting amplifier $G(s)$ whose overall gain is $-G_o$, and the capacitor $C_{p,c}$ are inserted between the collector and the base of $T_{dc}$.

A detailed analysis of the frequency response of the proposed CF-TIA is presented in next. Applying Kirchhoff’s current law at the negative input node of the integrator gives [16]:

$$i_{in} = sC_f (v_0 - v_{i,o}) + sC_s v_0 + \left( v_0 - \frac{v_{i,o}}{sC_1 R_1} \right) sC_p + \left( v_0 - \frac{G_e v_{i,o}}{sC_1 R_1} \right) sC_{p,c}$$

$$= -v_{i,o} \left( s \left( \frac{C_f + C_s + C_p + C_{p,c}}{A(s)} \right) + sC_f + \frac{G_e C_{p,c} - C_{p}}{C_1 R_1} + \frac{g_m}{sC_1 R_1} \right)$$

$$\approx -v_{i,o} \left( sC_f R_1 + 1 \right) \frac{g_m}{sC_1} \left( 1 + \frac{G_e}{C_1 R_1} \right)$$

(4)

where $v_{i,o}$ is the output voltage of the first stage integrator, $A(s)$ is the open-loop gain of the op-amp, $g_m = (I_{dc} / V_T)$ is the transconductance of $T_{dc}$, $I_{dc}$ is the DC input, $V_T$ is the thermal voltage (approximately 25 mV at a room temperature of 259 K), $C_1$ and $R_1$ constitutes the integrator in the DC feedback loop, and $\beta = G_e C_{p,c} - C_{p}$. In (4), (a) follows from substituting $v_0$ as $-v_{i,o}/A(s)$, and the approximation (b) follows from that $|A(s)|$ is exceedingly high within the system bandwidth.

By rewriting (4) to the transimpedance gain form, the transfer function of the integrator $H_i(s)$ is obtained as follows:

$$H_i(s) = \frac{v_{i,o}}{i_{in}} \approx -\frac{1}{C_f s^2 + \frac{\beta s}{C_1 R_1 C_f} + \frac{g_m}{sC_1 R_1}}$$

(5)

Rewriting (5) to a standard form of the transfer function of a second-order bandpass filter with a center frequency $w_0$ and a damping ratio $\zeta$ ($= 1/(2Q)$) yields:

$$H_i(s) = -\frac{C_1 R_1}{\beta} \frac{2 \zeta w_0 s}{\sqrt{\frac{g_m}{C_1 R_1 C_f}}} + \frac{2 \zeta w_0 s}{\omega_0^2}$$

(6)

where $w_0 = 2\pi f_0$,

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{g_m}{C_1 R_1 C_f}} \quad \text{and} \quad \zeta = \frac{\beta}{2\sqrt{g_m C_1 R_1 C_f}}$$

(7)

Now, we obtain the upper and lower cut-off frequencies, $f_{i,H}$ and $f_{i,L}$, of $H_i(s)$. From the fact that $f_0$ is the geometric mean of $f_{i,H}$ and $f_{i,L}$, and from (5), followings are derived:

$$f_{i,H} \cdot f_{i,L} = \left( \frac{1}{2\pi} \right)^2 \frac{g_m}{C_1 R_1 C_f} \quad \text{and} \quad f_{i,H} + f_{i,L} = \frac{\beta}{2\pi C_1 R_1 C_f}.$$  

(8)

When the wide passband is assumed as $f_{i,H} \gg f_{i,L}$, $f_{i,H} + f_{i,L} \approx f_{i,H}$. Thus, $f_{i,H}$ and $f_{i,L}$ can be expressed as follows:

$$f_{i,H} = \frac{\beta}{2\pi C_1 R_1 C_f} \quad \text{and} \quad f_{i,L} = \frac{g_m}{2\pi \beta}.$$  

(9)

Moreover, from the assumption of wide passband by $\zeta \gg 1/\sqrt{2}$, $f_{i,H} \gg f_{i,L}$ is proved, expressed as

$$\frac{\beta}{2\pi C_1 R_1 C_f} \gg \frac{g_m}{\pi \beta} > \frac{g_m}{2\pi \beta}.$$  

(10)
From the expressions for $\beta$ and $H_i(s)$ in (5), it can be observed that both $G_c$ and $C_{\mu,c}$ ensure the circuit stability. In the absence of $G_c$ and $C_{\mu,c}$, $\beta$ becomes negative, resulting in two positive real poles in $H_i(s)$. If the system has any poles with a positive real part, the part of outputs diverges without a bound, causing system instability. The value of $C_{\mu,c}$ is preferred to be negligibly small relative to the total input capacitance in order to maximize the achievable bandwidth as in (1).

In terms of stability, $G_c$ is preferred to be high, so that makes the system free of gain peaking as $\zeta \geq 1/\sqrt{2}$, even with the high $g_m$. Note that we assume that the stability is determined based on a condition of a maximally flat response (Butterworth response), which is $\zeta = 1/\sqrt{2}$. However, $G_c$ is limited by the condition that the first pole frequency of $G(s)$ should be placed above $f_0$. Note that $f_0$ varies with $I_{dc}$, and the case when $f_0$ exceeds the system bandwidth $f_H$ is not taken into account. The aforementioned discussion suggests the following conditions:

$$C_{\mu,c} \ll C_{in} \quad \text{and} \quad G_c \leq \frac{f_{GBWP}}{f_H}.$$  

(11)

By cascading the differentiator to the integrator, the overall CF-TIA transfer function, $H(s)$, is derived by multiplying $H_i(s)$ by the differentiator transfer function as follows:

$$H_d(s) = \frac{R_d}{R_2} \left( 1 + \frac{1 + sC_dR_2}{1 + sC_cR_d} \right),$$  

(12)

where $C_c$ is used to stabilize the differentiator as $C_c = 1/ (2\pi R_d f_H)$, and $R_2$ is placed parallel to $C_d$ in order to generate a zero in $H_d(s)$ at $f_{i,H}$ in (9) such that $C_dR_2 = C_fR_1C_f$. Then, the flat gain of $H_i(s)$ is multiplied by $R_d/R_2$, and the decrease in $H_i(s)$ beyond $f_{i,H}$ is compensated by the increase in $H_d(s)$ with the introduced zero. The resulting $H(s)$ becomes the bandpass filter transfer function, whose lower cutoff frequency $f_l$ is equal to $f_{i,L}$. $|H_i(s)|$, $|H_d(s)|$, and $|H(s)|$ are shown in Figure 3 for increasing $I_{dc}$ from 10 pA to 10 uA. Note that as $I_{dc}$ increases, $\zeta$ decreases. Eventually, a gain peaking occurs, as shown for $I_{dc} = 10$ uA in Figure 3.

![Figure 3. Transfer functions of the integrator, differentiator, and the overall system without $C_2$ for $I_{dc} = 10$ pA, 100 nA, 1 nA, and 10 uA, where $C_p = 1$ pF, $C_{\mu,c} = 1$ pF, $G_c = 50$, $C_f = 0.2$ pF, $C_d = 1$ nF, $C_c = 8.51$ pF, $R_d = 2$ k$\Omega$, $R_2 = 8.16$ k$\Omega$, $C_1 = 10$ nF, and $R_1 = 100$ k$\Omega$.](image-url)

We can include the additional capacitor $C_2$ parallel to $R_1$ to ensure stability, regardless of the $I_{dc}$ value. In the presence of $C_2$, following the approaches in (4) and (3) gives $H_i(s)$ as
\[
H_i(s) \approx -\frac{1}{s^2 + \frac{1}{1 + \gamma} \left( \frac{\beta}{C_1 C_f R_1} + \gamma g_m \frac{g_m}{\beta} \right) s + \frac{g_m}{(1 + \gamma) C_1 C_f R_1}},
\]

where \( \gamma \) is the parameter that controls the value of \( C_2 \) and system stability, such that \( \beta C_2 = \gamma C_1 C_f \). The design parameters are then described as follows:

\[
f_0 = \frac{1}{2\pi} \sqrt{\frac{g_m}{(1 + \gamma) C_1 R_1 C_f}} \quad \text{and} \quad \zeta = \frac{1}{2\sqrt{1 + \gamma}} \left( \frac{\beta}{\sqrt{g_m C_1 R_1 C_f}} + \gamma \frac{g_m C_1 R_1 C_f}{\beta} \right).
\]

Then, the upper and lower frequencies of \( H_i(s) \) are expressed in two cases depending on the amount of \( I_{dc} \). The first case is for a low \( I_{dc} \) with \( g_m \ll \beta^2/(\gamma C_1 C_f R_1) \), and

\[
f_{i,H} = \frac{\beta}{2\pi(1 + \gamma) C_1 R_1 C_f} \quad \text{and} \quad f_{i,L} = \frac{g_m}{2\pi \beta}.
\]

The second case is for a high \( I_{dc} \) with \( g_m \gg \beta^2/(\gamma C_1 C_f R_1) \), and

\[
f_{i,H} = \frac{\gamma g_m}{2\pi(1 + \gamma) \beta} \quad \text{and} \quad f_{i,L} = \frac{\beta}{2\pi \gamma C_1 R_1 C_f}.
\]

Notably, \( R_2 \) is placed to generate a zero in \( H_d(s) \) at \( f_{i,H} \) of (16) as previously discussed.

Eventually, multiplying \( H_d(s) \) of (12) to \( H_i(s) \) of (13) renders \( H(s) \) to the bandpass filter frequency response whose lower cutoff frequency is expressed as follows:

\[
f_L = \begin{cases} 
\frac{g_m}{2\pi \beta}, & g_m \ll \beta^2/(\gamma C_1 C_f R_1) \\
\frac{\gamma g_m}{2\pi(1 + \gamma) \beta}, & g_m \gg \beta^2/(\gamma C_1 C_f R_1). 
\end{cases}
\]

Note that the inclusion of \( C_2 \) reduces the overall flat gain magnitude by a factor of \( 1 + \gamma \). To achieve the same flat gain magnitude that is exhibited when \( C_2 \) is not included, either \( R_d \) or \( C_d \) should be multiplied by \( 1 + \gamma \). From the arithmetic-geometric mean inequality, \( \zeta \) of (15) has a lower bound of the following:

\[
\zeta \geq \sqrt{\frac{\gamma}{1 + \gamma}},
\]

where equality holds when \( g_m = \beta^2/(\gamma C_1 C_f R_1) \). For \( \gamma = 1 \), the stability is always ensured by \( \zeta \geq 1/\sqrt{2} \), regardless of the \( I_{dc} \) value, as in Figure 4.

Noise performance analysis is presented in the remaining part of this section. The input-referred noise model is commonly used in noise analysis for comparing input signals and noise levels. In this topology, instead of the thermal noise of the resistor, the current noise of the transistor, \( i_{TR} \), is added to the typical root mean square (RMS) value of the input-referred noise expression of [17] as follows:

\[
i_{N,rms} = \sqrt{i_n^2 + i_{TR}^2 + \frac{(e_n 2\pi f_c Cs + \beta)^2}{3}}.
\]

where \( i_n \) is the inverting-input current noise of the op-amp, and \( e_n \) is the differential voltage noise of the op-amp. The noise \( i_{TR} \) is the shot noise of \( T_{dc} \), where \( i_{TR}^2 \approx 2qI_{dc} \) and \( q (= 1.6e - 19) \) is the
electron charge. Note that a flicker noise can be significant when implementing circuits with CMOS technology or using MOSFET instead of BJT in \( I_{dc} \). However, the flicker noise can be made negligible when assuming the broad range of signal bandwidth and using a non-minimal MOSFET area [4].

\[
I_{DC} = 10 \text{ pA} \\
I_{DC} = 1 \text{ nA} \\
I_{DC} = 10 \text{ uA} \\
I_{DC} = 100 \text{ nA}
\]

**Figure 4.** Transfer functions of the integrator, differentiator, and overall system placing \( C_2 = 40.8 \text{ pF} \) such that \( \gamma = 1 \) for \( I_{dc} = 10 \text{ pA}, 100 \text{ nA}, 1 \text{ nA}, \) and \( 10 \text{ uA} \), where \( C_p = 1 \text{ pF}, C_{pc} = 1 \text{ pF}, G_c = 50, 
C_f = 0.2 \text{ pF}, C_d = 1 \text{ nF}, C_c = 8.51 \text{ pF}, R_d = 2 \text{ k}\Omega, R_2 = 8.16 \text{ k}\Omega, C_1 = 10 \text{ nF}, \) and \( R_1 = 100 \text{ k}\Omega \).

The proposed CF-TIA shows better overall noise performance compared to that of the conventional CF-TIA when the dynamic range of \( I_{dc} \) is wide. For example, assume that the dynamic range of \( I_{dc} \) is 30 dB from 100 nA (normal \( I_{dc} \)) to 100 uA (the expected maxima value of \( I_{dc} \)). Because of the maximum \( I_{dc} \), \( R_{dc} \) of the conventional CF-TIA is constrained to 50 k\( \Omega \) (\( = V_s/100 \text{ uA} \)) where the supply voltage \( V_s \) is 5 V. The maximum output voltage of the op-amp is assumed to be the same as the supply voltage. Then, the thermal noise current of \( R_{dc} \) becomes \( 1 \text{ pA}/\sqrt{\text{Hz}} = \sqrt{4kT/R_{dc}} \) where \( k (= 1.38 \times 10^{-23} \text{ J/K}) \) is the Boltzmann constant and \( T (=300 \text{ K}) \) is the absolute temperature.

This thermal noise current always exists even in normal \( I_{dc} \) degrading the overall noise performance. However, in the proposed CF-TIA, thermal noise current of the resistor is eliminated and the shot noise of a normal \( I_{dc} (=100 \text{ nA}) \) becomes \( 0.17 \text{ pA}\sqrt{\text{Hz}} = \sqrt{2qI_{dc}} \), which is much lower than the thermal noise current of 1 pA/\( \sqrt{\text{Hz}} \).

Furthermore, the noise of the proposed circuit is always less than that of the conventional CF-TIA implemented with CMOS, as in [6,7], in which the thermal noise and shot noise currents coexist. If the conventional CF-TIA is implemented with CMOS technology, the feedback resistor is implemented as a pseudo resistor with MOS devices. Therefore, the input-referred noise expression of conventional CMOS CF-TIA includes not only the thermal noise of feedback resistor, but also the shot noise of the MOS [7]. However, (20) has only the shot noise term without the thermal noise term.

Note that here \( \beta \) is associated with the noise contribution of the input capacitance term, the third term in (20). Both the influence on the total noise and the overall system stability should be considered together when determining \( G_c \).

### 3. SIMULATION and EXPERIMENT

The presented circuits were implemented and simulated using PSpice to verify the presented analyses of the transfer functions and design parameters. A photograph of the realized circuit is
presented in Figure 5. All the circuits were built using the same op-amp (OPA657, Texas Instruments). OPA657 has wideband and low-noise characteristics, and its $f_{\text{GBWP}}$ is 1.6 GHz; $A_{\text{ol}}$ is 75 dB at room temperature, and $C_{\text{op}}$ of 5.2 pF. It is to be noted that $f_{\text{GBWP}}$ is not a trimmed parameter and can vary by the maximum $\pm 40\%$ due to the process variation for any op-amp [18]. Consequently, even though the datasheet specifies the $f_{\text{GBWP}}$ to be 1.6 GHz, I have considered $f_{\text{GBWP}}$ to be 1.28 GHz, about 80% of this typical value in order to account for process variations.

![Figure 5. Hardware Implementation.](image)

Note that to compare the simulation, experiment, and analytic results, all values of the discrete components were set equivalently as the assumed values in the analytical example shown in Figure 4. Several variables were set by considering the laser position sensor application and its practical implementation. For the laser position sensor QP154-Q (First Sensor), $C_s$ is assumed to be 20 pF. Taking the lowest value of the practical discrete capacitor, $C_f$ is set to 0.2 pF. By using MMBT5179 NPN transistor (On Semiconductor) with low parasitic capacitance, $C_p$ is set to 1 pF. The $C_d$ value has an upper limit of approximately 1 nF because of the capacitive loading effect at the OPA657 output. In addition, Figure 6 shows an example of the implementation of $G(s)$ for the simulation and experiment. $R_{G,2}$ and $C_G$ render the amplifier AC coupled to prevent $v_{G,0}$ from being saturated with DC components. Given the aforementioned assumptions, the maximum achievable bandwidth was calculated as 9.3 MHz using (1), and overall flat gain magnitude was determined to be $5E + 6$ from (2).

![Figure 6. Implementation of $G(s)$. The values of the discrete components are $R_{G,1} = 1 \Omega$, $R_{G,2} = 50 \Omega$, $R_{G,3} = 1 \text{ M}\Omega$, and $C_G = 1 \mu\text{F}$.](image)

To assess the stability, the magnitude and phase of the loop gain were obtained through simulation, and plotted in Figure 7. Figure 7 shows the magnitude and phase of the loop gain of the integrator, depending on the presence or absence of $C_2$. For low $I_{dc}$, although the phase at low frequencies is about $-180^\circ$, the stability is ensured by a high gain margin. At high frequencies, the phase drops from $-180^\circ$, resulting in a very high phase margin at the gain crossover point where the magnitude of the loop gain reaches unity-gain (0 dB). However, as $I_{dc}$ increases, the point at which the phase begins to drop increases significantly. Eventually, for $I_{dc} = 10 \mu\text{A}$ in Figure 7a, the phase margin is meager at $6.5^\circ$, causing the system to become unstable. This result is consistent with the analysis result shown in Figure 3, where the gain peaking occurs with $I_{dc} = 10 \mu\text{A}$. In the presence of $C_2$, the zero
is added before the gain crossover frequency. Thus, we can ensure enough phase margin with $C_2$.

For $I_{dc} = 10\, \mu A$ in Figure 7b, the phase margin becomes $135^\circ$. This result is also consistent with the analysis result shown in Figure 4, where the gain peaking is prevented on the presence of $C_2$ with $I_{dc} = 10\, \mu A$.

![Figure 7. Simulation of integrator’s loop gain.](image)

The frequency responses of the simulation and results of the experiment are shown in Figure 8. The experimental results strongly agree with the simulation results as well as the analytical results of Figure 4. The only difference is that the experimental results start to roll off at about $f_{pWP}$, slightly lower than the roll-off point of simulation results. There can be several reasons why this roll-off point in the measurement results is lower than that in the simulation results, such as additional input capacitance in the PCB layout and variations in the parameters of the circuit components. The major reason appears that the $f_{pWP}$ of the op-amp used in the actual implementation is less than the ideal values recorded in the datasheet or the simulation model parameters due to the process variation [16].

![Figure 8. Simulation and Experimental result.](image)
4. Conclusions

In this study, a CF-TIA with a transistor in the DC feedback loop is proposed and analyzed for high DC input dynamic range. Our system avoids the shortcoming of the conventional CF-TIA, whereby the thermal noise for the maximum DC input always present even in normal or low DC input cases. In the proposed circuit, the thermal noise is replaced by the shot noise varying with DC input. Thus, the proposed circuit can have the benefit in overall noise performance for normal or low DC inputs. Moreover, the proposed circuit compensates for the adverse effect of the parasitic capacitance of the transistor, which would otherwise lead the system to diverge with a positive real pole in the frequency response. The overall frequency response and design parameters, such as the cut-off frequency and attenuation ratio associated with system stability, are analyzed providing useful guidelines for the proposed CF-TIA design. Furthermore, a method that avoids gain peaking, regardless of the DC input, is introduced. The proposed CF-TIA and its analyses are validated by the excellent agreement between the analyses, simulation, and experimental results. The proposed circuit and its analyses are not limited to a specific application. They can be applied to various sensor measurements, such as emerging bio-sensors, nuclear science instrumentation, and optical receivers, and their CMOS chip design implementations.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Chen, R.Y.; Yang, Z.-Y. CMOS transimpedance amplifier for gigabit-per-second optical wireless communications. IEEE Trans. Circuits Syst. II Exp. Briefs 2016, 63, 418–422. [CrossRef]
2. Chuah, J.H.; Holburn, D. Design of low-noise high-gain cmos transimpedance amplifier for intelligent sensing of secondary electrons. IEEE Sens. J. 2015, 15, 5997–6004. [CrossRef]
3. Ciofi, C.; Crupi, F.; Pace, C.; Scandurra, G.; Patane, M. A new circuit topology for the realization of very low-noise wide-bandwidth transimpedance amplifier. IEEE Trans. Instrum. Meas. 2007, 56, 1626–1631. [CrossRef]
4. Ferrari, G.; Gozzini, F.; Molari, A.; Sampietro, M. Transimpedance amplifier for high sensitivity current measurements on nanodevices. IEEE J. Solid-State Circuits 2009, 44, 1609–1616. [CrossRef]
5. Serri, M.; Saeedi, S. Ultra-low-noise TIA topology for MEMS gyroscope readout. AEU Int. J. Electron. Commun. 2020, 118, 153145. [CrossRef]
6. Crescentini, M.; Bennati, M.; Carminati, M.; Tartagni, M. Noise limits of CMOS current interfaces for biosensors: A review. IEEE Trans. Biomed. Circuits Syst. 2014, 8, 278–292. [CrossRef] [PubMed]
7. Kim, D.; Goldstein, B.; Tang, W.; Sigworth, F.; Culurciello, J.E. Noise analysis and performance comparison of low current measurement systems for biomedical applications. IEEE Trans. Biomed. Circuits Syst. 2013, 7, 52–62.
8. Psychalinos, C.; Minaei, S.; Safari, L. Ultra low-power electronically tunable current-mode instrumentation amplifier for biomedical applications. AEU Int. J. Electron. Commun. 2020, 117, 153120. [CrossRef]
9. Kamrani, E.; Lesage, F.; Sawan, M. Low-noise, high-gain transimpedance amplifier integrated with siapd for low-intensity near-infrared light detection. IEEE Sens. J. 2014, 14, 258–269. [CrossRef]
10. Oliveira, L.B.; Leitao, C.M.; Silva, M.M. Noise performance of a regulated cascode transimpedance amplifier for radiation detectors. IEEE Trans. Circuits Syst. I Reg. Papers 2012, 59, 1841–1848. [CrossRef]
11. Wright, P.; Ozanyan, K.B.; Carey, S.J.; McCann, H. Design of high-performance photodiode receivers for optical tomography. IEEE Sens. J. 2005, 5, 281–288. [CrossRef]
12. Djekic, D.; Fantner, G.; Lips, K.; Ortman, M.; Anders, J. A 0.1% THD, 1 MΩ to 1 GΩ Tunable, Temperature-compensated transimpedance amplifier using a multi-element pseudo-resistor. IEEE J. Solid-State Circuits 2018, 53, 1913–1923. [CrossRef]
13. Rajabzadeh, M.; Djekic, D.; Haebler, M.; Becker, J.; Anders, J.; Ortman, M. Comparison Study of Integrated Potentiostats: Resistive-TIA, Capacitive-TIA, CT ΣΔ Modulator. In Proceedings of the 2018 IEEE International Symposium on Circuits and Systems (ISCAS 2018), Florence, Italy, 27–30 May 2018.
14. Herle, M.; Djekic, D.; Fantner, G.E.; Lips, K.; Ortmanns, M.; Anders, J. An integrator-differentiator tia using a multi-element pseudo-resistor in its dc servo loop for enhanced noise performance. In Proceedings of the IEEE European Solid State Circuits Conference (ESSCIRC 2018), Dresden, Germany, 3–6 September 2018; pp. 294–297.

15. Shahdoost, S.; Medi, A.; Saniei, N. Design of low-noise transimpedance amplifiers with capacitive feedback. Analog. Integr. Circuits Signal Process. 2016, 86, 233–240. [CrossRef]

16. Noh, J. Frequency response analysis and design rules for capacitive feedback transimpedance amplifier. arXiv 2020, arXiv:2004.08631.

17. Giusi, G.; Cannatà, G.; Scandurra, G.; Ciofi, C. Ultra-low-noise large bandwidth transimpedance amplifier. Int. J. Circ. Theor. Appl. 2015, 43, 1455–1473. [CrossRef]

18. Bhat, A. Stabilize Your Transimpedance Amplifier. 2012. Available online: https://pdfserv.maximintegrated.com/en/an/TUT5129.pdf (accessed on 1 February 2020).

© 2020 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).