Analysis and Design Considerations for Achieving the Fundamental Limits of Phase Noise in mmWave Oscillators With On-Chip MEMS Resonator

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Abstract—Very small electromechanical coupling coefficient in micro-electromechanical systems (MEMS) or acoustic resonators is quite a concern for oscillator performance, especially at mmWave frequencies. This small coefficient is the manifestation of the small ratio of motional capacitance to static capacitance in the resonators. This work provides a general solution to overcome the problem of relatively high static capacitance at mmWave frequencies and presents analysis and design techniques for achieving extremely low phase noise and a very high figure-of-merit (FoM) in an on-chip MEMS resonator based mmWave oscillator. The proposed analysis and techniques are validated with design and simulation of a 30 GHz oscillator with MEMS resonator having quality factor of 10,000 in 14 nm GF technology. Post layout simulation results show that it achieves a phase noise of $-132$ dBc/Hz and FoM of 217 dBc/Hz at offset of 1 MHz.

Index Terms—Oscillator, MEMS, mmwave, phase noise, RFT.

I. INTRODUCTION

INCREASING demands for smaller footprints for multi-channel integration (MCI) and reduced bill-of-material (BoM) in wireless communication technologies, such as 5G, seek low power radio frequency (RF) transceivers with monolithic resonators as compared to the conventional bulky off-chip quartz crystal or surface acoustic wave resonators, which are usually available in the form of a surface mount device. For MCI, where large arrays of transceivers are used on the same chip, local carrier generation in each transceiver is more desirable than distributing a common clock over entire chip in order to reduce the power for clock-routing. Power can be further saved if RF carriers are generated without using a phase lock loop (PLL) in each transceiver as shown in [1]. However, problem with PLL-less RF synthesis is the compromise in phase noise. With advancements in MEMS technologies and recently reported high-frequency, high-Q (> 1,000) resonators, [2]–[4], it seems possible to to build low phase noise PLL-free oscillators with on-chip MEMS resonators at mmWave frequencies.

Fig. 1 shows the Butterworth-Van Dyke model of a resonator, where $R_m$, $L_m$ and $C_m$ are termed as motional resistance, inductance and capacitance, respectively. $C_0$ is the static capacitance due to the device structure and geometry at the driving and sensing ports. Table I lists parameters of few resonators. Usually MEMS resonators have very low electromechanical coupling coefficient $k_t^2 = (C_m/C_0)$, which signifies a low efficiency of energy transfer between electrical and mechanical domains. At mmWave frequencies, $C_0$ exacerbates the problem of low $k_t^2$, which can potentially lead to higher phase noise and lower figure-of-merit (FoM) in MEMS resonator based oscillators.

In this work, towards the goal of building low phase noise mmWave oscillator with on-chip high-Q MEMS resonator, we present: 1) design details of 30 GHz, high-Q Resonant FinFET (RFT) MEMS resonator [4] (Section II), 2) design challenges due to $C_0$ and their general solutions (Sections III and IV), 3) theoretical analysis for fundamental limits of phase noise and FoM with and general design technique to achieve high FoM (Section V). To validate the proposed analysis and design approach, a 30 GHz oscillator is designed and simulated in 14-nm Global Foundry (GF) process (Section VI). While the important insights presented in this work are shown with RFT, they can be applied in general for building extremely low phase noise mmWave oscillator with any high-Q monolithic MEMS resonator.

Manuscript received May 12, 2020; revised August 28, 2020; accepted September 15, 2020. Date of publication October 12, 2020; date of current version March 26, 2021. This work was supported by DARPA MIDAS Program. This brief was recommended by Associate Editor L. A. B. G. Oliveira. (Corresponding author: Abhishek Srivastava.)

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSII.2020.3030074.

Digital Object Identifier 10.1109/TCSII.2020.3030074

1108 IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 68, NO. 4, APRIL 2021

Fig. 1. Butterworth Van Dyke model of MEMS resonator.

| TABLE I |
| --- |
| **Electrical Parameters of Different Resonators** |
| **Frequency** | **Q** | **$R_m$** | **$L_m$** | **$C_m$** | **$C_0$** | **$|X_{C_m}|$** | **$X_{C_m}$** |
| 45 MHz (Quartz)[5] | 10 | 15.5 Ω | 4.4 nH | 1.955 pF | 4 pF | 384 MHz | 110 MHz |
| 400 MHz (2A00)[6] | 1600 | 14 ft | 97.5 μH | 1.596 pF | 2.1 pF | 190 MHz | 13 MHz |
| 2.4 GHz (PAA005) [7] | 1000 | 1.04 ft | 107.2 μH | 3.87 pF | 1.2 pF | 51.3 MHz | 50 MHz |
| 30 GHz (RFT) [4] | 10,000 | 3.3 ft | 37.5 μH | 1.6 μF | 1.6 μF | 330 MHz | 330 MHz |

* off-chip bulky surface mount devices, †MEMS, This work
II. RFT : mmWAVE MEMS RESONATOR

Fig. 2(a) depicts the cross sectional view of a unit cell of the 30 GHz RFT MEMS resonator. An acoustic waveguide capable of sustaining mechanical modes of vibration is created by repeating this unit cell in the x-direction. In order to confine the waveguide mode of interest in the fin region, back end of Line metal layers are used as Bragg reflectors. Each unit cell consists of separate, 3-fin drive and sense MOSCAPs (= 2C₀) in which the gate and the shorted source-drain form the two plates of the capacitor as shown in Fig. 2(b). The drive MOSCAPs are used as capacitive transducers for actuation, which are biased in the accumulation region for maximizing the transduction efficiency. Fig. 2(c) shows the layout of the RFT resonator in 14 nm GF process, where M1 and M2 dimensions are kept narrow enough to avoid any slotting.

The mode shape of RFT is shown in Fig. 2(d) depicting the alternating polarity of mechanical stress in the x-direction at each fin. A finite element method (FEM) based simulation yields the x-stress in the fins of the sense MOSCAPs with the maximum occurring at the resonance frequency of 30.3 GHz as shown in Fig. 2(e). Capacitive sensing is employed at the sense MOSCAPs which are also biased in the accumulation region. To maximize the transduction efficiency of both the drive as well as sense transducers, C₀ needs to be as large as possible. C₀ is evaluated to be 16 fF through an AC simulation of the layout extracted netlist of the RFT device.

III. CHALLENGES IN OSCILLATOR DESIGN DUE TO C₀ AT mmWAVE FREQUENCIES

Electrical model of RFT is shown in Fig. 3(a). It exhibits two resonance modes - series and parallel. The series (fₛ) and parallel (fₚ) resonant frequencies are defined in Eq. (1) [7].

$$f_s = \frac{1}{2\pi \sqrt{L_m C_m}}; f_p = f_s \left(1 + \frac{C_m}{2C_0}\right)$$

(1)

Impedance (Zₐb) across the resonator and its phase (φₐb) can be given by the equations (2) and (3), respectively.

$$Z_{ab} = \frac{1 - \omega^2 L_m C_m}{-\omega^2 R_m C_m C_0 - \omega (C_m + C_0)}$$

(2)

As depicted in Fig. 3(a), oscillators with MEMS resonator are conventionally built with a negative resistance in a close loop at fₛ or fₚ, where φₐb = 0° and resonator behaves as a resistor [7]. However, at mmWave frequencies C₀ poses some challenges discussed below, which makes it impossible to build oscillators by directly applying the conventional methods.

A. Non-Zero Phase

From Eq. 3, by equating φₐb to 0°, following condition (4) is obtained.

$$C_0 = \frac{C_m (\omega^2 L_m C_m - 1)}{\omega^2 R_m 2 C_m^2 + (\omega^2 L_m C_m - 1)^2}$$

(4)

From (4) and RFT parameters shown in Table I, value of C₀ required at 30 GHz is about 1.6 fF. However, this small value of C₀ is not feasible as explained in Section II. Magnitude and phase of the 30 GHz RFT device are also plotted in Fig. 3(b), which shows that the impedance is capacitive near 30 GHz and the resonator does not provide 0° phase shift and therefore, it can not be directly used to build an oscillator.

B. Signal Loss at mmWave Frequencies

As shown in the Table I, while static capacitance C₀ reduces as frequency increases, Xₐb = \frac{1}{j\omega C_0} also reduces and becomes comparable to Rₘ for the 30 GHz resonator. Therefore at fₛ, about half of the signal will flow to ground through C₀, which will pose higher driving requirements to build the oscillator.

From the foregoing discussions, some fundamental questions arise for utilizing on-chip MEMS resonators at mmWave frequencies: 1) how to get 0° phase-shift, 2) how to avoid signal loss and 3) is there any advantage in phase noise and FoM as compared to conventional LC oscillators. These questions are answered in Sections IV and V.

IV. C₀ COMPENSATION

In order to make φₐb = 0° at the frequency of interest (fₒ), Im[Zₐb] should be 0 at fₒ. Since Zₐb is capacitive near 30 GHz (Fig. 3(b)), it can be cancelled with an inductor in series or shunt as shown in Figures 4(a) and 4(b), respectively. Phase and magnitude of the impedances of the two schemes are plotted in Figures 4(c) and 4(d), respectively, which show that φₐb = 0° near 30 GHz. At resonance,
scheme of Fig. 4(b) solves the problem of non-zero phase, however, it does not solve the problem of signal loss to ground through $C_0$. Therefore shunt inductor compensation (Fig. 4(a)) is a better choice to resonate out $C_0$, which solves both the problems.

The shunt inductor ($L_0$) compensated resonator (SLCR) can also be thought of as a parallel combination of series $R_m L_m C_m$ and the parallel $L_0 C_0$ branches as shown in Fig. 5(a) with an overall AC response shown in Fig. 5(b). Q-factor of on-chip inductors ($Q_{L_0}$) are usually limited ($<$ 30), therefore Fig. 5(a) exhibits a loaded Q-factor ($Q_L$). However, as shown in Fig. 5(b), the overall frequency response (green coloured) is governed by the high-Q motional branch near $f_r$, having a Q-factor of $Q_{RFC}$. As shown in Figures 5(c) and (d), it can be derived that $Q_L = Q_{RFC} + (R_m \times Q_{L_0})$. This expression suggests that if $R_m << R_p$, then $Q_L \approx Q_{RFC}$. From $R_m << R_p$, it implies that $R_m << Q_{L_0}^2 R_{L_0} \Rightarrow \frac{V_{OSC}}{I_{OSC}} < \frac{Q_{L_0}^2}{Q_{L_0}} \Rightarrow Q_{RFC} >> \frac{V_{OSC}}{I_{OSC}}$. Therefore, $Q_{RFC}$ will dominate if it is much larger than the term ($\frac{R_m}{Q_{L_0}}$). For example, if $\frac{C_0}{Q_{L_0}} = 10^4$ and $Q_{L_0} = 10$, $Q_{RFC}$ should be much larger than 1000. Eq. (5) shows $Q_L$ as a function of $Q_{RFC}$ for two values of $Q_{L_0}$, 10 and 20.

As shown in the figure, for lower values of $Q_{RFC}$ ($< 1000$), there is a significant effect of loading and $Q_L$ is low. However, for $Q_{RFC} > 1000$ loading reduces and for $Q_{RFC} > 2000$, $Q_L \approx Q_{RFC}$. Therefore, as long as $Q_{RFC} > 2000$, $L_0$ with inherent low $Q_{L_0}$ ($< 20$) will not cause any significant loading and extremely low phase noise oscillators can be built. Phase noise analysis and design technique for the oscillator are discussed in the following section.

V. PHASE NOISE ANALYSIS AND GENERAL DESIGN TECHNIQUE FOR MMWAVE OSCILLATOR

For phase noise analysis, the oscillator with SLCR can be considered as an LC feedback oscillator with the resonance characteristics as shown in Fig. 5(b). Leeson’s proportionality defined in Eq. (5) can be used to capture the phase noise ($\mathcal{L}(\Delta f)$) of the oscillator at an offset of $\Delta f$ with center frequency $f_0$ [8].

$$\mathcal{L}(\Delta f) = F \frac{4kT R_m}{V_{OSC}^2} \left( \frac{f_0}{2Q_L \Delta f} \right)^2$$

In Eq. (5), $F$ is the noise factor of oscillator, which is defined as the total oscillator phase noise normalized to phase noise due to the MEMS resonator loss ($R_m$), $k$ is the Boltzmann’s constant and $T$ is the temperature in Kelvin.

A. Intuitive Analysis

As discussed in previous section, $Q_L \approx Q_{RFC}$ (for $Q_{RFC} > 2000$). However, due to the parallel combination of impedances, SLCR experiences a reduced effective resistance ($R_{RES}$) at resonance given by Eq. (6).

$$R_{RES} = R_m (Q_{L_0}^2 \times R_{L_0})$$

(6)

For a fixed bias current ($I_{BIAS}$), reduced $R_{RES}$ decreases both the oscillation amplitude ($V_{OSC} \propto I_{BIAS} \times R_{RES}$) and the carrier power ($P_c \propto V_{OSC}^2$) in the current limited regime. From (5), $\mathcal{L}(\Delta f) \propto \frac{1}{Q_{RFC}^2}$, which implies that overall phase noise can improve if high $Q_L$ dominates the reduced $P_c$. For example, as compared to a parallel LC tank with $Q$-factor of 20, with the shunt inductor compensated resonator with $Q_L = 2000$, if $P_c$ reduces by 20 dB due to reduced $R_{RES}$, there will still be about 20 dB improvement in the phase noise. However, in order to get this advantage, the resonant frequency of $L_0 C_0$ branch should match closely to $f_r$. As shown in Fig. 6(a), if there is significant mismatch, then due to the higher loop gain, oscillator will work at frequency defined by $L_0 C_0$ tank with lower $Q_{L_0}$ and hence will have a poor phase noise. Whereas, if the two resonances are aligned (Fig. 6(b)) at $f_0$, $Q_L$ will be equal to $Q_{RFC}$ and very low phase noise will be obtained. It can be considered that, a reasonable matching will be achieved when $Q_L C_0$ tank’s frequency falls within $-10$ dB bandwidth (BW) of MEMS resonator. That is, $BW_{-10 dB} = 3 \times BW_{-3 dB} = 3 \times \frac{f_0}{Q_{RFC}}$. For example, considering $f_0 = 30$ GHz and $Q_{RFC} = 1000$,
expressions (7) and (8) and defining $\beta$ we try to maximize $QL_L$ definitions presented in [9] and [10] for an LC oscillator.

$\text{FRL}(\text{dBc/Hz})$ at 1 MHz offset near 30 GHz for different values of $QRFT$, Fig. 7. (a) Oscillator schematic, (b) simulation results showing phase noise $\approx 100$ MHz. Therefore, to get benefit of high $QRFT$, the $L_0C_0$ tank should achieve a resolution within 100 MHz near 30 GHz.

**B. Quantitative Analysis**

As shown in Fig. 6(c), the oscillator has 3 major noise sources- 1) $R_{L0}$, 2) $R_{LO}$ and 3) active part of the circuit providing negative conductance for sustained oscillations (Fig. 6(d)). The fundamental minimum noise factor ($F_{min}$) of the oscillator is given by Eq. (7).

$$F_{min} = 1 + F_{RLO} + F_{ACTIVE}$$  

where, $F_{RLO}$ and $F_{ACTIVE}$ are the noise factors due to $R_{LO}$ and non-linear active circuit, respectively. $F_{RLO}$ and $F_{ACTIVE}$ can be represented by expressions (8a) and (8b) extending the definitions presented in [9] and [10] for an LC oscillator.

$$F_{RLO} = \frac{R_{LO}}{R_{m}}$$  

$$F_{ACTIVE} = \gamma - \frac{R_{RES}}{R_{m}} + \frac{4}{g_{mbias}R_{m}}\left(\frac{R_{RES}}{R_{m}}\right)^2$$  

where, $g_{mbias}$ is the transconductance of the tail current source and $\gamma$ is the channel noise coefficient of FET. By combining expressions (7) and (8) and defining $\beta = \frac{R_{RES}}{R_{m}}$, we get Eq. (9) shown below.

$$F_{min} = 1 + \frac{R_{LO}}{R_{m}} + \gamma \beta + \gamma \frac{4}{g_{mbias}R_{m}}\beta^2$$  

Eq. (9) gives the fundamental minimum noise factor of inductively compensated MEMS resonator based mmWave oscillator. Eq. (9) along with Eq. (5) give important insights about the design choices for oscillator. In order to reduce the $F_{min}$, lower values of $R_{LO}$ and $\beta$ are desirable. However, it is also desirable to have highest possible $Q_L$ and hence to have maximum $Q_{LO} (= \frac{\omega_0}{2\pi\eta})$ to have least effect on $QRFT$ as discussed in Section IV. From Eq. (6), $\beta$ can be reduced by choosing lower value of $R_{LO}$, however with limited $Q_{LO}$, it is only possible if $L_{O}$ is reduced. This leads us to a general suggestion to use a lower $L_{O}$ with lower $R_{LO}$ with highest possible $Q_{LO}$. This suggestion is counter intuitive as in LC oscillators we try to maximize $L_{O}$ such that higher oscillation amplitude can be achieved and hence reduced phase noise.

As compared to LC oscillator, $F$ increases for the proposed shunt-inductor compensated MEMS based oscillator by a factor of $\frac{R_{LO}}{R_{m}}$, however, $F$ reduces considerably due to very high $Q_{L}$ of the resonator as discussed in Section IV. Theoretical minimum phase noise for 100% ideal oscillator ($F_{min} = 1$) can be estimated by considering noise due to $R_{m}$ only. For $R_{m} = 332 \Omega$, $QRFT = 10$ K, $V_{OSC} = 300$ mV, $I_{D} = 250$ pA, $R_{LO} = 4.8 \Omega$, $Q_{LO} = 10$, $\beta = 0.6$, the calculated phase noise is about $-159$ dBc/Hz at 1 MHz offset for $f_{O} = 30$ GHz. For validating the theoretical values, a cross-coupled oscillator is designed in 14 nm GF technology (Fig. 7(a)). From simulations, while keeping only the noise contribution of $R_{m}$ ON and with the same component values used in theoretical analysis, the phase noise is about $-157$ dBc/Hz for $QRFT = 10$ K, which matches closely with the theoretical value.

FoM of an oscillator can be defined as follows:

$$\text{FoM} = \frac{(f_0/\eta)^2}{L(\Delta f)P_{DC}} \times 10^{-3}$$  

where, $P_{DC}$ is the total DC power consumed by the oscillator in watt. From equations (5) and (10) FoM for the shunt-inductor compensated MEMS resonator based oscillator can be defined as follows:

$$\text{FoM} = \frac{Q_L^2}{K_{TF}} \times \frac{V_{OSC}^2}{R_{m}P_{DC}} \times 10^{-3}$$  

Defining the power dissipated at output as $P_{OUT} = \frac{V_{OSC}^2}{2R_{RES}}$ and oscillator efficiency as $\eta = \frac{P_{OUT}}{P_{DC}}$, Eq. (11) reduces to $\text{FoM} = 2\beta \eta \frac{Q_L^2}{K_{TF}} \times 10^{-3}$. Theoretical maximum FoM of 100% efficient oscillator ($\eta=1$), with noise-less $R_{m}$ and noise-less negative conductance (F=1), can be given by Eq. (12).

$$\text{FoM}_{max} = 176.8 + 20\log Q_L + 10\log (\beta) \text{ (dBc/Hz)}$$  

The value of $\text{FoM}_{max}$ is about 250 dBc/Hz for the values taken in the previous example to calculate theoretical minimum phase noise, which is about 50 dB more than that for the conventional LC oscillators [10].

**C. General Design Technique for mmWave Oscillator With On-Chip MEMS Resonator**

- Identify the value of shunt inductor ($L_{O}$) to compensate $C_0$ taking into account the routing parasitics and buffer load at the oscillator output node.
- In order to minimize $R_{LO}$ and $\beta$, use minimum value of $L_{O}$ with highest possible $Q_{LO}$ for $QRFT \geq 2000$. Use additional MIM cap ($C_{fix}$) parallel to $L_{O}$.
- Use capacitor bank with very small unit size ($\approx 1/f$) to add frequency tunability to exactly resonate out $C_0$ with $L_{O}$ at $f_{O}$ for the best phase noise performance.
- Use minimum gate length transistors for reduced area. For initial sizing of the active part, find minimum transconductance using $g_m = \frac{\eta}{4\pi^2f_{O}C_{ox}}$, current using $I_{bias} = \frac{V_{OSC}}{2Q_{RES}}$ and then calculate $W/L = (g_m)^2/2(I_{Bias\mu pC_{ox}})$.

**VI. IMPLEMENTATION AND SIMULATION RESULTS**

Figures 8(a) and (b) show the schematic and layout of the shunt-inductor compensated oscillator topology, respectively, in 14 nm Global Foundry (GF) 12LP technology, by following the analysis and design techniques presented in this work. An inductor of about 200 pF ($Q \approx 8$) is used from the PDK to realize $L_{O}$. As discussed in Section V-A, in order to achieve the resonance matching to get the highest loaded $Q_{L}$ near 30 GHz, a resolution within 100 MHz required. For
this, with $L_0 \approx 200 \text{ pF}$ and $C_0 \approx 250 \text{ fF}$, a capacitive resolution ($\Delta C$) of about 2 fF is required ($\frac{\Delta C}{C_0} = \left(\frac{f_0}{f_0 - f_\Delta}\right)^2 \approx 0.2$). A MOS capacitor bank with unit size of $C_sh (\approx 1/\text{f})$ with a fixed MIM capacitor ($C_{fix}$) of 10 fF is added in parallel with $L_0$. For $C_0$, nFET (W/L = 192nm/16nm) has been used with a gate capacitance of 0.97 fF (at TT) which has about ±5% variation across corners.

Post-layout simulation results (Figures 8(c) and (d)) show that phase noise of the proposed oscillator is about $-130 \text{ dBc/Hz}$ at an offset of 1 MHz for the carrier frequency of 30 GHz for $Q_{RF} = 10$, 0.004 across the process corners. Fig. 8(e) shows the sensitivity of phase noise with respect to the non-alignment of the two resonances. As shown in the Figure 8(e), for about 6 fF variation in output capacitance, effect of high $Q_L$ is present and phase noise is $<-120 \text{ dBc/Hz}$ at 1 MHz offset. The proposed circuit consumes about 2 mW power from 0.8 V supply and have a simulated FoM of 217 dBc/Hz, Table II shows comparison of the proposed MEMS oscillator with other reported works for > 15 GHz oscillation frequencies. Table II conveys the fact that as compared to the other LC oscillators near 30 GHz, with the analysis and design techniques presented in this work, it is possible to utilize a high-Q on-chip MEMS resonators at mmWave frequency and build extremely low phase noise oscillator with FoM > 200, while consuming much smaller die-area.

VII. CONCLUSION

In this work, insights to achieve fundamental limits of phase noise in a mmWave oscillator circuit with high-Q on-chip MEMS resonator with extremely small footprint have been presented with detailed analysis. Following the analysis, general oscillator design technique has been proposed while providing solutions to the problems due to the high static capacitance of high-Q on-chip MEMS resonator. To validate the proposed analysis and low phase noise design method, a 30 GHz oscillator has been designed in 14 nm GF 12LPP technology. Post layout simulations show that 30 GHz oscillator exhibits a simulated FoM of 217 dBc/Hz, and a phase noise of $-132 \text{ dBc/Hz}$ at 1 MHz offset near 30 GHz frequency, while consuming 2 mW power from 0.8 V supply.

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