Experimental Study on the Space Electrostatic Discharge Effect and the Single Event Effect of SRAM Devices for Satellites

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Abstract: Space Electrostatic Discharge Effect (SESD) and Single Event Effect (SEE) are two major space environmental factors that cause spacecraft failure. Previous studies have established that both can lead to soft errors such as upset of memory cells. An ESD generator and a pulsed laser experimental facility were used to test a low-power asynchronous timing monolithic SRAM. The characteristics of soft error number, single/multi-bit upsets, and supply current values were compared for similarities and differences. The test revealed that SEE-induced soft errors were mainly single-bit upsets (SBU), whereas SESD-induced soft errors were predominantly multi-bit upsets (MBU). Additionally, when soft errors occur in the circuits, the current of the power supply drops, which enables the device to be evaluated by monitoring the current value. This study provides experimental support for distinguishing device errors caused by these two effects, as well as references for further accurate identification of in-orbit faults and corresponding protection design.

Keywords: SRAM; SEE; SESD; soft errors; failure identification

1. Introduction

In the complex radiation environment of space, high-energy particles produce a variety of environmental effects on spacecraft, resulting in spacecraft anomalies, of which the Space Electrostatic Discharge effect (SESD) and Single Event Effect (SEE) account for a large proportion [1–3]. NASA, Marshall Flight Center (MSFC), and AEROSPACE have investigated 114, 299, and 476 spacecraft anomalies [2–4] induced by the space environment in 1996, 1999, and 2009, respectively. According to the results, the percentage of anomalies caused by SESD and SEE were 33% and 38.7%, 54.2% and 28.4%, and 25% and 46%, respectively. The demand for highly integrated, high performance, low power, small size and low mass circuit devices on space exploration satellites and vehicles is growing rapidly. At the same time, they must also possess a very high level of radiation resistance in order to guarantee safety in flight. SRAM is the core element of the spacecraft and is responsible for data processing and storage. Potential SESD and SEE may cause it to malfunction in a variety of ways, even affecting the normal operation of the entire system.

Although researchers have studied the performance and physical mechanisms of SESD and SEE widely, their effects on spacecraft are often confused with each other. Several factors contribute to this difficulty. First of all, the spacecraft anomaly problem is very complex, involving a wide range of engineering and technical aspects. As well, anomalies occurring in space are more difficult to reproduce and study in depth through experiments on the ground. Secondly, traditional SEE research is primarily concerned with the effects of the space radiation environment on spacecraft circuits and devices, whereas traditional SESD research is primarily concerned with the effects of space plasma and high-energy electron storms on spacecraft materials and structures. This has resulted in the formation of two independent international research groups. Nuclear and Space Radiation Effects Conference (NSREC) and Radiation Effects on Devices and Systems Conference...
(RADECS) communicate the former, while the latter is primarily communicated through the Spacecraft Charging Technology Conference (SCTC), with very little joint research taking place between the two groups. Additionally, research on the effects of SESD on devices and circuits is quite limited, in comparison to the well-documented effects of SEE, which limits a comparative study of characteristics, patterns, and mechanisms. Over the past several years, the National Space Science Center has conducted preliminary experiments on errors and anomalies associated with these two effects in digital circuits, such as operational amplifiers (OPA), static random-access memories (SRAM), and field programmable gate arrays (FPGA). It was discovered that both SEE and SESD can lead to abnormal transient pulse signals, while the upset of the memory bit 0/1 state of commercial SRAM devices was examined. However, the characteristics of memory devices with radiation hardening for astronautics have not been studied.

From an interdisciplinary perspective, this study investigated the errors generated by SESD and SEE on a SRAM device with EDAC (Error Detection And Correction) redundancy design for spacecraft. First, an experiment was conducted to determine the relationship between soft error number and pulsed laser energy and electrostatic discharge voltage. According to the results, the number of errors is positively correlated with the energy of the external excitation source. Furthermore, in order to gain a more comprehensive understanding of the intrinsic mechanisms of errors caused by SESD and SEE, a statistical analysis of the types of errors induced by each was conducted. It was evident that SEE leads to single-bit upsets (SBU) predominantly, while SESD results in mostly multi-bit upsets (MBU). In addition, we investigated for the first time the relationship between the soft errors induced by these two effects and the supply current. A memory bit flip could be detected by monitoring the level of supply current in the device.

The remainder of this paper is organized as follows: Section 2 provides an overview of the experimental setup; Section 3 compares the characteristics of soft error number, error types, and the response of supply currents to memory bit flips; and Section 4 summarizes the study’s findings.

2. Experimental Setup

2.1. Device under Test

This study focused on JM001, a low-power asynchronous timing monolithic SRAM with a storage capacity of 8 K × 8 bits. This device consisted of an address input buffer circuit, a row decoder circuit, a column decoder circuit, a data input/output buffer circuit, a small signal readout amplifier circuit, a data output driver circuit, a logic control module, and a 256 × 256-bit memory cell array. It was powered by a single 5 V supply, with a read-write cycle of 30 ns. A schematic block diagram of the device is shown in Figure 1.

![Schematic block diagram of JM001.](image)
When the SRAM device is working normally, the serial port sends data periodically, but if an error occurs, it sends error data continuously. A description of the serial port data of the host software is shown in Figure 2.

Figure 2. Data description chart on PC software.

- (3) 0000 indicates the read error count;
- (8) 000000 indicates the address of error data when an error occurs;
- (10) 00 indicates the error data when an error occurs;
- (12) 00 indicates the expected correct data.

2.2. Test Facilities

For the Single Event Effect, the experiment was conducted using the pulsed laser single event effect simulation test facility of the National Space Science Center of the Chinese Academy of Sciences, and the main technical parameters of which are shown in Table 1.

| Item                          | Parameter                     |
|-------------------------------|-------------------------------|
| Irradiation Source            | Nd: YAG laser                 |
| Laser Wavelength              | 1.064 µm                      |
| Spot Diameter                 | 3~4 µm                        |
| Pulse Repetition Frequency    | 1.50 kHz                      |
| Minimum Scanning Step         | 0.6 µm                        |
| Equivalent LET                | 0.1~200 MeV·cm²/mg            |

Figure 3 illustrates the block diagram of the experimental setup. The experimental circuit board with the experimental device was mounted on a three-dimensional moving table, and the movement and position of the three-dimensional moving table were controlled by computer programming. The laser generated by the pulsed laser irradiated the experimental sample, after the optics had been adjusted and the objective lens had been focused. A CCD camera provided images of the sample’s surface and the laser spot on the computer display. A DC power was supplied to the sample, and the output of the supporting circuit was continuously monitored.

Figure 3. Schematic block diagram of pulsed laser irradiation test facility.
For the Space Electrostatic Discharge Effect, an ESD generator manufactured by SANKI, model SKS-0220G, was used, which fully complied with the requirements of the IEC61000-4-2 standard in terms of performance. With an adjustable voltage range of ±500 V to ±20 kV, energy storage capacitance of 150 pF and discharge resistance of 330 Ω, the ESD generator met the most severe electrostatic discharge voltage requirement in the standard. Figure 4 shows the current waveform of this ESD generator, which can be compared to the typical space discharge current waveform.

![Figure 4. Current pulse waveform of ESD generator.](image)

The experimental setup is depicted in Figure 5. The device under test (DUT) was placed horizontally on an insulated table, powered by a DC regulated power supply. Data was written and received through the serial port by a host computer. The radiation field method recommended by NASA-HDBK-4002A [5] was used for this experiment, and the ESD generator was used to discharge on a 10 cm × 10 cm aluminum plate grounded by a cable at one end.

![Figure 5. Schematic diagram of space electrostatic discharge test setting.](image)
3. Results and Discussions

3.1. Soft Error Number

Data (read error count) from the host software was extracted, and the data points were plotted as a curve of soft error number with laser energy, as shown in Figure 6. When the pulsed laser energy is 814 pJ (corresponding to the LET value [6–8] of 37 MeV·cm²/mg), soft errors due to SEE start to be generated, so the SEU threshold for this SRAM device is 814 pJ (±81 pJ). With increasing laser energy, the number of errors increases. When the pulsed laser energy reaches 1651 pJ (corresponding to the LET value of 75 MeV·cm²/mg), the number of errors is 11125 bits.

![Figure 6. Error number curve with pulsed laser energy.](image)

The variation curve between the number of soft errors and the electrostatic discharge voltage is shown in Figure 7. With the threshold of 12.5 kV, discharge voltages below 12.5 kV do not cause soft errors in the device. In the range of 12.5 kV to 20 kV, the number of soft errors increases with the increase of discharge voltage. In particular, the slope of the error number growth curve increases significantly between 17 kV and 20 kV.

![Figure 7. Error number curve with ESD voltage.](image)

According to Figure 7, when the discharge voltage is less than or equal to 12 kV, the number of errors in the detection system is not accumulated, but the character segment recording of the error address is recorded. The SEE experiment did not experience a
similar phenomenon. To investigate the issue, the read-only mode of operation of this SRAM device only recorded errors when a read error was detected (3 reads, $\geq 2$ mistakes), while the SEU error count accumulated. The set access time for the read/write circuit was approximately 30 nanoseconds, and the pulse width of the discharge pulse was also 30 nanoseconds. Thus, if the discharge pulse caused a functional failure of the read/write circuit, it would only last for one read-only data period. Only if a real error occurred in the SRAM storage data, would it trigger SEU data accumulation according to the three-check judgment scheme [9,10]. Therefore, it could be concluded that the read/write circuit of this SRAM device is more sensitive to discharge pulses than the memory circuit.

3.2. Error Types

During the experiments, the upper computer software generated a large amount of error data, and the hexadecimal digits of the write data and those of the read data were binary converted. In this way, it would be possible to compare the number of erroneous bits in each piece of data. A single byte error on an address bit is regarded as an SBU. When multiple byte errors occur at the same time for an address bit, we refer to this event as an MBU. Figure 8 summarizes the statistics of SBU and MBU.

![Figure 8. Percentage of error types (SBU/MBU) of SEE and SESD. (a) Percentage of SBU and MBU with the variation of pulsed laser energy. (b) Percentage of SBU and MBU with the variation of discharge voltage.](image-url)
Figure 8a illustrates that in the SEE experiment, the vast majority of errors were SBU, and a small number of errors were MBU. Using transistor T1 illustrated in Figure 9 as an example, when a single particle is incident on the drain, the ionizing charge generated is collected by the reverse biased PN junctions formed in the drain and trap areas due to the electric field in the space charge region, resulting in transient currents. Transient currents can alter the potential of the storage node, thereby upsetting its logic state. Multi-bit upsets can occur when laser traces ionize between multiple storage cells and generate a large number of charges. Due to the EDAC redundant design of this SRAM, MBU are restricted to generate. Therefore, the SEE appears to produce errors primarily due to SBU.

Figure 9. Schematic diagram of SRAM structure with SEE and SESD.

In addition, from Figure 8b, it is evident that most of the errors that occur during the SESD experiment are caused by multi-bit upsets. Discharge pulses couple the power supply pin of the device to form transient voltage pulses at the power and ground terminals. The transient pulses are then transmitted through the internal power supply circuit of the device to the power input of the internal memory circuit. If the core supply voltage changes instantly from the normal operating voltage to the lowest negative value, it is very easy for the power supply track of the device to collapse. In other words, when the power supply voltage value is lower than the minimum bias voltage required to maintain the data of the memory cell, the stored information of the memory cell will be erroneous. In SRAMs, the internal power supply circuit supplies power to multiple storage arrays, which causes multiple storage bit errors when track collapse [11,12] occurs in the internal power supply. It is indicated that the radiation-hardening design for SEE was no longer applicable to SESD.

3.3. Supply Current Values

During both the SEE and SESD experiments, the supply current of this SRAM showed small periodic fluctuations due to factors such as leakage current and power leakage [13–15] in the circuit. The comparison between the number of errors and the supply current (Figure 10) indicated that when a memory cell is flipped, the supply current drops significantly.
Combined with the structural characteristics of SRAM, the entire read/write processes require pre-charging of the bit lines, which increases the consumption of power. As long as the SRAM functions properly, the circuit performs a read-only operation, and the current drops uniformly. According to the predefined experimental mechanism, if an error occurs, the device automatically enters a refresh state to re-write the correct data to the incorrect address and identify it. In other words, once an error has been detected, the circuit immediately performs a write operation. At that time, the power consumption and leakage current of the read/write state appear superimposed, and the current appears to decrease at a higher magnitude than before. This means that the current characteristics can be used to measure the appearance of errors, and the greater the current decline, the greater the number of errors produced.

As shown in Figure 11, the minimum value of the collected current at the Vcc terminal is plotted as a line graph with laser energy and discharge voltage. The overall trend indicates that the higher the external sources of stimulation, the greater the decrease in the value of the current at the Vcc end. This could be explained by the fact that as the discharge voltage increases, so do the number of errors and the number of multi-bit upsets, and thus the number of bits that need to be refreshed. As a result, the read/write current consumption and leakage current in the circuit increase, causing the lowest current value at the Vcc terminal to display a decreasing trend over time.
Figure 11. The curve of the lowest current value at Vcc port. (a) The curve of minimum current with the variation of pulsed laser energy. (b) The curve of minimum current with the variation of discharge voltage.

4. Conclusions

Due to the differences in mechanisms causing in-orbit failure of a spacecraft by the Space Electrostatic Discharge Effect and the Single Event Effect, as well as the principal mechanisms by which the effects are brought about on the device, these effects may be simulated by an ESD generator and a pulsed laser facility, respectively. In this study, experimental simulations of the Space Electrostatic Discharge Effect and the Single Event Effect were conducted. The following conclusions were obtained by comparing the similarities and differences of the two effects on SRAM devices:

1. In both tests, the number of soft errors within the SRAM device increases as the discharge voltage and pulsed laser energy increase. This SRAM device has an upset threshold of 814 pJ for SEE and an upset threshold of 12.5 kV for SESD;
2. In contrast, SEE causes essentially single-bit upsets (SBU), whereas SESD produces mostly multi-bit upsets (MBU). Apparently, the radiation-hardening design for SEE is no longer applicable to SESD;
3. The soft error in the circuit is associated with a drop in supply current, so it can be detected by monitoring the current value to determine whether it is abnormal.

The findings presented above provide experimental evidence for screening SESD and SEE, as well as guidelines for subsequent protection design. Further work is required to
complement the simulation and theoretical analyses for the specific details of the distinction and the deep-seated mechanism study.

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