Vanadium gate-controlled Josephson half-wave nanorectifier

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Recently, the possibility to tune the critical current of conventional metallic superconductors via electrostatic gating was shown in wires, Josephson weak-links and superconductor-normal metal-superconductor junctions. Here we exploit such a technique to demonstrate a gate-controlled vanadium-based Dayem nano-bridge operated as a half-wave rectifier at 3 K. Our devices exploit the gate-driven modulation of the critical current of the Josephson junction, and the resulting steep variation of its normal-state resistance, to convert an AC signal applied to the gate electrode into a DC one across the junction. All-metallic superconducting gated rectifiers could provide the enabling technology to realize tunable photon detectors and diodes useful for superconducting electronics circuitry.

In the last few years, the possibility to suppress the critical current in conventional Bardeen-Cooper-Schrieffer (BCS) superconducting wires1, Dayem bridge (DB) Josephson junctions (JJ)2–5 and superconductor-normal metal-superconductor weak-links6 via electrostatic gating was demonstrated7. Such a technique is at the basis of a class of innovative all-metallic superconducting Josephson transistors, where a gate electrode is used to modulate down to full suppression the critical current of a superconducting channel, in analogy to what occurs for the current in standard gated semiconductor transistors. Furthermore, the impact of the electrostatic gating on the macroscopic phase, and on the phase slip dynamics was proved in superconducting quantum interference devices (SQUIDs)8 and in gated titanium DBs, respectively9. So far, the microscopic origin of the gating effect in metallic superconductors is still unclear, and the debate in the search of a satisfactory explanation for the aforementioned phenomenology has just started.4,10,11 Yet, several technological implementations based on gated superconducting transistors for both classical and quantum computation architectures were proposed1 til now, and promise new paradigms to realize innovative superconducting circuits. These are expected to benefit from operation frequencies close to those typical of rapid single flux quantum devices (up to ~750 GHz)12, but in a voltage-driven fashion which would provide a direct and convenient interface with complementary metal-oxide technology (CMOS).

Here, we demonstrate a vanadium (V) Josephson half-wave rectifier based on a scheme recently proposed5 which exploits the strong non-linearity of the resistance (R) of a gated superconducting nanotransistor vs gate voltage (Vg). Such a device might form the rectifying core of a photon sensor operating at high frequencies, relevant, for instance, for cosmological applications11, or could be exploited as a comparator14 to be used in all-superconducting digital electronic circuits7. The potentially-high operation frequency, the ease of fabrication and the simple geometry of our nanodevices makes them attractive as an effective alternative to conventional all-semiconductor15 and semiconductor-superconductor hybrid16–18 field-effect-transistor-based technologies.19,20 Below, we focus on the manipulation of the dissipative response of the V-based Josephson weak-link via the application of a voltage to a gate capacitively-coupled to the junction, and show its time-

![FIG. 1. (a) False-color scanning electron micrograph of a typical gate-controlled vanadium JJ nanotransistor. The DB constriction (light blue) is current biased, and the voltage drop is measured in a 4-wire configuration. The electrostatic field is applied via the gate electrode (orange). (b) Back and forth current I vs voltage V characteristics of a representative device measured at different bath temperatures from 2.0 K to 3.8 K. The curves are horizontally offset for clarity. The inset shows the 4-wire lock-in measurement (with biasing current I ≃ 15 nA) of the R vs T characteristic of the junction. The superconducting transition occurs at IC ≃ 3.6 K. (c) Evolution of the critical current IC (light blue dots) and retrapping current IR (yellow dots) vs bath temperature T. The black dashed line represents the best fit of IC(T) with the Bardeen’s theory, which yields IC = (2.2 ± 0.1) mA and TC/tr = (3.6 ± 0.07) K as fitting parameters.](image-url)
resolved response to periodic square-wave and sinusoidal signals applied to the gate thereby leading to electric rectification.

Our device consists of a planar 60-nm-tick, 160-nm-long, 90-nm-wide V Dayem bridge JJ with a 70-nm-apart, 120-nm-wide side-gate aligned to the constriction. The device fabrication was performed on a silicon oxide substrate with a single-step electron beam lithography followed by vanadium deposition performed at a rate of 0.36 nm/s in an ultra-high vacuum electron-beam evaporator with a base pressure of $\sim 10^{-11}$ Torr\textsuperscript{21-27}. Figure 1(a) shows the false color scanning electron micrograph of a representative V JJ transistor along with the 4-wire biasing scheme used for the low-temperature current vs voltage $(I - V)$ characterization of the devices performed in a filtered cryogen-free $^3$He-$^4$He dilution refrigerator.

For temperatures below $\sim 3.5$ K, the V JJ is superconducting and exhibit, at 2 K, a critical current $I_{C}$ of $\sim 1.42$ mA, a re trapping current $I_{R} \sim 380$ $\mu$A, and a normal-state resistance $R_{N}$ of around $\sim 110$ $\Omega$. The forward and backward current $I$ vs $V$ characteristics for temperatures $T$ ranging from 2.0 K to 3.8 K are shown in Fig. 1(b), where the full evolution of $I_{C}$ as a function of $T$ is highlighted by the grey area. The hysteretic behaviour of the curves stems from quasiparticle over-heating when the junction switches from the superconducting to the normal state\textsuperscript{28,29}. Moreover, the additional features present on the $I - V$ characteristics at higher current are likely to be related to the switching of the DB banks to the normal state. The decay of both $I_{S}$ and $I_{R}$ with the temperature is shown in Fig. 1(c), where the black dashed line represents a fit of the $I_{C}$ vs $T$ characteristic performed with the Bardeen’s equation: $I_{C}(T) = I_{C}^{0} \left[ 1 - \left( \frac{T}{T_{C}^{0}} \right) \right]^{2}$, where $I_{C}^{0}$ is the zero-temperature critical current, and $T_{C}$ is the DB critical temperature. The fitting procedure yielded $I_{C}^{0} = (2.2 \pm 0.1)$ mA and $T_{C}^{0} = (3.62 \pm 0.07)$ K. The latter value is in agreement with the experimental critical temperature determined from the 4-wire lock-in measurement of the junction resistance vs bath temperature $T$, as shown in the inset of Fig. 1(b).

The preliminary characterization of the gating effect on $I_{C}$ and $R$ was carried out by acquiring the forward and backward $I - V$ characteristics of a representative vanadium DB as function of the voltage applied to the gate electrode, $V_{G}$. Figure 2(a) displays the $I_{C}(V_{G})$ characteristics extracted from the $I - V$ acquired for several bath temperatures. The modulation of $I_{C}$ is almost symmetric for $V_{G} \rightarrow -V_{G}$, and the gate effect persists up to $\sim 3.3$ K, i.e., $\sim 0.9I_{C}$. We note that a sharper suppression of $I_{C}$ for positive values of $V_{G}$ seems to be in contrast to a possible field emitted electrons-driven effect, since electrons extraction from the gate (occurring at negative gate bias) is, in principle, more effective than that from the DB (occurring at positive gate bias) owing to the substantial asymmetry of the device geometry.

Let us now describe further the transport properties of the transistor by focusing on the behavior of the device resistance $R$ under the action of the electric field. The steep modulation of the critical current yields, at constant current bias $I_{B}$, an analogous modulation of the resistance of the device. Figure 2(b) displays the evolution of $R$ as a function of the gate voltage $V_{G}$ for several values of bias current $I_{B}$. We note that $R$ remains almost equal to 0 for $V_{G}$ values such that $I_{C}(V_{G}) > I_{B}$. Then, for higher gate voltage, the resistance jumps to finite values due to the gate-driven superconducting-to-normal state transition of the device. Finally, $R$ increases with $V_{G}$, probably owing to the enlargement of the normal-state region within the junction\textsuperscript{2}. In particular, for $I_{B} > 30$ $\mu$A, $R$ exhibits a linear dependence on $V_{G}$. Moreover, also the steepness of the resistance jump is a function of $I_{B}$, as customarily described by the figure of merit of the resistance derivative with respect to the gate voltage $(dR/dV_{G})$, which is shown in Fig. 2(c). The amplitude of the differential resistance peaks, corresponding to the transition to the normal state, increases with $I_{B}$ reaching the maximum value of $\sim 30$ $\Omega$/V at $I_{B} = 150$ $\mu$A. Furthermore, the peak center shifts towards lower $V_{G}$ values as the bias current is increased.

The strong non linearity typical of the $R(V_{G})$ characteristics, provided by the transition to the dissipative regime,
could be conveniently exploited to implement a superconducting half-wave rectifier converting an AC signal applied to the gate into a DC one across the DB. Such a mechanism, recently proposed for Nb gate-controlled transistors\textsuperscript{3}, could allow to realize, for instance, a radiation detector in which the AC electric field collected by an antenna coupled to the gate electrode would be rectified, thereby leading to an amplified non-zero average signal. The gain of such a device can be defined as the ratio \( g = \frac{V_{\text{out}}}{V_{\text{in}}} \), where \( V_{\text{in}} \) and \( V_{\text{out}} \) are the peak-to-peak amplitudes of the signal applied to the gate and the voltage drop across the DB, respectively. The quantity \( g \) can be calculated through the relation \( g = R(V_G)I_B/\sigma \), where \( R(V_G)I_B = V_{\text{out}} \) is the product of the gate dependent DB resistance \( R \) and the current bias \( I_B \), while \( \sigma / I = V_{\text{in}} \) is given by the ratio of the typical width \( \sigma \) of the switching current probability distribution for gate-driven superconducting field-effect transistors\textsuperscript{3} and the transconductance \( t = dI_C/dV_G \). For V-based devices, \( g \) is expected to reach values as high as \( \sim 7 \) with a typical power dissipation of \( \sim 40 \) nW. Our V DB nanotransistor shows gain performance similar to cryogenic semiconductor devices\textsuperscript{30,31} with a reduction in power consumption of about three orders of magnitude. Noteworthy, a series of \( N \) rectifiers can be realized by feeding the gate electrode of the \( n^{th} \) rectifier with the output voltage of the \((n-1)^{th}\) one, and resulting in a total gain equal to \( g^N \).

In the following, we shall focus on the time-resolved investigation of the response of V Josephson transistors to AC square-wave and sinusoidal gate signals. The measurements setup, comprising an input/output analog-to-digital/digital-to-analog converter (ADC/DAC) board for the generation and the acquisition of time-resolved alternate current and voltage signal, is depicted in Fig. 3(a). The voltage drop \( V(t) \) across the current-biased DB was measured as a function of a time dependent gate voltage \( V_G(t) \). In this configuration, when \( I_C[V_G(t)] < I_B \) the junction is in the normal state and a finite voltage drop is built across the DB (high-state). By contrast, when \( I_C[V_G(t)] > I_B \), the DB is superconducting, and \( V \sim 0 \) (low-state). The response of the device to a transistor-transistor-logic (TTL) like square-wave excitation was probed by feeding the gate with a signal consisting of a \( V_{\text{DC}} = 10 \) V DC bias added to a \( V_{\text{AC}} = 5 \) V square-wave signal with frequencies up to \( \sim 50 \) Hz, as shown in Fig. 3(c). The voltage drop in the high- and low-state for some representative values of \( I_B \) is shown in Fig. 3(d) as pairs of points with the same color, superimposed on the \( I - V \) characteristics taken at selected values of \( V_G \). As displayed in Fig. 3(d), the voltage drop across the junction preserves the shape of the input signal. On this regard, we emphasize that in our experiments the maximum operation frequency is limited by the low-pass filtering stages of the electrical lines of our setup. At present time, the timescale of gate-driven superconducting phase transition is unknown, nonetheless the ultimate cut-off frequency of the V gate-controllable rectifiers could be estimated to be at most \( 2\Delta / h \sim 265 \) GHz, where \( h \) is the Planck’s constant, a value which is comparable to state-of-art hybrid and CMOS field-effect transistors\textsuperscript{15,32,33}.

The response of the DB to a sinusoidal gate voltage excitation was measured by applying to the gate an AC sine signal \( V_{\text{AC}} \) with peak-to-peak amplitudes ranging from 1 to 3.5 V added to a \( V_{\text{DC}} = 11 \) V DC bias voltage. This results in a periodic sinusoidal oscillation of the critical current \( I_C \) above and below \( I_B \), producing a gate-driven periodic modulation of the device resistance. The voltage drop across the DB as a function of \( I_B \) and \( V_G \) is displayed in Fig. 4(a). We note that by

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**FIG. 3.** (a) Scheme of time-resolved measurements of the 4-wire voltage drop \( V(t) \) across the junction at constant current bias \( I_B \) vs DC (black dotted line) + AC (square-wave green line) gate voltage. The gate polarization signal is compared with the \( I_C \) vs \( V_G \) curve to highlight the dynamic working range of the system. (b) Voltage \( V \) vs current \( I \) characteristics for selected values of gate voltage \( V_G \). The dot pairs show the working points of the system for different values of the bias current \( I_B = 18, 37, 71 \) µA. (c) Evolution of the gate voltage vs time. The signal was obtained by summing a DC voltage \( V_{\text{DC}} = 10 \) V and an AC square-wave voltage with amplitude \( V_{\text{AC}} = 5 \) V. (d) Time-resolved voltage drop across the DB for selected values of the current bias. Dashed lines shows the corresponding working points in panel (b). These measurements were performed at \( T_B = 3 \) K.
For higher values of $V_G$, i.e., when $I_C(V_G(t)) < I_B$, the voltage drop increases due to the gate-driven evolution of the DB resistance, which eventually will saturate at the asymptotic value of the normal-state resistance. Figure 4(c) shows the voltage drop of the DB as a function of time, in response to the gate signal reported in Fig. 4(b). To clarify the response of the system to such excitation, we highlight in Figs. 4(a,b) three points corresponding to the minimum of the $V_G(t)$ signal (light green dot), the switching point (red dot), and the maximum of $V_G(t)$ (dark green dot). The value of the biasing current was set to $I_B = 72 \mu A$ in order to take advantage of both the sharp normal-to-superconductor transition and the linear relation between $R$ and $V_G$ for $I_B > I_C$. The latter feature allows to preserve the sinusoidal shape in the output voltage when the JJ is in the resistive state, as shown in Figs. 4(c,d,e) for different values of $V_{AC}$. Indeed, although the output signal resembles that of a conventional half-wave rectifier, it is worth to emphasize that, in our systems, it is possible to tune the rectification threshold $V_C^*$ by changing both $I_B$ and $V_{DC}$.

In summary, we have demonstrated a half-wave rectifier based on a gated vanadium Dayem nano-bridge Josephson transistor operating at 3 K. We showed the time-resolved response of our device to square-wave and sinusoidal gate signals, demonstrating the ability to convert an AC excitation into a DC one, and with a gain which is expected to obtain a value close to 7 at a power consumption of \( \sim 40 \) nW. The performance of the V DB represents a major improvement in energy efficiency compared to conventional cryogenic semiconductor technology.\(^{30,31}\) V-based gate-controllable Josephson rectifiers could represent a breakthrough and a possible enabling technology to implement innovative all-metallic superconducting photon detectors\(^{34-36}\) based on gating as well as electric diodes suitable for superconducting digital\(^{37}\) and quantum electronics\(^{38,39}\) circuitry.

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### Table 1: Parameters of the Junctions

| Parameter | Value |
|-----------|-------|
| $I_B$     | $72 \mu A$ |
| $V_{DC}$  | $11 V$ |
| $V_{AC}$  | $3.5 V$, $1.5 V$, $1.0 V$ |
| $V_{G}$   | $9.0$, $10.5$, $12.0$, $13.5$ V |
| $I_C$     | $\sim 7$ A |

### Figure 4

- **(a)** Density plot of the voltage drop across the junction as a function of the gate voltage ($x$ axis) and current bias ($y$ axis). From left to right, the three points represent the minimum zero resistance gate voltage value (light green), the transition between the superconducting and the normal state (red) and the maximum of both gate voltage and voltage drop (dark green) respectively. The dashed red curve highlights the critical current $I_C$ as a function of the gate voltage $V_G$.
- **(b)** Time evolution of the gate voltage. The signal was obtained adding a DC voltage $V_{DC} = 11 V$ and an AC sine wave voltage $V_{AC}$. The three dots highlight the working points described in panel (a).
- **(c)**, **(d)**, **(e)** Time resolved voltage drop across the DB for, respectively, $V_{AC} = 3.5$, $1.5$, $1.0$ V. The colormap is the same of panel (a). All these measurements were carried out at $T_B = 3 K$. 

Choosing $I_B$ and $V_{DC}$ [see Fig. 4(a)], it is possible to set a working point for the rectifier, which determines the intensity and the shape of the resulting output voltage signal through the evolution of the super-to-normal switching point [red dashed line in Fig. 4(a)], and through the dependence of the device resistance on the gate voltage (see also Ref.\(^2\)). Indeed, the system lies in the zero voltage state for $I_C(V_G(t)) > I_B$, and a voltage drop across the junction occurs when $I_C(V_G(t)) \approx I_B$. 

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