1. Introduction

Electronics devices such as the smartphone are now becoming higher in performance, multifunctional, and miniaturized for convenient access to internet services. High-speed operation is thus necessary for enhanced performance of such electronics devices.[1, 2] In terms of assembly technologies, flip-chip bonding (FCB) has been widely adopted in advanced packaging systems for high-speed operation rather than wire bonding.[3] The chip size for future LSI devices is generally expected to become larger, and therefore the stress in the chip after FCB will become a critical issue.[4]

There have been many reports to date on the residual stress after FCB.[5–9] Thermal expansion mismatch among the silicon chip, solder bumps, and substrate is the cause of this residual stress. This causes a local strain distribution in the package system that gives rise to a performance deterioration, such as the degradation of cold joints, electronic circuit damage from package cracks, and solder cracking from warpage. Test element group (TEG) chips with piezoresistive sensors are typically used to evaluate the residual stress in a package.[10–19] However, measurement of the local stress distribution in a TEG chip is limited because of the sensor and bump layout.

On the other hand, stress simulation using the finite element method (FEM) can be used to predict the chip stress.[20–22] The effect of a capillary underfill (CUF) or a non-conductive film (NCF) on FCB is generally evaluated using the FEM. However, the viscoelastic properties of a CUF and an NCF must be investigated thoroughly to obtain the correct FEM simulation results.[23–29] Thermosetting resins for the CUF and NCF typically exhibit nonlinear elasticity over the glass transition temperature $T_g$, the FEM can’t simulate nonlinear elastic properties over $T_g$ of thermosetting resin with high accuracy. Therefore, the simulation results are often different to the exper-
imental results. As such, a new and easier evaluation method to replace FEM simulation is required for resin design and improvement of the package performance.

The residual stress in a wire-bonded TEG chip with a piezoresistive sensor after molding, and compared it with FEM results using with CUF elasticity.[30] Instead of the piezoresistive sensor method, the high temperature warpage of a chip in an FCB package with a CUF using digital imaging correlation (DIC) and FEM.[31] The results indicated that warpage of the FCB package with a CUF decreased as the temperature increased towards the bonding temperature. However, the temperature dependence of the residual stress after FCB with a CUF and an NCF has not yet been measured using a piezoresistive sensor on a chip.

In this paper, the local distribution of residual stress in a chip is evaluated using TEG chips. After FCB with a CUF and an NCF, the change in electrical resistance is measured at elevated temperatures during the FCB process, the moisture sensitivity level (MSL) and reflow process for confirmation of the stress when peeling occurs.

2. Experimental

Figure 1 shows the configuration of the piezoresistive sensor on the TEG chip (STAC-0101JY, WALTS Co., Ltd.) with a die pad and bump structure as shown Fig. 1(a). Each piezoresistive sensor consists of two piezoresistors in the X- and Y-directions, as shown Fig. 1(b). The process-induced stress is determined by measuring the resistance change in the piezoresistive sensor before and after the process. This TEG chip theoretically involves a margin of error from 1/100 to 1/10 because the stresses in the X- and Y-directions are larger than those in other directions; however, the stress in other directions cannot be separated.[20] Figure 2(a) shows two pairs of piezoresistive sensors, each located at the center and at the corner of a TEG chip. The TEG chip size is $3 \times 3 \text{ mm}^2$ and one set including 9 chips ($9 \times 9 \text{ mm}^2$) is bonded as shown in Fig. 2(b). Four piezoresistive sensors (A, B, C, and D) are located on the TEG chip, as shown in Fig. 2(b). The TEG chip thickness is $550 \mu \text{m}$. The pad pitch is $300 \mu \text{m}$ and the pad size is $100 \times 100 \mu \text{m}^2$. The Cu post height is $20 \mu \text{m}$ and SnAg solder post height is $20 \mu \text{m}$, as shown in Fig. 1(a). Figure 3(a) and Fig. 3(b) shows the substrate used for flip chip bonding, the size of which is $45 \times 45 \times 1 \text{ mm}^3$ (WALTS-KIT STAC-0201JY, WALTS Co., Ltd.). The measurement points for the four-point sensing method on the substrate after FCB are given in Table 1.

Figure 4(a) shows the substrate with the TEG chip after FCB. The measurement pad positions on the substrate

![Fig. 1 Configuration of piezoresistive sensor on the TEG chip.](image)

![Fig. 2 Schematic illustration of piezoresistive sensor on the TEG chip.](image)

![Fig. 3 Appearance of substrate.](image)
after FCB are shown in Fig. 4(b). The resistance of piezoresistive sensor (the piezoresistance) is measured by the four-point sensing method from the pad positions on the substrate, such as shown in Fig. 4(b).

The induced stress can be calculated from the resistance change $\Delta R$, given by:

$$\frac{\Delta R}{R_0} = S \sigma,$$

where $R_0$ is the initial resistance without stress, $\sigma$ is the stress, and $S$ is the stress sensitivity.\[8\]

The process-induced stress is determined using a piezoresistive sensor by measuring the difference between the resistance $R_0$ before the process, and the resistance $R_1$ after the process. The resistance and stress are very sensitive to conditions such as the temperature; therefore, the temperature must be carefully controlled to obtain accurate stress values. Moreover, various piezoresistive sensor coefficients must be determined to estimate the stress behavior with the change of temperature and are thus obtained from four-point bending tests.\[32\] Figure 5 shows the measured change in resistance with the tensile stress applied at 30°C. The solid line in the figure was obtained by the least squares method, and the value of $S$ is shown in Table 2.

The temperature dependence of $S$ was obtained by measuring the piezoresistive sensor at various temperatures. First of all, at $T_0 = 30^\circ$C, the stress sensitivity $S$ was calculated using:

$$\sigma_{T_0} \approx \frac{1}{S} \frac{R_{1T_0} - R_{0T_0}}{R_0}.$$

The temperature dependence of $\Delta R/R_0$ at a temperature $T$, is given by [13]:

![Fig. 4 Measurement pad position definitions on the substrate.](image)

Table 1 Measurement point definitions of four-point sensing method.

| X-direction | Y-direction |
|-------------|-------------|
| $V_{dd}$   | 1           | 5           |
| $V_{dd-s}$ | 2           | 6           |
| $V_{ss}$   | 3           |             |
| $V_{ss-s}$ | 4           |             |

![Fig. 5 Relationship between stress and resistance change rate at 30°C.](image)

Table 2 Measured parameters for the piezoresistive sensor in this experiment.

| Parameter          | Value           |
|--------------------|-----------------|
| $S$: Stress sensitivity | $-1.31 \times 10^{-4}$/MPa |
| $\beta_1$: Thermal dependence coefficient of stress sensibility | $1.60 \times 10^{-3}$/°C |
| $\beta_2$: Thermal dependence coefficient of piezo resistance | $-2.44 \times 10^{-7}$/°C |
| $C$: Thermal dependence coefficient constant | $-4.58 \times 10^{-2}$ |
\[ \Delta R / R_0 = \beta_1 T^2 + \beta_2 T + C. \]  

(3)

where \( \beta_1 \) is thermal dependence coefficient of stress sensitivity, \( \beta_2 \) is thermal dependence coefficient of piezo resistance, and \( C \) is a thermal dependence coefficient constant. The stress \( \sigma_{T_1} \) at \( T_1 \) was obtained from:

\[
\sigma_{T_1} = \frac{1}{S} \left[ \frac{R_1T_1 - R_0}{R_0T_0} + \beta_2 (T_1^2 - T_0^2) + \beta_1 (T_1 - T_0) \right].
\]

(4)

Figure 6 shows the change in resistance measured up to 120°C. The solid curve was obtained by least squares fitting with Equation (3). The obtained parameters are given in Table 2, from which the stress in a TEG chip after FCB at an elevated temperature was calculated.

Figure 7 shows the evaluation process flow with CUF. The resistance change triggered by stress is so small that direct measurement of the piezoresistive sensor may lead to a large error; therefore, measurement of the voltage is more accurate. A four-point sensing method is useful to precisely measure the piezoresistance. The initial piezoresistance on the bare TEG chip is defined as \( R_0 \), which was measured with probes in a dark environment. The temperature during measurement was controlled precisely by checking the temperature at a location near to the test TEG chip. Each TEG chip was bonded to the substrate at 260°C with a load of 10 N for 10 s by the FCB method using a flip-chip bonder (FCB3, Panasonic FS Co., Ltd.) as shown in Fig. 8. FCB flux cleaning was then conducted by ultrasonication in ethanol for 3 min. After the flux cleaning process, the piezoresistance was measured by probing the pad of the substrate with a probing tool (HFP-120A-202, Micronics Co., Ltd.) at 30°C using the four-point sensing method. CUF was then dispensed at 100°C using a manual dispenser and was then cured at 150°C for 60 min. For subsequent measurement of the piezoresistance at an elevated temperature, \( T_0 \) measure the piezoresistance at elevated temperatures, the FCB package was connected to the probe with a wire cable using solder as shown in Fig. 8.
9(a) and placed in an oven, as shown in Fig. 9(b). The piezoresistive sensor is very sensitive to temperature change. Therefore, the FCB package was held at temperature for 1.0 h to achieve the prescribed temperature accurately, followed by piezoresistance measurement. The detailed heating conditions for the piezoresistance measurements are listed in Table 3. The stress variation after the MSL and reflow test at a peak temperature of 260°C was also investigated. Prior to the reflow test, the MSL process was performed according to JEDEC Level 2a.

The evaluation process flow with NCF (A) and NCF (B) is shown in Fig. 10. Each TEG was laminated with NCF using a vacuum laminator (ATM-812, Takatori Co., Ltd.) at 80°C with a load of 0.3 MPa and a vacuum pressure of 0.1 Pa for 180 s. Each TEG was then bonded to the substrate. The FCB condition with NCF (A) was at the tool setting temperature of 300°C with a load of 10 N for 10 s, while that with NCF (B) was at 350°C with a load of 10 N for 10 s, as shown in Fig. 8. After the FCB process, the package was cured at 150°C for 60 min and the piezoresistance was measured by probing the pad of the substrate with a probing tool at 30°C using the four-point sensing method. The FCB package with NCF was placed in an oven and the resistance measurement was conducted after holding at

![Lead wire cable to probe connected by solder](image)

(a) Cross view the FCB package with lead wire

(b) Overview Oven with FCB package

**Fig. 9** Schematic structure of FCB package measured at elevated temperature.

**Table 3 Heat condition for measurement of $R_3$ and $R_6$.**

| Heat Condition       |                  |
|----------------------|------------------|
| Temperature of substrate (°C) | 30, 50, 70, 90, 110, 120 |
| Exposure time (h)    | 1.0              |
| Four-point sensing method |                |
| Electronic current (mA) | 0.1              |

**Fig. 10** Evaluation process flow using NCF (A) and NCF (B).
that temperature for 1.0 h. The FCB packages with NCF were then subjected to MSL and reflow testing, as with the CUF packages, and the piezoresistance was measured at 30°C.

The definitions of piezoresistance for the various packages and conditions are listed in Table 4. The material properties for CUF, NCF (A) and NCF (B) used in this study are tabulated in Table 5. Void and bump position gaps were checked for all packages using constant-depth mode scanning acoustic microscopy (CSAM) and X-ray transmission measurements. Cross sections of some TEG chips were polished to confirm voids, delamination, solder flow, solder shape and solder wettability, as shown in Fig. 11.

3. Results and Discussion

The measured residual stresses after FCB with and without CUF and with NCF (A) are shown in Fig. 12. Each plot represents the mean value of three specimens. The highest compressive stress occurred in the central position A by FCB. The compressive stress was high in the center of the TEG chips and decreased toward the edge. The compressive stress in the X- and Y-directions was almost the same, which may be due to the effect of the square chip shape. The compressive stress after FCB without CUF was approximately 20 MPa in the central position A, and the tensile stress was 5 MPa in the corner position D. When CUF is dispensed and cured, the compressive stress changed to between 40 and 50 MPa in the central position A, and 5 MPa of tensile stress remained in the corner position D. The stress in the corner before and after FCB was almost the same. The increment of compressive stress is the release stress from bump stress. In this result, the release stress is 20–30 MPa. The stress in the middle position B near the bump is increased. CUF is an excellent material to efficiently buffer the stress applied to the bump. A similar position includes D, but the relaxation effect could not be confirmed because there were few changes of stress by this measurement. For the package with NCF (A), compressive stress from 50 to 60 MPa was observed in the central position A and 20–30 MPa of compressive stress in the corner position D. The compressive stress between the X- and Y-directions was almost the same.

The residual stress curve using NCF (A) is more uniform than with CUF from the center to the edge. The stress in the corner position D is compressive stress and the stress is larger than that of CUF. So the relaxation effect of NCF is excellent to release the bump stress. The package is exposed to high temperature during soldering by the FCB method; therefore, shrinkage occurs during the cooling operation, which leads to compressive stress in
the TEG. The difference in residual stress between the NCF (A) and CUF packages was approximately 10 to 20 MPa, which is considered to be due to the difference of $T_g$ between CUF and NCF (A).

The residual stress after FCB without CUF was small because the stress due to the difference in the coefficient of thermal expansion (CTE) between TEG and the substrate was relieved in the solder bump. Therefore, piezoresistive sensors on the TEG chip could not detect the stress. The bump position on a TEG chip must be considered for further analysis, because the local stress changes near bumps. In addition, the stress of NCF (A) was larger than that of CUF; therefore, FCB using NCF is an effective method for releasing the stress of the bump.

The stress was also measured with increasing temperature up to 120°C. Figure 13 shows the temperature dependence of the residual stress in the package using CUF, while Fig. 14 shows that in the package using NCF (A). The compressive stress uniformly decreased with increasing temperature regardless of the piezoresistive sensor position. In the case of CUF, Heating in oven the stress of center position decrease has traced the absorbed curing behavior at the cooling time of FCB. NCF (A) and CUF materials were compared through the same process. The temperature of residual stress-free such as zero on the TEG chip with CUF and NCF (A) was approximately 90°C. The stress change is smaller at 90°C or more. Stress-release ability of CUF and NCF (A) are lowered with softening by approaching each $T_g$. The compressive stress changed to tensile stress by increasing thermal expansion of substrate.

The stress of NCF (A) and (B) with different $T_g$ were measured. $T_g$ of NCF (A) is 142°C and $T_g$ of NCF (B) is 200°C. Figure 15 shows the residual stress in the package using NCF (A) and NCF (B). Good solderability was not achieved for NCF (B) at 300°C, which is approximately the FCB condition for NCF; therefore, a temperature of 350°C, 50°C higher than that for NCF (A), was used as the tool setting temperature. The residual stress of NCF (B) was higher than that of NCF (A), and the difference between

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**Fig. 13** Temperature dependence of residual stress in the (a) X-direction and (b) Y-direction for CUF.

**Fig. 14** Temperature dependence of residual stress in the (a) X-direction and (b) Y-direction for NCF (A).
the NCF (A) and NCF (B) packages was approximately 5 to 10 MPa. When using NCF (B) with high $T_g$ near the solder melting point temperature, stress relaxation was excellent. To achieve excellent stress relaxation for avoiding bump damage after FCB, NCF with higher $T_g$ will be better.

After processing of the packages with CUF, NCF (A) and NCF (B) following MSL JEDEC Level 2a and 260°C peak reflow, the residual stress was measured. Figure 16 shows the residual stress using NCF (A) and NCF (B), and Fig. 17 shows that using CUF. After MSL and reflow, the residual stress of NCF (A) and NCF (B) didn’t change. Figure 17 shows that the compressive stress at the D position is high for CUF. From CSAM inspection, no delamination was observed between the substrate and NCF (A) or NCF (B), which indicates that NCF (A) and NCF (B) have good reflow reliability. However, delamination were observed at position A, B and C between the substrate and CUF. The stress at positions A, B and C where delamination occurred was not a change, but the stress at position D where delamination did not occur was increased. The increasing stress at position D was cause of the stress concentration.
4. Conclusion

TEG chips with piezoresistive sensors were applied for evaluation of the stress distribution in packages produced by FCB with CUF, NCF (A) and NCF (B). The results obtained from this research are summarized as follows:

1) After NCF (A) lamination, the TEG chip was connected to the substrate by FCB. The stress inside the TEG chip was obtained at each process of FCB by measuring the change in the piezoresistive sensor. After FCB, the compressive stress was high in the center of the TEG chip and decreased toward the edge of the TEG chip.

2) After FCB, compressive stress appeared on the piezoresistive sensor and the stress for NCF (A) with higher $T_g$ was larger than that for CUF.

The stress at elevated temperatures was also measured up to 120°C. The compressive stress decreased with increasing temperature and both NCF (A) and CUF materials were compared. Heating in the oven caused the substrate to expand and the stress became almost zero close to the $T_g$ of CUF and NCF (A). The stress-free temperature for CUF and NCF (A) became approximately 90°C. Above 90°C, the compressive stress on the TEG chip was changed to tensile stress. In addition, the residual stress at the TEG chip surface could be approximately treated as a linear shaped elastic body until the stress-free temperature, regardless of the position. Good reliability against moisture absorption and reflow was ascertained for NCF and no change in the stress distribution on the TEG chip was observed.

3) The stress was also measured with two types of NCF (A and B) with different $T_g$. When $T_g$ was high, the stress at position B near the bump did not become larger than that at other positions; therefore, stress relaxation occurred uniformly without being affected by the distance from the solder bump. To achieve excellent stress relaxation for avoiding bump damage after FCB, NCF with higher $T_g$ will be better.

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