Real-Time Formal Verification of Autonomous Systems With An FPGA

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Abstract—Hamilton-Jacobi reachability analysis is a powerful technique used to verify the safety of autonomous systems. This method is very good at handling non-linear system dynamics with disturbances and flexible set representations. A drawback to this approach is that it suffers from the curse of dimensionality, which prevents real-time deployment on safety-critical systems. In this paper, we show that a customized hardware design on a Field Programmable Gate Array (FPGA) could accelerate 4D grid-based Hamilton-Jacobi (HJ) reachability analysis up to 16 times compared to an optimized implementation and 142 times compared to MATLAB ToolboxLS on a 16-thread CPU. Our design can overcome the complex data access pattern while taking advantage of the parallel nature of the HJ PDE computation. Because of this, we are able to achieve real-time formal verification with a 4D car model by re-solving the HJ PDE at a frequency of 5Hz on the FPGA as the environment changes. The latency of our computation is deterministic, which is crucial for safety-critical systems. Our approach presented here can be applied to different systems dynamics, and moreover, potentially leveraged for higher dimensions systems. We also demonstrate obstacle avoidance with a robot car in a changing environment.

I. INTRODUCTION

Autonomous systems are becoming more prevalent in our lives. Examples of these systems include self-driving cars, unmanned aerial vehicles, rescue robots, etc. One key factor that will allow wider adoption of autonomous systems is the guaranteed safety of these systems. Despite tremendous progress in autonomous system research in areas such as motion planning, perception, and machine learning, deployment of these systems in environments that involve interactions with humans and other robots remains limited due to the potential danger these robotic systems can cause. Formal verification methods can help autonomous robots reach their untapped potential.

Hamilton-Jacobi (HJ) reachability analysis is a formal verification approach that provides guaranteed safety and goal satisfactions to autonomous systems under adversarial disturbances. There are many ways to do reachability analysis, solving the HJ PDE is one way to characterize sets of safe states and synthesizes optimal controllers, which involves calculating Backward Reachable Tube (BRT) that describes a set of states the system must stay out of in order to avoid obstacles. HJ reachability analysis has been successfully applied in practical applications such as aircraft safe landing [1], multi-vehicle path planning, multi-player reach avoid games [2]. The appeal of this particular method is that it’s very powerful in handling control and disturbances, nonlinear system dynamics, and flexible set representations.

The main downside to HJ reachability is that it’s solved on a multi-dimensional grid with the same number of dimensions as the number of state variables and scales exponentially with the number of dimensions. This prevents HJ formulation to be applied on real-time systems where safety is increasingly demanded. While 3D or smaller systems could be computed quickly with multi-core CPUs, practical systems that usually involve 4 to 5 system components can take several minutes to hours to compute. There have been researches that proposed decomposing high dimensional systems into smaller tractable sub-systems that can exactly compute [3] or overapproximate the BRT in certain cases [4]. However, that challenge of applying HJ formulation on real-time systems remains, as some systems cannot be decomposed further than four dimensions, and over-approximation is introduced if projection methods are used.

In this paper, we expand the limit of the number of dimensions for which we could directly compute the BRT in real time through the use of FPGA. We would argue that customized hardware accelerators could complement well with those decomposition methods in making higher dimensional systems provably safe in real-time. As general-purpose computer no longer double its performance every two years due to the end of Moore’s law, we have seen examples of successful hardware accelerations in other areas such as machine learning’s training/inference [5]–[7], robot’s motion planning [8].

In this paper, our contributions are as follows:

- We prototype a customized hardware design on FPGA that accelerates HJ reachability analysis to 16x compared to state-of-the-art implementation and 142x compared to [9] on 16-thread CPU for 4D system
- We demonstrate that the system could meet real-time requirement of guaranteeing safety in changing environments by re-computing BRT at 5Hz
- Demonstrate obstacle avoidance with a robot car driving in an environment in which new obstacles are introduced during run time at 5Hz.

II. PRELIMINARIES

A. Hamilton-Jacobi Reachability Analysis

Let \( s \leq 0 \) be time and \( z \in \mathbb{R}^n \) be the state of an autonomous system. The evolution of the system state over time is described by a system of ordinary differential equations (ODE) below.

\[
\dot{z} = \frac{dz(s)}{ds} = f(z(s), u(s), d(s)) \quad (1)
\]
where \( u(\cdot) \) and \( d(\cdot) \) denote the control and disturbance function respectively. The system dynamics \( f \) are assumed to be uniformly continuous, bounded and Lipschitz continuous in \( z \) for fixed \( u \) and \( d \). Given \( u(\cdot) \) and \( d(\cdot) \), there exists a unique trajectory that solves equation (1).

The trajectory or solution to equation (1) is denoted as \( \zeta(s; z, t, u(\cdot), d(\cdot)) : [t, 0] \rightarrow \mathbb{R}^n \), which starts from state \( z \) at time \( t \) under control \( u(\cdot) \) and disturbances \( d(\cdot) \). \( \zeta \) satisfies (1) almost everywhere with initial condition \( \zeta(t; z, t, u(\cdot), d(\cdot)) = z \).

In reachability analysis, we begin with a system dynamics described by an ODE and a target set that represents unsafe states/obstacles [10]. We then solve a HJ PDE to obtain Backward Reachable Tube (BRT), defined as follows:

\[
\mathcal{A} = \{ z : \exists \gamma \in \Gamma, \forall u(\cdot) \in \mathcal{U}, \exists s \in [t, 0], \zeta(s; z, t, u(\cdot), d(\cdot)) \in \mathcal{T} \} \tag{2}
\]

In HJ reachability analysis, a target set \( \mathcal{T} \subseteq \mathbb{R}^n \) is represented by the implicit surface function \( V_0(z) \) as \( \mathcal{T} = \{ z : V_0(z) \leq 0 \} \). The BRT is then the sub-level set of a value function \( V(z, s) \) defined as below:

\[
V(z, s) = \min_{d(\cdot)} \min_{u(\cdot)} V_0(\zeta(0; z, t, u(\cdot), d(\cdot))) \tag{3}
\]

We assume disturbance is applied with non-anticipative strategies [11]. In a zero-sum differential game, the control input and disturbances have opposite objectives.

The value function \( V(z, s) \) can be obtained as the viscosity solution of this HJ PDE:

\[
\min \{ D_s V(z, s) + H(z, \nabla V(z, s)), V(z, 0) - V(z, s) \} = 0
\]

\[
V(z, 0) = l(z), s \in [t, 0])
\]

\[
H(z, \nabla V(z, s)) = \min_{\gamma[u(\cdot) \in \mathcal{U}]} \gamma[u(\cdot) \in \mathcal{U}] \nabla V(z, s)^T f(z, u) \tag{4}
\]

We compute the HJ PDE until it converges. Numerical toolboxes based on level set methods such as [9] are used to obtain a solution on a multi-dimensional grid for the above equation.

B. Basic Numerical Solution

Let us store the value function on a multi-dimensional grid, with the numerical solution of the value function denoted as \( V \). Let \( N_d \) be the grid size on the \( d \)th axis (1 ≤ \( d \) ≤ 4). We also let \( x_{d,i} \) denote the state of grid \( i \) in dimension \( d \).

In our approach throughout this paper, we will adopt the central differencing scheme for approximating derivatives in dimension \( d \), which is defined as follows:

\[
D^-_d V(x_{d,i}) = \frac{V(x_{d,i}) - V(x_{d,i-1})}{\Delta x_d},
\]

\[
D^+_d V(x_{d,i}) = \frac{V(x_{d,i+1}) - V(x_{d,i})}{\Delta x_d},
\]

\[
D_d V(x_{d,i}) = \frac{D^+_d V(x_{d,i}) + D^-_d V(x_{d,i})}{2} \tag{5}
\]

The two terms \( D^-_d \) and \( D^+_d \) are the left and right approximations respectively. Note that for grid points at each end of each dimension (i.e \( i = N_d - 1, i = 0 \)), (5) is computed with extrapolated points. The basic algorithm for solving on-grid for 4D systems is then described as follows:

**Algorithm 1 Value function solving procedures**

1. \( V_0[N_1][N_2][N_3][N_4] \leftarrow l(z) \)
2. // Compute Hamiltonian term, and max, min deriv
3. \( \text{for } i = 0 : N_1 - 1; j = 0 : N_2 - 1; k = 0 : N_3 - 1; l = 0 : N_4 - 1 \text{ do} \)
4. Compute \( \alpha_d \) for 1 ≤ \( d \) ≤ 4
5. \( \text{minDeriv} \leftarrow \text{min}(\text{minDeriv}, D_d V(x)) \)
6. \( \text{maxDeriv} \leftarrow \text{max}(\text{maxDeriv}, D_d V(x)) \)
7. \( u_{opt} \leftarrow \arg \max_{u \in \mathcal{U}} \nabla V(z, s)^T f(z, u) \)
8. \( x \leftarrow f(z, u_{opt}) \)
9. \( H_{i,j,k,l} \leftarrow \nabla V(z, s)^T x \)
10. end for
11. // Compute dissipation and add to H
12. \( \text{for } i = 0 : N_1 - 1; j = 0 : N_2 - 1; k = 0 : N_3 - 1; l = 0 : N_4 - 1 \text{ do} \)
13. \( \text{alpha}(x) \leftarrow \max_{p \in [\text{minDeriv}, \text{maxDeriv}]} \left| \frac{\partial H(x, p)}{\partial p} \right| \)
14. \( H_{i,j,k,l} \leftarrow H_{i,j,k,l} - \Sigma_{d=1}^{4} \alpha_d(x) \frac{D^+_d(x) - D^-_d(x)}{2} \)
15. \( \text{alpha}(x) \leftarrow \max(\text{alpha}(x), \alpha_d) \)
16. end for
17. // Compute stable integration time step
18. \( \Delta t \leftarrow (\Sigma_{d=1}^{4} \alpha_d(x))^{-1} \)
19. \( \text{while } V_{t+1} < \text{H} \Delta t + V_t \)
20. \( V_{t+1} \leftarrow \min(V_0, V_{t+1}) \)
21. \( t \leftarrow |V_{t+1} - V_t| \)
22. if \( t < \text{threshold} \) then
23. \( V_{t} \leftarrow V_{t+1} \)
24. Go to line 3
25. end if

The above algorithm loops through the 4D array three times. In the first grid iteration, the Hamiltonian terms, maximum and minimum derivative is determined (lines 3-9). In the next grid iteration, the dissipation is computed and added to the Hamiltonian in order to make the computation stable. At the same time, the maximum alphas in all dimensions defined in line 13 are computed. These \( \alpha_d \) are used to determine the step bound \( \Delta t \). In the third grid iteration (line 19), each grid point is integrated for a length of \( \Delta t \).

**Fig. 1:** 9 memory accesses (yellow + green colored grid) within each iteration for computing derivatives in all 4 directions as in line 3 (algorithm [2])

In certain cases, \( \alpha_d(x) \) in line 13 is the same as computing the absolute value of \( x \), which has been computed in line 8.
In addition, in a lot of cases, \( \alpha_d^{\max} \) stays the same across different time iterations. We also observed that \( \Delta t \) depends only on grid configuration and \( \alpha_d^{\max} \). So instead of re-computing \( \Delta t \) every time and then loop through the 4D grid array again, we could pre-compute \( \Delta t \) and re-use it for all the time iterations. Combining these ideas together, throughout this paper, we will use the following algorithm with one grid looping, which is more computationally efficient:

### Algorithm 2 Value function solving procedures

1. \( V_0[1][2][3][4] \leftarrow l(z) \)
2. for \( i = 0 : N_1 - 1; \quad j = 0 : N_2 - 1; \quad k = 0 : N_3 - 1; \quad l = 0 : N_4 - 1 \) do
   3. Compute \( u_{opt} \) for \( 1 \leq d \leq 4 \)
   4. \( \hat{x} \leftarrow f(z, u_{opt}) \)
   5. \( H_{i,j,k,l} \leftarrow \Delta V(z, s)^T f(z, u) \)
   6. \( V_{t+1,0,1,2,3} \leftarrow \arg \max_{u \in U} \Delta V(z, s)^T f(z, u) \)
   7. \( V_{t+1,1,2,3} \leftarrow \min(V_{0,0}, V_{1,0}, V_{2,0}, V_{3,0}) \)
   8. Go to line 2

C. Field Programmable Gate Arrays (FPGA)

FPGA are configurable intergrated circuits that are programmed for specific applications using hardware description language (HDL).

Computing platforms such as CPUs, GPUs, and FPGAs have a memory component and computing cores. Compute cores must request and receive all the necessary data from the memory component before proceeding with the computation. If the memory component cannot provide all data access the application requires to proceed at once, cores have to stall and wait, slowing down the computation. Efficient systems need to have both fast computing cores and fast data distributions from the memory. Depending on the application, the memory access and computing pattern will vary. General-purpose CPU/GPU are often architected towards a reasonable performance for a wide variety of applications, but unoptimized for any particular application. FPGA chip, on the other hand, provides programmable digital circuits to design customized computing core and memory blocks. Thus, one can leverage knowledge about the details of the computing workload to design an efficient system accordingly with FPGA. With FPGA, one could control and achieve a higher degree of parallelism from the digital hardware level at the cost of programmability.

D. Problem Description

A key observation of algorithm 2 is that each new grid point \( V_{t+1} \) could be computed independently with each other within one time iteration and therefore, in parallel. We could then leverage a high degree of parallelism on FPGA by having many cores to update as many grid points concurrently as possible.

However, before that, two challenges must be addressed. Firstly, memory blocks need to efficiently distribute data to compute cores. In order for a loop computation to proceed, each of these cores needs up to 9 data inputs (Fig 2) and a memory design needs to satisfy this. Secondly, a four-dimensional grid takes up tens of megabytes in memory and therefore cannot be fully fit to FPGA's on-chip memory for fast access.

In this paper, our goal is twofold. First, we will discuss our hardware design that can solve the above challenges and maximize parallel computation of algorithm 2 while efficiently making use of FPGA’s on-chip memory. Next, we will show that this enables low latency of computation on FPGA which could be deployed in real-time systems.

III. SOLVING THE HJ PDE USING FPGAS

Before going into details of the design, we will introduce some terminologies that will be relevant throughout the next section.

In digital systems, time is discretized into the unit of a clock cycle, which is the amount of time it takes for an operation such as computing, loading, and storing to proceed. Each clock cycle typically is a few nanoseconds. Dynamic Random Access Memory (DRAM) is a type of memory that sits outside of the FPGA, which has higher memory capacity but takes a lot more clock cycles to access.

Our custom hardware comprised two main components: on-chip memory buffer, and processing elements (PE) or computing cores (shown in Fig 2). The memory buffer is on-chip storage, providing access to all the grid points a PE needs to compute a new value function. Each PE is a digital circuit that takes 9 grid points from the memory buffer to compute a new value function at a particular grid point according to algorithm 2 (line 3-10). In the following subsections, we will go into the details of each component.

A. Indexed Processing Element (PE)

The PE has the following target design objectives: (1) increase compute throughput (defined as the number of output generated per second) through pipelining, (2) reduce the computation time of each PE, (3) and ensure the correctness of result while minimizing data transfer between DRAM and FPGA.

In our design, we use 4 PEs (as shown in figure 2). Each PE has an index \( idx \) with \( 0 \leq idx \leq 3 \) associated with it and computes the grid point \( V_{t+1}(i,j,k,l + idx) \). At the beginning of the computation of algorithm 2, each PE takes as input a grid index \( (i,j,k,l) \) and its 8 neighbours to start computing \( V_{t+1}(i,j,k,l) \) according to algorithm 2 (line 2-10).

To increase computation throughput, each PE is fully pipelined. Similar to an assembly line, the PE operation is divided into multiple stages taking a few clock cycles to
Fig. 2: System overview on FPGA (Right). The initial value array is first transferred from DRAM to FPGA’s on-chip memory. The memory buffer then distributes data to the 4 PEs to concurrently compute the new value function at 4 consecutive grid points. The output from PE is then written back to DRAM. Each fully pipelined PE outputs one grid point every clock cycle (Left). Inside the PE, there are hardware components that sequentially solve algorithm 2.

Fig. 3: Pipelining schedule of a single PE. The PE’s operation is an assembly line where multiple grid points could be processed at the same time at different stages. Each stage is physical hardware that computes specific parts of algorithm 2. At a particular stage and a particular cycle, the PE is busy computing a certain part of algorithm 2 for the grid point at the indices shown. Note that for simplicity, the indices shown here are for a single PE only.

complete (Fig. 3). Each stage within the pipeline is physical hardware that has a computation corresponding to one of the lines in algorithm 2 (line 3-10) for a particular index $i, j, k, l$. Every clock cycle, the result from previous stages will be loaded to the next stage, following the sequential order of algorithm 2. At any time during operations, the processing element is computing different intermediate components for multiple indices concurrently (explained in Fig. 3).

To ensure that the computation is correct, inside each of the PE, there are indices counters to keep track of loop variable $i, j, k, l$, with the inner loop variable incrementing by one every clock cycle. These indices are used to correctly address the state vectors during system dynamics computation. To avoid accessing external DRAM we store these 4 state/position vectors $x$ or any fixed non-linear functions such as $\cos(\cdot)$ and $\sin(\cdot)$ of these states as a lookup table stored in on-chip memory, as state vectors depend only on grid configuration and do not change with the environment. Each PE will have its own look-up table to avoid communications between PEs. Having this data on-chip will only require a few kilobytes of memory and no need to access DRAM throughout the computation.

B. On-Chip Memory Buffer

The memory buffer has the following key design objectives: (1) minimizing the amount of on-chip memory usage and external DRAM accesses while (2) concurrently providing 9 grid points to each PE every clock cycle.

One problem of working with a high-dimensional grid is that the whole grid can take up tens of megabytes and therefore cannot be fully fit to a state-of-the-art FPGA’s on-chip memory. Instead of storing everything on-chip, in our design, grid points are streamed continuously from DRAM into an on-chip memory buffer (shown in Fig. 2) and can be re-used many times for spatial derivatives computation in 4 dimensions before being thrown away. From the grid dimensions, we could compute the maximum reuse distance beyond which a grid point can be safely discarded as no longer needed. This maximum reuse distance is equal to the minimum size of on-chip memory buffer, which is dependent only on $N - 1$ dimensions [12] and can be fitted to an FPGA’s on-chip memory. Our memory buffer structure is implemented as First In First Out (FIFO) queue data structure. Every clock cycle, a new grid point supplied from DRAM will start entering the FIFO queue while the grid point reaching at the end of the FIFO queue will be discarded.
Fig. 4: Four lines of memory buffer supply all the grid data to the four PEs. Each of the rectangle blocks is a FIFO queue synthesized as Block RAM (BRAM). The overhead notation is the size of the FIFO queue with $N_1$, $N_2$, $N_3$, $N_4$ as the four grid dimensions. Note that the queue’s size depends only on three dimensions. Every clock cycle, new grid points streamed from DRAM start entering each buffer line (left-hand side) and grid points at the end of the lines are discarded (right-hand side).

FPGA on-chip memory buffers are composed of standard Blocks of Random Access Memory (BRAM). Each BRAM has two-ports and at most two reads can be requested concurrently in the same clock cycle. If all 9 grid points (shown in Fig. 1) are stored in the same BRAM at the same time, a PE would then have to wait for 5 clock cycles before performing the computation. One way to increase the number of accesses per clock cycle is to duplicate the data in multiple BRAMs, but this would not work well for multidimensional arrays since these array copies easily exceed FPGA on-chip memory. A different technique would be memory banking, which is to partition the memory on-chip into multiple BRAM that could concurrently deliver data to the PE, allowing the PE to start to compute new value function for a grid point in one clock cycle.

To allow concurrent access for multiple PEs, we adopted the parallel memory buffer microarchitecture from [12]. Corresponding to the number of PEs, our on-chip storage structure is made of 4 line buffers. Each of these line buffers is a sequence of BRAM connected acting in a queue fashion: a grid point moves towards the end of the line every clock cycle. The two endpoints of each BRAM (shown in Fig 4) provide tapping points that are connected as inputs to the PEs. The number of PEs, therefore, is mainly limited by the DRAM bandwidth.

We also made modifications to the execution flow in [13] to accommodate for computing values function at the boundary. Once each of the buffer lines is half full, all the processing elements can start computing a new value function.

C. Fixed-Point Representation

Computing a new value function based on algorithm 2 involves multiple addition operations on floating-point numbers. At the hardware level, the addition of floating-point numbers is as computationally expensive as fixed-point multiplication, which would take up lots of resources and chip’s area. Instead, we use fixed-point representations for our data to reduce the burden on the hardware. We will show in the next section that this has little impact on the correctness of the computation if the radix point is chosen carefully for the grid configuration.

IV. EXPERIMENT & RESULT

A. Experiment setup

In this section, we demonstrate that our system can meet the real-time requirement through an obstacle avoidance demonstration in a changing environment.

We used a Tamiya TT02 model RC car [14] controlled by an on-board Nvidia Jetson Nano microcontroller inside a 4m $\times$ 6m room. We use the following extended Dubins car model for its dynamics:

$$
\dot{x} = v \cos(\theta),
\dot{y} = v \sin(\theta),
\dot{v} = a,
\dot{\theta} = \frac{v}{L} \tan(\delta)
$$

(6)

where $a \in [-1.5, 1.5]$, $\delta \in [-\frac{\pi}{18}, \frac{\pi}{18}]$, and $L = 0.3$m. The control inputs are the acceleration $a$ and the steering angle $\delta$. We use a grid size of $60 \times 60 \times 20 \times 36$ with resolutions of...
0.1 m, 0.067 m, 0.2 m/s and 0.17 rad for x-position, y-position, speed and angle, respectively.

Inside the room, we use orange cones as obstacles and a motion capture system is used to accurately track the car’s state and the position of the obstacles. We initialize the initial value function as follows:

\[ V_0(x, y, v, \theta) = \sqrt{(x - x_o)^2 + (y - y_o)^2 - R} \]  

where \( x_o \) and \( y_o \) are the obstacle’s positions and \( R \) is the radius of the cone. Obstacle’s positions can be obtained from the motion capture system. Each of the cones has a radius of 0.08 m but is set as 0.75 m to account for the model mismatch between the car and the dynamics used.

For the experiment, we considered three different environments, with different cone placements, set up inside the room as shown in Fig. 5. For each environment, a user manually controls the car and tries to steer into the cones.

\[ V(x, y, v, \theta) < 0.15 \]  

Given the car’s state, when (8) is satisfied, the car is near the boundary of a BRT so optimal control computed from the value function is applied to safely avoid the cone. The optimal control is obtained from the value function as follows:

\[ u_{opt} = \arg \max_{u \in U} \nabla V(x, y, v, \theta, s)^T f(x, y, v, \theta, u) \]  

We pre-compute the BRTs with a horizontal time of 0.5 s for three environments using optimized dp [15] and demonstrate safety by correctly loading the value functions as the environment changes. We choose to pre-compute the BRTs in order to emulate having an FPGA on-board without extra latency resulted from communication with a remote AWS instance. For all environments, the maximum time step to make the integration stable is 0.007497 s. Initially, the room had a single cone but changed over time to different cone placements. The BRT of a new environment could not be used until 200 ms after the environment has changed, which is longer than the time taken to compute the same BRT on an FPGA. A video of these experiments can be found at [https://www.youtube.com/playlist?list=PLUBop1d3Zm2vgPL4Hxtz8JufnIPmvrlC](https://www.youtube.com/playlist?list=PLUBop1d3Zm2vgPL4Hxtz8JufnIPmvrlC)

### B. Hardware Correctness

We use fixed-point data representations for hardware computation. In particular, we use 32 bits with 5 bits to represent the integer part (including sign) and 27 bits for the decimal part. With this choice, the precision of our computation is \( 2^{-27} = 7.45 \times 10^{-9} \) and the range of our computation is from \(-16\) to 16. The area we use for the experiment is 4 m \( \times \) 6 m, hence the largest absolute distance is the diagonal of 7.2 m. Therefore, the number of integer bits is enough to represent all possible values in the solution \( V \), which has the physical interpretation of minimum distance to collision over time, given (3) and the choice of \( V_0 \) in (7).

We choose to synthesize and implement our design on AWS F1 FPGA because of its flexibility and availability. To correctly input data to the FPGA, we first generate an initial value array based on the obstacles’ positions and radius described by (7). Then this value array is converted from floating-point to fixed-point number correctly based on the bit choice discussed above. Afterward, the value array is passed to the FPGA for the HJ PDE solving procedure to start.

For all three experiment, we verified the correctness of BRT generated by our hardware with the toolbox at [15] by comparing the maximum error between corresponding grid points. The toolbox uses 32-bit floating-point numbers. The numerical error resulting from the different representations is shown in table below for the three environments in table I.

| Env. | Error          |
|------|----------------|
| 1    | \(1.68 \times 10^{-6}\) |
| 2    | \(1.78 \times 10^{-6}\) |
| 3    | \(1.37 \times 10^{-6}\) |

These negligible errors are due to precision difference between fixed-point and floating point number. Even though the computation is repeated for many iterations, the maximum
error does not grow dramatically over time. We believe that is because of the convergence property of BRT. As time grows, the rate of changes in the grid values also slows down leading to stable discrepancy between the correct floating point and fixed-point values.

C. Computational speed and Resources Usage

To measure the speed up for all three environments, we compare the computation time on AWS FPGA running at 250MHz against [15] and [9] running on a 16-thread Intel(R) Core(TM) i9-9900K CPU at 3.60GHz. The latency here is the time it takes to compute the BRT. For FPGA, latency can be computed by multiplying the clock cycles with the clock period. The result is summarized in the table below.

| TABLE II: FPGA |
|----------------|
| Clock cycles | Period | Iterations | Latency |
|----------------|---------|-------------|---------|
| Env. 1 44155209 | 4 ns | 67 | 0.176s |
| Env. 2 44155209 | 4 ns | 67 | 0.176s |
| Env. 3 44155209 | 4 ns | 67 | 0.176s |

| TABLE III: optimized_dp [15] |
|-----------------------------|
| Latency | Iterations | FPGA speed up |
|----------------|-------------|---------------|
| Env. 1 3.35 s | 67 | ×18.9 |
| Env. 2 2.99 s | 67 | ×17.1 |
| Env. 3 3.42 s | 67 | ×19.4 |

| TABLE IV: ToolboxLS [9] |
|-------------------------|
| Latency | Iterations | FPGA speed up |
|----------------|-------------|---------------|
| Env. 1 25.11 s | 70 | ×142 |
| Env. 2 25.14 s | 70 | ×142 |
| Env. 3 25.18 s | 70 | ×142 |

It can be observed that the latency of computation on FPGA is fixed and deterministic for all three environments while the latency on CPUs varies even though the computation remains the same. With the lower latency of 0.176s, we are able to update the value function at a frequency of 5.68Hz. The resources usage of our design for 4 PEs is shown in the table below.

| TABLE V: Resources Usage |
|---------------------------|
| LUT | BRAM | DSP |
|----------------|--------|-----|
| Used | 26319 | 519 | 598 |
| Available | 111900 | 1680 | 5640 |
| Utilization | 14.03% | 30.89% | 10.6% |

On an FPGA, arithmetic operations on numbers are implemented using Digital Signal Processing (DSP) hardware or Look Up Table (LUT) that perform logical functions. Our design does not significantly consume most of the available resources and could be scaled up to a larger grid size.

V. CONCLUSION

This paper introduces a novel customized hardware design on FPGA that allows HJ reachability analysis to be computed 16x faster than state-of-the-art implementation on a 16-thread CPU. Because of that, we are able to solve the HJ PDE at a frequency of 5Hz. The latency of our computation on FPGA is deterministic for all computation iterations, which is crucial for safety-critical systems. Our design approach presented here can be applied to system dynamics and potentially higher dimensional systems. Finally, we demonstrate that at 5Hz, a robot car can safely avoid obstacles and guarantee safety.

REFERENCES

[1] A. K. Akametalu, C. J. Tomlin, and M. Chen, “Reachability-based forced landing system,” Journal of Guidance, Control, and Dynamics, vol. 41, no. 12, pp. 2529–2542, 2018.
[2] M. Chen, Q. Hu, C. Mackin, J. F. Fisac, and C. J. Tomlin, “Safe platooning of unmanned aerial vehicles via reachability,” in 2015 54th IEEE Conference on Decision and Control (CDC), pp. 4695–4701, 2015.
[3] M. Chen, S. L. Herbert, and C. J. Tomlin, “Exact and efficient hamilton-jacobi guaranteed safety analysis via system decomposition,” in 2017 IEEE International Conference on Robotics and Automation, ICRA 2017, Singapore, Singapore, May 29 - June 3, 2017, pp. 87–92. IEEE, 2017.
[4] A. Li and M. Chen, “Guaranteed-safe approximate reachability via state dependency-based decomposition,” in 2020 American Control Conference (ACC), pp. 974–980, 2020.
[5] N. P. Jouppi, C. Young, N. Patil, D. Patterson, G. Agrawal, R. Bajwa, S. Bates, S. Bhatia, N. Boden, A. Borchers, R. Boyle, P.-l. Cantin, C. Chao, C. Clark, J. Coriell, M. Daley, M. Dau, J. Dean, B. Gelb, T. V. Ghaemmaghami, R. Gottipati, W. Gulland, R. Hagmann, C. R. Ho, D. Hogberg, J. Hu, R. Hundt, D. Hurt, J. Ibarz, A. Jaffey, A. Jaworski, A. Kaplan, H. Khaitan, D. Killebrew, A. Koch, N. Kumar, S. Lacy, J. Laudon, J. Law, D. Le, C. Leary, Z. Liu, K. Lucke, A. Lundin, G. MacKean, A. Maggire, M. Mahony, K. Miller, R. Nagarajan, R. Narayanaswami, R. Ni, K. Nix, T. Norrie, M. Omernick, N. Penukonda, A. Phelps, J. Ross, M. Ross, A. Salek, E. Samadiani, C. Severson, G. Sizikov, M. Snelham, J. Souter, D. Steinberg, A. Swing, M. Tan, G. Thorson, B. Tian, H. Toma, E. Tuttle, V. Vastadovan, R. Walter, W. Wang, E. Wilcox, and D. H. Yoon, “In-datacenter performance analysis of a tensor processing unit,” in Proceedings of the 44th Annual International Symposium on Computer Architecture, ISCA ’17, (New York, NY, USA), p. 1–12, Association for Computing Machinery, 2017.
[6] Y. Chen, T. Krishna, J. S. Emer, and V. Sze, “Eyeriss: An energy-efficient reconfigurable accelerator for deep convolutional neural networks,” IEEE Journal of Solid-State Circuits, vol. 52, no. 1, pp. 127–138, 2017.
[7] S. Han, X. Liu, H. Mao, J. Pu, A. Pedram, M. A. Horowitz, and W. J. Dally, “Eie: Efficient inference engine on compressed deep neural network,” in 2016 ACM/IEEE 43rd Annual International Symposium on Computer Architecture (ISCA), pp. 243–254, 2016.
[8] S. Murray, W. Floyd-Jones, Y. Qi, G. Konidaris, and D. Sorin, “The microarchitectures of a real-time robot motion planning accelerator,” pp. 1–12, 10 2016.
[9] I. Mitchell, “The flexible, extensible and efficient toolbox of level set methods,” J. Sci. Comput., vol. 35, pp. 300–329, 06 2008.
[10] M. Chen and C. J. Tomlin, “Hamilton–Jacobi Reachability: Some Recent Theoretical Advances and Applications in Unmanned Airspace Management,” Annual Review of Control, Robotics, and Autonomous Systems, vol. 1, no. 1, pp. 333–358, 2018.
[11] S. Bansal, M. Chen, S. Herbert, and C. J. Tomlin, “Hamilton-jacobi reachability: A brief overview and recent advances,” in 2017 IEEE 56th Annual Conference on Decision and Control (CDC), pp. 2242–2253, IEEE, 2017.
[12] Y. Chi, J. Cong, P. Wei, and P. Zhou, “Soda: Stencil with optimized dataflow architecture,” in 2018 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 1–8, 2018.
[13] J. Cong, P. Li, B. Xiao, and P. Zhang, “An optimal microarchitecture for stencil computation acceleration based on non-linear partitioning of data reuse buffers,” in 2014 51st ACM/EDAC/IEEE Design Automation Conference (DAC), pp. 1–6, 2014.
[14] NVIDIA-AI-IOT, “Jetracer.” Available at https://github.com/NVIDIA-AI-IOT/jetracer.
[15] M. Bui, “Optimized dynamic programming,” 2020. Available at https://github.com/SFU-MARS/optimized_dp.