A Note on Exhaustive State Space Search for Efficient Code Generation

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Abstract

This note explores state space search to find efficient instruction sequences that perform particular data manipulations. Once found, the instruction sequences are hard-wired in the code generator that needs these data manipulations. Since state space is only searched while developing the compiler, search time is not at a premium, which allows exhaustively searching for the best possible instruction sequences.

1 Introduction

Compilers must often emit instruction sequences that accomplish particular data manipulations in the generated code. For example, a compiler may have to generate instructions that swap the contents of two scalar registers prior to an instruction with strict constraints on its register operands. Or, as another example, a compiler may have to emit instructions that broadcast the value in a scalar register to all elements of a vector register in the prologue of a vector loop. Using an efficient instruction sequence for each desired data manipulation reduces the runtime of any application that executes these data manipulations frequently.

Clearly, an optimizing compiler could try to find efficient instruction sequences during actual code generation. Although this possibly provides additional context for optimization, the major drawback of this approach is that search time directly contributes to compile-time during AOT compilation or, worse, runtime during JIT compilation. Alternatively, efficient instruction sequences for desired data manipulations could be searched for earlier, i.e. while the compiler is still being developed. Although this may provide less opportunities to exploit code context, search time is not at a premium in this approach, and an exhaustive state space search to find the best possible instruction sequences becomes possible. Once found, instruction sequences are hard-wired in the code generator and become at the immediate disposal of the compiler.

In this note, we explore using Prolog [Col93] for such a state space search. To keep the presentation brief, we focus on finding efficient Intel SSE instruction sequences for a few simple SIMD data manipulations. However, the presented ideas easily generalize to other instructions sets and code generation problems.
State Space Search

Finding an efficient instruction sequence to accomplish a particular data manipulation can be expressed as a state space search problem \cite{LS89,Nil98}, with the original contents of memory and registers as start state, the machine instructions as transitions from one state to another state, and the desired contents of memory and registers as goal state. A path from the start state to the goal state provides a solution to the problem. The best solution is given by the shortest path, i.e. the path with minimal length if all transitions have the same cost, or the path with minimal total weight if different transitions have varying costs, such as different cycle counts for the instructions.

2.1 State Space

As stated before, for the sake of brevity, we focus on finding efficient Intel SSE instruction sequences for a few simple SIMD data manipulations. Furthermore, to keep the state space size manageable, we focus on just a subset of the SIMD state, data types, and instructions, abstracting away from details related to general-purpose registers and instructions, state flags, memory operands, etc. In this simplified view, the SIMD state is fully defined by eight xmm-registers, represented in Prolog as a list with eight variables (variables start with an uppercase letter).

\[
[ \text{XMM0, XMM1, XMM2, XMM3, XMM4, XMM5, XMM6, XMM7} ]
\]

Here, each variable can be bound to a Prolog term that represent particular contents, such as a list \([17.5, 11.9]\) to denote a packed double-precision floating-point data type with the given numerical values, an atom \(\text{xmm0}\) (atoms start with a lowercase letter) to denote a particular but otherwise non-exploitable value, or the anonymous variable \(\_\) to denote any term. For example, the following list denotes a SIMD state in which registers 0, 3, and 7 contain packed data types with the given numerical values, registers 1 and 2 have particular but different contents that are not subject to further inspection, and all other registers are undefined.

\[
[ [0,0,0,0], \text{xmm1, xmm2, xmm3, xmm4, xmm5, xmm6, xmm7} ]
\]

In the remainder of the paper, we will just consider packed dwords represented by 4-elements lists, with the convention that the higher to lower packed elements appear left-to-right in the list.

2.2 Transitions

Each instruction transforms a SIMD state into another SIMD state. These transitions are modeled by a set of Prolog rules for each Intel SSE instruction in our simplified model. Each rule is this set will have the form

\[
i(\text{instruction, op1, op2, S, T}).
\]

to indicate that applying instruction to the given operands transitions from state \(S\) to state \(T\). For example, the change in SIMD state by executing instruction

\[
\text{pxor xmm0, xmm0}
\]
is modeled by rule show below, which specifies that any contents of register xmm0 (the anonymous variable \( \_ \)) is zeroed out (the list \([0,0,0,0]\)) while the contents of all registers remain unaffected.

\[
\begin{align*}
\text{ipxor, xmm0, xmm0,} \\
\text{[ \[ \_ \], XMM1, XMM2, XMM3, XMM4, XMM5, XMM6, XMM7 ]}, \\
\text{[ [0,0,0,0], XMM1, XMM2, XMM3, XMM4, XMM5, XMM6, XMM7 ]}.
\end{align*}
\]

Similarly, using Intel syntax, where the destination register appears first, the change in SIMD state after

\[
\text{paddd xmm1, xmm7}
\]

is modeled by the following rule, which adds the packed integral elements of one register to the packed integral elements of another register.

\[
\begin{align*}
\text{ipaddd, xmm1, xmm7,} \\
\text{[ XMM0, [A,B,C,D], XMM2, XMM3, XMM4, XMM5, XMM6, [E,F,G,H] ]}, \\
\text{[ XMM0, [A+E,B+F,C+G,D+H], XMM2, XMM3, XMM4, XMM5, XMM6, [E,F,G,H] ]}.
\end{align*}
\]

Although this allows Prolog to reason about the instruction symbolically, sometimes we are also interested in evaluating the values using integral arithmetic. To that end, the following rule is added as well, which evaluates expressions in which all values are integers (such rules could be refined further to allow for partial evaluation).

\[
\begin{align*}
\text{ipaddd, xmm1, xmm7,} \\
\text{[ XMM0, [A,B,C,D], XMM2, XMM3, XMM4, XMM5, XMM6, [E,F,G,H] ]}, \\
\text{[ XMM0, [P,Q,R,S], XMM2, XMM3, XMM4, XMM5, XMM6, [E,F,G,H] ]} := \\
\text{integer(A), integer(E), P is A+E, integer(B), integer(F), Q is B+F,} \\
\text{integer(C), integer(G), R is C+G, integer(D), integer(H), S is D+H.}
\end{align*}
\]

Similar rules are added for all other arithmetic, logical, comparison, and conversion instructions, and for all combinations of register pairs. A data shuffling instruction such as

\[
\text{punpckldq, xmm0, xmm3}
\]

is modeled as shown below.

\[
\begin{align*}
\text{ipunpckldq, xmm0, xmm3,} \\
\text{[ [\_,\_,A,B], XMM1, XMM2, [X,Y,C,D], XMM4, XMM5, XMM6, XMM7 ]}, \\
\text{[ [C,A,D,B], XMM1, XMM2, [X,Y,C,D], XMM4, XMM5, XMM6, XMM7 ]}.
\end{align*}
\]

A shift instruction like

\[
\text{psrlq xmm2, 4}
\]

is modeled by the rule below.

\[
\begin{align*}
\text{ippsrlq, xmm2, 4,} \\
\text{[ XMM0, XMM1, [A,B,C,\_], XMM3, XMM4, XMM5, XMM6, XMM7 ]}, \\
\text{[ XMM0, XMM1, [0,A,B,C], XMM3, XMM4, XMM5, XMM6, XMM7 ]}.
\end{align*}
\]

The SIMD state change after the data movement instruction

\[
\text{movd xmm4, I}
\]

is modeled with this rule.

\[
\begin{align*}
\text{imovd, xmm4, I,} \\
\text{[ XMM0, XMM1, XMM2, XMM3,} \\
\text{[ \[ \_ \], XMM5, XMM6, XMM7 ]}, \\
\text{[ XMM0, XMM1, XMM2, XMM3, [0,0,0,1], XMM5, XMM6, XMM7 ]}.
\end{align*}
\]

Obviously, writing all these Prolog rules by hand would be too tedious and error-prone. Instead, a utility should be used to generate all rules automatically, preferably directly from an instruction set description in an electronic format. A complete and accurate rule set will obviously yield the best results.
2.3 Search

Given a complete Prolog rule set that model the SIMD state transitions of all instructions, we need a search mechanism to find a path in the state space from the start state to the goal state. This search mechanism is also expressed with Prolog rules.

A first reasonable attempt is shown below (we will refine these rules slightly later). The two rules states that any state \( S \) transitions into itself for an empty instruction sequence, or otherwise breaks down into the transition of a single instruction from state \( S \) to state \( U \) followed by the transition from state \( U \) to state \( T \) of an subsequent instruction sequence \( J \). The list of 3-arity \( i \) predicates built by these rules ultimately indicate an instruction sequence that transitions state \( S \) to state \( T \).

\[
s(S, [], S).
s(S, [i(I,R1,R2)|J], T) :- i(I, R1, R2, S, U), s(U, J, T).
\]

Now suppose we are interested in finding the best way to zeroing the contents of register \( xmm0 \). It may be tempting to express that particular state space search problem with the following Prolog query.

\[
s(S, I, [[0,0,0,0] | _]).
\]

However, this query returns the following first solution, with an interpretation that the shortest way of resetting register \( xmm0 \) to zero is by executing no instructions at all (empty list \( I \)) but instead starting with all zeroes in that register (initial state \( S \)). Although correct, this is obviously not what we were searching for.

\[
I = []
S = [[0,0,0,0]|_]
\]

As a side note, this mistake can demonstrate a potential danger of using anonymous variables. The almost identical query

\[
s(_, I, [[0,0,0,0] | _]).
\]

would have given the solution

\[
I = []
\]

as well, but without even listing bindings for the two anonymous variables, obscuring the fact that the initial state was bound to a state with the first register already zeroed out. So each anonymous variable really denotes any suitable term. Rather, named variables should be preferred when contents matter.

The correct way of formulating the original query is by explicitly stating the fact that all registers contain unusable and unrelated initial values, as shown below with eight different atoms.

\[
s([xmm0, xmm1, xmm2, xmm3, xmm4, xmm5, xmm6, xmm7], I, [[0,0,0,0] | _]).
\]

This query will prompt the following list as a first solution, indicating a single instruction way of zeroing out register \( xmm0 \).

\[
I = [i(pxor,xmm0,xmm0)]
\]
2.4 Iterative Deepening Search

Prolog’s DFS (depth-first search) is not very suited for this particular kind of state space search problem, since it will continuously append instructions to existing partial solutions in an attempt to reach the goal state. A BFS (breadth-first search) works much better, since it will report the shortest instruction sequences from the initial state to the goal state first. We will implement such a search using Prolog’s DFS, but without the inherently high memory demands of BFS, using IDS (iterative deepening search). To this end, the search rules given earlier are refined into the following set.

\[
s(S, I, T) :- \text{count}(D, 0), s(S, I, T, D).
s(S, [], S, 0).
s(S, [i(I,R1,R2)|J], T, X) :- X > 0, Y is X - 1, i(I, R1, R2, S, U), s(U, J, T, Y).
\]

The search rules themselves are as before, but restricted to a given depth. The \text{count} rules define a simple increment mechanism.

\[
\text{count}(X, Y) :- Z is Y + 1, \text{count}(X, Z).
\]

Combined, these rules try to find solutions within subsequent instruction sequences of length 0, 1, 2, etc. As a result, shorter instruction sequences are reported first (note that with some effort, this search mechanism can be adapted for other criteria of the best solution, such as finding the instruction sequences with the lowest total cycle counts). For example, running the query

\[
s( [ xmm0, xmm1, xmm2, xmm3, xmm4, xmm5, xmm6, xmm7], I, [ [-1,-1,-1,-1] | _ ] ).
\]

reports the desired solution

\[
I = [i(pcmpsd,xmm0,xmm0)]
\]

before it reports the following alternative, but longer solution, which basically just clobbers the register with an unused value before resorting to the shorter solution.

\[
I = [i(pxor,xmm0,xmm0),i(pcmpsd,xmm0,xmm0)]
\]

Suppose we are interested in broadcasting a value to all elements in a SIMD register, an idiom that is frequently used in the prologue of a vector loop by a vectorizing compiler [Bik04]. An instruction sequence for such a broadcast can be found using the following query, where atom \(c\) denotes the value that needs broadcasting.

\[
s( [ xmm0, xmm1, xmm2, xmm3, xmm4, xmm5, xmm6, xmm7], I, [ [c,c,c,c] | _ ] ).
\]

Lacking a shuffle operation in our simplified rule set, the shortest instruction sequence for the broadcast consists of a data movement instruction followed by two unpack instructions.

\[
I = [i(movd,xmm0,c),
i(punpckldq,xmm0,xmm0),
i(punpckldq,xmm0,xmm0)]
\]
2.5 Usable Start State

The examples so far searched for a particular goal state given an unusable state state. Often, however, the start state may contain some known, usable information. As a simple example, the query

\[ s([\text{xmm0}, [1,2,3,4], \text{xmm2}, \text{xmm3}, \text{xmm4}, \text{xmm5}, \text{xmm6}, \text{xmm7}], I, [[1,2,3,4] | _]). \]

yields the following solution, which indicates that the best way to assign particular contents to register xmm0 given a state where register xmm1 already has these contents is simply moving the register.

\[ I = [i(\text{movdqa}, \text{xmm0}, \text{xmm1})] \]

As a more practical application, this approach can be used to find the best sequence to sum up all elements in a SIMD register "horizontally", an idiom used by a vectorizing compiler [Bik04] to finalize the computation after converting a sum-reduction loop into SIMD code. Here the query

\[ s( [ [\text{a,b,c,d}], \text{xmm1}, \text{xmm2}, \text{xmm3}, \text{xmm4}, \text{xmm5}, \text{xmm6}, \text{xmm7}], I, [\text{...}, (d+b)+(c+a)] | _ ] ). \]

yields the following instruction sequence as first suitable solution.

\[ I = [ i(\text{movdqa}, \text{xmm1}, \text{xmm0}), \\
i(\text{psrldq}, \text{xmm0}, 8), \\
i(\text{paddd}, \text{xmm1}, \text{xmm0}), \\
i(\text{punpckldq}, \text{xmm0}, \text{xmm1}), \\
i(\text{paddd}, \text{xmm0}, \text{xmm1}), \\
i(\text{psrldq}, \text{xmm0}, 4) ] \]

Subsequent solutions with the same length provide some true alternatives (here, cycle counts could help finding the truly best one).

\[ I = [ i(\text{movdqa}, \text{xmm1}, \text{xmm0}), \\
i(\text{psrldq}, \text{xmm0}, 8), \\
i(\text{paddd}, \text{xmm1}, \text{xmm0}), \\
i(\text{movdqa}, \text{xmm0}, \text{xmm1}), \\
i(\text{psrldq}, \text{xmm1}, 4), \\
i(\text{paddd}, \text{xmm0}, \text{xmm1}) ] \]

Other solutions of the same length that follow may simply provide the same instruction sequences using different intermediate registers.

Note that in this example, a statically known property of the context in which the instruction sequence is needed allowed for adding some usable information to the start state (viz. the SIMD register contains four partial results that need to be summed up). As stated in the introduction, at runtime the compiler could even exploit some dynamically known properties of the context to find better instruction sequences, but it is unlikely that exhaustive search (let alone Prolog) could be used under such circumstances.
3 Conclusions

In this note, we explored using Prolog for finding efficient data manipulating instruction sequences. The problem is expressed as a state search problem, with the initial memory and register contents as start state, machine instructions as transitions, and the desired memory and register contents as goal state. Modeling instructions with a complete and accurate Prolog rule set of transitions will yield the best results, where it preferable to extract such a rule set automatically from an instruction set description in an electronic format. Search is expressed with Prolog rules as well, enhanced with iterative deepening to work around obvious complications with the default depth-first search of Prolog.

Once the best solution is found after exhaustively searching the state space, the instruction sequence can be hard-wired in any code generator that needs the data manipulation, and becomes at the immediate disposal of the compiler. Here, the best can be defined as the shortest instruction sequence or, with some adaptation, as the instruction sequence with minimal total weight, such as summing the cycle counts. For the sake of brevity, we restricted our focus on finding efficient Intel SSE instruction sequences using just a subset of the SIMD state, instructions, and data types. However, the presented ideas easily generalize to broader instruction sets and code generation problems.

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