An estimation method of timing mismatch error in hybrid filter bank DACs

Linglong Yin\textsuperscript{1}, Shulin Tian\textsuperscript{1}, Ke Liu\textsuperscript{a1}, Guangkun Guo\textsuperscript{1}, and Yindong Xiao\textsuperscript{1}

Abstract This paper presents an estimation method of timing mismatch error in hybrid filter bank digital-to-analog converter (HFB DAC). An approximated transfer function of HFB DAC with timing mismatch is derived based on the Taylor series. Then an iteration method is introduced to approach the timing error. Besides, we analyze the influence of test signal and give the requirements on test input. Using this signal, the iteration will have a fast convergence speed. Simulation experiments show the effectiveness of the proposed estimation method.

key words: hybrid filter bank, digital to analog converter, timing mismatch, estimation method, Taylor series

Classification: Circuits and modules for electronic instrumentation

1. Introduction

The rapid development of modern electronic test and measurement system exhibit a high demand for wideband signal generation \cite{1, 2, 3}. Flexible signal generators such as arbitrary waveform generators (AWG) have been widely used in these aspects \cite{4, 5}. However, the bandwidth of these instruments are restricted by the speed of Digital-to-Analog Converter (DAC). Many studies focus on the time-interleaved (TI) DAC \cite{6, 7, 8, 9} and frequency-interleaved (FI) DAC \cite{10, 11} have been published to solve this problem. TIDAC is a parallel structure. The sub-DACs perform the digital to analog conversion alternately and hence achieve a high equivalent sampling rate. The main problem of this architecture is that although the sampling rate has been multiplied, it has limited ability to improve the output bandwidth \cite{12, 13, 14}. The zero-order-hold (ZOH) characteristics still restrict the bandwidth with in two Nyquist band. The FI-DAC is an effective way to overcome the restriction caused by ZOH. A typical FIDAC architecture is introduced in \cite{10}. The digital signal is fed through digital Fourier transform (DFT) to obtain the frequency domain representation and then split into several parts to perform the conversion individually. This architecture requires the signal to be completely fed into the system and then the DFT could be performed. So it is not applicable for those signal generators that continuously receive data from host.

Another promising way to enlarge the bandwidth is hybrid filter bank (HFB) DAC \cite{15}. The HFB DAC uses digital analysis filter bank to split the signal into narrow bands instead of carrying it out in frequency domain like FIDAC. HFB is widely used to analysis time interleaved Analog-to-Digital Converter (TIADC) \cite{16, 17, 18, 19} while the HFB DAC is relatively less studied. Since the mismatch errors of filter banks significantly degrade the system performance \cite{20, 21, 22, 23}. Many studies \cite{24, 25, 26, 27} focus on the perfect reconstruction design of filter banks while the mismatch estimation and calibration are relatively less studied. In \cite{28}, a pre-compensation method for mixers mismatch error in HFB DAC is proposed. However, the mismatch is a prior information which is assumed to be known before compensation. In \cite{29}, an estimation and compensation method of time delay in HFB DAC is presented. Nevertheless, this method can only estimate and compensate one channel at once. Besides, it assumed an ideal digital down-conversion which is difficult to realize in real applications.

In this paper, we present an estimation method of timing mismatch in HFB DAC. An approximated transfer function is derived using Taylor series. Based on this, we introduce an iteration method to estimate the timing mismatch. The requirements on the test signal are analyzed. With this signal, the iteration would have a fast convergence speed and make more accurate estimation. The rest of this paper is organized as follows. Section 2 gives a brief analysis of HFB DAC with timing mismatch. Section 3 introduces the estimation method and analyze the requirements on test input. Section 4 presents the simulation experiments. Section 5 gives the conclusion.

2. Hybrid-filter-bank DAC with timing mismatch

Hybrid-filter-bank DAC is proposed to perform the digital to analog conversion with low speed DACs. Fig. 1 shows a typical diagram of HFB DAC. The input $x[n]$ is a real valued data with clock period of $T$. It will be filtered with analysis filter and down sampled to match the speed of DAC device. The output $x_m[n]$ is given by
where \( X(e^{j\omega}) \) is the discrete time Fourier transform (DTFT) of input. \( F_m(e^{j\omega}) \) is the analysis filter of \( m \)-th channel. The common used DAC has a sample-and-hold circuit (e.g. zero-order-hold, ZOH) to maintain the output value over a sampling period. This causes a sinc-shaped envelope on spectrum. Hence, the output of \( m \)-th DAC could be represented as

\[
\tilde{X}_m(j\Omega) = X_m(e^{j\Omega MT})H_{ZOH}(j\Omega)
\]  

(2)

where the DACs run at the speed of \( MT \). \( H_{ZOH}(j\Omega) \) represents the frequency character of ZOH and is given by

\[
H_{ZOH}(j\Omega) = MT \cdot \text{sinc}(\Omega MT / 2) \cdot e^{-j\Omega MT / 2}
\]  

(3)

The output of subchannel would be shifted to a specific frequency band by means of mixer and filtered by the synthesis filter \( G_m(j\Omega) \). The spectrum of \( \tilde{y}_m(t) \) could be written as

\[
\tilde{y}_m(j\Omega) = \frac{1}{2} (\tilde{X}_m(j\Omega - j\Omega_m) + \tilde{X}_m(j\Omega + j\Omega_m)) G_m(j\Omega)
\]  

(4)

where \( \Omega_m = [m/2] \frac{2\pi}{MT} \). All these subchannel signals \( \tilde{y}_m(j\Omega) \) would be summed together to yield the reconstructed output signal \( y(t) \)

\[
Y(j\Omega) = \sum_{m=0}^{M-1} \tilde{y}_m(j\Omega) = \sum_{p=0}^{M-1} X(e^{j\Omega_T - j\frac{2\pi p}{M}}) T_p(j\Omega)
\]  

(5)

where

\[
T_p(j\Omega) = \frac{1}{2M} \sum_{m=0}^{M-1} F_m(e^{j\Omega_T - j\frac{2\pi p}{M}}) G_m(j\Omega)
\]  

(6)

\[
\times [H_{ZOH}(j\Omega - j\Omega_m) + H_{ZOH}(j\Omega + j\Omega_m)]
\]

It could be observed from Eq. (5) that the output is a mixture of desired signal \( p = 0 \) and the spurious components \( p = 1, 2, \ldots, M - 1 \). If the transfer function \( T_p(j\Omega) \) satisfy

\[
T_p(j\Omega) = \begin{cases} 
  e^{-j\Omega_T t} & p = 0 \quad \Omega \in (-\frac{\pi}{T}, \frac{\pi}{T}) \\
  0 & p \neq 0 \quad \Omega \in (-\frac{\pi}{T}, \frac{\pi}{T})
\end{cases}
\]  

(7)

where \( c \) is a nonzero constant and \( T_d \) denotes the delay. It could be regarded as a perfect reconstruction HFB system. Several studies have been published focus on the design of perfect reconstruction \([25, 26, 27]\)

If the timing mismatch error occurred, \( x'_m(t) = \tilde{x}_m(t - \Delta t_m) \).

Eq. (2) could be represented as

\[
X'_m(j\Omega) = X_m(e^{j\Omega MT})H_{ZOH}(j\Omega) e^{-j\Omega \Delta t_m}
\]  

(8)

\( \Delta t_m \) represents the time error of \( m \)-th DAC. Substituting Eq. (8) into Eq. (5), we could obtain the transfer function \( T'_p(j\Omega) \) with timing mismatch

\[
T'_p(j\Omega) = \frac{1}{2M} \sum_{m=0}^{M-1} F_m(e^{j\Omega_T - j\frac{2\pi p}{M}}) G_m(j\Omega)
\]  

(9)

\[
\times [H_{ZOH}(j\Omega - j\Omega_m) e^{-j\Omega \Delta t_m} + H_{ZOH}(j\Omega + j\Omega_m) e^{-j\Omega \Delta t_m}]
\]

3. Estimation method and requirements on the input

3.1 Estimation method

Since the timing mismatch \( \Delta t_m \) is usually very small compared to the DAC sampling period \( MT \) \([30]\), we use Taylor series to make an approximation of complex exponential function \( f(t) = e^{jt} \) around the point \( t = 0 \) and it could be written as

\[
f(t) = \sum_{k=0}^{\infty} \frac{f^{(k)}(0)}{k!} t^k
\]  

(10)

Here, we preserve the first order and substitute it into Eq. (9). An approximated transfer function is represented as

\[
\hat{T}_p(j\Omega) = \frac{1}{2M} \sum_{m=0}^{M-1} F_m(e^{j\Omega_T - j\frac{2\pi p}{M}}) G_m(j\Omega)
\]  

(11)

\[
\times [H_{ZOH}(j\Omega - j\Omega_m)(1 - (j\Omega - j\Omega_m)\Delta t_m) + H_{ZOH}(j\Omega + j\Omega_m)(1 - (j\Omega + j\Omega_m)\Delta t_m)]
\]

Considering a test input given by

\[
X(e^{j\omega t}(-\frac{2\pi p}{M})) = 0 \quad \text{for} \; X(e^{j\omega t}) \neq 0
\]  

(12)

where \( \omega t' \in (-\pi, \pi) \). It simplifies the Eq. (5) and the output could be represented as

\[
Y(j\Omega_t') = X(e^{j\Omega_T t}j\Omega_t')
\]  

(13)

where \( \Omega_t T = \omega t' \). This means no aliasing at the frequency \( \Omega_t \). We could further write Eq. (13) into a matrix form

\[
O = D + W \Delta t
\]  

(14)

where

\[
\Delta t = [\Delta t_0, \Delta t_1, \ldots, \Delta t_{M-1}]^T
\]

\[
O = [Y(j\Omega_1), Y(j\Omega_2), \ldots, Y(j\Omega_N)]^T
\]

\[
D = [X(e^{j\Omega_{1T}})T_0(j\Omega_1), \ldots, X(e^{j\Omega_{NT}})T_0(j\Omega_N)]^T
\]
could be adopted. However, if we choose frequency bins from this low-pass signal, it may cause an inaccurate result and a low speed convergence. This will be shown in the simulation experiment. Here, we give a brief analysis. Considering the frequency bin located at $\Omega_i = \omega_i / T$, the output could be written as

$$Y(j\Omega_i) = \frac{1}{2M} X(e^{j\omega_i T}) \sum_{m=0}^{M-1} R_m(j\Omega_i)$$

(19)

$$R_m(j\Omega_i) = F_m(e^{j\omega_i}) G_m(j\Omega_i)$$

$$\times [H_{ZOH}(j\Omega_i - j\Omega_m) e^{-j(\Omega_i - \Omega_m)T/2} + H_{ZOH}(j\Omega_i + j\Omega_m) e^{-j(\Omega_i + \Omega_m)T/2}]$$

The frequency response consists of $M$ parts $R_m(j\Omega_i)$, $m = 0, 1, \ldots, M - 1$. Since the analog synthesis filters distribute across a wide frequency band. For the synthesis filter $G_{M-1}(j\Omega)$ whose passband is roughly located at $(\frac{(M-1)}{M} \pi, \pi) / T$. A low-pass signal will fall into its stopband, and the amplitude of $|R_{M-1}(j\Omega_i)|$ will be significantly small.

As a result, the timing mismatch error in $(M-1)$-th channel would have little impact on the overall frequency response at $\Omega_i$. It implies that the estimated $\Delta t_{M-1}$ is insensitive to the actual timing error $\Delta t_{M-1}$. This may cause a slow convergence speed of $\Delta t_{M-1}$. To avoid this problem, the test frequency bins should be distributed among the passband of all the synthesis filter. Hence a wideband multitone signal is considered to be the test input in this paper.

4. Simulation results

To verify the effectiveness of the proposed estimation method. A four channel $(M=4)$ 12-bit HFB DAC is modeled.

Each DAC has a sampling rate of 500MSPS and hence the system has an equivalent sampling rate of $F_s = 2$GSPS. The analysis filter banks and synthesis filter banks are designed using the method in [26] and have same parameters. Timing mismatch error is set to $\Delta f = [0.02, -0.03, 0.01, -0.05]T \times MT$. A wideband multitone signal $x_1[n]$ with frequency bins $[101, 701, 1193, 1801] / 4096 \times F_s$ is adopted as the test input. The iteration starts at $(\Delta f)_0 = [0, 0, 0, 0]T \times MT$.

![Fig. 2. Block diagram of the estimation structure](image)

Fig. 2 shows the block diagram of the estimation structure.

![Fig. 3. Spectrum of output with $x_1[n]$ before iteration](image)

Fig. 3 shows the output spectrum of test signal before iteration, it can be seen that there are many spurious components in the output. However, due to the careful selection of frequency bins, the spurious tones do not alias on the chosen
frequency. After 3 iterations, Fig. 4 shows the spectrum of output, the spurious signal is significantly attenuated.

![Graph showing spectrum of output](image)

Fig. 4. Spectrum of output with $x_1[n]$ after 3 iteration

Table I shows the detailed value of each iteration. It could be observed that the results converge at the 4th iteration. Using Eq. (17), the final estimated value is $\Delta\hat{f} = [0.0200, -0.0300, 0.0100, -0.0500]^T \times MT$. Fig. 5 shows the convergence procedure.

![Graph showing convergence procedure](image)

Fig. 5. Convergence procedure with $x_1[n]$

To further show the performance and effectiveness of the estimation method, a Monte Carlo (MC) simulation with 500 trials for each test is also performed. In this experiment, the timing error of each channel follows the zero-mean Gaussian distribution with variance $\sigma^2$. Table II shows the simulation results. It could be seen that when the timing mismatches become worse (i.e. $\sigma$ becomes larger), the estimation procedure trends to need more iterations. However, it still has an accurate estimated value.

To verify the analysis of test input, a low-pass signal $x_2[n]$ with frequency bins $[73, 151, 201, 297]/4096 \times f_s$ is also tested. Fig. 6 shows the iteration procedure, it takes 6 iterations to converge. Detailed result of each iteration is listed in Table III. The final estimated value is $\Delta\hat{f} = [0.0200, -0.0300, 0.0100, -0.0501]^T \times MT$. It can be seen that the estimation of $\Delta\hat{f}_{MT}$ becomes not that accurate when using low-pass signal. It could also be observed in Fig. (6) that $\Delta\hat{f}_m$ has different converge speed. $\Delta\hat{f}_0$ and $\Delta\hat{f}_1$ is faster than $\Delta\hat{f}_2$ and $\Delta\hat{f}_3$. This is consistent with our analysis.

![Graph showing convergence procedure with $x_2[n]$](image)

Fig. 6. Convergence procedure with $x_2[n]$

**5. Conclusion**

In this paper, an estimation method of timing mismatch error in HFB DAC is proposed. An approximated model is derived using Taylor series and then an iteration method is introduced to approach the mismatch value. Besides, we give an analysis of the requirements on the test signal and design a wideband multitone signal. When using this test signal, the iteration has a fast convergence speed. Simulation experiments show the effectiveness of the proposed estimation method.

**References**

[1] F. Sun, et al.: “Wideband frequency reconfigurable antenna array,” IEICE Electron. Express 15 (2018) 20171210 (DOI: 10.1587/elex.15.20171210).

[2] G. Engel, et al.: “RF digital-to-analog converters enable direct synthesis of communications signals,” IEEE Commun. Mag. 50 (2012) 108 (DOI: 10.1109/MCOM.2012.6316784).

[3] H. He, et al.: “Wideband MIMO Systems: Signal Design for Transmit Beampattern Synthesis,” IEEE Trans. Signal Process. 59 (2011) 618 (DOI: 10.1109/TSP.2010.2091410).

[4] Y. Veyrac, et al.: “A 65-nm CMOS DAC Based on a Differentiating Arbitrary Waveform Generator Architecture for 5G Handset Transmitter,” IEEE Trans. Circuits Syst. II, Exp. Briefs 63 (2016) 104 (DOI: 10.1109/TCSII.2015.2504947).
[5] Deping Zhang, et al.: “An ultra-high ramp rate arbitrary waveform generator for communication and radar applications,” IEICE Electron. Express 12 (2015) 20141163 (DOI: 10.1587/elex.12.20141163).

[6] C. Krall, et al.: “Time-Interleaved Digital-to-Analog Converters for UWB Signal Generation,” ICUWB (2015) 366 (DOI: 10.1109/ICUWB.2007.438097).

[7] G. Hovakimyan, et al.: “Digital Correction of Time Interleaved DAC Mismatches,” 2019 IEEE Int. Symp. Circuits Syst. (ISCAS) (2019) 1 (DOI: 10.1109/ISCAS.2019.8702209).

[8] Ke Liu, et al.: “Analysis of Phase Truncation Error Based on Multi-Path Pseudo-Interleaved Direct Digital Frequency Synthesis,” J CIRCUIT SYST COMP 24 (2015) 1550146 (DOI: 10.1142/S0218126615501467).

[9] S. Xu and J. W. Lee: “Calibration and Correction of Timing Mismatch Error in Two-Channel Time-Interleaved DACs,” 2019 IEEE Int. Symp. Circuits Syst. (ISCAS) (2019) 1 (DOI: 10.1109/ISCAS.2019.8702463).

[10] C. Schmidt, et al.: “Digital-to-analog converters for high-speed optical communications using frequency interleaving: impairments and characteristics,” Opt. Express 26 (2018) 6758 (DOI: 10.1364/OE.26.006758).

[11] C. Schmidt, et al.: “Digital-to-Analog Converters Using Frequency Interleaving: Mathematical Framework and Experimental Verification,” Circuits Syst Signal Process 37 (2018) 4929 (DOI: 10.1007/s00034-018-0791-y).

[12] S. Balasubramanian, et al.: “Direct digital-to-RF digital-to-analogue converter using image replica and nonlinearity cancelling architecture,” Electron. Lett. 46 (2010) 1030 (DOI: 10.1049/el.2010.1154).

[13] S. Balasubramanian, et al.: “Architectural trends in GHz speed DACs,” NORCHIP 13 (2012) 1 (DOI: 10.1109/NORCHIP.2012.6403097).

[14] S. Balasubramanian, et al.: “Ultimate Transmission,” IEEE Microwave Mag. 13 (2012) 64 (DOI: 10.1109/MMM.2011.217398).

[15] S. R. Velazquez, et al.: “Design of hybrid filter banks for analog/digital conversion,” IEEE Trans. Signal Process. 46 (1998) 956 (DOI: 10.1109/78.668549).

[16] X. Liu and Y. Zhao: “A novel oversampling scheme for design of hybrid filter bank based ADCs,” IEICE Electron. Express 15 (2018) 20180007 (DOI: 10.1587/elex.15.20180007).

[17] X. Liu, et al.: “Adaptable Hybrid Filter Bank Analog-to-Digital Converters for Simplifying Wideband Receivers,” IEEE Commun. Lett. 21 (2017) 1525 (DOI: 10.1109/LCOMM.2017.2690281).

[18] B. Szlachetko: “Toward wide-band high-resolution analog-to-digital converters using hybrid filter bank architecture,” Circuits Syst. Signal Process. 35 (2016) 125 (DOI: 10.1007/s00034-015-0332-2).

[19] X. Peng, et al.: “Calibration technique for new-structure, two-channel hybrid filter banks ADC,” IEICE Electron. Express 15 (2018) 20180290 (DOI: 10.1587/elex.15.20180290).

[20] S. J. Liu et al.: “Calibration for Realization Errors of Two-Channel Hybrid Filter Bank Analog-to-Digital Converters Based on Frequency-Dependent Model,” Circuits, Syst. Signal Process. 33 (2014) 761 (DOI: 10.1007/s00034-013-9657-5).

[21] S. J. Darak et al.: “Reconfigurable Filter Bank With Complete Control Over Subband Bandwidths for Multi-standard Wireless Communication Receivers,” IEEE Trans. Very Large Scale Integr. VLSI Syst. 23 (2015) 1772 (DOI: 10.1109/TVLSI.2014.2347899).

[22] S. H. Zhao and S. C. Chan: “Design and Multiplierless Realization of Digital Synthesis Filters for Hybrid-Filter-Bank A/D Converters,” IEEE Trans. Circuits Syst. I, Reg. Papers 56 (2009) 2221 (DOI: 10.1109/TCSI.2008.212213).

[23] D. E. Marelli et al.: “Hybrid Filterbank ADCs With Blind Filterbank Estimation,” IEEE Trans. Circuits Syst. I, Reg. Papers 58 (2011) 2446 (DOI: 10.1109/TCSI.2011.2123750).

[24] S. R. Velazquez, et al.: “A hybrid filter bank approach to analog-to-digital conversion,” Proc. IEEE-SP Int. Symp. Time-Frequency Time-Scale Anal. (1994) 116 (DOI: 10.1109/TFSAS.1994.67350).

[25] X. Yang, et al.: “Minimax design of digital FIR filters using linear programming in bandwidth interleaving digital-to-analog converter,” IEICE Electron. Express 15 (2018) 20180565 (DOI: 10.1587/elex.15.20180565).

[26] L. Yin, et al.: “Optimization of synthesis filters for hybrid filter bank DACs,” IEICE Electron. Express 16 (2019) 20190053 (DOI: 10.1587/elex.16.20190053).

[27] X. Yang, et al.: “Minimax and WLS designs of Digital FIR Filters using SOCP for Aliasing Errors Reduction in BI-DAC,” IEEE Access 7 (2019) 11722 (DOI: 10.1109/ACCESS.2019.2891974).

[28] L. Yin, et al.: “An integrated digital pre-compensation framework for Hybrid-Filter-Bank DAC,” IEEE AU-TOTESTCON (2019) 1 (DOI: 10.1109/AUTOTESTCON.2019.8961080).

[29] X. Yang, et al.: “Estimation and compensation methods of time delay and phase offset in hybrid filter bank DACs,” Electron. Lett., 54 (2018) 806 (DOI: 10.1049/el.2018.0937).

[30] J. Deveugele, et al.: “Parallel-path digital-to-analog converter for Nyquist signal generation,” IEEE J. Solid-State Circuits 7 (2004) 1073 (DOI: 10.1109/JSSC.2004.829968).

[31] G. Golub and W. Kahan: “Calculating the Singular Values and Pseudo-Inverse of a Matrix,” Journal of the Society for Industrial and Applied Mathematics, Series B: Numerical Analysis 2 (1965) 205 (DOI: 10.1137/0702016).