Large-Scale-Compatible Stabilization of a 2D Semiconductor Platform toward Discrete Components

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Atomically thin 2D materials have drawn considerable attention in the past years with potential ranging from transistors to optoelectronics. As such, they are now foreseen as strong candidates for epitaxy-free technologies and the tetrad of size-weight-power-and-cost (SWAP-C) reduction. Targeting radiofrequency (RF) applications, the 2D semiconducting transition metal dichalcogenides (TMDC) family can offer the opportunity of wide tunability of their electronic properties, providing a large variety of band gaps. However, evaluation and integration of those materials into discrete components requires a stabilization of their properties. This work focuses on the evaluation of a large-scale compatible fabrication/passivation process on large area (>1000 μm²) monolayers of the prototypical 2D semiconductor MoS2. The process is developed including pre- and post-patterning protection/passivation layers. It is shown to reduce the initial natural p-doping of the sample, leading to lower transistor threshold voltages, a 10^6 I_{ON}/I_{OFF} ratio, and an effective averaged field-effect mobility under ambient conditions of 20 cm² V⁻¹ s⁻¹ (up to 35 cm² V⁻¹ s⁻¹ for some devices), which represents an increase by a 40-fold factor compared to a conventional process carried on the large scale platform. This work represents an important step toward the integration of 2D TMDCs in discrete RF circuits and components.

1. Introduction

Since the discovery of graphene in 2004,[1] 2D materials have raised a huge interest in many fields as electronics,[2–6] spintronics,[7,8] optoelectronics,[9–11] radiofrequencies,[12–14] and so on. It was highlighted that integrating those materials into radiofrequencies (RF) applications would allow significant size-weight-power-and-cost (SWAP-C) reduction.[15,16] Such an interest can be closely related to their outstanding 2D material nature. In particular, compared to III-V semiconductors, 2D materials are epitaxy-free (with low thermal budget), CMOS compatible (easily transferable to any compound), and allow low cost fabrication while enabling stacking into heterostructures to develop new functionalities.[17] Among them, a new generation of 2D semiconductors has emerged, widening the perspectives introduced with graphene. TMDCs have a sizable bandgap of 1–2.5 eV and therefore exhibit pronounced drain current saturation, where the main disadvantage of graphene is overcome. Beyond allowing simultaneous GHz operation frequency and power gain, their gap modularity should give a wide range of options for, channel resistance, length, ON/OFF ratio, and power gain for the best device compromise. Molybdenum disulphide (MoS2) is probably their most prototypical example with a mobility expected to reach up to ≈500 cm² V⁻¹ s⁻¹.[18] A striking particularity of MoS2 (and of 2Ds in general) is the tunability of its electronic properties. For example, its bandgap can be tailored from 1.29 eV for the bulk to 1.90 eV for the monolayer.[19] Such an interest can be closely related to the perspectives introduced with graphene. TMDCs have a sizable bandgap of 1–2.5 eV and therefore exhibit pronounced drain current saturation, where the main disadvantage of graphene is overcome. Beyond allowing simultaneous GHz operation frequency and power gain, their gap modularity should give a wide range of options for, channel resistance, length, ON/OFF ratio, and power gain for the best device compromise. Molybdenum disulphide (MoS2) is probably their most prototypical example with a mobility expected to reach up to ≈500 cm² V⁻¹ s⁻¹.[18] A striking particularity of MoS2 (and of 2Ds in general) is the tunability of its electronic properties. For example, its bandgap can be tailored from 1.29 eV for the bulk to 1.90 eV for the monolayer.[19] Furthermore, as the needs for multifunctional radar and wireless communications systems continue to grow, complex RF front end modules are required to enable reconfigurable and multiband operations. This leads to increasing demands on each component in the signal chain. Hence, the next technological platform should provide reduced size, increased power efficiency, and reconfigurability among other aspects. 2Ds, such as MoS2, offer opportunities toward exploring these applications.[19,20] Importantly, while being epitaxy-free among other advantages, the thickness control at atomic precision allows 2D materials to bring new opportunities when compared to III-V materials. Nevertheless, due to their 2D nature, their properties are highly disturbed by their interaction with the environment. Hence, reaching a stabilized large...
scale 2D semiconductor platform remains a key challenge for applications.

In this study, we introduce a large-scale compatible fabrication process-flow leading to properties stabilization of the prototypical MoS$_2$. In our work we focused on the fabrication process with this early technological implementation in mind. Thus, to properly develop the early technological bricks essential for our device realization, we defined four key requirements: i) work on relatively large surfaces of material (>1000 $\mu$m$^2$) to realistically integrate properties over large-scale material and extract a mean value relevant to the considered platform exploitation compatible with discrete component fabrication (Figure 1). ii) Be compatible with targeted applications (CMOS and RF) relying on a low-loss low-cost substrate already used in many RF applications.iii) Develop processes that are compatible with large-scale integration (at least 4-inches wafer). All our processes need to be scalable in terms of passivation, lithography processes for contacts deposition or etching. This is why we chose to focus on scalable physical vapor deposition (PVD) and atomic layer deposition (ALD) processes (Figures 2 and 3). iv) Stabilize the 2D material’s electronic properties with clear ON/OFF states (Figure 4). In the following, we detail our process step by step considering the necessary requirements stated above.

2. Results and Discussion

Following the first requirement (i), we focused on a large MoS$_2$ surface with a size on par with crystals domains reached by CVD processes but achieved from bulk crystals thanks to an adapted exfoliation process as exfoliated material

![Figure 1. a) Schematics of the MoS$_2$ monolayer modified exfoliation process to obtain large surface flakes. b) Optical image of a monolayer MoS$_2$ on an RF compatible substrate. The whole surface is covered with MoS$_2$. A specific zone with a scratch is selected for the Raman map in (d) to show some contrast. c) Corresponding Raman spectrum of MoS$_2$ monolayer. d) Large Raman mapping of the A$'$_1 mode intensity (red for high intensity to black for zero intensity) performed on the highlighted part of the image in (b) and showing high homogeneity of the MoS$_2$ monolayer. e) Photoluminescence spectrum corresponding to MoS$_2$ monolayer.](image-url)
quality remains the reference for the field. Crucially, we took care that our process remained fully compatible with any future emerging large-scale 2D material source. Since interlayer force for MoS2[29] (29 × 1018 N m−3) is stronger than for graphene[30] (12.8 × 1018 N m−3), the yield of thin flakes of MoS2 resulting from tape method exfoliation[31] is poor.[31] To alleviate this issue we opted for a modified exfoliation process flow following the work of Desai and coworkers.[32] This process is schematized in Figure 1a. First, bulk material is exfoliated from the crystal using a standard scotch tape exfoliation technique. We then evaporate a layer of gold (≈100 nm) on top of the MoS2 which bonds with the chalcogen (sulfur) atoms of the upper layer. This is the key step of this process as the interaction between chalcogen and gold is known to be stronger than van der Waals forces between the MoS2 layers.[33] This allows us to selectively exfoliate the topmost monolayer of MoS2 using a thermal release tape (TRT). Then, we transfer the MoS2/Au/TRT stack onto the targeted HR-Si/SiO2 substrate. The TRT is heated (∼90 °C) to release Au and underlying MoS2 onto the substrate. We used a KI/I2 wet etch diluted in water to etch Au without damaging MoS2. Finally, we end up with large monolayers of MoS2 on HR-Si/SiO2 substrate. TRT process is a solution we adopted to derive a reference exfoliated crystal on scales large enough to assess our encapsulation approach. While this whole procedure already allows to produce devices on small-scale for discrete components demonstrators—a crucial starting point for industrial developments—we envision it to be applied to any emerging large scale 2D fabrication.

We present in Figure 1b–e characterization of the MoS2 transferred on the HR-Si/SiO2 substrate. Figure 1b displays an optical image of the derived MoS2 layer with a feeble contrast pointing to its monolayer nature. The Raman spectrum of this layer (514 nm laser) under ambient conditions is shown in Figure 1c. The difference between A₁’ and E’ modes (Δω = 175 cm−1) confirms the presence of a monolayer.[34] Additionally, a map of the Raman A₁’ mode intensity is presented in Figure 1d highlighting the flake homogeneity. In Figure 1e the flake photoluminescence (PL) spectrum is presented where a direct bandgap of ~1.85 eV, consistent with reported literature value for the monolayer, can be clearly observed.[35] All these characterizations confirm the presence of a monolayer with a surface of about 10⁴ μm², 3–4 orders of magnitude larger than the standard exfoliation approach.

Since conventional O₂ plasma treatment classically used in microelectronics to remove residual resist after lithographic processes would lead to etch the MoS2,[36] a classical fabrication process (Figure 2a) resulted in devices with really high contact resistances (>10 GΩ μm) not allowing electrical characterization. To overcome this issue, we developed the protection/passivation process described in Figure 2b starting from the 2D layer on HR-Si substrates to follow requirement (ii). The next steps were developed following requirement (iii) of choosing processes that are compatible with large-scale integration. First, we deposited a thin aluminum layer by PVD and we further oxidized it in air, resulting in a continuous protection layer of ~1 nm of alumina (Al₂O₃) over the sample. This protection layer was shown not to damage 2D materials[38,37] but also to prevent their degradation under ambient atmosphere.[38] This allows to protect MoS2 ahead of the technological steps. For example, during a lift-off process, the MoS2 layer is never directly in contact with the resist. The MoS2 layer was then etched to define the device channel. The next step was contact metal deposition. Here, the protection layer was removed by using tetramethylammonium hydroxide (TMAH) diluted in water (1:4) before performing the metal evaporation. Finally, we encapsulated the device in a passivation layer consisting in 10 nm of Al₂O₃ grown by atomic layer deposition (ALD). In the following we describe the characterization of this protection/passivation process and show that it leads to a MoS2 platform stabilized against environment.

We performed Raman and PL spectroscopies after both the protection and passivation steps in order to see how the MoS2 properties were influenced. We observed that Raman spectra (see Figure 3b) were affected by the protection/passivation process. The process induced a red-shift of the A₁’ mode but no obvious modification for the E’ mode which could correspond to a decrease of the environmental p-type dopant.[39] A special representation allows extraction of the MoS2 doping variation by taking into account strain variations.[40] It consists in representing the A₁’ as a function of the E’ mode (see Figure 3a). In our case, we obtain a reduction of the environmental p-type...
doping. In Figure 3c,d the PL spectroscopy of monolayer MoS₂ is presented at each process step and we can see a PL intensity drop as well as red-shift of the bandgap which can be attributed to the same doping modification observed in Raman spectroscopy. This is in-line with previous studies showing that this protection/passivation process affects graphene doping, reducing the p-doping caused by ambient conditions.

Finally, we present electrical transport characterization. Thanks to this protection/passivation process, we could observe a contact resistance improvement allowing to electrically characterize our device. We chose to realize a Hall bar design where probes are deported as shown in Figure 4a: this results in more robust non-invasive measurements. We use a back-gate voltage applied directly to the substrate that allows us to extract the threshold voltage ($V_T$), $I_{ON}/I_{OFF}$ ratio and four-probe field-effect carrier mobility ($\mu_{ef}$) of the device. Figure 4b shows the drain–source current versus backgate voltage with a constant drain-source bias of 5 V. We can notice that adding the passivation layer on top of the channel, reduces the absolute value of the electric field corresponding to the threshold voltage $V_T$ by 50% from 0.26 V nm$^{-1}$ to approximately 0.13 V nm$^{-1}$ (for a 780 nm SiO₂ layer). More importantly, the passivation layer increases the $I_{ON}/I_{OFF}$ ratio by two orders of magnitude to a value of $\approx 10^6$, allowing higher current intensity through the channel. Already an $I_{ON}/I_{OFF}$ ratio in the range of $10^4$ to $5 \times 10^7$ (depending on requirements, high performances or low-power) is in-line with requirements for FETs to be used in CMOS logic and we note that even further improvements can be foreseen. This is well in agreement with the observed reduction of environmental p-doping of the n-type MoS₂ channel by Raman and PL analyses, as explained before (Figure 3) allowing us to reach higher $I_{ON}$. We note that this
result has been well reproduced showing the stabilization of the properties with similar mobility, threshold voltage, and saturation velocity being extracted: the variability is reduced when using our protection/passivation scheme (see Figure S1, Supporting Information). This result has been well confirmed on >10 devices without noticing a change in extracted characteristics, confirming that fabricated long devices give a reliable averaged response. Next, we extracted the four-probe field-effect carrier mobility (μeff) of our devices following Lembke et al.[42] The four-probe conductivity σ of the MoS2 monolayer was found from \[ \sigma = \frac{L_{\text{CH}} I_{\text{DS}}}{W \Delta V} \], where \( L_{\text{CH}} \) is the length of the channel separating the voltage probes (=12 μm), \( W \) is the width of this channel (=3 μm), \( I_{\text{DS}} \) is the drain–source current, and \( \Delta V \) is the potential drop between the two central voltage probes (see Figure 4a). From this conductivity, the extracted four-probe field-effect carrier mobility was derived using \( \mu_{\text{eff}} = \frac{1}{C_{\text{ox}}} \frac{d}{dV_{\text{BG}}} \), where \( C_{\text{ox}} \) is the oxide capacitance and \( V_{\text{BG}} \) is the applied backgate voltage. In the following discussion, we assume the capacitance to be \( C_{\text{ox}} = \frac{E_{\text{ox}}}{d} = 4.5 \times 10^{-3} \text{ F m}^{-2} \) (with SiO2 dielectric constant \( \varepsilon_r = 3.9 \) and thickness \( d = 780 \text{ nm} \)).

In the inset of Figure 4b, we can see a comparison of the different four-probe field-effect mobilities that can be extracted as a function of the different fabrication processes used. The standard process without any protection is given as reference, some studies have already shown the striking potential of CVD grown layers with large mobilities.[51–58]

3. Conclusion

In conclusion, we present in this study a process flow toward the implementation of a large-scale compatible 2D semiconductor platform constrained by key technical requirements toward integration in small series of discrete functional devices. The results we present in this study would certainly benefit many different fields such as RF,[12,13] digital applications,[99,100] analog devices,[101] optoelectronics,[63] spintronics,[8] and beyond. We made use of large 2D layers compatible with the definition of discrete components and basic cascading, CMOS and RF compatible substrates, scalable PVD and ALD processing, and aimed stabilized ON/OFF conditions. Following these requirements, we already measured transport characteristics equivalent to much shorter exfoliated 2D MoS2 channels previously reported and a 40-fold improvement of the four-probe field-effect mobility. Our successful protection/passivation results, complementary to first large-scale 2D semiconductor growths[27,28] and test-line wafer scale device integrations[26] reported recently, highlight a very positive path for the definition of highly-efficient large-scale 2D semiconductor platforms.

4. Experimental Section

Device Fabrication: Devices were fabricated on relevant SiO2/HR-Si substrate. As an initial fabrication step, Ti/Pt alignment marks were applied with a constant source–drain bias (VDS) of 5 V for the protected sample with and without passivation. The protection/passivation process allows to restore a large ON/OFF ratio. Inset: relative four-probes field-effect mobility (μeff) comparison for the different fabrication processes. The protection/passivation process leads to a 40-fold increase in the mobility.

![Figure 4](https://www.advancedsciencenews.com/content/21/6/7111113/fig4/fig4.jpg)

Figure 4. a) Optical image of a device with a long monolayer MoS2 channel. b) Drain–source current intensity (I DS) versus backgate electric field (V BG) applied with a constant source–drain bias (V DS) of 5 V for the protected sample with and without passivation. The protection/passivation process allows to restore a large ON/OFF ratio. Inset: relative four-probes field-effect mobility (μeff) comparison for the different fabrication processes. The protection/passivation process leads to a 40-fold increase in the mobility.
defined on the substrate. These were designed to resist the gold layer etching step during 2D deposition process. Further device structures were defined by PVD metal depositions and lift-off processes.

**Dielectric Deposition:** For the PVD deposition, the samples were transferred under inert atmosphere into an ultra-high vacuum evaporator system (base pressure 10⁻⁸ mbar). A 1 nm-thick layer of metallic Al was evaporated on the sample (the deposited thickness and the deposition rate of 40 pm s⁻¹ were controlled using a quartz crystal microbalance) and was then exposed to air so that the Al was oxidized instantly to form an Al₂O₃ passivation layer.

**Electrical Characterization:** All electrical measurements were performed under ambient conditions at room temperature using a Keithley 4200 electrical characterization bench.

**Supporting Information**
Supporting Information is available from the Wiley Online Library or from the author.

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**Conflict of Interest**
The authors declare no conflict of interest.

**Data Availability Statement**
The data that support the findings of this study are available from the corresponding author upon reasonable request.

**Keywords**
2D semiconductors, MoS₂, transition metal dichalcogenides, radiofrequency, passivation

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