Effects of Post-Deposition Annealing Time in Forming Gas Ambient on Y$_2$O$_3$ Films Deposited on Silicon Substrate

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Abstract. Effects of post-deposition annealing (PDA) time (15, 30, and 45 min) at 800˚C in forming gas (95% N$_2$-5% H$_2$) ambient was systematically studied for RF-magnetron sputtered Y$_2$O$_3$ films on n-type Si(100) substrate. X-ray diffraction characterization has revealed the detection of Y$_2$O$_3$ phase oriented in (400), (440), (541), and (543) planes for all of the investigated samples. In addition, capacitance-voltage characteristics of the investigated Al/Y$_2$O$_3$/Si-based metal-oxide-semiconductor capacitors were also presented in this work.

1. Introduction

The continuous downsampling of silicon (Si)-based metal-oxide-semiconductor (MOS) devices for performance enhancement throughout the years has pushed SiO$_2$ thickness to its limit, wherein further downsampling of SiO$_2$ thickness would contribute to high leakage current due to direct tunneling mechanism [1]. In order to circumvent this issue, there is a need of replacing the existing low dielectric constant ($k$) SiO$_2$ with high-$k$ materials, such as HfO$_2$, Al$_2$O$_3$, ZrO$_2$, CeO$_2$, and Y$_2$O$_3$ as passivation layer for Si-based MOS devices [2-5]. Of these high-$k$ materials, Y$_2$O$_3$ possesses fascinating properties of high-$k$ value ($k = 15-18$), large band gap (~ 5.5 eV), large conduction band offset (~ 2.3 eV), low lattice mismatch and good thermal stability with Si [6,7].

Previous investigation has revealed an alteration on electrical characteristics of Y$_2$O$_3$ films deposited on Si substrate through post deposition annealing (PDA) in various types of ambient, which include argon, nitrogen, forming gas (hydrogen + nitrogen), oxygen, and nitrous oxide at 1000˚C [7,8]. Of the investigated PDA ambient, Y$_2$O$_3$/Si system subjected to forming gas ambient PDA has revealed the acquisition of the lowest capacitance as well as the presence of more oxygen related defects in the Y$_2$O$_3$ films than that of Y$_2$O$_3$ films subjected to PDA in argon, oxygen, and nitrous oxide [7,8]. In addition, a poorer interfacial quality was attained by Y$_2$O$_3$/Si system subjected to PDA in forming gas ambient, wherein a higher interface trap density and total interface trap density was attained by this sample when compared with oxygen and nitrous oxide annealed Y$_2$O$_3$/Si system [7]. However, Y$_2$O$_3$/Si system subjected to forming gas annealing has attained a better interfacial quality than argon and nitrogen ambient, which could be related to the existence of hydrogen to passivate the interface related defects as well as repairing the broken bonds in Y$_2$O$_3$ films [7]. Therefore, it was proposed in this work to reduce the PDA temperature to 800˚C to minimize the formation of interfacial layer that would eventually influence the acquisition of capacitance at accumulation level. Effects of PDA time...
(15, 30, and 45 min) at 800°C in forming gas (95% N₂-5% H₂) ambient on the morphological, structural, and electrical characteristics of RF-magnetron sputtered Y₂O₃ gate on Si substrate are systematically investigated.

2. Experimental Process

3 inch n-type Si wafer was diced into smaller pieces (1 x 1 cm²) and these samples were subjected to RCA cleaning. The RCA cleaned samples were dipped into HF/H₂O solution with ratio of 1:50 prior to the deposition of Y₂O₃ films using RF-magnetron sputtering. Subsequently, these samples were directly loaded into the RF-magnetron sputtering machine (Edwards A500) and the thickness of the deposited 5 nm thick Y₂O₃ films was monitored by a quartz crystal monitor (FTM-7). The detailed of deposition process of Y₂O₃ films has been reported in [6]. The as-deposited Y₂O₃ samples were subjected to post deposition annealing at 800°C in forming gas (95% N₂-5% H₂) ambient for 15, 30, and 45 min. A heating and cooling rate of approximately 10°C/min were used. In order to fabricate a metal-oxide-semiconductor (MOS) test structure, a blanket of aluminum (Al) was deposited on top of the Y₂O₃ films using thermal evaporator (AUTO 306) and photolithography process was employed to form an array of Al gate electrodes with area of 0.0025 cm². The backside of Si substrate was deposited with a layer of Al using thermal evaporator. Phase and orientation of the investigated samples were characterized using X-ray diffraction (XRD; P8 Advan-Bruker). The capacitance-voltage characteristics of the investigated samples were measured using inductance-capacitance-resistance (LCR) meter (Agilent 4284A).

3. Results and discussion

Figure 1 presents XRD patterns of the investigated samples subjected to different post deposition annealing (PDA) time from 15 to 45 min. The investigated samples have revealed the detection of 4 diffraction peaks with regards to cubic phases of Y₂O₃ (ICCD file no. 00-041-1105) that were oriented in (400), (440), (541), and (543) planes. In addition, Y₂Si₃O₇ phase oriented in (130) plane was also detected for all samples and an increment in the intensity of this phase was perceived as a function of PDA time. The detection of Y₂Si₃O₇ phase for all samples would propose the formation of interfacial layer comprising of a mixture Y₂SiO₃ and SiO₂. It was reported previously that Y₂SiO₃ was formed through the reaction between Y₂O₃ and SiO₂. Therefore, the attainment of a higher intensity of peak related to Y₂Si₃O₇ phase as PDA time was prolonged would indicate the formation of interfacial layer comprising of more Y₂Si₃O₇ phase than other samples.

High frequency (1 MHz) capacitance-voltage measurements were performed on the investigated samples from -4V to +4V and the acquired results are presented in Figure 2. Negative flatband voltage shift (∆V FB) was observed for all of the investigated samples indicating the presence of positive charged traps in Y₂O₃ films [7,8]. An increment in PDA time from 15 to 30 min has contributed to the formation of a higher density of positively charged traps due to the acquisition of a larger ∆V FB. Hence, it was believed that the increment of PDA time to 30 min did not contribute to the formation of thicker interfacial layer as a higher accumulation level of capacitance was attained by this sample when compared to Y₂O₃ films PDA at 15 min. The acquisition of a higher intensity of peak related to Y₂Si₃O₇ phase at 30 min would suggest that the increment of PDA time from 15 min would enhance the reaction of Y₂O₃ and SiO₂ to form more Y₂Si₃O₇ compound. However, a reduction in ∆V FB as well as the attainment of the lowest accumulation level of capacitance was perceived as PDA time was prolonged to 45 min. The attainment of the lowest accumulation level of capacitance for this sample would indicate the formation of thickest interfacial layer, wherein more oxygen vacancies were formed in Y₂O₃ films. Hence, more oxygen was dissociated from Y₂O₃ films and diffused inward to react with Si substrate to form interfacial layer comprising of Y₂Si₃O₇ and SiO₂.
The generation of more positively charged oxygen vacancies in Y$_2$O$_3$ films formed at 45 min could be supported by the acquisition of a larger $\Delta V_{FB}$ at 45 than 15 min. The estimation of traps present in Y$_2$O$_3$ films could be verified through the calculation of effective oxide charge ($Q_{\text{eff}}$) using the following equation [10]:

$$Q_{\text{eff}} = \frac{\Delta V_{FB} C_{\text{ox}}}{q A}$$

(1)

where $C_{\text{ox}}$ is the maximum accumulation capacitance, $q$ is the electronic charge, and $A$ is the capacitor area. Figure 3 shows the calculated $Q_{\text{eff}}$ value of the investigated samples.
Terman’s method has been employed to extract interface trap density ($D_{it}$) of the investigated samples using the following equation [11]:

$$D_{it} = \frac{C_{ox}d(\Delta V_g)}{qA_d(\Psi_s)}$$

(2)

where $\Delta V_g = V_g - V_g(\text{ideal})$ is the voltage shift of the experimental curve from the ideal curve, $V_g$ is the experimental gate voltage, and $\Psi_s$ is the surface potential of Si at a specific gate voltage. Figure 4 presents the calculated $D_{it}$ values as a function of energy trap level ($E_c-E_t$) for the investigated samples. Of these investigated samples, sample subjected to PDA for 15 min has attained the lowest $D_{it}$ due to the formation of a thinner interfacial layer when compared with sample subjected to PDA for 30 and 45 min. Although a thicker interfacial layer was postulated to be formed at the longest PDA time (45 min), a lower interface trap density was acquired by this sample than sample subjected to PDA for 30 min. This could be explained through the formation of interfacial layer comprising of more $Y_2Si_2O_7$ phase that would contribute to an improvement in interfacial quality.
4. Conclusion
Sample subjected to PDA at 15 min has demonstrated the attainment of the lowest $Q_{\text{eff}}$ and $D_{\text{it}}$. Prolonging the PDA time beyond 15 min has triggered the formation of thicker interfacial layer, wherein samples PDA at 30 and 45 min have attained higher $Q_{\text{eff}}$ and $D_{\text{it}}$ than sample PDA at 15 min.

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References
[1] Quah H J, Hassan Z and Lim W F 2019 Appl. Surf. Sci. 493 411-22
[2] Sen B, Wong H, Filip V, Choi H Y, Sarkar C K, Chan M, Kok C W, Poon M C 2006 Thin Solid Films 504 312-6
[3] Nam W H, Rhee S W 2004 Chem. Vapor Dep. 10 201-5
[4] Lappalainen J, Tuller H L and Lantto V 2004 J. Electroceramics 13 120-33
[5] Quah H J, Hassan Z, Yam F K, Ahmed N M, Salleh M A M, Matori K A, Lim W F 2017 J. Alloys Compd. 695 3104-15
[6] Quah H J and Cheong K Y 2015 J. Exp. Nanosci. 10, 19-28
[7] Quah H J and Cheong K Y 2013 Nanoscale Res. Lett. 8 53
[8] Quah H J and Cheong K Y 2012 J. Alloys Compd. 529 73-83
[9] Quah H J and Cheong K Y 2011 Mat. Chem. Phys. 130 1007-15
[10] Cheong K Y, Dimitrijiev S, Han J and Harrison H B 2003 J. Appl. Phys. 93 5682-6
[11] Schroder D K 1998 Semiconductor material and device characterization (New York: John Wiley & Sons)