A 1.8-nW sub-1-V self-biased sub-bandgap reference for low-power systems

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Abstract An ultra-low power sub-bandgap voltage reference circuit fabricated in a standard 0.18-µm CMOS technology is proposed. Exploiting the negative temperature characteristics of VGS and VTH, a novel self-biased circuit configuration with a combination of a parasitic BJT and MOSFETs is employed to achieve a temperature-compensated sub-bandgap voltage reference with nanowatt power dissipation. The measurement results show that, the proposed circuit provides an average reference voltage of 261.6 mV with a variation coefficient of 0.86%. The line regulation (LR) is 0.26%/V in a supply voltage range of 0.9 V to 1.8 V at 27°C, and the power supply rejection ratio (PSRR) is ~49 dB at 100 Hz. With one-time trimming, measurements performed over a set of 18 samples shows an average temperature coefficient of 25.9 ppm/°C in a temperature range from ~20 to 100°C. The power dissipation is 1.8 nW with a supply voltage of 0.9 V at 27°C. The chip area is 0.0038 mm².

Keywords: ultra-low power, sub-bandgap voltage reference, CMOS, temperature coefficient, chip area

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

With the rapid development of low-power Internet of Things (IoT) applications, ultra-low power and small size are urgently required to extend system lifetime and improve the portability of devices [1, 2, 3]. Conventional bandgap references can achieve high accuracy [4, 5, 6, 7, 8, 9, 10, 11, 12, 13]. However, their power dissipation is typically tens of µW to hundreds of µW, and the complex structure using resistors inevitably leads to a large chip area. This makes them unattractive for ultra-low power applications.

Compared to bandgap references, subthreshold voltage references (SVR) are more suitable for ultra-low-power systems as they consume ultra-low power at the nW level[14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28]. A basic temperature compensation strategy of all-MOSFETs voltage references is that using a biased current (proportional to $I^2$) to extract the threshold voltage from the $V_{GS}$ of a diode-connected MOSFET [14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24]. The temperature characteristics of the current and $V_{GS}$ can compensate for each other to improve temperature stability. Unfortunately, the biased current generator is usually implemented with special devices such as high $V_{TH}$ MOSFET, isolated MOSFET, and DT莫斯FEt, which inevitably increases the cost and decreases the process compatibility because of extra fabrication steps. Design in [15] achieves excellent temperature stability (15 ppm/°C) without any special devices, but a complex structure with amplifiers and multiple current branches inevitably leads to extra power consumption (the branch current is 36 nA, and total power dissipation is 300 nW@1.4 V) and big chip area. Voltage references consist of MOSFETs except for the bipolar transistors [25, 26, 27]. Employing a high-order temperature compensation technique, design in [25] obtains a bandgap voltage with low TC. But this solution requires the supply voltage above 2 V. To decrease supply voltage, a sub-bandgap reference using a current generator, voltage divider, and PTAT voltage generator is proposed, which can operate at a sub-1-V supply [27]. Designs in [29, 30, 31] are implemented with resistors and complex circuit configurations, which directly lead to a large chip area.

According to the above review, we can find that it is still a huge challenge to achieve high temperature stability, small chip area, and good process compatibility for ultra-low power reference designs. In this work, we propose a low-power sub-bandgap reference with a new self-biased circuit, which consists of a parasitic PNP transistor and MOSFETs. A temperature-compensated reference voltage is achieved by exploiting the negative temperature characteristics of $V_{BE}$ and $V_{TH}$. Without any special MOSFETs, resistors, and amplifiers, the proposed compact topology is conducive to good process compatibility and small chip area. With the same power dissipation level, measurement results indicate that the proposed design achieves lower TC and smaller chip area than the previous solutions.

2. Circuit design

The topology of the proposed voltage reference is shown in Fig. 1. The start-up circuit on the left consists of $M_{S1}$, $M_{S2}$, $M_{S3}$, $M_{S4}$, and $C_{S1}$, which is used to inject currents during the power-up stage to get rid of the locked zero-current state in the current mirror. The main circuit consists of $M_{P1}$, $M_{P2}$, $M_{N1}$, $M_{N2}$, $M_{N3}$, and $Q_{1}$. In Fig. 1, all the MOSFETs are operated in the subthreshold region to ensure low power operation. Transistors $M_{P1}$ and $M_{P2}$ are current mirrors with the same size. The transistor $Q_{1}$ is the parasitic diode-connected PNP transistor. Based on the proposed circuit configuration in Fig. 1, after current $I_{S}$ injecting into the transistor $Q_{1}$, a complementary-to-absolute-temperature (CTAT) voltage $V_{TH}$ is generated at the gate terminal of $M_{N1}$. The current $I_{S}$ flows through $M_{N1}$, $M_{N2}$, and $M_{N3}$. The gate-
source voltages of $M_{N1}$ and $M_{N2}$ are also CTAT voltage. A temperature-compensated reference voltage can be obtained at the drain of $M_{N3}$ with the difference between two kinds of CTAT voltages. For a subthreshold MOSFET, if $|V_{DS}|$ is larger than 200 mV, the relationship between drain current $I_D$ and gate-source voltage $V_{GS}$ is approximately given as [15, 32]

$$I_D = K I_0 \exp \left( \frac{V_{GS} - V_{TH}}{\eta V_T} \right)$$  

where $I_0$ is equal to $\mu C_{ox}(\eta - 1)V_{DS}^2$, $\mu$ is the carrier mobility, $C_{ox}$ is the gate oxide capacitance, $\eta$ is the sub-threshold slope factor, $V_T = k_B T/q$ is the thermal voltage, $k_B$ is the Boltzmann constant, $T$ is the absolute temperature, $q$ is the electron charge, $K$ is the aspect ratio of channel width and length, $V_{GS}$ is the gate-source voltage, $V_{TH}$ is the threshold voltage. Among these parameters, $\mu$ and $V_{TH}$ are temperature-dependent. In Fig. 1, the current $I_1$ can be expressed as

$$I_1 = K I_0 \exp \left( \frac{V_{GS1} - V_{THN1}}{\eta V_T} \right)$$

$$I_2 = K I_0 \exp \left( \frac{V_{GS2} - V_{THN2}}{\eta V_T} \right)$$

$$I_3 = K I_0 \exp \left( \frac{V_{GS3} - V_{THN3}}{\eta V_T} \right)$$

The gate-source voltages of $M_{N1}$, $M_{N2}$, and $M_{N3}$ can be respectively given as

$$V_{GSN1} = \eta V_T \ln \left( \frac{I_1}{K I_0} \right) + V_{THN1}$$

$$V_{GSN2} = \eta V_T \ln \left( \frac{I_2}{K I_0} \right) + V_{THN2}$$

$$V_{GSN3} = \eta V_T \ln \left( \frac{I_3}{K I_0} \right) + V_{THN3}$$

where $V_{GSN2} = V_{DS2}$, $V_{GSN3} = V_{DS3} = V_{REF}$. Without consideration of the mismatch of the current mirrors, the current $I_1$ is equal to $I_2$. The emitter-base voltage of $Q_1$ can be given as

$$V_{EB1} = V_{REF} + V_{DSN2} + V_{GSN1}$$

According to the relationship proposed in [33], the emitter-base voltage of a diode-connected transistor is given as

$$V_{EB} = V_T \ln \left( \frac{I_1}{I_S} \right),$$

$$I_S = CT^\alpha \exp \left( -\frac{V_0}{V_T} \right)$$

where $I_S$ is the saturation current, $C$ is a temperature-independent constant, $\alpha$ is a process-dependent constant with an approximate value between 3.6 and 4, $V_0$ is the extrapolated bandgap voltage of silicon at 0 K. Based on Eq. (3) to Eq. (7), the current $I_1$ can be derived as

$$\ln (I_1) = \eta V_T \ln \left( K_1 K_2 K_3 I_0^\eta \right) - V_T \ln (I_S) - V_{THN1} - V_{THN2} - V_{THN3}$$

$$\frac{(3\eta - 1) V_T}{V_T}$$

The reference voltage can be derived as

$$V_{REF} = V_{EB} - V_{GSN} - V_{DSN}$$

$$= \frac{\eta}{3\eta - 1} \left( V_0 - V_{THN1} - V_{THN2} - V_{THN3} \right)$$

$$\eta (\lambda_1 + \lambda_2) (1 - 2\eta) \lambda_3 + \ln \left( \frac{(K_1^\eta K_2^{2\eta - 1})}{K_3^{2\eta - 1}} \right) \eta k_B / q T$$

$$\frac{3\eta - 1}{3\eta - 1}$$

According to [15], the threshold voltage can be given as

$$V_{TH} = V_{TH0} - \lambda T$$

where $V_{TH0}$ is the threshold voltage at 0 K (hypothetical), $\lambda$ is the TC of $V_{TH}$. Due to the body effect and different device sizes, $V_{TH0}$ and $\lambda$ of $M_{N1}$, $M_{N2}$, $M_{N3}$ are all different. Substituting (10) into (9), $V_{REF}$ can be given as

$$V_{REF} = \frac{\eta}{3\eta - 1} \left( V_0 - V_{THN10} - V_{THN20} - V_{THN30} \right) + V_{THN30}$$

$$\eta (\lambda_1 + \lambda_2) (1 - 2\eta) \lambda_3 + \ln \left( \frac{(K_1^\eta K_2^{2\eta - 1})}{K_3^{2\eta - 1}} \right) \eta k_B / q T$$

$$\frac{3\eta - 1}{3\eta - 1}$$

With proper adjustment of the ratio $(K_1 K_2)^\eta / K_3^{2\eta - 1}$, the linear term in Eq. (11) can be cancelled out. Neglecting the high-order temperature terms, Eq. (11) can be remodeled as

$$V_{REF} \approx \frac{\eta}{3\eta - 1} V_0$$

$$+ \frac{(2\eta - 1) V_{THN30} - \eta (V_{THN10} + V_{THN20})}{3\eta - 1}$$

$$\frac{3\eta - 1}{3\eta - 1}$$

Fig. 2 shows the simplified topology of voltage reference in Fig. 3 to further analyze the supply voltage stability. $R_{P1}$, $R_{N2}$, $R_{N3}$, and $R_{Q1}$ are the equivalent resistance of $M_{P1}$, $M_{N2}$, $M_{N3}$, and $Q_1$, respectively. $R_{GS1}$ and $R_{OP2}$ are the output resistance of $M_{N1}$ and $M_{P2}$, respectively.
there is a slowly small variation \((v_{dd})\) in the supply voltage, it will lead to a small changing current \((i_{out})\) and changing voltage \((v_{out})\) in the circuit. The gain from \(v_{out}\) to \(v_{dd}\) can be derived as following. The small-signal gate-source voltage of \(M_{P2}\) is given as
\[
v_{gsP2} = -i_{out} R_{P1} \tag{13}\]
The current flowing through \(r_{OP2}\) is expressed as
\[
i_{OP2} = \frac{v_{dd} - v_X}{r_{OP2}} \tag{14}\]
Based on the Kirchoff’s current law (KCL), the equation is given as
\[
v_{dd} - v_X + i_{out} R_{P1} G_{mP2} = \frac{v_X}{R_{Q1}} \tag{15}\]
Without consideration of the body effect of \(M_{N1}\), the equivalent trans-conductance of \(M_{N1}, R_{N2}\), and \(R_{N3} (G_{mN1})\) can be given as
\[
G_{mN1} = \frac{g_{mN1} r_{ON1}}{R_{N2} + R_{N3} + r_{ON1} + g_{mN1} r_{ON1} (R_{N2} + R_{N3})}
= \frac{i_{out}}{v_X} \tag{16}\]
From Eq. (15) and Eq. (16), Eq. (17) can be given as
\[
\frac{v_{out}}{v_{dd}} \approx \frac{R_{N3}}{r_{OP2}} \left( \frac{1}{G_{mN1} (r_{OP2} | R_{Q1})} - 1 \right)^{-1} \approx \frac{R_{N3} R_{Q1}}{r_{OP2} (R_{N2} + R_{N3} - R_{Q1})} \tag{17}\]
As we can observe in Eq. (17), the supply voltage stability increases as \(r_{OP2}\) becomes larger. To improve the performance of line regulation, the selection of a large transistor size is helpful to improve performance. The designed device parameters are shown in Fig. 1. The optimal parameters of the MOSFETs are designed under TT corner according to Eq. (11). However, process variation and the local mismatches of the MOSFETs worsen the temperature coefficient of the reference voltage. In order to correct the process variation and the mismatch effect, a 4-bit trimming circuit for \(M_{N3}\) is designed for the proposed voltage reference to correct the drift of temperature coefficient, as shown in Fig. 3.

3. Measurement results and discussion

The proposed voltage reference was fabricated in a 0.18-\(\mu m\), 1-poly, 4-metal standard CMOS process. Fig. 4 shows the die photograph and layout. The chip area is 0.00376 mm\(^2\) (= 47\(\mu m \times 80\mu m\)). An extra buffer was used to avoid unwanted loading effects during measurements. Fig. 5 shows the measured \(V_{REF}\) vs. temperature with four different supply voltages. The output voltages have similar temperature characteristics with different supply voltages. The average output voltage is about 264.6 mV at 27°C. The average temperature variation is 0.85 mV in a temperature range from \(-20\) to 100°C. The average temperature coefficient is 26.9 ppm/°C. Fig. 6 shows the measured \(V_{REF}\) vs. power supply at 27°C. The minimum required supply voltage for the normal operation is about 0.75 V. \(V_{REF}\) varies about 0.62 mV as supply voltage changes from 0.9 V to 1.8 V. Its line regulation is 0.26%/V. Fig. 7 shows the power supply rejection ratio (PSRR) at 27°C with a 0.9 V power supply. At 100 Hz, 1 kHz, and 10 kHz, the PSRR levels are −49 dB, −30 dB, and −28 dB, respectively. Fig. 8 shows the measured supply current as a function of temperature with four different supply voltages. The current is about 2 nA at room
Fig. 6 Measured $V_{\text{REF}}$ vs. power supply voltage at room temperature.

Fig. 7 Measured PSRR with supply voltage of 0.9 V.

Fig. 8 Measured current consumption vs. temperature at different power supply voltages.

Temperature and reaches the maximum of 10.4 nA at 100 °C. The power dissipation of the circuit with a 0.9 V power supply is 1.8 nW at room temperature. Fig. 9 shows the measured oscilloscope waveform at startup. It takes about 480 μs for the output reference to reach the final value. The measured value is much longer than the actual settling time of $V_{\text{REF}}$ because of the limitation of the employed buffer.

With one-time trimming, Fig. 10 shows the measured $V_{\text{REF}}$ vs. temperature for 18 samples on different chips from the same wafer. The supply voltage is set to 0.9 V. Temperature coefficients from 20.2 to 35.8 ppm/°C were observed in the 18 samples. The output voltages mostly fall between 258.5 mV and 266.7 mV at 27°C. The D2D variation in $V_{\text{REF}}$ is about 8.2 mV.

Fig. 11 and Fig. 12 show the distribution of $V_{\text{REF}}$ and its TC for the 18 samples. The mean value ($\mu$) and standard deviation ($\sigma$) are as follows:

- $\mu=261.6$ mV
- $\sigma=2.24$ mV

- $\mu=25.86$ ppm/°C
- $\sigma=4.63$ ppm/°C
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power CMOS voltage reference circuit based on thermal com-

Table 1: Comparison results with previous works in the literature.

| Designs | [1] | [15] | [16] | [27] | [31] | This work |
|---------|-----|-----|-----|-----|-----|----------|
| Years   | 2019 | 2009| 2011| 2013| 2020| 2021     |
| Technology (μm) | 0.18 | 0.35| 0.18| 0.35| 0.18| 0.18     |
| Supply Voltage (V) | 1.4-3.6 | 1.4-3 | 0.45-2 | 0.7-1.8 | 2-5 | 0.9-1.8 |
| Temp. Range (°C) | 0-100 | -20-80 | 0-125 | -40-120 | -45-125 | -20-100 |
| Ref. Voltage (mV) | 1250 | 745 | 263.5 | 548 | 1200 | 261.6     |
| Power Cons. (nW) | 0.033 | 300 | 2.6 | 100 | 192 | 1.8     |
| Mean TC (ppm/°C) | 31 | 15 | 165 | 114 | 32.7 | 25.9     |
| Line Reg. (%) | 0.31 | 0.002 | 0.44 | N/A | 0.058 | 0.26    |
| PSRR (dB/100kHz) | -41 | -45 | -45 | -62 | N/A | -49     |
| σV (%) | 0.8 | 0.87 | 3.88 | 1.05 | 0.17 | 0.86     |
| Setting time (ms) | 92.2 | N/A | N/A | N/A | N/A | 0.48    |
| #Samples | 60 | 17 | 40 | 9 | 30 | 18     |
| Chip area (mm²) | 0.002 | 5 | 0.055 | 0.043 | 0.024 | 0.063 | 0.003 |

The mean value and standard deviation of TC are 261.6 mV and 2.24 mV respectively, showing a variation coefficient (σ/μ) of 0.86%. This value is relatively small because the sample chips were fabricated from the same wafer. Besides, the output voltage is mainly the sub-bandgap voltage, which is less affected by process variation. The mean value and standard deviation of TC are 25.86 ppm/°C and 4.63 ppm/°C. Its variation coefficient is 17.9%. Table 1 summarizes the performance comparison results with state-of-the-art works in the literature. The proposed circuit design achieves good temperature stability and a small chip area with ultra-low power consumption. Compared to [1], the proposed sub-bandgap reference requires no native MOSFETs and shows an improved performance in TC, LR, settling time, and temperature range. Besides, the required supply voltage is below 1 V. As paid for the trade-off, the power consumption is increased from pW to nW and the area is increased by 1.5 times. Compared to [16], under the premise of the same power consumption, this work has great advantages in TC, LR, area consumption, and 3σ inaccuracy.

4. Conclusion

This letter proposes an ultra-low-power sub-bandgap voltage reference with a new self-biased circuit, which combines a parasitic BJT and MOSFETs to generate a temperature-compensated sub-bandgap reference voltage. Without any native MOSFETs, amplifiers, and resistors, the proposed design not only achieves nanowatt power consumption, but also shows competitive temperature stability, process compatibility, and chip area for low power IoT applications.
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