ParaLarH: Parallel FPGA Router based upon Lagrange Heuristics

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Abstract. Routing of the nets in Field Programmable Gate Array (FPGA) design flow is one of the most time consuming steps. Although Versatile Place and Route (VPR), which is a commonly used algorithm for this purpose, routes effectively, it is slow in execution. One way to accelerate this design flow is to use parallelization. Since VPR is intrinsically sequential, a set of parallel algorithms have been recently proposed for this purpose (ParaLaR and ParaLarPD).

These algorithms formulate the routing process as a Linear Program (LP) and solve it using the Lagrange relaxation, the sub-gradient method, and the Steiner tree algorithm. Out of the many metrics available to check the effectiveness of routing, ParaLarPD, which is an improved version of ParaLaR, suffers from large violations in the constraints of the LP problem (which is related to the minimum channel width metric) as well as an easily measurable critical path delay metric that can be improved further.

In this paper, we introduce a set of novel Lagrange heuristics that improve the Lagrange relaxation process. When tested on the MCNC benchmark circuits, on an average, this leads to halving of the constraints violation, up to 10% improvement in the minimum channel width, and up to 8% reduction in the critical path delay as obtained from ParaLarPD. We term our new algorithm as ParaLarH. Due to the increased work in the Lagrange relaxation process, however, this aspect is easily compensated by using more number of threads.

Keywords: FPGA routing, Linear programming, Sub-gradient method, Lagrange relaxation, Lagrange heuristic

1. Introduction

The Electronic Design Automation (EDA) process has been the single biggest factor behind the thriving of the semiconductor industry in the last fifty years. However, it is very time consuming with routing taking a big percentage of this time. In this paper, we focus on a large subset of this problem, i.e. the expensive Field Programmable Gate Array (FPGA) [1] routing process. FPGA routing is computationally expensive because the common standard algorithm to perform routing, i.e. Versatile Place and Route (VPR [2]) is intrinsically slow. One way to accelerate routing is to exploit parallelization capabilities of the modern High Performance Computing (HPC) machines. Since VPR is fundamentally sequential, new parallel routing algorithms need to be developed.

One of the first attempts in parallelizing this routing process was done in [3]. Here, the authors formulated the problem as a Binary Integer Linear Program (BILP), applied the Lagrange relaxation to eliminate constraints, and then solved the resulting optimization problem using the sub-gradient method and the Steiner tree algorithm. The final algorithm was termed as ParaLaR.

In one of our recent works [4], we substantially improved the constraints violation drawback of ParaLaR. We achieved this by developing a more problem specific version of the sub-gradient method and fine tuning the size of its iterative step. The final algorithm was termed as ParaLarPD. When tested on the MCNC benchmark circuits, on an average, ParaLarPD
achieved about a 20% reduction in the constraints violation (that is related to the metric of the minimum channel width) as compared to ParaLaR. There are two other important metrics used to determine the efficiency of the FPGA routing process; the total wire length and the critical path delay, with the later one being more easily measurable. In [4], we showed that on an average, ParaLarPD achieved the same total wire length but a slightly deteriorated critical path delay when compared with ParaLaR.

In this work, we sizably improve ParaLarPD further. Since the core problem of this class of parallel routing algorithms is the constraints violation, we design a family of Lagrange heuristics to improve the Lagrange relaxation process. The new algorithm is defined as ParaLarH. When tested on the MCNC benchmark circuits, on an average, our ParaLarH halves the constraints violation when compared with ParaLarPD, which is the first improvement. Second, on an average, 10% reduction is achieved in the related minimum channel width metric. The average total wire length obtained by ParaLarH is almost the same as that obtained by ParaLarPD. The third improvement obtained by ParaLarH, when compared to ParaLarPD, is in the average critical path delay (8% reduction).

The use of heuristics to reduce the constraints violation in ParaLarH does incur an overhead such that the total routing time is slightly increased (when compared to ParaLarPD). However, this drawback is easily fixable by using more threads in a parallel setting. To further demonstrate the usefulness of our approach, we also compare ParaLarH with the original algorithm that ParaLarPD improved upon (ParaLaR [3]), the common standard algorithm used for routing (VPR [2]), and two other algorithms that are sparingly prevalent (RVPack [5] and GGAPack2 [5]). ParaLarH gives results that are overall best among these as well.

The rest of this paper has four more sections. In Section 2, we present the ParaLarPD algorithm from [4]. Our Lagrange heuristic, its variants, and the resulting algorithm of ParaLarH are discussed in Section 3. In Section 4, we present the experimental results. Finally, conclusions and future work are given in Section 5.

2. Background

The routing problem in FPGA or a electronic circuit is formulated as a weighted grid graph \( G(V, E) \), where \( V \) and \( E \) are the sets of certain vertices and edges, respectively, and there is a cost associated with each edge [3, 4]. In this grid graph, we have three types of vertices; the net vertices, the Steiner vertices, and the other vertices. A net is represented as a set \( N \subseteq V \) consisting of net vertices with other types of vertices playing a supporting role.

Here, the goal is to find a route for each net such that the union of all the routes will minimize the total path cost of the graph \( G \), which is directly proportional to the total wire length of FPGA. To achieve this objective, the problem of routing of nets is formulated as an LP problem given by [3] (ParaLaR paper).

\[
\begin{align*}
\min_{x_{e,i}} & \quad \sum_{i=1}^{N_{nets}} \sum_{e \in E} w_e x_{e,i}, \\
\text{Subject to} & \quad A_i x_i = b_i, i = 1, 2, \ldots, N_{nets}, \\
& \quad x_{e,i} = 0 \text{ or } 1, \\
& \quad \sum_{i=1}^{N_{nets}} x_{e,i} \leq W, \forall e \in E
\end{align*}
\]

with meaning of each variable given in Table 1. The equality constraints guarantee that a valid route is formed for each net (these are implicitly satisfied by our solution). The inequality constraints are the channel width constraints that restrict the number of nets utilizing an edge to \( W \). These constraints also relate to our other complementary requirement, that is, the minimization of the channel width of each edge (achieved by an iterative reduction in the solution process).

| Symbols | Meaning |
|---------|---------|
| \( x_{e,i} \) | The binary decision variables that can have value either 0 (if net \( i \) does not utilize an edge \( e \)) or 1 (if net \( i \) utilizes an edge \( e \)) |
| \( N_{nets} \) | The number of nets |
| \( E \) | The set of edges with \( e \) denoting one such edge |
| \( w_e \) | The cost/ time delay associated with the edge \( e \) |
| \( W \) | A constant (input and iteratively reduced) |
| \( A_i \) | The node-arch incidence matrix (the constraints matrix of the minimum cost flow problem) |
| \( x_i \) | The vector of all \( x_{e,i} \) that represents the route of the \( i^{th} \) net |
| \( b_i \) | The demand/ supply vector, which signifies the amount of cost flow to the \( i^{th} \) net |
The inequality constraints need to be relaxed or eliminated. This is because they introduce dependencies between the routing of different nets leading to the difficulty in solving the LP in a parallel manner. The Lagrange relaxation [6] is a technique where the constraints can be eliminated by integrating them into the objective function. This introduces Lagrange multipliers $\lambda_e$ for each constraint, with relaxation carried out by adding $\lambda$ times the corresponding constraint to the objective function. That is, instead of the LP given in (1)-(2c), we have the following [3] (again ParaLaR paper):

$$\min_{x_{e,i},\lambda_e} \left( \sum_{i=1}^{N_{nets}} \sum_{e\in E} (w_e + \lambda_e)x_{e,i} - W \sum_{e\in E} \lambda_e \right), \quad (3)$$

Subject to $A_i x_i = b_i$, $i = 1, 2, \ldots, N_{nets}$,  

$$x_{e,i} = 0 \text{ or } 1 \quad \text{and} \quad (4b)$$

$$\lambda_e \geq 0. \quad (4c)$$

In the above LP, $(w_e + \lambda_e)$ is the new cost associated with the edge $e$. As earlier, this LP can be easily solved in a parallel manner.

In (3)–(4c), we have two sets of variables $x_{e,i}$ and $\lambda_e$. Since the decision variables $x_{e,i}$ can have values either 0 or 1, this LP is a Binary Integer Linear Program (BILP) that is non-differentiable [7–9]. Hence, the traditional methods such as the Simplex method [7], the interior point method [10], etc. fail here. The sub-gradient based methods [11, 12] are iterative methods for solving optimization problems without stringent differentiability requirements. In these methods, the variable (say $x$) is updated as $x^{k+1} = x^k - \alpha^k g^k$, where $\alpha^k$ is the step size, $g^k$ is a sub-gradient of the objective function, and the superscript $(k$ or $k + 1$) denotes the iteration number. Since a sub-gradient based algorithm will not give binary solutions, which we need (recall $x_{e,i}$ can be 0 or 1), we use it to compute the Lagrange multipliers $\lambda_e$ only. For solving $x_{e,i}$, we use the minimum Steiner tree algorithm.

There are many variants of the sub-gradient based methods available such as the projected method [12], the primal–dual method [13], the conditional method [14], the deflected method [14], etc. In our ParaLaR algorithm [4], which as earlier improved the ParaLaR algorithm [3], we demonstrated the superiority of using the primal–dual method with computation of the Lagrange multipliers done as below.

$$\lambda_e^{k+1} = \lambda_e^k + \alpha^k \max \left( 0, \sum_{i=1}^{N_{nets}} x_{e,i} - W \right), \quad (5)$$

where $\sum_{i=1}^{N_{nets}} x_{e,i} - W$ is a sub-gradient of the objective function at the $k^{th}$ iteration—the partial derivative of the objective function in (3). Also $\lambda^0_e$ is taken as zero for all edges.

In our ParaLaR paper [4], we also proposed a new step size updation strategy that works better than the corresponding technique proposed in the ParaLaR paper [3]. That is,

$$\alpha^k = \left( \frac{1}{k} \right) / \left\| T^k \right\|_2, \quad (6)$$

where $k$ is the iteration number, $T^k$ is the Karush–Kuhn–Tucker (KKT) operator of the objective function (3), and $\left\| T^k \right\|_2$ is the 2-norm of $T^k$.

Next, the minimum Steiner tree algorithm [15] is used to compute $x_{e,i}$. Here, the input is a set $S$ that contains the net vertices. The intermediate goal is to compute the set of Steiner vertices for $S$, which is initially empty (say $U$). The algorithm begins by forming a triple of vertices from $S$. Next, a possible candidate Steiner vertex is found such that the total path cost from the vertices in the triple to the candidate vertex is minimized. This process is repeated for all the sets of triples to find the possible Steiner vertices, out of which $U$ is formed. Finally, the union of $S$ and $U$ is obtained using the minimum spanning tree algorithm leading to the minimum Steiner tree. The edges that are used in this tree have $x_{e,i} = 1$ and all other edges have $x_{e,i} = 0$.

After one complete iteration of the primal–dual sub-gradient algorithm as well as the Steiner tree algorithm, the value of $W$ is reduced and these steps are repeated. This helps us obtain a better local minima both for the total wire length and the channel width. For easy reference the pseudo code of ParaLarPD, as published in [4], is given in Algorithm 1.

3. Proposed Approach

As mentioned earlier, in our proposed work we first perform FPGA routing using our ParaLaRPD. Since some constraints are often violated by the obtained solution, second, we develop a heuristic that converts the infeasible solution to a feasible one (i.e. tackle the is-
Algorithm 1 ParaLarPD [4]

Input: Architecture description file and benchmark file.
Output: Route edges.

1: Run VPR with the input architecture and benchmark circuit.
2: steiner_points ← ∅
3: grid_graph ← InitGridGraph()
4: \( \lambda_e = 0, \forall e \in E \)
5: for iter = 1 to max_iter do
6: Calculate the step size \( \alpha \) using (6).
7: route_edges ← ∅
8: parallel_for i = 1 to Nnets do
9: points ← \( \{ p : p \in \{ \text{source and sinks of } ith \text{ net} \} \} \)
10: if iter == 1 then
11: steiner_points[i\text{th net}] ← Min_Span_Tree(grid_graph, points)
12: end if
13: route_edges[i\text{th net}] ← Min_Span_Tree(grid_graph, steiner_points[i\text{th net}] ∪ points)
14: end parallel_for
15: while \( e \in E \) do
16: Update Lagrangian relaxation multipliers \( \lambda_e \) using the Equation (5).
17: Update the edge weight of the grid_graph on route_edge. New edge weights are \( w_e + \lambda_e \).
18: end while
19: end for

The algorithm is again iterated with the new probability based information.

Our basic Lagrangian heuristic to remove the constraints violation in ParaLarPD consists of the five steps as below. Here, we initially explain these steps using the example shown in Fig. 1, and then in the form of an algorithm. In this example, the channel widths as computed by ParaLarPD are written next to the corresponding edge in the figure. Since \( W \) is taken as forty, we have three edges where the constraints violation occur. That is AE, BF, and DH that are highlighted in bold in Fig 1.

Another example is [17] where assignment of the students to the classes (based upon their preferences) is formulated as a graph partitioning problem with the capacity constraints. This problem is further modeled as a Quadratic Program (QP), and similar to [16], the constraints are relaxed by introducing Lagrange multipliers, which are solved by the sub-gradient method. As expected, the obtained solutions are not necessarily feasible, and hence, a Lagrange heuristic is built. In this, the constraints violation are assigned probabilities based upon certain characteristics of the solution.

1. Pick an edge with the constraints violation, and find a new alternate path between the nodes of this edge using any path finding algorithm. There
may be many alternative paths possible so pick any one. If the new path contains an edge that already has the constraints violation, then drop it and move to the next alternative path.

For example here, without loss of generality, the edge picked is BF and the first alternate path chosen is BA -> AE -> EF. Since this path contains the edge AE, which violates the constraints, and hence, we drop it and pick the next possible path (BC -> CG -> GF) where no such violation occurs.

2. Next, compute the available capacity of each edge in the new path to route more nets without the constraints violation. Minimum of these capacities is termed as Threshold, and used further. Mathematically,

\[ \text{Threshold} = \min \left( W - \sum_{i=1}^{N_{nets}} x_{e,k,i} \right) \]

\[ \forall k \in \{ \text{edges in the new path} \}. \]

For our example, the value of Threshold is 8.

3. Calculate the amount of violation

\[ d = \sum_{i=1}^{N_{nets}} x_{e,i} - W \]

for the edge under consideration e. Further, calculate the number of nets where the constraints violating edge needs to be replaced by the selected new path. This is computed as

\[ q = \min(\text{Threshold}, d) \]  \hspace{1cm} (7)

so that no edge in the added new path has the constraints violation.

For the edge under consideration (BF), \( d = 43 - 40 = 3 \), and hence, \( q = \min(8, 3) = 3 \).

4. Finally, replace this edge under consideration with the selected path in \( q \) number of nets.

In this example, this corresponds to replacing BF with BC -> CG -> CF in 3 nets.

5. If in (7) above, \( \text{Threshold} < d \), then we would have not completely eliminated the constraints violation in the edge under-consideration. In this case, the search for the alternate path needs to resumed from the start until the violation is completely eliminated or no such path exists.

We repeat the above steps for all the edges that are violating the constraints. This violation is directly related to the minimum channel width (discussed earlier), i.e. we improve this requirement as well. Algorithm 2 describes our heuristic design in an algorithmic form. The points above map to the respective line numbers in the algorithm, which is termed as ParaLarH. For enhanced clarity, we describe ParaLarH via a data flow diagram as well (in Fig. 2).

**Algorithm 2 Heuristic Design**

**Input:** Set of nets and edges that are being used; and the decision variables determined by ParaLarPD algorithm.

**Output:** Updated set of nets and edges that are being used.

```
for (each edge \( e \in E \)) do
  while \( (d = \sum_{i=1}^{N_{nets}} x_{e,i} - W \geq 0) \) do
    1. Find a path using any path finding algorithm \( p : e_1 e_2 \cdots e_{r-1} e_r \) between the end points of the edge \( e \) such that
      \[ e_1.start = e.start, \]
      \[ e_j.end = e_{j+1}.start \]
      \[ \forall j \in \{1, 2, \ldots, r - 1\}, \]
      \[ e_r.end = e.end, \]
      \[ \sum_{i=1}^{N_{nets}} x_{e,j,i} \leq W \forall j \in \{1, 2, \ldots, r\}, \]
    2. Compute
      \[ \text{Threshold} = \min \left( W - \sum_{i=1}^{N_{nets}} x_{e,k,i} \right) \]
      \[ \forall k \in \{1, 2, \ldots, r\}. \]
    3. Calculate \( q = \min(\text{Threshold}, d) \).
    4. If \( \text{Net}^t = \{N_{nets}^1, N_{nets}^2, \ldots, N_{nets}^t\} \) denotes the \( t \) nets where edge \( e \) is used. Replace \( e \) with path \( e_1 e_2 \cdots e_r \) in \( q \) such nets. Usually \( t > q \).
      // The Point 5 as discussed in text maps to the while statement above.
  end while
end for
```

3.1. **Other Variations of our Heuristic**

Next, we discuss some variants of ParaLarH. As mentioned earlier, these variations are designed to help reduce the constraints violation further, however, they
do negligibly increase the computational cost of the overall algorithm.

(A) The first variant is based upon the fact that there may exist multiple paths between any two end points, and in Step 1 above we should pick the one that gives the best results. Hence, instead of picking just one path randomly, we pick $\beta$ number of paths. Further, we perform Steps 1, 2 and 3 for all these $\beta$ paths.

(B) In the second variant, in Step 4 above we begin by sorting the $t$ nets where the edge under consideration $e$ is used. This sorting is done in the increasing order of the number of new edges that get added to each net while eliminating $e$. Then, we replace $e$ with the new path in the first $q$ nets ensuring minimization of the overall constraints violation.

The results obtained by our basic heuristic and the above variants are approximately the same. Therefore, in the next section, without the loss of generality, we present the results for the second variant. As mentioned in the Introduction, the extra computation in implementing the heuristic does increase the overall runtime of our algorithm. However, this is easily offsetted by using more threads in a parallel setting (discussed further in the next section).

4. Experimental Results

We perform multiple experiments to demonstrate the usefulness of our ParaLarH algorithm. In Section 4.1, we compare ParaLarH with ParaLarPD [4], the algorithm we improve upon, in multiple ways. In Section 4.2, we compare ParaLarH with another algorithm of the same family (ParaLaR [3]), the current standard (VPR [2]), and two other sparingly used algorithms (RVPack [5] and GGAPack2 [5]).

We perform experiments on the MCNC benchmark circuits [22] that range from small-sized to large-sized logic blocks. Experiments are done on a single Intel Xeon (R) CPU E5-1620 V3 machine running at 3.50 GHz with 64 GB RAM. The operating system is Ubuntu 14.04 LTS, and the kernel version is 3.13.0-100. Our codes are written in C++11 and compiled using GCC version 4.8.4 with O3 optimization flag. After compilation, the resulting codes are run using different number of threads from the Intel Threading Building Blocks (TBB) libraries.

4.1. Comparison with ParaLarPD

Here, first, we discuss the setup of our experiments. Second, we compare ParaLarH with ParaLarPD using the main metric of the constraints violation as well as the related metric of the minimum channel width. Here, we also compare the two algorithms using the metrics of the total wire length and the critical path delay. Third, and finally, we compare ParaLarH with ParaLarPD using the speedups obtained because of multi-threading.
4.1.1. Setup

We use the most common architecture parameters [2, 4, 5, 23] as given in Table 2. Here, the value of \( N \) specifies that the CLBs in the architecture contain ten Fracturable Logic Elements (FLEs). The value of \( K \) specifies that each FLE has six inputs. The values of \( F_{cin} \) and \( F_{cout} \) specify that every input and output pin is driven by 15% and 10% of the tracks in a channel, respectively. We also perform experiments with \( F_{cin} = 1 \) and \( F_{cout} = 1 \). In this paper, we do not report these results because in most of the modern FPGA designs, input and output pins are not driven by 100% of the tracks in a channel. However, our ParaLarH gives better results than ParaLarPD for this as well. The value of \( F_s \) specifies the number of wire segments that can be connected to each wire where the horizontal and the vertical channels intersect. This value can only be a multiple of 3. In this paper, we report the results for \( F_s = 3 \). We also perform experiments with \( F_s = 6 \), the results of which are not reported here. However, for this case too, ParaLarH gives better results than ParaLarPD. The value of Length specifies the number of logic blocks spanned by each segment. Here, we take this value as 4, though our proposed FPGA routing can be used for architectures with other values of Lengths as well, e.g. Length = 1 or a mix of Length = 1 and Length = 4.

| FPGA design architecture parameters used in our experiments. |
|---|
| **N** | **K** | **\(F_{cin} \)** | **\(F_{cout} \)** | **\(F_s \)** | **Length** |
| 10 | 6 | 0.15 | 0.10 | 3 | 4 |

Initially, the circuits are packed and placed using VPR. After that, routing is performed by the respective algorithm. There is no general rule of choosing the initial value of the channel width for experimental purposes. However, a value of 20% to 40% more than the minimum channel width obtained from VPR is commonly used [3,4,23]. Our algorithms are initialized with the initial channel width (\( W \)) as \( 1.2W_{\text{min}} \), where \( W_{\text{min}} \) is the minimum channel width obtained from VPR. We also perform experiments with an initial \( W \) as \( 1.4W_{\text{min}} \), which does not change the results. We use an upper limit of 50 for the number of iterations and perform 100 runs of all the algorithms. The best results out of these are reported.

4.1.2. Basic Comparison

The results here are independent of the number of threads used, and hence, we give results for a single thread only. We use up to five significant digits to report our data. Specifically, we round the constraints violation, the minimum channel width and the critical path delay to two decimal places, and the total wire length to the nearest integer. Here, we also report the geometric mean (Geo. Mean) of all the values obtained for the different benchmark circuits, which indicates the central tendency of a set of numbers and is commonly used [3,4].

In Table 3, we compare the constraints violation and the minimum channel width of ParaLarH and ParaLarPD. As evident from this table, for all the benchmarks, ParaLarH substantially improves both these metrics. The average constraints violation reduces to half, and the average reduction in the minimum channel width is 10%, which as per the FPGA routing domain experts is considered very good.

| Benchmark | Absolute Constraint Violation | Minimum Channel Width |
|---|---|---|
| | ParaLarH | ParaLarPD | ParaLarH | ParaLarPD |
| Alu4 | 4.67 | 5.54 | 34.67 | 35.54 |
| Apex2 | 5.12 | 10.08 | 45.12 | 50.08 |
| Apex4 | 1.87 | 5.58 | 41.87 | 45.58 |
| Bigkey | 5.18 | 9.04 | 15.18 | 19.04 |
| Clma | 5.32 | 16.44 | 70.32 | 81.44 |
| Des | 5.40 | 11.17 | 25.40 | 31.17 |
| Diffeq | 2.67 | 7.52 | 32.67 | 37.52 |
| Dsip | 4.86 | 5.63 | 24.86 | 25.63 |
| Elliptic | 5.20 | 12.42 | 50.20 | 57.42 |
| Ex1010 | 4.78 | 8.83 | 44.78 | 48.83 |
| Ex5p | 4.23 | 8.31 | 59.23 | 63.31 |
| Frisc | 6.45 | 13.71 | 61.45 | 68.71 |
| Misex | 4.56 | 7.27 | 39.56 | 42.27 |
| Pdc | 4.34 | 8.67 | 69.34 | 73.67 |
| S298 | 4.87 | 9.00 | 34.87 | 39.00 |
| S38417 | 5.34 | 10.48 | 45.34 | 50.48 |
| Seq | 4.68 | 8.85 | 44.68 | 48.85 |
| Spla | 4.92 | 9.41 | 54.92 | 59.41 |
| Tseng | 4.87 | 9.65 | 34.87 | 39.65 |
| Geo. Mean | 4.56 | 8.98 | 40.99 | 45.55 |
While this work focuses on minimizing the constraints violation, we measure our algorithm's impact on other metrics as well, i.e., the total wire length and the critical path delay. In Table 4, we compare these metrics for ParaLarH and ParaLarPD. We observe almost a negligible increment in the total wire length obtained by ParaLarH as compared to ParaLarPD (on an average 0.92%). If we look at the easily measurable critical path delay, we observe that on an average critical path delay of ParaLarH is 7.60% less as compared to ParaLarPD, which again is considered a very good improvement.

| Benchmark Circuits | Total Wire Length | Critical Path Delay |
|--------------------|-------------------|---------------------|
| ParaLarH           | ParaLarPD         | ParaLaR             | VPR | RVPack | GGAPack2 |
| Au4                | 5030              | 5030                | 6.99 | 7.30   |
| Apex2              | 7978              | 7935                | 7.30 | 7.41   |
| Apex4              | 5807              | 5630                | 6.51 | 7.08   |
| Bigkey             | 3927              | 3896                | 3.32 | 4.01   |
| Clma               | 49474             | 49278               | 15.42| 15.46  |
| Des                | 7043              | 6952                | 5.47 | 5.55   |
| Diffq              | 4693              | 4349                | 5.84 | 5.65   |
| Dsp                | 4771              | 4778                | 3.19 | 3.62   |
| Elliptic           | 15253             | 15125               | 7.53 | 10.83  |
| Ex5p               | 4916              | 4889                | 6.32 | 6.94   |
| Ex1010             | 23603             | 23596               | 12.00| 14.57  |
| Frisc              | 19713             | 19484               | 12.68| 13.13  |
| Mixes3             | 5195              | 5194                | 6.19 | 6.49   |
| Pdc                | 30435             | 30423               | 12.39| 12.63  |
| S298               | 5256              | 5250                | 11.67| 12.71  |
| S38417             | 21962             | 21907               | 9.11 | 10.44  |
| Seq                | 7685              | 7654                | 6.00 | 6.14   |
| Spla               | 20139             | 20117               | 10.23| 10.43  |
| Tseng              | 2491              | 2484                | 5.78 | 5.78   |
| **Geo Mean**       | **9124.20**       | **9041.01**         | **7.42** | **8.03** |

**Table 4**

Comparison of the total wire length and the critical path delay between our proposed ParaLarH and ParaLarPD [4].

### 4.1.3. Comparison of Speedups

The speedups obtained in executing the benchmarks via ParaLarH in a parallel setting are given as a bar graph in Fig. 3. In this figure, on the x-axis we have the benchmark circuits arranged in the increasing order of their execution time when running them with one thread. This time is directly proportional to the benchmark size, and arranging them this way ensures that the benchmarks are sorted in the order of their increasing size (used below). On the y-axis, we have the speedups in execution of these benchmark circuits when using 2 threads, 4 threads, and 8 threads in ParaLarH.

We make two observations from this bar graph. First, the benchmarks of larger sizes (towards the right of the graph) have more speedups as compared to those of smaller sizes (towards the left of the graph). Second, on an average, 2, 4, and 8 threads give speedups of 1.63, 2.74, and 3.32, respectively.

In ParaLarPD [4], the average speedups when using 2, 4, and 8 threads comes to be 1.80, 3.11, and 5.11, respectively. If we compare the speedups obtained from ParaLarH with ParaLarPD, we observe that there is a slight deterioration in the case of ParaLarH.

This drop in speedups is acceptable because of two reasons. First, as compared to ParaLarPD, ParaLarH substantially improves the constraints violation (halving it), the minimum channel width (reducing it by 10%), and the critical path delay (reducing it by 8%) while keeping the total wire length almost the same. Second, this slight loss in speedups is easily compensated by using more number of threads.

### 4.2. Comparison with the Other Algorithms

As mentioned earlier, here we compare ParaLarH with the other algorithms for FPGA routing. That is, ParaLaR, VPR, RVPack and GGAPack2. This comparison is done using all the above discussed metrics; the minimum channel width\(^1\), the total wire length, the critical path delay, and the speedups.

For ParaLaR and VPR, we use the setup as discussed in Section 4.1.1. RVPack and GGAPack2 design is fundamentally different from the other algorithms (i.e. ParaLarH, ParaLarPD, ParaLaR, and VPR), and hence, the above mentioned setup cannot be used. Further, replicating the setup of RVPack and GGAPack2 is challenging as well due to the involved randomness. Hence, we use VPR as the base algorithm against which we compare ParaLarH, ParaLaR, RV-Pack and GGAPack2 with experiments done here for the first two algorithms and data picked from the original paper ([5]) for the last two. Since in VPR, RV-Pack, and GGAPack2 there is no concept of parallelization, all comparisons are done using a single thread.

This comparison is given in Table 5, with the best improvements highlighted in bold. Here, a negative

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\(^1\)This captures the constraints violation implicitly.
sign indicates deterioration. From this table, we can see that for the percentage gain in the minimum channel width as well as the critical path delay, ParaLarH triumphs the other three algorithms. Its percentage improvement in the total wire length is also almost the best (very close to that of ParaLaR). Regarding speedups, the percentage gain in ParaLarH is the second best (and slightly below that of ParaLaR), which is acceptable since it can be easily compensated as discussed in Section 4.1.3.

Table 5

Performance comparison of ParaLarH with ParaLaR [3], VPR [2], RVPack [5] and GGAPack2 [5].

| Algorithms        | % Improvement over VPR |
|-------------------|------------------------|
|                   | Minimum Channel Width  | Total Wire Length | Critical Path Delay | Speedup |
| ParaLarH          | 34.68                  | 48.39             | 9.95                | 2.28    |
| ParaLaR           | 9.08                   | 48.83             | 4.00                | 2.70    |
| RVPack            | 12.37                  | 7.19              | -31.64              | 1.28    |
| GGAPack2          | 2.23                   | -5.78             | -35.94              | <100    |

5. Conclusions and Future Work

In this work, we improve upon ParaLarPD, the best available algorithm for the parallel routing of Field Programmable Gate Array (FPGA) design flow. ParaLarPD formulates the design process as a Linear Program (LP) and solves it using the Lagrange relaxation, the sub-gradient method, and the Steiner algorithm. Here, we improve this algorithm’s Lagrange relaxation process by introducing a set of Lagrange heuristics resulting in substantial reduction of the constraints violation by the solution vector. We term our algorithm as ParaLarH.

With experiments on the MCNC benchmark circuits we show that as compared to ParaLarPD, on an average, ParaLarH halves the constraints violation, reduces the minimum channel width metric by 10% and the easily measurable metric of critical path delay by 8%. The extra work in implementing the heuristic does slightly deteriorate the parallelization speedups of ParaLarH as compared to that of ParaLarPD, however, this is easily fixable by using more number of threads. In future, we plan to work towards designing algorithms that would completely remove the constraints violation. We also plan to apply our techniques to the field of Internet of Things (IoT) where similar design challenges arise.

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