Overview of the IBM Neural Computer Architecture

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Abstract—The IBM Neural Computer (INC) is a highly flexible, re-configurable parallel processing system that is intended as a research and development platform for emerging machine intelligence algorithms and computational neuroscience. It consists of hundreds of programmable nodes, primarily based on Xilinx’s Field Programmable Gate Array (FPGA) technology. The nodes are interconnected in a scalable 3d mesh topology. We overview INC, emphasizing unique features such as flexibility and scalability both in the types of computations performed and in the available modes of communication, enabling new machine intelligence approaches and learning strategies not well suited to the matrix manipulation/SIMD libraries that GPUs are optimized for. This paper describes the architecture of the machine and applications are to be described in detail elsewhere.

Index Terms—FPGA, parallel processors, machine intelligence, re-configurable hardware.

1 INTRODUCTION

The revolution in deep learning over the last decade has been mainly driven by the confluence of two equally important factors – the generation of large amounts of data, and the availability of GPUs to train large neural networks. Those contributed to accelerated research in the algorithmic domain by significantly decreasing experiment turnaround time. In recent years, as the computational demands for deep learning have increased, especially in consumer facing domains such as image and speech recognition, there is a trend towards more hardware specialization to improve performance and energy-efficiency. For instance, recent hardware approaches feature techniques such as reduced precision, aggressive compression schemes and customized systolic data paths aimed at accelerating today’s DNNs.

While these efforts are extremely important both from research and commercialization perspectives, the currently available hardware landscape is also somewhat restrictive. This is because GPUs (and their variants) may not lend themselves well to use cases where mini-batching/data parallelism is non-trivial because multiply-accumulate operations are not dominant or when low latency is critical. Therefore, as machine intelligence algorithms continue to evolve, it is unfortunate that promising approaches may be sidelined simply because they do not map well to a GPU, just as backpropagation trailed more conventional machine learning approaches for decades due to the lack of GPUs. One of the prime examples of an algorithm which is not well matched to SIMD architecture is Monte Carlo Tree Search used in the Google Deepmind’s AlphaGo system [8].

This indicates the need for new computer architectures for machine intelligence. However, there is an obvious challenge – namely, how does one build hardware for algorithms and use cases that may not yet exist? The approach we have taken is to build a hardware system with tremendous flexibility, which will be explored in depth in the rest of the paper. This flexibility extends to the types of algorithms being executed, the portions that need to be off-loaded and accelerated, the model of communication, and the types of parallelism deployed.

The system, named IBM Neural Computer (INC), is fundamentally a large, highly scalable parallel processing system with compute nodes interconnected in a 3D mesh topology. The total number of compute nodes within the existing single-cage system is 432. Each compute node contains a Xilinx Zynq System-on-Chip (an ARM A9 CPU + FPGA logic on the same die) along with 1GB of dedicated RAM [9], [10], [11]. The availability of FPGA resources on every node allows application-specific processor offload, a feature that is not available on any parallel machine of this scale that we are aware of.

The communication network that realizes the 3D mesh topology is implemented using single-span and multi-span SERDES (Serializer-Deserializer) links connected to the FPGA fabric of the Zynq. It is therefore possible to build tailored hardware network controllers based on the communication mode(s) most suited to the application. The ability to optimize the system performance across application code, middle-ware, system software, and hardware is a key feature of INC.

One may envision that this 3D topology of distributed memory and compute, with the ability to have nodes exchange signals/messages with one another is somewhat reminiscent of works targeting the human brain (most prominently, the SpiNNaker project [12], [13]). However, an important distinction is that our goal is more general than computational neuroscience, and extends to machine intelligence in general.

The rest of the paper is organized as follows. Section
Fig. 1. 3D Mesh Topology of a single INC card, with some node numbers shown. Each node contains its own dedicated Zynq System-on-Chip with an ARM Cortex-A9 and FPGA logic. Node 100 (blue shaded cube) is the gateway node to the external Ethernet. Nodes 000 (green shaded cube) and 200 have PCIe Interfaces to communicate with a host computer.

Fig. 2. Hierarchical organization of the INC system (a) Conceptual design of INC 9000 with 48 cards and 1296 nodes (not yet built), (b) INC 3000 with 16 cards and 432 nodes (operational), (c) Single card with 27 nodes, (d) One node.

2 begins with an overview of the INC system. Section 3 discusses inter-node communication mechanisms in INC. Section 4 contains details on diagnostic and debug capabilities of the INC system, which are crucial in a development environment. Section 5 will conclude the paper.

2 INC OVERVIEW

The INC system is designed primarily to be a development platform for emerging machine intelligence algorithms. It is a parallel processing system with a large number of compute nodes organized in a high bandwidth 3D mesh network. The platform is designed to be highly flexible. Within each node is a Xilinx Zynq system-on-chip, which integrates a dual-core Cortex A9 ARM processor and an FPGA on the same die, allowing the system to be reconfigured on a per node basis. Each node also includes 1GB of dedicated DRAM that can be used as program and data space, and is accessible both from the processor and the FPGA. In an eventual at-scale high-performance learning task, we envision that most of the performance critical steps will be offloaded and optimized on the FPGA, with the ARM only providing auxiliary support – including initialization, diagnostics, output transfer, etc.

While INC is a distributed system in that it is composed of distinct processor+memory nodes interconnected by communication links, it has a unique combination of features not available elsewhere. It is not a multi-FPGA ‘sea of gates’ system [14], [15] whose structure would need to be defined by the logic resident on the FPGA. It has a very well defined structure of compute nodes with a well defined communications network. Therefore it does not carry the performance compromise associated with the need to support a fully-generic interconnect.

It is also different from other distributed systems such as BlueGene [16]. In addition to the available FPGA offload capability at every node, the communication interfaces are
not pre-defined to support a limited set of known use cases. Instead, access to the physical communication links is through the FPGA, and multiple distinct ‘logical’ channels of communication can be established, all utilizing the same underlying SERDES links. In this way, the network interfaces can be designed (and even progressively optimized) to best suit the applications executing on INC.

2.1 INC card

The basic building block of the system is an INC card. Each card contains 27 nodes arranged in a 3×3×3 cube. Figure 1 shows the 3x3x3 topology of an individual card, along with (XYZ) co-ordinates overlaid to indicate the organization of the 3D mesh. The 27 nodes are placed on the card in a way to minimize the connection lengths between logically adjacent nodes. All 27 nodes on a single card are identical except for some important differences. Node (100) includes an Ethernet port, and can act as a gateway connecting an internal Ethernet network implemented on the FPGAs to a conventional external network. Node (000) is a controller node, and includes a 4 lane PCIe 2.0 connection that can be connected to a host PC. It also has a serial connection that can serve as a console during boot time, or be forwarded to the other nodes on the card. Node (200) is also capable of supporting a PCIe interface, should an application need additional bandwidth.

2.2 Backplane, Cages and Racks

In an INC system, individual cards plug into a backplane. Each backplane can support up to 16 cards, and the backplane wiring arranges the 432 nodes of the 16 cards into a 12×12×12 mesh. The backplane and cards are enclosed in an INC card cage (INC 3000 system (Fig. 2b)). Connectors on the back side of the backplane allow up to four cages to be connected vertically to build a system of up to 12 cages. The card design supports building an INC system with anywhere from one to 512 cards (13,824 nodes). However, to grow beyond the size of the INC 9000 system, a new backplane design is required.

2.3 Physical Links

Each node on a card is connected to its nearest orthogonal neighbors by a single span link composed of two unidirectional serial connections. Each node has six single span links. The nodes on the faces of the cube (i.e. all nodes other than the central (111) node) have single span links that leave the card, and may have nearest neighbors on other cards in the system. In addition to single span links, 6 bi-directional multi-span links allow for more efficient communication in a larger system. Multi-span links connect nodes that are three nodes apart in any one orthogonal direction, and will always begin and terminate on different cards. With a total of 432 links leaving or entering the card, and 1 Gigabyte (GB) per second per link, this amounts to a potential maximum bandwidth of 432 GB per second leaving and entering one card. The bisection bandwidths for the INC 9000 and INC 3000 systems are 864 GB per second and 288 GB per second respectively.

The communications links are pairs of high speed, serial, unidirectional SERDES connections. Each connection only has two wires: the differential data lines. There are no additional lines for handshake signals. The links are controlled by a credit scheme to ensure that overrun errors do not occur and no data is lost. A receiving link sends (via its paired transmit link) a count of how many bytes of data it is willing to receive. A transmitting link will decrement its count as it sends data and never send more data than it holds credits for from the receiver. The receiving side will add to the credit balance as it frees up buffer space. This credit system is implemented entirely in the hardware fabric and does not involve the ARM processor or software.

2.4 Packet Routing

The communication network currently supports directed and broadcast packet routing schemes. Features such as multi-cast or network defect avoidance are being considered at the time of writing, and can be included based on application or hardware needs.

In a directed routing mode, a packet originating from the processor complex or the FPGA portion of a compute node is routed to a single destination. Both single-span and multi-span links may be used for the routing, and the packet will be delivered with a minimum number of hops. However, a deterministic routing path is not guaranteed, as each node involved may make a routing decision based on which links happen to be idle at that instant. This implies that in-order delivery of packets is not guaranteed. The packet routing mechanism is implemented entirely on the FPGA fabric, and the ARM processors may only be involved at the source and destination nodes, if at all.

A broadcast packet radiates out from the source node in all directions and is delivered to every node in the system. Broadcast packets only use the single-span links in the system for simplicity of routing. Depending on which link received a broadcast packet, the receiving node may choose to a) forward to all other links, b) forward to a subset of links, or c) stop forwarding. By choosing the rules for these three scenarios carefully, it is possible to ensure that all nodes in the system receive exactly one copy of the broadcast packet.

3 CONNECTIVITY AND COMMUNICATION

Multiple virtual channels can be designed to sit atop the underlying packet router logic described in the previous section to give the processor and FPGA logic different virtual or logical interfaces to the communication network. In this section we will review three approaches currently implemented on INC – Internal Ethernet, Postmaster Direct Memory Access (DMA) and Bridge FIFO.

3.1 Internal Ethernet

One of the virtual interfaces is designed to appear similar to an Ethernet interface. While the underlying hardware is

1. This does not preclude applications that need in-order delivery, as reordering can be achieved in either FPGA hardware or in software, or a different packet routing scheme can be devised as necessary.

2. Note that this is an interface for node to node communication, and is different from the ‘real’ physical Ethernet interface at node (100) which is intended for communicating with the external world.
Fig. 3. Operation of the virtual internal Ethernet interface: Network packets generated at a source node are initially in its DRAM. At the request of the Ethernet Device driver, a DMA transfer is initiated and the packet is transferred to the router logic facing the SERDES links. The packet will traverse through zero or more intermediate nodes without processor interaction before reaching the destination, where the Ethernet device implemented on the FPGA fabric will raise a hardware interrupt, notifying the driver and thereby the kernel of the new packet to be processed.

quite different from an Ethernet network, this design point is chosen to take advantage of the large amount of standard application software readily available for IP networks such as ssh. A Linux OS and associated device driver running on an ARM processor can then use these applications to communicate with other nodes on the internal network operating as if it were communicating with a real Ethernet device. Similarly, applications that depend on standard parallel software libraries (e.g., Message Passing Interface (MPI) [17] and its variants) can be easily supported. Using stable, well-established networking applications was also extremely useful during initial debugging of the network hardware and the system software.

The operating mechanism for transmitting packets is conceptualized in Fig. 3. During the Transmit Operation, the application passes information to the kernel networking stack, which adds various headers and sends it on to a virtual internal Ethernet interface (ethX). This interface is owned by the device driver, which manages a set of buffer descriptors that contain information about the size and memory locations of various packets in the DRAM. The device driver then informs the hardware about the availability of a packet to be transmitted, by setting a status bit. The actual transfer from the DRAM into the FPGA fabric is a DMA operation, using an AXI-HP bus on the Zynq chip. Packet receive is conceptually a reverse operation, with the distinction that the device driver has two mechanisms to know of the arrival of a packet on the interface – one is a hardware interrupt, and the other is a polling mechanism that is far more efficient under high traffic conditions. Note that while this description assumes applications running in software as the producers and consumers of the packets, the internal Ethernet can also be accessed from other hardware blocks on the FPGA fabric itself, if at all necessary.

The availability of this virtual internal Ethernet also makes it straightforward for any node in the system to communicate with the external world using TCP/IP. This is done by using the physical Ethernet port on node (100) and configuring this node as an Ethernet gateway implementing Network Address Translation (NAT) and port forwarding. One immediate and obvious use of this feature is the implementation of an NFS (network file system) service to save application data from each of the nodes (whose file systems are implemented on the DRAM and are therefore volatile) to a non-volatile external storage medium.

3.2 Postmaster DMA

The postmaster DMA logic provides a method to move small amounts of data between nodes in the system. The function is intended to be used directly by machine intelligence application code on the software or by application hardware modules on the FPGA. It provides a communications channel with much lower overhead than going through the TCP/IP stack.

Postmaster DMA is a tunneled queue model (Fig. 4), where the processor (or hardware module) sees a queue that can be written at a known, fixed, address. Data written to that queue is transferred to a remote node where it is picked up by a DMA engine and moved to a pre-allocated buffer in system memory. Multiple initiators may send data to the same target. At the target, the received data is stored in a linear stream in the order in which it is received. The Postmaster hardware guarantees that a packet of data from a single initiator is always stored in contiguous locations. To reiterate, it is not necessary that the postmaster DMA be used only for processor-to-processor communication; other FPGA hardware implemented on the source/destination nodes could use it too if necessary (although in some cases this may make the ‘DMA’ superfluous).

Packets from multiple initiators will be interleaved within the single data queue. This model is particularly well-suited to Machine Intelligence applications in which regions or learners are distributed across multiple nodes, and each node generates multiple small outputs during each
time step which become the inputs in the next time step. The function of Postmaster is to allow the node to send those outputs to their intended targets as they are generated rather than collect them and send them out as a larger transmission at the end of the time step. In addition to eliminating the burden of aggregating the data, this approach also allows much more overlap of computation and communication.

3.3 Bridge FIFO

The bridge FIFO is intended to facilitate direct hardware to hardware communication between two hardware modules located in separate FPGAs by exposing a regular FIFO interface. The bridge FIFO takes care of assembling the data into network packets and communicating with the packet router logic. Figure 5 presents an implementation of the bridge FIFO.

The interface is composed of two modules implemented in pairs: the Bridge FIFO transmit and the Bridge FIFO receive. The first one corresponds to the write port of the FIFO while the second corresponds to the read port. They are always implemented in pairs and must be located on the source node for the transmit unit and on the destination node for the receive unit. Together, they form a communication channel.

On the source Node, the Bridge FIFO transmit converts its input (words of data) into network packets. These Bridge FIFO packets are multiplexed with other protocol packets within the Packet Mux unit which transmits all the networks packets to the Packet Router unit. The Packet Mux unit enables coexistence of multiple communication protocols. On the destination Node, the Packet Router transmits the received network packets to the Packet Demux unit, which separates the various protocol packets and directs them to their corresponding receiver. The Bridge FIFO receive unit receives the packets and converts them back into words of data.

If multiple independent communication channels are required, then multiple pairs of Bridge FIFO transmit and receive can be instantiated. The Bridge FIFO transmits will be multiplexed within the Bridge FIFO mux and the bridge FIFO receives will be demultiplexed within the Bridge FIFO demux. The Bridge FIFO Mux (respectively Demux) supports up to 32 Bridge FIFO transmit (respectively receive). If more channels are required, then another Bridge FIFO Mux (respectively Demux) must be instantiated.

The Bridge FIFO supports different configurable bit-widths ranging from 7 to 64. If a wider FIFO is needed, then multiple bridge FIFOs must be used in parallel to achieve the required width.
TABLE 1
Communication latency of the bridge FIFO between two nodes.

| Number of hops (in Node) | 0   | 1   | 3   | 6   |
|--------------------------|-----|-----|-----|-----|
| Latency (in µs)          | 0.25| 1.1 | 2.5 | 4.7 |

Table I presents the measured latency when using the bridge FIFO. Number of hops being zero correspond to the case where sender and receiver are on the same node, where the latency corresponds to the delay incurred by the Bridge FIFO logic alone. The cases with 1, 3 and 6 hops are the best, average and worst case respectively on a single card system (27 nodes arranged in a cubic 3D mesh with 3 nodes on each edge).

4 Diagnostic Capabilities

INC features a wide array of diagnostic capabilities built into the hardware platform. This is especially important in a development platform, as the reconfigurable hardware, the system software and the application software are all concurrently evolving. While some of these have been mentioned in passing in earlier sections, we present a more detailed discussion here.

4.1 JTAG

Each INC card has a single JTAG chain that is daisy chained through all 27 Zynq FPGAs. The JTAG chain can be used to access both the individual processors and the FPGAs, as these appear as different devices on chain. Therefore, it can be used for a broad variety of tasks including configuring the FPGAs, loading code, debugging FPGA logic with Xilinx Chipscope, and debugging the ARM code through the ARM debug access port (DAP). This mode of debug is especially useful in ironing out issues during initial system bring up, when other modes may not yet be readily available.

4.2 Ring Bus and NetTunnel

The Ring Bus is a sideband communications channel that links all 27 nodes on the escape card. The bus is implemented as a ring composed of 27 unidirectional point-to-point links. The topology allows data transfer between any two nodes by forwarding request and write data or read response through the intervening nodes. The topology also supports broadcast write operations by forwarding a given write command to all nodes on the ring. The routing of ring traffic is controlled by the hardware with no processor intervention.

The NetTunnel logic is functionally similar to the Ring Bus, but uses the network fabric as the transport as opposed to a dedicated sideband channel. This allows the NetTunnel logic to span the entire system, whereas the Ring Bus is confined to a single card. Note that NetTunnel does not automatically make the Ring Bus superfluous, as the network and router logic can change depending on the demands of the applications. In this scenario, having a dedicated and reliable sideband for communication is particularly useful.

As both of these mechanisms have access to the entire 4GB address space on each node they can reach, they can be used in a wide variety of scenarios. For instance, debugging reconfigurable logic often involves reading a set of hardware registers to determine the current status, active interrupts, errors and so forth. This is especially useful when communication between nodes is involved, as the issue could be at the source, the destination or indeed along links on intermediate nodes. Similarly, checkpoints, statistics or relevant program data may be written into, and subsequently retrieved from, hardware registers. This can be very useful in debugging application or device driver code if stdout is not available or is too late, such as in a hang scenario.

4.3 PCIe Sandbox

PCIe Sandbox is an interactive utility that runs on a host x86 machine and provides access to the INC system through the PCIe interface on node (000). Using a set of simple commands, a user can read and write to addresses on all nodes in the INC system. PCIe Sandbox also supports a ‘read all’ command that uses the Ring Bus to retrieve data from the same address location on all nodes of the card. Underneath, PCIe Sandbox ‘translates’ these commands into read or write requests on the Ring Bus and NetTunnel mechanisms described above. This abstraction layer proves very useful for rapid debugging.

By reading and writing to registers on a node, special tasks can be accomplished including attaching the UART serial console to a particular node, reading bitstream IDs for all the nodes, temperature of the card, EEPROM information (which may contain useful information such as USB-UART serial number, MAC ID of the gateway Ethernet interface on (100) etc), and the system configuration (i.e. how many cards are on the system).

Finally, PCIe Sandbox is capable of loading chunks of data into the DRAM of the compute nodes. This is the preferred method for system boot up, as one can broadcast the kernel images and associated device-trees to all the nodes in the system and then write to a boot command register that initiates boot. The same method is used to configure the FPGAs in the system with new bitstreams or to program FLASH chips in the individual nodes.

Programming the FPGAs and FLASH using the PCIe host connection and internal network is much faster than programming over JTAG. For example, programming 27 FPGAs on a single card over JTAG takes approximately 15 minutes. On the other hand, programming 27 FPGAs on a single card over PCIe takes a couple of seconds, including the data transfer. Similarly, programming 432 FPGAs on 16 cards is nearly identical to programming one card, thanks to the network broadcast capability. It is important to note that JTAG can only work on a single card. The programming speed advantage is even more pronounced for programming the FLASH chips. On one occasion, it took more than 5 hours to program 27 FLASH chips on a single card over JTAG. In contrast, it takes about 2 minutes to program 1, 16, or 432 (or anything in between) FLASH chips over the PCIe interface.

4.4 ARM Processor

The ARM processor provides another dimension of per-node debug and diagnostic capability. Getting Linux run-
ning on the ARM immediately makes available a rich and varied set of diagnostic utilities. Network utilities such as **iperf** [18], **tcpdump** [19] and even **ping** [20] were used in debugging the internal Ethernet interface and the associated device driver. Counters on the ARM Performance Monitoring Unit can be readily accessed by device driver. Counters on the ARM Performance Monitoring Unit can be readily accessed by **perf** [21] or other utilities to understand bottlenecks in application code and identify candidates for FPGA offload. Standard debuggers such as **gdb** [22] or **valgrind** [23] could also be cross-compiled and ported, though this is untested at this time.

5 Conclusions

We presented an overview of the INC machine intelligence platform, and publications on applications will follow shortly. Here we focused on highlighting the main features of the hardware including flexibility, configurability, high bandwidth, highly interconnected node-to-node communication modes, and diagnostic capabilities. The uniqueness of our system is that each of the 432 nodes allows application-specific offload and this feature is not available on any other parallel machine of this scale.

The practical challenges of using the INC systems lie at the interface of hardware and software. Programming directly at the FPGA level is often a daunting task for machine learning practitioners who are used to high-level languages and frameworks. On the other hand, hardware designers are accustomed to working with well-defined specifications and functionality, as circuit and micro-architecture trade-offs are often different as the task being offloaded change. This is a rather significant disconnect, exacerbated by the fast-paced, rapidly evolving field of artificial intelligence.

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