Distributed low-precision Training Without Mixed Precision

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Abstract

Low-precision training is one of the most popular strategies for deploying deep neural models on hardware with resource constraints. Fixed-point implementation of deep models has the potential to alleviate complexities and facilitate potential deployment on embedded hardware. However, most low-precision training solutions are based on a mixed precision strategy. In this paper, we present an ablation study on different low-precision training strategies and propose a solution for IEEE FP-16 format throughout the training process. We demonstrate the effectiveness of our solution with ResNet50 on the ImageNet-full dataset using a cluster with 128 GPUs. The experimental results show that it is not essential to use FP32 format to train deep models.

1 Introduction

Deep convolutional networks have widely been applied to the non-trivial machine learning problems in computer vision task [19, 18], and there has been a gradual advance in the model representation. However, complex models are computationally intensive, which makes it hard to deploy on embedded systems. To address this issue, there has been a surge of interests recently in reducing the model complexity of the deep model, including light-weight deep learning models utilizing computation/memory efficient operations, exemplified by MobileNet [14], ShuffleNet [29], quantization [4, 31, 17, 23] and pruning [10, 12]. Among these approaches, quantization that reduce the precision requirements for the weights and activations by representing network weights with low-precision (lower then FP32), thus yielding highly compact deep models compared to their floating-point counterparts.

Meanwhile, the quantization not only requires less working memory and cache but accelerate the computation speed and cuts down the energy consumption of the computational device. [6] has proved the feasibility of low-precision training in a well-conditioned situation. It has proved that reduce the precision of the data would not significantly change the distribution of the data, so it is feasible to replace float32 data with fixed-point data, which has dramatically reduced performance and space consumption. The details of the energy consumption of the different operations in different precision are presented in Table [1] However, it is necessary to adjust the order values to avoid overflow dynamically. Unfortunately, the statistical effects of low-precision computation during training are still not well understood. Therefore, if the pure low-precision computation is used throughout training, it is often challenging to match the statistical accuracies of traditional, higher-precision hardware architectures. Hence, the mixed-precision strategy is becoming popular. [4] proposed training with binary weights, all other tensors and arithmetic were in full precision. [5] extended that work also to binarize the activations, but gradients were stored and computed in single precision. [15] considered quantization of weights and activations to 2, 4 and 6 bits, gradients were real numbers. Besides the mixed-precision training strategy, most of the works are not adopted on large scale datasets like
ImageNet [7] and very deep models like ResNet [11]. Fixed precision training is a strategy that aims to tackle the challenge of the above problems. Currently, the state-of-the-art mixed-precision training strategy like [20] using the strategy of maintaining a master copy of weights in FP32, loss-scaling that minimizes gradient values becoming zeros, and FP16 arithmetic with accumulation in FP32 indicating that strategy is not a full FP16 training process. This strategy has significantly increased the training cost and hard to implement on a large-scale distributed system. What is more, a fully FP16 training strategy could also take advantage of the NVIDIA Pascal GPU, which support to accelerate the whole training process twice [13]. With mentioned above disadvantages, we viewed that the mixed-precision training strategy is an essential exploration to achieve pure FP16 training.

| Precision | Operation | Energy(pJ) | Area(µm²) |
|-----------|-----------|------------|-----------|
| FP16      | addition  | 0.4        | 1,360     |
| FP32      | addition  | 0.9        | 4,184     |
| FP16      | multiplication | 1.1    | 1,640     |
| FP32      | multiplication | 3.7    | 7,700     |

Table 1: The energy consumption of different operations in different precision

Training on FP16 reduces memory consumption by half compared with FP32. The main challenge of non-full FP16 training is that the FP16 has a narrower dynamic range than FP32. Some operations like Batch Normalization [16] require the computation of the sum of squares, square-root, and reciprocal operations to avoid zero variance, which requires high precision and a broad dynamic range. Thus, some works avoid to use Batch Normalization layer [25] or kept the precision of the parameters unchanged [30] to avoid facing this challenge. To tackle this problem, [11] has proposed Range Batch Normalization that normalizes inputs by the range of the input distribution. However, all the existing quantization solutions are based on 1-bit inference, which is insensitive to the gamma in the Batch Normalization layer before each ReLU.

In this work, we proposed to easily swap the position of the Gamma/Beta to solve this problem, which is a more straightforward approach to solve this problem. We also developed a low-precision training as an approach to accelerating the deep neural networks (DNN) training approach. There is no doubt that low-precision training would cut down the budget of the GPU storages, so scaling full low-precision training is also appealing. However, even for the traditional FP32 training model, scaling ImageNet-1k training would still waste great computational resources, communication bandwidth. Moreover, end-to-end training would be more efficient to train the models. [27] proposed Layer-wise Adaptive Rate Scaling (LARS) to address this issue.

Our specific contributions are:

1. Proposed a fully FP16 training without FP32 throughout the training process on ImageNet while maintaining model accuracy. To our knowledge, our proposed strategy is the first fully FP16 training solution without sacrificing accuracy.
2. We proved the scalability of our proposed FP16 training strategy over the large-scale distributed deep learning training cluster without accuracy sacrificed.

2 Related Works

Reduced precision methods for deep learning training is an approach to improving compute efficiency by reducing the precision requirements for the weights and activations by representing network weights with low-precision. Quantized weights significantly reduce memory size and access bandwidth, improve power efficiency exploit hardware-friendly bitwise operations, and accelerate inference throughput. Moreover, since the bandwidth is the major bottleneck of the distributed system [27], the mitigated bandwidth would also help to improve the utilization of the computational resources, thus accelerate the model training process. [9] has demonstrated that deep neural networks can be trained with minimal loss in accuracy, using 16-bit fixed-point representation. However, most of the low-precision training strategies were not using deep models like ResNet [11] and tested on large-scale datasets like ImageNet [7] because most low-precision training strategies are highly unstable. Accumulation of errors will collapse the accuracy of the whole model with the updating process by back propagation. It is challenging to deal with low-precision weights and stimulate researchers’ interest in new training methods. The main challenge lies when the learning rate is
very small, the stochastic gradient method updates the weight parameters. [1] applied their proposed algorithm to deep convolutional models where they analyzed the quantization sensitivity of the network for each layer and then manually decide the quantization bitwidths. [24] quantized the weights and activations of pre-trained deep networks using 8-bit fixed-point representation to improve inference speed. After each training iteration, the weights are binarized/discretized and rounded up, which leads to training stagnation [5]. Some updating gradients are not helpful for the training process [2]. Thus the straightforward approach that quantizing weights with a rounding procedure yields unsatisfactory results when weights are represented in low-precision numbers. The other approaches address this problem by using mixed-precision training strategies that using full precision and single precision together during the training procedure [21]. [20] that maintaining a master copy of weights in FP32, loss-scaling that minimizes gradient values becoming zeros, and FP16 arithmetic with accumulation in FP32.

3 Precision Standard

The IEEE Standard for Floating-Point Arithmetic (IEEE 754) [3] is a technical standard for floating-point computation, which specifies the exchange and arithmetic format and method of binary and decimal floating-point operations in a computer programming environment. The IEEE 754 standard requires support for a handful of operations. These include the arithmetic operations add, subtract, multiply, divide, square root, fused multiply-add, remainder, conversion operations, scaling, sign operations, and comparisons.

The standard mandates binary floating-point data be encoded on three fields: a one-bit sign field, followed by exponent bits encoding the exponent offset by a numeric bias specific to each format, and bits encoding the significant (or fraction).

To ensure consistent computations across platforms and to exchange floating-point data, IEEE 754 defines basic and interchange formats. However, although Google has introduced a BFloat16 training on its designed chips, Tensor Processing Unit (TPU) [26]. However, the design of BFloat16 has sacrificed computational versatility.

4 Full Low-Precision Training Strategy

In this section, we introduce a pure FP16 training strategy which is more memory-efficient than BFloat16 and Float32, without sacrificing training accuracy. We have explored the limitation of low-precision training.

4.1 Swap the BatchNorm

We have found Mantissa Underflow Risk and Exponent Underflow Risk during the Batch Normalization Layer training process. The underflow exception shall be signaled when a tiny non-zero result is detected.
Batch Normalization (BN) [16] is a popular technique that normalizes the activation statistics at the output of every layer, reducing dependencies across layers while significantly improving model accuracy. However, Batch Normalization requires some operations that require high precision and a broad dynamic range, including the computation of the sum of squares, square-root, and reciprocal operations to avoid zero variance, which requires high precision and a broad dynamic range. What is more, we analyze the variance of each layer $x_l$, denoted by $\text{Var}[x_l]$ (which is technically defined as the sum of the variance of all the coordinates of $x_l$). For the deep structure like ResNet, prevents $x_l$ from vanishing by forcing the variance to grow with depth, i.e. $\text{Var}[x_l] < \text{Var}[x_{l+1}]$ if $E[\text{Var}[F(x_l)|x_l]] > 0$. This causes the output variance to explode exponentially with depth without normalization for positively homogeneous blocks, which are detrimental to learning because it can, in turn, cause gradient explosion.

The most exponent-risky term is the gamma ($\gamma$) in the BN. For a layer with $n \times d$ - dimensional input $x = (x_1, x_2, \cdots, x_d)$, the traditional batch normalization would normalizes each dimension

$$\hat{x}^{(d)} = \frac{x^{(d)} - \mu^d}{\sqrt{\text{VAR}[x^{(d)}]} + \epsilon}$$

$$y^{(d)} = \gamma \hat{x}^{(d)} + \beta^{(d)}$$

where the given $\mu^d$ is the expectation of the $x^{(d)}$, $n$ is the batch size, and the $\text{VAR}[x^{(d)}]$ is the variance of the given input. $\gamma$ and $\beta$ are a pair of parameters to scale and shift the normalized value. The term $\sqrt{\text{VAR}[x^{(d)}]}$ involves sums of squares, and the learned that could lead to numerical instability as well as to arithmetic overflow when dealing with large values. Since the $\gamma$ is to scale on the related highly unstable term $\frac{1}{\sqrt{\text{VAR}[x^{(n)}]}}$, the potential of the arithmetic overflow would be enlarged.

To tackle the above challenges, an intuitive solution is to learn the $\frac{1}{\gamma}$ instead of $\gamma$. However, we have found that learning $\frac{1}{\gamma}$ instead of $\gamma$ would improve the training stability with hurting precision, since IEEE standard intrinsically defined the product of positive MAX and positive MIN $= 2^{\text{bit of mantissa} - 1}$.

$$\text{activation} - \beta \frac{1}{1 - \beta}$$

To address this problem, we propose to swap the position of residual connection and gamma ($\gamma$) in BatchNorm after the last convolution layer in each Residual Block means that less processing and less precision requirement when adding up results from 2 different branches in the computing chip.

### 4.2 Mantissa Underflow Risk - Exponent Term Dilemma

We found the fact that there is a dilemma between the Mantissa Underflow risk and the Exponent Term that the less Mantissa Underflow risk the more Exponent Term. The Mantissa Underflow is the process of aligning mantissa; digits may flow off the right end of the mantissa. In such a case truncation method such as chopping, the round is used. The mantissa underflow risk comes from the range of weights, which is proven not sensitive in [28].

However, we found that it can be easily tackled if introducing LARS-like method.

We do not use LARS, but we multiples output by 0.25 right after every BatchNorm in each Residual Block. Meanwhile, the BatchNorm in the stem is kept as it is.

### 5 Experiments

#### 5.1 Setup

In this section, we adopted the ResNet50 [11] on [7] a large-scaled GPU cluster with 128 GPUs. Our framework is PyTorch [22]. Hence, we have adopted an ablation study with 8, 64, 128 GPU set up with different precision in the same experiment set up. To note that, the learning rate and the batch size has a strong correlation. In our experiment, when the batch size is multiplied by $k$, multiply the learning rate by $k$. All other hyper-parameters (weight decay, etc.) are kept unchanged. Because the
training strategy of FP32 has many skills and data enhancement strategies to improve the training effect, to make a fair comparison, the training strategy of Resnet50 in FP32 precision was used from the public repository. All our experiments were conducted under the same settings. For large-scale training, all batch normalization is implemented in a single GPU, which means synchronous batch normalization is not used throughout the pipeline.

The initialization strategy of our experiments is a zero weight decay in all Batch Normalization layers, and zero $\gamma$ in the last Batch Normalization layer in every Residual Block. To avoid a sudden increase in the learning rate, allowing healthy convergence at the start of training, we adopted our learning rate schedule as the same as [8], which we set 5 round warm-up [11], decay the learning rate by 0.1 at 30th/60th/80th epochs. The total length of our training is 90 epochs, which are the same as [3].

5.2 Ablation Study

Table 2 depicts the ablation study of our proposed method. Our baseline (FP32) model is the single-precision storage, which is used for activations, weights, and gradients. All arithmetic is also in FP32. The FP16 precision indicated that all arithmetic and its related activations, weights, and gradients are all stored in FP16 precision. There is no master copy of any parameters that are stored in high precision. The experimental results show that the proposed pure FP16 training strategy does not sacrifice much precision. Under the same experimental conditions, compared with the traditional FP32 training strategy, our Top-1% accuracy is only reduced by 0.7%, which is acceptable in the large-scale image classification challenge.

Our experiments show it can be harmful to precision when the batch size is over $128 \times 32 = 4096$, and is fatal to convergence when batch size is over $256 \times 32 = 8192$ if we continuously use the "the batch size is multiplied by $k$, multiply the learning rate by $k$." strategy in [8] and this is even cannot be alleviated by using LARS [27].

| Precision | Chips | Batch Size | Top 1(%) | BN Swap | LARS | Source |
|-----------|-------|------------|----------|---------|------|--------|
| FP32      | 8     | 256        | 75.6     | No      | No   | Ours   |
| FP16      | 8     | 256        | 74.7     | No      | No   | Ours   |
| FP16      | 64    | 2048       | 75.3     | No      | No   | Ours   |
| FP16      | 64    | 2048       | 74.5     | Yes     | No   | Ours   |
| FP16      | 128   | 4096       | 74.5     | No      | No   | Ours   |
| BFloat16  | 256   | 16384      | 75.08    | No      | No   | Google [26] |
| BFloat16  | 256   | 32768      | 76.40    | No      | Yes  | Google |
| FP32      | 1024  | 32768      | 73.0     | No      | Yes  | Berkeley [27] |

6 Conclusion

In this work, we have analysed the details of the pure FP16 training strategy. We have established that the communication cost reduction, model compression and large-scale distributed training are three coupled problems. This is the first full FP16 training strategy on ResNet50 without sacrificing the accuracy on the ImageNet dataset, which is also the first solution for 5 exponent lower-bound for a wide range of deep learning training schemes.

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2https://github.com/PyTorch/examples/tree/master/imagenet
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