Modified quantum frequency standard on Hg-199 ions

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Abstract. The world around us depends on devices capable of producing or maintaining a signal with an extreme precision. Quantum frequency standards are the answer to this problem. This article presents a modified version of newly developed quantum frequency standard based on trapping Hg-199 ions by magnetic field. The new prototype was developed a while ago and now it was modified due to algorithm improvements and renewed digital hardware, analog and digital circuitry being reordered. Results for Allan deviation show 3 % improvement for long-term frequency stability and more than 5 % for short-term stability.

1. Introduction
The carrying out various scientific studies, transmitting information, determining the coordinates of an object strictly requires the use of time synchronization devices [1-12]. These devices have different principles of physical work, especially when applied at moving objects [4-10, 13-16]. In some cases, instruments based on highly stable quartz are enough to ensure the operation of on-board navigation systems, radio monitoring and radar stations [17-23]. In the case of operation of these devices for a long time in difficult conditions, a number of problems arise [4-9, 24-30], especially in case of large congestion. The accuracy of determining the position of the object is reduced. The use of optical fibers and optical information processing methods [18, 19, 31-36] do not solve this problem.

The modernization process of standards’ construction is not a trivial task, since the work of various blocks is related to each other. Therefore, the task of modernizing the frequency standard must be solved in a complex manner [1-5, 10, 24-30, 37]. By reducing the size and weight of the main units, the introduction of new algorithms for the automatic control system of the magnetic field and the photon registration system, the development of a system for automatic tuning of the resonant frequency, this task was realized within the framework of this work before the commissioning of the existing prototype.

2. Supplying scheme
The trap is the power consumer and the main operating unit of the standard. For a new small-sized design of the trap and driver, a switching circuit was developed.
To generate a signal of a certain type and control a power stage with a transformer, we have designed a miniature version of the driver. The signal is pre-amplified and sent through 2 single-shot channels to the key circuit, which accumulates energy in the primary winding of the transformer, feeding the trap electrodes. High response speed and good temperature parameters provide stable control over the RF signal.

The signals of the modulation frequency, clock frequency, as well as the input data received from the microcontroller are received at the counter input. The purpose of the counter is to generate a signal with variable count and pause windows, as well as to count photon pulses over the corresponding time interval. The counting of pulses is carried out with a positive or negative sign, depending on the half-period of the signal of the frequency synthesizer in which the photons were recorded. The resulting counting result characterizes the frequency detuning of the crystal oscillator, on the basis of which the microcontroller generates a control voltage that changes the frequency of the crystal oscillator.

After the assembly, experimental studies of the characteristics of the new prototype, as well as separately designed parts, were carried out. The signal from the driver was tested on a breadboard, which showed that there was no influence of parasitic components on the output signal spectrum. A review of residual oscillations after switching off the device was also carried out, which indicated a good tuning of the output circuit due to the absence of parasitic oscillations and dependences other than $\sim \exp(-t)$. The software was pre-tested in the ModelSim environment and then incorporated into the Standard.

3. Computing part

It was obvious that to implement a high-performance counter, the architecture of the entire block had to be changed. Simplification of the circuit consisted in dismembering the module into separate functions and transferring the latter to specific electronic devices. So, the detection function is now performed by a comparator or an optical detector, the microcontroller is engaged in the processing of the output data, and the conversion from the bit sequence to the analog signal of the DAC is performed. These measures significantly reduced the load on the counter processor, but the speed of its operation still did not meet the needs of the consumer. Unfortunately, with all the advantages, microcontrollers are much inferior in speed to programmable logic integrated circuits (FPGAs).

However despite all the advantages of programmable logic integrated circuits, they cannot completely replace the operation of a microcontroller. The fact is that FPGAs have less processing power, and also have no memory, which makes the operation of these devices very limited. Based on the experience of developing such devices, in this project it was decided to implement photon counting on FPGAs, and to process and transmit output data to peripheral devices on the basis of microcontroller technology.

In this work, an Altera FPGA of the MAX 7000S family, model EPM7128SLI84-10N, was chosen as the key element of the photon counting unit. This microcircuit operates at frequencies up to 147.1 MHz, and also has a low latency of 6 ns. Thanks to these parameters, the selected microcircuit will be able to quickly process large input data, and 8 logical blocks will not clutter the program code and
output intermediate results to check the FPGA operation algorithm. The choice of a programming tool in our case fell on the VHDL language. The latter surpasses Verilog in readability, but loses significantly in the amount of code.

For FPGAs from Altera, the company of the same name created the Quartus development tool, which was successfully modified by Intel specialists. Quartus software provides the ability to work with FPGAs from design to debugging within one CAD system. Within the framework of this project, the Quartus II version was used, this software supports operation for the selected FPGA, and also has some advantages over later versions: block design technology and hardware debugging capabilities using a logic analyzer. To check the hardware implementation and time characteristics of the project on the FPGA, the HDL-modeling system for digital devices - ModelSim was used.

4. Photon counting
The structure of the photon counting functional block, its structural diagram is shown in Figure 2. Initially, the signals of the modulation frequency, clock frequency, as well as input data received from the microcontroller are sent to the counter input. The task of the counter is to generate a signal with variable counting and pause windows, as well as to count photon pulses over the corresponding time interval.

![Figure 2. Block diagram of the photon counting functional block](image)

Pulses counting is carried out with a positive or negative sign, depending on the half-period of the signal of the frequency synthesizer, in which the photons were recorded. The resulting counting result characterizes the frequency detuning of the crystal oscillator, on the basis of which the microcontroller forms a control voltage that changes the frequency of the crystal oscillator.

The transmission of the signal parameters, during which the photons are counted, is realized via the serial peripheral interface SPI. This data transmission standard was created for simple and high-speed communication between the microcontroller and peripherals in full duplex mode - the mode of receiving and transmitting information. The SPI bus is designed according to the master-slave principle, and there can be several slaves. Data transfer using this protocol is carried out bit by bit, and
the synchronization frequency is generated by the master device, most often the microcontroller processor.

The operation of the block for transmitting data to the FPGA input via SPI is illustrated in the timing diagram (Figure 3). Input signals data00 and data01 set the parameters of the time of the counting and pause windows, the data for transmission are presented in the form of binary numbers. These values are transmitted bit by bit via the SPI interface; for this, special synchronization signals sdvig and strob are used. The synchronized operation of the FPGA and the microcontroller can be checked using the analog signal data1, the level of which at the leading edge of the sdvig pulses corresponds to the input data bits. Zeroing of the data1 signal on the strob edge occurs due to the end of the transmission of the input value data00, with the beginning of the next edge of sdvig, the number of the pause window (data01) will be transmitted.

![Figure 3. Input data transfer time diagram](image)

Filling the registers of the counting and pause windows with input values is carried out using the overwrite signal S. As the recording ends, namely on the strob front, the next block of the program checks the first two bits of the signal S. After filling the registers with input data, it is necessary to generate a photon counting signal, and its period should be constant and equal to the period of the modulation signal freq_m1. The freq_m1 front serves as the beginning of the digitization of the error signal. Since the work of the counter is performed on digital equipment, it is necessary to take into account the time of switching the FPGA from one logic signal level to another. If you do not take into account the effect of transient processes at the output, you can get the so-called signal race - a situation in which, due to the delay of the input signal relative to the output, false signals appear, and, accordingly, the device malfunctions. One of the options for eliminating the races at the counter output, the formation of the counting window should be shifted relative to the front of the modulation signal. For the same reasons, the photon counting does not stop when freq_m1 decays.

The counting of photon pulses is carried out during the counting windows in the positive and negative half-periods of the modulation signal; this data with the corresponding signs is transferred to the accumulating adder.

The final stage is transferring the count value to the microcontroller for generating the feedback signal of the automatic frequency control system. Output data, like input data, is transmitted via the SPI serial interface. To ensure the transfer of the result, the binary count number is converted into an analog signal using the auxiliary signals sdvig_out_filt and strob_out_filt, the functionality of the latter
is similar to the input sdvig and strob, respectively. The difference in the implementation of information transfer is additional protection against FPGA transients.

5. Conclusion
The use of newly developed blocks and the use of new algorithms for automatic tuning made it possible, while reducing the size of the structure of the standard on mercury ions by three times and the weight by more than 65% compared to the previously operated ground sample and surpassing the accuracy characteristics of the standard applied on rubidium atoms: short-term (from 100 to 10,000 seconds) by 5%, and at long intervals (1 day) by 3% in comparison with previously used designs.

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