Failure analysis for opening characteristic of high voltage and high-power silicon carbide module

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Abstract. According to the abnormal curve of opening characteristics in the process of double pulse test, the failure of 6.5kV/100A SiC module is judged, and it is preliminarily concluded that the gate of the module is damaged; The failure of the module is located by means of module anatomy, static characteristics test and chip screening test. It is concluded that the failure of the module is caused by the abnormality of two SiC MOSFET chips in the module; The damage of the chip was located by using stereomicroscope, OBIRCH, SEM and other equipment, and the root cause of MOSFET failure was studied by stripping anatomy. The preparation process of the gate and passivation strip on the MOSFET was poor, and the introduction of defects led to the breakdown of the gate unable to withstand high voltage.

Keywords: SiC MOSFET, Opening characteristics, Damage anomaly location, Failure analysis, Gate voltage breakdown.

1. Introduction

SiC (Silicon Carbide) materials, as the third-generation semiconductor materials, have a variety of excellent performance which is suitable for high voltage and high-power electronic devices, high-power electronic equipment based on SiC chips have lighter weight, smaller volume, faster switching frequency, higher voltage, higher temperature tolerance, etc. [1]. Thus, the power density and performance of the whole system are greatly improved [2]. Although most specifications of SiC MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) has not yet reached the ability to compete with Si IGBT (Insulated Gate Bipolar Transistor), in the medium and low voltage field SiC MOSFET has been rapidly developed, and occupies a certain market [3]. In the field of high-voltage and high-power devices, only Cree [4], The GEIRI (Global Energy Interconnection Researcher Institute) [5] and a few other foreign research and development institutions have publicly reported the development of 6500V SiC MOSFET module [6], and no commercial high-voltage and high-power devices have been put into the market. At present, there are few reports on the failure analysis of high-voltage and high-power silicon carbide modules. However, with the development of modules, it is of urgent feedback significance and importance to investigate the failure reasons of modules and internal chips for the optimization and improvement of modules and chips [7].
According to the abnormal test curve of the opening characteristics of the 6.5kV/100A SiC MOSFET module in the double-pulse dynamic test, the failure state of the module during and after the test was described in this paper. Combined with the internal circuit schematic diagram of the module, the failure possibility of the Gate (G), Source (S) and Drain (D) of the module were preliminarily analyzed. It was verified that the module failure was caused by the gate failure of two 6.5kV/25A SiC MOSFET in the internal parallel chip by means of disassembling the module, microscopic detection and internal chip electrical performance screening detection. After that, the chip failure was located by using stereo microscope and laser scanning positioning microscope. Finally, the chemical stripping method was used to verify that the root cause of gate failure is that the gate passivation bar is defective and cannot withstand high voltage and breakdown.

2. Module packaging structure and dynamic test circuit principle

In this paper, the failure reason of the opening process of the 6.5kV/100A single-channel full SiC power switch module developed by GEIRI is analyzed layer by layer during the double-pulse dynamic test. The module is composed of four 6.5kV/25A SiC MOSFETs and four 6.5kV SiC SBDs (Schottky barrier diode) [5] chip with parallel package, the circuits between chip with DBC (Direct Bonding Copper), and DBC with DBC are connected by 15mIL aluminum wire. After the SiC MOSFET and SBD power chips, DBC and copper substrate are welded back, they are installed into the corresponding plastic packaging shell and filled with silicone gel with insulation function to protect the inside of the module. After the final packaging is completed, the physical object is shown in Figure 1(a), and the simplified internal circuit principle of the module is shown in Figure 1(b).

![Figure 1. Appearance and circuit structure principle of 6.5kV/100A SiC MOSFET module](image)

The module failed during the double-pulse turn-on and turn-off test. The test conditions were bus voltage \( V_{DS}=V_{CC}=3600\,\text{V} \), gate source voltage \( V_{GS}=-5\,\text{V}/+20\,\text{V} \), drain current \( I_D=94\,\text{A} \), gate resistance \( R_G=33\,\Omega \), and test temperature \( T_f=25^\circ\text{C} \). Figure 2 shows the circuit principle of the module during the double-pulse dynamic test. During the test, the Lower Driver of MOSFET connected to the gate of the SiC module controls the gate voltage of the SiC module and provides a double-pulse pilot signal.
3. Opening characteristic test and failure status

In opening characteristic test, when the first pulse signal of double pulse test is introduced, the abnormal module open features was found. The system detected the abnormal process and stop to test immediately. The changing process of the curves of \( V_{\text{GS}} \) (Gate-Source voltage) and \( I_{\text{GS}} \) (Gate-Source current) were recorded as shown in Fig. 3. And the changing process of the curves of \( V_{\text{DS}} \) (Drain-Source voltage) and \( I_{\text{DS}} \) (Drain-Source current) were recorded as shown in Fig. 4.
According to the curves in Figure 3: After the gate voltage $V_{GS}$ increases to the gate threshold voltage $V_{GS(th)}$, the module starts to conduction. However, when the $V_{GS}$ continues to increase to 15V, there is a small drop and then it begins to appear abnormal oscillation significantly. The positive maximum value exceeds 25V, and the negative maximum value drops out of the range of -10V. During this period, the gate current $I_{GS}$ also showed abnormal oscillation with the amplitude exceeding 25A. In the same period of time, the drain current $I_{DS}$ also drops sharply and is close to zero after it increases to about 100A quickly. The drain voltage $V_{DS}$ drops sharply to 500V and then has a large abnormal oscillation, with the maximum positive oscillation reaching 4kV. After the oscillation, it recovers to a stable state of 3.6kV.

After the above anomalies, the gate voltage $V_{GS}$ shows the stable state of 5V after the period of underdamped vibration attenuation, while the gate current also maintains the steady state of about 0.5A, while the drain voltage continues to be 3.6kV, and the drain current is close to zero. It shows that after the oscillation of the gate voltage, the drain source of the module has been turned off. Although the gate voltage is stable to 5V, which is greater than the threshold voltage, the module still cannot be turned on again.

By the curves of flat steady-state phase of the gate current and the gate voltage after the abnormal oscillation, we can see that the state between the gate with the source have failed in the module, which is equivalent to the work status of the constant resistance after conducting. It indicates that, the gate-opening control capability have failed in the early stages of the gate voltage increases, and directly affects that the conduction process of the drain-source cannot be controlled. After the static test verification, it is further proved that the opening characteristics of the module gate-source have failed, but the blocking characteristics of the module are also in a normal state. Moreover, according to the analysis of the gate voltage pulse curve, the cause of the abnormality is due to the failure of the module gate under pulse loading. Although the drain-source has a voltage of 3.6kV, the current is still zero, indicating that the drain-source has not broken down. Therefore, this paper will mainly analyze the gate-source failure of the module.

In order to further verify the cause of failure, firstly it is necessary to determine the failure position in the module. In this paper, the backward analysis of the above modules with gate-source failure in the turn-on characteristics during the double pulse dynamic test is continued to implement. After the module is disassembled, the plastic package shell is removed, and then the silica gel is dissolved. The internal state of the remaining module with substrate is as follows the figure 5. Through the observation of

![Figure 4. The curves of $V_{DS}$ and $I_{DS}$.](image-url)
stereomicroscope, it can be directly seen that there are obvious ablation black spots near the gate bonding line pin of the MOSFET chip D, as shown in the following figure 6. As shown in, according to the large amplitude oscillation of the gate pulse test curve beyond the normal range (-5V~+20V) during the turn-on process, it can be shown that the SiC MOSFET chip is likely to be unable to withstand the high gate voltage, and breakdown after being subjected to the oscillating gate voltage. A high current density at the local position in the gate is generated, so that the gate of the MOSFET chip D was burn through at the failure point.

In order to further analyze whether there are other failed chips or parts in this module, we cut off the crimping bonding lines on the gate and source of the failed MOSFET chip D, and separate the MOSFET chip D from the module. The static test of the module shows that the gate-source breakdown voltage of the module is still greater than 30V, showing that the module still shows a failure state. It indicates that there are still failed devices in the remaining SiC MOSFET and SBD chips in the module. Therefore, the static performance of MOSFET and SBD chips in the module are screened with the probe tests separately. It is found that the static characteristics of MOSFET chip B, C and four SBD chips are normal, indicating that they have not failed. However, it is found that the gate, source and drain of MOSFET chip A show small resistance characteristics [8], indicating that the opening characteristics of the MOSFET chip A have failed. After that, the MOSFET chip A was microscopically inspected, and no ablative black spots were found, showing that the abnormal part of the chip A may be located in the chip interior below the electrode layer, and the damage point did not expand to the device surface. Therefore, the specific location of the failure point cannot be detected only through the appearance microscopic inspection, and other methods need to be taken to further locate the failure point.

The MOSFET chips A and D with static detection failure are further analyzed to study their failure modes. Firstly, the laser scanning microscope is used to locate the failure point (Optical Beam Induced
Resistance Change, OBIRCH [9]) of MOSFET chip A. Adding 0.18V DC between the gate and source of MOSFET A, and the current through the bonding line pin is 2.26mA. When thermally exciting the gate surface layer with the laser of the scanning microscope, there is a visible abnormal impedance change point on the surface of MOSFET chip A, which is located at the edge of the gate bonding area, as shown in Fig. 8.

So far, we have found out that the failure of the module is caused by the internal SiC MOSFET chips A and D. The damaged parts of the failed MOSFET chips A and D in the module are found by means of stereomicroscope and laser scanning microscope thermal excitation positioning, and the failure point positioning from the module to the internal chips is completed.

4. Chip delamination analysis
According to the located failure point, this paper uses the method of delamination to observe the root causes of the failure point. The Al electrode layers on the surfaces of MOSFET chips A and D are removed by chemical stripping, and the gate bonding area of the chip is scanned and checked. It is observed that the area adjacent to the source electrode at the gate bonding point on the surface of MOSFET chip D is severely burned, accompanied by metal melting and visible melting pits, as shown in Fig. 9. Moreover, there are many damage phenomena of passivation layer on the edge of bonding point and gate strip on the gate of chips A (Fig. 10) and D. Especially the damage of gate and gate strip of chip D is more serious. Under the electron microscope (SEM), the melting morphology can be observed at the damaged position of the passivation layer, showing typical voltage breakdown characteristics.

Combined with the stereomicroscope examination after stripping and comparing the previous failure positioning results, it is concluded that the damaged position of the passivation layer of SiC MOSFET chip A is consistent with the position of the abnormal impedance change point found in OBIRCH positioning. This shows that the failure of the MOSFET chip is due to defects in the gate passivation layer. During the opening process, when the gate voltage increases to a certain extent, the defective part is broken down, resulting in the damage of the passivation layer on the gate strip. After the breakdown, the current density increases sharply, and then the excessive heat is accumulated and burned completely. Combined with the detection results of the chip failure part after stripping. The chip D has the phenomenon of ignition, so that the metal layer and PI glue passivation layer are blackened by burning.

5. Conclusions
In this paper, the failure analysis of SiC MOSFET module with abnormal turn-on characteristics during double pulse test is carried out. According to the turn-on test curve, the root causes of module failure are deeply studied layer by layer from module to chip and then to the internal structure of chip gate. The following conclusions are drawn:
(1) By means of stereomicroscope surface damage microscopic inspection and I-V small resistance characteristic test and screening, it is found that the failure of the module is caused by the abnormal forward characteristics of two SiC MOSFET chips, and the failure location of the whole module is completed;

(2) The methods of stereo microscope scanning and laser scanning microscope thermal excitation (OBIRCH) to locate the abnormal impedance were used to locate the damage of the failed chip, and the failure location of the MOSFET chip was realized;

(3) Using the method of chemical stripping for the chip gate, the metal layer of the chip gate is removed. Combined with the failure location, SEM micro scanning is used to observe and analyze that the root cause of the chip failure is the defect of the gate passivation strip, and the damaged part presents a typical thermal ablation morphology after voltage breakdown. Therefore, this paper concludes that there are defects in the gate passivation strip of SiC MOSFET chip in the preparation process, resulting in the chip cannot bear too high gate voltage, so that the gate of SiC MOSFET chips A and D in parallel during the opening process of the module flows through too much current and burns through under the same gate voltage, loses the control ability of the chip opening process, and the module cannot be opened. So, the SiC module appears as the failure state with the opening characteristic.

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