Design of weak signal detection circuit of CMOS detector with large dynamic range by twice sampling method

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Abstract. In the field of detecting weak signals with large dynamic range, CMOS image sensor, as an optical sensor component, has the advantages of large dynamic range and wide spectral response range, and is often used to detect weak signals. The commercial CMOS image sensor system usually adopts the ADC with 16-bit accuracy, which can not satisfy the detection of weak signal in some cases. In this study, CMOS image sensor S10122 chip from Hamamatsu company of Japan was used as the core device. ADI company's 16-bit ADC chip LTC2182 and 16-bit DAC chip LTC1668 were used. The circuit was designed according to twice sampling principles to improve ADC accuracy. The results show that the accuracy of ADC can be improved from 16 to 18 bits under certain conditions.

1. Introduction
CMOS image sensor has the advantages of large dynamic range, wide spectral response range, high reliability and fast speed, etc. It is a kind of modulated spectral detector that can be used to measure two-dimensional materials[1-3]. On the other hand, low power consumption, high performance and mixed signal processing are the main development directions of ADC. The accuracy of an ADC is inversely proportional to its speed. In order to design a detection circuit with a large dynamic range of weak signals, it is necessary to use 16-bit ADC to achieve high-speed and high-precision ADC conversion results through further design to meet the requirements of the dynamic range of modulation spectral signals.

Generally, the dynamic range of CMOS image sensor is 1000:1 to 10000:1. Therefore, a 16-bit (65536) ADC is usually used to process the signal. However, this conventional CMOS image sensor cannot meet the requirements when studying weak signals with large dynamic range. In this paper, CMOS image sensor chip S10122 is used to study how to detect weak signals with large dynamic range. The full well capacity of a pixel unit of S10122 is 200M electrons, and the number of noise electrons is about 1000, so the dynamic range is 200000:1. The ADC of 16bit can not meet the requirements of quantification, so at least 18-bit ADC can meet the voltage quantification requirements of S10122 when detecting weak signals.

In the design, CMOS image sensor with large dynamic range is used as the core device to obtain the optical modulated spectral signal. In signal processing, a dual-channel 16-bit ADC chip and a 16-bit DAC chip are mainly used to build two sampling hardware circuits, and the signals are transmitted correctly to the upper computer for further processing through USB. The results show that the system accuracy can be improved from 16 to 18 bits.
2. Design of twice sampling circuit

2.1. Principle of twice sampling
In order to improve the accuracy and reduce the cost of ADC under the condition of guaranteeing the speed, the dynamic scale expansion method is adopted in the experiment, that is, twice sampling ADC. Principle of twice sampling ADC: firstly, the first rough measurement of measured voltage is made by using an analog-to-digital converter, and then the error value between the first measurement and the measured voltage is measured again. By adding and subtracting the weight of the first measurement and the value of the second measurement, the measurement result with higher accuracy can be obtained [4].

![Figure 1. Schematic diagram of twice sampling principles](image)

The principle of twice sampling is shown in Figure 1. The output voltage of the sensor is defined as Vx, and the first measurement value of Vx is denoted as N1 after the 16bit data collected by ADC is cached in FIFO. The data in FIFO are sent to DAC and converted into analog voltage denoted as V1, and then Vx and V1 are sent to 8-fold differential amplifier to get voltage denoted as V2. At this time, the obtained voltage value is the error value of 8-fold amplification. Then ADC is used to convert voltage V2 into 16bit data cache into FIFO, and the second measurement value is denoted as N2. The output result after FPGA processing is N1+N2/8.

2.2. Twice sampling circuit design
The schematic diagram of ADC circuit design is shown in Figure 2. In order to simplify the design of the entire circuit, the ADC chip LTC2182 with dual-channel 16-bit parallel output from ADI company is adopted in this experiment, and its maximum sampling speed can reach 65MSPS. The first sampling uses ADC channel 1, and the second sampling uses ADC channel 2. In order to make the signal transmission more stable, the input end of this ADC chip adopts differential signal transmission, so the ADT1-1WT chip is used to process the single-end input to obtain differential signal when designing the ADC circuits [5-6]. This ADC adopts CMOS parallel output mode and adds current-limiting resistance at the output end to prevent excessive current exceeding the rated value.
As shown in Figure 3, ADI's 16-bit parallel input DAC chip LTC1668 is adopted in this design. Since this DAC is current output type, LT1812 operational amplifier is adopted in the circuit design to convert current into voltage signal. High speed operational amplifier OPA606 was used in the subtraction amplifier circuit mainly to realize the subtraction of the two signals, and adjusts the gain by resistance R5. Finally, the obtained signal is sent to the second channel of ADC and converted into digital signal.

In terms of timing configuration, the whole circuit system is mainly controlled by FPGA. When ADC sampled parallel data is transmitted to DAC, the data must be synchronized. FIFO caches 16 bit of ADC output, and the FIFO read-clock should be consistent with the DAC sampling clock. The sampling clock of DAC is to sample data at the rising edge, which must meet the requirements of setting time and holding time, so the optimal situation is that the rising edge of the sampling clock is to sample data in the middle [7]. The DAC input digital signal was captured by the logic analyzer is shown in Figure 4. After the values of N1 and N2 are correctly collected, the value of N1+N2/8 is obtained through FPGA calculation.
2.3. **USB module design**

In order to transfer the data sampled by the second ADC to the upper computer, the USB module FX2 of Cypress company is adopted here. The communication mode between FPGA and FX2 is shown in Figure 5. FX2 receives data from FPGA through endpoint 6 and transfers data to upper computer through internal USB engine. The chip in FX2 module has Slave FIFO and GPIO external interface communication modes, in this design, Slave FIFO mode is mainly used for communication [8].

![Figure 5. Communication mode between FPGA and FX2](image)

The communication between FPGA and FX2 requires 8 signals: IFCLK: clock output by FX2, which can be connected to FPGA by FX2 output or FX2 by external clock signal as input. SLCS is FIFO chip selection signal; SLOE is FIFO output capability; SLRD is FIFO read signal; SLWR is a FIFO write signal; FD[15:0] is to transmit 16bit data line; FIFOADR[1:0] selects the address lines of the four FIFO endpoints. The simulation waveform of data sent from FPGA to FX2 module is shown in Figure 6.

![Figure 6. Simulation waveform of data sent from FPGA to FX2 module](image)

In order to make USB and upper computer transfer correctly, it is necessary to install the official firmware program. After installing the software, connect the FX2 module to the upper computer, install the USB driver, and burn the USB2.0 firmware. Download the FPGA program to FX2 module, select the endpoint of "Bulk in endpoint (0x86)" in the Control Center, and click Transfer Data-in to read 512 bytes of Data in the Data Transfer option on the right. After connecting and debugging the whole system, the Data content read to ADC output will be displayed in the information window of the Control Center.

3. **Results analysis**

3.1. **Twice sampling results**

Figure 7. shows the output of the CMOS image sensor as the input signal waveform of ADC. As seen from the diagram, the time unit of each large lattice of transverse coordinates is 4 μs, and each large...
lattice of longitudinal coordinates is 1 V. Under normal light irradiation, the output voltage of CMOS image sensor is about 2V, and the frequency is maintained at 125KHz. In one cycle, the high level means that the internal switch of the CMOS image sensor is closed once, and the voltage signal of a pixel is output. Low level means that the internal switch is disconnected and the junction capacitance of the photodiode in the pixel is in an integral state, at which time there is no signal output. The output results of V1 after conversion by ADC and DAC are shown in Figure 8. The collected signals are almost identical with the output signals of sensors, indicating that the circuit design and timing configuration of ADC and DAC are correct.

![Figure 7. Waveform of voltage Vx](image1)

![Figure 8. Output waveform of voltage V1](image2)

Figure 9 is an error value between the voltage Vx to be measured and the DAC output voltage V1. After the oscilloscope is adjusted, the output of the module is detected by the probe, and the result is that the signal strength is about 1 mV. Due to the precise scope of the oscilloscope itself, the whole circuit generates some noise and there is some error in itself. The results show that the output waveform of the oscilloscope is basically in accordance with the design requirements.

![Figure 9. Error voltage waveform of signal subtraction](image3)

3.2. USB transmission results

After each module is connected and relevant software is installed, the data collected in the USB Control Center window is shown in Figure 10. IN "BULK IN transfer", 1 column of data on the left is used to mark the number of rows received by the upper computer software to record the data received by the upper computer, while the whole block on the right represents the collected data. The data collected in the window is a part of the real-time data of the whole system. Through the data collected in the window, it shows that USB module can correctly realize data transmission.
4. Conclusion

In the whole system, the CMOS sensor is used to detect weak signals by twice sampling method. This method can also be used in other scenarios to improve ADC accuracy. According to the actual needs, ADC with different accuracy and multiple of differential amplifier can be selected to build corresponding hardware circuit, so as to realize the conversion from low-precision ADC to high-precision ADC. The final test results show that the hardware circuitry can transfer the signals acquired by the CMOS image sensor to the upper computer properly after processing.

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