Tungsten Diselenide Top-gate Transistors with Multilayer Antimonene Electrodes: Gate Stacks and Epitaxially Grown 2D Material Heterostructures

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We have demonstrated that with e-beam deposition of a thin Al2O3 layer before atomic layer deposition, a uniform Al2O3 film can be obtained on WSe2/sapphire samples. Device performances are observed for WSe2 top-gate transistors by using oxide stacks as the gate dielectric. By using thermal evaporation, epitaxially grown multilayer antimonene can be prepared on both MoS2 and WSe2 surfaces. With multilayer antimonene as the contact metal, a significant increase in drain currents and ON/OFF ratios is observed for the device, which indicates that high contact resistance between metal/2D material interfaces is a critical issue for 2D devices. The observation of multilayer antimonene grown on different 2D material surfaces has demonstrated less dependence on the substrate lattice constant of the unique van der Waals epitaxy for 2D materials. The results have also demonstrated that stacking 2D materials with different materials plays an important role in the practical applications of 2D devices.

With increasing demand for smaller electronic devices, <3 nm technology node has become a bottleneck in Si industries. Therefore, in addition to traditional Si or strained Si materials, people have started to turn their attention to 2D materials 1–5. Unlike bulk materials, 2D materials can exhibit material characteristics in just a few atomic layers. The thickness is usually below 1 nm, which is advantageous for device fabrication in the nm range. One of the most studied 2D crystals in the last decade is graphene6. With its ultrahigh mobility value, researchers believe that the material can be used for next-generation high-speed electronics. However, the zero bandgap nature of this material has limited its applications in logic circuits. Thus, people have gradually turned their attention to other 2D materials, such as transition-metal dichalcogenides (TMDs). The major advantage of TMDs is that these materials have bandgaps, and transistors with high ON/OFF ratios can be fabricated on these materials7. However, their limited field-effect mobility values have raised another concern for practical applications. Recently, researchers have again moved their research focus to other group V 2D materials, such as phosphorene, which is also known as black phosphorus (BP)8. BP is expected to have high mobility values and a bandgap value of approximately 1.75 eV. However, its device application is hindered by the rapid degradation of bP under atmospheric conditions9,10. Compared with MoS2 transistors, enhanced transistor performances based on WSe2-graphene lateral heterostructures have been demonstrated in another publication11. High ON/OFF ratios up to 107 and acceptable mobility values up to 84 cm2/V·s were observed for the device. The results demonstrated that selenide-based materials can be a promising 2D material for electronic device applications.

However, for the application of 2D materials in transistors, there are two major challenges. Although bottom-gate transistors are frequently adopted in the literature to demonstrate the unique characteristics of 2D materials, the major device architecture that is on the market is the top-gate transistor. Therefore, one of the challenges lies in the growth of high-quality dielectric layers on 2D material surfaces. Because there are no dangling
bonds on 2D material surfaces, it is difficult to grow dielectric layers directly on 2D material surfaces. Buffer layers and special treatments may be required before dielectric layer growth.\textsuperscript{12,13} The other challenge for 2D devices is the choice of metal contacts. Unlike traditional semiconductors such as Si or GaAs, it is difficult to obtain Ohmic contacts between conventional metals adopted for semiconductor devices and 2D materials. It has been proposed in previous publications that by using either graphene or crystallized thin indium (In) films as the contact metals, significant contact resistance reduction can be observed for 2D devices.\textsuperscript{11,14} The results have demonstrated that one possible solution for the choice of contact metals for 2D devices may be conducting crystals. In this paper, we have demonstrated that with a predeposited thin Al$_2$O$_3$ layer using an e-beam evaporator, a uniform dielectric layer can be obtained on WSe$_2$ surfaces after atomic layer deposition (ALD) of an additional Al$_2$O$_3$ layer. By using the oxide stacks as the gate dielectric, device performances are observed for the WSe$_2$ top-gate transistors. By using epitaxially grown multilayer antimonene on WSe$_2$ surfaces as the contact metal, significant increases in drain currents and ON/OFF ratios are observed.

Results and Discussion

**Monolayer WSe$_2$ growth by using chemical vapor deposition.** A picture of the WSe$_2$ sample taken under an optical microscope is shown in Fig. 1(a). As shown in the figure, triangular WSe$_2$ flakes with widths of 100–200 µm are obtained after the chemical vapor deposition (CVD) growth procedure. Also shown in the figure, smaller triangular WSe$_2$ is present on the centers of some large WSe$_2$ flakes, which suggests that a second or even third layer of WSe$_2$ starts to grow from the center of the large flakes. The results demonstrate that the growth of WSe$_2$ may initiate from a seed. The lateral growth rate of WSe$_2$ on the sapphire substrate should be much faster than that on WSe$_2$ surfaces. In this case, large WSe$_2$ flakes would form before the second layer of WSe$_2$ starts to grow on top of the large flakes. During CVD growth, H$_2$ gas may act as the catalyst. Without H$_2$ gas, the selenization procedure would not take place. To verify the thickness/layer numbers of the WSe$_2$ flakes, the atomic force microscope (AFM) image of one WSe$_2$ flake is shown in Fig. 1(b). The line profile on the edge of the WSe$_2$ flake is also shown in the figure. As shown in the figure, the height of the flat WSe$_2$ flake is around 0.686 nm, which is close to the thickness (0.7 nm) of mono-layer WSe$_2$.\textsuperscript{15} The results reveal that mono-layer WSe$_2$ flakes are obtained by using CVD. The Raman spectrum of the sample is shown in Fig. 1(c). As shown in the figure, two characteristic Raman peaks corresponding to the lateral vibration mode E$_{2g}^{1}$ and the longitudinal vibration mode A$_{1g}$ located at 250.3 and 261.8 cm$^{-1}$, respectively, are observed. The observation of the two Raman peaks suggests that single-crystal WSe$_2$ is obtained by using CVD.\textsuperscript{15} The photoluminescence (PL) spectrum of the sample is shown in Fig. 1(d). Intense luminescence intensity located at 753 nm is observed. Because of the large exciton binding energy of WSe$_2$, the exciton emission in monolayer WSe$_2$ dominates the photoluminescence spectra at room temperature with emission peak at 1.625–1.660 eV (763–747 nm).\textsuperscript{16} The emission peak shown in Fig. 1(c) is at 753 nm (~1.65 eV), which is lower than the direct band gap value of ~1.89 eV for monolayer WSe$_2$ on sapphire substrates due to the deduction of the exciton binding energy.\textsuperscript{17} A schematic diagram of the exciton transition energy for monolayer WSe$_2$ is shown in Fig. 1(e). The exciton transition energy (E$_{pl}$) of monolayer WSe$_2$ can be estimated by using the equation E$_{pl}$ = E$_g$ – E$_{bi}$, where E$_g$ and E$_{bi}$ are the band gap energy and exciton binding energy of monolayer WSe$_2$, respectively. The exciton binding energy thus obtained is 0.24 eV, which is consistent with previous results.\textsuperscript{17} Since multilayer WSe$_2$ turns into an indirect bandgap material, the intense PL intensity...
suggests that single-crystal and monolayer WSe$_2$ with large flake sizes are obtained by using the CVD growth technique.

**Dielectric layer growth on WSe$_2$ surfaces.** One major challenge for the fabrication of 2D material top-gate transistors is the growth of the dielectric layers. To investigate this phenomenon, 30-nm Al$_2$O$_3$ is grown directly on two WSe$_2$/sapphire samples by using atomic layer deposition (ALD) at 150 and 180 °C. The atomic force microscopy images of the two samples are shown in Fig. 2(a). As shown in the figure, flat Al$_2$O$_3$ films can be grown uniformly on sapphire surfaces at the two different growth temperatures. However, grained Al$_2$O$_3$ films are observed on the WSe$_2$ surfaces. On the edges of the WSe$_2$ flakes, reduced Al$_2$O$_3$ grains are observed for the sample grown at 150 °C. The phenomenon became more pronounced as the growth temperature increased to 180 °C. Due to the lack of dangling bonds on 2D material surfaces, a non-uniform precursor distribution is obtained during the ALD growth procedure. In this case, grained Al$_2$O$_3$ instead of a flat oxide film is observed on 2D material surfaces. With increasing growth temperatures, the precursor on the 2D material edges is attracted to the sapphire substrate, and therefore, a region ~ 200 nm in width with no oxide coverage on the WSe$_2$ edges is observed in the AFM image of the sample grown at 180 °C, as shown in Fig. 2(a). The two phenomena would both induce high gate leakage currents and result in device failure. To improve the quality of the dielectric layer, a thin 5-nm Al$_2$O$_3$ film is deposited by using an e-beam evaporator before the ALD growth of another 20-nm layer of Al$_2$O$_3$. The growth temperature for ALD is 180 °C. The AFM images of the sample are shown in Fig. 2(b). As shown in the figure, uniform Al$_2$O$_3$ films are observed on both the sapphire and WSe$_2$ surfaces. The depth profile also shown in the figure reveals an ~ 1 nm step on the WSe$_2$ edges with the sapphire substrates, which is close to the 0.7-nm layer thickness of monolayer WSe$_2$. The results have demonstrated that with an additional 5-nm Al$_2$O$_3$ film deposited before ALD growth, uniform Al$_2$O$_3$ coverage can be obtained on 2D material surfaces. Unlike the absence of oxide growth on WSe$_2$ edges, uniform Al$_2$O$_3$ growth across the interfaces is observed for the sample with the thin e-beam-deposited Al$_2$O$_3$ layer.

**Top-gate WSe$_2$ transistors.** The fabrication procedure of the WSe$_2$ top-gate transistors is shown in Fig. 3(a). After WSe$_2$ growth, 80 × 80 μm$^2$ S/D electrodes with 100 nm Au/10 nm Ti are fabricated on the WSe$_2$ surface following standard photolithography, thermal evaporation and metal lift-off procedures. After the S/D definitions, a 25-nm dielectric layer with a 5-nm e-beam-deposited Al$_2$O$_3$ layer before the 20-nm ALD-grown Al$_2$O$_3$ layer is prepared on top of the whole sample. Although the e-beam-deposited Al$_2$O$_3$ layers can provide better coverage of dielectric films, dielectric layers prepared by using ALD can provide more complete film growth with a proper choice of seeding layers on 2D material surfaces, which will lead to lower gate leakage currents. After that, the gate electrode with 100 nm Au/10 nm Ti is fabricated on the WSe$_2$ channel. The $I_{D}$-$V_{GS}$ curve of
the device at $V_{\text{DS}} = 2\, \text{V}$ is shown in Fig. 3(b). The gate currents of the device are also shown in the figure. With a low gate leakage current down to $10^{-12}\, \text{A}$, it is demonstrated that the 5-nm e-beam-predeposited $\text{Al}_2\text{O}_3$ layer not only improved the film morphology but also depressed the gate leakage currents. Combining e-beam evaporation and ALD, we can avoid the problem of precursor distribution on 2D material surfaces with the help of physically deposited thin oxide layers (e-beam) and still obtain a flat dielectric layer through a chemical growth technique (ALD). In this case, n-channel transistor performances can be observed for the WSe$_2$ top-gate transistors. However, the drain currents of the device are relatively low, which would result in a low ON/OFF ratio of $5 \times 10^3$. There are several possible mechanisms responsible for this phenomenon. Since the channel is only monolayer WSe$_2$, although the e-beam-predeposited $\text{Al}_2\text{O}_3$ layer helps establish a working gate dielectric, the 2D material channel may still be damaged during the oxide deposition procedure. Thus, 2D material heterostructures may help to prevent the channel from the significant influence of the oxide interface$^{18}$. Further investigation is still required in the future. The other possible mechanism responsible for the low drain currents is the high contact resistance on metal/2D material interfaces.

van der Waals epitaxy of antimonene on WSe$_2$ surfaces. In one previous publication, it was demonstrated that single-crystal multilayer antimonene can be grown on MoS$_2$ surfaces by using molecular beam epitaxy (MBE)$^{19}$. Significant contact resistance reduction was observed in that paper. Since the growth mechanisms of thermal evaporation are similar to those of MBE, it is possible to grow multilayer antimonene on the same MoS$_2$ surfaces by using a thermal evaporator. To investigate this possibility, a 50-nm antimony film is deposited on MoS$_2$ surfaces by using thermal evaporation at 200 °C. The cross-sectional high-resolution transmission electron microscopy (HRTEM) image of the sample is shown in Fig. 4(a). As shown in the figure, similar to the MBE-prepared sample, well-stacked multilayer antimonene is also observed on the MoS$_2$ surface by using thermal evaporation$^{19}$. The results have demonstrated that by using a different growth technique of thermal evaporation with a lower vacuum requirement, elemental 2D material antimonene can also be grown on MoS$_2$ surfaces. Following similar growth procedures, a 50-nm antimony film is also deposited on the WSe$_2$ surface by using thermal evaporation at a reduced growth temperature of 120 °C. The Raman spectra of the sample is shown in Fig. 4(b). The Raman spectra are measured at the center of the WSe$_2$ flake after antimonene growth. Since multilayer antimonene will fully cover the WSe$_2$ surface, a similar Raman spectrum will be obtained across the WSe$_2$ flake. In addition to the Raman peaks corresponding to WSe$_2$, additional peaks are observed at 118 and 153 cm$^{-1}$ after antimony deposition, which correspond to the $E_g$ and $A_{3g}$ Raman peaks of antimonene, respectively$^{19}$. The similar Raman peaks to those of the MBE-prepared multilayer antimonene film grown on MoS$_2$ surfaces suggest that by using thermal evaporation, antimonene can also be formed on WSe$_2$ surfaces. To further investigate the
crystalline quality of the antimonene film, the cross-sectional HRTEM image of the sample is shown in Fig. 4(c). As shown in the figure, in addition to monolayer WSe2, well-stacked layered multilayer antimonene is observed. The layer separations of WSe2 and antimonene are 0.7 and 0.4 nm, respectively, which are consistent with previous publications. The similar well-stacked layered antimonene film grown on both WSe2 and MoS2 surfaces suggests that van der Waals epitaxy of the same 2D material may occur on different 2D material surfaces. Besides antimonene, in one previous publication, we have also demonstrated that other group-IV elemental 2D materials can also be grown on MoS2 surfaces. Since the lattice constants of these 2D materials are quite different, the results have demonstrated that the van der Waals epitaxy takes place on 2D material surfaces will help on the crystal growth of the epi-layers and is less dependent on the substrate constants. The lower dependence on the substrate lattice constant of the van der Waals epitaxial growth mode may create more possibilities for crystal growth on 2D material surfaces.

Conducting 2D materials as the contact metal. The device fabrication procedure for the top-gate WSe2 transistor with Au/multilayer antimonene electrodes is shown in Fig. 5(a). After WSe2 growth, 100-nm multilayer antimonene is deposited on the sample at 120 °C by using thermal evaporation. After that, 80 × 80 μm2 S/D electrodes with 100-nm Au are fabricated on the multilayer antimonene surface following standard photolithography, thermal evaporation and metal lift-off procedures. By using the Au electrodes as the hard mask, the multilayer antimonene outside the electrodes is selectively etched off by dipping the sample into a basic solution for 300 sec. The oxide growth and gate electrode deposition procedures are the same as those for the device with Au/Ti electrodes. The ON/OFF ratio also increases to 4 × 10^4. The results demonstrate that the high contact resistance between the electrode/2D material interface is indeed one mechanism responsible for the low drain currents of WSe2 top-gate transistors. By using multilayer antimonene as the contact metal, the contact resistance is effectively reduced, and higher drain currents can be observed for the device. The increasing ON/OFF ratio of the device also indicates that there is no additional leakage current created between the source and drain electrodes due to the additional multilayer antimonene growth on WSe2. The low gate currents at approximately 10−11–10−12 A also indicate that the etching procedure does not affect the surface property of WSe2 for subsequent Al2O3 growth. To further investigate this phenomenon, the RDS-VGS curves when using Au/titanium and Au/multilayer antimonene electrodes as the contact metal are shown in Fig. 5(c). The RDS values are obtained through the equation RDS = VDS/ID. Based on the equation RDS = 1/ID = Rcontact + Rchannel, RDS has contributions...
The cross-sectional HRTEM images were obtained by using a JEOL JEM-2800F TEM system operated at 200 kV. Surface morphologies, AFM measurements were carried out with a BRUKER Dimension ICON AFM system. Using a HORIBA Jobin Yvon HR800UV Raman spectroscopy system equipped with a 488 nm laser. To obtain the measured by using a Keithley 2636B system. The Raman and photoluminescence (PL) spectra were obtained \( \mu \) width were 5 and 40.

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In conclusion, we have demonstrated that with a predeposited thin Al2O3 layer using an e-beam evaporator, a uniform dielectric layer can be obtained on WSe2 surfaces after ALD of an additional Al2O3 layer. By using oxide stacks as the gate dielectric, device performances are observed for WSe2 top-gate transistors. With epitaxially grown multilayer antimonene on WSe2 surfaces using thermal evaporation as the contact metal, significant increases in the drain currents and ON/OFF ratios are observed. The results demonstrate that the high contact resistance between metal/2D material interfaces is a critical issue for 2D devices. The similar well-layered multilayer antimonene film grown on both WSe2 and MoS2 surfaces suggests that van der Waals epitaxy of the same 2D material may occur on different 2D material surfaces. The lower dependence on the substrate lattice constant of the van der Waals epitaxial growth mode may create more possibilities for crystal growth on 2D material surfaces. The results have also demonstrated that the stacking of 2D materials with different materials plays an important role in the practical applications of 2D devices.

**Methods**

For the preparation of WSe2, WO3 and pure Se were chosen as the precursors. WO3 \( (0.26 \text{ g}) \) was placed in a ceramic boat located in the center of the furnace tube heating zone. During the growth procedure, Se \( (0.45 \text{ g}) \) was placed in a ceramic boat maintained at 250 °C. The sapphire substrate was placed top down facing the \( \text{WO}_3 \) precursor in the center of the furnace tube. The \( \text{Se} \) vapor was transferred to the substrate using an Ar/H\(_2\) mixture gas as the carrier gas \( (\text{Ar} = 85 \text{ sccm}, \text{H}_2 = 15 \text{ sccm}, \text{pressure} = 100 \text{Torr}) \). The central heating zone was heated to 950 °C at a ramp rate of 20 °C/min for WSe2 growth. After reaching 950 °C, the sample was left for a growth duration of 30 minutes. After growth, the furnace was cooled to room temperature to remove the sample. For the top-gate transistor fabrications, two growth techniques of e-beam evaporation and ALD were adopted for the dielectric layer growth. The growth temperature for \( \text{Al}_2\text{O}_3 \) using the e-beam evaporator was 70 °C. After the deposition of 5 nm \( \text{Al}_2\text{O}_3 \) by using the e-beam evaporator, the other 20 nm \( \text{Al}_2\text{O}_3 \) layer is grown by using the ALD. Before growth, the reaction chamber was pumped down to 1 mTorr. Trimethylaluminium (TMA) and H\(_2\)O vapor were used as the precursor and reactant for aluminum and oxygen, respectively. Each ALD cycles consisted of a 20 ms TMA, a 5 sec. N\(_2\) purge, a 20 ms H\(_2\)O pulse, and a 5 sec. N\(_2\) purge. The growth temperature is kept at 180 °C. Devices with Au \( (100 \text{ nm})/\text{Ti} \ (10 \text{ nm}) \) and Au \( (100 \text{ nm})/\text{multilayer antimonene} \ (100 \text{ nm}) \) electrodes were fabricated using a thermal evaporator and standard photolithography and metal lift-off procedures. For the growth of multilayer antimonene on WSe2 surfaces, the same thermal evaporator was adopted. The chamber was pumped down to \( 3 \times 10^{-4} \text{Torr} \) before growth. Antimony flakes were loaded in a tungsten boat as the source. During the deposition procedure, the substrate was kept at 120 °C, and the deposition rate was 0.5 Å/sec. The channel length/width were 5 and 40 μm, respectively, for the devices. The I-V curves for the devices with different electrodes were measured using a Keithley 2636B system. The Raman and photoluminescence (PL) spectra were obtained using a HORIBA Jobin Yvon HR800UV Raman spectroscopy system equipped with a 488 nm laser. To obtain the surface morphologies, AFM measurements were carried out with a BRUKER Dimension ICON AFM system. The cross-sectional HRTEM images were obtained by using a JEOL JEM-2800F TEM system operated at 200 kV.

Received: 31 October 2019; Accepted: 25 March 2020; Published online: 06 April 2020

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Acknowledgements
This work was supported in part by projects MOST 108-2221-E-001-017-MY3, MOST 108-2622-8-002-016 and MOST 108-2911-I-001-507 funded by the Ministry of Science and Technology, Taiwan, and in part by the iMATE project AS-iMATE-109-41 funded by Academia Sinica, Taiwan.

Author contributions
Y.-W. Zhang and J.-Y. Li performed the material growth/characterizations and device fabrication/measurements. Y.-W. Zhang, C.-H. Wu, C.-Y. Chang, S.-W. Chang, M.-H. Shih and S.-Y. Lin clarified the experimental data and produced the manuscript. S.-Y. Lin is the group leader and oversaw this work.

Competing interests
The authors declare no competing interests.

Additional information
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