A technique to enable frequency dependent power savings in a level crossing analog-to-digital converter

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The level crossing analog-to-digital converters are meant for the effective conversion of sparse signals by construction. In these converters, the bandwidth-power trade-off requires a re-design of the comparators which takes a lot of time and effort to reach the application optimum point. Inspired by synchronous converters that have a dynamic power component that can be traded with bandwidth with the change of a clock frequency, a technique to allow such trade-off in the level crossing converter was developed. The resulting level crossing ADC has an input signal dependent dynamic power which can reach up to 42% OFF time during the conversion of sine waves, achieving 45.5% power reduction in the simulated design with TSMC 180nm PDK.

Introduction: The mathematical model of the level crossing conversion done by Allier et al in [1]. For this type of converter, there is no Nyquist frequency, but there are a frequency-amplitude curve which set the constraint to which the converter can still track the input signal. For a sine wave input, this relation is shown in the Inequality (1), where $A$ is the amplitude, $f_{\text{max}}$ the frequency, $\Delta$ the quantization level, $t_{\text{loop}}$ is the level crossing update loop time.

$$A \times f_{\text{max}} \leq \frac{\Delta}{2\pi \times t_{\text{loop}}} \quad (1)$$

The values of $\Delta$ and $t_{\text{loop}}$ are set during the design phase. Thus, while aiming to be efficient in the same low frequency spectrum of conversion as the SAR type ADCs, the level crossing ADC does not have the same post fabrication trade-off between bandwidth and power consumption via clock frequency control. In other words, the speed of the level crossing ADC is always over-designed for its application to the point that the total signal dependent power consumption may be inefficient. To change this scenario, a technique to power down the comparator during the time they are not being used is proposed and simulated. Being the comparators the only source of static power consumption, this technique enables power savings controlled by a clock signal which does not changes the asynchronous behavior of the architecture but does move the frequency-amplitude curve of its place.

The architecture: The modified ADC is shown in Figure 1. The ADC level crossing loop is controlled by a Burst Mode Asynchronous Finite State Machine (BM AFSM). The ADC update is event-driven by the crossing of the input signal from the floating analog window generated by the two CDACs ($V_{\text{in}} - V_{\text{ref}} = \Delta$). This state machine then updates the value of the Register which feeds the DACs with the new position for the floating window accompanying the input signal. While processing a level crossing, the comparators are powered down via an ON signal. In this architecture, this loop time can be controlled by the circuit in Figure 2 which is clock gated to prevent power consumption during self-transitions. The Figure 3 shows a timing diagram where a REQ+ represents the level crossing event which occurs asynchronously. Then, the clock signal is used to propagate the REQ signal to the ACK signal, completing the loop of the BM AFSM. As shown, the time of this propagation is determined by the next two adjacent rising edges of the clock signal, thus it is possible to increase the loop time by choosing an appropriate slower clock. This increase in loop time will later enable the architecture to trade bandwidth for power savings.

The comparators used are continuous time comparators. To prevent glitches during the power up of the comparator (which would be disastrous for the BM AFSM correct behavior), these parts are modified to include two reset switches that act to discharge internal nodes of the comparators. These nodes are related to the up-transition signal path of the comparator output, thus the discharge adds to the inertia of the output and prevents the propagation of the ON signal to the output. Circuit level simulation with the TSMC 180nm PDK showed correct behavior through all corners. The average ON power of the ADC was found to be $2.6\mu$W, dominated by the static power of the comparators and the average OFF power was found to be $0.2\mu$W, coming of the leakage current of the transistors.

Power reduction model: Based on the timing diagram, one can derive the power reduction model for the architecture based on the assumption that the moment the level crossing occurs is random and uniformly distributed along one clock period. The Equation 2 presents the boundary for the conversion of a sine wave input signal given a clock speed. The Equations 3 and 4 show the estimation of the power reduction given the previous assumptions. Where $A$ is the amplitude of a sine wave input, $f_{\text{max}}$ is the input frequency (maximum for the given amplitude), $\Delta$ is the quantization level, $t_{\text{OFF}}$ is the clock period, $I_{\text{OFF}}$ is the mean value of the off time after a conversion, $N_{\text{L}}$ is the number of level crossing during a measurement time called $t$. As said before, the $P_{\text{ON}}$ is mainly dominated by the static power of the comparators and the $P_{\text{OFF}}$ is mainly leakage current.
\[ f_{\text{max}} \times A = \frac{\Delta}{2\pi \times 2T_{clk}} \]  
\[ t_{OFF} = \frac{3 \times T_{clk}}{2} \]

The first intuition we can build from the expressions is the fact that the effectiveness of the technique for power reduction is better if the signal is more active, thus increasing the number of crossings per unit of time. To further guide the design choices for clock speed, some curves were built based on macro models of the converter and the control circuit. Figure 5 shows the optimal clock choice for a full-scale sine wave driving the input of the converter at given frequency. Note that, for a full-scale signal, the converter cannot correctly handle frequencies higher that what is bounded by the clock value. At that maximum frequency, the percentage of off time of the comparators converge to a value close to 45.5%, where small variations are expected given the random distribution of the crossing moment and the time of the simulation.

Finally, in Figure 6 one can see the bandwidth trade-off with respect to the chosen clock frequency. The top line is the limit set by the comparator at given input signal.

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