Low-power reliable SRAM cell for write/read operation

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Abstract: Low power SRAM cell is a critical component in modern VLSI systems. The major portion of the power dissipation in the SRAM cell is due to large voltage swing on the bit lines during write operation. In this paper, a low-power reliable (LPR) SRAM cell is proposed for minimizing the power consumption and to enhance the performance. A new write mechanism is proposed to reduce the charging/discharging activity on the respective bit lines. The cell is simulated in terms of power, delay and static noise margin (SNM). The simulated results show that write and read power of the proposed LPR cell are reduced up to 78% and 50% at 0.7 V (in 65 nm technology) respectively compared to the 6T cell. The proposed design achieves 2.4\times higher read static noise margin (SNM) than the 6T cell.

Keywords: low power, SRAM cell, power consumption, leakage current, SNM, and delay

Classification: Integrated circuits

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1 Introduction

SRAM represents a large portion of the chip, and it is expected to increase in future in both portable devices and high-performance processors. In many processors, SRAM caches occupy about 90% of the total chip area. Studies show that the power dissipated by cache is usually a significant part of the total chip power. Due to this fact, power consumption in the memory circuit has become an important consideration in the design of microprocessors. As the industry is constantly searching for low power and high speed memory to keep up with the advancement of VLSI circuits, new SRAM designs are being tested and evaluated to fulfill the demand of low power and high speed [1, 2]. Since, cache accesses include both read and write operations, therefore, it is required to reduce the power consumption during both operations. Many researchers have paid their attention for reducing the power consumption during write operation [3, 4, 5] and others for reducing the read power [5, 6, 7]. The proposed ZA [3] as well as low power 7T [4] SRAM cells are designed for power reduction in write ‘0’ operation. These cells gave hardware burden due to need of extra signal to control the switching activity of the extra included transistor. In the modern technology when the feature size is reduced drastically, supply voltage and threshold voltage must also reduce in same pace. The decrease in power supply reduces the power consumption quadratically but degrades the stability and access time. To overcome the stability problem in 6T cell, many new SRAM cells were proposed [7, 8, 9].

In this paper, we have proposed a new Low-Power Reliable (LPR) cell. The proposed LPR cell uses separate circuit for write and read operations to improve the read stability and performance. The cell is simulated in 65 nm CMOS technology using Microwind3 CAD tools [10] in terms of power consumption, area, read/write delay and static noise margin. During write operation, the latch property is broken to flip the data on the storage nodes faster. The write power consumption of the cell reduces due to lower discharging activity at the respective bit lines. The rest of this paper is organized as follows. In section 2, the architecture of the proposed cell is described. The simulated results and comparison are explained in section 3. Section 4 concludes the paper.

2 Architecture of proposed SRAM cell

The architecture of the Low-Power Reliable (LPR) cell is shown in Fig. 1(a). The cell is divided into two circuits: write and read circuits. The write circuit contains two cross coupled inverters namely inv.1 and inv.2. The inv.1 contains transistors T1 and T3 whereas inv.2 contains transistors T2 and T4. The access transistors T5 and T6 are connected to write word line (WWL) through transistors T9 and T10 respectively. During write operations the feedback path between two inverters is broken by transistors T7/T8 and the cell behaves as dynamic cell. Also, one of the bit lines is disconnected from the storage nodes due to off transistors T9/T10 which restricts the leakage current through the bit line. In the proposed SRAM, no extra signal is included as proposed by others [3, 4]. During the read operation/hold mode, BL and BLB are set at VDD which turns ON the feedback transistors and latch property of the cell is restored. The read operation is performed using
transistors T11 and T4. Transistor T11 is used to decouple the storage node Q from the read bit line during write operation/standby mode. The detail operation of the LPR SRAM cell is:

In write operation, set read word line (RWL) low. The write operation starts by breaking the feedback path. To write ‘0’ at node Q, the bit line (BL) has to be set at ‘0’ and BLB = 1 before asserting WWL to high. Transistors T7 and T10 turn ON while transistors T8 and T9 turn OFF. Once WWL is high, the access transistor T6 turns ON and the access transistor T5 turns OFF so that BL is disconnected from the node Q1 as shown in Fig 2(a). The high voltage at Q2 flips the node voltage Q low. To write ‘1’ at node Q set BL = 1 and BLB = 0. Now transistors T8 and T9 turn ON while transistors T7 and T10 turn OFF. The access transistor T6 is turned OFF by T10 which disconnect BLB from node Q2 (Fig. 2(b)). The high voltage at node Q1 (due to ON transistor T5) will result low voltage at the node nQ. Since nodes Q2 and nQ are connected through transistor T8, node Q will flip high. The read operation in the cell is performed by two transistors T4 and T11. The waveforms for write and read operations are shown in Fig. 1(c) and Fig. 1(d) respectively.
3 Simulation results and discussions

This section presents the detailed simulation analysis of the LPR SRAM cell for 65 nm CMOS technology with BSIM4 model parameters. The simulations are performed in terms of power consumption, access time and stability. Since in the 6T SRAM cell, one of the two bit lines must be discharged to low regardless of the written value, the power consumption in both writing ‘0’ and ‘1’ are same and high. In contrast, the 7-T cell [4] uses the complement of input data to perform the write operation that prevents the single write bit line from being discharged if the written value is ‘0’, therefore, the write ‘0’ power is far less than the write ‘1’ power. In the LPR cell, we are preventing any single bit line from being discharged during write 0 as well as write 1 operation, which saves considerable power as seen in Table I(a).

Table I. (a) Write power consumption and (b) access time (VDD = 0.7 V, Vth = 200 mV)

| SRAM cell | Write Power (µW) | Read Delay (ps) | Write Delay (ps) |
|-----------|-----------------|----------------|-----------------|
| 6T        | 0.016 4.938 4.944 0.016 | 80 80 128 128 |
| 7T [6]    | 0.004 0.987 5.073 0.017 | 80 91 62 136 |
| LPR       | 0.004 0.889 0.890 0.004 | 81 15 60 60 |

For read ‘1’ operation (Q = 1 & nQ = 0), transistor T4 turns OFF. Since RBL and node Q are at same voltage level, RBL does not discharge which reduces power consumption as shown in Fig. 3(a). During read ‘0’ operation, RBL discharges through two ON transistors T11 and T4. The average percentage read power reduction is 50% compared to the other cells (Fig. 3(a)). This is due to lower voltage drop (ΔV_RBL) on the read bit line. The write delay is defined as the time between the activation 50% of WL to when nQ is 90% of its full swing. Due to dynamic behavior of the cell, write access time is smaller than the other cells.
The read ‘0’ access time is faster compared to the 6T cell (Table I(b)). The read ‘1’ delay is same as the conventional 6T cell. The proposed cell can be used even in worse condition (\(T = 137^\circ C\)) with minimal power loss (Fig. 3(b)). This small change in power consumption is due to absence of leakage paths during read operation and due to isolation of write and read circuits. We have simulated the SRAM cells at different temperature for hold mode. In the proposed cell, increase in hold leakage power is less even at 137°C than the 6T cell (Fig. 3(c)) which makes the cell suitable for low power cache design. The minimum voltage required to flip the storage data at node Q high in the proposed cell for \(V_{DD} = 0.7\) V, \(T = 27^\circ C\), and \(V_{th} = 200\) mV is 290 mV. Due to source-follower action of transistors T5 and T9, the voltage at node nQ is only \((V_{DD}/C0) - 2V_{th}\) = 300 mV which degrades the write margin of the proposed cell. The write ability of the cell is further degraded if low threshold voltage transistor (\(V_{th} = 0.18\) V) is used at \(T = -40^\circ C\). The write margin of the proposed LPR cell improves significantly when \(V_{DD}\) is chosen to be 1 V instead of 0.7 V which is approximately 600 mV for \(V_{th} = 0.2\) V and \(T = 27^\circ C\) on the cost of increased power consumption (1.27 \(\mu\)W at \(V_{DD} = 1\) V). The read static noise margin (SNM) of the proposed cell (265 mV) is 2.4\(\times\) higher than the 6T cell (75 mV) due to isolated write and read circuits as seen from Fig. 4(a). When node nQ is at 0.7 V, node Q is maintained strictly at 0 V (see Fig. 4(a)). Due increased change in current by carrier diffusion at high temperature (\(T = 137^\circ C\)), read SNM decreases to 226 mV from its room temperature value. The percentage decrease in SNM as temperature increases from 27°C to 137°C is only 15% (Fig. 3(d)). Fig. 4(b) shows the variation of read SNM with different threshold

![Figure 3](image)

**Fig. 3.** (a) Read power consumption, (b) read power with temperature, (c) leakage power with temperature and (d) SNM of LPR with temperature.
voltage of transistor T11 at $V_{DD} = 1$ V. The read SNM shows a slight variation with $V_{th}$ due to low leakage current in the cell. The use of low threshold voltage reduces the read SNM to 258 mV compared to 51 mV of conventional 6T cell. The layouts of the 6T and LPR SRAM cells (Fig. 1(b)) are drawn using generalized 65 nm design rules. The proposed cell consumes 45% area overhead compared to the 6T cell. Because, the percentage of the cell array to cache area is about 70%, the overall cache overhead is roughly $(45\% \times 70\%) = 31.5\%$.

4 Conclusion

The proposed cell saves up to 78% power during write mode and 50% power during read mode compared to the 6T SRAM cell. Due to isolation of stored data from bit lines during read operation, the SNM of the proposed cell is $2.4 \times$ higher than the conventional cell. The simulation result shows significant improvement in write ability at $V_{DD} = 1$ V compared to the 0.7 V. Due to lower leakage current and power consumption, the proposed LPR cell is an attractive choice for mobile devices.