A FR4-based compact VCO with wide tuning range using SISL transformed triple-tanks

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This work proposes a compact voltage-controlled oscillator (VCO) using the transformer-based triple-tanks on substrate integrated suspended line (SISL) platform for 5G applications. In order to broaden the tuning range, the varactors are loaded on the second tank to avoid the effect of parasitic capacitance of bipolar junction transistors (BJTs) on the tuning range, and compact transformed triple-tanks are designed to decrease the parasitic capacitance. By using a compact transformed triple-tanks and double layers wiring technology, the core circuit area is only 0.1λg × 0.1λg, which is the smallest among the reported board-level VCOs. Although the low-cost FR4 is chosen, the phase noise is still acceptable by adopting cross-coupled topology and multi-tanks technology. The measured results show that the VCO exhibits a wide tuning range of 28.9% from 2.88 to 3.85 GHz, and the best phase noise is –119.45 dBc/Hz @1 MHz at 3.76 GHz.

Introduction: Compact and broadband transceivers draw much attention in 5G system. As the local oscillator of the transceiver, it is crucial for voltage-controlled oscillators (VCOs) to feature a wide tuning range and a compact size. A microstrip square open-loop multiple split-ring resonators in [1] and SIW cavity resonators in [2, 3] are used to improve the phase noise. However, these designs have a narrow tuning range and large size. In [4], a compact VCO is designed on a substrate-integrated suspended line (SISL) platform [5], but the tuning range is narrow. In order to increase the tuning range, a parasitic capacitance cancelling technique is presented in [6]. A SIW-based VCO using three tunings via posts on the cavity resonator is introduced [7], but this VCO is fabricated on high-performance Rogers 6010, of which the material cost is higher as compared to low-cost FR4 material.

In this letter, a compact VCO with wide tuning range, compact size and low cost is proposed on the SISL platform. Utilizing the double-layer wiring and the compact transformer-based triple-tanks, the SISL VCO has a compact size of 0.1λg × 0.1λg, where λg is the guide wavelength at the centre frequency of 3.37 GHz. By connecting varactors to the second tank of the triple-tanks, a wide frequency tuning range from 2.88 to 3.85 GHz is achieved. Low-cost FR4 are chosen for all substrate layers to reduce the cost. In order to compensate for the phase noise, we utilize the multi-tanks [8] to improve the quality factor. And a cross-coupled topology is adopted to suppress common mode noise.

The proposed vco design: Figure 1 shows the 3-D diagram of the designed VCO. This VCO contains five substrates (sub1 to sub5), among which sub1, 2, 4 and 5 are FR4 with a thickness of 0.6 mm and sub3 is FR4 with a thickness of 0.127 mm. Ten metal layers (g1–g10) on both sides of each substrate are copper with a thickness of 0.035 mm. The core circuit of the SISL VCO is realized on g5 and g6. Sub2 and sub4 are hollowed with a specific shape. Part of the edge of sub1 and sub2 are cut for the path of DC input and AC output. The VCO realizes the electromagnetic shielding of the air cavities and the connection of g1–g10 through via holes, which can reduce the radiation loss.

As shown in Figure 2, the core circuit of the VCO is designed on g5 and g6. The compact transformer-based triple-tanks are composed of tank1, tank2 on g5 and tank3, tank4 on g6. And the metal trace widths of tank1, tank2 and tank3 are 1.2 mm, 0.3 mm and 0.4 mm respectively. By decreasing the distance between tank1 and tank2, the coupling coefficient k12 will be increased, which can enhance the tank Q. Tank3 is stacked under the gap between tank1 and tank4, which can reduce the coupling capacitance brought by stacked coupling and therefore increase the self-resonant frequency of the transformer. Varactors C1 and C2 are inter-connected by via holes and share the common voltage Vc. Two bipolar junction transistors (BJTs) Q1 and Q2 are welded symmetrically to g5 and g6, respectively.

The circuit topology of the proposed crossed coupled VCO is shown in Figure 3a. The cross-coupled pairs of the VCO are formed of two BJTs Q1–Q2, and C1–C2 are varactors for frequency tuning. C is used as a block DC. Vb, Vc and Rb are used to provide the DC bias of the transistors. Tank1 and tank2 are used as a frequency selection network, and tank3 is adopted to convert the differential signal to single-ended output.

The simplified equivalent circuit of the VCO is shown in Figure 3b. L1, L2 and L3 denote the inductance of the triple-tanks. C1, C2 and C3 represent the parasitic capacitance of tank1, tank2 and tank3 respectively. The parasitic resistance of the transformer can be defined as R1, R2 and R3 respectively. R1 and R2 denote the overall resistance loss of the varactors. In this work, we define C1 and C2 as follows:

\[ C_1 = C_{pl} + C_{v1} \]  \hspace{1cm} (1)
\[ C_2 = C_{pl} + C_{v2} \]  \hspace{1cm} (2)

Fig. 1 3-D diagram of the designed VCO based on SISL

Fig. 2 Core circuit on sub3: (a) core circuit on g5 and g6. (b) top view of the circuit on g5. and (c) and top view of the circuit on g6

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According to the analysis in [9], the resonant frequency can be given by:

$$\omega_{L,II} = \sqrt{\frac{L_1C_1 + L_2C_2 \pm \sqrt{(L_1C_1 - L_2C_2)^2 + 4k_{12}^2L_1L_2C_1C_2}}{2L_1C_1L_2C_2(1 - k_{12})}}$$  \hspace{1cm} (3)

To take advantage of the Q enhancement of the triple-tanks, the oscillation is excited at lower resonant frequency $\omega_{L1}$. Without loss of generality, the capacitance ratio $\alpha_1 = C_{V1}/C_1$ and $\alpha_2 = C_{V2}/C_2$ are defined. In addition, since $C_{p1}$ with additional parasitic capacitance of the cross-coupled pairs is larger than $C_{p2}$, which results in $\alpha_1 < \alpha_2$, the tuning ability of $C_{V1}$ will be limited. Therefore, we load another two varactors $C_{V2}$ on the second tank without BJTs to broaden the tuning range. And due to the compact size with less parasitic capacitance, the tuning range can be further broadened.

Measured results: The proposed VCO was fabricated by using the PCB process. The photographs of the fabricated VCO are shown in Figure 4. Figure 4a shows the VCO structure on each substrate from sub1 to sub5. Figure 4b shows the core VCO circuits on sub3 with components soldered, and all of the five substrates fastened by screws are shown in Figure 4c, the overall VCO size is 20 mm $\times$ 19.45 mm and the core circuit area is 0.1 mm $\times$ 0.1 mm. As is shown in Figure 5, the best phase noise is $-119.45$ dBc/Hz at 1 MHz at 3.76 GHz. And Figure 6 shows that the output power is $-8.25$ dBm. It can be seen from Figure 7 that the frequency tuning range is 28.9% from 2.88 to 3.85 GHz, and during the entire tuning range, the phase noise is better than $-114.7$ dBc/Hz. Table 1 summarizes the performance comparisons of the VCOs on PCB.

Conclusion: In this letter, a high-performance transformer-based triple-tanks VCO using SISL technology is presented. Compared with other VCOs on PCB, the proposed VCO has advantages of wide tuning range, compact size and self-packaging. Moreover, the cost of the VCO is significantly reduced due to the use of low-cost FR4, which possesses a high practical value.

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Table 1. Performance comparisons of board-level VCOs

| Ref. | Technology | $f_c$ (GHz) | PN@1 MHz (dBc/Hz) | FTR <sup>(a)</sup> (%) | Size <sup>(b)</sup> ($\lambda_g \times \lambda_g$) | $P_{DC}$ (mW) | FOMT <sup>(c)</sup> @1 MHz (dBc/Hz) | Material cost |
|------|------------|-------------|------------------|------------------------|--------------------------|--------------|-------------------------------|---------------|
| [3]  | MWCL SIW cavity | 11.39 | -125.8 | 4.1 | 1.6 x 1.1 | 20 | -186.3 | High (Rogers 5880) |
| [4]  | MWCL SIISL TRS (Colpitts) | 4.16 | -132.1 | 4.1 | 0.15 x 0.24 | 17.3 | -184.4 | High (Rogers 5880) |
| [7]  | MWCL Tunable SIW | 1.95 | -130 | 26 | 0.2 x 0.25 | 51 | -187.4 | High (Rogers 6010) |
| [10] | EuMC SIW cavity (cross-coupled) | 11.6 | -105 | 0.68 | Null | 42 | -146 | High (Rogers 4003) |
| This work SISL transformer (cross-coupled) | 3.37 | -119.45 | 28.9 | 0.1 x 0.1 | 37.1 | -183.5 | Low (All FR4) |

<sup>(a)</sup> FTR is frequency tuning range, and $FTR = \frac{f_{\text{max}} - f_{\text{min}}}{f_c} \times 100\%$.

<sup>(b)</sup> Size is core circuit size, and $\lambda_g$ is the guide wavelength at $f_c$.

<sup>(c)</sup> $\text{FOMT} = \text{PN} - 20 \log \left( \frac{\text{FTR}(\%)}{10} \right) + 10 \log \left( P_{DC}(\text{mW}) \right)$.

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