Computing-in-Memory for Performance and Energy Efficient Homomorphic Encryption

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Abstract—Homomorphic encryption (HE) allows direct computations on encrypted data. Despite numerous research efforts, the practicality of HE schemes remains to be demonstrated. In this regard, the enormous size of ciphertexts involved in HE computations degrades computational efficiency. Near-memory Processing (NMP) and Computing-in-memory (CiM) — paradigms where computation is done within the memory boundaries — represent architectural solutions for reducing latency and energy associated with data transfers in data-intensive applications such as HE. This paper introduces CiM-HE, a Computing-in-memory (CiM) architecture that can support operations for the B/FV scheme, a somewhat homomorphic encryption scheme for general computation. CiM-HE hardware consists of customized peripherals such as sense amplifiers, adders, bit-shifter, and sequencing circuits. The peripherals are based on CMOS technology, and could support computations with memory cells of different technologies. Circuit-level simulations are used to evaluate our CiM-HE framework assuming a 6T-SRAM memory. We compare our CiM-HE implementation against (i) two optimized CPU HE implementations, and (ii) an FPGA-based HE accelerator implementation. When compared to a CPU solution, CiM-HE obtains speedups between 4.6x and 9.1x, and energy savings between 266.4x and 532.8x for homomorphic multiplications (the most expensive HE operation). Also, a set of four end-to-end tasks, i.e., mean, variance, linear regression, and inference are up to 1.1x, 7.7x, 7.1x, and 7.5x faster (and 301.1x, 404.6x, 532.3x, and 532.8x more energy efficient). Compared to CPU-based HE in a previous work, CiM-HE obtain 14.3x speed-up and >2600x energy savings. Finally, our design offers 2.2x speed-up with 88.1x energy savings compared to a state-of-the-art FPGA-based accelerator.

Index Terms—Homomorphic encryption, Computing-in-memory, encrypted data processing, cloud computing.

I. INTRODUCTION

There are growing concerns regarding the security and privacy of clients’ data stored in the cloud. Due to the nature of the cloud environments where computations need to be performed on outsourced data, Fully Homomorphic Encryption (FHE) [1], [2] may be a suitable solution for data security in the scenarios of data/computation outsourcing, because it enables any number of additions and multiplications on ciphertexts directly. However, additions and multiplications on ciphertexts accumulate noise, and a time-consuming bootstrapping mechanism is required to reduce the noises so that the final decryption contains the correct result.

Somewhat Homomorphic Encryption (SHE) [3], [4] enables a limited number of additions and multiplications on encrypted data without losing the ability to decrypt the results of encrypted computation. Notably, multiplications cause the noise of ciphertexts to grow at a much faster pace than additions. For this reason, the depth of a SHE implementation is defined in terms of the number of multiplications it can support without invoking bootstrapping, which is denoted as multiplicative depth. The multiplicative depth in the arithmetic circuits is limited to a constant number in SHE; however, as highlighted in [5], the number of operations on encrypted data is finite in many real-life applications. Therefore, the application of SHE instead of FHE may be sufficient and more practical because computationally intensive bootstrapping can be avoided.

While SHE enables secure and private computing in the cloud, the large size of ciphertexts (hundreds of KB) may result in low speeds due to long computation times as well as the need to constantly transfer data between memory and the CPU. New computing paradigms such as Near-Memory Processing (NMP) and Computing-in-Memory (CiM) are potential solutions for reducing the overhead of data transfers between memory and the CPU [6]–[10]. NMP reduces the energy and latency associated with memory accesses by placing processing units close to the memory. Alternatively, CiM lowers the number of overall memory accesses by integrating certain logic and arithmetic operations directly in either the memory cells or memory peripherals. Compounded with the benefit of fewer data transfers, CiM may offer further speedups in computation due to the inherently high internal bandwidth of the memory [11]. In other words, CiM-based solutions enable a high level of parallelism in their operations by processing many words simultaneously without data movement [11], which could reduce the time overheads in HE.

Recent research efforts have investigated whether compute-and data-intensive applications can be accelerated with NMP and CiM architectures based on different technologies, e.g., in [6], [11]–[19]. However, most of the previous work on CiM/NMP targets general purpose computation or specific machine learning tasks. When compared to traditional applications, HE (i) has much longer data words — in the order of hundreds or even thousands of bits, and (ii) features previously unsupported operations such as modulo reduction and scaling (division with rounding). That said, the CiM infrastructure in previous works have not been designed to perform multiplication of long words and polynomials efficiently (as required by some HE schemes). Furthermore, the integer $X$ modulo $q = 2^k$ operation and the PolyScale primitive present in HE...
require conditional execution of steps by the CiM components, as well as arbitrary division and multiplication by powers of two, which cannot be supported in previous works.

In this work, we introduce a CiM architecture to support the processing of encrypted data by employing the well-known Brakerski/Fan-Vercauteren (B/FV) SHE scheme that is designed with polynomial rings [3]. While we focus on the B/FV cryptosystem in this work, our architecture is directly applicable to other encryption schemes that incorporate similar operations (e.g. the BGV [20], GSW [21], TFHE [22], and CKKS [23] schemes. Our proposed CiM-HE targets four primitive polynomial operations used in the B/FV scheme: polynomial addition (PolyAdd), polynomial subtraction (PolySub), rounded polynomial scaling (PolyScale), and polynomial multiplication (PolyMult). Furthermore, we propose restrictions on the parameter settings to facilitate CiM-friendly solutions. Namely, CiM-HE employs moduli of \(2^k\) for some integer \(k\). Also, the PolyScale primitive assumes a divisor of the form \(2^k\) for some integer \(k'\). Our parameter settings do not impact the security of HE, but rather make it CiM-friendly. To enable full support to all of the essential operations of HE, we make the following circuit/architecture contributions:

**Division by arbitrary powers of two in memory:** The execution of PolyScale requires division by arbitrary powers of two in memory, which is achieved with large and varied number of bit shifts enabled by the bi-directional logarithmic bit shifter in our CiM architecture. Importantly, previous work [19] performs bit shifting in memory with configurable interconnects. However only a small number of unidirectional shifts were demonstrated in their architecture, which are not sufficient to meet the requirements of the HE operations.

**Conditional execution by the CiM architecture:** The execution of PolyScale and the Integer \(X\) modulo \(q = 2^k\) operation require conditional execution of atomic operations in the CiM architecture, which has not been done in previous work. For instance, the result of PolyScale might need to be rounded up depending on the rest of the division. Similarly, modular reduction needs to ensure that \(x_q \in [-\frac{q}{2}, \frac{q}{2})\). These conditions can only be checked at runtime by our CiM-HE. To support such conditional execution, we introduce a horizontal OR operation performed at the sense amplifier level. The result of this operation generates a flag that is interpreted by our CiM sequencing circuit. Namely, the sequencing circuit examines the flag value and take the appropriate action while executing the CiM operation.

**Polynomial multiplication in CiM:** The execution of PolyMult needs (i) integer multiplication and (ii) an efficient procedure to multiply polynomials of very large order in memory. We rely on carry select adders (CSLA) [24], in-place copy buffers [12] and logarithmic bit shifters to perform integer multiplication of long words. To realize polynomial multiplication with CiM-HE, we implement a CiM-friendly Karatsuba multiplication algorithm enabled by in-place move buffers (IPMB). The IPMBs allow us to move data from column \(i\) to column \(i + F\) in an array, where \(F\) is a pre-defined column offset. By performing this operation in \(c\) cycles, it is possible to move data with \(cF\) different offsets.

We perform simulations using Verilog and SPICE to evaluate speed and energy consumption of CiM-HE. We employ the BSIM-CMG FinFET model from [25] for a 14nm technology node, and compare the runtime of three HE primitives (HomAdd, HomSub, and HomMult, based on the four primitive polynomial operations) in our CiM-HE design — without algorithmic optimizations — against a CPU-based implementation based on the widely-used Microsoft Simple Encrypted Arithmetic Library (SEAL) [26] with various algorithmic optimizations enabled. Our results indicate speedups of \(>10000\) (4.6x) for homomorphic addition (multiplication), and energy savings for addition (multiplication) of \(>290\)x (530x) for a single execution of each homomorphic operation.

We also demonstrate the benefits of CiM-HE by evaluating widely used operations in data analytics, i.e., arithmetic mean, variance and linear regression, as well as inference, on encrypted data using HE primitives. The speedups (and energy savings) of CiM-HE varies by task. In our experiments with a memory size of 4MB (8 MB), we obtain maximum (minimum) speedups of \(>26000\) (1.1x) and maximum (minimum) energy savings of 532.8x (299.7x). Better speedups are obtained for tasks whose execution time is dominated by additions, e.g., in the arithmetic mean. Furthermore, compared to an alternative CPU-based HE based from [27], we obtain a 14.3x speedup and \(>2600\) energy savings for homomorphic multiplications. Finally, compared to a state-of-the-art FPGA-based SHE accelerator [5], our design is 88.1x more energy efficient with speedup of 2.2x for a security level of 80 bits and a multiplicative depth of 4.

II. BACKGROUND AND PRELIMINARIES

A. B/FV scheme based on RLWE and its polynomial primitives

SHE schemes based on polynomial rings and the NP-Hard Ring Learning-With-Error (RLWE) problem [3], [28] have become popular recently due to their security against quantum algorithms. Their implementations are widely available and actively maintained as well [22], [26], [29]. We focus on the well-known B/FV scheme [3] in this paper, but our design is easily extensible to the BGV [20], GSW [21], TFHE [22], and CKKS [23] schemes. The B/FV scheme takes in plaintext messages from \(\mathcal{R}_t := \mathbb{Z}[X]/\Phi_M(X)\), i.e., the set of residue classes of the polynomial \(\Phi_M(X)\) whose coefficients are from \(\mathcal{Z}_t\), and operates on ciphertext polynomials in \(\mathcal{R}_q := \mathbb{Z}_q[X]/\Phi_M(X)\). These sets form rings of polynomials under polynomial addition and multiplication. We provide a brief overview of B/FV SHE below. Details with respect to key generation, encryption, and decryption are omitted as the focus of this work is on the acceleration of homomorphic operations on encrypted data.

A plaintext message (e.g., numbers) can be encoded into a plaintext polynomial in \(\mathcal{R}_t\) with standard encoding techniques (e.g., integer encoding, fraction encoding [30]), which is then encrypted into a pair of polynomials in \(\mathcal{R}_q^2\), which is the ciphertext \(c = (c[0], c[1])\) of the plaintext polynomial.

\(^1\)In the applications of homomorphic encryption, key generation, encryption and decryption are one-time process, and the bottleneck lies in the homomorphic operations. The details can be found in the original publication [3].
Given two ciphertexts \( c_1 \) and \( c_2 \) which are ciphertexts of two messages \( m_1, m_2 \) respectively, homomorphic addition is defined as:

\[
HomAdd(c_1, c_2) = ([c_1[0] + c_2[0]])_q, [c_1[1] + c_2[1]])_q
\]

where \( q \) is the moduli of ciphertext polynomials and \([\cdot])_q\) for an integer denotes the reduction modulo \( q \) defined as \([x]_q = x - [x/q]\). When the input of \([\cdot])_q\) is a polynomial, the reduction modulo \( q \) is applied to all coefficients. The resulting ciphertext is the encrypted addition \( m_1 + m_2 \).

In Microsoft’s SEAL [26] that implements the B/FV scheme, homomorphic subtraction between two ciphertexts \( c_1 \) (minuend) and \( c_2 \) (subtrahend) is implemented as:

\[
HomSub(c_1, c_2) = ([c_1[0] - c_2[0]])_q, [c_1[1] - c_2[1]])_q
\]

Similarly, the resulting ciphertext is the encrypted subtraction \( m_1 - m_2 \).

The homomorphic multiplication between two ciphertexts \( c_1 \) and \( c_2 \) is defined as a series of polynomial operations. First, the following polynomials are computed:

\[
c_x = [[t(c_1[0] \cdot c_2[0])/q]]_q
\]

\[
c_y = [[t(c_1[1] \cdot c_2[1] + c_1[1] \cdot c_2[0])/q]]_q
\]

\[
c_z = [[t(c_1[1] \cdot c_2[1])/q]]_q
\]

Here, \( t \) is the moduli of plaintext polynomials. Then, the relinearization key \( r\ell k = (r\ell k_0, r\ell k_1) \) generated from the key generation algorithm (which is a pair of polynomials) is used to generate the final ciphertext, also a pair of polynomials:

\[
HomMul(c_1, c_2) = (c_x + \langle r\ell k_0, c_z \rangle, c_y + \langle r\ell k_1, c_z \rangle)
\]

Here, \((poly_x, poly_y)\) represents the inner product between two polynomials (i.e., the sum of coefficient-wise multiplications). The resulting ciphertext is the encrypted multiplication \( m_1 \cdot m_2 \).

The computations above are comprised of two types of operations: (i) ring operations, which are polynomial additions, subtractions and multiplications. These consist of modular additions and multiplications closed in \( \mathbb{Z}_q \). For ring operations, we support three primitive operations on polynomials: polynomial addition \((PolyAdd)\), polynomial subtraction \((PolySub)\), and polynomial multiplication \((PolyMult)\). Additionally, (ii) rounded polynomial scaling scales a polynomial by \( t/q \) and returns the closest polynomial in the ring, i.e., coefficients are rounded to the nearest integer and the tie is broken by rounding it up. For this step, our CiM-HE implements the rounded polynomial scaling \((PolyScale)\) as the final primitive.

B. Related Work

1) CiM and NMP designs for HE: CiM enables significant speedups and energy savings for data-intensive problems in multiple application domains, e.g., [6]–[11], [13]–[18]. CiM designs targeting SRAM-based caches [6] or main memory [7] have been fabricated. With respect to security-centric applications, CiM-based engines have been used for realizing encryption schemes such as AES [31], [32]. However, there is limited work regarding “in-memory” HE due to the complexity of operations involved in these encryption schemes (e.g., multiplication between ciphertexts that are hundreds of KB in size). In this regard, SCAM [33] proposes a modification to the homomorphic XOR and AND operations as defined in the FHEW scheme [34] in order to perform search operations on encrypted data using a fully-additive search function. CiM and NMP implementations of this search function were presented in [24] and [10], respectively. CiM and NMP approaches enable speedups and energy savings compared to [33]. To the best of our knowledge, there are no other works on the implementation of both homomorphic additions and homomorphic multiplications in either CiM or NMP.

2) Hardware Accelerators: Several hardware accelerators for HE have been proposed [5], [35]–[40]. Most designs are based on Field Programmable Gate Arrays (FPGAs), which provide an option for implementation of varied HE circuits. Some designs, e.g., [37]–[39], focus on the design of multiplier units for very large numbers, which are useful for performing homomorphic multiplications. For instance, references [39], [41] focus on the implementation of polynomial multiplication and the Fast Fourier Transform/Number Theoretical Transform (FFT/NTT), which are building blocks commonly used for fast multiplication. However, these works do not propose/evaluate a complete solution that enables the realization of a complete set of HE primitive operations, i.e., homomorphic additions and homomorphic multiplications, in a scenario of massive amount of data transfers.

Accelerators for general HE computation are proposed in [5], [35], [36], [39], [40]. References [35], [36] and [41] propose accelerating the YASHE [4] and CKKS schemes, respectively. The YASHE scheme has prohibitively large ciphertext sizes, which aggravates the impact of memory transfers on performance due to memory bandwidth limitations. This fact is not accounted for in [36]. Furthermore, the YASHE scheme is proven insecure as it is subject to a subfield lattice attack [42]. As for CKKS, this scheme is also based on polynomials operations (like the B/FV), but it can operate on floating-point numbers, which is amenable to machine learning applications. In [41], improvements of two orders of magnitude in homomorphic multiplication time are reported when compared to a CPU solution that implements CKKS. However, the work does not provide an evaluation for a larger workload, i.e., operations with a set of tens or hundreds of ciphertexts as likely to occur in a real-life setting are not included in the evaluation.

In this work, we evaluate the functionality of CiM-HE for the B/FV scheme. Likewise, [5], [40] can perform the essential operations of the B/FV SHE scheme, i.e., homomorphic multiplications and additions. To ensure the fairest comparison possible between different works, we do not compare CiM-HE to others that are based on different schemes, e.g., YASHE, CKKS, etc. Regarding prior work that focuses on the B/FV scheme, reference [40] reports a homomorphic multiplication time of 463.9 ms for 80-bit security, which is \(\sim92.8x\) more than the time reported in [5] for the same operation with same security level. As [5] represents a state-of-the-art FPGA-based HE accelerator, we choose to compare CiM-HE with that work in our evaluation (see Sec. IV).
III. CiM-HE Framework

In this section, we describe our proposed CiM-HE framework, which consists of CiM hardware as well as the mapping of primitives (PolyAdd, PolySub, PolyScale, and PolyMult) to a sequence of CiM-friendly steps. We also discuss HE parameter settings used by the CiM-HE framework.

A. Parameter settings for CiM-friendly HE

Per Sec. II polynomial primitives are always computed over polynomial rings $\mathbb{Z}_q$ with moduli $q$ for coefficients. To expedite the integer reduction modulo $q$ in memory, we set $q$ to be a power of two. Thus, the polynomial ring of interest is $\mathbb{Z}_{2^k} := \mathbb{Z}_{2^k}[X]/\Phi(X)$ for some positive integer $k$. When divisions are needed during the polynomial scaling, we divide the coefficients by powers of two, which can be done by performing bit shifting in memory. This choice of parameters does not affect the security of HE schemes [3], [43]–[45], because the RLWE problem is hard regardless of whether the moduli of the polynomial coefficients are powers of two instead of prime numbers or products of coprime numbers.

We have followed the widely-accepted analysis of Lindner and Peikert [46] to choose the parameters $n$ (ciphertext polynomial degree) and $\log_2(q)$ (ciphertext modulus size) to achieve an acceptable level of security in CiM-HE, i.e., $\geq 128$ bits. In Sec. IV, we compare the performance and energy consumption of CiM-HE to a CPU-based implementation with four $[n, \log_2(q)]$ pairs to achieve different multiplicative depths and levels of security. Furthermore, in Sec. IV we also compare CiM-HE with previous work, assuming the same parameter setting as [5], [27], which enables us to achieve 80-bit security and a multiplicative depth of 4.

B. CiM hardware

Fig. 1 illustrates our CiM hardware architecture. A CiM-HE bank (Fig. 1(a)) consists of multiple CiM-HE arrays of $M \times N$ size where ciphertexts are stored. When designing a bank, we should choose the number and dimension of the arrays based on (i) the number of ciphertexts we wish to store in a single CiM-HE bank, (ii) the coefficient’s modulus ($q = 2^k$), and (iii) the degree of polynomials ($n$). When positioning polynomials in the CiM-HE banks before a HE operation, we have to write the polynomials in a column-aligned fashion (so coefficients of the same degree are mapped to the same columns in the CiM arrays) to facilitate the execution of polynomial primitives by our CiM-HE hardware.

Figs. 1(a) and 1(b) illustrate the mapping of polynomial coefficients to the memory arrays in a CiM-HE bank. Recall that the ciphertext has the form $c = (c[0], c[1])$. In Fig. 1(a), we define arrays numbered 1 to $n_1$ to store the first polynomial ($c[0]$), while arrays numbered $n_1 + 1$ to $n_2$ store the second polynomial ($c[1]$). The coefficient mappings depicted in Fig. 1(b) are for arrays 1 and $n_1 + 1$. $M$ and $N$ are the number of rows and columns in an array, respectively. $M’$ is the number of rows reserved as a scratch space to store intermediate results of CiM-HE operations. The coefficients of the two polynomials $c[0]$ and $c[1]$ are labeled as $c[0][y][z]$ and $c[1][y][z]$, where $y$ is the index for the coefficients, and $z$ is the index for ciphertexts that are stored in memory. As such, each array holds up to $C = N/(w \times 64)$ coefficients of $M’$ ciphertexts. In this equation, $w$ represents the number of standard-sized 64-bit words that are necessary to store each $k$-bit coefficient. Namely, $w \times 64 \geq k$. The coefficients of $M$ different ciphertexts of the same degree are placed in
PolyScale is a new operation, "horizontal OR," in which the bitwise AND bit-wise logic between two memory words. We also introduce select adder and a customized sense amplifier that enables circuits similar to those in [12], [24], i.e., an in-memory carry with less area overhead. For instance, a log shifter with $L$ to other bit shifters such as a barrel shifter, the log shifter can perform right bit shifts that enable divisions by powers in memory in the subsequent cycle.

Computation, we keep the output (computation result) stored primitive (see Sec. III-C1 and Sec. III-C4). At the end of each multiplication in PolySub adder is also used to implement subtraction and coefficient amplifiers, and in-memory adders and bit shifters, which are described below.

1) Controller: The controller activates appropriate clock signals so the customized sense amplifier and in-memory adder circuits can perform operations at the correct times. In addition to operation sequencing, the controller receives flag inputs from the customized sense amplifiers that allow for the conditional execution of steps in a reduction of integer $X$ modulo $q = 2^i$ operation and the PolyScale primitive (see Sec. [III-C1] and Sec. III-C4).  

2) Customized sense amplifiers/in-memory adders: The customized sense amplifiers and in-memory adders employed in this work perform bitwise logic and word-wise addition between two ciphertexts stored in memory. The in-memory adder is also used to implement subtraction and coefficient multiplication in PolySub and PolyMult primitives. We employ circuits similar to those in [12], [24], i.e., an in-memory carry select adder and a customized sense amplifier that enables bitwise logic between two memory words. We also introduce a new operation, “horizontal OR”, in which the bitwise AND result is ORed horizontally, i.e., within all the bits of a word. The “horizontal OR” operation is used to generate modulo reduction and rounding flags for the execution of the PolyScale primitive (see Sec. III-C1] and Sec. III-C4). At the end of each computation, we keep the output (computation result) stored in a temporary latch, so it can be copied/moved to an address in memory in the subsequent cycle.

3) Bit shifters: The bit shifters implemented in CiM-HE can perform right bit shifts that enable divisions by powers of two for the PolyScale primitive. We choose to implement a logarithmic (log) shifter in the memory (Fig. 2). Compared to other bit shifters such as a barrel shifter, the log shifter employed in CiM-HE offers flexibility in terms of the number of shifts possible to achieve in a single round of computation with less area overhead. For instance, a log shifter with $L$ levels can perform $2^L$ combinations of right/left shift in a single round of bit shifting, and multiple rounds can be used to achieve any desired number of right/left bit shifts. It is possible to arbitrarily choose the number of bit shifts each level performs to favor either larger or smaller shifts in one cycle. For instance, Fig. 2 depicts the log shifter in our CiM-HE. We have a 5-level log shifter; each level enables 1, 4, 16, 32, or 64 bit shifts, which can be combined in a single cycle to achieve greater numbers of shifts, e.g., “64+32+16+4+1=117”, or “64+4+1=69”. It is possible to activate only certain levels of the log shifter and keep others deactivated, i.e., performing a shift by 0. The shift mask $S_1$, a 15-bit number, is used to activate left/right or no shifts in every level $L$ of the log shifter. Note that, when setting a mask, we must make sure that one (and only one) transistor is selected per level.

4) In-place copy buffers/In-place move buffers: In-place copy buffers (IPCBs) based on [12] are used to copy CiM outputs (i.e., the results of a bitwise logic, addition, or right/left shift) to an address defined in the memory scratch space. IPCBs are always placed in alignment with each sense amplifier column in the memory array. As such, they do not allow data movement between column $i$ and $i + F$ ($F$ is a pre-defined offset). As CiM-HE needs both (i) a copy of outputs to same column in the array, and (ii) data movement between distinct columns for the execution of polynomial operations, we introduce in-place move buffers (IPMBs) in our architecture. While IPMBs have a similar schematic as IPCBs, we use a different routing scheme in IPMBs that allows us to move data from column $i$ to column $i + F$ in an array, where $F$ is a pre-defined column offset. Note that by performing this operation in $c$ cycles, it is possible to move data with $cF$ different offsets.

The described architecture is used to implement steps that allow for the execution of polynomial primitives in support of HE operations in the B/FV scheme. The mapping between our CiM-HE hardware and such polynomial primitives is detailed in Sec. [III-C].

C. Mapping operations in SHE to CiM hardware

We now describe how CiM-HE components can be used to execute polynomial primitives that are used to support the computational requirements of the B/FV scheme. Each primitive is broken down into a sequence of CiM-friendly steps that require one or more cycles to be executed. Note that we reduce integers $X$ modulo $q$ (as described below) after the execution of every polynomial primitive, to ensure that our results are in the ring $\mathbb{Z}_q$.

1) Reduction of integer $X$ modulo $q = 2^k$: Because all coefficients of polynomials are closed in $\mathbb{Z}_q$, the first operation we need to support is the integer reduction modulo $q$. Computing the reduction of integer $X$ modulo $q = 2^k$ (i.e. $[x]_q \in [−\frac{q}{2}, \frac{q}{2}]$) after the execution of polynomial primitives. Integer reduction modulo $q = 2^k$ in CiM-HE is facilitated by the fact that the $k$th bit — and all other bits to the left — represent the integer part when performing division by $q$. As such, these bits can be ignored if we are only interested in the modulo. While simple, the aforementioned method only returns moduli in the interval $[0, q-1]$. To find the modulo in the correct interval, i.e. $[x]_q \in [−\frac{q}{2}, \frac{q}{2}]$, additional CiM steps are required. We compare half of $q$ (the bit in the $(k−1)^{th}$ position) to the value of our current modulo via a three-step process.

- **Step 1:** We store a mask with all ‘0’s and a single ‘1’ in the $(k−1)^{th}$ position in a scratch space of the CiM memory. We perform a bitwise in-memory AND between
this mask and the residues from $[0, q - 1]$, which results in a $k$-bit number (an intermediate result).

- **Step 2**: At the customized sense amplifier, we perform a horizontal OR between the $k$ bits of the intermediate result. The horizontal OR operation generates a flag value, either ‘0’ or ‘1’, which is used by the CiM controller to indicate the next operation.

- **Step 3**: If the flag is ‘0’, the current modulo is a positive number in the interval $[0, \frac{q}{2}]$, which satisfies our desired form for modulo reduction. If the flag is ‘1’, a PolySub operation between the current modulo and $q$ has to be performed, so a modulo in the interval $[-\frac{q}{2}, 0)$ can be found ($q$ is stored in the scratch space of the CiM memory).

2) Homomorphic Addition via PolyAdd: Homomorphic addition (Sec. II-A) requires polynomial additions, i.e., PolyAdd. As long as coefficients of the same order of two (or more) polynomials are placed in the memory in a column-aligned fashion, this can be directly realized by the in-memory adder described in Sec. III-B.

3) Homomorphic Subtraction via PolySub: The homomorphic subtraction (Sec. II-A) requires polynomial subtractions, i.e., PolySub. This can also be realized by the in-memory adder described in Sec. III-B but requires an extra step before the addition itself, which consists of finding the 2’s complement of the subtrahend. The PolySub primitive can be performed as a two-step procedure.

- **Step 1**: Performing a NOT operation on the subtrahend with our customized sense amplifier, and copying the result to the scratchpad space in the memory array.

- **Step 2**: Adding the minuend with inverted subtrahend, while setting the carry-in bit of the in-memory adder to ‘1’. (This is equivalent to performing the subtraction via 2’s complement arithmetic.)

4) PolyScale for Homomorphic Multiplication: The homomorphic multiplication (Sec. II-A) involves rounded scaling. Therefore, before introducing HomMult, we describe how our CiM-HE architecture supports scaling. Our CiM-HE can perform rounded scaling by powers of two. Given a polynomial $c$ and a divisor in the form $D = 2^{k'}$, we perform rounded scaling by performing a division by $2^{k'}$ for every coefficient, which returns the integer quotient for every coefficient. Divisions by powers of two in memory can be implemented with our CiM log-shifter circuit (described in Sec. III-B).

The log shifter in CiM-HE has 5 levels that allows us to have either 0, or a pre-defined number of right shifts in each level. The pre-defined shifts in each level are 64, 32, 16, 4, and 1. Therefore, for a division by $D = 2^{127}$, we break down the division into three right-shift rounds:

- **Round 1**: $64 + 32 + 16 + 4 + 1 = 117$;
- **Round 2**: $0 + 0 + 0 + 4 + 1 = 5$;
- **Round 3**: $0 + 0 + 0 + 4 + 1 = 5$.

After each right-shift division round, the result is stored in the memory though IPCBs (Fig. 1(c)). To determine which CiM log-shifter levels must be activated in the next round, we perform a subtraction between $k'$ and the value of activated levels (pre-determined values that can be stored in the scratch space of the CiM array). If the result of this subtraction is negative (which can be verified by looking at its signal bit), we know that the number of bit-shifts is beyond what is needed by the division. Hence, we make the highest active level equal to 0 for the next right-shift round and continue the process iteratively until we reach a number of accumulative right-shifts equal to $k'$.

After performing the division with right-shifts, we need to round the value of $z$ to the nearest integer (round up/down). This can be done by a two-step procedure as follows:

- **Step 1**: We compare the bits to the right of $k'$ in the dividend, (i.e., the remainder) to half of the divisor. We use a bit mask with all ‘0’s and a single ‘1’ in the $(k' - 1)^{th}$ position. We perform an in-memory AND followed by horizontal OR operations to generate a rounding flag (similar to the reduction of integer $X \mod q$). Otherwise, $z$ should be rounded down (the bit shifts perform this type of rounding by default).

- **Step 2**: If the result of the AND-OR flag is ‘1’, rounding up is performed by adding ‘1’ to the quotient $z$. Otherwise, $z$ should be rounded down (the bit shifts perform this type of rounding by default).

5) Homomorphic Multiplication via all polynomial primitives: Homomorphic multiplication (Sec. II-A) involves multiple polynomial primitives. For example, to calculate $c_y$, one needs to perform two multiplications of two polynomials (PolyMult), add the two resulting polynomials (PolyAdd), and then perform rounded scaling for the resulting polynomial (PolyScale) to round the polynomial after scaling it by $t/q$.

Implementing PolyMult in the memory using the naive “schoolbook” multiplication method would require $O(n^2)$ multiplications between each pair of coefficients, which could trigger impractically high data movement between CiM arrays. Thus, we employ the Karatsuba multiplication algorithm [47], and execute it with our CiM design. The Karatsuba algorithm recursively breaks a multiplication of two polynomials into multiplications of polynomials with half the number of terms. Compared to a “schoolbook” method, the data movement between arrays — and thus the complexity of implementation — is significantly lower with Karatsuba multiplication. The steps for the Karatsuba multiplication with CiM are described in Algorithm 1.

The CiM implementation of the Karatsuba algorithm is executed recursively. The base case consists of a multiplication between two coefficients (in our case, $k$-bit numbers), i.e., a product that can be computed by Shift-Add operations (Algorithm 2). To perform these operations in memory, we initially (i) reserve a memory address to store the accumulation of partial products (out), (ii) copy the value of multiplicand to the scratch space in memory (so we can shift it in each iteration), and (iii) store the value of the multiplier in a temporary register in the controller ($b'$). We access the bits of $b'$ in the $k$ subsequent cycles in order to determine whether we shift $a'$, i.e. the copy of the multiplicand, 1 bit to the left, or if we add the contents of out to $a'$.

The mapping of Karatsuba multiplication operations for execution in memory are described with a toy example in Fig. 3. In our example, we want to multiply $A = 11_{10}$ and $B = 0_{10}$ ($A = 1011_{2}$ and $B = 0110_{2}$). In the first step of the algorithm, we first move the high part of both operands
Algorithm 1 Karatsuba algorithm [47], [48]

Input: Polynomials $A, B$ of degree $n$ and $k$-bit coefficients

Output: $A \times B$

KARATSUBA($A, B$)

1: if $n == 1$ then
2: return SHIFT-ADD($A, B$)
3: $HighA, LowA := \text{SPLIT}(A, [n/2])$; \hspace{1cm} $\triangleright$ IPMBs
4: $HighB, LowB := \text{SPLIT}(B, [n/2])$; \hspace{1cm} $\triangleright$ IPMBs
5: $R1 := \text{KARATSUBA}(HighA + LowA, HighB + LowB)$; \hspace{1cm} (Figs. 3(e))
6: $R2 := \text{KARATSUBA}(HighA, HighB)$;
7: $R3 := \text{KARATSUBA}(LowA, LowB)$;
8: $R1 := R1 - R2 - R3$;
9: return $R2 \times 2^{2nk} + R1 \times 2^{nk} + R3$ \hspace{1cm} $\triangleright$ shifts/additions

Algorithm 2 Shift-Add algorithm

Input: Multiplicand $a$ and multiplier $b$, which are $k$-bit coefficients

Output: $\text{out} = a \times b$

SHIFT-ADD($a, b$)

1: $\text{out} := 0$; \hspace{1cm} $\triangleright$ reserve in memory
2: $a' := a$; \hspace{1cm} $\triangleright$ copy to memory
3: $b' := b$; \hspace{1cm} $\triangleright$ copy to controller
4: for $i = 1 : k$ do
5: if $b'(i) == 0$ then
6: $a' := \text{SHIFT}(a')$; \hspace{1cm} $\triangleright$ 1-bit left shift
7: if $b'(i) == 1$ then
8: $\text{out} := \text{ADD}(\text{out}, a')$;

\end{algorithm}

(\textit{High}_A = 102$ and \textit{High}_B = 012$) so that they are aligned to ($\textit{Low}_A = 112$ and \textit{Low}_B = 102$), i.e., the high and low parts of the coefficients would map to the same columns, respectively. This step is illustrated in Fig. 3(a). We use IPMBs (described in Sec. III-B4) to move data from column $i$ to column $i + F$ in an array.

The second step consists of computing the additions $\text{Low}_A + \text{High}_A = 112 + 102 = 11112$ and $\text{Low}_B + \text{High}_B = 102 + 012 = 10112$ (Fig. 3(b)) with an in-memory adder (described in Sec. III-B). The results of the additions, i.e., $\text{Low}_A + \text{High}_A = 10112$ and $\text{Low}_B + \text{High}_B = 0112$, are copied to scratchpad addresses in memory with IPCBs (represented in Fig. 1(c)).

Next, we compute the product $R1 = \text{Low}_A + \text{High}_B = 10112$ and $\text{Low}_B + \text{High}_B = 0112$ using the Shift-Add operation (Fig. 3(c)). The product $R1 = 11112$ is copied to the scratchpad space in memory with IPCBs. Similarly, we compute the other two products $R2 = 102$ and $R3 = 01102$ — between low (and high) parts of $A$ and $B$ — using the same procedure as for computing $R1$ (Fig. 3(d)).

The fifth and sixth steps of the in-memory Karatsuba multiplication (in Figs. 3(e) and 3(f)) are for computing the subtraction $R1 - R2 - R3 = 01112$. The subtraction is performed in two parts: first, we compute the two-term subtraction $R1 - R3 = 10012$ using the in-memory subtraction as described in Sec. III-C3. We use IPMBs to move the result of this subtraction so that it is aligned with product $R2 = 102$ (Fig. 3(e)). Next, we perform another subtraction of two-terms, i.e. between $R1 - R3 = 10012$ and $R2 = 102$. The result of the subtraction $R1 - R2 - R3$, which we rename as $R1$, is copied to memory with IPCBs (Fig. 3(f)).

After we compute the subtraction, we shift: (i) $R1 = 01112$ by $nk$ bits, and (ii) $R2 = 102$ by $2nk$ bits using the log shifter (Fig. 3(g)). In this example, $k = 2$ and $n = 1$, i.e., the smaller product to be computed by the algorithm has 2-bit terms (base case). The results of the shifts are copied to scratchpad addresses in memory with IPCBs. Next, we perform an addition between $R1 \times 2^{nk} = 111002$ and $R2 \times 2^{2nk} = 1000002$, and move the result (111102) so that it is aligned to $R3 = 01102$. The steps described are illustrated in Fig. 3(h). Last, we perform the final addition $(R2 \times 2^{2nk} + R2 \times 2^{nk} + R3 = 01000102)$ (Fig. 3(i)). This result is equivalent to the product $A \times B$.

The dominant part of the execution time for this procedure is the multiplications between coefficients, i.e., the computation of products $R1$, $R2$ and $R3$. The other operations are additions, subtractions and copies (movement of data either within the same or different columns in memory). Due to the parallelism in CiM, we can compute the products $R2$ and $R3$ in parallel. In this scenario, the complexity of the Karatsuba algorithm can be reduced from $O(n \log^2 n)$ to $O(n \log n)$ [48].

Finally, note that the support of polynomial primitives that form the basis the execution of HomAdd, HomSub, and HomMult operations enables CiM-HE to perform all computations required by HE.

IV. Evaluation

We evaluate our CiM-HE architecture and compare the runtime and energy consumption of the three operations (HomAdd, HomSub and HomMult in Sec. III) with a CPU-based HE implementation based on SEAL [26]. Furthermore, we evaluate three end-to-end tasks (arithmetic mean, variance, and linear regression) performed with both CiM-HE and the CPU. Finally, we compare the runtime and energy of HomMult (the most expensive HE operation) with a state-of-the-art FPGA-based accelerator [5].

A. Experimental setup

The operations in the B/FV scheme are computed over a polynomial ring $R_q$. We take $q$ to be a 218-bit number, (i.e. $\lceil \log_2 q \rceil = 218$) and the degree of ciphertext polynomials to be $n = 2^{13} = 8192$. We choose these parameters to match the 128-bit security, one of the default settings of Microsoft’s SEAL [26], which exceeds the minimum security requirement of NIST [49] which is 112 bits. The security afforded by these parameters can be shown to be 128 bits with the estimator [50]. Consequently, each ciphertext contains two polynomials of degree 8192 with 218-bit coefficients, and the ciphertext size is 436 KB. Furthermore, the multiplicative depth of the supported functions is $L = 5$, which can be shown by the following inequality [3]:

$$L < \frac{\log(\frac{n}{2}) + \log(q) - \log(q) + 1.25}{\log(\delta_R) + \log(\delta_R) + 1.25 + \log(t)}$$

In our setting, the bound of the error distribution $B$ is 1, the expansion factor $\delta_R$ is $n$, and the plaintext modulus $t$ is $2^{10}$. 


allow for RNS decomposition of ciphertext coefficients. Thus using $2^k$ as a modulus would slow down computation on non-CiM systems. SEAL thus automatically chooses $q$ to be a 218-bit that is a product of 5 coprime numbers of 43 or 44 bits. SEAL uses several algorithmic optimizations for HE, including coefficient-wise RNS decomposition as in [51], and the Number-Theoretic Transform (NTT) for fast polynomial multiplication (concisely described in [53]). In our CiM-HE system, we have not implemented any of these optimizations. Thus, our basis for comparison for CiM-HE is the best case for the CPU. Despite the differences in the choice of the parameter $q$, (CiM-HE uses moduli in the form $2^k$, and SEAL uses a product of coprimes), the security level of both implementations is the same at 128 bits.

The configuration of our test machine is listed in Table I. To account for runtime, we use the C++ std::chrono library. We use the Powerstat tool [54] to measure the power of the CPU while running the HE primitives. To offset the power consumption of system tasks not related to HE, we measure the idle power for the same amount of time as the execution of HE primitives and subtract it from the total power consumption. Finally, we calculate energy consumption as the product between HE net power and operation runtime.

2) CiM-HE. The time and energy of HE primitives implemented in CiM-HE is evaluated based on simulations of the architecture described in Sec. III. The modulus $q$ is set as a power of two, i.e. $q = 2^{218}$, which is CiM-friendly. Memory arrays and peripherals are simulated in HSPICE [55] using the 14nm BSIM-CMG FinFET model [25] (the same technology node as the CPU). The CiM controller and decoders are synthesized in Verilog with the Open Cell Library [56] at the same FinFET technology node. In circuit-level simulations, we measure the time and energy of executing each CiM step required by the polynomial operations (as described in Sec. III-C). Then, we determine the complete sequence of steps needed for each polynomial primitive. Based on this sequence, we compute the time and energy of all the polynomial primitives, which will ultimately be used to obtain the time and energy of each HE operation running on CiM-HE.

Our CiM architecture is implemented at the L3 cache level, which consists of 1 bank with 8192 arrays of size $8 \times 1024$ 6T-SRAM cells. Each array holds up to 32 coefficients of 218 bits, which can fit in 4 standard-sized words of 64 bits. 0.25 KB per array are reserved as scratch space to store intermediate results of CiM-HE operations. The total size of a CiM-HE bank is 4MB. To minimize the number of cycles needed for each CiM-HE primitive, we assume that coefficients of the same degree (of different ciphertexts) are stored in a column-aligned fashion (see Fig. 1(b) in Sec. III-B for more details). With the column-aligned placement scheme described in Sec. III-B as well as the 8192 arrays in our CiM architecture,

![Diagram](image-url)

Fig. 3: Mapping the Karatsuba multiplication for execution in memory. A toy example for multiplication of $A = 1110$ and $B = 610$ ($A = 1011_2$ and $B = 0110_2$) is presented. Blue arrows (and shades) indicate the storage of intermediate computation results by IPCBs and IPMBs. Different colors, i.e., purple/red, green, orange and pink, are used to represent additions, coefficient-wise multiplications, subtractions and shifts, respectively. The flow of the algorithm execution is presented in eight parts. (a) Alignment of high and low parts of coefficients $A$ and $B$. (b) Computation of additions $Low_A + High_A$ and $Low_B + High_B$. (c) Computation of product $R1$. (d) Computation of products $R2$ and $R3$, which are performed in parallel. (e) Subtracting $R3$ from $R1$. (f) Subtracting $R2$ from $R1 - R3$. (g) Left-Shifting $R1 = R1 - R2 - R3$ by $nk$ and $R2$ by $2nk$. (h) Adding up the shifts results. (i) Computation of final addition $R2 \times 2^{2nk} + R1 \times 2^nk + R3$. 

### Table I: Specifications of CPU-based HE

| CPU Model: Intel(R) Core(TM) i5-5300U CPU @ 2.30GHz |
|----------------------------------------------------|
| L1 cache: 32 KB (L1i), 32KB (L1d) |
| L2 cache: 256 KB |
| L3 cache: 3 MB |
| RAM: 8 GB DDR3 |

1) CPU-based HE: To evaluate HE primitives on a CPU, we run HomAdd, HomSub, and HomMult using the Microsoft SEAL library [26]. CPU-based HE performs best when the modulus $q$ is a product of distinct coprime numbers, as this allows residue number system (RNS) decomposition of coefficients as in [51] or [52]. Because $2^k$ cannot be factored as a product of coprimes, using $2^k$ as a modulus does not
TABLE II: Time and Energy of Single Execution of HE Operations

| Primitive | CPU | CiM | Imp. | Energy (J) |
|-----------|-----|-----|------|------------|
| HomAdd   | 8.2E-5 | 7.9E-9 | 10426.5x | 3.6E-6 | 296.9x |
| HomSub   | 8.7E-5 | 8.9E-9 | 9790.6x | 1.4E-3 | 8.7E-5 |
| HomMult  | 3.0E-2 | 6.6E-3 | 4.6x | 3.7E-1 | 7.0E-4 |

we are able to perform 2 simultaneous PolyAdd operations, i.e., 16384 coefficient-wise additions in parallel for our HE parameter settings.

B. Single Execution of HE Operations

We evaluate the single execution of HE operations (HomAdd, HomSub and HomMult) on CiM-HE using the polynomial primitives described in Sec. [III]. In Table II we summarize the energy and runtime of these operations for CiM-HE and CPU-based implementations. We observe high speedups (up to 10426.5x) for operations that require only the execution of polynomial primitives between coefficients of the same degree, i.e. HomAdd and HomSub, as these operations can all be executed in parallel by CiM-HE components described in Sec. [III-B].

A smaller speedup is observed for HomMult, since this operation requires many steps to execute the required number of polynomial multiplications (PolyMult) just as with the CPU. Note that the runtime of PolyMult is proportional to both \(\log(q)\) and \(n\), and this polynomial primitive requires (i) multiplication between coefficients of the same degree (implemented with Add-Shift operations), and (ii) multiplications, additions and subtractions between coefficients of different \(n\) degrees. While CiM-HE is able to perform many coefficient-wise operations in parallel because of the inherently high internal bandwidth of the memory, the PolyMult algorithm implemented on CiM relies on Karatsuba multiplication and does not employ more advanced optimizations such as NTT or RNS.

CiM-HE enables energy savings of 296.9x for HomAdd and 532.8x for HomMult. Besides in-memory additions, multiplications involve numerous shifts and copies, which consumes much less energy than additions when performed in memory. As such, shifts and copies lower the average power of HomMult in comparison to HomAdd. The high energy savings for multiplication with CiM-HE reflects its lower average power.

CiM-HE can support various parameter settings for the B/FV encryption scheme, which in turn results in different security levels and multiplicative depths. Table III show the time and energy improvements for a single execution of HomAdd, HomSub, and HomMult when compared to a CPU-based implementation with same parameters. The improvements are in the same order of magnitude as reported in Table II for all four settings investigated (A through D).

C. Area evaluation

We estimate the area of one CiM-HE array of \(8 \times 1024\) size based on the modular layout of a \(8 \times 16\) tile, as depicted in Fig. [4]. We use Cadence Virtuoso with FreePDK15 design kit [57] to construct the layout. Furthermore, we estimate the area of the sequencing circuit from the synthesized Verilog netlist with Cadence Encounter. The area of row decoders is not included in our evaluation, as they are standard elements in a memory and not exclusive to CiM-HE. Based on the modular design, the area of 1 CiM-HE array corresponds to \(64 \times\) the area of one \(8 \times 16\) tile. When the sequencing circuits (and their respective routing overhead) are included, the resulting area is 33,804.2 \(\mu\text{m}^2\).

Fig. 4: Area evaluation of a CiM-HE array.

We compare the area overhead of CiM-HE to a naive approach of placing multiplier units near the SRAM array. As reported in [58], a single \(32 \times 32\) Booth-Wallace multiplier constructed in the 14nm FinFET technology node occupies an area of 2621.4 \(\mu\text{m}^2\). For the multiplication of coefficients with up to 256 bits using \(32 \times 32\) multipliers, we need either (i) to serialize the operation, or (ii) construct a larger multiplier of size 256\(\times\)256. Assuming the second approach, we roughly estimate the area of such multiplier as \(8 \times 2621.4\mu\text{m}^2 = 21,131.2\mu\text{m}^2\). To process the same amount of integer multiplications as CiM-HE in one shot, i.e., two multiplication of \(n\) coefficients, assuming the parameter setting as in Sec. [IV-B] we would need 2\(\times\)8192 multipliers that occupy a total area of 346.2mm\(^2\) (a 78% increase in area overhead when compared to CiM-HE).
D. Multiple Executions of HE Operations

Here, we consider multiple executions of HE operations for different numbers of CiM-HE banks and different sizes of a CPU’s L3 cache to evaluate the impact of data transfers on the runtime and energy efficiency of HE. Our evaluation is divided into two scenarios as described below:

- **Scenario 1**: We consider a single CiM-HE bank of size 4MB, and further assume a CPU’s L3 cache of 4MB. We operate on $N$ ciphertexts. Only 6 (8) ciphertexts are present in CiM-HE (CPU’s L3 cache) initially. The rest $N – 6 \ (N – 8)$ ciphertexts must be fetched from DRAM.

- **Scenario 2**: We consider two CiM-HE banks of size 4MB (a total size of 8MB), and further assume a CPU’s L3 cache of 8MB. We operate on $N$ ciphertexts. Only 12 (16) ciphertexts are present in CiM-HE (CPU’s L3 cache) initially. The rest $N – 12 \ (N – 16)$ ciphertexts must be fetched from DRAM.

These two different scenarios are evaluated with an increasing number of HE operations on ciphertexts, i.e., $2^0 - 2^9$. CiM-HE speedup (and energy savings) for Scenarios 1 and 2 are depicted in Fig. 5(a) (and Fig. 5(b)). The CiM-HE-based L3 cache is filled with 6 ciphertexts on which we initially operate (i.e., the cache is at its full capacity, considering that scratch space is needed to store intermediate results from the execution of HE algorithms). Likewise, the CPU’s L3 cache of 4MB (iso-capacity) stores 8 ciphertexts as no scratch space is needed. We define the speedup as

$$\frac{T_{CPU} + MT_{CPU}}{T_{CiM} + MT_{CiM}}$$

where $T_{CPU}$ (and $T_{CiM}$) refers to execution time on CPU (CiM) and $MT_{CPU}$ (and $MT_{CiM}$) refers to the time required to transfer data from DRAM to the L3 cache/CiM.

With a single CiM-HE bank of 4MB and equivalent size of CPU’s L3 cache (Scenario 1), the maximum speedups (and energy savings) depicted in Fig. 5(a) (Fig. 5(b)) are 12308.2x (301.1X), and 11449.9X (368.4X) for ADD, 11449.9X (368.4X) for SUB, and 4.6x (532.8x) for MULT, respectively. When the number of operations is larger than 6 for CiM-HE (and 8 for CPU), more ciphertexts need to be fetched from DRAM to replace the ciphertexts already present in the cache. For instance, when we perform 8 operations, CiM needs to fetch 2 ciphertexts from main memory, while the CPU’s L3 cache already contains all the ciphertexts needed for computation. The difference in the number of ciphertexts present in the two L3 caches causes the CiM-HE speedup to drop below 1 for all operations (except MULT) when the number of operations is equal to 8. For a larger number of operations, the speedup of $HomAdd$ and $HomSub$ stays close to 1, because $MT_{CPU} \gg T_{CPU}$, and $MT_{CiM} \gg T_{CiM}$ for these primitives. $HomMult$ can sustain its speedups at the same level because its computation time is more significant than the time spent on data transfers, i.e., for

$$\frac{T_{CPU} + MT_{CPU}}{T_{CiM} + MT_{CiM}}$$

$$\frac{T_{CPU} + MT_{CPU}}{T_{CiM} + MT_{CiM}}$$

$$\frac{T_{CPU} + MT_{CPU}}{T_{CiM} + MT_{CiM}}$$

$$\frac{T_{CPU} + MT_{CPU}}{T_{CiM} + MT_{CiM}}$$

$HomMult$, $T_{CPU} \gg MT_{CPU}$ and $T_{CPU} \gg MT_{CPU}$. Unlike speedup, the energy savings of CiM-HE for all operations (depicted in Fig. 5(b)) do not suffer a significant drop when there are data transfers from DRAM to cache. This is because the energy spent on data transfers is much smaller than the energy spent on HE computations.

With an 8MB L3 cache (Scenario 2), the CPU stores 16 ciphertexts (twice as many as in Scenario 1), while CiM-HE stores 12 ciphertexts (6 in each CiM-HE bank of 4MB). Therefore, the CPU has an advantage of 4 more ciphertexts that are cached before the need for fetching from DRAM. By using 2 CiM-HE banks, two HE operations can be performed in parallel (a similar scenario as in [5]), which leads to further improvements with CiM-HE when compared to the CPU (dash lines in Fig. 5(a)). Namely, we achieved maximum speedups (and energy savings) of 26386.7x (301.1X), 24461.1x (368.3X) and 9.1x (532.8x) for ADD, SUB and MULT, respectively.

As in Scenario 1, in Scenario 2 we observe a drop in speedup (but not in energy savings) when we start fetching data from DRAM, as the runtime is dominated by data
TABLE IV: Evaluation of Mean, Variance, and Latency tasks over (a) 6 and (b) 60 ciphertexts for Scenario 1. Number of dimensions for Latency is 4.

| Task | Mean (µ) | Variance (σ²) | Latency (µs) |
|------|----------|---------------|-------------|
| CPU  | 1.5E+1   | 5.2E-4        | 532.4       |
| CM   | 1.2E+1   | 6.8E-4        | 532.3       |
| Multi | 5.3E-1   | 7.5E-3        | 532.0       |

TABLE V: Inference evaluation for Scenario 2. Number of dimensions for Latency is 4.

| Task | Mean (µ) | Variance (σ²) | Latency (µs) |
|------|----------|---------------|-------------|
| CPU  | 1.5E+1   | 5.2E-4        | 532.4       |
| CM   | 1.2E+1   | 6.8E-4        | 532.3       |
| Multi | 5.3E-1   | 7.5E-3        | 532.0       |

Fig. 6: (a) Structure of the 3-layer MLP neural network. (b) Original activation function and polynomial approximations with degree 2, 3, and 5 are found. The clients perform the polynomial division by n. The result is then decrypted and divided by the client.

TABLE VI: Inference evaluation for Scenario 2. Number of dimensions for Latency is 4.

| Task | Mean (µ) | Variance (σ²) | Latency (µs) |
|------|----------|---------------|-------------|
| CPU  | 1.5E+1   | 5.2E-4        | 532.4       |
| CM   | 1.2E+1   | 6.8E-4        | 532.3       |
| Multi | 5.3E-1   | 7.5E-3        | 532.0       |
network achieves 93.1% accuracy at inference. The fact that the B/FV SHE scheme operates on polynomials with integer coefficients require the weights and the activation function to be adjusted for inference on encrypted data. The adjustments are listed below. Note that after we perform these adjustments, the 3-layer MLP neural network can perform inference on encrypted MNIST data set without the need for bootstrapping.

- **Adjustment 1:** A scaling factor $F_{w}$ was applied to the weights post training to ensure that their values are integers;
- **Adjustment 2:** A scaling factor $F_{a}$ was applied to the activation function, which becomes: $Y = F_{a} \times (1/(1 + e^{-x}))$. The scaled sigmoid function is approximated by polynomial functions (Fig 6(b)). The coefficients of the polynomials must be rounded to the nearest integer. The linear function $y = 1x + 900$ is found to be a possible solution to the approximation, and it is used in our evaluation. The function yields 84% testing accuracy versus 77% when using another option available, i.e., $y = 2x + 899$.

5) **Result Discussion:** The results of our evaluation for the $Mean$, $Variance$, and $LinReg$ tasks are presented in Tables IV and V. Two different situations are considered regarding file sizes, which represent the number of ciphertexts (inputs) to be processed in each one of these tasks. Namely, we evaluate $Mean$, $Variance$, and $LinReg$ tasks with CiM-HE and CPU considering:

- A file size of 6 ciphertexts (Table IV(a) for Scenario 1 and Table V(a) for Scenario 2)
- A file size of 60 ciphertexts (Table IV(b) for Scenario 1 and Table V(b) for Scenario 2)

The Inference task has a fixed input size, i.e., an image with 28 x 28 pixels, therefore we present the results of our evaluation for this task in a separate table (Table VI). When encrypted, the input corresponds to 784 ciphertexts that encode 1 handwritten digit. Note that the 4MB and 8MB caches are not large enough to hold all the ciphertexts at inference time, so data transfers occur for the two different CiM size scenarios during inference.

Computing the $Mean$, $Variance$, and $LinReg$ with a file size of 6 ciphertexts requires no data fetches in either Scenario 1 or Scenario 2, as all ciphertexts are present in the L3 caches per Sec. [IV-D]. More than five orders of magnitude speedup ($>11,000x$ with Scenario 1 and $>26,000x$ with Scenario 2) are observed for the $Mean$ task as only $HomAdd$ operations are executed. The execution time of $HomMult$ dominates others in variance and linear regression tasks, i.e., the speedup with Scenario 1 for $Variance$ and $LinReg$ is 4.6x, which is analogous to the speedup of $HomMult$ alone.

On the other hand, executing $Mean$, $Variance$, and $LinReg$ for a file size of 60 ciphertexts causes the improvement for the $Mean$ task to drop to 1.1X in either scenario as the time to fetch ciphertexts dominates computational time. As expected, for other tasks where multiplication operations dominate runtime, we observed a minimum speedup of 4.4x and 4.1x for $Variance$ and $LinReg$ with Scenario 1.

The runtime of the Inference task is also dominated by multiplications, which explains the 4.2x (7.5x) runtime improvements of CiM-HE when compared to CPU for cache sizes of 4MB (8MB). While doubling the memory size does not change the runtime of the CPU-based solution, it allows for more parallel computations to happen in two distinct CiM banks (similar to the two co-processors solution in [5]).

Energy improvements reach two orders of magnitude for all the tasks evaluated, i.e., we obtain a minimum of >290x energy savings for $Mean$ and maximum of >500x energy savings for $LinReg$ and Inference. CiM-HE consumes more energy in $Mean$ than in other tasks. Calculating a sum homomorphically with $HomAdd$ requires only additions between coefficients of the same degree, which can be performed with the fast in-memory carry select adders in our CiM-HE architecture. Other tasks, e.g., $Variance$, $LinReg$, and $Inference$ are dominated by multiplications ($HomMult$). As shown in Sec. [IV-B], $HomAdd$ has higher power consumption than $HomMult$, hence the lower energy improvement for tasks that involve more additions.

**F. Comparison with Related Works**

Here, we compare the performance and energy efficiency of $HomMult$ running on CiM-HE with previous works that propose HE implementations [5, 27]. As highlighted in [5], homomorphic multiplications are the primary bottleneck of HE due to their extremely long runtime. As such, a comparison for this primitive alone is sufficient to assess the benefits of our proposed CiM-HE when compared to existing work. Reference [27] is a CPU implementation based on the NFLlib [62] that employs the B/FV scheme. Reference [5] proposes an accelerator that employs up to 2 FPGA-based co-processors for HE, and implements NTT and RNS for homomorphic multiplications that are also based on the B/FV scheme.

An important challenge of making a fair comparison between CiM-HE and other works is that each HE implementation uses a different set of parameters, which can significantly impact security, multiplicative depth and runtime of HE operations. For this reason, the parameters $log q$ and $n$, as well as the use of NTT and RNS optimizations in [5, 27] and this work are listed in Table VII. The security level resulted from these parameters is only 80 bits, which has not been considered to be acceptable by NIST since 2015 [49]. Nevertheless, we use a similar parameter setting in our design so as to make a fair comparison between CiM-HE and the existing work [5, 27].

Table VIII presents the homomorphic multiplication time and energy for [5, 27] and CiM-HE. Roy, et al. employ their faster configuration with 2 FPGA-based co-processors. Bos, et al. run their HE implementation on an Intel Core i5-3427 CPU at 1.8 GHz. Per [63], latest generation Intel i5 reaches up to 40W on heavy load operations, which we assume when comparing energy consumption of [27] with our proposed CiM-HE. The same assumption was made by [5].
TABLE VII: Parameters* used in HE Implementations

| HE implementation | log q | n | Optimizations |
|-------------------|------|---|---------------|
| Bos, et al. [27]  | 186  | 4096 | Yes           |
| Roy, et al. [5]   | 180  | 4096 | Yes           |
| CiM-HE (this work)| 180  | 4096 | No            |

*Note: These parameter settings enable a security level of 80-bit and a multiplicative depth of 4.

TABLE VIII: Runtime and energy of HomMult running on different HE platforms

| Figure of Merit (HomMult) | Bos, et al. [27] | Imp. | Roy, et al. [5] | Imp. | CiM-HE |
|---------------------------|------------------|------|----------------|------|--------|
| Runtime                    | 35 ms            | 14.3x| 5 ms           | 2.2x | 2.3 ms |
| Energy                     | 1.3 J            | 2632.4x | 43.5 mJ | 88.1x | 494.0 µJ |

Execution of a homomorphic multiplication takes 5.0 ms and 33.0 ms in [5] and [27], respectively. CiM-HE performs the same operation in 2.3 ms, which represents a speedup of 14.3x with energy savings of >2600x when compared to [27]. The use of 2 FPGA-based co-processors (1 CiM-HE bank that processes two HE operations in parallel) allows for a throughput of 400 (861) multiplications per second in [5] (CiM-HE). Furthermore, CiM-HE enables 88.1x more energy savings, with same the security level and multiplicative depth.

The energy efficiency of CiM-HE is due to two main factors: (i) CiM-HE does not use algorithmic optimizations like NTT or RNS, (ii) computation is performed in memory. The impact of these factors is explained below. For (i), the PolyMult primitive that relies on additions and shifts (Karatsuba) requires simpler hardware when compared to the hardware required for NTT in [5]. The latter requires the design of large multiplier units and special modules for performing polynomial lift and scaling (which are not used/needed in our design). The modulo reduction circuitry is also more complicated than the bit shifters in CiM-HE, which employs moduli q that are powers of 2. For (ii), CiM avoids large amounts of data transfers to processing units while performing HE operations. CiM-HE takes advantage of data placement (as described in Sec. III) to perform Boolean logic at the bitline level with the use of customized sense amplifiers. Boolean operations can be leveraged to implement more complex functions, e.g. arithmetic additions, with a lower area overhead when compared to implementing arithmetic logic units (ALUs) from scratch [12], [24].

Note that if one were to decide not to leverage optimizations such as NTT and RNS in a design that performs conventional data-processing, i.e., not in-memory, we expect item (ii) above to significantly influence the associated speedups/energy savings when compared to CiM-HE implementations. This is because it is not easy to design processing units that can match the processing power of CiM, which performs logic at the sense amplifier level and takes advantage from inherently high internal bandwidth of the memory [11].

V. CONCLUSION AND FUTURE WORK

We propose a CiM architecture that realizes essential operations for the B/FV scheme, a well-known SHE scheme. Our CiM-HE architecture consists of customized CMOS peripherals such as sense amplifiers, adders, bit-shifters, and sequencing circuits. The peripherals and memory cells are based on a 14nm FinFET technology. Circuit-level evaluation of the CiM-HE design indicates maximum (minimum) speedups of 9.1x (4.6x) and maximum (minimum) energy savings of 266.4x (532.8x) for homomorphic multiplications (the most expensive HE operation). Furthermore, we evaluate arithmetic mean, variance, linear regression, and inference tasks using CiM-HE. The speedups (and energy savings) are associated with the dominant HE operation required by each task. Furthermore, our results support the idea that using multiple CiM banks can improve CiM-HE speedups by allowing them to operate on different ciphertexts in parallel, taking advantage of internal memory bandwidth. However, a more efficient multi-bank approach for CiM-HE may require larger memory sizes. Therefore, we plan to study the use of CiM-HE in the main memory as an alternative to the cache by employing denser memory cells based on CMOS (DRAM) or emerging technologies. We also plan to integrate algorithmic optimization techniques into our design to further increase the speedup of CiM-HE.

REFERENCES

[1] C. Gentry, “Fully homomorphic encryption using ideal lattices,” in Proceedings of the 41st Annual ACM Symposium on Theory of Computing, ser. STOC ’09. New York, NY, USA: ACM, 2009, pp. 169–178. [Online]. Available: http://doi.acm.org/10.1145/1536414.1536440
[2] L. Ducas and D. Micciancio, “FHEW: bootstrapping homomorphic encryption in less than a second,” in Eurocrypt. Springer, 2015, pp. 617–640.
[3] J. Fan and F. Vercauteren, “Somewhat practical fully homomorphic encryption,” IACR Cryptology ePrint Archive, 2012.
[4] J. W. Bos, K. Lauter, J. Loftus, and M. Naehrig, “Improved security for a ring-based fully homomorphic encryption scheme,” in BIA International Conference on Cryptography and Coding. Springer, 2013, pp. 45–64.
[5] S. Sinha Roy, F. Tiran, K. Jarvinen, F. Vercauteren, and I. Verbauwhede, “Fpga-based high-performance parallel architecture for homomorphic computing on encrypted data,” in HPCA, Feb 2019, pp. 387–398.
[6] S. Jeloka, N. B. Akesh, D. Sylvester, and D. Blaauw, “A 28 nm configurable memory (tcam/hcam/sram) using push-rule 6t bit cell enabling logic-in-memory,” IEEE Journal of Solid-State Circuits, vol. 51, pp. 1009–1021, April 2016.
[7] J. T. Pawlowski, “Hybrid memory cube (hmc),” in IEEE HCS. IEEE, 2011, pp. 1–24.
[8] J. Ahn, S. Hong, S. Yoo, O. Mutlu, and K. Choi, “A scalable processing-in-memory accelerator for parallel graph processing,” in ISCA, June 2015, pp. 105–117.
[9] J. Ahn, S. Yoo, O. Mutlu, and K. Choi, “Pim-enabled instruction: A low-overhead, locality-aware processing-in-memory architecture,” in ISCA, June 2015, pp. 336–348.
[10] A. O. Glova, I. Akgun, S. Li, X. Hu, and Y. Xie, “Near-data acceleration of privacy-preserving biomarker search with 3d-stacked memory,” in DATE, March 2019, pp. 800–805.
[11] S. Jain, A. Ranjan, K. Roy, and A. Raghunathan, “Computing in Memory With Spin-Transfer Torque Magnetic RAM,” TVLSI, vol. PP, pp. 1–14, 2017.
[12] S. Aga, S. Jeloka, A. Subramaniyan, S. Narayanasamy, D. Blaauw, and R. Das, “Compute caches,” in HPCA, Feb 2017, pp. 481–492.
[13] M. Imani, S. Gupta, Y. Kim, and T. Rosing, “Floatpim: In-memory acceleration of deep neural network training with high precision,” in ISCA. New York, NY, USA: ACM, 2019, pp. 802–815.
[14] P. Chi, S. Li, C. Xu, T. Zhang, J. Zhao, Y. Liu, Y. Wang, and Y. Xie, “PRIME: A Novel Processing-in-Memory Architecture for Neural Network Computation in ReRAM-Based Main Memory,” in ISCA, June 2016, pp. 27–39.
[15] N. Tala, S. Gupta, P. Mane, and S. Kvatinsky, “Logic design within memristive memories using memristor-aided logic (magic),” TNANO, vol. 15, pp. 635–650, 2016.
