Cooling of electronic components on the LTCC module with an embedded flat heat pipe

D A Nesterov†, V A Derevyanko†, S B Suntsov‡

1 Institute of Computational Modelling of the Siberian Branch of the Russian Academy of Sciences, 660036, Krasnoyarsk, Russia,
2 Joint Stock Company "Academician M.F. Reshetnev "Information Satellite Systems", Zheleznogorsk, Krasnoyarsk Region, Russia

Abstract. The results of the experimental investigations of a ceramic circuit board test sample with an embedded flat heat pipe are presented. The sample was made based on the technology of low temperature co-fired ceramic (LTCC). The flat heat pipe is formed at the bottom side of a ceramic substrate using a capillary structure made of sintered copper powder. The developed prototype of the LTCC module was used for the investigation of removing and spreading of high heat fluxes from high power electronic components mounted on the module. The embedded flat heat pipe filled with acetone provides 40 W/cm² of heat flux removal from the heat source with the heat dissipation area of 1 cm². The measured value of the thermal resistance between the heat source and cooler surface under the module is 0.8 °C/W.

1. Introduction

The Low Temperature Co-fired Ceramic (LTCC) technology is widely used for manufacturing electronic modules due to excellent high-frequency dielectric properties and the possibility of three-dimensional integration of passive electronic components inside one multilayer substrate [1, 2]. The thermal conductivity of LTCC is not high (2-3 W/m·K), therefore cooling of the high-power miniature components mounted on the LTCC module is a relevant problem especially under vacuum conditions. One of the solutions is the integration of a flat heat pipe directly into the LTCC module [3, 4, 5]. The flat heat pipe allows effectively spreading heat from miniature high-power heat sources, which significantly reduces the density of heat fluxes and facilitates further heat removal from the module [6].

This paper presents the results of the experimental investigation of a ceramic circuit board test sample with an embedded flat heat pipe. The sample is designed for investigating the possibilities to increase the power of electronic components based on the LTCC modules. The developed prototype of the LTCC module includes a flat heat pipe, which is intended for removing and spreading the concentrated heat load from the high-power electronic components mounted on the module. The spreading of the high heat flux over the entire area of the flat heat pipe allows further removing the heat from the bottom side of the module with a lower heat flux and consequently, with a smaller temperature drop.

* corresponding author: ndanda@icm.krasn.ru
2. Description of the problem
The development of the LTCC-module sample was based on the following main requirements:

- The module contains miniature electronic components with the dissipated heat flux $q_s \approx 20 \text{ W/cm}^2$;
- The heat must be removed from the bottom surface of the module, which is mounted on a heat-removing base with a thermal grease or adhesive having a low thermal conductivity value;
- The heat-removing base under the module has the limit for the maximum heat flux value of about $\leq 3 \text{ W/cm}^2$;
- The module with high-power components should be a self-contained unit which can easily be installed or replaced in electronic equipment.

The high-power heat sources in the module are active electronic components that are installed on the top surface of the ceramic board. At the considered input heat fluxes of $q_s = 20 \text{ W/cm}^2$, the heat transfer to the bottom surface of LTCC with the thickness of $d \approx 1-2 \text{ mm}$ leads to the temperature drop $\Delta T \sim 100 ^\circ \text{C}$. The well-known solution to increase the effective thermal conductivity of LTCC in the transversal direction is thermal vias embedded into the LTCC layers under the heat sources [7]. The thermal vias allow reducing the temperature drop across the ceramic layers by 4-6 times, but the problem of further high heat flux removal from the bottom surface of the LTCC module remains. At the considered high heat flux, the temperature drop on the thermal contact between the module and the heat-removing base, on which the module is installed, is up to tens of degrees. Moreover, the cooling system under the module may not be able to remove such high heat fluxes.

The solution of the problem requires reducing the high heat flux. Flat heat pipes (vapor spreaders) are efficient thermal devices that can reduce the local input heat flux by spreading it to a large area with a very small temperature gradient. The use of the flat heat pipe in the LTCC-module can spread the heat flux from the miniature high-power component with the area of $\approx 1 \text{ cm}^2$ to the entire module area of 25 cm$^2$. This will reduce the heat flux by an order of magnitude. Since the module must be a self-contained unit which can easily be installed or replaced in electronic equipment, the flat heat pipe must be embedded into the module. The transfer of the high heat flux from the heat sources to the flat heat pipe (to the vapor in the heat pipe) should be maximum effective.

3. Design of the sample
The sample is designed for investigating the possibilities to increase the power of electronic components based on the LTCC modules. The developed prototype of the module consists of a LTCC substrate of 50 x 50 mm, which is combined constructively with a flat heat pipe (figure 1).

![Figure 1. LTCC-module with the flat heat pipe.](image1)

![Figure 2. Internal structure of the test sample.](image2)
The capillary structure of the flat heat pipe is made of copper sintered powder. It consists of two porous layers of 0.25 mm each (figure 2). Between the layers there is an array of 11 × 11 (121 in total) cylindrical porous columns arranged with the step of 4 mm. The columns have a height of 1 mm and diameter of 2 mm. The space between the porous layers forms a vapor core. The capillary structure is attached to the lower metalized surface of the LTCC substrate and it is covered by a bottom cover, which has a hermetically sealed contact with the LTCC substrate along the perimeter. The bottom cover is made of kovar (nickel-cobalt ferrous alloy), which is compatible with the thermal expansion characteristics of LTCC. The bottom cover and the LTCC substrate form the case of the flat heat pipe.

The flat heat pipe was filled with 0.95 g of acetone (1.2 cm³ at 20 °C). The optimum amount of the working fluid was determined experimentally and it exceeded the estimated total pore volume of the capillary structure of 0.8 cm³. Acetone was used due to the need to operate the heat pipe at low temperatures (down to minus 40 °C). Methanol can also be considered as a promising working fluid, especially for higher operating temperatures of the heat pipe. Additionally, it can be noted that water is not suitable for the heat pipe design used. An attempt was made to use water, but the temperature difference along the heat pipe was too high. Apparently, kovar is incompatible with water. Thus, only the results for acetone are presented here.

4. Heat transfer in the sample
The heat transfer scheme is shown in figure 3. The module is mounted on a heat-removing base (cooler) with the temperature $T_c$. The high heat flux $q_s$ from the heat source (transistor) on the module is transferred through solder layers, ceramic layers and a porous wick to the evaporation zone of the working fluid in the flat heat pipe. The vapor spreads over the entire area of the heat pipe and condenses on the lower layer of the wick. Then, the low heat flux $q_c$ is transferred through the wick layer, bottom cover of kovar and thermal grease to the cooler.

![Figure 3. Heat transfer in the sample.](image)

The temperature drop between the terminal of the transistor $T_B$ and the cooler $T_C$ can be expressed as a sum of three terms:

$$
\Delta T_{B:C} = \Delta T_{B:V} + \Delta T_V + \Delta T_{V:C},
$$

where $\Delta T_{B:V}$ is the temperature drop between the terminal of the transistor and the vapor in the heat pipe, $\Delta T_V$ is the temperature drop along the moving vapor in the flat heat pipe, $\Delta T_{V:C}$ is the temperature drop between the vapor and the surface of the cooler.
The temperature drop $\Delta T_{b,v}$ occurs at the high heat flux $q_v$. Table 1 shows the thickness, the estimated value of the thermal conductivity and the resulting specific thermal resistances (per unit area) of the corresponding layers of the materials. The total value of the specific thermal resistance is equal to $r_{b,v} \approx (6-10) \cdot 10^{-3}$ K·m$^2$/W. With the heat flux of $q_v = 20$ W/cm$^2$, the temperature drop can be estimated as $\Delta T_{b,v} = q_v r_{b,v} \approx 12-19$ °C.

The estimation shows that the main contribution to the temperature drop $\Delta T_{b,v}$ is made by the ceramic layers under the heat source. The total thickness of these layers cannot be reduced due to technological difficulties.

The wetted wick layer in the heat pipe also makes a significant contribution to the thermal resistance. Table 1 presents a rough estimation. The transfer of the input heat flux through the wetted wick to the evaporation zone at the liquid-vapor interface is a complex process, which is determined by the geometry and properties of the porous structure, thermal properties of the working fluid and value of the heat flux. In addition, the thermal resistance of the wetted wick may decrease with increasing the input heat flux. This may occur gradually with the recession of the liquid [8] or abruptly due to a transition from the evaporation to the boiling regime [9]. When the heat load exceeds a certain critical value, the wick begins to dry out, a hot spot appears and the temperature drop on the wick increases rapidly. The critical value of the heat load depends on limitations for the heat pipe operation (capillary limit, boiling limit).

| Material layer       | $d$ (mm) | $\lambda$ (W·m$^{-1}$·K$^{-1}$) | $r$ ($10^6$×K·m$^2$·W$^{-1}$) |
|----------------------|----------|--------------------------------|--------------------------------|
| Solder               | $2 \times 0.1$ | 50                             | 4                              |
| LTCC with thermal vias | 0.6      | 15-20                          | 30-40                          |
| LTCC                 | 0.05     | 2-4                            | 12-25                          |
| Wick                 | 0.25     | 10-20                          | 12-25                          |
| **Total**            |          |                                | **≈ 60-100**                   |

The temperature drop $\Delta T_{v,c}$ occurs at the low heat flux $q_c$. The estimation of the specific thermal resistance of the material layers is given in table 2. The estimated total value is equal to $r_{v,c} \approx (1.5-1.6) \cdot 10^4$ K·m$^2$/W. For the heat flux $q_c = 1$ W/cm$^2$, the temperature drop has a low value $\Delta T_{v,c} = q_c r_{v,c} \approx 1-2$ °C.

The temperature drop $\Delta T_v$ is determined by the thermal properties of the working fluid used, design of the vapor channels and configuration of the heat input/sink areas. For acetone as a working fluid, the temperature drop is low, $\Delta T_v < 1$ °C.

In addition, it should be noted that the temperature drop in the heat pipe depends on the quality of the heat pipe filling and it can increase in the presence of non-condensable gases or in the case of an excessive amount of the working fluid.

| Material layer       | $d$ (mm) | $\lambda$ (W·m$^{-1}$·K$^{-1}$) | $r$ ($10^6$×K·m$^2$·W$^{-1}$) |
|----------------------|----------|--------------------------------|--------------------------------|
| Wick                 | 0.25     | 10-20                          | 12-25                          |
| Solder               | 0.1      | 50                             | 2                              |
| Kovar                | 0.5      | 20                             | 25                             |
| Thermal grease       | 0.2      | 1.8                            | 110                            |
| **Total**            |          |                                | **≈ 150-170**                   |
As a result of the estimation, it can be concluded that the total thermal resistance between the high-power heat source ($S \approx 1 \text{ cm}^2$) on the module and the cooler ($S \approx 25 \text{ cm}^2$) will be within $R_{S-C} = 0.6-1.1 \degree C/W$.

During the experiments, the temperature of the top of the transistor case $T_s$ is measured (see figure 3). Inside the transistors used, a heat-dissipating semiconductor substrate is mounted on the drain terminal attached to the bottom of the case. The drain terminal is a heat sink for the hot semiconductor substrate. The hot substrate has almost no thermal contact with the ceramic case of the transistor. Therefore, the temperature of the top of the case $T_s$ is close to the terminal temperature $T_B$.

5. Results of the experiments

The experimental investigations of the ceramic circuit board test sample with the embedded heat pipe were conducted under different conditions. The objectives of the investigations were as follows:

1) evaluation of the flat heat pipe operation efficiency for the spreading of the high heat flux from the small-size heat source over the entire area of the sample; 2) measurement of the maximum power of the heat source, at which the wick in the heat pipe begins to dry out; 3) measurement of the thermal resistances between the heat source and the cooler.

For the experiments, the sample of the LTCC module was installed horizontally on the cooled surface, which was a metal plate with channels for a liquid coolant. The coolant was pumped through the channels. The temperature of the coolant was controlled by means of a thermostat. The measurements were carried out for two variants of heat removal. For the first variant, only a half of the bottom surface of the sample was pressed against the cooled surface (figure 4a). In this case, the heaters used were located on the edge opposite to the cooling area (transistors 1 and 2). Such a configuration makes it possible to estimate the efficiency of the heat pipe by the distribution of the heat flux over the entire area of the sample. For the second variant, the sample was installed by the entire bottom surface of the sample on the cooler (figure 4b). The second configuration allows determining the values of thermal resistances under the best heat removal conditions. For brevity, both of the heat removal configurations are further referred to as “half area cooling” and “entire area cooling”.

![Diagram](image)

Figure 4. Variants of the heat removal configurations from the sample in the experiments: a) heat removal from the half bottom surface of the sample (half area cooling); b) heat removal from the entire bottom surface of the sample (entire area cooling).

Two series of experiments were carried out. The first series of experiments was carried out using an infrared camera. Thermal images allow estimating the performance of the flat heat pipe for the heat flux spreading from the transistors over the entire area of the sample. The experiments were performed under atmospheric conditions at the cooler temperature of 20 ℃.
The second series of experiments was carried out in vacuum. The purpose of the experiments was to investigate the influence of the cooler temperature on the efficiency of the heat pipe operation and on the values of the thermal resistances. The experiments in vacuum allow one to exclude the heat exchange with the ambient air, and also to conduct studies at temperatures below zero. During the tests in vacuum, the infrared camera was not used, with the temperatures being measured by thermocouples (T-type).

During the experiments for a given cooler temperature, the power of one or two heat sources was increased stepwise. For each power value after reaching a stationary state, the temperatures of the transistors $T_{S1}-T_{S3}$ (on the top of case) and the surface temperature of the cooler $T_c$ were measured. When using the infrared camera, the temperature of the transistor was determined as the maximum value for the region of the transistor case on the thermal image. In the experiments without the infrared camera (in vacuum), thermocouples were placed on the transistor cases at the hottest points determined by the thermal images obtained previously.

To analyze the measurement results, the temperature $T_{v}$ was also used, which was calculated as the average temperature of the non-used transistors (without heat dissipation). The value of $T_{v}$ was considered as the value of the vapor temperature in the heat pipe. The following is an estimate of the deviation of the measured non-used transistor temperature from the vapor temperature. This deviation is determined by the heat leakage $Q_{td}$ from the non-used transistor to the environment and thermal resistance $R_t$ between the temperature measuring point and vapor: $\Delta T_{Tv} = Q_{td}/R_t$.

The value of $R_t \leq 5 \, ^{\circ}C/W$ was estimated from the internal structure of the transistor and thermal resistance of the layers under the transistor (table 1). The value of $Q_{td}$ depends on the experimental conditions. For atmospheric experiments (using the infrared camera), the $Q_{td}$ value is determined by the convective heat exchange with the ambient air and radiation between the transistor and the environment. For the transistor with the temperature of 40 °C and the ambient air with the temperature of 20 °C, the $Q_{td}$ value does not exceed 0.05 W. For the experiments in vacuum, the thermocouples were pressed to the transistor using a heat-insulating material.

The assessment of the possible heat leakage $Q_{td}$ through the clamping structure gives a range from minus 0.15 W (heat flow to the transistor at minus 40 °C) to 0.05 W (at +40 °C). Thus, the deviation $\Delta T_{Tv}$ ranges from minus 0.3 °C to +0.8 °C, depending on the temperature of the non-used transistor. In addition, it can be noted that in the experiments the measured temperatures of the non-used transistors were close to each other within 1-2 °C (except for the experiments at $T_c = -40 \, ^{\circ}C$ when the temperature difference reached up to 3.5 °C).

Based on the results of the temperature measurements, the following thermal resistances were calculated: the total thermal resistance between the heat-dissipating transistor and the cooler $R_{S-C} = (T_S - T_c) / Q_S$, thermal resistances between the transistor and the vapor $R_{S-V} = (T_S - T_v) / Q_S$ and between the vapor and the cooler $R_{V-C} = (T_v - T_c) / Q_S$. The power $Q_S$ was calculated from the electric current and voltage drop between the drain and the source terminal of the transistor.

5.1. Results of the experiments in atmosphere using infrared camera

Figure 5 presents the measured dependences of the thermal resistances vs. power of a single transistor (transistor 1 in figure 4). The blue and red lines correspond to various configurations of the heat removal from the module: entire area cooling and half area cooling, respectively (labeled "entire" and "half").

At the heat loads below 15-20 W, the measured thermal resistances decrease with the increasing power. The causes for this decrease can be the following: 1) the peculiarities of the heat pipe operation; and 2) the influence of the parasitic inflow heat to the module from the environment during the experiment. With the further increase in the power, the thermal resistances remain almost constant until the heat load exceeds a certain critical value, after which the thermal resistance between the transistor and the cooler $R_{S-C}$ begins to grow. The growth of the thermal resistance is connected with the wick dryout in the heat pipe. At half area cooling (red lines in figure 5), the wick dryout begins at the power $Q_{dry} = 35-40$ W. At entire area cooling (blue lines in figure 5), the power of the wick dryout
exceeds the value of $Q_{dry} > 40$ W (at $Q = 45$ W, there is a slight increase in the thermal resistance value).

The optimum (minimum) value of the total thermal resistance $R_{S-C}$ is about 0.60-0.65 °C/W and 0.70-0.75 °C/W for the entire and for the half area cooling configurations, respectively. The difference is due to different areas of the heat sink from the module and therefore, different thermal resistance $R_{V-C}$ between the vapor in the heat pipe and the cooler. The value of $R_{V-C}$ is 0.1 °C/W and 0.2 °C/W for the entire and for the half area cooling configurations, respectively.

Figure 6 presents an infrared image of the module at the single transistor heat dissipation of 30 W at the cooler temperature $T_c = +20$ °C. The half area cooling configuration is used. The maximum temperature on the transistor case is 41 °C. The temperature of the module surface (beyond the heated transistor) is almost isothermal within 25-26 °C. This means that the heat flow from the heat source is transferred to the vapor in the heat pipe and effectively spreads to the entire area of the module.

Figure 7 shows the measured values of the thermal resistances vs. power upon simultaneously heating two transistors. The indices "1" and "2" in the notations in figure 7 correspond to transistors 1 and 2, respectively, as is shown in figure 4. The powers of both transistors in the experiment are set to be the same, $Q_1 = Q_2$. The values of $R_{S1-C}$, $R_{S2-V}$, $R_{S1-C}$ and $R_{S2-V}$ are calculated from the power value of the corresponding transistor $Q_1$ or $Q_2$; the value of $R_{V-C}$ is calculated from the total value of the power $Q_1 + Q_2$.

At entire area cooling (blue lines in figure 7), the values of the thermal resistances $R_{S1-C}$ and $R_{S2-C}$ are close to each other. At the power higher than 15 W per transistor, the thermal resistances are approximately the same and equal to 0.7-0.8 °C/W.

At the power of $Q = 45$ W per transistor (total 90 W), the thermal resistance for the second transistor $R_{S2-C}$ (solid square marks in figure 7) begins to grow. At half area cooling (red lines in figure 7), the thermal resistances for both transistors $R_{S1-C}$ and $R_{S2-C}$ are almost the same below the power of $Q \approx 25$ W (per each). With the further power growth, the value of $R_{S2-C}$ begins to increase rapidly. The value of $R_{S1-C}$ also begins to increase, but at a higher power, about 30 W. This is due to the fact that the heat dissipation area of transistor 2 (drain of the transistor) is farther from the heat removal area (see, figure 4a).

Figures 8 and 9 present the infrared images of the module for two simultaneously heated transistors at the half area cooling configuration. The infrared image at the transistor power of 20 W per each (total 40 W) is shown in figure 8. The temperatures of the transistor cases do not exceed 38 °C. The thermal resistances between the transistors and the condenser are equal to 0.9 °C/W. The surface temperature of the board, including the unheated transistors (number 3 and 4), has the uniform
distribution within 27.0-28.5 °C. This means that the flat heat pipe effectively spreads the heat flux to the entire area of the module. The thermal resistance between the vapor in the heat pipe and the condenser \( R_{V-C} \) is equal to 0.2 °C/W.

Figure 7. Thermal resistances vs. power at the heat dissipation of two transistors

Figure 9 presents the infrared images for the case of the wick dryout in the heat pipe at the high heat dissipation of 45 W per transistor (total 90 W). Hot areas can be seen around the heated transistors especially near transistor 2. This overheating occurs as a result of the wick dryout in the flat heat pipe. The temperatures of the transistors reach \( T_{S1} = 75 \) °C and \( T_{S2} = 89 \) °C. The temperature of the adiabatic section of the flat heat pipe (the vapor temperature) is in the range of approximately \( T_V \approx 39-44 \) °C, which corresponds to the thermal resistance \( R_{V-C} \approx 0.2-0.3 \) °C/W. In addition, it can be noted that the area with the lower temperature is observed near the filling tube. The liquid is displaced from the zone of the wick dryout. Therefore, the excessive amount of the liquid accumulates in the condensation area of the heat pipe and blocks a part of its area near the filling tube.

Figure 8. Infrared image of the LTCC module with the heat dissipation power of two transistors 20 W per each.

Figure 9. Infrared image of the LTCC module with the heat dissipation power of two transistors 45 W per each.
The experiments conducted in the atmosphere using the infrared imager show that the heat pipe efficiently spreads the heat flow from the transistors with the heat dissipation area of 1 cm² to the entire module area of 25 cm². This makes it possible to reduce the heat flux density and to simplify further heat removal from the module. The board outside the heated transistors has a uniform temperature close to the temperature of the heat-removing base. The heat load, at which the wick dryout begins, exceeds \( Q_{dry} > 40 \) W for the single heated transistor. With the two heated transistors the value of \( Q_{dry} \) is about 40 W per each (total 90 W) at entire area cooling and 25-30 W per each (total 50-60 W) at half area cooling.

5.2. Results of the experiments in vacuum at various cooler temperatures

Figures 10 and 11 present the measured dependences of the thermal resistances vs. heat dissipation power of the single transistor in vacuum at the entire and half area cooling configurations, respectively. The measurements were made for different temperatures of the cooler \( T_C \): -40 °C, -20 °C, 0 °C and +20 °C.

The dependences are typical. At the low heat loads, the total thermal resistance between the transistor and cooler \( R_{S-C} \) decreases with the increasing heat load. After exceeding a certain value of the heat source power, the thermal resistance begins to grow. The increase in the thermal resistance is usually connected with the wick dryout due to reaching one of the limitations of the heat pipe operation.

At entire area cooling (figure 10), the thermal resistance \( R_{S-C} \) begins to grow when the power exceeds the value of approximately \( Q_{dry} \approx 35-45 \) W. Since the growth is slow, the beginning of the wick dryout is difficult to identify. At half area cooling (figure 11), the growth of \( R_{S-C} \) is more rapid. The wick dryout occurs at the power \( Q_{dry} \approx 30 \) W for \( T_C = +20 \) °C. At lower temperatures of the cooler, the value of \( Q_{dry} \) is slightly lower: at \( T_C = -40 \) °C, the \( Q_{dry} \approx 25 \) W.

The values of the thermal resistance \( R_{S-C} \) increase with the decreasing temperature of the cooler. At entire area cooling (figure 10) at \( T_C = +20 \) °C, the value of \( R_{S-C} \) in the power range from 25 to 45 W remains almost constant and has the value of about 0.75 °C/W. At half area cooling (figure 11), at \( T_C = +20 \) °C, the thermal resistance \( R_{S-C} \) has the minimum value of 0.8 °C/W at the power of 25-30 W. When the cooler temperature is decreased to \( T_C = -40 \) °C, the value of \( R_{S-C} \) increases by 30-50%.
The thermal resistance between the vapor in the heat pipe and the cooler $R_{v-c}$ (dashed lines) increases with decreasing the cooler temperature, especially at low heat loads. This is mainly due to the change in the thermal properties of acetone with the decreasing temperature. Reducing the density and pressure of the saturated vapor leads to the increase in the temperature drop along the vapor moving path in the heat pipe.

The experiments conducted in vacuum show that the heat load of the wick dryout beginning at $Q_{dry}$ weakly depends on the cooler temperature and has the values of 35-45 W and 25-30 W at entire and half area cooling, respectively. If it is necessary to operate the module at low temperatures of the cooler, it does not require imposing additional restrictions on the heat source power.

The values of the thermal resistance $R_{v-c}$ increase with the decreasing temperature of the cooler. The causes for this increase are: 1) change in the characteristics of acetone with temperature; 2) possible presence of non-condensable gases in the heat pipe; 3) parasitic heat inflows during the experiment, especially at low operating temperatures and low heat loads. The increase in the total thermal resistance with the decreasing temperature of the cooler does not lead to an increase in the absolute value of the transistor temperature. The temperature of the heated transistor does not rise above 55 °C for the cooler temperatures from −40 °C to +20 °C at powers of 45 W and 30 W for the entire and half area cooling configurations, respectively.

6. Conclusions
A test sample of the LTCC-module with an embedded flat heat pipe is developed and investigated. The sample is a self-contained unit, which includes MOSFET transistors as miniature high heat flux electronic components. The embedded flat heat pipe provides the effective spreading of the high heat flux from the heat sources of 30-40 W power with the heat dissipation area of ≈1 cm$^2$ to the entire bottom surface of the module with the dimensions of 5 × 5 cm$^2$. A significant decrease in the density of the heat flux facilitates the heat removal from the module. The temperature of the ceramic board outside the areas of the high-power heat sources location has an almost uniform distribution and remains close to the temperature of the heat-removing base under the module.

The total thermal resistance between the transistors in the module and the heat-removing base under the module depends on the heat load, area of the heat removal from the module, and temperature of the cooler. At low heat loads the thermal resistance decreases with the increase in the power of the heat source. When the heat load exceeds a certain critical value the thermal resistance begins to increase due to drying out of the wick in the heat pipe.

At the cooler temperature of ±20 °C, at the heat removal from the entire bottom surface of the module, the thermal resistance reaches the minimum value of 0.7-0.8 °C/W at the heat source power of 35-40 W. At the heat removal from the half area of the bottom surface of the module, the minimum thermal resistance of 0.8-0.9 °C/W is observed at the heat source power of 25-30 W.

The total thermal resistance increases with a decrease in the temperature of the cooler. At the cooler temperature minus 40 °C, the thermal resistance increases by 30-50% as compared to the cooler temperature of ±20 °C.

The main contribution (50-70 %) to the temperature drop between the heat sources and the cooler is made by the ceramic layers under the heat sources. Though these layers contain thermal via arrays, their thermal resistance reaches 0.4-0.6 °C/W. The total thickness of these layers could not be reduced due to technological difficulties. This is the drawback of the design, which makes it difficult to transfer heat from the heat sources to the heat pipe. In the future, it is planned to improve the design, allowing one to mount electronic components through holes in the ceramic board directly to the wall of the heat pipe through a separate thin heat-conducting dielectric substrate.

The thermal resistance of the wick layer at the heat input area is the second most important point. Based on the results of the experiments, the value is estimated to be 0.1-0.3 °C/W. In the future, to reduce the total thermal resistance, it is planned to decrease the thickness of the porous layer in the capillary structure at the heat input side.
The thermal resistance between the vapor in the heat pipe and the heat-removing base under the LTCC-module has a low value of 0.1 °C/W (when removing heat from the entire bottom surface of the module). Since the flat heat pipe provides the heat spreading to the entire area and significant decrease in the heat flux, the LTCC-module can be mounted on the heat-removing base with a thermal grease or adhesive having a low thermal conductivity value.

7. References

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