Improved charging phenomenon with a modified barrier structure for flexible displays fabricated on polyimide substrates

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In a previous study, the authors investigated that abnormal $V_{th}$ behaviour could occur due to polyimide charging when a voltage was applied to the gate in thin film transistors fabricated on polyimide substrates. The authors propose a barrier structure that could prevent this charging phenomenon when fabricating flexible thin film transistors on polyimide substrates. The barrier layer was changed to an SiOCH/SiO2 double layer to reduce the influence of fluorine ions generated in PI by negative bias temperature stress. To confirm the effect of the SiOCH layer, Al/PI/SiO2/Al, Al/PI/SiOCH/SiO2/Al metal-insulator-metal capacitors were fabricated and electrical properties were measured. When bias stress was applied, changes in current and capacitance were observed only in the device with a single SiO2 barrier layer. In addition, it was confirmed through secondary ion mass spectrometry measurements that the Si–CH3 bonds in the SiOCH layer were replaced with Si–F bonds by the fluorine ions originating from PI. It was also verified that the abnormal behaviour of $V_{th}$ did not occur after negative bias temperature stress of the thin film transistor fabricated using an SiOCH/SiO2 double layer.

**Introduction:** Flexible displays can be applied to various forms by improving the degrees of freedom of space and shape such as clothing, automobiles, artificial intelligence industries, and combinations thereof [1]. A flexible display requires flexibility to be freely deformable, so a polymer material is used as the substrate. Among the many available polymer materials, polyimide (PI) is mainly used due to its good heat resistance and high thermal conductivity [2,3]. Prior to depositing the driving circuit, a barrier structure for flexible displays fabricated on polyimide substrates is used widely because it has excellent optical transparency and high thermal conductivity [2,3].

**Device Structure:** TFTs of three structures were used. Figure 1 shows the schematic cross-section of the top-gate-staggered amorphous indium-gallium-zinc-oxide (a-IGZO) TFT used in the experiment. The difference between Device A and Device B was that the substrate was glass or PI, respectively, and Device B and Device C possessed different barrier layers such as SiO2 and SiOCH/SiO2, respectively. The total thickness of SiO2 and SiOCH/SiO2 was controlled to 200 nm. The following processes after the barrier layer were the same for all TFTs. SiO2 and SiOCH used as the buffer layer were deposited via plasma enhanced chemical vapour deposition (PECVD). An Mo layer was deposited onto the buffer layer and then patterned via photolithography to form source and drain electrodes. A 50-nm-thick active layer of a-IGZO was formed via DC sputtering at 200 °C. A 50-nm-thick Al2O3 layer as a gate insulator (GI) was deposited via atomic layer deposition (ALD). Contact holes were formed on the GI layer by photolithography and dry etching. The gate electrode was deposited via DC sputtering.

The channel width ($W$) and length ($L$) of the TFTs used in the experiment were 40 μm and 100 μm, respectively. To confirm the charging effect more intuitively, electrical characteristics as $I-V$ and $C-V$ measured with Al/SiO2/PI/AI, Al/SiO2/SiOCH/Al metal-insulator-metal (MIM) capacitors using the barrier layer of the TFT device as an insulator were evaluated under NBTS. Finally, after NBTS, a secondary ion mass spectrometry (SIMS) analysis was carried out to confirm the interface between the barrier and PI.

**Results and Discussion:** Figure 2 shows the $I_{ds}$-$V_{G}$ plot measured over time while applying NBTS. NBTS was performed with $-10$ V applied to the gate at 70 °C; the duration of stress was 4000 s. To increase the reliability of the experimental data, five samples were evaluated for each device. After NBTS, the $V_{th}$ shift of each device can be seen in the box plot in Figure 2(d); the $V_{th}$ shifts of Device A, Device B, and Device C were $-0.48$ V, $0.21$ V, and $-0.47$ V, respectively. The direction of the $V_{th}$ shift was negative for Devices A and C but positive for Device B. In general, when NBTS was applied to a-IGZO TFT, holes became trapped in the PI.
the active channel and GI, resulting in a negative shift of \( V_{th} \) [6]. It was found in a previous study that the cause of the abnormal \( V_{th} \) behaviour in Device B was because \( F^− \) was generated from PI and charging occurred at the interface between PI and the barrier [5]. Although Device C was fabricated onto the PI substrate, the abnormal \( V_{th} \) behaviour did not occur by NBTS.

To verify that the barrier structure proposed here controlled the charging phenomenon by \( F^− \), the \( C-V \) of the MIM capacitor was measured prior to and after NBTS. Figures 3(a) and (b) show the \( C-V \) characteristics for various PI structures under NBTS. Stress voltages of \(-10 \text{ V}, -20 \text{ V}, \text{ and } -30 \text{ V} \) were applied to the upper electrode. As the voltage intensity increased, the capacitance of the Al/SiO2/PI/Al capacitor decreased; however, the Al/SiO2/SiOCH/Al capacitor was negligible. The same evaluation was performed with four samples for each capacitor. Figures 3(c) and (d) show the change in charge density (\( Q \)) of the MIM capacitor according to voltage. The change in charge density was 6.0 (C/cm²) when a single SiO2 layer was used as a barrier; however, a single SiO2 layer was used as a barrier. This implied that the change in charge density represents the generation of substrate bias applied to the a-IGZO TFTs. This indicated that the change in charge density represented the generation of substrate bias in the a-IGZO TFTs.

During the NBTS evaluation, it was estimated that increase in voltage stress caused a positive \( V_{th} \) shift through accumulation of holes in the active bulk layer of a-IGZO due to charging between the PI/barrier rather than hole trapping at the GI/a-IGZO interface in Device B.

Figure 4 shows the 1–V characteristics of the MIM capacitor under NBTS conditions. The current value of the device using SiO2 as a barrier layer increased as the voltage stress increased; however, the change was insignificant for the device using SiOCH/SiO2. It could be estimated that the leakage current increased due to the generation of defects as the bonds of the PI layer were broken. Figure 5 shows the SIMS results before/after NBTS of the capacitor structures shown above. It could be seen in Figure 5(a) that the fluorine ions separated from PI were accumulated at the SiO2 and PI interface after NBTS. It is not known exactly how the polymer chain bond structure is formed in PI, but it can be confirmed indirectly through SIMS results that F bonds are included. These accumulated fluorine ions at the interface could affect the electrical characteristics of TFT structures fabricated on PI substrates. The SiOCH film is a low dielectric and relatively more Si–CH3 bonds with weak strength than SiO2 film [7]. For the device using SiOCH/SiO2, there was no change in fluorine ions even after NBTS as shown in Figure 5(b); instead, SiF increased between PI and SiOCH. This can explain why F (328 KJ/mol) has a higher electron affinity compared to C (122 KJ/mol). Thus, the bond of Si–CH3 is broken due to stress, and the Si–F bond is strengthened by replacing the CH2 group. Furthermore, unbonded carbon can be replaced by non-polar C–C or C–H bonds, thereby preventing the charging effect [8]. As a result, charging effects were effectively prevented by consuming fluorine ions via introducing the SiOCH layer.

**Conclusion:** We proposed a method to improve the charging phenomenon that occurred between the PI substrate and the barrier of flexible TFTs. In such a device fabricated on PI substrates, fluorine ions can be induced from the PI by BTS. A barrier of flexible TFT was proposed as a double layer of SiOCH/SiO2 and it was found that charging was suppressed by consuming fluorine ions generated from PI. This result was expected to play a big role towards improving the reliability of not only the flexible display industry but also PI-based flexible devices.

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