Investigation of Plasma Enhanced Chemical Vapor Deposition Chamber Mismatching by Photoluminescence and Raman Spectroscopy

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Slight differences between supposedly identical process chambers are a well known problem in semiconductor manufacturing. In particular, individual plasma-aided process chambers are difficult to characterize and tune to match each other because plasma is a non-equilibrium state and can leave its “footprint” in subtle ways on a wafer. This process chamber mismatching phenomena was investigated in a dual chamber, commercial, high density plasma chemical vapor deposition system by monitoring SiO2/Si interface quality using multiwavelength room temperature photoluminescence and Raman spectroscopy. Effects on the SiO2/Si interface quality, from altering the gas flow pattern in the plasma process chamber, are also studied. © The Author(s) 2015. Published by ECS. This is an open access article distributed under the terms of the Creative Commons Attribution 4.0 License (CC BY, http://creativecommons.org/licenses/by/4.0/), which permits unrestricted reuse of the work in any medium, provided the original work is properly cited. [DOI: 10.1149/2.01610P314] All rights reserved.

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Multiple processing systems are used for a single task in large scale Si semiconductor device manufacturing facilities. A processing system often consists of more than one process chamber. Sometimes the identical task may even be performed in process chambers from different equipment suppliers. Even if the process chambers are from the same equipment supplier and supposedly identical, we often experience difficulty in matching the process results after a lot of process tuning effort.1–8 Process tuning is typically done by matching physical dimensions and apparent physical properties of processed materials on Si wafers (for example; deposition, etching, bulk and surface treatment, annealing etc.).4–11 In some cases, problematic process chambers cannot be commissioned for device manufacturing, even after process tuning due to unexplained device performance variations of wafers processed in them for undiscovered reasons.2,3,12 It takes several iterations of device fabrication and test cycles to figure this out. It can easily take several months and significant resources.7–9 Process chamber mismatching problems are more prone to processes in which plasma takes an active role.7,10–12 Since plasma itself is a non-equilibrium state, with many variables (such as pressure, gas flow pattern, r. f. frequency, r. f. power, electrode configurations, d. c. bias, impedance, wafer temperature, chamber seasoning, etc.), it is difficult to characterize a plasma state and match the process results perfectly.5,7,10–12 Electrical performance variations of final devices processed in different process chambers generally determines whether a particular process chamber can be commissioned for device manufacturing, or not.2,3,12 If we can detect the potential mismatching problems in a process chamber at an early stage and without going through the lengthy device fabrication and test cycles, it would greatly reduce cost and perhaps shorten the process tuning cycle. For these reasons, gathering large amounts of data, and data mining to extract and analyze useful information, are getting increasingly more important to solve challenging problems which impact yield.1,4,7,12 Unfortunately, the number of published studies in this area is very small because it naturally contains very sensitive information such as trade secrets, technical competence and business competitiveness. Very valuable and critical information is often kept non-contact, optical characterization techniques, to gain insights into subtle differences (hidden variables) which specific diagnostic metrology evaluation of the SiO2 films and/or SiO2/Si interface might reveal. The thicknesses and optical properties of the SiO2 were measured as essentially identical using conventional measurement techniques. Multiwavelength, room temperature photoluminescence (RTPL) and Raman spectroscopy were then used to characterize SiO2/Si interface quality and stress of the Si beneath the SiO2 layers. The SiO2 films were grown under identical control process variables, but, not necessarily identical (chamber) process conditions. Effects of gas flow pattern changes in the qualified HDP-CVD chamber on SiO2 films and SiO2/Si interfaces were also investigated.

Experimental

Thin (6 nm thick) SiO2 films were thermally grown on 300 mm p− Si(100) wafers in a commercial vertical batch furnace. The thickness of Si wafers was 775 μm. The thermal SiO2/Si wafers were used as the optical characterization reference material for the purpose of investigating and characterizing HDP-CVD chamber mismatching using controlled starting materials. Details of the HDP-CVD system can be found in Ref. 13. Plasma SiO2 films with a target thickness of ~580 nm were deposited on top of thermally grown 6 nm-thick SiO2/Si wafers in a commercial available HDP-CVD system using SiH4 and O2 as source gases. The wafer temperature and chamber pressure were maintained at ~350 °C and ~5 mTorr for both (dis-qualified) Chamber A and (qualified) Chamber B process chambers, respectively. Two gas flow patterns (high and low gas flow ratios of chamber center nozzles to chamber edge nozzles) were tested in the qualified process chamber to see the effect of gas flow patterns on the oxide film thickness and oxide quality distribution.

Results and Discussion

Figure 1 shows UV-VIS-NIR reflectance spectra, in the wavelength range of 200 ~ 1100 nm, from a bare Si wafer with native oxide, a thermally grown 6 nm-thick SiO2/Si reference wafer and three ~580 nm-thick HDP-CVD SiO2 films grown on 6 nm-thick SiO2/Si wafers. The 6 nm-thick SiO2/Si wafer showed similar reflectance spectra to the bare Si wafer with a native oxide layer. They showed two distinct peaks at ~280 nm and ~360 nm corresponding to Eg(1) (∼3.4 eV) and Eg(2) (∼4.2 eV), the energy separation characteristic of Si. Due to the ultra thin layers of native oxide (~1 nm) and thermal oxide (~6 nm), there was no interference on the reflectance spectra of the SiO2 films. The wafers with ~580 nm thick HDP-CVD oxide films showed numerous interference fringes corresponding to the thickness and refractive index (RI) of oxide films. From just the oxide thickness and RI
measurements of the HDP-CVD oxide films on Si, the disqualified and qualified chambers were nearly identical. No noticeable differences were observed.

Similarly, from a device performance perspective, the differences between wafers processed in the disqualified process chamber and qualified chamber are not detectable from film thickness and RI measurements of blanket Si wafers processed under the identical process conditions. Other physical characteristics of the SiO2/Si seemed to be responsible for the difference in device performance of wafers processed in the disqualified and qualified process chambers.

To gain further insights into the physical properties of SiO2/Si structures prepared in different process chambers, and with various gas flow patterns in the same process chamber, multiwavelength RTPL and Raman characterizations were performed on the thermally grown 6 nm-thick SiO2/Si reference wafer and three ~580 nm-thick HDP-CVD SiO2 films grown on 6 nm-thick SiO2/Si wafers.

It is well known that RTPL of crystalline Si at wavelengths near band edge of Si (~1.1 µm) is very sensitive to the density of nonradiative bulk and surface defects.14-15 Most RTPL studies on Si measure RTPL intensity centered at ~1 µm using a photodiode, without measuring actual RTPL spectra. No spectral information is available to separate the asymmetric band-to-band transition RTPL peak centered ~1140 nm and a small band tail RTPL peak extended to ~1270 nm, which is sensitive to the Si lattice damage. Multiwavelength spectroscopic RTPL is useful in understanding defects in silicon and electronic property changes (such as band bending) at the dielectrics/Si interface, which would be missed by a single wavelength measurement.

RTPL spectra were measured from the thermal SiO2/Si and HDP-CVD SiO2/Si wafers under two excitation wavelengths (650 and 827 nm). The spectroscopic RTPL system (Wafers’ Masters’ MPL-300 system) is described elsewhere.16-23 Multiwavelength, spectroscopic RTPL mapping was done at 15,101 points in 2 mm intervals in x- and y-directions. The penetration depths for the RTPL excitation wavelengths of 650 and 827 nm were ~4.0 µm and ~10 µm, respectively. The excitation laser beam was focused at the wafer surface with diameter in the range of 50 ~ 100 µm. Since the electronic properties, including electronic carrier lifetime and radiative recombination (photoluminescence: PL) probability, are strongly influenced by the SiO2/Si interface quality, the presence of Si lattice damage (possibly by plasma process induced damage (PPID)) and charges (ions and traps) in SiO2 can significantly impact RTPL spectra/intensity, as well as the electrical properties of SiO2/Si in device wafers. In this study, due to the non-contact nature of the spectroscopic RTPL technique, it is used as a technique for early determination of the potential acceptability of electrical performance of devices, without using physical electrodes.

Micro-Raman wafer mapping of the SiO2/Si wafers was performed under three excitation wavelengths (457.9, 488.0 and 514.5 nm) in the visible wavelength range to investigate Si lattice stress from the SiO2/Si interface in the depth direction. Multiwavelength micro-Raman system (MRS-300) is described elsewhere.16-18,21,23-25 The focused laser beam diameter at the wafer surface was in the range of ~1 µm. The Raman probing depths in Si for 457.9, 488.0 and 514.5 nm laser beam are ~290 nm, ~490 nm and ~645 nm, respectively.23-25 Weighted average stress of Si from the SiO2/Si interface, over the Raman probing depths, can be measured at a given excitation wavelength.23-25 By measuring the Raman signal from Si under different excitation wavelengths, Si lattice stress under the SiO2 and its distribution into bulk Si can be evaluated.

Figure 1 summarizes the SiO2 film thickness, calculated from ellipsometry measurements, using an He-Ne laser (633 nm), RTPL wafer maps and RTPL line scans, results, under 650 and 827 nm excitation, in the Y-direction from the wafer notch. The RTPL spectra line scans in the wavelength range of 900 ~ 1400 nm were plotted in the Y-direction from the wafer notch. Ellipsometry measurements were done for all wafers at 225 points with 10 mm edge exclusion. The average film thickness and uniformity of the reference thermal SiO2/Si wafer were 5.5 nm and 6.3% in 1σ. The average thickness (and uniformity) of three HDP-CVD SiO2 films were calculated to be 582.8 nm (0.96%), 584.6 nm (1.95%) and 588.2 nm (1.37%), in order, from Chamber A (high gas flow ratio at the center), Chamber B-1 (high gas flow ratio at the center) and Chamber B-2 (low gas flow ratio at the center). From a thickness uniformity point of view, HDP-CVD Chamber A (the disqualified chamber) gave better results than the SiO2 deposition conditions (B-1 and B-2) of the qualified chamber.

RTPL intensity of the ~6 nm-thick thermal SiO2/Si reference wafer showed very low counts (~5,000 counts at 650 nm excitation and ~10,000 counts at 827 nm). The RTPL line scans show very uniform intensity/spectra across the wafer, under both excitation wavelengths, indicating homogeneous SiO2/Si interface quality. RTPL spectral distributions were almost identical across the wafer. No noticeable RTPL spectral distribution change, due to the significant localized lattice damage, was observed across the wafer. Since the RTPL spectral distributions are alike at all measurement points, it is safe to simply compare the RTPL intensity between HDP-CVD SiO2/Si wafers measured in this study. All HDP-CVD SiO2/Si wafers showed very intense (5 ~ 8 times stronger) RTPL signals compared to the reference SiO2/Si wafer with ~6 nm thick thermal oxide. However, the RTPL line scans in the Y-direction showed ~30% variation in the RTPL intensity range.

In general, RTPL intensity was higher at the wafer center and lower near the wafer edge. The HDP-CVD SiO2/Si deposited in the disqualified chamber (Chamber A, with high gas flow ratio of chamber center nozzles to chamber edge nozzles) showed ~20% lower RTPL intensity compared to the wafers processed in qualified chamber (Chamber B with high (B-1) and low (B-2) gas flow ratios of chamber center nozzles to chamber edge nozzles). Two RTPL intensity dips, near 45 and ~35 mm, in the Y-direction from the wafer center are due to the end effector marks of the HDP-CVD system from the wafer back side. Electrically active defects generated on the wafer back side by end effector contact are responsible for localized drops in RTPL intensity. Since Chamber A and Chamber B are attached to the same wafer transfer module, the end effector marks appear as mirror images to each other. The mean free path of free carriers in high quality Si can easily exceed 1 mm (larger than the thickness of a Si wafer) and PL signal intensity is very sensitive to band bending at the SiO2/Si interface, residual damage in Si (especially residual damage within the probing depths) and wafer back side interface quality variations, even though the RTPL probing depths are up to ~10 µm from the SiO2/Si interface.

The RTPL intensity Y-line scan trends, for the same high gas flow ratio of chamber center to chamber edge nozzles, for the disqualified chamber (Chamber A) and qualified chambers (Chamber B-1), were very wavelike, other than the RTPL intensity itself. The gas flow ratio is often varied to adjust within wafer distribution of electrical properties of devices without having good understanding of its physical impact. It is considered “a knob” for process tuning. Since most process and material monitoring and/or characterization techniques
Figure 2. Oxide film thickness maps, RTPL intensity maps and RTPL spectra Y-line scan results of blanket Si wafers with native oxide, 6 nm thick low temperature thermal oxide and 6 nm thick thermal oxide + 580 nm thick HDP-CVD oxide deposited using different process chambers and gas flow patterns.

(such as thickness measurement, refractive index measurement and film stress measurements through wafer bow measurements) are not as meaningful or sensitive enough to the electrical properties of devices. In practice, these time consuming trial-and-error approaches are wastefully repeated on device wafers. Good process and material monitoring and/or characterization techniques, which are sensitive enough to the electrical properties of devices processed under the same conditions, have long been desired to save valuable device wafers. The RTPL line scan results of the Chamber B-1 and Chamber B-2 in the Y-direction show the correlation between the change of RTPL intensity patterns and the change of gas flow ratios of chamber center to the chamber edge nozzles. The change of SiO₂ film thickness maps due to changes of the gas flow ratio showed almost no correlation with the change of RTPL intensity maps. The changes in the SiO₂ film thickness map does not, to first order, reflect the changes seen in the RTPL intensity map. This strongly suggests that the way the source gases are supplied to the HDP-CVD process chamber can affect the electrical properties of SiO₂/Si interface and possibly the electrical properties of devices.

Previous RTPL studies on PPID on Si wafers that underwent plasma etching (PE) of an SiO₂ layer and plasma enhanced chemical deposition (PECVD) of SiO₂ showed significant drops in RTPL intensities where PPID is present on the Si wafers. Other RTPL studies also showed significant drops in RTPL intensities in SiO₂/Si with UV exposure during routine optical characterization and ionic charge exposure in air during Corona charge-based, non-contact electrical (I-V and C-V) characterization. All of these left permanent damage to the Si lattice and/or SiO₂/Si integrity which can impact electrical properties. Portions of the damage were recovered after annealing in forming gas (96% N₂ + 4% H₂). Multiwavelength RTPL intensity...
measurements of SiO$_2$/Si wafers showed very promising features as a non-contact optical characterization technique for probing electrical properties of dielectric/Si structures.

The chamber-to-chamber RTP intensity comparisons between the qualified chamber (Chamber B-1) and disqualified chamber (Chamber A) showed $\sim$20\% reduction. The gas flow pattern change within the qualified chamber (Chamber B-1 and B-2) showed how gas flow impacts SiO$_2$ thickness distribution and RTP intensity distribution on Si wafers. The increase of gas flow from the chamber edge nozzles (Chamber B-2) resulted in $\sim$10\% drop in RTP intensity at wafer edge, while the RTP intensity at wafer center stayed the same. The change in RTP intensity distribution on Si wafers (Chamber B-1 and B-2) resembled the change of typical yield patterns on device wafers processed under the same gas flow patterns in the qualified chamber (Chamber B). The RTP intensity, and its intensity ratio, can be used as an indicator and signal for evaluating HDP-CVD process chambers as seen in Figs. 3 and 4.

To investigate possible changes in Si lattice stress under various process conditions, multiwavelength Raman wafer mapping measurements were done at 93 points on all wafers. Figure 5 shows the average Raman shift, full-width-at-half-maximum (FWHM) of Raman peak and Raman peak intensity of all wafers under three excitation wavelengths (457.9, 488.0 and 514.5 nm). The reference Si wafer, with native oxide, showed a Raman peak at 520.3 cm$^{-1}$ under all excitation wavelengths. The Si lattice stress can be calculated from the difference in Raman shift values from the value (520.3 cm$^{-1}$) for a stress free reference Si wafer. A positive shift of 0.1 cm$^{-1}$ is equivalent to compressive stress of $-43.4$ MPa. The calculated Raman shift values equivalent to Si lattice stress of $-30$ MPa, $-40$ MPa and $-50$ MPa are shown in Fig. 5a.

The weighted Si lattice stress of the reference 6 nm-thick thermally grown SiO$_2$/Si wafer, under three excitation wavelengths with probing depths of 290 $\sim$ 645 nm, were in the compressive stress range of $-30.7 \sim -37.5$ MPa. The highest compressive stress was measured under 457.9 nm excitation indicating effect from very near the SiO$_2$/Si interface. The resolution and repeatability of Raman measurements after curve fitting are 0.01 cm$^{-1}$ and 0.05 cm$^{-1}$, respectively. All $\sim 580$ nm-thick HDP-CVD SiO$_2$/Si wafers showed slightly higher compressive stress values. The HDP-CVD SiO$_2$/Si wafer deposited in the disqualified chamber (Chamber A) showed the lowest compressive Si lattice stress compared to the other HDP-CVD SiO$_2$/Si wafers processed in the qualified chamber (Chamber B). It also showed a significant drop in Si lattice stress, as the probing depths of Raman measurements increased from $\sim$290 nm to $\sim$490 nm (from 457.9 nm to 488.0 nm excitation). Relatively steep compressive Si lattice stress drop in the depth direction is present. The two HDP-CVD SiO$_2$/Si wafers deposited in the qualified chamber (Chamber B) showed slightly higher compressive stress of $-51.7 \sim -52.1$ MPa and the gradual release of compressive Si lattice stress in the depth direction, regardless of the alteration of the gas flow ratio of the center nozzles to the edge nozzles. This Si lattice stress value, and its change in the depth direction beneath the HDP-CVD SiO$_2$ layer, seemed to be correlated to the RTP intensity difference in the HDP-CVD SiO$_2$/Si wafers deposited in the different plasma process chambers.

Raman FWHM values are very similar, within measurement errors, for all SiO$_2$/Si wafers, including the 6 nm-thick thermally grown SiO$_2$/Si wafer. The variations of FWHM under different excitation wavelengths were close to the limit of the wavelength (or frequency) coherency of the Ar$^+$ laser of micro-Raman system. Raman intensity of the 6 nm-thick thermally grown SiO$_2$/Si wafer was relatively weak under all excitation wavelengths due to the negligible interference from the 6 nm-thick SiO$_2$ layer (Fig. 1). All the 580 nm-thick HDP-CVD SiO$_2$/Si wafers showed similar Raman intensity trends. The highest Raman intensity was measured at 488.0 nm excitation due...
to the lower reflectance for 580 nm-thick HDPCVD SiO\textsubscript{2}/Si at that wavelength (Fig. 1).

The device issues related to carrier recombination and stress effects are in the Si region. PPID in the Si region and distribution of residual electrical charges in HDP-CVD oxide films can strongly affect carrier recombination rates and band bending at the SiO\textsubscript{2}/Si interface. The area of weak RTPL intensity of the disqualified chamber (Chamber A) generally showed a higher threshold voltage ($V_{th}$) shift than did the surrounding areas and strongly affected device yield. The RTPL intensity maps of HDPCVD SiO\textsubscript{2}/Si, from the disqualified chamber, showed good correlation with device yield-loss maps.

Summary

In summary, process chamber mismatching phenomena was investigated in a dual chamber, commercial, HDP-CVD system by monitoring SiO\textsubscript{2}/Si interface quality using multiwavelength RTPL and Raman spectroscopy. Different HDP-CVD SiO\textsubscript{2}/Si electrical properties, obtained from supposedly identical process chambers, were investigated. Effects on the SiO\textsubscript{2}/Si interface quality, from altering the gas flow pattern in the plasma process chamber, were also studied. Multiwavelength Raman characterization of Si lattice stress beneath the SiO\textsubscript{2} layer, and its change in the depth direction, can provide very valuable insights into the state of the Si, which cannot be accessed from typical routine monitoring of thickness and optical properties of SiO\textsubscript{2} films after deposition. Multiwavelength RTPL measurements also provide the effect of SiO\textsubscript{2} film deposition techniques and conditions on electrical integrity of the SiO\textsubscript{2}/Si structure. New characterization techniques such as multiwavelength RTPL and Raman spectroscopy can provide additional insights into the root cause of the “mysterious” process chamber mismatching problems which causes significant short-falls in semiconductor manufacturing. The use of multiwavelength RTPL and Raman spectroscopy can provide very valuable inputs on process chamber behaviors on processed wafers for process chamber qualification/disqualification and guide process chamber tuning without going through lengthy device fabrication and test cycles. This will greatly shorten the process chamber qualification/disqualification.

References

1. http://www.businesswire.com/news/home/20070207005202/en/ISMI-Reveals-Cost-Saving-Method-Correcting-Process-Variation#VP3faKxFvW1.
2. E. Chang and A. Park, ECS Transactions, 27(1) 205 (2010).
3. T.-H. Pan, S.-S. Jang, and D. S.-H. Wong, IEEE Trans. on Systems, Man, and Cybernetics, Part C: Applications and Reviews, 42(4), 576 (2011).
4. http://www.plasmetrex.com/ag/chambermatching_r.html.
5. R. W. Brounley, High Frequency Electronics, April 2004, 30 (2004).
6. C. Zhang and R. Ordóñez, Extremum-Seeking Control and Applications, Advances in Industrial Control, (Springer-Verlag London, 2012) Chap. 7.
7. L. Kulkarni, S. Kurakula, and H. Armer, http://www.appliedmaterials.com/nanochip/fab-solutions/december-2013/methodology-feature-partnering-with-customers-to-improve-yield.
8. L. Zhang and H. Armer, http://www.appliedmaterials.com/nanochip/fab-solutions/december-2013/methodology-feature-partnering-with-customers-to-improve-yield.
9. N. Hershkowitz and R. A. Reun, Rev. Sci. Instrum., 68(1), 880 (1997).
10. S. K. Baldwin, P. Patrick, and N. Williams, Electrochem. Soc. Proc., 99-30, 55 (1999).
11. A. Iline, B. Bastien, and D. Lootens, https://www.onsemi.com/site/pdf/DiagnosticsforHDP.pdf.
12. US Patent: US 6,170,428 B1 (Jan. 9, 2001).
13. D. H. Baek, S. B. Kim, and D. K. Schroder, J. Appl. Phys., 104, 054503 (2008).
14. M. Tajima, M. Ikebe, Y. Ohshita, and A. Ogura, J. Electron. Mater., 39(6), 747 (2010).
15. S. K. Jang, C. C. Jeng, T. C. Wang, C. M. Huang, Y. L. Wang, and W. S. Yoo, ECS J. of Solid State Sci. and Technol., 2(5) 214 (2013).
16. S. K. Jang, C. C. Jeng, T. C. Wang, C. M. Huang, Y. L. Wang, and W. S. Yoo, J. Mater. Res., 28(9), 1269 (2013).
17. S. K. Jang, C. C. Jeng, T. C. Wang, C. M. Huang, Y. L. Wang, and W. S. Yoo, J. Mater. Res., 28(9), 2012.
18. S. K. Jang, C. C. Jeng, T. C. Wang, C. M. Huang, Y. L. Wang, and W. S. Yoo, J. Mater. Res., 28(9), 1269 (2013).
19. S. K. Jang, C. C. Jeng, T. C. Wang, C. M. Huang, Y. L. Wang, and W. S. Yoo, J. Mater. Res., 28(9), 1269 (2013).
20. J. G. Kim, H. J. Cho, S. K. Park, S. H. Lee, B. G. Choi, J. Y. An, Y. I. Cheon, Y. H. Jeon, T. Ishigaki, K. Kang, and W. S. Yoo, JES Solid State Lett., 3(3), N11 (2014).
21. W. S. Yoo, B. G. Kim, S. W. Jin, T. Ishigaki, and K. Kang, ECS Trans., 61(2) 161 (2014).
22. W. S. Yoo, B. G. Kim, S. W. Jin, T. Ishigaki, and K. Kang, ECS J. Solid State Sci. and Technol., 3(11), N142 (2014).
23. W. S. Yoo, B. G. Kim, S. W. Jin, T. Ishigaki, and K. Kang, ECS Trans., 66(4) 263 (2015).
24. W. S. Yoo, B. G. Kim, S. W. Jin, T. Ishigaki, and K. Kang, ECS J. Solid State Sci. and Technol., 4(7) N76 (2015).
25. W. S. Yoo, B. G. Kim, S. W. Jin, T. Ishigaki, and K. Kang, ECS J. Solid State Sci. and Technol., 4(7) N76 (2015).
26. W. S. Yoo, B. G. Kim, T. Ueda, and T. Ishigaki, Appl. Phys. Exp., 2, 116502 (2009).
27. W. S. Yoo, J. H. Kim, and S. M. Han, J. Micro/Nanolithography, MEMS, and MOEMS, 13(1), 011205 (2014).