Electrical and dielectric parameters in TiO$_2$-NW/Ge-NW heterostructure MOS device synthesized by glancing angle deposition technique

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This paper reports the catalyst-free coaxial TiO$_2$/Ge-nanowire (NW) heterostructure synthesis using the glancing angle deposition (GLAD) technique integrated into an electron beam evaporator. The frequency and voltage dependence of the capacitance–voltage (C–V) and conductance–voltage (G/ω–V) characteristics of an Ag/TiO$_2$-NW/Ge-NW/Si device over a wide range of frequency (10 kHz–5 MHz) and voltage (−5 V to +5 V) at room temperature were investigated. The study established strong dependence on the applied frequency and voltage bias. Both C–V and G/ω–V values showed wide dispersion in depletion region due to interface defect states (D$_{it}$) and series resistance (R$_s$). The C and G/ω value decreases with an increase in applied frequency. The voltage and frequency-dependent D$_{it}$ and R$_s$ were calculated from the Hill-Coleman and Nicollian-Brews methods, respectively. It is observed that the overall D$_{it}$ and R$_s$ for the device decrease with an increase in the frequency at different voltages. The dielectric properties such as dielectric constant ($\epsilon'$), loss ($\epsilon''$) and loss tangent (tan δ) were determined from the C–V and G/ω–V measurements. It is observed that $\epsilon'$, $\epsilon''$ decreases with the increase in frequency. Therefore, the proposed MOS structure provides a promising alternative approach to enhance the device capability in the opto-electronics industry.

One-dimensional (1D) nanostructures like nanowires and nanorods have attracted huge interest over the last few decades in the field of metal oxide semiconductor (MOS) for various applications like photodetectors$^{1-4}$, sensors$^{5,6}$, photovoltaic systems$^{7}$, non-volatile memory applications$^{8,9}$ etc. Following the Moore's law, the current semiconductor based MOS devices are facing a technological limitation in the form of scalability and leakage current. In order to further improve the MOS device performance, the International Technology Roadmap for semiconductors (ITRS) for future technology has recommended the use of a high mobility material as an alternative solution. In this context, recent papers have reported Germanium (Ge) with high-k dielectric based MOS devices which show good overall performance$^{10,11}$. This is because Ge has high electron and hole mobility compared to silicon (Si) and a low band gap which enables operation at low voltage$^{12}$. This feature, together with the opportunity to co-integrate Ge with high-k dielectrics such as Al$_2$O$_3$, HfO$_2$, TiO$_2$ etc., makes Ge a practical candidate for future MOS device applications. However, the integration of Ge with a MOS capacitor is challenging due to the native unintentional formation of GeO$_x$ which is unstable compared to SiO$_2$. This issue is mitigated by the integration of titanium dioxide (TiO$_2$) which is a high dielectric material with Ge. The unstable GeO$_x$ is reduced by the diffusion of Ge into the TiO$_2$. At the same time, rutile-TiO$_2$ can be formed which has a high-dielectric constant$^{13}$. Recent reports suggests that this approach can be achieved by various synthesis techniques for different applications$^{14-18}$. Amongst these synthesis techniques, the glancing angle deposition (GLAD) is a catalyst free environment friendly technique which can synthesize numerous materials for various applications$^{19-21}$. Furthermore, vertical nanowires can be easily achieved with the GLAD technique compared to other available techniques$^{22}$.

In this work, a Ag/TiO$_2$-NW/Ge-NW/Si (MOS) device is synthesized using the GLAD technique integrated into an electron-beam evaporator. The frequency and voltage dependence capacitance (C) and conductance
(G/ω) at room-temperature are analyzed. The aim of the work is to investigate the effect of interface state density (Dit), series resistance (Rs) on the C–V and G/ω–V characteristics as well as the dielectric parameters of the proposed MOS device with the applied bias voltage and frequency.

Results and discussion
The C–V and G/ω–V measurements of Ag/TiO2-NW/Ge-NW/Si MOS device are obtained for different frequencies and voltage ranges at room-temperature as shown in Fig. 1a,b. It is observed from Fig. 1a, that the MOS device displayed extensive distribution in depletion, inversion and accumulation regions. As seen in the figure, the MOS device showed an inversion region (-5 V to 0 V), a depletion region (0 V to 2 V) and an accumulation region (2 V to 5 V) at almost each frequency respectively. The voltage shift is due to the presence of surface states in the MOS device. The measured capacitance (C) and conductance (G/ω) values showed strong dependence on frequency and voltage in the depletion region which might be due to the Dit and Rs in the MOS device. The decrease in C and G/ω with the increase in frequency as shown in Fig. 2a,b, might be because the Dit cannot follow the alternating current (ac) signal at high frequencies and hence the contribution of these states to capacitance and conductance decrease with the increase in frequency. This makes the contribution of interface state capacitance to the total capacitance negligible. Thus, the measured C–V and G/ω–V values are close to the ideal case at high frequencies. At low frequency, the wide dispersion present in depletion region for both the C–V and G/ω–V curves is due to the existence of Dit.

The electrical parameters Dit and Rs could have attributed to the deviation in both the C–V and G/ω–V curves from the ideal behaviour. The unsymmetrical growth of nanowires due to the shadowing effect inherent in the GLAD technique may have induced inhomogeneous contact during the metallization process between the metal contact and the semiconductor junction. This also could be the reason for the deviation from the ideal behaviour of the MOS device. The Nicollian and Brews method is used to determine the parameters Rs in the measured voltage range of the MOS device. This method is reported to be more precise in comparison with Norde and Cheung functions and conductance and admittance methods as per previous report. Rs is calculated using the Eq. (1) given below:

Figure 1. Plots of the (a) C–V and (b) G/ω–V for the Ag/TiO2-NW/Ge-NW/Si (MOS) device.
where \( C_{m_a} \) and \( G_{m_a} \) are the measured C and G for any biased voltage and \( \omega \) is the angular frequency. Figure 3a,b, show the \( R_s-V \) plots determined from Eq. 1. It is observed from Fig. 3a that \( R_s \) decreases with an increase in frequency and the presence of peak around \( -0.5 \) V to \( 1.3 \) V at low frequencies is due to the presence of \( D_{it} \). The changes in \( R_s \) from region to region clearly shows that \( R_s \) is dependent on both the applied frequency and voltage. The change in \( R_s \) is evident especially in the inversion and depletion regions from the low to the high frequency range. It should be noted that \( R_s \) is independent of frequency at the accumulation region from frequency greater than \( 30 \) kHz. Furthermore, the voltage dependent \( R_s \) show almost constant value at higher frequencies (frequency > \( 200 \) kHz). This shows that for Ag/TiO$_2$-NW/Ge-NW/Si (MOS) device, the \( R_s \) is effective in the accumulation region in high voltage at high frequencies (frequency > \( 200 \) kHz).

The \( D_{it} \) is another parameter which affects the measured C–V and G/ω–V for the Ag/TiO$_2$-NW/Ge-NW/Si (MOS) device. The frequency dependent \( D_{it} \) plot can be obtained using the Hill-Coleman method from Eq. (2)

\[
R_s = \frac{G_{m_a}}{G_{m_a}^2 + (\omega C_{m_a})^2}
\]  

\[
D_{it} = \frac{2}{qA} \left( \frac{G_{m_a}}{C_{\text{ox}}^{\text{max}}} \right) + \left( 1 - \frac{C_{\text{ox}}}{C_{\text{ox}}^{\text{max}}} \right)^2
\]

where \( C_{\text{ox}} \) and \( (G_{m_a}/\omega)^{\text{max}} \) are the interlayer capacitance, maximum value of conductance which is corresponding to \( C_{\text{ox}} \) and the value of \( C_{\text{ox}} \) can be calculated from the measured C and G/ω values at the strong accumulation region using Eq. (3)

\[
C_{\text{ox}} = \frac{C_m}{1 + (\omega C_{\text{ox}})^2}
\]
The frequency dependent Dit determined using Eqs. 2 and 3 is shown in Fig. 4. It is observed that the Dit decreases with an increase in frequency for the Ag/TiO₂-NW/Ge-NW/Si (MOS) device which is due to the low power follow rate at high frequencies. Furthermore, the obtained Dit value at high frequency (frequency > 400 kHz) is found to be better in comparison with the reported values and thus addresses the serious issue of high interface state densities. The distinct peak seen in the Dit plot in Fig. 4 (inset) at 100 kHz and 300 kHz having Dit values of 1.73 × 10¹³ eV⁻¹ cm⁻² and 2.05 × 10¹⁰ eV⁻¹ cm⁻² with defect lifetime of ~ 10 μs and 3.3 μs, respectively. The difference in the lifetime of the defects observed from the Dit plot is primarily due to the slow traps and fast traps also known as interface traps corresponding to large defect lifetime and small defect lifetime, respectively. It can be seen that the maximum value of Dit decreases with an increase in Rs which is in good agreement with the theoretical results stated by Chattopadhyay et al. In order to obtain the corrected capacitance (Cc) and corrected conductance (Gc/ω) at different frequencies both measured C and G/ω are corrected considering the effect of series resistance (Rs) using the Eq. (4–6)

\[ C_{ox} = C_{ma} \left( 1 + \left( \frac{G_{ma}}{\omega C_{ma}} \right)^2 \right) \]

\[ C_c = \frac{G_m^2 + (\omega C_m)^2}{d^2 + (\omega C_m)^2} C_m \]
Figure 5 represents the CC–V and Gc/ω–V plots for the Ag/TiO2-NW/Ge-NW/Si (MOS) device. It is observed after making the correction that is considering the effect of Rs in Cc versus V plot, there is no significant change in the corrected capacitance (Cc) values. However in the case of the corrected conductance (Gc), it is observed that there is a decrease in the Cc value with an increase in frequency and the existence of peaks in the Gc/ω–V plot confirms the charge transfer taking place at the interface.

The dependence of the dielectric constant (ε′), dielectric loss (ε″) and dielectric loss tangent (tan(δ)) on the frequency and voltage are investigated in various frequencies (10 kHz to 5 MHz) at different voltage ranges (-5 V to 5 V) at room-temperature. The values of the dielectric constant (ε′), dielectric loss (ε″) of the Ag/TiO2-NW/Ge-NW/Si (MOS) device are obtained using the measured C, G/ω, thickness of the oxide layer, area of diode and permittivity of free space (ε0). The complex dielectric constant (ε* = ε′ − jε″), the real and imaginary parts could then be determined from the relations given in Eq. (7–8) given below:

\[
\varepsilon' = \frac{C_{ox}}{C_0}
\]

\[
\varepsilon'' = \frac{d_{ox} G_m}{A \varepsilon_0 \omega} = \frac{G_m}{C_0 \omega} \]

where C0 = ε0 (A / d_{ox}); A is the area of the device, d_{ox} is the oxide layer thickness, ε0 is the permittivity of free space (ε0 = 8.85 × 10−12 F/cm), Gm is the conductivity of MOS structure and ω is the angular frequency and j is the imaginary root of −1. The dielectric loss tangent can be determined by the relation given in Eq. (9) given below:

\[
\tan \delta = \frac{\varepsilon''}{\varepsilon'}
\]

Both the real and imaginary parts are calculated from the measured C and G/ω. The dielectric loss is expressed as the energy loss caused by the heating of a dielectric material in a variable electric field. The loss factor is known as the energy spent at the dielectric to avoid bound charge displacement to be in phase with the field alternations. From Fig. 6a-c, it is observed that the ε′, ε″ and tan(δ) values show independent behaviour from frequency in the inversion region and then starts to increase from the depletion region to the accumulation region. Furthermore, the ε′, ε″ and tan(δ) values decrease with increasing frequency. This behaviour can be explained by the fact that when the frequency is increased, the interfacial dipoles in the dielectric have less time to orient themselves in the direction of the alternating electric field and alternatively, the polarization decreases with the increase in frequency and remains constant. This implies that at higher frequencies, the contribution of D_a and dipole polarization could be neglected. In other words, the decrement in the ε′ is due to the fact that the dipoles do not have enough time to orient themselves in the direction of electric field and the D_a cannot follow the ac signal. Furthermore, the mix-phase established from the XRD plot, where both anatase and rutile type TiO2 are reported might also be the reason behind the decrement in the ε′. The broad peak observed in the tan(δ) plot at frequencies less than 200 kHz could be attributed to the relaxation process and the D_a. In addition,
the behaviour of decrease in the values of the measured capacitance (C), dielectric constant ($\varepsilon'$) and dielectric loss ($\varepsilon''$) decreases with the increase in frequency is attributed to the presence of the interfacial polarization mechanism. Moreover, to show the effect of voltage on the dielectric parameters, frequency dependent plots are shown in Fig. 7a–c at different bias voltage, respectively. It is observed that the decrease in values of $\varepsilon'$, $\varepsilon''$ and tan(δ) with the increase in frequency is due to the decrease in polarization with the increase in frequency and the values remains constant at high frequency. This implies that the contribution of dipole polarization and Dit could be neglected at high frequency. Therefore, the Dit cannot follow the ac signal and the absence of any interfacial polarization mechanism in the MOS device makes the contribution to C, $\varepsilon'$ and $\varepsilon''$ negligible at high frequencies (> 200 kHz). The low frequency dielectric behaviour of the MOS device can be attributed to four possible mechanisms: electrode interface, dc conductivity, dipole-orientation and charge carriers.

Experimental procedure

TiO$_2$-NW/Ge-NW is fabricated on a 1 cm × 1 cm n-type Si (100) substrate using the GLAD technique incorporated into an electron-beam evaporator (Vacuum Coating Unit Model-BC-300). Using an ultra-sonicator, the Si substrates are cleaned in a 3-step sequence using electronic grade acetone, methanol, and rinsed with de-ionized (DI) water. During the synthesis process, the base pressure of ~ 2 × 10$^{-6}$ mbar is maintained inside the electron-beam chamber. A deposition rate of 0.5 Å s$^{-1}$ is maintained during the synthesis of TiO$_2$-NW/Ge-NW using a digital thickness monitor (DTM). Firstly, a thin-film (TF) layer of Ge (30 nm) is deposited over the Si substrate using a pure 99.999% Ge source. Next the substrate is azimuthally rotated at.

Figure 5. Plots of the (a) $C_{C-V}$ and (b) $G_{C-\omega-V}$ for the Ag/TiO$_2$-NW/Ge-NW/Si (MOS) device.
30 rpm with substrate holder kept inclined at 85° with respect to the source where Ge-NW (200 nm) was synthesized. Subsequently the TiO2-NW (200 nm) is fabricated using pure 99.999% TiO2 source over the Ge-NW to obtain coaxial TiO2-NW/Ge-NW assembly. Finally, silver (Ag) metal contacts are fabricated using an aluminum mask with a hole area ~ 7 mm² on both the samples. The schematic of the Ag/TiO2-NW/Ge-NW/Si MOS device is given in Fig. 8a-d. The electrical characterization of the devices is performed using a Keithly 4200 SCS from 10 kHz to 5 MHz.

Conclusion

The electrical and dielectric parameters of a GLAD synthesized Ag/TiO2-NW/Ge-NW/Si (MOS) device have been studied over a wide frequency and voltage ranges. It has been determined from the measured C and G/ω behaviour of the MOS device that the parameters were dependent on the applied frequencies and voltages. In addition, the wide dispersion exhibited in both C and G/ω curves in the depletion region was mainly attributed to the existence of the D_{it}. Furthermore, the measured C and G/ω behaviour with the applied frequency and voltage were dependent on the D_{it}, R, and the polarization process. The D_{it} and R parameters were computed using the Hill-Coleman and Nicollian–Brews methods in wide frequency and voltage ranges. The dielectric properties analysis of the MOS device established that the ε’, ε” and tan(δ) parameters were dependent on frequency and that the values decrease with the increase in frequency. Furthermore, it is observed at higher frequencies (> 200 kHz), the ε’ and ε” values remains constant which is attributed to the interfacial polarization. Moreover, the decrement in the ε’ value for the MOS device is also due to the mix-phase of anatase and rutile type TiO2 present in the structure as determined from the XRD study reported earlier. Therefore, the study of the proposed MOS device has highlighted that it offers improved device capability for opto-electronics applications and also the potential for further improvement to obtain better device performance.

Figure 6. Plot of (a) ε’–V, (b) ε”–V, (c) tan(δ)–V for the Ag/TiO2-NW/Ge-NW/Si (MOS) device.
Figure 7. Plot of (a) $\varepsilon'$ versus ln f, (b) $\varepsilon''$ versus ln f, (c) tan(δ) versus ln f for the Ag/TiO$_2$-NW/Ge-NW/Si (MOS) device.

Figure 8. (a) Si wafer, (b) Synthesis of Ge-TF, (c) Synthesis of TiO$_2$-NW/Ge-NW/Si using GLAD technique, (d) Synthesis of Ag/TiO$_2$-NW/Ge-NW/Si (MOS) device schematic.
Data availability

The datasets generated during and/or analysed during the current study are available from the corresponding author on reasonable request.

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Author contributions
H.M.S performed the investigation, data curation, formal analysis and written the original draft. L.Y.Y contributed in review and editing of the original draft. P.C, the corresponding author conceptualize, provided supervision, validation, review and editing of the original draft. All authors reviewed the manuscript.

Competing interests
The authors declare no competing interests.

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