Low power analogue equaliser with adaptive digital tuning for fast ethernet

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Abstract: This work presents an analogue equaliser with digital tuning. It compensates the losses introduced by up to 120 m long category 5 unshielded twisted pair cables and baseline wander (BLW). The equaliser is designed for Fast Ethernet with a symbol rate of 125 MHz. A gbC filter, based on three first-order high pass filters, is used to compensate the cable loss. To minimise power consumption, three operational transconductance amplifiers (OTAs) are merged into a novel multi-input OTA structure. Additionally, a robust digital control logic is presented to automatically adjust the parameters of the equaliser for different cable lengths. A fast settling time below 250 μs is demonstrated for different scenarios. The equaliser is fabricated as part of a Fast Ethernet PHY chip in a 180 nm CMOS technology of GLOBALFOUNDRIES. Measurement results demonstrate error-free data transmission (bit error rate below 10^{-12}) for cable lengths up to 120 m. The power consumption of the analogue equaliser ranges from 2.3 mW (short cable) to 6.5 mW (120 m cable). To the best of the authors' knowledge, this is the lowest power consumption of an analogue equaliser for Fast Ethernet, supporting additional BLW and flat loss compensation reported to date.

1 Introduction

Wired communication via unshielded twisted pair (UTP) cables and in particular Ethernet is widely used for various applications. The used cables introduce frequency-dependent losses due to the skin effect, which result in intersymbol interference (ISI) [1]. To cope with this ISI, the loss of the cable has to be compensated by an equaliser. This equaliser can be placed either at the transmitter or at the receiver. This work focuses on the standard Fast Ethernet [2], which provides data rates of up to 100 Mb/s over up to 100 m category 5 UTP cables and is still widely used for many industrial applications. In this standard, it is clearly defined that the equaliser has to be placed at the receiver, which is typically implemented using digital finite impulse response (FIR) filters [3, 4]. This requires a high-speed analogue-to-digital converter (ADC) with a high resolution as well as several digital multipliers for the FIR filter, resulting in high power consumption. On the other hand, new trends as the Industrial Internet of Things are leading to a massive increase in the number of connected devices. Hence, the power consumption of Ethernet transceivers has to be reduced significantly for environmental and economic reasons. Additionally, in modern System-on-Chip designs where one or more transceivers are integrated together with data processing units, sensors and actuators, a reduction of the power consumption of the transceivers can help to avoid a costly and bulky cooling. These trends resulted for example in the introduction of the Energy Efficient Ethernet (IEEE 802.3az) standard in 2010 [5]. Energy Efficient Ethernet saves power by putting the transceiver in a sleep mode during long idle periods. However, this can only reduce the power consumption in use-cases with long idle periods or low data rates. Additionally, the cooling still needs to be dimensioned for high power consumption during long active periods. All in all, it is therefore also important to reduce the power consumption of the transceiver while it is active. In order to lower the power consumption of the receive path, this work presents the design of an advanced analogue equaliser for Fast Ethernet.

Besides the power savings, the analogue equaliser has the advantage of reduced latency. While digital filters have latency in the order of tens of clock periods, an analogue equaliser can have a group delay that is just a small fraction of the clock period. This reduced latency (and especially latency jitter) is very well suited for real-time applications as accurate time synchronisation [6, 7].

Besides the above-mentioned frequency-dependent loss, the analogue equaliser should compensate baseline wander (BLW). BLW is a low frequency offset, that occurs due to the low frequency cutoff frequency of the transformers used for ac-coupling. Additionally, small broadband losses (flat loss) may be compensated separately to the high frequency loss [8]. While analogue equalisers for Fast Ethernet or similar applications have been reported previously [8–11], most of them lack to compensate BLW [9–11]. For example, the low power equaliser in [11] is only designed to roughly compensate the high frequency loss for a simple two-level modulation. For Fast Ethernet, a three-level modulation is used. This requires a higher performance of the equaliser as the margin for noise or overshoot is decreasing. In [8] such an analogue equaliser for Fast Ethernet was presented that is able to additionally compensate BLW and the flat loss. In contrast to [8], the equaliser presented here achieves lower power consumption. Furthermore, the proposed equaliser tunes the high frequency gain by means of the bias current. This further reduces the power consumption for applications using short cables, providing even higher power savings compared to previous works [8].

In contrast to digital equalisers, it is challenging to automatically tune the parameters of the analogue equaliser for the used cable. This drawback is a reason why digital equalisers are preferred in simple implementations. To overcome this, a digital control logic is presented in this work, which is able to reliably tune the parameters of the analogue equaliser to the cable loss. This paper is organised as follows: in Section 2 the channel models used in this work are presented. Based on these models the design of the analogue equaliser is described in Section 3. Section 4 presents the digital control logic that is used to tune the parameters of the analogue equaliser to the used cable. The measurement results of the equaliser, fabricated in a 180 nm technology from GLOBALFOUNDRIES, are discussed in Section 5. Finally, in Section 6 a conclusion is given.
The transmitted voltage levels are +1, 0 and −1 V. At the transmitter after a 100 m cable shown in Fig. 1. The main signal impairments come from the UTP cables introducing losses and from the transformers used for ac-coupling. The full link model is characterised by the RLGC parameters \( L', G', C' \) and \( R' \) is modelled frequency-dependent to cover the losses by the skin effect:

\[
R'(\omega) = k_R(1+j)\sqrt{\omega} \cdot 1s
\]

In this work the following typical values from [1] are used:

\[
L' = 0.6 \, \mu H/m, \quad C' = 0.05 \, nF/m, \quad G' = 0.
\]

The parameter \( k_R = 0.2 \, \mu m \Omega/m \) is a constant depending on the material and geometry of the cable [1]. For Fast Ethernet cables with a maximum length of 100 m are used. However, to have margin, cables with a length of up to 120 m are used in this work. The calculated transfer functions using the model above are plotted in Fig. 2 for 90 and 120 m cables. These models are compared to the measured transfer functions of 90 and 120 m cables that are used to characterise the equaliser performance in measurements. The cable model shows a good agreement to the measured cables with a deviation of below 1 dB. The 120 m cable shows damping very similar to the maximum allowed insertion loss defined in the IEEE Ethernet standard [2]. Thus, the 120 m cable is used in simulations and measurements as the worst-case cable, to demonstrate the equaliser performance in the worst-case scenario.

### 2.2 Baseline wander

BLW is another issue that needs to be compensated at the receiver. In Fast Ethernet transformers with a minimum inductance of 350 \( \mu H \) are used to achieve an ac-coupling (see Fig. 1). This transformer will damp low frequency content in the data, which leads to a shift in the low frequency signal content at the receiver (offset) [12]. This offset is depending on the transmitted data. In the worst-case the offset will be as high as the signal itself, doubling the dynamic range of the signal [12]. However, this only occurs if a very long sequence of consecutive +1 or −1 symbols are sent, which is very unlikely. Therefore, for practical cases, a worst-case BLW frame is defined [13]. This worst-case BLW frame generates an offset of about 750 mV, which is 3/4 of the signal amplitude. This is high enough to shift the signal by more than the decision threshold. Thus, without a BLW compensation, a large amount of bit errors will occur.

The BLW is data-dependent and changes over time with frequencies below the cutoff frequency of the transformer (in the range of tens of kHz), which makes it challenging to compensate. Thus, most analogue equalisers lack to compensate BLW and shift this problem to the digital domain, which in turn increases the complexity for the ADC. To avoid this, the equaliser in this work is designed to compensate this low frequency offset in order to cancel the BLW in the analogue domain.

### 3 Design of the analogue equaliser

#### 3.1 Approximating the cable loss

To compensate the frequency-dependent loss of the cable an analogue filter is needed with the inverse transfer characteristic of the cable. The damping of the cable in dB is approximately proportional to \( \sqrt{\omega} [1] \), thus it can only be approximated by simple transfer functions with a finite number of poles and zeros. As done in [8], one can approximate the inverse transfer function of the cable with a superposition of multiple first-order high pass filters. As a general approach an approximation in the following form is proposed:

\[
G_{\text{equal}}(\omega) = G_0 + G_1 \frac{j\omega}{j\omega + 2\pi f_{p1}} + \cdots + G_n \frac{j\omega}{j\omega + 2\pi f_{pn}}
\]

The parameters \( G_0, \ldots, G_n \) represent the gain of the individual terms and \( f_{p1}, \ldots, f_{pn} \) are the pole frequencies of the high pass filters. The concept of this approximation is shown in Fig. 3 for \( n = 3 \) poles. If the filter parameters \( G_0, \ldots, G_n \) and \( f_{p1}, \ldots, f_{pn} \) are chosen correctly, it is possible to approximate the inverse transfer characteristic of the cable. To find the best filter parameters the quadratic difference of the magnitude (in dB) of the transfer...
 Due to this ambiguity, the optimisation may result in a higher than necessary gain $G_i$ and pole frequency $f_{pi}$. On the one hand, this will amplify noise at higher frequencies unnecessarily large, on the other hand, the implementation of the higher gain and bandwidth will also require a higher power consumption. Therefore, it is crucial to limit the last pole frequency and the overall gain to a reasonable value. To do so, the optimisation problem is adopted and a novel error $E_i$ is defined:

$$E_i = (G_i + G_{i+1} + \ldots + G_n) \cdot E$$

(5)

$E_i$ modifies the error $E$ defined in (4) by multiplying it to the squared overall gain. By minimising the error $E_i$, a good approximation of the cable damping (minimising $E$) is obtained, while also keeping the required overall gain low. If $f_{pi}$ and $G_i$ are increased, the error $E$ remains mostly unchanged, as the transfer function stays similar in the relevant frequency range. However, the overall gain is increased, which will increase the error $E_i$. Thus, minimising $E_i$ solves the problem with the ambiguity and helps to lower the power consumption of the equaliser as the needed gain and bandwidth is minimised as much as possible.

To use the equaliser for different cable lengths its parameters must be tunable. However, changing all parameters of the equaliser in dependency of the cable requires a complex tuning scheme. Therefore, a simplified tuning scheme is used: the pole frequencies are kept constant and will not change, only the gains $G_1$ to $G_n$ are tuned. To do so, all the parameters are first optimised for the worst-case cable model of 120 m, minimising (5) numerically. To adapt these parameters for different cable lengths, only two independent tuning parameters ($\alpha_{DC}$ and $\alpha_{HF}$) are used, that change high and low frequency gain:

$$G_i = \alpha_{DC} \cdot G_{i,120 \text{m}}$$

(6)

$$G_{i,120 \text{m}}$$ represent the gain settings obtained for the 120 m cable model ($G_{i,120 \text{m}} = 1$, $G_{i,120 \text{m}} = 0.24$, $G_{i,120 \text{m}} = 0.51$ and $G_{i,120 \text{m}} = 8.3$). Thus, for this worst-case damping $\alpha_{DC}$ and $\alpha_{HF}$ are set to 1. For shorter cables with lower losses, the tuning factors are decreased. In general, $\alpha_{DC}$ is always near 1 and is used to compensate for the flat loss. For a simple implementation one can keep $\alpha_{DC} = 1$ constant to further reduce the complexity of the tuning. However, in this work $\alpha_{DC}$ was implemented with some tuning capability to be able to compensate process variations or small changes in the flat loss. The factor $\alpha_{HF}$ is used to compensate the high frequency loss and is tuned from 0 (for very short cables) to 1 (for the maximum cable length). As will be discussed below, these two parameters ($\alpha_{DC}$ and $\alpha_{HF}$) are sufficient to obtain a good approximation of the damping for different cable lengths (see Fig. 5).

### 3.2 Implementation of the filter

There are two basic options for the implementation of the analogue filter described above: Operational amplifier (opamp) based filters [8] or $G_{mC}$-C filters [9–11]. Opamp based filters using an opamp with strong negative feedback typically achieve high linearity. For a very short cable, the input amplitude of the equaliser can be quite high as the undamped MLT-3 signal uses differential amplitude of 1 V with an additional offset of up to 750 mV due to BLW. Thus, in [8] an opamp-based topology is chosen for the equaliser to achieve the required linearity. However, the advantage of a $G_{mC}$-C filters is, that the gain of the filter is typically adjusted by the transconductance and thus by the current, which is beneficial for low power equalisers as follows. The maximum gain of the equaliser is only needed for long cables. For short cables, a much lower gain is needed. Using a $G_{mC}$-C filter, the gain can be decreased by reducing the current to reduce the transconductance. Thus, overall power consumption can be decreased for short cables. To utilise this advantage a $G_{mC}$-C filter as shown in Fig. 6 is implemented.
As desired, this equation has the same structure as the proposed filter transfer function in (3). The proposed equaliser can, therefore, be used to implement the filter transfer function obtained in Section 3.1. To do so, the circuit parameters \( R_i, G_{T_i}, R_C \) and \( C_i \) are obtained by comparing (8) to (3). The values of the resistors \( R_i \) to \( R_c \) and the capacitances \( C_i \) to \( C_c \) are derived from the pole frequencies \( f_{pi} \) to \( f_{pi} \), by the following equation:

\[
f_{pi} = \frac{1}{2\pi R_i C_i} \quad \text{for } i = 1, \ldots, 3
\]

The used values for the pole frequencies and the implementation with \( R_c \) and \( C_c \) are summarised in Table 1.

The transconductances \( G_{T_1} \) to \( G_{T_3} \) and the load resistance \( R_L \) are calculated based on the desired gains \( G_0 \) to \( G_3 \). Firstly, the load resistance \( R_L \) is determined, which limits the bandwidth of the equaliser together with a capacitive load. The parasitic capacitance at the output node of the equaliser together with a load capacitance from the following stages is approximately 400 fF. This capacitance forms an additional pole with the load resistance \( R_L \), which reduces the gain at high frequencies. A pole frequency of 150 MHz (about five times higher than the operating frequency of the equaliser) is targeted to not affect the equaliser performance. This gives a maximum load resistance of \( R_L = 2.74 \, \text{k} \Omega \), which is used in the design. A smaller value of \( R_L \) is not reasonable as it will increase the power consumption. After \( R_L \) is determined, the transconductances can be calculated as \( G_{T_i} = G_i/R_L \). To further lower the required transconductances the output swing is reduced to one-fifth of the input amplitude (200 mV instead of 1 V), so that it can be implemented easier with reduced supply voltages. To reduce the output swing is of course a trade-off between noise and power consumption. However, to reduce the output swing to 200 mV is found to be a good compromise that is still implementable with low enough noise and allows for a low power consumption. Thus, the transconductances are calculated as

\[
G_{T_i} = \frac{1}{5 \cdot \frac{G_i}{R_L}} \quad \text{for } i = 0, \ldots, 3
\]

Finally, BLW compensation is dimensioned. For the worst-case frame, a maximum BLW of ±750 mV is expected. With the damping of the equaliser, this corresponds to an offset of ±150 mV at the output of the equaliser. The current steering DAC will steer a differential current to the output. The DAC is designed such that an offset of −210 to +210 mV can be introduced with the load \( R_L \). This leaves some margin to cope with process variations or to compensate an offset generated by the mismatch in the equaliser itself.

### Table 1: Used values for the pole frequencies

| \( i \) | \( f_{pi} \) | \( R_i \), \( \Omega \) | \( C_i \), \( \text{pF} \) |
|---|---|---|---|
| 1 | 720 kHz | 44.2 | 5 |
| 2 | 5.38 MHz | 14.8 | 2 |
| 3 | 66.3 MHz | 2.4 | 1 |

### 3.3 Design of the OTAs

The OTAs used in the implementation require high linearity, as the input signal for a short cable will be very large. OTAs based on transistors operating in the triode region are used for the equaliser (see Fig. 7). Such designs are known to achieve very high linearity [14, 15]. The transistors \( M_1 \) and \( M_2 \) operate in triode region where their drain current \( I_D \) is linearly related to the gate-source voltage \( V_{GS} \):

\[
I_D = k_M (V_{GS} - V_{th}) \frac{V_{DS} - V_{th}}{2}
\]

Additionally, the drain current is strongly dependent on the drain-source voltage. Thus, an opamp is used to keep the drain potential constant (see Fig. 7). Furthermore, the opamp sets the drain-source voltages \( V_{DS1} \) and \( V_{DS2} \) equal to the tuning voltage \( V_{tune} \) which can therefore, be used to tune the transconductance. Assuming that the drain-source voltage equals the tuning voltage \( V_{tune} \); the small-signal transconductance is calculated as follows:

\[
G_T = k_M V_{tune}
\]

Thus, the transconductance can be linearly tuned by means of \( V_{tune} \). However, the transconductances \( G_{T_1} \), \( G_{T_2} \) and \( G_{T_3} \) are tuned by the same factor \( \Delta V_{tune} \). Therefore, these three OTAs can be combined in one cell by adding their currents already at the source of \( M_1 \) and \( M_2 \). This results in a proposed multi-input OTA, that is depicted in Fig. 8. The advantage is that the three stages share the same opamps for tuning. This reduces the complexity of the circuit and the power consumption, as only two opamps are required independent of the number of inputs of the multi-input OTA. For

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the case with three inputs, the number of opamps reduces from six (using three conventional OTAs as in Fig. 7) to only two, leading to lower power consumption and reduced chip area. The transconductance regarding each input of the multi-input OTA is again described by \( k_n V_{\text{tune}} \). As \( V_{\text{tune}} \) is now equal for \( G_{T1} \) to \( G_{T3} \), the individual transconductances are set by adjusting the width to length ratios of the transistors \( M_{11} \) that change the parameter \( k_n \) that is defined as:

\[
    k_n = \mu_n C_{\text{ox}} W / T
\]

The factors \( \mu_n \) and \( C_{\text{ox}} \) describe the mobility of the electrons and the oxide capacitance per area, respectively. The parameter \( k_n \) is linearly dependent on the width to length ratio \( W/L \), which can, therefore, be used to set the individual transconductances. As annotated in Fig. 8, the width to length ratios of the input transistors are scaled for each input to set the required transconductance. Thick-oxide transistors are used for these inputs to cope with the high input voltage swing. In the used technology, therefore, be used to set the individual transconductances. As annotated in Fig. 8, the width to length ratios of the input transistors are scaled for each input to set the required transconductance. Thick-oxide transistors are used for these inputs to cope with the high input voltage swing. In the used technology, therefore, be used to set the individual transconductances. As annotated in Fig. 8, the width to length ratios of the input transistors are scaled for each input to set the required transconductance.

\[
    \text{Table 1: Equaliser parameters for different cable lengths}
\]

| Cable Length (m) | \( V_{\text{tune}, \text{HF}}, \text{mV} \) | \( V_{\text{tune}, \text{DC}}, \text{mV} \) |
|------------------|------------------|------------------|
| 0                | 0                | 92               |
| 30               | 24               | 97               |
| 60               | 40               | 100              |
| 90               | 64               | 100              |
| 120              | 100              | 100              |

All in all two different OTAs are used within the equaliser: For the flat loss, the OTA \( G_{T2} \) is implemented as in Fig. 7 and for the high frequency loss the three transconductances \( G_{T1}, G_{T2}, \) and \( G_{T3} \) are merged within the multi-input OTA as in Fig. 8. Their tuning voltages are set by simple 8 Bit current steering DACs with respect to \( \alpha_{\text{DC}} \) and \( \alpha_{\text{HF}} \). The tuning voltage \( V_{\text{tune}} \) for the OTA \( G_{T3} \) ranges from 50 to 150 mV, while a value of 100 mV represents the nominal value \( \alpha_{\text{HF}} = 1 \). Thus, the additional margin is available to further increase the high frequency gain beyond the value calculated nominally for a 120 m cable.

The opamp used in the OTAs is a simple two-stage opamp shown in Fig. 9. The input stage is implemented with a PMOS differential pair, as the input common mode range of the opamp is at low voltages in the range of 100 mV. Because the opamp has a major contribution to the output noise of the equaliser, it was mainly optimised for low noise. To do so, the input differential pair (\( M_1 \) and \( M_2 \)) is realised with a high \( W/L \) using a high width to length ratio, while the load (\( M_3 \) and \( M_4 \)) uses a low width to length ratio. To ensure stability the capacitance \( C_k \) and resistor \( R_k \) are added.

The output voltages of the equaliser are \(-200, 0 \) and \(+200 \) mV for the three symbols, the decision threshold is therefore at \( \pm100 \) mV. Thus, the overall magnitude for noise is 100 mV. However, one has to consider that the equaliser may not compensate the ISI perfectly, that there is some noise (crosstalk) coupling into the cable or that jitter of the recovered clock might degrade the performance. For this reason, the equaliser is dimensioned such that the impact of the noise should not degrade the output voltage by more than 33 mV (one-third of decision margin). As a bit error rate (BER) as low as \( 10^{-12} \) is targeted, the root mean square (rms) value of the noise should be approximately seven times smaller so that the probability of the output voltage to exceed 33 mV is below \( 10^{-12} \) assuming Gaussian noise. Therefore, an output rms noise voltage of below 5 mV is targeted. Simulations are carried out to analyse the output noise of the equaliser and optimise the opamp. With the optimised transistor parameters given in Fig. 9 and a bias current of 100 µA flowing through \( M_1 \) and \( M_2 \) an output noise voltage of the equaliser of 4.5 mV is achieved. Thus, the opamps need to draw an overall current of about 200 µA to fulfil the noise requirements. This underscores the advantage of the proposed multi-input OTA presented above, with which the total number of opamps in the equaliser can be reduced from eight to four. This reduces the total current drawn by the opamps from 1.6 to 0.8 mA.

3.4 Simulation results

The equaliser is simulated for multiple cable lengths (0 to 120 m in steps of 30 m) using the cable model described above. The tuning parameters (high frequency gain and low frequency gain) are adjusted by hand to fit the given cable characteristics. They are given in Table 2. The simulated transfer functions for the different cable lengths are shown in Fig. 5 in comparison to the damping of the cable. It can be seen that the equaliser works very well to compensate for the cable loss for different cable lengths up to the frequency of \( f_{\text{max}} = 31.25 \text{MHz} \). The gain is tuned by changing the control voltages, which changes the bias currents in the OTAs.

The power consumption is therefore dependent on the cable length and varies from 2.3 mW for very short cables to 6.5 mW for a 120 m cable (see Fig. 10). This adaptivity is an advantage of the presented equaliser. It reduces the power consumption for many cases using short cables. For example, using a 40 m cable would halve the power consumption of the equaliser compared to a 120 m cable.

The equaliser should be robust against process variations. While deviations of the load resistance or transconductances can be easily...
The signal is overequalised leading to an overshoot, the process variations will be compensated by adjusting the gain settings for a little bit shorter or longer cables. Therefore, the presented analogue equaliser is inherently very robust against process variations.

4 Automatic control of the equaliser parameters

In order to adapt the settings of the equaliser for a given cable length, automatic control is needed to adjust the filter parameters. In general three parameters have to be adjusted: the high frequency gain, the low frequency gain and the offset for BLW cancellation. Such control can either be implemented analogue or digital. In [11] an analogue control loop is used to adjust the equaliser settings. However, in [11] only the high frequency gain is adjusted. No BLW compensation or compensation of flat loss is included. The realised control logic in [16] works only for fine-tuning. The initial equaliser settings have to be close enough in order for the control loop to converge, which is achieved with a coarse tuning during startup. In this work, in contrast, a robust control algorithm is proposed that is also able to converge from any initial conditions.

For the digital tuning, a low-resolution ADC is used to gather information about the equaliser output signal in order to update its filter coefficients. In this work, a flash ADC with five comparators is used. Note that this ADC has a much lower resolution, as it is required for a digital equaliser. Two of the comparators are used as a detector to determine which of the three symbols (+1, 0 or −1) is received. For each of the three symbols an additional comparator is added, to detect whether the equaliser output is smaller or larger than the symbol value. The information from all five comparator outputs is used to update the equaliser settings. The top-level schematic of the receiver is depicted in Fig. 12. At the output of the analogue equaliser are the five comparators to detect the signal. The comparator outputs are fed to the digital control logic that updates the equaliser coefficients. Three 8 Bit DACs are used to set the control algorithm is proposed that is also able to converge from any initial conditions.

The comparator outputs are fed to the digital control logic that updates the equaliser coefficients. Three 8 Bit DACs are used to set the control algorithm is proposed that is also able to converge from any initial conditions.

4.1 Control of the high frequency gain

To detect whether the high frequency gain of the equaliser is too high or too low, the transitions of +1 to 0 (and −1 to 0) are analysed. The received data transitions from +1 to 0 and stays at 0 for some
The frequency gain setting are not distinguished perfectly, which gives not perfect, as the signal might not have settled that fast, but it is a small frequency gain is too small, the signal is only slowly approaching zero. These patterns can be distinguished by means of the comparator that is checking whether the signal is larger or smaller than zero. For example, if the signal drops below zero after +1 to 0 transitions, the high frequency gain is decreased. Otherwise, it is increased. However, BLW could also be responsible for the same outcome. If the signal has a positive offset (BLW), the output can be above zero due to the offset itself. Thus, a positive offset can be wrongly interpreted as a too small high frequency gain. In order to distinguish between an offset and a wrong high frequency gain, data transitions from −1 to 0 have to be analysed additionally. For these transitions, similar patterns as in Fig. 13 with flipped y-axes) are observed. However, due to the flipped y-axis, a positive offset would now be interpreted as a too-large high frequency gain. Therefore, combining the information between both transitions allows to correctly identify if the high frequency gain is wrong or if an offset due to BLW is present. Thus, the control logic updates the equaliser parameters based on the last +1 to 0 transition and the last −1 to 0 transition. Depending on the result of both transitions the corresponding parameter (offset or high frequency gain) is incremented or decremented. However, as the control of the gain setting can be quite slow, the value of ctr_HF is only incremented or decremented with an update rate of 1 MHz (averaging the patterns of the last 125 clock cycles). This averaging will reduce the noise in the control parameter. The same is done for the low frequency gain setting described below.

4.2 Control of the low frequency gain

Very similar to the case above, another pattern is used to tune the low frequency gain. For this, the transitions from 0 to +1 or from 0 to −1 are analysed. This is shown in Fig. 14 with two example waveforms. If the low frequency gain is too high, the signal will approach a value greater than +200 mV after some time. If the low frequency gain is too small, the signal will approach a value smaller than +200 mV after some time. Ideally, one should analyse the output of the comparator checking if the signal is larger than 200 mV after a long sequence of +1 symbols. However, this occurs rarely in the signal stream. In this implementation, the value is analysed two clock cycles after the transitions from 0 to +1 to check whether the low frequency gain needs to be adjusted. This is not perfect, as the signal might not have settled that fast, but it is a reasonable trade-off in order to increase the likelihood that this pattern is occurring in a random data stream that worked well in simulation. However, long term BER measurements (discussed below) show that the low frequency gain setting and the high frequency gain setting are not distinguished perfectly, which gives some performance degradation for long cables. Thus, for future implementations, the pattern should be extended to check the low frequency gain several clock cycles after the transition at the cost of reduced convergence speed.

Similar to the pattern for the high frequency gain, the same comparator outputs can also occur due to an offset (BLW). However, this can be distinguished again by analysing both transitions (0 to +1 and 0 to −1) and combining the results in the same manner as for the high frequency gain.

4.3 Control of the BLW compensation

The above-described patterns for low and high frequency gains allow to cancel the offset (BLW compensation). However, as BLW can evolve quickly, it is crucial that the control loop to track the BLW is very fast. Therefore, an additional pattern is used that is triggered every MLT-3 cycle. Thus, it occurs very often and is used to speed up the convergence if BLW results in a fast change of the offset. The additional pattern detects if the signal is larger (or smaller) than +200 mV after a transition from 0 to +1 and larger (or smaller) than −200 mV after a transition from 0 to −1. This will be due to a positive (or negative) offset. By using both transitions, one can distinguish a wrong offset from other effects like a wrong gain setting. Note the difference to the patterns for the low frequency gain described above, which checks the amplitude several cycles after a transition and requires multiple consecutive +1 or −1 symbols. For the BLW compensation described here, the amplitude right after the transition is analysed. Thus, each 0 to +1 (or 0 to −1) transition can be used to detect the offset in the data. To further improve the convergence speed, the increment step of ctr_blw is increased if the same offset is detected consecutive times. Typically, ctr_blw is increased or decreased by one if negative or positive BLW is detected. However, if a positive (or negative) BLW is detected m times in a row without detecting negative (or positive) BLW in between, ctr_blw is decreased (or increased) by m instead of 1. Thus, the control logic is faster and can better track BLW as it develops.

4.4 Additional patterns

The following additional patterns are used to allow and improve the convergence in case the equaliser is strongly detuned (e.g. after startup):

1. If the signal is not exceeding either +100 or −100 mV for a long period of time (256 clock cycles) the high frequency gain is increased.
2. If non-allowed MLT-3 transitions from +1 to −1 (or −1 to +1) occur, the high frequency gain is decreased. Those transitions are typically detected if the high frequency gain is much higher than required.
3. If a wrong MLT-3 cycle is detected with a signal going from +1 to 0 and back to +1 the offset is decreased. The offset is increased for wrong cycles going from −1 to 0 and back to −1.
4. If the signal is not exceeding −100 mV for a long period of time (256 clock cycles) the offset is increased. Similarly, if the signal does not go below 100 mV the offset is decreased.

Those patterns cover all extreme cases in which the gain or offset settings are much too high or much too low. The convergence is verified in simulation for all corner cases in which the initial values for the three parameters of the equaliser are at their minimum or maximum setting and for different cable lengths. This demonstrates the robustness of the presented control algorithm that is able to reliably converge to the correct equaliser settings.

4.5 Implementation

The digital control logic is implemented in SystemVerilog. Synthesis and place and route the circuit is done with Synopsys Design Compiler and Cadence SoC Encounter, respectively. The digital control logic uses 965 standard cells, occupies a layout area of 0.046 mm² and has a power consumption (including the DACs) of about 2.3 mW operating from 1.8 V supply in the used 180 nm technology.

5 Experimental results

The equaliser was fabricated as part of a Fast Ethernet PHY chip in a 180 nm technology of GLOBALFOUNDRIES. For
measurement, the chip is bonded to a printed circuit board (PCB) with some required off-chip components. It is connected to a second PCB with an STM32F4 microcontroller with integrated media access control (MAC) layer, which is used to transmit and receive data over the implemented Ethernet PHY. This configuration is shown in Fig. 15.

Two of these PCB setups are used to measure the performance of the equaliser. One PHY chip is used as a transmitter [19], while the other one is used as a receiver with the equaliser to be characterised. For measurement, a buffer is included for the analogue output signal of the equaliser. This signal is measured with a 4 GHz real-time oscilloscope (Rhode & Schwarz RTO1044) in the time domain. In Fig. 16 the measured eye diagrams are shown for different cable lengths and setups. The shortest cable that is used has a length of 0.3 m as cables with length 0 m cannot be realised practically. However, this can still be compared to the simulations with a length of 0 m, as the damping of a 0.3 m cable is negligible. For each cable length (0.3, 90, and 120 m) the eye diagram is shown without equaliser (setting $ctr_{HF} = 0$ and $ctr_{DC} = 110$), with the manual tuning of the equaliser parameters and with the automatic tuning of the equaliser parameters with the integrated digital control logic. For the short cable (0.3 m) one can see that the eye diagram is still open without equaliser (no ISI present) as expected. For the long cables (90 and 120 m) the eye diagram is seriously degraded without equaliser. With the equaliser, the signal quality can be massively improved. In all cases, the automatic digital control logic is able to control the equaliser settings such that an open eye is achieved. A comparison of the results obtained from manual tuning and the results with the digital control logic shows only small degradations due to the digital control algorithm. Therefore, we can conclude that the presented digital control algorithm works very well to automatically adjust the equaliser parameters. A more detailed and quantitative analysis is obtained by BER measurements, which are discussed as follows.

5.1 Bit error rate

The most important measure besides the eye diagram is the BER. The BER is measured using the complete receive path of the
settle to the optimal parameters. For different samples, BERs in the range of $10^{-7}$ to $10^{-10}$ are measured. This is still a good value, showing that the control logic is working quite well. However, it does not reach the same performance as with careful hand-tuned parameters. The reason for this issue is found in the dependency between the low and high frequency gains’ setting. The patterns to detect the low frequency gain are also dependent by the high frequency gain. To decouple this, longer sequences of $+1$ or $-1$ symbols should be analysed to extract the low frequency gain. The result is more accurate. However, the low frequency gain is always very close to one, as the broadband losses in such an Ethernet link are very small. Thus, it is possible to set the low frequency gain to a fixed value and only change the high frequency gain and the BLW compensation. If the low frequency gain is fixed to the optimal value, the digital control loop is able to find the correct setting for the high frequency gain and the link is error-free. For this final setting the BER measurements are carried out for a guaranteed length of more than $10^7$ bits. The low frequency gain setting is set to 110 for all cable lengths, while the BLW compensation and high frequency gain setting are controlled automatically by the digital control logic. For all cables (0.3, 90 and 120 m) no bit errors occurred for more than $10^7$ bits transmitted. Thus, the link is considered to be error-free with a BER $< 10^{-12}$. The equaliser is still able to automatically adjust its parameters to the connected cable by means of the high frequency gain setting. In a future version the problem with the control of the low frequency gain can be fixed by using a longer sequence of consecutive $+1$ or $-1$ symbols to decouple the different gain settings. That will further improve the robustness and can compensate small changes of the low frequency gain due to process variations. The drawback will be a longer setting time. However, the equaliser is still working very well with a fixed control setting for the low frequency gain.

5.2 Setting behaviour of the digital control logic

The digital control logic allows the automatic control of the equaliser parameters. This control loop converged in all measurements for all tested cable lengths. To analyse the robustness and setting behaviour of the control loop, different scenarios like disconnect and reconnect of the cable are tested. If the cable is disconnected, the equaliser will be tuned for the maximum gain settings as the input signal is zero. If the cable is reconnected later, the control logic must be able to converge to the correct equaliser settings from this extreme starting point of maximum gain. This test is passed for all cables tested. In Fig. 18 the setting behaviour is shown after a reconnect of a short 0.3 m cable, which represents the worst-case, as the gain needs to be reduced the most. It can be seen that after the reconnect the gain starts at its maximum setting, that is too high for the short cable. Within 250 μs the control loop settles and automatically reduces the gain settings to the correct value. This convergence behaviour matches with the simulation results. The setting time of about 250 μs is very low and allows a fast startup of the link. For Fast Ethernet, the link should be recovered within 1 μs, which is achieved by a great margin.

The settling behaviour at the startup of the digital control logic for the 120 m cable is shown in Fig. 19. In this case, the equaliser parameters are set to the minimum settings manually before the control logic is activated. With the minimum settings, the gain is too small for the long cable. Thus, the control logic is increasing the equaliser gain settings. Convergence is again achieved within 250 μs, showing the good performance of the digital control logic.

Finally, the digital control logic is tested for the compensation of BLW. To do so, the worst-case BLW frame [13], producing a BLW of up to 750 mV, is transmitted and the waveform after the equaliser at the receiver is measured. Note that this offset is damped to 150 mV at the output of the equaliser. For the 120 m cable, the waveforms with and without the BLW compensation are shown in Fig. 20. The BLW frame is received at $t = 0$ and has a length of 1500 bytes payload (120 μs). It can be seen that without the BLW compensation large negative BLW develops within 20 μs after the start of the frame. The offset at the output of the equaliser

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**Fig. 17** Measured BER for different settings of the high frequency gain (ctr_HF) for short and long cables. The low frequency gain setting (ctr_DC = 110) is constant, only the offset (BLW compensation) is determined automatically using the digital control logic.

**Fig. 18** Measured setting behaviour of the equaliser output after reconnecting a 0.3 m cable.

**Fig. 19** Measured settling behaviour at startup of the digital control logic for a 120 m cable.
correct behaviour of the BLW compensation is additionally shown with the eye diagrams of the transient waveforms shown in Fig. 20. Without BLW compensation the offset is massively degrading the eye, making the correct detection of the symbols impossible. With the BLW compensation, an open eye is achieved that shows no significant degradation due to the offset. Of course, the BLW compensation does also work for shorter cables, only the most critical case (long cable) is shown here.

### 5.3 Comparison to the state-of-the-art

The fabricated PHY chip using the equaliser of this work has a total power consumption of <70 mW under full link utilisation and using a 120 m cable, which matches the expectations from the simulation. The exact power consumption of the analogue equaliser cannot be measured as the same supply is used for the complete analogue part of the PHY chip. However, from simulation, power consumption of 2.3 mW (for short cables) to 6.5 mW (for 120 m cable) is obtained. To verify this, the difference in the power consumption using a 120 m cable and 0.3 m cable is measured to be 4.0 mW, which matches the simulation results (4.2 mW) with a difference of only 5%. Table 3 summarises the performance of the presented analogue equaliser and compares it with the state-of-the-art. Only the analogue equaliser without the digital control logic is compared to the other work to allow a fair comparison. In [11] a very low power consumption of 3.7 mW is achieved. However, it does only support two-level on-off keying (OOK) and no BLW and flat loss compensation. With a two-level modulation the requirements for the equaliser are much more relaxed: on the one hand, the margin for noise is larger. On the other hand, wrong equaliser settings (in particular overshoot) have a smaller effect. For a three-level modulation an overshoot of the symbol 0 may be wrongly detected as +1 or −1. Therefore, the impulse response of the cable has to be approximated with increased accuracy. This lack of important features for Fast Ethernet explains the very low power consumption in [11]. In [8] a low power analogue equaliser for Fast Ethernet is presented that fulfils all important requirements (BLW compensation and 3-level encoding). However, the power consumption of the equaliser in our work (6.5 mW for 120 m cable) is significantly smaller than that reported in [8]. Additionally, the power consumption of the equaliser presented here is adaptive, resulting in decreased power consumption for short cables. The equaliser works for cable lengths up to 120 m, which is slightly better than the other work that only demonstrated cable lengths up to 100 m. For very short cables, the power consumption of the analogue equaliser further reduces to only 2.3 mW, improving the work in [8] by more than a factor of 4.

### 6 Conclusion

This work presents a low power analogue equaliser for Fast Ethernet with a digital control logic to automatically tune the equaliser parameters. Measurements demonstrate that the equaliser is able to compensate high frequency losses, flat loss and BLW for up to 120 m long category 5 UTP cables. The power consumption is dependent on the cable length as the bias current is used to tune the gain. This adaptivity helps to reduce the power consumption in use-cases where non-maximum cabling is used. The power consumption of the analogue equaliser ranges from 2.3 mW for short cables up to 6.5 mW for long cables (120 m). To achieve this, the design is specially optimised for low power consumption as follows. To fit the equaliser transfer function to the cable loss, an error function is proposed that is minimised numerically. This error function includes the overall gain, such that the required gain for the equaliser will be minimised, which in turn reduces the power consumption. Additionally, three OTAs in the design of the equaliser are combined in a multi-input OTA. This novel approach reduces the number of opamps that are required in the OTAs and therefore reduces the power consumption and chip area.

The analogue equaliser features three tuning parameters to tune the high frequency loss, the flat loss and BLW independently from each other. These parameters are set by the digital control logic, that detects patterns in the received data stream to increment or decrement these parameters. This digital control logic with the DACs consumes only about 2.3 mW of additional power. Measurement results verify that the digital control logic can reliably converge to the correct equaliser settings from different initial conditions (unplugging the cable, startup from extreme initial conditions). Some difficulties in distinguishing the low and high frequency gains’ setting have been discussed. This can degrade the BER slightly for long cables. This problem can be addressed in a future version. However, by setting the low frequency gain to a fixed value and only adjusting the high frequency gain and BLW compensation automatically, this problem can be solved. Doing so, an error-free link with BER < 10⁻¹² is demonstrated.

The equaliser transfer characteristic is designed to compensate the cable losses up to about 31.25 MHz to be well suited for usage in a low power Fast Ethernet PHY with a symbol rate of 125 MHz. The equaliser and especially the digital control logic are optimised for this standard and cannot be directly used for other applications. However, future work can analyse the possibilities to apply the same principle to other standards or frequency ranges. Especially Gigabit Ethernet (1000BASE-T), which is using the same baud rate as Fast Ethernet, could use the same analogue equaliser. Usage for
Gigabit Ethernet would require changes in the digital control logic to be compliant with other signal levels and modulation formats. Additionally, future work should analyse possibilities to increase the bandwidth of the analogue equaliser for further applications. With the presented fitting method, the losses of a cable or channel can be fitted to an OTA-based equaliser as described in this work. Depending on the required accuracy, multiple pole frequencies can be used. In general, OTA-based filters are well suited to operate at high frequencies. However, the OTA used in this work uses an opamp in the feedback path, that is limiting its high frequency performance. Therefore, if the equaliser is used in higher frequency applications it may be necessary to either use a different topology for the OTA or to use a more advanced process node. Similarly, the digital control logic is also limited by the operating frequency and the given technology.

The equaliser is used in a real-time Fast Ethernet PHY chip optimised for lowest power consumption. The proposed equaliser reduces the power consumption of the receive path and thus helps to reduce the power consumption of the overall PHY. The total power consumption of the complete Ethernet PHY chip, fabricated in a 180 nm technology from GLOBALFOUNDRIES, is below 70 mW under full link utilisation and for operation with a 120 m cable.

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