Electrical Properties of Sulfonated Polyaniline Thin Film Grown on Different GaAs Substrates

Mohammed Kadhim Jaqsi, a Dler Adil Jameel,b,c † Diyar Sadiq a

a Centre for Material Science and Nanotechnology, Department of Physics, Faculty of Science, University of Zakho, Kurdistan Region-Iraq
b Department of General Science, College of Basic Education, University of Zakho, Kurdistan Region-Iraq
c School of Physics and Astronomy, Nottingham Nanotechnology and Nanoscience Center, University of Nottingham, NG7 2RD, United Kingdom
† Corresponding author: dler.jameel@uoz.edu.krd

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The paper describes the impact of the crystallographic orientation of an n-type GaAs substrate on the electrical properties of a sulfonated polyaniline (SPAN) thin film with a thickness of 120 nm grown on different n-type GaAs substrates orientation, which are (100), (311)A, and (311)B GaAs planes. Electrical characterization was performed by using current density-voltage (J−V) at room temperature and different temperatures (60−360 K). An ideality factor (n), a Schottky barrier height (Φb), and an activation energy (Ea) were extracted from forward J−V characteristics. From the J−V results, it was obtained that the rectification value at 0.5 V for the SPAN/(311)B GaAs hybrid device is higher than those for SPAN grown on the (100) and (311)A GaAs planes. Furthermore, as the temperature of the three heterojunction devices rises, the value of Φb increases, n drops, and Ea rises. The Ea measurements revealed that Ea for the SPAN/(311)B n-type GaAs heterostructure is lower than those for SPAN samples grown on the (100) and (311)A n-type GaAs planes. This could be related to the low number of defects in SPAN/(311)B than the other two samples. These results make SPAN with a thickness of 120 nm grown on the high index GaAs planes an interesting hybrid device for future devices applications.

Keywords Organic-inorganic device; (100) n-type GaAs; (311)A n-type GaAs; (311)B n-type GaAs; J−V and activation energy

I. INTRODUCTION

Organic semiconductors, for instance, sulfonated polyaniline (SPAN), polyaniline (PANI), poly(p-phenylene-vinylenes), polythiophene polymers, etc. [1], have the most observation for applications in optoelectronics and electronic devices because of easy synthesis and their unique electrical properties [2−4]. Therefore, this type of polymers has been utilized in different applications such as solar cells [5, 6], gas sensors [7], organic light emitting diodes [8, 9], electromagnetic interference shielding [10], photodiodes [11], radiation sensors [12], anti-corrosive coatings [13, 14], biosensors [15], transistors [16], energy storage [17], and battery electrodes [18, 19].

SPAN, which is a kind of self-doped conducting polymers, and a p-type semiconductor with a direct band gap energy of 2.755−2.883 eV [20], represents a derivative of polyaniline. It attracts a significant attention recently because of its individual electroactive physical properties, potential industrial applications, and enhanced process ability [21−23]. This material remains naturally steady at different temperatures. Interestingly, it has been grown with low cost over large areas as thin films [3]. Moreover, SPAN forms ohmic contacts with metals such as Ag, Cu, and Al used in microelectronic applications [6]. SPAN with a thickness of 200 nm has been grown successfully on GaAs substrates depending on the applications [24]. Much research has focused on the devices based on the low index of GaAs such as a (100) plane. Recently, high index GaAs substrates have attracted much attention [25, 26], such as (311)B GaAs [25, 27] and (311)A [27]. This is due to the optical characteristics of heterojunction grown on high index (311)A and (311)B...
GaAs that are much better than the one grown on conventional (100) GaA orientation [27].

As noted, there was an important influence on the integration of impurities and defects, therefore on the electronic properties of III-V materials by the substrate orientation [28]. The quality of the Schottky interface is stated by the barrier height and ideality factor (n) which are basic parameters of the Schottky barrier diode. The analysis of the current density-voltage (J−V) properties of the Schottky barrier diode does not afford exact data concerning the mechanism of conduction and the barrier nature made at the metal-semiconductor interface when measured only at room temperature. Therefore, it must be determined over different temperatures to recognize these phenomena and the mechanism of conduction and the barrier nature made at room temperature. Therefore, it must be determined over different temperatures to recognize these phenomena and the Schottky diodes parameters. Hardikar et al. [29] studied the J−V measurements that stated a decline in the values of n and an increase in the values of a zero-barrier height (Φn0) with increasing temperature. Subsequently, the barrier height and the ideality factor obtained from forward J−V data were observed to be dependent on the temperature. This verifies that the Schottky barrier height in nature is nonhomogeneous at the interface between the conducting polymer and the inorganic semiconductor. This conduct is effectively described based on the thermionic emission with a Gaussian distribution of the barrier height [30]. Additionally, Jameel et al. [24] pointed out that the SPAN (200 nm)/(311)B n-type GaAs samples showed better electrical properties than SPAN (200 nm)/(100) n-type GaAs and SPAN (200 nm)/(311)A GaAs hybrid devices.

This study presents the fabrication and electrical characteristics of a SPAN thin film with a thickness of 120 nm grown on a conventional (100) n-type GaAs substrate and high index (311)A and (311)B n-type GaAs substrates. Additionally, the influence of the substrate orientation of n-type GaAs on the parameters of heterojunction, i.e., Φn0, n, and the activation energy (Ea), has been investigated by using short current-voltage technique at different temperatures. We note that SPAN (120 nm)/(311)B n-type GaAs samples illustrated better electrical properties than the ones created on the conventional (100) and high index (311)A n-type GaAs substrates. In addition, it is important to mention that the electrical characteristics of our SPAN (120 nm)/(311)B GaAs devices are better than the SPAN devices with a thickness of 200 nm grown on (100), (311)A and (311)B n-GaAs substrates [24]. Therefore, the SPAN thin film with a thickness of 120 nm fabricated on (311)B n-GaAs plane can be considered as the strongest candidate to enhance efficiencies of such organic/inorganic hybrid.

### III. RESULTS AND DISCUSSION

The J−V measurements for all three samples were done by employing a current-voltage source meter unit (Solartron 1260 Impedance/gain-phase Analyzer) and a probe station (CRX-4K, Lake Shore Cryotronics, Inc.) at different temperatures (60–360 K) with an interval of 20 K. A profilometer (Dektak 6M) was used to measure thicknesses of the thin films.

II. EXPERIMENTAL DETAILS

SPAN thin films were grown utilizing the same technique as reported by Jameel et al. [24]. Briefly, n-type silicon-doped (100), (311)A, and (311)B GaAs substrates with a silicon concentration of 2 × 10^{18} cm^{-3} were utilized to grow the SPAN thin films. Following cleaning of the substrates, we deposited Ni–Au on the backside of the substrates through the thermal evaporation process to fabricate an ohmic contact. After the backside electrical deposition, a thin film of SPAN with a thickness of 120 nm was deposited. SPAN was grown on the low index (100) and high index (311)A as well as (311)B n-type GaAs substrates at a rate of 1.8 nm h^{-1} by employing the method that was initially developed by Yang et al. [31] and explained in Ref. 16. However, the amounts of metallic acid and aniline (1.715 g and 455 µL, respectively) and the growth temperature (10°C) were different. Finally, by using thermal evaporation, a circular electrical contact of Au with different areas were fabricated on the SPAN thin films as presented schematically in Figure 1. The fabricated heterojunction devices were termed as Au/SPAN/(100) n-type GaAs, Au/SPAN/(311)A n-type GaAs, and Au/SPAN/(311)B n-type GaAs.

The J−V plots for all three devices measured at various temperatures are displayed in Figure 2. It can be observed from Figure 2(d) that a better J−V characteristics at room temperature were measured on SPAN/(100) n-type GaAs, SPAN/(311)A n-type GaAs, and SPAN/(311)B n-type GaAs heterostructure devices. Moreover, to investigate Φn0, n, and Ea, the J−V measurements were carried out in a range of 60–360 K with an interval of 20 K for all three samples. Semi-logarithmic scale J−V plots for all three devices measured at various temperatures are displayed in Figure 2.
applied voltage of ±0.5 V and at room temperature are found to be approximately 89.85 for SPAN/(100) n-type GaAs, 4.6 × 10³ for SPAN/(311)A n-type GaAs, and 4.4 × 10⁴ for SPAN/(311)B n-type GaAs. It is to be noted that the higher rectification value for SPAN/(311)B n-type GaAs is considered to be an indication that the interface charge is at the lowest point between the SPAN and (311)B n-type GaAs planes. The rectification values that have been recorded by Jameel et al. [24] for the samples with the SPAN thickness of 200 nm are not as high as the ones obtained in this study, as exhibited in Table 1. Therefore, the devices of the present study demonstrate better electrical properties because of the reduction of the thickness of conducting polymer (SPAN) from 200 to 120 nm. Valaski et al. [32] argued that the device efficiency is expected to decrease for a large thickness because the performance of the device was limited due to a higher series resistance which results in an increased potential drop inside the device as the current density increases. This indicates that, in addition to the effect of substrates orientations of GaAs, the thickness of the polymer affects the electrical properties.

Table 1: Summary of the rectification ratio, the ideality factor, and the barrier height at room temperature (T = 300 K) for the SPAN samples with thicknesses of 120 and 200 nm grown on (100), (311)A, and (311)B GaAs.

| Sample                  | Rectification ratio (Jr/Jr) | Ideality factor (n) | Barrier height (Φb) | Reference  |
|-------------------------|----------------------------|---------------------|---------------------|------------|
| SPAN (120 nm)/(100) GaAs| 89.85                      | 1.503               | 0.521 eV            | this work  |
| SPAN (200 nm)/(100) GaAs| 2 × 10²                    | 1.77                | 0.62 eV             | [24]       |
| SPAN (120 nm)/(311)A GaAs| 4.6 × 10³                 | 1.297               | 0.649 eV            | this work  |
| SPAN (200 nm)/(311)A GaAs| 3.7 × 10³                 | 1.63                | 0.67 eV             | [24]       |
| SPAN (120 nm)/(311)B GaAs| 4.4 × 10⁴                 | 1.232               | 0.734 eV            | this work  |
| SPAN (200 nm)/(311)B GaAs| 1.7 × 10⁴                 | 1.61                | 0.72 eV             | [24]       |
factor, the series resistances, and the barrier height parameters. The forward bias of the $J$–$V$ measurements, as presented in Figure 2(a–c), were entirely nonlinear at high voltages as a result of the influence of defects at the interface and the series resistance. The $J$–$V$ characteristics could be explained by well-known the thermionic emission of conducting electrons and are expressed by [33];

$$J = J_0 \left[ \exp \left( \frac{qV}{nkT} \right) - 1 \right], \quad (1)$$

where the saturation current density ($J_0$) is obtained from an intercept point on the $\ln J$ axis at $V = 0$ of $\ln J$ as a function of $V$ (Figure 3) [33]. $J_0$ is expressed by

$$J_0 = A' \exp \left( -\frac{q\Phi_{b0}}{kT} \right). \quad (2)$$

When $J_0$ is calculated, $\Phi_{b0}$ could be obtained by applying Eq. (3):

$$\Phi_{b0} = \frac{kT}{q} \ln \left( \frac{A'T^2}{J_0} \right) \quad (3)$$

In the above equations, $T$ is the absolute temperature, $q$ is the elementary charge, $k$ is the Boltzmann constant, $V$ is the forward bias voltage, and $A'$ is the effective Richardson’s constant [33]. The ideality factor ‘$n$’, from Eq. (1), represents an assessment of the conformity of the diode behavior to pure thermionic emission. $n$, which is a dimensionless quantity, can be described by

$$n = \frac{q}{kT} \frac{\partial \ln J}{\partial V}. \quad (4)$$

For all three samples at each temperature, $\Phi_{b0}$ and $n$ were obtained by using Eqs. (3) and (4) from the forward bias $\ln J$ as a function of $V$ (Figure 3). The values of $n$ and $\Phi_{b0}$ for the SPAN/(100) n-type GaAs heterojunction varied from 6.892 and 0.1199 eV at 60 K to 1.383 and 0.563 eV at 360 K, respectively. For the identical temperature range, these values changed from 5.608 and 0.159 eV to 1.172 and 0.7009 eV for SPAN/(311)A n-type GaAs and from 5.188 and 0.1896 eV to 1.112 and 0.779 eV for SPAN/(311)B n-type GaAs. Clearly, as shown in Figure 4, $n$ and $\Phi_{b0}$ depend on the temperature, i.e., $n$ decreases and $\Phi_{b0}$ increases with increasing temperature for all three heterojunction samples. This behavior was also noted in polyaniline/GaAs heterostructures [34]. The current which passes through the interface between organic and inorganic materials is a temperature activated procedure, where the electrons have capability to overcome only the lower

![Figure 3](image3.png)

**Figure 3:** Plot of $\ln J$ as a function of $V$ for (a) SPAN/(100) n-type GaAs, (b) SPAN/(311)A n-type GaAs, and (c) SPAN/(311)B n-type GaAs hybrid devices at different temperatures.

![Figure 4](image4.png)

**Figure 4:** Temperature dependence of (a) the ideality factor and (b) the barrier height experimentally obtained from the forward $J$–$V$ characteristics of the SPAN/(100) n-type GaAs, SPAN/(311)A n-type GaAs, and SPAN/(311)B n-type GaAs devices in the temperature range between 60 and 360 K.
barriers at low temperatures and, consequently, the current transport is controlled by the current flowing across the regions of larger $n$ and lower $\Phi_{b0}$ [35]. This indicates that, once the temperature increases, more electrons have an enough energy to overcome a higher barrier. Consequently, additionally to the zones of the heterojunction with the low barriers, the prevalent barrier in other regions will increase with the bias voltage and the temperature [34]. Moreover, inhomogeneity of the thickness and barrier inhomogeneity as well as other influences, for instance, nonuniformity of the interfacial charges and defects, result in an obvious increase in the ideality factor and a decrease in the barrier height at low temperatures [29].

The room temperature ideality factors are found to be 1.503, 1.297, and 1.232 for SPAN/(100) n-type GaAs, SPAN/(311)A n-type GaAs, and SPAN/(311)B n-type GaAs, respectively, as displayed in Figure 4(a). Furthermore, as observed in Figure 4(b), the room temperature barrier heights are calculated to be 0.521, 0.649, and 0.734 eV for SPAN/(100) n-type GaAs, SPAN/(311)A n-type GaAs, and SPAN/(311)B n-type GaAs, respectively. The value of $\Phi_{b0}$ of SPAN fabricated on the (311)B n-type GaAs substrate is higher than the other two substrates and is larger than the one stated by Jameel et al. for the SPAN (200 nm)/(311)B n-type GaAs sample [24], as displayed in Table 1. Therefore, a good quality of the SPAN film grown on the n-GaAs substrates is verified by the low values of $n$ and the high values of $\Phi_{b0}$ at 300 K. For an ideal diode ($n = 1$), it can be seen that all three devices have different values of $n$ which differs from unity, nonetheless the SPAN/(311)B n-type GaAs hybrid sample is closest to the ideal state and better than the value observed by Jameel et al. [24], as exhibited in Table 1. The ideality factors of the heterojunctions studied in this research were greater than unity ($n > 1$). The large ideality factor is associated with the existence of a bias dependent Schottky barrier height [36]. The recombination current process at the SPAN/n-GaAs interface, the potential decline in the interfacial layer, and the existence of additional current can be factors for the larger values of $n$ [24].

From Table 1, it can obviously be noted that the SPAN/(311)B GaAs sample have greater rectification, the lower $n$ values, and the higher $\Phi_{b0}$ values when they are not only compared to SPAN (120 nm) grown on the (100) and (311)A GaAs planes but also to SPAN (200 nm) fabricated on (100), (311)A and (311)B GaAs, which were studied by Jameel et al. [24]. These results indicate that the SPAN (120 nm)/(311)B GaAs sample have good electrical properties and homogeneities. In addition, it is worthwhile to mention that the SPAN/(311)A GaAs sample is of higher quality than the SPAN/(100) GaAs device due to their electrical properties and barrier homogeneities. For that reason, the orientation of the substrate and the thickness of the polymers considerably affect the barrier inhomogeneities and electrical characterization of the heterostructures.

To further investigate the impact of n-type GaAs substrate orientation on the electrical characterization of the SPAN/n-type GaAs sample, $E_a$ was determined from the experimental $J$−$V$ characteristics. The minimum energy required for a reaction to occur is called an activation energy. When the current is directly proportional to the number of carriers that enable to climb an energy barrier of $E_a$ and when the thermal energy of the carriers can be determined by the Boltzmann law, this is the physical meaning of the activation energy [37]. The temperature dependence of the activation energy at different temperatures can be described by the Arrhenius law; thus, the activation energy is calculated from Eq. (5);

$$ J = J_0 \exp \left( \frac{qV}{E_a} \right). \quad (5) $$

$E_a$ will be obtained by rewriting Eq. (5) as

$$ \ln J = \ln J_0 + \frac{qV}{E_a}. \quad (6) $$

From the above equation, $E_a$ can be expressed as

$$ E_a = \frac{qV}{\ln J}. \quad (7) $$

Figure 5 shows $E_a$ versus temperature for the SPAN/(100), (311)A, and (311)B n-type GaAs heterojunction devices, which were calculated from the slopes of the forward-bias $\ln J$ as a function of $V$ at different temperatures (see Figure 3). The value of $E_a$ for the SPAN/(100) n-type GaAs device changed from $3.55 \times 10^2$ eV at 60 K to $4.3 \times 10^2$ eV at 360 K. For SPAN grown on the (311)A n-type GaAs substrate, this value varied from $2.9 \times 10^2$ to $3.6 \times 10^2$ eV for the identical temperature scope. For SPAN grown on the (311)B n-type GaAs substrate, the change from $2.6 \times 10^2$ to $3.1 \times 10^2$ eV for SPAN/(100) n-type GaAs, $3.3 \times 10^2$ eV for SPAN/(311)A n-type GaAs, and $3.1 \times 10^2$ eV for SPAN/(311)B n-type GaAs sample is closest to the ideal state and better than the value observed by Jameel et al. [24], as exhibited in Table 1. The ideality factors of the heterojunctions studied in this research were greater than unity ($n > 1$). The large ideality factor is associated with the existence of a bias dependent Schottky barrier height [36]. The recombination current process at the SPAN/n-GaAs interface, the potential decline in the interfacial layer, and the existence of additional current can be factors for the larger values of $n$ [24].

![Figure 5: Temperature dependence of the activation energy in the temperature range of 60–360 K at a 20-K interval for the SPAN/(100) n-type GaAs, SPAN/(311)A n-type GaAs, and SPAN/(311)B n-type GaAs hybrid devices.](image-url)
GaAs. It can be seen from Figure 5 that the activation energy reveals substantially temperature reliance, that is the value of $E_a$ increases with the increase of the temperature for three samples, which is a similar behavior to that of other disordered materials [38]. Clearly, as noted from the same figure, the activation energies of the SPAN/(311)B n-type GaAs device are lower than the other two devices.

Experimentally, it has been noticed that an increase of the temperature by 20 K generally gives a double or triple rate of a reaction between molecules. The increase in temperature results an increase in the energy levels of the molecules involved in the reaction, therefore, the rate of the reaction increases. Likewise, the rate of the reaction will decrease with decreasing temperature. It is worth pointing out that the lower activation energies for the SPAN/(311)B n-type GaAs sample is a verification of their outstanding electrical properties once they are compared with both SPAN/(100) and (311)A n-type GaAs heterostructures. It is worthwhile to mention that the electrical characteristics of SPAN grown on (311)A n-type GaAs orientation is better than those of the hybrid devices. Moreover, the crystallographic orientation of the substrates has a remarkable impact on the electrical characteristics of the hybrid devices.

IV. CONCLUSION

To summarize, the electrical properties of conducting polymer SPAN grown on the n-type GaAs substrates with various orientation, namely, (100), (311)A, and (311)B, were investigated. The $J-V$ properties of all three devices revealed that the rectification ($J_{on}/J_{off}$) value at 300 K and $\pm0.5$ V for the SPAN samples fabricated on (311)B n-type GaAs is higher than the devices grown on the (100) n-type GaAs and (311)A n-type GaAs planes. Moreover, lower $n$ and higher $\Phi_0$ values for the SPAN/(311)B n-type GaAs device probably related to uniformity of the interfacial charges, less impurities, and less barrier inhomogeneity in comparison with those in the SPAN/(100) n-type GaAs and SPAN/(311)A n-type GaAs heterostructure devices. In addition, the lower values of $E_a$ in SPAN grown on (311)B n-type GaAs could be attributed to the lower number of defects than in the SPAN/(100) and (311)A GaAs samples. This certifies that the substrate orientation of GaAs has a considerable impact on integration of defects and consequently on the electrical characteristics of SPAN grown on n-type GaAs substrates. Other studies on organic semiconductors grown on identical crystallographic orientation of the n-type GaAs substrate have as well highlighted that the high index planes have a significant role to improve the electrical properties of the devices. Thus, it is obvious from the current study that the electrical characteristics of SPAN (120 nm) fabricated on (311) n-type GaAs, especially of SPAN (120 nm)/(311)B n-type GaAs, are better than SPAN (120 nm) grown on the (100) GaAs and SPAN (200 nm) grown on (100), (311)A, and (311)B, which were investigated by Jameel et al. [24]. Consequently, these new results confirm that the quality of conducting polymer/n-type GaAs heterojunction samples would strongly depend on the GaAs planes and the thickness of conducting polymer (SPAN).

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