Measurement-free error correction with coherent ancillas

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We show that coherent error correction with redundant syndrome extraction is feasible even when realistic error models for the ancilla qubits are used. This is done by means of a fault-tolerant circuit that has a favorable error threshold for a conservative error model. It is optimal when Toffoli gates are available, as they are in many implementations. The possibility of coherent error correction is important for those quantum computing platforms in which measurements in the course of the computation are undesirable.

I. INTRODUCTION

Future large scale quantum computers based on existing qubits will require quantum error correction. The actual error correction protocol depends strongly on the platform used. For some implementations, measurement during the course of a computation is not advisable. For example, in neutral atom quantum computation the measurement time is much longer than other gate times and crosstalk due to light scattering in the course of the measurement is difficult to control. For spin qubits in semiconductors, long measurement times also make traditional quantum error correction less appealing. There is a known solution to this problem, which is coherent error correction (CEC). CEC protocols do not require measurements to detect errors. Instead the error information is transferred to ancilla qubits during a syndrome detection cycle, and this quantum information is then used for correction using conditional gates. The ancillas are then reset, which flushes the entropy from the computer. Generally speaking, the overhead involved in fault-tolerant CEC has been thought to be greater than in fault-tolerant measurement-based error correction (MEC). A recent calculation suggested that this may not be the case, which would make neutral-atom and electron-spin implementations more attractive.

However, the calculation in Ref. along these lines used an error model that is not appropriate for the envisioned applications. It did not allow for phase-flip errors on the ancilla qubits. Such phase errors will certainly occur and should be given finite probability. In fact, we show below that the circuit used in Ref. is actually not fault-tolerant when these errors are included, i.e., there is no error threshold. It is also shown, however, that a modified circuit is fault-tolerant when all errors are given reasonable probabilities. This circuit retains the innovative feature of redundant syndrome extraction. We calculate the threshold and show that it is somewhat smaller than in Ref., but still favorable.

II. CIRCUIT DESIGN

The error-correction circuit from Ref. is shown in Fig. 1. Data qubits are in the top half and ancillas on the bottom. The circuit is based on the Steane 7-qubit error correction code but there are two major differences. The first is that ancillas are used to detect the error, as is standard in CEC. The second is that there is redundancy in the set of stabilizer operators associated with the code. That is, instead of the usual 6 operators that are usually measured for syndrome extraction, 14 diagnostic results are encoded in the ancillas. This redundancy builds fault tolerance into the circuit, obviating the need for repetition of the syndrome extraction.

If phase errors on the ancillas are included then we can get back-action on the data qubits by a well-known mechanism. This is shown in Fig. 1, where a phase error on the 1st ancilla (the blue Z) produces data errors in the data qubits that ultimately result in a logical error at the end, indicated by the 3 red X’s at the top right of the figure. Thus the phase errors spread through the computer, rendering it faulty: the probability of a logical error is linearly proportional to the probability of a phase-flip error on the ancillas. We calculate this probability below.

To identify the single qubit errors that destroy the fault tolerance of the previously proposed circuit we must consider the correction procedure for both bit- and phase-flip type errors. While simulations of CSS codes typically take advantage of the natural division of the stabilizer group into multiqubit Pauli X and Z operators, doing so would blind us to the crucial fault of this implementation. When a phase error happens on an ancilla qubit halfway through a stabilizer measurement, the entangling gates propagate two phase errors into the data register. These are rotated into bit-flip errors by the time the circuit attempts to correct the errors. As the stabilizers form a group, these two errors together are interpreted as a third: the bitwise sum of the two syndrome strings of the propagated phase errors is equal to the syndrome of another, and therefore the circuit erroneously corrects a qubit which had no error, and we have a fatal logical error. After identifying the dangerous errors, we can proceed to reconfigure the circuit to avoid them.
FIG. 1. (color online) The coherent error correction circuit with redundant stabilizer extraction proposed in Ref. [6]. Moving from left to right, the first quarter of the circuit extracts syndromes for bit flip errors, the second quarter corrects them, while the third and fourth do the same for phase errors. This circuit is not fault tolerant when phase errors on the ancilla qubits are included. An example of a single phase error (blue Z) in the ancilla block propagating (red X’s) to a logical error at the end is shown. \( R \) gates reset the ancilla qubits to \( |0\rangle \).

To do this we must insist that there is no way for an error to happen during the syndrome extraction for a single stabilizer element. By using a textbook circuit identity, we can re-order the gates and flip the role of target and control qubits during extraction to ensure this. The problem, though not the solution, is somewhat similar to “hook” errors [10].

In Fig. 2, we introduce a new circuit that does not allow phase errors to propagate and produce logical errors. It retains the important feature of redundant syndrome extraction. The crucial operational change is to use the ancillas as the control qubits for \( C_k \) NOT (Toffoli) gates rather than the data qubits. With this circuit design, any errors that happen in the syndrome extraction do not spread because the syndrome information for each stabilizer is extracted in a single time step. This step does introduce errors in the data qubits and joint errors in a data qubit and the appropriate ancilla. The point, however, is that these errors are controlled by the redundancy - multiqubit errors are still possible, but all of them lie within the stabilizer group. Hence they do not destroy fault tolerance.

III. RESULTS

We test these ideas with a sequence of 3 simulations and calculations. With the exception of the inclusion of the ancilla phase errors, the details of the error model used in the simulations are the same as in Ref. [6]. In particular, we take the gate error rate to be the same as the memory or “idle” error rate, both denoted by \( p \). The results are presented in Fig. 3. For each, the logical error probability \( p_{\text{log}} \) is plotted against the physical error probability \( p \).

1. For comparison to earlier results, we simulate the circuit in Fig. 1 allowing only bit flip errors on the ancillas. This means treating them as essentially classical, as was done in Ref. [6]. We find a threshold value of about \( 6 \times 10^{-5} \) but we stress once more that this is not a physically realistic model. This is the green curve, shown together with a fit, in Fig. 3. The threshold occurs when the curve crosses the dashed line that represents the equation \( p = p_{\text{log}} \).

2. We simulate the circuit in Fig. 1 allowing bit flip and phase flip errors and we calculate the logical error rate by counting the error sites between the first and second pair of CNOT gates on each ancilla qubit. A fraction of these errors involve a phase flip. Two of the three single qubit errors and eight of the 15 two-qubit errors result in logical errors. This gives a prediction for the logical error rate as a function of the physical error rate. If the dangerous memory and gate error sites are \( N_m \) and \( N_g \) we can estimate that

\[
p_{\text{log}}(p) = \left( N_m \times \frac{2}{3} + N_g \times \frac{8}{15} \right) p + O(p^2) \approx 11.73 \, p.
\]

This form fits the simulations well. The data and the fit are the red curve in Fig.3. Note that it does not intersect the dashed line, indicating that there is no threshold: the circuit is not fault tolerant.

3. We simulate the revised circuit of Fig.2 allowing for both flip and phase errors on the ancillas. The results and a fit are shown as the blue curve in Fig. 3. (It lies very close to the green curve.) There is a threshold, which we compute to be about \( 5 \times 10^{-5} \). This means that the revised circuit is indeed fault tolerant with a realistic error model.

This work shows that CEC can be performed with thresholds that are comparable to those of MEC. It is important to use redundancy in the syndrome extraction. This increases the threshold. We have assumed
FIG. 2. (color online) Revised circuit that avoids logical errors due to back-action by extracting each stabilizer to an ancilla in a single time step. The main change from the circuit of Fig. 1 is the reversal of the roles of data qubits and ancilla qubits in the extraction process. This circuit is fault tolerant even in the presence of phase errors on the ancilla qubits.

FIG. 3. (color online) Data and fits for three simulations. The dashed line represents $p_{\log} = p$. The green curve and points represent the results for the circuit in Fig. 1 without allowing for phase errors on ancilla qubits. There is a threshold of about $6 \times 10^{-5}$. The circuit is fault tolerant but the error model is not realistic. The red curve and points represent the results for the circuit in Fig. 1 allowing for phase errors on ancilla qubits. There is no threshold, since the curve does not intersect the dashed line. The circuit is not fault tolerant with this more realistic error model. The blue curve and points represent the results for the circuit in Fig. 2 allowing for phase errors on ancilla qubits. There is a threshold of about $5 \times 10^{-5}$. The circuit is fault tolerant with a realistic error model.

in this work that there is a native C$_k$NOT gate available. This is likely to be the case in, for example, neutral atom set-ups, where such gates have been demonstrated [11]. If only strictly 2-qubit gates are used, then the C$_k$NOTs used in the syndrome extraction can be replaced by CNOT gates at the cost of $k - 1$ additional ancillas per extraction [12]. This modification would not destroy the fault-tolerant nature of the circuit. However, it would involve a considerable number of additional qubits.

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