DYNAMAP: Dynamic Algorithm Mapping Framework for Low Latency CNN Inference

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ABSTRACT

Most of the existing work on FPGA acceleration of Convolutional Neural Network (CNN) focus on employing a single strategy (algorithm, dataflow, etc.) across all the layers. Such an approach does not achieve optimal latency on complex and deep CNNs. Emerging CNNs have diverse per-layer computation characteristics including parallelism, arithmetic intensity, locality, and memory footprint. Per-layer strategy selection and fine-grained tuning is required to achieve low end-to-end latency. However, specialized hardware modules dedicated for each layer limit the per-layer utilization and adversely affect end-to-end latency. In this paper, we address these problems by an algorithm-architecture co-optimization framework, DYNAMAP, consisting of (1) a unified hardware overlay that can be reused across layers, supporting dynamic mapping of all three families of popular convolution algorithms, and further allowing flexible dataflow switching to maximize hardware utilization for each layer; (2) a novel software Design Space Exploration (DSE) flow that customizes the hardware overlay and chooses optimal strategy mapping. We show that the algorithm mapping space increases exponentially with network depth, and while the optimal algorithm selection problem is NP-hard in general, by exploiting the series-parallel structure of CNN models, we demonstrate a polynomial-time solution for optimal algorithm mapping. DYNAMAP is optimized for any CNN, including those having diverse computation and memory requirements across the layers. We demonstrate DYNAMAP using two state-of-the-art CNNs - GoogleNet and Inception-V4. The generated accelerators achieve up to 2.8× and 1.4× speedups, respectively, wrt inference latency compared with the state-of-the-art FPGA implementations.

1 INTRODUCTION

CNNs are powerful techniques used in many computer vision related machine learning tasks spanning from image and video processing to automatic learning of agents in robotics and games. Recently, new families of CNNs featuring various convolution (CONV) layers [7, 20, 21] have been developed. These CNNs show superior performance wrt prediction accuracy while introducing new convolution operations (e.g. depthwise CONV in MobileNet, “Fire” module in SqueezeNet, 1×7 filter in “Inception module”). As CNNs continue to be more compute- and memory-intensive, FPGAs become promising candidates for CNN inference implementation with superior latency and reduced energy consumption. To avoid expensive run-time reconfiguration, most existing FPGA-based solutions usually use a specific algorithm across all the layers and reuse a generic architecture to speed up the algorithm [13, 14, 26, 28, 30]. These approaches leave some performance and hardware efficiency on the table due to (1) use of a fixed algorithm across diverse layers and (2) under-utilization due to fixed hardware. This situation is compounded since state-of-the-art CNNs have more diverse layer shapes and complex structures, resulting in sub-optimal latency.

Many algorithms have been proposed to optimize various types of CONV operations, such as GEMM (General Matrix-Matrix Multiplication) based methods (im2col [2], kn2row [23], Winograd-fast matrix multiplication [10]) and frequency-domain methods [24]. DYNAMAP is primarily motivated by the possibility of bridging the performance gap between the widely used “one size fits all” design methodology and an ideal design methodology where dedicated layer-wise algorithm tuning is performed to realize low end-to-end latency and maximal hardware-reuse across layers. To achieve this goal, this paper explores dynamic algorithm mapping for various layers using a domain specific architecture that can support all the GEMM-based CONV algorithms.

Different algorithmic approaches and layer configurations introduce different trade-offs wrt parallelism, memory requirements and data layout which can easily cause hardware under-utilization. Deeper and increasingly complex CNN models lead to exponential explosion of algorithm design space. For example, GoogleNet has 22 CONV layers. Assuming each layer can be implemented with 3 algorithm choices, this leads to an algorithm mapping space of over 30 billion (3^{22}) combinatorial choices. It is non-trivial effort to decide which algorithm mapping is the best for a given CNN model.
on a given assignment problem naturally maps to Partitioned Boolean Quadratic Programming (PBQP) [16] optimization problem, which is NP-hard in its general form. To address the challenge of hardware-under-utilization, we apply dataflow optimization to minimize wasted computation. To achieve fast optimal algorithm mapping, we propose a polynomial-time solution taking advantage of the series-parallel graph structure of CNNs. These are integrated into DYNAMAP, which takes as inputs (a) the CNN model parameters (input and kernel shapes, stride sizes) (b) the set of algorithms, and (c) FPGA device meta data (DSP resources, on-chip memory size and external bandwidth). The outputs are algorithm selection for each layer and customized accelerator on the target device specified in Verilog.

Our main contributions are:

- A unified template hardware overlay re-used across layers with the following novel optimizations:
  - **Algorithm Switching**: We enable low-overhead layer-wise layout transformation, allowing dynamic switching of three popular GEMM-based CONV algorithms: im2col, kn2row and Winograd algorithms;
  - **Dataflow Optimization**: We optimize the Processing Elements (PE) design to support no-overhead switching between different dataflows to achieve maximum hardware utilization, enhanced with conflict-free memory latency;
  - **Accurate modeling of the computation and communication latency for various CONV algorithm combinations to allow easy construction of a parameterized dependency graph representation for any CNN models, capturing architectural parameters, FPGA device capabilities, and CNN meta data;
  - A framework, DYNAMAP, that proposes a 2-step DSE flow:
    - **Hardware Mapping**: Identifying the fixed architectural parameters as well as the most efficient dataflow for each layer under all algorithm settings;
    - **Algorithm Mapping**: Polynomial-time optimal algorithm selection exploiting the series-parallel characteristic of CNN graphs;
  - We evaluate the DYNAMAP-generated hardware design on a Xilinx Alveo U200 board. Our designs achieve up to 2.8x and 1.4x end-to-end latency improvements compared with state-of-the-art FPGA implementations on two recent deep complex-form CNNs - GoogleNet and Inception-V4.

## 2 BACKGROUND & MOTIVATION

### 2.1 GEMM-based Convolution

Convolution (CONV) layers are major building blocks of CNNs and their meta data are defined as follows: Each CONV layer has \( C_{\text{in}} \) \((C_{\text{out}})\) input (output) channels, where each channel is a \( H_1 \times H_2 \) \((O_1 \times O_2)\) 2D feature map. The layer weights \( W \) contain \( C_{\text{in}} \times C_{\text{out}} \) number of kernels, each sized at \( K_1 \times K_2 \). In this work, we focus on spatial convolution. Spatial convolution performs sliding window multiply-accumulate operation of the kernels over the feature maps. As CONV layers dominate the memory and computations in a CNN, a number of algorithms have been proposed for efficient implementation of convolution operation. Among these General-matrix-multiplication (GEMM) - based methods are most widely adopted [2, 10, 23] for spatial convolution. In this section, we summarize three families of popular GEMM-CONV algorithms and their trade-offs.

#### 2.1.1 im2col Method

im2col [2] is a popular algorithm that converts spatial convolution into GEMM. For a feed forward pass of a CONV layer:

\[
z_{x,y} = \sum_{x'} \sum_{y'} \sum_{w} w_{w,x',y'} x_{x',y'} (y+y')
\]

im2col stretches each group of \( C_{\text{in}} \) kernels into a row of the weight/kernel matrix, \( X \), and each group of \( C_{\text{in}} \) corresponding windows of input feature maps into a column of the input activation matrix, \( W \). Expressing the feed forward pass as:

\[
z_i = W_1(C_{\text{out}} \times K_1 K_2 C_{\text{in}}) \times X_i(C_{\text{in}} \times O_1 O_2)
\]

In the second phase, ‘Pad-and-Accumulate’, the intermediate output patches of all unit-convolutions, \( P_{k_1, k_2} \), are shifted by their offsets w.r.t. the center patch, padded with 0 on the non-overlapping areas and Hadamard-added to generate the final output feature maps:

\[
z_i = \sum_{k_1, k_2} P_{k_1, k_2} x_{x+(k_1-\frac{K_1}{2}), y+(k_2-\frac{K_2}{2})} + \frac{K_1}{2}, \frac{K_2}{2}
\]

#### 2.1.2 kn2row Method

The kn2row [23] method is based on the decomposition of convolutions and reordering the data layout. In the first phase, ‘unit-CONV GEMM’, a \( K_1 \times K_2 \) convolution is computed using \( K_1 K_2 \) separate \( 1 \times 1 \) unit-convolutions, which is equivalent to a GEMM call:

\[
P_{k_1, k_2} = W_1(C_{\text{out}} \times C_{\text{in}}) \times X_i(C_{\text{in}} \times O_1 O_2)
\]

In the second phase, ‘Pad-and-Accumulate’, the intermediate output patches of all unit-convolutions, \( P_{k_1, k_2} \), are shifted by their offsets w.r.t. the center patch, padded with 0 on the non-overlapping areas and Hadamard-added to generate the final output feature maps:

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z_i = \sum_{k_1, k_2} P_{k_1, k_2} x_{x+(k_1-\frac{K_1}{2}), y+(k_2-\frac{K_2}{2})} + \frac{K_1}{2}, \frac{K_2}{2}
\]

#### 2.1.3 Winograd Minimal Filtering Method

Winograd algorithm [10] is a fast matrix multiplication algorithm which reduces the number of operations in a GEMM call. A \( F(m \times m, r \times r) \) Winograd algorithm can generate output as Equation 5. In this equation, \( Y \) and \( d \) represent output and input tiles, while \( g \) represents kernels. \( A, G, \) and \( B \) are constant transforming matrices and \( \otimes \) represents Hadamard multiplication. Input feature map \( D \) is partitioned into multiple input tiles, \( d_i \), with size \( (m + r - 1) \times (m + r - 1) \) while adjacent tiles share an \( (r - 1) \) overlap. Each output tile size is \( m \times m \) and kernel size is \( r \times r \).

\[
Y = A^T \left[ G g G^T \otimes B^T B \right] A
\]

The final output feature map is calculated by concatenating all output tiles, \( Y \), and summing up over the depth of the input tensor. Equivalently, we can reduce over \( C_{\text{in}} \) channels in the transform space before applying the inverse transform \( A \) to the sum. This amortizes the cost of the inverse transform over the number of channels, and allows us to alternatively express the Hadamard products and depth-wise additions into \((m + r - 1) \times (m + r - 1)\) independent GEMMs [10]:

\[
M_d(\xi, \nu) = \sum_{x, y} u(x, y) v(x, y)
\]

where we label each single component of the tiled Hadamard multiplication separately, as \((\xi, \nu) \in [0, m + r - 1] \times [0, m + r - 1] \) and \( U \) and \( V \) represent the input and kernel tiles \( G g G^T \) and \( B^T B \), respectively; and the tuple \( (x, y) \) indicates the coordinate of the input tile corresponding to \( k^{th} \) kernel \( 0 < k \leq C_{\text{out}} \).
Trade-offs: While im2col has the same computation load as spatial convolution, it suffers from memory overhead due to input feature duplication, especially for large kernels and small stride sizes. kn2row is known as a low-memory algorithm because it eliminates the need to duplicate feature map elements by using $1 \times 1$ convolutions. However, it incurs extra overhead in the 'Pad-and-Accumulate' phase compared to im2col method. The advantage of Winograd CONV comes from the lower computation complexity. For example, an $F(4 \times 4, 3 \times 3)$ Winograd algorithm requires 36 multiplications for one output tile, while the Spatial CONV needs 144 multiplications. The reduction of multiplications is 4 times in this case. However, Winograd introduces memory overhead and extra additions due to the transformation in Equation 5.

2.2 Motivation
State-of-the-art CNNs [8, 20–22] have highly complex architectures with multiple branches and wide variations in CONV layer configurations. As illustrated in Figure 1, using three common layer configurations, relative performance of the three GEMM based convolution algorithms depends heavily on the layer configuration, Thus, using a single algorithm across all the layers is not an optimal strategy to minimize the latency of CNN inference. Rather, the ability to switch algorithms between layers is needed. Enabling efficient algorithm switching requires us to solve the following problem: (a) As wide variety of CONV configurations and convolution algorithms exist, a unified architecture which is general enough to execute all combinations, while, simultaneously supporting algorithm specific optimizations to extract maximum performance is needed (Section 3). (b) As each algorithm requires the input and produces the output in its own specific format a low overhead data re-ordering mechanism is needed (Section 3.3). (c) As state-of-the-art-CNNs are extremely deep with number of CONV layers easily surpassing 50 or 100 (Inception-v4 has 141 CONV layers), a low complexity algorithm, which can handle the exponential combinatorial explosion in design choices ($3^{141}$ for Inception-v4) is needed to determine optimal algorithm for each layer (Section 4).

We solve the problems mentioned above and present DYNAMAP — a framework that takes any CNN model and maps it onto FPGA in order to obtain extremely low latency CNN inference (Section 5).

2.3 Related Work
[11, 14] developed efficient FPGA accelerators for Winograd CONV expressed as hadamard multiplication between input tiles. [13, 28, 29] focus on frequency-domain CNN acceleration which are usually advantageous for large kernels. [30] used kn2row and achieved state-of-the-art speedup on Inception v-4 which has more memory-bound layers. While these works adopt certain strategies to accelerate CNN inference, they do not explore the flexible switching of different algorithms within the same network.

[26] proposed a hls-implemented accelerator that allows switching between Winograd and Spatial CONV, achieving high-throughput inference on VGG-16. However, their design is not optimized for more memory-bound CONV layers such as those in Googlenet, mobilenet, Resnet and Inception networks. [33] proposed to combine fast convolution algorithms including Winograd and Fast Fourier Transform by developing separate modules for the two strategies and partition the resource for different layers executing each; [32] explores a hardware DSE scheme that allocates resources to a generic module that accelerate majority of the layers and specific modules heavily customized and dedicated to certain types of layers. While these works exploit fine-grained layer specific tuning, their designs do not maximally re-use the available resource when executing no-batch inference. This is because the dependencies in CNN graph leads to idling of these specific modules when single image inference needs to be performed. [3] proposes a polynomial-time heuristic to a general module selection problem for streaming applications. While this approach focuses on throughput-area tradeoff fitting multiple operators where module circuit implementations are selected(mapped) to each operator, it does not capture CNN-specific algorithm choices such as im2col, kn2row and Winograd to CONV operators(layers). In contrast, we exploit maximal circuit-reuse across different layers and map different algorithms to layers for low-latency CNN inference. To exploit both layer-wise fine-tuning and hardware utilization, we take a different approach than the existing works - We define a unified computing unit that is general enough to execute all layer-algorithm combinations, while, simultaneously supports algorithm switching and algorithm-specific optimizations for maximum performance.

3 ARCHITECTURE OVERLAY DESIGN FOR DYNAMIC ALGORITHM SWITCHING

We develop a unified architecture template with a shared central Computing Unit which can be used by all the supported algorithms and separate algorithm-specific auxiliary functional modules. To address the challenges of: (a) hardware under-utilization due to different layer-specific parallelism requirements and (b) algorithm
switching overhead, we propose the following optimizations, respectively: (a) a novel PE design that enables stall free computations between layers and enables selection of algorithm specific optimal systolic array dataflow to extract maximum parallelism in GEMM operations (Section 3.2), (b) a low overhead data layout transformation module to enable fast algorithm switching between layers (Section 3.3).

3.1 Architecture Overview
Figure 2 shows a high-level overview of the template architecture design. The accelerator is composed of a GEMM Computing Unit performing, Linear Transform Modules for Winograd, a Pad-and-Accumulation Module for kn2row, Data Layout Transformation (DLT) Modules for data re-ordering when switching between different layers and algorithms, and a Pooling Module for max pooling on spatial feature maps. The Computing Unit (CU) is a \( P_{SA1} \times P_{SA2} \) 2-D systolic array of Multiply-Accumulation (MAC) units optimized for GEMM. The Input Buffer and Kernel Buffer are organized into \( P_{SA1} \) and \( P_{SA2} \) banks, respectively. Each bank stores a partition of input feature/kernel matrix. During GEMM execution, \( P_{SA1} \) and \( P_{SA2} \) data elements are read concurrently by parallel PEs in the systolic array, and written to \( P_{SA1} \) or \( P_{SA2} \) banks of output buffer in parallel.

Under im2col mode, the Toeplitz matrices of input feature maps and kernel parameters are loaded into the Input and Kernel Buffers. The output feature maps are directly written into the output buffer.

Under kn2row mode, the independent \( 1 \times 1 \) unit convolutions are expressed as a series of GEMM calls. Then Pad-and-Accumulate Module shifts each intermediate output patch to align with the position determined by the original \( K_1 \times K_2 \) kernel and produces the final output feature maps using an accumulation buffer. The bank indices and address offsets for Pad-and-Accumulate are pre-computed based on CONV layer meta data [30]. The “unit-CONV GEMM” and “Pad-and-Accumulate” phases are pipelined enabling CU to start working on the next patch of unit-CONV GEMM while accumulation buffer still processes the last patch. This reduces the overall “Pad-and-Accumulate” overhead of kn2row.

Under Winograd mode, both input feature maps and kernels are fed into the Linear Transformation Modules so that the GEMM operates in Winograd-transformed space. Each of \((m+r-1) \times (m+r-1)\) input feature map tile (overlapped by \( r-1 \) in adjacent tiles) and \( r \times r \) kernel tile are transformed into a \((m+r-1) \times (m+r-1)\) sized tile. All the tiles are scattered and reordered into \((m+r-1) \times (m+r-1)\) independent input and kernel matrices [10] sized at \((\frac{P_{SA1}}{m} \times \frac{P_{SA1}}{m}, C_{in})\) and \(C_{in}, C_{out}\), respectively. These GEMMs are fed into the systolic array sequentially and the output is again multiplied with transformation matrices to recover the output tensor shape \((O_1 \times O_2, C_{out})\). Linear Transform Module requires multiplication by constants and additions which are determined by Winograd hyper-parameters \((m, r)\). For instance, in a \( F(2,3) \), the transformation matrices are only composed of values of \( \pm 1 \) and \( \pm \frac{1}{2} \), which can be easily implemented using shift and add operations.

3.2 Dataflow-switchable & Stall-free PE design
Performance of GEMM on a fixed systolic array heavily depends upon the dimension chosen for parallelism. For example, consider a \( 31 \times 31 \) systolic array size for multiplying input matrices of sizes \((a, b), (b, c) = (62, 124), (124, 64)\). Parallelizing along dimensions \( a, c \) and breaking each input matrix into tiles sized at \((124, 31)\) and \((124, 31)\), respectively, will require extensive zero padding in the last tile which will have only 2 columns along dimension \( c \). The effective PE utilization will only be 68%. However, if we parallelize along dimension \( a, b \) instead, no under-utilization will occur.

To handle such scenarios, we develop a novel PE design that allows for no-overhead switching between different dataflow to improve PE utilization. 

Non-stationary (NS) Dataflow: The input matrices \( W(b \times c) \) and \( X(a \times b) \) are partitioned along dimensions \( a \) or \( c \) into tiles of size \( b \times P_{SA1} \) (or \( P_{SA2} \)). Each Processing Element (PE) computes a vector-product that contributes to one output feature. In each clock cycle each PE performs one multiply-accumulation (MAC) and shifts the input and weight along two directions. Once all the MAC computations for a pixel are finished, the final result is shifted out of the PE and the PE proceeds to work on a new pixel. The NS datapath in a PE is shown in Figure 3 with black and red-colored wires. Each pass of matrix partitions incurs an initialization overhead \( I_{SA} \) that is proportional to \( \max(P_{SA1}, P_{SA2}) \) and in a naive implementation will be incurred for each pass in each layer. We alleviate these overheads to implement stall-free GEMM as follows (Figure 3): MUX highlighted in grey selects between shifting accumulation result of \( P_{EX,y} \) and other PEs. When one PE completes the dot product for one pixel, the accumulation result is directly shifted out, and during the computation of the next PE, accumulation results of other PEs can be shifted concurrently such that \( I_{SA} \) is overlapped with next-pass computation. To further avoid additional stalls due to accumulation result congestion between passes when \( b < P_{SA} \) (commonly occurs in layers with small filter and shallow feature maps), we widen the wire(s) used to shift down accumulation results by \( \frac{1}{\text{pass}} \) for PEs at the \( j^{th} \) row. This ensures that the rate at which outputs are shifted out of each PE matches the rate at which outputs are generated. 

Weight-Stationary (WS) Dataflow: In WS, in each pass, the PEs pre-load a (stationary) block of the weight/kernel matrix sized at \( P_{SA1} \times P_{SA2} \) into their local registers. Then the input matrix is fed as tiles of size \( P_{SA1} \times a \) into the systolic array in a pipelined fashion. In each clock cycle each PE performs a MAC operation, shifting the input to the next neighbor along \( P_{SA1} \) direction and shifting the partial result down to accumulate the partial sums. Each \( \frac{b}{P_{SA1}} \) pass produces an intermediate
in each pass the PEs pre-load a (stationary) block of the input
Transformation (DLT) Module to achieve layout transformation
(produces output in a specific layout. We design the Data Layout
Module to achieve layout transformation.

\[
WS: \text{in each pass the PEs pre-load a (stationary) block of the input}
\]

Each algorithm — im2col, kn2row and Winograd requires input and
produces output in a specific layout. We design the Data Layout
Transformation (DLT) Module to achieve layout transformation
on-the-fly with minimal overheads. At data-store (data-load) side,
DLT module streams in the [on-chip SRAM (DRAM) address, data] tuples,
converts the output layout of the previous layer into the correct input tensor layout for the algorithm implemented in the
following layer, generates the [DRAM (on-chip SRAM) address, data] tuples and stream out to the DDR controller. As the DLT at
data-load side performs symmetric operations as that at data-store side with flipped on-chip SRAM / DRAM address tuples, we only
show the transformation scheme for data-store side.

While all three algorithms have different layout for the input tensor shape, im2col and kn2row outputs the intermediate feature map in the same layout - spatial 3D tensor layout. Therefore
the DLT Module selects from one of six available combinations
for layout conversion. When both layers use kn2row algorithm, the output layout is the same (3D tensor) as the next input layout.
In this case, the transformation is simply a one-to-one matching
between consecutive on-chip SRAM and DRAM addresses. We list
the other conversions below:

**Table 1: Tensor Layout transformations**

| Transformation          | 3D Tensor → Toeplitz | 3D Tensor → Winograd | Winograd → 3D Tensor |
|-------------------------|----------------------|----------------------|----------------------|
| \( O \)                  | \( S \)               | \( H_{1} \)          | \( H_{1} \)          |
| \( P_{SA1} \times m \)  | \( P_{SA2} \times m \) | \( m \times k \)     | \( m \times n \)     |
| \( K_{1} \)              | \( H_{1} \)           | \( k \)              | \( k \)              |
| \( K_{2} \)              | \( m \times n \)      | \( m \times n \)     | \( m \times n \)     |
| \( K_{3} \)              | \( m \times n \)      | \( m \times n \)     | \( m \times n \)     |
| \( H_{1} \)              | \( m \times n \)      | \( m \times n \)     | \( m \times n \)     |
| \( H_{2} \)              | \( m \times n \)      | \( m \times n \)     | \( m \times n \)     |

\[ x = (i + j) \% P_{SA1} \]
\[ y = \frac{i \times P_{SA2}}{P_{SA1} - P_{SA2}} \]

\[ (7) \]

3.3 Data Layout Transformation Module

Each algorithm — im2col, kn2row and Winograd requires input and
produces output in a specific layout. We design the Data Layout
Transformation (DLT) Module to achieve layout transformation
array dimensions and store the blocks in a circular-shifted manner.
Equation 7 shows the mapping between feature block \((i, j)\) and its location \((\text{Bank}_x, \text{Block}_y)\) in on-chip SRAM. Using such bank
layout we ensure single-cycle parallel access in both directions can
be achieved without bank conflicts.

\[ x = (i + j) \% P_{SA1} \]
\[ y = \frac{i \times P_{SA2}}{P_{SA1} - P_{SA2}} \]

\[ (7) \]

3.3.1 3D Tensor Layout Transformations. The input layout for
im2col is known as the Toeplitz matrix, where each group of \( C_{in} \)
windows of input feature maps corresponding to a filter size is
stretched into a column of the Toeplitz matrix, sized at \((O_1 O_2, K^2 C_{in})\).
We define the output layout of im2col and kn2row as spatial 3D Tensor
Layout, which is a matrix of shape \((H_1 H_2, C_{in})\). Figure 5 shows a high-level Finite-State Machine diagram of the mechanism
adopted in a Layout Transformation Unit (LTU) implementing the
transformations, where \(B, D\) represent the on-chip SRAM and DDR
addresses corresponding to a data point in the feature map. Incrementing \(B\) by 1 (or \(H + S\)) means jumping to the address of
the adjacent data (or data at distance of \(S\) rows) in the original feature
map in on-chip SRAM to obtain a new tuple, and incrementing \(D\) by
1 means setting the next consecutive address as write-back address.
The generated (DDR address, data) tuples are buffered until DDR
transfer burst length (BL) is saturated, and are then sent to DDR.

**Figure 5: LTU (Data-Store side): FSM flow**
interface. \( \text{Iter}_x \) denotes the counters that keep track of the number of times state \( x \) is visited. The process for transforming a 3D Tensor output to a Toeplitz input is shown in Table 1 first row, state 2 loops inside each row (length \( K_1 \)) of sliding window, state 3 iterates all \( K_2 \) rows in a sliding window and state 1 steps over all overlapped sliding windows.

3.3.2 Winograd Layout Transformation. In Winograd Input Tensor Layout, \( \frac{H_4}{m} \) input feature tiles (each sized at \( (m + r - 1)^2 \)) are stretched into rows and adjacent tiles share an overlap with width of \( r - 1 \). As each tile sized at \( (m + r - 1)^2 \) is initially scattered to \( (m + r - 1)^2 \) different matrices for separate matrix multiplications [10], \( \frac{H_4}{m} \) elements corresponding to the same relative position in each overlapping tile should be adjacent in on-chip SRAM. When transforming from 3D tensor layout to Winograd input Layout (Table 1 row 2). Consistently, in the Winograd output Tensor Layout, the \( m^2 \) elements of each output tile are scattered to locations spaced out at \( \frac{H_4}{m} \) horizontally or \( \frac{m}{H_4} \) vertically, and \( \frac{H_4}{m} \) elements from different tiles are adjacent in the Output Buffer. Therefore, to transform from Winograd output layout to Toeplitz layout, we first need to restore the 3D Tensor layout (Table 1 row 3), then transform to Toeplitz input layout using row 2 configurations. To avoid extra roundtrip to DRAM, we double-buffer the Output Buffer into two bank groups, where the systolic array writes to bank group A, LTU #1 transforms 3D Tensor and writes into bank group B, while LTU #2 takes input from bank group B and writes into DRAM.

3.4 Pooling

MaxPool and AvgPool are the most common Pooling layers. To avoid expensive data traffic between the host processor and FPGA, we allocate dedicated hardware module for MaxPool, and express AvgPool of window \( K_1 \times K_2 \) as equivalent to a 2D convolution with a \( K_1 \times K_2 \) kernel where each element is of value \( \frac{1}{K_1 K_2} \). The hardware building block for the MaxPool module are the Pooling Units (PU). Each PU contains a Horizontal PU (HPU) to read data from input feature map horizontally in a pipelined manner. The HPU outputs one intermediate Pooling result each clock cycle. After HPU produces \( K_1 \) rows of intermediate Pooling results, the Vertical PU (VPU) with the same architecture starts processing in the vertical direction, producing one Pooling result each clock cycle, overlapping the HPU in a pipelined fashion. We use an array of PUs to exploit parallelism across feature maps.

4 OPTIMIZATION FORMULATION FOR ALGORITHM MAPPING

Given a graph representation of a CNN model and the target FPGA platform, we need to determine the following: (a) For each layer, the choice of the convolution algorithm and the choice of the dataflow. We call this algorithm-dataflow pair. (b) parameters to customize architecture overlay for the CNN model on the target platform. We discuss (a) in this section, and (b) in Section 5. Note that as optimal dataflow for each algorithm in each layer can be determined in step (b), algorithm mapping here implicitly implies algorithm-dataflow pair mapping.

As described in Section 3.3, the choice of algorithm-dataflow pair not only impacts the execution time of the layer, it also impacts the execution time of all the neighboring layers as represented by the edges in the graph \( G \). This is because data layout transformations are needed to ensure data is available to the algorithms in the correct format. Thus, greedily selecting algorithm-dataflow pairs that minimize the execution time at each layer will not minimize the overall execution time of the CNN.

We assume the CNN graph is \( G = (V, E, C, T_e) \), with each vertex \( v \in V \) representing a layer of the model and each edge \( e \in E \) representing the ordering between two layers. Let vertices be labelled \( 1, \ldots, N \), where \( N = |V| \). \( C_o \) is the cost vector array that represents the computation costs of the vertices (Section 5.1.1) under different algorithm-dataflow pairs. For vertex \( i \), \( \bar{c}_i \) denotes the cost vector. \( T_e \) is the set of transition cost matrices that represent the cost of data layout transformation between vertices (Section 5.1.2). \( T_{ij} \) denotes transition matrix for each edge \( (i, j) \). The objective is to determine algorithm-dataflow mapping for each layer of CNN such that the cost — total latency of executing the CNN is minimized. \( \bar{x}_j \) is a 0-1 assignment vector with \( \bar{x}_j(k) = 1 \) if algorithm \( k \) is chosen and 0 otherwise. Exactly one entry of \( \bar{x}_j \) can be set to 1. The problem can be formulated as follows:

\[
\text{minimize } \sum_{1 \leq i < j \leq N} \bar{x}_i^T T_{ij} \bar{x}_j + \sum_{1 \leq i \leq N} \bar{x}_i^T \bar{c}_i \\
\text{s.t. } \bar{x}_i \in \{0,1\}^{|\bar{c}_i|}, \quad \forall 1 \leq i \leq N \\
||\bar{x}_i||_1 = 1
\] (8)

This problem formulation is known as Partitioned Boolean Quadratic Programming (PBQP) problem [16]. PBQP has been used to model a number of problems in compiler optimization such as register allocation for architectures with irregular instruction sets [16], and instruction selection on DAGs [5].

PBQP is NP-Complete [1, 16]. However, we show that for a class of graphs, known as series-parallel graphs, PBQP can be solved in polynomial time. Moreover, we show that the graphs of a majority of popular CNN architectures fall into this class. This allows us to develop a polynomial time optimal algorithm for the algorithm mapping optimization problem defined above.

Definition 1: A (undirected) graph, with two distinguished vertices — source \( s \) and sink \( t \), is a series-parallel graph if it can be turned into a \( K_2 \) graph (a graph with two vertices connected with an edge) by a sequence of the following operations [4]:

1. Remove a degree 2 vertex other than \( s \) or \( t \) and the edges incident on it. Directly connect the two neighbors with a single edge.
2. Replace a pair of parallel edges with a single edge that connects the two endpoint vertices.

Theorem 4.1. PBQP can be solved in polynomial time if the graph is a series parallel graph. Moreover, for a graph with \( N \) vertices and \( d = \max[|\bar{c}_i|] \), the running time is \( O(Nd^2) \).

Theorem 4.2. On any series-parallel graph, reduction operations (1) and (2) preserves the optimality of PBQP.

Proof. We prove Theorem 4.1 and 4.2 by induction.

The inductive property is that any series-parallel graph can be constructed from a base \( K_2 \) Graph \((s, t)\), where \( s \) is its source and \( t \) is its sink, by a combination of the following two steps:
Base steps: (1) adding a vertex with an edge connected to $s$ or $t$ of the base K-2 Graph; (2) adding an edge between $s$ and $t$ of the base K-2 Graph;

Inductive steps: (1) adding a vertex with an edge connected to the source or sink of an existing series-parallel graph; (2) adding an edge between the source and sink of an existing series-parallel graph; Note that adding a degree-2 vertex connected to the source and sink of a K-2(or, series-parallel) graph $G_t$ is equivalent to performing Base(or, Inductive) step (1) followed by Inductive step (2) on $G_t$.

In the following, we prove that any series-parallel graph constructed this way can be reduced to a K-2 graph with preserved optimality.

Base Cases: (1) For a graph $G^1$ with three vertices $i, j, k$ and edges $(i, k), (j, k)$, the optimal solution is obtained by choosing algorithms ($d_k$) for vertex $k$ such that $d_k = \arg\min\{c_1(d_i) + c_1(d_j) + c_2(d_k) + \hat{c}_2(k,j, d_i, d_j)\}$ for all $(d_i, d_j)$ pairs in $G^1$. Applying operation 1 on vertex $k$ to obtain $K^1_2$ graph $G_k$ and setting $T_{ij}(d_i, d_j) = \min\{T_{ij}(k, d_i, d_j) + c_1(d_k) + \hat{c}_2(k,j, d_i, d_j)\}$ for all $(d_i, d_j)$ in $G_k$, the optimal solution on the reduced graph can be found by iterating through $(\hat{c}_1(d_i), \hat{c}_1(d_j))$ pairs. Thus, optimality is preserved.

(2) For a graph $G^1$ with two vertices $i, j$ and two parallel edges between vertices $(i, j)$ and $(i, j)^2$, the optimal solution is $\min\{\hat{c}_1(d_i) + T_{ij}^{(1)}(d_i, d_j) + T_{ij}^{(2)}(d_i, d_j)\}$, where $T^{(1)}$ and $T^{(2)}$ are matrices of the parallel edges. Applying operation 2 by updating $T_{ij}(d_i, d_j) = T_{ij}^{(1)}(d_i, d_j) + T_{ij}^{(2)}(d_i, d_j)$, the optimality is preserved.

Inductive Hypothesis: We assume that a subgraph, $G^S = (V^S, E^S)$, of a series-parallel graph, where $|V^S| = N, |E^S| = M$, can reduce to a $K^2$ graph with preserved optimality.

Inductive Cases: We show that a series-parallel graph $G = (V, E)$ constructed by adding a vertex/edge to $G^S$ specified above can still reduce to a $K^2$ graph with optimality preserved: (1) If $G(|V| = N + 1, |E| = M + 1)$ is constructed by adding a vertex, $k$, with an edge connected to the source $s$ or the sink $t$ of $G^S$ by an edge $(k, s)$ or $(k, t)$, the optimal solution can be obtained by treating $G^S$ as its reduced $K^2$ graph (due to Inductive Hypothesis). Assuming we connected $k$ to $t$, $G$ can be treated as having three vertices $s, t, k$ connected by two edges $(s, t), (t, k)$, which is reducible to $K^2$ graph with $s, k$ connected by an edge using the same method as shown in Base case: (1). (2) If $G(|V| = N, |E| = M + 1)$ is constructed by adding an edge, $(s, t)$, connecting a vertex $s$ or the sink $t$ of $G^S$, the optimal solution can be obtained by treating $G^S$ as its reduced $K^2$ graph (due to Inductive Hypothesis), therefore $G$ can be treated as having two vertices $(s, t)$ and two parallel edges, which is reducible to $K^2$ graph using the method shown in Base case: (2). Therefore any series-parallel graph can be reduced to a $K^2$ graph, preserving the optimality of the solution on the original graph. As described in the base cases, each reduction operation (1) or (2) requires $O(d^2)$ amount of work and is performed $O(N)$ times in total for a given graph.

We demonstrate the proof for the optimality-preserving reduction with a simple example in Figure 6, where we assume $N = 3, d = 2$ and $c_i = 0, 0 \leq i \leq d$.

Lemma 4.3. Resnet [6], VGG [17], Alexnet [9], etc. which do not have any branches are series parallel graphs.

![Figure 6: Sample Reduction Process](image)

Proof. Let the input layer be denoted by vertex $s$ and the output layer by vertex $t$. The degrees of vertices corresponding to all the other layers for VGG and Alexnet are 2. By repeatedly applying operation 1, we obtain a $K^2$ graph. In ResNet, some vertices have higher degrees due to skip connections. However, the vertices between the end points of each skip connection have degree 2. Thus, repeatedly applying operation 1 on these nodes until an edge parallel to the skip connection edge is obtained, and then applying operation 2 results in a graph with all vertices except $s$ and $t$, having degree 2. By repeatedly applying operation 1, we obtain a $K^2$ graph.

□

Lemma 4.4. GoogleNet [21], Inception-v1 to v4 and Inception-ResNet-v1 [20, 22], which are composed of inception modules are series parallel graphs.

Proof. Due to space limitations, we prove this lemma only for Inception-v4. Similar arguments can be made for the other networks. Consider Inception-C block (Figure 6 in [19]). The output of the Filter concat layer at the bottom splits into 4 branches. The left 2 branches have only degree 2 nodes and can be converted to a single edge by operation 1. For the third branch from left, applying operation 1 on $1 \times 3$ and $3 \times 1$ CONV layers, followed by operation 2 on the resulting parallel edge and then applying operation 1 on $1 \times 1$ CONV layer will result in a single edge. Similarly, the rightmost branch can also be converted into a single edge. The four parallel edges can be merged (operation 2) resulting in a $K^2$ graph. In a similar manner, Inception-A, B and Stem modules can also be reduced to $K^2$. Thus, Inception-v4 network (Figure 9 in [19]) can be reduced into a number of $K^2$ graphs connected in series which can in turn be trivially reduced to $K^2$.

□

5 DYNAMAP: FRAMEWORK SPECIFICATION

DYNAMAP Software Execution Flow: DYNAMAP uses a hardware overlay template (Section 3), which is parameterized with $P_{SA1}, P_{SA2}$, sequence of $\psi$, and sequence of control signals encoded by specific algorithm mapping that defines the behavior of DLT, Linear Transform and Pad-and-Accumulate modules. As shown in Figure 7, after inputs (FPGA device capabilities, CNN meta data) are provided, DYNAMAP executes the following steps: (1) Algorithm 1
first identifies $P_{SA1}, P_{SA2}$ and best $\psi$ associated with available algorithms in each layer. 2 These parameters are used to construct and populate the CNN graph as discussed in Section 5.1. 3 Then, an off-the-shelf PBQP solver [15] is utilized to perform the node reduction steps for algorithm mapping as described in Section 4. The PBQP solver outputs the optimal algorithm assignment vectors for all layers. 4 Based on the algorithm-dataflow mappings, the template overlay is customized. 5 CNN is scanned to identify any consecutive layers whose total memory consumption do not exceed on-chip SRAM capability. Store-side LTUs are allocated and customized to generate SRAM addresses and store the layer output into the Input Buffer. Thus, on FPGA devices with larger on-chip memory, redundant off-chip data traffic will be avoided. 6 Integrating all the optimizations, control signal sequences are generated to support the algorithm switching on the hardware overlay. The output of DYNAMAP is synthesizable VERILOG program that can be deployed on the target FPGA.

In the following, we discuss in detail (i) the CNN Cost Graph Construction, which assumes a fixed systolic array of size $P_{SA1} \times P_{SA2}$, and identifies the cost vectors $\psi$ and Transition matrices $T$ for each layer; (ii) the Hardware Customization, which performs DSE to identify the systolic array dimensions and dataflow mapping to algorithms, providing input to the Cost Graph Construction.

5.1 Cost Graph Construction

To construct cost graph $G = (V', E', C_v, T_v)$ from CNN graph $G = (V, E)$, for each vertex $v' \in V'$, we add a node $v'_i$ into $V'$. Moreover, for each $v' \in V | outdegree(v') > 1$, we add another node $v''_i$ into $V'$ because: Layer $i$ that is connected directly to multiple downstream layers can store the output in only one format. The data load time of each downstream layer is dependent upon this format. The vertex $v'_i$ is used to capture the format in which layer $i$ needs to store the data to DRAM. Now, for an edge $(v', v') \in E$, if outdegree($v'$) ≤ 1, we simply add the edge $(v'_i, v''_j) \in E'$. Else we add the following new edges: $(v'_i, v'_j), (v'_i, v''_j) \forall j$.

5.1.1 Cost Vector Array Construction. Let $\psi$ denote the dataflow. For a GEMM operation with dimensions $a \times b$ (input) and $b \times c$ (weight), the execution time on the systolic array $P_{SA1} \times P_{SA2}$ is given by the following equations:

$$C_{\text{mem}}(P_{SA1}, P_{SA2}; \psi) = \begin{cases} \text{NS} & : \frac{a}{P_{SA1}} + \frac{b}{P_{SA2}} \times a + b + I_{SA}, \\ \text{WS} & : \frac{a}{P_{SA1}} + \frac{b}{P_{SA2}} \times b + I_{SA}, \\ \text{IS} & : \frac{a}{P_{SA1}} + \frac{c}{P_{SA2}} \times a + c + I_{SA}. \end{cases} \quad (9)$$

where $I_{SA}$ represents the one-time initialization overhead.

Thus, the latencies of executing a CONV layer on a device with frequency $FREQ$ are given by Equation 10 for im2col, 11 for kn2row and 12 for Winograd ($m, r$) algorithm.

$$C_{\text{conv}}(P_{SA1}, P_{SA2}; \psi')(O_i, O_k, K_2, C_{\text{out}}) \times K_1 / FREQ \quad (10)$$

The $1^{st}$ row of Table 2 shows the transformation from 3D Tensor to Toepilz layout, which incurs some data copies due to overlapping sliding windows but can be streamed out, as consecutive DRAM addresses are accessed (Section 3.3). In the $2^{nd}$ row, between im2col/kn2row output and kn2row 3D Tensor input, one-to-one matching is required. With Winograd output features, some re-ordering is required but the amount of data is not changed. For 3D Tensor to Winograd input layout transformation shown in $3^{rd}$ row, both data re-ordering and data duplication are needed, and the generated DDR addresses are $H_iK_j$ apart. Note that in Section

![Figure 7: DYNAMAP Software Tool Flow](Image)

### Table 2: Load/Store Latency

| Algo Format: $AF_i \rightarrow AF_{i+1}$ | Load/Store Latency |
|----------------------------------------|-------------------|
| im2col $\rightarrow$ im2col $k$n2row $\rightarrow$ im2col $O_1O_2K_2C_{\text{out}}(1)$ | $H_1H_2C_{\text{out}}(4)$ |
| im2col $\rightarrow$ kn2row $k$n2row $\rightarrow$ kn2row $O_1O_2K_2C_{\text{out}}(2)$ | $H_1H_2C_{\text{out}}(1)$ |
| kn2row $\rightarrow$ Winograd $O_1O_2K_2C_{\text{out}}(3)$ | $H_1H_2C_{\text{out}}(1)$ |
| Winograd $\rightarrow$ $im2col$ $O_1O_2K_2C_{\text{out}}(1) + \text{ overhead}$ | $H_1H_2C_{\text{out}}(4)$ |

$H_1, H_2, K, R, O_i, O_j$ are Layer$i_{th}$ metadata.
3.3 We show the transformation of feature map with depth 1, but in the transformation we access $C_{out}(i)$ altogether for each address increment. Thus, depending on whether each transaction of $C_{out}(i)$ addresses saturate the entire DDR burst length, burst length wastage may occur. We use $f$ to capture such possible wastage of bandwidth:

$$f(BW, C_{out}(i)) = \begin{cases} 
C_{out}(i) & \text{if } C_{out}(i) \geq BL \\
C_{out}(i) / \text{BL} & \text{otherwise}
\end{cases}$$ (13)

The 4th row models the transformation from Winograd output to Winograd input layout, taking advantage of the fact that both are in the “scattered” layout, streaming access can be achieved. The 5th row models the time for the 2-step transformation: Winograd output to 3D Tensor followed by 3D Tensor to Toeplitz layout. We use 2 pipelined LTU operating on double-buffered SRAM, and use $vohd$ to denote the initialization overhead.

The idea of Algorithm 1 is as follows: We iterate through possible values $\mathcal{G}_{PSA1,PSA2}$ for algorithm in layer $i$. For a fixed $\mathcal{G}_{PSA1,PSA2}$ pair, we calculate the value of empirical total node cost, $\tau_{emp}$, which is the sum of the execution times of all the algorithms over all the layers (line 6-11). Execution time of an algorithm for a layer is calculated using the dataflow that leads to the minimum value (line 7-8). $\mathcal{G}_{PSA1,PSA2}$ with minimum $\tau_{emp}$ is output.

5.2 Hardware Customization

We use Algorithm 1 to determine: (1) $\mathcal{G}_{PSA1,PSA2}$ and (2) optimal dataflow mapping for each algorithm for each layer. $\mathcal{G}_{PSA1,PSA2}$ is then used to construct the CNN cost graph $\mathcal{G}_{PSA1,PSA2}$. The key idea of Algorithm 1 is as follows: We iterate through possible values of $\mathcal{G}_{PSA1}$ and $\mathcal{G}_{PSA2}$ (line 4). For a fixed $\mathcal{G}_{PSA1,PSA2}$ pair, we calculate the value of empirical total node cost, $\tau_{emp}$, which is the sum of the execution times of all the algorithms over all the layers (line 6-11). Execution time of an algorithm for a layer is calculated using the dataflow that leads to the minimum value (line 7-8). $\mathcal{G}_{PSA1,PSA2}$ with minimum $\tau_{emp}$ is output.

6 EVALUATIONS

The fundamental objective of our framework is to reduce hardware under-utilization induced by diverse layer shapes and minimize the total end-to-end inference latency. In this section, we use the framework to generate the hardware-algorithm co-designs for two state-of-the-art CNNs, GoogleNet[21] and Inception-v4[21] and show: (1) how our dynamic dataflow selection and architecture configuration technique achieves local optimal acceleration at each layer by driving up effective PE utilization; (2) how our novel algorithm mapping achieves global optimal acceleration by improving end-to-end inference latency.

We use Xilinx Alveo U200 FPGA board hosted on a Xeon Server CPU (E5-2698 v4 @2.2GHz) to evaluate the designs generated by our framework. We use 8-bit fixed-point data representation to perform CNN inference. The designs were synthesized using Vivado 2018. We input the CNN model and FPGA device meta data into our framework to obtain the architecture customization as output. We limit the systolic array DSP consumption to 6084 instead of using all the available DSPs to obtain a fair performance comparison with the state-of-the-art implementations. DYNAMAP returns optimal ($\mathcal{G}_{PSA1,PSA2}$) as (92.66) for GoogleNet, and (95.64) for Inception-V4. The resource utilization are shown in Table 3.

6.1 Evaluation of Optimizations

6.1.1 Hardware Utilization under different accelerator configurations. We define the metric, effective PE utilization, $\mu_i$, as ratio of the total number of effective computations and the total number of computed by all PEs. That is,

$$\mu_i = \frac{\sum_t \text{PE}_{\text{exe}}}{
\sum_t \text{PE}_{\text{total}}}
= \frac{Y_{\text{CONV}}}{T \cdot \text{PE}_{\text{total}}}
$$ (14)

where $T$, $Y_{\text{CONV}}$, denote the total consumed cycles and the total number of required multiply-accumulate operations for one CONV layer, respectively. $\text{PE}_{\text{total}}$ is the number of effective working PEs in cycle $t$ that contributes to effective $Y_{\text{CONV}}$ computations. $\text{PE}_{\text{total}}$ is the total number of PEs.

Figure 9,10 show the values of $\mu_i$ for each CONV layer $i$ in Inception-v4 and GoogleNet. In each figure, we use the algorithm mapping returned by the framework. The "square-NS" ($b_1$) plot shows the theoretical layer-wise effective PE utilization assuming the algorithms are deployed with the stall-free PE and data layout optimizations on the largest square-shaped systolic array within the resource constraint on the target FPGA, but no dataflow optimization is applied and only NS dataflow is used across all layers. Considering the upper DSP bound - 6084×78×78 - input into the framework, such largest systolic array is shaped at (78,78). The "algo1-NS" ($b_1)$ plot evaluates the effect of systolic-array dimension identification as performed using Algorithm 1, without dataflow optimization. The "algo1-optimized" (OPT) plot shows the resulting effective PE utilization when running the same set
of algorithms using the \((P_{SA1}, P_{SA2}, \psi)\) identified by DYNAMAP (Algorithm 1). Compared to \(bl_3\), which only uses NS dataflow, \(OPT\) shows consistent improvement on almost all the layers as it minimizes zero-paddings required in the systolic array as discussed in Section 3.2. Compared to \(bl_1\), which uses a square-shaped systolic array, although for a very small number of layers the \(OPT\) utilization is not as saturated, the performance loss in those layers are much smaller than the performance gains obtained in other layers. Algorithm 1 finds the sweet spot for the shape of the systolic array that drives up \(\mu\) across all the layers and minimizes end-to-end latency. Global CNN wide trade-off analysis performed by \(OPT\) ensures that the performance benefit on more compute-intensive layers outweighs any losses on other layers. Overall, compared to a NS-dataflow implementation on the largest square-shaped systolic array, by implementing the designs generated by DYNAMAP, we observe 32\% and 35\% lower latency in end-to-end latency for Googlenet and Inception-v4, respectively.

### 6.1.2 Effect of layer-wise algorithm switching

We calculate the execution time of each CNN module using different algorithms. Figure 11 and 12 shows the results for the two CNNs, where on the x axis we group all the CONV layers in each Inception (Reduction) Module, consistent with the notions in [20, 21] and the corresponding columns show the sum of computation and communication latency of all layers in an Inception (Reduction) Module. The STEM module in Inception-v4 is broken down by the first Filter Concatenation layer for better visibility. The ”im2col-only” (\(bl_3\)) columns show the result of using one algorithm - im2col - across all the layers, the ”kn2row-applied” (\(bl_4\)) columns show the results of applying kn2row where possible and im2col everywhere else, and the ”wino-applied” (\(bl_5\)) columns show the results of applying Winograd \((m = 2, r = 3)\) where applicable (i.e. layers with square-shaped kernels) and im2col everywhere else. \(OPT_{returned}\) are the results using algorithm mapping returned by DYNAMAP, which is observed to be superior than all \(bl_3\) - \(5\) on all modules. In Inception-v4, a large portion of the kernels are shaped 7(3)\(\times\)1, making such layers more memory-bound, therefore kn2row almost always out-perform im2col, which requires data duplication and results in less data-reuse. However, on GoogleNet, for most layers the lower-communication-cost benefit of kn2row do not offset the overheads due to ”Pad-and-Accumulate” and serializing a large GEMM into \(K^2\) smaller ones, making it less advantageous. A typical
Algorithm Mapping with the smallest layer node cost $c$

Table 4: End-to-end Latency Improvement due to Dynamic Algorithm Mapping

| Algorithm         | $b_{L_1}$ | $b_{L_2}$ | $b_{L_3}$ |
|-------------------|-----------|-----------|-----------|
| GoogleNet         | 67.5%     | 78%       | 22%       |
| Inception-V4      | 86%       | 61%       | 17%       |

![Figure 11: Layer exe. times: Inception-v4](image)

GoogleNet Inception Module has two layers with square-shaped $3 \times 3$ and $5 \times 5$ kernels among others. While applying Winograd on such layers always reduces the computation complexity, it is not always optimal overall. This is because for kernels larger than $3 \times 3$, $\frac{K}{K^2}$ rounds of Winograd is required, resulting in severe transformation overheads and amortized decrease in computation complexity reduction. Winograd also imposes high memory overheads and layout transformation cost, so kn2row is overall better for such layers with slightly higher computation cost but significantly lower communication cost. These observations suggest that an algorithm mapping scheme that greedily chooses the algorithm with the smallest layer node cost $c$ would not return the optimal mapping. DYNAMAP captures the tradeoffs that occur in such algorithm transitions, yielding lower end-to-end latency than using any of the algorithm or even all three algorithms greedily selected based on layer node costs. The algorithm mapping obtained in DYNAMAP is optimal on the given systolic array (as supported by Theorem 4.1) and is obtained within 2 seconds on an AMD 3700X CPU. The overall percentage decrease in the latency of the designs returned by DYNAMAP compared to the base-lines ($b_{L_3-5}$) are summarized in Table 4.

![Figure 12: Layer exe. times: GoogleNet](image)

6.2 Comparison with State-of-the-art

Table 3 compares the performance of our design produced by DYNAMAP with the state-of-the-art. We achieve 286MHz frequency for both GoogleNet and Inception-v4 accelerator designs. GoogleNet acceleration using DYNAMAP significantly outperforms [12] and [27] in terms of both latency and throughput. This is partly due to the advantage of DYNAMAP’s optimizations on dataflow and algorithm switching, partly due to the lower-precision we adopted enabling more PEs. Even if we scale down the systolic array size (2 DSP consumption per PE), in the worst case the performance would be halved and we still achieve 2x and 1.4x lower latency compared with [12] and [27], respectively. For Inception-v4, we compare with [31] which applies dynamic memory management to overcome data transfer bottlenecks and [25] that uses kn2row method for all layers in GoogleNet. Compared to [25], even with lower frequency, our design achieves 20% speedup. While using Winograd on some layers leads to low complexity, its impact is limited as there are more memory-bound than computation-bound layers in Inception-v4. However, DYNAMAP allocates kn2row to those memory-bound kernels while keeping the computation-bound layers optimized as well, integrating dataflow optimization to improve hardware utilization in both cases. As CNNs evolve to be more layer-diverse and the tradeoffs become less obvious, the benefits of using DYNAMAP will become much more pronounced.

The motivation of FlexCNN [18] is similar to that of DYNAMAP. However, it uses dynamic tiling with data layout optimizations across different layers to drive up effective DSP utilization to as high as 93.5%/91.4% on $3 \times 3$/$1 \times 1$-kernel layers on the OpenPose-v2 network (2.9 GOPS). It achieves a single-image inference latency of 24.7ms using $8 \times 8 \times 8$ systolic array. To estimate the best-case performance using FlexCNN to accelerate Googlenet ($\sim 3$ GOPS) and Inception-v4 ($\sim 9$ GOPS), we project this latency onto GoogleNet (Inception-v4) with $92 \times 66 / 95 \times 64$ PEs as deployed in our design (optimistically assuming 100% DSP utilization on all types of layers): $l_{\text{projected-GN}} = 24.7ms \times \frac{8 \times 8 \times 8 \times 93\%}{92 \times 66 \times 100\%}, \frac{3 \text{ GOPS}}{2 \text{ GOPS}} = 2ms$, $l_{\text{projected-Inp4}} = 24.7ms \times \frac{8 \times 8 \times 8 \times 93\%}{95 \times 64 \times 100\%}, \frac{3 \text{ GOPS}}{2 \text{ GOPS}} = 6ms$, both higher than DYNAMAP’s achieved latency. This is because DYNAMAP uses compute-reducing algorithm, Winograd, and memory-saving algorithm, kn2row, to resolve bottlenecks in both compute-intensive and memory-bound layers. The achieved performance benefits offset the additional overheads for switching between different algorithms in DYNAMAP.

7 CONCLUSION

In this paper, we proposed an architecture-algorithm co-optimization framework to achieve low-latency CNN inference on FPGA. Our proposed hardware overlay includes several optimizations to achieve no-overhead dataflow switching and low-overhead algorithm switching. Our software tool flow achieves fast algorithm mapping and hardware customization. DYNAMAP has a wide applicability in optimizing the acceleration of any complex CNN models, even with extremely diverse layer configurations, on any FPGA devices. In the future, we will explore the possibility of generalizing DYNAMAP to a wider range of algorithms, including strided-Winograd and frequency-domain methods.

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