Interface reactions at TiN/HfSiON gate stacks: Dependence on the electrode structure and deposition method

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Received 21 October 2006; received in revised form 22 December 2006; accepted 27 December 2006
Available online 6 March 2007

Abstract

We systematically investigated intrinsic and extrinsic thermal reactions at TiN/HfSiON gate stacks. The formation of an ultrathin TiO2 interlayer was found to be an intrinsic reaction at the metal/insulator interface, but growth of SiO2 underlayers between HfSiON and Si substrates, which determines the electrical thickness of metal-oxide-semiconductor (MOS) devices, depends on the structure and deposition method of the gate electrodes. Physical vapor deposition (PVD) grown TiN electrodes covered with W overlayers exhibited excellent thermal stability at up to 1000°C. Formation of ultrathin TiO2 interlayers reduced gate leakage current (I_g), and growth of the oxide underlayer was suppressed by less than a few angstroms even for 1000°C annealing. In contrast, we found that halogen impurities within CVD-grown metal electrodes enhance interface SiO2 growth, resulting in deterioration of equivalent oxide thickness (EOT) versus I_g characteristics of the gate stacks.

Keywords: High-k gate dielectrics; Metal electrode; Thermal stability; Interface reaction; Electrical degradation; Hafnium silicate; Titanium nitride

1. Introduction

Metal-oxide-semiconductor field effect transistors (MOSFETs) have been scaled down, and the physical thickness of SiO2 dielectrics has correspondingly dropped below 2 nm. Accordingly, the gate leakage current due to direct tunneling through the gate oxide has increased drastically. High-permittivity metal oxides have been extensively studied as alternative gate dielectrics (high-k gate dielectrics) in the hopes of achieving continuous scaling of gate dielectrics beyond 45-nm nodes and of developing low-power devices [1]. Hf-based insulators, such as Hf silicate (HfSiO) and nitrided films (HfSiON) based on it, are promising candidates for high-k dielectrics due to their excellent thermal stability when in contact with Si substrates [2,3]. In addition, substituting poly-Si electrodes using metal materials improves the current drivability of MOSFETs because using metal electrodes can eliminate gate depletion at the electrode/insulator interface. Thus, metal/high-k gate stacks need to be developed for advanced MOSFETs. Titanium nitride (TiN) has been reported to be thermally stable and has a suitable effective work function (eWF) as a p-type or midgap metal on Hf-based high-k dielectrics. However, even though these materials have superior thermal stability, MOSFETs with a TiN/HfSiON gate stack reportedly experience degradation of carrier mobility, a change in eWF, and an increase in the electrical thickness [4]. These results indicate several kinds of thermal reactions occur at the metal/high-k interface and that some of them are inevitable and an intrinsic feature of the system.

In our previous study, we investigated interface reactions between a physical vapor deposition (PVD)-grown TiN...
electrode and HfSiON dielectric [5]. Our results indicated that an ultrathin TiO$_2$ interlayer formed due to a thermal reaction at TiN/HfSiON at 700 °C or more. The interlayer formation did not cause serious degradation in terms of electrical thickness and gate leakage at up to 900 °C, but these results are not consistent with other reports which shows monotonous increase of these values after annealing [4]. This discrepancy indicates that extrinsic effects caused by the film deposition method and electrode structure also affect the thermal stability of the TiN/HfSiON gate stacks.

In this study, we systematically investigated the physical and electrical properties of the metal/high-$k$ gate stacks to clarify the effects of intrinsic and extrinsic reactions at TiN/HfSiON interfaces.

2. Experimental

The HfSiON gate dielectrics used in this study were formed by metal–organic chemical vapor deposition (MOCVD) on p-type Si(001) substrates [5,6]. The Hf ratio [Hf/(Hf+Si)] was 0.6, and nitridation of the silicate films was carried out using NH$_3$ annealing. The equivalent oxide thickness (EOT) and leakage current at a gate bias $V = V_{fb} - 1V$ ($V_{fb}$: flat band voltage) are 1.2–1.3 nm and about 4 × 10$^{-2}$ A/cm$^2$, respectively. The silicate films remained amorphous after activation annealing over 1000 °C. To characterize the intrinsic and extrinsic nature of the TiN/HfSiON interface systematically, we fabricated W/TiN/HfSiON layered structures using various methods and under various growth conditions. The thickness of the work function metal, that is, the TiN underlayer, was 10 nm for each sample. We deposited low-resistivity $W$ overlayers with thicknesses ranging from 50 to 100 nm. The TiN layers were deposited using PVD or chemical vapor deposition (CVD) methods. Reactive sputtering using a Ti target was conducted for PVD-TiN fabrication. The CVD-TiN was formed by using TiCl$_4$ and NH$_3$ sources at growth temperatures of 450 or 650 °C. The W overlay of capacitor samples for electrical characterization was also fabricated using PVD with a W target or using CVD with a WF$_6$ source. The physical characterization of the metal/high-$k$ gate stacks was performed using reflection high-energy electron diffraction (RHEED) and secondary ion mass spectroscopy (SIMS). For RHEED analysis of TiN/HfSiON interfaces, the TiN electrodes were removed using an H$_2$O$_2$ solution after annealing the samples in nitrogen ambient from 300 to 1100 °C for 30 s (see Fig. 1).

The impurity of W/TiN/HfSiON layered structures, such as fluorine, chlorine, and oxygen, were also examined by SIMS. The electrical properties of the W/TiN/HfSiON gate stacks fabricated using various methods and under various conditions were studied through capacitance–voltage ($C$–$V$) and current–voltage ($I$–$V$) measurements after annealing. The $C$–$V$ measurement was performed at 1 MHz.

3. Results and discussion

3.1. Intrinsic reactions at TiN/HfSiON interface

We reported on the formation of ultrathin polycrystalline TiO$_2$ at PVD-TiN/HfSiON interfaces after moderate annealing conditions around 700 °C [5]. In our previous experiments, we selectively removed TiN electrodes by wet etching to observe changes in interface structure using RHEED, as shown in schematic illustrations in Fig. 1. The RHEED patterns labeled (a)–(e) represent results from PVD-grown TiN electrodes we reported in our previous paper [5]. The RHEED pattern after 500 °C annealing only showed a diffuse background (Fig. 1(a)), indicating that HSION film remains amorphous at this temperature range. However, we observed ring patterns after annealing at higher temperatures. Fig. 2 shows the results of diffraction pattern analysis, indicating that the ring patterns originate from a polycrystalline TiO$_2$ layer. The polycrystalline interlayer at a moderate annealing temperature of 700 °C (Fig. 2(a)) was assigned to an anatase-TiO$_2$ phase, while the structure changed to a rutile-TiO$_2$ phase after 1100 °C annealing (Fig. 2(b)). Although partial oxidation occurred on the TiN surfaces, the surface oxidized layer could be easily removed by wet etching, and the formation of a stable and uniform TiO$_2$ interlayer was confirmed from RHEED, total-reflection X-ray fluorescence and atomic force microscopy [5].

Thermal reactions at the aforementioned TiN/HfSiON interfaces are reproducible. However, ion-induced damage should be considered for PVD-grown TiN to determine the nature of the metal/high-$k$ interface. To understand the intrinsic features of the TiN/HfSiON interface, we also fabricated TiN layers using the CVD method. We deposited TiN films at 450 or 650 °C because the growth temperature is a crucial parameter for chemical reactions. Figs. 1(d)–(i) show RHEED patterns obtained from the CVD-TiN/HfSiON interfaces after annealing them at various temperatures. We observed diffuse RHEED patterns from amorphous HfSiON layers after 500 °C annealing for both of the growth conditions. This indicates that the CVD-TiN/HfSiON interface is thermally stable at up to 500 °C as was observed for the PVD-TiN electrode. Moreover, we obtained quite similar ring patterns both for the CVD and PVD-TiN samples at higher annealing temperatures. Our pattern analysis showed that polycrystalline anatase and rutile TiO$_2$ phases formed at 700 and 1100 °C annealing, respectively. These were independent of the fabrication method and the growth temperature of TiN electrodes. These results clearly mean that formation of the TiO$_2$ interlayer is an intrinsic reaction at the TiN/HfSiON interfaces.

3.2. Extrinsic reaction dependent on electrode structure and deposition method

Even though an intrinsic reaction occurs at the TiN/HfSiON interface, many controversial reports on the
electrical properties of metal/high-
$k$ stacks have a different thermal budget. A possible explanation for the discrepancy is extrinsic effects that depend on the deposition method and structure of the electrodes. Thus, we fabricated W/TiN/HfSiON/Si capacitors using various fabrication methods and under various conditions, and systematically investigated the thermal stability of the gate stacks in terms of EOT scaling and gate leakage ($I_g$). Table 1 shows the fabrication conditions of the metal/high-$k$ capacitors. The TiN underlayer was deposited using PVD or CVD methods, in which 450 or 650°C was selected as the growth temperatures for the CVD. Then, the low-resistivity W overlayer was also deposited using PVD or CVD methods. After annealing the W/TiN/HfSiON/Si capacitors at various temperatures in nitrogen ambient, $C$–$V$ and $I$–$V$ measurements were carried out to estimate EOT and $I_g$. Fig. 3 shows the EOT stability of the gate stacks prepared under various conditions. The EOT increase due to interfacial SiO$_2$ growth was less than a few angstroms when TiN underlayers were deposited using the PVD method. In addition, for the PVD-W/PVD-TiN stacked structure, we obtained excellent thermal stability at up to 1000°C. In contrast, an apparent EOT increase was observed for a CVD-W/CVD-TiN electrode at temperatures over 700°C. Note that the electrical degradation was severe for a low-temperature CVD condition at 450°C. Moreover, the EOT increase could be suppressed at 900°C when using a CVD-TiN underlayer formed by a high-temperature CVD condition and PVD-W overlayer. These results mean that the PVD method is preferable and that the deposition method of the TiN underlayer is the crucial factor from the viewpoint of EOT scaling. However, when we consider the ion-induced damage of the PVD method and conformal growth of the metal electrode for three-dimensional and replacement gate devices, a combination of CVD-growth of work function metal and a PVD-grown overlayer could be a possible solution for fabricating metal/high-$k$ gate stacks.

Fig. 4 shows typical EOT versus $I_g$ characteristics of W/TiN/HfSiON/Si capacitors, in which the W overlayers were fabricated using the CVD method. Note that the deposition method of the TiN underlayer apparently affects the electrical properties of the gate stacks. As shown in Fig. 3, the EOT increase in the CVD-W/PVD-TiN/HfSiON/Si capacitors is moderate compared with the CVD-TiN case. The EOT versus $I_g$ characteristic for the PVD-TiN electrode shown in Fig. 4(a) does not change after annealing at 600°C, and we also observed an $I_g$ reduction of about one order of magnitude after annealing at 700–900°C without an EOT increase. These results coincide well with the intrinsic nature of the TiN/HfSiON interface discussed in the former section because the formation of the insulating TiO$_2$ interlayer, which has an extremely high permittivity, suppresses the tunneling
current without a marked increase in the electrical thickness. However, at a higher temperature of 1100 °C, growth of interfacial SiO₂ due to residual oxygen and degradation of insulating features both of TiO₂ and HfSiON lead to an increase in the EOT as well as $I_g$. However, when using a CVD-TiN electrode (Fig. 4(b)), we observed a monotonous EOT increase and $I_g$ reduction even at temperatures over 700 °C.

To clarify the extrinsic thermal stability of the TiN/HfSiON interface, we next studied the impurities of the metal electrodes by SIMS. Fig. 5 shows the SIMS profiles of chlorine, fluorine, and oxygen impurities within the PVD and CVD-grown metal electrodes. CVD-grown films contain larger amounts of chlorine and fluorine impurities than films having a PVD-W/PVD-TiN stacked electrode (Fig. 5(a)), especially for a low growth temperature condition (see Figs. 5(b) and (c)). These results mean that growth of the interface oxide (SiO₂) causing an EOT increase is closely related to the amount of halogen impurities near the HfSiON dielectric. Considering that fluorine-enhanced thermal oxidation occurs on Si surfaces [7], we conclude that interface oxide growth due to residual oxygen diffusing through the metal electrodes is enhanced by halogen impurities near the dielectric interface. We also

| Table 1 | Fabrication conditions of W/TiN/HfSiON/Si gate stacks |
|---------|-------------------------------------------------------|
|         | PVD-TiN | CVD-TiN (650 °C) | CVD-TiN (450 °C) |
| PVD-W   | o       | o                | x                |
| CVD-W   | o       | o                | o                |

Fig. 2. RHEED pattern analysis of the polycrystalline interlayer formed after nitrogen annealing at (a) 700 °C and (b) 1100 °C. Diffraction intensities from candidate materials are also shown at the lower part of the RHEED patterns.

Fig. 3. EOT stability of W/TiN/HfSiON/Si capacitors prepared by different deposition methods and growth conditions. The thickness of the bottom TiN layer was 10 nm, and that of the low-resistivity W overlayer ranged from 50 to 100 nm. The electrical thickness was estimated from a conventional $C-V$ measurement at a frequency of 1 MHz.
obtained quite similar results for work function metals, such as TaN and TaSi, covered with CVD or PVD-W overlayers (data not shown). Therefore, we believe that a low-damage PVD method or low-impurity work function metals covered with PVD-grown overlayers is indispensable for fabricating advanced metal/high-$k$ gate stacks down to the sub-1-nm EOT region.

4. Conclusions

We studied the thermal stability of metal/high-$k$ gate stacks. The formation of a polycrystalline TiO$_2$ interlayer for TiN/HfSiON interfaces is an intrinsic reaction at temperatures at 700 °C or more. In terms of EOT versus $I_g$ characteristics, this intrinsic reaction improves the...
electrical properties of the gate stack. We also found that halogen impurities within the CVD-grown metal electrodes deteriorate the EOT stability due to growth of the interface SiO$_2$ layer. Therefore, the PVD method is preferable from the viewpoint of EOT scaling. However, a combination of low-impurity CVD growth for thin work function metal and PVD-grown overlayer metal is also a possible solution for fabricating advanced MOSFETs if we wish to utilize the advantages of the CVD growth.

Acknowledgment

This work was partly supported by the Grant-in-Aid for the 21st Century COE Program from the Ministry of Education, Culture, Sports, Science and Technology of Japan and by the “High-$\kappa$ Network” in cooperation with academic, industry, and government institutes.

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