Accelerating Bulk Bit-Wise X(N)OR Operation in Processing-in-DRAM Platform

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ABSTRACT
With Von-Neumann computing architectures struggling to address computationally- and memory-intensive big data analytic tasks today, Processing-in-Memory (PIM) platforms are gaining growing interests. In this way, processing-in-DRAM architecture has achieved remarkable success by dramatically reducing data transfer energy and latency. However, the performance of such system unavoidably diminishes when dealing with more complex applications seeking bulk bit-wise X(N)OR- or addition operations, despite utilizing maximum internal DRAM bandwidth and in-memory parallelism. In this paper, we develop DRIM platform that harnesses DRAM as computational memory and transforms it into a fundamental processing unit. DRIM uses the analog operation of DRAM sub-arrays and elevates it to implement bit-wise X(N)OR operations between operands stored in the same bit-line, based on a new dual-row activation mechanism with a modest change to peripheral circuits such as sense amplifiers. The simulation results show that DRIM achieves on average 71× and 8.4× higher throughput for performing bulk bit-wise X(N)OR operations compared with conventional CPU and GPU, respectively. Besides, DRIM outperforms recent processing-in-DRAM platforms with up to 3.7× better performance.

1 INTRODUCTION
In the last two decades, Processing-in-Memory (PIM) architecture, as a potentially viable way to solve the memory wall challenge, has been well explored for different applications [1–7]. The key concept behind PIM is to realize logic computation within memory to process data by leveraging the inherent parallel computing mechanism and exploiting large internal memory bandwidth. The proposals for exploiting SRAM-based [8, 9] PIM architectures can be found in recent literature. However, PIM in context of main memory (DRAM- [2, 3, 10]) has drawn much more attention in recent years mainly due to larger memory capacities and off-chip data transfer reduction as opposed to SRAM-based PIM. Such processing-in-DRAM platforms show significantly higher throughputs leveraging multi-row activation methods to perform bulk bit-wise operations by either modifying the DRAM cell and/or sense amplifier. For example, Ambit [2] uses triple-row activation method to implement majority-/AND/OR logic, outperforming Intel Skylake-CPU, NVIDIA GeForce GPU, and even HMC [11] by 44.9×, 32.0×, and 2.4×, respectively. DRISA [12] employs 3TIC- and 1TIC-based computing mechanisms and achieves 7.7× speedup and 15× better energy-efficiency over GPUs to accelerate convolutional neural networks. However, there are different challenges in such platforms that make them inefficient acceleration solutions for X(N)OR- and addition-based applications such as DNA alignment and data encryption. Due to the intrinsic complexity of X(N)OR logic, current PIM designs are not able to offer a high-throughput X(N)OR-based operation despite utilizing the maximum internal bandwidth and memory level parallelism. This is because majority/AND/OR-based multi-cycle operations and required row initialization in the previous designs.

To overcome the memory bandwidth bottleneck and address the existing challenges, we propose a high-throughput and energy-efficient PIM accelerator based on DRAM, called DRIM. DRIM exploits a new in-memory computing mechanism called Dual-Row Activation (DRA) to perform bulk bit-wise operations between operands stored in different word-lines. The DRA is developed based on analog operation of DRAM sub-arrays with a modest change in the sense amplifier circuit such that X(N)OR operation can be efficiently realized on every memory bit-line. In addition, such design addresses the reliability concerns regarding the voltage deviation on the bit-line and multi-cycle operations of the triple-row activation method. We evaluate and compare DRIM’s raw performance with conventional and PIM accelerators including a Core-i7 Intel CPU [13], an NVIDIA GTX 1080Ti Pascal GPU [14], Ambit [2], DRISA-1TIC [3], and HMC 2.0 [11], to handle bulk bit-wise operations. We observe that DRIM achieves remarkable throughput compared to Von-Neumann computing systems (CPU/GPU) through unblocking the data movement bottleneck by on average 71×/8.4× better throughput. DRIM outperforms other PIMs in performing X(N)OR-based operations by up to 3.7× higher throughput. We further show that a 3D-stacked DRAM built on top of DRIM can boost the throughput of the HMC by ~13.5×. From the energy consumption perspective, DRIM reduces the DRAM chip energy by 2.4× compared with Ambit [2] and 69× compared with copying data through the DDR4 interface.

To the best of our knowledge, this work is the first that designs a high-throughput and energy-efficient X(N)OR-friendly PIM architecture exploiting DRAM arrays. We develop DRIM based on a set of novel microarchitectural and circuit-level schemes to realize a data-parallel computational unit for different applications.

2 BACKGROUND AND MOTIVATION
2.1 Processing-in-DRAM Platforms
A DRAM hierarchy at the top level is composed of channels, modules, and ranks. Each memory rank, with a data bus typically 64-bits wide, includes a set of memory chips that are manufactured with a variety of configurations and operate in unison [2, 15]. Each chip is further divided into multiple memory banks that contains 2D sub-arrays of memory cells virtually-organized in memory matrices (mats). Banks within same chips share I/O, buffer and banks in different chips working in a lock-step manner. Each memory sub-array, as shown in Fig. 1a, has 1) a large number of rows (typically 2^9 or 2^10) holding DRAM cells, 2) a row of Sense Amplifiers (SA), and 3) a Row Decoder (RD) connected to the cells. A DRAM
cell basically consists of two elements, a capacitor (storage) and an Access Transistor (AT) (Fig. 1b). The drain and gate of the AT is connected to the Bit-line (BL) and Word-line (WL), respectively. DRAM cell encodes the binary data by the charge of the capacitor. It represents logic ‘1’ when the capacitor is full-charged, and logic ‘0’ when there is no charge.

- **Write/Read Operation:** At initial state, both BL and BL are always set to $\frac{V_{dd}}{2}$. Technically, accessing data from a DRAM’s sub-array (write/read) after initial state is done through three consecutive commands [2, 16] issued by the memory controller: 1) During the activation (i.e., ACTIVATE), activating the target row, data is copied from the DRAM cells to the SA row. Fig. 1b shows how a cell is connected to a SA via a BL. The selected cell (storing $V_{dd}$ or 0) shares its charge with the BL leading to a small change in the initial voltage of BL ($\frac{V_{dd}}{2} \pm \delta$). Then, by activating the enable signal, the SA senses and amplifies the $\delta$ of the BL voltage towards the original value of the data through voltage amplification according to the switching threshold of SA’s inverter [16]. 2) Such data can be then transferred from/to SA to/from DRAM bus by a READ/WRITE command. In addition, multiple READ/WRITE commands can be issued to one row. 3) The PRECHARGE command precharges both BL and WL again and makes the sub-array ready for the next access.

- **Copy and Initialization Operations:** To enable a fast (\(< 100\text{ns}\)) in-memory copy operation within DRAM sub-arrays, rather than using \(~1\mu s\) conventional operation in Von-Neumann computing systems, RowClone-Fast Parallel Mode (FPFM) [17] proposes a PIM-based mechanism that does not need to send the data to the processing units. In this scheme, two back-to-back ACTIVATE commands to the source and destination rows without PRECHARGE command in between, leads to a multi-kilo byte in-memory copy operation. This operation takes only 90ns [17]. This method has been further used for row initialization, where a preset DRAM row (either to ‘0’ or ‘1’) can be readily copied to a destination row. RowClone imposes only a 0.01% overhead to DRAM chip area [17].

- **Not Operation:** The NOT function has been implemented in different works employing Dual-Contact Cells (DCC), as shown Fig. 1c. DCC is mainly designed based on typical DRAM cell, but equipped with one more AT connected to BL. Such hardware-friendly design [2, 18, 19] can be developed for a small number of rows on top of existing DRAM cells to enable efficient NOT operation with issuing two back-to-back ACTIVATE commands [2]. In this way, the memory controller first activates the $W_{L\text{dec}1}$ (Fig. 1c) of input DRAM cell, and reads the data out to the SA through BL. It then activates $W_{L\text{dec}2}$ to connect BL to the same capacitor and so writes the negated result back to the DCC.

- **Other Logic Operations:** To realize the logic function in DRAM platform, *Ambit* [2] extends the idea of RowClone by implementing 3-input majority (Maj3)-based operations in memory by issuing the ACTIVATE command to three rows simultaneously followed by a single PRECHARGE command, so-called *Triple Row Activation (TRA)* method. As shown in Fig. 2a, considering one row as the control, initialized by $D_k = 0/1$, Ambit can readily implement in-memory AND2/OR2 in addition to Maj3 functions through charge sharing between connected cells ($D_k$, $D_1$ and $D_2$) and write back the result on $D_r$ cell. It also leverage TRA mechanism along with DCCs to realize the complementary functions. However, despite Ambit shows only 1% area over commodity DRAM chip [2], it suffers from multi-cycle PIM operations to implement other functions such as XOR2/XNOR2 based on TRA. Alternatively, *DRISA*-3T1C method [3] utilizes the early 3-transistor DRAM design [20], in which the cell consists of two separate read/write ATs, and one more transistor to decouple the capacitor from the read BL (rBL), as shown in Fig. 2b. This transistor connects the two DRAM cells in a NOR style on the $rBL$ naturally performing functionally-complete NOR2 function. However, DRISA-3T1C imposes very large area overhead (2T per cell) and still requires multi-cycle operations to implement more complex logic functions. *DRISA*-1T1C method [3] offers to perform PIM through upgrading the SA unit by adding a CMOS logic gate in conjunction with a latch, as depicted in Fig. 2c. Such inherently-multi-cycle operation can enhance the performance of a single function through add-on CMOS circuitry, in two consecutive cycles. In first cycle, $D_1$ is read out and stored in the latch, and in the second cycle, $D_1$ is sensed to perform the computation. However, this design imposes excessive cycles to implement other logic functions and at least 12 transistors to each SA. Recently, *Dracc* [21] implements a carry look-ahead adder by enhancing Ambit [2] to accelerate convolutional neural networks.

### 2.2 Challenges

There are three main challenges in the existing processing-in-DRAM platforms that make them inefficient acceleration solutions for XOR-based computations and we aim to resolve them:
• Limited throughput (Challenge-1): Due to the intrinsic complexity of X(N)OR-based logic implementations, current PIM designs (such as Ambit [2], DRISA [3], and Drac [21]) are not able to offer a high-throughput and area-efficient X(N)OR or addition in-memory operation despite utilizing maximum internal DRAM bandwidth and memory-level parallelism for NOT, (N)AND, (N)OR, and MAJ/MIN logic functions. Moreover, while DRISA-ITIC method could implement either XNOR or XOR functions as the add-on logic gate, it requires at least two consecutive cycles to perform the computation, which in turn limits other logics implementation. We address this challenge by proposing the DRA mechanism in Section 3.1 and 3.4.

• Row initialization (Challenge-2): Given R=AopB function (op ∈ AND2/OR2), TRA-based method [2, 16] takes 4 consecutive steps to calculate one result as it relies on row initialization: 1-RowClone data of row A to row D1 (copying first operand to a computation row to avoid data-overwritten), 2-RowClone of row B to D2, 3-RowClone of ctrl row to D3 (copying initialized control row to a computation row), 4-TRA and RowClone data of row D1 to row D2, and 5-TRA. Therefore, TRA method needs average 360ns to perform such in-memory operations. When it comes to XOR/XNOR operation, Ambit requires at least three row-initialization steps to process two input rows. Obviously, this row-initialization load could adversely impact the PIM's energy-efficiency especially dealing with such big data problems. This challenge is addressed in Section 3.1 through the proposed sense amplifier, which totally eliminates the need for initialization in performing X(N)OR-based logic.

• Reliability concerns (Challenge-3): By simultaneously activating three cells in TRA method, the deviation on the BL might be smaller than typical one-cell read operation in DRAM. This can elongate the sense amplification state or even adversely affect the reliability of the result [2, 16]. The problem can be even intensified when multiple TRA are needed to implement X(N)OR-based computations. To explore and address this challenges, we perform an extensive Monte-Carlo simulation on our design in Section 3.3.

3 DRIM DESIGN

DRIM is designed to be an independent, high-performance, energy-efficient accelerator based on main memory architecture to accelerate different applications. The main memory organization of DRIM is shown in Fig. 3 based on typical DRAM hierarchy. Each mat consists of multiple computational memory sub-arrays connected to a Global Row Decoder (GRD) and a shared Global Row Buffer (GRB). According to the physical address of operands within memory, DRIM’s Controller (Ctrl) is able to configure the sub-arrays to perform data-parallel intra-sub-array computations. We divide the DRIM’s sub-array row space into two distinct regions as depicted in Fig. 3: 1- Data rows (500 rows out of 512) that include the typical DRAM cells (Fig. 1b) connected to a regular Row Decoder (RD), and 2- Computation rows (12), connected to a Modified Row Decoder (MRD), which enables multiple row activation required for bulk bit-wise in-memory operations between operands. Eight computational rows (x1, ..., x8) include typical DRAM cells and four rows (dec1, ..., dec4) are allocated to DCCs (Fig. 1c) enabling NOT function in every sub-array. DRIM’s computational sub-array is motivated by Ambit [2], but enhanced and optimized to perform both TRA and the proposed Dual-Row Activation (DRA) mechanisms leveraging charge-sharing among different rows to perform logic operations, as discussed below.

3.1 New In-Memory Operations

• Dual-Row Single-Cycle In-Memory X(N)OR: With a careful observation on the existing processing-in-DRAM platforms, we realized that they are not able to efficiently handle two main functions prerequisite for accelerating a variety of applications (XNOR, addition). As a result, such platforms impose an excessive latency and energy to memory chip, which could be alleviated by rethinking about SA circuit. Our key idea is to perform in-memory XNOR through a DRA method to alleviate and address three of the challenges discussed in Section 2.3. To achieve this goal, we propose a new reconfigurable SA, as shown in Fig. 4a, developed on top of the existing DRAM circuitry. It consists of a regular DRAM SA equipped with add-on circuits including three inverters and one AND gate controlled with three enable signals (EnM, EnX, EnC). This design leverages the charge-sharing feature of DRAM cell and elevates it to implement XNOR2 logic between two selected rows through static capacitive-NAND/NOR functions in a single cycle. To implement capacitor-based logic, we use two different inverters with shifted Voltage Transfer Characteristic (VTC), as shown in Fig. 4b.

In this way, a NAND/NOR logic can be readily carried out based on high switching voltage (Vc) low-Vc inverters with standard high-Vth/low-Vth NMOS and low-Vth/high-Vth PMOS transistors. It is
worth mentioning that, utilizing low/high-threshold voltage transistors a long with normal-threshold transistors have been accomplished in low-power application, and many circuits have enjoyed this technique in low-power design [22–25].

Consider \( D_i \) and \( D_j \) operands are RowCloned from data rows to \( x_1 \) and \( x_2 \) rows and both \( BL \) and \( BL \) are precharged to \( \frac{V_{dd}}{2} \) (Precharged State in Fig. 5). To implement DRA, DRIM’s ctrl first activates two \( WLs \) in computational row space (here, \( x_1 \) and \( x_2 \)) through the modified decoder for charge-sharing when all the other enable signals are deactivated (Charge Sharing State). During Sense Amplification State, by activating the corresponding enable signals \( (E_{MCD} \) and \( E_{SR} \) ) tabulated in Table 1, the input voltage of both low- and high-\( V_C \) inverters in the reconfigurable SA can be simply derived as \( V_i = \frac{n \cdot V_{dd}}{C} \), where \( n \) is the number of DRAM cells storing logic ‘1’ and \( C \) represents the total number of unit capacitors connected to the inverters (i.e. 2 in DRA method).

\[
\begin{array}{|c|c|c|c|}
\hline
\text{In-memory operations} & E_{MCD} & E_{SR} & E_{NC} \\
\text{Write/Copy/NOT/TRA} & 1 & 1 & 0 \\
\text{DRA} & 0 & 1 & 1 \\
\hline
\end{array}
\]

Table 1: Control bits status in Sense Amplification state.

Now, the low-\( V_C \) inverter acts as a threshold detector by amplifying deviation from \( \frac{1}{2} V_{dd} \) and realizes a NOR2 function as tabulated in the truth table in Fig. 4b. At the same time the high-\( V_C \) inverter amplifies the deviation from \( \frac{3}{4} V_{dd} \) and realizes a NAND2 function. Accordingly, XOR2 and XNOR2 functions of input operands can be realized after CMOS AND gate, respectively, on the \( BL \) and \( BL \) based on Equation-(1) in a single memory cycle.

\[
BL = (D_i, D_j) \cdot (D_i + D_j) = D_i \cdot D_j + D_i \cdot D_j = D_i \oplus D_j \\
\Rightarrow BL = D_i \oplus D_j
\]  \hspace{1cm} (1)

DRIM’s reconfigurable SA is especially optimized to accelerate X(N)OR2 operations, as well as supporting other memory and in-memory operations (i.e. Write/Read, Copy, NOT, and TRA). DRIM ctrl activates \( E_{MCD} \) and \( E_{SR} \) control-bits simultaneously (when \( E_{NC} \) is deactivated) to perform such operations. However, in this work, we only use Ambit’s TRA mechanism to directly realize in-memory majority function (\( \text{Maj3} \)).

\[
\begin{array}{|c|c|c|}
\hline
\text{Precharged state} & \text{Charge sharing state} & \text{Sense Amplification} \\
\text{Start} & \text{Start} & \text{Start} \\
\text{W1x1} & \text{W1x2} & \text{W1x3} \\
\text{Vdd} & \text{Vdd} & \text{Vdd} \\
\hline
\end{array}
\]

Figure 5: Dual Row Activation to realize XNOR2.

The transient simulation results of DRA method to realize single-cycle in-memory XNOR2 operation is shown in Fig. 6. We can observe how \( BL \) voltage and accordingly cell’s capacitor is charged to \( V_{dd} \) (when \( D_i, D_j = \overline{00} \)) or discharged to GND (when \( D_i, D_j = \overline{01} \)) during sense amplification state. Therefore, DRA method can effectively provide a single-cycle X(N)OR logic to address the challenge-1 and -2 discussed in Section 2.3 by eliminating the need for multiple operations, as well as row initialization steps.

- **In-Memory Adder**: DRIM’s sub-array can perform addition/subtraction (add/sub) operation quite efficiently. Assume \( D_i \), \( D_j \), and \( D_k \) as input operands, the carry-out \( (C_{out}) \) of the Full-Adder (FA) can be directly generated through \( \text{MAJ}(D_i, D_j, D_k) = D_i \oplus D_j \oplus D_i \cdot D_j \cdot D_k \) using TRA method. Moreover, the \( \text{Sum} \) can be readily carried out through two back-to-back XOR2 operations based on the proposed DRA mechanism.

\[
(D_i, D_j) = (0, 0) \quad (D_i, D_j) = (1, 0) \quad (D_i, D_j) = (1, 1)
\]

TRA- [2] or NOR-based [3] operations as well as row initialization steps.

**3.2 ISA Support**

While DRIM is meant to be an independent high-performance and energy-efficient accelerator, we need to expose it to programmers and system-level libraries to utilize it. From a programmer perspective, DRIM is more of a third party accelerator that can be connected directly to the memory bus or through PCI-Express lanes rather than a memory unit, thus it is integrated similar to that of GPUs. Therefore, a virtual machine and ISA for general-purpose parallel thread execution need to be defined similar to PTX [26] for NVIDIA. Accordingly, the programs are translated at install time to the DRIM hardware instruction set discussed here to realize the functions tabulated in Table 2. The micro and control transfer instructions are not discussed here.

DRIM is developed based on \( \text{AAP} \) primitives and most bulk bitwise operations involve a sequence of \( \text{AAP} \) commands. To enable processor to efficiently communicate with DRIM, we developed four types of \( \text{AAP} \)-based instructions that only differ from the number of activated source or destination rows:

1. \( \text{AAP} \) (src, des, size) that runs the following commands sequence: 1) \( \text{ACTIVATE} \) a source address (src); 2) \( \text{ACTIVATE} \) a destination address (des); 3) \( \text{PRECHARGE} \) to prepare the array for the next access. The size of input vectors for in-memory computation must
be a multiple of DRAM row size, otherwise the application must pad it with dummy data. The type-1 instruction is mainly used for copy and NOT functions; 2- AAP (src1, src2, des1, des2, size), 1) ACTIVATE a source address; 2) ACTIVATE two destination addresses; 3) PRECHARGE. This instruction copies a source row simultaneously to two destination rows; 3- AAP (src1, src2, des, size) that performs DRA method by activating two source addresses and then writes back the result on a destination address; 4- AAP (src1, src2, src3, des, size) that performs Ambit-TRA method [2] by activating three source rows and writing back the MAJ3 result on a destination address.

For instance, in order to implement the addition-in-memory, as shown in Table 2, three AAP-type2 commands double-copy the three input data rows to computational rows (x1, ..., x6). Then, the Sum function is realized through two back-to-back XOR2 operations with AAP-type3. The Ccount is generated by AAP-type4 and written back to the designated data row.

### 3.3 Reliability

We performed a comprehensive circuit-level simulation study to evaluate the effect of process variation on both DRA and TRA methods considering different noise sources and variation in all components including DRAM cell (BL/WL capacitance and transistor, shown in Fig. 7) and SA (width/length of transistors Vt). We ran Monte-Carlo simulation in Cadence Spectre with 45nm NCSU Product Development Kit (PDK) library [27] (DRAM cell parameters were taken and scaled from Rambus [28]) under 10000 trials and increased the amount of variation from ±0% to ±30% for each method. Table 3 shows the percentage of the test error in each variation. We observe that even considering a significant ±10% variation, the percentage of erroneous DRA across 10000 trials is 0%, where TRA method shows a failure with 0.18%. Therefore, DRIM offers a solution to alleviate challenge-3 by showing an acceptable voltage margin in performing operations based on DRA mechanism. By scaling down the transistor size, the process variation effect is expected to get worse [2, 17]. Since DRIM is mainly developed based on existing DRAM structure and operation with slight modifications, different methods currently-used to tackle process variation can be also applied for DRIM. Besides, just like Ambit, DRIM chips that fail testing due to DRA or TRA methods can be potentially considered as regular DRAM chips alleviating DRA yield.  

| Func | Operation | Command Sequence | AAP Type |
|------|-----------|-----------------|----------|
| NOT | D1 ← ¬D2 | AAP(D1, ¬D2) | 1        |
| MAJMIN | Dp ← MAJ(N1, D1, D2) | AAP(Dp, ¬D1, ¬D2) | 1        |
| XOR/| X0R2 | Dp ← D1 ∨ D2 | AAP(Dp, ¬D1, ¬D2) | 1        |
| AND/Sub† | Sum ← D1 ∨ D2 | AAP(D1, ¬D2) | 2        |

† Complement functions and Subtraction can be realized with dace rows.

### 3.4 Performance

**Throughput:** We evaluate and compare the DRIM’s raw performance with conventional computing units including a Core-i7 Intel CPU [13] and an NVIDIA GTX 1080Ti Pascal GPU [14]. There is a great deal of PIM accelerators that present reconfigurable platforms or application-specific logics in or close to memory die [29–49]. Due to the lack of space, we shall restrict our comparison to four recent processing-in-DRAM platforms, Ambit [2], DRISA-IT1C [3], DRISA-3T1C [3], and HMC 2.0 [11], to handle three main bulk-bit-wise operations, i.e., NOT, XOR2, and add. To have a fair comparison, we report DRIM’s and other PIM platforms’ raw throughput implemented with 8 banks with 512x256 computational sub-arrays. We further develop a 3D-Stacked DRAM with 256 banks in 4GB capacity similar to that of HMC 2.0 for the DRIM (i.e., DRIM-S) considering its computational capability. The Intel CPU consists of 4 cores and 8 threads working with two 64-bit DDR4-1866/2133 channels. The Pascal GPU has 3584 CUDA cores running at 1.5GHz [14] and 352-bit GDDR5X. The HMC has 32 vaults each with 10 GB/s bandwidth. Accordingly, we develop an in-house benchmark to run the operations repeatedly for 227/228/229-length input vectors and report the throughput of each platform, as shown in Fig. 8.

**Table 2:** The basic functions supported by DRIM.

**Figure 7:** Noise sources in DRAM cell. Glossary: Cwbl, Cs, and Ccross are WL-BL, BL-substrate, and BL-BL capacitance, respectively.

**Figure 8:** Throughput of different platforms (Y: log scale).

We observe that 1) either the external or internal DRAM bandwidth has limited the throughput of the CPU, GPU, and even HMC platforms. However, HMC outperforms the CPU and GPU with ~25x and 6.5x higher performance on average for bulk bit-wise operations. Besides, PIM platforms achieve remarkable throughput compared to Von-Neumann computing systems (CPU/GPU) through unblocking the data movement bottleneck. Regular DRIM (DRIM-R) shows on average 71X and 8.4X better throughput compared to CPU and GPU, respectively. 2) while DRIM-R, Ambit, and DRISA platforms achieve almost the same performance on performing bulk bit-wise NOT function, DRIM-R outperforms other PIMs...
in performing X(N)OR2-based operations. Our platform improves the throughput 2.3×, 1.9×, 3.7× compared with Ambit [2], DRISA-1T1C [3], and DRISA-3T1C [3], respectively. 3) DRIM-S can boost the throughput of the HMC by 13.5×. To sum it up, DRIM’s DRA mechanism could effectively address challenge-1 by proposing the high-through bulk bit-wise X(N)OR-based operation.

**Energy:** We estimate the energy that DRAM chip consumes to perform the three bulk bit-wise operations per Kilo-Byte for DRIM, Ambit [2], DRISA-1T1C [12], and CPU [1]. Note that, other operations such AND2/NAND2 and OR2/NOR2 in DRIM can be built on top of TRA method with almost the same energy consumption to that of Ambit. Fig. 9 shows that DRIM achieves 2.4× and 1.6× energy reduction over Ambit [2] and DRISA-1T1C [12], respectively, to perform bulk bit-wise XNOR2 operation. Besides, compared with copying data through the DDR4 interface, DRIM reduces the energy by 69×. As for bit-wise in-memory add operation, DRIM outperforms Ambit, DRISA-1T1C, and CPU, respectively, with ~2×, 1.7×, and 27× reduction in energy consumption.

![Energy consumption of different platforms](image)

**Figure 9:** Energy consumption of different platforms (Y: log scale).

- **Area:** To assess the area overhead of DRIM on top of commodity DRAM chip, four hardware cost sources must be taken into consideration. First, add-on transistors to SAs; in our design, each SA requires 22 additional transistors connected to each BL. Second, two rows of DCCs with two WL associated with each; based on the estimation made by [18], each DCC row imposes roughly one transistor over regular DRAM cell to each BL. Third, the 4:12 MRD overhead (originally 4:16); we modify each WL driver by adding two more transistors in the typical buffer chain, as depicted in Fig. 4a. Fourth, the Ctrl’s overhead to control enable bits; ctrl generates the activation hits with MUX units with 6 transistors. To sum it up, DRIM roughly imposes 24 DRAM rows per sub-array, which can be interpreted as ~ 9.3% of DRAM chip area.

4 DISCUSSION

- **Virtual Memory:** DRIM has its own ISA with operations that can potentially use virtual addresses. To use virtual addresses, DRIM’s ctrl must have the ability to translate virtual addresses to physical addresses. While in theory this looks as simple as passing the address of the page table root to DRIM and giving DRIM’s ctrl the ability to walk the page table, it is way more complicated in real-world designs. The main challenge here is that the page table can be scattered across different DIMMs and channels, while DRIM operates within a memory module. Furthermore, page table coherence issues can arise. The other way to implement translation capabilities for DRIM is through memory controller pre-processing of instructions being written to DRIM instruction registers. For instance, if the programmer writes instruction APP (src, dec, 256), then the memory controller intercepts the virtual addresses and translates them into physical addresses. Note that most systems have near memory controller translation capabilities, mainly to manage IOMMU and DMA accesses from I/O devices. One issue that can arise is that some operations are appropriate only if the resulting physical addresses are within specific plane, e.g., within the same bank. Accordingly, the compiler and the OS should work together to ensure that the operands of commands will result physical addresses that are suitable to the operation type.

- **Memory Layout and Interleaving:** While high-performance memory systems rely on channel interleaving to maximize the memory bandwidth, DRIM adopts a different approach through maximizing spatial locality and allocating memory as close to their corresponding operands as possible. The main goal is to reduce the data movement across memory modules and hence reducing operations latency and energy costs. As exposing a programmer directly to the layout of memory is challenging, DRIM architecture can rely on compiler passes that take memory layout and the program as input, then assign physical addresses that are adequate to each operation without impacting the syntaxics of the application.

- **Reliability:** Many ECC-enabled DIMMs rely on calculating some hamming code at the memory controller and use it to correct any soft errors. Unfortunately, such a feature is not available for DRIM as the data being processed are not visible to the memory controller. Note that this issue is common across all PIM designs. To overcome this issue, DRIM can potentially augment each row with additional ECC bits that can be calculated and verified at the memory module level or bank level. Augmenting DRIM with reliability guarantees is left as future work.

- **Cache Coherence:** When DRIM updates data directly in memory, there could be stale copies of the updated memory locations in the cache, thus data inconsistency issues may arise. Similarly, if the processor updates cached copies from memory locations that DRIM will process later, DRIM could actually use wrong/stale values. There are several ways to solve such issues in off-chip accelerators, the most common one is to rely on operating system (OS) to unmap the physical pages accessible by DRIM from any process that can run while computing in DRIM.

5 CONCLUSION

In this work, we presented DRIM, as a high-throughput and energy-efficient PIM architecture to address some of the existing issues in state-of-the-art DRAM-based acceleration solutions for performing bulk bit-wise X(N)OR-based operations i.e. limited throughput, row initialization, reliability concerns, etc. incurring less than 10% on top of commodity DRAM chip.

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