DMAPS: a fully depleted monolithic active pixel sensor — analog performance characterization

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ABSTRACT: Monolithic Active Pixel Sensors (MAPS) have been developed since the late 1990s based on silicon substrates with a thin epitaxial layer (thickness of 10–15 µm) in which charge is collected on an electrode, albeit by disordered and slow diffusion rather than by drift in a directed electric field. As a consequence, the signal of these conventional MAPS is small (∼1000 e−) and the radiation tolerance is limited. In this paper, the development of a fully Depleted Monolithic Active Pixel Sensors (DMAPS) based on a high resistivity substrate allowing the creation of a fully depleted detection volume is presented. This concept overcomes the inherent limitations of charge collection by diffusion in the standard MAPS designs. We present results from a prototype chip EPCB01 designed in a commercial 150 nm CMOS technology. The technology provides a thin (∼50 µm) high resistivity n-type silicon substrate as well as an additional deep p-well which allows to integrate full CMOS circuitry inside the pixel. Different matrix types with several variants of collection electrodes and pixel electronics have been implemented. Measurements of the analog performance of this first implementation of DMAPS pixels are presented.

KEYWORDS: Front-end electronics for detector readout; Radiation-hard detectors; Pixelated detectors and associated VLSI electronics

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1 Introduction

Monolithic Active Pixel Sensors (MAPS) have been proposed [1, 2] as tracking detectors for experiments in High Energy Physics (HEP) allowing high spatial resolution and a superior material budget compared to hybrid pixel detectors [3]. Unlike the latter, MAPS integrate both sensor and front-end (FE) electronics in a single silicon chip and thus do not require costly and often difficult chip-to-sensor interconnection. However, standard MAPS pixel sensors have two drawbacks which limit their area of application: first, in a standard CMOS process the common implant well configuration does not allow to use both transistor types (NMOS and PMOS) in the pixel area, thus severely limits the complexity of the electronics circuitry. To overcome this limitation, an additional implant must be added in the technology to isolate the electronics from the charge collection nodes as introduced for example in [4] and [5]. Second, the collection of charge, released from a particle or radiation, is accomplished by diffusion rather than by drift in an electric field and is hence slow, limiting the achievable time resolution (e.g. for time stamping) and rendering the sensor more vulnerable to bulk damage by non-ionizing radiation especially to levels required by LHC [6, 7]. The low resistivity of the silicon substrate in standard CMOS processes (typically about $10 \Omega \cdot \text{cm}$) only allows the creation of a very small depletion layer formed around the charge collecting p-n junction. Attempts have been made [8, 9] using epitaxial layers of a few $\mu$m high purity silicon to allow more charge to be collected. Some CMOS technologies allow using high voltage through which the silicon substrate can be depleted by $\approx 10 \mu$m [10], but the rest of the silicon remains undepleted. In this paper, an implementation of an advanced MAPS concept...
employing full CMOS (NMOS and PMOS) electronics in the active area of pixels using a high resistivity (detector-grade) silicon substrate is presented. This sensor concept is called DMAPS — Depleted Monolithic Active Pixel Sensor. The technology is introduced and the performance of test chip EPCB01 which contains different circuit variants is characterized with respect to analog performance and tolerance to ionizing radiation. The charge collection properties of the DMAPS sensor are investigated in a separate publication [11].

2 Test chip EPCB01

To investigate the concept of the DMAPS pixels and their applicability in experimental High Energy Physics (HEP), a prototype chip — EPCB01 has been designed, fabricated and tested. The fabrication process is a 150 nm CMOS process using a high resistivity (>2 kΩ·cm) n-type silicon substrate. The chip itself has been thinned down to a thickness of 50 µm. A schematic cross section of a DMAPS pixel is shown in figure 1.

A deep p-well is implanted in the n-type high resistivity silicon substrate forming a p-substrate for the integration of the front-end (FE) electronics. MOSFET transistors of both types are contained within an additional deep n-well, which isolates the transistors from the p-substrate and allows adjusting of potential of the p-substrate independently of the pixel electronics. The sensor backplane is heavily doped and forms a p+ region in the n-type substrate. The sensitive elements are implemented by n-wells implanted in the high resistivity n-type substrate. Although these n-wells (charge collection electrodes) do not form p-n junctions, they create regions with high electric potential and thus build up an electric drift field in the depleted bulk. The depletion region is formed between the p-substrate and the high resistivity n-substrate and between the p+ backplane and the high resistivity n-substrate (see figure 1). This technology allows biasing of the charge collecting n-wells with high voltage (HV_BIAS tested up to 15 V), while the FE electronics operates at 1.8 V. More information about the technology can be found in [12]. The collection electrode collects electrons, which are the preferred charge carriers due to their higher mobility compared to holes. In theory, if full depletion is achieved, a signal of approximately 4000 e− per Minimum Ion-
A single DMAPS pixel implemented in the EPCB01 can be divided in three sections: 1. high resistivity charge collection part biased with high voltage, 2. analog FE electronics and 3. digital logic for pixel configuration and read-out. Micrograph of EPCB01 and layout of one DMAPS pixel with highlighted functional blocks is shown in figure 2. The pixel size is 40×40 µm² and the charge collection electrode occupies 25% of the total pixel area. The circuitry inside a pixel contains about 160–180 transistors (depending on the pixel variant). Different pixel variants are labeled V1-V6 and they are described in table 1. A simplified schematic of each pixel variant is shown in figure 3.

The analog pixel FE electronics follows a similar scheme as the FE electronics commonly used in hybrid pixel detectors for HEP. One of the key parameters of tracking detectors in HEP are

**Table 1.** Different variants of the DMAPS pixel matrices implemented in EPCB01.

| Pixel variant | Biasing      | Coupling | FE architecture | Matrix dimensions |
|---------------|--------------|----------|-----------------|-------------------|
| V1            | resistor     | AC       | continuous      | 8 × 8             |
| V2            | diode        | AC       | continuous      | 8 × 8             |
| V3            | CSA feedback | DC       | continuous      | 6 × 8             |
| V4            | switched     | DC       | switched        | 6 × 8             |
| V5            | diode        | AC       | switched        | 8 × 8             |
| V6            | resistor     | AC       | switched        | 8 × 8             |
Figure 3. Six different variants of DMAPS pixel matrices (V1-V6) shown in figures a-f are implemented in EPCB01.

Signal to Noise Ratio (SNR) and uniform detection threshold, while linearity and spectroscopic performance are of less importance. The DMAPS implemented in EPCB01 have binary resolution of the signal amplitude (the pixel provides information whether it recorded a hit above the threshold or not). Standard MAPS often use 3 Transistor (3T) FE architecture (as described for example in [2]) to convert signal charge to voltage by a source follower. The charge conversion factor (gain) is at the first order given by the sum of the gate capacitance of the input transistor and by the capacitance of the charge collection electrode. In this case, the signal charge is shared between both capacitances depending on their capacitance ratio, which limits the achievable signal amplitude. Next limitation of this architecture arises from non-constant voltage of the charge collection electrodes. When the signal charge is collected by a 3T pixel, the voltage of the charge collection electrode will move by the same or higher voltage difference as the output voltage of the 3T circuit.

DMAPS pixels use rather a Charge Sensitive Amplifier (CSA) than the 3T circuit to convert the signal charge to voltage. In an ideal CSA (infinite open loop gain), the gain is given solely by its feedback capacitance. Vast majority of the signal charge is collected by the CSA and voltage of the charge collection node remains effectively constant. The CSA in the DMAPS pixels has been optimized to achieve high Signal To Noise Ratio (SNR). To maximize SNR, three parameters of the CSA has been optimized: feedback capacitance, width $W$ and length $L$ of the input transistor M1 (see figure 4) of the CSA. The optimum solution to achieve high SNR is small feedback capacitance represented only by a parasitic gate-drain capacitance of the input transistor of the CSA and minimum size input transistor ($W \times L = 320 \times 150 \text{ nm}^2$). In order to suppress effects of mismatch of minimum size transistors, the input transistor has dimensions of $W \times L = 400 \times 300 \text{ nm}^2$. The optimization has been done with expected capacitance of the charge collection electrode of 2 fF. However, concrete parameters (gain and noise) of the CSA are very much model dependent. A full schematic of the CSA implemented in pixel variant V2 is shown in figure 4.

Two different architectures of the analog FE electronics have been implemented — (time) continuous and switched. The continuous architecture uses a CSA with a continuous current source
Figure 4. Schematic of the CSA implemented in the pixel variant V2.

feedback followed by standard (time-continuous) discriminator. The switched architecture uses a CSA with a switched feedback and a clamp-and-sample circuit followed by a discriminator with regenerative feedback (sometimes called dynamic or clocked discriminator). Motivation for implementation of the clamp-and-sample circuit is reduction of the low frequency component of the noise. Resetting of the CSA, clamping and sampling is synchronous with a clock frequency of 1 MHz. Digital part of the pixel stores the configuration data for the analog part of the pixel and enables the read-out of the pixel matrix. Data read-out is implemented through a shift register.

4 Performance of the EPCB01 prototype chip

The (analog) performance of the DMAPS pixels was studied by an external charge injection with an in-pixel 2 fF injection capacitor as well as with radioactive source $^{90}$Sr.

4.1 Gain determination with charge injection

Pixel electronics in all pixel matrices except V4, which does not contain an injection capacitor, have been examined by external charge injection. The DMAPS pixels provide information whether the signal is above or below the detection threshold and effectively encode the signal with 1-bit resolution. Measurement of the gain of the CSAs integrated in the pixels has been done by multiple charge injections while sweeping the discriminator threshold voltage VREF. Number of hits, recorded at a constant threshold ($n_{\text{hits}}$), as a function of the threshold has been fitted by a function described by the following formula:

$$n_{\text{hits}}(\text{VREF}) = n_{\text{hitsMax}} \cdot \frac{1}{2} \left( 1 - \text{erf} \left( \frac{\text{VREF} - \text{VREF}_{50\%}}{\sqrt{2} \cdot \sigma} \right) \right).$$
$n_{\text{hitsMax}}$ is the number of injected charge pulses at constant threshold voltage $V_{\text{REF}}$. $V_{\text{REF}50\%}$ is the threshold voltage at which 50% of the of the hits is above the threshold. $\sigma$ describes the standard deviation of the noise voltage of the CSA measured with the threshold scan. \textit{erf} is the error function defined by the following formula:

$$\text{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} \, dt.$$  

An example of the of two threshold scans when injected charge is 0 e\(^-\) (baseline) and 1000 e\(^-\) is shown in figure 5.

Gain of the charge sensitive amplifier was then extracted by using the following formula:

$$\text{gain}(Q) = \frac{V_{\text{REF}50\%}(Q) - V_{\text{REF}50\%}(Q = 0)}{Q}.$$  

During the measurements, a high bias voltage of 11 V (HV\_BIAS) was connected to the charge collection electrodes to keep the silicon substrate depleted. P-substrate and the chip backplane were biased with negative voltage of $-1.5$ V. The best analog performance has been achieved with the DMAPS pixels V2, which will therefore be the design variant on which this paper is mainly focused to. In general, the pixel variants with a continuous rather than a switching circuit architecture have better performance than the switched variants. Significant area and power limitation in DMAPS design do not allow using rail-to-rail discriminator or precise voltage adder to implement functionality of in-pixel threshold adjustment (TDAC). Therefore the gain of the pixel variants V1, V2 and V3 have been further corrected by non-linearity of the source follower integrated in the TDAC (see section 4.3 for more details about the TDAC) and by voltage offset of the discriminator. This correction is based on data obtained from design simulation. The switched variants suffer from a large parasitic charge injection originating from the dynamic (clocked) discriminator. Figure 6 describes the clamp-and-sample circuit and path of the parasitic charge. When the discriminator samples the signal on the rising edge of CLK signal, the clamping capacitor is discharged by a large amount of parasitic charge injected from the discriminator. The clamping capacitor is implemented by MOSCAP capacitor. Capacitance of the MOSCAP depends on the voltage applied on its terminals. When the signal at the output of the CSA is large, voltage difference across the MOSCAP is small and its capacitance is also small. When this signal is sampled by the discriminator, the
Figure 6. Dynamic discriminator in pixels V5 and V6 injects parasitic charge into the MOSCAP capacitor and degrades the analog performance of the switched pixel variants.

Figure 7. Mean gain of the FE electronics integrated in the DMAPS pixel matrices. Size of the error bars was scaled down by factor of 2.

Voltage across the MOSCAP is lowered by a higher amount compared to the situation when the signal from the CSA is small. This effect is responsible for gain decline of the pixel variant V5.

The gain curves of the pixel variants V5 and V6 were not corrected by the non-linear effects of the clamp-and-sample circuit due to significant model and bias setting dependence. Figure 7 shows the resulting gain of the FE electronics in various DMAPS pixel matrices as a function of the injected charge. Each point represents a mean gain of all pixels of the particular pixel matrix and its error bar corresponds to a standard deviation of the gain arising from gain variations from pixel to pixel within the matrix. The error bars have been down-sized by a factor of 2 to keep the graph readable.

The highest gain of 91 μV/e− measured after the injection of 1 ke− (typical operating threshold) was achieved with the pixel matrix V2. The gain dispersion of the pixels within the matrix variant V2 is 17 μV/e−. Origin of the gain dispersion is mismatch of parameters of the electronic components on the chip. Particularly interesting is comparison of gain of the matrices V1 and V2. The FE electronics in both matrices is identical (including the layout). The shape of the gain dependence on the injected charge (gain curve) is similar in both cases, but they are shifted by 18 μV/e− on average. The gain shift most likely emerges due to the different capacitances of the collection
electrodes used in these pixel variants. A schematic cross section of the collection electrode used with diode biased variants (V2, V5) is shown in figure 8. Layout of the collection electrodes used in all other pixel variants has been provided by the foundry after design submission and the designers do not have access to the exact layout parameters. However, if the design of this collection electrode contains wide n-well or n+ diffusion it can easily increase capacitance of the collection electrode. The CSA uses a common source stage implemented by the transistors M1 and M2 (see figure 4) with a relatively small open loop gain of about 76 in the all pixel variants. Therefore the closed loop gain is sensitive to the sensor capacitance. Even greater shift in gain was observed in case of V3 with respect to V2. The collection electrode in V3 is DC coupled to the FE electronics and is biased by a voltage of about 370 mV provided by CSA feedback. The collection electrode is not fully depleted at this voltage. Therefore the capacitance is even higher than in V1 and the gain is therefore smaller. Almost the same shifts (for small signals) of the gain-curves have been observed in case of V5 and V6. However, the character of the non-linearity of the switched variants is different compared to the continuous variants. The gain-curves of V5 and V6 are not equidistant. The reason for different non-linearity of V5 and V6 could be due to their different gain. Since the pixels of variant V5 have higher gain, these pixels reach the point when the MOSCAP looses its capacitance at smaller injected charge than pixels of variant V6.

4.2 Noise performance

The noise performance of the DMAPS pixels has been determined by threshold scans and s-curve fits and evaluated in terms of Equivalent Noise Charge (ENC). ENC as a function of injected charge is displayed in figure 9.

The lowest noise was measured with the matrix V2. The differences of the ENC-curves of the matrices V1, V2 and V3 can be attributed to the differences of the sensor capacitance. Each of the switched variants behaves differently in terms of noise. At the beginning of the dynamic range, the noise of V5 is comparable with its continuous counterpart (V2) and increases with increasing signal, because at the same time the gain decreases. The noise of the pixel variant V6 is much higher than in case of V5 and might be caused by incomplete reset of the CSA during the reset phase due to possible instability of the CSA due to excessive input capacitance.

Random Telegraph Signal noise (RTS) represents a significant noise component of all variants of the DMAPS pixels in EPCB01. Spikes caused by the RTS are clearly visible in figure 10. RTS noise is not a speciality of EPCB01 only. The RTS noise often appears in monolithic pixels as described for example in [13] and [14].
Figure 9. Mean ENC of the FE electronics integrated in the DMAPS pixels. Size of the error bars has been scaled down by a factor of 2.

Figure 10. RTS noise observed at the analog output of the DMAPS pixel.

4.3 Threshold dispersion

The HEP applications require a uniform detection threshold across the pixel matrix. Dispersion of the threshold originates from the fabrication process variations and mismatch of the integrated electronic components. These process related effects are responsible for dispersion of the quiescent voltage at the output of the CSA (baseline dispersion) and also for dispersion of the voltage offset of the discriminator both contributing to the dispersion of the detection threshold. Each DMAPS pixel contains a 4-bit DAC (TDAC) for threshold equalization. The implementation of the TDAC is different in the continuous variants (V1, V2 and V3) and in the switched variants (V4, V5 and V6). The continuous variants use a resistive TDAC embedded in a source follower as shown in figure 11 (a). The advantage of the resistive TDAC is the possibility to adjust the threshold equalization range if needed. However, the output voltage of the TDAC is not perfectly linear function of the input voltage, resistors occupy a large area in the pixel and the entire TDAC consumes an
Figure 11. Two different variants of a discriminator with TDAC have been implemented in EPCB01. A continuous discriminator with resistive TDAC (a) and a dynamic discriminator with switched capacitors TDAC (b).

Figure 12. Threshold dispersion of the DMAPS pixels of variant V2 before (a) and after threshold equalization (b).

additional power. The switched variants use a two stage dynamic discriminator. The input voltage offset of the dynamic discriminator is very sensitive to the capacitance of the routing. This fact has been used in the design of a switched capacitor TDAC as shown in figure 11 (b).

By adjusting the capacitance between two branches of the discriminator, the voltage offset (detection threshold) can be adjusted. This TDAC does not introduce non-linearity to the threshold setting. In addition, this TDAC is very compact in the pixel layout and does not increase the power budget of the pixel. Both variants of the TDAC have been proven to significantly reduce the threshold dispersion. The distributions of a 1 ke\(^{-}\) threshold setting before and after threshold equalization of pixels of variant V2 is shown in figure 12 (a, b) and threshold dispersion of variant V5 is shown in figure 13 (a, b).

4.4 Cluster size measurement

In a fine-pitch pixel sensor, the signal charge originating from an ionizing particle diffuses on its path to the collection electrode. The signal charge can be collected by a cluster of neighboring pixels, the size of which depends on the depleted thickness of the traversed sensor. The cluster size was measured using the DMAPS pixels upon radiation from a \(^{90}\)Sr radioactive source. The cluster
analysis has been performed with the DMAPS pixel array of V2 at several sensor bias voltages (HV_BIAS). The detection threshold has been set to 1 ke\textsuperscript{−} and has been equalized over the matrix. Distributions of the cluster size measured at bias voltages of 2 V and 11 V are shown in figure 14.

By comparing these distributions, it is visible that at 2 V bias voltage 29\% fewer events are recorded than with a bias voltage setting of 11 V. Events from \(^{90}\)Sr are predominantly single pixel clusters. However, double pixel clusters become more pronounced at 11 V than at 2 V. Notwithstanding the possibility that due to slower charge collection at low bias and hence signal loss due to the amplifier discharge leading to a smaller number of double pixels at low bias we believe that the decrease at high bias indicates a different origin. At high bias voltage, the sensor depletes leading to a larger charge spread by diffusion broadening when the depletion depth becomes larger hence leading to more double hit clusters.

Figure 15 shows the ratio of single to double pixel clusters as a function of the sensor bias voltage. This ratio decreases with increasing sensor bias voltage and saturates at a voltage of 6 V, while the event rate does not increase beyond this point. At a voltage of 6 V and above, the sensor does not collect any more charge and the cluster size ratio remains roughly constant. With the caveat mentioned above this is an indication of full depletion. Given a sensor thickness of 50 \(\mu\)m, a depletion voltage of 6 V would indicate a substrate resistivity of 4.5 k\(\Omega\) \cdot c, which corresponds to a bulk doping density of approximately \(3 \cdot 10^{12}\) cm\(^{-3}\).
4.5 Rise-time

DMAPS are potentially fast sensors in terms of charge collection time because DMAPS use drift rather than diffusion as a charge collecting mechanism. Direct measurement of the charge collection time is rather difficult to perform with EPCB01 because the analog signal is available only from one pixel in each DMAPS matrix and the pixel lies at the edge of the matrix and unwanted edge effects may play role. Upper limit on the charge collection time is given by the rise-time of the signal measured at the output of the CSA. The rise-time has been measured as a time difference between 25% and 75% of the full signal amplitude and two signal sources have been used: radioactive source $^{90}\text{Sr}$ and external charge injection of 3 ke$^-$ as a reference. The charge injection was performed with analog multiplexer with slew rate of 540 V/$\mu$s into injection capacitor of 2 fF. The physical charge injection into the CSA input is slower due to the parasitic capacitance and resistance of the routing in the chip and is expected to be 2.8 ns (injection time from 25% to 75% of the total injected charge). The mean signal rise-time at the analog output of the CSA in DMAPS pixel measured with charge injection is 14.2 ns (see figure 16 (a)). The events recorded from $^{90}\text{Sr}$ have been processed and only events with signal between 2.7–3.3 ke$^-$ have been used in the analysis to suppress rise-time dependence on the signal amplitude. The mean rise-time measured with $^{90}\text{Sr}$ is 19.5 ns (see figure 16). The relatively small difference between rise-time measured with charge injection and radioactive source indicates that charge collection time from DMAPS pixels is in order of several nanoseconds. For comparison, the charge collection properties of conventional MAPS based on epitaxial layer of various thickness are presented in [9].

5 Radiation tests

Radiation tolerance of the test chip EPCB01 has been investigated with irradiation from an X-ray tube with end-point energy of 60 keV. The irradiation has been performed within several steps achieving a total ionizing dose of 50 Mrad. After each irradiation period the chip has been annealed for 100 minutes at 80°C. Several tests of the analog and digital part of the pixels have been performed after each irradiation period. Radiation induced effects have only been observed in the analog part of the FE electronics. The most sensitive node of the analog part of the DMAPS pixel is the NMOS feedback transistor in the CSA. Radiation induced shift of the threshold voltage
Figure 16. Rise-time measured with an external charge injection of 3 ke$^{-}$ (a) and with radioactive source $^{90}$Sr (b).

Figure 17. Signal pulse at the output of the CSA (V2) shortens after irradiation.

of the feedback transistor changes the discharge time of the CSA. The greatest difference of the discharge time has been observed between an unirradiated state and after the first irradiation period (200 krad), then the discharge time changed only insignificantly up to 50 Mrad as can be seen in figure 17. The X-ray irradiation has an overall impact on the FE electronics in terms of changes of gain and noise level of the DMAPS pixels. The dependence of these parameters on the level of irradiation is shown in figure 18 (a, b). The digital part of the DMAPS pixels has been tested between irradiation periods by writing test data patterns in the configuration shift register and reading them back. No difference has been observed in the data patterns passing the configuration register of the irradiated chip EPCB01.

An additional radiation study has been done with an array of individual NMOS and PMOS transistors which is part of EPCB01. All transistors in the array have constant channel length of 150 nm but variable channel width. The NMOS transistor with channel width of 3070 nm has enclosed layout geometry while all other transistors have standard layout. Radiation induced shift of threshold voltage has been observed as well as degradation of transconductance of the transistors.
Figure 18. Gain (a) and noise (b) of the DMAPS pixels as a function of X-ray radiation dose. Error bars have been reduced by factor of 2.

Figure 19. Threshold voltage shift $\Delta V_{th}$ (a) and transconductance (b) of MOSFET transistors as a function of total ionizing dose. Transistors differ by channel width $w$ while channel length remains constant (150 nm).

Both results are shown in figure 19 (a, b). Threshold voltage of both transistor types shifts by less than 30 mV within the range of radiation dose. Maximum transconductance of the NMOS transistors degrades by less than 2% and in case of PMOS transistors transconductance degrades by less than 15%. In general, the radiation effects are more significant in small channel width transistors.

6 Summary

A novel concept of Depleted Monolithic Active Pixel Sensors (DMAPS) has been introduced. DMAPS pixels integrate a complex “hybrid pixel like” CMOS electronics and simultaneously benefit from a fully depleted sensor within the same substrate. A commercial CMOS process has been used for fabrication of a prototype DMAPS chip — EPCB01. First tests indicate good functionality of this detector concept, while there is ample room for improvement of the FE electronics. The best performance has been achieved with an AC coupled diode biased collection electrode connected to the time-continuous FE electronics. The gain is $\approx 90 \mu$V/e$^-$, the noise is $\approx 40$ e$^-$ with a discharge time of about 1 $\mu$s. The threshold dispersion after equalization is 135 e$^-$. The RTS noise
has been observed in all variants of the DMAPS pixels and most likely emerges from fluctuations of current of close to minimum size transistors used in the FE electronics. The depletion voltage of the high resistivity substrate has been determined by the means of cluster size saturation to be approximately 6 V. Measurement of the signal rise-time from the DMAPS pixels places an upper limit of 19.5 ns on charge collection time of the signal of $^{90}\text{Sr}$ from depleted 50 $\mu$m thick silicon substrate. Small radiation effects have been observed in the performance of the analog FE electronics after absorbing the X-ray radiation dose of 50 Mrad. More measurements need to be done to fully understand the DMAPS pixels. In particular, more radiation test are needed to learn about the radiation effects in the charge collecting part and evaluate suitability of DMAPS sensors for their applications in HEP experiments. However, important lessons have already been learned during the design and testing of the EPCB01 and they will be addressed in the next generation of the DMAPS test chip.

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