Proximu$: Efficiently Scaling DNN Inference in multi-core CPUs through Near-Cache Compute

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Abstract

Deep Neural Network (DNN) inference is emerging as the fundamental bedrock for a multitude of utilities and services. CPUs continue to scale up their raw compute capabilities for DNN inference along with mature high performance libraries to extract optimal performance. While general purpose CPUs offer unique attractive advantages for DNN inference at both datacenter and edge, they have primarily evolved to optimize single thread performance. For highly parallel, throughput-oriented DNN inference, this results in inefficiencies in both power and performance, impacting both raw performance scaling and overall performance/watt.

We present Proximu$, where we systematically tackle the root inefficiencies in power and performance scaling for CPU DNN inference. Performance scales efficiently by distributing light-weight tensor compute near all caches in a multi-level cache hierarchy. This maximizes the cumulative utilization of the existing bandwidth resources in the system and minimizes movement of data. Power is drastically reduced through simple ISA extensions that encode the structured, loop-y workload behavior. This enables a bulk offload of pre-decoded work, with loop unrolling in the light-weight near-cache units, effectively bypassing the power-hungry stages of the wide Out-of-Order (OOO) CPU pipeline.

Across a number of DNN models, Proximu$ achieves a $2.3 \times$ increase in convolution performance/watt with a $2 \times$ to $3.94 \times$ scaling in raw performance. Similarly, Proximu$ achieves a $1.8 \times$ increase in inner-product performance/watt with $2.8 \times$ scaling in performance. With no changes to the programming model, no increase in cache capacity or bandwidth and minimal additional hardware, Proximu$ enables unprecedented CPU efficiency gains while achieving similar performance to state-of-the-art Domain Specific Accelerators (DSA) for DNN inference in this AI era.

I. INTRODUCTION

New data-centric paradigms of compute have made machine learning (ML) and Deep Neural Networks (DNN) pervasive in all fields of human endeavor. The race to build the optimal hardware for DNN execution continues with custom Domain Specific Accelerators (DSA), programmable FPGAs and general purpose GPUs and CPUs all throwing their hats in the ring. CPUs offer unique attractive advantages for DNN inference in the datacenter and also at the edge. Advances in DNN-inference topologies and algorithms continue at a rapid pace. The programmable general-purpose nature of CPUs with their rich and mature ecosystem of tools and programming models allows for implementation of functionality that is not present in custom DNN hardware, enabling quick development and deployment. Additionally, DNN topologies do not exist in a vacuum and a tight coupling of DNN and non-DNN tasks is required to meet strict inference latency requirements for sufficient quality-of-service to the end users. Software driver-based offload of DNN-inference tasks to a separate piece of hardware (DSAs, GPUs) incurs unacceptable latency and memory costs. Hence CPUs are better suited to real time DNN-inference tasks. DNN tasks with limited parallelism, like Recurrent NNs, fit more naturally to CPUs which have few fast cores, than to GPUs which have many slow cores. Finally, the wide prevalence of CPUs already in datacenters provisioned for peak load levels in conjunction with diurnal load cycles, leads to the abundant availability of “free” CPU compute for DNN-inference. Hence, efficient scaling of DNN-inference on CPUs is highly crucial both for meeting customer Service-Level Agreements (SLAs) and enabling Total Cost of Ownership (TCO) savings for datacenter providers as applications using DNNs proliferate.

However, modern CPUs have evolved to optimize primarily for single thread performance. The conventional CPU organization involves wide and deep OOO cores, with all compute placed “monolithically” atop a serially accessed multi-level cache hierarchy designed to minimize average load latency. While each cache level is potentially an independent source of bandwidth, all loads and stores must go through the L1 cache, thus restricting it to be the primary source of bandwidth. Furthermore, every instance of every instruction across all loop iterations in the workload is unrolled and travels through the entire CPU pipeline, consuming a significant amount of power.

DNN-inference primitives like convolution, inner-product are highly structured and repetitive, with any invocation having a number of fixed iteration count loops. They are also heavily data-parallel with performance governed by raw compute throughput and a required data throughput (bandwidth) to feed it. Generational compute scaling in CPUs is achieved via both intra-core scaling and multi-core scaling. The required bandwidth to feed the compute
however, depends on primitives themselves; the higher the compute intensity (Ops/Byte) the lower the bandwidth required, and vice-versa. As DNN usages and topologies evolve, there is an increasing heterogeneity in their Ops/Byte (Compute/Bandwidth) requirements.

The monolithic core-centric CPU organization results in sub-optimal performance, resource utilization and power when executing DNN primitives with diverse Ops/Byte requirements. Matrix-Matrix primitives (like convolution) illustrated in Figure 2 typically have high Ops/Byte. High reuse and hit-rate in the L1 cache delivers sufficient bandwidth to achieve close to peak compute efficiency. However, serialized accesses through the hierarchy means the L2 and L3 cache bandwidths are heavily underutilized. Matrix-Vector primitives (like inner-product), shown in Figure 3 have much lower Ops/Byte. Low hit-rates and bandwidth from small L1 caches result in low compute efficiencies. In fact, any data movement into the L1 is essentially wasteful and puts unnecessary pressure on outer cache levels while consuming power. Larger L2 caches have higher hit-rates resulting in spare L3 bandwidth. Power consumption is dominated by the unrolled fetch, decode, allocate and dispatch of every instruction despite the repetitive structured nature of execution.

We present Proximu$, where we systematically tackle the root inefficiencies in power and performance scaling for CPU DNN inference. Performance scales efficiently by distributing light-weight tensor compute near all caches in a multi-level cache hierarchy. This maximizes the cumulative utilization of the existing bandwidth resources in the system and minimizes unnecessary movement of data across the hierarchy. We leverage the structured and repetitive nature of DNN-inference primitives to define simple “Proximity Support Extensions” (PSX) to the ISA that condense and encode multiple levels of loops. The core does fewer fetches and decodes, with a bulk offload of decoded tensor work (load/store/compute) to the light-weight near cache “Tensor Functional Units” (TFU). With unrolled tensor execution within the TFU, a majority of the power-hungry stages of the OOO CPU pipeline are effectively bypassed, drastically reducing power. We further leverage the PSX extensions and Simultaneous Multi Thread (SMT) capabilities of the CPU to distribute work across threads and cores with no changes to the CPU programming or memory model.

We make the following key contributions in this paper.

- We do a fundamental analysis of state-of-the-art implementations of multiple DNN-inference primitives executed on state-of-the-art datacenter CPUs, and identify key bottlenecks to performance scaling and performance/watt efficiency.
- We present Proximu$, where we distribute light-weight Tensor Functional Units, near each level of cache. Proximu$ maximizes efficient utilization of the existing cumulative bandwidth in the system and minimizes data movement. Proximu$ adds minimal additional hardware with no increase in cache capacity or bandwidth to the CPU, while scaling performance to levels matching state-of-the-art DNN DSAs.
- We develop simple “Proximity Support Extensions” to the ISA that condense and encode multiple loops of fixed iteration count information. This effectively ensures that unnecessary power-hungry stages of the OOO CPU pipeline are effectively bypassed and all work (unrolling and execution) is performed in close proximity to the data, drastically improving achieved performance/watt.
- By leveraging the PSX extensions and existing SMT capabilities of cores, Proximu$ requires no change to the CPU programming or memory model.

Evaluated across multiple DNN models, Proximu$ achieves a $2.3 \times$ improvement in convolution performance/watt with a $2 \times$ to $3.94 \times$ scaling in raw performance. Similarly, Proximu$ achieves a $1.8 \times$ increase in inner-product performance/watt with $2.8 \times$ performance. With no changes to the programming model, no increase in cache capacity or bandwidth and minimal additional hardware, Proximu$ enables unprecedented CPU efficiency gains and TCO savings for datacenters while matching performance levels of state-of-the-art DNN DSAs.
II. CHARACTERIZATION AND OPPORTUNITY

We first perform an in-depth power and performance characterization of multiple primitives common to DNN inference on state-of-the-art CPU configurations. The goal is to derive insights that can lead to efficient performance and performance/watt scaling.

A. Programming and Execution Model

Figure 4 depicts the overall flow currently followed when implementing DNN models. Models are specified in frameworks like Tensorflow [27], Caffe [44], PyTorch [20], MXNet [4], OpenVino [19] etc. These frameworks provide developers with easy-to-use APIs to describe topologies and model parameters while abstracting away the underlying hardware. The frameworks in-turn leverage highly-optimized, platform-specific libraries like Intel MKL-DNN [13] [24] [12], AMD’s BLIS or libFLAME [10], ARM’s compute libraries [5] and Nvidia cuDNN [17] to extract maximum performance from the underlying hardware. The inner-most loops of DNN primitives are typically implemented in a vectorized, highly optimized (often JITed [37]) manner for optimal performance and maximum data reuse (Figure 5). The outer-most loops in the primitives are parallelized using well established threading run-times (OpenMP [18], TBB [15]) to distribute work across compute cores in the target hardware.

B. Performance and Power Analysis

We evaluate state-of-the-art MKL-DNN [13] primitives (up to 198X performance improvement [3]) on state-of-the-art CPU configurations across multiple DNN topologies. We focus on int8 data types since several seminal studies [38] have shown that 8 bit (or lower) precision is sufficient for inference accuracy. The use of lower precisions reduces dependence on expensive off-chip DRAM bandwidth with the remaining bandwidth bottlenecks becoming mostly on-die thereafter.

The compute intensity or Ops/Byte property of any DNN primitive plays a fundamental role in determining its bandwidth requirements (and hence compute efficiency) from the system. This metric needs to be evaluated at multiple levels of abstraction:

- **Algorithm:** The theoretical peak Ops/Byte is based on the work being performed if we had an “infinite” register file (RF) holding data. For example, in 1x1 convolution (Figure 5), every weight element is reused across all input plane elements in the same input channel (for different output plane elements). Similarly, input and output elements also have peak possible reuse opportunities (shown in Figure 5).

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1. Our evaluation methodology and workloads are described in detail in Section IV.
### TABLE I: ResNet-50 Convolution and Transformer Inner Product Characterization

| Metric | ResNet50 Convolution | Transformer InnerProduct |
|--------|-----------------------|--------------------------|
| **Ops/Byte: Based on Algorithm** | | |
| Input  | 1021  32  4608  1727  1024  33708 | | |
| Weight | 2245  100  25600  1  1  1 | | |
| Output | 998  64  4608  2057  1024  33708 | | |
| **Memory Transactions/Op-Instr: Based on Kernel** | | |
| Loads  | 0.49  0.39  0.69  1.35  1.19  1.41 | | |
| Stores | 0.058  0.003  0.25  7E-04  3E-05  9E-04 | | |
| **Hardware: Performance (Peak 2*64 MAC/Cycle)** | | |
| Ops/Cyc | 120.4  100.0  127  12.99  8.81  14.02 | | |
| **Hardware: On-Die Cache Hit-Rate** | | |
| L1 $ | 86%  57%  98%  23%  15%  26% | | |
| L2 $ | 88%  51%  99%  72%  0%  100% | | |
| L3 $ | 99.4%  97.6%  99.5%  99%  64%  100% | | |
| **Hardware: Data Movement Overhead** | | |
| L1-L2 | 20%  1%  69%  106%  81%  121% | | |
| L2-L3 | 2%  0.3%  5.8%  47%  27%  99% | | |
| Total | 22%  2%  71%  156%  147%  181% | | |

- **Kernel**: The software implementation that extracts reuse out of the finite RF of the compute core and depends on the RF size and the data-flow implemented. This determines the minimum number of loads and stores to be executed. For the kernel example in Figure 5, the number of weight loads (reused across inputs in the inner-most loop) and the number of iterations of the innermost loop (reusing weights to compute different outputs) is governed by the RF size.

- **Hardware**: The kernel execution on the underlying hardware, where on-die cache hit-rates determine bandwidth delivery to the core and the cross-cache data movement incurred. We define Data Movement Overheads introduced by the hardware as the ratio of cumulative cross-cache data movement (fills and evictions) to the loads and stores to/from the compute core’s RF (determined by the kernel).

1) **Convolution Characterization**: Convolution is essentially a high Ops/Byte matrix-matrix operation. We evaluate the optimized MKL-DNN option that allows for fusing of the convolution and ReLU (non-linear function on the output) primitives. Table I details our characterization of the convolution primitive across all convolutional layers of ResNet-50 [40] and shows several interesting insights. First, the MKL-DNN convolution kernels subsume most of the variability in Ops/Byte across layers through reuse within the core’s RF. The kernels employ output-stationary data-flows, requiring very low store bandwidth (Stores/MAC-Instr). Interestingly, input and weight reuse variability is also subsumed within the RF resulting in a fairly steady 0.5 Loads/MAC-Instr requirement across all layers. Second, high average L1 hit-rates (86%) result in high compute efficiency (120 MACs/cycle out of a peak 128 (Intel CascadeLake cores have two 64 MAC/cycle execution units per core)). Fills and evictions at the L1 cache still add an average 20% overhead in data movement. The conv1 layer has poor L1 hit-rate, adding 69% data movement overhead at L1, dropping performance to 50 MACs/cycle.

**Performance Opportunity**: High L1 hit-rates coupled with the 0.5 loads/MAC-instr requirements means that we use only about 60% of available L1 bandwidth (2 loads/cycle/core at L1 for Intel CascadeLake). Furthermore, the L2 and L3 bandwidths are still hugely under-utilized. This can be exploited by placing tensor compute near each of these caches, enabling further scaling of performance without any increase in overall on-die capacity or bandwidth. More re-use directly from these caches would also reduce data movement to the L1 caches. The 0.5 loads/MAC-instr requirement and peak bandwidths of each cache determines the peak compute required near each cache level.

2) **Inner-Product Characterization**: Inner-Product primitives involve matrix-vector operations and have lower peak Ops/Byte compared to convolutions. These primitives are prominent in Recurrent DNN models and Sequencer-to-Sequence models (eg. Transformer [59]) which are heavily used in applications like natural language processing. Table I also details our inner-product characterization for all layers in Transformer. This primitive has a poor 23% L1 hit-rate, which coupled with a high 1.35 Load/MAC-instr bandwidth requirement results in low compute efficiency achieving only 13 MACs/cycle. Furthermore, we see up to a whopping 156% overhead in cross-cache data movement.

**Performance Opportunity**: While L1 hit-rates are low, hit-rates in the larger L2 (1MB) and L3 (1.375MB per core) are significantly better. Tensor compute placed directly near these caches, bypassing the small L1 entirely, would leverage the higher hit-rates for higher bandwidth to feed the compute. Along with eliminating all data movement to an under-sized L1, we would see better performance, with no increase in cache capacity or bandwidth.

3) **Pooling/Concat**: We also evaluate Pooling (dimensionality reduction) and Concat primitives and they mainly involve data movement with low data reuse. For example, models like DenseNet-169 [43] pass lower level features
(outputs) directly to later layers as inputs, using the Concat primitive to prepare data. Near L2 and/or L3 caches execution would reduce this data movement cost.

4) Power Analysis: Figure 6 shows the contribution to total power from various clusters in the CPU. CPUs unroll every instance of every instruction in each iteration of all loops into every stage of the CPU pipeline. Despite the structured, fixed iteration count loopy nature of the DNN kernels (Figure 5) all instructions go through fetch and decode, allocation and dispatch. Register allocation and renaming (RAT) and OOO dispatch (from RS) is extremely expensive in power for wide and deep OOO cores. For compute bound ResNet-50, these stages contribute to 60% of total power! For bandwidth bound inner-product primitives in Transformer, they contribute to 50% of total power with cache and data movement adding another 45%.

![Fig. 6: Stackup of Power Consumption in Convolution Dominated ResNet50 and Inner Product Dominated Transformer](image)

**Power Opportunity:** With structured and repetitive DNN kernels, loop unrolling should happen in a “lean” scheduler, close to the tensor compute. Using a “macro”-ISA that encodes this loop information, the CPU can offload multiple loops of decoded (but not unrolled) work to the “lean”, low-cost near-cache compute effectively bypassing power-hungry stages of the legacy CPU pipeline for most of the execution.

5) Summary: Table II concludes this section by summarizing our main observations for performance and power. A heterogeneity in characteristics across various primitives leads to sub-optimal performance and/or resource utilization in the CPU. Optimally executing primitives near caches best suited to their requirements can provide performance, power and resource utilization benefits. Furthermore, we should leverage the structured, fixed iteration count loop nature of the workloads to bypass or minimize usage of the power-hungry front-end stages of the legacy CPU pipeline - preferably unrolling and scheduling pre-decoded instructions near the execution units.

**TABLE II: Primitive Characterization Summary**

| Primitive            | Observations                                                                 | Data Movement Overhead | Opportunity                                      |
|----------------------|------------------------------------------------------------------------------|------------------------|--------------------------------------------------|
| Convolution          | Bandwidth over-provisioned w.r.t. compute, Under-utilization of L2/L3 Bandwidth | Mostly at L1-L2        | Perform tensor compute near all caches (L1,L2,L3) |
| Inner-product        | Compute over-provisioned w.r.t. bandwidth, Poor hitrate at 32KB L1          | High at L1-L2 and L2-L3| Place tensor compute near large caches (L2 and L3) |
| Pooling/Concat        | Low data reuse, Mostly data movement                                         | High at L1-L2 and L2-L3| Execute near outer cache levels (L3/L2)           |
| Power dominated by unrolled wide OOO Fetch, Alloc and Dispatch |                                                                            | Exploit structured/loopy kernel to encode multiple loops |
We present Proximu\$, which places light-weight “Tensor Function Units” (TFU) near all on-die caches in the system as depicted in Figure 7. In combination with “Proximity Support Extensions” (PSX) to the ISA, the goal is to efficiently leverage existing system resources (maximizing or minimizing use as required) for performance and power benefits. Crucially, Proximu\$ also retains the existing CPU programming and memory models which can significantly speed up development and deployment efforts. We now detail the architectural, micro-architectural and programming model aspects of Proximu\$.

![PROXIMU$](image)

**Fig. 7: An overview of Proximu$ design**

A. Proximu\$: Architectural Support

1) **Proximity Support Extensions (PSX):** A close examination of state-of-the-art MKL-DNN kernels implementing DNN primitives shines light on opportunities to encode multiple loops of information succinctly. Such optimizations would enable minimizing and bypassing the power-hungry front-end stages of the CPU pipeline with unrolling and dispatch of work proximal to the execution units.

Depicted in Figure 8 is the meta-data information each instruction requires to encode its loop behavior in the kernel. First, we need to know the number of loops and their iteration counts. The ISA can set a limit on the maximum number of loops encoded, and we find that supporting four loops is sufficient for all these kernels (capturing load, compute and store operations). Each instruction needs to know the set of loops it resides within. In the example, weight loads are only executed in the outer loop. Second, loads and stores need a base address as well as an address stride for each loop it resides in. These can be computed since DNN primitive implementation employs structured data layouts to maximize cache port width and capacity. Finally, data dependence is still through registers. Hence, we can require stride values per loop for destination register ids as well. In the example, iterations of the innermost loop reuses weights for all output sets.
(being loaded in the outer loop) to compute different output elements that need to be stored in different registers. Here, the destination register id stride is determined by the number of outputs computed in the innermost loop (4).

| Instructions (PSX enabled Kernel) | Comments |
|-----------------------------------|----------|
| ✠ TFULoopStart                    | Flushes TFU Code Register in the core |
| ✠ TFULoopCount 2                  | Sets total expected loops to 2 |
| (Loop Iteration Calculation into R0) Baseline ISA. Executed in the core. | |
| ✠ TFULoopIteration 1, R0 //eg. = 64 | Sets iteration count of outer loop (loop1) to calc. value |
| (Loop Iteration Calculation into R0) Baseline ISA. Executed in the core. | |
| ✠ TFULoopIteration 2, R0 //eg. = 4 | Sets iteration count of inner loop (loop2) to calculated value |
| Load motionsWeight R1 ↔ [A, +Δn] | PSX instruction to be executed in TFU near a cache |
| ✠ TFULoopDisable 2                | Disables outer loop for previously allocated PSX instr. |
| (BaseAddress Calculation into R0) Baseline ISA. Executed in the core. | |
| ✠ TFUBaseAddress R0               | Sets BaseAddress for previously allocated PSX instr. |
| (Stride Calculation into R0) Baseline ISA. Executed in the core. | |
| ✠ TFUStride 1, R0                 | Sets stride for loop1 of previously allocated PSX instr to calc. value |
| ...                               | |
| MAC motions R(e+6+B) ↔ R1, R5      | PSX instruction to be executed in TFU near a cache |
| ✠ TFURegStride 2, 4               | Dest. register id. to be incremented by 4 every inner loop (loop2) |
| ...                               | |
| ✠ TFULoopEnd                      | Offload decoded PSX instructions to near cache TFU |

Fig. 9: Proximu笋 New PSX instructions and execution semantics

Figure 9 illustrates the new PSX instructions and their semantics. Kernel instructions are tagged with a PSX-bit (denoting near-cache TFU execution) and are decoded and allocated into new TFU Code Registers in the core. Our examination of primitives across multiple DNN models shows 32 registers to be sufficient. However, if a kernel has more than 32 instructions (and/or 4 loops) it would need to be split into smaller kernels that fit within these constraints. New PSX instructions (TFULoopCount, TFULoopIteration, TFULoopDisable, TFUBaseAddress, TFUStride, and TFURegStride) populate their respective meta-data loop information for the instructions tagged with PSX-bit. The meta-data information can be calculated using regular ISA (similar to the way the baseline kernels currently do it). The new TFULoopStart instruction flushes the TFU Code Registers for new PSX-tagged instructions and the TFULoopEnd instruction dispatches the TFU Code Registers to the near-cache TFU for unrolled execution. We conservatively estimate each TFU Code Register holds 8B of information (opcode, up to 3 registers (or a register and base address), 4 loop iteration counts (with a valid bit) and 4 address and register strides). The entire offload takes 16 cycles (8B offload bus width) and this time is amortized by the hundreds of cycles of unrolled execution in the TFU.

2) Tensor Functional Units (TFU): Figure 10 depicts the Tensor Functional Units (TFU), with 16 TFU Code Registers. A lean “Unrolling Scheduler” populates two 8-entry in-order Issue Queues - one for all compute opcodes and another for loads and stores. The design simplifies scheduling (lower power!) and allows hoisting of loads over compute (to hide load latency) while maintaining strict load/store ordering within the TFU. Loads and stores directly access the cache each TFU is placed proximal to - bypassing any inner levels. Snoops into inner cache levels, as required, are handled through added coherency support to the cache (Section III-B3). A small Translation Cache assists in memory management (Section III-B1).

![Schematic of the Tensor Functional Unit (TFU)](image)

Fig. 10: Schematic of the Tensor Functional Unit (TFU)

Both kernel characterization and performance analysis show that a 48-entry “deep” TFU Data Register File per TFU is sufficient - with no register renaming (lower power again!) required. The loads/MAC-instr requirement of the
workload and the near cache bandwidth bounds the peak compute “width” (the number of 64B MAC execution units) of the TFU. We evaluate the performance, power and energy implications of different compute widths in Section V. TFU area analysis is included in Section IV.

3) Leveraging SMT: Modern server-class CPUs support 2-way (Intel, AMD) and 4-way SMT (IBM, Sun SPARC). However, since all compute is shared across SMT threads, DNN frameworks disable SMT or use only one thread for the primitives, relying on multi-core compute scaling instead. With Proximus, each TFU is essentially a lean compute engine directly accessing one cache level in the hierarchy. As shown in Figure 11, we leverage SMT to bind each TFU exclusively to one of the logical SMT threads in the physical core. Therefore, each TFU is part of a fully capable, OS-visible hardware context. **DNN frameworks can then distribute work across TFUs using existing threading runtimes.** This also enables fine grained control over which caches and TFUs to use for a primitive (Section III-C3). PSX ISA, TFU design and SMT usage allow Proximus to maintain the CPU memory model (Section III-B4).

B. Proximus: Micro-Architectural Support

1) Virtual Memory: The TFU AGUs compute the virtual address for loads and stores while caches in modern CPUs are physically tagged. However, MKL-DNN optimizations use structured and special layouts, customized to feed compute, with a high spatial locality of tensor accesses [25]. Through extensive characterization across all primitives and models we find that a small 6-entry Translation Cache (TC), holding recently observed virtual to physical mappings, can achieve a 90% hit-rate. Misses in the TC (10%) can go through the existing TLBs and Page Walkers of the local physical core for translations without adding any significant bandwidth pressure on them. To ensure the TC entries are fully coherent, any TLB invalidation or page swap invalidates all TC entries in all TFUs.

2) Distributed L3 caches: L3 caches in modern CPUs are multi-bank structures shared across multiple-cores. Any cache-block aligned address can reside in only one L3 bank. This presents a challenge for TFU compute placed near each L3 bank. Multiple near-L3 TFUs will likely need to access the same addresses (example: a weight element used to compute multiple different output elements mapped to different TFUs in convolution). Depending on the reuse out of the TFU RF, addresses may need to be loaded multiple times. Traversing the L3 interconnect for every address not available locally would cripple near-L3 TFU performance and add significant extra data movement overhead. We leverage existing technologies like Intel’s CAT [11] or ARM’s cache lockdown [6] to simply partition a portion of the set-associative cache (a small subset of its total ways) in each L3 bank as a local cache for the attached TFU (with added coherency support). Section V includes performance sensitivity to the reserved local cache capacity for each near-L3 TFU.

3) Coherency Support: Since the TFUs represent new loads, stores and compute near each level of on-die cache, Proximus needs small additional tracking to maintain overall cache coherence. L2 caches need an extra bit per cache-line to denote whether L1 currently owns the cacheline, to ensure that it has ownership before doing a store. Similarly the directory entries at L3 need an extra bit per near-L3 TFU in their “sharer/owner” vector structures. This denotes whether the partitioned, local scratch-pad ways in that L3 bank have/own the cacheline. Hence, **Proximus maintains the baseline CPU cache coherence**, generating appropriate snoops at L2 and L3 as required.
4) Memory Model (Ordering): Proximu$\$ maintains the Total Store Order (TSO) memory model in CPUs. Within a TFU, strict loads/store ordering is maintained. We add a hardware fence in the core to prevent simultaneous TFU/non-TFU execution within a thread. A bulk offload of hundreds of cycles of work to the TFU (through PSX-ISA) amortizes any performance cost of this serialization. Non-TFU load/store ordering continues to be maintained by the core. Since TFUs are on different SMT threads, we do not need to guarantee any ordering in execution of loads and stores across TFUs.

5) Handling Context Switches and Exceptions: TFUs signal exceptions like existing functional/compute units in the physical cores. To support context switches on a thread, the core must also save/restore the TFU Code Registers and TFU Data Registers for the TFU on that thread as well as invalidate the local Translation Cache.

C. Proximu$: Programming Model Support

1) Generating PSX Code: High performance libraries already implement primitives using optimized code that is JITed \cite{37}. The kernel instructions must now be tagged with the PSX-bit. The JITer is already used to compute various loop variables. We extend the JITer to add PSX-bit tags to the new PSX instructions that populate the loop variables. Note that the programmer need not be aware of the exact TFU and cache level where these PSX instructions will eventually be executed. Optimizing compilers to generate PSX code from native languages without JITing is possible but we do not explore that direction in our work.

2) Exposing Proximu$\$ Capability at Each Cache Level: Presence of TFUs in each cache level and their corresponding compute width is exposed through the cpuid interface that is supported by all modern processors.

3) Optimal TFU selection for primitives: As we characterize and summarize in Table II and with further analysis in Section IV each primitive has an optimal set of TFUs for power-performance efficiency. We leverage the use of SMT (binding a TFU to a logical thread) and use existing OpenMP APIs to set the affinity of a primitive to a subset of cores. Specifically, we use \texttt{KMP\_SET\_AFFINITY} in the LLVM OpenMP Runtime \cite{22} to achieve this. DNN frameworks (TensorFlow, Caffe etc) would do the same before invoking the MKL-DNN implementation of a primitive (similar to currently only using one thread per core).

4) Distribution of work across TFUs: Since caches across the multi-level hierarchy have different bandwidths, their corresponding TFU will have different compute “widths” as well. For compute bound primitives like convolution, we need to divide work across TFUs proportionate to their compute strength for optimal performance. With high cache hit-rates and predictable performance, such a “static” division of work is sufficient for these workloads. Towards this, we introduce a simple new schedule kind called \texttt{static asymmetric} in the LLVM OpenMP runtime. For example, for three TFUs with compute strengths in a 2:2:1 ratio, a static equal division of work would result in unequal thread completion times with the third (weakest) TFU determining final runtime. With a static asymmetric distribution, in the same 2:2:1 ratio, all threads optimally complete at the same time.

5) Summary: Table III summarizes the intercepts in the overall software stack by Proximu$\$ with no changes to the current CPU programming model.

| Level in Software Stack | Proximu$\$ Support |
|-------------------------|--------------------|
| DNN Frameworks          | Set \texttt{KMP\_SET\_AFFINITY} appropriately for each primitive |
| (Tensorflow, Caffe, PyTorch) |                     |
| High Performance Library| Use PSX extensions for tensor load/store/compute instructions |
| (MKL-DNN)               |                     |
| Threading Runtime       | Asymmetric static scheduling when appropriate (e.g. Convolution) |
| (OpenMP)                |                     |

5) Summary: Table III summarizes the intercepts in the overall software stack by Proximu$\$ with no changes to the current CPU programming model.

IV. Evaluation Methodology

Simulation Framework: We use a modified version of Sniper \cite{31} for our cycle-accurate multi-core simulations. We model a state-of-the-art Intel 28 core datacenter processor \cite{2} but with 4-way SMT whose parameters are listed in Table IV. This baseline supports a peak 128 (2*64) MACs/cycle/core of compute (similar to Intel DL-Boost \cite{53}) with per-core on-die cache bandwidth including two 64B read ports at L1, two 64B read/write ports at L2 and one 64B read/write port at L3.

The simulation framework has been thoroughly validated against silicon by executing all the evaluated MKL-DNN primitives and verifying the performance trends using a Cascade Lake system running Ubuntu 16.04 with MKL-DNN v1.0 library. CACTI \cite{49,56} and McPAT \cite{47} are used to quantify cache and overall energy impact.

Proximu$: We model all of Proximu$ in Sniper allowing sweeps of peak compute at each TFU at different cache levels. The last SMT thread is tied to L1 TFU but not used. We use prefix “P” (for Proximu$) or “M” (for traditional monolithic core) followed by a number which indicates the peak number of MACs/cycle/core that the configuration
has. Further, the notation also attaches an explicit distribution of compute resources across the cache levels as indicated in Table IV. Mxxx configurations have MAC units that support xxx MACs/cycle/core. Table V specifies the hardware resources and the distribution for the Proximu$ configurations.

### Area Requirements of the Proximu:

We synthesize a Verilog implementation of a TFU instance that is capable of 256 (4*64) MACs/cycle/TFU to support the P640 configuration. Synthesis is done using TSMC 28nm library, setting a target clock of 1 GHz, using Synopsys Design Compiler [23]. The total area per TFU is 0.38mm² and the detailed breakup area is given in Table IV. An additional 2KB/core of storage is required for new core-valid bits in L2 and L3 for full coherence. Total area overhead is the sum of this coherence storage and the area required for three TFUs/core. Projecting the total overhead to the 14nm technology [59], [1] in which the Intel Xeon server chips are built, we conservatively estimate the overall overhead due to Proximu$ to be a mere 2.63% of a single Xeon core. From observing die-plots (58, [21]), Proximu$ takes 35% less than the AVX-512 unit already present in the cores, while delivering a higher peak MACs/cycle/core cumulative compute.

### Workloads and Software Stack:

We evaluate six DNN topologies end-to-end including ResNet-50 [40], DenseNet-169 [43], MobileNet [41], ResNext-101 [61], Transformer [59] and TwoStream [35]. Of these, Transformer comprises solely of inner-product layers while the others have mostly convolution layers. We use the latest open source MLK-DNN v1.0 and the Intel C++ compiler 19.0 to ensure we are evaluating state-of-the-art software implementations. Note that these are full system (including DRAM), multi-core evaluations. Since we study int8 inference, most model weights fit in caches. Coupled with high reuse, overall impact on performance and power from DRAM is very low. These workloads are parallelized using the OpenMP multi-threading framework using our new static asymmetric scheduling.

## Results

We will first present performance and data movement impact of Proximu$ near-cache compute for DNN primitives in the ResNet-50 and Transformer models. We then do a detailed power, performance and energy study for Proximu$ on ResNet-50 and Transformer. This is followed by results for all six DNN topologies evaluated. We then summarize the performance and performance/watt goodness of Proximu$ and conclude by comparing it with available MLPerf data for GPUs and DSAs.

### Convolution

Figure 12 shows the impact of Proximu$ on ResNet50 convolutional layers and reveals multiple interesting observations. Traditional scaling of compute plateaus at an average 180 MACs/cycle/core from M256 onwards, since L1 bandwidth saturates, despite using only 40% of total available on-die bandwidth. However, Proximu$ scales well in performance at all points, achieving between 2x to 3.9x2 performance over baseline, with up to 90% cumulative bandwidth utilization in the higher peak compute points. Proximu$ P256 also has 41% higher performance than M256, achieving near peak performance. M256 needs peak bandwidth (100% hit-rate) from L1 to achieve performance. In contrast, the P256 config doesn’t require peak bandwidth from any of its caches and is hence able to get higher performance.

PSX-ISA achieves an average 20× reduction in dynamic instructions executed in the legacy OOO pipeline, which will translate to power savings. Peak compressibility is actually 37×, with the new PSX instructions to populate loop

### TABLE IV: Simulator Parameters

| Cores     | 2.6GHz, 4-way SMT, 320-entry ROB, 128 (2*64) MACs/cyc/core |
|-----------|---------------------------------------------------------------|
| L1 cache  | Private, 32kB, 8-way set associative, LRU, 8-entry MSHR, 2x 64B read ports, 1x 64B write ports, Data access=4 cycles, Tag lookup=1 cycle |
| L2 cache  | Private, 1MB, 16-way set associative, LRU, 48-entry MSHR, 2x 64B read/write ports , Data access=8 cycles, Tag lookup=2 cycle |
| L3 cache  | Distributed, Non-inclusive, 1.375 MB/slice, 11-way set associative, RRIP, 48-entry MSHR, 1x 64B read/write port per slice, Data access latency=10 cycles |
| Tag directory | MESIF, 10 cycle latency |

### TABLE V: Notation for Proximu$ configurations

| Name | MACs/Cycle/Core | Details |
|------|----------------|---------|
| P128 | 128            | same as M128 |
| P256 | 256            | 128L1, 640L2, 640L3 |
| P320 | 320            | 128L1, 128L2, 640L3 |
| P512 | 512            | 256L1, 128L2, 128L3 |
| P640 | 640            | 256L1, 256L2, 128L3 |
TABLE VI: Area Breakdown for TFU (in mm$^2$)

| Registers | MACs    | TC, Queues, Control |
|-----------|---------|---------------------|
| 0.15      | 0.17    | 0.06                |
| Total Bytes: 3184 |
| Total Area: 0.38 mm$^2$ |

Fig. 12: Impact of Proximu$\dagger$ on ResNet50 Convolutional Layers

meta-data accounting for the difference. Finally, Proximu$\dagger$ reduces data movement overheads from 20% down to 10%, mainly going down at the L1-L2 interface.

Fig. 13: Per ResNet-50 convolution layer Proximu$\dagger$ performance for P256 and P640 configurations and Compressibility using PSX ISA

Figure 13 shows per-layer performance and compressibility for the 53 convolution layers in ResNet-50 for the P256 and P640 configurations. Note that the last few convolutional layers of ResNet-50, including the res5c_branch2c layer, achieve lower performance with Proximu$\dagger$. These layers have lower total Ops/Byte with the near-L3 TFUs see low hit-rates in their 256KB local partitioned cache (2 out of 11 ways), with high cross-L3 traffic. Increasing the reserved near-L3 ways from 2 to 8 ways, improves performance for these layers by 40%-60%. Compressibility increases with increase in the input channel dimension (due to higher accumulation required per output) and is generally lower for 1x1 kernels compared to 3x3 kernels (due to lower input reuse).

B. Inner Product

Figure 14 plots the average impact of Proximu$\dagger$ configurations on performance, data-movement for the 106 Transformer inner-product layers. Since these are low Ops/Byte bandwidth bound primitives, we only use the P256 Proximu$\dagger$ configurations.
configuration but schedule threads selectively at different cache levels. By merely executing the inner-product directly near the large 1MB L2, with better hit-rate and therefore bandwidth delivery, Proximu$ achieves 2.2× more performance and a 2.6× reduction in data movement overheads. All L1 traffic has been eliminated. Execution only near-L3, with a 2-way 256KB local cache, also reduces data movement. However, as we can now expect, provisioning more capacity to the near-L3 compute increases performance to match Proximu$ near-L2. Executing the primitive at both L2 and L3 improves performance by a huge 3.3× over what can be achieved by the baseline. This is achieved with no increase in on-die cache bandwidth while simultaneously reducing data movement overhead by 5.6×. Finally, the new PSX-ISA achieves 10× compression, which will directly translate to power and energy savings.

C. Pooling and Concat Layers

For brevity, we summarize the main observations from evaluations of the pooling and concat primitives. Executing the res5c ResNet-50 pooling layer solely near L3 reduces data movement overhead by 95% (103% down to 8%). Similarly, Concat layers in DenseNet-169 see an average 150% data movement overhead, which is brought down by 70%-95% (down to 25%-5% overhead) via near L2 or near L3 execution.

D. Detailed Energy Analysis

Figure 15 represents a detailed energy analysis of the ResNet-50 convolutional layers and Transformer inner-product layers on the baseline M128 and P256 configurations. All the energy components are shown relative to the total energy cost of running on a M128 configuration. We deconstruct the impact of the near-cache and PSX ISA components of the Proximu$ proposal separately and when put together.
In ResNet50, the FE and OOO stages of the CPU pipeline dominate overall energy (60%). M256, even while having twice the resources as M128, is iso-energy with M128 as long as near-cache capabilities are not included to them. Adding near-cache compute reduces inter cache data movement costs between L1 and L2 but also increase direct accesses to the larger (costlier in power) L2/L3 caches. Therefore, near-cache compute ends up iso-energy with baseline. Third, due to high Ops/Byte and high reuse, the PSX ISA proposal achieves an average $20 \times$ compression, which translates to a $17 \times$ reduction in energy from the FE and OOO stages of the pipeline. Proximu$^\text{P256}$ configuration therefore operates at 42% of baseline energy (translating to a 13% decrease in power, along with a 2x increase in performance).

The bandwidth bound, low Ops/Byte inner-product layers in Transformer present a different story: data movement reduction (primarily by eliminating L1) brings a 18.6% reduction in energy. Despite lower data reuse compared to convolution, the PSX ISA proposal achieves a $10 \times$ compression, bypassing the FE and OOO pipeline stages and providing a 42.8% energy reduction. Put together, we see a 61.5% reduction in overall energy consumption (at 1.5% lower in power due to 2.77x better performance).

**E. Overall Performance, Power and Energy**

Figure 16 and Figure 17 show performance, energy and power impact of two Proximu$^\text{P}$ configs (P256 and P640 respectively) over six DNN-inference topologies. Inner-product heavy Transformer is bandwidth bound. It achieves 2.78x better performance at iso-power (65% lower energy) for both Proximu$^\text{P}$ configs. The rest of the DNN models have mostly convolution layers. With the exception of DenseNet-169, these topologies see around 2x performance with 2x compute (P256 vs M128), at 12%-14% lower power (60% lower energy). This increases to around 3.95x higher performance with 5x more compute (P640 vs M128) at 65% higher power (and 60% lower energy). DenseNet-169 has a number of Concat layers which take nearly 20% of total runtime. Proximu$^\text{P}$ reduces power for this data shuffling primitive but doesn’t impact performance. This results in slightly lower performance improvement for DenseNet-169 with Proximu$^\text{P}$, but at slightly better power compared to the other convolution heavy DNN topologies.
F. Proximu$\$: **Performance and Performance/Watt**

Figure 18 succinctly summarizes the goodness of Proximu on ResNet-50. The PSX-ISA improves performance/watt by 2.3×. Furthermore, by leverage near-cache compute, performance can scale by 2× to 3.94× depending on the available TDP (13% lower power to 68% higher power). Similarly, for inner-product heavy topologies like Transformer, Proximu$\$ achieves a 1.8× increase in inner-product performance/watt with 2.8× improvement performance. These gains are achieved with minimal additional hardware, no increase in cache capacity or bandwidth and no change in the CPU programming and memory models.

G. Proximu$\$ comparison to DSAs and GPUs

We compare Proximu$\$ with other platforms that are used for DNN inference by using state-of-the-art, vendor-provided, publicly available throughput results on ResNet-50 v1.5 from MLPerf Inference results [16], [52]. Figure 19 shows the number of queries processed by a variety of accelerators (Habana Labs [8], Intel Nervana [14], TPU v3 [45]), GPUs(using a Titan RTX T496X2 card), and Cascade Lake based Intel Xeon Platinum 9200 processor (similar to our CPU baseline). We normalize the data to per node (for accelerators and GPUs) or per socket (for CPUs) and use the best results for each platform.

Proximu$\$ can achieve comparable (or even somewhat better) performance to state-of-the-art DSAs (Intel Nervana, Google TPU v3). We don’t make any performance/watt comparisons due to the absence of these metrics in MLPerf. However, we have shown significant (1.8×-2.3×) improvement in CPU performance/watt with Proximu$\$. Proximu$\$ requires significantly lower area than the DSAs since it reuses existing cache, memory and scheduling resources in the CPU.
1) Sensitivity to cache bandwidth: We further study the effectiveness of using Proximu$ in systems that have different bandwidth configurations at L2 and L3 (reducing L2 bandwidth to a single 64B port (2/1/1) or increasing per-slice L3 bandwidth to two 64B ports (2/2/2)). We follow our methodology of sizing compute proportional to the associated cache bandwidth: for example, reducing to 128 MACs/cycle/core near-L2 when it has a single read/write port (2/1/1). As shown in Figure 20 while the baseline performance plateaus beyond the peak 256 MACs/cycle/core point, Proximu$ enabled systems continue to scale performance. Proximu$ achieves around 75% compute efficiency at every compute and bandwidth configuration.

![Fig. 20: Sensitivity of Proximu$ to cache bandwidth scaling](image)

VI. PROXIMU$ ON LOW-POWER, EDGE CPUs

We have verified the performance/power benefit of Proximu$ across a range of compute widths, caches sizes and bandwidths; including lower compute (16/32 MAC/cycle/core) and cache bandwidths typical to lower power edge CPUs. These systems can pose two additional challenges. First, they typically have shallower cache hierarchies, often with multiple cores sharing an L2 cache. With Proximu$, we would still have a TFU per core at the L2 cache, but with lower compute strength. The total compute strength across all TFU near a shared-L2 should be proportional to the L2 bandwidth. Second, these cores typically do not have SMT capabilities. This essentially means a core would simultaneously schedule to all its TFUs, breaking support for TSO memory ordering. Prior studies [7] have shown that relaxed consistency is fine for ML workloads. For low power and low cost edge SOCs, where budget, latency and battery life requirements reduce the ROI of adding specialized DSA hardware with driver-based offload, we believe Proximu$ represents an excellent CPU solution on all cost, performance and energy metrics.

VII. RELATED WORK

Over the past few years, there have been numerous works targeting moving processing to in or near memories like DRAM[54, 55, 53], 3D-stacked HBM[9] or HMC[51] (29, 64, 46, 42, 30) and even SSDs[48]. Compute Cache[28], Neural Cache[34], and Duality Cache[36] are all recent works that propose converting the CPU on-die caches into compute units capable of bit-serial /bit-parallel operations in the SRAM sub-arrays. While these works show hugely impressive gains, they involve changes to highly optimized SRAM sub-arrays, and can degrade or complicate signal integrity, density, floorplan. Proximu$ takes a light-weight, compute-near-cache approach, reusing existing micro-architectural interfaces and extracting large improvements in performance, power and area utilization, all with no changes to the existing programming model.

VIII. SUMMARY

As the amount of data created and analyzed grows at an exponential pace, OEMs are willing to harness all forms of available compute to tackle their computational needs. While CPUs are the dominant platform-of-choice for DNN inference in datacenters, our in-depth analysis reveals significant opportunities for more efficient CPU resource utilization leading to drastic improvements in performance/watt and the ability to scale performance without increasing cache capacity or bandwidth. Using a combination of simple ISA enhancements and light-weight tensor compute near all caches in the CPU, Proximu$ raises the bar for CPU-based DNN-inference performance and performance/watt while maintaining the same programming and memory models. Proximu$ represents a fundamental re-imagination of the general-purpose CPU, better suited for the AI era.
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