All-Amorphous Junction Field-Effect Transistors Based on High-Mobility Zinc Oxynitride

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1. Introduction

Electronic devices based on amorphous oxide semiconductors (AOS) provide a variety of advantages such as low-temperature and homogeneous large-scale fabrication. Intensive studies were conducted on multi-cation compounds such as amorphous indium-gallium-zinc-oxide (a-IGZO), which already entered the display market as channel material of pixel driving thin-film transistors (TFTs). Nevertheless, the use of the critical raw materials indium and gallium is not preferable in terms of cost-effectiveness and sustainability, particularly if one bears in mind the growing interest in the Internet of Things technology. That is why research is still going on to find earth-abundant substitutes with high mobility values (>20 cm² V⁻¹ s⁻¹) enabling environment-friendly, low-cost, high-performance devices.

In 2009, amorphous zinc oxynitride (a-ZnON) was demonstrated to be a promising high-mobility semiconductor for low-temperature fabricated, high-performance thin-film transistors. But up to now only metal-insulator-semiconductor field-effect transistors (MISFETs) based on a-ZnON have been reported. Very recently, we demonstrated the first ZnON-based metal-semiconductor field-effect transistors (MESFETs) with low-voltage operation and high field-effect mobility values.

In the current work, we investigate the electrical characteristics of amorphous p-n diodes and their implementation in junction field-effect transistors (JFET) based on room-temperature (RT)-deposited p-type ZnCo₂O₄ and n-type ZnON. Like MESFETs, JFETs have the advantages of low operating voltages and fast switching speed due to the lack of a gate dielectric. Further, JFETs were already used within oxide-based inverter circuits, which can be integrated into logic circuits.

2. Results and Discussion

Hall effect measurements at RT reveal a free electron concentration of \( n = 1.5 \times 10^{17} \text{ cm}^{-3} \) and a Hall mobility of \( \mu_{\text{Hall}} \approx 100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1} \) for the as-received, \( \approx 90 \text{ nm}-\text{thick a-ZnON thin film.} \)

Figure 1a shows a typical current density versus voltage (j–V) characteristic of a p-ZCO/n-ZnON heterojunction diode at RT with a rectification ratio of \( 5.4 \times 10^{2} \) at \( \pm 2 \text{ V} \). Modeling of the diode forward current according to the Shockley equation

\[
j = j_{s} \left[ \exp \left( \frac{e(U - I R_{s})}{n k_{B} T} \right) - 1 \right] + \frac{U - I R_{s}}{A R_{p}}
\]

yields an ideality factor \( n = 2.04 \) (forward voltage sweep) and \( n = 1.78 \) (backward voltage sweep), respectively, indicating generation-recombination dominated current transport. \( A \) denotes the diode area, \( R_{s} \) the series resistance, \( R_{p} \) the parallel resistance, \( j_{s} \) the saturation current density, \( k_{B} \) the Boltzmann constant, and \( T \) the absolute temperature. The observed hysteresis, which depends on the voltage sweep rate, is ascribed to trapping and detrapping effects at the interface. To prevent such hysteresis effects one would have to measure with larger integration time than the used 20 ms per 0.01 V step. However, the other fit parameters of the forward and backward voltage sweep do not differ significantly. \( R_{s} \), \( R_{p} \), and \( j_{s} \) are \( >900 \Omega \), \( >9 \text{ M}\Omega \) and \( >3 \times 10^{-7} \text{ A cm}^{-2} \), respectively, for the shown diode characteristic in Figure 1.

The rectification ratio of our investigated diodes lies between values of similar AOS-based heterojunction diodes reported...
A hypothetical band diagram of the investigated pn-heterojunction can be estimated by using literature values for the band gap $E_g$ and electron affinity $\chi$ values of ZCO ($E_g \approx 2.5$ eV, $\chi_p \approx 2.9$ eV) and ZnON ($E_g \approx 1.3$ eV, $\chi_n \approx 4.0$ eV) under the assumption of a similar conduction band minimum position as for ZnO and is shown in Figure 1b. But one has to keep in mind that there is a relatively large uncertainty in the energetic positions of band edges due to the amorphous nature of both semiconductor materials. As the doping density in ZCO ($10^{20} - 10^{21}$ cm$^{-3}$) is several orders of magnitude larger than that of ZnON ($10^{17} - 10^{18}$ cm$^{-3}$), the space charge region mainly spreads into the n-type ZnON yielding a one-sided p$^+$-n-diode, which can be treated similar to a Schottky diode. Considering the vanishing valence band offset $\Delta E_v$, current transport at room temperature is expected to occur via thermionic emission of holes into the neutral n-region as well as via recombination at interface traps, as the ideality factor of 2 suggests. Under the assumption of a predominantly thermionic emission current one calculates a potential barrier height of 0.75 eV from the saturation current density $j_s$ according to the Schottky diode model. In order to obtain further insight into the current transport, temperature-dependent current–voltage ($I$–$V$) measurements were performed in the temperature range of 120–290 K in 10 K–steps (Figure 2a).

Reliable modeling of the forward $I$–$V$ characteristics according to Equation (1) was possible down to 180 K, as exemplarily depicted in Figure 2b. With decreasing temperature slight deviations from the model in the forward bias regime $V > 1$ V become apparent, which are probably related to laterally potential inhomogeneities. Further, a bias-dependent current in the reverse bias region is observable. It is suggested that this temperature- and bias-dependent reverse current is caused by trap-assisted tunneling. Trap-limited conduction transport was reported for a-ZnON TFTs due to a high density of localized tail states, attributed to nitrogen-deficiency-related defects, near the conduction band minimum. Such trap states, distributed in the space-charge region, enhance the tunneling probability and with that increase the recombination rate in p-n diodes leading to higher reverse currents. However, such an effect becomes only apparent when the thermionic saturation current becomes small. A similar behavior, attributed to oxygen defects, was observed in ZnO-based p-n diodes.

![Figure 1](image1.png)

**Figure 1.** a) Current density versus applied voltage ($j$–$V$) characteristic of an amorphous p-n heterojunction ZCO/ZnON diode measured at RT in dark ambient (black curve) under forward (−2 to 2 V) and backward (2 to −2 V) voltage sweeps indicated by arrows, and corresponding fit curve (green). b) Schematic band alignment according to literature values and Anderson's rule (also known as electron affinity rule) for the investigated ZCO/ZnON p-n heterojunction at zero bias.

![Figure 2](image2.png)

**Figure 2.** a) ZCO/ZnON p-n diode $j$–$V$ characteristic measured at temperatures between 120 and 290 K. b) Measured data (open circles) and corresponding fit curves (lines) for selected temperatures as labeled.
The drain-current on/off-ratio is improved by one order of magnitude to 1.1 as expected, the drain-current bar turns about 0.3 V. Similar observations were already discussed for ZnON-based Schottky diodes[8] and corroborate the assumption that current transport in ZnON-based devices is substantially affected by trap-assisted tunneling processes. 

Figure 3a depicts typical RT transfer characteristics at a drain-source voltage of $V_{DS} = 3$ V, as well as the respective absolute gate current, of the investigated JFET devices consisting of a p-ZTO gate and a n-ZnON channel with two different channel thicknesses. The 90 nm-thick ZnON channel device is normally-on and exhibits a drain current on/off-ratio of four orders of magnitude and a subthreshold swing of 240 mV dec$^{-1}$. It is evident that the transistor’s off-current is dominated by the gate leakage current, thus limiting the drain-current on/off-ratio and the subthreshold swing. A channel thickness reduction to 48 nm yield normally-off transistors with current on/off-ratio and the subthreshold region. A channel dominated by the gate leakage current, thus limiting the drain-current on/off-ratio.

For a reliable channel mobility extraction we compared different methods. Following the methodologies for MOSFETs[23] there are:

a) the effective mobility $\mu_{eff}$ obtained from the drain conductance $g_d$ for low $V_{DS}$ (linear regime):

$$\mu_{eff} = \frac{g_{d,lin} \cdot d}{W} \varepsilon_0 \varepsilon_r (V_{GS} - V_{th})$$  (2)

b) the saturation mobility $\mu_{sat}$ obtained from the transconductance $g_m$ for high $V_{DS}$ (saturation regime):

$$\mu_{sat} = \frac{g_{m,sat} \cdot d}{W} \varepsilon_0 \varepsilon_r (V_{GS} - V_{th})$$  (3)

These equations are only similar to that of MOSFETs near threshold ($V_{GS} = V_{th}$) since the gate capacitance per unit area is gate-bias dependent in JFETs. Figure 4a compares the calculated channel mobilities according to Equations (2), (3), and (5) in dependence on applied gate bias $V_{GS}$. The threshold voltage $V_{th}$, as well as the saturation mobility according to Equation (4) were determined from $\frac{\partial I_{D,sat}}{\partial V_{GS}}$ versus $V_{GS}$ plot, shown in Figure 4b. To calculate $\mu_{eff}$ the drain current $I_{D,lin}$ for $V_{DS} \approx 0$ V is obtained from the output curve in Figure 4c. It is worth to mention here, that JFET transfer characteristics cannot be measured in the linear regime ($V_{DS} \ll V_{GS} - V_{th})$ due to the non-insulating gate leading to negative drain current (confer output curve in Figure 4c for $V_{GS} \approx 1$ V). The transconductance $g_{m,lin,sat}$ was calculated from the corresponding transfer curve Figure 4d. All methods yield similar channel mobility peak values around 45 cm$^2$ V$^{-1}$ s$^{-1}$ for the 90 nm-thick ZnON channel. It is verified that all mobility extraction methods are applicable to JFETs and yield reliable values if the gate current is negligible. For further analysis and statistics we determined the channel mobility after Equation (4), since this method allows the determination of $V_{th}$ and $\mu_{sat}$ at the same time from the transfer curve. The $\mu_{sat}$ obtained from the transfer characteristic depicted in Figure 3a is 51 cm$^2$ V$^{-1}$ s$^{-1}$, whereas for the 48 nm-channel JFET a value of 86 cm$^2$ V$^{-1}$ s$^{-1}$ is extracted. This
higher value can be ascribed to the non-negligible contribution of the gate current in the transistors on-regime rendering the transistor equations invalid. Such behavior is inherent in JFETs, especially if the transistors turn-on voltage is in the onset regime of the gate diode forward current, as it is the case for the 48 nm-channel JFET.

The channel mobility is lower than the measured Hall mobility \( \mu_{\text{Hall}} \approx 100 \, \text{cm}^2 \, \text{V}^{-1} \, \text{s}^{-1} \). This is explained by additional scattering and trapping effects at the ZCO/ZnON interface and in the ZnON channel, respectively. On the one hand, it was observed that ZnON is attacked by the diluted sodium hydroxide solution used for developing the photoresist. Thus, the processing of the top-gate structures on ZnON thin films results in a degraded surface with a presumably large interface-trap density. On the other hand, ZnON is known to exhibit trap-limited conduction, which means the drift mobility depends on the ratio of free and trapped carriers in the channel and with that on the position of the Fermi level (determined by the applied gate voltage), on the energetic and spatial distribution of traps within the channel as well as on temperature.\(^{6,24}\)

The histograms in Figure 5 summarize the electrical parameters, extracted from the RT transfer characteristics for \( V_{DS} = 3 \, \text{V} \), of the investigated JFET devices. The small spread in the parameter distribution can be ascribed to the aforementioned non-optimal processing conditions for the investigated top-gate structures. In Table 1 the electrical parameters of the best investigated JFETs are collected. To the best of our knowledge, this is the first demonstration of JFET devices based on a-ZnON channels. The comparison with ZnON-based MISFETs (also in Table 1) shows that JFETs have the advantage of better switching behavior (lower switching voltage and subthreshold swing) due to the lack of an insulator, which render them more suitable for high-frequency device applications.

3. Conclusion

In summary, we fabricated and characterized the first ZnON-based n-channel JFETs using a fully amorphous p-n heterojunction gate diode comprising p-ZCO and n-ZnON. The resulting devices are found to exhibit excellent switching characteristics with an \( \text{ON/OFF} \) ratio, subthreshold swing and saturation mobility of \( 10^5 \), 134 mV dec\(^{-1} \), and \( \geq 50 \, \text{cm}^2 \, \text{V}^{-1} \, \text{s}^{-1} \), respectively. We observed that current transport in ZnON-based devices is presumably affected by trap-assisted tunneling processes. Future work should concentrate on transport measurements in dependence on trap densities in order to provide a further in-depth understanding of current transport in AOS devices aside from MISFETs.

Figure 4. a) Gate bias dependence of the channel mobility for a ZnON-based JFET with a gate width-to-length ratio \( W/L \) of 430 \( \mu \text{m}/40 \, \mu\text{m} \) and channel thickness \( d = 90 \, \text{nm} \). b) \( \sqrt{J_D} \) versus gate voltage plot and the corresponding c) output and d) transfer curves.
4. Experimental Section

DC-sputtered a-ZnON thin films on glass substrates were supplied by Y. Ye. Further details on the fabrication process can be found in ref. [2].

The electrical properties of the thin films were investigated by means of RT Hall effect measurements using a four-probe van der Pauw geometry and a magnetic field of 0.43 T. Gold contacts placed on the corners of a 10 × 10 mm² sample were dc-sputtered under Ar atmosphere providing ohmic contacts, as confirmed by current–voltage (I–V) measurements (Figure S1, Supporting Information). The electrical characterization of ZnON-based diodes and field-effect transistors (FET) was conducted in dark ambient at RT using an Agilent 4155C Semiconductor Parameter Analyzer in connection with a SÜSS waferprober system. For this purpose, circular diodes of various diameters as well as top-gate FET structures were processed by means of standard photolithography. Defined channel mesas were formed by wet chemical etching of ZnON in diluted hydrochloric acid (1:100) for 25 s. The ohmic source and drain electrodes were fabricated by dc-sputtering of 70 nm-thick Au and patterned using lift-off technique. The amorphous p-type ZnCo₂O₄ was deposited by pulsed laser deposition at RT and an oxygen partial pressure of p(O₂) = 0.05 mbar according to ref. [25]. Subsequently, a 30 nm-thick Au capping layer was dc-sputtered as gate electrode. A schematic device structure is depicted in Figure 3c.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest
The authors declare no conflict of interest.

Data Availability Statement
Research data are not shared.

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