Stability enhancement of top-gate self-aligned tin-doped indium gallium oxide thin film transistor by low temperature annealing

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Abstract. Top-gate self-aligned IGTO TFTs were used as an example to study the contradiction of uniformity and PBTS stability when developing TFT with high mobility. High intrinsic carrier concentration restricted the tuning of SiO2 deposition. To ensure the uniformity, relatively higher power was employed for GI deposition to reduce donor-type oxygen vacancies. Deep electron traps formed by excess oxygen lead to poor PBTS stability. The PBTS stability was improved without deterioration of uniformity by introducing low temperature (200 °C) annealing, to control hydrogen diffusion from ILD layer which would passivate the electron traps.

1. Introduction
Although amorphous indium gallium zinc oxide (a-IGZO) thin film transistors (TFTs) with a typical mobility of ~10 cm2/Vs has become the standard backplane for high-end screen products, such as large size organic light-emitting diode displays, there are reports showing that higher mobility is required for internal compensation for active-matrix organic light-emitting diode (AMOLED) and mini/micro light-emitting diode (m/μ-LED) display [1]. As a promising candidate, IGTO shows sufficient high mobility (>25 cm2/Vs) benefited from the identical electron configuration of Sn4+ and In3+. However, IGTO TFTs usually suffer from unstable device characteristics in comparison with the IGZO TFT due to higher carrier concentration [2].

In this work, top-gate self-aligned structured TFTs with sputtered IGTO active layer are used to study the influence of low temperature post-annealing on the instability dependent upon bias and temperature stress. The TFTs were then fabricated on Gen. 4.5 (920 mm × 730 mm) glass. By introducing low temperature post-annealing, the device stability was enhanced without deterioration of global uniformity.

2. Experimental details
100-nm thick IGTO thin films were deposited at room temperature by direct current (DC) sputtering using an indium-rich IGTO target provided by Samsung Corning Advanced Glass Co. The sputtering was carried out in argon/oxygen gas mixture with a sputtering pressure of 0.6 Pa. Oxygen percentage in total gas (PO2) was maintained 33%. The structural properties the IGTO films was analysed by out-of-plane grazing incidence X-ray diffraction (XRD).
Top gate self-aligned (TG-SA) TFTs were then fabricated on Gen 4.5 glass substrates. The device structure is schematically shown in figure 1. First, a Mo layer was deposited and patterned by standard photolithography to form the light shielding structure. This was followed by the deposition of a 400 nm SiO₂ layer as a buffer layer. A 30 nm IGTO as an active layer was deposited by DC sputtering at room temperature. Subsequently, 150 nm SiO₂ gate insulating layers were deposited by plasma enhanced chemical vapour deposition (PECVD) under different ratio frequency (RF) power. Mo/Al/Mo was deposited by DC sputtering and patterned as the gate electrode. After wet etching of the gate electrode, the GI was dry etched for the self-alignment process. For the interlayer dielectric (ILD), 400 nm SiO₂ layer was deposited through PECVD. Then, via-holes on the source/drain (S/D) region and S/D electrodes were formed. Finally, a 350 nm SiO₂ was deposited as passivation layer. The low temperature post-annealing was performed at 200 °C in air atmosphere.

The electrical properties of the devices were collected using an Agilent B1505 semiconductor analyser. The TFT’s threshold voltage (Vth) is taken as the gate voltage (V GS) at which the normalized drain current (IDS) reaches 1 nA. The field-effect mobility (μFE), derived from transconductance (gM) is given by

\[ \mu_{FE}(V_{GS}) = g_m(V_{GS}) \frac{L}{W C_{OX} V_{DS}} \]

Where, the C ox is the gate-oxide capacitance per unit area and drain voltage (V DS) = 0.1 V. For positive bias temperature stress (PBTS) measurements, a constant V GS of +30 V is applied at 60 °C for 1 hour under dark conditions.

3. Results and discussions

Figure 2 shows the XRD pattern of the IGTO thin film. A pronounced diffraction peak located at ~31° is observed. Since the percentage of indium oxide (In₂O₃) in the target is higher than 70%, this diffraction peak can be assigned to the 222 diffraction of body-center cubic structure of In₂O₃. The higher 2θ value than the theoretical one (~30.5°) are expected when In³⁺ (ionic radius of 0.81 Å) are partly substituted by Ga³⁺ (ionic radius of 0.62 Å). The full width at half maximum of the diffraction peak is ~0.5°, indicating the micro-crystalline nature. It has been reported that crystallized IGTO film possessed larger amount of oxygen vacancy related defects.

TG-SA structure with light shielding layer has merits of high stability against bias, heat and light, and good saturation behaviour and has been widely used in AMOLED and micro-LED applications. Three samples, marked as sample A, B and C, were fabricated with SiO₂ gate insulators deposited by PECVD at different RF power in a narrow window. SiO₂_A, SiO₂_B, and SiO₂_C deposited at a normalized power of 0.95, 1.0, and 1.05 were applied to sample A, B and C respectively. The deposition rate of SiO₂ decreases with RF power as shown in figure 3(a), which can be explained by increased gas phase reaction. Decreasing the growth rate of SiO₂ should lead to a better build up of the oxide network, however, it becomes complicate when applying as gate insulator in TG-SA TFTs.
Figure 3(b)-(c) show the overlapped transfer curves obtained from 13 points of TFTs on Gen 4.5 glass for the three samples. The channel width and length of the device are 10 and 8 um, respectively. The global uniformity of sample B and C are excellent with standard deviation less than 0.18 V. Sample A shows deteriorated uniformity, in which some TFTs become normally on and could not be turned off even at $V_{GS} = -15$ V. Table 1 summaries the device characteristics parameters. The negative $V_{th}$ and high mobility of sample A are attributed to high intrinsic carrier concentration. When the SiO$_2$ is deposited at higher power, larger amount of oxygen atoms are injected into the IGTO active layer either reducing donor-type oxygen vacancies or forming deep electron traps. As carrier concentration decreases, the $V_{th}$ becomes positive and the percolation conduction is weakened.

Table 1. List of device parameters for sample A, B, and C with GI deposited at different RF power removing the data from the normally-on TFTs of sample A.

| Sample | A | B | C |
|--------|---|---|---|
| Gate Insulator | SiO$_2$ A | SiO$_2$ B | SiO$_2$ C |
| $V_{th} \pm 3\sigma$ (V) | $-0.25 \pm 1.07$ | $0.31 \pm 0.53$ | $0.4 \pm 0.52$ |
| Mobility (cm$^2$/Vs) | $-49$ | $-35$ | $-29$ |
| SS (V/dec) | 0.19 | 0.21 | 0.21 |
| PBTS $\Delta V_{th}$ (V) | 4.2 | 6.5 | 10.1 |

The PBTS instability of the three sample are shown in figure 4. After PBTS, sample A, B and C have different threshold voltage positive shift of 4.2, 6.5 and 10.1 V. The large amount of $V_{th}$ shift can be explained by the incorporation of excess oxygen and associated subgap defects with a negative- U characteristic [3]. SiO$_2$ deposited at lower power benefits PBTS stability, however, high intrinsic carrier concentration of crystalline IGTO restricts further tuning of the deposition of gate insulator.

To overcome this dilemma, low temperature annealing was employed. The global uniformity and PBTS instability of sample B after annealing for 2 hrs are shown in figure 5. The $V_{th}$ shifts negatively from 0.31 to 0.18V without deterioration of uniformity after annealing. The mobility increases from ~35 to ~45 cm$^2$/Vs, which indicates the increasing carrier concentration. On the other hand, significant enhancement of stability against PBTS is observed with a reduction of $\Delta V_{th}$ from 6.5 V to 1.8 V.

Annealing at 200 °C is sufficient to activate the diffusion of hydrogen [4]. During annealing process, the hydrogen from the interlayer dielectric will diffuse from the channel sides to the center, passivating the electron trap originated from excess oxygen. Though carrier concentration of the IGTO channel will increase, the devices remain normally off since the amount of donor-type oxygen vacancy has been decreased by the oxygen injection during relatively high power deposition of GI SiO$_2$. Furthermore, the effective channel length ($L_{eff}$) and channel length reduction ($\Delta L$) with $L_{eff}=L - 2\Delta L$ were extracted using transmission line method (TLM) [5]. The increase in $\Delta L$ from 0.46 to 1.5 um is indicative of hydrogen diffusion.
Figure 4. The PBTS time evolution of sample A, C, and B w or w/o annealing.

To evaluate the long-time PBTS stability of the devices after annealing, the time dependences of the ΔVth are fitted by the stretched-exponential equation which is defined as [6]:

\[
\Delta V_{th} = \Delta V_{th0}[1 - \exp\left(-\left(t/\tau\right)^\beta\right)]
\]

where ΔVth0 is the ΔVth at infinite time, \(\tau = \tau_0 \exp(E/\kappa T)\) represents the characteristic trapping time of electrons/holes. The PBTS instability of the device after 60 hours is expected to be less than 5 V.

4. Conclusions

In this work, TG-SA TFTs with crystalline IGTO active layer were studied. High carrier concentration restricted the tuning of PECVD of GI SiO2. To ensure the uniformity, relatively higher power was employed for GI deposition to reduce donor-type oxygen vacancies. Deep electron traps formed by excess oxygen lead to poor PBTS stability. The PBTS stability could be improved without deterioration of uniformity by introducing low temperature annealing, to control hydrogen diffusion from ILD layer which would passivate the electron traps.

Acknowledgments

The authors acknowledge the support from National Engineering Laboratory for AMOLED Process Technology.

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