Vertical Integration of 2D Building Blocks for All-2D Electronics

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2D materials are promising building blocks for novel electronic devices. It is possible that future electronic devices will be entirely made of 2D materials to fully realize their potential, due to their natural thinness, atomically flat surface/interfaces and diverse properties. In this work, three typical 2D materials, i.e., monolayer molybdenum disulfide (MoS$_2$), hexagonal boron nitride (hBN), and few layer graphene (FLG) serving as semiconducting, dielectric, and contact/gating materials, respectively, are assembled for vertically integrated multilayer devices via the layer-by-layer stacking process. An individual layer of all-2D field effect transistors (FETs) shows comprehensive device performances with parameters of ultralow off-current $\approx 100$ fA, ultrahigh on/off ratio approaching to $10^{10}$, ideal subthreshold swing (SS) $= 100$ mV dec$^{-1}$, and decent room temperature mobility up to 52 cm$^2$ V$^{-1}$ s$^{-1}$, benefiting from the effective dual-gate modulation and high contact quality. Vertically stacked multilayers of all-2D FETs are successfully achieved with nearly multiplied on-current density, equivalent device mobility, and persevered on/off ratio and SS of the individual layers. The vertical integration of multilayered devices with different layer functions, e.g., memory, logic and sensor, are further demonstrated. This work provides a technological base for future high-performance integrated devices based on all-2D materials.

In the past few decades, various low-dimensional materials including carbon nanotubes, oxide interfaces, 2D materials, topological insulators and semimetals, have been proposed as potential candidates in the post-silicon era.[1–13] From a technological point of view, 2D materials, especially their single-crystalline forms, are superior if considering their intrinsic thinness and potential availability at a large scale.[14–16] Besides, those 2D materials without dangling bonds at their surfaces are also stable and easy to be stacked into complexed multilayers, e.g., the so-called van der Waals (vdW) heterostructures, through artificial assembling of individual atomic layers in a chosen sequence. Such a stacking strategy is nearly free of those interface limitations, such as the lattice mismatch and inter diffusion, usually present in previous thin film deposition process.[11,17] The produced vdW heterostructures have been not only offered a great opportunity to address many novel physic problems but also used in various 2D materials based functional devices.[18–22]

So far, 2D materials have grown up to a big family. Following the discovery of graphene,[5] hundreds of 2D materials such as hexagonal boron nitride (hBN),[23] transition-metal dichalcogenides,[9,13]...
and black phosphorus,[24] just to mention a few, have been discovered. These materials possess a broad range of properties and almost all category of bulk materials such as metals, insulators, semiconductors, and superconductors can be found in their 2D counterparts. Therefore, it is possible that future devices are solely made from 2D materials by replacing conventional materials by 2D ones. Considering the thinness and ease of vertical stacking of 2D materials, such all-2D devices might offer ideal building blocks for vertical integration to increase the device capacity and reach ultimate device performances, which is also a main theme in thin-film based advanced semiconductor devices right now.[25]

In this work, we choose three typical 2D atomic crystals, i.e., few layer graphene (FLG), monolayer MoS2 and tens of layer of hBN for vertically integrated multilayer devices. The three 2D materials are all stable in air and serve as the contact/gating, semiconducting, and dielectric materials, respectively. By optimizing the device configurations and vertical assembly of different 2D materials, we successfully fabricated all-2D FETs. We further show that these devices can be vertically integrated into multilayers with vertical vias interconnects inside the stack (up to three device-layers) through repeated layer-by-layer stacking process.

**Figure 1a** shows the schematic device structure for a single layer of FETs constructed solely from FLG, hBN, and MoS2. High quality monolayer MoS2 triangles grown by chemical vapor deposition (CVD) process are used as channel materials.[26] Mechanical exfoliated FLG (0.5–3 nm) and hBN (2–50 nm) are used as contact/gating electrodes and gate-dielectric layers, respectively. Optical images of typical as-fabricated devices with both single-gate (SG) and dual-gate (DG) geometries are shown in Figure 1b. DG structure was “gate-all-around” device structure by connecting top gate and bottom gate together for driving the MoS2 channel to much higher carrier densities,[25,27,28] owing that DG structure have multiplied geometry capacitance. Please also see Figure S1 (Supporting Information) for MoS2 characterizations and Figure S2 (Supporting Information) for detailed fabrication process. Before electrical measurements, we carried out current annealing to these devices for further device cleaning and contact improving between FLG and MoS2 interface (Figure S6 in the Supporting Information). This process can improve the current density by 66 times in SG FET.

**Figure 1c–f** shows output and transfer curves of a typical FET device with the channel length (L), channel width (W), and top/bottom dielectrics thickness (hBAX) of 3 μm, 10 μm, and 47 nm/45 nm, respectively. Detailed electrical performance analyses of SG and DG FETs are listed in Figures S7–S14 in the Supporting Information. Under SG modulations, the transistor shows an on-current density (I_on/W) of ~50 μA μm⁻¹ (Figure 1c) at a bias voltage of 15 V (V_g = 19 V); while under DG modulations, it raises significantly to ~200 μA μm⁻¹ (V_g = 24 V), owing to higher electrostatic gate controllability of MoS2 channel (Figure S7 in the Supporting Information). Besides, subthreshold swing (SS) of the device can also be significantly reduced from ~200 mV dec⁻¹ for SG FET to ~100 mV dec⁻¹ for DG FET as calculated in Figure S8 in the Supporting Information. (Note that SS could decrease to the thermionic limit of 60 mV dec⁻¹ with thinner hBN as dielectric layer.) In both SG and DG measurements, a record-high on/off ratio (~10⁶ for SG FET at 10 V bias and ~10⁸ for DG FET at 5 V bias), ultralow off-current 10–100 fA and leakage current ~100 fA can be achieved.
Table 1. Summary of the device performances of various MoS2-based FETs.

| Configuration         | Layer | \( l_{on}/l_{off} \) | \( l_{on}/W \) \( \mu \)A \( \mu \)m | \( l_{on} \) | SS | \( \mu_{FE} \) | \( R_{c} \) \[ k\Omega \mu \)m | SBH \[ meV | References |
|-----------------------|-------|----------------------|----------------------------------------------------------------------------------|-------------|---|-------------|----------------|-------------|-----------|
| Dual-gate FETs        | Top gate (hBN) | 1L                  | 10^4                                    | 2.5         | 50 \*A | 74 mV dec^{-1} | 10–60          | 38          | [6,33]    |
| TT-phase contact FETs | Back gate (SiO_2) | 1–3L                | 10^4                                    | 85          | >1 \*A | 800 mV dec^{-1} | 46             | 0.24        | [34]      |
| Graphene contact FETs | Top gate (hBN) | 1L                  | 10^4                                    | 9           | 100 \*A | 93 mV dec^{-1} | 38             | 5           | [35]      |
| t-SPL FETs            | Top gate (hBN) | 1L                  | 10^9–10^10                              | 44          | 10^6 \*A | 64 mV dec^{-1} | 30             | 7            | [30]      |
| vdW contact FETs      | Back gate (SiO_2) | 1L (CVD)           | 10^9–10^10                              | 17          | 1 \*A | 10–20 V dec^{-1} | 170            | 3.3         | [32]      |
| Crested MoS_2 FETs    | Back gate (hBN) | Few layer            | 10^1                                    | 310         | 1 \*A | 1.67 V dec^{-1} | 50–800         |             | [36]      |
| Multilayer MoS_2 FETs | Back gate (Al_2O_3) | Multilayer         | <10^1                                    | 9           | 1 \*A | 70 mV dec^{-1}  | >100           |             | [37]      |
| NC FETs               | Back gate (HZO) | Few layer            | 10^1–10^2                               | 510         | 100 \*A | <60 mV dec^{-1} |                |             | [38]      |
| FLG contact FETs      | Single-gate (hBN) | 1L (CVD)          | 10^1                                    | 50          | 100 \*A | 200 mV dec^{-1} | 21             | 3.9         | 30        |
| Dual-gate (hBN)       | 1L (CVD) | 10^10                | 200                                     | 100 \*A | 100 \*A | 100 mV dec^{-1} | 52             | 1.3         | 12        |

(Figure 1d,f and Figure S9 in the Supporting Information), which are important parameters for integrated electronics, with increasing the processing speed and reducing the energy consumption. At high bias voltages, we also observed the current saturation behavior (Figure 1e), which is important in logic gates or thin film transistors applications. We also calculated the room temperature mobility \( \mu_{FE} \) of the device in both SG and DG cases, according to the following formula

\[
\mu_{FE} = \frac{l_{on}/l_{off}}{d_{i}} = \frac{1}{V_{g}C_{i}V_{ds}}
\]

where \( C_{i} \) is the normalized capacitance and the dielectric constant is \( \varepsilon \)BN = 3.455 (Figure S15 in the Supporting Information). The calculated DG-mobility is \( \approx \)52 cm^2 V^{-1} s^{-1}, which is 2.5 times larger than SG-case (Figure S7 in the Supporting Information). All these results reveal that DG electrostatic modulation of the MoS2 channels are much more effective than the SG configuration.

These excellent device performances are also a result of high contacting quality at vdW contacts between FLG and MoS2, as evidenced from the much linear \( I–V \) curves at small bias (insets of Figure 1c, e). In order to estimate the Schottky barrier height (SBH) and contact resistance \( R_{c} \) in our devices, we thus carried out cryogenic electrical measurements and transfer length method (TLM) characterizations of SG and DG FETs (Figures S11–S12 in the Supporting Information). Typical results are shown in Figure 1g from fitting source-to-drain current \( I_{ds} \) in a temperature regime of 80–280 K according to the formula

\[
I_{ds} = \frac{A_{d}x}{K_{B}T} \exp \left( \frac{q \Phi_{h}}{K_{B}T} \right) \left( 1 - \frac{qV_{ds}}{K_{B}T} \right)
\]

where \( A_{d}x \) is the 2D equivalent Richardson constant, \( q \Phi_{h} \) is the SBH, \( T \) is the absolute temperature, \( K_{B} \) is the Boltzmann constant and \( q \) is the electronic charge. At \( T = 100–250 \) K, the activated behavior fits our data very well. By fitting the Arrhenius plot of the conductance in the insulating regime, we obtained SBH of 30/12 meV for SG/DG device configurations as shown in Figure 1g. Besides, the extracting \( R_{c} \) minimum value at different gate voltages \( V_{G} \) is \( 3.9/1.3 \) k\( \Omega \) \( \mu \)m for SG/ DG configurations (Figure 1b). Small SBH and \( R_{c} \), i.e., 12 meV and 1.3 k\( \Omega \) \( \mu \)m, are among the lowest ones reported previously, suggesting FLG is an excellent electrode for contacting monolayer MoS2.

In Table 1, we summarize typical electrical performances of various MoS2-based FETs from the previous results in literature. We can see that our devices feature comprehensive device parameters with low \( R_{c} \) and SBH, high on-current density, extremely low off-current, a record-high \( I_{on}/I_{off} \) ratio, high \( \mu_{FE} \) and ideal SS value, which are comparable to the best values in recent works. Due to passivation effects of the hBN capsulation in our DG device structure, nearly absence of charge traps or contaminations at the interface of these atomic crystals are also expected and confirmed to some extent from the small hysteresis (Figure S7 in the Supporting Information) and stable threshold voltages in transfer curves and their long term (up to 6 months) stability in ambient conditions (Figure S14 in the Supporting Information). Moreover, from the insets of Figure 1g, we can see that SG FET is always working in the insulated regime, but an obvious metal–insulator-transition (MIT) at \( V_{G} \approx 10 \) V can be seen for DG FET. Temperature-dependent device mobilities of DG FET were extracted in Figure S13 in the Supporting Information. At \( T > 100 \) K, mobility can be fitted by \( \mu = T^{-\gamma} \) with \( \gamma = 0.72–1.34 \) which is close to the predicted value of \( \gamma = 1.52 \), suggesting an electron–phonon scattering dominated transport behavior at high temperatures. At low \( T \), \( \mu_{FE} \) can be enhanced to \( \approx 182 \) cm^2 V^{-1} s^{-1} and saturated below 40 K, indicating that hBN capsulation could effectively suppress the Coulomb scattering on electron impurities and improves the mobility.

Based on the single layer of all-2D DG FETs with symmetry structure and ideal device performance as described above, next we fabricated the vertical integrated multilayer FETs through a repeated layer-by-layer assembling process (detailed fabrications shown in Figure S3 in the Supporting Information). Figure 2a shows the schematic stacking of 16 individual layers of 2D materials, resulting to three layers of assembled devices. As-fabricated devices after different fabrication stages, from 1 to 3 device layers, are shown in Figure 2b.
hBN insulating layers was designed to have a similar thickness (Figure S4 in the Supporting Information) in order to avoid layer-to-layer fluctuations in performances. Note that, in these devices, the source/drain/gate electrodes were vertically connected inside the stacks from one device layer to another through metal interconnects during the layer fabrication process, thus forming an assembled equivalent device with multiplied, parallel and fully gated conduction channels of monolayer MoS\textsubscript{2}. For example, the marked 2L and 3L devices can be formed by interconnecting the 1st–2nd and 1st–2nd–3rd device layers accordingly.

For these assembled multilayer devices, multiplied current capacities are expected as reference the total resistance model (Figure S17 in the Supporting Information). \textit{I–V} and transfer curves of 1L, 2L, and 3L equivalent devices are shown in Figure 2c,d, respectively. (Details of electrical measurements of multilayer FETs shown in Figures S16 and 17 in the Supporting Information.) We can observe that the current densities multiples with vertical integrated device layer as 1L, 2L, and 3L devices have an equivalent current density of 18, 35, and 54 μA μm\textsuperscript{-1}, respectively, at \(V_{ds} = 1\) V, \(V_{gs} = 12\) V (Figure 2c), as expected. Surprisingly, the off-currents of all assembled devices show no obvious change and all stay at the level of 10–100 fA (Figure 2d). We attribute this anomalous behavior to the detection limit of our measurement set-up, that is, the off-current of an individual device is at the same level to the instrument noise (10–100 fA at the present case). As a result, an equivalent on/off ratio of 10\textsuperscript{10} and SS of ≈100 mV dec\textsuperscript{-1} can be well preserved in these device assemblies. We also calculated the equivalent \(\mu_{FE}\) of the vertically assembled multilayer FETs (Figure S17 in the Supporting Information), which multiplies with the assembled device layers. For example, \(\mu_{FE}\) of 3L devices can reach up to ≈145 cm\textsuperscript{2} V\textsuperscript{-1} s\textsuperscript{-1} at a room temperature. Such significant improvement in the device mobility therefore offers a solution to overcome the intrinsic mobility limitation in MoS\textsubscript{2} based FETs. Note that, another possible way to increase the mobility in a MoS\textsubscript{2}-FET is to employ multilayer MoS\textsubscript{2} as the channel material in order to increase the channel thickness.[37,39] In contrast, due to the weak gate tunability and screening effect in such devices, the mobility enhancement is very limited meanwhile sacrificing devices’ on–off ratio, SS, and off-current.

Based on the technique of assembling multilayer FETs, we further demonstrated vertical integration of all-2D multiple functional device layers to show the versatility of the vertical integration electronic system.[4,22] As an example, memory, logic, and sensor layers were demonstrated. The technique routes, detailed fabrications and corresponding optical images of multilayer functional devices is shown in Figure S5 in the Supporting Information. FLG gate, FLG contact/inner-connect and BN layers are marked by black dashes lines, black lines and other-color dashed lines, respectively. Finally, we performed the cooperative working demonstration between optical sensor and floating gate memory devices. Note that the optical sensor (3rd layer) cooperatively work with floating gate memory (1st layer)
here is used only for demonstration purposes; the top device layer (sensor) could be replaced with other forms of sensing layer as inputs or other logic, data storage devices, etc.

For the memory layer, three two-terminal nonvolatile floating gate memory devices were fabricated by vertically stacking FLG/hBN/MoS2 with FLG contact and appropriate hBN thickness (Figure 3a and Figure S5e in the Supporting Information). Figure 3d shows I–V switching of a typical memory device with the programming and erasing process, respectively. e) Output voltage $V_{\text{out}}$ of the inverter as a function of input voltage $V_{\text{in}}$, with drain-to-drain voltage $V_{\text{dd}}$ varying from 1 to 10 V (inverter is constructed by interconnecting devices L1–L2 in 2nd device layer). Insets are the schematic and the maximum gain value which approaches to 300 at $V_{\text{dd}} = 10$ V. f) Output voltage of the logic NAND gate at four typical input states with $V_{\text{dd}} = 1.5$ V (NAND gate is realized by interconnecting devices L1–L2–L3 in 2nd layer). g) Static photosresponse of the optical sensor under both dark and blue light environments (light power $P_{\text{blue light}} = 30$ mW cm$^{-2}$). Bias is 1 V. Inset shows the specific detectivity of the photodetector. h) Dynamic photosresponse of the optical sensor at different gate voltages with 1 V-bias reading. Light is turned on (blue shadow) for 5 s then turned off for 5 s. i) The cooperative working between sensor and memory functional layers. The RS of memory device (M3), outlined by the red dash line, is gradually changed with the signal from optical sensor (S1).
approaches to 300 V V$^{-1}$ at $V_{dd} = 10$ V. For NAND logic gate, the logic functions could be successfully demonstrated in Figure 3f at four typical input states with $V_{dd} = 1.5$ V.

For the upper sensor layer, we fabricated three individual MoS$_2$ FETs as optical sensor (Figure 3c). Figure 3g shows the static transfer curves of the photodetector working under both dark conditions and blue light with power of $P = 30$ mW cm$^{-2}$. Higher on/off ratio could be obtained at negative gate voltages. The calculated maximum photoresponsivity ($R$) is 6330 A W$^{-1}$ at $V_g = 0$ V (Figure S20b in the Supporting Information) and maximum detectivity ($D^*$) is larger than 10$^{10}$ Jones at $V_g = -7$ V (inset of Figure 3g). Figure 3h shows time-resolved dynamic photoresponse of the sensor at different gate voltages with 1 V bias reading. During the measurements, light is turned on (blue shadow) for a period of 5 s then turned off for another 5 s.

The cooperative working demonstration was performed between optical sensor and floating gate memory with an electrical amplifier (Figure S21 in the Supporting Information). For simplicity, different functional layers were connected through external wiring. The photocurrent of the optical sensor could be enlarged to 10 V output voltages with the amplifier magnification of $\times 20000000$ V A$^{-1}$. Then, the 10 V output voltage signal was loaded on the memory device (initialized to HRS). Figure 3i shows the output signal of the memory device. The output signal is on the order of $3 \times 10^{-5}$ A when the light is on ($\sim$ 10 V for operation) and the output signal is $10^{-7}$–$10^{-6}$ A when the light is off ($\sim$ 0.5 V for reading). The RS of memory device changes with the optical pulse numbers indicating that the carriers could tunnel through hBN dielectric layer and store on floating gate, thus, the MoS$_2$ memory could be tuned higher conductance states.

In summary, we demonstrate high performance all-2D materials FETs, vertical integration of multilayer FETs with vertical interconnects and multilayer functional devices with cooperative working relationship. This vertical integration electronics based on all-2D materials hold the potential for new generation of sensing–processing–computing nanosystems and advanced electronic applications. Although the fabrications in this work are at a quite small scale and complicated, large scale integration can be envisioned in the near future if considering the recent rapid progress on scalable growth$^{34-36,42}$ and transfer$^{11,42}$ of various high-quality 2D materials.

**Experimental Section**

**Materials Preparation:** High-quality CVD-grown, sub-millimeter and monolayer MoS$_2$ single crystals were selected as channel materials for fabricating FETs. The growth process of MoS$_2$ triangles was carried out in a three-temperature zone CVD system$^{24}$ (Alfa, 99.5%, 8 g) powder and MoO$_3$ (Alfa, 99.9995%, 30 mg) powder was used as reaction sources. 2 in. c-plane polished sapphire wafers annealed in O$_2$ atmosphere at 1000 °C for 4 h were used as substrates. During the growth, carrier gases of Ar (40 sccm) and Ar (240 sccm)/O$_2$ (4 sccm) were fluxed for S power and MoO$_3$ individually and the pressure in the chamber was $\approx$ 1 Torr. The temperature was held at 130, 530, and 930 °C for S-source, MoO$_3$-source and substrates. Each growth run lasts about 30 min. High quality hBN and FLG flakes were exfoliated from larger grain size bulk BN crystals and natural flaggy graphite flakes (purchased from NGS Trading & Consulting GmbH, Germany). Large-scale FLG and hBN flake ($\geq$ 200 $\times$ 200 μm$^2$) can be obtained by poly-propylene-carbonate (PPC) assisted thermal exfoliation methods.

**Device Fabrications:** The MoS$_2$ triangles on a sapphire substrate were first spin-coated by a μm-thick polyethylene-methylacrylate (PMMA) layer then etched in KOH solution (1 mol L$^{-1}$, 110 °C) for 30 min. The as-received MoS$_2$ triangles supported on PMMA films, FLG or hBN flakes hold by poly-propylene-carbonate (PPC) films were stacked precisely through layer-by-layer stacking methods in our homemade transfer station according to the assembling sequence listed in Section S2 of the Supporting Information. The sacrificial layer of PMMA or PPC can be removed by rinsing in acetone for $\geq$ 1 h at a room temperature. The contact between FLG and MoS$_2$ channel was patterned through electron beam lithography (EBL) and oxygen reactive ion etching (RIE) process and aligned together. The vertical metal via interconnected inside the hBN layer were etched by CHF$_3$/O$_2$ plasma by RIE. Devices were finally wired out by Ti/Au electrode for electrical measurements.

**Spectroscopic and Electrical Characterizations:** The Raman and PL spectra were acquired from a Horiba Jobin Yvon Lab RAM HR-Evolution Raman system with a 532 nm He–Ne laser (spot size = 1 μm, power 10 mW) in ambient conditions. Surface morphology was characterized by atomic force microscope (Asylum Research Cypher S instruments) with AC160 TS tip under the tapping mode. The electrical measurements were carried out in a close-cycle cryogenic (liquid N$_2$) probe station and cryogenic Dewar (Janis, liquid He) equipped with an Agilent 4156C and B1500 semiconductor parameter analyzers. All the measurements were carried out in vacuum at a base pressure of $10^{-6}$ Torr.

**Supporting Information**

Supporting Information is available from the Wiley Online Library or from the author.

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**Conflict of Interest**

The authors declare no conflict of interest.

**Author Contributions**

G.Z. conceived the idea and supervised the experiments. J.T. fabricated the devices and carried out the electrical measurements. Q.W. and Z.W. supplied high-quality MoS$_2$ films. K.W. and T.T. supplied high-quality hBN crystals. J.T. and G.Z. analyzed data and wrote the manuscript, and all authors discussed and commented on it.

**Keywords**

2D electronics, 2D materials, vertical integration
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