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A generic method to control hysteresis and memory effect in Van der Waals hybrids

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Abstract
The diverse properties of two-dimensional materials have been utilized in a variety of architecture to fabricate high quality electronic circuit elements. Here we demonstrate a generic method to control hysteresis and stable memory effect in Van der Waals hybrids with a floating gate as the base layer. The floating gate can be charged with a global back gate-voltage, which it can retain in a stable manner. Such devices can provide a very high, leakage-free effective gate-voltage on the field-effect transistors due to effective capacitance amplification, which also leads to reduced input power requirements on electronic devices. The capacitance amplification factor of ~10 can be further enhanced by increasing the area of the floating gate. We have exploited this method to achieve highly durable memory action multiple genre of ultra-thin 2D channels, including graphene, MoS2, and topological insulators at room temperature.

The exfoliation of graphene, which provided the platform for the subsequent discoveries of several other atomically thin two-dimensional (2D) materials such as MoS2, hBN, and Bi-based topological insulators (TIs) have led to a revolution in the research of devices [1–11]. The weak interlayer van der Waals coupling allows these materials to be exfoliated even down to a single atomic layer, displaying several novel phenomenon. Some of the remarkable properties displayed by the Dirac Fermionic carriers in graphene and topological insulators (TIs) include room temperature quantum Hall effect, superconductivity, and quantum anomalous Hall effect [4, 12–18]. MoS2 is one of the most important members of the transition metal-dichalcogenide family, and has found numerous applications in electronics, optoelectronics, piezoelectricity, and valleytronics [7, 19–23]. The diverse properties of these materials have been best exploited by fabricating hybrids out of them, by stacking one on top of the other, leading to state-of-the-art sensors, and providing a solid platform for further miniaturization of devices and faster electronics [8, 9, 16, 18, 19, 24–42].

One major area of thrust with Van der Waals hybrids has been to achieve non-volatile, durable memory action, which provide several advantages such as reduced power consumption, higher integration density, and enhanced life-times [43, 44]. In this work, we have demonstrated a generic device architecture to achieve non-volatile memory effect in stacked made using 2D materials in a floating gate geometry [45–48]. While the floating gate geometry has been exploited in case of transition metal dichalcogenide-based in 2D atomic/molecular layers, it’s applicability for a broader range of 2D materials, and an optimization of the architecture itself, remains unexplored. The floating gate can be charged by the application of a back-gate voltage (V\textsubscript{BG}). The charge remains stored even after the gate-voltage is switched off due to lower back transfer probability, and gives rise to higher effective gate-voltage compared to that of the standard 285 nm SiO\textsubscript{2}. The cyclic charge trapping due to V\textsubscript{BG}-dependent band-bending leads to a large hysteresis window, which can be accurately tuned by controlling the area of the floating gate. This effect can be utilized in a variety of devices such as extremely robust low power,
non-volatile memory applications using MoS$_2$, which is difficult to achieve with graphene due to the absence of any band-gap. The high effective $V_G$ can also be implemented to achieve ambipolar transport in topological insulators, and highly repeatable large hysteresis window, even at room temperature. Attaining ambipolar transport usually requires a large gate-voltage, and low temperature due to high residual bulk doping. Such devices can be utilized for exploring several properties of Dirac Fermions in TIs when access to the surface states is required.

The durable memory action in our devices is made possible due to the presence of the floating gate. Floating gate MOSFETs (FGMOS) have been extensively used as in memory applications such as EPROMs (Erasable Programmable Read Only Memories) and EEPROMs (Electrically Erasable Programmable Read Only Memories), and can be used in neural networks as well [46, 49, 50]. With substantial improvement of the fabrication techniques and the emergence of two-dimensional materials, such circuits can be implemented using entirely Van der Waals materials, leading to further miniaturization. The advantage of using a floating gate rests in the amplification of the equivalent capacitance ($C_{eqv}$), and hence the effective $V_G$ on the channel, which is our case, is graphene, MoS$_2$, and TIs. A typical schematic to understand the capacitance amplification in the present scenario is illustrated in figure 1(a). Let $C_1$ be the capacitance between the graphene channel and the 2DM underlayer. The thickness of this capacitor is equal to the thickness of hBN ($d_{hBN}$), which also acts as the tunnel barrier in these devices. The area of the capacitor is equal to the area ($A$) of the channel. Let $C_2$ be the capacitance between the Si back gate and the 2DM underlayer, whose thickness is equal to the thickness of SiO$_2$ ($d_{SiO2}$), and the area is equal to the area of the underlayer ($A_{2D}$). Let us now assume that the area of the underlayer is equal to the area of the channel ($A_{2DM} = A$), which is illustrated in figure 1(a). Since $C_1$ and $C_2$ both have the same area and the dielectric constant of hBN and SiO$_2$ are also similar ($\varepsilon_r \sim 4$), we can write $C_1 = nC_2$, where $n = d_{SiO2}/d_{hBN}$. If $V_G$ is applied on the Si gate, and $V_0$ is the voltage at the underlayer, since the charge induced on the underlayer and the channel is same, we can write

$$C_2(V_0 - V_0) = C_1 V_0$$

$$V_0 = \left(\frac{C_2}{C_1 + C_2}\right)V_G$$

In real devices, however, the area of the underlayer is always larger, and can be expressed as $A_{2D} = A + xA$. Here $A$ is the part of the underlayer that is lying underneath the channel, and $xA$ is the extended part of the underlayer located outside the channel area. In such a scenario, the capacitance between the Si gate and the underlayer ($C'_1$) can be expressed as $C'_1 = C_2 + xC_2$, which is schematically represented in figure 1(b). This implies that the voltage at the underlayer $V_A$ can be expressed as,

$$V_A = \left(\frac{C_2(x + 1)}{C_1 + xC_2 + C_2}\right)V_G$$

Figure 1. Basics of capacitance amplification: (a) The top panels show the capacitance circuits for devices without and with extended underlayers, respectively. $C_1$ and $C_2$ are underlayer to channel and underlayer to back gate capacitances (with area equal to the area of the channel), respectively. $xC_2$ is the capacitance between the extended part of the the underlayer and the back gate. (b) The bottom panels show typical device schematics without and with the extended underlayer.
The capacitance amplification ($A_V$) in our devices is defined as the ratio of $V_A$ and $V_G$. It can be expressed as

$$A_V = \frac{V_A}{V_G} = \frac{C_2(x + 1)}{C_1 + C_2(x + 1)} \times \frac{C_1 + C_2}{C_2}$$

(3)

Using the relation $C_1 = kC_2$ and considering the fact that both $k$, $x > 1$, equation (3) can be rewritten as

$$A_V = \frac{(x + 1)(k + 1)}{x + k + 1} \approx \frac{xk}{x + k}$$

(4)

Equation (4) clearly enunciates that the effective $V_G$ can be further enhanced by the increasing area of the underlayer, a property which has been exploited in our present work.

The devices studied in this manuscript have been fabricated from several two dimensional materials such as single layer graphene (SLG), molybdenum disulphide (MoS$_2$), Bi-based chalcogenide Bi$_{1.6}$Sb$_{0.4}$Te$_2$Se topological insulators (TIs), and boron nitride. While the top channel is formed by graphene, MoS$_2$, and TIs, the floating gate is primarily made of single or multi-layer graphene, and MoS$_2$. In certain devices, the area of the floating gate has been extended by depositing 20 nm Au, which is connected only to the 2D underlayer only. In all our devices, hBN forms the tunnel barrier between the channel and the floating gate. In order to process these devices, graphene, MoS$_2$, Bi$_{1.6}$Sb$_{0.4}$Te$_2$Se, and hBN were separately exfoliated on standard 285 nm SiO$_2$/Si substrate, followed by the fabrication of the required hetero-structure in a home-made transfer assembly. The contacts were patterned by standard electron beam lithography followed by thermal evaporation of 5/30 nm Cr/Au for source, and drain electrodes. All resistivity measurements were performed using a lock-in amplifier with a carrier frequency of 227 Hz, in a home-made variable temperature cryostat.

The preliminary transfer characteristics of a typical device using the floating gate geometry with single layer graphene as the top channel (figure 2(a)) is shown in figure 2(b), which exhibits two distinct features. Firstly, the transport in the graphene channel with 2DM underlayer displays a strong hysteresis between the forward and backward $V_G$ sweeps, while the standard hysteresis-free $R$ vs $V_G$ is restored when the 2D underlayer is absent. Secondly, the sharpness of the transfer characteristics is significantly enhanced in the presence of the 2D layer, suggesting an increase in either the carrier mobility in the channel or the effective capacitance. Since hBN is the common substrate to the entire channel, both effects can only be due to the presence of the 2D underlayer. Both these effects, however, are absent when the 2D underlayer is electrically grounded, and the transfer characteristics is determined by the extent of $V_G$-dependent screening by the doped 2D layer (see supplementary section A available online at stacks.iop.org/MRX/7/014004/mmedia). The extent of (anti-)hysteresis can be
Figure 3. Features of MoS2-FETs with a floating gate: (a) Graphical illustration of a typical MoS2 device. The bottom panel shows a hybrid after transfer, while the right image shows an optical micrograph of an actual device. (b) Hysteresis observed in MoS2 devices. Inset shows calculation of sub-threshold swing ($S = 80 \text{ mV/decade}$ for the representative device). (c) Temporal dependence of drain current after a program ($-9/7 \text{ V}$) or erase ($+9/7 \text{ V}$) pulse for a drain bias of 10 mV (yellow line) and 50 mV (blue line). (d) Demonstration of the repeatability of memory action for over 100 cycles of program and erase pulse. The memory ratio, defined as the ratio of the on and off state current, for 100 cycles is shown in the inset.

reduced, and eventually completely removed, by decreasing the sweep range below a critical value $V_{CG} (\pm 12 \text{ V})$ for the device in figure 2(c)), which suggests that the total trapped charge in the 2DM layer remains fixed as long as the sweep range is below $V_{CG}$ around the Dirac point. The enhanced sharpness of the transfer characteristics in the presence of the 2DM underlayer, however, has negligible effect on the range of the $V_{CG}$ sweep.

To understand its origin, we have extracted the carrier density $n$ in the channel directly from Hall measurements. The measured $n$ for forward and backward sweeps over a sweep range of 60 V is shown in figure 2(d). The dependence of $n$ on $V_{CG}$ is also (anti-)hysteretic, with the Dirac points coinciding with the reversal in the sign of the carriers. Around the Dirac points $n$ varies linearly with $V_{CG}$, and the total capacitance ($C_G$) is obtained from the slope. Evidently, $C_G$ is considerably larger than $C_0$ (slope of the solid line in figure 2(d)), where $C_G^{-1} = (C_{SiO_2}^{-1} + C_{2DM}^{-1} + C_{hBN}^{-1})$ is the sum of the respective geometric capacitances of SiO$_2$, 2DM and hBN layers in series. Here $C_{SiO_2} = \varepsilon_0 \varepsilon_{SiO_2} / d_{SiO_2}$ and $C_{hBN} = \varepsilon_0 \varepsilon_{hBN} / d_{hBN}$, where $d_{SiO_2}$ and $d_{hBN}$ are the thicknesses of the SiO$_2$ and hBN layers, respectively. $C_{2DM}$ is usually 10–100 times larger that $C_{SiO_2}$ and $C_{hBN}$, and can be neglected. This confirms that the sharpness in the $R \sim V_{CG}$ characteristics is indeed due to enhanced $C_G$, rather than an improbable increase in the carrier mobility in the channel region just above the 2DM underlayer. By restricting the sweep range below $V_{CG}$, the variation of $n$ with $V_{CG}$ can be made completely non-hysteretic, irrespective of the location of the Dirac point, i.e. the extent of trapped charge in the 2DM underlayer. Figure 2(e) illustrates this at three locations of the Dirac point.

The clockwise hysteresis (i.e. anti-hysteresis) of $R \sim V_{CG}$ in figure 2(f) is the effect of cyclic charge trapping by the 2DM due to $V_{CG}$-dependent bending of the hBN bands, and has been recently observed in memory devices based on trilayer Van der Waals hybrid of similar architecture [45, 47]. When $V_{CG}$ increases in positive or negative directions from the Dirac point, the transfer of electrons or holes from the graphene channel to the 2DM causes an effective gate voltage shift, that can be erased only by reversing the polarity of $V_{CG}$. The enhancement in $V_A$ is limited by the band gap $\Delta_{hBN}$ of hBN, and for voltage $|V_{CG}| > \Delta_{hBN}$, electric field–induced band bending within hBN will cause charge to flow across the dielectric, thereby pinning the Fermi level of the channel. This allows us to estimate both $\Delta V_{CG} \sim \Delta_{hBN} C_{hBN} / C_G$, as well as the saturation carrier density $n_{max} \sim \varepsilon_0 \varepsilon_{hBN} \Delta_{hBN} / \varepsilon_{SiO_2} d_{SiO_2}$ both of which could be directly verified from their dependence on $d_{SiO_2}$. Further amplification of the effective capacitance can be achieved by enhancing the area of the floating gate, which can be done by connecting the underlayer with Au. Using this, $A_V$ has been found to increase by an order of magnitude (See Supplementary section B).

One of the shortcomings of graphene is the lack of a band-gap, rendering it unsuitable for non-volatile memory based applications. To circumvent this, we have utilized the floating gate technique in an MoS2-FET to evoke the possibility of high performance and power efficient non-volatile memory devices. The device structure is shown in (figure 3(a)) where the graphene and molybdenum disulphide layer have been interchanged from (figure 2(a)). Similar hysteresis is also observed when MoS2 forms the top current carrying layer as demonstrated in figure 3(b) due to the screening of back gate electric field by the trapped charges in the floating gate. Such structures have been previously investigated in [45, 47, 51]. One of the major parameters that
determine electronic device performances is the sub-threshold swing. It is defined as the amount of gate voltage bias required to change the source-drain current ($I_{sd}$) by one decade, and is given by the following expression,

$$S = \frac{\delta V_G}{\delta (\log I_{sd})} = \frac{\delta V_G}{\delta \psi_S} \frac{\delta \psi_S}{\delta (\log I_{sd})}$$  \hspace{1cm} (5)

Here $S$ is the surface potential in the channel. The second term in the equation (5) has Boltzman theoretical limit of 60 mV/decade at room temperature while the first term, known as the body factor is given by

$$\frac{\delta V_G}{\delta \psi_S} = 1 + \frac{C_S}{C_{eqv}}$$  \hspace{1cm} (6)

where $C_S$ is the quantum capacitance of the channel. The equivalent capacitance for our extended floating gate structure is the capacitance of the hBN dielectric, which is much larger than that of the 285 nm SiO$_2$. From equation (6) it is clear that higher the equivalent capacitance, lower is the value of sub-threshold swing (5) leading to faster switching, and reduced power consumption. The higher capacitance per unit area of hBN allows us to reduce the body factor significantly leading to almost ideal subthreshold slope in all the measured devices for over four decades of $I_{sd}$ as shown in the inset of figure 3(b).

The large memory window and the near ideal subthreshold swing (figure 3(b)) make the extended floating gate MoS$_2$ devices perfect candidates for non-volatile memory storage. The binary memory action is depicted in figure 3(c) with a ON/OFF ratio of $\approx 10^4$ at a drain bias of 50 mV, with a pulse time of 1 sec. The pulse rise time has a significant effect on the on/off ratio, which is expected due to increased storage of charges on the floating gate, and is depicted for pulse widths of 0.1, 1, and 10 msec (Supplementary section C.1). The devices also show excellent retention, with negligible change of $I_{sd}$ upto $\sim$10000 secs for all three pulse times (Supplementary section C.1). To obtain the switching transition, a program and erase pulse of +9 and −9 V respectively was applied to the silicon back gate. The memory action is robust and repeatability has been checked for 100 program and erase cycles (figure 3(d)). We find a very low cycle to cycle variability in the memory ratio, defined as the ratio of the on and off state current, demonstrating the reliability of these non-volatile memory devices (inset of figure 3(d)). Furthermore, the memory ratio in our devices, which can be as high as $10^8$, is comparable to state of the art sensors fabricated with two-dimensional materials, that have reported in literature (Supplementary section C.2)\[52–59\]. Additionally, the low bias requirements and program state current value makes the device power efficient with an observed power dissipation of $\approx$10 pW in the program state in our MoS$_2$ based memory devices \[51\]. A lower stress on the gate dielectric due to reduced program and magnitude improves the reliability of these devices making them ideal for low power portable memory applications.

We have further exploited this technique by using topological insulators (TIs) as the conducting channel. High bulk conductivity due to doping from defects in the bulk makes it difficult to tune the Fermi level across the Dirac point, and achieve ambipolar transport. This severely limits the T range for practical applications of TIs since the surface transport regime remains inutile. This problem can be circumnavigated either by going to very low temperatures, where the bulk doping is suppressed, which is not a feasible solution for several practical applications, or by using an ionic liquid top gate, can degrade the device characteristics due to intercalation of ions \[60–65\]. To address this, we have utilized capacitance amplification to access the Dirac Fermion dominated transport regime, even at high T. To fabricate the devices, the TI Bi$_{1.6}$Sb$_{0.4}$Te$_2$Se was used, which offers reduced bulk conductivity due to reduced program and magnitude. The scanning electron micrograph of a typical device with MoS$_2$ as the floating gate is shown in figure 4(a). The $R - V_G$ as shown in figure 4(b) shows ambipolar transport at $T = 22$ K, and remarkably at $T = 300$ K as well. Similar transfer characteristics were observed in devices with multi-layer graphene as the floating gate (Supplementary section D.1). Such large and controlled hysteresis in TI-FETs clearly demonstrate that they can be used in non-volatile memory operations at room temperature. The percentage change in $R$, however, is $\sim$10%–20%, which implies that only the bottom surface is affected by the $V_G$, and the top surface remains unaffected due to screening of $V_G$ by the bottom surface and the bulk. The measured $R$ is possibly limited by the top surface, and any residual bulk conducting channels. To verify the ambipolar nature of transport, we have performed Hall measurements in the sample at different $V_G$-s across the Dirac point. The Hall number density ($n$), extracted using $R_H = -\frac{V_y}{I_y R_2} = \frac{1}{ne}$, is shown in Figure 4(c), as a function of $V_G$, where $R_H$ is the Hall co-efficient. The number density shows a clear change in sign across the Dirac point, thus validating the ambipolar nature of transport in our TI devices. The capacitance of the stack can be estimated using $ne = C_{eqv}(V_G - V_D)$, and is equal to $7.5 \times 10^{-4}$ F, which is $\sim$6 times larger than the 285 nm SiO$_2$ dielectric. The $R-V_G$ data for several sweep rates clearly indicates that the hysteresis is independent of the sweep rate (Supplementary section D.2). From $R - V_G$ at different temperatures, the impurity density as well as mobility of the TIs can be extracted from $T = 22$–$300$ K (Supplementary section D.3). The mobility of the sample increases as the $T$ is reduced, as expected. However, the value of mobility is low ($<50$ cm$^2$V$^{-1}$S$^{-1}$) at low
Manifold when the SiO2 substrate is replaced by the atomically flat BN, where the effect of trapping-detrapping and dangling bonds on the electrical transport in the sample is significantly reduced. This clearly signifies that the low mobility in TI samples can be attributed to the contribution of bulk defects which act as the dominant scattering centers [68–71], and provide an intrinsic limit to the mobility.

In summary, we have utilized capacitance amplification due to a floating gate in Van der Waals hybrids fabricated out of graphene, MoS2, and topological insulators. The increase in effective capacitance leads to an increase in the effective gate-voltage on the conducting channel, which shows a large hysteresis due to cyclic trapping and detrapping of charges. This effect has been used in a variety of ultra-thin materials like graphene, MoS2, and topological insulators to demonstrate highly stable, non-volatile memory response at room temperature. Our work provides a framework for employing hybrids of atomically thin quantum materials for memory-based applications requiring high durability, and low power.

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