Design of SRIO Reconstruction and Switching Network Architecture

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Abstract. The image processing system of the parallel processor array will face the problems of complex system structure, long development period and the inability to flexibly adjust and upgrade the platform hardware. This paper proposes a design concept of dynamic reconfiguration hardware architecture and a compatible design. Dynamic reconstruction and dynamic reconstructed image processing system of image algorithm. At the same time, CPS1848 is used as the SRIO switch chip as the switching core of the high-speed data network and a switching network routing method is designed. Tests have proved that the transmission performance of the system's SRIO high-speed data internetwork meets the requirements. Compared with previous image processing devices, the system can flexibly meet the task requirements of multiple application scenarios; improve the versatility of the device and save hardware resources and equipment costs.

1. Introduction
The so-called reconfiguration is the way in which the hardware system dynamically changes the configuration structure and functions in the circuit without changing its own hardware resources. His is mainly through the reconfiguration of the programmable devices in the system to achieve system reconstruction. Through system reconfiguration, the system can meet the needs of various occasions without changing the hardware, and it can also save hardware resources and equipment production costs, and has the advantages of flexible configuration and high efficiency. His dynamic reconfiguration means that in the process of using the system, the reconfiguration instruction is responded to in real time without interruption, and the next task is executed quickly after reconstruction.

The Institute of Image Recognition and Artificial Intelligence at Huazhong University of Science and Technology designed and developed a multi-DSP parallel system reconfiguration framework using FPGA to realize interconnection. By implementing a software communication protocol between DSPs on the FPGA, the internal FIFO is used to interconnect the DSP. The architecture of the system is an interconnected FIFO network structure. Every two DSPs are connected by a FIFO. Changing the FPGA program can change the parallel system structure. It can enhance the processing capability of the system through dynamic reconstruction and also enhance the flexibility of the system.

China Electronics Technology Group Corporation has developed a dynamic reconfigurable system based on CPCI [1]. The main controller uses Xilinx's VIRTEX 5, and the FPGA core processor is TI's TMS320C6455 DSP and VIRTEX 6 FPGA. Using host computer software to send the configuration file to the main control FPGA through the CPCI bus, the main control FPGA completes the dynamic loading of the core processor DSP and FPGA, and can complete the entire system reconstruction process through the CPCI bus [2] control, inspection, information storage and other functions, this party enters the human-computer interaction interface, greatly improves the convenience and occupancy time of the operation than the traditional reconstruction methods, and can quickly complete the different functions
and work of the device through the man-machine interface. The rapid switching of modes greatly increases the scalability and operability of the system.

It can be seen that in practical applications, the dynamic reconstruction method is not limited to implementing hardware multiplexing by directly modifying the logic code in the FPGA, but can also achieve the effect by the on-line computer programming or configuring the FPGA and the DSP at the same time. Therefore, in the process of designing the reconstruction system, the main consideration is to be able to reconfigure the hardware resources and achieve the effect of different functions and applications.

2. Hardware structure analysis

2.1. PS1848 switching chip

All SRIO port devices use IDT's SRIO switching chip CPS1848 as the switching center. As shown in the chip block diagram of Figure 1, configuring their operating modes requires the use of a JTAG interface or I2C interface to configure their registers and routing tables. The transmission mode and connection status between all SRIO devices of the chip.

![Figure 1. PS1848 Interface and Internal Structure](image)

The CPS1848 switch chip supports the SRIO 2.1 standard switch chip, with up to 240Gbps data throughput and 48 bidirectional data differential pairs(lane). It can be configured into 1x, 2x, and 4x three-port modes and can be configured to a maximum of 18 1x. Or 12 4x ports, the speed of each lane can be set to 1.25 Gbit/s, 2.5 Gbit/s, 3.125 Gbit/s, 5 Gbit/s, or 6.25 Gbit/s. The CPS1848 application is intended for large processor clusters or backplanes. It supports multiple topologies and can be configured in a flexible manner.
2.2. Topology reconstruction based on switch chip

Based on the switching chip topology connection shown in Figure 2, each SRI0 port device is connected to the switch chip through the SRI0 bus, and each SRI0 port device ID number is fixed, in the reconstruction process through the ARM through the I2C interface The CPS1848 registers are configured to complete system reconfiguration. And ARM must control through the instruction of PC. When the system is powered on, ARM configures the CPS1848 as the I2C master device through the PIN-MM_N pin to first read the default configuration in the EEPROM and write the configuration to the CPS1848. By default, the full port broadcast mode is used. he dynamic and dynamic reconstruction image processing measurement and control system software runs in the windows system. Ethernet introduces a dynamic reconfiguration control link. The ARM configures the CPS1848 as a slave mode. In the software, it uses the communication protocol between the serial port and the ARM. The configuration instructions of the upper software are converted to the I2C host interface of the ARM and online configuration is performed. The switching mode and port interconnection mode of the SRI0 switch chip are changed in real time, so that the SRI0 port device is reconfigured according to the application requirements or actually expanding the board card requirements of the interface.

3. Design of SRI0 reconfiguration switching network architecture

3.1. Dynamic refactoring process

Dynamic reconstruction is divided into two application scenarios: system-wide reconstruction and system partial reconstruction. System-wide reconstruction scenarios are commonly used. Generally, all system topologies are replaced to complete specific algorithm verification scenarios. Local dynamic reconfiguration may occur when the algorithm flow has special conditions that need to be hot-swapped to add new devices or need to maintain the execution state of the algorithm to change the topology of the system connection. Local dynamic reconfiguration reconstructs the specified local port connection device based on the system-wide reconfiguration. After the local system reconfiguration process is mastered, the locally-processed port is configured as all ports that need to be reconstructed and the local area is reduced. The data isolation operation can be performed during system reconfiguration. Therefore, this section only designs a local dynamic reconstruction method.

In general, the local reconstruction process can be divided into 3 steps, and the port device insertion/reset is prepared for the pull-out/reset. By analyzing the SRI0 protocol and the switching chip control method, the flow of partial dynamic reconfiguration based on the management of data packets and events in this article is as follows:

3.1.1 Unplug/Reset

(1) Disable the event notification of the target device except the insert/remove event.
(2) Discard packets that are initiated by the target device or routed to the target device.
(3) The target device is prohibited from receiving new data packets.
(4) Reset/unplug the target device.
(5) Receiving the unplugging event confirms resetting/unplugging.

3.1.2 Prepare the port
(1) Clear all error conditions on the port.
(2) Continue to disable event notification on the corresponding port.
(3) Configure event management wait insertion events.

3.1.3 Device insertion/reset
(1) Establish a route to the target device.
(2) Disable event notification and isolation.
(3) Simultaneous reset of target device and CPS1848 port.

No matter whether it is a partial reconstruction or a complete reconstruction, the SRIO port device in
the system can be reconstructed through the above method as a core reconstruction method.

3.2 SRIO routing dynamic configuration
In the SRIO interconnection structure, communication between devices is data transmission between
devices realized by forwarding SRIO packets through a destination ID. In the dynamic and dynamic
reconstruction image processing measurement and control system with switching chip as the core, the
data transmission efficiency after system reconstruction is the key problem in the whole system working
process. Therefore, the routing configuration design becomes the key to data transmission within the
system.

The route configuration is mainly divided into static route configuration and dynamic route
configuration. The static route configuration fixes the IDs of all SRIO devices and uses a fixed routing
table to route these IDs with a fixed path. The dynamic routing configuration is to run a routing algorithm
through an SRIO host, communicate with the CPS1848 through maintenance packets, enumerate the
SRIO devices in all systems, and configure the entire system for routing. However, running the routing
algorithm is difficult and expensive, so this method is not suitable for this system.

In the following, by using a combination of mobile static routing and dynamic routing, the dynamic
configuration of SRIO is realized and the dynamic configuration using SRIO hosts is simplified,
improving the development efficiency.

(1) Default route static configuration:
Design and plan an interconnected routing solution for all SRIO devices in the entire system. The ID
numbers of all devices are fixed. The forwarding path of the data packets for all IDs in the switching
system is determined in advance, and the configuration file is generated and programmed into the
EEPROM memory of the I2C interface. After the system is powered on, the CPS1848 is configured in
I2C master mode, and the routing configuration and initialization of the entire system are completed by
reading the configuration file in the fixed-address I2C memory.

(2) Dynamic routing configuration:
When the system needs to be reconfigured, the SRIO host is not used to perform dynamic
configuration in the standard sense through the SRIO bus. Instead, the reconfiguration instruction is sent
to the ARM on the switch board through the network port of the upper layer software of the windows.
After receiving the instruction, ARM switches the CPS1848 to an I2C slave device and configures the
switching chip through the I2C bus for dynamic configuration. The sub-SRIO device also remains
unchanged during the entire dynamic configuration process.

3.3 Dynamic reconstruction time
The dynamic reconstruction time includes the time when the upper layer software of the windows issues
the reconfiguration instruction and the new SRIO routing table time, the time when all the SRIO devices
establish a new connection, and the time for the system to reply to the upper layer software of the
windows. The system tests the time through different port data bandwidths and baud rates.
Table 1. System reconstruction time in 4x/2x/1x mode

| Ingress and Egress Port Width | Ingress and Egress Baud Rate (Gbaud) | Minimum Latency(ns) | Maximum Latency(ns) |
|-------------------------------|-------------------------------------|---------------------|---------------------|
| 4x mode                       | 6.25                                | 106.0               | 114.2               |
|                               | 5.0                                 | 111.6               | 120.6               |
|                               | 3.125                               | 128.4               | 135.0               |
|                               | 2.5                                 | 139.6               | 152.6               |
|                               | 1.25                                | 195.6               | 216.6               |
|                               | 6.25                                | 109.2               | 117.4               |
|                               | 5.0                                 | 115.6               | 124.6               |
| 2x mode                       | 3.125                               | 134.8               | 141.4               |
|                               | 2.5                                 | 147.6               | 160.6               |
|                               | 1.25                                | 211.6               | 232.6               |
|                               | 6.25                                | 115.6               | 123.8               |
|                               | 5.0                                 | 123.6               | 132.6               |
| 1x mode                       | 3.125                               | 147.6               | 154.2               |
|                               | 2.5                                 | 163.6               | 176.6               |
|                               | 1.25                                | 243.6               | 264.6               |

According to the test data in Table 1, it can be found that even if the minimum port data bandwidth and baud rate are adopted in this system, the maximum reconstruction time is 264.6 ns. Meet the requirements of rapid reconstruction.

4. Summary
In order to realize the requirement of high-performance and dynamic image processing system, this paper proposes a design based on SRIO reconstruction and switching network architecture, and adopts SRIO high-speed data transmission within the architecture. Provides SRIO high-speed data transmission dynamic reconstruction network for image processing algorithms. Finally, high-performance dynamic reconfigurable architecture functions are achieved and the reconstruction process reaches nanoseconds. This solves the problem that traditional image processing systems of parallel processor arrays will face complex system structures, long development cycles, and inflexible hardware adjustments when they are applied.

5. References
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