High thermal stability ohmic contacts to nitride semiconductors with refractory metal sidewall diffusion barrier deposited by magnetron sputtering

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Abstract. GaN HEMTs are generally promising candidates for RF and switching power transistors due to their high breakdown strength and the high current density giving a low on-resistance. Low-resistance ohmic contacts are needed to reduce losses and self-heating. Conventional ohmic contacts use Ti and Al with a cap to avoid oxidation of the Al layer. Alternative ohmic metals for use with nitride semiconductors are being sought using Hf or Ta, which can be annealed at lower temperatures. That have been shown, the Au-free low temperature Ta/Al ohmic contacts fabricated with the refractory sidewall diffusion barrier have the lower contact resistance and the better surface morphology after the high temperature annealing. Normally-off p-gate high voltage GaN transistor based on Ta/Al ohmic contacts with the sidewall diffusion barrier have the higher drain-source current, lower gate-source current and higher source-drain breakdown voltage.

1. Introduction

GaN HEMTs have potential applications for devices operating at high temperature, frequency and power density [1]. To realize high performance in AlGaN/GaN HEMTs good ohmic contacts with low resistivity are critical. Low-resistance ohmic contacts are needed to reduce losses and self-heating. Conventional ohmic contacts in GaN HEMTs use Ti and Al, along with a cap to avoid oxidation of the Al layer [2]. The cap often consists of Ni or Mo with Au. But these structures require the high annealing temperature (>800°C) to achieve good ohmic properties, which can damage the performance of semiconductor heterostructure on which the HEMT action depends. These temperatures can also melt Al, creating unwanted surface roughness of the contact. Thus making it difficult to implement gate-first process, which is useful for the self-aligned process development. Alternative ohmic metals for use with nitride semiconductors are being sought using Mo, Hf or Ta, for example, which can be annealed at lower temperatures. In study [3] are presented a low thermal budget (<600°C) Hf/Al/Ta (15/200/20 nm) ohmic contact scheme on unintentionally doped In₀.₁₈Al₀.₈₂N/GaN grown on Si substrate, which has demonstrated low contact resistivity (0.59 Ohm·mm) and smooth surface morphology. In addition, the In₀.₁₈Al₀.₈₂N/GaN HEMTs fabricated with Hf/Al/Ta ohmic contacts have shown significantly improved breakdown voltage, compared to devices with traditional Ti/Al/Ni/Au ohmic contacts, own to the source-carrier-injection mechanism suppressed by the smooth metal-
semiconductor interface in the former. In work [4] the ohmic metal contact scheme based on Ta and Al only is presented. Overall, the minimum contact resistance found for Ta/Al/Ta (10/280/20 nm) based ohmic contacts were 0.4 Ohm mm after annealing at $T=550^\circ\text{C}$ during $t=60$ s. However both Hf- and Ta-based ohmic contacts have the some disadvantages. At the first, there are sold state phases of Al film observed after low temperature annealing at $T<660^\circ\text{C}$. At the second, Aluminum can oxidize at ohmic sidewalls and can react with wet chemicals. At the third, GaN HEMT use Au based interconnects. Once Au can diffuse to Al-based ohmic contacts at sidewalls to make high resistivity intermetallic compounds. Especially, purple plague (AuAl$_2$) has nearly twenty times larger resistivity [5]. It leads to the degradation of the device performance and bad reliability.

In this study we report the Au-free low temperature Ta/Al based ohmic contacts with the sidewall refractory diffusion barrier to improve ohmic performance and prevent Au sidewall diffusion into Al based ohmic from interconnects.

2. Experimental

AlGaN/GaN heterostructure layers grown on Si wafers by metal organic chemical vapor deposition (MOCVD) are used. The grown starts with AlN nucleation layer, followed by a 2200 nm Fe-doped GaN buffer layer, 300 nm GaN channel layer and 10 nm Al$_{0.25}$Ga$_{0.75}$N. Finally, 50 nm p-GaN layer is used as a capping layer. The room temperature mobility of 2DEG AlGaN/GaN was about 1500 cm$^2$∙V$^\text{-1}$∙s$^\text{-1}$. First, the mesa isolation was formed by BCl$_3$/Cl$_2$/Ar dry etching in ICP plasma. Second, Ni/Au (30/400 nm) was deposited as gate metal followed by the BCl$_3$/SF$_6$ selective plasma etching of p-GaN layer to define the self-aligned p-gate. Then SiN with a thickness of 100 nm was used as the passivation layer. After SiN via etching the Ta/Al/Ta (10/280/20 nm) films were deposited as source-drain metal. The Al film was deposited by e-beam evaporation in vacuum. But Ta films were deposited by e-beam evaporation (figure 1a) and in-situ magnetron sputtering (figure 1b) in the same vacuum chamber to form the sidewall thin film (refractory sidewall diffusion barrier).

![Figure 1. The cross sectional schematic images of Ta/Al/Ta ohmic contacts without (a) and with Ta sidewall diffusion barrier (b).](image-url)

After metal lift-off annealing of contacts was carried out in nitrogen environment for $t = 60$ s at various temperatures (from $T=500$ to 650°C). Transfer Line Method was used to evaluate the contact resistance. Ohmic contact pads morphology was observed by the optical and scanning electron microscopy (SEM). The DC parameters of the fabricated p-gate GaN transistors were measured by HP4156A Semiconductor Parameter Analyzer.
3. Results and discussion

Figure 2 shows the contact resistance of Ta/Al ohmic contacts without (curve 1) and with Ta sidewall diffusion barrier (curve 2) versus annealing temperature in nitrogen environment. That have been shown, the Ta/Al ohmic contacts fabricated with the sidewall diffusion barrier have the lower contact resistance (0.3 Ohm x mm) after annealing at $T=550^\circ$C. After annealing at higher temperatures ($T=650^\circ$C) Ta/Al ohmic contacts with the sidewall diffusion barrier (curve 2) demonstrate the lower contact resistance (0.52 Ohm·mm). Therefore introduce the Ta based sidewall barrier in low temperature Ta/Al based ohmic contacts let to improve the thermal stability of contact resistance.

![Figure 2](image)

**Figure 2.** The contact resistance of Ta/Al/Ta ohmic contacts w/o (curve 1) and w/i Ta sidewall diffusion barrier (curve 2) versus annealing temperature for $t=60$ s in nitrogen environment.

Figure 3 shows the SEM images of contact morphology of Ta/Al/Ta ohmic contacts without (curve 1) and with Ta sidewall diffusion barrier (curve 2) after annealing at $T=650^\circ$C for $t=60$ s in nitrogen environment. The Ta/Al ohmic contacts fabricated with the sidewall diffusion barrier have the better surface morphology after the high temperature annealing. It can be caused by prevent the Al film interactions during thermal annealing.

![Figure 3](image)

**Figure 3.** SEM images of contact morphology of Ta/Al/Ta ohmic contacts without (1) and with Ta sidewall diffusion barrier (2) after annealing at $T=650^\circ$C for $t=60$ s in nitrogen environment.
Figure 4 shows the benchmark the observed contact resistance values with prior arts of Au free ohmic contacts [4], [6-14].

![Graph showing contact resistance versus annealing temperature for different Au free ohmic contacts: comparison between our results and relevant published data.](image)

**Figure 4.** Contact resistance versus annealing temperature for different Au free ohmic contacts: comparison between our results and relevant published data.

In figure 4 we summarize the contacts resistance obtained using Au free ohmic contacts schemes, comparing this work’s results with relevant published data. It can be seen, that Ta/Al ohmic contacts fabricated with the sidewall diffusion barrier have the low contact resistance at the lowest annealing temperature ($T=550^\circ C$). The observed improvement may be caused by the fully prevent the Al film interactions with wet chemicals and air environment during resist lift off and thermal annealing.

Figures 5 and 6 present the cross section images of $p$-gate GaN HEMT fabricated with Ta sidewall diffusion barrier. The gate length is defined by the $p$-$\text{GaN}$ width is 1.0 $\mu$m, gate-source distance is 0.4 $\mu$m and distance between the source and drain is 5.5, 7.5, 9.5 and 11.5 $\mu$m.

![Cross section image of $p$-gate GaN HEMT](image)

**Figure 5.** The cross section image of $p$-gate GaN HEMT fabricated with Ta sidewall diffusion barrier.

![Cross section SEM image of $p$-gate](image)

**Figure 6.** The cross section SEM image of $p$-gate.

Figure 7 shows the dependence of drain-source current $I_{ds}$ from the gate-source voltage $V_{gs}$ of $p$-gate GaN transistors based on Ta/Al ohmic contacts. It can be seen that the fabricated $p$-GaN/AlGaN/GaN transistors demonstrate the normally-off operation with the threshold voltage is $V_{th}=+1.2$ V. The maximum drain current is $I_{ds}=0.4$ and 0.45 A/mm at $V_{gs}=8$ V for GaN HEMTs fabricated w/o and w/i Ta based sidewall diffusion barrier, accordingly. Therefore introduce Ta sidewall diffusion barrier lead to increase the maximum drain-source current of GaN transistor.
Figure 8 shows the dependence of gate-source current $I_{gs}$ from the gate-source voltage $V_{gs}$ of $p$-gate GaN transistors based on Ta/Al ohmic contacts. It can be seen that the $p$-GaN/AlGaN/GaN transistors with Ta based sidewall barrier has a lower gate-source current $I_{gs}$ at $V_{gs}=8$ V. Lower on-state gate current is preferred for reliability and for compatibility with gate drivers, that are often designed for insulated gate technologies and to lower the power consumption (i.e. high gate leakage is associated with a continuous power consumption and associated heating of the gate driver).

Figure 7. Dependence of the drain-source current $I_{ds}$ from the gate-source voltage $V_{gs}$ (1 – w/o sidewall barrier; 2 – w/i sidewall barrier).

Figure 8. Dependence of the gate-source current $I_{gs}$ from the gate-source voltage $V_{gs}$ (1 – w/o sidewall barrier; 2 – w/i sidewall barrier).

Figure 9 shows the dependence of the drain-source breakdown voltage from the drain-source distance of $p$-gate GaN transistor. Normally-off $p$-gate high voltage GaN transistor based on Ta/Al ohmic contacts without and with the sidewall diffusion barrier have the source-drain breakdown voltage $BV_{ds}=150$ and 240 V at $L_{ds}=5.5$ µm, accordingly. Further increase the source-drain distance lets to reduce this difference. And at the source-drain distances $L_{ds}=11.5$ µm the $BV_{ds}$ of both samples are similar. Use the refractory metal sidewall diffusion barrier into the low temperature Ta/Al based ohmic contacts can reduce of electric field intensity at the ohmic contacts edge. It lets to increase the source-drain breakdown voltage of $p$-gate GaN transistor.

Figure 9. Dependence of the drain-source breakdown voltage $BV_{ds}$ from the drain-source distance $L_{ds}$ (1 – w/o sidewall barrier; 2 – w/i sidewall barrier).

Figure 10. Dependence of specific on resistance $R_{on}$×$A$ from the drain-source distance $L_{ds}$ (1 – w/o sidewall barrier; 2 – w/i sidewall barrier).
Figure 10 shows the dependence of the specific on resistance $R_{on}\times A$ from the drain-source distance $L_{ds}$ of $p$-gate GaN transistors. Normally off $p$-gate high voltage GaN transistors based on Ta/Al ohmic contacts without and with the sidewall diffusion barrier have the similar specific on-resistance in the wide source-drain distance range. The specific on-resistance is 1.7 and 4.7 mOhm-cm$^2$ for source-drain distance of $L_{ds}=5.5$ and 11.5 µm, accordingly.

4. Conclusion
GaN HEMTs have potential applications for devices operating at high temperature, frequency and power density. To realize high performance in AlGaN/GaN HEMTs good ohmic contacts with low resistivity are critical.

In present work, it was shown that Au-free low temperature Ta/Al ohmic contacts fabricated with the sidewall diffusion barrier have the lower contact resistance and the better surface morphology after the high temperature annealing. Normally-off $p$-gate high voltage GaN transistor based on Ta/Al ohmic contacts with the sidewall diffusion barrier have the higher drain-source current, lower gate-source current and higher source-drain breakdown voltage. Therefore use the refractory metal sidewall diffusion barrier into the low temperature Ta/Al based ohmic contacts let to improve the electrical performance of high power GaN devices.

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