Complexity Analysis of Reversible Logic Synthesis

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Abstract. Reversible logic circuit is a necessary construction for achieving ultra low power dissipation as well as for prominent post-CMOS computing technologies such as Quantum computing. Consequently automatic synthesis of a Boolean function using elementary reversible logic gates has received significant research attention in recent times, creating the domain of reversible logic synthesis. In this paper, we study the complexity of reversible logic synthesis. The problem is separately studied for bounded-ancilla and ancilla-free optimal synthesis approaches. The computational complexity for both cases are linked to known/presumed hard problems. Finally, experiments are performed with a shortest-path based reversible logic synthesis approach and a (0-1) ILP-based formulation.

1 Introduction

Asymptotically zero power dissipation can be achieved by performing computation in a reversible manner, which implies [1] that logical reversibility must be supported to achieve physical reversibility. Consequently, major research attention is given towards the synthesis of a Boolean function using basic reversible logic gates, a problem otherwise known as reversible logic synthesis.

1.1 Background

An \(n\)-variable Boolean function \(f\) is a mapping \(f : GF(2^n) \rightarrow GF(2)\). An alternative representation of a Boolean function \(f\) is a mapping \(f : \{0, 1\}^n \rightarrow \{0, 1\}\), which is known as the truth table representation. Using any basis of \(GF(2^n)\), we can express each \(x \in GF(2^n)\) as an \(n\)-tuple \((x_1 x_2 \ldots x_n), x_i \in GF(2), i = 1, \ldots, n\). Thus we can derive the truth table representation from the former representation.

Alternatively, an \(n\)-variable Boolean function \(f(x_1, \ldots, x_n)\) can be considered to be a multivariate polynomial over \(GF(2)\). This polynomial can be expressed as a sum-of-products representation of all distinct \(k\)-th order \((0 \leq k \leq n)\) of the variables. This representation of \(f\) is called the Algebraic Normal Form (ANF) of \(f\).

An \(n\)-variable Boolean function is reversible if all its output patterns map uniquely to an input pattern and vice-versa. It can be expressed as an \(n\)-input, \(n\)-output bijection or alternatively, as a permutation function over the truth value set \([0, 1, \ldots, 2^n-1]\).

The problem of reversible logic synthesis is to map such a reversible Boolean function on a reversible logic gate library. Reversible gates are characterized by their implementation cost in Quantum technologies, which is dubbed as Quantum Cost (QC) [23]. Prominent classical reversible logic gates include NOT, Feynman (or CNOT), Toffoli (or CCNOT) gates. Controlled NOT gates can be generalized as \(T_{of_n}\) gate, where first \(n-1\) variables are used as control lines. There are other reversible logic gate families such as Fredkin gate family \((Fred_n)\), where first \(n-2\) variables are used as control lines and last 2 lines undergo swap, when the logical conjunction of first \(n-2\) variables is true.

- NOT gate:
\[
 f(A) = \overline{A} \tag{1}
\]

- Controlled NOT gate: Also known as Feynman or CNOT gate.
\[
 f(A) = A, f(B) = A \oplus B \tag{2}
\]

- Controlled Controlled NOT gate: Also known as Toffoli gate.
\[
 f(A) = A, f(B) = B, f(C) = A \cdot B \oplus C \tag{3}
\]

This gate can be generalized with \(T_{of_n}\) gate, where first \(n-1\) variables are used as control lines. NOT gate is denoted as \(T_{of_0}\) gate.
Swap gate:

\[ f(A) = A, f(B) = A \]  

(4)

This gate can be generalized to the Fredkin gate family \( (Fred_n) \), where first \( n-2 \) variables are used as control lines and last 2 lines undergo swap.

\[ f(A) = A, f(B) = \overline{A} \cdot B + A \cdot C, f(C) = \overline{A} \cdot C + A \cdot B \]  

(5)

Multiple sets of reversible gates form an universal gate library for realizing classical Boolean functions such as, (i) NCT: NOT, CNOT, Toffoli. (ii) NCTSF: NOT, CNOT, Toffoli, SWAP, Fredkin. (iii) GT: \( Tof_n \). (iv) GTGF: \( Tof_n \) and \( Fred_n \). Generally, gates with more control lines incur higher QC.

![Reversible Logic Gates](image)

Fig. 1. Reversible Logic Gates

Reversible logic synthesis begins from a given \( n \)-variable Boolean function, which can be irreversible. The first step is to convert it to a reversible Boolean function by adding additional constant input bits (known as ancilla inputs). If these constant input bits are not restored to their original values at the end of computation, then these are referred as ancilla.

2 Related Work and Motivation

Reversible logic synthesis methods can be grossly classified as following. First, optimal implementation is found by making a step-by-step exhaustive enumeration or by formulating the reversible logic synthesis as a SAT problem [4]. Optimal implementation up to 4-variable Boolean functions are known [5,6]. Pseudo-optimal synthesis for linear Boolean functions is proposed at [7]. Second, transformation-based methods [8,9], which apply controlled transformations to map output Boolean functions to input Boolean functions. Third category includes methods based on decision diagrams [10], each node of the decision diagram is converted to an equivalent reversible circuit structure. While these methods are known to scale for large Boolean functions, they introduce too many garbage bits. Finally, search-based methods start from an Exclusive Sum-of-Product (ESOP) representation of the Boolean function. The ideal candidates for reversible logic realization at each depth is chosen via heuristic search [11]. Another synthesis, based on ESOP formulation, is proposed in [12]. There a heuristic ESOP minimization tool [13] is used for generating reversible circuits with fixed number of ancilla lines. For a detailed survey of reversible logic synthesis, reader is kindly referred to [14,15].

Motivation: The promise held by Quantum computing is driving the research of reversible logic synthesis. Despite several major advancements of this research, the complexity study of the problem is not done so far. This is important since, optimal, comprehensive reversible circuit synthesis is done up to only all 4-variable Boolean functions [6] and up to selected 6-variable Boolean functions [4,16].
The rest of this paper is organized as following. In the following section 3, the performance objectives for reversible logic synthesis are discussed. In section 4, analysis of computational complexity for bounded-ancilla reversible logic synthesis is presented. This is followed by the computational complexity analysis for ancilla-free reversible logic synthesis in section 5. Two different formulations for exactly solving the reversible logic synthesis problem is presented in sections 6 and 7, respectively. Experimental results with these methods are reported in section 8. The paper is concluded and future works are outlined in section 9.

3 Performance Objectives

Before presenting the complexity analysis of reversible logic synthesis, it is necessary to develop a better understanding of the performance objectives. The major performance objectives of reversible logic synthesis are gate count, logical depth, Quantum cost, ancilla and garbage count.

Ancilla Count In literature, either ancilla count or garbage count or total line count is reported. Ancilla-free synthesis is achievable by several methods [8,4], whereas several synthesis methods compromise ancilla count for achieving scalability [10] or lowering QC [12].

Gate Count Gate count is used as a major performance objective in many synthesis flows [8,12] due to its simple cost annotation. However, several composite gates (e.g. Peres gates) are presented both as a single gate or multiple gates in literature. For example, Peres gates are considered as a single gate for multiple benchmark circuits presented in [2], whereas the gate counts reported for the Quantum arithmetic circuits in [17] count Peres gates as a collection of Toffoli and CNOT gates. To avoid confusion, library-specific gate counts are reported in [11].

Quantum Cost Quantum Cost (QC) for a reversible gate is technology-dependent. A set of primitive gates are actually implemented on experimental quantum circuits, which are used to build more complex gates and thus the QC is computed by simply adding those primitive gates. Early studies of primitive reversible gates are presented at [3], which is adopted for the derivation of QC for generalized Toffoli and Fredkin gates in [2]. Recent advances at experimental quantum computing [18] shows that the QC of negative-control gates are comparable to that of positive-control gates, thereby spawning several works on reversible logic synthesis with mixed-polarity gate libraries [19]. An improved circuit, in terms of less Quantum cost, for generalized Toffoli gates is presented in [20]. In a significant new result, improved QC for generalized Peres gates as well for generalized Toffoli gates are presented in [21]. Reduced QC values are reported by introducing a new gate library in [22].

Though there are established performance metrics for evaluating the quality of a reversible circuit, yet the continuously evolving Quantum technology needs to be considered for a fair benchmarking. The synthesis tools should also be adaptable to new performance objectives and their trade-offs.

4 Complexity Analysis of Bounded-Ancilla, Exact Reversible Logic Synthesis

The complexity of exact Sum-of-Product (SOP) minimization, in terms of number of literals, where the input is an incomplete or complete truth-table specification is studied in [23] and [24]. It is shown that the problem - Is there a SOP representation of a given Truth-table specification with at most k literals? - is NP-complete. The proof is based on the fact that the well-known exact procedure of SOP minimization, Quine-McCluskey includes a function call to the minimum cover problem. Minimum cover problem is shown to be NP-complete in 1972 [25]. We introduce few definitions, which are needed for rest of this section.

Definition 1. Given a set of elements $U = \{1, 2, \cdots, n\}$ and a set $S$ of $n$ sets, whose union equals $U$, the minimum set covering problem is to identify the smallest subset of $S$, the union of which contains all elements of $U$.

Definition 2. Exact cover or exact set cover problem is a decision problem, where the goal is to find a subset of $S$, the union of which contains all elements and each element of $U$ is covered exactly by one subset. Exact cover problem returns false if no such set exists.
For example, given a set $U = \{1, 2, 3, 4, 5\}$ and $S = \{\{1, 2\}, \{2, 3, 4, 5\}, \{3, 4\}, \{5\}\}$, returns the minimum set cover and $\{\{1, 2\}, \{3, 4\}, \{5\}\}$ returns an exact cover. The exact cover problem and the decision version of set covering problem are NP-complete [25].

The worst-case complexity of SOP formulation ($2^n - 1$) is more than the corresponding complexity of the ESOP formulation $3 \cdot 2^{n-3}$ [26], for an $n$-variable Boolean function. This led researchers to look for efficient ESOP minimization flows and several exact ESOP minimization algorithms have been presented [27, 28]. For the computational complexity of reversible logic synthesis, exact ESOP minimization holds a clue, since for an $n$-variable Boolean functions, an ESOP formulation with $k$ cubes directly corresponds to a reversible circuit realization with $k \cdot 2^n$ gates and at most $n$ ancilla lines, each corresponding to one output function. It might be argued that, the function of an ESOP is independent of the order of its product terms whereas, the function of a reversible circuit is affected by the order of the sequence of $2^n \cdot 2$ gates. However, that does not hold true for a bounded-ancilla reversible logic circuit, where the ancillae ensure that the inputs remain unchanged. The NOT gates inserted between the $T$ of $n$ gates can be ignored if mixed-polarity $T$ of $n$ gates are considered.

This is exemplarily shown in the reversible circuit realizations depicted in Fig. 2 for the Boolean functions $f(a, b, c) = a \oplus a \cdot b \oplus b \cdot c$ and $f(a, b, c) = a \oplus c \oplus a \cdot b$ respectively.

![Fig. 2. ESOP-based Reversible Circuit Realization](image)

Exact minimization of ESOP is well-studied in literature [29, 28]. In [29], exact ESOP minimization is done based on the shortest path enumeration of a decision diagram, which leads to the complexity of $O(2^{3n})$ for an $n$-variable Boolean function. Computational complexity analysis is not done there. Another exact ESOP minimization is proposed by Steinbach and Mishchenko [28]. There, the exact ESOP formulation is reduced to a problem of a so called coverage matrix. We adopt the exact minimization procedure from [28] for studying the computational complexity. In the following, we briefly describe the formulation.

First, the SOP or truth table formulation is converted to an ESOP formulation. For a SOP to ESOP formulation, the following transformation can be used.

$$a + b = a \oplus b \oplus a \cdot b$$

(6)

It is straightforward to show that for a SOP formulation with $k + 1$ cubes, an ESOP formulation with $2^{k+1} - 1$ literals is obtained. Alternatively, constructing an ANF from a Boolean truth table specification can be done using $O(n 2^n)$ operations with standard algorithm.

The input to the algorithm is the truth table $f = [f(0) f(1) f(2) \ldots f(2^n - 1)]$, and the output is the coefficient vector of the canonical Algebraic Normal Form (ANF), represented as $C = [c_0 c_1 c_2 \ldots c_{2^n - 1}]$. Only if $c_j = 1$, where $0 \leq j \leq 2^n - 1$, then the monomial $x_0^{j_0} x_1^{j_1} \cdots x_{n-1}^{j_{n-1}}$ exists in the ANF of $f$, where $(j_0, j_1, \ldots, j_{n-1})$ is the
binary representation of index \( j \). For an \( n \)-variable Boolean function, \( C = fA_n \), where \( A_n \) can be computed as following. \( A_n = \begin{bmatrix} A_{n-1} & A_{n-1} \\ 0 & A_{n-1} \end{bmatrix} \), where \( A_0 = 1 \).

First, the SOP or truth table formulation is converted to an ESOP formulation. Based on the ESOP formulation, a Special Normal Form (SNF) is introduced in [28]. It was shown that it is also a canonical ESOP representation like ANF. Whereas ANF is a positive-polarity expression, SNF is mixed-polarity. For exact ESOP minimization, a coverage matrix is constructed, where the rows and columns correspond to all possible \( \left( 2^n \right) \) cubes of an \( n \)-variable Boolean function \( f \) and the cubes of SNF(\( f \)) respectively. The goal of exact ESOP minimization is to include the fewest row-cubes from \( f \) to cover all the column-cubes from SNF(\( f \)), which reduces to a variation of the minimum set covering problem. However, there is a subtle difference between the minimum set covering problems encountered in ESOP and SOP minimization. For the SOP formulation, the goal is to cover the ON-set of output function with minimum number of cubes, where multiple cubes can cover a ON-value as in inclusive OR.

For ESOP formulation, an ON-value can be covered by odd number of cubes and an OFF-value can be covered by even number of cubes as in exclusive OR. This is exemplarily shown in the Karnaugh-map diagrams in Fig. 3. The dotted lines shows the exact cover without multiple covering of an element. The solid lines shows the covers with multiple covering. Note that while multiple cover of the OFF-set in the left-hand figure decreases the number of cubes, whereas multiple covers of the ON-set elements leaves the number of cubes intact but, increases the sizes of the cubes, thus reducing literals. Based on this, we propose the following formulation of ESOP minimization.

\[ Z = X \cup Y, \text{ where} \]
\[ e \in Z \text{ if } e \in X \land e \notin Y \]
\[ e \in Z \text{ if } e \in Y \land e \notin X \]

We refer to the problem as XOR-SET-COVER. Formally, the XOR-SET-COVER problem is:

**INPUT:** \( \langle U, A, K \rangle \) where \( A \) is a set of subsets, consisting of members from \( U \) and \( K \in \mathbb{N} \)

**QUESTION:** Does \( U \) have a \( A \)-cover of size \( K \), where the union of two sets is defined as above?

**Claim.** XOR-SET-COVER is in NP.

**Proof.** Let us say, \( B \) is a proposed \( A \)-cover solution. We propose the following verification flow.

- \( |B| \leq K \)
- \( \forall u \in U \exists B \in B \mid u \in B \land \text{count}(u) \text{ is odd} \)

The verifier runs in time polynomial in the length of the \( B \).
Theorem 1. XOR-SET-COVER problem is NP-Complete.

Proof. Suppose we have a black box $M_{XS}$ which takes a three tuple $⟨U, A, K⟩$ as input and returns 1 iff $U$ has a XOR SET A COVER of size $K$ otherwise it returns 0. Here, $U, A, K$ is same as defined previously. Now using $M_{XS}$ as a subroutine we have to solve the EXACT SET COVER problem. So, the input for EXACT SET COVER problem is also a three tuple $⟨U, A, K⟩$ and we have to answer whether $U$ has a set $A$-cover of size $K$. If for any input $⟨U, A, K⟩$, the $M_{XS}$ gives 1 as output, then we can conclude that $⟨U, A, K⟩$ is an exact set cover. Now the problem is when $M_{XS}$ gives 0 as output. Then there are two following possibilities.

1. $U$ has exact $A$-set cover of size $K$, let $S_K ⊆ A$ be a solution i.e, union of the elements of $S_K$ gives the set $U$. As $M_{XS}$ is giving the output 0, so, we can say that if we perform the XOR operation defined previously among the elements of $S_K$, then there exists at least one element $u ∈ U$ which is present in even number of elements of $S_K$.

2. $U$ doesn’t have exact $A$-cover of size $K$.

Among the above two possibilities, for the first possibility, we can take an element $u ∈ U$ and remove it from one element of $A$, say $A'_u$ be the new set of subsets and check whether $U$ has xor set $A'_u$-cover of size $K$. Then, we can repeat this process for each element of $A$ for a fixed $u$ and then repeat this process for each element $u ∈ U$. If for every input $M_{XS}$ gives 0 as output then conclude that $U$ doesn’t have exact $A$-set cover of size $K$ otherwise, if for at least one single query to $M_{XS}$ it give the output 1 conclude that $U$ has exact $A$-set cover of size $K$. So, here we have reduced the EXACT SET COVER problem to XOR-SET-COVER problem. As, EXACT SET COVER is known NP-complete problem and XOR-SET-COVER is in NP, so XOR-SET-COVER problem is NP-complete.

It is important to show how the XOR-SET-COVER is applicable to the problem at hand. We start by enumerating all possible cubes w.r.t. $n$ input variables of the Boolean function $f$. We arrange a coverage matrix, where all possible cubes ($3^n$) are arranged row-wise and the cubes from the canonical SNF or ANF are arranged column-wise. Let us assume that we have $I$ and $J$ elements in the ON-set and in the OFF-set respectively. Further, the cubes belonging to the OFF-set are also added to the columns. Hence, we get a $3^n \times 3^n$ coverage matrix. The elements of the matrix are assigned a value of 0 if a row-cube does not cover a column-cube. Otherwise, the element value is assigned to be 1 if the column-cube belongs to the ON-set and a value of −1 if it belongs to the off-set. An exemplary coverage matrix is shown in Table 1 where the ON-set column headers are marked bold.

A valid solution for the coverage matrix is a XOR-SET-COVER, where the columns belonging to ON-set can be replicated odd number of times and the columns belonging to the OFF-set can be replicated even number of times. Note that, there is a upper limit of replication [28]. The ON-set cubes can be replicated up to $2^n − 1$ times and OFF-set cubes can be replicated up to $2^n$ times.

Table 1. Exemplary 2-variable Coverage Matrix [28]

|   | 00 | 01 | 10 | 11 |
|---|----|----|----|----|
| - | -1 | 01 | 11 | 11 |
| - | 01 | 00 | 00 | 00 |
| -1| 00 | 01 | 01 | 01 |
| 0 | 01 | 01 | 00 | 00 |
| 0 | 00 | 01 | 01 | 00 |
| 0 | 00 | 00 | 01 | 01 |
| 0 | 00 | 00 | 00 | 01 |
| 0 | 01 | 00 | 00 | 01 |
| 0 | 01 | 01 | 00 | 01 |
| 1 | 01 | 00 | 01 | 01 |
| 1 | 01 | 01 | 00 | 01 |
| 1 | 00 | 00 | 01 | 01 |
| 1 | 00 | 01 | 00 | 01 |

Fig. 4 shows an example for 4 or 6 variable Boolean function, where the element 1 is covered 3 times resulting in a reduced cube count.

Lemma 1. To decide if bounded-ancilla reversible logic synthesis is achievable with a specified gate count is NP-complete.

Proof. This follows the previous theorem directly.
Lemma 2. To decide if bounded-ancilla reversible logic synthesis is achievable with a specified Quantum Cost is $NP$-complete.

**Proof.** The decision version of bounded-ancilla reversible logic synthesis with an user-specific QC is an instance of the decision version of ESOP minimization, where the element values ($1$, $-1$ and $0$) are replaced with the number of literals ($l$, $-l$ and $0$) in the particular row-cube. The number of literals directly indicate the $ToF_n$ to be employed and hence, reflect the QC of the circuit. The decision version of ESOP minimization i.e. XOR-SET-COVER is shown to be $NP$-complete. Hence, the proof.

5 Complexity Analysis of Ancilla-free, Exact Reversible Logic Synthesis

Exact synthesis for a reversible Boolean specification is so far proposed by modeling the synthesis as a satisfiability (SAT) problem [4] as well as modeling the problem in terms of symbolic reachability analysis [30]. However, none of these works attempt the complexity analysis of reversible logic synthesis.

We can easily show that the ancilla-free reversible logic synthesis is in the class of NP.

**Claim.** The decision problem of whether an ancilla-free reversible circuit with $K$ gates exist, for a given permutation $\pi$ is verifiable in polynomial time. Hence, the problem is in NP.

**Proof.** Let us say, $C$ is a proposed $K$-gate circuit. We propose the following verification flow.

- $C$ results in a permutation $\sigma$
- $\sigma^{-1} \cdot \pi = I$

The verifier runs in time polynomial in the cardinality of $\pi$.

In order to explore the complexity of ancilla-free reversible logic synthesis, we connect the reversible logic synthesis problem to sorting. A reversible Boolean function can be defined as an ordered set of integers corresponding to a permutation $\pi$ of its domain. The reversible circuit, when traversed from output towards input, essentially converts the permutation $\pi$ to an Identity $I$. We explain this with an example.

**Definition 3.** Let $S$ be an arbitrary nonempty set. A bijection of $S$ onto itself is called a permutation of $S$.

Following Cauchy’s two-line notation where all the mapping $x : S \to S$ can be written as

\[
\begin{pmatrix}
\alpha_1 \alpha_2 \alpha_3 \ldots \alpha_n \\
\beta_1 \beta_2 \beta_3 \ldots \beta_n
\end{pmatrix}
\]  

(7)

where the top row is some enumeration of the points of $S$ and $\beta_i$ is the image of $\alpha_i$ under $x$ for each $i$. This can be alternatively formalized as a functional digraph.
Definition 4. Given a function $f : [0, n] \rightarrow [0, n]$, the functional digraph $G(f) = (V, E)$ associated with $f$ is a directed graph with $V = \{0, ..., n\}$ and $E = \{(v, f(v)) : \text{for each } v \in V\}$

The functional digraph of the reversible function $\{7, 1, 4, 3, 0, 2, 6, 5\}$ is given in figure 5.

![Functional digraph](image)

Fig. 5. Functional digraph

For a permutation $\pi$ of $0, 1, \cdots, n$, $G$ is a collection of disjoint cycles, since the in-degree and out-degree of each vertex is exactly one. Each cycle can be written as a $k$-tuple $c = (a_1, a_2, \cdots, a_k)$, where $k$ is the length of the cycle and $a_{i+1} = c(a_i)$.

In other words, the permutation cyclically shifts all entries in $\{a_1, a_2, \cdots, a_k\}$ and keeps all other elements fixed.

$$a_1 \rightarrow a_2 \rightarrow a_3 \rightarrow \cdots a_k \rightarrow a_1$$

Transposition is defined as a cycle of length 2, when it is applied on two adjacent blocks. Otherwise, it is defined as block interchange. Given a permutation $\pi$, a block interchange with parameters $\{i, j, k, l\}$, where $1 \leq i < j \leq k < l \leq n + 1$, is applied to $\pi$ by exchanging the blocks $[\pi_i, \cdots, \pi_j]$ and $[\pi_k, \cdots, \pi_l]$. A special case of this is transposition, where $j = k$. A sorting $s$ of a permutation $\pi$ is a sequence of transpositions that transform $\pi$ into $I$, where $I$ denotes the identity element of $S_n$, i.e., $s \cdot \pi = I$. The length of the sequence of transpositions to perform sorting is known as transposition distance, whereas the length of the sequence of block interchanges is called minimum block interchange distance.

The fact that a permutation can be decomposed into transpositions was first applied into genome sequence comparison [31], where the transposition distance ($d_t(\pi)$), i.e., number of transpositions needed to reach from one permutation to $I$ is studied. The problem of sorting by transposition is defined as following - given a permutation $\pi$ and an integer $k$, is $d_t(\pi) \leq k$? We briefly state two results connecting reversible logic gates and sorting.

Lemma 3. When the reversible Boolean function is represented as a permutation $\pi$, the application of a $Tof_n$ gate is equivalent to a block interchange.

Proof. Any uni-polarity/multi-polarity $Tof_n$ gate introduces change in exactly one bit position, which is nothing but exchange of two elements in $S$. This is equivalent to a 2-cycle, though not necessarily for the adjacent elements. Hence, a $Tof_n$ gate introduces a block interchange.

Lemma 4. A block interchange defined by the parameters $\{i, j, k, l\}$, where $j = i + 1, j < k, l = k + 1$ incurs a definite non-negative cost in terms of $Tof_n$ gate count.

Proof. The block interchange swaps two elements $\pi_i$ and $\pi_k$. Let the number of bits required to represent an element of the permutation be $n$. A multi-polarity $Tof_n$ gate will be active to a permutation element iff all positive and negative control lines evaluate to one and zero correspondingly. In that case, the target bit is inverted. Hence a $Tof_n$ gate can perform a block interchange of two permutation elements with a Hamming distance of 1. Let the Hamming distance between $\pi_i$ and $\pi_k$ be $H(\pi_i, \pi_k) = h_{i,k}$. To achieve the swap, we first transform $\pi_i$ to $\pi_k$ by applying a series of $Tof_n$ gates. We identify the bits of $\pi_i$ that differ from corresponding bits of $\pi_k$. For each bit, we apply a $Tof_n$ gate whose target line maps to that bit and the control lines corresponds to other bits of $\pi_i$. After each step, the Hamming distance will decrease by 1. After $h_{i,k}$-th step, the combined circuit will transform $\pi_i$ to $\pi_k$. The $h_{i,k}$-th $Tof_n$ gate will also invert a bit of $\pi_k$ as the Hamming distance between $\pi_k$ and intermediate
output of $\pi_i$. If we apply these series of $Tof_n$ gates in reverse order it will transform $\pi_k$ to $\pi_i$. As there is one common gate, total number of gates needed are $2h_{i,k} - 1$.

As we are applying each $Tof_n$ gate twice, once in direct and once in reverse order, this will cancel out the introduced changes in the permutation elements other than $\pi_i$ and $\pi_k$.

Since the introduction of sorting by transpositions by Bafna and Pevzner [31], it has been studied with the context of varying applications, e.g., genome sequencing and rank permutation coding. The special case of sorting by block interchange is shown to be solvable in polynomial time [32]. However, this is not applicable to reversible logic synthesis since, even though each $Tof_n$ gate introduces a block interchange, the block interchange required by the polynomial-time algorithm may not be realizable with a single $Tof_n$ gate. Furthermore, the algorithm in [32] does not include the cost of a block interchange. For reversible logic synthesis, the cost for different block interchanges could be different.

The problem of sorting by transposition is shown to be NP-hard [33]. This is, again, not directly applicable to the case at hand since, sorting by transposition attempts to find minimum transposition distance as well as imposes a restriction that the sorting needs to be achieved by transpositions only. Whereas, for the reversible logic synthesis, the output Boolean function, could be sorted by a series of block interchanges. With this context, we define the following problem, which is mappable to reversible logic synthesis directly.

Ancilla-free reversible logic synthesis is sorting by minimum-cost block interchange problem, where the cost of exchanging two single-element blocks and the block cardinality are as following.

$B_i = \{\pi_i\}, B_j = \{\pi_j\}$,
\[
\text{Cost}(B_i, B_j) = 2h_{i,j} - 1, \quad \text{and} \quad |B| = 1
\]

A related problem of sorting by cost-constrained transpositions [34] is studied recently, for which the complexity is yet to be established.

6 Shortest Path Problem Formulation

The most prominent heuristics for ancilla-free reversible logic synthesis adopt a branch-and-bound heuristic [11] or apply repeated transformations [8,9]. The former approach is built on top of an ESOP synthesis, hence reduces to the previously identified complexity. The latter approaches do not link their result to optimality and hence we refrain from the corresponding complexity analysis. In the following, we present reversible logic synthesis as a shortest path problem. This has been briefly explored in [35] without the complexity analysis.

It is shown in [4] that for an $n$-variable Boolean function, there exist $n \cdot 2^{n-1}$ Toffoli gates. Along similar lines, the total number of Fredkin gates can be shown to be $\binom{n}{2} \cdot 2^{n-2}$. The following analysis is done for Toffoli gates, with further extensions to Fredkin or other reversible gate families being trivial.

For the ancilla-free reversible logic synthesis, we construct a graph $G = \mathcal{V}, \mathcal{E}$, where $\mathcal{V}$ is the set of vertices representing an $n$-variable Boolean function as a permutation function over the truth value set $\{0, 1, \ldots 2^{n-1}\}$. An edge from the set of edges ($\mathcal{V}$) represent the application of a $Tof_n$ gate. Since the gates are reversible, the edges are not directed. Note that, the set of all permutation functions $S(P)$ holds closure under the application of $Tof_n$ gate. This implies that the $G$ contains cycles. An algorithm for constructing $G$ is provided as a pseudo-code in the following algorithms [1] and [2].

**Algorithm 1: Create_Graph**

```plaintext
input : $S(P)$
output : $G(\mathcal{V}, \mathcal{E})$
while $S(P) \neq \emptyset$ do
    $v_{curr} = \text{Create_Vertex}(p \in S(P));$
    \text{ConnectChild}($v_{curr}$);
return $G(\mathcal{V}, \mathcal{E})$
```

The function Create_Graph iterates over all possible permutations $S(P)$. For each permutation $p$, a vertex is created. For that vertex, all possible $Tof_n$ gate is applied. The resulting new permutation is stored in a vertex
Algorithm 2: \texttt{Connect} \texttt{Child}

\begin{algorithmic}
\State \textbf{input} : $v_{\text{curr}}$
\State $S(P) \rightarrow \text{remove}(\text{perm}(v_{\text{curr}}))$
\State $G \rightarrow \text{append}(v_{\text{curr}})$
\State \textbf{foreach} gate $\in T_{\text{Tof}}$, do $v_{\text{res}} = T_{\text{Tof}}(v_{\text{curr}})$;
\State $\text{Connect}(v_{\text{res}}, v_{\text{curr}})$;
\If{$(v_{\text{res}} \notin G)$}
\State $S(P) \rightarrow \text{remove}(v_{\text{res}})$;
\State $\text{Connect} \text{Child}(v_{\text{res}})$;
\EndIf
\end{algorithmic}

$(v_{\text{res}})$ and connected via an edge to the current vertex. If $v_{\text{res}}$ is not already included in $G$, then the function \texttt{Connect} \texttt{Child} is called recursively.

The total number of nodes in $G(V, E)$ is same as the total number of permutation functions for an $n$-variable Boolean function, which is $2^n!$. From the aforementioned constructed graph, determining the optimal reversible circuit for a given permutation $p_r$ function is nothing but the determination of shortest path from the permutation $p_r$ to the input permutation $p_i$. The edges can be assigned with a weight of 1 or the weight of QC corresponding to the transformation for determining the reversible circuit with minimum gate count or minimum QC respectively. The complexity of single-source shortest path computation with edges having non-negative weight is $O(E + V \log V)$, where $E$ is the edge count and $V$ is the vertex count \[36\]. Clearly, the complexity in our case is exponential.

Combining previous results, the complexity of optimal ancilla-free reversible logic synthesis for Toffoli network is $O((2^n! \cdot n \cdot 2^{n-1} + (2^n!\log(2^n!)))$.

Figure 6 shows parts of a $G(V, E)$ for a 2-variable Boolean function. The nodes represent the permutation functions and the edges represent the application of different reversible gates. For determining the optimal gate count, the edge weight can be disregarded (every edge weight is 1) and a simple breadth-first search with complexity $O(E)$ can be performed, where $E = (2^n! \cdot n \cdot 2^{n-1}$. For determining minimum QC, however, the algorithm from \[36\] needs to be applied, which is of higher complexity.

![Fig. 6. Reversible Logic Synthesis via Shortest Path](image)

7 (0-1)-ILP Formulation

In this section we present another formulation of ancilla-free reversible logic synthesis as an optimization problem using ILP. An Integer Linear Program (ILP) takes the following form

\[
\begin{align*}
\text{minimize} & \quad c^T x \\
\text{subject to} & \quad Ax \geq b
\end{align*}
\]
where $A$ is an integer $m \times n$ matrix, $c$ is an integer $n$-vector, $b$ is an integer $m$-vector. The values of $x$, an integer $n$-vector to be determined. When the solution set is restricted to either 0 or 1, then it becomes a (0-1) ILP, which is known to be NP-complete [25]. The (0-1) ILP formulation for reversible logic synthesis has several interconnected modules for expressing the constraints, which are explained in the following.

**Initialization Module**: Corresponding to $n$ variables, $n$ target binary vectors of $2^n$ length are derived. Each target vector ($t_v$) is assigned a truth-table expansion corresponding to an input variable.

**Target Selection Module**: All the target binary vectors are interchanged to derive new set of target binary vectors. This permutation network is ensured to preserve the exclusivity of the targets. The last line is selected as the target for the following operation. In case of Fredn gate, the last two lines are selected as the target.

**Tof Module**: All but the last target lines are operated on with a conditional AND, where the condition is specified in a vector $c_{tof}$. Based on the result of the AND operation, new target binary vectors are derived. Control lines are transported unchanged to new target binary vectors as well. Note that, if the control condition is 0, the AND contributor for that particular control line should be 1 in order not to disturb the final control value. This reduces to the following specification for a control contribution, where $d$ indicates the current depth.

$$
\bigwedge_{i=1}^{n-1} (t_v[d][i] == 1) \lor (c_{tof}[d][i] == 0)
$$

(9)

This can be interpreted by the optimizer as a NOT gate, when the $c_{tof}$ contains 0 in each element. To keep the gate count for such assignment and drive the optimizer, an additional element $c_{en}$ is introduced as following.

$$
c_{en}[d] \land \bigwedge_{i=1}^{n-1} (t_v[d][i] == 1) \lor (c_{tof}[d][i] == 0)
$$

(10)

The operational modules are connected via a target selection module. This allows for a compact formulation. The modules are repeated $D$ times, which is maximum possible depth for a given variable count, before assigning the target to the output Boolean specification to be synthesized.

**Fredn Module**: Similar formulation applies to Fredn gates as well, where the control values are taken from all but last two target vectors. The condition vectors are maintained using $c_{fred}$, which is enabled with an element $c_{en}$ for the particular depth.

The optimization goal can be specified as minimization of gate counts or QC, both of which are based on the condition vector $c_{tof}$. For QC minimization, the $c_{tof}$ condition vector is added to identify the number of control lines and corresponding QC value is applied. For gate count minimization, the condition vector is checked to contain a single truth-value or not. Correspondingly, a gate is inferred.

## 8 Experimental Results

Both the shortest path approach and ILP formulation explained are implemented as standalone C++ program. For the ILP formulation, the API calls for the commercial ILP solver IBM CPLEX version 12.2 [37] are utilized. For both the techniques, experiments are done using Intel(R) Core(TM) i7-2670QM CPU @ 2.20GHz machine with 4 GB RAM, running Red Hat Linux version 2.6.32-358.6.2.el6.x86_64.

### Table 2. Execution Time for Selected Benchmarks

| Function | Variable Count | Gate Count | Execution Time (seconds) |
|----------|----------------|------------|--------------------------|
| Peres    | 3              | 2          | < 0.01                   | 2.16                     |
| Fredkin  | 3              | 3          | < 0.01                   | 7.19                     |
| Miller   | 3              | 5          | < 0.01                   | 1536.68                  |

For benchmarking the efficiency of the ILP solver against state-of-the-art exact approaches, we compare the execution times with those reported in [16]. In [16], a Satisfiability Modulo Theory (SMT)-based solver with function-specific optimizations have been used. The results are presented in table 2. Clearly, (0-1) ILP does not provide a practical solution to reversible logic synthesis, despite its capability to explore the optimization space
rather than determining a satisfiable solution as in SAT. Even for the most basic examples, the runtime quickly increased. To control the runtime, the solution space is restricted in CPLEX by setting `IntSolLim` to 1. Even then, it produced the result with gap of several orders of magnitude execution time, when compared to SAT.

In contrast, the shortest path problem formulation led to comprehensive results for complete 3-variable Boolean functions. The flexibility of our solution allowed including different gates (N - NOT, C - CNOT, T - Toffoli, F - Fredkin, P - Peres) and also consider positive control and inverted control lines, indicated by ‘+’ and ‘-’ in Table 3. Table 4 reports corresponding QC values. It can be observed that Fredkin gate is decomposed into Toffoli gates and therefore, the QC values are same for NCT and NCTF family, while reporting optimized QC. For each of these gate families, optimal gate count and optimal QC values are obtained within a minute for the entire set of 3-variable functions. Note that, this study only presents the optimal gate/Quantum cost for classical gates. The detailed QC values with non-classical gates, as reported in [38], is avoided because of space limitations.

| GC | NCT | NCF | NCTF | NCTPF |
|----|-----|-----|------|-------|
| 0  | 1   | 1   | 1    | 1     |
| 1  | 12  | 27  | 21   | 15    |
| 2  | 102 | 369 | 101  | 280   |
| 3  | 625 | 2953| 676  | 2422  |
| 4  | 2785| 13822| 3411| 11229 |
| 5  | 9291| 20480| 11378| 18689 |
| 6  | 17049| 3236| 17970| 7558  |

Table 3. Optimal Gate Count results for 3-variable circuits

| QC | NCT | NCF | NCTF | NCTPF |
|----|-----|-----|------|-------|
| 0  | 1   | 1   | 1    | 1     |
| 1  | 9   | 15  | 9    | 15    |
| 2  | 51  | 117 | 51   | 117   |
| 3  | 187 | 433 | 187  | 433   |
| 4  | 393 | 534 | 393  | 534   |
| 5  | 477 | 240 | 477  | 0     |
| 6  | 260 | 196 | 260  | 196   |
| 7  | 338 | 1320| 338  | 1320  |
| 8  | 577 | 0   | 577  | 0     |

Table 4. Optimal QC results for 3-variable circuits

The shortest path formulation for reversible logic synthesis provides the computational viewpoint of what has been a purely memory-oriented approach in [5] and [6]. The sheer number of nodes for 4-variable and beyond presents a bottleneck for scaling the shortest path approach. On the other hand, this may provide opportunities for utilizing graph theoretic results such as approximate shortest paths.
9 Conclusion and Future Work

In this paper, we studied the complexity of exact reversible logic synthesis, for both the cases of the circuit being bounded-ancilla and ancilla-free. For the bounded-ancilla scenario, the problem is shown to be NP-hard. For ancilla-free reversible logic synthesis, we linked the problem to sorting by cost-constrained transpositions, for which the computational complexity is not known.

We attempted two different formulations for solving the exact problem namely, (0-1) ILP and shortest path problem. The former approach fails to produce optimal solutions in acceptable time. The shortest path problem formulation is used to generate comprehensive results for 3-variable functions, while scaling it up to larger variable sizes remain an interesting future work.

References
1. C. H. Bennett, “Logical reversibility of computation,” IBM J. Res. Dev., vol. 17, pp. 525–532, Nov. 1973.
2. Reversible Benchmarks, http://webhome.cs.uvic.ca/~dmaslov
3. A. Barenco et al., “Elementary gates for quantum computation,” Phys. Rev. A, vol. 52, pp. 3457–3467, Nov 1995.
4. D. Grosse, R. Wille, G. Dueck, and R. Drechsler, “Exact multiple-control toffoli network synthesis with sat techniques,” IEEE TCAD, vol. 28, no. 5, pp. 703–715, 2009.
5. V. Shende, A. Prasad, I. Markov, and J. Hayes, “Reversible logic circuit synthesis,” in ICCAD, pp. 353–360, 2002.
6. O. Golubitsky, S. M. Falconer, and D. Maslov, “Synthesis of the optimal 4-bit reversible circuits,” in DAC, DAC ’10, pp. 653–656, 2010.
7. K. N. Patel, I. L. Markov, and J. P. Hayes, “Optimal synthesis of linear reversible circuits,” Quantum Info. Comput., vol. 8, pp. 282–294, Mar. 2008.
8. D. Miller, D. Maslov, and G. Dueck, “A transformation based algorithm for reversible logic synthesis,” in DAC, pp. 318–323, 2003.
9. C. Chandak et al., “Analysis and improvement of transformation-based reversible logic synthesis,” in ISMVL, pp. 47–52, 2013.
10. R. Wille and R. Drechsler, “BDD-based Synthesis of Reversible Logic for Large Functions,” in DAC, DAC ’09, pp. 270–275, 2009.
11. P. Gupta, A. Agrawal, and N. Jha, “An algorithm for synthesis of reversible logic circuits,” IEEE TCAD, vol. 25, no. 11, pp. 2317–2330, 2006.
12. N. M. Nayeem and J. E. Rice, “Improved esop-based synthesis of reversible logic,” in Proc. Reed-Muller Workshop, 2011.
13. A. Mishchenko and M. Perkowski, “Fast heuristic minimization of exclusive-sums-of-products,” in Proc. Reed-Muller Workshop, pp. 242–250, 2001.
14. R. Wille and R. Drechsler, Towards a Design Flow for Reversible Logic. Springer, 2010.
15. M. Saeedi and I. L. Markov, “Synthesis and optimization of reversible circuits - a survey,” ACM Comput. Surv., vol. 45, pp. 21:1–21:34, Mar. 2013.
16. R. Wille and D. Grosse, “Fast exact toffoli network synthesis of reversible logic,” in ICCAD, ICCAD ’07, pp. 60–64, 2007.
17. Y. Takahashi, S. Tani, and N. Kunihiro, “Quantum addition circuits and unbounded fan-out,” Quantum Info. Comput., vol. 10, pp. 872–890, Sept. 2010.
18. A. G. Fowler, A. M. Stephens, and P. Groszkowski, “High-threshold universal quantum computation on the surface code,” Phys. Rev. A, vol. 80, p. 052312, Nov 2009.
19. M. Szywopowski and P. Kerntopf, “A study of optimal 4-bit reversible circuit synthesis from mixed-polarity toffoli gates,” in Nanotechnology (IEEE-NANO), IEEE Conference on, pp. 1–6, 2012.
20. D. Maslov and G. Dueck, “Improved quantum cost for n-bit toffoli gates,” Electronics Letters, vol. 39, no. 25, pp. 1790–1791, 2003.
21. M. Szywopowski and P. Kerntopf, “Low quantum cost realization of generalized peres and toffoli gates with multiple-control signals,” in Nanotechnology (IEEE-NANO), IEEE Conference on, 2013.
22. Z. Sasanian, R. Wille, and D. M. Miller, “Realizing reversible circuits using a new class of quantum gates,” in DAC, DAC ’12, pp. 36–41, 2012.
23. W. J. Masek, “Some NP-complete set covering problems,” tech. rep., MS Thesis, MIT Lab. Computer Science, MIT, Cambridge, 1978.
24. C. Umans, T. Villa, and A. Sangiovanni-Vincentelli, “Complexity of two-level logic minimization,” IEEE TCAD, vol. 25, no. 7, pp. 1230–1246, 2006.
25. R. M. Karp, “Reducibility among combinatorial problems,” in Complexity of Computer Computations (R. E. Miller and J. W. Thatcher, eds.), pp. 85–103, New York: Plenum, 1972.
28. B. Steinbach and A. Mishchenko, “SNF: a Special Normal Form for ESOPs,” in Proc. Reed-Muller Workshop, pp. 66–81, 2001.
29. T. Sasao, “An exact minimization of and-exor expressions using reduced covering functions,” in In Proceedings of the Synthesis and Simulation Meeting and International Interchange, pp. 374–383, 1993.
30. W. N. N. Hung, X. Song, G. Yang, J. Yang, and M. Perkowski, “Quantum logic synthesis by symbolic reachability analysis,” in Proceedings of the 41st Annual Design Automation Conference, DAC ’04, pp. 838–841, 2004.
31. V. Bafna and P. A. Pevzner, “Sorting by transpositions,” SIAM J. Discret. Math., vol. 11, pp. 224–240, May 1998.
32. D. A. Christie, “Sorting permutations by block-interchanges,” Information Processing Letters, vol. 60, no. 4, pp. 165 – 169, 1996.
33. L. Bulteau, G. Fertin, and I. Rusu, “Sorting by transpositions is difficult,” SIAM Journal on Discrete Mathematics, vol. 26, no. 3, pp. 1148–1180, 2012.
34. F. Farnoud (Hassanzadeh) and O. Milenkovic, “Sorting of permutations by cost-constrained transpositions,” IEEE Trans. Inf. Theor., vol. 58, pp. 3–23, Jan. 2012.
35. I. L. Markov and M. Saeedi, “Constant-optimized quantum circuits for modular multiplication and exponentiation,” Quantum Inf. Comput., vol. 12, pp. 361–394, May 2012.
36. M. L. Fredman and R. E. Tarjan, “Fibonacci heaps and their uses in improved network optimization algorithms,” J. ACM, 1987.
37. CPLEX Optimizer, http://www-01.ibm.com/software/commerce/optimization/cplex-optimizer/
38. M. Rahman and G. Dueck, “Optimal quantum circuits of three qubits,” in Multiple-Valued Logic (ISMVL), 2012 42nd IEEE International Symposium on, pp. 161–166, May 2012.
