Abstract—This brief proposes a fully dynamic discrete-time ΔΣ ADC using closed-loop two-stage cascoded floating inverter amplifiers (FIA). The proposed FIA uses a non-cascoded FIA as the 1st stage and a cascaded one as the 2nd. By using this arrangement as well as applying metal-insulator-metal (MIM) capacitors for floating reservoir capacitors, it stably achieves high gain even with the input common-mode voltage fluctuation without an additional CMFB nor calibrations. The proposed ADC fabricated in a 65 nm standard CMOS process realizes a fully dynamic operation without calibration and achieves 88.5 dB SNDR, 97.9 dB SFDR with an OSR of 256. It consumes 43.5 μW from a 1V supply at a 10 MHz sampling frequency.

Index Terms—Delta-sigma, analog-to-digital converter, dynamic, floating inverter amplifier, calibration-free.

I. INTRODUCTION

HIGH resolution analog-to-digital converters (ADCs) are always demanded and widely used especially for audio and sensor applications. For these purposes, among different ADC architectures, a ΔΣ ADC is often used thanks to its oversampling and noise-shaping properties [1]. A ΔΣ ADC usually uses operational transconductance amplifier (OTA), which is one of the most power-hungry components in the modulator [2], [3]. Recently, numerous IoT devices and systems that have multiple sensors are commonly employed [4]. To save power for an extended lifetime of those IoT systems, there is an increasing demand for the analog front end to have the scalability of the power and the operating speed in order to realize flexible system management. To achieve high resolution and high energy efficiency at the same time, one of the candidate architectures is noise-shaping SAR ADC, which can be fully dynamic [5], [6]. However, to achieve high SNR, a CDAC capacitance mismatch calibration that complicates the design is essential. In addition, since the CDAC capacitance tends to be large, driving the sampling capacitance also becomes challenging. A discrete-time (DT) ΔΣ ADC utilizing a dynamic amplifier is another candidate thanks to its simple structure without requiring complex calibration [7], [8]. However, using the dynamic amplifier in the ΔΣ loop has its drawbacks; Its moderate DC gain can not sufficiently suppress the thermal and 1/f noise contributions of the latter stages, which leads to the SNR degradation [7]. This issue is not resolved by increasing the OSR. Thus it is necessary to have high gain amplifiers even in high OSR modulators. In [8], an additional 1/f noise reduction circuit is required to improve the SNR. Another drawback is its unregulated output common-mode voltage. As the output common-mode voltage of the dynamic amplifier is typically dependent on the amplification time, the operating condition will change once the sampling frequency is altered. This prevents the scalable operation of the DT ΔΣ ADC.

The latter issue has been addressed by a floating inverter amplifier (FIA) [9]. The FIA offers a stable output common-mode voltage as well as robustness to the input common-mode fluctuation as it works in its isolated power domain powered by a floating reservoir capacitor CRES. These properties are utilized in [10] to realize the scalability of power consumption with the sampling frequency in a DT ΔΣ ADC. However, to further improve the DC gain of the FIA with single-stage configuration, it requires large transistors with a large CRES, which would deteriorate its power and area efficiency. In [11], a closed-loop, three-stage cascoded FIA is proposed as a residue amplifier in a pipeline ADC. Though it achieves a DC gain of 82 dB, an additional common-mode feedback (CMFB) circuit is required to have a stable gain, which increases the power consumption and circuit complexity.

In this brief, a single-loop 2nd-order fully dynamic DT ΔΣ ADC using a closed-loop two-stage cascoded FIA is proposed. Our two-stage cascoded FIA is composed of a conventional non-cascoded FIA as the 1st stage and a cascaded FIA as the 2nd. The proposed FIA achieves about 17 dB higher gain without an additional CMFB nor calibrations. By applying this FIA, the proposed 2nd-order DT ΔΣ ADC fabricated in 65 nm CMOS realizes a fully dynamic operation and achieves 88.5 dB SNDR at a 10 MHz sampling frequency with an OSR of 256.

The rest of this brief is organized as follows. Section II describes the proposed two-stage cascoded FIA. Section III...
Fig. 1. Schematic diagram of the proposed two-stage cascoded FIA.

Fig. 2. Simulated 1st-stage FIA output common-mode voltage.

Fig. 3. Simulated DC gain versus input common-mode voltage.

Fig. 4. (a) Unity gain frequency (UGF) and phase margin (PM) dependence on supply voltage and (b) corner conditions, and (c) DC gain dependence on supply voltage and (d) on corner conditions. In (b) and (d), the horizontal axes represent corner conditions where the first two characters respectively indicate NMOS and PMOS process corners, and C and H represent 0°C and 80°C respectively.

common-mode voltage since the bias voltage for the cascode transistors is fixed at $V_{CM}$, its impact is highly relaxed with the proposed two-stage arrangement by applying the non-cascoded FIA as the 1st stage whose output common-mode voltage is ideally constant. As reported in [9], however, the parasitic capacitance of the reservoir capacitor $C_{RES}$ degrades the stability of the output common-mode voltage. The change of the output common-mode voltage can be approximated as [9]

$$\Delta V_{OUT,CM} \approx -2 \cdot \Delta V_{IN,CM} \cdot \frac{C_P}{C_{OUT}},$$  

where $\Delta V_{OUT,CM}$, $\Delta V_{IN,CM}$, $C_P$ and $C_{OUT}$ represent the output common-mode voltage change, input common-mode voltage change, the parasitic capacitance of the reservoir capacitor $C_{RES}$ and the output capacitance of the FIA, respectively. In the case of the cascaded structure, $C_{OUT}$ for the 1st-stage FIA is usually small as it is only the gate capacitance of the input transistors in the 2nd-stage. Therefore, as given by (1), $\Delta V_{OUT,CM}$ of the 1st-stage FIA is non-negligible with a small $C_{OUT}$ in the denominator. Thus [11] chose to use a CMFB circuit to alleviate the impact. In this brief, this issue is mitigated by implementing $C_{RES}$ with a metal-insulator-metal (MIM) capacitor that consists of upper metal layers instead of a metal-oxide-metal (MOM) one. Since the MIM capacitor has much less parasitic capacitance $C_P$ than the MOM does, it can suppress the fluctuation of the output common-mode voltage even without using a dedicated compensation circuitry. In our design, to balance the parasitic capacitance at $V_{DD}$ and ground sides, the MIM capacitor for $C_{RES}$ is split into two and the connection of the one is flipped as shown in Fig. 1. Although the density of the MIM capacitor is lower than the MOM capacitor, $C_{RES}$ of the 1st-stage FIA is 2 pF in our design, which does not occupy a large part of the overall ADC. To relax the design, the 2nd-stage FIA also uses the same 2 pF $C_{RES}$, although we may be able to further improve the stability by using a smaller $C_{RES}$ in the 2nd stage as presented in [6] and [11].
III. PROPOSED DISCRETE-TIME ΔΣ ADC USING TWO-STAGE CASCODED FIA

Figure 5 shows a circuit block diagram of the proposed DT ΔΣ ADC. It is composed of a single-loop 2nd-order single-bit architecture with the input feedforward path, which relaxes the linearity requirement of the amplifiers by suppressing the signal component at their inputs. Both of the two integrators are composed of the proposed closed-loop two-stage cascoded FIA. A chopping is applied only to the 1st-stage integrator to exclude its 1/f noise contribution. \( V_{CM} \) is set to a half of \( V_{DD} \). A simple StrongArm latch comparator is used for a 1-bit quantizer [12]. No calibration is applied to the proposed DT ΔΣ ADC. Figure 5 also shows a timing diagram of the proposed ADC. Before the conversion starts, the ADC is in its reset mode where \( C_{11,2} \), \( C_{F1-3} \) and \( C_{S2} \) are discharged and all FIAs are reset. While the ADC is working, the 1st and the 2nd integrators work alternately.

Figure 6 shows a signal flow graph of the proposed DT ΔΣ ADC. With the cascaded structure, the output voltage swing of the FIA is limited. The scaling factors in the loop are properly tuned so that the output voltage of the cascoded FIA is confined within the proper range for sufficient gain, e.g., 300 mV~700 mV. Signal transfer function (STF) and noise transfer function (NTF) are respectively given by

\[
\text{STF}(z) = \frac{\left(10^{-5} - 14z^{-1} + 2z^{-2}\right)k}{1 + \left(\frac{1}{\sqrt{5}}z - 2\right)z^{-1} + \left(1 - \frac{2}{\sqrt{5}}k\right)z^{-2}}\]  \hspace{1cm} (2)

\[
\text{NTF}(z) = \frac{\frac{1}{1 + \left(\frac{1}{\sqrt{5}}z - 2\right)z^{-1} + \left(1 - \frac{2}{\sqrt{5}}k\right)z^{-2}}}{(1 - z)^{-2} - 1}, \]  \hspace{1cm} (3)

where \( k \) is the equivalent gain of the 1-bit quantizer. Equivalent quantizer gain \( k \) is determined by the following equation [13], [14].

\[
k = \frac{1}{N} \sum_{n=0}^{N} v[n]y[n] < y, y > = \frac{1}{N} \sum_{n=0}^{N} y[n]y[n], \]  \hspace{1cm} (4)

where \( v \), \( y \), and \( N \) represent the quantizer output, quantizer input, and the number of samples, respectively. This \( k \) depends on the modulator input. \( v \) and \( y \) are obtained by behavioral simulations using MATLAB. Input amplitude, frequency, and the number of samples are set to \(-6 \text{dBFS}, 2.01225 \text{kHz}, \) and \( 1048576 \), respectively, resulting in \( k = 10.1 \). With this \( k \) value, Fig. 7 depicts the STF and NTF versus the frequency normalized by the sampling frequency that exhibits almost flat STF up to the Nyquist frequency with the 2nd-order noise shaping.

IV. MEASUREMENT RESULT

The prototype of the proposed DT ΔΣ ADC is fabricated in TSMC 65 nm standard CMOS process. It occupies 190 \( \mu \text{m} \times 210 \mu \text{m} \) as shown in Fig. 8(a). To evaluate the prototype, a differential input and clock signals are applied from SRS DS360 and Tektronix AFG31252 function generators, respectively. The 1-bit output is captured by Digilent Digital Discovery logic analyzer then processed with a PC. The ADC
consumes 43.5 µW from a 1V supply at a 10 MHz sampling frequency. Figure 8(b) depicts a power breakdown of this ADC, where the analog and the digital parts consume 30.3 µW (70%) and 13.2 µW (30%), respectively. Figure 9 shows the measured output spectrum of the ADC with −0.4 dBFS input where the peak SNR of 88.9 dB is achieved at the OSR of 256. A red line in Fig. 9 shows the measured spectrum without the input source, which exhibits a lower noise floor without the power line noise. We expect from

![Fig. 6. Signal flow graph of the proposed DT ΔΣ ADC.](image)

![Fig. 7. STF and NTF of the proposed DT ΔΣ ADC.](image)

![Fig. 8. (a) Die micrograph and (b) measured power breakdown.](image)

![Fig. 9. Measured output spectra at 10MHz sampling frequency.](image)
this result that the noise contribution of the signal source used to evaluate the ADC is larger than that of the ADC itself. Supposing that the spectrum measured without the input source represents the inherent noise of the ADC, by taking the noise power from the red spectrum while taking the signal and distortion powers from the blue one, the true performance of the proposed ADC is calculated to be 88.5 dB SNDR and distortion powers from the blue one, the true performance of the noise power from the red spectrum while taking the signal itself. Supposing that the spectrum measured without the input used to evaluate the ADC is larger than that of the ADC this result that the noise contribution of the signal source

Fig. 10. Measured SNDR/SNR versus input amplitude.

Fig. 11. Measured power consumption versus sampling frequency.

Fig. 12. Measured SNDR/SNR versus sampling frequency.

V. Conclusion

This brief presents a fully dynamic 2nd-order DT ΔΣ ADC using closed-loop two-stage cascaded FIA. By implementing floating reservoir capacitors as MIM capacitors, the proposed two-stage cascaded FIA achieves high DC gain and robustness to the input common-mode voltage fluctuation without an additional CMFB circuit. The measurement results of the prototype fabricated in a 65 nm standard CMOS process prove that the proposed ADC realizes a fully dynamic operation and achieves competitive performance with a simple architecture without calibrations.

ACKNOWLEDGMENT

The LSI chip fabricated in this brief has been supported through the activities of VLSI Design and Education Center, the University of Tokyo in collaboration with Cadence Design Systems Inc. and Mentor Graphics, Inc.

REFERENCES

[1] J.-H. Han, K.-I. Cho, H.-J. Kim, J.-H. Boo, J. S. Kim, and G.-C. Ahn, “A 96dB dynamic range 2kHz bandwidth 2nd order delta-sigma modulator using modified feed-forward architecture with delayed feedback,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 68, no. 5, pp. 1645–1649, May 2021.
[2] L. Yao, M. S. J. Steyaert, and W. Sansen, “A 1-V 140-μW 88-dB audio sigma-delta modulator in 90-nm CMOS,” IEEE J. Solid-State Circuits, vol. 39, no. 11, pp. 1809–1818, Nov. 2004.
[3] L. Qi, S.-W. Sin, S.-P. U, F. Maloberti, and R. P. Martins, “A 4.2-mW 77.1-dB SNDR 5-MHz BW DT 2-1 MASH ΔΣ modulator with multirate opamp sharing,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 64, no. 10, pp. 2641–2654, Oct. 2017. [Online]. Available: https://ieeexplore.ieee.org/document/7913658
[4] M. Konijnenburg et al., “A 769 μW battery-powered single-chip SoC with BLE for multi-modal vital sign health patches,” in Proc. IEEE ISSCC, San Francisco, CA, USA, 2019, pp. 360–362.
[5] Y. Zhang, S. Liu, B. Tian, Y. Zhu, C.-H. Chan, and Z. Zhu, “A 2nd-order noise-shaping SAR ADC with lossless dynamic amplifier assisted integrator,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 67, no. 10, pp. 1819–1823, Oct. 2020.
[6] X. Tang et al., “9.5 a 13.5b-ENOB second-order noise-shaping SAR ADC with multirate opamp sharing,” in IEEE A-SSCC, Toyama, Japan, 2016, pp. 317–320.
[7] B. Zhang, R. Dou, L. Liu, and N. Wu, “A 91.2dB SNDR 66.2fJ/conv. Dynamic amplifier based 24kHz ΔΣ modulator,” in Proc. IEEE ISSCC, San Francisco, CA, USA, 2020, pp. 162–164.
[8] S. Ma, L. Liu, T. Fang, J. Liu, and N. Wu, “A discrete-time audio ΔΣ modulator using dynamic amplifier with speed enhancement and flicker noise reduction techniques,” IEEE J. Solid-State Circuits, vol. 55, no. 2, pp. 333–343, Feb. 2020.
[9] X. Tang et al., “An energy-efficient comparator with dynamic floating inverter amplifier,” IEEE J. Solid-State Circuits, vol. 55, no. 4, pp. 1011–1022, Apr. 2020.
[10] Y. Zhao et al., “A 94.1 dB DR 4.1 nW/Hz bandwidth/power scalable DTDSM for IoT sensing applications based on swing-enhanced floating inverter amplifiers,” in Proc. IEEE CICC, Austin, TX, USA, 2021, pp. 1–2.
[11] X. Tang, X. Yang, J. Liu, W. Shi, D. Z. Pan, and N. Sun, “27.4 A 0.4-to-40MS/s 75.7dB-SNDR fully dynamic event-driven pipelined ADC with 3-stage cascaded floating inverter amplifier,” in Proc. IEEE ISSCC, San Francisco, CA, USA, 2021, pp. 376–378.
[12] H. Xuand A. Abidi, “Analysis and design of regenerative comparators for low offset and noise,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 66, no. 8, pp. 2817–2830, Aug. 2019.
[13] S. Pavan, G. C. Temes, and R. Schreier, Understanding Delta-Sigma Data Converters, 2nd ed. Hoboken, NJ, USA: Wiley, 2017.
[14] A. F. Yeknami, F. Qazi, and A. Alvandpour, “Low-power DT ΔΣ modulators using SC passive filters in 65 nm CMOS,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 61, no. 2, pp. 358–370, Feb. 2014.