Process variation and analysis of FinFET for low-power applications

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Abstract: In today's microelectronics, FinFET played a leading role to reduce the device dimension at the nanometer scale. The ultra-thin fin on the FinFET device leads to suppression in short channel effect and leakage current that can make a different edge on the performance of the VLSI circuit. In this article, a comprehensive simulation and compact model of 14nm N-type FinFET presented. N-Type FinFET is simulated and analyzed the performance on the different parameters like power dissipation and on-off current ratio (I\textsubscript{on}/I\textsubscript{off}) concerning the different oxide material. Further, we analyzed the proposed device performance through the process variation by varying the parameter temperature from 200K to 350K and oxide thickness from 1 nm to 3 nm. The high current ratio value of 10\textsuperscript{10} observed in high-k oxide material in comparison to low-k oxide material that enhance the switching speed of the device in the proposed design along with analyzed the bandgap also. The power dissipation of the proposed design improved upto 38% in comparison to a low-k oxide material.

1. INTRODUCTION

As we scale down the transistor size, it leads to an increase in the leakage current (I\textsubscript{off}) that will be a challenging aspect to maintain the high performance of the VLSI circuit [1-4]. Nowadays in the VLSI industry, both low power circuits and Arithmetic & Logic circuits have become very important. In various Adder circuits, Multipliers and Digital signal processor is the key element for designing the Arithmetic unit. So certain parameters like delay, power, and power delay product are getting crucial for enhancing the efficiency of the circuit. So the designer is giving more importance to addressing constraints like low power consumption, high speed, and small area. In narrow channel MOSFET, the drain potential gets influenced by the electrostatics of FinFET channel length, this resulted to unable off the device by gate terminal saturation region. By usage of narrow gate oxides and higher-k dielectric material helps to minimize this issue by compensating an increase in the capacitance of the gate-channel. [4-6]. To minimize this issue and reducing the Leakage current & short channel, FinFET devices are considered as an alternative of the CMOS for designing the device below 22nm [6-9].

To minimize the drawbacks of the MOSFET structure concerning short channel effect and threshold, for reducing the voltage roll-off and subthreshold swing can be eliminated by the usage of FinFET devices [8-9]. Trapezoidal form shape FinFET devices used in many fabrication industries [10]. In this article, we have compared the performance parameter like on Current (I\textsubscript{on}) & off current (I\textsubscript{off}), ON/OFF (I\textsubscript{on}/I\textsubscript{off}) ratio current and Power on a different scale to the different oxide material like Silicon Oxide and Hafnium Oxide. We further investigate the proposed design by using the process variation technique. In the process variation, 3D simulation carried on TCAD Cogenda tool by varying the temperature parameter from 200K to 350 K and oxide thickness from 13nm to 16nm, observed the performance parameter of the proposed design of 14-nm FinFET device. We divided this paper divided into three segments, in the first segment brief the introduction and in second segment brief about the
work done so far on FINFETS and in the third segment explain the simulation setup with result discussion. In the last segment, we discussed the conclusion.

2. REVIEW OF THE LITERATURE

By introducing the concept of a new scaling technique like high-k/metal-gate and channel strain improved the performance of the transistor and attain better stability in terms of cost, speed, and power improvements in the VLSI Circuit[10]–[12]. Scaling down of the channel length from 22nm to 7nm is possible due to the introduction of the FinFET and it leads to further improvement on the channel electrostatics. As per the historical scaling trend of channel length leads to the double gate architecture and new scaling parameter introduces as a channel thickness [13]. Due to the three dimensional nature of the FinFET channel has reduced the overall transistor footprint and new performance booster parameter named as a ‘Fin-Effect’ ($W_{eff}$/Fin-Pitch) that’s not available in planar MOSFETs structure. The fin height (H), the width of the fin (W) and gate length ($L_{gate}$), oxide thickness, the parameter can affect the FinFET performance. The performance of the FinFET devices can boast up by varying these parameters [14]. But on these parameters are need to keep at a minimum value to avoid the short channel effect like fin thickness should be equal to 1/3 to the channel length [15]. For reducing the leakage current, gate stack can be used by introducing the dielectric material of high-k [16]. Generally, the gate stack of dielectric material (usually high-k material) minimized the degradation of the oxide layer and improved the capacitive coupling between gates to channel. Due to the smaller size with the three-dimensional structure of FinFETs, it’s very difficult to develop a compact model for its [17]. By increasing the height of the fins can moderate the Short channel Effect in FinFETs lead to significant DIBL and better subthreshold slope [18]. With a combination of increasing the Fins Effect and along with channel length leads to better result in terms of reduction in the contact area that increase the contact resistance and leads to better device performance [20]. FinFETs can be designed in two types SOI and Bulk. Substrate fin is not attached to the substrate in case of SOI but on the other hand, fin attached to the substrate directly [19]. Due to no direct contact between the fin and substrate SOI provides better insulation that minimizes the leakage current but if increases the self-heating effect. Due to this self-heating, it’s very crucial to monitor the effect of temperature on the FinFET device [21]. If we change the material of oxide from with hafnium oxide that minimizes the leakage current but it’s difficult to analyze the temperature effect due to this inclusion on the device [22]. Off current can be reduced by including spacer that results in minimizing the short channel effects. Metal gate contacts can be used instead of using polysilicon [23], and to minimize the short channel effects for fin material GaAs can be used instead of silicon [24-25].

![Figure 1. Proposed Design of the FinFET of Low- K material.](image_url)
3. STRUCTURE DESIGN & SIMULATION SETUP

| S.No | Parameter of the Proposed Device | Face value |
|------|----------------------------------|------------|
| A    | Width of the Fin of FinFET (nm)  | 12         |
| B    | Oxide thickness of the FinFET (nm) | 10 to 12 |
| C    | Height of the Fin (nm)           | 15 to 25   |
| D    | Doping Concentration of the Channel (/cm$^3$) | 10$^{15}$ to 10$^{20}$ |
| E    | Oxide Thickness (nm)             | 1 to 2     |

3.1. Material Composition & Structure Design Parameter

In the proposed designed we used the SOI structure for designing the 14-nm FinFET and used the rectangular fins shape. All the Simulation carried on the Visual TCAD by Cogenda [20]. Table 1 represents the proposed design dimensions. In the proposed material we used the low-k material of silicon oxide and high-k dielectric material Hafnium Oxide for gate oxide and substrate and fin use the silicon material. Figure 1 and figure 2, showing the 3D view of rectangular FinFET.

3.2. Simulation Setup

Visual T CAD is used for creating the three dimensional model of the proposed FinFET. In this simulation we used the drift-diffusion model and Boltzmann statistics is used. Measurement of the recombination rate analyzed by taking the summation of Direct Combination & Shockley read hall recombination. For changing the parameter of temperature in the device we set the external temperature through global command. For the channel doping of donor ($N_{d}$) 1.12×10$^{19}$ cm$^{-3}$ and acceptor ($N_{a}$) 1.12×10$^{20}$ cm$^{-3}$ is done. Doping levels of the drain and source region is different from the channel doping. In the proposed design we proposed the channel length ($L_{c}$) of the device at 14
nm and other hand drain and source region extended upto 33 nm from both sides. For the gate material, we used the PPolySi. The width of the proposed design and fin height are kept at 12 nm and 20 nm respectively. Work Function of 5.27 is used. The concentration of Hole and electron added in simulation as per below equations 1 & 2 [26].

\[
\nabla n = -\left(\frac{h^2}{6q m_n}\right) \left(\nabla^2 \sqrt{n}\right) / \sqrt{n} \\
\nabla p = -\left(\frac{h^2}{6q m_p}\right) \left(\nabla^2 \sqrt{p}\right) / \sqrt{p}
\]

(1) (2)

Where, valance band, hole concentration and electron concentration in conduction band represented by n and p & electron charge represented by q & Planck’s constant represented by h, electron and hole effective mass represented by \( m_n^* \) and \( m_p^* \).

\[
E_g(T) = E_g(0) - \alpha E_T^2 / (T + \beta E)
\]

(3)

Where, \( \beta_E = 206 \text{ K} \) and \( E_g = 1.420 \text{ eV} \) and \( \alpha \) for Si = \( 5.41 \times 10^{-4} \text{ eV/K} \).

The relationship between temperature and bandgap can be analyzed by equation 3.[28]

4. RESULTS AND DISCUSSION

At zero gate voltage, inversion charge stable inside the semiconductor but when we increase the gate voltage that impacts the inversion charge and it starts decreasing as we increase the gate voltage due to the accumulation of the majority charge in that area. Generally, this kind of modulation is used around the gate region of the FinFETs device. [27-29]. In this paper, we compared the device performance based on the different dielectric material. All the parameters are kept the same for both the designed.

\[
I_D = \Phi + \mu C_{OX} \left(W_g L_g\right) \left(V_{gs} - V_{ds}\right) / 2m
\]

(4)

Where \( I_D \) is Drain current at saturation region, \( W_g \) is width of gate and \( L_g \) is length of the gate and \( V_{ds} \) is drain to source voltage and \( m \) follow by 2. \( \Phi \) is gate material work function, \( \mu \) is mobility and \( V_{gs} \) is gate to source voltage

\[
m = 1 + \left(3T_{OX} / T_{Si}\right)
\]

(5)

Where \( T_{ox} \) is gate oxide thickness and Fin thickness is \( T_{Si} \).

Figure 3 shows the comparison of the drain current vs. gate voltage at a constant value of drains source voltage (1V). Figure 3 depicts that on current and off current on the higher side for high-\( k \) material in comparison to low-\( k \) material. This is due to the increase in the concentration of the electron around the channel due to the increase in the permittivity of the oxide.

As per table 2 and figure 3, OFF current and on current values are on the higher side. Mainly ON state Current (\( I_{on} \)) and off-state current (\( I_{off} \)) are two key parameters for measurement of the electrical performance of any circuit to measure its speed and standby time. By changing the value of the work function of gate metal of a device can attain the different application requirements such as low-standby power and high-performance. The value of the ON state current and OFF state current calculated for both the region Active and saturation region as shown in table 2. The current ratio can be enhanced by increasing and or decreasing by using the gate stack with high- \( k \) material. On/Off Ratio current goes upto \( 10^{10} \) in case of high-\( k \) in comparison to low-\( k \) which enhances the switching speed of the device.
TABLE 2: Comparison of Gate Voltage vs. Drain Voltage

| Gate Voltage (V) | Drain Current (A) at high-K | Drain Current (A) at Low-K |
|------------------|----------------------------|---------------------------|
| 0                | 2.15E-16                   | 1.62E-12                  |
| 0.05             | 6.24E-16                   | 4.61E-12                  |
| 0.1              | 2.02E-15                   | 1.28E-11                  |
| 0.15             | 7.41E-15                   | 3.50E-11                  |
| 0.2              | 3.01E-14                   | 9.47E-11                  |
| 0.25             | 1.23E-13                   | 2.54E-10                  |
| 0.3              | 4.99E-13                   | 6.77E-10                  |
| 0.35             | 2.01E-12                   | 1.79E-09                  |
| 0.4              | 7.96E-12                   | 4.71E-09                  |
| 0.45             | 3.07E-11                   | 1.23E-08                  |
| 0.5              | 1.15E-10                   | 3.16E-08                  |
| 0.55             | 4.22E-10                   | 7.94E-08                  |
| 0.6              | 1.52E-09                   | 1.90E-07                  |
| 0.65             | 5.41E-09                   | 4.15E-07                  |
| 0.7              | 1.90E-08                   | 8.23E-07                  |
| 0.75             | 6.51E-08                   | 1.49E-06                  |
| 0.8              | 2.13E-07                   | 2.51E-06                  |
| 0.85             | 6.25E-07                   | 3.94E-06                  |
| 0.9              | 1.58E-06                   | 5.85E-06                  |
| 0.95             | 3.46E-06                   | 8.31E-06                  |
| 1                | 6.83E-06                   | 1.14E-05                  |

TABLE 3: Comparison of Gate Voltage vs. Power

| Gate Voltage (V) | Power At High-K(W) | Power At Low-K(W) |
|------------------|--------------------|-------------------|
| 0                | 2.14E-16           | 1.62E-12          |
| 0.05             | 6.25E-16           | 4.61E-12          |
| 0.1              | 2.02E-15           | 1.28E-11          |
| 0.15             | 7.44E-15           | 3.50E-11          |
| 0.2              | 3.02E-14           | 9.47E-11          |
| 0.25             | 1.24E-13           | 2.54E-10          |
| 0.3              | 5.04E-13           | 6.77E-10          |
| 0.35             | 2.04E-12           | 1.79E-09          |
| 0.4              | 8.11E-12           | 4.71E-09          |
| 0.45             | 3.15E-11           | 1.23E-08          |
| 0.5              | 1.19E-10           | 3.16E-08          |
| 0.55             | 4.42E-10           | 7.94E-08          |
| 0.6              | 1.61E-09           | 1.90E-07          |
| 0.65             | 5.78E-09           | 4.15E-07          |
| 0.7              | 2.05E-08           | 8.23E-07          |
| 0.75             | 7.09E-08           | 1.49E-06          |
| 0.8              | 2.32E-07           | 2.51E-06          |
| 0.85             | 6.74E-07           | 3.94E-06          |
| 0.9              | 1.68E-06           | 5.85E-06          |
| 0.95             | 3.62E-06           | 8.31E-06          |
| 1                | 7.06E-06           | 1.14E-05          |

Figure 4 and Table 3, shows the comparison of the Gate voltage vs. Power for both the dielectric material at different oxide material. In low- k material, dissipation of the power is high at saturation region in comparison to high- k material and the same has been observed in the active region for both the design. This is due to minimize leakage current in high- k material hence minimum power dissipation observed. In contrast to the active region, power dissipation is on the higher side for high- k material as compared to the material having low-k value. For high-k material on current value is a little higher in comparison to the material with low- k value (as per table 3) due to this power dissipation is high.
\[ V_{th} = \phi + \left( \frac{KT}{q} \right) \ln \left( \frac{2C_{ox}KT}{q^2n_{i,Si}} \right) + \left( \frac{h^2n^2}{2m_d w^2} \right) \]  

(6)

Where \( V_{th} \) is threshold voltage, \( K \) is Boltzmann’s constant, \( q \) is charge of electron and \( n_i \) is intrinsic silicon concentration, \( h \) is Planck’s constant, fin thickness is \( T_{SI} \) and \( T \) is temperature (K), \( W_{Si} \) is width of the fin.

As per equation 6, for the proposed design threshold voltage calculated and it around 0.049 V for the higher oxide material and 0.098 V for the lower oxide material.

Charge carrier and temperature can be co-related as per equation given in 7. Where Energy gap represented with \( E_g \) and Temperature represented by \( T \).

\[ N_i = 5.2 \times 10^{15} \times T^3 \times e^{\frac{-E_g}{2kT}} \]  

(7)

When the temperature of the devices rises, then the gap between the Fermi levels and conduction band in the channel region decreases due to increases in the charge carrier. As per figure 6 and Table 4, we can analyze this phenomenon as we change the temperature value from 200 K to 350K. At 250 K, the maximum variation in the drain current vs. gate voltage is observed as off Current value at 2.15E-16 and on current value is 8.05E-06 in comparison to 200K, 300K, and 350K.

It has been observed that analysis was done on the temperature, phonon scattering is more dominating and while increasing the temperature from 200K to 350 K, mobility of the device decreases as per the equation 8. Where \( T_0 \) is the temperature at 300K and \( T \) is the lattice temperature, mobility of the electron is represented by \( \mu_{eff} \)

\[ \mu_{eff} = \mu_{eff0} \left( \frac{T}{T_0} \right)^{-2} \]  

(8)

As per figure 7, as we increase the temperature from 200 K to 350K, the gap between the conduction band and Fermi level band decreases due to more accumulation of the charge density inside the Fin parts. Moreover, this factor more dominant inside the channel region as compared to the Source and drain region.

As per figure 5 and Table 5, we can depict that while changing the oxide thickness for high-k designed from 1 nm to 3 nm will not affect the device performances. As we decreasing the oxide thickness then gate losses its better controllability over the channel but in the proposed device it is showing less impact as we reduce from 3nm to 1nm.
Figure 5. Oxide Thickness Variation of high k material Fin-FETs.

Figure 6. Temperature Analysis at $V_{ds}$ (1V)

Figure 7. Conduction Band Vs. Channel length
| Gate voltage (V) | Drain Current (A) | Drain Current At Vds 0.1 (V) when Oxide thickness 2nm | Drain Current At Vds 1 V when Oxide thickness 3nm | Drain Current At Vds 0.1 (V) when Oxide thickness 4nm | Drain Current At Vds 1 V when Oxide thickness 4nm |
|-----------------|------------------|----------------------------------|---------------------------------|---------------------------------|---------------------------------|
| 0.05            | 6.25E-16         | 6.25E-16                         | 6.25E-16                       | 6.24E-16                       | 6.24E-16                       |
| 0.1             | 2.02E-15         | 2.02E-15                         | 2.02E-15                       | 2.02E-15                       | 2.02E-15                       |
| 0.15            | 7.44E-15         | 7.45E-15                         | 7.44E-15                       | 7.42E-15                       | 7.42E-15                       |
| 0.2             | 3.02E-14         | 3.03E-14                         | 3.02E-14                       | 3.01E-14                       | 3.01E-14                       |
| 0.25            | 1.23E-13         | 1.24E-13                         | 1.24E-13                       | 1.23E-13                       | 1.23E-13                       |
| 0.3             | 5.01E-13         | 5.07E-13                         | 5.04E-13                       | 4.99E-13                       | 4.99E-13                       |
| 0.35            | 2.02E-12         | 2.05E-12                         | 2.04E-12                       | 2.01E-12                       | 2.01E-12                       |
| 0.4             | 7.99E-12         | 8.19E-12                         | 8.11E-12                       | 7.93E-12                       | 7.93E-12                       |
| 0.45            | 3.09E-11         | 3.21E-11                         | 3.15E-11                       | 3.06E-11                       | 3.06E-11                       |
| 0.5             | 1.16E-10         | 1.23E-10                         | 1.19E-10                       | 1.15E-10                       | 1.15E-10                       |
| 0.55            | 4.26E-10         | 4.42E-10                         | 4.42E-10                       | 4.21E-10                       | 4.21E-10                       |
| 0.6             | 1.54E-09         | 1.54E-09                         | 1.61E-09                       | 1.52E-09                       | 1.52E-09                       |
| 0.65            | 5.49E-09         | 5.49E-09                         | 5.78E-09                       | 5.40E-09                       | 5.40E-09                       |
| 0.7             | 1.93E-08         | 2.00E-08                         | 2.05E-08                       | 1.89E-08                       | 1.89E-08                       |
| 0.75            | 6.65E-08         | 7.25E-08                         | 7.09E-08                       | 6.51E-08                       | 6.51E-08                       |
| 0.8             | 2.18E-07         | 2.54E-07                         | 2.32E-07                       | 2.13E-07                       | 2.13E-07                       |
| 0.85            | 6.38E-07         | 7.80E-07                         | 6.74E-07                       | 6.27E-07                       | 6.27E-07                       |
| 0.9             | 1.61E-06         | 1.98E-06                         | 1.68E-06                       | 1.58E-06                       | 1.58E-06                       |
| 0.95            | 3.51E-06         | 4.23E-06                         | 3.62E-06                       | 3.47E-06                       | 3.47E-06                       |
| 1               | 6.90E-06         | 8.05E-06                         | 7.06E-06                       | 6.85E-06                       | 6.85E-06                       |

**TABLE 4. Temperature Analysis of high-k material.**
5. CONCLUSION

In the paper, the three-dimensional structure of 14nm FinFET is proposed that analyzed the different oxide materials like silicon oxide and hafnium oxide and compared its performance parameters like Current ratio on the different regions like saturation and active. In high-\-k material current on/off ratio achieved at a 1010 and power dissipation also improved upto 38% in the proposed design. Further, process variation also carried out on the proposed design and analyze shifting of Fermi level band for the design. So the proposed design attains more stability while increasing the temperature from 200K to 300K. Due to high switching speed and temperature stability, we can use this device for designing of RF-based application.

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