A Hybrid FeMFET-CMOS Analog Synapse Circuit for Neural Network Training and Inference

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Abstract—An analog synapse circuit based on ferroelectric-metal field-effect transistors is proposed, that offers 6-bit weight precision. The circuit is comprised of volatile least significant bits (LSBs) used solely during training, and non-volatile most significant bits (MSBs) used for both training and inference. The design works at a 1.8V logic-compatible voltage, provides $10^{10}$ endurance cycles, and requires only 250ps update pulses. A variant of LeNet trained with the proposed synapse achieves 98.2% accuracy on MNIST, which is only 0.4% lower than an ideal implementation of the same network.

I. INTRODUCTION

Given the exponential growth of data, researchers are investigating new ways to automate data analysis through the use of deep neural networks (DNNs). DNN accelerators that perform multiplication and addition in the analog domain, e.g., using resistive devices as synapses in crossbar arrays, are appealing and could reduce the time and energy associated with DNN training and inference [1] by orders of magnitude [2].

Per [2], to offer the greatest application-level impact, synapses (i.e., crosspoints in crossbar arrays) should afford (i) update pulses with 1ns width and ±1V magnitude for potentiation and depression (i.e. increasing and decreasing conductance, respectively), and (ii) symmetric and linear weight updates where weights have 1000 unique states/offer ~10-bit precision. Emerging non-volatile resistive devices, e.g., FeMFETs [9] and CMOS transistors. FeMFETs represent non-volatile most significant bits (MSBs) and are employed during training. The proposed synapse operates at a logic-compatible voltage of 1.8V, requires symmetric and identical 250ps programming pulses for very fast potentiation and depression, and provides $10^{10}$ MSB endurance cycles. The synapse circuit is simulated using an experimentally calibrated FeMFET model [9] and a 65nm CMOS PTM [10] model (for uniform comparisons to other approaches). When training a variant of LeNet [11] on the MNIST [12] dataset, we achieve an accuracy of 98.2%, which is only 0.4% lower than an ideal implementation of the same network with the same bit precision. Furthermore, the proposed synapse offers improvements of up to 26% in area, 44.8% in leakage power, 16.7% in LSB update pulse duration, and two orders of magnitude in endurance cycles, when compared to state-of-the-art hybrid synaptic circuits. Our proposed synapse can be extended to an 8-bit design, enabling a VGG-like network to achieve 88.8% accuracy on CIFAR-10 (only 0.8% lower than an ideal implementation of the same network).

II. BACKGROUND AND RELATED WORK

A. The FeMFET device

A FeMFET incorporates a ferroelectric (FE) capacitor in the back-end of line (BEOL) (Fig. 1(a)), which reduces the maximum required programming voltage to a logic-compatible level of 1.8V (compared to 4V in FeFETs) and increases endurance to $10^{10}$ cycles. These improvements are obtained by independently optimizing the area of the FE capacitor and the MOSFET, which allows for maximum voltage drop across the FE [9]. FeMFETs have been experimentally demonstrated [9].
A. Synapse circuit design

Our proposed 6-bit synapse, (Fig. 3(a)) is comprised of 3T1C LSB and 1T1FeFET MSB sub-circuits. Though our synapse circuit is similar to the 2PCM+3T1C design in Fig. 2(a), it operates with a single-phase read-out and does not require additional circuitry for arithmetic operations (to be elaborated below). Furthermore, our design reduces the number of elements compared to the 2PCM+3T1C design while attaining the same bit precision. One might wonder if one could substitute a FeFET with a FeMFET in the 2T1F design (Fig. 2(b)) to alleviate high programming voltages and large I/O transistor overheads. Unfortunately, a simple drop-in replace does not suffice. By changing FeFET polarization, the threshold voltage is changed without altering the shape of the memory window [4], which facilitates the 2T1F design. However, when programming a FeMFET to a different state, both the threshold voltage and the memory window shape change [9], which prohibits a 2T1FeMFET design.

Our proposed synapse works as follows. The MSB sub-circuit encodes data as the FeMFET polarization state. Four distinct FeMFET states were chosen as the MSB states which replace does not suffice. By changing FeFET polarization, the threshold voltage is changed without altering the shape of the memory window [4], which facilitates the 2T1F design. However, when programming a FeMFET to a different state, both the threshold voltage and the memory window shape change [9], which prohibits a 2T1FeMFET design.

Finally, while ongoing efforts aim to improve endurance, the endurance of current FeFETs is ~10^5 write cycles [15], which limits the applicability of this design for in-situ training.

III. HYBRID FeMFET-CMOS SYNAPSE CIRCUIT

We adapt a model, calibrated by experimental data, to represent the characteristics of FeMFETs [14]. Fig. 1(b) shows four different states (i.e., on current) of a FeMFET obtainable with different programming voltages. While the FeMFET device does not in and of itself deliver 1000 states [2], its low write voltage and high endurance make it attractive as a synaptic device for crossbar arrays/hybrid synaptic circuits.

B. Existing hybrid synapse circuits

Hybrid synapse circuits built with CMOS and emerging devices can exploit the advantages of both types of devices. A hybrid synapse was first proposed in [5] where two PCM devices (for positive and negative values) represent the MSBs, and a three-transistor plus one capacitor (3T1C) circuit represents the LSBs (Fig. 2(a)) – referred to as a 2PCM+3T1C design. The MSBs are non-volatile and used for training and inference, while the LSBs are volatile and are only used during training (i.e., as higher precision is required for training than inference [5], [8]). This design requires update pulses of 300ps width and 1V magnitude. It also requires a 3-phase read-out which induces additional delay. Furthermore, once the three values ($G^+$, $G^-$, and $g$ in Fig. 2(a)) are read from the synapse and digitized, the actual contribution of the synapse to the output must be calculated as $F \times (G^+ - G^-) + g$, where $F$ is the gain factor. This operation is typically done with multiplication in the periphery of the crossbar. Training with this synapse structure on the MNIST dataset achieved an accuracy of 97.95% for an MLP with 784-150-125-10 neurons. Note that two PCM devices are required in this design as PCM devices do not have bi-directional symmetry in weight updates, which inversely impacts crossbar array area and energy.

In [8], a 2T-1FeFET (2T1F) synapse circuit (Fig. 2(b)) was proposed and can obtain 6 or 7 bits of precision via 2 non-volatile MSBs represented by the polarization states of an FeFET, and 4 or 5 volatile LSBs represented by the gate voltage of the FeFET. This design only uses 3 devices and works with a single-phase read-out scheme. The 2T1F synapse achieves a training accuracy of 97.3% and 87% for a variant of LeNet and a VGG-like network for the MNIST and CIFAR-10 datasets, respectively. However, this circuit uses I/O transistors with 3.3V supplies and an FeFET with programming voltages in the 2V-4V range. Collectively, these requirements increase power consumption and complicate the logic compatible implementation of the 2T1F design. Furthermore, by relying on a large FeFET ($4\mu m \times 2\mu m$) with a large gate capacitance to represent the LSBs, and large I/O transistors ($L = 0.5\mu m$), the area of the synapse is not reduced despite a lower device count.
simulated the synapse circuit in SPICE. Fig. 4(a) shows the simulated conductance update curve of the proposed 6-bit synapse, which exhibits high linearity and up/down symmetry.

Fig. 4(b) shows the weight update operation (as waveforms obtained from SPICE simulation) of the proposed 6-bit synapse circuit. When positive/negative pulse inputs are applied to $V_{gp}/V_{gn}$ (Fig. 4(b-i)), $V_G$ increases/decreases by 10mV per pulse. When $V_G$ surpasses 0.73V (Fig. 4(b-ii)), the total current of the synapse ($I_{SL}$) becomes larger than the reference current (Fig. 4(b-iii)), which triggers a weight transfer from the LSB sub-circuit to the MSB sub-circuit. The MSB device must be programmed to a higher state and $V_G$ must be reduced to the voltage of the lowest state, keeping the total current $I_{SL}$ the same. Similarly, if the current drops below the reference current, the MSB must be programmed to a lower state and $V_G$ must be increased to the voltage of the highest state. For the 6-bit design, 3 reference currents are required to distinguish between the 4 FeMFET states.

B. Training and inference with the proposed synapse circuit

When performing neural network inference with our synapse, only the MSB sub-circuit is active and its conductance is multiplied with the input voltages to generate outputs. When training neural networks with the proposed synapses, update pulses are applied to the volatile, highly symmetric, and fast LSB sub-circuit to attain high accuracy and rapid training. For every training batch, errors are backpropagated using stochastic gradient descent and appropriate up/down pulses are applied to the LSB. After every $N$ (e.g., 100, 200, or 300) batches, the information in the LSB sub-circuit must be transferred to the MSB sub-circuit to preserve information in non-volatile MSBs and avoid LSB saturation. Determining transfer frequency and what state the LSB should retain after transfer is critical to the training accuracy (see Sec. [IV]).

To elaborate, note that the state of the LSB sub-circuit is degraded as $V_G$ leaks over time. Hence, information cannot be stored in it for long periods. However, information transfer from the LSBs to the MSBs is an expensive operation as (i) the current of the synapse must be examined to ensure that an MSB update is indeed required, and (ii) longer and higher amplitude pulses must be employed to update the MSBs. Thus, information should be transferred to the non-volatile MSB sub-

circuit at a rate that avoids information loss of the LSBs, and as infrequently as possible. The impact of the transfer interval length will be evaluated in Sec. [IV].

To accurately implement weight transfer, the residual information in the LSBs must be preserved. However, this implementation requires additional high-resolution DAC/ADC pairs to program the LSB according to the residual information. To reduce this transfer overhead, once the transfer is conducted, our design simply sets the state of the LSB to its mid-range. The MSB synapse design with three reference currents $I_1$, $I_2$, and $I_3$, three scenarios can occur after a weight transfer: (i) $I_1 \ll I_{SL} < I_2$, i.e., the synapse is closer to the next MSB state. After the transfer, $V_G$ being programmed to its mid-range state leads to a lower LSB state. (ii) $I_1 < I_{SL} \ll I_2$ (the opposite of case (i)). In this case, the LSB state is higher than it should be. (iii) LSBs are (ideally) in the mid-range state. Clearly, the first two cases incur some loss in the LSB state and reduce the achieved training accuracy. We will evaluate the effects of this in Sec. [IV].

C. 8-bit extension of the proposed synapse circuit

To improve the accuracy in both training and inference for more complicated datasets such as CIFAR10, we propose to extend the design in Fig. 3(a) to an 8-bit synapse circuit. Specifically, an extended MSB (EMSB) sub-circuit is added to the 6-bit circuit as shown in Fig. 5(a). The total current of the 8-bit circuit with two MSB (EMSB and MSB) sub-circuits is shown in Fig. 5(b). The W/L of the FeMFET in the EMSB sub-circuit is increased by $4 \times$ when compared to that of the MSB sub-circuit to allow more distinct conductance states. Similar to the 6-bit design, in this circuit, the difference between the states of the EMSB sub-circuit is filled by the MSB current values, and those of the MSBs are filled by the LSBs, to realize 8-bit precision. The weight update operation of this design is similar to the 6-bit design, with the difference of having 3 extra reference currents to distinguish EMSB device states.

IV. Evaluation

We first evaluate the training accuracy of our synapses. We train a variant of LeNet with the MNIST [12] dataset using the 6-bit synapse circuit, and a VGG-like network with the CIFAR10 dataset using the 8-bit design. The LeNet and VGG networks are identical to the networks trained in [8].
In this paper, new hybrid FeMFET-CMOS analog synapse circuits offering 6-bit and 8-bit precision for in-situ training of neural networks were proposed. Our design is superior to other hybrid synapse designs in terms of area, power, performance, and endurance, and approaches software accuracies.

### A. Neural network training accuracy evaluation

Fig. 6 shows the results of training the LeNet network with the 6-bit synapse circuit with MNIST. The software baseline is not trained with our synapse circuit, assuming that weight transfer occurs when the LSB is saturated and no residual information is lost on the LSB after transfer. The achieved accuracy is ~98.5% (~0.1% lower than the baseline). Recall that weight transfers may cause LSB information loss (Sec. III-B). Thus, shorter transfer intervals lead to the accumulation of information loss on the LSB due to more frequent transfers. Hence, the achieved accuracy of our synapse is directly correlated with the transfer interval. A transfer interval of 300 batches achieves ~98.2% accuracy, with only ~0.4% degradation compared to the baseline, whereas a transfer interval of 100 shows ~1.6% degradation and achieves a ~97% accuracy.

Though, theoretically, longer transfer intervals lead to higher accuracy, the existence of the leakage current path in the LSB sub-circuit results in LSB information decay. Hence, to choose a suitable transfer interval, we estimate the required time for training LeNet (forward pass + backpropagation + weight update) on a single batch (batch size is 100) using the proposed synapse circuits. With 250ps pulses and the same array assumptions as [8], i.e., $128 \times 128$ array size, 2ns read delay, and 8 columns sharing an ADC, we find this time to be ~700ns. We then evaluate the leakage of node G in Fig. 3(b) and find the time for $V_G$ to drop 10mV (equivalent to one LSB state) to be 215$\mu$s in the worst-case scenario. This allows for a batch transfer interval of ~300 when training LeNet with the MNIST dataset, whereas the 2T1F design can only achieve a transfer interval of ~200 [8]. Comparing our accuracy results with the 2T1F design shows an improvement of almost ~1% in accuracy due to both increased transfer interval and a more linear and symmetric update curve (Fig. 4(a)).

When considering a VGG network, an 8-bit synapse, the CIFAR-10 dataset, and a transfer interval of 300 batches, the achievable accuracy is 89.3% – just 0.3% lower than a baseline software implementation of 89.6%. Having 4 bits for MSBs reduces the significance of the 4 LSBs compared to 2 bits for MSBs. Also, LSB state loss during transfers adds stochasticity to the weights. However, as a larger network must be trained, the training time per batch increases by ~3x when compared to LeNet. Hence, we can only use a transfer interval of 100 batches, which achieves an accuracy of ~88.8% – 1.8% higher than the 2T1F design (87%).

### B. System-level benchmark results

System-level benchmark results of the 2T1F and 2PCM+3T1C hybrid synapse circuits are presented in [18] using the NeuroSim+ [17] tool. For fair comparison, we benchmark our proposed 6-bit synapse circuit with the same assumptions made in [18]. Table I presents the device parameters as well as the area and leakage power for training an MLP with 400×200×10 neurons with MNIST. The proposed 6-bit synapse circuit reduces the area by 26%, given the reduced number of devices when compared to the 2PCM+3T1C design. As the size of the employed transistors in the 2T1F design is larger, smaller transistor sizing afforded by our FeMFET approach reduces the leakage power of our design by 44.8%. Update pulse speed is improved by 16.7% via tuning of the LSB sub-circuit. Furthermore, FeMFETs yield 2 and 5 orders of magnitude more endurance cycles compared to PCMs [5] and FeFETs [15], respectively, which is favorable when using the circuits for in-situ training.

### V. Conclusion

In this paper, new hybrid FeMFET-CMOS analog synapse circuits offering 6-bit and 8-bit precision for in-situ training of neural networks were proposed. Our design is superior to other hybrid synapse designs in terms of area, power, performance, and endurance, and approaches software accuracies.

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