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Improving stability in two-dimensional transistors with amorphous gate oxides by Fermi-level tuning

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Electronic devices based on two-dimensional semiconductors suffer from limited electrical stability because charge carriers originating from the semiconductors interact with defects in the surrounding insulators. In field-effect transistors, the resulting trapped charges can lead to large hysteresis and device drifts, particularly when common amorphous gate oxides (such as silicon or hafnium dioxide) are used, hindering stable circuit operation. Here, we show that device stability in graphene-based field-effect transistors with amorphous gate oxides can be improved by Fermi-level tuning. We deliberately tune the Fermi level of the channel to maximize the energy distance between the charge carriers in the channel and the defect bands in the amorphous aluminium gate oxide. Charge trapping is highly sensitive to the energetic alignment of the Fermi level of the channel with the defect band in the insulator, and thus, our approach minimizes the amount of electrically active border traps without the need to reduce the total number of traps in the insulator.

Two-dimensional (2D) semiconductors are a potential channel material for ultimately scaled field-effect transistors (FETs). In contrast to silicon, 2D semiconductors retain sizable mobilities at atomic layer thicknesses below 1 nm, a thickness that also helps to suppress short-channel effects in FETs and thus allows for physical channel lengths below 5 nm (ref. 1). Furthermore, the integration of 2D materials in van der Waals heterostructures provides design options for energy-efficient transistors that can overcome the limitations of thermal charge-carrier injection. In addition, 2D materials are of potential use in a broad range of applications, including photonics and optoelectronics, neuromorphic computing, nanoelectromechanical systems, and gas and biological sensors.

There is, however, currently a lack of low-resistive contacts to 2D semiconductors, which minimize the prevalent Schottky barriers. In addition, there is a lack of suitable gate insulators that can ensure high interface quality, scalability and a minimum of electrically active border traps, the presence of which in the insulator close to the channel limits device stability. These two challenges are major obstacles for the industrial applications of 2D-based nanoelectronics and, being independent from each other, need to be separately addressed. There has been recent progress regarding the formation of low-barrier contacts for 2D semiconductors using contact gating or semimetallic bismuth contacts to achieve ultralow contact resistances11. However, the need to find a suitable insulator with a minimum number of electrically active traps remains. Stability studies of 2D FETs typically show a stability that is at least two orders of magnitude worse12,13 compared with silicon-based FETs4,14.

Measurements of FET stability typically evaluate the hysteresis in the transfer characteristics15 and stability of threshold voltage under prolonged periods of applied elevated gate biases and temperatures (bias temperature instability (BTI))14. Charge trapping inside the gate oxide has been identified as the root cause of BTI15,16. At elevated gate biases and temperatures, charges are transferred between the channel and gate oxide in a phonon-mediated transition, with charging time constants spanning a wide range, from picoseconds to years14,17. Border traps in the gate oxide close to the channel determine the long-term stability and reliability of silicon FETs14, whereas in 2D-material-based FETs, they typically limit device stability on much shorter timescales14,18.

In amorphous oxides, the defect trap levels vary due to the differing surroundings of every instance of atomic defects19. In the first approximation, the energy levels of defects follow a normal distribution around the average defect levels, forming defect bands20. Consequently, the overall density of border traps and the widths of the corresponding defect bands can be considerably reduced by using crystalline insulators, such as hexagonal boron nitride (hBN) or calcium fluoride (CaF2). However, these insulators are difficult to synthesize and have several technological challenges. For example, current state-of-the-art crystalline hBN can be grown only at temperatures above 1,200 °C (ref. 21) and CaF2 requires a crystalline silicon(111) substrate for growth, allowing only back-gated configurations21. In addition, hBN is unsuitable for use as a scaled gate insulator because of its small dielectric constant22.

In this Article, we show that the stability and reliability of 2D-material-based FETs with amorphous gate oxides can be improved by tuning the Fermi level (EF) of the 2D channel material such that it maximizes the energy distance between the charge carriers in the channel and the defect bands in the gate insulator during device operation. This can be achieved via a careful selection of the 2D material and amorphous gate oxide, as well as by doping the 2D layer to shift EF away from the defect bands in the gate insulator. Graphene FETs (GFETs) with aluminium oxide (Al2O3) as the top-gate oxide are measured and compared, where one of

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the device batches uses a p-doped graphene layer. The GFET batch where $E_F$ is tuned away from the $\text{Al}_2\text{O}_3$ defect band edge shows reduced hysteresis and BTI. We further verify the approach with technology computer-aided design (TCAD) simulations\(^1\). In addition, double-gated GFETs are fabricated, where the back gate is used to directly tune the Fermi level in the graphene monolayer via electrostatic doping. This shows that the stability observed for top-gate operation strongly depends on the location of $E_F$. Our approach aims to design a metal–oxide–semiconductor (MOS) system with a minimal amount of electrically active border traps without the need to reduce the total number of traps in the insulator.

**Fermi-level tuning for increasing stability of 2D FETs**

Our stability-based design approach is centred on the analysis and design of the band diagram of the MOS system, including the defect bands in the insulator. Fig. 1a shows a top-gated GFET that forms an example MOS system out of aluminium (metal), $\text{Al}_2\text{O}_3$ (oxide) and graphene (semiconductor). The corresponding band diagram of a cut through the MOS stack (Fig. 1a, left, indicated by arrow) is shown on the right. Every material is characterized in this view by its electron affinity and thus the energetic distance of the conduction band edge to the vacuum level, as well as its bandgap. In the case of metals and semi-metals, the work function, the energetic distance of $E_F$ to the vacuum level, determines the energetic location of charge carriers. In this regard, we use the Schottky–Mott rule to determine the band alignments shown as a zero-order approximation, thereby neglecting interface-specific reactions and charge imbalances that would lead to additional shifts on the order of a few hundred millielectronvolts\(^1\). Knowledge of the energetic position of the oxide’s defect bands and alignment to $E_F$ is the core of our design approach.

The energetic position of defect bands in amorphous oxides is an intrinsic material property\(^2,3\), as defect bands are related to certain defective atomic configurations inside the amorphous material, which result in slightly varying trap levels depending on the local surroundings of the defects. In effect, the superposition of the trap levels of many atomic defects forms the defect band, characterized by the average energetic trap level $E_T$ and the standard deviation of the trap level distribution $\sigma_{E_T}$. To experimentally determine the energetic location of the defect bands, the oxide defect states can be probed by electrical measurements, which analyse conductance variations in MOS systems\(^2,3\) or by electron paramagnetic resonance measurements, which detect the magnetic moment of unpaired electrons\(^4\). Defect bands can be theoretically determined using ab initio calculations where possible defect states and their prevalence are analysed, thereby identifying electrically active defect configurations such as oxygen vacancies\(^5\) or hydrogen-related defects\(^6\). Currently, the energetic locations of oxide defect bands are known for amorphous $\text{SiO}_2$ (ref. \(^7\)), $\text{HfO}_2$ (refs. \(^2,6\)) and $\text{Al}_2\text{O}_3$ (ref. \(^2\)) insulators. Besides the location of the defect bands, another essential property of insulator traps is their extremely broad distribution of time constants, ranging from the picoseconds regime up to years\(^8,9\). As these insulator traps lead to noise, hysteresis and drifts, it is important to thoroughly characterize both traps’ time constants and their energetic location within the defect bands.

Based on the band alignment of the graphene work function to the defect bands in $\text{Al}_2\text{O}_3$, we can predict the electrical stability of the threshold voltage in these FETs. In Fig. 1a (left band diagram), the work function of graphene is shown to be at 3.9 eV, which corresponds to n-doped graphene\(^7\). This graphene layer’s $E_F$ lies in the middle of the $\text{Al}_2\text{O}_3$ defect band. Due to this alignment within the defect band, charge traps in the oxide capture and frequently emit charges. As the applied gate voltage modifies the charging probabilities of the defects according to the electric field\(^7\), $V_{TH}$ depends on the biasing history and a pronounced hysteresis is visible. In addition, $V_{TH}$ drifts considerably during prolonged periods of applied gate biases.

However, the theoretical considerations of Fig. 1a suggest that FET stability can be tuned by moving $E_F$ down by p doping the graphene layer. Here the $E_F$ value of graphene of 5.1 eV can be achieved through p doping\(^4\). As the graphene Fermi level is located below the $\text{Al}_2\text{O}_3$ defect band, charge transfer is unlikely. Therefore, the oxide defects are electrically inactive, resulting in stable $V_{TH}$ throughout device operation, independent of the applied biases. In graphene, doping with different adsorbates and substrates results in a quasi-continuous variation in the Fermi level between 3.4 and 5.1 eV (refs. \(^5,10\)), which can be used to tune the Fermi level during device design to minimize the impact of oxide defect bands.

With some adaptation, the same stability-based design process can be applied to enhance the stability in FETs based on 2D semiconductors; Fig. 1b shows the schematic of a WS\(_2\) FET with $\text{HfO}_2$ top-gate oxide. If the Fermi level is aligned close to the conduction band, electrons within WS\(_2\) are the majority charge carriers dominating the current flow in Schottky-barrier FETs. As the conduction band edge of WS\(_2\) is aligned with the electron-trapping defect band of $\text{HfO}_2$, charge transfer to oxide defects is frequent. If WS\(_2\) was p doped instead of n doped, holes at the valence band edge would be the majority (Fig. 1b, right band diagram). As the valence band edge of WS\(_2\) is located below the hole-trapping band in $\text{HfO}_2$, the charging of oxide defects is highly unlikely. Therefore, for p-doped WS\(_2\) in combination with $\text{HfO}_2$ gate oxide, there are no electrically active oxide traps, leading to a stable $V_{TH}$ during device operation. It should be noted that for 2D semiconductors, the charges are always injected from the conduction or valence band edges. Thus, when designing a stable n-type or p-type MOSFET, a suitable combination of 2D semiconductor and oxide needs to be selected. In this context, a recent study has suggested that Fermi-level pinning in MoS\(_2\) is weaker if the oxide defect bands can be avoided. It was observed that the degree of Fermi-level pinning is reduced when using $\text{Al}_2\text{O}_3$, which possesses no oxide defect band in the vicinity of the valence band edge of MoS\(_2\), instead of $\text{SiO}_2$ in back-gated FETs\(^1\).

The physical possibilities for tuning the stability in the context of stability-aware device design are illustrated in Fig. 1c–d. By doping the graphene layer, graphene’s $E_F$ can be tuned within the entire grey-shaded area (Fig. 1c). Thus, the design freedom for a stability-based device is large in graphene FETs; furthermore, the role of $\text{SiO}_2$ defect bands can be reduced with an $E_F$ alignment in the middle of the two defect bands, whereas the impact of the $\text{Al}_2\text{O}_3$ defect band can be minimized when using p-doped graphene layers. For 2D semiconductors like WS\(_2\), the freedom for stability-aware design is smaller. Fig. 1d shows that either the conduction or valence band edge can be chosen via doping. However, n-type WS\(_2\) presumably will be electrically unstable for the amorphous oxides investigated here, whereas stable p-type FETs could be designed using $\text{Al}_2\text{O}_3$ or $\text{HfO}_2$.

It is worth noting that several studies have reported high densities of fixed charges at the interfaces of 2D materials with amorphous oxides, for example, MoS\(_2)/\text{SiO}_2$ (refs. \(^2,3\)), WS\(_2)/\text{SiO}_2$ (ref. \(^3\)) or graphene/$\text{SiO}_2$ (ref. \(^4\)). This evidence suggests that there might be a loss of charge neutrality at the ill-defined interfaces between van der Waals–bonded 2D layers and amorphous oxides, causing deviations from the Schottky–Mott rule\(^2\). These deviations result in offsets to the band alignments that can be determined, for example, with internal photoemission measurements\(^1\) or scanning probe techniques\(^1\). Although these offsets would need to be taken into account for optimum matching of the Fermi level at a maximum distance to the oxide defect bands, they are neglected for the proof-of-concept study presented here.

At the same time, the intentional placement of charges at the interface could be used to shift the band edges away from the oxide defect bands using, for example, surface charge transfer doping\(^4\). However, fixed charges at the interfaces would also degrade the mobility in the semiconducting 2D channel\(^5\). This could be avoided
by using more complex gate stacks with electric dipoles at the interfaces between different oxides. Such a dipole engineering approach has been successfully used to improve the reliability of silicon FETs with an HfO2/SiO2 gate stack21,44.

To estimate the electrical stability improvement that can be achieved by Fermi-level tuning in FETs with amorphous oxides, we simulated the hysteresis width in FETs based on 2D semiconductors in relation to the location of the conduction band edge, $E_{\text{CB}}$. For simulations, we used the previously developed drift-diffusion-based TCAD methodology45 coupled to a non-radiative multiphonon model43 (Supplementary Section 1). In Fig. 2, we calculated the hysteresis width in a model system of monolayer MoS2 with a back-gate oxide of SiO2 (ref. 45). We evaluated the hysteresis width as a function of varying distance of the trap level $E_T$ to $E_{\text{CB}}$.

For an oxide defect-band width of $\sigma_{E_T} = 0.3$ eV, the hysteresis width can be reduced by half an order of magnitude if the conduction band edge is shifted 350 meV downwards, as illustrated in Fig. 2a. In graphically represented forms: for Graphene FETs (a), 2D semiconductor FETs (b), and single-layer WS2, bilayer WS2, and bulk WS2 (c), the number of layers modifies the bandgap and doping determines whether electrons or holes will be the majority carriers and thus govern device stability.

In Fig. 1, Fermi-level tuning to maximize the energetic distance to oxide defect bands. a, Schematic (left) shows a top-gated GFET with an Al2O3 gate oxide. For a cut through the GFET along the indicated arrow, the energetic alignment of the Fermi level to the defect band in the aluminium gate oxide is shown. In the band diagram (left), the device is electrically unstable with respect to variations in the threshold voltage as the Fermi level is aligned within the defect band. In the band diagram (right), the Fermi level has been shifted downwards, rendering the device more stable. b, Schematic of the charge transfer of electrons flowing through the WS2 channel to traps in the HfO2 gate oxide (left). This situation is depicted in the left band diagram where the Fermi level is aligned close to the conduction band edge, rendering the device unstable. If the Fermi level is instead aligned close to the valence band edge, the FET is stable. c, In this band diagram, the possible range of the graphene Fermi levels, which is currently achievable by doping, is shown as a grey-shaded region. The Fermi level can be continuously tuned within this region. d, Injection of electrons and holes from the band edges of WS2. In a layered semiconductor, the number of layers modifies the bandgap and doping determines whether electrons or holes will be the majority carriers and thus govern device stability.
in the band diagrams in Fig. 2c. These shifts in the conduction or valence band edges can be achieved, for example, by transitioning from monolayers to bulk materials (Fig. 1d). For example, in WS₂, the conduction and valence band edges shift by approximately 160 meV when using bilayers instead of monolayers, or by about 370 meV when using bulk WS₂ (ref. 46). Thus, we would expect that n-type characteristics with those of Type 2 graphene (Fig. 3d), it is expected that the higher quality of the graphene channel leads to higher currents. Based on two-probe measurements of the I_D-V_G characteristics, we estimate the field-effect mobilities to reach up to 5,000 cm²/V·s in Type 1 GFETs, four times the average mobility of about 600 cm²/V·s in Type 2 GFETs. These results are expected based on the Raman analysis and originate from the higher amount of defects in Type 2 graphene.

To test the functionality and performance of our GFETs, the output (I_D-V_G) and transfer (I_D-V_T) characteristics are shown for a representative Type 1 GFET (Fig. 3b, c). We observe ambipolar device operation with kinks in the output characteristics at higher V_D, features typical for GFETs(47). This local saturation of the output characteristics has been linked to a pinch-off region in the monolayer graphene channel, where the majority charge type changes and the charge concentration declines locally(27). When we compare these characteristics with those of Type 2 graphene FETs (Fig. 3d), it is evident that the higher quality of Type 1 graphene leads to higher current densities. Based on two-probe measurements of the I_D-V_G characteristics, we estimate the field-effect mobilities to reach up to 5,000 cm²/V·s in Type 1 GFETs, four times the average mobility of about 600 cm²/V·s in Type 2 GFETs. These results are expected based on the Raman analysis and originate from the higher amount of defects in Type 2 graphene.

Negatively charged dopants in Type 2 lead to higher variability and shift V_D, towards more positive voltages, as evident from the comparison of V_D measured on 50 devices for each graphene type (Fig. 3c). More details on the variability of the two types of GFET studied here are provided in Extended Data Fig. 4 and Supplementary Section 5. A more positive V_D corresponds to a higher p doping concentration within the graphene channel.

Graphene Fermi level and Al₂O₃ defect bands
To test our proposed stability-based design, we fabricated two batches of GFETs using graphene samples with different doping levels, termed as Type 1 graphene and Type 2 graphene. In addition, we fabricated GFETs with a double-gated structure where the back gate can be used to electrostatically dope the graphene channel(47,48). In the first two batches, graphene monolayers form a channel with an area of W×L=100 μm×160 μm on top of mechanically flexible polyimide (PI) substrates(49). In the top-gated device layout, a 40-nm-thick amorphous Al₂O₃ layer, grown by atomic layer deposition, is used as the gate oxide. The two fabricated GFET batches using Type 1 and Type 2 graphene mainly differ in the respective doping and quality of their graphene channels. These graphene layers were purchased from different vendors using different parameters for the chemical vapour deposition (CVD) process and layer transfer. Type 1 graphene exhibits a work function that results in a small distance of E_F to the Al₂O₃ trap band (ET). According to our theory, this small value of ET - E_F predicts electrically unstable devices. In contrast, Type 2 graphene is p doped with a higher distance of E_F to ET, predicting electrically more stable FETs. Furthermore, the graphene films have vastly differing qualities, with Type 2 graphene exhibiting a higher concentration of defects (Extended Data Fig. 3 and Supplementary Section 4 show the respective Raman spectra). Although we anticipate that a higher defect concentration would lead to an overall degraded GFET performance, if our hypothesis is correct, the p doping of Type 2 devices should nevertheless lead to more stable devices due to the larger distance of E_F from the defect band.
Fig. 3 | GFET design and performance. a, Schematic showing the cross section (left), and the optical microscopy image shows the top view of the device layout (right). S, source; D, drain. b,c, Output ($I_D$-$V_D$) characteristics of a representative device of Type 1 (b) and Type 2 (c) and transfer ($I_D$-$V_G$) characteristics (c). Type 2 GFETs have the same layout as Type 1 GFETs, but are based on a different CVD-grown graphene layer from another vendor. d, Transfer ($I_D$-$V_G$) characteristics of a representative device based on Type 2 graphene. Here only the forward sweeps are shown; the backward sweeps are reported in Fig. 5. e, Mean current and voltage at the Dirac point are compared for the Type 1 and Type 2 devices ($V_{D_{\text{Dirac}}}$, and $V_{D_{\text{Dirac,T2}}}$, respectively). These values were calculated from the transfer characteristics measured on 50 different GFETs of every type using $V_{DS} = 0.1\,V$, with every single measurement value given as a small dot. The large dots show the mean value and the bars denote the error bars, giving an error of 1σ. f, Cross section through the GFETs with a silicon wafer as the global back gate. g,h, For these double-gated GFETs, $I_D$-$V_{DS}$ curves recorded at $t_{sw} = 0.4\,s$ are shown for $V_{SS} = 20\,V$ (g) and $V_{SS} = -20\,V$ (h) including the backward sweep (dashed lines).

of the sample and correlates with a higher work function ($E_w$)\(^{34}\). Pristine graphene has a work function of 4.56\,eV (ref. 50), which is shifted towards higher values by p doping\(^{34}\) and towards smaller values by n doping\(^{33,35}\). To calculate the Fermi-level location in the two graphene types, we obtain the charge-carrier concentration ($n$) based on the analytic expression for $n$ in the MOS capacitor\(^{33,35}\). At a top-gate bias of 0\,V, we extract the charge-carrier concentration ($n$) caused by the intrinsic doping of graphene samples

$$n(V_{TG}) = \frac{C_{tot}}{q} |V_{TG} - V_{Dirac}|,$$

with the total gate capacitance of the structure ($C_{tot}$) and elementary charge $q$. Here, $C_{tot}$ is given by the capacitance of Al$_2$O$_3$ ($C_{ox}$) in series with the capacitance of 0.5\,nm van der Waals gap ($C_{vdW}$) and the quantum capacitance of graphene\(^{32}\) ($C_q$), amounting to $C_{tot}$ = 0.16\,µF\,cm$^{-2}$. This expression gives a p-doping density for Type 1 graphene of $n_p = 5.5 \times 10^{12}$ cm$^{-2}$ and for Type 2 graphene of $n_p = 2.8 \times 10^{12}$ cm$^{-2}$. Thus, Type 2 graphene is more p doped by an additional doping density of approximately 2.75 \times 10^{12} cm$^{-2}$. These hole densities in the graphene layers at 0\,V gate voltage determine the work function via\(^{33,32}\)

$$E_w = h \nu_F \sqrt{\pi n},$$

where the Fermi velocity in graphene is $\nu_F = 1.1 \times 10^6$ m s$^{-1}$ (ref. 33). Consequently, we obtain $E_w$ of Type 1 graphene to be 4.6\,eV and $E_w$ of Type 2 graphene to be 4.8\,eV, that is 0.2\,eV higher
(Supplementary Section 6 shows the calculation of the work function.) For all the typical FET metrics, Type 2 graphene suggests poorer performance, including lower mobility and lower ON/OFF ratio. However, because $E_{\text{W}}$ is higher than $E_{\text{W}}$, our stability-based design theory suggests that Type 2 graphene should produce more stable GFETs, which is what we set out to prove below.

To further analyse our model system, we fabricated devices with Type 1 graphene but using thermal SiO$_2$ on silicon and quartz substrates instead of a flexible PI layer. In addition, the quality of the interface between graphene and Al$_2$O$_3$ was modified by transferring single-layer CVD-grown hBN layers before the ALD deposition or by sputtering ~2-nm-thick aluminium as a seed layer for the Al$_2$O$_3$ growth process. As shown in Extended Data Fig. 5 and Supplementary Section 7, the substrate primarily impacts the maximum current density, whereas the quality of the interface with Al$_2$O$_3$ impacts device stability.

Furthermore, we fabricated double-gated GFETs using 90 nm SiO$_2$ as a back-gate oxide and the silicon wafer as a global back gate (Fig. 3f). This configuration allows electrostatic control of the doping of the monolayer graphene channel via the back gate$^{48}$. By applying a positive voltage at the back gate of, for example, 20 V (Fig. 3g), the Dirac voltage of the top gate is shifted towards more negative voltages, corresponding to a smaller work function of graphene. Conversely, $V_{\text{BG}} = -20$ V makes $V_{\text{Dirac}}$ of the top gate more positive and results in a higher graphene work function (Fig. 3h). Consequently, these devices are expected to be more electrically stable at higher negative $V_{\text{BG}}$ than at higher positive $V_{\text{BG}}$, as shown below.

To accurately determine the alignment of $E_F$ in graphene to the electron-trapping band of the amorphous Al$_2$O$_3$ gate oxide at $E_F$, knowing the precise location of the oxide defect band is essential. Several studies have investigated the alignment of this defect band using trap spectroscopy by charge injection and sensing (TSCS)$^{10,11}$, BTI$^{10,11}$ and hysteresis measurements$^{17}$. The defect band alignments of Al$_2$O$_3$ as obtained from the literature are shown in Fig. 4a, with the corresponding parameters listed in Supplementary Section 8. Based on density functional theory (DFT) calculations, this defect band can be associated with either oxygen vacancies$^{10}$ or aluminium interstitials$^{10}$. For our study, we use a normally distributed defect band with the mean defect level at $E_F - E_F = 2.15 \pm 0.30$ eV below the conduction band edge of Al$_2$O$_3$. The electron affinity ($\chi$) of Al$_2$O$_3$, which determines the location of the conduction band edge, varies in the literature. Here we use 1.96 eV as obtained from internal photoemission measurements$^{44}$. For all the measurement ranges used in our work, we only probe the lower part of a potentially wider defect band further up, as reported using other methods$^{35}$. This is illustrated in Fig. 4b, where the regions that can be probed by measurements are shaded in red and yellow. These shaded regions reach the upper edge of the defect band used here, but cover only the lower part of the wider defect band reported elsewhere$^{35}$. For Type 1 graphene, $E_F$ is aligned within the defect band (small $E_F - E_F$, electrically unstable) (Fig. 4c), whereas for Type 2 graphene, it is aligned below the defect band (high $E_F - E_F$, electrically stable) (Fig. 4d).

Below, we discuss that as proposed above, the 200 meV downward shift of the Fermi level of Type 2 graphene is sufficient to make the $V_{\text{Dirac}}$ value of these GFETs more electrically stable.

**Hysteresis dynamics of GFETs**

We first compare the double-sweep transfer characteristics for a small voltage range of $[-5, 5$ V$]$ on five GFETs based on Type 1 graphene (Fig. 5a). We note little variability, which is confirmed when studying the hysteresis width $\Delta V_{\text{BG}}$ as a function of the inverse sweep time ($t_{\text{sw}}$), namely, the sweep frequency ($f = 1/t_{\text{sw}}$). In Fig. 5b, the hysteresis width as a function of the sweep frequency is shown for five GFETs based on Type 1 graphene and five GFETs based on Type 2 graphene. Type 2 devices show a considerably higher variability of $\Delta V_{\text{BG}}$ than Type 1 devices, which is linked to the increased variability of $V_{\text{Dirac}}$. On Type 2 (Fig. 5e), the hysteresis is higher; for both types, the largest hysteresis is observed for the slowest sweeps as the largest number of oxide defects can change their charge state$^{21}$. Since the observed hysteresis critically depends on the voltage ranges used for the gate-voltage sweeps, we compare the bias ranges used with ranges for various applications (Supplementary Section 9), concluding that the gate-oxide fields investigated here are standard operating conditions for radio-frequency applications.

An increased bias range of $[-10, 10$ V$]$ increases the hysteresis, because more oxide defects become accessible for charge transfer (Fig. 5c) for the representative Type 1 and Type 2 GFETs. To shed more light on this behaviour, the dynamics of the Dirac voltage shifts are analysed as a function of the sweep frequency (Fig. 5c). For the $[-5, 5$ V$]$ sweep, $V_{\text{Dirac,up}}$ and $V_{\text{Dirac,down}}$ as a function of the sweep frequency show similar slopes for both types. However, for the 10 V sweep range and Type 1 GFET, $V_{\text{Dirac,up}}$ is shifted to more negative voltages in slow sweeps, whereas $V_{\text{Dirac,down}}$ is shifted to more positive voltages. This indicates that for large sweep ranges on Type 1 GFETs, a large amount of electrons are emitted from the oxide traps between $-10$ V and $V_{\text{Dirac,up}}$ whereas for Type 2 GFETs, charge trapping can be neglected in this interval. This reversed drift of $V_{\text{Dirac,up}}$ to more negative voltages at slower sweeps results in an increase in the hysteresis width in Type 1 GFETs (Fig. 5c). The increased hysteresis at large sweep ranges for Type 1 GFETs confirms our hypothesis that as the $E_F$ value of Type 1 GFET is located closer to the Al$_2$O$_3$ defect band, the GFETs are electrically less stable.

The band alignments shown in Fig. 4c,d qualitatively explain the larger hysteresis in Type 1 GFETs compared with Type 2: in Type 1 GFETs biased at $V_{\text{time}}$, a considerable number of defects are negatively charged. If a negative voltage is applied, these defects discharge due to band bending, and thus, $V_{\text{Dirac}}$ is shifted to more negative voltages during a slow up-sweep (Fig. 5c). In contrast, in Type 2 GFETs, the Fermi level is located below the defect band at $V_{\text{Dirac}}$, as its Fermi level has been shifted down by 200 meV via p-doping. Thus, most defects are neutral at the Dirac voltage. If a long time is spent with the GFET biased at negative voltages, the charge states do not change and the location of $V_{\text{Dirac}}$ during the up-sweep is stable, independent of the sweep time.

In summary, the higher $E_F - E_F$ of Type 2 graphene with respect to the Al$_2$O$_3$ defect band leads to a smaller hysteresis width for large sweep ranges. At small gate-bias ranges and fast hysteresis sweeps, Type 2 devices suffer from more charge trapping at the defective interface with the Al$_2$O$_3$ insulator, and the hysteresis is similar or even higher in Type 2 devices compared with Type 1 devices (Fig. 5b, Extended Data Fig. 6 and Supplementary Section 10). For fast sweeps, fast traps at the defective interface in Type 2 GFETs increase the hysteresis, giving the impression of a frequency-independent hysteresis width (Fig. 5c). Type 1 GFETs exhibit a cleaner interface but a smaller $E_F - E_F$ with respect to Al$_2$O$_3$ defects, strongly degrading the GFETs during slow sweeps. For high gate-bias ranges and slow sweeps, the border traps of Al$_2$O$_3$ dominate the device stability, thus more stable operation of Type 2 GFETs is observed.

In the double-gated configuration, the graphene layer can be dynamically doped in situ (Fig. 3f). To determine the impact of electrostatic back-gate doping on the top-gate stability, we characterized the hysteresis in the top-gate $I_{\text{DS}}$ ($V_{\text{GS}}$) curves after biasing the devices at a static $V_{\text{BG}}$. Subsequently, the top-gate hysteresis was measured at different sweep rates. In Fig. 5e, the hysteresis at the top gate is shown for slow sweeps and various back-gate voltages from 12 V down to $-40$ V. When comparing the hysteresis widths as a function of the sweep time and the applied back-gate voltage (Fig. 5f), two trends are clearly observed. First, the hysteresis is reduced for fast sweeps; second, the hysteresis is the smallest for the most negative $V_{\text{BG}}$. It is expected that hysteresis can be reduced for high
The work function was calculated based on the measured $V_{\text{BG}}$ for the charging and discharging of defects in $\text{Al}_2\text{O}_3$ for Type 1 graphene with a work function of $4.6\text{ eV}$. A value that can be qualitatively reached also with $V_{\text{BG}} = 20\text{ V}$. An improvement of a factor of up to 4.5 is observed for a work-function shift of 340 meV, as shown in the corresponding comparison of the work function for these measurements (Fig. 5i). Thus, we observe an improvement of about 750 meV $\text{dec}^{-1}$ when more negative back-gate voltages are applied, in good agreement with the theoretical results (Fig. 2b). However, in this double-gated configuration, full improvement cannot be achieved in every measurement round; in particular, for high...
Hysteresis in the transfer characteristics of GFETs. a, Hysteresis in the transfer characteristic measured on five different Type 1 GFETs, illustrating the variability of the devices. b, Hysteresis width as a function of 1/t_{SW} is shown for five different devices for each graphene type. The circles and triangles are used to represent Type 1 and Type 2 GFETs, respectively, whereas the solid and dashed lines are guides to the eye for Type 1 and Type 2 GFETs, respectively. c, Hysteresis width for Type 1 and Type 2 GFETs is shown as measured on one representative GFET per type. d, Dirac-point shifts of the up and down sweeps are shown with empty/full symbols for V_{Dirac,up}/V_{Dirac,down}, respectively. e, f, For double-gated GFETs, the I_{D}-V_{G} curves at slow sweeps are compared for two different V_{BG} values (e) with the respective hysteresis widths as a function of the inverse sweep time (f). g, Extent of doping the GFET as a function of the back gate voltage, for various sweep times, based on V_{Dirac} and equations (1) and (2). h, Relative change in the hysteresis width for the slowest sweeps is shown for different measurement rounds on two GFETs (D1 and D2) at varying V_{BG} values, illustrating that the hysteresis width increases for higher V_{BG}. i, Respective effective electrostatic doping for the measurement rounds on D1 and D2.

\( V_{BG} \) a strong modulation of the work function by the back gate is hindered by the charging of oxide traps in SiO_{2}. Nevertheless, all the hysteresis measurements show that a shift in the graphene work function to higher values, away from the defect band in AlO_{x}, successfully reduces the amount of electrically active border traps, thereby stabilizing the GFETs.

**Stability under static gate bias**

To evaluate the long-term stability of GFETs, we analysed the Dirac-voltage shifts (\( \Delta V_{Dirac} \)) after static elevated gate voltages (V_{G(high)}) were applied for varying charging times (t_charging). We record the magnitude of the initial \( \Delta V_{Dirac} \) shift and monitor the recovery after the increased gate-biasing period with fast I_{D} (V_{G}) sweeps at logarithmically spaced recovery times. In Fig. 6a, the fast I_{D} (V_{G}) sweeps recorded during the recovery from negative gate biasing (negative-bias temperature instability (NBTI)) at –10 V are shown. Such BTI measurements give a complementary perspective on the long-term stability and reliability of FETs compared with the hysteresis measurements discussed earlier. Although during hysteresis measurements, GFETs are subjected to slow up and down gate-voltage sweeps, during a BTI measurement, an elevated gate bias is applied for a certain charging time and the recovery of the Dirac point is recorded. With this well-established measurement scheme, the impact of border traps is studied\(^{12,13}\). Thus, in a BTI measurement, the observed hysteresis during the probing sweeps is small and not in focus. To avoid measurement artefacts coming
from fast traps causing the hysteresis in the probing $I_D (V_G)$ curves, the down-sweep $I_D (V_G)$ curves are used to evaluate the $V_{Dirac}$ shifts for all NBTI measurements and the up-sweep $I_D (V_G)$ curves for positive gate biasing (positive-bias temperature instability (PBTI)) (Methods and Extended Data Fig. 8).

NBTI measured by subjecting the devices to a gate bias of $-10$ V for increasingly long charging times is shown for Type 1 GFETs (Fig. 6b) and for Type 2 GFETs (Fig. 6c). As planned, the $V_{Dirac}$ shifts are smaller on Type 2 devices than on Type 1 devices. GFETs based on Type 2 graphene are more stable with respect to long-term degradation because the graphene $E_F$ is further away from the Al2O3 defect band (Fig. 4d). Therefore, on Type 2 GFETs, fewer oxide traps change their charge state during negative gate biasing, resulting in smaller shifts in $V_{Dirac}$, which also recover faster as the traps that emit electrons are located closer to the interface and thus have smaller time constants. Extended Data Fig. 9 shows the recovery traces of NBTI at $-5$ V. For Type 2 GFETs, slight over-recovery\textsuperscript{13} is observed for the shortest charging time of 1 s (Supplementary Section 12). This over-recovery is also visible for the fast $I_D (V_G)$ sweeps used for the BTI evaluation of Type 2 GFETs (Extended Data Fig. 10). In Fig. 6d, the fast $I_D (V_G)$ sweeps measured after a positive bias at 10 V are shown, together with the corresponding recovery traces for Type 1 GFETs (Fig. 6e) and Type 2 GFETs (Fig. 6f). For both device types, degradation on applying positive biases (PBTI) are higher than NBTI shifts, as the Fermi level in graphene is at the lower edge of the Al2O3 defect band (Fig. 4c). Thus, the number of defects that become more negatively charged during a positive bias is larger than the number of defects that emit one of their electrons during a negative bias. As Type 2 graphene is more p doped, $E_F$ is located further away from the Al2O3 defect band, ultimately reducing the amount of charge trapping without the need to modify the insulator or reduce the total number of traps.

Interestingly, throughout the charging times, the shifts on Type 1 devices do not recover, whereas the shifts on Type 2 devices show complete recovery, even for a short charging time of 1 s. This observation was confirmed when subjecting the devices to a smaller gate-bias voltage of 5 V (Extended Data Fig. 9). We hypothesize the active creation of defects in Al2O3 to explain the permanent component of BTI degradation in Type 1 GFETs. In silicon FETs using SiO2 as a gate dielectric, the permanent component of BTI has been associated with gate-sided hydrogen release\textsuperscript{16}. We speculate that a similar mechanism of bias-facilitated oxide defect creation in Al2O3 is responsible for the permanent PBTI observed for our GFETs, which will need to be investigated by future studies.

**Conclusions**

We have reported an approach to improve the electrical stability of FETs based on 2D materials. Charge trapping at the border traps in amorphous oxides is the principal cause of the threshold-voltage drifts and reduced long-term stability in 2D FETs. Therefore, the impact of defect bands in amorphous gate oxides can be reduced by tuning the energy alignment of the Fermi level. We demonstrate our approach using GFETs with Al2O3 as the top-gate oxide and two different types of graphene, which differ in their doping and Fermi-level alignments based on their respective fabrication methods. Our measurements show that the GFETs, which are based on
the more p-doped Type 2 graphene with a higher \((E_p - E_h)\), have a smaller hysteresis and increased stability of their Dirac voltage when subject to prolonged elevated gate biases. Furthermore, by electrostatic doping of the graphene channel via a back gate, the hysteresis width can be reduced by a factor of up to 4.5. These results suggest that more stable and reliable 2D-material-based FETs using common amorphous gate oxides can be built by minimizing the impact of defect bands in the gate oxides during design.

In 2D semiconductors, the design options mainly consist of choosing suitable materials depending on n or p doping, or varying the thickness of the channel material. There is more design freedom with graphene, as the graphene Fermi level can be tuned over a range of up to 2 eV. Moreover, our approach to improve stability may be universally applicable to other insulators, such as crystalline insulators, where the impact of narrow insulator-defect bands can be reduced further than in amorphous oxides. However, future studies will be necessary to clarify what levels of stability can be achieved by Fermi-level tuning in systems based on amorphous oxides and crystalline insulators. In addition, the stability-based design approach relies on prior knowledge about the energy location of the defect bands in the oxide, which at the moment is incomplete.

**Methods**

**Device fabrication.** Our top-gated GFETs were fabricated on spin-coated PI substrates using photolithography. First, the flexible substrate was prepared by spin coating PI in the liquid form on a Si wafer and subsequently curing the layer. The thickness of the solidified PI film was about 8 µm. During the fabrication process, a rigid Si substrate was used as a support layer. In the next step, a CVD-grown graphene layer was transferred to the PI substrate. We study two batches of GFETs where the channel is formed by graphene samples purchased from different vendors, namely, vendor 1 (Type 1) and vendor 2 (Type 2). For Type 1 devices, CVD graphene was transferred from the copper growth substrate using a polymethyl methacrylate (PMMA)-assisted wet transfer method; for Type 2 GFETs, the transfer was performed by vendor 2. The Type 1 graphene flake covered an area of 2 × 2 cm² and was of higher quality than the Type 2 flake (which covered a six-inch wafer). The different qualities of the graphene layer were confirmed by Raman spectroscopy (Extended Data Fig. 3 and Supplementary Section 4). The graphene layer was patterned in an oxygen-plasma etch step to form channels with length \((L)\) of 160 µm and width \((W)\) of 100 µm. In the next step, the source and drain contacts were deposited by sputtering 50 nm Ni, followed by a lift-off process. This step was followed by growing 40 nm Al₂O₃, with atomic layer deposition (ALD) on top of the devices to form the gate oxide in a top-gated configuration. To finalize the GFETs, the top-gate electrode was fabricated by sputtering 10 nm Ti and 150 nm Al and patterned in a lift-off process. To be able to contact the source and drain pads, vias were opened through the Al₂O₃ with a wet-buffered oxide etchant. For our device and GFETs, we suggested in our previous work, we expressed the BTI degradation/recovery magnitude using a field-effect mobility of the GFETs and found it to be 4.000 cm² V⁻¹ s⁻¹ for Type 1 graphene and 1,000 cm² V⁻¹ s⁻¹ for Type 2 graphene. The Hall mobility of both the samples was found to be slightly higher. The hysteresis was analysed by measuring the double-sweep \(I_F-V_G\) characteristics using different sweep times \(t_{sweep}\) and sweep ranges of \(V_{min}\) and \(V_{max}\). The hysteresis width \(ΔV_{hyst}\) was extracted as the difference between the forward- and reverse-sweep \(V_{max}\) value. As suggested in our previous work, we suggested in our previous work, we expressed the hysteresis dynamics using \(ΔV_{hyst}(1/t_{rel})\) traces. Finally, the BTI degradation/recovery dynamics were analysed using subsequent degradation/recovery rounds with either fixed stress time \(t_{stress}\) and increasing high-voltage levels \(V_{max}\), or fixed \(V_{max}\) and increasing \(t_{stress}\). During the recovery period, we applied a constant recovery voltage of \(V_{rec} = 1\) V between the sweeps. This voltage is chosen to be close to the charge-carrier equilibrium at \(V_{min}\). To avoid artefacts from fast traps charged during the sweep, the down-sweep \(I_F-V_G\) curve is used to monitor the recovery of NBTI. The characteristics obtained when using up-sweeps to measure the NBTI recovery are shown in Extended Data Fig. 8. For PTBTI measurements, the record of the up-sweep minimizes artefacts; thus, we used \(I_F-V_G\) to measure the NBTI degradation magnitude using a Dirac-point voltage shift \(ΔV_{min}\) and plotted it versus the relaxation time \(t_{rel}\). To gain more statistics, all our measurements were repeated on several devices.

**Data availability**

The data that support the findings of this study are available from the corresponding author upon reasonable request.

**Code availability**

For the calculations of the hysteresis width depending on the defect band alignment, simulations of the transfer characteristics of GFETs and calculations of charge trapping in the oxide defect bands, we used GTS Minimos-NT (https://www.globalcad.com/products/gts-minimos-nt/) and the implementation of non-native multiphonon model therein. For educational purposes and academic research, this software can be used free of charge via an online Web interface (https://www.globalcad.com/simonline/). For the central conclusions relevant to this paper, the simulations could be performed using the Comphy code, which is publicly available from https://comphy.eu/ (ref 2).
25. Afanas'ev, V. V. et al. Band alignment at interfaces of two-dimensional materials: internal photoemission analysis. J. Phys.: Condens. Matter 32, 413002 (2020).
26. Raza, G. et al. Comphy—a compact-physics framework for unified modeling of BTI. Microelectron. Reliab. 85, 49–65 (2018).
27. Shluger, A. Defects in Oxides in Electronic Devices. In: Andreadis W., Yip S. (eds) Handbook of Materials Modeling 1013–1034 (Springer, 2020).
28. Degraeve, R. et al. Trap spectroscopy by charge injection and sensing (TSCIS): a quantitative electrical technique for studying defects in dielectric stack. In 2008 IEEE International Electron Devices Meeting 1–4 (IEEE, 2008).
29. Nagumo, T., Takeuchi, K., Hase, T. & Hayashi, Y. Statistical characterization of trap position, energy, amplitude and time constants by RTN measurement of multiple individual traps. In 2010 International Electronic Devices Meeting 28.1.1–28.3.4 (IEEE, 2010).
30. Xia, M., Martin, I., Yablonskii, E. & Jiang, H. W. Electrical detection of the spin resonance of a single electron in a silicon field-effect transistor. Nature 430, 435–439 (2004).
31. Muñoz Ramo, D., Gavartin, J. L., Shluger, A. L. & Bersuker, G. Spectroscopic properties of oxygen vacancies in monoclinic HfO2 calculated with density functional theory. Phys. Rev. B 75, 205336 (2007).
32. Grasser, T. et al. On the microscopic structure of hole traps in pMOSFETs. In 2014 IEEE International Electron Devices Meeting 21.1.1–21.1.4 (IEEE, 2014).
33. Park, J. et al. Work-function engineering of graphene electrodes by self-assembled monolayers for high-performance organic field-effect transistors. J. Phys. Chem. Lett. 2, 841–845 (2011).
34. Shi, Y. et al. Work function engineering of graphene electrode via chemical doping. ACS Nano 4, 2689–2694 (2010).
35. Kwon, K. C., Choi, K. S., Kim, B. J., Lee, J. L. & Kim, S. Y. Work-function decrease of graphene sheet using alkali metal carbonates. J. Phys. Chem. C 116, 26586–26591 (2012).
36. Wittmann, S. et al. Electric surface charge engineering for electrostatic doping of graphene. ACS Appl. Electron. Mater. 2, 1235–1242 (2020).
37. Mooltheri, V. et al. Understanding ambipolar transport in MoS2 field effect transistors: the substrate is the key. Nanotechnology 32, 135202 (2021).
38. Takenaka, M., Ozawa, Y., Han, J. & Takagi, S. Quantitative evaluation of energy distribution of interface trap density at MoS2 MOS interfaces by the Terman method. In 2016 IEEE International Electron Devices Meeting 5.8.1–5.8.4 (IEEE, 2016).
39. Chiappe, D. et al. Controlled sulfurization process for the synthesis of large area MoS2 films and MoS2/WSe2 heterostructures. Adv. Mater. Interfaces 3, 1500635 (2016).
40. Trepalin, V. et al. Evaluation of the effective work-function of monolayer graphene on silicon dioxide by internal photoemission spectroscopy. Thin Solid Films 674, 39–43 (2019).
41. Afanas'ev, V. V., Steams, A. & Tsai, W. Determination of interface energy band diagram between (100)Si and mixed Al–H2 oxides using internal photoemission spectroscopy. Appl. Phys. Lett. 82, 245–247 (2003).
42. Zhang, Y. et al. Giant phonon-induced conductance in scanning tunnelling spectroscopy of gate-tunable graphene. Nat. Phys. 4, 627–630 (2008).
43. Pang, C. S. et al. Atomically controlled tunable doping in high-performance WSe2 devices. Adv. Electron Mater. 6, 1901304 (2020).
44. Franco, J. et al. Low thermal budget dual-dipole gate stacks engineered for sufficient BTI reliability in novel integration schemes. In 2019 Electron Devices Technology and Manufacturing Conference 215–217 (IEEE, 2019).
45. Knobloch, T. et al. A physical model for the hysteresis in MoS2 transistors. IEEE J. Electron Devices Soc. 6, 972–978 (2018).
46. Jo, S., Ubrig, N., Berger, H., Kuzmenko, A. B. & Morpurgo, A. F. Mono- and bilayer WS2, light-emitting transistors. Nano Lett. 14, 2019–2025 (2014).
47. Meric, I. et al. Current saturation in zero-bandgap, top-gated graphene field-effect transistors. Nat. Nanotechnol. 3, 654–659 (2008).
48. Yu, Y.-j. et al. Tuning the graphene work function by electric field effect. Nano Lett. 9, 3430–3434 (2009).
49. Wang, Z. et al. Flexible one-dimensional metal–insulator–graphene diode. ACS Appl. Electron. Mater. 1, 945–950 (2019).
50. Yan, R. et al. Determination of graphene work function and graphene-insulator-semiconductor band alignment by internal photoemission spectroscopy. Appl. Phys. Lett. 101, 022105 (2012).
51. Ma, N. & Jena, D. Carrier statistics and quantum capacitance effects on mobility extraction in two-dimensional crystal semiconductor field-effect transistors. 2D Mater. 2, 015003 (2015).
52. Xia, J., Chen, F., Li, J. & Tao, N. Measurement of the quantum capacitance of graphene. Nat. Nanotechnol. 4, 505–509 (2009).
53. Martin, J. et al. Observation of electron–hole puddles in graphene using a scanning single-electron transistor. Nat. Phys. 4, 144–148 (2008).
54. Zahid, M. B. et al. Applying complementary trap characterization technique to crystalline γ-phase-Al2O3 for improved understanding of nonvolatile memory operation and reliability. IEEE Trans. Electron Devices 57, 2907–2916 (2010).
55. Franco, J. et al. Suitability of high-k gate oxides for III–V devices: a PBTI study in In0.53Ga0.47As devices with Al2O3. In 2014 IEEE International Reliability Physics Symposium 6A.1.1–6A.2.6 (IEEE, 2014).
56. Putcha, V. et al. Impact of slow and fast oxide traps on In0.53Ga0.47As device operation studied using CET maps. In 2018 IEEE International Reliability Physics Symposium Proceedings 5A.3.1–5A.3.7 (IEEE, 2018).
57. Dicks, O. A., Cottom, J., Shluger, A. L. & Afanas'ev, V. V. The origin of negative charging in amorphous Al2O3 films: the role of native defects. Nat. Nanotechnol. 30, 205201 (2019).
58. Grasse, T. et al. Gate-sided hydrogen release as the origin of ‘permanent’ NRTI degradation. In 2015 IEEE International Electron Devices Meeting 20.1.1–20.1.4 (IEEE, 2016).
59. Suk, J. W. et al. Transfer of CVD-grown monolayer graphene onto arbitrary substrates. ACS Nano 5, 6916–6924 (2011).

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Author contributions
T.G., M.C.L., T.K., B.U. and Y.Y.I. conceived the study. T.G. and M.C.L. supervised the project. B.U., Z.W. and M.O. fabricated the GFETs under the guidance of D.N. Y.Y.I. and T.K. electrically characterized the GFETs using the equipment developed by M.W. and T.K. performed the TCAD simulations in frequent discussions with L.F, Y.Y.I. and T.G. T.K. prepared the manuscript draft and all the authors commented on the final version of the manuscript.

Competing interests
The authors declare no competing interests.

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Extended Data Fig. 1 | Band alignment of various 2D semiconductors with amorphous oxides. Band diagram showing the band alignment of several monolayer 2D semiconductors to the three most common gate oxides and their respective defect bands. In (a) the band edge alignment of the 2D semiconductors is shown together with the defect bands in three oxides to give an overview over possible combinations. Based on (a) potentially stable combinations of 2D semiconductors with HfO$_2$ are shown in (b), revealing BP as a promising candidate. In (c) the selection for Al$_2$O$_3$ is presented, where HfSe$_2$ or ZrSe$_2$ could maximize the distances of conduction and valence band edges to the defect band.
Extended Data Fig. 2 | TCAD estimate of the stability improvement for insulators with narrow defect bands. For a defect band which is only 0.07 eV wide, the hysteresis can be considerably reduced with Fermi level tuning. Here, a model system of MoS$_2$ and SiO$_2$ with a hypothetical, narrow defect band is used. (a) The hysteresis width $\Delta V_h$ is extracted at the threshold voltage, defined as $E_i$ being located at 50 meV below the conduction band edge, see the bending of the band edges at the top. This corresponds to a constant current criterion of $I_{\text{crit}} = 4.8 \times 10^{-5} \mu A / \mu m$. (b) The hysteresis width $\Delta V_h$ is shown as a function of the distance of the oxide trap level $E_T$ to the MoS$_2$ conduction band edge $E_C$. If $E_C$ is moved 82 meV away from the trap band, the hysteresis width will improve by one order of magnitude. (c) At two different locations of $E_C$, namely at $E_T - E_C = 0.168$ eV in dark blue and 0.25 eV in light blue corresponding to the colors of the dotted lines in (b), the band diagrams of the MoS$_2$/SiO$_2$ system are shown, demonstrating how fewer oxide traps change their charge state if the conduction band edge is shifted down.
Extended Data Fig. 3 | Raman spectroscopy on Type 1 and Type 2 Graphene. In Fig. (a), the median Raman spectra with respect to the intensity ratio I(D)/I(G) are shown for Type 1 and Type 2 Graphene. Fig. (b) shows the distribution of the relative count of ratios I(D)/I(G) for different locations across the surface, showing a more defective tail of locations for Type 2. In Fig. (c) the distribution of the FWHM of the 2D peak of the Raman spectra is compared for both graphene types. Fig. (d) shows a spatial map of the intensity peak ratio I(D)/I(G) calculated from the measured Raman spectra of Type 1 Graphene. In Fig. (e) the same spatial map as recorded on Type 2 Graphene is shown. Both maps cover a representative area of 20 μm × 20 μm, the x and y axis give the location on the sample surface in μm. Fig. (f) shows the spatial map of the FWHM of the 2D peak of the Raman spectra for Type 1 Graphene which can be compared with the same map for Type 2 in Fig. (g).
Extended Data Fig. 4 | Variability of GFETs based on Type 1 and Type 2 Graphene. Here, the full statistics from Fig. 3(e) in the main manuscript are compared to the characteristics of 5 selected devices for each graphene type, selected for the hysteresis and long term stability studies. In (a) the average Dirac point location of the 5 selected devices is compared. Fig. (b) shows the variability of the 5 selected devices of Type 1 in comparison to all 50 devices of Type 1 and Fig. (c) shows the equivalent comparison for Type 2 devices. In Fig. (d), the full transfer characteristics of 30 Type 1 GFETs are compared to the transfer characteristics of the 5 selected Type 1 GFETs and in Fig. (e) the comparison for Type 2 GFETs is shown.
Extended Data Fig. 5 | Impact of the substrate choice and the gate oxide to channel interface on the hysteresis. The impact of the variation of the substrate from flexible polyimide to SiO₂ grown on Si, to quartz wafers is studied. For the devices on quartz in one batch a single layer of hBN was used as an interlayer between graphene and Al₂O₃, see the overview in (a). In (b) the hysteresis in the \( I_D-V_G \) on various substrates is compared. In (c) the curves are shifted by their respective Dirac point (\( I_D - (V_G - V_{Dirac}) \)) to allow for a better comparison of the overdrive current, the currents at a certain overdrive voltage above the Dirac point. Three measurements of every device type are shown. In (d) the currents at fixed overdrive voltages and hysteresis widths are compared for three measurements on every device type. In (e) the dependence of the hysteresis width on the sweep time for the different substrates is shown. Fig. (f) shows the impact of the seed layer for the growth of the Al₂O₃ top gate insulator. As the quality of the seed layer varies substantially across the wafer, measurements were repeated for different devices at different locations across the wafer, represented by A, B, C and D. In (g) the hysteresis widths on the GFETs with seed layer are compared to a GFET without seed layer.
Extended Data Fig. 6 | Hysteresis in Type 1 and Type 2 GFETs for varying devices and sweep ranges. In (a) the hysteresis on devices with two different graphene types is compared for the sweep voltage range of [-5V, 5V]. The same hysteresis comparison for a larger sweep voltage range of [-10V, 10V] is shown in (b). The hysteresis as measured on two different devices of Type 1 and Type 2 for the same large sweep voltage range of [-10V, 10V] is given in (c). On the devices where the characteristics are shown in (c) the hysteresis width as a function of different sweep voltage ranges and sweep times are compared in (d).
Extended Data Fig. 7 | Hysteresis in the transfer characteristics of double gated GFETs. In (a) the $I_D(V_{TG})$ curves for top gate sweeps within $\pm 5\, \text{V}$ are shown for $V_{BG}$ varying between 6 V in the first measurement and -20 V in the last measurement on GFET D2 in round (1). In (b) the hysteresis width for this measurement round (D2(1)) for varying sweep times is shown and in (c) the work function shift as a function of the applied back gate voltage is compared for all the sweep frequencies. In Fig. (d), the measurement round (2) on D1 with $V_{TG} \in \pm 5\, \text{V}$ and $V_{BG} \in [-20\, \text{V}, 20\, \text{V}]$ is shown at the slowest sweep time and the hysteresis width for varying $t_{SW}$ is shown in (e). Figs. (f) and (g) show similar graphs for the measurement round (1) on D1 with $V_{BG} \in [-20\, \text{V}, 5\, \text{V}]$. Fig. (h) shows the absolute hysteresis width for different measurement rounds as a function of $V_{BG}$ and Fig. (i) shows the dependence of $V_{Dirac}$ on $V_{BG}$ which is used to calculate $E_W$. 
Extended Data Fig. 8 | NBTI evaluation using up-sweeps. In (a) the degradation on Type 2 devices is compared when evaluated using up sweeps in comparison to down sweeps. In (b) it can be seen that when using up sweeps for the evaluation of NBTI degradation a fast trapping component is active which also increases the over-recovery towards more positive Dirac voltages.
Extended Data Fig. 9 | BTI for a reduced high gate bias level of 5V. In (a) the fast sweep $I_D(V_G)$ curves after negative bias at -5V for increasingly long charging times are shown on Type 1 devices. The corresponding recovery traces can be seen in (b) for Type 1 and in (c) for Type 2. In an analog way, in (d) the fast sweep $I_D(V_G)$ curves after positive bias of 5V are shown. For Type 1 devices the degradation is barely recoverable (e). On Type 2 FETs the degradation is mostly recoverable also for long charging times, see (f).
Extended Data Fig. 10 | BTI on Type 2 GFETs. For Type 2 GFETs the fast sweep \( I_D(V_G) \) curves after positive and negative gate biasing are shown. These transfer characteristics were recorded to evaluate \( V_{Dirac} \) directly after the biasing at an elevated gate voltage, at \( t_{\text{recovery}} = 0.5 \text{ s} \). In (a), NBTI curves are shown at \(-10 \text{ V}\), and in (b), at \(-5 \text{ V}\). In (c) and (d), PBTI curves are shown at 10 V and 5 V, respectively. The corresponding fast sweep \( I_D - V_G \) curves for Type 1 GFETs are shown in Figs. 6(a) and (d), and in Extended Data Figs. 9(a) and (d).