A Channel Self-Alignment process for High-Voltage VDMOSFETs in 4H-SiC

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Abstract. In this paper, we describe a channel self-alignment process to produce High-Voltage VDMOSFETs in 4H-SiC. We use polysilicon as a mask for two injection methods, because the oxidation rate of polysilicon is different from that of silicon carbide, we can generate a certain thickness of silicon oxide flank wall by controlling the oxidation rate and time. Therefore, there will be a certain distance between the N+ source region and the Pbase region, and this distance is the length of the channel. Obviously, no pattern transfer occurs between the two ion implantation processes, so the channel is self-aligned. As long as the thickness of the side wall is controlled accurately, the channel length of sub-micron can be obtained.

Keywords: Self-Alignment, oxidation, polysilicon, flank wall.

1. Introduction
Since the 1990s, researchers in power electronics devices have turned their attention to wide bandgap semiconductor materials such as silicon carbide (SiC), which have better electrical properties. SiC is the most mature third generation of wide band gap semiconductor materials. The breakdown electric field strength is one order of magnitude higher than silicon material, so in the same epitaxial thickness and doping concentration, devices in SiC can achieve higher breakdown voltage. Carriers have higher saturated mobility and thus can operate at higher frequencies. Good thermal conductivity can get greater power density, so it is very suitable for the production of high temperature, high frequency, high power electronic devices [1-4], and will be widely used in the field of power electronics.

The Vertical double-diffusion metal-oxide-semiconductor field-effect Transistor (Abbreviated as VDMOS) of high input impedance, high operating frequency, drive circuit is relatively simple, so in low power, high frequency switching field has been widely used. The leakage pole of VDMOS is located on the back substrate, the source and gate electrodes are located on the surface, and the current path is perpendicular to the device surface, thus simplifying surface wiring. In addition, the conductivity of most carriers makes the on-resistance of VDMOS have positive temperature characteristics, and it is generally considered that there is no secondary breakdown, so multiple cells can be connected in parallel to achieve large current. However, the specific on-resistance of the single-pole device increases with the increase of the breakdown voltage. For Si devices, the resistance will increase dramatically to levels...
unacceptable for practical high voltage applications. The IGBT reduces the specific on-resistance while maintaining the breakdown voltage through the conductance modulation effect, but the reverse recovery characteristic is obviously degraded due to the presence of minority carriers. And SiC VDMOS can set high voltage, high current, high temperature and high frequency working characteristics in one, is the best choice to replace Si IGBT in a certain voltage level. In addition, the full SiC MOS/JBS diode module provides higher energy conversion efficiency than the Si IGBT/PiN diode module. It can be said that SiC devices will be the "green energy" devices that will drive the new energy technology revolution in the future. Therefore, it is very important to complete the self-developed SiC VDMOS device for the development of power grid.

In the fabrication process of SiC VDMOS device, the main factors affecting the channel length are the layout line width and the precision of the etching. In order to avoid the human error and environmental error caused by lithography, Si VDMOS uses polysilicon as the barrier layer of p-type and N-type ion diffusion, and uses the difference in transverse diffusion ratio to form the channel, while the polysilicon is retained as the gate, which is the origin of the name of "double diffusion". Because there is no pattern transfer between the two diffusion processes, no lithographic error occurs in the channel region, known as "self-alignment". However, there is no diffusion junction in SiC, and high temperature annealing will melt polysilicon silicon, so the gate must be made after ion implantation annealing, so Si VDMOS self-aligned process cannot be applied to 4H-sic VDMOS devices. A self-alignment process for 4H-SiC VDMOS devices needs to be developed [5-8].

For low and medium voltage SiC MOSFET devices, the channel resistance \( R_{\text{CH}} \) forms the main part of the device resistance due to low channel mobility [9,10], thin drift region and high doping concentration. And affects the output characteristics of SiC MOSFET devices. The mobility of SiC MOSFET channel field effect is low, and short channels are used to improve the device's on-performance. However, if the channel is too short, it will lead to short channel effect, and the blocking performance of the device cannot be guaranteed. In general, there is a certain alignment deviation in photolithography. The photolithography method to realize MOSFET channel needs enough redundancy on both sides of the cell, which reduces the device's on-off ability. Therefore, self-alignment method is needed to realize the processing of MOSFET channel with high symmetry.

In this paper, polysilicon is used as the ion implantation mask of P base. After the P base region is formed, polysilicon is oxidized or deposited and etched to form the ion access mask of N plus region. This method can achieve short channels below 1um, reduce the cellular area of MOS devices, and improve the current density of devices.

2. Photolithography for Channel
As is known to all, the diffusion coefficient of SiC is low, and the doping requires the ion implantation process. Therefore, SiC cannot use the Si standard double diffusion process to form the channel. The channel length of silicon carbide MOSFETs has a great influence on the on-resistance of the device. The smaller the width of the channel, the smaller the resistance of the channel. At present, many processes use photolithography to generate the field effect channel [11,12]. This method uses two ion implantations to generate the field effect channel. For n-type FET, first lithography p-well pattern and p-type ion implantation were performed, followed by lithography N plus pattern and ion implantation, as shown in Figure 1. The process of two photolithography for the field effect channel. The distance between two lithography in the center is the length of the channel. This method is the simplest, the length of the channel is controlled by the layout structure, and the process is simple. However, it is difficult to achieve a short channel by photolithography due to the influence of the alignment accuracy of two photolithography. This method is generally difficult to achieve channels below 1.0 um.
3. Organization of the Text

The simulation results show that when the ion implantation concentration in P base region is $4.6 \times 10^{17} \text{cm}^{-3}$ and the channel width is 0.5 um, the short channel effect is not guaranteed and the threshold voltage is about 3 V. The fabrication of short channel MOSFETs requires high precision of alignment of photolithography and etching.

In the manufacture of silicon-based VDMOSFET, polysilicon gate is often used as the ion implantation mask of P base and N plus source region. By changing the diffusion time and diffusion temperature after ion implantation, the ion diffusion length after implantation can be controlled and the width of the channel can be controlled. The polysilicon gate is retained as the gate of VDMOSFET. This process is commonly referred to as a "self-alignment process". The ion diffusion coefficient of silicon carbide is very low, and there is no diffusion junction. At the same time, the activation annealing temperature of silicon carbide after ion implantation is up to 1800 ℃ which is much higher than the melting point of polysilicon. Therefore, the silicon-based "self-aligned process" is not suitable for the production of silicon carbide MOSFETs.

A self-alignment process for silicon carbide MOSFETs was developed according to the unique properties of the material. Photoresist is not suitable as a mask for ion implantation of silicon carbide because the injection of silicon carbide is generally carried out at high temperatures. Moreover, because of the high energy required by silicon carbide ion implantation, a thick mask is needed as the barrier layer of ion implantation. The thick mask requires that the mask material should be easy to process and have good steepness after processing. Therefore, we can choose polysilicon as the mask layer of silicon carbide ion implantation. Due to oxidation rate of polycrystalline silicon and silicon carbide, about 5 ~ 6 times, so we can be in the first P base, after the completion of injection on oxidation process, select the appropriate oxidation process conditions, to control the thickness and the thickness of silicon carbide.
oxidation on the side of the polysilicon, after DHF rinse, can be used as the second N plus injection mask barrier layer. The process flow chart is shown in Figure 2. In this way, the second photolithography is not used in this process, and the problem of short channel generation is better solved, so that the channel length is independent of the precision of casing and photolithography, and the channel length completely depends on the polysilicon side wall oxidation thickness, ensuring the consistency of channel length on both sides of the cell.

![Figure 2. Preparation of self-aligning channel by oxidation of polysilicon.](image)

4. Experiment and Results

In this process, polycrystalline silicon with a thickness of 1.2 um is first grown on a SiC wafer, and then lithographic exposure P base plate is used to etched the polycrystalline silicon. After the completion of P base injection, the silicon carbide wafer enters the oxidation furnace to be oxidized. By improving the oxidation time, temperature and gas flow, the side wall with different thickness is obtained, and the oxidation thickness of silicon carbide surface and polysilicon side wall is suitable as shown in table 1.

| Numble | Temperature (℃) | O₂ Flow (L) | N₂ Flow (L) | Time (min) |
|--------|-----------------|-------------|-------------|------------|
| 1      | 1250            | 18          | 2           | 90         |
| 2      | 1250            | 18          | 4           | 90         |
| 3      | 1250            | 18          | 0           | 90         |
| 4      | 1200            | 20          | 0           | 90         |
| 5      | 1200            | 20          | 0           | 150        |
| 6      | 1200            | 22          | 0           | 150        |
| 7      | 1250            | 20          | 0           | 120        |
| 8      | 1250            | 22          | 2           | 150        |
| 9      | 1250            | 20          | 0           | 150        |
| 10     | 1250            | 20          | 0           | 90         |
| 11     | 1250            | 22          | 0           | 120        |
| 12     | 1300            | 20          | 0           | 120        |
| 13     | 1300            | 22          | 2           | 120        |
| 14     | 1300            | 18          | 0           | 150        |
Finally, the following figure was obtained under the conditions of temperature 1250°C, gas flow rate 20 L/min and time 150 min. The cross section of samples as shown in Figure 3 (a). Figure (b) is the picture after the oxidation layer on the surface of silicon carbide is removed by DHF rinses, and the final silicon oxide layer about 0.5 um is formed at the side wall of polysilicon.

As can be seen from Figure 3, after oxidation, the silicon carbide wafer generates about 40 nm ~ 50 nm oxide layer, while the growth thickness on the surface of polysilicon is about 540 nm ~ 550 nm, and the thickness of the oxide layer on the side wall of polysilicon is about 560 nm ~ 570 nm. After DHF rinsing, the silicon oxide on the silicon carbide surface was removed, and the remaining thickness of the side wall of the silicon oxide was 480 nm ~ 510 nm. If the required channel width is 300 nm, we only need to reduce the oxidation time to 120 min., and keep the oxidation temperature at 1250°C and the gas flow rate at 20 L/min unchanged.

![Figure 3. The SEM for cross section of oxidation side wall.](a) Before DHF rinsing; (b) After DHF rinsing.)

5. Conclusion
In this article, we based on the research of the silicon carbide and polycrystalline silicon oxidation characteristics, developed in view of the "double injection" silicon carbide mosfets channel since the alignment process, through to the gas flow rate, temperature, time changes, as the injection mask of polysilicon and silicon oxide on the surface of the silicon carbide side has a certain proportion, removal of silicon oxide, silicon carbide surface The thickness of silica on the polysilicon side wall becomes the channel thickness suitable for MOSFETs. Obviously, there is no pattern transfer between the two ion implantation processes. This method can better solve the problem of short channel generation, making the channel length independent of the precision of the casing and lithography, and the channel length completely depends on the polycrystalline thickness and the oxidation process, ensuring the consistency of the channel length on both sides of the cell.

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