Single-Electron Transistor in Strained Si/SiGe Heterostructures

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A split gate technique is used to form a lateral quantum dot in a two-dimensional electron gas of a modulation-doped silicon/silicon-germanium heterostructure. e-beam lithography was employed to produce split gates. By applying negative voltages to these gates the underlying electron gas is depleted and a lateral quantum dot is formed, the size of which can be adjusted by the gate voltage. We observe single-electron operation with Coulomb blockade behavior below 1K. Gate leakage currents are well controlled, indicating that the recently encountered problems with Schottky gates for this type of application are not an inherent limitation of modulation-doped Si/SiGe heterostructures, as had been speculated.

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With the introduction of the Si/SiGe heterobipolar transistor into large scale production, Si-based heterostructures have become an important material system for electronic high-performance device with full compatibility with standard Si technologies. Meanwhile, the first digital CMOS circuits with selectively grown SiGe epilayers are commercially available and intense research and development is dedicated to the fabrication of SiGe pseudosubstrates and SiGe-on-insulator substrates for further device applications. In terms of basic research, great effort is directed toward spintronic and quantum computing as potential techniques for future computation and encrypting facilities. Si-based heterostructures have distinct advantages in these fields because of the extremely long spin coherence times, which are attributed to the small spin-orbit interaction, and the low natural abundance of isotopes with nuclear spin. Moreover, in this material system the interaction between the spins of the conduction electrons and the nuclei can be further reduced or even completely suppressed by employing enriched Si, and Ge with a depleted Ge isotope. This way, matrix materials free of nuclear spins are conceivable in addition to the unrivalled ultra-large scale integration capabilities of Si technologies.

On a device level, single electron transistors (SET) with carrier confinement in all three directions of space are considered a key-component for spin manipulation and programmable entanglement. While SET development for laboratory applications have reached a mature state in heterosystems based on III-V compound semiconductors, only few Si/SiGe SETs have been reported. Moreover, none of these was achieved by the usual split-gate technique that is considered a precondition for efficient coupling of quantum dots and for high integration. It was pointed out in some of these papers that a lateral quantum dot cannot be achieved by Schottky split gates due to detrimental leakage currents through threading dislocations in the crystal and Fermi level pinning. Here we demonstrate that excessive leakage currents are not an intrinsic limitation of modulation-doped Si/SiGe heterostructures: Our split-gate SETs show well-behaved Coulomb blockade and very low leakage currents of the Pd Schottky gates.

A high-mobility n-type modulation-doped Si/SiGe heterostructure, similar to the one described in detail in Ref., was grown by molecular beam epitaxy (MBE) in a Riber SIVE 45 Si aperatus. In brief, on a standard 4" Si (001) substrate a 2.5 μm thick relaxed step graded buffer (Si0.95Ge0.05 to Si0.75Ge0.25) is grown. A 0.5 μm thick constant composition buffer (Si0.75Ge0.25) follows the step graded buffer. The 2DEG is formed at the upper interface of a 150 Å thick strained Si channel which is grown subsequently. The 200 Å thick antimony-doped Si0.75Ge0.25 layer was grown at 300°C, and is separated from the channel by a 150 Å thick Si0.75Ge0.25 spacer layer. Finally a 450 Å thick Si0.75Ge0.25 layer and a 100 Å Si cap were grown at an temperature of 600°C. Shubnikov-de-Haas and Hall measurements performed at 1.5 K show an electron density of 3.2 × 10¹¹ cm⁻² with an electron mobility of 150000 cm²/Vs.

Ohmic contacts were formed by deposition of Au/Sb and subsequent annealing at 350°C for 60sec. A Hall-bar structure was prepared by optical lithography and reactive ion etching (RIE) with SF₆. Subsequently the split gate structures were written by e-beam lithography with a LEO Supra 35 scanning electron microscope (SEM) into PMMA. The split gates were fabricated by using a lift-off technique. Pd was used as a gate metal, which has (together with Pt) the highest Schottky barrier on n-silicon. A SEM micrograph of the final structure is shown in figure 2. The pitch between the upper gates is 185nm. Finally, connections from the split gates to the bond pads where also made of Pd using optical lithography and lift-off in acetone.

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To measure the leakage current all gates were connected in parallel to increase the area of the Schottky gates and thus probe the worst-case leakage currents. Measurements where performed in an He\(^3\) cryostat at a temperature of about 300 mK. Down to a voltage of about -3 V leakage currents were below 0.02 nA, which is at the sensitivity limit of the experimental set-up. Below -3 V the current increases rapidly as expected for a Schottky diode. However, conductance oscillations are observed at gate voltages between -1.46 and -1.6 V, which is in the non-conduction part of the diode characteristics.

By applying negative voltages to the gates the underlying 2DEG can be depleted and a laterally constricted area of free carriers ("dot") is formed between the gates. By varying the plunger gate (G2) voltage, the energy levels inside the quantum dot can be moved into and out of resonance with the Fermi level in the leads. The conductance will increase whenever the energy level in the dot is aligned with the Fermi levels of the leads, and decrease in between, forming the so called Coulomb oscillations. Resistance oscillation measurements were performed in an He\(^3\) cryostat at 300 mK using a low frequency lock-in technique with 200 \(\mu\)V ac voltage applied between source (S) and drain (D) contacts. Figure 4 shows typical resistance oscillations observed by sweeping the gate voltages of gates G1 and G2 and keeping the voltages of the gates G3 and G4 fixed. Resistance minima are clearly separated by regions of increased resistance.

By measuring the conductance as a function of the plunger gate voltage and an additional dc voltage applied between source and drain contacts, one can obtain the quantum dot spectrum, resulting in Coulomb block-
FIG. 5: Conductivity as a function of the Source-Drain voltage for two combinations of fixed gate voltages. The lower curve shows the dot in a nonconducting state. In the upper curve an energy level is aligned with the Fermi sea at no bias.

FIG. 6: Quantum dot spectrum taken at 300mK.

From the size and shape of the diamonds electrical properties such as capacitances of the gates and leads with respect to the dot can be analyzed. One can estimate the dot capacities and thus the size of the dot by analyzing the distance of neighboring Coulomb diamonds and their slopes. This analysis yields a gate capacity of 5.6 aF and a source capacity of 34 aF. The total dot capacity of 56 aF gives an estimated dot radius \( R \) of about 650 Å, when assuming that the dot capacity is the same as a metallic disc with a capacity of \( C = \frac{8\epsilon\epsilon_0}{\epsilon_0}R \). \( \epsilon_0 \) is the permittivity of vacuum and \( \epsilon \) the relative permittivity of silicon. Therefore the electron number in the dot can be estimated to be about 40 by using the measured electron density of \( 3.2 \times 10^{11} \) cm\(^{-2}\).

In summary, a lateral quantum dot has been fabricated on modulation doped Si/SiGe heterostructures with a split-gate technique. The quantum dot spectrum has been measured up to a temperature of 1 K. These results show that SET functionality can be achieved in modulation-doped Si/SiGe heterostructures with a standard split-gate approach that can easily be integrated into an array of coupled SETs for spintronic applications, as suggested in Ref. 7.

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