Effects of DC gate and drain bias stresses on the degradation of excimer laser crystallized polysilicon thin film transistors

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Abstract. The effects of gate and drain bias stresses on thin film transistors fabricated in polysilicon films crystallized using the advanced sequential lateral solidification excimer laser annealing (SLS ELA) process, which yields very elongated polysilicon grains and allows the fabrication of TFTs without grain boundary barriers to current flow, are investigated as a function of the active layer thickness and of the TFT orientation relative to the grains. The application of hot carrier stress, with a condition of $V_{GS} = V_{DS}/2$, was determined to induce threshold voltage, subthreshold swing and transconductance degradation for TFTs in thicker polysilicon films and the associated stress-induced increase in the active layer trap density was evaluated. However, this device degradation was drastically reduced for TFTs fabricated in ultra-thin films. Furthermore, the application of the same stress condition to TFTs oriented vertically to the elongated grains resulted in similar threshold voltage shift but in substantially decreased subthreshold swing and transconductance degradation. The immunity of ultra-thin active layer devices to degradation under hot carrier stress clearly suggests the implementation of ultra thin SLS ELA polysilicon films for the fabrication of TFTs exhibiting not only high performance but, especially, the high reliability needed for integrated systems on panel.

1. Introduction
High performance, low temperature polysilicon thin film transistors (TFTs) are nowadays necessary for advanced active matrix liquid crystal displays, as high resolution and sophisticated peripheral functions cannot be delivered by amorphous or as-deposited polysilicon TFTs. Moreover, recent crystallization advances have improved TFT performance to the point of allowing their use for the monolithic integration of TFT-based circuits on the display substrates and making silicon on insulator (SOI) and system on glass panel (SOP) applications possible. A critical breakthrough has been the introduction of lateral solidification excimer laser annealing (ELA) technologies [1,2], which yield elongated high quality polysilicon grains resulting in very high performance TFTs [3] and appear to be increasingly becoming the industry standard [4].

The performance level and the electrical-stress-induced degradation of such advanced TFTs are of great importance to system designers for the integration of high functionality sub-systems on LCD panels. Thus, a systematic investigation of the device ageing behavior under hot carrier stress is
necessary. While TFTs in polysilicon films made using advanced laser-based techniques have been characterized [5] and degradation studies have begun to appear for polysilicon films of a given thickness [6,7], no evaluation of the effect of film thickness, which influences crystalline quality, on post-stressed TFT characteristics has been reported; this becomes particularly important in light of the fact that from the device operation point of view thinner device channels are desirable [8] and a polysilicon film thickness well below 50 nm is expected to be used in TFTs in the near future.

In this paper the effects of DC hot carrier stress on TFTs fabricated using the sequential lateral solidification (SLS) excimer laser annealing (ELA) lateral crystallization technique are investigated. The degradation of critical MOSFET device performance parameters and of extracted trap densities is determined for TFTs in SLS ELA polysilicon films with thickness ranging from 30 to 100 nm. The effect of film thickness as well as of TFT orientation relative to the polysilicon grains is evaluated.

2. Experimental

NMOS TFTs were fabricated in polysilicon films 30 to 100 nm thick, formed by crystallization of amorphous silicon films deposited at 320°C by plasma enhanced chemical vapor deposition (PECVD) on quartz substrates. The a-Si films were transformed to polysilicon ones by excimer laser annealing, using the sequential lateral solidification (SLS) process [1]. The SLS process was conducted by scanning the samples under an appropriately shaped [2] laser beam, generated by a LPX 315i Lambda Physik excimer laser (XeCl, 308nm) with a discharge frequency of 150Hz. The resulting polysilicon films have a structure composed of very long crystal grains, much longer than the device channel length, separated by roughly parallel domain boundaries [3].

The fabricated TFTs had a non-self-aligned top metal gate structure, with a 100 nm-thick PECVD SiO₂ gate dielectric layer, and were aligned (unless otherwise indicated) with the grain boundaries parallel to the direction of current conduction, maximizing the electron mobility. Data were obtained from devices having channel dimensions of (W, L) = (8 µm, 8 µm). The TFTs were characterized and stressed using a HP4140B semiconductor analyzer. The I_DS-V_GS transfer characteristics were taken at room temperature with V_DS=0.1 V and for V_GS of −7 V to +7 V. The slope of a line fitted to the I_DS-V_GS curve at the point of maximum transconductance g_m yielded the field-effect electron mobility µ, while the intercept of that line yielded the extrapolated threshold voltage V_th. The subthreshold slope s was extracted from the maximum slope of the I_DS-V_GS characteristic, drawn in semilog scale. A bias stress (V_GS, V_DS) = (7 V, 14 V) was applied for various durations of up to 120 hours (V_GS = V_DS/2 corresponds to worst ageing conditions), the I_DS-V_GS curves were taken at each stressing time and the same device parameters were extracted in order to determine the effect of hot carrier stressing.

3. Results and Discussion

Figure 1 shows an SEM micrograph of an SLS-crystallized polysilicon film, in which the very elongated structure of the polysilicon grains is evident. It can be observed that devices placed parallel to the elongated grains have no grain boundaries vertical to the drain current flow; this allows them to approach SOI level performance. On the contrary, in devices placed at a perpendicular angle the drain current electrons have to cross several boundaries, a fact that significantly limits their mobility.

Figures 2, 3 and 4 show the degradation, against stressing time, of the threshold voltage V_th, the subthreshold slope s and the transconductance g_m for TFTs fabricated with orientations parallel to the grain direction in 30, 50 or 100 nm SLS ELA polysilicon films. In addition, the degradation of the same parameters for TFTs in 100 nm films oriented vertical to the grains is shown. It can be observed that the thicker the polysilicon films, the more pronounced parameter degradation is measured, especially for s and g_m. TFTs in the thinnest 30 nm films are almost insensitive to the bias stressing.

The positive V_th shift observed in figure 2 is attributed to trapping of injected electrons in oxide traps and in interface trap states created by the stressing-induced electron injection, such as weak and broken silicon bonds. Electron injection into the oxide can be facilitated by surface asperities on the polysilicon films that lead to localized field enhancement. In figures 3 and 4 s and g_m are observed to exhibit degradation, which is ascribed to stress-induced creation of interface and active layer defects; s
is controlled by the energy and density $D_n$ of interface and active layer traps with energy levels near the silicon mid-gap [9]. The degradation rate becomes more pronounced for increasing polysilicon film thickness, indicating a larger rate of trap creation (mostly at grain boundaries) for thicker films.

The crystalline quality of SLS ELA polysilicon films is improved with increasing film thickness, with wider crystal domains and reduced trap density in the regions between the boundaries [3]. Thus, TFTs in thicker films exhibit higher currents and more self-heating degradation. Also, the lower defect density in thicker films may mean a proportionally more evident stress-induced degradation. In thinner, more defective films electrons may suffer more scattering but at a lower energy, as their mobility and drift velocity are lower, eventually resulting in less pronounced degradation. Thus, it appears that the same stressing condition and duration results in a defect generation that is larger, with respect to the defect density in unstressed devices, in films of originally better quality.

The $V_{th}$ shift for vertically oriented (at a $90^\circ$ angle to the grains) TFTs is similar to that for ones oriented parallel to the grains in films of the same thickness. This indicates a similar charge injection into the oxide; $V_{th}$ is affected more by electron injection than by active layer degradation, as also observed by TFT degradation studies for varying conditions [10]. However, vertically oriented TFTs in 100 nm films exhibit very small $s$ and $g_m$ deterioration, approaching the immunity to degradation exhibited by the (parallel oriented) ones in 30 nm films. This is consistent with a higher defect density in the active layers of vertically oriented unstressed devices, as compared to similar parallel oriented
ones, due to the inclusion of grain boundaries in the channel, in a similar way that the higher initial defect density of thinner films corresponds to less pronounced degradation of TFTs fabricated in them.

Figure 5 shows the evolution, with stressing time, of the grain boundary trap density $N_t$, extracted by a Levinson [11] fit, and of the midgap trap density $D_{ts}$ (of defect trap states with energy levels near the silicon midgap, either intragrain or grain boundary ones), extracted from the subthreshold slope, normalized with respect to their values before stress. It can be observed that in both cases (a) the TFTs in thin 30 nm films are insensitive to the DC hot carrier stressing, with a negligible trap creation, and (b) the degradation, that is, stress-induced grain boundary and intragrain trap creation, increases with polysilicon film thickness. It is also observed that the degradation of $D_{ts}$ is more pronounced than that of $N_t$, indicating some intragrain midgap level trap generation (which affects $D_{ts}$ but not $N_t$).

Figure 4. $g_m$ degradation vs. stressing time for SLS ELA TFTs in various polysilicon films.

Figure 5. $N_t$ and $D_{ts}$ evolution vs. stressing time for SLS ELA TFTs in various polysilicon films.

4. Conclusions
The application of DC hot carrier stress on poly-Si TFTs fabricated using the advanced SLS ELA process was determined to result in degradation strongly dependent on polysilicon film thickness and device orientation. The device parameters $V_{th}$, $s$, $g_m$ and the trap densities $N_t$ and $D_{ts}$ showed a marked degradation rate reduction with decreasing active layer thickness, with ultra-thin TFTs exhibiting very high reliability. This feature allows the integration of high functionality sub-systems on LCD panels.

5. References
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