I. INTRODUCTION

It is widely accepted that potential scalability by means of the present-day or prospective microelectronic technology is the main advantage of solid state qubits, and in particular, superconducting qubits (see, e.g., [1, 2]). One of the many requirements necessary to realize this potential is a reasonably high integration density of both the qubit and control circuits, which almost unavoidably means that control circuits should be located close to qubits with their milli-kelvin operating temperatures, and are allowed to dissipate only small amount of energy. The requirement of low energy dissipation and ability to function below liquid-helium temperatures make superconductor Single-Flux-Quantum (SFQ) devices [3] the most promising candidate for prospective qubit control circuit technology [4]. Reported SFQ devices are also much faster than their semiconductor counterparts (see, e.g., [3]) and, as a result, should provide a much better accuracy of qubit control.

Although the SFQ circuits have been investigated for many years, one of the implied “design objectives” of these investigations was the possibility to increase rather than decrease operating temperature, and many of the suggested approaches can not be immediately applied to qubit control circuits. The main new obstacle introduced by low operating temperatures is a dramatic degradation of thermal conductivities of all materials at milli-kelvin temperatures. This should cause strong overheating of the SFQ circuits, which dissipate power that is small in comparison to semiconductor devices, but is still very significant in the sub-kelvin temperature range. Overheating establishes effective temperature of the SFQ components far above the bath temperature. It also affects the qubit part of the circuit both directly, through the heat flow to qubits, and indirectly, by creating stronger electromagnetic noise that acts as an extra source of decoherence for qubits.

In this work, we analyze the overheating problem facing SFQ circuits at sub-kelvin temperatures. The analysis results in semi-quantitative understanding of the magnitude of the SFQ-induced disturbance of the qubits, and re-scaling of the SFQ circuits required to satisfy thermal constraints of the sub-kelvin temperature range. The main elements of this re-scaling can be summarized as follows. For a given clock frequency of a conventional SFQ circuit, its power dissipation $P$ is proportional to typical critical current of the Josephson junctions in the circuit. In its turn, the critical current can not be reduced below some thermal value which scales linearly with effective operating temperature $T$ of the circuit because of the thermally induced errors in its dynamics. Finally, the temperature $T$ is determined by the balance between the dissipated power $P$ and efficiency of the heat removal from the circuit. Qualitatively, since the thermal conductivities of all materials show strong dependence on the temperature $T$, direct re-scaling of conventional SFQ circuits will be capable of providing only relatively modest reduction of their effective temperature (in practical terms, to about 0.4 K). Overheating of the SFQ components of this magnitude requires their careful thermal insulation from the qubits, which in the case of SFQ circuits with large complexity can be easily achieved by placing them on a separate chip. Alternative solutions, such as specially modified substrates or advanced thermal coupling with the sink, are more complicated and as a result they could be recommended for “industrial type” projects.

II. HEAT FLOW AT SUB-KELVIN TEMPERATURES AND ESTIMATES OF THE THERMAL RESISTANCES

Temperature of a superconductor integrated circuit is defined by the balance of the power dissipated in the cir-
In the “differential” form, expression for the heat flux $P$ between the two regions with temperatures $T_1$ and $T_2$ is valid for small temperature difference $\Delta T \equiv T_2 - T_1 << T_1 \simeq T_2 \equiv T$:

$$P = \gamma T^\beta \Delta T.$$  \hspace{1cm} (1)

The corresponding “integral” expression valid for arbitrary $T_1$ and $T_2$ is

$$P = \frac{\gamma}{\beta + 1}(T_2^{\beta+1} - T_1^{\beta+1}).$$  \hspace{1cm} (2)

In the next subsections we discuss different specific mechanisms of the heat conduction and their effect on the temperature distribution in the SFQ circuits.

### A. Electron-phonon coupling

Electrons in the bias and shunt resistors are the main sources of the dissipated energy in the SFQ circuits, and as a result, have the highest temperature among the elements of the circuit. This temperature is the most important one for the circuit operation since the magnitude of the fluctuation-induced errors obviously depends on the electron rather than phonon temperature. Resistors in the SFQ circuits are typically attached at the ends to superconducting electrodes so that the heat flow through the contacts is suppressed by Andreev reflection. Electron-phonon relaxation provides then the main mechanism of electron cooling in the resistors. According to the standard model of this relaxation in a metal, steady-state electron temperature $T_e$ and the lattice temperature $T_p$ in the resistor are related as follows [11, 12]:

$$P_{e-p} = \Sigma \Lambda (T_e^5 - T_p^5).$$  \hspace{1cm} (3)

Here $P_{e-p}$ is the heat flux between the electrons and the lattice, $\Sigma$ is a material constant, and $\Lambda$ is the volume of the resistor. For metals, typical value of $\Sigma$ is $\Sigma \simeq 10^9$ Wm$^{-3}$K$^{-5}$. Equation (3) shows that electron-phonon coupling decreases very rapidly with temperature, and at sub-kelvin temperatures electrons in the resistors are significantly overheated by electrical current. Because of the strong power-law dependence in Eq. (3), and for power values relevant for the SFQ circuits, electron temperature is determined mostly by the applied power and only little by the lattice temperature and for $T_e > T_p$ can be safely estimated as $T_e \simeq (P_J/(\Sigma \Lambda))^{1/5}$, where $P_J$ is the Joule heating due to electrical current through the resistor. For the power range and resistor volumes of interest (on the order of nW and $\mu$m$^3$, respectively), this estimate falls into the temperature interval 0.1 K - 1 K. In this temperature range, the thermal resistance ($G^{-1}_{p-sub}$) between phonons in the film and the substrate is usually taken to be rather small compared to the electron-phonon resistance ($G^{-1}_{e-p}$) due to strong coupling between phonon systems in a thin film and a substrate [11, 12, 12, so
that the effective “electron-substrate” coupling can be described by Eq. (3).

An experiment to check the validity of Eq. (3) and the arguments above in realistic conditions was performed, using a typical wafer from HYPRES Inc., with molybdenum resistors. The idea of the experiment was to use transition at temperature $T_c$ of Mo resistor from normal to superconducting state as an electron thermometer and estimate the electron-phonon thermal coupling as follows. In spite of the limitation that we can detect only one electron temperature $T_e$ (measured to be $\approx 0.893\ \text{K}$ for these Mo resistors) we can measure the Joule heating power needed to keep the resistor in the resistive state at a temperature just above $T_e$, for different (smaller) lattice temperatures. Thus this measurement produces all the data necessary for analysis based on Eq. (3): the electron temperature $T_e = T_c$, the heating power, and the phonon temperature which we take to be equal to the temperature $T_0$ of the sample holder. This approximation is justified, since at temperatures $T_0$ below the electron temperature $T_c$ the actual phonon temperature is practically irrelevant because of the strong power-law dependence in Eq. (4).

Figure 2(a) illustrates our measurement procedure. We make use of strong hysteresis of the current-voltage characteristics of the resistor. Initially, at low currents, the resistor remains in the superconducting state and $P_J = 0$ (trace A $\rightarrow$ B in Fig. 2(a)). Only after exceeding the critical current of the molybdenum strip ($I_c = 1.065\ \text{mA}$ at $T_0 = 380\ \text{mK}$ in Fig. 2(a)) we dissipate power in the resistor (B $\rightarrow$ C corresponds to superconducting - normal state transition). Now the Joule heating is very strong, and only by reducing the current far below the critical current to $I_{res}(T_0)$ (D $\rightarrow$ E in Fig. 2(a)) we reduce the electron temperature sufficiently to finally detect transition back to the superconducting state (E $\rightarrow$ F). The power at this working point, $P_J = R^2 I_{res}(T_0)$ heats the system up to $T_e = T_c$. Experimental values of $I_{res}$ at different bath temperatures and heating power $P_J$ as a function of $T_e - T_0$ are presented in Fig. 2(b,c). The dashed line shows good fit of the measured data using Eq. (3), $A = 24\ \text{µm}^2$, and

$$\Sigma = 0.9 \cdot 10^9\ \text{Wm}^{-3}\text{K}^{-5}.$$  \tag{4}

We see that the electron-phonon constant obtained from this fit is indeed in line with the typical metal values.

Generally an SFQ circuit contains a large number of resistors with different electronic temperatures and the error rate depends on all these temperatures. However, the cumulative effect of electronic temperatures $T_{eb}$ and $T_{es}$ of the two resistors used to bias ($R_b$) and shunt ($R_s$) the same Josephson junction can be reduced to a single noise temperature $T_N$:  

$$T_N = (T_{eb}R_s + T_{es}R_b)/(R_s + R_b).$$ \tag{5}$$

To get a feeling for the magnitude of possible electron overheating we estimate the noise temperature $T_N$ for a typical junction with critical current $I_c = 10\ \mu\text{A}$ biased by the dc current $I_b = 7\ \mu\text{A}$. The junction is critically damped ($\beta = 1$) by a resistor $R_s = 10\ \Omega$ ($I_c R_s = 100\ \mu\text{V}$) and the bias voltage $V_b$ is taken to be about 300 $\mu\text{V}$, i.e., $R_b = 43\ \Omega$. These parameters are reasonable for the fabrication technology for the sub-kelvin circuits offered by HYPRES, which is the only one available commercially. In this technology, Josephson junctions have 100 $\text{A/cm}^2$ density of critical current and all resistors are made of $0.1\ \mu\text{m}$ $\text{PdAu}$ film with 2 $\Omega$ sheet resistance. The bias current $I_b$ in the resistor $R_b$ is nearly time-independent and therefore $T_{eb}$ can be estimated in the steady-state model. Resistor area $A_b$ required for the calculation of the specific heat flux $P_{e-p}$ can be varied.
freely while keeping its resistance (set by the ratio of its length and width) constant. According to a conventional (miniaturization) wisdom the resistor dimensions should be made as small as possible. In HYPRES technology, the minimal recommended dimension (width) is 3 µm, and 43 Ω resistor is 65 µm long in this case. For comparison we will calculate also overheating of the bias resistor of a larger size, with 10 µm width.

From the dissipated power \( P_J = 7 \mu\text{A} \cdot 300 \mu\text{V} = 2.1 \cdot 10^{-9} \text{W} \) and resistor volume \( \Lambda_0 \) that for our two examples is equal to 1.9 \( \cdot 10^{-17} \text{m}^3 \) and 2.1 \( \cdot 10^{-16} \text{m}^3 \), we see that at \( T_p = 0 \) the corresponding electronic temperatures in the two cases are very close: 0.64 K and 0.4 K, despite the factor-of-10 difference in volumes. Shunt resistor \( R_s \) can in principle be much colder (with \( T_e \) approaching \( T_p \)) since the current flows via it only during short (pico-second) SFQ pulses generated by the Josephson junction. Each of such pulses dissipates energy of about \( I_e \Phi_0 \), where \( \Phi_0 \) is the magnetic flux quantum, \( \Phi_0 = \pi \hbar / e \). Corresponding evolution of electron temperature is described by the equation:

\[
P_J = P_{e-p} + C_e dT_e / dt, \tag{6}
\]

where the heat flux \( P_{e-p} \) is given by Eq. (8) and \( C_e \) is the heat capacity of the electron gas. The linear dependence of \( C_e \) on temperature: \( C_e = \gamma_e T_e \), where \( \gamma_e \approx 200 \text{Jm}^{-3} \text{K}^{-2} \) \[14\], and the fact that in the relevant temperature range the SFQ pulses are very fast in comparison to the relaxation time

\[
\tau_{e-p} = (\gamma_e / 3\Sigma) \cdot T^{-3} \approx (0.07 \text{ µK}^3) \cdot T^{-3}, \tag{7}
\]

give the following relation for electron temperature \( T_{ei} \) after passage of \( i \) SFQ pulses:

\[
T_{ei}^2 = T_{ei-1}^2 + 2Q / \gamma_e \Lambda_s. \tag{8}
\]

For the junction parameters in our example, the dissipated energy is \( Q \approx I_e \Phi_0 \approx 2 \cdot 10^{-26}\text{J} \), and the shunt resistor volume is \( \Lambda_s = 4.5 \cdot 10^{-18}\text{m}^3 \). If we start then from \( T_{ei} = 0 \), electron temperature jumps sequentially to 7 mK, 10 mK, 12 mK ... These figures show that our shunt resistor will not be overheated during a "single shot" experiments with only a few SFQ pulses.

As one can see from Eqs. (6) and (8) with \( P_J = 0 \), and assuming again that \( T_p = 0 \), electron temperature changes between the jumps with time \( t \) non-exponentially:

\[
T_e^3 = (\gamma_e / 3\Sigma) / t \tag{9}
\]

and the notion of the relaxation time introduced in Eq. (7) can not be used rigorously, but gives only the characteristic time scale of the temperature variations. Nevertheless, Eq. (7) shows qualitatively that overheating of the shunt resistors becomes significant if the pulse repetition rate exceeds 10 MHz. In particular, at an achievable 10 GHz clock frequency the power is dissipated quasi-continuously and electron temperature of the shunt is constant and high, about 0.4 K.

From this discussion we see that the noise temperature \( T_N \) of a Josephson junction in our example can range from 75 mK for the junction that is not switching frequently and has the bias resistor of large volume, to 0.44 K for the continuously switching junction with the small-volume bias resistor. However, even in the regime of low \( T_N \), the real electron temperature of the bias resistor is high (about 0.4 K) and can produce other overheating effects besides errors in the SFQ circuit operation.

B. Phonon resistances and temperature distribution along the chip

The second important thermal resistance in the chain (Fig. 1) of the heat propagation from a resistor, is that of the substrate. A typical substrate can be viewed as a generic insulator crystal with thermal conductivity \( K \) that can be written at low temperatures as

\[
K = C v l / 3, \tag{10}
\]

and depends on three different parameters. Specific heat \( C \) and an average speed of sound \( v \) are characteristics of the material that are temperature-dependent but are practically independent of material imperfections and sample geometry. For instance, for silicon substrates at low temperatures these constants give:

\[
K(l) = 1200 T^3 l [W m^{-2} K^{-4}]. \tag{11}
\]

In contrast to \( C \) and \( v \), the mean free path \( l \) depends strongly on the crystal quality, doping concentration and other parameters, and varies from several centimeters in single crystals to few tens of nanometers in glasses. For instance, the mean free path of thermal phonons in single-crystal Si can reach up to few centimeters at sub-Kelvin temperatures \[15\]. In this case, the actual thermal conductivity and temperature profile in a wafer with thickness \( d \ll l \) is determined by properties of phonon scattering at the surfaces; therefore thermal conductivity depends on surface properties. In a typical situation of rough surface with diffusive scattering, the conductivity can still be estimated from Eqs. (10) or (11) by taking \( l \sim d \). For specular reflection, ballistic phonon propagation in single-crystal substrate can lead to complicated temperature profiles determined by the “geometric optics” of phonons \[16\].

For a thin wafer, the temperature profile along it due to heat spreading from a resistor is determined by the competition between the heat conduction along the wafer and heat transfer to the sample holder which acts as the heat sink. The heat resistance to the sink consists (Fig. 1) of the heat resistance of the layer of glue (epoxy) and the “Kapitza” resistance of the Si-epoxy and epoxy-Cu interfaces due to mismatch of acoustic properties of these materials. The acoustic-mismatch theory of the Kapitza resistance \[6, 17\] describes the interface conductance \( G_K \) in terms of probability \( D \) for phonons to be transmitted through the interface. In the case of plain interface
between the two materials with equal sound velocities \( v \), “transparency” \( D \) is determined by the difference of their acoustic impedances \( Z_{1,2} \):

\[
D = 4Z_1 Z_2 / (Z_1 + Z_2)^2 ,
\]

where \( Z_i = \rho_i v \), and \( \rho_i \) is the mass density of the material. The interface thermal conductance is then given by the expression similar to Eq. (10), \( G_K = C v D / 4 \), i.e.

\[
G_K = \gamma_K T^3 .
\]

The values of coefficient \( \gamma_K \) for various interfaces, including those encountered in a typical SFQ chip (Fig. 1) can be found, e.g., in [6, 18, 19]. In general, \( \gamma_K \) lies in the range \( 10 - 10^3 \) Wm\(^{-1}\)K\(^{-4}\) for most of the dielectric-to-dielectric or dielectric-to-metal interfaces.

Thermal conductance of the epoxy or other glue layer between the substrate and the sink depends on several factors, including the deposition method [20]. For sufficiently thick layers, however, the conductance should follow the \( T^3 \) temperature dependence characteristic for amorphous materials in the sub-kelvin temperature range [6, 21].

\[
K = \gamma T^2 ,
\]

where \( \gamma \) is within the range \( 10^{-3} - 10^{-1} \) Wm\(^{-1}\)K\(^{-3}\). The two thermal resistances [13] and [14] are connected in series and both contribute to the substrate-sink resistance. The dominant contribution is determined by the thickness \( d_a \) of the amorphous layer, with the transition between mostly Kapitza to mostly bulk resistance occurring at a characteristic value \( d_a = \gamma / (\gamma_K T) \). At \( T \approx 1 \) K, and \( \gamma \) and \( \gamma_K \) at intermediate values within the ranges mentioned above, \( d_a \) is order of 100 \( \mu \)m, implying that at the sub-kelvin temperatures the substrate-sink resistance should typically be dominated by the Kapitza resistance. This is because the thickness of the glue layer, while uncertain, should not be much larger than 100 \( \mu \)m.

To obtain experimental insight in the actual temperature profile on a standard silicon substrate we performed a few experiments with a virtually point-like heater and local thermometers at different distances from it. A small (0.5 \( \mu \)m x 0.5 \( \mu \)m) superconductor-insulator-superconductor (SIS) tunnel junction placed in the center of a silicon chip and biased above the double gap voltage was used as a heat source. Superconductor electrodes were aluminium, with aluminium oxide as the tunnel barrier. Similar junctions at different distances from the heater were used as thermometers. In some of the experiments superconductor-insulator-normal metal-insulator-superconductor (SINIS) structures were used instead as heaters and thermometers with similar results (see Fig. 3). The size of the normal copper island in this case was about 2 \( \mu \)m x 0.2 \( \mu \)m. In both schemes, the strong temperature dependence of the quasiparticle current-voltage characteristics served as a local probe of temperature on the surface of the chip. Figure 4 shows results of a measurement on a wafer used by HYPRES [12] as a standard substrate for Josephson junction circuits. The thickness of the boron doped (10 \( \Omega \) cm), double-side polished (100) wafer was 0.635 mm, and the size of the chip was 8 mm \( \times \) 8 mm. Temperature as a function of power was measured at two different distances (7 \( \mu \)m and 2.8 \( \mu \)m) from the heat source placed approximately in the center of the chip. The bath temperature of the experiment was 77 mK. The temperature at the distance of 7 \( \mu \)m from the heat source reaches twice the bath temperature at the power level of 0.15 nW. Power of 180 nW is required to heat the thermometer at the distance of 2.8 mm from 77 mK up to 150 mK. In addition to the samples made from a typical HYPRES wafer, few other silicon wafers with different thicknesses of oxide layer (including wafer with thin native oxide layer) have been measured and showed similar results.
To attempt fitting these results using the understanding of the phonon heat transport described at the beginning of this section, we need to use different models for the short and long distances from the heater. For distances shorter than the substrate thickness $d$, i.e. including the 7 µm in experiment, phonons propagate ballistically from the point source in the Si substrate. As a relatively crude but simple approximation, one can assume that the point heater at the surface of the Si substrate radiates the power $P$ uniformly in the hemisphere filled by the substrate. In this case the energy density $u$ at a distance $r$ from the source is

$$u = \frac{P}{(2\pi r^2 \nu)}.$$  

(15)

A fraction $f$ of this energy in the non-equilibrium flux of phonons is absorbed by the thermometer. In this process, it is seen by the thermometer as the excess energy density $u_e$ that corresponds to local equilibrium at some temperature $T$ above the background bath temperature $T_0$. In the temperature range of the experiment, we can use the usual Debye law, $u \propto T^4$, for the equilibrium energy density of the phonon system,

$$u_e = (\nu/4)(T^4 - T_0^4),$$  

(16)

where $\nu$ is the coefficient in the Debye specific heat $C = \nu T^3$. Equating the energy density (15) to a fraction $f$ of density (16), we get the effective substrate temperature at the distance $r$ from the source:

$$T(r, P) = T_0^4 + \frac{2fP}{\pi r^2 \nu}.$$  

(17)

The 7-µm solid line in Fig. 4 shows the dependence of temperature $T$ on power $P$ calculated from Eq. (17) using the fraction $f$ as a fitting parameter. The combination of other factors $\nu \nu$ in Eq. (17) is the same as the one that determines the thermal conductivity in Eqs. (10) and (11), and its value for Si can be taken from Eq. (10). We see that one can obtain good fit of the observed $T(P)$ dependence with $f \simeq 0.72$.

The strength of the substrate heating at the larger distance, 2.8 mm, is determined by the interplay of the horizontal heat flow along the substrate, and the heat leakage into the sink through the glue layer (Fig. 1). As was discussed above, since the phonon mean free path $l$ is much larger than the substrate thickness $d = 0.635$ mm, the horizontal heat conductance $K_h$ is dominated by the phonon scattering at the substrate surface. For mostly diffusive scattering, $l \simeq d$, and Eqs. (10) and (11) give:

$$K_h = d \lambda K(d) \equiv \sigma T^3.$$  

The vertical heat conductivity $K_v$ is determined by either Kapitza resistance or heat resistance of amorphous glue layer and can be written as

$$K_v = \lambda(\beta) (T^3 - T_0^3),$$  

where the power $\beta$ is equal to 3 or 4, and the coefficients $\lambda(\beta)$ include all temperature-independent factors.

Neglecting the influence of the external boundaries of the substrate we assume that the heat flow from the heater has radial symmetry. In this case, equation describing the balance between the horizontal and vertical heat flows has the form:

$$\frac{1}{r} \frac{\partial}{\partial r}(r \sigma T^3 \frac{\partial T}{\partial r}) = \lambda(\beta) (T^3 - T_0^3),$$  

(18)

where $r$ is the radial distance from the heater. This equation is valid on the scale of distances larger that the substrate thickness $d$, and should be solved with the boundary conditions describing the generation of power $P$ by the heater at $r = 0$ and negligible heat flow though the outer edge of the substrate at $r = R, (R \simeq 4 \text{ mm for the data presented in Fig. 4})$:

$$\frac{\sigma T^3}{2\pi r} \frac{\partial T}{\partial r} = 0, \quad r \to 0; \quad \frac{\partial T}{\partial r} = 0, \quad r = R.$$  

(19)

Results of solution of Eq. (18) with the boundary conditions (19) are shown as dotted ($\beta = 4$) and dashed ($\beta = 3$) lines for 2.8 mm in Fig. 4. In these curves, an attempt was made to describe the data by fitting $\lambda(\beta)$. One can see that the model does not describe the rapid temperature rise with the power $P$ in the whole range of powers. The initial upturn of temperature with power can be reproduced assuming either $\beta = 3$ or $\beta = 4$ if we take

$$\lambda(3) = 6 \text{ W/m}^2\text{K}^3, \quad \text{or} \quad \lambda(4) = 44 \text{ W/m}^2\text{K}^3.$$  

(20)

The variation of modelling curves with $\beta$ (more rapid temperature rise for $\beta = 3$) suggests that the discrepancy between theory and experiment is due to the substrate-sink heat conductance dominated by the mechanism with weaker temperature dependence, although it is unclear what could be such a mechanism in our set-up. Nevertheless, the fact that the numbers in Eq. (20) lie within the reasonable range discussed above, makes it possible to say that the overall level of the substrate-sink heat conduction agrees roughly with theoretical expectations. Finally, the overall level of the substrate overheating presented in Fig. 4 seems to be consistent with other measurements on similar Si substrates, although the limitations of the thermometer used in [22] do not allow for detailed comparison.

C. Thermalization of resistive films

In some cases gradient of electron temperature along the resistor could play a significant role in electron-phonon relaxation discussed above. In particular, this is the case if the resistor consists of two parts. One (the vertical strip in Fig. 5(a)) actually serves as the resistor, while the other (the horizontal strip) does not carry electric current and serves as the cooling sink or fin. This shape of the resistor enables one to optimize the two parts separately simplifying the design procedure. In this sub-
section, we estimate the length which limits the useful size of the cooling fin. Increasing the fin size beyond this length does not improve electron cooling because of the finite electron thermal conductivity in the resistor film. The distribution of electron temperature along the fin is determined by the electron thermal conductivity \( K_e \) in the film and strength of electron-phonon relaxation \( K_{e-p} \). The conductivity \( K_e \) is proportional to the film thickness \( d_f \) and electron temperature \( T_e \):

\[
K_e = d_f \kappa_e T_e = \sigma_e T_e,
\]

whereas

\[
K_{e-p} = d_f \Sigma (T_e^5 - T_0^5) = \lambda_{e-p} (T_e^5 - T_p^5).
\]

A similar model of the temperature distribution is obtained by assuming a uniform semi-infinite film connected at its side to a hot spot (see Fig. 4(b)). This hot spot approximates one end of a resistor of width 2\( r_1 \). Equations corresponding to the distribution of electron temperature along the fin both in the linear \((m = 0)\) and in cylindrical \((m = 1)\) case can be presented as:

\[
\frac{1}{r^m} \frac{\partial}{\partial r} r^m \sigma_e T_e \frac{\partial T_e}{\partial r} = \lambda_{e-p} (T_e^5 - T_p^5).
\]

Equation (23) for the linear case \((m = 0)\) and \( T_e \gg T_p \) has an analytical solution:

\[
T_e = \left( \xi_S/(r + r_0) \right)^{2/3},
\]

where \( \xi_S \equiv \sqrt{(14/9)} \kappa_e/\Sigma \), and \( r_0 = \xi_S/T_{e1}^{3/2} \) with \( T_{e1} \) denoting electron temperature at the left (hot) boundary of the fin. Solution for the cylindrical case \((m = 1)\) is qualitatively similar if \( r \) is replaced with \( r - r_1 \).

The distance \( r_d \) at which the efficiency of electron-phonon relaxation \( \sim T_e^5 \) becomes two times smaller than at the boundary \((T_e^5 = 0.5 \ T_{e1}^5)\),

\[
r_d = (2^{3/10} - 1)r_0 \approx 0.23r_0,
\]

can be considered as the maximum effective size of the fin: increase of the fin size beyond \( r_d \) does not noticeably improve resistor cooling. On the other hand, for \( r \leq r_d \), one can neglect the variation of electron temperature in the fin, and its thermal resistance is determined by its volume \( \Lambda \) and electron phonon coupling constant \( \Sigma \) through Eq. (4). As a numerical example, we take a copper film for which \( \kappa_e \approx 1 \ \text{WK}^{-2}\text{m}^{-1} \) and \( \Sigma \approx 2 \cdot 10^9 \ \text{WK}^{-3}\text{m}^{-3} \). This gives \( r_d \approx 2 \ \text{mm} \) at the electron temperature of \( T_e = 100 \ \text{mK} \).

III. GENERAL RECOMMENDATIONS ABOUT THERMAL DESIGN

To summarize our arguments we present in Fig. 8 the thermal designs for the SFQ-qubit circuits with different levels of power dissipation. A scientific experiment on qubits controlled by a simple SFQ circuit with the power dissipation below 50 nW is basically doable on a single silicon chip (Fig. 6(a)). In this case, the temperature of silicon substrate \((T_1)\) in the vicinity of qubits can only slightly exceed the bath temperature \( T_0 \) while the electron temperature of resistors of the SFQ circuit can be as high as 500 mK. If needed, electron temperature in a few resistors can be reduced to about 100 mK by cooling fins. A higher dissipation power is acceptable for the chip with additional thermal insulation (for example, porous silicon or specially etched structure on the back of the chip) between areas with qubits and SFQ circuits (Fig. 4(b)). The relatively high thermal resistance along the substrate as compared to the resistance between the substrate and the sample holder makes it possible to keep qubits at low temperature \((T_1)\). The increase of power dissipation above 500 nW requires even better thermal separation of the circuits, and in this case the SFQ circuits could not be placed on the same chip with the qubits. The two-chip design (Fig. 6(c)-(e)) practically eliminates the problem of overheating of qubit circuitry. Moreover, it allows utilization of two independent fabrication technologies for SFQ and qubit circuits, and as a result, the conventional SFQ circuits can be immediately used in qubit support circuits. Both chips can be kept on the same metal sample holder (Fig. 8(c)) if the dissipated total power does not increase \( T_0 \) significantly above the temperature of the mixing chamber. Usually the cooling power of a dilution refrigerator is not a problem up to a dissipation level of few \( \mu \text{W} \). For higher power (more complicated SFQ circuits) the separate active cooling of both circuits is required (Fig. 8(d)). The quantum circuit is supposed to be at the temperature below 50 mK, but
FIG. 6: Optimization of thermal design for the circuits of different complexity. Designs with both circuits mounted on the same holder: (a) RSFQ and quantum circuits on the same Si chip, (b) substrate with improved thermal insulation between two parts, (c) two-chips solution. Separate cooling of circuits with different temperatures and power dissipations: two chips with independent cooling connected by RF lines (d) and inductively (or capacitively) coupled (e).

the SFQ chip can be kept at higher temperature ($T_3$). In this case few different refrigerating stages with the cooling power in the mW range can be used for cooling SFQ circuits. As discussed above, the electron temperature of shunt resistors in the SFQ circuits with reduced critical current should typically be about 500 mK and does not strongly depend on the lattice temperature which is below 500 mK. A $^3$He evaporation refrigerator delivering enough cooling power at a temperature of about 300 mK is a very attractive solution for cooling SFQ circuits. Unfortunately this leads to essential complication of cryogenic equipment. A more natural solution is to make use of different stages in the dilution refrigerator for cooling the SFQ circuit: 1 K pot (temperature 1-2 K) or $^3$He evaporator (600 - 800 mK). The latter is more attractive and natural due to lower temperature and because some heating of this stage is in any case necessary for operation of the dilution refrigerator.

When we consider two circuits mounted at different temperatures, the thermal load through connecting wires should be limited to prevent overheating of the qubit circuit. In the case of superconducting (Nb, Al) leads connecting two chips at 1 K and at 20 mK, respectively, a heat load is about 100 nW, if the total cross-section area of the wires is 0.1 mm$^2$ and the length is 10 mm. This may be acceptable in most cases, but an inductive or/and capacitive coupling between the circuits (Fig. 6(e)) is a more suitable option for a fully scalable solution.

Our discussion assumed a chip size $5 \times 5$ mm$^2$ glued to a bulk copper heat sink, and the power levels mentioned above should be considered as order-of-magnitude estimates. These estimates can be affected by changes in the system design, i.e., different substrate materials and geometry (both area and thickness), improved thermal contact between the substrate and the heat sink (increased contact area, modification of the contact surfaces, etc.), and more powerful dilution refrigerator.

IV. SFQ CIRCUIT OPERATING AT SUB KELVIN TEMPERATURES

The direct way of transferring SFQ circuit design to the sub-kelvin temperature range is to reduce all currents, including critical currents of Josephson junctions and dc bias currents, proportionally to the effective temperature of the junctions. With this scaling, the existing technology can then be used as such and most of the existing SFQ logic elements can be adopted with some modifications. We carried out such scaling for several basic SFQ circuits, and present here the results for the simplest circuit, a balanced comparator. The balanced comparator is one of the principal building blocks of more complex circuits, but it can also be used directly as a thermometer, providing a convenient way of testing thermal characteristics of the circuit.

The circuit (Fig. 7) contains three shunted Josephson junctions and requires for its operation three dc bias currents. One bias current provides the necessary dc bias of comparator junctions $J_2$ and $J_3$. The junctions are in superconducting state and carry dc current about 70% of their critical currents. The other bias current is applied to a relatively low resistance $R_V$ to supply a low, e.g. $12 \mu$V, voltage drop $V_{in}$. Junction $J_1$ converts this dc voltage into a sequence of SFQ pulses generated with frequency $f = (2e/h)V_{in}$. The SFQ pulses escape from the circuit either via junction $J_2$ or via junction $J_3$ depending on the dc current $I$. Thermal or quantum noise
shunt resistors. Can be used to determine electronic temperature in the
\[ \text{[23, 24, 25]} \] for details. Temperature dependence of \( \Delta I \) is determined by comparator and driver characteristics - see

Here \( I_T = 2\pi k_B T/\Phi_0 \) and \( \alpha \) is a dimensionless parameter determined by comparator and driver characteristics - see \[ \text{[23, 24, 25]} \] for details. Temperature dependence of \( \Delta I \) can be used to determine electronic temperature in the shunt resistors.

The comparator was fabricated using standard 100 A/cm² Nb trilayer process of HYPRES with PdAu resistors. The layout of the comparator, which includes two nominally identical junctions (left part of the circuit) and the driver, is shown in Fig. 7. The comparator parameters, \( I_c = 10 \mu A, R_s = 2 \Omega \), were chosen for operation at sub-kelvin temperatures. The junction critical current \( I_c \) was thus reduced by an order of magnitude from its usual value for temperatures around 4 K. For these parameters, the junctions are overdamped, and the crossover temperature \( T^* \) between the regimes of thermal and quantum fluctuations \[ \text{[23]} \] is given by the relation \( T^* \approx eV_c/\pi k_B \approx 70 \text{ mK} \), where \( V_c = I_c R_s \). This means that quantum broadening of the gray zone of the comparator can be neglected in our measurements.

The measurement procedure was similar to that described in Ref. \[ \text{[23]} \]: the width \( \Delta I \) of the gray zone was obtained from the dc voltage \( V \) across one of the comparator junctions as a function of the applied current \( I \) (inset in Fig. 8) and its temperature dependence is presented in Fig. 8. The dashed line corresponds to the theoretical prediction in the thermal limit \[ \text{[Eq. \text{[26]}]} \] assuming that the effective electron temperature of the resistors coincides with the bath temperature \( T \). At bath temperatures above 0.4 K experimental behavior of \( \Delta I \) agrees well with the theoretical prediction. At lower temperatures, \( \Delta I \) does not demonstrate noticeable dependence on \( T \) as a result of the overheating of the comparator circuit. This prevents the reduction of electron temperature below 0.4 K.

Electrical and geometrical parameters of the circuit can be used to estimate the electron temperature expected from the heating model discussed in Sec. II. The circuit contains four resistors. Two shunt resistors of the comparator junctions are located about 4 \( \mu m \) from the junctions. Each of them occupies an area 7.25 \( \mu m \cdot 12.5 \mu m \approx 90 \mu m^2 \). One more resistor with the area 10.5 \( \mu m \cdot 14.5 \mu m \approx 152 \mu m^2 \) shunts the driver junction \( J_1 \) and is located at about 50 \( \mu m \) from the comparator junctions. The last resistor \( R_v \) (seen in the layout of Fig. 7 as 4 resistors in parallel) has the total area 25.5 \( \mu m \cdot 6 \mu m \times 4 \approx 612 \mu m^2 \) and is 125 \( \mu m \) away from the comparator. All resistors are made of 0.1 \( \mu m \) PtAu film with 2 \( \Omega \) sheet resistance, and designed values of the comparator shunts, driver shunt, and resistor \( R_v \) are 2 \( \Omega \), 1.8 \( \Omega \), and 1.4 \( \Omega \), respectively. The voltage drop across the generator shunt, \( R_v \) resistor, and the cumulative voltage drop on both comparator shunts are all about 12 \( \mu V \), while the distribution of the voltage between the two comparator junctions \( J_2 \) and \( J_3 \) depends on the current \( I \).

We estimate electron temperature \( T_e \) in the shunts of the comparator junctions at the center of the gray zone (\( I \approx 0 \)), when both shunts have the same voltage drop 6 \( \mu V \). The shunt parameters from the previous paragraph give their volume \( \Delta = 9 \cdot 10^{-18} \text{ m}^3 \) and the dissipated power \( P = 1.8 \cdot 10^{-11} \text{ W} \). Using these numbers together with negligible phonon temperature \( T_p \) and an estimate of electron-phonon constant \[ \text{[1]} \) in Eq. 3, we get \( T_e \approx 0.3 \text{ K} \). Remote resistors do not affect the estimate of \( T_e \). Their electrical noise changes only the comparator bias and does not contribute to the width of the gray zone in the case of identical junctions \( J_2 \) and \( J_3 \). The phonon overheating in the vicinity of the comparator junctions due to the power dissipated in these resistors

\[
\Delta I \approx (2\pi\alpha I_T I_c)^{1/2}.
\]

FIG. 7: Layout and equivalent circuit of the measured comparator.

FIG. 8: Temperature dependence of the width of the gray zone of the measured comparator. Squares and dashed line are experimental data and theoretical prediction for thermal limit, respectively.

\[
\Delta I \approx (2\pi\alpha I_T I_c)^{1/2}.
\]

(26)
can be estimated from Eq. (17) to be negligible, \(\sim 30 \text{ mK}\). This means that electron overheating in the junction shunt resistors is indeed the dominant overheating factor in our experiment. We note that the measured overheating is somewhat higher than the estimate within our model. The most probable reason for this discrepancy is a small asymmetry between the junctions J2 and J3 which makes it possible for the noise of all resistors in the circuit to contribute to \(\Delta I\). In view of this and other possible sources of extra broadening, agreement between the estimate of \(T_e\) and the observed saturation of \(\Delta I\) is quite good.

V. CONCLUSION

We have analyzed thermal properties of a typical SFQ circuit at sub-kelvin temperatures and performed several measurements testing the basic elements of the heat conduction scheme (Fig. 1) of the circuit. Local overheating of electrons in resistors is controlled by electron-phonon coupling, while global overheating of the chip is determined by the competition between ballistic phonon propagation along the substrate and the leakage into the heat sink that is limited by the Kapitza resistance or the thermal resistance of the glue layer. Our analysis and data suggest that integration of simple SFQ circuits with qubits on a single chip should be possible if the total power dissipated by the SFQ components is below 50 nW. Scalable solutions for a multi-qubit system with large power dissipation require two-chip (hybrid) designs with separate active cooling of the qubit and the SFQ chips. An alternative strategy based on complete revision of the SFQ approach (e.g., development of reversible SFQ circuits) should be considered as a longer term goal.

VI. ACKNOWLEDGMENT

We thank Yu. Polyakov for his help with grey zone measurements. This work was supported in part by "RSFQubit" FP6 project of European Union (A.M.S and J.P.P.), and in part by ARDA and DOD under the DURINT grant # F49620-01-1-0439 and by the NSF under grant # EIA-0121428 (D.V.A. and V.K.S.). Integrated circuit with Josephson comparator has been fabricated at HYPRES, Inc.