Low Temperature Characterization of Hole Mobility in Sub-14nm Gate Length Si$_{0.7}$Ge$_{0.3}$ Tri-Gate pMOSFETs

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Abstract. We performed low temperature characterization of hole mobility in SiGe Trigate nanowires (NW) with gate length scaled down to 10nm. Trigate NWs with high-k/metal gate stack were fabricated on SOI wafers using solely optical lithography to design the wires with width down to 15nm. Drain current measurements are conducted within a cryogenic probe station enabling study on a 80K-350K temperature range. From these measurements we extracted the temperature dependence of the low field mobility $\mu_0$ for a wide range of gate lengths and NW widths using the Y-function method in order to cancel the influence of the mobility attenuation factor due to series resistances. The impact of the temperature over the mobility can be used to identify the dominant scattering mechanism in the channel. Overall, we observed that hole transport is predominantly limited by the extra scattering due to neutral defects in all devices with a gate length under 40 nm. Source/Drain implantations trace the origins of these defects. Consequently, these particular process steps should gain special care in the design of further node generation as they critically hinder charge mobility at that scale.

1. Introduction

The successive inventions of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), Complementary Metal Oxide Semiconductor (CMOS) and the integrated circuits (ICs) in the 1960s initiated the pace of transistors scaling. In 1967, Gordon Moore observed that the number of transistors in a dense integrated circuit approximately doubled every two years and this pace should continue for at least another decade. Moore’s law has been unexpectedly respected for more than forty years by the microelectronic industries since it has irremediably led to cost reduction per fabricated transistor. It is only since 2012 that the transition time has slightly increased with the introduction of the 22 nm transistor node. Actually, since dimensions shrink, advanced fabrication and new physical phenomena challenge this development. Technological evolutions had to be implemented to reach adequate transistor performances by increasing their frequency operation and reducing their power consumption. The introduction of other channel material and strain engineering [1] in order to boost carrier mobility initially degraded by short channel effects illustrate such evolutions. Another recent advancement is the introduction of high-k dielectric in the metal gate stack at the 45 nm node in order to counter increasing gate leakage [2]. Recently, Tri-Gate MOSFET (as FinFET) has been introduced at the 22 nm transistor node by Intel and they now sell microprocessors with built-in 14nm transistor node. Thanks to their multigate geometry, which confers excellent electrostatic control over the channel, they provide a steeper sub-threshold slope, allowing operation at lower voltage to reduce...
power and/or improve switching speed, resulting in better performance than their planar counterpart [3].

Channel mobility has always been used as a figure of merit in MOS technology since it characterizes well the carrier transport, representative of the transistor global performance. In this study we probed the hole mobility in strained SiGe channel in Tri-Gate pMOSFETs with alternative nanowire (NW) geometry. Such transistors are considered as promising candidates alongside FinFETs to continue scaling without performance loss. From these measurements we extracted the temperature dependence of the low field mobility $\mu_0$ for a wide range of gate lengths and NW widths using the $Y$-function method. The impact of the temperature over the mobility can be used to identify the dominant scattering mechanism in the channel. Overall, we observed that hole transport is predominantly limited by the extra scattering due to neutral defects in all devices with a gate length under 40 nm.

2. Experiments and electrical parameters extraction methodology

2.1. SiGe Tri-Gate pMOSFET fabrication

Tri-gate pMOSFETs were produced at CEA-LETI on 300 mm strained Silicon Germanium on Insulator (SGOI) wafers. Our NW devices are fabricated along the $<110>$ direction. The process flow in figure 1 details the major steps of our fabrication. We first produce the NW using a mesa isolation technique which consists of patterning transistor’s channel width by deep UV photolithography, then trim the resist and etch the substrate before proceeding to successive steps of fin oxidation in order to reduce the diameter as small as $\approx 15$ nm. Next, we deposit the high-k/metal gate stack before same photolithography process described above to pattern the gate and achieve gate length scaled down to 10nm. Moreover, lithography masks had broad range of gate and channel size in order to obtain different panel of devices. Thus, we obtain triple sided gate shape on all NWs. Then offset spacers are added on the sidewall of the gate before silicon raised source/drain, light dose implantation and annealing activation in order to reduce access resistances. Second spacer is added for more protection of the channel from a second highly dose source and drain implantation, activation spike anneal and silicidation. Finally, tungsten contacts and standard Cu back-end-of-the-line processes end the fabrication.

![Figure 1](image)

**Figure 1** a) Process flow of Tri-gate Nanowire MOSFET. b) Top view SEM of a 10nm tri-gate length NW transistor after gate etching and c) TEM of a longitudinal cross-section of the same NW. On b) and c) is highlighted in red the effective channel.

Furthermore, along the single wire MOSFET depicted in figure 1b and 1c, multi wires MOSFETs have also been produced. They consist of ten parallel wires sharing a common Source, Drain and Gate (see figure 2). The multiplication of channels on a single device increases the drain current intensity allowing more accurate parameter extraction for mobility analysis.
2.2. Electrical characterization setup
The electrical characterization was conducted on a manual cryogenic probe station under vacuum using triaxial cables and a semiconductor device analyzer (Agilent B1500). Results presented in this study range from 80K to 350K in order to preserve the devices from special quantum effects appearing usually below 50K [4]. Simple three probes measurements to contact the source, drain and gate of transistors were conducted to record \( I_d(V_g) \) curves. We applied a small Voltage bias on the drain \( (V_d=20 \text{ mV}) \) in order to stay in the linear region of these transistors as required by the Y-function methodology.

2.3. Y-function methodology
As for all MOS technology, Tri-gate MOSFETs have different mobility than bulk for same material. Its effective mobility is described by the electric field penetration into the channel, quantization in the inversion layer and scattering mechanisms and is modeled as follows:

\[
\mu_{\text{eff}}(V_{GS}) = \frac{\mu_0}{1+\theta_1 V_{GT} + \theta_2 V_{GT}^2}
\]  

(1)

where \( \mu_0 \) is the low field mobility and \( \theta_1 \) and \( \theta_2 \) are respectively a linear and a quadratic attenuation factors due to scattering mechanisms.

Then we can express the linear current in a simplified equation at low transverse field as:

\[
I_{\text{lin}}(V_{DS}, V_{GS}) = W C_{ox} \mu_0 V_{DS} V_{GT} L_{\text{eff}} (1+\theta_1 V_{GT})
\]  

(2)

where \( W \) is the width of the device, \( C_{ox} \) is the oxide capacitance and \( L_{\text{eff}} \) is the effective length of the channel. Note that the quadratic term attenuation \( \theta_2 \) related to scattering occurring at the gate oxide/channel interface [5] is neglected as the gate voltage is restricted to 1.5 V. Then, Y-function is defined as the combination of the drain current over its squared root of transconductance as [6],

\[
Y = \frac{I_d}{\sqrt{G_m}} = \frac{W C_{ox} \mu_0 V_{DS}}{L_{\text{eff}}} V_{GT}
\]  

(3)

By canceling the influence of the first order mobility attenuation factors, \( \theta_1 = 0 + (R_{sd} W C_{ox} \mu_0 / L_{\text{eff}}) \), \( R_{sd} \) being the source/drain series resistance, we are able to extract the low-field mobility \( \mu_0 \) from the slope of the Y function provided \( W \), \( C_{ox} \) and \( L_{\text{eff}} \) are known, while the threshold voltage \( V_{th} \) can be read at the x axis intercept. Typical plots of drain current and corresponding Y-function with gate voltage are shown in figure 3.

**Figure 2** SEM of a) single wire and b) multi-wires tri-gate MOSFETs after gate patterning.
3. Results and discussions

3.1. Results

We applied the Y-function methodology in order to extract $\mu_0$ from various devices for a temperature range from 80K to 300K. We report here representative devices with several gate lengths from 400 nm down to 10 nm for fixed 15 nm, 60 nm and 240 nm channel widths. Graphics in figure 4a) display low-field mobility behavior versus gate length at each width. Moreover, each curve within a graphic represents the characteristic of $\mu_0$ at a given temperature. From these data we observe two global trends. Firstly, the low-field mobility decreases along the gate length at the same amplitude for all three devices, meaning only physical phenomena due to variation of gate length are responsible for this mobility attenuation. Secondly, lower temperatures reduce slightly the scattering of the carriers enhancing the mobility in the channel.

In order to interpret the reduction of mobility with smaller gate length, we plotted the same data with different axes where the low-field mobility is now represented in function of temperature (see figure 4b)). Again, we observe similar trend for the low field mobility for each nanowire width (excepted when $W=60$ nm and $L=100$ nm) which depend now on the gate length. For long gate lengths over 40 nm, the mobility increases when the temperature decreases, which is a typical trend for acoustic phonon scattering. However, for gate lengths below 40 nm, the mobility is nearly independent of temperature, which is characteristic of neutral impurity scattering. Thanks to Matthiessen’s rule it is possible to express the mobility within the channel as the sum of its various components in function of temperature as [7, 8]:

$$\frac{1}{\mu_0(T)} = \frac{T}{300\mu_{ph}} + \frac{300}{\mu_c T} + \frac{1}{\mu_{neu}}$$ (4)

where $\mu_{ph}$ is the mobility contribution related to the acoustic phonon, $\mu_c$ is related to remote coulombic interactions while $\mu_{neu}$ is an additional term due to neutral defects [9,10]. Temperature dependences shown in figure 4b) are well fitted with equation (4).

Thus we were able to extract the different components of the mobility for each device. Figure 5 displays the percentage of contribution to low-field mobility scattering from each of its extracted component in respect to the gate length. From these graphics it is clear that scattering due to neutral
defects in the channel prevails over acoustic phonon and coulombic interactions at ultimate gate scaling. For 15nm nanowire width and gate length of 10 nm, neutral defects scattering represents over 90% of mobility attenuation. Its contribution fades for longer gate length but holds majority for narrower wires, when for wider devices (W=240 nm) we get back to acoustic phonon-dominated scattering.

![Graphs showing mobility and scattering contributions](image)

**Figure 4** a) Low-field mobility $\mu_0$ extracted with Y-function in function of gate length. Within a graph each curve represents $\mu_0$ behavior for a distinctive temperature. b) $\mu_0$ in function of temperature for different gate lengths. All fits let us to extract the different mobility components at each gate length.

![Graphs showing percentage of scattering contributions](image)

**Figure 5** Percentage of contribution to scattering from each mobility component in respect to the gate length.
3.2. Discussions
As shown in the previous paragraph, neutral defects in short channel wires dominates scattering considerably over acoustic phonon and coulombic interactions. Origin of these defects are subjected to interpretations, thus we expose here our understanding of the phenomenon. We believe these defects are introduced after implantation of doping of the source and drain areas. At this stage of the fabrication, the channel under the gate is protected by a first set of spacers at both sides of the gate. Thus, the ions and interstitial atoms created in the SiGe crystal by the implantation are believed to be injected from the source and drain into the channel ends. Naturally, these devices are still in development and will need further adjustments to match industrial need. Improvement of low-field mobility for smaller devices should arise from better controlled doping and annealing steps during fabrication, in particular in-situ doped source/drain process without implantation could help in this respect. As an alternative, spacer size could also be adjusted to reduce the injection of these defects into the channel. Moreover, at this development stage, the temperature-independent mobility behaviour of our devices induces cooling will not enhance their electrical properties, resulting in low current intensity at any temperature.

4. Conclusions
In this work we characterized hole mobility within the channel of Si$_{0.7}$Ge$_{0.3}$ Tri-gate pMOSFETs over a 80K - 350K temperature range. Hole mobility from various devices in gate lengths and widths is extracted using the Y-function method in order to remove the attenuation from the source and drain series resistances. Then, the influence of temperature over the low-field mobility is used to identify the dominant scattering mechanisms in the channel. In particular, we discriminated the scattering components using Matthiessen’s rule into phonon, coulombic and neutral defects scattering mechanisms. We identified strong mobility attenuation due to neutral defects in all devices from 40 nm gate length and below, regardless of their width, due to independent temperature behavior. Specifically for 15 nm gate length devices, neutral defects scattering represents over 90% of mobility attenuation. We believe Source/Drain implantations trace the origins of these defects. Therefore, these process steps should gain special care in the design of further node generation as they limit charge mobility at that scale.

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References
[1] Takagi S, Hoyt J-L, Welser J-J and Gibbons J-F Comparative study of phonon-limited mobility of two-dimensional electrons in strained and unstrained Si metal-oxide-semiconductor-field-effect-transistors 1996 J. Appl. Phys 80 1567
[2] Wallace R-M and Wilk G-D Materials issues in high-k gate dielectric selection and integration 2005 High Dielectric Constant Materials: VLSI MOSFET applications (Springer Berlin Heidelberg).
[3] Auth C, Allen C, Blattner A, Bergstrom D, Brazier M,Bost M, Buelher M, Chikarmane V, Ghani T, Glassman T, Grover R, Han W, Hanken D, Hattendorf M, Hentges P, Heussner R, Hicks J, Ingerly D, Jain P, Jaloviar S, James R, Jones D, Jopling J, Joshi S, Kenyon C, Liu H, McFadden R, McIntyre B, Neirynck J, Parker C, Pipes L, Post I, Pradhan S, Prince M, Ramey S, Reynolds T, Roesler J, Sandford J, Seiple J, Smith P, Thomas C, Towner D, Troeger T, Weber C, Yashar P, Zawadzki K and Mistry K. A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors 2012 Symposium on VLSI Technology (VLSIT)
[4] Lavieville R, Triozon F, Barraud S, Corna A, Jehl X, Sanquer M, Li J, Abisset A, Duchemin I and Niquet Y-M. Quantum Dot Made in Metal Oxide Silicon-Nanowire Field Effect Transistor Working at Room Temperature 2015 Nano Lett, 15, 2958.

[5] Ong T-C, KO P-K and Hu C, gate-Oxide MOSFET's at 77 K 1987 IEEE Trans. Electron Devices 34, 2129

[6] Ghibaudo G. New method for the extraction of MOSFET parameters. 1988 Electron Lett 24(9):543-5

[7] Cros A, Romanjek K, Fleury D, Harrison S, Cerutti1 R, Coronell P, Dumont B, Pouydebasque A, Wacquez R, Duriez B, Gwoziecki R, Boeuf F, Brut H, Ghibaudo G and Skotnicki T, Unexpected mobility degradation for very short devices : A new challenge for CMOS scaling. 2006 IEEE Proc. IEDM, 439-402

[8] Shin M, Shi M, Mouis M, Cros A, Josse E, Kim G-T, Ghibaudo G, Low temperature characterization of mobility in 14 nm FD-SOI CMOS devices under interface coupling conditions. 2015 108 30-35

[9] N. Sclar. Neutral Impurity Scattering in Semiconductors. 1956 Phys. Rev., 104, 6, 1559–1561

[10] T.C. McGill et R. Baron. Neutral impurity scattering in semiconductors. 1975 Physical Review B, 11, 5208–5210