Study on Power Minimization techniques in SAR ADC Devices by Using Comparators Circuits

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Abstract. Comparators play an important role in designing of SAR ADC. In this paper we achieve the required performance of SAR ADC at minimum power usage. Using of comparators will reduce the power and noise, Dynamic latch circuit used in comparator increases the speed. The differential amplifier is also discussed. Here we will get to know about Ramp ADC and also about various DAC’s like M-DAC and AUX-DAC. The time-interleaving technique is the design technique that is used to increase the speed.

Keywords: Comparator, SAR ADC, Dynamic latch comparator, Differential amplifier.

1. Introduction

Power consumption is the major problem which arises in the SAR devices. So we use different types of comparators in SAR for reducing the power. A Successive approximation register (SAR) ADC digitizes a continuous analog waveform [1]. SAR ADC comprises of three primary constituents which are ADC, SAR logic and a comparator [2]. ADC converts analog signals to digital signals and in SAR logic specimen signal and the DAC output signals are matched using the comparator [2]. A Comparator is a device which matches two analog inputs and provides the digital output depending upon which input is higher. It also compares two input voltages or currents. We use comparators for various applications. Using comparators, we can increase the speed or reduce the power consumption. SAR ADC is used mainly because it consumes low power and its speed and has a very good resolution. Comparators are of two types, namely1. Static comparators and 2. Dynamic comparators. Static comparators consist of amplifiers, while dynamic comparators consist of low gain amplifier connected to the latch circuit [1]. For improving the speed of the SAR ADC’s we use different type of design techniques i.e., time-interleaving technique and we should increase the conversion bits for each time [3]. We should design a SAR ADC such that it consumes low voltage and noise should be reduced [4]. We attach a capacitor loading at the output of the comparator to reduce the noise but it increases the power consumption and proceeds with low speed. Using voltage-controlled delay line (VCDL) with positive feedback and phase detector which works on adaptive time domain (ATD) with adaptive
oscillation circuit (AOC) decreases the noise effect. Generally we use dynamic comparators for reducing the power in SAR ADC.

Now-a-days, in microelectronic digital communication system- analog to digital convertors play an important role because they connect analog and digital systems. As the technology is increasing day by day in CMOS, the signal processing functions are used in digital system for decreasing cost and consumes less power, higher yielding . It plays an important role whenever the data from analog form to the digital form by processing over sensors or transducers and when chips are fabricated in the same circuit panel then data between them can be transmitted with wireless connection and with more fast transmission power. Based on the application requirements they are different type of ADC’s depending upon high speed, converting low resolution power to high resolution power, when more samples obtained with time lagging and in noise presence. For the resolution in ADC, after the certain number of cycles are completed, the digital signal which is stored in the SAR equivalents to the analog signal with particular quantization error and generates one bit per clock cycle. It occupies low area, wide range applicable and high resolution. SAR uses high resolution ADC.

This paper discusses about the comparator and successive approximation register. In section 2 we discussed about the comparator and its operation and how a dynamic latch based comparator is modified further. In section 3 we will learn about working of SAR ADC and also functioning of Differential amplifier using block diagrams.

2. Literature Review

In today world, there are different types of comparators are present. The LM111 family of comparator was the earliest type of comparator. The LM119 family of comparators are high speed comparators, which need lower power supply voltages for the differential voltages. Rail to rail comparators from LM139 family consists of p-n-p transistors, which takes only input potential to drop of 0.3 volts lower than the negative supply rail and these comparators do not permit it to increase beyond the positive rail. LMH7322 are ultra-fast comparators which permits the input signal to operate above the positive rail and lower than the negative rail by a small margin of 0.2v.

Based on 90nm CMOS technology, there are different type of comparators are manufactured. The type of dynamic comparators along with output buffer circuit which was proposed is discussed in next sections.

Conventional dynamic comparator: Pre-amplifier and the latch are the phases in the computer. This comparator consists of inverting and non-inverting terminals in which input signal is given to the non-inverting terminal and a reference signal is given to the inverting terminal. Cross coupling of inverters helps in forming latch. The charging of the nodes of the comparator goes to VDD through the reset stage. The clock will be higher when the comparator passes through decision phase. The discharging of nodes occurs in the decision phase. When differential voltage flows through the circuit the latch that was in the dynamic comparator creates separation to the inputs and outputs due to the change in inputs provided. The inputs to the latch stage are selected in such a way that it provides perfect speed and enhances the load further. The pre-amplifier stage uses more power than the latch stage because of voltage provided and speed. The original dynamic latch based comparator was proposed to operate in two differential modes due to clock applied. They are the reset phase and the assessment phase. The output nodes in the reset stage where clock applied equals to ‘zero’ charges to supply voltage. The output is dependent on the input which is produced by the output node when clock applied equals to ‘1’ in the evaluation phase. The regenerative latch converts the data received into the complete digital values. The drawback in this type of comparator is that it requires more time to charge the capacitances in the output stage during the reset phase. This will result in decreasing the speed of the comparator. The dynamic latch based comparator was further developed which increases the speed and the time lag for the data receiving is decreased. The dynamic power consumption is avoided by the switching transistors of SM1, SM2 and also the differential outputs are charged to VDD by the control transistor CM1, CM2. In this comparator during the reset phase where clock equals to ‘0’ the
control transistors CM1 and CM2 are off which are cross coupled as the M4 and M5 of PMOS transistors which are already charged to VDD. When clock equals to ‘1’ in the evaluation phase, the NMOS of the tail transistor M1 goes ON and based on the voltages of the input transistors M2, M3: the output points drops to various rates. The transistor will drop the potential at the drain terminal when input voltage of transistor which is higher takes the more current and by making either one of the control transistor ON and other control transistor is OFF. It will result in discharging one of the output terminals, to zero voltage and the other terminal will have more voltage. By proposed design of the dynamic latch based comparator we can increase the speed and the no delay time in receiving the data [5].

3. Design Procedure

COMPARATOR

Comparator is a device that compares the voltage or current at the two input terminal and converts it into a digital signal. The comparator consists of two inputs one is inverting terminal and another one is non-inverting comparator. \( V_+ \) and \( V_- \) are the two analog input terminals of the comparator and the output signal is \( V_0 \)

\[
V_0 = \begin{cases} 
1; & V_+ > V_- \\
0; & V_+ < V_- 
\end{cases}
\]

A comparator consists of specific high gain differential amplifier. It is mostly found in devices that convert analog signals to digital signals such as ADC and also relaxation oscillators. Hence the output of comparator is given to SAR ADC.

Where, A Successive approximation ADC uses the binary search method by quantizing all the levels before converging on a digital output to convert a continuous analog signal into discrete digital signal [1]. It is mostly widely used ADC method. The basic norm of this type of SAR ADC is that the input signal is estimated to an n-bit digital value one bit at a time, starting with the MSB. The method of 4 bit conversion using successive approximation process is discussed below. The input voltage range is successively divided by half. The following steps are explained below. (1) In MSB we set 1 as initially and the rest of the bits are set as 000. The unknown analog output is being compared with digital equivalent voltage. (2) If digital equivalent signal is lesser than the analog input signal, then the MSB is continued as 1 and a second MSB is put to 1. Or else, first MSB is put to 0 and the second MSB is put to 1. Here the contrast is decided as in step (1) to choose to continue or rest the second MSB.

**Successive Approximation ADC**
Where, SOC is Start of Conversion and EOC is End of Conversion. The block diagram of successive approximation ADC is as shown in Fig. 2. In this method, a successive approximation register is used to generate an approximated bit stream for an analog voltage signal. The successive approximation register can generate bit stream according to the output of comparator. Successive approximation register (SAR), DAC and comparator are present in ADC. The input of n-bit DAC is taken from the output of SAR. The non-inverting input of the comparator is applied to the equivalent analog output potential difference of DAC. The unidentified analog input voltage VA is given as the second input to the comparator. The successive approximation logic of SAR is activated by using the output of the comparator.

When the start command is applied the MSB is set to logic 1 by the SAR and the other bits are made logic 0, so the trial code becomes 1000.

The SAC logic is:

1) If C=1, then MSB(i) is made “1”.
2) If C=0, then MSB(i) is made “1” and MSB(i-1) is made “0”.

Where i = Iteration number.

The DAC output voltage is, \[ V_D = \frac{8(D_3)+4(D_2)+2(D_1)+D_0}{16} \]

Here, MSB levels are \( D_3 = \text{MSB}_1 \), \( D_2 = \text{MSB}_2 \), \( D_1 = \text{MSB}_3 \), \( D_0 = \text{MSB}_4 \)

\[ Table 1: \text{Tabular form results} \]

| Iteration Number | \( V_i=V_+ \) | \( V_D=V_- \) | Condition | C   | D3 D2 D1 D0 | VD(i+1) |
|------------------|---------------|---------------|-----------|-----|-------------|---------|
| i=1              | 11.7V         | 0V            | \( V_+ > V_- \) | 1   | 1000        | 8V      |
| i=2              | 11.7V         | 8V            | \( V_+ > V_- \) | 1   | 1 1 0 0     | 12V     |
| i=3              | 11.7V         | 12V           | \( V_+ < V_- \) | 0   | 1 0 1 0     | 10V     |
| i=4              | 11.7V         | 10V           | \( V_+ > V_- \) | 1   | 1 0 1 1     | 11V     |
| i=5              | 11.7V         | 11V           | \( V_+ > V_- \) | 1   | 1 0 1 1     | 11V     |
After N = 4 Iterations, latch will be enabled to store the output data. Thus, the analog signal can be converted into digital data signal using successive approximation ADC.

**Block Diagram of Differential Amplifier**

The block diagram of Differential Amplifier is shown below in Fig. 3. Using DAC generation of quantization steps is processed and binary search algorithm is used for finding then input signal that is nearer to it. For this the input that is used will be already sampled during conversion. The sequential order of the bits from LSB to MSB is decided by control logic of SAR depending upon the decision generated by the comparator. The LSB bit place in the SAR ADC is designed in such a way that it faces the strongest noise requirements. Higher RMS noise is needed so the comparator noise does not affect the performance of ADC.

![Block diagram of Differential Amplifier](image)

**Figure 3:** Block diagram of Differential Amplifier

Due to the difference in the distribution of signal voltage at the comparator input for each bit phase creates a difference in effect of comparator noise over performance of each bit step. This tells us that the power consumption can be reduced by using different comparators for different cycles of the bits. Majority –vote comparison is the method that is used to realize the variable noise comparator. The disadvantage in using this method multiple times over a bit cycle creates reduction in its applications to low frequencies.

To overcome this and to make the operation faster switching of SAR ADC over different comparators that has different noise variances. So this paper theoretically tells us about the performance by reduction in usage of power can be obtained using optimal comparators.

The analysis of SAR ADC response is explained using simple mathematical model. Secondly based on the power requirements, equations are derived for obtaining the allocation of the noise in each bit cycle and then we analyze the less number of comparators that can be used for this process.

**4. Applications**

Successive approximation ADC (Analog- to-Digital Convertor) is mostly used application among the different applications that has been advanced from many ADC execution schemes. The SAR ADC is used to get various advantages due to this the power consumed will be low, the resolution is high, there will be no time lag when the data received in the output because of small size [1].In space applications Delta Sigma Analog-to-Digital Convertors are used over a great extent. So that we need to have some applications such as frequency should be high and also the infallibility is high. The application we used is consecutively approximated data in Ramp ADC’s but only in a collinear
manner. Because of this the major drawback we get is the more time lags that may lead to variation in computed digital output [6]. M-DAC and AUX-DAC are the two DAC in ADC and also a shared interpolator and comparators are of four groups. M-DAC is required for sampling the input signal and executing the successive approximation logic. The threshold voltage is produced by the AUX-DAC for comparison cycle [7].

5. Result

The result shows that, by using a greater number of comparators we can decrease the noise and in 10b and 12b SAR ADC devices we can save the power upto 50% and 60% by using 10 to 12 comparators.

6. Conclusion

In this paper we decrease the power, time delay and increased the speed of Successive Approximation ADC by using a comparator of dynamic latch-based comparator. Latch is enabled to store output data after n=4 iterations. Hence, in successive approximation ADC we converted analog signal into digital data signal. Hence, we can conclude that comparator plays a major role in SAR ADC to get required data output.

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