Readout electronics of the ALICE photon spectrometer

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Abstract. The photon spectrometer (PHOS) in the ALICE experiment at LHC is a PbWO₄ crystal based electromagnetic calorimeter, dedicated to measuring photons, π⁰’s and η’s over a broad p_T range from about 100 MeV/c to 100 GeV/c with the best possible energy and position resolution. The front-end electronics of the PHOS is thus required to cover a large dynamic range, to achieve a timing resolution better than ∼ 2 ns in order to discriminate against 1-2 GeV/c (anti-)neutrons, and to provide high p_T trigger to select rare high p_T events. In this paper, we present the full PHOS readout system, including the avalanche photo-diode, the low-noise charge sensitive preamplifier, the 32 channel front-end electronics card, the trigger region unit and the trigger OR module. Results from PHOS commissioning with beam particles and cosmic rays will also be presented to address the performance of the PHOS readout electronics.

1. Introduction

ALICE [1, 2] is a general-purpose heavy-ion experiment designed to study the properties of the quark matter produced in ultra-relativistic heavy-ion collisions at LHC by comprehensive measurements of hadrons, leptons and photons. Photons produced throughout all stages of the collision are believed to carry important information on the evolution of the colliding system. The ALICE photon spectrometer (PHOS) [3] is designated to measure photons, π⁰’s and η’s over a wide p_T range with the aim of exploring thermal and dynamical properties of the initial phase of the collisions through low p_T direct thermal photon measurements and studying parton energy losses through the measurements of high p_T π⁰ and γ-jet correlations.

PHOS is a highly segmented electromagnetic calorimeter with individual detection cells made of very dense PbWO₄ (PWO) material with dimensions of 2.2×2.2×18 cm³. PHOS is subdivided into five PHOS modules and positioned at the bottom of the ALICE setup with a distance of 4.6 m to the nominal interaction point. A PHOS module contains 56 × 64 detection channels and subtends 0.24 in pseudo-rapidity and 20° in azimuth. Each crystal is optically coupled to an Avalanche Photo-Diode (APD), which is connected to a low-noise Charge-Sensitive Preamplifier (CSP). To increase significantly the light yield of the PWO crystal (by a factor of ∼ 3 compared...
to that at room temperature), the detector is located in a “cold” volume operated at \(-25^\circ C\) with a precision better than 0.3\(^{\circ}\)C, whereas the readout electronics is separated by an insulation layer from the “cold” volume.

2. PHOS readout and trigger

The schematic overview of PHOS readout system is shown in Fig. 1. Light induced by incident particles is detected by APDs and the resulted charge is converted into a voltage signal by a CSP. 32 CSP output signals are readout via a PHOS FEE card [4], in which the signals are shaped in dual shapers with different gains, and then digitized with the 10 bit ALICE TPC Readout (ALTRO) chip [5] for a 14-bit effective dynamic range, covering a full energy range of 80 GeV with a least significant bit of 5 MeV.

The FEE also regulates the individual bias voltage between 210 and 400 V for each of the 32 APDs. The setup, control and readout of the FEE cards occurs over a custom GTL bus under mastership of a Readout and Control Unit (RCU) card [6]. Each RCU card masters 28 PHOS FEE cards. The RCU carries a Detector Control System (DCS) daughter card which provides control via a Linux operating system by Ethernet connection and provides the interface to the central trigger processor (CTP). The RCU carries an ALICE Source Interface Unit (SIU) card for transmission of data via an ALICE Detector Data Link (DDL) to the ALICE DAQ and high level trigger (HLT) system. Upon reception of a Level 1 (L1) trigger from LTU [7], the RCU sends via the GTL back-plane a strobe signal to all ALTRO chips in the FEE, which enables the storing of ADC samples of the triggered event in readout buffers. Data in these buffers are either transmitted via the RCU through a DDL to the DAQ and HLT system or discarded depending on whether L2a trigger arrives in \(\sim 88\ \mu s\).

PHOS also provides input to the Level 0 (L0) and L1 trigger decisions in ALICE. The signals of \(2 \times 2\) detection channels are analog summed via a fast shaper in the FEE boards and transmitted via short cable to a local Trigger Region Unit (TRU) board, where trigger data are
digitized and processed by the trigger algorithm implemented in FPGA to generate local L0 yes/no decision. Both L0 decision and the digitized trigger data are transmitted to the Trigger OR (TOR) board. TOR multiplexes the L0 decisions of all TRUs and generates global L1 trigger decisions.

The front-end electronics of one PHOS module consists of 112 FEE boards each processing the signal from 32 crystals, eight TRU boards each covering a region of $28 \times 16$ crystals, and 4 RCU boards each serving two branches of 14 FEE boards and 1 TRU board through GTL buses.

2.1. APD and charge sensitive preamplifier

PHOS uses the Hamamatsu S8148 (S8664-55) type APDs, which has an active area of $5 \times 5 \text{ mm}^2$. The gain $M$ of an APD increases with decreasing temperature, typically by a factor of 3 at $-20^\circ \text{C}$ compared to that at $20^\circ \text{C}$, with a bias voltage of 350 V. The voltage coefficient of the gain $\frac{dM}{dV}$ increases with gain, which in turn increases with increasing bias voltage. Even with the same reverse-bias voltage, there is a considerable spread of the gain factors for production batches. Thus, to choose a nominal APD gain factor, a compromise is required between a high signal gain, noise and signal stability. To achieve best energy resolution, the APDs are decided to be operated at moderate gain of 50, which corresponds to a reverse-bias voltage of $\sim 300\text{-}390$ V at operating temperature of $-25^\circ \text{C}$. This choice has a lower excess noise which has a direct effect on the stochastic term of the energy resolution. More importantly, a low gain keeps the gain dependencies on temperature and voltage low. These dependencies have an important impact on the constant term of the energy resolution. Particularly, the programmable gain inter-calibration is limited if the gain is set too high. With a gain dependence of 3.3% per V at APD gain of 50, an inter-calibration precision of 0.66% is achievable with a bias voltage increment of 0.2 V/bit.

A charge-sensitive preamplifier [8] on a printed circuit board of area $19 \times 19 \text{ mm}^2$ is mounted to the back side of the APD. The CSP produces an output voltage step which is proportional to the charge collected by APD on its input capacitance and inversely proportional to the feedback capacitor $C_f$. With effective $C_f$ value of 1.2 pF, the amplifier gain is around 0.833 V/pC or 0.133 $\mu V/e^-$. Taking into account the detector surface and quantum efficiency of APD, about 200 electrons per MeV are generated in the APD by primary electromagnetic particles at the PHOS operating temperature of $-25^\circ \text{C}$. Thus, the corresponding voltage signal at the preamplifier output is 26.7 $\mu V/\text{MeV}$.

2.2. Front-end electronics card

To extract a direct photon signal from a huge background of decay photons from neutral mesons (mainly $\pi^0$ and $\eta$), it is necessary for PHOS to achieve a good energy and position resolution. It is desired for PHOS FEE to have an electronic noise per channel of 5 MeV or less, and also a high inter-calibration precision of APD gain and uniformity across all channels.

Fig. 2 shows a photograph of the final 32-channel FEE card. To cover a large dynamic range with optimal energy resolution, 64 second-order (CR-RC2) signal shapers are implemented on a 10-layer board with a gain ratio of $\sim 16$ for high and low gain, digitized separately with 10 bit ADCs contained in 4 ALTRO-16 chips. A shaping time of 1 $\mu s$ has been adopted for the shapers in order to achieve a good timing resolution to discriminate against 1-2 GeV/c (anti-)neutrons. For each CSP input channel, a low noise buffer of gain 2 separates the combined RC differentiator/pole-zero network from the two active Bessel filters. The high gain shaper passes the low energy signals from 5 MeV to 5.12 GeV into the 1 V input range of the 10 bit ADC. With a total gain of 7.2, the low energy range shaper features an optimal RMS noise of 0.62 ADC counts with connected detector at APD gain $M=50$. The high energy range shaper applies an attenuation of 0.45 in order to fit high-energy CSP signal amplitudes of up to 2.4 V into the 1 V
ADC window covering a energy range from 80 MeV to 81.92 GeV. The effective dynamic range is 14 bits. The semi-Gaussian pulse-shapes are digitized by the ALTRO-16 chip, which contains multiple buffers of up to 512 samples for each ADC channel. With a sampling frequency up to 10 MHz, a pipe-lined multi-event buffer inside the ALTRO is loaded with triggered events that can be readout via a custom GTL bus and used in off-line analysis to extract the energy and timing information by fitting the reconstructed pulse shape in time domain to a $\Gamma^2$ function [9].

The FEE card implements also 32 individual high-voltage bias controllers for gain control of all connected APDs. Each APD bias is set via a 10 bit digital value, converted by a 10 bit DAC with a bias voltage increment of 0.2 V/bit in the range of 210-400 V, giving a gain resolution of 0.66% at APD gain of 50. Each DAC is controlled via the Motorola SPI serial bus, mastered by the FEE board controller implemented in FPGA.

The FEE board controller, shown in Fig. 3, controls and monitors access to the FEE card resources. The RCU I²C slave logic allows RCU address-mapped access to both the control and data sections of the FEE cards. The address spaces include ALTRO-chip internal registers, APD bias control registers, registers for monitoring voltages, currents and temperatures.

For trigger purposes, the sums of $2 \times 2$ analog signals are processed through a fast shaper amplifier on the FEE board and transferred into the TRU for further processing.

2.3. Trigger region unit

The TRU has been designed [10] to receive 112 fast OR signals from 14 FEE cards and to generate threshold triggers based on charge sums over $4 \times 4$ sliding windows over 448 channels. Octal, 12 bit 40 MHz Flash ADCs of 170 ns conversion time with serial outputs are used to digitize all 112 fast $2 \times 2$ analog sum signals and concentrate 112 Fast OR streams into a single Virtex FPGA. Fig. 4 is a block diagram of the TRU board controller. The trigger algorithm implemented in the Trigger Module of the FPGA calculates in parallel all $4 \times 4$ sliding window sums of the digitized energy signals from the trigger region and makes local L0 yes/no decision.
within 250 ns by searching for charge above threshold in $4 \times 4$ APD areas. Both L0 decision and the digitized 12-bit $2 \times 2$ sum trigger data for the global L1 processing are transmitted to TOR unit via LVDS cables. In addition, for offline analysis, raw $2 \times 2$ samples from the ADCs with the 2 least significant bit truncated can be readout similar to the FEE card via RCU and appended to the event stream through the “Fake ALTRO” mechanism [11] implemented in TRU board controller.

3. PHOS performance

The performance of PHOS FEE has been studied extensively with FEE prototypes and final products at laboratory with LED pulse and at T10 beam line of the CERN PS during the commissioning of PHOS module. The first PHOS module was assembled in 2006 for calibration at CERN PS. Calibration and measurements of the energy resolution were carried out at operating temperature of $-17^\circ C$. Calibration of energy gain was obtained with 2 GeV electron beam for approximately 2/3 of the detection channels and it was found that the gains of the detection channels could be equalized to $\sim 4\%$ by adjusting the APD bias voltage. The response from different channels can be equalized to very high precision via offline calibration. Enough data were accumulated to estimate the energy resolution at 1, 2, 3, 4 and 5 GeV. The results are shown in Fig. 5 as a function of energy together with previous results from the PHOS prototype at $-25^\circ C$. The measured energy resolution of the first PHOS module is consistent with previous results from prototype and fulfills the PHOS requirement.

While PHOS trigger commissioning is ongoing, cosmic data taken last year with PHOS L0 trigger show the energy distribution of all clusters (mainly single crystal clusters) in PHOS module 2 peak at the right energy position of 210 MeV, indicating that L0 trigger algorithm works as expected. Test on PHOS L0 trigger latency shows that PHOS L0 decisions arrive at the ALICE CTP within 800 ns. For detailed results on PHOS trigger commissioning, please refer to Ref. [12] in this proceedings.

4. Conclusion

We have presented in this paper the full readout electronics of the ALICE PHOS. The performance studies show that PHOS readout electronics are overall in very good shape. While PHOS trigger commissioning is ongoing, commissioning results have already shown that PHOS trigger makes correct L0 decision within ALICE L0 trigger latency.
Figure 5. Energy resolution measured in 2006 with the first PHOS module together with previous results from the PHOS prototype.

Acknowledgments
This work is supported by the NSFC under Grant Nos. 10975061, 10875051 and 10635020, the Chinese Ministry of Education under Key Grant No. 306022, the Research Council of Norway (NFR), the Federal Agency of Science of the Ministry of Education and Science of Russian Federation, International Science and Technology Center, Russian Academy of Sciences, Russian Federal Agency of Atomic Energy, Russian Federal Agency for Science and Innovations, CERN-INTAS, and the ALICE CERN team.

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