A Novel Framework for Dataset Generation for profiling Disassembly attacks using Side-Channel Leakages and Deep Neural Networks

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Abstract
Various studies among side-channel attacks have tried to extract information through leakages from electronic devices to reach the instruction flow of some appliances. However, previous methods highly depend on the resolution of traced data. Obtaining low-noise traces is not always feasible in real attack scenarios. This study proposes two deep models to extract low and high-level features from side-channel traces and classify them to related instructions. We aim to evaluate the accuracy of a side-channel attack on low-resolution data with a more robust feature extractor thanks to neural networks. As investigated, instruction flow in real programs is predictable and follows specific distributions. This leads to proposing a LSTM model to estimate these distributions, which could expedite the reverse engineering process and also raise the accuracy. The proposed model for leakage classification reaches 54.58% accuracy on average and outperforms other existing methods on our datasets. Also, LSTM model reaches 94.39% accuracy for instruction prediction on standard implementation of cryptographic algorithms.

Keywords: Reverse Engineering, Side Channel Analysis, Deep Neural Networks, Convolutional Neural Networks

1 Introduction
Reverse engineering using side-channel analysis has become more critical in hardware security in the last two decades due to its ability to extract information from target hardware. Technically speaking, reverse engineering aims to assign a related label to each side channel trace. This label could be a bit in bit-level attack scenarios, where the target is a single bit, or an instruction in instruction-level attacks, in which the target is an instruction. Extracting a specific bit or instruction relies on the amount of information leaks from the target device. Obtaining high resolution data during profiling phase is required in a bit-level attack because the target is one bit. On the other hand, for instruction-level attacks, the target is to find a sequence of bits representing an instruction for which we are looking. It seems that deploying an instruction-level attack is more practical in low sample rates with lower-cost tools.

Although many statistical methods have been developed in the last two decades to disassemble a target microprocessor using side-channel information, reaching high accuracy in such attacks with low-resolution data is still an open problem. These methods suffer from a common problem, i.e.,
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Deploying a reverse engineering attack using side-channel information includes two phases: the profiling phase and the attack phase. In the first phase, the attacker obtains enough knowledge about the processor of the target device. This phase includes gathering side-channel traces while the device is running some instructions. The amount and quality of leakage in this phase is various depending on the different scenarios are running. In this case, the attacker may use different sequences of instructions to gather a dataset that spans as much as possible situations that might happen. Subsequently, this data is applied to model the leakage of the target device and later be used in real attack scenarios. The generalization of this method is based on multiple factors such as noise level, the pipeline of the target device, and the ability of the model to estimate the behavior of the target device.

Recently, most of the proposed methods aim to solve this barrier by estimating the leakage and recognizing instructions from their related traces [2–5]. These references evaluate their proposed methodologies in real attack scenarios. However, they have some strict assumptions on their target devices and attack scenarios which lead to severe defects including:

- Employing high-cost measurement tools (high resolution data)
- Using minority instructions of the target device’s instruction set
- Target devices are mostly PIC which have a simple pipeline

Most state-of-the-art articles suffer from these critical issues, which are mostly not satisfied in real attack scenarios or require expensive experimental tools. In this study, we will show that employing a well-designed model for feature extraction could distinguish instructions from their leakage, even in low sample rates.

This study uses convolutional neural networks (CNNs) for feature extraction from side-channel traces and a fully connected (FC) layer for classifying extracted features. Since 2012, CNNs have proved to outperform most of the state-of-the-art algorithms in signal processing [6]. These networks are robust against shifting and scaling due to the localization they apply to the input, leading to spatial feature extraction. This robustness lets these architectures get more information from traces, hence make them appropriate for side channel attacks. Training such a CNN requires labeled dataset including traces and related instructions. Therefore, due to the lack of an open dataset a custom one has been gathered in this work. The recorded traces should be gathered from random-order instructions to span all possible sequences of instructions while it should be balanced. We will discuss more about the proposed data gathering mechanisms in section 3.

As mentioned, the proposed dataset should be as general as possible to contain the most plausible types of instruction sequences. However, if the attacker obtains knowledge about the target device code and figures out what type of code is running on it, then the instruction set could be limited. This limitation lets the model distinguish traces better because of an elimination of some possible labels. Furthermore, instruction flow in some specific programs is predictable which means that instructions do not follow each other randomly as assumed before. In fact, they follow some probability distributions. An algorithm based on Long-Short Term Memory (LSTM) would be proposed to estimate these distributions. LSTM is a deep neural network which can learn and memorize temporal features in its hidden states. This network is very effective, especially dealing with time series. However, its hidden states increase the number of learning parameters, which imposes more data and more computational power. An instruction frequency analysis model is proposed in the section 4 based on LSTM to analyze and estimate the instruction flow in a target device on which a specific code is running.

Our Contribution

We first design a scheme to generate assembly programs, including random instructions and random register values. Then, a customized version of an open-source simulator is employed to simulate generated random programs and extract run time labels. These labels are then used in a supervised learning procedure to train a deep CNN model on gathered traces. Furthermore, a tool including random instruction generator along with a customized simulator is designed to simplify the profiling phase in performing the side-channel
attack (SCA). Two deep neural network models based on CNN architecture are proposed to extract features from side-channel traces for leakage estimation. Then, a FC layer will be used to assign a label to each trace. After training this network, LSTM model is employed to estimate the probability distribution of instructions for standard implementation of cryptographic algorithms.

The achieved results show that using CNN for feature extraction and classification of side-channel traces have more generalization and outperform state-of-the-art reverse engineering models for especially low-resolution traces. Besides, LSTM model could reduce the possible instructions in the training phase when the attacker possesses information about the type of program running on the target device. Finally, a discussion about the proposed method and its practicability is presented. Also a table including the instruction recognition probability is proposed, which determines the leakage for each instruction.

2 Related Works

Several researchers around the world have tried to use side-channel analysis to extract information from devices [5, 7–9]. This information could be employed to extract a hidden key for a cryptography algorithm or to reverse the whole procedure of the device. A SCA could be modeled as a classification problem in which the classification is used for a hidden key extraction or for instructions detection. Since SCA can be interpreted as assigning a label or instruction to specific trace, the machine learning solution for classification can be used as a suitable approach for researchers.

From key extraction point of view, Quisquater et al. employed self organizing map (SOM) for instruction recognition of a de-packaged processor [2]. Later, least squares support vector machine (LS-SVM) [3] is exploited to extract the key of an advanced encryption standard (AES) with no countermeasures [4]. Their achieved results show that LS-SVM with RBF kernel could outperform template attack (TA) [5] on their dataset. Lerman et al. evaluated different machine learning methods, including SOM, SVM, and random forest (RF) on the implementations of triple data encryption standard (3-DES) and RSA-512 on FPGA [10]. They later provided results of high dimension data in the profiling phase and compared TA with RF and SVM [11]. They indicated that TA performs better if points of interest could be recognized for data. However, RF can result in better for high dimensional traces. In [12], it is also indicated the superiority of machine learning techniques compared to TA while dealing with limited traces. Thereafter, Cristiani et al. introduced a mutual information estimator based on multi-layer perceptron (MLP) to extract features between input bits and traces [13]. The proposed method was evaluated with AES implementation on a PIC microcontroller while electromagnetic (EM) traces was used from multiple probe positions. In 2017, ELMO (leakage simulator for the ARM Cortex-M0) was developed to model second-order bit-interaction terms [14]. This work was proposed based on the linear regression-based leakage modeling for ARM Cortex-M0 and Cortex-M4 [15]. However, it is claimed that ELMO could not second-order leakages as the original paper stated [16]. As the reviewed papers discussed, machine learning techniques outperform classic methods such as TA, and they are more capable of dealing with high dimensional data [17].

Extracting the hidden key of a cryptographic function is not the sole approach in side-channel analysis. The leaked information could be employed for reverse engineering and disassembling the bit flow of the whole program. ML techniques are widely used in reverse engineering problems. In bit-level approaches, Cristiani et al. presented a disassembler utilizing EM radiations of the target device to extract the entire processed bits [18]. Their success rate on a PIC microcontroller was 99.41%. Nonetheless, deploying such attack requires precise measurement devices to fix the probe on desired positions and record the traces. Among instruction-level attack scenarios, a multivariate normal model was employed to estimate the templates of instruction classes [19]. The authors have utilized principal component analysis (PCA) [20] and linear discriminant analysis (LDA) for dimensionality reduction and feature selection. The result of this method on 35 instructions from PIC was 70.1%. In other work, a SCA was deployed on AVR using K-nearest neighbor (KNN) for classification and PCA as feature extractor in [21]. Their target subset contained 35 instructions which they reached to near 100% accuracy. However, target instructions were
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Fig. 1 Mapping space

quite simple to distinguish, hence recognizing similar instructions with this method is not possible. Strobel et al. designed an attack based on the KNN algorithm for classification and polychotomous LDA [22] for dimensionality reduction [23]. The reported success rate was 96.24%. Park et al. employed continues wavelet transform (CWT) to map the traces to the time-frequency domain. Then, they used Kullback–Leibler (KL) divergence for feature extraction, and LDA for dimensionality reduction on the traces [24]. Finally, they reached a 99.03% success rate using quadratic discriminant analysis (QDA). Their target device was AVR, and they have used 112 instructions for the profiling and attacking phase. However, this method could not reach a good accuracy on our dataset because of the high sampling resolution of their dateset. It should be noted that 315 samples exist in each instruction on their dataset while in the proposed dataset it is 125 samples.

Note that some essential assumptions are required for the performance of ML techniques for SCA, such as having high resolution of sampling on side-channel traces and low noise setup for trace recording. In this article, these constraints are released, and the model is proposed to perform well under desired circumstances thatnks to generalization of CNN model. The rest of this paper is organized as follows. Section 3 includes the dataset gathering procedure, customizing simavr, and designing AVR random instruction generator and simulator for side-channel attacks (ARCSim). In section 4, the proposed CNN architectures based on two different models are explained. Then, LSTM model and the training mechanism to estimate the probabilities are expressed. Section 5 contains experimental results for both proposed models, and finally, achieved results and methodologies are discussed in section 7.

3 Dataset

Since dataset has a critical role in data driven and supervised models in the profiling phase, we explain the proposed approach to gather a labeled dataset.

3.1 Random Instruction Generation

For a typical SCA, the leakage estimation of the target device is the most significant phase which forms the baseline of the attack phase. Hence, it is crucial to stimulate all possible states of the target device in the profiling phase to obtain a rich dataset. Sample programs that are using is the profiling phase should be diverse, and runtime conditions have to be considered. Some of the main challenges are as below:

- Jump or branch to undefined memory addresses
- Covering all possible instructions in AVR instruction set
- Implementing subroutines with unknown number of instructions and subroutines inside subroutines

To satisfy these conditions, a random instruction generator (RIG) for AVR microcontrollers is proposed which is inspired by the program counter (PC) and the stack concept in AVR architecture. The proposed instruction generator can produce entirely random assembly instructions which are implementable on AVR. Besides, all register values that may be read or written in run time are filled with random numbers. The procedure to design this tool is shown in Algorithm 1.

With respect to the mentioned conditions, RIG has been developed in Python including all instructions from AVR instruction set. This tool could support all AVR cores, but in our study we have implemented five cores:
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Algorithm 1 Random Instruction Generation

Require: $n$ ▷ Number of instructions
Require: stack.put(0) ▷ Put the first line address on stack
Require: $pc ← 0$ ▷ program counter

1: while $pc < n$ do ▷ program counter
2: $inst ← \text{new instruction}$
3: $pc ← pc + 1$
4: if argument required then ▷ registers, register values, branch address
5: if argument uses $X$, $Y$, or $Z$ pointer then
6: $X$, $Y$, or $Z$ pointer $←$ random value
7: end if
8: argument $←$ random value
9: end if
10: if $(inst = \text{jump}) \text{ or } (inst = \text{branch})$ then
11: limit arguments inside memory
12: end if
13: if $inst = \text{subroutine}$ then
14: stack.put(current address) ▷ Put a value on stack
15: end if
16: if $inst = \text{return}$ then
17: $pc ← stack[-1]$ ▷ Last value of stack
18: stack.pop() ▷ Delete the last value of stack
19: end if
20: end while

- ATmega8
- ATmega16
- ATmega32
- ATmega128
- ATmega328

RIG is designed modular, thus extending it to support other AVR cores is straightforward. To extend a RIG to a new core, the instruction set of desired core and the supported memory addresses are required. Then, by importing and selecting the new instruction set for the related core in the Python source code, it will use this instruction set as the reference set. As all instructions from AVR instruction set are implemented, this tool will use those implementations to generate the new assembly code with respect to selected core memory addresses.

3.2 Compiling and Programming

After generating an assembly code including random instructions, AVR-GCC is used to compile the generated assembly file and produce a programmable hex file. One important issue about AVR-GCC is the mapping between the instructions that are existed in the assembly file and those that are translated to the hex file. The mapping between these two spaces translated by the compiler is not one-to-one, which means instructions in the assembly file do not necessarily exist in the hex file. Some of these mappings are shown in figure 1.

Thus, the label space is limited to those existed in the hex file so that some instructions will not exist in the run-time hex file. After compiling, AVRDUDE is employed to program the target IC and write fuse-bits. AVRDUDE is an AVR downloader and uploader which is exploited on Linux operating system to program target core.

3.3 Extracting run-time labels

As mentioned before, due to using supervised learning algorithms, labels are required to train the proposed model. However, extracting run-time labels for instructions is an undetermined procedure because some instructions are multi-cycle and some of them are one cycle regarding run-time conditions. As a case in point, "brne" could be a one-cycle instruction if a branch is not occurred or a two-cycle instruction if it is branched. Consequently, a simulation of generated hex code is required to obtain run-time labels and simavr is employed to simulate randomly generated programs. However, simavr does not export a label file for the simulated program. Therefore, the source code of simavr has been customized to export desired labels in a text file. It is worth mentioning that multi-cycle instructions in the customized version are labeled with indices to separate different cycles of an instruction (e.x. $mul_1$ and $mul_2$ for two cycles of mul instruction). Thus, all randomly generated programs could be simulated and labeled by a customized version of simavr to estimate the leakage model in the profiling phase.

3.4 ARCSim

Combining RIG with the customized version of simavr gives ARCSim in one software. ARCSim
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3.5 Recording data

After designing and implementing ARCSim, this tool is used to record side-channel traces on a target device. The framed data structure proposed in [24] is employed to record side-channel traces. Two different datasets have been gathered to train a model and evaluate the proposed methodology. Instructions that manipulate stack value or interact with I/O ports are discarded in the generation phase because these instructions may cause some run-time pauses, leading to simulation failure. Power side-channel traces of the target device are recorded by employing an OWON VDS 3102 USB oscilloscope. The sample rate is 1GS/s which is reduced to 500 MS/s when one channel is used as the trace recorder and the other one is applied as the trigger port. Target ATmega runs with an 8 MHz clock frequency, which leads to 125 samples per instruction. The descriptions for the gathered datasets are as below:

- **Dataset #1**: This dataset includes only one-cycle instructions that ATmega8 can support. It contains 54 instructions from the AVR instruction set, leading to 45 classes due to the mapping problem. Each cropped sample in this dataset consists of 400 sample points with pre-target and post-target instructions.

- **Dataset #2**: This dataset is more general and covers 109 instructions from the AVR instruction set, leading to 96 classes due to mapping problems. Each cropped sample in this dataset consists of 200 sample points with pre-target and post-target instructions.

3.6 Preprocessing

After gathering traces, some signal processing techniques are required to enhance signal representations before training the proposed model. They include cropping, alignment, normalization, and short-time Fourier transform (STFT) for better signal representation (Figure 2). The traces are cropped regarding the cycles of each instruction as shown in Figure 3. A trigger signal is employed to detect the starting of each frame and consequently aligns the signals. Then, a normalization phase is performed on traces to scale the values in the interval [0, 1]. Finally, the STFT is applied to all traces for extracting time-frequency coefficients.

4 Proposed Model

In this section, two models based on CNN are proposed to estimate the leakage of the target device and learn the distributions of instructions. The first model which has less layers than the second one is proposed to evaluate the capability of CNN in SCA. The second model is proposed to assess the impact of high level features in a typical SCA. Then, LSTM model is applied to estimate the probability distributions of instructions by knowing previous instructions.

4.1 Trace classification

CNN has been proved to be efficient in signal processing. It can outperform classic methods in
signal processing such as image and speech. Two different CNN architectures are proposed: The first model is inspired by the VGG network [25], and the second model is based on ResNet18 architecture [26] which has a residual block in its structure. These models are originally designed for image processing. In this study, they are employed for time series or one-dimensional signal processing. Hence, some modifications are made to original architectures to fit desired conditions as below:

- **Multi-channel inputs:** The original networks are designed for image processing which usually require three input channels as RGB. Here, the input channels are increased to 50, where all channels in the input contain traces related to a specific instruction from different programs and run times. This means that the pre-target and post-target instructions with all register values are different between channels and the only common part among these channels for one input is the target instruction. This forces network to extract features that distinguish the target instruction and does not get biased on other parts.

- **1D convolutions:** Both architectures employ 2D convolutions to extract spatial features from images. However, 1D convolutions are used because our intention is to get more attention on some specific frequencies to distinguish different instructions. Furthermore, our tests show that using the spatial information among multiple frequencies misleads the network to learn undesired features, leading to low accuracy.

- **SELU as activation function:** We alter the activation functions from rectified linear unit (ReLU) to scaled exponential linear units (SELU) [27] since SELU does not completely discard the negative values. This results in
higher accuracy during instruction recognition in the reverse engineering on our dataset.

By performing these modifications to original architectures, the first proposed model is shown in Figure 4(a). The model is called M1 for the rest of this paper. M1 has a simple architecture, and it is not very deep. Based on ResNet18 architecture, another model called M2 (Figure 4(b)) is proposed which is deeper than M1. This model includes the same architecture of the original ResNet18 with respect to the three mentioned modifications. These modifications make it suitable for our purpose, so that by using the residual blocks, the effect of a deep CNN is more observable on the dataset.

4.2 Probability distribution estimation

It is mentioned that our ARCSim generates entirely random instructions in recording the dataset. However, it should be noted that the instruction flow is not random in real programs at all, but it is based on some statistical distributions. Estimating or even learning these distributions entirely or partially could assist reverse engineering models where the target device is a black box. Hence, the proposed model in this section is employed to estimate these probability distributions and predict the next instruction. Here, the number of previous instructions is significant because the first $q$ instructions are not predictable due to absence of initialize instructions. LSTM networks are known for their ability to learn temporal features, which means they have memory. Suppose the attacker knows about the type of code running on the target device. In that case, he/she can use this information to estimate the probability distributions and eliminate the instructions with zero probability from training set for CNN models. The proposed instruction probability predictor based on LSTM is inspired by the hidden Markov model (HMM) presented in [19], which aims to model the microprocessor as a state machine. This analysis could determine the following instruction regarding the current instruction, specially could help CNN when the noise level is high enough, and the confidence of its prediction is low. A LSTM model is developed in this section, where the structure is shown in Table 1.

| Layer | LSTM architecture |
|-------|-------------------|
| Input | previous instruction labels |
| Layer 1 | 128 neurons |
| Layer 2 | 128 neurons |
| FC | (-1, class numbers) |

5 Experimental results

This section includes the implementation procedure and the results for both proposed models. We have trained and evaluated all proposed models on Nvidia GTX 1080 Ti.

5.1 CNN for reverse engineering

Two different models are explained in section 4.1 in order to trace classification. In the training procedure, Adam optimizer and Cross-Entropy loss function are used. The learning rate is set to 0.0001, and after 40 epochs the learning rate is reduced to 0.00001. The training is stopped at epoch 60 to avoid model overfitting. Two attack scenarios are designed for reverse engineering using these two models as below:

- **Sole scenario:** This method employs one model to classify all traces.
- **Hierarchical scenario:** A hierarchical attack contains two phases. First, instructions classified regarding their functionalities. Then, another model assigns a label for instructions of each group. This type of attack is inspired by [24], however, some modifications are done here.

Both M1 and M2 are employed to deploy such attacks in both scenarios on datasets and the results are reported in Table 2. The first dataset has 45 classes from one-cycle instructions while the second dataset has 96 classes. Thus, accuracy is higher in the first dataset compared to the second dataset. Besides, using a hierarchical scenario helps the network to divide the classification problem into two phases which results in higher accuracy. However, reported accuracy values in Table 2 are not comparable for both scenarios due to the existence of two phases in hierarchical scenario which have different probability weights.
Accordingly, an instruction-based table is available in the appendix A to determine the exact recognition accuracy using both scenarios for both datasets.

Among proposed methods, M2 outperforms M1 because of the residual blocks in the structure of M2. After applying the proposed methods on datasets, two of the most known attacks proposed in [5] and [24] are applied on datasets to compare with our proposed methods. Other existing methods usually include a small part of the instruction set which are not appropriate for comparison. PCA and LDA are combined with TA to evaluate their efficiencies in the reverse engineering using side channel information. The important implementation detail about TA is that our traces have 200 sample points; but this causes computational problems in calculating the determinant of the sample matrix. Thus, one, 10, and 20 features are selected in three different experiments to solve this problem. These features are chosen at the points where traces between two classes have the maximum mean difference. The results are reported in Table 3.

5.2 Instruction frequency analysis using LSTM

LSTM model is proposed for instruction frequency analysis and the probability estimation of instruction sequences. The dataset should not contain random instructions for this purpose. Since these models aim to extract the instruction flow of a real program, cryptographic algorithms are chosen as the target program to reverse. The provided training set includes eight cryptographic functions from AVR-crypto-lib which is a standard implementation. The customized version of simavr is employed to simulate the selected functions and export the label files. Then, some instructions are defined as the initial instructions for the network, which is the penalty for LSTM model. In our experiments, initial instructions are set two, five, and 10 respectively to test the capability of model. Results are shown in Table 4. As expected, the network obtains more information from previous instructions by increasing the number of initial instructions. In fact, more instructions in the queue, higher prediction accuracy is achieved. However, the purpose of this network is to assist M1 or M2 model in a real attack scenario to increase the final accuracy. In this way, most of initial instructions will be determined by M1 or M2 and LSTM model will be used in the cases in which M1 or M2 could not reach a high confidence classification for a trace.

6 Discussion

Using CNN for side-channel trace processing helps the attacker to use unaligned data. As our four different types of instructions indicate, the target instructions are not aligned in different types. But, the proposed architecture can distinguish them in the attack phase. So, our proposed model shows that CNN is resistant to misalignment of signals.

M1 and M2 models are employed to analyze the leakage of each instruction. Referring to our results (appendix B), the status register’s bit instructions and arithmetic instructions are the


Table 2  

| Model | Scenario     | Dataset #1 | Dataset #2 |
|-------|--------------|------------|------------|
|       | Sole         | 76.19%     | 49.37%     |
| M1    | Grouping     | 98.81%     | 95.13%     |
|       | Worst/Best   | 61.35%/92.52% | 44.64%/98.68% |
| M2    | Sole         | 78.27%     | 54.58%     |
|       | Grouping     | 99.02%     | 95.68%     |
|       | Worst/Best   | 42.10%/92.16% | 49.18%/94.08% |

Table 3  

| Method          | Feature Points | Mean Accuracy |
|-----------------|----------------|---------------|
| TA              | 1              | 23.21%        |
|                 | 10             | 21.08%        |
|                 | 20             | 20.57%        |
| PCA + TA        | 1              | 24.77%        |
|                 | 10             | 22.15%        |
|                 | 20             | 21.80%        |
| LDA + TA        | 1              | 26.32%        |
|                 | 10             | 25.54%        |
|                 | 20             | 23.76%        |
| KL Div. + QDA   | 200            | 29.17%        |
| Ours            | 200            | 54.58%        |

Table 4  

| Model | Number of Initial Instructions | LSTM |
|-------|--------------------------------|------|
|       | 2                              | 67.34% |
|       | 5                              | 89.03% |
|       | 10                             | 94.39% |

two groups with fewer side-channel leakages. So, it is crucial to have more data to reduce the noise as much as possible. However, we suggest using the LSTM model alongside the M1 or M2 model to increase the output’s confidence. The LSTM model can be used in two different phases. First, in the profiling attacks, the attacker does have extra information about the target processor. So, he can use this prior knowledge to limit the training dataset of the M1 and M2 models. For example, suppose the attacker knows that the target processor is executing a cryptographic algorithm. In that case, he can extract the probability of the instructions and then eliminate the instructions with zero probability from the training dataset. Consequently, the M1 or M2 model will be trained only on the possible instructions. Second, the LSTM model can be employed in instruction classification after M1 or M2. In this case, when the M1 or M2 model has more than one label assigned to a certain leakage, the LSTM model can be used to determine the correct label between the assigned labels by analyzing the previous instructions.

7 Conclusion

In this paper, we proposed a new mechanism for random dataset generation for disassembly attacks using side-channel information. The ARCSim was developed using python for instruction generation, simulation, and exporting labels file for profiling attacks. Later, our customized deep models are trained using the gathered dataset, and the results are compared to the three state-of-the-art side-channel attacks using machine learning. The practical results have shown the advantage of CNNs over other attacks in the feature extraction from low resolution data. Furthermore, a table including exact recognition accuracy per instruction in hierarchical scenario is reported in the appendix B, which could be referred to determine the leakage of each instruction. Referring to such
table could specify the prediction confidence for each instruction in real attacks. The dataset generated during the current study are available from the corresponding author on reasonable request.

By extending this work to more complex architectures, the amount of leakage could be determined, which could be helpful in designing new architectures to prevent these leakages and improve the security level. Another approach is to use attention-based neural networks to extract better features. Furthermore, employing information-theoretic feature extractors in preprocessing could help the network training and reduce the computational cost.

### Appendix A

Our modifications to group instructions in hierarchical scenario are applied on the original instruction groups. They are shown at the table below:

**Table A1** Grouping of instructions

| Groups | Instructions               | #  |
|--------|---------------------------|----|
| 1      | add,adc,sub,sbc,and,or,eor,cpse,cp,cpc, mov,movw | 12 |
| 2      | adiw,subi,sbci,sbiw,andi,ori,,cpi,ldi | 8  |
| 3      | com,neg,inc,dec,tst,clr,lsl,lsr,rol,ror,asr,swa | 12 |
| 4      | rjmp,breq,brne,brcs,brc,brmi,brpl,brhs, brhc,brts, brcf,brs,br,br,brid | 15 |
| 5      | ld_x,ld_x-,ld_x+,ld_y,ld_y-,ld_y+,ld_x,ld_x-, ld_x+,ld_x-,ld_x+,ld_y,ld_y+,ld_y-,ld_x,ld_x- | 20 |
| 6      | sec,clc,send,cln,sez,clz,ses,cls,sev,clv,set,slt, seh,clh | 14 |
| 7      | sbrc,sbrcs,brbc,bst,bld | 6  |
| 8      | lpm,lpm_x,lpm_x+ | 3  |
| 9      | muls,mulsu,fmul,fmulu,fmulsu | 6  |

### Appendix B

An instruction based accuracy is proposed including the exact leakage in a balanced dataset.

| Instruction | Leakage | Leakage |
|-------------|---------|---------|
|             | Sole    | Hierarchical |
| add         | 0.07    | 0.13    |
| adc         | 0.19    | 0.44    |
| sub         | 0.36    | 0.71    |
| sbc         | 0.23    | 0.62    |
| and         | 0.07    | 0.47    |
| or          | 0.07    | 0.29    |
| eor         | 0.07    | 0.18    |
| cpse        | 0.38    | 0.61    |
| cp          | 0.32    | 0.36    |
| cpc         | 0.14    | 0.42    |
| mov         | 0.20    | 0.34    |
| movw        | 0.88    | 0.79    |

**Table B2** Group1

| Instruction | Leakage | Leakage |
|-------------|---------|---------|
|             | Sole    | Hierarchical |
| adiw        | 0.97    | 1        |
| subi        | 0.36    | 0.71    |
| sbci        | 0.35    | 0.60    |
| sbiw        | 0.99    | 1        |
| andi        | 0.48    | 0.86    |
| ori         | 0.63    | 0.82    |
| cpi         | 0.55    | 0.97    |

**Table B3** Group2

| Instruction | Leakage | Leakage |
|-------------|---------|---------|
|             | Sole    | Hierarchical |
| com         | 0.50    | 0.76    |
| neg         | 0.34    | 0.59    |
| inc         | 0.14    | 0.41    |
| dec         | 0.48    | 0.77    |
| tst         | 0.30    | 0.58    |
| clr         | 0.30    | 0.55    |
| lsl         | 0.07    | 0.25    |
| lsr         | 0.13    | 0.21    |
| rol         | 0.07    | 0.56    |
| ror         | 0.19    | 0.35    |
| asr         | 0.20    | 0.44    |
| swa         | 0.19    | 0.28    |

**Table B4** Group3

For profiling Disassembly attacks using Side-Channel Leakages and Deep Neural Networks
A Novel Framework for Dataset Generation for profiling Disassembly attacks using Side-Channel Leakages and Deep Neural Networks

| Instruction | Leakage  |
|-------------|----------|
|             | Sole | Hierarchical |
| rjmp        | 0.73 | 0.95         |
| breq        | 0.51 | 0.77         |
| brne        | 0.53 | 0.74         |
| brcs        | 0.44 | 0.61         |
| brcc        | 0.51 | 0.58         |
| brmi        | 0.17 | 0.42         |
| brpl        | 0.23 | 0.39         |
| brhs        | 0.37 | 0.43         |
| brhc        | 0.26 | 0.45         |
| brts        | 0.22 | 0.41         |
| brtc        | 0.19 | 0.47         |
| brvs        | 0.55 | 0.77         |
| brvc        | 0.54 | 0.72         |
| brie        | 0.36 | 0.92         |
| brid        | 0.83 | 0.91         |

**Table B5** Group 4

| Instruction | Leakage  |
|-------------|----------|
|             | Sole | Hierarchical |
| ld_x        | 0.76 | 0.77         |
| ld_x-       | 0.67 | 0.97         |
| ld_x+       | 0.73 | 0.91         |
| ld_y        | 0.68 | 0.93         |
| ld_y-       | 0.99 | 1            |
| ld_y+       | 0.85 | 0.99         |
| ld_z        | 0.52 | 0.77         |
| ld_z-       | 0.76 | 0.94         |
| ld_z+       | 0.71 | 0.90         |
| lds         | 0.98 | 1            |
| st_x        | 0.54 | 0.80         |
| st_x-       | 0.61 | 0.82         |
| st_x+       | 0.91 | 0.98         |
| st_y        | 0.51 | 0.60         |
| st_y-       | 0.78 | 0.96         |
| st_y+       | 0.99 | 1            |
| st_z        | 0.56 | 0.80         |
| st_z-       | 0.53 | 0.91         |
| st_z+       | 0.94 | 1            |
| sts         | 0.88 | 1            |

**Table B6** Group 5

| Instruction | Leakage  |
|-------------|----------|
|             | Sole | Hierarchical |
| sec         | 0.45 | 0.58         |
| clc         | 0.07 | 0.18         |
| sen         | 0.14 | 0.23         |
| chn         | 0.06 | 0.34         |
| sez         | 0.08 | 0.12         |
| clz         | 0.09 | 0.15         |
| ses         | 0.13 | 0.27         |
| cls         | 0.10 | 0.13         |
| sev         | 0.12 | 0.31         |
| clv         | 0.19 | 0.29         |
| set         | 0.05 | 0.25         |
| clt         | 0.10 | 0.23         |
| seh         | 0.13 | 0.33         |
| clh         | 0.12 | 0.28         |

**Table B7** Group 6

| Instruction | Leakage  |
|-------------|----------|
|             | Sole | Hierarchical |
| shrc        | 0.73 | 0.82         |
| sbrc        | 0.43 | 0.58         |
| brbs        | 0.28 | 0.54         |
| brbc        | 0.43 | 0.81         |
| bst         | 0.44 | 0.22         |
| bld         | 0.35 | 0.56         |

**Table B8** Group 7

| Instruction | Leakage  |
|-------------|----------|
|             | Sole | Hierarchical |
| lpm         | 0.98 | 0.98         |
| lpm_z       | 0.94 | 0.95         |
| lpm_z+      | 0.96 | 0.98         |

**Table B9** Group 8

| Instruction | Leakage  |
|-------------|----------|
|             | Sole | Hierarchical |
| muls        | 0.69 | 0.57         |
| muls        | 0.40 | 0.41         |
| mulsu       | 0.47 | 0.85         |
| fmul        | 0.79 | 0.94         |
| fmul        | 0.65 | 0.78         |
| fmul        | 0.41 | 0.68         |

**Table B10** Group 9
References

[1] Wu, L., Weissbart, L., Krč, M., Li, H., Perin, G., Batina, L., Picek, S., et al.: On the attack evaluation and the generalization ability in profiling side-channel analysis. Cryptology ePrint Archive (2020)

[2] Quisquater, J.-J., Samyde, D.: Automatic code recognition for smartcards using a kohonen neural network. In: 5th Smart Card Research and Advanced Application Conference (CARDIS'02) (2002)

[3] Suykens, J.A., Vandewalle, J.: Least squares support vector machine classifiers. Neural processing letters 9(3), 293–300 (1999)

[4] Hospodar, G., Gierlichs, B., De Mulder, E., Verbauwhede, I., Vandewalle, J.: Machine learning in side-channel analysis: a first study. Journal of Cryptographic Engineering 1(4), 293 (2011)

[5] Chari, S., Rao, J.R., Rohatgi, P.: Template attacks. In: International Workshop on Cryptographic Hardware and Embedded Systems, pp. 13–28 (2002). Springer

[6] Krizhevsky, A., Sutskever, I., Hinton, G.E.: Imagenet classification with deep convolutional neural networks. Advances in neural information processing systems 25, 1097–1105 (2012)

[7] Kocher, P., Jaffe, J., Jun, B.: Differential power analysis. In: Annual International Cryptology Conference, pp. 388–397 (1999). Springer

[8] Brier, E., Clavier, C., Olivier, F.: Correlation power analysis with a leakage model. In: International Workshop on Cryptographic Hardware and Embedded Systems, pp. 16–29 (2004). Springer

[9] Schindler, W., Lemke, K., Paar, C.: A stochastic model for differential side channel cryptanalysis. In: International Workshop on Cryptographic Hardware and Embedded Systems, pp. 30–46 (2005). Springer

[10] Lerman, L., Bontempi, G., Markowitch, O.: Power analysis attack: an approach based on machine learning. International Journal of Applied Cryptography 3(2), 97–115 (2014)

[11] Lerman, L., Poussier, R., Bontempi, G., Markowitch, O., Standaert, F.-X.: Template attacks vs. machine learning revisited (and the curse of dimensionality in side-channel analysis). In: International Workshop on Constructive Side-Channel Analysis and Secure Design, pp. 20–33 (2015). Springer

[12] Picek, S., Heuser, A., Jovic, A., Ludwig, S.A., Guilley, S., Jakobovic, D., Mentens, N.: Side-channel analysis and machine learning: A practical perspective. In: 2017 International Joint Conference on Neural Networks (IJCNN), pp. 4095–4102 (2017). IEEE

[13] Cristiani, V., Lecomte, M., Maurine, P.: Leakage assessment through neural estimation of the mutual information. In: International Conference on Applied Cryptography and Network Security, pp. 144–162 (2020). Springer

[14] McCann, D., Oswald, E., Whitnall, C.: Towards practical tools for side channel aware software engineering:‘grey box’modelling for instruction leakages. In: 26th USENIX Security Symposium (USENIX Security 17), pp. 199–216 (2017)

[15] McCann, D., Whitnall, C., Oswald, E.: Elmo: Emulating leaks for the arm cortex-m0 without access to a side channel lab. IACR Cryptol. ePrint Arch. 2016, 517 (2016)

[16] Gao, S., Marshall, B., Page, D., Oswald, E.: Share-slicing: Friend or foe? IACR Transactions on Cryptographic Hardware and Embedded Systems, 152–174 (2020)

[17] Heuser, A., Kasper, M., Schindler, W., Stöttinger, M.: A new difference method for side-channel analysis with high-dimensional leakage models. In: Cryptographers’ Track at the RSA Conference, pp. 365–382 (2012). Springer

[18] Cristiani, V., Lecomte, M., Hiscock, T.: A
A Novel Framework for Dataset Generation for profiling Disassembly attacks using Side-Channel Leakages and Deep Neural Networks

bit-level approach to side channel based disassembling. In: CARDIS 2019 (2019)

[19] Eisenbarth, T., Paar, C., Weghenkel, B.: Building a side channel based disassembler. In: Transactions on Computational Science X, pp. 78–99. Springer, ??? (2010)

[20] Jolliffe, I.: Principal component analysis. Encyclopedia of statistics in behavioral science (2005)

[21] Msgna, M., Markantonakis, K., Mayes, K.: Precise instruction-level side channel profiling of embedded processors. In: International Conference on Information Security Practice and Experience, pp. 129–143 (2014). Springer

[22] Friedman, J.H.: Another approach to polytomous classification. Technical Report, Statistics Department, Stanford University (1996)

[23] Strobel, D., Bache, F., Oswald, D., Schellenberg, F., Paar, C.: Scandalee: a side-channel-based disassembler using local electromagnetic emanations. In: 2015 Design, Automation & Test in Europe Conference & Exhibition (DATE), pp. 139–144 (2015). IEEE

[24] Park, J., Xu, X., Jin, Y., Forte, D., Tehranipoor, M.: Power-based side-channel instruction-level disassembler. In: 2018 55th ACM/ESDA/IEEE Design Automation Conference (DAC), pp. 1–6 (2018). IEEE

[25] Simonyan, K., Zisserman, A.: Very deep convolutional networks for large-scale image recognition. arXiv preprint arXiv:1409.1556 (2014)

[26] He, K., Zhang, X., Ren, S., Sun, J.: Deep residual learning for image recognition. In: Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition, pp. 770–778 (2016)

[27] Klambauer, G., Unterthiner, T., Mayr, A., Hochreiter, S.: Self-normalizing neural networks. In: Proceedings of the 31st International Conference on Neural Information Processing Systems, pp. 972–981 (2017)