Qubit Mapping Based on Subgraph Isomorphism and Filtered Depth-Limited Search

Sanjiang Li, Xiangzhen Zhou, Yuan Feng

Abstract—Mapping logical quantum circuits to Noisy Intermediate-Scale Quantum (NISQ) devices is a challenging problem which has attracted rapidly increasing interests from both quantum and classical computing communities. This paper proposes an efficient method by (i) selecting an initial mapping that takes into consideration the similarity between the architecture graph of the given NISQ device and a graph induced by the input logical circuit; and (ii) searching, in a filtered and depth-limited way, a most useful SWAP combination that makes executable as many as possible two-qubit gates in the logical circuit. The proposed circuit transformation algorithm can significantly decrease the number of auxiliary two-qubit gates required to be added to the logical circuit, especially when it has a large number of two-qubit gates. For an extensive benchmark set of 131 circuits and IBM’s current premium Q system, viz., IBM Q Tokyo, our algorithm needs, in average, 0.3801 extra two-qubit gates per input two-qubit gate, while the corresponding figures for three state-of-the-art algorithms are 0.4705, 0.8154, and 1.0066 respectively.

Index Terms—NISQ, quantum circuit transformation, qubit mapping, subgraph isomorphism, heuristic search.

1 INTRODUCTION

SINCE Shor’s exciting quantum algorithms for solving integer factorisation and discrete logarithm [1], many quantum algorithms have been proposed that could offer an exponential speed-up when compared with best classical algorithms. These include in particular the HHL algorithm for solving systems of linear equations [2] and other machine learning algorithms derived from HHL (cf. [3] for a summary). Typically, the implementation of these algorithms requires quantum computers with millions of qubits which are perhaps still not available in the next two decades. On the other hand, IBM, Intel and Google have all announced their quantum devices with around 50-70 qubits recently. The Noisy Intermediate-Scale Quantum (NISQ) era seems coming in reality. Despite that quantum error correction is not yet available in the near future, quantum supremacy has recently been demonstrated in Google’s 53-qubit quantum processor Sycamore [4].

There is yet another gap between theoretical research on quantum algorithms and their implementation on realistic quantum devices. When designing quantum algorithms, typically, the quantum circuit model allows multi-qubit gates to act on any set of qubits without restriction. This is, however, not the case in realistic NISQ devices, which have “limited number of qubits, limited connectivity between qubits, restricted (hardware-specific) gate alphabets, and limited circuit depth due to noise” [5]. In the superconducting devices of IBM, Google, and Rigetti, only single and special two-qubit gates (like CNOT or CZ) are supported. Even worse, these two-qubit gates can only be implemented between neighbouring qubits. For example, Fig. 1 shows the architecture graph of IBM’s current premium quantum system IBM Q Tokyo (also known as IBM Q20), which supports elementary single-qubit gates and two-qubit CNOT gates and a CNOT gate can be implemented only between qubits which are connected by an (undirected) edge. In order to use these NISQ devices, the desired quantum functionality in an ideal quantum circuit should be transformed or mapped so that the underlying coupling constraints imposed by these quantum devices are satisfied.

More precisely, in order to implement an ideal quantum circuit on an NISQ device like IBM Q Tokyo, we need to address two issues. The first is to decompose the desired functionality (arbitrary quantum gates) into elementary operations that can be directly applied on the NISQ device. This issue has already been properly addressed in several works [6], [7], [8]. The second issue, known as qubit mapping or circuit transformation, is to map or route the qubits in the ideal quantum circuit to qubits of the quantum device so that the coupling constraints imposed by the quantum device are satisfied and thus the two-qubit gates in the ideal quantum circuit are executable.

In the past several years, the qubit mapping problem has attracted rapidly increasing interests from both classical and quantum computing communities, see, e.g., [9], [10], [11].

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Given an arbitrary quantum circuit and an NISQ device, the task of qubit mapping is to construct automatically a quantum circuit with the same functionality which can be immediately implemented in the NISQ device. For ease of presentation, we call the quantum circuit to be transformed a logical circuit and call a circuit that is implementable in the NISQ device a physical circuit. Similarly, we call qubits in a logical (physical) circuit logical (physical) qubits. We assume that gates in the input logical circuit are already decomposed into elementary gates supported by the NISQ device. In particular, each gate in the logical circuit involves at most two qubits. Naturally, we also assume that the number of logical qubits is not larger than the number of physical qubits.

It is not difficult to find such a solution for an input logical circuit. Indeed, we can start with an arbitrary initial mapping and then execute one two-qubit gate per round (note single-qubit gates can be executed directly) by inserting several SWAP operations to transform the current mapping to a mapping that can execute the current two-qubit gate. The challenge is if we can find a solution with minimal overhead in terms of the number of SWAP gates inserted. This is crucial for the success of quantum computing as a large number of extra two-qubit gates will significantly accumulate the error of the output physical circuit.

Finding an optimal solution for the qubit mapping problem is often very difficult. Indeed, it is NP-complete [11] to decide if an input logical circuit can be transformed into an equivalent physical circuit using up to $k$ SWAP gates for a fixed integer $k > 0$. Several previous works use off-the-shelf tools like dynamic programming [11], SAT solvers [10], temporal planners [12], Integer Linear Programming (ILP) [19], satisfiability modulo theory (SMT) solvers [13]. In worst cases, all these approaches take time exponential in the number of qubits.

Many other works devise specialised heuristic search algorithms for solving the qubit mapping problem. For example, Zulehner, Paler and Wille [14] partitioned the input logical circuit into layers and introduced an $A^*$ search algorithm. When combined with a lookahead scheme and a dedicated method for selecting the initial mapping, their algorithm performs much better than IBM’s own solution. However, this $A^*$-approach takes time exponential in the number of qubits. Li, Ding and Xie [15] proposed a search algorithm based on reverse traversal, which is polynomial in the number of qubits and works very well for small circuits with less than a hundred two-qubit gates. Their algorithm, called SABRE, outperforms the $A^*$-approach [14] with exponential speedup and comparable or better results on various benchmarks. Childs, Schoute and Unsal [16] also proposed efficient methods that attempt to minimise the circuit depth or size overhead and have worst-case time complexity polynomial in the sizes of the input circuit and the architecture graph. To this end, they decomposed the problem into two subproblems: qubit movement and qubit placement. The first subproblem considers how to transform the current mapping to a selected next mapping by imposing SWAP gates on edges in the architecture graph, while the second subproblem gives method to compute the next mapping. In another work, Cowtan et al. [17] described a solution implemented in the platform-independent compiler $t(ket)$. They also partitioned the input circuit into layers and selected the SWAP which can maximally reduce the diameter of the subgraph composed of all pairs of qubits in the current layer. We address their algorithm as the Cambridge algorithm henceforth. In [18], we designed a new qubit mapping algorithm, called SAHS in this paper, which uses simulated annealing for constructing an initial mapping and searches the next mapping by using a heuristic function that reflects the variable influence of gates in different layers. Empirical results show that SAHS outperforms both SABRE and the Cambridge algorithm by a large margin. Initial mappings of SAHS are, however, computed non-deterministically by simulated annealing, which is sometimes unstable and runs slowly when the circuit size is large [18].

In this paper, we propose a new search algorithm based on subgraph isomorphism and filtered depth-limited search. The idea is to construct a graph $G$ from the input circuit which is isomorphic to a subgraph of $AG$, the architecture graph of the given NISQ device, and select any embedding from $G$ to $AG$ as the initial mapping. Starting from this initial mapping, we then, step by step, construct the physical circuit while removing executable gates from the logical circuit. If the current mapping can execute some gates in the front layer of the logical circuit, we remove them from the logical circuit and properly append them to the current physical circuit; if there are no executable gates in the front layer, then we need to insert SWAP gates and obtain a new mapping so that some two-qubit gates in the front layer can be executed. To select a good next mapping, we tend to exhaustively search all possible combinations of SWAP operations such that the number of executable two-qubit gates per SWAP is maximised. As selecting the best SWAP combination is expensive, we fix $k > 0$ and only consider combinations of at most $k$ SWAPs. The search process could be further sped up if we ‘filter’ those SWAPs which do not interact with gates in the first several layers of the circuit. Such filters are designed and used in our algorithm.

While less efficient when compared with the Cambridge algorithm, the search process of our algorithm is polynomial in all relevant parameters and can significantly reduce the number of SWAPs required to transform the input logical circuit. Indeed, empirical evaluation shows that our algorithm can often reduce by half the number of SWAPs required when compared with SABRE, if the input logical circuit has hundreds or more two-qubit gates. Similar empirical evaluations also show that our algorithm is significantly better than the Cambridge algorithm [17] and our SAHS algorithm [18] in terms of the size of the output circuits.

The remainder of this paper is organised as follows. In Sec. 3 we recall some background of quantum computation and quantum circuits, and describe and analyse our algorithm in Sec. 3. Detailed empirical evaluation on IBM Q Tokyo is reported in Sec. 4. We further discuss in Sec. 5 possible extensions, scalability, efficiency and effectiveness of our approach and report more evaluation results on three large architectures. The last section concludes the paper with discussions on directions for future research.
2 Backgrounds

In this section, after a brief introduction of quantum gates and quantum circuits, we describe the dependency graph associated to a logical circuit and show how to partition the logical circuit into layers by using the dependency graph.

2.1 Quantum Gates and Quantum Circuits

Qubit is the counterpart of bit in quantum computation. While a ‘classical’ bit can only be in one of two states, viz., 0 and 1, a qubit can be in the superposition state \(|\psi\rangle = \alpha |0\rangle + \beta |1\rangle\) of the two basis states, \(|0\rangle\) and \(|1\rangle\), where \(\alpha, \beta \in \mathbb{C}\) are probability amplitudes satisfying \(|\alpha|^2 + |\beta|^2 = 1\). For example, \(|+\rangle = \frac{1}{\sqrt{2}} (|0\rangle + |1\rangle)\) and \(|-\rangle = \frac{1}{\sqrt{2}} (|0\rangle - |1\rangle)\) are two superposition states. The success of quantum computation partially lies in ingenious use of quantum superposition.

Quantum computation is realised by applying quantum gates on qubits. Complex, multi-qubit gates can be decomposed into elementary single or two-qubit gates. In fact, any quantum gate can be approximated to arbitrary accuracy using a fixed set of single-qubit gates and CNOT gates [20].

Fig. 2 illustrates three very useful gates: Hadamard gate \(H\), CNOT gate and SWAP gate. Hadamard gate is a single-qubit gate which can evenly mix the basis states to produce a superposed one. Precisely, \(H\) maps \(|0\rangle\) to \(|+\rangle\) and \(|1\rangle\) to \(|-\rangle\). CNOT and SWAP are both two-qubit gates, i.e., they operate on two qubits. A CNOT gate flips the target qubit (indicated graphically with \(\oplus\)) if and only if the control qubit (indicated graphically with a black dot \(\bullet\)) is in state \(|1\rangle\), while a SWAP gate exchanges the states of the two qubits operated. Precisely, CNOT maps \(|a\rangle|b\rangle\) to \(|a\rangle|a \oplus b\rangle\) and SWAP maps \(|a\rangle|b\rangle\) to \(|b\rangle|a\rangle\) for \(a, b \in \{0, 1\}\). Most NISQ devices do not support SWAP gates directly and, if this is the case, we may implement a SWAP gate by three CNOT gates (see Fig. 2 (right)).

Quantum circuits are the most commonly used model to describe quantum algorithms, which consist of input qubits, quantum gates, measurements and classical registers [21]. As only input qubits and quantum gates are relevant in the qubit mapping problem, in this paper, we represent a quantum circuit simply as a pair \((Q, C)\), where \(Q\) is the set of involved qubits and \(C\) a sequence of quantum gates.

2.2 Dependency Graph and Front Layer

Two-qubit gates in a logical circuit \(LC = (Q, C)\) are not independent in general. We say a two-qubit gate \(g_1\) depends on another two-qubit gate \(g_2\) if the latter must be executed before the former. This happens when \(g_2\) is in front of \(g_1\) in \(C\) and they share a common qubit, or when \(g_1\) depends on a two-qubit gate \(g_3\) which depends on \(g_2\). For clarity, we say \(g_1\) directly depends on \(g_2\) if \(g_2\) is in front of \(g_1\) in \(C\) and they share a common qubit and there are no other gates between them which share the same common qubit.

For a logical circuit \(LC = (Q, C)\), we construct a directed acyclic graph (DAG), called the dependency graph, to characterise the direct dependency between two-qubit gates in \(LC\) [15, 16]. Each node of the dependency graph represents a two-qubit gate and each directed edge the direct dependency relationship from one two-qubit gate to another. The front layer of \(LC\), denoted \(F(LC)\) or \(L_0(LC)\), consists of all two-qubit gates in \(LC\) which have no parents in the dependency graph. The second layer \(L_1(LC)\) is then the front layer of the circuit obtained from \(LC\) by deleting all gates in \(F(LC)\). Analogously, we can define the \(k\)-th layer \(L_k(LC)\) of \(LC\) for all \(k \geq 0\).

Example 1. Consider the logical circuit \(LC = (Q, C)\) shown in Fig. 3 (left), where

\[ Q = \{q_0, q_1, q_2, q_3\}, \]
\[ C = \{q_0 \equiv \{g_2, q_0\}, q_1 \equiv \{q_3, q_2\}, q_2 \equiv \{q_0, q_3\}, q_3 \equiv \{q_0, q_2\}, 
q_4 \equiv \{q_3, q_2\}, q_5 \equiv \{q_0, q_3\}, q_6 \equiv \{q_3, q_1\}\]where \(\{q_2, q_0\}\), for example, denotes the CNOT gate in the logical circuit with \(q_2\) being the control qubit and \(q_0\) the target.

For this circuit, we have \(F(LC) = \{q_0\}, L_1(LC) = \{q_1\}, L_2(LC) = \{q_2\}\), and \(L_3(LC) = \{q_3\}\), and so on. From the dependency graph (showing in Fig. 3 (right)), we can see that, for example, gate \(g_2\) can be executed only after \(g_0\) and \(g_1\).

3 The Proposed Approach

The main objective of qubit mapping is to transform an input logical circuit to a physical one with minimal size or depth so that the constraints imposed by the NISQ device are satisfied. To simplify the discussion, we only consider the connectivity constraints for two-qubit gates as specified by the architecture graph. This means that single-qubit gates have no effect in the circuit transformation process. Furthermore, we make the following assumptions [17]:

1. The NISQ device supports all single-qubit gates and CNOT gates;
2. The architecture graph of the NISQ device, \(AG\), is an undirected graph;
3. CNOT gates are the only two-qubit gates in the input logical circuit.

From now on and as in Example 1, we write a CNOT gate simply as a pair \(\langle q, q'\rangle\), where \(q\) and \(q'\) are the control and target qubits, respectively. We call the CNOT gate \(\langle q, q'\rangle\) the inverse of \(\langle q', q\rangle\).

Let \(AG = (V, E)\) be the undirected architecture graph of the NISQ device we are given, where \(V\) is the set of physical qubits and \(E\) the set of edges along which CNOT gates can be performed. Recall that an edge \(e\) in an undirected graph is an unordered pair of endpoints \(p, q\) of \(e\). In the following, we write \(e\) simply by \(\langle p, q\rangle\), i.e., the set of its two endpoints.

Let \(LC = (Q, C)\) be a logical circuit with \(|Q| \leq |V|\). Suppose \(C\) consists of only CNOT gates after removing all single-qubit gates. We need to construct a physical circuit \(PC = (V, C^p)\) which contains only CNOT gates and satisfies:

1. it is functionally equivalent to \(LC\) after adding back all single-qubit gates accordingly, and
2. it respects the connectivity constraints imposed by \(AG\), i.e., \(\{q, q'\} \in E\) for any CNOT gate \(\langle q, q'\rangle\) in \(C^p\).

It is easy to find a physical circuit that satisfies the above conditions, but the real challenge is to find one with

1. The occurrences of CNOT gates may be replaced by CZ gates when, e.g., a Rigetti device or Google’s Sycamore is used.
minimal size or depth, which is NP-complete in general [11].

In this paper, we modify the input logical circuit stepwise by inserting auxiliary SWAP operations (each implemented with three CNOT gates as in Fig. 2 (right)) until the logical circuit is transformed into a physical circuit that can be executed on the NISQ device. To evaluate the effectiveness of qubit mapping algorithms, we use the sizes of the output circuits, i.e., the total number of its two-qubit gates.

### 3.1 Qubit Mapping

In each step, qubits in the logical circuit are mapped or allocated to physical qubits in the NISQ device. Mathematically, a (partial) qubit mapping is a (partial) function τ from Q to V such that τ(q) = τ(q′) if and only if q = q′ for any q, q′ ∈ Q. We say a partial qubit mapping is complete if it is defined for every q in Q. A physical qubit v is occupied or allocated if τ maps some logical qubit q to v. Otherwise, we say v is unoccupied. The mapping may change in consecutive steps of the transformation which is determined by the inserted auxiliary SWAP operations.

Given a logical circuit LC and a mapping τ, a CNOT gate g = ⟨q, q′⟩ in LC is said to be satisfied by τ, or τ satisfies g, if \{τ(q), τ(q′)\} is an edge in AG. Furthermore, g is executable by τ if it appears in the front layer of LC and τ satisfies g. If this is the case, we remove g from LC and append a CNOT gate τ(g) := ⟨τ(q), τ(q′)⟩ to the end of the physical circuit. This process is called the execution of g.

For two physical qubits v, v′ in AG, we write distAG(v, v′) for the distance (i.e., the length of a shortest path) from v to v′ in AG.

For any mapping τ and any two-qubit gate g = ⟨q, q′⟩, the physical distance between the two qubits q, q′ in g under mapping τ, written distph(q, q′, τ), is defined as

- the distance between τ(q) and τ(q′) in AG, i.e., distAG(τ(q), τ(q′)); if both τ(q) and τ(q′) are defined,
- the shortest distance between τ(q) or τ(q′) to all unoccupied physical qubits if only one of τ(q) and τ(q′) is defined, and

- the shortest distance between two unoccupied qubits if neither τ(q) nor τ(q′) is defined.

Apparently, a gate g = ⟨q, q′⟩ in the front layer is executable by τ if both τ(q) and τ(q′) are defined and the physical distance between q and q′ under τ is 1.

**Example 2** (Example 1 cont’d). Consider the logical circuit LC shown in Fig. 3. Let τ1 : Q → V be the mapping specified by \(τ_1(q_0) = v_2, \, τ_1(q_1) = v_0, \, τ_1(q_2) = v_{10}, \, τ_1(q_3) = v_6\), see Figure 4 (left). Then, because \(τ_1(q_2) = v_{10}\) and \(τ_1(q_6) = v_2\) and distAG(v_2, v_{10}) = 2, we can see that \(q_0 \not\equiv ⟨q_2, q_6⟩\) is not executable by \(τ_1\) in IBM Q Tokyo. However, \(q_0\) is executable by the mapping \(τ_3\) shown in Figure 4 (right) and, indeed, every gate in LC is satisfied by \(τ_3\).

### 3.2 Initial Mapping

An initial mapping can be constructed step by step or selected arbitrarily or computed from a dedicated subroutine. Zulehner et al. [14] tested both arbitrary initial mappings and initial mappings evolved from an empty mapping. Their experimental evaluation showed that, in general, the latter approach has better performance. In [15], Li et al. proposed to use an initial mapping that takes the whole input circuit into consideration. Starting from a randomly generated mapping \(τ_0\), they first take this mapping as the initial mapping and apply it on the input circuit \((Q, C)\), the obtained final mapping \(τ_1\) is then used as the initial mapping and applied to the inverse circuit \((Q, C^{\text{inv}})\), and finally, the obtained final mapping \(τ_j\) is selected as the initial mapping for their main algorithm SABRE. Their approach was demonstrated as consistently better than the \(A^*\) search algorithm in [14]. In [18], we proposed SAHS, which uses simulated annealing to search for the best initial mapping that fits well with the input logical circuit and empirical evaluation there shows that, when compared with the naive mapping that sends \(q_i\) to \(v_i\), SAHS works significantly better with the initial mapping obtained by simulated annealing.

2. Note the “inverse” here has a different meaning as the “inverse” CNOT gate defined in page 5.
In this section we show how to obtain a good initial mapping by matching a particular graph induced by the input circuit with the architectural graph.

Suppose \( LC = (Q, C) \) is the input logical circuit. We first construct an undirected graph \( G_{\text{circ}}(C) = (Q, E_{\text{circ}}) \) on \( Q \), where \( \{q, q'\} \) is an edge in \( E_{\text{circ}} \) if either \( \{q, q'\} \) or its inverse \( \{q', q\} \) is in \( C \). If \( G_{\text{circ}}(C) \) happens to be isomorphic to a subgraph of the architecture graph \( A_G \), then the qubit mapping problem is solved by constructing an (arbitrary) isomorphic embedding \( \tau \) from \( G_{\text{circ}}(C) \) to \( A_G \). For NISQ devices, which have up to several hundreds qubits, this can be solved by, for example, the VF2 algorithm \[22\]. If \( G_{\text{circ}}(C) \) is not isomorphic to a subgraph of \( A_G \), then we may select a maximal sub-circuit \( C_{\text{top}} \) of \( C \) such that

(i) \( C_{\text{top}} \) is a front section of \( C = \{ q_i \in C \mid 1 \leq i \leq n \} \) w.r.t. the dependency graph of \( C \), i.e., a two-qubit gate \( q_i \) is in \( C_{\text{top}} \) only if all two-qubit gates \( q_j \) on which \( q_i \) depends are in \( C_{\text{top}} \);

(ii) the graph \( G_{\text{circ}}(C_{\text{top}}) \) is isomorphic to a subgraph of \( A_G \); and

(iii) the graph \( G_{\text{circ}}(C_{\text{top}} \cup \{ q_{i^*} \}) \) is not isomorphic to a subgraph of \( A_G \) for any \( q_{i^*} \) that is in the front layer of \( C \setminus C_{\text{top}} \).

We call \( G_{\text{circ}}(C_{\text{top}}) \) a top subgraph (topgraph for short) of \( G_{\text{circ}}(C) \). Let \( \tau_{\text{top}} \) be an isomorphic embedding from \( G_{\text{circ}}(C_{\text{top}}) \) to \( A_G \). We select \( \tau_{\text{top}} \) as the initial mapping, which satisfies all gates in \( C_{\text{top}} \). Note that \( \tau_{\text{top}} \) might not be a complete mapping from \( Q \) to \( V \).

**Example 3** (Example 1 cont’d). For the circuit \( LC \) in Example 2, we have \( Q = \{q_0, q_1, q_2, q_3\} \) and \( E_{\text{circ}} = \{\{q_0, q_2\}, \{q_0, q_3\}, \{q_2, q_3\}, \{q_1, q_3\}\} \). Clearly, \( G_{\text{circ}}(C) \) is isomorphic to a subgraph of \( A_G \), and such an isomorphism is specified by the qubit mapping \( \tau_3 \) in Fig. 4 (right).

Note that \( \tau_{\text{top}} \) often does not take the whole circuit into consideration. We propose another method for constructing the initial mapping that considers the whole circuit. For a logical circuit \( LC = (Q, C) \), we introduce a weight function \( \omega \) which assigns a weight on each edge of \( E_{\text{circ}} \) (the edge set of the undirected graph \( G_{\text{circ}}(C) \) defined above) such that \( \omega(\{q, q'\}) \) is the number of gates \( q_i \) in \( C \) with \( g_{\text{circ}} = \{q, q'\} \) or \( g_{\text{circ}} = \{q', q\} \). Let \( E_{\text{circ}}^w = \{e_1, e_2, ..., e_n\} \) where \( \omega(e_1) \geq \ldots \geq \omega(e_n) \). We then construct a subgraph \( G^* = (Q, E^*) \) of \( G_{\text{circ}}(C) \) which is isomorphic to a subgraph of \( A_G \) as follows. We start by letting \( E^* = \{e_1\} \) and then consider the next edge \( e_2 \). In general, suppose we have decided if \( e_i \) should be put into \( E^* \) or not for all \( i < k \) for some \( k \leq n \) and the current subgraph \( G^* \) is isomorphic to some subgraph of \( A_G \). We consider \( e_{i+1} \). If putting \( e_{i+1} \) into \( E^* \) will make \( G^* \) non-isomorphic to any subgraph of \( A_G \), we skip this edge; otherwise, we put \( e_{i+1} \) into \( E^* \) and update \( G^* \), which is still isomorphic to some subgraph of \( A_G \). If \( i + 1 < n \), we continue to consider \( e_{i+2} \) till there is no edge left in \( E_{\text{circ}}^w \). In this way, we obtain a subgraph \( G^* \) of \( G_{\text{circ}}(C) \) that is isomorphic to some subgraph of \( A_G \). The sum of weights of edges in \( G^* \), though not necessary the largest, is sufficiently large among all subgraphs of \( G_{\text{circ}}(C) \) that are isomorphic to some subgraph of \( A_G \). Using the VF2 algorithm, we can find an embedding \( \tau_{\text{wgt}} \) which embeds \( G^* \) into \( A_G \). Again, we note that \( \tau_{\text{wgt}} \) might be a partial mapping from \( Q \) to \( V \).

In the following, we call \( \tau_{\text{top}} \) the topgraph initial mapping and call \( \tau_{\text{wgt}} \) the weightgraph initial mapping of \( LC \). Besides these two initial mappings, we also introduce a method for evolving an initial mapping from the empty mapping. A similar idea was used by Zulehner et al. \[14\], while we extend a partial mapping only when necessary, i.e., when the thus extended mapping can execute a two-qubit gate in the current front layer or it can reduce the minimum physical distance (cf. Sec. 3.1) between qubits in a two-qubit gate in the current front layer. This mapping extension technique is also used when \( \tau_{\text{top}} \) or \( \tau_{\text{wgt}} \) is incomplete.

### 3.3 Fixed-Depth Heuristic Search

In most search-based algorithms for the qubit mapping problem, a heuristic function is used to select an action (i.e., a swap or a sequence of swaps) which can maximally reduce the sum or the minimum of the distances between the two qubits in the CNOT gates of the front layer and, sometimes, the lookahead layer.

For each edge \( e = \{v, v'\} \) in \( A_G \) there is an associated swap operation, written \( \text{swap}(e) \), which swaps the states on \( v \) and \( v' \). More precisely, suppose \( \tau \) is the current mapping and \( \tau(q) = v, \tau(q') = v' \). Then \( \text{swap}(e) \) transforms \( \tau \) into a new mapping \( \tau' \) such that \( \tau'(q) = v', \tau'(q') = v, \text{ and } \tau'(q^*) = \tau(q^*) \text{ for } q^* \notin \{q, q'\} \). In case if \( \tau(q) \) is not defined and \( \tau(q') = v' \), then \( \tau(q') \) is not defined and \( \tau(q) = v' \). The case when \( \tau(q') \) is not defined and \( \tau(q) = v \) is analogous. If both are undefined, then \( \tau' = \tau \). We often write \( \text{swap}(e) \circ \tau \) for \( \tau' \).

**Example 4** (Example 1 cont’d). For the three qubit mappings in Fig. 4, we have \( \tau_2 = \text{swap}(1, 6) \circ \tau_1 \) and \( \tau_3 = \text{swap}(6, 10) \circ \tau_2 \).

In this section, we propose a new heuristic function which measures how efficient the mapping can execute gates in the logical circuit. For convenience and by abuse of
terminology, we say a CNOT gate not in the front layer is executable by a mapping \( \tau \) if the gate itself and all CNOT gates it depends on are satisfiable by \( \tau \).

Starting with a selected initial mapping \( \tau^0 \), we write \( s^0 = (\tau^0,PC^0,LC^0) \) for the initial state of the search process, where \( LC^0 \) is obtained by removing all CNOT gates \( (q,q') \) that are executable by \( \tau^0 \) from \( LC \), and \( PC^0 \) is obtained by adding the corresponding CNOT gates \( (\tau^0(q),\tau^0(q')) \) in an empty physical circuit. Step by step, we select an action \( a \) from \( S \), the set of sequences of SWAPs on \( \mathcal{A}_G \) and enforce all SWAPs in \( a \) one by one to get the next mapping (and the next state) till there are no gates left in the logical circuit.

Suppose \( s^i = (\tau^i,PC^i,LC^i) \) is the current state and all gates that are executable by \( \tau^i \) are already removed from \( LC^i \). For a sequence \( a = (\text{SWAP}1,\text{SWAP}2,\ldots,\text{SWAP}_\ell) \) of SWAPs on \( \mathcal{A}_G \), we define a function

\[
gval(\tau^i,a) = \frac{\text{number of gates executable by } \tau^i}{\text{len}(a) \times 3},
\]

where \( \tau^i \) is the mapping obtained by enforcing SWAPs in action \( a \) one by one on \( \tau^i \) and \( \text{len}(a) = \ell \) is the number of SWAPs in \( a \). Recall each SWAP is implemented by three CNOT gates (see Fig. 2(right)).

Our action set consists of all sequences of SWAPs on \( \mathcal{A}_G \) and we select any one with the maximal value, i.e., we select \( a^* \) from

\[
\arg \max_{a \in S} \ gval(\tau^i,a).
\]

After selecting \( a^* \), we enforce on \( \tau^i \) SWAPs in \( a^* \) one by one and obtain the next mapping \( \tau^{i+1} \). Then we remove all gates that are executable by \( \tau^{i+1} \) from \( LC^i \) and write \( LC^{i+1} \) for the resulted logical circuit. In the meanwhile, we append to \( PC^i \) three CNOT gates (as in Fig. 2(right)) for each SWAP in \( a^* \), and a CNOT gate \( (\tau^{i+1}(q),\tau^{i+1}(q')) \) for each CNOT gate \( (q,q') \) removed from \( LC^i \). In this way, we obtain \( PC^{i+1} \) and the next state \( s^{i+1} = (\tau^{i+1},PC^{i+1},LC^{i+1}) \).

Apparently, considering all sequences of SWAPs is inefficient. In practice, we propose to consider actions with up to \( k \) SWAPs for some fixed \( k \geq 1 \). In particular, for IBM Q Tokyo, we select \( k = 3 \), which reflects a good compromise between efficiency and effectiveness.

**Example 5 (Example 1, cont’d).** Suppose \( \tau_1 \) is the qubit mapping which maps \( q_0,q_1,q_2,q_3 \) to, respectively, \( v_2,v_0,v_{10},v_6 \), see Fig. 2(left). As the front layer contains only \( q_0 = (q_2,q_0) \), which is not executable by \( \tau_1 \), there are no gates in \( LC \) that can be executed by \( \tau_1 \). Examining all sequences of up to 3 SWAPs, the four best actions are as follows:

- \( a_1 = (\text{SWAP}(1,6),\text{SWAP}(6,10)) \), which can execute all 7 gates in \( LC \);
- \( a_2 = (\text{SWAP}(5,6),\text{SWAP}(2,6)) \), which can execute all 7 gates in \( LC \);
- \( a_3 = (\text{SWAP}(6,7),\text{SWAP}(6,10)) \), which can execute all but the last gate in \( LC \);
- \( a_4 = (\text{SWAP}(6,11),\text{SWAP}(2,6)) \), which can execute all but the last gate in \( LC \).

The fifth best action contains 3 SWAPS. Thus \( a_1 \) and \( a_2 \) are optimal actions, with the optimal value \( gval(\tau_1,a_1) = gval(\tau_1,a_2) = 7/6 \).

### 3.3.1 Heuristics used in related works

Now it is a good time to compare our heuristic function with those used in the related works.

Zulehner et al. [14] selected the action that results in a mapping which can execute all gates in the front layer and the lookahead layer. The action consists of a sequence of SWAPS and is selected by using \( A^* \) search and the following heuristics:

\[
h(\tau) = \sum_{(q,q') \in \mathcal{L}_0 \cup \mathcal{L}_1} \left\{ 3 \times (\text{dist}_{\mathcal{A}_G}(\tau^i(q),\tau^i(q')) - 1) \right\},
\]

where \( \mathcal{L}_0 \) and \( \mathcal{L}_1 \) are the first two layers of the current logical circuit and, for any two-qubit gate \( (q,q') \), \( \text{dist}_{\mathcal{A}_G}(\tau^i(q),\tau^i(q')) \) is the distance from \( \tau^i(q) \) to \( \tau^i(q') \) in \( \mathcal{A}_G \). The heuristic cost is not admissible and thus an optimal action is not guaranteed. Moreover, the worst-case time complexity of this \( A^* \) search algorithm is exponential in the number of logical qubits.

Childs et al. [16] selected the action which can maximally reduce the total distance between qubits in the CNOT gates in the current front layer, i.e.,

\[
R(\tau^i) = \sum_{(q,q') \in \mathcal{L}_0} \text{dist}_{\mathcal{A}_G}(\tau^i(q),\tau^i(q')).
\]

Their algorithm is polynomial in all relevant parameters but its performance is not directly compared with the \( A^* \) algorithm in [14].

To overcome the inefficiency of the \( A^* \) search algorithm, several researchers (see, e.g., [15], [17]) proposed to select a single SWAP each time. Their methods are more efficient than the \( A^* \)-approach when processing logical circuits with more than 15 qubits. In [15], Li et al. designed a heuristic cost function that can reduce the sum of distances between the two qubits in each two-qubit gate in the front (and the lookahead) layers. Analogously, Cowtan et al. [17] used a heuristic cost function that can reduce the diameter of the subgraph composed of all qubits in the two-qubit gates of the front layer. In the evaluation section, we will see that the efficiency of these algorithms is partially achieved at the cost of the quality of the output physical circuit.

In the SAHS algorithm [18], we introduced a heuristic function that supports weight parameters to reflect the variable influence of gates in different layers. In each step, instead of selecting the action with the minimal cost, SAHS selects the SWAP which has the best consecutive SWAP to apply.

### 3.4 Optimisation and Fallback

Considering all sequences of up to \( k \) SWAPs is still not efficient for devices with a medium to large architecture graph. Let \( \tau \) be the current mapping and \( \mathcal{L}_i \) the current \( i \)-th (\( 0 \leq i \leq k \)) layer. Write \( Q_i \) for the set of logical qubits in \( \mathcal{L}_i \). It’s natural not to consider SWAPs that do not interact with gates in the first one or several layers. This idea was used for edges in the front layer, e.g., [14], [15], [18].

For an edge \( e = (v,v') \), if neither \( \tau^{-1}(v) \) nor \( \tau^{-1}(v') \) is in \( Q_0 \), then swapping \( v \) and \( v' \) does not reduce the minimum distance between qubits in a two-qubit gate in the current front layer, viz. \( Q_0 \). Therefore, it is reasonable to introduce
the following filter for selecting an action \(a = (e_1, e_2, ..., e_\ell)\) with at most \(k\) SWAPS:

1. \(Q_0\)-filter: We say \(a = (e_1, e_2, ..., e_\ell)\) is a \(Q_0\)-plausible action if, for any edge \(e_j = \{v, v'\}\) of \(a\), we have either \(\tau_{j-1}(v) = \tau_j(v')\) is in \(Q_0\), where \(\tau_0 \equiv \tau\) and \(\tau_j\) is obtained from \(\tau_{j-1}\) by enforcing \(\text{SWAP}(e_j)\) for \(1 \leq j \leq \ell\).

Similarly, we could look ahead and introduce \(Q_i\)-filter for \(0 < i < k\).

2. \(Q_i\)-filter: We say \(a = (e_1, e_2, ..., e_\ell)\) is a \(Q_i\)-plausible action if, for any edge \(e_j = \{v, v'\}\) of \(a\) with \(j > i\), we have either \(\tau_{j-1}(v) = \tau_j(v')\) is in \(Q_i\), where \(\tau_0 \equiv \tau\) and \(\tau_j\) is obtained from \(\tau_{j-1}\) by enforcing \(\text{SWAP}(e_j)\) for \(1 \leq j \leq \ell\).

The above \(Q_i\)-filter could be weakened by requiring that either \(\tau_{j-1}(v) = \tau_j(v')\) is in (a subset of) \(Q_0 \cup Q_1 \cup ... \cup Q_i\).

In our evaluation, we used various combinations of \(Q_0\) and \(Q_i\) filters and the results are very promising (see Sec. 3.4).

It should be stressed that, sometimes, \(Q_0\)-filter may ‘filter’ out optimal actions.

**Example 6 (Example 1 cont’d).** Note that \(Q_0 = \{0, 2\}\) and \(\tau_1(q_0) = v_2\), \(\tau_1(q_2) = v_1\). Each \(a_i\) for \(1 \leq i \leq 4\) in Example 6 is not \(Q_0\)-plausible. Thus our algorithm with \(Q_0\)-filter cannot find an optimal action. In fact, the following \(Q_0\)-plausible action is selected by our algorithm

\[
\left\{ \begin{array}{c}
\bullet \quad a_5 = (\text{SWAP}(2, 7), \text{SWAP}(1, 6), \text{SWAP}(6, 10)). \\
\end{array} \right.
\]

This action (see Fig. 4) can execute all 7 gates in \(LC\) and has \(\text{gval}(\tau_1, a_5) = 7/9\).

Another type of filters is also introduced in our algorithm. Let \(\tau\) be the current mapping and \(L_i\) the \(i\)-th layer of the current logical circuit. Recall the notion of physical distance defined in Sec. 3.4 and assume that \(\gamma \in [0, 1]\) is a discount factor and \(s \geq 0\). For two mappings \(\tau_1\) and \(\tau_2\), we say \(\tau_1\) is \(s\)-better than \(\tau_2\) if \(\bar{R}_s(\tau_1) < \bar{R}_s(\tau_2)\), where for \(i = 1, 2\) we have

\[
\bar{R}_s(\tau_i) = \sum_{\ell=0}^s \left( \sum_{(q,q') \in L_\ell} \text{dist}_{\text{ph}}(q, q', \tau_i) \right). \tag{4}
\]

Intuitively, \(\tau_1\) being \(s\)-better than \(\tau_2\) implies that it is easier to transform all gates in the first \(s\) levels if we start from \(\tau_1\) instead of \(\tau_2\), or, in other words, the ‘distance’ from \(\tau_1\) to the first \(s\) levels is shorter than that from \(\tau_2\).

Analogously, we define the \(D_s\)-filter as follows.

3. \(D_s\)-filter: We say \(a = (e_1, e_2, ..., e_\ell)\) is a \(D_s\)-plausible action if \(\tau_{j-1}\) is not \(s\)-better than \(\tau_j\) for any \(1 \leq j \leq \ell\), where \(\tau_0 \equiv \tau\) and \(\tau_j\) is obtained from \(\tau_{j-1}\) by enforcing \(\text{SWAP}(e_j)\) for \(1 \leq j \leq \ell\).

Note that if \(\gamma = 0\) then \(D_s\)-filter is the same as \(D_0\)-filter.

**Fallback**

For a prefixed positive integer \(k\), it is possible that, in some cases, no sequence of \(k\) SWAPS with length \(\leq k\) can lead to a mapping which can execute any CNOT gate in the current front layer. If this is the case, we use the following natural fallback:

\[
\text{Fallback: Select any SWAP that can reduce } \text{FB}(\tau), \text{the minimum distance between qubits in a two-qubit gate in the current front layer, which is formally defined as follows:}
\]

\[
\text{FB}(\tau) = \min_{(q,q') \in e_0} \text{dist}_{\text{AS}}(\tau(q), \tau(q')). \tag{5}
\]

It is worth noting that, for our experiments on IBM Q Tokyo and an extensive set of logical circuits, the fallback is rarely activated.

**3.5 Complexity Analysis**

From above we can see that our QCT algorithm has two independent processes:

1. the initial mapping construction process, and
2. the search process.

The construction of the topgraph and wgtgraph initial mappings requires determining if a graph is embeddable in another graph, which in the worst-case has time complexity exponential in the number of qubits. Although it is an NP-complete problem, there are practical and efficient algorithms, say the VF2 algorithm [22], which can quickly solve the subgraph isomorphism problem for graphs with several thousands nodes. Fortunately, the QCT problem in the NISQ era considers only graphs with up to 1000 nodes and thus, by using VF2, we can construct the topgraph and wgtgraph initial mappings in a reasonable time. Experiments on various architecture graphs with up to 361 nodes and circuits with up to 50 qubits and 15,000 CNOT gates confirm that the time consumption is acceptable. Please see Sec. 5.3 for detailed empirical results and discussion.

In the following we give a rough estimation of the complexity of the search process of our algorithm.

Suppose \(LC = (Q, C)\) is a logical circuit and \(AG = (V, E)\) the architecture graph of a NISQ device. Write \(|Q|, |V|, \text{ and } |E|\) for, respectively, the cardinalities of \(Q, V, \text{ and } E\). Let \(m\) be the number of CNOT gates in \(C\), \(\text{diam}\) and \(\text{deg}\) the diameter and maximum degree of \(AG\), respectively.

We have the following simple observations:

\[
\text{• The dependency graph of } LC\text{ can be computed in time linear in } m, \text{ the number of CNOT gates in } C. \\
\text{• For any mapping } \tau \text{ and any logical circuit } LC, \text{ we can identify (and remove from } LC \text{ as well as from its dependency graph) in time linear in } m \text{ the set of gates in } LC \text{ executable by } \tau.}
\]

We first consider the ideal case when fallback is never activated during the search process. As described in Sec. 3.3 starting with a selected initial mapping \(\tau^0\), step by step, we select an action \(a\) consisting of up to \(k\) SWAPS on \(AG\) and enforce all SWAPS in \(a\) one by one to get the next mapping till there are no gates left in the logical circuit. Suppose \(s^i = (\tau^i, PC^i, LC^i)\) is the current search state. As there are at most \(O(|E|^k)\) actions with up to \(k\) SWAPS, we can generate at most \(O(|E|^k)\) different mappings from \(\tau^i\). To select from these mappings the one which can execute the most gates in \(LC^i\), we need time \(O(|E|^k \cdot m)\) (cf. the second observation above). Because each step removes at least one CNOT from \(LC\), in at most \(O(|E|^k \cdot m^2)\) time, we can execute all gates in \(LC\). This is often an overestimated upper bound. If any \(Q\)-filter is used, there are at most \(|Q|^k \cdot \text{deg}^k\) actions with up to
k swaps, where deg is the maximum degree of $AG$—which is 6 for IBM Q Tokyo and 4 for grid-like AGs.

Now, suppose fallback is activated. Since each activation of the fallback reduces by (at least) one the minimum distance between qubits in a CNOT gate in the current front layer (i.e., $FB(\tau)$ in Eq. 3), the whole search process activates the fallback procedure at most $m \times \text{diam}$ times. Note that each activation (see Eq. 3) needs to compute the shortest distance between the control and target qubits in a CNOT gate in the front layer of the current logical circuit and there are at most $|Q|/2$ CNOT gates in the front layer. Using Dijkstra’s algorithm with lists, $FB(\tau)$ can be computed in time $O(|Q| \cdot |V|^2)$. Thus the total fallback on-cost is at most $O(|Q| \cdot |V|^2 \cdot m \cdot \text{diam})$.

Therefore, the overall space complexity of the search process is $O(|E|^k \cdot m^2 + |Q| \cdot |V|^2 \cdot m \cdot \text{diam})$. As $|Q| \leq |V| \leq |E| + 1$ and diam is usually very small when compared with $m$, the overall space complexity is bounded by $O(|E|^k \cdot m^2)$ if $k \geq 3$. In practice, this could be significantly reduced if we use Q-filters as the base in $|E|^k$ can be significantly reduced.

As for the space complexity, in each state $s$, we maintain, besides the logical and physical circuits, the dependency graph of the current logical circuit and the set of plausible actions with up to $k$ swaps. Thus the space complexity of the algorithm is bounded by $O(|E|^k + m)$.

## 4 Evaluation

In this section, we compare our approach with the SABRE algorithm of Li et al. [15], the Cambridge algorithm of [17], and our qubit transformation algorithm SAHS based on simulated annealing and heuristic search [18], which are three state-of-the-art algorithms for the qubit mapping problem on IBM Q Tokyo (see Fig. 1). Although we focus on a particular NISQ device in the evaluation, our approach is applicable to any undirected architecture graph, including Rigetti 16Q Aspen-4, IBM Q Rochester and Google’s Sycamore. We use Python as our programming language and IBM Qiskit as auxiliary environment. All experiments are conducted in a MacBook Pro with 3.1 GHz Intel Core i5 processor and 8GB memory.

As for benchmark circuits, we consider all publicly available circuits evaluated in [15] or [17]. Note that only CNOT gates are considered in our comparison. For each individual circuit, we extract all its CNOT gates and use the thus reduced circuit as the input of our qubit mapping algorithm. We then compare the involved algorithms in terms of the number of logical and physical circuits, the dependency graph of the current logical circuit and the set of plausible actions with up to $k$ swaps. Thus the space complexity of the algorithm is bounded by $O(|E|^k + m)$.

### 4.1 Comparison Among Different Initial Mappings

We first compare the two subgraph isomorphism related initial mappings (viz., the topgraph initial mapping $\tau_{\text{top}}$ and the wgtgraph initial mapping $\tau_{\text{wgt}}$) introduced in Section 3 with the empty mapping and the naive initial mapping (which maps $q_i$ to $v_i$ for each $q_i$ in $Q$). Table 1 summarises the results for all (small, medium, large) circuits in $B_{c}$. For each of these circuits and each initial mapping, the transformation can be completed within about 500 seconds by using our algorithm.

From Table 1 we can see that the two isomorphism subgraph related initial mappings, $\tau_{\text{top}}$ and $\tau_{\text{wgt}}$ are significantly better than the empty initial mapping and the naive initial mapping for small and medium circuits, but the difference is not significant when large circuits are evaluated. This is not a surprise as the search heuristics plays a dominant role if the circuit has a large size. Note that if a logical circuit can be transformed into a physical circuit with zero overhead, our algorithm, when using either the topgraph or wgtgraph initial mapping, will very likely detect this.

Since the topgraph initial mapping is slightly better than the other three initial mappings, in the following, when compared with other algorithms, we always use the topgraph initial mapping.

### 4.2 Comparison with SABRE, Cambridge, and SAHS

We then compare our algorithm with SABRE [15] on the small benchmark set $B_{s}$ of circuits used in [15]. We use the topgraph initial mapping $\tau_{\text{top}}$. Recall that SABRE starts with a random initial mapping. For each circuit, we execute SABRE on our computer 5 times and take as the overhead the smallest number of added gates out of the 5 attempts and take its time consumption as the total time of the 5 attempts. The results are reported in Table 2 where we can see that the running time of SABRE is comparable with ours.

Let $n_{\text{sabre}}$ and $n_{\text{ours}}$ be the numbers of CNOT gates added, respectively, by SABRE and by ours. The ‘Comparison’ column of Table 2 shows the ratio $n_{\text{ours}}/n_{\text{sabre}}$, which is set as 1 if $n_{\text{ours}} = n_{\text{sabre}} = 0$. Apparently, the smaller
the ratio is, the better our algorithm performs. From Table 2 we can see that only one circuit has ratio larger than 1. For all circuits with more than 500 CNOT gates, the ratio is at most 62%. In terms of the CNOT index, we have successfully decreased the index $I_{CNOT}^B$ from $1 + 47808/50534 = 1.9461$ to $1 + 20790/50534 = 1.4114$.

We further compare our algorithm with the Cambridge algorithm of [17] and our SAHS algorithm [18] on the large benchmark set $B_c$, which contains 131 circuits. A summary of the results in terms of the CNOT index is presented in Table 1. It is worth stressing that the results of the Cambridge algorithm as presented in Table 1 are obtained without using postmapping optimisations. Precisely, we have removed the following codes from their algorithm:

- ‘Transform.OptimisePhaseGadgets().apply(tkcirc)’
- ‘Transform.OptimisePostRouting().apply(outcirc)’

This is because the Cambridge algorithm was implemented in C++ and compiled, and the above postmapping optimisation codes are not directly transplantable to our algorithm. To provide a fair comparison, we did not do any postmapping optimisations in our algorithm either. In Table 1 we didn’t include the time information of these algorithms. However, we note that Cambridge is super fast; it takes only 5.2 seconds to transform the 131 circuits in $B_c$!

From Table 1 we can see that, for the benchmark set $B_c$, the $I_{CNOT}^B$ index of our algorithm is 1.4231, while the indices for SAHS and Cambridge are, respectively, 1.4761 and 1.8154. This shows that our algorithm can in average generate significantly better results than Cambridge and SAHS. This is particularly true for large circuits which contain 1000 or more CNOT gates. When compared with SAHS, our algorithm is slightly better for small circuits, 2 points (1.2886 vs. 1.3101) better for medium circuits, and 4.8 points better for large circuits (1.4280 vs. 1.4763). Both algorithms are significantly better than Cambridge in all three categories.

In the above experiments, we used $Q_0$-filter for the first SWAP and $Q_1$-filter (see Section 5.4) for all the other SWAPS when filtering actions with up to 3 SWAPS. If we use $Q_0$-filter for all SWAPS, then the index becomes 1.4774, which is about 5 points inferior to the index 1.4231 reported in Table 1. However, if we weaken $Q_1$-filter by using the qubits in the front layer and the lookahead layer, then the index could be further improved to 1.3801 from 1.4231. We denote by Q01x this weakened combination of $Q_0$ and $Q_1$-filters. This better performance is achieved at the cost of relatively slower search process: the total time consumption for the whole benchmark set is now 13,224 seconds, or 3.7 hours, while for six very large circuits (e.g., ’mlp4_245’ with 16 qubits and 8232 CNOT gates), the transformation process requires 900-1600 seconds.

6. Shortly we will analyse why our algorithm works bad on this circuit in Example 7, Sec. 5.2.

### 5 Further Discussion

From the above evaluation, we can see that our algorithm has significant better performance on IBM Q Tokyo than state-of-the-art algorithms. In this section, we give a more detailed discussion on the effectiveness, extensibility and time efficiency of our algorithm. In particular, we report more experiments on three larger architecture graphs, viz., Sycamore (53 qubits), Rochester (53 qubits), and an artificial 19x19 Grid-like device with 361 qubits, called Q19x19.

#### 5.1 Extension

Our filtered depth-limited approach actually can adopt heuristic value functions other than Eq. 1. Indeed, we have implemented another value function based on the function specified in Eq. 4. The new heuristic value function is obtained by replacing “number of gates executable by $\tau$” in Eq. 3 with $\hat{R}_s(\tau) - \hat{R}_s(\tau')$, the difference of the ‘distance’ to the first $s$ levels of the current logical circuit from $\tau$ and $\tau'$. In this way we have a new value function

$$dval_s(\tau, a) = \frac{\hat{R}_s(\tau) - \hat{R}_s(\tau')}{|\text{len}(a)| \times 3},$$

where $\tau'$ is the mapping obtained by enforcing SWAPS in action $a$ one by one on $\tau$ and $\text{len}(a) = \ell \leq k$ is the number of SWAPS in $a$. Using this value function, we then select any action with the maximal $D$-value as our next action. To distinguish between the two implementations of our algorithm, we call the one using $dval$ as FiDLS-Gs, and the other using $dval$ as FiDLS-Ds, where $s$ indicates the level of gates we considered. It is easy to see that FiDLS-Ds has the same computational complexity as FiDLS-Gs.

#### 5.2 Effectiveness

While it works much better in average and especially on large circuits, our algorithm performs not better on several small or medium circuits. For example, the circuit ‘alu_v0_27’ contains 5 qubits and 17 CNOT gates. To execute it on IBM Q Tokyo, our QCT algorithm needs to insert 3 (2, resp.) swaps if the topograph (wgtgraph, resp.) initial mapping is used, while both Cambridge and SABRE only require 1 swap.

This bad performance is perhaps due to three reasons. First, during the search process, our algorithm works in a greedy way and always tries to find the action with the best value. This, however, often leads to a series of optimal local transformations, which gives no guarantee on the optimality of the global transformation. Second, there are many different mappings which can embed a given graph into $AG$. Our algorithm selects an arbitrary one. Selecting a better embedding by, for instance, comparing their $\hat{R}_s$ value (cf. Eq. 4) may further improve the performance of our algorithm. Third, our selection of the initial mapping
Table 2

Comparison of our algorithm with SABRE in [15] on IBM Q Tokyo. The numbers in the last column indicate the ratio of our added CNOT gates (with the topgraph initial mapping) against that of SABRE.

| Circuit Name | qubit no. | input gate | input CNOT | SABRE added | SABRE time (s) | topgraph added | topgraph time (s) | Comp. |
|--------------|-----------|------------|------------|-------------|----------------|----------------|------------------|-------|
| 4mod3-v1_22  | 5         | 21         | 11         | 0           | 0.02           | 0              | 0                | 1     |
| mod5slls_65 | 5         | 35         | 16         | 9           | 0.03           | 0              | 0                | 0     |
| alu-v0_27   | 5         | 36         | 17         | 3           | 0.03           | 9              | 0.07             | 3     |
| decod24-v2  | 4         | 52         | 22         | 12          | 0.04           | 0              | 0                | 0     |
| 4gt13_92    | 5         | 66         | 30         | 21          | 0.05           | 0              | 0                | 0     |
| ising_model_10 | 10       | 480       | 90         | 0           | 0.09           | 0              | 0                | 1     |
| ising_model_13 | 13       | 633       | 120        | 0           | 0.12           | 0              | 0                | 1     |
| ising_model_16 | 16       | 786       | 150        | 0           | 0.23           | 0              | 0                | 1     |
| qft_10      | 10        | 200       | 90         | 48          | 0.17           | 39              | 1.6              | 0.81  |
| qft_16      | 16        | 512       | 240        | 171         | 0.57           | 153             | 21.06             | 0.89  |
| rd84_142    | 15        | 343       | 154        | 141         | 0.36           | 72              | 5.01              | 0.51  |
| adr4_197    | 13        | 3439      | 1498       | 1185        | 5.69           | 630             | 19.85             | 0.53  |
| radd_250    | 13        | 3213      | 1405       | 1092        | 4.98           | 555             | 28.21             | 0.51  |
| sym5_268    | 11        | 3073      | 1343       | 1072        | 3.92           | 630             | 16.19             | 0.59  |
| wism6_145   | 7         | 3888      | 1701       | 1290        | 6.63           | 513             | 2.93              | 0.40  |
| missex1_241 | 15        | 4813      | 2100       | 1275        | 9.22           | 786             | 24.62             | 0.62  |
| rd72_252    | 10        | 5321      | 2319       | 2250        | 9.94           | 1095            | 9.72              | 0.49  |
| cycle10_2_110 | 12    | 6050      | 2648       | 2406        | 14.32          | 1194            | 10.93             | 0.50  |
| square_root_7 | 15      | 7630      | 3089       | 2403        | 19.06          | 1338            | 228.29            | 0.56  |
| sqn_258     | 10        | 10223     | 4459       | 4404        | 37.01          | 1578            | 17.73             | 0.36  |
| rd84_253    | 12        | 13658     | 5960       | 6291        | 39.57          | 2352            | 54.35             | 0.37  |
| co14_215    | 15        | 17936     | 7840       | 8946        | 34.77          | 4257            | 128.33            | 0.48  |
| sym9_193    | 11        | 34881     | 15232      | 14790       | 406.19         | 5589            | 70.29             | 0.38  |
| sum         | -         | 117289    | 50534      | 47908       | 593.01         | 20790           | 639.18            | 0.43  |

Table 3

The circuit graph (Fig. 5 (left)) is not embeddable in \( \mathcal{AG} \), the architecture graph of IBM Q Tokyo (cf. Fig. 1). A part of \( \mathcal{AG} \) is shown in the right of Fig. 5. Let \( C_{\text{top}} \) be the sub-circuit of the first 10 gates in \( C \). Then the circuit graph of \( C_{\text{top}} \) is the topgraph of \( C \) and can be embedded in \( \mathcal{AG} \). Let \( \tau' \) be such an embedding. After removing gates in \( C_{\text{top}} \), the rest gates (involving only qubits 0, 2, and 4) cannot be solved with one swap from \( \tau' \). However, letting \( \tau \) be the mapping as shown on the right of Fig. 5 we can see that \( \tau \) solves only the first 9 gates but, after swapping 0 and 1, all the rest 7 gates can be solved.

Example 7. Consider the circuit 'alu-v0_27', which contains 5 qubits and the 17 CNOT gates in

\[
C = (3, 4), (2, 1), (1, 3), (2, 1), (3, 2), (3, 1), (2, 1), (3, 2), (1, 3), (2, 0), (0, 4), (2, 0), (4, 2), (4, 0), (2, 0), (4, 2), (0, 4)).
\]

The circuit graph (Fig. 5 (left)) is not embeddable in \( \mathcal{AG} \), the architecture graph of IBM Q Tokyo (cf. Fig. 1). A part of \( \mathcal{AG} \) is shown in the right of Fig. 5. Let \( C_{\text{top}} \) be the sub-circuit of the first 10 gates in \( C \). Then the circuit graph of \( C_{\text{top}} \) is the topgraph of \( C \) and can be embedded in \( \mathcal{AG} \). Let \( \tau' \) be such an embedding. After removing gates in \( C_{\text{top}} \), the rest gates (involving only qubits 0, 2, and 4) cannot be solved with one swap from \( \tau' \). However, letting \( \tau \) be the mapping as shown on the right of Fig. 5 we can see that \( \tau \) solves only the first 9 gates but, after swapping 0 and 1, all the rest 7 gates can be solved.

5.3 Scalability and More on Time Complexity

In Sec. 3.5 we have seen that the search process of our algorithm is polynomial in all relevant parameters. As we go deeper in the search tree, our algorithm becomes considerably slower than Cambridge. The significant decrease of the CNOT index shows that this is, however, worthwhile.

In contrast with the search process, the initial mapping construction process relies on the efficiency of subgraph isomorphism algorithms, which have time complexity exponential in the number of qubits in the circuit and the AG. We argue that this is not a serious problem for the following reasons. First, for the QCT problem in the NISQ era, only graphs with up to 1000 nodes are involved, which are manageable by existing algorithms like VF2 [22]. Second, the architecture graphs usually have very simple and regular (e.g., grid-like) topologies, which can be exploited to design customised efficient subgraph isomorphism algorithms. Last but not least, good approximate solutions can often do the job well. This is partially evidenced by the results summarised in Table 1 where it shows that, for large circuits, the transformation results with an empty mapping are only slightly inferior to that using the selected topgraph initial mappings.

To further evaluate the effectiveness and efficiency of our approach, we have experimented on IBM Q Rochester (53 qubits), Google’s Sycamore (53 qubits), and the artificial 19×19 grid architecture graph Q19x19, which has 361 nodes and each node has at most 4 neighbours. The results are summarised in Table 3 where we adopted the two value functions specified in Eqs. 1 and 6, respectively. The two search methods are noted as FDIS-G and FDIS-D, respectively, where the latter uses the \( D_2 \)-filter and the discount factor \( \gamma \) in Eq. 6 is fixed as 0.8 and all other parameters are same as in Sec. 4.

Table 3

From Table 3 we can see that Cambridge is super fast. This is partially because it is implemented in C++, which is usually 10-100 times faster than the same Python program. Nevertheless, when the number of nodes of the AG goes
We have proposed a new algorithm for qubit mapping based on subgraph isomorphism and filtered depth-limited search. Our algorithm, called FdLS, can significantly reduce the extra two-qubit gates required in the output circuit. If the input circuit can be executed directly, FdLS can very likely detect this. It seems that this nice property is not enjoyed by many other approaches.

From our experimental results, we can see that, when the circuit has less than 1000 two-qubit gates, our subgraph isomorphism induced initial mappings are much better than empty mappings and naive mappings that assign the $i$-th qubit in the logical circuit to the $i$-th qubit in the quantum device. Experiment results on a large set of 131 benchmark circuits show that FdLS performs significantly better than state-of-the-art algorithms on IBM Q Tokyo, the architectural graph of which has a relatively large average node degree and smaller diameter. More experiments on three large NISQ devices with up to 361 qubits and the 131 benchmark circuits as well as 19 additional benchmark circuits with 20-50 qubits further demonstrated the scalability, efficiency, and effectiveness of our algorithm.

Siraichi et al. [25] suggested to allocate qubit by combining subgraph isomorphism with token swapping. The idea is to partition the input circuit into a series of segments each of which can be executed by finding an appropriate mapping and then ‘glue’ these mappings by token swapping. Experiment results in [25] show that their algorithm can produce output circuits with 16% less gates than SABRE on IBM Q Tokyo, which is not better than our results as reported in Table 2. This is perhaps due to that a series of optimal local mappings do not always lead to an optimal global one. See Example 7 for such a counter-example.

A weighted graph like ours (see Section 5.2) is also introduced in a recent work [29], where Lin, Anschuetz, and Harrow exploited spectral graph theory to qubit mapping. The performance of their algorithm is in general not better than the $A^*$ approach of [14]. They also suggested to use their “spectral mapper to provide an initial mapping” while its effectiveness needs further investigation.

It seems that we are still quite far from devising algorithms that could output circuits with nearly minimal overheads. Future work will investigate along the following directions:

- A better, possibly customised, subgraph isomorphism algorithm will improve the quality of our results. The approximate subgraph isomorphism algorithm proposed in [25] seems a promising one.
- Minimising depth or latency and circuit error is also important for qubit mapping. Although the number of CNOT gates in our output circuit is already smaller than the depth of the output circuit (only CNOT gates are counted) of some compared algorithms [17] (see [18] for a more detailed analysis), it

\[ \text{TABLE 4} \]

Performance of our algorithm on four AGs and benchmark $B_{19x19}$, where Cambridge is implemented in C++ and times are in seconds.

from 20 to 361, the time consumption of our algorithm does not deteriorate too much while that of Cambridge increases more than 800 times.

As circuits in the benchmark set $B_n$ have only up to 16 qubits, we also tested another benchmark of circuits with large number of qubits. The benchmark $B_{19x19}$ and first used in [24], consists of a selection of circuits for Quantum Computational Chemistry generated using the Qiskit chemistry package [23]. $B_{19x19}$ contains 19 circuits with 20-50 qubits and up to 15000 CNOT gates. Results are summarised in Table 3, where we can see that the running time of our algorithm on Q19x19 is comparable with that of Cambridge (implemented in C++).

As for the effectiveness on the three large NISQ devices, our algorithm does not perform consistently better than Cambridge. For benchmark $B_{19x19}$, which contains 131 circuits with up to 16 qubits, Table 3 shows that FdLS-D and Cambridge perform better than FdLS-G. However, for benchmark $B_{bigQ}$, Table 4 shows that our algorithm performs better than Cambridge on all three large NISQ devices, which is particular true for Sycamore and Q19x19. While we are not certain why this happens, it may be related to the following facts: (a) the AG of IBM Q Tokyo has larger average degree and smaller diameter than the other three large AGs, and (b) when searching for the best SWAP action, Cambridge tends to keeps the occupied qubits staying together. The former fact seems especially favourable for FdLS-G while the latter fact seems very helpful for Cambridge when compiling circuits with small number of qubits on large AGs but this is not the case when compiling circuits with large number of qubits.

Remark 1. From Table 4, we can see that the I-index results on Q19x19 are not always better than that on Sycamore. This implies that both Cambridge and our algorithm did not exploit the fact that the AG of Sycamore is embeddable into that of Q19x19 and, thus, every circuit that is executable on Sycamore can be executed on Q19x19 with a good initial mapping. This observation should be included in the implementation of every QCT algorithm.
will be nice if we can adapt our approach to address other or multiple optimisation objectives.

- Machine learning and deep learning algorithms may be designed to quickly select the best action in Eq. (2) especially when the search depth becomes large.

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**ACKNOWLEDGEMENTS**

This work was partially supported by the National Key R&D Program of China (Grant No. 2018YFA0306704) and the Australian Research Council (Grant No. DP180100691).