Experimental demonstration of single-flux-quantum sequential-access mask ROM

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Abstract: We present a superconducting single-flux-quantum (SFQ) mask ROM comprising 2-bit storage cells and a sequential-access driver. Four types of storage cells for 2-bit data ("00," "10," "01," "11") are adopted for reduction of the cell dimensions, whereas the sequential access is suitable for a single-chip quantum voltage waveform generator implemented with an SFQ-based digital-to-analog converter. 2-bit storage cells of 60 × 70 µm² are fabricated using a niobium integration technology and tested in liquid helium. Operation of a sequential-access mask ROM with data of 8 bits × 6 words is also demonstrated.

Keywords: Josephson effects, single-flux-quantum (SFQ), niobium integrated circuits, mask ROM

Classification: Superconducting electronics

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1 Introduction

As well as their fast switching characteristics with low power dissipation, precise voltage generation is a unique feature of superconducting single-flux-quantum (SFQ) circuits, which may realize quantum AC voltage standards [1]. There are several reports on SFQ-based digital-to-analog converters (DACs) for metrological applications [2, 3]. We developed DACs based on SFQ pulse-frequency modulation (PFM) [4], and recently, we demonstrated a 9-bit, 2.5-mVpp SFQ-PFM DAC [5].

An SFQ-based DAC synthesizes arbitrary voltage waveforms according to its digital input code. From the viewpoint of AC voltage standards, on the other hand, output voltage waveforms are often limited to sinusoidal, resulting that the digital input code can be fixed. That is, we may integrate a digital code generator on the same chip with an SFQ-based DAC. Actually, we demonstrated several single-chip voltage waveform synthesizers [6, 7, 8], where digital input codes were generated using on-chip SFQ digital circuits. Elimination of an external digital data generator and I/O cables are desirable for reduction of noise and heat flow into a cryostat.

The maximum resolution of our single-chip sinusoidal voltage waveform synthesizers was 6 bits [7]. Differently from simple waveforms such as triangle and saw-tooth, code generators for sinusoidal waveforms require rather complicated digital circuits. No scalable design of SFQ on-chip code generators has been developed for sinusoidal waveforms, whereas SFQ-PFM DACs have scalable architectures. Consequently, the resolution of single-chip SFQ sinusoidal voltage waveform synthesizers would be limited by the complexity of SFQ code generators.

Recently, we demonstrated a 6 bits × 6 words SFQ sequential-access mask ROM [9]. SFQ sequential-access mask ROMs would be alternative to SFQ on-chip code generators, because digital codes are implemented simply by placing ROM cells. On the other hand, since we employed conventional logic cells to construct the ROM cell array, it consumed a relatively large circuit area, as described later.
In this letter, we present custom-designed SFQ cells for mask ROMs, of which the area occupancy and the number of Josephson junctions (JJs) are reduced by 67% and 36% for 2-bit “11” data storage. Operation of a sequential-access mask ROM with data of 8 bits × 6 words is also demonstrated.

2 Methods

We assumed and used the 25-µA/µm² Nb/AlOₓ/Al Josephson integration process of the National Institute of Advanced Industrial Science and Technology (AIST), Japan, referred to as the AIST-STP2. The minimum dimensions and critical current of JJs were 2 × 2 µm² and 0.10 mA, respectively. Physical layouts of the ROM cells were designed with the aid of an inductance extraction program (L-meter [10]) and a circuit parameter optimization program (SCOPE2 [11]). Digital circuits other than the custom-designed ROM cells were constructed using the SFQ digital cell library referred to as the CONNECT library [12].

In measurements, test circuits were cooled at 4.2 K in liquid helium. A two-layer magnetic shield of µ-metal cans reduced the residual magnetic field on the chip.

3 2-bit SFQ ROM cells

Our first design of the “1” storage circuit comprised of 2 × 2 general cells such as a splitter, a confluence buffer, and Josephson transmission lines (JTLs), whereas that of the “0” storage included only JTL cells. Although their structures were rather simple, they respectively consumed areas of 80 × 80 µm² [9]. We then designed 2-bit ROM storage cells of 80 × 80 µm² for data “11,” “10,” “01,” and “00” as shown in Fig. 1 [13].

Since our second design, we have further reduced circuit elements and reached the cell dimensions of 60 × 70 µm². We focus on the the “11” storage cell in this section, because other storage cells for “10,” “01,” and “00” are simpler. The equivalent circuit of the “11” storage cell is shown in Fig. 2 with its CAD layout.

We have checked the bias conditions of a test circuit including a single “11” storage cell on three different chips, which are shown in Fig. 3 with numerical simulation results. Experimental bias conditions of the cells on Chip1 and Chip2 agree well with the numerical results, while those of the cell on Chip3 is shifted downward. Since the fabricated critical current density ($J_C$) on Chip3 was 75% of the nominal value, we have simulated the test circuit operation with a junction.
model having 0.75\(J_C\), of which the result is in good agreement with the experimental result.

In Table I, the custom-designed 2-bit “11” storage ROM cell is compared with that constructed using the CONNECT library [9]. The circuit area, number of JJs, and bias current are reduced by 67%, 36%, and 52%, respectively. Simple estimation for a ROM cell array of 10 bits \(\times\) 256 words, which is our target size, results in the area occupancy of 5.4 mm\(^2\) (= 0.06 \times 0.07 \times 10 \times 256/2). It is a feasible value for the present Nb integration technologies including the AIST-STP2.
8 bits × 6 words sequential-access mask ROM

After the evaluation of the 2-bit ROM cells, we have tested a prototype of an SFQ sequential-access mask ROM of 8 bits × 6 words, which is shown in Fig. 4. The ROM array, which stores 8-bit data of “11111111,” “11101111,” “10111110,” “10111011,” “10101110,” and “10101010,” is composed of “11” and “10” cells. The ROM driver is a series array of seven delay flip-flops with a feed-back loop including a 4-bit binary counter (4 toggle flip-flops). An 8-bit shift resister with an SFQ/dc converter is attached for demonstration of ROM read out operation. One clock signal source is used for both the ROM driver and the read-out shift register.

Experimental ROM read out operation with a 5 kHz-clock is shown in Fig. 5. Sequential access is successfully demonstrated, where 8-bit data are reversely retrieved in every 16 (= 2^4) clocks. We confirmed that the output waveform in Fig. 5 was repeated, and that the stop signal (“STOP”) cleared out the ROM driver. The bias margin of the ROM cell array was from −15% to +18%, while that of numerical result was from −20% to +25%.

Fig. 4. Circuit configuration and photomicrograph of a sequential-access mask ROM with data storage of 8 bits × 6 words. The ROM driver accesses 8-bit words sequentially. The clock signal “CLK” is supplied to both the ROM driver and the read-out shift resistor.

Fig. 5. Experimental result of sequential read-out operation (f_{clock} = 5 kHz). “OUT” is the output voltage of the SFQ/dc converter, where SFQ output signals are represented by voltage transitions.
5 Conclusion

An SFQ sequential-access mask ROM is a candidate of a digital data storage in a single-chip SFQ voltage waveform synthesizer. For realizing large storage capacity, we redesigned our 2-bit SFQ ROM storage cells and reduced their dimensions to $60 \times 70 \, \mu m^2$. The bias margins of the fabricated “11” storage cells were as large as the value predicted by simulation. We also designed and operated an 8 bits × 6 words 2-bit SFQ sequential-access mask ROM.

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