Reduction of Input Current Harmonics Using Dual Inverter for Motor Drive

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This paper proposes a control method to reduce the capacitance of an inverter driven motor system comprising two inverters and an open-end winding machine. In the proposed method, the inverter connected to the DC power supply switches based on the fundamental electric angular frequency of the motor. The other inverter is a pulse-width modulator controlled to generate a compensation voltage to supply a sinusoidal voltage waveform to the motor. Therefore, the carrier-frequency-order component of the input current harmonic can be reduced greatly, which helps reduce the current ripple of the filter capacitor across the DC-bus. Furthermore, this paper proposes a new control method to suppress the voltage fluctuation of the floating capacitor of the secondary-side inverter. The voltage fluctuation of the floating capacitor and hence its capacitance are reduced. The effectiveness of the proposed system is verified through experiments. The proposed control method suppresses the voltage fluctuations of the floating capacitor by 35.0% compared to the conventional driving method.

Keywords: Input current harmonics, DC-bus filter capacitor, dual inverter, open-end winding machine

1. Introduction

Recently, three-phase AC motors are being used in various applications such as automobiles, home appliances, and industrial systems (1)-(4). For in-vehicle applications, in particular, battery-powered motor drive systems are used (5)-(6). Not only motors but also various electrical components such as audio, navigation, and engine-control systems are connected to the batteries in in-vehicle systems. An input current in a voltage-source inverter (VSI) is known to be a switched current pulse from each phase leg of a three-phase pulse width modulation (PWM), and contains many high-order switching harmonics (7)-(10). The switching noise generated from the inverter used in the motor drive system is propagated to other electrical components via the DC-bus. This deteriorates the performance and reliability, and causes other electric components to malfunction (7). In addition, higher harmonic currents flow to the battery, increasing the loss and reducing the life. Therefore, in a motor drive system that uses a battery as the power source, it is necessary to reduce the input current harmonics of the inverter. To address these issues, an additional circuit is used to filter the harmonic current that flows into the DC-bus. Some parts of the filter circuit are composed of capacitors and reactors. As a large capacitance is required for the capacitor, an electrolytic capacitor is used in the filter. The capacitors absorb harmonic currents, leading to joule losses in the equivalent series resistance of the capacitors. In the case of electrolytic capacitors, heat generation due to joule loss shortens the lifetime and reduces system reliability.

Several modulation methods for VSI, which reduce the input current harmonics in motor drive systems, have been reported (11)-(18)(21). In (11)-(14), a switching pattern based on space vector PWM (SVPWM) was proposed to reduce the input current harmonics of the inverter. For the high modulation index, a vector of three adjacent voltage vectors was used, whereas two nonadjacent voltage vectors and one zero-vector was used for the low modulation index. In (15), a control method was proposed that reduced the input current harmonics by using a discontinuous PWM, assuming implementation in a general-purpose microcomputer. In these papers, the motor drive system consisted of VSIs and wye-connected motors. In (16), the reduction of the input current harmonics when the legs of each phase of the inverter were connected in parallel and driven by an interleave method was confirmed analytically and experimentally. However, in this method, as the inverter switched at a high frequency, many harmonic components still flowed in the input current.

The topology and modulation strategies of a dual inverter system consisting of two VSIs and an open-end winding machine have been researched for several purposes such as multi-level operations (17)-(21), wide speed range operations (20)-(21), and fault-tolerant functions (22)-(23). In multi-level operations, the DC-link voltage are controlled to be 2:1 for the purpose of high-efficiency driving of the motor, and a 5-level waveform is generated in the winding phase voltage (17)(19). In wide speed range operations, the inverter connected to the floating capacitor supplies reactive power to the motor. Thereby, the speed range is expanded by changing the equivalent impedance seen from the inverter connected to the power supply and increasing the active power supplied by the power supply (20). In the dual inverter system, the difference in the voltage output from each inverter is applied to the motor. By adopting this system, the degree of freedom for switching the inverter connected to the power supply was increased. In particular, in a dual inverter system equipped with a single power supply and a floating capacitor, the DC section of each inverter is independent (17)-(21)(23). Therefore, only the switching of the inverter connected to the power supply is involved in the current flowing through the DC-bus line. In (21), the inverter switches at six times the fundamental frequency of the load to reduce the harmonic content of the input current. Further, as this switching pattern did not output a zero-
vector, the utilization factor of the power supply was improved and the mechanical output of the motor was increased. However, the problem with this control method was that, when the rotation speed of the motor was low, the voltage fluctuations of the floating capacitor connected to the secondary-side inverter became large; therefore, a large capacitance was required.

This paper proposes a control method that reduces the capacitance of the floating capacitor of a dual inverter driven motor system, reducing the carrier-frequency component of the DC-bus input current. The dual inverter supplies load power from two VSIs. In the proposed control method, the inverter connected to the DC power supply switches through an 18-step operation and the inverter connected to the floating capacitor is PWM controlled for generating a compensation voltage to supply a sinusoidal voltage waveform to the motor. By applying the proposed control method, the charge/discharge amount of the floating capacitor per operation is reduced; consequently, the voltage fluctuation of the floating capacitor is reduced, and it is possible to reduce the capacitance required for compensating the load power.

This paper is organized as follows; first, descriptions of the input current of the three-phase VSI and basic configuration of the dual inverter system are introduced. Next, the control method for the dual inverter system and the design method for the capacitance of the floating capacitor are introduced. Finally, the experimental and analytical results are shown.

2. Dual Inverter Driven Motor System

2.1 DC-bus Input Current Harmonics

Fig. 1 shows a motor drive system that uses a conventional single inverter equipped with a filter circuit across a DC-bus. In this system, the inverter whose power supply is connected to the input section performs PWM to supply arbitrary power to the load. The instantaneous value of the inverter input current \( i_{dc} \) is a superpositioned summation of the switched current pulses from each phase leg, and is calculated as follows (6).

\[
i_{dc} = \sum_{x=u,v,w} (i_x \cdot SW_x), \quad \text{...........................................(1)}
\]

where \( SW_x \) is 1 when the upper arm \( SW_{up} \) of each phase leg is ON and 0 when the lower arm \( SW_{dn} \) is ON. The motor drive system must operate at a variable speed. In the single inverter system, the VSI performs PWM control; therefore, the input current is a chopped phase current waveform, as can be seen from Eq. (1). Therefore, the input current of the inverter contains many carrier-frequency components resulting from the instantaneous changes.

2.2 Dual Inverter System

Fig. 2 shows a motor drive system that uses a dual-inverter system. In this system, two VSIs drive the motor with open-end winding. One VSI (Inv.1) is connected to the DC power supply and the other VSI (Inv.2) is connected to the floating capacitor \( C_{dc2} \). As the power to Inv.2 is supplied for \( C_{dc2} \), the system does not require an additional DC power supply. The voltage of \( C_{dc2} \) changes as the capacitor is charged and discharged. Therefore, the dual inverter system that uses floating capacitors requires control that considers the charging and discharging of the capacitors.

In the dual inverter system, the voltage applied to the load is the difference between the output voltages of Inv.1 \( (v_u-v_w) \) and Inv.2 \( (v_{u2}-v_{w2}) \). The voltage \( (v_u-v_w) \) applied to the load is given by

\[
v_z = v_{z1} - v_{z2}, \quad (z=u, v, w). \quad \text{...........................................(2)}
\]

Table 1. Inv.1 output vector and switching state in six-step drive.

| Phase command | Output vector (Sector) | Switching state |
|---------------|------------------------|-----------------|
| -n/6 < f < n/6 | V_1 (1) | on off off on off on |
| n/6 < f < n/2 | V_2 (2) | on on off off off off |
| n/2 < f < 5n/6 | V_3 (3) | off on off off on off |
| 5n/6 < f < 5n/8 | V_4 (4) | off on off on on off |
| 5n/8 < f < 7n/8 | V_5 (5) | off on off on off on |
| 7n/8 < f < 11/6 | V_6 (6) | off off off on off on |
| - | V_7 | off on off off on off |
| - | V_8 | off on off off on off |

Fig. 1. Motor drive system using the single inverter with filter circuit.

Fig. 2. Motor drive system using the dual inverter.

Fig. 3. Output voltage vector of dual/inverter system.
3. Proposed Control Method

3.1 Input Current Harmonic Reduction Control Method

In the motor drive system that uses a single inverter as shown in Fig. 1, the motor power is supplied from the PWM inverter, which is connected to the dc power supply. Therefore, the dc input current of the inverter contains several carrier-frequency components. However, in the motor drive system using the dual inverters, shown in Fig. 2, the difference in the output voltages of each inverter is applied to the load. Therefore, a driving method is possible in which Inv.1 outputs only the active vector at a switching frequency that is six times the fundamental frequency of the load (six-step drive), and Inv.2 performs PWM at the carrier-frequency to compensate the load power (21). With this driving method, the inductance component of the motor can act as a filter, and the harmonic current of the carrier-frequency component generated from Inv.2 is filtered. Therefore, the carrier-frequency component of the input current can be reduced significantly. In addition, the angle of the phase current that appears in \( i_d \) changes due to the influence of the load power factor. On the other hand, current harmonics on the order of kHz are filtered by the inductance component of the motor. Therefore, the effect of reducing the harmonics of \( i_d \) in the proposed method is maintained without depending on the change in the load power factor due to the motor control method.

Table 1 shows the output voltage vector and switching states with respect to the phase command \( \theta \) of the output voltage of Inv.1 when performing six-step operation. As the output voltage vector of Inv.1, the vector of the phase closest to \( \theta \) is selected, and this is switched every \( \pi/3 \) phase shift. In the six-step operation, Inv.1 does not use the zero-vector, and thus, the fundamental frequency component of the voltage applied to the load is \( 4/\pi \) for sinusoidal PWM (SPWM) and \( 2\sqrt{3}/\pi \) for SVPWM. Therefore, the output range of the motor can be expanded.

When Inv.1 performs the six-step operation, the output voltage of Inv.1 contains low-order harmonic components, as shown in \( V_{dc2} \) of Fig. 2. In order to supply a sinusoidal voltage waveform \( V_{load} \) to the motor, \( V_{dc2} \) in Inv.2, compensates for the deviation of the output voltage vector of \( V_{inv.1} \) from the sinusoidal waveform as shown in Fig. 3.

3.2 Proposed Control Method to Reduce Capacitance

The capacitance of \( C_{dc2} \) is described by the compensation power of Inv.2 \( W_{inv.2} \) and the upper limit \( V_{dc2 \_max} \) and lower limit \( V_{dc2 \_min} \) of \( V_{dc2} \) as follows:

\[
C_{dc2} = \frac{2W_{inv.2}}{V_{dc2 \_max}^2 - V_{dc2 \_min}^2} \quad (3)
\]

It is assumed that there is no loss in Inv.2 and \( C_{dc2} \). Fig. 4 shows the relationship between the output voltage \( V_{dc1} - V_{dc2} \) of Inv.1 and charging or discharging of \( C_{dc2} (V_{dc1} - V_{dc2}) \). The charging and discharging cycles of \( C_{dc2} \) in the six-step driving are equal to the switching cycles of Inv.1. Inv.1, in this case, outputs only the active vector. When the fundamental frequency of the load decreases, such as when the motor operates at a low rotation speed, the charging and discharging cycles of \( C_{dc2} \) become longer. Therefore, the charging and discharging power per charge increases, resulting in large fluctuations in \( V_{dc2} \). As these voltage fluctuations must be within a certain limit, a large capacitance is required.

In order to reduce the required electrostatic capacitance when considering the operation at low rotation speeds, this paper proposes inserting the zero-vector as the switching pattern in Inv.1, which is called the 18-step operation. The proposed zero-vector is inserted during the time when \( C_{dc2} \) is being charged during the six-step operation. There are two patterns of switching states that output a zero-vector (\( V_6 \) or \( V_7 \)). The vector with the smallest change in switching state is selected according to the active-vector being output. \( V_6 \) is selected when \( V_4 \) is output, and \( V_7 \) is selected when \( V_5 \) is output. In the 18-step operation, the charge and discharge power per operation is reduced, when compared to that in the six-step operation; thus, the fluctuations in \( V_{dc2} \) are suppressed. Therefore, the capacity of \( C_{dc2} \) can be reduced.

In the 18-step operation, the switching frequency of Inv.1 is triple that of the six-step drive. This increase in switching frequency may affect the harmonic components of the input current. Therefore, the six-step drive is used during high-speed operation where \( V_{dc2} \) fluctuations are relatively small, and the 18-step operation is used during low-speed operations where the \( V_{dc2} \) fluctuations are large. In this way, it is desirable to switch the control method according to the rotation speed of the motor.

3.3 Floating Capacitor Voltage Control Method

The voltage of \( C_{dc2} \), which changes the power supply of Inv.2, must be kept higher than the power supply voltage. This is because Inv.2 must compensate for the load power in all operating areas. Therefore, it is necessary to control the voltage of \( C_{dc2} \). Fig. 5 shows the block diagram for controlling that voltage. In order to keep the average of \( V_{dc2} \) constant, it is necessary to equalize the average value of the voltage applied to the motor and the voltage output from Inv.1. Therefore, in the region where the modulation index is 1 or less, a shift amount of \( \theta_{iff} \) is applied to the phase \( \theta_{inv.1} \) of the output voltage of Inv.1, with respect to the phase reference \( \theta_{ref} \) of the motor current.
\[ \theta_{\text{inv.1}} = \theta_{\text{ref}} + \theta_{\text{shift}} \] ................................. (4)

The amount of phase shift is given by the following equation:
\[ \theta_{\text{shift}} = \cos^{-1}\left( \frac{V_{\text{load}}}{V_{\text{act. max}}} \right) \] ................................. (5)

where \( \theta_{\text{shift}} \) is in the range of \(-\pi/2 < \theta_{\text{shift}} < \pi/2\) and the motor cannot be driven in any other range. In addition, the calculated result has a deviation due to a nonlinear element, and is thus compensated by proportional integral (PI) control. When switching the operation mode between six-step operation and 18-step operation, the integral term of the PI controller is reset to zero to prevent large fluctuations in \( V_{\text{dc2}} \) due to the difference in the compensation amount after switching. \( V_{\text{load}} \) is the magnitude of the load voltage vector and is expressed as follows:
\[ V_{\text{load}} = \sqrt{V_{a}^{2} + V_{b}^{2}} \] ................................. (6)

where \( V_{\text{act. max}} \) is the average of Inv.1 output voltage under the condition of \( \theta_{\text{shift}} = 0 \) radians and is expressed as
\[ V_{\text{act. max}} = \frac{2}{\pi} V_{\text{dc1}} \left( 1 - \frac{6 \theta_{\text{zero}}}{2\pi} \right) \] ................................. (7)

where \( V_{\text{dc1}} \) is the supply voltage and \( \theta_{\text{zero}} \) is the zero-vector output angle per sector.

The power factor of the motor changes depending on the driving state of the motor, such as changes in load torque and field weakening. The change in power factor affects the current flowing through \( C_{\text{dc2}} \) and appears as a deviation of \( \theta_{\text{shift}} \). The deviation is corrected by the PI controller. Therefore, it is possible to operate in response to changes in the power factor.

### 3.4 Determination Method of Capacitance and Voltage of Floating Capacitor

The power \( W_{\text{dc2}} \) compensated by the floating capacitor connected to the secondary-side inverter is given by
\[ W_{\text{dc2}} = \frac{V_{\text{dc1}} I_{\text{load}} S_{\text{dc2}}}{\omega_{\text{load}}} \] ................................. (8)

where \( I_{\text{load}} \) is the phase current peak, \( \omega_{\text{load}} \) is the fundamental angular frequency of the load, and \( S_{\text{dc2}} \) is the compensation area of \( C_{\text{dc2}} \). Assuming that the circuit loss of Inv.2 does not occur, \( W_{\text{dc2}} = W_{\text{dc1}} \). From Eq. (3) and Eq. (8), the \( C_{\text{dc2}} \) required to suppress the load pulsation power is written as follows:
\[ C_{\text{dc2}} = \frac{2 V_{\text{dc1}} I_{\text{load}} S_{\text{dc2}}}{\omega_{\text{load}} (V_{\text{dc2}, \text{max}} - V_{\text{dc2}, \text{min}})} \] ................................. (9)

From Eq. (9), the floating capacitor \( C_{\text{dc2}} \) is determined by the acceptable voltage ripple and compensating load power. The maximum value of voltage ripple \( V_{\text{dc2}, \text{max}} \) is limited by the breakdown voltage of the device used in Inv.2. The minimum value of Inv.2 input voltage that enables the system to compensate for the load voltage is given as follows:
\[ V_{\text{dc2}, \text{min}} = \begin{cases} \frac{4}{\pi} V_{\text{dc1}} & \text{(driven by SPWM)} \\ 2 \sqrt{3} \frac{V_{\text{dc1}}}{\pi} & \text{(driven by SVPWM)} \end{cases} \] ................................. (10)

Fig. 6 (a) shows the relationship between the output vector locus of Inv.1 and \( S_{\text{dc2}} \) during six-step operation. \( S_{\text{dc2}} \) when Inv.1 performs six-step operation is expressed as
\[ S_{\text{dc2}} = S_{\text{dc1}} = S_{\text{db1}} \] ................................. (11)

where \( C_{\text{dc2}} \) is charged by \( S_{\text{dc2}} \), discharged by \( S_{\text{db1}} \), and \( S_{\text{dc2}} \) is controlled to be constant, so that their areas are equal. \( \theta_{\text{h}} \) is the phase angle at which charging and discharging switch, and is given by
\[ \theta_{\text{h}} = \tan^{-1} \left( \frac{\sin \theta_{\text{h}}}{\cos \theta_{\text{h}}} + 1 \right) \] ................................. (12)

The threshold is expressed by Eq. (13) and Eq. (14) from the average \( V_{\text{inv.1, ave}} \) of the Inv.1 output vector.
\[ \theta_{\text{h}} = \cos^{-1} \left( \frac{2 V_{\text{inv.1, ave}}}{V_{\text{dc1}}} - 1 \right) \] ................................. (13)
\[ V_{\text{inv.1, ave}} = \sqrt{6 S_{\text{inv.1}}} \] ................................. (14)

The Inv.1 output fluctuates periodically at sixfold fundamental frequency such that \( S_{\text{inv.1}} \) can be obtained by integrating the section from angle \( \theta_{1} \) to \( \theta_{2} \) during when the output vector of Inv.1 switches.
\[ S_{\text{inv.1}} = \int_{0}^{2\pi} r dr \theta \] ................................. (15)

\[ D = (r(\theta) \theta_{1} \leq \theta \leq \cos \theta_{1}, \theta_{2} \leq \theta \leq \theta_{2}) \] ................................. (16)

\[ \theta_{1} = -\frac{\pi}{6} + \theta_{\text{shift}} \] ................................. (17)
\[ \theta_{2} = \frac{\pi}{6} + \theta_{\text{shift}} \] ................................. (18)

\( S_{\text{dc2}} \) and \( S_{\text{db1}} \) in the six-step operation are calculated as in Eq. (17) and Eq. (18) under the condition \(-\theta_{\text{dc1}} < 0\) where the area of \( S_{\text{dc1}} \) is symmetric with respect to 0 radians.
\[ S_{\text{dc1}} = 2 \int_{0}^{\theta_{\text{dc1}}} V_{\text{inv.1, ave}} dr \] ................................. (19)
\[ D_{\text{dc1}} = (r(\theta) \theta_{1} \leq \theta \leq \cos \theta_{1}, 0 \leq \theta \leq \theta_{\text{dc1}}) \] ................................. (20)
\[ S_{\text{db1}} = 2 \int_{-\theta_{\text{db1}}}^{-\theta_{\text{dc1}}} V_{\text{inv.1, ave}} dr \] ................................. (21)
\[ D_{\text{db1}} = (r(\theta) \theta_{1} \leq \theta \leq \cos \theta_{1}, 0 \leq \theta \leq \theta_{\text{db1}}) \] ................................. (22)
Under other conditions, they are calculated as follows:

\[
S_{BA} = \int_{D_a} \int_{D_b} r \, d\theta_0 \left( \frac{1}{2} \right) \tan^{-1} \left( \frac{1}{2} \right) \rho_{\theta a}^2 \theta_{\text{inv.1}, \text{ave}} \, d\theta_0, \quad \text{......... (19)}
\]

\[
D_A = [(r,0)0 \leq r < \cos \phi, \theta_1 \leq \theta_0 < \theta_2]
\]

\[
S_{AB} = \frac{1}{2} \int_{D_b} \int_{D_b} r^2 \rho_{\theta a}^2 \theta_{\text{inv.1}, \text{ave}} \, d\theta_0, \quad \text{......... (20)}
\]

\[
D_B = [(r,0)0 \leq r < \cos \phi, \theta_0 \leq \theta_2]
\]

Fig. 6 (b) shows the relationship between the output vector locus of Inv.1 and Inv.2 during 18-step operation. The correction amount of \( S_{BA} \) in this case is given by the Eq. (21) when the maximum value of \( S_{BA} \) to \( S_{BA} \) is \( S_{BA} \).

\[
S_{BA} = S_{BA, \text{max}} \quad \text{......... (21)}
\]

\( S_{BA} \) and \( S_{BA} \) are the charging periods of \( S_{BA} \), and \( S_{BA} \) and \( S_{BA} \) are the discharging periods. The phase angle at which charging and discharging are switched is given by the Eq. (12), as in the case of the six-step drive. Then, \( S_{BA} \) is given as

\[
S_{BA} = \int_{D_a} \int_{D_b} r \, d\theta_0 - \int_{D_b} \int_{D_b} r \, d\theta_0, \quad \text{......... (22)}
\]

\[
D_A = [(r,0)0 \leq r < \cos \phi, \theta_1 \leq \theta_0 < \theta_2]
\]

\[
D_A = [(r,0)0 \leq r < \cos \phi, \theta_0 \leq \theta_2]
\]

where \( \theta_{\text{inv.1}} \) and \( \theta_{\text{inv.2}} \) are the beginning and end of the phase angle at which Inv.1 outputs the zero-vector. \( S_{BA} \) to \( S_{BA} \) for the 18-step operation are expressed as follows:

\[
S_{BA} = \int_{D_a} \int_{D_b} r \, d\theta_0 - \frac{1}{2} \left( \frac{1}{2} \right) \theta_{\text{inv.1}, \text{ave}} \, d\theta_0, \quad \text{......... (23)}
\]

\[
D_A = [(r,0)0 \leq r < \cos \phi, \theta_1 \leq \theta_0 < \theta_{\text{zero}}]
\]

\[
S_{BA} = \frac{1}{2} \int_{D_b} \int_{D_b} \rho_{\theta a}^2 \theta_{\text{inv.1}, \text{ave}} \, d\theta_0 \quad \text{......... (24)}
\]

\[
S_{BA} = \int_{D_b} \int_{D_b} r \, d\theta_0 - \frac{1}{2} \left( \frac{1}{2} \right) \theta_{\text{inv.1}, \text{ave}} \, d\theta_0, \quad \text{......... (25)}
\]

\[
D_A = [(r,0)0 \leq r < \cos \phi, \theta_{\text{zero}} \leq \theta_0]
\]

Table 2. System and Motor Parameters.

| Description                  | Symbol | Parameter |
|------------------------------|--------|-----------|
| Power supply voltage         | \( V_{dc1} \) | 13V       |
| Voltage reference of floating capacitor | \( V_{dc2}^* \) | 30V       |
| Floating capacitor           | \( C_{dc2} \) | 165pF     |
| Carrier-frequency            | \( f_{sw} \) | 10kHz     |
| Proportional gain and integral gain of voltage control | \( K_{d}, K_{ref}, K_{vdc2} \) | 0.3, 3.0 |
| Stator resistance            | \( R_s \) | 16.2mΩ    |
| dq-axis inductance           | \( L_d, L_s \) | 92.3μH    |
| Linkage flux                 | \( a \) | 8.91mWb   |
| Number of pulse pairs        | \( P_s \) | 5         |
| Rated torque                 | \( T \) | 11.1Nm    |
| Switching device of Inv.1    | FDP8860 |
| Switching device of Inv.2    | 2SK2753 |
| Floating capacitor           | B32526F11336K000 (5 parallel) |

\[
S_{BA} = \frac{1}{2} \int_{D_b} \int_{D_b} \rho_{\theta a}^2 \theta_{\text{inv.1}, \text{ave}} \, d\theta_0 \quad \text{......... (26)}
\]

\[
D_A = [(r,0)0 \leq r < \cos \phi, \theta_0 \leq \theta_2]
\]

3.5 Proposed Control Block Diagram Fig. 7 shows the proposed control block diagram based on the dc input current harmonic reduction control method, the driving method to reduce capacitance, and the input capacitor voltage control method of the floating inverter. The proposed control method assumes an open-ended surface permanent magnet synchronous motor (SPMSM) load. Inv.1 uses the switching table (shown as Table 1) to generate the gate signal from the phase reference value described in Subsection 3.3. The insertion position of the zero-vector during 18-step operation is provided for \( \pm \theta_{\text{inv.2}} \), based on the central angle \( \theta_{\text{zero}, \text{ctr}} \) of the zero-vector. It is also output at the same time for each sector. The voltage reference value of Inv.2 is calculated based on Eq. (2), from the output value of the PI controller of the current on the \( dq \)-axes and the output voltage of Inv.1 reproduced in the DSP. The output voltage of Inv.1 reproduced in the DSP is calculated from \( V_{dc1} \) and \( \theta_{\text{inv.1}} \) in the same way as used in the Inv.1 switching table. The gate signal of Inv.2 is generated by SPWM from the voltage reference value obtained using the above method.

4. Experimental Result

The effectiveness of the proposed control method was confirmed.
Motor Drive System for Reducing Input Current Harmonics (Ren Okumura et al.)

Fig. 8. Steady-state waveform of experimental results in dual inverter system at 1000rpm and 1.1Nm; u-phase load voltage, u-phase load current, Inv.1 input current and floating capacitor voltage.

by experiments using an open-winding machine as a load. In the experiments, a three-phase SPMSM was used as the tested motor. The tested motor was driven with a constant torque. The constant rotational speed was obtained by using a load motor connected to a single VSI. The proposed control method was implemented with a Texas Instruments TM320 floating-point digital signal processor. The experimental waveform was observed by DL850E. The system and motor parameters are listed in Table 2. The proposed system is intended for motor drive systems used where multiple electrical loads are connected to a single power source. Therefore, assuming a motor drive system used for radiator fans of in-vehicle auxiliary equipment and power steering, tests are conducted with this power supply voltage. The proportional gain $K_{p, V_{dc2}}$ and integral gain $K_{i, V_{dc2}}$ of the floating capacitor voltage control were designed by trial and error based on the simulation results. The insertion position of the zero vector in the case of 18-step operation in this experiment is $\theta_{zvec,cr} = 345$ degrees, taking sector 1 as an example. The other sectors, the zero vector output period is provided as in the case of sector 1.

4.1 Floating Capacitor Voltage Control and Voltage Fluctuation Suppression Effect

Fig. 8 shows the steady-state waveform of the experimental results in the dual inverter system shown in Fig. 2. Fig. 2 (a) shows the experimental waveform when operated under the control method of six-step operation. Fig. 2 (b) shows the experimental waveform when operated using the proposed control method of 18-step operation. Both control methods control the average voltage of the floating capacitor at 30V. In addition, the DC input current of Inv.1 depends on the fundamental frequency of the load, and a chopped load current is produced. In the six-step operation, the capacitor is charged and discharged once in each cycle (for each sector). The fluctuation of $V_{dc2}$ in this case is 22.5V to 34.5V. In the proposed 18-step operation, the capacitor is charged and discharged twice in each cycle (for each sector). The fluctuation of $V_{dc2}$ is 26.2V to 34.0V. By using the proposed control method, the variation of $V_{dc2}$ is suppressed by 35.0% under this experimental condition.

Fig. 9 shows the experimental waveforms when switching the operation mode between six-step operation and 18-step operation. Fig. 9 (a) is the experimental waveform obtained when switching from the six-step operation to the 18-step operation. Fig. 9 (b) is the experimental waveform obtained when switching from the 18-step operation to the six-step operation. In Fig. 9 (a), $V_{dc2}$ drops by several units after the switching. This occurs because there is a deviation due to the nonlinear component in $\delta_{Zvec}$ during the 18-step

6 IEEJ Trans.
operation after switching. However, as the voltage is not lower than $V_{dc,\text{min}}$, it does not affect the compensation of the load power by Inv.2; thus, there is no problem. It also does not affect the motor output torque. Similarly, in Fig. 9 (b), the mechanical output is not affected.

4.2 Capacitance Reduction Effect of the Floating Capacitor
Fig. 10 shows the capacitance reduction rate of the floating capacitor when 18-step operation is applied, compared to that under six-step operation. Under the same operating conditions as in Fig. 8, the rotation speed is changed between 600rpm and 1300rpm. The rate of capacitance reduction in the experimental results is calculated from Eq. (3) by measuring the variation of $V_{dc}$ when the same capacitor is used. Then, this is the same as the comparison when the capacitance is determined so that the voltage fluctuations are the same. Under the operating conditions, the maximum point of the capacitance reduction effect is approximately 1100rpm in the calculation results and 1000rpm in the experimental results. The reduction effect depends on $\theta_{dc0}$ when the insertion position of the zero-vector is constant. The calculated $\theta_{dc0}$ is larger than that in the experiment because the voltage drops in the devices other than the motor is not considered. This difference corresponds to a back electromotive force of approximately 100rpm. Therefore, such a difference occurs. As can be seen from each result, the effect of reducing the electrostatic capacitance by the 18-step operation is clear. It is possible to obtain a further reduction effect by selecting the insertion position of the zero-vector appropriately, according to the driving condition.

4.3 Inv.1 Input Current Harmonics
Fig. 11 shows the results of the harmonic analysis of the Inv.1 input current in the conventional single inverter system driven by SPWM and dual inverter system driven by the six-step and proposed 18-step methods. The carrier-frequency in the experiment was 10kHz, and the results of the harmonic analysis show the integer-order component of the carrier-frequency. The harmonic components of the input current are normalized by the fundamental component of the phase current. In the single inverter system, the inverter connected to the power supply is driven by SPWM. Therefore, the input current contains many carrier-frequency components. In the dual inverter system, Inv.2 is driven by the SPWM at the carrier-frequency; however, its switching harmonics are filtered by the motor inductance component. Therefore, the harmonics of the carrier-frequency component are reduced to approximately 1/10 in the dual inverter system, when compared to that in the single inverter system. When comparing the six-step operation and the proposed 18-step operation, the harmonic components tend to increase when the 18-step operation is used. This is because the switching frequency of Inv.1 connected to the power supply is tripled. However, the application of the 18-step operation is at low rotation speeds where $V_{dc}$ fluctuation is large and the switching frequency is low; therefore, so the effect is sufficiently small.

4.4 Capacitor Current Stress
Fig. 12 shows the measurement results of the filter-capacitor $C_{dc}$ current $i_{dc}$ and the $C_{dc2}$ current $i_{dc2}$. The current stress of the capacitor has been experimentally verified by a system equipped with an LC-filter on the DC-bus line as shown in Fig. 1. The filter-inductor $L_{dc}$ is 0.47H, the $C_{dc}$ is 2200μF, and the load conditions are the same as in subsection 4.1. Each drive method controlled at $V_{dc2} = 30V$ in the dual inverter system has an increased total current than the single inverter system. However, the lifetime of the capacitor is greatly affected by heated by joule loss. Fig. 13 shows the joule loss of the capacitor. The joule loss assumes that the equivalent series resistances of $C_{dc}$ and $C_{dc2}$ are equal for comparison. In addition, each value is normalized by the joule loss in the single inverter system. In the dual inverter system, the joule loss of the capacitor can be reduced as compared with the single inverter system. In addition, by controlling $V_{dc2}$ higher, the modulation index of Inv.2 decreases. Therefore, the current effective value of $i_{dc2}$ decreases, and it is possible to further reduce the joule loss of the capacitor.
5. Conclusions

This paper proposed a control method that reduced the capacitance of the floating capacitor in the dual inverter system that reduced the input current harmonics of the inverter connected to the DC power supply. The proposed system consisted of two inverters and an open-end winding machine. In the proposed modulation method, the inverter connected to the power supply did not perform PWM. Therefore, it contributed to the reduction of the current ripple of the filter capacitor. The proposed control method could suppress the fluctuations in the voltage of the floating capacitor, and was particularly effective in the low-speed rotation region where the fluctuations increased. The effectiveness of the proposed system was demonstrated by experimental results with an open-end winding SPMMSM load. Under this condition, the voltage fluctuation of the floating capacitor was suppressed by 35.0%, when compared to that during six-step operation. In addition, switching of operation modes was achieved without affecting the mechanical output. It was also, the proposed control method could reduce the input current harmonics significantly, when compared to the conventional single inverter system. Therefore, it was confirmed that the current stress of the capacitor in the entire system can be reduced.

From these results, this paper confirmed the effectiveness of the motor drive system that used the dual inverter and the proposed control method to reduce the electrostatic capacitance of the floating capacitor.

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