**PyTorch-Direct: Enabling GPU Centric Data Access for Very Large Graph Neural Network Training with Irregular Accesses**

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**Abstract**

With the increasing adoption of graph neural networks (GNNs) in the machine learning community, GPUs have become an essential tool to accelerate GNN training. However, training GNNs on very large graphs that do not fit in GPU memory is still a challenging task. Unlike conventional neural networks, mini-batching input samples in GNNs requires complicated tasks such as traversing neighboring nodes and gathering their feature values. While this process accounts for a significant portion of the training time, we find existing GNN implementations using popular deep neural network (DNN) libraries such as PyTorch are limited to a CPU-centric approach for the entire data preparation step. This "all-in-CPU" approach has negative impact on the overall GNN training performance as it over-utilizes CPU resources and hinders GPU acceleration of GNN training. To overcome such limitations, we introduce PyTorch-Direct, which enables a GPU-centric data accessing paradigm for GNN training. In PyTorch-Direct, GPUs are capable of efficiently accessing complicated data structures in host memory directly without CPU intervention. Our microbenchmark and end-to-end GNN training results show that PyTorch-Direct reduces data transfer time by 47.1% on average and speeds up GNN training by up to 1.6×. Furthermore, by reducing CPU utilization, PyTorch-Direct also saves system power by 12.4% to 17.5% during training. To minimize programmer effort, we introduce a new "unified tensor" type along with necessary changes to the PyTorch memory allocator, dispatch logic, and placement rules. As a result, users need to change at most two lines of their PyTorch GNN training code for each tensor object to take advantage of PyTorch-Direct.

1 **Introduction**

Graphs are widely used to represent relational information between different entities. Many real-world applications such as social networks, e-commerce, and logistics networks use graphs to track the relationship between human to human, human to product, location to location, and so on. To take full advantage of this relational information, there has been increasing interest in adopting graph neural networks (GNNs) to enable various kinds of analysis such as node classification, link prediction, and graph property prediction (Hu et al., 2020a) on graph-based databases.

In Figure 1 (a), we show a simple example of GNN training. To generate the embedding of node 4, we traverse the input graph and gather information (features) of neighboring nodes 2, 4, 7, 9, and 25. The gathered features go through a GNN architecture dependent aggregator to generate a state. In this case, we assume node 4 is a root node, and the state generated by the first layer of aggregation is the final state, which is also a node embedding. This process can be done multiple times recursively to look up further nodes.

With the advent of GNNs, there have been several efforts to provide generalized GNN training frameworks (Data61, 2018; Grattarola & Alippi, 2020; Wang et al., 2019; Fey &

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**Figure 1:** (a) A simple example showing feature aggregation in GNN training. (b) An example of node features in memory. The nodes might be close to each other in the graph, their features are not necessarily in memory.
However, directly applying the DNN libraries for GNN training also introduces a new kind of performance challenge due to their CPU-centric way of transferring data between CPU and GPU. Unlike training classical neural networks such as convolutional neural networks (CNNs), a single forward propagation of GNNs requires reading hundreds or even thousands of separate samples (node features) depending on the input graph topology and the number of GNN layers. Accessing the features of neighboring nodes in graphs is not as simple, i.e. not as structured, as accessing the neighboring pixel values in images. Due to the way graph structures are stored in memory, features that the training algorithm accesses in order to process the output for a given node are likely scattered in memory, as depicted in Figure 1(b).

Now, the main challenge arises when we attempt to accelerate GNN training by using GPUs. Similar to training other DNNs, GNN training also requires a huge number of arithmetic operations while aggregating the features, which makes the usage of GPUs attractive. Unfortunately, transferring the scattered data to the GPUs with the existing DNN libraries is not straightforward. Initiating a direct memory access (DMA) call on each data fragment is too expensive and therefore the scattered data needs to be first gathered by the CPUs before the transfer. For small graphs, this inefficiency can be bypassed by simply loading the whole features into GPU memory, but real world graphs can go beyond billions of nodes (Ying et al., 2018) and thus far exceed GPU memory capacity.

In GNN training, the gather operation is not the only workload for CPUs. CPUs need to generate subgraphs for each mini-batch and constantly traverse input graphs to identify neighboring nodes. The number of these graph structure related operations and the portion of total training time they consume is non-trivial (44%-99%) (Liu et al., 2020). While CPU resources are already overloaded, it is impractical to further burden CPUs with data transfer operations.

Conventional wisdom would argue that since the graph feature data is in host memory, the CPU should have significant latency and bandwidth advantage over GPUs in performing the gather operations on these features. However, GPUs with their ability to issue a massive number of concurrent memory accesses to tolerate latency, have been recently shown to be effective in accessing data with irregular structures like graphs that reside in the host memory (Min et al., 2020). If successful, having the GPUs perform gather operations also eliminates the need to perform a data copy from the CPU to the GPU after the feature data has been gathered. It is therefore desirable to explore the use of GPUs to perform feature gather accesses to significantly reduce end-to-end GNN training time. In this work, we present PyTorch-Direct, a GPU-centric data access design for GNN training.

PyTorch-Direct presents a new class of tensor called “unified tensor.” While a unified tensor resides in host memory, its elements can be accessed directly by the GPUs, as if they reside in GPU memory. To support seamless transition of applications from the original PyTorch to PyTorch-Direct, we design the programming interface for using unified tensors to be consistent with the existing PyTorch GPU tensor declaration mechanism. Users can take full advantage of PyTorch-Direct, by merely modifying 2 lines of their PyTorch GNN implementation.

PyTorch-Direct also includes an important memory access alignment optimization for direct host memory access over PCIe. Without the aligned memory accesses, direct access over PCIe could suffer performance drop of nearly 44%. To prevent this, we implement a circular shift stage in PyTorch GPU indexing function which automatically calculates the offset values required to enforce alignment and generate adjusted indices. The adjustment algorithm is entirely implemented in the PyTorch backend CUDA code and general users do not need to do anything special in their code to take advantage of it.

With PyTorch-Direct, the time spent for accessing irregular data structures in host memory is reduced on average by 47.1% compared to the baseline PyTorch approach. In real GNN training, we show PyTorch-Direct can speedup end-to-end GNN training by up to 1.62× depending on GNN architecture and input graph. Furthermore, by reducing the CPU workload, PyTorch-Direct provides 12.4% to 17.5% of reduced system power consumption during GNN training.

We designed PyTorch-Direct targeting high performance, portability, and ease of use. The main contributions of this paper are summarized as follows:

- We identify inefficient host to GPU data transfer patterns in existing GNN training schemes that cause high CPU utilization and increase end-to-end training time.

- We propose a GPU-centric data access paradigm with a novel circular shift indexing optimization for GNN training to reduce training time, CPU utilization, and power consumption.

- We incorporate the proposed system level changes seamlessly into a popular DNN library, PyTorch, with a comprehensive implementation to benefit a broad range of GNN architectures.
2 BACKGROUND AND RELATED WORK

2.1 Graph Neural Networks

Graph neural network (GNN) is a type of neural network that works on graph data. Unlike the conventional neural networks, GNNs can retain the relational information between entities represented by the graph nodes. A common example of GNN application is a recommender system in social networks (Hamilton et al., 2017; Ying et al., 2018; Kipf & Welling, 2017). GNNs are largely composed of two types of components: aggregators and updaters (Zhou et al., 2018). Aggregators gather features from each node’s neighbors and updaters update nodes’ hidden states. Together, the process of outputting a state embedding $h_v$ of an arbitrary node $v$ can be expressed as follows:

$$h_v = f(x_v, x_{co[v]}, x_{ne[v]}, h_{ne[v]})$$ (1)

Here, $f$ is a parametric function, $x_v$, $x_{co[v]}$, and $x_{ne[v]}$ are the input features of the node $v$, edges connected to the node $v$, and neighboring nodes of node $v$, respectively, whereas $h_{ne[v]}$ represents the states of neighboring nodes of node $v$. This process can be done recursively in a bottom-up tree traversal manner to aggregate features and states of nodes several hops away. The final output embeddings can be used for many downstream tasks, such as node classification.

2.2 GPU Out-of-memory Solution for GNN Training

In GNN training, the input features are located in a 2D array where the row indices are the IDs of nodes and the columns are the features of each node. In Figure 1, we show a case of retrieving the node features of the neighboring nodes during the GNN training. Due to the structural discrepancy between the graph and the array, accessing the features of neighboring nodes in the graph results in accessing rather unpredictable and non-sequential rows of the Feature Array.

A straightforward approach to sending these non-consecutive rows to the GPU is to call data copying functions like cudaMemcpy() multiple times, once for each row. Unfortunately, making multiple calls to data copying functions incurs significant overhead and can be highly inefficient. When the input graphs are small, one can bypass this issue by simply placing the entire feature array into the GPU memory at the beginning of GNN training. However, in reality, it is not reasonable to assume the the entire feature array can always fit into the GPU memory.

Currently, the solutions for training GNNs on very large graphs can be largely divided into two categories: 1) Only the immediately necessary features for the current mini-batch are gathered by the CPU, and then sent to the GPU memory (Ying et al., 2018). 2) Before training, partition the input graphs into multiple smaller subgraphs that can be fit into the GPU memory, and then train on them one by one (Chiang et al., 2019; Zeng et al., 2020). In the former category, the CPU can become a bottleneck and slows down the training pipeline. In the latter category, the subgraphs inevitably lose some of the distinct structural patterns of the original graphs (Wu et al., 2020). Pytorch-Direct addresses these deficiencies by enabling the GPU to directly gather all the needed features from the host memory on demand.

2.3 GNN Frameworks with Python DNN Libraries

To simplify GNN development, there are several efforts to combine some of the commonly required functionalities in GNN trainings and create a framework using popular Python-based DNN libraries such as PyTorch and TensorFlow. Deep graph library (DGL) (Wang et al., 2019) is developed based on MXNet, PyTorch, and TensorFlow. PyTorch-Geometric (Fey & Lenssen, 2019) is a PyTorch-based GNN framework. StellarGraph (Data61, 2018) and Spektral (Grattarola & Alippi, 2020) are based on TensorFlow and Keras API. In this work, we demonstrate the benefit of our approach by extending PyTorch.

3 MOTIVATION

In current implementations of deep learning frameworks, host to GPU data loading process is implemented in a CPU-centric manner. When data that needs to be processed by the GPU is scattered in host memory, it is the CPU’s respon-
sibility to gather the data fragments before calling a DMA. Figure 2 (a) shows the four main steps of this CPU-centric approach. The CPU first reads (gathers) the features, i.e., relevant rows of the Feature Array in this example, into its cache (1), it then writes them into consecutive locations in a temporary buffer (2) before it calls a data copy function to set up a DMA operation (3) and finally, the DMA hardware on the GPU reads the data from the temporary buffer in host memory into a corresponding buffer in the GPU memory (4).

In Figure 3, we show the impact of this CPU-centric data loading approach on GNN training. As a comparison, we use AlexNet (Krizhevsky et al., 2012) and ResNet-18 (He et al., 2015) as CNN examples and GraphSAGE (Hamilton et al., 2017) and graph attention network (GAT) (Veličković et al., 2018) as GNN examples. We use Torchvision (Marcel & Rodriguez, 2010) for CNN training and DGL backed by PyTorch for GNN training. While the time spent for data loading is less than 1% of the CNN training time, it consumes 47% and 82% of the GNN training time for GraphSAGE and GAT, respectively. As the vertical axis on the right of Figure 3 shows, CPU utilization is also much higher in GNN training. This happens partly because the data gathering part of the code is multithreaded and tries to maximize the throughput and thus minimize latency. Additionally, multi-threading is also used to maximize the performance of graph traversal and subgraph generation during data loading.

In short, in GNN training, unlike CNN training, data loading incurs significant time and resource overheads. In this work, we aim to reduce this overhead that comes from inefficient use of CPU resources in gather operations. We propose a GPU-centric approach to accessing data for GNN training based on the direct host-memory-access capability of modern GPUs (Figure 2 (b)). Modern GPUs have their own address translation units and are capable of accessing host memory directly. If GPUs are connected over PCIe, they can simply generate PCIe read/write I/O requests to the host. From the programmer’s point of view, accessing host memory can be simply done by dereferencing unified memory pointers just like dereferencing device memory pointers.

This direct access feature is different from the conventional unified virtual memory (UVM) method which is based on page migration. In UVM, the data transfer between host and GPU is done in page granularity which is at least 4kB per page in modern computing systems. Whenever a required page is missing from the GPU, the CPU needs to handle the page fault through a hardware interrupt service. Since the minimum data transfer granularity is a page and the hardware interrupt service process is costly, the performance of the UVM method depends on the applications’ spatial and temporal localities (NVIDIA, 2016). When dealing with highly irregular data structures such as a graph, using UVM incurs excessive page-faults and I/O amplification (Gera et al., 2020; Min et al., 2020; Sabet et al., 2020).

In the following section, we describe our implementation of PyTorch-Direct which enables GPU-centric data accesses for the PyTorch DNN library. We mainly focus on PyTorch in this work due to its straightforward and intuitive way of binding data to a certain physical location from the user’s perspective. But the main idea of the GPU-centric data accessing mechanism can still be applied to the other DNN frameworks such as TensorFlow.

## 4 PyTorch-Direct

This section describes the design and implementation of PyTorch-Direct. First, we provide an overview of design goals and introduce a new type of tensor, i.e., the unified tensor, which incorporates new concepts in need. We then discuss the unified tensor API and its advanced configurations. Finally, we describe our implementation and optimizations.

### 4.1 Overview

PyTorch-Direct aims to enable GPU out-of-memory training and inference for GNN while incorporating the direct access feature to improve data access performance. To achieve this, PyTorch-Direct presents to the developers several API features that are centered around a new type of tensor called “unified tensor”. It is a new, independent type parallel to PyTorch native GPU or CPU tensors, from both the perspective of user interface and its implementation in the runtime system. We have developed all the supporting code that allows unified tensors to be used as a full-fledged type of tensor in all PyTorch runtime activities such as memory allocator, torch.device class, dispatch, etc. This makes it extremely easy for the application developers to adapt their PyTorch code to use unified tensors.

Unified tensors are at the core of the PyTorch-Direct design which enables GPUs to directly operate on the host memory. Both of the underlying CUDA and CPU C++ codes of
PyTorch-Direct runtime code can directly access unified tensors by simply dereferencing unified memory pointers. In comparison, PyTorch native CPU tensors can be only accessed by CPU and GPU tensors can be only accessed by GPU, thus limiting the type of computation devices that can participate in the processing of these tensors. Unified tensors eliminate these limitations.

By default, PyTorch-Direct physically allocates the unified tensors in the host memory and allows GPUs to directly access them over the PCIe. Since the unified tensors are located in the host memory, their sizes can grow beyond the GPU memory size. From the CPU’s perspective, accessing the unified tensors is identical to accessing CPU tensors.

Application developers can adapt their PyTorch code to use unified tensors with minimal change to their code. In Listing 1, we show a simplified example of GNN training in PyTorch. After loading all the features into host memory, in every training step, it sends the features in the minibatch to GPU by calling to("cuda") before invoking the train function (line 10–13).

```python
# Load features into regular CPU tensor
features = dataload()

# Gather features using neighbor_id and then copy to GPU
input_features = \n    features[neighbor_id].to("cuda")

train(input_features, ...)
```

Listing 1: An example of GNN training in PyTorch.

The procedure with the unified scheme is shown in Listing 2. In this example, to migrate to the unified tensor scheme, the developer only needs to remove the to("cuda") invocation on features[neighbor_id] and instead invokes to("unified") on features at the beginning. The features of the whole graph is now stored in a unified tensor that can hold data beyond the GPU memory capacity. After that, GPU kernels that are launched by the train function can directly access features since it can access unified tensor and its derived tensors. Therefore, no more to() invocation is needed. Section 4.2 describes more about the API design, including advanced configurations.

```python
# Load features into unified tensor
features = dataload().to("unified")

# Gather features using neighbor_id and then copy to unified tensor
input_features = \n    features[neighbor_id]

train(input_features, ...)
```

Listing 2: GNN training in PyTorch-Direct with unified tensor. Only two lines (2 and 11) from Listing 1 are changed to incorporate unified tensor.

PyTorch-Direct APIs are designed to provide interface to unified tensors in the idiomatic PyTorch manner. Table 1 demonstrates typical use of unified tensor APIs. Developers can create a unified tensor by copying from another tensor via PyTorch built-in to() method of torch.Tensor. It can also be created from scratch by specifying the device argument as unified device in PyTorch APIs, such as torch.ones. The user can check if a tensor is of unified type by invoking the is_unified method.

Unified tensors can be computed with CPU or GPU tensors, providing great flexibility. Meanwhile, they are free from redundant data movements since CPU and GPU can directly access their underlying memory without creating temporary copies. By contrast, in the native PyTorch API, CPU tensors typically cannot work with GPU tensors because of the device binding, unless additional routines to handle them have been implemented manually in PyTorch runtime system. For example, subscript operator allows a GPU tensor to be indexed by a CPU tensor, and binary and comparison operators accept GPU scalar and CPU scalar as the two operands.

PyTorch-Direct also exposes two configurations, placement rule hints and cudaMemAdvise hints, so that experienced developers can perform advanced optimizations. These hints can be used in a handful of APIs, as shown in Table 2.

One configuration is the placement rule hint flag, propagatedToCUDA, that is owned by each unified tensor. The placement rules will be detailed in Section 4.3. PyTorch-Direct allows the developer to specify the placement rule hint during creation, and switch in the middle. Switching is provided by the set_propagatedToCUDA
method. It only switches the placement rule of a unified tensor without memory allocation, deallocation or data copy. Though this is a torch.Tensor method, invoking this method on a non-unified tensor triggers RuntimeError.

As for cudaMemAdvise, PyTorch provides the interface to suggest the CUDA runtime to populate, migrate or prefetch data on the specified device. This can be done by invoking the memAdvise method of torch.Tensor. The two parameters of the memAdvise method are the same as cudaMemAdvise, though they are in the form of Python str and torch.device. PyTorch-Direct runtime converts the arguments and invokes cudaMemAdvise. Similar to set_propagatedToCUDA, the memAdvise method triggers a RuntimeError if the argument tensor is not of unified type.

Users may also specify the cudaMemAdvise hint as optional arguments in tensor creation methods invocation, just like in the case of placement rules. In such cases, PyTorch-Direct invokes cudaMemAdvise right after the memory allocation. On the other hand, the developer may instead invoke the tensor's memAdvise method after its creation. However, the implementation of some PyTorch tensor creation APIs involves GPU accesses to the new tensor before returning to the Python interpreter, bringing in side effects to the CUDA runtime. In such cases, calling memAdvise method instead of specifying cudaMemAdvise keywords in creation cannot properly affect the GPU accesses that happen before the creation function returns, which can lead to unexpected cudaMemAdvise outcomes.

4.3 Computation and Storage Placement Rules

Although the unified tensor type abstracts away the binding to physical devices, the computation of each operator needs to be executed in one of the physical CPU or GPU devices. The runtime also needs to determine which one of the physical devices should hold the output tensors. Moreover, in cases where the output tensors are to be reused for multiple times by a GPU device, it will be more performant to explicitly transfer them to the GPU device’s memory, instead of having the GPU repetitively perform direct access to them from the host memory.

Thus, it is important to clearly specify the computation and storage placement rules applied to each operation as well as to allow application developers to take advantage of data reuse opportunities. To achieve this, each unified tensor indicates its placement preference between two options with its propagatedToCUDA flag. The placement rule for each operator is determined dynamically.

A unified tensor with propagatedToCUDA set to True prefers GPU as the computation device. Besides, it prefers the output tensor type to be GPU or unified. Placing computation to GPU and creating GPU output tensors give the best performance when the output tensor is reused after the computation. A unified tensor with propagatedToCUDA set to False prefers the opposite.

Complications arise when the operands of an operation are of different tensor types or indicate opposite preferences. The complete placement rules are shown in Table 3. It uses “propagation” to refer to unified tensor with propagatedToCUDA set to True, and “non-propagation” to indicate otherwise. The table lists the computation device and output tensors type in all the six scenarios, with rows specifying the condition of non-unified tensors and columns specifying the condition of unified tensors.
4.4 Implementation Details

The core object in PyTorch runtime system is `at::Tensor`. Every PyTorch tensor (torch.Tensor object) is a THPVariable object in C++ runtime code, which is the wrapper class combining an `at::Tensor` object with Python metadata. The PyTorch runtime dispatches each method call to the right definition according to the device and data types of the tensor arguments. A PyTorch method operating on tensors goes eventually into a function of `at::Tensor`.

PyTorch-Direct implements the unified tensor mechanisms in PyTorch runtime as a complete type of tensor. This allows the design to be modular, extensible, and well integrated into the PyTorch runtime code. A new memory allocator is implemented to govern the memory allocation for all unified tensors. It adapts the allocation recycling mechanism from the PyTorch CUDA allocator to reduce the number of CUDA API invocations.

Two dispatch keys are introduced to the runtime system. They each represent either state of the `propagatedToCUDA` flag of the unified tensor and participate in resolving the placement rules of operators, as detailed in Section 4.3. Therefore, PyTorch-Direct now dispatches invocations with unified tensors according to the dispatch table of unified tensors, allowing future extensions. PyTorch-Direct in most cases dispatches to existing CPU or CUDA definitions because they can directly access the memory underlying unified tensors without modifications. Nevertheless, we augment the logic of a few tensor creation methods to use unified memory allocator in the cases where unified tensors should be created.

PyTorch-Direct also implements other facilities, such as `c10::DeviceTypes` for unified device and auxiliary methods to determine if an `at::Tensor` object is of unified type. They are helpful in developing new logic and reusing existing code. For example, an existing GPU or CPU operator definition checks if tensors are of GPU or CPU type at the beginning. Modifying such checks to allow unified tensor enables the same function definition to also work for unified tensors.

4.5 Memory Alignment Optimization

To achieve efficient PCIe data transfer, memory requests from the GPU threads in the same warp should be aligned and merged to the GPU cacheline (128-byte) granularity (Min et al., 2020). However, the default PyTorch GPU indexing function does not guarantee the memory alignment unless the input feature tensors are naturally aligned with the GPU cacheline size. In Figure 4, we depict a simplified working mechanism of the default PyTorch GPU indexing function. In this specific example, we scale down the warp size (32 threads in real) and the GPU cacheline size (128-byte in real) by a factor of 8. We assume each feature is 4-byte and each node has 11 features. Now, due to the size mismatch between the cacheline (16-byte) and the node feature (44-byte), misaligned accesses can occur.

In the example of Figure 4, assume the GPU needs to access the 0th, 2nd, and 4th nodes. To achieve this, each thread accesses a single feature. For example, the first 11 threads access the 11 features of the 0th node, next 11 threads access the 11 features of the 2nd node, and so on. This looks simple in a logical view on the left side of Figure 4, where we highlight the accesses of thread 11-21 to features of node 2. However, when we redraw the access patterns based on cacheline and warp alignments on the right side of Figure 4, we can see that the accesses are fragmented into multiple cachelines and warps.

To solve the problem of misaligned access patterns, we use a circular shift method as described in Figure 5. In this method, all threads calculate the required index offset values to make aligned accesses. In the case of Figure 5, the threads need to do a right shift by an offset of 1. The threads on the edges check the boundary conditions and make additional adjustments by adding or subtracting the length of the node feature so that they do not accidentally access the other node features. When the indexed values are written to the output, the output indices are also identically adjusted to maintain the ordering. With the optimization, PyTorch-Direct reduces the number of total PCIe requests from 7 to 5 in this case. Inside the PyTorch GPU indexing kernel, we check the input tensors and apply this optimization only when the input tensors are unified tensors and the feature widths are not naturally aligned to 128-byte granularity. All these adjustments are automatically made as a result of our modifications to PyTorch source code. As such, there

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| Table 3: Placement Rules Applied to Operators with Unified Tensors Operands |
|---------------------------------------------------------------|
| All unified tensors prefer propagation. | At least one unified tensor prefer non-propagation. |
| At least one operand is non-scalar CPU tensor. | compute on output type |
| Previous row is not applicable. And, at least one is GPU tensor operand. | GPU unified non-propagation |
| All non-unified tensors are CPU scalars. Or, no non-unified tensors exist. | compute on output type |
| CPU if no operand prefers propagation, else GPU unified non-propagation | |

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is no programmer effort required for solving the memory alignment problem.

5 Evaluation

In this section, we evaluate PyTorch-Direct performance using a well-defined microbenchmark and end-to-end GNN training. Using the microbenchmark, we demonstrate that (1) PyTorch-Direct is faster than the baseline PyTorch approach in accessing features from GPU under different combinations of data sizes and systems and (2) the effectiveness of our optimized memory alignment mechanism. In GNN training, we show the benefit of using PyTorch-Direct for faster training with lower power consumption.

5.1 Evaluation Setup

Datasets: The datasets we use for the GNN training evaluation are shown in Table 4. For the sk-2005 (Boldi & Vigna, 2004), twitter7 (Kwak et al., 2010), and wikipedia_link_en (Kunegis, 2013) datasets, we have created them from existing real world graphs but with synthetic feature values just for the purpose of training time evaluation. Datasets reddit (Hamilton et al., 2017), ogbn-products, and ogbn-papers100M (Hu et al., 2020b) are commonly used datasets in the field for comparing the training accuracies between different GNN architectures.

Test System: The platforms we have used for the evaluation are described in Table 5. We use NVIDIA 450.51.05 driver and CUDA 10.2 on the evaluation platforms. System2 and System3 configurations are only used in Section 5.2.

Microbenchmark: We would like to answer the following questions with the microbenchmark:

- How does increasing the feature size affect the PyTorch-Direct performance? The feature sizes vary greatly across datasets. For example, while a node of ogbn-products (Hu et al., 2020b) has 100 features, a node of reddit (Hamilton et al., 2017) has 602 features.
- How does increasing the number of features to be copied affect the PyTorch-Direct performance? Depending on factors such as a connectivity of the input graph and the batch size, the number of neighboring nodes which need to be fetched per batch can vary.
- How well does the alignment optimization as discussed in Section 4.5 work with misaligned input features?
- What is the performance impact of using PyTorch-Direct on different systems?
The microbenchmark is designed to mimic the behavior of the data gathering and copy processes in the GNN training. The microbenchmark uses a random number generator (RNG) to generate random indices which are used to index feature values. The total number of items is fixed to 4M for all experiments.

**GNN Training**: In this evaluation, we use GraphSAGE (Hamilton et al., 2017) and graph attention network (GAT) (Veličković et al., 2018) implementations from the deep graph library (DGL). Both implementations of DGL have all necessary supports (e.g., subgraph generation) to perform GNN mini-batching, which makes it suitable to work even if the input graphs cannot be fit in to the GPU memory. The features are located in host memory and during training only the immediately required features are transferred to the GPU memory. In the baseline implementation with PyTorch, the required features are gathered by the CPU and then copied to the GPU memory through DMA. In the PyTorch-Direct implementation, the entire features are located in the unified tensor and the GPU directly accesses only the immediately required features. Beside the data movement parts, the core training algorithms of the DGL implementations are left unmodified.

### 5.2 Microbenchmark - Size and System Dependency

The result of copying different numbers of features with different sizes are shown in Figure 6. The ideal case only includes the pure data transfer time under the theoretical peak bandwidth of interconnect. Due to the lack of system memory, we do not run the (256K, 16KB) setup with System3. With the baseline PyTorch approach, the performance varies greatly depending on the system configurations. While the slowdowns in System2 are about 3.31× to 5.01×, and the slowdowns in System1 are about 1.85× to 2.82×. On the other hand, with PyTorch-Direct, we are able to consistently reach near to the ideal performance regardless of the system configuration unless the data transfer volume is very small. When the total data transfer volume is very small, the overall execution time is dominated by the CUDA API calls and kernel launch overheads. Except for the (8K, 256B) case, the baseline PyTorch approach shows 1.85× to 3.98× slowdowns while PyTorch-Direct shows only 1.03× to 1.20× slowdowns compared with the ideal case. Overall, PyTorch-Direct shows about 2.39× of performance improvement in average compared to the baseline PyTorch approach.

### 5.3 Microbenchmark - Memory Alignment

To evaluate the impact of the memory alignment optimization in PyTorch-Direct, we measure data access times for various feature sizes from 2048-byte to 2076-byte in 4-byte stride. The evaluation result is shown in Figure 7. For the PyD Naïve case, we use unmodified GPU indexing kernel from PyTorch and the kernel has no knowledge of memory alignment. For the PyD Optimized case, the optimization from Section 4.5 is applied.

Figure 7 shows that PyTorch-Direct reduces the data access time significantly compared to the PyTorch baseline. However, the benefit is only limited without the memory-alignment optimization. For example, when the feature size is 2052-byte, the PyD Naïve provides only 1.17× of performance improvement over Py, while the PyD
Figure 8: Single epoch execution time breakdown for both PyTorch (Py) vs. PyTorch-Direct (PyD) when running (a) GraphSAGE and (b) GAT in different datasets. Training epoch time reductions written on the bars.

Optimized provides $1.95 \times$ of performance improvement. Based on the results, we observe the optimization provides a consistent benefit over the PyTorch baseline (averagely $1.93 \times$) regardless of the data alignment.

5.4 GNN Training Performance

In Figure 8, we compare the breakdown of the training epoch time when using unmodified DGL implementations in PyTorch vs. PyTorch-Direct. In the GAT training, we do not run sk dataset due to the DGL’s out-of-host-memory error for both PyTorch and PyTorch-Direct cases. Similar to the microbenchmark results in Section 5.2, we observe about 47.1% of reduction in the feature copy times. The other portions of the training epoch times remain almost identical to the baseline case. PyTorch-Direct gives less benefit for datasets with smaller feature sizes (e.g. paper), because the feature copy time is smaller in the end-to-end training time. Similarly, GAT training is computationally heavier than GraphSAGE and therefore we observe a less benefit of PyTorch-Direct. Overall, we observe between $1.01 \times$ to $1.45 \times$ speedup when we use PyTorch-Direct in GNN training.

With more efficient data access, in addition to the training speedup, PyTorch-Direct saves system power by 12.4% to 17.5% during GNN training. Figure 9 compares power consumptions across different GNN trainings measured at electricity meter.

6 Conclusion

In this work we present PyTorch-Direct, which proposes a GPU-centric rather than a CPU-centric data access paradigm for GNN training. We show that PyTorch-Direct is effective in reducing CPU utilization in GNN training and results in higher end-to-end training performance and lower power consumption. For the input data sets and GNN architectures evaluated, PyTorch-Direct reduces the overall training time by up to 38.2% and saves system power by up to 17.5%. PyTorch-Direct has minimal required programmer effort. Users can take full advantage of the benefits PyTorch-Direct provides by modifying at most two lines of their original code.

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