Two-dimensional arrays of ordered, highly dense and ultra small Ge nanocrystals on thin SiO$_2$ layers

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Abstract. In this work, we have developed two original processes for the fabrication of 2-dimensional arrays of ordered Ge nanocrystals embedded in thin SiO$_2$ layers for their use in nanocrystal floating gate memories. Ordering is achieved by a combination of focused ion beam nano-patterning and self assembly of Ge islands on the patterned SiO$_2$ surface. In the first process the Ge islands are grown by selective chemical vapor deposition of Si / Ge / Si on Si holes fabricated by FIB patterning, while the second process uses solid phase epitaxy by MBE of amorphous Ge on SiO$_2$ at room temperature, followed by annealing for crystallization. Highly ordered and highly dense (1.5×10$^{11}$/cm$^2$) ultra-small (~ 20 nm) Ge dots on SiO$_2$ were achieved by both processes. This work has been carried out within the European IST project FORUM FIB: Fabrication, Organisation and Use of Memories obtained by Focused Ion Beam.

1. Introduction
Semiconductor nanocrystal memories are investigated as alternative technologies to conventional non-volatile polysilicon floating gate memories (NVM), which show limitations in following device scaling down. In nanocrystal memories the floating gate constitutes a distributed charge storage medium, which permits the use of thinner oxide layers than in the case of the electrically continuous polysilicon floating gate. So far, most of the studies in this field have been devoted to silicon nanocrystals (NCs) embedded in SiO$_2$ and fabricated by different techniques. The maximum NC density reached was $\sim 2 \times 10^{12}$/cm$^2$. However, although a high density is desirable in order to reduce the device area for the same stored charge, there is a maximum density for which lateral diffusion of the stored charge is limited. This was found to be of the order of $\sim 3 \times 10^{11}$/cm$^2$ [1]. Requirements in NCs density, size, interspacing etc. are widely discussed in the literature [2].

In order to improve data retention in NVM it is interesting to use Ge instead of Si NCs because of the important valence band offset between substrate and NCs, even for large islands. This produces two phenomena: a faster charging process in Ge islands and a larger potential barrier for carrier leakage to the substrate, resulting in a larger retention time [3-7]. Recent theoretical studies have demonstrated the better retention properties of Ge NC memories, compared with those based on Si NCs and an ideal size for Ge islands of $\sim$15 nm [8].

Ge islands (quantum dots: QDs) are known to develop during epitaxial growth on Si in the Stranski–Krastanov growth mode. Recently, various self-assembling methods have been attempted in
order to create regular 2D arrays of Ge QDs on Si, however neither ordering nor high density of QDs were achieved. The lack of lateral ordering is due to the random heterogeneous nucleation of Ge nanodroplets on Si during CVD growth experiments. Moreover, kinetics of formation and coalescence of nanoclusters which are still not well understood lead to size non-uniformity. Improvement in QD ordering and size uniformity are necessary towards using Ge QDs in reliable devices.

In the present work we have developed two different processes that permit to obtain highly dense 2D periodic arrays of ordered Ge QD on oxidized silicon substrates. They both start with nanopatterning of an ultra thin oxide (UTO) layer on Si by a focussed ion beam (FIB), followed by subsequent self-assembling of Ge NCs on the patterned area. In the first case Ge island growth is made by selective chemical vapour deposition on Si holes in the oxide, while in the second case a patterned UTO is created on which Ge QDs are grown by MBE deposition of amorphous Ge at room temperature, followed by annealing for crystallization.

2. Experimental results and discussion
A field oxide, 500nm thick, was first fabricated on all wafers. Using standard optical lithographic techniques and wet chemical SiO\textsubscript{2} etching, 10×10µm\textsuperscript{2} windows were opened in this oxide in order to easily locate the arrays of holes produced by FIB. The wafers were then oxidized again to form the oxide mask for FIB milling (10 or 20nm thick SiO\textsubscript{2} layer).

Milling investigations were performed with a Philips FEI FIB XL 200 TEM. The FIB instrument is equipped with a Gallium liquid metal primary ion gun. With such a type of field emission gun the minimum spot size is ~10 nm and the brightness is very high. Both features combined with the ion mass and energy used allow a sharp and fast milling of silicon. The FIB process has been performed using a dual beam system in order to minimize the possible Gallium implantation during image grabs required for target area location. Navigation on the wafer surface is done using SEM imaging mode. FIB was used only for milling. However, the center of the wafer has been used to setup the instrument. Ion source gallium at normal incidence angle with impact energy of 30 keV and 1 pA primary current were used.

After FIB milling, Ga was removed by chemical cleaning in HCl:H\textsubscript{2}O followed by RTA at 900°C 1 minute in N\textsubscript{2}.

The formation of regular 2D Ge dots arrays was obtained following two flow charts schematically described in Figure 1.

1- Selective epitaxial growth (SEG) of Ge NCs in Si holes in SiO\textsubscript{2} was carried out in a cold wall load-locked high vacuum LPCVD system with a base pressure of 7×10\textsuperscript{-8} Torr. The pressure was 0.1

Figure 1. Schematic representation of the fabrication process for ordered Ge QDs on an oxidized Si wafer. (a) Selective epitaxial growth in Si holes on SiO\textsubscript{2} by LPCVD and (b) MBE deposition of amorphous silicon on patterned SiO\textsubscript{2}, followed by annealing.
Torr during deposition using as source gas He-diluted GeH₄ and Si₂H₆ and H₂ as carrier-gas. The typical growth temperature was 700°C. Details on dot growth in holes in SiO₂ of different diameters were given elsewhere [1,10].

2- Solid phase epitaxy (SPE) was carried out in a Riber MBE system with a base pressure of 10⁻¹¹ Torr. Si and Ge were evaporated from an electron beam evaporator and an effusion cell respectively. The deposition rates were about 0.03 nm/sec. Ge was deposited at room temperature and crystallized by in-situ annealing at 650°C for 30 min.

The above two processes have been designed for implementation in a MOSFET fabrication process. Morphological characterization of the samples was performed by AFM operating in air in tapping mode.

Figure 2. SEM images of (a) FIB hole ~ 60 nm wide written in 76 nm SiO₂ and (b) Si-Ge-Si dot selectively grown in the Si hole in SiO₂. The diameter of the dot is ~ 60 nm. (c) SEM image of the Si/Ge/Si stack after oxide etching and re-oxidation, as in the process flow of figure 1.

Figure 3. AFM images of a regular array of FIB holes with diameter of about 40 nm before (a) and after (b) the deposition of Si/Ge/Si stack. (c) and (d) show the perfectly uniform 2D dot arrays after oxide removal in an area of 250 x 250 nm² and 1x1 µm² respectively. Experimental details are given in [10].
We have performed first experiments with wafers where the oxide patterned by FIB was rather thick (20 nm). Figure 2a and 2b display SEM images of a FIB hole before and after deposition of 20 nm Si / 0.7 nm Ge / 20 nm Si respectively. The stack obtained after thermal oxidation of the complete structure is presented in figure 2c. Diameter of the pillar was determined in relation with the thickness of the Si layer in contact with the substrate in order to ensure a good oxide uniformity below the pillar. More details about the process optimisation can be found in [10]. Increase of FIB hole density leaded to regular Ge dots of uniform size and a density of $5 \times 10^{10}$ dots/cm$^2$. An example is given in figure 3, where AFM images of dot arrays are shown.

The second process developed is based on MBE deposition of Ge at room temperature, followed by annealing. The deposited Ge is amorphous, 1 nm thick. Annealing is done at 650°C for 20 or 30 min. The formation of Ge NCs is induced by the combination of crystallisation and un-wetting of Ge on SiO$_2$. Ordering takes place on the top areas between the FIB holes because of energetic parameters. Mechanisms of formation and ordering of Ge NCs are discussed in [11]. Figure 4 shows AFM images of: (a) a patterned ultra thin oxide, 5 nm thick, with a pitch of 50 nm (density of patterns ~ $4 \times 10^{10}$/cm$^2$) before Ge deposition and (b) after self-assembling of Ge NCs on the patterned oxide.

4. Conclusion
In this work ultra-dense 2-D arrays of FIB holes on ultra thin SiO$_2$ layers were fabricated (densities about $10^{11}$/cm$^2$) and they were used to grow high density ordered Ge QDs of uniform size by two techniques: a) selective Ge growth by LPCVD on FIB holes in the oxide and b) MBE deposition of Ge at room temperature, followed by situ crystallization. The obtained dot arrays are adequate for use in Ge nanocrystal memories.

5. References
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