The d and q Axes Technique for Suppression Zero-Sequence Circulating Current in Directly Parallel Three-Phase PWM Converters

DECHA PANPRASERT, (Member, IEEE), AND BUNLUNG NEAMMANEE
Department of Electrical and Computer Engineering, King Mongkut’s University of Technology, North Bangkok 10800, Thailand
Corresponding author: Decha Panprasert (dps.mee@gmail.com)

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ABSTRACT The directly parallel pulse width modulated converter (DPC) method is used to construct large-scale converter systems to increase system performance and reduce costs. However, circulating currents arise when the converters supply unbalanced currents or have different converter parameters. Circulating currents cause distortions in the current, increase the current coming from each converter, and degrade the system performance. This paper proposes a circulating current control (CCC) methodology to eliminate circulating currents through the analysis and approximation of the circulating current of the fundamental harmonic current at 150 Hz. By using the phase shift technique, this new model of the circulating current in the $0_d$-axis was extended to the $0_d$- and $0_q$-axes. The proposed CCC was then designed according to the new circulating current model and added to the conventional controller. The performance of the proposed CCC converter was verified via simulation and experimentally with three directly parallel 5.5 kVA converters. The proposed CCC enhanced controller and conventional controller were tested with various current values, and all resulting circulating currents were recorded. The experimental results showed that the proposed CCC eliminated nearly all the circulating currents and that it had a fast, dynamic response to step-change currents. Using ramp current sharing, the experimental results were confirmed. Additionally, the efficiency of the proposed CCC in the DPC was significantly higher than the conventional controller, and the system’s efficiency was the same as that of a single converter connection. Thus, using the proposed CCC in DPC systems is economical, highly efficient, modular, and flexible.

INDEX TERMS PWM converter, directly parallel PWM converters, circulating current control, current sharing, CCC.

I. NOMENCLATURE

- $d_{ax}, d_{bx}, d_{cx}$: modulation signal of phases $a, b, c$ of converter $x$: $x = 1, 2, \ldots n$
- $d_{acx}, d_{bcx}, d_{ccx}$: compensated modulation signal of phases $a, b, c$ of converter $x$: $x = 1, 2, \ldots n$
- $d_{dSVMx}, d_{bSVMx}, d_{cSVMx}$: space vector modulation (SVM) of phases $a, b, c$ of converter $x$: $x = 1, 2, \ldots n$
- $d_{dx}, d_{qk}, d_{dx}$: modulation signal of the $d-, q$-axes
- $d_{kx}$: duty ratio for phase $k$ of the $x^{th}$ converter
- $d_{comax}, d_{combx}$: zero-sequence modulation signal of the $0_d$-axis of converter $x$
- $d_{comax}, d_{comq}$: zero-sequence modulation compensation signal of the $0\alpha$-, $0\beta$-axes
- $d_{com0d}, d_{com0q}$: zero-sequence modulation compensation signal of the $0d$-, $0q$-axes
- $d_{0SVMx}$: HEPWM
- $i_{ax}, i_{bx}, i_{cx}$: current of converter $x$: $x = 1, 2, \ldots n$
- $i_{ax}, i_{bcx}, i_{ccx}$: grid current
- $i_{0d}, i_{0q}$: grid current in the synchronous reference frame

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II. INTRODUCTION
Pulse width modulated (PWM) converters are popular converters used for low-voltage and high-power applications, such as bidirectional conversion, renewable energy, energy storage systems, three-phase power factor correction (PFC), and distributed generators (DGs) [1]. These converters can be set up in parallel to increase the power rating, reliability, and efficiency and decrease the current and voltage ripples. Parallel converters work well in modular system designs, providing flexibility and ease in system maintenance [2], [3].

The structure of a DPC system is shown in Fig. 1. The grid sides of each converter have a common connection at nodes a, b, c, and the DC busses have a common connection at nodes P and N. The currents for each converter, namely, \(i_{dx}, i_{qx}\), \(i_{0x}\), \(i_{0x}, i_{0y}, i_{0z}\), are divided into two main parts. The first part flows to the grid, and the second part flows to the other parallel converters, resulting in circulating current. However, when the converters are directly parallel, circulating currents are generated automatically. These currents can cause current distortion, increase the current of each converter, and degrade the overall performance. Circulating currents can be the result of different parameters for each converter, unbalanced current sharing, and other aspects, such as unequal dead time, measurement errors, and analog-to-digital conversion errors. There are many techniques for avoiding circulating currents, such as using isolated DC supplies [4] or isolation transformers [5], [6]. Interphase reactors connected between the converters can be used to increase the impedance and thus reduce the circulating current, but these reactors can reduce only medium-frequency and high-frequency circulating currents, not low-frequency, circulating currents [7], [8]. In addition, these methods are bulky and costly because hardware needs to be added. The methods used to eliminate circulating currents without additional hardware are applied directly to the parallel PWM converters and are listed as follows.

A. SYNCHRONIZED CONTROL
This approach basically treats the DPC as one converter through a synchronization control signal. For example, a parallel converter system with two converters can be controlled as a single six-phase converter [9] in which the switch timing of the DPC is synchronized through fiber-optics [10]. This method can reduce the circulating currents, but it requires balanced current sharing. Furthermore, the control system design is complicated. References [11], [12] present a method to reduce the high-frequency circulating currents of the DPC by shifting the carrier signal of the converter to the proper position to reduce the circulating current. However, this method does not control the circulating current at low frequency (frequency 150 Hz).

B. SPECIAL PWM TECHNIQUE
The special PWM technique can be used in place of traditional space vector pulse width modulation (SVPWM) to eliminate the circulating current. In [13], Chen proposed the harmonic elimination pulse width modulation (HEPWM) method, which effectively eliminates the circulating current but suffers from high switching losses. A multicarrier PWM technique was proposed by Hou [14]. This technique can effectively mitigate the circulating current by eliminating the use of zero vectors, but it has difficulties in generating a PWM signal and requires additional hardware.

C. CIRCULATING CURRENT CONTROL
Circulating currents are caused by unequal zero-sequence modulation signals of the converters. A PI controller is used
to eliminate the circulating current [15]–[17] by making the zero-sequence modulation signals of the converters the same, but its bandwidth is limited, so it cannot respond promptly. Tsung [18] proposed the feed-forward method, which allows each converter to use a common zero-sequence modulation signal. On the other hand, Zhang [19], [20] proposed a feed-forward zero-sequence modulation signal to expand the bandwidth of the 0-axis current loop. Reference [21] proposes a PI-quasi resonant controller to control circulating current and feed-forward controller to reduce the difference in duty cycles. However, the zero-sequence modulation signal of the first converter needs to be sent to generate the modulation signals of the other converters. Both methods can effectively eliminate the circulating current, but a high-resolution analog zero-sequence modulation signal must be sent, so these methods are difficult to implement.

This paper proposes a CCC method for a DPC that eliminates the bandwidth limitations of a PI controller in the 0-axis current loop without a feed-forward zero-sequence modulation signal. This proposed transformation technique has the following advantages:

1) Circulating currents are eliminated without additional hardware.
2) Each converter in the DPC is controlled independently to facilitate the modular design and to increase the overall performance.
3) The total cost is reduced.

In this paper, in section II, an equivalent circuit model of the DPC is derived to analyze the behavior of a circulating current when an SVPWM modulation technique is used. The circulating current approximation and transformation, the proposed circulating current model in the 0-axis, and the proposed CCC methodology are described in section III. Section IV discusses the simulation results, and section V goes over the experimental system, system parameters, and case studies. The last section offers conclusions.

III. CIRCUIT CURRENT BEHAVIOR IN A DPC
A. EQUIVALENT CIRCUIT MODEL FOR A DPC
For the sake of convenience, node $N$ in Fig. 1 is used as a reference point, and the duty ratio of the top switch in phase $k$ ($k = a, b, c$) of converter $x (x = 1, 2, \ldots n)$ is defined as $d_{kx}$. Hence, the average mathematical model of a converter in the stationary reference frame can be obtained as shown in Eqs. (1) and (2).

$$\frac{d}{dt} \begin{bmatrix} i_{d_x} \\ i_{q_x} \\ i_{0_x} \end{bmatrix} = \begin{bmatrix} v_{am} \\ v_{bn} \\ v_{cn} \end{bmatrix} + \begin{bmatrix} v_n \\ v_n \\ v_n \end{bmatrix} + \begin{bmatrix} d_{kx} \\ d_{kx} \\ d_{kx} \end{bmatrix} \cdot v_{dc} \quad (1)$$

$$C \frac{dv_{dc}}{dt} = \begin{bmatrix} i_{d_x} \\ i_{q_x} \\ i_{0_x} \end{bmatrix} - i_{dc} \quad (2)$$

FIGURE 2. Equivalent circuit model of a PWM converter in the synchronous reference frame.

Eqs. (1) and (2) can be transformed into a synchronous reference frame by using Eqs. (3) and (4).

$$T_{abc/dq0} = \begin{bmatrix} \cos \omega t & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ -\sin \omega t & -\sin(\omega t - \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) \end{bmatrix}$$

$$X_{dq0} = T_{abc/dq0} \cdot X_{abc} \quad (3)$$

Then, the average mathematical model of PWM converters in the synchronous reference frame can be obtained as Eqs. (5) and (6).

$$L_x \frac{d}{dt} \begin{bmatrix} i_{d_x} \\ i_{q_x} \end{bmatrix} = \begin{bmatrix} v_d \\ v_q \end{bmatrix} + L_x \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_{d_x} \\ i_{q_x} \end{bmatrix} + \begin{bmatrix} d_{dx} \\ d_{qx} \\ d_{0x} \end{bmatrix} \cdot v_{dc} \quad (5)$$

$$C \frac{dv_{dc}}{dt} = \begin{bmatrix} i_{d_x} \\ i_{q_x} \end{bmatrix} - i_{dc} \quad (6)$$

Using the average mathematical model in Eqs. (5) and (6), one can write the equivalent circuit model for each PWM converter in the synchronous reference frame, as shown in Fig. 2. Each equivalent circuit model is composed of four circuits; on the left-hand side of Fig. 2, the circuit is composed of three independent current sources, namely, $d_{0x}i_{0x}$, $d_{qx}i_{qx}$, and $d_{dx}i_{dx}$, that connect in parallel with a DC bus $v_{dc}$. The three circuits on the right-hand side at the top, middle, and lower parts of the circuit represent the equivalent circuits in the $d$-axis, $q$-axis, and $0$-axis respectively. The top two circuits are each composed of an inductor, an independent voltage source, and two dependent voltage sources. There are two voltage cross-couplings between the two circuits, namely, $\omega L_x i_{dx}$, and $\omega L_x i_{dx}$. For the top circuit, the signal $d_{dx}$ is used to control
the currents to the grid. If the voltages is not controlled by the conventional controller and is parallel value, and dividing the value by three, as in Eq. (7) below.

\[ i_{dx} = \frac{1}{3}(i_{acx} + i_{bcx} + i_{ccx}) \]  

(7)

B. ANALYSIS OF CIRCULATING CURRENT BEHAVIORS

From the 0-axis circuit on the lower right-hand side of Fig. 3, the circulating current \( i_{0x} \) does not occur when the zero voltages \( d_{0x}v_{dc} \) or zero-sequence modulation signals \( d_{0x} \) of the converters are equal, as shown in Eqs. (8) and (9).

\[ d_{01}v_{dc} = d_{02}v_{dc} = \ldots = d_{0n}v_{dc} \]  

(8)

\[ d_{01} = d_{02} = \ldots = d_{0n} \]  

(9)

Circulating currents appear when the zero-sequence modulation signals \( d_{0x} \) are unequal, which could be the result of differences in the converter’s parameters or unbalanced current sharing. If the zero-sequence modulation signals \( d_{0x} \) of the converters are the same, circulating currents do not appear.

Fig. 4(a) shows the block diagram of the SVPWM signal generator of the conventional PWM converter. The modulation signals in the \( d- \) and \( q- \) axes \((d_{dx} \) and \( d_{qx} \)) are sent from the current controller and then transformed to \( d_{ax} \) and \( d_{bx} \), respectively, via the \( dq/\alpha \beta \) block. The SVM block receives the \( d_{ax} \) and \( d_{bx} \) signals and converts them to sinusoidal signals located on the \( \alpha- \), \( \beta- \), and \( c- \) axes with modulation indexes of 1. Then, the \( d_{0x} \) signal, according to Eq. (10), compensates to reduce the modulation index. For the output signals \( d_{ax}, d_{bx}, \) and \( d_{cx} \), the compensated signals, \( d_{ax}, d_{bx}, \) and \( d_{cx} \), respectively, are sent to the PWM block to generate the gate drive signals. Fig. 4(b) shows that the modulation signals of the \( \alpha- \), \( \beta- \), and \( c- \) phases are \( d_{ax}, d_{bx}, \) and \( d_{cx} \), respectively, at a frequency of 50 Hz. The zero-sequence modulation signal \( d_{0x} \) has a triangular shape with a frequency of 150 Hz.

\[ d_{0x} = \frac{1}{3}(d_{ax} + d_{bx} + d_{cx}) \]  

(10)

The zero voltage \( d_{0x}v_{dc} \) has the same shape as \( d_{0x} \) but a different amplitude. By using the Fourier series transformation, the zero voltage, \( d_{0x}v_{dc} \) can be written as Eq. (11).

\[ d_{0x}(\omega t)v_{dc} = \frac{8A_c}{\pi^2}v_{dc}[\sin(\omega t) - \frac{1}{9}\sin(3\omega t) + \frac{1}{25}\sin(5\omega t) - \ldots] \]  

(11)

where \( A_c \) is the amplitude of the zero-sequence modulation signal.

The zero voltage, \( d_{0x}v_{dc} \) generates circulating currents when the amplitudes and phases of these voltage sources are unequal. From Fig. 5, the circulating current \( i_{0x} \) that flows through converter \( x \) can be written as Eq. (12).

\[ i_{0x} = i_{0x1} + i_{0x2} + \ldots + i_{0xn} \]  

(12)
where \( i_{0\alpha} \) is the \( 0 \)-axis current of \( x \)-th converter caused by the voltage source \( d_{0\alpha}v_{dc} \) of the \( n \)-th converter.

The current \( i_{01} \) is the \( 0 \)-axis current caused by the converter and can be calculated by dividing Eq. (11) by its impedance at each harmonic frequency, as shown in Eq. (13), as shown at the bottom of the page.

We assume that \( L = L_1 = L_2 = \ldots = L_n \) and \( L \) can be found with Eq. (17).

From Eq. (12), the current \( i_{01x} (x \neq 1) \) is the current in \( 0 \)-axis flowing through converter 1 from other converters and can be calculated according to Eq. (16).

From Eqs. (12), (15), and (16), the circulating currents of converter 1, namely, \( i_{01} \), can be found with Eq. (17).

\[
i_{01} = \left[ KA_1 - \frac{K}{n-1}(A_2 + A_3 + \ldots + A_n) \right] \cdot \sin(\omega t) - \frac{1}{27} \sin(3\omega t) + \frac{1}{125} \sin(5\omega t) - \frac{1}{343} \sin(7\omega t) + \ldots
\]

The circulating current of converter \( x \), namely, \( i_{0x} \), can be found with Eq. (18).

\[
i_{0x} = i_{01}^{\prime\prime} \sin(\omega t) - \frac{1}{27} \sin(3\omega t) + \frac{1}{125} \sin(5\omega t) - \frac{1}{343} \sin(7\omega t) + \ldots
\]

where

\[
i_{0x} = \left[ KA_1 - \frac{K}{n-1}(A_1 + A_2 + \ldots + A_{x-1} + A_{x+1} + \ldots + A_n) \right] \cdot \sin(\omega t) - \frac{1}{27} \sin(3\omega t) + \frac{1}{125} \sin(5\omega t) - \frac{1}{343} \sin(7\omega t) + \ldots
\]

IV. THE PROPOSED CCC METHODOLOGY FOR THE DPC

The CCC for the DPC is achieved by adding the proposed CCC to the conventional controller, as shown in Fig. 6. When the current reference \( i_{0x}^{\prime\prime} \) of the proposed CCC is set to zero, the proposed CCC generates the zero-sequence modulation compensation signal \( d_{0\alpha\text{com}} \) to be combined with the conventional modulation signals of phases \( a \), \( b \), and \( c \) in \( d_{ax}, d_{bx}, \) and \( d_{cx} \), respectively, to create the new modulation signals in \( d_{ax}, d_{bx}, \) and \( d_{cx} \), respectively. As a result, the zero-sequence modulation signal is modified by the proposed CCC according to Eqs. (20) and (21). To compensate for the zero-sequence modulation signals of the other converters, the magnitudes are equal and in phase. As a result,
the circulating current of the DPC is zero.

\[ d_{0cx} = \frac{1}{3} (d_{ax} + d_{0comx} + d_{bx} + d_{0comx} + d_{cx} + d_{0comx}) \]
\[ = \frac{1}{3} (d_{ax} + d_{bx} + d_{cx}) + d_{0comx} \quad (20) \]
\[ d_{0cx} = d_{0x} + d_{0comx} \quad (21) \]

The zero-sequence modulation compensation signal \( d_{0comx} \) needs to compensate the waveform at a frequency of 150 Hz. The PI controller is not able to respond to this frequency due to the limitations of the bandwidth. Therefore, this paper proposes new transformation techniques that are able to use the PI controller to control the circulating current \( i_{0x} \). These techniques are presented in the next subsection.

### A. CIRCULATING CURRENT APPROXIMATION AND TRANSFORMATION

This paper focuses on a three-phase balance system. When the symmetrical component method is applied to the converter currents, the components are divided into positive and zero-sequence components. In general, the transformation matrix is used to transform the stationary reference frame to the synchronous reference frame at the grid frequency while transforming only the positive sequence components into the \( d \)- and \( q \)-axes to control the active power and reactive power, respectively. However, the zero-sequence component is not transformed and controlled. To completely control the circulating current, the \( \theta \)-axis current, which is the circulating current, must be transformed in the \( 0d \)- and \( 0q \)-axes, but there are two problems with this transformation, which are that 1) the circulating current Eq. (18) is nonsinusoidal and that 2) the circulating current \( i_{0x} \) has only one signal.

From Eq. (19), it is clear that the circulating currents consist of the sum of many odd harmonic currents. To completely control the circulating current, the many harmonic currents must be controlled. Hence, many bandpass filters (BPFs) must be designed to separate the signals of these harmonic currents. Then, the various odd harmonic currents must be transformed to the \( 0d \)- and \( 0q \)-axes. Subsequently, a controller must be designed to completely control the current at each harmonic order. Due to the many BPFs and controllers that must be designed, it is difficult to carry this operation out in practice. To reduce the complexity of the CCC system, this paper estimates the circulating current in a simple form. From Eq. (18), the coefficient for the fundamental harmonic current is very high relative to the others. By using the coefficient of the fundamental harmonic current as of the base value, the coefficients of the 1\(^{\text{st}}\), 3\(^{\text{rd}}\), 5\(^{\text{th}}\), and 7\(^{\text{th}}\) harmonic currents can be computed in PU, as shown in Table 1. The magnitude of the fundamental harmonic current is very high compared with those of the other harmonic currents. Therefore, the circulating current \( i_{0x} \) can be estimated by using the fundamental harmonic current component, as shown in Eq. (22). The approximate circulating current \( \dot{i}_{0x} \) in Eq. (22) is represented by a sinusoidal function that has a frequency of 150 Hz.

\[ \dot{i}_{0x} \approx I_s \sin (\omega_3 t) \quad (22) \]

| Harmonic Order | Coefficient (PU) |
|----------------|------------------|
| 1\(^{\text{st}}\) | 1.0000 |
| 3\(^{\text{rd}}\) | -0.0370 |
| 5\(^{\text{th}}\) | 0.0080 |
| 7\(^{\text{th}}\) | -0.0029 |

The final problem facing the transform is that there is only one circulating current signal, which can be found with Eq. (22). The transformation block diagram from \( x(t) \) to the \( x_d \)- and \( x_q \)-axes is created by using the input signal \( x(t) \) as \( x_\alpha \) and shifting the phase of the input signal \( x(t) \) to 90\(^{\circ} \) to obtain the second signal \( x_\beta \) and is shown in Fig. 7. Then, \( x_\alpha \) and \( x_\beta \) are transformed to \( x_{0d} \) and \( x_{0q} \), respectively, by using Eq. (23).

\[ \begin{bmatrix} x_d \\ x_q \end{bmatrix} = T_{\alpha\beta}/d_q \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \quad (23) \]

### B. PROPOSED CIRCULATING CURRENT MODEL

Using the \( \theta \)-axis model on the lower right-hand side of Fig. 2 and Eq. (22), the \( \theta \)-axis model can be rewritten as shown in Fig. 8. The approximate circulating current signal has a sinusoidal form with a frequency of 150 Hz. The signal is constantly changing, making the design of the controller difficult. Therefore, to simplify the design of the circulating current controller, the transform technique shown in Fig. 7 is used to create a new model on the \( 0d \)- and \( 0q \)-axes and then to design the circulating current controller.

Using Fig. 8, the voltage equation \( v_0 \) can be written as follows:

\[ v_0 = d_{0x} v_{dc} - L_x \frac{d \dot{i}_{0x}}{dt} \quad (24) \]

Using the phase shift technique to shift the signal in Eq. (24) 90\(^{\circ} \) moves the signals on the \( \alpha \)- and \( \beta \)-axes as shown in Eq. (25).

\[ \begin{bmatrix} v_{0ax} \\ v_{0bx} \end{bmatrix} = \begin{bmatrix} d_{0ax} \\ d_{0bx} \end{bmatrix} \cdot v_{dc} - L_x \frac{d}{dt} \begin{bmatrix} i_{0ax} \\ i_{0bx} \end{bmatrix} \quad (25) \]
The proposed circulating current circuit model in the $0d$- and $0q$-axes.

FIGURE 9. The proposed circulating current circuit model in the $0d$- and $0q$-axes.

FIGURE 10. The proposed circulating current model.

Premultiplying Eq. (23) by $T_{αβ/dq}^{-1}$ results in Eq. (26).

\[
\begin{bmatrix}
    x_d \\
    x_q
\end{bmatrix} = T_{αβ/dq}^{-1} \begin{bmatrix}
    x_d \\
    x_q
\end{bmatrix} = \begin{bmatrix}
    \cos \theta & -\sin \theta \\
    \sin \theta & \cos \theta
\end{bmatrix} \begin{bmatrix}
    x_d \\
    x_q
\end{bmatrix}
\]  

(26)

Using Eq. (26), Eq. (25) can be rewritten as shown in Eq. (27).

\[
L_x \frac{d}{dt} \left( T_{αβ/dq}^{-1} \begin{bmatrix}
    0_d \\
    0_q
\end{bmatrix} \right) = T_{αβ/dq}^{-1} \begin{bmatrix}
    d_0_d \\
    d_0_q
\end{bmatrix} \cdot v_{dc} - T_{αβ/dq}^{-1} \begin{bmatrix}
    v_{0d} \\
    v_{0q}
\end{bmatrix}
\]

(27)

\[
L_x \left( T_{αβ/dq}^{-1} \frac{d}{dt} \begin{bmatrix}
    0_d \\
    0_q
\end{bmatrix} + \left( \frac{d(T_{αβ/dq}^{-1})}{dt} \right) \begin{bmatrix}
    0_d \\
    0_q
\end{bmatrix} \right) = T_{αβ/dq}^{-1} \begin{bmatrix}
    d_0_d \\
    d_0_q
\end{bmatrix} \cdot v_{dc} - T_{αβ/dq}^{-1} \begin{bmatrix}
    v_{0d} \\
    v_{0q}
\end{bmatrix}
\]

(28)

Now, we premultiply Eq. (28) by $T_{αβ/dq}$ to arrive at:

\[
L_x \left\{ \frac{d}{dt} \begin{bmatrix}
    0_d \\
    0_q
\end{bmatrix} + T_{αβ/dq} \left( \frac{d(T_{αβ/dq}^{-1})}{dt} \begin{bmatrix}
    0_d \\
    0_q
\end{bmatrix} \right) \right\} = \begin{bmatrix}
    d_0_d \\
    d_0_q
\end{bmatrix} \cdot v_{dc} - \begin{bmatrix}
    v_{0d} \\
    v_{0q}
\end{bmatrix}
\]  

(29)

By substituting $\omega_3 t$ for the $\theta$ of $T_{αβ/dq}$ and $T_{αβ/dq}^{-1}$ in Eq. (29), we obtain Eq. (30):

\[
L_x \frac{d}{dt} \begin{bmatrix}
    0_d \\
    0_q
\end{bmatrix} = \begin{bmatrix}
    d_0_d \\
    d_0_q
\end{bmatrix} \cdot v_{dc} + L_x \begin{bmatrix}
    0 & -\omega_3 \\
    \omega_3 & 0
\end{bmatrix} \begin{bmatrix}
    0_d \\
    0_q
\end{bmatrix} - \begin{bmatrix}
    v_{0d} \\
    v_{0q}
\end{bmatrix}
\]

(30)

Eq. (30) can then be used to construct the new model of the circulating current in the $0d$- and $0q$-axes, as shown in Fig. 9.

Replacing the model in the $0$-axis in Fig. 2 with the proposed circulating current circuit model in Fig. 9 results in Fig. 10. As seen in Fig. 10, this model consists of three main parts:

1) There is a DC bus circuit on the left-hand side that is connected to the load or source.

2) The positive sequence components of $d$- and $q$-axes circuits are in the middle and connected to the grid voltage. The $d$- and $q$-axes components are used to control the active power and reactive power via the currents $i_{0d}$ and $i_{0q}$, respectively.

3) The zero-sequence components of the $0d$- and $0q$-axes circuits are on the right-hand side; both circuits are open circuits. These $0d$- and $0q$-axes circuits are used to design the proposed circulating current controller. Note that this model uses a frequency of 150 Hz in the transformation.

C. PROPOSED CCC DESIGN METHODOLOGY

The proposed CCC model of the PWM converter in Fig. 10 is used to design the circulating current controller shown below in Fig. 11. The controller in Fig. 11 has two parts: the first part is the conventional controller, which is shown at the top of the figure and is used to control the active power and reactive power, and the second part is the proposed circulating current controller, which is shown on the bottom of Fig. 11 and is designed from the proposed circulating current circuit model of the $0d$- and $0q$-axes shown on the right-hand side of Fig. 10. The controller is added to the conventional controller to eliminate the circulating current $i_{0x}$.

This CCC system measures the current of each phase, namely, $i_{acx}$, $i_{bcx}$, and $i_{ccx}$, to calculate the circulating current $i_{0x}$ according to Eq. (7), then estimates the circulating current $i_{0x}$ according to Eq. (22). The BPF is used to separate the fundamental frequency of the circulating current. The current $i_{0x}$ is sinusoidal and has a frequency of 150 Hz. Due to the current $i_{0x}$, there is only one signal. Hence, the phase shift technique is used to construct the second current signal $i_{0βx}$ and then to transform the currents $i_{acx}$ and $i_{bcx}$ into $i_{0dx}$ and $i_{0gx}$, respectively. The relationship between the two currents follows Eq. (30). Eq. (31) includes the cross-coupling between the $0d$- and $0q$-axes. The decoupling between the two axes is accomplished by designing a voltage-decoupling controller, which is shown in the shaded area in Fig. 11. The
reference currents $i_{d_{01}}$ and $i_{d_{02}}$ are set to zero, and hence, the output signals from this controller are $d_{\text{cont1}d_{01}}$ and $d_{\text{cont2}d_{02}}$, then, $d_{\text{cont1}d_{01}}$ and $d_{\text{cont2}d_{02}}$ are transformed into $d_{\text{com1}d_{01}}$ and $d_{\text{com2}d_{02}}$. The signal $d_{\text{commax}}$ is used to compensate the signals $d_{ax}$, $d_{bx}$, and $d_{cx}$ in the SVPWM block diagram, where the signal $d_{\text{commax}} = d_{\text{commax}}$, and the control signal $d_{\text{commax}}$ is combined with the modulation signals $d_{ax}$, $d_{bx}$, and $d_{cx}$ as in Eq. (20) to completely control the circulating current.

V. SIMULATION RESULTS

To verify the performance of the proposed CCC, a case study is conducted by using two directly parallel converters, one with a conventional controller and the other with the proposed CCC, and comparing their responses to various currents. By varying the currents, we can observe and compare the converter currents, grid currents, circulating currents, the modulation signals of phase $a$, and the zero-sequence modulations.

By setting the 1st converter’s supply current to 8 A and the 2nd converter’s supply current to 2 A (see Fig. 12(a)), we can show the responses of the conventional converters. The top of the figure shows phase $a$ of the grid current (purple line), the 1st converter current (brown line), and the 2nd converter current (blue line). The bottom of the figure shows the circulating current (green line). Fig. 12(b) provides the same information for the proposed CCC.

VI. EXPERIMENTAL RESULTS

To verify the performance of the proposed CCC system in terms of eliminating the circulating current, a DPC experimental system with three PWM converters is constructed.
as shown in Fig. 13. The diagram consists of PWM converter 1, PWM converter 2, and PWM converter 3, which are directly parallel. Each converter consists of a DC bus capacitor, H-bridge insulated-gate bipolar transistors (IGBTs), filter inductors, voltage and current sensors with a signal conditioner, a microcontroller unit (MCU) board implemented with a TMS320F28379D, a gate drive, and a magnetic contactor. The test system and the test parameters of the electrical system and the PWM converter parameters are shown in Fig. 14 and Table 2, respectively. In practice, the measurement of circulating current $i_0$ is achieved by taking the sum of the phase currents $i_{ac1}$, $i_{ac2}$, and $i_{ccx}$ using a current probe, meaning that the measured value is $3i_0$; that is, the oscilloscope shows $3i_0$ instead of $i_0$.

A. BEHAVIOR AND PERFORMANCE OF THE PROPOSED CCC SYSTEM

To examine the control performance of the proposed CCC system, the test system is configured so that the converters are directly parallel, as shown in Fig. 13. Two of the converters are used in two experiments. The first experiment is done in the same manner as the simulation in section IV and is designed to assess the steady state behavior and control performance. The second experiment uses stepping and ramping of the converter current during directly parallel activities to examine the dynamic behavior of the proposed CCC system.

1) STEADY-STATE BEHAVIOR

The testing of the two converters is conducted under two sets of conditions. In the first case, there is balanced current sharing, with both converters supplying $i_{ac1} = i_{ac2} = 8\text{ A}_{\text{rms}}$ to the grid. In the second case, there is unbalanced current sharing, and the converters supply, $i_{ac1} = 8\text{ A}_{\text{rms}}$ and $i_{ac2} = 2\text{ A}_{\text{rms}}$ to the grid. In both cases, the signals are measured. The test results are as follows.

Fig. 15 shows the responses of the two PWM converters in case 1. Fig. 15(a) and (c) shows the responses of the conventional converters, and Fig. 15(b) and (d) shows the responses of the proposed circulating current-controlled converters. In Fig. 15(a), the currents in phase $a$ for the two converters, namely, $i_{ac1}$ and $i_{ac2}$, and the phase $a$ current of the grid $i_a$ are sinusoidal. The current $i_a$ is the sum of the currents $i_{ac1}$ and $i_{ac2}$. The circulating current $3i_0$ should not occur with balanced current sharing, but in the figure, $3i_0 = 0.726\text{ A}$. Circulating currents occur in practice because $d_{01}$ and $d_{02}$ are slightly different because the parameters of the two converters are slightly different. Fig. 15(b) records the responses to the test conditions in Fig. 15(a) using the proposed circulating current-controlled converters. The currents $i_{ac1}$, $i_{ac2}$, and $i_a$ are nearly the same as those in Fig. 15(a), but the circulating current decreases from 0.726 A to 0.646 A.

Fig. 15(c) and (d) shows the zero-sequence modulation signals $d_{01}$ and $d_{02}$ and the modulation signals for phase $a$, namely, $d_{a1}$ and $d_{a2}$ of the conventional converters and the proposed circulating current-controlled converters, respectively. In Fig. 15(c) and (d), the zero-sequence modulation signals $d_{01}$ and $d_{02}$ are slightly different, as are the modulation signals for phase $a$, namely, $d_{a1}$ and $d_{a2}$. As a result, the $0$-axis voltages generated by the converters are almost the same. Hence, a small circulating current flows between the converters.

Fig. 16 shows the responses of the two directly parallel converters when the currents are unbalanced; that is, $i_{ac1} = 8$...
A and $i_{ac2} = 2$ A. Fig. 16 shows the responses of the two directly parallel converters when the currents are unbalanced; that is, $i_{ac1} = 8$ A and $i_{ac2} = 2$ A. Fig. 16(a) and (c) shows the response of the DPC using conventional control, and Fig. 16(b) and (d) shows the response of the proposed circulating current-controlled DPC. In Fig. 16(a), when the two currents are unbalanced, the circulating current is $3i_0 = 5.27$ A because the zero-sequence modulation signals $d_{01}$ and $d_{02}$ have unequal amplitudes and phases, as shown in Fig. 16(c). As a result, the phase $a$ currents of the two converters $i_{ac1}$ and $i_{ac2}$ are distorted by the sinusoidal waveform (which causes the inductors $L_1$ and $L_2$ to vibrate abnormally) and have values of 8.53 A and 2.59 A, respectively. The sum of the currents of the two converters combined into the grid current $i_{ac}$ is still sinusoidal because the circulating current cannot flow to the grid because the grid is a three-phase, three-wire system. In Fig. 16(b), the converter currents $i_{ac1}$ and $i_{ac2}$ are sinusoidal, and when these currents are combined into the grid current $i_{ac}$, the resulting current is still sinusoidal. The circulating current $3i_0$ decreases from 5.27 A in Fig. 16(a) to 0.87 A due to the proposed CCC generated compensation signal, which, combined with the modulation signal for phase $a$ of the 2nd converter $d_{a2}$, causes the modulation signal $d_{a1}$ to be distorted from the modulation signal $d_{a1}$, as shown in Fig. 16(d). As a result, the signals $d_{01}$ and $d_{02}$ overlap, but at the peak of either signal they are unequal because the proposed CCC is designed to control the system at a frequency of 150 Hz. Consequently, the voltages of the converters generated in the $d$-axis are almost the same. Therefore, the circulating current decreases to almost zero, and the inductors $L_1$ and $L_2$ vibrate normally compared to their performance in the conventional converters.

2) DYNAMIC RESPONSE TO STEPPED CURRENT SHARING

Fig. 17 shows the stepped current responses of the two directly parallel converters, which are created by disconnecting the 1st converter and connecting it at time $t_1$ at a stepped current of $i_{ac1} = 2$ A and allowing the 2nd converter to supply a constant current $i_{ac2} = 8$ A. Fig. 17(a) shows the currents $i_{ac1}$, $i_{ac2}$, $i_a$ and $3i_0$ of the conventional converter. Before $t_1$, $i_a$ and $i_{ac2}$ are sinusoidal, and the circulating current $3i_0$ is zero. At time $t_1$, the current $i_{ac1}$ is stepped, and $i_a$ is still sinusoidal; however, $i_{ac1}$ and $i_{ac2}$ are distorted by the sinusoidal influence, and the circulating current $3i_0$ is 5.27 A with an overshoot of 12 A. Fig. 17(b) shows the same response as that in Fig. 17(a) but for the proposed circulating current-controlled converters. Before $t_1$, $i_a$ and $i_{ac2}$ are sinusoidal, and the circulating current $3i_0$ is zero. At time $t_1$, a current of $i_{ac1} = 2$ A is stepped, $i_{ac1}$, $i_{ac2}$, and $i_a$ are still sinusoidal, and the proposed CCC system can keep the circulating current near zero.

Fig. 18 shows the step current responses of the two directly parallel converters created by setting the 1st converter up to supply a constant current $i_{ac1} = 2$ A. The 2nd converter is disconnected and at time $t_1$ reconnected at a stepped current of $i_{ac2} = 8$ A. The response in this case is similar to the response in the first case, but the overshoot of the circulating current has a peak value of approximately 9 A and achieves a steady state within 60 ms at $t_2$, as shown in Fig. 18(b).

3) RESPONSE CAPABILITY WITH RAMP CURRENT SHARING

Fig. 19 shows the ramp current responses of the two directly parallel converters created by setting the 1st converter’s supply current $i_{ac1} = 8$ A and having the 2nd converter supply current ramp up from 0 A to 8 A then down from 8 A to 0 A with slopes of ± 8 A/s. The proposed circulating current-controlled converters can almost completely control the circulating current $3i_0$ throughout the operating range, as shown in Fig. 19(b). In the case of conventional control,
\(3i_0\) increases when the currents \(i_{ac1}\) and \(i_{ac2}\) are less similar, as shown in Fig. 19(a).

**B. OPTIMIZATION OF THE DPC USING THE PROPOSED CCC**

To verify the control performance and the optimization of the DPC using the proposed CCC, the full experimental setup with three PWM converters (Fig. 13) is tested. Fig. 20 shows the responses of the DPC during unbalanced current sharing. Here, the 1\(^{st}\) converter’s supply \(i_{ac1} = 8\) A, the 2\(^{nd}\) converter’s supply \(i_{ac2} = 6\) A, and the 3\(^{rd}\) converter’s supply \(i_{ac3} = 2\) A. The current values at each converter are set before they are configured directly parallel.

Fig. 20(a) shows the circulating currents of the conventional system. Here, \(3i_0\)\(_{1}\), \(3i_0\)\(_{2}\), and \(3i_0\)\(_{3}\) are 4.32 A, 2.80 A, and 6.06 A, respectively. From the figure, the circulating current that flows through the converter supplying the smallest current is the highest. This current is equal to the circulating currents from the other two converters combined but flows in the opposite direction. Fig. 20(b) has the same setup as Fig. 20(a), but the proposed CCC is used. Here, \(3i_0\)\(_{1}\), \(3i_0\)\(_{2}\), and \(3i_0\)\(_{3}\) are reduced to 1.29 A, 0.907 A, and 0.808 A, respectively. With three directly parallel converters, the proposed CCC can still nearly completely control the circulating current.

The efficiency of the proposed CCC system is determined by measuring the power while three directly parallel converters operate and supply currents of 8 A, 6 A and 2 A, respectively. The input power is measured at the DC bus, and the output power is measured at the grid. Comparative tests between the proposed CCC converters and the conventional converters are conducted. The measurement results and efficiency calculations are shown in Table 3. From the table, the total efficiency of the proposed CCC system is higher than that of the conventional system by 1.12%. The total power loss of the proposed CCC system is 620 W (the 1\(^{st}\), 2\(^{nd}\) and 3\(^{rd}\) converters have losses of 310, 220 and 90 W, respectively), and the total power loss of the conventional system is 730 W (the 1\(^{st}\), 2\(^{nd}\) and 3\(^{rd}\) converters have losses of 340, 240 and 150 W, respectively).

Table 4 shows the efficiency of a single PWM converter used in the experiment with currents supplied in different ranges. When the 1\(^{st}\), 2\(^{nd}\) and 3\(^{rd}\) converter supply currents are 8, 6 and 2 A, respectively, the efficiencies are 93.14\%, 93.47\% and 92.10\%, respectively, of those of the system (Table 3). The converters have the same efficiencies. Thus, the proposed CCC system can nearly completely control the circulating currents of converters that are directly parallel and does not reduce the efficiencies of the converters, as is the case with the conventional controller. The DPC system works as if only one converter was connected.

**VII. CONCLUSION**

This paper presented a method for eliminating the circulating current in a DPC based on the compensation modulation signal technique used in the SVPWM. Using an analysis of the circulating current carried out on an equivalent circuit model in the \(0\)-axis, it was discovered that the circulating current occurs because the zero-sequence modulation signals of the converters are unequal in both amplitude and phase. To design the proposed CCC system, the circulating current components of the circulating current were analyzed via a Fourier series. It was found that the circulating current can be estimated with the fundamental harmonic current of 150 Hz. Next, the \(0\)-axis model of the converters was transformed to the \(0d\)- and \(0q\)-axes using the proposed transformation. Then, a controller was designed to control the circulating current by forcing the zero-sequence modulation signals of the converters to be identical. To examine the performance of the proposed CCC system, a DPC system was constructed using three 5.5 kVA PWM converters, and current sharing was tested under various conditions. The steady-state behavior...
of the conventional system showed that a circulating current occurs when there is an unbalanced current. As a result, the current of each converter is distorted due to the sinusoidal influence, causing the inductors to exhibit abnormal noise and vibrations. When the proposed CCC system was used, the zero-sequence modulation signals could be held at the same value, resulting in a circulating current of nearly zero. Any remaining circulating current when the proposed CCC was in use was controlled at the fundamental harmonic frequencies, so the circulating currents remained at the 3rd, 5th, ... harmonic frequencies. As a result, the currents for each converter were nearly sinusoidal, and the inductors operated normally. The step responses of the proposed CCC system were quick to eliminate the circulating current caused by the step current; as a result, it was possible to instantly connect the proposed CCC converters to or disconnect them from the DPC system.

In addition, the ramp response test confirmed that the proposed CCC system can nearly completely control the circulating current throughout the operating range. Moreover, the overall efficiency of the proposed CCC system was significantly higher than that of the conventional system. If there is suitable management of current sharing through keeping each converter operating in its highest efficient range, then the proposed CCC system will be at its most effective throughout the operating range. This approach utilizes only software, so it is inexpensive, and the optimized converters can be chosen to reduce cost and increase efficiency.

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