ATLAS LAr calorimeters readout electronics upgrade
R&D for sLHC

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Abstract. The ATLAS Liquid Argon (LAr) calorimeters consist of an electromagnetic barrel calorimeter and two end-caps with electromagnetic, hadronic and forward calorimeters. A total of 182,468 signals are digitized and processed real-time on detector, to provide energy and time deposited in each detector element at every occurrence of the Level-1 trigger. A luminosity upgrade of the LHC will occur in the years ~2020. The current readout electronics will need to be upgraded to sustain the higher radiation levels. A completely innovative readout scheme is being developed. The front-end readout will send out data continuously at each bunch crossing through high speed radiation resistant optical links, the data will be processed real-time with the possibility of implementing trigger algorithms. This article is an overview of the R&D activities and architectural studies the ATLAS LAr Calorimeter Group is developing.

1. Introduction
The ATLAS experiment [1] is a general-purpose detector designed to study the proton-proton collisions produced at the Large Hadron Collider (LHC) with a center-of-mass energy of 14 TeV and to explore the full physics potential of the LHC at CERN.

![Figure 1. Schematic drawing of the ATLAS LAr calorimeters](image)

Liquid Argon (LAr) calorimeters [2] in ATLAS are high precision, high sensitivity and high granularity detectors designed to provide precision measurements of electrons, photons, jets and...
missing transverse energy. The LAr calorimeters consist of four sub-detectors and are contained within three cryostats between the inner tracking detectors and the outer muon chambers as shown in Figure 1. The central cryostat houses the electromagnetic barrel calorimeter (EMB) which covers the pseudo-rapidity range $0 < |\eta| < 1.475$, while each end-cap cryostat contains an end-cap electromagnetic calorimeter (EMEC) which covers $1.375 < |\eta| < 3.2$, two hadronic end-cap wheels (HEC) covering $1.5 < |\eta| < 3.2$ and a three wheels forward calorimeter (FCAL) which covers the region very close to the beam axis ($3.1 < |\eta| < 4.9$) to achieve large acceptance.

2. Readout Electronics of LAr Calorimeters

![Figure 2. LAr calorimeters readout electronics architecture](image)

The readout electronics architecture of LAr calorimeters is depicted in Figure 2. When a charged particle traverses and ionizes the liquid Argon in the gap between a LAr electrode and an absorber, an ionization current signal is preamplified, shaped, buffered and digitized by the front-end boards (FEB) [3] installed on the detector. The FEBs send the digitized pulse via optical links to the Readout Drivers (ROD) which are installed in a radiation free area (USA15) next to the detector cavern (UX15). In total 182,468 calorimeter cells are to be read out. Each ROD receives the data from up to 8 FEBs and calculates the energy deposited, the time of the deposition and a quality factor for cells with high energy deposit, using an optimal filtering algorithm [4]. RODs send data to the Readout Buffers (ROBs) hosted on PCs (ROS) through S-links. Analog trigger sum signals are formed on front-end electronics boards and sent to the receiver system through copper cables before interface to the Level-1 calorimeter trigger.
(L1Calo) system. The LAr calorimeters front-end electronics system [5] is installed on detector and includes 58 Front End Crates (FEC) which house 1,524 FEBs and other electronics boards. The back-end electronics system [6] consists of 16 back end crates and 68 ROS PCs, and there are total 192 RODs plugged in back end crates.

3. Motivations of Readout Electronics Upgrade

LHC is expected to be upgraded in two phases. Phase 1 is planned in 2016 and phase 2 is planned in 2020 which is also known as super-LHC (sLHC). sLHC will have 10 times luminosity and the current LAr front-end electronics need to be upgraded to sustain the higher radiation levels [7]. The present front-end architecture is very complex. A FEB has 11 ASICs based on different technologies, some of which (e.g. DMILL) are already obsolete. The FEB is designed and produced for 10 years operation with limited number (∼6%) of spares, it has also intrinsic limitations on Level-1 trigger acceptance. Therefore component level upgrade is not possible, and a new front-end architecture has been proposed as shown in Figure 3.

![Figure 3. Proposed front-end readout architecture of LAr calorimeters](image)

The new front-end readout will send out data continuously at each bunch crossing through high speed radiation resistant optical links. Large volume of data (∼100Gbps each board) will be processed real-time with the possibility of implementing trigger algorithms for clusters and electron/photon identification at a finer granularity than what is currently implemented. The new architecture simplifies the system design while keeping many options open, such as pipeline design, shaping and gain settings etc. It requires many R&D efforts and the following section describes these R&D activities for LAr calorimeters readout electronics upgrade.

4. R&D Studies of Readout Electronics Upgrade

4.1. Front-end ASIC Design

Front-end electronics design for sLHC becomes more critical with requirements of both high performance and higher radiation levels. Three R&D efforts are going on which are focused on the analog front-end and mixed-signal front-end ASIC design.

4.1.1. Analog Front-end ASIC

An analog front-end chip LAPAS (Liquid Argon PreAmplifier Shaper) has been designed and received in early 2009. It uses IBM 8WL 0.13 µm SiGe (silicon-germanium) BiCMOS technology. The preamplifier design of LAPAS chip is based on low noise line-terminating circuit topology presently used in LAr calorimeters. It has full 16-bit dynamic range and very low noise (∼0.26nV/√Hz). The shaper design of LAPAS chip is fully differential and based on $CR - (RC)^2$ topology with two gain settings (×1 and ×10). The uniformity is better than 5% across 17 tested ASICs, the INL (integral non-linearity) over full scale of two gains is less than 0.1%.

The LAPAS chip has been tested with hand wired prototype board, all measurements are as expected. The TID (total ionization dosage) test results show no significant concern. A new test
print circuit board shown in Figure 4 is available. The full characterization is still in progress. The future plan is to explore SiGe technologies from different manufactures (e.g. IHP, AMS) and study the feasibility of CMOS only design.

![Figure 4. Test print circuit board with LAPAS chip populated](image1.png)

Figure 4. Test print circuit board with LAPAS chip populated

![Figure 5. Layout and package of Nevis09 chip](image2.png)

Figure 5. Layout and package of Nevis09 chip

4.1.2. Mixed-signal Front-end: ADC  ADC is the most technologically challenging component in the new architecture due to the requirements of high dynamic range, radiation tolerance and SEE (single event effects) immunity. Some commercial ADCs (e.g. ADI-AD9259, ST-RHF1201 and TO-ADC5821) have been identified and planned to be tested in radiation environment, while a custom ADC is being developed.

The Nevis09 chip has been designed and received in late 2009. The layout and package of the chip is shown in Figure 5. It uses IBM 8RF 0.13 µm CMOS technology to implement 12-bit precision OTA (operational transconductance amplifier) with cascade of two T/H (track-and-hold) to achieve S/H (sample-and-hold) effect for testing. The preliminary test results show the circuit could reach 65dB, the full characterization test is still ongoing.

4.1.3. HEC Cold Electronics  The HEC preamplifier and summing boards (PSB) are located at the perimeter of the HEC wheels inside the liquid Argon. The ASIC on PSB is designed and built by Gallium-Arsenide (GaAs) TriQuint QED-A 1 µm technology[8]. The present ATLAS requirements for the HEC PSB boards are $2 \times 10^{12} \text{n/cm}^2$ per year. After 10 years of LHC operation, the present HEC cold electronics would be operated at its limit. It is therefore planned to develop a new ASIC that will be ten times more radiation hard against neutrons.

| Material | SiGe | SiGe | SiGe | Si | Si | GaAs | GaAs |
|----------|------|------|------|---|---|------|------|
| Transistor | Bipolar | Bipolar | Bipolar | CMOS | CMOS | CMOS | FET |
| Foundry Type | IHP | IBM | AMS | IHP | IHP | AMS | TriQuint |
| 10 MHz | 5% | 5% | 5% | 4% | 4% | 3% | 0% |
| 40 MHz | 3% | 2% | 5% | 2% | 3% | 3% | 2% |

The radiation hardness against neutron irradiation has been studied for transistors of SiGe, Si and GaAs technologies. The loss of gain for the transistors for two different frequencies, studied
at a neutron fluence of $2 \times 10^{15} \text{n/cm}^2$ is shown in Table 1. All technologies investigated show only a small degradation of the gain up to the irradiation level expected for sLHC. Based on these studies both options, bipolar SiGe as well as CMOS FET technologies, are sufficiently stable under neutron irradiation and are being investigated further. A first design of amplifier based on IHP SGB25V CMOS technology will be available for test in Sept 2010, while a similar design based on IBM 8RF CMOS technology is planned to be done in late 2010.

4.2. Radiation Resistance Optical Link
The new readout architecture requires high bandwidth radiation resistant optical link to transmit data out of the detector. The SMU_P1 chip based on 0.25 µm Silicon on Sapphire CMOS technology has been received in late 2009. It includes a 5Gbps 16:1 serializer, a 5GHz LC VCO based PLL, the CML driver, a divide-by-16 circuit, a varactor and an SRAM block. The full characterization test is still ongoing. The preliminary test results show the serializer works in the range of 3.8 to 6.2Gbps with $\sim 507 \text{mW}$ power consumption. The tuning range of the LCPLL is 4.7 to 5GHz, the power consumption at 4.9GHz is $\sim 121 \text{mW}$, the random jitter is less than 2.5ps and the deterministic jitter is less than 17ps.

4.3. Back-end High-speed Processing Unit
The ROD is the heart of the back-end electronics system, serving as the bridge between the front-end electronics system, the ROS and possibly the L1Calo system. With the new front-end architecture, ROD will have to be upgraded to process huge amount of data ($\sim 1.5 \text{Tbps per board}$) from the detector. A possible implementation, currently under study, of the ROD board is shown in Figure 6.

![Figure 6. Schematic representation of the LAr signal dataflow](image)

A SubROD and a SubROD Injector based on ATCA platform have been developed and shown in Figure 7 and 8, the integration test was performed in Oct 2009. They use commercial parallel optical transceiver running at 75Gbps with MPO®/MTP low profile connector, SERDES of Xilinx Virtex-5 FPGA and Altera Stratix II GX FPGA are tested successfully.

The feasibility of fast and large volume data preparation within fixed latency budget for Level-0 and Level-1 trigger upgrade is being investigated. The data volume is expected to be 40Tbps for L0Calo processing and 2Tbps for L1Calo processing. The other R&D studies related to ROD, such as IPMI (Intelligent Platform Management Interface) controller, interface to ROS over 10Gbit Ethernet and software development, are also being performed.
4.4. Low Voltage Power Supply

The current front-end power supply system is of centralized architecture with each FEC having its own LVPS which takes 280V input from USA15 through \(\sim 100\) m cable and provides seven different voltages. A LVPS has high power density (\(\sim 3.2\) kW) and is water cooled. The new LVPS will have to sustain higher radiation levels, even though total power budget of front-end electronics will be kept same. The number and levels of voltages have to be rationalized, to reduce different voltages across devices. Two possible LVPS architectures, distributed power architecture and intermediate bus architecture, are being investigated.

5. Summary

Radiation levels and probably natural aging will require an upgrade of the ATLAS LAr calorimeters front-end electronics for sLHC. A new front-end readout architecture has been proposed and is being developed for the readout electronics upgrade. The upgrade R&D projects are progressing smoothly and more test results are expected in the near future. The feasibility of the readout architecture is expected to be demonstrated in next 2-3 years.

References

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