Error factors of AC-DC conversion circuits accuracy

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Abstract: Voltage standard source is an important basic instrument in the electrical measurement and testing field, and it has important guarantee significance for many industries. AC voltage standard source is based on AC-DC conversion technology to achieve output function of high precision AC voltage. In order to get a better effect of AC-DC conversion, the three factors—operational amplifier, resistance and diode—that have a greater impact on the accuracy of the rectifier output were taken the research object, and their impacts on the circuit error were analyzed respectively. The output result was compared with the output of full wave precision rectification circuit under ideal state, and the scheme of reducing error in the precision rectifier circuit was summarized, which provides a reference for improving the accuracy of AC-DC conversion in the design of full wave rectifier circuit.

1. Introduction
As an important part of precision instrumentation, AC-DC conversion circuits are mostly used in signal generators, multifunctional standard sources, voltmeter and various signal processing circuits[1]. Taking the AC voltage standard source as an example: the output voltage of the source converts DC voltage through the AC-DC conversion circuit in the feedback loop. When it changes, the feedback DC voltage can be compared with the DC reference to calibrate the error[2]. The current methods to achieve AC-DC conversion are mainly divided into: thermoelectric conversion method[3], digital sampling method[4] and analog rectification method[5][6] and so on, among which the rectification circuit scheme is widely used for its simple structure and faster speed.

The precision rectifier circuit uses the combination of diodes and operational amplifiers (op-amps) to reduce the effect of forward voltage when the diode is turned on, but it still faces two problems: the high requirement of the resistance matching degree and the distortion of the signal near the zero point. In order to investigate the causes of these problems, this paper calculates and analyzes the three main circuit parameters—operational amplifier, resistance, and diode—that affect the output accuracy. After finding the sources of the errors, the corresponding solution can be made from influencing factors such as components selection and resistance matching.

2. Principle of full-wave rectifier circuit
The full-wave rectifier circuit is generally made up of resistances, op-amps and diodes[7], the circuit is shown in figure 1.
In the simple rectifier circuit or bridge rectifier circuit, the transmit characteristic is limited by the diodes forward voltage regardless of whether silicon or germanium diodes are used, which can cause the large deviations for weak input signals, the above two circuits are generally suitable for circuits with low accuracy AC-DC conversion. In contrast, diodes which in the full-wave rectification circuit are placed in the feedback loop, and the effect of the diode's forward voltage on the output is suppressed due to deep negative feedback mode. Op-amp A1 realizes half-wave rectification, A1 and A2 both realize full-wave rectification. Ideally, the output of this circuit can be described by

\[ u_o = \begin{cases} \frac{R_f}{R_1 R_2} u_i, & u_i > 0 \\ -\frac{R_f}{R_4} u_i, & u_i < 0 \end{cases} \] (1)

Where \( u_i \) is the input signal voltage, \( u_o \) is the output signal voltage, \( R_1 \) is the resistance at the inverting input of op-amp A1, \( R_3 \) and \( R_4 \) are the resistances at the inverting input of op-amp A2, \( R_{f1} \) is the op-amp A1 feedback resistance, \( R_{f2} \) is the op-amp A2 feedback resistance.

Matching op-amp feedback resistances and non-inverting input resistances \( R_{f1} = 2R_1 \), \( R_{f2} = R_3 = R_4 \), the output \( u_o = |u_i| \) can be obtained. Under ideal conditions the circuit can maintain undistorted full-wave rectification when external resistances form the relationship of the above equation, and the output signal is the absolute value of the input. The circuit output pulsating DC voltage with inputting sinusoidal voltage signal, and then the DC voltage signal with ripple is obtained through subsequent filtering processing.

3. Circuit parameter error analysis

3.1. Factors causing errors

In order to accurately realize the AC-DC voltage conversion, the sources of errors should be analyzed. The factors that generate errors are mainly including the following aspects: (1) Non-idealities of operational amplifiers; (2) Resistance accuracy deviations; (3) Diode errors; (4) Environmental changes. Among them, the errors caused by environmental changes can be suppressed or even avoided by partial measures: the experimental environment with constant temperature and humidity conditions can improve the problem of devices parameter changes caused by temperature and humidity; electromagnetic shielding of the circuit board can ensure the requirements of electromagnetic compatibility and avoid interference from external magnetic fields.

3.2. Error analysis of operational amplifier

In actual circuit, the output voltage of the rectifier circuit is limited by various circuit parameters of the op-amp, such as input offset voltage, bias current, common-mode rejection ratio, power supply rejection ratio, slew rate[8]. Figure 2 shows the equivalent model of critical circuit parameters in the actual op-amp, the left op-amp is an ideal op-amp with open-loop amplification \( A_{io} \), the right op-amp constitutes an ideal follower. The main circuit parameters that interfere with the output accuracy are: the input offset voltage \( V_{OS} \), the input bias current \( I_B \), and the input offset current \( I_{OS} \), which are both composed of \( I_{B+} \) and \( I_{B-} \). Next, the different parameters were analyzed separately.
3.2.1. Input offset voltage. When the op-amp has no input voltage, a small voltage will appear at the output terminal. In order to make this voltage zero, the compensation voltage needs to be added to the input terminal. This compensation voltage is called the input offset voltage. Because the differential input stage transistor cannot guarantee complete symmetry, resulting in the actual op-amp non-inverting input terminal cannot avoid the existence of $V_{os}$. The order of magnitude of $V_{os}$ varies greatly between op-amps in different purposes, ranging from 1μV to 100mV. Only considering the existence of $V_{os}$, the output of the full-wave precision rectification is calculated as:

$$u_{o} = \begin{cases} \frac{R_1 R_2 - R_2 R_3}{R_1 R_3} u_1 - \frac{R_2 R_3}{R_4} V_{os1} + (1 + \frac{R_2 R_3}{R_4}) V_{os2}, & u_1 > 0 \\ -\frac{R_2 R_3}{R_4} u_1 - \frac{R_2 R_3 + R_4}{R_3} V_{os1} + \left[1 + \frac{R_2}{(R_1 + R_3)/R_4}\right] V_{os2}, & u_1 < 0 \end{cases}$$

(2)

Where $V_{os1}$ is the input offset voltage of op-amp A1, $V_{os2}$ is the input offset voltage of op-amp A2.

To achieve the same rectification effect, the ideal resistances $R_1 = R_3 = R_4 = R_{f2} = 0.5 R_{f1} = R$ should be ensured. And then equation (2) may be expressed as:

$$u_o = \begin{cases} u_1 - 3 V_{os1} + 3 V_{os2}, & u_1 > 0 \\ -u_1 - \frac{1}{3} V_{os1} + \frac{7}{3} V_{os2}, & u_1 < 0 \end{cases}$$

(3)

At this time $u_o$ is only affected by the two-stage op-amp $V_{os}$, showing the effect of DC offset at the output. If the sum of the input sine wave peak values and offset DC voltage values reaches or exceeds the peak of op-amp power supply, it will be peak clipping at the end. Even if the same model is selected for the front and the after op-amps, it cannot guarantee that the differential input stage is exactly the same. When $u_1 > 0$, it cannot be regarded as two $V_{os}$ cancel each other, and the error needs to be calculated separately. It is known that the standard sine wave passes through an ideal low-pass filter circuit after rectification to obtain the DC signal whose amplitude is average value, the DC voltage is $\bar{u}_0 = 2A/\pi$, where $A$ is the standard sine wave amplitude. This paper calculates the relative error $\delta = (\bar{u} - \bar{u}_0)/\bar{u}_0$ to measure the degree of various circuit parameters impact, where $\bar{u}$ is the average value of the non-ideal output signal.

Input a standard sine wave with 1V amplitude and keep the resistance scale factor constant. OP07, ADA4522-2 and ADA4528-1 three op-amps are selected for rectification. After calculating the relative error, table 1 can be obtained:

| Op-amp model | $V_{os}$ typical value (maximum) /μV | Maximum relative error when A1 is not ideal $\delta_{v1}$ | Maximum relative error when A1 is not ideal $\delta_{v2}$ |
|--------------|-------------------------------------|----------------------------------------------------------|----------------------------------------------------------|
| OP07         | 30 (75)                             | -2.0×10^{-4}                                             | 3.1×10^{-4}                                             |
| ADA4522-2    | 0.7 (5)                             | -1.3×10^{-5}                                             | 2.1×10^{-5}                                             |
| ADA4528-1    | 0.3 (2.5)                           | -6.5×10^{-6}                                             | 1.0×10^{-5}                                             |

It can be seen that for a single op-amp the relative error is proportional to the offset voltage. Since the DC error will not vary, the smaller the input signal voltage, the greater the relative error.
In non-experimental environment, the offset drift should also be selected. The input offset voltage fluctuation can reduce the stability of the output, and even the drift of the offset voltage may be bigger than $V_{BS}$. Therefore, the precision op-amps with small input offset voltage and offset drift, such as ADA4522-2 (typical value of offset voltage drift is 2.5nV/°C) should be used.

3.2.2. Input bias current and input offset current. $I_{B+}$ and $I_{B-}$ are the currents flowing into the two inputs of the op-amp when no signal input. For the op-amp input stage consists of the bipolar junction transistor (BJT), the current is the transistor base quiescent current, and for the op-amp input stage composed of the field effect transistor (FET), the current is the transistor gate leakage current. Because the FET is the voltage-controlled device, there is basically no need for current to flow into the input end during operation, so the latter $I_{B+}$ and $I_{B-}$ are very small.

The input bias current $I_B$ is the average value of $I_{B+}$ and $I_{B-}$, the input offset current $I_{OS}$ is the difference between $I_{B+}$ and $I_{B-}$:

$$I_B = (I_{B+} + I_{B-})/2$$

(4)

$$I_{OS} = I_{B+} - I_{B-}$$

(5)

The output of full-wave rectification when only $I_B$ and $I_{OS}$ exist can be deduced:

$$u_o = u_i - \frac{R_f}{R_i} \left( I_{B1} (R_f/R_i - R_2) - \frac{1}{2} I_{OS1} (R_f/R_i + R_2) \right) + \frac{R_f}{R_s} \left( I_{B2} (R_f/R_s - R_3) + \frac{1}{2} I_{OS2} (R_f/R_s + R_3) \right), \quad u_i > 0$$

$$-\frac{R_f}{R_i} u_i - \left( I_{B1} (R_f/R_i - R_2) - \frac{1}{2} I_{OS1} (R_f/R_i + R_2) \right) - \frac{R_f}{R_s} \left( I_{B2} (R_f/R_s - R_3) + \frac{1}{2} I_{OS2} (R_f/R_s + R_3) \right), \quad u_i < 0$$

(6)

Where $I_{B1}$ is the input bias current of op-amp A1, $I_{B2}$ is the input bias current of op-amp A2, $I_{OS1}$ is the input offset current of op-amp A1, $I_{OS2}$ is the input offset current of op-amp A2, $R_5$ is the resistance at the non-inverting input of op-amp A1, $R_5$ is the resistance at the non-inverting input of op-amp A2.

Similarly let the resistance $R_1 = R_3 = R_4 = R_f = 0.5R_f = R$, the equation (6) is expressed as:

$$u_o = \left\{ \begin{array}{l}
  u_i - 3 \left[ I_{B1} \left( \frac{2}{3} R - R_2 \right) - \frac{1}{2} I_{OS1} \left( \frac{2}{3} R + R_2 \right) \right] + 3 \left[ I_{B2} \left( \frac{1}{3} R - R_5 \right) - \frac{1}{2} I_{OS2} \left( \frac{1}{3} R + R_5 \right) \right], \quad u_i > 0 \\
  -u_i - \left[ I_{B1} \left( 2R - \frac{1}{3} R_2 \right) + \frac{1}{2} I_{OS1} \left( 2R + \frac{1}{3} R_2 \right) \right] + \frac{10}{3} \left[ I_{B2} \left( \frac{3}{10} R - R_5 \right) - \frac{1}{2} I_{OS2} \left( \frac{3}{10} R + R_5 \right) \right], \quad u_i < 0 
\end{array} \right.$$

(7)

In the equation, all values are constant except for $u_i$, the second term is the error caused by op-amp A2, $I_B$ and $I_{OS}$ are converted into new offset voltages through resistances, and the new offset continues to exist as DC voltages at the output. $R_2$ and $R_5$ are also called balance resistances. In the single-stage op-amp, the DC offset error can be controlled by changing the resistance value. For example, when $u_i > 0$, let $R_2 = 2/3R$ and $R_5 = 1/3R$ to eliminate the impact of $I_B$. However, the output signal $u_o$ is a piecewise function, $R_2$ and $R_5$ cannot satisfy the two conditions of $u_o$ at the same time, and the maximum value can only be obtained by estimation. After consulting the data sheets of various op-amps, it is known that $I_B$ and $I_{OS}$ reflect the difference between the two inputs. In most of the op-amps $I_B$ and $I_{OS}$ belong to the same order of magnitude, and there is no case where $I_{OS}$ is zero after subtracting $I_{B+}$ and $I_{B-}$. Therefore, when the balance resistances cannot be accurately matched, the maximum error can be estimated through the second and third terms of equation (7):

$$u_o = \left\{ \begin{array}{l}
  u_i - 3 \left[ 2I_{B1,max} \times \max \left( \frac{2}{3} R, R_2 \right) \right] + 3 \left[ 2I_{B2,max} \times \max \left( \frac{1}{3} R, R_5 \right) \right], \quad u_i > 0 \\
  -u_i - \left[ 2I_{B1,max} \times \max \left( 2R, \frac{1}{3} R_2 \right) \right] + \frac{10}{3} \left[ 2I_{B2,max} \times \max \left( \frac{3}{10} R, R_5 \right) \right], \quad u_i < 0 
\end{array} \right.$$

(8)

Where $I_{B1,max}$ is the maximum input bias current of op-amp A1, $I_{B2,max}$ is the maximum input bias current of op-amp A2.
It can be seen that value of the balance resistances can determine the upper limit of the errors. When the resistance values of \( R_2 \leq 2/3R \) and \( R_5 \leq 1/3R \) are selected, the maximum error could be reduced. At the same time, the external resistance \( R \) should be selected with a smaller resistance value, which is beneficial to reduce the new offset voltage formed by \( I_B \) and \( I_{OS} \). Assuming \( R = 1000\Omega, R_2 = 600\Omega, R_5 = 300\Omega \), inputting the sine wave with amplitude 1V, continuing to select three op-amps OP07, ADA4522-2, ADA4528-1. According to the calculation of equation (8) to obtain table 2.

| Op-amp model | \( I_B \) Typical value (maximum) | \( I_{OS} \) Typical value (maximum) | Maximum relative error when A1 is not ideal \( \delta_{I1} \) | Maximum relative error when A2 is not ideal \( \delta_{I2} \) |
|--------------|---------------------------------|---------------------------------|-----------------|-----------------|
| OP07         | 1.2 (4) nA                      | 0.5 (3.8) nA                    | -2.5×10^{-5}    | 1.3×10^{-5}     |
| ADA4522-2   | 50 (150) pA                     | 80 (250) pA                     | -9.4×10^{-7}    | 4.7×10^{-7}     |
| ADA4528-1   | 90 (200) pA                     | 180 (400) pA                    | -1.3×10^{-6}    | 6.3×10^{-7}     |

Because the error polarity caused by op-amp A1 and A2 is opposite, the relative error when affected by two op-amps working at the same time is between the two when the op-amps are operation alone. According to the superposition theorem, the total relative error \( \delta \) when affected by the main circuit parameters of the op-amps can be obtained in the following range:

\[
\delta_{v1} + \delta_{l1} \leq \delta \leq \delta_{v2} + \delta_{l2}
\]  

(9)

According to table 1 and table 2, the range of \( \delta \) under three different operational amplifiers can be calculated:

| Op-amp model | \( \delta_{v1} + \delta_{l1} \) | \( \delta_{v2} + \delta_{l2} \) |
|--------------|-----------------|-----------------|
| OP07         | -2.2×10^{-4}    | 3.3×10^{-4}     |
| ADA4522-2   | -1.4×10^{-5}    | 2.1×10^{-5}     |
| ADA4528-1   | -7.8×10^{-6}    | 1.1×10^{-5}     |

### 3.3. Resistances error analysis

The output accuracy of full-wave rectifier circuit in the ideal state is highly dependent on the matching degree of resistances, and it is necessary to perform an error analysis on the resistances. Since the value of \( V_{OS}, I_B, I_{OS} \) multiply by the resistance changing value is very small, this change to the output voltage signal can be basically ignored, so the op-amps in the rectifier circuit can be regarded as ideal when the resistance is analyzed separately. Calculating the error of \( R_{f1}, R_{f2}, R_1, R_3, R_4 \) by equation (1). Assuming that \( R_1 = R_3 = R_4 = R_{f2} = 1000\Omega, R_{f1} = 2000\Omega \), the resistance accuracy is 0.01%. Inputting 1V, 50kHz standard sine wave. Take the change of \( R_{f1} \) resistance as an example, as shown in figure 3.

![Figure 3. Output signal deviation when only \( R_{f1} \) resistance value accuracy is 0.01%.

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**Table 3. The range of relative error \( \delta \) on different op-amps models (amplitude \( A = 1 \).**

| Op-amp model | \( \delta_{v1} + \delta_{l1} \) | \( \delta_{v2} + \delta_{l2} \) |
|--------------|-----------------|-----------------|
| OP07         | -2.2×10^{-4}    | 3.3×10^{-4}     |
| ADA4522-2   | -1.4×10^{-5}    | 2.1×10^{-5}     |
| ADA4528-1   | -7.8×10^{-6}    | 1.1×10^{-5}     |
The relative error of 0.02% occurs in the positive half cycle of the input signal. In the same way, table 4 can be obtained.

| Resistance | Relative error at \( u_i > 0 \) | Relative error at \( u_i < 0 \) | Output average (V) | Relative error of output average |
|------------|---------------------------------|---------------------------------|--------------------|-------------------------------|
| \( R_{f1} \) | 0.02% | 0 | 0.636681447 | 1.0×10^{-4} |
| \( R_{f2} \) | 0.01% | 0.01% | 0.636681447 | 1.0×10^{-4} |
| \( R_1 \) | -0.02% | 0 | 0.636554130 | -1.0×10^{-4} |
| \( R_2 \) | -0.02% | 0 | 0.636554130 | -1.0×10^{-4} |
| \( R_3 \) | 0.01% | -0.01% | 0.636617785 | -7.5×10^{-15} |

The drift of \( R_4 \) has little effect on the result and can be considered at the end. When the accuracy of the remaining four resistances is 0.01%, most of the errors caused by the output DC voltage are within 0.01%, and its instability has a certain impact on the output signal. When the conversion accuracy is high, the precision resistance network needs to be selected. Make the resistance change in the same direction and ensure that the resistance proportionality coefficient is basically unchanged to lessen the DC errors.

3.4. Diode error analysis

3.4.1. Nonlinear characteristics of diodes. According the volt ampere characteristic of the diode known that when the diode is positive biased the forward voltage is shown as:

\[
V_D = \frac{kT}{q} \ln \left(1 + \frac{I_D}{I_S}\right)
\]  

Where \( V_D \) is the diode forward voltage, \( I_D \) is the diode forward current, \( I_S \) is the reverse saturation current, \( k \) is the Boltzmann’s constant, \( T \) is the thermodynamic temperature, \( q \) is the quantity of electric charge.

\( V_D \) follows \( I_D \) and presents the nonlinear change. The diode is mainly located in the half-wave rectifier circuit of the first-stage amplifier, the difference with the previous one is that the inverting input of op-amp A2 needs to be regarded as a non-ideal situation with offset current \( I_{B1} = \frac{u_+}{R_1} \). \( R_1 \) is the input resistance of the op-amp, as shown in figure 4.

![Half-wave rectifier circuit](image)

When \( u_i < 0 \), diode D1 is forward biased and D2 is reverse biased, D1 has no effect on the output. When \( u_i > 0 \), D1 is reverse biased and D2 is forward biased, A1 is in a closed-loop state, in this state the \( u_- \) point is

\[
\frac{u_i - u_-}{R_1} = \frac{u_+ - u_{O1}}{R_{f1}} + \frac{u_-}{R_1}
\]

Where \( u_{O1} \) is the half-wave rectified output signal.

Also available that
\[ u_o = -u_\times \cdot A_{uo} = V_{D2} + u_{Q1} \]  

(12)

Where \( A_{uo} \) is open-loop voltage gain, \( V_{D2} \) is the forward voltage of diode D2.

Assuming the value of the input resistance \( R_i \) approaches infinity, according to equations (11) and (12) it can be calculated that

\[ u_{Q1} = \frac{-(R_1 + R_{f1})V_{D2} - A_{uo}R_{f1}u_I}{R_1 + R_{f1} + A_{uo}R_1} \]  

(13)

Let \( F = R_1/(R_1 + R_{f1}) \), where \( F \) is the feedback factor of A1, and after simplification the equation is

\[ u_{Q1} = -\frac{R_{f1}}{R_1} \left( 1 - \frac{1}{1 + A_{uo}F} \right) u_I - \frac{V_{D2}}{1 + A_{uo}F} \]  

(14)

When A1 is an ideal op-amp, the open-loop voltage gain is infinite, and the circuit becomes an inverting amplifier at \( u_I > 0 \), \( u_{Q1} = -R_{f1}u_I/R_1 \). From equation (14), it can be seen that the nonlinear characteristic affects the full-wave rectification by affecting the output of the half-wave rectification. \( I_{D2} \) flows through D2, at the output load end there is \( I_{D2} = \frac{u_\times - u_{Q1}}{R_{f1}} = -\frac{u_{Q1}}{R_{f1}/R_L} \), \( R_L \) is the load resistance. \( u_{Q1} \) also affects the diode forward voltage in the circuit. In order to reduce influence of the diode nonlinear error, the internal resistance and the open-loop voltage gain of op-amp should be selected as large as possible. At the same time, it is necessary to control the change of \( I_{D2} \). Consider employing new devices such as current conveyors to suppress the change of \( V_{D2} \) \[9\].

3.4.2. Diode causes zero point distortion. When observing the output signal, it is found that distortions always occur near the zero point in the output waveform. The distortion degree can be observed by selecting different amplitudes or different frequencies, as shown in figure 5. The green line represents the input signal and the black line represents the output signal. From the figure, it can be seen that: (1) When the polarity of the input sine wave changes from negative to positive, distortion will appear at the zero point; (2) The higher the frequency of the input signal, the higher the distortion levels; (3) At the same frequency, the smaller the input signal amplitude, the more obvious the output waveform distortion.

![Figure 5. Full-wave rectification output voltage with different parameters.](image-url)
The reason for this phenomenon is that when the sinusoidal input signal is close to zero, both diodes in the circuit will be in the cutoff state in a short time. So that the op-amp A1 in figure 1 is in the open loop state for a limited time\textsuperscript{[10]}, as shown in figure 6.

![Simplified circuit diagram when A1 is in open loop state.](image)

Figure 6. Simplified circuit diagram when A1 is in open loop state.

Figure 7 shows the voltage at the inverting input of op-amp A1 when the input amplitude is 1V and the frequency is 50kHz sine wave, which is also the voltage between the resistances \( R_1 \) and \( R_{f1} \) in figure 6. Because the input impedance of the op-amp is very high, the two input terminals are generally in virtual ground state, and the voltage is maintained near the zero point. In the figure, the positions where the voltage waveform produces burrs are all located at the time point of the polarity change. The sudden change voltage at this point indicates that the inverting input terminal is no longer virtual ground, which proves that the op-amp A1 is open loop at this time.

![Voltage at A1 inverting input.](image)

Figure 7. Voltage at A1 inverting input.

Assuming that the open loop time is \( t_d \), input signal is \( u_i = A \sin(2\pi f t) \). Due to the input and output are both periodic signals, the rectified output with distortion is calculated in a period \( T \) as:

\[
u_o = \begin{cases} 
-\frac{R_{f2}}{(R_1+R_{f1}+R_3)//R_4} A \sin(2\pi f t), & 0 < t \leq t_d \\
\frac{R_{f2} R_{f3}}{R_1 R_3} - \frac{R_{f3}}{R_4} A \sin(2\pi f t), & t_d < t \leq \frac{T}{2} \\
-\frac{R_{f2}}{(R_1+R_{f1}+R_3)//R_4} A \sin(2\pi f t), & \frac{T}{2} < t \leq \frac{T}{2} + t_d \\
-\frac{R_{f2}}{R_4} A \sin(2\pi f t), & \frac{T}{2} + t_d < t \leq T 
\end{cases}
\] (15)

According to the above equation, the reason for the waveform distortion in figure 5 can be explained: when the input signal polarity changes from negative to positive, \( u_i \) direct passes through the inverting amplifier by A2 during the open loop time, and the output polarity is negative. Similarly, when the polarity of the input signal changes from positive to negative, the output polarity is positive. Therefore,
it can be seen that the distortion caused by the negative to the positive phase of the input signal is more obvious. After reading the paper [10], it can be seen that \( t_d \) is in inverse proportion to the cube root of unit gain bandwidth \( \sqrt[3]{f_T} \). Choosing the op-amp with a large unity gain bandwidth will reduce the open loop time of the circuit and reduce the degree of distortion, at the same time it can also improve the response of high-frequency signals.

4. Conclusion

This paper analyzes the errors of three main components that produce errors in full-wave rectifier circuit, and obtains the following conclusions:

(1) Try to choose precision operational amplifier with small circuit parameters such as \( V_{OS}, I_B, I_{OS} \) and their drift.

(2) Strictly match external resistances \( R_1 = R_3 = R_4 = R_{f2} = 0.5R_{f1} = R \) and give preference to balancing resistances \( R_2 \leq 2/3R, R_5 \leq 1/3R \). In order to keep the equation relationship between the resistances unchanged, the resistance network structure is selected to make its performance consistent.

(3) The distortion of the output voltage signal at the zero point is because that the two diodes are all disconnected near the zero point, making the op-amp A1 in the open loop state. The output voltage is no longer rectified during the open loop time \( t_d \). And the levels of distortion depend on the length of the \( t_d \), which is negatively correlated with the unit gain bandwidth of the op-amp. Therefore, it is necessary to choose an op-amp with higher unit gain bandwidth (or gain bandwidth product) when inputting high frequency signals.

This paper calculates the error caused by op-amp and resistance in the output in practice, explores the nonlinear influence of diodes and the cause of rectification zero point distortion, summarizes some principles on the selection of components for rectifier circuit, provides some theoretical guidance for further improving the accuracy of the full-wave rectifier circuit in the future.

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