Remote Configuration of the ProASIC3 on the ALICE Inner Tracking System Readout Unit

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Abstract—A Large Ion Collider Experiment (ALICE) is one of the four major experiments conducted at the CERN Large Hadron Collider (LHC). The ALICE detector is currently undergoing an upgrade for the upcoming Run 3 at the LHC. The new Inner Tracking System (ITS) sub-detector is part of this upgrade. The front-end electronics of the ITS is composed by 192 Readout Units, installed in a radiation environment. Single Event Upsets (SEUs) in the SRAM-based Xilinx Kintex Ultrascale FPGAs used in the ITS readout represent a real concern. To clear SEUs affecting the Kintex configuration memory, a secondary Flash-based Microsemi ProASIC3E (PA3) FPGA is used. This device configures and continuously scrubs the Xilinx FPGA while data-taking is ongoing, which avoids accumulation of SEUs. The communication path to the RUs is via the radiation hard Gigabit Transceiver (GBT) system on 100 m long optical links. The PA3 is reachable via the GBT Slow Control Adapter (GBT-SCA) ASIC using a dedicated JTAG bus driving channel.

During the course of Run 3, it is foreseeable that the FPGA design of the PA3 will require upgrades to correct possible issues and add new functionality. It is therefore mandatory that the PA3 itself can be configured remotely, for which a dedicated software tool is needed. This paper presents the design and implementation of the distributed tools to re-configure remotely the PA3 FPGAs.

Index Terms—Flash FPGA, Giga-bit transceiver, High Energy Physics

I. INTRODUCTION

The ALICE experiment is designed to study the strong interactions between quarks, in particular the properties of Quark-Gluon Plasma (QGP), through measurements and observations of heavy ion collisions at the LHC. The LHC is undergoing an upgrade during Long Shutdown 2 (LS2), which started in December 2018. This upgrade will bring the target integrated luminosity of Pb-Pb collisions to 10 nb$^{-1}$ at the design LHC energy of $\sqrt{s_{NN}}=5.5$TeV. This higher luminosity represents an increase of a factor of 10 in the inspected luminosity for rare signals, and a factor of 100 for the minimum-biased data sample [1]. The major upgrade that the ALICE apparatus is undergoing has therefore to cope also with the increased data rate. During LS2, a completely new detector will replace the Inner Tracking System (ITS), with significantly reduced material budget while delivering higher detector resolution. It is based on the ALPIDE (ALIce PXel DEtector, a custom-made CMOS monolithic active pixel sensor) chip sensors, which are controlled and read-out by the Readout Units (RUs) in ITS.

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several links that connect RUs and CRUs are capable of transmitting one 120-bit GBT frame per LHC bunch crossing interval ($\approx 25$ns), resulting in a line data rate of 4.8 Gbps. Two additional bits in the GBT frame are the External Control (EC) field [3]. The EC is passed to the GBT-SCA from the GBT interface. This field carries the configuration data for PA3. The CRU sits in the First Level Processors (FLPs) in the counting room. The FLP hosts software for control and data read-out, and is responsible of forwarding the aggregated data from different links over Ethernet to the Event Processing Nodes (EPNs) which stores the data for further analysis. Each FLP is capable of hosting up to two CRUs on its PCI Express slots, and each CRU is capable of linking up to eight RUs.

The CRU is responsible for data aggregation and control of the front-end electronics. The CRU memory space is PCIe BAR-mapped by the Portable Driver Architecture (PDA) driver via the ReadoutCard (RoC) module of the ALICE Online-Offline computing system (ALICE O2). The RoC module is a C++ library that provides a high-level interface for accessing and controlling data acquisition PCIe cards [4]. It offers an API to the PCIe BAR.

B. Motivation for remote configuration of the PA3

The remote configuration application for the PA3, pa3jtag, is a dedicated software tool that is foreseen to be used by detector experts only in periods when data taking is not ongoing. It uses the same hardware and driver structures as the central Detector Control System (DCS), therefore a low level arbitration is needed. This exists in the ALICE O2 [5], and the pa3jtag application utilizes this to ensure safe detector operation.

It is not foreseen that remote configuration of the PA3 will be a frequent operation. It is however important to have the opportunity to remotely upgrade the PA3 for potential future upgrades or bug-fixes. Special PA3 builds also exist that enable for instance fault injection, which can be used to qualify the robustness of new versions of the main FPGA firmware. Additionally, the physical access to the RUs are limited due the radiation environment and the actual location of the installation, so it is of vital importance to have a remote configuration functionality.

C. Structure of the paper

This paper presents pa3jtag, a new software tool that is used to reconfigure the PA3 FPGA on the ALICE ITS Readout Unit for the ITS experts. The structure of the paper is:

1) Section I gives an overview of upgraded ALICE Inner Tracking System, and the motivation for developing pa3jtag.
2) Section II describes the hardware components related to pa3jtag in ITS.
3) Section III introduces DirectC, the software tool based on which pa3jtag has been developed.
4) Section IV lays out the design and implementation of pa3jtag.
5) Section V summarizes the work.

II. SYSTEM COMPONENTS AND DATAPATH OF THE PA3 CONFIGURATION

A. The GigaBit Transceiver - Slow Control Adapter

The PA3 configuration data is transmitted via the 2-bit EC field in the GBT Frame from the CRU to the RU. As shown in Figure II, the GBT-SCA is connected to a dedicated port on GBTx0 through e-links, which is a 80 Mbps dual redundant bidirectional data-link. GBTx0 passes the EC information to GBT-SCA via the e-links. The GBT-SCA has several user-configurable interface ports: 1 SPI master, 16 independent 1-bit masters, 1 JTAG master, and 32 General Purpose IOs, as is shown in the GBT-SCA block diagram in Figure II. The GBT-SCA move the EC data from the E-PORT to the Network Controller via a Wishbone bus. The GBTx is transparent to the communication between the CRU and the GBT-SCA. The GBT-SCA interface channels are memory mapped on the PCIe bus, thus accessible from the RoC API. The JTAG Master channel is connected to the RU JTAG configuration chain, hence it is utilized for the configuration of PA3.

The JTAG channel configuration registers in the GBT-SCA are described in Table II. The JTAG channel of GBT-SCA has two 128-bit shift registers that serializes and deserializes the data between the JTAG lines and the internal modules. The TDO and TDI shift registers physically share the same...
hardware registers, though the assigned addresses in the PCIe BAR space differ. The control register defines the number of bits transmitted in a single JTAG operation, the MSB/LSB, and serves as the busy flag of the JTAG bus. The vacancy of a JTAG TAP controller in the GBT-SCA means the JTAG data packets will be generated by an agent deployed on the other end of the GBT optical links.

A typical JTAG command that writes to the TDI line consists of the following steps:

1) Setting the TDI data packet length by writing to the control register
2) Writing the TDI data to the TDI shift register, if the data is longer than 32 bits, then multiple writes to adjacent sections of the buffer are necessary
3) Write to the JTAG_GO register, which starts the serial communication on the JTAG bus

### TABLE I

| Register | Mode | Function | Size (bit) |
|----------|------|----------|------------|
| Control  | R/W  | Define operation mode of the channel | 16 |
| Frequency| R/W  | Set the operating frequency of the channel | 16 |
| TDO      | R/W  | Data transmit buffer for the TDO line | 32×4 |
| TDI      | R    | Data receive buffer for the TDI line | 32×4 |
| TMS      | R/W  | Data transmit buffer for the TMS line | 32×4 |

#### B. The RU JTAG Configuration Scheme

The JTAG configuration datapath on the RU is shown in Figure 5. The TMS pins of PA3 and the main FPGA are connected in parallel with the TMS output pin of GBT-SCA; whereas the TDI/TDO line is connected in serial. The Instruction Registers (IR) and Data Register (DR) are connected in a long shift register from the TDO to the TDI pins of GBT-SCA. The IR lengths for PA3 and the main FPGA are 4, and 6 respectively. The DR length depends on the instruction in the IR, and when the device is in bypass mode, the DR length is set to 1.

#### III. DirectC

DirectC is a suite of C/C++ code designed for the In-System Programming (ISP) of several series of Microsemi FPGA products. Users need to make modifications to the software suite taking different system constraints into account. A typical ISP setup consists of three major parts: a JTAG Test Access Port (TAP) controller, a memory space storing the configuration file, and the JTAG configuration chain where the programmable devices are connected end-to-end. DirectC serves as the JTAG TAP controller in a way that it programs the processor to toggle certain spaces in the memory that is designated to the output port, for instance the GPIO pins, which is physically connected to the JTAG pins on the JTAG configuration chain in system. DirectC by default supports bit-banging of the JTAG signal protocol, which is inefficient in the context of Slow Control communication, so it must be adapted to use the buffer register in the JTAG master module of GBT-SCA.

#### A. The .dat Configuration File

The .dat configuration file is generated by the Microsemi Libero development tool, and is preferred by the DirectC toolset. The .dat file for PA3 contains the following sections:

1) Header Block - Identifies the type of the image, the size of the image, device information, and different flags that guide the DirectC algorithm to identify which block is supported and its associated options.
2) Data Lookup Table - Pointers to the starting of the relative location of all the different data blocks used in DirectC algorithm, and the size of each block.
3) Data Block - The configuration binary data for the data blocks pointed in the Data Lookup Table.

The sizes, and the main information of each section are given in Table II.

| Size (Byte) | Information                                           |
|------------|--------------------------------------------------------|
| HB         | 69 Designer version number, Header size, Image size, Compression Flag, etc. |
| DLT        | $n_1 \times 9$ Data Identifier 1, Pointer to data 1 memory location in the data block section, # of bytes of data 1; Data Identifier 2, Pointer to data 2 memory location in the data block section, etc. |
| DB         | $n_2 + 2$ Configuration binary data, CRC of the entire image |

The size of DLT is $n_1 \times 9$ Bytes, where $n_1$ is the number of data pointers; the size of DB is $n_2 + 2$ Bytes, where $n_2$ is the size of the configuration binary data, and the final 2 Bytes are CRC of the entire image. Over 99.9% of the .dat file is the configuration binary data.

B. The Algorithm of DirectC

The entry function of DirectC is dp_top. dp_top passes an Action_code to dp_top_g3. dp_top_g3 initializes the system for configuration, and invokes dp_perform_action to execute the corresponding algorithms based on the given Action_code in a switch statement.

For example, when the program tries to read the device id information, dp_perform_action would invoke dp_read_idcode, and the pseudo code for this function is shown below:

```c
void dp_read_idcode(void)
{
    opcode = IDCODE;
    IRSCAN_in();
    goto_jtag_state(JTAG_RUN_TEST_IDLE);
    DRSCAN_out(IDCODE_LENGTH, global_buf);
    device_ID = mem_shift(global_buf);
    return;
}
```

The dp_read_idcode action function consists of three consecutive software-hardware interactive steps:

1) The global variable opcode is assigned with the IDCODE, and IRSCAN_in (IR stands for Instruction Registers) shifts the opcode to the TDO/TDI line of the JTAG chain;
2) goto_jtag_state shifts the corresponding TMS packet to invoke JTAG state changes;
3) DRSCAN_out (DR stands for Data Registers) shifts the TDO read-back TDO/TDI line to the memory space controlled by the processor.

The Action_code look-up table is pre-defined by the vendor. To verify the device_id read-back, the DirectC asserts it with the corresponding information stored in the .dat file. The relative location of this information is pre-defined in DirectC header files.

The functions: IR scan-in, DR scan-out, and the JTAG state-change all invoke dp_jtag_tms_tdi_tdo, which calculates the JTAG pin digits, assigns them to a global 8-bit static variable char jtag_port_reg, and passes it to jtag_outp. jtag_outp sets the JTAG port by toggling the specified memory space, thus putting the configuration digits on the JTAG lines.

IV. pa3jtag Design and Implementation

The goal of pa3jtag is to configure the PA3 via the Slow Control datapath by utilizing the PCIe BAR-mapped JTAG channel of GBT-SCA from the FLP. Simply put, configuration of an FPGA consists in writing the configuration file into the FPGA configuration memory, after having passed through the preparation steps such as setting the JTAG transmitting frequency, verifying the JTAG chain, checking the device ID etc.

Initially, various options for remote configuration of the PA3 were investigated, such as writing the software from scratch, or adapting the STAPL Player code.

Making the tool from scratch was infeasible for two main reasons: (1) Configuring the PA3 requires taking various parameters of the device defined by the vendor into the program, and these parameters are usually defined in the compatible configuration tools maintained by the vendor. So the development was to rely partly on the open-source code released by the vendor, and (2) the schedule of the project forbade the developing-from-scratch approach.

The Standard Test and Programming Language (STAPL) was first introduced in 1999 to support the programming of programmable devices and testing of electronic systems, using the IEEE Standard 1149.1: "Standard Test Access Port and Boundary Scan Architecture" (commonly referred to as JTAG). As a STAPL file is executed, signals are produced on the IEEE 1149.1 interface, as described in the STAPL file. The STAPL Player is an interpreter program that executes the statements in the STAPL file directly without compiling these statements into a binary executable file.

The earliest STAPL Player available was released by Actel in 2003 with Application Note AC171. And the most recent Actel STAPL Player (v1.1) was released in 2008. Though it was tried to modify STAPL Player v1.1 for configuring PA3, and performing few other actions such as scanning the JTAG chain, reading the device information worked with the modified code, but the programming action failed with syntax errors in the STAPL file that was generated by the Microsemi Libero tool.

The LHCb team who worked on a similar agenda encountered similar issues with the Actel STAPL Player, and diverted to DirectC. Other STAPL Player options, such as the Intel Jam STAPL Player, are not compatible with the PA3 STAPL files generated by Microsemi Libero.

It turned out that basing the pa3jtag on DirectC v4.1 was the best option for remote configuration. As introduced in section III, DirectC is a tool that is capable of parsing and interpreting a .dat file to JTAG Test Mode Select (TMS) and Test Data In (TDI) bitstreams, and writing/reading the TMS, TDI/TDO (Test Data Out) sequential bits to/from the JTAG ports. As

1) Actel was acquired by Microsemi in 2010.
mentioned in section II-B, the JTAG chain on the RU has two components: the main FPGA and the PA3. The configuration file in DirectC sets the data register and instruction register lengths of both devices. This ensures that the configuration file is written correctly to the target FPGA.

What DirectC lacks is the utilization of the upper part of the configuration datapath from the FLP to GBT-SCA. Therefore a GBT_SCA class that utilizes the GBT-SCA JTAG channel has been designed based on the GBT-SCA user manual [11].

The GBT-SCA interface class GBT_SCA As introduced in section II-A, the JTAG channel of GBT-SCA includes two 128-bit shift registers as transmit buffers that serializes and deserializes the configuration TMS and TDI/TDO packets. In order to accelerate the configuration of the PA3, multiple modifications have been applied to the DirectC algorithm so that it uses the transmit buffers in the JTAG channel. The 128-bit transmit buffers, each of which consists of four 32-bit registers, and the CONTROL and FREQUENCY registers are accessible respectively from GBT_SCA class. The GBT_SCA class implements the option of setting the optimal size of the packets prior to writing it on the JTAG line. The packets have different sizes in different parts of the JTAG bitstream, and some requires verifying the TDO read-backs, while others do not. The pseudo code for sending a data packet to the JTAG line is shown below:

```c
void jtag_tr(u128_t tms, u128_t tdi, u32_t length) {
    if(length != G_length) {
        G_length = length;
        jtag_w_CTRL(G_length);
    }
    if(tms != G_tms) {
        G_tms = tms_data;
        jtag_w_TMS(G_tms);
    }
    jtag_w_TDI(tdi);
    jtag_start_transmission();
}
```

In order to minimize the number of accesses to the JTAG channel, some of the data to be transmitted are compared with global variables storing the data from the previous transmission. If the data to be transmitted is the same as the last transmission, then `pa3jtag` omits this transmission. The TDO/TDI register is always used to transmit different data, so this mechanism is only implemented for TMS buffer and the control register.

Apart from accessing the transmission and control registers, the GBT-SCA interface also provides functions on an operational level, such as power switch of the JTAG channel, setting JTAG transmitting frequency, GBT-SCA id verification, and GBT-SCA initialization, etc.

Concatenating data packets in JTAG state shifts The function IRSCAN_in, which sends an opcode to the JTAG lines, is a frequently used function in the DirectC algorithm. It consists of three TMS writes and one TDI write. Sending each of the TMS/TDI packet requires one write to the GBT-SCA JTAG transmit buffer and one write to the `JTAG_GO` command register, therefore eight GBT-SCA accesses were required in the original algorithm. Depending on different opcodes, the TDI packets vary, but the rest stays the same. Plus, this function does not require TDO read-backs. Based on this observation, the algorithm has been modified into a way that the packets generated in IRSCAN_in are concatenated and written to the JTAG transmit buffer with three GBT-SCA writes (one TDI packet, one TMS packet, and one `JTAG_GO` command), thus reducing the number of accesses to GBT-SCA as optimally few as possible. Often, the length of the packet involved in IRSCAN_in is less than 32-bit, in which case it is sufficient in these cases to utilize only the least-significant section of the transmit buffer. This strategy has also been applied to modify other functions in the DirectC algorithm in the similar manner.

Accelerating `program_array` The most time-consuming part of the PA3 configuration is writing the configuration data on the Look-Up Table (LUT) array. In the PA3, the 3444-Row (also know as Column Grid, or CG) memory block array stores the configuration. Based on our observation of the JTAG bitstream involved with `program_array`, the total length of the TDI packets corresponding to one CG is 98-bit, therefore the algorithm has been modified in a way to concatenate all the involved packets to a single 98-bit packet, and utilizes all the four section of the 128-bit shift register for the transmission. As for the TDO read-backs involved with `program_array`, tests and observations did show that the TDO read-backs are constants representing device information and configuration status, instead of variables depending on the configuration data. Therefore the algorithm has been modified for `pa3jtag` to skip the execution of TDO read-backs, and provided with “fake TDO read-back” constants to further accelerate the configuration process.

V. COMPARISON AND SUMMARY

A similar problem of controlling the Front-end Electronics (FE) from the Experiment Control System (ECS) via the GBT-SCA chip was encountered by one of the sub-detector teams at the LHCb experiment. They have a different approach. In the LHCb solution, a dedicated interface board (SOL40) is designed to distribute all the control signals to the FEs [12]. In the SOL40’s firmware, the SOL40-SCA core is responsible of sending ECS commands to the GBT-SCA.

Figure 6 shows the block diagram of how the SOL40-SCA core interfaces between the LHCb ECS and FEs.

When configuring the FPGAs on the FE, the SOL40-SCA core serves as a JTAG TAP controller, thus it significantly lowers the time consumption for the FPGA JTAG configuration action, compared to our solution.
The ALICE CRU is at the same hierarchical position as SOL40 in LHCb, however an interface like the SOL40-SCA is not added in the CRU firmware, hence the pa3jtag needed to be implemented as a pure software tool. If a similar functionality as the SOL40-SCA was added to the CRU firmware, the ITS team would be responsible for the maintenance of this ITS specific module, which opposes to the current situation where the CRU team is fully in charge of the CRU firmware. The complexity of the CRU design would increase if sub-detector specific modules are added. The manpower to develop and provide maintenance to this module would also be something to consider. Therefore a pure software solution is reasonable for our application.

In conclusion, the size of the .dat file for PA3 is 537,694 Bytes, and the bottleneck of the configuration is the access to the GBT-SCA JTAG channel registers from the FLP, which takes on average 3 ms. Although various techniques have been applied to accelerate the configuration, the unavoidable TDO read-backs and the transmission of smaller packets significantly slow down the process. As of now, pa3jtag is able to configure the PA3 in 31 minutes, implying that the effective configuration bit rate is around 2.4 Kbps. The time consumption is however acceptable for the contextual usage. In principle, pa3jtag can also be used to configure the main FPGA. But the size of the configuration file for the main FPGA is 24,125,021 Bytes, ≈45 times to the PA3. The configuration time of the Xilinx using the PA3 and the flash memory is approximately 2 s, therefore it makes no sense to use the Slow Control data path for the configuration of the main FPGA.

However, since the PA3 configuration action is not considered to be frequently executed, and it is possible to run it in parallel on each individual FLP, it is considered to be fast enough in our case. The possibility to configure the PA3 on the RU is anyway considered an important component to ensure the robustness of the real-time data taking system the ITS RU represents.

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