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High-frequency single-switch PFC with frequency-modulation controlled class-E² converter

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Abstract
This paper presents a single-switch zero-voltage switching (ZVS) power-factor correction converter based on the class-E² converter at 1 MHz switching frequency. A design method for ensuring the ZVS for the entire line-voltage period is proposed. By visualising the ZVS region in the parameter space, circuit parameters can be easily obtained to achieve the ZVS for the entire line-voltage period. Additionally, a closed-loop controller is applied for achieving a high power factor, low total harmonic distortion of the input current and output voltage regulation. The experimental circuit achieved the ZVS in the entire line-voltage period against load variations. As a result, the implemented converter achieved the same level of power-conversion efficiency as the 100-kHz power-factor correction converters and a high power factor with low total harmonic distortion, which denoted the effectiveness of the proposed design method.

1 Introduction

AC–DC power supplies with power factor correction (PFC) are used in a wide range of applications. The applications of AC–DC converters include battery charger [1–6], light-emitting diode (LED) lighting [7–16], electric vehicle (EV) [17, 18] and laptop computer [19, 20]. A two-stage PFC power converter [1, 2, 21–24] is a series connection of an AC–DC converter for correcting PF and a DC–DC one for regulating the output voltage. The two-stage AC–DC converter requires at least two power switches and two individual controllers, which leads to a high cost and a large volume. On the other hand, a single-stage AC–DC converter combines the PFC stage and the voltage-regulating one into a single converter [3–16, 20, 24–31]. Therefore, single-stage converters have a small component number and achieve low costs compared with two-stage converters, and are often applied for space-constrained applications such as battery chargers [3–6].

Traditional converter topologies, such as boost [11, 12], buck [13], buck-boost [13, 14], and Flyback converters [9, 10], have been widely applied to the single-stage AC–DC converters. These converters have simple topologies. However, traditional converter topologies often suffer from low power-conversion efficiencies. This is because most of them are hard-switching converters [9–14], which generate large switching losses. For power-conversion efficiency improvements, the resonant topologies, such as the LLC converters [4, 5, 15, 30, 31] and class-E converters [7, 8, 16, 21, 32–39], have also been applied to the AC–DC converters [4–8, 15, 16, 20–23, 30–32]. The resonant converters have more circuit components than the traditional converters because of the resonant circuit. However, it is an advantage of the resonant AC–DC converters to achieve soft switching and switching loss reduction.

A high-frequency operation is required for the resonant single-stage AC–DC converter for reducing the circuit volume as much as possible. The class-E² converter [32–37], one of the typical resonant converters, is a leading candidate for high-frequency resonant AC–DC converters. Compared with the LLC converter, the class-E² converter has no high-side switch,
which can avoid the driver-design difficulty at high frequencies. It is expected to realise the single-stage AC–DC resonant converters with megahertz-order operation by applying the class-E² converters.

The class-E AC–DC converters work at several hundred-kilohertz frequencies in previous researches [7, 8, 16, 21]. In these papers, the class-E AC–DC converters were designed with the fixed input voltage and the rated load resistance as a DC–DC converter in the steady-state. However, the input voltage of the AC–DC converter varies with line frequency, which is much lower than the switching frequency, and the cutoff frequency of the output filter is determined by the line frequency. Namely, the class-E AC–DC converter always works in the transient state in the time range of the switching period, and the mismatch occurs with the design assumption. As a result, the switching losses occurred at a certain angular displacement range in the line-voltage period. This switching loss can be ignored at a 100-kHz switching frequency but cannot be done at megahertz operation. Therefore, it is necessary to establish the design method of the AC–DC converter for ensuring the zero-voltage switching (ZVS) operation in the entire range of the line-voltage period for achieving megahertz frequency operation.

This paper, which is the extended version of [32], presents a single-switch ZVS PFC converter based on the class-E² converter at one megahertz switching frequency. A design method for ensuring the ZVS for the entire line-voltage period is proposed. Additionally, system performance against load variation is investigated.

2 | DESCRIPTIONS OF PROPOSED CONVERTER AND CONTROLLER

2.1 | Circuit topology and operation principle

Figure 1 shows a topology of the proposed AC–DC converter. The system includes the input stage and the class-E² converter, which consists of the class-E inverter and the class-E rectifier connected in series. This system converts the input ac line voltage into the DC voltage via the class-E² converter, whose switching frequency is much higher than the line frequency.

Figure 2 shows example waveforms of the proposed converter in the line-voltage-period domain and switching-period domain, where $\theta_L = 2\pi f_L t$ and $\theta_S = 2\pi f_S t$ are phase displacements with the line frequency $f_L$ and the switching frequency $f_S$, respectively.

2.1.1 | Input stage

The input of the system is the sinusoidal voltage with line frequency $f_L$, which is

$$v_I = \sqrt{2} V_I \sin \theta_L = V_m \sin \theta_L,$$

where $V_m$ is the amplitude, $V_I$ is the RMS value of the input AC voltage.

The input-stage circuit consists of a rectifying bridge, as shown in Figure 1. The rectifying bridge generates absolute-valued sinusoidal voltage $v_I$, as shown in Figure 2(a), which becomes the input voltage of the class-E inverter.

2.1.2 | Class-E inverter

The class-E inverter has input inductance $L_{C_S}$, FET $S$, shunt capacitance $C_S$, and resonant circuit $L_0$–$C_0$, as shown in

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1 In [32], only the circuit topology and the experiment at full-load condition are presented. In this paper, the circuit design method based on the ZVS region map is proposed. Additionally, system performance against load variation is investigated.
Figure 1. There is only one source-grounded FET in the class-E inverter, and there is no source-floating FET. Therefore, the gate driver circuit becomes simple, which is one of the benefits of the class-E inverter for high-frequency operations.

The switching frequency of the class-E inverter is much higher than the input line frequency. Therefore, the output voltage of the rectifying bridge \( V_B \) looks constant within one switching period of the class-E inverter, as shown in Figure 2(b). Besides, the input inductance \( L_C \) is sufficiently high that the input current of the class-E inverter \( i_C \) is regarded as DC current in one switching period.

The switching device \( S \) turns on and off periodically with switching frequency and the on-duty ratio \( D_S \). Because of the shunt capacitance \( C_S \), the pulse-type shape of voltage appears across the switch when the switch is in the off-state. For the class-E inverter, there are particular switching conditions when the FET turns on, which are

\[
\tau_S(2\pi) = 0, \tag{2}
\]

\[
\left. \frac{d\tau_S(\theta_S)}{d\theta_S} \right|_{\theta_S=2\pi} = 0. \tag{3}
\]

The conditions in Equations (2) and (3) are called class-E ZVS and zero-derivative switching (ZDS) conditions. When the switching voltage satisfies the class-E ZVS/ZDS conditions, the converter operates at the “nominal state.” The switching frequency for satisfying the class-E ZVS/ZDS conditions is defined as nominal switching frequency \( f_{Sn} \). The converter, however, does not achieve the class-E ZVS/ZDS conditions when the converter parameters vary from the nominal conditions. The detailed discussion of the switching patterns was done in [38]. At outside of the nominal state, there are two switching modes. One is the ZVS, which can be achieved with the help of the FET body diode. The other one is the non-ZVS, which deteriorates the power-conversion efficiency at high frequencies, in particular.

Due to the \( L_0-C_0 \) resonant filter, the resonant-frequency component \( f_0 = 1/(2\pi\sqrt{L_0C_0}) \) of the switch voltage is extracted. Therefore, the current flowing through the resonant
2. The bridge rectifier $B_i$ is modelled by the ideal switches and on-resistances $r_{DB}$. Therefore, the input stage is expressed by the voltage source $v_B$ and the diode on-resistance $r_B = 2r_{DB}$, which are connected in series, as shown in Figure 3(a). The input voltage $v_B$ is derived as:

$$r_B = \sqrt{2}V_m \left| \sin \theta_1 \right| = V_m \left| \sin \theta_L \right|, \quad (4)$$

3. The FET with its body diode is modelled by ideal switches, resistances, and voltage source, as shown in Figure 3(b), where $r_{DS}$ is the FET on-resistance, $V_{SD}$ is the forward voltage of the body diode, and $r_{SD}$ is the on-resistance of the body diode.

4. The class-E rectifier diode is expressed by ideal switch, on-resistance $r_{DS}$, and forward voltage $V_F$, as shown in Figure 3(c).

5. ESRs of inductances $L_C$, $L_O$ and $L_F$ are considered. The current-sensing resistor $r_1$ and ESRs of all the capacitances are ignored because they are sufficiently small compared with ESRs of inductances and on-resistances.

### 3.2 Circuit parameters and system equations

The numerical analysis model is formulated with the normalised variables and parameters. The converter characteristics can be discussed with a generality because of the dimensionless space. Namely, the obtained results are independent of switching frequency, input voltage amplitude, and load resistance.

Now, we define the following dimensionless parameters:

$$\alpha_s = f_s / f_{so}, \quad \alpha_L = f_L / f_{so}, \quad \alpha_f = f_c / f_{so}, \quad \beta = f_s / f_{so},$$

$$\gamma_s = C_s / C_0, \quad \gamma_D = C_D / C_0, \quad \lambda_L = L_L / L_0, \quad \lambda_F = L_F / L_0, \quad \gamma_0 = 2\pi f_0 L_0 / R_{L0}, \quad Q_L = 2\pi f_c L_0 / R_{L0}, \quad \rho_C = R_C / R_{L0}.$$ Besides, $\rho$ means a normalised resistance parameter, for example, $\rho_{LC} = \rho_{L_0} / R_{L0}$. By using these parameters, the circuit equations can be formulated as:

$$\frac{d\alpha_s}{d\theta_S} = \frac{\alpha_s}{\alpha_s + \rho_{L_0}/\lambda_L} \left( \sqrt{2} \sin \theta_1 \right) + \left( \gamma_D - \rho_D \right) \frac{\alpha_s}{\alpha_s + \rho_{L_0}/\lambda_L} \left( \sqrt{2} \sin \theta_1 \right)$$

$$\frac{d\alpha_f}{d\theta_S} = \frac{\alpha_f}{\alpha_f + \rho_{L_0}/\lambda_L} \left( \sqrt{2} \sin \theta_1 \right) + \left( \gamma_D - \rho_D \right) \frac{\alpha_f}{\alpha_f + \rho_{L_0}/\lambda_L} \left( \sqrt{2} \sin \theta_1 \right)$$

$$\frac{d\alpha_f}{d\theta_S} = \frac{\alpha_f}{\alpha_f + \rho_{L_0}/\lambda_L} \left( \sqrt{2} \sin \theta_1 \right) + \left( \gamma_D - \rho_D \right) \frac{\alpha_f}{\alpha_f + \rho_{L_0}/\lambda_L} \left( \sqrt{2} \sin \theta_1 \right)$$

$$\frac{d\alpha_f}{d\theta_S} = \frac{\alpha_f}{\alpha_f + \rho_{L_0}/\lambda_L} \left( \sqrt{2} \sin \theta_1 \right) + \left( \gamma_D - \rho_D \right) \frac{\alpha_f}{\alpha_f + \rho_{L_0}/\lambda_L} \left( \sqrt{2} \sin \theta_1 \right)$$

$$\frac{d\alpha_f}{d\theta_S} = \frac{\alpha_f}{\alpha_f + \rho_{L_0}/\lambda_L} \left( \sqrt{2} \sin \theta_1 \right) + \left( \gamma_D - \rho_D \right) \frac{\alpha_f}{\alpha_f + \rho_{L_0}/\lambda_L} \left( \sqrt{2} \sin \theta_1 \right)$$

$$\frac{d\alpha_f}{d\theta_S} = \frac{\alpha_f}{\alpha_f + \rho_{L_0}/\lambda_L} \left( \sqrt{2} \sin \theta_1 \right) + \left( \gamma_D - \rho_D \right) \frac{\alpha_f}{\alpha_f + \rho_{L_0}/\lambda_L} \left( \sqrt{2} \sin \theta_1 \right)$$

1. All the passive components work linearly.

### 3 FORMULATION OF SYSTEM MODEL

#### 3.1 Assumptions

The steady-state analysis is often applied for the class-E converters [36, 38]. The class-E AC–DC converter proposed in this paper works in the time range of switching period. It is difficult to derive the theoretical steady-state waveforms of the line-voltage-period domain. In this paper, numerical analysis is adopted for the proposed converter.

Because of the coexistence of high switching frequency and low line frequency, the system becomes stiff. Therefore, the step interval should be small to derive the waveforms numerically. In this paper, we analyse the converter by the equivalent ideal model and the self-developed numerical program for computation-cost reduction. Figure 3 shows the equivalent model of the proposed converter. For simplifying the converter model, the following assumptions are given.
where the superscript “*” denotes a normalised variable. All the voltages are normalised by the RMS value of the input voltage \( V_i \), for example, \( V_\text{rms} = \frac{v}{V_i} \). Besides, all the currents are normalised by \( V_i \) and rated load resistance \( R_{Lr} \), for example, \( i_\text{rms} = \frac{i}{R_{Lr} V_i} \).

In Equation (5), resistances of the switch \( \rho_S \) and the diode \( \rho_D \) are

\[
\rho_S = \begin{cases} 
\rho_{DS}, & \text{for } 0 \leq \theta_S < 2\pi D_s, \\
\rho_{SD}, & \text{for } 2\pi D_s \leq \theta_S < 2\pi \text{ for } V_i^\ast < -v_\ast^\prime, \\
\infty, & \text{otherwise},
\end{cases}
\]

and

\[
\rho_D = \begin{cases} 
\rho_{D\text{ON}}, & \text{for } V_i^\ast \leq -V_i^\ast, \\
\infty, & \text{otherwise},
\end{cases}
\]

respectively.

### 3.3 Program execution and computation cost

By applying our differential equation solver, whose algorithm is based on the Runge–Kutta method, the transient waveforms of converters can be derived. We execute the program for \( 0 < \theta_L < 100\pi \). It is regarded that the numerical waveforms are in the steady-state at \( \theta_L = 100\pi \).

Performances of commercial software PSPICE and the self-development program are compared in the same environment. Computation times of the PSPICE simulator and our program are 21,920 and 1688 s, respectively, for \( \theta_L = 100\pi \). The computation cost can be dramatically reduced because of the simplified circuit model and self-development numerical program.

### 4 CONTROL SYSTEM

#### 4.1 Frequency modulation control

Generally, the output voltage of the class-E\(^2\) converter is proportional to the input voltage in the steady-state operation. In the proposed AC–DC converter, however, the cutoff frequency of the rectifier is tuned to the line frequency. Therefore, the output voltage does not follow the variation of \( r_B \). As a result, the class-E\(^2\) converter works in the transient state in the time range of the switching period. Namely, the equivalent input resistance of the class-E\(^2\) converter is not constant in the line-voltage-period domain. Figure 5 shows an example of numerical waveforms of the proposed converter with and without input current control. In the case of no input-current control, the input current distorts like a square wave, which means high-order harmonics are included in the input current. It is necessary to meet the restrictions on THD of the input current, such as the IEC-61000-3-2 [40].

On the other hand, the output voltage depends on the load resistance. For example, the output voltage increases as load resistance increases. For regulating the output voltage against load variations, a specific control needs to be applied.

For achieving PF correction, THD reduction, and output voltage regulation, a double-input single-output controller is adopted in the proposed system. There are two loops in the control structure. The inner loop shapes the sinusoidal input current with fast dynamics. The outer loop regulates the output voltage against load variations with a large time constant [41]. The switching frequency of the class-E\(^2\) converter is determined by the controller.

### 4.2 Control circuit

Figure 1 includes the control circuit. In this research, the digital signal processor (DSP) is adopted as the controller, whose maximum input voltage is \( V_{\text{DD}} \). The output of the DSP is the square-waveform driving signal \( D_s \) with frequency \( f_s \) and fixed on-duty ratio \( D_s \), which is the input of the gate driver. It is necessary to sense output voltage \( v_O \), inverter input voltage \( v_B \), and input-inductance current \( i_C \) determining the switching frequency in the DSP.

The output voltage \( v_O \) is scaled into \( v_{OS} \) by the voltage-divider resistances \( r_{O1} \) and \( r_{O2} \). Because \( r_{O1} \) should be less than \( V_{\text{DD}} \), \( r_{O1} \) and \( r_{O2} \) should be chosen to satisfy

\[
v_{OS} = \frac{V_O r_{O2}}{r_{O1} + r_{O2}} = \mu V_{\text{DD}},
\]

where \( V_O \) is the rated output voltage, and \( \mu < 1 \) is a coefficient for keeping a margin against \( V_{\text{DD}} \).

The inverter input voltage \( v_B \) is scaled into \( v_{BS} \) by the resistances \( r_{B1} \) and \( r_{B2} \). In the ideal operation, the maximum value of \( r_B \) is the amplitude of the input voltage \( V_m \). Therefore, the resistances are determined from

\[
r_{BS} = \frac{V_m r_{B2}}{r_{B1} + r_{B2}} = \mu V_{\text{DD}},
\]

The input-inductance current \( i_C \) is sensed by the resistance \( r_I \). The voltage across \( r_I \) is amplified by the current-sense amplifier into \( v_{IS} \) with the voltage gain \( G_C \). In the ideal operation, namely the pure sinusoid of the input current and the unit PF, the maximum value of \( i_C \) becomes

\[
I_{\text{max}} = \frac{2 V_O^2}{R_{\text{min}} V_m},
\]

where \( R_{\text{min}} \) is the minimum value of the load resistance. Therefore, \( \eta \) is determined by:

\[
r_{IS} = I_{\text{max}} = \eta G_C = \mu V_{\text{DD}}.
\]
In the transient state, however, there is a possibility that the sensed voltage is higher than $V_{DD}$. Therefore, the Zener diodes $D_{z1}$ and $D_{z2}$ with operating voltage $V_Z$ are adopted to the input ports of the DSP to prevent overvoltage, as shown in Figure 1.

4.3 Model of FM control

Figure 4 shows a block diagram in the DSP controller. In this figure, the variable prime symbol “$'$” denotes a discrete-time variable. The DSP controller gives the switching frequency $f_S$.

4.3.1 Output-voltage controller

The outer loop derives the reference of input-current amplitude $I_{ref}^{*}$, which is used for the reference value of the inner control loop. The outer-loop purpose is to regulate the output voltage to $V_{Or}$. It is a fundamental characteristic of the class-E DC–DC converter that the output voltage increases as the input current increases. Therefore, the output voltage is regulated by determining the target value of the input-current amplitude $I_{ref}^{*}$ by PI-1 controller, as shown in Figure 1.

The sensing voltage $v_{OS}^{*}$ is sampled by every 20 periods of the line voltage. After sampling, the scale is restored by multiplying $K_O$. As a result, we obtain

$$v_{OS}^{*}(m) = K_O v_{OS}^{*}(m) = \frac{r_{O1} + r_{O2}}{r_{O2}} V_{OS}(m),$$

for $20m\pi \leq \theta_L < 20(m+1)\pi$, 

where $m$ is a natural number. By using $v_{OS}^{*}(m)$, the input of the PI-1 controller is,

$$v_{e}^{*}(m) = V_{Or} - v_{OS}^{*}(m).$$

The output of the PI-1 controller is the reference value of input inductance current amplitude $I_{ref}^{*}(m)$, which is defined by

$$I_{ref}^{*}(m) = K_{PV} v_{e}^{*}(m) + K_{IV} \sum_{k=0}^{m} v_{e}^{*}(k),$$

where $K_{PV}$ and $K_{IV}$ are the proportional and integral gain coefficients of the PI-1 controller, respectively. The transfer function of the output-voltage controller is

$$G_{P11}(z) = \frac{Z(I_{ref}^{*})}{Z(v_{e}^{*})} = K_{PV} + K_{IV} \frac{z}{z - 1},$$

where $Z$ denotes the Z-transform.

4.3.2 Input-current controller

The purpose of the inner-loop control is to shape the input current with unit PF and no harmonic component, as

$$v_{e}^{*}(m) = I_{ref}^{*} \sin \theta_L.$$

For generating the reference current signal of the inner loop, it is necessary to derive $|\sin \theta_L|$, which is realised by sensing the waveform $v_B$ because $V_m$ is regarded as constant. In the inner loop, the sampling frequency needs to be adjusted to the
switching frequency range. Concretely, the switching frequency is updated every 20 switching periods in the proposed converter. Therefore, from $v_{BS}$, the DSP obtains the reference signal as

$$i_{ref}'(n) = i_{ref}'(m) \times K_S v_{BS}(n)$$

$$\approx i_{ref}'(m) \sin \theta_L$$

for $20\pi \leq \theta_L < 20(n+1)\pi$ (17)

The input of the PI-2 controller is the error between the reference current $i_{ref}'$ and restored input-inductance current, which is

$$i_e'(n) = i_{ref}'(n) - i_{eC}(n) = i_{ref}'(n) - \frac{1}{\eta C_L} i_{IS}'(n)$$

(18)

The output of the PI-2 controller is the normalised switching frequency $\beta'(n)$, which is calculated from

$$\beta'(n) = K_{PC} i_{eC}'(n) + K_{IC} \sum_{k=0}^{n} i_{eC}'(k),$$

(19)

where $K_{PC}$ and $K_{IC}$ are proportional and integral gain coefficients of the PI-2 controller, respectively. Namely, the transfer function of the input-current controller is

$$G_{PI2}(z) = \frac{Z(\beta')}{Z(i_{eC}')} = K_{PC} + K_{IC} \frac{z}{z-1}.$$  (20)

### 4.4 Control parameter determination

In this work, we can adjust the control parameters $K_{PC}$, $K_{IC}$, $K_{PV}$ and $K_{IV}$ based on the developed numerical program. The traditional hand-tuning method for PID controller, Ziegler–Nichols method [40, 41], is adopted in this paper.

Figure 6 shows the algorithm for tuning the control parameters. Firstly, the current-control parameters $K_{PC}$ and $K_{IC}$ are tuned while the outer-control loop is disabled. After that, the outer-control loop parameters are tuned. These steps are repeated until both control loop shows good stability. In Figure 6, we recognise that oscillation of $i_C$ occurs when

$$\Delta i_C^e > 0.05,$$  (21)

where $\Delta i_C^e$ is the peak-to-peak ripple of $i_C^e$ during $\pi/2 < \theta_L < \pi/2 + 40\pi/\alpha_L$. Besides, the oscillation of $v_O$ is detected by

$$\Delta v_O^e > 0.05,$$  (22)

where $\Delta v_O^e$ means the peak-to-peak ripple of $v_O^e$ during $0 < \theta_L < 40\pi$.

### 5 DESIGN STRATEGY

#### 5.1 Problem statement

In the normalised parameters, $\alpha_s$, $\alpha_f$, $\lambda_c$, $Q_f$ and $Q_0$ can be roughly determined. For example, the converter characteristics are almost the same when we elect parameters $Q_0$ and $Q_f$ from the range of $0.1 < Q_f < 10$ and $Q_0 < 0.1$. Additionally, $\lambda_c$ need to be large to ensure the $L_c$ works as a choke inductance, for example $\lambda_c > 10$. The value of $\alpha_L$ is sufficiently large because the switching frequency is much higher than the line frequency. Conversely, $\alpha_f$ should be small, for example, $\alpha_f < 5$ for the reduction of the output voltage ripple. Therefore, the major issue of the proposed converter design is to determine the parameters set $\lambda = [\alpha_s, \gamma_s, \gamma_D]$ for always satisfying the
ZVS condition in the line-voltage period in the specified range of load resistances. If the brute-force method is applied for searching the proper three-parameter set, the computation cost becomes quite high.

5.2 System design method

The class-\(E^2\) AC–DC converter works in the transient state in the switching-period range. Therefore, it is necessary to establish the design method that can guarantee the ZVS operation in the entire line-voltage period against load variations in the steady-state. In this paper, we propose a novel design method for the class-\(E^2\) AC–DC converter for achieving ZVS against input-voltage variations. Figure 7 shows the flowchart of the proposed design procedure.

ZVS achievability of the class-\(E^2\) DC–DC converter against load variations is discussed in [36]. When the converter satisfies the class-E ZVS/ZDS conditions at the nominal load \(R_{Lr}\), the ZVS condition can be maintained at light loads, with the help of FET body diode. However, when the load resistance is smaller than the nominal resistance, the ZVS condition cannot be satisfied. Therefore, for ensuring the ZVS for the whole load-variation range, it is a good strategy to set the smallest load resistance to a nominal resistance, namely \(\rho_L = 1\).

Here, we define the DC voltage-transfer ratio of the uncontrolled class-\(E^2\) DC–DC converter as

\[
M_{DC} = \frac{V_{ODC}}{V_1},
\]

where \(V_{ODC}\) is the output voltage of the uncontrolled converter with DC voltage input \(V_1\). In the previous researches, the class-E AC–DC converters were designed for \(M_{DC} = V_{OD}/V_1\). However, in this case, non-ZVS appeared at a certain range of \(\theta_1\). Our idea is to consider only \(M_{DC}\) as an investigation parameter. When we give \(M_{DC}\), it is possible to determine the parameters

\[
\begin{align*}
\mathbf{z} & = [\alpha_S, \gamma_S, \gamma_D] \\
F(\mathbf{z}) & = \begin{bmatrix} v_{O}^*(2\pi, \mathbf{z}) \\
\frac{dv_{O}^*(\theta_S, \mathbf{z})}{d\theta_S} \big|_{\theta_S = 2\pi} \\
V_{ODC}^*(\mathbf{z}) - M_{DC} \end{bmatrix} = 0.
\end{align*}
\]

The three conditions in Equation (24) mean ZVS condition, ZDS condition, and rated output-voltage satisfaction, respectively. The converter parameters \(\mathbf{z}\) can be obtained by solving the algebraic equations in Equation (24) numerically with the computation techniques presented in [37, 39]. Figure 8 shows the flowchart of the derivation of \(\mathbf{z}\). Because we investigate just

\[
V_{ODC}^*(\mathbf{z}) = \frac{1}{2\pi} \int_0^{2\pi} v_{O}^*(\theta_S, \mathbf{z}) d\theta_S.
\]
only one parameter \( M_{\text{DC}} \), it is quite simple and effective to find the proper parameter set of \( \alpha_S, \gamma_S \) and \( \gamma_D \).

Figure 9(a) shows the ZVS region on the \( \theta_1-M_{\text{DC}} \) space for \( V_{\text{SD}}/V_1 = 1.9 \), \( D_S = 0.5 \), \( \alpha_1 = 5 \times 10^{-5} \), \( \alpha_c = 3 \), \( \lambda_c = 30 \), \( Q_D = 0.5 \), \( Q_F = 0.01 \), and \( \alpha_F = 3 \). The on-resistances of the switching devices are set as \( \rho_{DS} = \rho_{SD} = \rho_{DON} = 0.001 \). Besides, the ESRs of inductances, normalised forward voltages \( V_{SD}^* \) and \( V_F^* \) are set to 0.

We can determine three parameters from Equation (24) for the given \( M_{\text{DC}} \), and the steady-state waveforms of the AC–DC converter are derived numerically from Equation (5). When the anti-parallel diode of the FET is in the on-state at the FET turn-on instant, namely, \( i_S^* < 0 \) at \( \theta_S = 2n\pi \), it is regarded that the ZVS is achieved.

By drawing Figure 9(a), the ZVS region can be comprehended visually. It is seen from Figure 9(a) that non-ZVS occurs in the range of \( 55^\circ < \theta_1 < 90^\circ \) when the converter is designed with \( M_{\text{DC}} = 1.9 \). It is also seen that the ZVS is achieved for the entire line-voltage period if we select \( M_{\text{DC}} \) in the range of \( 2.03 < M_{\text{DC}} < 2.21 \).

Figure 9(b) shows a contour map of the normalised switching frequency \( \beta \) on the \( \theta_1-M_{\text{DC}} \) space. It is seen from this figure that the switching frequency variation range in the line-voltage period is reduced as \( M_{\text{DC}} \) increases. Because Figure 9 is discussed on the normalised parameter space, this figure is valid for any design specification of the AC–DC converter. From Figure 9(a), we pick \( M_{\text{DC}} = 2.1 \) for the concrete converter-parameter design.

### EXPERIMENTAL VERIFICATIONS

#### Specifications and circuit components

In this paper, we implemented the class-E\(^2\) AC–DC converter for battery charger applications. The following specifications are given: RMS value of input line voltage \( V_1 = 100 \) \( \text{V} \), input line frequency \( f_1 = 50 \) \( \text{Hz} \), rated output DC voltage \( V_{\text{Or}} = 190 \) \( \text{V} \), nominal switching frequency \( f_{\text{Sn}} = 1 \) \( \text{MHz} \), and rated output power \( P_0 = 250 \) \( \text{W} \). Output power varies in the range of \( 0.25 < R_f/R_N < 1.0 \). \( L_C = 0.50 \) \( \text{mH} \), \( L_F = 0.84 \) \( \text{mH} \), and \( C_f = 390 \) \( \mu\text{F} \) were set in this experiment.

From the numerical calculation, the maximum values of the voltages across the FET and the rectifying diode are \( V_{\text{DSMax}} = 491 \) \( \text{V} \) and \( V_{\text{FMax}} = 550 \) \( \text{V} \), respectively. Therefore, a TPH3208PS GaN-FET from Transfig was used as the switch device. From datasheet, we obtain permissible drain-to-source voltage \( V_{\text{DSMax}} = 650 \) \( \text{V} \), on-resistance is \( r_{DS} = 0.13 \) \( \Omega \), forward voltage of the body diode \( V_{\text{SD}} = 1.6 \) \( \text{V} \) and on-resistance of body diode \( r_{SD} = 0.14 \) \( \Omega \). Additionally, we used a Rohm SC3302AP SiC Schottky-barrier diode in the class-E rectifier, whose maximum reverse voltage \( V_{\text{FMax}} = 650 \) \( \text{V} \), on-resistance \( r_{DON} = 0.2 \) \( \Omega \), and forward voltage \( V_f = 1.35 \) \( \text{V} \). We selected a KBU8D bridge rectifier from Vishay Semiconductor for rectifying the input line voltage, whose on-resistance per diode is \( r_{DR} = 0.33 \) \( \Omega \).

From the specified \( f_{\text{f}}, R_f \) and \( f_s \), we have the resonant inductance \( L_0 = 17.6 \) \( \text{mH} \). The core material of the resonant inductance was 3F4 from Ferroxcube. The inductance was implemented with two sets of E43/10/28 cores with 0.6 mm air gap. AWG 46 Litz wires with 660 strands were used as the winding wire. The number of turns is \( N_{L,0} = 6 \). The measured self-inductance and ESR of the resonant inductance were 18.0 \( \mu\text{H} \) when \( f_s = 1 \) \( \text{MHz} \) and \( r_s = 0.18 \) \( \Omega \), respectively, at 1 MHz. Similarly, \( L_c \) and \( L_f \) were made, whose self-inductance were \( L_c = 0.50 \) \( \text{mH} \) and \( L_f = 0.82 \) \( \text{mH} \). The ESRs of \( L_c \) and \( L_f \) were \( r_c = 0.15 \) \( \Omega \) and \( r_f = 0.06 \) \( \Omega \), respectively.

From these component parameters, the three parameters of \( \alpha_S, \gamma_S \) and \( \gamma_D \) were re-derived from Equation (24) as \( \alpha_S = 0.66 \), \( \gamma_S = 0.62 \) and \( \gamma_D = 0.73 \).

By applying the control-coefficient tuning method as shown in Figure 6, we derived the control parameters as \( K_{\text{DC}} = -0.01 \), \( K_{\text{IC}} = -0.001 \), \( K_{\text{IV}} = 0.2 \) and \( K_{\text{TV}} = 1.0 \). We adopted the TMS320F28379D Delfino DSP from Texas Instruments as the digital controller, whose input withstand voltage \( V_{\text{DD}} = 3.0 \) \( \text{V} \). The input voltage margin of the DSP was chosen as \( K = 0.7 \). According to Equations (9) and (10), the voltage divider resistances were \( R_{f1} = 30 \) \( \text{k}\Omega \), \( R_{f2} = 470 \) \( \Omega \), \( R_{f3} = 30 \) \( \text{k}\Omega \), and \( r_{O2} = 300 \) \( \Omega \). We adopted a TI INA240A2 current sensor, whose gain is \( C_{\text{C}} = 50 \). Then, the current-sensing resistance is chosen as \( n = 0.01 \) \( \Omega \) according to Equation (11). Furthermore, for over-voltage protection, we selected two Zener diodes PDZ3.0B from Nexperia as \( D_{Z1} \) and \( D_{Z2} \), whose operating
TABLE 1 Design specification and component values

|   | Designed | Measured | Difference |
|---|----------|----------|------------|
| $V_I$ | 100 V | 100 V | 0.00% |
| $V_O$ | 190 V | 189 V | −0.53% |
| $R_{Lr}$ | 144 $\Omega$ | 144 $\Omega$ | 0.00% |
| $L_C$ | 0.52 mH | 0.50 mH | −3.85% |
| $L_0$ | 17.6 $\mu$H | 18.0 $\mu$H | 2.27% |
| $L_F$ | 0.26 mH | 0.26 mH | 0.00% |
| $C_0$ | 390 $\mu$F | 380 $\mu$F | −2.56% |
| $r_{LC}$ | 0.15 $\Omega$ (100 Hz) | − |
| $r_{LD}$ | 0.18 $\Omega$ (1 MHz) | − |
| $r_{LF}$ | 0.06 $\Omega$ (100 Hz) | − |
| $r_{DS}$ | 0.13 $\Omega$ | − |
| $r_{SD}$ | 0.14 $\Omega$ | − |
| $r_{DSN}$ | 0.20 $\Omega$ | − |
| $r_{DB}$ | 0.33 $\Omega$ | − |
| $r_1$ | 0.01 $\Omega$ | 0.01 $\Omega$ | 0.00% |
| $r_{b1}$ | 30 $\Omega$ | 30 $\Omega$ | 0.00% |
| $r_{b2}$ | 470 $\Omega$ | 471.6 $\Omega$ | 0.34% |
| $r_{s1}$ | 30 $\Omega$ | 30 $\Omega$ | 0.00% |
| $r_{s2}$ | 300 $\Omega$ | 301.5 $\Omega$ | 0.50% |
| $V_{SD}$ | 0.60 V | − |
| $V_F$ | 1.35 V | − |

voltage is $V_Z = 3.0$ V. Finally, the Renesas EL7104 low-side gate driver generates the gate voltage $v_g$.

Table 1 gives the obtained component values, where all the component values were measured by the Keysight E4990A impedance analyser. Figure 10 shows a photo of the implemented prototype, where the Kikusui PLZ205W electronic load was used as the load device.

FIGURE 10 Photo of the experimental prototype

6.2 Evaluations of experimental measurements

Figure 11 shows numerical and experimental waveforms of line-voltage-period domain at the rated load for $P_O = 250$ W, where the experimental waveforms were measured by Tektronix MSO-54 oscilloscope with the TCP0030A current probe. It can be seen that the output voltage is kept at the rated output voltage $V_{O_r}$. It is also seen that the waveforms of input current $i_I$ look almost pure sinusoidal. These results showed the validity of the control loops of the proposed FM control system.

Figure 12(a) shows PF and THD of the input current as a function of the output power. The THD of the input current is defined as [38]

$$\text{THD} = \sqrt{\sum_{k=0}^{40} \frac{i_k^2}{i_1}},$$

where $i_{1k}$ means the RMS value of the $k$th harmonic current of $i_I$, $i_{11}$ means the fundamental frequency component. Besides, PF is defined as

$$\text{PF} = \frac{\cos \varphi}{\sqrt{1 + \text{THD}^2}},$$

where $\varphi$ is the phase displacement between the input current $i_I$ and input voltage $v_I$. It can be seen from Figure 12(a) that the THD of the input current was in the range from 5.6% to 8.4%, and the PF was larger than 0.995 over the entire load variation range. Figure 12(b) shows harmonic components of $i_I$ at the rated output power with the limitation values set by the IEC 61000-3-2 standard limitation. We can see that all harmonic components met the standard. These results verified the validity of the inner loop of the control system.
Figure 12 shows the converter waveforms of the switching-period domain at the fixed output power and the fixed line-voltage phase. The input voltages of the converter were almost constant from the view of switching-period domain, but the voltage level varies according to $\theta_L$. In this situation, the output was independent of the line voltage. Additionally, it can be confirmed from Figure 13(a–c) that all the switch-voltage waveforms satisfied the ZVS, which proved the accuracy of the ZVS region in Figure 9(a). Besides, we can see from Figure 13(d–f) that all the switch-voltage waveforms also achieved the ZVS at light load. This result showed the validity of the design strategy that we concentrate on the ZVS achievements at the smallest load resistance. Additionally, we confirmed that the experimental waveforms of both line-voltage-period and switching-period domains agreed with the numerical waveforms quantitatively, which showed the effectiveness of the simplified converter model in Equation (5) and the self-development numerical program.

Figure 13 shows the converter waveforms of the switching-period domain at the fixed output power and the fixed line-voltage phase. The input voltages of the converter were almost constant from the view of switching-period domain, but the voltage level varies according to $\theta_L$. In this situation, the output was independent of the line voltage. Additionally, it can be confirmed from Figure 13(a–c) that all the switch-voltage waveforms satisfied the ZVS, which proved the accuracy of the ZVS region in Figure 9(a). Besides, we can see from Figure 13(d–f) that all the switch-voltage waveforms also achieved the ZVS at light load. This result showed the validity of the design strategy that we concentrate on the ZVS achievements at the smallest load resistance. Additionally, we confirmed that the experimental waveforms of both line-voltage-period and switching-period domains agreed with the numerical waveforms quantitatively, which showed the effectiveness of the simplified converter model in Equation (5) and the self-development numerical program.

Figure 14 shows the waveforms against step load variations. It can be seen from the waveforms that the output voltage converged into the rated output voltage against step load variations. Additionally, the turn-on switching voltage is plotted in Figure 14. Although the hard-switching occurred at the sudden load-change instant, the converter recovered the ZVS immediately. We think these non-ZVS and the switching loss are ignorable.

Figure 15 shows the power-conversion efficiency and power-loss breakdown as functions of the output power. Figure 15 shows the power-conversion efficiencies as functions of the output power. For obtaining Figure 15, the power-conversion efficiency is derived by

$$\eta = \frac{P_o}{P_i} = \frac{V_o^2}{R_i P_i},$$

where the input power $P_i$ is derived as

$$P_i = \frac{1}{2\pi} \int_{0}^{2\pi} r_s(\theta_L) v_s(\theta_L) d\theta_L.$$  

In the experiments, the input power was obtained from the Tektronix MSO-54 oscilloscope. Besides, the output voltage was measured by the Iwatsu VOAC7523H digital multimeter.

Even if the system operated at 1 MHz, the implemented converter achieved high power conversion efficiencies, which was 91.4% at the rated load. This is because the ZVS could be achieved in the entire line-voltage period. It is also seen from Figure 15(a) that we can predict the power-conversion efficiency accurately from the equivalent model in Equation (6).

Figure 15(b) shows the power-loss breakdown of the system. In our model, we considered six power-loss factors, namely conduction loss of the FET

$$P_{S} = \frac{1}{2\pi} \int_{0}^{2\pi} \frac{v_s^2(\theta_L)}{R_s(\theta_L)} d\theta_L,$$

conduction loss of the bridge rectifier

$$P_{B} = \frac{1}{2\pi} \int_{0}^{2\pi} \frac{r_B}{R_B} i_C^2(\theta_L) d\theta_L,$$

power loss of the input inductance

$$P_{L} = \frac{1}{2\pi} \int_{0}^{2\pi} \frac{r_{L}}{R_L} i_C^2(\theta_L) d\theta_L,$$

conduction loss of the rectifier diode

$$P_{D} = \frac{1}{2\pi} \int_{0}^{2\pi} \frac{v_D^2(\theta_L)}{R_D(\theta_L)} d\theta_L,$$

power loss of the resonant inductance

$$P_{L0} = \frac{1}{2\pi} \int_{0}^{2\pi} \frac{r_{L0}^2}{R_{L0}} i_{L0}^2(\theta_L) d\theta_L,$$

and power loss of the output inductance $L_F$

$$P_{F} = \frac{1}{2\pi} \int_{0}^{2\pi} \frac{r_{F}}{R_F} i_F^2(\theta_L) d\theta_L.$$
Figure 13: Waveforms of switching-frequency domain. (a–c) At rated load of \( P_O = 250 \text{ W} \). (d–f) At light load of \( P_O = 62.5 \text{ W} \). Blue dashed line: numerical waveforms, black solid line: experiment waveforms. (Horizontal axis: 400 ns/div)

It can be seen from Figure 15(b) that at the heavy load, the power losses were almost proportional to the output power. Therefore, the power-conversion efficiency was almost constant. At the light load, the switch conduction loss \( P_S \) and resonant inductor \( P_L \) were almost independent of output power, which became the main power-loss component at light load.

7 | PERFORMANCE COMPARISON

Table 2 gives the performance comparisons among previous researches on single-switch AC–DC converters. It can be stated from this table that the resonant inductance of the proposed converter is effectively reduced due to the megahertz-frequency operation. However, the magnetic-component power loss increases compared with the 100-kHz converters due to the AC winding losses and the core losses. As a result, the power-conversion efficiency of the proposed converter was almost the same as the others. This result shows the usefulness of the proposed ZVS-achievement design method. From these comparisons, it can be stated that the proposed converter opens the way to the megahertz operation of the AC–DC converters.

8 | CONCLUSION

This paper presented a single-switch ZVS PFC converter based on the class-E\(^2\) converter at 1 MHz switching frequency. A numerical design method for ensuring the ZVS for the entire line-voltage period was proposed. By visualising the ZVS region
TABLE 2  Comparative study among presented researches

| Research | [7] | [8] | [15] | [16] | [21] | [27] | [29] | This work |
|----------|-----|-----|------|------|------|------|------|-----------|
| Year     | 2016| 2016| 2018 | 2019 | 2021 | 2014 | 2019 | 2021      |
| Stage    | 1   | 1   | 1    | 1    | 2    | 1    | 1    | 1         |
| Circuit topology | Buck-boost + SEPIC + Boost + Class-E Inv. + Class-E-D Boost + Boost + Class-E² |
| Maximum output power (W) | 100 | 100 | 100  | 100  | 211  | 102  | 160  | 250       |
| Switching frequency (kHz) | 100 | 100 | 55   | 100  | 90   | 50   | 200  | 1000      |
| Efficiency(%) | 89.5–90.8 | 89.5–91.2 | 89.6–92.5 | 88.0–90.3 | 85–88.3 | 86.0–92.0 | 76–92 | 86.6–91.4 |
| THD(%) | 5.1–8.2 | 5.2–8.2 | N/A  | 2.1–7.6 | 8.8–28 | 10.3 | 6.9  | 5.6–8.4   |
| Resonant inductance | 1400 μH | 1400 μH | 118 μH | 86 μH | 350.95 μH | 300 μH | 100 μH | 17.6 μH   |
| Number of active switches | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Number of diodes (B, excluded) | 6 | 6 | 2 | 4 | 2 | 3 | 2 | 1 |
| Turn-on characteristic of switches | ZCS | ZCS | ZVS | ZVS | ZVS | ZVS | ZVS | ZVS |
| Turn-off characteristic of switches | Hard switching | Hard switching | Hard switching | ZVS | ZVS | ZVS | ZVS |

FIGURE 14  System waveform against step-load variation. Blue dashed line: numerical waveforms, black solid line: experiment waveforms. (Horizontal axis: 1 s/div)

in the parameter space, we can easily obtain circuit parameters to achieve the ZVS for the entire line-voltage period. Therefore, the implemented converter achieved the same level of power-conversion efficiency as the 100-kHz-frequency PFC converter. Additionally, we applied a closed-loop controller for achieving a high PF, low THD of the input current, and output voltage regulation. The experimental circuit always achieved the ZVS in the entire line-voltage period against load variations. As a result, the system delivered a high power-conversion efficiency and a high PF with low THD despite the megahertz operation, which denotes the proposed design-method effectiveness.

The design of the much higher-frequency AC–DC converter at very-high frequency (VHF) band [31–33] and the small-signal analysis of the class-E² AC–DC converter are problems we should address in the future.

FIGURE 15  Converter performance as functions of the output power. (a) Power-conversion efficiency. (b) Power-loss breakdown

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