A configurable qualitative-modeling-based silicon neuron circuit

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Abstract: A silicon neuronal network is a neuro-mimetic system that aims to realize an electronic-circuit version of the nervous system by connecting silicon neuron circuits via silicon synapse circuits. In our previous works, we proposed a qualitative-modeling-based design approach that provides a solution to the trade off in the silicon neuron circuits between the power consumption and the variety of supported neuronal activities. By this approach, we developed an analog silicon neuron circuit that can be configured to Class I, Class II, regular spiking, elliptic bursting, and square-wave bursting modes with power consumption less than 72 nW. Simulation and experimental results for the first 4 modes are reported.

Key Words: qualitative neuronal modeling, silicon neuron, Nonlinear dynamics, low-power circuit, neuromorphic systems

1. Introduction

Neuromorphic systems are of growing significance as a possible basis for the next generation computing systems that satisfy the social and technological demands to energy-efficient, intelligent, and autonomous information processing. Their neuro-inspired or neuro-mimetic architectures intend to exploit the computing principles in the nervous system which is the only existing system that meets those demands. A silicon neuronal network is a neuro-mimetic system that is composed of a network of silicon neuron (SN) circuits connected via silicon synapse circuits. It is a most fine granular approach to the neuromorphic systems and is expected to be able to realize a system comparable to the brain in future. One of the classical but still critical difficulties in this field is the trade-off between the reproducibility of the neuronal activities and the power consumption of the circuit. A wide variety of complex neuronal activities in the nervous system can be modeled precisely by the differential equations that describe the dynamics of the ionic currents and the membrane potential (ionic conductance models). Their direct circuit implementation [1–3] can precisely reproduce the neuronal behavior, but complex and high-power consuming (over 100 μW) circuitry is required because their equations generally have many variables and are composed of complex formulae. For energy-efficient and/or high-density implementation, simpler models are required. A majority of such SN circuits [4–
9] adopt integrate-and-fire (I&F)-based models in which a neuronal spike is treated as an event and the timing of spike generation is described by simple equations. However, it was reported that the neuronal spikes are not uniform in the brain and the variance may play some roles in the information processing [10, 11]. It is also known that the Class II neurons in Hodgkin's classification [12] produce neuronal spikes in a graded manner depending on the stimulus strength (graded response). Thus, there is a possibility that the I&F-based models cannot capture an important aspect of the information processing mechanisms in the brain.

Another class of simple neuronal models has been developed on the basis of the mathematical techniques of qualitative neuronal modeling [13–15]. They are described by simple low-dimensional differential equations but maintain the dynamical structures for neuronal spike generation. For example, the FitzHugh-Nagumo model [16] belongs to Class II in Hodgkin's classification and produces the graded response. The qualitative models help understanding of the mechanisms because they generally are described by simple polynomial expressions. We proposed to design a qualitative SN model that is described by formulae of characteristics curves of elemental circuits with desired features such as low-power consumption and simplicity. We have been developing low-power analog very-large-scale integrated (aVLSI) circuit SNs on the basis of this approach [18–27]. They can support multiple classes of neuronal activities by selecting appropriate voltage parameters after fabrication. One of our low-power analog SN circuits reported in [19, 20, 22, 24] consumes less than 72 nW and can be tuned for Class I/II in Hodgkin’s classification, regular spiking (RS), square-wave bursting, and elliptic bursting (EB). Two ultra-lower power circuits designed by a similar approach are reported in [28, 29]. They realized power consumption more than one order of magnitude lower than our circuit (about 3 nW) by designing dedicated circuits for a simple neuronal class; one is dedicated to Class I and another to Class II.

In [17, 19, 22, 24], we explained the square-wave bursting mode of our circuit. In this article, we report detailed simulation and experimental results of our circuit in its Class I, Class II, RS, and EB modes which were partially explained in [19, 20, 22]. In the next section, the ideal model of our SN is explained and its simulation results are reported. Bifurcation analysis and numerical integration in this section were performed using the XPPAUT software. Experimental results are shown in section 3, which is followed by concluding remarks.

2. Silicon neuron model

The model of our circuit was designed by combining the formulae of the input-output characteristic curves of low-power elemental circuits composed of subthreshold metal-oxide semiconductor field-effect transistors (MOSFETs) which have been traditionally used in low-power SN circuits. Its equations are

\[
C_v \frac{dv}{dt} = -g(v) + f_m(v) - n - q + I_a + I_{\text{stim}},
\]

\[
\frac{dn}{dt} = \frac{f_n(v) - n}{\tau_n},
\]

\[
\frac{dq}{dt} = \frac{f_q(v) - q}{\tau_q},
\]

where \(v, n, \) and \(q\) represent the membrane potential, the fast dynamics, and the slow dynamics, respectively [19]. The first two variables compose the fast subsystem that generates neuronal spikes and \(q\) provides a slow negative feedback to it. Parameter \(C_v\) is the membrane capacitance. Parameters \(\tau_n\) and \(\tau_q\) are the time constants of \(n\) and \(q\), respectively, thus \(\tau_q \gg \tau_n\). Parameter \(I_a\) is a constant current. Functions \(f_x(v) (x = m, n, q)\) and \(g(v)\) are the formulae of the idealized \(V-I\) characteristic curves of the differential pair and transconductance amplifier circuits, respectively. The former is an increasing sigmoidal function and the latter is a shallower decreasing sigmoidal function. Combination of these two sigmoidal functions realizes the reversed \(N\)-shaped \(v\)-nullcline, which is typical in the neuronal models. Refer to Eqs. (4) and (5) in [19] for the equations of \(f_x(v)\) and \(g(v)\).
2.1 Class I mode

Figure 1(a) illustrates the $v$-$n$ phase plane of our model when they are configured to Class I. In this setting, $q$ is fixed to zero. As seen in the figure, one of the three equilibrium points, $(T)$, is a saddle point whose unstable manifolds are attracted to the stable point $(S)$ which corresponds to the resting state. The third equilibrium point $(U)$ is unstable. The $v$-nullcline is displaced upward by application of a sustained stimulus current $I_{\text{stim}}$, which induces a saddle-node on invariant circle bifurcation (Fig. 1(b)). Stable equilibria and stable limit cycles correspond to resting and periodically spiking states, respectively. Because the stable limit cycle generated via this bifurcation has an arbitrarily long period near the bifurcation point, our model in this setting meets the definition of Class I, namely ability to generate spikes with arbitrarily low frequency in response to a sufficiently weak sustained stimulus (see Fig. 1(e)).

We simulated pulse stimulus responses to verify that our model in this mode has the basic property of the excitable cells: (i) a spike is generated when the membrane potential is over a threshold voltage, and (ii) the threshold voltage rises for a while after spike generation. Figure 1(c) plots single pulse stimulus responses. A spike is generated only when the membrane potential exceeds a threshold by sufficiently strong stimulus (property (i)). Because a spike is generated when $v$ is pushed up to $-50.4$ mV by the pulse stimulus whose intensity is $0.2$ nA, the threshold voltage is estimated to be less than this voltage. Figure 1(d) shows the double pulse stimulus responses. The first pulse is $0.3$ nA and the second pulse is applied at $t = 15$ ms. The threshold voltage is estimated to be above $-49.5$ mV because no spike is generated when $v$ rises to this voltage in response to the second pulse stimulus whose intensity is $0.38$ nA. This indicates the threshold effect is enhanced by generation of a spike
2.2 RS mode

Our model is configured to RS by activating the equation of $q$ and maintaining the other settings. Figure 2(a) illustrates the $v-q$ plane in this mode. The left-right reversal of Fig. 1(b) appears on this plane because $q$ acts as a negative stimulus current. The $q$-nullcline crosses the stable equilibrium point of the fast subsystem at (S). It is the only stable state of this system and corresponds to the resting state. When an excitatory sustained stimulus $I_{\text{stim}}$ is applied, the dynamical structure in the fast subsystem is displaced rightward (Fig. 2(b)). The resting state (S) is lost and the state point is attracted to the fast subsystem’s stable limit cycle. While the state point is on it, $q$ starts to increase slowly. Note that $\frac{dq}{dt}$ is positive (negative) above (below) the $q$-nullcline. The period of the limit cycle becomes arbitrarily long when the state point approaches the saddle-node on invariant circle bifurcation point. Thus, the spike frequency decreases as $q$ increases. The system state converges to a closed orbit where the amount of the increase of $q$ while the state point stays above the $q$-nullcline balances with that of the decrease while it is below the $q$-nullcline. This dynamics induces the spike frequency adaptation as shown in Fig. 2(c), which is the core characteristics of RS. In this figure, it can be seen that the spike frequency converges to a higher value if the sustained stimulus is more intense, which is also a feature of RS [30]. The amount of displacement of the dynamical structure in the fast subsystem is increased and the system state converges to a limit cycle more distant from the bifurcation point.

2.3 Class II mode

Figure 3(a) illustrates the $v-n$ phase plane of our model when they are configured to Class II. In this setting, $q$ is fixed at zero. As seen in the figure, the sole equilibrium point (S) is a stable point, which
corresponds to the resting state. The $v$-nullcline is displaced upward by application of a sustained stimulus current $I_{stim}$, which induces a subcritical Hopf bifurcation (Fig. 3(b)). In this case, no dynamical structure that extends the period of the limit cycle up to infinity exists. Thus, our model in this setting meets the definition of Class II, accompanied with a relatively narrow range with a lower limit of the spike frequency in the periodic spiking in response to a sustained stimulus (see Fig. 3(e)).

Simulation results of the single pulse stimulus response are shown in Fig. 3(c). A spike is generated only when the membrane potential rises sufficiently (property (i)), although a threshold voltage cannot be defined clearly because of its graded responses. Figure 3(d) shows the double pulse stimulus responses. The first pulse is 0.35 nA and the second pulse is applied at $t = 8$ ms. When the intensity of the second stimulus is 0.467 nA, it pushes up the membrane potential to $-22.4$ mV. The membrane potential is risen to $-22.4$ mV when the intensity of the stimulus is 0.25 nA in the above single pulse responses. As plotted in the figures, the peak of the membrane potential in the double pulse stimulus response is lower than that in the single pulse stimulus response despite $v$ is risen to the same voltage. This indicates the threshold effect is enhanced by generation of a spike (property (ii)).

2.4 EB mode
Our model is configured to EB by activating the equation of $q$, modifying constant current $I_a$, and maintaining the other settings as in the Class II mode. Figure 4(a) illustrates the $v$-$q$ plane in this mode. Because $\frac{dq}{dt}$ is positive (negative) above (below) the $q$-nullcline, $q$ decreases slowly when the state point is on the fast subsystem’s stable focus. It is attracted to the fast subsystem’s stable limit cycle when $q$ exceeds the Hopf bifurcation point and the stable focus is transformed to an unstable
focus. While the state point is on the stable limit cycle, \( q \) slowly increases (decreases) if it is above (below) the \( q \)-nullcline. If the \( q \)-nullcline is carefully configured so that the amount of the increase in a cycle is larger than that of the decrease, spikes are generated repetitively until \( q \) exceeds the fold bifurcation point at which the stable limit cycle vanishes. Then the state point is attracted to the fast subsystem’s stable focus. Alternation of silent and spiking phases produced by the repetition of this process is the mechanism of EB. Parameter \( M_q \) which abstractly represents the density of slow ionic channels on the nerve membrane can control the period of the bursting as shown in Fig. 4(b). Because this parameter specifies the steepness of the \( q \)-nullcline, it controls the distance between the \( q \)-nullcline and the fast subsystem’s stable focus. Large \( M_q \) makes this distance short, which leads to small \( |\frac{dq}{dt}| \) on the fast subsystem’s stable focus. Thus the period of bursting is extended by increase in \( M_q \).

3. Circuit experimental results

Figure 5 (a) illustrates a block diagram of a circuit that implements our model (Eqs. (1)–(3)). Equations (2) and (3) are solved by integrating the output current of the \( f_n \) and \( f_q \) circuits using a current-mode integrator circuit named Tau-cell [31] (the blue blocks in the figure). Variables \( n \) and \( q \) are coded by their output currents, \( I_n \) and \( I_q \), respectively. Equation (1) is solved by integrating
Fig. 6. Measurement circuits. (a) Circuit diagram. The integrated voltage follower circuit is composed of a 2-stage opamp. The off-chip voltage follower circuit is composed of OPA 376 (TI corp). The ADCs are PXI-5922 (NI corp) and the electrometer is 8240 (ADC corp). The parameter voltage generators (not shown) are PXI-6733 (NI corp). (b) Integrated high impedance circuit.

the output currents of these two Tau-cell, the $f_m(v)$, $g(v)$, and $I_a$ circuits. Thus, $v$ is coded by the voltage across $C_v$. Refer to Fig. 1 in [19] for the circuitry of the $f_x(v)$, $g(v)$, and Tau-cell circuits. The equation for the Tau-cell circuit is described in Eq. (6) in this reference. A transconductance amplifier is utilized for the $I_a$ circuit. Stimulus current $I_{st}$ is also generated by a transconductance amplifier, whose differential input voltage is $V_{st}$. We fabricated this circuit using a Taiwan Semiconductor Manufacturing Company 0.35 μm mixed-signal CMOS process. This circuit may be made smaller if a finer process is used, because the device mismatch can be compensated after fabrication by utilizing the parameter tuning procedure described below. Its micrograph is shown in Fig. 5(b).

Each parameter in the model is controlled by a corresponding parameter voltage that is applied externally to the circuit. The parameter voltages can be calculated from the parameters for simulations, but they have to be compensated for each circuit instance to cancel the second effects of the transistors and the effect of fabrication mismatch. The voltage clamp amplifier circuit at the top of the block diagram facilitates the compensation process. It is activated by closing SW_v and opening SW_n and SW_q (the nullcline mode). In this setting, the output current of the amplifier clamps $v$ at a value specified by $V_c$. The $v$-, $n$-, and $q$-nullclines are measured by observing $I_v$, $I_n$, and $I_q$ while $V_c$ is swept. Current mirror circuits that copy these currents are incorporated for this measurement. In the normal mode where SW_v is open and SW_n and SW_q are closed, bifurcation diagrams of stable states in the fast subsystem can be drawn by sweeping the bifurcation parameter step by step and observing the behavior of $v$ and $I_n$ at each step. We can tune the parameter voltages so that the shape of the nullclines, their relationship and the bifurcation structure mimic those in the model.

Figure 6(a) illustrates the measurement setup for our circuit. The Tau-cells and voltage clamp amplifiers have two additional mirrored current outputs for measurement. One of them is connected to a package pin, which is directly connected to an electrometer. The other is connected to a high impedance circuit which converts the current to a voltage. This voltage as well as the membrane potential ($v$) is buffered by an integrated voltage follower circuit whose output is buffered by an off-chip voltage follower circuit and then measured by an A/D converter (ADC). The high impedance circuits are composed of a transconductance amplifier (see Fig. 6(b)). It is composed of a transconductance circuit whose input transistors are with source degeneration which expands its linear range. The voltage applied to $V_{ofst}$ and the tail current $I_C$ specify the offset of the output voltage and the conductance, respectively. Because the scale of the output currents of the Tau-cells and voltage clamp amplifiers are very small (below about 1 nA), its off-chip measurement requires a long time. Before the evaluation of our circuit, we measured both the direct and voltage-converted outputs of the Tau-cells and the voltage clamp amplifiers by scanning $v$ using the voltage clamp technique. This gives a correspondence table by which the current is obtained from the voltage measured by the
Fig. 7. Experimental results in a Class I setting. (a) \(v\)- and \(n\)-nullclines. (b) and (e) bifurcation diagrams of \(v\) and the spike frequency where sustained stimulus is the bifurcation parameter. (c) and (d) pulse stimulus responses. The time width of the pulse stimulus is 1 ms. The first pulse is applied at \(t = 0\). In (d), \(V_{\text{stim}} = 40\, \text{mV}\) for the first pulse and the second pulse is applied at \(t = 11.5\, \text{ms}\).

 ADC. The parameter voltages are generated by multichannel D/A converters. For measurement of power consumption, the Vdd terminal for the silicon neuron circuit is connected to a semiconductor parameter analyzer. The time average of the consumed current over about 5 seconds was calculated for 50 times. The power consumption was calculated by multiplying their average by the power supply voltage (3.3 V). Connection between the printed circuit board (PCB) and the measurement instruments is with a standard shield connected to the ground. The PCB was placed in an air-conditioned booth whose temperature is kept at 27 °C without any noise shielding.

3.1 Class I mode

Figure 7(a) shows the measured nullclines in a Class I setting. In this setting, the \(q\) block is disactivated by opening SW\(_q\). In this figure the two nullclines cross each other at only one point unlike in Fig. 1(a). Mismatch in the current mirror circuits that copy \(I_v\) and \(I_n\) induces offset and amplitude errors in the \(v\)- and \(n\)-nullclines. The offset error can roughly be canceled by vertically shifting the measured \(v\)-nullcline so that it crosses the \(n\)-nullcline at a point that corresponds to the resting state which can be measured in the normal mode. However, because the amplitude error is difficult to be compensated, delicate structures such as multiple crossing points between the two nullclines close to each other are not always measured correctly. This limitation can be covered by drawing a bifurcation diagram. In this setting, we observed a stable limit cycle that appears just after the disappearance of the resting state (Fig. 7(b)) and the spike frequency could be reduced to very low by applying a sufficiently weak stimulus (Fig. 7(e)). These results allowed us to confirm that our circuit was configured to Class I.

Single pulse stimulus responses in this setting are shown in Fig. 7(c). A spike is generated only when \(v\) exceeds a threshold voltage in the same manner as in Fig. 1(c). When stimulus intensity \(V_{\text{stim}}\)
Fig. 8. Experimental results in a Class II setting. (a) $v$- and $n$-nullclines. (b) and (e) bifurcation diagrams of $v$ and the spiking frequency where sustained stimulus is the bifurcation parameter. (c) and (d) pulse stimulus responses. The time width of the pulse stimulus is 1 ms. The first pulse is applied at $t = 0$. In (d), $V_{\text{stim}} = 30$ mV for the first pulse and the second pulse is applied at $t = 9$ ms.

was 24 mV, $v$ reached $-47.1$ mV at the end time of the stimulus and a spike was generated, whereas $v$ reached $-48.2$ mV and no spike was generated when $V_{\text{stim}}$ was 23 mV (not shown in the figure). Thus the threshold voltage is estimated to be between $-48.2$ mV and $-47.1$ mV. In the double pulse stimulus responses shown in Fig. 7(d), no spike was generated if the second pulse intensity was 42 mV. Because $v$ was $-44.3$ mV at the end time of the second pulse stimulus, the threshold is estimated to be above this value. This indicates that the threshold voltage is risen by spike generation.

In this setting, the average power consumption was about 44 nW.

3.2 Class II mode

Figure 8(a) illustrates the $v$- and $n$-nullclines observed in a Class II setting. The $q$ block is disactivated in this setting. They cross each other at only one point in the same manner as in the ideal model (Fig. 3(a)). In Figs. 8(b) and (e), ‘+’ marks represent the transition of measured stable states when the sustained stimulus $V_{\text{stim}}$ was increased step by step. A stable limit cycle appeared just after the disappearance of the resting state as in the case of Class I setting, however, the spiking frequency could not be reduced below 60 Hz. Another plot marked with ‘×’ in these figures represents the transition when the stimulus was decreased step by step. The bifurcation point from a stable limit cycle to the resting state was about 1 mV smaller than that in the plot with ‘+’ marks. In this bistability region, the $v$ coordinate of the resting state was between the upper and lower limits of the limit cycle. Thus we can confirm that the resting point disappeared via a subcritical Hopf bifurcation in the plot with ‘+’ marks.

Single pulse stimulus responses in this setting are shown in Fig. 8(c). A spike is generated only when sufficiently intense stimulus is applied in the same manner as in Fig. 3(c). When stimulus intensity
Fig. 9. Activities in RS and EB modes.

$V_{\text{stim}}$ was 24 mV, $v$ reached $-40.7$ mV at the end time of the stimulus and a moderate spike was generated. In the double pulse stimulus responses shown in Fig. 8(d), $v$ rose beyond this voltage but no spike was generated if the second pulse intensity was 65 mV. This indicates that the threshold effect was enhanced by generation of a spike.

In this setting, the average power consumption was about 67 nW.

3.3 RS and EB modes

By activating the $q$ block (closing $\text{SW}_q$) while maintaining the fast subsystem in a Class I mode, we realized RS (Fig. 9(a)). The spiking frequency converges to a higher value in response to a stronger sustained stimulus in the same manner as in the simulation results (Fig. 2(c)). In the case that the fast subsystem was in the Class II mode, appropriate configuration of the $q$ block induced EB (Fig 9(b)).

The bursting activity was varied by the effect of noises but the period between bursts is generally extended by increase of parameter voltage $q_{\text{ChSM}}$. This voltage is applied to the gate terminal of a transistor ($M_0$ in Fig. 1(b) in [19]) which controls the tail current for the transconductance amplifier in the $f_q(v)$ circuit. This tail current corresponds to $M_q$ in the ideal model.

If the $v$-$q$ plane of the circuit can be drawn, the parameter voltages related to the $q$ block can be efficiently configured taking note of the geometrical relationship between the fast subsystem’s structures and the $q$-nullcline. The fast subsystem’s structures can be drawn on the $v$-$q$ plane by projecting the bifurcation diagram of $v$. However, because our circuit is not equipped with a circuitry for measurement of $I_{\text{stim}}$ which is generated by an integrated $V-I$ converter circuit, we could not draw the dynamical structures in the fast subsystem on the $v$-$q$ plane. In above settings, we imagined the $v$-$q$ plane by converting $V_{\text{stim}}$ to $q$ using circuit simulation results.

The average power consumption was about 71 nW in the EB mode. The circuit was damaged before measuring the power consumption in the RS mode, but we roughly estimate that it was about 48 nW. In the $q$ block, most of the power is consumed by the bias voltage generator for the Tau-cell circuit and this power consumption is constant in the above two modes. Thus, we can estimate that the power consumption of the $q$ block in the RS mode is similar to that in the EB mode. It is calculated to be about 4 nW by subtracting the power consumption in the Class II mode from that in the EB mode. We added it to the power consumption in the Class I mode.

4. Concluding remarks

We developed a low-power SN circuit by applying the mathematical techniques utilized in the qualitative neuronal modeling. Its ideal model was designed by combining the formulae of the input-output characteristic curves of low-power elemental circuit blocks composed of subthreshold MOSFETs. This approach allowed us to design a simple circuitry in which the dynamical structures for various neuronal activities are implemented. We reported analysis results of the ideal model and experimental results of the fabricated circuit. Our SN model and circuit could be configured to Class I, Class
II, RS, and EB modes by selecting appropriate parameter values. The voltage clamp amplifier and current mirror circuits were incorporated to our circuit for configuration of its parameter voltages. In spite of their unavoidable errors and limitations, they could facilitate their tuning procedures. This procedure has to be automated when a number of our SN circuits is integrated in a silicon neuronal network. An automatic parameter tuning procedure was proposed in [1] which utilizes the differential evolution method to find an appropriate parameter set. We are working on similar algorithm that exploits the data of the nullclines obtained by the voltage clamp amplifier.

The power consumption of our circuit was less than 72 nW. As described in introduction, this value is far lower than the power consumption of [1–3], but is more than one order of magnitude higher than that of the ultra-low power Class I and Class II SNs designed by a similar approach in [28, 29]. To bridge this gap, we are developing an SN circuit that consumes about one order of magnitude lower [18]. We aim to reduce the power consumption penalty for the configurability down to several nanowatts.

Another issue in ultra-low power analog SNs is their temperature dependency. This is because the characteristics of the subthreshold MOSFET, which is used in many SNs, is not negligible. The experimental results in this article were obtained keeping the air temperature at 27 °C. For application of silicon neuronal networks, it is important to solve this issue. Taking advantage of the configurability of our circuit, we are trying to develop an algorithm that compensates the effect of temperature change by dynamically tuning the parameter voltages [32].

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References
[1] F. Grassia, L. Buhry, T. Levi, J. Tomas, A. Destexhe, and S. Saïghi, “Tunable neuromimetic integrated system for emulating cortical neuron models,” Frontiers in NEUROSCIENCE, vol. 5, no. 134, pp. 1–12, December 2011.
[2] J. Schemmel, D. Brüderle, A. Grubl, M. Hock, K. Meier, and S. Millner, “A wafer-scale neuromorphic hardware system for large-scale neural modeling,” Proceedings of 2010 IEEE International Symposium on Circuits and Systems, pp. 1947–1950, May 2010.
[3] M.F. Simoni and S.P. DeWeerth, “Two-dimensional variation of bursting properties in a silicon-neuron half-center oscillator,” IEEE Transactions on Neural Systems and Rehabilitation Engineering, vol. 14, no. 3, pp. 281–289, September 2006.
[4] N. Qiao, H. Mostafa, F. Corradi, M. Osswald, F. Stefanini, D. Sumislawsk, and G. Indiveri, “A reconfigurable on-line learning spiking neuromorphic processor comprising 256 neurons and 128K synapses,” Frontiers in Neuroscience, vol. 9, no. 141, pp. 1–17, April 2015.
[5] C. Mayr, J. Partzsch, M. Noack, S. Hänsche, S. Scholze, S. Höppner, G. Ellguth, and R. Schüffny, “A biological-realtime neuromorphic system in 28 nm CMOS using low-leakage switched capacitor circuits,” IEEE Transactions on Biomedical Circuits and Systems, vol. PP, no. 99, pp. 1–12, February 2015.
[6] S. Moradi and G. Indiveri, “An event-based neural network architecture with an asynchronous programmable synaptic memory,” IEEE Transactions on Biomedical Circuits and Systems, vol. 8, no. 1, pp. 98–107, June 2014.
[7] P.A. Merolla, J.V. Arthur, R. Alvarez-Icaza, A.S. Cassidy, J. Sawada, F. Akopyan, B.L. Jackson, N. Imam, C. Guo, Y. Nakamura, B. Brezzo, I. Vo, S.K. Esser, R. Appuswamy, B. Taba, A. Amir, M.D. Flickner, W.P. Risk, R. Manohar, and D.S. Modha, “A million spiking-neuron integrated circuit with a scalable communication network and interface,” Science, vol. 345, no. 6197, pp. 668–673, August 2014.
[8] A. Cassidy, J. Georgiou, and A.G. Andreou, “Design of silicon brains in the nano-CMOS era: Spiking neurons, learning synapses and neural architecture optimization,” Neural Networks,
vol. 45, pp. 4–26, September 2013.

[9] J.V. Arthur and K.A. Boahen, “Silicon-neuron design: A dynamical systems approach,” IEEE Transactions on Circuits and Systems–I, vol. 58, no. 5, pp. 1034–1043, May 2011.

[10] Y. Shu, Y. Yu, J. Yang, and D.A. McCormick, “Selective control of cortical axonal spikes by a slowly inactivating $K^+$ current,” PNAS, vol. 104, no. 27, pp. 11453–11458, July 2007.

[11] H. Alle and J.R.P. Geiger, “Combined analog and action potential coding in hippocampal mossy fibers,” Science, vol. 311, pp. 1290–1293, March 2006.

[12] A.L. Hodgkin, “The local electric changes associated with repetitive action in a non-medullated axon,” The Journal of Physiology, vol. 107, no. 2, pp. 165–181, March 1948.

[13] X.-J. Wang and J. Rinzel, “Oscillatory and bursting properties of neurons,” In The Handbook of Brain Theory and Neural Networks, ed. Michael A Arbib, 2nd, pp. 835–840, MIT Press, MA, 2003.

[14] E.M. Izhikevich, Dynamical Systems in Neuroscience, The MIT Press, MA, 2007.

[15] J. Rinzel and B. Ermentrout, “Analysis of neural excitability and oscillations,” In Methods in Neural Modeling, eds. Christof Koch and Idan Segev, 2nd, chapter 7, pp. 251–291, MIT Press, MA, 1998.

[16] R. FitzHugh, “Impulses and physiological states in theoretical models of nerve membrane,” Biophysical Journal, vol. 1, no. 6, pp. 445–466, July 1961.

[17] T. Kohno, M. Sekikawa, J. Li, T. Nanami, and K. Aihara, “Qualitative-modeling-based silicon neurons and their networks,” Frontiers in NEUROSCIENCE, vol. 10, Article 273, 2016.

[18] T. Kohno and K. Aihara, “A qualitative-modeling-based low-power silicon nerve membrane,” Proceedings of 21st IEEE International Conference on Electronics Circuits and Systems, pp. 199–202, December 2014.

[19] T. Kohno and K. Aihara, “Silicon neuronal networks towards brain-morphic computers,” IEICE NOLTA Journal, vol. E5-N, no. 3, pp. 1–12, July 2014.

[20] M. Sekikawa and T. Kohno, “Bifurcation structure of a class 2 silicon nerve membrane integrated circuit,” Proceedings of the 2012 International Symposium on Nonlinear Theory and its Applications, pp. 824–827, October 2012.

[21] T. Kohno and K. Aihara, “Reducing a fluctuation in burst firing of a square-wave burster silicon neuron model,” Proceedings of Physcon 2011, IPACS Electronic Library, http://lib.physcon.ru/doc?id=8b4e8b1b12f1, September 2011.

[22] T. Kohno and K. Aihara, “A mathematical-structure-based aVLSI silicon neuron model,” Proceedings of the 2010 International Symposium on Nonlinear Theory and its Applications, pp. 261–264, September 2010.

[23] M. Sekikawa, T. Kohno, and K. Aihara, “An integrated circuit design of a silicon neuron and its measurement results,” Journal of Artificial Life and Robotics, vol. 13, no. 1, pp. 116–119, December 2008.

[24] T. Kohno and K. Aihara, “A simple aVLSI burst silicon neuron circuit,” Proceedings of the 2008 International Symposium on Nonlinear Theory and its Applications, pp. 556–559, September 2008.

[25] T. Kohno and K. Aihara, “A design method for analog and digital silicon neurons –Mathematical-model-based method–,” AIP Conference Proceedings, vol. 1028, pp. 113–128, July 2008.

[26] T. Kohno and K. Aihara, “Mathematical-model-based design method of silicon burst neurons,” Neurocomputing, vol. 71, no. 7–9, pp. 1619–1628, March 2008.

[27] T. Kohno and K. Aihara, “A MOSFET-based model of a Class 2 Nerve membrane,” IEEE Transactions on Neural Networks, vol. 16, no. 3, pp. 754–773, May 2005.

[28] S. Brink, S. Nease, and P. Hasler, “Computing with networks of spiking neurons on a biophysically motivated floating-gate based neuromorphic integrated circuit,” Neural Networks, vol. 45, pp. 39–49, September 2013.

[29] A. Basu and P.E. Hasler, “Nullcline-based design of a silicon neuron,” IEEE Transactions on Circuits and Systems I, vol. 57, no. 11, pp. 2938–2947, November 2010.
[30] M. Pospischil, M. Toledo-Rodriguez, C. Monier, Z. Piwkowska, T. Bal, Y. Frégnac, H. Markram, and A. Destexhe, “Minimal Hodgkin-Huxley type models for different classes of cortical and thalamic neurons,” *Biological Cybernetics*, vol. 99, no. 4–5, pp. 427–441, November 2008.

[31] A. van Schaik and C. Jin, “The Tau-Cell: a new method for the implementation of arbitrary differential equations,” *Proceedings of IEEE International Symposium on Circuits and Systems 2003*, pp. 569–572, May 2003.

[32] E. Green and T. Kohno, “Compensating temperature-dependent characteristics of a subthreshold-MOSFET analog silicon neuron,” *Proceedings of International Conference on Artificial Life and Robotics 2016*, pp. 116–119, January 2016.