

HWGN$^2$: Side-channel Protected Neural Networks through Secure and Private Function Evaluation

Mohammad Hashemi
mhashemi@wpi.edu
Worcester Polytechnic Institute
Worcester, MA, USA

Domenic Forte
dforte@ece.ufl.edu
University of Florida
Gainesville, FL, USA

Steffi Roy
steffiyroy@ufl.edu
University of Florida
Gainesville, FL, USA

Fatemeh Ganji
fganji@wpi.edu
Worcester Polytechnic Institute
Worcester, MA, USA

Abstract
Recent work has highlighted the risks of intellectual property (IP) piracy of deep learning (DL) models from the side-channel leakage of DL hardware accelerators. In response, to provide side-channel leakage resiliency to DL hardware accelerators, several approaches have been proposed, mainly borrowed from the methodologies devised for cryptographic implementations. Therefore, as expected, the same challenges posed by the complex design of such countermeasures should be dealt with. This is despite the fact that fundamental cryptographic approaches, specifically secure and private function evaluation, could potentially improve the robustness against side-channel leakage. To examine this and weigh the costs and benefits, we introduce hardware garbled NN (HWGN$^2$), a DL hardware accelerator implemented on FPGA. HWGN$^2$ also provides NN designers with the flexibility to protect their IP in real-time applications, where hardware resources are heavily constrained, through a hardware-communication cost trade-off. Concretely, we apply garbled circuits, implemented using a MIPS architecture that achieves up to 62.5× fewer logical and 66× less memory utilization than the state-of-the-art approaches at the price of communication overhead. Further, the side-channel resiliency of HWGN$^2$ is demonstrated by employing the test vector leakage assessment (TVLA) test against both power and electromagnetic side-channels. This is in addition to the inherent feature of HWGN$^2$; it ensures the privacy of users’ input, including the architecture of NNs. We also demonstrate a natural extension to the malicious security model just as a by-product of our implementation.

CCS Concepts
• Security and privacy → Side-channel analysis and countermeasures. Privacy-preserving protocols.

1 Introduction
An ever-increasing number of applications are demanded from machine learning and, in particular, deep learning (DL). These applications include image processing, natural language processing, network intrusion detection systems (NIDSs), biometrics systems, and analysis of medical data – just to name a few cf. [35]. These, among other compute-intensive services, have been supported by cloud platforms equipped with hardware acceleration [11]; however, cloud platforms are not the only hosts of DL algorithms and modules. IoT edge devices have embodied modules to perform many tasks, for instance, image classification or speech recognition as required by wearable devices for augmented reality and virtual reality [34]. In addition to those, so-called mobile and wearable devices, low-cost DL chips (e.g., sensors or actuators) have been employed in cameras, medical devices, appliances, autonomous surveillance, ground maintenance systems, and even toys. In these cases, heavy demands have been put on (always-on) DL-inference accelerators with power constraints, e.g., ARM Cortex-M microcontrollers.

Under DL-inference scenarios, trained neural networks (NNs) are made available to users. To obtain such a trained NN, a large training dataset is used in a time-consuming process to tune NN hyperparameters, which cannot be repeated in a straightforward manner. Therefore, it can be tempting for an adversary to target the DL-inference accelerator and extract those parameters. Besides hyperparameters, the architecture of NNs is another asset to protect as it may (even partially) reveal private information [18, 20] or at least help the adversary to reconstruct the NN [1] cf. [4]. In fact, having the knowledge of the NN architecture allows the adversary to launch power attacks, for instance, cryptanalysis of trained NNs aiming to extract an identical copy of NN models [10]. Since physical access can make it further easier for attackers to reverse-engineer and disclose the assets (i.e., architecture and hyperparameters) corresponding to NNs, usual protections, e.g., blocking binary readback, blocking JTAG access, code obfuscation, etc. could be applied to prevent binary analysis [4]. These, of course, would not stop an attacker from leveraging the information that leaks through side-channels.

Side-channel analysis (SCA) has been widely performed to evaluate the robustness of cryptographic implementations against one of the most dangerous types of physical attacks. SCA has been considered effective and applicable due to its (relatively) low cost and feasibility in real-world conditions, especially, when applied against small embedded devices [66]. Interestingly enough, DL has played an important role in the SCA domain of study by offering competitive performance corresponding to more capable attackers [49]. In doing so, DL can be a double-edged sword: DL implementations have been already come under side-channel attacks [4, 16, 69, 72]. These attacks have resulted in considerable efforts to devise countermeasures. Intuitively, masking schemes developed to protect
cryptographic modules against SCA have been one of the first solutions discussed in the literature [14, 15]. These methods come with their own set of challenges, e.g., being limited to a pre-defined level of security associated with the masking order or even to a particular modality. Moreover, evidently, masking cannot stop the attacker from disclosing the architecture of the NN under attack.

The natural question to be asked is why fundamental cryptographic concepts that can provide NNs with robustness against SCA have not yet been examined. Concretely, secure function evaluation (SFE), specifically garbled circuits evaluation, has been considered to prevent side-channel leakage cf. [28, 43]. Nevertheless, in practice, SFE has not been considered to stop side-channel attacks, perhaps, due to the high overhead initially observed in [28]. This study has attempted to introduce a provably side-channel resistant one-time program [21] implemented on a field-programmable gate array (FPGA). Their implementation is a combination of tamper-resistant SFE, specifically garbled circuits evaluation, and SFE, realized through a general purpose processor cf. [60, 62]. Interestingly enough, as opposed to the argument in [28, 43] suggesting the side-channel resiliency of garbled circuits, Levi et al. have recently demonstrated a side-channel attack against garbling schemes leveraging the free-XOR optimization [37]. HWGN$^2$ is not susceptible to this attack since PFE is taken into account to make the function private. It is noteworthy that the privacy of the NN model is understudied even with their own set of challenges, e.g., being limited to a pre-defined level of security associated with the masking order or even to a particular modality. Moreover, evidently, masking cannot stop the attacker from disclosing the architecture of the NN under attack.

A secure and private DL-inference hardware accelerator, resilient to SCA. To protect the NN model (including its architecture and parameters) against SCA, HWGN$^2$ relies on the principles of private function evaluation (PFE) and SFE, realized through a general purpose processor cf. [60, 62]. Interestingly enough, as opposed to the argument in [28, 43] suggesting the side-channel resiliency of garbled circuits, Levi et al. have recently demonstrated a side-channel attack against garbling schemes leveraging the free-XOR optimization [37]. HWGN$^2$ is not susceptible to this attack since PFE is taken into account to make the function private. It is noteworthy that the privacy of the NN model is understudied even in existing software garbled DL-inference [2, 53, 55]. Interestingly enough, our instruction set-based HWGN$^2$ is model-agnostic. Moreover, in the most cost-efficient setting with a DL-inference realized by using XNOR operators, our implementation does not require any modification to the NN, in contrast to what has been proposed as software garbled DL-inference [53].

Assessment of the effectiveness and cost of SCA protection relying on SFE/PFE. To evaluate the feasibility of our approach, we identify two implementation scenarios, namely (1) resource- and (2) communication-efficient. In the first category, compared to the unprotected NN, the overhead is up to 0.0011$x$ and 0.018$x$ more logical and memory hardware resources, respectively; however, this relatively low overhead is achieved at the cost of communication overhead of about factor $10^6 \times$ compared to an unprotected AES embedded in an FPGA.

Apart from the leakage properties of SFE and its realization garbled circuits, they have been developed to ensure the security of users’ data, when two parties jointly evaluate a known function. Therefore, in a natural way, garbled circuits have been investigated to put forward the notion of privacy-preserving inference-as-a-service [53, 54]. These results are further backed by more theoretical studies that aim to, for instance, heavily optimize garbled circuits to suit TensorFlow classifier descriptions [2]. In spite of these results, the gap between these studies is evident: design of countermeasures against SCA, software implementation of garbled NNs [26, 53, 55], and hardware implementations of garbled circuits [60]. To narrow this gap, this paper introduces HWGN$^2$ (hardware garbled NN) and contributes to the following aims.

- **Comprehensive discussion on various aspect of our design.** Although SCA better fits the specification of an attacker in the honest-but-curious (HbC) setting as defined in cryptography, it is also secure in the presence of malicious (active) adversary [38] as a byproduct of our hardware implementation. Furthermore, we discuss how the implementation of maliciously-secure GCs can form a basis for allowing the user to perform multiple executions [25].

## 2 Adversary Model

Valuable assets of NNs, as intellectual property (IP), include their NN architectures, hyperparameters, and the parameters critical to achieving reasonable accuracy [4]. On the other hand, these NNs might be used in applications in which their inputs contain sensitive information (e.g., medical or defense records [44]). Hence, the security of inputs given to NNs along with the privacy of the networks themselves must be guaranteed. Note that here the definitions of security and privacy are borrowed from SFE- and private function evaluation- (PFE) related literature [6]. Classically, two threat models have been considered in prior works in the contexts of SFE and PFE: (i) semi-honest (so-called Honest-but-curious (HbC)) and (ii) malicious (active) adversary. An HbC adversary is expected to follow the protocol execution and does not deviate from the protocol specifications. To be more specific, the HbC adversary may only be able to learn information without interfering with the protocol execution. On the contrary, a malicious adversary may attempt to cheat or deviate from the protocol execution specifications. In doing so, to extract the information on users’ data, the adversary constructs an arbitrary, well-chosen garbled circuit computing a different function, which cannot be detected due to the garbling [38]. It is evident that this scenario does not match the one describing SCA; however, we will discuss how HWGN$^2$ naturally ensures the
security even in this setting, where NN developers would attempt to violate users’ data security (see Section 7).

In our work, we consider (mainly) the HbC adversary, whose role is played by Bob (i.e., the evaluator), whereas Alice is the garbler [6, 38] (see Figure 1). Following the definition of the attack model presented in the state-of-the-art, e.g., [14, 15], the garbler trains the DL model in an offline fashion, and the evaluator performs the inference. It is important to stress that the hardware implementation encompasses solely the evaluator engine, i.e., neither garbling module nor encryption one is implemented on the hardware platform. To evaluate the garbled DL accelerator, the evaluator feeds her garbled inputs prepared in an offline manner. The evaluator can collect power/EM traces from the device either via direct access or remotely, see e.g., [58, 73]. For this, the evaluator follows a chosen-plaintext-type attack model, where she sends her inputs to the device for classification and readily captures multiple traces. These traces will be then used to launch power/EM-based side-channel attacks [9, 12, 32]. The goal of the garbler is to protect the NN architectures, hyperparameters, and parameters from the HbC evaluator. HWGN fulfills this requirement through SFE/PFE techniques (see Section 5). Moreover, in contrast to prior countermeasures against SCA mounted on NNs, our approach could show resiliency against fault injection and cache/memory attacks (see Section 7 and Appendix A for more information).

3 Related Work

3.1 SCA against NNs

The main goals of side-channel attacks targeting DL hardware accelerators can be: (i) extraction of deep learning model (DL Model) architectures, and (ii) revealing NN parameters (i.e., weights and biases). Table 1 summarizes some of these attacks. In more details, Xiang et al. [69] presented a power side-channel attack to extract the DL Model architecture. For this purpose, they modeled the power consumption of different DL Model components such as pooling, activation functions, and convolutional layers based on how many addition and multiplication those components have. Using these power consumption models, an SVM-based classifier was trained to reveal the DL Model architecture based on the captured power consumption traces when the DL Model runs on the hardware accelerator. This line of research has also been pursued by Batina et al. [4] who introduced an attack scenario based on the EM and timing side-channel to extract the number of layers, the number of neurons in each layer, weights, and activation functions (AF). First, they modeled the timing side-channel of all possible AF (e.g., Relu or Tanh) and extracted the AF used in the NN by comparing the response time of the DL hardware accelerator when it executed the AF and the timing model of each possible AF. This is followed by analyzing EM traces captured when the DL hardware accelerator runs, where the EM patterns determine the number of layers and number of neurons in each layer. By feeding different random inputs to the accelerator and capturing the EM traces, it was made possible to launch a Correlation Power Analysis (CPA) to reveal the weights. In another approach, Breier et al. [8] present a reverse engineering attack to extract the DL model weights and biases (parameters) with the help of fault injection on the last hidden layer of the network.

3.2 Security-preserving DL Accelerators

To protect NNs against SCA, Liu et al. [42] introduced a shuffling and fake memory-based approach to mitigate reverse engineering attacks that increase the run time of a DL hardware accelerator when the depth of the NN increases. Regarding the similarity between SCA launched against cryptographic implementations and DL accelerators, in a series of work, Dubey et al. have proposed hiding and masking techniques to protect NNs [14–16]. Yet, the differences between these implementations make the adaptation of known side-channel defenses challenging; for instance, integer arithmetic used in neural network computations that is different from modular arithmetic in cryptography, which has been addressed in [14, 16]. Despite the impressive achievements presented in these studies, the approaches suffer from the known limitations of masking, i.e., their restriction to a specific side-channel security order. Furthermore, the implementation of masked DL models (i.e., a new circuit should be designed/implemented for different NNs) would be a challenging task. Moreover, masking cannot protect the architecture of DL accelerators.

3.2.1 Garbled Accelerators Table 2 summarizes the most recent frameworks developed with regard to principles of SFE, more specifically, garbling. Among those proposals, GarbledCPU [62] and RedCrypt [55] are of great importance to our work since they consider a hardware implementation of garbled circuits, whereas other relevant studies such as [3, 26, 53, 54, 56, 60] devoted to software-based garbling engine/evaluator.

General-purpose hardware accelerators: In contrast to that, [62] has demonstrated a hardware garbling evaluator implemented on general-purpose sequential processors, where the privacy of NN architectures is also ensured. While benefiting from the simplicity of programming a processor, their design is specific to Microprocessor without Interlocked Pipelined Stages (MIPS) architecture. This has been addressed by introducing ARM2GC framework, where the circuit to be garbled/evaluated is the synthesized ARM processor circuit that can support pervasiveness and conditional execution [61]. The efficiency in terms of hardware resources and communication cost has been reported as well. This is followed by introducing an FPGA-based garbling engine (FASE) that can be further extended to evaluator [27]. FASE is optimized to enable cloud servers to provide secure services to a large number of clients simultaneously without violating the privacy of their data; however, the privacy of circuits (e.g., NN architecture) is not considered in this study.

Hardware DL accelerators: RedCrypt attempts to enable cloud servers to provide high-throughput and power-efficient services to their clients in a real-time manner [55]. For this, FPGA platforms (Virtex UltraScale VCU108) have been used as a garbling core to present an efficient GC architecture with precise gate-level control per clock cycle, which ensures minimal idle cycles. This results in a multiple-fold improvement in the throughput of garbling operation compared to the previous hardware garbled circuit accelerator [60, 62]. In their scenario, a host CPU is involved in an OT to communicate the evaluator labels/input with the client, which may need high bandwidth. Although RedCrypt [55] has achieved significant improvement in computational efficiency, the DL model implemented on the FPGA cannot be easily diversified. Their proposed hardware DL accelerator suits a specific type of DL
Table 1: Summary of most recent side-channel attacks against DL accelerators.

| Paper               | Targets     | Side-channel Modality | Attack Scenario                                                                 | Implementation Platform       |
|---------------------|-------------|-----------------------|--------------------------------------------------------------------------------|-------------------------------|
| Xiang et al. [60]   | DL Model Architecture | Power               | • Modeling the power consumption of different DL hardware accelerator components based on the number of additions and multiplications • Trained a classifier to reveal the DL Model architecture based on the captured power consumption traces | Raspberry Pi                 |
| DeepEM [72]         | DL Model Architecture | EM                   | • Prevention of a layer computations • Finding the number of parameters through each layer based on EM traces | PyTorch                      |
| CSI NN [4]          | DL Model Architecture +Weights +AF | Timing + EM       | • Modeling, all possible AF timing side-channel • Extracting the AF used in the DL Model Architecture • Distinguishing the EM patterns to find the number of layers and neurons • Launching CPA to reveal the weights | ARM Cortex M3 + Atmel ATMega328P |
| Dubey et al. [16]   | DL Model Weights | Power               | • Exploring the power consumption traces from changing status of pipeline registers • Launching a CPA based attack to reveal weights | SAKURA-X FPGA board           |
| Yoshioka et al. [71] | DL Model Weights | Power               | • Launching a CPA based attack to reveal weights | Xilinx Spartan3-A             |

Table 2: Summary of garbled DL accelerators and their features.

| Paper                  | Adversary Model | Approach | Contributions                                                                                     | Implementation Platform       |
|------------------------|-----------------|----------|---------------------------------------------------------------------------------------------------|-------------------------------|
| DeepSecure [56]        | HBC             | Garbling | • Presentation of pre-processing approach • A:proce that would reveal some information about the network parameters and structure of data other than [50] | Intel Core i7 CPUs            |
| Chameleon [54]         | HBC             | Hybrid   | • Performs linear operations using additive secret sharing and nonlinear operations using Yao’s garbled circuit | Intel Core i7 - 4850w CPUs    |
| Bari et al. [2]        | HBC             | Hybrid   | • Improvement of the BMR scheme [1] to support Non-linear operations                               | Intel Core i7 - 4850w CPUs    |
| XONN [53]              | HBC             | Garbling | • Support Binary NNs • Conversion of Matrix Multiplication to XORN PopCount                        | Intel Xeon CPU ES-2650       |
| TinyGarble2 [26]       | HBC + Malicious | Garbling | • Provision of protection against malicious adversary • Allegation garbling memory cost            | Intel Xeon CPU ES-2650       |
| Garblek.FU [52]        | HBC             | Garbling | • Presentation of FPGA accelerator for GC evaluation                                              | Virtex 7 FPGA                 |
| ReSt-Crypt [55]        | HBC             | Garbling | • Minimizing the hardware architecture side channels to achieve scalable garbling                 | Virtex UltraScale VXU1000    |

Table 3: State-of-the-art approaches vs. HWGN² (‘P’arameters Secrecy of DL Model. ‘U’pgradeable to supporting malicious security model. ‘A’rchitecture protection of DL model. ‘C’t. = constant round complexity. ‘I’ = independence of a secondary server). Inspired by [33].

| Approach              | F | U | X | C | P |
|-----------------------|---|---|---|---|---|
| DeepSecure [56]       |   |   |   |   |   |
| Chameleon [54]        |   |   |   |   |   |
| Bari et al. [2]       |   |   |   |   |   |
| XONN [53]             |   |   |   |   |   |
| TinyGarble2 [26]      |   |   |   |   |   |
| ReSt-Crypt [55]       |   |   |   |   |   |
| HWGN² [This paper]    |   |   |   |   |   |

model and is built on the assumption that the network architecture is publicly available, which allows an adversary to launch an SCA attack easier [4]. These shortcomings are tackled by HWGN² that is NN-agnostic and protects the privacy of the DL model, i.e., the secrecy of its architecture. A qualitative comparison between the most state-of-the-art approaches and HWGN² is provided in Table 3. HWGN² shares similarities with TinyGarble2 [26], although it is a software accelerator, whereas HWGN² is a hardware one.

4 Background

4.1 SFE/PFE Protocols

SFE protocols enable a group of participants to compute the correct output of some agreed-upon function f applied to their secure inputs without revealing anything else. One of the commonly-applied SFE protocols is Yao’s garbled circuit [70], a two-party computation protocol. To formalize this protocol, we employ the notions and definitions provided in [6] to support modular and simple but effective analyses. In this regard, a garbling algorithm Gb is a randomized algorithm, i.e., involves a degree of randomness. Gb(f) is a triple of functions (F,e,d) ← Gb(f) that accepts the function f : {0,1}n → {0,1}m and the security parameter k. Gb(f) exhibits the following properties. The encoding function e converts an initial input x ∈ {0,1}n into a garbled input X = e(x), which is given to the function F to generate the garbled output Y = F(X). In this regard, e encodes a list of tokens (so-called labels), i.e., one pair for each bit in x ∈ {0,1}n: En(e,·) uses the bits of x = x1· · ·xn to select from e = (X11, X12, · · · , X1m, X21, · · · , X2m, · · · , Xnm). By reversing this process, the decoding function d generates the final output y = d(Y), which must be equal to f(x). In other words, f is a combination of probabilistic functions d·f o e. More precisely, the garbling scheme G = (Gb, En, De, Eu, ev) is composed of five algorithms as shown in Figure 2, where the strings d,e, f, and F are used by the functions De, En, ev, and Ev (see Section 5 for a concrete protocol flow in the case of NNs).

Security of garbling schemes: For a given scheme, the security can be roughly defined as the impossibility of acquiring any information beyond the final output y if the party has access to (F,X,d). Formally, this notion is explained by defining the side-information function Φ(). Based on the definition of this function, an adversary cannot extract any information besides y and Φ(f) when the tuple (F,X,d) is accessible. As an example of how the function Φ() is determined, note that for an SFE protocol, where the privacy of the function f is not ensured, Φ(f) = f. Thus, the only thing that leaks is the function itself. On the other hand, when a PFE protocol is run, Φ(f) is the circuit/function’s size, e.g., number of gates.

Oblivious transfer (OT): This is a two party protocol where party 2 transfers some information to party 1 (so-called evaluator); however, party 2 remains oblivious to what information party 1 actually obtains. A form of OT widely used in various applications is known as “chosen one-out-of-two”, denoted by 1-out-of-2 OT. In this case, party 2 has bits X0 and X1, and party 1 uses one private input bit s. After running the protocol, party 1 only gets the bit Xs, whereas party 2 does not obtain any information on the value of s, i.e., party 2 does not know which bit has been selected by party 1. This protocol can be extended to support the n-bit case, where party 1 bits x1, · · · , xn are applied to the input of party 2 X0, X1, · · · , Xn to obtain X0, X1, · · · , Xn. This is possible by sequential repetition of the basic protocol [6]. It has been proven that 1-out-of-2 OT is universal for 2-party SFE, i.e., OT schemes can be the main building block of SFE protocols [31].
4.2 Neural Network

Neural Network is one of the main categories of machine learning, which refers to learning a non-linear function through multiple layers of neurons with the goal of predicting the output corresponding to a given input fed to a network trained on a dataset. To perform such prediction, the input is fed to the first layer of the network (so-called input layer), whereas in the next layers (so-called hidden layers) the abstraction of the data takes place. For a multi-layer perceptron (MLP) that is a fully connected NN, each layer’s input (including the input layer) is multiplied by neuron weights, added to the bias, and finally given to a commonly-applied activation functions at the output of each layer (excluding the input layer). The most common activation functions are Sigmoid, Tanh, and Rectified Linear Unit (ReLU). The activation functions that might be used in DL models include linear, Sigmoid, and softmax.

5 Foundations of HWGN

Protocol flow: Here we provide insight into how SFE/PFE schemes can be tailored to the needs of a secure and private DL accelerator. According to the general flow illustrated in Figure 2, the goal of a garbling protocol $G$ is to evaluate a function $f$ against some inputs $x$ to obtain the output $y$. The evaluator (i.e., the attacker) is never in possession of the raw NN binaries. Let $f = f_{NN}$ denote the function corresponding to the NN. The attacker aims to obtain the information on $f_{NN}$ by collecting the side-channel traces. To achieve this, here we give an example of SFE protocol $G$ that has OT at its core and follows Yao’s garbling principle, i.e., the garbling protocol $G = (Gb, En, De, Ev, eo)$ as shown in Figure 2. To execute the protocol, the designer of the NN accelerator (garbler) conducts $(F, e, d) \leftarrow Gb(1^k, f)$ on inputs $1^k$ and $f$ and parses $(X^1_0, X^1_1, \ldots, X^n_0, X^n_1) \leftarrow e$. Afterward, the garbler sends $F$ to the evaluator, i.e., the attacker. In order to perform the function $Eo$, the attacker and the garbler run the OT, where the former has the selection string $x$ and the latter party has already parsed $(X^1_0, X^1_1, \ldots, X^n_0, X^n_1)$. Hence, the evaluator can obtain $X = X^1_0, \ldots, X^n_1$ and consequently, $y \leftarrow De(d, Eo(F, X))$. Note that even with the tuple $(F, X, d)$ in hand, the attacker cannot extract any information besides $y$ and $\Phi(f)$. Moreover, although the NN provider has access to $(F, e, d)$, no information on $x$ leaks. In an inference scenario, $x$ represents the evaluator’s input data. Nevertheless, if $G$ is an SFE scheme, $\Phi(f) = f$.

To construct a PFE scheme protecting the architecture, parameters, and hyperparameters of the NN that relies on the scheme $G$, we first define a polynomial algorithm $\Pi$ that accepts the security parameter $k$ and the (private) input of the party [6]. The PFE scheme is a pair $F = (\Pi, e\Pi)$, where $e\Pi$ is as defined for the garbling scheme (see Section 6 for more information about $\Pi$). The scheme $F$ enable us to securely compute the class of functions $\{ev(f, \cdot) : f \in \{0, 1\}^k\}$, i.e., any function that $G$ can garble. The security of the PFE scheme $F$ relies on the security of the SFE protocol underlying $F$ (see Section 4.1); however, $\Phi(f)$ is the circuit size, i.e., the function $f$ remains private when executing the SFE protocol. In other words, the NN, its architecture, parameters and hyperparameters are now kept private from the attacker.

Oblivious Inference: Oblivious inference tackles the problem of running the DL model on the user’s input without revealing the input or the result to the other party (i.e., garbler in our case). For the latter, another interesting characteristic of SFE/PFE schemes is their ability to adapt to specific scenarios, where the output $y$ should also be protected. This would not be interesting in our case, where the security of the NN against SCA mounted by the evaluator is the objective. Nonetheless, for the sake of completeness, if the decryption of $Y$ should be performed securely, the privacy of inference results can easily be preserved by applying a one-time message authentication code (MAC) to the output and XORing the result with a random input to hide the outcome. These operations can be included in the design of the NN and naturally increase its size and the input fed by the garbler; however, the increase is linear in the number of output bits and considered inexpensive [39].

5.1 Implementation of HWGN

When defining the SFE scheme $F$, it is mentioned that $F$ can securely and privately compute any function, which can be garbled by running the garbling scheme $G$. Our garbled universal circuit $F$ depends on the fact that a universal circuit is similar to a universal Turing machine [23], which can be realized by a general purpose processor cf. [60, 62]. Note the difference between our goal, i.e., realizing $F$, and one achieved in [67]: optimizing the emulation of an entire public MIPS program. Although we implemented a MIPS-based scheme, the prototypes can be extended to ARM processors. HWGN2 garbles the MIPS instruction set with a minimized memory and logical hardware resource utilization (see Section 5.1.1).

Similarities between HWGN2 and TinyGarble2: One of the state-of-the-art GC frameworks is TinyGarble2 [26] offering solely software DL inference, without ensuring the privacy of the NN.
HWGN$^2$ remedies these shortcomings; however, it shares similarities with TinyGarble2, namely regarding the flow of the protocol. The technique presented in TinyGarble2 is based on the division of a large netlist, such as DL models, into $i$ smaller sub-netlists and evaluating them one after another. The size of the sub-netlists could be either one gate or equal to the total number of gates in the $f$ netlist. The fewer gates included in each sub-netlist, the less memory utilization the gates require to be evaluated.

Figure 3 illustrates the flow of HWGN$^2$ in the presence of an HbC adversary (for the extension to the malicious security model, see Appendix A). First, the garbler chooses input encryption labels (e) (Step 1.1). Afterward, instead of sending the complete set of GTs and L to the evaluator, in each cycle the garbler sends the evaluator a subset $G_{Ti}, L_i$ (Step 1.2), and either $e$ (if the sub-netlist includes the gate with the inputs connected to the $f$ netlist) or $X_i$ (the garbled input corresponding to the sub-netlist). These subsets can be prepared offline and independent from the input of the evaluator. The evaluator also garbles its inputs as shown in Step 2, which is done offline as well. In the next step, the evaluator evaluates the gate and sends the garbler the garbled output $Y_i$, i.e., garbled output of the $i^{th}$ sub-netlist (Step 3). This process repeats until all $i$ sub-netlists, excluding the gates whose output is connected to the NN outputs, are evaluated. Then in Step 4, the garbler sends the garbled tables and labels related to the gates that are connected to the NN output (so-called NN output layer). After the evaluator evaluates all output layer-related gates, the garbler sends the decryption label (Step 5) along with the concatenated garbled outputs to the evaluator. Finally, the evaluator decrypts the concatenated garbled output $Y$ and achieves its raw output $y$. Also, instead of sending the complete set of GTs, L, and $e$ through one OT interaction, TinyGarble2 requires one OT interaction per sub-netlist. The trade-off of minimizing the memory utilization using TinyGarble2 is the communication cost.

**What makes HWGN$^2$ superior:** Since HWGN$^2$ is a hardware accelerator, it can benefit from parallelism offered by hardware platforms, e.g., FPGAs. HWGN$^2$, contrary to the previous software and hardware accelerators including TinyGarble family [26, 60], also gives the flexibility of tuning the communication costs and hardware resource utilization to the garbler (e.g., NN provider). In the applications where communication cost poses a limitation (such as real-time applications), one can implement DL hardware accelerators by sending the complete set of GTs, L, and $e$ through one OT interaction. This minimizes the communication cost while hardware resources are utilized at the maximum amount. In contrast, in the application with the limitation of hardware resources, one can use the HWGN$^2$ that implements DL hardware accelerators with the sub-netlist size of one or a small number of gates. This leads to a noticeable strength of the HWGN$^2$: the evaluator has access to neither the netlist (GC mapping file, often comes in Simple Circuit Description, SCD, format [60]) nor all GT and labels at once. Furthermore, scheduling is taken care of on the garbler-side; hence, the scheduler module is not accessible by the evaluator; hence, HWGN$^2$ can be used to extend our framework to malicious security model and multiple-execution setting (for more details, see Section 7 and Appendix A).

Figure 4: Garbled MIPS evaluator, able to process any given number of instructions instead of a determined number. The black modules are extended and improved versions of memory and instruction handler in Lite MIPS architecture [60]: the instruction handler prepares the controller sequence by comparing the garbled MIPS instructions and the OP mapping. The controller runs the process sequence by generating the ALU mode and executing the read and write operations.

As opposed to TinyGarble2, HWGN$^2$ implementation is based on the garbled MIPS architecture, making the circuit private (i.e., no information about the NN architecture leaks) as explained next.

### 5.1.1 MIPS Evaluator in HWGN$^2$

As explained before, in order to ensure the privacy of the NNs, the Boolean function representing the NN (so-called netlist) is converted to a set of reduced instruction set computing (RISC) instruction set architecture (ISA) and evaluated on a core that executes the MIPS instructions [30]. It might be thought that a subset of instructions required to execute the NN is sufficient to be garbled in order to reduce the overhead; however, this could increase the probability of guessing which instructions are used and, consequently, violates the privacy of the NN.

To implement HWGN$^2$ on an FPGA, we modify Plasma [52] MIPS execution core emulating a RISC instruction set on the FPGA, to act as the garbled MIPS evaluator. Figure 4 illustrates the architecture of our garbled MIPS evaluator. The garbled evaluator receives three inputs: (i) a set of garbled instructions, (ii) the mapping for the instruction handler to fetch/decode the garbled instructions, and (iii) the evaluator’s garbled input. The combination of the first and second ones (i,ii) is the set of garbled tables and labels described before. Our garbled MIPS evaluator can evaluate the garbled MIPS instructions in two modes: (a) by receiving only one instruction and the operation code (OP) mapping and its corresponding instruction each cycle, i.e., the garbled evaluator with the capacity of one instruction per OT interaction, or (b) by receiving the complete set of instructions and their corresponding OP mapping at once. To achieve the resource-efficient implementation (mode i), we have modified the Lite MIPS instruction handler module in a way that the memory size related to the received garbled instructions (not the OP code mapping) decreases from 128 cells to only one cell. The controller is further enhanced by discarding the unnecessary scheduler, SCD storage memory and its parsing modules and tailoring the core to need of only one instruction conversion per OT. Moreover, we include the erase state in the instruction MEM controller, which sets all memory blocks to 0 after converting each garbled instruction to the OP code. To take advantage of the resource-efficient implementation, an extra step should be taken to divide the netlist into the sub-netlists with the number of gates selected by the user. The sub-netlists are fed to HWGN$^2$ in the same order provided in
the SCD file. This allows the user to make a trade-off between the resource efficiency and performance of the HWGN\textsuperscript{2}.

Specifically, in the first mode (a), in the first step, the instruction handler module receives one garbled instruction and OP mapping (all possible combinations of garbled MIPS instructions necessary to follow SFE protocol), which are stored in the instructions memory (MEM). In the next step, the instruction handler compares the given garbled instructions with garbled instructions MEM information and converts each garbled instruction to a set of OPs. Finally, the instruction handler sends the OP to the arithmetic-logic unit (ALU), erase instructions MEM, and repeats above-mentioned steps for the next garbled instructions. In the second mode (b), however, the instruction handler module works similarly to the Lite\_MIPS architecture cf. [60]. As both instruction sets and decode mapping are garbled on the garbler side, the evaluator cannot decrypt the garbled instructions due to the lack of the decryption key. Therefore, the garbler’s inputs and the DL model parameters are secure following the SFE and PFE protocols.

6 Evaluation of HWGN\textsuperscript{2}

6.1 Resource Utilization

To understand the interplay between communication cost, hardware resources utilization, and performance, we have synthesized the garbled evaluator with the capacity of 1 and 2345 (complete set of instructions) garbled MIPS instructions per one OT interaction. We have used Xilinx Vivado 2021 to synthesize our design and generate a bitstream. To make sure that the bitstream is correctly associated with the design, we have disable Xilinx Vivado place-and-route optimization and also utilize the DOWN TOUCH attribute.

The garbling framework considered in our implementations is Just\_Garble [5], also embedded in TinyGarble2 framework [26], which enjoys garbling optimization techniques such as Free-XOR [33], Row Reduction [47], and Garbling with a Fixed-key Block Cipher [5]. Our implementation is applied against three typical MLPs: the first one, with 784 neurons in its input layer, three hidden layers each with 1024 neurons, and an output layer with 10 neurons that is associated with the design, we have disable Xilinx Vivado place-and-route optimization and also utilize the DOWN TOUCH attribute.

Table 4 shows a comparison between the hardware utilization and OT cost of an unprotected MIPS evaluator core (Plasma[52]). HWGN\textsuperscript{2} and the state-of-the-art approaches applied to BM1. To give an insight into how much overhead cost the protection approaches impose, we have implemented Plasma core, an unprotected MIPS evaluator core on an Artix-7 FPGA. Note that we choose this architecture for the sake of a better comparison with the state-of-the-art solutions, e.g., [14]. It is also worth mentioning that since the ultimate goal of our paper is to demonstrate the applicability of garbling techniques for side-channel resiliency, the network mentioned above is chosen to serve as a proof of concept. As the HWGN\textsuperscript{2} processes the garbled instructions and inputs with the width of 32-bits, to have a fair comparison, we include the 32-bit MAC unit [55] in the resource utilization reported in Table 4.

In Table 4, BoMaNET and ModulaNET do not use OT to exchange their inputs. RedCrypt uses two OT interactions, one for the evaluator’s input and another for the evaluator’s output. However, in HWGN\textsuperscript{2}, in addition to the input and output labels exchange OT requirement, HWGN\textsuperscript{2} requires M more OT interactions, where M is the number of sub-netlists. There is an important observation made from Table 4: HWGN\textsuperscript{2} with the capacity of one instruction per OT interaction utilizes 0.0011× and 0.018× more logical and memory hardware resources, respectively, compared to an unprotected MIPS evaluator. The reason behind this efficiency is the size of instruction memory which stores only one instruction per OT interaction instead of the complete set of instructions. As mentioned in Section 5.1, to minimize resource utilization, one should sacrifice the communication cost, leading to an increased execution time. Hence, we set the size of the sub-netlist to just one gate, and every four gates are converted to a garbled instruction: $M = \frac{N_{\text{gate}}}{4}$, where $N_{\text{gate}}$ is the number of gates in the netlist. In this setting, HWGN\textsuperscript{2} requires 2 + 9380/4 = 2346 OT interactions, where 9380 is the number of gates included in the BM1 netlist. Based on the results of Table 4, HWGN\textsuperscript{2} utilizes up to roughly 11×, 4.5×, 3.2×, and 62.5× fewer logical and 16×, 6×, 4×, and 66× less memory hardware resources compared to GarbledCPU [62], BoMaNET [15], ModuloNET [14], and RedCrypt [55], respectively. Based on results presented in Table 4, HWGN\textsuperscript{2} is the most resource-efficient approach compared to the state-of-the-art approaches. In real-time applications where the execution time is the bottleneck, the OT interactions must be minimum [55]. Therefore, in Table 5, we have reported the hardware resource utilization in two cases: (i) when the number of OT interactions is maximum (first row) and (ii) when the number of OT interactions is minimum (second row). The results in Table 5 are for the implementation of BM1. As shown in Table 6, HWGN\textsuperscript{2} with the maximum performance is 2.5× faster than GarbledCPU [62]. Performance of HWGN\textsuperscript{2} is close to the performance of Redcrypt [55], the fastest state-of-the-art approach, while utilizing 62.5× fewer logical and 66× less memory than RedCrypt [55].

| Approach          | UT | PP | OT Interaction |
|-------------------|----|----|----------------|
| Plasma [52]       | 1775 | 1278 | N/A |
| GarbledCPU [52]   | 2346 | 2346 | 0 |
| RedCrypt [55]     | 9380 | 9380 | 2 |
| BoMaNET [15]      | 9835 | 9835 | N/A |
| ModulaNET [14]    | 5635 | 5635 | N/A |
| HWGN\textsuperscript{2} (1 instruction per OT interaction) | 1775 | 1278 | 2346 |

### Table 5: BM1 implemented by HWGN\textsuperscript{2} with different capacities of instruction per OT interaction.

| Instruction capacity per OT interaction | UT | PP | OT Interaction |
|-----------------------------------------|----|----|----------------|
| Complete set of instructions            | 1775 | 1278 | 2346 |
Table 6: Execution time and communication cost comparison between HWGN² and the state-of-the-art approaches (for BM1). Results for [62] and HWGN² are reported based on FPGA with clock frequency equals to 20MHz. (N/R: not reported, inst.: instructions).

| Approach         | Time (Sec) | Communication (MB) |
|------------------|------------|--------------------|
| tsgarbleCPU [62] | 1.74       | N/R                |
| RedCrypt [33]    | 0.63       | 3520               |
| HWGN² (Complete set of inst. per OT interaction) | 0.86 | 647               |
| TinyGarble2 [26] | 9.1        | 7.38               |

Table 7: Execution time and communication cost comparison between BM1 accelerator and XNOR-based version of that.

| Architecture | Instructions | OT Interaction | Execution Time (Sec) | Communication (MB) |
|--------------|--------------|----------------|----------------------|--------------------|
| BM1          | 5520         | 0.86           | 12.30                |
| XNOR-based BM1 | 1629       | 2.31           | 9.71                 |

with the FPGA, for the sake of comparison, we have used HostCPU presented in [55]. Note that in a real-world application, where the communication is performed over high latency links, the protocol execution remains fast due to the constant number of rounds in Yao’s GC underlying our design cf. [29, 40]. Moreover, we have used the EMP-toolkit [68] to establish the OT interaction between the garbler and the HostCPU. Table 6 shows the execution time and communication cost comparison between HWGN² and the state-of-the-art approaches employed against BM1. The memory footprint of classical GC approaches is \(O(1 + N_{gate})\), where \(I\) is the number of input wires and \(N_{gate}\) is the number of gates in the netlist. In contrast, the memory footprint of HWGN² and TinyGarble2 is the same: \(O(1 + N_{gate,m} + l_{m})\) where \(N_{gate,m}\) is the number of gates in the largest among sub-netlists included in the design, and \(l_{m}\) is the number of inputs of the sub-netlist, which equals 1 and 2, respectively, in the case of HWGN² with the instruction capacity 1 per OT interaction.

To compare the execution time and communication cost of TinyGarble2 with our approach, we have chosen the semi-honest mode when using their framework. HWGN² outperforms the TinyGarble2 implemented on CPU thanks to the parallel implementation made possible by the FPGA. On the other hand, when minimizing the OT interactions by investing more hardware resource utilization, HWGN² has a performance close to the RedCrypt with 62.5× fewer logical and 66× less memory utilization.

As an optimization technique, we have implemented the XNOR-based BM1. As the XOR operation is free in the garbling protocol [33], it is possible to decrease the size of the garbled netlists, which results in fewer instructions to be executed. Table 7 shows a comparison between two architectures. Using an XNOR-based implementation of a DL hardware accelerator decreases the number of instructions, leading to a less OT cost and execution time. The only limitation of this optimization is that the weights of the DL model must be binarized, and such binarization may slightly decrease the DL hardware accelerator output accuracy (see Section 7 for more details). Nevertheless, there are methods devised to deal with this, which can be adopted to bring significant benefits to garbled DL accelerators in terms of both OT cost and execution time.

6.2 Side-channel Evaluation

6.2.1 Side-channel Measurement Setup HWGN² has been implemented on Artix-7 FPGA device XC7AT100T with package number FTG256. We have captured the power and EM traces (see Appendix C) using Riscure setup, including LeCroy wavePro 725Zi as the setup oscilloscope. To prevent information loss, we have set our design frequency to 1.5MHz and the oscilloscope sampling frequency to 127.5MHz to reduce the time- and memory-complexity of the test. For each clock cycle, we have acquired 85 sample points. Decreasing the design frequency with the purpose of acquiring high-resolution side-channel traces made our design execution time 3.25 to 4.73 seconds for each classification performed by BM1. For this network, acquiring side-channel traces in the order of millions has high time complexity. Therefore, similar to [14], another MLP architecture, namely, BM2 is used for traces collection. The changes in MLP architecture hyperparameters allowed us to execute each classification in 312ms using HWGN² with 1.5MHz design frequency. As HWGN² executes each instruction separately in a sequential manner and the nature of the NNs is repetitive, we argue that the smaller MLP architecture can represent a larger one in terms of leakage.

6.2.2 Leakage Evaluation We have used a common methodology, namely Test Vector Leakage Assessment (TVLA) test, to evaluate HWGN² leakage resiliency. Although the TVLA test is subject to two disadvantages – false positive/negative results and limited ability to reveal all points of interests [17, 46, 63] – it is still the most common methodology used in recent papers to evaluate the resiliency of the approach against side-channel leakage.

In the TVLA test methodology, Welch’s t-test is used to check the similarity between two trace groups captured from two populations of inputs. Welch’s t-test calculates the t-score based on the following equation: \(t = (\mu_1 - \mu_2) / \sqrt{(s_1^2/n_1) + (s_2^2/n_2)}\), where \(\mu_1\) and \(\mu_2\) are the means, \(s_1\) and \(s_2\) are the standard deviations, and \(n_1\) and \(n_2\) are the total number of the captured traces for first and second population, respectively. Based on the null-hypothesis, if two populations are chosen from one distribution, their corresponding t-score must be less than \(\pm 4.5\). Exceeding t-score magnitude of 4.5 (so-called null-hypothesis) means the design is subject to side-channel leakage with probability greater than 99.99%. In our setup, we choose the non-specific fixed vs. random t-test in a way that our setup, first, captures the power consumption/EM traces from a fixed input computation for all the traces; then, the experiment repeats for a set of randomly generated inputs. Based on the two captured traces, for fixed and random inputs, our setup calculates the t-score based on the aforementioned equation.

6.2.3 Power Side-channel Leakage Assessment To illustrate the side-channel protection offered by HWGN², we have mounted the TVLA test on power traces of an unprotected MIPS core. Plasma core presented by Opencores projects [52], and HWGN², with the capacity of one instruction per OT interaction. Figure 5 shows the TVLA results of an unprotected MIPS core and HWGN², with the capacity of one instruction per OT interaction. The t-scores are calculated based on 10000 captured traces, 5000 for each fixed and random input population. As one can observe, an unprotected MIPS core
t-score has exceeded the ±4.5 threshold with only 10000 traces, while the HWGN$^2$’s t-score remains below the threshold.

To have a design with leakage resiliency, the t-score results must remain below the threshold with the traces populations in the order of millions [13, 14, 46, 63]. Hence, in the next experiment, we have captured a total of 2 million (2M) traces, 1M traces for each fixed and random input populations. A low t-score, less than ±4.5, calculated from a trace population in the order of millions confirms the protection strength of HWGN$^2$. It should be noted that these traces are captured in the low-noise setup (i.e., more optimistic for the attacker) while in the actual scenario, the number of traces to break the garbling scheme should be significantly higher due to more noisy environments.

As a proof of concept that HWGN$^2$ side-channel resiliency is independent of the function or architecture we also mount the TVLA test on two more implementations: XNOR-based DL hardware accelerator and DL hardware accelerator. Figure 6, (a) and (c), illustrates the t-score of HWGN$^2$ applied to XNOR-based BM2, with the capacity of complete set of instructions per OT interaction and one instruction per OT, respectively. As can be seen, the t-scores of HWGN$^2$ stay below the threshold of ±4.5 for different cases of instruction capacity per OT interaction and the function or architecture implemented on an FPGA using HWGN$^2$. The t-scores in Figure 6, (b) and (d), indicate that not only HWGN$^2$ with the capacity of one instruction per OT interaction provides a strong protection against power side-channel attacks but also changes in the number of instruction capacity per OT interaction does not affect this protection (for results of EM SCA, see Appendix C).

**Can we see the architecture-related patterns?** Based on the attack presented by Batina et al. [4], revealing the DL model architecture can enhance the attacker’s ability to obtain DL model parameters. They showed that the EM trace captured from an unprotected DL model implementation on Atmel ATmega328P microcontroller can be used to extract the DL model architecture. The reason behind these irregular patterns is that each garbled instruction is encrypted; therefore, in the evaluation phase, the EM traces do not follow a pattern which could result in revealing the DL model architecture.

### 7 Discussion

**Security in the presence of malicious adversary – a byproduct.** According to our adversary model defined in Section 2, the garbler may act as a malicious adversary to extract information related to the user’s input by generating a corrupted GC [38]. Note that it does not match the scenario defined for SCA, although as a byproduct, one can consider the extension to the malicious security model. In doing so, to protect the evaluator from the malicious garbler, the concept of cut-and-choose, see, e.g., [38, 39], has been...
widely employed to ensure the security of the evaluator’s input. The principal behind the cut-and-choose protocol is that the garbler constructs many GCs instead of one and sends them to the evaluator. The evaluator then, chooses a random set of GCs, opens them, and checks whether the GCs are constructed correctly or not. To cope with the computation and communication overhead, Lindel has introduced a fast cut-and-choose protocol based on the majority outputs calculation with a cheating probability of at most $2^{-4}$ where $s$ is the number of constructed GCs by the garbler [38], e.g., to achieve a cheating probability of at most $2^{-40}$ garbler must generate 40 GCs [38, 50]. It is remarkable that not every available garbling tool supports the malicious security model, although TinyGarbled2 can handle this, of course, with some modifications to satisfy the hardware implementation (e.g., pipelining). Therefore, if needed, HWGN$^2$ can be easily upgraded to support the security under the malicious adversary scenario. To the best of our knowledge, HWGN$^2$ is the first hardware accelerator to fulfill this need. The details of our implementation and results are given in Appendix A.

**Multiple-execution setting.** The multiple-execution setting has been understudied in the existing literature on the implementation of private DL accelerators. This is despite of the cryptographic protocols developed to guarantee the security of GCs under this circumstance. The multiple-execution setting is relevant if the DL accelerator (possibly with different inputs) is evaluated multiple times, either in parallel or sequentially. When executing the protocol for the first time, it could be feasible to send the entire set of inputs at once (sometimes called parallel execution). Nonetheless, the sequential execution of the OT and the SFE protocol built upon leads to a more resource-efficient implementation since all the labels should not be stored together. Note that to guarantee security, a fresh garbled function $F$ for each user/a set of inputs should be generated. To extend the protocol to multiple-execution setting, a straightforward approach is to run a maliciously-secure protocol multiple times. In this regard, if the cheating probability is kept as before, i.e., at most $2^{-4}$, the number of constructed GCs should be increased to $s + \log t$ from $s$, where $t$ is the number of executions. This overhead can be indeed reduced if a more efficient protocol, e.g., one presented in [25], is considered. Noteworthy is the fact that, this protocol has been built upon the cut-and-choose protocol [38], whose overhead for HW DL accelerators is discussed in Appendix A. We argue that as the core computation for HWGN$^2$ is the same in HbC, malicious, and multiple-execution settings, no side-channel leakage can be observed in the two latter cases either.

**Trade-off between accuracy and efficiency.** Thanks to the binary values and bitwise operations, Binarized NNs (BNNs) can perform the computation efficiently, although at the price of exhibiting less precision compared to their full precision counterparts. For instance, XNOR can perform the multiplication in a bitwise manner. Afterward, the accumulation needed by the dot product can be done by counting the number of bits set to “1” in a group of XNOR products, multiplying this value by 2 and subtracting the total number of bits producing an integer value. Alternatively, a Popcount instruction can be used from the processor instruction sets. Compared to multi-bit floating-point or fixed-point multiplication and accumulation, these bitwise operations are much faster and hardware resource-efficient to perform [59]. In this regard, the size of BNN models, even their original (i.e., not garbled) designs, is much smaller, which promotes further research into the implementation of NNs on hardware platforms, e.g., FPGAs. Having these advantages in mind, efforts have been made to improve the accuracy of BNNs, for instance, XNOR-Net has been proposed to narrow the gap when considering datasets like ImageNet [51].

By keeping the balance between the accuracy and hardware resource-efficiency in the original XNOR-Net design, it is also possible to achieve high hardware resources-efficiency, when garbling the BNNs as XNORing is free. To minimize the cost in terms of accuracy, one can take advantage of algorithmic solutions to scale up the size of XNOR-Net during the training phase and prune the network afterward cf. [53]. Note that the accuracy of our garbled BNNs is not affected by the garbling process, i.e., the accuracy of the garbled NNs is similar to that of the trained NNs.

**Homomorphic Encryption (HE) vs. GCs.** One of the promising solutions for oblivious inference is HE, where fully HE enables us to perform computation on encrypted data at the price of (relatively) high computational complexity. Partially HE (PHE) exhibits less overhead, but solely supports a subset of functions or depth-bounded arithmetic circuits. Even though HE-based DL accelerators could suffer from difficulties, e.g., complicated implementation of non-linear functions such as ReLU, high computational complexity, and truncation error [45, 53], the advancement in this domain makes these accelerators more feasible in practice. In addition to software implementation of such accelerators, including [20, 29, 41, 45], a hardware accelerator has been designed to bridge the gap between FHE and unencrypted computation through a specialized accelerator taking advantage of hardware acceleration [57].

Since HE can also offer resiliency against SCA, it could be useful to compare the resource utilization of HWGN$^2$ and a HE-based DL accelerator. As results for typical NNs employed in the relevant work, e.g., [29, 41, 45], are not reported in [57], we compare implementation of HWGN$^2$ with ones presented in [29, 41] (see Table 8). The NN used in this example is the benchmark NN, first used in [45] and then employed against Gazelle and MiniONN in [29, 41].

It is important to remark that these studies have focused on fully-software-based implementation of HE schemes, whereas HWGN$^2$ results are collected from an ARTIX-7 FPGA (clock frequency of 20 MHz) board as the evaluator. As precisely mentioned in [29], both HE and GC techniques have their limitations. To select one for an application, it is suggested to take their trade-offs into account: for application with timing constraints, HWGN$^2$ can offer similar time-complexity compared to Gazelle that shows a great deal of time-efficiency. On the other hand, if the major bottleneck is communication complexity, HWGN$^2$ with the 1 instruction per OT could be useful. We remark again that the comparison presented in Table 8 is not completely fair as HWGN$^2$ accelerator is implemented in hardware. Moreover, HE methods might not support circuit privacy as given by PFE and supported by HWGN$^2$, although there are HE protocols that attain this objective [7, 19]. As it is beyond the scope of this paper, we will not provide details on this.

**Interactive and non-interactive garbling:** If an SFE protocol with garbling scheme $G$ is built upon an OT, after receiving the inputs $F$ and $d$, party 1 can initiate the OT protocol to obtain the output $y$. In other words, the interaction between parties happens solely...
Table 8: Execution time and communication cost of HE-based approaches vs. HWGN. NNs (input layer:784 neurons, two hidden layers: 128 neurons each, and an output layer: 10 neurons) trained on MNIST. The results for HE schemes presented in [29, 41] are taken from [53] (inst.: instructions).

| Approach       | Time (Sec) | Communication (MB) |
|----------------|------------|--------------------|
| MiniONN* [41]  | 1.84       | 15.8               |
| Gazelle [29]   | 0.09       | 0.5                |
| HWGN^2 (1 inst. per OT Interface) | 0.79 | 2.95              |
| HWGN^5 (Complete set of inst. per OT interface) | 0.14 | 145               |

when the OT protocol is executed. Therefore, if a non-interactive OT can be realized, the SFE protocol can be run non-interactively, e.g., by incorporating appropriate hardware such as trusted platform modules (TPMs) [22]. For malicious security model, however, their proposal would not be secure; hence, One-Time Programs (OTP), i.e., GCs with OT calls being implemented with One-Time Memory (OTM) tokens, have been introduced [21]. These primitives can also offer an important byproduct that is one-time or limited-time execution, i.e., the DL inference can occur only once or for a limited time, which can be helpful for enforcing license agreements. To the best of our knowledge, Jarvinen et al. [28] was the first to adopt these notions and further obtained leakage-resilience hardware implementations of cryptographic implementations, even in the non-interactive setting and in the presence of malicious adversary. Nevertheless, in their design, the privacy of the circuit has not been dealt with. The extension of HWGN to non-interactive model can be considered as our future work.

8 Conclusion

In this paper, we have examined the feasibility of garbling to prevent attackers from launching SCA attacks against DL hardware accelerators. We have implemented HWGN as a garbled DL hardware accelerator on an Artix-7 FPGA. By tailoring the concepts known only for software garbled DL accelerator [26] to the needs of a hardware DL accelerator, the implementation of such accelerator is enhanced: HWGN requires up to 62.5% fewer logical and 66x less memory utilization compared to the state-of-art approaches. This is indeed possible at the price of more communication overhead. HWGN provides users the flexibility to protect their NN IP both in real-time applications and in applications where the hardware resources are limited by hardware resource utilization or communication cost. As our leakage evaluation results indicated, for both EM and power side-channels, the t-scores are below the threshold (±4.5), which shows the side-channel leakage resiliency of HWGN with trace population in the order of millions. Another strength of HWGN is the DL model architecture thanks to the SFE/PFE protocol realized through MIPS instructions. Last but not least, we have discussed how HWGN can be implemented in the presence of a malicious adversary– as a by-product.

References

[1] Giuseppe Atzeniese, Luigi V Mancini, Angelo Spognardi, Antonio Villani, Domenico Vitali, and Giovanni Felici. 2015. Hacking smart machines with smarter ones: How to extract meaningful data from machine learning classifiers. In Inf. J. Security and Networks 10, 3 (2015), 157–160.

[2] Marshall Ball, Brent Carmer, Tal Malkin, Mike Rosulek, and Nichole Schimanski. 2019. Garbled neural networks are practical. Cryptology ePrint Archive (2019).

[3] Marshall Ball, Tal Malkin, and Mike Rosulek. 2016. Garbling gadgets for boolean and arithmetic circuits. In Proc. of the 2016 ACM SIGSAC Conf. on Computer and Communications Security: 565–577.

[4] Lejla Batina, Shivam Bhasin, Dirmanto Jap, and Stepan Picek. 2019. CSI NN: Reverse engineering of neural network architectures through electromagnetic side channel. In 28th USENIX Security Symp. (USENIX Security 19): 515–532.

[5] Mihir Bellare, Viet Tung Hoang, Sriram Keertheedhi, and Phillip Rogaway. 2013. Efficient garbling from a fixed-key blockcipher. In 2013 IEEE Symp. on Security and Privacy. IEEE: 478–492.

[6] Mihir Bellare, Viet Tung Hoang, and Phillip Rogaway. 2012. Foundations of garbled circuits. In Proc. of the 2012 ACM Conf. on Computer and communications security: 784–796.

[7] Florian Bourse, Rafael Del Pino, Michele Minelli, and Hoeteck Wee. 2016. FHE circuit privacy almost for free. In Annual Int’l Cryptology Conf. Springer: 62–89.

[8] Jakub Breier, Dirmanto Jap, Xiaolu Hou, Shivam Bhasin, and Yang Liu. 2021. SNIFF: reverse engineering of neural networks with fault attacks. IEEE Trans. on Reliability (2021).

[9] Eric Brier, Christophe Clavier, and Francis Olivier. 2004. Correlation power analysis with a leakage model. In Intl. workshop on cryptographic hardware and embedded systems. Springer: 189–218.

[10] Nicholas Carlini, Matthew Jagielski, and Ilya Mironov. 2020. Cryptanalytic extraction of neural network models. In Annual International Cryptology Conference. Springer: 189–218.

[11] Anrin Chakraborti, Reza Curtmola, Jonathan Katz, Jason Nieh, Ahmad-Reza Sadeghi, Radia Sion, Yiqiang Zhang, et al. 2022. Cloud Computing Security: Foundations and Research Directions. Foundations and Trends® in Privacy and Security: 2, 3 (2022), 103–213.

[12] Suresh Charji, Josyula R Rao, and Pankaj Rohatgi. 2002. Template Attacks. In Int’l. Conf. on Security and Privacy (S&P’02). IEEE: 138–147.

[13] Suresh Charji, David DeCruze, Malik Sha, and Amir Moradi. 2018. Hardware masking revisited. IACR Trans. on Cryptographic Hardware and Embedded Systems (2018): 123–148.

[14] Anuj Dubey, Afzal Ahmad, Muhammad Aied Paisha, Rosario Cammarota, and Aydin Aysu. 2020. Module.NET: Neural Networks Meet Modular Arithmetic for Hardware Efficient Masking. IACR Trans. on Cryptographic Hardware and Embedded Systems (2022): 506–556.

[15] Anuj Dubey, Rosario Cammarota, and Aydin Aysu. 2020. BosMl.NET: Boolean masking of an entire neural network on an FPGA. In 2020 IEEE/ACM Int’l. Conf. On Computer Aided Design (ICCAD). IEEE: 1–9.

[16] Anuj Dubey, Rosario Cammarota, and Aydin Aysu. 2020. Maskednet: The first hardware inference engine aiming power side-channel protection. In 2020 IEEE Intl. Symp. on Hardware Oriented Security and Trust (HOST). IEEE: 197–208.

[17] François Durvaux and François-Xavier Standaert. 2016. From improved leakage detection to the detection of points of interests in leakage traces. In Annual Int’l. Conf. on the Theory and Applications of Cryptographic Techniques. Springer: 249–262.

[18] Matthew Fredrikson, Eric Lantz, Somesh Jha, Simon Lin, David Page, and Thomas Ristenpart. 2014. Privacy in Pharmacogenetics: {A}n (End-to-End) Case Study of Personalized Warfarin Dosing. In 23rd USENIX Security Symp. (USENIX Security 14): 17–32.

[19] Craig Gentry. 2009. A fully homomorphic encryption scheme. Ph. D. Dissertation. Stanford University. crypto.stanford.edu/craig.

[20] Ran Gilad-Bachrach, Nathan Dowlin, Kim Laine, Kristin Lauter, Michael Naehrig, and John Wernsing. 2016. Cryptonets: Applying neural networks to encrypted data with high throughput and accuracy. In Intl. conference on machine learning, PMLR: 201–210.

[21] Shafi Goldwasser, Yael Tauman Kalai, and Guy N. Rothblum. 2008. One-time programs. In Annual Intl. Cryptology Conf. Springer: 39–56.

[22] Vandana Gunupudi and Stephen R. Tate. 2008. Generalized non-interactive oblivious transfer using count-limited objects with applications to secure mobile agents. In Intl. Conf. on Financial Crypt. and Data Security Springer: 98–112.

[23] Roll Herken. 1988. The universal Turing machine: a half-century survey. Springer.

[24] Johann Heyszl, Dominik Merli, Benedict Heinz, Fabrizio De Santis, and Georg Sigl. 2012. Strengths and limitations of high-resolution electromagnetic field measurements for side-channel analysis. In Intl. Conf. on Smart Card Research and Advanced Applications. Springer: 248–262.

[25] Yan Huang, Jonathan Katz, Vladimir Kolesnikov, Ranjit Kumaresan, and Alex J. Malozemof. 2014. Amortizing garbled circuits. In Annual Crypto ‘14. Springer: 458–475.

[26] Siam Hussian, Baiyu Li, Farinaz Koushanfar, and Rosario Cammarota. 2020. TinyGarble2: Smart, Efficient, and Scalable Yao’s Garbled Circuit. In Proc. of the 2020 Workshop on Privacy-Preserving Machine Learning in Practice. 65–67.

[27] Siam Hussian and Farinaz Koushanfar. 2019. FASE: FPGA acceleration of secure function evaluation. In 2019 IEEE 27th Annual Intl. Symp. on Field-Programmable Custom Computing Machines (FCCM). IEEE: 280–288.

[28] Kimmo Jarvinen, Vladimir Kolesnikov, Ahmad-Reza Sadeghi, and Thomas Schneider. 2010. Garbled circuits for leakage-resilience: Hardware implementation and evaluation of one-time programs. In Intl. Workshop on Cryptographic Hardware and Embedded Systems. Springer: 383–397.

[29] Chirag Juvvark, Vinod Vaikuntanathan, and Anantha Chandrakasan. 2018. [GAZELLE]: A low latency framework for secure neural network inference.
In 27th USENIX Security Symp. (USENIX Security 18). 1651–1669.

[30] Gerry Kane. 1988. mips RISC Architecture. Prentice-Hall, Inc.

[31] Joe Kilian. 1988. Founding cryptography on oblivious transfer. In Proc. of the annual ACM Symposium on Theory of computing. ACM, 319–329.

[32] Paul Kocher, Joshua Jaffe, and Benjamin Jun. 1999. Differential power analysis. In Annual international cryptology conference. Springer, 388–397.

[33] Vladimir Kolesnikov and Thomas Schneider. 2008. Improved garbled circuit: Free XOR gates and applications. In Intl. Colloquium on Automata, Languages, and Programming. Springer, 468–498.

[34] Yann LeCun. 2019. 1.1 deep learning hardware: Past, present, and future. In 2019 IEEE Intl. Solid-State Circuits Conf. (ISSCC). IEEE, 12–19.

[35] Yann LeCun, Yoshua Bengio, and Geoffrey Hinton. 2015. Deep learning. nature 521, 7553 (2015), 436–444.

[36] Yann LeCun, Yoshua Bengio, and Geoffrey Hinton. 2015. Deep learning. Nature 521, 7553 (2015), 436–444.

[37] Iftar Levi and Carmit Hazay. 2022. Garbled-Circuits from an ACA Perspective: Free XOR can be Quite Expensive. Cryptology ePrint Archive (2022).

[38] Yehuda Lindell. 2016. Fast cut-and-choose-based protocols for malicious and covert adversaries. Journal of Cryptology 29, 2 (2016), 456–490.

[39] Yehuda Lindell and Benny Pinkas. 2007. An efficient protocol for secure two-party computation in the presence of malicious adversaries. In Annual international conference on the theory and applications of cryptographic techniques. Springer, 52–78.

[40] Yehuda Lindell, Benny Pinkas, Nigel P Smart, and Patrick Hazen. 2019. Gradient-based learning applied to document recognition. Proc. of the IEEE 86, 11 (1998), 2278–2324.

[41] Jian Liu. 2018. Deep learning for side-channel security. IEEE Security & Privacy 16, 6 (2018), 129–139.

[42] Jian Liu, Dana Duchman-Soled, and Ankur Srivastava. 2019. Mitigating reverse engineering attacks on deep neural networks. In 2019 IEEE Computer Society Annual Symp. on VLSI (ISVLSI). IEEE, 606–616.

[43] Jian Liu, Dana Duchman-Soled, and Ankur Srivastava. 2019. Mitigating reverse engineering attacks on deep neural networks. In 2019 IEEE Computer Society Annual Symp. on VLSI (ISVLSI). IEEE, 606–616.

[44] Payman Mohassel and Yupeng Zhang. 2017. Secureml: A system for scalable privacy-preserving machine learning. In 2017 IEEE symposium on security and privacy (SP). IEEE, 19–38.

[45] Payman Mohassel and Yueng Zhang. 2017. Secureml: A system for scalable privacy-preserving machine learning. In 2017 IEEE symposium on security and privacy (SP). IEEE, 19–38.

[46] Amir Moradi, Bastian Richter, Tobias Schneider, and François-Xavier Standaert. 2018. Leakage detection with the x2-test. IACR Trans. on Cryptographic Hardware and Embedded Systems (2018), 209–237.

[47] Moni Naor, Benny Pinkas, and Reuban Sumner. 1999. Differential power analysis. In Annual international cryptology conference. Springer, 388–397.

[48] Nikola Samardzic, Axel Feldmann, Aleksandar Kravstev, Srinivas Devadas, Ronald Dreslinski, Christopher Peikert, and Daniel Sanchez. 2021. F1: A fast and programmable accelerator for fully homomorphic encryption. In MICRO-54: 54th Annual IEEE/ACM Intnl. Symp. on Microarchitecture. IEEE, 252–260.

[49] Stjepan Picek, Guilherme Perin, Luca Mariot, Lichao Wu, and Lejla Batina. 2021. A survey on hard-versus soft errors in modern microprocessors. Computers & Security 101, 101764 (2021).

[50] Eric Peeters, François-Xavier Standaert, and Jean-Jacques Quisquater. 2007. Power analysis on the RC5 S-box with the x2-test. In 2007 IEEE Annual Symposium on Security and Privacy. IEEE, 99–134.

[51] Taylor Simons and Dah-Jye Lee. 2019. A review of binarized neural networks. IEEE Trans. on Computers 68, 11 (2019), 1820–1834.

[52] Mark Zhao and G Edward Suh. 2018. FPGA-based remote power side-channel attacks. In Proc. of the 2018 Annual IEEE/ACM Intnl. Conf. on Computer and Communications Security (CCS). IEEE, 183–194.

[53] Kota Yoshida, Takaya Kubota, Shunsuke Okura, Mitsuru Shiozaki, and Takeshi Weinert, and Tim Weißmantel. 2020. RiCaSi: rigorous cache side-channel mitigation via selective circuit compilation. In Intl. Conf. on Cryptology and Network Security. Springer, 505–525.

[54] Sparsh Mittal, Himanshu Gupta, and Srishti Srivastava. 2021. A survey on hardware security of DNN models and accelerators. Journal of Systems Architecture 117 (2021), 102163.

[55] Payman Mohassel and Yueng Zhang. 2017. Secureml: A system for scalable privacy-preserving machine learning. In 2017 IEEE symposium on security and privacy (SP). IEEE, 19–38.

[56] Amir Moradi, Bastian Richter, Tobias Schneider, and François-Xavier Standaert. 2018. Leakage detection with the x2-test. IACR Trans. on Cryptographic Hardware and Embedded Systems (2018), 209–237.

[57] Nikola Samardzic, Axel Feldmann, Aleksandar Kravstev, Srinivas Devadas, Ronald Dreslinski, Christopher Peikert, and Daniel Sanchez. 2021. F1: A fast and programmable accelerator for fully homomorphic encryption. In MICRO-54: 54th Annual IEEE/ACM Intnl. Symp. on Microarchitecture. IEEE, 252–260.

[58] Mark Zhao and G Edward Suh. 2018. FPGA-based remote power side-channel attacks. In Proc. of the 2018 IEEE Security and Privacy (SP) IEEE, 229–244.

[59] Mohammed Hashemi, Steffi Roy, Domenic Forte, and Fatemeh Ganji

Appendix A. HWGN² in the Presence of Malicious Adversaries

To implement our approach on FPGA, we have used garbled MIPS evaluator presented in Section 5.1.1. Figure 8 illustrates the flow of the HWGN² in the presence of a malicious adversary. Note that the numbers in the paragraphs are corresponding to the arrow indices in the Figure 8 and the garbled evaluator represents garbled MIPS evaluator. In the first step (1.1), the garbler constructs many garbled instructions sets, more than 40 instruction sets, from function f and sends them to the evaluator. In addition, the garbler generates two matrices (1.2): e and d corresponding to constructed garbled instructions sets’ input encryption labels output decryption labels, respectively. The dimension of each matrix, e and d, equals
The XOR-tree approach presented in [39]. In the evaluation phase, the evaluator must garbled and feed 40 garbled instructions sets, the evaluator must garbled and feed the same input to the evaluator (2.3), to check whether every 40 garbled instructions sets generate the same output or not. The opening and checking process contains two phases: (i) evaluation and (ii) XOR-tree approach presented in [39]. In the evaluation phase, the evaluator encrypts the chosen input with the corresponding input encryption labels (e) (3.1), evaluates the chosen garbled instructions set, and decrypts the generated garbled output (3.2) using the corresponding output decryption labels (d) (3.3). Thereafter, in the XOR-tree phase, the evaluator calculates the XOR value of all decrypted outputs (3.3), bit by bit, to find any difference between the outputs. If the output of the XOR-tree becomes 1 (3.4), it means that the garbler is a cheater. Otherwise (3.5), the evaluator can only assume that none of the 40 chosen garbled instructions sets is corrupted. To minimize the cheating probability of the garbler even more, the evaluator evaluates the rest of the garbled instructions sets (4.1) (the remaining sets of instructions in (1.1)) and chooses the majority output of the evaluation of all the garbled instructions sets as its correct output (4.2).

The above-mentioned protection approach against the malicious garbler introduces two overheads to the design: (i) the XOR-tree and Majority Output calculation modules and (ii) increasing the size of garbled instructions memory of garbled evaluator core. To alleviate the latter overhead, HWGN$^2$ with an improved hardware resource efficiency is a better choice to minimize the hardware memory resource utilization with the trade-off of increasing communication costs. In a nutshell, in real-time applications, the hardware resource utilization should be maximum and the communication cost should be minimum to obtain the minimum execution time; using TinyGarble-based implementation of HWGN$^2$ is the best implementation choice. On the contrary, in the application where the hardware resource utilization is the burden, the design netlist must be divided into n sub-netlists, where n is the number of gates which means each sub-netlist contains just one gate, and the evaluation of GC must be done gate by gate each via an OT interaction (refer to Section 6.1 to see the comparison results). Overall, using HWGN$^2$ gives the flexibility of using GCs in different types of applications.

**Figure 8: The flow of the presented approach in the presence of a malicious adversary (Garbled Instructions Set: corresponding to the set of garbled MIPS instructions corresponding to the function $f_i$, Garbled Instructions to OP-code Decode Mapping: the complete garbled ISA based on which the garbled MIPS core evaluates the garbled MIPS instructions, Random Label: number of the randomly chosen garbled instructions set to be opened and checked, XOR-tree: a tree of cascaded XORs to find any difference in between the outputs corresponding to the evaluation of randomly chosen garbled instructions sets, and Majority Output: calculates the evaluator’s output based on the majority of all evaluations outputs’ value. (Note: starred modules (*) are inspired from [38]).**
Table 9: Hardware resource utilization costs of HWGN\(^2\) in the presence of a malicious adversary. NNs (input layer: 784 neurons, three hidden layers: 1024 neurons each, and an output layer: 10 neurons) trained on MNIST.

| Module                      | LUT | FF  | OT interaction |
|-----------------------------|-----|-----|----------------|
| Garbled MIPS Evaluation     | 1375| 1278| 2346           |
| Majority Output             | 10  | 0   | 0              |
| Overall                     | 1485| 1308| 2346           |

Table 10: Execution time and communication cost comparison between HWGN\(^2\) and the state-of-the-art approach in the presence of a malicious adversary (Implementation of LeNet interface).

| Approach                        | Time (ms) | Communication (MB) |
|---------------------------------|-----------|--------------------|
| Tinygarble2 (60)                | 291       | 72.75              |
| HWGN\(^2\) (DIL hardware accelerator) | 39.12    | 93.02              |
| HWGN\(^2\) (XNOR based DIL hardware accelerator) | 26.43 | 61.85 |

Figure 9: TinyGarble-based implementation [60] of HWGN\(^2\) (L: wires garbled labels, GT: garbled tables, e: encryption labels, d: decryption labels, x: evaluator’s raw input, X: evaluator’s garbled input, Y: garbled output, Y\(_i\), X\(_i\), GT\(_i\), L\(_i\): garbled input, output, garbled tables, wire labels corresponding to \(i\)th sub-netlist, respectively, y: evaluator’s raw output, and SCD: A custom circuit description which allows TinyGarble to evaluate the Boolean circuit).

In the final step (Step 3.2), output decryption labels (d) are sent to the evaluator to decrypt the evaluator core’s garbled output Y and obtain its raw output y. The sequential evaluation supported by TinyGarble provides the GC protocol the scalability of evaluation of larger netlists. However, when one implements the DL hardware accelerator in the garbled format which has a large netlist, memory and logical resource utilization become burdens for DL hardware accelerators [28] (see Section 6.1).

Appendix C. TVLA Test Evaluation of EM Side-channel

One of the first studies that has compared the capabilities of attackers launching power vs. EM SCA is [48], where it is suggested that the EM leakage can provide more information than the power consumption of the same chip cf. [64]. This has been further justified in [64] through the evaluation of the information theoretic and security metrics [65]. Therefore, it might be thought that the EM side-channel could offer some information about the secret, i.e., the weights of the garbled NN. To collect the EM traces, it has been already verified that measurements from the frontside of a chip can offer a high signal-to-noise ratio [24]; hence, we stick to this setting to perform measurements. Our setup described in Section 6.2.1 is equipped with HP EM probe 125 (SN126 0.2mm). Figure 10 shows the t-scores computed for HWGN\(^2\) applied against BM2. As shown in Figure 10, the t-scores of EM traces are below the threshold (±4.5) which is the proof of the EM leakage resiliency of HWGN\(^2\).