Black-sun noise immune correlated double sampling scheme for CMOS image sensors

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Abstract This paper presents a black-sun immune correlated double sampling (CDS) scheme for high-quality imaging. Based on an analysis of signal characteristics in strong light conditions, a clamping circuit-based signal difference generator is proposed to accurately present the bright light information. The proposed scheme eliminates the black-sun noise with simple circuitry to improve the A/D conversion efficiency. Moreover, it can be is reversible to the conventional algorithm so that it still preserves the structural advantages of the existing CMOS image sensor (CIS) structure. A prototype CIS with a column-parallel 11-bit single-slope (SS) analog-to-digital converter (ADC) was fabricated in a 0.11-µm 1P4M CIS process with a 2.9-µm pixel pitch.

Keywords: CMOS image sensor, black-sun noise, correlated double sampling, single-slope analog digital converter

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Recently, CISs have received considerable attention for a variety of applications [1, 2, 3, 4, 5, 6]. Owing to the increasing demand for high-quality images, various CIS structures with low-noise performance have been developed [7, 8, 9, 10]. In commercial CISs, a SS ADC structure with a 4-transistor active pixel sensor (4T-APS) is employed for its structural advantages [11, 12, 13] that it can adopt correlated double sampling (CDS) scheme during the pixel readout operation to eliminate fixed pattern noise (FPN) [14, 15, 16]. However, when the initial value is contaminated, it is difficult to obtain an accurate signal value because the voltage difference obtained is considered as the signal value. As reported in previous studies [17, 18, 19, 20], in strong light illumination conditions, the photo-charge overflows from a photodiode (PD) to a floating node (FD). This causes the initial value of the pixel to drop abnormally during the CDS operation resulting in output image errors (i.e., black-sun noise). To solve this problem, in [17] a new readout scheme was proposed to eliminate black-sun noise.

However, due to additional circuitries, the circuit area and design complexity also increased. In this paper, an efficient black-sun immune CDS scheme is proposed with a novel signal difference generator (SDG). The proposed scheme maintains the existing commercial structure and readout operation form, thereby presenting several commercial advantages.

2. Proposed black-sun immune CDS scheme

Fig. 1 shows a simplified schematic of a conventional SS ADC with the proposed SDG. The SDG is connected to the pixel output (Vpx) node. It consists of an analog switch (Mux.), two signal voltages (Vselb and Vref), and current bleeding circuits (Mpc, Msb, and Men). It is based on the Vpx common generator [21], which is used only after completing the pixel readout operation. According to rolling shutter techniques [22], when the Vpx node is changed from Vsig–1 to Vrst (Vsel is off), Msb is switched by Vselb and Vpx remains constant at a certain voltage level, which reduces Vpx fluctuation. Here, Vrst and Vsig represent a pixel reset voltage and pixel signal voltage, respectively.

In this study, the SDG is utilized to achieve an additional performance. When pixel readout operation starts (Vsel is on), Msb is biased to a predetermined voltage (Vref). Subsequently, it observes whether Vpx is lower than Vref – Vth and prevent a drop in Vpx, as a the Vpx-clamping circuit. Here, Vref can be set at the Vpx-clamping level, Vth is the threshold voltage for Msb.

The operational timing diagram and those waveforms are illustrated in Fig. 2 (a) and (b), respectively. For the pixels chosen by Vsel, Vpx becomes Vrst and Vsig for the pixel control signals of Vrx and Vtx, respectively. Vpx and Vamp pass through AC-coupling capacitors (Cen and Csp) and into comparator input nodes (Vin and Vvinp), respectively. To perform a dual CDS [23, 24], the analog CDS [25, 26] is performed when Vaz is on while the digital CDS [27, 28] is performed twice, for both Vrst and Vsig when Vaz is on. Note that the initial value (Vrst) should be maintained until it changes to the signal value (Vsig) to

Fig. 1 Simplified schematic of the proposed column-parallel SS ADC.
obtain an accurate difference ($V_{\text{CDS}}$). However, in strong light illumination conditions (as plotted by the blue dashed line in Fig. 2 (a)), $V_{\text{RST}}$ drops to a low voltage level and produces an incorrect CDS result ($V_{\text{CDSB}} < V_{\text{CDSN}}$). Consequently, dark spots are formed within the bright region of the captured image; this is because $V_{\text{RST}}$ is not maintained at a constant level just before $V_{\text{TX}}$ is switched on. To solve this problem, the SDG is enabled ($V_{\text{EN}}$ is on) right before $V_{\text{TX}}$ is switched on; furthermore, whether $V_{\text{RST}}$ is lower than $V_{\text{REF}} - V_{\text{TH}}$, is observed. As shown in Fig. 2 (b), if $V_{\text{RST}} < V_{\text{REF}} - V_{\text{TH}}$, the SDG clamps $V_{\text{RST}}$ at approximately $V_{\text{REF}} - V_{\text{TH}}$. While the SDG is disabled ($V_{\text{EN}}$ is off), the maximum signal difference ($V_{\text{CDSB}} \geq V_{\text{CDSN}}$) is generated which represents the bright light information. In this manner, the black-sun noise can be effectively eliminated during the dual CDS operation while maintaining the existing CIS structure and operational timing.

3. Implementation and experimental results

Fig. 3 shows the prototype chip and CIS test board. The prototype chip is fabricated using a 0.11-μm CIS process with a dimension of $4.15 \times 2.55\, \text{mm}^2$. It has a pixel array of $1024 \times 300$ with 2.9 μm-pitch 4T-APS. The prototype CIS chip demonstrates 210 frames per second (fps) with a power consumption of 30.5 mW. The test environment for the prototype CIS is comprised a chip and field programmable gate array (FPGA) board. Here, an off-chip FPGA is used to generate multiple control signals for the prototype CIS. The captured image information (the output digital signals) is transferred to the computer using a USB interface and displayed through the Microsoft foundation class library (MFC)-based interface program. To evaluate the prototype chip in various test environments, $V_{\text{REF}}$ is provided through an external DAC mounted on the CIS test board.

Fig. 4 shows the captured image while a bright light source [29] over approximately 100,000 lux is focused on the prototype CIS. Note that the measurements were taken at room temperature using an infrared-cut filter. To verify the effects of the proposed black-sun immune CDS scheme while extracting captured images, the proposed scheme was applied to only half of the rows (represented by B-region) and the other half was left unchanged (represented by A-region). In A-region, because dark spots are more visible with the bright surroundings, the image quality seems to be worse. In contrast, the dark spots in B-region are eliminated while maintaining the original image quality.

Table I compares the performance of the current study with recently published works [17, 30, 31, 32]. For a fair performance comparison, the figure of merits (FoMs) are calculated according to [33, 34]. Compared to [17], it requires an additional area of approximately $2.9 \times 110\, \text{μm}^2$, however, the proposed CDS scheme can be applied to the
existing CIS structure and control-timing which results in a better area efficiency. Moreover, the prototype CIS with proposed CDS scheme demonstrated elimination of the black-sun noise while maintaining structural advantages over a commercial CIS.

4. Conclusion

In this study, a black-sun immune CDS readout scheme is proposed for high-quality imaging in strong light conditions. The proposed CDS scheme eliminated the black-sun noise without additional complex circuitry and operational timing modifications which degrades the A/D conversion efficiency. Moreover, the proposed scheme could be easily reversed to use the conventional SS A/D algorithm, thus, it can be effectively utilized in various commercial CIS applications as one of functions to improve image quality.

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