Cryo-CMOS Band-gap Reference Circuits for Quantum Computing

Yuanyuan Yang, Kushal Das, Alireza Moini, and David. J. Reilly

Abstract—The control interface of a large-scale quantum computer will likely require electronic sub-systems that operate in close proximity to the qubits, at deep cryogenic temperatures. Here, we report the low-temperature performance of custom cryo-CMOS band-gap reference circuits designed to provide stable voltages and currents on-chip, independent of local temperature fluctuations. Our circuits are fabricated in 0.35 $\mu$m Silicon Germanium (SiGe) BiCMOS and 28 nm Fully Depleted Silicon On Insulator (FDSOI) CMOS processes, and we compare the performance of each. Beyond their specific application as low-power references, these circuits are ideal test-vehicles for developing design approaches that mitigate the adverse effects of cryogenic temperatures on circuit performance.

Index Terms—BGR, voltage reference, current reference, SiGe, BiCMOS, cryogenic temperature, cryogenic electronics, cryogenic CMOS, cryogenic ASIC, quantum computer.

I. INTRODUCTION

REFERENCE circuits producing stable and precise voltages or currents are considered foundational elements of modern integrated circuit (IC) design, and in general, set the limit on the performance of many analog systems. For semiconductor devices, it was realized in the 1950s that the material system itself readily presents a natural voltage reference in the form of the energy band-gap between valence and conduction bands, typically of order 1 eV or so [1]. Thermally activated currents however, depend exponentially on the ratio of the thermal energy to the bandgap, $E_G$, rendering a direct approach strongly susceptible to temperature fluctuations. The solution, known now for many decades [2], is in the design of a circuit that first generates a current proportional to temperature and then uses this current to produce a voltage that can cancel the original temperature dependent signal (to first order). These so-called band-gap references (BGRs) are now ubiquitous circuit blocks underpinning applications that span stand-alone voltage regulators, complex mixed-signal ICs, and system on chips (SoCs).

Although the purpose of a BGR is to produce a stable voltage that is largely immune to temperature variations, the basic semiconductor physics underpinning the functionality of the transistors themselves can limit the circuit to applications operating near room temperature. This presents a challenge for emerging technologies such as medical detectors [3], [4], space applications [5]–[9] and quantum computers [10]–[13], which will likely require complex control interfaces operating at deep-cryogenic temperatures. Under these conditions new phenomena emerge in the behavior of transistors including carrier freeze-out [14]–[17], kink-effect [14], [18], [19] and threshold voltage shift [14], [20]–[25]. At the same time, cryogenic operation also requires inherently low-power operation and noise specifications near fundamental limits.

Our focus on cryogenic reference circuits is motivated firstly by the need for stable, low-power voltage and current sources on-chip, dynamically configurable and tightly integrated with auxiliary qubit devices in a scaled-up control system. In particular, for CMOS-based control systems that can generate significant heat relative to the available cooling power at cryogenic temperatures, the use of temperature-stable integrated reference circuits can help mitigate the adverse effects arising from on-chip temperature variations. A secondary motivation stems from the use of these circuits as generic test-vehicles for examining circuit design techniques and general approaches to nullify the unwanted effects of the cryogenic environment. Bandgap references are well suited for this purpose since, at their core, they employ feedback to compensate for undesirable temperature dependence. Beyond voltage references, similar feedback approaches can be used to establish a tool-kit of circuit techniques for use in architecting cryogenic control systems.

Here we demonstrate cryogenic operation of voltage and current reference circuits specifically designed to enable applications in quantum computing, where classical electronic sub-systems are required to interface with quantum devices. Extending the use of bandgap references to the deep cryogenic regime, we compare the low-temperature performance of circuits fabricated in 0.35 $\mu$m SiGe BiCMOS and 28 nm Fully Depleted Silicon On Insulator (FDSOI) CMOS processes. By way of a simple model, for each circuit we undertake a detailed analysis of how variations in temperature and fabrication-dependent parameters lead to uncertainty in the output of the reference.

This paper is organized as follows: Section II presents our choice of technologies and circuit topologies of the designs; Section III presents experimental results of our reference circuits measured in cryogenic probe stations and dilution refrigerators over a wide temperature range; Section IV is the conclusion.
II. PROCESS AND DESIGN CHOICES

The original [27] and modified [28] BGR topologies have been utilized as one of the essential building blocks in analog ASICs. When it comes to deep cryogenic temperatures, silicon-based bipolar junction transistors (BJTs), which rely on thermally-ionised dopants, typically freeze-out to the extent that conventional BGRs are rendered non-operational. The SiGe hetero-junction bipolar transistor (HBT), due to its engineered band structure, does not suffer from carrier freeze-out [29]–[32] to the same extent and can be employed to design a BGR voltage reference.

MOS-based voltage references [33]–[39] are another alternative for cryogenic applications, despite being susceptible to an increase in uncertainty of threshold voltage that stems from process variations. This type of reference voltage is usually generated based on the diode connected MOS transistor. MOS devices are known to be functional at cryogenic temperatures [40]–[42] as the formation requires a channel inversion that does not require thermally activated carriers. Nevertheless, there are two significant challenges to implement MOS-only voltage references. The first one is commonly referred to as “kink effect” in bulk CMOS processes [14], [18], [19], in which the increase in resistance of the transistor body leads to a gating effect as charge becomes unable to dissipate. This phenomena may increase the uncertainty of a node voltage, reduce the gain of a control circuit and alter the stability margin of a feedback loop. The second challenge is the significant threshold voltage \( V_{TH} \) variation that occurs as bulk MOS devices are cooled from room to cryogenic temperatures [14], [20], [21], [25]. Addressing the challenges of bulk CMOS, we additionally implement reference circuits in a 28nm FD-SOI process. The fully-depleted feature of this process eliminates the unwanted “kink effect” [43]. Meanwhile, this technology offers back-gate control nodes to both PMOS and NMOS transistors [14], enabling in situ control of threshold voltage at cryogenic temperature.

A. BGR Designs in 0.35 \( \mu \)m SiGe Process

The first generation of our low-temperature reference circuits are designed and fabricated in 0.35 \( \mu \)m SiGe BiCMOS process. The process provides CMOS and HBT devices on the same die. We implement two versions of current mirror based SiGe BGRs, as shown in Fig. 1. The circuit on the left hand side of the figure, SiGe BGR1, follows a conventional topology of the BGR design with the purpose of benchmarking cryogenic performance. The design in Fig. 1(b), SiGe BGR2, is similar to that reported in [26]. It uses a modified start-up circuit and a frequency compensated output stage. For some of our applications, the output stage needs to directly drive other electronic systems at a different temperature via a cable. This introduces a capacitive load, and together with any parasitic capacitance at the base terminal of Q3, will reduce the stability margin of the output stage. The compensation capacitor \( C_C \) in Fig. 1(b) provides a fast signal coupling path which enhances the stability.

The SiGe BGRs in Fig. 1 employ first-order temperature co-efficient (TC) cancellation at a targeted temperature \( T_0 \). For SiGe BGR2, the output voltage is formed by a complementary to absolute temperature (CTAT) voltage at the base terminal of Q4 plus the proportional to absolute temperature (PTAT) voltage drop on R2. Without exploiting detailed low-temperature models, it is neither straightforward to directly set \( T_0 \) to a target cryogenic temperature (4K) nor possible to predict the reference voltage uncertainties due to (process-voltage-temperature) PVT variations. Nevertheless, a basic analysis of the circuit behavior provides insight into how these circuits function at low temperatures and how the room-temperature non-idealities translate into cryogenic-temperature non-idealities.

The output voltage variations due to BGR internal error sources are studied for a room-temperature BGR design [45]. Particularly, in conventional BGR designs, the device mismatches are the major error contributors. At cryogenic tem-
temperatures, it has been reported [41], [46] that the threshold mismatch in CMOS current mirrors becomes larger than its room-temperature value. We can readily identify M5 - M7, R1 and R2 are matching critical devices in BGR1, see Fig. 1(a). As the current mirrors set the PTAT current and output current value; the resistors set the PTAT part of the output voltage. In BGR2, see Fig. 1(b), in addition to that of BGR1, the BJTs Q1, Q2, and Q3 are match critical elements, as Q5 mirrors the PTAT current in the output stage.

| ATM | Bypass |
|-----|---------|
| Main Controller and Registers | MUX Control |
| Short Channel MOS-Only V_{sas} | I_{sas} |
| Short Channel BGR V_{sas} | |
| Long Channel MOS-Only V_{sas} | |
| Long Channel BGR V_{sas} | |
| I_{sas} | Enable |

Fig. 3. Simplified test architecture of our 28 nm FDSOI CMOS SoC. This architecture is modified according to the scope of this paper.

B. Reference Designs in 28 nm FDSOI

Despite the potential suitability of our SiGe BGRs for cryogenic operation, the use of this technology platform for complex, mixed-signal applications is limited, in particular with respect to ultra-low power operation required for quantum computing. The 28 nm FDSOI CMOS technology provides a platform for implementing logic and analog circuits using a 1 V supply to achieve better power efficiency. There has also been work showing sub-1 V operations of low-voltage BGR circuits [47]–[51]. At low temperatures, the increase in threshold voltages for both PMOS and NMOS transistors reduces the voltage headroom for proper circuit operations, which pose significant design challenges for analog circuits. For this reason, we implement our reference circuits using I/O devices with thicker oxide and operate them at 1.8 V power supply.

There are two different strategies to configuring the back-gate control terminals in this technology, as shown in Fig. 2. From both of the cross sections in the figure, we can see that the NMOS transistor’s back-gate control voltage N_{BG} cannot go below the ground potential V_{SS}. This means we cannot obtain high threshold voltage NMOS devices via back-gate controls. In fact, we would like to reduce the threshold voltages of the MOS transistor for our low-temperature applications. In the approach shown on the left in this figure, we can see that the PMOS back-gate control voltage P_{BG} cannot be higher than the NMOS back-gate voltage N_{BG} and when it comes to extreme high back-gate biases (beyond the value of power supply voltages), this scheme will have higher voltage stress at the PN junction interface of D1 and D2 compared to the cross section shown on the right of the figure. The scheme on the right mimics a traditional triple well CMOS technology, and it provides more freedom for the choice of back-gate voltages due to the physical separation of the P_{BG} and N_{BG}. In Fig. 2(b) using a clean power supply, V_{DD}, better noise isolation between the PMOS and NMOS devices can be achieved, as they are physically isolated. For the above reasons, we place and route our digital blocks using the cross section shown in

**Fig. 2.** Cross section view of the FDSOI technology. N_{BG} is the back-gate control terminal of NMOS transistors and P_{BG} is the back-gate control terminal of PMOS transistors.

**Fig. 3.** Simplified test architecture of our 28 nm FDSOI CMOS SoC. This architecture is modified according to the scope of this paper.

**Fig. 4.** Circuit schematic diagram of the ATM buffer amplifier.
Our reference voltage and current generation circuits have been implemented as part of an SoC. The simplified chip architecture is presented in Fig. 3. In this chip, commands are sent through a serial-parallel-interface (SPI). An Analog Test MUX (ATM) is implemented to buffer the voltage reference signals when driving the load from external test and measurement instruments. The buffer uses a rail-to-rail amplifier topology and its circuit diagram is presented in Fig. 4. The ATM can be bypassed when performing current reference tests.

We implement the reference circuits by configuring transistors of different length. In the short channel version of the circuit, the long transistors (L > 0.5 µm) are replaced with a number of shorter series transistors with L < 0.5 µm. The current reference circuits are all implemented using short channel devices.

The MOS-only voltage reference shown in Fig. 5 is based on a modified form described in [52]. We have added two dynamic start-up circuits, because at low temperatures the start-up mechanism which relies on leakage current may not function properly. Without a “kick” on the gate of M6 and M7, the node voltage on X and Y will be almost zero as there is no current flowing through both of the two branches. At room temperature, there may be a small leakage current flowing through M6 and M7. The voltage at node X will still be around zero and the voltage at node Y can be around the threshold voltage of M1 - M4. Then the leakage current through M2 may become large enough to drive the M6 and M7 gate voltage low to bring up the voltage at node X and Y. Then the circuit starts to function as designed. For low temperature applications, the start-up may take a very long time. Therefore, we have added the start-up circuit on the right hand side.

Notice that at low current the Y node has a higher impedance than the X node, as the Y branch would not conduct current until the node voltage at Y reaches around the threshold voltage of M1 - M4. The X node sees a constant impedance of R1. Then at high current, the Y node must see a lower impedance than the X node to maintain stability at DC. As described in [52], the transistors M1 - M4 operate at the edge of linear and saturation region to achieve zero temperature co-efficient (ZTC) current as well as ZTC drain voltage.

We consider that transistors M1 - M4 are effectively one long transistor MX. We first assume MX works in saturation region and due to the amplifier formed by M1 - M5, the node voltage at X and Y will be the same. Thus, we reach the following expressions:

\[
\frac{1}{g_{m, sat}} = \frac{1}{\sqrt{2I_D \mu C_{ox} \frac{W}{L}}} + \frac{V_{th}}{I_D}
\]

\[
R_1 = \frac{2}{\sqrt{2I_D \mu C_{ox} \frac{W}{L}}} + \frac{V_{th}}{I_D} = \frac{2}{g_{m, sat}} + \frac{V_{th}}{I_D},
\]

where \(g_{m, sat}\) is the transconductance of MX in saturation region and \(I_D\) is the current in both of the X and Y branches. Similarly, if MX works in the linear region, then we can have:

\[
\frac{1}{g_{m, lin}} = \frac{\mu C_{ox} \frac{W}{L} V_{DS}}{2I_D} + \frac{V_{DS} + 2V_{th}}{2I_D}
\]

\[
R_1 = \frac{1}{\mu C_{ox} \frac{W}{L} V_{DS}} + \frac{V_{DS} + 2V_{th}}{2I_D} = \frac{1}{g_{m, lin}} + \frac{V_{DS} + 2V_{th}}{2I_D},
\]

where \(g_{m, lin}\) is the transconductance of MX in linear region and \(V_{DS}\) is the drain to source voltage of MX. It can be seen that for both operating conditions, the impedance of Y branch is always smaller than that of X branch. Therefore, the Y and X branches form the positive and negative feedback loops respectively. For stable operations, we would like to ensure the negative feedback loop is always “stronger” than the positive feedback loop. That is to say, at all frequencies, the impedance at node Y should be smaller that the impedance seen at node X, which has already been indicated by (1) and (2) for DC. Frequency compensation of the two coupled loops can be performed similar to what is commonly done in low drop-out (LDO) voltage regulators, by adding zeros in the form of additional equivalent series resistance (ESR). The zeros from \(C_{C1}, R_{C1}\) and \(C_{C2}, R_{C2}\) cancels the internal pole at the gate of M6 and M7 for individual loops. The compensation load

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Fig. 5. MOS-only voltage reference implemented using 1.8 V I/O transistors in 28 nm FDSOI CMOS process.
capacitors $C_1$ and the impedance seen at node X create an output pole $p_{01}$ at this node. Similarly another output pole $p_{02}$ can be identified at node Y. It is obvious that $p_{02}$ frequency is lower than that of $p_{01}$, which maintains stability of the entire circuit.

We simulated this circuit and obtained the following performance and sensitivity parameters as shown in Table I and Table II respectively. It can be seen from Table I that the output reference voltage is closely related to process parameters such as the threshold voltage of $M_X$ and the absolute value of the on-chip resistors. These two parameters change at low temperatures. In addition, the matching for resistor $R_{2a}$ is also important to the designs. For those reasons, we implemented binary based trimmings to both $R_1$ and $R_{2a}$ in Fig. 5 and the LSB accuracy is about 1% of the individual resistor value. The back-gate control node can also be used to tune the threshold voltage of $M_X$ at low temperature. We note that the simulated nominal output reference voltage is now 494 mV after implementing trimmings.

In this 28 nm FDSOI CMOS process, we have also implemented a conventional BJT based BGR circuit as a experimental comparison. Due to the increase in threshold voltage in MOS transistors, we shifted the cascoded current mirror BGRs into a low supply voltage oriented design, as shown in Fig. 6. This circuit is powered by 1.8 V supply. Multiplexers are used to switch among different types of BJTs (the lateral PNP or vertical NPN) and PN junctions.

The current reference provides bias current for most of the analog sub-modules of the chip. The current reference is designed using existing voltage reference topologies. We have implemented a conventional BJT based BGR, a BJT based BGR current generator and a MOS-only voltage reference for this current reference. The simplified diagram is shown in Fig. 7 which only shows one version of voltage to current conversion. In this design, we employ a multiplexing scheme as we expect the BGR circuits using normal silicon BJTs will freeze-out at temperatures below 60 K. Due to the negative TC of the on-chip resistors, the voltage references cannot be directly plugged in for voltage to current conversion. In fact, we have generated a CTAT voltage and applied it to the resistor $R_{buf}$ to create a ZTC reference current. Resistor trimming has been used, for example, $R_3$ in BGR circuit and $R_1$ in MOS-only reference circuit. The trimming range of $R_{buf}$ covers approximate ±60% of the range with Least Significant Bit (LSB) accuracy of 2%.

### III. Cryogenic Measurements

We fabricated two BGR-based voltage reference circuits in 0.55 $\mu$m SiGe BiCMOS process. The chip photo is shown in Fig. 8. BGR1 is a conventional SiGe HBT based current mirror BGR and the BGR2 has an output buffer stage, (see Fig. 1 for schematic diagrams). We have also implemented four voltage reference circuits and three current references in a 28 nm FDSOI CMOS process. The chip photo is presented in Fig. 9 in which, we have also displayed the layout of the circuits as the chip is fully covered by density fills. In this figure, $V_{REF1}$ is the long channel voltage references and $V_{REF2}$ is the short channel version.

The SiGe BGRs are tested in a LakeShore CRX-4K closed cycle refrigerator (CCR) based cryogenic probe station with

**TABLE I**

| Performance | Simulation results |
|-------------|--------------------|
| Nominal $V_{REF}$ | 503 mV |
| Minimum $V_{DD}$ | 0.8 V |
| Temperature range | -40°C - 150°C |
| Temperature co-efficiency | 1.3 ppm/°C |

**TABLE II**

| Error sources | $V_{REF}$ deviations |
|---------------|----------------------|
| $V_{th}$ vary by 1 mV | $M_X$ | 1 mV |
| $V_{th}$ mismatch by 1 mV | $M_1$ and $M_2$ | 0.15 mV |
| $V_{th}$ mismatch by 1 mV | $M_3$ and $M_4$ | 0.11 mV |
| $V_{th}$ mismatch by 1 mV | $M_6$ and $M_7$ | 1 mV |
| Resistor values vary by 1% | $R_{1}$, $R_{2a}$ and $R_{2b}$ | 1.1 mV |
| Resistor mismatch by 1% | $R_1$ | 0.45 mV |
| Resistor mismatch by 1% | $R_3$ | 1.6 mV |
| Resistor mismatch by 1% | $R_{2b}$ Negligible |
LakeShore TC336 temperature monitor and control unit. This setup enables a wide temperature range sweep from 250 K to 6 K. The probe station is not fully enclosed by the radiation shield limiting the base temperature to 6 K. The advantage of using a cryogenic probe station is fast turn-around time (cools down and warms up quickly due to small thermal mass) and temperature control for the test samples. The temperature of the probe station can be set and stablized to a given value.

We have measured the SiGe BGRs and plotted the output voltage with respect to temperature in Fig 10. The output voltage is recorded using Keysight 34460A digital multi meter (DMM) with load impedance set to 1 GΩ to minimize loading to the BGR circuits. The room-temperature current consumptions of BGR1 and BGR2 are 4 µA and 4.8 µA respectively from a 3.3 V power supply. At low temperature (6 K), we need to increase the power supply voltage to 3.6 V due to increased threshold voltages in both PMOS and NMOS transistors. The currents consumed by BGR1 and BGR2 reduce to about 0.4 µA and 0.5 µA respectively, corresponding to power consumption of approximate 1.5 µW and 1.8 µW respectively. We believe this is due to the reduction in PTAT currents in BGRs.

The maximum deviation of output voltage from BGR1 is 26 mV across the measured temperature range (6 K to 250 K), resulting in a TC of 107 ppm/°C. BGR2 has a maximum
reference output voltage change of 37 mV, indicating a TC of 152 ppm/°C. These temperature stability performances are comparable with the one in [26] and our BGRs consumes much less power at cryogenic temperature (1.5 µW and 1.8 µW versus 130 µW).

Power-supply sweep tests are performed at 4 different temperatures as shown in Fig. 11. We observe that the BGR circuits start to work at higher supply voltages when the temperature is lowered, as the threshold voltage increases at low temperatures. The hysteresis between power-up and power-down becomes large at low temperatures. At 6 K, low power-supply design techniques may be necessary for many of the analog designs.

The noise performance of the SiGe BGR circuits are shown in Fig. 12. In this experiment, the output of the BGRs are connected to Stanford research systems (SR560). The output of the amplifier is captured using a digital scope. The purpose of using this setup is that the BGRs cannot directly drive the input load of the scope. We can see that at low temperature, the low-frequency noise of both of the two BGRs is higher than their room-temperature counterparts. BGR1 and BGR2 show similar room-temperature noise performance, and at cryogenic temperatures, the 1/f noise from the MOS transistors, especially from the current mirrors increases the output noise. At low frequencies, BGR1 and BGR2 have similar noise characteristics. The BGR2 shows a higher noise power spectral density at the mid-frequency range at low temperature compared to BGR1. It is likely that at low temperature, due to drastically reduced bias current in all circuit branches, the loop bandwidth of the output buffer in BGR2 becomes too narrow to provide efficient feedback. Although a compensation capacitor is implemented in BGR2 output buffer stage, see Fig. 1(b), it is not effective to provide a noise coupling path at this mid-frequency range. Therefore, the noise current from M7 and M8 cascade sees different impedance at the drain side of M8. In BGR1, this impedance is approximately R2 plus the impedance of diode connected BJT. In BGR2, the noise current cannot pass through the base of Q3, because when there is a small base current, Q3 will source a large current from the supply to bring up the emitter voltage. Therefore, this noise current sees roughly a collector-emitter resistance, which is typically higher than that in BGR1, and converts into a noise voltage. At higher frequencies, the compensation coupling capacitor begins to be effective and a noise cancellation path via Cc and Q4 can be identified.

The reference circuits taped-out in 28 nm FDSOI CMOS technology are measured in a BlueFors XLD dilution refrigerator. In this setup, we first acquire data at room temperature, then we cool down the sample in the fridge and perform measurements whenever a predetermined temperature is reached. For the long channel MOS-only voltage reference circuit trimming test, we trim R1 and R2a and apply zero back-gate control voltage, (see Fig. 5 for circuit diagram information). The measurement results are shown in Fig. 13. We implement 6-bit trimming for both of these resistors. Due
Fig. 12. Measured SiGe BGRs’ noise performance at room temperature and 6 K. (a), BGR1 noise performance; (b), BGR2 noise performance.

Fig. 13. Measurement results on resistor trimmings in the long channel MOS-only voltage reference circuit with zero back-gate control voltage: (a), $R_1$ trimming with $R_{2a}$ set to its nominal value, the bigger the trimming code number, the lower the resistance; (b), $R_{2a}$ trimming with $R_1$ set to its nominal value, the bigger the trimming code number, the lower the resistance.

Fig. 14. Measurement results on long channel MOS-only voltage reference circuit for different back-gate control voltages along with the temperature sweep. The back-gate control voltage is noted as “Vbg” in the figure.
offset is measured by applying an external 1 \( \mu \)A current to both the input current and subtracting the input current from the output current. A negative value indicates the output current is smaller than the input current. This result can be experimentally reproduced across different sample chips, likely due to the excessive number (32 in our case) of short-channel transistors implemented for \( M_{X1} - M_{X4} \). At low-temperatures, the source and drain resistance may potentially increase. We can see at higher back-gate voltages, while the threshold voltage of the output transistor decreases, the increase of source and drain resistance takes a larger portion of the output voltage, which results in larger voltage differences between the short-channel and long-channel voltage references. Further increase back-gate voltages, i.e. from 1.66 V and above, referring to Fig. 5, the output transistors’ threshold voltage will reduce and thus the current in both X and Y branches. The amount of voltage drop on the increased source and drain resistance tends to decrease which results in output voltage different decrease.

The MOS-only current reference shows similar trend as the voltage reference circuit, shown in Fig. 17(a). The main reason is the similar circuit topology used in Fig. 7. The current mirror, which is the last stage of the current reference, is also tested for its offset characteristics using an external 1 \( \mu \)A current. The difference is taken via subtracting the input current from the output current. The large negative values

(which are off the scale of this plot) are mainly due to the ATM MUX switches, which short the measurement instrument to the chip ground at high back-gate voltages. We can see that at low end of the measured temperature range, the output current tends to have a smaller values of a given input current, perhaps due to the matching property changing in the MOS transistors for a high back-gate bias. The offset reaches a peak of approximate 7.5% at 1.66 V back-gate control voltage.

We have also performed resistor trimming test during the temperature sweep. In this test, we use MOS-only voltage reference in Fig. 5 to drive the current generator circuit (Fig. 7) and we trim \( R_1 \) and \( R_{buf1} \) independently. Trimming \( R_{2a} \) resistor (Fig. 5) has a similar effect as trimming \( R_{buf1} \), as both of them shift the curves vertically, but \( R_{buf1} \) has a much wider trimming range. The resistor trimming experiment results are presented in Fig. 18. In this measurement, we apply zero back-gate bias.

The silicon BJT based BGRs in this 28nm FDSOI process fail at about 40 K according to our measurement. The back-gate control does not shift the output voltage of such a BGR circuit as the output voltage of this type of reference is not a function of the threshold voltage of the MOS transistors. For different types of BJTs (lateral PNP and vertical NPN in

- **Fig. 15.** Transistor level switch diagram used in ATM MUX. The ground-connected NMOS transistor shunts off-switch noise when two transmission gates are turned OFF.
- **Fig. 16.** Short channel version MOS-only reference voltage minus that of long channel version.
- **Fig. 17.** Measured current reference at different temperatures using back-gate controls. (a) Reference output using nominal trimming values for \( R_1 \) and \( R_{buf1} \); (b), measured current mirror offset at different back-gate biases. The offset is measured by applying an external 1 \( \mu \)A input current and subtracting the input current from the output current. A negative value indicates the output current is smaller than the input current.
higher temperature applications. Circuits will not function at 4 K, they can still be used for cryogenic applications, particularly those that relate to engineering a scalable control interface of a quantum computer.

IV. CONCLUSIONS

In conclusion, we have presented cryogenic operation of bandgap reference circuits fabricated in both 0.35 μm SiGe BiCMOS and 28 nm FDSOI CMOS processes. These references demonstrate low power operation across a wide range of temperatures from 300 K to 4 K. The measured power consumption of SiGe BGRs are 1.5 μW and 1.8 μW respectively at the measurement temperature of 6 K. The reference circuits based on MOS-only topologies in 28 nm FDSOI CMOS process remain functional on an SoC down to 4 K temperature. Taken collectively these results and design techniques establish the performance of bandgap references for cryogenic applications, particularly those that relate to engineering a scalable control interface of a quantum computer.

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