Research and practice of three-phase signal source design based on DDS technology

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Abstract. This paper analyzes the working principle and basic structure of DDS, combined with the design points of three-phase signal source based on DDS technology, including software development platform, hardware description language, sinusoidal signal, AM module, FM module, ASK modulation and demodulation, system assistant, system top, etc. The purpose is to improve the application value of DDS technology and the application effect of three-phase signal source.

1. Introduction
Based on the previous practical experience, we can understand that in the operation of the test system, the signal generator is an important communication carrier, and its working state stability will also affect the working quality of the system. Direct digital frequency synthesis (DDS) technology as a new type of synthesis technology, through its application to the design of three-phase signal source, not only can improve the stability of signal transmission process, but also can reduce the signal phase noise, improve the speed of signal frequency switching.

2. The working principle and basic structure of DDS
2.1. Working principle

Direct digital frequency synthesis technology (DDS) is to synthesize new transmission signals by digital processing of the content to be transmitted, so as to explore the frequency synthesis law. As an attribute of the signal, phase is used to measure the change of the signal waveform and reflect the state of the signal at each moment. The so-called direct digital frequency synthesis is aimed at the characteristic that the phase can increase linearly with the external reference clock. According to the Nyquist sampling theorem, the required signal is synthesized by querying the sinusoidal table. The process of synthesizing signals based on DDS technology is shown in Figure 1. Taking sinusoidal signal as an example, it is assumed that a periodic sinusoidal signal with a fixed frequency is Q(t). At this time, the signal is sorted out and the discretized analysis is carried out by using the time domain theorem. The discretized signal...
is denoted as \( Q(T_1), Q(T_1 + A), Q(T_1 + 2a), Q(T_1 + 3a), \ldots, Q(T_1 + ma), \) and \( Q(t) = Q(t_1) + Q(t_1 + A) + Q(t_1 + 2a) + Q(t_1 + 3a) + \ldots + Q(t_1 + ma), \) \( m=1,2,3, \ldots M. \)

2.2 Basic structure

2.2.1 Phase accumulator

The structure of the phase accumulator is shown in Figure 2. The initial phase value of the adder is \( \theta \), the reference clock frequency is \( f_c \), and the frequency control word is \( K \). When the first clock pulse arrives, the adder adds \( \theta \) to \( K \), and inputs the result \((\theta+K)\) into the register. The register does two things with the received \((\theta+K)\): On the one hand, it sends it to the next level as the lookup address; On the other hand, it feeds back to the adder input. When the second clock pulse arrives, the adder adds the feedback \((\theta+K)\) from the previous period to the frequency control word \( K \). The result \((\theta+2K)\) is also input into the register and serves as the adder's input value when the next clock cycle arrives. When the last phase value stored in the register is \((\theta+2nK)\), the accumulation can be stopped. The time from the initial value to the overflow of the register is the period of the synthesized signal. When the initial phase \( \theta \) is equal to 0, the accumulated phase has a linear relationship with the frequency control word \( K \).

![Fig. 2 Analysis of working principle of phase accumulator](image)

2.2.2 Waveform memory

Waveform memory is often called sinusoidal query table because, although in theory, waveform memory can store the phase and amplitude information of arbitrary waveform periodic signal, in practical application, Mostly give priority to in order to store the information of sinusoidal signal its main function is to synthesize the phase accumulator containing phase information of the N bit binary code into the corresponding D a binary code contains the amplitude information, which in each reference clock cycle, will pass to superiors phase information as the address, read the corresponding address corresponding to the amplitude information query table. At the same time, it can be learned from experience that the larger the length of the data word \( D \) in the ROM of waveform memory is, the more the values stored in the query table are. Moreover, theoretically, the larger \( D \) is, the smaller the quantization error is. Therefore, the error in the quantization process can be reduced by increasing the number of digits of the phase accumulator.

2.2.3 Digital-to-analog converter

In the application process of DDS technology, the digital-to-analog converter also belongs to a very important part, in practical application, its main role is to process the binary discrete sequence after the superior, according to a certain order to complete the analog signal conversion, the obtained signal continuity is strong, can meet the corresponding transmission needs. But from the point of practical application, the resulting analog signals on the application is not a completely smooth sine wave, but consists of a number of small rectangular, it also means in signal processing, the reduction of only 90% to 95%, in other ways, residual signal is needed to complete the transformation, so as to meet the job requirements. Based on this, in the design of DDS chip, also need to use high conversion rate of digital
to analog converter, with D/A converter, can successfully complete the conversion of parameter information and high-precision processing, so as to improve the application quality of the output signal.

2.2.4 Low pass filter
In the process of system operation, the low-pass filter expands and smoothing the sinusoidal signal generated during the operation of the previous step of the system, so as to filter out some aliasing signals better and improve the purity of the output result of the signal, so as to meet the filtering requirements of the signal. D/A converter in the application process, can carry on the comprehensive processing to the stray component, understand the relevant law of the existence of the signal, under normal circumstances, its central law will be the reference clock law integer times. And according to the spectrum analysis results, we can know that the stepped sinusoidal signals generated include not only the main frequency signals, but also other multiple harmonic signals, which meet the requirements of signal development. In order to filter out the redundant harmonic components smoothly, the reference clock frequency is also installed at the output end of the D/A converter, and based on this, the system is optimized and the practicability of the analysis results is improved.

3. Design points of three-phase signal source based on DDS technology

3.1 Software development platform
In the design process of three-phase signal source, the primary task is to establish a software development platform with strong compatibility, so as to give full play to the application advantages of DDS technology. In terms of practical application, the commonly used development tool is Quartus series, which also provides a more complete platform design environment to meet the corresponding design requirements. Based on Quartus software, VHDL and Verilog logic synthesizer are embedded inside the software. In this case, language description can be better completed, and the frequently used FPGA Compiler series software can also intuitively reflect the system simulation function to meet the updating requirements of the system. From the actual application, the compatibility of the system can reach more than 90%, and also has a strong expansibility, which also lays a good foundation for the smooth realization of subsequent software performance.

3.2 Hardware description language
In the process of system operation, also involves the hardware description language, this is a kind of advanced programming language, would be able to complete the function of the logic circuit, and also need to circuit connection status, scheduling, and circuit function analysis, this can go smoothly in the application of different abstract level analysis, meet the demand of the design of the system. However, compared with other programming software, this kind of language also has a strong parallelism in the application, and the frequently used description languages mainly include VHDL hardware description language and Verilog HDL hardware description language. Taking VHDL Hardware Description Language as an example, the main program structure included in this language is as follows: First, entity. The main function of this structure is to successfully associate with external interfaces to meet the corresponding operation requirements. Second, the structure, whose main function is to complete the processing of design units and meet the relevance processing of input and output relations [1]. Third, configuration. The main function of this structure is to screen the corresponding support system according to the requirements in the existing library to meet the operational requirements of the system. Fourthly, the package set, whose main function is to store the shared data of different modules, belongs to the design unit that can be compiled. Fifth, libraries, which hold pre-compiled packages.

3.3 Sine signal
Based on DDS technology, its internal is mainly composed of phase accumulator and sinusoidal lookup table, while in the processing of the peripheral part, it is mainly composed of two parts of the digital to analog converter and filter content. From the actual composition, this part of the design process, its
content includes the system clock, phase accumulator, three-phase phase controller, waveform memory, signal module and so on. Taking the system clock module as an example, the clock module with frequency division processing needs to be selected in the optimization design to provide working clock for other modules. During the clock operation, the reset signal, the clock signal (mainly 50MHz) and the output signal module are included to match different application frequencies so as to meet the corresponding management requirements.

3.4 AM module
In the application of communication field, in order to ensure the stability of signal transmission, the actual situation needs to be combined with the signal modulation processing, the signal in the processing process, can also control the carrier parameters reasonable control, so that the amplitude modulation can be successfully completed, so that it can be maintained in a relatively stable application state. In the specific application process, its circuit diagram is shown in Figure 3. Its structure is mainly composed of DDS circuit (carrier DDS circuit and modulation DDS circuit), adder and multiplier, thus forming a stable operation of DDS amplitude modulation circuit. At the same time, in the system design, the ROM module data will also be sorted out, and its output content is mainly represented by 0 ~ 255 sinusoidal signals, and these signals need to be sorted out in advance when they are processed, so that the data application rate can be increased to more than 95% [2].

![Fig. 3 Schematic diagram of AM module circuit](image)

3.5 FM module
In the process of communication engineering operation, in order to ensure the stability of the signal processing process, it is also necessary to complete the FM processing according to the requirements, which is also an important value of FM module design. In the process of signal processing, it is also necessary to control the carrier instantaneous frequency reasonably, so as to successfully complete the frequency modulation, so that it can be maintained in a reliable working state. From the actual application situation, the structure is mainly composed of DDS circuit as the application carrier, with the corresponding processing signal and FPGA module, so that the signal can be implemented smoothly, and then improve the practical value of the processing results. In the signal modulation process of the system, the bit width of the phase accumulator in the DDS module will be processed with 16 bits. In this way, the signal quantization processing can be completed smoothly, so as to meet the specific processing requirements [3].

3.6 ASK modulation and demodulation
In the signal design process, it is also necessary to do ASK modulation and demodulation processing, which is the key to improve the stability of the system. From the specific design situation, ASK will use unipolar non-return to zero code as carrier frequency control in its application, and it also needs to complete binary digital signal processing with the help of conventional theory to meet the practicability
of signal processing results. And in the ASK signal processing process, the multiplier will also be used to assist signal processing, and the signal sequence will be processed in the application to meet the spectrum shift processing. In addition, in the signal processing process, the multiplier can also completely solve the high and low frequency harmonic interference, so that the output signal can meet the detection and control requirements, thus improving the practical value of the signal processing results and meeting the signal processing requirements [4].

3.7 System auxiliary
In order to stabilize the signal transmission process, it is also necessary to do a good job in the auxiliary design of the system. From the perspective of practical application, the following contents should be considered in the auxiliary design: First, display control design. Based on previous design experience, it can be learned that dynamic scanning mode is mostly used for design. In the processing background of such application modules, dynamic processing can be carried out in the clock signal, thus improving the accuracy of digital tube display results [5]. Second, keyboard interface design, from the point of practical application, the system can use DDS frequency control system as a standard interface design, but also in the application will use a PS / 2 keyboard interface to its associated with FPGA system together, and the interface can also use the generic circular plug, so the system can also help them more stable operation.

3.8 The top system
Design content in addition to the above mentioned, in the process of three-phase signal source design, the top design work, also need to pay attention to the system can be used in the specific design content of analytic hierarchy process (ahp) to assist in the design, will have been generated element combination in the new principle of the graphic, and gets the top to the system entities, with engineering translation process, enhancing the use value of the results of the analysis. From the point of view of specific application, the system will be optimized on the FPGA system, and I/O pins will also be used to complete the arrangement of device models. With the corresponding application schematic diagram and PCB board, the top-level file design of the system can be realized smoothly, which also lays a foundation for the smooth progress of system debugging. At the same time, it also improves the stability of working state by 60%-70% [6].

4. Simulation test and performance analysis

4.1 System Simulation
In the process of system simulation, attention should be paid to the following contents: First, do a good job in the control of software parameters. In the specific application, the clock signal processing will be carried out in the input logic. In general, the clock parameters can be controlled within 10-50KHz. In addition, signal sampling content processing will be completed in the "Sample" column of the Data box, so as to improve the use value of Data analysis and processing results [7]. Second, in the process of use, the parameters of Signal Tap II should be optimized as required. For carrier signals involved, the Signal frequency should be controlled at 10-50KHz, and the sampling clock frequency should also be controlled above the maximum frequency value of the measured Signal, such as it can be set at more than 100KHz. Analyze relevant parameters of Signal Tap II to obtain corresponding data.

4.2 The system test
In the system test process, mainly includes the following points: First, the signal output test, combined with the DDS equation to complete the three-phase sinusoidal signal frequency calculation, according to the theoretical situation, its value should be controlled in the reference clock frequency 1/2, after several measurements, the summary of reliable test results. Second, for AM, FM and ASK test, three test is similar to the requirements of the relevant, are combined with DDS equation to complete test data statistics, but also need to advance to determine, amplitude, frequency, numerical and theoretical value
to formulate standards, then the test results were compared with standard value, to get reliable data analysis results, to meet the specific application requirements [8].

4.3 System performance analysis
According to get the test results, can get the following results: (1) Performance signal relative bandwidth, under the background of DDS equation, the resulting relative bandwidth value is 85% of the theoretical value, it will also analyze the exponential level content, according to the analysis results can learn, relative bandwidth signal is larger, can better meet the demand of application [9]. (2) Frequency resolution, combined with the application nature of DDS technology, the resolution of its output signal will be controlled within 10-20Hz, and the system has strong reconfiguration, which can facilitate the system to be modified more flexibly, thus improving the convenience and practicability of the system overhaul process.

5. Conclusion
To sum up, in the design process of three-phase signal source, DDS technology has a good application value. By relying on DDS technology to optimize the three-phase signal source system, it can not only improve the integrity and practicability of the system content, but also has a positive significance for improving the stability of the system operation.

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