Fast LDO Handles a Wide Range of Load Currents and Load Capacitors, up to 100 mA and Over 1 µF

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ABSTRACT This paper proposes a low dropout voltage regulator (LDO) that exhibits both a fast response to load transients and the ability to handle practically any load capacitor. Starting from a typical LDO topology, an error amplifier (EA) that drives a PMOS pass transistor and a passive feedback network, we inserted a novel circuit, with the input AC-coupled to the LDO output and the output connected directly to the pass transistor gate. This circuit creates an inner feedback loop able to react quicker than the main feedback loop to variations in the output voltage, and appropriately inject or sink current to/from the gate node. Moreover, the inner feedback loop helps reduce the equivalent small-signal impedance at the LDO output, which in turn reduces the impact the pole associated with the output node has on the LDO stability. A compact circuit implementation of this topology is presented in this paper: it combines the proposed fast transient & frequency compensation circuit with a high slew-rate EA. The resulting LDO was integrated in a 130 nm standard CMOS technology. The measurement results are in good agreement with simulations and validate the concept and design. The LDO provides a steady 1 V output with the supply voltage varying from 1.2 V to 1.5 V and the load current going up to 100 mA. Its fast response to load transients helps maintain the output voltage overshoot and undershoot below 250 mV for $C_L = 0$ and under 60 mV for $C_L = 1$ µF, when the load current varies between 1 µA and 100 mA in 1 µs. The LDO requires only 6.2 µA of quiescent current and occupies 0.018 mm² of die area.

INDEX TERMS Any load capacitor, fast-transient LDO, high slew-rate error amplifier, fast response to load transients.

I. INTRODUCTION

A standard LDO consists of an error amplifier (EA) that drives a PMOS or PNP pass transistor, and a passive feedback network, as shown in Fig.1(a). Its frequency characteristics are largely determined by two poles: the first is associated with the gate of the pass transistor, while the second is associated with the LDO output node. The latter depends on the load current, $I_L$, and load capacitor, $C_L$. Therefore, the wider the ranges of $C_L$ and $I_L$ values that need to be accommodated, the more difficult it is to ensure the LDO stability. A typical solution is to employ a Miller-type pole-splitting frequency compensation. However, this approach reduces the gain-bandwidth product (GBW) of the LDO, impairing its dynamic performance. Fig.1(b). shows the typical LDO response to steep variations of the load current: as $I_L$ increases, the output voltage decreases sharply; it takes the time $\Delta t_1$ for the feedback loop to arrest the decrease and start bringing $V_{OUT}$ back to its steady-state value. A similar scenario is shown when $I_L$ decreases sharply, only this time $V_{OUT}$ increases for the period $\Delta t_2$, before the loop starts correcting the $V_{OUT}$ variation. The maximum variation of the output voltage, $\Delta V_{undershoot/overshoot}$, and the periods $\Delta t_1, \Delta t_2$ can be approximated as follows [1]:

$$\Delta V_{undershoot} \approx \Delta t_1 \frac{I_{L\_max}}{C_L}$$
$$\Delta V_{overshoot} \approx \Delta t_2 \frac{I_{L\_max}}{C_L}$$

(1)
where $BW_{cl}$ is the closed loop bandwidth of the system, $t_{sr}$ is the slew-rate time - the time needed to charge/discharge the parasitic gate capacitance of the pass element, $\Delta V_{GATE}$ is the voltage variation at the gate of the pass transistor and $I_{GATE, sr}$ is the maximum current available to discharge and charge the capacitance $C_{GATE}$ at that node GATE, $A_{v, pass}$ is the voltage gain of the Mpas and $C_{GS}, C_{GD}$ are the gate-source and gate-drain capacitances of the pass transistor. Equations (1) and (2) show that by increasing the $I_{GATE, sr}$ current, the overshoot/undershoot of the regulated voltage can be reduced. However, this usually comes at a cost in quiescent current.

Most solutions proposed in the literature for speeding up the LDO response to load transients employ an additional feedback loop, connected directly between the LDO output and the gate of the pass transistor, as illustrated in Fig. 1(a) by the dotted line rectangle. This second feedback path improves the transient response of the LDO, otherwise limited by the GBW of the main loop [2].

In [2], a capacitor is connected between the LDO output and the source of a cascode, so that the output voltage variations are sensed and converted into a current signal, which is then amplified and conveyed to the gate of the pass transistor. This fast path increases momentarily the $I_{GATE, sr}$ current available to discharge the parasitic gate capacitance. However, the output voltage overshoot remains relatively large and the maximum $C_L$ value the LDO proposed in [2] is stable for, is only 100 pF. The solutions proposed in [3] and [4] use operational transistor amplifiers with enhanced slew rate and adaptive biasing; they require less quiescent current and are more effective in reducing the output voltage overshoot than the LDO proposed in [2], but they, too, cannot handle load capacitors larger than 100 pF.

LDOs designed to operate with external capacitors usually have a narrow closed-loop bandwidth, and rely on the charge accumulated by the $C_L$, usually with values in the $\mu$F – tens of $\mu$F range, to reduce the output voltage variations caused by steep load transients. The $C_L$ Equivalent Series Resistance (ESR) diminishes the effectiveness of this approach, but it may help improve the stability of LDO. Moreover, the impact a large decoupling capacitor can have on reducing the variation in the voltage delivered to a load located inside the IC is further diminished by the parasitic series inductance and resistance of the track between the internal load and the external $C_L$.

The need for LDOs able to handle a wide range of load currents and capacitors, while providing a fast response to load transients, has been increasing steadily. Analog Devices registered the term anyCAP as a trademark and provides LDOs that ensure stability for all types of external capacitors and over a wide range of $C_L$ values [5]. The LDO proposed in [6] uses an EA based on the flipped-voltage-follower structure, with a slew rate enhancement technique for fast transient response, and a feed-forward frequency compensation network that ensures stability for $C_L$ values up to 2 nF. However, it requires a large quiescent current, between 50 $\mu$A and 190 $\mu$A. The LDOs proposed in [1] and [7] rely on pole-zero cancellation realized by a parallel amplifier structure, or by a modified pass element with several transistors connected in parallel. However, the quiescent currents required by these rather complex structures are also large.

The topology of the LDO proposed in this paper is similar to the ones described above, but the local feedback is implemented by a novel circuit, which ensures both a fast response to load transients and the LDO stability for practically any load capacitance. This circuit is combined with an EA with enhanced slew-rate to obtain a compact LDO, suitable for low quiescent current operation and a small die footprint. These are presented in Section II, along with an intuitive small-signal analysis of the resulting LDO, which yields the key sizing equations.

Section III presents a design example: the proposed LDO was integrated in a 130 nm standard CMOS technology; simulation and measurement results prove that the design can handle capacitive loads up to tens of $\mu$F, exhibits small output voltage overshoots and undershoots when $I_L$ varies between 1 $\mu$A and 100 mA in 1 $\mu$s, while its quiescent current is just 6 $\mu$A. This section also comprises a comprehensive comparison with state-of-the-art. Conclusions are drawn in the last Section.

\section{II. PROPOSED LDO: TOPOLOGY, IMPLEMENTATION, AND ANALYSIS}

\subsection{A. PROPOSED TOPOLOGY AND MAIN IDEA FOR CIRCUIT IMPLEMENTATION}

Fig. 2(a). depicts the block diagram of the LDO proposed here. The topology is similar to the one shown in Fig. 1(a) but highlights the fact that the additional local feedback created between the LDO output and its pass transistor is used to ensure both a fast response to load transients and an effective frequency compensation. A circuit that achieves these goals is presented in Fig. 2(b): capacitors C1 and C2 are connected between the LDO output and the sources of transistors MyN and MyP, respectively. In steady-state operation, the potentials at these sources are set by the voltage drops across resistors Rn and Rp, caused by a current derived from the bias current Idc by the cascaded current mirrors M5-M6, MxN-MyN-Rn and M7-M8, MxN-MyN-Rp. Let us assume that, starting from a stable operating point, the output voltage decreases fast due to a sudden increase in the load current. The main feedback loop, that includes the EA, needs time to react but the output voltage variation is conveyed immediately by capacitor C1 to the source of MyN. Thus, the potential of node N is pushed down fast, and it can go below the GND rail. Therefore, the gate-source voltage of
MyN increases quickly, causing a dramatic increase of its drain current. Similarly, as the output voltage decreases, the node P is pulled down, but this results in the source-gate voltage of transistor MyP being shrunk. Therefore, the current injected into the node GATE by MyP decreases, while the current sunk from that node by transistor MyN increases. The combined effect is to pull down the gate of the PMOS pass transistor, so that it sources more current into the load, which in turn arrests the decrease of the output voltage. Conversely, when the output voltage increases due to a sudden decrease of the load current, the circuit shown in Fig. 2(b) injects more current into the GATE. As the gate voltage of Mpass increases its source-gate voltage shrinks, resulting in a drastic decrease of the current it sources into the load. This prevents the output voltage from increasing any further.

The cascodes M6 and M8 help increase the output impedance of the fast transient and frequency compensation circuit so that it does not significantly impact the equivalent small-signal resistance between nodes GATE and GND, hence neither the gain of the main voltage-control feedback loop.

The voltages at nodes P and N go outside the supply rails, but the circuit can be sized so that this does not result in SOA violations. This is demonstrated in Fig. 3, where the voltages at nodes P and N go above, respectively below the corresponding supply line but only by 81mV and 168mV.

Fig. 3 provides a direct comparison of the transient response to a load current step between an ordinary LDO before and after inserting the fast transient circuit shown in Fig. 2(b). When using the additional circuit, a larger current is injected and sunk into and from the gate of the pass transistor, which leads to a faster reaction of the LDO to variations of the output voltage. This behaviour can be seen in Fig. 3, and is consistent with (1) and (2): as $\Delta t$ is reduced by adding in the fast transient circuit, the output voltage overshoot and undershoot are also reduced. The faster settling time is also worth noticing.

To conclude, the circuit presented in Fig. 2(b) reacts very fast to variations of the LDO output voltage, driving the gate
of \( M_{\text{pass}} \) so that the Vout variations are arrested quickly, well before the main feedback loop can react. This way, both the output voltage undershoot and overshoot are diminished.

In steady-state operation, the circuit shown in Fig. 2(b) implements a parallel-parallel inner feedback loop that helps reduce the impedance at the LDO output. In turn, this reduces the impact the pole associated with the output node, which also depends on the load capacitance, \( C_L \), has on the LDO stability. Section II.C explains in detail the impact of this circuit on the loop frequency characteristics.

### B. AN EFFICIENT CIRCUIT IMPLEMENTATION

1) ERROR AMPLIFIER WITH HIGH SLEW RATE

The operational transconductance amplifier (OTA) shown in Fig. 4 employs a recycled folded cascode topology [8] and adaptive biasing to achieve large values for the low-frequency gain and slew rate (SR) [4].

The input stage is formed by two pairs of matched cross-coupled transistors, \( M_{1a}-M_{1b} \) and \( M_{2a}-M_{2b} \), and two level-shifters, \( M_{13a} \) and \( M_{13b} \), and operates in class AB [9]. Assuming that transistors \( M_{1a}, M_{1b}, M_{2a}, M_{2b}, M_{13a}, M_{13b} \) work in the saturation region, the output current is a 4\(^{\text{th}}\) order function of the differential input voltage, \( V_{\text{id}} = V_{\text{InP}} - V_{\text{InM}} \) [4]:

\[
I_{\text{out}} = \pm \frac{\beta_{4a,4b}}{2} \times \left\{ \frac{2I_{cm}}{\beta_{3a,3b}} + \frac{R}{2} \left( \frac{2(I_{13b})}{\beta_{13b}} + |V_{id}| \right) \right\}^2
\]

where \( \beta = \mu C_{ox} \left( \frac{W}{L} \right) \) is the transconductance factor and \( I_{cm} = (I_{2a} + I_{2b})/2 \).

Thus, this OTA is well suited to implement the error amplifier depicted in Fig. 2(a): the current that charges or discharges the gate capacitance of the pass transistor can easily reach values well above the quiescent current - effectively boosting the equivalent slew-rate of this circuit.

However, a complicated and somewhat unwieldy LDO, that requires considerable quiescent current and die area, results if one simply inserts the schematics presented in Fig. 2(b) and Fig. 4 into the LDO block diagram shown in Fig. 2(a).

2) COMBINED EA AND FAST TRANSIENT CIRCUITRY

Fig. 5 presents a very compact circuit implementation of the proposed LDO topology: the idea is to reduce the number of circuit elements by embedding the Fast transient & Frequency compensation (Ft&Fc) circuit shown in Fig. 2(b) into the error amplifier shown in Fig. 4.

By analysing the three schematics mentioned above, one notices that in Fig. 5 the Ft&Fc circuit is implemented by adding only passive elements – \( C_1, C_2, R_p \) and \( R_{n1}, R_{n2} \), drawn in blue in Fig. 5 - to the OTA shown in Fig. 4. All MOS transistors within the Ft&Fc circuit shown in Fig. 2(b) – drawn in red in Fig. 5 - are obtained by assigning dual function to several transistors within the initial OTA. This way, the Ft&Fc circuit does not require additional quiescent current, and the die area increase is minimized.

### C. SMALL SIGNAL ANALYSIS

Fig. 6(a) presents a simplified small-signal representation of the circuit shown in Fig. 5, in unity-gain configuration (FB node connected directly to OUT node). Here is a brief description:

- \( G_{\text{mEA}} \) is the transconductance of the EA OTA, with the noninverting input connected directly to the LDO output. Its internal pole, due to the pair of nodes denoted A and B in Fig. 5, has to be considered; let its angular frequency be \( \omega_{pEA} \);
\( \mathbf{G_{m\text{PASS}}} \) is the transconductance of the pass transistor, \( \text{Mpass} \);

- \( \mathbf{G_{mFB1}} \) is the transconductance of the section of the local feedback implemented by the \( \text{Ft}&\text{Fc} \) circuit that is connected to the LDO output through \( \mathbf{C1} \). It consists of \( \text{M4yNb-M6} \) and \( \mathbf{Rn2} \). Its input impedance is represented by \( \frac{1}{\mathbf{G_{mFB1}}} \parallel \mathbf{Rn} \).

- \( \mathbf{G_{mFB2}} \) is the transconductance of the local feedback implemented by the \( \text{Ft}&\text{Fc} \) circuit that is connected to the LDO output through \( \mathbf{C2} \). It consists of \( \text{M10yP-M8} \) and \( \mathbf{Rp} \). Its input impedance is represented by \( \frac{1}{\mathbf{G_{mFB2}}} \parallel \mathbf{Rp} \).

- \( \mathbf{R_G} \parallel \mathbf{C_G} \) represents the small-signal impedance between the nodes denoted GATE and GND in Fig. 5, while \( \mathbf{R_L} \parallel \mathbf{C_L} \) is the small-signal impedance between nodes OUT and GND.

Brute-force analysis of the small-signal equivalent of the circuit shown in Fig. 6(a) yields the loop gain expression:
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implemented by the Ft&Fc circuit symmetrical, that is:

the unity-gain frequency of each loop-gain, rather than the usual stability criteria, the entire circuit is stable.

stability is easier to analyse.

an equivalent circuit with only one feedback loop, whose loop is replaced by its closed loop equivalent, yielded by the
to reduce it to a two-real-poles-and-one-zero expression similar to Ahuja’s [10] (also simplified)
and relatively small C-inner (R-l C-inner < R-C C-l)

This highlights the two distinct feedback loops within the LDO: the main one, that comprises the EA, and the inner one, formed by the Ft&Fc circuit. The latter closes parallel-parallel feedback around the pass transistor; thus, the ensemble can be represented by a single block, as shown in
Fig. 6(c). Its transfer function, corresponding to the parallel-parallel feedback topology, is the transimpedance Z-inner, whose expression results simply from the classical feedback theory:

where LG-inner is the loop gain of the inner loop and a-inner and f-inner are the open loop gain and the feedback transmittance of the inner loop, respectively:

As LG-inner = a-inner f-inner, one obtains:

The loop gain of the entire LDO results by analysing Fig. 6(c):

The small-signal representation of the circuit shown in Fig. 5 can be reduced to the schematic presented in Fig. 6(b).

Instead, we developed a version of the approximate graphical analysis method introduced in [11] and [12], and
developed in [13]. Its main points are:

– a circuit with multiple feedback loops can be simplified iteratively, starting from the inner loop and moving outwards.

At each step, the section enclosed by the inner-most feedback loop is replaced by its closed loop equivalent, yielded by the
classical feedback theory. In this way, one eventually obtains an equivalent circuit with only one feedback loop, whose stability is easier to analyse.

- if the final equivalent circuit, as well as the sections obtained at each step of topological transformation, meet the usual stability criteria, the entire circuit is stable.

- focus the analysis on the narrow frequency range around the unity-gain frequency of each loop-gain, rather than the loop-gain expressions over the entire frequency range.

By making the two sections of the local feedback implemented by the Ft&Fc circuit symmetrical, that is:

\[ G_{mFB1} = G_{mFB2} = G_{mFB}; \quad C_1 = C_2 = C; \quad R_n = R_p = R \] (6)

\[ T = G_{mEA} R_G G_{mPASS} R_L * \]

\[ \frac{1}{1 + sR_G C_G} \]

\[ \frac{1}{1 + sR_G C_l} \]

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If $LG_{INNER} \ll 1$, then $LG_{LDO} = G_{mEA}g_{INNER}$

$$LG_{LDO} = G_{mEA} \frac{1}{f_{INNER}}$$ (12)

If $LG_{INNER} \gg 1$, then $LG_{LDO} = G_{mEA}$

$$LG_{LDO} = G_{mEA}$$ (13)

For the LDO to be stable, the inner feedback circuit shown in Fig. 6(c) must be stable, as well. Therefore, one needs to analyse both $LG_{INNER}$ and $LG_{LDO}$. For this, we will use an intuitive method based on approximate representations of the module frequency characteristics of the two loop gains, considering all relevant combinations of load current (which determines $G_{mPASS}$ and $R_L$) and load capacitance values.

To ensure a proper phase margin for both feedback loops, let us set two general requirements:

i. the magnitude characteristic of $LG_{INNER}$ should cross the 0 dB horizontal with a −20 dB/dec slope;

ii. The unity-gain angular frequency, $\omega_u$, of the $|LG_{LDO}|$ frequency characteristic should occur more than a decade below $\omega_{peEA}$. In other words, this internal pole of the EA ought to be sized so that it is always beyond $\omega_u$.

1) ANALYSIS OF THE INNER LOOP GAIN, $LG_{INNER}$

Fig. 7(a) presents the magnitude frequency characteristics of the two loop gains derived by using TABLE 2-(13), when $I_L$ is close to the maximum value, $I_{L_{MAX}}$, while $C_L$ is relatively small, so that $R_L C_L < R_G C_G$.

The frequency characteristics of $LG_{INNER}$ are determined by a zero placed in the origin, two main poles associated with the GATE and OUT nodes, $\omega_G = \frac{1}{R_{DG} C_G} < \omega_L = \frac{1}{R_{LC} C_L}$ in this case, and a third pole introduced by the $Ft&Fc$ circuit – as described by (10). It crosses the 0 dB horizontal with a −20 dB/dec slope if its unity gain angular frequency, $\omega_{u2}$, is no larger than the angular frequency of the third pole:

$$\omega_{u2} \leq \omega_3 \quad (14)$$

This can be ensured by setting the following constraint on the maximum value of the inner loop gain:

$$1 < |LG_{INNER}|_{\text{max}} \leq \frac{\omega_3}{\omega_L} \quad (15)$$

As the load current decreases, the equivalent small-signal resistance at the OUT node, $R_L$, increases, while $G_{mPASS}$ decreases. Also, at very light load, the gate of the pass transistor rises, which pushes the Pmos cascoded mirror of the EA into the linear region. As a result, the total gain of the LDO decreases. This scenario is illustrated in Fig. 7(b): the pole associated with the OUT node moves to a lower angular frequency, $\omega_{u1}$; concurrently, the level of the $LG_{INNER}$ plateau decreases, pulling the unity-gain frequency lower, down to $\omega_{u2}$, while the first zero-crossing occurs at a higher angular frequency, $\omega_{u1}$. As long as $|LG_{INNER}|_{\text{max}} > 0$ dB and $\omega_G$ remains the dominant pole, (15) yields:

$$\frac{C}{C_G} \left( G_{mFB} G_{mPASS} R_L \left| \frac{1}{G_{mFB}} \right| \right) \leq \frac{R_L C_L}{R \left| \frac{1}{G_{mFB}} \right| C} \quad (16)$$

For $R \ll \frac{1}{G_{mFB}}$ one can approximate $R \left| \frac{1}{G_{mFB}} \right| \approx R$. Therefore, (16) can be rewritten as follows:

$$\frac{C_G}{G_{mFB} G_{mPASS} R_L} \leq RC \leq \frac{C_G C_L}{G_{mFB} G_{mPASS}} \quad (17)$$

2) ANALYSIS OF MAIN LOOP GAIN, $LG_{LDO}$

Let us now analyse the LDO loop gain for the case shown in Fig. 7(a). Equations (12) and (13) indicate that:

- for $\omega < \omega_{u1}$ and $\omega > \omega_{u2}$ the LDO loop gain is approximated by the product $G_{mEA}g_{INNER}$;
- for $\omega_{u1} < \omega < \omega_{u2}$ the $LG_{LDO}$ follows $G_{mEA} \frac{1}{f_{INNER}}$.

Therefore, the $LG_{LDO}$ dominant and secondary poles are set by the zero-crossing points of the $|LG_{INNER}|$ characteristic:

$$\omega_{dp} = \omega_{u1} \quad ; \quad \omega_{sp} = \omega_{u2} \quad (18)$$

In this case, we can provide for the $LG_{LDO}$ magnitude frequency characteristic to cross the 0 dB horizontal with a −20 dB/dec by setting the following condition:

$$\left| G_{mEA} \frac{1}{f_{INNER}} \right| = A_h = \frac{G_{mEA}}{G_{mFB}} < 1 \quad (19)$$

Furthermore, the unity gain frequency of the LDO loop gain, $\omega_u$, can be found at the intersection of the $G_{mEA} \frac{1}{f_{INNER}}$ frequency characteristic with the 0 dB horizontal:

$$\omega_u = \frac{G_{mEA}}{2 R C G_{mFB}} = \frac{1}{2} A_h \frac{1}{R C} \quad (20)$$

The $\omega_u$ value is close to $\omega_{pEA}$ but in this case the LDO stability is ensured by condition (19).

For the scenario depicted in Fig. 7(b), the dominant pole of $LG_{LDO}$ moves up in frequency, while its secondary pole moves down, to $\omega_{u1}^* = \omega_{u1}$ and $\omega_{u2}^* = \omega_{u2}$, respectively. Although the low-frequency gain decreases, the 0 dB-crossing occurs after the secondary pole, $\omega_{sp} < \omega_{u2}$. However, the LDO remains stable because the unity-gain frequency is far lower than in the previous case, shown in Fig. 7(a), while the parasitic pole of the $G_{mEA}$, $\omega_{pEA}$, does not move. The LDO phase margin depends mainly on the distance between $\omega_u^*$ and $\omega_{sp}^*$, which becomes an important design constraint.

Fig. 8 illustrates four real-life cases for the $LG_{INNER}$ and $LG_{LDO}$: the load current is kept constant at a normal operating level, $I_L_{MIN} < I_L < I_L_{MAX}$, while the load capacitance takes four values $C_{La} < C_{Lb} < C_{Lc} < C_{Ld}$, from near-zero to very large values, in the $\mu$F to tens of $\mu$F range.

Fig. 8(a) shows the case of a load capacitance value, $C_{La}$, relatively small, such that $R_L C_L < R_G C_G$. This is similar to the case shown in Fig. 7(b), except for the higher level of the $LG_{INNER}$ plateau. As the value of $C_L$ increases, the secondary pole of the $LG_{INNER}$ characteristic, $\omega_{u2} = \frac{1}{R_{LC} C_L}$, moves towards lower frequencies, dragging with it the zero-crossing point of that characteristic, $\omega_{dp}^*$; this ensures the stability of the inner loop. According to (18), this forces the secondary pole of $LG_{LDO}$ to move to a lower
frequency, while its main pole does not change position. Therefore, the $|L_{G_{LDO}}|$ characteristic crosses the 0 dB axis after the secondary pole, $\omega_{p2} < \omega_{u2}$. As the distance between the main $|L_{G_{LDO}}|$ poles decreases, so does the LDO phase margin. This situation is similar to, but slightly better than, the one shown in Fig. 7(b), because here the dominant pole does not move. Therefore, the LDO stability is ensured by the same factors: the unity-gain angular frequency decreases, while the $G_{mEA}$ parasitic pole does not move, thus $\omega_{u2} \ll \omega_{pEA}$. The value of the LDO phase margin is set by the distance between these poles, i.e. the ratios $\omega_{p2}/\omega_{u2}$ and $\omega_{pEA}/\omega_{p2}$.

As the load capacitance increases further, the $L_{G_{INNER}}$ pole associated with the OUT node moves to even lower frequencies; for the load value $C_{Lb}$, it reaches the position of the pole associated with the GATE node, $\omega_G = \omega_{Lb}$. The frequency characteristics for this case are shown in Fig. 8(b). With respect to LDO stability, the situation is worse than the one presented in Fig. 8(a): as the second pole of $|L_{G_{LDO}}|$ moves down in frequency, the distance between it and the dominant pole, which remains fixed, decreases. In turn, this results in a larger distance between the second pole and the zero-crossing point, $\omega_{u2}$, thus resulting in a smaller phase margin.

However, the phase margin remains positive as long as $\omega_{p2}/\omega_{u2} < \omega_{pEA}/\omega_{p2}$ and its actual value can be adjusted through appropriate sizing.

By further increasing the load capacitance to $C_{Lc}$, one obtains the frequency characteristics depicted in Fig. 8(c): for the $|L_{G_{INNER}}|$ characteristic, the pole associated with the OUT node becomes the dominant pole, exceeding the pole associated with the GATE node, while its second zero-crossing frequency decreases further, $\omega_{u2} < \omega_{u2}$, albeit at a slower pace than in the previous case. Therefore, the secondary pole of the $|L_{G_{LDO}}|$ characteristic moves to lower frequencies, while the other two poles maintain their positions. In this case, by reiterating (14), the constraint set on the maximum value of the inner loop gain becomes:

$$1 < |L_{G_{INNER}}|_{max} \leq \frac{\omega_3}{\omega_G}$$

which leads to:

$$\frac{C}{C_L} \left( \frac{G_{mFB}G_{mPASS}R_G(R\frac{1}{G_{mFB}})}{G_{mFB}G_{mPASS}R_G} \right) \leq \frac{R_GC_G}{R\frac{1}{G_{mFB}}}$$

$$\frac{C_L}{G_{mFB}G_{mPASS}R_G} \leq RC \leq \sqrt{\frac{C_GC_L}{G_{mFB}G_{mPASS}}} \quad (23)$$

The situation is similar to the case illustrated in Fig. 8(b), with two differences: the plateau of the $|L_{G_{INNER}}|$ characteristic is a function of $C_L$ now and gets smaller than in the previous cases, and the distances between the $|L_{G_{LDO}}|$ zero-crossing point and the second and third poles are slightly larger. It follows that the LDO phase margin may be a bit smaller but remains positive.

The level of the $|L_{G_{INNER}}|$ plateau decreases as the load capacitance increases further, eventually reaching values below 0 dB, as shown in Fig. 8(d). In this case, the main poles of the $|L_{G_{LDO}}|$ characteristic are mainly determined by the first two poles of the $|L_{G_{INNER}}|$ characteristic, $\omega_{u1} = \frac{1}{R_LCL_L} < \omega_G = \frac{1}{R_GC_G}$. Therefore, as $C_L$ increases, the dominant pole moves to lower frequencies, while the second pole maintains its position. The zero-crossing frequency of $|L_{G_{LDO}}|$ decreases, but it gets closer to the second pole, $\omega_{p2}$.

Therefore, the LDO phase margin increases.

To conclude, for all cases analysed here the LDO phase margin remains positive; the circuit can be sized in order to ensure that the LDO phase margin remains above a minimum allowed value. The circuit sizing should be optimized for the case illustrated in Fig. 8(c), by taking into account (17) and (23), equations that can be rewritten as follows:

$$\max \left\{ \frac{C_L}{G_{mFB}G_{mPASS}R_G}, \frac{C_G}{G_{mFB}G_{mPASS}R_L} \right\} \leq RC$$

$$\leq \sqrt{\frac{C_GC_L}{G_{mFB}G_{mPASS}}} \quad (24)$$

This makes the approach to the analysis of multiple-loop LDOs more effective and useful to the circuit designer than [10] and [14].

III. DESIGN EXAMPLE

A. LDO DESIGN REQUIREMENTS AND SIZING STRATEGY

The LDO introduced in the previous Section, with the schematic shown in Fig. 5, was used to implement a regulator for an SoC integrated in a standard 130 nm CMOS process. Multiple instances of this LDO are used for various digital sections within the SoC, so it has to cater for a wide range of loads. This led to the following set of design requirements:

- $Vout = 1$ V, when supply voltage varies between 1.2 V and 1.5 V and $I_L$ varies between 1 $\mu$A and 100 mA;
- maximum $V_{drop} = 100$ mV; max quiescent current $I_{Q} = 7$ $\mu$A;
- the LDO stability should be ensured for $I_L$ varying from 1 $\mu$A to 100 mA and $C_L$ ranging from 0 to at least 1 $\mu$F, and irrespective of the ESR of $C_L$.
- output voltage undershoot/overshoot when $I_L$ steps up from 1 $\mu$A to 100 mA in 1 $\mu$s, then back: no more than +/− 20% of nominal value, so that the difference $Vout_{max} - Vout_{min}$ remains smaller than 400mVppk.
- PSR of at least 50 dB at 10 kHz for mid-range load currents, and better than 30 dB at full load, over the entire $C_L$ range.
- design and integrate in a standard 130 nm CMOS process.
- due to the die size limitations, the total value of on-chip capacitors ($C_1, C_2$) should be maintained to less than 100 pF.

As such, we propose the following sizing strategy for the frequency compensation circuit to meet these demands for the LDO stability.
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**FIGURE 8.** Frequency characteristics of the $|L_{GDDO}|$ and $|L_{INNER}|$ loop gains when $I_L$ is kept at a constant, small-to-large value, and the $C_L$ is increased in four steps: (a) initial small value, for which $R_L C_L < R_G C_G$; (b) medium values, for which $R_L C_L = R_G C_G$; (c) large values, for which $R_L C_L > R_G C_G$ and (d) very large values. In the (b)-(d) cases the starting point shown in (a) is represented by dotted lines, while the main changes are highlighted in blue.

**FIGURE 9.** LDO Phase Margin over all values of $I_L$ and $C_L$ without the F&Bc circuit.

Step 1: Size the pass transistor according to the dropout requirement and estimate the total gate parasitic capacitance, $C_G$, at node GATE of the pass transistor.

Step 2: Size the remaining transistors in order to obtain the desired open loop DC gain given by (12), considering precision and PSR. This should follow the common design strategy (distribute the quiescent current for each circuit branch, bias the transistors in saturation etc.). Therefore, this step is not expanded in further details.

Step 3: By running parametric sims, find the $I_L$ and $C_L$ values for which the LDO without the frequency compensation circuit has a phase margin smaller than required. In our case, this resulted in the values shown with dark red in Fig. 9. Notice that no $C_L$ value can ensure the LDO stability over the entire range of load currents.

Step 4: From (24) find the RC value for which the frequency compensation covers the values of $I_L$ & $C_L$ found at Step 3 – the area delimited by the upper ($\sqrt{\frac{C_G C_L}{G_{mFB} G_{mPASS}}}$) and lower ($\max\left\{\frac{C_L}{G_{mFB} G_{mPASS} R_G}, \frac{C_G}{G_{mFB} G_{mPASS} R_L}\right\}$) boundaries. The 3D representation of (24) is shown in Fig. 10, followed by a top-view of the same, Fig. 11.

Step 5: For the RC value obtained at the previous step, choose the values for R & C for which the dynamic response
of the Ft&Fc circuit is optimal (exhibits the highest output current). Testing the fast transient circuit part connected to the NMOS transistor resulted in a non-intuitive optimal value for R & C around 500 kΩ & 100 pF, as shown in Fig. 12. For higher values for R the circuit exhibits less current. Given the RC value obtained at the previous step, area constraints and voltage drop on R, a good tradeoff was to choose R = 10 kΩ and C = 80 pF. The capacitance value will be split between C1 and C2.

Step 6: Check the LDO Phase Margin for the values of R & C obtained at Step 5 and ensure that, for all combinations of I_L & C_L, the Phase Margin is greater than the minimum allowed value.

B. SIMULATION RESULTS

All results shown in this section were obtained by running simulations on netlists that included post-layout-extracted parasitics. Fig. 13 shows the frequency characteristics of the LDO loop gain for C_L = 1 pF and two load currents: I_L = 1 µA, then 100 mA. For I_L = 100 mA the simulated magnitude characteristics are similar to those approximated by Fig. 7(a): the first pole, \( \omega_{dp} \), is placed around the first zero crossing of the \(|L_{INNER}|\), while the second pole, \( \omega_{sp} \), is placed at the second zero crossing of \(|L_{INNER}|\), which occurs after the unity-gain frequency of the \(|L_{LDO}|\) – in this case 1.54 MHz. This resulted in a comfortable phase margin value, 89.71°.

As indicated by Fig. 7(b), for I_L = 1 µA the \(|L_{LDO}|\) low-frequency value is significantly smaller than for I_L = 100 mA; also, the first pole of \(|L_{LDO}|\) has moved up in frequency, while the second pole has moved to a lower frequency. Therefore, the \(L_{LDO} \) magnitude characteristic started decreasing with a \(-40 \text{ dB/dec}\) slope before reaching its unity-gain frequency, of 594.1 kHz. This resulted in a substantially smaller phase margin value than the previous case, 23.28°, but large enough to ensure the LDO stability.
Note that in both cases the $|LG_{LDO}|$ low-frequency values are relatively large, 82.85 dB for $I_L = 100$ mA and 69.63 dB for $I_L = 1$ µA. This ensures good values for the LDO line regulation and load regulation.

Fig. 14 shows the $|LG_{LDO}|$ frequency characteristics at light load ($I_L = 1$ µA), when the load capacitor takes values between 1 pF and 1 µF. Fig. 15 presents a similar set of simulations, but for the maximum load current, $I_L = 100$ mA, and a smaller range of $C_L$ values: 1 pF to 100 nF. Fig. 16 depicts the frequency characteristic of the LDO for the same maximum load current, but in this case the output capacitor takes values between 1 µF and 300 µF.

The simulation setup used to obtain the results shown in Fig. 14 corresponds to the cases presented in Fig. 8. As long as the $C_L$ values are small enough to satisfy condition $R_L \times C_L < R_G \times C_G$, the dominant pole is given by the first zero-crossing of $|LG_{INNER}|$ and only the secondary pole moves down in frequency as $C_L$ increases – this corresponds to the cases shown in Fig. 8(a) and (b). Therefore, the LDO phase margin decreases.

For larger $C_L$ values, for which $R_L \times C_L > R_G \times C_G$, the level of the inner loop gain plateau, $|LG_{INNER}|_{max}$, starts decreasing; the secondary pole continues to move down in frequency as $C_L$ increases, but by smaller amounts - see Fig. 8(c). As a result, the LDO phase margin degradation continues at a smaller pace, eventually reaching a minimum value, just over 8°, for $C_L = 281$ pF. For even larger $C_L$ values, $|LG_{INNER}|_{max}$ starts decreasing such as it reaches below 0 dB. In this case, the $|LG_{LDO}|$ dominant pole starts moving to lower frequencies, while the secondary pole remains practically at the same frequency. This situation corresponds to the one illustrated by Fig. 8(d): as the value of $|LG_{INNER}|_{max}$ gets smaller than unity, the $|LG_{LDO}|$ dominant pole is given by the OUT node with the angular frequency inversely proportional to $C_L$, while the secondary pole is determined by the GATE node. Therefore, the LDO phase and gain margin start increasing, and continue to do so as the $C_L$ value increases further. Note that for $C_L$ values larger than 100 nF, the phase margin stays above 60 degrees. This proves that at light loads the LDO remains stable for practically any value of the load capacitor.

For small $C_L$ values, that is, as long as $R_L \times C_L < R_G \times C_G$, the simulation setup used to obtain the results shown in Fig. 15 corresponds to the case illustrated in Fig. 7(a): the $|LG_{LDO}|$ characteristic crosses the 0 dB axis with a $-20$ dB/dec slope. As the value of $C_L$ increases, the secondary pole of the $|LG_{LDO}|$ characteristic moves towards lower frequencies, so that it occurs around the zero-crossing point of that characteristic. As $C_L$ increases furthermore, case shown in Fig. 16, the secondary pole of $|LG_{LDO}|$ moves down even more in frequency, so that it occurs above the 0 dB; this corresponds to the case shown in Fig. 8(a). From there on, the situation evolves similarly to the light-load case shown in Fig. 14: as the distance between the two $|LG_{LDO}|$ main poles decreases, so does the LDO phase margin, reaching a value slightly above 10° for $C_L = 3.7$ µF. For larger $C_L$ values the phase margin starts increasing. The pole associated with the OUT node moves down in frequency and becomes the dominant pole of the $|LG_{LDO}|$ characteristic.

Fig. 18 shows the LDO Phase Margin for all combinations of $I_L$ & $C_L$ values, with $I_L$ taking values between 0.01 µA and 100 mA and $C_L$ between 1 pF and 1 µF. The effectiveness of the proposed frequency compensation is demonstrated.

FIGURE 14. Loop gain frequency characteristics of the proposed LDO for light load ($I_L = 1$ µA) and $C_L$ taking values from 1 pF to 1 µF. At low $C_L$ the pole placed around the first zero crossing of the $LG_{INNER}$ is the dominant pole of the LDO; as $C_L$ increases, the pole associated with the output node moves down in frequency and becomes the dominant pole of the LDO.

FIGURE 15. Loop gain frequency characteristics of the proposed LDO for heavy load ($I_L = 100$ mA) and $C_L$ taking values from 1 pF to 100 nF. The pole associated with the output node (in this case, the second pole) goes down in frequency as $C_L$ increases.

FIGURE 16. Loop gain frequency characteristics of the proposed LDO for heavy load ($I_L = 100$ mA) and $C_L$ taking values from 1 µF to 300 µF. The pole associated with the output node becomes the dominant pole of the LDO at a $C_L$ value far larger than in the light-load case.
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FIGURE 17. The phase margin and gain margin for the proposed LDO when a) \( I_L = 1 \mu A \), \( C_L \) takes values between 1 pF to 1 \( \mu F \); b), and c). \( I_L = 100 \text{ mA} \), \( C_L \) takes values between 1 pF to 100 nF, then between 1 \( \mu F \) to 300 \( \mu F \).

FIGURE 18. LDO Phase Margin over all values of \( I_L \) and \( C_L \) with the proposed Ft&Fc circuit.

by comparing these results with their counterparts depicted in Fig. 9, obtained for a similar core LDO but without the Ft&Fc circuit. One notices that the proposed frequency compensation ensures the LDO stability over the entire range of \( I_L \) and \( C_L \) values, with double digit Phase Margin values for most cases, except for the small area highlighted at the top of Fig. 18.

There, the Phase Margin reaches its minimum value of 7 degrees, but exhaustive transient simulations confirmed that the LDO remains stable. It should be noted that the simulation results presented in both Fig. 9 and Fig. 18 were obtained for a particularly tough case with respect to the LDO stability: no track resistance and capacitors with ESR = 0 and ESL = 0.

FIGURE 19. A 3D representation of the LDO Phase Margin over \( I_L \) and \( C_L \) with and without Ft&Fc circuit.

Fig.19 shows a 3D representation of the Phase Margin for the proposed LDO, with and without the Ft&Fc circuit, over all values of \( I_L \) and \( C_L \). The gray area highlights the values of \( I_L \) & \( C_L \) for which the Phase Margin values are smaller than zero. Notice that with the chosen values for R and C, the LDO with fast transient does not contain regions of instability for any combination of \( I_L \) and \( C_L \).

Looking closely at Fig. 17(a) and (b), one notices that there are three worst cases regarding stability, where phase margin and gain margin take values below 10° and 10 dB,
respectively. In Fig. 17(a) the minimum PM value is 8.2° for $C_L = 281 \text{ pF}$ and the smallest GM is 8.7 dB for $C_L = 91 \text{ pF}$. In Fig. 17(b) the worst case is for GM. The smallest value is found at $C_L = 19.35 \text{ nF}$ and is 6.45 dB. The following figures, Fig. 20 and Fig. 21, illustrate the transient response of the LDO to a load current step for the worst cases described above. At $t = 2 \text{ ms}$ the load current jumps from 1 $\mu \text{A}$ to 100 mA in 1 $\mu \text{s}$ and at 2.04 ms back to 1 $\mu \text{A}$. The small ringing at the output voltage confirms that the LDO is stable even for PM and GM values smaller than 10° and 10 dB, respectively.

The LDO output noise of the LDO for $I_L = 1 \text{ mA}$ and $C_L = 0 \text{ pF}$ is shown in Fig. 22. Fig. 23 shows the LDO Power Supply Rejection (PSR) for the same load current and $C_L$ values between 1 pF and 1 $\mu \text{F}$.

C. MEASUREMENTS RESULTS

Fig. 24 shows the die photographs of the proposed LDO integrated in a 130 nm CMOS test chip, with a zoom-in that details the LDO floorplan. Most of its 0.018 mm$^2$ active area is occupied by the two capacitors within the $F_t$&$F_c$ circuit, $C_1$ and $C_2$. Therefore, the LDO area can be reduced substantially if high-density metal capacitors are available.

The error amplifier is located separately from the pass transistor, so that it is not affected by the thermal gradients caused by the power MOS transistor.

The LDO was configured in a unity feedback structure as shown in Fig. 5, that is the worst case with respect to stability.

Figures 25 - 27 show the measured LDO response to load current jumps between 1 $\mu \text{A}$ and 100 mA in 1 $\mu \text{s}$ for three $C_L$ values: the response depicted in Fig. 25 was obtained for $C_L = 0$; the one shown in Fig. 26 was obtained for $C_L = 91 \text{ pF}$, the value for which the LDO Gain Margin reached its minimum in Fig. 17(a); Fig. 27 depicts the load transient response for the maximum $C_L$ value, 1 $\mu \text{F}$. The test setup used for these measurements was similar to the one described in [13].

Fig. 28 shows the PSR frequency characteristic of the proposed LDO for the maximum load current, $I_L = 100 \text{ mA}$, and three die temperatures: −40°C, 25°C and 150°C. These
measurements indicate that the LDO meets the PSR design requirement set in Section III.A. Fig. 29 and Fig. 30 present the LDO response to a 300mV line jump with the rise/fall time of 1μs, measured for the same load current, 100 μA, and the extreme values for the load capacitor, respectively $C_L = 0$ and $C_L = 1 \mu F$. The output voltage overshoot and undershoot are quite small (20mV and 21mV) even for $C_L = 0$, and are further reduced when a large external capacitor is used. The measurement shown in Fig.30 proves that the LDO is stable for the loading conditions ($C_L = 1 \mu F$, $I_L = 100 \mu A$) for which simulation results yielded a small Phase Margin value of less than 10 degrees. The settling time is longer for $C_L = 1 \mu F$ than for $C_L = 0$, as expected considering the different Phase Margin values obtained for the two load capacitor values.

The measurement results presented here validate the design and prove that the proposed LDO meets the requirements set out in Section III.A. The circuit is able to operate without a placed decoupling capacitor, as well as with large, external load capacitors. For practical reasons, the maximum load capacitor employed here was 1 μF but the LDO can handle even larger loads, as indicated by Fig. 17(c).

D. COMPARISON WITH STATE-OF-THE-ART

For a comprehensive comparison of the LDO presented in this work against state-of-the-art, let us first employ two of the most popular Figures-of-Merit (FOM) proposed in the literature:

- FOM1 proposed in [15] is effective for comparing LDOs with widely different values for the quiescent current, $I_q$, load capacitance $C_L$ and load current:

$$FOM_1 = \frac{\Delta V_{out, pkp} \cdot C_L \cdot I_q}{I_L^2}$$

where $\Delta V_{out, pkp}$ is the maximum output voltage variation (undershoot + overshoot) caused by the largest current load step the LDO can handle, range, $\Delta I_L = I_{L, \text{max}} - I_{L, \text{min}}$. In general, the $C_L$ values used to calculate FOM1 were the ones for which the largest $\Delta V_{out, pkp}$ was obtained. If that value was zero, $C_L = 1 \text{pF}$ was used instead.

- FOM2 introduced in [16] is suitable for comparing capacitorless LDOs. It takes into account the rise/fall time of the load current step, which has a particularly large impact on the step response of LDOs that operate with no or only a small decoupling capacitor at their output. Also, it includes a process-dependent factor – $FO4_{\text{Delay}}$, the propagation delay of a standard CMOS inverter with fan-out of four – to obtain
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Table 1. Performance comparison of LDOs designed to operate with large load capacitors, up to tens of µF.

| PARAM                  | [7]†† | [17]† | [18]† | [19]†† | [20]†† | [6]†† | [13]†† | [21]†† | This work†† |
|------------------------|-------|-------|-------|--------|--------|-------|--------|--------|------------|
| Year                   | 2004  | 2013  | 2014  | 2016   | 2018   | 2019  | 2020   | 2021   | 2021       |
| CMOS [µm]              | 0.5   | 0.065 | 0.065 | 0.18   | 0.18   | 0.065 | 0.13   | 0.18   | 0.13       |
| F04 delay              | 130   | 17    | 170   | 47     | 47     | 17    | 35     | 47     | 35         |
| Supply Voltage [V]     | 3-7   | 1.2   | 1.2   | 1.8    | 1.2-1.8| 1.2-1.5| 1.4-1.8 | 1.2-1.5   |
| Output Voltage [V]     | 2.3-2.5 | 1   | 1.2   | 1.1    | 1.1    | 1.2-1.6 | 1         |
| Dropout Voltage [mV]   | 446   | 200   | 200   | -      | 100    | 200   | 200    | 100     |
| PSR [dB]750kHz         | -     | -     | -52†  | -44†   | -45†   | -50†  | -70†   |
| Noise@100kHz (mV/Hz)   | -     | -     | -43†  | -42†   | -30†   | -50†  |
| IqMax – IqMin [µA]     | 0-150m | 0-50m | 0-50m | 10µ-10m| 1m-100m| 100µ-50m| 1µ-100m| 0.1m-300m| 1µ-100m |
| Lq [µA]                | 110   | 13.2  | 23.7  | 265    | 110    | 50-190| 0.7    | 0.94-255 | 6.2       |
| Cc [F]                 | 0.47µ | 10p-100m | 10p-10m| 200p-500m| 0-1µ | 0-2n | 0-1µ | 0-1µ | 0-1µ      |
| δVout [mV]             | 1900† | 44†   | 39    | 40†    | 176    | 77    | 76     | 37     | 170        |
| δVout – (–δVout) [mV]  | 2500† | 342†  | 58    | 30†    | 140    | 80    | 198    | 96     | 234        |
| Average Iq, tΔ, Δt [ns] | 2000 | 100†  | 100   | 50     | 1000   | 2    | 1000   | 1000   | 1000       |
| Rise time ratio K      | 1000  | 50    | 50    | 250    | 500    | 1     | 500    | 500    | 500        |
| Active Area [mm²]      | -     | -     | 0.079 | 0.039  | 0.01   | 0.047 | 0.037  | 0.018   |           |
| FOM1 [6]Noise†  | 17.6* | 101.9b | 7299.6d | 734192.65 † | 3.55* | 7.54** | 0.02* | 189237.36** | 0.25* |
| FOM2 [V/µs]            | 203.8 | 22.08 | 7.91  | 258.27 | 598.32 | 40.72** | 1.06  | 7.92** | 6.6       |
| FOM3 [10¹]             | 0.38b | 59.94 | 214.69 | 6584.6 | 6.79b | 20.19** | 0.05b | 100624.62** | 0.72b |

References [6], [18] and [19] reported smaller values for the output voltage undershoots and overshoots than this work, but they used smaller load steps - from 0 A to 50 mA – and they required up to ten times more quiescent current than the LDO presented here. The second smallest quiescent current was reported by [21], but it refers only to the no-load operation; as that LDO uses an adaptive biasing technique, its quiescent current increases as the load current increases, reaching values above 100µA at full load.

The smallest quiescent current is reported by [13] and it achieves better FOMs value than the LDO presented here. In fact, the circuit we introduced in [13] is a particular case of the topology shown in Fig. 2, with a circuit implementation optimized for ultra-low power consumption. The error amplifier in [13] employs a common-gate input stage, to maximize the speed. Thus, it consumes only 0.7 µA and its transient response is slightly below 300mV for a load jump of 100mA. However, it is inferior to the LDO presented in this paper with respect to three other parameters: its PSR value at low-frequency is 20 dB smaller, the output noise at 100 kHz is five times larger and its output voltage overshoot caused by a 300 mV/2.5 µs line jump is 1.5 times worse.

The LDO presented here exhibits the largest $\Delta V_{out, pkpk}$ for $C_{L} = 0$, but a value of 1pF was used to calculate FOM1. Even so, the FOM1 value for the proposed LDO is the second

TABLE 2. Performance comparison of LDOs designed to operate with small load capacitors, up to hundreds of pF.

| PARAM            | [4]† | [22]† | [23]†† | [24]†† | [25]†† | [26]†† | [27]†† | This work†† |
|------------------|------|-------|--------|--------|--------|--------|--------|------------|
| **Year**         | 2015 | 2017  | 2018   | 2019   | 2019   | 2020   | 2021   | 2021       |
| CMOS [µm]        | 0.18 | 0.18  | 0.13   | 0.13   | 0.065  | 0.065  | 0.065  | 0.13       |
| F04_delay        | 47   | 47    | 35     | 35     | 17     | 17     | 17     | 35         |
| Supply Voltage [V] | 1.8  | 1–1.4 | 1–1.4  | 1.2    | 1.2–2.5| 0.95–1.2| 1.2    | 1.2–1.5    |
| Output Voltage [V] | 1    | 1     | 0.8    | 1      | 1.0–1.3| 0.8    | 1      | 1          |
| Dropout Voltage [mV] | 90   | 200   | 200    | 200    | 200    | 200    | 150    | 100        |
| PSR [dB] @1kHz   | -    | 65    | 62*    | 92*    | 45*    | 34     | 57*    | 70*        |
| @10kHz           | -    | 53    | 56*    | 85*    | 26*    | 33     | 56*    | 50*        |
| Noise@1kHz[mV/Hz] | -    | -     | -      | 41     | -      | -      | -      | 192†       |
| Lmax [µF]        | 10µ-100m | 0-100m | 120µ-25m | 50-50m | 150µ-70m | 100m-100m | 1µ-100m | 6.2        |
| C1 [pF]          | 0-100p | 0-300p | 0-25p  | 0-400p | 0-100p | 0-100p | 300p   | 0-1µ        |
| ΔVout [mV]       | 212   | 42    | 21     | 80     | 180    | 133    | 71     | 170        |
| ΔVout [mV]       | 274   | 39    | 14     | 140    | 322    | 230    | 59     | 234        |
| Average Ii, t40, Δt [ns] | 1000 | 300   | 10     | 100    | 100*   | 132.5  | 0.8    | 1000       |
| Rise time ratio K | 1250  | 375   | 12.5   | 125    | 125    | 125    | 125    | 1250       |
| Active Area [mm²] | -     | -     | -      | 0.008  | 0.046  | 0.007  | 0.0105 | 0.053      |
| FOM1 [6]         | 5.44c | 19.52*** | 48.63** | 1478.4a | 98.48** | 50.82c | 5367.29** | 0.25*      |
| FOM2 [V/µs]      | 12.39 | 3**   | 27.24** | 26.4   | 117.35** | 16.42  | 59.37** | 8.95       |

*Calculated considering C1 values that result in the worst-case ΔVout. †± uncertainties: C1 = 1 pF; C1 = 100 pF; C1 = 1000 pF. ††Measurements were done for C1 varying from 0 to 1 µF, but according to simulations shown in Fig. 17, the proposed LDO can handle any practical C1. †Simulation; ††Measurements.

best, 14 times better than the nearest competitor, [20], and 30 times better than the next one, [6].

The LDO presented here also yielded the second-best FOM2 value, overtaken only by the LDO we reported in [13], which is based on the same topology.

To calculate the FOM3 for the LDO presented here the maximum C_L value was considered 1 µF, as measurement results were presented only for this value. Under these conditions, our LDO occupies the third place, with an FoM3 value twice as large as the second-best. However, it should be noted that the LDO reported in [7] owns its second place to its large maximum C_L value, 47 µF, a value the LDO presented here can handle, according to Fig. 17(c).

Table 2 lists the main parameters of other seven LDOs, this time designed for load capacitors with maximum values in the hundreds of pF range. When compared against these LDOs, the LDO described in this work exhibits the best FoM1 value - 21 times better than the second best, [4] – and the second-best FoM2 value. It should be noted that the best FoM2 is yielded by the LDO reported in [22], which occupies the third position with respect to FoM1.

The data presented in Table 1 and Table 2 indicates that the LDO proposed in this work performs very well against its competitors in terms of power consumption and ability to handle a wide range of load capacitors, while ensuring a good response to steep and large variations of the load current.

IV. CONCLUSION

This paper presents an LDO topology and a circuit implementation that provides fast responses to load transients and can handle any practical capacitive loads, from near-zero to ten-hundreds of µF. Besides the main voltage control feedback loop, the LDO topology employs an additional feedback loop, connected directly between the LDO output and the gate of the pass transistor. This additional loop is implemented by a novel circuit, which not only ensures a fast response to load transients but also helps improve the LDO frequency compensation, especially at light loads. This circuit can be used in conjunction with most types of error amplifiers, for LDOs that exhibit a relatively large small-signal resistance between the gate of their pass transistor and the ground line.

A very compact transistor-level implementation of the proposed LDO was presented: the Fast transient & Frequency compensation circuit described above was embedded into the structure of an OTA with high slew rate, so that only passive elements had to be added, while all MOS transistors were obtained by dual-using transistors within the initial OTA. In this way, no additional quiescent current was required, and the die area required by the additional circuitry was minimized.

A simplified, intuitive, and effective small-signal analysis of the proposed LDO was performed; it yielded insight into the LDO operation under various conditions for the load current and capacitance, as well as key sizing equations.
An LDO based on the proposed topology and circuit implementation was integrated in a 130 nm CMOS process. Simulation results and measurements performed on a test chip confirmed the excellent performance of the proposed LDO.

A comprehensive comparative analysis was performed against fifteen LDOs reported previously, with similar levels of output voltage and current: eight of them designed for a wide range of external decoupling capacitors and seven LDOs designed for narrow ranges of on-chip load capacitors. Three Figure-of-Merit metrics were used, two of them introduced in previous works and one newly proposed. They considered the quiescent current, the maximum load current and load capacitance, the output voltage undershoot and overshoot — in absolute value or referred to the nominal value - and the slope of the current step. Two of them also include edge time and process scaling. The LDO reported by this work yielded the first and second-best values for two of these metrics and the third-best for the third. Therefore, one can conclude that it provides a very good overall performance, considering the power consumption and the ability to handle a wide range of load capacitors while ensuring a good response to steep and large variations of the load current.

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