Drain-Engineered Reconfigurable Transistor Exhibiting Complementary Operation

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Abstract

In this paper, we propose and simulate a multifunctional transistor that exhibits device reconfigurability and realizes both nFET and pFET electrical characteristics when adequately biased. The use of this device will significantly reduce the transistor count in realizing sequential and combinational circuits and will result in highly compact design. The device uses a dual fin structure having a single mid-gap workfunction gate ($\sim 4.65$ eV) alongside dual metal (metal-silicide) drain regions. It employs $n^+/p^+/i$ junctions at the source-channel interface along with the Schottky junctions at the channel-drain interface. In practice, metal-silicides such as erbium/ytterbium silicide (ErSi$_x$/YbSi$_x$) for the $n$-drain and platinum silicide (PtSi) for the $p$-drain can be used as they provide smallest electron and hole Schottky-barrier heights (SBHs). Simulations carried out using calibrated parameters show better drive current ($\approx 10^{-2} - 10^{-3} \text{A}/\mu\text{m}$) compared to the quantum tunneling current in simulated state-of-the-art multifunctional devices ($\approx 10^{-4} - 10^{-5} \text{A}/\mu\text{m}$). In addition, butterfly curves show symmetric high (NM$^H$) and low (NM$L$) noise margins of 0.43V and 0.29V for zero and finite SBHs, respectively. The switching characteristics is shown to have an overshoot of $\sim 0.15$V for realistic SBHs which is then eliminated for the case of zero SBHs. In the last section, it is also demonstrated that a simplified structure having single mid-gap workfunction ($\sim 4.65$ eV) drain of Nickel silicide (NiSi) does not hamper the reconfigurability of the device.

Keywords MOSFET · Multifunctional circuit · CMOS · Schottky junction

1 Introduction

For the past four decades, the primary technique used in the VLSI industry to keep Moore’s law valid is the aggressive scaling of the MOSFET physical dimensions. This so far has resulted in high level of device integration and has given rise to integrated circuits (IC’s) with high speed and density [1, 2]. However, as CMOS dimensions have entered into the nanometer regime, the ever-increasing short-channel effects (SCes) along with the unscalable subthreshold slope (SS $\sim 60 \text{mV/dec}$) limit of the MOSFET [2], and similar current transport devices [3, 4], has resulted in a rapid rise in the leakage current. This increases the standby power consumption significantly, and in consequence, has imposed the limit on transistor integration alongside the switching speed [5].

Steered by the need to overcome the aforementioned limitations, various advanced device geometries including FD SOIs[3], III-V MOSFETs [5], FinFETs[6], nanowire FETs[7] have been proposed in the literature. Alternate current transport devices based on Schottky barrier tunneling based dopant-segregated ultrathin-body MOSFET [8, 9], band-to-band tunneling (BTBT) such as silicon based lateral/line Tunnel FETs [10–12], graphene based TFET [13], negative capacitance (NC) based nanowire TFETs [14] and junctionless FET [15] alongside electrostatically-doped source-drain TFETs[16] have also been explored. In addition, to overcome the doping limitations, DG architecture based on charge plasma concept[17], nanowire(NW)

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and nanosheet (NS) junctionless FETs [18–20] have also been heavily investigated. All these geometries have so far focused on achieving the increased performance out of the individual device unit alongside supply voltage (V_{DD}) scaling, whereas a few handful of them have tried to increase the device functionality instead [21–23]. In this regard, Si NWs based reconfigurable transistor that can be programmed dynamically by an external voltage were fabricated [24]. The NWs are undoped and are controlled by a dual Schottky junctions at the source-channel and channel-drain ends. In consequence, carrier injection (holes for pFET and electrons for nFET) can be modulated by keeping one gate voltage constant and other variable. Another device fabricated that exhibit reconfigurability is a vertically-stacked (VS) Si Gate-all-around (GAA) NW FET having control-gate (CG) and polarity-gate(PG) [25]. PG is kept constant which determines the mode and CG acts as a conventional gate in that particular mode. Earlier, a complementary device using a double-gate (DG) architecture based on a Schottky-barrier (SB) tunneling has also been demonstrated via simulations [22]; however, it has certain downsides: 1) the inherently low drive current associated with the SB FET; 2) the need of two individually tuned gate workfunctions for optimum device functionality; 3) the leakage due to the coupling between non-isolating channels during the pFET and nFET operation. Other than this, in terms of fabrication, complementary operation in a single device so far reported [22, 24–27] have been at the cost of high operating voltages (V_{DD} of ~ 3–4V).

Most of the complementary devices are based on the Schottky tunneling based current injection mechanism; however, they inherently suffer from low drive current compared to conventional FET. To understand the reason for this, we revisited the fundamentals. For a silicide source, the emitted current density \( J_e \) is composed mainly of two components, i.e., the thermal emission \( J_{th} \) and the current due to quantum mechanical tunneling through the Schottky barrier \( J_{fe} \) (thermionic field-emission and field-emission current are clubbed together here for simplicity). At small \( V \) (gate voltage), \( J_e \) equals \( J_{th} \); however in the ON-state, when there is a high field, \( J_e \) is mainly dominated by the \( J_{fe} \). So, unlike the conventional FET wherein current is controlled by the thermal-emission barrier in the channel, current in SB FET is limited by the tunneling barrier at the source [28–30]. For this reason, a low current drivability in SB FET is observed.

Keeping in view the above drawbacks, in this paper, a transistor exhibiting device reconfigurability is proposed and simulated and can also be biased in the inverter mode. The veracity of the complementary switching mechanism is envisaged using a dual fin design having doped \( n/p \) sources and metal (metal-silicide) as drains. The device is being termed as a Drain-Engineered Reconfigurable FET (DE RFET) due to the connected metal (metal-silicide) drains. It overcomes the low drive current originating from the quantum tunneling current \( J_{fe} \), as present in the silicide-source SB FET architecture [22]. Additionally, the wrap-around gate architecture facilitates the path to volume inversion compared to that of a thin inversion layer in DG architecture.

Recently, we have also proposed a vertically stacked dual drain exhibiting reconfigurability [31] but its junctionless behavior demands complex doping strategy, and therefore, dual fin design mitigates this to some extent. The present work employs single gate and differs from [31] as it has double gate architecture. In addition, in the present work, the choice of single silicide drain having mid-gap workfunction to simplify the device architecture is also proposed in the last section.

2 Device Structure

Figure 1(a) and (b) shows a bird’s eye view alongside the top view of the proposed DE RFET. Fin isolation width of 60nm is used to separate N-source (donor ND = 1×10^{20} cm^{-3}) and P-source (acceptor NA = 1×10^{20} cm^{-3}) regions. Two silicon fins, controlled by a single gate, will contribute individually to the \( n/p \) sections of the device operation. Both the sections have an extended undoped channel length of L_{ext}. In addition, dual-connected \( n/p \) silicide drains of suitable workfunction, \( \phi_{Dn} \) and \( \phi_{Dp} \) (or SBH, \( \Phi_{Dn} \) and \( \Phi_{Dp} \)), are used to sink-in the electron and hole currents, respectively, during the \( n/p \) FET operations. All other device parameters are provided in the Table 1.

It is an arduous task to come up with a detailed process flow until the device has actually been fabricated. However, key processing possibly include: starting with an SOI wafer, the device island can be patterned with fins [34]. Next, gate dielectric can be thermally grown or deposited. After this, gate metal layer such as titanium nitride (TiN) can be deposited via chemical or plasma vapor deposition (CVD or PVD) and then patterned [35]. Next, silicon nitride gate-sidewalls spacers can be formed [34]. Thereafter, selective deposition of borosilicate glass (BSG) layer and phosphosilicate glass (PSG) layer, respectively, for \( p \)-type and \( n \)-type doping can be done, followed by the high temperature annealing process [35]. Selective deposition of near band-edge workfunction Pt metal for D2 and Er or Yb metal for D1 can next be done, followed by silicidation to form connected drains. Unreacted metals can be removed using wet chemical etch. Finally, metallization and chemical mechanical polishing (CMP) can be done.
Fig. 1 (a) Bird’s eye view of the proposed DE RFET schematic with terminals shown. (b) Shows the top view of the DE RFET having dual fins. Cutlines/Cutplanes AA’ and BB’ are drawn the fins. Simulation models were calibrated from fabricated the tri-gate SOI JLT [32] by matching the transfer characteristics. In addition, lateral tunneling parameters are taken from [33] to account for the OFF-state leakage.

3 Simulation Methodology

To have a proper Schottky junction at the channel-drain interface, complementary or near band-edge metal-silicides are required. The choice of workfunctions for the same are as follows: \( \Phi_{Dn} < \Phi_{Si} < \Phi_{Dp} \) where \( \Phi_{Si} = \chi_{Si} + E_g/2 \), is the undoped silicon workfunction; \( \chi_{Si} \) is the electron affinity (4.05eV), \( \Phi_{Dn} \) and \( \Phi_{Dp} \) are \( n/p \) metal drain workfunctions and \( E_g \) is the bandgap of bulk silicon (1.12eV). \( \Phi_{Dn} < \Phi_{Si} \) [36, 37] provides no barrier to electron flow but creates barrier for hole diffusion from silicon to metal (metal-silicide). Similarly, \( \Phi_{Dp} > \Phi_{Si} \) [36, 37] provides no barrier to hole flow but creates barrier for electron diffusion from silicon to metal (metal-silicide). In practice, near band-edge metal-silicides such as erbium silicide ErSi\(_x\) or ytterbium silicide YbSi\(_x\) (\( \Phi_{Dn} \sim 0.27–0.36eV \) for electrons) [37, 38] for the \( n \)-drain (D1) and nickel or platinum silicide (\( \Phi_{Dp} \sim 0.15–0.27eV \) for holes) [37, 38] for the \( n \)-drain (D2) can be used. Here, \( \Phi_{Dn} \) and \( \Phi_{Dp} \) are, respectively, the smallest electron and hole SBH reported with the silicon, [38]. Ideally, the SBH \( \Phi_{Dn} \) and \( \Phi_{Dp} \) equals \( \Phi_{Si} \) for the \( n \)-drain and \( (E_g - \Phi_{Dp} + \chi_{Si}) \) for the \( p \)-drain, respectively, however, it may vary depending upon the non-idealities. In addition, close to mid-gap workfunction for the gate, corresponding to the TiN metal [39] (~4.6–4.9eV), is chosen.

All 3-D simulations were performed on the Synopsys Sentaurus TCAD [40]. Various models invoked in the simulations are Philips unified mobility model that takes into account the concentration dependent mobility along with its degradation due to both impurity and carrier-carrier scattering. In addition, Bandgap narrowing model (BGN) due to the highly doped \( n/p \) source, Shockley-Read-Hall

| Parameter | Value |
|-----------|-------|
| Fin width, \( W_{fin} \) | 10-20 nm |
| Fin gap | 60 nm |
| Fin height, \( H_{fin} \) | 20-60 nm |
| Gate length, \( L_g \) | 20-50 nm |
| Effective oxide thickness, \( t_{ox} \) | 1 nm |
| \( n/p \) source length, \( L_{on}=L_{op} \) | 50 nm |
| Extended channel, \( L_{ext} \) | 5-20 nm |
| BOX thickness, \( T_{BOX} \) | 50 nm |
| Substrate thickness, \( T_{Sub} \) | 100 nm |
| Gate workfunction (\( \Phi_G \)) | 4.65 eV |
| \( n/p \) drain workfunction (\( \Phi_{Dn}/\Phi_{Dp} \)) | 4.05/5.02 eV |
| Source doping, \( N_D \) | \( 1 \times 10^{20} \) cm\(^{-3} \) |
| Drain doping, \( N_A \) | \( 1 \times 10^{20} \) cm\(^{-3} \) |
| Channel doping | \( 1 \times 10^{18} \) cm\(^{-3} \) |
| Substrate doping | \( 1 \times 10^{15} \) cm\(^{-3} \) |
| Supply voltage, \( V_{DD} \) | 1V |
(SRH) and Auger recombination models are also invoked. Fermi statistics is utilized in conjunction with the drift-diffusion physics. As indicated in the Fig. 1(c), simulation models were first calibrated by reproducing the transfer characteristics and matching it with the tri-gate SOI JLT [32]. To account for the lateral tunneling dominant in the OFF-state, nonlocal BTBT model calibrated from the [11, 33, 40] is activated. Besides, carrier confinement due to the quantization effect is taken care of using the modified local density approximation (MLDA) model.

4 Results and Discussion

4.1 Biasing Scheme and Transfer Characteristics

Figure 2(a) and (b) shows the working and biasing scheme of the device for the n/p FET operations. For pFET, the n-section of the fin remains in equilibrium and vice-versa. As shown in the figure, during pFET operation, at $V_G=0V$, a path for hole flow between the $p$-source (S2) and $p$-drain (D2) is created and conduction occurs. Similarly, for nFET operation, with $V_G=V_{DD}$, a path for electron flow between the $n$-source (S1) and $n$-drain (D1) is created.

4.2 Band Diagrams During n/p FET Operation

Figure 3(a) and (b) shows the band diagrams, respectively, for the pFET configuration taken across the cutline AA’ and BB’. In a p-section fin, we observe a barrier to the current flow (h^+ s) at the source-channel junction in the OFF-state,
which then is eliminated with the applied gate bias in the ON-state. Note that the n-section during the pFET operation remains in equilibrium and remains inactive. Similarly, during nFET as shown in the Fig. 3(c) and (d), p-section fin remains inactive and the other fin contribute to the conduction with the proper gate bias. Here, $E_{fn}$ and $E_{fp}$ represent the fermi-level in the n-drain (D1) and p-drain (D2) regions, respectively.

### 4.3 OFF-State Leakage During n/p FET Operation

Further, to understand the reason for the OFF-state leakage, Fig. 4(a) shows the nFET OFF-state 2-D hole generation rate showing the increased lateral tunneling at smaller $L_{ext}$ of 5nm, verifying the increased leakage in the OFF-state, shown in the Fig. 2(e) and (f). In nFET, carriers tunneling constitutes of the holes moving from the metallic drain region (D1) and CB of the underlap region into the channel VB. As shown in the Fig. 4(b), we also observe the tunneling during pFET operation for $\phi_G = 4.65$eV at reduced $L_{ext} = 5$nm. This is due to the sufficient band bending across the channel/drain region during the pFET operation, which results in the tunneling of electrons from the metallic drain region (D2) and CB of the underlap region into the channel VB.

### 4.4 Current Density Profile During n/p FET Operation

Figure 5(a) and (b) shows the $e^-$CurrentDensity and $h^+$CurrentDensity, respectively, for the nFET and pFET operating conditions. At $V_G = V_{DD}$, only n-section fin is active and have a large $e^-$CurrentDensity constituting the nFET current while at the same time, pFET fin remains inactive. Similarly, during pFET operation, at $V_G = 0$V, only p-section fin is active and have a large $h^+$CurrentDensity accounting for the pFET current while the nFET fin remains inactive. This verifies the complementary FET operation realized using the dual fins in a single device.

### 4.5 Output, VTC and Transient Characteristics

The output characteristics corresponding to the n/p FET configurations are shown in Fig. 6(a). The pFET drain current flows between the terminal D2 and S2, denoted by $I_{DS2}$ and corresponding, nFET drain current flows between the terminal D1 and S1, denoted by $I_{DS1}$. A reasonable output characteristics with good saturation are obtained for both the modes. As depicted in Fig. 6(b), when DE RFET is configured as an inverter unit with biasing scheme shown as an inset in the figure, a reasonable symmetric VTC curve with good high and low logic levels ($V_{OH}$ and $V_{OL}$) were
**Fig. 4** 2-D contour profile showing OFF-state holes generation rate for (a) nFET along the cutplane AA’, (b) pFET along the cutplane BB’. $\phi_G = 4.65 \text{eV}$

**Fig. 5** (a) nFET $e^-$ Current Density at $V_G = V_{DD}$. Shows negligible $e^-$ Current Density between S2 and D2. (b) pFET $h^+$ Current Density at $V_{in} = 0 \text{V}$. Shows negligible $h^+$ Current Density between S1 and D1. Gate where $V_G$ is applied, is deliberately removed for clarity.

**Fig. 6** (a) Output curves of both the n/p FETs are shown. Voltage transfer characteristic (VTC) of the DE RFET (b) with $V_{DD}$ scaling, (c) for different $\phi_G$. Inset of (b) shows the device operating in inverter mode. (d) Switching characteristics of the DE RFET at $V_{DD} = 1 \text{V}$
obtained at \( V_{DD} = 1 \text{V} \). The reason is the matched \( n/p \) FET characteristics obtained with the gate workfunction tuning, \( \phi_G \) to 4.65eV (slight ON-current mismatch occurs due to the mobility difference between the holes and electrons).

However, \( \phi_G \) of 4.75eV adversely shifts the cross-over \( n/p \) FET voltage close to 0.6V, as illustrated in the Fig. 6(c). This will, in turn, result in the asymmetric noise margins (\( \text{NMH} > \text{NML} \)) which was reduced by an optimum \( \phi_G \) of 4.65eV. A slight mismatch in \( n/p \) FET ON-currents still persists; however, VTC curve remains close to symmetric, implying equal high and low noise margins. We have also shown the impact of the \( V_{DD} \) scaling on the VTC curve upto 0.6V. DE RFET design offers the possibility of scaling the \( V_{DD} \) without much degradation in the VTC. Further, Fig. 6(d) shows the transient analysis of the DE RFET when subjected to a ramp input pulse of 1V peak-voltage with rise time: \( t_r \approx 1 \text{ps} \), fall time: \( t_f \approx 1 \text{ps} \) and on time: \( t_{on} \approx 50 \text{ps} \). A close to CMOS-like switching characteristics with minimal rise/fall propagation delay is achieved using only a single device.

### 4.6 Impact of Device Parameter Scaling on Reconfigurability

With recent trends moving towards the device scaling, it is essential to explore its impact on the device performance. In this regard, Fig. 7(a)-(c) compares the impact of gate length, \( L_g \), fin width, \( W_{fin} \) and fin height, \( H_{fin} \) scaling upon the reconfigurability of the DE RFET. We observe a significant deterioration in the ON/OFF ratio at \( L_g = 20 \text{nm} \) compared to that at 50nm, both for the \( nFET \) (\( \approx 10^6 \)) and the \( pFET \) (\( \approx 10^4 \)) operation of the device. This is due to the increased short-channel-effects (SCEs) causing reduced gate controllability at short gate lengths. This can be mitigated by reducing the fin width alongside the use of smaller EOT of 0.5nm. We further observe that increasing the fin height increases the ON-current of the device without much degradation in the OFF-state current. Similar observation is also made for the fin width. With reduction in the \( W_{fin} \), tight gate control results in better subthreshold slope. Despite all these variations, the reconfigurability aspect of the DE RFET remains intact with reasonable deviations in the device parameters. Further, Fig. 7(d) explores the plausibility of using the proposed DE RFET as the supply voltage, \( V_{DD} \) is scaled. The device works reasonably well in the inverter mode up to the \( V_{DD} \) of 0.6V.

Moreover, DE RFET, as a reconfigurable device has also been compared with the existing literature, as listed in the Table 2. The device is comparable in terms of performance with the window for further reducing the operating voltage.

### 4.7 Impact of Finite SBH

So far we have taken D1 and D2 workfunctions as such that the effective SBH is close to zero. However, in practice
| Devices                  | Design | Ref. | Current injection at source | Lg  | Modes | $V_D$ | $V_G$ | $I_{ON}$ ($A/\mu m$) | SS ($mV/\text{dec}$) |
|-------------------------|--------|------|-----------------------------|-----|-------|-------|-------|---------------------|---------------------|
| SSS; simulated.         | DG     | [22] | Schottky                    | 50nm| $n$   | 0.5V  | 0.5V  | $\approx 1 \times 10^{-5}$ | $\approx 130$       |
| SiNW RFET; fabricated. | NW     | [24] | Schottky                    | -   | $n$   | 1V    | 3V    | $\approx 2.5 \times 10^{-4}$ | $\approx 220$ (min) |
| DH-FET; fabricated.     | Bulk   | [26] | Thermionic emission         | -   | $n$   | 2.5V  | 2.5V  | $\approx 7 \times 10^{-4}$ | -                   |
| TF-TFET; simulated.     | DG     | [27] | BTBT                        | 30nm| $n$   | 0.5V  | 0.5V  | $\approx 1 \times 10^{-5}$ | $\approx 30$ (min)   |
| SiNW GAA FET; fabricated.| NW    | [25] | Schottky                    | 45nm| $n$   | 2V    | 4V    | $\approx 1.7 \times 10^{-3}$ | $\approx 70$        |
| VS NS JLFET; simulated. | JL/Stacked Nanosheet(NS) | [31] | Thermionic emission         | 50nmNS width=7nm | $n$ | 0.8V | 0.8V | $\approx 1.8 \times 10^{-4}$ | $\approx 95$        |
| DE RFET; simulated.     | SOI (fin) | This work | Thermionic emission         | 50nm| $n$   | 1V    | 1V    | $\approx 1.2 \times 10^{-2}$ | $\approx 60$ (min)   |
the SBHs are not negligible rather it has a finite value. Therefore, here we set the electron SBH for D1: \( \Phi_{Dn} \approx 0.28 \text{eV} \), corresponding to the erbium silicide ErSi
subscript{x} and hole SBH for D2: \( \Phi_{Dp} \approx 0.15 \text{eV} \), corresponding to the platinum silicide PtSi. We then observe in the Fig. 8(a) that the VTC curve is slightly degraded due to the increased barrier resistance existing at the channel-drain junctions. To assess and evaluate the noise margin, we have considered two conditions, as indicated in the Fig. 8(b) and (c): 1) VTC with ideally zero SBHs and 2) VTC with finite SBHs. In both cases we have drawn butterfly curves and calculated the high and low noise margins, \( \text{NM}_H \) and \( \text{NM}_L \). For the

Fig. 9 (a) Schematic of DE RFET with single mid-gap silicide, \( \Phi_{Dn} = \Phi_{Dp} = 4.65 \text{eV} \). Comparison of \( I_D-V_G \) characteristics (b) during n-FET operation and (c) during p-FET operation
case of zero SBHs, $N_{M} = N_{L} = 0.43V$ while for the finite SBHs, $N_{M} = N_{L} = 0.29V$ is observed. Equal noise margin indicates that the VTC is close to symmetric. Further, in Fig. 8(d), the impact of finite SBHs on the inverter characteristics is analyzed. We observe increased overshoot voltage alongside increased output delay in comparison to the zero SBH case shown in the Fig. 7(d).

4.8 Impact of Single Mid-Gap Silicide on Reconfigurability

In this section, a new device architecture having a single silicide as a drain region is analyzed instead of two near band edge silicides, as shown in the Fig. 9(a). A mid-gap drain silicide (NiSi) corresponding to the workfunction of 4.65eV is used. We observe marginal decrement in the SBH at the channel-drain junction of both the fins. Further, it is noteworthy that the mid-gap silicide also increases the lateral tunneling of carriers during the OFF-state. The use of single drain silicide, however, does not hamper the reconfigurability and we observe good $I_D-V_G$ characteristics, as shown in the Fig. 9(b) and (c). Finally, we can infer that the proposed concept is generic in nature, and therefore can be further extended to other device geometries or alternate current transport devices.

5 Conclusion

In summary, using 3-D mixed-mode simulations, a new device concept, DE RFET, is proposed and investigated. The device can be reprogrammed as an n-type, p-type FET and a complete inverter unit with adequate biasing. The use of single mid-gap silicide or connected dual near band-edge metal (metal-silicide) drains envisage the complementary switching action. Insights into the device operation reveals device reconfigurability, CMOS-like inverter action with a window for future $V_{DD}$ scaling.

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consent to participate YES

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References

1. Henson WK, Yang N, Kubicek S, Vogel EM, Wortman JJ, De Meyer K, Naem A (2000) Analysis of leakage currents and impact on off-state power consumption for cmos technology in the 100-nm regime. IEEE Trans Electron Devices 47(7):1393–1400. https://doi.org/10.1109/16.848282
2. Horowitz M, Alon E, Patil D, Naffziger S, Kumar R, Bernstein K (2005) Scaling, power, and the future of cmos, in IEDM Tech. Dig IEEE 7–15. https://doi.org/10.1109/IEDM.2005.1609253
3. Loan SA, Qureshi S, Iyer SSK (2010) A novel partial-ground-plane-based mosfet on selective buried oxide: 2-d simulation study. IEEE Trans Electron Devices 57(3):671–680. https://doi.org/10.1109/TED.2009.2039545
4. Ehteshamuddin M, Loan SA, Rafat M (2018) Planar junctionless silicon-on-insulator transistor with buried metal layer. IEEE Electron Device Lett 39(6):799–802. https://doi.org/10.1109/LED.2018.2829915
5. Del Alamo JA (2011) Nanometre-scale electronics with iii–v compound semiconductors. Nature 479(7373):317. https://doi.org/10.1038/nature10677
6. Rahman A, Dacuna J, Nayak P, Leatherman G, Ramey S (2018) Reliability studies of a 10nm high-performance and low-power cmos technology featuring 3rd generation finfet and 5th generation hk/mg. In: 2018 IEEE international reliability physics symposium (IRPS), pp 6F.4–1–6F.4–6. https://doi.org/10.1109/IRPS.2018.8353648
7. Björk M, Hayden O, Schmid H, Riel H, Riess W (2007) Vertical surround-gated silicon nanowire impact ionization field-effect transistors. Appl Phys Lett 90(14):142110. https://doi.org/10.1063/1.2720640
8. Patil GC, Qureshi S (2013) Engineering buried oxide in dopant-segregated schottky barrier soi mosfet for nanoscale cmos circuits. Microelectronics Reliability 53(3):349–355. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0026271412004520
9. Patil GC, Quresi S (2013) Asymmetric drain underlap dopant-segregated schottky barrier ultrathin-body SOI MOSFET for low-power mixed-signal circuits. Semiconductor Science and Technology 28(4):045002. [Online]. Available: https://doi.org/10.1088/0268-1242/28/4/045002
10. Ehteshamuddin M, Loan SA, Rafat M (2018) A vertical-gaussian doped soi-fet with enhanced dc and analog/rf performance. Semiconductor Science and Technology 33(7):075016. https://doi.org/10.1088/1361-6641/aac97d
11. Ehteshamuddin M, Loan SA, Alharbi AG, Alamoud AM, Rafat M (2019) Investigating a dual moscap variant of line-fet with improved vertical tunneling incorporating fiquc effect. IEEE Transactions on Electron Devices 66(11):4638–4645. https://doi.org/10.1109/TED.2019.2942423
12. Wang P, Tsui B (2016) Band engineering to improve average subthreshold swing by suppressing low electric field band-to-band tunneling with epitaxial tunnel layer tunnel fet structure. IEEE Trans Nanotechnol 15(1):74–79. https://doi.org/10.1109/TNANO.2015.2501829
13. Fahad MS, Srivastava A, Sharma AK, Mayberry C (2016) Analytical current transport modeling of graphene nanoribbon tunnel field-effect transistors for digital circuit design. IEEE Trans Nanotechnol 15(1):39–50. https://doi.org/10.1109/TNANO.2015.2496158

14. Kobayashi M, Jang K, Ueyama N, Hiramoto T (2017) Negative capacitance for boosting tunnel fet performance. IEEE Trans Nanotechnol 16(2):253–258. https://doi.org/10.1109/TNANO.2017.2658688

15. Bhagat KB, Patil GC (2019) Negative capacitance δ bulk planar junctionless transistor for low power applications. Micro & Nano Letters 14(10):1107–1110

16. Kumar M, Jit S (2015) Effects of electrostatically doped source/drain and ferroelectric gate oxide on subthreshold swing and impact ionization rate of strained-si-on-insulator tunnel field-effect transistors. IEEE Trans Nanotechnol 14(4):597–599. https://doi.org/10.1109/TNANO.2015.2426316

17. Hur J, Moon D, Han J, Kim G, Leon C, Choi Y (2017) Tunneling effects in a charge-plasma dopingless transistor. IEEE Trans Nanotechnol 16(2):315–320. https://doi.org/10.1109/TNANO.2017.2663659

18. Lin Y, Cheng C, Jhan Y, Kurniawan ED, Du Y, Lin Y, Wu Y (2018) Hybrid p-channel/n-substrate poly-si nanosheet junctionless field-effect transistors with trench and gate-all-around structure. IEEE Trans Nanotechnol 17(5):1014–1019. https://doi.org/10.1109/TNANO.2018.2848283

19. Lin Y, Lin Y, Chen Y, Hsu Y, Chen Y, Huang Y, Wu Y (2020) Performance of junctionless and inversion-mode thin-film transistors with stacked nanosheet channels. IEEE Trans Nanotechnol 19:84–88. https://doi.org/10.1109/TNANO.2019.2960836

20. Georgiev VP, Mirza MM, Dochioiu A, Adamu-Lema F, Amoroso SM, Towie E, Riidet C, MacLaren DA, Asenov A, Paul DJ (2017) Experimental and simulation study of silicon nanowire transistors using heavily doped channels. IEEE Trans Nanotechnol 16(5):727–735. https://doi.org/10.1109/TNANO.2017.2665691

21. Marino FA, Stocco A, Barbato M, Zanoni E, Meneghesso G (2014) Double control gate field-effect transistor for area efficient and cost effective applications. IEEE Electron Device Lett 35(11):1073–1075. https://doi.org/10.1109/LED.2014.2354112

22. Loan SA, Kumar S, Alamoud AM (2016) A novel double gate metal source/drain schottky mosfet as an inverter. Superlattice Microst 91:78–89. https://doi.org/10.1016/j.spmi.2015.12.042

23. Kumar S, Loan SA, Alamoud AM (2016) Design of a novel high performance schottky barrier based compact transmission gate. Superlattice Microst 92:337–347. https://doi.org/10.1016/j.spmi.2016.02.030

24. Heinzig A, Slesareck S, Kreupl F, Mikolajick T, Weber WM (2011) Reconfigurable silicon nanowire transistors. Nano letters 12(1):119–124. https://doi.org/10.1021/nl103094h

25. De Marchi M, Sacchetto D, Zhang J, Frache S, Gaillardon P, Leblebici Y, De Micheli G (2014) Top–down fabrication of gate-all-around vertically stacked silicon nanowire fets with controllable polarity. IEEE Trans Nanotechnol 13(6):1029–1038. https://doi.org/10.1109/TNANO.2014.2363386

26. Marino FA, Meneghesso G (2011) Double-halo field-effect transistor—a multifunction device to sustain the speed and density rate of modern integrated circuits. IEEE Transactions on Electron Devices 58(12):4226–4234. https://doi.org/10.1109/TED.2011.2169067

27. Bagga N, Chauhan N, Gupta D, Dasgupta S (2019) A novel twofold tunnel fet with reduced miller capacitance: Proposal and investigation. IEEE Transactions on Electron Devices 66(7):3202–3208. https://doi.org/10.1109/TED.2019.2914305

28. Guo J, Lundstrom MS (2002) A computational study of thin-body, double-gate, schottky barrier mosfets. IEEE Transactions on Electron Devices 49(11):1897–1902. https://doi.org/10.1109/TED.2002.804696

29. Patil GC, Qureshi S (2012) Underlap channel metal source/drain soi mosfet for thermally efficient low-power mixed-signal circuits. Microelectronics Journal 43(5):321–328. special Section NANO-TECH 2011. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0026269211002655

30. Patil GC, Quresi S (2012) Engineering spacers in dopant-segregated schottky barrier SOI MOSFET for nanoscale CMOS logic circuits. Semiconductor Science and Technology 27(4):045004. [Online]. Available: https://doi.org/10.1088/0268-1242/27/4/045004

31. Ehteshamuddin M, Loan SA, Rafat M (2021) Drain-engineered vertically stacked junctionless fet exhibiting complementary operation. J Comput Electron 20(1):545–555

32. Colinge J-P, Lee C-W, Azfalian A, Akhavan ND, Yan R, Ferain I, Razavi P, O’neill B, Blake A, White M et al (2010) Nanowire transistors without junctions. Nature nanotechnology 5(3):225–229

33. Sahay S (2017) Design and analysis of emerging nanoscale junctionless fets from gate-induced drain leakage perspective. Ph.D. dissertation, Elect. Eng., Indian Institute of Technology, Delhi, India

34. Hu C, King T-J, Subramanian V, Chang L, Huang X, Choi Y-K, Kedzierski JT, Lindert N, Bokor J, Lee W-C (2002) Finfet transistor structures having a double gate channel extending vertically from a substrate and methods of manufacture. uS Patent 6,413,802

35. Wu C-C, Wu S-L (2007) Method of forming an n channel and p channel finfet device on the same semiconductor substrate. uS Patent 7,187,046

36. Rhoderick E, Williams R (1988) Metal-Semiconductor contacts. Oxford, vol 2

37. Gupta G, Rajasekharan B, Hueting RJE (2017) Electrostatic doping in semiconductor devices. IEEE Trans Electron Devices 64(8):3044–3055. https://doi.org/10.1109/TED.2017.2712761

38. Larson JM, Snyder JP (2006) Overview and status of metal s/d schottky-barrier mosfet technology. IEEE Trans Electron Devices 53(5):1048–1058. https://doi.org/10.1109/TED.2006.871842

39. Lima L, Dekkers H, Lisoni J, Diniz J, Van Elshocht S, De Gendt S (2014) Metal gate work function tuning by al incorporation in tin. Journal of Applied Physics 115(7):074504. https://doi.org/10.1063/1.4866323

40. TCAD Sentaurus Device Version J-2014. [Online]. Available: http://www.synopsys.com

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