A high-linearity capacitance-to-digital converter with capacitive offset cancellation technique

Chanrong Jiang¹, a), Changchun Chai¹, Yi Yang¹, and Yintang Yang¹

Abstract A linear, high-precision capacitance-to-digital converter (CDC) for grounded-type capacitive sensors is presented in this paper. The designed CDC consists of an analog front-end (AFE) circuit that converts capacitance to voltage signal and a noise-shaping successive approximation register (NS-SAR) analog-to-digital (ADC) that converts voltage to digital output. Firstly, in order to measure very small capacitance with a grounded target electrode in the presence of a large offset capacitance, a variable capacitance multiplier circuit is introduced, which ensures that the final output is independent of the offset capacitance. Secondly, the designed CDC implements a fully differential operational amplifier (FDOA) with two T-networks to reduce non-linearity, which provides an output proportional to the variable capacitance. Accordingly, the design complexity of the analog front-end circuit can be minimized effectively. The interface is designed as an integrated circuit using a standard 0.18 μm CMOS process. The functionality of the proposed CDC is verified first using simulation results, showing that for a sensor capacitance ranging from 1 fF – 1 pF, the minimum measurement accuracy can reach 0.1 fF with a parasitic capacitance up to 100 pF. The whole CDC consumes approximately 0.8 mA from a 1.8 V power supply.

Keywords: capacitance-to-digital converter (CDC), grounded capacitive sensor, linear front-end, noise-shaping SAR ADC

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Nowadays, capacitive sensors are well accepted in the fields of sensors due to their simple structure, high sensitivity, fast transient response and insensitivity to temperature variation, etc. [1, 2, 3, 4, 5, 6, 7]. Depending on the connection way of the measured capacitance to the interface circuit, the interface principles can be categorized as floating or grounded sensors [8, 9, 10, 11]. Sensing circuits favor the floating sensor due to their high noise immunity and insensitivity to sensor parasitic capacitance [12, 13, 14, 15]. However, in some specific applications, the target must be connected to grounded for safety reasons, that is, one of the electrodes of the capacitance must be grounded [16, 17, 18]. Such a configuration has many applications including ice layer detection [19], human proximity sensing [20] and touch screen sensor [21], etc.

Generally, a grounded capacitance sensor is modelled as a parallel combination of variable (to be measured) capacitance and parasitic capacitance, where the value of the parasitic capacitance is usually much larger than the value of the capacitance to be measured. The existence of such a large offset capacitance puts forwards more stringent resolution and dynamic range requirements for the electronic interface and may lead to increased power consumption and even design complexity.

The universally used approach, charge amplifier [22, 23, 24], improves the noise immunity of the CDC circuit, but this approach can be only directly used to floating capacitive sensors. Several solutions have been presented with a grounded capacitive sensor [8, 25]. However, the switched-capacitor active guarding has an effect on system errors, resulting in inaccurate measurement results. The latest high-performance capacitive sensor readout circuits often combine the capacitance detection front-end capacitor array with sigma-delta technique to obtain the digital output directly [26]. However, their oversampling procedure repeatedly charges and discharges the sensor capacitor, resulting in poor conversion energy. One power-efficient and easy-to-implement technique for CDC is composed of a capacitance-to-voltage converter (CVC) followed by an analog-to-digital converter (ADC).

In summary, there are three main issues to be resolved in designing a high precision CDC with simple structure and wide dynamic range. That is, capacitive offset cancellation technique, analog front-end circuit with high linearity output and an efficient ADC.

A new capacitance-to-digital converter circuit has been developed for capacitive sensors in grounded configuration in this paper. First, a variable capacitance multiplier circuit is introduced to counteract the influence of the offset capacitance, which greatly improves the measurement accuracy of the CDC circuit and reduces the area of the capacitance simultaneously. Second, in order to improve the linearity of the front-end circuit, a fully differential operational amplifier is used, which also improves the ability to resist the common mode noise interference. In addition, a noise-shaping SAR ADC is implemented to convert the voltage signal to the digital output, which can further improve the conversion accuracy while maintaining low power consumption.

Rest of the paper is organized as follows: Section 2 presents the architecture and control strategy of the proposed CDC circuit. Section 3 describes the circuit implementation. Simulation results and discussion are given in Section 4, which is followed by conclusion in Section 5.

¹ Wide Bandgap Semiconductor Technology Disciplines State Key Laboratory, Xidian University, Xi’an 710071, P.R. China
a) crjiangx@163.com

DOI: 10.1587/elex.17.20200268
Received August 4, 2020
Accepted August 27, 2020
Publicized September 9, 2020
Copyedited September 25, 2020

Copyright © 2020 The Institute of Electronics, Information and Communication Engineers
2. Architecture and control strategy

Fig. 1 shows the block diagram of the proposed CDC for grounded capacitive sensor with a variable capacitance multiplier, which is composed of two main blocks: analog frontend (AFE) circuit and the NS-SAR ADC. The AFE circuit converts the unknown capacitance into a linearly related voltage signal, which is then converted into digital output after sampling by the NS-SAR ADC. The analog interfaces for wide range capacitive sensors are typically based on sinusoidal wave generators, which generates an output voltage linearly related to the capacitance $C_X$ by periodically charging and discharging the capacitor.

Although the sensor itself is single-ended, the AFE circuit employs a fully differential operational amplifier with the same source impedance to increase the robustness to common-mode noise. To this end, two T-networks are implemented in the two feedback paths of the FDOA. The first T-networks is constructed by impedance $R_2$, capacitor $C_1$ and capacitance $C_P+C_X$. Where capacitance $C_X$ is the grounded offset-affected capacitance while $C_P$ represents all parasitic capacitance in parallel with $C_X$. Another T-network consists of resistance $R_2$, capacitor $C_1$ and a variable capacitance multiplier ($C_R$). The common-mode input voltage of the FDOA is roughly 0 V with an extra input common-mode feedback (ICMFB) pair. So that when calculating the current flowing through $R_1$, it can be assumed that the input voltage of the FDOA is virtual ground.

The AFE circuit is excited by a sinusoidal signal source $v_s$, where $v_s = V_M \sin \omega t$ and the current generated after it flows through the resistor $R_1$ is:

$$i_s = \frac{v_s}{R_1} \quad (1)$$

Thus, the voltage generated on capacitance $V_X$ and parasitic capacitance $C_P$ is given by Eq. (2).

$$v_o = -\frac{v_sR_2}{R_1} \quad (2)$$

Due to symmetry, the voltage on the capacitance $C_R$ is equal to $V_X$. As a result, the positive output voltage of the FDOA can be obtained as Eq. (3).

$$v_x = -\frac{v_sR_2\left[j\omega C_1 + j\omega (C_P + C_X) + \frac{1}{R_2}\right]}{R_1j\omega C_1} \quad (3)$$

Similarly, the negative output voltage of the FDOA can be obtained and its expression can be written as Eq. (4).

$$v_y = -\frac{v_sR_2\left(j\omega C_1 + j\omega C_R + \frac{1}{R_2}\right)}{R_1j\omega C_1} \quad (4)$$

Then $v_x$ and $v_y$ are given to the instrumentation amplifier (INA) and the output voltage of the INA can be written as Eq. (5).

$$v_o = \frac{Av_sR_2(C_P - C_R + C_X)}{R_1C_1} \quad (5)$$

Where $A$ represents the gain of INA. It can be seen from Eq. (5) that the output of INA is related to several variables such as $C_P$, $C_R$ and $C_X$. The adverse effects of the parasitic capacitance can be eliminated simply by setting $C_R = C_P$. Then, Eq. (5) will get modified as Eq. (6).

$$v_o = \frac{Av_sR_2C_X}{R_1C_1} \quad (6)$$

As can be seen from Eq. (6), the output of INA is linear with respect to the capacitance $C_X$, successfully eliminating the influence of the offset capacitance.

3. Circuit implementation

3.1 Fully differential operational amplifier

In order to obtain a relatively stable input common-mode voltage, the FDOA employs a common-mode feedback (CMFB) loop at its input, rather than its output, which is simply implemented by adding two extra PMOS transistors to a folded-cascode fully differential amplifier [27]. As shown in Fig. 2, both the input signal path and the CMFB loop are designed to have approximately the same loop gain and bandwidth, thereby ensuring that the interface is a virtual ground for both differential and common-mode signals.

3.2 Variable capacitor multiplier

Since the parasitic capacitance will change with the application environment, in order to adapt the CDC circuit to different application environment, it is necessary to generate a varying capacitance $C_R$ to cancel out the corresponding $C_P$. Therefore, a variable capacitance multiplication circuit [28] is introduced in this design, which can achieve a larger capacitance value through a smaller capacitor, thereby reducing the chip area, simultaneously.

As shown in Fig. 3, the variable capacitance multiplier consists of two operational amplifiers (OA), a smaller capacitor $C_{MR}$, and two variable resistors $R_4$ and $R_5$. Assuming
that the current flowing through resistors \( R_a \) and \( R_b \) is \( I_0 \), the voltage across \( C_{MR} \) is obtained as follows.

\[
V_{CMR} = I_0(R_a + R_b)
\]

(7)

The equivalent capacitance seen from point A to ground is \( C_R \), shown in Fig. 3, then Eq. (8) can be obtained from the charge equivalent theory.

\[
C_R I_0 R_b = C_{MR} I_0 (R_a + R_b)
\]

(8)

So the equivalent capacitance value is written as Eq. (9).

\[
C_R = \frac{1 + \frac{R_a}{R_b}}{C_{MR}}
\]

(9)

As can be seen from Eq. (9), a variable capacitance can be obtained by adjusting the values of the variable resistors \( R_a \) or \( R_b \).

### 3.3 Noise-shaping SAR ADC

Among all kinds of analog-to-digital structures, delta-sigma ADC can achieve high conversion accuracy due to the oversampling and noise-shaping techniques. SAR ADC has the advantages of low power consumption, simple structure and good process evolution. Therefore, combining oversampling and noise-shaping techniques with SAR ADCs can achieve a good compromise between power consumption, conversion accuracy and design complexity.

In this paper, a zero-pole optimized passive noise-shaping SAR ADC is used to improve the Signal-to-Noise-Distortion Ratio (SNDR) and Spurious-Free Dynamic Range (SFDR) while reducing the capacitance area and the power consumption of the comparator.

The architecture of the Noise-Shaping SAR ADC and its time diagram are shown in Fig. 4. The NS-SAR ADC includes Capacitive Digital-to-Analog Converter, the passive integrator, the comparator and the SAR logic.

Fig. 5 shows the passive gain realization and residue integration process. In residue integration phase \( \phi_1 \) of the cycle n-1, the residue voltage \( V_{res}(n-1) \) will be doubled by passive addition technique. Meanwhile, the CDAC capacitor \( C \) is connected to the parallel capacitor \( 2C \). The residue integration is executed as Eq. (10).

\[
2C \cdot V_{res}(n-1) + 4C \cdot V_{int}(n-1) = 5C \cdot V_{int}(n)
\]

(10)

The z-domain integration can be expressed as:

\[
V_{int}(z) = \frac{0.4 \cdot V_{res}(z)}{1 - 0.8z^{-1}}
\]

(11)

The conversion process of the NS-SAR is shown in Fig. 6. In the conversion phase \( \phi_c \) of the cycle n, the integrated voltage \( V_{int}(n) \) achieves 4 times the passive gain by splitting the capacitor \( 2C \) into four capacitors \( C/2 \) while the input voltage of the comparator is equal to \( V_{res}(n)+4V_{int}(n) \).

The signal flow diagram of the NS-SAR is shown in Fig. 7. From the signal flow diagram, the digital output can be expressed as Eq. (12).

\[
D_{out}(z) = V_{in}(z) + 4V_{int}(z) + Q(z)
\]

(12)

Combining Eq. (11) and Eq. (12), the transfer function of the NS-SAR can be derived as Eq. (13), which reflects that it has the effect of first-order noise-shaping.

\[
D_{out}(z) = \frac{V_{in}(z)}{1 + \frac{1 - 0.8z^{-1}}{0.8z^{-1}}}Q(z)
\]

(13)
4. Results and discussion

4.1 Accuracy and linearity
The proposed CDC circuit was designed and implemented using a 0.18 μm CMOS process. Post layout simulation studies of the CDC circuit were conducted to test the functionality of the technique with a power supply of 1.8 V. Fig. 8 shows the layout of the CDC circuit with an area of 0.52 mm² excluding the interface pads. Different layout techniques such as the common-centroid technique were implemented for sensitive regions.

In order to verify the accuracy and linearity of the system, the offset capacitance $C_P$ was set to be 10 pF and $C_X$ was chosen from 1 fF to 1 pF in steps of 50 fF and the output voltage of the AFE was simulated, shown in Fig. 9. A sine waves of amplitude 1 V and frequency 5 KHz was used as the input excitation signal. In order to better observe the linearity of AFE, the linear fitting error was also shown in Fig. 9. The worst-case non-linearity observed in output, $V_o$, is about 1%.

Further, simulations were extended to verify the measurement accuracy of the capacitance. In the case where the parasitic capacitance is 10 pF, the output voltage of the AFE with $C_X$ from 1 fF to 10 fF was simulated. As shown in Fig. 10, the worst-case non-linearity at the output of the AFE appears at $C_X = 1$ fF, which is 0.086 mV. On the other hand, it can be seen from Fig. 10 that the output voltage difference between 1 fF and 1.1 fF is worst, which is 0.22 mV. Since the reference voltage of the subsequent noise-shaping SAR ADC is 1.8 V and its effective number of bits is approximately 14, the minimum conversion accuracy is $1.8 \, V/(2^{14}) \approx 0.1$ mV.

The fact that the minimum detection accuracy of the NS-SAR ADC is 0.1 mV indicates that the worst-case non-linearity does not exceed 0.1 mV, this error can be ignored by ADC. Therefore, in the subsequent calculation process, the results from the linear fitting can be utilized to approximate the value of the capacitance to be measured. In addition, the minimum difference of the output voltage corresponding to the two capacitors with a difference of 0.1 fF is 0.22 mV, which is greater than the minimum detection accuracy of the NS-SAR ADC, proving that the minimum detection accuracy of the CDC meets the requirement of 0.1 fF with a certain margin left.

4.2 Effect of capacitive offset
Simulation was also conducted for different offset capacitance. The subsection details obtained for various offset values [$C_P = 2$ pF, 10 pF, 50 pF, 100 pF] within the range of $C_X$ from 1 fF to 1 pF are shown in Fig. 11. It can be seen from the simulation results that in the range of 2 pF to 100 pF, the offset capacitance has almost no effect on the output voltage of the AFE, which proves that the variable capacitance $C_X$ generated by the variable capacitance multiplier circuit can well counteract the influence of the offset capacitance $C_P$.

4.3 Noise-shaping SAR ADC
The digital output of the NS-SAR ADC was subjected to
a fast Fourier change and the resulting output spectrum is shown in Fig. 12. From the figure, it can be seen that the frequency of the input signal is 5 KHz and the sampling clock frequency is 1 MHz. The Signal to Noise Distortion Ratio (SNDR) is 85 dB and the Effective Number of Bits (ENOB) can reach approximately 14 bits when the bandwidth of the input signal is 31.25 KHz and the oversampling rate is 16.

A performance summary and a comparison with several state-of-the-art interfaces are shown in Table I [29, 30]. As can be seen from the Table, on the basis of sacrificing a certain amount of power consumption, the proposed CDC circuit can get a higher ENOB in a larger parasitic range.

5. Conclusion

A novel linear CDC circuit with a capacitive offset elimination technique for grounded capacitive sensors is presented. The capacitive offset elimination technique is realized by the implementation of variable capacitance multiplier circuit. Due to the symmetrical design of the AFE circuit, the influence of non-ideal effects such as common mode noise is further reduced. This circuit can accept capacitive sensors with large offset capacitance and provides a digital output proportional to the variable capacitance. Simulation studies are performed to verify the performance of the proposed scheme and the results demonstrate that the worst-case capacitance error observed is less than 0.1 fF, while the parasitic capacitance varies from 2 pF to 100 pF, indicating that the proposed CDC can be used for grounded capacitive sensors with good performance.

Acknowledgments

Projected supported by the National Nature Science Foundation of China (No. 61974116).

References

[1] K.C. Baby and B. George: “A simple analog front-end circuit for grounded capacitive sensors with offset capacitance,” IEEE Instrumentation & Measurement Technology Conference (2013) (DOI: 10.1109/IMTC.2013.655638).
[2] B. Li, et al.: “A l pF-to-10 nF generic capacitance-to-digital converter using zero-crossing ΔΣ modulation,” IEEE Trans. Circuits Syst. I, Reg. Papers (2017) (DOI: 10.1109/TCSI.2017.2777872).
[3] B. Li, et al.: “A high-linearity capacitance-to-digital converter suppressing charge errors from bottom-plate switches,” IEEE Trans. Circuits Syst. I, Reg. Papers 61 (2014) (DOI: 10.1109/TCSI.2014.2298285).
[4] H.Y. Park, et al.: “A touch sensor readout circuit using switched-capacitor charge pump,” IEICE Electron. Express 9 (2012) (DOI: 10.1587/exle.9.1090).
[5] R. Yang and S. Nithianov: “A time/resistor-referenced sensor interface for displacement measurement in the sub-nanometer range,” IEEE International Symposium on Industrial Electronics (2013) (DOI: 10.1109/ISIE.2013.6563796).
[6] R. Lv, et al.: “A closed-loop ΔΣ modulator for micromechanical capacitive sensors,” IEICE Electron. Express 15 (2018) (DOI: 10.1587/exle.15.20171112).
[7] S.K. Kar, et al.: “A differential output interfacing ASIC for integrated capacitive sensors,” IEEE Trans. Instrum. Meas. (2017) (DOI: 10.1109/TIM.2017.2761238).
[8] F. Reverter, et al.: “A novel interface circuit for grounded capacitive sensors with feedforward-based active shielding,” Measurement Science & Technology 19 (2008) (DOI: 10.1088/0957-0233/19/2/025202).
[9] A.A. Bijargah, et al.: “An accurate and power-efficient period-modulator-based interface for grounded capacitive sensors,” International Journal of Circuit Theory and Applications (2019) (DOI: 10.1002/cta.2642).
[10] D. Marioli, et al.: “High-accuracy measurement techniques for capacitance transducers,” Measurement Science & Technology 4 (1993) (DOI: 10.1088/0957-0233/4/3/012).
[11] J. O’Dowd, et al.: “Capacitive sensor interfacing using sigma-delta techniques,” IEEE Sensors J. (2006) (DOI: 10.1109/ ICSENS.2005.1597858).
[12] X. Guo and S.N. Nithianov: “A capacitive sensing technique for measuring displacement with one floating target electrode,” IEEE International Conference on Industrial Technology (2010) (DOI: 10.1109/ICIT.2010.5472457).
[13] F. Aezinia and B. Bahreyni: “A readout circuit with wide dynamic range for differential capacitive sensing applications,” 26th IEEE Canadian Conference on Electrical and Computer Engineering (2013) (DOI: 10.1109/CCECE.2013.657799).
[14] A. Alhoshany, et al.: “A 45.83/Step, energy-efficient, differential SAR capacitance-to-digital converter for capacitance sensing,” Sensors and Actuators A: Physical 245 (2016) (DOI: 10.1016/j.sna.2016.04.038).
[15] Y. Wang and V. Chodavarapu: “Differential wide temperature range CMOS interface circuit for capacitive MEMS pressure sensors,” Sensors 15 (2015) (DOI: 10.3390/s150204253).
[16] W.C. Haase: US Patent 6703932 B2 (2004).
[17] Q. Jia, et al.: “An integrated interface for grounded capacitive sensors,” IEEE Sensors J. (2005) (DOI: 10.1109/ ICSENS.2005.1597890).
[18] A. Heidary: “A low-cost universal integrated interface for capacitive sensors,” Ph.D. Dissertation, Delft University of Technology (2010) (DOI: urn:nbn:nl:ui:2013103036).
[19] A.A. Bijargah, et al.: “Design trade-offs of a capacitance-to-voltage converter with a zoom-in technique for grounded capacitive sensors,” International Journal of Circuit Theory and Applications (2018) (DOI: 10.1002/cta.2557).
[20] K.C. Baby and B. George: “A capacitive ice layer detection system suitable for autonomous inspection of runways using an ROV,” IEEE International Symposium on Robotic and Sensors Environments (ROSE) (2012) (DOI: 10.1109/ROSE.2012.6402627).
[21] B. George, et al.: “A warning system for chainsaw personal safety based on capacitive sensing,” IEEE Sensors J. (2008) (DOI: 10.1109/ICSENS.2008.4716467).

[22] I.-S. Yang and O.-K. Kwon: “A touch controller using differential sensing method for on-cell capacitive touch screen panel systems,” IEEE Trans. Consum. Electron. 57 (2011) (DOI: 10.1109/TCE.2011.6018851).

[23] H.-R. Kim, et al.: “A mobile-display-driver IC embedding a capacitive-touch-screen controller system,” IEEE Solid-State Circuits Conference Dig. Tech. Papers (2010) (DOI: 10.1109/ISSCC.2010.5434080).

[24] Y. He, et al.: “A 0.05mm² 1V capacitance-to-digital converter based on period modulation,” 2015 IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers (2015) (DOI: 10.1109/ISSCC.2015.7063138).

[25] A. Heidary, et al.: “An integrated interface circuit with a capacitance-to-voltage converter as front-end for grounded capacitive sensors,” Measurement Science & Technology 20 (2009) (DOI: 10.1088/0957-0233/20/1/015202).

[26] Y. Jung, et al.: “A 17.4-b delta-sigma capacitance-to-digital converter for one-terminal capacitive sensors,” IEEE Trans. Circuits Syst. II, Exp. Briefs 64 (2017) (DOI: 10.1109/tcssi.2015.2505960).

[27] S. Xia, et al.: “A capacitance-to-digital converter for displacement sensing with 17b resolution and 20μs conversion time,” IEEE International Solid State Circuits Conference Dig. Tech. Papers (2012) (DOI: 10.1109/ISSCC.2012.6176973).

[28] National Semiconductor: “LM101a/LM201a/LM301a operational amplifiers” (1999).

[29] A.K. George, et al.: “A 0.8 V supply- and temperature-insensitive capacitance-to-digital converter in 0.18-μm CMOS,” IEEE Sensors J. 16 (2016) (DOI: 10.1109/jSEN.2016.2559164).

[30] H. Omran, et al.: “A 33fJ/step SAR capacitance-to-digital converter using a chain of inverter-based amplifiers,” IEEE Trans. Circuits Syst. I, Reg. Papers 64 (2017) (DOI: 10.1109/tcisi.2016.2608905).