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Accurate and Efficient Dynamic Simulations of Ferroelectric Based Electron Devices

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I. INTRODUCTION

In recent years electron devices based on ferroelectric materials have attracted a lot of interest well beyond FeRAM memories. Negative capacitance transistors (NC-FETs) have been investigated as steep slope transistors [1], [2], and Ferroelectric FETs (Fe-FETs) are under intense scrutiny also as synaptic devices for neuromorphic computing, where the minor loops in ferroelectrics can allow to achieve multiple values of conductance in read mode [3], [4], [5]. Furthermore, the persistence of ferroelectricity in ultra-thin ferroelectric layers paved the way to ferroelectric tunnelling junctions [6], where a polarization dependent tunneling current can be exploited to realize high impedance memristors, amenable for ultra-power-efficient and thus massive parallel computation.

In all the above devices the dynamics of ferroelectric domains must be solved self-consistently with the device electrostatics. Furthermore, in MOS transistors having a semiconductor channel, the semiconductor introduces a strong non linearity in the electrostatics, and consequently in the dynamic equations describing the ferroelectric device evolution. The defects at the interfaces also play an intriguing role in ferroelectric FETs [7], in contrast to the well established and detrimental effects in conventional FETs [8]. Moreover, the presence of different trap levels imply a large range of charging and discharging time constants, possibly very different compared to the ferroelectric time constants.

In this paper we compare different numerical integration methods to achieve an accurate and effective simulation of NC-FETs, where the dynamics is governed by possibly very different time constants for either the ferroelectric or interface traps.

II. MODEL DESCRIPTION AND NUMERICAL ALGORITHMS

In the multi-domain, time-dependent Landau-Khalatnikov Equations (LKE) the description of ferroelectric domains requires the numerical solution of a set of differential equations for the polarization \( P_i \) of the \( i \)-th domain that read [9], [2]

\[
\frac{dP_i}{dt} = -(a_i P_i + b_i P_i^3 + c_i P_i^5) + V_{fe,i} \rho P_i + k \sum_j (P_j - P_i) \quad (1)
\]

where \( \rho \) is a resistivity associated to domain switching, \( k \) is a coupling factor between nearest neighbor domains and \( V_{fe,i} \) is the ferroelectric voltage drop for the \( i \)-the domain. The ferroelectric parameters were calibrated by comparing to experiments in [10], and the resulting set is [2] \( a = -9.5 \times 10^{-8} \text{ m/F}, b = 2.01 \times 10^{10} \text{ m}^5/\text{F}/\text{C}^2, c = 5.11 \times 10^{10} \text{ m}^9/\text{F}/\text{C}^4 \). When the ferroelectric is operated at small \( P \) (e.g. in NC-FETs), the linear term in Eq. (1) is dominant and a time constant \( \tau_{fe} = \rho |a| \) is readily identified, which is a property of the ferroelectric material.

Our analysis will be focused on an \( n \)-type, double-gate ultra-thin body (DG-UTB), nanoscale NC-FET (see Fig.1(a)), and a single domain analysis is used because the channel length is comparable to the size of ferroelectric domains [11]. Current is calculated with a simple ballistic top-of-the-barrier (ToB) model [12], [13], where electrons at the ToB with positive and negative velocity are taken to be in equilibrium with respectively the source, \( E_{f,s} \), and drain Fermi level \( E_{f,d} = (E_{f,s} - q V_{DS}) \) [12].

Quantization in the semiconductor is described with a 1D, parabolic effective mass Schrödinger solver, with valley multiplicities, and effective masses corresponding to a [100] silicon interface [14]. The link between the semiconductor and dielectrics is given by continuity conditions for the electric displacement at the interfaces; more modelling details may be found in [15].

We included in our analysis acceptor-type traps in the upper half of the silicon energy gap (see Fig. 1(b)), which exchange electrons with the conduction band with an emission, \( e_n \), and...
capture rate \( c_n \). The continuity equation for the carrier density \( n_T \) in traps with energy \( E_T \) can be written as [16]
\[
\rho \frac{\partial n_T}{\partial t} = c_n (N_T - n_T) - e_n n_T
\]
(2)
where \( N_T \) is the trap density at energy \( E_T \), and
\[
e_n = \sigma v_{th} N_C \exp[(E_T - E_C)/(K_B T)]
\]
(3a)
\[
e_n = \sigma v_{th} N_C \exp[(E_f - E_C)/(K_B T)]
\]
(3b)
with \( E_C \) and \( E_f \) being the conduction band edge and local Fermi level, and \( \sigma, v_{th}, N_C \) denoting respectively the trap cross-section, thermal velocity and conduction band effective density of states. For any trap energy \( E_T \), we solve Eq. (2) self-consistently with the ferroelectric dynamics governed by Eq. (1), in fact the charge in the traps \( Q_i = -q \sum_{E_T} n_T(E_T) \) influences the overall electrostatics in the gate stack and thus across the ferroelectric.

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\[
|\phi_{\delta t} - \phi_{10fs}| := max (|\phi_{\delta t} - \phi_{10fs}|)
\]
(4)
where the potential calculated for \( \delta t=10fs \) was used as the reference. However Fig.3 also shows that the explicit integrator becomes unstable for time steps larger than those needed to produce an error of 0.2mV. In other words, the explicit method is forced to continue using very small time steps and producing a small error even when larger errors would be acceptable. On the other hand the implicit integrator does not have stability problems, not even when using larger time steps when targeting larger values of the error in exchange for faster simulation times. For instance, if an error of 1mV is considered acceptable by the user, the implicit integrator could solve the problem in just 3 minutes while the explicit integrator would still be forced to require more than 4 hours to solve the problem to avoid numerical instability.

Fig.4 reports the simulated \( I_{DS-VG} \) curve and for two frequencies of the triangular gate voltage waveform. A few periods of the \( V_G \) input waveform were simulated and we verified that the \( I_{DS} \) becomes periodic after the first two or three periods, so that the \( I_{DS-VG} \) curve plot can be obtained by taking the corresponding \( I_{DS} \) and \( V_G \) values in the last period of the \( V_G \) waveform. The results obtained with explicit and implicit methods are compared at two time steps, demonstrating a remarkable speed-up of the
Fig. 4: Comparison of $I_{DS}$-$V_G$ characteristics at different frequencies and for two integration methods. The curves are obtained with a uniform trap density $D_{it}=10^{13}$ cm$^{-2}$/eV, the LKE coefficients reported in Fig.2 and for a $\rho=0.5\Omega$m. The curves obtained with the different integration methods are almost indistinguishable, but the speedups are consistent with the ones reported in Fig.3.

Fig. 5: Occupation probability $P_t=n_t/N_t$ for two trap levels (in midgap position and closer to the conduction band) corresponding to the $f=500$MHz curve in Fig.4 and for three integration time-steps $\delta_t$; the $V_G$ input waveform is also shown (right y axis). $\Delta E_T=E_C-E_T$ is the distance between the energy level of the trap and the conduction band at the semiconductor-dielectric interface.

Fig. 6: Total simulation time (for one period of the input signal and for $f=5$MHz) versus the relative error on the current $I_{DS}$ for the implicit integrator; the reference used to calculate the error is the simulated current at $\delta t=10$fs. We here label as on- and off-state current the $I_{DS}$ at respectively $V_G=0.25$ V and $V_G=-0.3$ V (see also the $I_{DS}$ versus $V_G$ characteristics in Fig.4).

In summary, in this work we systematically demonstrated the advantages of an implicit trapezoidal integrator with respect to a explicit Runge-Kutta method for the simulation of NC-FETs having a wide range of time constants set either by the ferroelectric or by the interface traps dynamics. Advantages are observed in terms of robustness of convergence and in terms of simulation time at fixed accuracy. Our results are expected to be useful in the development of robust TCAD tools for ferroelectric based devices, that are important for the design and optimization of ferroelectric FETs and ferroelectric tunnelling junctions. The growing interest for negative capacitance, steep slope FETs and ferroelectric based synaptic devices for neuromorphic computing will make the modeling and simulation of ferroelectric devices a topic of increasing technological relevance in the near future.
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