Compensation of Reconstruction Filter Effect in Digital Signal Processing System

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Abstract This paper proposes the reduction effect of reconstruction filter for digital signal processing system. It is well known that the reconstruction filter limits the bandwidth of output signal processing and the output signal is staircase form or has high frequency components. For effect reduction we use the nonrecursive system which corresponds with the inverse system function of the reconstruction filter. The initial step starts with the analog system function of the reconstruction filter and is converted to a discrete-time system using the approximation of derivative technique and inverse system. This inverse discrete-time system function is a nonrecursive system to compensate the reduction effect of the reconstruction filter implemented by using the software. For hardware experiments, we use TMS320C31 digital signal processor, D/A, PIC-32 microcontroller, PWM analog output. The experimental results of the proposed principle show that it can be used to compensate the bandwidth and reduce the total harmonic distortion (THD) of high frequency signal. In addition, this experiment shows that the nonrecursive system for compensation uses only first-order system and it does not utilizes any more processor. Furthermore, it is able to increase the performance. The applications are such as digital filtering, digital control and audio processing. They can be done with high accuracy using the proposed principle.

Keywords: reconstruction filter, nonrecursive system, approximation of derivative, pulse width modulator, total harmonic distortion

1. Introduction

The digital signal processing systems include the input filter or anti-aliasing filter, analog to digital converter (A/D), digital processor, digital to analog converter (D/A) and output filter or reconstruction filter [1-4], some cases, the hardware of analog signal output of the digital signal processing system may be changed from D/A to PWM (pulse width modulator) in order to reduce the size of hardware implementation. In practice, the bandwidth of system is limited by anti-aliasing filter, D/A sampling property and reconstruction filter [5]. The anti-aliasing filter is used to protect the high frequency while the frequency in the system is more than f/2. The attenuation of anti-aliasing filter happens because of the transition band at Nyquist frequency due to the anti-aliasing is not ideal, but it can be solved by increasing the order. The sampling D/A property could be solved by using the pre-equalizing or post-equalizing technique [6]. The pre-equalizing circuit is connected before the D/A stage, is implemented by using the finite impulse response filter (FIR) with higher order and the post-equalizing technique uses the analog active filter circuit and it is connected after reconstruction filter stage. However, the bandwidth at output of D/A is compensated with both methods and limited by the reconstruction filter. If the cut-off frequency of reconstruction filter is Nyquist frequency, the signal will be attenuated; especially the signal frequencies near the Nyquist frequency. In addition, if the cut-off frequency is more than the Nyquist frequency, the output signal will be distorted due to the result of total harmonic distortion (THD). The reason for this problem is that reconstruction filter is not an ideal lowpass filter and has the transition band.

To solve the attenuation problem at high frequency, it is possible to increase the order of the reconstruction filter. To increase the order of the reconstruction filter, it requires a lot of analog hardwares. In the other hand, we can delete the reconstruction filter which signal is not be attenuated and the output signal is non-smooth or in staircase form. In order to solve the problem, this paper proposes a new method for bandwidth compensation of the digital signal processing at high frequency caused from reconstruction filter by using a nonrecursive system. The nonrecursive system will ensure a stable system because it has all pole positions...
at the origin inside the unit circle and it is easy to implement by using floating point or fixed point processor [2].

2. Conventional Principle

The complete digital signal processing system is shown in Fig. 1. The output signal \( y(t) \) from a digital signal processor is converted to be analog signal \( y(t) \) by using D/A circuit and passes through to the reconstruction filter [4]. The reconstruction filter reduces the step signal and the cut-off frequency is \( f_c/2 \). It has a problem near the Nyquist frequency due to the transition band of reconstruction filter. To solve the attenuation, it is able to change the cut-off frequency of reconstruction filter to be higher than the Nyquist frequency. It makes a wide passband and the signal is staircase form because of the filter cannot eliminate the high frequency component of output signal.

The digital signal processing system operates at 15.9 kHz sampling frequency and it affects clearly the reconstruction filter. To select the first-order of passive reconstruction filter which has 1kHz cut-off frequency, the system samples the sinusoidal signal from A/D through D/A. The analog output signal with reconstruction filter and without reconstruction filter is shown in Fig. 2. At 1 kHz frequency, the amplitude of the analog signal with the reconstruction filter is attenuated and the output signal without the reconstruction filter is slightly attenuated due to the D/A with zero-order hold circuit [6]. The magnitude response of D/A with zero-order hold circuit is Sinc envelope as shown in Fig. 3.

To reduce the effect of Sinc envelope of D/A by using the pre–equalizing filter and post-equalizing filter reported in [6]. The pre–equalizing filter is implemented by using FIR filter with inversing Sinc frequency response and the post-equalizing filter has been implemented by using the high-order analog filter.

As the applications, the highpass filter, notch filter and allpass filter will be affected by the reconstruction filter because the property of a reconstruction filter is a lowpass filter. The digital notch filter operating at 1kHz notch filter and 15.9kHz sampling frequency and the reconstruction filter has been implemented with the first-order lowpass filter operating at 1kHz cut-off frequency.

The magnitude response of the digital notch filter will be attenuated at high frequency by the reconstruction filter as shown in Fig. 4. The magnitude of the digital notch filter has error at high frequency; especially it is similar to the magnitude response of the first-order lowpass filter or reconstruction filter.

![Fig. 1 Diagram of conventional digital signal processing system](image)

![Fig. 2 Analog output signal with/without the reconstruction filter](image)

However, the solution of Sinc envelope attenuation is presented in [6]. This paper proposes the attenuation of reconstruction filter. The hardware does not increase the system as the proposed technique uses the software technique. This software shares the processing with main processing and it also uses a short processing time.

3. Proposed Principle

Diagram of digital signal processing system with compensated reconstruction filter is shown in Fig. 5. The function of the nonrecursive system has to be opposite to the reconstruction filter and will be implemented by using the software. Figure 6 shows the reconstruction filter with the first-order analog lowpass filter. The compensated system is designed by using the inverse system of output filter (reconstruction filter) as shown in Fig. 5. Therefore, it might not be designed for the high-order. The attenuation of output filter is neglected from compensated system and the signal of D/A is flat with non-staircase. The compensated system by using anti-aliasing limits the system bandwidth.
In the design of compensated system function, the first step starts with the system function of the analog reconstruction filter; $H(s)$ in Fig.6 as shown in Eq. (1).

$$H(s) = \frac{1}{s + \frac{1}{RC}}$$

The analog function in Eq. (1) is continuous-time system and converted to be discrete-time system $H(z)$ by approximating the derivative principle [1, 3] as shown in Eqs. (2) and (3). The function $H(z)$ has a nonrecursive system property [1]. The transformation method of continuous-time system transforms to discrete-time system such as bilinear transform as presented in [2, 5]. The inverse system function is a recursive system. The recursive system has the pole positions which are not placed at the origin but it places at circular perimeter. Thus, the inverse of recursive system may be unstable.

$$s = \frac{1 - z^{-1}}{T}$$

The second step is to invert the system function in Eq. (3) to Eq. (4). The system function in Eq. (4) is stable because the system has the pole at origin inside the unit circle. Thus, the system function in Eq. (4) is a nonrecursive system [1].

$$H(z) = \frac{aT}{1 + aT - z^{-1}}$$

where $a = \frac{1}{RC}$ and T is sampling rate.

Define $Y_i(z)$ as output signal before the compensation and $Y_f(z)$ as output signal after the compensation. Equation (4) can be rewritten as in Eq. (5).

$$H_i(z) = \frac{Y_f(z)}{Y_i(z)} = \frac{1 + aT - z^{-1}}{aT}$$

The nonrecursive system function for reconstruction filter compensation in Eq. (5) has converted to a difference equation by inverting z-transform as shown in Eq. (6) and implemented by software using a digital processor as shown in Fig. (7).

$$y_n(n) = (1 + \frac{1}{aT})y_{i}(n) - \frac{1}{aT}y_{i}(n-1)$$

From Fig. (7), $y_i(t)$ is defined as D/A output signal or PWM and $y(t)$ as system output.
4. Design Example

Letting $C = 0.1 \ \mu F$ and $R = 1k \Omega$ in Fig. 6 the actual cut-off frequency of the reconstruction filter is 1.59kHz and the sampling frequency of system is 21.853kHz. Eq. (1) - Eq. (3), the discrete-time system function is shown in Eq. (7) and pole-zero plots are shown in Fig. 8.

$$H(z) = \frac{0.4572}{1.4572 - z^{-1}}$$

The pole-zero plots as shown in Fig. 8 illustrates the discrete-time system function of the reconstruction filter. From Eq. (7), $H(z)$ is converted to nonrecursive system as shown in Eq. (8) and the difference equation is shown in Eq. (9). The pole-zero plots of nonrecursive system is shown in Fig 9. Equation (9) will be converted by using software for digital signal processor to construct compensated reconstruction filter.

$$H_i(z) = \frac{1.4572 - z^{-1}}{0.4572}$$

$$y_4(n) = 3.1874y_3(n) - 2.1874y_3(n-1)$$
5. Experiments and Results

The experiments are divided into three parts:
A. Implementation of TMS320C31 floating point digital signal processor with D/A,
B. Implementation of PIC32 32-bit fixed point microcontroller with PWM,
C. Application to the digital notch filter implemented by using TMS320C31.

The hardwares in the experiments are TMS320C31 DSP starter kit [8-10], MAX-547 12 bits external D/A interface board with two passive reconstruction filters, arbitrary function generator Tektronix AFG 320 and digital oscilloscope Tektronix TDS-3014. The A/D converter is a TLC32040 [9] with 14 bits resolution on DSP board and the TMS320C31 digital signal processor operating at 21.853kHz sampling frequency. Figure 10 shows the input signal \( x(t) \), output signal from D/A without the reconstruction filter, output signal with the reconstruction filter, output signal with the reconstruction filter and amplitude compensation are connected to oscilloscope channels 1, 2, 3 and 4, respectively. The application software is unity gain amplifier in order to obtain \( y(t) = x(t) \), and the results for two kinds of cut-off frequencies (1kHz and 1.59kHz) are compared. The frequency of the input signal is varied from 50Hz to 2kHz. The resulting signals from the experiments are shown in Figs. 11 and 12, and the magnitude response with/without amplitude compensation is shown in Fig. 13.

5.1 Implementation of TMS320C31 with D/A output

The diagram of experiments is shown in Fig. 10.

![Implementation diagram of TMS320C31 with D/A](image)

The distortions of the output signal of the proposed principle are compared in term of total harmonic distortion (THD) [7] using the input signal, output signal without the reconstruction filter and output signal and also with the reconstruction filter without compensation. All measurements of the THD in this experiment are measured by using a dynamic signal analyzer Agilent 35670A, and the THD measurement in each frequency (50Hz – 2kHz) contains the distortion at the fundamental frequency and the 2nd to 20th harmonic frequencies as shown in Table 1. The measured THD of signal by using the dynamic signal analyzer may be erroneous because the frequency component may not match with the 2nd to 20th harmonic frequencies.

| Frequency (Hz) | Signal generator (THD) | D/A output without the reconstruction filter | The 1 kHz cut-off frequency of reconstruction filter | The 1.59 kHz cut-off frequency of reconstruction filter |
|---------------|------------------------|---------------------------------------------|---------------------------------|---------------------------------|
|               |                        | without compensation | with compensation | without compensation | with compensation |
| 50            | 0.0384                 | 0.0996                    | 0.0831                  | 0.0934                  | 0.0924                  | 0.0874                  |
| 100           | 0.0381                 | 0.0909                    | 0.0829                  | 0.0841                  | 0.0739                  | 0.0758                  |
| 200           | 0.0322                 | 0.0861                    | 0.0641                  | 0.0657                  | 0.0685                  | 0.0732                  |
| 300           | 0.0341                 | 0.0865                    | 0.0529                  | 0.0607                  | 0.0584                  | 0.0707                  |
| 400           | 0.0338                 | 0.0881                    | 0.0479                  | 0.0587                  | 0.0523                  | 0.0650                  |
| 500           | 0.0337                 | 0.0878                    | 0.0421                  | 0.0582                  | 0.0493                  | 0.0592                  |
| 600           | 0.0341                 | 0.0871                    | 0.0376                  | 0.0585                  | 0.0447                  | 0.0575                  |
| 700           | 0.0340                 | 0.0887                    | 0.0355                  | 0.0593                  | 0.0431                  | 0.0588                  |
| 800           | 0.0340                 | 0.0922                    | 0.0334                  | 0.0573                  | 0.0403                  | 0.0559                  |
| 900           | 0.0347                 | 0.0965                    | 0.0311                  | 0.0550                  | 0.0397                  | 0.0573                  |
| 1000          | 0.0341                 | 0.1019                    | 0.0310                  | 0.0540                  | 0.0365                  | 0.0532                  |
Table 1 (Continued) Total harmonic distortion of signal at output of D/A

| Frequency (Hz) | Signal generator (THD) | D/A output without the reconstruction filter | The 1 kHz cut-off frequency of reconstruction filter with compensation | The 1.59 kHz cut-off frequency of reconstruction filter with compensation |
|---------------|------------------------|---------------------------------------------|---------------------------------------------------------------------|---------------------------------------------------------------------|
|               |                        |                                              | without compensation                                                | with compensation                                                   |
| 1100          | 0.0344                 | 0.1265                                       | 0.0342                                                              | 0.0342                                                              |
| 1200          | 0.0344                 | 0.0921                                       | 0.0311                                                              | 0.0311                                                              |
| 1300          | 0.0340                 | 0.1001                                       | 0.0285                                                              | 0.0449                                                              |
| 1400          | 0.0335                 | 0.0941                                       | 0.0301                                                              | 0.0434                                                              |
| 1500          | 0.0335                 | 0.0937                                       | 0.0273                                                              | 0.0422                                                              |
| 1600          | 0.0338                 | 0.0990                                       | 0.0272                                                              | 0.0407                                                              |
| 1700          | 0.0337                 | 0.0934                                       | 0.0266                                                              | 0.0389                                                              |
| 1800          | 0.0321                 | 0.1128                                       | 0.0381                                                              | 0.0487                                                              |
| 1900          | 0.0377                 | 0.1354                                       | 0.0318                                                              | 0.0335                                                              |
| 2000          | 0.0377                 | 0.0988                                       | 0.0273                                                              | 0.0339                                                              |
| Average       | 0.0342                 | 0.0977                                       | 0.0402                                                              | 0.0539                                                              |

5.2 Implementation of PIC32 with PWM output

The diagram of experiment is shown in Fig. 14.

![Diagram of implementation of PIC32 microcontroller with PWM](image)

The hardwares in this experiment are the PIC-32MX460512L 32-bit microcontroller [11, 12] with 10-bit A/D, 5-channels pulse width modulator (PWM), two passive circuit reconstruction filters as external interface, arbitrary signal generator and TDS-3014 digital oscilloscope. The A/D of PIC-32 microcontroller operates at 4 kHz sampling frequency, and the PWM is 10-bit resolution and operates at 44.1kHz pulse width frequency. The input signal $x(t)$ must be added to the offset voltage because the A/D of PIC-32 microcontroller has 0-3.3V input voltage range. The input signal, the output signal from PWM, the output signal from PWM with the reconstruction filter and the amplitude compensation, the output signal from PWM with the reconstruction filter, are all connected to oscilloscope channel 1, 2, 3 and 4, respectively. The cut-off frequencies of the reconstruction filter are 500Hz and 800Hz with defining as $y(t) = x(t)$. The frequency of input signal starts at 50Hz and varies to 1kHz. The results of the experiment are shown in Figs. 15 and 16. The magnitude response with/without amplitude compensation is shown in Fig. 17. The total harmonic distortion of signal is shown in Table 2.

5.3 Application to digital notch filter

The experiment in this section uses the same hardwares as in part 5.1. The digital notch filter operates at 1 kHz notch frequency and 15.9kHz sampling frequency. The design method of the digital notch filter is presented in [13, 14], and the system function of the digital notch filter is shown in Eq. (10). The magnitude response of the digital notch filter with/without the bandwidth compensation and taken by the dynamic signal analyzer 35670A are shown in Figs. 18 and 19, respectively.

$$H(z) = \frac{0.99005 - 1.8283z^{-1} + 0.99005z^{-2}}{1 - 1.8283z^{-1} + 0.9801z^{-2}}$$

(10)
Fig. 11 Results of signals with 1kHz cut-off frequency of the reconstruction filter by varying the input signal frequency as 50Hz, 100Hz, 500Hz, 1kHz, 1.5kHz and 2kHz
CH 1: Input signal
CH 2: Output signal from D/A without the reconstruction filter
CH 3: Output signal from D/A with the reconstruction filter
CH 4: Output signal from D/A with the reconstruction filter and amplitude compensation
Fig. 12 Results of signals with 1.59kHz cut-off frequency of the reconstruction filter by varying the input signal frequency as 50Hz, 100Hz, 500Hz, 1kHz, 1.5kHz and 2kHz
CH 1: Input signal
CH 2: Output signal from D/A without the reconstruction filter
CH 3: Output signal from D/A with the reconstruction filter
CH 4: Output signal from D/A with the reconstruction filter and amplitude compensation
Fig. 13 Magnitude response of the conventional principle (without compensation) versus the proposed principle (with compensation)

Table 2 Total harmonic distortion of signal at PWM output

| Frequency (Hz) | Signal generator (THD) | The 500 Hz cut-off frequency of reconstruction filter | The 800 Hz cut-off frequency of reconstruction filter |
|---------------|------------------------|----------------------------------------------------|----------------------------------------------------|
|               |                        | without compensation | with compensation | without compensation | with compensation |
| 50            | 0.0422                 | 0.0601                | 0.1678             | 0.6523                | 0.7216             |
| 100           | 0.0348                 | 0.0593                | 0.1786             | 0.5338                | 0.7042             |
| 200           | 0.0353                 | 0.0897                | 0.1792             | 0.4141                | 0.6321             |
| 300           | 0.0361                 | 0.2271                | 0.4168             | 0.3559                | 0.5824             |
| 400           | 0.0425                 | 0.3740                | 0.7301             | 0.3070                | 0.5751             |
| 500           | 0.0355                 | 0.4685                | 1.0073             | 0.2723                | 0.5778             |
| 600           | 0.0460                 | 0.4406                | 1.1423             | 0.2414                | 0.5970             |
| 700           | 0.0368                 | 0.3771                | 0.9024             | 0.2497                | 0.5922             |
| 800           | 0.0372                 | 0.3167                | 0.9930             | 0.2734                | 0.6629             |
| 900           | 0.0378                 | 0.2988                | 0.8916             | 0.2759                | 0.6949             |
| 1000          | 0.0452                 | 0.3048                | 0.8811             | 0.2912                | 0.7308             |
| **Average**   | **0.0390**             | **0.2742**            | **0.6809**         | **0.3515**            | **0.6428**         |
Fig. 15 Results of signals with 500Hz cut-off frequency of the reconstruction filter by varying the input signal frequency as 50Hz, 100Hz, 200Hz, 500Hz, 800Hz, and 1kHz

CH 1: Input signal
CH 2: Output signal from PWM
CH 3: Output signal from PWM with the reconstruction filter and amplitude compensation
CH 4: Output signal from PWM with the reconstruction filter.
(a) 50Hz (b) 100Hz
(c) 200Hz (d) 500Hz
(e) 800Hz (f) 1kHz

Fig. 16 Results of signals with 800Hz cut-off frequency of the reconstruction filter by varying the input signal frequency as 50Hz, 100Hz, 200Hz, 500Hz, 800Hz, and 1kHz

CH 1: Input signal
CH 2: Output signal from PWM
CH 3: Output signal from PWM with the reconstruction filter and amplitude compensation
CH 4: Output signal from PWM with the reconstruction filter
(a) 500Hz cut-off frequency of the reconstruction filter

(b) 800Hz cut-off frequency of the reconstruction filter

Fig. 17 Magnitude response of the conventional principle (without compensation) versus the proposed principle (with compensation)

Fig. 18 Magnitude response of digital notch filter without bandwidth compensation

Fig. 19 Magnitude response of notch filter with bandwidth compensation
6. Conclusions

The results of the compensated reconstruction filter in digital signal processing system using a nonrecursive system according to the proposed principle show that the used D/A hardware is not attenuated and smooth (or non-staircase) as the signal frequency increases. The results of PWM hardware are obviously shown to be the same as the D/A hardware output, although the PWM signal is very different from the sinusoidal signal. The results of signal distortion are shown in Tables 1 and 2. From Table 1, the D/A output signal without the reconstruction filter has more the higher THD than with the reconstruction filter. The average of THD without compensation is less than with compensation because the compensation technique increases the gain at high frequency which also amplifies the harmonics of output signal and the THD at high frequency decreases the harmonic due to transition band of reconstruction filter.

Although, both have low THD, without compensation method attenuates the amplitude at high frequency as shown in Fig. 13. In addition, at 1 kHz and 1.59kHz cut-off frequency of reconstruction filters show that the 1kHz cut-off frequency has the lower THD than at 1.59kHz cut-off frequency.

The results in Table 2 are similar to Table 1. Thus, the reconstruction filter of the digital signal processing system should use a cut-off frequency less than $f_s/2$ for reducing the THD. The bandwidth is not affected because it can be compensated by using the proposed principle. The experiment reveals that the reconstruction filter compensation needs only the first-order hardware and software for implementation. The proposed technique does not use any more processors to increase the performance. As shown in 4.3, the magnitude response of the digital notch filter can be operated with high accuracy because the effects of the reconstruction filter are attenuated by the proposed principle.

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References

[1] J. G. Proakis and D. G. Manolakis: Digital Signal Processing Principle, Algorithms, and Applications, Prentice Hall, 1996.
[2] E. C. Ifeachor and B. W. Jervis: Digital Signal Processing: A Practical Approach, Addison Wesley, 1996.
[3] A. V. Oppenheim, R. W. Schafer and J. R. Buck: Discrete-Time Signal Processing, Prentice Hall, 1999.
[4] S. K. Mitra: Digital Signal Processing, A Computer-Based Approach, McGraw-Hill, 2001.
[5] S. J. Orfanidis: Introduction to Signal Processing, Prentice Hall, 1995.
[6] http://www.maximic.com/appnotes/index.mvp/id/3853.
[7] J. Mittal and B. S. Kumar: Total harmonic distortion measurement and establishment of traceability of distortion factor using attenuation standard and spectrum analyzer, No. EM 016, AdMet, 2012.
[8] TMS320C3x User’s Guide, Texas Instruments Inc., 1994.
[9] TMS320C3x DSP Starter Kit User’s Guide, Texas Instruments Inc., 1996.
[10] TMS320C3x/4x Optimizing C Compiler User’s Guide, Texas Instruments Inc., 1998.
[11] L. D. Jasio: Programming 32-bit Microcontrollers in C Exploring the PIC32, Elsevier, 2008.
[12] D. Ibrahim: Microcontroller-Based Applied Digital Control, John Wiley & Sons, 2006.
[13] S. Yimman and K. Dejhan: IIR multiple-notch filter design with optimum pole position, Journal of Signal Processing, Vol.12, No.2, pp.167-174, March 2008.
[14] S. Yimman, W. Hinjit, S. Sriboonsong, M. Puangpool and K. Dejhan: IIR notch filter design with modified pole-zero placement algorithm, Proc. of IEEE International Symposium on Signal Processing and Information Technology (ISSPIT 2003), pp. 822-825, Darmstadt, Germany, December 2003.

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