Microsecond Crystallization of Amorphous Silicon Films on Glass Substrates by Joule Heating

Won-Eui Hong\textsuperscript{a} and Jae-Sang Ro\textsuperscript{b,∗∗}

\textsuperscript{a}AP Group\textsuperscript{c} Team, Dawonsys Co., Gyeonggi-do 15655, Korea
\textsuperscript{b}Department of Materials Science and Engineering, Hongik University, Seoul 04066, Korea

Joule-heating-induced crystallization (JIC) of amorphous silicon (a-Si) films was conducted by applying an electric pulse to a conductive layer located beneath or above the films. Crystallization occurs across the whole substrate surface within a few tens of microseconds. The phase-transformation phenomena during the JIC process were detected electrically and optically by in-situ measurements of input voltage/current and normal reflectance at wavelength of 532 nm. We devised a method for the crystallization of a-Si films while preventing arc generation; this method consisted of pre-patterning an a-Si active layer into islands and then depositing a gate oxide and gate electrode. Electric pulsed was then applied to the gate electrode formed using a Mo layer. JIC-processed poly-Si thin-film transistors were fabricated successfully, and the proposed method was found to be compatible with the standard processing of coplanar top-gate poly-Si TFTs. The p-channel JIC poly-Si TFT with $W/L = 7 \mu m/7 \mu m$ exhibited a field effect mobility of 38.9 cm$^2$/V·s, a threshold voltage of $-2.8$ V, and a gate voltage swing of 0.35 V/dec.

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Experimental

The schematic diagram of the JIC process is shown in Fig. 1, where Joule heat was generated by applying a pulsed electric field to a conductive layer, used to raise the temperature of the silicon film to crystallization temperature. Here, we utilize a conductive Mo-layer located beneath the amorphous silicon film as a Joule-heating source for the JIC specimen. A SiO$_2$ layer with a thickness of 300 nm was formed on a 0.5 mm-thick glass substrate, using the plasma enhanced chemical vapor deposition (PECVD) method. A Mo thin film with a thickness of 100 nm, was deposited on the first dielectric layer by sputtering, and then a SiO$_2$ layer with a thickness of 300 nm was deposited there on using the PECVD method. Finally, an amorphous silicon thin film of thickness 50 nm was deposited on the second dielectric layer using the PECVD method again. Overall dimensional size of the specimen this study is $20 \times 30$ mm$^2$, where those of a process window and two electrodes at both edges of the process window are $20 \times 20$ mm$^2$ and $5 \times 20$ mm$^2$, respectively. Real-time measurements of the electric

[Image 410x65 to 548x112]

Figure 1. Schematic diagram for Joule-heating induced crystallization (JIC) process of amorphous silicon on glass backplane.
pulse inputs to the JIC specimen were carried out through the voltmeter and the ammeter (Tektronix TDS 2012B) connected to the electrodes of the specimen, as depicted in Fig. 1.

For in-situ observation of the JIC crystallization process, normal reflectances of the specimen during the JIC process were measured with a laser of wavelength 532 nm and a photo-sensor. Here, normal reflectances were measured through an optical system with optical fibers, a beam splitter, and lenses.

The structure and the process flow for fabricating JIC poly-Si TFTs is illustrated in Fig. 2. The substrates used were Corning 7059 glasses with dimensions of $20 \times 30 \times 0.7$ mm$^3$. First, plasma-enhanced chemical vapor deposition (PECVD) was used to form a SiO$_2$ buffer layer (the first dielectric layer) with a thickness of 500 nm on a glass substrate. Moreover, the PECVD method resulted in a 50-nm-thick a-Si thin film being deposited on the first dielectric layer. This a-Si film was patterned and dry-etched to form active islands before the deposition of a 120-nm-thick oxide as a gate insulator. A 150-nm-thick Mo layer was then deposited by sputtering to form the gate metal. This Mo layer was also used as a Joule-heat source for the crystallization of the a-Si films. An electric field was applied to a Mo film with dimensions of $20 \times 20$ mm$^2$ for 11 $\mu$s in order to crystallize the pre-patterned a-Si islands. Thereafter, the Mo layer was patterned and wet-etched to form a gate electrode. Self-aligned ion implantation was conducted to form a source/drain by using 30 keV B$^+$ ions at a dose of $1 \times 10^{15}$/cm$^2$. Activation annealing was performed at 450 C for 1 h by using a tube furnace in nitrogen ambient.

### Results and Discussion

In order to investigate kinetic paths of phase transformation encountered in the JIC process we fabricated the JIC samples as illustrated in Fig. 1. We changed the processing parameters under two nominal conditions of 1250 V for 18 $\mu$s and 500 V for 250 $\mu$s (625 V/cm for 18 $\mu$s and 250 V/cm for 250 $\mu$s), whose in-situ experimental input voltages and currents are given in Fig. 3. Comparison of shorter and longer pulse applications indicates that there is a dip in the voltage variation for the shorter one, which does not appear in the longer one. The existence of this dip implies that the phase transformations of...
amorphous silicon are different from each other, since such a sudden voltage drop is induced by a sudden change of electric resistance, which will be discussed later.

After the initial overshoot governed by the inductance of the electric circuit, the current was observed to decrease slightly until the end of the nominal period of 18 $\mu$s, followed by the final decay governed by the circuit capacitance. This current decrease might be caused due to the increase of electrical resistance of the Mo film during the heating process and the decrease of the input voltage. During the main process stage between the initial overshoot and final decay (from 7 $\mu$s to 18 $\mu$s), the ratio of voltage to current could be considered as the resistance of the Mo film, which tended to increase slightly. Since the electric resistance of Mo is approximately proportional to the temperature as described in Fig. 4, this increase of the electric resistance was due to the increase of the film temperature.

Figure 4 shows the variation of sheet resistances for Mo film as a function of temperatures. The sheet resistances of the specimen measured for temperatures ranging from 300 K to 550 K were higher than the bulk values of the Mo by around a factor of 1.1. Since the slopes of the resistances with temperature were very close to each other, however, it could be assumed that the difference in the resistances by 1.1 was due to additional resistances such as contact or other external resistances. The sheet resistances for high temperatures were extrapolated from the measured values.

Figure 5 compares the in-situ normal reflectances and temperatures of silicon films during the JIC process for nominal pulses of 1250 V for 18 $\mu$s and 500 V for 250 $\mu$s. While temperatures predicted using the longer pulse input are in good agreement with those from the experimental values estimated from the ratio of voltage to current shown in Fig. 5b, temperatures predicted for shorter pulse input start to deviate from the experimental values after 11 $\mu$s. This deviation does not imply the sudden change of temperatures during the short pulse application, but does indicate the sudden change of electric resistance of the specimen due to the melting of silicon, as discussed previously for the voltage dip appeared in Fig. 3a. For this shorter pulse application, the temperature increases steeply at the early stage and approaches a value limited by the melting point of silicon. At temperatures below the melting point of silicon the overall electric resistance of the JIC specimen is almost the same as that of Mo thin-film, since the resistance of solid-phases is much larger than that of Mo thin-film. At temperatures where silicon starts to melt, the dramatically reduced resistance of liquid-phase silicon must be considered to estimate the overall resistance of the specimen. Here, the compensation for the reduced overall resistance to estimate the experimental resistance has not been included, since this drop is one of evidences for the existence of liquid-phase silicon during the JIC process under the shorter pulse input condition.

For the longer pulse application this kind of voltage drop has not been found, since the temperatures do not reach the melting point of silicon, as shown in Fig. 5b. Furthermore, in-situ reflectances measured at wavelength of 532 nm indicate that the sudden increase for the shorter pulse application is due to the incipience of melting, which does not appear for the longer one. Therefore, we may understand that the process for the shorter pulse application undergoes the melting phenomenon, while that for longer one does not. The peaks observed at the beginning and the end of the JIC process are due to electromagnetic interference from power supply and thus are not to be meaningful.

The structure of the sample used in fabricating JIC poly-Si TFTs was a conductor/SiO$_2$/a-Si/SiO$_2$/glass sandwich structure, as shown in Fig. 2a. During electrical pulsing, the temperature of silicon films may approach or surpass their melting point, depending on the processing parameters such as power density and pulsing time. A-Si is transformed into poly-Si at temperatures near the melting point of silicon where it becomes a conductor. At this point, the system of interest attains a conductor/SiO$_2$/Si-conductor capacitor structure in which vertical generation of sparks may occur when the potential difference, $\Delta V$, as indicated in Fig. 6b, between the conductor and silicon exceeds the dielectric breakdown voltage of the SiO$_2$ insulator. This, in turn, is followed by the generation of an intense arc because of an open circuit that forms under the applied electric field.

Figure 6a shows the method for preventing arc generation during JIC. The silicon films are patterned into size-sized islands before crystallization by using electrical pulsing. As long as significant amounts of free carriers are not generated in the intrinsic silicon films at relatively low temperatures during the JIC process, equal potentials will be preserved between the conductor and silicon films in both the structures shown in Fig. 6a.
a-Si films are transformed into conductive poly-Si at high temperatures, the electric potential will be equal throughout the electrically floated silicon islands, which creates a potential difference ($\Delta V$) between the conductor and silicon, as illustrated in Fig. 6b. As mentioned earlier, vertical sparks may be generated in the conductor/SiO$_2$/Si-conductor sandwich structures when the value of $\Delta V$ exceeds the breakdown voltage of SiO$_2$. Meanwhile, the value of $\Delta V$ indicated in Fig. 6b could be negligible as long as the patterned width of the silicon films is small enough to prevent dielectric breakdown. Silicon dioxide grown by PECVD typically has a dielectric strength of $\sim 5 \times 10^6$ V/cm. For example, if a gate oxide with a thickness of 100 nm is used, the threshold voltage for dielectric breakdown will be 50 V. Therefore, the pattern width of active a-Si islands should be $< 500$ μm in order to avoid dielectric breakdown if JIC crystallization is carried out using an electric field of 1300 V/cm; thus, the maximum size of Si islands for avoiding dielectric breakdown would be $\sim 770$ μm, assuming that PECVD SiO$_2$ has dielectric breakdown at $\sim 5 \times 10^6$ V/cm.

If the method of producing JIC samples illustrated in Fig. 6a is adopted, coplanar top-gate poly-Si TFTs can be fabricated without any additional process steps indicated in Fig. 2 as compared to standard processing. An electric pulse was applied on the Mo thin film for crystallizing pre-patterned a-Si islands. Fig. 7 shows transmission electron (TEM) micrographs of the JIC sample after JIC processing carried out under the conditions of a nominal electric pulse of 1300 V for 11 μs. It can be observed from the plan-view TEM image in Fig. 7a that a-Si was converted to a polycrystalline phase with a grain size of $< 0.1$ μm. It was also found that the Mo/SiO$_2$ and SiO$_2$/poly-Si interfaces retained their sharp morphologies, as can be seen in the cross-sectional TEM images in Fig. 7b.

Figure 8 shows the transfer characteristics of poly-Si TFTs fabricated using the JIC poly-Si film. The $p$-channel JIC poly-Si TFT with W/L = 7 μm/7 μm exhibited a field effect mobility of 38.9 cm$^2$/V-s, a threshold voltage of $-2.8$ V, and a gate voltage swing of 0.35 V/dec. Even though the grain size was smaller than that obtained using SPC at around 600 °C, a typical SPC temperature, the carrier mobility was relatively high. This may be due to the presence of a small amount of intragranular defects, as can be observed in the TEM image in Fig. 7a. The off current ($I_{\text{off}}$) was 1.04 pA/μm, and the $I_{\text{on}}/I_{\text{off}}$ ratio was $4.42 \times 10^6$. The interface between the gate oxide and poly-Si was not degraded, as can be seen in the TEM image in Fig. 7b. Moreover, poly-Si could not be contaminated from the Mo layer, because the diffusion of metallic species into the active layer through the gate oxide would not occur within a very short pulsing time. These two factors may explain why a high value of $I_{\text{on}}/I_{\text{off}}$ was obtained. Excimer laser annealing (ELA) is now being used for crystallizing a-Si films. The typical value of the grain size of the ELA poly-Si is around 0.3 μm. The mobility of p-type ELA poly-Si TFTs is $\sim 80$ cm$^2$/V-s.
Although the mobility of JIC poly-Si TFTs is small compared to that of ELA ones due to small grain size JIC poly-Si TFTs would find its application in large-sized devices such as AMOLED-TVs.

Conclusions

We observed different kinetic paths of phase transformation depending on the input conditions using in-situ measurements of temperatures and reflectances at 532 nm. A sudden increase in reflectance was detected when melting initiated, while a gradual increase in reflectance was observed when Si remained in the state of solid phase during the process. By performing JIC of pre-patterned a-Si islands, crystallization was achieved without arc instability since the potential difference (∆V) between the conductor and silicon islands was negligible enough to avoid dielectric breakdown in the conductor/SiO₂/Si-islands sandwich structures. Poly-Si produced using JIC showed equiaxed grains with a grain size of < 0.1 μm. In this way, coplanar top-gate p-channel JIC poly-Si TFTs were fabricated without any additional processing steps.

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