Low-Latency Analog-to-Analog Signal Processing using PC Hardware and USRPs

Maximilian Engelhardt†, Carsten Andrich†‡, Alexander Ihlow‡, Sebastian Giehl†, Giovanni Del Galdo†‡

†Technische Universität Ilmenau, Institute for Information Technology, Ilmenau, Germany
‡Fraunhofer Institute for Integrated Circuits IIS, Ilmenau, Germany

Abstract—In this paper, we implement a low-latency rapid-prototyping platform for signal processing based on software-defined radios (SDRs) and off-the-shelf PC hardware. This platform allows to evaluate a wide variety of algorithms in real-time environments, supporting new developments in the fields of classical, AI-based, and hybrid signal processing. To accomplish this, the streaming protocol of the used USRP X310 devices is implemented using the Data Plane Development Kit (DPDK), which allows to handle network communication in userspace only. This bypasses the kernel and thus avoids the latencies caused by interrupt handling, scheduling, and context switches. It allows signal processing to be performed on isolated processor cores that are protected from interrupts to a great extent. To validate our approach, linear time-invariant channel emulation has been implemented. For this, an analog-to-analog latency of 31 µs was achieved, demonstrating that our PC-based approach enables the implementation of rapid-prototyping systems with low latency.

Index Terms—USRP, software-defined radio (SDR), rapid prototyping, signal processing, integrated communication and sensing, artificial intelligence in signal processing

I. INTRODUCTION

Signal processing applications requiring low latency and deterministic timing are typically realized using field-programmable gate arrays (FPGAs), involving significant implementation effort. Software-defined radios (SDRs) with standard drivers are focused on the easy implementation of algorithms, but make it difficult to meet real-time requirements. Here, we present a platform based on PC hardware and the widely used SDR USRP X310, manufactured by Ettus Research, with a software implementation tuned for low latency.

For this, communication with the SDR is not handled via the standard driver, but an optimized implementation of the protocol is used that bypasses the kernel network stack. Furthermore, the operating system is configured to interfere as little as possible with the application running on isolated CPU cores. As a test case, LTI channel emulation is implemented, although the platform allows to evaluate a wide variety of algorithms, supporting new developments in the field of AI-based and hybrid signal processing.

A. State of the Art

For the used SDRs, a driver package is provided by the manufacturer, the so-called USRP Hardware Driver (UHD). To enable low-latency data processing, it also supports the use of the Data Plane Development Kit (DPDK), a framework for optimized network communication [1]. The performance of this interface is evaluated in [2]: A Long-Term Evolution (LTE) user equipment (UE) is implemented, whereby a data rate of 30 Mbit/s is achieved. Rather than the overall latency of the system, the jitter of the packet processing is analyzed. Employing the DPDK allows to reduce it to as little as 179 µs, while the best result achieved without DPDK was 448 µs.

As an example of low-latency signal processing implemented directly on an FPGA, [3] can be considered, where a channel emulation is implemented directly on the FPGA of the SDR. This allows for an outstanding performance, a latency of only 3.5 µs at 100 MSa/s. However, this approach is limited to the resources offered by a single device: In this case, the available ports restrict it to 2x2 multiple input multiple output (MIMO) and the implemented signal processing algorithm is fixed (tapped delay line (TDL) with 18 taps).

II. SOFTWARE IMPLEMENTATION

A. UHD

The UHD is a common driver for the broad portfolio of SDR devices manufactured by Ettus Research, which are connected via various interfaces. Since the model used for our experiments, X310, is connected via Ethernet, it is discussed here specifically. The network connection is established via the conventional kernel network stack. However, instead of the socket API, an interface based on boost::asio is used to avoid copies of the transferred data.

This method is not optimal for low-latency signal processing, since delays may occur on several levels (see Figure 1): First, the kernel must be notified about incoming packets which is done via an interrupt, introducing a delay. In high-load scenarios, interrupt coalescing may be used (see [4]), whereby packets are processed in batches, resulting in an even higher latency, which is why this optimization should be deactivated in real-time applications. Then, the packet is processed in the kernel and passed to the waiting application thread. In this step, a further delay arises from the necessary scheduling and second context switch.

Analogously, recurring context switches between application software and kernel are also required when sending samples. In addition, the user does not have full control over the host-side Tx buffers managed by the UHD [5]. This is problematic because buffered samples increase the latency of...
the system. Therefore, for a low-latency application, Tx-side buffering on the host should be avoided.

B. UHD DPDK

One possible solution to the problem described above is to use the DPDK, which the UHD supports as an alternative network interface. This software framework allows network communication to be implemented entirely in userspace, bypassing the kernel network stack. To achieve this, it provides its own userspace-only drivers for a wide range of NIC types. These are based on polling so that the delay associated with interrupts can be circumvented. A DPDK application is executed on isolated CPU cores, which it fully occupies and does not share with other threads. This completely avoids delays due to scheduling and context switching. In addition, the DPDK offers other functionalities that support the development of optimized applications, such as efficient memory management and queues.

DPDK integration is implemented in the UHD in such a way that each device is assigned a core that handles only the network communication. The samples are then exchanged via queues with the application threads running on other cores, where the actual signal processing takes place.

The accompanying documentation provides instructions for moving system interrupts away from the used cores [5]. Additionally, the performance of the used central processing unit (CPU) cores was increased by deactivating the respective hyper-threading siblings.

C. Pure DPDK Protocol Implementation

To circumvent the problems described above, we implemented the sample streaming protocol directly in the DPDK-based application. This bypasses the UHD in the performance-critical path and allows integrating the reception and transmission of packets into the signal processing flow, eliminating the need for separate IO threads. To achieve this, it is necessary to implement the sample streaming protocol of the USRP, which is outlined in the following.

D. The CHDR Protocol

The USRP devices rely on the proprietary protocol designated as condensed hierarchical datagram for RFNoC (CHDR) described in [6]. Since this documentation does not cover all relevant aspects, it was necessary to rely on reverse-engineering of the open-source UHD in some cases. Thereby, only the actual sample streaming was re-implemented: The highly complex initialization of the device was done with the UHD for our experiments, as this is not performance relevant.

The analysis of the USRP’s protocol has shown that it is not designed for real-time applications: As shown in Figure 2 in case of a Tx sample packet arriving too late, a complex recovery process has to be triggered to continue sample-synchronous streaming, requiring 3 round-trips. This cannot be solved by adding a timestamp to each sample packet: The device will still discard any further arriving packets until the error-handling process is completed.

E. Latency Optimization

To achieve the lowest possible latency, not only the application itself but also the environment must be optimized. It is of great importance that no other tasks are running on the CPU cores that perform the real-time signal processing.

The basic measure here is to set the scheduling policy SCHED_FIFO, which is optimized for real-time applications,
and to ensure with the boot parameter isolcpus that no other processes are scheduled on these cores.

The next steps are to avoid interference not only from other processes but from the kernel itself. There are several options that can be activated via boot parameters:

- The periodic scheduling clock can be disabled with nohz_full [7].
- irqaffinity allows setting which cores handle hardware interrupts [8]. The real-time cores should be excluded here.
- The kernel uses read-copy-update (RCU) for lock-less mutual exclusion. This requires to schedule callbacks for later execution. With the options rcu_nocbs and rcu_noch_poll, the behavior can be optimized to move this task away from the real-time cores [9].

However, all these measures only mitigate interrupts but do not prevent them completely. The recent activity on the Linux kernel mailing list (LKML) shows that there are efforts by some developers to create a complete solution here [10], but no inclusion in the mainline kernel seems foreseeable yet.

### III. Evaluation Method

#### A. Hardware

As shown in Figure 3, the core of our test setup is a host PC fitted with a CPU of the type AMD Ryzen 9, which offers 16 physical cores. Two SDRs of type Ettus Research USRP X310 are connected to it, whereby each is fitted with two daughterboards of type UBX. Only one channel is used per daughterboard to avoid crosstalk between the channels. For single-channel tests, only one of the SDRs is used, while both devices together allow experiments with 2x2 MIMO. The connection to the host is established via one 10 GBit Ethernet link each. The two SDRs are synchronized by connecting their PPS and 10 MHz ports.

![Test setup consisting of the host PC and two SDRs. The second SDR, drawn in gray, will only be used for MIMO tests.](image)

As measurement device, we use a broadband channel sounding system which is also based on the USRP X310. This allows for measuring the analog-to-analog latency of the overall system, which is the central parameter for our evaluation. Furthermore, it allows evaluating the correctness of the channel emulation: If the implementation is correct, the measured channel corresponds to the emulated one.

We use a sample rate of 100 MSa/s and a center frequency of 3.75 GHz for our experiments. Another important parameter is the number of samples per packet: In the default setting, the UHD selects the highest possible value here, which minimizes the overhead, but increases latency. For our measurements, we set 512 samples per packet, which results in a packetization delay of 5.12 µs.

#### B. Pass-Through

The most basic test case is the unchanged transmission of the received signal. This implies that no signal processing takes place in the host, but the application only forwards the received samples. This elementary example allows determining the minimum achievable analog-to-analog latency for this system architecture.

#### C. LTI Channel Emulation

As a second test case, the emulation of a linear time-invariant (LTI) channel is implemented. Mathematically, this means that the received signal is convolved with a given channel impulse response $h(t)$. According to the convolution
In this paper, we investigated the possibility of implementing a low-latency signal processing system based on USRPs and off-the-shelf PC hardware. In doing so, the hardware driver provided by the manufacturer UHD was replaced by an optimized custom solution based on the DPDK framework. With this, a very good performance was achieved, reducing the pass-through latency from 104.8 µs to only 25.2 µs. The performance of the UHD’s own DPDK interface failed to match this. The resulting software shows the potential of our approach but has to be seen as a prototype so far. The employed hardware is capable enough for MIMO signal processing. Overall, it was shown that a rapid-prototyping platform for low-latency signal processing can be implemented with the combination of PC hardware and SDRs.

VI. FUTURE WORK

As was discussed in Section IV-B, the presented isolation techniques are not sufficient to completely isolate the real-time application from kernel interference. Since for a continuous output stream every sample packet must arrive in time, the achievable system latency is limited by the worst-case delay. This is particularly important for more complex applications: The longer the computing time, the higher the probability that the processing of a single packet can be disturbed by several interrupts. Therefore, solving this incomplete isolation is an important starting point for further optimization.
Furthermore, it must be noted that the CHDR protocol is not designed for coherent sampling in real-time applications as described in Section II-D. A modified protocol design, whereby the device merely replaces missing packets in the Tx stream with zeros, would significantly shorten the resulting gap in the output signal. Also, a desirable protocol feature would be to allow distributing Rx samples to multiple hosts, for example via the Ethernet multicast mechanism. This is not provided by the UHD’s protocol, obstructing the scaling of the system to multiple hosts. Overall, an SDR optimized for low-latency real-time applications should use a protocol adapted to it.

Another possible further development would be the integration of the GPU, where DPDK enables a low-latency zero-copy interface. This would involve additional effort but would provide the enormous computational power of the GPU, which is an invaluable enhancement for AI-based algorithms.

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