DESIGN OF HIGH PERFORMANCE ADDER USING MODIFIED GDI BASED FULL ADDER

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Abstract:

Adders are the fundamental building blocks for any digital processors in VLSI design. The propagation delay should be low for high level applications and thus the speed is depends on the propagation delay of the full adders. Hence, the efficient design of the full adder is one of the major concerns in fulfilling the requirements of latest applications. As there is lot of research is carrying on full adder designs, still there is a scope of improvement. This paper aimed at design of high performance Carry Save Adder (CSA) using a modified 1-bit full adder. Initially, the basic building block i.e., a full adder is discussed using existing and proposed Modified Gate Diffusion Input (Modified GDI) techniques. Later, by using this proposed adder the CSA have been designed and compared its performance with respect to speed, Power dissipation and area. All the proposed designs are designed in mentor graphics tools at 90nm technology.

Keywords: 1-bit full adder, Carry Save Adder, Gate Diffusion Input, Power Dissipation, Propagation Delay.

I. Introduction

Applications like of signal processing and embedded systems are majorly depends on performance of adders. Adders are used in digital electronics to perform addition on 2 or more numbers, it is also used to calculate the address in chips. The performance like speed, power consumption and area are important criteria in any adder circuits in order to integrate in chip designs. There are many techniques that aims for the performance criteria some of the techniques like GDI (Gate Diffusion Input), pass transistor logic and transmission gate logic are considered as emerging technologies due to speed, power and delay [I]. The principle aim is to minimize...
power consumption and hence adders can be designed with various power minimizing techniques along with to reduce the propagation delay which is also a considerable performance characteristic.

Though the application of a full adder is to add 3 one bit numbers, it is the main component in an ALU. In ALU, to store a data in a new address, it has to use the adder to increment the address and store it in the corresponding location. Or in any case the instruction counter, which keeps track of the next instruction to be executed. Hence, these adders are useful in processor architecture.

II 1-Bit Full Adder Design Using Existing Techniques

This part of the paper is discussing about the design of one bit full adder with low power, high speed and minimum size by using conventional CMOS and GDI techniques. Primarily, conventional CMOS adder with 28-transistors is discussed. The functionality of the adder is described in Table 1 and also its boolean expressions are presented in Eq.1 and Eq. 2 respectively [II-III]. Inputs are ‘a’ and ‘b’ which are to be added to ‘c’, the carry input and, ‘S’ is the sum output, $C_0$ is the output carry. Direct implementation of these two expressions using CMOS technique requires 46-transistors.

$$S = a \oplus b \oplus c$$ \hspace{1cm} (1)

$$C_0 = ab + bc + ca$$ \hspace{1cm} (2)

| a | b | c | S | $C_0$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Table 1: Functionality table of 1-bit Full adder

Simplified form of adder can be designed by modifying the Eq.4.1 and Eq.4.2 as described below [III]. Eq. 2. can be rewritten as

$$C_0 = ab + c(b + a)$$ \hspace{1cm} (3)

and then

$$\overline{C_0} = \overline{ab} + c(\overline{b} + \overline{a})$$ \hspace{1cm} (4)

By using Eq. 4, the Sum expression in Eq. 1 can be expressed as

$$S = abc + (a+b+c)\overline{C_0}$$ \hspace{1cm} (5)

The expressions mentioned in Eq. 3 and Eq. 5 are used in designing and is shown in Fig 1. In Fig 1., N and P are the NMOS and PMOS transistors respectively [IV-VI].
Next, consider the design of a GDI based full adder design. The principle of operation and construction procedure has been described[VI]. This design requires 10-transistors. The drawback of GDI full adder is full output swing is not obtained for Sum and Carry-Out ports. The reasons for this are, the applied low supply voltage (1.8V) and low input pulse voltage (1V) and also due to the improper substrate connections when input $A=0'$. Because of these reasons, body effect is increased and thus degraded output swing is observed at the output. Therefore, the GDI based full adder is less preferred to high performance applications. To get proper functionality during this case, at the output of this adder should be require an additional circuitry (debugging circuit). The design with debugging concept is shown in Fig 2, in which each Sum and Carry-Out ports are cascaded with two back to back connected inverters separately. The corresponding output functionality for the same input data considered above is represented in Fig 2.

III. Proposed 1-bit Full Adder

To overcome the drawbacks mentioned in GDI based adder, this paper presenting the adder design using Modified Gate Diffusion Input (MGDI) technique. It requires fewer transistors in compared with conventional CMOS adder which is described above and improves the output swing than GDI based adder. As mentioned, one of the important requirements of full adder cell especially at low voltage is to provide enough driving capability to the cascading stages. The drivability is ensured by the full signal swing of the initial stage, so that the second stage of full adder which generates sum and carry output will have enough input drive. Fig.3 presents the design of MGDI based full adder.

\[ \text{Fig 1. Conventional CMOS 1-bit full adder with 28 transistors} \]

\[ \text{Fig 2. GDI based full adder design with debugging concept} \]

\[ \text{Fig 3. MGDI based full adder design} \]
From the Fig 4, it can be understood that the sum and carry outputs are degraded by approximately threshold voltages of MOS transistors. This is due to the number of cascaded stages used in this design at low input voltage (1V) that will cause a significant output drop. Due to this, the driving capability of the entire circuit will be reduced.

This work also presents the feasible solution to get high drivability using proposed MGDI full adder. A PMOS transistor is used as feedback transistor at the second stage output i.e., the node at $A \oplus B$ operation is obtained. This will increase the strength of the logic ‘1’ transfer during the operation, thereby increasing the driving capability. This design is shown in Fig 5, where the PMOS feedback transistor is represented as F1. The corresponding output functionality is represented in Fig 6. It is understood from the Fig 6, that the full swing output is achieved through the proposed MGDI adder by using an additional PMOS transistor unlike the debugging circuits used in GDI based full adder.
Fig 4. Output waveforms of 1-bit full adder using MGDI without feedback transistor

Fig 5. MGDI based 1-bit full adder with feedback transistor
From the Table 2., it can be inferred that the proposed MGDI based full adder (with feedback transistor) has many advantages like less propagation delay, low power dissipation and less area occupied with respect to conventional adder designs.

**Table 2**: Propagation delay, Power dissipation, and Transistor count of various 1-bit full adders

| S.No | Design method                     | Power dissipation in mw | Propagation delay in ns | Transistor Count |
|------|----------------------------------|-------------------------|-------------------------|-----------------|
| 1    | Static CMOS                      | 99.21                   | Carry=59.66 Sum=40.87   | 28              |
| 2    | GDI (Without debugging)          | 20.32                   | Carry=49.58 Sum=20.05   | 10              |
| 3    | GDI (With debugging)             | 54.58                   | Carry=55.65 Sum=38.39   | 18              |
| 4    | MGDI (without feedback transistor)| 16.03                   | Carry=48.6 Sum=19.95    | 10              |
| 5    | MGDI (with feedback transistor)  | 14.01                   | Carry=47.7 Sum=19.3     | 11              |

**IV. Design of 4-bit Carry Save Adder**

Fig 7. represents the Carry Save Adder (CSA) for the addition of 4-binary numbers with 4-bits each. Assume that the input operands are A, B, C, D and C0, where C0 is a initial carry. In the design, 3 by 2 counters are placed at the top and,
and a 4-bit Carry Propagating Adder (CPA) is placed at the bottom. 3- bits of the same significance will be taken by the CSA operator and calculates the sum and carry outputs.

Fig 7. A 4-Operand 4-bit CSA

This design can also be extended to addition of k- operands as input. In this case, to implement the addition, it is required that (k-2) no.of CSA levels and one CPA. With this arrangement, the total time required to get the addition is

\[ T = T_{CPA} + (k-2) \cdot T_{CSA} \]  

Eq.6 depicts the time needed for implementing k-bit CSA. Here, \( T_{CSA} \) and \( T_{CPA} \) are the corresponding execution times of the CSA and CPAs. Fig.8, represents the 8-bit Carry Save Adder. The required 1-bit full adder and RCA are already designed by using CMOS, GDI and MGDI techniques [II]. Those designs will be used here as modules and there by obtaining the required 8-bit CSA which is designed by using the existing techniques of CMOS, GDI and the proposed technique of MGDI. Fig 8. describes the design of 4-operand 8-bit Carry Save Adder. Carry Save block located at the top of the design and the carry propagation block is placed at the bottom of the design. The sub-modules design has been discussed in the previous sections. In the top two levels, 16 one bit adders and in the bottom level an 8-bit RCA has been used. The four operands considered for addition are, a, b, c and d with each of 8-bits length, namely \( a[0:7] \), \( b[0:7] \), \( c[0:7] \), \( d[0:7] \).

V. Results and Discussions

In Fig. 8, the inputs \( a[0:7] \), \( b[0:7] \) and \( c[0:7] \) are applied to first level adders. The input \( d[0:7] \) is applied to the second stage adders along with sum outputs and carry-out of the previous stage. The last stage is used to carry propagation and the final result of sum and carry are obtained at this stage. In the Fig.8, \( S[0:8] \) are the sum outputs and \( C_{out} \) is the final carry-output. The design procedure is the same for all the three techniques except the design of internal sub-modules. In CMOS 8-bit CSLA design, CMOS based designs are used.

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Simulation results of MGDI based CSA is depicted in Fig.9. and the functionality has been verified for the following data.

\[
\begin{align*}
    a[7:0] &= 10111111, \\
    b[7:0] &= 01111111, \\
    c[7:0] &= 10101111, \\
    d[7:0] &= 11110000, \\
    \text{and } C_{in} &= 0.
\end{align*}
\]

The resulted sum and carry outputs are \( S[8:0] = 010011101 \) and \( C_{out} = '1' \) respectively. For applying the above input data, \( Y_1 \) and \( Y_2 \) have been considered with logic ‘1’ and logic ‘0’ respectively and are connected to \( a_i's \) and \( b_i's \) as per the input bit streams.

![Figure 8. 4-operand 8-bit Carry Save Adder](image)

**Table 3:** Power Dissipation, Propagation Delay and Transistor count of Carry Save Adder

| Type of Adder  | Parameter                  | CMOS       | GDI        | MGDI 1  |
|----------------|----------------------------|------------|------------|---------|
| 8-bit CSA      | Total Power Dissipation in pW | 812.67x10³ | 517.15     | 287.9   |
|                | Propagation Delay in ns    | 130.5      | 80         | 65      |
|                | Transistor Count           | 672        | 432        | 264     |
From the Table 3, it is observed that MGDI based 8-bit Carry Save Adder dissipates a total power dissipation of 287.96pW where as CMOS and GDI cases have the dissipation of 812x10^6pW and 517.15pW respectively. This shows that there is much reduction in MGDI based Carry Save Adder when compared with CMOS based Carry Save Adders. Similarly in 16-bit operation, total power dissipation in MGDI case is having 539.5pW where as CMOS and GDI cases have the dissipation of 1012.67x10^3pW and 1009.09pW respectively. With reference to the propagation delay, 8-bit MGDI Carry Save Adder has 65ns where as CMOS and GDI have 80ns and 130.5ns respectively.

VI. Conclusions

In this paper, high performance adder CSA have been discussed. The proposed 1-bit full adder using MGDI technique has been used in designed MGDI based high performance adders. The adder is designed in three different techniques namely, CMOS, GDI and the Modified GDI techniques. Functionalities of MGDI based designs have been verified. It is observed that MGDI based designs offers less power dissipation, high speed and require less no. of transistors. Hence, it is concluded that MGDI based adders can be used in high performance applications and can be used in the multipliers.
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