

VTA: An Open Hardware-Software Stack for Deep Learning

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Abstract

Hardware acceleration is an enabler for ubiquitous and efficient deep learning. With hardware accelerators being introduced in datacenter and edge devices, it is time to acknowledge that hardware specialization is central to the deep learning system stack.

This technical report presents the Versatile Tensor Accelerator (VTA, pronounced \textit{vita}), an open, generic, and customizable deep learning accelerator design. VTA is a programmable accelerator that exposes a RISC-like programming abstraction to describe operations at the tensor level. We designed VTA to expose the most salient and common characteristics of mainstream deep learning accelerators, such as tensor operations, DMA load/stores, and explicit compute/memory arbitration.

VTA is more than a standalone accelerator design: it’s an end-to-end solution that includes drivers, a JIT runtime, and an optimizing compiler stack based on TVM. The current release of VTA includes a behavioral hardware simulator, as well as the infrastructure to deploy VTA on low-cost FPGA development boards for fast prototyping.

By extending the TVM stack with a customizable, and open source deep learning hardware accelerator design, we are exposing a transparent end-to-end deep learning stack from the high-level deep learning framework, down to the actual hardware design and implementation. This forms a truly end-to-end, from software-to-hardware open source stack for deep learning systems.

1 Introduction

Specialized deep learning hardware is starting to become commonplace in the datacenter, and on the edge. Much of the progress in ML system has been fueled by hardware specialization, which allows faster training and inference at lower energy costs [7, 4, 9, 6].

Using specialized hardware, though, requires deep learning frameworks to be re-designed around novel hardware architectural features and interfaces. Google’s TensorFlow XLA and TPU [7] system stack is an excellent example of a complete framework built to take full advantage of hardware acceleration. However at the time of this writing, not much of the TPU hardware design, low-level programming interface, code-generation, or operator libraries are made transparent and available for researchers to maintain, experiment, and customize.

In order to understand how hardware specialization is transforming the deep learning system landscape, it is essential to give systems, compilers, and machine learning researchers access to a complete system stack that transparently exposes all of its layers, including the hardware architecture of the accelerator itself, and its low-level programming interface.

We present the VTA stack, a complete deep-learning system stack built with TVM [1] around VTA, a generic deep learning hardware accelerator design. VTA aims to serve as a blueprint to deep learning, systems, and compilers researchers who want to understand how hardware accelerators dictate new constraints across the system stack, and how the latter can be better co-designed with hardware.

The VTA stack was designed with the following design objectives:

• Provide a common deep learning system stack for hardware, compilers, and systems researchers alike to incorporate state-of-the-art optimizations and co-design techniques.

• Lower the barrier of entry for machine learning practitioners to experiment with novel network architectures, operators and data representations that require specialized hardware support.
1.1 Use-Case Scenarios of the VTA Stack

We discuss several scenarios where the VTA stack enables novel opportunities across hardware, compilers, and deep learning research.

**Hardware Designers and Computer Architects.** Deep learning accelerators are becoming commonplace in high-performance hardware architecture, with new ASIC designs being regularly announced. Building a complete and usable software stack on top of novel hardware is essential to gain adoption both in academic circles, and commercially. The VTA stack aims to provide a reference software stack implementation built around specialized hardware. We hope that the VTA software stack will empower hardware designers to quickly build and deploy optimized deep learning libraries ready to be utilized by high-level frameworks of the likes of TensorFlow or PyTorch.

In addition, the quick deployment on FPGA hardware allows hardware architects to (1) produce end-to-end workload evaluation results to understand the benefits and limits of hardware acceleration, and Amdahl’s law limitations, and (2) provide a reference hardware platform for ACM artifact reproducibility.

**Optimizing Compilers Researchers.** Novel domain-specific intermediate representations and optimizing compilers have been proposed to better take advantage of deep learning workloads’ domain specificity [11, 12, 5]. The VTA stack extends TVM to support accelerator-centric scheduling primitives, and low-level code generation. This serves as a blueprint for extending other optimizing deep learning compilers to support new flavors of hardware accelerators.

VTA’s TVM-based open-source deep learning compiler stack also aims to emulate the success of LLVM, by getting contributors to improve the hardware-centric TVM passes over time. The extendability of the compiler stack, combined with the ability to modify the architecture and the programming interface of the hardware back-end opens up novel opportunities in hardware-software co-design for deep learning workloads.

**Deep Learning Researchers.** Having a transparent and customizable software and hardware stack empowers deep learning researchers to come up with novel neural network operators and data representations, while having the opportunity to evaluate the effect of these optimizations on end-to-end workloads. Techniques like binarization [4] are currently limited to the confines of CPU and GPU evaluations. This approach yields limited results unless significant engineering resources are dedicated to produce an FPGA or ASIC implementations to evaluate the technique’s full energy savings potential.

With a reference hardware stack that is readily deployable, the VTA stack aims to lower the barrier of entry to hardware customization for practitioners who don’t have a hardware background.

1.2 Stack Overview

Figure 1 provides an overview of the VTA stack, and the abstraction layers that make up its composition. The goal of the VTA stack is to bridge the gap between productivity-oriented deep learning frameworks, and performance-focused hardware substrates, such as FPGAs which bring hardware specialization to the masses.

**NNVM Intermediate Representation.** NNVM provides a graph-level Intermediate Representation (IR) to deep learning frameworks to take advantage of graph-level optimizations, such as operator fusion [11]. The NNVM IR is also used to specify data layout and data format constraints, which is useful in the context of deep learning acceleration.

The output of the NNVM layer are calls into operators that compose the neural network graph. Next we look at how these operators are implemented and optimized using TVM.

**TVM Intermediate Representation (Section 4).** TVM builds upon the Halide [9] DSL and schedule primitives to provide an optimizing compiler capable of bringing performance portability to deep learning workloads across divergent hardware back-ends [11]. Specifically TVM brings novel scheduling primitives that target specialized hardware accelerators. Examples include tensorization, which lowers computation onto tensor-tensor hardware instructions. In addition, TVM provides scheduling primitives and lowering rules that allow for explicit memory management, and memory vs. compute arbitration for hiding latency.

In the case of VTA, TVM produces lowered LLVM-IR which calls into a custom VTA runtime API, which we discuss next.
Figure 1: The VTA hardware - TVM software stack, where each layer represent an abstraction that bridge the gap between user-facing high-level deep learning frameworks and performance-oriented hardware implementation on an FPGA.

**VTA JIT Runtime (Section 3).** The VTA runtime presents a C++ API that takes care of JIT compilation of VTA binaries, manages shared memory buffers between the CPU and the FPGA, and handles calls to the VTA drivers to perform explicit synchronization. The runtime presents an API that is generic to TVM, hiding away platform-specific bookkeeping tasks. This makes the inclusion of other hardware FPGA platforms or accelerator designs possible, without having to drastically modify the TVM passes, and lowering rules.

The runtime produces an VTA instruction binary in VTA's custom ISA, which we discuss next.

**VTA Instruction Set Architecture (Section 2.2).** VTA’s two-level ISA consists of (1) a high-level CISC ISA that describes high-level, variable latency operations such as DMA transfers, or tensor matrix multiplication and (2) a low-level, fixed latency RISC ISA that describes the compute operations in terms of their memory access patterns. This two-level ISA allows VTA to remain programmable and efficient.

This ISA is specific to VTA, but provides a generic programming interface that is representative of other deep learning accelerator designs [7].

**VTA Hardware Micro-Architecture (Section 2).** VTA's hardware micro-architecture can be considered the bottom-most abstraction layer as it describes how FPGA resources or ASIC transistors should be allocated to expose a programmable layer on which to offload deep learning workloads. With a flexible enough hardware design specification, we aim to make VTA portable to other FPGA platforms, and eventually to ASICs once the design reaches maturity.

## 2 VTA Hardware Architecture

The Versatile Tensor Accelerator (VTA) is a generic deep learning accelerator built for fast and efficient dense linear algebra. VTA is inspired by mainstream deep learning accelerators, including Google’s TPU [7] which is built around a large systolic array-based matrix multiplication accelerator. VTA incorporates a simple RISC-like processor that can perform dense linear algebra operations on rank 1 or 2 tensor registers. In addition the design adopts decoupled access-execute to hide memory access latency [10].

To a broader extent, VTA can serve as a template deep learning accelerator design for full stack optimization, exposing a generic tensor computation interface to the compiler stack.
Figure 2: The VTA hardware organization. VTA is composed of modules that communicate via FIFO queues, and SRAMs. This enables task-level pipeline parallelism, which helps maximize compute resource utilization.

### 2.1 VTA Design Overview

Figure 2 gives a high-level overview of the VTA hardware organization. VTA is composed of four modules that communicate among each other via FIFO queues and local memory blocks (SRAM), to enable task-level pipeline parallelism.

- **Fetch module**: Takes care of loading an instruction stream from DRAM. It also decodes those instructions to route them into one of three command queues.
- **Load module**: Takes care of loading input and weight tensors from DRAM into data-specialized on-chip memories.
- **Compute module**: Performs both dense linear algebra computation with its GEMM core, and general computation with its tensor ALU. It also takes care of loading data from DRAM into the register file, and loading micro-op kernels into the micro-op cache.
- **Store module**: Stores results produced by the compute core back to DRAM.

Section 2.2 provides an overview of the VTA high-level CISC ISA. Section 2.3 explains how the hardware organization of VTA provides memory latency hiding. Section 2.4 describes the front-end of the VTA pipeline that performs instruction fetching and decoding. Section 2.5 describes how VTA performs tensor computation in order to accelerate deep learning workloads. Section 2.6 describes VTA’s memory organization.

### 2.2 VTA ISA

VTA’s instruction set architecture (ISA) is composed of 4 CISC instructions that have a variable execution latency, two of which execute a micro-coded instruction sequence to perform computation. These CISC-instructions echo the TPU [7] and Cambricon [8] set of high-level instructions quite closely. For that reason, VTA can be used to experiment with compiler optimizations that target hardware designs that are not publicly available.

The VTA instructions are listed below:

- **LOAD** instruction: Loads a 2D tensor from DRAM into the input buffer, weight buffer, or register file. It can also load a micro-kernel into the micro-op cache. Supports dynamic padding when loading input and weight tiles.
- **GEMM** instruction: Performs a micro-op sequence of matrix-matrix multiplications over an input tensor and a weight tensors, and adds the result to a register-file tensor.
- **ALU** instruction: Performs a micro-op sequence of matrix-matrix ALU operations over register-file tensor data.
Figure 3: The VTA CISC instruction fields. LOAD and STORE instructions perform 2D strided DMA reads/writes between DRAM and SRAM. GEMM instructions are used to perform matrix multiplication, and 2D convolutions, while ALU instructions can perform a wide range activation, normalization, and pooling tasks.

Figure 4: Task-level pipeline parallelism allows concurrent utilization of compute and memory resources in hardware. Depending on the granularity of the task-level-parallelism, much of the memory access latency can be hidden for compute intensive workloads.

- **STORE** instruction: stores a 2D tensor from the output buffer to DRAM.

The LOAD instructions are executed by the load and compute modules depending on the store memory buffer location target (which is further described by Section 2.4). The GEMM and ALU instructions are executed by the compute module’s GEMM core and tensor ALU. Finally, the STORE instructions are executed by the store module exclusively.

The fields of each instruction is described in Figure 3. Note that the VTA ISA changes as VTA’s architectural parameters are modified (i.e. GEMM core shape, data type, memory size etc.), and as a result the ISA does not guarantee compatibility across all variants of VTA. This is acceptable however, since the VTA runtime adapts to parameter changes, and produces binary code tailored for the version of the accelerator that gets generated. This exemplifies the co-design philosophy adopted by the VTA stack which embraces fluidity of the hardware-software interface.

The interpretation of those instruction fields is described in more details in Section 2.6 for the LOAD and STORE instructions, and in Section 2.5 for GEMM and ALU instructions.

### 2.3 Task-Level Pipeline Parallelism

Managing memory movement to keep compute resources busy is the key to efficient hardware acceleration. Task-Level Pipeline Parallelism (TLPP) is for this reason an important notion in hardware design: it allows for the simultaneous utilization of compute and memory resources in order to maximize their utilization. TLPP is achieved via access-execute decoupling [1], which is the mechanism employed by Google’s TPU [7] to maximize compute resource utilization.

**Latency Hiding.** Figure 4 demonstrates the benefits of performing access-execute decoupling in order to unlock task-level pipeline parallelism. By allowing instructions to execute concurrently in separate hardware modules rather than within a monolithic module, the memory operations can be performed concurrently with compute operations. This
has the effect of hiding memory access latency in typical deep learning workloads. Specifically with 2D convolutions and their high operational intensity, much of the memory access latency can be hidden with this mechanism.

**Data Dependences.** Implementing a decoupled access-execute hardware pipeline requires explicit data dependences between instructions. Figure 5 explains the need to insert those dependences. Let’s assume that we are performing blocked matrix multiplication, where execution phase consists for two load operations for input and weight tensors, a matrix multiply compute operation, and a store operation. In order to extract TLPP, we partition memories into two mutually-exclusive execution contexts, so that concurrent load, compute, and store operations don’t interfere with one another. It’s worth noting that those partitions are software-defined, and don’t require physical separation.

Figure 5 indicates that without dependences, tasks execute as soon as each hardware module is available: this can result in erroneous execution due to operations executing too soon (e.g. the first store will read the results of the first matrix multiplication before the latter is computed). By inserting read-after-write (RAW) dependences between tasks, we can ensure that the producer-to-consumer ordering gets enforced.

Figure 5 shows that even with RAW dependences, erroneous execution can still occur. For example, for a given execution context, a producer task (input load) can overwrite input data in local SRAM before the consumer task (matrix multiplication) from the previous matrix multiplication phase finishes reading it. To alleviate this problem, we rely on write-after-read (WAR) dependences, as a means for one task to signal to the next that it is finished. We rely on both RAW and WAR dependences to guarantee timely and correct execution for decoupled access-execute instruction streams.

**Dataflow Execution.** Now that we conceptually discussed how dependences were necessary to ensure correct ordering of concurrent instructions - we take a look at how those dependences are enforced in hardware. VTA uses dependence FIFO queues between hardware modules to synchronize the execution of concurrent tasks. Figure 6 shows how a given hardware module can execute concurrently from its producer and consumer modules in a dataflow fashion through the use of dependence FIFO queues, and single-reader/single-writer SRAM buffers.

Figure 6 details the pseudo-code that describes how a module executes a given instruction predicated on dependences with other instructions. Dependence flags (see Figure 3) are contained within each instruction, and are decoded in hardware. If the instruction has an incoming RAW dependences, execution is predicated upon receiving a RAW
dependence token from the producer module. Similarly, if the task has an incoming WAR dependence, execution is
predicated upon receiving a WAR dependence token from the consumer module. Finally when the task is done, we
check for outgoing RAW and WAR dependences, and notify the consumer and producer modules respectively.

Figure 6 shows a VTA design composed of four modules that describe a 3-stage task pipeline (load-compute-store). Following the hardware organization principle described in Figure 6, that consists of connecting each module to its producer and consumer via dependence queues, and single-reader/single-writer SRAMs, we can extend the pipeline to include more stages. For example, we can envision separating the tensor ALU from the GEMM core in order to maximize the utilization of the GEMM core. This would result in a load-gemm-activate-store task pipeline which closely reflects the TPU [7] design. Adding more stages has a cost however: it can add storage and extra logic overhead, which is why we opted for a default 3-stage pipeline.

2.4 Instruction Decoding with the fetch Module

VTA is programmed by a linear instruction stream. Those instructions are CISC-like instructions that describe multi-
cycle operations, and are divided into 4 main instruction types: LOAD, GEMM, ALU, and STORE instructions. We discussed
the ISA specification in more details in Section 2.2.

The fetch module is the entry point of VTA to the CPU and is programmed via three memory mapped registers:

- The read-write control register starts the fetch module, and is read to check for its completion.
- The write-only insn_count register sets the number of instructions to execute.
- The write-only insns register sets the start address of the instruction stream in DRAM.

The CPU prepares the instruction stream in DRAM in a physically-contiguous buffer prepared by the VTA runtime. When the instruction stream is ready, the CPU writes the start physical address into the insns register, the length of the instruction stream into the insn_count register, and asserts the start signal in the control register. This procedure starts VTA, which reads in the instruction stream from DRAM via DMA.

Upon accessing the instruction stream, the fetch module partially decodes instructions, and pushes those instructions into command queues that feed into the load, compute, and store modules:

- STORE instructions are pushed to the store command queue to be processed by the store module.
- GEMM and ALU instructions are pushed to the compute command queue to be processed by the compute module.
Figure 7: The VTA GEMM core can perform one matrix multiplication per cycle. It performs matrix-multiplication
over an input tensor read from the input buffer, a weight tensor read from the weight buffer, and accumulates the
result into an accumulator tensor read from the register file. The data addressing of the computation are specified by a
micro-code sequence that executes in a 2-level nested loop.

- LOAD instructions that describe a load operation of micro-op kernels or register file data are pushed to the compute
  command queue to be processed by the compute module.
- LOAD instructions that describe a load operation of input or weight data are pushed to the load command queue to
  be processed by the load module.

When one of the command queues becomes full, the fetch module stalls until the queue is not full. Consequently,
the command queues are sized to be deep enough to allow for a wide execution window, and allow multiple tasks to be in
flight concurrently across the load–compute–store pipeline.

2.5 VTA Compute Core

VTA’s compute core acts as a RISC processor that performs computation on tensor registers rather than scalar registers.
Two functional units perform operations on the register file: the tensor ALU, and the GEMM core. The tensor ALU
takes care of performing low-arithmetic intensity tensor operations, such as element-wise addition. The GEMM core on
the other hand performs high-arithmetic intensity matrix multiplication over data from the input and weight buffers,
and accumulates the result into the register file. As new results are being written to the register file, they concurrently get
flushed to the output buffer to be later stored to DRAM.

Micro-Ops. The compute core executes RISC micro-ops from the micro-op cache, which describe how computation
is performed over data. There are two types of compute micro-ops: ALU and GEMM operations. ALU micro-ops are
executed by the tensor ALU, while GEMM micro-ops are executed by the GEMM core.

To minimize the footprint of micro-op kernels, while avoiding the need for control-flow instructions such as
conditional jumps, the compute core executes micro-op sequences inside a two-level nested loop that computes the
location of each tensor register location via an affine function. This compression approach helps reduce the micro-kernel
Tensor ALU Micro-Ops

| Micro-Op Semantics       | Tensor ALU               |
|--------------------------|--------------------------|
| MIN(x, y)                | \( R[x] = R[x] < R[y] \ ? R[x] : R[y] \) |
| MAX(x, y)                | \( R[x] = R[x] > R[y] \ ? R[x] : R[y] \) |
| ADDI(x, C)               | \( R[x] = R[x] + C \) |
| ADD(x, y)                | \( R[x] = R[x] + R[y] \) |
| MULI(x, C)               | \( R[x] = R[x].lo * C \) |
| MUL(x, y)                | \( R[x] = R[x].lo * R[y].lo \) |
| SHLI(x, C)               | \( R[x] = R[x] << C \) |
| SHRI(x, C)               | \( R[x] = R[x] >> C \) |

ALU Instruction Pseudo-Code:

```python
for i0 in range(0, end0):
  for i1 in range(0, end1):
    for uop_idx in range(uop_bgn, uop_end):
      x, y = decode_alu_indices(uop_buffer[upc])
      dst_idx = i0 * x0 + i1 * x1 + x
      stc_idx = i0 * y0 + i1 * y1 + y
      if USE_IMM:
        reg_file[dst_idx] = OP(reg_file[dst_idx], IMM)
      else:
        reg_file[dst_idx] = OP(reg_file[dst_idx], reg_file[src_idx])
```

Figure 8: The VTA tensor ALU can implement tensor-tensor element wise operations, or tensor-scalar operations.

Instruction footprint, and applies to both matrix multiplication and 2D convolution, commonly found in neural network operators. The next two paragraphs will describe in more details how micro-ops get executed to perform computation.

**GEMM Core.** The GEMM core evaluates GEMM instructions, by executing a micro-code sequence in a 2-level nested loop described in Figure 7's pseudo-code block. The instruction fields of the GEMM instruction are detailed in Figure 5. The GEMM core can perform one input-weight matrix multiplication per cycle, as Figure 7 shows.

The dimensions of the single-cycle matrix multiplication defines a hardware tensorization intrinsic which the TVM compiler has to lower a computation schedule onto. This tensorization intrinsic is defined by the dimensions of the input, weight and accumulator tensors. Each data type can have a different integer precision: typically both weight and input types are low-precision (8-bits or less), while the accumulator tensor has a wider type to prevent overflows (32-bits).

In order to keep the GEMM core busy, each of the input buffer, weight buffer, and register file have to expose sufficient read/write bandwidth, as derived in Figure 7.

**Tensor ALU.** Figure 8 details the range of operators that the Tensor ALU supports to implement common activation, normalization, and pooling operations. VTA being a modular design, the range of operators that the Tensor ALU supports can be extended for higher operator coverage, at the expense of higher resource utilization. The Tensor ALU can perform tensor-tensor operations, as well as tensor-scalar operations on an immediate value. The opcode of the tensor ALU, and the immediate value are specified by the high-level CISC instruction which fields are listed in Figure 3. The micro-code in the context of tensor ALU computation only takes care of specifying data movement patterns, as shown in the ALU instruction pseudo-code block in Figure 8.

In terms of computational throughput, the Tensor ALU does not execute at a rate of one operation per cycle. The limitation comes from the lack of read-ports: since one register file tensor can be read per cycle, the tensor ALU has an initiation interval of at least 2 (i.e. performs at most 1 operation every 2 cycles). In addition, performing a single tensor-tensor operation at once can be expensive especially given that register file types are wide, typically 32-bit integers. As a result, in order to balance the resource utilization footprint of the Tensor ALU with the GEMM core, a tensor-tensor operation is by default performed via vector-vector operations over multiple cycles.

9
Figure 9: The load module can perform 2D DMA loads with a strided access pattern from DRAM to SRAM. In addition, it can insert 2D padding on the fly, which is useful when blocking 2D convolution. This means that VTA can tile 2D convolution inputs without paying the overhead of re-laying data out in DRAM to insert spatial padding around input and weight tiles.

### 2.6 VTA Memory Subsystem

VTA has a single-level on-chip memory hierarchy composed of SRAM memories that are data-specialized, e.g. weight and input activations are stored in different physical SRAM modules. Figure 2 shows that SRAM buffers serve as unidirectional data channels between hardware modules. Each buffer has a single reader, single writer to allow for concurrent execution of both modules.

**Bandwidth Considerations.** Having data-specialized buffers allows each SRAM memory to expose the right amount of bandwidth required to keep the GEMM core busy. For instance, with 8-bit inputs and weights, 32-bit accumulators, $\text{BATCH}=2$, $\text{BLOCK}_\text{IN}=16$, and $\text{BLOCK}_\text{OUT}=16$, the bandwidth required to keep a GEMM core clocked at 200MHz busy is: 51.2 Gb/s, 409.6 Gb/s, and 204.8 Gb/s for each of the input buffer, weight buffer and register file SRAM memories. This divergence in bandwidth requirements explains why VTA relies upon data-specialized SRAM memories, rather than a single memory structure from which to read/write all data.

**Memory Access Latency Hiding.** VTA’s load and store modules perform DMA transfers from DRAM to the input and weight SRAM buffers, and from the SRAM output buffer to the DRAM respectively. These operations can be performed while computation is taking place in the compute core using the latency-hiding mechanisms described in Section 2.3.

**Tiled Access Patterns.** The load and store modules can perform strided 2D accesses from and to DRAM as Figure 9 shows. This feature is useful for describing cached reads and writes over tiled tensor data with a single instruction. The load module can also dynamically insert padding as Figure 9 suggests, in order to tile input and weight tensors in the context of 2D convolution without paying the overhead of spatial packing.

### 3 VTA Runtime System

The VTA runtime library exposes an C++ API of hardware intrinsics that a lowered TVM schedule can call into. It acts as a glue between the TVM compiler and the VTA low-level programming interface, by performing just-in-time (JIT) compilation on accelerator binaries, managing dynamic memory allocation, and handling synchronization with the accelerator.

#### 3.1 Compilation Overview

The role of the runtime can be explained in the context of the TVM compilation flow, summarized in Figure 10 for an ARM-based SoC target. Starting from a hardware-agnostic TVM schedule, scheduling transformations are applied in order to obtain a lowered VTA-specific schedule. These optimizations are discussed in more depth in Section 4.

The lowered schedule, which includes calls to the VTA’s C++ runtime API gets cross-compiled with LLVM into an object file that the TVM RPC library sends over the network to the target device (i.e. Pynq board). The RPC is a TVM
feature that offers flexible and interactive Python-based development on x86 host machines, and efficient deployment on ARM edge devices.

The target ARM embedded system runs the TVM RPC server, loading in the JIT runtime library, continuously listening to incoming requests. Upon receiving a compiled TVM kernel object, the RPC server loads it into a TVM module and returns a handle to the host. The module handle finally gets remotely invoked, thus starting the JIT compilation, memory allocation, and CPU-VTA synchronization tasks to offload the TVM kernel to VTA.

3.2 JIT Runtime

The VTA JIT runtime performs bookkeeping tasks needed to offload computation onto VTA. It exposes a C++ API that performs the following:

- Dynamic memory allocation and buffer management.
- Direct Memory Access (DMA) transfers between main memory (DRAM) and accelerator memory (SRAM).
- Micro-op kernel generation and caching.
- Explicit dependence management in the instruction stream.
- Synchronization between the target CPU and VTA.

We discuss each one of those runtime functionalities in light a lowered TVM schedule example that performs vector addition, dictated by the graph in Figure 11. The TVM schedule below is the result of schedule optimizations and lowering. The resulting TVM code has calls to the VTA runtime which we’ll explain next.
Dynamic Memory Allocation. The VTA runtime memory allocator API includes calls such as VTABufferAlloc() and VTABufferCopy() to allocate and deallocate physically contiguous memory buffers in DRAM. Upon allocating a buffer, the runtime can expose its physical (or virtual) address for the accelerator (or CPU resp.) to access it. In scenarios where the CPU and VTA share coherent memory accesses (e.g. via the ACP port on an ARM SoC) no cache flushing or invalidation needs to take place. In the converse scenario, the runtime will perform cache invalidation before the CPU reads from a buffer, and cache flushing after the CPU writes to a buffer.

DMA Transfers. DMA transfers allow for bulk memory copies between DRAM and the accelerator’s local SRAM. DMA transfers are initiated by DMA masters within VTA modules that access DRAM via the FPGA’s memory controller. As discussed in Section 2.6, VTA supports 2D strided access patterns, which facilitates tiling when tensors don’t fit in VTA’s on-chip buffers. The VTA runtime exposes the VTALoadBuffer2D() and VTAStoreBuffer2D() API calls to generate LOAD and STORE VTA instructions. In the vector add code example in Listing 3.2, these functions are inserted when preparing the SRAM buffers, and when sending the results back to DRAM.

Micro-Op Kernel Generation. In addition to generating an instruction stream composed of LOAD, STORE, ALU, and GEMM instructions, the VTA runtime generates and manages micro-op kernels. A micro-op kernel has to be generated for each unique compute instruction in order to describe the memory access pattern of the compute task. For instance, a 2D convolution with window size of 3 will and stride of 1 will have a different access pattern to a convolution with window size of 7 and stride of 2.

This on-the-fly micro-kernel generation is handled using the VTAUopLoopBegin(), VTAUopLoopEnd(), and VTAUopPush() runtime API functions, listed in the vector addition example. The Begin and End functions prepare and package the micro-op kernel, to produce a CISC compute instruction that will call into the kernel. Each micro-kernel is generated once and cached in DRAM throughout the entire lifetime of the program. Upon each VTAUopPush() call, the runtime adds a VTA micro-op to current micro kernel to construct the kernel. The runtime decides when to swap each micro-kernel into VTA ’s micro-op cache based on a simple LRU cache replacement policy.

Explicit Dependence Management. We saw in Section 2.3 that labeling task dependences explicitly in the instruction stream is necessary to expose task-level pipeline parallelism. The runtime exposes an explicit dependence insertion API, which is illustrated in Figure 12. The VTADepPop() and VTADepPush() calls set the dependence flags of the in-flight instructions to insert a dependence edge between two instructions.

Let’s look at how the runtime can enforce a RAW dependence between a LOAD and its subsequent ADD instruction (e.g. the RAW dependence between ld0 and add0 in Figure 12). At first, the VTADepPush(1load, compute) is called
while preparing the ld0 instruction. This sets the dependence flag of the ld0 instruction so that when that instruction gets executed by the load module, a dependence token gets pushed into the RAW dependence FIFO leading to the compute hardware modules. Second, the VTADepPop(load, compute) is called before preparing the add0 instruction. This sets the dependence flag of the upcoming add0 instruction. When the add0 instruction is executed by the compute module, it pops the dependence token that the previous ld0 pushed in the RAW dependence FIFO, in order to enforce the dependence between the two instructions.

**CPU-VTA Synchronization.** The VTA runtime handles synchronization between the CPU and accelerator in order to synchronously offload work. This is enabled by the VTASynchronize() runtime call which finishes preparing the instruction stream and micro-kernels, and hands-off control to the accelerator. VTA fetches and executes the instruction stream, initiating DMA transfers to and from DRAM. The runtime then waits for the accelerator to notify that is has completed its work.

## 4 TVM Support for VTA

TVM [1] is an optimizing compiler that exposes an intermediate representation (IR) and set of scheduling transformations to produce efficient code for a multiplicity of hardware back-end based on a hardware-agnostic algorithm description. The process of generating multiple valid implementations builds on Halide’s idea of decoupling algorithm descriptions from computation rules (i.e. schedule optimizations) [9].

Figure 13 shows how to apply TVM schedule transformations to lower a high-level hardware-agnostic matrix multiplication expression down to a low-level implementation targeting VTA. The idea is to incrementally change the schedule by applying a set of basic transformations that preserve the logical equivalence of the original program. After the transformations, the lowered schedule for VTA calls directly into the VTA runtime, which then compiles the accelerator binaries on the fly, as discussed in Section 3.

In the following subsections we highlight how TVM is used to apply schedule transformations to target VTA. These compiler passes were described in [1], but we revisit those in light of VTA’s hardware, and runtime internals. It is also worth noting that the scheduling passes that we discuss were implemented in TVM using VTA as a template accelerator target. At the time of building TVM, no commercial deep learning accelerator were available with a completely exposed low-level programming interface, so VTA played a significant role in helping develop the set of accelerator-focused scheduling optimizations that TVM shipped with.

We describe three scheduling primitives that tackle the challenges associated with targeting deep learning accelerators of the likes of VTA: explicit memory management, tensorization, and latency hiding.
4.1 Explicit Memory Management

One aspect that differentiates CPUs and GPUs from deep learning accelerators is explicit management of on-chip memories. In CPUs for instance, caches are implicitly managed by keeping most-recently accessed data on-chip. For accelerators of the likes of the TPU[7], the compiler needs to explicitly specify when data needs to be brought in or out.

TVM introduced the concept of memory scopes to the schedule space so that a compute stage buffer could be assigned to an explicitly managed memory region (AL, BL and CL in the code). In the context of programming VTA, memory scopes let us assign a TVM buffers to a specific memory region and subsequently create region-specific lowering rules.

Section 2.6 explained that VTA had data-specialized memories, meaning that input activation tensors could not be stored in the same memory structure as kernel weight tensors. TVM memory scopes lets us enforce these data specialization constraints, by assigning a given TVM buffer to a particular VTA hardware memory structure. In the example in Figure 13, this translates to assigning CL to the accumulator buffer (a.k.a. register file), AL to the input buffer etc. When reasoning about a TVM dataflow graph, like the one shown in Figure 11 we differentiate between global memories that sit in DRAM, and scoped memories that sit in VTA’s on-chip buffers.

4.2 Tensorization

Deep learning accelerators take advantage of the high operational intensity (i.e. compute to memory operation ratio) of deep learning with hardware functional units specialized for matrix-matrix or matrix-vector computation. To address this growing trend, TVM introduced the tensorization scheduling primitive in order to map dense computation onto high operational intensity tensor hardware intrinsics. Tensorization has analogies with vectorization in SIMD architectures: it
Figure 14: TVM virtual thread lowers a high-level thread-parallel program to a single instruction stream with explicit low-level synchronizations. During execution, the hardware can recover task-level parallelism from the instruction stream to hide memory access latency.

4.3 Explicit Memory Latency Hiding

Section 4.3 motivated VTA’s use of decoupled access-execute instruction pipeline to reduce runtime latency. Programming accelerators that require explicit low-level synchronization is difficult as we discussed saw in the Figure 12 explicit dependence insertion example. To reduce the burden on the programmer, TVM introduced a virtual threading scheduling primitive that let the programmer specify a high-level data parallel program in the same way that they would for a multi-threaded CPUs. TVM automatically lowers the virtual threaded program to a single instruction stream with low-level explicit synchronization, as shown in Figure 14. The algorithm starts with a high-level multi-threaded program schedule and then inserts the necessary low-level synchronization operations to guarantee correct execution within each thread. Next, the operations of all virtual threads are interleaved into a single instruction stream. Finally, the hardware recovers the available pipeline parallelism dictated by the low-level synchronizations in the instruction stream.

5 Evaluation

This section presents a preliminary evaluation of VTA on the Pynq low-cost FPGA evaluation board. The FPGA development board is based on an 2012 SoC, and contains less than 1MB of on-chip storage. We chose this development board due to its high affordability for academics, and the challenge that the limited resources presented in terms of hardware design. The point of the evaluation is to emphasize the full stack at work, rather than to show that we’ve achieved peak performance allowed by the underlying hardware platform – there is still lots of room for improvement. We aim to iterate on the hardware and software stack with the help of the open source community to reach industrial strength results on this platform and upcoming FPGA ones.

Platform. We implement the VTA design on a low-power PYNQ board which incorporates an ARM Cortex A9 dual core CPU clocked at 667MHz and an Artix-7 based FPGA fabric. On the modest FPGA resources, we implement a
Table 1: Configurations of all conv2d operators in ResNet-18 used in the single kernel experiment. H/W denotes height and width, IC input channels, OC output channels, K kernel size, and S stride size. All ops use “SAME” padding.

| Name | Operator | $H, W$ | $IC, OC$ | $K, S$ |
|------|----------|--------|----------|--------|
| C1   | conv2d   | 224, 224 | 3, 64  | 7, 2  |
| C2   | conv2d   | 56, 56  | 64, 64  | 3, 1  |
| C3   | conv2d   | 56, 56  | 64, 64  | 1, 1  |
| C4   | conv2d   | 56, 56  | 64, 128 | 3, 2  |
| C5   | conv2d   | 56, 56  | 64, 128 | 1, 2  |
| C6   | conv2d   | 28, 28  | 128, 128 | 3, 1 |
| C7   | conv2d   | 28, 28  | 128, 256 | 3, 2 |
| C8   | conv2d   | 28, 28  | 128, 256 | 1, 2 |
| C9   | conv2d   | 14, 14  | 256, 256 | 3, 1 |
| C10  | conv2d   | 14, 14  | 256, 512 | 3, 2 |
| C11  | conv2d   | 14, 14  | 256, 512 | 1, 2 |
| C12  | conv2d   | 7, 7    | 512, 512 | 3, 1 |

Figure 15: Roofline of an FPGA-based deep learning accelerator running ResNet inference. With latency hiding enabled by TVM, the performance of the benchmarks are brought closer to the roofline, demonstrating higher compute and memory bandwidth efficiency.

16 × 16 matrix-vector unit clocked at 100MHz that performs products of 8-bit values and accumulates them into a 32-bit register every cycle. The theoretical peak throughput of this flavor of the VTA design lies around 51GOPS/s. We allocate 16kB of resources for microkernel cache, 32kB of resources for activation storage, 256kB for parameter storage, and 128kB for the register file (i.e. accumulator storage). These on-chip buffers are nowhere near large enough to provide enough on-chip storage for a single layer of ResNet, and therefore provide motivational case-study for effective memory reuse and memory access latency hiding.

**Benchmark.** We train a ResNet-18 neural network with MxNet, and perform post-training adjustments on the parameters to convert them to 8-bit weights from 32-bit floating point. The Imagenet top-5 validation accuracy is 63% after fixed-point conversion (we did not focus so much on recovering training accuracy).

We offload all convolution layers of the ResNet-18 network onto the FPGA accelerator, except for the first convolution layer C1, which is evaluated on the CPU due to its low number of input channels. Activations and batch normalization operators are evaluated on the FPGA, while max pooling and fully connected layers are currently evaluated on the CPU.

We describe each of the ResNet-18 layers that we evaluated on the FPGA in Table 1.

**Resource Utilization Efficiency.** A popular method used to assess the efficient use of hardware are roofline diagrams: given a hardware design, how efficiently are different workloads utilizing the hardware compute and memory resources. The roofline plot in Figure 15 shows the throughput measured on different convolution layers of the ResNet-18 inference
Figure 16: We offload convolutions in the ResNet workload to an FPGA-based accelerator. The grayed-out bars correspond to layers that cannot be accelerated by the FPGA and therefore have to run on the CPU. The FPGA can provide a 40x acceleration on offloaded convolution layers over the Cortex A9.

benchmark. Each layer has a different arithmetic intensity, i.e. compute to data movement ratio. In the left half, convolution layers are bandwidth limited, whereas on the right half, they are compute limited.

The goal behind designing a hardware architecture together with its compiler stack is to allow each workload to be brought as close as possible to the roofline of the hardware. The plot belows shows the result of having the hardware and compiler work together to maximize utilization of the available hardware resources. The technique showcased is latency hiding, which requires explicit dependence tracking at the hardware level, compiler support to partition work via virtual threading, and explicit dependence insertion in the instruction stream during JIT code-generation. The result is overall higher utilization of the available compute and memory resources. Peak compute utilization increases from 70% with no virtual threading to 88% with virtual threading turned on (to hide memory access latency). This experiment demonstrates the VTA-TVM stack’s potential for implementing cross-stack optimizations that require visibility into both the hardware and compiler layers.

End-to-end ResNet Evaluation. We leverage TVM to generate ResNet inference kernels on the PYNQ platform and offload as many layers as possible to VTA. We utilize TVM to generate both schedules for the CPU only and CPU+FPGA implementation. Due to its shallow convolution depth, the first ResNet convolution layer could not be efficiently offloaded on the FPGA and is instead computed on the CPU. All other convolution layers in ResNet, however, are amenable to efficient offloading. Operations including residual layers and max pooling are also performed on the CPU since our TVM extensions do not support these operations yet.

A benefit of having a complete compiler stack built for VTA is the ability to run end-to-end workloads. This is compelling in the context of hardware acceleration because it allows us to understand what performance bottlenecks, and Amdahl limitations stand in the way to obtaining faster performance. Figure 16 shows inference performance with and without offloading the convolutions to the FPGA-based VTA design on the ARM Cortex-A9 SoC available on the Pynq board. At a glance, VTA drastically reduces the time it takes to perform convolutions (dark blue) reduces inference time from over 3s down to less than 0.5s. However, it is clear that other operators require offloading if we wish to reduce inference latency even further. This kind of visibility is essential to system designers who want to understand the full story beyond just micro-kernel benchmarks.

6 Conclusion

We introduced the Versatile Tensor Accelerator(VTA), an open, generic, and customizable deep learning accelerator for cross-stack deep learning research and optimization. VTA is complemented by a complete TVM-based compiler stack, and a JIT runtime. This full-stack implementation allows VTA to be utilized by high-level deep learning frameworks to run end-to-end workloads. We show preliminary evaluation results on the low-cost Pynq FPGA development board which demonstrates the complete VTA design and TVM stack working together.

VTA has been upstreamed to the TVM GitHub repository, which is available to the public.
References

[1] Tianqi Chen, Thierry Moreau, Ziheng Jiang, Haichen Shen, Eddie Yan, Yan Wang, Yuwei Hu, Luis Ceze, Carlos Guestrin, and Arvind Krishnamurthy. Tvm: End-to-end optimization stack for deep learning. arXiv preprint arXiv:1802.04799, 2018.

[2] Yu-Hsin Chen, Joel Emer, and Vivienne Sze. Eyeriss: A spatial architecture for energy-efficient dataflow for convolutional neural networks. In Proceedings of the 43rd International Symposium on Computer Architecture, ISCA ’16, pages 367–379, Piscataway, NJ, USA, 2016. IEEE Press.

[3] Yunji Chen, Tao Luo, Shaoli Liu, Shijin Zhang, Liqiang He, Jia Wang, Ling Li, Tianshi Chen, Zhiwei Xu, Ninghui Sun, and Olivier Temam. Dadiannao: A machine-learning supercomputer. In Proceedings of the 47th Annual IEEE/ACM International Symposium on Microarchitecture, MICRO-47, pages 609–622, Washington, DC, USA, 2014. IEEE Computer Society.

[4] Matthieu Courbariaux, Yoshua Bengio, and Jean-Pierre David. Binaryconnect: Training deep neural networks with binary weights during propagations. CoRR, abs/1511.00363, 2015.

[5] Scott Cyphers, Arjun K. Bansal, Anahita Bhiwandivalla, Jayaram Bobba, Matthew Brookhart, Avijit Chakraborty, William Constable, Christian Convey, Leona Cook, Omar Kanawi, Robert Kimball, Jason Knight, Nikolay Korovaiko, Varun Kumar, Yixing Lao, Christopher R. Lishka, Jaikrishnan Menon, Jennifer Myers, Sandeep Aswath Narayana, Adam Procter, and Tristan J. Webb. Intel ngraph: An intermediate representation, compiler, and executor for deep learning. CoRR, abs/1801.08058, 2018.

[6] Song Han, Xingyu Liu, Huizi Mao, Jing Pu, Ardavan Pedram, Mark A. Horowitz, and William J. Dally. Eie: Efficient inference engine on compressed deep neural network. In Proceedings of the 43rd International Symposium on Computer Architecture, ISCA ’16, pages 243–254, Piscataway, NJ, USA, 2016. IEEE Press.

[7] Norman P. Jouppi, Cliff Young, Nishant Patil, David Patterson, Gaurav Agrawal, Raminder Bajwa, Sarah Bates, Suresh Bhatia, Nan Boden, Al Borchers, Rick Boyle, Pierre-luc Cantin, Clifford Chao, Chris Clark, Jeremy Coriell, Mike Daley, Matt Dau, Jeffrey Dean, Ben Gelb, Tara Vazir Ghaemmaghami, Rajendra Gottipati, William Gulland, Robert Hagmann, C. Richard Ho, Doug Hogberg, John Hu, Robert Hundt, Dan Hurt, Julian Ibarz, Aaron Jaffey, Alek Jaworski, Alexander Kaplan, Harshit Khaitan, Daniel Killebrew, Andy Koch, Naveen Kumar, Steve Lacy, James Laudon, James Law, Dhemthu Le, Chris Leary, Zhiyuan Liu, Kyle Lucke, Alan Lundin, Gordon MacKean, Adriana Maggiore, Maire Mahony, Kieran Miller, Rahul Nagarajan, Ravi Narayanaswami, Ray Ni, Kathy Nix, Thomas Norrie, Mark Omernick, Narayana Penukonda, Andy Phelps, Jonathan Ross, Matt Ross, Amir Salek, Emad Samadiani, Chris Severn, Gregory Sizikov, Matthew Snelham, Jed Souter, Dan Steinberg, Andy Swing, Mercedes Tan, Gregory Thorson, Bo Tian, Horia Toma, Erick Tuttle, Vijay Vasudevan, Richard Walter, Walter Wang, Eric Wilcox, and Doe Hyun Yoon. In-datacenter performance analysis of a tensor processing unit. In Proceedings of the 44th Annual International Symposium on Computer Architecture, ISCA ’17, pages 1–12, New York, NY, USA, 2017. ACM.

[8] Shaoli Liu, Zidong Du, Jinhua Tao, Dong Han, Tao Luo, Yuan Xie, Yunji Chen, and Tianshi Chen. Cambricon: An instruction set architecture for neural networks. In Proceedings of the 43rd International Symposium on Computer Architecture, ISCA ’16, pages 393–405, Piscataway, NJ, USA, 2016. IEEE Press.

[9] Jonathan Ragan-Kelley, Connelly Barnes, Andrew Adams, Sylvain Paris, Frédéric Durand, and Saman Amarasinghe. Halide: A language and compiler for optimizing parallelism, locality, and recomputation in image processing pipelines. In Proceedings of the 34th ACM SIGPLAN Conference on Programming Language Design and Implementation, PLDI ’13, pages 519–530, New York, NY, USA, 2013. ACM.

[10] James E. Smith. Decoupled access/execute computer architectures. In Proceedings of the 9th Annual Symposium on Computer Architecture, ISCA ’82, pages 112–119, Los Alamitos, CA, USA, 1982. IEEE Computer Society Press.

[11] Nicolas Vasilache, Oleksandr Zinenko, Theodoros Theodoridis, Priya Goyal, Zachary DeVito, William S. Moses, Sven Verdoolaege, Andrew Adams, and Albert Cohen. Tensor comprehensions: Framework-agnostic high-performance machine learning abstractions. CoRR, abs/1802.04730, 2018.
[12] Richard Wei, Vikram Adve, and Lane Schwartz. Dlvm: A modern compiler infrastructure for deep learning systems. CoRR, abs/1711.03016, 2017.