Quantum Circuit Optimization and Transpilation via Parameterized Circuit Instantiation

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Abstract—Parameterized circuit instantiation is a common technique encountered in the generation of circuits for a large class of hybrid quantum-classical algorithms. Despite being supported by popular quantum compilation infrastructures such as IBM Qiskit and Google Cirq, instantiation has not been extensively considered in the context of circuit compilation and optimization pipelines. In this work, we describe algorithms to apply instantiation during two common compilation steps: circuit optimization and gate-set transpilation. When placed in a compilation workflow, our circuit optimization algorithm produces circuits with an average of 13% fewer gates than other optimizing compilers. Our gate-set transpilation algorithm can target any gate-set, even sets with multiple two-qubit gates, and produces circuits with an average of 12% fewer two-qubit gates than other compilers. Overall, we show how instantiation can be incorporated into a compiler workflow to improve circuit quality and enhance portability, all while maintaining a reasonably low compile time overhead.

I. INTRODUCTION

Circuit instantiation is an operation performed in many hybrid-classical quantum algorithmic workflows such as VQE [1] or QAOA [2]. In this setting, the algorithm has associated a circuit ansatz, where gates are represented in their parameterized form, e.g. $R_z(\theta)$. The execution iterates, and at each step the gate parameters are instantiated (often by a numerical optimizer) using results from previous quantum executions. Due to the popularity of hybrid algorithms, circuit instantiation is directly supported by popular compilation infrastructures such as IBM Qiskit [3], Google Cirq [4] or Tket [5].

Instantiation is also becoming an important step in circuit synthesis tools such as BQSKit [6] (QSearch [7] and QFAST [8]), NACL [9], Squander [10], [11], and CPFlow [12]. Here, circuits are built bottom-up using parameterized gates and are instantiated using numerical optimization at each step.

In this paper, we demonstrate that instantiation is a powerful primitive that can be easily incorporated into any quantum compilation workflow. In our approach, given an input circuit, we replace its gates with parameterized representations and apply instantiation to improve the resulting quality for two essential tasks: circuit optimization and gate-set transpilation.

Circuit Optimization: Circuit depth is a direct measure of quantum program performance. Errors compound its impact in the NISQ era, and as a result, a significant portion of the compilation workflow is dedicated to circuit depth reduction. Our algorithms reduce circuit depth by iteratively deleting gates and reinitializing the circuit until convergence criteria are met. As each gate in a circuit becomes parameterized, numerical optimizers face scalability problems for large circuits. For these, we use a circuit partitioning approach introduced in [13] combined with iterative deletion.

Gate-set Transpilation: Any available quantum processor architecture exposes to users a reduced native gate-set: a few single-qubit rotations and usually a single two-qubit gate. Programs are often generated or expressed in only one gate-set, e.g., $\{R_z, SX, CNOT\}$ for some IBM processors. When transpiling a program to a different native gate-set, most compilers convert two-qubit gates using fixed gate identities or KAK [14] decompositions. In some cases, translations from one gate to another are not readily available. Indeed, when considering the set of existing native two-qubit gates $\{CNOT, CZ, XX, ZZ, \sqrt{iSWAP}, SYC\}$, we note that the most widely used compilers have limited support for transpiling between these gates. Our instantiation-based formulation is completely portable as we directly represent gates by their associated unitary matrix.

The main contributions of this work are as follows:

1) A formal definition of instantiation and a brief survey of it in quantum compiler literature.
2) An optimization algorithm that performs well in existing compilation pipelines and introduces non-local optimizations not present in current passes.
3) A quantum circuit retargeting algorithm that works well on any gate-set without user-defined rules. The algorithm can be further specialized with user rules, if so desired. It even works on gate-sets with multiple two-qubit gates and produces circuits shorter than every other algorithm. The transpiled circuits are informative about the efficacy of a particular gate-set to represent algorithms.
4) A verification procedure for non-exact compilation algorithms on very large circuits that are not simulatable.

We evaluate our approach on a set of circuits used by other researchers to assess the efficacy of compiler optimizations [3], [5], [15]. For comparison, we consider the Qiskit, Cirq, and Tket compilers. When adding our instantiation-based optimization to already existing optimizing workflows, we observe an additional gate reduction of 5% for two-qubit gates and 23% for single-qubit gates. When transpiling to existing hardware gate-sets, we observe an average final two-qubit gate reduction of 12%. In particular, when we were transpiling a 64-qubit time-evolution circuit to Google’s Sycamore gate (SYC),
we recorded a circuit with 3970 two-qubit gates, which is a 51% reduction over Cirq’s circuit with 8064 two-qubit gates.

When examining the execution time overhead, we observe an average slowdown of $14\times$; however, we demonstrate the tunability of our algorithms by speeding up a specific execution by $13\times$ while only reducing quality by 0.6%.

The following intuition provides an explanation for the quality of our results. During circuit optimization, the available compilers use a sequence of rule-based peephole transformations, where at each step, the circuit is only transformed locally. Similarly, for transpilation, they form two-qubit blocks and either apply rule-based translations or KAK-based decompositions. In contrast, a circuit undergoes many global transformations with our approach.

Overall, we believe that the results indicate that instantiation can be easily and safely incorporated as a step in the compilation workflow. The ability to transpile algorithms well between native gate sets enables interesting architectural compilation workflow. The ability to transpile algorithms well can be easily and safely incorporated as a step in the optimization and retargeting algorithms in Section III. We introduce parameterized circuit instantiation and provide a brief survey of it in compiler literature. Then we describe our optimization and retargeting algorithms in Section III. We include our experimental setup and verification procedure in Section IV and evaluate the algorithms in Section V. Lastly, we discuss the results in Section VI and conclude in Section VII.

II. PARAMETERIZED CIRCUIT INSTANTIATION

Instantiation is the process of finding the parameters for a circuit’s gates that make it to most closely implement a target unitary. Techniques that perform instantiation are ubiquitously deployed in quantum compiler toolchains. The formal problem definition is given by:

**Parameterized Circuit Instantiation Problem:** Given a parameterized quantum circuit $C : \mathbb{R}^k \rightarrow U(N)$ and a target unitary $V \in U(N)$, solve for

$$\arg\max_{\alpha} \text{tr}(V^\dagger C(\alpha))$$

where $k$ is the number of gate parameters in the circuit, and $U(N)$ is the set of all $N \times N$ unitary matrices. This definition is very general and considers the parameterized circuit as a parameterized unitary operator, see Figure 1. The $\text{tr}(V^\dagger C(\alpha))$ component measures the Hilbert-Schmidt inner product, which physically represents the overlap between the target unitary and the circuit’s operator. The maximum value this can have is equal to $N$ the dimension of the matrix, and this occurs when $C(\alpha)$, the unitary of the circuit with gate parameters $\alpha$, is equivalent to $V$ the target unitary up to a global phase.

The most common form of instantiation is the KAK [14] decomposition, which uses analytic methods to produce the two-qubit circuit that implements any two-qubit unitary. Compilers have used this decomposition to optimize long sequences of operations. This is done by first grouping together consecutive gates on a pair of qubits, then calculating the unitary implemented by the grouped gates, and finally applying the KAK decomposition to convert to a potentially shorter sequence of gates.

For every universal gate-set, the KAK decomposition can yield a parameterized circuit, which to can instantiate any two-qubit unitary. Therefore, applying the KAK decomposition to retarget a circuit’s gate-set is also possible. Once a template is discovered in the desired gate-set, it can be utilized similarly to the optimization procedure to convert grouped gates to gates of a different type. However, producing a circuit template when designing a new gate-set may be nontrivial.

Recently, bottom-up approaches to quantum synthesis have been successful through numerical instantiation [7], [8], [9], [10], [11], [17]. Rather than fixed mathematical identities, these techniques employ a numerical optimizer to closely approximate a solution to the instantiation problem. This is done by minimizing a cost function, often the unitary error or distance between the circuit’s unitary and a target unitary. This is given by the following formula using the same notation as before.

$$\Delta(C(\alpha), V) = 1 - \frac{|\text{tr}(V^\dagger C(\alpha))|}{N}$$

Other variations of this distance function include:

$$\Delta_f(C(\alpha), V) = 1 - \frac{\text{Re}(\text{tr}(V^\dagger C(\alpha)))}{N}$$

and

$$\Delta_p(C(\alpha), V) = \sqrt{1 - \frac{|\text{tr}(V^\dagger C(\alpha))|^2}{N^2}}$$

All three methods have a range of $[0, 1]$, and as they approach zero, the circuit’s unitary approaches $V$. For the rest of our paper, we refer to the unitary distance or error as $\Delta$, the first formulation.
Bottom-up synthesis methods build up the parameterized circuit by iteratively placing more gates. At every step, they instantiate the parameters using numerical optimizers and claim a solution when the error is less than some $\epsilon$ threshold. For example, QSearch [7] phrases the synthesis problem as a search over circuit templates, instantiating candidates as it searches over them. QFAST [8] expands on this by conflating the search and numerical optimization using a unique circuit encoding. In the NACL [9] algorithm, machine learning methods are used alongside instantiation to synthesize noise-aware circuits. SQUANDER [11] takes a more direct approach to bottom-up synthesis. Here the circuit template is grown and re-instantiated iteratively until a solution is found, at which point, the circuit is then compressed into its optimal form. In [17], instantiation is used in a similar bottom-up approach to produce approximate circuits. More recently, the optimization space of instantiation has been studied and a hypertuned synthesis algorithm, CPFlow [12], has been built. Lastly, in Quartz [18], a similar method to instantiation is employed to dynamically construct circuit substitution rules for any environment.

Several compilation algorithms have leveraged the high quality of results produced during bottom-up synthesis. QGo [13] combined circuit partitioning with synthesis to create a circuit mapping and optimization procedure. QUEST [19] uses similar techniques to produce robust and resource-efficient approximate circuits. The growth of algorithms using numerical instantiation has been a motivation for BQSKit [6] developers to build a Python framework around instantiation.

III. NUMERICAL INSTANTIATION-BASED ALGORITHMS

Numerical instantiation is a powerful tool for restructuring circuits in non-intuitive ways leading to circuit optimizations likely unattainable by rule-based applications. Many synthesis algorithms have utilized it for high-quality circuit construction through some variation of the bottom-up loop described in Figure 2a. We have found small changes to this loop can yield a strategy for modifying already existing circuits, see Figure 2b. We demonstrate this strategy by building two algorithms, a circuit optimization algorithm and a gate-set retargeting algorithm.

A. Gate Deletion

The most straightforward way to use the transformation loop described in Figure 2b is to remove gates from a circuit. This gate deletion process can be done by selecting a gate or group of gates to remove and then instantiating the parameters to the remaining gates to accommodate the loss in accuracy. See Figure 3 for an illustration.

It is not always guaranteed that the result from deleting a gate will be an acceptable solution to the target unitary. This is partially because not all circuits can implement all unitaries. It may be the case that removing a gate ensures the remaining gates can never implement the original target, and therefore, even an ideal instantiation tool will never find an acceptable solution. Gate deletion can also be fallible because the circuit space is extremely high dimensional, and the optimizers can get stuck in local minima. To combat this, one can use multi-start optimization [20] strategies during instantiation.

B. Optimization Algorithm

We need a methodology to select candidate gates for removal to use gate deletion in an optimization algorithm. For the same reasons mentioned previously, different strategies will lead to different results. Additionally, an algorithm’s runtime is directly related to the number of times instantiation is performed.

At one end of the spectrum, we have exhaustive search procedures that scale exponentially with the number of gates in the starting circuit: the method will find the optimal result. This can be accomplished by first attempting to remove each gate individually and then repeating this step on all circuits that successfully removed a gate.

At the other end of the spectrum, a linear complexity method will consider deleting each gate only once. A gate that failed to be removed will never be reconsidered. Assuming that we have an ideal oracle instantiator, this approach will also find the optimal result in many cases. However, in practice we often find that order of deletion matters: after removing a gate, re-evaluating the removal of a previously considered gate can lead to a successful deletion. Two observations explain this behavior: 1) the instantiation problem is challenging to existing numerical optimizers; and 2) the newer problem is different and it has lower dimensionality, leading to fewer local minima.

Our deletion algorithm uses a middle-ground approach where we iteratively scan the circuit using a linear strategy: in each scan we attempt to delete each gate only once. The algorithm stops when no more gates can be deleted subject to the $\Delta$ accuracy convergence criteria requested by the user. Algorithm 1 provides pseudocode for this method.

This algorithm can work on any circuit with any gate-set because it only relies on numerical instantiation and not fixed rules. It can also work on multi-level systems such as qutrits. Furthermore, gate deletion will only ever remove gates, which implies it can be run on a routed circuit without the worry of ruining the routing.

C. Gate-Set Transpilation

Another use of the transformation loop described in Figure 2b is to substitute gates with different ones. Instead of deleting a gate, we can remove and replace a gate or group of gates with another gate or group of gates.

We propose a gate-set transpilation algorithm based on gate substitution using numerical instantiation. This works by iteratively replacing gates from one gate-set with gates from a target set. Since single-qubit gates can always be grouped and decomposed into gates from any universal gate-set trivially, we focus on two-qubit gates in this algorithm.

First, we group together consecutive two-qubit interactions (gates) that act on the same two qubits. These interactions will be replaced with gates in the new gate-set, one at a time in a left-to-right sweep over the circuit. Note that
Fig. 2: Instantiation is the core subroutine in all bottom-up circuit synthesis algorithms. The standard bottom-up loop (left) is to create an initial circuit template guess then continue to instantiate and extend it until an acceptable solution is found. Through a slight modification to this flow, instantiation can also be used to transform or optimize a quantum circuit (right). Instead of extending a circuit template like in bottom-up synthesis, we reduce or transform a circuit template and continue until it is no longer successful or necessary.

Algorithm 1 Iterative Scanning Gate Removal

1: $C \leftarrow \text{input circuit}$
2: $\epsilon_t \leftarrow \text{acceptable error threshold}$
3: $U_t \leftarrow \text{the unitary implemented by } C$
4: $N \leftarrow \text{the number of gates in } C$
5: $M \leftarrow 0$
6: while $N \neq M$ do
7:     for $g \in C$ do
8:         Remove $g$ from $C$
9:         $C, \epsilon \leftarrow \text{instantiate}(C, U_t)$
10:        if $\epsilon > \epsilon_t$ then
11:            Place $g$ back into $C$
12:        end if
13:     end for
14:     $M \leftarrow N$
15:     $N \leftarrow \text{the number of gates in } C$
16: end while

existing compilers use a similar strategy of forming a new generic two-qubit gate that is subsequently transpiled using either KAK decomposition or some other prescribed rule-based transformations. When introducing new two-qubit gates it may be non trivial to derive rules for transpiling from one source gate to the newly introduced one.

Once a generic two-qubit gate is formed, our approach is based on the results from Bremner et al. [21] which shows that any two-qubit unitary can be represented by a short sequence of single qubit gates and arbitrary two-qubit entangling gates: the upper bound on two-qubit entangling gates required can be easily calculated based on the single qubit gate set. This is the first main intuition behind our approach. The second intuition is that we can search over the space of these representations during instantiation.

Thus, we attempt to replace each generic interaction found at the first step with a series of templates created using gates in the new target gate-set. This collection is an enumeration of circuits starting with depth zero and ranging to an upper depth bound determined using [21]. Figure 4 illustrates four templates with zero to three two-qubit gates in its place. If a generic two qubit unitary can be implemented with fewer than $N$ (three) gates in the new gate-set, this information can be used to reduce the number of candidate solutions instantiated, see Figure 4. The results in this paper are obtained with the four shown templates.

The retargeting procedure is simple. We take the circuit in its original gate set and start traversing it, e.g. left to right. At each step, we replace a grouped two-qubit interaction from the circuit with all of the possible templates and reinstantiate. At each step of the algorithm, we have a collection of circuits equal to the number of template possibilities. Each of these circuits is composed of a prefix in the new gate set and a suffix in the original gate set. After instantiation, we select

Fig. 3: Gates can be removed from circuits through the use of instantiation. This can be done by first selecting and removing a gate, then instantiating the remaining gates’ parameters to make up for the loss. This is not always successful. If the error on the new circuit is less than some threshold then the new circuit is accepted, otherwise the circuit is rejected.
When using our retargeting algorithm, each gate from the old gate-set is replaced with templates containing new gate types. In the generic case, we use four templates with zero to three two-qubit gates. However, if we don’t need all four templates, as in the case with some gates, we can reduce the number of candidate solutions instantiated improving runtime.

This retargeting algorithm is advantageous to rule-based or KAK-based retargeting algorithms for a few reasons.

The second advantage is this algorithm’s ease-of-use. Retargeting algorithms that rely on KAK decompositions or circuit identities require users to gather and input rules. Often when working with uncommon gate-sets, these rules can become difficult to produce. Numerical instantiation in this optimization algorithm removes the need to identify rules, enabling it to support any circuit without restriction.

Lastly, this algorithm can easily be adapted to target gate-sets with multiple two-qubit gates. To accomplish this, one can generate an additional set of candidate circuits for each additional two-qubit gate. Then after instantiation, the shortest acceptable circuit would be selected dynamically picking the gate providing the shortest implementation for each interaction.

D. Partitioning and Scalability

Since methodologies that use numerical instantiation scale exponentially with the size of the system being instantiated, we employ the circuit partitioning procedure described by Wu et al [13] to ensure competitive performance and scalability, see Figure 6. For large circuits, we partition in smaller blocks which we can optimize (delete gates) or transpile directly, transform the blocks and reassemble the original circuit.

There is a trade-off present with the size of partitions. One advantage of our optimization and translation algorithm is the ability to change non-local operations when instantiating. Whenever we partition a circuit and restrict numerical instantiation within each block, we reduce the amount of non-local operations considered. Also, the partition size chosen determines the size of unitary matrices, and a larger matrix will lead to exponentially longer runtimes. With both algorithms, larger block sizes will likely lead to better quality results but smaller block sizes will complete quicker. In this work we evaluate forming only blocks of three and four qubits.

### Algorithm 2 Numerical Retargeting Algorithm

| Line | Description |
|------|-------------|
| 1    | \( C \leftarrow \) input circuit |
| 2    | \( \epsilon_t \leftarrow \) acceptable error threshold |
| 3    | \( U_t \leftarrow \) the unitary implemented by \( C \) |
| 4    | \( G_t \leftarrow \) initial gate set |
| 5    | \( G_t \leftarrow \) target gate set |
| 6    | \( n \leftarrow \) max number of replaced gates per interaction |
| 7    | \( \text{while } \exists g \in G_t, \text{ s.t. } g \in C \) do |
| 8    | \( \text{Group } g \text{ with neighbor gates} \) |
| 9    | \( C_{\text{candidates}} = \{ \} \) |
| 10   | \( \text{for } j \in G_t \) do |
| 11   | \( \text{for } i \in \{0, 1, \ldots, n\} \) do |
| 12   | \( h \leftarrow \) block with \( i \) gates of type \( j \) |
| 13   | \( C_c \leftarrow \) with \( g \) replaced with \( h \) |
| 14   | Push \( C_c \) on \( C_{\text{candidates}} \) |
| 15   | \( \text{end for} \) |
| 16   | \( \text{end for} \) |
| 17   | \( C_{\text{success}} = \{ \} \) |
| 18   | \( \text{for } C_c \in C_{\text{candidates}} \) do |
| 19   | \( C_c, \epsilon \leftarrow \) instantiate(\( C_c, U_t \)) |
| 20   | \( \text{if } \epsilon \leq \epsilon_t \) then |
| 21   | Push \( C_c \) on \( C_{\text{success}} \) |
| 22   | \( \text{end if} \) |
| 23   | \( \text{end for} \) |
| 24   | \( C \leftarrow \) shortest circuit from \( C_{\text{success}} \) |
| 25   | \( \text{end while} \) |

IV. EXPERIMENTAL SETUP

Both optimization and retargeting algorithms are implemented using the BQSKit framework [6], and have been recently integrated into the main BQSKit package available at https://github.com/bqskit/bqskit. We evaluated them with Python 3.8.10 on a 64-core AMD Epyc 7702p sys-

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**Fig. 4:** When using our retargeting algorithm, each gate from the old gate-set is replaced with templates containing new gate types. In the generic case, we use four templates with zero to three two-qubit gates. However, if we don’t need all four templates, as in the case with some gates, we can reduce the number of candidate solutions instantiated improving runtime.

| Generic Portable Templates |
|----------------------------|
| ![Generic Portable Templates](image1) |

| Gate Specific Templates |
|-------------------------|
| ![Gate Specific Templates](image2) |
Fig. 5: Instantiation can be used to convert gates from one type to another. This can be done by replacing the desired gate with a sequence of other gates and reinstantiating. Since this is not guaranteed to find a solution, we try a few different gate sequences, each one longer than the last. By default, we create 4 different sequences with 0, 1, 2, and 3 gates from the new gate-set respectively. After instantiating, we select the successful circuit with the fewest number of gates.

Fig. 6: The original circuit on the left is partitioned into blocks containing three qubits. This will group together consecutive gates acting on the same three-qubits. This allows algorithms making use of numerical instantiation to scale to very large circuits.

We used a benchmark suite consisting of real quantum algorithms of various different types and ranging in size from 5 to 64 qubits. There are multiplication and addition arithmetic circuits in the suite since they are commonly used to compare optimizing compilers [13], [22]. Generated arithmetic circuits also tend to have ladders of two-qubit gates without single-qubit operations in between, which is valuable to test against. These circuits are known to be sub-optimal. Additionally, we have a couple of variational quantum algorithms in our benchmark suite. Two circuits using the Quantum Approximate Optimization Algorithm (QAOA) [2] to solve the MaxCut problem with the hardware efficient ansatz [23]. Three circuits are simulating a spinful Hubbard model generated with the Bravyi-Kitaev mapping [24], [25]. We include a Grover...
circuit generated with Qiskit's algorithm library [26]. Lastly, we include four time evolution circuits, two for Transverse Field Ising Models (TFIM) [27] and two for Transverse Field XY (TFXY) models. These circuits were generated by the constant-depth F3C++ compiler [28] and are believed to be the best known implementations. The benchmarks are listed in Figure 7 alongside their gate counts.

B. Verification

We fully verified the results of our algorithms in two ways. For circuits that were simulatable in size, we directly calculated the unitary error. All these circuits had a total error lower than $10^{-10}$, with a majority having zero error. For circuits that were unable to be directly simulated, we first partitioned the circuit into large simulatable sections. We then ran the algorithms within these sections, further partitioning to employ numerical instantiation as necessary. After the algorithms finished, we then directly computed the error of each section and calculated the theoretical upper-bound on process distance by summing them together [19], see Figure 8. Section size matters when using this verification process. As the section size approaches the size of the circuit, the error upper-bound becomes more accurate.

For example with the 60-qubit multiplier circuit, there were 2150 three-qubit blocks. After running our optimization algorithm, summing the error on these small blocks gives an upper-bound of $9.97 \times 10^{-11}$; whereas, if we first partition the circuit into 8-qubit sections and use these to calculate the upper-bound, we get $2.61 \times 10^{-11}$. If we further increase the section size, it is likely the upper-bound will decrease more.

For all circuits, the total distance error $\Delta < 10^{-10}$ when partitioning in three-qubit blocks. As simulating large circuits is computationally intensive, we have performed the coarse grained procedure only for selected candidates to confirm the intuition that the error upper bound is indeed loose and the resulting circuits are accurate.

Fig. 8: By partitioning large circuits into simulatable sections, we can calculate an upper-bound on error by summing together the individual section errors. As the section size increases, the upper-bound becomes more accurate.

V. Evaluation

A. Optimization Algorithm

The optimization algorithm is directly compared against Qiskit, Cirq, and Tket. Additionally, we include data from optimizing circuits after running them with the aforementioned tools, which are labeled “+Qiskit”, “+Cirq”, and “+Tket”. The execution times and percent of gates reduced are plotted in Figure 9. When run stand-alone and compared against compilers, our algorithm is able to improve on single-qubit gate count for 50% of inputs, and on two-qubit gate count on 8% of the inputs. When run after other tools, the optimizer produces shorter circuits in all cases, removing on average another 5% of the two-qubit gates. When run together with either Qiskit or Tket, there was a reduction in two-qubit gate counts discovered in the TFIM circuits that was not possible with any individual optimizer.

This behavior is explained by the interaction between original input circuit depth and partitioning: longer inputs form more partitions, with some loss of optimization potential at boundaries. Partition size further affects the quality of the optimization: larger partitions provide better opportunity for optimization at the expense of execution time.

For example, the 4-qubit Hubbard model was the only circuit directly optimized without partitioning. This led to a 78% reduction in CNOTs and a 86% reduction in single-qubit gates, but required the longest compile time at 5728.9 seconds. The best result from the other compilers was only a 13% reduction in CNOT counts for the same circuit. This illustrates the trade-off with partitioning for scalability. By using larger blocks in partitioning or directly optimizing the circuit, we allow instantiation to consider more non-local interactions leading to a better optimization at the cost of runtime.

B. Retargeting Algorithm

The retargeting algorithm was evaluated by converting the benchmark circuits to gate-sets that exist in hardware today: AQT and Rigetti’s CZ gate [29], [30], Honeywell’s ZZ gate [31], IonQ XX gate [32], and Google’s Sycamore and √SWAP [33] gate. For each gate-set, we compared directly to compilers that support that gate-set. Neither Qiskit, Cirq, nor Tket support ZZ gate decomposition out-of-the-box, so we compared to the theoretical rule that translates 1 CNOT to 1 ZZ gate. The ratio of final two-qubit gate counts to initial
two-qubit gate counts is plotted alongside execution times for the different benchmarks and compilers in Figure 10.

The numerical instantiation based retargeting algorithm was able to translate circuits into new gate-sets using fewer two-qubit gates in all but one case. Google’s Cirq was able to produce the 12-qubit Hubbard circuit in Sycamore Gates with 0.35% fewer gates than this algorithm.

When converting to CZ gates, all the other compiler produced roughly the same quality of result in roughly the same time. Our algorithm produced circuits with an average of 8% fewer CZ gates and up to 32% fewer CZ gates on the four-qubit Hubbard circuit.

Qiskit and Cirq used a one-to-one rule to convert CNOT gates to XX gates, but did not optimize much past that. When compared our algorithm produced gates with 10% fewer XX gates on average and a maximum of 30% fewer gates for the four-qubit Hubbard circuit.

In most cases we were able to beat the one-to-one rule for ZZ gates significantly with an average of improvement of 10%. In the case of the four-qubit Hubbard model, we produced a result with 32% fewer ZZ gates in the translated circuit versus CNOT gates in the input circuit.

Converting to $\sqrt{iSWAP}$ and Sycamore gates was only supported by Cirq, and these do not have a one-to-one rule to convert between CNOTs. Our algorithm produced circuits with 11% fewer $\sqrt{iSWAP}$ gates and 29% fewer Sycamore gates. In some cases the difference between Cirq and our rebasings was quite significant. For example, the 64-qubit TFXY circuit compiled with our tool produced a circuit with 3970 sycamore gates, whereas Cirq produced a circuit with 8064 sycamore gates.

Our algorithms relied on numerical instantiation rather than analytic methods, and as a result, we experienced a 14× slowdown on average. The maximum slowdown for retargeting was compiling the 9-qubit adder to the $\sqrt{iSWAP}$ gate which took a total of 56.46 seconds. The longest partitioned optimization execution was 1650.61 seconds for the 60-qubit multiply circuit.

C. Comparison of Gate-sets

The transpiled circuits are informative about the efficacy of different gate-sets across the algorithms. In Figure 11, we plot the final gate count as ratios to the original gate counts for all gate-sets. We also include the benchmarks compiled to a gate-set including both $\sqrt{iSWAP}$ and the Sycamore gate.

In every case, circuits including the $\sqrt{iSWAP}$ or Sycamore gates required more gates than with the others. However, not all gates are equal. The Sycamore gate is executed in 12ns on Google’s hardware, where the CZ gate requires 24ns [16]. In all cases, circuits in the Sycamore gate set required less than twice the number of CZs gates. This implies that, although the total circuit depth is greater in the Sycamore gate set, the total execution time and potentially decoherence may be less. This is especially true in the time evolution circuits, where the same amount gates were required regardless of the type.

We also tried to test whether using more than one two-qubit gate is beneficial and compiled targeting both $\sqrt{iSWAP}$ and Sycamore gates. The results are not conclusive, but it is probably premature to abandon this line of inquiry. It may be the case that further tuning of our algorithm or other approaches may improve on circuit quality.

D. Tuning the Algorithms

Throughout the evaluation, we ran our algorithms configured for four multi-starts and partitioned them into three-qubit blocks. While this is a recommended default and seems to produce good results, we can also trade circuit quality for execution speed: 1) bound the number of iterations during the optimization pass to improve execution speed; 2) configure for faster but “inferior” numerical optimization; and 3) increase circuit quality with bigger partitions/blocks at the expense of execution time.

The initial implementation of the mu160 circuit contains 11405 CNOT gates and 23666 single qubit gates. With the default configuration, we optimized the 60-qubit multiplier circuit to 10798 CNOTs and 15384 single-qubit gates in 1650.61 seconds. When dialing the algorithm to improve performance at the cost of quality by using only one multi-start and only sweeping the circuit once during gate deletion we obtain 10865 CNOTs and 15765 single-qubit gates in only 119.82 seconds. This is about a 13× speed-up at the cost of 0.6% in quality.

Similarly, we can configure the block width used during partitioning and the number of multi-starts for each instantiation when tuning the retargeting algorithm. With the same configuration used for other circuits, we produced a 60-qubit multiplier circuit with 12472 $\sqrt{iSWAP}$ gates in 2045.45 seconds. If we increase the block width to four from three, we get 11746 $\sqrt{iSWAP}$ gates in 6043.13 seconds. This configuration gives a 5.8% improvement in quality with 3× execution time increase.

VI. DISCUSSION

The retargeting algorithm proposed improves upon state-of-the-art techniques in both portability and quality, while the proposed optimization algorithm is competitive and augments well existing compilation workflows. Overall, the results are very encouraging for the adoption of numerical instantiation algorithms in compilers. We consider instantiation a good middle ground between “peephole” compilers and full-blown circuit synthesis: 1) it is more computationally intensive than compilers, but also able to improve circuit quality; 2) it has linear complexity when compared to the exponential complexity of full synthesis.

We have shown how the algorithms can be tuned to execute in a time comparable to a traditional optimizing compiler. We note that further performance improvements are attainable through parallelization and exploiting GPU hardware. For the large circuits, partitioning results in an embarrassingly parallel problem easy to solve in distributed memory settings.
Current state-of-the-art numerical instantiators rely on CPU-based optimization routines. There is a lot of active work efficiently simulating quantum circuits on GPUs [34], which could be valuable to getting instantiators running on GPUs. Moving to GPUs may significantly speed up algorithms while also improving quality by batching more multi-starts.

The algorithms can also be adapted to process multiple gates or interactions in parallel. For example, instead of considering one two-qubit interaction at a time in the retargeting algorithm, we could attempt to change two or more interactions in every instantiation call. This change would reduce the total number of instantiation calls but potentially affect the quality.

One practical question is where to place instantiation in a complete compilation workflow. Throughout our evaluations, we performed the algorithms on the reference circuits as they came and we never considered mapping or routing the initial inputs. Since both algorithms respect the logical connectivity of the input circuit, i.e., they never introduce a new gate on a pair of qubits not interacting in the input, they could be run post-routing. Furthermore, circuits with SWAP gates introduced during routing may benefit from our retargeting algorithm. Instead of applying the one-to-three SWAP gate conversion to CNOTs, which most compilers use, our retargeting algorithm can be run post-routing. Additionally, circuits with SWAP gates on a pair of qubits not interacting in the input, they could get removed during optimization.

VII. CONCLUSIONS

In this work, we introduced and surveyed parameterized circuit instantiation and presented two numerical instantiation-based compiler algorithms for circuit optimization and gate-set transpilation. We demonstrated the tunability of our algorithms and verified our procedures using an error bound on very large circuits. Overall, these algorithms performed well and are a valuable addition to existing and new quantum compiler tools.

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REFERENCES

[1] Jarrod R McClean, Jonathan Romero, Ryan Babbush, and Alán Aspuru-Guzik. The theory of variational hybrid quantum-classical algorithms. New Journal of Physics, 18(2):023023, 2016.
[2] Edward Farhi, Jeffrey Goldstone, and Sam Gutmann. A quantum approximate optimization algorithm. arXiv preprint arXiv:1411.4028, 2014.
[3] Qiskit Developers. Qiskit: An Open-source Framework for Quantum Computing, January 2019.
[4] Cirq Developers. Cirq, August 2021. See full list of authors on Github: https://github.com/quantumlib/Cirq/graphs/contributors.
[5] Seyon Sivarajah, Silas Dilkes, Alexander Cowtan, Will Simmons, Alec Edgington, and Ross Duncan. t—ket2: a retargetable compiler for nisq devices. Quantum Science and Technology, 6(1):014003, 2020.
[6] Ed Younis, Costin C Iancu, Wim Lavrijsen, Marc Davis, Ethan Smith, et al. Berkeley quantum synthesis toolkit (bqskit) v1. Technical report, Lawrence Berkeley National Lab.(LBNL), Berkeley, CA (United States), 2021.
[7] Marc G Davis, Ethan Smith, Ana Tudor, Koushik Sen, Irfan Siddiqi, and Costin Iancu. Towards optimal topology aware quantum circuit synthesis. In 2020 IEEE International Conference on Quantum Computing and Engineering (QCE), pages 223–234. IEEE, 2020.
[8] Ed Younis, Koushik Sen, Katherine Yelick, and Costin Iancu. Qfast: Conflating search and numerical optimization for scalable quantum circuit synthesis. In 2021 IEEE International Conference on Quantum Computing and Engineering (QCE), pages 232–243. IEEE, 2021.
[9] Lukasz Cincio, Kenneth Rudinger, Mohan Sarovar, and Patrick J Coles. Machine learning of noise-resilient quantum circuits. PRX Quantum, 2(1):010324, 2021.
[10] Péter Raktya and Zoltán Zimborás. Approaching the theoretical limit in quantum gate decomposition, 2021.
[11] Péter Raktya and Zoltán Zimborás. Efficient quantum gate decomposition via adaptive circuit compression, 2022.
[12] Nikita A Nemkov, Evgeniy O Kitkenko, Ilia A Luchnikov, and Alexey K Fedorov. Efficient variational synthesis of quantum circuits with coherent multi-start optimization. arXiv preprint arXiv:2205.01121, 2022.

Fig. 9: The number of gates removed by different optimization algorithms as well as their runtime across a variety of different benchmarks. The number of gates removed are broken down into single-qubit and two-qubit gates removed. Additionally, the total number of gates removed are plotted. In some cases, more gates were added during optimization than removed, which is because some optimizers will prioritize two-qubit gates over single-qubit gates.
Fig. 10: Retargeting algorithm efficiencies and runtime across a variety different benchmarks. On the left, the ratio of final two-qubit gates to initial two-qubit gates is plotted for 5 different gate sets found in existing hardware. On the right, execution times for the different retargeting algorithms are plotted.

Fig. 11: A comparison between all the gate-sets for each circuit produced with our instantiation-based algorithm.
[13] Xin-Chuan Wu, Marc Grau Davis, Frederic T. Chong, and Costin Iancu. Reoptimization of quantum circuits via hierarchical synthesis. In 2021 International Conference on Rebooting Computing (ICRC), pages 35–46, 2021.

[14] Robert R Tucci. An introduction to cartan’s kak decomposition for qc programmers. arXiv preprint quant-ph/0507171, 2005.

[15] Teague Tomesh, Pranav Gokhale, Victory Omole, Gokul Subramanian Ravi, Kaijin N Smith, Joshua Viszlai, Xin-Chuan Wu, Nikos Hardavellas, Margaret R Martonosi, and Frederic T Chong. Supermarq: A scalable quantum benchmark suite. arXiv preprint arXiv:2202.11045, 2022.

[16] Google devices. https://quantumai.google/cirq/google/devices. Accessed: 2022-04-29.

[17] Liam Madden and Andrea Simonetto. Best approximate quantum compiling problems. ACM Transactions on Quantum Computing, 3(2), mar 2022.

[18] Mingkuan Xu, Zikun Li, Oded Padon, Sina Lin, Jessica Pointing, Auguste Hirth, Henry Ma, Jens Palsberg, Alex Aiken, Umut A Acar, et al. Quartz: superoptimization of quantum circuits. In Proceedings of the 43rd ACM SIGPLAN International Conference on Programming Language Design and Implementation, pages 625–640, 2022.

[19] Tirthak Patel, Ed Younis, Costin Iancu, Wibe de Jong, and Devesh Tiwari. Quest: systematically approximating quantum circuits for higher output fidelity. In Proceedings of the 27th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, pages 514–528, 2022.

[20] Jeffrey Larson and Stefan M. Wild. Asynchronously parallel optimization solver for finding multiple minima. Mathematical Programming Computation, 10(3), 2 2018.

[21] Michael J. Bremner, Christopher M. Dawson, Jennifer L. Dodd, Alexei Gilchrist, Aram W. Harrow, Duncan Mortimer, Michael A. Nielsen, and Tobias J. Osborne. Practical scheme for quantum computation with any two-qubit entangling gate. Physical Review Letters, 89(24), nov 2002.

[22] Steven A Cuccaro, Thomas G Draper, Samuel A Kutin, and David Petrie Moulton. A new quantum ripple-carry addition circuit. arXiv preprint quant-ph/0410184, 2004.

[23] Abhinav Kandala, Antonio Mezzacapo, Kristan Temme, Maika Takita, Markus Brink, Jerry M Chow, and Jay M Gambetta. Hardware-efficient variational quantum eigensolver for small molecules and quantum magnets. Nature, 549(7671):242–246, 2017.

[24] Sergey B Bravyi and Alexei Yu Kitaev. Fermionic quantum computation. Annals of Physics, 298(1):210–226, 2002.

[25] John Hubbard. Electron correlations in narrow energy bands. Proceedings of the Royal Society of London. Series A. Mathematical and Physical Sciences, 276(1365):238–257, 1963.

[26] Lov K Grover. A fast quantum mechanical algorithm for database search. In Proceedings of the twenty-eighth annual ACM symposium on Theory of computing, pages 212–219, 1996.

[27] Dongbin Shin, Hannes Hübscher, Umberto De Giovannini, Hosub Jin, Angel Rubio, and Noejung Park. Phonon-driven spin-fluqet magneto-valleytronics in mos₂. Nature Communications, 9(1):638, 2018.

[28] Lindsay Bassman, Roel Van Beeumen, Ed Younis, Ethan Smith, Costin Iancu, and Wibe A de Jong. Constant-depth circuits for dynamic simulations of materials on quantum computers. Materials Theory, 6(1):1–18, 2022.

[29] Bradley K Mitchell, Ravi K Naik, Alexis Morvan, Akel Hashim, John Mark Kreikebaum, Brian Marinelli, Wim Lavrijsen, Kasra Nowrouzi, David I Santiago, and Irfan Siddiqi. Hardware-efficient microwave-activated tunable coupling between superconducting qubits. Physical review letters, 127(20):200502, 2021.

[30] Gates and instructions. https://pyquil-docs.rigetti.com/en/v2.7.0/apidocs/gates.html. Accessed: 2022-04-29.

[31] Juan M Pino, Jennifer M Dreiling, Caroline Figgatt, John P Gaebler, Steven A Moses, CH Baldwin, M Foss-Feig, D Hayes, K Mayer, C Ryan-Anderson, et al. Demonstration of the qccd trapped-ion quantum computer architecture.

[32] Klaus Mølmer and Anders Sørensen. Multiparticle entanglement of hot trapped ions. Phys. Rev. Lett., 82:1835–1838, Mar 1999.

[33] Frank Arute, Kunal Arya, Ryan Babbush, Dave Bacon, Joseph C Bardin, Rami Barends, Ryan Biswas, Sergio Boixo, Fernando GSL Brandao, David A Buell, et al. Quantum supremacy using a programmable superconducting processor. Nature, 574(7779):505–510, 2019.