5.2.4 Radiation Hardness Testing for Electronics against High Energy Ions

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The mechanisms of Single Event Effects (SEEs) on Silicon Carbide (SiC) power devices are becoming clearer. However, to completely understand the mechanisms of SEEs on SiC power devices and to explore radiation hardened technologies for SiC power devices, it is necessary to study the radiation response of SiC power devices using high-energy heavy ions at accelerator facilities such as the Heavy Ion Medical Accelerator in Chiba (HIMAC). The radiation hardening test methodology using high energy heavy ions is reviewed and the application of HIMAC for SEE testing is introduced with recent results from tests of SiC power devices.

Key Words: HIMAC (Heavy Ion Medical Accelerator in Chiba), high energy ion, silicon carbide, single event effect

1. Introduction

Semiconductor devices are indispensable components of satellites. These semiconductor devices are exposed to a variety of radiation effects such as γ-rays, electrons, protons, and heavy ions, each having a wide range of energies in space, and radiation-induced malfunctions are known to occur. Therefore, both high reliability and radiation tolerance are required for semiconductor devices for use in space.

Radiation effects on semiconductor devices can be categorized into three types, Total Ionizing Dose (TID) effects, Displacement Damage Dose (DDD) effects and Single Event Effects (SEEs). TID and the DDD effects result in functional degradation due to cumulative radiation damage of devices caused by electrons, photons and γ-rays from the radiation belts and the solar wind. Therefore, these TID and DDD effects are a significant issue for devices in Earth orbit.1)

TID involves positive charge creation in gate oxides near the oxide-semiconductor interface devices due to ionization by protons, heavy ions and γ-rays. These charges act as a fixed charge in the oxide and produce a potential within the device. Thus, the threshold voltage of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) is shifted from the nominal voltage. DDD is defined as a material performance degradation due to point defect creation in semiconductor crystals by incident energetic particles. A power efficiency degradation for solar panels and a gain depression of bipolar transistors are well known DDD phenomena.

SEEs are defined as a transient disturbance of de-
vice operation or instantaneous malfunctions of devices due to an unintentional flow of charge induced by single heavy ions incident on the device. Heavy ions create electron hole pairs (e-h pairs) along the ion track in the materials by ionization. The amount of ion-induced charge in depends on the ionization energy loss, or linear energy transfer (LET) of the ions in device materials, and the LET depends on the ion mass and the energy of ions. Therefore, for estimation of SEE tolerance, exposure to a wide variety of high energy ions is required.2)

In this section, we review the SEE hardening test methodology using high energy heavy ions. Then, we show our latest SEE test results obtained from silicon carbide (SiC) power devices at HIMAC (Heavy Ion Medical Accelerator in Chiba).

2. Single Event Effects

The SEEs are divided into several modes according to results of events. For example, the well known Single Event Upset (SEU) manifests as a bit flip of memory devices by radiation induced charge. This upset itself does not damage not only for device materials device functional performance. Thus, the devices can recover from bit flip errors by resetting memory.

Destructive events induced by single ions are also categorized as SEEs. The flow of an ion induced charge (current flow) raises the temperature of a small region along the path of the current flow. The heat damages the materials of devices physically, and the devices eventually lose their functionality. These destructive SEEs are additionally divided into several modes according to the size of the affected area in the device. Single Event Gate Rupture (SEGR) and Single Event Burnout (SEB) are two well-known destructive SEEs. A SEGR destroys the ability of the gate to regulate current flowing from the source to the drain by permanently damaging the gate insulator (SiO₂) layer on MOSFETs. A SEB, on the other hand, dose not damage the insulator but shorts the source to the drain of MOSFETs.3)

SiC is regarded as a promising candidate for high radiation tolerance devices, since amounts of charge induced in SiC by ions are about 2 times smaller than the silicon (Si) used in conventional semiconductor devices. In addition, SiC can endure an electric field about eight times higher than Si before exhibiting avalanche breakdown, which is known as a trigger of SEB. Recently, commercially available SiC power devices such as MOSFETs and Schottky Barrier Diodes (SBDs) have been released commercially. It is known that the risk of SEB increases with increasing applied bias voltage, and the higher breakdown electric field for SiC allows the operation of SiC devices with higher voltage than Si devices. Therefore, it is necessary to explore the radiation hardness of SiC.

3. SEE Testing with High Energy Heavy Ions

3.1 High Energy Heavy Ions and Semiconductor Devices

Fig. 1 shows the number of heavy ions in space per area per second as a function of integrated LET of ions in space in units of MeV·cm²/mg. There is
an altitude dependence of number of heavy ions at lower LET of 0.5 MeV·cm²/mg. The most notable aspect of this data is that the number of ions having LET of higher 40 MeV·cm²/mg decreases sharply.⁴)

The LET dependence of SEU cross-sections (essentially the probability) show saturation in general, as shown in Fig. 2. The saturated value corresponds to the size of the SEU-sensitive area in the device. Therefore, the SEU cross-section at an LET value of 40 MeV·cm²/mg is used as a criterion of SEU tolerance. At the same time, ions used for testing have to penetrate the sensitive region of the devices. For SEE testing for devices having an active region of less than about 30 µm from the surface of devices, accelerators available in Japan include the K=110 MeV cyclotron at Takasaki Ion Accelerators for Advanced Radiation Application (TIARA) at the National Institutes for Quantum and Radiological Science and Technology (QST), Takasaki, Japan. As shown in Table 1, we can use a wide variety of ions for SEU testing, although the testing should be in a vacuum chamber. (Ions do not have enough penetration depth in air.⁵) The LETs and ranges can be obtained by SRIM estimation.⁶ The cyclotron at the Cyclotron Radioisotope Center (CYRIC), Tohoku University, Sendai, Japan, is also available for SEU testing. The ion species available at CYRIC are shown in Table 2.⁷

For SEE testing of devices having an active region of more than about 30 µm from the surface of devices, heavy ion energies up to several hundred GeV/particle are needed to penetrate the sensitive region of devices. Few accelerators in the world can accelerate ions to hundreds of GeV/particle. One of these is the Heavy Ion Medical Accelerator in Chiba (HIMAC), QST, Japan.⁸ As shown in Table 3, a wide variety of ions with sufficiently high energies are available at HIMAC.

![Fig. 2 An example of the LET dependence of SEU cross-sections. Generally, the saturated value corresponds to the SEU sensitive area size of the device.](image)

| Ion | Energy [MeV] | Range in Si, SiC [µm] | LET in Si, SiC [MeV·cm²/mg] |
|-----|--------------|-----------------------|-------------------------------|
| N   | 56           | 53, 36                | 3.4, 3.5                      |
| Ne  | 75           | 42, 28                | 6.3, 6.7                      |
| Ar  | 150          | 40, 26                | 15, 16                        |
| Kr  | 322          | 41, 27                | 40, 42                        |
| Xe  | 454          | 39, 26                | 70, 73                        |
| Os  | 490          | 37, 24                | 88, 94                        |
3.2 SEU Testing

As mentioned in the above section, the LET dependence of the SEU cross-section (probability) is typically measured in the case of SEU tolerance estimation for integrated circuit devices. The SEU cross-section is defined as a number of a data (bit) mismatches before and after one ion hit. Devices having a data pattern are irradiated with heavy ions with a constant ion flux around $10^4$ ions/cm$^2$·s. After the irradiation, the data pattern is compared with the data before irradiation. The ion fluence is controlled to prevent double bit flips, where a bit flips from $l_0$ to $l_1$ and flips again from $l_1$ to $l_0$. A large number of double flips occurring in a device during irradiation time makes it impossible to correctly estimate the SEU cross-section. The appropriate ion fluence can be estimated from the expected sensitive area size, since the saturated value corresponds to the size of the SEU sensitive area of the device.

From the obtained threshold LET, saturation cross-section, and rise of the cross-section curve, we estimate an error rate of the device in a specified space mission duration for a specified space radiation distribution. If the radiation tolerance is lower than what is acceptable, we can implement a radiation tolerant operation algorithm to the devices. The ions are also used for SEU mechanism research. Charge collection and transient current induced by heavy ions in a single MOSFET and a discrete device are measured.

3.3 SEGR and SEB Testing for SiC Devices

Responses of SEGRs and SEBs for Si power devices have also been studied. Recently the SEGR and SEB tolerance of SiC devices has become better known. Understanding of the mechanisms for the development of the radiation tolerant devices based on SiC is needed. However, experimental data for

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Table 2 Characteristics of heavy ions typically used at the Tohoku University cyclotron. Ranges and LETs are estimated by using SRIM$^6$)

| Ion | Energy [MeV] | Range in Si, SiC [µm] | LET in Si, SiC [MeV·cm²/mg] |
|-----|--------------|------------------------|-----------------------------|
| C   | 79           | 125, 85                | 1.8, 1.8                    |
| O   | 105          | 102, 69                | 3.0, 3.2                    |
| Ne  | 131          | 88, 59                 | 4.6, 4.8                    |
| Ar  | 195          | 53, 36                 | 14, 15                      |
| Kr  | 405          | 50, 33                 | 39, 40                      |

Table 3 Characteristics of the heavy ions typically used at HIMAC. Energies of the accelerated Kr and Xe beams are 400 MeV/u and 290 MeV/u, respectively. Ion energies include energy loss in air between the beam window to sample surfaces. Energy, Ranges and LETs are estimated by using SRIM$^6$)

| Ion | Energy at Sample [GeV] | Range in Si, SiC [mm] | LET in Si, SiC [MeV·cm²/mg] |
|-----|------------------------|------------------------|-----------------------------|
| Kr  | 27.4                   | 20.8, 14.6             | 3.5, 3.6                    |
| Xe  | 25.9                   | 6.5, 4.6               | 10.6, 10.9                  |
understanding the exact mechanisms of SEGRs and SEBs in the SiC power devices are very scarce and mechanisms of SEGRs and SEBs in SiC devices are not yet fully understood. Therefore, we are studying the single event response of SiC devices by using discrete devices.

3.3.1 SEGR

For SEGR testing, we prepared self-fabricated SiC MOS capacitors having a 72.5 nm thickness gate oxide. Samples were irradiated with ions as shown in Table 1 and Ni at 9 and 18 MeV. The beam fluxes are controlled to be between $0.50 \times 10^3$ to $4.43 \times 10^3$ ions/cm$^2$·s to avoid the accumulation of radiation-induced damage.

As mentioned in section 2, SEGR is defined as the destruction of the gate insulator (SiO$_2$) layer on MOSFETs. Therefore, we measured the LET dependence of breakdown gate electric field of gate oxide (the so-called critical field $E_{cr}$) during an ion hit. At ion incidence, the leakage current through the gate oxide of the MOS capacitors was monitored under direct current (DC) biases. We defined the $E_{cr}$ as the electric field at which the leakage current density exceeded 1 A/cm$^2$. Samples were incrementally biased from 20 to 100 V in steps of 0.2 V, and at each step the bias was maintained for 6 s.

Fig. 3 shows the leakage current density through the MOS capacitors with and without ion irradiation as a function of the electric field applied to the gate oxide. After increasing gradually, the leakage current density increases sharply to 1 A/cm$^2$ for all samples. This result clearly indicates that the SEGR occurs at a lower electric field strength when ions with a higher LET penetrate SiC MOS devices.

Fig. 4 shows the LET dependence of the inverse of SEGR electric field. For comparison, the LET dependence of inverse of the SEGR electric field in Si MOS capacitor is superimposed. For both SiC and Si MOS capacitors, the value of $1/E_{cr}$ increases linearly with LET. This the first time the linear relation between LET and $1/E_{cr}$ for SiC MOS capacitors has been obtained, although the linear relation between LET and $1/E_{cr}$ has been reported for Si MOS capacitors. The slope of $1/E_{cr}$ obtained for SiC MOS capacitors is gentler compared to that for SiC MOS capacitors. This result suggests that the radiation response of SiC MOS capacitors is smaller than that of Si MOS capacitors, and as a result, SiC MOS capacitors have higher radiation resistance than Si MOS capacitors. However, further experiments, analysis, and device simulation are needed to clarify the dominant factors underlying the LET and...
3.3.2 SEB

Ion induced charge collection characteristics in biased SiC devices are used to explore the mechanisms of SEBs, since the amount of collected charge and flow of the charge seem to be a major trigger of SEBs in any device. To investigate the charge dynamics in SiC devices, we measured the reverse bias dependences of ion induced charge for SiC-SBDs. The SiC-SBDs used in this experiment were fabricated on n-type epitaxial layer grown by the Central Research Institute of Electric Power Industry (CRIEPI). The thickness and doping concentration of the epitaxial layer are 30 µm and 2–3 × 10^5 cm⁻³, respectively. The anode was grounded and the cathode was biased from +100 V to +1000 V by high-voltage supply via a charge-sensitive pre-amplifier. Charge collected from the pre-amplifier was shaped into a voltage-pulse having a pulse height proportional to the collected charge. The SiC-SBDs were irradiated with a 322 MeV Krypton beam.

Fig. 5 shows the collected charge spectra from SiC-SBD at different bias conditions. The vertical axes are ion-induced pulse generation cross-sections. The horizontal axis corresponds to the charge. Normally the collected charge spectrum might have a mono-peak similar to that found in a SiC-SBD spectrum. However, here two peaks under bias conditions higher than 300 V are observed. The first peak exists at a value of 6.2 pC in every bias condition. The first peak increases with increasing the reverse bias applied to the cathode, and finally saturates, because the depletion width in the epitaxial layer increases with the reverse bias. The upper limit of the first peak (6.2 pC) corresponds to the charge induced in SiC by the fully stopped 300 MeV Kr ion. The experiment showed an anomalous charge collection peak. In other words, the ion-induced charge was enhanced in the SiC-SBD at higher bias voltages. From these results, we assume that the key physical factors in charge enhancement are the impact ionization and the trap-assisted-tunneling. Currently we are studying the parameters of the charge enhancement mechanisms.

3.4 SEB Testing for SiC Devices at HIMAC

A heavy-ion induced charge collection and a leakage current measurement have been demonstrated for SiC MOSFETs at HIMAC. The samples used in this study were SiC-Implantation and Epitaxial MOSFETs (IE-MOSFETs) with planar gate structure and SiC-Implantation and Epitaxial Trench MOSFETs (IE-UMOSFETs) with trench gate structure fabricated on n-type epitaxial layer by the National Institute of Advanced Industrial Science and Technology (AIST) as shown in Fig. 6. These MOSFETs have vertical channel structure, therefore, the sensitive area depth of these MOSFETs corresponds to the epitaxial layer thickness. The drain of the MOSFETs was biased, and the ion-induced charge was collected at the drain via charge sensitive pre-amplifier. The MOSFETs were irradiated in air with a broad beam of 27.4 GeV Krypton (Kr) and...
Fig. 7 (a), (b) show Kr ion induced charge collection spectra from the IE-MOSFET and the IE-UMOSFET. The charge value theoretically induced in 4H-SiC epitaxial layer (drift layer) by 27.4 GeV of a Kr ion was estimated to be about 0.25 pC. In these measurements, about 6 pC is the upper limit of the charge measurement.

Fig. 7(a) shows charge collection spectra from the IE-MOSFET. For the IE-MOSFET, multiple peaks are observed, as seen in our results on the SBDs, which suggests that similar charge collection processes and multiplication occur in the IE-MOSFETs. In addition, the peaks shifted to higher charge values with increased drain bias voltage. In all drain bias conditions, charges larger than the 0.25 pC predicted by theory are observed to be induced in the drift layer, and the maximum charge signal exceeds the measurement limit of the measurement setup. On the
other hand, a single peak was observed from the IE-UMOSFET at a drain bias of 400 V, as shown in Fig. 7(b). Even though the peak splits into two peaks in the case of not less than 600 V of drain bias voltage, these peaks overlap compared to the spectra for IE-MOSFET in Fig. 7(a), and the observed maximum charge value was 1.2 pC at 800 V.

Fig. 8 shows the leakage current for the IE-UMOSFET as a function of drain bias voltage in the case of Xe irradiation. The leakage current increase on the SiC MOSFET (CMF10120D) fabricated by CREE Inc. is superimposed for comparison.

The leakage current did not increase at 650 V, which is higher than the SEB voltage of CREE MOSFETs despite similar LET ion irradiation. Moreover, the IE-UMOSFET worked at the typical operation voltage of 650 V under irradiation conditions. Therefore, we can state that we showed that the SEB tolerance of IE-UMOSFETs is higher than that of the CREE MOSFET. Using high energy heavy ion from HIMAC the gate structure dependence of charge collection distribution between SiC planar gate MOSFETs and trench gate MOSFETs fabricated by the same technology was shown for the first time.

4. Conclusion

We reviewed the SEE hardening test methodology using high energy heavy ions. In addition, our latest SEE results obtained at HIMAC are also described. As shown in this study, the SEEs for SiC devices are becoming clearer, however, experimental data for understanding the exact mechanisms of SEEs in SiC devices are still scarce, and mechanisms of SEEs have not yet been fully understood. Therefore, more studies are needed for single event response of SiC devices by using high energy ions such as are available at HIMAC.

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