Safe and Practical GPU Acceleration in TrustZone

Heejin Park
Purdue ECE

Felix Xiaozhu Lin
University of Virginia

ABSTRACT
We present a holistic design for GPU-accelerated computation in TrustZone TEE. Without pulling the complex GPU software stack into the TEE, we follow a simple approach: record the CPU/GPU interactions ahead of time, and replay the interactions in the TEE at run time. This paper addresses the approach’s key missing piece -- the recording environment, which needs both strong security and access to diverse mobile GPUs. To this end, we present a novel architecture called CODY, in which a mobile device (which possesses the GPU hardware) and a trustworthy cloud service (which runs the GPU software) exercise the GPU hardware/software in a collaborative, distributed fashion. To overcome numerous network round trips and long delays, CODY contributes optimizations specific to mobile GPUs: register access deferral, speculation, and metastate-only synchronization. With these optimizations, recording a compute workload takes only tens of seconds, which is up to 95% less than a naive approach; replay incurs 25% lower delays compared to insecure, native execution.

1. INTRODUCTION

GPU in TrustZone Trusted execution environments (TEE) has been a popular facility for secure GPU computation [58, 34]. By isolating GPU from the untrusted OS of the same machine, it ensures the GPU computation’s confidentiality and integrity. This paper focuses on GPU computation in TrustZone, the TEE on ARM-based personal devices. For these devices, in-TEE GPU compute is especially useful, as they often run GPU-accelerated ML on sensitive data, e.g., user’s health activities, speech audio samples, and video frames.

GPU stack mismatches TrustZone Towards isolating the GPU hardware, TrustZone is already capable [16, 40], which is contrast to other TEEs such as SGX. The biggest obstacle is the GPU software stack, which comprises ML frameworks, a userspace runtime, and a device driver. The stack is large, e.g., the runtime for Mali GPUs is an executable binary of 48 MB; it has deep dependency on a POSIX OS, e.g., to run JIT compilation; it is known to contain vulnerabilities [57, 4, 5]. Such a feature-rich stack mismatches the TEE, which expects minimal software for strong security [64, 60, 55]. Recognizing the mismatch, prior works either transform the GPU stack [58] or the workloads [7, 67, 58]. They suffer from drawbacks including high engineering efforts and loss of compatibility, as will be analyzed in Section 2.

Goal & overall approach Can the TrustZone TEE run GPU-accelerated compute without an overhaul of the GPU stack? To this end, a recent approach called GPU replay shows high promise [54]. It executes a GPU-accelerated workload \( W \), e.g., neural network (NN) inference, in two phases. (1) In the record phase, developers run \( W \) on a full GPU stack and log CPU/GPU interactions as a series of register accesses and memory dumps. (2) In the replay phase, a target program replays the pre-recorded CPU/GPU interactions on new input data without needing a GPU stack. GPU replay well suites TEE. The record phase can be done in a safe environment which faces low threats. After record is done once, replay can happen within the TEE repeatedly. The replay can be as simple as a few KSLoC, has little external dependency, and contains no vulnerabilities seen in a GPU stack [2, 4, 5]. Note that it is crucial to record and replay at CPU/GPU boundary; recording at higher levels, e.g., ML framework APIs, would bloat the TEE with implementation of these APIs.

Yet, a key, unsolved problem is the recording environment, where the full GPU stack is exercised and CPU/GPU interactions are logged. The recording environment must simultaneously (1) enjoy strong security and (2) access the exact GPU hardware that will be used for replay. These requirements preclude recording on the OS of the same mobile device, as TEE does not trust the OS. They also preclude recording on a developer’s machine, because it can be difficult for developers to predict and possess all GPU hardware models that their workloads may execute on. Section 2 will present...
details on today’s diverse mobile GPUs.

**Key idea** We present a novel approach called collaborative dryrun (CODY), in which the TEE leverages the cloud for GPU recording. As shown in Figure 1, a cloud service hosts the GPU software stack without hosting any GPU hardware. To record, the TEE on a mobile device (referred to as the “client”) requests the cloud to run a workload, e.g., NN inference. The cloud exercises its GPU stack without executing the actual GPU computation; it tunnels all the resultant CPU/GPU interactions between the GPU stack and the physical GPU isolated in the client TEE. The cloud logs all the interactions as a recording for the workload. In future execution of the workload on new inputs, the TEE replays the recording on its physical GPU without invoking the cloud service.

CODY addresses the needs for a secure, manageable recording environment. First, unlike mobile devices which face high threats from numerous apps, the cloud service runs on rigorously managed infrastructures and only exposes a small attack surface – authenticated, encrypted communication with the client TEE. Importantly, the cloud service never learns the TEE’s sensitive data, e.g., ML input and model parameters. Second, the cloud service accesses the exact, diverse GPU hardware (Figure 2) without the hassle of hosting them. It is responsible for hosting drivers for the GPU hardware, a task which we will show as practical.

**Challenges and Designs** The main challenge arises from spanning GPU/GPU interactions over the connection between the cloud and the client. A GPU workload generates frequent register accesses (more than 95% are read), accesses to shared memory, and interrupts. If the GPU stack and the GPU hardware were co-located on the same machine, each interaction event takes no more than microseconds; since we distribute them over wireless connection, each event will take milliseconds or seconds. Forwarding the interactions naively results in formidable delays, rendering CODY unusable.

To overcome the long delays, we exploit two insights.

1. The sequence of GPU register accesses consists of many recurring segments, corresponding to driver routines repeatedly invoked in GPU workloads, e.g., for job submission and GPU cache flush. By learning these segments, the cloud service can predict most register accesses and their outcomes. (2) Unlike IO-as-a-service [61], which must produce correct results, the cloud only has to extract replayable interactions for later actual executions. With the insights, CODY automatically instruments the GPU driver code in the cloud to implement the following mechanisms.

2. To further mask the network delay of a commit, the cloud service predicts the outcomes of register reads in the commit. Without waiting for the commit to finish, the cloud allows the driver to continue execution based on the predicted read values. The cloud validates the speculation after the client returns the actual register values. In case of misprediction, both the cloud and the client leverage the GPU replay technique to rapidly rollback to their most recent valid states.

3. Metastate-only synchronization. Despite physically distributed memories, the driver in the cloud and the client GPU must maintain a synchronized memory view. We reduce the synchronization frequency by tapping in GPU hardware events; we reduce the synchronization traffic by only synchronizing GPU’s metastate – GPU shaders, command lists, and job descriptions – while omitting workload data, which constitutes the majority of GPU memory. As a result, we preserve correct CPU/GPU interactions while forgoing the compute result correctness, a unique opportunity of dryrun.

**Results** We build CODY atop Arm platforms and Mali Bifrost, a popular family of mobile GPUs, and evaluate it on a series of ML workloads. Compared to naive approach, CODY lowers the recording delays by two orders of magnitude, from several hundred seconds to 10 – 40 seconds; it reduces the client energy consumption by up to 99%. Its replay incurs 25% lower delays as compared to insecure, native execution of the workloads.

**Contributions** We present a holistic solution for GPU acceleration within the TrustZone TEE. We address the key missing piece – a safe, practical recording environment. We make the following contributions.

- A novel architecture called CODY, where the cloud and the client TEE collaboratively exercise the GPU stack for recording GPU/GPU interactions.
- A suite of key I/O optimizations that exploit GPU-specific insights in order to overcome the long network delays between the cloud and the client.
- A concrete implementation for practicality: lightweight instrumentation of the GPU driver; crafting the device tree for VMs to probe GPU without hosting the GPU; a TEE module managing GPU for record and replay.

## 2. MOTIVATIONS

### 2.1 Mobile GPUs

This paper focuses on mobile GPUs which share mem-
Our goal is to run GPU compute inside the TrustZone TEE, for which prior approaches are inadequate.

### Porting GPU stack to TEE

One approach is to pull the GPU stack to the TEE (“lift and shift”) \cite{34, 48}. The biggest problem is the clumsy GPU stack: the stack spans large codebases (e.g., tens of MB binary code), much of which are proprietary. The stack depends on POSIX APIs which are unavailable inside TrustZone TEE. For these reasons, it will be a daunting task to port proprietary runtime binaries and a POSIX emulation layer, let alone the GPU driver. **Partitioning** the GPU stack and porting part of it, as suggested by recent works \cite{33, 68}, also see significant drawbacks: they still require high engineering efforts and sometimes even hardware modification. The ported GPU code is likely to introduce vulnerabilities to the TEE \cite{1, 4, 3}, bloating the TCB and weakens security.

### Outsourcing

Another approach is for TEE to invoke an external GPU stack. One choice is to invoke the GPU stack in the normal-world OS of the same device. Because the OS is untrusted, the TEE must prevent it from learning ML data/parameters and tampering with the result. Recent techniques include homomorphic encryption \cite{67, 20}, ML workload transformation \cite{39, 30}, and result validation \cite{18}. They lack GPU acceleration or support limited GPU operators, often incurring significant efficiency loss.

### 2.3 GPU replay in TrustZone

Unlike prior approaches, GPU replay provides a new way to execute GPU-accelerated compute \cite{54}. (1) In the record phase, app developers run their ML workload once on a trusted GPU stack; at the driver level, a recorder logs all the CPU/GPU interactions – register accesses, GPU memory dumps which enclose GPU commands and shaders, and interrupt events. These interactions constitute a recording for the ML workload. (2) In the replay phase, a target app in the TEE supplies new input to the recording. The TEE does not need a GPU stack but only a simple replayer (30 KB) for interpreting and executing the logged interactions.

Figure 3 exemplifies how GPU replay works for NN inference. To record, developers run the ML inference once and produce a sequence of recordings, one for each NN layer; each NN layer invokes multiple GPU jobs, e.g., convolution or pooling. To replay, a target ML app executes the recordings in the layer order. The granularity of recordings is a developers’ choice as the tradeoff between composability and efficiency. Alternatively, developers may create one monolithic recording for all the NN layers (not shown in the figure).

### Why is GPU replay practical?

(1) An ML workload such as NN often runs pre-defined GPU jobs. High-level GPU APIs can be translated to GPU primitives ahead of time; at run time, the workload does not need the stack’s dynamic features, e.g., JIT and fine-grained sharing. (2) An NN often has a static GPU job graph with no conditional branches among jobs. A single record run can exercise all the GPU jobs and record them. (3) Nondeterministic GPU events can be systematically prevented or tolerated, allowing the replayer to faithfully reproduce the recorded jobs. For instance, the recorder can serialize GPU job submission and avoid nondeterministic interrupts.
2.4 The Problem of Recording Environment

To apply GPU replay to TrustZone, a missing component is the recording environment where the GPU stack is exercised and recordings are produced. Obviously, the environment should be trustworthy to the TEE. What is more important, the environment must have access to the GPU hardware that matches the GPU for replay. Recording with the exact GPU model is crucial. In our experience, one shall not even record with a different GPU model from the same GPU family, because replay can be broken by subtle hardware differences: (1) register values which reflect the GPU’s hardware configuration, e.g. shader core count, based on which the JIT compiler generate and optimize GPU shaders; (2) encodings of GPU pagetables; (3) encodings of shared memory, with which GPU communicates its execution status with CPU.

Can recording be done on developers’ machines? While developers’ machines can be trustworthy [66], it would be a heavy burden for the developers to foresee all possible client GPUs and possess the exact GPU models for recording. As shown in Figure 2, mobile GPUs are highly diverse [36]: today’s SoCs see around 80 mobile GPU models in four major families (Apple, PVR, Mali, and Adreno); no GPU models are dominating the market; new GPU models are rolled out frequently.

Can recording be done on a “mobile device farm” in the cloud? While such a device farm relieves developers’ burden, managing a large, diverse collection of mobile devices in the cloud is tedious if not impractical. Not designed to be hosted, mobile devices do not conform to the size, power, heat dissipation requirements of data centers. The device farm is not elastic: a device can serve one client at a time; planning the capacity and device types is difficult. As new mobile devices emerge every few months, the total cost of ownership is high.

3. CODY

We advocate for a new recording environment: dryrun the GPU stack in the cloud while using the physical GPUs on the clients.

3.1 The Approach

Figure 4 illustrates our approach. (1) Developers write an ML workload as usual, e.g. MNIST inference atop Tensorflow. They are oblivious to the TEE, the GPU model, and the cloud service. (2) Before executing the workload for the first time, the client TEE requests the cloud service to dryrun the workload. As the cloud runs the GPU stack, it forwards the access to GPU hardware to the client TEE and receives the GPU’s response from the latter. In the mean time, the cloud records all the CPU/GPU interactions. (3) For actual executions of the ML workload, the client TEE replays the recorded CPU/GPU interactions on new input data; it no longer involves the cloud.

Our approach fundamentally differs from remote I/O or I/O-as-a-service [61]. Our goal is neither to execute GPU compute in the cloud [22, 19] (in fact, the cloud has no physical GPUs) nor run the GPU stack precisely in the cloud, e.g. for software testing [65]. It is to extract the software’s stimuli to GPU and the GPU’s response. This allows CODY to skip much communications and optimize the cloud execution.

Why using the cloud for recording? The cloud has the following benefits.

(1) Rich resources. The cloud can run a GPU stack that is too big to fit in the TEE; it can also host multiple variants of GPU stack, catering to different APIs and frameworks used by ML workloads.

(2) Secure. The cloud isolates the GPU stack in a safer environment. In contrast to client mobile devices which often run a myriad of apps and face threats such as clickbait and malware, the cloud infrastructure has more rigorous security measures [62, 63]. As the dryrun service uses dedicated VMs that only serve authenticated TEEs, the attack surface of the GPU stack is minimized.

(3) No sensitive data exposed. A client TEE’s invocation of dryrun service never gives away its ML model weights or inputs, because recording by design does not need them. For this reason, the dryrun service does not have to be hosted in a cloud TEE, e.g. SGX. Section 7.1 will present a detailed security analysis.

Can the cloud emulate GPUs? One may wonder if the cloud operates with software-based GPU emulators [24], thereby avoid communicating with client GPUs. Building such emulators is difficult, as it would require precise emulation of GPU interfaces and behaviors. However, modern GPUs are diverse [36]; they often have undisclosed behaviors and interfaces; their hardware quirks are not uncommon.

Will the cloud see GPU driver explosion? The cloud VMs for dryrun need to install drivers for all GPU models on clients. Fortunately, maintaining the drivers will not add much burden, as the total number of needed GPU drivers is small. A single GPU driver often supports many GPU models of the same family [14, 13].
these GPUs share much driver code while differing in register definitions, hardware revisions, and erratum. For instance, Mali Bifrost and Qualcomm Adreno 6xx drivers each support 6 and 7 GPUs [11, 44]. As Section 5 will show, by crafting the kernel device tree, we can incorporate multiple GPU drivers in one Linux kernel image to be used by the cloud VMs.

3.2 The CODY architecture

Figure 4 shows the architecture. The cloud service manages multiple VM images, each installed with a variant of GPU stack. The VM is lean, containing a kernel and the minimal software required by the GPU stack. Once launched, a VM is dedicated to serving only one client TEE. All the communication between the cloud VM and the TEE is authenticated and encrypted.

CODY’s recorder comprises two shims for the cloud (DriverShim) and for the client TEE (GPUShim). DriverShim at the bottom of the GPU stack interposes access to the GPU hardware. It is implemented by automatic instrumenting of the GPU driver, injecting code to register accessors and interrupts handlers. GPUShim, instantiated as a TEE module, isolates the GPU during recording and prevents normal-world access.

After a record run, DriverShim processes logged interactions as a recording; it signs and sends the recording back to the client. To replay, the client TEE loads a recording, verifies its authenticity, and executes the enclosed interactions. During replay, the TEE isolates the GPU; before and after the replay, it resets the GPU and cleans up all the hardware state.

3.3 Challenge: long network delays

A GPU stack is designed under the assumption that CPU and GPU co-locate on an on-chip interconnect with sub-microsecond delays. CODY breaks the assumption by spanning the interconnect over the Internet with tens of ms or even seconds of delays. As a result, the GPU driver is blocked frequently. The GPU driver frequently issues register accesses; each register access stalls the driver for one round trip time (RTT). Taking MNIST inference as an example, the GPU driver roughly issues 2800 register accesses, taking 117 seconds on cellular network.

Long RTTs also make memory synchronization slow. CODY needs to synchronize the memory views of the driver (cloud) and the GPU (client). When they run on the same machine, the driver and the GPU exchange extensive information via shared memory: commands, shader code, and input/output data. When the driver and the GPU are distributed, maintaining such a shared memory illusion may see prohibitive slowdown. As we will show in Section 5, classic distributed shared memory (DSM) misses key opportunity in dryrun.

The long recording delay, often hundreds of seconds shown in Section 7, render CODY unusable. (1) An ML workload has to wait long before its first execution in TEE. (2) During a record run, the TEE must exclusively owns the GPU, blocking the normal-world GPU apps for long and hurting the system interactivity. (3) The cloud cost is increased, because CODY keeps the VMs alive for extended time. (4) The GPU stack often throws exceptions, because the long delays violate many timing assumptions implicitly made by the stack code.

4. HIDING REGISTER ACCESS DELAYS

To overcome the long network delays in CPU/GPU interactions, we retrofit known I/O optimizations to exploit new opportunities.

4.1 Register Access Deferral

**Problem** By design, a GPU driver weaves GPU register accesses into its instruction stream; it executes register accesses and CPU instructions synchronously in program order. For example in Figure 5(a), the driver cannot issue the second register access until the first access and the CPU instructions preceding the second register access complete. The synchronous register access leads to numerous network round trips. This is exacerbated by the fact that GPU register accesses are dominated by reads (more than 95% in our measurement), which cannot be simply buffered as writes.

**Basic idea** We coalesce the round trips by making register accesses asynchronous: as shown in Figure 5(b), DriverShim defers register accesses as the driver executes, until the driver cannot continue execution without the value from any deferred register read. DriverShim then synchronously commits all deferred register accesses in a batch to the client GPU. After the commit, DriverShim stalls the driver execution until the client GPU returns the register access results.

To implement the mechanism, DriverShim injects the deferral hooks into the driver via automatic instrumentation. The driver source code remains unmodified.

**Key mechanisms for correctness** First, DriverShim keeps the deferral transparent to the client and its GPU. For
correctness, the GPU must execute the same sequence of register accesses as if there was no deferral. The register accesses must be in their exact program order, because (1) GPU is stateful and (2) these accesses may have hidden dependencies. For instance, read from an interrupt register may clear the GPU’s interrupt status, which is a prerequisite for a subsequent write to a job register. For this reason, DriverShim queues register accesses in their program order. It instantiates one queue per kernel thread, which is important to the memory model to be discussed later.

Second, DriverShim tracks data dependencies. This is because (1) the driver code may consume values from uncommitted register reads; (2) the value of a later register write may depend on the earlier register reads. Listing 1(a) shows examples: variable qrk_mmu depends on the read from register MMU_CONFIG; the write to MMU_CONFIG on line 7 depends on the register read on line 3. To this end, for each queued register read, DriverShim creates a symbol for the read value and propagates the symbol in subsequent driver execution. Specifically, a symbol can be encoded in a later register write to be queued, e.g. reg_write(MMU_CONFIG, S1|0x10), where S is a symbol. After a commit returns concrete register values, DriverShim resolves the symbols and replaces symbolic expressions in the driver state that encode these symbols.

Third, DriverShim respects control dependencies. The driver control flow may reach a predicate that depends on an uncommitted register read, as shown in Listing 1(b), line 3. DriverShim resolves such control dependency immediately: it commits all the queued register accesses including the one pertaining to the predicate.

When to commit? DriverShim commits register accesses when the driver triggers the following events.

- Resolution of control dependency. This happens when the driver execution is about to take a conditional branch that depends on an uncommitted register read.
- Invocations of kernel APIs, notably scheduling and locking. There are three rationales. (1) By doing so, DriverShim safely limits the scope of code instrumentation and dependency tracking to the GPU driver itself; it hence avoids doing so for the whole kernel. (2) DriverShim ensures all register reads are completed before kernel APIs that may externalize the register values, e.g. printk() of register values. (3) Committing register accesses prior to any lock operations (lock/unlock) ensures memory consistency, which will be discussed below.
- Driver’s explicit delay, e.g. calling the kernel’s delay family of functions. The drivers often use delays as barriers, assuming register accesses preceding delay() in program order will take effect after delay(). For example, the driver writes a GPU register to initiate cache flush and then calls delay(), after which the driver expects that the cache flush is completed and coherent GPU data already resides in the shared memory. To respect such design assumptions, DriverShim commits register accesses before explicit delays.

Memory consistency for concurrent threads The GPU driver is multi-threaded by design. Since DriverShim defers register accesses with per-thread queues, if a driver thread assigns a symbolic value to a variable X, the actual update to X will not happen until the thread commits the corresponding register read. What if another thread attempts to read X before the commit? Will it read the stale value of X?

DriverShim provides a known memory model of release consistency to ensure no other concurrent threads can read X. The memory model is guaranteed by two designs. (1) Given that the Linux kernel and drivers have been thoroughly scrutinized for data race, a thread always updates shared variables (e.g. X) with necessary locks, which prevent concurrent accesses to the variables. (2) DriverShim always commits register accesses before the driver invokes unlock APIs, i.e. a thread commits register accesses before releasing any locks. As such, the thread must have updated the shared variables with concrete values before any other threads are allowed to access the variables.

Optimizations To further lower overhead, we narrow down the scope of register access deferral. We exploit an observation: GPU register accesses show high locality in the driver code: tens of “hot” driver functions issue more than 90% register accesses. These hot functions are analogous to compute kernels in HPC applications.

To do so, we obtain the list of hot functions via profiling offline. We run the GPU stack, trace register ac-
cesses, and bin them by driver functions. At record time, DriverShim only defers register accesses within these functions. When the driver’s control flow leaves one hot function but not entering another, DriverShim commits queued register accesses. Note that (1) the choices of hot functions are for optimization and do not affect driver correctness, as register accesses outside of hot functions are executed synchronously; (2) profiling is done once per GPU driver, hence incurring low effort.

4.2 Speculation

Basic idea Even with deferred register accesses, each commit is still synchronous taking one RTT (Figure 5(b)). DriverShim further makes some commits asynchronous to hide their RTTs. The idea is shown in Figure 5(c): rather than waiting for a commit \( C \) to complete, DriverShim predicts the values of all register reads enclosed in \( C \) and continues driver execution with the predicated values; later, when \( C \) completes with the actual read values, DriverShim validates the predicated values: it continues the driver execution if the all predictions were correct; otherwise, it initiates a recovery process, as will be discussed below. Misprediction incurs performance penalty but does not violate correctness.

Why are register values predictable? The efficacy of speculation hinges on predictability of register values. Our observation is that the driver issues recurring segments of register accesses, to which the GPU responds with identical values most of time. Such segments recur within a workload (e.g. MNIST inference) and across workloads (e.g. MNIST and AlexNet inferences).

Why recurring segments? We identify the following common causes. (1) Routine GPU maintenance. For instance, before and after each GPU job, the driver flushes GPU’s TLB/cache. The sequences of register accesses and register values (e.g. the final status of flush operations) repeat themselves. (2) Repeated GPU state transitions. For instance, each time an idle GPU wakes up, the driver exercises the GPU’s power state machine, for which the driver issues a fixed sequence of register writes (to initiate state changes) and reads (to confirm state changes). (3) Repeated hardware discovery. For instance, during its initialization, the driver probes GPU hardware capabilities by reading tens of registers. The register values remain the same as the hardware does not change.

When to speculate? Not all register accesses belong to recurring segments. To minimize misprediction, DriverShim acts conservatively, only making prediction when the history of commits shows high confidence.

When DriverShim is about to make a commit \( C \), it looks up the commit history at the same driver source location. It considers the most recent \( k \) historical commits that enclose the same register access sequence as \( C \): if all the \( k \) historical commits have returned identical sequences of register read values, DriverShim uses the values for prediction; otherwise, DriverShim avoids speculation for \( C \), executing it synchronously instead. \( k \) is a configurable parameter controlling the DriverShim’s confidence that permits prediction. We set \( k = 3 \) in our experiment.

How does driver execute with predicted values? Based on predicted register values, the GPU driver may mutate its state and take code branches; DriverShim may make a new commit without waiting for outstanding commits to complete. To ensure correctness, DriverShim stalls the driver execution until all outstanding commits are completed and the predictions are validated, when the driver is about to externalize any kernel state, e.g. calling printk() on a variable. This condition is simple, not differentiating if the externalized state depends on predicted register values. As a result, checking the condition is trivial: DriverShim just intercepts a dozen of kernel APIs that may externalize kernel state. DriverShim eschews from fine-grained tracking of data and control dependencies throughout the whole kernel.

Optimization: Only checking the above condition has a drawback: in the event of misprediction, both the driver and the GPU have to roll back to valid states, because both may have executed based on mispredicted register values. Listing 1(b) shows an example: if the read of JOB_IRQ_STATUS (line 9) is found to be mispredicted after the second commit (line 10), the driver already contains incorrect state (in dev) and the GPU has executed incorrect register accesses (e.g. write to JOB_IRQ_CLEAR).

To this end, DriverShim can relieve the client GPU from rollback in case of misprediction. It does so by prevent spilling speculative state to the client. Specifically, DriverShim additionally stalls the driver before committing register accesses that themselves are speculative, i.e. having dependencies on predicted values. For example, in Listing 1(b), the second commit must be stalled if the first is yet to complete, because the second commit consists of register accesses (JOB_IRQ_CLEAR and TILER/SHADER_PRESENT) that casually depend on the outcome of the first commit. To track speculative register accesses, DriverShim taints the predicted register values and follow their data/control dependencies in the driver execution. In the above example, when the driver takes a conditional branch based on a speculative value (line 3), DriverShim taints all updated variable and statements on that branch to be speculative, e.g. dev->tiler. For completeness, the taint tracking applies to any kernel code invoked by the driver.

How to recover from misprediction? When DriverShim finds an actual register value different from what was predicated, the GPU stack and/or the GPU should restore to valid states. We exploit the GPU replay technique [54] for both parties to restart and fast-forward
Listing 2: Code example of a polling loop

4.3 Offloading polling loops

A GPU driver often invokes polling loops, e.g. to busy wait for register value changes as shown in Listing 2. Polling loops contribute a large fraction of register accesses; they are a major source of control dependencies.

Problem Naive execution of a polling loop incurs multiple round trips, rendering the aforementioned techniques ineffective. (1) Deferring register access does not benefit much, because each loop iteration generates control dependency and requests a synchronous commit. (2) Speculation on a polling loop is difficult: by design above, DriverShim must predict the iteration count before the terminating condition is met, which often depends on GPU timing (e.g. a GPU job’s delay) and is nondeterministic in general.

Observations Fortunately, most of polling loops are simple, meeting the following conditions.

- Register accesses in the loop are idempotent: the GPU state is not be affected by re-execution of the loop body.
- The iteration count has only local impact: the count is a local variable and does not escape the function enclosing the loop. The count is evaluated with some simple predicates, e.g. (count < MAX).
- The addresses of kernel variables referenced in a loop are determined prior to the loop, i.e. the loop itself does not compute these addresses dynamically.
- The loop body does not invoke kernel APIs that have external impact, e.g. locking and printk().

Simple polling loops allow optimizations as will be discussed below. DriverShim uses static analysis to find all of them in the GPU driver. Complex polling loops that misfit the definition above are rare; DriverShim just executes them without optimizations.

Solution DriverShim executes simple polling loops as follows. (1) Offloading. DriverShim commits a loop in a shot to the client GPU, incurring only one RTT. To do so, DriverShim offloads a copy of the loop code as well as all variables to be referenced in the loop. GPUShim runs the loop and returns updated variables. Offloading respects release memory consistency as described in Section 4.1, because accesses to shared variables inside the loop must be protected with locks and the loop itself does not unlock. (2) Speculation. DriverShim further masks the RTT in offloading a loop. Rather than predicting the exact iteration count (e.g. the final value of max in Listing 2), DriverShim extracts and predicts the predicate on the iteration count, e.g. (max==0), which is more predictable. When the client returns the actual iteration count, DriverShim evaluates the predicate in order to validate the prediction.

5. MEMORY SYNCHRONIZATION

Problem While the driver (cloud) and the GPU (client) run on their own local memories, we need to synchronize the view of shared memory between them as in Figure 6. Memory synchronization has been a central issue in distributed execution. Memory synchronization has been a central issue in distributed execution. A proven approach is relaxed memory consistency: one node pushes its local memory updates to other nodes only when the latter nodes are about to see the updates. Accordingly, prior systems choose synchronization points based on program behaviors, e.g. synchronizing thread-local memory at the function call boundary or synchronizing shared memory of a data-race free program at the lock/unlock operations.

Unlike these prior systems, the memory sharing protocol between CPU and GPU is never explicitly defined. For example, they never use locks. From our observations, we make an educated guess that CPU and GPU write to disjoint memory regions and order their memory accesses by some register accesses and some driver-injected delays. However, it would be error-prone to build CODY based on such brittle, vague assumptions.

Approach Our idea is to constrain the GPU driver behaviors so that we can make conservative assumptions for memory synchronization. To do so, we configure the driver’s job queue length to be 1, which effectively serializes the driver’s job preparation and the GPU’s job execution. Such a constraint has been applied in prior work and shows minor overhead, because individual GPU compute jobs are sizable. With the constraint, the driver prepares GPU jobs (and accesses the shared memory) only when the GPU is idle; the GPU is executing jobs (and accesses the memory) only when the driver is idle. As a result, we maintain an invariant:

The driver and the client GPU will never access the shared memory simultaneously.

When to synchronize? The cloud and client synchro-
Client TEE

- shim

GPU Driver

- shim

No sync

GPU pgtables shaders cmds ...

Prog. data Metastate Local mem dumps (zipped)

Client TEE

- shim

GPU

No sync

GPU pgtables shaders cmds ...

Prog. data Metastate Local mem

Figure 6: Selective memory synchronization of GPU metastate but not program data.

- Cloud ⇒ client. Right before the register write that starts a new GPU job, DriverShim dumps kernel memory that the driver allocates for the GPU and sends it to the client. The memory dump is consistent: at this moment, the GPU driver has emitted and flushed all the memory state needed for the new job, and has updated the GPU page tables for mapping the memory state.

- Client ⇒ cloud. Right after the client GPU raises an interrupt signaling job completion, GPUShim forwards the interrupt and uploads its memory dump to the cloud. The memory dump is also consistent: at this moment the GPU must have written back the job status and flushed job data from cache to local memory. Specifically, the GPU cache flush action is either prescribed in the command stream or requested at the beginning of the interrupt handler.

To further safeguard the aforementioned invariant, we implement continuous validation. After DriverShim sends its memory dump to the client, it unmaps the dumped memory regions from CPU and disables DMA to/from the memory. As such, any spurious access to the memory region will be trapped to DriverShim as a page fault and reported as an error. In the same fashion, GPUShim unmaps the shared memory from the GPU’s page table when the GPU becomes idle; any spurious access from GPU will be trapped and reported.

What to synchronize? As shown in Figure 6, we minimize the amount of memory transfer with the following insight: for recording, it is sufficient to synchronize only the GPU metastate in memory, including GPU commands, shader code, and job descriptors. Synchronizing program data, including input/output and intermediate GPU buffers, is unnecessary. This is effective as program data constitutes most of GPU memory footprint.

How to locate metastate in the shared memory, given that the memory layout is often proprietary? We implement a combination of techniques. (1) Some GPU page tables have permission bits which suggest the usage of memory pages. For instance, the Mali GPUs map metastate as executable because the state contains GPU shader code. (2) For GPU hardware lacking permission bits, CODY infers the usage of memory regions from IOCTL() flags used by ML workloads to map these regions. For instance, a region mapped as read-only cannot hold GPU commands, because the GPU runtime needs the write permission to emit GPU commands. (3) If the above knowledge is unavailable, the DriverShim simply replaces an ML workload’s inputs and parameters as zeros. Doing so will result in abundant zeros in the GPU’s program data, making memory dumps highly compressible.

Atop selective memory synchronization, we apply standard compression techniques. Both shims use range encoding to compress memory dumps; each shim calculates and transfers the deltas of memory dumps between consecutive synchronization points.

6. IMPLEMENTATIONS

Platforms We implement the CODY prototype on the following platforms. The cloud service runs on Odroid C4, an Arm board with 4 Cortex-A55 cores. The client runs on Hikey960 which has 4 Cortex-A73 and A53 cores, and a Mali G71 MP8 GPU. Our choice of Arm processors for the cloud is for engineering ease rather than a hard requirement; the cloud service can run on x86 machines with binary translation.

The cloud service runs Debian 9.4 (Linux v4.14) with a GPU stack composed of a ML framework (ACL v20.05), a runtime (libmali.so), and a driver (Mali Bifrost r24). Under the cloud service, KVM-QEMU (v4.2.1) runs as the VM hypervisor. The client runs Debian 9.13 (Linux v4.19) and OPTEE (v3.12) as its TEE.

DriverShim We build our code instrumentation tool as a Clang plugin. For static analysis and code manipulation, the plugin traverses the driver’s abstract syntax tree (AST). With the Clang/LLVM toolchain, our tool compiles the GPU driver and links it against our instrumentation tool processes 19 functions in total. The instrumentation itself incurs negligible overhead. We implement DriverShim as a kernel module (∼1K SLoC) to be invoked by the instrumented driver code; the module performs dependency tracking, commit management, and speculation, as described in Section 4 and 5.

DriverShim communicates with the client via TCP-based messages in our custom formats. To avoid potential timeout due to network communications, we add a fixed delay (e.g., 3 seconds) to all the timeout values in the driver. We prepare and install GPU devicetrees in the cloud VM, so the GPU stack can run transparently even a physical GPU is not present. To support multiple GPU types, we implement a mechanism for the cloud service to load per-GPU devicetree when a VM boots. As a result, a single VM image can incorporate multiple GPU drivers, which are dynamically loaded depending on the specific client GPU model.
**GPUShim** We build GPUShim as a TEE module. Following the TrustZone convention, GPUShim communicates with the cloud using the GlobalPlatform APIs implemented by OPTEE [27]. The communication is authenticated and encrypted by SSL 3.0 with the TEE, before it forwarded through the normal-world OS.

By design, the client’s trusted firmware dynamically switches the GPU between the normal world and the TEE with a configurable TrustZone address space controller (TZASC) [10]. Yet, our client platform (Hikey960) has a proprietary TZASC which lacks public documentation [22]. We workaround this issue by statically reserving memory regions for GPU and mapping the memory regions and GPU registers to the TEE.

We modify the secure monitor to route the GPU’s interrupts to the TEE. GPUShim forwards the interrupts to DriverShim for handling. We avoid interrupt injection to the VM hypervisor and keep it unmodified.

To bootstrap the GPU, the client TEE may need to access SoC resources not managed by the GPU driver, e.g. power/clock for GPU. While the TEE may invoke related kernel functions in the normal-world OS via RPC [65], we protect these resources inside the TEE as did in prior work for stronger security [40].

### 7. Evaluation

The evaluation answers the following questions.

- Is CODY secure against attacks? (§ 7.1)
- What are the delays of CODY? (§ 7.2)
- Are CODY’s optimizations significant? (§ 7.3)
- What is the energy implication of CODY? (§ 7.4)

#### 7.1 Security Analysis

**Threat model** We trust the cloud service, assuming its GPU stack is being attested [62, 63]. We trust the client’s TEE and hardware but not its OS. We consider two types of adversaries: (1) a local, privileged adversary who controls the client OS; (2) a network-level adversary who can eavesdrop the cloud/client communications during recording.

**Integrity** CODY’s recording integrity is collaboratively ensured by (1) the trusted cloud service, (2) the client’s TrustZone hardware, and (3) the encrypted cloud/client communication. In particular, GPUShim locks the GPU MMIO region during recording, preventing any local adversary from tampering with GPU registers or shared memory. CODY’s replay integrity is ensured by the TrustZone hardware. Since the replayer only accepts recordings signed by the cloud, it exposes no additional attack surface to adversaries.

**Confidentiality** CODY’s recording never leaks program data from TEE, e.g. ML model parameters or inputs, since recording does not require such data. It however may leak some information of the ML workload, as the workload code such as GPU shaders moves through the network. Although the network traffic is encrypted, it may nevertheless leak workload information, e.g. NN types, via side channels. Such side channels can be mitigated by orthogonal solutions [53, 72].

Since replay is within the client TEE and requires no client/cloud communication, its data confidentiality is given by TrustZone. We notice TrustZone may leak data to local adversaries via hardware side channels, which can be mitigated by existing solutions [71, 47].

**Availability** Like any cloud-based service, recording availability of CODY depends on network conditions and the cloud availability, which are vulnerable to DDoS attacks. Its replay availability is at the same level of the TrustZone TEE, given the GPU power is managed by the TEE not the OS [40].

### 7.2 Performance

**Methodology** As shown in Table 1, we test CODY on inference with 6 popular NNs running atop ARM Compute Library [12]. We measure CODY’s recording delay under two network conditions as controlled by NetEm [31]: i) WiFi-like (20 ms RTT, 80 Mbps) and ii) cellular-like (50 ms RTT, 40 Mbps) [56]. The hardware platform is described in Section 6.

We study the following versions:

- **Naive** incurs a round trip per register access and synchronizes entire GPU memory before/after a GPU job.
- **OursM** includes selective memory synchronization (§ 4.1); it generates per-commit round trips.
- **OursMDS**, in addition to **OursM**, includes register access deferral (§ 4.1); it generates per-commit round trips.
- **OursMDS** additionally includes speculation (§ 4.1.2). It represents CODY with all our techniques.

**Recording delays** Figure 7 shows the end-to-end recording delays. **Naive** incurs long recording delays even on WiFi ranging from 52 seconds (MNIST, a small NN) to 423 seconds (VGG16, a large NN). Such delays become much higher on the cellular network, range from 116 seconds to 795 seconds. As discussed in Section 3.3, such high delays not only slow down ML workload launch but also hurts interactivity because the TEE must lock the GPU during recording. Compared to **Naive**, **OursMDS** reduces the delays by up to 95% to 18 seconds (WiFi) and 30 seconds (cellular) on average. We deem these delays as acceptable, as they are comparable to mobile app installation delays reported to be 10 – 50 seconds [33].

**Replay delays** CODY’s replay incurs minor overhead in workload execution as shown in Table 2. Compares native executions, CODY’s replay delays range from 68% lower to 3% higher (25% lower on average). CODY performance advantage comes from its removal of the complex GPU stack. We notice that these results are consistent with the prior work [54].
Table 1: Statistics of record runs, showing CODY significantly reduces network round trips that block the recording and the memory synchronization traffic.

| NNs | # Blocking RoundTrip | MemSync (MB) |
|-----|----------------------|--------------|
|     | OursM     | OursMD     | OursMDS    | Naive     | OursM     |
| MNIST (23) | 2837 | 585 | 65 | 3.07 | 0.75 |
| AlexNet (60) | 5008 | 1392 | 196 | 454.91 | 4.22 |
| MobileNet (104) | 7307 | 2097 | 320 | 37.39 | 11.79 |
| SqueezeNet (98) | 7373 | 2049 | 303 | 41.26 | 11.3 |
| ResNet12 (111) | 8326 | 2352 | 345 | 1215.23 | 10.21 |
| VGG16 (96) | 7662 | 2184 | 309 | 37.39 | 11.3 |

Figure 7: Recording delays of CODY (OursMD) are significantly lower than other versions.

Table 2: Replay delays of CODY (OursMD) are similar to Native, which executes benchmarks on the GPU stack in the normal world of the same device.

| Delay (ms) | MNIST | Alex | Mobile | Squeeze | Res12 | VGG16 |
|------------|-------|------|--------|---------|-------|-------|
| Native     | 15.2  | 63   | 60.9   | 64.3    | 362.1 | 372.2 |
| OursMDS    | 4.8   | 54.8 | 45.2   | 45.3    | 373.9 | 364.8 |

7.3 Validation of key designs

Efficacy of deferral As shown in Figure 7 (OursM vs. OursMD), register access deferral reduces the overall delays by 65% (WiFi) and 69% (cellular). Table 1 further shows that the deferral reduces the number of round trips by 73% on average. With deferral, each commit encapsulates 3.8 register accesses on average.

Efficacy of speculation We run all six benchmarks with retaining register access history in between, allowing CODY to reuse history across benchmarks. Figure 7 (OursMD vs. OursMD) shows that speculation reduces the recording delays by 60% to 74%. Table 1 further shows that OursMD achieves 86% reduced number of round trips on average. Such benefit mainly come from coalescing round trips of asynchronous commits.

We further investigate the speculation success rates and find 95% of commits (99% register accesses) satisfy the speculation criteria (4.2). These commits are generated by GPU driver routines that roughly fall into four categories. (1) Init: probe hardware configuration when the driver is loaded. (2) Interrupt: read and clear interrupt status. (3) Power state: periodic manipulation of GPU power states. (4) Polling: busy wait for GPU to finish TLB or cache operations. Figure 8 shows a breakdown of commits by category. All register values in these commits are highly predictable.

The commits that fail the criteria are due to reads of nondeterministic register values. For example, on each job submission, the Mali driver reads and writes a register LATEST_FLUSH_ID which reflects the GPU cache state and can be nondeterministic.

Misprediction cost For the above reasons, we have not observed misprediction in our 1,000 runs of each workload. To validate that CODY can handle misprediction, we artificially inject into record runs wrong register values. In all the cases of injection, CODY always detects mismatches between the speculative and the injected register value, initiating rollback of the software and the hardware states properly. In the worst case (misprediction at the end of a record run), we measure the delays of rollback is 1 and 3 seconds for MNIST and VGG16, respectively. The delays are primarily dominated by driver reload and GPU job recompilation, which overshadow the replay delays on the client GPU hardware.

Selective memory synchronization Figure 7 (OursM vs. Naive) shows that the technique reduces the recording delays by 1 – 57% on average. The reduction is more pronounced on large NNs such as AlexNet and VGG16 (34 – 57%). Table 1 shows the network traffic for memory synchronization is reduced by 72 – 99%.

Polling offloading (4.3) The numbers of polling instances range from 117 (MNIST) to 492 (VGG16), that generate from 130 to 550 round trips. Offloading polling reduces the total round trips by 13 – 58, making the cost of polling instance one RTT; This is because without offloading, a polling loop often takes a few RTTs (the RTT is long as compared to GPU operations being polled such as cache flush): with offloading and speculation, the RTTs often become hidden.

7.4 Energy consumption

We measure the whole client energy using a digital multimeter which instruments the power barrel of the...
client device (Hikey960). The client device has no display. It uses the on-board WL1835 WiFi module for communication; it does not run any other foreground applications. Each workload runs 500 iterations and we report the average energy. Figure 9 shows the results.

**Record.** The energy consumed by recording is moderate, ranging from 1.8 – 8.2 J, which is comparable to one by installing a mobile app, e.g. 16 J for Snapchat (80MB) on the same device. Note that it is one-time consumption per workload. Compared to Naive, CODY reduces the system energy consumption by 84 – 99%.

**Replay.** As a reference, we measure replay energy per benchmark. It ranges from 0.01 – 1.3 J, consistent with the replay delays in Table 2. The replaying energy is comparable with the native execution on the original GPU stack of the client device (not shown in the figure).

8. RELATED WORK

**Remote I/O** is adopted for cross-device I/O sharing [8] [52] and task offloading [22] [33]. Unlike CODY, however, their remoting boundary is at higher-level – device file [8], Android binder IPC [52], and runtime API [33]. Such clean-cut boundaries ease a course-grained I/O remoting, e.g. function-level RPC calls. To apply to TEE, however, the client TEE must keep a part of (e.g. device driver) or the entire I/O stack while bloating TCB.

Similar to CODY, prior works have explored the lowest software level; For efficient dynamic analysis, they forward I/O from VM to mobile system [65] or low-level memory access from emulator to real device [69] [37]. However, their cross-device interfaces are wired, faster than what CODY addresses, (i.e. wireless connection). CODY has a different goal: hosting a dryrun service for GPU recording, mitigating communication cost.

**Device isolation with TEE.** Recent works propose TEE-based solutions for GPU isolation by hiding GPU stack in the TEE [44] [48] or security-critical GPU interfaces in the GPU hardware [68]. They, however, require hardware modification and/or bloat TCB inside TEE. Favorable to the insight given by GPU replay [54], CODY offers a remote recording service for clients to reproduce GPU compute without the stack in TEE.

Leveraging TrustZone components, prior works build a trusted path locally, e.g. for secure device control [40] or remotely [41], e.g. to securely display confidential text [7] and image [53]. Their techniques are well-suited to CODY for i) discarding adversarial access to the GPU while recording and replaying; ii) building secure channel between cloud VM and client TEE;

**Speculative execution** is widely explored by prior works; based on caching and prefetching, they facilitate asynchronous file I/O [17] [51] [59] or speed up VM replication [23] and distributed systems [70]. Unlike such works, CODY does not prefetch I/O access ahead of time; instead, CODY hide I/O latency by speculatively continue driver’s workflow deferring real values while replacing them as symbolic expression; it then commit when facing value/control dependencies.

**Mobile cloud offloading.** There has been previous works on cloud offloading [19] [21] [28], which partitions mobile application into two parts: one for local device and the other for the cloud. Facilitating application-layer virtual machine or runtime, each part of the application cooperatively runs from both sides continuously. Unlike them, CODY does not require runtime or vm support from the client; the offloading is also temporal for dryrun of GPU compute to capture the interactions.

**GPU record and replay** has been explored to dig out GPU command stream semantics [6] [42] [29], enhance performance [38], migrate runtime calls [15], and reproduce computation [54]. While they care what to record, CODY’s focus is how to record; CODY addresses costly interaction overhead for remote GPU recording.

**Secure client ML.** Much works has been proposed to protect model and user privacy [49] [50] and/or to secure ML confidentiality [30] [39]. However, they all lack GPU-acceleration which is crucial for resource-hungry client devices. While recent work [67] suggests a verifiable GPU compute with TEE, the complexity of homomorphic encryption significantly burdens client devices.

9. CONCLUSIONS

CODY provides a cloud service for GPU recording in a secure way; it performs GPU dryrun interacting with the client GPUs over long wireless communication. Retrofitting known I/O optimization techniques, CODY significantly reduces the time and energy consumed by client to get a GPU recording.

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