A Novel SEPIC-Čuk-Based High Gain Solar PV Microinverter for Grid Integration

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Abstract—A SEPIC-Čuk-based transformerless microinverter capable of interfacing a 35 V, 250 W solar PV module to a single-phase 220–230 V ac grid is proposed in this article. The circuit employs only one high-frequency switch and four line-frequency switches thereby reducing the switching losses. This also enhances the overall reliability of the system. The circuit is made to operate in discontinuous conduction mode (DCM) under all possible operating conditions to achieve high gain and at the same time ensure negligible turn-on loss for the high-frequency switch. The direct connection existing between the PV neutral and the utility ground makes the magnitude of the leakage current to be zero. In order to reduce the size of the capacitor across the PV module, an active power decoupling circuit is employed. Hence, this capacitor can be realized by a thin film capacitor instead of an electrolytic capacitor thereby improving the reliability of the system. Detailed analysis of the proposed microinverter is carried out. The effectiveness of the proposed scheme is verified by performing detailed simulation studies. A 250 W laboratory prototype of the inverter is fabricated, and detailed experimental studies are carried out to confirm the viability of the proposed scheme.

Index Terms—DC–AC conversion, discontinuous conduction mode (DCM), grid integration, high voltage gain, SEPIC, solar PV microinverter, Čuk converter.

I. INTRODUCTION

In the current scenario of electric power generation, renewable sources (solar, wind, etc.) are being considered widely over the conventional sources (thermal, nuclear, etc.), as they are environment friendly and inexhaustible in nature. In India, where solar irradiation is generally high all over the country throughout the year, the Ministry of New and Renewable Energy (MNRE) has set a target of 100 GW of grid-connected solar power generation by 2022, out of which, 40 GW has to be rooftop installations [1]. In the case of grid-connected solar rooftop installations, microinverters have become popular over the central or string inverters due to their attractive features like modularity, scalability, existence of plug and play mode, and most importantly the capability of extracting the maximum available power from every solar PV module [2].

Since each microinverter is interfaced between one PV module and the single-phase grid, the input dc voltage for the inverter is around 30–35 V, and its power rating is in the range of 200–300 W. In countries like India, the distribution voltage level is 220–230 V ac. Hence, one of the major challenges in the design of the microinverter is to obtain a high voltage gain. Flyback transformer-based topologies are widely being used by the leading microinverter manufacturers [3]. One of the major problems in the topologies those utilize flyback transformer or coupled inductor is the presence of leakage inductance which increases the voltage stress of the high-frequency (HF) switch. In order to limit this voltage stress, requirement of an additional snubber circuit becomes necessary. In addition to this, due to their low power rating and high voltage gain the efficiency of microinverters remains to be low compared to other schemes like central or string inverters. In order to improve the efficiency, less number of conversion stages are desired which has led to the development of transformerless single-stage topologies [4], [5].

In the case of transformerless topologies, there exists a path for the leakage current to flow through the parasitic capacitance of the PV module to the grid [6]. The magnitude of the leakage current needs to be maintained within the standard limit as stipulated by various regulatory authorities in order to avoid hazards to personnel and deterioration of the module [7]. The magnitude of the leakage current is significantly low in H5 [8], H6 [9], and in the case of the topology reported in [10]. But then the aforesaid topologies are not suitable for realizing a microinverter as they do not possess voltage boosting capability.

Several single-stage nonisolated microinverter topologies are reported in the literature [5]. The issue related to the leakage current has been addressed by shorting the module ground with that of the ac grid [11], [12], [13], [14], [15], [16], [17], [18], [19]. A buck–boost-based topology with only one HF switch is presented in [11]. In [12], a buck–boost-based and in [13], a Čuk converter-based single-stage microinverter topologies are reported, wherein the PV module and the ac grid share the common ground. In [14] and [16], a four switch-based topology has

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been reported. A three-switch microinverter with the common ground is reported in [18] wherein the voltage gain of the inverter can be made both positive and negative, but then it involves three inductors in the main inverter and all the switches operate at HF. A single-phase PV inverter with wide buck–boost voltage operation is presented in [19] wherein the input voltage can vary in a wide range of 42–200 V.

The life of a microinverter needs to be comparable with that of a PV module. Hence, the usage of electrolytic capacitors having a shorter lifespan needs to be avoided to the extent possible. However, the issue of instantaneous power mismatch in the case of single-phase dc–ac inverters results in a significant magnitude of voltage ripple in the PV terminal, which in turn reduces the efficiency of the maximum power point tracker (MPPT) [20]. In order to reduce the voltage ripple below 5% at the terminal of the PV module, the capacitance required for upf operation as per the design guideline presented in [21] is 13 mF. The size of a 13 mF thin film capacitor bank would be impractical for a microinverter. The value of the capacitance can be reduced by incorporating one of the various active power decoupling circuits (APDC) reported in the literature [21], [22]. This ensures that the thin film capacitor can be used instead of an electrolytic capacitor. The issue of instantaneous power mismatch is addressed in [12] and [15] without using APDC. Though the inverters are operated in continuous conduction mode (CCM), the source current is discontinuous in [12] thereby increasing the filtering requirement at the input side.

However, all the switches of these inverters [12], [13], [14], [15], [16], [17], [18], [19] operate at HF during positive half cycle (PHC) and/or negative half cycle (NHC). As all the aforesaid inverters are designed to be operated in CCM, the gain of the inverters remains to be low, and hence they can be interfaced to a single-phase ac grid having voltage level of only up to 110 V while the PV module voltage is 30–35 V. A modification to the circuit reported in [13] has been accomplished by employing an additional HF switch for controlling the reactive power fed to the grid, and is presented in [17]. Though the circuit is operated in discontinuous conduction mode (DCM), the grid voltage reported was 70 V. Hence all the aforementioned single-stage transformerless topologies are not suitable for Indian distribution grid of 220 V.

A coupled inductor-based microinverter topology operating in DCM is presented in [23], which can be interfaced to a single-phase 220 V grid. This microinverter is designed incorporating two HF switches and four line frequency (LF) switches. The topology reported in [24] is suitable for 220 V grid connection, but then, this topology requires seven switches.

In view of this, an effort has been made in this article to design a single-stage transformerless microinverter suitable for getting interfaced to a single-phase 220 V grid from a PV module having $V_{mpp}$ of 35 V, while utilizing only one HF switch and four LF switches in order to reduce the switch count, and improve the reliability and efficiency of the system. The inverter is operated in SEPIC mode during PHC, and in Ćuk mode during NHC. The combination of SEPIC and Ćuk mode of operation has led to a reduction in the number of HF switches to one. As the negative terminal of the PV module is connected to the grid neutral, the leakage current is zero.

All the aforementioned inverters except [12], [15], have not addressed the issue pertaining to instantaneous power mismatch. However, [12] and [15] are not suitable for getting interfaced to a 220 V grid. On the contrary, the proposed main microinverter does not have the inherent power decoupling capability. In order to improve the reliability of the system by replacing the electrolytic capacitor by a thin film one, an APDC reported in [25] is employed along with the proposed main microinverter. Detailed simulation studies are carried out on MATLAB/Simulink platform to ascertain the effectiveness of the proposed inverter. A semiengineered 250 W laboratory prototype of the inverter has been fabricated, and detailed experimental studies are carried out to confirm the viability of the proposed scheme.

II. PRINCIPLE OF OPERATION OF THE PROPOSED MICROINVERTER

The schematic diagram of the proposed SEPIC-Ćuk-based microinverter along with the APDC is shown in Fig. 1. The four LF switches are employed to change the mode of operation of the circuit from SEPIC to Ćuk and vice-versa. They also help to synthesize an ac output voltage with respect to the negative terminal of the PV module. The diode $D$ is employed to block the reverse current flow through the four MOSFETs, $S_2$–$S_5$ operating at LF. As sinusoidal current is required to be injected to the grid, the HF switch is applied with switching pulses which are obtained by comparing the rectified sine wave with a triangular carrier wave. The instantaneous duty ratio of $S_1$ is determined by multiplying a rectified sine wave with the peak duty ratio $d_{peak}$. The switch is operated with $d_{peak}$ when the instantaneous grid voltage is at its peak. The current through $L_2$ is a rectified sine wave of twice the grid frequency having high-frequency switching harmonics superimposed on it. The required sinusoidal output current is obtained from the double-frequency rectified sine wave by appropriately switching $S_2$–$S_5$. The output capacitor $C_2$ filters out the high-frequency switching harmonics from the output current.

The inductors of the inverter can be chosen appropriately so that the inverter can be operated either in CCM or in DCM. In CCM, the voltage gain of both SEPIC and Ćuk converter is $\frac{d}{2}$, wherein $d$ is the duty ratio of $S_1$. However, for interfacing the 35 V module to a 220 V ac grid whose peak voltage is 311 V, the duty ratio at the peak of the ac grid voltage is required to be maintained at 0.9. Operating the inverter at such a high value of duty ratio would reduce the operating efficiency significantly. In

![Fig. 1. Schematic diagram of SEPIC-Ćuk based microinverter with active power decoupling circuit.](image-url)
order to address this issue, the proposed topology is operated in DCM to obtain high voltage gain while maintaining a reduced duty ratio compared to that of CCM operation. It may be noted that in the case of SEPIC and Čuk converters, DCM operation means that there exists a time interval in a switching time period when neither the switch nor the diode (e.g., $S_1$ and $D$ in the case of the proposed topology) is conducting [26]. In this interval, both $i_{S1}$ and $i_{L2}$ remains unchanged, while their value may not be necessarily zero [26], [27], [28]. Further, the DCM operation ensures that turn ON switching loss of $S_1$ is negligible. But this is achieved at the cost of increased peak current that flows through the input inductor $L_1$.

### A. Active Power Decoupling Circuit

In order to reduce the size of the capacitor while maintaining ripple voltage within the specified limit, a boost type APDC, which is reported in [25], is incorporated as shown in Fig. 1. As the APDC is connected across the PV module through an inductor, the switching frequency harmonics drawn from the PV module is less compared to the buck and buck–boost type APDC topologies [22]. This is due to the fact that in the case of buck or buck–boost type of topologies, the current supplied by the APDC is discontinuous in nature as an HF switch is existing in its path. The APDC supplies the second-order harmonic current as required by the main inverter. The switches $S_{bk}$ and $S_{bs}$ are operated in complementary to each other in such a way that the desired current through $L_{ap}$ is maintained.

### III. ANALYSIS OF THE PROPOSED INVERTER

In order to simplify the analysis of the inverter, a dc source, $V_{dc}$ is considered instead of a PV module. Since the switching frequency is very high compared to that of the line frequency, it is assumed that the output voltage and current requirement is almost constant throughout the switching time period ($T_s$). The ripple in the voltages in the capacitors $C_1$ and $C_2$ can be considered to be negligible. The average value of $v_{C1}$ and $v_o$ over a switching time period are assumed to be $V_{C1}$ and $V_o$, respectively. The current and voltage waveforms over a switching cycle are shown in Fig. 4. The switching time period ($T_s$) is divided into three time intervals as follows: 1) $T_1 (=dT_s)$; 2) $T_2$; 3) $T_3 (=d_0T_s)$, respectively. As $T_1 + T_2 + T_3 = T_s$, therefore $T_2 = (1 - d - d_0)T_s$.

#### A. Positive Half Cycle (SEPIC Mode)

Switches $S_2$ and $S_3$ both are turned ON, while $S_4$ and $S_5$ are kept OFF. In order to estimate the voltage across $C_1$ in PHC, the circuit loop that needs to be analyzed is $V_{dc} - L_1 - C_1 - L_2 - S_2 - V_{dc}$, which exists in all the three modes of operation. Hence

$$V_{dc} - v_{L1} - V_{C1} + V_{L2} = 0. \tag{1}$$

Since $V_{dc}$ and $V_{C1}$ are assumed to remain constant throughout the switching cycle, it can be obtained by taking average of (1) over a switching cycle as follows:

$$V_{dc} - \langle v_{L1} \rangle_{T_s} - V_{C1} + \langle v_{L2} \rangle_{T_s} = 0 \tag{2}$$

where $\langle v_{L1} \rangle_{T_s}$ and $\langle v_{L2} \rangle_{T_s}$ are switching time averages of $v_{L1}$ and $v_{L2}$, respectively. However, at steady state, the magnitudes of both $\langle v_{L1} \rangle_{T_s}$ and $\langle v_{L2} \rangle_{T_s}$ are zero. Hence, from (2) at steady state

$$V_{C1} = V_{dc}. \tag{3}$$

1) **Mode I ($0 < T < T_1$):** $S_1$ is turned on and the current through $L_1$ increases as it flows through the path, $V_{dc} - L_1 - S_1 - V_{dc}$ as shown in Fig. 2(a). The intermediate capacitor $C_1$ gets discharged while the current flowing through $L_2$ increases as it flows through the path $C_1 - S_1 - S_2 - L_2 - C_1$. The capacitor $C_2$ supplies power to the grid in this interval. The diode $D$ blocks the current through the switch $S_3$ even though it is receiving the gating pulse. In this mode $i_2$ is zero. Hence

$$V_{dc} = L_1 \frac{di_{L1}}{dt} = L_1 \frac{I_{L1p} - I_{L1v}}{dT_s} = L_1 \frac{\Delta I_{L1}}{dT_s} \tag{4}$$

$$V_{C1} = L_2 \frac{di_{L2}}{dt} = L_2 \frac{I_{L2p} - I_{L2v}}{dT_s} = L_2 \frac{\Delta I_{L2}}{dT_s} \tag{5}$$

where $\Delta I_{L1} = (I_{L1p} - I_{L1v})$ and $\Delta I_{L2} = (I_{L2p} - I_{L2v})$.

2) **Mode II ($T_1 \leq T < (T_1 + T_2)$):** $S_1$ is turned OFF. The current flows through the path, $V_{dc} - L_1 - C_1 - D - S_3$-grid (along with its filter)-$V_{dc}$ as shown in Fig. 2(b) thereby charging $C_1$. The energy stored in $L_2$ is transferred to the grid as well as to $C_2$ through the path, $L_2 - D - S_3$-grid along with its filter-$S_2 - L_2$. This mode ends when $i_{L1} = -i_{L2}$. At the end of this mode, let the magnitude of the currents through $L_1$ and $L_2$ be $I_{L1m}$ and $I_{L2m}$ respectively. Therefore

$$V_{dc} - V_{C1} - V_o = L_1 \frac{di_{L1}}{dt} = L_1 \frac{I_{L1m} - I_{L1p}}{(1 - d - d_0)T_s} \tag{6}$$

$$-V_o = L_2 \frac{di_{L2}}{dt} = L_2 \frac{I_{L2m} - I_{L2p}}{(1 - d - d_0)T_s} \tag{7}$$

$$i_2 = i_{L1} + i_{L2}. \tag{8}$$
3) Mode III \((T_1 + T_2) \leq T < T_o\): This mode starts when the current through the diode \(D\) becomes zero. The diode turns off and blocks the current flowing through \(S_3\). The current path in this mode is \(V_{dc} - S_2 - L_2 - C_1 - L_1 - V_{dc}\) as shown in Fig. 2(c). Since \(V_{C1} = V_{dc}\), the currents in the inductors will remain unchanged in this mode. The capacitor \(C_2\) supplies power to the grid in this interval. Hence

\[
I_{L1m} = I_{L1v} = -I_{L2m} = -I_{L2v}.
\]

Solving (4)–(7) and (9), the expression for the voltage gain can be obtained as

\[
\frac{V_o}{V_{dc}} = \frac{d}{(1 - d - d_0)}.
\]

\[
(10)
\]

B. Negative Half Cycle (Cuk Mode)

Switches \(S_1\) and \(S_3\) both are turned on, while \(S_2\) and \(S_3\) are kept off. In order to estimate the value of \(V_{C1}\), a similar analysis can also be carried out for NHC as well, wherein there exists a loop \(V_{dc} - L_1 - C_1 - L_2 - S_4 - L_3 - V_{dc}\) for all the three modes. Considering the switching time average voltage across \(L_1\), \(L_2\), and \(L_3\) to be equal to zero

\[
V_{C1} = V_{dc} - V_o.
\]

\[
(11)
\]

1) Mode I \((0 \leq T < T_1)\): \(S_1\) is turned on and the current through \(L_1\) increases as it flows through the path, \(V_{dc} - L_1 - S_1 - V_{dc}\) as shown in Fig. 3(a). The intermediate capacitor \(C_1\) gets discharged while the current flowing through \(L_2\) increases as it flows through the path, \(C_1 - S_1\)-grid along with its filter- \(S_4 - L_2 - C_1\). The diode \(D\) blocks the current through the switch \(S_5\) even though it is receiving the gating pulse. Hence

\[
V_{dc} = L_1 \frac{dI_{L1}}{dt} = L_1 \frac{I_{LL1p} - I_{L1v}}{dTs}.
\]

\[
(12)
\]

\[
V_{C1} + V_o = L_2 \frac{dI_{L2}}{dt} = L_2 \frac{I_{LL2p} - I_{L2v}}{dTs}.
\]

\[
(13)
\]

2) Mode II \((T_1 \leq T < (T_1 + T_2))\): \(S_1\) is turned off. The current flows through the path, \(V_{dc} - L_1 - C_1 - D - S_5 - V_{dc}\), as shown in Fig. 3(b) thereby charging \(C_1\). The energy stored in \(L_2\) is transferred to the load as well as to \(C_2\) through the path, \(L_2 - D - S_5\)-grid along with its filter- \(S_4 - L_2\). This mode ends when \(i_{L1} = -i_{L2}\). At the end of this mode, let the magnitude of the currents through \(L_1\) and \(L_2\) be \(I_{L1m}\) and \(I_{L2m}\), respectively. Therefore

\[
V_{dc} - V_{C1} = L_1 \frac{dI_{L1}}{dt} = L_1 \frac{I_{L1m} - I_{L1p}}{(1 - d - d_0)Ts}.
\]

\[
(14)
\]

\[
V_o = L_2 \frac{dI_{L2}}{dt} = L_2 \frac{I_{L2m} - I_{L2p}}{(1 - d - d_0)Ts}.
\]

\[
(15)
\]

3) Mode III \(((T_1 + T_2) \leq T < T_o)\): This mode starts when the current through the diode \(D\) becomes zero. The diode turns off and blocks the current flowing through \(S_3\). The current path in this mode is \(V_{dc}\)-grid along with its filter- \(S_4 - L_2 - C_1 - L_1 - V_{dc}\) as shown in Fig. 3(c). Since \(V_{C1} = V_{dc} - V_o\), the currents in the inductors will remain unchanged in this mode. Hence

\[
I_{L1m} = I_{L1v} = -I_{L2m} = -I_{L2v}.
\]

\[
(16)
\]

Solving (12)–(16), the expression for the voltage gain can be obtained as

\[
\frac{V_o}{V_{dc}} = -\frac{d}{(1 - d - d_0)}.
\]

\[
(17)
\]

C. Combined Operation

From (10) and (17), the common expression for the voltage gain can be written as

\[
\frac{V_o}{V_{dc}} = \frac{d}{(1 - d - d_0)}.
\]

\[
(18)
\]

It may be noted that the term, \(d_0\) exists in the expression for the voltage gain in (18). However, its value depends on the instant when the diode \(D\) turns off, which cannot be controlled externally. Similar to the buck–boost converter operating in DCM, the span of the interval \((d_0Ts)\) when both the switch and the diode are not conducting, is a function of the load. Hence \(d_0\) can be eliminated from the voltage gain expression by suitably replacing it with the equivalent load resistance.
From (3) and (11), it can be inferred that the expression for \( V_{C1} \) is different in the PHC and in the NHC. By substituting the expression of \( V_{C1} \) from (3) and (11) to (4), (5), (6), (7), (12), (13), (14), and (15), the model of the system can be simplified as follows:

\[
L_1 \frac{\Delta I_{L1}}{dT_s} = L_2 \frac{\Delta I_{L2}}{dT_s} = V_{dc} \quad (19)
\]

\[
L_1 \frac{\Delta I_{L1}}{(1 - d - d_0)T_s} = L_2 \frac{\Delta I_{L2}}{(1 - d - d_0)T_s} = |V_o| \quad (20)
\]

From Fig. 4, in both the half cycles the expression of switching time average of the dc side current is obtained as

\[
I_{dc} = I_{L1v} + \frac{\Delta I_{L1}}{2}(1 - d_0). \quad (21)
\]

Further, from Fig. 4 it can be observed that in the PHC the wave shape of \( i_2 \) in a switching time period is different from that in the NHC. Let the switching time average of \( i_2 \) be \( I_2 \), and it can be approximated to be equal to the grid current \( i_o \). It can be noted that this waveform is exactly negative to that of \( i_2 \) in \( \text{Cuk} \) mode of operation. Hence, in this mode, \( I_2 \) is equal to the switching time average of \( i_{L2} \) but with a negative sign. Therefore

\[
|I_2|_{\text{Cuk}} = I_{L2v} + \frac{\Delta I_{L2}}{2}(1 - d_0). \quad (22)
\]

For \( \text{SEPIC} \) mode, \( I_2 \) can be expressed as

\[
|I_2|_{\text{SEPIC}} = \frac{1 - d - d_0}{2} (I_{L1p} + I_{L2p}) = \frac{(1 - d - d_0)}{2} (\Delta I_{L1} + \Delta I_{L2}). \quad (23)
\]

Assuming the system to be loss-less

\[
\frac{I_{dc}}{I_{2}|_{\text{SEPIC}}} = \frac{V_o}{V_{dc}} = \frac{d}{(1 - d - d_0)}. \quad (24)
\]

Using (19), (21), and (23)

\[
\frac{(1 - d - d_0)}{2I_{L1v}} \frac{dT_s V_{dc}}{L_{eq}} = \frac{1 - d - d_0}{d} \quad (25)
\]

where \( L_{eq} = L_1 \parallel |L_2| \). Simplifying (25)

\[
I_{L1v} = \frac{d T_s V_{dc}}{2} \left[ \frac{d}{L_2} - \frac{(1 - d - d_0)}{L_1} \right]. \quad (26)
\]

If, \( I_{L1v} \) has to be positive

\[
\frac{L_2}{L_1} < \frac{d}{1 - d - d_0} = \frac{V_o}{V_{dc}} \quad (27)
\]

needs to be satisfied. However, in that case when \( V_o \) becomes zero at the zero crossing instants as per (27), \( L_2 \) needs to assume a negative value which is not possible. Hence the value of \( L_2 \) is chosen so that, \( I_{L1v} \) remains negative for all possible operating conditions.

In \( \text{SEPIC} \) mode of operation, the average current through \( L_2 \) is given by

\[
I_{L2} = I_{L2v} + \frac{\Delta I_{L2}}{2}(1 - d_0) = (1 - d - d_0) \frac{dT_s V_{dc}}{2L_{eq}}
\]

\[
= \frac{(1 - d - d_0)}{2} (\Delta I_{L1} + \Delta I_{L2}). \quad (28)
\]

From (23) and (28) it can be inferred that \( I_2 \) is equal to \( I_{L2} \) in \( \text{SEPIC} \) mode of operation as well. Hence in the combined operation, \( I_{L2} = |I_2| \), which means that, \( i_{L2} \) can be manipulated to control \( i_o \). Since the absolute value of the output current expression is the same in both the half cycles it can be inferred that (26) and (27) are also valid for \( \text{Cuk} \) mode of operation as well. Therefore, the design condition for \( L_2 \) remains the same in both the half cycles.

Substituting \( I_{L1v} \) in (21)

\[
I_{dc} = \frac{d^2 T_s V_{dc}}{2 L_{eq}}. \quad (29)
\]

Since the output voltage and current is sinusoidal and they are in phase with each other

\[
I_{dc}(t) = 2 I_{pv} \sin^2 \omega t \quad (30)
\]

wherein \( I_{pv} \) is the average current drawn from PV module. Further, \( V_{pv} = V_{dc} \) and \( D(t) \) being positive, its expression can be written as

\[
d(t) = d_{peak} \sin \omega t \quad \text{where,} \quad d_{peak} = 2 \sqrt{\frac{I_{pv} L_{eq}}{T_s V_{pv}}}. \quad (31)
\]

Hence, \( d(t) \) needs to be a rectified sine wave with an amplitude of \( d_{peak} \). The value of \( d_{peak} \) will be dictated by the irradiance level experienced by the solar PV module.

1) Voltage Gain Considering Resistive Load: Considering the load resistance as \( R_o \), and the system to be loss-less, (29) can be rewritten as

\[
\frac{V_o^2}{R_o} = \frac{d^2 T_s V_{dc}^2}{2 L_{eq}} \Rightarrow \frac{V_o}{V_{dc}} = d \sqrt{\frac{T_s R_o}{2 L_{eq}}}. \quad (32)
\]

From (32) it can be inferred that although the voltage gain expression of (18) is having the term \( d_0 \), the voltage gain of the inverter can be expressed independent of \( d_0 \).

IV. SELECTION OF PARAMETERS

A. Design of Inductor (\( L_1 \))

For the limiting case when the inverter operates at the verge of discontinuity at the peak of the grid voltage, and operating at the rated condition

\[
d \leq \frac{v_o}{v_o + V_{dc}} = \frac{V_{om}}{V_{om} + V_{pv}}
\]

where \( V_{om} \) is the amplitude of the grid voltage, \( v_o \). At this instant, the switching time average of \( i_{L1} \) is \( 2 I_{pv} \). Hence

\[
L_1 = \frac{d T_s V_{pv}}{4 I_{pv}} \leq \frac{T_s V_{om} V_{pv}}{4 I_{pv} (v_o + V_{om})}. \quad (33)
\]

B. Design of Intermediate Capacitor (\( C_1 \))

As the average voltage of \( v_{C1} \) is less during \( \text{SEPIC} \) mode of operation, the voltage ripple of \( C_1 \) is much higher in this mode compared to the operation of the inverter in the \( \text{Cuk} \) mode. Hence, the design of \( C_1 \) is carried out considering the operation
of the inverter in SEPIC mode which is as follows:
\[
C_1 = \frac{\Delta Q_{C1}}{\Delta V_{C1}} = \frac{(1 - d - d_o)T_s I_{L1\text{PV}}}{2V_{pv}} \left( \frac{\Delta V_{C1}}{V_{C1}} \right) = \frac{(dT_s)^2 V_{pv}}{2V_o L_1 \left( \frac{\Delta V_{C1}}{V_{C1}} \right)}.
\]

**C. Design of Output Inductor (L₂)**

The switching time average current through \( L_2 \) is the current fed to the grid during this interval. The current ripple in \( L_2 \) is derived and subsequently the design criterion of \( L_2 \) is obtained as follows:
\[
\Delta I_{L2} = \frac{dT_s V_{dc}}{L_2} \Rightarrow L_2 = \frac{dV_{pv} T_s}{L_o \left( \frac{\Delta I_{L2}}{I_o} \right)}.
\]

**D. Design of Output Capacitor (C₂)**

The output capacitor is chosen so that the cutoff frequency, \( f_c = \frac{1}{2\pi \sqrt{L_2 C_2}} \), is significantly above the grid frequency \( f_g \) and well below the switching frequency \( f_s \), i.e., \( f_g << f_c << f_s \), and hence, the value of \( C_2 \) is obtained to be
\[
C_2 = \frac{1}{4\pi^2 f_c^2 L_2}.
\]

**E. Design of C \(_{\text{cap}}\) and L \(_{\text{cap}}\)**

It is assumed that during a switching cycle \( v_{\text{cap}} \) is constant. The expression for \( C_{\text{cap}} \) is given by
\[
C_{\text{cap}} = \frac{P}{2\pi f_g V_{\text{cap}} \Delta V_{\text{cap}}}.
\]
where, \( P \) is the rated power supplied by the PV source, \( V_{\text{cap}} \) and \( \Delta V_{\text{cap}} \) is the average capacitor voltage and its maximum allowable peak to peak second harmonic ripple, respectively.

Since hysteresis current control is employed, the switching frequency is not constant in a cycle of the utility voltage. The switching time period of APDC for a given operating point is given by
\[
T_s = \frac{2I_h L_{\text{cap}}}{V_{dc}} \left( \frac{1}{V_{\text{cap}}} + \frac{1}{v_{\text{cap}} - V_{dc}} \right) = \frac{2I_h L_{\text{cap}}}{V_{dc}} \left( 1 - \frac{V_{dc}}{v_{\text{cap}}} \right)
\]
where, \( 2I_h \) is the bandwidth of the hysteresis controller. Hence from \( (39) \) at maximum allowable switching frequency \( f_{s,\text{max}} \) is given by
\[
L_{\text{cap}} \geq \frac{V_{dc} \left( 1 - \frac{V_{dc}}{v_{\text{cap,\text{max}}} - V_{dc}} \right)}{2f_{s,\text{max}} I_h}
\]
where the maximum value of capacitor voltage \( v_{\text{cap,\text{max}}} \) is \( V_{\text{cap}} + \frac{\Delta V_{\text{cap}}}{2} \).

The system parameters chosen for simulating the microinverter is provided in Table I.

The inverter parameters (see Table II) are obtained by substituting the system parameters in \( (33), (34), (35), (36), (37), \) and \( (39) \). The ESR of the inductors and the capacitors are also provided.

### Table I

| Parameters | Values |
|-----------|--------|
| \( V_{\text{mpp}} \) and \( V_{\text{oc}} \) at STC\(^2\) | 34.7 V and 44 V |
| \( I_{\text{mpp}} \) and \( I_{\text{sc}} \) at STC | 6.35 A and 6.6 A |
| MPP power, \( P_{\text{mpp}} \) at STC | 220.34 W |
| Grid voltage (rms), \( V_g \) | 220 V |
| Grid frequency, \( f_g \) | 50 Hz |
| Switching frequency, \( f_s \) | 50 kHz |

\(^1\text{V}_{\text{oc}}\): Open circuit voltage of the PV module
\(^2\text{STC}: \) Standard test condition (Solar Insolation=1 kW/m\(^2\), Temp.=25°C)
\(^3\text{I}_{\text{sc}}\): Short circuit current of the PV module

### Table II

| Parameters | Values |
|-----------|--------|
| \( L_1 \), \( \tau L_1 \) | 16 \( \mu \)H, 15 mΩ |
| \( C_1 \), \( \tau C_1 \) | 0.94 \( \mu \)F, 6.5 mΩ |
| \( L_2 \), \( \tau L_2 \) | 0.47 \( \mu \)H, 13 mΩ |
| \( L_{\text{cap}} \) | 1 mH, 0.195 Ω |
| \( C_{\text{cap}} \) | 200 \( \mu \)F |

### Fig. 5

Block diagrams of control configurations. (a) Controller for the main inverter. (b) Controller for the APDC.

### V. CONTROL CONFIGURATION

The schematic block diagram of the controller of the proposed microinverter is shown in Fig. 5. In order to draw the maximum available power from the solar PV module, incremental conductance-based MPPT algorithm has been incorporated [29]. The MPP controller provides the reference \( i_{\text{pv}}^* \) to be maintained at the terminal of the solar PV module. This reference is compared with the measured voltage of the PV module, and the error so generated is processed through the PI controller, PI-1 to generate the peak reference \( I_{L2} \) for \( i_{L2} \). Since the switching time average of \( i_{L2} \) in a switching cycle is equal to that of the output current \( i_o \), the output current can be controlled by controlling \( i_{L2} \). The instantaneous reference current \( i_{L2}^* \) is obtained by multiplying \( I_{L2} \) with a rectified sine wave template. This sine wave template is generated from the grid by using single-phase enhanced PLL method [30]. This reference \( i_{L2}^* \) is compared with the measured \( i_{L2} \), and the error is processed through the PI controller \( C(s) \) to generate \( d \). The feed-forward component \( \bar{d} \), which can be obtained from \( (31) \) is added with \( d \) to obtain the duty ratio \( d \).
The schematic block diagram of the control configuration for the APDC is shown in Fig. 5(b). The second-order harmonic component of the inverter current is extracted through a filter which is realized by means of a second-order generalized integrator SOGI-1. The dc component of \( v_{cap} \) is extracted by subtracting the second-order harmonic component from it which is then compared with the reference \( V_{cap}^* \). The error is processed through the PI controller, PI-2, and the output is subtracted from the output of SOGI-1 to obtain the reference \( i_{lap}^* \). The sensed current \( i_{lap} \) is then compared with \( i_{lap}^* \) and the error so generated is passed through a hysteresis controller to determine the switching instance for \( S_{bs} \) and \( S_{ls} \).

### A. Mathematical Model of the System

Applying the state space averaging technique over a switching cycle for both the half cycles and the transfer functions \( G_s(s) \) and \( G_c(s) \) for PHC and NHC, respectively, can be obtained through small signal modeling. Considering the system and inverter parameters as depicted in Tables I and II along with the steady-state variables \( i_{L1}, i_{L2}, i_{ap}, v_{C1}, v_{C2} \) at STC, the transfer functions \( G_s(s) \) and \( G_c(s) \) are obtained and are provided in (40) and (41) shown at the bottom of this page, respectively.

The values of \( K_p \) and \( K_i \) in \( C(s) \) are 6.67 \( \times \) 10\(^{-5} \) and 5 \( \times \) 10\(^{-4} \), respectively. The frequency response of \( G_s(s) \), \( G_c(s) \), \( G_s(s)C(s) \) and \( G_c(s)C(s) \) are shown in Fig. 6. From this figure, it can be inferred that the closed-loop system has a gain and phase margin of 15.7 dB, 85.1° for \( G_s(s)C(s) \) and 18.6 dB, 82.6° for \( G_c(s)C(s) \) which impart sufficient stability margin for the closed-loop system.

### VI. Simulated Performance of the System

Detailed simulation studies of the proposed microinverter have been carried out on MATLAB/Simulink platform. The parameters depicted in Tables I and II are used to simulate the system. In order to evaluate the performance of the system the solar insolation level is varied as depicted in Table III. The slope considered for variation is chosen to be 1 kW/m\(^2\)/s, which is more steeper than realistic situations. The values of \( K_p \) and \( K_i \) in PI-1 are 0.04 and 4 s\(^{-1} \), respectively, while the values of \( K_p \) and \( K_i \) in PI-2 are 0.02 and 1 s\(^{-1} \), respectively.

The power drawn from the PV source and the level of irradiance are shown in Fig. 7. The voltage across the PV module and its current are shown in Fig. 8. From Fig. 7 it can be observed that the maximum power point has been tracked appropriately.

\[
G_s(s) = \left. \frac{\frac{1}{L_2}(s)}{d(s)} \right|_s = \frac{-44.47 s^4 + 6.909 \times 10^{10} s^3 + 5.832 \times 10^{13} s^2 + 2.325 \times 10^{20} s + 1.122 \times 10^{23}}{s^5 + 880.5 s^4 + 8.286 \times 10^9 s^3 + 4.913 \times 10^{12} s^2 + 1.56 \times 10^{19} s + 5.298 \times 10^{24}}
\]

(40)

\[
G_c(s) = \left. \frac{\frac{1}{L_2}(s)}{d(s)} \right|_c = \frac{-54.87 s^4 + 6.777 \times 10^{10} s^3 + 5.769 \times 10^{13} s^2 + 1.442 \times 10^{20} s + 9.488 \times 10^{22}}{s^5 + 880.5 s^4 + 1.786 \times 10^{13} s^3 + 1.21 \times 10^{16} s^2 + 2.793 \times 10^{19} s + 7.635 \times 10^{24}}
\]

(41)
in sympathy with the variation in solar insolation level. The grid voltage and the grid current for the aforementioned variation in the solar insolation level is depicted in Fig. 9. While the system is negotiating at the maximum insolation level of 1 kW/m², the THD of the grid current is found to be 3.33%. The profile of the duty ratio \( d \) for the insolation levels of 400 W/m² and 1 kW/m² is shown in Fig. 10(a) and (b), respectively. The peak duty ratio at an insolation level of 1 kW/m² is found to be 0.7, while it is approximately 0.45 for 400 W/m² thereby validating (31).

### VII. EXPERIMENTAL VALIDATION

In order to confirm the viability of the proposed inverter, a 250 W semiengineered laboratory prototype of the microinverter is fabricated, and detailed experimental validations have been carried out. The passive elements as depicted in Table II are utilized to realize the prototype. The capacitors used are of thin film type to enhance the reliability of the system. The switch, \( S_1 \) is realized by the MOSFET, IPW60R024P7 while \( S_2 - S_5, S_{sh} \) and \( S_{sb} \) are realized by MOSFET, IPW60R037P7. The controller is implemented on TMS320F28335 platform using the trapezoidal method. In this method, the stability of the continuous system and its discretized form are equivalent irrespective of the choice of the time step. The time step for the discretization is chosen to be \( 25 \mu s \). A 1.5 kW programmable dc power supply (EPS power supply PSI 9360-15) is employed to emulate the PV module. The photograph of the prototype is shown in Fig. 11.

The measured performance of the proposed microinverter while it is interfacing a PV module of 35 V to a single-phase grid of 220 V, 50 Hz is depicted in Fig. 12. The irradiance is varied from 400 to 1000 W/m² in steps. The figure shows the voltage across the PV module, grid voltage, grid current, and the power fed to the grid. The magnified plots of the grid voltage and the grid current are also shown for 400 and 1000 W/m². It can be inferred from the figure that the proposed microinverter can extract power from a 35 V PV module as dictated by MPPT controller and feed sinusoidal current to the grid. It can be observed from Fig. 15 that the THD of the grid current is 3.18% while negotiating the irradiance level of 1000 W/m².

Fig. 13 shows the measured steady-state response of \( v_{C1}, i_{L1}, \) and \( i_{L2} \). It can be observed that during PHC \( v_{C1} \) is equal to the input voltage which confirms the SEPIC mode of operation. During NHC it can be noted that \( v_{C1} \) is equal to the sum of the input and output voltage which corroborates Ćuk mode of operation. The waveform of \( i_{L1} \) and \( i_{L2} \) are shown over a shorter time scale near the peak of the grid voltage. The peak magnitude of \( i_{L1} \) at full load is 30 A. It can also be inferred from the figure that the inverter operates in DCM while delivering rated power. The peak duty ratio is found to be 0.7 at this operating condition which matches with the value obtained through simulation at a solar irradiance of 1 kW/m².

The response of the APDC parameters are shown in Fig. 14. It can be observed that the APDC is supplying the second-order harmonic current required by the inverter. The voltage across
The measured and estimated efficiency versus load plots of the proposed microinverter are shown in Fig. 16. The measured efficiency of the main inverter while the inverter is negotiating the irradiance level of 1000 W/m² is 95.2%. The overall measured efficiency including the APDC is 94%.

VIII. COMPARISON OF THE PROPOSED MICROINVERTER WITH EXISTING TOPOLOGIES

The performance features of the proposed topology are compared with the topologies of transformerless microinverters reported in the literature, and are tabulated in Table IV. It can be observed from the table that the topology reported in [24], and the proposed one of this article are the only two cases designed for interfacing a 35 V PV module to a 220 V ac grid while all other topologies [12], [13], [14], [15], [17], [18], [19] are meant for interfacing a 35 V PV module to a 110 V ac grid. In order to objectively compare the efficiency of the proposed microinverter with that of the topologies suitable for 110 V grid operation, the efficiencies of the main inverter and the microinverter are calculated and the estimated overall efficiency is compared with the efficiency of the APDC. Since all the topologies have different ratings, the following benchmark conditions are chosen based on the objectives mentioned in section-I to compare them on a common base.

1) The rating of the PV module: 35 V, 220 W.
2) AC grid: 220 V, 50 Hz.
3) Maximum switching frequency: 50 kHz.
4) The maximum allowable ripple in the inductor currents is 20% of its average value for the inverters operating in CCM while for the inverters operating in DCM, the inductances are chosen in such a way so that it ensures DCM operation for all the possible operating conditions.
5) Maximum allowable ripple in $V_{pv}$ is 5%, while for the inverters having decoupling capacitors, the voltage rating of the decoupling capacitor is chosen to be 350 V with an allowable ripple of 10%.
6) The output L-C filters are not considered.

The component count, their ratings (estimated under the aforesaid benchmark conditions) and a few other features of the proposed microinverter is theoretically estimated while it is being made to interface a 50 V solar PV module to a 110 V ac grid. It can be inferred from Table IV that the estimated efficiency of the proposed microinverter under more or less similar operating conditions is higher than the reported efficiencies of the aforesaid topologies.

The parameters like: 1) total energy stored in the inductor $E_L$; 2) total energy stored in the capacitor $E_C$; 3) total VA rating of the switches $S_{sw}$ can be estimated for all the microinverter topologies for any given operating condition, as they do not depend on the type and quality of components used to realize the microinverter [4]. The aforesaid parameters can be expressed as follows:

$$E_L = \frac{1}{2} \sum_{i=1}^{N_L} L_i I_{pk,i}^2; \quad E_C = \frac{1}{2} \sum_{j=1}^{N_C} C_j V_{pk,j}^2;$$

$$S_{sw} = \sum_{m=1}^{N_{sw}} \frac{V_{pk,m}}{I_{pk,m}}.$$

While the volume of the inductors and capacitors depends on the parameters $E_L$ and $E_C$ respectively, $S_{sw}$ decides the overall rating of the MOSFETs used. Since the ratings of the microinverters under consideration are different, the following benchmark conditions are chosen based on the objectives mentioned in section-I to compare them on a common base.

1) The rating of the PV module: 35 V, 220 W.
2) AC grid: 220 V, 50 Hz.
3) Maximum switching frequency: 50 kHz.
4) The maximum allowable ripple in the inductor currents is 20% of its average value for the inverters operating in CCM while for the inverters operating in DCM, the inductances are chosen in such a way so that it ensures DCM operation for all the possible operating conditions.
5) Maximum allowable ripple in $V_{pv}$ is 5%, while for the inverters having decoupling capacitors, the voltage rating of the decoupling capacitor is chosen to be 350 V with an allowable ripple of 10%.
6) The output L-C filters are not considered.

The component count, their ratings (estimated under the aforesaid benchmark conditions) and a few other features of the proposed microinverter are compared with the topologies of transformerless microinverters reported in the literature, and are tabulated in Table IV. It can be observed from the table that the topology reported in [24], and the proposed one of this article are the only two cases designed for interfacing a 35 V PV module to a 220 V ac grid while all other topologies [12], [13], [14], [15], [17], [18], [19] are meant for interfacing a 35 V PV module to a 110 V ac grid. In order to objectively compare the efficiency of the proposed microinverter with that of the topologies suitable for 110 V grid operation, the efficiencies of the main inverter and the microinverter are calculated and the estimated overall efficiency is compared with the efficiency of the APDC. Since all the topologies have different ratings, the following benchmark conditions are chosen based on the objectives mentioned in section-I to compare them on a common base.

1) The rating of the PV module: 35 V, 220 W.
2) AC grid: 220 V, 50 Hz.
3) Maximum switching frequency: 50 kHz.
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5) Maximum allowable ripple in $V_{pv}$ is 5%, while for the inverters having decoupling capacitors, the voltage rating of the decoupling capacitor is chosen to be 350 V with an allowable ripple of 10%.
6) The output L-C filters are not considered.

The component count, their ratings (estimated under the aforesaid benchmark conditions) and a few other features of the proposed microinverter are compared with the topologies of transformerless microinverters reported in the literature, and are tabulated in Table IV. It can be observed from the table that the topology reported in [24], and the proposed one of this article are the only two cases designed for interfacing a 35 V PV module to a 220 V ac grid while all other topologies [12], [13], [14], [15], [17], [18], [19] are meant for interfacing a 35 V PV module to a 110 V ac grid. In order to objectively compare the efficiency of the proposed microinverter with that of the topologies suitable for 110 V grid operation, the efficiencies of the main inverter and the microinverter are calculated and the estimated overall efficiency is compared with the efficiency of the APDC. Since all the topologies have different ratings, the following benchmark conditions are chosen based on the objectives mentioned in section-I to compare them on a common base.

1) The rating of the PV module: 35 V, 220 W.
2) AC grid: 220 V, 50 Hz.
3) Maximum switching frequency: 50 kHz.
4) The maximum allowable ripple in the inductor currents is 20% of its average value for the inverters operating in CCM while for the inverters operating in DCM, the inductances are chosen in such a way so that it ensures DCM operation for all the possible operating conditions.
5) Maximum allowable ripple in $V_{pv}$ is 5%, while for the inverters having decoupling capacitors, the voltage rating of the decoupling capacitor is chosen to be 350 V with an allowable ripple of 10%.
6) The output L-C filters are not considered.

The component count, their ratings (estimated under the aforesaid benchmark conditions) and a few other features of the
TABLE V

TOPOLOGICAL COMPARISON OF THE PROPOSED TOPOLOGY WITH EXISTING TRANSFORMERLESS MICROINVERTER TOPOLOGIES

| Topology | Component count | Dual grounding | Operation | \( E_L \) (mJ) | \( E_C \) (J) | \( S_{\text{sw}} \) (kVA) | \( d_{\text{max}} \) | Isolated dc source reqd. |
|----------|-----------------|----------------|-----------|---------------|--------------|----------------|--------|---------------------|
| [12]     | 2+3\#           | LF, LF        | Yes       | 41            | 0            | 4              | 10.0   | 0.91                |
| [13]     | 1+4\#           | LF, LF        | Yes       | 50            | 7.4          | 4              | 9.91   | 4                   |
| [14]     | 4\#             | LF, LF        | Yes       | 24            | 7.4          | 21.3           | 0.9    | 3                   |
| [15]     | 2+3\#           | LF, LF        | Yes       | 38.6          | 4            | 9              | 0.91   | 4                   |
| [17]     | 1+4\#           | LF, LF        | Yes       | 4.5           | 7.4          | 26             | 0.77   | 4                   |
| [18]     | 3               | LF, LF        | Yes       | 46.6          | 7.4          | 15.4           | 0.9    | 3                   |
| [19]     | 1+4\#           | LF, LF        | Yes       | 27            | 7.4          | 17.1           | 0.9    | 5                   |
| [24]     | 1               | 4+2\#         | No        | 9.2           | 7.4          | 11.8           | 0.67   | 4                   |
| Proposed | 1               | 4+2\#         | Yes       | 8             | 7.4          | 14.7           | 0.7    | 3                   |
| Proposed*| 3               | 4+2\#         | Yes       | 13            | 3            | 15.9           | 0.7    | 4                   |

\# two switches operate at double LF
\* including APDC
\# these switches operate at HF during either PHC or NHC

S: Switch
D: Diode
L: Inductor
C: Capacitor
BCM: Boundary conduction mode

The proposed topology is compared with the existing microinverter topologies, and are tabulated in Table V.

From this table, it can be observed that, the number of switches in the main inverter of the proposed topology is five, which is the same as that of the topologies reported in [12], [13], [15], and [19]. But then all the five switches in the aforementioned topologies are operated in HF in at least one half cycle of the grid voltage, whereas in the case of the proposed topology, four out of the five switches operate in LF, which reduces the switching losses significantly. The topologies reported in [17] and [24] require six and seven switches, respectively, which are higher than that of the proposed topology whereas topologies reported in [14] and [18] require less number of switches. The number of isolated dc power supplies required for the main inverter of the proposed topology is three which is the same as that of [14] and [18] whereas in the case of all other topologies, the number of isolated dc power supplies required is more than three.

It can be also inferred from Table V that for the chosen benchmark conditions, the maximum duty ratio of the proposed microinverter is 0.7, which is less than any other topologies except that of [24], where a coupled inductor is used. However, the presence of leakage inductance of the coupled inductor causes voltage spike across the switch which has to be limited by employing an additional snubber circuit. This issue does not arise in the proposed topology, and hence the snubber circuit is not required. For other topologies operating in CCM, the maximum duty ratio required is 0.9 or more, which reduces the efficiency significantly. Though the maximum duty ratio is minimum in [24], the major disadvantage of this topology is that the leakage current issue is not addressed. All the other topologies under comparison including the proposed topology is dually grounded, thereby eliminating the path for the leakage current flow.

In terms of the total switch kVA rating under benchmark condition, \( S_{sw} \) of the proposed main microinverter topology is higher than that of the topologies presented in [12], [15], and [24]. On the other hand, the value of \( E_L \) for the proposed topology is higher than that of [17], but then the value of \( S_{sw} \) for [17] is significantly high. The value of \( E_L \) in the topologies of [12], [13], [14], [15], [18], and [19] are significantly high. Though in [24], the value of \( S_{sw} \) is lower and \( E_L \) is slightly higher than those of the proposed topology, the flow of leakage current is not eliminated in the case of the topology of [24].

It can also be observed from Table V that the value of \( E_C \) in the case of the proposed topology when the APDC is replaced by a decoupling capacitor is similar to that of the topologies reported in [13], [14], [17], [18], [19], and [24]. In [12] and [15], the value of \( E_C \) is significantly less, but then the problems associated with these topologies have already been mentioned. When the combination of APDC and the proposed main microinverter is considered as a combined unit, the value of \( E_C \) becomes minimum among the topologies under consideration while \( E_L \) and \( S_{sw} \) increase slightly compared to the case when APDC is not used. The number of isolated dc power supply required in this case increases to four, which is the same as that of [12] and [15]. Even if the APDC is included, the value of \( E_L \) remains significantly low compared to that of [12] and [15].

Hence, it can be inferred from the table that the proposed microinverter is an effective means for interfacing a 35 V PV module to a 220 V grid with negligible leakage current flow, while having enhanced reliability.

IX. CONCLUSION

A novel SEPIC-Čuk-based solar PV microinverter was proposed in this article. The salient features of the proposed inverter were as follows:
1) The microinverter was capable of interfacing a 35 V PV module to a 220 V ac grid.
2) The main microinverter was realized using only one HF switch thereby reducing the switching losses.
3) The inverter was operated in DCM, which ensured high voltage gain and zero turn ON loss for the HF switch.
4) Since the negative terminal of the PV module was connected directly to the grid neutral, the leakage current flow was negligible.
5) The employment of the APDC reduced the value of the PV module capacitor. Hence all the capacitors of the microinverter were realized by thin film capacitors thereby enhancing the reliability of the system.

The principle of operation of the proposed microinverter along with its rigorous analyses were presented. The design guidelines for the passive components were provided. A 250 W semi- engineered laboratory prototype of the inverter was fabricated, and the viability of the microinverter was confirmed by performing detailed simulation and experimental studies.

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