Noise limited computational speed

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(Dated: February 1, 2008)

In modern transistor based logic gates, the impact of noise on computation has become increasingly relevant since the voltage scaling strategy, aimed at decreasing the dissipated power, has increased the probability of error due to the reduced switching threshold voltages. In this paper we discuss the role of noise in a two state model that mimic the dynamics of standard logic gates and show that the presence of the noise sets a fundamental limit to the computing speed. An optimal idle time interval that minimizes the error probability, is derived.

PACS numbers: 05.10.Gg, 89.20.Ff, 85.40.Qx

The role of noise in computation devices has become increasingly relevant both in the quantum\cite{1, 2} and in the classical\cite{3, 4} regime. With the present tendency to scale down CMOS based devices toward the nanometer region\cite{5, 6}, the noise immunity in a low energy dissipation scenario has become the recurring objective of significant research efforts in this field\cite{7, 8}. Some authors have focused their attention on the potential role of noise in nanoscale devices where noise driven dynamics\cite{9} has been invoked to explain the experiments and to optimize future design\cite{10}. In order to address a non-negligible error probability a number of strategies have been devised where a probabilistic approach to the computational task has been often invoked\cite{11}. In this letter we focus our attention on the very basic mechanisms of the switch dynamics that are responsible of the functioning of traditional transistor based logic gates, with the aim of clarifying the impact of noise on computation errors.

Noise can affect the functioning of computing devices in a number of different ways. To fix our ideas let’s consider a simple logic gates that constitute the building block of complex networks aimed at realizing computing tasks in modern electronic devices. Here the noise has two deleterious effects: first, it can interact with an unperturbed static signal causing the loss of information carried by the static node of the computational network; second, it can affect the functioning of a switching node by altering its dynamical properties (e.g.: slew, delay). In this letter we deal with the second effect. More precisely, we focus our attention on the very basic mechanism of the switching event in a logic gate. Reduced to the essential this mechanism can be sketched as an output change in response to a threshold-crossing event. For the sake of simplicity we consider here the simpler of the various switching computing elements: the Logic Inverter or NOT gate. This gate is usually operated as a pure switching device, governed by the following rule: the output logic state commutes from 1 (or HIGH) to 0 (or LOW) if the input signal crosses from below the upper switching threshold $b_u$ (transition from LOW to HIGH).

As shown in Fig.1 (left hand side) a time delay between input and output occurs: before the output signal is stable in the desired logic state, some time is required after the application of the input signal. The amount of such a delay, called propagation delay, $t_p$, characterizes the different Logic Families (TTL, CMOS, ECL,...) and ranges between few ns and few tens of ns. A significant contribution to the propagation delay is given by the rise time $t_r$ that in turn affects what is usually called the slew rate of the device. The separation voltage between the up and down thresholds, $b_u - b_d$, depends on the different Families and ranges from 0.7 V in ECL logic to around 28 V in relay logic.

A number of different noise induced phenomena, ranging from switching delays (see e.g. noise on timing and noise-on-delay effects) to bit-flip errors, threaten the correct functioning of threshold-crossing based logic gates. Main physical noise sources being power supply noise, environmental noise and also thermal noise when the devices dimensions hit the nanoscale. In order to model the dynamical effects of the noise on the switching mechanism we sketched in fig.1 (right hand side) a common scenario. Here, the time diagram shows the input and output time series for the case where the input signal is affected by noise of intensity comparable with the threshold separation. For generality purpose we considered the case of exponentially correlated, Gaussian distributed, stationary noise with correlation time $\tau$ and standard deviation $\sigma$. This noise is added to the deterministic signal shown in the leftmost part of the figure and the resulting signal is presented in the upper diagram. The effect of the noise in the gate response (output time series, lower diagram) is twofold: 1) it can initially prevent the input signal from crossing the relevant threshold ($b_u$ in the example) postponing in time this event and thus resulting in a longer propagation delay $t_p$ (delayed switching error). 2) Once the device switching is completed, it might cause a re-crossing of the opposite threshold ($b_d$ in the example) causing a bit-flip error.

In the following we will analyze in detail the statistics of these two events that directly reflects into the compu-
tational error probability.

1) delayed switching. The delayed switching error is produced when the NOT gate, expected to be in the LOW state is found instead still in the HIGH state due to a delayed switch. This error is clearly time dependent and we are interested in estimating how its probability evolves with time. In order to have a switch delayed, two conditions have to be met:

a) at time \( t = t_0 \), due to the presence of noise, the input signal of amplitude \( i_u \) that makes the device commute from HIGH to LOW cannot reach the switching threshold \( b_u \). This happens when \( i_u + \xi_0 < b_u \), or \( \xi_0 < b_u - i_u = b_c \), where \( \xi_0 = \xi(t_0) \) is the instantaneous value of the noise (a realization of the stochastic process \( \xi(t) \) sampled at \( t = t_0 \)). Such an event happens with probability:

\[
P_{1a} = \Phi \left( \frac{b_c}{\sigma} \right) = \frac{1}{2} (1 + \text{Erf}(\overline{b_c}))
\]  

(1)

where \( \text{Erf}(x) \) indicates the Error-function and \( \overline{b_c} = b_c/(\sqrt{2}\sigma) \).

b) At time \( t > t_0 \) the noise is such that the condition \( \xi(t) < b_u - i_u \) still holds. This second condition is satisfied with probability \( P_{1b} \) that can be estimated as follows [12]. Once the condition a) is satisfied (\( \xi_0 < b_c \)) it can take some time before the input signal reaches the upper threshold \( b_u \). This delay can be estimated by considering the so-called First Passage Time (FPT), i.e. the time the stochastic process \( \xi(t) \) takes to reach \( b_c \) (i.e. to go from \( \xi(t_0) < b_c \) to \( b_c \) with absorbing boundary in \( b_c \) and reflecting boundary in \( -\infty \)). This delay is a random variable \( t \) whose mean value \( < t > = T_1 \) is called MFPT and whose probability density function \( p_1(t) \) is exponential [13, 14]. The error probability \( P_{1b} \) coincides with the probability that in the time interval \([t_0, t]\) there was no crossing of \( b_c \), i.e.:

\[
P_{1b}(t_0, t) \equiv 1 - \int_{t_0}^{t} p_1(t) \, dt = e^{-\frac{(i_u - \xi_0)}{\tau}}
\]  

(2)

The relevant time \( T_1 \) is a function of the noise characteristics [12]:

\[
T_1(b_c) = \tau \left[ \overline{b_c} \int_{-\infty}^{\overline{b_c}} \int_{-\infty}^{\overline{b_c}} e^{-z^2 + x^2} (1 + \text{Erf}(x)) \, dx \, dz \right]
\]  

(3)

Where \( N = \frac{1}{2} (1 - \text{Erf}(\overline{b_c})) \).

Finally the delayed switching error probability is obtained by the combination of the two error probabilities:

\[
P_1(t_0, t) = P_{1a} P_{1b} = \Phi \left( \frac{b_c}{\sigma} \right) e^{-\frac{(i_u - \xi_0)}{\tau}}.
\]  

(4)

Having obtained the expression for the error probability \( P_1 \) we can now derive a useful prediction for operating the NOT gate in noisy conditions. In Fig.2 the delayed switching error probability \( P_1 \) is shown as a function of \( t/\tau \). As expected this probability decreases with time and becomes negligible in the long time. If we fix what we consider an acceptable error probability \( \epsilon \), than we can easily compute a safe wait time \( t_w \) after which the
error probability stays below $\epsilon$, i.e. $P_1 < \epsilon$ when $t > t_w$. The relation between $t_w$ and $\epsilon$ is easily obtained from eq. (4) as

$$t_w = T_1 \ln \left( \frac{\Phi(b_c/\sigma)}{\epsilon} \right)$$

(5)

where for simplicity we have assumed $t_0 = 0$. Most notably, if we are willing to accept an error probability $\epsilon = \Phi(b_c/\sigma)$ or greater, the wait time $t_w$ amounts to zero.

![FIG. 2: (Color online) Computational error probability. The delayed switching error probability $P_1$ is shown as a function of $t/\tau$ (red online) together with the bit-flip error probability $P_2$ (blue online) and the resulting total error probability $P_e$ (black online). Parameter values: $\tau = 10^{-3}$ s and $\sigma = 1$ V, $i_u = 4.2$ V, $b_u = 4.0$ V, $b_c = 0.2$ V. As an example, an error probability $\epsilon = 0.3$ line is drawn across the curves. The intercepts at $t_w$ and $t_h$ respectively are drawn (down arrows). Inset: normalized wait time $t_w/\tau$ versus $\sigma/b_c$ for different values of the error probability (from above): $\epsilon = 10^{-1}$ (green), $\epsilon = 10^{-3}$ (black), $\epsilon = 10^{-5}$ (red), $\epsilon = 10^{-7}$ (blue). Theoretical predictions (continuous line) are in close agreement with digital simulation (crosses).

2) bit-flip: Operationally, notwithstanding the delayed switching error, it would seem that we can still use the NOT gate with a negligible error probability, provided we are willing to wait long enough (longer than $t_w$). Unfortunately there is another error that comes into play if we want to wait too long: the bit-flip error. As shown in Fig.1, after a switch event (HIGH to LOW) occurs, a new unwanted switch can occur in the opposite direction (LOW to HIGH), if the noise assumes a value $\xi(t) < b_d - i_u = c_e$ at a time $t$, while the input signal is still $i_u$. For practical purposes also a bit-flip error of short duration is deleterious to the signal integrity and can seriously compromise the functioning of the logic gate. To estimate the bit-flip error probability $P_2$, let’s assume that at $t = t_0$ there is a switch event (HIGH to LOW), i.e.: $\xi(t_0) \geq b_e$. We are interested in computing the time $t$ the stochastic process $\xi(t)$ takes to reach $c_e$ (i.e. to go from $\xi(t_0) \geq b_e$ to $c_e$ with absorbing boundary in $c_e$ and reflecting boundary in $+\infty$). This time $t$ is a random variable whose mean value is $T_2$ (MFPT) and whose probability density function $p_2(t)$ is exponential[12]. For what we said, $P_2(t_0, t)$ represents the probability that there was a crossing of $c_e$ in the time interval $[t_0, t]$.

$$P_2(t_0, t) = \int_{t_0}^{t} p_2(t) \, dt = 1 - e^{-\frac{t - t_0}{\tau}}.$$  

(6)

The relevant time $T_2$ can be computed as[12]:

$$T_2(t_e, t_w) = \frac{\tau}{N} \int_{t_e}^{t_w} \int_{t_e}^{t_w} e^{-z^2 + z^2} (1 - \text{Erf}(x)) \, dx \, dz$$

(7)

In Fig.2 $P_2$ is shown as a function of $t/\tau$. As expected this probability increases with time and approaches unity when $t$ grows to infinity.

For the bit-flip error, once we fix an acceptable error probability $\epsilon$, we obtain a safe hurry time $t_h$ before which the error probability stays below $\epsilon$. The relation between $t_h$ and $\epsilon$ is easily obtained from eq. (6) as

$$t_h = -T_2 \ln(1 - \epsilon),$$

(8)

where we have assumed $t_0 = 0$.

Finally, if we take into account the two errors previously discussed, we are now in position to express the total error probability: $P_e = P_1 + P_2$. $P_e$ is also shown in Fig.2. It is apparent that $P_e$ has a minimum for $t = t_m$ with $t_w < t_m < t_h$. Operatively, if we fix an acceptable error probability $\epsilon$ this identifies an idle time interval $(t_{is}, t_{ie})$ of amplitude $\Delta T_i = t_{ie} - t_{is}$, where the total error probability $P_e$ is smaller than $\epsilon$. When $T_1 \ll T_2$ we can approximate $t_{ie}$ with $t_h$ and $t_{is}$ with $t_w$, thus $\Delta T_i \approx t_h - t_w$. It is worth noticing that one of the consequences of this analysis is that $P_e$ assumes a minimum value identified by the condition $t_{is} = t_{ie} = t_{m}$. This implies that when operating a logic gates in the presence of noise, the probability of error cannot be made arbitrarily small but only as small as $\epsilon_m = P_e(t_m)$. Remarkably $\epsilon_m$ does not depend on the noise correlation time but only on the noise intensity[13].

The role of noise in computing devices however can also be seen from a different perspective. Instead of being a mere disturbance it can be considered as an essential part in the computing process itself. This is the case for example, when we consider sub-threshold gate driving, i.e. when $i_u < b_u$. In the absence of noise no switch is possible and the gate cannot operate. Instead, also a noise of small intensity can bring (in due time) the input signal above the threshold and thus drive the gate for the
input signal amplitude and the threshold value can seri-
of intensity comparable with the difference between the
becomes negligible.

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two scenarios (supra- and sub-threshold) are compared.
In Fig. 3 the error probabilities for the
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computational task. Scenarios where the noise can play a
beneficial role are not new in the literature; see e.g. the
Stochastic Resonance phenomenon\[15\] or the Dithering
effect\[16\]. To compute the time evolution of the error
probability \( P_{1s} \) for the sub-threshold case we can pro-
cceed as we did before for the analogous quantity \( P_1 \).
We obtain:
\[
P_{1s}(t) = P_{1sa}P_{1sb} = \Phi_{bc} e^{-\frac{t}{T_{1s}}},
\]
(9)
The main difference being that in this case \( b_u - i_{us} = b_c > 0 \). Moreover, while \( T_1 \) is a monotonic growing function of \( \sigma, T_{1s} \), the MFPT for this process, is a monotonic
decreasing function of \( \sigma \) and \( T_{1s} > T_1 \) for any value of \( \sigma \)[18]. The derivation of the bit-flip error probability \( P_{2s} \)
is made according to the derivation of \( P_2 \) for the supra-
threshold case. In Fig. 3 the error probabilities for the
two scenarios (supra- and sub-threshold) are compared.
Noticeably, for a given acceptable error probability the
following relation holds for the two corresponding idle in-
terval: \( t_w < t_{ws} < t_{hs} < t_h \). However, in the large noise
intensity limit \( \sigma \gg |b_u| \), \( t_w \) and \( t_{ws} \) admit the same
limit and the idle time difference between the two cases
becomes negligible.

In conclusion we have shown that the presence of noise
of intensity comparable with the difference between the
input signal amplitude and the threshold value can seri-
ously limit the computing speed of standard logic gates.
More specifically, we have demonstrated that computa-
tion in threshold based devices (e.g. transistor based
logic gates) can still be performed provided that the sys-
tem clock is operated accordingly to the existence of a
proper idle time interval that is a function of the noise
properties. Finally we have shown that in the large noise
scenario, the computing device can be operated also with
an energy saving sub-threshold signal. We anticipate
this result to be potentially relevant toward the design of
nano-scale computers where thermal and ambient noises,
instead of being a mere source of disturbances could be
useful components of the computing process. The author
gratefully acknowledge financial support from Ministero
Italiana della Ricerca Scientifica (PRIN 2004) and Eu-
ropean Commission (FPVI, STREP Contract N. 034236
SUBTLE: Sub KT Low Energy Transistors and Sensors).
The author also thanks the Office of Naval Research for
support during the initial phase of this research.

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