Retraction

Retraction: Analytical Modeling and Performance Analysis of Surface Potential for Junctionless MOSFET (J. Phys.: Conf. Ser. 1916 012026)

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IOP Publishing regrets that our usual quality checks did not identify these issues before publication, and have since put additional measures in place to try to prevent these issues from reoccurring. IOP Publishing wishes to credit anonymous whistleblowers and the Problematic Paper Screener [1] for bringing some of the above issues to our attention, prompting us to investigate further.

[1] Cabanac G, Labbé C and Magazinov A 2021 arXiv:2107.06751v1

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Analytical Modeling and Performance Analysis of Surface Potential for Junctionless MOSFET

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Abstract. The advancement in semiconductor technology requires small devices with low power consumption. This paper presents an analytical modeling of surface potential for junctionless MOSFET. Parabolic approximation is utilized to find out the surface potential. The effect of device parameter variation on surface potential and electric field has been studied. The variation in gate work function has been investigated for surface potential. Moreover, the consequence of variations in device parameters like drain bias, gate length ratio, radius of silicon pillar and doping concentration are also inspected. It is found that present device shows an excellent behaviour for future VLSI chips. The analytical results are matched with the TCAD results which validates the model.

Keywords: Surface Potential, Threshold Voltage, Junctionless MOSFET, SCEs, Gate engineering.

1. Introduction

The CMOS is the predominant technology of choice for industry. The demand of portable, mobile phones and handheld devices have been increased drastically. Battery lifetime becomes very important factor which differentiate between present technology. People required small dimension and low power consuming devices which puts pressure on device engineer to innovate new devices that fulfill the requirement. The present devices reach their scalable limit. So, Junctionless MOSFET can be scaled aggressively to achieve low power.

The device physical properties are more understandable by using the analytical models because it provides physical insight into the device. It seems that analytical models are more exact. The very common technique to find out the surface potential ($\Psi_S$) and its relationship with gate voltage ($V_G$) is the use of Poisson’s Equation with appropriate assumptions and boundary conditions [1]. The surface potential model further can be used to find the threshold voltage. The threshold voltage is the gate voltage at which the carrier density of inversion layer is equal to the bulk carrier concentration [2].
2. Analytical Model

Figure 1 depicts the double gate Junctionless Transistor (JLFET). The modelling of the surface potential for DG-JLFETs is carried out. In the above modelling, the impression of drain voltage on surface potential is unkempt. The above modelling holds true only for the long-channel JLFETs. However, the separation between source/channel interfaces to drain is very small. Hence, the electrical field interacts with the surface potential. This interaction disturbs the surface potential at source/channel interface and caused DIBL [3]. Hence, the modelling for short channel JLFETs must take SCEs into consideration. The quasi-2D scaling equation is used to obtain the simple second-order differential equation from the 2D Poisson’s Equation. The 2D Poisson’s Equation for MOSFETs in the sub-threshold regime may be written as by ignoring the mobile carriers in total charge density.

\[
\frac{\partial^2 \Psi(x, y)}{\partial x^2} + \frac{\partial^2 \Psi(x, y)}{\partial y^2} = \frac{qN_A}{\epsilon_{Si}} \quad (1)
\]

The parabolic potential approximation is taken in x-direction [4].

\[
\Psi(x, y) = \alpha_0(y) + \alpha_1(y)x + \alpha_2(y)x^2 \quad (2)
\]

Similarly using boundary condition, we have equation (2) as

\[
\Psi(x, y) = \alpha_0(y) + \alpha_2(y)x^2 \quad (3)
\]

The value of \(\alpha_2\) can be found assuming continuity of electric displacement vector

\[
-C_{\text{oxide}}(V_G - V_F - \Psi_{\text{Si}}) = -\epsilon_{\text{Si}} \frac{d\Psi}{dx} = -\epsilon_{\text{Si}} \alpha_2(y) \quad (4)
\]

Equation (3) modified by putting the value of \(\alpha_2\).

\[
\Psi(x, y) = \Psi_0(y) + \frac{C_{\text{oxide}}}{\epsilon_{\text{Si}}} (V_G - V_F - \Psi_S(y)) y^2 \quad (5)
\]

The relation among the central and the surface potential can be represented as

\[
\Psi_{\text{Si}}(y) = \Psi_S(y) = \Psi_0(y) + \frac{C_{\text{oxide}}}{4\epsilon_{\text{Si}}} (V_G - V_F - \Psi_S(y)) \quad (6)
\]

The surface potential can be written as

\[
\Psi_S(y) = \frac{\Psi_0(y) + \frac{C_{\text{oxide}}}{4\epsilon_{\text{Si}}} (V_G - V_F)}{1 + \frac{C_{\text{oxide}}}{4\epsilon_{\text{Si}}} y^2} \quad (7)
\]

Utilizing equation (7) to solve equation (1), the central potential is given as

\[
\frac{\partial^2 \Psi_S(y)}{\partial y^2} = \frac{4C_{\text{oxide}}}{\epsilon_{\text{Si}}} (\Psi_S(y) - V_G - V_F + \frac{qN_A}{4C_{\text{oxide}}} ) = 0 \quad (8)
\]
The equation (8) can be simplified by considering $1/L^2 = 4C_{oxide}/\epsilon_{Si}\cdot t_{Si}$, $\xi_S = VG - \gamma_1$ and $\gamma_1 = V_f - (qN_{AtSi})/4C_{oxide}$. Here $L_1$ is the natural length. $\xi_S$ is long channel surface potential. The above equation can be written as

$$\frac{d^2\Psi_S(y)}{dy^2} - \frac{1}{L_1^2}(\Psi_S(y) - \xi_S) = 0$$

(9)

The solution of the differential equation is

$$\Psi_S(y) = \xi_S + a_1 e^{\frac{y}{L_1}} + a_2 e^{-\frac{y}{L_1}}$$

(10)

As observed from the equation (10), $L_1$ represents the extension of potential profile and is proportional to the thickness of gate oxide and the channel thickness [5-6]. The natural length also describes the impact of the drain electric field on channel. For the better suppression of SCEs, the gate length should be more than its natural length.

3. Results & Discussion

The device features like surface potential and electric field have been analysed by varying the device parameters like channel doping concentration, oxide thickness, drain bias, silicon thickness and work-function of gate for the Junctionless Field Effect Transistor having HfO$_2$ as gate dielectric.

3.1 Surface Potential

The electrostatic potential developed due to the presence of surface-confined charges is known as surface potential. The surface potential profile for JLTFET devices is numerically simulated using Atlas Device Simulator. These simulated surface potential profiles were compared with surface potential profile developed from the analytical models. The following section discusses the variation in surface potential profile with various parameters.

3.1.1 Oxide thickness variation

The mutation in surface potential for various oxide thicknesses corresponding to channel length is shown in Figure 2.

![Figure 2: Mutation in surface potential for various oxide thicknesses](image)

The numerous values of surface potential are simulated and plotted at the oxide thickness of 2 nm, 3 nm, and 5 nm. The data is in close agreement with the analytical results. As depicted in Fig. 2, the surface
potential abates with reduction in the gate oxide thickness. This reduction in surface potential causes the reduction in DIBL due to the better electrostatic control of the gate for a thin gate dielectric. Hence, it results in suppression of Short Channel Effects (SCEs).

### 3.1.2 Silicon channel thickness variation

The mutation in surface potential for various channel thickness corresponding to channel length is shown in Fig. 3. The various values of surface potential are simulated and plotted at the oxide thickness of 5nm, 8nm and 10 nm. The simulated value is well correlated with the analytical results.

It can be seen from the Figure 3 as the thickness of the silicon channel increases, the surface potential decrease. It is due to the better control on the thin channel by the gate.

![Figure 3: Mutation in surface potential for various silicon channel thicknesses](fig3)

### 3.1.3 Variation of drain to source bias

The mutation in surface potential for various drain to source bias corresponding to channel length is shown in Figure 4.

![Figure 4: Mutation in surface potential for various drain to source bias](fig4)
The numerous values of surface potential are simulated and plotted at the drain to source bias value of 0.1V, 0.5V and 1.0V. The simulated value is well matched with the analytical results. The metal gate having high work-function minimizes the effects of drain to source bias variation. As can be seen from Fig. 4 the effects of bias variation are prominent on the drain side and almost the same surface potential profile exists towards the source side.

### 3.1.4 Variation in Channel doping

![Figure 5: Mutation in surface potential for various channel doping](image)

The mutation in surface potential for various channel doping corresponding to channel length is shown in Figure 5. The numerous values of surface potential are simulated and plotted for different channel doping value of 1e-19 cm\(^{-3}\), 1.25e-19 cm\(^{-3}\) and 1.5e-19 cm\(^{-3}\). As reveals from Fig. 5, the simulated value is in good paired with the analytical results. It can also be scrutinized that with the decrease in doping concentration the value of surface potential decreases as the lower doping concentration results in the efficient depletion of the channel and effective suppression of the SCEs [7].

### 3.1.5 Variation in gate work-function

![Figure 6: Mutation in surface potential for various gate work-function](image)
The mutation in surface potential for various gate work-function corresponding to channel length is shown in Figure 6. The numerous values of surface potential are simulated and plotted for dissimilar gate work-function of 5.1eV, 5.2eV and 5.3eV. As can be seen from Fig. 6, the enhancement in work-function of gate yields the better gate control and efficient depletion of the channel is achieved.

3.2 Electric Field Distribution

The electric field for JLT having HfO$_2$ as a dielectric is determined and analysed for various parameters. The electric field profiles are numerically simulated using Atlas Device Simulator. These simulated electric field profiles were compared with electric field profile developed from the analytical models. The following section discusses the variation in electric field profile with various parameters.

3.2.1 Oxide thickness variation

![Figure 7: Mutation in electric field for various silicon oxide thickness](image)

The mutation in electric field for various oxide thicknesses corresponding to channel length is shown in Figure 7. The numerous values of the electric field are simulated and plotted at the oxide thickness of 2 nm, 3 nm, and 5 nm. The simulated data is well matched with the analytical results. It can be securitized from Fig. 7 that the lower values of oxide thickness yield the uppermost peak of electric field. The average electric field enhances with reduced oxide thickness.

3.2.2 Silicon channel thickness variation
The mutation in electric field for various channel thickness corresponding to channel length is shown in Figure 8. The numerous values of electric field are simulated and plotted at the oxide thickness of 5nm, 8nm and 10 nm. The simulated data is found in good agreement with the analytical results [8]. It can be seen from Fig. 8 that gain in electric field is observed with mitigation in channel thickness. It indicates the reduction in the value of DIBL and SCEs.

3.2.3 Variation of drain to source bias

The mutation in electric field for various drain to source bias corresponding to channel length is shown in Fig. 9. The electric field is simulated and plotted at the drain to source bias value of 0.1V, 0.5V and 1.0V. The simulated value is well correlated with the analytical results.

It can be seen from Figure 9 the peak of the electric field is located inside drain, which minimizes the chances of electrons to go into the oxide layer and acts as hot electron. Hence overall reduction in the effect of the hot electron is observed in JLTs. It can also be seen that the value of the electric field is less for V=0.1 V and V=1V but the highest for V=0.5 V, this is due to the existence of drain voltage stress-induced degradation at lower voltage in JLTs and higher impact ionization rate at high drain bias.

Figure 8: Mutation in electric field for various silicon channel thickness

Figure 9: Mutation in electric field for various drain to source bias
3.2.4 Variation in Channel doping

The mutation in electric field for various channel doping corresponding to channel length is shown in Fig. 10. The field is simulated and plotted for dissimilar channel doping value of 1e-19 cm⁻³, 1.25e-19 cm⁻³ and 1.5e-19 cm⁻³. As can be seen from Figure 10, the simulated value is in good agreement with the analytical results. The lower doping concentration in channel suggests efficient depletion in the channel during off state. The reduction in the electric field due to reduction in channel doping can be interpreted as reduction in HCEs.

![Figure 10: Mutation in electric field for various channel doping](image)

3.2.5 Variation in gate work-function

The deviation in the electric field along the channel length for different value of gate work-function is shown in Figure 11. The electric field is simulated and plotted for different gate work-function values of 5.1eV, 5.2eV and 5.3eV. As can be seen from Fig. 11, there is not much significant difference in electric field due to the variation of the work-function. It shows that electric field is almost independent of the work function of the gate.

![Figure 11: Mutation in electric field for various gate work-function](image)
4. Conclusion

This paper presents the basics of junctionless transistor and various parameters which affects its performance. The analytical modeling for surface potential has been developed by using parabolic approximation. Finally, the variation of surface potential profile and electric field with different parameters is carried out using Atlas and the results were also validated by analytical modeling. The surface potential mitigates with the reduction in the thickness of gate oxide whereas field enhances with gate oxide. As the thickness of the silicon channel increases the surface potential decrease. It further noticed that SCEs behavior of the device improves with varying device parameters. So, JLFET is a potential candidate for future VLSI circuits.

References

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