**MUSE: Multi-Use Error Correcting Codes**

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**ABSTRACT**

In this work we present a new set of error correcting codes – Multi-Use Error Correcting Codes (MUSE ECC) – that have the ability to match reliability guarantees of all commodity, conventional state-of-the-art ECC with fewer bits of storage. MUSE ECC derives its power by building on arithmetic coding methods (first used in an experimental system in 1960s). We show that our MUSE construction can be used as a “drop in” replacement within error correction frameworks used widely today. Further, we show how MUSE is a promising fit for emerging technologies such as a DDR5 memories. Concretely, all instantiations of MUSE we show in this paper offer 100% Single Error Correction, and multi-bit error detection between 70% and 95% while using fewer check bits. MUSE ECC corrects failure of a single chip on a DIMM with check bit space savings of 12.5% compared to conventional techniques. The performance overheads, if any, are negligible. Our results open the possibility of reusing ECC storage for things beyond reliability without compromising reliability, thus solving a 40-year-old puzzle.

**1. INTRODUCTION**

Error Correcting Codes (ECCs) are a standard technique for improving system reliability and are widely used today. ECCs improve reliability by encoding data in a redundant format that uses additional bits of information to identify, and correct, data bits that change value while in storage or transit. To minimize storage and transmission overheads, codes that use fewer redundancy bits for a desired level of reliability and are easy to implement have gained widespread use.

In 1983, Gumpertz observed that in some cases, it is possible to encode not only the data but also the metadata about the data in the same number of ECC bits without actually storing the metadata [17]. However, Gumpertz’s ECC scheme does not offer this property in the general case for any data type, and thus a 40-year puzzle was born: Can we store metadata and data in ECC bits without compromising on ECC’s ability to detect and correct errors on both the data and the metadata, and without any restrictions on the type of data that is stored in ECC?

In this work, we solve this puzzle with MUSE ECC. MUSE ECC is a novel ECC code that allows metadata to be stored along with the data, but without compromising reliability guarantees of the ECC. These benefits come from two pieces: first, MUSE ECC has a higher rate for the same reliability, i.e., uses fewer bits, and these saved bits can be used for storing metadata in a manner that also protects the reliability of the metadata. Second, we show how space can be harvested from the code by taking advantage of the linear and explainable relationship between the data and codeword that allows additional data to be stored in the codeword.

MUSE ECC revisits ECC techniques used in experimental systems more than half a century ago but were never adopted in mainstream systems [4, 12, 18, 47]. Though it is hard to say why such techniques were not further pursued, it is likely that the limited hardware budgets of the time (pre-Moore’s-Law and pre-DRAM era), and some limitations of the older code constructions, made alternate lightweight codes such as Hamming and Hsiao codes more attractive to hardware designers of that era.

Unlike traditional error correction techniques used in modern processors such as Hamming, Hsiao, and Reed-Solomon (RS) codes that require a deep understanding of complex mathematics, our approach, in contrast, consists solely of the simple mathematical operations of division and multiplication and is easy to understand. We can break down our method into three steps: (1) multiplying data with a deliberately chosen multiplier before storing it into memory, (2) dividing values retrieved from memory by our multiplier, and (3) using the remainder to uniquely identify and repair any incorrect data bits. Since we multiply our data by a fixed multiplier, we expect the value retrieved from memory in step (2) to have a remainder of zero in the case that no bits were flipped. If some bits were flipped, we could use the value of the remainder to identify those flipped bits and restore their original value.

To derive the relationship between remainders and bit flips we need to have an one-to-one mapping between the remainders and the position of the bits to be flipped. Conceptually, we achieve this as follows: we assign each bit a specific, unique integer value, typically $\pm 2^i$ where $i$ is the position of the bit and the $\pm$ is determined based on the direction of the bit flip, viz., $1 \rightarrow 0$ or $0 \rightarrow 1$, such that once that bit is flipped, the encoded (multiplied) data value in memory is changed by this specific integer value. When the data is retrieved and divided by the multiplier, it will have a remainder that is related to the value assigned to the integer: for single bit errors, the remainder will be exactly the integer the corresponds to the flipped bit, and for multiple bit flips, i.e., multi-bit error, the remainder will be equal to the sum of integer values of each flipped bit.
How do we choose a multiplier? First, we need to identify the error model that we wish to support, e.g., single bit, multi-bit adjacent, multi-bit disjoint, unidirectional errors etc. Then, we enumerate all possible error patterns in that model, and then search for a multiplier that leaves a unique remainder for each error pattern when it is applied to any codeword. A good multiplier is the smallest integer number that satisfies the unique remainder property, as a smaller number corresponds to fewer redundancy bits. While prior works from the 1960s, hereafter referred to as AN codes \(^1\) were able to identify these remainders for single-bit errors, there were significant challenges in scaling to multi-bit errors.

The difficulty for scaling to multi-bit errors is that the required number of remainders grows exponentially with the number of errors, and multiplier values become too large for practical use. To overcome this problem, we invent a new optimization we call shuffling. Shuffling changes bit positions of the multiplied data before the data is written to memory. The goal of shuffling is to take advantage of the error model such that errors that need not be handled end up having non-unique remainders. Because the remainders are directly related to the integer values of the errors, by changing the order of the bits, we can increase the chances of finding a multiplier.

In terms of implementation, even though multiplication and division are typically expensive operations, we do not need to use general multipliers and dividers since we know the MUSE code multiplier is constant. Additionally, we leverage algorithmic optimizations and careful encoder/decoder design and show that these operations are not on the critical path.

Our experiments show the following:

- **MUSE ECC** matches the reliability of the state of the art ECC schemes for single-bit error correction and multi-bit error detection. For example, unlike Hamming code with its average multi-bit error detection rate of \((71.66 \pm 29.4)\%\), MUSE ECC uniformly detects \((70.85 \pm 0.5)\%\) of multi-bit errors.

- **MUSE ECC** successfully corrects multi-bit errors confined to a single DDR5 or DDR4 x4 device on a memory module. MUSE ECC achieves this level of reliability with at least five fewer bits of redundancy compared to Reed-Solomon codes. Moreover, we show that under the unidirectional error model, MUSE ECC can to correct single device errors for x8 DRAM DIMMs as well while using three fewer bits of storage.

- **MUSE ECC** not only matches multi-bit error detection and correction capabilities of state of the art ECC schemes but also achieves this goal while using a smaller amount of the redundancy bits. Alternately the codes can encode more data for a given amount of redundancy bits.

- Through circuit implementations and simulations we evaluate the performance overheads of MUSE ECC and observe that they are negligible. Finally, the higher area overheads in our scheme are insignificant in modern designs with billions of transistors on chip.

The rest of the paper is organized as follows: Section 2 describes how to construct MUSE ECC codes as well as the optimizations that make it practical. Section 3 presents some practical codes. We describe a microarchitectural implementation of MUSE ECC in Section 4. Section 5 highlights and explains the advantages of MUSE ECC over existing ECCs. In Section 6 we evaluate the performance of MUSE ECC compared to Hamming, Hsiao, and RS codes. We discuss related work in Section 7 and then conclude in Section 8.

2. **MUSE ECC**

There are three steps in the construction of MUSE code: (1) group bits into symbols, and order bits within and across groups (2) compute the error values for each possible error in all of the symbols in the word, and (3) compute the remainders for all error values from step (2) given some multiplier \(m\). If all the remainders are distinct, i.e., we have a bijective mapping between remainders and errors, \(m\) would define a code. As the multiplier value is known, the overheads of the code is \(r_b = \log_2 m\). For instance, with the \(k\)-bits data words, the codeword length is \(n = r_b + k\). We denote this code as MUSE(n,k).

The following equations describe how the data integer data is encoded into a codeword integer codeword, decoded, and how the errors are detected and corrected:

\[
\text{codeword} = m \times \text{data} \tag{1}
\]

\[
\text{remainder} = \text{codeword} \mod m \tag{2}
\]

\[
\text{data} = \begin{cases} 
\frac{\text{codeword}}{m} & \text{remainder} = 0 \\
\frac{\text{codeword} - \text{error(remainder)}}{m} & \text{otherwise}
\end{cases} \tag{3}
\]

The data is encoded to codeword by multiplying data by \(m\) (Eq. 1). Upon reading the codeword, we check the remainder of codeword divided by \(m\) (Eq. 2). When the remainder is zero, we can recover the original data simply dividing the codeword by \(m\) (error-free case); otherwise we subtract the error value derived from remainder \(r\) to correct the codeword and then recover the data by dividing by \(m\) (Eq.3). For this scheme to work we pick \(m\) so that each remainder corresponds to one error only, allowing for unambiguous error correction.

So, how does one use integer values of remainders to detect and fix bit flips in memory? We explain this next. However, before that we will present another important optimization in terms of code construction.

**A Systematic MUSE Code.** The MUSE ECC method outlined in Eq. 3 creates a situation where the original data is available only after the division is done. In the common case of no errors this is far from desirable as this will add latency of memory loads. However, by using the scheme developed by Chien [12], MUSE ECC can be constructed such that the data and the error correction bits can be stored separately (in a “systematic” manner). Eq. 4 depicts the approach, where \(r_b\) being number of bits for redundancy, data is the integer value of the data bits, and \(X\) is picked in such a way so that \(\text{codeword} \mod m = 0\).
\[ \text{codeword} = \text{data} \times 2^s + X \]
\[ X = m - \text{data} \times 2^n \mod m \]  

This way the data in the codeword is separated from the redundancy (i.e. \( X \)) and the expensive integer division is not required to recover the data upon reading from memory. Although it seems that systematic form is superior and no one should be bothered with the non-systematic codes, in Section 5 we show that non-systematic form has its benefits and is useful.

2.1 Mapping Remainders to Bit Positions

1-bit Error Remainders When a memory error flips bits, it transforms codeword to be some other codeword. The difference between these two codewords is what we refer to as the error value, and each bit flip has two error values: one for \( 0 \rightarrow 1 \) bit flips, and the other for \( 1 \rightarrow 0 \) bit flips.

As illustration, let us look into two examples. Say, the integer value 243 is the codeword. The binary representation is: 1111 0011. Now assume that bit #1 (the bolded bit) is flipped and the value of the codeword is changed to 1111 0001 or 241, leading to error value of \(-2\). As a second example, say the codeword is 972 or 0111 1100 1100. If the same bit #1 was flipped \( 0 \rightarrow 1 \), corrupting the codeword to 0111 1101 1100 = 974, the value of error would be \(+2\). So, we see that flip of the same bit has different error values, and the value itself depends on the direction of the bit flip. Thus, for every bit in the word we would need two remainders, so that we can identify the corrupted bit and correct its value.

Moreover, both of those error values are integers powers-of-two: \(-2 = -1 \times 2^1\) and \(2 = 1 \times 2^1\). The main takeaway is that, error at bit \(i\) has error values of \(\pm 2^i\), where \(+\) for bit error \(0 \rightarrow 1\), and \(-\) for the error \(1 \rightarrow 0\).

N-bit Error Remainders We saw that single bit error manifests itself in two different error values, but what happens to multi-bit errors? In the case on \(n\)-bit errors (where \(n\) bits of the data are corrupted), the error is just a combination of individual bit flips, or more formally:

\[ E = E_i + E_j + \ldots + E_k, \quad 0 \leq i \neq j \neq \ldots \neq k \leq n \]

In this formula, \(E_i, E_j, \ldots\) are individual bit flips with values \(\pm 2^i\), where \(i\) is the position of the erroneous bit in the word, and the sign is determined by the direction of the flip.

Let us look at an example: Consider, 243 = 0...01111001112. Consider what happens when bits #4, #2, and #1 are flipped, and the codeword becomes 0...01110011012 = 229. For this bit corruption pattern the error value is \(-14\):

\[ E = E_4 + E_2 + E_1 = -2^4 + 2^2 - 2^1 = -14 \]

In general, in the \(n\)-bit word each bit may undergo one of the two bit flips or stay the same, hence there are \(3^n - 1\) possible error values:

\[ E_b = \sum_{i=0}^{i=n-1} p(i) \times 2^i \]

\[ p(i) \in \{-1, 0, 1\} \] and determines both whether bit \(i\) was corrupted as well as the direction of the flip.

Contiguous Errors. Let’s look into \(n\)-bit errors which are confined within a byte. We are interested in this specific class of errors because codewords are stored in memory across multiple DRAM chips on a DIMM, and if one of the chips is faulty the errors are localized to the corresponding part of the codeword. To aid us clearly talk about DRAM device failures, we define a notion of symbols which are groups of \(s\) bits such that every bit is assigned into one symbol only. Note, that these symbols may or may not be formed in a contiguous manner, however, once formed the bits within a symbol are placed contiguously in a DRAM.

With this construction, every symbol will be written to a specific DRAM chip on a DIMM, and every symbol will correspond to a failing DRAM device. For example, if the DIMM has \(x4\) DRAM chips (i.e., each chip provides 4 bits per transaction), the codeword will be partitioned to a sequence of symbols \(S_{-1}, S_{-2}, \ldots, S_0\) of length 4 bits each. We can treat symbols as short words of \(s\) bits, thus each symbol may have one of \(2^s - 1\) values. The total number of possible errors is \(2 \times (2^s - 1)\) as the number of possible transitions from one \(s\)-bit value to another (we discuss alternatives in Section 2.2).

Unidirectional Errors. Let us consider an additional class of errors – unidirectional errors. Under the model of unidirectional errors only one type of erroneous transition is possible in the device: \(0 \rightarrow 1\) or \(1 \rightarrow 0\). Unidirectional errors may be useful especially if failing memory devices have a tendency to get disconnected and thus turn values towards one direction. Without loss of generality, let us assume \(0 \rightarrow 1\) errors only. Thus, error value of a single bit error must be a positive integer. Similar to symbol errors, unidirectional symbol error has error value as a combination of positive error values of individual bit flips within the symbol. This assumption cuts down the number of remainders by one half increasing the chances of finding a bijective mapping between errors and remainders.

2.2 Codeword Shuffling

Sometimes we find that certain multi-bit errors leave the same remainder values for all possible multipliers. When multiple errors end up having the same remainder these errors become indistinguishable. What we discovered is that by changing the assignment of bits into symbols the error value of a multi-bit error can be changed, leading to fewer remainder collisions among different error patterns. This allows us to evaluate each possible multiplier with various assignments of bits into symbols, until a multiplier and a bit assignment (aka shuffle) produces a distinct remainder for each error value.

The process of shuffling bits between the symbols leads to fewer remainders because \(\mod m\) is a periodic function, i.e. consecutive integer ranges \([0 : m-1]\), \([m : 2m-1]\), ... map to the same interval \([0, m-1]\). Thus, when searching for a multiplier \(m\) we would want to make sure that computed error values are packed as densely as possible to decrease the chance of two different errors having identical remainders. For example, integers 10 and 11 are less likely to have identical remainders than 10 and 10000.

To see the benefits let us consider a toy example of the first two symbols of size, \(s\), such that \(s = 2\) in a codeword...
illustrated in Figure 1(a). We use Eq. 5 with the sequential assignment to get the following error values for symbols $S_0(0,1)$ (red color) and $S_1(2,3)$ (blue color):

$$S_0(0,1): \text{Error values} = \{1, 2, 3, -1, -2, -3\}$$

$$S_1(2,3): \text{Error values} = \{4, 8, 12, -4, -8, -12\}$$

Now let us change the assignment by putting bit #1 into $S_1$, and bit #3 into $S_0$ resulting in symbol $S'_0$ with bits (0,3) and symbol $S'_1$ with bits (2,1). The error values for these new symbols are:

$$S'_0(0,3): \text{Error values} = \{1, 8, 9, -1, -8, -9\}$$

$$S'_1(2,1): \text{Error values} = \{4, 2, 6, -4, -2, -6\}$$

What we notice is that (1) the overall numerical range of error values for both symbols decreased from 1 to 12, to 1 to 9, and (2) the density of error values increases. Moreover, with the sequential assignment of bits, the error values of the symbols never overlap, i.e., they increase as a monotonic sequence of non-overlapping ranges. For example, before we reassigned the bits error values of $S_0$ were confined to 1 to 3, while error values of $S_1$ were in the range 4 to 12. However, symbols $S'_0$ and $S'_1$ have numerical range of 2 to 6 in common.

Figure 1(b) shows an interface routing between DRAM and memory controller to support the shuffling of the bits. Since the multiplier value is paired with a specific bit assignment, both are static properties of the code.

2.3 Code Search

Algorithm 1 is a pseudocode implementation for finding a suitable multiplier. The inputs to the algorithm are the code length $n$, the symbol size $s$, and the redundancy budget $r_b$. The procedure starts (line 1) by assigning codeword bits to symbols, initializing an empty set of valid multipliers $muls$ (line 2) and precomputing a required number of reminders for the code (line 3). Then via a for loop we iterate over all possible odd multiplier values (line 4) one by one. For each multiplier $m$ we iterate over the symbols of the codeword (line 6) and compute all the remainders for all the error values in this symbol (lines 7-9). For each $errPattern$ in the symbol $S_i$ the $getErrVals()$ function (lines 14-19) is called. The computed remainders are inserted into a remainder set (line 9) which is initialized (line 5) for every new multiplier we try. We compare the size of remainders set to the required number $R$ (line 10), if they match we put multiplier $m$ into a list of valid multipliers for the code (line 11). We repeat this procedure until we exhaustively checked every multiplier that fits the redundancy budget $r_b$.

3. PRACTICAL CODE EXAMPLES

In this section we describe four $\text{MUSE}$ codes to satisfy different error and system models to showcase the flexibility and applicability of our code in practical modern contexts. We summarize code parameters such as multipliers and bit assignments in Table 1.

MUSE ECC(72,64) SEC Code. Multiplier $m = 243$ defines a SEC $\text{MUSE}(72,64)$ code. This code can be used for DRAM in settings where low-level reliability is sufficient (i.e. not Chipkill) or for on-die caches where SEC-DED codes are commonly used to allow power savings of memory subsystem [38, 41, 51]. This code has perfect single error correction ability, and has double error detection rate of 77.88%.

MUSE ECC(144,133) Single Symbol Correct (SSC) Systematic Code. While DDR5 standard has been finalized and devices are being sampled, it is likely that older DDR4 standard devices will continue to be utilized for at least a few more years. So, we show how $\text{MUSE}$ can be used to provide ECC for DDR4 DIMMs. For this class of devices, for server and enterprise settings, a specific type of capability known as “Chipkill” is desired. Informally, ChipKill allows operation even when one or more of the DRAM chips completely fails on a DIMM.

Here we show how $\text{MUSE}$ can be used to design codes that can handle device failures. In constructing these codes, rather than designing for device failures, we design for handling symbol failures, as symbols are at least as large as DRAM devices, and usually a small multiple of the smallest device size.

Typically, to achieve Single Symbol Correction (SSC), the DIMM is constructed out of x4 devices and 288 bits of data (256 bits of data, and 32 bits of redundancy) are stored eighteen x4 devices and accessed in four bursts over 72 bit channel (72 bits because that is channel width as specified by the DDR4 standard). The minimum granularity of access is 32 bytes, which is typically one-half of a cache line. In this mode of operation, there are no spare bits. Intel refers to this capability/configuration as Single Device Data Correction (SDDC) [40]. Depending on the configuration, the system may switch to a “lockstep” or striped mode after failure, or continue working in lockstep before and after failure [49].

To be able to correct single device failure with x4 devices, we use the MUSE (144,133) with $m = 2005$ with x4 symbol sizes. In our scheme, the data is striped across two DIMMs each having eighteen x4 devices. The data is received from these two DIMMs across eight bursts over an 144 bit channel, or sixteen bursts (eight form each DIMM) over a 72 bit channel depending on the design. Under these conditions, $\text{MUSE}$ code requires only eleven bits of redundancy for 133 bits of data. In other words, our code yields five spare bits.

MUSE ECC(80,70) Single Symbol Systematic Code. Recently published DDR5 standard [26] doubles the number of channels per DIMM, requiring two 40-bit memory channels per DIMM (32-bit data + 8-bit parity) [1]. As of this writing,
there are no commercially available DDR5 ECC DIMMs, and as such it is not clear how exactly the DIMMs will be configured. It is possible that they could be made of ten \( x \times 4 \) devices per channel, for a total of 20 devices per DIMM; or five \( x \times 8 \) devices per channel, for a total of 10 devices per DIMM.

Like in DDR4, we can design a 4-bit symbol (80,70) code to where the data is striped across two channels within a DIMM. Unlike DDR4 where the data needs to be fetched from two different DIMMs, here the data comes from the same DIMM but across two channels. MUSE(80,70) code encodes 70-bit data into 80-bit codewords. With this code, we can correct failure of one device on a DIMM with six bits to spare; and we can correct failure of two devices with two bits to spare. If a DIMM is to be constructed out of \( x \times 8 \) devices, then we need to work with 8-bit or 16-bit symbols in this model. We leave creation of these codes for future work once DDR5 DIMM architectures become better known but show a \( x \times 8 \) example next. A traditional RS(80,64) code with \( x \times 8 \) symbols or a RS(40,32) with \( x \times 4 \) symbols do not have any symbol code with DDR5. For this code, the regular MUSE construction with sequential assignment of bits to symbols yields no multipliers less than 16 bits. Thus, we shuffle the

|  |  |
|---|---|
| \( S \) | \( \) |
| \( m \) | \( \) |
| \( \) | \( \) |

Algorithm 1: Code Multiplier Search

```
input : \( r \) redundancy bits, \( s \) byte size, \( n \) code length
output : List of multipliers \( m \)
1 \( S \leftarrow \) assignBitsToSymbols\((s,n)\);
2 \( muls \leftarrow \) empty();
3 \( R \leftarrow \) remaindersNeeded\((s,n)\);
4 for \( m \in 2^n + 1 \) to \( 2^{s+1} - 1 \)
5 \( \) remSet \( \leftarrow \) empty();
6 for \( S \in \) S do
7 for \( errPattern \in 1 \) to \( 2^n - 1 \) do
8 \( \) for \( errVal \in \) getErrVals\((errPattern,S_i)\) do
9 \( \) remSet.insert\((errVal \mod m)\);
10 if \( \) remSet.size() == \( \) R then
11 \( \) muls.insert\((m)\);
12 Function remaindersNeeded\((s,n)\):
13 // \( \) \( s \times (2^n - 1) \) - with shuffling
14 return \( 2 \times \frac{s}{2^n - 1} \);
15 Function getErrVals\((errPattern,S_i)\):
16 locErrVals \( \leftarrow \) empty();
17 binPattern \( \leftarrow \) to_bin\((errPattern)\);
18 for \( vec \in \) genAllVectors\((binPattern)\) do
19 \( \) locErrVals.insert\((vec \cdot S_i)\); // \( a \cdot b - \) dot product
20 return locErrVals;
```

4. MUSE ECC MICROARCHITECTURE

In this section, we discuss the microarchitectural implementation of MUSE codes. We start with the system-level integration, discuss the design of the encoder and decoder blocks, and finish with lower-level building blocks and optimizations for fast multiplication and a fast modulo operations that are required to build efficient decoders and encoders.

System Overview. Figure 2 shows the high-level overview of how MUSE is integrated in a system and the parallelism among different operations. On the read path, once all of the codeword has been read from main memory, the decoder unit computes the remainder based on the multiplier. The remainder is then passed to the Error Lookup Table (ELT) to determine whether an error has occurred. If the ELT provides a value (\( \)error\( \)) to correct the data via addition for non-zero remainders. The corrected data is then supplied to LLC. On the write path to main memory, the data is read from the LLC, encoded and transmitted to the main memory.

Decoder. Figures 3(a) and (b) show the microarchitecture of the decoder non-systematic and systematic codes. Both decoders use a fast modulo computing circuit to compute the remainder of the incoming codeword. The non-systematic decoder divides the codeword by code multiplier \( m \) to recover the data using fast multiplier circuit. On the other hand, the systematic code decoder enjoys the separability of the data and does not incur any latency penalty for memory reads.

Encoder. The non-systematic encoder pictured in Figure 3(c) is much simpler than the decoder and based on a single fast multiplier. The encoded data is multiplied by code multiplier \( m \) and sent over the channel to DRAM. The systematic
encoder in 3(d) is a bit more complicated because it computes the value of \( X \) (see Eq. 4) to ensure that \( c \bmod m = 0 \).

To build the encoder, we used the fast modulo described in Section 4.1.

**Error Correction.** Since errors are very rare, the latency of error correction is not critical to performance. Thus, we implement an error correction circuit as a simple ROM table that maps an incoming remainder to an error value which is used to correct the error. For example, MUSE(144,133) code with \( m = 2005 \) error correction is built around a lookup table with 1080 entries and a full adder. Each table entry is 156 bits wide, where the first 11 bits store the value of the remainder, 144 bits store the value of the error, and remaining single control bit determines whether the error was a positive of a negative integer. The full adder should support both the addition and subtraction operations, and the type of the operation is determined by the control bit.

**Error Detection.** There are two ways to detect multi-bit errors with MUSE ECC. By design, the multiplier of the code is required to be larger than the number of single error remainders it generates. This leaves some remainder values unused, and those unused remainders can indicate a multi-bit error. This can be detected using the circuit designed for correcting multi-bit errors.

An additional way to detect multi-bit errors is to examine if the computed remainder can reliably point to an error. Say, a multi-bit error remainder indicates that a particular bit should be set to 1. However, if the actual value of a bit before the correction is 1, we can be assured that a multi-bit error had occurred. In other words, our MUSE codes by construction differentiate bit flip directions via unique remainders, and hence, when the error remainder is computed, the correct bit value is known. If the potentially erroneous bit value is equal to the value computed based on the remainder, we know that a multi-bit error is detected\(^2\).

To demonstrate this, let’s consider an example of MUSE(72,64) code with multiplier \( m = 243 \) and a codeword \( 1 \times 243 = 243 = 111100111 \). Consider a double error flipping the bits #4 and #3, then the corrupted codeword is 235 = 1110 1011, and the remainder is 235. However, the remainder of 235 corresponds to a single \( 1 \rightarrow 0 \) bit flip of the #3 bit: \(-2^3 \bmod 243 = 235\). By examining the current value of bit #2,\(^2\)

\(\text{Figure 2: View of the memory subsystem with integrated MUSE decoder.}\)

\(\text{Figure 3: (a) Decoder for the non systematic code features multiplication by inverse constant to compute the data in parallel to the computation of the remainder; the delay of the critical path is the delay of the multiplier. (b) The systematic code decoder has zero delay on the critical path due to the separation of the data and redundancy bits. The value of remainder is used by the error detection circuit, to determine whether the error had occurred, and if so, where. (c) the encoder for the non systematic code is made of one fast multiplier, (d) the encoder for the systematic encoding first computes the residue, and then attaches it to the raw data making a separable codeword.}\)

which is 1, and comparing it to the potential erroneous transition \( 1 \rightarrow 0 \) given by the computed remainder, we see a contradiction – it is impossible to flip the current bit value of 1 to be 1. Thus, we conclude that a multi-bit error should be reported.

### 4.1 Fast Arithmetic Blocks

MUSE ECC requires three arithmetic operations: integer division, multiplication, and modulo. For the non-systematic variant of the code, fast multiplication is required for the encoding, while fast modulo and division by constant are used for the decoding process. The systematic code’s decoding and encoding are done by computing the modulo. Table 3 summarizes these operations for each type of MUSE ECC.

**Division by Constant.** The non systematic decoder performs integer division for data recovery and modulo for error detection/correction. However, even the fastest high-performance processors perform integer division in about 13–44 clock cycles for AMD ZEN2 or 24–95 clock cycles in the case of the Intel Skylake-X [9].

Two observations enable us to substantially reduce decoder latencies:

1. A generic divider is not required: we always divide by a known constant multiplier of the code \( n \).

2. Using multiplication by the inverse instead of the division: a commonly used optimization technique in compilers [16,32].

As a result, we reduce the problem of designing a fast
Figure 4: (a) The microarchitecture of generic multiplier with Booth Encoding. Three main components are multiplier Booth Encoding, Wallace Tree to sum the partial products, and final adder stage. Booth Encoding reduces the number of partial products, allowing for a shallower Wallace tree. (b) Microarchitecture of a circuit for direct remainder computation. Both multipliers are custom multipliers from (a), implementing a scheme described by Lemire [32].

Table 2: Multipliers and their inverses for MUSE codes

| n  | Multiplier Code | Inverse Code |
|----|-----------------|--------------|
| 243| 9950006745799417075771|               |
| 2005| 113895077772217136207946421701342604759612941|               |
| 1005| 7698632085108862866861|               |
| 5621| 176187825188230243585305|               |

† shift right 81, × shift right 154, ◻ shift right 88, ◄ shift right 93 (see Section 4)

divider to a task of designing a fast multiplier by a constant.

Multiplication by Constant. Generic integer multiplication of 64b operands is done in 3–4 cycles in most modern CPUs [15]. However, because the codewords are at least 72b long, and decoding is on the critical path, we need a much faster multiplier. To achieve this goal, we devised a custom Wallace Tree [50] multiplier based on Radix-4 Booth Encoders [33]. Figure 4(a) shows the architecture of the multiplier with its three components: (1) Multiplier encoder with Radix-4 Booth Encoding (BE), which allows reducing the number of partial products by half and thus making the tree shallower, (2) Wallace tree that performs the summation of partial products, and (3) a final adder that produces the product. We optimized the depth of the adder even further by manually analyzing partial products. If some of the partial products are zero, we will remove those from the multiplier tree, further reducing the latency, hardware, and energy costs of the multiplier. For example, for the MUSE ECC(144,133) code, Booth Encoding of the inverse value has 74 partial products, 23 of which are equal to 0. By eliminating these, we reduce the depth of the Wallace tree by 1, thus reducing the latency by 4 XOR delays. Table 2 summarizes the multipliers, their inverses and shift amounts we used to implement the codes. The results section includes the actual measured latencies.

Modulo by Constant. The naive approach to compute \( c \mod m \) is as follows:

\[
r = c - m \times \lceil c/m \rceil
\]

where the last division can be substituted by fast multiplication with the inverse.

As a result, the latency of the modulo operation is the latency of two multiplications and one subtraction, which can be done in 7 cycles on a modern CPU [15]. However, the technique developed by Lemire et al. [32] allows computing the modulo even faster. The idea is based on using discarded bits from first multiplication by the inverse. The value, represented by these bits, is multiplied by the code multiplier \( m \) and thus is equal to the result of modulo.

Figure 4(b) shows a schematic of a circuit to compute modulo based on two consecutive multiplications. The second multiplier is much faster than the first one because it multiplies by \( m \), which is much smaller than the inverse constant of \( m \). Therefore, the resulting latency of a code modulo is much smaller than the latency required by chaining generic CPU operations.

Table 3: Basic arithmetic operations for systematic and non-systematic encoding and decoding processes.

| Process | Systematic Code | Non-Systematic Code |
|---------|-----------------|---------------------|
| decode | \( d = c >> r_b \) | \( d = \lfloor c/m \rfloor \) |
| r = c \mod m | \( r = c \mod m \) |
| encode | \( c = d << r_b - r \) | \( c = d \times m \) |

\( r_b \) is the bit budget for code redundancy, or \( r_b = \lceil \log_2 m \rceil \)

5. MUSE USE CASES

In this section, we discuss how space gained with MUSE code can be used for other storing metadata.

Exploiting Unused States Let us start with an obvious case. Consider a MUSE(80, 70) code with a multiplier \( m = 1005 \) that can be encoded in 10 bits, thus giving us 6 bits of harvestable space that one can use for any task. In other words, with a 80-bit codeword, we can store up to 70 bits of data to achieve chipkill-like functionality, but since the basic granule of protection is 64 bits (8 bytes) in most existing schemes, we get to store six additional bits of free storage. This storage can be put to a number of uses; the ARM Memory Tagging Extensions (v8.5A ARM ISA), requires the ability to store 4 bits of metadata for each 16-byte granule. Currently, there are two methods to store this data: 1) store the metadata in another part of memory and include tag caches to avoid two DRAM access per access, or 2) store the metadata in the ECC at the expense of reliability. If MUSE is used on a system with MTE, the four additional bits can be stored inline for each 16-byte granule leaving a full byte to store additional information. This also creates a pathway for increasing the tag sizes if desired in future architectures. Similarly, the additional storage can be used to store authentication information, or replay counters to mitigate the overhead of memory authentication and encryption techniques.

Fractional Space Harvesting Since MUSE ECC is based on integer arithmetic, the reasoning about code space bounds and unused code states is extremely intuitive. Let us consider an \( n \)-bit code. The maximum value of the data that can be encoded with multiplier \( m \) is:

\[
data_{\text{max}} = \left\lfloor \frac{2^n - 1}{m} \right\rfloor
\]
Thus, if $\log_2 m < r_b$, then some number of codewords in the code will never be used! Let us consider an example of MUSE(72,64) code with $m = 243$. The $\log_2 data_{max,m=243} = 64.075$, thus a range of 65-bit numbers can be encoded into 72-bit codewords. Such a behavior is not possible in a conventional parity-based ECC like Hamming code.

How do we exploit these additional states? For MUSE(72,64), the available space is less than 1 bit, but unlike standard Hamming or Hsiao codes, we know the maximum value that the data can take after encoding is $m \times (2^{64} - 1)$. A value higher than this is not possible. This creates a clear separation between the encoded codeword space and unused codeword space. We can use this codeword separation to implicitly derive metadata about the data. Let us say that a 64-bit data item can have property X or property Y. We could create an encoding where if the data has property X, then it is the normal space, and if it has property Y, then it falls in the normally unused space. When we see a value from the normally unused space, we know that the data item has property Y. To account for the fact that there are not enough codewords to represent property Y for all possible data values, we need to use this space when property Y holds for a smaller subset of the data.

Let us discuss a concrete example. Let us say that we want to determine if a piece of data is a pointer or regular data item. Usually, this would take one additional bit of information. However, with MUSE(72,64), we can use the following encoding. If the data value is a pointer, given that we know that pointers in 64-bit architectures are only 48 bits, then we can use the normally unused space. If we see a value in the normal space, we know that the data value is not a pointer, and if we see a value from a normally unused space, then we know that the value is a pointer. Several additional optimization techniques are possible over this basic scheme to use these “fractional” states.

It is possible to increase the number of states in the conventional parity-based codes too, for example, by adding more bits to the data and making the codeword longer. However, it may result in the data not being a multiple of 8B, which is not desirable because of the DDR standards in use today (and also it leads to memory fragmentation and performance degradation). Another option is to reduce reliability guarantees of the code and repurpose a portion of parity bits for storage so that the overall size of the codeword remains the same. MUSE ECC does not require non-standard interfaces and does not sacrifice the reliability to gain more state storage!

6. RESULTS

In this section we study the following questions:
1. How does the error correction capability of MUSE compare to a traditional SEC-DED code?
2. How does the error correction capability of MUSE compare to a chipkill code?
3. How do the VLSI overheads of MUSE compare to traditional codes?
4. How does the performance overhead of MUSE compare to traditional codes?

6.1 SEC-DED: Hamming vs MUSE

To compute the error rates for $b$-bit errors we sampled from all ($2^b$) permutations of columns in the parity check matrix of the Hamming code. If the sum $\mod 2$ of $b$ columns is not found in the parity check matrix, that $b$-bit error is considered successfully detected.

Figure 5 exemplifies how error detection rate of MUSE(72,64) with a multiplier $m = 243$ compares to two Hamming codes. The blue line is the SEC-DED Hamming 72,64 code, while the red line shows Hamming 72,65 code that represents the trade-off between the detectability of all double errors, and 1 bit of storage to store 265 states.3 The green line is for the MUSE(72,64) code with $m = 243$ and the ability to store $2^{59.77}$ extra states, while uniformly detecting 70.85% of multi-bit errors! Unlike MUSE ECC with a constant detection rate of multi-bit errors, Hamming(72,64) code detects all even weight errors and only 44.5% of the odd weight ones. While offering a comparable average detection rate for multi-bit errors of 71.6%, Hamming(72,64) code cannot provide even a single harvestable state (same applies to Hsiao codes).

6.2 CHIPKILL: Reed-Solomon vs MUSE

Similar to the analysis of Hamming codes, we used combinatorics to derive the multi-symbol detection rate for Reed-Solomon and MUSE codes. Out of all $k$-symbol error patterns in the $n$-symbol codeword, we randomly picked 10000 patterns, while for the errors with less than 10000 patterns, we picked all the patterns. To each symbol in the selected patterns, we randomly assigned error values and constructed a multi-symbol error. Overall, for each pattern we constructed

3There is no 72,65 Hsiao [20] code because with 7-bit parity only 57 odd weight vectors of length seven exist.
at least 1000 multi-symbol errors, so that for every \( k \)-symbol combination we evaluated \( 10^7 \) errors. For each multi-symbol error, we computed a syndrome and compared this syndrome to all the syndromes of single symbol errors. If no match is found, then that specific multi-symbol error is detectable. The fraction of detectable multi-symbol errors of all sampled multi-symbol errors is the multi-symbol error detection (MSED) rate.

Similarly, we derived the MSED rate for the \textit{MUSE} code. However, instead of syndromes, we computed multi-symbol error remainders and checked if those are not equal to the remainders of single symbol errors. Because \textit{MUSE} codes differentiate bit flip direction, only a half of the multi-symbol error remainders which are equal to the single symbol error ones will be considered as silent data corruptions. In those cases, correction of the error in the symbol will overflow and flip some bits in adjacent symbols. However, the code is constructed such that symbols and errors are disjoint the overflow will happen only during miscorrections.

Table 4 summarizes how \textit{MUSE} compares to Hamming and Reed-Solomon codes. Reed-Solomon codes offer higher level of MSED rates compared to \textit{MUSE}. For example, RS(144,128) has MSED rate of 93.73\%, while comparable \textit{MUSE}(144,133) has MSED rate of 76.93\%. On the other hand, \textit{MUSE} offers at least 5 extra bits of storage, while Reed-Solomon codes offers none. Potentially, those bits may be used to increase the reliability of \textit{MUSE} for double symbol errors at the cost of extra space. But even in this scenario, \textit{MUSE} will offer extra storage if used in its non-systematic form.

### 6.3 VLSI Overheads

We implemented the basic arithmetic blocks, decoders, encoders and error correctors in Verilog, and synthesized them with Synopsys Design Compiler Version: O-2018.06 using Low-Vt NangateOpenCell 45nm open-source standard cell library [46]. Designs were synthesized with full hierarchy ungroupping, and high effort for delay optimization. Table 5 summarizes the latency and silicon area of the decoder, encoder and error corrector for all discussed codes. For reference, Intel Xeon X5400 “Harpertown” series of CPUs was built with 45nm technology, had 1066–1600MHz bus between the CPU and the memory controller [23]. Thus, we will use “Harpertown” as a reference model to derive latency parameters of the decoders and encoders in our simulation models to evaluate the overheads of introducing \textit{MUSE} ECC into the system.

For example, the encoder of non-systematic single error correcting \textit{MUSE}(72,64) code is 0.59 ns, while the latency of the syndrome generator is 1.18 ns. The \textit{MUSE}(72,64) error correction is done via a lookup table of remainders paired to error values with total latency of error correction 0.84 ns. Assuming a clock frequency of 1600 MHz or 625 ps, pipelined encoder will incur additional latency of 1 clock cycle thus delaying the writes to main memory, while syndrome generation delays error detection by 2 more clock cycles. In case of an error, the total time to correct the error will be 2 cycles to generate the syndrome, and 2 more cycles to correct the error.

**Hamming Code Implementation.** Hamming codes are systematic, and hence when the codeword is read from memory, no additional operation beyond error checking is performed. The syndrome generator for Hamming codes is a simple XOR tree for binary multiplication of the codeword with the parity check matrix. We implement the Hamming code syndrome generator in Verilog and synthesize it. The latency of the syndrome generator, and thus error detection, is 0.4 ns, and takes 291\(\mu\)m\(^2\) of area. Encoders for the Hamming codes are built in the same fashion, and as a result, the latency is 0.54 ns with 343\(\mu\)m\(^2\). The error correction for Hamming codes is done by comparing the syndrome to the columns of the parity check matrix, the position of the matched column indicates the position of a corrupted bit. The total delay of the syndrome generation and error correction is 0.53 ns, with error correction circuit occupying 576\(\mu\)m\(^2\) silicon area.

**Reed-Solomon Code Implementation.** Similar to the Hamming code, the Reed-Solomon code is systematic as well, thus nothing should be done to separate the data from redundancy bits. For comparison, we implemented a series of decoders and encoders for Reed-Solomon codes:

- RS(40,32) based on Galois Field \(GF(16)\) as single device correct code for DDR5. As a result, the encoder requires 0.4 ns latency and 151\(\mu\)m\(^2\) of area, syndrome generator requires 0.4 ns latency and 111\(\mu\)m\(^2\) of area, and error correction is done in 0.87 ns and 444\(\mu\)m\(^2\) of area.
- RS(80,64) based on Galois Field \(GF(256)\) as single device correct code for DDR5. The encoding latency is 0.45 ns with the silicon area of 491\(\mu\)m\(^2\), the syndrome generation is done with 0.42 ns and 495\(\mu\)m\(^2\) of silicon area, and error correction requires 1.54 ns and 2777\(\mu\)m\(^2\).
- RS(144,128) based on Galois Field \(GF(256)\) as single device correct code for DDR4. The encoding and syndrome generation are done with 0.52 ns and 0.45 ns latency respectively, and 901/895\(\mu\)m\(^2\) of area, while error correction latency us 1.54 ns and silicon area is 2777\(\mu\)m\(^2\).
40.67 times more silicon area for both encoder and decoder than RS(80,64), while only 2 more clock cycles of latency. These high area overheads are expected because Wallace Tree nodes are 2 serially connected full adders, while XOR trees use single XOR gate.

In terms of error correction, Hamming code requires 2 cycles to decode the syndrome and correct the error, while MUSE(72,64) needs 4. Reed-Solomon has slightly smaller delay of 4 clock cycles, while MUSE needs 5. The lead of parity codes is due to being natively suited for binary arithmetic, and thus is not surprising. Because errors are rare events (and except for the case of permanent device failure) this additional 2 cycles latency has no significant effect on performance. Moreover, real systems tend to have real-time monitoring and logging, and failing devices are replaced frequently alleviating the need for operating under constant error correction.

### 6.4 Performance

**Simulation Setup.** We evaluated the impact of MUSE ECC decoder on performance on the gem5 simulator with the SPEC 2017 benchmarking suite [10]. We configured a Haswell-like CPU with 3.4GHz frequency, 64kB L1 cache equally split for instructions and data, L2 256kB/core, L3 of 8MB, and 8GB DDR4 memory. To emulate the latency of encoding we delay each store instruction by the latency of 8MB, and 8GB DDR4 memory. To emulate the latency of the encoder, and each load is delayed by the latency of the decoder. To achieve this goal we modified a memory controller of the gem5 simulator. For convenience, the details of the simulated system are summarized in Table 6.

For the simulation, we picked TimingSimpleCPU which provides detailed timing simulation of the memory subsystem, and executes the instructions in a single clock cycle. We used gcc 4.8.5 to build dynamically-linked all components.

**Results and Discussion.** Figure 6 summarizes the slowdown of SPEC 2017 for different error correction schemes introduced into the system. We normalize the results to the system with no ECC present, i.e. no additional delays for memory accesses. As expected, a non-systematic MUSE SEC (yellow bars) code causes the highest performance hit – 0.35% on average, because every memory read will require to decode the data first, as its encoded in a non separable way. The comparable Hamming code (green bars) has a 3x smaller slowdown of 0.11%. As we see from the results, MUSE, despite taking 2 more cycles on each write, has the same 0.11% system slowdown as Reed-Solomon code (red bars).

### 7. RELATED WORK

MUSE builds on several advances over a period of 60 years and has some very interesting history. A brief historical overview is presented in Figure 7.

About the same time when BCH and Reed-Solomon codes were developed [8, 19, 43], Brown in 1960, published what is now referred to as an “AN” code [9]. The work was developed in the context of robust error correction for arithmetic circuits. To generate a codeword for a data word N it is multiplied by an integer A. To retrieve the data word (and/or check for errors), the code word is divided by A. In AN codes, if the sum of two codewords, say, A · x and A · y, is also a code word, A · (x + y), and any error in addition or subtraction can be identified by dividing the result by A and checking the error remainder. A variation of AN codes called residue codes [12, 18] were also developed in the context of fault-tolerant arithmetic units. Instead of creating a code word as A · N, residue codes are created as N × P + A − B where P is a power of 2 and B is the remainder when N is divided.

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Table 5: Implementation results of syndrome generators/encoders/correctors for MUSE and parity-based ECC schemes

| Code                | Syndrome Gen. | Encoder | Corrector |
|---------------------|---------------|---------|-----------|
|                     | Latency, ns   | std_cells Area, µm² | Latency, ns   | std_cells Area, µm² | Latency, ns   | std_cells Area, µm² |
| MUSE(144,133)       | 2.12          | 29609   | 46332     | 1.94          | 25194         | 41287       | 1.08          | 8183         | 7507       |
| MUSE(80,70)         | 1.8           | 29043   | 16372     | 1.81          | 14358         | 23734       | 1.13          | 7881         | 7292       |
| MUSE(72,64)         | 1.18          | 11410   | 18065     | 0.59          | 1680          | 1697        | 0.88          | 2459         | 2230       |
| Hamming(72,64)      | 0.4           | 191     | 291       | 0.45          | 158           | 343         | 0.53          | 446          | 576        |
| RS(144,128)         | 0.45          | 512     | 895       | 0.52          | 484           | 901         | 1.54          | 2643         | 2777       |
| RS(80,64)           | 0.42          | 248     | 495       | 0.45          | 249           | 491         | 1.56          | 2356         | 2415       |
| RS(40,32)           | 0.94          | 99      | 151       | 0.4           | 72            | 111         | 0.87          | 419          | 444        |

```latex
\text{Table 5: Implementation results of syndrome generators/encoders/correctors for MUSE and parity-based ECC schemes.}
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Figure 6: Slowdown of a system due to ECC encoding/decoding on a memory interface. Modeled in gem5 using latencies from decoders/encoders synthesized with NanGateOpenCell 45nm open source process (See Section 4).
by a multiplier $A$. The nice thing about this construction is that it makes the code systematic, i.e., the data bits are separated from the check bits. These work and other works [6, 34] were published during the pre-Moore’s-Law time frame, and there was likely a significant paucity of transistors that multiplications and divisions could not be performed to check addition. These ideas appear to have remained of theoretical interest till the early 70s [5]. In 1970 The STAR Computer\footnote{Avizienis was awarded the Eckert Mauchly award for his pioneering work on this project} was presented [4] - a research project funded by NASA with the goal of developing a reliable computer for space probes [14]. Finally, Sullivan [48], in 2010, explored the idea of using residue codes in the context of modern ALUs.

In 1966, Dennard invented DRAM, and soon after there was a flurry of work on improving the reliability of these new “high-speed” memories [11]. While technology scaling in the 1970s permitted the creation of single-chip microprocessors in this era, latency was still a significant concern, and it was believed that high-speed memories would need error correction techniques that can “encode and decode” in parallel [42]. Alas, the arithmetic and residue error codes cannot be parallelized unless significant restrictions are placed on

In 1994, Grunlund and Montgomery published a paper “Division by invariant integers using multiplication” [16] in the Programming Languages Design and Implementation Conference. They observed that computers were multiplying much faster than dividing — around one order of magnitude, — so they asked the question, would it be possible to perform a division as a multiplication. For division by constants this is clearly possible, especially if the constants can be precomputed at the compile time of the program. For instance, to divide a number by 5, we can multiply it by 0.2. To avoid floating point calculation we can multiply this by a large integer factor that is a power of 2, and then divide by the large integer factor. The last division is implemented by a shift operation which is really cheap. We leverage this advance in this paper to enable all the benefits of AN and residue codes.

In the early 90s, most server systems still employed parity for error detection. The race for more reliability and availability features increased with the rise of e-commerce websites in the late 90s. IBM introduced “ChipKill” memory, a commercial name for a system that uses Reed-Solomon codes. Unlike parity, ChipKill can continue operation even if an entire DRAM device fails. Basically, in the late 90s, the error model moved from single errors to supporting burst errors.

Figure 7: Historical timeline of significant developments with respect to AN codes.

Table 6: Simulation model and parameters

(A) gem5 simulated system configuration

| Core       | 2.4GHz Haswell-like @ 3.4GHz |
|------------|-----------------------------|
| L1-I Cache | 32kB, 8-way, 1-cycle latency |
| L1-D Cache | 32kB, 8-way, 3-cycle latency |
| L2 Cache   | 256kB, 8-way, 6-cycle latency |
| L3 Cache   | 8MB, 16-way, 18-cycle latency |
| DRAM       | 8GB, DDR4-2400               |

(B) Decoder/Encoder latency in cycles

| ECC                  | Encode delay | Decode delay |
|----------------------|--------------|--------------|
| Baseline (no ECC)    | 0            | 0            |
| Hamming 72.64        | 1            | 0            |
| RS(144,128), 80,64   | 1            | 0            |
| (40,32)              | 1            | 0            |
| MUSE(72,64)          | 2            | 3            |
| MUSE(144,133)        | 4            | 0            |

Table 7: Division by multiplication

| ECC                  | Encode delay | Decode delay |
|----------------------|--------------|--------------|
| Baseline (no ECC)    | 0            | 0            |
| Hamming 72.64        | 1            | 0            |
| RS(144,128), 80,64   | 1            | 0            |
| (40,32)              | 1            | 0            |
| MUSE(72,64)          | 2            | 3            |
| MUSE(144,133)        | 4            | 0            |
These types of availability features were also used in space missions such as NASA's pathfinder MARS probe [22]. In contrast to these popular burst codes, MUSE provides the same or better reliability with fewer check bits.

In 2000, JEDEC standardized the DDR interface to memory [25]. Standardization meant interoperability but it also introduced several constraints on how memory would be integrated, and pertinently, how error correction could/should be performed. DDR4 memory ECC DIMMs are 72 bits wide – 64 bits of data and 8 bits for check bits. This architecture can be used to implement a 72,64 code, or a 144,128 code [2]. Typically, the 72,64 code supports SEC-DED using Hsiao or Hamming codes, and 144,128 is used for single and burst error correction. With the continuing technology and voltage scaling trends, DRAM has suffered more and more reliability problems, especially Low-Power DDR memories (used in mobile phones and embedded devices). As a mitigation vendors started to implement on-die ECC [24, 36], typically as simple SEC-DED codes without the ability to correct burst errors. The idea of using on-die error correction has now been standardized in the latest generation of JEDEC’s DDR5 standards [26]. Our MUSE code works in this context, and is orthogonal to on-die ECC in memories.

Along with the growth in reliability problems, the last decade also witnessed an increase in security problems. Several companies have proposed solutions that increase the demand for memory including encrypting memory [27], adding authentication code [13], or requiring additional storage to support software reliability [3]. MUSE ECC was developed to be able to support both reliability and security. Prior work in the area of co-designing security and reliability assumes standard ChipKill or SEC-DED code [21, 44, 45] and those codes do not provide a way to extract more state for security or performance features or reduce the amount of storage for reliability which are key contributions of MUSE ECC. MUSE ECC is also orthogonal to architectural optimizations such as Frugal ECC [30], Virtualized ECC [52], and COP [37]. These layout ideas can be used with MUSE to increase the reliability of these techniques further.

8. CONCLUSION

In this paper, we present a novel ECC construction that provides the same reliability as other ECCs but crucially also allows spare ECC space to be harvested and used for additional purposes. Using simple multiplication and division properties, MUSE ECC encodes, decodes, detects, and corrects multi-bit errors that may occur in DRAM. Additionally, we introduce the novel optimizations of shuffling and aliasing to enable finding suitable multipliers for our scheme. With these optimizations and specialized hardware, we propose the first ECC scheme that offers significant improvements since the traditional ECC methods were introduced. When we evaluated the error correction on the SPEC 2017 benchmarks, we not only found successful uniform single- and multi-bit error correction, but also significant extra states, reasonable area overhead, and negligible performance overhead. A remaining challenge for this work is finding even better multipliers and symbol shuffles. While we were able to find a multipliers and shuffles both these problems are NP-hard. It is indeed possible that even more space savings are possible with better multipliers and shuffles. The benefits of MUSE codes also go beyond space savings and holding metadata. For instance, MUSE codes integrate much more easily into processing in memory style computations and homomorphic computations, making MUSE a very exciting ECC option for the next decade and beyond.

9. ACKNOWLEDGEMENTS AND DISCLOSURES

This work was supported through gifts from Bloomberg and Qualcomm, a Qualcomm Innovation Fellowship, and support from Columbia University. Simha Sethumadhavan has significant financial interest in Chip Scan. Patent pending technology.

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