Die-Stacked DRAM: Memory, Cache, or MemCache?

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Abstract
Die-stacked DRAM is a promising solution for satisfying the ever-increasing memory bandwidth requirements of multi-core processors. Manufacturing technology has enabled stacking several gigabytes of DRAM modules on the active die, thereby providing orders of magnitude higher bandwidth as compared to the conventional DIMM-based DDR memories. Nevertheless, die-stacked DRAM, due to its limited capacity, cannot accommodate entire datasets of modern big-data applications. Therefore, prior proposals use it either as a sizable memory-side cache or as a part of the software-visible main memory. Cache designs can adapt themselves to the dynamic variations of applications but suffer from the tag storage/latency/bandwidth overhead. On the other hand, memory designs eliminate the need for tags, and hence, provide efficient access to data, but are unable to capture the dynamic behaviors of applications due to their static nature.

In this work, we make a case for using the die-stacked DRAM partly as main memory and partly as a cache. We observe that in modern big-data applications there are many hot pages with a large number of accesses. Based on this observation, we propose to use a portion of the die-stacked DRAM as main memory to host hot pages, enabling serving a significant number of the accesses from the high-bandwidth DRAM without the overhead of tag-checking, and manage the rest of the DRAM as a cache, for capturing the dynamic behavior of applications. In this proposal, a software procedure pre-processes the application and determines hot pages, then asks the OS to map them to the memory portion of the die-stacked DRAM. The cache portion of the die-stacked DRAM is managed by hardware, caching data allocated in the off-chip memory. Through detailed evaluations of various big-data applications, we show that our proposal improves system performance by 28% and up to 139% over the previous best-performing proposal.

1 Introduction
The increase in core count of chip multiprocessors (CMPs) has been driving the designs into the memory bandwidth wall, mainly because of pin count limitations [14, 41, 65]. Current CMPs with tens of cores already lose performance because of the limited bandwidth of DIMM-based DDR memories, and the problem is exacerbated as the number of cores increases [46, 59]. Therefore, continuing performance scaling through core count scaling requires a commensurate enhancement in the bandwidth of the memory system.

Emerging die-stacked DRAM technology is a promising solution to fulfill the ever-increasing bandwidth requirements of multi-core processors. The progress in manufacturing has enabled stacking several DRAM modules on the active die using high-density through-silicon vias (TSVs). Compared to traditional DIMM-based DDR memories, die-stacked DRAM provides several orders of magnitude higher bandwidth, but with approximately the same latency [6, 20, 21, 51, 71, 73]. In recent years, several models have been developed for the die-stacked DRAM [2, 3, 5, 6, 9], and many commercial vendors have planned to use such models in their products [4, 7, 8, 10, 49, 72].

One critical feature of the die-stacked DRAM is its limited capacity. Technological constraints, such as power-delivery and thermal limitations, restrict the size of the die-stacked DRAM to utmost a few gigabytes [35, 53]. As such, it cannot accommodate the whole datasets of modern big-data applications with the datasets ranging from hundreds of gigabytes to a few terabytes. Consequently, prior proposals use the die-stacked DRAM either as a memory-side cache [28, 34, 42, 43, 44, 45, 52, 56, 57, 64, 69, 70, 80, 84, 86] or as a part of software-visible main memory [11, 12, 26, 58, 60, 68], as shown in Figure 1.

DRAM caches can quickly react to changes in the data working sets of applications, and use the DRAM capacity...
more effectively by evicting cold data and keeping actively-accessed objects. However, the DRAM cache designs suffer from the tag overhead, which is substantially more than the tag cost of traditional SRAM caches. As the size of the die-stacked DRAM is quite large, managing it as a cache requires megabytes of storage, somewhere in the system, for storing the tag information. As placing such a large structure in the active die (i.e., SRAM) is impractical, most proposals put the tags in the die-stacked DRAM itself [33, 39, 43, 57, 64, 84]. Nevertheless, placing the tags in the die-stacked DRAM can add significant latency to the critical path of cache accesses, as the DRAM should be accessed twice; once for the tag and then for the data. Some approaches [43, 64] store the tags and data next to each other and stream them out together in a single access to avoid this serialization latency overhead. While these approaches are able to mitigate the latency overhead of tag-checking, they still incur significant extra bandwidth overhead.

On the other hand, using die-stacked DRAM as a part of main memory eliminates the main drawback of caches: there is no need for tags. Consequently, no tag storage is required, and the tag latency/bandwidth overhead is eliminated. Memory, however, cannot respond to dynamic variations in the data working sets of applications, due to its static nature. In memory designs, over time, there would be many pieces of cold data in the die-stacked DRAM that are not currently being used, wasting its capacity. Prior work [60] proposed to swap pages between die-stacked and off-chip DRAM periodically, using run-time Operating System (OS) support. Upon each period, the OS identifies hot and cold pages in off-chip and die-stacked DRAM, respectively, and swaps them in order to have the currently-used pages in the high-bandwidth DRAM. Such approaches, nonetheless, are not cheaply-realizable and present significant challenges to both software and hardware. First, as OS intervention is very time-consuming, the periodic intervals should be large enough (e.g., hundreds of milliseconds) to amortize the enormous costs of interrupts, page migrations, and TLB shootdowns.

As such, the pages that are highly-utilized for a short duration of time cannot be captured by these approaches. Second, as full OS pages should be transferred between die-stacked and off-chip DRAM, there is a significant bandwidth overhead associated with these approaches. Third, as the OS has no precise information about the utilization of pages at runtime, it cannot robustly rank them, and correctly identify hot and cold pages.

In this work, we make a case for using the die-stacked DRAM partly as main memory and partly as a cache (Figure 1-c). We corroborate prior work [22, 26, 61] that using the whole capacity of the die-stacked DRAM as a part of the main memory is suboptimal to using it as a cache. However, we observe that, in modern big-data applications, there are numerous hot pages with a large number of accesses. Based on this observation, we classify application datasets into two distinct categories: hot datasets (hot pages), and transient datasets (transient pages). Hot datasets refer to data objects that are accessed steadily by an application and serve a significant fraction of memory accesses throughout the whole execution of an application. Transient datasets point to data structures that are utilized only for a short period of time. In this work, we suggest MemCache for exploiting such heterogeneity in the access behavior of applications in the context of multi-gigabyte die-stacked DRAM. We suggest to use a portion of the die-stacked DRAM as a part of main memory and allocate hot pages in this part and use the rest of the capacity of the die-stacked DRAM as a hardware-managed cache to capture the transient datasets of applications. By allocating hot pages in the memory portion of the die-stacked DRAM, a considerable fraction of accesses are served from the high bandwidth memory without the overhead of tag-checking. The cache portion of the die-stacked DRAM remains intact and caches the transient datasets, providing quick responses to the dynamic variations in the datasets of applications.

To identify hot pages, we use a static profile-based approach before the execution of an application. A software procedure, incorporated into the compiler, pre-processes the application and sorts the pages based on their access frequency. Then it picks the top pages and asks the OS to map them to the memory portion of the die-stacked DRAM. We show that by using a representative input-set, such an offline analysis can classify pages robustly.

We evaluate MemCache against the state-of-the-art cache and memory proposals for the die-stacked DRAM and show that it significantly outperforms them on various big-data applications. Compared to a baseline without die-stacked DRAM, MemCache offers 114% performance improvement on average and up to 309%. Meanwhile, MemCache outperforms the best-performing prior design (Banshee Cache [84]) by 28% on average and up to 139%.

2 Background

Modern big-data applications have vast datasets that dwarf capacity-limited SRAM caches and reside in memory [15, 30]. Such applications frequently access the off-chip memory for data, putting significant pressure on the DRAM modules. Consequently, substantial performance is lost solely because of bandwidth limitations of the off-chip memory.

Recent research suggests using the die-stacked DRAM to break the bandwidth wall [18, 55]. As die-stacked DRAM cannot accommodate the whole datasets of big-data applications, prior proposals use it either as a large cache or as a part of main memory. In this section, we explore and discuss the design space of the die-stacked DRAM.
2.1 Die-Stacked DRAM as a Memory-Side Cache

One major challenge in architecting a giga-scale DRAM cache is microarchitecting the tags. Since the size of die-stacked DRAMs is in the range of several gigabytes, maintaining the tag information of such a large structure requires megabytes of storage. For example, the tag array of a 4 GB block-based DRAM cache requires in excess of 64 MB of storage. Managing the DRAM as a page-based cache reduces the tag storage to nearly 14 MB, which is still significant. Obviously, affording such large structures in SRAM is impractical; hence, most practical approaches store the information within the die-stacked DRAM itself. However, storing the tag information in the die-stacked DRAM imposes latency and bandwidth overheads, because, before every data access, the corresponding tag information should be checked via accessing the die-stacked DRAM. Many pieces of prior work targeted this overhead and suggested techniques to improve latency and/or bandwidth efficiency of cache accesses.

Various design objectives (e.g., hit latency, bandwidth-efficiency and hit ratio) have been considered in architecting giga-scale DRAM cache designs. Alloy Cache [64] is a block-based cache design that targets minimizing hit latency using a direct-mapped organization. Alloy Cache locates data and the corresponding tag, adjacently, and streams them out upon each access. This way, the latency of tag-checking is eliminated from the cache access if the access hits in the DRAM cache. Nevertheless, Alloy Cache suffers from two fundamental inefficiencies: (1) extra die-stacked DRAM bandwidth is consumed for accessing tag information, and (2) low hit ratio because of being a block-based cache and employing a direct-mapped organization.

Unison Cache [43] improves the hit ratio of a DRAM cache by caching the data at the page granularity with a set-associative structure. As the size of the tag array, even for page-based designs, is significant, Unison Cache likewise co-locates the tag and data in the die-stacked DRAM. Caching the data at the page granularity improves the hit ratio but imposes substantial bandwidth overhead, because many blocks of a page are never used during the residency of the page in the DRAM cache [42, 44]. Moreover, employing a set-associative organization necessitates searching all cache ways before touching the data, which adds latency and bandwidth overheads to the cache accesses.

Naively implementing a page-based design not only does not improve performance but may also harm it, mainly because of bandwidth inefficiency [42, 44, 45, 84]. To reduce the traffic of page-based caches, Unison Cache takes advantage of a predictor for fetching the blocks within a page that will be used while the page is in the cache (i.e., referred to as the footprint of the page [44]). Upon a cache miss, only those blocks within the requested page that are predicted to be used will be brought into the cache to reduce the traffic. While this technique (i.e., footprint caching) is useful at reducing the bandwidth usage, its efficiency is restricted by the accuracy of the predictor. For every misprediction, either the cache suffers from an extra miss due to not having the requested block in the cache, or non-useful blocks will be brought into the cache, wasting valuable bandwidth of off-chip and die-stacked DRAM. Moreover, the naive implementation of a set-associative structure requires two serialized accesses to the DRAM cache to get a cache block: (1) one access to read the tags and identify the location of the piece of data (i.e., way) and (2) another access to read the piece of data. To reduce the cache access latency, Unison Cache uses a way predictor to access the requested block with two overlapped read operations for tag and data. Unfortunately, every time the predictor makes a mistake, the cache has to be accessed one more time, which increases the cache access latency and wastes valuable cache bandwidth. Moreover, even when the prediction is correct, extra bandwidth is consumed for accessing tag information, which puts further pressure on the die-stacked DRAM.

Another kind of DRAM caching approaches, referred to as Tagless DRAM Cache (TDC) [42, 52], align the granularity of caching with OS pages to track the tags of cache-resident pages within the Page Table and Translation Lookaside Buffers (TLBs). With such approaches, whenever a TLB miss occurs, the information of residency of the page in the DRAM cache (e.g., whether the page is cached or not and the location of the page in the DRAM cache if it is cached) are fetched together with the corresponding Page Table Entry (PTE). This way, the latency of tag-checking becomes virtually zero, but at the cost of significant complexities that are pushed into both software and hardware. In such approaches, the contents of the TLBs of all the cores should (seem to) be coherent. Therefore, they use system-wide TLB shootdowns for updating the content of all TLBs whenever a piece of data is replaced in the DRAM cache. In addition to the complexities that are imposed because of run-time hardware-software co-operations, frequent TLB shootdowns cause significant performance degradation due to costly software interventions and present a scalability challenge, as the latency of system-wide TLB shootdowns increases with increasing the core count [60, 66].

Another major drawback of these methods is the massive bandwidth overhead which is consumed because of fetching data at page granularity. Techniques like footprint caching [44] have limited applicability for such schemes, as these methods are restricted to use otherwise-unused bits in the PTEs to store footprint metadata, which is not adequately-spacious storage. For example, recent 64-bit Intel Xeon Phi processors [72] use 64-bit PTEs, in which, 18-bits are left unused. However, a 4 KB page includes 64
cache blocks, and hence, 64-bits are required to precisely record the corresponding footprint information (i.e., one bit for each block, representing whether or not the block was touched during the last residency of the page in the cache). Footprint-augmented TDC (F-TDC) [42] attempts to solve this problem by storing \( m \)-line granularity footprint metadata, where a single bit is used to represent the existence of \( m \) cache blocks in the footprint of each page, in order to fit within the capacity limitations of PTEs. Unfortunately, this strategy leads to the over-fetching of data and bandwidth pollution, as the precise knowledge of the residency of cache blocks is lost. On each misprediction, up to \( m \) blocks are over-fetch, which leads to further bandwidth pollution. The problem is even more significant because modern big-data applications heavily use large (e.g., 4 MB) and huge (e.g., 1 GB) OS pages for increasing the TLB reach, as discussed in the recent work [63]. Employing \( m \)-line granularity footprint prediction for 1 GB pages requires saving 1 bit for every 450 K blocks. As a consequence, upon every misprediction, up to 450 K cache blocks are over-fetch, imposing an unbearable bandwidth overhead.

Lastly, since these methods use different address spaces for caches (i.e., SRAM caches plus a DRAM cache) and off-chip memory, and because they do not flush the state entries of SRAM caches after each page remapping, they sacrifice consistency among physical addresses and are prone to result in wrong execution\(^2\).

Recent work, namely the Banshee Cache [84], addresses the first problem by coalescing Page-Table updates. The Banshee Cache caches the details of recently-remapped pages (i.e., pages that were recently placed in or evicted from the DRAM cache) in an auxiliary SRAM structure, named the Tag Buffer. Whenever the occupancy of the Tag Buffer exceeds a certain threshold, a software interrupt is triggered to flush its entries into the Page Table and the TLBs. By provisioning enough capacity for the Tag Buffer (e.g., \( \sim 5 \) KB), the frequency of Page Table updates decreases, which helps amortize the high cost of software interrupts. However, employing such a structure imposes SRAM storage overhead and may present scalability challenges as the core count increases. With more cores, the pressure on the Tag Buffer increases as the frequency of re-mapping increases, resulting in more frequent flushes and costly software interventions. Therefore, the size of the Tag Buffer should commensurately be increased when increasing the number of cores, to preserve performance scalability. Furthermore, the complexity of run-time hardware-software co-operation is still a problem, as software is responsible for flushing the Tag Buffer into the Page Table and TLBs. To reduce the over-fetching problem, the Banshee Cache uses a bandwidth-aware replacement policy, in which, pages are replaced lazily to lower the bandwidth pressure on die-stacked and off-chip DRAM. While the replacement policy is effective at reducing the movement of pages, it still consumes extra bandwidth to access page metadata (e.g., tag and replacement information) stored in the die-stacked DRAM. Finally, the Banshee Cache solves the address consistency problem of previously-proposed Page Table based approaches by using the same address space for the die-stacked and off-chip DRAMs.

2.2 Die-Stacked DRAM as a Part of Main Memory

Using the die-stacked DRAM as a part of main memory eliminates the necessity of tags, and hence tag overheads, the major drawback of cache designs. The OS allocates some of the pages in the die-stacked DRAM physical address space and the rest in the off-chip DRAM. Such a scheme, however, cannot respond to dynamic changes in the data working sets of applications. Even if the OS applies intelligent algorithms for allocating hot pages in the high-bandwidth die-stacked memory, over time, there would be many pages in the die-stacked DRAM that are not currently being used, wasting its precious capacity. This happens because modern big-data applications have many dynamic data-dependent behaviors, which cannot be detected/exploited statically before the execution of an application at page-allocation time [40, 75].

Several pieces of prior work [26, 60, 68] propose swapping pages between the high- and low-bandwidth memory, periodically, to capture the dynamic data-dependent behavior of applications throughout their execution. In the state-of-the-art approach [60], regularly, the OS ranks all pages based on their usage and moves hot pages into the die-stacked DRAM and cold pages out.

Unfortunately, such approaches suffer significantly from the massive cost of page swapping concerning both latency and bandwidth. In each interval and after the page swapping, the OS should update all PTEs and shoot down all TLBs for coherence, which takes a considerable amount of time. Moreover, exchanging many pages between die-stacked and off-chip DRAM consumes considerable bandwidth, as whole pages (and not their footprints, as in cache designs) should be transferred. For example, swapping two 4 KB pages, \( P1 \) and \( P2 \), requires 16 KB of data transfer bandwidth: 4 KB for reading \( P1 \), 4 KB for writing \( P1 \), 4 KB for reading \( P2 \), and 4 KB for writing \( P2 \). If an application has many transient pages, the number of pages that should be swapped in each interval is also increased, exacerbating the bandwidth inefficiency of these approaches. Therefore, these methods perform the page swapping at very coarse granularity (e.g., hundreds of milliseconds) to amortize the associated latency and bandwidth overheads. Consequently, the pages that are highly-utilized for a short duration of time (which we call transient pages) cannot be captured by these approaches.

Another drawback of these methods is the limited ability to detect hot pages. As the OS has no precise information

\(^2\)We do not further discuss this problem, as it is entirely addressed in the recent work [84], where it is called the address consistency problem.
about the utilization of pages at run-time, it cannot accurately rank them, and correctly identify hot and cold pages. Usually, there is a single bit in each PTE that indicates whether the page is used or not, and no knowledge of access frequency is available at run-time. Therefore, precisely ranking the pages at execution time requires non-trivial changes to both hardware and software, which makes such designs more complex.

3 Motivation

We first show that, in modern big-data applications, there is a discrepancy in page usage; some of the pages are used more frequently than the others. Then we compare two extreme use cases of the die-stacked DRAM: (1) whole die-stacked DRAM as a cache, and (2) whole die-stacked DRAM as a part of main memory. Finally, we motivate to use a part of the die-stacked DRAM as main memory and the rest as a cache.

3.1 Hot Pages

Corroborating many pieces of prior work (e.g., [11, 12, 45, 61, 75, 79, 80, 84]), we observe that, in modern big-data applications, there are many hot pages with a large number of accesses. Hot pages refer to the phenomenon that some pages are accessed with higher frequency than the others. This causes a small fraction of an application’s memory working set to serve a significant fraction of accesses (e.g., 10% of data working set serve 80% of requests).

Figure 2 shows the cumulative distribution of accesses to the main memory for several big-data applications. The figure shows that most of the applications contain many hot pages that serve a significant fraction of total memory accesses. For example, in pr, only 10% of pages (~7 GB of memory footprint) serve more than 91% of requests. The figure further indicates that applications consist of many transient pages. As an example, in pr, the remaining 9% of accesses are distributed among 90% of pages with nearly the same access frequencies. We find that hot pages that are responsible for a significant fraction of accesses are used steadily throughout the whole execution of applications. In contrast, transient pages are used only for a short period of time.

The existence of hot pages motivates identifying and allocating them into the die-stacked memory to efficiently exploit the higher bandwidth that it provides. However, if we use the whole capacity of the die-stacked DRAM as a part of main memory and allocate hot pages into it, transient pages will be served from the off-chip DRAM. In contrast, if we use the die-stacked DRAM as a cache, we can serve both hot and transient datasets from the die-stacked DRAM, but have to pay the tag overhead (cf. Section 2.1).

3.2 Full-Cache Versus Full-Memory

If the goal is to use the die-stacked DRAM as a part of main memory, the best one can do is to place pages with the highest number of references (i.e., hottest pages) in the die-stacked memory. Figure 3 shows the number of requests that go off-chip in a 4 GB die-stacked memory normalized to a 4 GB page-based cache for several big-data applications. In this experiment, we go over the sequence of accesses and find pages with the highest number of accesses and place them in the die-stacked memory.

As Figure 3 clearly shows, using the whole capacity of the die-stacked DRAM as a memory considerably increases the number of accesses to the bandwidth-limited off-chip DRAM, as compared to using it as a cache. It comes from the fact that a die-stacked DRAM as memory cannot adapt itself to the dynamic run-time changes in the data working set of applications and yet is not large enough to capture the entire datasets of big-data applications. The results indicate that even an ideal memory, which is oracularly filled with the hottest pages, increases the number of off-chip accesses from $4.6 \times$ in sssp to $60.5 \times$ in tc, as compared to a cache design. The results are consistent with those of prior work [22, 26, 61] concluded that, for big-data applications, memory designs are inferior to caches at reducing the number of off-chip accesses.

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3We elaborate more on this observation later in Section 6.6.
3.3 What Fraction of Die-Stacked DRAM Can Be Turned into Memory?

Even though using the whole capacity of the die-stacked DRAM as a part of main memory increases the number of off-chip accesses as compared to caches, the existence of hot pages with a considerable number of accesses may suggest that we can use a part of the die-stacked DRAM as a memory for hosting a subset of such hot pages and use the rest of the capacity as a cache for capturing the dynamic data-dependent behavior of applications.

The single major drawback of using the die-stacked DRAM as memory is its inability to respond to dynamic changes of applications. Over time, many transient pages will emerge in the data working set of an application, and since such pages were not detected and allocated in the die-stacked DRAM, a large number of requests will be sent to the bandwidth-limited off-chip memory. This causes memory designs to offer an order of magnitude lower hit\(^1\) ratio (higher off-chip accesses) as compared to cache designs (cf. Section 3.2). Therefore, the mixture design (i.e., the design which uses the die-stacked DRAM partly as main memory and partly as cache) will lose nothing compared to the full-cache design, if it is able to offer a hit ratio as high as the cache.

In order to determine what fraction of a die-stacked DRAM can be turned into memory without losing the benefits of the cache design, we first consider the die-stacked DRAM as a set of frames. Each frame in the die-stacked DRAM is a physical location where a piece of data at the granularity of a page reside, regardless of the fact that the die-stacked DRAM is managed as a cache or as a memory. We first consider the whole die-stacked DRAM as a sizeable page-based cache and calculate the Average number of Hits per Frame (AHF). Then we turn each frame into memory and allocate the hottest unallocated page in it until the AHF becomes smaller than that of the cache. Algorithm 1 summarizes the steps that we take in order to determine the fraction of die-stacked DRAM that can be turned into a memory.

Figure 4 shows the fraction of a 4 GB die-stacked DRAM that can be managed as memory and still offer the same hit ratio as a 4 GB page-based cache. As the figure shows, a significant fraction of the die-stacked DRAM can be managed as a memory without negatively increasing the number of off-chip accesses. The fraction ranges from 11% in gems\(^2\) to 96% in pr, with an average of 65%. This means that, on average, 65% of a 4 GB DRAM can be turned into memory without losing the benefits of a full-cache design. Note that, this is the fraction, at which, the hit ratio of the design that uses the die-stacked DRAM partly as main memory and partly as cache remains intact as compared to the full-cache design. While the hit ratio is important for die-stacked DRAM organizations, prior work showed that minimizing hit latency [64] or efficiently utilizing the die-stacked DRAM bandwidth [84] are of equal importance if not more. As memory organizations generally offer lower access latency than cache organizations and do not waste DRAM bandwidth for replacements/tag manipulations, we expect that even a larger fraction of the die-stacked DRAM (> 65% on average) can be managed as a part of main memory. We determine the fraction of the die-stacked DRAM’s capacity that can be managed as a memory using a performance sensitivity analysis in Section 6.4.

Taking advantage of this observation, we propose to use a portion of the die-stacked DRAM as a part of the main memory and allocate hot pages to it and use the rest of the capacity of the die-stacked DRAM as a hardware-managed cache to capture the transient data-dependent behavior of applications. By allocating hot pages in the memory portion of the die-stacked DRAM, a significant fraction of accesses is served from the high-bandwidth memory without the overhead of tag-checking (bandwidth and latency). The cache portion of the die-stacked DRAM also remains intact and

\(^{1}\)In this paper, by hit, we refer to a state where the requested data is in the die-stacked DRAM, regardless of the fact that it is managed as a cache or as a part of memory. Analogously, by miss, we refer to the state, in which, the requested data is not in the die-stacked DRAM.

\(^{2}\)gemsm is an exceptional case, in which, requests are distributed among all pages with nearly the same frequency (i.e., it does not have a considerable number of hot pages. cf. Figure 2).

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**Algorithm 1 Calculate the Memory Fraction**

1. `cacheAHF = totalCacheHits/dramFrames;`
2. `pages = sort(pages);`\(^\star\) Sort pages based on their access count
3. `memFrames = 0;`
4. `totalAccessesToMemFrames = 0;`
5. `while (totalAccessesToMemFrames ≥ memFrames × cacheAHF) do`
6. `hotPage = pages.top();`\(^\star\) The hottest unallocated page
7. `memFrames ++;`\(^\star\) Allocate the hot page in the die-stacked memory
8. `pages.removeTop();`
9. `totalAccessesToMemFrames += hotPage.accessCount;`
10. `done`
11. `memFraction = memFrames/dramFrames;`

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![Figure 4](image-url)
caches the transient pages, providing quick responses to dynamic variations in the datasets of applications.

4 The Proposal

In order to exploit the heterogeneity in the access behavior of applications to hot and transient pieces of data, we propose MemCache, a design that uses a part of the die-stacked DRAM as main memory and the rest as a cache. The software is responsible for filling the die-stacked memory with the identified hot pages. The transient pages are also served from the hardware-managed cache portion of the die-stacked DRAM. For every Last-Level SRAM Cache (LLSC) miss, if the miss address is mapped to the memory portion of the die-stacked DRAM, it is served by the die-stacked memory (i.e., without the overhead of tag-checking). Otherwise, it checks the DRAM cache tag array. In case of a cache hit, the request is served by the cache portion of the die-stacked DRAM, and in case of a cache miss, it proceeds to the off-chip memory.

4.1 Memory Portion

The memory frames of the die-stacked DRAM should be filled with the hot pages of applications. First off, the hot pages of an application should be identified. We use a profiling approach in order to distinguish hot pages from cold ones. A software procedure, incorporated into the compiler, using profiling, determines which virtual pages of the application are hot. To do so, the software procedure sorts virtual pages based on their access count, in descending order, and then, conveys this information as clues to the page allocation unit of the OS.

There are quite a few ways to implement the profiling step needed in our mechanism, two of which are more common and are elaborated upon here. One approach is that the compiler profiles the program by simulating the behavior of the on-chip cache hierarchy of the target machine [27]. The simulation is used to gather the access counts of pages, which are then used to identify hot pages. Note that, such a profiling approach does not necessitate an accurate timing simulation of the processor and cache hierarchy; rather, it requires simply a trace-driven simulation of memory operations in order to gather information about accesses that are not captured in on-chip SRAM caches (i.e., LLSC misses and evictions). Another approach for implementing the profiling step is relying on hardware support. In this strategy, the target machine provides support for profiling operations (e.g., Informing Load Operations [37]). With this support, throughout the profiling run, the compiler gathers the access counts of application’s pages, and at the end, sorts them accordingly. In this paper, we use the first approach as it requires no change in the hardware.

Identifying hot pages by the compiler demands for a sample inputset on which the profiling step should be run. The sample inputset must be large enough to enable the compiler to observe various pages, gather adequate access counts on them, and distinguish hot pages from cold ones by sorting them. To shed light on how large the inputset should be, we perform the following experiment: First, we use quite large inputsets6, such that simulating the on-chip cache hierarchy of applications to hot and transient pieces of data, we propose MemCache, a design that uses a part of the die-stacked DRAM as main memory and the rest as a cache. The software is responsible for filling the die-stacked memory with the identified hot pages. The transient pages are also served from the hardware-managed cache portion of the die-stacked DRAM. For every Last-Level SRAM Cache (LLSC) miss, if the miss address is mapped to the memory portion of the die-stacked DRAM, it is served by the die-stacked memory (i.e., without the overhead of tag-checking). Otherwise, it checks the DRAM cache tag array. In case of a cache hit, the request is served by the cache portion of the die-stacked DRAM, and in case of a cache miss, it proceeds to the off-chip memory.

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4.1 Memory Portion

The memory frames of the die-stacked DRAM should be filled with the hot pages of applications. First off, the hot pages of an application should be identified. We use a profiling approach in order to distinguish hot pages from cold ones. A software procedure, incorporated into the compiler, using profiling, determines which virtual pages of the application are hot. To do so, the software procedure sorts virtual pages based on their access count, in descending order, and then, conveys this information as clues to the page allocation unit of the OS.

There are quite a few ways to implement the profiling step needed in our mechanism, two of which are more common and are elaborated upon here. One approach is that the compiler profiles the program by simulating the behavior of the on-chip cache hierarchy of the target machine [27]. The simulation is used to gather the access counts of pages, which are then used to identify hot pages. Note that, such a profiling approach does not necessitate an accurate timing simulation of the processor and cache hierarchy; rather, it requires simply a trace-driven simulation of memory operations in order to gather information about accesses that are not captured in on-chip SRAM caches (i.e., LLSC misses and evictions). Another approach for implementing the profiling step is relying on hardware support. In this strategy, the target machine provides support for profiling operations (e.g., Informing Load Operations [37]). With this support, throughout the profiling run, the compiler gathers the access counts of application’s pages, and at the end, sorts them accordingly. In this paper, we use the first approach as it requires no change in the hardware.

Identifying hot pages by the compiler demands for a sample inputset on which the profiling step should be run. The sample inputset must be large enough to enable the compiler to observe various pages, gather adequate access counts on them, and distinguish hot pages from cold ones by sorting them. To shed light on how large the inputset should be, we perform the following experiment: First, we use quite large inputsets6, such that simulating the on-chip cache hierarchy on them, produces 10 B LLSC misses/evictions for each application. Based on these inputsets, we find the hottest pages of every application that fill a 4 GB memory. We refer to the set of these hot pages (identified by evaluating 10 B LLSC misses/evictions) as ideal pages. Then, we redo the same experiment based on just a part of the same inputsets, that results in 1 B LLSC misses/evictions for every application, and again identify the hottest pages that fill a 4 GB memory. Finally, we compare these hot pages with ideal pages and report the ratio of similar pages to all pages as the accuracy of page classification. We also repeat the same experiment based on 2 B, 3 B, . . . , and 9 B LLSC misses/evictions. Figure 5 shows how the accuracy of page classification varies with increasing the sample inputset size.

A critical observation we make here is that by observing a small fraction of the inputset, a static profile-based approach is able to classify pages accurately. This is especially true for modern throughput-oriented big-data graph applications. For example, in cc, classifying pages into hot and cold based on observing the first 1 B accesses yields 98% of the accuracy of an ideal classifier which is aware of the future and classifies pages based on the whole 10 B accesses7. On average across all applications, by observing only 1 B accesses, a profile-based approach is able to classify pages accurately, realizing roughly three-fourths of the accuracy of an ideal mechanism. Note that this fairly simple mechanism (i.e., profile-based classification of pages) works well mainly because of the fact that the size of the die-stacked DRAM is quite large. That is,

6 The details of applications and their inputsets are explained in Section 5.
7 Later in Section 6.1, we show that not only is such a page classification accurate, but it also produces robust results. That is, the pages that are classified as hot remain hot throughout the whole execution of an application.
the die-stacked DRAM is capacious enough to accommodate thousands and even millions of pages, and a few misclassifications do not have a significant effect on the overall accuracy. After detection of hot pages, their details are coded into the program binary. Whenever the program gets executed, the Loader passes the required information of hot pages to the OS. Then, the OS tries to map such hot pages to physical locations that belong to the memory portion of the die-stacked DRAM. For the OS, allocating pages in the die-stacked and off-chip memory is similar to the same operations in Non-Uniform Memory Architecture (NUMA) systems. Therefore, the OS, as well as system libraries, is able to use the same memory allocation algorithms for allocating pages in the die-stacked and off-chip memory. Furthermore, other operations, like virtual address translation and virtual memory management, for the die-stacked and off-chip memory are quite the same as in a NUMA system.

4.2 Cache Portion
The cache portion of the die-stacked DRAM filters requests to the pages that are allocated in the off-chip memory (i.e., pages that have not been identified as hot). The cache is transparent to the software and can be managed using any DRAM cache management technique. In this paper, we evaluate three cache architectures (Alloy CACHE [64], Unison CACHE [43], and Banshee CACHE [84]) for the cache portion of the MemCache.

4.3 Memory-Cache Capacity Partitioning
The optimal capacity of the die-stacked DRAM which can be turned into a part of the main memory directly depends on the applications. For applications with significant hot pages (e.g., pr), it is better to dedicate less space for the cache and more to memory. On the other hand, for applications with few hot pages (e.g., gems), partitioning the capacity towards more cache would be beneficial. However, dynamically changing the partition based on the running applications makes the system more complex, especially when the system is supposed to run multiple applications and frequently switch from one application to another.

In this paper, we consider two variants for MemCache; one design which its partitioning is tuned based on the application, and another which has fixed partitioning. In the first design, named MemCache-D, the compiler determines what fraction of the die-stacked DRAM capacity should be devoted to the memory and what fraction to the cache. To do so, the compiler runs Algorithm 1, thereby finding a fairly suitable partitioning. Then, the OS, using a specific instruction, announces the partitioning to the memory controllers. This way, the memory controllers become able to redirect requests to their correct locations. MemCache-D adapts itself based on the application behavior and is supposed to offer higher performance than a design that its partition is determined statically. However, it needs to change the partitioning for every application, which obviously is a costly operation, and may not be effective when the system runs multiple applications, frequently switching from one to another.

Therefore, we believe that MemCache-D is a suitable design for systems where a specific application (or a set of specific applications) runs for a long time (e.g., datacenter applications).

The other variant of MemCache we consider in this work is MemCache-S. In MemCache-S, a fixed fraction of the die-stacked DRAM is devoted to the memory and the rest to the cache. The partitioning is determined by the user, at boot time, and is then reported to the OS by the BIOS, along with other information. While a fixed partitioning might not give the best performance for all of the applications, it realizes a significant fraction of the performance benefit of dynamic application-based partitioning (i.e., MemCache-D). In this paper, we choose the capacity partitioning of MemCache-S based on the performance sensitivity analysis of all applications (Section 6.4) and show that such a static design offers a level of performance close to that of a design that picks the best memory-cache partitioning for each application.

The case where multiple applications share the processor, and the system frequently switches from one application to another, presents complications to MemCache and other hybrid memory systems where multiple dissimilar memories are used (e.g., DRAM+NVM systems where DRAM has characteristics entirely different from NVM, or even NUMA systems where accessing Local Memory has lower latency than Remote Memories). The problem arises from the fact that when the hot pages of an application (or set of applications) are being allocated in the die-stacked memory, information about the hot pages of other applications that

\[\text{As discussed in Section 3.3, in Algorithm 1, first a full-cache design is simulated. Then, the frames of the die-stacked DRAM are gradually turned into memory until the whole design becomes susceptible to fall behind a full-cache design.}\]

\[\text{By checking the physical address of a request and comparing it with the physical address of the last frame which has been devoted to memory, the memory controller decides whether to send the request to the memory portion of the die-stacked DRAM or serve it from the cache portion.}\]

\[\text{When the memory-cache partitioning of the die-stacked DRAM changes, not only is a system-wide TLB shootdown required, but also the valid data in the memory frames and modified data in the cache frames should be written back to the off-chip memory if the functionality of the frames changes.}\]

\[\text{In this paper, we evaluate this technique when multiple dissimilar applications co-run on the CMP.}\]
will possibly be running in the future is unknown; therefore, filling the die-stacked DRAM merely based on the current applications may result in suboptimal performance if future applications will be more bandwidth-hungry and require more capacity from the die-stacked DRAM. Various proposals (e.g., [13, 47, 54, 62, 78]) have suggested to optimize memory management in such situations typically by gradually or periodically migrating application pages between different types of memories based on factors like programming model, application’s criticality, sharing degree, and so on. Such approaches are orthogonal to MemCache and can augment it to provide performance/fairness benefits; however, we leave the analysis of enhancing our method with these techniques for future work, promoting a clearer understanding of our contribution in the context of prior die-stacked DRAM literature.

5 Methodology

We use ZSim [67] to simulate a system whose configuration is shown in Table 1. We model the system based on one Sub-NUMA Cluster (SNC) of Intel’s Knights Landing processor [74]. The chip has 16 OoO cores with an 8 MB LLC and a 4 GB die-stacked DRAM. One channel is used for accessing off-chip DRAM, providing a maximum bandwidth of 21 GB/s, and four channels are responsible for establishing communications with the die-stacked DRAM, providing up to 84 GB/s bandwidth. In comparison, Intel’s Knights Landing processor has four SNCs, offering 72 cores, 36 MB LLC (512 KB per core; 8 MB per 16 cores), 16 GB die-stacked DRAM (4 GB per SNCs), 90 GB/s off-chip peak bandwidth (1.25 GB/s per core; 20 GB/s per 16 cores), and up to 400 GB/s stacked bandwidth (5.5 GB/s per core; 88 GB/s per 16 cores). DRAM modules are modeled based on DDR3-1333 technology, parametrized with data borrowed from commercial device specifications [1]. Physical addresses are mapped to memory controllers at 4 KB granularity. The link width among memory controllers and die-stacked DRAM is 16 B, but the minimum data transfer size is 32 B [83, 84].

Table 1. Evaluation parameters.

| Parameter            | Value                                                                 |
|----------------------|----------------------------------------------------------------------|
| Cores                | Sixteen 4-wide OoO cores, 2.8 GHz                                    |
| L1-D/I               | 32 MB, 2-way, 1-cycle load-to-use                                     |
| L2 Cache             | 8 MB, 16-way, 15-cycle hit latency                                   |
| Die-Stacked DRAM     | 4 GB, 4 channels, 4 KB interleaved                                   |
| Off-Chip DRAM        | 1 channel, up to 21 GB/s bandwidth                                   |
| DRAM Modules         | 4 ranks/channel, 8 banks/rank, 16-byte bus width                     |
|                      | tCAS-tRCD-tRP-tRAS = 10-10-10-24                                     |

5.1 Workloads

Table 2 summarizes the key characteristics of our simulated workloads. We use all graph processing workloads from GAPBS [17] and run them with the Twitter inputset [48]. While the primary target of this work (and the systems that employ die-stacked DRAM) is throughput-oriented workloads like graph processing, yet for reference, we also include workloads from the SPEC [36] benchmark suite. We choose four SPEC benchmarks whose memory footprints exceed 4 GB and run them with the reference inputset in RATE mode (i.e., all sixteen cores run the same single-thread program). We also consider a mix of the four SPEC programs in which the processor executes four copies of each program.

5.2 Die-Stacked DRAM Organizations

We compare the following die-stacked DRAM organizations:

**Alloy Cache**: A state-of-the-art block-based cache design that uses a direct-mapped organization to minimize hit latency. Alloy Cache has a simple structure and was shown to be quite effective [64].

**Unison Cache**: A state-of-the-art page-based four-way set-associative cache design with LRU replacement policy that uses a footprint predictor [44] to reduce the off-chip bandwidth pressure. Moreover, it uses a way predictor to avoid the serialization latency of tag and data accesses. In this paper, in order to decouple the results of cache design from the accuracy of predictors, we use perfect predictors for fetching expected-to-use blocks and the cache way where the data is located at. For modeling a perfect footprint predictor, we follow a similar methodology as prior work [84]. We first profile applications offline and measure the average number of blocks that are used from cache pages (i.e., average footprint size). In timing simulations, whenever we want to bring a page into the die-stacked DRAM, we transfer as many cache blocks as the average footprint size of the application. However, unlike prior work [84], we consider an accurate 1-line granularity footprint predictor (instead of 4-line granularity).

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**Table 2. Application parameters.**

| Application | L2SC MPKI | Memory Footprint (GB) |
|-------------|-----------|-----------------------|
| GAPBS       |           |                       |
| bc          | 61.4      | 92.9                  |
| bfs         | 32.9      | 113.3                 |
| cc          | 85.6      | 9.6                   |
| pr          | 129.9     | 76.5                  |
| sssp        | 73.4      | 140.1                 |
| tc          | 12.5      | 53.4                  |
| SPEC        |           |                       |
| bwaves      | 17.6      | 13.1                  |
| gems        | 26.7      | 12.6                  |
| mcf         | 66.9      | 26.1                  |
| milc        | 17.0      | 10.2                  |
| mix         | 17.8      | 13.4                  |
**Banshee Cache:** A state-of-the-art page-based four-way set-associative cache design that tracks the tags of cache-resident pages in the Page Table and Tag Buffer. We consider a 1K-entry 8-way associative Tag Buffer (5.5 KB of SRAM storage) and set the baseline sampling coefficient to 10% based on the original proposal [84]. Whenever the occupancy of the Tag Buffer exceeds 70%, it should be flushed to the Page Table (and TLBs) to make all information coherent. We consider 25 μs latency for the software procedure that updates the Page Table and shoots down TLBs based on the original proposal.

**HMA:** The whole die-stacked DRAM is used as a part of main memory. Upon every $10^6$ LLC misses, a software procedure swaps the pages between the die-stacked and off-chip DRAM to have currently-used pages in the high-bandwidth memory. For every page in the system, we consider a counter that counts the number of accesses to that page. Upon each OS interval, we precisely sort the pages and allocate highly-used ones in the high-bandwidth memory.

By accurately modeling the bandwidth of page swapping, we observed that the performance (IPC) of this technique consistently drops to zero in all workloads because of the massive bandwidth overhead. The simulated workloads already utilize the bandwidth of both die-stacked and off-chip DRAM, and hence, there is not much unused bandwidth left for swapping numerous large pages on each interval. Increasing the page swapping period (e.g., once every 10 seconds) may amortize the associated bandwidth overhead, but doing so will further reduce the ability of this technique to respond to the dynamic changes in the memory access behavior of applications (i.e., transient datasets). In this paper, we model an idealized case, in which, page swapping consumes no bandwidth and happens instantaneously with no latency.

**MemCache-S:** Based on the performance sensitivity analysis (see Section 6.4), 3 GB of the die-stacked DRAM is used as a part of main memory, and the remaining 1 GB operates as a cache. Software allocates the identified hot pages in the memory portion of the die-stacked DRAM based on the warm-up instructions (i.e., the instructions and the part of inputset which are used for identifying hot pages and filling the die-stacked memory are not used/collected in the actual experiments). Without loss of generality, we consider a Banshee Cache architecture for the cache portion of the die-stacked DRAM. In Section 6.5, we evaluate other cache architectures for the cache portion of MemCache, as well.

**MemCache-D:** For every application, the memory-cache capacity partitioning is determined using Algorithm 1. The other specifications are the same as MemCache-S.

**INFINITE:** Die-stacked DRAM has infinite size and is used as a memory to host the whole datasets of applications.

## 5.3 Simulation Parameters

For trace-driven experiments, we gather 16 billion LLC misses, using the first 2 billion for warm-up and the rest for measurements. For timing analysis, we run the simulations for 200 billion instructions and use the first 20 billion for warm-up and the next 180 billion for measurements. We ensure that after the warm-up period, the die-stacked DRAM has become well-filled (i.e., no empty frame has remained), and the statistics are in the steady state.

## 6 Evaluation

### 6.1 Performance

Figure 6 shows the performance of all designs, normalized to a system without die-stacked DRAM. Moreover, solid dots in the figure indicate Misses Per Kilo Instructions (MPKI) of the competing designs. On average, MemCache-S/D offer 107%/114% performance improvement, which is 21%/28% higher than Banshee Cache, the best-performing prior proposal.

Unison Cache improves the performance by 12% on average and has the lowest performance enhancement among the evaluated designs. While it offers a high hit ratio (thanks to the page-based organization and ideal footprint predictor), it suffers from inefficiencies in utilizing the die-stacked DRAM.
DRAM bandwidth, as we show in Section 6.2. Due to frequent replacements of large pages and checking/updating the tags, a significant bandwidth overhead is imposed on the die-stacked DRAM, preventing it from offering considerable performance improvement.

As compared to Unison Cache, Alloy Cache has better performance improvement (38% on average), mainly because of imposing less bandwidth pressure on the die-stacked DRAM. Alloy Cache caches data at block granularity, and hence, consumes less bandwidth upon replacements. Moreover, it uses a direct-mapped organization which frees it from the tag-updating bandwidth (e.g., LRU bits). However, Alloy Cache still consumes significant bandwidth for probing the tag and speculatively loading data, as we show in Section 6.2. For minimizing hit latency, Alloy Cache co-locates tag and data adjacently and streams them out in a single access. Whenever a request hits in the DRAM cache, the latency of accessing data is a single DRAM access, but extra bandwidth is consumed for loading the tag. In case of a cache miss, not only the tag but also the speculatively-loaded data impose bandwidth overhead. Another drawback of Alloy Cache is its relatively high MPKI. Caching data at block granularity and employing a direct-mapped organization synergistically decrease the cache hit ratio because of not exploiting the spatial locality and the increased conflict misses.

HMA has no tag overhead but suffers extensively from the low hit ratio of the die-stacked DRAM. As the periods of page swapping (OS intervals) are too long, the technique is unable to serve requests to transient datasets. Therefore, requests to data objects that are highly utilized for only a short period of time are served from the bandwidth-limited off-chip memory. We emphasize that reducing the period of OS intervals is not feasible because of the colossal associated latency and the bandwidth overhead of swapping numerous large pages.

Banshee Cache tracks tags of cache-resident pages through TLBs and hence eliminates the latency of tag-checking. Moreover, its bandwidth-aware replacement policy significantly reduces the frequency of replacements, resulting in less bandwidth pressure on the die-stacked and off-chip DRAM. However, its performance is far from that of Infinite. Lazily replacing pages performed by the bandwidth-aware replacement policy of Banshee Cache reduces the hit ratio, resulting in serving more requests from the bandwidth-limited off-chip memory. Moreover, in order to reach the metadata of pages (e.g., tag and counter) that are stored in the die-stacked DRAM, Banshee Cache consumes considerable bandwidth, which prevents it from reaching the peak performance. Finally, costly software interrupts that read and flush the Tag Buffer entries to the Page Table and TLBs take significant system cycles (each accounts for tens of kilo-cycles), resulting in performance degradation.

The performance improvement of MemCache-S/D ranges from 18%/19% to 294%/310% with an average of 107%/114%. Compared to Banshee Cache, the best-performing previous proposal, MemCache-S/D improves the performance by 21%/28% on average and up to 85%/138%. The performance improvement is more evident in bandwidth-hungry throughput-oriented applications (e.g., pr). The performance improvement of MemCache-S/D over Banshee Cache comes from:

1. MemCache-S/D mitigates wrong replacement decisions made by Banshee Cache (i.e., not caching pages\textsuperscript{16}). Therefore, it reduces both miss ratio and off-chip bandwidth of Banshee Cache. On average, MemCache-S/D reduces the MPKI of Banshee Cache by 8%/15% and up to 36%/45%. Moreover, it reduces the off-chip bandwidth by 22%/27%, on average, and up to 56%/59%.

2. MemCache reduces the bandwidth pressure of the die-stacked DRAM that is imposed because of accessing metadata in Banshee Cache for either replacement or tag-probing. It comes from the fact that, a significant fraction of requests is served from the memory portion of the die-stacked DRAM, for which, no metadata bandwidth is consumed. On average, MemCache-S/D consumes 13%/15% less stacked bandwidth (up to 31%/30%) as compared to Banshee Cache.

3. The number of costly software interrupts is reduced with MemCache, as compared to Banshee Cache. The main reason is that, with serving a significant fraction of requests from the memory portion of the die-stacked DRAM, there is a lighter load on the Tag Buffer, and hence, it is filled up more slowly. MemCache-S/D reduces the number of Tag Buffer flushes by 78%/87% on average and up to 94%/99%.

MemCache-D offers higher performance as compared to MemCache-S. MemCache-D outperforms MemCache-S by 7% on average and up to 84%, mainly because of more intelligent partitioning of the die-stacked DRAM capacity. However, in few cases, the performance improvement of MemCache-D is slightly less (up to 2%) than that of MemCache-S. It is because we partition the die-stacked DRAM capacity (i.e., Algorithm 1) towards memory, conservatively. That is, we dedicate frames to the memory as much as the whole design (i.e., the composition of memory and cache) becomes susceptible to fall behind the full-cache design. However, as discussed in Section 3.2, since the memory

\textsuperscript{16}Banshee Cache caches a page only if, intuitively, the page is identified hotter than other pages resident on the same set. This is problematic when more than four hot pages are mapped to the same set, preventing having all many of them in the high-bandwidth DRAM. Increasing the associativity may mitigate this problem, but will exacerbate the bandwidth pressure on the die-stacked DRAM as more bytes need to be transferred upon each metadata access. MemCache virtually eliminates this problem by allocating hot pages in the memory portion of the die-stacked DRAM.
has better latency/bandwidth characterizations as compared to the cache, the optimal point in capacity partitioning might be where the memory fraction is slightly higher than what Algorithm 1 determines. One solution may be enhancing the offline partitioning algorithm by considering factors other than hit ratio, such as bandwidth and/or latency. However, doing so adds complications to the offline process since the compiler should run a timing simulation rather than simply a trace-driven simulation. We conclude that the minor performance improvement does not justify this increased complexity.

Impractical INFINITE has the highest average performance improvement. INFINITE improves the performance by 149% on average and up to 275%. However, in several cases (e.g., cc, pr, sssp, and mcf), its performance is less than that of MemCache-S/D (in mcf also less than HMA). This is because, with INFINITE, applications benefit only from the bandwidth of the die-stacked DRAM and not the off-chip DRAM. Therefore, with INFINITE, the total bandwidth available to applications is less than other approaches in which the bandwidth of both die-stacked and off-chip DRAM are available.

6.2 Die-Stacked DRAM Traffic

As throughput-oriented applications (like graph processing) are able to utilize the bandwidth of die-stacked DRAM, managing die-stacked DRAM in a bandwidth-efficient manner is crucial for reaching the peak performance.

Figure 7 shows the breakdown of die-stacked DRAM traffic for the competing designs. We use Bytes Per Instruction [84] as the metric for bandwidth intensity of applications. The breakdown consists of Data, Metadata, Spec. Data, and Replacement. Data refers to the traffic that is used for reading and updating data in the die-stacked DRAM. Metadata includes the bandwidth consumed for reading/updating tag and replacement metadata (e.g., LRU bits). Spec. Data corresponds to the traffic that is imposed to speculatively load and replace cache blocks/pages.

HMA has the lowest traffic as it touches the die-stacked DRAM only for data. Alloy Cache and Unison Cache impose an order of magnitude higher traffic to the die-stacked DRAM, mainly because of metadata accesses. The metadata traffic is higher in Unison Cache because it employs a set-associative structure and is required to update metadata information upon each access. Banshee Cache has lower bandwidth pressure because it has fewer metadata accesses and lazily replaces pages in the die-stacked DRAM. Meanwhile, it has higher bandwidth usage as compared to MemCache. By serving a significant fraction of requests from the memory portion of the die-stacked DRAM, MemCache-S/D reduces the die-stacked bandwidth usage of

\[\text{Figure 7. The breakdown of die-stacked DRAM traffic.}\]

\[\text{Figure 8. Off-chip DRAM traffic of evaluated designs.}\]
Banshee Cache by 13%/15%. The reduction mainly comes from the cut down on metadata and replacement traffic.

6.3 Off-Chip DRAM Traffic

Figure 8 shows the traffic of the off-chip DRAM for the evaluated designs. Off-chip DRAM traffic is more important than that of the die-stacked DRAM because more gap between the bandwidth of die-stacked and off-chip DRAM is expected with the future technologies [77].

HMA has the highest traffic because of its lower hit ratio. As discussed previously, HMA is unable to capture the dynamic behavior of applications, due to its long OS intervals. Therefore, in this technique, virtually all requests to transient data objects are served from the off-chip DRAM, imposing a significant bandwidth overhead. Unison Cache and Alloy Cache impose traffic on the off-chip DRAM due to cache misses and dirty writebacks. Banshee Cache has a less off-chip bandwidth, as compared to Unison Cache and Alloy Cache, because it has fewer replacements. MemCache has the lowest off-chip bandwidth among the evaluated designs. The bandwidth reduction of MemCache-S/D over Banshee Cache is 22%/27% (up to 56%/59%) and comes from mitigating wrong replacement decisions made by Banshee Cache, resulting in higher hit ratio of the die-stacked DRAM.

6.4 Sensitivity to Memory-Cache Capacity Partitioning

The optimal capacity partitioning between the cache and memory in the die-stacked DRAM depends on the applications. Figure 9 shows the performance and MPKI of MemCache-S as the fraction of memory varies. Applications that have many hot pages (e.g., pr) favor dedicating smaller capacity to the cache and larger to the memory. On the other hand, for applications with significant transient pages (e.g., gems), partitioning the capacity towards more cache is beneficial. Among the different partitionings, the design which devotes 3 GB to memory and 1 GB to cache offers the highest average performance; consequently, we choose this partitioning for the MemCache-S. We note that on average, cache design (i.e., 0/4) performs better than full-memory design (i.e., 4/0). This confirms that due to the mismatch between the dataset size and die-stacked DRAM capacity, full-memory is suboptimal to full-cache designs. However, in few cases and despite the fact that full-memory design has higher MPKI than the cache design, its performance is slightly better. This is due to the fact that a full-memory design completely eliminates the whole overhead associated with the evaluated cache scheme (i.e., Banshee Cache): no metadata overhead, no replacement, and no expensive software interrupt.

An interesting data point is that, for applications that largely benefit from the die-stacked DRAM technology (i.e., the performance gets more than doubled), it is beneficial to dedicate more capacity to memory and less to cache. This is the main reason why the design that uses three-fourths of the die-stacked DRAM as memory offers a significant performance improvement of the dynamically-partitioned design. Modern big-data throughput-oriented applications (e.g., most of the graph-processing applications in our suite) have a significant number of hot pages (cf. Section 3.1) which can be hosted in the memory portion of the die-stacked DRAM, enabling better usage of the die-stacked DRAM technology, and hence higher performance improvement.

6.5 The Architecture of the Cache Portion

The results reported for MemCache are obtained for a design where the cache part is organized as a Banshee Cache as it offers the highest performance. In this section, we evaluate other architectures for the cache portion of the die-stacked DRAM. Figure 10 shows the performance of MemCache with various cache designs, as compared to the performance of the corresponding cache design. MemCache-S with Alloy Cache/Unison Cache/Banshee Cache improves performance by 13%/9%/21% over the corresponding cache design. Furthermore, MemCache-D with Alloy Cache/Unison Cache/Banshee Cache enhances

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**Figure 9.** The sensitivity of performance (bars) and MPKI (solid dots) to memory-cache capacity partitioning. Performance is normalized to a baseline without die-stacked DRAM. X/Y represents a design that dedicates X GB to memory and Y GB to cache.
the performance of the corresponding cache design by 26%/25%/28%. The performance improvement of MemCache-S/D with Alloy Cache as compared to the full-cache design is 13%/26% on average and up to 45%/103%. The performance improvement comes from: (1) 18%/38% lower MPKI, (2) 16%/27% less die-stacked DRAM bandwidth usage, and (3) 17%/36% lower traffic on the off-chip DRAM. MemCache-S/D with Unison Cache improves performance by 9%/25% on average and up to 66%/174% over the full-cache design. The performance enhancement comes from: (1) 8%/49% MPKI reduction, (2) 18%/35% less bandwidth pressure on the die-stacked DRAM, and (3) 5%/33% lower off-chip DRAM traffic.

The results indicate that MemCache is not limited to a specific cache design and can be used with other cache organizations, as well. Moreover, even with MemCache, the performance is significantly affected by the cache architecture. Since most of the bottlenecks on the road to achieve the peak performance are cache-induced (e.g., tag-checking bandwidth and limited associativity), and not memory-induced, the architecture of the cache portion has a decisive role in the overall performance.

6.6 How Long are the Pages Hot?

We fill the memory part of MemCache with hot pages that are distinguished at compile time. Any static and profile-based approach has the risk that its results become stale over time. Here, we measure the fraction of the requests that are served from the memory part, as time spent from the point where timing simulations have finished. Figure 11 shows how this fraction changes over 100 seconds for 3 GB of the hottest pages (i.e., MemCache-S). As shown, except for one workload (i.e., tc), the metric remains steady. The results indicate that:

1. Hot pages stem fundamentally from the data access patterns of applications and stay hot throughout the whole execution.
2. A static compile-time analysis with a representative input-set is able to easily detect hot pages in the context of a giga-scale die-stacked DRAM.

The tc application exhibits significant dynamic data-dependent behavior (cf. Figure 3) that results in a sharp drop in the reuse of pages that are classified as hot at the beginning of the execution. One solution for such workloads is to dynamically re-identify and swap pages between die-stacked and off-chip memories, just like prior work [26, 60, 68]. Note that, even for such applications, as a part of the die-stacked DRAM in MemCache is managed as a cache, it quickly responds to the dynamic changes of applications. Therefore, there is room for significantly increasing the period of OS interventions (e.g., once every 100 seconds), in order to amortize the high latency/bandwidth overhead. Evaluating such ideas is beyond the reach of architectural simulators, and hence, we leave them for future work.

6.7 Sensitivity to Inputset

To evaluate the impact of inputset on the effectiveness of MemCache, we consider two other inputsets (i.e., Web [25] and Urand [29]) for GAPBS applications18 and compare the results with those of the so-far–evaluated Twitter inputset [48]. Table 3 summarizes the key characteristics of applications when they run these inputsets. Corroborating the characterization study performed by Beamer et al. [17], Web graphs, despite the large size, exhibit substantial locality owing to their topology and high average degree [25]. Synthetically-generated Urand graphs, on the other hand, manifest the worst-case locality as every vertex in the graph has equal probability to be a neighbor of every other vertex [29]. Twitter graphs, as they come from real-world data, have characteristics that lie in between Web and Urand.

18We do not perform a similar experiment for SPEC programs since other standard inputsets of SPEC applications are unable to fill the capacity of the die-stacked DRAM in a reasonable simulation time.
Table 3. LLSC MPKI and memory footprint of evaluated graph-processing applications when they use different inputsets.

| Application | Twitter | Web | Urand | Twitter | Web | Urand |
|-------------|---------|-----|-------|---------|-----|-------|
| bc          | 61.4    | 10.2| 71.3  | 92.9    | 107.9| 304.4 |
| bfs         | 32.9    | 8.6 | 58.4  | 113.3   | 68.6 | 234.8 |
| cc          | 85.6    | 8.2 | 98.7  | 9.6     | 9.2  | 25.0  |
| pr          | 129.9   | 19.2| 179.1 | 76.5    | 216.9| 102.6 |
| sssp        | 73.4    | 23.8| 98.2  | 140.1   | 94.9 | 496.0 |
| tc          | 12.5    | 2.9 | 16.2  | 33.4    | 21.5 | 256.2 |

Figure 12. Sensitivity of performance improvement of various die-stacked DRAM organizations to inputset.

Figure 12 shows the average performance improvement of die-stacked DRAM organizations when the applications use different inputsets. On average, with the Twitter/Web/Urabd inputset, MemCache-S outperforms the best of cache and memory by 21%/6%/10%. MemCache-D also outperforms MemCache-S by 7%/9%/6%. While considerable, the performance improvement with Web and Urabd inputsets is less than the improvement with the Twitter inputset. The improvement with Web is relatively low because most of the accesses hit in SRAM caches due to the high locality of graphs (cf. Table 3), reducing the bandwidth requirements of applications, and hence, downplaying the effect of bandwidth-improvement techniques. The lack of a considerable locality in Urabd graphs, on the other face of the coin, defeat the caching and hot-page–detection policies used in the die-stacked DRAM organizations, giving rise to less performance improvement with these approaches. By and large, with all inputsets, MemCache-S/D consistently outperform both cache and memory designs, reinforcing our stance that using the die-stacked DRAM, partly as main memory and partly as cache, is the right design choice for modern throughput-oriented big-data applications.

6.8 Sensitivity to Die-Stacked DRAM Size

Figure 13 shows the performance improvement of various methods with different die-stacked DRAM sizes. The figure shows that regardless of the die-stacked DRAM capacity, the hybrid design (i.e., MemCache) outperforms both cache and memory, because of simultaneously reaping the benefits of both cache and memory. More to the point, with increasing the size of the die-stacked DRAM, the fraction of capacity that should be devoted to the memory in order to gain higher performance also increases. With increasing die-stacked DRAM capacity, the number of identified/allocation hot pages (cf. Section 3.3) and the accuracy of offline page classification (cf. Section 4.1) increase, giving rise to increasing the memory fraction of optimal design.

7 Related Work

To the best of our knowledge, this is the first research that proposes to use the die-stacked DRAM partly as main memory and partly as a cache. Nevertheless, MemCache, in the sprite, is similar to Hybrid configuration of Multi-Channel DRAM (MCDRAM) modules in Intel’s Knights Landing processor [74]. In MCDRAM modules of Knights Landing processor, similar to MemCache-S, a fixed portion of the die-stacked DRAM is devoted to memory, and the rest acts as a cache. The programmer is responsible for allocating data structures in the memory portion of MCDRAM modules, using high-level instructions like hbw_malloc and FASTMEM. In this paper, we showed that such a heavy burden on the programmer could be lifted with compile-time page classification. We showed that the large capacity of the die-stacked DRAM paves the way for offloading the hot-pages–identification task to the compiler, providing programming ease (cf. Section 4.1). Moreover, we signified the potentials for dynamism in partitioning the capacity of the die-stacked DRAM, showing that the dynamic partitioning is able to outperform the static one by as much as 84% (cf. Section 6.1).

Some pieces of prior work [12, 58, 61] also proposed to profile applications and manage the die-stacked DRAM based
on the outcome. However, all of these approaches use the die-stacked DRAM entirely as a part of main memory and neither proposed nor discussed a design that uses the die-stacked DRAM partly as main memory and partly as a cache.

Chou et al. [22] proposed Cameo to minimize the number of accesses to the backend storage (e.g., SSD or Disk). Cameo manages die-stacked and off-chip DRAM in different address spaces to increase the physical address space of the system while attempting to preserve the benefits of caching via keeping recently-accessed data in the high-bandwidth DRAM. MemCache, however, uses a part of the die-stacked DRAM as the main memory to enable efficient access to hot data structures without the overhead of tag-checking. MemCache is distinct from Cameo but brings most of its benefits for free. Yet, Cameo is orthogonal to MemCache since the cache part of the die-stacked DRAM in MemCache can be managed like Cameo.

Tertiary Caching was proposed in the context of multi-socket systems. In Tertiary Caching [76, 85], a portion of each node’s local memory is managed as a cache for caching only data objects that are allocated in remote nodes. While there are similarities between MemCache and Tertiary Caching, they are conceptually different. In MemCache, the memory part is used for keeping only hot pages, while in Tertiary Caching, memory hosts all local pages. Besides, MemCache uses the cache for the transient datasets of applications, while Tertiary Caching dedicates a part of memory to the cache in order to cache only remotely-allocated data objects.

In addition to schemes thoroughly discussed in Section 2, there are other proposals for managing the die-stacked DRAM as a cache. Loh and Hill [57] suggested a set-associative DRM cache in which the tags and data of each set fit in a single DRAM row, allowing it to serve cache hits without the need to open more than one DRAM row. Jiang et al. [45] proposed Chop, a design that caches only pages with high expected reuse to avoid the significant bandwidth overhead of page-based caches. Loh [56] proposed organizing each DRAM cache set as a multi-level queue to evict dead-on-arrival cache lines immediately after insertion. Guler et al. [33] proposed Bi-Modal DRAM Cache to obtain the advantages of both block-based and page-based caches via dynamically choosing the caching granularity. Sim et al. [69] proposed techniques that enable accessing off-chip DRAM when the die-stacked DRAM cache bandwidth is highly utilized. In this paper, we showed that a large DRAM cache is suboptimal to a design that uses both cache and memory at the same time.

Numerous strategies were proposed to improve the efficiency of die-stacked DRAM. DAP [32] and Batman [21] attempt to maximize the total bandwidth utilization of systems with both die-stacked and DIMM-based DRAM modules. These approaches forbid data movement from the off-chip DRAM to the die-stacked DRAM when the bandwidth usage of the die-stacked DRAM exceeds a certain threshold to efficiently exploit the available bandwidth of both DRAM components. Freney and Lipasti [31] proposed Tag Tables, a technique for compressing the tag array of DRAM caches to enable fabricating it in SRAM. Accord [81] provides associativity for direct-mapped Alloy Cache using way-prediction and way-install. Chou et al. [23] suggested Bear for reducing the bandwidth pressure of die-stacked DRAM caches. Bear decreases the tag-checking bandwidth by maintaining certain status details of the DRAM cache in the active die. Moreover, it samples replacement decisions, effectively trading hit ratio for bandwidth efficiency. Young et al. [82] introduced DICE, a technique for compressing DRAM caches mainly for reducing bandwidth usage and then for having a higher effective capacity. DICE attempts to get multiple useful blocks in a single DRAM access by compressing data and adaptively adjusting the set-indexing scheme of the cache. Huang and Nagarajan [39] proposed ATCache to provide faster access to the tag array of a DRAM cache. ATCache exploits the empirically-observed spatio-temporal locality in tag accesses and caches/prefetches some tags of the die-stacked DRAM in an SRAM structure. Candy [24] and C^D [38] facilitate the use of DRAM caches in the context of multi-node systems by making them coherent. Most of these approaches are orthogonal to our work and can be used together.

8 Conclusion
Die-stacked DRAM has shown the potential to break the bandwidth wall. The research community has evaluated two extreme use cases of the die-stacked DRAM: (1) as a sizable memory-side cache, and (2) as a part of software-visible main memory. In this work, we showed that both designs are sub-optimal to a scheme that uses the die-stacked DRAM partly as main memory and partly as a cache. By analyzing the access behavior of various big-data applications, we observed that there are many hot pages with a significant number of accesses. We proposed MemCache, an approach that uses a portion of the die-stacked DRAM as the main memory for hosting hot pages and the rest as a cache for capturing the dynamic behavior of applications.

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