Performance Evaluation of Sequential Adder using Neural Networks

K. Kiron, B. Srinath, Pochamreddy Satishwar Reddy and Husnul Budhiraja

Department of ECE, SRM University, Kattankulathur, Kancheepuram, Chennai – 603203, India; nonpareil.kiron@gmail.com, bsrinath86@gmail.com, satishwarreddy.pocham@gmail.com, husnulbudhiraja@yahoo.com

Abstract
Objectives: Power consumption in digital systems is a crucial issue with the greater emphasis on nano-scaled technologies. Power consumption is greatly curbed by reducing the voltage levels. However, this compromises the circuit delay. Also, by decreasing the voltage level, circuit delay rises exponentially and hence there is an increase in static energy consumption. Methods/Statistical Analysis: In this paper, adders are the architectures chosen for optimization due to the fact that in most of the modern digital systems, the maximum operating speed depends on how fast adders can process the data. This, in turn, is responsible for setting the minimum clock cycle time in processors. The primary focus of this paper is to reduce the delay of Serial Full Adder (SFA), a sequential adder. The delay, power, and area of six different 16-bit adders are examined and compared with respect to their structure and logic depth. This paper presents optimized architectures for 32-bit and 64-bit SFA which operates with less delay and occupies less area by using massively parallel structures. Introducing the concept of neural networks helps us to formulate a power estimation method for adder architectures in SOC Using supervised learning method in Feed Forward Back Propagation Network, the estimated dynamic, leakage and total power is obtained for SFA for any desired input voltage. Findings: The experimental results shows that proposed SFA provides better results with power and delay as metric. The convergence of the proposed estimation method based on neural networks is faster due to its learning and training. Application/Improvements: This method can be extended to estimate the power of any adder architecture and using any other neural network.

Keywords: Adder Architecture, Power Consumption, Neural Networks, VLSI Power Estimation Method.

1. Introduction
VLSI implies miniaturization. The need of the hour is to ensure maximum possible efficiency in minimum possible area coupled with minimum power consumption and delay. Adders have been chosen for optimization as addition forms the most fundamental operation in any modern digital system. The major problem with binary addition is the propagation delay in the carry chain. We know that

\[ P = 0.5 \cdot CV^2 \]  

(1)

Where, \( P \) is power in Watts, \( C \) is capacitance in Farad and \( V \) is voltage in Volts.

From the above equation, it can be said that in sub-threshold region, both static and dynamic elements of power consumption are reduced considerably because of lower supply voltage. Circuit delay grows exponentially with descending voltage level and consequently, there is an increase in the static energy consumption. This is the problem being addressed in this paper.

The existing system comprises five combinational and one sequential adder. Some of these combinational adders have greater area, greater delay, greater fan-out or higher power consumption. Hence, SFA is designed. The architecture for SFA proposed in this paper aims at reducing the power-delay product and computes results for larger number of bits in smaller number of clock cycles.

*Author for correspondence
2.2 Feed Forward Back Propagation Network

It is a multi-layered forward network using the rule of back propagation of errors. It prunes the total squared error of the output computed. The network is trained by supervised learning method. The objective is to train the network to establish a balance between the ability to respond correctly to input patterns that are used for training and also, the ability to provide good responses to similar inputs.

2.3 Power Estimation using Neural Networks

The ‘ntool’ is invoked in MATLAB to formulate a power estimation method based on the neural network approach. In this tool, the gate count, voltage and temperature are given as inputs and subsequently, dynamic, leakage and total power of the adders obtained after physical design in Cadence are given as the targets. The input data and the target data are to be given as matrix of the same size. Now, the selected network is trained with the given input and target data. After training the Feed Forward Back Propagation Network, the desired voltage is given as a third input during simulation for the trained network. The network estimates the dynamic, leakage and total power to be expected for the given voltage when simulated in real-time.

3. Serial Full Adder

The Serial Full Adder in Figure 1 is a sequential digital circuit that performs bit-wise binary addition. The SFA consists of three single-bit inputs, i.e. the numbers to be added and the carry in. It produces two single-bit outputs, one for the sum and the other for carry out. The previously calculated carry-out signal forms the carry-in signal. In each clock cycle, addition is performed bitwise, lowest to highest. SFA has three components, a full adder combined with a 2:1 multiplexer and a D-flip flop to use the adder unit at different clock cycles in a time-serialized ripple-carry manner. The number of clock cycles equals to the number of bits.

3.1 Comparison with Serial Processing

1. On comparing serial processing with parallel processing, it can be concluded that the series circuits are...
4.2 Design of 32-Bit SFA

In the design shown in Figure 2 the input, which is of 32-bits, is divided into two parts, which are of 16-bits each. Except for the initial 16 bits (a[15:0], b[15:0]), the remaining sub-parts of the two inputs are given to the two SFAs which are in the same column. The rightmost SFA and the SFAs which are in the top row are given input carry as ‘0’ while the SFAs in the bottom row are given the input carry as ‘1’. Usually, a 32 bit normal SFA takes 32 clock cycles to add two 32 bit inputs but by using the above architecture, the computation can be completed in 16 clock cycles. In 16 clock cycles, all the SFAs complete their addition operation. If the output carry of the rightmost SFA is ‘1’, then the bottom SFA becomes a part of the output. If the output carry of the rightmost SFA is ‘0’, then the SFA module in the top row is selected and its respective result is taken as a part of the 32-bit addition output. This is repeated with the other modules.

4.3 Design of 64-Bit SFA

In the design in Figure 3 the input, which is of 64-bits, is divided into 4 sub-parts of 16-bit each. Except for the
initial 16-bits \((a_{15:0}, b_{15:0})\), the remaining sub-parts of the two inputs are given to two SFAs which are in the same column. The rightmost SFA and the SFAs which are in the top row are given input carry as ‘0’ while the SFAs in the bottom row are given the input carry as ‘1’. Usually, a 64-bit SFA takes 64 clock cycles to add two 64 bit inputs. However, by using the above architecture, the addition can be performed in 16 clock cycles. In 16 clock cycles, all the SFAs complete their addition operation. If the output carry of the rightmost SFA is ‘1’, then the bottom SFA becomes a part of the output. If the output carry of the rightmost SFA is ‘0’, then the SFA module in the top row is selected and its respective result is taken as a part of the 64-bit addition. This is repeated with the other modules. This operation can be extended for n-bit addition. The simulation result is shown in Figure 4.

5. Results and Discussion

Following Verilog Design and Simulation, physical design was done for the adders using Cadence Digital Encounter. Power and area reports were taken both before physical design and after physical design shown in Figure 5. The gate count, power and area reports were taken for two voltages, 0.9V and 1.62V, post generation of net list and constraint files for each adder. Power estimation by feed forward back prop network: 22.43% from Figure 6 and Figure 7.

Figure 4. RCA Layout.

Figure 5. Simulation Result for 16-bit SFA.

Figure 6. Regression Analysis.

Figure 7. Comparison of Power Delay Product of Adders.
11.408ns and 15.321ns respectively. Hence, optimization of the existing SFA architecture is achieved using the concept of parallelism. The proposed delay-optimized parallel architecture of SFA can be employed to create an n-bit adder which can perform addition operation in smaller number of clock cycles. Lastly, neural network based approach to power estimation is employed which estimates power with about 22 percent tolerance. Estimation of power is important because the generated estimation allows the user to have a rough approximate of the power to be expected during real time simulation. The neural network based approach for power estimation can be done using other neural networks and extended to other architectures.

6. Power Estimation of SFA using Neural Networks

The concept of neural networks is employed to formulate a power estimation method for adder architectures in SOC. Using supervised learning in Feed Forward Back Propagation Network and Elman Back Propagation Network, the estimated dynamic, leakage and total power is obtained for SFA for any desired input voltage. This method can be extended to estimate the power of any adder architecture. Neural network tool of the MATLAB is used for power estimation of the different adders at different PVT values.

The first step is to train a neural network to make it familiar with the environment. A trained neural network can be thought of as an “expert” in the category of information it has been given to analyse. This “expert” can then be used to provide projections given new situations of interest and answer “what if” questions. Figure 8 shows regression test after results after the network is trained. It is observed the linear regression is obtained to show that the network is trained well for given value of input vectors.

7. Conclusion

Following logic design, simulation, physical design and comparison, it is proved that 16-bit SFA has the lowest delay when compared with its 16-bit combinational adder counterparts. Also, it is noted that the power decreases after physical design as compared to the power value before physical design. The total power consumed by the SFA can be reduced by replacing the D-flip flop with a latch. This can reduce the power to a greater extent while using the SFA modules in parallelism. However, in ASIC, there is always trade off between delay and area. Smaller delay entails greater area and vice-versa. Hence, a separate architecture is proposed for SFA which reduces the effective area. The proposed paralleled SFA architectures perform 32-bit and 64-bit computation with small delay of

8. References

1. Thakur A, Chilamakuri D, Velenis D. Effects of process and environmental variations on adder architectures 49th IEEE International Midwest Symposium on Circuits and Systems. 2006 Aug. p. 36–40.
2. Liu F, et al. A comparative study of parallel prefix adders in FPGA implementation of EAC. 12th. Euromicro Conference on Digital System Design, Architectures, Methods and Tool; Patras; 2009 Aug. p. 281–6.
3. Islam A, Imran A, Hasan M. Robust subthreshold full adder design technique. International Conference on Multimedia, Signal Processing and Communication Technologies (IMPACT); Aligarh; 2011 Dec. p. 99–102.
4. Dorosti H, Teymouri A, Fakhraie SM, Salehi ME. Ultra low-energy variation-aware design: Adder architecture study. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 2016 Mar; 24(3): 1165–68.
5. John, Talsania M, Eugene. A comparative analysis of parallel prefix adders, Scientific Publications of the State University of Novi Pazar. 2013. p. 29–36.
6. Bekakos MP, Milovanovic IZ, Toki CTI, Doli Canin CB, Milovanoci EVI. Selecting mathematical method for systolic processing, Scientific Publications of the State University of Novi Pazar. 2011. p. 53–8.
7. John, Talsania M, Eugene. A comparative analysis of parallel prefix adders, Scientific Publications of the State University of Novi Pazar. 2013. p. 29–36.
8. Weste DH. CMOS VLSI Design: A Circuits and Systems Perspective. Fourth Edition. New York: Pearson; 2010, p. 1–867.
9. Deepa SN, Sivanandam SN. Introduction to Neural Networks using Matlab 6.0. First Edition. New Delhi: Tata McGraw-Hill Education; 2006.
10. Latha A, Vijaya Kumar Reddy K, Sekhara Rao JC. Performance analysis on modeling of loop heat pipes using artificial neural networks. Indian Journal of Science and Technology. 2010 April; 3(4): 1–5.