A Single-Event Transient Radiation Hardened Low-Dropout Regulator for LC Voltage-Controlled Oscillator

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Abstract: A voltage-controlled oscillator (VCO) is an essential part of the clock circuitry in satellite communication systems. Low-dropout regulators (LDO) provide stable voltage supply to the VCO and inevitably bring in new radiation-sensitive nodes. In this paper, by conducting single-event transient (SET) sensitivity analysis of LDO in voltage-regulated VCO, we find the sensitive nodes of LDO in oscillation circuits located on the relevant transistors that determine the bias voltage of the tail transistor in the error amplifier (EA). To immunize SET, a symmetrical hardening method combining sensitive node splitting and resistive-decoupling is proposed for the sensitive nodes. This method achieves 80.8% analog single-event transient (ASET) mitigation. This study was conducted in 28-nm CMOS process.

Keywords: radiation-hardened-by-design (RHBD); single-event transient (SET); voltage regulator; low-dropout regulator (LDO); voltage-controlled oscillator (VCO)

1. Introduction

Phase-locked loop (PLL) is widely used to generate stabilized clocking in satellite communication systems. The cosmic radiation environment that the satellite-based PLL is exposed to makes it necessary to consider radiation resistance besides performance metrics in its design [1]. The particle impaction in the cosmic environment can lead to catastrophic failure of satellite communications. The single-event effect (SEE) is caused by a single particle that deposits a certain number of charges on the silicon substrate, which instantly interferes with the operation of the integrated circuit [2]. In addition to the single-event upset (SEU), which can flip the output of a digital logic circuit, SEE includes single-event transient (SET), which propagates through the circuit [3]. SET is a voltage disturbance caused by a collected radiation-induced charge in a circuit node that travels through the circuit.

A voltage-controlled oscillator (VCO) is the core module in the PLL, and its phase noise directly affects the performance of the PLL[4]. The power supply noise is the crucial source of phase noise in the VCO [5]. Therefore, the conventional design of VCO is focused on noise suppression of the power supply. A low-dropout regulator (LDO) is a common method to provide high-quality power supply to the VCO [6, 7].

LC VCO as a widely used component in high-speed communication applications, and many studies have been conducted on the SETs of LC VCO in the cosmic radiation environment [8–14]. When a single particle hits a sensitive node in VCO, it can lead directly to frequency deviation and signal distortion of the VCO outputs and even a temporary stop of oscillation [2, 15]. LDO as a structure to suppress VCO power supply noise has been studied for its SET characteristics in different semiconductor processes [16, 17]. Those studies found that loop stability [18], input voltage [19], and load conditions [20] all affect the SETs of linear regulators significantly.
Radiation Hardening by Design (RHBD) is one solution to SET mitigation. Unlike Radiation Hardening by Process (RHBP), RHBD is implemented in the CMOS process to achieve circuit-level hardening by applying a schematic and layout change.

Three-mode redundancy (TMD) is widely used in analog and mixed-signal circuit hardening, Ref. [21] used the TMD to harden the LC VCO, while Ref. [22] used this technology to harden ring VCO. It shows great hardening effects but at the cost of a significant increase in circuit surface area and power consumption. Filtering can reduce SET amplitude and duration on the circuit and system levels. Ref. [23] used filtering in LDO hardening design; however, the introduction of capacitors also increases the circuit surface area and power consumption. Ref. [24] proposed a fast transient response circuit under narrow-band conditions to improve the recovery speed of the LDO in the environment of radiation. This approach does not change the response loop in the LDO but introduces extra circuits that can be sensitive nodes. Resistive decoupling was first applied as a technique for hardening memory cells. Ref. [25] proposed an improvement in the SET response by adding a resistor in series with the base of the power transistor in the linear regulator. Ref. [26] used this method on the charge pump (CP) of PLL. Time-skewed space-split is an implementation of sensitive node-splitting technology, which is usually used to harden switched capacitor circuits. Ref. [27] used this method to harden the power transistor in LDO.

Research on the SETs of LDOs is mainly focused on commercial LDO chips and the SETs of on-chip LDOs have been less studied, especially those applied to LC VCOs. This paper analyzes the SET-sensitive nodes of LDO applicable to LC VCO and proposes a radiation-hardened LDO design based on sensitive node splitting and resistive decoupling under the restrictions of surface area and power efficiency.

This paper is organized as follows. Section 2 analyzes the SET effect for LDO in LC VCO. Section 3 discusses the corresponding radiation hardening structure. Section 4 summarizes the paper.

2. Responses of Single-Event Transients in the LDO

2.1. PLL Architecture

At present, the commonly used PLL is based on charge pumps, and its overall topology is shown in Figure 1. In the PLL, the clock $CLK_{OUT}$ generated by the VCO is compared with the reference clock $CLK_{REF}$ after the frequency divider (DIV), and the CP sources or sinks charges for a controlled amount of time according to the comparison signal $UP$ and $DN$. The low-pass filter (LPF) responds to the pump current with voltage a jump, and $V_{cont}$ controls the frequency of the signal generated by the VCO.

![Figure 1](image_url). Conventional charge pump phase-locked loop (CP-PLL) structure. $R_p$ represents the equivalent parallel resistance of the inductor in LC voltage-controlled oscillator (VCO), and $S_{vl}$ controls the constant tank capacitors, $C$. 
The source of VCO phase noise is electronic noise, power supply noise, and substrate noise; the phase noise directly determines the quality of the clock signal generated by the PLL [28]. The phase noise of the LC VCO can be expressed in Equation (1) [29]:

\[
S_{\phi n}(f) = \left( \frac{\sqrt{2}}{2} \gamma + 1 \right) \frac{\pi^2 kT}{2 R_p I_{\text{tail}}} \left( \frac{f_0}{2Qf} \right)^2
\]

where \( f_0 \) is the VCO oscillation frequency, \( Q \) is the quality factor of the LC oscillator, \( k \) is the Boltzmann constant, and \( T \) is the temperature in Kelvin. Equation (1) shows that the oscillation frequency \( f_0 \) is related to all capacitors in the LC VCO, including the switch-controlled constant capacitor \( C \), the switch-equivalent capacitor, the variable capacitor \( C_{\text{var}} \), and the drain-bulk capacitance of \( M_1 \) and \( M_2 \). When the power supply fluctuates, all variable capacitors, including the drain-bulk capacitance of \( M_1 \) and \( M_2 \), will be changed with the fluctuation of the power supply, thus changing the VCO output frequency \( f_0 \), which affects the phase noise of the VCO. Simultaneously, the power supply fluctuation also changes the \( K_{VCO} \) of the VCO, which directly affects the magnitude of the VCO output signal.

To suppress power-supply noise in VCOs, LDOs are commonly used in modern VCO designs. Any added circuit introduces extra sensitive nodes in the radiation environment; thus, SET-sensitive node analysis for the LDO is necessary. Since the LDO is used to suppress the power supply noise of the VCO and the SET-sensitive nodes in the LDO cannot be analyzed merely by considering the output voltage; therefore, the LDO and VCO need to be analyzed together.

2.2. Responses of SET in LDO

The LDO used in this study is shown in Figure 2a. The differential pair used in the error amplifier is an n-MOS transistor, and the power transistor is p-MOS transistor. SETs are simulated using a double exponential current source [30].

![Figure 2](image-url)

**Figure 2.** Low-dropout regulator (LDO) structure: (a) Supply-regulated VCO. (b) Unhardened regulator schematic.

Figure 2b shows the implementation of the LDO circuit in this paper. A start-up circuit is not presented in the schematic. Double exponential current sources with a peak value of 2 mA and a decay time of 2 ns are injected at the drains of MN6, MP1, MP3, and MP5, respectively.

To evaluate the impact of these current pulses, the output voltage of the regulator \( V_{\text{reg}} \), and the frequency of the VCO were analyzed. The simulation results are shown in Figure 3a–c.
Figure 3a shows the transient response of the LDO output voltage \( V_{\text{reg}} \) and VCO oscillation frequency when the particle strike occurs on the \( \text{MN}6 \). The LDO output voltage changed from 700 mV to 493 mV, and the VCO oscillation frequency changed from 8.589 GHz to zero. The oscillation recovery time was 492 ns.

Figure 3b, c present the transient simulation of the LDO output voltage \( V_{\text{reg}} \) and VCO oscillation frequency when the particle strike occurs on the \( \text{MP}1 \), \( \text{MP}3 \) and \( \text{MP}5 \). The LDO output voltage changed from 700 mV to 546 mV, 529 mV, and 732 mV, respectively. The oscillation recovery times were 278 ns and 5.7 ns for \( \text{MP}1 \) and \( \text{MP}3 \).

It can be seen that when a single particle strikes on \( \text{MN}6 \), \( \text{MP}1 \), and \( \text{MP}3 \), the LDO voltage decreased, which caused the VCO to stop oscillating, exhibiting a greatly varied non-oscillating duration. To maintain the oscillation of the VCO, the tail current source in the VCO should provide enough current to meet its oscillation conditions. When the power supply of the VCO is directly connected to the main power supply, the power supply can provide enough current to keep the VCO working as long as the tail current source of the VCO is in normal condition. However, when the regulator provides the power supply to the VCO, it will cause the VCO to stop oscillating if the regulator does not work correctly when injected with charges.

The transfer function between the LDO output voltage \( V_{\text{reg}} \) and the LDO input voltage \( V_{\text{ref}} \) is shown in Equation (2).

\[
\frac{V_{\text{reg}}}{V_{\text{ref}}} = \frac{A_{EA} \cdot A_p}{1 + A_{EA} \cdot A_p} \tag{2}
\]

where

\[
A_p = G_{\text{mMP5}}(R \parallel \frac{1}{sC}) / r_{\text{VCO}}
\]

\[
A_{EA} = G_{\text{mEARoEA}}
\]

\[
\approx G_{\text{mMN4}} \left\{ \left[ 1 + G_{\text{mMN2}r_{\text{MN2}}} \right] r_{\text{MN4}} \right\} / r_{\text{MP3}} \tag{3}
\]

\[
\approx G_{\text{mMN4}} \left\{ (G_{\text{mMN2}r_{\text{MN2}}}r_{\text{MN4}}) / r_{\text{MP3}} \right\} \tag{4}
\]

\[
G_{\text{mMN4}} = \frac{2 \cdot \frac{1}{2} I_{\text{tail}}}{V_{\text{gsMN4}} - V_{\text{irMN4}}} = \frac{I_{\text{tail}}}{V_{\text{gsMN4}} - V_{\text{irMN4}}} \tag{5}
\]

Power-supply rejection ratio (PSRR) is a term that quantifies the ability of a circuit to suppress fluctuations on the power supply.

\[
\Delta V_{\text{reg}} = \Delta V_{\text{ddlev}} \cdot A_p + \Delta(V_{\text{ref}} - V_{\text{reg}}) \cdot A_{EA} \cdot A_p \tag{6}
\]

\[
\text{PSRR}_{DC} = \frac{\partial V_{\text{reg}}}{\partial V_{\text{ddlev}}} = \frac{A_p}{1 + A_{EA} \cdot A_p} \approx \frac{1}{A_{EA}} \tag{7}
\]
When a particle impacts the LDO, the output voltage $V_{\text{reg}}$ of the LDO will change and no longer follow its reference voltage $V_{\text{ref}}$. The re-following process, realized slowly with the regulation of the loop, is closely related to the response time of the loop, which indicates that the bandwidth of the entire loop determines its regulation speed.

When a single particle hits the MP1 or MN6, the tail transistor $MN_7$ in the error amplifier no longer works in its saturation region, disabling the entire error amplifier. The failing error amplifier affects the power transistor $MP_5$ in the LDO circuit, making it unable to continue working in the saturation region. Inevitably, the LDO fails to provide sufficient current to the VCO, in which case the oscillation is terminated. Under this circumstance, the PLL will not be able to lock in a significant period. It is meaningless to achieve quick recovery by improving the loop response time since the drastic change in bias conditions will not recover instantly by the feedback loop. For $MP_3$, SET will potentially reduce its drain voltage, causing the LDO voltage output to decrease and eventually stop the VCO. However, the working region of the $MN_7$ is not changed, and the entire system will be immediately recovered once the particle strike is over.

3. The Proposed SET Hardened LDO Regulator

As mentioned in the previous analysis, it is essential to add an LDO regulator to the VCO in the PLL design. However, the added LDO regulator will introduce additional sensitive nodes, making the study of regulator hardening necessary. The previous analysis proved that under SET, the sensitive node inside the regulator that de-oscillates the VCO is the insufficient current source of the error amplifier. In other words, the bias voltage of the $MN_7$ is too low to work in the saturation region, and the recovery takes time. The hardening design principle is to reduce the possibility of bias voltage being cut off and to avoid introducing additional sensitive nodes.

3.1. Proposed SET Radiation-Hardened (RH) Structure

The key to our hardening design is to reduce the possibility of $MN_7$ being turned off or to stabilize $MN_7$ to provide sufficient current to the differential pair transistors under single particle impaction. As Figure 4 shows, to achieve this goal, we split the required tail current into multiple parts, which are provided by different transistors ($MN_7_1$–$MN_7_n$), to ensure that they are independent of each other. When one of the transistors is impacted by a single particle and no longer provides sufficient current, other transistors still work normally.

$$I_{\text{tail}} = \sum_{i=1}^{n} I_{\text{tail}_i}$$

In analog integrated circuit design, the gate width of the transistor is usually a multiple of 2 to match the layout. When we split the current $I_{\text{tail}}$, the number of current splits $n$ must be a power of 2. The number of split parts is limited by the size of the transistors in the unhardened circuit design.

To make the split $MN_7$ parts independent of each other, all the splits are provided by independent bias circuits. When splitting $MN_7$, it is necessary to split $MP_1$, $MP_4$, $MN_5$, and $MN_6$, respectively, into the same number of parts as $MN_7$. To further attenuate the effect of the SET on the current, resistive decoupling is adopted in this design. The splits of the same node are connected by a resistor in the middle. The current is supplied.
in the multi-path, and transistors are symmetrically split. The overall hardened circuit symmetrical multi-path splitting (SMPS) when transistors are split into two parts is shown in Figure 5.

From the previous simulation results, it can be seen that single particle impaction on either MN6 or MP1 will cause the VCO to stop oscillation for a different duration. When the single particle impaction occurs on MP1, it takes a certain path to transmit the MN7; meanwhile, SET has its transfer characteristics that will be attenuated by physical distance, thus causing a relatively shorter stop of oscillation. However, the impaction on MN6 directly affects the bias of MN7, causing a longer stop of oscillation. Since the MN6 is more sensitive to SET, we will use MN6 as an example to explain the hardening design in the following discussion.

![Figure 5](image)

Figure 5. Symmetrical multi-path splitting (SMPS) regulator, with a split factor \( n = 2 \).

### 3.2. Analysis

A comparison before and after the implementation of the hardened design of MN6-related circuits is shown in Figure 6.

![Figure 6](image)

Figure 6. (a) Unhardened MN6 related circuit; (b) symmetrical multi-path splitting (SMPS) circuit-related MN6.

The two ends of each resistor \( R_{split} \) are symmetrically connected to MN6 \((n-1)\), MN7 \((n-1)\), MP4 \((n-1)\), C1 \((n-1)\), and MN6 \(n\), MN7 \(n\), MP4 \(n\), C1 \(n\), and the
electric potentials at both ends are \( V_{G(n-1)} \) and \( V_{Gn} \). In the absence of SET, that is, when direct current (DC) is stabilized, both ends of \( R_{\text{split}} \) have the same electric potential because of the completely symmetrical circuit structure, and no current passes through \( R_{\text{split}} \).

As mentioned above, the number of splits \( n \) must be a power of two. When \( n = 2 \), the bias voltage of \( MN7_1 \) is provided by \( V_{G1} \), and the bias voltage of \( MN7_2 \) is provided by \( V_{G2} \). When the drain of \( MN6_1 \) is affected by a single particle, the voltage fluctuation occurs, and this voltage fluctuation will change the current \( I_{\text{tail.1}} \) of \( MN7_1 \). To analyze the propagation of this fluctuation in the circuit, we give the equivalent circuit of SMPS, as shown in Figure 7a.

Note that the small-signal equivalent circuit of the \( MN7_n \) is not shown in the figure, because the change in the \( MN7_n \) bias voltage is the main concern. \( R_{eq} \) is the equivalent resistance of \( MP4_n \) and \( MN6_n \), and \( C \) is the equivalent capacitance of \( C1_n \) and each transistor combined.

\[ R_{\text{eq}} \text{ presents the equivalent resistance of } MN6 \text{ and } MP4. \]

When the drain of \( MN61 \) is injected with the same SET model as in Section 2, the current generated by the SET will cause voltage fluctuation \( \Delta V_{G1} \) at \( V_{G1} \). Then, the voltage fluctuation at \( V_{G2} \), \( \Delta V_{G2} \) is

\[
\Delta V_{G2} = \frac{R_{eq} / \left( \frac{1}{sC} \right)}{R_{eq} / \left( \frac{1}{sC} \right) + R_{sp}} = \frac{1}{1 + sCR_{sp} + \frac{R_{sp}}{R_{eq}}} \cdot \Delta V_{G1} \tag{9}
\]

\( R_{sp} \) is short for \( R_{\text{split}} \).

It can be seen that SET-induced voltage fluctuation at \( V_{G2} \) can be significantly reduced by splitting the transistor and by adding the resistor, reducing the fluctuation of \( I_{\text{tail.2}} \).

If the value of \( R_{\text{split}} \) is set to be small, the equation can be simplified to

\[
\Delta V_{G2} = \frac{1}{1 + sCR_{sp}} \cdot \Delta V_{G1} \tag{10}
\]

This is the same as the equation in Figure 7b, so we use the simplified circuit shown in Figure 7b in the following analysis.

If we split the circuit into four parts (when split factor \( n = 4 \)), the voltage fluctuation of each stage is gradually reduced. Figure 8 shows the equivalent circuit when \( n = 4 \).

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**Figure 7.** Small-signal equivalent circuit diagram associated with \( MN6 \) in SMPS when split factor \( n = 2 \). (a) \( R_{eq} \) presents the equivalent resistance of \( MN6 \) and \( MP4 \). (b) Ignored transistor-equivalent resistance.

**Figure 8.** Small-signal-equivalent circuit diagram associated with \( MN6 \) in SMPS when split factor \( n = 4 \).
In Figure 8, with the same voltage fluctuation at $V_{G1}$, the voltage fluctuation at $V_{G2}$ is

$$
\Delta V_{G2} = \frac{[(R_{sp} + \frac{1}{sC})/\frac{1}{sC} + R_{sp}]/\frac{1}{sC} + R_{sp}}{[(R_{sp} + \frac{1}{sC})/\frac{1}{sC} + R_{sp}]/\frac{1}{sC} + R_{sp}} \cdot \Delta V_{G1}
$$

(11)

The voltage change at $MN_{6_3}$ is

$$
\Delta V_{G3} = \frac{[(R_{sp} + \frac{1}{sC})/\frac{1}{sC} + R_{sp}]/\frac{1}{sC} + R_{sp}}{1 + sCR_{sp}} \cdot \frac{1}{1 + 6sCR_{sp} + 5(sC)^2R_{sp}^2 + (sC)^3R_{sp}} \cdot \Delta V_{G1}
$$

(12)

The voltage change at $MN_{6_4}$ is

$$
\Delta V_{G4} = \frac{[(R_{sp} + \frac{1}{sC})/\frac{1}{sC} + R_{sp}]/\frac{1}{sC} + R_{sp}}{1 + sCR_{sp}} \cdot \frac{1}{1 + 6sCR_{sp} + 5(sC)^2R_{sp}^2 + (sC)^3R_{sp}} \cdot \Delta V_{G1}
$$

(13)

The equations indicate that the voltage fluctuation is related to the value of the resistance $R_{sp}$. Furthermore, the more splits there are in SMPS, the smaller the corresponding bias voltage fluctuation of $MN_{7}$ will be. Hence, the tail current change caused by the voltage fluctuation will be reduced and the total change in the current $I_{tail}$ induced by SET will be smaller.

Next, we will compare the hardening effect of different splits and different $R_{sp}$ values.

### 3.3. Simulations

As mentioned above, the number of splits is limited by the size of the transistors. In our original unhardened design, the size of $MN_{5}$ and $MN_{6}$ is $W/L = 2 \ \mu m/1 \ \mu m$, $M = 8$. The size of $MN_{7}$ is $W/L = 2 \ \mu m/300 \ nm$, $M = 72$. The size of $MP_{1}$ and $MP_{4}$ is $W/L = 1.25 \ \mu m/500 \ nm$, $M = 4$. In an SMPS circuit, $MP_{1}$ and $MP_{4}$ can be split into eight parts at most. We analyzed the performance when $n = 2$, $n = 4$, and $n = 8$ in the following analysis.

To measure the hardening effect, the same double exponential current source with a peak value of 2 mA and a decay time of 2 ns was injected into the drain of $MN_{6_1}$ to simulate the single particle hit. We simulate the total current sum of $MN_{7_1}$ to $MN_{7_n}$ in the SMPS circuit, as well as the frequency of the VCO output signal, considering how they change under the impaction of the same SET as the unhardened circuit.

Figure 9 illustrates the transient simulation results of the SMPS circuit when the split factor is 2.
Figure 9. SET-induced disturbance in (a) total current sum of $MN_7_1$ and $MN_7_2$; (b) VCO oscillation frequency with SMPS circuit when the split factor is 2.

It can be seen that in the increase in the resistance value of the split resistor, the change in the total current inducted by the SET becomes smaller and the stopping time is shortened. However, even if the resistance value reaches 288 kΩ, the total current of $I_{tail}$ decreased from 2.43 mA to 1.22 mA when particle strike occurred, which is not enough for the EA to operate correctly. So it still cannot be fully immune to SET and will cause VCO oscillation to stop. The hardening effect is not obvious when $n = 2$ in SMPS design.

Figure 10 presents the transient simulation results of a hardened circuit when the split factor is four.

Figure 10. SET induced disturbance in (a) total current sum of $MN_7_1$, $MN_7_2$, $MN_7_3$ and $MN_7_4$. (b) VCO oscillation frequency with SMPS circuit when the split factor is 4.

As the resistance value of the split resistor increasing, the change in the total current due to SET becomes smaller. When the resistance value reaches 24 kΩ, the total current of $I_{tail}$ decreases from 2.43 mA to 1.66 mA, no VCO oscillating stop occurs, and it can fully realize the immunity to SET. For our original unhardened design, the minimum split factor for effective hardening is when $n = 4$.

Figure 11 shows the transient simulation results of SMPS circuit when $I_{tail}$ is split into eight parts.

When the split factor $n = 8$, SET immunity can be achieved with a 4 kΩ or 5 kΩ split resistor. The total current of $I_{tail}$ decreases from 2.43 mA to 1.54 mA and 1.62 mA, respectively.
Figure 11. SET induced disturbance in (a) total current sum of $MN7_1$–$MN7_8$. (b) VCO oscillation frequency with SMPS circuit when the split factor is 8.

From Figures 9–11, we can figure out that both the split factor and the resistance value affect the hardening effect of the SMPS circuit. Notably, a higher split factor requires more resistors. So we should compare the hardened effect in terms of total resistance value.

We consider the total resistance value needed for the hardening of $MN6$. Naturally, the resistance value needed for the overall circuit should be multiplied by two because the overall hardened structure is symmetric.

Figure 12 illustrates the relation between the total resistance in the SMPS structure for hardening $MN6$ and the VCO oscillating recovery time at different split factors. The VCO oscillating recovery time’s decreasing trend for $n = 2$ (black square in the figure) clearly shows that it is unlikely to achieve SET immunity. When the total resistance reaches about 40 kΩ with $n = 4$ and $n = 8$, VCO oscillating does not stop when SET occurs.

Figure 12. VCO oscillating recovery time versus total resistance at different split factors.

Figure 13 presents the SET induced LDO output disturbance with different SMPS configurations. The voltage variation is less than 40 mV, while it is 207 mV in unhardened LDO (see Figure 3a).

For the three combinations that can achieve the SET immunity, we simulated their power consumption. The power consumption here is the average power loss when the circuit is in a stable condition without SET. It is calculated by multiplying the power supply voltage of the LDO by the power supply current of the LDO. The result is shown in Table 1.
Figure 13. SET induced LDO output disturbance with different SMPS configurations.

Table 1. Power loss comparison.

|                      | Unhardened Structure | SMPS ($n = 4$ $R_{sp} = 24 \text{k}\Omega$) | SMPS ($n = 8$ $R_{sp} = 4 \text{k}\Omega$) | SMPS ($n = 8$ $R_{sp} = 5 \text{k}\Omega$) |
|----------------------|-----------------------|---------------------------------------------|---------------------------------------------|---------------------------------------------|
| Power Loss (mW)      | 11.46902              | 11.48909                                    | 11.48197                                    | 11.48194                                    |

In the simulation, SMPS does not increase power consumption because no extra transistors are added. Furthermore, the added resistors at both ends do not add much power because the circuit structure is symmetrical when the layout is matched.

Figure 14 illustrates an LDO PSRR comparison between unhardened LDO and several SMPS LDOs with different configurations. SMPS structure does not affect the PSRR of the LDO.

The characteristics of SMPS are summarized and compared with other state-of-art techniques in Table 2.
Table 2. Comparison with other state-of-the-art analog single-event transient (ASET) mitigation methods.

| Ref. No. | Ref. [27] | Ref. [23] | Ref. [31] | This Work |
|----------|-----------|-----------|-----------|-----------|
| Method   | time-skewed space-split | built-in filter | bulk tied to source | symmetrical multi-path splitting (SMPS) |
| Technology | 180 nm | 180 nm | 40 nm | 28 nm |
| ASET mitigation | 63% | 64.6% | 75.8% | 80.8% |
| Hardening level | circuit | circuit | transistor | circuit |

1 Compare in analog single-event transient (ASET) peak voltage.

4. Conclusions

This paper analyzes the single-event transient (SET) sensitive nodes in a low-dropout regulator for an LC voltage-controlled oscillator. A symmetrical multi-path-splitting (SMPS) hardening structure for SET mitigation in LDO is proposed. Based on commercial 28 nm CMOS technology, the Spice simulation results indicate that SMPS reduces 80.8% of SET-induced LDO output fluctuation. This structure has no additional power consumption and does not effect the LDO power-supply rejection ratio.

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Abbreviations
The following abbreviations are used in this manuscript:

- ASET: analog single-event transient
- CP: charge pump
- DC: direct current
- DIV: frequency divider
- EA: error amplifier
- LDO: low-dropout regulator
- LPF: low-pass filter
- PLL: phase-locked loop
- PSRR: power-supply rejection ratio
- RH: radiation-hardened
- RHBD: radiation-hardened-by-design
- RHBP: radiation-hardened-by-process
- VCO: voltage-controlled oscillator
- SEE: single-event effect
- SET: single-event transient
- SEU: single-event upset
- SMPS: symmetrical multi-path splitting
- TMD: three-mode redundancy
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