Abstract—Multilevel inverters are used to improve power quality and reduce component stresses. This paper describes and compares two multilevel cascaded three phase inverter implementations with two different modulation techniques: Phase Shifted Pulse Width Modulation, and Nearest Level Control. Further analysis will show required number of inverter levels with respect to modulation techniques to provide desired power and power quality to resistive load or grid. Cascaded inverter will be designed and simulated to draw power from PV cells.

I. INTRODUCTION

A multi-level inverter is a power electronic system that synthesizes a desired voltage output from several levels of DC voltages as inputs [9]. Today, there are many different topologies of multilevel converters including, but not limited to, Diode-Clamped, Flying Capacitor, and Cascade H-bridge (CHB). While the topologies may be different, they all offer similar beneficial features. For sinusoidal outputs, multilevel converters improve their output voltage in quality as the number of levels of the converter increase, thus decreasing the Total Harmonic Distortion (THD) [6]. For this reason and others, multilevel converters have been used for high power photovoltaic (PV) inversion, electric motor drivers in electric vehicles, and other research and commercial applications [6], [3], [2], [9], [2]. Although, technological problems such as reliability, efficiency, the increase of the control complexity, and the design of simple modulation methods have slowed down the application of multilevel converters [6].

Figure 1 shows a 5 level CHB converter. As can be seen, CHB converters consist of multiple MOSFET (or equivalent) H-bridges that are connected in series. Each H-bridge having its own isolated DC voltage source. For the shown 5 level case, it requires two H-bridges that can be configured to output the 5 levels: +V, +V/2, 0, -V/2, and -V. While the theory of adding and subtracting isolated voltage sources is simple, such is harder to do in practice. Common methods include using isolated DC-DC converters such as flyback and forward converters that have transformers with multiple secondary windings [6]. Others use individual, or multiple isolated sets of PVs that power individual H-bridges [9], [2].

This paper uses two of the common modulation techniques for CHB converters, Phase Shifted PWM (PSPWM) and Nearest Level Control (NLS), to propose designs for a utility 3 phase PV inverter. Our designs will display many of the common advantages and disadvantages of the different modulation techniques for CHB. Our design requirements were to develop a 3 phase utility PV CHB inverter to supply 125kW at $480V_{\text{RMS}}$ with a THD below 5%.

II. NEAREST LEVEL SWITCHING

The Nearest-Level Switching control for a multilevel converter compares a control sine wave to DC voltage levels. For a Cascading Multi-level Converter consisting of $N$ H-bridges, each trigger when the voltage control sinusoidal is greater than their respective threshold given by the equation:

$$V_{\text{thresh}}(i) = V_{\text{pk}} \frac{2i - 1}{2N}$$  \hspace{1cm} (1)

Where $N$ is the number of H-bridges equal to $N = \frac{L-1}{2}$ for an $L$ level Cascade H-bridge (CHB), and $i$ is the switch number which ranges from 0 to $N-1$.

Figure 2 shows the waveform for the Nearest Level Switching. It should be noted that for every DC voltage source, the threshold voltage is at half of the DC value. Additionally, the peak output voltage is equal to $N \times V_{\text{DC}}$.

Figure 3 shows the PWM waveforms for the top H-bridge of a 9-level NLS CHB. The PWM for switches 1 and 3 are not the same, as is the case for switches 2 and 4. For
Figure 2. Nearest Level Switching Waveform Synthesis

For a cascading H-Bridge Multilevel Inverter with L levels, using the Nearest-Level-Switching technique, the switching point $\alpha_i$ for level $i = 0$ to $i = \frac{L-1}{2}$, are given by the equation:

$$\alpha_i = \sin^{-1} \left( \frac{2i + 1}{L-1} \right)$$

A. Root Mean Squared

From [8], the equation for calculating the RMS ($X_{RMS}$) of a function $x(t)$ is given as:

$$X_{RMS} = \sqrt{\frac{1}{T} \int_0^T (x(t))^2 \, dt}$$

B. 5-Level

For the simple 5-level Inverter with NLS, the RMS voltage of a resistive load can be calculated to be:

$$V_{5-L}^{RMS} = \frac{1}{\pi} \int_{\alpha_0}^{\pi-\alpha_1} (V_m)^2 \, dt + \int_{\pi-\alpha_0}^{\pi-\alpha_1} (V_m)^2 \, dt + \int_{\pi-\alpha_1}^{\pi-\alpha_0} (V_m)^2 \, dt$$

$$= V_m \sqrt{\frac{1}{\pi} \left( \frac{t}{2} \right) \frac{\pi}{\alpha_0} + \frac{t}{4} \frac{\pi}{\alpha_0} + \frac{t}{4} \frac{\pi}{\alpha_1} - \frac{t}{2} \frac{\pi}{\alpha_1}}$$

For $\alpha_0 = \sin^{-1} \left( \frac{1}{5} \right)$ and $\alpha_1 = \sin^{-1} \left( \frac{3}{5} \right)$

$$V_{5-L}^{RMS} \approx V_m 0.7449$$
C. 7-Level

For the simple 7-level Inverter with NLS, the RMS voltage of a resistive load can be calculated to be:

\[
V_{7-L}^{\text{RMS}} = \frac{1}{\pi} \left( \int_{\alpha_0}^{\alpha_1} \frac{V_m}{3} \, dt + \int_{\alpha_1}^{\alpha_2} \frac{2V_m}{3} \, dt \right)
+ \int_{\alpha_2}^{\pi/2} (V_m)^2 \, dt + \int_{\pi/2}^{\pi-\alpha_2} \left( \frac{2V_m}{3} \right)^2 \, dt
+ \int_{\pi-\alpha_2}^{\pi-\alpha_1} \left( \frac{V_m}{3} \right)^2 \, dt \right)^{1/2}
\]

\[
= \sqrt{\frac{V_m}{\pi}} \left( \int_{\alpha_0}^{\alpha_1} \alpha_0 + \frac{2\alpha_2}{3} \right)
+ \int_{\alpha_2}^{\alpha_1} \frac{2\alpha_1}{\pi - \alpha_1} \right)^{1/2}
\]

\[
= \sqrt{\frac{V_m}{\pi}} \left( \int_{\alpha_0}^{\alpha_1} \frac{\alpha_0}{2} - \frac{2}{9} \alpha_0 - \frac{6}{9} \alpha_1 - \frac{10}{9} \alpha_2 \right)
\]

\[
= \sqrt{\frac{V_m}{\pi}} \left( \int_{\alpha_0}^{\alpha_1} \alpha_0 - \frac{6}{9} \alpha_1 - \frac{10}{9} \alpha_2 \right)
\]

\[
V_{7-L}^{\text{RMS}} \approx V_m 0.7217
\]

D. L-Level

From the previous derivations and Equation 2, a pattern for the RMS voltage can be seen. For a multilevel cascade H-Bridge Inverter with L levels, the equation for the RMS voltage of a resistive load can be given by:

\[
V_L^{\text{RMS}} = V_m \sqrt{1 - \sum_{i=0}^{N-1} \left( \frac{2(2i+1)}{\pi N^2} \right) \sin^{-1} \left( \frac{2i+1}{L-1} \right) (2i+1)}
\]

E. Fourier Series Expansion

The Fourier Series Expansion was also performed on the ideal cascade H-bridge Inverter. In the ideal case with a purely resistive load, the output waveform has odd symmetry and quarter-wavelength symmetry inherently. From [8], the Fourier Series Expansion Coefficients for such symmetry are given as:

\[
a_h = 0
\]

\[
b_h = \frac{4}{\pi} \int_0^{\pi/2} (x(t) \sin(h\omega t)) \, dt
\]

1) 3-Level: For the simple 3-level Inverter with NLS, the Fourier Series Expansion Coefficients of a resistive load can be expressed as:

\[
b_h(3) = \frac{4}{\pi} \int_{0}^{\pi/2} (V_m \sin(h\omega t)) \, dt
\]

\[
= \frac{4V_m}{\pi h} \left[ -\cos(h\omega t) \right]_{\alpha_0}
\]

\[
= \frac{4V_m}{\pi h} \cos(h\alpha_0)
\]

F. 5-Level

For the simple 3-level Inverter with NLS, the Fourier Series Expansion Coefficients of a resistive load can be expressed as:

\[
b_h(5) = \frac{4}{\pi} \left( \int_{\alpha_0}^{\pi/2} (V_m \sin(h\omega t)) \, dt \right)
+ \int_{\alpha_1}^{\pi/2} \left( \frac{V_m}{2} \sin(h\omega t) \right) \, dt
\]

\[
= \frac{2V_m}{\pi h} \left( -\cos(h\omega t) \right)_{\alpha_0} + \frac{2V_m}{\pi h} \cos(h\omega t)
\]

\[
= \frac{2V_m}{\pi h} (\cos(h\omega t) + \cos(h\alpha_0))
\]

G. L-Level

For a multilevel cascade H-Bridge Inverter with L levels, the Fourier Series Expansion Coefficients of a resistive load can be expressed as:

\[
b_h(L) = \frac{4}{\pi} \sum_{i=0}^{N-1} \int_{\alpha_i}^{\pi/2} \left( \frac{V_m}{N} \sin(h\omega t) \right) \, dt
\]

\[
= \frac{4V_m}{\pi h N} \sum_{i=0}^{N-1} \cos(h\alpha_i)
\]

This can be simplified using the trigonometry identity:

\[
\cos(\sin^{-1}(x)) = \sqrt{1 - x^2}
\]

From Equation 2 the Fourier Series first Coefficient can be simplified to be:

\[
b_1(L) = \frac{4V_m}{\pi N} \sum_{i=0}^{N-1} \left( \sqrt{1 - \left( \frac{2i+1}{L-1} \right)^2} \right)
\]

H. Total Harmonic Distortion

From [8], the equation for the Total Harmonic Distortion (THD) is given by:

\[
THD = \frac{\sqrt{\left( X_{RMS} \right)^2 - \left( X_1^{RMS} \right)^2}}{X_1^{RMS}}
\]

From Equation 5 the equation for the RMS magnitude of the first harmonic can be calculated as:

\[
V_1^{RMS}(L) = \frac{4V_m}{\pi N \sqrt{2}} \sum_{i=0}^{N-1} \left( \sqrt{1 - \left( \frac{2i+1}{L-1} \right)^2} \right)
\]
Equations [7], [4], and [6] were combined and plotted using Python (Appendix A) to calculate the THD of an L-level CHB inverter with a resistive load. At the same time, PSIM simulations for the same number of levels were run with resistive loads and compared against one another.

| Levels (L) | PSIM THD (%) | Calculated THD (%) |
|-----------|--------------|-------------------|
| 3         | 31.0512      | 31.08419          |
| 5         | 17.5799      | 17.6012           |
| 7         | 12.2126      | 12.2272           |
| 9         | 9.35322      | 9.363669          |
| 11        | 7.58321      | 7.587252          |
| 13        | 6.3712       | 6.378124          |
| 15        | 5.40467      | 5.502021          |
| 17        | 4.83621      | 4.837995          |
| 19        | 4.31314      | 4.317328          |
| 21        | 3.89612      | 3.89809           |
| 23        | 3.55342      | 3.553263          |
| 25        | 3.26193      | 3.264629          |
| 27        | 3.017        | 3.01947           |

Table I shows the THD results from both the Theoretical Calculated THD and the PSIM simulated THD for 3 levels to 27 levels. The two data sets are consistent with each other. From the Table, as the number of levels increases, the THD decreases. This quantitatively confirms that the output sinusoidal quality improves with more and more additional levels of the CHB.

### IV. Nearest Level Switching Simulation Design

As previously mentioned, the design goals were to produce a 60 Hz 3 phase inverter at $480V_{L-L}^{RMS}$ with a real power output of 125 kW. The THD of our inverter also needed to be below 5%. These specifications were consistent with other commercially available PV inverters [3].

From [7], for a buck converter, we know:

$$ V_o = D V_s $$

$$ \Delta i_L \approx \frac{V_i + \Delta t}{L} $$

$$ \approx \frac{D V_o (1 - D) T}{L} $$

$$ L \approx \frac{D V_o (1 - D) T}{\Delta i_L} $$

$$ \Delta V_c \approx \frac{T \Delta i_L}{8C} $$

We expect $I_{Lpk} \approx 30A$. Let $f_s = 200kHz$, $V_s = 48.9V$, $V_o = 480V \sqrt{2}/3/\sqrt{3} \approx 30.15V$, $\Delta V_c = 4V$, and $\Delta i_L = 5% = 6A$. Then:

$$ D = 0.6165 $$

$$ L = 9.633 \mu H \approx 10 \mu H $$

$$ C = 937nF \approx 1 \mu F $$

The capacitor and inductor were intentionally kept small, but above critical values such to reduce their equivalent impedance when placed in series. Once the buck converters were designed, a single phase was simulated against a grid ac voltage source with a phase shift of -2.5 degrees in order to determine the desired cutoff frequency for the output filter. From our simulations, a cutoff frequency of approximately 700Hz was selected based on the output current harmonics. A simple LC low pass filter was chosen, with a cutoff frequency given by [7] as:

$$ f_c = \frac{1}{2 \pi \sqrt{LC}} $$

An inductor $L_f = 1mH$ and a capacitor $C_f = 50\mu F$ were selected.

### V. Nearest Level Switching Simulation Simulation

#### A. NLS Results

The NLS-CHB was first simulated with a single phase using ideal switches and a phase angle of -2.5 degrees from the grid voltage source. The simulation was able to reach a power level of 8.5 kW per phase at the desired line to neutral voltage level. The output current RMS was 30.66A and the current THD was 3.02%. At this current level, using the PV arrays from [10], we would need two in parallel going connected to each buck converter.

The NLS-CHB was then simulated with a single phase using the PSIM default lossy switching models for NMOS...
MOSFETs. In addition, all reactive components were given series resistance values of 50mΩ. The circuit was simulated for 0.5s and the output THD increased to 4.486% at a power factor of 99.56%.

The NLS-CHB was finally simulated with all three phases, each with a respective phase shift of -2.5 degrees. Figure 5 shows the PSIM file of the NLS-CHB three phase simulation. Figures 6 and 7 show the output waveforms and characteristics respectively. The desired output voltage of \(480\text{V}_{\text{RMS}}\) was achieved. The output real power was approximately 25kW with an output current THD of approximately 3.12%. From our simulation, in order to achieve our design requirements, 5 of such three phase inverters would need to be placed in parallel.

**Figure 8. Nearest Level Switching H-bridge Switch Stresses**

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**Figure 8. Nearest Level Switching H-bridge Switch Stresses**

The benefits that the Nearest Level Switching brings include greater efficiency and the ability to use additional active elements (additional H-bridges) in order to improve output waveform quality [3], [4]. From our analysis it has been shown that by increasing the number of H-bridges and levels, the THD of the output waveform decreases, thus making the output closer to a pure sinusoid. Due to the slow switching nature of the NLS technique, all switches turn on and off only once for the fundamental period of the output waveform, reducing the commutation losses of the switches but increasing the conduction losses. Also, as the number of H-bridges increases, the voltages across each of the switches in the H-bridges decreases (Equation 1), thus reducing individual switch losses and stresses. At the same time, as the number of H-bridges increases, the number of total switches will increase, thus increasing the total losses as well as the overall complexity of the control for all of the switches [4]. Thus the optimized number of switches depends on the specifications of the switches used as well as the output voltage and power. As a result, NLS CHB circuits are better suited for some applications more than others [3], [6].

**B. NLS Comments**

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VI. PHASE SHIFTED PWM

The Phase Shifted PWM control for a multilevel converter applies a triangular waveform in comparison to a control sinusoidal function in order to obtain the desired PWM for each H-bridge. Each H-bridge’s triangle waveform has a phase shift depending on the number of levels:

$$\theta_{\text{shift}} = \frac{360^\circ}{L-1} = \frac{360^\circ}{2N}$$

(12)

Where N is the number of H-bridges in the cascade. The DC voltage for each H-bridge level is defined as:

$$V_{DC} = \frac{V_{DC,0}}{N}$$

(13)

Where $V_{DC,0}$ is the DC voltage required to generate desired AC output voltage in case of a single level inverter.

VII. PHASE SHIFTED PWM INVERTER DESIGN

For this project, it has been decided to choose cascade consisting of 6 level H-bridge inverters with PSPWM control. The carrier waveforms for all of the 6 levels were triangle waves of 100kHz. The overall 3 phase circuit with load, and level circuitry are shown in Figures 9 and 10. Note that the inverter is connected to the grid and the grid has an associated inductance is 1 mH. The grid voltage was given a -2.5° phase shift with respect to inverter output voltage to facilitate current flow from inverter to grid.

From our project requirements, the required output voltage was $480\sqrt{2}\text{V}_{\text{RMS}}$, or $\approx 277\sqrt{2}\text{V}_{\text{RMS}}$. From [8] and Equation [13] the total required DC voltage $V_{DC,0}$ and the individual H-bridge DC voltages $V_{DC,\text{level}}$ were found as:

$$V_{DC,0} = \frac{V_{\text{rms},LL}}{mA_{m_0}=0.8} \times \sqrt{\frac{2}{3}} = \frac{2}{3} \times \frac{480}{0.8} \approx 490V$$

$$V_{DC,\text{level}} = \frac{490}{6} \approx 81.67V$$

Similarly, from equation [12] the individual carrier wave phase shift can be found as:

$$\theta_{\text{shift}} = \frac{360^\circ}{2 \times 6} = 30^\circ$$

Figure 10 shows the carrier signals for a 6 level cascaded H-bridge inverter (positive leg control signals are shown in top part, and negative leg control signals are shown in bottom part).

Figure 11 displays the PS-PWM buck converter used. The inductor and capacitor values were calculated using Equations [9] and [10] (Final inductor and capacitor values were chosen to be 100µH and 100µF).This circuit will facilitate power flow from the PV network to the cascaded inverter. Based on the single phase inverter, current draw from the circuit was $\approx 13.7ADC$. That leads to conclude that the inverter’s levels will behave as resistive load of 6Ω for the buck converter. This figure has been used to design the appropriate buck converter (Equation [11]).

VIII. PS-PWM SIMULATION RESULTS

A. 3φ Simulation Data Analysis

First, the PSIM simulations for a single phase using the default PSIM lossy MOSFET models and lossy reactive elements ($R_{\text{series}} = 50m\Omega$) were examined.

Figures 13 and 14 display the output voltage and current filtered and unfiltered waveforms as well as the wave to each buck converter would be needed in order to provide sufficient voltage and current for our inverter. Hence, the input voltage and available current for buck converter are: 120.6 VDC @ 19.42 ADC. This defines duty cycle of buck converter to be $0.677$ from Equation [8].

Based on the unfiltered voltage and current simulation data, the voltage high frequency harmonics at frequencies above 2 kHz. Therefore, in order to have a low filtered THD with reasonably high L and C values for filter, it was decided to set cut-off frequency of LC filter at $\approx 1453Hz$. In addition to LC filter, the equivalent grid line inductance of 1 mH also acts as a filter. From Equation [11] the calculated filter values were:

$$L_f = 200\mu\text{H}$$

$$C_f = 60\mu\text{F}$$
Figure 11. Buck converter required to facilitate 81.67 VDC for inverter level

Figure 12. Filtered and unfiltered voltage and current output waveforms characteristics respectively for the single phase lossy simulation. As can be seen, the output voltage met the required line-line voltage of $480\sqrt{2}$ V. In addition, all of the THD values were below 5%. The single phase output power was approximately 6.8kW.

B. 3φ Simulation Data Analysis

Next, the PSIM simulations for a three phase circuit using the default PSIM lossy MOSFET models and lossy reactive elements ($R_{\text{series}} = 50\,\text{m} \Omega$) were examined. Figures 15 and 16 display the output voltage and current filtered and unfiltered waveforms as well as wave their characteristics for the single phase lossy simulation. As can be seen, the output voltage and output current THD values are below the required 5%. The total output power from the three phase simulation was calculated to be approximately 20.3kW. Thus in order to meet the design requirement of 125kW, at least seven three phase H-bridge inverters of this topology would need to be used.

Figure 17 shows the voltages and currents experienced by the H-Bridges of the PS-PWM inverter. Based on the simulation data, the voltage stress on MOSFETs was approximately 85 VDC, and current stress was approximately 40 A. Base on design experience, voltage and current ratings are desired to be increased by 150% to maintain safe operation at extreme performance cases. That implies that actual switch ratings should be 150 VDC / 60 A.

IX. CONCLUSIONS

Multilevel converters inherently provide desired characteristics for high powered applications; but with them come inherent issues such as more complex structure and operation. The CHB in particular has a structure that allows for very high power applications due to their series connections of isolated power supplies. The drawback of this structure is that if a single power source is used to supply each of the levels, then the isolation transformer would require currently non-standard transformers with large numbers of secondary windings[4]. Our solutions, as well as [9], [2], solve this problem by having isolated PV cells. This method assumes that all of the PV’s output the same current, but in practice would require more.
complex control in order to achieve the desired output voltage and power from PV cells that are not providing equal power. In addition, the gate control of each H-bridge would require to be isolated.

This paper proposes two solutions for creating CHB inverters capable of outputting 125kW at $480\text{V}_{L-L}^{\text{RMS}}$. Our simulation results show that such is possible while maintaining a current THD below 5% as required for IEEE-519 \cite{IEEE519}. Multilevel converters such as the CHB have unique features for power quality and modularity. Although they are not commonly used in industry now, they have great potential for the future.

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from math import pi, asin, sqrt

def rms_value(L):
    '''
    Function to return the rms value for the 'L' level cascade H-bridge inverter
    :param L: int for the number of levels (needs to be odd)
    :return: float of the magnitude of rms value
    '''
    N = (L-1)/2 # Number of H-bridges
    sum_steps = 0 # summation variable
    for ii in range(0, int(N), 1): # loop from 0 to N-1
        sum_steps = sum_steps + asin((2*ii+1)/(L-1))*(2*ii + 1)
    return sqrt(1 - (2/(pi*N*N))*sum_steps)

def first_harmonic_rms(L):
    '''
    Funciton to return the rms value of the first harmonic for
    the 'L' level cascade H-bridge inverter
    :param L: int for the number of levels (needs to be odd)
    :return: float of the magnitude of the rms of the first harmonic
    '''
    N = (L-1)/2 # Number of H-bridges
    sum_steps = 0 # summation variable
    for ii in range(0, int(N), 1): # loop from 0 to N-1
        sum_steps = sum_steps + sqrt(1-((2*ii+1)/(L-1))**2)
    return (8/(pi*1.0*(L-1)))*sum_steps/sqrt(2)

def main():
    '''
    Main Method
    '''
    L_array = range(3, 29, 2) # L from 3 to 27 odd integers
    for L in L_array:
        rms = rms_value(L) # get rms
        f_harm = first_harmonic_rms(L) # get first harmonic rms
        thd = sqrt(rms**2 - f_harm**2) / f_harm # calc THD
        print("Levels: ",L, "Vrms: ",rms, "V,1,rms: ",f_harm , "THD: ", thd)

if __name__ == "__main__":
    main()