In-sensor optoelectronic computing using electrostatically doped silicon

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Complementary metal–oxide–semiconductor (CMOS) image sensors allow machines to interact with the visual world. In these sensors, image capture in front-end silicon photodiode arrays is separated from back-end image processing. To reduce the energy cost associated with transferring data between the sensing and computing units, in-sensor computing approaches are being developed where images are processed within the photodiode arrays. However, such methods require electrostatically doped photodiodes where photocurrents can be electrically modulated or programmed, and this is challenging in current CMOS image sensors that use chemically doped silicon photodiodes. Here we report in-sensor computing using electrostatically doped silicon photodiodes. We fabricate thousands of dual-gate silicon p-i-n photodiodes, which can be integrated into CMOS image sensors, at the wafer scale. With a 3×3 network of the electrostatically doped photodiodes, we demonstrate in-sensor image processing using seven different convolutional filters electrically programmed into the photodiode network.

In complementary metal–oxide–semiconductor (CMOS) image sensors1,2, the front-end silicon photodiode array converts light into electrical currents. These electrical data undergo analogue-to-digital conversion and are then shuttled to a digital back-end for image processing. Although this standard sequence of front-end image capture and back-end processing restricts the role of the photodiode array to sensing, emerging machine vision applications would benefit from data processing within the photodiode array to sensing, emerging machine vision of front-end image capture and back-end processing restricts the analogue-to-digital conversion and are then shuttled to a digital back-end for image processing. This in-sensor computing requires an electrical modulation or programming of photocurrents and has recently been demonstrated with electrostatically doped photodetectors whose photocurrents can be modulated with gate biasing3–15. These works have created electrostatically doped photodetectors by gating two-dimensional transition metal dichalcogenide layers or their van der Waals stacks12–14. Such in-sensor computing is not possible with current CMOS image sensors because they employ chemically doped silicon photodiodes whose photocurrents are not amenable to electrical modulation.

In this Article, we report in-sensor computing using an array of electrostatically doped silicon p-i-n photodiodes. We fabricate thousands of dual-gate silicon p-i-n photodiodes at the wafer scale, and then perform in-sensor computing on serial optical images using a 3×3 network of the electrostatically doped photodiodes by electrically programming the network into seven different convolutional filters. Our photodiodes could be integrated with CMOS image sensor electronics by replacing the chemically doped silicon photodiode array, potentially accelerating the practical application of in-sensor computing14,15,16.

Electrostatically doped silicon photodiodes

The photocurrent of a diode \(I_{ph}\) grows with the power of incident light \(P\) where responsivity \(R\) is the proportionality constant1, that is, \(I_{ph} = RP\). A conventional, chemically doped photodiode exhibits a constant responsivity \(R\), since the parameters that determine \(R\), especially the doping densities of the p and n regions, are fixed. On the other hand, in an electrostatically doped photodiode, where the doping densities can be modified by gate biasing, \(R\) is electrically programmable (as an aside to draw a parallel for a broader perspective, we note that light-emitting diodes have been also controlled by gate biasing3,17). The electrostatically doped photodiode can, thus, perform analogue multiplication between incident light power \(P\) and electrically programmed responsivity \(R\). This programmable optoelectronic analogue multiplication is the key to in-sensor image processing.

Our electrostatically doped photodiode is built on an intrinsic silicon wafer. It contains two contact electrodes—namely, electrodes 1 and 2—to provide the current path, and two top gate metals, which, when biased with the same voltage magnitude of opposite signs, create electrostatically doped p and n regions in silicon (Fig. 1a,b). The part of silicon without any overlying gate metal is an intrinsic (i) region, and acts as a channel in the device. This channel region is directly exposed to light from above. The contact and gate electrodes are arranged in an interdigitated fashion for a high channel width/length ratio of 5,576/5\(\mu\)m, with the active region of the diode occupying an area of 300\(\mu\)m×300\(\mu\)m (all the diodes presented in this paper have the same design and dimensions as described here). Detailed fabrication steps are described in Methods and Supplementary Fig. 1. The resulting p-i-n diode exhibits a standard rectifying behaviour (Supplementary Fig. 2), which

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confirmed the electrostatic doping. As we swap the signs of the two gate biases, the rectifying behaviour flips its polarity (Supplementary Fig. 2), which further verifies the electrostatic doping.

Illumination of the intrinsic channel region by light with a photon energy higher than the silicon bandgap (~1.12 eV), or equivalently with a free-space wavelength smaller than 1,100 nm, generates a photocurrent. For this photocurrent generation mode, throughout this work, we bias both contact electrodes at zero voltage and define the current flow from electrode 1 to 2 as positive. The genesis of the photocurrent is the electrons and holes excited by light, which are swept across the device with a 0.5 V step, and simultaneously the voltage at the gate above electrode 1 is stepped up from –3.0 to 3.0 V with a 0.5 V step, whereas the voltage at the gate above electrode 2 (V_{G,2}, red; V_{G,1}, not shown). A red-filtered halogen lamp (P_{source} = 15 μW) is used as the light source, V_{G,1} is stepped up from ~3.0 to 3.0 V with a 0.5 V step, and V_{G,2} is simultaneously stepped down from 3.0 to ~3.0 V with a 0.5 V step.

**Fig. 1 | Electrostatically doped silicon p–i–n photodiode.** a, Optical microscopy (top), scanning electron microscopy (SEM, middle; scale, 100 μm) and atomic force microscopy (AFM, bottom; scale, 10 μm) images of an electrostatically doped p–i–n photodiode prototype. Contact electrodes 1 and 2 and two gate electrodes above (false coloured with blue and red shades in the SEM and AFM images) are interdigitated. b, Part of the SEM image of the device (top) and the corresponding schematic (bottom) of the cross-sectional view of the photodiode, gate biased to form p–i–n and n–i–p configurations. Supplementary Fig. 4 provides a more realistic spatial profile of the electron concentration under gate biasing. c, Measured photocurrent with pulsed light (blue) and stepped gate voltages (V_{G,1} = 3.0 V, V_{G,2} = –3.0 V with a 0.5 V step, and simultaneously the voltage at the gate above electrode 1 (V_{G,1} = 3.0 V, V_{G,2} = –3.0 V with a 0.5 V step, whereas the voltage at the gate above electrode 2 (V_{G,2}) is stepped down from 3.0 to ~3.0 V with a 0.5 V step. The optical power of the light source, P_{source}, is 15 μW, which is different from, but proportional to, the power P of the light incident on the device, scaled according to the device and/or beam area. The measured photocurrent (Fig. 1c) exhibits the expected modulation of R by the gate-bias voltages. Repetition of such gate-controlled photocurrent modulation for ~50 min shows the stability of the programmability in R (Supplementary Fig. 3).

COMSOL Multiphysics simulation also confirms the operating principle of the electrostatically doped p–i–n diode. The gating clearly creates p and n regions, with band bending across the channel (Supplementary Fig. 4a–c) and responsivity R changing with the gating, as expected (Supplementary Fig. 4d).

**Programmable optoelectronic multiplication**

We further investigate the dependence of the photoresponse on the gate voltages as well as on the light power (Fig. 2a). Figure 2b shows the photocurrent map with two independently swept gate voltages, each from –5.0 to 5.0 V with a step of 0.1 V, whereas the photodiode is illuminated by blue laser light (473 nm) with a fixed P_{source} of 125 μW. When the two gate voltages are identical, that is, V_{G,1} = V_{G,2}, whether it is positive (n–n doping) or negative (p–p doping), no overall potential gradient develops and thus no photocurrent should be produced. The corresponding p–p to n–n line, with zero current, is indeed close to the ideal positive diagonal line, and its slight deviation is possibly due to charge carrier trapping at defects formed during fabrication. On the other hand, when we sweep the two gate voltages at the same magnitude, but with opposite signs, along the negative diagonal line, the photocurrent monotonically increases from the negative maximum to the positive maximum, which is consistent with the monotonic change in V_{th} from the...
negative maximum to the positive maximum (Fig. 1b). Figure 2c plots this photocurrent response along the negative diagonal line as a function of $V_{G,1} = -V_{G,2}$, which we denote as programming voltage $V_p$. This measured dependence of the photocurrent on $V_p$ is also qualitatively consistent with the COMSOL Multiphysics simulation (Supplementary Fig. 4d). From here on, all the gate biasing is configured as $V_p = V_{G,1} = -V_{G,2}$.

Moreover, we demonstrate the linear dependence of $I_{ph}$ on $P_{e}^{source}$—and therefore on $P$—for any given $R$ programmed by tuning $V_p$. This linearity is important for high-fidelity analogue multiplication between $P$ and a given $R$. Figure 2d shows the measured $I_{ph}$ as a function of $P_{e}^{source}$ (red-filtered halogen lamp) for various $V_p$ (and thus $R$) values. A simple linear fit yielding a high coefficient of determination (0.996 averaged across all the $V_p$ values) confirms the linear dependence of $I_{ph}$ on $P_{e}^{source}$, and thus on $P$, for each programmed value of $R$. Linearity is also confirmed for different wavelengths of incident light (Supplementary Fig. 5).

**Wafer-scale fabrication and characterization**

Electrostatically doped silicon photodiodes may accelerate the real-world realization of in-sensor computing due to their suitability for large-scale integration with CMOS electronics. As a demonstration, we fabricated, in-house, 4,900 of the dual-gate p–i–n silicon photodiodes on a four-inch silicon wafer (Fig. 3a, left) using CMOS-compatible fabrication (Methods). The fabricated wafer features $7 \times 7 = 49$ reticles, with each reticle containing $10 \times 10 = 100$ photodiodes (Fig. 3a, right).

Figure 3b shows the photocurrent maps obtained by illuminating a 400 nm LED light with a fixed $P_{e}^{source}$ of $170 \mu W$ serially—diode by diode—across an example reticle containing 100 photodiodes, for various $V_p$ values (−5 to 5 V with a 2 V step; clockwise from right, top corner). These maps show a high device-to-device uniformity in the responsivity programming within the reticle. In the wafer-scale photocurrent measurement of a $5 \times 7$ reticle array (3,500 photodiodes) with an automated probe station with $V_p$ varied from −5.0 to 5.0 V with a 0.1 V step, 3,282 devices showed programmable responsivity (~94% yield). Concretely, as we sweep $V_p$, the photocurrents of the 3,282 devices, in response to the 400 nm LED light with fixed $P_{e}^{source}$ of $170 \mu W$, varied from $-380 \pm 50$ to $430 \pm 47 nA$ (Fig. 3c).

Figure 3d shows the distribution of the 3,282 photocurrents for selected $V_p$ values (−5 to 5 V with a 1 V step), where device-to-device variations are more pronounced than those from the single reticle, which is standard at the wafer scale.

**In-sensor optoelectronic convolutional image processing**

As shown in Fig. 4a, we also fabricated a $3 \times 3$ network of connected photodiodes with a diode-to-diode pitch of $\sim 3$ mm to perform analogue multiplication between the incident light power and the programmed responsivity in each photodiode, and to sum, or accumulate, the resulting nine photocurrents via Kirchhoff’s current

**Fig. 2 | Programmable photoresponse of the dual-gate silicon p–i–n photodiode.** a, Schematic of the measurement setup. Incident light with power $P$—that is, $P_{e}^{source}$ scaled according to the device and/or beam area—is converted to photocurrent $I_{ph}$, which is modulated by the two gate voltages $V_{G,1}$ and $V_{G,2}$. b, Photocurrent map measured by sweeping each gate voltage from −5.0 to 5.0 V with a 0.1 V step. Since there are 101 swept voltages for $V_{G,1}$ and 101 swept voltages for $V_{G,2}$, the map consists of a total of 10,201 points. c, Photocurrent response with $V_p = V_{G,1} = -V_{G,2}$ swept from −5.0 to 5.0 V with a 0.1 V step. The light source for b and c is a blue laser (473 nm) with $P_{e}^{source} = 125 \mu W$. d, Measured photocurrent versus $P_{e}^{source}$ with $V_p$ as a parameter, varied from −4 V (blue) to 4 V (red) with a 1 V step. The light source is a red-filtered halogen lamp.
law. The photocurrent sum resulting from this analogue multiply–accumulate operation is a dot product between the \(1 \times 9\) incident light power vector and the \(9 \times 1\) vector of programmed responsivities. Consequently, the nine-photodiode network (Fig. 4a) serves as an optoelectronic convolutional processor, with the \(9 \times 1\) vector of programmed responsivities—or equivalently the \(3 \times 3\) map of responsivities programmed across the photodiode array—serving as an image filter kernel (our choice of the \(3 \times 3\) kernel is to follow the widely used practice\(^{11,21–26}\)). The accumulated photocurrent is converted to an output voltage \(V_{\text{out}}\) via a transimpedance amplifier on a printed circuit board. Supplementary Fig. 6 shows our measurement system.

With an image filter kernel programmed, the nine-photodiode network not only captures an input scene but also processes it simultaneously. Figure 4b–d shows an example demonstration where the network finds the edges of a moving light spot. We program the photodiode network to feature the specific responsivity map shown in Fig. 4b by independently tuning \(V_p\) of each photodiode (Methods). This filter kernel is designed for edge detection along the \(x\) axis, resulting in positive and negative photocurrents when the photodiode network is at the right and left edges of the light spot, respectively, and otherwise negligible photocurrents. Figure 4c shows \(V_{\text{out}}\) monitored with a light spot from a liquid-crystal display (LCD) projector (power set to 255 out of 255, green channel only) moving from left to right across the whole array at a frequency of 4 Hz. An optical chopper with an aperture diameter of \(\sim 2.5\) cm, rotating in front of the projector, effectively moves the light spot, demonstrating the consistent positive (6 V) and negative (\(-6\) V) responses as the spot moves over the array. We have evaluated this dynamic processing up to a spot movement frequency of 500 Hz (Fig. 4d), which is the maximum speed of our optical setup. The electrostatically doped diode itself has a photoresponse time (rise time) of, at most, 3 ns in a conservative measure (Supplementary Fig. 7).

Expanding from the simple example above, we perform in-sensor processing of a \(256 \times 256\) pixel image (Fig. 5a, grey scale; 8-bit depth, from the USC-SIPI image database\(^{29}\)) with the contrast-inversion filter kernel (Fig. 5b) programmed into the nine-photodiode network (Methods). The details of the optical setup here are different from those shown in Fig. 4. Concretely, a \(3 \times 3\) patch of the image is illuminated onto the photodiode network using \(3 \times 3\) light spots from an LCD projector (green channel only), with each light spot having a diameter of \(\sim 500 \mu\)m falling only on one diode. This results in an accumulated photocurrent as the outcome of the optoelectronic convolution. By sliding the \(3 \times 3\) patch through the \(256 \times 256\) image and repeating the optoelectronic convolution, we generate a \(254 \times 254\) matrix of accumulated photocurrents (a total of 64,516 accumulated photocurrents), which represents the image (Fig. 5c) processed with the contrast-inversion filter kernel.

Besides the contrast-inversion filtering, we have repeated in-sensor image processing using six other widely used filter kernels\(^{11,21–26}\): difference of Gaussians, Gaussian blurring, image sharpening, box blurring, horizontal Sobel and vertical Sobel filters (Supplementary Fig. 8). As the 63 photocurrent values programmed with a fixed \(P_{\text{source}}\) from the LCD projector (green channel only; nine values per filter and a total of seven filters), which correspond to the 63 programmed \(V_p\) values, are compared with their target values, which range from \(\sim 2\) to \(4\) mA, the maximum error was 18 nA. Since the ratio of the maximum error to the target range, \(1/333\), is between \(1/2^3\) and \(1/2^4\), the programming accuracy is 8 bits. The images shined with the LCD projector (green channel only) and processed with these filter kernels are shown in Fig. 5d, bottom; the Sobel-filtered image in Fig. 5d, bottom, is a composite produced by
the root sum of squares of the horizontal and vertical Sobel-filtered images (Supplementary Fig. 9)\(^21\). The juxtaposition of these images processed in the analogue domain within the photodiode array (Fig. 5d, bottom) with those computed digitally (Fig. 5d, top) unequivocally verify our in-sensor computing scheme.

**Conclusions**

Bioinspired computing has driven increasing levels of global research into in-memory computing inspired by the co-location of memory and computing in the brain, as well as in-sensor computing inspired by the brain's sensory peripheral systems where sensing is combined with early information processing\(^3,4,10,11,24,27–32\). In in-sensor computing, data processing in image sensors is a key focus due to the importance of visual data and the prevalence of its production. Previous work\(^3,11\) pioneered the strategy of using electrostatically doped photodetectors for data processing in image sensors and demonstrated it with two-dimensional material photodetectors. In this work, we have adopted this strategy and applied it to silicon photodiodes, creating an electrostatically doped silicon photodiode array for data processing in image sensors. Due to its compatibility with mainstream CMOS electronics infrastructure, this silicon-based approach could accelerate the practical development of in-sensor computing.

Future work on this system should focus on the monolithic integration of the electrostatically doped silicon photodiode array with control electronics using CMOS foundry fabrication. The large area of the electrostatically doped photodiode we have fabricated here can be scaled down with foundry-grade processes. Similarly, the gate-bias (\(V_p\)) range (–5 to 5 V) in our devices with a 30-nm-thick gate dielectric can be substantially reduced by decreasing the gate dielectric thickness to a few nanometres, which is routinely done in CMOS processes (as shown in Supplementary Fig. 10, optimization of other fabrication steps, besides the gate-dielectric thickness, can already reduce the gate-bias range below –1 to 1 V). Also, using CMOS processes, the array size can be expanded from 3\(^x\)3 not only to capture a whole input scene at once but also to enable high-throughput in-sensor processing on the captured image by running, in parallel, several duplicated filter kernels across the array. Such a large-scale array would require a large number of interconnects and control electronics, which can be readily implemented with CMOS processes.

**Methods**

**Electrostatically doped silicon photodiode fabrication.** Device fabrication began with wafer cleaning by dipping a four-inch undoped Si wafer with 200 nm thermal oxide (Biotain Hong Kong; resistivity; >10,000\(\Omega\cdot\)cm) in a piranha solution (\(\text{H}_2\text{SO}_4\cdot\text{H}_2\text{O}_2 = 3:1\)) at 80\(^\circ\)C for 10 min. To build a device on a Si surface,
the device fabrication area is defined through conventional photolithography. Hexamethyldisiloxane is employed in advance to the photoresist to prevent undercut during a wet-etch process. A spin-rinse dryer is used for wafer drying through all the processes. Then, 200 nm of thermal oxide is etched using buffered oxide etchant (6:1) for 3 min. The pattern is stripped by acetone, isopropyl alcohol and spin-rinse dryer. Contact electrodes (Cr/Au 10/25 nm) are formed by a conventional lift-off process using electron-beam evaporator. A lift-off resistor (LOR 3A) is employed for a higher fabrication yield. Then, 30 nm Al2O3 gate dielectric is deposited using atomic layer deposition at 250 °C (base pressure, 220 mtorr; trimethylaluminium (TMA) precursor pulse time, 0.015 s; water vapour oxidant pulse time, 0.015 s; purging time between precursor and oxidant, 8,000 s). After via formation by patterning with hexamethyldisiloxane and buffered oxide etchant (1 min), gate electrodes (Cr/Au 10/250 nm) are formed by the lift-off process.

**Iterative programming.** Although all the pixels are exposed to constant, maximum light from the LCD projector (255 for the 8-bit range, green channel only), \( V_k \) for each pixel is set to a calculated \( V_k \) value for the \( k \)th iteration cycle, for each of the nine pixels. We keep modulating \( V_k \) until the difference between \( I_{\text{target}} \) and \( I_k \) is less than the allowed error range, that is, 23 nA if we set an 8-bit accuracy for the full range of 6 μA.

**Data availability**

Source data are provided with this paper. The data that support the other findings of this study are available from the corresponding authors upon reasonable request.

**Code availability**

Experimental code is available from the corresponding authors on reasonable request.

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**Fig. 5 | In-sensor image processing using the 3 × 3 dual-gate p-i-n photodiode network.**

- **a.** A 256 × 256 input image (left) and its example portion (top, right). The bottom right is an example of a 3 × 3 patch from this input image, which is projected onto the 3 × 3 photodiode network.
- **b.** Programmed photocurrent map with a fixed power of light—that is, a responsivity map—for contrast-inversion filtering. The maximum LCD projector brightness (255 out of 255, green channel only) is used for this programming.
- **c.** The 254 × 254 map of accumulated photocurrents with the nine-photodiode network programmed as in b, where the 64,516 accumulated photocurrents are serially obtained by illuminating, using the LCD projector (green channel only), the photodiode network with a 3 × 3 patch sliding through the 256 × 256 input image.
- **d.** Various filtered images obtained with digital computing (top) and in-sensor computing (bottom).

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Author contributions
H.J., H.H., S.P. and D.H. conceived and designed the experiments. H.J., M.P. and S.-K.L. designed and fabricated the electrostatically doped silicon photodiodes. H.H. designed the interface electronics. H.J., H.H., M.P. and S.-K.L. performed the measurements of individual dual-gate p–i–n photodiodes. H.J. and H.H. performed the in-sensor image processing. M.-H.L. and C.K. performed the wafer-scale measurements. W.-B.J. performed the COMSOL Multiphysics simulations on the dual-gate p–i–n photodiode. H.J., H.H., W.-B.J., M.-H.L., C.K., M.P., S.-K.L. and D.H. analysed the data. S.P. and D.H. supervised the project. H.J., H.H. and D.H. wrote the article. All the authors discussed the results and implications, and reviewed the article.

Competing interests
The authors declare no competing interests.

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