Junctionless Dual In-Plane-Gate Thin-Film Transistors with AND Logic Function on Paper Substrates

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ABSTRACT: Dual-gate thin-film transistors (DGTFTs) have attracted increasing attention in the past few years because of threshold voltage modulation and device logic functionality. Here, solution-processed chitosan-based proton conductors are used as the gate dielectric. The threshold voltage shift depends on the ratio of the capacitances of the two gate dielectrics. The second interesting application of DGTFTs is logic functionality. This device demonstrates AND logic function controlled by applying either 0 or −1 V to each of the gate electrodes. When both gates were simultaneously applied to be 0 V, the current flows (ON). Otherwise, the current is blocked (OFF). In order to provide a comprehensive overview of these paper devices, the planarization of paper surface and switching stability of such DGTFTs are all discussed.

1. INTRODUCTION

In 1981, one of the first dual-gate thin-film transistors (DGTFTs) based on CdSe was reported by Luo et al.1 From then on, many kinds of DGTFTs were reported.2–5 The advantages of DGTFTs reported by many researchers are steeper subthreshold slope and increased gate modulation. The second gate electrostatically modifies the charge carrier distribution in the channel accumulated by the first gate, so the second gate can set threshold voltage ($V_{th}$) accurately.6 The threshold voltage can be set as a function of the applied biases, and the effective threshold voltage shift depends on the ratio of the capacitances of the two gate dielectrics. Besides setting the threshold voltage to modulate the operation mode of DGTFTs, such devices are demonstrated as AND gates. Several circuit applications of utilizing DGTFTs have already been reported;7–9 however, it does not make full use of all the special advantages of DGTFTs. Numerous logic circuits which are widely used in devices require multiple inputs, while this functionality can be achieved by using a single DGTFT. Hence, the number of transistors required in many digital applications is reduced and the circuits are simplified. These advantages can be used to realize new functional devices.

Recently, a new kind of transistor, called junctionless transistor, has been reported.7–9 In this paper, all the channel and source/drain electrodes of such junctionless DGTFTs are realized by a thin indium tin oxide (ITO) film without any source/drain junction formation. Such a junctionless paper transistor shows high promise for future electronics application because of simple device process and low-cost paper substrates. Paper is an intriguing alternative to fulfill low-cost demand because it is ubiquitous in daily life and the cheapest flexible substrate. Moreover, paper is also environmentally friendly because it is recyclable and made of renewable raw materials.10 However, the paper surface is rough and porous; until now, it is still a challenging test to fabricate TFTs on the paper substrate. To solve this problem, the SiO$_2$ film is used as a buffer layer to realize planarization of paper surface, which has been discussed in our previous paper.11 TFTs on paper substrates with higher than 10 V operation voltage have been reported by several groups;12,13 however, the device performance and stability are still far from satisfaction to be used for portable applications. Thus, to fabricate a low-voltage paper TFT, novel gate dielectric materials that offer both high gate-specific capacitance and low-temperature processability are in high demand. Recently, polymer electrolytes14 and inorganic nanogranular electrolytes15 with huge electric double layer (EDL) capacitances have been reported. In this paper, solution-processed chitosan films with huge EDL gate-specific capacitance are used as the gate dielectric layers. The major advantage of the EDL effect in chitosan dielectric is that the specific capacitance is extremely large at low frequencies, so that a small gate voltage variation ($\sim$1.5 V) could induce several orders of magnitudes change in the drain current.

2. RESULTS AND DISCUSSION

The schematic diagram of the proposed junctionless dual in-plane-gate paper TFTs is shown in Figure 1a. The capacitance of DGTFTs can be coupled by the bottom ITO layer has been reported by our previous work.16 As shown in Figure 1b, three capacitors (C1, C2, and C3) are coupled by the bottom ITO
layer (G1), and the operation mechanism of such DGTFTs is demonstrated by the equivalent circuit. Thus, the channel current $I_{DS}$ controlled by one gate electrode (G2) can be modulated by the other gate electrode (G3). In order to understand the operation mechanism of the junctionless dual in-plane-gate paper TFTs, the specific capacitance of chitosan dielectric is measured. As shown in Figure 1c, when decreasing frequency, the capacitance of chitosan dielectric increases and reaches to $3.7 \mu F/cm^2$ at 20 Hz. The gate leakage current is shown in Figure 1d, and an ultralow leakage current (<80 pA) was observed.

Figure 2a shows the transfer curves of such junctionless DGTFTs with different channel thicknesses ($T_{ITO} = 5, 20, 40,$ and $60$ nm) at a fixed $V_{DS} = 1.5$ V. The bottom gate (G1) has no modulation effect on the channel current ($I_{DS}$) when $T_{ITO} = 5, 40,$ and $60$ nm. However, the bottom gate shows effective modulation effect on the channel current when $T_{ITO} = 20$ nm. The subthreshold swing (S) and current on/off ratio ($I_{on}/I_{off}$) were calculated to be 0.12 V/dec and $5.8 \times 10^6$, respectively. The channel length is 1 mm, the channel width is 0.15 mm, the specific capacitance of chitosan dielectric is $3.7 \mu F/cm^2$, $I_{DS} = 7 \mu A$ at $V_{G1} = 1.5$ V and $V_{th} = 0.1$ V, according to the equation of $I_{DS} = (W/C_{i})/(V_{G1} - V_{th})^2$, and the field-effect mobility ($\mu_{sat}$) is calculated to be $12.8 \ cm^2/Vs$. Figure 2b shows the output curves of such junctionless DGTFTs with 20 nm channel thickness, and the bottom gate voltage increased from −0.5 to 1.5 V. It reveals excellent linear characteristics at low drain/source voltage and good current saturation behaviors at high drain/source voltage. The transfer characteristics with a constant $V_{DS}$ of 1.5 V of such junctionless DGTFTs is shown in Figure 3a, which shows that the transfer curves would shift from negative direction to positive direction when the secondary gate voltage decreased from 2.0 to −2.0 V.

The threshold voltage ($V_{th}$) of such junctionless DGTFTs on paper substrates is shown in Figure 3b. The $V_{th}$ of such junctionless DGTFTs would change from −0.53 to 0.97 V when the secondary gate ($V_{G3}$) voltage decrease from 2.0 to −2.0 V, so the operation mode of such junctionless DGTFTs change from depletion to enhancement. The threshold voltage ($V_{th}$) modulation effect of the secondary gate (G3) voltage could be explained as follows. The channel would be more conducting when a positive voltage was applied on the secondary gate (G3), so a negative voltage has to be applied on the first gate (G2) to modulate the channel current, which makes the subthreshold voltage shift to negative direction. Otherwise, the channel would be depleted when a negative voltage was applied on the secondary gate (G3), so a positive voltage has to be applied on the first gate (G2) to modulate the

Figure 1. (a) Schematic picture of junctionless dual-gate paper TFTs. (b) Equivalent circuit of such junctionless DGTFTs. (c) Specific gate capacitance of junctionless dual-gate paper TFTs. (d) Leakage current of such TFTs.

Figure 2. (a) $I_{DS}$−$V_{GS}$ curves of junctionless DGTFTs on paper substrates with various channel thicknesses ($T_{ITO} = 5, 20, 40,$ and $60$ nm) at $V_{DS} = 1.5$ V. (b) $I_{DS}$−$V_{DS}$ curve for a fresh device with $T_{ITO} = 20$ nm.
channel current, which makes the subthreshold voltage shift to positive direction. When the secondary gate (G3) voltage changes from 2.0 to −2.0 V and the first gate (G2) voltage is a constant value of 0 V, the circuit model shown in Figure 1b could be equivalent to the combination of C3 and a parallel capacitance (C1 and C2). If considering the width of gate electrodes, the values of these three capacitances should be approximately equal (C1 ≈ C2 ≈ C3). The voltage change ratio between the bottom gate (G1) and the secondary gate (G3) should be equivalent to C3/[C3 + (C1 + C2)] = 1:3, which is consistent with the experimental data [0.97 − (−0.53)]/[2 − (−2)] = 1:2.7. Because of the sensitivity of Vth to the secondary gate (G3) voltage, such junctionless DGTFTs are very potential for sensor applications based on ion-sensitive thin-film transistors. In this paper, the values of C1 and C2 are changeable at different secondary gate (G3) voltages, which lead to the asymmetric shift behavior of threshold voltage (Vth). The gate electrodes would be highly conducting when a positive voltage was applied on the secondary gate (G3); at this time, C1 and C2 were equivalent to the huge specific EDL capacitance of chitosan dielectric. However, C1 and C2 would be smaller because of the depletion effect caused by the negative voltage applied on the secondary gate (G3), so a negative secondary gate voltage would lead to a larger shift of threshold voltage (Vth) based on this equation of ΔVth = ΔV G3C3/[C3 + (C1 + C2)].

The threshold voltage and current on/off ratio are shown in Figure 4a, where the threshold voltage decreases with increasing secondary gate (G3) voltage. However, the current on/off ratio remains constant at different secondary gate (G3) voltages. The field-effect mobilities and subthreshold swings are shown in Figure 4b, where the field-effect mobility decreases from 1.54 to 1.04 cm²/Vs when the secondary gate (G3) voltage decreases from 2.0 to −2.0 V. However, the subthreshold swing remains a constant at different secondary gate (G3) voltages, which indicates that the subthreshold swing was hardly affected by the secondary gate (G3) voltage.

In order to find out whether electrochemical doping existed in the ITO channel layer during the fabrication process, low-frequency pulse respond characteristic is shown in Figure 5a. The current on/off ratio remains a constant of ∼10⁷ without on current decrease, which indicates that no chemical doping or chemical reaction occurs at the chitosan/ITO interface because IDS would decrease after gate scanning when chemical doping or chemical reaction occurred. To demonstrate the

![Figure 3](image3.png)

Figure 3. (a) Transfer characteristics of such junctionless DGTFTs on paper substrates with V G3 ranging from 2 to −2 V. (b) (IDS)¹/² vs V G3 curves.

![Figure 4](image4.png)

Figure 4. (a) Vth and I on/I off ratio of such DGTFTs on paper substrates at different V G3. (b) μ and S of such DGTFTs on paper substrates at different V G3.

![Figure 5](image5.png)

Figure 5. (a) Low-frequency pulse respond characteristic of the device with V G2 = −0.5 to 1.5 V, V G3 = 0 V, and V DS = 1.5 V. (b) AND logic function with a large I on/I off.
logic function of such junctionless DGTFTs, different voltage pulse sequences were applied on the dual in-plane gates used as inputs and the drain/source current $I_{DS}$ used as the output, which are shown in Figure 5b, where $V_T$ is the voltage of the transistor, and the current on/off means the device is OFF. This is exactly AND logic function of such junctionless DGTFTs on paper substrates were studied. The threshold voltage of such junctionless DGTFTs could be effectively modulated from negative ($-0.53$ V) to positive ($0.97$ V) when the secondary gate (G3) voltage changed from $-0.7$ V to $0.53$ V. Such junctionless DGTFTs on paper substrates with AND logic function are very potential for paper sensor applications.

3. CONCLUSIONS
In conclusion, the dual-input AND logic gate based on a single DGTFT was experimentally demonstrated. The dual-gate electrostatic modulation and low-voltage operation mechanism of the junctionless DGTFTs on paper substrates were studied. The threshold voltage of such junctionless DGTFTs could be effectively modulated from negative ($-0.53$ V) to positive ($0.97$ V) when the secondary gate (G3) voltage changed from $-0.7$ V to $0.53$ V. Such junctionless DGTFTs on paper substrates with AND logic function are very potential for paper sensor applications.

4. EXPERIMENTAL SECTION
The paper substrates used for oxide-based TFT arrays were ink-jet printing papers. Radio-frequency (RF) magnetron sputtering and plasma-enhanced chemical vapor deposition were used for the fabrication of junctionless paper TFTs gated by solution-processed chitosan dielectrics. The entire process was performed at room temperature. First, a $2.0 \mu m$ microporous SiO$_2$ film was deposited on paper substrates for surface passivation, the performance of TFTs can be improved by the smooth surface and interface of paper substrates. Second, a $200 nm$ ITO film was deposited on passivated paper substrates by RF magnetron sputtering at $0.5$ Pa. Third, the dielectric layer was fabricated by chitosan solution ($2 \ wt \%$ in acetic acid) and dried in ambient air. At last, ITO source/drain and dual in-plane gate electrodes were completed by RF sputtering through a nickel shadow mask. Electrical characterizations of the junctionless paper TFTs and chitosan dielectric were performed by an impedance analyzer (Agilent 4294A) and a semiconductor parameter analyzer (Keithley 4200 SCS).

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Thin-film transistor and device performance was fabricated and characterized by W.D. The manuscript was prepared by W.D and Y.T. W.D examined and commented on the manuscript. The project was guided by W.D.

Notes
The authors declare no competing financial interest.

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