The design of a time-interleaved analog–digital conversion modulator based on FPGA-TDC for PET application

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Abstract—Fully Field Programmable Gate Array (FPGA) based digitizer for high-resolution time and energy measurement is an attractive low-cost solution for the readout electronics in positron emission computed tomography (PET) detector. In recent years, the FPGA based time-digital converter (FPGA-TDC) has been widely used for time measurement in the commercial PET scanners. Yet, for the energy measurement, few studies have been reported on a fully FPGA based, large dynamic range and high resolution alternative to the commercial analog–digital converter (ADC). Our previous research presents a 25 Ms/s FPGA-TDC based free-running ADC (FPGA-ADC), and successfully employed it in the readout electronics for PET detector. In this work-in-progress study, by means of the time-interleaved strategy, a 50 Ms/s FPGA-ADC is presented. With only two off-chip resistors, both the A/D conversion and energy measurement are achieved on a Xilinx Kintex-7 FPGA. Therefore, this method has great advantages in improving system integration. Initial performance tests are also presented, and we hope it can give us a possibility to develop a new FPGA-only front-end digitizer for PET in future.

Keywords—FPGA, PET, ADC, TDC, energy measurement

I. INTRODUCTION

A positron emission computed tomography (PET) detector module needs to measure the arrival time, energy, and position of the incident 511-keV photon [1]. To identify tiny scintillator elements for high spatial resolution, a PET scanner requires tens of thousands of readout channels. Power consumption and density become challenging issues when the readout electronics system scales up. Although Application Specific Integrated Circuit (ASIC) technology can be resorted to solve the problem, its long development cycle and high cost is not feasible for laboratory experiments [2]. Thus, in many applications, light-sharing technique based on a multiplexing network with discrete components is still a common choice to reduce the number of signal processing channels [3-4]. Even so, the number of readout channels is still very large for a general PET scanner. There is a strong demand for simple and efficient readout electronics to use in the development of a compact and cost-effective PET system.

Researches in recent years succeed in integrating high-resolution time-digital converters into the field programmable gate array device (FPGA-TDC), which makes the time measurement much cheaper and simpler [5]. Nevertheless, the energy measurement is commonly based on a commercial high speed analog–digital converter (ADC) chip to digitalize the analogue signals, which certainly leads to high system power consumption and cost. So far the most common alternative solution is time-over-threshold (TOT) method which compares the integral signal with a pre-set threshold to translate the signal amplitude into a TOT time width measured with TDC [6]. For some one-to-one readout or hybrid charge division systems, it can be used because the pulse shape does not change with respect to position. However, its drawbacks of nonlinearity, small dynamic range, and low SNR make it impractical for high precision measurement especially in light-shared systems. Another method is called multi-voltage threshold (MVT) for digitizing a PET event by sampling with respect to certain reference voltages. By fitting the mathematical model of SiPM signals to the several sampled pulses, a high energy resolution with low dead time can be obtained. Nevertheless, MVT circuit consumes lots of comparators or FPGA I/Os [7]. Thus, it is still a great challenge to achieve high resolution energy measurement over a large dynamic range without an ADC chip.

We previously reported a 25 Ms/s FPGA-TDC based free-running ADC (FPGA-ADC), and successfully employed it in the readout electronics for both one-to-one coupled and light-shared PET detectors based on SiPM and LYSO arrays [8]. This simple FPGA-ADC based on a carry chain TDC implemented on a Kintex-7 FPGA consists of only one off-chip resistor and two FPGA I/Os so it has greater advantages in improving system integration and reducing cost than commercial chips. However, due to the low sampling rate of these ADC, we have to employ an analogue shaper to widen the signals (~600 ns) from SiPMs, which certainly increases system complexity and deteriorates the system’s dead time and pipe up performance. To optimized the sampling rate performance, by means of the time-interleaved strategy, this work-in-progress study presents a 50 Ms/s FPGA-ADC. With only two off-chip resistors, both the A/D conversion and energy measurement are achieved on a Xilinx Kintex-7 FPGA. Compared with the TOT and MVT circuit, this method does not need additional digital-analog converter (DAC) or other active device, and we can get the real-time waveforms of the analogue signals. The electronics evaluation test results are presented, and an initial experiment was also conducted using a single LYSO crystal under 22Na point source excitation. We hope it can give us a possibility to develop a new FPGA-only front-end digitizer for PET in future.
II. PRINCIPLE AND CIRCUIT DESIGN

A. Time-interleaved FPGA-ADC modulator

![Figure 1 structure of the time-interleaved modulator](image)

The structure of the presented time-interleaved FPGA-ADC is shown in Figure 1. Two clocks with a phase shift of 180°, synthesized by the internal phase locked loop (PLL), are separately filtered to a quasi-triangular sampling ramp by a simple low pass filter formed by a serial resistor (Rs) with the parasitic capacitance (Cp) at the input of the user I/O ports. The analogue input signal is discriminated by the sampling ramps using the differential FPGA I/Os working in LVDS receiver mode and the width of the output digital pulses can be used to characterize the voltage amplitude of the analog signals. The discriminated widths are then measured by two following carry chain TDCs. Compared with the previous single sampling scheme, the time-interleaved modulator doubles the sampling rate. The high level of output clocks is 3.3 V.

On the basis of the precious research, the sampling frequency (Fs) of single sampling and Rs are configured as 25 MHz and 90 ohms. The circuit simulation indicates the measurable amplitude range can reach around 1.7 V (0.8 V–2.5 V). Besides, the employed TDC is normalized to 9 bits after online delay tap calibration (bin-by-bin) with an equivalent bin size of around 7.8 ps. Considering the maximum width of the measured pulses is 40 ns, the range of each single channel is larger than 12 bits.

B. Correction methods

As mentioned before, the sampling ramps are not standard triangular ramps, which would lead to large conversion nonlinearity. This nonlinearity would bring harmonics at the multiples of the input frequency. To calibrate the conversation curve, we scanned different DC levels over the measurable amplitude range and made a look-up-table (LUT, size: 4096 × 4096) stored in FPGA to conduct a simple conversation nonlinearity correction mechanism.

Besides, for a time-interleaved A/D system, it is necessary to correct the gain, phase and offset difference between sampling channels. Generally, the correction algorithms are very complicated and resource intensive, which is not appropriate for the massive channels application [9]. Considering the sampling frequency of the FPGA-ADC is not very high, in this design we corrected only the gain and offset difference between the two time-interleaved channels. We reduced the phase difference by controlling the PCB layout and the TDC’s routing constraints.

The ADC with online corrections has been implemented on a Kintex-7 FPGA (XC7K325T-2FFG900). The FPGA resource usage of one channel (including 2 TDCs with delay tap calibration, nonlinearity correction, gain&offset correction and the width calculation section) is listed in Table 1.

| Resource  | Usage | Usage/total |
|-----------|-------|-------------|
| LUT       | 3960  | 1.94%       |
| LUT RAM   | 1726  | 2.7%        |
| Block RAM | 5     | 0.12%       |
| Flip-flop | 1418  | 0.35%       |
| DSP       | 1     | 0.12%       |
| IO        | 4     | 0.8%        |

Total on-chip power: 0.384 W

III. INITIAL EXPERIMENT RESULTS

The test platform is shown in Figure 2. A signal generator is used to evaluate the ADC’s electronics performance, and then a LYSO crystal (4 mm × 4 mm × 15 mm) coupled with a 4 mm × 4 mm SiPM (J-series from ON semiconductor) under 22Na excitation (~60 μi) is tested to get the single energy spectrum. The LYSO has been polished and later covered by reflective material (Teflon). The LYSO and the SiPM are pasted with optical grease (BC630). All the measured data, controlled commands, and debug information are communicated with the Host PC via PCIE bus.
A. ADC’s dynamic performance

The signal generator outputs continuous sine waves with a nearly full voltage swing to the ADC, and the dynamic performance is shown in Figure 3. The results indicate that the effective number of bits (ENOB) is around 6 bits at 1 MHz and 4.5 bits at 5 MHz.

B. Measurement range and resolution

Figure 3 the ADC’s dynamic performance (the frequency of input is 1 MHz)

Figure 4 the measured conversation curve and resolution for the SiPM-like signals

In some light-shared PET applications, it is important to ensure the ADC’s dynamic performance and resolution over a large dynamic range. We generated the signals according to the outputs of the SiPM’s anode and the test results are shown in Figure 4. Test results indicate that the measurement integral nonlinearity (INL) is within ±1.0% without any correction and the resolution is better than 6.0% in the input range from 200 mV to 1.8 V with a 0.7 V DC offset.

C. Energy spectrum

The tested energy spectrum of $^{22}$Na is shown in Figure 5. The test results indicate that the energy resolution is around 10.5% at 511 keV before the SiPM saturation correction. The spectrum is almost the same as that acquired by the oscilloscope.

IV. Conclusion and Future Work

In this work-in-progress paper, we present a 50 Ms/s time-interleaved analog-digital conversion modulator based on FPGA-TDC. With only two off-chip resistors, all the A/D conversion and energy measurement are achieved on FPGA. Therefore, this method has greater advantages in improving system integration than traditional schemes. The initial test results indicate that this method can get a clear $^{22}$Na energy spectrum, which gives us a possibility to develop an FPGA-only front-end digitizer for PET in future.

In the next work, we will test the ADC’s performance for the crystal array, especially in the light-shared application. And then a fully FPGA based digitizer for clinical PET scanner will be developed.

REFERENCE

[1] Z. Hu et al., “An LOR-based fully-3D PET image reconstruction using a blob-basis function,” 2007 IEEE Nuclear Science Symposium Conference Record, Honolulu, HI, USA, 2007, pp. 4415–4418, doi: 10.1109/NSSMIC.2007.4437091.

[2] B. Wu, Y. Wang, Q. Cao, J. Kuang, M. Wang and X. Zhou, “An FPGA-based Time Sampling Charge Measurement Method for TOF-PET Detectors,” 2019 IEEE International Instrumentation and Measurement Technology Conference (I2MTC), Auckland, New Zealand, 2019, pp. 1-5, doi: 10.1109/I2MTC.2019.8827035.

[3] Y. Wu, C. Catana and S. R. Cherry, “A Multiplexer Design for Position-Sensitive Avalanche Photodiode Detectors in a PET Scanner,” IEEE Transactions on Nuclear Science, vol. 55, no. 1, pp. 463-468, Feb. 2008, doi: 10.1109/TNS.2007.909948.

[4] Downie E, Yang X, Peng H, “Investigation of analog charge multiplexing schemes for SiPM based PET block detectors”, Physics in Medicine and Biology, vol. 58, no. 11, pp. 3943-3964, 2013, doi: 10.1088/0031-9155/58/11/3943.

[5] N. Roy, F. Nolet, F. Dubons, M. Mercier, R. Fontaine and J. Pratte, “Low Power and Small Area, 6.9 ps RMS Time-to-Digital Converter for 3-D Digital SiPM,” IEEE Transactions on Radiation and Plasma Medical Sciences, vol. 1, no. 6, pp. 486–494, Nov. 2017, doi: 10.1109/TRPMS.2017.2757444.

[6] Chang C M, Cates J W, Levin C S, “Time-over-threshold for pulse shape discrimination in a time-of-flight phoswich PET detector,” Physics in Medicine & Biology, vol. 62, no. 1. 2017, doi: 10.1088/1361-6560/62/1/258.
[7] D. Xi, C. Kao, W. Liu, C. Zeng, X. Liu and Q. Xie, "FPGA-Only MVT Digitizer for TOF PET," IEEE Transactions on Nuclear Science, vol. 60, no. 5, pp. 3253-3261, Oct. 2013, doi: 10.1109/TNS.2013.2277855.

[8] C. Ma et al., “Design and evaluation of an FPGA-ADC prototype for the PET detector based on LYSO Crystals and SiPM arrays,” IEEE Transactions on Radiation and Plasma Medical Sciences, doi: 10.1109/TRPMS.2021.3062362.

[9] Ye C F, Zhao L, Feng C Q, et al. “A new method of waveform digitization based on time-interleaved A/D conversion,” Chinese Physics C, vol. 37, no. 11, 2013, doi: 10.1088/1674-1137/37/11/116102.