Performance tests of a power-electronics converter for multi-megawatt wind turbines using a grid emulator

Nurhan Rizqy Averous¹,², Anica Berthold¹,³, Alexander Schneider⁴, Franz Schwimmbeck⁴, Antonello Monti¹,³ and Rik W. De Doncker¹,²

¹ Center for Wind Power Drives, RWTH Aachen University, Aachen, Germany
² Institute for Power Generation and Storage Systems, E.ON Energy Research Center, RWTH Aachen University, Aachen, Germany
³ Institute for Automation of Complex Power Systems, E.ON Energy Research Center, RWTH Aachen University, Aachen, Germany
⁴ Siemens AG, Ruhstorf a. d. Rott, Germany

E-mail: post.pgs@eonerc.rwth-aachen.de

Abstract. A vast increase of wind turbines (WT) contribution in the modern electrical grids have led to the development of grid connection requirements. In contrast to the conventional test method, testing power-electronics converters for WT using a grid emulator at Center for Wind Power Drives (CWD) RWTH Aachen University offers more flexibility for conducting test scenarios. Further analysis on the performance of the device under test (DUT) is however required when testing with grid emulator since the characteristic of the grid emulator might influence the performance of the DUT. This paper focuses on the performance analysis of the DUT when tested using grid emulator. Beside the issue regarding the current harmonics, the performance during Fault Ride-Through (FRT) is discussed in detail. A power hardware in the loop setup is an attractive solution to conduct a comprehensive study on the interaction between the power-electronics converters and the electrical grids.

1. Introduction
In the last decades, a vast increase of wind energy penetration into the electrical grids has forced WT to support the grid operation. Hence, WT nowadays must undertake grid compliance tests to prove if WT can perform as required by the grid codes. One crucial test is the so-called Fault Ride-Through (FRT) test. In this test, the capability of WT to remain synchronized with the electrical grid is proven as it is required by todays grid codes [1][2].

Typically, FRT tests are performed by means of a shunt-impedance-based fault generator[3][4]. Another test method using a power-electronics-based grid emulator has been developed for the 4 MW WT test bench at the Center for Wind Power Drives (CWD), RWTH Aachen University [5]. Compared to the first method, it offers a higher flexibility to the test conditions due to the controllability of the grid emulator. However, the tests using grid emulators might result in a different performance as compared to the conventional method. The voltage harmonic distortion due to switching of the grid emulator converters might result in an undesired harmonic interaction with the DUT. Moreover, the impedance formed by the passive elements of the grid emulator could lead to a different voltage reaction at the PCC during the FRT tests.
This paper focuses on the analysis on the behavior of the DUT when operating with the grid emulator, particularly the harmonics interactions and the performance during FRT tests. The analysis in this paper is conducted based on the simulation of the system using the software MATLAB/Simulink and PLECS which provides preliminary evaluation of the design of the newly developed grid emulator and DUT as well as the expected interaction prior to the operation.

At first, the improved power-electronics-based grid emulator for the WT test bench at the CWD is described. Afterwards, the construction of the considered DUT as well as its main features are presented in detail. Before discussing the FRT tests, the harmonics interactions related issues in the operation of the DUT with the grid emulator are briefly discussed. This delivers an important information if the passive components and switching of the grid emulator will harm the components of the DUT after synchronization.

Finally, the behavior of the DUT during the FRT tests using the grid emulator is analysed. The results of the FRT tests are then compared with the typical FRT tests conducted using a shunt-impedance-based fault generator. Beside showing if the construction of the grid emulator leads to instability during emulated grid faults, it provides the basic characteristic of the grid emulator in comparison to the conventional test method.

2. Grid emulator

In principle, the grid emulator provides a controllable 50 Hz ac grid at the point of common coupling (PCC) to the DUT. It actively regulates the voltage at the PCC according to the grid conditions to be emulated. For the test bench at CWD, a power-electronics-based grid emulator is used. As shown in Fig. 1, the grid emulator is constructed by three parallel medium-voltage (MV) converters with Three-Level Neutral-Point-Clamped (3L NPC) topology [6]. Thereby, a controllable ac voltage of 3 kV (line-to-line) can be generated with a 5 kV dc bus.

![Figure 1. Schematic of the grid emulator on the test bench at Center for Wind Power Drives](image-url)
Table 1. Grid emulator specifications

| Parameter                  | Symbol   | Value               |
|----------------------------|----------|---------------------|
| **Converter**              |          |                     |
| Max. phase current (200 ms)| $I_{GE,max}$ | $3 \times 1100$ A  |
| Carrier frequency          | $f_{car,GE}$ | 750 Hz             |
| Series inductor            | $L_{f,GE}$ | 100 $\mu$H         |
| **Transformer**            |          |                     |
| Windings                   |          | Secondary | Tertiary   |
| Rated power                | $S_{N,TR,GE}$ | 3 $\times$ 2000 kVA | 2000 kVA |
| Rated voltage              | $V_{N,TR,GE}$ | 3 $\times$ 3 kV   | 6 kV     |
| Short-circuit voltage      | $v_{k,TR,GE}$ | 3 $\times$ 4.25% | 2.08%    |
| **Filter**                 |          |                     |
| Capacitor                  | $C_{f,GE}$ | 14.5 $\mu$F        |
| Damping resistor           | $R_{f,GE}$ | 3.2 $\Omega$       |

interleaved switching strategy, a three-phase series inductor $L_{f,GE}$ is installed in between every converter and the transformer windings. In Table 1, the specifications of the grid emulator are summarized.

3. Device under test

A grid-connected converter system designed for a 2.75 MW research wind turbine is considered as the DUT. It comprises three parallel-connected power blocks and a control unit that controls the entire converter. Each power block consists of a grid-side converter (GSC) and a machine-side converter (MSC) based on a low-voltage two-level voltage-source converter topology. Because the power blocks are switched synchronously, the system can then be treated as one unit system with a larger capacity.

In the research wind turbine, the MSC drives a 2.75 MW asynchronous generator and provides the necessary electromagnetic torque to control the WT. On the grid side, the GSC is equipped with a passively-damped $LC$-filter that forms with the stray inductance of the transformer $TR_{DUT}$ an $LCL$-filter. During the operation, the DUT converter synchronizes the voltage on the low-voltage (LV) side of $TR_{DUT}$ that steps the voltage up from 690 V to 20 kV at PCC. Detailed parameters of the DUT are listed in Table 2.

The grid filter has been designed to meet the harmonics criteria given in the BDEW grid code[2]. Care must be taken when connecting the GSC to a converter-based grid emulator. Current harmonics produced by the grid emulator due to switchings might additionally stress
Table 2. Key parameters of the device under test (DUT)

| Parameter                  | Symbol     | Value            |
|----------------------------|------------|------------------|
| Converter                  |            |                  |
| Rated power                | $S_{N,DUT}$| 3.05 MVA         |
| Rated current              | $I_{N,DUT}$| 2552 A           |
| Rated power factor         |            | 0.9 cap. and ind.|
| Rated dc-link voltage      | $V_{DC,DUT}$| 1.05 kV         |
| Carrier frequency          | $f_{car,DUT}$| 3.2 kHz        |
| Filter inductor            | $L_{f,DUT}$| 33.3 µH          |
| Filter capacitor           | $C_{f,DUT}$| 2.07 mF          |
| Filter resistor            | $R_{f,DUT}$| 7.83 mΩ          |
| Transformer                |            |                  |
| Nominal power              | $S_{N,TR,DUT}$| 3.5 MVA       |
| Short-circuit voltage      | $v_{k,TR,DUT}$| 7.5 %          |

The DUT has been designed to fulfill the recent grid code regarding the FRT requirements. Besides staying synchronized with the grid during the fault occurrence, the converter is able to deliver reactive current $I_{PCC,R}$ (in p.u.) to the grid according to (1). It depends on the residual grid voltage $V_{PCC,res}$ as well as the factor $k$. The resulting $I_{PCC,R}$ is negative in case of grid faults $V_{PCC,res} < 0.9$ p.u. indicating an overexcited operation. The adjusted factor $k$ is to be coordinated with the grid operator prior to the initial grid connection and can vary from 0 up to 10. In case the combination of $V_{PCC,res}$ and $k$ results in $|I_{PCC,R}| > 1$ p.u., the magnitude of the reactive current is limited to 1 p.u.

$$I_{PCC,R} = \max (k \times (V_{PCC,res} - 0.9), -1) \text{ p.u. for } V_{PCC,res} \leq 0.9 \text{ p.u.}$$ (1)

4. Harmonics interaction

4.1. Stress on filter components

Grid filter components of the DUT, $C_{f,DUT}$ and $R_{f,DUT}$, are dimensioned according to the current harmonics that occur due to switchings of the power-electronics converters. Usually, the grid voltage is assumed to be harmonics free such that only the switching of the DUT converters contribute to the stress of the filter components $C_{f,DUT}$ and $R_{f,DUT}$. When operating the DUT on a test bench with a power-electronics-based grid emulator, additional stress due to the produced harmonics by the grid emulator converters (GEC) might occur. Therefore, it must be ensured that $C_{f,DUT}$ and $R_{f,DUT}$ are not overstressed during the operation with the grid emulator. To study this issue, the power loss mainly in the $R_{f,DUT}$ is analysed and compared to the value the $R_{f,DUT}$ is designed for.

Figure 3 shows the frequency spectrum of the emulated grid voltage $V_{PCC}$ on the low-voltage (LV) side of $TR_{DUT}$ obtained from the simulation with two possible grid emulator setups. The setup 1 applies the specification given in Table 1. For the setup 2, a higher carrier frequency $f_{car,GE} = 1050$ Hz is used and the entire filter components $C_{f,GE}$ and $R_{f,GE}$ are disconnected. Both setups result in a voltage total harmonic distortion $\text{THD}_V$ lower than 5 % as required in [3] which can be obtained using (2).
Harmonic order

\( V_{\text{PCC}}, \text{LV} \) in V

\( V_u \) in p.u.

(a) Setup 1

(b) Setup 2

Figure 3. Frequency spectrum of the emulated grid voltage on the LV side of TR_{DUT} at no-load

\[
\text{THD}_V = \sqrt{\sum_{h=2}^{50} \frac{|V_{\text{PCC},h}|^2}{V_{\text{PCC},N}^2}} \times 100 \%
\]  \hspace{1cm} (2)

It must be noted that the given equation for \( \text{THD}_V \) considers a frequency range only up to the 50\(^{\text{th}}\) harmonic for a 50 Hz power system (2500 Hz). Thereby, the grid emulator setup 2 still fulfills the \( \text{THD}_V \) requirement even though the grid emulator filter branch is disconnected. Due to the increase in the carrier frequency \( f_{\text{car},GE} \), the voltage harmonics are shifted outwards the evaluated frequency range in (2). This can potentially overload the installed filter components in the DUT.

To obtain the power loss in the filter resistance \( R_{f,DUT} \), simulations of the entire system including the grid emulator and the DUT have been carried out using the software PLECS. Besides with the aforementioned grid emulator setups, a simulation with a reference grid has also been conducted. The reference grid is a simplified grid model that incorporates an inductive grid impedance with a short-circuit power of 110 MVA. Since the voltage of the reference grid is assumed to be free of harmonic distortion, the power loss occur in the \( R_{f,DUT} \) is solely due to the GSC of the DUT. The total power loss in the DUT’s filter resistances \( P_{f,DUT} \) obtained from simulation with different grid setups and grid voltage magnitudes \( V_{\text{PCC}} \) is displayed in Fig. 4.

Figure 4. Total power loss in the \( R_{f,DUT} \)

As can be seen in Fig. 4, the influence of the grid emulator on the \( P_{f,DUT} \) is relatively low. When operating the DUT with the grid emulator, only 5\% higher power loss \( P_{f,DUT} \) can be observed compared to with the reference grid. This increase of power loss is still within the acceptable range for a safe operation of the DUT. Even with the grid emulator setup 2, only
a slight increase occurs in the $P_{f,DUT}$. This indicates that the series impedance formed by the stray inductance of the TR$_{DUT}$, stray inductances of the TR$_{GE}$ and $L_{f,GE}$ provides a sufficient attenuation for the harmonics produced by the GEC to avoid an overload in $R_{f,DUT}$.

Figure 4 also reveals the dependency of the $P_{f,DUT}$ on the $V_{PCC}$. Besides the power at fundamental frequency, the harmonics produced by the power-electronics converters also contributes to the variation in the $P_{f,DUT}$. According to [8], these harmonics are affected by the applied dc-link voltage as well as the modulation ratio of the GEC. Thereby, the contribution of the switching harmonics of the GEC to the increase in the $P_{f,DUT}$ is also slightly higher. However, due to the the series impedance between the DUT and grid emulator, the increase of $P_{f,DUT}$ is still kept below 5%.

### 4.2. Current harmonics at PCC
Prior to the connection of wind turbines to an electrical grid, the injected current harmonics must be evaluated according to the valid grid code. When tested with the grid emulator, the resonance introduced by the passive elements of the grid emulator can amplify the current harmonics injected by the DUT to the grid. In addition, the harmonic contents present in the emulated grid voltage $V_{PCC}$ can falsify the measured current harmonics of the DUT at the PCC [7]. These two issues need to be investigated separately.

![Figure 5. Influence of the grid emulator on the current harmonics at the PCC](image)

To identify the possible harmonics amplifications caused by the passive elements of the grid emulator setup 1, the frequency response of the PCC current $I_{PCC}$ due to the voltage at the GSC’s terminal of the DUT $V_{GSC}$ as displayed in Fig. 5(a) is used. Beside with the grid emulator setup 1, the frequency response with the reference grid, which is the assumed grid condition while designing the grid filter of the DUT, is also plotted. It can be seen in Fig. 5(a) that no significant difference between both grid setups is observed in the attenuation around the carrier frequency of the DUT (3.2 kHz), where the harmonics are mainly located. At this frequency, the impedance of both grid setups is relatively small compared to the impedance the stray inductance of the TR$_{DUT}$. Thereby, the influence of the grid emulator setup on the PCC current is negligible at this frequency. In addition, no amplification caused by the passive components of the grid
emulator can be seen in Fig. 5(a) since it is well damped by the $R_{f, GE}$. Hence, it can be concluded that the grid emulator setup has a negligibly impact on $I_{PCC}$.

Besides the impedance of the grid emulator, the voltage distortion of the grid emulator can affect the obtained current harmonics at the PCC $I_{PCC}$. Figure 5(b) presents the frequency spectrum of $I_{PCC}$ on the LV side of $TR_{DUT}$ obtained from the simulation with two different grid setups. In the upper graph, the current harmonics of the DUT with the reference grid are displayed. Since the reference grid is free of harmonic distortion, the harmonic content in $I_{PCC}$ with the reference grid is solely due to the DUT. However, the harmonic content caused by the DUT is significantly affected by the harmonic distortion caused by the GEC as displayed in the lower graph of Fig. 5(b). When the current harmonics of the DUT needs to be determined on the test bench with the grid emulator, the current harmonics caused by the DUT need to be calculated based on the measured $V_{GSC}$ and the system admittance $\frac{I_{PCC}}{V_{GSC}}$ as in Fig. 5(a).

5. Fault ride-through (FRT) tests

As previously mentioned, several advantages can be gained when performing FRT tests of the DUT with the grid emulator. In the following subsections, the dynamic behavior of the grid emulator will be firstly characterised. Afterwards, typical fault voltage waveforms for the certification of wind turbines [3][9] are emulated at the PCC and the simulated performance of the overall system is analyzed. Lastly, the behavior of the DUT during grid faults is compared with the field test results performed using a shunt-impedance voltage divider. For the following analysis, only the grid emulator setup 1 as defined in Table 1 is considered.

5.1. Characteristics of the grid emulator

Before performing the FRT tests with the grid emulator, it must be ensured that the emulated fault voltage represents what the DUT might experience in the field. To conduct this evaluation, standard IEC 61400-21 [3] is used as a reference. It provides a standardized waveform for fault voltages in the root-mean-square (RMS) domain that can be used to perform certification regarding the FRT capability. Figure 6(a) shows the emulated three-phase grid fault voltage with a residual voltage $V_{PCC, res} = 0.5$ p.u. and a fault duration $t_{fault} = 100$ ms. In the Fig. 6(b), the corresponding rms waveform is plotted along with the tolerance area according to the standard IEC 61400-21.

![Waveforms of an emulated grid fault voltage obtained from a simulation](image)

**Figure 6.** Waveforms of an emulated grid fault voltage obtained from a simulation

As projected in Fig. 6(b), the dynamic of the grid emulator is high enough to realistically emulate grid faults. The rms waveform lies within the tolerance area for the entire fault duration. At the fault occurrence as well as fault recovery, the voltage reaches its final value within less than 20 ms as required by the standard IEC 61400-21. A small oscillation observed at the beginning of the voltage transient is mainly due to the resonance formed by the filter capacitor $C_{f, GE}$, the filter inductor $L_{f, GE}$ and the stray inductances of $TR_{GE}$. The oscillation is damped by the
resistances in the system mainly by $R_{\text{f,GE}}$ such that it lasts only less than 2 ms and does not significantly influence the rms waveform of the voltage.

### 5.2. Simulation of FRT tests
To observe the behavior of the entire system while performing an FRT test, a grid fault scenario is simulated using the simulation platform MATLAB/Simulink. The DUT supplies an active power of 1 MW when a grid fault with $V_{\text{PCC, res}} = 0.39 \text{ p.u.}$ and $t_{\text{fault}} = 600 \text{ ms}$ occurs at the PCC. For this test, $k = 2$ has been selected such that a reactive current $I_{\text{PCC,R}}$ of 1 p.u. is supplied by the DUT during the fault event.

![Graphs showing instantaneous and rms voltages and currents during FRT test](image)

**Figure 7.** FRT test with the grid emulator: $V_{\text{PCC, res}} = 0.39 \text{ p.u.}$, $t_{\text{fault}} = 600 \text{ ms}$

Figure 7 presents the behavior of the DUT during the occurrence of the grid fault. The upper graphs show the instantaneous PCC voltages and currents measured on the low-voltage side of the TRDUT whereas in the lower graphs the rms voltage and currents are plotted. Negative active and reactive currents indicate a current flow towards the grid. Immediately after the fault occurs, the DUT stays synchronized with the grid and the active current is increased up to 0.7 p.u. to compensate the dropping grid voltage. As expected, the reactive fraction of the grid current $I_{\text{PCC,R}}$ also rises towards 1 p.u. due to the pre-programmed $k$ factor. It results in a current magnitude higher than 1 p.u. which is still permitted regarding the stress on the installed semiconductor devices.

As a result of the voltage support functionality via $I_{\text{PCC,R}}$ within the fault duration, the $V_{\text{PCC}}$ slightly rises to about 0.46 p.u. from 0.39 p.u. at no-load leading to a slight reduction of $I_{\text{PCC,R}}$ to 0.9 p.u. This voltage increase is caused mainly by the voltage drop over the stray inductance of the TRDUT, stray inductance of TRGE and the filter inductor $L_{\text{f,GE}}$. Due to the relatively small size of $C_{\text{f,GE}}$ and the relatively low PCC voltage throughout the grid fault, the filter branch of the grid emulator does not significantly contribute to the voltage variation. It can be concluded that the emulated grid fault using the grid emulator reflects a fault situation where the fault impedance is relatively small. Due to the relatively high impedance of TRDUT compared to the impedance of the grid emulator at the PCC, the DUT can stay synchronized with the grid emulator without any instability problems.

In order to have a comparison on the behavior of the DUT at the PCC, a practical FRT test using a shunt-impedance-based fault generator has been carried out in the test field of
Siemens AG in Ruhstorf a. d. Rott, Germany. The schematic of the fault generator [10] and the measured fault voltage at no-load are presented in Fig. 8. To apply the fault at the PCC, the switch CB₁ must be firstly opened to limit the influence on the public grid during the test via the $X_{sr}$. Afterwards, the switch CB₂ is closed and a short-circuit via the impedance $X_{sc}$ occurs at the PCC leading to a voltage dip. $X_{sr}$ and $X_{sc}$ must be selected according to the desired residual voltage $V_{PCC,\text{res}}$.

In the conducted test, a fault with $V_{PCC,\text{res}} = 0.39 \text{ p.u.}$ for $t_{\text{fault}} = 2500 \text{ ms}$ is applied while the DUT operates with an active power of $1 \text{ MW}$. The residual voltage is proven at no-load condition (Fig. 8(b)) to exclude the influence of the DUT, $k = 2$ is selected in the DUT controller so that the DUT is expected to deliver reactive current $I_{PCC,R}$ of $1 \text{ p.u.}$ through the fault duration. The voltages and currents measured on the low-voltage side of TRDUT are plotted in Fig. 9.

Through an FRT test with the shunt-impedance-based fault generator, a similar behavior of the DUT can be identified. The active current rises proportionally to the dropping $V_{PCC}$ and the reactive current support $I_{PCC,R}$ is activated. However, only $0.6 \text{ p.u.}$ of $I_{PCC,R}$ can be observed from Fig. 9. Due to a relatively high fault impedance formed by the reactances in the fault generator circuit, the reactive current $I_{PCC,R}$ forces the PCC voltage to rise significantly from $0.4 \text{ p.u.}$ to $0.6 \text{ p.u.}$ Due to the voltage rise, the DUT has to adjust the $I_{PCC,R}$ accordingly.

### 6. Power-Hardware-in-the-Loop (PHiL) Setup

Both FRT tests are implemented with a standardized voltage curve. In case of the grid emulator the reference to the converter comes from data generated offline. Due to this implementation only the effect of the fault impedance on the behavior of the DUT can be shown. In reality the behavior of the DUT during a grid fault is determined by the complex grid structure. One solution to consider the grid structure in the FRT tests without connecting DUT to the real...
grid is by means of the so-called Power-Hardware-in-the-Loop (PHiL) setup depicted in Fig. 10. It allows further critical tests of the DUT as well as comprehensive interaction studies between the DUT and the electrical grids.

![PHiL setup](image)

**Figure 10.** PHiL setup

PHiL describes a process, where a part of a system is simulated and another part of the system exists in real, described as device under test (DUT). A PHiL setup always requires a power interface. In this case the grid emulator is the power amplifier of the system [11][12][13]. The grid emulator acts as a controlled voltage source which obtains the output of the real-time grid simulation as reference voltage and provides the appropriate voltage at the PCC for the DUT. The current at the PCC is measured and fed back into the real-time simulation. The real time digital simulator (RTDS) is used for the implementation of a real-time simulation of the power grid [14]. The RTDS is part of the real time laboratory at the Institute for Automation of Complex Power Systems (ACS). The challenge in this setup is the distance between the ACS real-time laboratory and the test bench at the Center for Wind Power Drives (CWD) since a low latency between the RTDS and the grid emulator is necessary for the stability of the PHiL setup. Fiber optic cables are used as communication link between the two locations, which have a distance of 2 km to each other.

7. Conclusions and Outlook

The performance of a power-electronics converter for WT might be influenced by the behavior of the power-electronics-based grid emulator. The analysis has shown that the DUT can be safely operated without any overstress in the filter components although the measured harmonics at the PCC are strongly influenced by the grid emulator. Regarding the FRT test, the grid emulator shows a relatively low grid fault impedance which results in a significant different behavior of the DUT during grid faults compared to the test results with the shunt-impedance-based fault generator. Hence, the influence of the DUT on the PCC voltage is relatively minimum compared to the conventional method. PHiL setup developed for the 4 MW Wind Turbine Test Bench at CWD RWTH Aachen University is an attractive solution for the comprehensive interaction study between power-electronics converters for WT and the electrical grids. Although the evaluation is based on simulation results, it also provides the preliminary characteristics of the newly developed grid emulator and its expected interaction with the DUT. Since the test bench is currently being commissioned, the verification of the presented evaluation will be presented in a future paper.

Acknowledgement

The authors would like to thank the Federal Ministry for Economic Affairs and Energy of Germany for the financial support of this work.
References

[1] Verordnung zu Systemdienstleistung durch Windenergieanlagen (Systemdienstleistungsverordnung - SDLWindV), Std., July 2009. [Online]. Available: www.bundesgesetzblatt.de

[2] BDEW, Technical Guideline Generating Plants Connected to the Medium Voltage Network, June 2008.

[3] IEC, Wind turbines - Part 21: Measurement and assessment of power quality characteristics of grid connected wind turbines, IEC Std. 61 400-21, 2008.

[4] J. Dirksen, “Lvrt - low voltage ride-through,” DEWI Magazine, no. 43, August 2013. [Online]. Available: http://www.dewi.de/

[5] N. Averous, M. Stieneker, S. Kock, C. Andrei, A. Helmedag, R. De Doncker, K. Hameyer, G. Jacobs, and A. Monti, “Development of a 4 mw full-size wind-turbine test bench,” in Power Electronics for Distributed Generation Systems (PEDG), 2015 IEEE 6th International Symposium on, June 2015, pp. 1–8.

[6] A. Nabae, I. Takahashi, and H. Akagi, “A new neutral-point-clamped pwm inverter,” IEEE Transactions on Industry Applications, vol. 1A-17, no. 5, pp. 518–523, Sept 1981.

[7] N. Averous, M. Stieneker, and R. De Doncker, “Grid emulator requirements for a multi-megawatt wind turbine test-bench,” in Power Electronics and Drive Systems (PEDS), 2015 IEEE 11th International Conference on, June 2015, pp. 419–426.

[8] D. G. Holmes and T. A. Lipo, Pulse Width Modulation for Power Converters: Principles and Practice. John Wiley & Sons, 2003.

[9] FGW, TR 3: Bestimmung der elektrischen Eigenschaften von Erzeugungseinheiten am Mittel-, Hoch- und Hochspannungsnetz, March 2010.

[10] F. T. S. GmbH. (2013, February) Mobile lvrt test laboratory 5 mva, 10 - 30 kv: Product information. FGH Test Systems GmbH.

[11] K. Jha, S. Mishra, and A. Joshi, “Boost-based amplifier for power-hardware-in-the-loop simulations of utility-tied dg,” in Industrial Electronics Society, IECIN 2015 - 41st Annual Conference of the IEEE, Nov 2015, pp. 003 242–003 247.

[12] G. Lauss, F. Lehu, A. Viehweider, and T. Strasser, “Power hardware in the loop simulation with feedback current filtering for electric systems,” in IECIN 2011 - 37th Annual Conference on IEEE Industrial Electronics Society, Nov 2011, pp. 3725–3730.

[13] A. Helmedag, “System level multi-physics power hardware in the loop testing for wind energy converters,” Dr., Zulg.: Aachen, Techn. Hochsch., Aachen, 2015, prfungs: 2015; Zugl.: Aachen, Techn. Hochsch., Diss., 2015. [Online]. Available: http://publications.rwth-aachen.de/record/466674

[14] Rtds: Real time digital simulator. [Online]. Available: www.rtds.com