A five-level multilevel topology utilizing multicarrier modulation technique

Rabiya Rasheed1, Saju K. K.2, Bindu V.3
1,2 Department of Mechanical Engineering, Cochin University of Science and Technology, India
3 Department of Electrical and Electronics Engineering, Model Engineering College, India

ABSTRACT

This paper presents a new topology for cascaded H-bridge multilevel inverter utilizing multicarrier modulation technique. The new five-level topology utilizes a capacitive divider network consisting of two capacitors for producing output voltage levels. The developed circuit has reduced number of switches and dc sources compared to conventional five level inverters. Five main power switches, a single additional diode apart from antiparallel diodes, two capacitors and a dc supply constitute a single five level unit. Simulations as well as experimental results are verified for the new topology utilizing multicarrier modulation technique with reduced harmonic distortions in the output.

Keywords:
Five-level inverter
Multicarrier modulation

1. INTRODUCTION

Multilevel inverters are gaining attention in power system engineering especially in the field of renewable energy systems. By operating at different voltage levels, these converters effectively decreases the voltage stress to the operating switches. They can be classified into three main categories: diode clamped, flying capacitor type and cascaded H-Bridge type [1]. Different modulation strategies comprising of sinusoidal pulse width modulation, selective harmonic elimination and space vector modulation have been developed based on these conventional multilevel inverters. The diode clamped topology consists of a number of uncontrolled switches. Even though the topology is being used in statcom based applications, the flying capacitor type is considered much more flexible. But these converters require a large number of capacitors to clamp different voltage levels. As a rectification to these problems, cascaded multilevel inverters were developed [2-7]. Gerardo Ceglia et al proposes a five level inverter topology utilizing auxiliary switches and dc link capacitors [8]. Even though the topology suggests the distribution of capacitor voltages which are being charged in a self balancing form, it requires additional diodes for its working. Also the increase in number of diodes are also essential for increasing voltage levels.

This paper presents a new five-level multilevel inverter topology utilizing a single additional diode apart from antiparallel diodes. Reduction in the number of main power switches [9-12] has been the main advantage of this topology compared to conventional multilevel inverters. Power circuit operation of the developed topology and modulation scheme for the same using multicarrier modulation technique has also been conducted. The Total Harmonic Distortion (THD) of the new converter by conducting experimental and simulation studies is carried out using Spartan 3AN XC3S1400AN-4FG676C FPGA kit and PSIM software respectively.
2. **NEW FIVE LEVEL INVERTER**

2.1. **Circuit configuration**

The new five level inverter topology utilizing a zener diode is shown in Figure 1. With a specific switching pattern, the developed inverter can produce five levels of distinct voltage levels ($V_S$, $V_S/2$, 0, $-V_S/2$ and $-V_S$). A conventional five level inverter requires eight main power switches for producing five level output voltage. This topology requires only five main controllable switches and a single additional diode for its proper working. This saving in the number of main power switches will result in a considerable reduction in the switching losses of the circuit.

![Figure 1 New five level inverter](image)

2.2. **Power stage operation**

The switching states of the new five level inverter are given in Table 1. “1” and “0” indicates the ON and OFF states of the switches respectively.

| Modes     | $V_O$ | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ |
|-----------|-------|-------|-------|-------|-------|-------|
| Mode-1    | $V_S$ | 1     | 1     | 0     | 0     | 1     |
| Mode-2    | $0.5V_S$ | 1     | 1     | 0     | 0     | 0     |
| Mode-3    | 0     | 0     | 0     | 1     | 1     | 0     |
| Mode-4    | $-V_S$ | 0     | 0     | 1     | 1     | 1     |
| Mode-5    | $-0.5V_S$ | 0     | 0     | 1     | 1     | 0     |

2.3. **Modulation strategy**

New five level inverter utilizes multicarrier modulation technique [13] involving carrier based PWM. Comparators compare modulating signal with carrier signals to produce control signals. The modulating and carrier signals have been shown in Figure 2. The control pulses and the specific switching pattern for the new inverter are as shown in Figure 3. The switching pulses for the new inverter are finally obtained with the help of logical gates using Boolean equations given in (1).

\[
S_1 = S_2 = P_1 C_1 \\
S_3 = S_4 = P_2 C_1 \\
S_5 = C_2
\] (1)

Modulation index for a multilevel inverter can be defined as

\[
M_a = A_m/A_r (k-1)
\] (2)

Where $k$ is the number of voltage levels per half cycle.
$A_c$ is the peak to peak value of carrier wave, $A_m$ is the peak value of modulating signal. Hence by applying equation (2), modulation index ($M_a$) for proposed inverter can be defined as.

$$M_a = \frac{A_m}{2A_c} \quad (3)$$

The operation of the inverter has been separated to four modes. By increasing the number of pulses per half cycle, harmonic amplitudes of output voltage can be limited to higher order harmonics alone. Higher order harmonics can then be easily filtered out [14]. Harmonic distortion of the proposed inverter is significant for modulation index less than unity. Total harmonic distortion (THD) of output voltage reduces with higher values of modulation index [15-17].

Different multicarrier techniques have been developed in multilevel inverters utilising triangular carriers. Multicarrier modulation technique has been conducted at high switching frequencies. Multicarrier modulation involves either phase shifting of multiple carrier signals or disposition of carrier signals. This work emphasizes on carrier disposition method for comparison with modulating signal.

3. EXPERIMENTAL

New multilevel topology has been experimentally verified using the block diagram in Figure 4. Control signals are generated in real time through Spartan 3E FPGA kit incorporating Xilinx System Generator and ISE Design Suite.
3.1. Generation of modulating and carrier signals in XSG

Digitalised modulating and carrier signals are generated in MATLAB through Xilinx System Generator [18-20]. Again VHDL code is developed using Integrated Software Environment (ISE) simulator which is then integrated into Spartan 3AN XC3S1400AN-4FG676C FPGA kit.

3.2. Generation of carrier signals

Frequency of the carrier wave selected is 2KHz. Carrier wave generation can be explained with the help of block diagram in Figure 5. Up-Counter in XSG is used to generate a ramp signal varying from 0 to 8192. Bit slicer extractor slices off a particular sequence of bits from the input. It then creates a new data value, $2^{12}=4096$. Finally reinterpret block is used to change signal type from signed to unsigned.

![Block diagram representation of hardware for new five level inverter](image)

Figure 4. Block diagram representation of hardware for new five level inverter

![Block diagram representation for generation of carrier signals](image)

Figure 5. Block diagram representation for generation of carrier signals

3.3. Generation of modulating signal

Modulating signal is generated at a frequency of 50 Hz as shown in block diagram in Figure 6. To increment the count value from 0 to 999, number of bits required for the Xilinx up-counter is $2^{10}=1024$. The initial value of ROM block is $\sin(2\pi f)$. Using the gain block, amplitude of sine wave has been varied for different values of modulation indexes. Digitised sine wave is then compared with carrier signals. Generation of Switching Pulses Xilinx relational operator is used to compare rectified modulating signal and two carrier signals which are phase shifted to produce required switching pattern for the new inverter as per the modulation strategy.

![Block diagram representation for generation of modulating signal](image)

Figure 6. Block diagram representation for generation of modulating signal

3.4. Experimental prototype

Establishment of power circuit for the new inverter is done by using four IRF 540N MOSFET’s in H-Bridge and a single IRF540N across the diode. The load chosen is resistive load of 50Ω and an inductive load of 1mH. Output voltage and current for the new five level topology for a modulation index of unity is shown in Figure 7. FFT spectrum for a modulation index of unity is also observed using harmonic analyzer as shown in Figure 8. Experimental set up for the new topology is shown in Figure 9.

![Experimental prototype](image)

Figure 7. FFT spectrum for a modulation index of unity

3.5. Results and discussion

Results from simulation as well as experimental prototype agrees with proper working of new five level inverter. Five distinct levels of voltages have been obtained in both cases. FFT spectrums for different modulation indexes have been visualized in PSIM software. It is seen that a clean spectrum has been obtained for higher values of modulation indexes by introducing output filters. FFT spectrum for modulation index of unity has been verified experimentally and similar results have been obtained.

---

*A five-level multilevel topology utilizing multicarrier modulation technique ... (Rabiya Rasheed)*
4. CONCLUSIONS

Simulated results and experimental set up shows that new five-level topology works as expected. Minimized converter switching and conduction losses can be obtained. Considerable weakening in balancing of capacitor voltages is prevented, since the charges are balanced in a cycle of output. Replacement of MOSFET’s by IGBT’s and new concepts in converter switches may lead to higher efficiencies.

REFERENCES

[1]. J. Rodriguez, J-S. Lai, and F. Z. Peng, “Multi-level inverter: a survey of topologies, controls, and applications,” *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724-738, Aug. 2002.

[2]. F. Minai and A. Tariq, “Analysis of Cascaded multilevel inverter,” *India International Conference on Power Electronics 2010 (IICPE2010)*, vol. 2, pp. 1–6, Jan. 2011.

[3]. X. Sun and S. Gao, “Research on topology and PWM control method of a novel cascaded multilevel inverter,” *2010 IEEE International Conference on Mechatronics and Automation*, pp. 523–528, Aug. 2010.

[4]. Malinowski, M., Gopakumar, K., Rodriguez, J., et al.: ‘A survey on cascaded multilevel inverters’, *IEEE Trans. Ind. Electron.*, 2010, 57, (7), pp. 2197-2206.

[5]. Barzegarkhoo, R., Zamiri, E, Vosoughi, N, et al.: ‘Cascaded multilevel inverter using series connection of novel capacitor-based units with minimum switch count’, *IET Power Electron.*, 2016, 9, (10), pp. 2060- 2075

[6]. D. Patel, R. Saravanakumar, K. K. Ray, and R. Ramesh, “A review of various carrier based PWM methods for multilevel inverter,” *India International Conference on Power Electronics 2010 (IICPE2010)*, vol. 1, pp. 1–6, Jan. 2011.

[7]. K. A. Corzine, M. W. Wielebski, F. Z. Peng, and J. Wang, “Control of cascaded multilevel inverters,” *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 732-738, May 2004.
[8]. Gerardo Ceglia, Victor Guzman, Carlos Sanchez, Fernando Ibanez, Julio Walter, and Maria I. Gimenez, “A New Simplified Multilevel Inverter Topology for DC-AC Conversion,” IEEE Trans. Power Electron., vol. 21, no. 5, pp. 1311-1319, Sep. 2006.

[9]. Y. Hinago and H. Koizumi, “A single phase multilevel inverter using switched series/parallel DC voltage sources,” 2009 IEEE Energy Conversion Congress and Exposition, pp. 1962–1967, Sep. 2009.

[10]. M. R. Banaei and E. Salary, “New multilevel inverter with reduction of switches and gate driver,” 2010 18th Iranian Conference on Electrical Engineering, no. 2, pp. 784–789, May 2010.

[11]. E. Babaei, “A cascade multilevel converter topology with reduced number of switches,” IEEE Trans. Power Electron., vol. 23, no. 6, pp. 2657-2664, Nov. 2008.

[12]. Gupta, K. K., Ranjan, A., Bhatnagar, P., et al.: ‘Multilevel inverter topologies with reduced device count: A Review’, IEEE Trans. Power Electron., vol 31, (1), pp. 135-151, 2016.

[13]. B. P McGrath and D. G Helmes, “Multicarrier PWM strategies for multilevel inverters”, IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 858-867, Aug. 2002.

[14]. N. Farokhnia, H. Vadizadeh, F. A. Asl, and F. Kadkhoda, “Comparison between approximate and accurate line voltage THD, case II: Multilevel inverter with equal DC sources,” The 2nd International Symposium on Power Electronics for Distributed Generation Systems, pp. 246–251, Jun. 2010.

[15]. Y. Xue and M. Manjrekar, “A new class of single-phase multilevel inverters,” The 2nd International Symposium on Power Electronics for Distributed Generation Systems, pp. 565–571, Jun. 2010.

[16]. K. Wang, “A new transformerless cascaded multilevel converter topology,” 2009 IEEE Energy Conversion Congress and Exposition, pp. 3124–3129, Sep. 2009.

[17]. Bifarretti, S., Tarisciotti, L., Watson, A., Zanchetta, P., Bellini, A., Clare, J.: ‘Distributed commutations pulse-width modulation technique for high power AC/DC multilevel converters’, IET Power Electron., 5, (6), pp. 909-919, 2012.

[18]. S. Rajasekar, Rajesh Gupta, “Rapid prototyping of power electronics converters for photovoltaic system application using Xilinx System Generator”, IET Power Electron., 7, (9), pp.2269-2278, 2014.

[19]. Mekhilef, S., Masaoud, A.: ‘Xilinx FPGA based multilevel PWM single phase inverter’. IEEE Int. Conf. On Ind. Tech. (ICIT 2006), 15-17 December, pp. 259-264, 2006.

[20]. Mekhilef, S., Rahim, N. A.: Xilinx FPGA based three-phase PWM inverter and its application for utility connected PV system’. IEEE Conf. On Comp. Comm. Cont. And Power Eng. (TENCON ‘02), 28-31 October, pp. 2079-2082, 2002.

BIOGRAPHIES OF AUTHORS

Rabiya Rasheed was born in 1981. She received B. Tech and M. Tech degrees from Rajiv Gandhi Institute of Science and Technology, India. She is currently working as Assistant Professor at Federal Institute of Science and Technology, India. Also she is a part time research scholar at Cochin University of Science and Technology, India. Her interests include design of linear integrated circuits and power electronic converters.

Dr. Saju K.K was born in 1970. He received the B. Tech degree from Calicut University, India, the M. Tech degree from NIT, Calicut, India and the Ph. D. degree from Cochin University of Science and Technology, India. He is currently working as Professor at Cochin University of Science and Technology, India. He is also the Director of the International Relations and Academic Admissions at Cochin University. His interests lie in material science, robotics and automation. He is the author of more than 20 international publications and has handled several funded projects.

Dr. Bindu V received the B. Tech and M.Tech degrees from Regiona Engineering College, Calicut, India and the Ph. D. degree from Cochin University of Science and Technology, India. Currently she is the head of department at Electrical Engineering of Model Engineering College, Thrissakkara, India. Her interest lies in the area of soft computing techniques in the field of sensorless vector control of ac drives.

A five-level multilevel topology utilizing multicarrier modulation technique ... (Rabiya Rasheed)