High Performance Energy Efficient Computation Elements of Processing Unit

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Abstract: In our manuscript, various circuits for arithmetic summation are compared. Cadence 90nm technology and Quartus II EP2C20F484C7 are used for implementation of design. Logic gate-based adders, PFCA, TG and HSD technique-based adders characteristics are analyzed. Y finding is PFCA with 10T transistor performs slightly efficient compare to its counterpart. Exclusive OR-NOR design is optimum for least delay Adders for high performance energy efficient processing unit.

Keywords: Adders, Multipliers, Power Dissipation, Delay.

I. INTRODUCTION

The use of portable devices like laptops, mobile, tablets etc have been increasing tremendously over the years. We know that, ALU consists of Arithmetic and Logical Units. Arithmetic operations are performed by Adders, Multipliers and Subtractor. PFCA has been implemented using 11T. But there is voltage degradation during that implementation. So, the number of transistors has been reduced to 10 to reduce the voltage degradation to some extent. If in the 10T transistors, buffers to the both Summation and carry-out, waveform without any glitches and voltage degradation is obtained.

II. ADDER

A. Adder with ripple carry design (CLA)

RCA [1] is a sequence of full-adders. For n-bit RCA, n full adders are required. Carry bit generated is propagated from initial stage to next.

B. Plagiarism Adder with Carry look ahead design (CLA)

To reduce the delay, CLA [1] uses propagation (P) and generation (G) signals. P=input 1 $^\lor$ input 2 and G = input 1. input2 where input 1 & input 2 are labeled as A and B. The delay is less than RCA since the computation of the output of the next stage doesn’t depend upon the output carry of the previous stage.

Fig. 1. 4-bit RCA circuit.

Fig. 2. Waveforms of 4-bit RCA.

Here, input 1=4'b0101 and input 2=4'b0010 and we get the output as sum=4'b0111, here the carry of the 1st stage is rippled into the 2nd stage.

Fig. 3. Carry Look Ahead Adder.
Simulation Report of CLA (4-bit)

Here, a=4'b0010 and b=4'b1011 and we get the output as sum=4'b1110.

C. CARRY SELECT ADDER (CSA)

In CSA it is not required to wait for carry in every stage. Once the carry is known immediately the result can be obtained. For a 4-bit CSA, four-bit inputs are given. These inputs are applied to full-adders. Multiplexers are also used to generate resultant values in final stage.

D. PARALLEL FEEDBACK CARRY ADDER (PFCA)

The basic building component of PFCA is a half-adder. As a Full-adder is made up of two HA with OR logical element, whereas HA has one AND gate and one XOR gate. So, half-adder is just a component of PFCA. It has a parallel mode of operation with a feedback which as a whole provides speed to the adder and computation time is also low. The architecture of 4-bit PFCA is shown in Fig 4.

Implementing the circuit with CMOS gate shows that voltage degradation occurs when PMOS transistor passes 0 and NMOS transistor passes 1 logical output. Fig. 5 displays schematic structure of PFCA using 10T. The power dissipation is also high due to leakage current of the inverter. This leakage current makes the NMOS transistor to turn on in some unwanted situations. It can be avoided by using a PMOS transistor in series with the pull-up transistor of the inverter. The schematic is shown in Fig. 6. It has been implemented in Cadence by using the library gpdk90 with VDD=1.5V.

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III. SIMULATION RESULT

For SUM output:

![PFCA I/O waveforms using 10T](image1)

For Carry Output:

![PFCA I/O waveforms using 10T](image2)

Fig. 9. PFCA I/O waveforms using 10T.

IV. ADDER USING HSD (HIGH SPEED DOMINO) TECHNIQUE

In adders based on HSD technique [2], P-Type keeper transistor (kt) pullup network reduce the current leakage which is connected to the kt. a clock signal is applied to its gate.

![Simulation Result: Adder using HSD Technique with Carry as output](image3)

Simulation Result:

![Input and Cout waveforms of adders using HSD Technique](image4)

Fig. 12. Input and Cout waveforms of adders using HSD technique.

Adder based on Domino logic

![Fig. 13. Domino Logic](image5)

Fig. 13. Domino Logic
The Domino Logic [3] is shown in Fig. above. When the clock goes zero, $M_p$ is on and pre-charging takes place and the dynamic node is charged. During high level clock, the PDN network is operating and it evaluates the dynamic node called as the evaluation phase. The high-level dynamic node is preserved until the next pre-charge phase. The schematic diagram of 2-bit Domino Logic is shown in Fig. 14.

Fig. 14. Adder using 2-bit Domino Logic having Sum Output

Simulation Results:

Fig. 15. Schematic of 2-bit adder based on domino logic with carry as output

EX-OR with EX-NOR adder design

Fig. 16. Input and sum waveforms of 2-bit Domino Logic

Fig. 17. Input and carryout waveforms of 2-bit domino logic adder

Fig. 18. Full Adder Circuit using EX-OR /EX-NOR.
In order to obtain the complete voltage swing [4] for the output values, the TG $M_1$, $M_2$, $M_3$, $M_4$ are used. $M_1$ and $M_2$ transmission gates (TG) are connected to the XOR/XNOR output from where we get the sum as result. The transmission gates $M_3$ and $M_4$ are connected to the output of XOR/XNOR circuit from here we get the carry as result. When XOR generates logic 1 and XNOR generates logic 0, the TG $M_1$ switches on and $M_2$ switches off. The inverted input $Cin$ is given to the sum output. When the output of the XOR is at logic 0 and XNOR is at logic 1, $M_1$ is off and $M_2$ is on. Hence, the sum output is same as input $Cin$. This is the operation for the sum output. When the output of XOR is at logic high and XNOR is logic low, the transmission gate $M_3$ switches on and $M_4$ gate switches off. The carry-out bit is similar to $Cin$. When the output of XOR is low (0) and XNOR output is high (1), $M_4$ turns on and $M_3$ turns off. Hence, the carry-out is similar to the B input. This circuit can be implemented in Cadence in 90nm technology using $V_{DD}$=1.5V.

**PROPOSED CIRCUIT**
In the 10T PFCA, voltage degradation issue can be prevented by introducing buffers to both outputs in inverter form. The generated output is free from glitches with no degradation in voltage.

| TABLE 1. Comparison of adder circuits using Cadence and $V_{dd}$=1.5V |
| Adders | Power (µW) | Delay (ps) |
|--------|------------|------------|
| 2-bit Domino logic | 6.455 | 39.8 |
| High Speed Domino | 41.74 | 35.6 |
| PFCA (11T) | 120.4 | 45.76 |
| PFCA (10T) | 106.2 | 41.55 |
| Based on X-OR and X-NOR gates | 34.8 | 1.989 |

| TABLE 2. Comparison of adder circuits implemented in Cyclone II Family in Quartus II |
| Adders | No. of pins | No. of logic elements | Dynamic power dissipation (mW) | Static power dissipation (mW) | Delay (ns) |
|--------|-------------|----------------------|-----------------------------|-------------------------------|-----------|
| RCA  | 14 | 10 | 0 | 47.35 | 20.751 |
| CLA  | 14 | 15 | 0 | 47.35 | 17.234 |
| CSA  | 15 | 8 | 0 | 47.35 | 15.012 |

Fig. 19. Schematic EX-OR and EX-XNOR FA design

Simulation result:

![I/O waveforms of adder with X-OR and X-NOR gates](image1.png)

![Simulation result of 10T PFCA with buffers](image2.png)
V. CONCLUSION

11T design implementation of PFCA suffers with voltage degradation. If it is modified with 10T instead of 11T, the voltage degradation is reduced to some extent. Analysis of different adder circuits by implementing ASIC library and FPGA families is tabulated. Comparison of existing multipliers and proposal of a new design for optimized performance [11] may be the next level of development.

Implementation of Design of basic building blocks of ALU [9], MAC[15], FPU[14], RNS MAC[13], ALU-DBGU [12], FinFET based design [5], Reversible logic based ALU [6], Floating-Point Fused Multiply-Add Unit[7], Reversible logic based ALU[8] are few design were modified basic blocks can be used as library component for future analysis.

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