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Solution-Processed Memristor Devices Using a Colloidal Quantum Dot-Polymer Composite

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Abstract: In this study, we demonstrate solution-processed memristor devices using a CdSe/ZnS colloidal quantum dot (CQD)/poly(methyl methacrylate) (PMMA) composite and their electrical characteristics were investigated. Particularly, to obtain stable memristive characteristics with a large current switching ratio, the concentration of CdSe/ZnS QDs in the PMMA matrix was optimized. It was found that with the CdSe/ZnS QD concentration of 1 wt%, the memristor device exhibited a high current switching ratio of ~10^4 and a retention time over 10^4 s, owing to the efficient charge trapping and de-trapping during the set and reset processes, respectively. In addition, we investigated the operational stability of the device by carrying out the cyclic endurance test and it was found that the memristor device showed stable switching behavior up to 400 cycles. Furthermore, by analyzing the conduction behavior of the memristor device, we have deduced the possible mechanisms for the degradation of the switching characteristics over long switching cycles. Specifically, it was observed that the dominant conduction mechanism changed from trap-free space charge-limited current conduction to trap charge-limited current conduction, indicating the creation of additional trap states during the repeated operation, disturbing the memristive operation.

Keywords: memristors; colloidal quantum dot; polymer; solution process; endurance

1. Introduction

Recently, memristors have received significant interest for next-generation electronics such as neuromorphic computing systems, owing to their potential advantages such as high energy efficiency, good scalability, and compatibility with conventional complementary metal-oxide-semiconductor fabrication processes [1–10]. Particularly, memristors are considered as the fourth fundamental non-linear circuit element linking charge and magnetic flux [11]. In the memristor device, the electrical resistance state can be changed according to the history of the external stimulation, such as the voltage pulses, allowing the emulation of learning behavior and various neuromorphic functions. To realize the memristor device, various material systems have been investigated including ferroelectrics [12], ferromagnetics [13], and phase-changing materials [4,14]. In addition, organic/inorganic hybrid materials have received much attention recently due to their wide tunability in electrical properties, good mechanical flexibility, low-temperature process, and large-area scalability [15,16]. Moreover, since the organic/inorganic hybrids can be deposited by a simple solution process, the use of sophisticated vacuum deposition processes can be omitted, enabling the realization of cost-effective and area-scalable neuromorphic systems.

In the case of organic/inorganic hybrid-based memristors, it is claimed that the inorganic components such as the metallic or semiconducting nanoparticles play an important role in regulating the resistance state by acting as charge storage or charge trapping centers [17,18]. For the inorganic component, colloidal quantum dots (CQDs) can be a good candidate since they are solution processable and their bandgap can be tuned by adjusting...
the size of the QDs [19,20]. Particularly, when the QDs are embedded in an insulating polymer with a large bandgap over 3 eV [21], effective charge trapping can be expected at the QDs due to the relatively small bandgap of the QDs. Moreover, the QD-polymer memristors can provide potential advantages such as good mechanical flexibility [22], high optical transparency, and low voltage operation for efficient energy consumption [20]. To date, although some research has been carried on QD-polymer-based memristors [23], there is still a need for optimizing the QD concentration since the trapping and de-trapping of charge carriers at the QDs largely affect the memristive characteristics. Furthermore, a study on the conduction mechanism is required to understand the dominant conduction mechanism of the QD-polymer-based memristors and the possible origin of the degradation mechanisms under repeated operations.

In this study, we demonstrate solution-processed memristor devices using a CdSe/ZnS QD-poly(methyl methacrylate) (PMMA) composite, and their electrical characteristics were investigated. Particularly, to obtain stable memristive characteristics, we optimized the concentration of CdSe/ZnS QDs in the PMMA matrix. The CdSe/ZnS QD:PMMA memristor with an optimized QD ratio exhibited decent memristive characteristics with a high current switching ratio up to $10^4$ and a relatively long retention time over $10^4$ s. In addition, the operational stability of the device was investigated by performing the cyclic endurance test and it was found that the memristor devices showed stable switching behavior up to 400 cycles. Furthermore, by investigating the conduction behavior of the memristors, we have deduced the possible mechanisms for the degradation of the switching characteristics over long switching cycles. Particularly, by analyzing the I-V characteristics, we show that the dominant charge conduction mechanism changed from trap-free space charge-limited current (SCLC) conduction to trap charge-limited current (TCLC) conduction, indicating the creation of additional trap states during the repeated operation, disturbing the memristive operation.

2. Materials and Methods

For the fabrication of CdSe/ZnS QD-PMMA memristors, a PMMA powder ($M_w \sim 996,000$ g/mol, Sigma Aldrich, St. Louis, MO, USA) was first dissolved in toluene (Sigma Aldrich, 99.5%) at a concentration of 4 wt%. After a thorough stirring of the solution, colloidal CdSe/ZnS QDs (NSQDs-HOS-530, Nanosquare, Seoul, Korea) were added to the solution at a concentration of 1, 3 or 5 wt%. The size of CdSe/ZnS QDs with oleic acid ligands was around 6~8 nm with a ZnS shell thickness of 2~3 nm. After mixing the QDs, the solution was sonicated to uniformly disperse the CdSe/ZnS QDs in the solution. To fabricate the memristor device, a glass substrate with a 150 nm-thick indium-tin-oxide (ITO) was used. The ITO layer was used as the bottom electrode. The substrate was sonicated in isopropyl alcohol for 10 min and rinsed with deionized water. Then, an ultraviolet (UV)/ozone treatment was followed for 15 min to remove any organic residues and to enhance the wetting of the CdSe/ZnS QD-PMMA solution. On the ITO-coated glass substrate, the CdSe/ZnS QD-PMMA solution was spin-coated and the resulting assembly was dried on a hot plate for 20 min at $-110 \, ^\circ\text{C}$ to remove the residual solvent and to form a CdSe/ZnS QD-PMMA film. Next, a 150 nm-thick Al electrode was deposited by thermal evaporation as a counter electrode. The active area of the device was $3 \times 3 \text{ mm}^2$. Finally, to protect the device from the ambient gases during measurements, the device was encapsulated with a glass in a nitrogen ambient glove box. The current-voltage (I-V) characteristics, data retention, and the endurance characteristics of the memristors were analyzed using a semiconductor parameter analyzer (Agilent, Santa Clara, CA, USA, 4155C). The light absorption and the photoluminescence (PL) characteristics of the CdSe/ZnS QDs were analyzed using a UV/vis spectrophotometer (KLAB, Optizen pop) and a PL system equipped with a 500 W Xenon lamp as an excitation light source (PSI, Darsa-5000), respectively. Additionally, the cross-sectional structure of the device was observed using a high-resolution transmission electron microscope (HRTEM) (JEOL, JEM-2100F) to examine the dispersion of CdSe/ZnS QDs in the PMMA matrix.
3. Results
3.1. Device Structure and Electrical Characteristics

Figure 1a shows the device structure of the CdSe/ZnS QD-PMMA memristor device. The device has an asymmetric electrode structure with a high work-function ITO (Φ = 4.8 eV) used as a bottom electrode and a low work-function Al (Φ = 4.3 eV) used as a top electrode [24]. The CdSe/ZnS QD-PMMA layer, which is positioned between the ITO and Al electrodes, had an average thickness of 204.8 nm. As shown in Figure 1b, the CdSe/ZnS QDs were well dispersed in the PMMA matrix without noticeable agglomeration of the QD particles (QD concentration: 1 wt%). Figure 1c shows the light absorbance and normalized PL spectra of the CdSe/ZnS QDs, which were measured in the toluene solution. The CdSe/ZnS QDs showed an emission peak centered at around 530 nm, which corresponds to a bandgap of ~2.34 eV. Additionally, the full-width-half-maximum of the PL peak was ~34.5 nm, showing a narrow distribution of the QD size.

![Device Structure and Optical Image](image1.png)

Figure 1. (a) Device structure and an optical image of solution-processed CdSe/ZnS QD-PMMA memristors. (b) Cross-sectional TEM images of the CdSe/ZnS QD-PMMA memristor. The inset shows the structure of CdSe/ZnS QDs with oleic acid as the ligand. (c) Light absorption and photoluminescence (PL) characteristics of CdSe/ZnS QDs. (d) Current-voltage (I-V) characteristics of CdSe/ZnS QD-PMMA memristors with QD concentrations of 1 wt% and 3 wt%, and (e) 5 wt%.

In the QD-polymer based memristors, electron trapping and de-trapping occurring at the QDs play the dominant role, affecting memory characteristics such as the set/reset voltages, memory margin, and the current switching ratio [25]. In particular, the large band offset between the polymer and the QDs allows effective electron trapping at the QDs. Since the charge trapping characteristics are mainly governed by the embedded CdSe/ZnS QDs, it is necessary to optimize the CdSe/ZnS QD concentration in the polymer matrix. To optimize the QD concentration, we varied the concentration of CdSe/ZnS QDs as 1, 3, and 5 wt%, which correspond to volume concentrations of 0.21, 0.63, and 1.05 v/v%, respectively. Typical I-V characteristics of CdSe/ZnS QD-PMMA memristor devices are shown in Figure 1d when the CdSe/ZnS QD concentration was 1 and 3 wt%. Clearly, in both devices, set and reset operations accompanying abrupt changes of resistance states were observed. Initially, upon sweeping the bias to the positive bias direction, the device was in a high-resistance state (HRS). Then, at around 2.5 to 3 V, a transition to a low-resistance state (LRS) was observed, which is regarded as the set process. Particularly, at around the set bias, the current variation was approximately ~10^4 and 10^2~10^3 for 1 wt% and 3 wt% devices, respectively, which are comparable to those of TiO_2-based memristors [26]. The LRS maintained after the set process until a sufficient negative
bias was applied ($-2 \text{ V}$); then, a transition from LRS to HRS was induced. Increasing the CdSe/ZnS QD concentration to 5 wt%, however, resulted in abnormal I-V behavior showing mostly either insulating or conducting characteristics. In particular, as shown in Figure 1e, the device with conducting behavior followed the Ohmic conduction mechanism (linear I-V) with a relatively large current level ($>10^{-2} \text{ A}$), while the device with insulating behavior exhibited relatively low current levels ($<10^{-7} \text{ A}$). Since the PMMA is an insulating polymer and only a weak electric field is applied to the device during the operation ($<0.20 \text{ MV/cm}$), it is likely that the occurrence of conducting or insulating characteristics is due to the agglomeration of CdSe/ZnS QDs in PMMA. For instance, when the number of QD particles is low at a specific region, the device could operate similar to a metal-insulator-metal diode exhibiting insulating behavior. On the other hand, when the QDs are agglomerated in a restricted region, specific conductive pathways could be formed [27], resulting in a highly conducting state.

3.2. Operation Mechanism of CdSe/ZnS QD-PMMA Memristors

Concerning the set and reset processes, the operating mechanism can be described as follows. As shown in Figure 2a, due to the large difference between the lowest-unoccupied-molecular-orbital (LUMO) level of PMMA and the work function of Al, the PMMA is likely to act as a charge blocking layer. Additionally, the difference between the highest-occupied-molecular-orbital level of PMMA and the work function of ITO is large enough ($\Delta E \sim 2.5 \text{ eV}$) to effectively block the hole injection from the ITO electrode. When a positive bias is applied to the ITO electrode, electrons start to inject from the Al electrode into the CdSe/ZnS QD-PMMA layer and trapped at the CdSe/ZnS QDs (Figure 2b). Here, due to the large difference between the LUMO level of PMMA and the conduction band minimum of CdSe/ZnS QDs (2.2 to 2.6 eV) [28], it is likely that the trapped electrons are well-confined in the QDs. Then, when a sufficiently high bias is applied, the electric field formed between the QDs is increased, and consequently, the electronic occupation probability of the QDs increases [25], leading to a shift of Fermi level toward the LUMO level of PMMA [25]. This, in fact, may generate conducting filaments in the CdSe/ZnS QD-PMMA layer, resulting in an LRS. On the other hand, when a negative bias is applied to the ITO electrode, electrons are de-trapped from the CdSe/ZnS QDs and the device returns to the initial HRS, as shown in Figure 2c.

![Figure 2](image_url)

**Figure 2.** (a) An energy band diagram of the CdSe/ZnS QD-PMMA memristor. The change in the energy band diagram of the device during (b) set, and (c) reset process.

Obtaining uniform and stable switching characteristics is a prerequisite for realizing highly reliable memristor devices. To evaluate the operational stability of the CdSe/ZnS QD-PMMA memristors, the I-V characteristics were measured repeatedly for 50 times and the variation of the switching behavior was analyzed. Figure 3a shows the I-V curves obtained at the 1st, 25th, and 50th measurements. As displayed, the device exhibited stable switching characteristics during the repetitive operation with the current switching ratio in the range of $10^3$ to $10^4$. Figure 3b,c show the corresponding cumulative distribution of currents at LRS and HRS, and the variation of set/reset voltages, respectively. Particularly, the current at the LRS was in the range of $2.0 \times 10^{-6} \text{ A}$, and at HRS, the current was in the range of $0.7 \sim 7.3 \times 10^{-7} \text{ A}$. Additionally, the set and reset voltages were varied...
in the ranges of 2.09 ± 0.159 V and −1.26 ± 0.307 V, respectively. Nonetheless, these results show that the CdSe/ZnS QD-PMMA memristors exhibit relatively stable switching characteristics.

![Figure 3. (a) I-V characteristics of CdSe/ZnS QD-PMMA memristors during a cyclic test (50 cycles) (QD: 1 wt%). (b) The variation of LRS and HRS currents during the cyclic test. (c) The distribution of set and reset voltages during the cyclic test.](image)

3.3. Operation Stability of CdSe/ZnS QD-PMMA Memristors

To further demonstrate the stable switching operation of CdSe/ZnS QD-PMMA memristors, the data retention and the endurance characteristics were analyzed. Particularly, the data retention and the endurance characteristics are important for memristor devices because they reflect the reliability of memory functions. Additionally, since the switching between the LRS and HRS relies on the trapping and de-trapping of electrons at the CdSe/ZnS QDs, it is important to determine any undesired degradation of the device which may result in a loss of memory state. To evaluate the data retention characteristics of CdSe/ZnS QD-PMMA memristors, the device was programmed to either the LRS or HRS state using a $V_{\text{bias}}$ of +3 V or −3 V, respectively, and the variation of the current level was traced with $V_{\text{read}}$ of +1 V. Here, $V_{\text{read}}$ was set to +1 V, which is lower than the typical set bias. Figure 4a shows the time-dependent current variation for LRS and HRS states up to ~10 ks. As displayed, the LRS and HRS states were well-maintained without a significant change in the current level. The corresponding current switching ratio variation is shown in Figure 4b, and up to ~10 ks, the switching ratio was maintained at around $10^3$. These results indicate that the electrons trapped at the CdSe/ZnS QDs are energetically stable and the de-trapping and/or recombination of electrons rarely occurred during this period. Figure 4c shows the endurance measurement data in which the set and reset operations were repeatedly performed for up to 500 cycles. Here, the $V_{\text{set}}$ and $V_{\text{reset}}$ were +3 V and −3 V, respectively, and each $V_{\text{set}}$ or $V_{\text{reset}}$ was applied for 50 ms ($V_{\text{read}} = +1$ V). As shown in Figure 4c, the device exhibited relatively stable switching between LRS and HRS with the current switching ratio maintaining at ~$10^3$ (Figure 4d). We observed, however, that after around 400 cycles of set/reset switching, the device started to show occasional unstable operation with reduced switching ratios. This can be more clearly identified in Figure 4d, where the variation of the current switching ratio is displayed as a function of the cycle number. These results imply that the device may experience partial degradation, possibly owing to the change in the conduction mechanism.

3.4. Degradation Mechanisms

To closely investigate the possible origin for the instability occurring at high-number cycles, the conduction mechanism change during the switching operation was analyzed in detail. Figure 5a,b show the $\ln I$ vs. $\ln V$ plots for the CdSe/ZnS QD-PMMA memristor before (fresh device) and after the degradation (device underwent 500 endurance cycles), respectively. The fresh device showed a clear difference in the conduction mechanism at HRS and LRS regions. Initially in the HRS region, the I-V curve followed $I \propto V^{0.2}$. Then, at around the set voltage (+2.3 V), the slope ($\alpha$) becomes larger than 2, indicating a transition to the trap filling regime or the TCLC [30]. The presence of the TCLC regime is an indication that the traps are exponentially distributed in the forbidden gap [30], and at this stage,
the injected electrons fill the trap levels. Following, after the set process, the dominant conduction mechanism changes to trap-free SCLC, showing the relation, \( I \propto V^{1.89} \). Ideally, for the trap-free SCLC, the I-V is related by the following equation [17,31].

\[
I \propto \frac{9\varepsilon_i \mu V^2}{8d^3}
\]

(1)

where \( \varepsilon_i \) is the insulator permittivity, \( \mu \) is the carrier mobility and \( d \) is the insulator thickness. As displayed in Figure 5a, the \( \alpha \) value in the LRS region (1.89) is similar to that of the ideal case, suggesting that most of the traps are filled with the electrons during the set process. These transitions in conduction mechanism are in a good agreement with the operation mechanism described in Figure 2. After the degradation, however, the dominant conduction mechanisms and their transitions are significantly different from the fresh device. Figure 5b shows the \( \ln I \) vs. \( V \) plot, which is measured after the degradation. Interestingly, the I-V characteristics were similar in both forward and reverse sweeps. For the forward and reverse sweeps, the corresponding \( \alpha \) values were 3.38 and 3.58, respectively. Thus, the dominant conduction mechanism is considered as the TCLC, suggesting that during the repeated operation, additional traps are created in the CdSe/ZnS QD-PMMA layer, preventing the occurrence of trap-free SCLC behavior. Previously, it has been reported that electronic trap states can be created and eliminated in the CdSe CQDs [31]. Particularly, by doping and charging, atomic dimmers at the QD surface can be formed or broken, creating trap states within the bandgap [32]. Moreover, the oxidation of reactive metallic components in QD particles can be another possible reason for the creation of additional trap states. Nevertheless, from our observation, it is clear that the dominant conduction mechanism is changed after the degradation, possibly originating from the creation of additional trap states in the CdSe/ZnS QD-PMMA layer. Therefore, to obtain highly reliable QD-polymer-based memristors, surface-stabilized QDs and the prevention of oxidative reactions would be necessary.

![Figure 4](image-url)

**Figure 4.** (a) The data retention characteristics of the CdSe/ZnS QD-PMMA memristor (QD: 1wt%). The LRS and HRS states were programmed with biases of +3 V and −3 V, respectively. Additionally, the \( V_{\text{read}} \) was +1 V. (b) The variation of current switching ratio during the data retention test up to \( 10^4 \) s. (c) The endurance cyclic test data of the CdSe/ZnS QD-PMMA memristor (500 cycles). The LRS and HRS states were programmed with biases of +3 V and −3 V, respectively. Additionally, the \( V_{\text{read}} \) was +1 V. (d) The variation of current switching ratio during the endurance test.
In this paper, we demonstrated solution-processed CdSe/ZnS QD-PMMA-based memristors for potential memory and neuromorphic applications. The fabricated memristors exhibited a high retention time over $10^4$ s and good stability, having an endurance cycle up to 400 times. Additionally, to understand the degradation mechanism, we investigated the conduction mechanism change before and after the degradation. It was determined that the dominant conduction mechanism changed from the trap-free SCLC mechanism to TCLC, suggesting that additional trap states are generated in the CdSe/ZnS QD-PMMA layer during the repeated operation, causing a permanent failure of the device.

Figure 5. (a) Current-voltage (I-V) curves of the CdSe/ZnS QD-PMMA memristor, (a) fresh device, and (b) after degradation.

4. Conclusions

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