Method for Evaluating the Degree of Metallization Corrosion Damage of Integrated Circuits under Accelerated Tests

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Abstract. This paper focuses on evaluation results of accelerated tests for integrated circuits metallization corrosion resistance. It has been proposed to use the average area of corrosion damage to bond pads and the average number of metallization damages as an indicator of the degree of metallization damage. The evaluation method is applicable for comparative tests of various design and technological options for integrated circuits manufacture.

1. Introduction
Currently, a significant part of industrial electronics and IT equipment hardware components used in industrial or civil construction facilities is digital integrated circuits (IC) such as microprocessors, microcontrollers, encoders/decoders, digital-to-analog converters, etc. It means that functional reliability of these facilities will be largely determined by ICs reliability.

Technology based on the use of complementary transistors with the structure of metal-oxide-semiconductor (CMOS IC) is now widely used in the manufacture of digital ICs. Its main advantages are low power consumption and a wide range of supply voltages. However, these advantages, on the other hand, also led to low corrosion resistance of IC metallization. As a result, special technological measures were required to increase its corrosion resistance, as well as methods to evaluate effectiveness of these measures.

There are two methods to improve ICs reliability:
- eliminate causes of operational failures by improving the technology and using more stringent process control;
- identify potentially unreliable ICs and remove them from the batch at the stage of accelerated screening tests (QA test) of finished ICs [1].

The first method is more efficient, however, the best result is achieved when it is combined with the second method.

To assess sealed CMOS IC resistance to metallization electrolytic corrosion (second method), generally, the median time to failure is used as resistance indicator [2]. The tests are carried out using heat and cold chambers where ICs run under normal electrical conditions for several hundred hours, which significantly increases the cost of testing.

To assess how ICs design and manufacturing process features affect metallization corrosion resistance (first method), it is reasonable to apply stress test methods, during which unsealed ICs are exposed to high temperature and humidity in combination with the supply voltage [3].

It is feasible to compare test results under these conditions based not on time between failures, but on the scale of metallization corrosion damage.

However, using mean time between failures as a corrosion resistance indicator for assessing results of such tests is not feasible. This leads to considerably higher cost of tests and lower integrity of
results due to a larger number of parametric failures that are caused by a relatively thick water film forming on the surface of IC chip.

The method of metallization resistance assessment by bond pad surface discoloration as observed through an optical microscope has been described in several studies [4, 5]. However, it is not sufficiently accurate since evaluation of discoloration degree is subjective, and it is not suitable to assess damages observed in the case of electrolytic corrosion.

Due to the above-mentioned reasons, this study aims at developing a simple method for assessing the degree of corrosion damage to IC bond pad metallization specific for electrolytic corrosion.

2. Methods
The method of unsealed ICs accelerated testing in unsaturated water vapor at elevated temperatures with simultaneous electrical voltage used in this paper does not replace sealed ICs tests and is not intended to verify ICs reliability. Its purpose is a comparative assessment of aluminum metallization corrosion resistance for various design and technological options in IC manufacture.

The following conditions are selected as basic ones [6]:
- relative humidity of 85%, temperature of 85°C (implemented using a heat and humidity chamber);
- relative humidity of 85%, temperature of 120°C (implemented using autoclave).

If purpose-built equipment is not available, the conditions of 100% relative humidity, 85°C temperature are accepted with mandatory control of electrolytic corrosion process self-similarity.

Tests duration is determined by their purpose, laboratory equipment capabilities, IC design and technological features, and the selected conditions. The minimum test time is 72 hours for the heat and humidity chamber, 66 hours for the autoclave.

This paper proposes to use the value of corrosion damage area derived as the average of cathode \( \Delta S_k \) and anode \( \Delta S_a \) bond pads area as an indicator that directly characterizes metallization resistance to electrolytic corrosion. This parameter may be used for an approximate quantitative assessment of corrosion resistance, as well as for comparative assessment of the rate of corrosion processes.

The bond pad area \( \Delta S \) affected by corrosion is determined using:

\[
\Delta S = \left( \frac{(S_0 - S_n)}{S_0} \right) \times 100\%
\]

where \( S_0 \) is the bond pad aluminum area observed in the optical microscope prior to start of test (not including the area closed from the observer by the thermo-compression bonding); \( S_n \) is the undamaged aluminum bond pad area at the end of tests. An example of \( \Delta S_k \) assessment is shown in figure 1, 2.

Further, the \( \overline{\Delta S} \) average value of all tested ICs is calculated separately for the cathode \( \Delta S_k \) and anode \( \Delta S_a \) bond pads:

\[
\overline{\Delta S_k} = \frac{1}{N_k} \sum_{j=1}^{N_k} \Delta S_{kj} = \frac{1}{n N_k} \sum_{j=1}^{N_k} \sum_{l=1}^{n} \Delta S_{kl}
\]

\[
\overline{\Delta S_a} = \frac{1}{N_a} \sum_{j=1}^{N_a} \Delta S_{aj} = \frac{1}{n N_a} \sum_{j=1}^{N_a} \sum_{l=1}^{n} \Delta S_{aj}
\]

where \( n \) is the number of tested ICs; \( N_k, N_a \) is the number of cathode and anode bond pads in each IC.
Figure 1. Corrosion damage of IC bond pads and interconnects ($\Delta S = 20\%$, $M = 18$).

Figure 2. Corrosion damage of IC bond pads in SEM ($\Delta S = 10\%$).

The average number of corrosion spots on the interconnects (excluding bond pads) of a single chip $\bar{M}$ is determined by:

$$\bar{M} = \frac{1}{n} \sum_{i=1}^{n} M_i$$

(4)
where \( n \) is the number of ICs from one batch undergoing corrosion resistance assessment; \( M_i \) is the number of spots on chip metallization of the \( i \)-th IC.

When conducting tests for the purpose of quick response quality control of the IC manufacturing process, the level of metallization corrosion resistance is unsatisfactory if corrosion damage of aluminum is observed on bond pads and interconnects.

When conducting comparative tests of aluminum metallization corrosion resistance for various design and technological IC options, quantitative assessment of the degree of metallization corrosion damage is made separately for cathode \( \Delta S_k \) and anode \( \Delta S_a \) contact pads, as well as \( \overline{M} \) interconnects.

3. Discussion of the results

The proposed method for assessing the degree of metallization corrosion damage and indicators are sufficiently informative, reliable and reproducible.

In particular, it is possible to directly check the degree of metallization corrosion damage by visual inspection, as well as effectively use extensive statistical material. For example, when testing 20 ICs in 16-pin bodies, the \( \Delta S_k \) and \( \Delta S_a \) values are calculated as the average of 160 values each, which increases evaluation results integrity.

The method of assessing corrosion damage degree was used for corrosion resistance comparative assessment of 564 series IC (Russian analogue CD4000A) before and after the implementation of measures to increase IC corrosion resistance.

The table shows some results of corrosion resistance assessment of 564 series IC. The tests were carried out at a relative humidity close to 100%, which was due to the need to evaluate, first of all, metallization resistance to high humidity exposure.

| IC batch No. | Design and technological option | Test conditions | | | |
|--------------|-------------------------------|----------------|-----|-----|-----|
|              |                               | 85°C/100%/15 V | 121°C/100%/15 V | \( \Delta S_k \), % | \( \overline{M} \), pc. | \( \Delta S_a \), % | \( \overline{M} \), pc. |
| 1            |                               | 65             | 45   | 11  |
| 2            | Before the implementation of measures | 97             | 11   | 0.7 |
| 3            |                               | 77             | 0.9  | 0.3 |
| 4            |                               |               | 72   | 7   |
| 5            | After the implementation of measures | 0              | 0    | 0   |
| 6            |                               | 0              | 0    | 0   |

Obviously, the proposed assessment method allows us to confirm the effectiveness of measures to increase the corrosion resistance of IC metallization (selection of metallization composition and application method, additional protective films, reducing the chip surface contamination level).

Also, the assessment method can be used to assess the test results of various additional surface protection systems for an IC chip. For example, such as silicone coatings, polymers and photoresists [7].

4. Conclusions

The proposed method for assessing corrosion damage degree based on average damaged area separately for cathode \( \Delta S_k \) and anode \( \Delta S_a \) bond pads helps assess the degree of damages specific for electrolytic metallization corrosion. This method does not require big financial investments and complex diagnostic equipment and allows to effectively conduct the comparative assessment of
aluminum metallization corrosion resistance for various design and technological options of IC manufacture.

The assessment method is easy to implement and has sufficient efficiency and statistical stability.

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