Abstract—We propose a new family of spatially coupled product codes, called sub-block rearranged staircase (SR-staircase) codes. Each SR-staircase code block is constructed by encoding rearranged preceding code blocks and new information blocks, where the rearrangement involves sub-blocks decomposition and transposition. The proposed codes can be constructed to have each code block size of $1/q$ to that of the conventional staircase codes while having the same rate and component codes, for any positive integer $q$. In this regard, we can use strong algebraic component codes to construct SR-staircase codes with a similar or the same code block size and rate as staircase codes with weak component codes. Moreover, both waterfall and error floor performance can be further improved by using a large coupling width. The superior performance of the proposed codes is demonstrated through density evolution and error floor analysis as well as simulation.

I. INTRODUCTION

Modern optical transport networks (OTN) are required to support data transmission of 400 Gbit/s and beyond over long distances. As a result, the use of most packet retransmission protocols becomes inefficient. This necessitates the design of low-complexity forward error correction (FEC) coding schemes that can achieve a rate close to capacity while having extremely low error floor. Particularly, a bit error rate (BER) lower than $10^{-15}$ is required in the error floor region [1], [2]. Spatially coupled low-density parity-check codes [3] have become the popular candidates for OTN [4] due to their close-to-capacity performance and low error floor [5], [6]. However, their remarkable performance requires soft-decision decoding which poses several challenges in implementation, such as large internal data flow [7] and high hardware and power cost for enabling high-resolution analog-to-digital conversion.

The FEC codes based on hard-decision decoding have significantly lower decoding complexity and hardware costs, which makes them appealing to OTN. The authors in [7] proposed staircase codes by applying spatial coupling to product codes [8] with Bose-Chaudhuri-Hocquenghem (BCH) component codes. Staircase codes can achieve a performance within 0.56 dB from the capacity of the binary symmetric channel (BSC) under iterative bounded distance decoding (iBDD) [2] and outperform existing FEC solutions in ITU-T G.975.1 [9]. Another class of spatially coupled product codes called braided block codes were introduced in [10], which, when using BCH component codes, i.e., braided BCH codes [11], have comparable error performance to staircase codes. Both codes [7], [11] can be described under a unified framework named “zipper codes” [12]. The authors in [12] also proposed tiled diagonal zipper codes which can be seen as a combination of continuously interleaved BCH codes [13] and staircase codes [7].

In addition to spatial coupling, another line of work is to construct symmetry-based product codes [14] to reduce the blocklength of product codes [15] while having the same component code and similar code rates. Thanks to this property, one can also employ stronger algebraic component codes to construct symmetry-based product codes in a bid to achieve better waterfall and error floor performance while maintaining similar blocklengths and code rates as the conventional product codes. The first examples of such codes are half-product codes [16], whose codewords are derived from product codes with the additional constraint that the code arrays are antisymmetric, thereby leading to an effective blocklength about half to that of the product codes. Later, this idea motivated the design of quarter-product codes and octal-product codes in [17] as well as half-braided BCH codes in [18]. However, all the above symmetric-based product codes require square code blocks and the same component codes for row and column encoding. In addition, the codes in [17] restrict the component codes to be reversible (i.e., a code that is invariant under a reversal of the coordinates in each codeword [19]). These restrictions reduce the design space of symmetric-based product codes and may limit their potential applications.

This paper focuses on designing new FEC schemes under low-complexity iBDD to achieve better waterfall and error floor performance with lower miscorrection probability than staircase codes [7] with similar blocklengths and rates. Motivated by spatial coupling and symmetry, we propose sub-block rearranged staircase (SR-staircase) codes. The proposed codes can be constructed to have each code block with a size of $1/q$ to that of the conventional staircase codes with the same algebraic component codes while maintaining the same code rate, for any positive integer $q$. This means that we can employ stronger algebraic component codes to construct SR-staircase codes with a similar or the same code block size and rate as staircase codes with weak component codes. However, unlike all the aforementioned symmetric-based product codes, the proposed codes do not impose any additional constraint on the component codes and code array shapes. We use density...
evolution to characterize the decoding thresholds on the BSC and investigate the error floor by analyzing the contributing error patterns. Both theoretical and simulation results show that the designed SR-staircase codes achieve better waterfall and error floor performance over the conventional staircase codes under iBDD. Moreover, the decoding threshold and error floor of SR-staircase codes can be further improved by using a large coupling width.

This paper uses the following notations. Let \( \mathbb{N} \) represent the set of natural numbers. The sets of even and odd natural numbers are represented by \( 2\mathbb{N} \) and \( 2\mathbb{N} - 1 \), respectively. We define \( [n] \triangleq \{1, \ldots, n\} \) for any \( n \in \mathbb{N} \). \([x]\) gives the nearest integer that is not less than \( x \). The indicator function is represented by \( \mathbb{1}\{\cdot\}\).

II. SUB-BLOCK REARRANGED STAIRCASE CODES

We consider that the underlying component codes are binary primitive BCH codes. A SR-staircase code comprises a sequence of code blocks \( B_1, B_2, \ldots \). At time \( i \in \mathbb{N} \), code block \( B_i = [K_i, P_i] \) is a concatenation of information block \( K_i \) and parity block \( P_i \). To construct the SR-staircase code, two shortened BCH codes \( C_j \) for \( j \in \{1, 2\} \) are used. We denote by \( k_j, n_j, t_j, e_j \), and \( G_j \), the message length, codeword length, error correction capability, shortening parameter, and generator matrix, respectively, of \( C_j \). Note that we can also express the codeword length and information length of \( C_j \) as \( n_j = 2^\nu_j - 1 - e_j \) and \( k_j = 2^\nu_j - 1 - t_j - e_j \), respectively, for some positive integers \( \nu_j \geq 3 \), where \( \nu_j \) is Galois field extension [20] Chap. 3.3.

A. Construction

The encoding of SR-staircase codes is performed in a recursive manner like the conventional staircase codes. The main difference is that each preceding SR-staircase code block \( B_{i-1} \) is decomposed into \( q_1 \) equal-size sub-blocks if \( i \in 2\mathbb{N} - 1 \) and \( q_2 \) equal-size sub-blocks if \( i \in 2\mathbb{N} \). Each sub-block is then transposed and encoded row-by-row with BCH encoding to obtain the current code block \( B_i \). The size of \( B_i \) is \( \frac{m_n}{q_1} \times m_2 \) if \( i \in 2\mathbb{N} - 1 \) and \( \frac{m_n}{q_2} \times m_1 \) if \( i \in 2\mathbb{N} \). Moreover, all the bits in each row of \( B_i \) are the last \( m_j \) bits of a codeword of \( C_2 \) when \( i \in 2\mathbb{N} - 1 \) and the last \( m_1 \) bits of \( C_1 \) when \( i \in 2\mathbb{N} \). Note that the numbers of columns for \( B_i \), \( m_1 \) and \( m_2 \), have to be divisible by \( q_1 \) and \( q_2 \), respectively. We also denote by \( w \) the coupling width, where \( w \geq 2 \) and both \( m_1 \) and \( m_2 \) have to be divisible by \( w - 1 \).

1) Case \( w = 2 \): For ease of presentation, we first describe the encoding steps for \( i \in 2\mathbb{N} \).

Step 1 (Initialization): Set all the entries of \( B_0 \) to zero: \( B_0 = 0_{\frac{m_n}{q_1} \times m_2} \), which are known by the encoder and decoder.

Step 2 (Decomposition): The preceding block \( B_{i-1} \) with size \( \frac{m_n}{q_1} \times m_2 \) is divided into \( q_2 \) consecutive equal-size sub-blocks with size \( \frac{m_n}{q_1} \times \frac{m_2}{q_2} \) as

\[
B_{i-1} = [B_{i-1,1}, B_{i-1,2}, \ldots, B_{i-1,q_2}].
\]

Step 3 (Transposition): Apply matrix transpose to each sub-block decomposed from \( B_{i-1} \) in Step 2 and recombine all the transposed sub-blocks into a size \( \frac{m_n}{q_2} \times \frac{m_1}{q_1} \) block \( B_{i-1}^T \)

\[
B_{i-1}^T = \left[ B_{i-1,1}^T, B_{i-1,2}^T, \ldots, B_{i-1,q_2}^T \right].
\]

Each sub-block \( B_{i-1,l}^T \) has a size of \( \frac{m_n}{q_2} \times \frac{m_1}{q_1} \) for \( l \in [q_2] \). Note that all bits in the same column position of every transposed sub-block, \( B_{i-1,1}, \ldots, B_{i-1,q_2}^T \), belong to the same BCH component codeword of \( C_2 \).

Step 4 (Array Concatenation): Construct the message matrix with size \( \frac{m_n}{q_2} \times (k_1 + e_1) \) to be encoded at time \( i \),

\[
K_i = \left[0_{\frac{m_n}{q_2} \times e_1}, B_{i-1}^T, K_i \right],
\]

where \( K_i \) is an \( \frac{m_n}{q_2} \times (k_1 - m_n q_2 / q_1) \) block filled with information bits, and \( 0_{\frac{m_n}{q_2} \times e_1} \) represents the block filled with shortened bits.

Step 5 (Component Code Encoding): Obtain the codeword matrix with size \( \frac{m_n}{q_2} \times n_1 \) at time \( i \) as

\[
C_i = K_i^i G_1
= \left[0_{\frac{m_n}{q_2} \times e_1}, B_{i-1}^T, K_i, P_i \right]
= \left[0_{\frac{m_n}{q_2} \times e_1}, B_{i-1}^T, B_i \right].
\]

where \( P_i \) is the parity block with size \( \frac{m_n}{q_2} \times (n_1 - k_1) \), and \( B_i = [K_i, P_i] \) is an \( \frac{m_n}{q_2} \times m_1 \) code block to be transmitted. Each row of \( \left[ B_{i-1}^T, B_i \right] \) is a shortened codeword of \( C_1 \).

The steps to obtain \( B_i \) for \( i \in 2\mathbb{N} - 1 \) are similar to the above. After Step 5, each row of \( \left[ B_{i-1}^T, B_i \right] \) is a shortened codeword of \( C_2 \) for \( i \in 2\mathbb{N} - 1 \). For \( B_i \), the relation between the component codeword length, time index \( i \), the number of decomposed sub-blocks, and the number of columns satisfies

\[
n_1(i) = m_n - \frac{m_n}{q_1} \phi(i) - \frac{m_n}{q_2} \phi(i - 1) - \frac{m_n}{q_1} \phi(i),
\]

where \( \phi(\cdot) \) is a mapping function such that \( \phi(x) = \frac{3x - 1}{2} \).

Finally, Steps 1-5 are performed for \( i \geq 1 \) to obtain all code blocks. The code rate is

\[
R = \frac{1}{2} \left( \frac{k_1}{m_1} + \frac{k_2}{m_2} - \frac{q_2}{q_1} \right).
\]

Note that in Step 3, the transformation of \( B_{i-1} \) into \( B_{i-1}^T \) in (2) can be generalized by adding a permutation function \( \pi(\cdot) \) which permutes the rows and columns of a matrix, i.e.,

\[
B_{i-1}^\pi = \pi \left( B_{i-1,1}^T, B_{i-1,2}^T, \ldots, B_{i-1,q_2}^T \right).
\]

Alternatively, Step 3 may be described by using the zipper code framework [12] by specifying a bijective interleaver map which maps the position of each bit from \( B_{i-1} \) to \( B_{i-1}^T \).
2) Case \( w > 2 \): In this case, we need to ensure that each sub-block used for coupling has the same size. This is possible if and only if \( m_1 = m_2 \equiv m \) and \( q_1 = q_2 \equiv q \). Consider \( i \in 2\mathbb{N} \). To obtain \( B_i \), we first modify Step 1 of the encoding in Sec. II-A1 by setting \( B_0, \ldots, B_{w-2} \) to all-zero matrices. Next, we modify Step 4 by further dividing the transformed preceding code block \( B_{i-l}^\pi \) obtained from (2) into \( w - 1 \) consecutive equal-size sub-blocks for \( l \in [w-1] \), i.e., \( B_{i-l}^\pi = [B_{i-l-1}^\pi, \ldots, B_{i-l-w+1, w-1}^\pi] \), where each sub-block is an \( \frac{m_1}{w-1} \times \frac{m_2}{w-1} \) binary matrix. Then, the message matrix to be encoded at time \( i \) is constructed by taking the \( l \)-th sub-block of preceding transformed code block \( B_{i-l}^\pi \) for \( l \in [w-1] \), i.e., \( K_i' = \{0, \ldots, e_i, B_{i-1,1}^\pi, B_{i-2,2}^\pi, \ldots, B_{i-w+1, w-1}^\pi, K_i \} \). The rest of the encoding steps are the same as those in Sec. II-A1.

It is important to note that when \( w \geq q + 1 \), the bits in different column positions of the coupled block \( [B_{i-1,1}^\pi, \ldots, B_{i-w+1, w-1}^\pi] \) in \( K_i' \) are protected by different component codewords because any pair of sub-blocks, \( B_{i-l}^\pi \) and \( B_{i-l'}^\pi \) with \( l \neq l' \) and \( l, l' \in [w-1] \), are decomposed from different preceding code blocks.

B. Connections to Other Spatially Coupled Codes

SR-staircase codes are motivated and derived by introducing symmetry in the conventional staircase codes [7]. Consider a SR staircase code with \( w = 2 \) and let \( q \equiv q_1 = q_2 \). By concatenating \( q \) identical SR-staircase code blocks \( B_i \), one obtains the resultant code block as \( B_i^* = [B_i^1, \ldots, B_i^{\pi}] \). \( B_i^* \) is obtained by encoding rearranged preceding block \( B_{i-1}^\pi = [(B_{i-1}^{\pi})^T, \ldots, (B_{i-1}^{\pi})^T]^T \), where the construction of \( B_{i-1}^\pi \) follows either (2) or (3). As a result, each row of \( [B_{i-1}^\pi, B_i] \) is a valid codeword of \( C_i \) when \( i \in 2\mathbb{N} \) and \( C_2 \) when \( i \in 2\mathbb{N} - 1 \). Clearly, each code block \( B_i^* \) is drawn from a subset of the set of the conventional staircase code blocks due to symmetry, i.e., having \( q - 1 \) replicas of \( B_i \). Thus, the staircase code \( B_1^*, \ldots, B_w^* \) is a subcode of the conventional staircase code. Notice that when \( q = 1 \), the encoding steps in Sec. II-A1 produce the conventional staircase codes. By removing any \( q - 1 \) replicas of \( B_i \) as they do not contain any new information, the resultant SR-staircase codes achieve the same rates and an effective block size of \( 1/q \) to the staircase codes from which they are derived. In this regard, the proposed construction allows one to employ stronger BCH codes to construct SR-staircase codes with improved error performance while maintaining similar or the same block sizes and rates compared to the conventional staircase codes.

SR-staircase codes can also be seen as a generalization of the tiled diagonal zipper codes in [12]. Specifically, one can obtain a tiled diagonal zipper code from the proposed construction by enforcing \( C_1 = C_2 \), \( w - 1 = q_1 = q_2 \), \( m_1 = m_2 \), and using a specific block interleaver. However, we emphasize that the proposed codes are motivated and derived by applying the idea of symmetry-based product codes [14], [17] to staircase codes [7] starting from \( w = 2 \) as illustrated above. Compared to tiled diagonal zipper codes, the proposed codes have a more flexible structure suitable for a wider range of applications and the design of code parameters will be justified via density evolution and error floor analysis.

It is also worth noting that the proposed construction is related to the class of partially coupled codes, i.e., [21]–[23]. This can be seen by noting that a fraction of information and/or parity bits in one code block are repeated and coupled to become a part of the input to the encoders of consecutive code blocks. All repeated bits are punctured before transmission. This allows us to employ stronger component codes to improve the overall performance of the coupled codes.

C. Decoding

We restrict the decoding to be iBDD similar to [7] Sec. IV-A] due to its simplicity and low complexity. The detailed decoding steps are omitted due to space limitations. We will see in Sec. V that the performance of SR-staircase codes under iBDD is close to that under miscorrection-free iBDD [24] due to the use of BCH component codes with larger \((t_1, t_2)\).

III. DECODING THRESHOLD ANALYSIS

A. Graph Model

Following the approach in [25], we consider a deterministic code structure since the interleaver of the proposed codes is fixed. The analysis performed on a deterministic code structure allows one to make precise statements about the performance of actual codes.

For illustrative purpose, we consider the case of \( w = 2 \). From Sec. II-A1 we know that code block \( B_i \) has \( \frac{m_2}{q_1} \) rows for \( i \in 2\mathbb{N} \) and \( \frac{m_2}{q_1} \) rows for \( i \in 2\mathbb{N} - 1 \). By using the Tanner graph representation [26], it can be seen that the \( i \)-th spatial position (time instance) on the graph has \( \frac{m_2}{q_1} \) check nodes (CNs) when \( i \in 2\mathbb{N} \) and \( \frac{m_2}{q_1} \) CNs when \( i \in 2\mathbb{N} - 1 \) because one component codeword poses constraints on a row of \( B_i \). Each bit in \( B_i \) is represented by a variable node (VN) that connects a pair of CNs in the \( i \)-th and \((i + 1)\)-th spatial positions via an edge. Thus, each VN always has degree 2. All CNs in any two neighboring spatial positions are fully connected. More precisely, each pair of CNs in the two neighboring spatial positions \( i \) and \( i + 1 \) are connected via \( q_1 \) and \( q_2 \) edges for \( i \in 2\mathbb{N} \) and \( i \in 2\mathbb{N} - 1 \), respectively, where a VN lies on each edge. We use an example to illustrate the graph representation of a SR-staircase code with given specific parameters.
Example 1. Consider a SR-staircase code with \((m_1, m_2) = (4, 9)\) and \((q_1, q_2) = (2, 3)\). The code blocks and the corresponding graph model of this SR-staircase code are shown in Fig. 1(a) and Fig. 1(b), respectively. Sub-blocks are indicated in different colors. Consider \(i \in 2\mathbb{N}\). Since each VN always has degree 2, we use an edge to represent a VN that connects a pair of CNs for simplicity. We label two bits in \(B_j\), i.e., \(B_j(3, 1)\) and \(B_j(2, 4)\), in Fig. 1(a) and mark their corresponding edges (VNs) in the Tanner graph with the same color in Fig. 1(b).

Notice that when \(\min(q_1, q_2) \geq w = 2\), the SR-staircase code has a multi-edge graph representation shown in Fig. 1(b) such that every \(q\) bits are protected by two component codewords. When \(q_1 = q_2 = q\) and \(w \geq q+1\), the SR-staircase code has a single-edge graph representation according to the construction in Sec. II-A. When \(2 < w < q+1\), the connectivity between CNs is mixed with single-edge and multi-edge. For this case, the number of connecting edges ranges from 1 to \(\lceil \frac{q}{w-1} \rceil\) and depends specifically on \((q, w)\).

B. Density Evolution

We derive the DE equations based on the graph model in (II-A). The analysis is performed on the BSC. To make precise statements about the performance of the proposed codes with deterministic structures under iBDD, we adopt the approach in [23] to perform DE analysis. Moreover, we assume that the iBDD is miscorrection-free according to [23].

We start with the case of \(w = 2\). Consider the SR-staircase code constructed in Sec. II-A with code blocks \(B_i, i \in [L]\). Let \(p\) be the crossover probability of a BSC. We define the effect channel quality to be

\[
\lambda_{\varphi(i)} \triangleq \frac{m_{\varphi(i)} \cdot q_{\varphi(i)}(i-1)}{q_{\varphi(i)}},
\]

(7)

whose operational meaning is the expected average number of bits received in errors per component code constraint of \(C_{\varphi(i)}\) and \(\varphi(.)\) is a mapping function defined right after (5). We further define a parameter \(x_i^{(t)}\), \(i \in [L]\), whose operational meaning is that the probability of a randomly chosen erroneous bit attached to a component code of \(C_{\varphi(i)}\) in \(B_i\) is not recovered after \(t\) decoding iterations converges asymptotically to \(x_i^{(t)}\). DE is performed by tracking \(x_i^{(t)}\). Define \(f(\lambda, t) \equiv 1 - \sum_{j=1}^{t-1} \frac{\lambda^j}{j!} e^{-\lambda}\) to be the complementary Poisson cumulative distribution function for a Poisson random variable \(\lambda\) with support \(t\). Following [23], the DE equation for SR-staircase codes is

\[
x_i^{(t)} = f \left( \frac{M_{\varphi(i)}}{2} \left( x_{i-1}^{(t-1)} + x_{i+1}^{(t-1)} \right), \lambda_{\varphi(i)} \right),
\]

(8)

where \(x_i^{(0)} = 1\) for \(i \in [L]\) and \(x_i^{(t)} = 0\) for \(i < 1\) and \(i > L\). Note that since \(q_{\varphi(i)}\) is fixed and \(n_{\varphi(i)} \gg q_{\varphi(i)}\) and based on the argument in [27] Sec. IV-A, the DE equation (8) can be applied to the proposed codes regardless of whether the Tanner graph is single-edge or multi-edge. The BSC decoding threshold is defined as \(\tilde{p} \triangleq \sup \{ p > 0 \mid \lim_{t \to \infty} x_i^{(t)} = 0 \_L \}\).

When \(w > 2\), we let \(m_1 = m_2 \triangleq m\) and \(q_1 = q_2 \triangleq q\) according to Sec. II-A. The expected number of initial errors per component code is \(M_1 = M_2 \triangleq M\). Due to coupling, the \(l\)-th sub-block of preceding code block \(B_{i-1}\) for \(l \in [w-1]\) is used as a part of the inputs to encode \(B_i\) while \(B_i\) is also used as a part of the inputs to encode \(B_{i+1}, \ldots, B_{i+w-1}\). The DE equation in (8) is then modified to

\[
x_i^{(t)} = f \left( \frac{M_{\varphi(i)}}{2(w-1)} \sum_{j=1}^{w-1} (x_{i-j}^{(t-1)} + x_{i+j}^{(t-1)}), \lambda_{\varphi(i)} \right). \quad (9)
\]

C. Decoding Threshold Results

We use the above DE equations to compute the decoding threshold. For illustrative purpose, we consider \(\nu_1 = \nu_2 \triangleq \nu\), \(m_1 = m_2 \triangleq m\), \(q_1 = q_2 \triangleq q\), and assume full decoding of the entire spatial code chain. The decoding thresholds of the proposed codes and some existing staircase codes are reported in Table I. It can be observed that the proposed codes achieve a lower threshold than the conventional staircase codes for the same or similar rates and with comparable block sizes. Moreover, increasing the coupling width provides further performance gain. Recall that all the thresholds are based on the assumption of using miscorrection-free decoding. Hence, the actual performance gain of the proposed codes over the conventional staircase codes can be much larger than the corresponding threshold gain in Table I because larger \((t_1, t_2)\) lead to lower miscorrection probability of iBDD.

| Scheme | Rate | \(\nu\) | \(m\) | \(t_1, t_2\) | \(q\) | \(B\) | \(|\cdot|\) |
|--------|------|-------|-----|-------------|-----|-----|------|
| Proposed | 0.941 | 2 | 11 | 748 | (4, 4) | 1 | 559504 | 5.240x10^{-4} |
| Proposed | 0.941 | 2 | 11 | 936 | (5, 5) | 2 | 436178 | 5.281x10^{-4} |
| Sec. IV-A | 0.951 | 4 | 11 | 1022 | (4, 5) | 2 | 432324 | 5.334x10^{-4} |
| Sec. IV-A | 0.951 | 4 | 11 | 1022 | (5, 5) | 2 | 432324 | 5.334x10^{-4} |

| Proposed | 0.917 | 2 | 10 | 360 | (3, 3) | 1 | 129620 | 7.029x10^{-4} |
| Proposed | 0.917 | 2 | 10 | 450 | (4, 4) | 2 | 175200 | 8.767x10^{-4} |
| Proposed | 0.917 | 2 | 10 | 450 | (4, 4) | 2 | 175200 | 8.767x10^{-4} |
| Proposed | 0.867 | 2 | 8 | 128 | (2, 2) | 1 | 16384 | 4.102x10^{-2} |
| Proposed | 0.867 | 2 | 9 | 216 | (4, 4) | 2 | 17872 | 4.295x10^{-2} |
| Proposed | 0.867 | 2 | 9 | 216 | (4, 4) | 2 | 17872 | 4.295x10^{-2} |
| Proposed | 0.833 | 3 | 9 | 112 | (2, 2) | 1 | 12996 | 3.146x10^{-2} |
| Proposed | 0.833 | 3 | 9 | 244 | (4, 4) | 2 | 14884 | 1.815x10^{-2} |

IV. STALL PATTERN ANALYSIS

The error floor performance of the class of staircase codes is affected by stall patterns [7] Def. 1. To determine the BER due to stall patterns, we consider a fixed code block \(B_i\) and the error bits of stall patterns including positions in \(B_i\) and possibly additional positions in \(B_{i+1}, \ldots, B_{i+w-1}\). The BER of the error floor is dominated by the occurrence probability of the stall patterns with the smallest size [7], [13]. [23]. Consider a BSC with crossover probability \(p\) and under miscorrection-free iBDD. The BER can be approximated by using the union bound technique \(\text{BER}_{\text{floor}} \approx 2^{m_{\text{min}}/2} m_{\text{min}}/\text{size of \(B_i\)}\)

following [7] Sec. VI, [2] Eq. (7.91)], where \(m_{\text{min}}\) is the multiplicity of minimum stall patterns, and \(\text{size of \(B_i\)}\) is the number of error bits of a minimum stall pattern.
In what follows, we present the main results for $s_{\text{min}}$ to gain some insights into the error floor and justify the choice of code parameters. Due to space limitations, we omit the proof and the analysis of $A_{\text{min}}$. For more details, we refer the interested reader to [29].

**Theorem 1.** Consider a SR-staircase codes with parameters $(t_1, t_2)$, $(q_1, q_2)$, and $w = 2$. The exact number of the error bits of the minimum stall pattern is

$$s_{\text{min}} = \min \left\{ \max \left\{ \frac{t_2 + 1}{q_1}, \frac{t_1 + 1}{q_1}, \frac{t_2 + 1}{q_2}, \frac{t_1 + 1}{q_2} \right\}, \max \left\{ \frac{t_1 + 1}{q_2}, \frac{t_2 + 1}{q_1}, \frac{t_2 + 1}{q_2}, \frac{t_1 + 1}{q_1} \right\} \right\}. \quad (10)$$

Based on Theorem 1, it is desirable to have $\max\{q_1, q_2\} \leq \min\{t_1, t_2\}$ when $w = 2$ to ensure that any minimum stall pattern will not become a one-dimensional vector whose $s_{\text{min}}$ becomes very small. Although the size of a minimum stall pattern for SR-staircase codes is smaller than that for the conventional staircase codes when both codes are with the same $(t_1, t_2)$, the proposed codes can still achieve a better error floor due to much smaller multiplicity [arxiv to be uploaded] and the use of BCH component codes with larger $(t_1, t_2)$.

For a large coupling width, we need to set $m_1 = m_2 \triangleq m$ and $q_1 = q_2 \triangleq q$ according to Sec. II-A2. In the interest of space, we consider $w \geq q + 1$ in the subsequent analysis. Unlike for $w = 2$, obtaining the exact $s_{\text{min}}$ for $w > 2$ is difficult. Instead, we find the lower bound on $s_{\text{min}}$, which serves as the upper bound on the BER of the error floor.

**Theorem 2.** Consider a SR-staircase code with parameters $(t_1, t_2)$, $m_1 = m_2 \triangleq m$, $q_1 = q_2 \triangleq q$, and $w \geq q + 1$. The size of the minimum stall pattern satisfies

$$s_{\text{min}} \geq \frac{(\min\{t_1, t_2\} + 1)(\min\{t_1, t_2\} + 2)}{2}. \quad (11)$$

Notice that all of our designs in Table I satisfy $|t_1 - t_2| \in \{0, 1\}$ because these designs achieve a better threshold than those with $|t_1 - t_2| > 1$. Under this condition, the lower bound of $s_{\text{min}}$ for $w \geq q + 1$ in Theorem 2 is larger than the exact $s_{\text{min}}$ for $w = 2$, $q_1 \geq 2$ and $q_2 \geq 2$ in Theorem 1. Hence, the error floor can be improved by increasing $w$.

**Lemma 1.** Consider the SR-staircase code in Theorem 2 with $w \geq q + 1$. If $(q, w, t_1, t_2)$ further satisfy one of the following conditions: 1) $\min\{t_1, t_2\} \geq q$; 2) $\min\{t_1, t_2\} + 1 \leq q$ and $w \leq (1 + \min\{t_1, t_2\})/2$, then $s_{\text{min}}$ is strictly larger than the lower bound in (11).

Lemma 1 shows that if both $q$ and $w$ are not too large, the size of the minimum stall pattern can become larger. Hence, a proper choice of $(q, w, t_1, t_2)$ would lead to a better trade-off between threshold and error floor for SR-staircase codes.

**V. Numerical Results**

We evaluate the performance of SR-staircase codes over the additive white Gaussian noise (AWGN) channel. Note that all BCH component codes used in our designs do not have any extended parity bits.

We first use simulation results to validate our theoretical analysis by assuming miscorrection-free iBDD. We construct three SR-staircase codes with parameters $(m, \nu, t, q, w) = (126, 8, 2, 2, 2)$, $(126, 8, 2, 2, 3)$, and $(441, 9, 3, 2)$, respectively. The decoding window size is $W = 7$. The simulated BER, decoding threshold (converted from the BSC threshold) and the estimated error floor BER$_{\text{floor}}$ are shown in Fig. 2. For the proposed codes with $w = 2$, their simulated error floor BER matches closely to BER$_{\text{floor}}$ based on Theorem 1. However, the BER$_{\text{floor}}$ for the code with $w = 3$ can only be estimated based on Theorem 2. Since the code parameters $(t, q, w) = (2, 2, 3)$ satisfies the conditions in Lemma 1 the actual error floor of the code with $w = 3$ is lower than the BER$_{\text{floor}}$. Observe that the simulated waterfall performance for all the codes is in agreement with the derived decoding threshold (the threshold curves for the codes with $t = 2$ and $w \in \{2, 3\}$ are overlapped). Therefore, both DE and error floor analysis can be used to effectively predict the simulated performance if the probability of miscorrection is low, which is the case in our subsequent design with large $(t_1, t_2)$.

Next, we compare the designed SR-staircase codes with the conventional staircase codes. For SR-staircase codes (labeled as “SR-SC”), we consider two designs from Table I whose parameters are $(m, \nu, t, q, w) = (876, 11, 5, 3, 2)$, and $(m, \nu, t, q, w) = (964, 11, 6, 5, 4, 5)$, respectively. We also consider two benchmark conventional staircase codes, where the first one (labeled as “SC1”) has parameters $(m, \nu, t) = (510, 10, 3)$ and two parity bits extended following [7] Sec. IV-C while the second one (labeled as “SC2”) has parameters $(m, \nu, t) = (478, 10, 3)$ and no extended parity bits. All the codes have rate 0.937 and comparable code block size as shown in Table I. The decoding window size is $W = 9$. The error performance under iBDD (solid lines), miscorrection-free iBDD (dash lines, labeled as “MF”), and the estimated error floor BER$_{\text{floor}}$ are shown in Fig. 3 (the BER$_{\text{floor}}$ of the
SR-staircase code with $w = 5$ is not shown in the figure as it is in the order of $10^{-33}$. Observe that SC2 under iBDD has the worst performance due to the highest probability of miscorrection. Even though SC1 uses two additional parity bits to reduce miscorrection probability, it still has a noticeable gap to its miscorrection-free performance. In contrast, all the proposed codes operate close to their miscorrection-free performance and outperform the conventional staircase codes in terms of better waterfall and error floor performance. Most notably, the SR-staircase code with $w = 5$ has the best performance among all the codes and achieves slightly better waterfall performance with iBDD than the conventional staircase code with miscorrection-free iBDD.

VI. CONCLUDING REMARKS

We proposed SR-staircase codes, which are motivated and derived from the conventional staircase codes. The most appealing feature of the proposed codes is that one can employ stronger BCH component codes to construct a SR-staircase code to achieve better decoding threshold and error floor while having the same rate and similar block size compared to the conventional staircase code. The superior performance of the proposed codes over the conventional staircase codes was demonstrated via theoretical analysis and simulation.

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