MoS₂ Nanoribbon Transistors: Transition from Depletion-mode to Enhancement-mode by Channel Width Trimming

Han Liu, Jiangjiang Gu, Student Member, IEEE, and Peide D. Ye, Senior Member, IEEE

Abstract - We study the channel width scaling of back-gated MoS₂ metal-oxide-semiconductor field-effect transistors (MOSFETs) from 2 μm down to 60 nm. We reveal that the channel conductance scales linearly with channel width, indicating no evident edge damage for MoS₂ nanoribbons with widths down to 60 nm as defined by plasma dry etching. However, these transistors show a strong positive threshold voltage (V_T) shift with narrow channel widths of less than 200 nm. Our results also show that transistors with thinner channel thicknesses have larger V_T shifts associated with width scaling. Devices fabricated on a 6 nm thick MoS₂ crystal underwent the transition from depletion-mode to enhancement-mode.

Index Terms—MoS₂ nanoribbon, width scaling, threshold voltage shift

I. INTRODUCTION

THE triumph of aggressive scaling of silicon based integrated circuits has dramatically changed our lifestyle in the past couple of decades. However, as the scaling of silicon approaches its physical limit, efforts in finding alternative channel materials have been made for the extension of the Moore’s Law. Of these materials, Ge and III-V materials are among the most promising candidates because of their high carrier mobilities. They have been widely studied for logic applications in the past years [1-4]. Although graphene, a single layer of carbon atoms having superior carrier mobilities of up to 200,000 cm²/V·s, has been recognized as another material candidate, its gapless nature limits its further application in logic devices [5]. Nevertheless, the discovery of graphene has spurred research of other two-dimensional (2D) layered structures, including boron nitride, topological insulators (Bi₂Te₃, Bi₂Se₃, etc.), and transitional metal dichalcogenides (TMDs) [6-10]. TMDs, e.g. MoS₂, have enjoyed several advantages in device applications because they have large bandgaps (usually >1 eV), satisfactory electron mobilities of up to several hundred, good thermal stability, and can be used to form ultrathin body transistors with atomic layers, which make them a desirable channel material with superior immunity to short channel effects [11-13]. The MoS₂ devices are mostly n-type transistors in experimental observations, which might be attributed to the stoichiometric composition [10,15,16]. Also, its charge neutrality level is in the vicinity of the conduction band (E_C), thus n-type contacts can be more easily made for MoS₂ transistors and the transistors behave as depletion-mode n-channel MOSFETs with large negative threshold voltages [14]. The 2D nature of MoS₂ (as well as other layered materials) makes it difficult to realize channel doping as a way to achieve desirable positive V_T or enhancement-mode operation for various desirable circuitry configurations. Therefore, making an enhancement-mode MoS₂ MOSFET is quite challenging.

II. EXPERIMENTS

In this letter, we study the width scaling of MoS₂ transistors by forming nanoribbon channels, and show that the V_T of MoS₂ transistors can be modulated to be both positive and negative through appropriate width selection. The fabrication process of sets of MoS₂ transistors is shown in Figure 1(a), as described below. MoS₂ flakes were mechanically exfoliated from bulk ingot (SPI Supplies) and then transferred to a heavily p-doped silicon substrate (0.01-0.02 Ω·cm) with a 300 nm SiO₂ capping layer. The silicon substrate served as a global back gate, while the 300 nm SiO₂ served as the gate dielectric. After the flake transfer, we used electron beam lithography to pattern the flake, followed by plasma dry etching (BCl₃: 15 sccm, Ar: 60 sccm, Pressure: 0.6 Pa, RF source power: 100W, RF Bias Power: 50W, time: 5 min) to remove the excess parts of the flakes, leaving connected rectangles with a fixed length (2 μm) but various widths to be used as device channels. Finally, contacts were defined by electron beam lithography, followed by a 50 nm Au metallization by electron beam deposition. The
bias. This increased gate leakage could be ascribed as more nanoribbons, as well as an increased leakage current at negative gate biases. The transfer curves are noisy, due to fewer conduction modes in the device is shown in Figure 2(c). Compared to Figure 2(a), the extrinsic field-effect mobility of this device is 21.8 cm²/V·s, which can be further improved by high-k dielectric passivation (Figure 1(c) inset). Smooth edges without obvious damage by dry etching was observed at the MoS2 nanoribbons.

Over-etching of the MoS2, removal of excess MoS2 crystals, created a rectangular step in the SiO2 capped substrate surrounding the flake, and also created SiO2 sidewalls at the edges of the MoS2 channels (Figure 1(c) inset). Smooth edges without obvious damage by dry etching was observed at the MoS2 nanoribbons.

Figure 2(a-d) show the transfer and output characteristics of the devices with 2 μm and 60 nm widths, selected from one of three sets of devices. These devices were fabricated using one of the 6 nm thick crystals (D1). Figure 2(a) shows well-behaved transfer curves from the 2 μm wide transistor. The current on/off ratio is approximately 10², as the ultrathin MoS2 crystal can be easily depleted at negative gate biases. The extrinsic field-effect mobility of this device is 21.8 cm²/V·s, which can be further improved by high-k dielectric passivation [10,15]. The transfer curve of the 60 nm wide nanoribbon device is shown in Figure 2(c). Compared to Figure 2(a), the transfer curves are noisy, due to fewer conduction modes in the nanoribbons, as well as an increased leakage current at negative bias. This increased gate leakage could be ascribed as more defects are induced in the vicinity of etching windows in the SiO2. We also observe a larger subthreshold swing (SS). The SS for the 2 μm wide device is around 2 V/dec, however for the 60 nm wide device, this value increases to almost 10 V/dec. The SS value of the 2 μm wide device indicates a reasonably good interface (interface trap density $D_{it} \sim 2.3 \times 10^{12}$/cm²·eV) between the MoS2 crystal and SiO2 dielectric. If we replace the 300 nm SiO2 layer with 5 nm of Al2O3, while assuming that $D_{it}$ remains unchanged, the SS would be significantly reduced to ~75 mV/dec by simply applying $SS=kT/q(1/C_{ox}/C_{it})$, where $k$ is the Boltzmann constant, $T$ is the temperature and $C_{ox}$ and $C_{it}$ are capacitances modeling the oxide and interface traps, respectively. The differences in SS for the two devices are expected because edge roughness and defects play more important roles in nanoribbon transistors. We also observe a large difference in threshold voltages for these two devices. At a 2 V drain voltage with zero gate bias, the drain current for the 2 μm wide device is 13.0 mA/mm, showing typical depletion-mode operation. However, for the narrower device, the drain current is near zero with zero gate bias, indicating an obvious $V_T$ shift to the positive side, signaling enhancement-mode operation. At the same $V_{ds}=2V$ and $V_{gs}=50V$, we achieve the highest drain current density to be 39.4 mA/mm for the 2 μm wide device and 16.4 mA/mm for the 60 nm wide device. This difference in normalized drain current suggests that $V_T$ is different for these two devices, assuming that the current scales linearly with the channel width, which is verified below.

In order to confirm that the current scales linearly with various channel width, we plot the total conductance (1 over resistance) versus channel width for all three sets of devices, as shown in Figure 3(a). The on-resistance ($R_{on}$) of the transistor has contributions from the contact resistance and channel resistance. Since the contact area and width for all transistors scales with channel width, the contact resistance should scale linearly with the channel width. The same is true for the channel resistance. After determining $V_T$ via linear extrapolation from transfer characteristics, $R_{on}$ is extracted at the same reference voltage point $V_{gs}=V_T+26V$. Our result shows that the $R_{on}$ or total conductance scales linearly with channel width. As expected, MoS2 acts as a conventional semiconductor, in great contrast to 3D topological insulators such as Bi2Te3 or Bi2Se3, where edge or surface conductance could be enhanced or dominate [17]. The width dependent conductance is about 6-7 μS/μm for the two 6 nm thick devices (D1 and D2) and 5 μS/μm for the 11 nm device (D3). We are not clear about why the thicker device has a lower conductance and this result needs further investigation. As shown in the inset of Figure 3(a), with much reduced channel widths, the extracted conductance becomes noisier as fewer conduction modes are available in the nanoribbons. But, the data points still fall along the scaling trend.

Lastly, we studied the $V_T$ shift of all devices associated with the channel width. The $V_T$ is extracted from the linear extrapolation method at a low drain voltage. $V_T$ is calculated by $V_T = V_{GSi} – V_{ds}/2$, where $V_{GSi}$ is the intercept gate voltage, and $V_{ds}$ is the drain voltage [18]. Threshold voltages for all three sets of devices are plotted in Figure 3(b). Similar trends can be observed for all sets of devices. The $V_T$ remains constant for transistors with wider channel width (W>500 nm). As the width of the channel is narrowed down to 200 nm, we start to observe the $V_T$ shift to positive values. Apparently, transistors with thinner bodies (D1 and D2) are more likely to be influence by this effect. For one of the 6 nm thick set of transistors (D2), the threshold voltage ultimately shifts from -20V to 30V, indicating...
a clear transition from being a depletion-mode transistor to being an enhancement-mode operation just by trimming down the channel width. The geometry of these nanoribbon transistors with channel width less than 100 nm has a similar structure to Si FinFETs, if we ignore that the MoS2 channel is modulated only from the back gate. Similar trends of V_T shift have also been observed in Si FinFETs as well as InGaAs nanowire transistors. This narrow channel effect was ascribed to the lateral expansion of depletion layer due to fringing field effect or quantum confinement in device channels [19-21]. However, the channel widths are strictly defined in our MoS2 transistors thus they cannot have a lateral expansion in depletion layer. Also, they are much wider than those of these Si FinFETs and InGaAs nanowire MOSFETs. We believe that our V_T shift is due to edge deformation, similar to what has been observed in majority carrier GaN nanoribbon devices [22]. The edge deformation could be induced by either electric fields or ambient molecules (e.g. H2O) adsorbed at the MoS2 surface. Given our previous surface study of atomic layer deposition (ALD) growth on 2D crystals, these polarized molecules can be strongly adsorbed at MoS2 surface and even persist at 300-400 °C [23]. As expected, the V_T of the devices fabricated on the thicker crystal (D3) show relatively minor shifts compared to the devices with thinner flakes, as shown in the same figure. The observation of V_T shifts for MoS2 transistors with width scaling is important. The 2D nature of MoS2 and other TMD based transistors makes them difficult to engineer the channel through doping. This demonstrated approach, using the width to achieve V_T adjustments on the same starting channel material in order to realize both enhancement-mode and depletion-mode operation, is a simple and favorable method for circuit designs such as to realize an enhancement-mode/depletion-mode based inverter.

III. CONCLUSION

In summary, we have studied effect of the width scaling on MoS2 transistors. We demonstrated that the channel conductance scales linearly for sets of devices with various channel widths down to 60nm. We also revealed that the threshold voltage has a significant shift from negative to the positive for transistors with channel widths of less than 200 nm. As a result, these transistors show a clear transition from depletion-mode to enhancement-mode operation simply by channel width trimming. Our result provides a new approach for threshold voltage engineering and is favorable for circuit applications based on 2D crystal nanomaterials.

REFERENCES

[1] R. Pillarisetty, “Academic and industry progress in germanium nanodevices”, Nature, vol. 479, pp. 324-328, 2011; references therein.
[2] Y. Xuan, Y. Q. Wu, and P. D. Ye, “High-Performance Inversion-Type Enhancement-Mode InGaAs MOSFET With Maximum Drain Current Exceeding 1 A/mm”, IEEE Electron Devices Letters, vol. 29, pp. 294-296, 2008.
[3] H. Ko, K. Takei, R. Kapadia, S. Chung, H. Fang, P. W. Leu, K. Ganapathsi, E. Plis, H. S. Kim, S.-Y. Chen, M. Madsen, A. C. Ford, Y.-L. Chueh, S. Krishna, S. Salahuddin and A. Javey, “Ultrathin compound semiconductor on insulator layers for high performance nanoscale transistors”, Nature, vol. 468, pp. 286-289, 2010.
[4] M. Xu, R. Wang, and P. D. Ye, “GaSb Inversion-Mode PMOSFETs With Atomic-Layer-Deposited Al2O3 as Gate Dielectric”, IEEE Electron Devices Letters, vol. 32, pp. 883-885, 2011.
[5] Y. Zhang, J. W. Tan, H. L. Stormer, P. Kim, “Experimental observation of the quantum Hall effect and Berry’s phase in graphene”, Nature, vol. 438, pp. 201-204, 2005.
[6] K. S. Novoselov, D. Jiang, F. Schedin, T. J. Booth, V. V. Khotkevich, S. V. Morozov, and A. K. Geim, “Two-dimensional atomic crystals”, Proc. Natl Acad. Sci. USA, vol. 102, pp. 10451-12453, 2005.
[7] H. Zhang, C. X. Liu, X. X. Qi, X. Dai, Z. Fang, and S. C. Zhang, “Topological insulators in Bi2Se3, Bi2Te3 and Sb2Te3: with a single Dirac cone on the surface”, Nature Physics, vol. 5, pp. 438-442, 2009.
[8] H. Liu and P. D. Ye, “Atomic-layer-deposited Al2O3 on Bi2Te3 for topological insulator field-effect transistors”, Appl. Phys. Lett., vol. 99, pp. 252108, 2011.
[9] V. Podzorov, M. E. Gershenson, K. Cloc, R. Zeis, and E. Bucher, “High-mobility-field-effect transistors based on transition metal dichalcogenides”, Appl. Phys. Lett., vol.84, 3301, 2004.
[10] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti and A. Kis, “Single-layer MoS2 transistors”, Nature Nanotechnology, vol.6, pp. 147-150, 2011.
[11] K. F. Mak, C. Lee, J. Hone, J. Shan, and T. F. Heinz, “Atomically Thin MoS2: A New Direct-Gap Semiconductor”, Phys. Rev. Lett., vol. 105, pp.136805, 2010.
[12] Y. Yoon, K. Ganapathsi, and S. Salahuddin, “How Good Can Monolayer MoS2 Transistors Be?”, Nano Lett., vol. 11, pp. 3768-3773, 2011.
[13] H. Liu, A. T. Neal and P. D. Ye, “Channel Length Scaling of MoS2 MOSFETs”, submitted to ACS Nano, 2012.
[14] B. L. Abrams and J. P. Wilcoxon, “Nanofinectors for photooxidation,” Crit. Rev. Solid State Mater. Sci., vol. 30, pp. 153-182, 2005.
[15] L. Liu and P. D. Ye, “MoS2 Dual-Gate MOSFET with Atomic Layer Deposited Al2O3 as Top-Gate Dielectric”, IEEE Electron Devices Letters, vol. 33, pp. 546-548, 2012.
[16] Z. Yin, H. Li, H. Li, L. Jiang, Y. Shi, Y. Sun, G. Lu, Q. Zhang, X. Chen, H. Zhang, “Single-Layer MoS2 Phototransistors”, ACS Nano, vol. 6, pp. 74-80, 2012.
[17] J. G. Analytis, R. D. McDonald, S. C. Riggs, J.-H. Chu, G. S. Boebinger and I. R. Fisher, “Two-dimensional surface state in the quantum limit of a topological insulator”, Nature Physics, vol. 6, pp. 960-964, 2010.
[18] D. K. Schroder, “Semiconductor Material and Device Characterization”, 3rd Edition, Wiley, New York (2006).
[19] K. E. Kroell and K. G. Ackermann, “Threshold Voltage of Narrow Channel Field Effect Transistors”, Solid-State Electronics, vol. 19, pp. 77-81, 1976.
[20] H. Lee, L.-E. Yu, S.-W. Ryu, J.-W. Han, K. Jeon, D. Y. Jung, K.-H. Kim, J. Lee, J.-H. Kim, S. C. Jeon, G. S. Lee, J. S. Oh, Y. C. Park, W. H. Bae, H. M. Lee, J. M. Yang, J. J. Yoo, S. J. Kim, Y.-K. Choi, “Sub-5 nm all around gate FinFET for ultimate scaling,” in VLSI Symp. Tech. Dig., 2006, pp. 58-59.
[21] J. J. Gu, Y.Q. Liu, Y.Q. Wu, R. Colby, R.G. Gordon, and P.D. Ye, “First Experimental Demonstration of Gate-all-around III-V MOSFETs by Top-down Approach”, IEDM Tech. Dig. pp. 769-772, 2011.
[22] B. Lu, E. Miotoli and T. Palacios, “Tri-Gate Normally-off GaN Power MISFET”, IEEE Electron Device Letters, vol. 33, pp. 360-362, 2012.
[23] H. Liu, K. Xu, X. J. Zhang and P. D. Ye, “The Integration of High-k dielectric on Two-Dimensional Crystals by Atomic Layer Deposition”, Appl. Phys. Lett., vol.100, 152115, 2012.