Robust Microfabrication of Highly Parallelized Three-Dimensional Microfluidics on Silicon

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We present a new, robust three dimensional microfabrication method for highly parallel microfluidics, to improve the throughput of on-chip material synthesis by allowing parallel and simultaneous operation of many replicate devices on a single chip. Recently, parallelized microfluidic chips fabricated in Silicon and glass have been developed to increase the throughput of microfluidic materials synthesis to an industrially relevant scale. These parallelized microfluidic chips require large arrays (>10,000) of Through Silicon Vias (TSVs) to deliver fluid from delivery channels to the parallelized devices. Ideally, these TSVs should have a small footprint to allow a high density of features to be packed into a single chip, have channels on both sides of the wafer, and at the same time minimize debris generation and wafer warping to enable permanent bonding of the device to glass. Because of these requirements and challenges, previous approaches cannot be easily applied to produce three dimensional microfluidic chips with a large array of TSVs. To address these issues, in this paper we report a fabrication strategy for the robust fabrication of three-dimensional Silicon microfluidic chips consisting of a dense array of TSVs, designed specifically for highly parallelized microfluidics. In particular, we have developed a two-layer TSV design that allows small diameter vias (d < 20 µm) without sacrificing the mechanical stability of the chip and a patterned SiO2 etch-stop layer to replace the use of carrier wafers in Deep Reactive Ion Etching (DRIE). Our microfabrication strategy allows >50,000 (d = 15 µm) TSVs to be fabricated on a single 4” wafer, using only conventional semiconductor fabrication equipment, with 100% yield (M = 16 chips) compared to 30% using previous approaches. We demonstrated the utility of these fabrication strategies by developing a chip that incorporates 20,160 flow focusing droplet generators onto a single 4” Silicon wafer, representing a 100% increase in the total number of droplet generators than previously reported. To demonstrate the utility of this chip for generating pharmaceutical microparticle formulations, we generated 5–9 µm polycaprolactone particles with a CV < 5% at a rate as high as 60 g/hr (>1 trillion particles/hour).

In many sub-fields of microfluidics, parallelization - the placing of many replicate devices that operate in parallel onto a single chip - has been a successful strategy to increase the throughput of otherwise slow processes. Parallelization has been used with particular success to increase the production rate of microfluidic generated materials to the scale required for economic commercial use, including nanomaterials, microparticles, and a variety of single and multiple emulsions. In particular, microfluidic generated micro and nanoparticles have shown excellent pharmacokinetic properties, superior control over drug release rates, long term stable formulations and higher drug encapsulation efficiencies compared to conventional approaches, such as ball milling. This approach has also been applied successfully to increase the throughput of micro-sensors to detect cells and molecular markers and to perform digital droplet based assays. To deliver fluid to and collect fluid from many parallel microdevices on a single chip, three-dimensional microfabrication strategies have been used to incorporate a layer of delivery channels and vias that connect these delivery channels to microfluidic devices in a layer below. Three-dimensional fabrication strategies have been developed for both polymer (PDMS, perfluoropolyether-polyethylene glycol, etc.) and for Silicon based devices. Using these fabrication

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methods, architectures have been developed that make it possible to operate many microfluidic droplet generators in parallel \cite{12,23}. Although Silicon devices are significantly more expensive than polymer devices, they have several key advantages that motivate their use, in particular for the generation of micro- and nanomaterials. Importantly, Silicon devices can operate at high pressure $P_{\text{max}} > 1000$ PSI and high temperature $T_{\text{max}} > 500^\circ C$, use solvents useful for material synthesis but that are incompatible with polymer devices, and can be fabricated with significantly less variance in device dimensions than soft-lithography based devices, resulting in more monodispersed materials \cite{6,28}.

The microfabrication of Silicon to create highly parallelized microfluidic devices has several fabrication challenges, which have not been adequately addressed in prior studies \cite{20} and which must be addressed to produce high performing chips with high yield. These parallelized microfluidic devices incorporate arrays (>10,000) of Through Silicon Vias (TSVs) that connect fluid from delivery channels in one layer to a layer of parallelized devices below. Conventional TSV approaches cannot be easily applied to these architectures 1. because of the small footprint of these TSVs ($d < 20 \mu m$), necessary to allow many microfluidic devices to be packed onto a single wafer, 2. because of the requirement of these chips for microfabricated features on both sides of the wafer, and 3. because of the stringent requirement for minimal debris and wafer warping such that the device can be permanently bonded to glass. We describe a set of microfabrication strategies specifically for parallelized microfluidics in Silicon and glass. By incorporating the microfabrication strategies described in this paper, we achieved a device fabrication yield of 100% ($M = 16$ wafers) using conventional semiconductor fabrication modalities compared to 30% using previous approaches \cite{20}. The two key innovations in this paper to address these issues, and which make use of conventional MEMS fabrication modalities, are: 1. We have developed a technique to through-etch the Si to produce vias that are compatible with the specific requirements of parallelized microfluidics, i.e. the requirement for DRIE features on both sides of the wafer and the requirement for minimal debris and wafer warping. To accomplish this goal, we replace the conventionally used carrier wafer with a stress relieved SiO$_2$ membrane as an etch-stop for DRIE. 2. We have implemented trenches in our delivery channel, which allow the tradeoff between the diameter of the vias and the mechanical stability of the wafer to be eliminated, allowing the fabrication of small footprint devices to allow many replicate devices to be incorporated onto a single chip.

To demonstrate the utility of these fabrication strategies, we have developed a Very Large Scale Droplet Integration (VLSDI 2.0) chip that incorporates 20,160 flow focusing droplet generators onto a single 4" Silicon wafer, representing a 100% increase in the total number of droplet generators on a single chip than has previously been reported \cite{12,14-16,20}. Using these generators that are connected in a ladder geometry with only one set of inlets and outlets, we generated 1 trillion monodispersed droplets / hour with a CV $< 5\%$ for diameters ranging from 21–28$\mu m$. We have also generated monodispersed polycaprolactone (PCL) solid microparticles ($d = 5.3–9.0 \mu m$) with a coefficient of variation CV $< 5\%$ at a production rate as high as 60 grams/hr. We believe our fabrication strategy can be widely used to enhance the reliability of microfabrication of three-dimensional Silicon and glass microfluidic chips for a variety of applications.

Results

The VLSDI 2.0 chip. Our 3D fabricated parallelized chips is built using a 4” diameter 500$\mu m$ thick double side polished Si wafer (University Wafers, Part 1095). The chip consists of 370$\mu m$ height delivery channels on one side of the wafer and includes a trench that has a depth of 75$\mu m$. On the other side of the wafer, there are flow focusing droplet generators with a height $h = 24$ $\mu m$. Connecting these two layers of microfluidics are vias with a diameter $d = 15$ $\mu m$ and a height $h = 85$ $\mu m$. Both sides of the wafer are permanently bonded with Borofloat 33 glass (University wafers, Part 517) using anodic bonding to encapsulate the channels (Fig. 1a). In this work, we have increased the total number of droplet generators that can be incorporated onto a single wafer by reducing the size of the vias, resulting in a footprint (80$\mu m \times 1.6$ mm) for each droplet generator that is 50% smaller than that reported in our previous work (Fig. 1b,c) \cite{20}.

Microfabrication challenges. The microfabrication of VLSDI chips in Silicon is made particularly challenging because of the Through Silicon Vias (TSVs) required to create the connections between the delivery channels and the droplet generators \cite{24}. Although there is a well developed literature on TSVs for MEMS applications and for CMOS chips \cite{24-29}, VLSDI chips have several unique requirements that warrant special consideration. Unlike many through-etching applications, parallelized microfluidic chips require microfabricated patterns on both sides of the chip, making many existing through-etching techniques not easy to implement, i.e. the use of mechanical polishing to expose TSVs \cite{30}. Moreover, parallelized microfluidic chips must be anodically bonded with glass to encapsulate the microfluidic devices, making the fabrication process sensitive to wafer warping and to contamination from debris. Finally, from a design perspective, in VLSDI chips it is advantageous to pack as many parallelized chips onto a wafer as possible. Therefore it is important that the vias have the smallest possible footprint. This requirement makes techniques such as anisotropic wet etching (e.g. potassium hydroxide KOH, tetramethylammonium hydroxide TMAH) unfavorable, due to their angled sidewalls \cite{31}. Finally, VLSDI chips often require high aspect ratio features (height/width $\sim 5$), motivating the use of Deep Reactive Ion Etch (DRIE) for the etching of the microfluidic channels.

Etching of through silicon vias (TSVs). Through-etching using DRIE is challenging because in a typical DRIE Bosch process the backside of the wafer is kept at a positive pressure to keep the wafer at a low temperature using He gas, and the frontside is maintained under a vacuum necessary for reactive ion etching. (Fig. SI 7) When a TSV punches through a Silicon wafer it connects the positive pressure and vacuum, halting the etching process. The etch quality, uniformity across the wafer, and photosist selectivity depends on the wafer temperature, and as such the He cooling is necessary. This problem is particularly pertinent for parallelized microfluidics, because of the variety of the diameter of TSVs used. Larger diameter TSVs etch faster, and therefore break through the...
Silicon before the smaller ones (Fig. 8). Conventionally, chips are often bonded to a carrier wafer using a temporary adhesive like crystal bond to facilitate TSV etching (Fig. 2a). However, it can be challenging to remove all air pockets between the two wafers, which leads to wafer breakage in the DRIE’s vacuum (Fig. 2b). In addition, even if the wafers do not break, the presence of small air pockets between the carrier wafer and the VLSDI can lead to nonuniform etching on the wafer. (Fig. 2c). The yield of our VLSDI chip when we used a carrier wafer was only 30% (Fig. 2d). By combining our two innovations, i.e our trench technique to achieve small vias and our stress relieved oxide backing layer, we have achieved a yield of 100% ($N = 20,160$ devices per chip, $M = 16$ chips).

In our VLSDI 2.0 approach, instead of using a carrier wafer we instead use a Chemical Vapor Deposition (CVD) grown oxide layer as an etch stop (Fig. 2e). A 6 µm thick layer of CVD grown SiO$_2$ is deposited on to the delivery channels side of the wafer before the vias are etched. The use of an SiO$_2$ back-layer obviates the need for the temporary adhesives and associated problems with uniformity of temperature across the wafer during processing. To avoid mechanical stress on the wafer from the 6 µm thick SiO$_2$ layer, which can lead to wrinkling of the SiO$_2$ membrane and breaking of the Si wafer (Fig. 2f), the SiO$_2$ layer is lithographically patterned to relieve the mechanical stress.

There is an additional challenge in this fabrication that arises due to the finite aspect ratio of the vias achievable using DRIE. In a DRIE Bosch process, TSVs can be etched with aspect ratios as high as width: height = 1:10. To ensure uniform etching across the wafer, and to ensure a high yield, we use a more conservative value 1:5. Therefore, to achieve a $d = 15$ µm TSV, the etch depth must be $h < 75$ µm. However, if we etched the delivery channels to within 75 µm of the backside of the wafer, the chips became mechanically unstable and would often break during sample handling (Fig. 2g,h).

To overcome this challenge, in this work we incorporate a two-layer design strategy to allow small diameter vias ($d = 15$ µm) to be etched without sacrificing the mechanical stability of the VLSDI 2.0 chip (Fig. 2i). This trench approach results in mechanically stable membranes that act as effective etch stops and maintain the seal between the He cooling and the DRIE’s vacuum, leading to uniform and reproducible TSV etching over the entire 4” wafer (Fig. 2j–l). To achieve this goal, we etched the via in two steps. First, we etched a trench in the delivery channel with a height $h = 75$ µm and a width $w = 110$ µm. Subsequently, the vias are etched within the trench with a height $h = 85$ µm and diameter $d = 15$ µm to connect to the backside layer.

**VLSDI 2.0 design for high throughput and low droplet polydispersity.** The design principals and ladder geometry of our VLSDI chip have been described in detail previously. Briefly, the main microfluidic design goals of our ultra-large-scale parallelization device is, 1. to evenly distribute both dispersed and continuous phase fluids to each of densely packed $N$ microfluidic droplet generators, 2. to maximize the number of microfluidic droplet generators $N$ that can be packed per unit area, and 3. to maximize the generation of uniform droplets from each of these $N$ droplet generators at the highest possible flow rate. These design goals and the physics of multiphase flows provide trade off relationships that guide our ultra large scale parallelization design strategies. By satisfying these design considerations, we have designed a chip that consists of 20,160 microfluidic
droplet generators arranged in a 36 × 560 rectangular array with a total footprint of 6.28 × 4.93 cm², with each generator having a footprint of 80 µm × 1.6 mm.

The flow focusing droplet generators consist of a high aspect ratio flow resistor to ensure even distribution of flow across all 20,160 devices and a flow focusing droplet generator designed to remain in the dripping regime, by reducing the capillary number (Ca) of the continuous phase and the Weber (We) of the dispersed phase at high volumetric flow rates (Fig. 3a–c). The dimensions of the droplet generators are shown in Fig. 3a–g. The width of the flow resistors $w = 8$ µm are less than the height, and thus allow the resistance to have a cubic dependence on the flow resistor’s width $R \propto 1/(hw^3)$, and not the height of the entire droplet generator layer, decoupling each individual device's flow resistance from its maximum flow rate so that droplet break-up remains in the dripping regime.

The delivery channels have dimensions $w = 0.43$ mm, $h = 0.37$ mm, $l = 54$ mm (Fig. 3h–j). The supply channels, which supply fluid to the delivery channels, have dimensions $w = 2.2$ mm, $h = 0.38$ mm, $l = 66$ mm (Fig. 3l–o). The trenches in the delivery channel have a $w = 110$ µm and $h = 75$ µm and the vias $d = 15$ µm and $h = 85$ µm (Fig. 3j,k). The underpasses, which allow the output to cross the supply lines, have the dimensions $w = 3$ mm, $l = 7.8$ mm, and $h = 30$ µm (Fig. 3l,o).

**Droplet generation.** We first evaluated the efficacy of our new fabrication technique, by using the VLSDI 2.0 to generate hexadecane droplets in water (2 wt% Tween 80). We confirmed that at all flow rates droplets are generated in every one of the 20,160 droplet generators (Supplementary Movies S1–S3). We found that our device transitioned from making uniform droplets to polydisperse droplets at a critical flow rate $\phi_{d_{\text{max}}}$ = 5.3 L/hr, resulting in a maximum throughput of 1 trillion droplets/hour (Fig. 4a–f) consistent with previous results. When the device was in the dripping regime, the droplets were highly monodispersed (CV < 5%) and at flow rates where the droplet generator were in the jetting regime, the droplets became highly polydisperse (CV > 5%). We further tested the mass production of oil-in-water emulsion by changing the dispersed phase flow rate over the range of $\phi_d = 1.0$ L/hr (20 PSI) to 5.3 L/hr (90 PSI) and the continuous aqueous phase over the range of $\phi_c = 1.9$ L/hr (22 PSI) to 16.2 L/hr (115 PSI). By doing so, the average droplet size could be controlled over a range of $d = 21–28$
μm (Fig. 5a,b). The droplets were highly monodisperse at all flow rates, with a coefficient of variation CV < 5% (Fig. 5c,d).

**Large-scale manufacturing of polymer microparticles.** To demonstrate the utility of this approach in materials synthesis, we generate polycaprolactone (PCL) solid microparticles as small as \( d_p = 5.3 \mu m \) and as large as 9.0 μm, at a production rate as high as 60 grams/hr, and a CV < 5%. PCL is a biodegradable material that is approved by the United States Food and Drug Administration, and used as an injectable drug delivery system33. Emulsion templates for the solid particles were generated on our chip using a dispersed phase of dichloromethane (DCM) with 4 wt% PCL. The continuous phase was deionized water with 2 wt/vol% of polyvinyl alcohol (PVA) (Fig. 6a, Supplementary Movie S4). These emulsion templates were generated on our chip at high throughput (Fig. 6b), collected, and processed using roto-evaporation and lyophilization. After the DCM was extracted, spherical, highly monodispersed solid PCL polymer particles were observed (Fig. 6c,d). To demonstrate the
VLSDI 2.0’s capability to produce highly monodispersed particles with a determined particle diameter, we generated three particle formulations (Fig. 6e–g). We generated particles with a diameter $d_p = 9.0 \mu m$ (CV = 4.0%), $d_p = 7.6 \mu m$ (CV = 4.3%), and $d_p = 5.3 \mu m$ (CV = 4.6%) (Fig. 6h). These particles were generated using emulsion templates produced using the following flow conditions, respectively, $\phi_c = 2.9 L/hr$, $\phi_d = 0.7 L/hr$ (35 grams/hour PCL), $\phi_c = 1.9 L/hr$, $\phi_d = 0.4 L/hr$ (21 grams/hour PCL), and $\phi_c = 7.7 L/hr$, $\phi_d = 1.2 L/hr$ (60 grams/hour PCL), respectively.

To clean the VLSDI 2.0 chip for repeated use, the device is immediately connected to two 1-gallon pressure vessels. The VLSDI 2.0 chip is flushed sequentially with 1 liter of dichloromethane, acetone, and isopropyl alcohol. The chips are then dried by being flushed with Nitrogen gas.
In summary, we have developed strategies for the robust microfabrication of three-dimensional microchannels in Silicon to create highly parallelized microfluidic devices. We demonstrated the utility of these fabrication strategies by developing a VLSDI 2.0 chip that incorporates 20,160 flow focusing droplet generators onto a single 4" Silicon wafer. Our microfabrication strategy allows >50,000 TSVs to be incorporated on a single 4" wafer, with diameters as small as 15 µm, with a 100% yield. Although we focus on the production of oil in water emulsions in this work, the VLSDI 2.0’s modular design enabled by the incorporation of flow resistors that decouple the design requirements for parallelization and the design of each individual microfluidic device allow for more complex designs to be parallelized for fabrication of solid polymer microparticles, multiple emulsions, microfibers, and nanomaterials.

Etching of TSVs in Silicon has received much attention outside of microfluidics for its applications in three dimensional die stacking, memory stacking, CMOS, and Lab/System on a chip applications. Etching of TSVs in Silicon has been done using either laser machining, wet etching, or DRIE. Laser machining is a serial process and therefore not practical with wafer-scale processes that require >50,000 vias. Wet etching of Silicon using KOH or TMAH is limited because isotropic etches lead to larger footprint devices, because the via diameter and the via depth are coupled. DRIE, which is a parallel process, has become an industry standard to etch vias in Silicon wafers with sharp sidewalls. The strategies detailed in this manuscript can potentially be used in CMOS and MEMS fields, beyond its microfluidics applications.

**Materials and Methods**

**Step-by-step fabrication of microfluidic devices.** Our device has six mask layers (Fig. SI 1–SI 6), including layers for delivery channels (Layer 1), trenches (Layer 2), oxide mechanical stress relief (Layer 3), under-pass channels (Layer 4), through Silicon vias (Layer 5) and droplet generator channels (Layer 6). To fabricate these six layers, we produced six photomasks that are prepared on chrome-coated soda lime glass (AZ1500) using a Heidelberg 66 plus mask writer and a 10 mm write head. After exposure, all are developed in MF 319 developer for 1 minute and cleaned in SRD and then kept at 100 °C on a hotplate for 10 minutes. The fabrication steps are carried out as described below, and are shown schematically in Fig. 7a–g and as electron micrographs in Fig. 7h. For the first layer (Fig. 7a), we first coat the wafer with 12 µm of spray-coated photoresist and a 10 mm write head. After exposure, all are developed in MF 319 developer for 2 minutes and then cleaned in SRD and then kept at 100 °C on a hotplate for 10 minutes.
The wafer is then cleaned again in a spin rinse dryer and etched in DRIE to achieve an etch depth of 370 µm. The etched wafer is subsequently cleaned in acetone, isopropyl alcohol (IPA) and deionized water for 5 minutes each and in nanostrīp for an hour and then cleaned in SRD. For the second layer (Fig. 7b), we first coat the wafer with 8 µm of spray coated photoresist, soft baked at 90 °C for 2 minutes, and exposed with the trench channels (Layer-2) (Fig. SI 2) photomask. After exposure, the wafer is left idle at room temperature for 1 hour for rehydration. The wafer is then developed in MF 319 for 2 minutes and cleaned in SRD and then kept at 100 °C rehydration for 5 minutes. The wafer is cleaned again in SRD and etched in DRIE to a height of \( h = 75 \) µm. The wafer is cleaned and kept in nanostrīp for an hour. The etched wafer is then cleaned in SRD.

For the third layer (Fig. 7c), we first deposit 6 µm of PECVD oxide layer at a rate of 0.3 µm per minute. After deposition of oxide layer, the wafer is cleaned in nanostrīp for an hour. The wafer is coated with 8 µm of spray coated photoresist, soft baked at 90°C for 2 minutes, and exposed with the oxide pattern (Layer-3) (Fig. SI 3) photomask. After exposure, the wafer is left idle at room temperature for 1 hour for rehydration. The wafer is then developed in MF 319 for 2 minutes, cleaned in SRD, and then kept at 115°C for 8 minutes. The wafer is cleaned again in SRD and etched in 25% HF for 1 minute to pattern oxide layers. The wafer is then cleaned and kept in nanostrīp for an hour and cleaned in SRD. For the fourth layer (Fig. 7d), the wafer is flipped. We coat the wafer with 4 µm of spray coated photoresist which is soft baked at 90°C for 2 minutes and subsequently exposed to UV with the underpass channels (Layer 4) (Fig. SI 4) photomask. After exposure, the wafer is left idle at room temperature for 20 minutes for rehydration. The wafer is then developed in MF 319 for 2 minutes, cleaned in SRD and kept at 100°C for 3 minutes. The wafer is subsequently cleaned again in spin rinse dryer and etched in DRIE for an etch depth of 30 µm. The wafer is cleaned in acetone, IPA, water and kept in nanostrīp for an hour and cleaned again in SRD. For the fifth layer (Fig. 7e), we spray coat the wafer with 8 µm of photoresist, soft bake at 90°C for 4 minutes, and exposed with the vias (Layer 5) (Fig. SI 5) photomask. After exposure, the wafer is left at room temperature for 1 hour for rehydration. The wafer is then developed in MF 319 for 2 minutes, cleaned in SRD and kept at 100°C for 5 minutes. The wafer is subsequently cleaned again in spin rinse dryer and etched in DRIE for through Silicon vias. The microfabricated wafer is cleaned and kept in nanostrīp for an hour. For the sixth layer (Fig. 7f), the wafer is coated with a monolayer of hexamethyldisilane (HMDS) in Yes Plus Oven to improve the adhesion of photoresist to the etched Silicon wafer. This step is necessary for the droplet generator layer (Layer 6) (Fig. SI 6), because the

Figure 7. Schematic step by step description and 3D fabrication of VLSDI 2.0 chip in a single 4” Silicon wafer. (a) Fabrication of delivery channels. (b) Fabrication of trenches inside delivery channels. (c) Fabrication of SiO₂ etch-stop layer. (d) Fabrication of underpass channels in backside of wafer. (e) Fabrication of Through Silicon Vias (TSVs). (f) Fabrication of flow focusing generators. (g) The 3D etched wafer and 4” Borofloat 33 glass wafers are anodically bonded to encapsulate the microfluidic channels. (h) Scanning electron micrograph image shows the sequential etch process of fabrication in VLSDI 2.0 chip. Scale bar 115 µm, for ease of comparison the images are not flipped.
spacing between channels is less than 8 µm and the resist can delaminate in the presence of developer or during SRD. Subsequently, 4 µm of photore sist is spray coated, soft baked in an oven at 130°C for 5 minutes, and exposed to UV with the droplet maker channel (Layer 6) photomask. After exposure, the wafer is left at room temperature for 10 minutes. The wafer is then developed in MF 319 for 2 minutes and cleaned in SRD and kept at 100°C for 5 minutes. The wafer is cleared in SRD again and etched in DRIE to a 24 µm depth to form the droplet generators.

Finally, the 3D etched wafer is permanently bonded to two 4” diameter Borofloat 33 glass wafers to encapsulate the microfluidic channels (Fig. 7g). The 3D etched wafer is cleaned in acetone, IPA, and DI water for 5 minutes each and then in nanostrip for an hour. The 3D etched wafer and a 4 inch Borofloat 33 glass wafer are kept in piranha solution for 1 hour and immersed in deionized water for 5 minutes, and cleaned in SRD. The cleaned wafers are anodic bonded by applying 100 N force and 800 Volts for an hour in an EVG 510 anodic bonding tool. Another 4 inch Borofloat 33 glass wafer with excimer laser-drilled 1 mm holes that serve as inlets and outlets is cleaned in acetone, IPA, and DI water for 5 minutes each. The laser drilled glass wafer and the VS LDI 2.0 chip are kept in piranha solution for 1 hour and then immersed in deionized water. To completely remove the piranha solution from the microchannels, a long immersion time in water is recommended. The wafers are anodic bonded, applying 100 N force and 800 Volts for an hour. Both wafers are cleaned thoroughly and handled carefully in the entire process during bonding procedure to avoid possible dust or debris that may result in weak anodic bonding (Fig. SI 10 that may finally result in device leakage during operation (Fig. SI 11). To connect the VS LDI 2.0 chip to the outside world, we subsequently connect the chip to a custom-built pressure-driven flow manifold. Stainless steel compressed tube fittings (1/8” tube OD) from McMaster Carr (52245K609) are bonded to the glass wafer using chemically resistant epoxy from Master Bond (EP41S-5). The epoxy is allowed to cure at room temperature for 4 days. 1/8” OD PTFE tubes were connected to the fittings. Pressure driven flow is used to conduct the experiments. Nitrogen pressure tanks were connected to the 1 gallon and 3 gallon stainless steel pressure vessels (Alloy products). The 1 gallon vessel is used for dispersed phase and the 3 gallon vessel is used for continuous phase. The VS LDI 2.0 chip is connected to the pressure vessels using PTFE tubings. The VS LDI 2.0 chip is housed in a custom-built acrylic box and mounted onto an x y z translational stage. Inline filters (McMaster Carr: 9816K72) are used to filter debris for both the continuous and dispersed phases. An inline flow meter (McMaster Carr: 5084K23) is used to measure the flow rate of water phase. The detailed experimental setup for VS LDI 2.0 chip is shown in Fig. SI 9.

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Acknowledgements
We thank Professor Mark Allen for his comments and inputs on our manuscript. We thank Noah Clay (Director), Meredith Metzlerm, Kyle Keenan, Hiromichi Yamamoto, Eric Johnston, David Jones, Gyuseok Kim, Charles Veith, Jarret Gilinger and all of the QNF Staff at University of Pennsylvania for their help in device fabrication. We would like to acknowledge support from The National Science Foundation (1554200), Chip Diagnostics, and The Hartwell Foundation. D.L. acknowledges the support from NSF CBET 1604536.

Author Contributions
S.Y. conceived and performed all designs, fabrication, experiments, and characterization in this study, as well as prepared the manuscript and figures. D.L. and D.I. conceived and oversaw all aspects of this study, and prepared the manuscript.

Additional Information
Supplementary information accompanies this paper at https://doi.org/10.1038/s41598-019-48515-4.

Competing Interests: The authors declare no competing interests.

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