A simplified SVPWM method for cascaded multilevel inverters

Nishant Matale¹, Mohan Thakre¹ and Rakesh Shriwastava²

¹K.K. Wagh Institute of Engineering Education and Research, Nashik, India
²MCOE &RC, Nashik, India

mpthakre@kkwagh.edu.in

Abstract. A highly popular alternative in medium voltage and high-power applications is multilevel converters because of their superior performance over conventional two-level converters. The most commonly used control methods in the case of multilevel inverters are sine pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM) methods. Among these two control strategies, SVPWM has superior performance over SPWM in terms of DC bus voltage utilization along with a reduction in total harmonic distortion (THD) of line voltages. The classical SVPWM method has various drawbacks such as computational complexity for identifying the location of reference voltage vector, sector identification, region identification, memory requirement to store lookup tables for switching vectors. The novel simplified SVPWM technique is presented for cascaded H-Bridge multilevel inverter (CHBMLI) in this paper. This simplified SVPWM method has overcome the drawbacks of the classical SVPWM method. This new technique has been implemented into a five-level CHBMLI to evaluate performance and also to compare with the SPWM method. The simulation has been performed in MATLAB software.

Keywords. CHBMLI, SVPWM, SPWM, THD, simplified SVPWM

1. Introduction

In recent years requirement of medium voltage and high-power rating equipment in various industrial applications has been increased drastically [1]. The high-power and medium voltage are desired for a large number of motor drives and utility applications. The multilevel inverters are desired alternatives for these applications [2]. The multilevel inverters are formed by high quantity of semiconductor switches through some lesser DC voltage sources in order to produce staircase waveform of voltage. A multilevel term starts with three-level converters. The merits of multilevel converters over two-level converters are reduced harmonics into line voltages and output currents, less stress in voltage across semiconductor switches, less common-mode voltages and better output waveform quality [3]. The three basic topologies of multilevel inverters are diode-clamped (DCMLI), flying-capacitor (FCMLI) and CHBMLI. Among all these topologies of multilevel inverters, a CHBMLI is widely used because of its advantages such as a highly modular structure and lower number of device count as no clamping diodes and voltage balancing capacitors are needed [4-5].

The working of any multilevel inverter is mainly depending upon modulation technique. The most popular control methods aimed at multilevel inverters are SPWM and SVPWM methods [6]. The phase disposition (PD) based sine PWM method is extensively described for multilevel inverters due
to its merits like easy implementation and lower computational burden [7]. On the other hand, the SVPWM method is advantageous to the SPWM method due to better utilization of DC link voltage, improved harmonic profile and also the ability to work in the over-modulation range [8-12]. The classical SVPWM method involves four steps, such as to identify the number of sectors based on reference voltage vector angle along with triangle number and type of triangle then to calculate dwell times of active vectors followed by a selection of redundant switching states then to generate switching sequence and Lastly calculation of ON times for each switching device [13-16]. The execution of the classical space vector PWM technique is relatively difficult because of a high quantity of triangles along with a high quantity of redundant switching states present within a space vector diagram (SVD) [17-19]. A method based on the decomposition of SVD of a 3-level inverter in six 2-level SVD is presented in [20-26] having high complications for increased levels. Another SVPWM algorithm is presented in [27] based on 60 degrees co-ordinate system has drawbacks like improper switching states and voltage imbalance problems in a capacitor. A novel simplified SVPWM method for CHBMLI is presented in this paper. This simplified technique does not require sector identifications, look-up tables or any other calculations as required in the classical SVPWM method.

2. Cascaded multilevel inverter
The highly popular topology of multilevel inverters aimed at high-power and medium voltage operations is CHBMLI [4]. A CHBMLI is generally consist of several h-bridge power cell modules. The main purpose of connecting these modules in series at the AC side is to obtain medium voltage and reduced harmonics. The main advantage of a CHB multilevel inverter is its modular structure as well as being easy to replace in case of failure. A high number of isolated DC sources are required by CHB multilevel inverter for feeding separate h-bridge power cells. An individual module can yield three various levels of voltage such as +V_{dc}, 0 and -V_{dc} by using different combinations of switches. A 5-level CHB multilevel inverter can produce five different levels of voltage such as +2V_{dc}, +V_{dc}, 0, -V_{dc} and -2V_{dc} by using two DC sources as illustrated in figure 1.

![Figure 1. Three-phase 5-level CHBMLI.](image-url)
3. PWM techniques
For multilevel power conversion applications, various modulation techniques are used. The two main categories of these PWM methods are SPWM and SVPWM methods. For CHBMLIs generally, carrier-based PWM techniques and SVPWM techniques are applied. The SVPWM method turn out to be difficult as the number of level increases hence carrier-based techniques are more desired than the SVPWM technique.

3.1. Sinusoidal PWM technique
The carrier-based PWM strategies aimed at multilevel inverters are composed of two categories which are level-shifted PWM and phase-shifted PWM techniques. For level-shifted SPWM technique, a comparison is made between sinusoidal reference and vertically disposed triangular carriers. The number of triangular carriers for a five voltage levels is four. For a five-level CHBMLI, four carriers are required as illustrated in figure 2. These all carriers are having the same magnitude and frequency. The three schemes of level-shifted PWM techniques are phase opposite disposition (POD), PD and alternative phase opposite disposition (APOD). Among these three schemes, the PD scheme is desired because it gives the finest harmonic spectrum. In the PD scheme, all carriers are in phase. The amplitude modulation index \( m_a \) is used to vary the magnitude of inverter output voltage. The \( m_a \) in case of multilevel inverter is given by,

\[
m_a = \frac{V_m}{V_{cr}(m-1)}
\]

Where \( V_m \) is magnitude of the reference wave and \( V_{cr} \) is magnitude of individual triangular carriers. Whereas frequency modulation index \( m_f \) is given by,

\[
m_f = \frac{f_{cr}}{f_m}
\]

Where \( f_{cr} \) is triangular carriers’ frequency and \( f_m \) is reference wave frequency.

Figure 2. Sine modulating wave and carrier waves for the five-level inverter.

3.2. Simplified space vector PWM technique
The classical SVPWM technique involves the complex calculation of sector identification as well as lookup tables for switching states in the case of multilevel inverters. For determining switching time interval in case of multilevel inverter the classical space vector PWM method requires plotting of
outside sector into internal sub hexagon sector. A new simplified SVPWM method is proposed in which an offset voltage is added to the reference phase voltages. By adding this offset voltage, we can obtain classical SVPWM like performance. To get the maximum possible DC bus voltage utilization, we have to add this offset voltage \( V_{\text{offset}} \) into the reference phase voltages.

\[
V_{\text{offset}} = -\frac{V_{\text{max}} + V_{\text{min}}}{2}
\]  

(3)

Where \( V_{\text{max}} \) and \( V_{\text{min}} \) are extreme and least magnitudes of sampled reference phase voltages into that particular sampling interval. The active switching vectors in an inverter are getting placed in the center within a given sampling period by adding \( V_{\text{offset}} \) into reference phase voltages. Figure 3 shows the modified reference wave with triangular carriers. These space vector references are then compared with triangular carriers in order to produce gate signals for switching devices.

![Figure 3. Simplified space vector reference with triangular carriers in five-level CHBMLI.](image)

4. Simulation results and discussions

The MATLAB/SIMULINK tool is used to show the effectiveness of this novel simplified SVPWM method. A five-level CHBMLI with RL load is used for simulation purposes. The line voltages of a five-level CHBMLI for various amplitude modulation index \( M_a \) are obtained separately for the SPWM method and simplified SVPWM method along with their THD values. The values of simulation model is given in table 1.

**Table 1. Simulation parameters.**

| Parameter             | Value  |
|-----------------------|--------|
| DC voltage            | 100 V  |
| Fundamental Frequency | 50 Hz  |
| Switching Frequency   | 1050 Hz|
| Resistive load (R)    | 50 ohms|
| Inductive load (L)    | 20 mH  |
4.1. Simulation results of a five-level CHBMLI by using the SPWM method

The subsystem of the SPWM method for a five-level CHBMLI is shown in figure 4. The output line voltage of a five-level CHBMLI for \( M_a = 1 \) using the SPWM method is illustrated in figure 5 and figure 6 shows their respective THD value.

Figure 4. Subsystem for a five-level CHBMLI using SPWM method.

Figure 5. Five-level CHBMLI output line voltage for \( M_a = 1 \).

Figure 6. Five-level CHBMLI output line voltage THD for \( M_a = 1 \).
Figure 7. Five-level CHBMLI output line voltage for $M_a=0.8$.

Figure 8. Five-level CHBMLI output line voltage THD for $M_a=0.8$.

Figure 9. Five-level CHBMLI output line voltage for $M_a=0.6$.

Figure 10. Five-level CHBMLI output line voltage THD for $M_a=0.6$.

Figure 11. Simulation model for a generation of modified SVPWM reference waves.

Figure 7 shows the line voltage of a five-level CHBMLI for $M_a=0.8$ using the SPWM method and figure 8 shows their respective THD value. Figure 9 illustrated the five-level CHBMLI output line voltage for $M_a=0.6$ using the SPWM method and figure 10 shows their respective THD value.

4.2. Simulation results of a five-level CHBMLI by using simplified SVPWM method
The simulation model for a generation of the modified SVPWM reference wave is illustrated in figure 11.

**Figure 12.** Five-level CHBMLI output line voltage for $M_a=1$.

**Figure 13.** Five-level CHBMLI output line voltage THD for $M_a=1$.

**Figure 14.** Five-level CHBMLI output line voltage for $M_a=0.8$.

**Figure 15.** Five-level CHBMLI output line voltage THD for $M_a=0.8$.

**Figure 16.** Five-level CHBMLI output line voltage for $M_a=0.6$.

**Figure 17.** Five-level CHBMLI output line voltage THD for $M_a=0.6$.

Figure 12 illustrated the 5-level CHBMLI output line voltage for $M_a=1$ using the simplified SVPWM method and figure 13 shows their respective THD value. Figure 14 illustrated 5-level CHBMLI output line voltage for $M_a=0.8$ and figure 15 shows their respective THD value. Figure 16 illustrated the 5-level CHBMLI output line voltage for $M_a=0.6$ using the simplified SVPWM method and figure 17 shows their respective THD value.
Table 2. Comparison of simplified SVPWM with SPWM.

| Modulation Index (Ma) | SPWM | Simplified SVPWM |
|-----------------------|------|------------------|
|                       | THD in line Voltage (%) | Fundamental voltage component | THD in line Voltage (%) | Fundamental voltage component |
| 1                     | 17.42 | 346.5 | 12.79 | 397.9 |
| 0.8                   | 22.13 | 276.3 | 16.78 | 319.6 |
| 0.6                   | 25.54 | 207.9 | 24.52 | 236.8 |

The results of simulation shows that the fundamental voltage component is more in line voltage of a five-level CHBMLI when controlled by simplified SVPWM method because of better utilization of DC bus voltage than in SPWM method. Also, the harmonic profile is improved in the simplified SVPWM method than SPWM method as shown in table 2.

5. Conclusion
A novel simplified SVPWM technique is implemented for a five-level CHBMLI in this paper. This simplified SVPWM method does not require complex and time-consuming calculations of sector identification, region identification and any lookup tables as required in the classical SVPWM method. A comparison is made between this new simplified SVPWM method and the SPWM method. This simplified SVPWM method gives higher fundamental voltage components in line voltage due to better DC link voltage utilization as compared to the SPWM method. Also, this method provides an improved harmonic profile in line voltage of CHB multilevel inverter than the SPWM method. This new simplified SVPWM method gives all the advantages of the classical SVPWM method.

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