High speed graphene-silicon electro-absorption modulators for the O-band and C-band

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In the past few years, graphene, a two-dimensional network of sp2-hybridised carbon atoms, has attracted a lot of interest due to its unique optoelectronic properties.1–3) Graphene is a zero bandgap material, with an optical bandwidth from visible to infrared (up to 180 nm in the C-band).4,5) It absorbs 2.3% of the light incident perpendicularly to the C-band.5,6) This can be enhanced further by integrating graphene on a waveguide to increase the interaction length between light and graphene.7 Graphene’s absorption can be easily tuned through capacitive charging by applying an electric field,8 and has therefore the potential to enable active optoelectronic functionality onto passive optical waveguides, such as Si and low-loss SiN waveguides.9,10) In addition, graphene is CMOS compatible and can be integrated into CMOS processes in the back end of line.11) These properties, together with the high carrier mobility (e.g., more than 300 000 cm2 V−1 s−1 with hBN encapsulation9), make graphene a candidate for applications in high-speed optoelectronic devices, such as photodetectors8–10) and modulators.11–21)

High-speed graphene modulators have been reported in literature in single-layer graphene (SLG)4–6,13–15,19) or double-layer graphene (DLG)13,14,20,21) configuration on top of the waveguide. DLG modulators are based on a graphene-oxide-graphene capacitor, while SLG modulators are based on a graphene-oxide-silicon (GOS) capacitor. Due to the presence of two graphene layers, DLG modulators offer potential for higher ER than SLG modulators, but they suffer from higher IL. In addition, SLG modulators have a simpler fabrication process compared to DLG modulators, requiring the transfer of only one graphene layer. A DLG ring modulator with 30 GHz 3 dB frequency response and open eye diagrams at 22 Gbit s−1 was demonstrated by reducing the capacitance of the device using a 65 nm thick Al2O3 as spacer between the two graphene layers.14) However, employing a thick Al2O3 comes at the expense of the high drive voltage (7.5 Vpp) and high DC bias (−30 V) necessary to operate the device. In addition, the device has limited optical bandwidth, due to the resonant nature of the ring modulator. A more recent work reports a 120 μm long DLG electro-absorption modulator (EAM), built on top of a silicon waveguide with a 20 nm thick SiN spacer between the two graphene layers, exhibiting 20 μm 3 dB extinction ratio (ER) and 16.0 GHz 3 dB bandwidth at 1 V DC bias. In the C-band EAM we achieve 6.5 dB ER and 14.2 GHz 3 dB bandwidth at 0 V DC bias. Open eye diagrams up to 50 Gbit s−1 are measured using 2.5 Vpp and −0.5 V DC bias at a wavelength of 1560 nm.© 2020 The Japan Society of Applied Physics

1. Introduction

Electro-optical modulators are key components in optical communication systems. Important requirements for modulators are low insertion loss (IL), high extinction ratio (ER), high operation speed and low energy consumption. In the past few years, graphene, a two-dimensional network of sp2-hybridised carbon atoms, has attracted a lot of interest due to its extraordinary properties, i.e., wide optical bandwidth, tunable absorption, high carrier mobility, and CMOS compatibility. It is a candidate to improve current state-of-the-art high-speed optoelectronic devices, such as modulators. In this work, we present a model that describes the DC and high-speed behaviour of single-layer graphene-oxide-silicon electro-absorption modulators (EAM). We compare the theoretical analysis with experimental results, and we find that p-doped graphene combined with n-doped silicon enables high-speed operation at low DC bias. Using this configuration, we demonstrate 75 μm long TM EAMs operating in the O-band and in the C-band. The O-band EAM exhibits 3.1 dB extinction ratio (ER) and 16.0 GHz 3 dB bandwidth at 1 V DC bias. With the C-band EAM we achieve 6.5 dB ER and 14.2 GHz 3 dB bandwidth at 0 V DC bias. Open eye diagrams up to 50 Gbit s−1 are measured using 2.5 Vpp and −0.5 V DC bias at a wavelength of 1560 nm.

1 V DC bias. With the C-band EAM we achieve 6.5 dB ER and 14.2 GHz 3 dB bandwidth at 0 V DC bias. Open eye diagrams up to 50 Gbit s−1 are measured using 2.5 Vpp and −0.5 V DC bias at a wavelength of 1560 nm.

The best static and high-speed performance is obtained on TM EAMs. The O-band EAM with 4.2 dB IL, 3.1 dB ER using 8 Vpp and 16.0 GHz 3 dB frequency response is demonstrated across a total wavelength range of 140 nm. On a 75 μm long O-band TM SLG EAM, we achieve 4.0 dB IL, 3.1 dB ER using 8 Vpp and 16.0 GHz 3 dB frequency response at 1 V DC bias at 1300 nm wavelength. In the C-band, we demonstrate a 75 μm long broadband SLG EAM with 4.2 dB IL, 6.5 dB ER using 8 Vpp and 14.2 GHz 3 dB frequency response at 0 V DC bias and 1560 nm wavelength. 

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wavelength. Open eye diagrams are obtained up to 50 Gbit s\(^{-1}\) at 1560 nm wavelength for the first time on a SLG EAM, using 2.5 V\(_{pp}\) and −0.5 V DC bias, thus showing potential for graphene integration in high-speed photonics applications.

2. Device design and fabrication

The SLG-silicon EAM is based on a 220 nm thick silicon (Si) waveguide, fabricated on a silicon-on-insulator (SOI) wafer with 2 μm buried oxide in imec’s 200 nm Si photonics platform [Fig. 1(a)].\(^{22}\) The waveguide is partially etched on one side, creating a rib structure that allows to contact the Si waveguide through the 70 nm thick slab layer. The waveguide is embedded in SiO\(_2\) to ensure a planar surface for the subsequent graphene transfer. Three separate doping levels (\(n^{++}\) or \(p^{++}\) for the contact region, \(n_{\text{slab}}\) or \(p_{\text{slab}}\) for the slab region, \(n_{\text{wg}}\) or \(p_{\text{wg}}\) for the waveguide region) are used to minimise the Si contact and sheet resistance, without significantly increasing the waveguide loss. After Si waveguide patterning, a chemical-mechanical planarisation step is performed to planarise the waveguides. Through thermal oxide growth the desired SiO\(_2\) thickness of 5 nm is obtained on top of the Si waveguide. After wafer dicing, subsequent processing is performed at coupon level in a cleanroom lab environment. Graphene grown by chemical vapour deposition is transferred on top of the Si waveguides. Both growth and transfer processes were carried out by Graphenea (www.graphenea.com). Subsequently, graphene is patterned to cover part of the Si waveguide and to define the length of the EAM. Contacts are made to graphene (50 nm Pd) and to the doped Si (10 nm Ti/20 nm Pt/50 nm Au) based on a standard lift-off process. These contact metals were selected to minimise the contact resistance to graphene and to Si respectively.\(^{23}\) The contacts are placed 2 μm away from the waveguide and therefore have no impact on transmission loss. The graphene and silicon contacts are used to apply an electric field across the device, which modulates the Fermi level in graphene.

3. Device modeling

3.1. Static electro-optical behaviour of the SLG EAM

The static electro-optical behaviour of the SLG EAM is defined by the relation between the absorption and graphene’s Fermi level \(\mu\). Graphene’s absorption is derived from the 2D complex optical conductivity \(\sigma_2(\omega, \Gamma, T, \mu)\), calculated from the Kubo formula.\(^{24}\) This formula takes into account interband and intraband transitions, and it depends on the angular frequency \(\omega\), the charged particle scattering rate \(\hbar \Gamma\), the temperature \(T\), and most importantly graphene’s Fermi level \(\mu\). The latter can be shifted by sweeping the voltage \(V_g\) across the GOS capacitor,\(^{25}\) according to

\[
V_g = \frac{q(n_0 + n_s)}{C_{\text{GOS}}} = \frac{q}{\pi(\hbar v_F)^2} \frac{\mu^2}{C_{\text{GOS}}},
\]

where \(q\) is the elementary charge, \(\hbar\) is the reduced Planck constant, \(v_F\) is the Fermi velocity of carriers in graphene and \(C_{\text{GOS}}\) is the capacitance of the GOS capacitor. The Fermi level \(\mu\) is the sum of two contributions:

\[
\mu = \mu_0 + \Delta \mu.
\]

\(\mu_0\) is the initial Fermi level position due to the fixed number of charges \(n_0\) (graphene’s intrinsic doping), and \(\Delta \mu\) is the Fermi level shift caused by the number of charges \(n_s\) accumulated on graphene when we apply \(V_g\) across the capacitor.

The static electro-optical behaviour of the SLG EAM as a function of applied voltage is mainly affected by two parameters: graphene’s intrinsic doping \((n_0)\) and the scattering rate \(\hbar \Gamma\). The intrinsic doping \(n_0\) affects the position of minimum transmission as a function of applied voltage. Figure 2(a) shows the simulation, performed using Numerical MODE Solutions, of the optical transmission as a function of gate voltage for a TE SLG EAM with 5 nm thick SiO\(_2\) and 500 nm wide waveguide operating at 1560 nm, for neutral \((n_0 = 0 \text{ cm}^{-2})\) and \(p\)-doped \((n_s = 12 \times 10^{12} \text{ cm}^{-2})\) graphene, for scattering rate \(\hbar \Gamma = 15 \text{ meV}\). For neutral graphene, the minimum is at 0 V, therefore switching between high transmission (on-state) and low transmission (off-state) requires \(\sim 3.5\) or \(\sim 4\) V DC bias. For \(p\)-doped graphene, the minimum transmission point is shifted to negative bias. In this case, switching occurs between −2 and 2 V, which is compatible with current CMOS technology. The scattering rate \(\hbar \Gamma\), which is inversely proportional to the mobility \(\mu\), affects the ER of the modulator. As shown in Fig. 2(b), a lower scattering...
rate, implying higher graphene quality, results in higher ER for a given $V_{gg}$ because graphene can reach full transparency. For example, a 75 μm long SLG EAM would show 0.5 dB higher ER for $h\Gamma = 0.43$ eV compared to $h\Gamma = 30$ eV. In real applications, graphene’s scattering rate is often more than 10 meV, resulting in a reduced ER and increased IL.

3.2. RC limited high-speed behaviour of the SLG EAM

The 3 dB frequency response of a SLG EAM is limited by the RC constant of the device, and can be explained using the equivalent electrical circuit in Fig. 1(b).

3.2.1. Device resistance.

The device total resistance ($R_{tot}$) is the sum of graphene’s contact and sheet resistance ($R_{graC}$ and $R_{gra}$) and the Si contact and sheet resistance ($R_{SiC}$ and $R_{Si}$).

Graphene’s resistance is affected by the scattering rate $h\Gamma$, which is proportional to the impurity density $n^*$, caused by local potential fluctuations and electron/hole puddles on the graphene layer.25,26 Higher scattering rate corresponds to lower mobility and therefore higher resistance. When the mobility is higher (lower $h\Gamma$ and $n^*$), the peak in graphene’s resistance corresponding to the neutrality point is higher. As a consequence, the resistance experiences a more abrupt change when the gate voltage is increased or decreased to move away from the neutrality point.24 The values of $R_{graC}$ and $R_{gra}$ at a fixed DC voltage bias are also affected by graphene’s intrinsic doping $n_0$. For $n_0 = 0$, graphene’s resistance reaches its peak value at 0 V voltage bias, and decreases for increasing (or decreasing) voltage bias. When applying $V_{gg}$ as indicated in Fig. 1(a), p-doped (n-doped) graphene shows a peak value at negative (positive) voltage bias due to the shift of graphene’s charge neutrality point [Fig. 3(a)]. The resistance then decreases as the voltage increases (decreases). In case of p-doped graphene, there is therefore a low resistance region for voltage values around or greater than 0 V. The Si contribution to $R_{tot}$ depends on the doping level of the three Si regions: contact, slab and waveguide areas. To properly estimate how the silicon doping impacts the resistance, we perform a process simulation using Sentaurus TCAD, which accurately emulates the real processing performed in the fab. Afterwards we extract the values of silicon resistance ($R_{Si}$ and $R_{SiC}$) for the three doped regions together (contact, slab and waveguide) by performing a transient device simulation at different voltage values. Figure 3(b) shows the values of $R_{tot}$ as a function of gate voltage for a 75 μm long device with p-doped graphene (mobility $\mu_c = 800 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$; $R_{graC} = 880 \Omega \mu\text{m}$ and $R_{gra} = 3400\square$ at 0 V) and a waveguide width of 500 nm, for p-doped ($p_{eq} = 1.9 \times 10^{18} \text{ cm}^{-3}$, $p_{dab} = 3.2 \times 10^{19} \text{ cm}^{-3}$) and n-doped ($n_{eq} = 2.3 \times 10^{18} \text{ cm}^{-3}$, $n_{dab} = 2.7 \times 10^{19} \text{ cm}^{-3}$) Si, p-doped silicon exhibits higher sheet resistance than n-doped silicon, due to the lower mobility of holes compared to electrons. The variation of $R_{tot}$ with gate voltage is influenced by the voltage-dependent behaviour of $R_{graC}(V)$ and $R_{gra}(V)$ only.

3.2.2. GOS capacitance.

The total GOS capacitance $C_{GOS}$ is given by the series of graphene’s quantum capacitance $C_q$, the oxide capacitance $C_{ox}$ and the Si depletion capacitance $C_{Si}$:

$$\frac{1}{C_{GOS}} = \frac{1}{C_q} + \frac{1}{C_{ox}} + \frac{1}{C_{Si}}. \quad (3)$$

Graphene’s quantum capacitance is given by the following equation:\n
$$C_q = \frac{2q^2}{\hbar \nu_F \sqrt{\pi}} \sqrt{|n_i + n_d|} = \frac{2q^2}{\hbar^2 \nu_F \sqrt{\pi}} |\mu|, \quad (4)$$

where $\mu$ is graphene’s Fermi level as defined in Eq. (2). The quantum capacitance is characterised by a minimum when $\mu = 0$ [Fig. 4(a)], and it increases linearly for $|\mu| > 0$ [Fig. 4(b)]. For intrinsic (undoped) graphene, the Fermi level is at the Dirac point, $\mu_0 = 0$ and therefore $C_q = 0$ for $\Delta \mu = 0$ [Fig. 4(b)]. In p-doped (n-doped) graphene, $\mu_0 < 0$ ($\mu_0 > 0$) and, as a consequence, the minimum of $C_q$ is located at $\Delta \mu = -\mu_0$ [Fig. 4(b)]. When graphene is not pristine, the additional impurity carrier density $n^*$ should be included in the calculation. The quantum capacitance becomes:

$$C_q = \frac{2q^2}{\hbar^2 \nu_F \sqrt{\pi}} \sqrt{|n_i + n_d| + |n^*|}. \quad (5)$$

If we compare $C_q$ with $C_{ox}$ calculated for 5 nm of SiO$_2$ (Fig. 4), we see that the latter is significantly smaller for each value of $\mu$ away from the neutrality point. When $n^* > 0$, the minimum of the quantum capacitance increases and $C_q$ becomes significantly higher than $C_{ox}$ for any value of chemical potential, as shown by the dotted lines in Fig. 4. For this reason, when placed in series with $C_{ox}$, the contribution of $C_q$ is minor.

The analytical model used to calculate $C_{GOS}$ as a function of applied voltage $V_s$ is based on the MOS capacitor...
neutral graphene (n-resistance as a function of gate voltage of a 75 μm long SLG EAM with p-doped graphene (n_0 = 12 × 10^{12} cm^{-2}), for p-doped (n_p= 1.9 × 10^{18} cm^{-3}, \rho_{gdx} = 3.2 × 10^{12} cm^{-3}) and n-doped silicon (n_{eq} = 2.3 × 10^{18} cm^{-3}, n_{dab} = 2.7 × 10^{19} cm^{-3}). P-doped silicon exhibits higher sheet resistance than n-doped silicon. The voltage-dependent behaviour is caused by R_{gdx} and R_{gtr}.

\[ C_{n} = \frac{q}{C_{ox}} n_{s} + \left( \frac{hv_{F}^2 \sqrt{n_{s} + n_{0}}}{2q} \right) \sqrt{n_{s} + n_{0} + |n^*|} + (V_{FB} - V_{F}) = 0. \]  

(7)

Once the value of \( n_{s} \) for each \( V_{F} \) is known, we can calculate \( C_{q} \) through Eq. (4) and therefore the total accumulation capacitance \( C_{GOS,acc} = \frac{n_{s}}{C_{ox} (n_{s} + n_{0}) + |n^*|} \). Graphene's natural doping \( n_{0} \) is considered in the calculation as an initial condition and it will automatically affect the position of graphene's charge neutrality point in the final result. In fact, \( n_{s} \) and \( n_{0} \) in Eq. (4) are summed up before applying the absolute value, which is necessary to make a distinction between n-doped (\( n_{0} < 0 \)) and p-doped graphene (\( n_{0} > 0 \)). In inversion (\( V_{F} > V_{FB} > 0 \) for p-doped Si and \( V_{F} < V_{FB} < 0 \) for n-doped Si, where \( V_{FB} \) is threshold voltage) the silicon layer has reached maximum depletion and the quantities to be considered are \( C_{q}, C_{ox} \) and \( C_{Sl,max} \). Equation (7) becomes

\[ \frac{q}{C_{ox}} n_{s} + \left( \frac{hv_{F}^2 \sqrt{n_{s} + n_{0}}}{2q} \right) \sqrt{n_{s} + n_{0} + |n^*|} + (V_{FB} - V_{F} - 2\phi_{F}) = 0, \]  

(8)

where the bulk potential \( \phi_{F} \) takes into account the voltage drop due to \( C_{Sl,max} \). The total inversion capacitance can be calculated as

\[ C_{GOS,inv} = \left( \frac{1}{C_{ox}} + \frac{1}{C_{e}} + \frac{W_{dep,max}}{\alpha_{0} n_{s}} \right)^{-1}, \]  

where \( W_{dep,max} \) is the maximum width of the depletion region in the silicon layer.

To calculate the total capacitance \( C_{GOS,dep} \) in depletion (\( V_{FB} < V_{F} < V_{F} \) for p-doped Si and \( V_{FB} > V_{F} \) for n-doped Si), a different approach is necessary. The width of the depletion region in silicon \( W_{dep} \) has to be calculated for values of the surface potential \( \phi_{s} \) ranging from 0 to 2\( \phi_{F} \). From
Fig. 5. (Color online) (a) Graphene quantum capacitance as a function of gate voltage for n-doped \( n_0 = -12 \times 10^{12} \text{ cm}^{-2} \), neutral \( n_0 = 0 \text{ cm}^{-2} \) and p-doped \( n_0 = 12 \times 10^{12} \text{ cm}^{-2} \) graphene \( n^* = 5 \times 10^{11} \text{ cm}^{-2} \). The minimum of \( C_q \) shifts depending on the graphene doping. (b) GOS capacitance as a function of gate voltage with fixed p-type silicon waveguide doping \( n_{\text{wg}} = 1.0 \times 10^{18} \text{ cm}^{-3} \), for n-doped \( n_0 = -12 \times 10^{12} \text{ cm}^{-2} \), neutral \( n_0 = 0 \text{ cm}^{-2} \) and p-doped \( n_0 = 12 \times 10^{12} \text{ cm}^{-2} \) graphene \( n^* = 5 \times 10^{11} \text{ cm}^{-2} \). \( C_q \) affects \( C_{\text{GOS}} \) only in proximity of its minimum.

3.3. Device optimisation

To optimise the SLG EAM for high-speed operation, the 3 dB frequency response of the device has to be maximised. This figure of merit is limited by the device RC constant, therefore the total resistance and capacitance of the device have to be minimised in the desired operating region in order to obtain the lowest possible RC. In fabricated devices, graphene is most often p-doped, due to dangling oxygen bonds in the SiO₂ below and also due to environmental and polymer contamination during processing.30,31 In terms of static electro-optical performance, as seen in Sect. 3.1, this means that the switching between on and off states takes place in the region between \(-2\) and \(2\) V voltage bias. This region corresponds to the low resistance region in case of p-doped graphene, as shown in Fig. 3. In order to have low capacitance in the same voltage range, p-doped Si is preferable because it allows to operate the device in depletion for voltage bias higher than 0 V. As a result, when p-doped graphene is combined with p-doped silicon, the total RC is reduced in the region between 0 and 2 V. Likewise, in case of n-doped graphene, the situation would be reversed and the best choice would be a device with n-doped silicon operating at low reverse bias. This is better visualised in the example in Fig. 7. Figure 7(a) shows the values of \( C_{\text{GOS}} \) as a function of gate voltage for a 75 μm long device with p-doped graphene \( n_0 = 12 \times 10^{12} \text{ cm}^{-2} \) and a waveguide width of 500 nm, for p-doped and n-doped Si (doping values in Table I). Using these values of \( C_{\text{GOS}} \) and values of \( R_{\text{hot}} \) from Fig. 3(b), the 3 dB frequency response is then extracted by simulating the electrical equivalent circuit in Fig. 1(b). Even though p-doped silicon exhibits higher sheet resistance than n-doped silicon, the considerably lower GOS capacitance of the EAM with p-doped silicon in the 0–2 V region allows to achieve a two-fold improvement in 3 dB frequency response at 0 V [Fig. 7(b)].

Patterning graphene under the contact area, e.g. with holes, to increase the edge contact perimeter between graphene and the metal can lead to a significant reduction in graphene’s contact resistance.32 Improved values of graphene contact and sheet resistance \( R_{\text{grac}} = 100 \Omega \) and \( R_{\text{grs}} = 60 \Omega/\square \) would allow to achieve a 3 dB frequency response of 17 GHz (18% improvement) at 0 V DC bias for a 75 μm long EAM and 25 GHz for a 25 μm long EAM. With reduced doping in the waveguide \( n_{\text{wg}} = 4 \times 10^{17} \text{ cm}^{-3} \) this values could be
further improved up to 23 and 31 GHz for $L_{\text{device}} = 75 \mu m$ and $L_{\text{device}} = 25 \mu m$ respectively.

4. Experimental results and discussion

In the first part of this experimental section, we compare the performance of four C-band SLG EAMs on TE waveguides between three samples, fabricated with different type and level of doping in Si. In Sect. 4.2, we select the sample with $p$-type Si doping and we compare the performance of C-band SLG EAMs on TE and TM waveguides, showing the benefit of using TM waveguides. In Sect. 4.3, on the same sample with $p$-type Si and using TM waveguides, we show uniform performance of SLG EAMs in the O-band, thus demonstrating broadband operation. In Sect. 4.4, we conclude that the best performance is given by SLG EAMs on TM waveguides in the C-band, and we measure open eye diagrams up to 50 Gbit s$^{-1}$.

4.1. Effect of Si waveguide doping on the performance of C-band TE SLG EAMs

We fabricated three samples with different type and level of doping in Si (summary in Table II). Sample A was fabricated with $n$-doped Si, with average carrier concentrations of $n_{\text{slab}} = 2.5 \times 10^{18} \text{ cm}^{-3}$ and $n_{\text{wg}} = 1.2 \times 10^{18} \text{ cm}^{-3}$ for the slab and the waveguide regions respectively. Sample B was fabricated using higher $n$-doping in the Si slab and waveguide regions than sample A ($n_{\text{slab}} = 2.7 \times 10^{19} \text{ cm}^{-3}$ and $n_{\text{wg}} = 2.3 \times 10^{18} \text{ cm}^{-3}$), with the purpose of reducing the total parasitic resistance without significantly impacting the GOS capacitance. Sample C was fabricated using $p$-doped Si ($p_{\text{slab}} = 3.2 \times 10^{19} \text{ cm}^{-3}$ and $p_{\text{wg}} = 1.9 \times 10^{18} \text{ cm}^{-3}$). The characterisation of the samples was carried out under ambient conditions.

The three samples were first characterised by performing unbiased fiber-to-fiber transmission measurements on SLG EAMs with waveguides optimised for TE mode propagation (TE waveguides, $W_{\text{wg}} = 500$ nm) and with four different device lengths ($L_{\text{device}} = 25, 40, 50$ and 75 $\mu m$). The transmission scales linearly with the device length, and the extracted average and standard deviation values of absorption are 0.08 ± 0.01, 0.08 ± 0.01 and 0.05 ± 0.01 dB $\mu m^{-1}$ for samples A, B and C respectively.

We then performed biased fiber-to-fiber transmission measurements on the same EAMs, by sweeping the wavelength from 1510 to 1600 nm, while applying a DC bias ranging from $-4$ to 4 V. Figure 8(a) shows the extracted ER versus device length ($L_{\text{device}}$) for the three samples at the peak transmission wavelength of 1560 nm. The values of ER scale...
compares the extracted 3 dB frequency response of the modulation curve compared to the other two samples. The average transparency, resulting in a more symmetrical transmission curve towards lower reverse bias. As a consequence, when the reverse bias on sample B is increased, graphene approaches again transparency, resulting in a more symmetrical transmission curve compared to the other two samples. The average and standard deviation values of modulation efficiency (ME = ER/Ldevice) across the four devices at 1560 nm are 0.03 ± 0.01, 0.05 ± 0.01 and 0.04 ± 0.01 dB μm⁻¹ for samples A, B and C respectively. The higher modulation in sample B is attributed to higher mobility in graphene compared to the other two samples. This is confirmed by the values of graphene’s mobility extracted from transfer length measurements (TLM) of graphene’s electrical test structures fabricated on the same sample (1610 cm² V⁻¹ s⁻¹ for sample B and 1490 cm² V⁻¹ s⁻¹ for sample C). The lower p-type graphene doping and the higher graphene mobility in sample B are attributed to sample-to-sample variations of graphene’s properties, caused by uncontrolled variations in processing conditions.

The electro-optical S21 frequency response of the modulators was measured between 100 MHz and 30 GHz at DC bias ranging from 0 to 2 V with a vector network analyser, using −8 dBm RF power and a 50 Ω load resistor. Figure 9(a) compares the extracted 3 dB frequency response (f3dB) of the three samples as a function of DC bias for Ldevice = 75 μm. Figures 9(b) and 9(c) compare the extracted Rtot and Cgos from the fitting of the S11 frequency response measured on the three samples, performed using the equivalent electrical circuit shown in Fig. 1(b). Among the n-doped samples, sample B exhibits the highest 3 dB frequency response at any forward voltage bias, with a maximum value of 8.9 GHz at 0 V DC bias for Ldevice = 75 μm. The decrease in Rtot (20% at 0 V DC bias) achieved in sample B with the higher doping in the slab and waveguide regions, counteracts the slight increase in Cgos caused by the higher waveguide doping (13% at 0 V DC bias). This allows to improve the f3dB from sample A to sample B at any forward voltage bias, e.g. with a gain of 2 GHz (29%) at 0 V DC bias (Table III). As expected from the theoretical analysis, the sample fabricated using p-doped Si (sample C) shows a substantial increase in 3 dB frequency response compared to sample B, with values up to 22.8, 21.6, 14.2 and 16.1 GHz at 0 V DC bias for Ldevice = 25, 40, 50 and 75 μm respectively (Table III). Even though the Si sheet resistance is higher, the lower Cgos obtained by operating the device in depletion mode instead of accumulation mode allows to significantly reduce the total RC constant, and thus enhance the 3 dB frequency response at any forward voltage bias. The values of f3dB decrease with higher device length, due to the increase in the total RC constant related to the 50 Ω load resistor (Table III).

4.2. Performance comparison of C-band TE and TM SLG EAMs

Despite the high 3 dB frequency response achieved with the sample with p-doped Si (sample C), the ER of the SLG EAMs remains limited when using TE-polarised light, with values ranging from 0.9 dB for Ldevice = 25 μm–2.6 dB for Ldevice = 75 μm. The performance with TE-polarised light can be improved by using an optimised waveguide thickness. However, in our case this approach is not possible due to specific waveguide height requirements of the fab used to fabricate the substrate. Using waveguides optimised for TM mode propagation (TM waveguides) can increase the ER for a given device length, due to the bigger overlap between the TM optical mode and the graphene layer compared to TE when the waveguide thickness is 220 nm [see inset of Fig. 10(a)]. To maximise the overlap with graphene but still ensure mode confinement in the waveguide, we use a waveguide width of 750 nm. Unbiased transmission measurements performed on sample C (p-doped Si) from 1510 to 1600 nm on SLG EAMs with TM waveguides, equivalent to the ones performed on TE waveguides, showed that graphene’s absorption is 0.09 ± 0.01 dB μm⁻¹, which is 2.3 times higher than the 0.04 ± 0.01 dB μm⁻¹ measured on TE waveguides, in agreement with the value of 2.2 extracted from Lumerical MODE simulations. The ME of the four SLG EAMs is consistent across the measured C-band spectrum for both TE and TM devices [Fig. 10(b)]. The drawback in using TM waveguides comes from the wider waveguide width, which leads to higher sheet resistance and GOS capacitance, resulting in a 1.1–1.5 times lower 3 dB frequency response compared to TE waveguides (Fig. 11). Nevertheless, due to the low Cgos...
at forward bias on the SLG EAMs with p-doped Si, TM waveguides exhibit 3 dB frequency response at 0 V DC bias of 20.7, 18.0, 15.7 and 14.2 GHz for $L_{\text{device}} = 25, 40, 50$ and 75 $\mu$m respectively.

### 4.3. Performance of O-band TM SLG EAMs

To demonstrate the broadband operation of graphene devices, we measured TM graphene-Si EAMs fabricated on sample C with exactly the same processing steps and cross section, but designed to operate in the O-band. We characterised four devices, with same lengths as the TM C-band devices demonstrated earlier ($L_{\text{device}} = 25, 40, 50$ and 75 $\mu$m) and waveguide width of 380 nm. Fiber-to-fiber transmission measurements from 1260 to 1330 nm, resulted in an average absorption across the four devices of $0.10 \pm 0.01$ dB $\mu$m$^{-1}$. The biased transmission measurements were performed sweeping the DC bias from $-4$ to 4 V and the wavelength from 1270 to 1320 nm. The average and standard deviation values of ME at the peak of the fiber grating couplers (1300 nm) across the four devices are $0.041 \pm 0.005$ dB $\mu$m$^{-1}$. The lower modulation efficiency compared to C-band TM devices is due to the higher energy of the photons in the O-band. As a consequence, it’s necessary to apply a higher voltage in order to achieve full transparency in graphene, which may result in oxide breakdown. The extracted ME of the four TM O-band SLG EAMs is consistent across the O-band spectrum, as shown in Fig. 12(a). The 3 dB frequency response of the O-band SLG EAMs, extracted from electro-optical $S_{21}$-parameters measurements at 1300 nm wavelength, reaches values of 19.7, 20.3, 19.3 and 16.0 GHz at 1 V DC bias for $L_{\text{device}} = 25, 40, 50$ and 75 $\mu$m respectively [Fig. 12(b)].

### Table III. Values of measured 3 dB frequency response ($f_{3\text{dB}}$) at 0 V DC bias on TE SLG EAMs for $L_{\text{device}} = 25, 40, 50$ and 75 $\mu$m. The $f_{3\text{dB}}$ is higher for sample C (p-doped Si) and for smaller device lengths.

| Sample | $L = 25 \mu$m | $L = 40 \mu$m | $L = 50 \mu$m | $L = 75 \mu$m |
|--------|---------------|---------------|---------------|---------------|
| Sample A | 10.9          | 7.7           | 8.2           | 6.9           |
| Sample B | 12.9          | 10.6          | 9.6           | 8.9           |
| Sample C | 22.8          | 21.6          | 14.2          | 16.1          |

Comparison of 3 dB frequency response between TE and TM SLG EAMs measured on sample C as a function of applied DC bias for different device lengths. TM SLG EAMs have lower $f_{3\text{dB}}$ than TE SLG EAMs.

### 4.4. Large signal high-speed performance

A summary of the performance of the C-band TE, C-band TM and O-band TM SLG EAMs on sample C is reported in Fig. 9.
The FOM is defined as ER/IL and should therefore be as high as possible. The C-band TM EAM represents the best compromise between IL and ER, as shown by the high value of FOM, while also exhibiting a 3 dB frequency response of 14 GHz. Eye diagrams were measured on the C-band SLG EAM with p-doped Si (sample C), TM waveguide and $L_{\text{device}} = 75 \mu m$ at 1560 nm using 2$^{23}$-1 PRBS, 2.5 Vpp, 14 dBm input optical power and a 50 $\Omega$ terminated probe. Open eye diagrams were generated from 5G b/s to 50 Gbit s$^{-1}$, thus demonstrating potential for high-speed data transmission using graphene technology. Examples at 10, 25 and 50 Gbit s$^{-1}$ are shown in Fig. 13(a). The large-signal ER and the signal-to-noise ratio (SNR) are reported in Fig. 13(b) as a function of bit rate. The dynamic energy consumption ($E_{\text{bit}} = C V^2/4$) of the SLG EAM is calculated to be $\sim 112 \Omega$, while the static power consumption is $< 10^{-8}$ mW, due to the low leakage current flowing through the GOS capacitor ($< 10$ pA).

### Table IV

|       | IL (dB) | ER (dB) | FOM | $f_{\text{Sat}}$ (GHz) | $\lambda$ (nm) |
|-------|---------|---------|-----|------------------------|----------------|
| C-band TE | 3.0     | 2.6     | 0.9 | 16.1                   | 1510–1600      |
| C-band TM | 4.2     | 6.5     | 1.5 | 14.2                   | 1510–1600      |
| O-band TM | 4.0     | 3.1     | 0.8 | 16.0                   | 1270–1320      |

Fig. 12. (Color online) (a) Modulation efficiency as a function of wavelength of the four TM O-band SLG EAMs. The devices are broadband and the ME is consistent across the O-band spectrum. Inset: normalised transmission as a function of applied DC bias measured on the 75 $\mu m$ long EAM. (b) $S_{21}$ parameters measured on the four TM O-band SLG EAMs at 1 V DC bias.

Fig. 13. (Color online) (a) Eye diagrams measured at 10, 25 and 50 Gbit s$^{-1}$ on the SLG EAM with p-doped Si, TM waveguide and $L_{\text{device}} = 75 \mu m$ (sample C). (b) SNR and large-signal extinction ratio plotted as a function of the bit rate for the same device. The SNR and the ER remain higher than 3.0 and 1.0 dB respectively up to 35 Gbit s$^{-1}$.

5. Conclusion

In this paper we analysed the DC and high-speed performance of SLG-silicon EAMs. Three samples were fabricated by transferring p-doped graphene on Si waveguides with different type and level of silicon doping. By means of a theoretical model, the influence of the waveguide doping on the total parasitic resistance and capacitance of SLG-silicon EAMs was discussed and compared to experimental results from the three samples. We found that the best static and high-speed performance is obtained on SLG EAMs fabricated using p-doped silicon waveguides. We demonstrated high-speed performance on SLG EAMs in the O-band and in the C-band, for a total wavelength range of 140 nm. On a 75 $\mu m$ long O-band TM SLG EAM, we achieved 3.1 dB ER and 16.0 GHz 3 dB frequency response at 1 V DC bias at 1300 nm wavelength. In the C-band, we demonstrated a 75 $\mu m$ long broadband SLG EAM with 6.5 dB ER and...
14.2 GHz 3 dB frequency response at 0 V DC bias at 1560 nm wavelength. Open eye diagrams were obtained up to 50 Gbit s⁻¹ using 2.5 Vpp and −0.5 V DC bias at 1560 nm, thus showing potential for the integration of SLG modulators in high-speed integrated photonics.

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