MgX: Near-Zero Overhead Memory Protection with an Application to Secure DNN Acceleration

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ABSTRACT
In this paper, we propose MgX, a near-zero overhead memory protection scheme for hardware accelerators. MgX minimizes the performance overhead of off-chip memory encryption and integrity verification by exploiting the application-specific aspect of accelerators. Accelerators tend to explicitly manage data movement between on-chip and off-chip memory, typically at an object granularity that is much larger than cache lines. Exploiting these accelerator-specific characteristics, MgX generates version numbers used in memory encryption and integrity verification only using on-chip state without storing them in memory, and also customizes the granularity of the memory protection to match the granularity used by the accelerator. To demonstrate the applicability of MgX, we present an in-depth study of MgX for deep neural network (DNN) and also describe implementations for H.264 video decoding and genome alignment. Experimental results show that applying MgX has less than 1% performance overhead for both DNN inference and training on state-of-the-art DNN architectures.

1. INTRODUCTION
As the technology scaling slows down, computing systems are increasingly relying on hardware accelerators to improve performance and energy efficiency. For example, modern ML models such as deep neural networks (DNNs) are often quite compute-intensive and increasingly run on hardware accelerators [8, 29] for both performance and energy efficiency. Similarly, hardware accelerators are widely used for other compute-intensive workloads such as video decoding, signal processing, cryptographic operations, genome assembly, etc. This paper proposes a novel off-chip memory protection scheme for hardware accelerators, named MgX (Memory guard for Xelerators), using secure DNN acceleration as a primary example application.

In many applications, the hardware accelerators may process private or sensitive data, which need strong security protection. For example, ML algorithms often require collecting, storing, and processing a large amount of personal and potentially private data from users to train a model. Moreover, due to its high computational demand, both training and inference are often performed on a remote server rather than a client device such as a smartphone, implying that the private data and ML models need to be stored in a remote server. Unfortunately, in traditional computing systems, private user data may be easily exposed or misused by the remote server if it is either compromised or malicious.

A promising approach to provide strong confidentiality and integrity guarantees even under untrusted software and potential physical tampering is to rely on trusted hardware to create a hardware-protected execution environment. This approach has primarily been studied in the context of general-purpose processors in the past. This paper considers extending this approach to accelerators. Figure 1 illustrates the approach in the context of a DNN accelerator. In order to protect sensitive data, the secure DNN accelerator keeps all confidential information including inputs, outputs, training data, and ML model parameters (weights) in an encrypted form outside of a trusted hardware boundary such as a custom ASIC, an FPGA accelerator, or an accelerator IP in an SoC. Each secure accelerator contains a unique private key that can only be used by the accelerator hardware itself. Users can authenticate the accelerator remotely using the corresponding public key and also send their private data and model parameters encrypted, which can only be decrypted and processed by the trusted accelerator. The secure accelerator also ensures that the ML computation cannot be tampered with by protecting the integrity of off-chip data. In this way, the secure DNN accelerator can ensure that private user data and weights cannot be accessed by an adversary even if they control the entire software stack on the system that contains the accelerator or can even physically access the off-chip DRAM.

The cryptographic protection of off-chip memory, namely memory encryption and integrity verification, represents an essential technology to enable the hardware-protected secure execution environment. The off-chip memory protection also represents the main source of performance overhead in the traditional secure processor designs [14, 18, 50, 53]. For a general-purpose processor, the memory protection schemes need to be able to handle any sequence of memory accesses to arbitrary memory locations, and typically protect memory accesses at a cache-block granularity. Each cache block is encrypted before written back to memory, and decrypted on a read. To hide decryption latency, the counter-mode encryption is often used, where a counter value (CTR) is encrypted with a block cipher to generate an encryption pad that is XORed with data for encryption. In secure processors,
the counter value is typically a concatenation of the memory address and a version number (VN) that increments on each write. The version number for each encrypted block is stored in memory. To protect integrity of off-chip memory, either a message authentication code (MAC) or a cryptographic hash needs to be attached to each cache block in memory. Moreover, in order to ensure freshness and prevent replay attacks, the integrity verification requires a tree of MACs. Unfortunately, the additional VN and MAC accesses can lead to non-trivial bandwidth and performance overhead for memory-intensive workloads.

In this paper, we show that memory encryption and integrity verification can be performed with almost no performance overhead for an application-specific accelerator by customizing protection to the accelerator-specific memory access pattern. We make key observations that the application-specific accelerators typically move data between on-chip and off-chip memory at a larger granularity than a cache block, and that the off-chip accesses are explicitly performed by the accelerator following a relatively simple control flow. The coarse-granularity data movements implies that the version numbers for memory encryption and the MACs for integrity verification can be maintained at a coarse granularity to reduce the overhead. Moreover, the relatively simple memory access patterns and the smaller number of version numbers suggest that version numbers can often be either stored on-chip or generated from the on-chip state without storing them in off-chip memory.

We study the memory access behaviors of DNNs such as convolutional neural networks (CNNs) and recurrent neural networks (RNNs) for both inference and training, and show how the version numbers can be determined even when dynamic pruning is used. By generating version numbers on-chip and performing protection at an application-specific granularity, MgX can eliminate most of overhead for off-chip memory protection; no version number is stored in the off-chip memory, no integrity tree is needed, and each MAC/hash protects a large amount of data instead of one cache block. We also study the applicability of MgX for H.264 video decoding and genome assembly acceleration using open-source RTL implementations, and found that version numbers can also be calculated from on-chip state.

We evaluate the overhead of MgX in the context of secure DNN accelerators using ChaiDNN [53], an open-source DNN accelerator from Xilinx, as the baseline. The experimental results show that MgX can provide memory encryption and integrity verification with almost no overhead in both performance and off-chip memory traffic. On the other hand, applying the existing general-purpose protection schemes lead to 20-30% overhead and even higher overhead with lower memory bandwidth. MgX also reduces the on-chip area overhead of the traditional memory protection schemes as it does not require any caches for version numbers (VNs) and MACs.

This paper makes the following major contributions:

- We propose MgX, a near-zero overhead memory protection scheme for accelerators. MgX minimizes the performance overhead of memory protection by assigning counter values for data and performing coarse-grained memory protection.
- We demonstrate the applicability of MgX by showing a concrete implementation of MgX for DNN, and detailed analyses of an H.264 video decoder and a genome assembly accelerator.
- We evaluate the secure DNN accelerator with MgX and show that the overhead is less than 1% for both DNN inference and training on the state-of-the-art models.
text, respectively. The AES encryption can be formulated as follows, where $\| \|$ represents bit-wise concatenation.

$$V = U \oplus AES_{ENC}(PA||VN)$$ (1)

Because a general-purpose processor can have an arbitrary memory access pattern that depends on the program that is executing, the version number for each data block, which represents the number of writes to that block, can be any value at a given time. As a result, a general-purpose secure processor typically needs to store the version numbers in memory along with encrypted data in order to determine the correct version number for a later read. Moreover, to avoid re-using the same counter value, the AES key needs to change once the version number reaches its maximum, which implies that the size of the version number needs to be large enough to avoid frequent re-encryption. For example, the memory encryption engine in Intel SGX [18] uses a 56-bit version number per each 64-byte data block, which introduces 11% storage and bandwidth overhead. In general, the version numbers cannot fit on-chip and are stored in DRAM.

2.1.2 Integrity Verification

To prevent off-chip data from being altered by an attacker, integrity verification cryptographically checks if the value from the off-chip memory is the most recent value written to the address by the processor. For this purpose, a MAC of the data value, the memory address, and the version number can be computed and stored for each data block on a write, and checked on a read from DRAM. However, only checking the MAC cannot guarantee the freshness of the data; a replay attack can replace the data and the corresponding VN and MAC in DRAM with stale values without being detected. In order to defeat the replay attack, a Merkle tree (i.e., hash tree) [16] needs to be used to verify the MACs hierarchically in a way that the root of the tree is stored on-chip. As shown in Figure 2(a), a state-of-the-art method [43] uses a Merkle tree to protect the integrity of the version numbers in memory, and includes a VN in a MAC to ensure the freshness of data. Previous works propose to use HMAC-SHA-1 [43], Carter-Wegman MAC [18], and AES-GCM [11] as the hash function. Let us denote the key for hash function, plaintext, and ciphertext as $k_{HV}, U, V$, respectively. The MAC of a data block can be calculated as:

$$MAC = H_{k_{HV}}(V, PA||VN)$$ (2)

The overhead of integrity verification is nontrivial as it requires traversing the tree stored in the off-chip memory. To mitigate this overhead, integrity verification engines typically use a cache to store recently verified MACs.

2.2 Intuition

The main overhead of traditional memory encryption and integrity verification comes from storing and accessing the VNs and MACs in the off-chip memory. Hardware accelerators, especially the memory-intensive ones such as video encoding/decoding, neural network, and DNA sequencing accelerators, often requires accessing a large amount of data in memory. Naïvely applying the traditional general-purpose memory protection scheme to those accelerators can lead to non-trivial performance overhead.

2.3 MgX Scheme

MgX provides application-specific memory protection by matching the access granularity of an accelerator and generating VN in DRAM with stale values without being detected. In that sense, an accelerator’s memory access pattern can often be encoded in a small amount of memory and the on-chip state of the accelerator contains most of the information needed to determine off-chip access patterns. This implies that an accelerator itself can often determine version numbers without off-chip memory.

In addition to coarser memory access granularity, accelerators also tend to have simpler memory access patterns compared to typical programs on CPUs. Control-intensive applications are often not a great fit for hardware acceleration, and the on-chip control unit of an accelerator needs to manage data movements between on-chip and off-chip memory. In MgX, memory protection can be reduced significantly if a version number is allocated per object instead of per cache block.

We propose to leverage these observations to optimize off-chip memory protection by increasing the granularity of protection to match the data movement granularity and version numbers from the on-chip state instead of storing them in memory. In other words, an accelerator or its designer needs to choose the protection granularity and provide version numbers to a memory protection unit. We call this memory protection scheme as MgX. If version numbers can be efficiently determined using on-chip state at run-time, they no longer need to be stored in DRAM, which also makes the Merkle tree unnecessary. The performance overhead of the memory encryption and integrity verification in MgX is largely removed as they require no off-chip memory accesses for the VNs and MACs for the VNs. The only extra memory accesses come from reading and writing the MACs for verifying the integrity of data blocks. We can also lower the MAC overhead by applying MACs at an object granularity, where a MAC is calculated for each memory object that an accelerator reads/writes at a time. In this way, the memory encryption and integrity verification can be performed with almost zero overhead.
is modified to choose the protection granularity and generate a VN when it issues a memory request. Instead of storing the VNs in the off-chip memory, the version number generator, as depicted in Figure 2, holds the MgX state in an on-chip memory and produces the VNs of objects based on the MgX state, the on-chip accelerator state, and the object identifier of each object. The size of the on-chip state depends on the memory access pattern of the accelerator and the number of objects existing in the application. The VN generator consists of two main functions — version generation (getVN) and state update functions (updateS). For memory read and write operations, getVN calculates the version number of an object based on the object identifier (IDobj), the on-chip accelerator state (Sxcel), and the on-chip MgX state (SMgx).

\[ \text{VNID}_{\text{obj}} = \text{getVN}(\text{SMgx}, \text{Sxcel}, \text{ID}_{\text{obj}}) \]  

The state update function is called when the on-chip state needs to be updated. The on-chip state is updated based on the current MgX and accelerator states.

\[ \text{updateS}(\text{SMgx}, \text{Sxcel}) \]  

As shown in Figure 2(b), once the VN for reading/writing an object is generated, the Enc and IV engines can encrypt, decrypt, and verify that object using the same equations in (1) and (2). The Enc and IV engines in MgX use standard AES counter-mode and keyed hash. As the VNs are generated on-chip and do not need to be verified, the MgX scheme does not need the Merkle tree in the off-chip memory. For security and correctness, the version number generation must satisfy the following requirements.

- **security**: The generated version number must be different for each write to a particular memory address.
- **correctness**: The generated version number for a read must match the value used for the most recent write to the same address, a requirement for correct decryption.

Note that sharing a version number among multiple memory locations does not sacrifice security as the counter value to a block cipher (counter value) in the counter mode already includes a memory address in addition to a version number. Also, note that generating version numbers in MgX does not require static memory access patterns. Reads do not affect the version number no matter how irregular they are. Writes can also happen in an arbitrary order using one version number as long as they occur once per each address. Skipping writes and only using a portion of an object can also be done with one version number per object as long as the skipped locations do not need to be read later. Finally, the version numbers can be stored on-chip as long as they fit.

### 2.4 Security Analysis

**Encryption** — MgX uses the same AES counter-mode encryption that is used by the traditional memory encryption scheme for processors. The only difference between MgX and the traditional scheme is that the version number in MgX is determined on-chip instead of being stored in off-chip memory. As long as the version number generator guarantees that the version number is unique for each write to a given memory location (security requirement), the counter value, which is a concatenation of the memory address and the version number, is different for each encryption. Therefore, the security of the memory encryption in MgX can be reduced to the AES counter-mode encryption, which is one of the secure approved modes of operation [10, 34].

**Integrity Verification** — MgX uses a stateful MAC to protect the integrity of data in memory. The MAC includes the address and the version number in addition to data as shown in Equation (2). This MAC construction is identical to the one that is used in the traditional integrity verification scheme (shown in Figure 2(a)), and protects against replay, relocation, and substitution attacks [39], as long as the version numbers are unique for each write to a location. In the traditional scheme, the version numbers need to be protected separately using a Merkle tree because they are stored in off-chip memory. In MgX, security requirement ensures that the counter value is unique for each memory write. Also, because version numbers are generated on-chip, they cannot be directly tampered by an attacker. Thus, the integrity protection in MgX can be reduced to that of the chosen keyed hash function.

### 3. MgX for DNN Acceleration

This section introduces the background on DNNs and discusses how MgX can be applied to enable efficient memory encryption and integrity verification for secure DNN computation in an untrusted environment.

#### 3.1 DNN Basics

DNNs mainly consist of six types of layers: convolutional (conv), dense, normalization, activation, and pooling layers. A DNN typically performs the normalization and activation operations after each conv/dense layer followed by an optional pooling operation. These four operations are often merged and performed together in a DNN accelerator for efficiency. Thus, in the context of off-chip memory protection, we only consider the conv and dense layers in DNNs.

**Inference** — The DNN inference is usually executed in a layer-by-layer fashion, where each layer takes either an external input (e.g., the first layer) or input features generated by the previous layer(s) to produce output features for the subsequent layer(s). For each conv/dense layer, the DNN accelerator fetches the input features (\(x\)) and weights (\(w\)) from the off-chip DRAM, generates the output features (\(y\)) by computing \(y = w \ast x\), and stores the output features back to DRAM. The DNN inference finishes after executing the last layer and generates a prediction for the given input.

**Training** — One iteration of the DNN training consists of a forward propagation and a backpropagation. The forward pass is essentially the same as the inference except that the DNN training requires computing the loss with respect to the ground truth label. After the loss is calculated, it is propagated in a backward manner through the entire network. For each layer, the DNN accelerator fetches the gradients from the subsequent layer (\(g_{\text{out}}\)), input features (\(x\)), and weights (\(w\)) from the off-chip DRAM, computes the gradients toward the input features (\(g_{\text{in}} = g_{\text{out}} \ast x\)) and weights (\(g_{\text{w}} = g_{\text{out}} \ast w\)), updates the weights using the calculated gradients toward the weights (\(w += -\alpha \cdot g_{\text{w}}\), where \(\alpha\) is the learning rate), and stores the gradients toward the input features back to the DRAM.
The gradients toward the inputs ($g_i$) are used as the output gradients for the previous layer. The backpropagation continues until reaching the first layer of the network.

**Static and Dynamic Pruning** — Many pruning techniques have been proposed to reduce the computational cost of DNNs while maintaining their accuracy. Most previous techniques prune a network by removing the features or weights statically [20, 22, 33, 37]. As the static pruning approaches are agnostic to input data at run time, the memory access pattern remains static for any given input. A more recent line of research is investigating dynamic pruning [3, 5, 25, 26, 41, 42], which skips redundant computations, features, and weights dynamically at run time. As dynamic pruning exploits input-specific characteristics, the memory access pattern may vary for a different input. However, the variations are still limited: dynamic pruning may skip some of the accesses that exist statically in the network model; but it does not introduce accesses that do not exist in the model.

### 3.2 Threat Model

The goal of a secure DNN accelerator is to protect the confidentiality and the integrity of a DNN execution in an environment where only the DNN accelerator itself can be trusted. For confidentiality, the secure DNN accelerator aims to protect inputs, outputs, training data, weights, and all intermediate results. The network architecture of a DNN model, however, is considered to be public. Following the typical threat model for secure processors, we assume that the internal operations and state of an accelerator cannot be directly observed or modified by an adversary through physical attacks whereas anything outside of the accelerator including off-chip memory and a host processor are assumed untrusted.

We do not consider other physical side-channel attacks such as the power and EM side channels. However, we believe that accurately recovering input/output values or network parameters such as weights through physical side channels will be far more difficult compared to the attacks on small cryptographic keys. We also do not consider adversarial machine learning attacks that exploit weaknesses in a model itself. However, a secure DNN accelerator can encrypt its outputs so that only a particular user can decrypt them.

### 3.3 High-Level Architecture

Figure 4 illustrates the high-level architecture of a secure DNN accelerator. As off-chip DRAM is untrusted, the secure accelerator requires a memory protection unit to encrypt confidential data stored in DRAM and detect unauthorized changes in values stored in external memory.

Because the interface to the secure accelerator cannot be trusted, the accelerator needs to provide support for a remote user to establish trust and securely communicate with the accelerator. For this purpose, the secure accelerator includes a unique private key, embedded by a manufacturer. We assume that a user obtains the corresponding public key using a private key infrastructure as in Intel SGX or Trusted Platform Modules (TPMs). The following commands are provided by the secure accelerator:

- **Initialization.** The accelerator clears its internal state, sets a pair of new symmetric keys for encryption and integrity verification, enables protection mechanisms, and establishes a secure (encrypted and authenticated) communication channel with a user using a standard protocol such as an SSL.
- **Remote Attestation.** The accelerator supports remote attestation so that the user can verify the identity and the state including firmware of the accelerator. The attestation also allows a user to verify the hash of DNN definition and the hash of the weights.
- **Load Model.** A user sends a DNN definition (e.g., prototxt file in Caffe) and weights through the encrypted channel. The accelerator loads the model by decrypting it with the communication key, and placing it in protected memory that is encrypted with the memory encryption key.
- **DNN Inference and Training.** The user sends inference/training data through an encrypted communication channel. The accelerator runs inference/training using the DNN model on it, and returns the prediction results/learned weights encrypted.

### 3.4 MgX Scheme for DNN Accelerator

In a DNN accelerator, weights and feature maps can be treated as objects. Knowing the object identifier of the weights and features and the MgX state including the DNN model number (CTR$_W$) and the input number (CTR$_I$) are sufficient for constructing the counter values efficiently. CTR$_W$ is incremented when a new model is loaded. CTR$_I$ is incremented for each new input. This section shows how MgX can be applied to both the inference and training of DNNs with and without pruning.

#### 3.4.1 CNN Inference

The computation of a CNN can be represented as a dataflow graph, where each layer in the network is a vertex and the input/output features and the weights of a layer are edges. Each edge in the graph represents a multidimensional tensor of features and weights. More specifically, we show two representative subgraphs that are widely used in modern DNNs — the plain feedforward networks such as AlexNet [30] and VGG [47] and networks with a bypass path such as ResNet [21] and DenseNet [27]. As discussed in Section 3.1, the input and output features and weights are usually stored in DRAM as the on-chip storage of a DNN accelerator is not large enough. To compute a layer during CNN inference, the accelerator reads the input features from the

![Secure DNN Accelerator](image-url)
Figure 5: The subgraph of two popular networks and the associated timing diagrams — A vertex (v) represents a layer and an edge (f) represents the input or output features of a layer. Each column of the timing diagram represents a time slot scheduled for executing a certain vertex (layer) and each row shows the memory operations on an feature edge. W, R, —, and empty slot stand for memory write, memory read, no memory operations but the edge exists in DRAM, and the edge does not exist in DRAM, respectively. The subscript of a feature edge is the vertex ID.

The weights of a DNN model are stored in the off-chip memory, performs the computation in a layer, and writes the output features to the off-chip memory, regardless of its micro-architecture details and data reuse strategies. The output features are written by a preceding layer and are read as the input features by the following layer. In Figure 5 we show the subgraphs and the corresponding timing diagrams of a valid scheduling of the two popular network structures.

The weights of a DNN model are stored in the off-chip memory and read-only during the entire execution. Therefore, we can use a constant as the version number for all weights until they are updated. As different DNN models can be loaded on the secure accelerator, we add CTRW in the on-chip MgX state to keep track of the version number of the model. Then, CTRW serves as the version number of weights.

The output features in memory are updated after each layer of a DNN model, and their version number needs to increase for each write. We assign each vertex in the data-flow graph with one fixed positive integer identifier (viD ∈ ℤ+). In the case where some vertices write to DRAM more than once (e.g., the partial results of the vertex are written back to the off-chip memory), we assign k viD to the vertex, where k is the number of times the vertex writes to DRAM. Then, the outgoing feature edge of a vertex (i.e., output features of a layer) can use the viD as its version number during a single execution. For example, in Figure 5 the subscript of each edge indicates its viD. If the feature maps are written once at the end of each layer, viD corresponds to the layer number. Therefore, the CNN inference needs L unique values for the viD, where L is the number of vertices in the graph (i.e., the number of layers in the CNN). The version number cannot be reused across multiple executions. For this purpose, we also add the total number of inputs (CTRf) received by the secure accelerator to the MgX state, and include that in version numbers.

Based on the above observations, the MgX algorithm for the CNN inference is shown in Algorithm 1. For the CNN inference, the weights and the feature maps are considered as MgX objects. The MgX state consists of CTRf and CTRW. For simplicity, the algorithm shows two separate getVN functions for weights (getVNw(()) and feature maps (getVNF(()) instead of passing IDobj as an argument, and also shows two

**Algorithm 1:** The getVN and updateS functions for CNN inference and training.

```c
1 int getVNw(SMgX) { return SMgX.CTRW; }
2 int getVNF(SMgX, viD) { return (SMgX.CTRF || viD); }
3 void updateSf(SMgX) { SMgX.CTRF++; }
4 void updateSw(SMgX) { SMgX.CTRW++; }
```

Figure 6: The subgraph of a feedforward network and the associated timing diagrams for training.

updateS functions for CTRf and CTRW. updateSf is called when there is a new input. updateSw is called when a new model (weights) is loaded. getVNw simply returns CTRW. getVNF returns the concatenation of CTRf and viD (|| represents bitwise concatenation). viD is passed as a part of the accelerator state.

Note that the version numbers for a CNN do not need to be stored in the off-chip memory; viD is obtained from the on-chip CNN state. CTRf and CTRW can be kept in on-chip registers. As only a small number of registers are needed, they can easily be made to be large enough to avoid overflows. CNNs with less than 256 layers will only require 8 bits for viD. For 64-bit version numbers, the secure accelerator can run $2^{32}$ different inputs before changing its AES key.

**Algorithm 2:** The DNN inference pseudo-code with MgX—

```c
object.ptr and object.size return the pointer and the size of an object, respectively. STMgX(obj, ptr, size, VN) encrypts the object with VN and stores the object in the memory region (ptr, ptr+size). LDmgX(ptr, size, VN) reads the object from the memory region (ptr, ptr+size) and decrypts it with VN.

```c
Input : input features $x_l$ and weights $w_l$ of layer $l$
Output : output feature $x_{l+1}$ of layer $l$
8 updateSf(SMgX);
9 for $l = 1; l \leq L; l++$ do
10 $w_l = LDmgX(w_l, ptr, w_l, size, getVNw(SMgX));$
11 $x_l = LDmgX(x_l, ptr, x_l, size, getVNF(SMgX, l));$
12 $x_{l+1} = RelU(w_l * x_l);$
13 $STMgX(x_{l+1}, x_{l+1}, ptr, x_{l+1}, size, getVNF(SMgX, l + 1));$
end
```

### 3.4.2 CNN Training

One iteration of training consists of a forward propagation and a backpropagation. The forward propagation is the same as the inference except that all features are required for computing the gradients with respect to the weights during the backpropagation. Therefore, we focus on the version number assignments for the gradients and weights during the backpropagation. In Figure 6 we illustrate the data-flow
graph and the associated timing diagram of the backpropagation. During backpropagation, each vertex first computes the gradients flowing to the previous vertex using the gradients flowing to current vertex and the associated weights (e.g., $g_1 = g_2 \cdot w_c$). Then, the associated weights are updated using the gradients flowing to current vertex and the saved features (e.g., $w_c^i = w_c - \alpha \cdot g_2 \cdot f_2$). There is a corresponding gradient edge for each feature edge during the backpropagation. Similar to the features in the forward propagation, the gradients are usually written once and read multiple times.

Based on the memory access pattern of CNN training, we propose the version generation algorithm: Each vertex in the data-flow graph owns one fixed integer vertex identifier (vID). As all features are read-only during the backpropagation, we still assign the vID of as the version number for the outgoing feature edges of a vertex. Similarly, the corresponding gradient edge (g) of each feature edge (f) uses the same version number. Each feature and gradient objects pair can use the same version number as they are stored in different memory locations in DRAM.

Similar to the inference, we combine vID and CTR_W as the version number for the features and gradients, where CTR_W represents the total number of executed training iterations and is incremented when the secure accelerator starts a new iteration. The weights still use CTR_W as the version number as all weights are updated/written the same number of times. CTR_W is used to track the number of updates to the weights. The MgX state consists of CTR_I and CTR_W. vID is assigned to new input is received or the weights are updated. The getVN and updateS functions remain the same as CNN inference in Algorithm 1.

### 3.4.3 RNN Inference and Training

The data-flow graph of RNNs contains a feedback loop. However, as depicted in Figure 7, an RNN with a feedback loop can be unrolled (or unfolded) into a feedforward network, where the feedback loop is unfolded to a sequence of a finite number of vertices (layers). After unrolling, the RNN inference is similar to the CNN inference in Figure 5 except that the number of inputs and outputs in RNNs can be greater than one. As the input and output features remain the same as CNNs, we can apply the same MgX algorithm for RNN inference.

As there may be many outputs in an RNN, the backpropagation of an RNN can be viewed as repeating the backpropagation of a CNN many times. Specifically, the loss of a RNN can be written as the sum of the losses for each output ($L(W, \hat{y}) = \sum_i -y_i \log \hat{y}_i$), where $y_i$ and $\hat{y}_i$ are the output and the ground-truth of the vertex $i$. The loss of each output should be back-propagated to the vertices before this output. Thus, the version generation algorithm can be extended to handle the RNN training.

### 3.4.4 Static and Dynamic Pruning

| Pruning Technique | CSR/CSC | RLC | Channel Pruning |
|-------------------|---------|-----|----------------|
| min. # of accesses (10^3) | 1936 | 1322 | 1796 |
| max. # of accesses (10^3) | 2239 | 1426 | 1827 |

Static pruning approaches still result in a static network model. The same version generation approach can be applied to the pruned model to determine the version numbers. Therefore, MgX is applicable to the statically pruned DNN models. At a glance, it may appear that the MgX scheme does not work for dynamic pruning, which skips memory accesses for some features and weights at run time. However, skipping version numbers does not affect the security of memory encryption or integrity verification as long as the version numbers are not reused. The decryption and integrity verification will also be functionally correct as long as a write and the corresponding reads use the same version number.

To verify the functionality of applying MgX on networks with both static and dynamic pruning, we implemented a variety of pruning techniques in PyTorch and emulated the MgX encryption in software using the proposed version generation approach. The PyTorch implementation follows the same data movement strategies in DNN accelerators where the partial results of features are kept on-chip to maximize the locality and the final results of features are stored in the off-chip memory. For pixel-level dynamic pruning, we implemented different zero compression techniques such as Compressed Sparse Row (CSR) [4], Compressed Sparse Column (CSC) [20, 51], and Run-Length Compression (RLC) [7, 41]. We also tested a threshold-based channel-level dynamic pruning scheme similar to [15], where the entire feature channel is pruned if over 90% of the features are zero. Algorithm 4 shows the pseudo-code of a DNN layer with dynamic pixel-level pruning, where the feature objects are stored in CSR format. The size of the feature object is input-dependent and only determined at run time. The feature object consists of three data structures — value ($V_x$), row pointer ($R_x$), and column index ($C_x$). $V_x$, $R_x$, and $C_x$ all share the version number of the corresponding feature object. The pseudo-code shows that the version numbers of the sparse features in CSR format only depend on the layer number and the MgX state even though memory accesses are dynamically determined.

### 3.5 Hardware Implementation

Compared to the traditional memory protection scheme, which requires an on-chip version number cache to reduce the number of off-chip version number accesses, MgX requires much less on-chip hardware resources. In addition to the encryption and integrity verification engine, MgX only needs two on-chip registers to store CTR_I and CTR_W. The value of the vID is the layer ID, which can be extracted from the on-chip control unit state. CTR_I is incremented when receiving new inference or training data. CTR_W is incremented when loading a new model during inference or updating the weights during training. The integrity verification engine can be programmed to calculate the MAC of the features and weights at the granularity of $k$ bytes, where $k$ is the maximum number of bytes that can be operated in parallel.
**Algorithm 3**: The pseudo-code of a DNN layer \( l \) with dynamic pixel-leveling pruning using compressed sparse row format. \( m, l, i, / \) are the DNN model number, the input number, and the layer number, respectively. To simplify the code, we only show the inner loops for computing one output channel. \( \text{SpVV} \) is the sparse vector vector product operation. \( \text{LD}_{MgX} \) and \( \text{ST}_{MgX} \) are defined in Algorithm 2.

```
Input : input feature \( x \) with \( c_{l} \) channels, weight kernel \( w \) with \( c_{l} \) channels, row pointer of \( c_{l} \) feature channels \( p_{l} \), column index of \( c_{l} \) feature channels \( i_{c} \), and \( M_{GX} \equiv m \times l \).
Output : one channel of the output feature \( x_{i+1} \)

for \( j = 0; j < c_{l}; j++ \) do
    \( w = \text{LD}_{MgX}(w_{j}.ptr, w_{j}.size, \text{getVN}_{w}(M_{GX})) \);
    \( V_{c} = \text{LD}_{MgX}(x_{i}[j].ptr, x_{i}[j].size, \text{getVN}_{F}(M_{GX}, l)) \);
    \( R_{c} = \text{LD}_{MgX}(p_{c}[l].ptr, p_{c}[l].size, \text{getVN}_{F}(M_{GX}, l)) \);
    \( C_{c} = \text{LD}_{MgX}(i[c].ptr, i[c].size, \text{getVN}_{F}(M_{GX}, l)) \);
    \( y += \text{SpVV}(V_{c}, R_{c}, C_{c}, w) \);
end

\( x_{i+1} = \text{ReLU}(y) \);

for \( k = 0; k < x_{i}.size, k++ \) do
    if \( x_{i}[k] > 0 \) then
        \( \text{ST}_{MgX}(x_{i+1}[k], x_{i}[k].ptr, l, \text{getVN}_{F}(M_{GX}, l + 1)) \);
end
```

Figure 8: Timing diagram of a conv layer in CHaiDNN, showing double buffering for features and weights.

The common divisor of the number of bytes written to and fetched from the off-chip memory at a time. Because the MACs are checked infrequently at a coarse granularity, we found that MgX is efficient enough even without an on-chip VN and MAC cache to exploit locality.

4. EXPERIMENTAL RESULTS

4.1 Methodology

**DNN Accelerator** — We use a publicly available accelerator from Xilinx to perform an experimental evaluation of MgX and secure DNN acceleration. CHaiDNN [55] is an open-source HLS-based DNN inference accelerator library for Xilinx Zynq UltraScale+ MPSoC devices. This frame-work can execute a complete DNN using a network definition and model in Caffe [28] format, and supports most of popular layer types. The CHaiDNN accelerator relies on parallelism to deliver high throughput. It consists of an array of processing elements (PEs), which utilize double-pumped DSP blocks (i.e. clocked at twice the normal operating frequency) to perform multiply-accumulate operations, and is specifically built for 6-bit/8-bit quantized operands.

To hide the memory access latency for a single batch, CHaiDNN exploits double buffering across several hierarchical levels. Figure 8 illustrates the double buffering in CHaiDNN. At a high level, the memory accesses for both input and output features are decoupled from computations. The accelerator overlaps loading weights for the next block with the computation for the current block. In that sense, the memory latency for loading weights is hidden by the computation latency or vice versa.

For our experiments, we synthesize the CHaiDNN accelerator into RTL using Vivado HLS 2019.1, and use RTL simulations of CHaiDNN combined with cycle-level simulations for DRAM to evaluate performance. For the HLS synthesis, we target a Xilinx UltraScale+ MPSoC device (XCZU9EG-ABX115). In all our experiments, we use the accelerator configuration using 1024 DSPs, generating 16 output feature maps and 32 output pixels in parallel, operating on the 8-bit integer data type, and targeting the frequency of 100/200 MHz for the IP/DSP blocks, respectively. For our chosen device, CHaiDNN allocates 512×2 KB for the input buffers, 288×2 KB for the output buffers, and 128×2 KB for the weight buffers.

To evaluate the performance of the existing memory protection scheme [18, 38, 43, 50] and MgX, we built a cycle-level simulator, as depicted in Figure 9. The simulator models the three main components — accelerator, memory protection, and off-chip memory. The CHaiDNN accelerator which includes the scheduler, on-chip buffer, and compute engine is simulated in a cycle-accurate RTL simulator. The RTL simulator generates computation and memory events with a start time and an event ID, where all parallel events have the same event ID. In addition, the latency of the computation and the address and the type (read or write) for each off-chip memory access are included for the computation and memory events, respectively. Then, the generated events are received by a memory protection simulator in Python. For each memory event, the memory protection simulator sends the original memory requests as well as the additional meta-data accesses required for memory encryption and integrity verification to the DRAMSim2 [44]. The DRAMSim2, which simulates the memory controller and DRAM, takes the memory request from the memory protection simulator and returns the memory latency of each access. Once an event is finished, the start time and the latency of the event are forwarded to a performance evaluation module to calculate the total DNN execution time and the bandwidth overhead of the memory protection schemes.

For MgX, the VNs and MACs of the data are 64-bit. For the baseline protection scheme, we implement a multi-level 8-ary Merkle tree proposed by the recent work [18] to represent the state-of-the-art. Note that this baseline uses version numbers in each level of the Merkle tree instead of only using MACs.
as in the traditional scheme shown in Figure 2(a). The root of the Merkle tree is stored in on-chip whereas the rest of the

![Figure 2](image)

The root of the Merkle tree is stored in on-chip whereas the rest of the tree is stored in DRAM. Following the previous work [18],

![Figure 10](image)

Figure 10: The memory traffic increase of the DNN inference and training on different network models — We use two

64-bit DDR channels for all accelerators. For the baseline protection scheme, we use an 8-ary Merkle tree which covers 128 MB of encrypted memory and a 4-KB fully-associative VN/MAC cache.

The advantage of MgX over the baseline protection scheme. The average memory traffic increase of MgX are 0.8% and 0.2%

for inference and training, respectively. MgX has almost no increase in off-chip memory accesses because it does not require any version numbers to be stored in off-chip memory and also uses each MAC to protect 1-KB data as feature and weight are accessed in the granularity of several KBS.

As discussed in Section 3.5, MgX has the advantage that it requires minimal hardware changes (e.g., no on-chip cache). However, as the baseline protection scheme needs an on-chip cache and a Merkle tree, we further explore different architectural parameters in the baseline protection scheme. Specifically, we choose three different cache sizes (1KB, 4KB, and 8KB) and three different depth of the Merkle tree (four, five, and six). Four-level, five-level, and six-level Merkle tree can cover 128MB, 1GB, and 8GB of memory, respectively.

As depicted in Figure 11(a), increasing the cache size from 1KB (16 entries) to 2KB (32 entries) helps reducing the additional memory traffic. If the VN/MAC cache is too small, the top-level version numbers in the Merkle tree will be evicted before the low-level version numbers since they are accessed less frequently. However, if we further increase the size of the cache, the additional benefit decreases as the spatial locality of most version numbers have already been exploited. Because the DNN accelerator has a largely streaming memory access pattern, there is not much benefit in increasing the VN/MAC cache unless it is big enough to leverage temporal locality across layers. In Figure 11(b), we show the memory traffic increase of the baseline protection scheme as the size of the protected memory varies, which is equivalent to varying the number of levels in the Merkle tree.

For a deeper Merkle tree, more version numbers are accessed for the memory encryption and integrity verification. However, as the version numbers are held in the on-chip

![Figure 11](image)

Figure 11: The impact on the memory traffic increase of the baseline protection scheme with different architectural parameters — We fix the number of DDR channels to be two and choose different sizes for caches and the encrypted memory region (i.e., the number of levels in the Merkle tree).

![Figure 9](image)

The memory traffic increase of the baseline protection scheme with different architectural parameters — We fix the number of DDR channels to be two and choose different sizes for caches and the encrypted memory region (i.e., the number of levels in the Merkle tree).

![Figure 8](image)

The memory traffic increase of the baseline protection scheme with different architectural parameters — We fix the number of DDR channels to be two and choose different sizes for caches and the encrypted memory region (i.e., the number of levels in the Merkle tree).

![Figure 7](image)

The memory traffic increase of the baseline protection scheme with different architectural parameters — We fix the number of DDR channels to be two and choose different sizes for caches and the encrypted memory region (i.e., the number of levels in the Merkle tree).

![Figure 6](image)

The memory traffic increase of the baseline protection scheme with different architectural parameters — We fix the number of DDR channels to be two and choose different sizes for caches and the encrypted memory region (i.e., the number of levels in the Merkle tree).

![Figure 5](image)

The memory traffic increase of the baseline protection scheme with different architectural parameters — We fix the number of DDR channels to be two and choose different sizes for caches and the encrypted memory region (i.e., the number of levels in the Merkle tree).

![Figure 4](image)

The memory traffic increase of the baseline protection scheme with different architectural parameters — We fix the number of DDR channels to be two and choose different sizes for caches and the encrypted memory region (i.e., the number of levels in the Merkle tree).

![Figure 3](image)

The memory traffic increase of the baseline protection scheme with different architectural parameters — We fix the number of DDR channels to be two and choose different sizes for caches and the encrypted memory region (i.e., the number of levels in the Merkle tree).

![Figure 2](image)

The memory traffic increase of the baseline protection scheme with different architectural parameters — We fix the number of DDR channels to be two and choose different sizes for caches and the encrypted memory region (i.e., the number of levels in the Merkle tree).
Table 2: The execution time of the baseline DNN accelerator for inference and training on four different networks — The execution time is reported in milliseconds.

| # of DDR Channels | Network Architecture |
|-------------------|----------------------|
|                   | LeNet                | AlexNet | GoogleNet | ResNet |
| Inf.              | 1 0.208             | 33.723  | 95.184    | 227.151 |
|                   | 2 0.159             | 16.542  | 51.621    | 131.883 |
|                   | 4 0.147             | 14.161  | 46.103    | 118.128 |
| Train.            | 2 0.652             | 66.792  | 214.734   | 535.853 |

Figure 12: The total execution time of the DNN inference and training on different networks models — We use two 64-bit DDR channels for all accelerators. For the baseline protection scheme, we use a four-level 8-ary Merkle tree and a 4KB cache.

For the inference and training, we normalize the execution time of all other accelerators to the execution time of the baseline accelerator with two DDR channels.

Figure 13 shows the impact on the total execution time of the baseline protection scheme with different architectural parameters — We fix the number of DDR channels to two and choose different sizes for caches and the encrypted memory region.

5. APPLICABILITY OF MGX

We believe that MgX is also applicable to other accelerators. For example, linear regression and SVM have regular memory access patterns, similar to a one-layer neural network. In this section, we show a couple of concrete examples to demonstrate the general applicability of MgX.

5.1 H.264 Video Decoder

We studied H.264/AVC video decoding as a potential candidate for MgX memory protection. Figure 15 shows a typical H.264 decoder architecture, which transforms an input bitstream into video frames. The input bitstream is typically encrypted with the standard counter mode [2]. The decoding process outputs different kinds of frames. Whereas I (intra-coded) frames are independent, the P (inter-predicted) frames are calculated using previous frames as a reference. B (bi-directional) frames use later frames as a reference, leading to out-of-order decoding. Therefore, multiple decoded frames are kept in off-chip memory buffers and if needed, are re-read by the inter-prediction stage.

To study how MgX can be applied to a H.264 decoder, we analyzed an open-source implementation [56]. This decoder stores the decoded and reference frames in external memory, and supports the Main H.264 profile, which can have B frames. Figure 16 shows the reference dependencies in an
example sequence of repeated IBPB frames. The decoder writes an output frame to an available buffer in external memory, but writes only once to an address in each frame. When a frame is used as a reference, it is read-only. Thus we can simply use the frame number (F) concatenated with the input bitstream number (CTR_F) as the version number when writing an output frame. CTR_F is a part of the MgX state, and is incremented when a new video bitstream is loaded for decoding.

```c
getVN(S_MgX, F) = { return (S_MgX.CTR_F || F); }
update(S_MgX) = { S_MgX.CTR_F++; }
```

The inter-prediction block can generate the version number for reading previously decoded frames based on the current frame number (F). For the IBPB sequence in Figure 16 a P frame reads only from the last I frame – hence needing to call getVN(S_MgX, F – 2). Note that the frame number represents the display order of the frames, not the order of decoding. For decoding a B frame, frames from both directions are read; the version numbers can be obtained by calling getVN(S_MgX, F – 1) and getVN(S_MgX, F + 1).

We added the MgX encryption to the H.264 decoder and performed an RTL simulation and verified functional correctness. The memory access pattern is illustrated in Figure 17 where there are three frame buffers in memory, one for the currently decoded frame and two for reference frames. The blue dots indicate writes and the pink dots indicate reads. Because the frame number (F) increments after writing each frame, our scheme ensures that a version number is different for each write to a memory location. While not clear from the figure due to a limited resolution, we verified that each location in the output buffer is written only once per frame. The figure also shows that MgX can handle a dynamic and irregular read pattern.

### 5.2 Genome Alignment Accelerators

In this study, we consider off-chip memory protection for Darwin [54], which is an accelerator for genome assembly. While Darwin also relies on a CPU to perform certain initialization operations and control the hardware acceleration, we assume that the CPU and its communications with Darwin are protected separately with a secure computing technology (e.g., Intel SGX) and focus on protecting memory accesses for the accelerators in this discussion.

Figure 19 shows the components and data accesses in Darwin. Darwin consists of two hardware-accelerated parts, D-SOFT and GACT, which use five types of data in off-chip memory: query sequences, reference sequences, a seed-pointer table, a position table, and traceback pointers. For a reference-assisted assembly, the reference sequence, the seed-pointer table, and the position table are loaded (written) into memory once by a CPU, then only read by the accelerators. Therefore, the version number for these three objects can be obtained simply from a counter in the MgX state, which increments on each new genome assembly (CTR_genome).

After initialization, the CPU loads a batch of query sequences into memory and runs D-SOFT and GACT on the accelerator for each query in the batch. Again, the query and reference sequences are only read by the accelerator. Then, as an output, GACT writes traceback pointers sequentially into memory for each query. For the query sequences and traceback pointers, we can keep another counter that increments for each new query batch (CTR_query) in the MgX state, and use (CTR_genome || CTR_query) as the version number.

The GACT part of Darwin is available as open-source. We validated the functional correctness and the security (no reuse of version numbers) for GACT memory accesses through RTL simulation – see Figure 18.
verification by predicting version numbers or using an unverified version numbers speculatively. MgX is built on the previous encryption and integrity verification schemes, but shows that the off-chip version numbers can be completely eliminated for accelerating DNNs.

Side-channel Attacks and Protection — MgX protects the confidentiality and the integrity of off-chip data, but does not prevent side-channel attacks. The DNN accelerator without dynamic pruning has a fixed memory access pattern and execution time, and is secure against memory and timing side channels. However, countermeasures for other side channels will be necessary for secure acceleration if protection against physical side channels is desired.

A variety of side-channel attacks have been shown to work against DNN accelerators. Memory and timing side-channels have been used to infer the underlying network structure of an accelerator with encrypted weights [24,60]. To counter such an attack, ORAM [13,17,48] offer a strong security guarantee for memory access obfuscation with higher overhead. Physical side-channel attacks on DNNs have been also recently exploited. A power side-channel attack has been used to retrieve the input image from a DNN accelerator [55]. Electromagnetic side-channel emanations have been used to recover the entire network topology including weights, albeit on a microcontroller-based inference engine [6].

**Fully Homomorphic Encryption** — MgX provides hardware memory protection for secure accelerators in an untrusted environment. Alternatively, fully homomorphic encryption (FHE) can provide much stronger protection by performing all computations in an encrypted format. Users send encrypted data and receive encrypted results with an expectation that adversaries cannot obtain decrypted data. While fully homomorphic encryption algorithms provide strong cryptographic guarantees without trusting any remote hardware or software, they come with significant performance overhead [9,55]. We believe that the secure accelerator still provides a valuable design point that provides hardware-based security with much lower performance overhead.

7. **CONCLUSION**

In this paper, we propose a novel off-chip memory protection scheme for hardware accelerators, named MgX, with a particular focus on enabling secure DNN acceleration. We discuss the detailed implementation of MgX on DNN accelerators for both inference and training. Our experimental results show that applying MgX only adds less than 1% performance overhead on multiple DNN models.

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