A Computational Model for Tensor Core Units*

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Abstract

To respond to the need of efficient training and inference of deep neural networks, a plethora of domain-specific hardware architectures have been introduced, such as Google Tensor Processing Units and NVIDIA Tensor Cores. A common feature of these architectures is a hardware circuit for efficiently computing a dense matrix multiplication of a given small size.

In order to broaden the class of algorithms that exploit these systems, we propose a computational model, named TCU model, that captures the ability to naively multiply small matrices. We then use the TCU model for designing fast algorithms for linear algebra problems, including dense and sparse matrix multiplication, FFT, integer multiplication, and polynomial evaluation. We finally highlight a relation between the TCU model and the external memory model.

1 Introduction

Deep neural networks are nowadays used in several application domains where big data are available, and have led to breakthroughs, such as reducing word error rates in speech recognition by 30% over traditional approaches [9], and cutting the error rate in an image recognition competition from 26% to 3.5% [10]. The huge data set size, although crucial for improving neural network quality, arises performance issues during network training, as well as inference. To respond to the increasing computational needs, domain-specific hardware architectures have been introduced by several IT firms, such as Google Tensor Processing Units [12], NVIDIA Tensor Cores [20], Intel KNL’s AVX extensions [24], Apple Neural Engine [2], and ARM’s Machine Learning Processor [3] among the others. These compute units have been specifically developed for some deep learning models, such as multilayer perceptrons, convolutional neural networks, and recurrent neural networks.

Although these architectures significantly vary in hardware specifications and architectures, they share hardware circuits for efficiently multiply small and dense matrices of fixed size. Indeed, matrix multiplication is one of the most important computational primitives in deep learning. By using a terminology introduced in [5], we refer to all accelerators supporting hardware dense matrix multiplication as Tensor Core Units (TCUs) (or simply tensor units). By focusing on a specific computational problem, namely matrix multiplication, TCUs exhibit at the same time both high performance and low energy consumption with respect to traditional CPUs or GPUs approaches [12].

TCUs are becoming the mainstream technology for deep learning, with constantly decreasing economic costs and a tighter integration with the main processing unit. Although TCUs were developed for domain-specific problems, it would be interesting and profitable to extend their application domain, for instance by targeting problems from linear algebra, data mining or machine learning (other than deep learning). A similar scenario appeared with the introduction of GPUs: introduced in the 2000s for accelerating computer graphics (in primis, video games), GPUs have been used since then for very different computational problems, like bioinformatics [10], data mining [6], and neural networks [25]. Will TCUs have the same wide impact of GPUs?

The goals of this paper are to present a framework for designing and analyzing efficient algorithms for TCUs, and to expand the class of algorithms that exploit TCUs. We first introduce in Section 3 a computational model for tensor core units, which we call \((m, ℓ)\)-TCU, that captures the main features of tensor units:

1. High performance matrix multiplication.

For a given model parameter \(m \geq 1\), two matri-
ces of size $\sqrt{m} \times \sqrt{m}$ can be multiplied in $O(m)$ time by using the (parallel) hardware circuit in tensor units.

2. Latency cost. The model parameter $\ell$ captures the latency cost for setting up the tensor unit and preparing the input/output operands.

3. Asymmetric behavior. Tensor units can efficiently deal with a left matrix with a large number $n$ of rows (i.e., a tall left matrix). Thus, we let the $(m, \ell)$-TCU to natively multiply a $n \times \sqrt{m}$ matrix for a $\sqrt{m} \times \sqrt{m}$ matrix, without splitting the left matrix into submatrices of size $\sqrt{m} \times \sqrt{m}$.

The multiplication requires $O(n\sqrt{m})$ time and we let $n \geq m$ to be an user defined value.

We recall that the $O(m)$ time for multiplying two $\sqrt{m} \times \sqrt{m}$ matrices is due to the hardware circuit implementation that implement a parallel systolic algorithm, and not to hardware implementations of fast matrix multiplication algorithms.

We will then use in Section 4 the $(m, \ell)$-TCU model for designing and analyzing some algorithms for linear algebra problems, such as dense and sparse matrix multiplication, FFT, integer multiplication, and polynomial evaluation. Our results show that TCUs can be exploited in these computational problems, for which tensor accelerators were not initially designed. Finally in Section 5 we observe that some lower bounds on the I/O complexity in the external memory model [28] translate into lower bounds on the running time in the TCU model.

1.1 Previous results

Tensor Core Units. The literature on tensor core units has mainly focused on architectural issues, see e.g. [12, 30, 23]. Some works, like [18, 21], have investigated the programming model and performance of deep neural networks workloads in the NVIDIA Tensor Cores.

To the best of our knowledge, the only papers that broad the class of algorithms expressible as TCU operations are [26, 8, 7]. The papers [8, 7] design algorithms for scanning and reduction that exploit NVIDIA tensor cores. In [26], it is shown how to speed up FFT by exploiting the half precision multiplication capability of NVIDIA tensor cores. The algorithm in [26] uses the Cooley–Tukey algorithm where FFTs of size 4 are computed using tensor cores, and it is a special case of the TCU algorithm proposed in this paper in Section 4.3. However, no one of the previous works have proposed a formal computational model and investigated the computational complexities of the algorithms.

Matrix multiplication From a practical point of view, the most efficient algorithms for dense matrix multiplication are those based on the definition of matrix multiplication and which require $\Theta(n^{3/2})$ for multiplying two $\sqrt{n} \times \sqrt{n}$ matrices (see e.g. the BLAS library). Nevertheless from a theoretical point of view, several papers have been investigating algorithms requiring $O(n^{\omega/2})$ operations for some $\omega < 3$. The work of Strassen [27] showed that $\omega \leq 2.81$, and then subsequent works have been improving the upper bound on $\omega$, up to the current best result $\omega < 2.3728$ [29, 10].

Related to our paper, there are some other works which tries to solve several computational problems, like triangle listing and sparse matrix multiplication, by using as a black box a fast matrix multiplication algorithm requiring time $O(n^{\omega/2})$ for some $2 \leq \omega \leq 3$. For instance, [3] shows how to list $t$ triangles in a (sparse) graph with $m$ edges in $O(m^{2\omega/(\omega+1)} + m \omega/(\omega+1) + 3\omega/(\omega+1))$ time. The work [11] shows how to compute a sparse matrix multiplication in time $O(\sqrt{mZ^{(\omega-1)/2} + 1})$, where $Z$ is the number of non-zero in the input $\sqrt{n} \times \sqrt{n}$ matrices and $Z$ is the number of non-zero in the output matrix. These algorithms automatically work in the $(m, \ell)$-TCU by replacing the $O(n^{\omega/2})$ running time of fast matrix multiplication in the RAM model, with the $O(n^{\omega/2}/(m+\ell)/m^{\omega/2-1})$ running time in the TCU model (see Theorem 4).

2 Preliminaries

2.1 Technical overview on some TCUs

With the advent of deep learning as the dominant paradigm for artificial intelligence based systems, a plethora of dedicated parallel architectures have been developed for accelerating training and inference phases. We briefly describe the main characteristics of the most relevant ones: Google’s Tensor Processing Unit (TPU) [12] and NVIDIA’s Tensor Cores [20] (TCs). They are used to accelerate convolution layers and the related matrix multiplication operation, which represent the most computationally expensive part of a deep learning applications.

The Tensor Processing Unit (TPU) is a custom application specific integrated circuit developed for accelerating the inference phase of deep neural networks. It is built around 65536 8-bit ALU Matrix Multiply Unit (MMU) and on-chip memory. TPU has been designed as an accelerator to plug into on traditional server as GPUs do through PCIe I/O bus. On the contrary to GPUs, the processor sends the instruction buffer instructions by avoiding the use of a fetch unit inside the TPU. Data are sent from the
CPU host memory to the local TPU memories, named Unified Buffer and Weight Memory, with the goal of offloading all the computation. In combination with a systolic execution model which allows data prefetching from the memory to MMU, this design allows to reduce the overhead and maximize the throughput. Specifically, MMU is composed by 256 \times 256 8-bit multiplier–accumulator units. The 16-bit products are stored in 32-bit Accumulators. The MMU performs 256-element partial sum per clock cycle. Briefly, the typical TPU workflow is summarized as follows:

1. \textit{Read\_Host\_Memory} reads data from the CPU host memory into the Unified Buffer memory.

2. \textit{Read\_Weights} reads elements from Weight Memory into the Weight FIFO to fill in the MMU.

3. \textit{MatrixMultiply} performs a matrix multiplication. This operation takes a variable-sized \( n \times 256 \) input, with \( n < 96K \), multiplies it by a 256 \times 256 constant elements, and produces a \( n \times 256 \) output, taking about \( n \) cycles to complete.

4. \textit{Write\_Host\_Memory} writes data from the TPU (Unit Buffer) to the CPU host memory.

In NVIDIA "Volta" architecture, Tensor Cores extend the traditional GPU architectures and the parallel programming interface (CUDA) by providing dedicated units to efficiently perform dense-matrix multiplication by dense-matrix multiplication. The Volta microarchitecture revised NVIDIA Streaming Multiprocessors (SM) design: the SM consists of 4 processing blocks. Each block contains: 2 Tensor Cores, 8 Floating Point (FP) unit operating at 64-bit, 16 FP operating at 32-bit, 8 Integer Unit operating at 32-bit and one Special Function Unit. Concerning the memory hierarchy, the L1 cache and the shared memory are located in same in-chip surface. The L2 is also included in the same die and it is accessed among multiple SMs. The High Bandwidth Memory (HBM) can be addressed by a 4096-bit memory interface. Tensor Cores allows to perform 64 floating-point Fused-Multiply-Add (FMA) operations in one cycle. FMA operates with one CUDA warp (32 threads). This requires primitives for data loading and the synchronization of the result from/to registers through load and store units. On the contrary to TPUs, which also provide specific units for accelerating other neural networks operations (e.g., Activation Unit), TCs can be used for a generic matrix multiplication.

2.2 Systolic algorithms for matrix multiplication

The circuits which implement matrix multiplication in the Google TPU and in the NVIDIA TC adopt a systolic algorithm for matrix multiplication. A systolic algorithm is an algorithm for a systolic array, that is a network of processing elements (PEs) that rhythmically compute and pass data through the system [17].

For the sake of completeness, we formalize the systolic algorithm implemented in the Google TPU [12]. The implementation on NVIDIA TCs is slightly different but shares the same high level structure, and we refer to [17] for a more complete overview on systolic algorithms. The systolic algorithm is implemented on a 2-dimensional array of \( m \) PEs, and we denote with \( p_{i,j} \) the PE at row \( i \) and column \( j \), for each \( 0 \leq i,j < \sqrt{m} \). Let \( A \) and \( B \) be the two \( \sqrt{m} \times \sqrt{m} \) input matrices, and let \( C = A \cdot B \) be the \( \sqrt{m} \times \sqrt{m} \) output matrix; we denote with \( a_{i,j}, b_{i,j}, c_{i,j} \) the entry in row \( i \) and column \( j \) of \( A, B, C \) respectively; for notational simplicity, we let \( a_{i,j} = 0 \) if \( i,j < 0 \) or \( i,j \geq \sqrt{m} \). The algorithm works as follows (see also Figure 1):

- In the first \( \sqrt{m} \) steps, matrix \( B \) is pushed within the \( m \) PEs so that \( p_{i,j} \) contains \( b_{i,j} \).
- The algorithm then executes \( 2\sqrt{m} \) steps. In each step \( k \), with \( 0 \leq k < 2\sqrt{m} \), each PE \( p_{i,j} \) receives: 1) an entry \( a \) of \( A \) from the left PE \( p_{i-1,j} \) or the input \( a_{k-i,j} \) if \( j = 0 \); 2) a partial sum \( c \) from the top PE \( p_{i,j-1} \), or we set \( c = 0 \) if \( i = 0 \). Then,

![Figure 1: Example of 3x3 systolic array after loading matrix B.](image-url)
each \( p_{i,j} \) computes \( c = c + a \cdot b_{i,j} \) (recall that \( b_{i,j} \) is in the local memory of \( p_{i,j} \)). Finally \( p_{i,j} \) forwards \( a \) to the right PE (\( p_{i,j+1} \), if any) and \( c \) to the bottom PE (\( p_{i+1,j} \) or it is output if \( i = \sqrt{m} - 1 \)).

- We observe that each \( p_{\sqrt{m}-1,j} \) outputs \( c_{i,j} \) at the end of step \( k = \sqrt{m} + i + j \).

We observe that the algorithm can be extended to compute \( C = A \cdot B \) where \( A \) is a \( n \times \sqrt{m} \) matrix and \( B \) is a \( \sqrt{m} \times \sqrt{m} \) matrix, by just continuing pumping all rows within the system. This feature is not available in the NVIDIA implementation since matrix \( B \) does not reside in the local PE memories, but it is percolated within the array as matrix \( A \).

3 The \((m, \ell)\)-TCU model

We propose a computational model for tensor core units that captures the following properties:

- **Matrix acceleration.** The hardware circuits implement a parallel algorithm for multiplying two matrices of a fixed size, and the main cost is dominated by reading/writing the input and output matrices. For a given hardware parameter \( m \), we have that the multiplication of two matrices \( A \) and \( B \) of size \( \sqrt{m} \times \sqrt{m} \) are implemented in time \( O(m) \). With time, we mean the running time as seen by the CPU clock and it should not be confused with the total number of operations executed by the unit, which is always \( O\left(m^{3/2}\right) \).

  Indeed, no existing tensor unit implements fast matrix multiplication algorithms, as for instance Strassen. The matrix multiplication operation is called by an instruction specifying the address (in memory) of the two input matrices and of the output matrix where the result will be stored; data will be loaded/stored by the tensor unit.

- **Latency cost.** A call to the tensor unit has a latency cost. As the state of the art tensor units use systolic algorithms, the first output entry is computed after \( \Omega(\sqrt{m}) \) time. There are also initial costs associated with activation, which can significantly increase when the unit is not connected to the CPU by the internal system bus or is shared with other CPUs. We thus assume that the cost of the multiplication of two matrices of size \( \sqrt{m} \times \sqrt{m} \) is \( O(m + \ell) \), where \( \ell \geq 0 \) is the latency cost.

- **Asymmetric behavior.** As tensor units are designed for improving training and inference in deep networks, the two matrices in the multiplication \( A \times B \) are managed differently. Matrix \( B \) represents the model which we are currently training/using, while rows in matrix \( A \) represent the vectors of \( \sqrt{m} \) entries to be evaluated. As the same model can be applied to \( k \) vectors, with \( n \gg \sqrt{m} \), it is possible to first load the weights in \( B \) and then to stream the \( n \) rows of \( A \) into the tensor unit (possible in chunks of \( \sqrt{m} \) rows), reducing thus latency costs. Thus, we assume in our model that two matrices of size \( n \times \sqrt{m} \) and \( \sqrt{m} \times \sqrt{m} \) can be multiplied in time \( O(n\sqrt{m} + \ell) \), where \( n \geq \sqrt{m} \) is the number of rows and it is a value defined by the programmer.

Following the previous observations, we define the **Tensor Computing Unit (TCU) model** as follows. The \((m, \ell)\)-TCU model is a standard RAM model where the CPU contains a circuit, named tensor unit, for performing a matrix multiplication \( A \times B \) of size \( n \times \sqrt{m} \) and \( \sqrt{m} \times \sqrt{m} \) in time \( O(n\sqrt{m} + \ell) \), where \( m \geq 1 \) and \( \ell \geq 0 \) are two model parameters and \( n \geq \sqrt{m} \) is a value (possibly input dependent) specified by the programmer. The matrix operation is initialized by a (constant size) instruction containing the addresses in memory of the two input matrices \( A \) and \( B \), of the output matrix \( C \), and the row number \( n \) of \( A \). The **running time** (or simply time) of a TCU algorithm is given by the total cost of all operations performed by the CPU, including calls to the tensor units. We assume no concurrency between tensor unit, memory and CPU, and hence at most one component is active at any time. We also assume that each CPU instruction works with operands of one memory word, and that each entry of a matrix in the TCU requires one memory word. Each memory word consists of \( \kappa \) bits (in general, we denote \( \kappa = \Omega(\log n) \) where \( n \) is the input size, that is enough for storing the input size in one word).

3.1 Discussion on the model

As our goal is to understand to which extent algorithms can exploit circuits of fixed size for matrix multiplication, we avoided the modeling of parallel tensor units and the limited numerical precision of tensor units in this work. We also do not directly consider the bandwidth between CPU and TCUs, assuming that one memory word can be transferred in the tensor unit in \( O(1) \) CPU cycles. We now make some considerations on how Google TPUs and NVIDIA TCs fit our model.

In the Google TPU (in the version described in [12]), the right matrix \( B \) has size \( 256 \times 256 \) words (i.e., \( m = 65536 \)). The left matrix \( A \) is stored in the local unified buffer of \( 96k \times 256 \) words; thus, TPUs can compute the product between two matrices of size...
96k×256 and 256×256 in one (tensor) operation. The number of rows of the left matrix in the TCU model is an user defined parameter (potentially a function of the input size); on the other hand, the number of rows of the left matrix in the TPU is user defined but it is upper bounded by a hardware-dependent value (i.e., 96K). Being this bound quite large, a TPU better exploits a tall left matrix than a short one, as in the TCU model. The systolic array works in low precision with 8 bits per word (κ = 8). Although the bandwidth was limited in the first TPU version (16GB/s), it has significantly increased in more recent versions (up to 600 GB/s). Although TPU has a quick response time, the overall latency is high because the right hand matrix has to be suitably encoded via a TensorFlow function before loading it within the TPU: in fact, the programming model in TPUs is strongly integrated with TensorFlow, and it does not allow to use bare matrices as inputs. The high latency cost might mitigate the fact that our model does not capture limited bandwidth.

The programming model of the NVIDIA Volta architecture allows to multiply matrices of size 16 × 16, although the basic hardware unit works on 4 × 4 matrices; we thus have m = 256. Memory words in systolic array have, as in the TPU, a limited precision (κ = 16 bits). TCs exhibit high bandwidth and low latency, as data are provided by a high bandwidth shared with the GPU processing units. Furthermore, both matrices A and B can be loaded within TCs without a special encoding as in TPUs, since the NVIDIA Volta natively provides support for matrix multiplication. Finally we observe that, as TCs are within a GPU, any algorithm for TCs has also to take into account GPU computational bottlenecks (see e.g. [3][4]).

4 Algorithms

4.1 Dense matrix multiplication

A Strassen-like algorithm for matrix multiplication was defined in [4] as a recursive algorithm that utilizes as base case an algorithm \( A \) for multiplying two \( \sqrt{n_0} \times \sqrt{n_0} \) matrices using \( p_0 \) element multiplications and \( O(n_0) \) other operations (i.e., additions and subtractions); we assume \( n_0 = O(p_0) \). Given two \( \sqrt{n} \times \sqrt{n} \) matrices with \( n > n_0 \), a Strassen-like algorithm envisions the two \( \sqrt{n} \times \sqrt{n} \) matrices as two matrices of size \( \sqrt{n_0} \times \sqrt{n_0} \) where each entry is a submatrix of size \( \sqrt{n/n_0} \times \sqrt{n/n_0} \); then, the algorithm recursively computes \( p_0 \) matrix multiplications on the submatrices (i.e., the \( p_0 \) element multiplications in \( A \)) and then performs \( O(n) \) other operations. For each parameters \( p_0 \) and \( n_0 \), the running time of the algorithm is \( T(n) = O(n^{\omega_0}) \), where \( \omega_0 = \log_{p_0} n_0 \).

By setting \( n_0 = 4 \) and \( p_0 = 8 \), we get the standard matrix multiplication algorithm (\( \omega_0 = 3/2 \)), while with \( n_0 = 4 \) and \( p_0 = 7 \) we get the Strassen algorithm (\( \omega_0 = log_4 7 \approx 1.403 \)). Any fast matrix multiplication algorithm can be converted into a Strassen-like algorithm [22].

The TCU model can be exploited in Strassen-like algorithms by ending the recursion as soon as a sub-problem fits the tensor unit: when \( n \leq m \), the two input matrices are loaded in the tensor unit and the multiplication is computed in \( O(m) \) time. For simplicity, we assume \( m \geq n_0 \) (otherwise the tensor unit would not be used) and we get the following result.

**Theorem 1.** Given a Strassen-like algorithm with parameters \( n_0 \) and \( p_0 \), then there exists a TCU algorithm that multiplies two \( n \times n \) matrices on an \( (m, \ell) \)-TCU model, with \( m \geq n_0 \), in time

\[
T(n) = O \left( \frac{n^{\omega_0}}{m^{\omega_0}} (m + \ell) \right).
\]

**Proof.** The running time is given by the following simple recursion:

\[
T(n) = \begin{cases} 
   p_0 T(n/n_0) + O(n) & \text{if } n > m \\
   O(m + \ell) & \text{if } n \leq m
\end{cases}
\]

If we use the standard matrix multiplication algorithm, we get a TCU algorithm with \( O \left( \frac{n^{3/2}}{m^{1/2}} + \frac{n(n/m)^{3/2}}{\ell} \right) \) time. The Strassen algorithm gives a \( O \left( \frac{n^{1.4037}}{m^{0.4037}} + \frac{n(m)^{1.4037}}{m} \right) \) time TCU algorithm.

We now show how to decrease the latency term, i.e., \( \frac{(n/m)^{3/2}}{\ell} \), in the TCU algorithm based on the standard algorithm. The idea is to keep as much as possible the right matrix \( B \) within the tensor unit by using a tall left matrix \( A \). We split the left matrix \( A \) into \( \sqrt{n/m} \) blocks \( A_i \) of size \( \sqrt{n} \times \sqrt{m} \) (i.e., vertical strips of width \( \sqrt{m} \)) and the right matrix \( B \) into square blocks \( B_{i,j} \) of size \( \sqrt{m} \times \sqrt{m} \), with \( 0 \leq i, j < \sqrt{n/m} \). Then, we compute \( C_{i,j} = A_i \cdot B_{i,j} \) for each \( 0 \leq i, j < \sqrt{n/m} \) using the tensor unit in time \( O(n \sqrt{m} + \ell) \). The final matrix \( C \) follows by computing the \( n \times \sqrt{m} \) matrices \( C_i = \sum_{j=0}^{n/m-1} C_{i,j} \).

**Theorem 2.** There exists an algorithm that multiplies two \( n \times n \) matrices in the \( (m, \ell) \)-TCU model in time

\[
T(n) = \Theta \left( \frac{n^{3/2}}{m^{1/2}} + \frac{n}{m} \right).
\]

\(^1\)We observe that \( \omega_0 \) corresponds to \( \omega/2 \), where \( \omega \) is the traditional symbol used for denoting the exponent in fast matrix multiplication algorithms.
If we require all elementary products to be performed in the tensor unit and to use only semiring operations, the above algorithm is optimal.

Proof. The upper bound follows since each multiplication $C_{i,j} = A_i \cdot B_{i,j}$ requires $O(\sqrt{n} \sqrt{m} + \ell)$ time, and there are $n/m$ such terms. The cost of the final summation in negligible.

When using only semiring operations, any algorithm must compute $n^{3/2}$ elementary products. Since each call to a tensor computes $m^{3/2}$ elementary products in $\Theta(m)$ time using a systolic algorithm, we need $\Omega(n^{3/2}/m^{3/2})$ time. Furthermore, since all entries of $B$ must be loaded in the tensor unit at least once and we cannot load more than $m$ entries in $B$ per tensor operation, the algorithm has to load at least $n/m$ distinct right matrices in the tensor unit; then a $\Omega((n/m)^2)$ lower bound on the time also follows.

### 4.2 Sparse matrix multiplication

A TCU algorithm for multiply two sparse matrices follows from the work [11] that uses as a black box a fast matrix multiplication algorithm for multiplying two $\sqrt{n} \times \sqrt{n}$ matrices in $O(n^{3/2})$ time.

Let $I$ be the number of non-zero entries in the input matrices $A$ and $B$, and let $Z$ be the number of non-zero entries in the output $C = A \cdot B$. We consider here the case where the output is balance, that is there are $\Theta(Z/\sqrt{n})$ non-zero entries per row or column in $C$; the more general case where non-zero entries are not balanced is also studied in [11] and can be adapted to TCU with a similar argument. The algorithm in [11] computes the output in time $O(\sqrt{n}Z^{(\omega-1)/2} + I)$ with high probability. The idea is to compress the rows of $A$ and the column of $B$ from $\sqrt{n}$ to $\sqrt{Z}$ using a hash function or another compression algorithm able to build a re-ordering of the matrix $A$. Then the algorithm computes a dense matrix product between a $\sqrt{Z} \times \sqrt{n}$ matrix and a $\sqrt{n} \times \sqrt{Z}$ using the fast matrix multiplication algorithm. Other data structures and techniques are required in the paper and we refer to [11] for more details; however, they do not exploit TCU and do not affect the running time. By replacing the fast matrix multiplication with the result of Theorem [1], we get the following.

**Theorem 3.** Let $A$ and $B$ be two sparse input matrices of size $\sqrt{n} \times \sqrt{n}$ with at most $I$ non-zero entries, and assume that $C = A \cdot B$ has at most $Z$ non-zero entries evenly balanced among rows and columns. Then there exists an algorithm for the $(m,\ell)$-TCU model requiring time:

$$T(n, Z, I) = O\left(\frac{n}{Z} \sqrt{\frac{Z}{m}} \omega (m + \ell) + I\right),$$

when $Z \geq m$ and where $\omega_0 = \log_m p_0$ is the exponent given by a Strassen-like algorithm.

Proof. The claim follows by observing that a multiplication between a matrix of size $\sqrt{Z} \times \sqrt{n}$ and a matrix of size $\sqrt{n} \times \sqrt{Z}$ can be decomposed into $\sqrt{Z} \sqrt{n}$ matrices of size $\sqrt{Z} \times \sqrt{Z}$, and each one can be solved with the algorithm of Theorem [1].

### 4.3 Discrete Fourier Transform

The Discrete Fourier Transform $y$ of a $n$-dimensional (column) vector $x$ can be defined as the matrix-vector product $y = x^T \cdot W$, where $W$ is the Fourier matrix (or DFT matrix) and $T$ denotes the transposes of a matrix/vector. The Fourier matrix $W$ is a symmetric $n \times n$ matrix where the entry at row $r$ and column $c$ is defined as: $W_{r,c} = e^{-2\pi i r c / n}$.

The Cooley–Tukey algorithm is an efficient and recursive algorithm for computing the DFT of a vector. The algorithm arranges $x$ as an $n_1 \times n_2$ matrix $X$ (in row-major order) where $n = n_1 \cdot n_2$; each column $X_{r,c}$ is replaced with its DFT and then each entry $X_{r,c}$ is multiplied by the twiddle factor $w_{r,c}^{i\ell}$; finally, each row $X_{r,*}$ is replaced by its DFT and the DFT of $x$ is given by reading the final matrix $X$ in column major.

For simplicity, we assume that the TCU model can perform operations (e.g., addition, products) on complex numbers; this assumption can be easily removed with a constant slow down in the running time: for instance, the multiplication between $\sqrt{m} \times \sqrt{m}$ complex matrices can be computed with four matrix multiplications and two sums of real values.

To compute the DFT of $x$ using a $(m,\ell)$-TCU, we use the Cooley–Tukey algorithm where we set

$n_1 = \sqrt{m}$ and $n_2 = n/\sqrt{m}$ (we assume all values to be integers). Then, we use the tensor unit for computing the $n_2$ DFTs of size $n_1 = \sqrt{m}$ by computing $X^T \cdot W_{\sqrt{m}}$. Then, we multiply each element in $X$ by its twiddle factor and transpose $X$. Finally, we compute the $n_1$ DFTs of size $n_2$: if $n_2 > \sqrt{m}$, the $n_1$ DFTs are recursively computed; otherwise, if $n_2 \leq \sqrt{m}$, the $n_1$ DFTs are computed with the multiplication $X^T \cdot W_{n_2}$ by using the tensor unit.

**Theorem 4.** The DFT of a vector with $n$ entries can be computed in a $(m,\ell)$-TCU in time

$$T(n) = O((n + \ell) \log_m n).$$

Proof. In each recursive level, we load matrix $B = W_{\sqrt{m}}$ at the beginning and then compute the $n_2$ DFTs of $n_1$ entries by multiplying a $n/\sqrt{m} \times \sqrt{m}$ matrix with $W_{\sqrt{m}}$ in time $O(n + \ell)$. The remaining operations (i.e., matrix transposition and multiplication by
We now study how to multiply two long integers by exploiting batch DFTs. However, the algorithm in [26] does not exploit batch DFTs (i.e., \( n/\sqrt{m} \) DFTs in one tensor operation) as in our algorithm.

### 4.4 Integer multiplication

We now study how to multiply two long integers by exploiting a \((m, \ell)\)-TCU. The input is given by two integers \( a \) and \( b \) of \( n \) bits each (without loss of generality, we assume both integers to be positives and \( n > m \)), and the output is the binary representation of \( c = a \times b \), of size \( 2n - 1 \). For this problem, we introduce in the design a third parameter \( \kappa \), which is the bit length of a memory word that can be managed by a TCU model. We assume that \( \kappa = \Omega(\log n) \), that is there are enough bits in a word to store the input/output size. It is easy to see that the tensor unit can multiply matrices of (positive) integers of \( \kappa' = \kappa/4 \) bits without overflow: the largest integer in the output matrix using \( \kappa' \) bits is \( 2^n \sqrt{m} \) which requires \( 2\kappa' + \log \sqrt{m} < \kappa \) (if \( n >> m \), then \( \kappa' = \kappa/2 - 1 \) suffices).

We initially show how to speed up the long integer multiplication algorithm [15], also known as the schoolbook algorithm, by exploiting the tensor unit. Then, we will use this algorithm to improve the recursive Karatsuba algorithm [13].

Let \( A(x) \) be the following polynomial, with coefficients from \( \mathbb{N} \):

\[
A(x) = \sum_{i=0}^{n'-1} A_i x^i
\]

where \( n' = n/\kappa' \) and \( A_i = (a_{(i+1)\kappa'-1} \ldots a_{i\kappa'})_2 \) is the integer given by the \( i \)th segment of \( \kappa' \) bits of \( a \). Let \( B(x) \) be defined similarly for \( b \). We have that \( a = A(2^{\kappa'}) \) and \( b = B(2^{\kappa'}) \). We define \( C(x) = A(x) \cdot B(x) \) and we observe that \( c \) is given by evaluating \( C(2^{\kappa'}) \). Note that \( A(X) \) and \( B(X) \) have degree \( n' - 1 \), while \( c \) has degree at most \( (2n-1)/\kappa' \leq 2n' - 1 \).

The coefficients of \( C \) can be evaluated with the matrix multiplication \( C = A \cdot B \) where: 1) \( B \) is the column vector with the \( n' \) coefficients of \( B(X) \); 2) \( A \) is a \((2n'-1) \times n' \) matrix where \( A_{i,j} = A_{n'-i+j-1} \) and we assume that \( A_{i,j} = 0 \) if \( h < 0 \) or \( h \geq n' \).

The product \( C = A \cdot B \) cannot exploit TCU since \( B \) is a vector. To fully exploit an \((m, \ell)\)-TCU, we show how to calculate \( C \) coefficients via the multiplication \( C' = A' \cdot B' \) where \( A \) is a \((n'+\sqrt{m} - 1) \times \sqrt{m} \) matrix and \( B \) is a \( \sqrt{m} \times n'/\sqrt{m} \) matrix.

- Matrix \( B' \) follows by considering vector \( B \) as the column major representation of a \( \sqrt{m} \times n'/\sqrt{m} \) matrix, that is \( B'_{i,j} = B_{n'-i-j\sqrt{m}-1} \).

- Matrix \( A' \) is given by considering all segments (starting from the rightmost) of length \( \sqrt{m} \) in the sequence \( 0_\sqrt{m}, A_0, A_1, \ldots A_{n'-1}, 0_\sqrt{m} \), where \( 0_\sqrt{m} \) denotes a sequence of \( \sqrt{m} - 1 \) zeros. More formally, the \( i \)th row \( A'_{i,s} \) is \( [A_{n'-i-1}, A_{n'-i-2}, \ldots A_{n'-i-\sqrt{m}}] \), where we assume again that \( A_{i,j} = 0 \) if \( h < 0 \) or \( h \geq n' \).

Then, we compute \( C' = A' \cdot B' \) with the algorithm for dense matrix multiplication of Theorem 2 (or equivalently the algorithms of Theorem 1): We decompose \( B' \) into \( n'/m \) submatrices of size \( \sqrt{m} \times \sqrt{m} \) and then compute \( n'/m \) products of a \((n'+\sqrt{m} - 1) \times \sqrt{m} \) matrix with a \( \sqrt{m} \times \sqrt{m} \) matrix. Finally, the coefficient of the \( x^h \) indeterminate in \( C(x) \), for each \( 0 \leq h < 2n' - 1 \), follows by summing all entries in \( C'_{i,j} \) such that \( h = 2(n'-1) - i - j \sqrt{m} \). Finally we compute \( c = C(2^{\kappa'}) \).

**Theorem 5.** Two integers of \( n \) bits can be multiplied in a \((m, \ell)\)-TCU with \( \kappa \) bits operations in time

\[
T(n) = O \left( \frac{n^2}{\kappa^2 \sqrt{m}} + \frac{n}{\kappa m} \ell \right).
\]

**Proof.** Let \( C_h \) be the coefficient of \( C(x) \) of \( x^h \) indeterminate. We have:

\[
C_h = \sum_{i,j | i+j = h} a_i b_j = \sum_{p=0}^{h/\sqrt{m}} \sum_{i=h-(p+1)\sqrt{m}+1} a_i b_{h-i}
\]

where as usual \( a_i = 0 \) and \( b_j = 0 \) if \( i < 0 \) or \( i \geq n' \). By definition of matrices \( A' \) and \( B' \), we can rewrite
the previous equation as:
\[ C_h = \sum_{p=0}^{[h/\sqrt{m}]} A'_{n'-h+p\sqrt{m}-1,*} B'_{*,(n'-1)/\sqrt{m}-p} \]  
\[ = \sum_{p=0}^{[h/\sqrt{m}]} C'_{n'-h+p\sqrt{m}-1,(n'-1)/\sqrt{m}-p} \]
We observe that the last sum is including all entries in \( C_{i,j} \) where \( h = 2(n'-1) - i - j\sqrt{m} \), as required in the algorithm. The algorithm then correctly computes all \( C_h \) coefficients and hence \( c = a \cdot b \).

We now consider the running time. The cost of the matrix multiplication \( C' = A' \cdot B' \) is \( O\left(\frac{n^2}{\sqrt{m}}(n'\sqrt{m} + \ell)\right) \). The cost of computing the \( C_h \) coefficients and the final evaluation is upper bounded by \( O(n'\sqrt{m}) \). The claim follows.

The Karatsuba algorithm is a well-known algorithm that computes \( c = a \cdot b \) by recursively computing three integer multiplications of size \( n/2 \) and then combining the solution in \( O(n/\kappa) \) time. If we stop the recursion as soon as the input size is \( n \leq k\sqrt{m} \) and solve the subproblem with the algorithm of Theorem 5, we get the following result.

**Theorem 6.** Two integers of \( n \) bits can be multiplied in a \((m,\ell)\)-TCU with \( \kappa \) bits operations in time
\[ T(n) = O\left(\left(\frac{n\log^3}{\sqrt{m}} + \frac{\ell}{\sqrt{m}}\right)\right). \]

**Proof.** The running time follows by the recurrence:
\[ T(n) = \begin{cases} 
3T(n/2) + O(n/\kappa) & \text{if } n > k\sqrt{m} \\
O(\sqrt{m} + \ell/\sqrt{m}) & \text{if } n \leq k\sqrt{m}
\end{cases} \]

### 4.5 Batch polynomial evaluation

We now show how to exploit the TCU for evaluating a given polynomial of \( A(x) = \sum_{i=0}^{n-1} a_i x^i \) of degree \( n - 1 \) on \( p \) points \( p_i \), with \( 0 \leq i < p \). For simplicity we assume \( n \) to be a multiple of \( \sqrt{m} \), \( p \geq \sqrt{m} \), and that the polynomial can be evaluated without overflow on the memory word available in the TCU model.

We initially compute for each \( p_i \) the powers \( p_i^j \) for each \( j \in \{0, 1, \ldots, \sqrt{m} - 1\} \cup \{k\sqrt{m}, \forall k \in \{1, \ldots, n/\sqrt{m} - 1\}\} \), that is \( p_i^0, p_i^1, \ldots, p_i^{\sqrt{m}-1} \) and \( p_i^{\sqrt{m}}, p_i^{2\sqrt{m}}, \ldots, p_i^{n-\sqrt{m}} \). We define the following matrices:

- A matrix \( A \) of size \( \sqrt{m} \times n/\sqrt{m} \) where \( A_{i,j} = a_{i+j\sqrt{m}} \) for each \( 0 \leq i < \sqrt{m} \) and \( 0 \leq j < n/\sqrt{m} \). Stated differently, we consider the sequence \( a_0, \ldots, a_{n-1} \) as the column major representation of \( A \).

We then compute the product \( C = X \cdot A \) by exploiting the tensor unit. As in the previous section, we decompose \( A \) into \( \sqrt{m} \times \sqrt{m} \) submatrices and then solve \( n/m \) multiplications. Then, for each \( p_i \), the values \( A(p_i) \) follows by the sum \( \sum_{j=0}^{n/\sqrt{m}-1} C_{i,j} p_i^j \sqrt{m} \).

**Theorem 7.** A polynomial of degree \( n - 1 \) can be evaluated on \( p \) points on a \((m,\ell)\)-TCU with \( \kappa \) bits operations in time
\[ T(n,p) = O\left(\frac{pn}{\sqrt{m}} + p\sqrt{m} + \frac{n\ell}{m}\right). \]

**Proof.** The correctness follows by observing that:
\[ \sum_{j=0}^{n/\sqrt{m}-1} C_{i,j} x^j \sqrt{m} = \sum_{j=0}^{n/\sqrt{m}-1} \left( \sum_{k=0}^{\sqrt{m}-1} p_i^k a_{k+j\sqrt{m}} \right) p_i^\sqrt{m} \]
\[ = \sum_{j=0}^{n/\sqrt{m}-1} \sum_{k=0}^{\sqrt{m}-1} p_i^{k+j\sqrt{m}} a_{k+j\sqrt{m}} \]
\[ = \sum_{h=0}^{n-1} a_h p_i^h = A(p_i). \]

The cost of the initial exponentiation and of the final evaluation is \( O(p(\sqrt{m} + n/\sqrt{m})) \). The cost of computing \( C \) is given by invoking the tensor unit \( n/m \) times on two matrices of size \( p \times \sqrt{m} \) and \( \sqrt{m} \times \sqrt{m} \), that is \( O\left(\frac{pn}{\sqrt{m}} + \frac{n\ell}{m}\right) \).

### 5 Relation with the external memory model

In this section we highlight a relation between the external memory model and the TCU model. We recall that the external memory model (also named I/O model, and almost equivalent to the ideal cache model) is a model capturing the memory hierarchy and consists of an external memory of potential unbounded size, of an internal memory of potential unbounded size, and a processor. The processor can only perform operations with data in the internal memory, and moves (input/output) blocks of \( B \geq 1 \) words between the external memory and the internal memory. The I/O complexity of an algorithm for the external memory model is simply the number of blocks moved between the two memories. We refer to the excellent survey in [25] for a more exhaustive explanation.
The upper bounds derived for some of the previous problems recall the I/O complexity in the external memory model. For instance, the cost of dense matrix multiplication with only semiring operations (Theorem 2) is $O\left(n^{3/2}/\sqrt{m}\right)$ when $\ell = O(1)$, while the I/O complexity for the same problem in the external memory model is $O\left(n^{3/2}/\sqrt{m}\right)$ when $B = O(1)$.

We observe that the product between two matrices of size $\sqrt{m} \times \sqrt{m}$ requires $O(m)$ I/Os to load and storing the input in a memory of size $M = 3m$. Therefore any call to the tensor unit in a TCU can be simulated in the external memory of size $M = 3m$ with $\Theta(m)$ I/Os. We now exploit this fact by providing a theorem showing that a lower bound in the external memory model translates into a lower bound in a weaker version of the TCU model. In the weak TCU model, the tensor unit can only multiply matrices of size $\sqrt{m} \times \sqrt{m}$ (i.e., we cannot exploit tall left matrices). We observe that any algorithm for the original TCU model can be simulated in the weak version with a constant slowdown when $\ell = O(m)$: indeed, the multiplication between an $n \times \sqrt{m}$ matrix with a $\sqrt{m} \times \sqrt{m}$ can be executed in the weaker model by splitting the $n \times \sqrt{m}$ matrix into $n/\sqrt{m}$ matrices of size $\sqrt{m} \times \sqrt{m}$ and then performing $n/\sqrt{m}$ matrix multiplication with total time $O(n\sqrt{m})$.

**Theorem 8.** Consider a computational problem $P$ with a lower bound $F_P$ on the I/O complexity in an external memory with memory size $M = 3m + O(1)$ and block length $B = 1$. Then, any algorithm for $P$ in the weak TCU model has $\Omega(F_P)$ time.

**Proof.** Consider an algorithm for the weak $(m,\ell)$-TCU, and let $T = T_t + T_o$ be the total running time with $T = o(F_P)$: we denote with $T_t$ the running time due to tensor units, and with $T_o$ all the remaining operations. We can simulate the algorithm on an external memory with $M = 3m + O(1)$ as follows. All standard operations are simulated using $O(1)$ internal memory and incurring $O(T_o)$ I/Os. Each call to the tensor unit can be simulated in the external memory by loading the two input matrices in the internal memory with $O(m)$ I/Os, computing the product with no I/Os, and then writing the result in external memory with $O(m)$ I/Os. If we have $k$ calls to the tensor unit, the algorithm requires $km = O(T_t)$ I/Os (recall that each call requires $\Theta(m)$ time). Thus the TCU algorithm gives an external memory algorithm with I/O complexity $O(T_t + T_o) = o(F_P)$, which is a contradiction. Therefore, we must have $T = \Omega(F_P)$.

## 6 Conclusion

In this paper, we have introduced the first computational model for tensor core units, namely the $(m,\ell)$-TCU model. We have used this model for designing and analyzing several algorithms from linear algebra, broadening the class of algorithms that benefit of a fast hardware circuit for matrix multiplication.

The paper leaves several open questions:

- The TCU model should be experimentally validated. Do experimental performance behave as predicted in the theoretical model? Can we use the TCU model for effectively model Google TPUs and NVIDIA TCs?
- Which other computational problems can benefit of a tensor unit? Can existing algorithms for deep learning on tensor cores be further improved?
- Hardware accelerators have parallel tensors and low numerical precision. How can we include these features in the TPU model, and to which extent do they affect TPU algorithm design?

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