1. Introduction

TSV (Through-Silicon Via) provides vertical interconnection through silicon substrate, which offers benefits such as increased packaging density, heterogeneous integration, lower power and high bandwidth due to shorter interconnect length. [1] 2.5D/3D integration with TSV as one possible breakthrough method can overcome semiconductor scaling limits. [2] In this paper, we report our packaging material technology, which gives strong impact on the higher density integration and its reliability. [3] Redistribution layers (RDL) on Si interposer help to reroute signal lines to provide chip-to-chip and chip-to-substrate connection and power delivery compensating for the mismatch between chip I/O pad and TSV. Multilayered RDL on interposer is expected to meet the needs of high density and large numbers of electrical interconnects. For the RDL as well as a buffer coat application, a photosensitive insulation material with high resolution, stress buffer property and mechanical reliability is required. [4–6] We report the assembly results, the mechanical reliability and stress comparison between with and without this material.

Underfill materials are filled between organic/inorganic substrate and chip for stress relief. The conventional capillary underfill is difficult to be applied to the package with fine pitch bumps. Pre-applied wafer level underfill, which is formed to the whole wafer by lamination or spin coating, has been investigated. Pre-applied wafer level underfill flows not to be trapped between bumps and overflows to outside of chip. [7] Therefore we study the assembly process to control the amount of overflowed resin and satisfy the productivity for multi-die stacks with fine pitch bumps and TSV using film type underfill.

2. Material

We have developed the high resolution photosensitive dielectric CA6001B, [8] which is a phenol-based positive-tone and can be cured at lower temperature such as 200°C for low stress. Two types of film type pre-applied wafer level underfill CU2000B and CU2001B-1 were evaluated to satisfy process compatibility for multi-die stacks and low outgas during thermal compression bonding. Epoxy type solid molding compound CE5005B is selected for the excellent mechanical properties.

3. Test Vehicles

Test elementary groups (TEG) designed by IMEC were...
used for material evaluations. TEG structure for underfill evaluation is shown in Table 1. PTCM1 wafer is for the top chip with 15 \( \mu \text{m} \) diameter bumps and PTCN1 wafer is for the bottom chip with 25 \( \mu \text{m} \) diameter bumps. 8,250 bumps were designed in full area. Figure 1 shows schematic cross-section and the overview of PTCM1-PTCN1 stacking sample.

Another TEG structure for underfill evaluation is shown in Table 2. The test wafers are manufactured by IMEC standard 65 nm CMOS BEOL process, 5×50 \( \mu \text{m} \) via-middle TSV technology,[9] and 20/40 \( \mu \text{m} \) pitch Cu/Sn micro bumping process module.[10] PTCO having TSV is for the top and also middle chip with 7.5 \( \mu \text{m} \) diameter bumps on one side and 12.5 \( \mu \text{m} \) diameter bumps on the other side. PTCP is for the bottom chip with 12.5 \( \mu \text{m} \) diameter bumps. 3,828 bumps were designed in peripheral area. Figure 2 shows schematic cross-section and overview of PTCO-PTCP stacking sample.

### Table 1 Design of PTCM1 and PTCN1.

| Item             | PTCM1       | PTCN1       |
|------------------|-------------|-------------|
| Use              | Top chip    | Bottom chip |
| Die size (mm²)   | 5.1 × 5.1   | 8.1 × 8.1   |
| Bump array       | Full area   |             |
| Number of bumps  | 8,250       |             |
| Bump diameter (\( \mu \text{m} \)) | 15           | 25           |
| Bump pitch (\( \mu \text{m} \)) | 50           |             |
| Bump height (\( \mu \text{m} \)) | 9.5          | 10          |
| Bump composition (\( \mu \text{m} \)) | Sn/Ni/Cu (3.5/1/5) | Cu (10) |

### Table 2 Design of PTCO and PTCP.

| Item             | PTCO       | PTCP        |
|------------------|------------|-------------|
| Use              | Top/Middle chip | Bottom chip |
| Die size (mm²)   | 5.2 × 5.2  | 10.2 × 10.2 |
| Bump array       | Peripheral |             |
| Number of bumps  | 3,828      |             |
| Bump diameter (\( \mu \text{m} \)) | 7.5/12.5   | 12.5        |
| Bump pitch (\( \mu \text{m} \)) | 20          |             |
| Bump height (\( \mu \text{m} \)) | 8.5/5       | 5           |
| Bump composition (\( \mu \text{m} \)) | Sn/Cu (3.5/5/Cu (5)) | Cu (5) |
| TSV              | Yes        | No          |

Fig. 1 Schematic cross-section and overview of PTCM1-PTCN1 stack.

Fig. 2 Schematic cross-section and overview of PTCO-PTCP stack.

4. Result and Discussion

4.1 Redistribution layers

We have designed RDL having copper interconnections insulated with double layered photosensitive dielectric, daisy chains connecting 154 single chains with via holes from 3 to 40 \( \mu \text{m} \) diameters (b), and single chains from 3 to 80 \( \mu \text{m} \) diameters (c) as shown in Fig. 3.

CA6001B was coated on the wafer, prebaked on hotplate and then the insulation layer of 10 \( \mu \text{m} \) as 1\,st dielectric layer was obtained. The wafer was exposed with i-line stepper through the photomask designed for RDL evaluation. Then the wafer was developed with 2.38\% TMAH and cured at 200\°C. Next, copper wiring as 2\,nd metal layer was fabricated through seed deposition, resist lithography, copper plating, resist removal and seed etching process. CA6001B as 2\,nd dielectric layer was formed by the same method as 1\,st dielectric layer. The detailed process flow is shown in Fig. 4. Figure 5 shows the wafer overview after the above processes. CA6001B is verified to be compatible with RDL fabrication process because no defect such as delamination is observed. The electrical property was measured from 63 dies across the wafer and calculated the yield (Fig. 6). The each diameter described in Fig. 6 is mask size. CA6001B shows the excellent yield with fine daisy chain of RDL, that is, minimum 3 \( \mu \text{m} \).

The thermal cycling test of the fabricated RDL samples was evaluated. Figure 7(a) and (b) show the electrical yield of daisy chain and resistance of single chain after 1,000 cycles from –40\°C to 125\°C, respectively. The yield loss in 10 \( \mu \text{m} \) and 30 \( \mu \text{m} \) via chain was caused by pad oxi-
dation for electrical test. Although the daisy chain with 3 μm via shows serious yield loss and resistance increasing after heat cycles, the fine multilayered RDL having more than 5 μm vias keeps good electrical yield and resistance. The cross-sectional SEM images of RDL sample are shown in Fig. 8. No crack and delamination are observed after heat cycles.
4.2 Pre-applied underfill

We performed chip stacking using film underfill CU2000B and CU2001B-1. The underfills were laminated on PTCM1 wafers. The wafers were diced so as to provide PTCM1 chips with underfills. The wafer was diced without underfill delamination and crack. The PTCM1 chip was bonded with PTCN1 chip by flip chip bonder. Electrical yield of the daisy chain connecting 4,125 bumps was calculated from 15 stacking samples. The electrical resistance criteria for good sample set from 350 to 450 Ω based on the value of stacked samples without underfill. The stacked samples with CU2001B-1 afford 100% of electrical yield as shown in Fig. 9. The electrical resistance values of all samples were around 400 Ω. However the samples with CU2000B show 92% of electrical yield. The stacks with CU2000B were failed during thermal cycling test of 1,000 cycles from -40°C to 125°C by the some cracks of junction showing over 2,000 Ω. Figure 10 shows SAM (Constant-depth mode Scanning Acoustic Microscope) images after stacking. Clear voids and delamination are not observed.

Cross-SEM of the stacked sample using CU2000B shows much more underfill entrapment between bumps than CU2001B-1 as shown in Fig. 11. The lowest viscosities of CU2000B and CU2001B-1 during heating are 4,000 Pa·s and 2,000 Pa·s, respectively. We considered that this difference caused underfill entrapment and yield loss. We have selected CU2001B-1 which showed excellent yield and bump junction for next multi-die stacking evaluation.

We evaluated multi-die stacking with TSV. CU2001B-1 was laminated on PTCO wafer having TSV. The wafer is diced so as to provide PTCO chips with CU2001B-1. PTCP chip was used as a bottom chip. Each PTCO chip with CU2001B-1 was stacked step by step over PTCP at 260°C sequentially to obtain multi-die stacks. Figure 12 shows the fillet shape and stacked chips after each stacking processes. When the third die was stacked, underfill overflowed to top chip surface and bonding tool was contaminated. In case we continue next die stacking, the chip was cracked by overflowed resin. We checked the influence of underfill thickness but this issue was not improved. From these results, we judged it is difficult to achieve multi-die stacks in this sequential stacking method.

We have developed the collective stacking method. Each PTCO chip with CU2001B-1 was stacked step by step over PTCP at 100°C to fix PTCO chips. Then, we conducted collective bonding at 260°C to obtain multi-die stacks. The internal actual temperatures between bottom PTCP and first PTCO and also between 3rd and 4th PTCO were measured by putting in a thermocouple during bonding in advance. We confirmed that the above temperature differences are below than 5%. Figure 13 shows cross-section of the fillet shape and stacked chips. The fillet shape was improved and there is no crack after each stacking processes. Figure 14 shows the overview of the five-die-stack, 4th PTCO, 3rd PTCO, 2nd PTCO, 1st PTCO and PTCP by vertical collective stacking.

Figure 15 shows the schematic cross-section of five-die-stack. The five-die-stack with CU2001B-1 affords excellent electrical yield in each layers as shown Fig. 16, which means almost all bumps have good junctions including
TSV. The yield loss was caused by not junction but wiring issue of the chip itself from failure analysis. Figure 17 shows cross-sectional SEM. Clear voids and delamination are not observed although there is entrapment between bumps. This entrapment is to be improved by the modification of thermal compression profile.

### 4.3 Material integration for 3D/2.5D package

We integrated the photosensitive dielectric CA6001B as buffer coat, film type underfill CU2001B-1, and solid molding compound CE5005B. CA6001B shows the elongation property over 40% and 15 MPa residual stress as stress buffer material. PTCN1 chip with 3 μm thick CA6001B as buffer coat was attached to PTCM1 chip with CU2001B-1 by flip chip bonder. The stacked samples with CA6001B and CU2001B-1 are 100% of electrical yield (Fig. 18). Figure 19(a) and (b) show cross-sectional SEM and T-SAM (Transmission-mode Scanning Acoustic Microscope) images, respectively. Clear voids and delamination are not observed.

The stacked samples were mounted on BGA (ball grid array) substrate and encapsulated by epoxy molding compound CE5005B. The schematic package structure and overview are shown in Fig. 20. The thermal cycling test of

![Cross-section of fillet shape and stacked chip obtained by vertical collective stacking method.](image1)

![Overview of five-die-stacks with TSV using CU2001B-1.](image2)

![Schematic cross-section of five-die-stacks with TSV.](image3)

![Electrical yield of five stacks with TSV.](image4)

![Cross-sectional SEM of five stacks with TSV.](image5)

![Electrical yield of PTCM1-PTCN1 with CA6001B and CU2001B-1.](image6)

![Cross-sectional SEM and (b) T-SAM inspection.](image7)

![Schematic package structure and overview.](image8)
1,000 cycles from –40°C to 125°C and pressure cooker test of 121°C/100% RH in 2 atm for 240 h after MSL 3 (30°C/60%RH/168 h) were performed as the package reliability test. The electrical yield and resistance keep constant values during the thermal cycling (Fig. 21). The cross-sectional SEM and T-SAM images as shown in Fig. 22 reveal there is no delamination in the package though the minor crack was observed in bump junction by underfill entrapment. Furthermore, the samples pass the pressure cooker test as well.

Stress distribution is estimated by means of raman shift. [11–14] The stress buffer effect in the stacked sample was investigated and the stress distribution was shown in Fig. 23. Raman shift was measured 500 nm depth from Si surface. The compression stresses under bumps in a TEG were estimated 300 MPa without buffer layer and 100 MPa with buffer layer, respectively. This result indicates that CA6001B buffer layer relieves stress under bumps by 3D stacks.

5. Conclusion

We have demonstrated fine RDL using photosensitive dielectric CA6001B and 2.5D/3D package structure using photosensitive dielectric as buffer coat, film underfill, and solid molding compound. The fine RDL with 5 μm via holes using CA6001B shows excellent electrical yield and passes thermal cycling test. The raman shift in 3D stacks with photosensitive dielectric CA6001B as a buffer layer indicated lower stress than the one with silicon nitride. PTCM1-PTCN1 stacks with 50 μm pitch using CU2001B-1 shows 100 % electrical yield. During the multi-die assembly in conventional sequential method, the stacked chip was cracked due to overflowed underfill. By the vertical collective stacking, five-die-stack with 20 μm pitch, which is connected by TSV shows excellent yield. Finally we integrated our photosensitive dielectric, pre-applied underfill and molding compound in the stacked package, passing reliability tests such as thermal cycling reliability and pressure cooker test.

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