Electrical and Thermal Properties of SnTe/Sb$_2$Te$_3$ Superlattice Phase Change Materials

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Abstract

The fundamental electrical and thermal properties of the devices consisting of Sn$_x$Te$_{1-x}$/Sb$_2$Te$_3$ superlattice (SnTeSL) materials have been investigated and compared with those of the conventional Ge$_2$Sb$_2$Te$_5$ (GST225) and GeTe/Sb$_2$Te$_3$ superlattice (GeTeSL) in terms of their resistance switching characteristics. A significant reduction in the switching power of SnTeSL is demonstrated by conducting a proper initialization procedure, varying $x$ in Sn$_x$Te$_{1-x}$/Sb$_2$Te$_3$, and applying short electric pulses. It is found that the observed drastic power reduction occurs due to the exponential decrease in the electric current under the pulse incidence. On the other hand, the thermal properties of the studied SL materials are very similar to those of the conventional phase change materials. The obtained transmission electron micrographs and results of multilevel-cell recording in GeTeSL and SnTeSL via multi-pulse incidence are totally different from the properties of the phase change materials along the GeTe-Sb$_2$Te$_3$ pseudo-binary tie line. Two different models (the partial switching and electric field-induced one) are proposed to elucidate the mechanism of the resistance switching in the SL materials.

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I Introduction

Phase-change memory (PCM), which has been practically implemented in rewritable optical disks, is a promising candidate for the next-generation solid-state memory technology. It possesses many advantages such as excellent high-speed switching characteristics and good scalability, which can be potentially utilized for the fabrication of high-speed large-capacity memory chips. However, PCM also has drawbacks, including high power consumption during the resistance switching from the low to the high state (reset operation), which is required for melting the PC component. If the melting point of the utilized material (and, therefore, the crystallization temperature) is too low, its reset power \( P_{\text{rst}} \) becomes very small, leading to the deterioration of its retention properties. Among various PC materials, Ge\(_2\)Sb\(_2\)Te\(_5\) (GST225)\(^{13}\) possesses a relatively low melting point, adequate crystallization characteristics, and good overwritability (endurance properties). However, even this material is unable to fully satisfy the requirements for PCM device. In previous studies, a superlattice-like (SL) PC material consisting of alternately stacked GeTe and Sb\(_2\)Te\(_3\) layers has been successfully prepared and utilized for the reduction of \( P_{\text{rst}} \) to a magnitude equal to about 1/3 the GST225 level. Surprisingly, this material demonstrated high overwritability despite the expectations that the layered structure would be destroyed after multiple melting cycles. Furthermore, the superlattice (SL) PC material has been propose (GeTeSL). While this SL consists of the alternate stacks of GeTe and Sb\(_2\)Te\(_3\) as SLL, its \( P_{\text{rst}} \) magnitude is equal to 1/10 of the GST225 value, which is about three times lower than that of SLL. The studied SL and SLL materials mainly differ in their layer thicknesses and crystalline structures. Thus, the thickness of the GeTe layer in SL is about 1 nm, while that in SLL is about 3.5 nm. Similarly, the crystalline structure of each GeTe layer in SL is aligned along the (111) direction, whereas the SLL layers are randomly oriented. However, these differences cannot fully elucidate the mechanism of lowering \( P_{\text{rst}} \) in SL and SLL. After the proposal of GeTeSL, a number of studies\(^{10-15}\) have been performed to investigate the properties of GeTeSL. Some studies\(^{15,20}\) have proposed the mechanism of low power switching in SL materials, which, however, should remain investigated more on the possibility to explain all the experimental results on SL materials including the results to be reported in this paper.

Moreover, a much lower \( P_{\text{rst}} \) has been obtained for the SL structure consisting of SnTe and Sb\(_2\)Te\(_3\) layers ("SnTeSL")\(^{21}\). In particular, the \( P_{\text{rst}} \) of Sn\(_{0.1}\)Te\(_{0.9}\)/Sb\(_2\)Te\(_3\) SL is smaller than that of GST225 by a factor of more than 10\(^3\). However, the reasons for such low \( P_{\text{rst}} \) and fundamental properties of this material remain unclear.

In this work, the fundamental characteristics of SnTeSL are examined experimentally, and the mechanism of the resistance switching in the SL PC materials is discussed by comparing them with the properties of the GST225 and GeTeSL materials. As a result, a reduction in \( P_{\text{rst}} \) by a factor of 10\(^{-3}\) is observed for Sn\(_x\)Te\(_{1-x}\)/Sb\(_2\)Te\(_3\) SL with \( x = 0.1 \) as compared to the value obtained for GST225. Experimental studies are performed by initializing the SL materials with short electric pulses; investigating their scaling and annealing properties; taking transmission electron microscopy (TEM) images of the as-deposited, set, and reset states; and obtaining multilevel cells (MLC) by applying multiple pulses.

II Experimental

SnTeSL and GeTeSL samples were prepared using the procedure described in the previous reports. Their cross-sections are depicted in Fig. 1. The utilized substrates consisted of the W electrodes deposited on Si wafers below SiO\(_2\) layers. The diameter of the electrode in this study was 120 nm if not specified otherwise. The remaining device structure consisted of TiN (1 nm), Sb\(_2\)Te\(_3\) (10 nm), PC, and W (50 nm) films obtained by sputter deposition. The PC films were GST with thicknesses of 50 nm: [GeTe (1 nm)/Sb\(_2\)Te\(_3\) (4 nm)]\(_8\) for GeTeSL and [Sn\(_x\)Te\(_{1-x}\) (1 nm)/Sb\(_2\)Te\(_3\) (4 nm)]\(_8\) for SnTeSL. To deposit a SL film, GeTe, SnTe, and Sb\(_2\)Te\(_3\) targets were sputtered alternately. During sputtering, the substrate was heated to 250°C in the cases of GST and GeTeSL, and to 200°C in the case of SnTeSL. The reason for selecting a lower temperature for SnTeSL was to avoid alloying the SnTe and Sb\(_2\)Te\(_3\) layers. After sputtering, electronic devices with sizes of about 100 \( \mu \)m were patterned using photolithography and reactive ion etching techniques.

The electric properties of the fabricated devices were investigated using the tester described elsewhere, which applied write and read pulses to the probes connected to the bottom and top electrodes. The read voltage was 0.1 V. The shape of the programmed pulse was rectangular whose typical length was 100 ns if not specified otherwise. The voltage pulses applied to the tested device became dull with time due to the existence of
parasitic resistance and capacity, which were measured using an active field-effect transistor (FET) probe. Fig. 2 shows the time evolution of the voltage and current passing through the device, indicating that the rise and fall times of the generated pulses ranged between 5 and 10 ns.

The electrical properties of the GST device measured using this system are shown in Fig. 3, where $V_{\text{pulse}}$ is the pulse voltage set by the computer, and $V_{\text{device}}$ denotes the voltage measured with the active FET probe during the pulse incidence. The differences between the data presented in Fig. 3(a) and (b) result from the dependence of the device resistance on the applied voltage. The total resistance in the measurement system can be written as the sum of the device resistance $R_{\text{device}}$ and the parasitic resistances brought by other components $R_{\text{para}}$, i.e., $R_{\text{device}} + R_{\text{para}}$. Accordingly, we can write $V_{\text{device}} = V_{\text{pulse}} R_{\text{device}} / (R_{\text{device}} + R_{\text{para}})$. Since $R_{\text{para}}$ can be considered independent of the pulse voltage and the device resistance, $V_{\text{device}}$ rapidly decreases when $R_{\text{device}}$ decreases rapidly by crystallization of GST225 in the device.

The thermal properties of the SnTeSL and GeTeSL devices were investigated by placing them on a hot plate and measuring their read resistances while increasing the plate temperature at a heating rate of 1°C/s. TEM observations were performed at Toray Research Center (Japan). The utilized TEM samples were Sn$_{0.5}$Te$_{0.5}$/Sb$_2$Te$_3$ devices in the initial, initialized low resistance (set) and reset states, and the broken state. The reset state was obtained after 10 rewriting cycles, whereas the broken cell was prepared by applying a high reset voltage of 4 V instead of the typical value equal to around 1 V.

### III Results

#### A Fundamental properties of the Sn$_{0.5}$Te$_{0.5}$/Sb$_2$Te$_3$ SL device

Fig. 4 describes the initialization process of the prepared Sn$_{0.5}$Te$_{0.5}$/Sb$_2$Te$_3$ SL device. It shows that its initial state corresponds to the high resistance state, although all the films inside the activated region retained their crystalline properties. This high initial resistance was observed in the majority of the cells in this study and also in GeTeSL. This property is similar to the previous reports. For the reasons currently remaining unclear, the initial resistances of most devices with low switching power are typically high, which will be discussed later in this work. Furthermore, the obtained results reveal that successful resistance switching requires the application of several initializing pulses. The initialization experiments conducted using multiple cells show that the number of these pulses depends on the cell type and is typically varied between one and three, while the utilized pulse voltage lies in the region of 1.0 - 1.2 V.

Fig. 5 shows the results of the pulse sweep measure-
Fig. 4. Initialization of the Sn<sub>0.5</sub>Te<sub>0.5</sub>/Sb<sub>2</sub>Te<sub>3</sub> SL material with high initial resistance. The applications of the (a) first, (b) second, (c) third, and (d) fourth pulses.

Fig. 5. Relationships between the voltage and read resistance $R_{\text{read}}$ (corresponding to the dynamic current $I_{\text{dyn}}$) obtained for the Sn<sub>0.5</sub>Te<sub>0.5</sub>/Sb<sub>2</sub>Te<sub>3</sub> SL device. The initial states are the (a)(c) high and (b)(d) low resistance states. The vertical axes denote the (a)(b) programmed voltage $V_{\text{pulse}}$ and (c)(d) practically applied voltage $V_{\text{device}}$.

ments performed after the initialization process. The obtained reset power was about 1/15 of that of the GST device. The data presented elsewhere<sup>10</sup> show that the $P_{\text{rst}}$ of the Ge<sub>0.5</sub>Te<sub>0.5</sub>/Sb<sub>2</sub>Te<sub>3</sub> SL device was about 1/10 of value obtained for the GST device, suggesting that the $P_{\text{rst}}$ of SnTeSL was of the same order of magnitude as that of GeTeSL.

Fig. 6 describes the endurance properties of the SnTeSL device with the endurance properties of GST and GeTeSL devices for comparison. This figure indicates that it is capable of sustaining at least $10^8$ switching cycles in SL devices, which confirm the results almost equivalent to the previous one reported by Simpson et al.<sup>8</sup> In contrast, the maximum number of cycles obtained for the GST device was $10^6$. The better endurance performance of SL devices may result from its lower switching power, which generates a lower amount of stress inside the cell. However, the read resistances of SL devices are much less stable than those of GST. Both the set and reset resistances increase after $10^3$ $10^4$ or $10^5$ cycles and recover their original values after overwriting. While this feature is undesirable for practical use, the relative instability of the read resistance can be corrected by controlling the set and reset voltages during rewriting (data not shown). Thus, this instability can be solved by verification of the formed read resistance which has been already adopted in the current semiconductor memories such as flash memories. This instability, however, should be solved if solvable. To this end, the cause of this instability should be clarified, which will be discussed in Sec. IV.

As shown in Fig. 4, the initial resistances of the majority of the studied cells were high. However, some cells exhibited low initial resistances. Their electric properties are described in Fig. 7. According to the obtained results, the reset voltage $V_{\text{rst}}$ and $P_{\text{rst}}$ of the SnTeSL device are almost equal to those of GST, and then once the device is in the reset state, the device shows the low power switching. Thus, this process that converts the initial low resistance into the reset state can be called the initialization process for low power switching. Nevertheless, the described procedure has been rarely successful. In most cases, the cell was broken and exhibited extremely high resistance (such as $10^{11}$ Ω) during the reset process. The similar property was observed also in GeTeSL where high power is necessary to form the high resistance from the low initial resistance to start low power switching. Thus, this property seems common to SL materials. From these experimental facts, the high initial resistance seems essential in SL materials. This fact is not contradictory with the previous
Fig. 6. Endurance properties of the (a) GST, (b) Ge$_{0.5}$Te$_{0.5}$/Sb$_2$Te$_3$ SL and (c) Sn$_{0.5}$Te$_{0.5}$/Sb$_2$Te$_3$ SL materials.

report\(^8\) where the initial resistance was high. Thus, this property seems to represent an important aspect of the switching mechanism of the tested SL devices, which will be discussed in more detail in Sec. IV.

Fig. 8 displays the result of the pulse sweep measurement conducted for the SnSbTe device fabricated by sputtering Sn$_{0.5}$Te$_{0.5}$ and Sb$_2$Te$_3$ targets simultaneously at the sputtering rates equal to those utilized for the fabrication of the SnTeSL devices. They show that the tested device was broken before reaching the high resistance state. The likely reason for the absence of amorphization of the SnSbTe layers was their very high recrystallization rate due to the Sn-doped GST\(^{22,23}\). Hence, it can be concluded that the presence of a superlattice or layered structure significantly affects the resistance switching properties of SnTeSL.

Fig. 9 displays the dependences of the set power $P_{set}$ and $P_{rst}$ of the GST, GeTeSL, and SnTeSL devices on their cell diameters (the scaling properties). About ten cells were examined for each device, and the obtained average values were plotted with the standard deviations drawn as the error bars. The obtained results show that both GeTeSL and SnTeSL devices exhibit no dependences on the cell diameter. Tai et al. has reported the scaling property of GeTeSL which concludes that the reset current shows approximately $r^{1.6}$ dependence where $r$ represents the size of the resistor\(^24\). Here four points are discussed regarding the discrepancy between their conclusion and the data in this paper. One is the difference of the quantity of the vertical axis where one is the reset current and the other is the reset power. This difference, however, is not essential because the reset voltage $V_{rst}$ of SL devices showed no dependence of the cell size in this paper. Secondly, the number of the data points in this reference\(^24\) is too small to draw an exact fitting curve. Moreover, no error bars on which a fitting curve should pass are not shown. Thus, their conclusion might be somewhat hasty. The number of the data in this paper, however, is also not very large. In discussing this kind of properties statistically, the number of data should be more than tens or hundreds. This issue should be remained as a more precise future work. The third point to be discussed is the difference in configurations where the device in this reference\(^24\) is pillar while the devices in this paper have the configuration shown in Fig. 1. The effect brought about by the difference in configurations is, however, not clear because of the unclear mechanism of the resistance switching in SL devices. Lastly, the common point to this reference and this paper is, despite the quantitative difference, that the scaling properties of the SL devices are weaker than that of GST\(^{22,25}\), which seems relevant to the mechanism of resistance switching in SL devices. Though the exact conclusion must be drawn af-
Fig. 8. Relationship between the programmed voltage $V_{pulse}$ and the read resistance $R_{read}$ of the SnSbTe device, which consisted of the SnTe and Sb$_2$Te$_3$ layers.

After more precise studies, the scalability will be discussed in Sec. IV under the assumption that the reset and set powers in the SL devices have almost no dependence on the cell size because Fig. 9 seems correct for the SL devices (both GeTeSL and SnTeSL) with the configuration as shown in Fig. 1.

Fig. 9. Scaling properties of the GST, GeTeSL, and SnTeSL materials determined during the (a) set and (b) reset operations.

Fig. 10 describes the reset properties of the studied cells determined at shorter pulse widths. Here, $V_{rst}$ is the value measured with the FET probe, which represents the voltage practically applied to the device. Because the short pulses become dull with time (see Fig. 2), their maximum amplitudes are plotted in Fig. 10. Both the voltage and current were normalized by the values of $V_{rst}$ and $I_{rst}$ measured at a pulse width of 100 ns, respectively. The $V_{rst}$ magnitudes obtained at different pulse widths were almost identical, while the values of $I_{rst}$ decreased after applying shorter pulses. As a result, the magnitude of $P_{rst}$ decreased with decreasing pulse width, which was also observed both qualitatively and quantitatively elsewhere [10], suggesting that this property was common for various SL structures.

Fig. 10. Relationships between the programmed reset pulse width and reset voltage ($V_{rst}$) / current ($I_{rst}$).

Fig. 11 shows the dependence of the read resistance on the annealing temperature, indicating that the reset resistances of all devices rapidly decrease at temperature $T_{set}$. Furthermore, the $T_{set}$ of GeTeSL was almost equal to that of GST, although its value determined for the GeTe device was about 200°C. From these results, it can be hypothesized that the interface between the GeTe and Sb$_2$Te$_3$ layers is mainly responsible for the resistance switching in the GeTeSL structure. This assumption can be used to explain the results presented in Fig. 8 for SnTeSL.

Fig. 11. Relationships between the annealing temperature and resistances of the GST, GeTeSL, and SnTeSL materials, whose initial states corresponded to the reset states.

B Properties of Sn$_{1-x}$Te$_x$/Sb$_2$Te$_3$ SL devices

Fig. 12 shows the set and reset voltages and currents of the Sn$_{1-x}$Te$_x$/Sb$_2$Te$_3$ SL devices, indicating that their $V_{rst}$ values obtained at various $x$ were almost identical, while the magnitudes of $I_{rst}$ decreased at smaller $x$. Note that the right axis in this figure representing the current...
is logarithmic, while the left one denoting the voltage is linear. The measured $P_{\text{rst}}$ of the Sn$_{0.1}$Te$_{0.9}$/Sb$_2$Te$_3$ SL device was smaller than that of GST by a factor of less than $10^{-3}$. Thus, the extreme reduction of the switching power at smaller $x$ resulted mainly from the decrease in the switching current. This observation appears to be consistent with the results obtained after the application of short pulses in Fig. 10.

![Fig. 12](image12.png)

**Fig. 12.** Set and reset voltages and currents measured for the Sn$_x$Te$_{1-x}$/Sb$_2$Te$_3$ materials at various $x$ during the (a) set and (b) reset operations.

Fig. 13 shows the set and reset read resistances of the Sn$_x$Te$_{1-x}$/Sb$_2$Te$_3$ SL devices, whose values increase with decreasing $x$. The $R_{\text{rst, read}}(x)/R_{\text{set, read}}(x)$ ratio between these two parameters decreases at smaller $x$; however, at $x = 0.1$, its value becomes equal to $10^2$, which is sufficient for practical use.

![Fig. 13](image13.png)

**Fig. 13.** Set and reset resistances of Sn$_x$Te$_{1-x}$/Sb$_2$Te$_3$ as functions of $x$.

### C TEM images of SnTeSL devices

Fig. 14 contains the TEM images of various states of the Sn$_{0.5}$Te$_{0.5}$/Sb$_2$Te$_3$ SL devices. In particular, Fig. 14(a), (b), and (c) show that the fabricated SL films are polycrystalline, although their grains exhibit similar structures characterized by the presence of five periodic atomic layers which likely originates from the Sb$_2$Te$_3$ layers with relatively long Te-Te bonding. The obtained three TEM micrographs exhibit no significant differences between the corresponding read resistances. This observation will be discussed in more detail in Sec. IV.

![Fig. 14](image14.png)

**Fig. 14.** TEM images of Sn$_{0.5}$Te$_{0.5}$/Sb$_2$Te$_3$ obtained for the (a) initial state, (b) initialized set state, (c) reset state, and (d) cell broken by applying a high reset voltage. The left column (1) shows the macroscopic images, the middle column (2) contains the atomic scale images, and the graphs depicted in the right column (3) characterize the effects of the electric pulses applied to produce samples for TEM observations.

Fig. 14(d) shows the TEM images of the cells broken by applying a high voltage. Panel (d-3) demonstrates a higher $V_{\text{rst}}$ than that of panel (c-2), indicating that this cell was broken at least as a SL device although not completely because it exhibits resistance switching at voltage higher than the typical voltage. The sample depicted in Fig. 14(d-1) is characterized by a lower degree of crys-
tallinity as compared to those of the specimens depicted in panels (a-1), (b-1), and (c-1). In contrast, the image presented in Fig. 14(d-2) does not exhibit the periodicity demonstrated in panels (a-2), (b-2), and (c-2). Thus, it can be concluded that good periodic properties are essential for achieving low $P_{\text{rst}}$ values.

Every TEM graph in Fig. 14 shows the SL film in polycrystalline state though some regions show the periodic order. This might indicate that the well-aligned single crystal superlattice structures are not always essential for low power switching. Fig. 14(a), (b) and (c) exhibit periodic structures consisting of five atoms while Fig. 14(d) does not show low power switching, does not. These facts indicate, as circumstantial evidences, that this periodic structure must be the key for low power switching. Though Fig. 14 shows the TEM graphs of Sn$_{0.5}$Te$_{0.5}$/Sb$_2$Te$_3$, the same discussion might be applied to Sn$_{0.1}$Te$_{0.9}$/Sb$_2$Te$_3$, which shows the lowest power switching in the superlattice phase change materials ever reported, because Soeysa et al. reported the structure analyses of Sn$_{0.1}$Te$_{0.9}$/Sb$_2$Te$_3$ where the same periodic structures consisting of five atoms Te-(Sn, Sb)-Te-(Sn, Sb)-Te, are concluded. Although this study challenged to identify the atomic species in this periodic layer, this identification failed because the atoms in this material have the close atomic numbers, 50, 51, and 52 where the identification using electron beams was impossible. Thus, the details of this structure are not clear. However, there is a possibility that Sn$_x$Te$_{1-x}$/Sb$_2$Te$_3$ studied in this paper have the same structure with the different composition ratio in (Sn, Sb). But still this hypothesis does not explain lower power switching for smaller $x$ in Sn$_x$Te$_{1-x}$/Sb$_2$Te$_3$. The relationship between low power switching and the structures of superlattice phase change materials must be studied further.

D Superlattice cycles and switching power

Fig. 15 shows the dependence of $V_{\text{rst}}$, $I_{\text{rst}}$ and $P_{\text{rst}}$ on the number of the superlattice layers (superlattice cycles) in Sn$_{0.5}$Te$_{0.5}$/Sb$_2$Te$_3$ SL devices, where the nominal superlattice cycles described in Sec. 11 is 8. This figure shows that both $V_{\text{rst}}$ and $I_{\text{rst}}$ decrease as reduction of the superlattice cycles. This might be reasonable because the volume to be switched decreases as the superlattice cycles are reduced. Note, however, that the decrease of $I_{\text{rst}}$ is close to exponential while the decrease of $V_{\text{rst}}$ is close to linear. As a result, $P_{\text{rst}}$ becomes $10^{-4}$ of that of GST in the device with the single superlattice cycle. The cause of this behavior will be discussed in Sec. IV.

E Multilevel cells of SL devices

MLCs are necessary components of the storage devices with large data capacities. Their formation can be achieved by applying a voltage of less than $V_{\text{rst}}$ to the PC device. For example, Fig. 8(a) shows that the voltages of 2.0 V, 2.2 V, and 2.6 V applied to GST resulted in the read resistances of $5.5 \times 10^3$ Ω, $2.3 \times 10^4$ Ω, and $1.4 \times 10^5$ Ω, respectively. However, the formation of MLCs in SL devices appears to be a challenging task because their set and reset processes occur rapidly without a significant voltage margin, as shown in Fig. 8. The experiments performed using different cells show that applying a voltage of slightly less than $V_{\text{rst}}$ leads to a medium read resistance, which is too unstable for practical use.

Fig. 16 displays the results of multiple pulse testing aimed at mitigating this issue. It shows that both the GeTeSL and SnTeSL devices exhibit three-level discrete read resistances. One of the interesting characteristics in these figures is that some cases (0.8 V in Fig. 16(a) and 0.75 V in Fig. 16(b)) show the resistances first increased and then decreased to constant values while other cases show the resistance increased with the number of pulses. This seems to indicate that these three levels are determined by some mechanism, which has not been fully clarified yet.

IV Discussions

This section mainly discusses the mechanism of low power switching in SL devices using partial switching and electric field-induced switching models. This task is performed by considering the data obtained in the current study. The explicability of each data by each model is listed in Table 1. The details on the models and their
Fig. 16. Relationships between the number of induced pulses and the read resistances of the (a) GeTeSL and (b) SnTeSL materials.

The diagrams describing the partial switching model are shown in Fig. 17. Here the activated regions are layered, which is essential for low power switching as shown in the TEM graphs depicted in Fig. 14. Fig. 17(a) displays the initial as-deposited state characterized by relatively high resistance. The initialization process produces multiple low resistance regions (Fig. 17(b)), which represent activated regions for the overwriting operation, while the other regions retain their high resistances. The reset operation switches the resistance of some of these activated regions (Fig. 17(c)) because it requires switching all the activated regions of only one layer into the high resistance state.

This partial switching model can satisfactorily explain the data presented in Fig. 4, Fig. 7, Fig. 8, Fig. 9, Fig. 11, and Fig. 12. The initialization processes in Fig. 4 and Fig. 7 can occur partially in some regions since the inhomogeneity in the deposited films produces sites that are relatively easy to switch (easily-switching sites). When these sites are switched multiple times during overwriting, the electric properties of the cell remain stable. The results presented in Fig. 7 can be explained as follows. If the initial resistance of the cell is low, the switching process requires relatively high power (similar to that used in ordinary phase change memory chips). Once the resistance of the entire cell becomes high, low power switching sites must be generated in the next step. The result in Fig. 8 (no switching in the alloyed state) is also explained if it is assumed that the layered structure or the interfaces of the layers generate the easily-switching sites. Furthermore, the absence of scalability in Fig. 9 is also explained because the switching power of a material is typically determined not by the cell size, but by the number of switching sites. The annealing properties of the studied materials described in Fig. 11 can be elucidated by assuming that the switching mechanism corresponds to a conventional phase change reaction consisting of the crystallization and amorphization processes at the switching sites. The low current switching depicted in Fig. 12 can be explained by modeling the switching sites as parallel resistors. In this case, the electric current is reduced by decreasing the number of the resistors, while the voltage remains almost the same. The low power switching in the layered structure (TEM graphs in Fig. 14) can be explained by assuming that the switching sites are located at the layer interfaces. For example, in the GeTeSL structure, both the GeTe and Sb₂Te₃ layers do not exhibit low power switching properties, while their alloying ratio varies in the vertical direction. If some interfacial sites are characterized by the optimal alloying ratio, they can undergo low power switching.

This partial switching model might explain the cause of the endurance properties in Fig. 6 by, for example, the following hypothesis as shown in Fig. 17(d). If the atomic mobility in some of the activated regions becomes low because of a certain local condition, the difference between the set and reset resistance becomes low until new regions are activated. This phenomenon is similar to resistive random access memories (ReRAMs) where similar instability in endurance is often observed. If the switching mechanism of SL materials is similar to that...
of ReRAMs, the instability of endurance in SL devices might be solved by the similar circumstances adopted in ReRAMs such as surface modification and so on. Although the partial switching model can explain many experimental findings as was shown above, it is not consistent with the data presented in Fig. 10, Fig. 15 and Fig. 16. While it was possible to elucidate the results of Fig. 10 in terms of switching a limited number of the switching sites induced by the low voltage, the generated read resistances exhibit exponential behavior, suggesting that the number of the switched sites was exponentially dependent on the applied voltage, which appeared to be explicable with the conventional theories of phase change. Moreover, this model requires that the total volume of the switching sites in the Sn$_{0.1}$Te$_{0.9}$/Sb$_2$Te$_3$ SL structure be equal to about $10^{-3}$ of that in the Sn$_{0.5}$Te$_{0.5}$/Sb$_2$Te$_3$ SL structure, which is relatively hard to maintain from one experiment to another. However, the obtained data exhibit high repeatability, as indicated by the error bars in Fig. 12. Thus, the partial switching model is unable to explain all the phenomena observed in this work.

Now the other model, the electric field-induced switching model which is capable of explaining almost all the data obtained in this study (except for Fig. 16), is considered. The results depicted in Fig. 4 and Fig. 7 are interpreted using an approach similar to that of the partial switching model if it is assumed that the electric field can switch the resistance in SL cells with some mechanism. No switching in the alloyed state (Fig. 8) can be explained if the utilized model is applicable only to the layered structure.

The data presented in Fig. 10, Fig. 12 and Fig. 15 which show that low power switching is caused by the extremely low electric current during the pulse incidence, can be satisfactorily explained by this model utilizing only the electric voltage or field as the main physical parameter and not the electric current nor the power such as Joule’s heat. In this case, the annealing properties described in Fig. 11 can be elucidated by assuming that the resistance switching induced by the applied electric field represents a conventional phase change process consisting of the crystallization and amorphization stages. Furthermore, the absence of scalability in Fig. 9 may be explained by estimating the intensity of the electric field induced by applying voltage to the cell. Its calculated values are shown in Fig. 18. The computation was performed in the cylindrical coordinates with the $x$ and $z$ axes defined as the horizontal and vertical directions, respectively. In these calculations, the resistivities of the Sb$_2$Te$_3$ and GeTe layers were assumed to be equal to that of crystalline GST, which did not significantly affect the obtained results because the resistivities of crystalline GST, Sb$_2$Te$_3$, and GeTe were about three orders of magnitude higher than that of W. The TiN underlayer was ignored because of its very small thickness.

The results presented in Fig. 18 show that both $E_x$ and $E_z$ are localized around the edge of the electrode and $E_x$ is more localized than $E_z$. The experimental data reported elsewhere indicate that the parameter $E_x$ mainly affects the low power switching process. From the results presented above, it can be concluded that the switching power is independent of the cell size because the driving force $E_x$ is localized at the cell edge. Moreover, Fig. 18(c)(f) show that the peak intensity of the field depends only weakly on the cell size, especially at $z = 10$ nm where the SL structure begins. These results are consistent with the TEM graphs presented in Fig. 12 indicating that the vectorial parameters (such as electric field) produce a greater effect on the layered structure than on the bulk system. The similar phenomenon has

| Experimental data (figure) | Partial switching | Field-induced switching |
|----------------------------|-------------------|------------------------|
| Initialization from high to low (Fig. 4) | Y | (Y) |
| Initialization from low to high (Fig. 7) | Y | (Y) |
| No switching in the alloyed state (Fig. 8) | Y | (Y) |
| No scalability (Fig. 9) | Y | (Y) |
| Low current switching by short pulses (Fig. 10) | N | Y |
| Annealing properties (Fig. 11) | Y | (Y) |
| Low power switching in layered structure (Fig. 14) | Y | Y |
| Reduction in $P_{rs}$ with decreasing SL cycles (Fig. 15) | N | Y |
| MLC formation by multiple pulses (Fig. 16) | N | N |

Table 1. Experimental results and interpretability of the proposed hypotheses. “Y” and “N” denote “explicability” and “inexplicability”, respectively. (Y) indicates “conditional” or “uncertain”.

The data presented in Fig. 10, Fig. 12 and Fig. 15 which show that low power switching is caused by the extremely low electric current during the pulse incidence, can be satisfactorily explained by this model utilizing only the electric voltage or field as the main physical parameter and not the electric current nor the power such as Joule’s heat. In this case, the annealing properties described in Fig. 11 can be elucidated by assuming that the resistance switching induced by the applied electric field represents a conventional phase change process consisting of the crystallization and amorphization stages. Furthermore, the absence of scalability in Fig. 9 may be explained by estimating the intensity of the electric field induced by applying voltage to the cell. Its calculated values are shown in Fig. 18. The computation was performed in the cylindrical coordinates with the $x$ and $z$ axes defined as the horizontal and vertical directions, respectively. In these calculations, the resistivities of the Sb$_2$Te$_3$ and GeTe layers were assumed to be equal to that of crystalline GST, which did not significantly affect the obtained results because the resistivities of crystalline GST, Sb$_2$Te$_3$, and GeTe were about three orders of magnitude higher than that of W. The TiN underlayer was ignored because of its very small thickness.

The results presented in Fig. 18 show that both $E_x$ and $E_z$ are localized around the edge of the electrode and $E_x$ is more localized than $E_z$. The experimental data reported elsewhere indicate that the parameter $E_x$ mainly affects the low power switching process. From the results presented above, it can be concluded that the switching power is independent of the cell size because the driving force $E_x$ is localized at the cell edge. Moreover, Fig. 18(c)(f) show that the peak intensity of the field depends only weakly on the cell size, especially at $z = 10$ nm where the SL structure begins. These results are consistent with the TEM graphs presented in Fig. 12 indicating that the vectorial parameters (such as electric field) produce a greater effect on the layered structure than on the bulk system. The similar phenomenon has
been reported\textsuperscript{27} where the atoms in GST migrate along the external electric field (Ge and Sb to the cathode and Te to the anode). This phenomenon might be related to the mechanism of resistance switching in SL materials. For example, Sb and Te migrate to the opposite sides, which should affect the behavior of the van der Waals forces at Te-Te bonds in Sb\textsubscript{2}Te\textsubscript{3} layers. If the external electric field reduces the distance of Te-Te bonds and applies the opposite forces to Ge and Te atoms, GeTe might get easier to change its phase, which leads to low power switching. This phenomenon easily occurs in SL materials maybe because the atoms are aligned more periodically in SL materials than in GST even though SL materials are in polycrystalline states. This discussion is applied also to SnTeSL because Sn is in the same group as Ge in the periodic table and has the similar ionic properties. A non-thermal phase change has been observed previously by applying picosecond pulses\textsuperscript{28}. Hence, it can be concluded that low power switching was achieved in this work due to the application of nanosecond pulses because the total amount of $E_x$ was greater in the layered structure despite the polycrystallinity of the SL layers (see Fig. 14). These data can qualitatively explain the non-scalability properties depicted in Fig. 9. The $E_x$ component is localized along the perimeter of the cell, which lead to the conclusion that the scalability of the studied cells is characterized not by their radii, but by the linear dependence of the radii. However, this conclusion is not consistent with the results presented in Fig. 9 which may be explained by the combination of the partial switching and electric field-induced switching models, where the applied electric field switches the resistance only at certain regions of the cell.

Although the electric field-induced switching model can partially explain the obtained experimental data, the results presented in Fig. 16 are not fully consistent with it. Moreover, many particular details of the related mechanism are not clear; thus, the explanation of some results obtained using this model is only "conditional".

While neither of these two models can explain all the experimental data obtained in this work consistently, some aspects did become clearer. One of them is that the existence of a layered or superlattice structure is essential for low power switching. However, a particular role of this structure has not been fully clarified yet. Various factors can be considered here such as the interfaces between multiple layers or the internal stress generated by the stratification of different materials.

The roles of the internal stress in phase change phenomenon have been reported in some previous reports\textsuperscript{19,20,29,30}. Though these studies focus on crystallization from the amorphous phase whose mechanism might not be applied to SL materials, similar discussions might be applied in common from the view point of the atomic mobility. It has been reported that the switching power decreases with decreasing number of SL layers, and its extremely low value (about $10^{-4}$ of that of GST\textsuperscript{225}) is observed for single-layered SnTeSL as shown in Fig. 15. It can be thought that the internal stress is higher in a thinner heterostructure film because a thinner film cannot relax the internal stress sufficiently. However, since no direct stress measurements were obtained to support any of these hypotheses, additional studies in this area must be performed.

The effect of the interfaces has also been discussed.
Simpson et al\textsuperscript{[5]} suggested that the interface between the GeTe and Sb\textsubscript{2}Te\textsubscript{3} layers produced the greatest effect, whereas Ohyanagi et al\textsuperscript{[15]} stressed the importance of the top layer of the SL material. Since no results were obtained to support any of these hypotheses, additional studies in this area must be performed.

As shown in Table\textsuperscript{[1]} no consistent model fully describing the resistance switching process in phase change SL materials has been developed yet. Hence, either a combination of the two models discussed above or a completely different mechanism must be considered. Additional macroscopic and microscopic studies are required for elucidating the resistance switching mechanism in SL materials and their practical use for manufacturing low power switching devices.

Next, the difference between GeTeSL and SnTeSL is discussed. Though the mechanism of the resistance switching in SL devices is still unclear, it might be thought that the same principle works for both SL materials because the experimental results shown in Fig.\textsuperscript{[7]} Fig.\textsuperscript{[10]} and Fig.\textsuperscript{[10]} which exhibit the essential differences from GST225, are qualitatively common to both SL materials. Recently the effect of van der Waals gaps in GST or GeTeSL has been discussed in relation to low power switching in GeTeSL\textsuperscript{[21,22,33,34]}. These discussions might be applicable also to SnTeSL because, as already shown and discussed, the TEM images in Fig.\textsuperscript{[14]} show that the devices which show low power switching contain the vacancy layers which are considered as van der Waals gaps while this vacancy layer is not observed in the broken device which does not exhibit low power switching. Thus, as in GeTeSL devices, this vacancy layer (possibly van der Waals gap) might possibly be the essential cause of low power switching. If van der Waals gap is modulated easily by the electric field, the electric field induced model can be supported. The vacancy layer observed in SnTeSL, however, has not been proved to be van der Waals gap. Moreover, it is controversial whether the multilevel resistances shown in Fig.\textsuperscript{[16]} can be explained in terms of van der Waals gap. Further studies are necessary from these points of view.

Lastly the perspectives of phase change SL materials are discussed. Though this paper has reported some advantages of SnTeSL material, there remain some issues to be solved, especially i) the instability of the unstable endurance property (Fig.\textsuperscript{[5]}, ii) the variation of the initial resistance (Fig.\textsuperscript{[7]}, iii) the retention property predicted by the thermal property (Fig.\textsuperscript{[11]}, and iv) the power consumed for resistance switching in smaller cells in connection with non-scalability (Fig.\textsuperscript{[9]}. Though the issues i) and ii) will possibly be solved by the operations such as an initialization algorithm and the adjustment of the formed resistance by verification, it is more desirable for practical use to solve these issues because these operations would take time and electric power to store data. Though the causes of these properties are not clear, they are thought to be related to the conditions of the as-deposited films in the device, which have to be solved by the device design and/or the fabrication processes. One of the possibilities of the cause is the polycrystalline state as shown in Fig.\textsuperscript{[11]} If the initial state was in the well-aligned single crystalline state, there would be no defects which would lead to the initial high resistance and the good endurance property due to the well-controlled generation of the activated regions. Moreover, as already discussed above, these issues might be solved by, for example, controlling the boundary between the electrodes and the SL material as circuitwise in ReRAM\textsuperscript{[23]}. The issue iii) might be solved by, for example, adding some impurity which increases the thermal stability. Addition of impurity, however, increases the reset power in many cases. The atomic species of the impurity which can fulfill these two requirements should be selected carefully, where a detailed clarification of the mechanism of resistance switching in the SL devices will be of great importance. Regarding the issue iv) on the scalability, the property of non-scalability seems to decline the value of SL materials. SnTeSL, however, showed the switching power of $10^{-3}$ $10^{-4}$ compared with GST225 using the cell with the diameter of 100 nm. This means that, by assuming that the switching power is simply proportional to the cell area, the switching power of SnTeSL will be $10^{-1} 10^{-2}$ of that of GST225 if the cell diameter is 10 nm with the higher endurance than GST225. This is still highly advantageous for semiconductor memory industry. However, as described above, one of the serious issues is the retention property. SnTeSL should be investigated further to solve this issue for practical use in the future.

V Conclusions

The fundamental properties of the phase change Superlattice (SL) materials, mainly Sn\textsubscript{x}Te\textsubscript{1−x}/Sb\textsubscript{2}Te\textsubscript{3} SL, were investigated in this work. It was found that their low power switching required a high initial resistance. The switching power of Sn\textsubscript{x}Te\textsubscript{1−x}/Sb\textsubscript{2}Te\textsubscript{3} SL decreased with decreasing $x$ and was equal to about $10^{-3}$ of the value obtained for the Ge\textsubscript{2}Sb\textsubscript{2}Te\textsubscript{5} (GST225) conventional phase change material at $x = 0.1$. During the pulse incidence, the electric current was drastically reduced, while
the switching voltage remained almost equal. The results of experiments conducted using short pulses revealed that a lower electric current was required for switching, while the switching voltage did not depend on the pulse width. The TEM images and experimental data obtained using the alloyed SnTe and Sb$_2$Te$_3$ layers indicate that the presence of a superlattice or a layered structure is essential for low power switching. At the same time, no dependence of the switching power on the cell size (scaling) was observed. Although the electric properties of the SL materials are different from those of the conventional GST materials, their annealing properties are very similar. In addition, multilevel cells were obtained by performing a multi-pulse reset operation. The partial switching and electric field-induced switching (as already proposed elsewhere\cite{10}) models were proposed to explain the experimental results obtained in this study, although none of them was able to explain the experimental results perfectly. Hence, additional studies are required to clarify the mechanism of the resistance switching in SL materials.

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