Systematic and deterministic graph minor embedding for Cartesian products of graphs

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Abstract The limited connectivity of current and next-generation quantum annealers motivates the need for efficient graph minor embedding methods. These methods allow non-native problems to be adapted to the target annealer’s architecture. The overhead of the widely used heuristic techniques is quickly proving to be a significant bottleneck for solving real-world applications. To alleviate this difficulty, we propose a systematic and deterministic embedding method, exploiting the structures of both the specific problem and the quantum annealer. We focus on the specific case of the Cartesian product of two complete graphs, a regular structure that occurs in many problems. We decompose the embedding problem by first embedding one of the factors of the Cartesian product in a repeatable pattern. The resulting simplified problem comprises the placement and connecting together of these copies to reach a valid solution. Aside from the obvious advantage of a systematic and deterministic approach with respect to speed and efficiency, the embeddings produced are easily scaled for larger processors and show desirable properties for the number of qubits used and the chain length distribution. We conclude by briefly addressing the problem of circumventing inoperable qubits by presenting possible extensions of our method.

Keywords Graph minor embedding · Cartesian product · Quantum annealing · Chip architecture
1 Introduction

The majority of the interesting combinatorial optimization problems are hard to solve. Graph similarity, graph partitioning, graph colouring, resource allocation, and scheduling problems are among those combinatorial optimization problems proven to be NP-hard [8,19,27]. Many of these problems have significant real-world applications which make them especially interesting. For example, determining similarities between graphs is a challenging problem that occurs when comparing the structures of different molecules and is thus of great importance in drug design applications [12]. Many of these problems can be formulated as quadratic unconstrained binary optimization (QUBO) problems, which can be solved on specialized quadratic solvers.

One type of quadratic solver which has garnered considerable attention in the past few years is the quantum annealing processor manufactured by D-Wave Systems [14,15]. In essence, the processor is a specialized quantum device that samples low-energy configurations of a set of Ising spin variables \( s \in \{-1, +1\}^n \) that serve as quantum registers or qubits. It is designed to solve a binary input problem formulated as an Ising Hamiltonian specified by a pair \((h, J)\), where \( h \in \mathbb{R}^n \) is a vector of local fields acting on the spin variables and \( J \in \mathbb{R}^{n \times n} \) is a symmetric matrix of quadratic couplings between these spins. The objective function to be minimized is specified by the energy \( E(s) \) of the spin configuration \( s \) and given by

\[
E(s) = E(s, h, J) = s^T J s + s^T h.
\]

We note that an Ising problem can be formulated as a QUBO problem through a simple linear transformation \( x = (s + 1)/2 \). Therefore, the quantum annealer is equivalently considered to be a quadratic unconstrained binary optimizer that minimizes a quadratic objective function \( Q \) given by

\[
E(x) = E(x, Q) = x^T Q x
\]

over the discrete configuration space of a set of qubits \( x \in \{0, 1\}^n \). The D-Wave solver has limited connectivity between its qubits such that not all pairs can be coupled together. In other words, only a subset of the terms of \( J \) or \( Q \) are allowed to be nonzero. For this reason, the structure of the problem to be solved must be mapped to the architecture of the solver, a process called embedding [6] which we define below.

In this paper, we will treat both the input problem and the solver as graphs. An input problem of interest, formulated as either a QUBO or Ising problem, can be represented as a graph \( G = (V, E) \), where \( V \) is a set of vertices representing either the logical variables or physical qubits and \( E \) is a set of edges representing the interactions between them. For the case of an Ising problem, the vertices of this graph are the variables \( s_1, \ldots, s_n \), while the set of edges is created by adding one edge for each pair of vertices \( s_i \) and \( s_j \) for which \( J_{ij} \) is nonzero. On the other hand, the processor’s architecture is described by the hardware graph \( C \). This graph represents the available physical qubits or registers and shows how they are coupled together on the processor. The earlier D-Wave Two’s hardware graph (see Fig. 6) has 512 physical qubits, and each qubit is adjacent to at most 6 others. This nearly regular hardware graph, the
Chimera graph, is denoted by $C_{N,M,L}$ and constructed as an $N \times M$ grid of bipartite blocks $K_{L_1,L_2}$, as defined in [4]. A bipartite block $K_{L_1,L_2}$ is a graph with two sets of vertices of sizes $L_1$ and $L_2$, respectively, where each vertex of each set is connected only to each vertex of the other set.

In order to embed the desired Ising model into the processor, the graph $G$ should be a subgraph of graph $C$. A mapping of the input graph to the target graph is called a direct embedding. Seeking a direct embedding places stringent constraints on the size and connectivity of the input graph. Alternatively, we can seek a graph minor embedding, which is a specific type of mapping where we further allow adjacent vertices of the target graph to be contracted into larger effective vertices, called chains. In this more general case, the graph $G$ should be a subgraph of a graph minor of $C$. For a detailed description of graph minor embedding, see [6]. In simple terms, a chain is created through the addition of strong penalty terms to the objective function such that the variables involved are forced to take the same value. In the Ising formulation, this is achieved by applying a strong ferromagnetic coupling between any two adjacent vertices $i$ and $j$ of $G$ in the same chain\(^1\) (see [17,20,26]).

In the most general case, where no assumption is made about the input and target graphs, seeking a graph minor embedding is an NP-hard problem [5]. Practically, this means that as the size of the graphs increases, the problem of finding a valid embedding quickly becomes prohibitively computationally expensive. To avoid having to solve an NP-hard problem with each embedding, we could use the fact that the structure of the solver is usually known in advance (here, it is a Chimera graph structure possibly less a few inoperable qubits and couplers). This means that polynomial solutions to the embedding problem remain achievable. While such an exact method exists, its poor scaling still renders it unusable for graphs larger than 10 vertices [1]. As a result, the most widely used embedding algorithms, such as the one introduced by Cai et al. [5], are heuristic in nature, compromising on embedding quality in order to achieve polynomial running times with a more favourable scaling. Even then, finding an embedding is typically very time-consuming. This is further exacerbated by other limitations of the analogue quantum device which can lead to highly variable performance, depending on the quality of the embedding, prompting the need to run the heuristic multiple times in order to select the best solution. Although less than ideal, heuristic solutions have proven to be mostly satisfactory for the exploratory work conducted on previous-generation quantum annealers, provided that sufficient computation time could be allocated for embedding. With the recent introduction of a 1000-qubit annealer, however, we are quickly reaching the point where more-scalable solutions are needed. In fact, quantum annealing making the leap from a nascent technology of purely academic interest to a useful mainstream tool is conditional on the availability of fast embedding methods that will not eradicate any potential quantum speed-up.

The most promising next-generation embedding methods should be systematic and scalable. It is unlikely that such properties will be attained for truly general approaches,\(^1\)

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\(^1\) It is worth mentioning that the ferromagnetic coupling between any two adjacent vertices should not be too strong. This is because the parameter range of the annealer is limited, so a very strong coupling will lead to a rescaling of the rest of the problem, which can prove detrimental.
and advances will come by exploiting not only the structure of the target architecture, but also the structure of specific problems. We believe that so long as embedding is needed, although general approaches are useful, it is with application-specific and systematic graph embedding approaches that the full potential of quantum hardware will be realized. The path to better or faster embedding algorithms, therefore, lies in restricting the graph minor embedding problem to specific cases. The triangular embedding of complete graphs [6], later generalized by Boothby et al. [4] approach of fast clique embedding for complete graphs, epitomizes this application-specific approach and creates a systematic embedding for fully connected problems on the Chimera graph architecture. The embeddings produced have equal-length chains and are general because any graph is a subgraph of a complete graph. Unfortunately, this approach is wasteful for applications that do not require a fully connected graph, limiting the size of problems embeddable with this method.

The first step in devising new embedding methods is to identify a common structure across many problems that can be exploited advantageously. As we will show below, a recurring graph structure which appears in the quadratic formulation of many of the NP-hard optimization problems mentioned above is the Cartesian product of two graphs. Cartesian products, being both ubiquitous and highly structured, are attractive targets for the type of improved methods we are advocating. One of the main contributions of this research is the analytical identification of this regularity and structure in the QUBO problem formulation of important families of NP-hard optimization problems. One of the most important advantages of this contribution is that it enables us to reuse the found embeddings for problems with similar structures. The ability to reuse embeddings reduces the computational complexity of the embedding process to a one-time cost per family of problems.

In this paper, we describe a procedure for embedding a Cartesian product of two graphs into a Chimera graph. The vertex set of the Cartesian product $G_1 \square G_2$ of two graphs $G_1 = (V_1, E_1)$ and $G_2 = (V_2, E_2)$ is the Cartesian product of the vertex sets of the individual graphs. In the resulting graph, two vertices $(v_1, v_2)$ and $(u_1, u_2)$ are adjacent if and only if $v_1 = u_1$ and $v_2$ is adjacent to $u_2$ or $v_2 = u_2$ and $v_1$ is adjacent to $u_1$ (see p. 154 of [9]). Denoting the adjacency matrices of graphs $G_1$ and $G_2$ by $A_1$ and $A_2$, and having $n_1 := |V_1|$ and $n_2 := |V_2|$, we can compute the adjacency matrix of $G_1 \square G_2$, that is, $A_{G_1 \square G_2}$, in terms of the adjacency matrices of $G_1$ and $G_2$ as follows:

$$A_{G_1 \square G_2} = I_{n_1} \otimes A_{G_2} + A_{G_1} \otimes I_{n_2}$$  \hspace{1cm} (3)

For the sake of generality with respect to embedding, for the remainder of this paper, we look into the Cartesian product of complete graphs.

2 Identifying the Cartesian product of complete graphs (CPCG)

The Cartesian product of graphs can appear in many application-driven problems (see [7,8,11,23,27]). To exploit this structure, however, we first need to either infer its presence from the problem’s QUBO form or preserve it as we formulate the problem.
from the outset. An alternative structure-preserving QUBO problem formulation can be found in [2]. Very efficient algorithms for identifying Cartesian products in arbitrary graphs have been proposed. For example, Imrich and Peterin [13] proposed an exact algorithm with linear scaling in terms of the number of edges for both the running time and memory requirement by using a clever edge-labelling technique. Nevertheless, it is useful to look at how Cartesian products occur when formulating optimization problems where doubly indexed binary variables are used. This is what we consider below.

Suppose we have a QUBO problem where the variables are doubly indexed binary variables $x_{ik}$, where $1 \leq i \leq N$ and $1 \leq k \leq K$. Such a structure occurs, for example, in the $K$-way graph partitioning problem. We formulate this graph partitioning problem as follows. Given a graph $G = (V, E)$ with $N$ vertices, we want to divide the vertex set into $K$ partitions, where $K$ is a positive integer, such that the sum of the number of edges inside the partitions is maximized. Let $A$ be the adjacency matrix of the graph $G$ built from the edge set $E$. For every vertex $i$ and partition $k$, the optimization variable $x_{ik}$ is 1 if vertex $i$ is in partition $k$, and 0 otherwise. Furthermore, without loss of generality, we assume that $N$ is divisible by $K$, and we let $P = N/K$. The objective is to find the assignment of vertices to partitions (i.e. a 0–1 configuration of $x_{ik}$’s) that maximizes the number of intra-partition edges and satisfies the following constraints:

1. **Orthogonality constraint** each vertex must be assigned to one and only one partition
2. **Cardinality constraint** each partition must have the same number of vertices assigned to it

We note that for the case where $N$ is not divisible by $K$, the second constraint is relaxed such that the size of each partition should not differ from all others by more than one vertex. This problem can be formulated as the following optimization problem:

$$\max_{x=\{x_{ik}\}} \sum_{k=1}^{K} \left( \sum_{(i_1, i_2) \in E} x_{i_1 k} x_{i_2 k} \right)$$

subject to:

$$\sum_{i=1}^{N} x_{ik} = P, \quad \forall \ 1 \leq k \leq K$$

$$\sum_{k=1}^{K} x_{ik} = 1, \quad \forall \ 1 \leq i \leq N$$

$$x_{i, k} \in \{0, 1\}, \quad \forall i, k \quad (4)$$

In order to formulate this problem as a QUBO problem appropriate for the annealer, we rewrite the objective function that needed to be maximized into an objective function to be minimized, and implement the equality constraints as quadratic penalty terms. The resulting QUBO problem is equivalent to the previous constrained optimization problem for appropriately chosen penalty constants $A$ and $B$: 

$$x_{i, k} \in \{0, 1\}, \quad \forall i, k \quad (4)$$
Fig. 1 A matrix representation of doubly indexed variables $x_{ik}$ in an example of a $K$-way partitioning problem on a graph with $N$ nodes. The matrix representation illustrates how subsets of variables contribute to specific orthogonality and cardinality constraints.

\[
\begin{align*}
\min_{x=\{x_{ik}\}} & \left[ -\sum_{k=1}^{K} \sum_{(i_1,i_2)\in E} x_{i_1k}x_{i_2k} + A \sum_{k=1}^{K} \left( \sum_{i=1}^{N} x_{ik} - P \right)^2 \\
& + B \sum_{i=1}^{N} \left( \sum_{k=1}^{K} x_{ik} - 1 \right)^2 \right] \\
& \text{cardinality constraints} \\
& \sum_{k=1}^{K} x_{1k} = 1 \quad \sum_{k=1}^{K} x_{2k} = 1 \quad \sum_{k=1}^{K} x_{Nk} = 1 \\
& \text{orthogonality constraints} \\
& A \sum_{k=1}^{K} \left( \sum_{i=1}^{N} x_{ik} - P \right)^2
\end{align*}
\]  

The Cartesian product’s structure is easily observed by constructing the QUBO problem graph for this partitioning problem. It can be built by reading the above QUBO objective function directly. The QUBO problem graph has a vertex for each doubly indexed binary variable, and an edge for each quadratic term of the objective function. The following quadratic terms are found:

1. For a fixed $k$, the first summation creates a quadratic term $x_{i_1k}x_{i_2k}$ if $(i_1, i_2) \in E$.
2. For a fixed $k$, the second summation creates a quadratic term $x_{i_1k}x_{i_2k}$ for all $1 \leq i_1 < i_2 \leq N$ (after expanding the square of the sum).
3. For a fixed $i$, the third summation creates a quadratic term $x_{ik}x_{ik'}$ for all $1 \leq k < k' \leq K$ (after expanding the square of the sum).

This correspondence between the quadratic terms and the edges in the QUBO problem graph results in the fact that any subset of vertices corresponding to a fixed $i$ or $k$ induces a complete graph on the problem graph. From this, we conclude that the resulting QUBO problem graph is a Cartesian product of two complete graphs $K_N \square K_K$. Figure 1 shows how grouping terms for a fixed partition $k$ and for a fixed vertex $i$ can assist in identifying the structure in the final QUBO formulation.
A similar argument can be used for any other input problem with doubly indexed variables to identify whether there exists a product graph structure in the resulting QUBO problem graph. In general, an input problem with doubly indexed variables where the objective function and constraints are defined on subsets of variables where one index is fixed will end up with QUBO problem graphs which are subgraphs of Cartesian products of complete graphs. Graph partitioning, graph colouring, and size-constrained clustering are important examples of such problems. In addition to these problems, Cartesian product structures have applications in error correction for adiabatic quantum computation. Recent research has shown that using the Cartesian product of graphs as an error-correcting scheme reduces the time to solution for certain families of problems [28].

Thus far, we have focused exclusively on Cartesian products of two complete graphs. We note, however, that the method presented by Imrich and Peterin [13] works for higher-dimensional products as well. Similarly, the identification of Cartesian products with multiply indexed variables with similar constraints for each index would proceed in essentially the same fashion. Indeed, the Cartesian product of graphs is commutative and associative. This means that we can group factors into a smaller number of factors for embedding purposes. For example, in the case of a graph $G = G_1 \Box G_2 \Box G_3$, we can group $G_1$ and $G_2$ together as $G_{\text{eff}_1}$ to obtain $G = G_{\text{eff}_1} \Box G_3$. The theoretical results for the Cartesian products of two graphs presented in the following sections can then easily be generalized to study the case of multiple factors, given a known grouping of the factors into two, by simply multiplying the sizes of the factors in each group.

### 3 Description of CPCG embedding

We have mentioned that a systematic embedding relies in part on the regularity of the target graph’s architecture. Our method is general and can be adapted to different architectures, provided that they can be described as a regular lattice of unit cells. Nevertheless, it will be convenient to restrict the presentation of our method to a specific case. The Chimera hardware graph is the obvious choice, as it describes the architecture of the only commercially available quantum annealer. The D-Wave Two processor uses a 512-qubit Chimera graph $C_{8,8,4}$, and the newer D-Wave 2× uses a 1152-qubit Chimera graph $C_{12,12,4}$.

The dimensionality of the lattice determines how many factors the product to be embedded can have. Since the Chimera graph structure is conveniently described by a two-dimensional lattice, we consider the Cartesian product of two complete graphs with sizes $m$ and $n$, that is, $K_m \Box K_n$, as the input graph. It is noteworthy that $K_m \Box K_n$ has $n$ distinct copies of $K_m$ as well as $m$ distinct copies of $K_n$ as induced subgraphs. We propose to first embed one copy of either $K_m$ or $K_n$, say $K_m$, into a repeatable unit which we call a *nexus*. More precisely, a nexus consists of a collection of adjacent unit cells of the Chimera graph. The regularity of the grid architecture then allows for the embedding of $n$ copies of $K_m$ by simply placing one *nexus instance* on the grid for each of them. We are left with the problem of choosing the exact placement of these instances and connecting them together to realize the full Cartesian product. We call
these inter-nexus connections buses and their arrangement the bus configuration. We have thus not only chosen a simpler high-level description of the original embedding problem, but also implicitly decomposed the problem into two subproblems: the nexus selection, and the nexus instances and bus configuration. We will now look at these subproblems in more detail and describe how they can be implemented to also achieve a scalable embedding strategy with advantageous properties.

We use the specific case of embedding $K_8 \square K_n$ on $C_{N,N,4}$ as a demonstration. Figure 2a shows how three adjacent unit cells of the Chimera graph, along with their couplers, are used for embedding $K_8$, and constitutes our preferred choice of nexus for hosting $K_8$. This embedding is essentially the same as the default triangular embedding for $K_8$ [15]. Figure 2b illustrates an embedding pattern based on this choice of nexus and how buses were placed to realize $K_8 \square K_7$ on $C_{8,8,4}$.

### 3.1 Nexus selection

The nexus shape depends on the structure of the graph to be embedded as well as on the Chimera graph’s architecture. Embedding a nexus can be viewed as a much smaller embedding problem with some added constraints pertaining to providing the appropriate connections to all variables through dedicated bus interfaces. The definition of these interfaces allows some level of encapsulation by abstracting away the
details of the nexus embedding for the rest of the method. On the target architecture, an interface is a high-level object that stands for the couplers coming out of the nexus and an indication of which variables are attached to them. In the high-level description, on the other hand, it serves as an attachment point for a bus extending a specific set of variables. Redundant interfaces can be defined if needed. It is important to note that the definition of the nexus interfaces will determine the optimal nexus placement and bus configuration. We can therefore seek a nexus and then list the interfaces available, or we can require a set of interfaces as a constraint. To demonstrate the method, we require only that all variables be accessible through an interface, leaving more-advanced considerations for future work.

Solving the limited problem of finding a valid nexus could potentially benefit from other known embedding techniques, including heuristics methods. For the case at hand, embedding a complete graph on as few Chimera blocks as possible, the triangular embedding algorithm proposed in [15] represents an attractive option. This choice exploits the Chimera graph’s large automorphism group (see [5]) and its resulting high level of symmetry. Figure 2a shows that for a Chimera graph with \( L = 4 \), three adjacent unit cells are sufficient to build a nexus for \( K_8 \). The bipartite nature of the Chimera block naturally partitions the set of variables corresponding to the nodes of \( K_8 \) into two subsets, each having four redundant interfaces: two that face downward and to the left and two that face upward and to the right. For example, we partition the corresponding vertex set \( \{A_1, \ldots, A_8\} \) of the \( K_8 \) nexus shown in Fig. 2a into two subsets \( \{A_1, A_2, A_3, A_4\} \) and \( \{A_5, A_6, A_7, A_8\} \).

Each subset of variables is assigned a number of redundant interfaces available for building the inter-nexus connections. An interface is therefore a set of connection points, called terminals, corresponding to the variables of the subset and placed on a specific face of the nexus. For example, in Fig. 2a, a vertical bus connects to an interface representing the subset of variables \( \{A_5, A_6, A_7, A_8\} \) and extend them downward, and a horizontal bus connects to a second interface on the same subset and extends them leftward. Similarly, two buses extend the subset \( \{A_1, A_2, A_3, A_4\} \) in the opposite directions.

### 3.2 Nexus instance placement and bus configuration

We have slightly simplified the embedding problem by introducing a high-level description involving nexuses and buses. We now need to solve that high-level problem. Fortunately, the number of degrees of freedom has been greatly reduced compared to that of the original problem. A tailored search algorithm can be implemented based on tabu search or simulated annealing, for example. The allowed steps or updates in configuration spaces are easily derived from the target architecture and its symmetries. We leave such a general solution for future work, however, and focus on a systematic method that works very well for embedding complete graphs on the Chimera architecture, inspired in part by the rooks problem [16]. A rook is a chess piece and the rooks problem is the problem of putting as many non-attacking rooks on an \( n \) by \( n \) chessboard. The maximum number is \( n \) and there are \( n! \) ways to arrange \( n \) non-attacking rooks on the board. The trivial solution to the problem is to put all of the rooks on the
diagonal. We will see below how this solution can be used in the problem of placing nexuses on the Chimera graph.

We call the area of the Chimera graph not occupied by nexus instances the bus space. First introduced near the beginning of Sect. 3, a bus, more precisely, is a set of parallel paths leaving from a nexus interface, with one path per variable (see Fig. 2b). Each path is assigned to a specific variable. Two buses can be linked together at a bus junction. Locating the nexus instances hosting multiple copies of the complete graph $K_m$ on the diagonal of the Chimera graph divides the bus space into disjoint bus spaces. A unit cell of the Chimera graph where two buses meet can be used as a junction.

The Chimera graph’s bipartite structure and the proposed triangular embedding naturally invite a partitioning of the variables of $K_m$ into two subsets. We therefore seek a placement of the nexus instances along a line that would divide the bus space into two bus subspaces, providing access to both subspaces to each nexus instance. The L-shape of the nexus also lends itself to a more efficient tiling if we place these instances along the diagonal of the Chimera graph.

We can now make the connection to the rooks problem and its diagonal solution. The Cartesian product structure of the CPCG problem requires that all corresponding variables be connected. Therefore, in our nexus and bus model there should be a path between any two corresponding variables from any two nexuses. In other words, nexuses should be placed in a way that does not block the paths needed for connecting other nexuses through the bus space. If we imagine that nexuses are rooks and the blocks of the Chimera graph are the chessboard, then the problem of placing non-blocking nexuses is analogous to the problem of placing non-attacking rooks.

Next, we need to extend the nexus interfaces to build the connectivity required by the full Cartesian product. For each subspace, this implies connecting each nexus instance through one of its interfaces to an interface of each other nexus instance in the same subspace. A valid configuration inspired by the rooks problem is to attach both a vertical and a horizontal bus that run to the edge of the chip. This creates a rectilinear grid where each pair of nexus instances meets at a single unit cell. We use each of the created disjoint bus spaces to establish the required connections for copies of $K_n$ in $K_m \Box K_n$. This embedding of copies of $K_n$ is achieved in a distributed manner through the buses, as opposed to the copies of $K_m$ that are fairly localized and encapsulated in a nexus.

We note that when attempting to embed $K_m \Box K_n$, it may happen that using the nexus for one of the complete graphs does not result in a valid embedding, while the other choice gives an appropriate embedding of the product. We simply choose the most promising graph and call it $K_m$ without loss of generality. Similarly, in the case where the product of graphs has more than two factors, different groupings of these factors into two can lead to different results.

Finally, we reiterate that the CPCG method can be applied to embed Cartesian products in other target architectures. The need to base the method on the specific structure at hand limits our ability to provide details on such hypothetical implementations. However, the focus on defining a high-level description, such as a lattice to describe the target architecture, and reusable structures such as nexuses and buses with capacities, is meant to facilitate the process of adapting the method and thus extend its applicability, despite its clear reliance on the specifics of a particular embedding problem.
4 Discussion

In this section, we show the clear advantage of the CPCG embedding method, *CPCG embedding*, over other embedding algorithms with respect to embedding success rates and the quality of the embeddings achieved. We then prove for a specific case that CPCG embedding is optimal with respect to the largest embeddable problem, before commenting on the scaling of the running time of the method. We begin by assuming the Chimera structure is perfectly regular (i.e. it has no inoperable qubits or couplers). The effect of irregularities is investigated in the next section.

4.1 Comparison to other embedding algorithms

To showcase the advantages of our method, we compare it to the de facto heuristic method introduced by Cai et al. [5]. The implementation of this embedding algorithm, `find_embedding()`, is distributed with D-Wave’s API and software tools. This function receives both the problem to be embedded and the target solver’s graph as inputs, making no assumptions about either of them. Given the NP-hardness of the embedding problem and the poor scaling of the polynomial methods when fixing the target graph, `find_embedding()` remains the only viable truly general alternative. The generality of the heuristic approach also has some added benefits when inoperable qubits are present, a topic that will be discussed in the next section. Since the Cartesian product of graphs $K_m$ and $K_n$ is a subset of a complete graph $K_{mn}$, the triangular systematic embedding method [6] provides a simple, yet wasteful, approach to embedding Cartesian products and will therefore serve as our second touchstone.

We will restrict our comparison to the specific case of embedding Cartesian products of the form $K_8 \Box K_n$ into a square Chimera target architecture $C_{N,N,4}$ made of an $N$ by $N$ array of bipartite blocks of 8 qubits ($K_4,4$). The `find_embedding()` method is a multi-start heuristic with a number of parameters to be specified. The algorithm will keep searching until a valid embedding is found or until it reaches one of its stopping criteria. The most important parameter is the maximum running time allowed for the search, which we set to one of 1, 100, or 1000 s. Each restart of the search is initiated when a maximum number of steps are reached without observing an improvement. We leave this at its default value of 10 steps. We further ensure that the search is not stopped prematurely (i.e. before the maximum running time) by setting the maximum number of restarts to a large value (e.g. 10,000 restarts given that each one takes at least 1 s).

In our comparison, we first consider the embedding success rate of the various methods as shown in Fig. 3. In the case of CPCG embedding and the triangular embedding, the success rate is simply 1.0 for all sizes smaller than some maximal size, which we can express as a function of the size $N$ of a square Chimera graph $C_{N,N,4}$. CPCG embedding can embed up to $K_8 \Box K_{N-1}$, which means that $n = 7$ is the largest case with a success rate of 1.0 for a 512-qubit chip and $n = 15$ is the largest case with that success rate for the announced next-generation 2048-qubit chip. Beyond these sizes the success rate is 0. Similarly, for triangular embedding, we can embed up to $K_8 \Box K_{N/2}$, which results in a success rate of 1.0 for $n \leq 4$ ($n \leq 8$).
The embedding success rate for embedding Cartesian products of complete graphs using `find_embedding()` (for 1000 s in light blue, 100 s in grey, and 1 s in yellow), the full triangular embedding (orange), and our systematic CPCG embedding (dark blue) for the case of $K_8 \Box K_n$ as a function of $n$. The last two are assumed to be produced in much less than a second. \(a\) results for the ideal case of the previous chip’s 512-qubit architecture $C_{8,8,4}$, \(b\) results for the announced 2048-qubit ideal Chimera architecture $C_{16,16,4}$ (Color figure online)

into a 512-qubit (2048-qubit) chip, and 0 otherwise. Since the results obtained from `find_embedding()` are probabilistic, we attempt to embed each problem size 100 times for each maximum running time considered. For short running times, we find a satisfactory success rate only for the smallest problem sizes. We can increase that probability somewhat by increasing the running time, but even a generous 1000 s will not be sufficient to embed the largest Cartesian products achievable with CPCG embedding. Aside from the obvious effect of the poor scaling of the running time of `find_embedding()` on the success rate, we also observe the limiting effect of the target chip’s size for a fixed running time. As we get closer to the maximum embeddable problem size for a specific chip size, the success rate is further reduced. The product $K_8 \Box K_6$, for example, is easily embeddable into a 2048-qubit chip, but only succeeds 18% of the time with a 1000 s running time on the 512-qubit chip. With limited chip size also comes a limited number of valid solutions, so the probability of finding a valid solution is lower. In other words, the success rate obtained with the `find_embedding()` method will get worse as the technology scales and we begin to address larger problem instances, but even more so when we test the limits of a specific architecture. CPCG embedding is clearly the superior choice for a perfect Chimera chip (i.e. one where all qubits are operable), as it can embed products far larger than the two alternatives in a very short time. We discuss the scaling of running time in...
Fig. 4 Average number of qubits used for embedding Cartesian products of complete graphs for the case of $K_8 \Box K_n$ as a function of $n$ into a 2048-qubit architecture $C_{16,16,4}$. Results are shown for D-Wave's `find_embedding()` heuristic (in red), the full triangular embedding (orange), and our systematic CPCG embedding (dark blue). A fit for the averaged number of qubits used in embeddings produced by `find_embedding()` and given by $16.63n^2 - 11.01n + 5.75$ is shown with a dashed red line (Color figure online)

more detail in Sect. 4.3. In fact, we can even show in some cases that CPCG embedding can embed the largest possible Cartesian product of complete graphs embeddable for a target chip size (see the next section on the discussion of optimality).

Beyond the ability to embed a problem into a chip, the quality of the embedding is paramount. Benchmarking for various types of optimization problems can show a difference of a few orders of magnitude between different embeddings of the same problem. At this point, there exists no single first-principle metric to rate embedding quality. Empirical ratings such as the metric used in [22] represent the most practical embedding quality metric at this point. Nevertheless, quantum annealing practitioners have used the number of physical qubits or the length of the longest chain as a conjectural measure of the embedding quality [5]. It has also been suggested that having heterogeneous chain lengths in an embedding is disadvantageous since the chains tend to exhibit unpredictable chain dynamics throughout the annealing process [4,26]. Clarifying the relative role of these various properties in determining the quality of an embedding is beyond the scope of this paper, so we will limit our comparison to the traditional indicators by comparing the number of physical qubits and the chain length distribution of the CPCG embedding with the other alternatives.

The number of physical qubits used is shown in Fig. 4, and the chain length distribution is shown in Fig. 5. CPCG embedding for an ideal Chimera graph for $K_8 \Box K_n$ produces chains of length $n + 2$. With $8n$ logical variables, the embedding uses a total of $8n(n + 2)$ physical qubits. In comparison, a triangular embedding
Fig. 5 Chain length for embedding Cartesian products of complete graphs for the case of $K_8 \boxtimes K_n$ as a function of $n$ into a 2048-qubit architecture $C_{16,16,4}$. Results are shown for D-Wave’s `find_embedding()` heuristic (in red and yellow), the full triangular embedding (orange), and our systematic CPCG embedding (dark blue). The latter two produce embeddings with chains that are all of equal length, shown as a single line. The spread of chain lengths produced by `find_embedding()` is illustrated by averaging the mean (central red line), maximum (upper yellow line), and minimum (lower yellow line) chain length over 100 embeddings. The average standard deviation (also in red) of the chain length is also shown such that the red shaded region illustrates where 65% of the chains can typically be found. A fit for the averaged maximum chain length is given by $0.12n^2 + 1.91n - 0.48$ (dashed yellow line) and a fit for the averaged mean chain length is given by $2.05n - 1.06$ (dashed red line) (Color figure online).

for a complete graph $K_{8n}$ has chains of length $2n + 1$ for a total number of physical qubits used equal to $8n(2n + 1)$. This is twice that of CPCG embedding in the asymptotic limit. Both of these embedding methods produce equal-length chains. The `find_embedding()` method, on the other hand, produces a spread of chain lengths for each successful embedding found. To illustrate this distribution, we average the mean, the minimum, and the maximum chain lengths over the 100 embeddings found. The average standard deviation is also shown such that 65% of the chains produced are found in the red shaded region. Results depend only marginally on the maximum running time, provided that it is long enough to find a valid embedding, so we allowed for a generous 1000 s. A quadratic function fit of the averaged number of qubits used is given by $16.63n^2 - 11.01n + 5.75$, and a fit for the averaged mean chain length is given by $2.05n - 1.06$. In the asymptotic limit, therefore, CPCG embedding produces chains that are less than half of the mean length produced by `find_embedding()`. Consequently, we observe that the required number of qubits is also less than half that of the number of qubits required by `find_embedding()`. Although `find_embedding()` found some embeddings for $K_8 \boxtimes K_{11}$, the statistics
are not shown as they were artificially skewed due to the smaller number of embeddings found.

We find that CPCG embedding behaves and scales favourably compared to both the heuristic method of `find_embedding()` and the systematic triangular embedding. It can embed larger products on chips of the same size while producing shorter chains of equal length.

### 4.2 Discussion of optimality

Having shown that CPCG embedding compares favourably against other techniques, in the following theorem we prove its optimality for certain cases.

We use the notions of the treewidth and bramble of undirected graphs. A tree decomposition of a graph $G = (V, E)$ is a pair $(T, X)$ where $T$ is a tree, $X = (X_t : t \in V(T))$, and each $X_t$ is a subset of $V$ such that

1. Every edge of $G$ has both endpoints in some $X_t$ and $\bigcup_{t \in V(T)} X_t = V$.
2. If $X_t$ and $X_{t'}$ both contain a vertex $v \in V(G)$, then all subsets $X_{t''}$ in the unique path between $X_t$ and $X_{t'}$ contain the vertex $v$ as well.

The width of a tree decomposition $(T, W)$ is defined as

$$\max\{|X_t| - 1 : t \in V(T)\},$$

and the treewidth $t \! w(G)$ of $G$ is the minimum width among all possible tree decompositions of $G$. For a detailed description of the `asdf`treewidth of a graph, see [25].

A bramble for an undirected graph $G$ is a family of connected subgraphs of $G$ such that any pair of these subgraphs have a non-empty intersection or there is an edge with one endpoint in each of them. The order of a bramble is the minimum number of vertices covering all subgraphs in the bramble. Seymour and Thomas proved [24] that a graph $G$ has a bramble of the order $k$ if and only if $t \! w(G) = k - 1$ (see also [10]).

**Theorem 1** Let $N$ be the smallest number such that CPCG embedding can embed $K_m \boxtimes K_n$ into the square Chimera graph architecture $C_{N,N,L}$. If one of $m$ and $n$ is divisible by $2L$ and the other one is odd, then this embedding is optimal in the sense that $K_m \boxtimes K_n$ cannot be embedded into a smaller square Chimera graph.

**Proof** By symmetry, we may assume that $2L$ divides $m$ and $n$ is odd. Let us choose $K_m$ to be the graph embedded in a nexus. By placing the nexuses on the diagonal, CPCG embedding described in the previous section embeds $K_m \boxtimes K_n$ into $C_{N,N,L}$, where

$$N = \left\lceil \frac{m}{L} \right\rceil (n - 1) + \left\lceil \frac{m}{L} \right\rceil = m(n + 1)/(2L).$$

Now suppose that $K_m \boxtimes K_n$ can be embedded into $C_{N',N',L}$. To prove optimality we need only show that $N' \geq N$. 

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The proof uses a treewidth argument. Let \( \text{tw}(G) \) denote the treewidth of a graph \( G \). Since \( K_m \square K_n \) can be embedded into \( C_{N',N',L} \), the former graph is a minor of the latter, so we have the following inequality between their treewidths:

\[
\text{tw}(K_m \square K_n) \leq \text{tw}(C_{N',N',L}). \tag{7}
\]

On the one hand, since \( n \) is odd, we can construct a bramble similar to that given in the proof of [18, Lemma 3.2] to show that

\[
m(n + 1)/2 - 1 \leq \text{tw}(K_m \square K_n). \tag{8}
\]

On the other hand, the treewidth of \( C_{N',N',L} \) is known to be \( N'L \). Indeed, using the triangular embedding method of [6], one can embed the complete graph \( K_{N'L+1} \) into \( C_{N',N',L} \). Thus, we have

\[
\text{tw}(K_{N'L+1}) = N'L \leq \text{tw}(C_{N',N',L}).
\]

Therefore, it suffices to show that \( \text{tw}(C_{N',N',L}) \leq N'L \). From Theorem 6 of [3], \( \text{tw}(C_{N',N',L}) \leq N'L \) if and only if there exists an elimination ordering \( \pi \) such that the triangulation of \( C_{N',N',L} \) with respect to \( \pi \) has a maximum clique of size at most \( N'L + 1 \). The suggested elimination ordering \( \pi \) is as follows. For each row \( i = 1, \ldots, N' \) of \( C_{N',N',L} \), we first eliminate all vertices that correspond to vertical qubits for each column \( j = 1, \ldots, N' \), and then eliminate all vertices that correspond to horizontal qubits for each column \( j = 1, \ldots, N' \).²

Combining these two treewidth results with (7) gives

\[
m(n + 1)/2 - 1 \leq N'L,
\]

which means that

\[
N' \geq m(n + 1)/(2L) - 1/L = N - 1/L.
\]

But since \( L > 1 \) and \( N \) and \( N' \) are positive integers, this implies that \( N' \geq N \), as required.

We believe that the result above also holds for \( K_m \square K_n \), where \( m \) is divisible by \( 2L \) and \( n \geq m \). However, the proof will require a complicated adaptation of the ideas given in [18, Lemma 3.2] that is beyond the scope of this paper.

As a concrete example, we consider the Chimera structure \( C_{8,8,4} \) corresponding to a 512-qubit chip. We know that CPCG embedding can embed \( K_8 \square K_7 \), and, consequently, any product of the form \( K_m \square K_n \), where \( m \leq 8 \) and \( n \leq 7 \). Indeed, the treewidth of \( C_{8,8,4} \) is 32, and \( K_8 \square K_7 \) has a treewidth smaller than or equal to 31 and is therefore embeddable, whereas any product of the form \( K_8 \square K_n \) with \( n > 7 \) must have a treewidth of at least 35 and is not embeddable.

² This argument is due to Marshall Drew-Brook, and we would like to thank Aidan Roy for pointing it out to us.
4.3 Running time

We may assume that the input to our algorithm is a polynomial in doubly indexed variables. For example, in the problem of colouring a graph of \( n \) vertices with \( m \) colours, the quadratic formulation of the problem contains a polynomial in the variables \( x_{ij} \), with \( i \in \{1, \ldots, n\} \) and \( j \in \{1, \ldots, m\} \). Then, we consider the Cartesian product of two complete graphs \( K_m \square K_n \) to be embedded into a Chimera graph.

In order to identify the appropriate complete graphs whose Cartesian product contains the input graph, we need \( O(n^2m^2) \) operations. Furthermore, from our proposed algorithm, the total number of operations needed to embed a Cartesian product \( K_m \square K_n \) into a Chimera graph is \( O(n^2m^2) \). It is worth mentioning that if we consider the input to be a graph with \( e \) edges, the number of operations needed to identify an appropriate Cartesian product of two complete graphs is \( O(e) \).

Now suppose a graph \( H \) is to be embedded into a graph \( G \), and both of them are the inputs to the embedding algorithm proposed by [5]. Let \( n_H \) and \( e_H \) denote the number of vertices and edges of graph \( H \), and \( n_G \) and \( e_G \) be the number of vertices and edges of graph \( G \), respectively. The running time of the algorithm in [5] is \( O(n_H n_G e_H (e_G + n_G \log n_G)) \).

5 Fault tolerance and extensions

One key to our low-complexity scalable algorithm is to make use of the lattice-like regularity in the target Chimera graph. Although the numerical results show significant improvement over general heuristics used for embedding into a perfectly regular Chimera graph, we have thus far not accounted for potential defects and their impact on CPCG embedding. One can, of course, argue that such defects are merely a temporary nuisance which will eventually be eliminated as the technology matures. Nevertheless, for the method to be of immediate practical use, the general case of a target graph with inoperable qubits and couplers must be considered. Unfortunately, these inoperable qubits break the perfect regularity of the Chimera graph, the very feature on which our approach is based. Figure 6 depicts an actual instance of a D-Wave chip with inoperable qubits. This chip with a Chimera structure \( C_{8,8,4} \) with 509 working qubits was installed at NASA’s Ames Research Center [21] and later replaced by a newer D-Wave 2 \( \times \) system. To address the issue of immediate applicability, we present simple cases where the current method can be applied unchanged. We then introduce a modified method that can be used despite the presence of a small number of inoperable components, and compare the results to other embedding methods.

We then provide some guidance on how the CPCG methods presented in this paper can be applied in the context of different hardware architectures and how the resulting patterns can be used to gain insight for future architectures.

5.1 Vanilla method in the presence of faults

Despite the fact that currently available quantum chips having a number of inoperable components, there are some simple ways in which the method presented above for
perfectly regular target architectures can remain useful. We describe two of them here.

One approach involves selecting a smaller subgraph of the target architecture that does not have any inoperable components. For example, a Chimera graph $\mathcal{C}_{N,N,L}$ might have a perfectly working subgraph corresponding to another Chimera graph $\mathcal{C}_{S,S,L}$ with $S < N$. In fact, multiple such perfect sections can usually be identified. It is true that the size of the graph embeddable in the subgraph can be much smaller than the largest embeddable Cartesian product of complete graphs, but the predictable properties of the resulting CPCG embedding method make it a desirable choice over other embeddings. Perfect subgraphs of a specific target solver can be identified in advance and used when the size of the problem is small enough to fit in one such subgraph.

Another direct use of the vanilla method is to ignore inoperable components when generating the embedding patterns and then remove the variables that have inoperable components. For example, if we have a pattern for $k_8 \Box k_7$, but one nexus has an inoperable component affecting a single variable, we are left with a valid pattern for $k_7 \Box k_7$. This idea appears straightforward, but its implementation can quickly become
more complicated if we want to maximize the size of the embedded product of graphs. This is because we can sometimes use symmetries of the target architecture to reach a better result. For the Chimera graph, more specifically, beyond the simple reflection symmetries, we can also permute the assignment of the input variable for each nexus individually. The required connections between nexuses remain possible under such permutations because of the bipartite nature of the connection block that joins the buses of two nexuses. This means that, even if each nexus has one inoperable variable, we can still choose a permutation for each nexus such that we are able to remove only one variable from the final product. In other cases, where an inoperable coupler is needed to connect two variables, either within a single nexus or between two nexuses, a choice must be made to remove one of the two variables. Once again, selecting a suitable variable can make a difference in the size of the final product. Given the speed of the CPCG method, one useful approach is to build a list of either all, or a subset of all, of the embedding patterns for a specific target architecture and set of inoperable components, and to store them in a database for future use.

An interesting avenue for future research would be to explore possible ways to fix some inoperable variables by rerouting around a faulty component. These methods would build on the embedding patterns produced with the vanilla method and use free nearby components such as the ones freed by removing other inoperable variables.

5.2 Presentation of the fault-tolerant method

The issue of having inoperable qubits can be addressed at the expense of adding more complexity to our scalable embedding approach. One simple idea is to use the CPCG embedding of the problem on an ideal solver as a starting point and apply small modifications so that a valid embedding that circumvents the irregularities caused by inoperable qubits is reached. We expect that such a solution should achieve reasonable performance on chips with high qubit yields, while a low qubit yield would lead to substantial degradation of both the embeddability and the embedding quality. We describe below how this type of extension can be implemented.

Using the embedding pattern on a perfect chip as a starting point, we address each nexus instance in turn. We begin with the first nexus and look at the capacity of its constituting blocks in each direction. The capacity of block \((i, j)\) in a given direction is denoted by \(c_{\text{direction}}^{i,j}\) where \((i, j)\) are indices on a two-dimensional grid. The block capacities determine how many paths for variables can run through a group of adjacent vertical or horizontal blocks to propagate a set of variables (i.e. the bus capacity). The presence of inoperable qubits along these directions will usually result in a reduced capacity. We then extend the size of the nexus until the relevant blocks along the vertical (horizontal) direction can form a bus with sufficient capacity. Then a variant of triangular embedding is used to embed the same complete graph in the newly extended space for the nexus. As a result of the nexus extension, we need to shift the other nexus instances appropriately. Although we have just described how a nexus extension can circumvent an inoperable qubit along a bus path, this shape modification can also help with embedding a nexus when there are inoperable qubits...
within the nexus boundaries. For lower qubit yields, triangular embedding might fail to embed a nexus instance regardless of the number of shifts and extensions. In such situations, a more complex nexus embedding algorithm should be used to compensate for the high irregularity in the target graph. Figure 7a illustrates how a simple nexus extension can address the problem caused by having an inoperable qubit within the nexus, and Fig. 7b provides a more complete example by showing which modifications need to be performed to embed a $K_8 \Box K_6$ on the specific 509-qubit chip in Fig. 6. As the figure illustrates, the shift-and-extension method is applied to bypass the columns and rows of lower bus capacity caused by inoperable qubits. In the next section, we provide the numerical analysis of the performance of this algorithm compared to the find_embedding() heuristic [5] for this specific chip architecture. The pseudo-code in Algorithm 1 provides a few more details of this proof of concept for this simple fault-tolerant method.

5.3 Comparison to other embedding methods

We have tested the simple fault-tolerant algorithm to embed the family of $K_8 \Box K_n$ problems on the quantum annealer described in Fig. 6. We again compare it to the results produced by the find_embedding() heuristic run for 1000 s and each problem was repeated 100 times to collect statistics. The other parameters used are the same...
Data: Adjacency matrix of the target Chimera graph $A_{C,M,N,L}$ with inoperable qubits, dimensions of the CPCG $(\alpha, \beta)$.

Result: An embedding $E_{(\alpha,\beta)}$ in the target Chimera graph.

Initialization:

$C[i,j] \leftarrow$ Calculate the capacity vector $(c^\text{vertical}, c^\text{horizontal})$ for each block $[i,j]$;

$E^*_{(\alpha,\beta)} \leftarrow$ Load a scalable embedding pattern on the ideal target graph $A^*_{C,M,N,L}$;

for direction $\in$ diagonals do

$\text{(ROW, COL)} \leftarrow$ coordinates of the corner block of the current direction;

for nexus $\in E^*_{(\alpha,\beta)}$ do

$nexus\_shape \leftarrow$ collection of blocks used by $nexus \in E^*_{(\alpha,\beta)}$;

Shift to the current available position $\text{(ROW, COL)}$;

while the nexus is not embedded do

$C_{nexus} \leftarrow$ required capacity by triangular embedding of $nexus$ based on $nexus\_shape$;

if $C[\text{ROW, COL}] < C_{nexus}$ then

extend $\leftarrow$ identify the direction to extend based on $\text{sign}(C_{nexus} - C[\text{ROW, COL}])$;

extend to $(C_{nexus} - C[\text{ROW, COL}])$ blocks towards extend direction;

$nexus\_embeddability \leftarrow$ Call triangular_embedding() on updated $nexus\_shape$;

if $nexus\_embeddability$ then

Locate $nexus$ on $A_{C,M,N,L}$;

Update $E_{(\alpha,\beta)}$ and $\text{(ROW, COL)}$;

continue to next $nexus$;

else

Locate $nexus$ on $A_{C,M,N,L}$;

Update $E_{(\alpha,\beta)}$ and $\text{(ROW, COL)}$;

end

end

end

Algorithm 1: Fault-tolerant CPCG embedding based on shifts and extensions

as in Sect. 4, Figure 7 shows an embedding of the maximum problem size embeddable on this chip with CPCG embedding. The find_embedding() heuristic can also embed this problem size, albeit with a success rate of about 18%. Unsurprisingly, the success rate of a heuristic method such as find_embedding() is not greatly affected by a small number of inoperable qubits. Figure 8 illustrates how the success probability of find_embedding() still drops faster than CPCG embedding with increasing problem size. We expect our previous observation that the advantage of CPCG embedding becomes more prominent for larger chip sizes to hold for high qubit yields. In other words, CPCG embedding should outperform find_embedding() by a larger margin for larger target architectures despite the presence of irregularities caused by a low density of inoperable qubits.

We also note that the embedding quality of CPCG embeddings remains superior with respect to the number of required qubits and chain length distribution. These are compared in Figs. 9 and 10 for the chip with 509 qubits. Here, too, the results are not shown for $K_8 \Box K_6$ for find_embedding() because they were skewed due to a lower embedding success rate. Again, we observe that the find_embedding() heuristic is not very sensitive to this small density of inoperable qubits, as the chain length distribution and qubit counts are almost identical to the ideal case. Given that CPCG embedding relies on the regularity of the target graph, unlike find_embedding(), we unsurprisingly observe a higher sensitivity to the irregu-
Fig. 8 The embedding success rate for embedding Cartesian products of complete graphs into a chip with inoperable qubits using D-Wave’s `find_embedding()` heuristic for 1000s (orange) and our systematic CPCG embedding (dark blue) for the case of $K_8 \Box K_n$ as a function of $n$. The $C_{8,8,4}$ chip used has 509 working qubits out of 512 and is described in Fig. 6. The largest problem embedded by both approaches is $K_8 \Box K_6$ with a success rate of 19% for `find_embedding()` and 100% for CPCG embedding (Color figure online)

Fig. 9 Average number of qubits used for embedding Cartesian products of complete graphs into a chip with inoperable qubits using D-Wave’s `find_embedding()` heuristic for 1000s (red) and our systematic CPCG embedding (dark blue) for the case of $K_8 \Box K_n$ as a function of $n$. The $C_{8,8,4}$ chip used has 509 working qubits out of 512 and is described in Fig. 6. CPCG embedding results for a perfect chip of the same size are also shown (dotted black line) (Color figure online)
Chain length for embedding Cartesian products of complete graphs into a chip with inoperable qubits using D-Wave’s `find_embedding()` heuristic for 1000s (yellow and red) and our systematic CPCG embedding (blue) for the case of $K_8 \Box K_n$ as a function of $n$. The $C_8,8,4$ chip used has 509 working qubits out of 512 and is described in Fig. 6. One CPCG embedding instance for each problem size is shown in blue with the dark blue line showing the average chain length and the shaded blue area representing the spread between the minimum and maximum chain lengths. The spread of chain lengths produced by `find_embedding()` is illustrated by averaging the mean (central red line), maximum (upper yellow line), and minimum (lower yellow line) chain lengths over 100 embeddings. The average standard deviation (also in red) of the chain length is also shown such that the red shaded region illustrates where 65% of the chains can typically be found (Color figure online).

Fig. 10

Fig. 10 Chain length for embedding Cartesian products of complete graphs into a chip with inoperable qubits. This results in some degradation in the embedding quality. The chains in each successful embedding are no longer equal because the algorithm needs to route around inoperable qubits, resulting in the spreading out of the distribution. For the same reason, we observe a larger qubit count for the embeddings on the real chip compared to the ideal case. Despite the changes, both the required number of qubits and the distribution of chain lengths remain significantly superior to `find_embedding()`. It is true that we are considering a high qubit yield, but Figs. 9 and 10 indicate that CPCG embedding still has potentially enough of an advantage over `find_embedding()` to remain the preferable method, even for lower qubit yields. Obviously, a crossing point is expected and methods like `find_embedding()` remain indicated for irregular target graphs.

We included this simple algorithm to show the possibility of modifying our approach to be used for real chips. However, this approach seems intuitively wasteful as it readily discards large blocks of qubits. There exists an obvious trade-off between the complexity of the fault-tolerant embedding algorithm and its performance in terms of embedding success rate and embedding quality. Work on a refined approach, still based
on modifying the ideal CPCG embedding pattern, is ongoing and will be presented elsewhere. We believe that improvements to the techniques described herein should allow us to achieve a higher tolerance to irregularities while preserving most of the desirable features such as running time and embedding properties.

5.4 CPCG-inspired chip architecture

One of the most important applications of the research on minor embedding is to devise better chip architectures to enhance the embeddability of specific problems (or in general). Moreover, application-specific chips might also be of great interest as fabrication challenges are overcome, given that there would be no need to satisfy the constraints involved in embedding general problems. The recurring CPCG structure identified in many optimization problems supports this argument and can serve to guide us towards application-specific chip architectures.

In order to understand how the CPCG embedding patterns can be used to create new architectures, we should again focus on the concepts of nexus and bus. In the context of quantum annealing, a minor embedding identifies certain qubits in a connected subgraph to create an effective qubit, that is, one that has the desired connectivity. In the nexus/bus model, the bus qubits are always added to the nexus qubits in order to extend them, thereby connecting them to other qubits in other nexuses. There are, therefore, certain regions of the chip (i.e. the bus space) that are always used to extend connections between qubits that represent variables in the nexuses. It is intuitive to consider the bus qubits as nothing more than effective wires between the nexus qubits.

Since quantum resources are scarce and difficult to control, it makes sense to use them only when needed. Therefore, regions of the chip that are used exclusively for wiring represent a waste of quantum resources that could be replaced by long-range superconducting couplings. This replacement would achieve the same embeddability for CPCG problems (according to our study), while using far fewer quantum resources and decreasing the area needed for the superconducting and control apparatus required for controlling qubits. Despite all of the advantages, establishing long-range couplings as wires might bring along its own fabrication challenges which would need to be addressed in a separate study.

6 Conclusion

Motivated by several interesting combinatorial problems such as graph colouring and graph partitioning, we proposed a systematic, deterministic, and scalable embedding algorithm for embedding the Cartesian product of two complete graphs into D-Wave Systems’ Chimera hardware graph. To develop this method, we exploited the intrinsic structure of a class of combinatorial optimization problems as well as the structure of the Chimera graph. Although more general (and perforce slower) methods will remain necessary, it is with such application-specific algorithms that the best performance can be achieved and we expect similar studies to follow suit in the near future. In the case of our CPCG embedding algorithm, we not only showed advantageous running time scaling, and how embedding patterns can be cost-effectively scaled up for larger
chip architectures, we also proved CPCG embedding to be optimal in specific cases. Beyond the better embedding success rate achieved, the quality of the embeddings generated, as measured by the usual empirical factors, is superior to other methods. Indeed, CPCG embedding produces equal-length chains on an ideal Chimera chip and uses far fewer physical qubits. Such improvements in the quality of embedding can play a major role in reducing the time to solution when solving problems. Given the algorithm’s reliance on the regularity of the target architecture, it is natural to expect a degradation of performance in the presence of defects. Although we did not explore optimal modifications to the method to handle inoperable qubits and couplers, we presented a simple version of the algorithm for those cases and tested it on the $\hat{C}_{8,8,4}$ 512-qubit NASA chip with 509 working qubits, described in [21]. The results suggest that for high qubit yields, CPCG embedding will retain some advantage in both embedding success rates and quality indicators over more general heuristic methods.

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Compliance with ethical standards

Conflict of interest The authors are employees of 1QBit, a company that has quantum software as one of its areas of focus. D-Wave Systems is a minority investor in 1QBit.

References

1. Adler, I., Dorn, F., Fomin, F.V., Sau, I., Thilikos, D.M.: Faster parameterized algorithms for minor containment. Theor. Comput. Sci. 412(50), 7018–7028 (2011). doi:10.1016/j.tcs.2011.09.015. http://www.sciencedirect.com/science/article/pii/S0304397511007912
2. Alghassi, H.: The algebraic QUBO design framework. To be published
3. Bodlaender, H.L., Koster, A.M.: Treewidth computations i. upper bounds. Inf. Comput. 208(3), 259–275 (2010)
4. Boothby, T., King, A.D., Roy, A.: Fast clique minor generation in chimera qubit connectivity graphs. Quantum Inf. Process. 15(1), 495–508 (2016). doi:10.1007/s11128-015-1150-6
5. Cai, J., Macready, W.G., Roy, A.: A practical heuristic for finding graph minors. Preprint (2014). arXiv:1406.2741
6. Choi, V.: Minor-embedding in adiabatic quantum computation: II. Minor-universal graph design. Quantum Inf. Process. 10(3), 343–353 (2011). doi:10.1007/s11128-010-0200-3
7. Dridi, R., Alghassi, H.: Homology computation of large point clouds using quantum annealing. Preprint (2015). arXiv:1512.09328
8. Fan, N., Pardalos, P.M.: Linear and quadratic programming approaches for the general graph partitioning problem. J. Glob. Optim. 48(1), 57–71 (2010). doi:10.1007/s10898-009-9520-1
9. Godsil, C., Royle, G.: Algebraic Graph Theory, Volume 207 of Graduate Texts in Mathematics (2001)
10. Grohe, M., Marx, D.: On tree width, bramble size, and expansion. J. Comb. Theory Ser. B 99(1), 218–228 (2009)
11. Hager, W.W., Krylyuk, Y.: Graph partitioning and continuous quadratic programming. SIAM J. Discret. Math. 12(4), 500–523 (1999)
12. Hernandez, M., Zaribafiyat, A., Aramon, M., Naghibi, M.: A novel graph-based approach for determining molecular similarity. Preprint (2016). arXiv:1601.06693
13. Imrich, W., Peterin, I.: Recognizing Cartesian products in linear time. Discret. Math. 307(3–5), 472–483 (2007)
14. Johnson, M.W., Amin, M.H.S., Gildert, S., Lanting, T., Hamze, F., Dickson, N., Harris, R., Berkley, A.J., Johansson, J., Bunyk, P., Chapple, E.M., Enderud, C., Hilton, J.P., Karimi, K., Ladizinsky, E., Ladizinsky, N., Oh, T., Perminov, I., Rich, C., Thom, M.C., Tolkacheva, E., Truncik, C.J.S., Uchaikin, S., Wang, J., Wilson, B., Rose, G.: Quantum annealing with manufactured spins. Nature 473(7346), 194–198 (2011)

15. Kaminsky, W., Lloyd, S.: Scalable architecture for adiabatic quantum computing of NP-hard problems. In: Leggett, A., Ruggiero, B., Silvestrini, P. (eds.) Quantum Computing and Quantum Bits in Mesoscopic Systems, pp. 229–236. Springer, New York (2004). doi:10.1007/978-1-4419-9092-1_25

16. Kaplansky, I., Riordan, J.: The problem of the rooks and its applications. Duke Math. J. 13(2), 259–268 (1946). doi:10.1215/S0012-7094-46-01324-5

17. King, A.D., Lanting, T., Harris, R.: Performance of a quantum annealer on range-limited constraint satisfaction problems. Preprint (2015). arXiv:1502.02098

18. Lucena, B.: Achievable sets, brambles, and sparse treewidth obstructions. Discret. Appl. Math. 155(8), 1055–1065 (2007)

19. Pardalos, P.M., Mavridou, T., Xue, J.: Handbook of Combinatorial Optimization: volume 2, chap. The Graph Coloring Problem: A Bibliographic Survey, pp. 1077–1141. Springer, Boston (1999). doi:10.1007/978-1-4613-0303-9_16

20. Perdomo-Ortiz, A., Fluegemann, J., Biswas, R., Smelyanskiy, V.N.: A performance estimator for quantum annealers: gauge selection and parameter setting. Preprint (2015). arXiv:1503.01083

21. Perdomo-Ortiz, A., O’Gorman, B., Fluegemann, J., Biswas, R., Smelyanskiy, V.N.: Determination and correction of persistent biases in quantum annealers. Sci. Rep. 6, 18628 (2016)

22. Rieffel, E.G., Venturelli, D., O’Gorman, B., Do, M.B., Prystay, E.M., Smelyanskiy, V.N.: A case study in programming a quantum annealer for hard operational planning problems. Quantum Inf. Process. 14(1), 1–36 (2014). doi:10.1007/s11128-014-0892-x

23. Rieffel, E.G., Venturelli, D., O’Gorman, B., Do, M.B., Prystay, E.M., Smelyanskiy, V.N.: A case study in programming a quantum annealer for hard operational planning problems. Quantum Inf. Process. 14(1), 1–36 (2015)

24. Seymour, P.D., Thomas, R.: Graph searching and a min–max theorem for tree-width. J. Comb. Theory Ser. B 58(1), 22–33 (1993)

25. Thomas, R.: Tree-decompositions of graphs (lecture notes). School of Mathematics. Georgia Institute of Technology, Atlanta, 30332 (1996)

26. Venturelli, D., Mandrà, S., Knysh, S., O’Gorman, B., Biswas, R., Smelyanskiy, V.: Quantum optimization of fully connected spin glasses. Phys. Rev. X 5, 031040 (2015). doi:10.1103/PhysRevX.5.031040

27. Venturelli, D., Marchand, D.J.J., Rojo, G.: Quantum annealing implementation of job-shop scheduling. Preprint (2015). arXiv:1506.08479

28. Young, K.C., Blume-Kohout, R., Lidar, D.A.: Adiabatic quantum optimization with the wrong Hamiltonian. Phys. Rev. A 88, 062314 (2013). doi:10.1103/PhysRevA.88.062314