Bootstrapped switch with improved linearity based on a negative-voltage bootstrapped capacitor

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Abstract This study introduces a new bootstrapped switch for improving sampling linearity. In this technology, the introduction of a negative-voltage bootstrap capacitor reduces the parasitic capacitance at the critical signal node, thus improving its linearity. The proposed circuit is simulated using 0.18-μm complementary metal-oxide-semiconductor technology. The parasitic capacitance of the proposed scheme is approximately 30% lower than that of the conventional structure. In the case of rail-to-rail input, the proposed switch achieves a signal-to-noise-plus-distortion ratio (SNDR) of 83.3 dB and a spurious-free dynamic range (SFDR) of 82.3 dB from a 1.2-V supply at a 50-MHz sampling rate. The SFDR and SNDR of the proposed bootstrapped switch increase by 11.7 and 12.7 dB, respectively, compared with those of conventional bootstrapped switches.

Keywords: bootstrapped switch, linearity, low voltage

1. Introduction

Sensors are ubiquitous devices that include audio, temperature, light, magnetic, and capacitive sensors as well as biopotential acquisition and biometric identification sensors for wearable devices. In various sensor applications, the analog-to-digital converter (ADC) is a key block, and the core circuit of an ADC is the sample-and-hold (S/H) circuit. The performance of the S/H circuit largely determines the ADC performance. The S/H circuit of a conventional metal-oxide-semiconductor (MOS) switch is adversely affected by problems, such as low linearity and channel charge injection, clock feedthrough, kT/C noise, and other nonideal factors that limit its accuracy and speed.

To address these problems, researchers have proposed bootstrapped-switch technology [1] including various optimization-compensation techniques for bootstrapped switches such as body-effect compensation of analog switches to improve linearity [2, 3, 4], couple-effect compensation of bootstrapped switches to improve the high frequency performance [5, 6, 7, 8, 9], and other improvements [10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32]. These bootstrapped switches have demonstrated improved performance. Although these various compensation techniques have improved the linearity of the bootstrap switch, the parasitic capacitance of key nodes has not been reduced, and the size of these parasitic capacitances affects the nonlinearity of the bootstrap switch. To address this, a bootstrapped switch with improved linearity based on a negative-voltage bootstrapped capacitor is proposed in this study. In this technology, the introduction of a negative-voltage bootstrap capacitor causes the gate-source voltage of the PMOS switch to be equal to 2VDD. That is, in the case of the same on-resistance, the size of the PMOS can be designed to be smaller to reduce the parasitic capacitance, which increases the linearity of the bootstrapped switch. Compared with the conventional bootstrapped switch, the number of transistors connected to the gate of the sampling transistor is smaller, which reduces the parasitic capacitance of the gate of the sampling transistor, thus improving the linearity of the bootstrapped switch.

2. Analysis of conventional bootstrapped switch

The conventional bootstrapped switch [5] is shown in Figure 1. When CLK = 0 and CLKB = 1, transistors M1, M3, M4, M9, and M10 are turned on, and transistors M2, M5, M6, M7, and M8 are turned off. Furthermore, the voltage across the bootstrapped capacitor C1 is charged to VDD and discharged to the ground. Because the sampling switch M8 is turned off, the output terminal voltage is in a holding state. When CLK = 1 and CLKB = 0, transistors M1, M3, M4, M9, and M10 are turned off, and transistors M2, M5, M6, M7, and M8 are turned on. The bootstrap capacitor C1 charges the sampling switch M8; thus, the gate-source voltage of the sampling switch is fixed near VDD. In this state, the output voltage follows the input signal. Because of the node parasitic capacitance in the bootstrapped-switch circuit, its gate voltage after sampling switch M8 is turned

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on can be expressed as
\[
V_{GS} = \frac{C_1 + C_{P1} + C_{P2}}{C_1 + C_{P1} + C_{P2}} V_{DD} + \frac{C_1}{C_1 + C_{P1} + C_{P2}} V_{IN} \tag{1}
\]
where \(C_{P1}\) and \(C_{P2}\) are the parasitic capacitances of the upper plate node of bootstrapped capacitor \(C_1\) and the gate node of sampling switch \(M8\), respectively. In the sampling phase, the gate-source voltage of \(M8\) can be expressed as
\[
V_{GS8} = \frac{C_1 + C_{P1} + C_{P2}}{C_1 + C_{P1} + C_{P2}} V_{DD} + \left(\frac{C_1}{C_1 + C_{P1} + C_{P2}} - 1\right) V_{IN} \tag{2}
\]
\[
R_{ON8} = \frac{1}{\mu_{p}C_{ox} \left(\frac{W}{L}\right) (V_{GS8} - V_{THS})} \tag{3}
\]

The foregoing analysis illustrates that the gate-source voltage of sampling switch \(M8\) is approximately equal to \(V_{DD}\) only when \(C_{P1} + C_{P2} \ll C_1\). This phenomenon also reveals that the parasitic capacitance \(C_{P1}\) and \(C_{P2}\) are nonlinear sources of the bootstrapped switch. Therefore, parasitic capacitances \(C_{P1}\) and \(C_{P2}\) need to be reduced during the design process.

3. Proposed bootstrapped switch

Compared with the disadvantages of the conventional bootstrapped switch, the proposed bootstrapped switch primarily reduces the parasitic capacitance of \(C_{P1}\) and \(C_{P2}\) and fixes the gate-source voltage of the PMOS transistor to \(2V_{DD}\). The proposed bootstrapped switch circuit is shown in Figure 2.

In the next step, we analyze the proposed bootstrap switch. For the sake of simplicity, we do not consider the influence of node parasitic capacitance. When \(CLK = 0\) and \(CLKB = 1\), the bootstrapped switch operates in the hold phase, and the input signal, \(V_{IN}\), is sampled at the top plate of negative-voltage bootstrapped capacitor \(C_2\) through transistors \(MN6\) and \(MP6\). The bottom plate of \(C_2\) is discharged to the ground. Transistor \(M2\) is turned off to isolate the gate-source voltage. Because the gate voltage of transistor \(MP5\) is charged to \(V_{DD}\), \(MP5\) is turned off in the holding phase. The working state of the other transistors is the same as that of a conventional bootstrapped switch. In the holding phase, the gate voltage of \(MP5\) and the voltage of the top and bottom plates of the \(C_2\) capacitor can be expressed as follows.
\[
V_{GS} = V_{DD} \tag{4}
\]
\[
V_{TOP-PLATE} = V_{IN} \tag{5}
\]
\[
V_{BOTTOM-PLATE} = V_{DD} \tag{6}
\]

When \(CLK = 1\) and \(CLKB = 0\), the bootstrapped switch operates in the sampling phase. Transistors \(MN6\) and \(MP6\) are turned off to isolate the input signal \(V_{IN}\). Because transistor \(M12\) is turned on, the bottom plate of \(C_2\) is discharged to the ground, and the top-plate voltage of capacitor \(C_2\) is bootstrapped to \(V_{IN} - V_{DD}\). The connection between the NMOS \(MN6\) substrate and the gate potential requires attention because it is critical in realizing a negative-voltage bootstrap capacitor. The potential of each node can be expressed as follows.
\[
V_{BOTTOM-PLATE} = 0 \tag{7}
\]
\[
V_{TOP-PLATE} = V_{IN} - V_{DD} \tag{8}
\]
\[
V_{GS7} = V_{IN} + V_{DD} - V_{IN} = V_{DD} \tag{9}
\]
\[
V_{GS5} = V_{TOP-PLATE} = V_{IN} - V_{DD} \tag{10}
\]
\[
V_{GS5} = V_{IN} + V_{DD} - (V_{IN} - V_{DD}) = 2V_{DD} \tag{11}
\]
\[
V_{GS8} = V_{IN} + V_{DD} - V_{IN} = V_{DD} \tag{12}
\]

The main switching transistors in the signal link are \(M5\) and \(M7\). The ON resistance of the switching transistor and sampling transistor \(M8\) can be expressed as follows.
\[
R_{ON5} = \frac{1}{\mu_{p}C_{ox} \left(\frac{W}{L}\right) (2V_{DD} - V_{THS})} \tag{13}
\]
\[
R_{ON7} = \frac{1}{\mu_{p}C_{ox} \left(\frac{W}{L}\right) (V_{DD} - V_{TH7})} \tag{14}
\]
\[
R_{ON8} = \frac{1}{\mu_{p}C_{ox} \left(\frac{W}{L}\right) (V_{DD} - V_{TH8})} \tag{15}
\]

In fact, according to formula (3), we must consider the parasitic capacitances \(C_{P1}\) and \(C_{P2}\), the sizes of which will affect the sampling linearity of the bootstrap switch.

According to the aforementioned analysis, the proposed bootstrapped switch circuit successfully enables the gate-source voltage of PMOS \(MP5\) to be fixed near \(2V_{DD}\). That is, in the case of the same on-resistance, the size of the PMOS \(MP5\) can be designed to be smaller to reduce the parasitic capacitance \(C_{P1}\) and \(C_{P2}\) so that the linearity of the bootstrapped switch is increased. In addition, compared with the traditional bootstrap switch circuit, the proposed circuit effectively reduces the gate capacitance of the sampling transistor because it removes the transistor \(M6\), as shown in Figure 1. This improves the linearity of the bootstrap switch.

4. Simulation results

The proposed bootstrapped switch was simulated using 0.18-\(\mu\)m CMOS technology. The following main transistor sizes were used in the circuit simulation: \(M3 = 2\mu\text{m}/180\text{nm}, M4 = 4\mu\text{m}/180\text{nm}, M5 = 4\mu\text{m}/180\text{nm}, MP5 =\)
Fig. 3 Transient analysis of the gate-source voltage of the PMOS switch in the signal main link (rail-to-rail input).

Fig. 4 Simulation of the difference in the gate-source voltage of the sampling switch.

Fig. 5 Output spectra of the (a) conventional and (b) proposed bootstrapped switches.

As random choices, a supply voltage of 1.2 V and a sampling frequency of 50 MHz with rail-to-rail input amplitude were applied. To detect the linearity improvement more effectively, the values of the bootstrapped capacitor $C_1$ and the sampling capacitor $C_S$ of the conventional and proposed bootstrapped switches, respectively, were both 1 pF. In the sampling phase, the waveform of the gate-source voltage of the PMOS switch transistor $M_5$ (MP5), shown in Figure 3, indicates that the proposed bootstrapped switch can achieve a gate-source voltage fixed at approximately $2V_{DD}$.

Figure 4 shows the gate-source voltage difference in the sampling transistors in the proposed and conventional bootstrapped switches. Because the proposed bootstrapped switch reduces the gate sampling capacitance, the conduction voltage of the sampling switch is closer to $V_{DD}$. Thus, the gate parasitic capacitance of the transistor $M_8$ in the proposed bootstrap switch is smaller.

The simulation result shown in Figure 4 is related to the set transistor parameters; the parameters of the transistor can be amplified in equal proportions to obtain more obvious changes. In fact, there is no need to enlarge the size because the analysis of the dynamic characteristics of the bootstrap switch circuit enables a clear conclusion to be drawn.

As a random choice, a rail-to-rail input with an input frequency of 342 kHz and a sampling frequency of 50 MHz was used. The output spectra of the proposed and conventional bootstrapped switches are shown in Figure 5. The spurious-free dynamic range (SFDR) and the signal-to-noise-plus-distortion ratio (SNDR) of the conventional bootstrapped switch were 70.7 and 70.6 dB, respectively, whereas those of the proposed bootstrapped switch were 82.3 and 83.3 dB, respectively. The SFDR and SNDR of the proposed bootstrapped switch increased by 11.7 and 12.7 dB, respectively, compared with those of the conventional bootstrapped switches.

Figure 6 shows the SFDR and SNDR plots obtained at the differential output for input-signal amplitudes of 0.4, 0.6, 0.8, 1.0, and 1.2 $V_{PP}$. The proposed method clearly improved both the SFDR and SNDR over the input-signal amplitude.

5. Conclusion

A new bootstrapped switch is proposed to improve the sampling linearity. Simulation is conducted using the 0.18-μm CMOS process. Compared with the conventional sampling switch, the parasitic capacitance of the proposed scheme is approximately 30% lower than that of the conventional structure, which improves the linearity of the bootstrapped
sampling switch circuit. The simulation results show that the SFDR and SNDR of the proposed bootstrapped switch are improved compared with those of the conventional bootstrapped switch.

Acknowledgments

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References

[1] A.M. Abo and P.R. Gray. “A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter,” IEEE J. Solid-State Circuits 34 (1999) 599 (DOI: 10.1109/4.760369).
[2] M. Asgari and O. Hashemipour. “Body effect compensation of analog switches using variable voltage function,” IEICE Electron. Express 8 (2011) 189 (DOI: 10.1587/exle.8.189).
[3] S.-E. Hsieh and C.-C. Hsieh. “A 0.44-μJ/conversion-step 11-bit 600-kS/s SAR ADC with semi-resting DAC,” IEEE J. Solid-State Circuits 53 (2018) 2595 (DOI: 10.1109/JSSC.2018.2847306).
[4] S. Sen, et al. “A distortion reduction technique for bootstrapped-gate MOS sample-and-hold circuits using body-effect compensation,” IEEE Fable Tension Faible Consumtion (2014) 1 (DOI: 10.1109/FITC.2014.6828613).
[5] C.-C. Liu, et al. “A 10-bit 50-MS/s SAR ADC with a monotonically capacitive switching procedure,” IEEE J. Solid-State Circuits 45 (2010) 731 (DOI: 10.1109/JSSC.2010.2042254).
[6] J.-H. Tsai, et al. “A 0.003 mm² 10b 240 MS/s 0.7 mW SAR ADC in 28 nm CMOS with digital error correction and correlated-reversed switching,” IEEE J. Solid-State Circuits 50 (2015) 1382 (DOI: 10.1109/JSSC.2015.2413850).
[7] S. Zheng, et al. “A clock-feedthrough compensation technique for bootstrapped switch,” International Conference on Electron Devices and Solid-State Circuits (EDSSC) (2017) 1 (DOI: 10.1109/EDSSC.2017.825495).
[8] T.B. Nazazzal and S.A. Mahmoud. “Low-power bootstrapped sample and hold circuit for analog-to-digital converters,” 2016 IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS) (2016) 1 (DOI: 10.1109/MWSCAS.2016.7870027).
[9] C.-C. Lu and T.-S. Lee. “A 10-bit 60-MS/s low-power CMOS pipelined analog-to-digital converter,” IEEE Trans. Circuits Syst. II, Exp. Briefs 54 (2007) 658 (DOI: 10.1109/TCII.2007.899449).
[10] Y. Cao, et al. “An operational amplifier assisted input buffer and an improved bootstrapped switch for high-speed and high-resolution ADCs,” IEEE International Symposium on Circuits and Systems (ISCAS) (2018) 1 (DOI: 10.1109/ISCAS.2018.8351071).
[11] L. Luo, et al. “A digitally calibrated 14-bit linear 100-MS/s pipelined ADC with wideband sampling frontend,” 2009 Proceedings of ESSCIRC (2009) 472 (DOI: 10.1109/ESSCIRC.2009.5325956).
[12] A. Zanchi and D. Chang. “A 16-bit 65-MS/s pipeline ADC with 80-dBFS SNR using analog auto-calibration in SiGe SOI complementary BiCMOS,” IEEE Trans. Circuits Syst. I, Reg. Papers 55 (2008) 2166 (DOI: 10.1109/TCSI.2008.920123).
[13] A. Sepahvand and O. Hashemipour. “A low voltage bootstrapped switch based on zero DC offset input voltage,” IEICE Electron. Express 5 (2008) 932 (DOI: 10.1587/exle.5.932).
[14] A. Shikata, et al. “A 0.5V 65m-CMOS single phase clocked bootstrapped switch with rise time accelerator,” IEEE Asia Pacific Conference on Circuits and Systems (2010) 1015 (DOI: 10.1109/APCCAS.2010.5774976).
[15] L. Wang, et al. “A bootstrapped analog switch for rail-to-rail sampling,” 2008 9th International Conference on Solid-State and Integrated-Circuit Technology (2008) 1977 (DOI: 10.1109/ICSCIT.2008.4734949).
[16] G. Huang and P. Lin. “A fast bootstrapped switch for high-speed high-resolution A/D converter,” IEEE Asia Pacific Conference on Circuits and Systems (2010) 382 (DOI: 10.1109/APCCAS.2010.5774977).
[17] L. Wang, et al. “A high-speed high-resolution low-distortion CMOS bootstrapped switch,” IEEE International Symposium on Circuits and Systems (ISCAS) (2007) 1721 (DOI: 10.1109/ISCAS.2007.377926).
[18] E. Swindlehurst, et al. “An 8-bit 10-GHz 21-mW time-interleaved SAR ADC with grouped DAC capacitors and dual-path bootstrapped switch,” ESSCIRC 2019 - IEEE 45th European Solid State Circuits Conference (ESSCIRC) (2019) (DOI: 10.1109/ESSCIRC.2019.8902621).
[19] M.G. Khajeh and J. Sobhi. “An 87-dB-SNDR 1MS/s/bilateral bootstrapped CMOS switch for sample-and-hold circuit,” 28th Iranian Conference on Electrical Engineering (ICE/E) (2020) (DOI: 10.1109/ICEE50131.2020.9260778).
[20] X. Meng and G.C. Temes. “Bootstrapping techniques for floating switches in switched-capacitor circuits,” IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS) (2014) 398 (DOI: 10.1109/MWSCAS.2014.6908436).
[21] O.D. Bernal, et al. “Radiation hardened bootstrapped switch in 0.18μm CMOS process,” 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS) (2014) 610 (DOI: 10.1109/ICECS.2014.7050059).
[22] S. Liu, et al. “A 12-bit 10MS/s SAR ADC with high linearity and energy-efficient switching,” IEEE Trans. Circuits Syst. I, Reg. Papers 63 (2016) 1616 (DOI: 10.1109/TCSI.2016.2581177).
[23] Y. Allasasmeh and S. Gregori. “Switch bootstrapping technique for voltage doublers and double charge pumps,” IEEE International Symposium on Circuits and Systems (ISCAS) (2011) 494 (DOI: 10.1109/ISCAS.2011.5937610).
[24] D.-G. Li, et al. “The design of high linear bootstrapped SI switch,” IEEE 3rd International Conference on Integrated Circuits and Microsystems (ICICM) (2018) 51 (DOI: 10.1109/ICCM.2018.8563674).
[25] L. Qian, et al. “A low distortion CMOS bootstrapped switch,” Pacific-Asia Conference on Circuits, Communications and Systems (2009) 261 (DOI: 10.1109/PACCS.2009.97).
[26] P. Pouya, et al. “A low-voltage high-speed high-linearity MOSFET-only bootstrapped switch for sample-and-hold circuits,” 2nd International Conference on Knowledge-Based Engineering and Innovation (KBEE) (2015) 418 (DOI: 10.1109/KBEI.2015.7436081).
[27] X. Wu, et al. “A CMOS bootstrapped switch with novel clock feed-through compensation,” IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC) (2009) 166 (DOI: 10.1109/EDSSC.2009.5394165).
[28] J. Wang, et al. “A 500-1000MS/s 12-bit resolution level-shift bootstrapped switch,” 12th IEEE International Conference on Solid-State and Integrated Circuits Technology (ISSCIT) (2014) 1 (DOI: 10.1109/ISSCIT.2014.7021306).
[29] D. Aksin, et al. “A bootstrapped switch for precise sampling of inputs with signal range beyond supply voltage,” Proceedings of the IEEE 2005 Custom Integrated Circuits Conference (2005) 743 (DOI: 10.1109/CICC.2005.1568775).
[30] J. Steensgaard. “Bootstrapped low-voltage analog switches,” IEEE International Symposium on Circuits and Systems (ISCAS) (1999) 29 (DOI: 10.1109/ISCAS.1999.780611).
[31] G.K. De Teyou, et al.: “Statistical analysis of harmonic distortion in a differential bootstrapped sample and hold circuit,” 10th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME) (2014) 1 (DOI: 10.1109/PRIME.2014.6872726).

[32] A. Mohammadi and M. Chahardori: “A low-power, bootstrapped sample and hold circuit with extended input ranged for analog-to-digital converters in CMOS 0.18 μm,” 15th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD) (2018) 269 (DOI: 10.1109/SMACD.2018.8434915).