A Modified Hybrid DC Circuit Breaker With Reduced Arc for Low Voltage DC Grids

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\textbf{ABSTRACT} The increasing demand for the development and utilization of renewable energy resources has lead to a growing interest in the development of LVDC systems. The dc grid provides more flexibility in integrating different forms of renewable energy sources effectively. However, the lack of a reliable protection mechanism remains the main drawback in the growth of dc distribution systems. Unlike ac systems, the absence of a natural zero crossing in dc systems for arc extinction makes the use of a conventional mechanical circuit breaker (MCB) a less reliable solution. The use of a solid-state circuit breaker (SSCB) results in fast fault interruption but reduces the overall efficiency of the system due to the on-state voltage drop of the semiconductor devices. A hybrid circuit breaker (HCB) combining MCB and SSCB yields better static and dynamic performances but the main challenges remains in the demagnetization of the transmission line inductance after a fault interruption and an arc formation between the MCB contacts. This paper proposes a hybrid circuit breaker (HCB) which is suitable for fast fault interruption in low voltage dc (LVDC) systems while alleviating the above issues. Proposed topology employs a semiconductor switch as well as an actively switched capacitor branch in parallel with the main mechanical breaker to facilitate fast current commutation during a fault. The mechanical breaker forming the main branch is turned off at zero voltage. This eliminates the arc formation across the moving contacts of the breaker. Moreover, the fault interruption process does not require a varistor for network demagnetization following the fault current commutation. This paper also presents a discharging mechanism for the capacitor in a practical implementation. Operation of the proposed dc circuit breaker is evaluated through a prototype tested in the laboratory.

\textbf{INDEX TERMS} Hybrid circuit breaker (HCB), LVDC, mechanical circuit breaker, varistor.

\textbf{I. INTRODUCTION} A practical solution to the efficiency and synchronization issues of an existing ac electrical grid can be represented by a dc distribution micro-grid. A dc grid also provides the much needed flexibility in integrating different forms of renewable energy sources effectively [1]–[4]. However, the inadequate protection options for direct current systems during faults cause a major restriction to the growth of dc distribution systems. A common practice is to use a mechanical circuit breaker (MCB) mimicking the ac system protection. Nevertheless, in dc systems, a current interruption results in the ionization of the moving circuit breaker contacts and medium between them. This generates an arc between the moving mechanical contacts and the fault current continues to flow through the arc. Multiple arcing events reduce the life cycle of the MCB, rendering it less feasible as a dc switchgear [5].

A simple solution to the challenges manifested in MCB switching is the use of semiconductor devices in place of the mechanical breaker, resulting in solid state circuit breakers (SSCB) [6]–[8]. A semiconductor device along with a suitable bypass protection network can interrupt the fault within microseconds. In addition, the arc formation is eliminated due to the absence of moving parts. Nonetheless, the relatively large on-state voltage drop of a semiconductor device causes a significant reduction in the overall efficiency of the
distribution network. Moreover, the need for an external cooling system for the thermal protection of the semiconductor devices increases the operating cost. Additionally, the bypass network necessitates a dissipative snubber to limit the voltage stress on the semiconductor switch. All of these factors have contributed to the growing focus in the research of hybrid circuit breaker (HCB).

The general idea behind an HCB is to combine the advantages of both MCB and SSCB, such that it exhibits minimal conduction power loss in the steady-state like an MCB, while the fault interruption speed is comparable to the SSCB [9], [10]. A classical hybrid circuit breaker consists of a semiconductor switch connected in parallel with a mechanical breaker. During the normal operation, the semiconductor device remains turned off while the load current is conducted by the mechanical switch. At the inception of a short-circuit fault, the semiconductor device is turned on in synchronization with the opening of the mechanical breaker contacts. Consequently, the fault current is completely diverted to the semiconductor branch which is allowed to conduct for a short duration before the fault is quenched by a varistor branch. Thus, the current commutation process in a conventional HCB involves arc formation between the moving contacts of the MCB. Also, the commutation of current from the MCB to the semiconductor branch depends on the magnitude of the arc voltage [11]. Such repeated arcing events reduce the effective life-cycle of the HCB.

An improved HCB topology was presented in [12] by connecting a semiconductor switch in series with the mechanical breaker. This semiconductor switch, termed the load commutation switch (LCS), improves the commutation time and minimizes the arc. However, the substantial conduction loss due to a semiconductor element in the main path remains a demerit. Other versions of HCBs found in the literature use different auxiliary commutation networks, such as a time delaying branch [13], a multilevel PWM converter [14], a buffer capacitor and a vacuum interrupter [15] or anti-parallel thyristors with energy storage elements [16]. However, the current commutation process in all of these HCB topologies results in large transient overvoltage across the MCB. Hence, suitable over voltage protection devices like metal oxide varistor (MOV) should be connected in parallel for the protection of the respective semiconductor devices.

The energy dissipated in the MOV is substantially large in dc systems due to the stray network inductance and the line inductance. Therefore, MOVs are prone to thermal failure, which necessitates external cooling arrangements for reliable operation. Moreover, MOVs do not provide \( \frac{dv}{dt} \) protection to the device which might cause device failure in fast current transitions. The system redundancy could be improved by using cascaded networks with smaller MOVs as represented in [17], [18]. Nonetheless, a more elegant solution to mitigate the issues related to MOV is provided by a family of HCBs known as zero current switching (ZCS) breakers. A generic ZCS HCB employs a pre-charged capacitor to make a forced zero crossing of the fault current before the MCB is turned off, thereby guaranteeing arc-less operation and also eliminating the need for surge arresters [19]–[21]. The main demerit of these topologies lies in the precharging requirement and the loss of breaking capacity due to the self-discharge of the capacitor. Also, the presence of parasitic elements and variable reaction time of the mechanical breaker makes the opening of mechanical switch at the exact zero crossing a much complicated process.

In summary, state-of-the-art HCB topologies manifest several operational disadvantages in terms of arc formation, increased power loss, low reliability of the MOV, and capacitor pre-charging, which affect the overall system reliability and increase the capital cost. To overcome these deficiencies, an alternate HCB solution is needed. This paper proposes a modified HCB with a switched capacitor branch that fits these design criteria. The main breaker branch consists of one high-speed and one low-speed mechanical switch in which the former can be turned off at zero voltage and the latter at zero current conditions. The switched capacitor branch demagnetizes the dc network following MCB turn-off [22]. The main contributions of the paper are,

- A novel hybrid dc circuit breaker topology
- Relatively negligible arc during the opening of the mechanical contacts (could also be considered as “arc-less operation”)
- Higher reliability as a result of low arc
- Does not need any additional capacitor charging circuits
- The topology do not require surge arrester to suppress the network stored energy

The remaining part of the paper is organized as follows. Section II illustrates the commutation process in the proposed HCB. A modification of the proposed topology for bidirectional operation is presented in section III. This section also highlights a simple discharging mechanism for the capacitor. The performance of the proposed dc breaker is evaluated experimentally as described in section IV. Finally, the paper is summarized in Section V.

II. PROPOSED HYBRID CIRCUIT BREAKER

A. OPERATING PRINCIPLE

The proposed hybrid circuit breaker topology is shown in FIGURE 1(a). \( HS \) is an ultra-fast mechanical switch, while \( LS \) refers to a low-speed MCB. The IGBT \( Q \) represents the parallel semiconductor branch. The auxiliary branch of capacitor \( C \) and diode \( D \) represents the switched capacitor network. \( D \) remains reverse biased during the power delivery mode. Consequently, the capacitor \( C \) remains uncharged. \( L_g \) represents the total series inductance of the LVDC network. \( LS \) does not take part in the current commutation, it is turned off once the fault interruption is complete to prevent power flow through the switched capacitor branch during the off state. It is to be noted that, \( Q \) and \( D \) might consist of several cascaded devices in a practical LVDC system. Apart from these the proposed breaker also consist of control unit that
is responsible for fault detection and sending respective command signals to the switching devices.

During normal mode of operation, contacts of both mechanical breakers are in closed condition. The IGBT $Q$ also remains gated on but since the on state resistance of the semiconductor device is large as compared to the parallel HS switch which is entirely made of conductor material, majority of the current will flow through the HS branch. Hence we can approximate that power flow during normal condition is as depicted in FIGURE 1(b). When the control unit detects that the current value exceeds a preset limit, a command signal is send to the mechanical switch HS. Since the parallel IGBT is already in on state the switch HS is turned off at near zero voltage condition, thus achieving arc-less operation.

Also the fault current is immediately commutated towards the semiconductor branch as shown in FIGURE 1(c).

The IGBT $Q$ is then made to conduct the fault current for a certain preset time interval so that the medium between the contacts could build up sufficient dielectric strength to prevent any chances of arc re-striking. The IGBT $Q$ is then gated off directing the fault current towards the switched capacitor branch resulting in a resonant network as depicted in FIGURE 1(d). Once the capacitor is fully charged, the diode $D$ gets reverse biased thus fully interrupting the flow of fault current. The low speed switch LS can then be turned off at zero current condition.

**B. ANALYSIS AND DESIGN**

Based on the principle of operation of the proposed HCB, the total fault interruption time can effectively be divided into four sub intervals as depicted in FIGURE 2.

1) **Reaction time of the mechanical circuit breaker ($t_0$-$t_1$):** Once the fault is detected, the control circuit sends a command to turn off the HS, but since being a mechanical device HS will take some time to react to the command signal before the contacts starts separating. This interval is described as the delay time of the mechanical switch, $t_d$. The degree of freedom for this interval is limited by the commercial availability of ultra fast disconnector switches.

2) **Current commutation period ($t_1$-$t_2$):** Once the contacts of the mechanical breaker starts separating, the fault current gets immediately commutated towards the semiconductor branch. The duration of this interval is relatively very small.

3) **IGBT conduction period($t_2$-$t_3$):** After current commutation is completed, IGBT is made to carry the fault current for a particular duration to eliminate arc re-striking. This time period has to be chosen carefully as prolonged conduction time can lead to heating of semiconductor devices. Though the lower limit for this interval is dependant on atmospheric conditions like room temperature and humidity, it can be improved by the use of vacuum interrupters.

4) **Capacitor charging period ($t_3$-$t_4$):** Once the IGBT is turned off, the energy stored in the leakage inductance is used to charge the previously uncharged capacitor.
The duration of this interval is mainly dependent on the choice of capacitor selection and transmission line inductance. The impedance offered by the load and other parasitic resistances present in the network will also have an impact on this duration. The capacitor charging circuit is effectively a resonant circuit as observed in FIGURE 1(e) with an initial current \( I_f \) which represent the fault current at the instant when IGBT is turned off. Capacitor voltage and charging current at this interval can be obtained by solving the circuit.

Applying Kirchhoff’s voltage law on the circuit and taking Laplace transform we get,

\[
-\frac{V_g}{s} + \left( sL_g + \frac{1}{sC} \right) I(s) - L_g I_f = 0
\]

\[
\left( 1 + s^2L_gC \right) I(s) = \frac{V_g}{s} + L_g I_f
\]

By considering \( \omega_0 = \frac{1}{\sqrt{L_gC}} \), the above equation can be written as

\[
I(s) = \frac{V_g}{L_g(s^2 + \omega_0^2)} + \frac{sl_f}{s^2 + \omega_0^2}
\]

The expression for capacitor current in time domain is obtained by performing the inverse Laplace transform,

\[
i_c(t) = \frac{V_g}{Z_o} \sin \omega_0 t_c + I_f \cos \omega_0 t_c
\]

(1)

Similarly voltage across the capacitor can be obtained as

\[
v_c(t) = V_g(1 - \cos \omega_0 t_c) + Z_o I_f \sin \omega_0 t_c
\]

(2)

where, \( Z_o = \sqrt{\frac{L_g}{C}} \) and \( \omega_0 = \sqrt{\frac{1}{L_gC}} \) are the characteristic impedance and the resonant frequency of the charging circuit, respectively. The charging current rises and reaches a maximum value of \( i_c^{\text{max}} \) as given in (3).

\[
i_c^{\text{max}} = \frac{1}{Z_o} \left[ \sqrt{V_g^2 + I_f^2 Z_o^2} \right]
\]

(3)

The magnitude of charging current decreases continuously and reaches to zero. This current charges the capacitor to a maximum value of \( v_c^{\text{max}} \), presented (4).

\[
v_c^{\text{max}} = V_g + \frac{V_g^2}{\sqrt{V_g^2 + (I_f Z_o)^2}} + \frac{I_f^2 Z_o^2}{\sqrt{V_g^2 + (I_f Z_o)^2}}
\]

\[
v_c^{\text{max}} = V_g + \frac{V_g^2}{\sqrt{V_g^2 + (I_f Z_o)^2}}
\]

(4)

Finally, the expression for capacitor charging time \( t_c \) is given as,

\[
t_c = \frac{1}{\omega_0} \left[ \pi - \tan^{-1}\left( \frac{I_f Z_o}{V_g} \right) \right]
\]

(5)

It may be noted from (4) that the blocking voltage of switches \( HS \) and \( Q \) is limited to the peak capacitor voltage and consequently fault current becomes zero. Further, the diode also opposes the reverse current flow. The value of capacitance required in the auxiliary branch can be found by using equation (4).

\[
C = \frac{L_f I_f^2}{(v_c^{\text{max}} - V_g)^2 - V_g^2}
\]

(6)

It may also be noted from (6) that there is a trade-off while selecting the values of \( C \) and \( v_c^{\text{max}} \), in order to meet the energy storage requirement of network inductance.

C. COMPONENT SIZING AND SELECTION

This section discusses about the component sizing and selection in the proposed circuit breaker. In dc protection an additional inductance is added in order to limit the fault current in the system. Hence, the maximum fault current \( I_f \) depends on the total network inductance (line inductance plus external inductance) of the dc system. For a specific application or a value of maximum fault current interruption requirement in dc system, one may find the value of external network inductance to be added, from (7).

\[
L_g = \frac{V_g(t_d + t_{sc})}{I_f - I_n}
\]

(7)

where, \( V_g \) is the grid voltage and \( I_f \) is the current interrupted by semiconductor branch and \( I_n \) is the nominal current flowing through the network. And \( t_d \) is the reaction time of the HS, and \( t_{sc} \) is the time taken by semiconductor branch to interrupt the current flow in its path(\( t_1 - t_3 \)). The total time \( (t_d + t_{sc}) \) depends on speed of the ultra fast interrupter, rate of recovery of dielectric medium between the mechanical contacts, and the reverse recovery time of semiconductor branch. In this section the total time for turn off of HS and \( Q \) is assumed to be 100\( \mu \)s. The \( L_g \) value can be chosen for different fault current requirements keeping grid voltage constant, using the plot shown in FIGURE 3. As discussed, the capacitor value depends on choices made for network.
inductance $L_g$ and the maximum voltage rating of capacitor $v_{c}^{\text{max}}$. Same can also be observed in equation (6). Taking the above facts, contour plots between the capacitor value and $L_g$ for different maximum capacitor voltage ratings and different charging times is drawn and elucidated in FIGURE 4 and FIGURE 5 respectively. The capacitor value to be used in auxiliary branch can be selected from the contour plot shown in FIGURE 4. From the choice of capacitance $C$, we can also estimate the charging time of capacitor to its maximum voltage $v_{c}^{\text{max}}$ from the contour plot shown in FIGURE 5. It may be inferred from FIGURE 6 that the energy stored in network inductor can be easily absorbed by the selected capacitor.

D. SIMULATION RESULTS

In order to elucidate the circuit waveforms, the proposed topology is simulated in LTspice for an 300V/20A system. The transmission line leakage inductance is assumed to be 15 mH and capacitor value is chosen to be 50 $\mu$F. The mechanical switch model is emulated by connecting a large capacitor to the gate source junction of an IGBT. FIGURE 7 shows the voltage and current through the switches during fault. The fault is provided at the instant $t=4$ ms and after a delay of 0.25 ms the fault current starts to commutate towards the semiconductor branch $Q$. Once the commutation is completed $Q$ is made to conduct the fault current for a preset duration of 1 ms before being turned off at $t=5.25$ ms. Once $Q$ is turned off, $C$ is charged by the fault current. Fault reduces to zero at $t=7$ ms, indicating a fault clearing time of 3 ms.

III. MODIFIED BIDIRECTIONAL HCB

In a practical LVDC system, bidirectional flow of power is often desired. The proposed breaker though exhibits fast arc-less fault interruption, is not suitable for bidirectional applications as it consist of unidirectional power electronic switches. Hence suitable modifications has to be made for the proposed HCB to make it operational in a bidirectional LVDC system. The modified HCB circuit is shown in FIGURE 8, here bidirectional four quadrant switches made of two IGBTs connected in anti-series arrangement is used in place of the IGBT and diode of FIGURE 1(a). The working operation remains nearly the same, when the power flow is from left to right (port 1-1’ to port 2-2’), $Q_1$ is kept gated on during normal operation and during fault interruption $T_1$ is turned on to complete the capacitor charging path after $Q_1$ turn off. Similarly, when the power flow is in opposite direction $Q_2$ and $T_2$ are operated accordingly. Also the need for the residual LS switch can also be avoided as the switched capacitor branch consist of fully controlled devices that would prevent the charging of capacitor during off state. The analysis and component sizing of this bi-directional variant remains same as that of the uni-directional counterpart, except that the capacitor used should be of bipolar nature.

A. CAPACITOR DISCHARGING

After the turn off of either $Q_1$ or $Q_2$ shown in FIGURE 8(a) depending upon the power flow direction, the energy stored in the leakage inductance of the transmission line will charge up the previously uncharged capacitor $C$ through the path $L_g - C - T_1 -$ body diode of $T_2$ for (forward power flow direction), and $L_g - C - T_2 -$ body diode of $T_1$ for (backward power flow direction).
Direction). Hence, after each fault it is necessary to discharge the capacitor before next fault can occur. A simple resistive discharging circuit is proposed for the same as shown in FIGURE 8(b). It consist of a current bi-directional switch in series with a discharge resistor. Following the interruption of fault either $Q_{d1}$ or $Q_{d2}$ is turned on depending on the direction of the power flow.

Applying KVL

$$C \frac{dv_c}{dt} = i_c R_d$$

(8)

on solving

$$v_c(t) = v_{c,\text{max}} e^{-\frac{t}{R_d C}}$$

(9)

where $v_{c,\text{max}}$ is the maximum capacitor voltage as given by (4).

From (9), the total discharge time for the capacitor can be found to be $5R_d C$.

Also the peak current through $Q_{d1}$ and $Q_{d2}$ is given by.

$$i_{Q_d(\text{peak})} = \frac{v_{c,\text{max}}}{R_d}$$

(10)

Hence $R_d$ should be selected such that it should be able to discharge the capacitor before the estimated fault clearing time and also should ensure that the peak discharge current is under the safety limits of the semiconductor devices used.

The operation of the modified circuit breaker in forward and reverse power flow modes along with capacitor discharging is shown in FIGURE 9 and FIGURE 10 respectively.

IV. EXPERIMENTAL VALIDATION

A. EXPERIMENTAL SETUP

Due to the limited power source and sinking capabilities of the laboratory, the proposed unidirectional HCB was tested for a 300V system. Fault is emulated by giving
a step load change from 10A to 20A. A custom made MCB shown in FIGURE 11 was used as the mechanical breaker part (HS) of the HCB and a Semikron make IGBT (model:SKM150GB12T4) of 1200V/40A ratings was used.
as the semiconductor switch ($Q$). Capacitor chosen was of $50 \mu F$ and an inductor of $15 \text{ mH}$ was provided to emulate the transmission line leakage inductance. An LEM make (LA55-P) current sensor along with Texas Instruments make MSP430 micro-controller formed the control unit and the control algorithm employed is elucidated in FIGURE 13.

**B. MECHANICAL SWITCH/BREAKER USED IN THE PROPOSED HCB**

A custom made MCB based on pneumatic cylinder was used as the mechanical breaker for this experiment. A pneumatic cylinder is a mechanical device which uses the stored potential energy in compressed air to produce a force in linear reciprocating motion. A solenoid valve is used to control the direction of the linear force. In our application the cylinder is used to close and open the breaker contacts based on the command signal from the micro-controller. In order to evaluate the performance, the mechanical breaker alone was first used to interrupt the fault in the specified 300V/10A system.

The current and voltage waveforms are captured through an oscilloscope and is shown in FIGURE 14. It can be observed that after the fault is detected, it took around 15 ms for the device to start opening its contacts, this defines the reaction time of the mechanical breaker. It has to be noted that reaction speed observed is much slower as compared to practically used ultra-fast Thomson coil based disconnectors and is only used because the main intention of this paper is to evaluate only the secondary and tertiary branch performances of the proposed breaker.
C. EXPERIMENTAL RESULTS

The experiment was conducted and the captured waveforms are shown in FIGURE 15. The fault is provided at the instant $t_0$, almost immediately it is detected by the control unit and command for the opening of MCB was provided. After a delay of 15ms (Reaction time of the mechanical disconnector) the MCB contacts starts separating and fault current is commutated towards the IGBT branch. The IGBT is then made to conduct for a pre-programmed delay time of 1.5ms, this is to provide time for medium between the MCB contacts to build sufficient dielectric strength to prevent arc re-striking. Eventually, IGBT is then turned off at $t_3$ and the energy stored in the inductor is transferred to the capacitor through the diode. Fault current is then reduced to zero at $t_4$ once the capacitor is fully charged. A magnified version showing the current commutation from MCB to IGBT branch is shown in FIGURE 16. It can be observed that time taken for commutation is even less than 10 $\mu$s and during this time voltage across the entire parallel network remains minimum showing no significant amount of arc was formed during contact separation. The capacitor is then discharged through the simple discharge circuit described in section III by gating on $Q_d$ as shown in FIGURE 17.

D. INFERENCE AND LIMITATIONS OF THE PROTOTYPE TESTED

The captured waveform showing the performance of the proposed breaker is compared with the one observed when MCB alone was tested in the same fault condition. The reaction time of the mechanical disconnectors induces a delay time of 15ms in both cases before the fault interruption can begin. From FIGURE 14, it could be observed that after breaker contacts start opening, it took around 29ms for the fault to be completely interrupted. This is due to the arc formation between the contacts, which can be verified by looking at the voltage and current profiles during the interruption. In the case of a practical LVDC system where the grid voltage is in kilo volts range, this arc interruption can extend for a much larger duration which could be hazardous to the connected devices. Also repeated arcing events can lead to wear and tear of the breaker contacts reducing the life span of the device. A solution to these problems can be observed by looking at the performance of the proposed HCB as represented in FIGURE 15. Here fault interruption time excluding the MCB delay is observed to be 6ms, making it nearly around five times faster than when MCB alone was used. Also, no arc is formed at any stage of the fault interruption process thus improving the redundancy and reliability of the system.

As observed from FIGURE 15, the total fault interruption time was found to be 21 ms which is a rather long duration considering the safety limits of a practical LVDC system. This prolonged interruption time is due to certain restrictions in the prototype development and testing in the laboratory. The major constraint was the longer reaction time of the mechanical disconnector used. As discussed earlier, the reaction time of the disconnector was observed to be 15 ms which is around nearly three fourth of the total interruption time. In a practical implementation, this could be solved by the use of an ultra-fast disconnector such as a Thomson coil-based actuator which has a reaction time of less than 5 ms. This could result through the diode. Fault current is then reduced to zero at $t_4$ once the capacitor is fully charged. A magnified version showing the current commutation from MCB to IGBT branch is shown in FIGURE 16. It can be observed that time taken for commutation is even less than 10 $\mu$s and during this time voltage across the entire parallel network remains minimum showing no significant amount of arc was formed during contact separation. The capacitor is then discharged through the simple discharge circuit described in section III by gating on $Q_d$ as shown in FIGURE 17.

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in the interruption time being reduced by more than fifty per cent of the one observed in the tested prototype. Another limitation in the tested prototype was that the semiconductor switch was made to conduct the fault current for 1.5 ms before being turned off. This was done to give time for the dielectric medium between the disconnecter contacts to gain sufficient dielectric strength to prevent arc re-ignition. This interval though relatively short could further be minimized by artificially improving the dielectric strength of the medium surrounding the MCB contacts. One such method is by the use of Vacuum interrupters which will create a vacuum around the contacts. Another constraint encountered during testing was the limitation of source current capability in the laboratory, which resulted in the fault being emulated by providing a step load change rather than short-circuiting the load terminals as depicted in section II. The impedance of the load bank would slow down the capacitor charging during the final interval (t3-t4). Thus we could say that in case of an actual fault the capacitor charging interval would also be much faster than what was observed in the experiment conducted. But the reduced damping also means the capacitor would charge up to a voltage level more than what was observed in the prototype.

V. CONCLUSION

A modified hybrid circuit breaker for LVDC systems has been presented in this paper. The proposed topology employs a two step commutation process that ensures the opening of the mechanical switch at a relatively negligible arc condition through near zero voltage switching. A switched capacitor branch is utilized to absorb the stored energy present in network leakage inductance. This eliminates the need for surge arresters for protection as employed in conventional HCBs. Detailed analysis has been carried out for selection of components and the operational waveforms of the proposed breaker topology were verified using an experimental prototype developed in the laboratory.

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