Reference Spur Reduction in Sampled-loop filter PLLs by Oversampling

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Abstract—A technique to eliminate reference spurs in both Integer-N and Fractional-N charge pump phase locked loops (PLLs) based on an oversampled loop filter architecture is proposed. A detailed analysis of the performance of the proposed technique in the presence of implementation non-idealities is also presented. It is shown through analysis and simulations that the proposed technique, in addition to completely eliminating reference spurs, adds an insignificant area and power overhead when applied to Integer-N PLLs and less than 6% increase in area and power in case of Fractional-N PLLs.

I. INTRODUCTION

One of the major problems in charge pump PLLs is reference spurs which arise from its periodic sampling nature in the presence of phase frequency detector (PFD) and charge pump (CP) non-idealities [1], [2], [3], [4], [5], [6]. Reference spurs increase period jitter and out of band emissions of the PLL and to filter these spas, the bandwidth of the PLL is reduced. A reduced bandwidth results in poor rejection of VCO Phase noise and an increased settling time. Hence reducing reference spurs is a major concern when designing wide bandwidth PLLs.

One popular approach to reduce reference spurs in CP-PLLs is the sample-reset loop filter (SLF) technique [3], [6], [7], [8] shown in Fig.1. By sampling the charge injected from CP onto a sampling capacitor (C_s) and then deliver the charge to the loop filter Z(s), after a delay T_D (when the CP current i_{cp}(t) is zero), the loop filter (and the VCO) does not 'see' the sudden voltage variations caused by the transient CP current. Thus the reference spurs are reduced in a SLF PLL.

However the charge injection from the sampling switch in the SLF-PLL can still produce significant reference spurs. Using dummy switches alongside the actual sampling switch can reduce the reference spurs to some extent. Since this relies on circuit techniques, a complete elimination is not practically feasible due to device mismatches. In this work a simple technique to completely eliminate reference spurs in SLF-PLL by using a sampling clock of higher frequency is proposed. The proposed technique, when applied to Integer-N PLLs eliminates reference spurs without any additional area or power overhead and in the case of Fractional-N PLLs, with a marginal increase (<6%) in area and power.

Section II discusses the proposed technique in Integer-N and Fractional-N PLLs. A detailed analysis and comparison of spur levels before and after applying the technique is discussed in Section III. Section IV presents the test bench and the simulation results for the proposed techniques. The conclusions are summarised in Section V.

II. REFERENCE SPUR REDUCTION BY OVERSAMPLED LOOP FILTER (OSLF) TECHNIQUE

The source of reference spurs in SLF PLL is the periodic charge injection from the sampling switch into the loop filter. The proposed solution in this work is to increase the frequency of the sampling switch control signal by M times the reference frequency. By doing so, the reference spurs will be absent up to M f_r. The problem now is to derive the high frequency switch control signal Sos without adding much to the complexity or power consumption of the PLL.

1) Integer-N PLLs: In case of Integer-N PLLs, the VCO frequency is an integer multiple of the reference frequency (f_{vco} = N f_r). Therefore the higher sampling frequency clock M f_r can be derived from the VCO clock using a frequency divider. But adding an additional divider increases the power consumption as it operates at the VCO frequency. So the feedback divider can be split into two parts and the high frequency signal can be derived from the feedback divider path as shown in Fig.2. The divider is split into N_1 and M. The value of N_1 can be computed as

\[ M f_r = \frac{f_{vco}}{N_1} \rightarrow N_1 = \frac{N}{M} \]  \hspace{1cm} (1)

2) Fractional-N PLLs: In case of Fractional-N PLLs, one possible approach to generate the high frequency sampling
clock is to split the Fractional-N divider in the feedback path into two parts $M$ and $N_1, f_1$ as shown in Fig.3, where $N_1, f_1 = N, f/M$. The output of the fractional divider $N_1, f_1$ gives the oversampling clock $Mf_r$. There are two problems with this approach, 1) Like any Fractional-N clock, the oversampling clock period changes every cycle and is only equal to $Mf_r$, on an average and 2) The $\Sigma-\Delta$ noise of the Fractional-N PLL is now increased as the quantization step size seen at the PFD input increases by $20\log_{10}(M)$.

To avoid the aforementioned problems, the oversampling clock $Mf_r$ is derived from the reference clock directly using a frequency multiplying PLL (MPLL) as shown in Fig.4. The jitter of the MPLL is not a major concern (as it only affects the sampling instant and not the charge injected into the loop filter) and hence the MPLL can be realised with much lower power (using ring oscillator based VCO) and smaller area compared to the Fractional-N PLL. The OSLF technique is used in the MPLL as well to ensure the oversampling signal $Mf_r$ does not contain any reference spurs. The output of the MPLL is chosen to be twice the oversampling frequency $f_{\text{mvco}} = 2Mf_r$, so that the signal $S_{os}$ has a 50% duty cycle.

3) *Choosing the delay $T_D$: The delay should be chosen such that the signal $S_{os}$ is 'low' at the beginning of the reference cycle when the CP current is not zero as shown in the shaded region in Fig.5.(a). Let $\Delta_{\text{max}}$ be the maximum phase excursion seen at the PFD input in the steady state. Then the signal $S_{os}$ should be delayed by $T_D$ seconds such that $T_D > \Delta_{\text{max}}$. Furthermore, since the frequency of the signal $S_{os}$ is much higher than the reference frequency, it should be ensured that the off-time of $S_{os}$, $T_{off} = T/2M > \Delta_{\text{max}} + T_m$, where $T_m$ is an additional time margin given to ensure that $S_{os}$ does not go 'high' in that region. This condition puts an upper limit on the value of $M$.

In case of Integer-N PLLs, the delay $T_D$ can be rounded-off to the nearest integral multiple of $0.5T_{\text{vco}}$ and realised using a series of flip-flops clocked at the alternate edges of VCO clock as shown in Fig.5.(b). The output of the flip-flops change at the oversampling frequency of $Mf_r$ and the power consumed in the delay element will be a small fraction of the frequency divider ($N_1$ in Fig.2) in the feedback path.

In case of Fractional-N PLLs the steady state phase error is much higher in comparison to Integer-N PLLs. The delay $T_D$ can be realised in a much simpler way by exploiting the multi-stage ring oscillator in the MVCO. In this work, the MVCO is designed as a four stage differential ring oscillator running at $2Mf_r$ and thus the oversampling clock $Mf_r$ can be delayed in steps of $T/16M$. The delay $T_D$ can be rounded-off to the nearest multiple of $T/16M$ and then realised using a single flip-flop clocked by one of the eight appropriate phases ($q_i$) of the MVCO as shown in Fig.5.(c). The same sampling signal can be used in the MPLL as well to save power.

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1Another point to note is that the MPLL output can in theory be used as a reference input to the Fractional-N PLL there by removing the reference spurs upto $Mf_r$ (and even reducing the $\Sigma-\Delta$ noise). However this approach has two major problems 1) The power of the PLL increases as the $\Sigma-\Delta$ modulator operates at $Mf_r$ and 2) The MPLL clock is very noisy and this will significantly increase the in-band noise of the Fractional-N PLL.

2$\Delta_{\text{max}}$ can be estimated from the behavioural level simulations of the PLL.
The phase margin \( n \) = \( (\pi - \phi) \) seconds apart as shown in Fig.6. In both.

\[ Z_{\Delta} = (\Delta Z_p, S) \]

\[ S_{\Delta,OSLF}(f) = (2M Q_m, f_r) \sum_k \delta\left( f - (2k + 1)M f_r \right) \]

The reference spur at the PLL output can be shown to be [1], [2], [3], [4]

\[ S_{\delta}(f_r) = 10\log_{10} \left( \frac{Z(f_r)K_v}{2k f_r} \right) \]

The highest spur level difference in both the techniques can be computed from Eq.(2), Eq.(3) and Eq.(4)

\[ S_{\delta,OSLF}(M f_r) - S_{\delta,SLF}(f_r) = -20\log \left( \frac{Z(f_r)}{Z(M f_r)} \right) \]

\[ \approx -20P \log(M) \]

where \( P = N_p - N_c \) is the difference between the number of poles \( N_p \) and zeroes \( N_c \) of the impedance \( Z(s) \). Thus the highest spur level in OSLF technique is \( 20P \log(M) \) lower than the highest spur in SLF technique.

**IV. Simulation Results**

A 2.4 GHz output PLL with a \( f_r = 20\) MHz reference frequency as shown at block level in Fig.7 is simulated to validate the proposed technique. The PLL is a Type-II PLL with two poles at DC, a stabilising zero and two high frequency poles after the unity gain bandwidth to reduce spurs. The parameters of the PLL are chosen to optimise the integrated jitter at the PLL output. The UGB of the Fractional-N PLL is \( f_u \approx 400\) kHz. The zero is placed at \( f_z = 100\) kHz, and the poles are at \( f_{p1} = 1.67\) MHz and \( f_{p2} = 8\) MHz. The phase margin of the PLL is \( \approx 60^\circ \). The nominal divide value in Integer-N mode is \( N = 120 \) and in Fractional-N mode \( N.f = 120.333 \). The VCO gain is \( K_v = 200\) MHz/V.

An offset is introduced in the PFD/CP characteristics by adding a mismatch in the reset path of the UP and DN signals to reduce the \( \Sigma - \Delta \) noise folding into the in-band due to the PFD/CP non-linearity [3], [10], [11], [12]. The MPLL on the other hand was designed to keep its area and power minimum. So the UGB of the MPLL is chosen to the maximum value of \( f_r/10 = 2\) MHz. The value of \( M \) is chosen to be 4.

All the blocks in the PLL are modeled behaviorally except the loop filter (including the CMOS switches) of the Fractional-N PLL and the MPLL, which are at schematic level. The devices used in the sampling switch are from the UMC 180nm CMOS process. A 5% mismatch in the CP current is modeled as shown in Fig.7. The VCO and the fractional divider were modeled with a combined VCO and divider model to reduce simulation time [13]. A 3rd-order \( \Sigma - \Delta \) MASH 1-1-1 modulator [14] was used to generate the divide value for the fractional part. To measure the reference spurs, the PLL is simulated in the Fractional-N mode in a transient simulation.

3To measure reference spurs in the Integer-N mode, the PLL can be locked in a periodic steady state (pss) simulation. Once the PLL is locked, using the Narrow band FM approximation [2], [4], the reference spurs can be obtained by passing the spectrum (obtained from the pss simulation) of the control voltage through the VCO transfer function \( K_v/2f_r^2 \). As there is no periodic steady state operating point in Fractional-N PLLs, a transient simulation with the same accuracy settings as a pss simulation was performed.
The phase noise (and the reference spur) at the PLL output can be estimated by computing the PSD of control voltage and then passing it through the VCO transfer function \( |K_v/2f|^2 \) to compute the one-sided PSD as shown in Fig.7.

Fig.8 shows the simulated phase noise of the SLF and OSLF PLL. It can be seen from the figure that the spurs up to 4\( f_r \) are absent in the OSLF technique. This is in close agreement with the analytical result given in Eq.(6), \(-20 \cdot P \log(M) = -40 \log(4) = -24 \text{dB}\). It should be noted that the spur at 4\( f_r \) in OSLF PLL can be further reduced by introducing additional poles in the loop filter after the reference frequency without affecting the phase margin of the PLL.

Now to study the area and power overhead due to the addition of the MPLL in the Fractional-N mode, the charge pump, VCO and divider currents of the MPLL are compared to that of the main Fractional-N PLL. To compare the VCO and divider power, schematic level simulations were carried out on the VCO, MVCO, frequency divider and delay circuits. The VCO is realised using a four-stage differential ring oscillator in both the Fractional-N PLL and MPLL. The schematic of the delay cell (current source is also at schematic level, but the details are not shown in the figure) used in the VCO is shown in Fig.9. For the Fractional-N PLL, the VCO is designed for a phase noise of -90 dBc/Hz at 1 MHz offset from the carrier and the MVCO is designed with 5% of the current of the main VCO. The capacitance and current in the delay cell are adjusted to get the center frequency of the main VCO and MVCO to 2.4 GHz and 160 MHz respectively. The frequency divider in the feedback path is implemented in CMOS logic in both the Fractional-N PLL and the MPLL. Table I shows the current consumption of the individual blocks and the loop parameters of the two PLLs.

| Parameter             | Frac-N PLL | MPLL   |
|-----------------------|------------|--------|
| Loop-filter \( (C_z) \) | 526.3 pF   | 15.83 pF |
| Loop-filter \( (C_p = 2C_s) \) | 33 pF     | 1 pF   |
| \( I_{cp} \) (mA)    | 0.5        | 0.025  |
| VCO current (mA)     | 1.51       | 0.08   |
| Divider(+delay) Current (mA) | 0.370     | 0.05   |
| Total Current (mA)   | \( \approx 2.4 \) | 0.13   |
| RMS integrated Jitter (ps) | 5.738     | \( \approx 50 \) |

It can be seen that the added MPLL increases the overall current consumption of the PLL by < 6% (the power consumed in the \( \Sigma \Delta \) modulator of the Fractional-N PLL is not included) and the loop filter area by < 2%. Thus the increase in area and power is not very significant.

V. CONCLUSION

Reference spurs in CP PLLs can be eliminated in both Fractional-N and Integer-N PLLs by applying the proposed OSLF technique. In case of Integer-N PLLs, it was shown that reference spurs can be completely eliminated by an insignificant power and area overhead. In case of Fractional-N PLLs, the reference spurs can be eliminated with an insignificant (< 6%) increase in power and area.
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