Failure Characterization and Analysis of Sub-module of Press-Packed Devices in High Temperature Reverse Bias Test

Hao Ma*, Zhenshuo Wang, and Xuebao Li
School of Electrical and Electronic Engineering, North China Electric Power University, Changping District, Beijing, 102206, China
*Corresponding author’s e-mail: mahao@ncepu.edu.cn

Abstract. The failure of sub-module of press-packed devices in course of high temperature reverse bias (HTRB) test was investigated in this paper. A high temperature reverse bias test platform for press-packed devices was built, which was capable of monitoring and collecting continuous leak current data of devices during the test. Through the analysis of the static characteristics of the chip before and after the high temperature reverse bias test, a method that uses the combination of IV and CV characteristic curves to characterize high temperature reverse bias failure was proposed. By means of finite element analysis to locate the reasons for the change of static characteristics, the accumulated charges around the terminal of chip were considered to be the primary source for the failure of sub-module under the HTRB test.

1. Introduction
Turning the basically uncontrollable grid into fully controllable one, Voltage Source Converter based High Voltage Direct Current (VSC-HVDC) transmission improves the security, reliability and economy of the power system [1][2]. The press-pack power device has the characteristics of large current capacity, easy series connection and short-circuit failure, and is especially suitable for applications in the field of flexible DC transmission [3]. As the core component in the key rectification and inverter links of flexible DC transmission, the reliability of press-pack power devices is profoundly important in actual operation. It’s quite essential for press-pack power devices to maintain reliable blocking capabilities under long-term high temperature and high voltage stress. The High Temperature Reverse Bias (HTRB) test effectively screens power semiconductor devices and improves the high temperature reliability. And it is particularly effective for removing early failure devices with surface effect defects.

Although the failure criterion after the HTRB test varies in different standards and companies, the current mainstream characterization quantity is the leakage current in the test. To provide more abundant device information to facilitate failure analysis, scholars have also explored the characterization methods of device high temperature reverse bias failure.

In 2012, Pomès adopted a new method to characterize MOSFET failure caused by electric charge. The measurement of QBD (charge to breakdown) is carried out directly at the probe-chip-wafer level [4]. In 2017, Hu Jie analyzed the failure in HTRB test through experiments and simulations. Combining the simulation results with the experimental results, they obtained the distribution of the two-dimensional electric field to characterize the failure [5]. Apart from using electrical characteristics, image methods could also be utilized to inspect the internal failure. Zhu J. studied the breakdown voltage and on-resistance degradation of MOSFET under HTRB stress. On account of the application of electron microscope images, HTRB failure is effectively characterized [6]. Different characterization methods correspond to different application scenarios. The leakage current method is suitable for routine
inspection and screening of failed devices. The two-dimensional electric field distribution is suitable for locating the failure point of the device. And the image method is suitable for confirming the location and type of physical defects. There is still a need for a characterization method that can clearly characterize the HTRB failure of the device and provide more abundant electrical information for HTRB failure research.

In terms of the study of failure characteristics, Infineon studied the service life of soldered packaged diode during the HTRB test and analyzed the influence of temperature and voltage on the service life of the device. The results showed that the package structure and chip-related effects may cause device failure under HTRB stress. Hitachi’s Matsushima et al. studied the terminal charge accumulation mechanism of VLD-terminated SiC diodes under the conditions of HTRB and found that different terminal structures can suppress surface charges and their abilities to improve the breakdown voltage [7]. From a statistical perspective, Yidan Tang studied the effects of high temperature and reverse bias voltage on the reliability of 4H-SiC under high temperature reverse bias conditions [8]. Yet the HTRB failure characterization of press-pack devices still need further supplements. Especially for press-pack power devices, there is a lack of HTRB failure research. And characterization method and pattern of high temperature reverse bias failure remain to ascertained.

Therefore, taking the press pack FRD sub-module as the research object, this paper builds a high-temperature reverse bias test platform for the press-pack device, and conducts the high-temperature reverse bias test of the sub-modules. The failure of the sub-module under high temperature reverse bias conditions was effectively characterized by the static characteristics of IV and CV. Furthermore, the finite element simulation tool was taken to analyze the high temperature reverse bias failure characteristics of the device. It provides data support and theoretical basis for the design optimization and practical application of high voltage and press-pack devices.

2. Experimental setup

In the HTRB test, the semiconductor chip is applied with a reverse bias voltage. At the extreme operating temperature, the applied reverse bias voltage is slightly lower than the blocking voltage of the device. It is expected that bulk silicon devices will not degrade at these temperatures, but experiments have revealed weaknesses or degrading effects in the field depletion structure at the edges of the device and the passivation layer. Therefore, the main objective of the HTRB test is the long-term reliability of the device terminal, passivation layer, and package structure. The commonly used standard in the high temperature reverse bias test is the IEC60747-9 standard, which provides a practical operating standard for the high temperature reverse bias test of power devices.

Therefore, an HTRB experiment platform for press-pack devices was built according to the above-mentioned standard, as shown in figure 1. The experimental platform focuses on the design of press-pack devices from three aspects: pressure equalization, heating control, and leakage current monitoring. In terms of pressure application, the experimental platform has designed a fixture for press-pack devices, which is capable of performing multi-level press-pack device HTRB experiments with sub-modules and single chips. The three studs and disc springs of the fixture ensure uniform pressure application on the sub-module to be tested, maintaining the pressure balance during the HTRB test.

![Figure 1. Platform for HTRB test of press-pack devices.](image)

In terms of heating control, the PI control heating stage of this platform can adjust the chip temperature in real time and apply high temperature conditions flexibly. In terms of leakage current monitoring, the platform could monitor and record failure leakage current characteristics online. The
nanovoltmeter monitors real-time leakage current recording leakage current data at a sampling frequency of 30 points/minute, uploading it to the PC via GPIB wire. The measured leak current curve is shown in Figure 2. In addition, the maximum voltage level of the experiment can reach 20kV, and the maximum temperature can reach 400°C.

As shown in figure 2, leakage current curve shows an upward trend rising from 1 mA to 1.3 mA at the beginning of the experiment, and then maintain rising gently around 1.3 mA. In this process, whenever a sub-module fails, the curve rises sharply, as shown in the above figure around 400h and 800h. After the failed device is replaced, the curve returns to the original trend.

The sample used in this paper is a press-pack fast recovery diode device. The FRD sub-module used in the experiment contains a PEEK frame package and a diode chip with a rated voltage of 3300V field limiting ring terminal structure, as shown in figure 3. The HTRB experiment of the FRD sub-module was carried out on the experimental platform. During the experiment, the Agilent power device analyzer B1505A was used to measure the static characteristics of the submodule before and after the high temperature reverse bias experiment.

3. Results and Analysis
The I-V and C-V electrical characteristic of the chip were measured before and after the high-temperature reverse bias experiment, and the failure characteristics of different package structures at the sub-module level were obtained by means of characteristic curves. During the experiments, the failed sub-modules could not maintain the rated voltage withstand capability and lost the blocking performance. Compared with non-failed devices, the I-V characteristics of the failed sub-modules will show a sudden increase in the tail, and the leakage current cannot maintain the holding voltage if the leakage current exceeds the limit, and the breakdown voltage significantly below the rated voltage. The static characteristic curves of the failed sub-modules are shown in figure 4 and figure 5, respectively.
Figure 4. I-V characteristic curve

Figure 5. C-V characteristic curve.

The research results show that after the high temperature reverse bias experiment, the static electrical characteristic curve can be clearly distinguished from the one before the experiment, so it is very appropriate to serve as a high temperature reverse bias failure characterization method. And compared to leakage current, two-dimensional electric field, and image methods, it can provide more electrical information to further analyze the characteristic changes caused by high temperature and high reverse voltage acting on the device for a long time. Considering the changes of the I-V and C-V characteristic curves, indeed the accumulated charge around the field ring was implied.

Besides, it has been noticed that there is a correlation between the change of the capacitance which equals the capacitance after HTRB failure minus the one before HTRB test and the change trend of the current curve. The capacitance change named by $\Delta C$ and voltage curve are shown in the figure 6.

Figure 6. $\Delta C$-V characteristic curve

It can be seen from figure 6 that the capacitance change $\Delta C$ rises rapidly at the beginning of the voltage application, and then remains almost unchanged. At the end of the application voltage, that is, around 2500V, the $\Delta C$ abruptly rises again. The correlation between C-V characteristic curve and I-V characteristic curve may imply more details of charge accumulation around field limiting ring terminal structure in device failure under the combined action of high electric field and high temperature.
4. Discussions

4.1. The effect of interface charge accumulation on I-V and C-V characteristics
For the field limiting ring terminal structure, the interface charge accumulation is an important cause of high-temperature reverse bias failure. And the interface charge has a significant impact on the withstand voltage of high-voltage devices with field limiting ring terminal structure [9]. The edge termination area structure of FRD shows in figure 7. The accumulation of interface charges reduces the breakdown voltage of the p-n junction of the terminal field ring and increases the reverse leakage current. Due to the electrostatic induction of the movable ion charge on the silicon surface, the surface of the field ring and the passivation layer is inverted, resulting in a channel. Therefore, the breakdown voltage decreases and the leakage current increases.

\[
\frac{1}{C^2} = 2\varepsilon q \frac{N_a N_d}{N_a + N_d} V_R
\]

where \( \varepsilon \) is the permittivity, \( q \) is the elementary charge, \( N_a \) is the acceptor concentration of field limiting rings, and \( N_d \) is the donor concentration of the epitaxial layer. Since \( \varepsilon \) is the constant, \( d(1/C^2)/dV_R \) is equivalent to a variation in \( N_a N_d/(N_a+N_d) \) of depleted region at a certain voltage.

In the process of depletion of the field ring, the donor concentration in the substrate area remains unchanged, while the acceptor concentration in the field ring area gradually decreases as the depletion layer is completely depleted, and the applied reverse voltage gradually increases, so it can be obtained that the capacitance curve is a negative square change. With the accumulation of electric charge caused by high temperature and high field strength for a long time, that is, the increase in the amount of electric charge, the capacitance curve gradually shifts down, that is, a negative capacitance change occurs, which is consistent with the law obtained by the experiment.

4.2. The influence of interface charge on static characteristics by simulation
Using experimental testing methods to quantitatively analyze the impact of the interface charge accumulation on the failure characteristics of the press-fit sub-modules is difficult to produce test samples, that is, it is difficult to artificially control the concentration and area of charge accumulation. The finite element method can be used to flexibly establish this failure form and its failure characteristics.

The distribution of the interface charge product at the terminal of the field ring is shown in figure 8. Structural modeling of the analytical parameters of FRD, using simulation software Silvaco to simulate the FRD during the process of HTRB test, in order to simulate the influence of the interface charge introduced in the HTRB experiment on the device.
In course of simulation of the FRD, the software Silvaco calculates basing on three equations determining the electrical characteristics of semiconductor devices, the Poisson equation, the continuity equation of electrons and holes, and the current density equation. After the simulating calculation, the results are to be attained, including the electric field intensity distribution map.

During the simulation process, a concentration of $1 \times 10^{11}$ cm$^{-2}$ interface charge was applied to the FRD simulation model to obtain the electric field intensity distribution map shown in figure 9 and changes in device characteristics before and after charge application shown in figure 10 and figure 11.

Owing to that the interface charge is concentrated at the field ring surface area, the electric field distribution near the p-n junction of the field ring is changed. The increase in electric field intensity creating weak points, raising risks of breakdown, which further reduces the breakdown voltage.

Figure 8. Schematic diagram of cross-section of terminal interface charge.

Figure 9. The distribution of the electric field at the terminal when interface charges accumulate.

Figure 10. Comparison of I-V characteristic curves before and after interface charge is applied to the device terminal.

Figure 11. Comparison of C-V characteristic curves before and after interface charge is applied to the device terminal.
As it can be seen from the above figure, in the simulation calculation results after the interface charge is applied, the breakdown voltage indicated by the I-V characteristic has decreased, and the interface charge has increased compared with before the interface charge is applied. The capacitance value indicated by the C-V characteristic has dropped, and this trend is consistent with the change in the static characteristics shown by the experimental results.

In addition, the chip has been simulated and calculated on the characteristics of I-V and C-V with different interface charge concentrations and different temperatures. The results are shown in figure 12 and figure 13.

![I-V characteristic curves with surface charges in different concentration.](image1)

**Figure 12.** I-V characteristic curves with surface charges in different concentration.

![C-V characteristic curves with surface charges in different concentration.](image2)

**Figure 13.** C-V characteristic curves with surface charges in different concentration.

As shown above, the obtained rule is the same as the result of comparing characteristic curves before and after interface charge is applied. As the amount of charge increases, the breakdown voltage gradually decreases. While in the non-breakdown interval, the capacitance gradually decreases with the increase of the charge amount. Therefore, the reason for the failure of HTRB can be located at the accumulation of interface charges under the combined action of high temperature and high field strength.

5. Conclusion
This paper built a high temperature reverse bias experiment platform for press-pack power devices. The HTRB experiments on 3.3kV press-pack FRD devices were conducted. A method to characterize failure conditions using static test C-V and I-V characteristic curves was proposed. Besides, through finite element analysis and simulation for the influence of interface charges on the change of static characteristics, the cause for HTRB failure of the FRD sub-module was the accumulation of the interface charges under the interface charges was the combined action of high temperature and high voltage electric field.

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