A 0.11–0.38 pJ/cycle Differential Ring Oscillator in 65 nm CMOS for Robust Neurocomputing

Xueyong Zhang\textsuperscript{\textdagger}, Graduate Student Member, IEEE, Jyotibdha Acharya\textsuperscript{\textdagger}, Member, IEEE, and Arindam Basu\textsuperscript{\textdagger}, Senior Member, IEEE

Abstract—This paper presents a low-area and low-power consumption CMOS differential current controlled oscillator (CCO) for neuromorphic applications. The oscillation frequency is improved over the conventional one by reducing the number of MOS transistors thus lowering the load capacitor in each stage. The analysis shows that for the same power consumption, the oscillation frequency can be increased about 11\% compared with the conventional one without degrading the phase noise. Alternatively, the power consumption can be reduced 15\% at the same frequency. The prototype structures are fabricated in a standard 65 nm CMOS technology and measurements demonstrate that the proposed CCO operates from 0.7 – 1.2 V supply with maximum frequencies of 80 MHz and energy/cycle ranging from 0.11 – 0.38 pJ over the tuning range. Further, system level simulations show that the nonlinearity in current-frequency conversion by the CCO does not affect its use as a neuron in a Deep Neural Network if accounted for during training.

Index Terms—Ring oscillator, low-power, neuromorphic, neurocomputing.

I. INTRODUCTION

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EEP Neural Networks (DNN) are gaining popularity recently in many applications such as face recognition [1], speech recognition [2], natural language processing [3] etc due to improved performance compared to other machine learning algorithms. Deploying these networks at the edge in the Internet of Things (IoT) is important for scalability and fast response by reducing data transmission to the cloud [4], [5]. However, due to battery life and processing constraints, it is imperative to have low power, low area implementations of the DNN.

Neuromorphic implementations that utilize analog or physical computing are good in that context [6] and have been known to be energy efficient compared to digital baselines when the required precision is low [7]. Neuro-inspired spiking neural networks (SNN) have also gained popularity due to the promise of sparse activation leading to lower energy dissipation [8]. In recent years, time-based computational circuits for DNN/SNN are gaining popularity due to the reduced power supply in scaled CMOS [9], [10]. An important building block in these designs is a digital delay cell. For example, it is used to create an oscillator that can convert analogue current to digital output (rate based neuron) in [11]–[13] or be used as an integrate and fire neuron [9] with bio-plausible refractory period and spike frequency adaptation features. The major requirements for an oscillator to function as a neuron are:

- Low area requirement since a large number of them are needed per chip.
- Low energy/cycle to reduce operational energy.
- Since these circuits typically co-exist with a large amount of digital circuits, they have to be robust against power supply noise and other interference.

Interestingly, for NN implementations, linearity of the tuning curve of the oscillator-based neuron is not important since learning can be used to correct for it.

Given these requirements, a CMOS ring oscillator (RO) based structure seems like a good choice due to its low-area and power requirements. To address the third point of robustness, differential ring oscillators should be the preferred topology [14]. In this paper, we propose a new differential delay cell that has reduced number of transistors compared to the conventional one thus reducing energy/cycle due to lower capacitance. Note this is different from [15] where the authors demonstrate reducing the number of stages. Given the popularity of rate based SNN converted from pre-trained artificial neural network (ANN) [16], [17], we show results from a fabricated chip in 65 nm CMOS where the proposed delay cell is used in a differential ring oscillator to convert input analog currents to a frequency or rate. Nevertheless, the proposed delay cell can be used in conventional mixed signal applications as well as differential delay line based neural networks [10]. Further, other neuromorphic computation using coupled oscillators are also gaining in popularity [18], [19]—the proposed oscillators can be used for such computations as well.

This paper is organized as follows. Section II gives a review of conventional ring oscillator based CCO (RO-CCO) structures. The proposed structure and analysis are introduced in section III. Section IV presents measurement results and shows a performance comparison. Section V discusses the neural network simulation with the proposed CCO neuron model, its potential for usage in spiking neural networks.
II. CONVENTIONAL RO-CCO REVIEW

A RO is made from gain stages, or delay stages, in feedback. ROs can be built in any standard CMOS process with a number of delay stages connected in a feedback loop.

A single ended RO is comprised of odd stages of inverters cascaded in self-feedback (Fig. 1(a)) with capability of rail-to-rail output. The most common way to derive an equation for the oscillation frequency of an $N$-stage ($N$ is an odd number) ring oscillator is to assume each stage provides a delay of $t_d$. For a stable oscillator, the signal must go through each of the delay stages twice to provide one period of oscillation, as shown in Fig. 1(a). Therefore, the period is $2Nt_d$, resulting in the oscillation frequency equation

$$f = \frac{1}{2Nt_d} = \frac{I_{ss}}{2NC_LV_{SW}} \propto \frac{I_{ss}}{C_L}.$$  

(1)

where $I_{ss}$ is the tail current, $C_L$ is the total load capacitance of a single stage, $V_{SW}$ is the amplitude of the voltage swing. Delay of each stage $t_d$ is defined as the time interval of output signal and input signal of the same stage at half $V_{DD}$, illustrated in Fig. 1(a). The propagation delay $t_d$ is the most important parameter of this type of oscillator because it directly determines the oscillation frequency, the number of stages and hence determines the number of output phases and the power consumption. Moreover, the stability of delay time $t_d$ also reflect the jitter characteristics in time domain and phase noise in frequency domain.

Eliminating the restriction of odd number of stages in single ended RO, pseudo differential RO is more flexible as well as the startup circuits. Finally, the conclusions are provided in section VI.

III. DIFFERENTIAL RO-CCO REVIEW

Since both odd and even stages are allowed. A 4-stage pseudo differential RO [14] is shown in Fig. 1(b). A single delay stage is composed of four inverters, in which two inverters work as pseudo differential structure, while another two grey inverters constitute cross-coupled regeneration to generate hysteresis phase shift. Differential RO can offer more output phases compared with single ended RO with the same stages. This is a very important criteria in time domain processing circuits especially where multiple phases are necessary for more accuracy operations.

Although single ended configurations consume less area, they are more susceptible to power supply variations and common-mode noise. In modern machine learning accelerators with analog computing neurons co-existing with digital memory and processing, it is extremely important to...
ensure good noise rejection properties for the analog blocks. A pseudo differential RO can suppress common mode noise and have a better common mode rejection ratio (CMRR) characteristic [14].

To further reduce the sensitivity to power supply variation and noise disturbance, current starved structures, as shown in Fig. 1(c), have been introduced [20], [21]. Since the current source and current sink transistors offer a negative feedback in the bias, the current variation is much less than non current starved structures. Another important advantage is that the current starved structures control the output frequency by controlling the bias current, resulting in the name of current controlled oscillator (CCO).

Finally, combining current starving and differential architecture, current starved fully differential RO (Fig. 1(d)) has better power supply rejection ratio (PSRR) and CMRR characteristics than other types of RO (shown later in Fig. 5). The power supply noise and substrate noise are isolated by current source and current sink, resulting in a better PSRR. Common mode disturbances such as temperature variations can also be suppressed by the differential structure.

Although in practice, current starving transistors are shared by all stages, it is easier to understand the operation of an unit delay cell by assigning a current source and a current sink to it. Fig. 2 shows the single delay stage of current starved fully differential RO. MN1, MP1 and MN2, MP2 constitute the differential input and differential output pair. MN3, MP3 and MN4, MP4 constitute the positive feedback latch to offer hysteretic phase shift. The controllable current source and current sink, MP5 and MN5, make the delay stage from pseudo differential structure to fully differential. The core stage is composed of a differential input-output path and a hysteresis delay cells (HDC) composed of two cross-coupled inverters based positive feedback latch.

III. PROPOSED STRUCTURE AND THEORETICAL ANALYSIS

As mentioned in Section I, two important metrics for oscillators used for neurocomputing are: (a) high resistance to common-mode noise and (b) low energy/cycle. While the former was addressed through a current starved fully differential architecture as mentioned in the previous section, we address the latter in this section. However, lowering energy is often associated with an increase in thermal noise induced jitter. We propose a new oscillator structure that is better than conventional structure in terms of energy/cycle while not adversely affecting the jitter performance.

A. Proposed Oscillator

From the analysis of conventional ring oscillators in section II and simulations shown later in this section (Fig. 5), we know that current starved fully differential structure has both better PSRR and CMRR. To offer differential inputs, outputs and a positive feedback hysteresis, each stage of the conventional differential RO uses four inverters (i.e. 8 transistors) except for the current starved transistors (Fig. 2). Our novelty stems from the observation that only four transistors seem necessary to realize oscillation as shown in Fig. 3(a). MP1 and MN2 are the pull-up and pull-down differential I/O pair while MN3 and MP4 serve as their loads respectively. At the same time, MN3 and MP4 constitute the simplest dynamic positive feedback latch. Another way to interpret this proposed structure is as follows: MP1 and MN3 constitute a dynamic inverter since outn and inp are almost the same (with a certain phase shift), similarly, MP4 and MN2 constitute another dynamic inverter since outp and inn are almost the same (with a certain phase shift). Likewise, the two dynamic inverters compose the regeneration cross pair to generate positive feedback and offer extra hysteresis phase shift. Every transistor acts as an active device for itself and a load device for another transistor. The push-pull nature and transistor reuse make the cell compact and efficient.

However, one problem is that inp and inn are strictly inverse only when oscillations have been sustained, while outn and outp are inverse with a phase delay of 180°/N. If for some reason, the initial condition of inp and inn (Fig. 3 (a)) are same at say 0 V, then outp is guaranteed to be pulled up to...
$V_{DD}$ but the condition of outn stays at initial condition since both MN2 and MP4 are OFF. If initial condition of outn was $V_{DD}$, then the outputs of this stage are both at high voltage and the oscillator gets locked in this state and cannot start oscillating. So a start-up circuit is necessary to maintain robust oscillations. Only a NMOS or PMOS or both (Fig. 3(b)) can oscillate. So a start-up circuit is necessary to maintain robust and the oscillator gets locked in this state and cannot start of this stage to be opposite in polarity thus breaking the lock state earlier. From SPICE simulations, the structure with start-up of both NMOS and PMOS as shown as Fig. 3(g), gives the best frequency performance (see Section V) and is adopted in the rest of the paper.

B. Frequency and Energy Dissipation

The novelty in our design of reducing the number of transistors should lead to an increased oscillation frequency per unit current. However, the charging currents also change and hence the combined effect is not obvious. Intuitively, the proposed delay stage offers less charging and discharging current by removing MP3 and MN4, which cuts down on power consumption. To precisely compare the charging/discharging current and the effect on the output frequency, we analyze the load capacitance and charging current model of a single stage in more details to present a theoretical prediction.

First, the load capacitor of each stage for the conventional structure (Fig. 2) is given by:

$$C_{L,conv} = C_{gdP1} + C_{gdn1} + C_{gdP3} + C_{gdn3} + C_{gP4} + C_{gN4} + 2C_{g,NextStage} = 4C_{gd} + 4C_g = 8C_{gd} + 4C_{gs}. \quad (2)$$

In comparison, for the proposed structure (Fig. 3(b)), it reduces to

$$C_{L,prop} = C_{gdP1} + C_{gdn1} + C_{gdP3} + C_{gP4} + 2C_{g,NextStage} = 3C_{gd} + 3C_g = 6C_{gd} + 3C_{gs}. \quad (3)$$

Thus, $C_{L,prop} = 3/4C_{L,conv}$. It is therefore reasonable to expect that the load capacitor decreases by 25% since the number of transistors of each stage decreases by the same amount.

Next, we analyze the charging process of the node of outp in Fig. 3(b), while the discharging process is same as the node of outn. Fig. 3(c) illustrates the charging period, which is divided into four phases (A, B, C and D) according to the operation of the transistors. $V_{max}$ and $V_{min}$ are the swing range of the oscillation, which is lower than rail-to-rail because of the current starved structure. In our design, $V_{max} \approx 900$ mV, $V_{min} \approx 300$ mV, and $V_{cm} \approx 600$ mV. For simplicity, we assume that $V_{TH} = |V_{TP}| = V_{T}, \Delta V_1 = \Delta V_4 = 50$ mV and $\Delta V_2 = \Delta V_3 = 250$ mV such that

$$\sum_{i=1}^{4} \Delta V_i = V_{max} - V_{min} = 600 \text{ mV}.$$

$$I_{d,conv} = \frac{C_{L,conv} \Delta V_1}{I_{1,conv}} + \frac{C_{L,conv} \Delta V_2}{I_{2,conv}} + \frac{C_{L,conv} \Delta V_3}{I_{3,conv}} + \frac{C_{L,conv} \Delta V_4}{I_{4,conv}} \quad (4)$$

$$I_{d,prop} = \frac{C_{L,prop} \Delta V_1}{I_{1,prop}} + \frac{C_{L,prop} \Delta V_2}{I_{2,prop}} + \frac{C_{L,prop} \Delta V_3}{I_{3,prop}} + \frac{C_{L,prop} \Delta V_4}{I_{4,prop}} \quad (5)$$

where, $I_{1,conv}$ and $I_{1,prop}$ represent charging current in four different phases of conventional and proposed stage respectively, which are given by

$$I_{l,conv} = I_{MP1} + I_{MP3} - I_{MN3}, \quad i = 1, 2, 3, 4. \quad (6)$$

$$I_{l,prop} = I_{MP1} - I_{MN3}, \quad i = 1, 2, 3, 4. \quad (7)$$

The equations and approximated average values of $I_{MP1}$, $I_{MP3}$ and $I_{MN3}$ in all phases are listed in Table I, where the charging process is divided into the four phases A, B, C and D as mentioned earlier. The regions of operation of the MOSFETs are referred to as 0, 1 and 2 for cut-off, linear and saturation respectively.

The drain current of short-channel MOSFETs is assumed to follow the widely used alpha power law [22], [23]. The carrier velocity saturation coefficient $\alpha$ is between 1.2 to 1.5 for sub-micron CMOS technology. Then, according to the above equations and the estimated values in the table, we can get the propagation delay relationship between the proposed and conventional RO as $I_{d,prop} = 88.4\%I_{d,conv}$, Thus, the relation between the frequencies are:

$$\frac{f_{prop}}{f_{conv}} = 1.156. \quad (8)$$

This means that the frequency of proposed RO increases 15.6% compared with conventional structure for the same input current. From equation 1, the average current relationship is expressed as:

$$\frac{I_{prop}}{I_{conv}} = \frac{f_{prop}C_{L,prop}}{f_{conv}C_{L,conv}} = 0.867. \quad (9)$$

This implies the average current of the proposed RO decreases by 13.3% compared to the conventional structure.

To verify these theoretical models, we conducted the current-frequency (I-F) transfer curve simulations of the conventional and proposed 4 stage RO using 65 nm CMOS models in SPICE. Fig. 4 shows the simulation results and the theoretical prediction results of the output frequency. As predicted, the proposed oscillator indeed produces higher frequency than the conventional one for the same input current. However, the theoretical values are slightly greater than that of simulation because of the inaccuracy in estimation of the current of the transistor MP3.

C. Robustness and Jitter

While the increase in oscillation frequency is good, it is not useful if the new oscillator has a degradation in other key metrics such as robustness and jitter. We first evaluate
TABLE I
COMPARISON OF CHARGING AND DISCHARGING CURRENT OF EACH CONTRIBUTORY TRANSISTORS FOR A CHARGING NODE IN FOUR PHASES, WHERE $\beta = \mu_0 C_{ox} W/L$. $\beta$ OF NMOS AND PMOS ARE THE SAME ASSUMING PROPER SIZING TO NOMINALLY MAXIMIZE NOISE MARGIN. REGION 0, 1 AND 2 REFER TO CUT-OFF, LINEAR AND SATURATION REGIMES OF OPERATION OF THE MOSFET.

| Phase | MP1 | MP3 | MN3 |
|-------|-----|-----|-----|
| A     | region=2 $v_{sg} \uparrow: V_{max} - V_{cm} \rightarrow$ $V_{max} - V_{min} \rightarrow 50mV$ $v_{sd} \downarrow: V_{max} - V_{min} \rightarrow$ $V_{max} - V_{min} \rightarrow 50mV$ $I = 1/2 \times \beta (v_{sg} - V_T)^{\alpha} \uparrow$ $T \approx 0.02\beta$ | region=0 | region=0 $v_{gs} \downarrow: V_{max} - V_{min} \rightarrow$ $V_{max} - V_{min} \rightarrow 50mV$ $v_{ds} \uparrow: 0 \rightarrow 50mV$ $I = \beta (v_{gs} - V_T)^{\alpha/2} v_{ds} \uparrow$ $T \approx 0.01\beta$ |
| B     | region=2 $v_{sg} \uparrow: V_{max} - V_{cm} \rightarrow$ $V_{max} - V_{min} \rightarrow 50mV$ $v_{sd} \downarrow: V_{max} - V_{min} \rightarrow$ $V_{max} - V_{min} \rightarrow 50mV$ $I = 1/2 \times \beta (v_{sg} - V_T)^{\alpha} \uparrow$ $T \approx 0.07\beta$ | region=0 | region=0 $v_{gs} \downarrow: V_{max} - V_{min} \rightarrow$ $V_{max} - V_{min} \rightarrow 50mV$ $v_{ds} \uparrow: V_{max} - V_{min} \rightarrow$ $V_{min} - V_{cm} \rightarrow 50mV$ $I = \beta (v_{gs} - V_T)^{\alpha/2} v_{ds} \uparrow$ $T \approx 0.01\beta$ |
| C     | region=2 $v_{sg} \uparrow: V_{max} - V_{min} \rightarrow$ $50mV$ $v_{sd} \downarrow: V_{max} - V_{min} \rightarrow$ $50mV$ $I = 1/2 \times \beta (v_{sg} - V_T)^{\alpha} \uparrow$ $T \approx 0.07\beta$ | region=2 $v_{gs} \uparrow: V_{max} - V_{min} \rightarrow$ $V_{max} - V_{min} \rightarrow 50mV$ $v_{ds} \uparrow: V_{max} - V_{min} \rightarrow$ $V_{min} - V_{cm} \rightarrow 50mV$ $I = 1/2 \times \beta (v_{sg} - V_T)^{\alpha} \uparrow$ $T \approx 0.02\beta$ |
| D     | region=1 $v_{sg} \uparrow: V_{min} - V_{cm} \rightarrow$ $50mV$ $v_{sd} \downarrow: V_{min} - V_{cm} \rightarrow$ $50mV$ $I = \beta (v_{sg} - V_T)^{\alpha/2} v_{sd} \uparrow$ $T \approx 0.02\beta$ | region=1 $v_{gs} \uparrow: V_{max} - V_{min} \rightarrow$ $V_{max} - V_{min} \rightarrow 50mV$ $v_{ds} \uparrow: V_{max} - V_{min} \rightarrow$ $V_{min} - V_{cm} \rightarrow 50mV$ $I = \beta (v_{gs} - V_T)^{\alpha/2} v_{ds} \uparrow$ $T \approx 0.02\beta$ |

Fig. 4. Simulation results of oscillation frequency of both conventional and proposed 4 stage fully differential RO, along with the theoretical prediction for the proposed structure. As expected, the proposed RO has higher frequency for the same current.

Fig. 5. Comparison of the sensitivity of four different types of CCO topology with power supply and temperature: pseudo differential, current starved single-ended, conventional and proposed current starved differential CCO. The proposed and conventional current starved differential designs have similar sensitivity that is much less than pseudo-differential or current starved single ended architectures.

the robustness of the proposed oscillator in comparison to the conventional one through simulations. The simulation results of line sensitivity (%/V) and temperature sensitivity (%/T) of four types of RO-CCO is shown in Fig. 5. As expected, the characteristics of differential current starved structures, both proposed and conventional, are better (≈18% for line sensitivity and <0.014% for temperature sensitivity) than non current starved pseudo differential RO (≈139% for line sensitivity and ≈0.14% for temperature sensitivity). For current starved structures, differential structures are better than single ended (≈61% for line sensitivity and ≈0.06% for temperature sensitivity) as expected. It can be seen that the line sensitivity and temperature sensitivity of the proposed differential structure is not degraded compared to the conventional
differential structure. The relatively high value of sensitivity to power supply is traced back to the tail current sources coming out of saturation at power supply voltages lower than 0.9 V–this can be solved by reducing the current range. Constrained to 1–1.2 V for power supply, the sensitivity is only around 1.5%.

Following [24], the variance of period jitter for a RO can be expressed as:

\[
\sigma_T^2 = \frac{KT}{f_0} \left( \frac{2}{V_{DD} - V_t} (\gamma_N + \gamma_P) + \frac{2}{V_{DD}} \right).
\]

(10)

where,

\[
f_0 \approx \frac{I}{C N V_{DD}}.
\]

(11)

\(N\) is the number of delay stage. \(\gamma_N\) and \(\gamma_P\) are technology-dependent noise factors for NMOS and PMOS respectively. Thus,

\[
\sigma_T^2 \propto \frac{C}{I^2}.
\]

(12)

In our implementation, the load capacitor and average current decrease by 25% and 13.3% respectively.

\[
\frac{\sigma_{Prop}^2}{\sigma_{Conv}^2} = \left( \frac{1 - 0.25}{1 - 0.133} \right)^2 \approx 1.
\]

(13)

So, the jitter of the proposed CCO is expected to be approximately the same as the conventional structure. This has been confirmed in simulations and measurement—we present these results in the next section.

**D. Frequency to Digital Conversion**

For usage within a neural network system, the raw frequencies of the CCO need to be often converted to a digital word. The easiest method to do this is to pass the CCO output as a clock to a counter [12]. However, this method incurs a large conversion time (\(\propto M\)) and concomitantly large conversion energy. A different approach, following [11] is used in our work as described next.

Fig. 6 shows the diagram of time to digital converter (TDC) with a four delay stage differential CCO and the sequential counters. Although the four stage differential CCO outputs eight phases totally, only half are unique with separate phase information while the rest are exactly the inverse of the unique phases and offer the same phase information. So only four phases with 45º phase shift of each other, as shown in Fig. 6(a), are utilized to generate the phase code counter (PC-CNT). Only 360º/45º = 8 codes are generated by the four stages differential CCO and hence only 3-bits are available in the PC-CNT acting as fine counter. The sequence diagrams of the four choice outputs and the corresponding complementary symmetry phase codes are illustrated in Fig. 6(b). The opposite phase of the last phase of PC-CNT is chosen to clock a Gray code counter (GC-CNT) serving as coarse counter. The number of bits of GC-CNT depends on the input current range while the number of bits in PC-CNT determines the accuracy of the converter. A Gray code counter is selected for higher reliability in neural networks with tightly packed layout. To enable wide dynamic range testing, a 12-bit GC-CNT is used in our design but the bit width can be optimized in neural network applications.

Both the phase code counter and Gray code counter possess the merits of energy efficiency and reliability since only one bit trips during state transition. Regarding the choice of number of stages in the CCO, we note that more stages of CCO structure (\(\times M\)) offers more valid output phases (\(\times M\)) and thus more bits in PC-CNT but has lower frequency and thus less bits in GC-CNT. Overall, the total number of bits is constant but more CCO stages consume more area overhead (\(\times M\)). Assuming the same input current for both cases, the tail current for CCO core is constant and hence energy per conversion due to CCO is constant. Energy dissipated in the counter is less for more
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IV. MEASUREMENT RESULTS

The prototype chip has been fabricated in a 65 nm standard CMOS technology and includes a four-stage conventional CCO and the proposed CCO with output inverter buffers and peripheral circuits. The die micrograph and major sub-blocks are shown in Fig. 7(a). The entire block is 110 × 90μm² in size. The testing board is shown in Fig. 7(b), where the configuration switches, testing points and power supply are on the front side of the testing board while an
FPGA board is hooked to the rear side. This section presents the measurement results and explains the testing condition and methodology.

The testing setup is illustrated in Fig. 8(a). The bias current of the CCO can be controlled in coarse steps using an external resistor \( R_{\text{ext}} \) on the board and in fine steps by a voltage input \( V_{DAC} \) from an on-board Digital to Analog Converter. The combination of resistor and voltage are converted into a reference current by a rail-to-rail operation amplifier based V-I converter (Fig. 8(b)) and then copied as the starved current for the CCO core by current mirrors. The range and amplitude of the current is also programmable by the configuration bit \( ISEL \). CCO cores selection is configured by \( CCO_{-SEL} \). The output of the oscillator is converted to a digital code by the coarse/fine digital quantizer as described earlier. The bit stream is serialized and sent to the FPGA for storage and analysis. The frequency of oscillation can be inferred from the digital code without having to measure a high frequency signal directly.

Note that the V-I converter is used just for convenience of testing. In an actual neural network, the input current \( I_{in} \) to the CCO will come from a synaptic array. Fig. 8(c) shows an example how the CCO can be integrated into a neural network system with resistive synapses [25]. Here the CCO is used as the \( i-th \) neuron in the \( (l+1)-th \) layer and the count output from one neuron feeds a digital—analog converter (DAC) in the next layer to create voltage inputs. Note that this is just an example implementation just to clarify that the V-I converter is not a part of the neuron.

Measured frequency transfer curves of the conventional and proposed CCOs are plotted in Fig.9(a) at different input current obtained by varying the DAC voltage over a wide range. The measured frequency of proposed CCO indeed achieves \( \approx 11\% \) improvement compared with that of the conventional one for the same current input, ranging approximately from 0 to 1.5 \( \mu A \), close to the simulation based result in Section III. Fig. 9(b) shows the measured power consumption at different oscillation frequencies. At the same oscillation frequency, the proposed CCO consumes 13\% less energy due to the less number of transistors and the corresponding capacitors. At the highest \( V_{DD} = 1.2 \) V, the energy/conversion step including V-I converter ranges from 0.56 – 0.63 \( pJ/Cycle \). For a lower \( V_{DD} = 0.7 \) V and excluding the V-I converter, the energy/conversion step ranges from 0.11 – 0.38 \( pJ/Cycle \). Equivalently, this energy efficiency can be quoted as 0.11 – 0.38 \( \mu W/MHz \). Finally, the dependence of the oscillation frequency on power supply voltage is tested. The experimentally obtained frequencies of the conventional and the proposed CCOs with different power supply \( V_{DD} \) are shown in Fig.9(c). The testing is under the condition of \( V_{DAC} = 0.2 \) V, \( R_{\text{ext}} = 0 \) \( \Omega \) and \( ISEL \) is set to low (total resistor is 1.05 \( M\Omega \) in this case). The result shows a sharp drop in frequencies for \( V_{DD} \) less than 1 V and is traced back to the reference circuit not functioning properly at these voltages resulting in a change in the starving current. However, the proposed oscillator produce higher frequencies than the conventional design for all values of \( V_{DD} \).
As mentioned before, the frequency of CCO can be tunable by both input voltage $V_{DAC}$ and the external resistor $R_{ext}$. Fig.10 shows the transfer curves, where $V_{DAC}$ sweeps from 100 mV to 1 V. First, the external resistor $R_{ext}$ is fixed to 8.95 $M\Omega$ and the configuration bit $ISEL$ is set to low, making the total resistance $R_{tot} = 10 M\Omega$. Tuning input voltage $V_{DAC}$ from 100 mV to 1 V covers the input current range from 10 nA to 100 nA, as shown in the blue line (R1). Then, the external resistor $R_{ext}$ is fixed to 650 $K\Omega$ and $ISEL$ is set to high, leading the total resistance $R_{tot} = 1 M\Omega$. Tuning input voltage $V_{DAC}$ from 100 mV to 1 V covers the input current from 100 nA to 1000 nA, as shown in the red line (R2). The testing points show the two kinds of tuning matches well and one can act as coarse tuning while another as fine tuning.

To test the jitter performance, the outputs of CCOs are connected to a time-to-digital converter (TDC) in the chip, as shown in Fig. 8 and described in the earlier section. A parallel in serial out (PISO) circuit is used to reduce the number of output pads. The 15-bit parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control. In our testing, the serial output data is captured by FPGA and then passed to PC to decode. Fig. 11 (a) and (b) display the measured period jitter performance for the conventional and proposed structure at a low and high frequency respectively. The duration of counter window is set to 50 $\mu s$ in the measurement. It can be seen that the two structures perform approximately the same with around 0.2% jitter at lower frequency and around 0.25% jitter at higher frequency.

Fig. 12 shows the relative area utilization and the simulated power breakdown. The 4-stage CCO core contributes a small area of 44 $\mu m^2$. It may be noted that although the V-I converter consumes a significant system power in our testing, this block is not an intrinsic part of our design but is there only for testing as mentioned earlier.

Table II compares characteristics and performance of various oscillators used in neuromorphic applications.

| Reference | Technology (nm) | Topology | Power Eff. ($\mu W/MHz$) | Frequency ($MHz$) |
|-----------|----------------|----------|-----------------|-----------------|
| This work | 65 | Differential, 4-stage | 0.11-0.38 | 80 |
| Lee 2018  | 2000 (SOI) | Single-ended, 3-stage | 360 | - |
| Yi 2017   | 65 | Differential, 4-stage | 0.71 | 70 |
| Yao 2017  | 350 | Single-ended, relaxation | 0.2 | 4 |
| Basu 2010 | 350 | Single-ended, relaxation | 17.4 | 100 |
| Sahoo 2019 | 65 | Single-ended | - | 1.5 |

1 Excluding V-I converter power

The proposed CCO has one of the highest energy efficiencies reported so far (except [12]). However, [12] presents a single ended design with a much lower frequency of operation. Further, compared with the other differential design in [11], the proposed work uses 25% less area.

Further, a detailed performance comparison is summarized in Table III for the recent time based ADC architectures. To compare with other ADCs, the center frequency of CCO is set to be 60 MHz in the prototype ADC. With the input analog bandwidth of 500 kHz, running at 5 MS/s, it consumes 72 $\mu W$ from 1.2 V in average with full input signal swing, out of which 40 $\mu W$ is drawn by the digital circuits and the buffer while 32 $\mu W$ is from analog (including CCO core and bias). The proposed novel CCO structure consumes less area and lower energy overhead by using less transistors. Besides, the Gray code counter and phase code counter consume less dynamic energy due to their merit of minimum change code. These lead to high energy efficiency of the time based ADC quantified by the figure of merit (FOM) calculated as:

$$FOM = \frac{P}{2\times ENOB \times 2 \times BW}$$  \hspace{1cm} (14)$$

where, $P$ is the total power consumed by the CCO-based ADC. The ADC achieves an FOM in the range of 79 – 102 fJ/conv-step for different input frequencies. Note that [35] achieves much lower FOM by using 2$^{nd}$ order
TABLE III
PERFORMANCE SUMMARY AND COMPARISON WITH STATE OF THE ART

| Reference | Technology (nm) | Architecture | Supply (V) | Power (mW) | Area (mm²) | Bandwidth (MHz) | FOM (fJ/conv.) | Application Comments |
|-----------|----------------|--------------|------------|------------|------------|-----------------|----------------|---------------------|
| This work | 65             | Novel CCO + TDC | 1.2        | 0.02       | 0.004      | 0.5            | 79¹            | silicon neuron in neuromorphic applications |
| Lee 2018  | [28]           | VCO + ΔΣ     | 0.5        | 1.3        | 0.006      | 0.011          | 175            | electrode bio-potential recordings |
| Li 2017   | [29]           | VCO + ΔΣ     | 1.2        | 1.05       | 0.13       | 0.4            | 118            | continuous-time delta-sigma modulator |
| Young 2014| [30]           | OTA + VCO    | 1.2        | 38         | 0.49       | 50             | 294            | continuous-time delta-sigma modulator |
| Talor 2013| [31]           | VCO          | 0.9        | 11.5       | 0.075      | 5.08           | 246            | digital wireless receiver, CT delta-sigma modulator |
| Kim 2014  | [32]           | delay cell + 3-D Vernier | 1.5 | 0.33 | 0.28 | 0.5 | 400 | time-of-flight (ToF) application |
| Tu 2017   | [33]           | PWM + ΔΣ     | 1.2        | 0.02       | 0.015      | 0.005          | 1643           | CMOS Image Sensor, X-ray detector |
| Jayaraj 2019 [34] | VCO + ΔΣ | 1.2 | 1 | 0.06 | 2.5 | 151 | continuous-time (CT) ADC |
| Jayaraj 2019 [35] | VCO + ΔΣ | 1 | 0.1 | 0.06 | 2.3 | 8.6 | continuous-time (CT) ADC |
| Zhong 2018| [36]           | VCO + ΔΣ     | 1.1        | 0.91       | 0.086      | 5.2            | -              | continuous-time (CT) ADC |

¹ FOM is based on simulation since V-I converter does not support high frequency input.

noise shaping loop; however, this benefit comes mostly due to reduced quantization noise and is orthogonal to the improvements in oscillator structure we report. Also, this improvement comes with a > 10X area penalty which may not be suited for neuron designs.

V. DISCUSSION

A. Neural Network Simulation

In this section, we explore potential application of the proposed CCO as a neuron in neural network (NN) implementations. The custom activation function of the proposed neuron is modelled using experimental results of the CCO (Fig. 9 and Fig. 11). The I-F transfer curve of CCO has a high sensitivity to process variations and hence the neurons on a chip are expected to have mismatch. Fig. 13 shows the mismatch of CCO through Monte Carlo (MC) simulation. As seen from the figure, the standard variation is 1.8 MHz at the mean frequency of 39.7 MHz leading to a coefficient of variation of ≈5%. The mismatch of CCO is observed by performing MC runs while sweeping input currents. The variability in the slope of this I-F curve is included in the NN simulation as shown next. Note that synaptic non-idealities are a separate issue and has to be considered for the full system as well. This is beyond the scope of this work but many strategies to handle synaptic non-idealities such as mismatch, low-precision and write non-linearity have been published [12], [37]–[40].

At first, the neural networks are trained and tested using ReLu activation function to establish a benchmark for further evaluation of proposed activation function. For hardware simulation, we adopted two strategies. In the first one, the networks are trained using ReLu activation and the custom activation function is introduced only during inference. In the second strategy, the custom activation is used both during training and inference. The simulation details are described in detail in algorithm 1.

Algorithm 1 Hardware Simulation

1: Fit a straight line for each set of readings (i-f curves) and get a distribution of slopes. Calculate mean slope $\bar{m}$.
2: Divide the curves in two regions and fit a straight line for each region. Optimum boundary between regions $B$ is determined based on minimising MSE over all curves.
3: For both the regions, obtain the slope distributions from Monte-Carlo simulations and model them using Gaussian distributions: $N_1(\mu_1, \sigma_1^2)$ and $N_2(\mu_2, \sigma_2^2)$.
4: Noise is modelled as Gaussian noise $n \sim N(\mu = 0, \sigma = \text{jitter})$.
5: Finally the custom activation function is given by: Custom Activation($x$) = ReLu($\bar{m}x$) + ReLu($m_1 x[x < B] + m_2 x[x > B]$) + ReLu($m_1 x[x < B] + m_2 x[x > B]$) × $n$, where $m_1 \sim N_1$ and $m_2 \sim N_2$.
6: For hardware simulation (inference):
   - training activation: ReLu($\bar{m}x$)
   - inference activation: Custom Activation($x$)
7: For hardware simulation (training + inference):
   - training activation: Custom Activation($x$)
   - inference activation: Custom Activation($x$)

We used three different datasets (MNIST [41], fashion MNIST [42], CIFAR-10 [43]) and two network topologies.
TABLE IV
NEURAL NETWORK SIMULATION

| Datasets | MNIST | Fashion MNIST | CIFAR-10 |
|----------|-------|---------------|----------|
| Network  |       |               |          |
| Software | 0.982 | 0.9926        | 0.8919   | 0.9174   | 0.5284 | 0.7478 |
| Hardware (inference) | 0.9812 | 0.9915 | 0.8846 | 0.9088 | 0.5014 | 0.6974 |
| Hardware (training+inference) | 0.9829 | 0.9931 | 0.8937 | 0.9135 | 0.5257 | 0.7435 |

Fig. 14. Usage of the CCO in an SNN based on SPICE simulations: (a) With leak current of 1 nA added, the CCO does not oscillate for input current less than $I_{leak}$. (b) For a step current input, the neuron only oscillates during the step input. (c) For pulse current inputs, the charge is integrated on a current mirror’s capacitor and outputs spike when the CCO reaches a desired phase.

(one ANN and one CNN) to evaluate the performance of the proposed neuron model. Since the primary aim of these simulations is to verify the viability of the CCO based neuron, instead of experimenting with different network architectures, we used the same ANN and CNN architectures for all the datasets and compared the performance of the hardware simulations with their pure software counterpart. The ANN comprises of two fully connected hidden layers with 800 and 300 neurons respectively. The CNN network architecture used can be described as: $A \times B \times C - 32:5 - m2 - 64:5 - m2 - 128:1 - m2 - fc512 - 0.5d - fc10$, where the input dimension is $A \times B \times C$, $XcY$ represents a convolution layer with $X \times Y$ size, $mZ$ represents a $Z \times Z$ 2D max-pooling layer, $Pd$ represent a dropout layer with dropout rate $P$ and $fcL$ represent a fully connected dense layer with $L$ neurons. All models are trained and tested through google colaboratory on a server with Intel Xeon CPU and NVIDIA Tesla K80 GPU. All the models are trained with categorical crossentropy loss and Adam optimizer and the testing accuracies for all the datasets and network topologies are averaged over 3 trials.

The results (mean across 3 trials) are shown in table IV. The key observations from the results are as follows: firstly, for simple datasets like MNIST, there is almost no loss of accuracy even if the custom activation function is introduced only during inference. For a relatively more complex fashion MNIST dataset, there is a small loss ($\sim 1\%$) in testing accuracy, while for more complex CIFAR10 dataset, the loss of accuracy becomes significant ($\sim 2.5 - 4\%$). Secondly, the loss in accuracy can be almost completely recovered even for complex datasets like CIFAR-10, if the custom activation is introduced during training i.e. weight learning through back-propagation is able to correct for any non-ideality resulting from the custom activation. Thirdly, in some cases, when the custom activation is introduced during training, the testing accuracies seem to surpass the software accuracy. This can be attributed to Gaussian Noise injection in the custom activation acting as noise regularization and improving overall network performance [44]. For all the datasets and both hardware simulation settings, the loss of accuracy is similar for both ANN and CNN network topologies. Since the ANN uses only two hidden layers while the CNN architecture consists of large number of layers, this observation establishes the scalability of the proposed neuron model. Finally, we evaluated in detail the variability in the performance of the classifiers caused by random variation of the custom activation function described in step 5 of algorithm 1. For MNIST classification task with ANN and CNN, we evaluated the classification accuracies over 20 trials where the slopes of the custom activation are randomly generated for each trial. The standard deviation of classification accuracy for ANN and CNN are 0.15% and 0.10% respectively. This goes to show that the performance variation introduced by the slope variability is very small and therefore, further proves the viability of the proposed neuron model.

Changes in power supply voltage and temperature are ideally common mode perturbations and affect the CCO less due to differential structure. Moreover, due to sharing of power supply, if all neurons are affected by the same factor, RELU based neural networks will not be ideally affected. However, due to variations between neurons, there will be some effect in real implementations. To capture this effect, Monte-Carlo simulations were done to find distributions of supply voltage sensitivity (temperature sensitivity is almost negligible as
shown in Section III). The resulting sensitivity distribution had a mean of \(-0.78\%\) and standard deviation of \(1.74\%\) when \(V_{dd}\) varied in the range of \(1 - 1.2\ V\). Including this as an additional perturbation for the neuron outputs during inference, the results for CIFAR-10 were re-evaluated. We observed negligible reduction in accuracy of \(<0.5\%\) confirming our hypothesis that the network is relatively robust against supply variations.

B. CCO as Spiking Neuron

The earlier sections showed the usage of the CCO as a rate encoded neuron similar to its use in [11], [12]. However, it may also be used as a spiking neuron with precisely timed output spikes as needed in spiking neural networks (SNN). While one way to use the CCO as a spiking neuron is shown in [9], we show next how some of the critical features can be included in the CCO much easily. We identify one of the phases of the CCO as the spike phase and the corresponding output of the fine counter is plotted as spike output.

First, we show in SPICE simulations that adding a leak current source [45] next to the PMOS input current mirror in Fig. 8(b) can act to suppress spurious neuron spikes at low input currents. The resulting I-F curve plotted in Fig. 14(a) shows that indeed valid neuron firing starts for input currents larger than \(I_{\text{leak}} = 1\ nA\). Next, the response of the CCO neuron to a step of magnitude \(I_{\text{in}} = 1\ \mu A\) is shown in Fig. 14(b). As expected, the neuron fires spikes only when the step is applied. Lastly, to see how to integrate such a neuron in a network, we show the response of the CCO neuron to spike inputs that may come from other neurons in the network. Plotted in Fig. 14(c), it shows that for input synaptic current pulses of magnitude 100 \(nA\), the neuron integrates the charge on the PMOS current mirror and produces an output spike for every 4 input spikes.

C. Startup Circuit

In Section III, we proposed the novel structure of CCO and explained the necessity of a start-up circuit. A robust oscillation can be ensured by a start-up circuit with only a PMOS transistor or a NMOS transistor or both. As shown in Fig. 15 (a), a start-up circuit is equipped at the differential output nodes to eliminate the uncertainty state. The start-up circuit would be a single PMOS acting as a pull-up device to eliminate the uncertainty of \(outn\), as shown in Fig. 15 (b), or a single NMOS acting as a pull-down device to eliminate the uncertainty of \(outp\), as shown in Fig. 15 (c), or both a PMOS and a NMOS to eliminate the uncertainty of both the differential outputs, as shown in Fig. 15 (d).

VI. Conclusion

In this paper, an energy- and area-efficient full differential CMOS current controlled ring oscillator (CCO) is presented as a suitable and compact structure in neurocomputing applications. The CCO achieves higher frequency while consuming lower area and lower energy due to less transistors being utilized compared with the conventional structure. By eliminating the unnecessary transistors, the proposed structure is composed of a simplest dynamic positive feedback latch and differential pairs, saving \(\approx 25\%\) in size. The CCO can be
tuned by both input voltage and external variable resistor. The measurement results show our work achieves 11% frequency improvement and 13% energy-efficient without degrading the jitter and phase noise characteristics. Simulations of both ANN and CNN with the proposed CCO characteristics as the neuron transfer curve show no degradation in accuracy if the CCO nonlinearity is included in training.

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Xueyong Zhang (Graduate Student Member, IEEE) received the B.S. degree in applied physics from Nantong University, China, in 2011, the M.S. degree in electronics and telecommunications from the University of Rennes 1, France, and the M.E. degree in microelectronics and solid-state electronics from Southeast University, China, in 2013 and 2014, respectively. He is currently pursuing the Ph.D. degree with Nanyang Technological University, Singapore. From 2014 to 2016, he was an IC Design Engineer with Silergy Corporation, where he was involved in power management unit design. He is also a Research Associate with Nanyang Technological University, Singapore. His research interests include low power analog IC, neuromorphic VLSI, and in-memory computing design.

Jyotibdha Acharya (Member, IEEE) received the B.E. degree in electronics and telecommunication engineering from Jadavpur University, India, in 2014, and the Ph.D. degree from Nanyang Technological University, Singapore, in 2020. He is currently a Scientist with the Institute for Infocomm Research, Agency for Science, Technology and Research (A*STAR), Singapore. His research interests include deep learning, neuromorphic algorithms, and biomedical applications.

Arindam Basu (Senior Member, IEEE) received the B.Tech. and M.Tech. degrees in electronics and electrical communication engineering from IIT Kharagpur, Kharagpur, India, in 2005, and the M.S. degree in mathematics and the Ph.D. degree in electrical engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2009 and 2010, respectively. He joined Nanyang Technological University, Singapore, in 2010, where he is currently a tenured Associate Professor. His research interests include bio-inspired neuromorphic circuits, non-linear dynamics in neural systems, low-power analog IC design, and programmable circuits and devices. Dr. Basu received the Best Student Paper Award from the Ultrasonics Symposium in 2006, the Best Live Demonstration at ISCAS 2010, and the Finalist in the Best Student Paper Contest at ISCAS 2008. He also received the MIT Technology Reviews inaugural TR35@Singapore Award in 2012, for being among the top 12 innovators under the age of 35 in Southeast Asia, Australia, and New Zealand. He received the Prime Minister of India Gold Medal from IIT Kharagpur in 2005. He was a Guest Editor for two special issues in the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS for selected articles from ISCAS 2015 and BioCAS 2015. He is serving as a Corresponding Guest Editor for the IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS Special Issue on “Low-Power, Adaptive Neuromorphic Systems: Devices, Circuit, Architectures and Algorithms.” He is currently an Associate Editor of the IEEE SENSORS JOURNAL, the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, and the Frontiers in Neuroscience. He was a Distinguished Lecturer of the IEEE Circuits and Systems Society from 2016 to 2017.