Dataflow Aware Mapping of Convolutional Neural Networks Onto Many-Core Platforms With Network-on-Chip Interconnect

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Abstract—Machine intelligence, especially using convolutional neural networks (CNNs), has become a large area of research over the past years. Increasingly sophisticated hardware accelerators are proposed that exploit e.g. the sparsity in computations and make use of reduced precision arithmetic to scale down the energy consumption. However, future platforms require more than just energy efficiency: Scalability is becoming an increasingly important factor. The required effort for physical implementation grows with the size of the accelerator making it more difficult to meet target constraints. Using many-core platforms consisting of several homogeneous cores can alleviate the aforementioned limitations with regard to physical implementation at the expense of an increased dataflow mapping effort. While the dataflow in CNNs is deterministic and can therefore be optimized offline, the problem of finding a suitable scheme that minimizes both runtime and off-chip memory accesses is a challenging task which becomes even more complex if an interconnect system is involved. This work presents an automated mapping strategy starting at the single-core level with different optimization targets for minimal runtime and minimal off-chip memory accesses. The strategy is then extended towards a suitable many-core mapping scheme and evaluated using a scalable system-level simulation with a network-on-chip interconnect. Design space exploration is performed by mapping the well-known CNNs AlexNet and VGG-16 to platforms of different core counts and computational power per core in order to investigate the trade-offs. Our mapping strategy and system setup is scaled starting from the single core level up to 128 cores, thereby showing the limits of the selected approach.

Index Terms—Convolutional neural network (CNN), network on chip (NoC), deep learning, application-specific instruction set processor (ASIP), dataflow optimization

I. INTRODUCTION

Convolutional neural networks (CNNs) are nowadays widely used for applications such as face recognition and object detection. While smaller networks like MobileNet[1] and SqueezeNet[2] can be efficiently processed using small dedicated accelerators or even ARM based general-purpose CPUs[3], larger networks require much more powerful dedicated hardware. In data-center applications, often GPUs are the method of choice due to their easy programmability and massive performance which, however, is paid for by their large power consumption compared to application-specific accelerators[4]. For future platforms, it is therefore desirable to have scalable performance with reasonable power consumption so that the accelerator can be tailored towards a certain set of problems.

Using a single large core yields high throughput and energy efficiency if designed for networks with specific dimensions. However, having a single very large accelerator makes it more difficult to find suitable mappings for CNNs with dimensionalities differing significantly from the initial design goals. As a result, the arithmetic units are often under-utilized as shown in[5]. This issue can be circumvented by having many smaller cores that allow a more fine-grained mapping of the available data-slices. These cores should provide sufficient flexibility, e.g. by being programmable, in order to allow for multiple processing schemes to be mapped onto them. One possible way of achieving this is to use application-specific instruction-set processors (ASIPs) as shown in[6].

The choice of arithmetic (e.g. limited precision fixed-point, binary/log quantized etc.) has a large impact on the power consumption of a system, so does the dataflow scheme. In this work, the term dataflow is used to describe both the temporal as well as the spatial distribution of data-packets, i.e. filter weights and feature maps of convolutional kernels, in the overall system. By maximizing the spatial correlation of data and minimizing the temporal dependencies, it is possible to reduce the number of off-chip accesses and, therefore, reduce the energy required for data movement. In the context of a many-core system it is, however, not sufficient to only optimize the dataflow for a single core but the optimization must be done for the entire system.

For many-core systems, a very important aspect is the choice of interconnect: While traditional crossbar based interconnects imply a moderate implementation complexity, they quickly become a bottleneck in terms of system scalability. Using a robust and well-proven network-on-chip (NoC), on the other hand, results in a larger initial implementation complexity that is rewarded by a much easier system scalability. For these reasons, we focus on configurable many-core systems that use a DRAM-centric NoC with a mesh topology as an interconnect.

While the dataflow of a single core can be accurately classified and evaluated based on its specific loop-order, loop-tiling and related loop-unrolling parameters[7], [8], a sophisticated system-level simulation is required to do so for many-core systems due to the interconnect. The main reason for this is that congestion phenomena in the NoC are not easily predictable and must therefore be simulated. This is because
the NoC requests issued by all the cores affect each other, i.e. causing stalls within some cores while waiting for data. The main contributions of this work can be summarized as follows:

- Based on previous work from [7], we provide a mathematical formulation for finding the optimal single-core mapping scheme for an existing programmable CNN accelerator with user-definable optimization targets: minimal runtime or minimal off-chip accesses.
- The single-core mapping problem is extended towards the many-core case and a heuristic for finding automatic mappings is described.
- Case studies for mappings of the well-known CNNs AlexNet and VGG-16 are presented and quantitatively evaluated using system-level simulations of a platform comprised of multiple accelerators and a network-on-chip.

The remainder of this work is structured as follows: In Section II a brief overview of existing CNN accelerators and dataflow optimization schemes is given. Next, the simulation setup is elaborated in Section III whereas the implementation details of the different system components are presented in Section III-A. A solution for the single-core mapping problem is mathematically formulated in Section IV and simulation results are depicted in Section V. Our proposed mapping heuristic for extension towards the many-core case is detailed in Section VI. Comprehensive simulation results for mappings onto different platform configurations are then presented in Section VII. Section VIII concludes this work with some final remarks.

II. BACKGROUND

A. Hardware Acceleration of CNNs

Starting with the widespread use of CNNs in the early 2010’s, there have been a number of hardware accelerators presented in both the research community as well as the industry. In general, the different types of accelerators can be grouped into one of the following categories: GPUs, FPGAs, ASICs and application-specific instruction-set processors (ASIPs), in which the latter two groups vary in terms of their data processing scheme. Some well-known examples of dedicated accelerators are Snowflake [9] (FPGA), Escher [10] (FPGA), Origami [4] (ASIC), Eyeriss [11] (ASIC), Envision [12] (ASIP) and ConvAix [6] (ASIP). While they differ in terms of their specific processing scheme, they are all optimized towards the same overall goal: Keep data as local as possible to reduce off-chip transfers and maximize processing intensity, thereby maximizing the utilization of their arithmetic units. A key difference in the presented architectures is their degree of flexibility, ranging from fixed dataflow to runtime configurable dataflow. Of course, having a more flexible processing scheme always comes at some cost in terms of area (additional control units) and energy (setting up the processing scheme and multiplexing the data), but it also gives designers more degrees of freedom. This freedom can then be exploited when optimizing the mapping which is especially important for many-core platforms. For this reason, we propose the use of a flexible dataflow accelerator, e.g. an ASIP, and incorporate a suitable system-level model of such a core into our overall simulation setup as described in Section III.

B. Convolutional Layer

Today's CNNs consist of a number of different layers, amongst them convolutional layers, pooling layers and activation layers. Due to the fact that the largest computational demand is generated by the regular convolutional layers, we focus our investigations on them. The convolutional operation can be described according to (1) as follows:

\[ O(c_o, y_o, x_o) = B(c_o) + \sum_{c_i=0}^{N_{of}} \sum_{k_y=0}^{N_k} \sum_{k_x=0}^{N_k} W(c_o, c_i, k_y, k_x) \cdot I(c_i, y_o \cdot s, x_o \cdot s) \]

whereby \( O \) depicts the entirety of all output feature maps (ofmaps) indexed by their channel \( c_o \) and position \( (y_o, x_o) \) within the ofmap, while \( I \) represents the set of all input feature maps (ifmaps) with the same indexing scheme as the ofmaps. The respective biases for each output channel are depicted by \( B \), with \( W \) being the weights associated with the ofmap channel \( c_o \), ifmap channel \( c_i \) and filter kernel position \((k_y, k_x)\). Lastly, \( s \) represents the stride of the convolution. The limits of the sums represent the total number of ifmaps \( N_{if} \) as well as the filter kernel’s height \( N_{k_y} \) and width \( N_{k_x} \). Since the result of (1) only calculates one single output pixel for one output channel, an even greater number of multiply-accumulate (MAC) operations is required to calculate all ofmaps completely. The actual implementation of this can be represented by many nested for-loops as shown in Algorithm 1.

\[
\begin{align*}
\text{Algorithm 1: Nested for-loops of a convolutional layer.} \\
\text{Input: ifmaps } I, \text{ filter weights } W, \text{ biases } B, \text{ stride } s \\
\text{Result: ofmaps } O \\
1 & \text{ for } (c_o = 0; \ c_o < N_{of}; \ c_o++) \\
2 & \quad \text{ for } (y_o = 0; \ y_o < N_{oy}; \ y_o++) \\
3 & \quad \quad \text{ for } (x_o = 0; \ x_o < N_{ox}; \ x_o++) \\
4 & \quad \quad \quad O(c_o, y_o, x_o) = B(c_o) \\
5 & \quad \quad \text{ for } (c_i = 0; \ c_i < N_{if}; \ c_i++) \\
6 & \quad \quad \quad \text{ for } (k_y = 0; \ k_y < N_{k_y}; \ k_y++) \\
7 & \quad \quad \quad \quad \text{ for } (k_x = 0; \ k_x < N_{k_x}; \ k_x++) \\
8 & \quad \quad \quad \quad \quad O(c_o, y_o, x_o) = + W(c_o, c_i, k_y, k_x) \cdot I(c_i, y_o \cdot s, x_o \cdot s)
\end{align*}
\]

C. Dataflow Optimization

Related work on the topic of dataflow optimization can be split twofold: First into work related to the topic of mapping tasks onto multi-many-core systems in general and second into techniques focusing on the optimal slicing and tiling of CNNs on the single accelerator level.

For the first topic, a comprehensive overview is presented in [13] where the authors introduce a taxonomy that allows...
TABLE I: Loop parameters for convolutional layers as proposed in [7].

| Filter kernels | Dimension | Tiling | Unrolling |
|----------------|-----------|--------|-----------|
| Height         | N_{ky}    | T_{ky} | P_{ky}    |
| Width          | N_{kx}    | T_{kx} | P_{kx}    |

| IFMaps         | Dimension | Tiling | Unrolling |
|----------------|-----------|--------|-----------|
| Height         | N_{iy}    | T_{iy} | P_{iy}    |
| Width          | N_{ix}    | T_{ix} | P_{ix}    |
| Channels       | N_{lf}    | T_{lf} | P_{lf}    |

| OFMaps         | Dimension | Tiling | Unrolling |
|----------------|-----------|--------|-----------|
| Height         | N_{oy}    | T_{oy} | P_{oy}    |
| Width          | N_{ox}    | T_{ox} | P_{ox}    |
| Channels       | N_{of}    | T_{of} | P_{of}    |

The main focus of this work is the optimization of the tiling parameters as they are runtime configurable and largely determine the dataflow. It should be noted that the term mapping in this work refers to a concrete set of aforementioned parameters with some additional slicing parameters which are related to the many-core case as introduced later. Since a detailed evaluation of all possible different loop orders is not possible within the scope of this work, we focus on the one presented in Algorithm I with some modifications as described in Section VI to cope with the many-core mapping.

III. Simulation Setup

To investigate the fitness of a CNN mapping in terms of runtime and communication cost, a simulation is required that is capable of accurately modeling both the single-core transactions as well as the actual communication via an interconnect network. While evaluation of a single-core mapping is possible based on analytical considerations only as shown in Section IV, the many-core case requires to account for the communication overhead induced by the NoC, i.e. network congestion caused e.g. by limitations in data buffers. The most accurate results for such an analysis could be obtained by using a full RTL-level simulation of the NoC and the accelerator cores, however this would result in an unreasonably high runtime. We therefore use a parameterizable system-level simulation in which different components of the system are implemented using approximately-timed transaction-level modeling (TLM) techniques as described in SystemC TLM [15]. Since the focus of this work is the investigation of the dataflow, each processing core is modeled in an abstract fashion: An inner process is defined that imitates the dataflow of the actual core in the way an external observer would see it. This is done by traversing the loop structure as previously described without actually performing any computations. However, the formation of data-packets (both send- and receive-packets) is carried out accurately and these packets are injected into the NoC at the corresponding times. Using a cycle-accurate instruction-set simulator of the processing core, we verified the correctness of the generated transactions. All remaining components, e.g. the NoC router, are modeled in a cycle-accurate fashion in order to accurately reflect any congestion phenomena that might occur during execution. Furthermore, to allow realistic modeling of a complex system, the simulation supports two clock domains, one for the NoC running at a higher frequency and one for the processing cores. Also, sophisticated monitoring and tracing facilities are included, thereby allowing quantitative evaluation of e.g. the number of data-packets routed over a certain router, the number of SRAM and DRAM memory accesses performed, the count of MAC operations executed per core and the average port buffer stalling times in the NoC.

A. System Overview

As mentioned before, a 2D mesh-style NoC that uses a credit-based flow control with the XY routing scheme was selected as system interconnect. Our NoC implementation is based on the work presented in [16] with some adaptations made.
especially to the direct memory network interface (DMNI) \cite{17} which is responsible for managing the data flow between the processing cores and the NoC. One possible configuration of the interconnect is shown in Fig. 1. Each router has 4 ports for each direction and an additional local port connected to the processing element.

In the following sections, different mesh- and processing core sizes are investigated. However, since the base components always stay the same, they are briefly introduced here. An exhaustive investigation of different NoC parameters such as the flit width, packet length, port buffer sizes and the positioning of the DRAM interface were conducted for this work. Based on this investigation, we use a flit width of 64 bit and a packet length of 40 flits per packet. The import buffer size of the router is set to 16 flits with the DRAM interface placed in the center of the mesh. If the mesh-size is increased beyond the 3x3 configuration depicted in Fig. 1, the DRAM block is always re-centered and the master core remains at position (0, 0) (top left). The additional positions within the mesh-grid are then filled with processing cores. Furthermore, the system uses two clock domains, one for the processing cores that runs at 500 MHz and one for the NoC that runs at a higher frequency of 1 GHz. According to \cite{18}, this is a reasonable choice for implementing a NoC in a modern CMOS technology.

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{fig1.png}
\caption{Example architecture of a 3x3 NoC with 7 processing cores, 1 master core and a DRAM interface block.}
\end{figure}

### C. Network-on-Chip Components

The relevant components of the NoC used in this work are the network router, the direct memory access network interface (DMANI), the DRAM interface handling data accesses to the external DRAM memory and the master core that schedules computations onto the processing cores described in Section III-B. Our implementation is closely based on the work of the HERMES infrastructure \cite{16} with some adoptions as described later on. Each packet within the NoC includes a flit containing the payload size, a header flit with a destination and - in contrast to HERMES - also a source address which is used by the DRAM interface as the destination for sending back data fetched due to a DRAM load request. More information on the separate components is given below.

**DMANI:** The DMANI used in this work is an extension of the DMNI introduced in \cite{17} whose main task is to offload the NoC packet-handling from the processing core so that said core can focus on performing computations. While the original DMNI required the accelerator to set up every NoC packet, containing information such as the target address and payload size, our DMANI does this on its own. It is used on top of the already existing direct memory access (DMA) controller contained within the core which is responsible for keeping tabs on outstanding read and write transactions. Whenever the core issues a new transaction, it is handed over to the DMANI which then determines the number of required packets and returns a request ID to the DMA. All requests handed to the DMANI are processed in a FIFO fashion. To further reduce the overhead for the processing core, the DMANI has direct access to the core’s SRAM memory via the core’s memory interface as shown in Fig. 2a. So, in contrast to the original DMNI, no interrupt routine is required for the DMANI to write or read data to/from the SRAM. Instead, whenever a request is handed to the DMA of the core, it is ensured in software that a sufficient large space within the SRAM is reserved. Access to the SRAM is arbitrated via the core’s own memory interface which leaves the possibility of in-accessibility during an ongoing transaction. To reduce the effects of such conflicts, the

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In order for the mapper to generate the best possible results, it is desirable to have a processing core with the highest possible flexibility with regards to the dataflow. We therefore decided to use an application-specific instruction-set processor (ASIP) that is very similar to the one presented in \cite{6}. The processor uses very long instruction words (VLIW) with 8 slots in parallel and a RISC-like instruction set architecture (ISA) that also incorporates some more complex vector instructions specifically targeted at CNNs.

The total number of parallel MAC operations that can be scheduled in one cycle depends on the design-time config-
DMANI has a receive buffer for packets being received from the NoC (as response to an earlier issued DRAM read request) and a write-buffer for pre-fetching data in case of a write to the NoC. Data contained within a service packet is used to configure the processing cores at the beginning.

**Router:** For any NoC, the router is one of the main components that enables communication between the different processing entities. As mentioned before, our router design is based on the original HERMES router presented in [16] which has four bi-directional ports for connecting to other routers (North, East, South, West) and a local port that is connected to its processing core as depicted in Fig. 2(b). The router consists of the following sub-components: crossbar, arbiter, routing module and individual port buffers. Each individual port buffer is responsible for requesting arbitration based on its stored requests. Arbitration is then handled according to a prioritization scheme that is as follows: East, West, North, South. Afterwards, the list is shifted in a cyclical fashion so that no starvation of requests occurs. A new packet is routed via the routing module by determining its destination address based on the XY routing protocol and the connection between the ports is established using the crossbar network. In total, this process, starting at the port buffers up to when the crossbar connection is established, takes 4 clock cycles.

**DRAM interface:** To allow access to an external DRAM memory, one of the grid-spaces within the NoC mesh is reserved for a DRAM interface that receives both read- and write-requests from the entire NoC and stores them in an internal request buffer that can save exactly one request per processing element. The interface preferably serves write-requests from the entire NoC and stores them in an internal request buffer that can save exactly one request per processing element. Each individual port buffer is responsible for requesting arbitration based on its stored requests. Arbitration is then handled according to a prioritization scheme that is as follows: East, West, North, South. Afterwards, the list is shifted in a cyclical fashion so that no starvation of requests occurs. A new packet is routed via the routing module by determining its destination address based on the XY routing protocol and the connection between the ports is established using the crossbar network. In total, this process, starting at the port buffers up to when the crossbar connection is established, takes 4 clock cycles.

**Master core:** The processing cores must be set up according to the mapping described in Section VII. In this work, a master-slave concept is employed in which a master core, that could be a RISC-like microprocessor, assigns the configurations to the different cores via a service message using the already introduced NoC packet structure. Since the actual configuration is determined offline, the master core only has to send these pre-calculated configuration packets and is, therefore, modeled as a simple state machine.

To summarize, the main system parameters used in this work are depicted in Table II.

### D. Energy Modelling

Since power and energy consumption are important metrics to determine the fitness of a mapping, we use a macro-modeling approach that estimates energy consumption at a high level. As mentioned before, relevant key figures with regards to energy consumption such as SRAM/DRAM load/store counts, number of MACs etc. are already traced in our simulation. These figures are used to estimate the overall energy consumption for the processing cores and DRAM according to (2) and (3) as follows:

\[
E_{\text{core}} = E_{\text{idle}} \cdot N_{\text{cycle}} + E_{\text{mac}} \cdot N_{\text{mac}} + E_{\text{sr RAM,ld}} \cdot N_{\text{sr RAM,ld}} + E_{\text{sr AM, st}} \cdot N_{\text{sr AM, st}}
\]

\[
E_{\text{dram}} = E_{\text{dram,ld}} \cdot N_{\text{dram,ld}} + E_{\text{dram, st}} \cdot N_{\text{dram, st}}
\]

where \(E_x\) represents the energy value associated with a single event of type \(x\) and \(N_x\) represents the event-count during the whole simulation time. The energy values for the processing core were extracted from time-annotated post-layout simulation of a design similar to the one presented in [6]. More details on the processing core are shown in Section III-B. Because these energy values were obtained using statistical methods, they already contain the energy required for e.g. program control of the processor (included in the idle energy) and register file accesses in case of MAC and memory operations. For DRAM memory accesses, we use an energy of 21 pJ/Bit as reported by [19] for LPDDR3 memory. For estimating the NoC’s energy consumption, we used the model presented in [20] which associates energies with the most energy intensive events in NoC routers: Routing a packet (\(E_{\text{route}}\)), arbitrating a request (\(E_{\text{arb}}\)), setting up the crossbar (\(E_{\text{crossbar}}\)), switching of the crossbar (\(E_{\text{crossbar, switch}}\)), buffering an incoming packet (\(E_{\text{buffer}}\)) and leakage (\(E_{\text{leak}}\)). The energy values used in this work are summarized in Table III. Since the original values presented in [20] were extracted from a 90 nm CMOS technology which is different from the TSMC 28 nm technology used for the core, all values were scaled to 28 nm according to \(E_{\text{new}} = E_{\text{old}} \cdot \left(\frac{V_{\text{new}}}{V_{\text{old}}}\right)^2 \cdot \frac{N_{\text{new}}}{N_{\text{old}}} \) with \(N\) being the gate pitch and \(V\) being the supply voltage.

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**TABLE II: System parameter overview.**

| Parameter                        | Value   |
|----------------------------------|---------|
| Max. packet length               | 40 flits|
| Flit width (\(W_{\text{flit}}\)) | 64 bit  |
| NoC clock frequency (\(f_{\text{noc}}\)) | 1 GHz   |
| Core clock frequency (\(f_{\text{core}}\)) | 500 MHz |
| Router input buffer size         | 16 flits|
| DMANI buffer size                | 64 words|
| DRAM bandwidth (\(BW_{\text{dram}}\)) | 64 \(\frac{\text{bit}}{\text{cycle}}\) |
IV. SINGLE-CORE DATAFLOW MAPPING

In order to find a suitable many-core mapping scheme, we use a bottom-up flow in which the single-core mapping, i.e. the determination of suitable tiling factors adhering to the taxonomy in Table I, is calculated first. The communication effects of the NoC are not considered in this step, thereby making it possible to use the high-level dataflow description from Algorithm 1 and formulate the mapping problem as a constrained mixed integer non-linear problem (MINLP). We introduce two different optimization targets: minimum overall computing time and minimum off-chip memory accesses. In the following, a derivation for the aforementioned cost-functions is given which then allows us to find optimal single-core tiling parameters using a regular MINLP solver.

Using knowledge of the actual software implementation of the convolutional layer as presented in Section II-B on our programmable ASIC, the nested loop structure with tiling can be elaborated as shown in Algorithm 2. Note that for brevity, the unrolled for-loops according to the selected \( P_{ox} \) and \( P_{of} \) values are not shown. For this work, we selected the following tiling dimensions as this made the most sense given current CNN topologies and the given hardware: tiling amongst the ofmap & ifmap channels (\( T_{of}' \), \( T_{if}' \)) and the ifmap width (\( T_{ix}' \)) which of course results in tiling along the ofmap width \( T_{ox}' = (T_{ix}' - N_{kx})/s + 1 \) (padding is already included in the ifmap width \( T_{ix}' \)). Furthermore, for examination of the single-core case, we use dashed values for the tile-size \( T_{x}' \), tile-count \( S_{x}' \) and dimension \( N_{x}' \) \((x \in \{of, if, ox, ix\})\) values in order to differentiate these single-core optimization parameters from the later to be introduced many-core optimization parameters \( T_{x} \) and \( S_{x} \). The numbers of resulting tiles per dimension as denoted by \( S_{x}' \) are calculated according to

\[
S_{of}' = \lceil N_{of}' / T_{of}' \rceil \\
S_{if}' = \lceil N_{if}' / T_{if}' \rceil \\
S_{ox}' = \lceil N_{ox}' / T_{ox}' \rceil.
\]

By annotating processing-cycle costs, e.g. for data prefetching and computations as well as data transfer-costs inferred by off-chip accesses, an overall cost for a tiling can be determined. As depicted in Algorithm 2, each step in the loop can be associated with a certain action, e.g. the DMA loading filters (line 10) or the calculation of a certain number of MAC operations (line 21). We subdivide these loops into an inner part that does not unconditionally depend on any off-chip accesses (marked in blue) and an outer part that directly relies on them (marked in red). Based on this information, we first derive the total number of off-chip accesses \( N_{dram} = N_{dram_{init}} + N_{dram_{par}} \). It is hereby important to differentiate between DMA requests that can be handled in parallel to the computations (line 10 and 23), denoted by \( N_{dram_{par}} \), and those that must be waited for (line 3, 4, 6 and 7), denoted by \( N_{dram_{init}} \).

\[
N_{dram_{init}} = N_{of}' \cdot N_{kx} \cdot N_{ky} \cdot N_{if} \quad \text{(filters)} \\
+ N_{of}' \quad \text{(biases)} \\
+ S_{if}' \cdot N_{ix}' \cdot N_{ky} \cdot N_{if} \quad \text{(initial ifmaps)} \\
+ (S_{if}' - 1) \cdot N_{ox}' \cdot N_{of}' \quad \text{(initial psums)} \quad (7)
\]

\[
N_{dram_{par}} = S_{if}' \cdot N_{ox}' \cdot N_{oy} \cdot N_{of}' \quad \text{(ofmap/psum store)} \\
+ S_{of}' \cdot N_{ix}' \cdot (N_{iy} - N_{if}) \cdot N_{if} \quad \text{(next ifmaps)} \\
+ (S_{if}' - 1) \cdot N_{ox}' \cdot (N_{oy} - 1) \cdot N_{of}' \quad \text{(next psums)} \quad (8)
\]

The required pure computational cycles within the inner loops (marked in blue) can be computed as follows:

\[
C_{comp} = (C_{mac} + C_{sram}) \cdot N_{oy} \quad (9)
\]

\[
C_{mac} = (C_{pfetch} + N_{kx}) \cdot T_{if}' \cdot N_{ky} \cdot T_{ox}' / P_{ox} \cdot T_{of}' / P_{of} \quad (10)
\]

\[
C_{pfetch} = \left[ \text{Stride} + 1 \right] / 2 - 1 \quad (11)
\]

\[
C_{sram} = 2 \cdot T_{ox}' \cdot T_{if}' \cdot P_{ox} \cdot P_{of} / \text{BW}_{sram} \quad (12)
\]
The prefetch cycle count \( C_{\text{fetch}} \) in [11] is specific to the processing core used in this work. The term \( \text{BW}_{\text{sram}} \) represents the bandwidth in words per cycle that the internal SRAM offers and is equal to \( 2 \cdot P_{\text{ox}} \). Since the on-chip memory is a banked dual-port memory with bank count equal to \( P_{\text{ox}} \). As mentioned before, certain DMA requests run in parallel to the computations, so to allow accurate calculation of the processing cycles for the inner loops, the estimated cycle count \( C_{\text{dram,par}} \) for these accesses must be calculated as well:

\[
C_{\text{dram,par}} = \frac{N_{\text{dram,par}}}{\text{BW}_{\text{dram}}} \quad (13)
\]

in which the term \( \text{BW}_{\text{dram}} \) represents the bandwidth in words per cycle that the DRAM can provide. In this work, aforementioned bandwidth is set to the NoC flit width per cycle divided by the wordwidth and multiplied with the clock ratio between the NoC and the core:

\[
\text{BW}_{\text{dram}} = 64 \, \frac{\text{bit}}{\text{cycle}} / 16 \, \frac{\text{bit}}{\text{word}} \cdot \frac{1 \, \text{GHz}}{500 \, \text{MHz}} = 8 \, \frac{\text{word}}{\text{cycle}} \quad (14)
\]

The cycle count for the outer loops \( C_{\text{outer,loop}} \) depends solely on the time required to finish the initial DRAM accesses \( N_{\text{dram,init}} \):

\[
C_{\text{outer,loop}} = \frac{N_{\text{dram,init}}}{\text{BW}_{\text{dram}}} \quad (15)
\]

Together with the previously calculated outer loop cycle count \( C_{\text{outer,loop}} \), the total cycle count \( C_{\text{total}} \) amounts to:

\[
C_{\text{total}} = C_{\text{outer,loop}} + C_{\text{inner,loop}} \quad (18)
\]

Last but not least, the allocated SRAM memory that depends on the tiling parameters must be constrained since the individual processing cores only have limited on-chip memory available:

\[
N_{\text{sram,alloc}} = \underbrace{\frac{T'_{\text{of}}}{\text{biases}}} + \underbrace{\frac{T'_{\text{of}} \cdot N_{\text{ky}} \cdot T'_{\text{if}}}{\text{filters}}} + \underbrace{\frac{T'_{\text{of}} \cdot (N_{\text{ky}} + \text{stride}) \cdot T'_{\text{ix}}}{\text{ifmaps}}} + \underbrace{3 \cdot T'_{\text{ox}} \cdot T'_{\text{of}}}{\text{ofmaps}} \quad (19)
\]

\[
N_{\text{sram,alloc}} \leq D_{\text{sram}} = P_{\text{ox}} \cdot 8 \, \text{KByte} = P_{\text{ox}} \cdot 4096 \, \text{word} \quad (20)
\]

As can be seen in [19], there are always 3 ofmap rows allocated because we use a triple-buffering scheme: One allocated row is used for pre-fetching the next partial sums (line [10] in Algorithm [2]), one is used for calculating the current ofmap row and the third is used as write-back buffer (needed in line [23]).

Depending on the optimization target, it is now possible to find tiling parameters either minimizing the computational cycles (hereafter referred to as \textit{min-comp}) or the total number of DRAM accesses (referred to as \textit{min-dram}). The final optimization targets are shown in (21) and (22).

\[
\min_{T'_{\text{af}} T'_{\text{if}} T'_{\text{ox}}} C_{\text{total}} \quad \text{(min-comp)} \quad (21)
\]

\[
\min_{T'_{\text{af}} T'_{\text{if}} T'_{\text{ox}}} N_{\text{dram,init}} + N_{\text{dram,par}} \quad \text{(min-dram)} \quad (22)
\]
For brevity, the previously introduced constraints for the minimization targets are not restated here but must be added to the problem formulation.

V. SINGLE-CORE MAPPING EVALUATION

The previously introduced single-core mapping algorithm is used to map two well known CNNs, VGG-16 [21] and AlexNet [22], onto a 3x1 system configuration with just one processing core, a master core and a DRAM interface block. Using our system-level simulation, the runtime, number of DRAM accesses as well as the energy consumption are obtained and the results are presented in Fig. 5. As can be seen, the min-comp target always achieves faster runtime compared to the min-dram target, however, this is achieved at the expense of an increased DRAM access count. Since AlexNet is a fairly small CNN compared to the much larger VGG-16, there are no large differences between both optimization targets. However, even though DRAM energy consumption is generally considered to be the main contributor in terms of overall energy, our results show that the total energy for VGG-16 is actually minimized for the min-comp case. The causes for this observation are layers 4.2 and 4.3 which exhibit a much longer runtime when optimized for min-dram. This can be explained as follows: To minimize the number of DRAM accesses, the optimization algorithm uses a configuration in which the width of the ofmap tiles $T_{ox}'$ is fairly small. In doing so, the on-chip SRAM is used to store a maximally large number of ifmap channels at the same time ($T_{if}'$ very large) thereby minimizing the need for any partial sum (psum) transfers. The small width of the ofmap tiles ($T_{ox}'$), however, causes a bad utilization of the processing core’s vALUs ($T_{ox}' < P_{ox}$) leading to the increased runtime. Finally, the energy that is consumed for baseline processing core operation during this additional runtime results in the overall higher energy consumption.

VI. MANY-CORE DATAFLOW MAPPING

To enable a large-scale evaluation of different CNNs onto arbitrary platform configurations, it is indispensable to have an automated method to assign computing tasks to the processing cores. The same taxonomy that was used for tiling the CNN layery in the single-core case (Section IV) is, therefore, used here as well. While the dashed single-core parameters such as tile-size $T_{x}'$ and tile-count $S_{x}'$ referred to data dimensions within one core, the un-dashed variables have a different meaning. These variables, namely $T_{x}$ and $S_{x}$, are used to express the size and count of complete CNN layer slices in the many-core context. So starting from the top-level, each CNN layer is subdivided into a number of slices along the ifmap and ofmap width dimension ($S_{if}$ and $S_{ox}$) as well as the ofmap channel dimension $S_{of}$ as depicted in Fig. 5a. For such a slice, it is then possible to determine an optimal single-core mapping as previously derived. An overview of the many-core mapping heuristic is given in Fig. 4 with a more thorough explanation in the following paragraphs.

In order to determine a suitable mapping it is indispensable to first define a cost function. Since we always encounter either a computation bound or an I/O bound for our application, it makes the most sense to optimize for these targets by incorporating the overall runtime and time required for communication via the NoC into the cost function. The resulting optimization goal is depicted in the following:

$$
\min_s \left( \frac{1}{\text{BW}_{\text{dram}}} \cdot \sum_{c \in \mathcal{C}} \sum_{p \in \mathcal{P}_c} F(p) \cdot W_{\text{flit}} \right) \quad (23)
$$

The first term in (23) represents all processing cores $c \in \mathcal{C}$ the one with the maximum cycle count $C_{\text{tot}_{\text{wo}_{\text{dram}}}}(s_c)$ not counting any cycles required for DRAM accesses. An abstract mapping vector $s_c$ hereby denotes the assignment of slices to processing cores. Taking the maximum is required here because in case of asymmetric mapping of slices to cores there might be a few cores left computing at the end, thereby dictating the runtime of the overall system. It can be calculated for each core as follows (see [9] and [16] for reference):

$$
C_{\text{tot}_{\text{wo}_{\text{dram}}}} = C_{\text{comp}} \cdot S_{ox}' \cdot S_{if}' \cdot S_{of}' \quad (24)
$$

In addition, the second term of (23) is used to model the overall NoC bandwidth requirement. To this end, the number of flits $F(p)$ for all NoC packets $p \in \mathcal{P}_c$ generated by each core $c$ is calculated. This is done by traversing the loop structure from Algorithm 2 and building an exact list of all packets with their associated lengths because only in doing so the overhead for e.g. having many small packets with associated header-flits can be accounted for. Since the calculation of each core’s computation cycles according to (23) requires knowledge of the single-core tiling parameters $T_{x}'$, $S_{x}'$ which in turn can only be calculated based on the slicing parameters $S_{x}$ and...

![Fig. 4: Flow-chart of many-core mapping heuristic.](image-url)
\( T_x \), we propose an iterative scheme as depicted in Fig. 4 that uses a heuristic to determine the latter parameters. This iterative process starts with determining a set \( \mathcal{T} \) of all possible slice parameters based on the constraint that the width \( T_{ox} \) and depth \( T_{of} \) of a slice should ideally be a multiple of the processing cores’ unrolling factors \( P_{ox} \) and \( P_{of} \) to maximally utilize the cores:

\[
\mathcal{T} := \{(mP_{of}, nP_{ox}) \mid \forall m \in \left[1, \left\lfloor \frac{N_{of}}{P_{of}} \right\rfloor \right], \quad \forall n \in \left[1, \left\lfloor \frac{N_{ox}}{P_{ox}} \right\rfloor \right]\} \quad (25)
\]

Afterwards, each possible slice parameter set \( T = (T_{of}, T_{ox}) \in \mathcal{T} \) is fed into the single-core tiling optimizer from Section IV and the set of optimal tiling parameters \( (T'_x, S'_x) \) is determined. Since each slice can be viewed as a new CNN layer of smaller dimension, the single-core optimizer is fed with the slice’s dimensions as follows:

\[
N'_{ox} = T_{ox} \quad (26)
\]

\[
N'_{ef} = (T_{ox} - 1) \cdot s + N_{kx} \quad (27)
\]

\[
N'_{of} = T_{of} \quad (28)
\]

Due to the constraint in the selection of the slice parameters, it only takes a few seconds to determine all possible tiling parameters. For a given slice parameter set \( T \), the number of resulting slices for each dimension is calculated as follows:

\[
S_{ox} = \left\lceil \frac{N_{ox}}{T_{ox}} \right\rceil \quad (29)
\]

\[
S_{of} = \left\lceil \frac{N_{of}}{T_{of}} \right\rceil \quad (30)
\]

As our investigations have shown especially for small CNNs such as AlexNet, it is not always desirable to distribute tasks to all processing cores. In fact, the cost for additional communication required by a large number of cores (second term in (23)) can greatly outweigh the potential saving in computational time, thereby rendering a solution with more cores slower than a competing solution with fewer active cores. Also, in addition to being slower, more active cores result in more energy being consumed during idle cycles, which again is not desirable. We found that using a waving scheme which systematically explores configurations with different numbers of active cores, starting with the ones closest to the DRAM interface block, gives better results compared to using all cores all of the time for every layer.

So in a final step, for each slice parameter set \( T \) and associated tiling parameters \( T'_x, S'_x \), aforementioned waving scheme is employed to distribute slices to core instances in the NoC. For the first step, all slices are mapped to a single core \( (k = 1) \). After this, the number of activated cores \( k \) is doubled and all tasks are assigned to the 2 cores closest to the DRAM. Again, the number of activated cores is doubled and the former steps are repeated until a configuration with all cores activated was tested. For each of these iterations, the overall cost \( C_{k,T} \) is saved in a set \( C \). Afterwards, the configuration corresponding to the lowest cost \( \min(C) \) is selected as final configuration. It should be noted that during slice assignment our algorithm makes sure to map slices with adjacent boundaries in the ofmap width dimension (neighboring \( T'_{ox} \) slices) to the same core which are then stitched together afterwards to remove the need for redundant filter loads. This method has proven to be very robust and fairly fast: Determining a mapping usually only takes a few minutes for e.g. VGG-16.

VII. MANY-CORE MAPPING EVALUATION

Using the previously described mapping scheme for the many-core case, a number of benchmarks are evaluated in this section. From a VLSI design perspective, it is much more appealing to build medium-sized processing cores and scale the system by adding more cores. This trend can be seen in the design choices made by manufacturers of large GPUs that usually consist of hundreds or even thousands of smaller RISC-like cores. Therefore, we simulate a system that employs a varying number of cores (4..128) which are scaled up or down (larger/smaller \( P_{ox} \) and \( P_{of} \) values) in such a way that the overall computing capabilities and on-chip SRAM of the system always stay at 2048 MAC cycle and 1 MByte respectively. Looking at the results for running VGG-16 in Fig. 5b, it can be concluded that while having many small cores is not optimal due to the increased communication overhead in the NoC, having only a few large cores does not give the best results. A medium-sized configuration with 16 processing cores (each core with configuration \( P_{ox} = 16, P_{of} = 8 \)) achieves the

Fig. 5: (a) Illustration of the many-core slicing. (b) Results for simulation of VGG-16 using a system-setup with constant overall computing capabilities and RAM, i.e. \( N_{cores} \times (P_{ox} \cdot P_{of}) \) & \( N_{cores} \times D_{sram} \) are constant (total MAC per cycle = 2048, total SRAM = 1 MByte).
fastest runtime for most layers as this yields the best trade-off between generating additional NoC communication on the one hand and enabling more degrees of freedom for the mapping algorithm on the other hand. It should be noted though that for networks with much larger ifmap widths, e.g. CNNs for semantic scene segmentation, it might be more favorable to include these larger cores as they provide a more natural match in terms of processing row width ($P_{ox}$). For these kinds of CNNs, however, the DRAM interface becomes the bottleneck no matter how optimal the mapping is. To further explore the performance scalability of our approach, we select the most promising processing core configuration as determined earlier ($P_{ox} = 16$, $P_{of} = 8$) and simulate the same workload, i.e. the convolutional layers of VGG-16 and AlexNet, for a system configuration starting just with a single core going up to a 5x5 NoC configuration with 23 processing cores in total. The uneven core-counts of e.g. 23 for a 5x5 NoC can be explained by the 2 positions required for the DRAM interface and the master core. Calculating the overall computational capability of each configuration (measured in MAC per second) can easily be done as follows: $N_{MAC} = N_{cores} \cdot P_{ox} \cdot P_{of}$ (each core has $D_{sram} = 128K$Byte of SRAM). For the smallest system, this results in $N_{MAC} = 128$ while the largest 23-core system offers up to $N_{MAC} = 2944$. To obtain fair values for the following speed-up comparison of a many-core system compared to the single-core case, the single-core 3x1 configuration is simulated with a very large packet-length of 10000 $\mu$s/packet. This is done in order to minimize any unnecessary communication overhead that would not be required in the single-core scenario. The results in Fig. 6 show the achieved speed-up relative to aforementioned single-core setup. Also, a line representing the theoretical bound is plotted which takes into consideration the tiling and slicing parameters generated by the algorithms introduced in Section IV and Section VI as well as the maximum available DRAM bandwidth. Said line denotes the speed-up that is achievable for given constraints without accounting for any of the overhead generated by the NoC and is calculated as follows:

$$f(N_{cores}) = \frac{C_{single-core}}{\max \left( C_{tot_{-}wo_{-}dram}, \frac{N_{sram}}{BW_{dram}} \right)}$$

(31)

where $C_{single-core}$ represents the number of processing cycles for the single-core setup.

The final simulation results in Fig. 6 show a close match between the theoretical bound as calculated by (31) and the actual system performance whereas the explanation for the gap between both curves is twofold: On the one hand, the overhead required for NoC communication including congestion phenomena slightly diminishes the achievable speedup. On the other hand, the width and depth of the last slices generated according to (25) are not necessarily a multiple of the cores’ hardware parallelism $P_{ox}$ and $P_{of}$, resulting in a core under-utilization for these last slices. On average, the difference between the simulation results and the theoretical bound is between 6.59% (N_{cores} = 2) and 27.48% (N_{cores} = 7) for AlexNet and between 3.28% (N_{cores} = 2) and 17.32%
($N_{\text{cores}} = 14$) for VGG-16. Another interesting observation is the fact that the mapping heuristic does not choose to activate more than 14 cores for any of the configurations even if more cores are available. This can be explained by the large additional NoC traffic that would be generated and, as a result, would actually slow down the overall system. Looking at the curves of Fig. 6, this trend of diminishing returns on investment can already be observed starting at 7 cores for most layers.

In general, most configurations with more than 7 cores are limited by the DRAM bandwidth with a few exceptions: Layer 1-2 and 2-1 of VGG-16 achieve very high speedups of up to 13x and 12.2x respectively for configurations with 14 cores. Since aforementioned layers are fairly wide ($N_{\text{of}} = \{224, 112\}$) and only have a limited number of output channels ($N_{\text{of}} = \{64, 128\}$), the mapping heuristic preferably slices along the width dimension. This minimizes the need for repeated loading of ifmaps thereby minimizing the bandwidth requirements and enabling the observed speedups. For later layers, this is not possible due to the larger ofmap channel counts and associated allocation of on-chip memory for filter-weights. This limitation could be overcome by enabling each core in the NoC to access the other cores’ on-chip memories in order to reduce the traffic going through the DRAM interface and thereby using the cores’ SRAM as caches.

VIII. CONCLUSION

Detailed strategies for mapping CNNs onto both single-core as well as many-core systems were presented and evaluated with regards to their practical feasibility. For the single-core mapping, two strategies, one for DRAM access minimization and one for runtime reduction, were investigated with the result that DRAM access minimization does not always lead to the desired energy reduction of the overall system. By using a system-level simulator, several system setups with different numbers of processing cores and core configurations were investigated. The results show that for the investigated CNNs AlexNet and VGG-16 configurations with 128 MAC units per core result in the highest speedups although this highly depends on the selected hardware unrolling factors $P_e$. Subsequent simulations that use this optimal core size have shown the speedup potential which saturates at a 4x4 system setup comprising 14 processing cores. The maximum speedups observed for this 4x4 system were 8.4x for AlexNet’s first layer and 13x for VGG-16’s second layer. Both layers share in common that they allow slicing in the ofmap width dimension which maps well to the given processing core’s architecture. Since unrolling in the ofmap width and channel direction is very common among other accelerators as well, similar results could possibly be obtained for them too. As usual for many-core systems, ultimately the maximum achievable speed-up is always limited by the available on-chip memory and off-chip bandwidth. The use of a NoC for the investigated application domain has shown promising results and the presented mapping heuristic has proven to make robust choices for a variety of system configurations.

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