Abstract—Cuk and SEPIC are some of the important DC-DC converters used for charging batteries. In this paper, a generalized circuit averaging technique is employed for Cuk and SEPIC converters. The derived equations are used to obtain the frequency response of open loop transfer function. The ratio of perturbed output voltage to duty cycle \( G_{vd} \) is simulated using LTSpice software package. The derived averaged models of the converters aids in faster and simpler simulation. The behavior of the converters in CCM and DCM was also simulated. The derived expressions can be generalized to power converters with two switches.

Keywords: Circuit Averaging, Cuk, DCM, CCM Instability, LTSpice, SEPIC

I. INTRODUCTION

DC-DC converters have gained popularity due to the emergence of Electric Vehicles (EVs). DC-DC converters can be classified into isolated and non-isolated topologies. Among various non-isolated converters, fourth order converters like Cuk and SEPIC have been given prominence as they provide advantages such as non-inverted output voltage and ability to operate from an input source which has a value greater or lesser than output voltage.

Determining open loop transfer function for such converters plays an important role as they provide useful info to assess converter stability and help improve controller design. In literature, several attempts have been made in examining different approaches for obtaining the transfer function. In [1], three different approaches such as: a) Small signal model, b) Circuit Averaging and c) State Space averaging for DC-DC converters in CCM and DCM was introduced.

It was shown that the losses in the converters are primarily contributed by switching and not by conduction. In [2], a SEPIC operating in DCM was selected to drive a Light-Emitting Diode (LED) for constant voltage application. An average and a switching model was developed, modeled in MATLAB / Simulink and validated against the experimental results. The transfer functions \( G_{vd} \) and \( G_{vg} \) (Output voltage to input voltage) were derived. It was shown that the SEPIC provided lower input current harmonics.

In [3], SEPIC was modelled for DCM operation by using State Space averaging technique, implemented using MATLAB and LTSpice simulation tools. It was shown that the Bode plots obtained from these tools closely matched experimental results at frequencies below 10 kHz. At higher frequencies, the simulation plots diverged from experimental results due to reduced order matrix.

In [4], an ideal SEPIC and Cuk operating in DCM are selected and used for Power Factor Correction (PFC). The advantages of the converters is discussed in detail. The input to the converters is supplied by a single phase rectifier. The open loop transfer function obtained using the small signal model are validated against the hardware results and they were found to be closely correlated.

In [5], concept of circuit averaging for converters like Buck, Boost and Buck-Boost in DCM was discussed. It was shown that the input and output ports of such converters behave like a resistive and power sink respectively.

In [6], an averaged model in LTSpice was developed for ideal Buck and Boost operating in CCM was constructed using CCM block available in LTSpice software package.

In [7], a mathematical model for Cuk converter operating in CCM was derived and modelled using Simulink. The importance of step size while capturing the transients was shown.

In this paper, DCM analysis for practical converters, SEPIC and Cuk are carried out using Circuit Averaging using LTSpice simulation tool. It was found that the cause of discontinuity in ideal and non-ideal converters was due to the sum of inductor currents \( i_{L1} + i_{L2} \) being zero. CCM-DCM block in LTSpice was used which solves for the various currents and voltages independent of the operation of the converter.

II. CIRCUIT AVERAGING FOR AN IDEAL SEPIC

Fig. 1: Circuit diagram of SEPIC

Fig. 1 shows an ideal SEPIC with two switches MOSFET and diode. The voltage across the MOSFET and diode are named as \( V_1 \) and \( V_2 \) respectively. Similarly, the current in MOSFET and diode are named as \( I_1 \) and \( I_2 \) respectively. Circuit averaging of any converter involves three major steps:
1) Separate the switch network from the converter and define the ports
2) Sketch the waveform of the switch current and voltage waveforms followed by averaging
3) Simplify equations and draw the equivalent switch network

The DCM operation occurs due to the unidirectional flow of current in the switch (Diode). Hence, the sum of inductor currents \( i_{L1} + i_{L2} \) contribute to the DCM operation in Cuk converter and SEPIC.
III. CIRCUIT AVERAGING FOR A NON-Ideal SEPIC

Fig. 5 shows a non-ideal SEPIC. The MOSFET and the diode have to be separated from the circuit as shown in Fig. 2. Fig. 6 shows the separation of the switches from the circuit with \( V_0 = V_{c2} \)

\[
< V_1 > = ((i_{L1} + i_{L2})R_{on1}D_1 + (V_{c1} + V_{c2}) + V \\
+ R_d(i_{L1} + i_{L2})D_2 + V_{c1}D_3
\]

\[
< V_2 > = ((V_{c1} + V_{c2}) - (i_{L1} + i_{L2})R_{on1})D_1
\]

\[
D_2(V_d + R_d(i_{L1} + i_{L2})) + D_3(V_0)
\]

\[
< I_1 > = D_1 * (i_{L1} + i_{L2})
\]

\[
< I_2 > = D_2 * (i_{L1} + i_{L2})
\]

From (19) and (20), it can be observed that the governing equation to describe DCM in a non-ideal SEPIC is similar to that of (15) and (16). Hence, the equivalent switch network is similar to Fig. 4.

IV. CIRCUIT AVERAGING FOR AN IDEAL CUK

Fig. 7 shows an ideal Cuk converter operating in DCM. Fig. 8 shows the MOSFET and Diode separated from the converter.

Fig. 9 shows the waveforms of switch voltages and currents at \( D_1T_s, D_2T_s \) and \( D_3T_s \) intervals.

\[
< V_1 > = D_2 * (V_{c1}) + D_3 * (V_{c1} + V_{c2})
\]

\[
< V_2 > = D_1 * (V_{c1}) - D_3(V_{c2})
\]

\[
< I_1 > = D_1 * (i_{L1} + i_{L2})
\]

\[
< I_2 > = D_2 * (i_{L1} + i_{L2})
\]

Therefore, the equivalent circuit would remain the same as that of the SEPIC.

V. CIRCUIT AVERAGING FOR A NON-Ideal CUK

Fig. 10 shows a non-ideal Cuk converter operating in DCM with the switches separated.

On Averaging the voltages and currents across the switches:

\[
< V_1 > = ((i_{L1} + i_{L2})R_{on1}D_1 + (V_{c1} + V_d + R_d(i_{L1} + i_{L2}))D_2 + D_3(V_{c1} + V_0)
\]
(26)\[D_2(V_d + R_d(i_{L1} + i_{L2})) - D_3V_0\]

(27)\[< I_1 > = (i_{L1} + i_{L2})D_1\]

(28)\[< I_2 > = (i_{L1} + i_{L2})D_2\]

It was observed that the equivalent circuit for (27) and (28) are similar to that of Fig. 4. Hence, the derived average model for two switch PWM DC-DC converter is generic and can be applied to any converter operating in DCM. The switch network is replaced by the equivalent circuit using CCM –DCM1 under average.lib in LTSpice.

VI. SPECIFICATIONS OF THE CONVERTERS

Assuming the converters’ operation in DCM, the specifications are selected. Table 1 and 2 show the specifications of Non ideal SEPIC and Cuk converters.

TABLE I: Specifications of Non Ideal SEPIC

| Parameters             | Value  |
|------------------------|--------|
| Input Voltage \((V_{g})\) | 62 V   |
| Output Voltage \((V_o)\)  | 22 V   |
| Output Resistance, R    | 52 Ω   |
| Inductor, \(L_1\)       | 13 mH  |
| Inductor, \(L_2\)       | 166 µH |
| Inductor ESR, \(R_{L1}\) | 130mΩ  |
| Inductor ESR, \(R_{L2}\) | 110mΩ  |
| MOSFET Resistance, \(R_{on1}\) | 31mΩ  |
| Duty Cycle, D           | 0.2    |
| Capacitor, \(C_1\)      | 0.5 µH |
| Capacitor, \(C_2\)      | 1000 µH |
| Capacitor ESR, \(R_{C1}\) | 270mΩ  |
| Capacitor ESR, \(R_{C2}\) | 110mΩ  |
| Switching Frequency, \(f_s\) | 50kHz |
| Diode Drop, \(V_d\)     | 0.75V  |
| Diode Forward Resistance, \(R_d\) | 0.12 Ω |

TABLE II: Specifications of Non Ideal Cuk

| Parameters             | Value  |
|------------------------|--------|
| Input Voltage \((V_{g})\) | 25 V   |
| Output Voltage \((V_o)\)  | -21 V  |
| Output Resistance, R    | 100 Ω  |
| Inductor, \(L_1\)       | 1 mH   |
| Inductor, \(L_2\)       | 1mH    |
| Inductor ESR, \(R_{L1}\) | 0.15Ω  |
| Inductor ESR, \(R_{L2}\) | 0.2Ω   |
| MOSFET Resistance, \(R_{on1}\) | 31mΩ  |
| Duty Cycle, D           | 0.42   |
| Capacitor, \(C_1\)      | 850 µH |
| Capacitor, \(C_2\)      | 47 µH  |
| Capacitor ESR, \(R_{C1}\) | 0.2Ω   |
| Capacitor ESR, \(R_{C2}\) | 0.3Ω   |
| Switching Frequency, \(f_s\) | 20kHz |
| Diode Drop, \(V_d\)     | 0.75V  |
| Diode Forward Resistance, \(R_d\) | 0.11Ω |

VII. COMBINED MODEL FOR CCM-DCM

The advantages of using such model is (a) Simulation of CCM / DCM operation can be achieved in the same model (b) The decision is taken by the model and is made internal to the circuit CCM/DCM 1 is an averaged block available under average.lib in LTSpice. A common equation satisfying CCM and DCM operation is shown below

For CCM and DCM operations, one of the governing equations is shown in [6] and (4). Where \(\mu\) is the duty cycle in DCM operation.

\[< I_1 > = V_1/R_e\] (29)

\[< V_1 > = ((1 - \mu)/\mu) V_2\] (30)

Where \(\mu\) is the duty cycle in DCM operation. Substituting, (30) in (4),

\[\mu = \frac{V_2}{V_2 + I_1 R_e}\] (31)

\[\mu = \frac{1}{1 + (R_e I_1)/V_1}\] (32)

\[\mu = D\] (33)

(32) and (33) define D for the converter in CCM and DCM operations. Combining them,

\[\mu = \max\left(d, \frac{1}{1 + (R_e I_1)/V_1}\right)\] (34)

It can be noted from [1], that \(\mu_{DCM} > \mu_{CCM}\). The model uses two inputs viz, (a) \(L_{eq} = L_1 L_2/(L_1 + L_2)\) and (b) \(f_s\).
VIII. RESULTS

Simulations were performed using LTSpice software package. The equivalent switch network was available as a built-in library under ‘average.lib’, CCM-DCM1. D was varied from 0.2 to 0.9 in steps of 0.01 and $V_0$ was analyzed. It was observed from Fig. 11 that $V_0$ and $i_{L1}$ increased with the increase in duty cycle. However, $i_{L2}$ decreased when the duty cycle increased which describes the working of a typical SEPIC. Varying D, step changes in $R_{L1}$ and $R_{L2}$ were applied.

$V_0$ and $i_{L1}$ were captured for the changes made. From Fig. 12 it was observed that highest value of $R_{L1}$ and lowest value of $R_{L2}$ showed maximum $V_0$. Fig. 13 shows the bode plot of $G_{vd}$ for a fixed load R. It was observed from that the phase crossover frequency was around 1.814 kHz, Gain margin around 5.254 dB, gain cross over frequency around 76.834 kHz, phase margin around 92.845°. Fig.14 shows the nature of $V_0$, $i_{L1}$ and $i_{L2}$ for varying D proportional to the the control voltage, $V_c$ for a Cuk converter. It was observed that as D increased, $V_0$ and $i_{L2}$ decreased which defines the typical working of the Cuk converter. Varying D, steps changes in $R_{L1}$ and $R_{L2}$ were applied. It can be observed from Fig. 15 that highest $R_{L1}$ and least $R_{L2}$ showed maximum $V_0$. Fig. 16 shows the frequency response of $G_{vd}$ for a fixed load R. The gain margin was to be infinity, phase cross frequency of 81.982 kHz and phase margin around 200.391°.
In this paper, the circuit averaging technique for fourth order converters like Cuk and SEPIC was carried out to obtain the frequency response for $G_{vd}$ using LTSpice simulation. This method can be generalized to find the response for any two switch DC-DC converters operating in CCM / DCM. This helps in developing an efficient feedback control design. Higher D produced higher $V_0$ in the converters. An appropriate controller to achieve sufficient gain margin and phase margin in closed loop operation and DCM analyses for isolated converters using CCM/DCM2 block are recommended.

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