Research article

Schottky barrier inhomogeneities at the interface of different epitaxial layer thicknesses of n-GaAs/Ti/Au/Si: Al_{0.33}Ga_{0.67}As

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ABSTRACT

The effects of an epitaxial layer on the rectifying behavior of n-GaAs/Ti/Au/Si:Al_{0.33}Ga_{0.67}As diodes have been examined through the inhomogeneity model on n-GaAs substrate with orientation. The electrical properties and conduction mechanism of these materials were understood through theoretical models. The inhomogeneity model was used to electrical behavior of these diodes was explained. The barrier height inhomogeneity model reveals a 13% and 15% barrier height inhomogeneity in N1 and N2 Schottky diodes, respectively. The ideal thermionic emission behavior increases the ideality factors and reduces barrier heights. Within the entire temperature range, the effective Schottky barrier for a thin epitaxial layer was higher. Such results depicted the presence of defects in the thick layer, which decreased the barrier height and ultimately degraded diode performance. The thermionic emission theory along with Gaussian distribution of barrier heights is explained by the temperature dependence of the forward bias current-voltage-temperature (I-V-T) features.

1. Introduction

Schottky diodes are essential in several semiconductor devices, which include metal-semiconductor field-effect transistors (MESFETs), solar cells, microwave diodes, and photodetectors [1]. Schottky barrier's characterization serves as the fundamental block of semiconductor devices. It portrays a likely barrier for external device connection at the metallization of a semiconductor surface [2]. III-V semiconductors dominate the low power applications and high frequency even though silicon continues to control the semiconductor industry [3, 4].

Gallium arsenide Schottky barrier diodes have been widely investigated because of their applications in many optoelectronics and microwave devices [5]. The p-type AlGaAs are extensively used in many hetero-structured semiconductors with high electron mobility transistors and laser devices [6]. The Schottky barrier inhomogeneity model was developed by Werner and Güttler [7]. This model assumes a barrier height with a Gaussian distribution to explain the current-voltage (I-V) characteristics deviation of these devices [8].

Schottky barrier height and ideality factors are significant factors that are temperature-dependent [9]. The calculated binding energy is 8.557 meV, whereas, the Si donor impurity in GaAs has a value of 5.86 meV [10]. In another study, the ionization energy of Si donor in AlGaAs was estimated to be 60 meV [11]. Schubert and Ploog [12] have estimated the thermal activation energy of n-type AlGaAs to be 130–135 meV at an alloy composition 0.20 ≤ x ≤ 0.30 and 140–150 meV at an alloy composition 0.35 ≤ x ≤ 0.40.

The conduction mechanism is revealed from the temperature dependence in these I-V structures and capacitance-voltage (C-V) characteristics [13]. In real simple metal-semiconductor Schottky diodes, the extraction of Schottky diodes becomes difficult with an ideality factor (n = 1) [14]. Because of non-ideal thermionic emissions, generation-recombination and quantum mechanical tunneling are encompassed within real simple metal-semiconductor in the space charge region [15]. Thereby, the ideal case deviates from the I-V characteristic where a fixed homogeneous SBH and abrupt junction are observed.

It is assumed that Li et al [16] have only investigated the electrical properties of GaAs/AlGaAs heterostructures in 2019, which can provide useful information about the improvement in these structures, even though these diodes have been examined for more than four decades. Therefore, this study has reported the impact of epitaxial layer thickness on the Schottky barrier height (SBH) and the ideality factor in Al_{0.33}Ga_{0.67}As as elevated by molecular beam epitaxy (MBE) throughout the temperature range of 300–420 K.

The electronic parameters of the Schottky barrier diodes also depend on temperature. This dependence changes the diodes' electronic parameters with temperature. The zero-bias height and the ideality factor

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values showed strong dependence on temperature changes. Thus, this study aimed to examine the impacts of the epitaxial layer thickness on Schottky barrier inhomogeneities in \( n\text{-GaAs/Ti/Au}/Si:Al_{0.33}Ga_{0.67}\text{As} \) as structures at the temperature range 300–420 K. With this aim, the inhomogeneity theory provides information on diode performance.

\( n\text{-AlGaAs/n-GaAs} \) Schottky diodes were classified by I-V from 300–420 K in this study. The diode parameters were then obtained from such attributes and were analyzed for identifying the specific type of mechanism for transferring heat, which is conduction mechanism. It was revealed that the clear ideality factor escalates with increasing temperature and it fulfills a high value of ~3 at 420 K. The objective of this work was to explain the infrequent behavior and pattern. The numerical computation was to examine whether impairments contribute in the development of this irregular trend. The analytical modeling shows the dominance of conduction mechanism.

2. Material and methods

The molecular beam epitaxy (MBE) method was used to fabricate \( n\text{-GaAs/Ti/Au}/Si:Al_{0.33}Ga_{0.67}\text{As} \) diodes on (100) \( n^-\text{GaAs} \) substrates. In it, the films were doped with Si. The study uses two different AlGaAs films with diameters of 0.75 mm. Both N1 and N2 samples had a carrier concentration of \( 2 \times 10^{18} \text{ cm}^{-3} \) with layer thicknesses of 1.5 and 2 \( \mu \text{m} \), respectively. A Varian Gen II system was used to elevate the samples in the work with the implementation of MBE on oriented \( n^-\text{GaAs} \) substrates.

The ionization gauge was used to measure the As Ga beam equivalent pressure ratio at approximately 12:1. The growth temperature is 610 \( ^\circ \text{C} \); the growth rates are 1 \( \mu \text{m} \) per hour for GaAs and 0.5 \( \mu \text{m} \) for AlAs, and arsenic overpressure is 1.2 \( \times 10^{-5} \text{ Torr} \). The epitaxial layer structures consisted of 1 \( \mu \text{m} \) GaAs \( (n = 3 \times 10^{16}) \) buffer layer followed by 1.5 \( \mu \text{m} \) for sample N1, and 2 \( \mu \text{m} \) for sample N2 Si-doped \( Al_{0.33}Ga_{0.67}\text{As} \) layer.

Schottky contacts were prepared by evaporating Ti/Au metal on the top layer and developed ohmic contacts based on the \( n^-\text{GaAs} \) substrate to evaporate Ge/Au/Ni/Au.

Diode measurement was performed in the standard temperature range of 300–420 K with 20 K steps using a closed cycle refrigerator Janis CCS-450 cryostat. A Lake Shore 331 temperature controller was used to control the temperature with \( \pm 0.1 \text{ K} \) sensitivity. The schematic geometry of the diode is shown in Figure 1. Written Matlab programs were used to determine different parameters from I-V characteristics.

3. Results and discussion

Figure 1 shows GaAs grown using low-temperature MBE, which were used as a buffer layer. The buffer layer is inserted between the active layer and the substrate. This GaAs layer provides a smooth interface when the structure is developed under ideal conditions [13]. The GaAs buffer layer is effectively grown at low temperatures because it is crystalline, highly resistant, and constitute a high breakdown voltage [14]. Both Schottky samples were used to portray behavioral and asymmetrical structures to demonstrate the rectification capacity of the devices. The asymmetry is explained as the proportion between forward and reverse current at certain applied voltage.

The results of Figure 2 represent forward bias I-V plots on a semi-logarithmic scale for both \( Si: Al\text{GaAs} \) films. Current increases in both devices with applied bias. The barrier distribution deformation under applied bias was identified by contacting the abrupt Schottky's ideality coefficient [15]. The reverse current was comparatively higher in thicker epitaxial layers. The I-V characteristic for diode N1 was more temperature-sensitive than that of device N2. The current flowing through device N2 is greater than the current made from device N1. Schottky barrier diodes are extensively used in the electrical characterization of defects, which are introduced during device processing, semi-conductor growth, and device testing after fabrication. The I-V characteristics obtained at different temperatures have provided complete information regarding the quality and transport process of Schottky barrier diodes (Figure 2).

In the thicker epitaxial layer N2, the reverse current was slightly observed higher as witnessed in Figure 2. The current/voltages characteristics provide a comprehensive illustration of the Schottky barrier diodes’ quality and transport process. Therefore, the reliance of temperature is often implemented on the I-V features as it provides explicit information about the type of mechanism used and illustrates emphasis on the likely non-ideality effects. In this study samples, a temperature range of 300–420 K was selected to perform I-V-T characteristics.

Schottky diode characteristics that follow the thermionic emission (TE) theory related to the diode's I-V relationship can be expressed through Eq. (1) [10],

\[
I = I_s \exp \left( \frac{qV}{n kT} \right) - 1
\]  \hspace{1cm} (1)

The saturation current is given by,

\[
I_s = A^+T^2 \exp \left( - \frac{q\phi_b}{kT} \right)
\]  \hspace{1cm} (2)

Where \( T \) is the temperature in Kelvin, \( A \) is the diode area, and \( A^+ \) is the Richardson constant and \( q \) is the absolute value of electron charge. From equation [2], the Schottky barrier height (\( \phi_b \)) is gained [10]:

\[
\phi_b = \frac{kT}{q} \ln \left( \frac{A^+T^2}{I_s} \right)
\]  \hspace{1cm} (3)

The value of the ideality factor ‘\( n \)’ can be calculated from the equation.

\[
n = \frac{q}{kT} \left( \frac{dV}{d \ln I} \right)
\]  \hspace{1cm} (4)

The ideality factors of the diodes are determined from the I-V characteristic, showing higher unity of the acquired ideality factors (\( n > 2 \)). Due to the presence of insulating layer, the higher ideality factor is found between the semiconductor and metal. These factors cause a downward curvature in I-V plots of the diodes with higher forward biases. This downward curvature causes non-ideal behavior because of the presence of series resistance and interface irregularities in the thickness of an epitaxial layer.

Barrier height inhomogeneity (BHI) causes abnormal electrical behavior in the Schottky barrier [17, 18, 19, 20]. When the barrier height fluctuates between low and high regions, it is considered an inhomogeneous barrier height and can be modeled with a Gaussian distribution [21]. The theoretical values of the Schottky barrier height (\( \phi_b \)) obtained from equation [3] are shown in Table 1.
The efficient values of Schottky barrier height for N1 and N2 varied from 0.952 eV and 0.844 eV at 300 K to 0.903 eV and 0.756 eV at 420 K. On the contrary, the ideality factor for N1 and N2 varies from 1.889 eV and 1.608 eV at 300 K, while the variation was 2.973 eV and 3.764 eV at 420 K. For both samples, the findings have shown that the effective barrier height ($\Phi_b$) reduces with elevating annealing temperature, while there was an increase in the ideality (n) factor.

The Gaussian model described by Werner and Güttler was used to explain the results [7]. The barrier height inhomogeneities in Schottky diode can be described by Gaussian distribution function having a mean value $\Phi_b$ and a standard deviation $\sigma_s$ [7].

\[ P(\Phi_b) = \frac{1}{\sigma_s \sqrt{2\pi}} \exp \left[ -\frac{(\Phi_b - \Phi_{\text{bo}})^2}{2\sigma_s^2} \right] \quad (5) \]

where $1/\sigma_s \sqrt{2\pi}$ is used to represent constant value for normalizing the Gaussian barrier height distribution. Following equation shows the overall current across a Schottky diode at the forward bias with barrier height inhomogeneities:

\[ I(V) = \int_{-\infty}^{\infty} I(\Phi_b, V) P(\Phi_b)d\Phi \quad (6) \]

Next equations show the ideality factor and barrier height, respectively:

\[ \Phi_{\text{ap}} = \Phi_{\text{bo}} - \frac{q\sigma_s^2}{2kT} \quad (7) \]

\[ \left( \frac{n_{\text{ap}}}{n_{\text{bo}}} - 1 \right) = \rho_1 - \frac{q\rho_3}{2kT} \quad (8) \]

where $\Phi_{\text{bo}}$ is the zero bias barrier height and $\sigma_s$ is the standard deviation, which are linearly bias dependent on Gaussian parameters, such as $\Phi_b = \Phi_{\text{bo}} + \rho_2 V$ and $\sigma_b = \sigma_{\text{bo}} + \rho_3 V$.

The temperature-dependent on ideality factor (n) and Schottky barrier height ($\Phi_b$) can be explained by local variations in the Schottky barrier height ($\Phi_b$) around the mean barrier height ($\Phi_{\text{bo(mean)}}$) through

Figure 2. Experimental forward bias of n-GaAs/Ti/Au/Si: Al$_{0.33}$Ga$_{0.67}$As Schottky diode at (a) various temperatures for N1 (1.5 μm) and (b) N2 (2 μm).

Table 1. Experimental values of Schottky barrier heights and ideality factors for both N1 and N2 devices.

| T (K) | $\Phi_b$ (eV) (N1) | $\Phi_b$ (eV) (N2) | n (N1) | n (N2) |
|-------|------------------|------------------|--------|--------|
| 300   | 0.952            | 0.844            | 1.889  | 1.608  |
| 320   | 0.936            | 0.833            | 2.126  | 1.741  |
| 340   | 0.928            | 0.821            | 2.343  | 1.962  |
| 360   | 0.919            | 0.792            | 2.662  | 2.263  |
| 380   | 0.911            | 0.767            | 2.904  | 2.752  |
| 400   | 0.907            | 0.753            | 2.922  | 3.331  |
| 420   | 0.903            | 0.756            | 2.973  | 3.764  |

Figure 3. Plot of ln (I/$T^2$) versus $10^3/T$ of Schottky diode with epitaxial layer thicknesses for (a) 1.5 μm and (b) 2 μm.
the Gaussian model. The reverse current increases with annealing to reduce the effective barrier height.

An Arrhenius plot of the forward current was obtained by plotting ln I_s/T^2 against 10^3/T, which gives the theoretical barrier heights Φ_b. The barrier heights Φ_b had a value of 1.071 eV for N1 devices and 0.953 eV for N2 devices. N1 and N2 diodes have similar temperature requirements regarding barrier height as compared with the barrier heights of diodes with a thick epitaxial layer and the values of those with a thin epitaxial layer increased [21] (Figure 3).

A reduction is shown in the sequence of effective barrier height when the reverse current elevates with annealing characteristics [22]. Wang et al. [23] have shown that annealing samples will increase the interface barrier heights. The energy carriers acquire sufficient energy for surmounting the patches. As a result, the ideality factor and; thus, the barrier height becomes temperature-dependent [25, 26].

The inhomogeneities of the barrier height in Schottky diodes explain the differences in the barrier height against the ideality factor (Figure 4). The barrier height has a Gaussian distribution over the Schottky contact area with mean barrier height (Φ_b0(mean)) and the standard deviation (σ_b), which corresponds to the distribution parameters [28].

\[
\Phi_{b0} = \Phi_{b0\text{, mean}} - \frac{q\sigma^2_{b0}}{2kT}
\]

Equation [9] gives a straight line to (Φ_b0(mean)) and (σ_b) as the intercept and slope, respectively. The plot between the barrier height and q/(2kT) (Figure 5) shows the mean barrier height of 0.779 eV and a standard deviation of 0.094 V for diode N1. It shows the mean barrier height of 0.505 eV and a standard deviation of 0.125 V for diode N2. It is therefore clear that the standard deviation is ≈13% for N1 and ≈25% for N2 by comparing (Φ_b0(mean)) and (σ_b) parameters. Compared with the mean barrier height for both diodes, the standard deviation was higher. The higher value of the standard deviation indicates increased inhomogeneities in the barrier height (Figure 5). Therefore, the lower σso value gives better rectifying performance and ideal behavior [26].

To obtain the effect of the inhomogeneity barrier height, equation [2] and [9] are combined:

\[
I_s = A\exp \left(-\frac{q\Phi_{b0\text{, mean}} - q\sigma^2_{b0}}{2kT}\right)
\]

This leads to the modified version of the conventional Richardson plot,

\[
\ln \left(\frac{I_s}{T^2}\right) - \ln[A\exp \left(-\frac{q^2\sigma^2_{b0}}{2k^2T^2}\right)] = \ln[AA^*] - \frac{q\Phi_{b0\text{, mean}}}{kT}
\]

The plot between ln (I_s/T^2) - (q^2σ^2_{b0}/2k^2T^2) versus 10^3/T yielded a straight line that gave an apparent barrier height and intercepts equal to the (ln AA^*) (Figures 6 and 7).
Equation [11] was plotted for both samples, which showed apparent barrier heights of 1.36 eV for diode N1 and 1.24 eV for diode N2. The inhomogeneities model fits well with the I-V data because the high value of the standard deviation indicates decreased homogeneous barrier height (Table 2).

The existence of an insulator layer can be influenced by the barrier height distribution in the junction at the interface and this charge density can emerge using a net charge in interface states or using mobile carriers collected at the junction interface [29, 30].

The thicker epitaxial layer of a similar material showed lower barrier height, which is confirmed by the results [21]. Some of the Schottky diodes follow the TE mechanism, whereas others do not follow this mechanism because of the patches related to decreased barrier height that is embedded in the interface of the Schottky diodes. This can be explained through the terms of density states that increase at the semiconductor surface because of surface roughness [30].

A similar result has been indicated for the I-V-T characteristics that employed the Schottky diodes along with decreasing temperature. The epitaxial thickness layer in this study was based on two specimens at two temperatures, while Zhang [27] has performed the epitaxial layer thickness at three different temperatures such as 300 K, 573 K, and 673 K.

The results in Table 3 show that the BHI increased from 13% to 25% as the thickness increased from 1.5 to 2 μm. Compared with (Φb0(mean)), the obtained (σso) for all samples was not small enough, which causes greater interfacial inhomogeneity and potential fluctuation [19]. The presence of BHI attributes in I-V and Richardson plots deviation from linearity [32].

The intercept of the Figure 7 which is the value of Richardson constant A** (Eq. (11)) is closely aligned with the value of 8.16 A cm⁻² K⁻² for n-type GaAs [33]. Also, the theoretical analysis is introducing to calculate the position of the Fermi level using a numerical iteration method developed by the author depending on the concentrations of the doping. The charge neutrality condition can be used to determine the position of the Fermi level (EF) and by considering fully ionized donor ND and acceptor NA concentrations, given by [10].

\[ p - n + N_D - N_A = 0 \] (12)

n and p are the electron and hole densities in the conduction and valence band respectively denoted by:

**Table 2.** Barrier height (Φb) as obtained from the I-V method and the modified plot of the conventional Richardson plot according to the inhomogeneities model for the two devices.

| Devices ID | Φb (eV) | Eq. (3) at R.T. | Eq. (9) | Eq. (11) |
|------------|---------|----------------|---------|----------|
| N1         | 0.952   | 0.779          | 1.36    |
| N2         | 0.802   | 0.505          | 1.24    |

**Table 3.** Comparison between the results of inhomogeneity model parameters.

| Φb0(mean) (eV) | σso (V) | Inhomogeneities % | Reference |
|----------------|---------|-------------------|-----------|
| 0.788          | 0.091   | 12%               | [31]      |
| 0.779          | 0.094   | 13%               | This work |
| 0.505          | 0.125   | 25%               | This work |

Figure 6. Modified plot of the conventional Richardson plot according to the inhomogeneities model for an N1 sample.

Figure 7. Modified plot of the conventional Richardson plot according to the inhomogeneities model for an N2 sample.

Figure 8. The value of the Fermi level against the temperature of the Si:AlGaAs samples. The zero energy presents the bottom of the conduction band.
investigated that the effective barrier height depends on the voltage applied to the diodes with different inhomogeneities. A study variation in the Schottky barrier height and its dependency on the essentially in the studied devices.

There is good reason to think that tunneling mechanism is contributes results for the other sample. At room temperature the position of EF is behavior for Si:AlGaAs, and that all the dopants are ionized (similar re-

doping concentration, 

The energies of the bottom of the conduction band, the valence band’s top, the states’ effective density, and effective states in the valence band is represented through Ec, Ev, NC and NV, respectively. The position of the EF increases with temperature T as shown in Figure 8. It was found that the EF is located inside the conduction band Ec. According to Figure the zero energy presents the bottom of the conduction band. However, the material clearly shows the non-degenerate behavior for Si:AlGaAs, and that all the dopants are ionized (similar re-

The room temperature (I-V) measurements are not sufficient to give enough information about the metal-semiconductor contact. Therefore, performing the measurements at a wide range of temperatures is required to give complete and detailed information regarding the conduction mechanism and explains the possible non-ideality effects. In this work, the electrical properties of AlGaAs Schottky diode were fabricated using Si as the n-type dopant. The experimental forward bias I-V-T curves based on TE theory revealed that the barrier height was decreased with increasing thickness of the epitaxial layer. Both samples indicated a real-life thermionic emission behavior was not working since ideality factors were observed to incline and barrier heights reduce with elevating the temperature. Nonetheless, the effective Schottky barrier was greater throughout the overall range of temperatures for the thinner epitaxial layer. Such observation might be presumed to the occurrence of further defects such as DX-like and DX centers in the thicker layer that degrade the diode performance and reduce the barrier height. The intercalation procedure was estimated to be approximately 0.75 eV of the Schottky barrier height. Drawing of the Fermi level as a function of temperature was used to examine whether the material was degenerated or not. Si ionization was dependent on the thermal energy and the position of the Si level within the energy bandgap. Also, by using the tunneling probability factor E00, it was predicted that the conduction mechanism of the carriers may dominate over other current transport. The conduction mechanism in any device depends on different parameters such as barrier height formation, the doping carrier concentration of the sample, and the substrate temperature. Buffer layer plays an important role in device performance and it works well in the device under study according to the desired requirements.

4. Conclusion

The energies of the bottom of the conduction band, the valence band’s top, the states’ effective density, and effective states in the valence band is represented through Ec, Ev, Nc and Nv, respectively. The position of the Ec increases with temperature T as shown in Figure 8.

The estimated E00 was found to be 25.2 meV for doping concentration of 2 × 10¹⁶ cm⁻³, which is much smaller than kT. With such value of E00, there is good reason to think that tunneling mechanism is contributes essentially in the studied devices.

The temperature-dependent I-V technique has been used to study the variation in the Schottky barrier height and its dependency on the voltage applied to the diodes with different inhomogeneities. A study investigated that the effective barrier height depends on the inhomogeneity and the voltage applied [35]. This clearly explains that the barrier height increases in diodes with small inhomogeneity compared with diodes with large homogeneity.

To discuss the effect of buffer layer during the growth process, impurities are unavoidably present in and on the substrate for migrating towards the epitaxial layers as noticed by Umansky’s group [36]. Development of a comparatively thick buffer layer, which in many cases comprises of AlGaAs-GaAs superlattice (SL) because of the high-chemical reactivity of the aluminum-containing layers for retarding impurities from migrating. Apparently, the selection of compensating doping density is based on to ensure complete ionization of dopants in order to avoid a parallel conductance path [36].

Imaizumi et al group [37] also discuss the benefit of using the buffer layer in their devices, by noticing that GaAs layer is comparatively relaxed but comprises of major dislocations when larger lattice and smaller layer thicknesses divergences are instigated in the buffer layer structure. On the contrary, few dislocations comprised within the GaAs layer but there is an opposite buffer layer design in a deformed lattice structure [37]. Additionally, the GaAs lattice plane tends to elevate with a development towards the off-cut angle direction of the GaP substrate in the case of large lattice and small layer thicknesses.

The material selected for the buffer layer is a dielectric including polyamide, silicone, and polypropylene. Low dielectric loss is comprised within these materials, restricting such materials from heating in the radio-frequency field. These dielectrics have a likelihood to have high breakdown voltage limit [38]. It becomes significantly importance as the main work aspects have a tendency to possess a lower dielectric breakdown in melted condition.

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Declarations

**Author contribution statement**

Noorah Ahmed Al-Ahmadi: Conceived and designed the experiments; Performed the experiments; Analyzed and interpreted the data; Contributed reagents, materials, analysis tools or data; Wrote the paper.

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The authors declare no conflict of interest.

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