A 15-bit, 5 MSPS SAR ADC with on-chip digital calibration

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Abstract. In this paper, a digital algorithm based on a 15-bit, 5 million samples per second (MSPS), high-speed successive approximation register (SAR) analog-to-digital converter (ADC) is presented. It features on comparator offset cancellation and capacitor mismatch calibration. The algorithm uses a 13-bit bypass array to measure the errors of both comparator and capacitors. During calibration, errors are read and put into the bypass array to compensate for the mismatches of the main array. Verified by MATLAB, the errors of the SAR ADC output can be corrected into 1 LSB with the help of calibration. The simulation results show that the proposed algorithm improves the precision of the SAR ADC significantly.

1. Introduction
The Internet of Things, automotive electronics and smart home in the forthcoming technological generation require energy efficient analog-to-digital converter (ADC) with high precision and high sampling rate. Benefiting from its low power consumption and simple structure [1], successive approximation register (SAR) ADC based on charge redistribution have gained great popularity. In recent researches, SAR ADC can achieve a resolution of 16 bit or higher and a sampling rate of several MSPS.

However, capacitor mismatches and comparator offset affect the accuracy of SAR ADC seriously with the number of bits increasing. Many digitally assisted techniques have been reported in an attempt to resolve the issue. Foreground calibration [2][3][4] and background calibration [5][6] were proposed to eliminate the mismatches of the capacitors. A multiple sub-array [7] was used to calibrate the high-order array in the digital-to-analog converter (DAC). In conventional high-performance SAR converters, the binary scaled DAC networks was used for settling error compensation [9][10]. Furthermore, A 14-bit SAR ADC with self-calibration and digital-trim technique [8] was proposed to correct static mismatches in CDAC. The technique reduces integral nonlinearity from as high as 7 LSBs down to 1 LSB. However, it needs several redundant capacitors to perform the calibration, which requires more clock cycles.

In this paper, a novel digital correction algorithm for 15-bit differential SAR ADC is described to correct the DAC mismatches for improving the linearity performance. This algorithm employs a 13-bit bypass array to compensate for the linearity due to both the mismatches of binary-weighted capacitors and the parasitic capacitance of the bridge capacitor. During the calibration cycle, typically performed after each power up, the offset of the comparator and the ratio errors of capacitors are calculated by the bypass array. Later in the subsequent normal conversion, the errors are read from the register and put into the bypass array to correct the ADC output in real time.
The rest of this paper is organized as follows. Section 2 describes the SAR ADC with bridge capacitor and the whole structure with calibration. Section 3 introduces the digital correction algorithm and principles. The simulated results are listed in Section 4. Finally, the conclusion is presented in Section 5.

2. Circuit Design

2.1. SAR ADC with bridge capacitor

Using split DAC is an effective way to reduce both chip area and capacitor’s value [12]. Figure 1 shows the split DAC with the fractional value bridge capacitor $C_S$. The bridge capacitor $C_S$ is implemented so that the two capacitor arrays have the same scaling [12]. The total weight of the left array is equal to the weight of the lowest bit in the right array. The left side is called LSB array, while the right side is MSB array.

2.2. SAR ADC with calibration circuit

Figure 2 shows the SAR ADC schematic with calibration circuit. The actual design is differential, here using single-ended design for simplicity. It consists of a 15-bit split DAC, a comparator, a SAR control logic and additional bypass DAC. The 13-bit bypass array is used to compensate for the mismatches of the capacitor in the main array. The left array is connected to the right array through the bridge capacitor $C_S$, and the bypass capacitor is connected through capacitor $C_{CS}$ in similarity. The comparator offset is measured at first in order to correctly detect the mismatches of the DAC [13]. Compared with the 8-bit lower array, the 13-bit bypass array can distinguish the smallest error of $1/32$ LSB, resulting in a total error less than $15/64$ LSB, so that the accuracy of the final result can be guaranteed.

3. Digital correction algorithm

The algorithm is implemented with the help of the bypass array in Figure 2. In this algorithm, errors associated with each capacitor in the main array are measured and stored during the calibration mode. Later the error calibration codes are used to program the bypass capacitors during normal operation.

3.1. Algorithm

For the N-bit DAC, each binary-weighted capacitor $C_k$ has a normalized error $C_{e_k}$ relative to the ideal value. Define the unit capacitance as

$$C_u = \sum_{k=0}^{N} C_k / 2^N$$

(1)

$C_0$ is the value of the dummy capacitance, which equals to 1. The capacitance of the main array can be written as
The purpose of the calibration is to obtain the mismatch of each capacitor compared with ideal value. However, the mismatch cannot show in the circuit directly. Therefore, we firstly measured the error between the tested capacitor and the sum of all capacitors smaller than it, and then calculate the wanted mismatch value.

The calibration cycle begins with the measurement of the error voltage due to the MSB capacitor $C_N$ [11]. The ratio error between $C_N$ and the sum of $C_{N-1}$-$C_0$ measured by bypass array is $X_{d,N}$. The $C_T$ is the sum of all capacitances in LSB and MSB array. Due to the mismatch, the voltage of the capacitors’ top plate after charge redistribution is changed. In other words, the error voltage is a direct reflect of the mismatch. Then the error voltage is expressed by the bypass array. The final correction code, which represents the deviation value of the capacitors in the main array, is defined as $x_N$. We can obtain

$$C_k = 2^{k-1}C_u + C_{r-k} \quad (1 \leq k \leq N) \quad (2)$$

From (3), the relationship of $x_N$ and $X_{d,N}$ is shown in (4). From the equation, it is easy to calculate the $x_N$ through $X_{d,N}$, which can be obtained from the circuit directly. The weight of the bypass array should multiply a factor of $k$ due to the bridge capacitor $C_{CS}$. Since the operations are all implemented on the bypass array, $k$ does not affect the accuracy of the subsequent calibration.

Similarly, the code value for the (N-1) bit capacitors can be expressed as

$$C_{N-1} + \sum_{k=0}^{N-2} C_k + C_N = C_T \quad (5)$$

Hence, $x_{N-1}$ can be calculated as

$$x_{N-1} = -\frac{1}{2}X_{d,N-1} + \frac{1}{4}X_{d,N} \quad (6)$$

According to (4) and (6), $x_k$ can be obtained by recursion
To calculate the $x_k$ of each capacitance in the main array, we should measure the $X_{d,k}$ between the $k$th capacitor and other capacitors smaller than it. The measurement begins with the MSB capacitor and ends with the LSB capacitor in sequence. Here takes the $n_{th}$ capacitor for example.

Firstly, connect the capacitors of the $n+1$~$15_{th}$ bits to $V_{CM}$ in both plates and keep them unchanged during subsequent operations. $V_{CM}$ refers to the common mode voltage of the input. Then, connect the top plate of other capacitors in the main array to $V_{CM}$. The bottom plate of the $n_{th}$ capacitor toggle from $V_{REF}$ to ground, and the remaining capacitors toggle from ground to $V_{REF}$. Suppose the voltage of the top plate at this moment is $V_X$, the total charge on the main array is given by

$$ Q = V_{CM} \sum_{k=0}^{n-1} C_k + (V_{CM} - V_{ref}) \cdot C_n $$

(8)

Next, disconnect the top plate of all capacitors from $V_{CM}$. The bottom plate of the $n_{th}$ capacitor toggle from $V_{REF}$ to ground, and the remaining capacitors toggle from ground to $V_{REF}$. Suppose the voltage of the top plate at this moment is $V_X$, the total charge on the main array is

$$ Q' = V_x \cdot C_n + (V_x - V_{ref}) \cdot \sum_{k=0}^{n-1} C_k $$

(9)

Due to charge conservation of (8) and (9), it can be easily shown that

$$ V_x = V_{CM} - \frac{C_n - \sum_{k=0}^{n-1} C_k}{C_n + \sum_{k=0}^{n-1} C_k} \cdot V_{ref} $$

(10)
From (10), the error voltage caused by $n_\theta$ capacitor is

$$V_k = \frac{C_n - \sum_{k=0}^{n-1} C_k}{C_n + \sum_{k=0}^{n-1} C_k} V_{\text{ref}}$$

(11)
The error ratio of the $n_0$ capacitor is directly reflected by the error voltage $V_e$. Then, $V_e$ is expressed by the bypass array to get the corresponding code value $X_{0, N}$. After testing all the capacitors, the final correction codes $X_N$ are calculated and stored accordingly.

3.2. Analog-to-digital conversion

During subsequent normal conversion cycles, the calibration mode is disengaged. Firstly, for the main array, P side samples positive input voltage, N side samples negative input voltage. The top plate of all capacitors connects to $V_{CM}$. Meanwhile, for P side, the top capacitor of the bypass array samples $V_{REF}$, other capacitors sample ground. For N side, the operation is complementary. The initial code “100…00” is the median value of the whole range which can be represented by the bypass array. The inputs of the main array are then disconnected from the bottom plates. Afterwards is the normal analog-to-digital conversion. Put the correction code in the bypass array. Set the code of the main array as “100…00” before start, too. During conversion, if the bit decision is 1, add the corresponding error code of the bit to the bypass array to compensate for the mismatch. Otherwise, the code is dropped, leaving the bypass array with the previous result.

4. Simulated results

To verify the correction algorithm, use MATLAB to simulate every step in the normal analog-to-digital conversion according to the flowchart shown in Figure 3.

The ratio error of each capacitor in the main array is around two thousandths due to process or other reasons. Set the mismatches of each capacitor artificially, supposing the ratio error of $C_1 ~ C_{15}$ is [0 0 0 0 0 0 0 -0.001 0 0 0.002 0 0 0.003 0.004]. The differential input voltages have linear change from 0V to 2.5V and 2.5V to 0V. Take a point every 0.005V for high accuracy.

The simulation results of SAR ADC with calibration and that without calibration are listed below. The error curve of the output voltage without calibration is shown in Figure 4. The abscissa is the conversion times, and the ordinate is the error voltage expressed by LSB. Without calibration, the error of the ADC can reach 100 LSBs in maximum. It caused great instability, which made the result meaningless.

Meanwhile, the error curve of the ADC’s output after calibration is shown in Figure 5. Compared to the previous one, the error after calibration is fluctuated in a small range between ±0.5 LSB roughly. The output has little deviation from the input, which can be dozens of microvolts. It means that the correction algorithm improves the accuracy of the final result effectively. Therefore, the accuracy of the final result increased a lot, which contributes to a higher linearity performance.

In addition to the linear function, we consider the sinusoid function of input signal and simulate the output of the ADC similarly. Set the differential input voltage as a sinusoid function around 1.25V and then convert the output of the ADC to analog domain through an ideal DAC. The results of the input voltage and output voltage without calibration are showed in Figure 6. The orange curve represents the difference input voltage ($V_1-V_2$), and the blue * represents the output voltage of the DAC. To make a clear comparison, zoom in the curve with a certain part, as shown in Figure 7. The output voltage of ADC without calibration is far away from the input voltage.

Similarly, with the same operation as before, the two curves with calibration are depicted in the Figure 8. The enlarged curves are shown in Figure 9. After applying the digital calibration algorithm, the output voltage of the DAC is almost the same as the input voltage. It can be proved that the algorithm enhances the accuracy of SAR ADC significantly.

5. Conclusion

In this paper, a 15-bit SAR ADC with on-chip digital calibration is proposed. After calibration, the offset of the comparator is cancelled. In addition, the mismatches of each capacitor in the main array is calculated by the added bypass array and stored in the register. During conventional analog-to-digital conversion, the pre-stored error code is used to compensate for the mismatches of capacitors in real time to achieve high-precision output. Verified by MATLAB, the ratio errors of the capacitor array
could be corrected into 1 LSB. In conclusion, the proposed algorithm can increase the precision of the SAR ADC significantly.

6. References

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