The digital controller for power supplies in HIAF

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Abstract. High Intensity Heavy Ion Accelerator Facility (HIAF) project has been proposed by Institute of Modern Physics, Chinese Academy of Sciences (IMP) for high power heavy ion researches. Due to the unique requirements of the Booster Ring (Bring) in HIAF, a digital controller is used as the controlling system of power supplies to achieve high performances. This paper explains the hardware and software architecture of the digital controller. It uses Cyclone V SX SoC FPGA which integrates dual-core ARM Cortex-A9 MP Core processor. The controller consists of high precision ADC, DAC, optical fibre modules, DDR3 SDRAM and Gigabit Ethernet modules. The PI regulation and PWM modulation have been realized in FPGA. The data pre-setting, web service, database, power supplies detection and protection management have been established in ARM. Finally, the results of prototype output measurements prove that this design is feasible and qualified.

1. Introduction
HIAF [1] is a new facility for heavy ion researches [2], which consists of two ion sources, a high intensity Heavy Ion Superconducting Linac (HISCL), a 45 Tm Accumulation and Booster Ring (ABR-45), and a multifunction storage ring system. Due to the Booster Ring has high quality requirement for beam, the digital controller of power supplies for magnets should have good tracking performance, high stability and small output error. This paper presents a controller designed for the Booster Ring dipole power supplies to achieve the requirements mentioned above.

2. Hardware architecture
The hardware of the controller is described in this section. Some papers have proposed a concept of a new controller [3] using Raspberry Pi and Field Programmable Gate Array (FPGA), which demonstrates the use of Advanced RISC Machines (ARM) and FPGA in accelerator power supplies area. Further, SoC FPGA, which integrates ARM and FPGA architectures into a single device, is used in this design, and it makes the controller more simplified than the above one [3]. The resource of an old generation FPGA is compared with SoC FPGA to illustrate the superiority of this design.

2.1. Chip selecting
The controller uses Cyclone V SX SoC FPGA, which has the main performance as: Hard memory controllers supporting 400 MHz DDR3 SDRAM with optional error correction code (ECC) support,
PCI Express with multifunction support, variable-precision digital signal processing (DSP) blocks, and HPS Dual-core ARM Cortex-A9 MP Core processor. There are rich peripherals such as DDR3 SDRAM, FLASH, fiber optic 88e1111, and Ethernet modules in the controller. Comparing the previous works [4], the main chip of the power supplies controller was usually Cyclone II FPGA EP2C70. The differences of resources between two FPGAs are listed in table 1. The upgraded FPGA improves the calculation speed of the controller because of the usage of DSP blocks and more multipliers.

| Items          | Cyclone V | Cyclone II |
|----------------|-----------|------------|
| Logic elements | 110,000   | 68,416     |
| Pins           | 499       | 422        |
| Memory bits    | 5,662,720 | 1,152,000  |
| DSP blocks     | 112       | /          |
| Multipliers    | 224       | 150        |
| Total PLLs     | 15        | 4          |

2.2. **Main Boards**

Figure 1 shows that the controller consists of a main board, mother board, ADC board, extended board, and PLC board. The high-speed serial transceiver GXB plays an important role in communicating with all these boards. In addition, this controller also adopts industrial protocol such as RS232, RS485, and CAN. Except for the boards mentioned above, the old controller [4] included an MCU board and a power board. Without the redundant boards, the controlling system is more reliable.

![Figure 1](image_url)

**Figure 1.** The photos of the power supplies controller. (a) Main board and mother board. (b) ADC board. (c) Combination of main board, mother board, ADC board and extended board. (d) Combination of DAC board, main board, mother board, PLC board, ADC board and extended board.

3. **Software architecture**

The software architecture of controller consists of the FPGA part and the ARM part. The FPGA part has been used for parallel calculation, and the ARM part has been used for task scheduling based on embedded real-time Linux operating system.

3.1. **FPGA Part**

The controller has current closed-loop control based on DCCT and ADC circuits. The PI regulation and PWM modulation are completed in FPGA. Some states such as the overcurrent fault, the overvoltage fault and the interlock fault are collected and processed in FPGA. In addition, the greater memory bits resources (table 1) make storage be more convenient.

3.2. **ARM Part**

Data pre-setting, web service, database, power supplies detection and protection management have been constructed in ARM. The controller adopts White Rabbit timing System due to real-time analysis. All the read-back data have timestamp which is convenient for the physicist to regulate beam. The
ARM part is used to run an embedded real-time Linux operating system. Compared to the old controller, it makes full use of Linux, and gives up the shortages of uC/OS II [4].

3.3. The Communication Between FPGA and ARM
The Hard Processor System (HPS, also called ARM) and FPGA communicate with each other through high bandwidth communication called Advanced eXtensible Interface (AXI). There are three bridges between HPS and FPGA based on AXI, called FPGA-to-HPS Bridge, HPS-to-FPGA Bridge, and Lightweight HPS-to-FPGA Bridge. HPS-to-FPGA Bridge is used to transmit pre-setting data from ARM to FPGA. Lightweight HPS-to-FPGA Bridge is used to transmit PIO signals to synchronize the time sequence. Besides, FPGA-to-HPS Bridge is used to pass read-back data from FPGA to ARM DDR3 SDRAM.

![Figure 2. Pre-set data transmission flow.](image)

![Figure 3. Read-back data transmission flow.](image)

The details about the pre-set data transmission are listed in figure 2. The waveform data is saved in the FLASH or SD card in the ARM part after being received. When the change-wave menu is on, the synchronous trigger module sends a signal in the waveform type through PIO, then the pre-set data, the wave length and the area flag are sent to FPGA. When the output-begin menu is on, the digital regulator is ready to work in FPGA based on the pre-set data.

![Figure 4. The testing photos. (a)The power supplies prototype. (b)The dipole magnets load, output current measurement on oscilloscope and the Human Machine Interface on PC.](image)
The read-back data transmission flow is shown in figure 3. There is a timer in ARM for reading the states of power supplies, the current and voltages value from the corresponding register in FPGA. After allocating the respective memory, a physical address and read-finished flag are sent from ARM to FPGA through the PIO. Based on this address and flag, the read-back data is written to the HPS DDR3 SDRAM. After processing the signal, the read-back data is saved in the database, FLASH, SD card or shown in the Human Machine Interface (HMI).

4. Result
The testing photos are shown in figure 4. In this experiment, power supplies prototype is single H bridge and its loads are dipole magnets. The maximum output of this prototype is 600A. The power supply that used this controller are tested in the pulse mode for 8 hours (figure 5). Similarly, the power supply in the direct current (DC) mode has also been tested for 8 hours (figure 6).

![Figure 5. Oscilloscope screenshot of output current in pulse mode.](image)

![Figure 6. Oscilloscope screenshot of output current in DC mode.](image)

In order to analyze this result, some read-back data stored in the SD card is extracted for further study. Figure 7 and 8 show output results based on the pre-set, output current and the error data. Due to a current closed-loop control based on the PI regulation in the controller, A good tracking performance has achieved. Figure 7 (a) shows output current is about 5ms slower than the pre-set current. Figure 8 (a) shows the relative stability of Direct Current (DC) operation mode is 4.6e-4 and it can be calculated in equation (1). Figure 7 (b) shows the maximum absolute error of pulse mode is 1.27602A and the calculation is shown in equation (2). Figure 8 (b) shows the maximum absolute error of the DC mode is 0.008135A and the calculation is shown in equation (3). Eventually, we can conclude that the design of the controller is qualified to the power supplies of HIAF Bring.

![Figure 7. Output data of power supply in pulse mode (only one cycle is shown). (a) The comparison between pre-set and output current data. (b) The error data between pre-set and output current.](image)
Figure 8. Output data of power supply in DC mode (only one cycle is shown). (a) The comparison between pre-set and output current data. (b) The error data between pre-set and output current.

RelativeStability = \frac{15.007006 - 14.993265}{15.007006 + 14.993265} = 4.6e^{-4} \quad (1)

AbsoluteError = 0.70566 - (-0.57036) = 1.27602A \quad (2)

AbsoluteError = 0.004265 - (-0.00387) = 0.008135A \quad (3)

5. Conclusions
In order to have a good tracking performance, high stability and small tracking error in the power supplies of HIAF Bring, a digital controller based on SoC FPGA is proposed in this paper. This work has realized a new design of using a SoC FPGA controller in accelerator power supplies field and makes full use of AXI between FPGA and ARM for communication. Finally, the results of testing the single H bridge prototype verify the feasibility of this controller.

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