LETTER

Optimizing read disturb phenomenon with new read scheme by partial-boosting channel in 3-D NAND Flash memories

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Abstract In 3D NAND Flash, new read operation scheme is proposed to optimize read disturb in unselected strings. During read operation, the two types of read disturb occur, which are soft programming and HCI-induced read disturb. These are caused by repetitive Fowler-Nordheim (F-N) stress and boosting channel potential difference, respectively. In this letter, we show optimization of two read disturb phenomena through technology computer-aided design (TCAD) simulation with partial-boosting channel potential. Furthermore, the various conditions that affect channel potential in read operation are investigated. These results will be basis of the practical 3D NAND read operation analysis.

key words: 3D NAND Flash, new read scheme, read disturb, hot carrier injection, partial boosting channel, optimization
Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

The non-volatile memory market has grown significantly due to demand for massive amounts of data storage. In particular, NAND Flash memory is widely used as a non-volatile memory in the market. For low bit cost and high density, NAND Flash memory has been scaling down continuously. However, Reliability issue and increased process cost make it difficult. Therefore, structure with the 3-D vertical channel and stacked Word-lines (WLs) was applied to the NAND Flash memory and the number of string/BL is increased [1, 2, 3, 4, 5]. This structure caused phenomenon different from soft programming such as hot-carrier injection (HCI) induced read disturb in unselected strings [6,7].

In conventional read operation, soft programming occurs by repeated F-N stress in unselected WLs of selected string [8]. In addition, it has been reported that HCI-induced read disturb occurs by boosting channel potential difference in unselected string. To be more specific, in unselected strings, select gates are turned off to prevent unwanted sensing and soft programming (see Fig. 2(b) ‘Conventional 1’) but it's boosting channel potential occurs large electric field between selected WL and unselected WL when verify voltage is applied. The large electric field causes band-to-band tunneling (BTBT), where electron-hole pairs are generated. Some electrons are accelerated in the spacer region and become hot carriers, which makes a large shift of threshold voltage ($V_{th}$) in two neighbor WLs [9,10]. Many efforts have been made to solve this HCI-induced read disturb [6, 11, 12]. For example, drain select line (DSL) and source select line (SSL) are turned on for long time with high voltage to make lower channel potential difference than conventional read operation (see Fig. 2(b) ‘Conventional 2’). However, this scheme induces new problem such as more severe soft programming [13,14]. For this reason, ‘Conventional 3’ was recently proposed to improve read/write performance and soft programming, but there is no specific physical analysis [15]. Therefore, we performed physical-based TCAD device simulation and proposed new read schemes based on ‘Conventional 3’ [16]. Then, we analyzed the factors affecting the channel potential and show applicability of ‘Proposed’ in various conditions to optimize read disturb.

2. Device structure for TCAD simulation

Fig. 1. Schematic cross section of p-BiCS structure used in the TCAD simulation.

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Fig. 1 shows the schematic cross section of pipe-shaped bit cost scalable (p-BiCS) device structure [17,18,19]. A NAND string has three DSL/SSL, two dummy WLS and 48 cells. For the sake of simplicity in simulation, the monocrystalline channel is assumed. Table I summarizes device parameter values used in TCAD simulation. The meaning of parameters is as follows: \( r_f \) is the filler oxide radius, \( t_ox, t_{si}/t_{ox}, t_{si}/t_{ox} \) are thickness of silicon channel, tunnel oxide/silicon nitride/oxide in order, and \( L_WL \) is cell gate length, \( L_SP \) is spacer length, and \( N_D^{BL, SL} \) and \( N_D^{ch} \) are the donor doping concentrations of the bit line, source line, and channel body, respectively. \( n_{CNT} \) and \( p_{CNT} \) are electron, hole nitride trap charge density [20].

To simulate the worst case of HCI-induced read disturb, all WLS are erased (\( V_i = -1.1V \)) and only select WL is programmed to PV7 (\( V_i = 4.5V \)) and the verify voltage is 0V to selected WL (\( V_{\text{verify}} = 0V \)), which makes maximum electric field between selected WL and neighbor cells in unselected strings.

| Parameter          | Value          |
|--------------------|----------------|
| \( r_f \)          | 15 nm          |
| \( t_ox \)         | 10 nm          |
| \( L_{亏/透/透} \)  | 5/5.6 nm       |
| \( L_WL = L_{SP} \)| 28 nm          |
| \( N_D^{BL} \)     | \( 5 \times 10^{10} \) cm\(^{-3} \) |
| \( N_D^{SL} \)     | \( 1 \times 10^{11} \) cm\(^{-3} \) |
| \( n_{CNT} = p_{CNT} \) | \( 5 \times 10^{15} \) cm\(^{-3} \) |

3. New read scheme in unselected strings

![Diagram](image)

**Fig. 2.** (a) Common bias in unselected string and only DSL/SSL bias is different. (b) Conventional 1: DSL/SSL are turned off and Conventional 2: DSL/SSL are fully turned on, Conventional 3: DSL/SSL are turned on slightly at unselected WL rising edge and Proposed: delayed pulse of ‘Conventional 3’.

Fig. 2 shows read operation schemes in unselected string. The BL and SL are biased to pre-charged voltage (\( V_{\text{pre}} = 0.5V \)) and ground, respectively. The read pass voltage (\( V_{\text{pass}} = 6.5V \)) is applied to unselected WLS. As previously mentioned, ‘Conventional 1–3’ have been proposed to improve read disturb. In this letter, the triangular pulse (Constant slope: 6.5 V/\( \mu \)s) is used to ‘Conventional 3’ and ‘Proposed’. As \( V_{\text{peak}} \) increases, the time of DSL/SSL pulse also increased. First, We will compare ‘Conventional 1–3’, then show how it differs from ‘Proposed’.

4. Results and Discussion

4.1 Effects of read operation schemes
To figure out the effect of schemes, we check the channel potential, electron density, electric field and current density of HCI at t = 3μs when maximum HCI-induce read disturb occurred. Fig. 3(a) shows channel potential with ‘Conventional 1~3’ (assume selected WL is in the middle). In ‘Conventional 3’, V_{peak} changes in order to observe the extent to which the channel potential decreases. First, for read operation with ‘Conventional 1’, the channel potential is fully boosted by read pass voltage and this scheme causes unwanted HCI-induced read disturb. Second, the channel potential by ‘Conventional 2’ is low and potential difference is also decreased. Even if the higher voltage is applied, the channel potential does not decrease anymore (so-called ‘saturation state’). Third, in read operation with ‘Conventional 3’, the channel potential decrease starts to occur when the V_{peak} is over 0.5V (because V_{th} of 3 DSL/SSL is 0.5V) and then, when V_{peak} is over 3.7V, the channel potential becomes ‘saturation state’.

Fig. 3(b)~(d) show electron density, electric field and current density of HCI with ‘Conventional 1~3’, respectively. In particular, Fig. 3(b) shows the reason why the channel potential decreases when DSL/SSL are turned on. The electrons from high doped SL and BL are injected and the higher the V_{peak}, the more amount of electrons remain in the channel. In ‘Conventional 3’, the channel potential is partially boosted and channel boosting level can be chosen by adjusting V_{peak}, and at the same time, electric field and current density of HCI should be considered as shown in Fig. 3(c) and (d).

Based on this ‘Conventional 3’ analysis, we proposed a new read scheme ‘Proposed’ and this pulse is delayed pulse of ‘Conventional 3’ by t_{delay}. Fig. 4 shows the effect of ‘Proposed’. Although same V_{peak} pulse was used, as the t_{delay} increases, channel injected electrons are increased the channel potential decreases and as shown in Fig. 4(a) and (b). Additionally, maximum electric field and current density of HCI are also decreased as shown in Fig. 4(c) and (d).

Through the results of Fig. 3 and 4, ‘Proposed’ is more effective than ‘Conventional 3’ in reducing the channel potential and HCI-induced read disturb because DSL/SSL starts to turn on when the unselected WLs bias is higher. Instead of applying a high voltage to the DSL/SSL, it is possible to optimize the channel potential by adjusting the delay time.
4-2 Investigation of channel potential

Fig. 5 shows channel potential depending on select WL location with ‘Proposed’. All conditions are the same as in Fig. 4, except that the select WL is close to the SL side. We can explain this tendency through electron density that is the reason for the decrease of channel potential. From the selected WL, channel volume of the BL side is larger than that on the SL side, and more electrons are required to decrease the channel potential. As a result, the channel potential on the BL side decreased less than when the select WL was near in the middle. On the contrary, SL side channel potential is further decreased. This result shows that selected WL location should be considered for read disturb optimization.

In this letter, the same pulse is applied to DSL and SSL in all read schemes. However, the channel potential of BL side and SL side can be controlled independently by applying ‘Proposed’. In Fig. 6, the DSL/SSL are applied to same $V_{peak} = 2V$ and $t_{delay,SSL} = 0.1\mu s$ and fixed, then $t_{delay,DSL}$ changes 0.15μs, 0.2μs and 0.25μs. The SL side channel potential is same in each pulse and only BL side channel potential is changed by $t_{delay,DSL}$. It means that we can handle channel potential both side independently and control soft programming and HCI for optimization. This read scheme can be applied considering Fig. 5, but only tendency was explained simply in here.

As previously mentioned, the WL layer stack is increasing for low bit cost and high density, which affect channel potential when DSL/SSL are turned on. For this reason, we show WL layer dependency in Fig. 7. As the WL layer increases, the channel potential decreases less because the volume of the channel to be filled with electrons increases. However, one thing to consider when we see this figure is that all WLs are erased except for selected WL. In practical 3D NAND operation, all WLs are programmed randomly and injection of electrons is difficult in low $V_{pass}$. For this reason, the difference of channel potential in Fig. 7 is not significant, but we can check tendency of channel potential depending on the number of WL layer. In practical 3D NAND operation, channel potential changes according to various conditions such as random cell pattern, and the soft programming and HCI will be affected [26, 27, 28, 29, 30]. Therefore, more research is needed to reduce read disturb, and we laid the groundwork in this study.

5. Conclusion

In this letter, we investigated various read schemes to optimize two different read disturb phenomena in 3D NAND Flash memories. Based on results, we proposed new read scheme with partial-boosting channel in unselected string. It is observed that channel potential and current
density of HCI can be optimized by adjusting the delay time and peak voltage of DSL/SSL pulse. Then, some factors that affect channel potential are investigated and the applicability of DSL/SSL pulse was also presented. These results will be basis of the practical 3D NAND read operation analysis.

Fig. 7 The channel potential depending on the number of WL layer with same read scheme.

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