Fast and Scalable Memristive In-Memory Sorting
with Column-Skipping Algorithm

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Abstract—Memristive in-memory sorting has been proposed recently to improve hardware sorting efficiency. Using iterative in-memory min computations, data movements between memory and external processing units can be eliminated for improved latency and energy efficiency. However, the bit-traversal algorithm to search the min requires a large number of column reads on memristive memory. In this work, we propose a column-skipping algorithm with help of a near-memory circuit. Redundant column reads can be skipped based on recorded states for improved latency and hardware efficiency. To enhance the scalability, we develop a multi-bank management that enables column-skipping for dataset stored in different memristive memory banks. Prototype column-skipping sorters are implemented with a 1T1R memristive memory in 40nm CMOS technology. Experimented on a variety of sorting datasets, the length-1024 32-bit column-skipping sorter with state recording of 2 demonstrates up to 4.08× speedup, 3.14× area efficiency and 3.39× energy efficiency, respectively, over the latest memristive in-memory sorting.

Index Terms—In-memory sorting, column-skipping, memristive memory, multi-bank management

I. INTRODUCTION

The past decade has witnessed an explosive growth of data and the needs for high-speed data processing. A large-scale data often needs to be sorted to enable higher efficiency. Sorting is a key kernel in many applications such as data mining [1], robotics [2] and machine learning [3]. To efficiently sort an array into an order, numerous sorting algorithms have been invented in the past, such as merge-sort [4] or quick-sort [5]. These algorithms can be accelerated using CPUs/GPUs [6], FPGAs [7]–[12] and ASICs [13]–[15]. However, transferring data between memory and external processing units incurs a long latency and a degraded energy efficiency. Techniques like memory management [16] have been developed to minimize the data movement, but such optimizations do not fundamentally solve the problem.

Memristive in-memory sorting [17], [18] have been proposed recently to tackle this challenge. Memristor-aided logic is developed in [17] to implement compare-and-select blocks in memory. However, a large number of memristor cells are used to implement logic gates with frequent write operations, resulting in a low memory density and a degraded device lifetime. The latest memristive in-memory sorting [18] uses iterative in-memory min computations with help of a near-memory circuit. The min values are searched by traversing each bit column using column reads (CR) on a 1T1R memristive memory. Frequent write operations in [17] are eliminated; however, the number of CRs is proportional to the number of 1T1R cells in the memristive memory, degrading the latency and energy efficiency.

In this work, we propose a column-skipping algorithm to minimize the number of CRs for improved sorting speed and hardware efficiency. A near-memory circuit is designed to keep track the column read conditions and skip those that are leading 0’s or have been processed previously. A multi-bank management is developed to enhance the scalability when sorting a larger array stored in different memristive memory banks. Implemented in a 40nm CMOS technology with 1T1R memristive memory and experimented on a variety of sorting datasets, the length-1024 32-bit column-skipping memristive sorter with state recording of 2 demonstrates up to 4.08× speedup, 3.14× area efficiency and 3.39× energy efficiency, respectively, over the latest memristive in-memory sorting implementation [18].

II. BACKGROUND

A. Sorting Applications

Sorting is a known bottleneck for many applications [1]–[5]. Here we briefly introduce two representative applications where sorting dominates the execution time: 1) Kruskal’s algorithm for minimum spanning tree (MST). In Kruskal’s algorithm, all the graph edges need to be sorted from low weight to high weight. Majority of the weights are small numbers with frequent repetitions; 2) MapReduce in distributed systems. In MapReduce, maps need to be sorted before transferring to the reducer stage [19]. These maps are typically clustered in a few groups. We use datasets generated from these two applications for benchmarking in Section V.

B. Memristive In-Memory Sorting

Iterative in-memory min computation is proposed in [18] for memristive in-memory sorting. It uses $N$ iterations to successively search and exclude the min values in a length-$N$ array. Suppose each memristor cell stores a bit in a 1T1R memristive memory. Fig. 1 shows an example for a length-$N$ ($N = 3$) array of $w$-bit ($w = 4$) numbers, $\{8, 9, 10\}$.

In each iteration, a $w$-step bit traversal algorithm searches the min value: at step $j$ ($j = w − 1 \rightarrow 0$), a near-memory circuit reads an bit column corresponding to the $j$-th bits of
all array elements, searches for 1’s in that bit column, and
eclude the rows that have 1’s. When a bit column contains
all 0’s or 1’s, the row exclusion can be skipped. Rows that
are corresponding to non-minimum values are excluded step
by step until the min value is reached. The row for the min
value is then excluded and marked as sorted before moving
to the next min search iteration. The near-memory circuit is
designed to support two operations, column read (CR) and
row exclusion (RE), and their associated control logic. Fig. 1
shows the steps to sort \{8,9,10\} using memristive in-memory
sorting [18]. Note that the near-memory circuit in [18] does
not keep track the number of remaining elements in the array;
therefore it takes \( N = 3 \) iterations of min search, each contains
\( w = 4 \) CRs. The total sorting latency is \( N \times w = 12 \) CRs.

III. COLUMN-SKIPPING MEMRISTIVE IN-MEMORY
SORTING

We observe that memristive in-memory sorting in [18]
introduces a large number of redundant CRs which are re-
peatedly executed on leading 0’s or bit columns that have been
processed previously. As shown in Fig. 1 when searching the
2nd minimum number 9, the first 3 CRs have been processed in
the 1st iteration and are repeated in the 2nd iteration. To
efficiently skip these redundant CRs, we propose a low-
latency column-skipping algorithm. We use unsigned fixed-
point number as example, but it can easily be applicable to
signed fixed-point and floating-point number formats with
small changes as described in [18].

A. Low-Latency Column-Skipping Algorithm

Redundant CRs can happen in two scenarios: 1) array
elements may include leading 0’s. CRs on these leading 0’s
are skipped at the beginning of each iteration; 2) some CRs
may have been processed previously for REs, i.e., we do not
need to exclude any new rows for those bit columns.

To detect and skip the redundant CRs, we propose to record
the \( k \) most recent RE states and their corresponding column
indexes. The recorded states can be reloaded to skip redundant
CRs. Fig. 2 summarizes the iterative min computation for a
length-\( N \) array with proposed column skipping algorithm
(where \( n = 1 \rightarrow N \)): 1) if state records are empty, the
\( w \)-step algorithm [18] traverses each bit column from LSB
(\( i = 0 \)), \( k \) most recent RE states whose bit columns are not all 0’s or 1’s and their corresponding column indexes are stored in a state controller; 2) if state

records are non-empty, we reload the most recent RE state
and the corresponding column index \( s \) and start from the next
bit column \( s - 1 \). CRs are executed on subsequent bit columns
until reaching the min value.

Fig. 3 illustrates the proposed column-skipping algorithm
with state recording \( k = 2 \) when sorting the 4-bit array
\{8,9,10\}. State recording in the first iteration helps to skip the
first 3 CRs in searching the 2nd minimum and the first 2 CRs
in searching the 3rd minimum. The total latency is reduced to
only 7 CRs. The selection of \( k \) affects the performance of the
proposed column-skipping algorithm. We study the impacts of
\( k \) on sorting speedup, silicon area and power consumption in
Section V.

B. Near-Memory Circuit for Column-Skipping

Fig. 4 demonstrates the near-memory circuit connected to a
1T1R memristive memory to implement the proposed column-
skipping algorithm. The 1T1R memristive memory stores the
binary bits of array elements with MSB on the leftmost column. Similar to [18], select lines with sense amplifiers
and bitline drivers are used for column reads. The proposed
near-memory circuit consists of three modules: 1) a column
processor that controls the column states; 2) a row processor
that controls wordline (or RE) states; 3) a state controller that
stores the RE states and their corresponding column indexes
using a \( k \)-entry table. It also controls signals to execute all the
operations.
The near-memory circuit supports the four operations in Fig. 2 as following: 1) column read (CR), where the column processor enables the bitline driver of a column and the corresponding bit column is read to the row processor. The column controller generates the next-step column state and the enable signal for column update (cen). Sense amplifiers measure the current on each select line to determine if it’s 0 or 1: 2) row exclusion (RE), where the row processor checks if the bit column are all 0’s or 1’s (through row controller) before updating the wordlines (or RE) states. The row controller generates the enable signal for wordline update (ren). The wordlines that are connected to 1’s are excluded and set to 0; 3) state recording (SR), where RE states and their corresponding column indexes are stored in a k-entry table. The recording is enabled (sen) if an iteration starts from the MSB and the bit column is not all 0’s or 1’s; and 4) state loading (SL), where the most recent RE state and the corresponding column index are sent to the row processor and column processor, respectively. The load enable signal (len) selects the reloaded states when updating the wordline and column registers. A top-level controller is used to schedule the four operations.

When multiple rows remain unexcluded at the end of an iteration due to repetitions in the array, the column processor stalls to avoid redundant CRs until all repetition elements are excluded successively in the row processor.

IV. MULTI-BANK MANAGEMENT

The near-memory circuit shown in Fig. 4 can be scaled up to support larger array (i.e., larger N) or higher precision (i.e., large w). However, practical array can be too big to fit in a single memristive memory. To solve this problem, we propose a scalable solution to sort larger array stored in multi-bank memristive memory.

Suppose a length-N array is stored in C-bank memristive memory, each bank stores N/C elements and has its own near-memory circuit that forms a length-N/C sub-sorter. To realize length-N sorting using C sub-sorters of length-N/C, sub-sorters’ operations need to be synchronized and run as a whole. A multi-bank manager is designed to connect the sub-sorters for this synchronization purpose: the judgement about all 0’s or 1’s needs to be considered globally to synchronize RE and SR operations while CR and SL operations are synchronized through the OR gates.

Fig. 5 shows the multi-bank manager to generate synchronization operation bits en-sync for local operation bits en_i from sub-sorter i, where i ∈ [1, C]. In each sub-sorter, the synchronized operation bits en_sync are used for replacing the original signals (en_i) to realize the corresponding function. The multi-bank manager monitors the sub-sorters’ states and select the output from one of the C sub-sorters if existing repetitions. Performance of the proposed multi-bank management are evaluated in Section V.

V. EVALUATION AND BENCHMARKING

We evaluate the proposed techniques using statistically distributed datasets (uniform, normal and clustered) and practical datasets (from Kruskal’s and MapReduce). We use 32-bit precision: the uniform distribution ranges from 0 to 2^{32} − 1, the normal distribution has a mean of 2^{31} and a standard deviation of 2^{31}/3, and the clustered distribution has 2 clusters centered at 2^{15} and 2^{25} with identical standard deviation of 2^{13}. To estimate the silicon area and power consumption, prototype sorters of length-1024 are implemented with ITIR memristive memory using a 40nm CMOS technology. The RRAM device has two states and the corresponding resistances are 10MΩ and 100kΩ, respectively. State-of-the-art memristive in-memory sorter [18] (baseline) and conventional digital merge sorter are implemented for comparison. All prototype sorters run at a 500MHz clock frequency.

A. Sorting Speedup

The baseline implementation [18] has a fixed sorting speed of 32 cycles per number for any datasets. The merge sorter outperforms the baseline by 3.2× in speed. The speed of column-skipping sorter depends on parameter k and dataset distribution. Fig. 6 shows the normalized speedup over the baseline on the selected datasets with N = 1024, w = 32 and varying state recording k. When k increases, the min search is more likely to start from a recorded RE state; however, the
reloaded starting position (s in Fig. 2) may be further away from the optimal starting position, degrading the speedup due to less number of skipped CRs. We observe that the speedup saturates when \( k \) reaches 2 or 3 and then goes down across selected datasets.

The proposed column-skipping algorithm achieves faster sorting speed (up to \( 2.22 \times \) over the baseline) on clustered dataset than the speedup on uniformly or normally distributed datasets (up to \( 1.21 \times \) and \( 1.23 \times \) over the baseline, respectively). This is because clustered elements with small centers signify more leading 0’s and redundant CRs. In Kruskal’s and MapReduce dataset, majority of the small and repetitive elements lead to much better results for a speedup up to \( 3.46 \times \) and \( 4.16 \times \) over the baseline, respectively.

\section{Area and Energy Efficiency}

With \( N = 1024 \) and \( w = 32 \), the baseline sorter occupies 77.8K \( \mu \)m\(^2\) in silicon while the merge sorter occupies 246.1K \( \mu \)m\(^2\). The merge sorter demonstrates 1.01\times area efficiency (throughput/area) over the baseline. We further measure the areas of column-skipping sorters with varying state recording \( k \). Fig. 7 presents the normalized area and area efficiency over the baseline when sorting the MapReduce dataset. With \( k = 1 \), column-skipping sorter demonstrates more than 3.2\times area efficiency over the baseline. When \( k \) increases, the sorter area increases due to larger state controller to store more RE states; however, the area efficiency goes down, because the speedup starts saturating when \( k \) reaches 2 or 3.

We measured power using Ansys PowerArtist considering switching activities when sorting MapReduce dataset. The baseline sorter and the merge sorter consume 319.7 mW and 825.9 mW, respectively. The merge sorter demonstrates 1.24\times energy efficiency (throughput/power) over the baseline. Column-skipping sorter consumes more power with increasing \( k \), but the energy efficiency reaches the peak at \( k = 2 \) as shown in Fig. 7, outperforming the baseline by 3.39\times. The area and power consumption of 1T1R array are orders of magnitude less than the near-memory circuit. One can select the parameter \( k \) based on target dataset for optimized speed, area and energy efficiency.

\section{C. Multi-Bank Management}

To evaluate multi-bank management, we build a column-skipping sorter of \( N = 1024 \) using sub-sorters of length \( N_s = 64, 256, 512 \). Multi-bank management does not change the speedup brought by column-skipping when clock frequency remains unchanged. Further reducing the sub-sorter length results in a degraded clock frequency under 500MHz due to more complex multi-bank manager. Fig. 8(a) demonstrates the normalized area and power of multi-bank management over the original \( N = 1024 \) sorter. We observe that the area and power of the near-memory circuit in sub-sorters decreases super-linearly when \( N_s \) decreases. Even with an extra multi-bank manager, the total area and power for multi-bank management goes down with smaller sub-sorter length. Using 16 sub-sorters of length \( N_s = 64 \), the area and power reduction can be up to 14\% and 9\% compared to the original \( N = 1024 \) sorter. Fig. 8(b) summarizes the implementation results for different sorters.

\section{VI. Conclusions}

We present a fast and scalable memristive in-memory sorting that employs a column-skipping algorithm and a multi-bank management. Near-memory circuit with state recording is designed to efficiently skip redundant column reads for improved sorting speed and hardware efficiency. The multi-bank manager enables column-skipping for dataset stored in different banks of memristive memory. Prototype sorters are implemented using 40nm CMOS technology and 1T1R memristive memory. Experimented on a variety of sorting datasets with array length-1024, data precision 32-bit and state recording of 2, the speed, area efficiency and energy efficiency are 4.08\times, 3.14\times and 3.39\times, respectively, than the state-of-the-art memristive in-memory sorting.
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