Sparse LMS algorithm for two-level DSTATCOM

Mrutyunjaya Mangaraj1 | Anup Kumar Panda2

1 Lendi Institute of Engineering and Technology, Vizianagaram, Andhra Pradesh 535005, India
2 National Institute of Technology, Rourkela, Odisha 769008, India

Abstract
Sparse least mean square algorithm is proposed for the DSTATCOM as an optimal current harmonic extractor to cope with the intermittent nature of loadings. Sparse least mean square is the improved version of adaptive least mean square learning mechanism with regards to sparsity. This innovative approach is utilized for better parameter estimation due to its algorithmic simplicity and parallel computing nature. Hence, sparse least mean square is expected to reduce the computation and storage requirements significantly. This suggested controller consists of six subnets. Three subnets for active and another three for reactive weight component are used to extract the fundamental component of the load current. Several factors like previous weight, normalizing weight and learning rate are involved in the sparse least mean square based weight-updating rule to have better dynamic performance, reduced computational burden and better estimation speed etc. The detailed control algorithm is formulated using MATLAB/Simulink, and validated using experimental analysis. Among these two algorithms, the sparse least mean square offers better voltage regulation, voltage balancing, source current harmonic reduction and power factor correction under various loading scenarios.

1 INTRODUCTION
With the various involvements of traction system, Renewable energy sources (RES), electric vehicle (EV) charging station and other nonlinear loads in the distribution system; Distribution Flexible AC Transmission System (d-FACTS) device is expected to deliver better power supply [1]. In fact, all these improvements are so much faster in the power industry due to the advancement of power electronics technologies [2]. But on the other way, these are the sole causes of creating several problems such as harmonics and unbalance in the supply current as well as improper regulation and unbalance in the voltage etc [2–3]. So the performances like minimisation of current harmonics and power factor improvement in the source side, voltage regulation in the DC side of Voltage Source Converter (VSC) as well as Point of Common Coupling (PCC), voltage balancing at PCC, and reduction in the sizing of VSC are most important and challenging task for such scenario. So, the research direction attains several designs and modelling of DSTATCOM in improving configuration, control structure and size in the different aspects. As a result, the power supply will be more reliable. In addition to that cost of repair and maintenance, including human intervention will lead to the economics saving [4].

Generally, DSTATCOM is most widely used as a current related reliable d-FACTS device to mitigate power quality issues [5–6]. So, keeping design consideration for different power levels, different topologies like three leg VSC-based, four leg VSC-based [7], three-leg parallel, three-leg modular, and two-leg modular of DSTATCOM was surveyed [8]. Besides topology, the performance of DSTATCOM depends upon the control algorithm.

The proposed DSTATCOM utilizes three phase three wire (3P3W) VSC topology as the main inverter circuit. The main control algorithm is used to generate the switching pulses to compensate all the power quality issues. The implementation followed by such controller is based on the mathematical procedure using MATLAB/Simulink. Additional two PI controllers are used as part of the control architecture [9]. Among these, each one is used for each respective AC and DC side to accommodate the voltage regulation. Three HCCs are used to generate the switching pulses to turn ON/OFF the devices as in the cited publications [10–12].
Several control techniques are reported to deal with the different kind of power quality issues in the cited literatures. One of the adaptive control techniques is conferred in the DSTATCOM for adjustment of internal parameter subjected to any disturbances occurs in the system [13]. An Adaptive control is designed for active power filter to tune the individual harmonic frequency using discrete frequency analysis [14]. Least mean square (LMS) algorithm is described for both amplitude and phase angle calculation [15]. A neural network technique is suggested based on convergence characteristics [16]. Several filtering methodologies are suggested by controlling the step size satisfying IEEE guidelines related to power quality issues [17]. The other techniques like filtered-X LMS algorithm [18], Voltera adaptive [19] and subspace leaky [20] are analysed with their performance. Similarly mean square error [21], variable LMS algorithm [22] and leaky adaptive techniques are reported for signal processing and conditioning with better convergence analysis [23, 24].

The problem involve in the application of neural networks are, selection of the proper size and topology of the networks. These problems become more complex in case of training very small error signal. The above discussed complexities can be abridged by implementing an improved NN with PI controller. The proposed mathematical modelling is implemented for single step size, fulfilling weight updating and normalization attributes. It aims at achieving better performance between the input and output neurons to adopt its own learning rule subjected to different parameter variations irrespective of time. This suggested algorithm is capable enough for the detection, measurement and monitoring of the signal attributes like amplitude, power factor and frequency and performs smooth operation among analog components and digital signal processor simultaneously in the real time applications.

In this paper, sparse least mean square (SLMS) algorithm is employed to extract both active and reactive components of distorted load currents. It possesses improved dynamic response, fast convergence characteristics and enhanced the optimised weight. On the other hand, other abilities like harmonic suppression, load balancing, unity power factor operation, voltage regulation are presented. The system modelling, design of control algorithms, and results discussion indicate the aptness of the DSTATCOM operation to maintain the power quality indices.

![Diagram](image-url)

**FIGURE 1** Schematic block diagram of the proposed DSTATCOM

for the realization of the DSTATCOM. These are elaborated in the different subsections.

### 3.1 ALMS control algorithm

In order to showcase the capabilility, ALMS algorithm is utilised for the operation of the control unit as shown in the Figure 2. The active updated weight of load current \( w_{pa}, w_{pb}, w_{pc} \) correspond to each phase are computed by this algorithm as follows:

\[
\begin{align*}
\hat{w}_{pa}(n+1) &= \sigma_k \gamma_k \left( i_{la}(n) - w_{pa}(n) u_{pa}(n) \right) u_{pa}(n) + w_{pa}(n) \\
\hat{w}_{pb}(n+1) &= \sigma_k \gamma_k \left( i_{lb}(n) - w_{pb}(n) u_{pb}(n) \right) u_{pb}(n) + w_{pb}(n) \\
\hat{w}_{pc}(n+1) &= \sigma_k \gamma_k \left( i_{lc}(n) - w_{pc}(n) u_{pc}(n) \right) u_{pc}(n) + w_{pc}(n)
\end{align*}
\]

\[(1)\]

Similarly, the extraction of reactive weight of load current \( w_{qa}, w_{qb}, w_{qc} \) are computed as follows:

\[
\begin{align*}
\hat{w}_{qa}(n+1) &= \sigma_k \gamma_k \left( i_{la}(n) - w_{qa}(n) u_{qa}(n) \right) u_{qa}(n) + w_{qa}(n) \\
\hat{w}_{qb}(n+1) &= \sigma_k \gamma_k \left( i_{lb}(n) - w_{qb}(n) u_{qb}(n) \right) u_{qb}(n) + w_{qb}(n)
\end{align*}
\]

\[(4)\]

### 2 SYSTEM TOPOLOGY

The proposed VSC based DSTATCOM with Electrical Distribution System (EDS) is described as follows: Source, rectifier load and DSTATCOM are chosen for three-phase three-wire (3P3W) utility. The DSTATCOM consists of six insulated gate bipolar transistors (IGBTs), a DC-link capacitor \( (C_{dc}) \) as shown in the Figure 1.

### 3 CONTROL ALGORITHMS

Two different types of neural network training algorithms like adaptive least mean square (ALMS) and SLMS are structured...
satisfying the sparse constraints. In this way, exact target sparseness is obtained. If sparsity is more, better updated weight can be achieved. Also, sparsity provides several advantages like reduction of wiring connection cost and energy consumption. The active updated weight of load current \( w_{qa}, w_{qb}, w_{qc} \) correspond to each phase are computed by this algorithm as follows:

\[
\begin{align*}
\hat{w}_{qa}(n+1) &= \mu_k c_k i_L q_a - \sigma_k \xi_k \operatorname{sgn}(w_{qa}(n)) \left[ \frac{w_{qa}(n)}{\xi_k} + \frac{w_{qa}(n)}{\xi_k} \right] + w_{qa}(n) \\
\hat{w}_{qb}(n+1) &= \mu_k c_k i_L q_b - \sigma_k \xi_k \operatorname{sgn}(w_{qb}(n)) \left[ \frac{w_{qb}(n)}{\xi_k} + \frac{w_{qb}(n)}{\xi_k} \right] + w_{qb}(n) \\
\hat{w}_{qc}(n+1) &= \mu_k c_k i_L q_c - \sigma_k \xi_k \operatorname{sgn}(w_{qc}(n)) \left[ \frac{w_{qc}(n)}{\xi_k} + \frac{w_{qc}(n)}{\xi_k} \right] + w_{qc}(n)
\end{align*}
\]

Similarly, the extraction of weighting values of fundamental reactive component of load current \( w_{qa}, w_{qb}, w_{qc} \) are computed based on proposed algorithm as follows:

\[
\begin{align*}
\hat{w}_{qa}(n+1) &= \mu_k c_k i_L q_a - \sigma_k \xi_k \operatorname{sgn}(w_{qa}(n)) \left[ \frac{w_{qa}(n)}{\xi_k} + \frac{w_{qa}(n)}{\xi_k} \right] + w_{qa}(n) \\
\hat{w}_{qb}(n+1) &= \mu_k c_k i_L q_b - \sigma_k \xi_k \operatorname{sgn}(w_{qb}(n)) \left[ \frac{w_{qb}(n)}{\xi_k} + \frac{w_{qb}(n)}{\xi_k} \right] + w_{qb}(n) \\
\hat{w}_{qc}(n+1) &= \mu_k c_k i_L q_c - \sigma_k \xi_k \operatorname{sgn}(w_{qc}(n)) \left[ \frac{w_{qc}(n)}{\xi_k} + \frac{w_{qc}(n)}{\xi_k} \right] + w_{qc}(n)
\end{align*}
\]
\begin{equation}
w_{qc}(n + 1) = \left[ \mu_ke^{\frac{1}{\tau_k}}w_{qc}(n) - \sigma_kY_k \frac{\text{sgn}\{w_{qc}(n)\}}{\xi_k} + w_{qf}(n) \right] + w_{qc}(n)
\end{equation}

### 3.3 Computation of mean value of active and reactive weighting value of the load current

The mean value \(w_p\) of the active weighting values of \(a\), \(b\) and \(c\)-phase is calculated as follows:

\begin{equation}
w_p = \frac{w_{pa} + w_{pb} + w_{pc}}{3}
\end{equation}

The mean value \(w_q\) of the reactive weighting values of \(a\), \(b\) and \(c\)-phase is calculated as follows:

\begin{equation}
w_q = \frac{w_{qa} + w_{qb} + w_{qc}}{3}
\end{equation}

### 3.4 Computation of in-phase and quadrature unit voltage template of the PCC voltage

The in-phase unit voltage templates \((u_{pa}, u_{pb}, u_{pc})\) are the relations of phase voltages & amplitude of PCC voltage \(v_t\) estimated as follows:

\begin{equation}
u_{pa} = \frac{v_a}{v_t}, \quad u_{pb} = \frac{v_b}{v_t}, \quad u_{pc} = \frac{v_c}{v_t}
\end{equation}

Similarly, the quadrature unit voltage templates \((u_{qa}, u_{qb}, u_{qc})\) are the relations of phase voltages as follows:

\begin{equation}
u_{qa} = \frac{u_{pb} + u_{pc}}{\sqrt{3}}, \quad u_{qb} = \frac{3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}}, \quad u_{qc} = \frac{-3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}}
\end{equation}

Where, \(v_t\) can be expressed as

\begin{equation}
v_t = \sqrt{\frac{2 (v_{sa}^2 + v_{sb}^2 + v_{sc}^2)}{3}}
\end{equation}

### 3.5 Estimation of active component of reference source currents

The DC voltage error \(v_{dc}\) can be achieved by subtracting sensed dc voltage from reference dc voltage and is expressed as

\begin{equation}
v_{dc} = v_{dc \left( ref \right)} - v_{dc}
\end{equation}

Where, \(v_{dc \left( ref \right)}\) is the reference DC voltage and \(v_{dc}\) is the actual DC link voltage. This difference is processed through the Proportional-Integral (PI) controller. The output of PI controller can be expressed as

\begin{equation}
w_{ip} = k_{pa}v_{dc} + k_{ia} \int v_{dc} \, dt
\end{equation}

The total active components of the reference source current are obtained by adding both output of PI controller and the average magnitude of active component of load current. It can be expressed as

\begin{equation}
w_{sp} = w_{ip} + w_{cp}
\end{equation}

### 3.6 Estimation of reactive component of reference source currents

The AC voltage error \(v_{re}\) can be achieved by subtracting sensed AC bus voltage from reference AC voltage and is expressed as

\begin{equation}
v_{re} = v_{t \left( ref \right)} - v_t
\end{equation}

Where, \(v_{t \left( ref \right)}\) is the reference AC voltage and \(v_t\) is the peak AC voltage. This difference is processed through the PI controller to maintain the constant AC bus voltage. The output of PI controller can be expressed as

\begin{equation}
w_{rq} = k_{pr}v_{re} + k_{ir} \int v_{re} \, dt
\end{equation}

The total reactive components of the reference source current are obtained by subtracting output of PI controller from the average magnitude of active component of load current. It can be expressed as

\begin{equation}
w_{sq} = w_{rq} - w_{cq}
\end{equation}

### 3.7 Estimation of triggering pattern

The instantaneous reference active component of each phase \((i_{sa}, i_{sb}, i_{sc})\) is estimated by multiplying in phase unit voltage template with active current component. These are as follows:

\begin{equation}
i_{sa} = w_{sp}u_{pa}, \quad i_{sb} = w_{sp}u_{pb}, \quad i_{sc} = w_{sp}u_{pc}
\end{equation}

Similarly, the instantaneous reference reactive component of each phase \((i_{ra}, i_{rb}, i_{rc})\) is estimated by multiplying the in-phase unit quadrature voltage template with reactive current component. These are as follows:

\begin{equation}
i_{ra} = w_{rq}u_{qa}, \quad i_{rb} = w_{rq}u_{qb}, \quad i_{rc} = w_{rq}u_{qc}
\end{equation}

The summation of active and reactive components of current \((i_{sa}, i_{sb}, i_{sc})\) is called as reference source currents and these are
obtained as

\[ i_{sa}^* = i_{sa} + i_{sb}, \quad i_{sb}^* = i_{sb} + i_{sc}, \quad i_{sc}^* = i_{sc} + i_{sa} \]  \hspace{1cm} (26)

Both the actual source currents \((i_{sa}, i_{sb}, i_{sc})\) and the reference source currents \((i_{sa}^*, i_{sb}^*, i_{sc}^*)\) of the respective phases are compared and then current error signals are fed to HCC.

4 | SIMULATION RESULTS

The performance of both ALMS and SLMS control algorithm based on its leaning pattern are simulated using MATLAB (SIMULINK) and Sim Power System (SPS) toolboxes in discrete time are discussed below.

4.1 | Performance of ALMS algorithm

The following performance of DSTATCOM using ALMS technique under different loading conditions are analysed in two subsections.

4.1.1 | Constant loading

Here, the load remains constant throughout the chosen time span as depicted in Figure 3 (i). It illustrates the various waveforms such as supply voltage \((v_s)\), load current \((i_l)\), source current \((i_i)\), compensator current \((i_{ic}, i_{ib}, i_{ic})\) and self-supported capacitor voltage \((v_{dc})\). A constant voltage of 600 V across the self-braced capacitor is obtained during this period, satisfying voltage regulation. It is also observed that the magnitude of PCC voltage is regulated at the reference value of 318 V even if subjected to the load switching and thus satisfying the voltage balancing. The total harmonic distortion (THD) of \(i_i\) observed in the absence of DSTATCOM is 18.28 %, whereas it is 4.56 % in the presence of DSTATCOM. Thus, a reduction of 75.05 % THD has been achieved by the application of DSTATCOM. Apart from these, balanced and sinusoidal source current remains in phase with supply voltage throughout the chosen time span, indicates significant improvement of p.f.

4.1.2 | Diversity loading

Here, the single-phase load is switched off in a-phase by disconnecting the circuit breaker (CB) at 0.6 Sec and switched on at 0.7 Sec. as depicted in Figure 3 (ii). It illustrates the various waveforms such as supply voltage \((v_s)\), load current \((i_l)\), source current \((i_i)\), compensator current \((i_{ic}, i_{ib}, i_{ic})\) and self-supported capacitor voltage \((v_{dc})\). With diversity loading also a constant DC voltage of 600 V is obtained across the self-braced capacitor during this period, satisfying voltage regulation. It is also observed the magnitude of PCC voltage is regulated at the reference value of 317 V (L-L) even if subjected to the load switching and thus satisfying the voltage balancing. The total harmonic distortion (THD) of \(i_i\) in the absence of DSTATCOM is 18.96 %, whereas the same is 4.85 % in the presence of DSTATCOM. Thus, there is a 73.64 % percentage reduction in THD by the application of DSTATCOM. Apart from these, balanced and sinusoidal source current remains in phase with supply voltage and so PF has improved.

4.2 | Performance of SLMS algorithm

Similarly, the following performance of DSTATCOM using SLMS technique under different loading conditions are analysed in the different two subsections:
4.2.1 Constant loading

Here, the load remains constant throughout the simulation time of interest as depicted in Figure 4 (i). It illustrates the various waveforms such as supply voltage \(v_s\), load current \(i_l\), source current \(i_s\), compensator current \(i_{ca}\), \(i_{cb}\) and \(i_{cc}\) and self-supported capacitor voltage \(v_{dc}\). A constant voltage of 542 V is obtained across the self-braced capacitor during this period and thus satisfying voltage regulation. It is also observed that the magnitude of PCC voltage is regulated at the reference value of 320 V (L-L) even if subjected to the load switching and so satisfies the voltage balancing. The total harmonic distortion (THD) of \(i_s\) in the absence of DSTATCOM is 17.84\% whereas the same is 2.72\% in the presence of DSTATCOM. Thus, a reduction of 84.75\% in THD, is achieved by the application of DSTATCOM. Apart from these, balanced and sinusoidal source current remains in phase with supply voltage indicates significant improvement of PF.

4.2.2 Diversity loading

Here, the single-phase load is switched off in a-phase by disconnecting the circuit breaker (CB) at 0.6 Sec and switched on at 0.7 Sec. as depicted in Figure 4 (ii). It illustrates the various waveforms such as supply voltage \(v_s\), load current \(i_l\), source current \(i_s\), compensator current \(i_{ca}\), \(i_{cb}\) and \(i_{cc}\) and self-supported capacitor voltage \(v_{dc}\). A constant voltage of 580 V is maintained across the self-braced capacitor during this period and hence satisfying voltage regulation. It is also observed the magnitude of PCC voltage is regulated at the reference value of 320 V even if subjected to the load switching and so satisfies the voltage balancing. The total harmonic distortion (THD) of \(i_s\) in the absence of DSTATCOM is 18.51\%, whereas the same is 3.32\% in the presence of DSTATCOM. Thus, a reduction of 82.06\% in THD, is achieved by the application of DSTATCOM. Apart from these, balanced and sinusoidal source current remains in phase with supply voltage indicates a better PF.

4.3 Analysis of DC-link voltage

It is inferred above observations that DC-link voltage of the DSTATCOM is reduced from 600 V to 542 V during constant loading and from 640 V to 580 V during diversity loading. Performance of both ALMS and SLMS control technique based DSTATCOM are compared to study the variation of \(v_{dc}\) and depicted in Figure 5 (i,ii).

The following major contributions are presented below:

(i) The SLMS control technique possesses its control action in regulating the DC-link voltage during unbalanced condition and is found to be 580 V, whereas it is 600 V in the ALMS control technique.

(ii) The SLMS control technique possesses its control action in regulating the DC-link voltage during unbalanced condition and is found to be 542 V, whereas it is 600 V in the ALMS control technique.

(iii) 4.4 Analysis of harmonic spectra

(iv) The detailed comparison on THD of both source and load current is summarized below:

(v) The THD of source and load current are 4.56\% and 18.28\% respectively under constant loading condition, whereas THD of source and load current are 4.85\% and 18.96\%, respectively under diversity loading condition using ALMS technique.

(vi) The THD of source and load current are 2.72\% and 17.84\% respectively under constant loading condition and the THD of source and load current are 3.32\%
and 18.51% respectively under diversity loading condition using SLMS control technique which is shown in the Table 1.

4.3 Analysis of kVA rating

It is also inferred that the rating of the DSTATCOM is reduced to nearly 78% (from 8.995 to 6.858 kVA).

4.4 Study of additional benefits

(i) The other benefits such as less capacitor stress, less stored energy and reduced rating of VSC leads to the foremost support of the proposed controller.

To analyse the dynamic performance, the simulation time for both the controllers is set at 1 s. But the convergence characteristics observed by SLMS at 0.05 s, whereas ALMS technique at 0.25 s in a single iteration. From this comparison, it is concluded that the proposed approach is having quick convergence and less computational complexity compared to the ALMS technique.

5 EXPERIMENTAL RESULTS

A 3P3W prototype DSTATCOM is developed in our laboratory to verify the practicability of both ALMS as well as SLMS controller and shown in Figure 6. The parameters used in experimental setup are the same as that mentioned in Table 2 for simulations. The DSTATCOM involves an IGBT based SEMIKRON (MD B61 600/415-30F) inverter assembled with required DC-supply and other accessories. Voltages and currents from various parts of the system are sensed using hall-effect voltage transducer LEM LV25-P, current transducer LA55-P, current probes (A622) and voltage probes (RP1050D). The dSPACE module DS1104 along with MATLAB2014a/Simulink and connector panel module CP1104 for analog feedback signal are used to implement the proposed control algorithm [27–30]. The supply voltage and load current are tracked through the dSPACE 1104 panel via DAC (digital to Analog converter) channel. The use of all 14 ADC channels at a time may be problematic because of high acquisition delays of the processor’s core. Here, sampling time of 20 µs is chosen to achieve efficient performance of the algorithm. The detailed execution process of d-SPACE is mention in the cited literature [25–30]. The current is determined with scale 25 A/div whereas the voltage scale is determined with 200 V/div.

5.1 Constant loading using ALMS control technique

The experimental waveforms of the load, compensator and source current under constant loading using ALMS control technique are shown in Figure 7 (i). As can be seen, the load current is distorted with its THD value as high as 18.28%. After compensation the grid current becomes close to sinusoidal with its THD reduced to 4.56%. The power factor realised at
FIGURE 6  Experimental setup of the proposed DSTATCOM

TABLE 2  System parameter

| Grid Load Controller | VSC |
|----------------------|-----|
| Grid Load Controller | VSC |
| V<sub>s</sub> = 230V (L-N) | 3-Ø diode bridge | μ<sub>k</sub> = 0.4 | k<sub>µ</sub> = 0.7 | C<sub>dc</sub> = 2000°F |
| f<sub>s</sub> = 50 Hz | Rectifier with RL load: | e<sub>k</sub> = 0.2 | k<sub>e</sub> = 0.1 | Compensating |
| R<sub>k</sub> = 0.04 Ω | R<sub>S</sub> = 10 Ω | σ<sub>k</sub> = 0.6 | k<sub>σ</sub> = 0.5 | impedance: |
| L<sub>k</sub> = 2 mH | L<sub>S</sub> = 20 mH | γ<sub>k</sub> = 0.4 | k<sub>γ</sub> = 0.02 | R<sub>S</sub> = 0.25Ω |
| v<sub>0</sub> = 325 V | | ξ<sub>k</sub> = 0.1 | | v<sub>dc(ref)</sub> = 600 V |

FIGURE 7  Experimental waveforms of load current (25A/div), supply current (25A/div) and filter current (25A/div) using ALMS technique under: (i) constant loading, (ii) diversity loading
source side is 0.96, which comply with IEEE 519–2014 and IEC 61000-3-2 STD. As a result, the voltage balancing demanded by the load is regulated at 600 V. Thus, it is evident that all the PQ issues are improved efficiently during constant loading.

5.2 Diversity loading using ALMS control technique

To evaluate the diversity loading performance, the experimental waveforms of the load, source and compensator using ALMS control technique are shown in Figure 7 (ii). As can be seen, the load current is distorted with its THD value as high as 18.96%. The grid current becomes more sinusoidal with its THD reduced to 4.85% and the compensating current contains harmonic spike is obvious. The power factor at source side is 0.897 which comply with IEEE 519–2014 and IEC 61000-3-2 STD. As a result, the voltage balancing demanded by the load is regulated at 580 V.

5.3 Constant loading using SLMS control technique

The experimental waveforms of the load, compensator and source current under constant loading using SLMS control technique are shown in Figure 8 (i). As can be seen, the load current is distorted with its THD value as high as 17.84%. The grid current becomes close to sinusoidal with its THD reduced to 2.72%. The compensating current contains harmonic spike is obvious. The power factor realised at source side is 0.99, which comply with IEEE 519–2014 and IEC 61000-3-2 STD. As a result, the voltage balancing demanded by the load is regulated at 542 V.

5.4 Diversity loading using SLMS control technique

To evaluate the diversity loading performance, the experimental waveforms of the load, compensator and source current using SLMS control technique are shown in Figure 8 (ii). As can be seen, the load current is distorted with its THD value as high as 18.51%. The grid current becomes close to sinusoidal with its THD reduced to 3.32%. The compensating current contains harmonic spike is obvious. The power factor at source side is 0.97, which comply with IEEE 519–2014 and IEC 61000-3-2 STD. As a result, the voltage balancing demanded by the load is regulated at 640 V.

To evaluate the reduced rating DC link voltage of the DSTATCOM, both the algorithms are compared and shown in Figure 9 (i,ii). As seen from Figure 9 (i), DC-link voltage of the DSTATCOM obtained is 600 V and 542 V under
balanced condition under ALMS and SLMS algorithm respectively, Whereas Figure 9 (ii) indicates 640 and 580 V during diversity loading under ALMS and SLMS algorithm respectively. The Figure 10 demonstrated the THD% of both source and load current using chat diagram. It is evident that the proposed algorithm is identified in a right research application to showcase its suitability and applicability for the power quality improvement.

6 | CONCLUSION

SLMS algorithm is proposed for the DSTATCOM as an optimal current harmonic extractor and its performance is investigated for PQ assessment in the EDS for different loading in this paper. Effectiveness and feasibility of the proposed algorithm for the EDS have been validated through experimental results.

The inference from the experimental studies satisfies the benchmark value of IEEE-519-2014 standard which are mentioned below:

(i) The THD of the source current is 2.72% and 3.32%, respectively under both balanced and unbalanced loading conditions.
(ii) The supply current becomes close to sinusoidal and almost unity power factor is achieved.
(iii) Reduced rating of DSTATCOM is realized.
(iv) Minimum value of DC capacitor voltage is attained so that capacitor stress can be reduced.
(v) The other benefits such as less capacitor stress, reduced rating of VSC and less stored energy are the major contribution of the proposed control method.

Hence, it can be expected that the proposed controller will perform better for any kind of topology designed for distributed FACTS devices dealing with power quality issues.

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