Design Pipeline Architecture with Fuzzy Logic

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Abstract. This paper aims to design the pipeline who is considered a set of related data processing elements in a series where the result of one element is the introduction of the next one, and it can be used to increase performance and speed at the same time, and we use it in computer systems or home appliances. Increasing the voltage in the pipeline increases the power. When the clock frequency increases to increase the performance of the pipeline, the power increases but at the same time the possibility of an error increases. System errors will lead to a wasted in energy consumption which in turn reduces system efficiency. The problem is how to reduce the power in the pipeline system without effecting the process speed or frequency so that we mention the same throughput with this power. We will deal with N bit full adder and study the effect of increasing these bits on both the time delay and the power consumption of the pipeline gate, and the results show that there is a direct relationship between the number of bits and the power. The razor circuit is used with the pipeline so that the errors that will occur in the pipeline will be detected and corrected within one clock cycle instead of wasting the time and energy on incorrect data, thus the power consumption will be reduced. By introducing a Fuzzy logic controller to the pipeline, it was possible to minimize the power consumption of the system by monitoring the number of bit errors and the consumed power. Also, we will make a comparison of the pipeline when using the controller and when not in use, and we will notice the effect of the controller in reducing the power consumption of the pipeline.

1. Introduction

A pipeline is a technique used to increase speed and also increase performance instead of taking something big and treating it at one time. We divide it into phases and begin treatment step by step so that it simplifies the process. We will use DVFS technology with the Razer to design the pipeline. This technology will provide for each stage of the pipeline its adjustable voltage. The voltage control unit searches for the error rate at each stage of the pipeline relay and performs the voltage control process in the stage where the error rate is high and therefore each stage of the pipeline will individually reduce its energy needs and this is what we seek. Since the 1960s, when the need for a device became fast, cost-effective, accurate, and fast, pipeline computer engineering has gained much attention, as demonstrated in researches (Singh and Parmar, 2012)(Abd-El-Barr and El-Rewini, 2005)(Loup bear, 2010). We can use the pipeline not only in computer systems and mobile phones, but we can also use it in home appliances or digital cameras to increase speed as well as improve performance. We will make a comparison of energy consumption when using the Fuzzy Logic Controller for the pipeline and when the
controller is not used, and we will prove through the results that using Fuzzy Logic will reduce energy consumption significantly.
In this paper will be organized as follows: we will design the pipeline architecture by simulating the power in the pipeline for a different number of bits and voltage and frequency and technology. And we will explain what the pipeline in the first section is, then in section two we will explain what the circuits used to design the pipeline is. In the third section, we will explain the controller used to control errors. Finally, we will make some conclusions in the final section.

2. Simple Pipeline

The performance of the pipeline depends on dividing the instructions into several subsections or stages, each of which performs part of the required operations, that is, each performs its function. The first stage is called Fetching Instructions (IF), and sequentially Decoding Instructions (ID), Executing Instructions (EX), and Memory (M), and the Write-Back (WB) as the sub-tasks needed to execute the instructions. In this case, there are likely to be up to five directives in the pipeline at the same time, thus reducing the instruction execution latency (Loup bear, 2010).

![Figure 1. Pipeline structure.](image)

3. Circuits Used to Design Pipeline

The designed pipeline in this work consists of five circuits connected in a series. These circuits are; the memory circuit followed by the Razer circuit, the full adder circuit, a second circuit for the Razer and the the memory circuit, as shown in following Figure
3.1. Razor

The processor pipeline should include a mechanism that is designed for detecting timing faults and restoring them to deal with rare situations that require more effort and reduce energy consumption. In this paper, the mechanism we will use to detect timing faults in the circuit is Razer (Austin et al., 2004).

The main purpose of using Razer is to modify voltage, that is, to give each phase of the pipeline its voltage, through measuring the error rate during circuit operation, thus eliminating the need for voltage margins and making use of circuit delay data (Kang et al., no date).

The operating circuit is based on two hours separated by a cycle text. During this course, the cycle will detect the error that occurs in the pipeline. The Razor will give an alarm signal when the error is confirmed, the pipeline stops for only one session. At the same time, the correct signal will be generated and entered into the pipeline, so that the correct value is not published until the beginning of the next cycle in the pipeline (Wang, Kim and Kim, 2008).

Figure 2. Pipeline design.

Figure 3. Razor circuit.
When converted circuit in Figure (3) by using NAND gate the circuit will be as shown in the following figure

![Diagram of Razor circuit using NAND gate]

**Figure 4.** Razor circuit by using NAND gate.

### 3.2. Memory

Memory devices as well as many other electronic circuits contain memory cells within which bits of digital data are stored. Certain memory cells can be static or dynamic.

![Diagram of Memory circuit]

**Figure 5.** Memory circuit.

### 3.3. Full Adder

The full Adder consists of 3 inputs and 2 outputs. Three bits be added at one time. The A and B bits to be added from both input and the third input of the load created by the previous addition.

\[
\begin{align*}
\text{sum} &= (A \oplus B) \oplus C_{in} \\
C_{out} &= A \cdot B + C_{in} \cdot (A \oplus B)
\end{align*}
\]  

\[(1-a) \quad (1-b)\]
4. Fuzzy logic control

There are different types of controllers. Most of these units require specific characteristics and accurate modelling to function properly. Energy model of digital systems has been established in many types of research that depend on random variables such as the structure of the logical system and the entry number. As a result, a classic regular controller cannot be used, instead, smart controllers such as NNCs and Fuzzy Logic Controllers should be used in all digital systems (Hasanien et al., 2014) (Thro and McNeill, no date) (Sasiadek, no date). By introducing a Fuzzy logic controller to the pipeline, it was possible to minimize the power consumption of the system by monitoring the number of bit errors and the consumed power. The Fuzzy logic controller is used to suggest the required biasing voltage for the pipeline so that the pipeline will consume less power without errors while maintaining the same speed. The results show that there is a considerable reduction in power consumption in the pipeline when using the Fuzzy Logic Controller compared to that without any controller.

![Figure 6. Circuit diagram of a full adder by using NAND gate.](image)

![Figure 7. Structure of fuzzy logic controller.](image)
To control voltage, the fuzzy logic we used in our design are is constructed, consisted of two inputs, namely bit-error and power, and one output $V_{DD}$.

![Fuzzy logic controller](image)

**Figure 8.** Fuzzy logic controller.

### 5. Power Calculation Algorithm
MATLAB was used to implement the power dissipation algorithm on digital circuits to calculate the circuit's power. This algorithm has been represented in stages; in the first stage, the load capacitor is calculated for every gate. This algorithm represents in stages, in the first stage we calculate dynamic power (Bajpai and Rana, 2017) and load capacitor for each gate and the calculation is according to the equations shown (Al-doori, 2017a)

\[
P_d = F \cdot C_L \cdot \alpha \cdot VDD^2
\]

\[
C_L = C_{DP} + C_{DN} + no \cdot (C_{GP} + C_{GN})
\]

($C_L$) is the load capacitor, $C_{DP}$ is the capacitor for p substrate drain, and $C_{DN}$ is the capacitor for n substrate, $C_{GP}$ and $C_{GN}$ are the capacitance of the p and n gate substrates. $no$ is the fan-out (number of connected exit gates).

The initial design parameters have been adopted according to the Table 2. After which we calculate $C_{OX}$ according to equation (4).

\[
C_{OX} = \frac{\varepsilon_{ox}}{t_{ox}}
\]

Where the $c_{ox}$ is the oxide capacitance and the $t_{ox}$ is the thickness of the oxide can be estimated from (Geometry and Analysis, 2008)

$\varepsilon_{ox}$ is given by:

\[
\varepsilon_{ox} = 3.9 \cdot \varepsilon_0
\]

$\varepsilon_0$ is the permittivity of the free space and is equal to 8.854x10-12 (F/M2).

| Table 1. the parameters used corresponding to the technologies(Cao et al., 2000; Zhao and Cao, 2006; Balijepalli, Sinha and Cao, 2007; Sinha et al., 2012) |
| Technology | $T_{ox}$ | $V_{th}$ | $V_{fp}$ | $u_{en}$ | $u_{ep}$ |
|-------------|---------|---------|---------|----------|----------|
| 45 nm       | 1.8e-009| 0.62261 | -0.587  | 0.049    | 0.021    |
| 22 nm       | 1.4e-009| 0.68858 | -0.63745| 0.035    | 0.011    |
| 16 nm       | 1.2e-009| 0.68191 | -0.6862 | 0.028    | 0.0075   |
and we also calculate $t_d$ according to the equation shown in equation (6) (Al-doori, 2017b).

$$t_d = \frac{C_L V_{PD}}{\mu C_{ox} W \left( V_{PD} - V_{th} \right)^2}$$

(6)

The given equations clarified the relationship between voltage, time delay, frequency, and gate connections to dynamic power. For proving that this relationship is working properly, a test have been performed on pipeline circuit.

### 6. Simulation Result

The following figures show the obtained results for calculating power and time delay. Many different technologies, as well as different values of voltages, have been implemented. It can be concluded that the smaller the value of the technology, the less energy consumption there will be. Therefore, the lower the voltage, the less energy consumption there is. Therefore, for the time delay, increasing voltage value results in decreasing the time delay value, and the lower the technology decreases the time delay value.

Figure (9) shows the values of three technologies 16, 22, and 45 which are compared with the design of one-bit pipeline, and changes to pipeline are observed in case of increasing the value of technology. It has been found that the greater the amount of voltage (0.9, 1.2, 1.5, 2, 2.5), the greater the amount of energy is because of the positive relationship between voltage and energy based on Equation (2). Simultaneously, the lower the value of the technology (16, 22, 45), the lower of the energy value becomes, with the lowest energy consumption being when the technology is 16 nm.

![Figure 9. Power Dissipation Vs Frequency 1-Bit pipeline using the MATLAB.](image)

Figure (10) shows the values of technology of (16, 22, and 45), which are compared to illustrate what happens to time delay. In one bit of the pipeline, and it has been found that with increasing the voltage value, the time delay decreases, which means that there is an inverse relationship between time delay and effort according to Equation (6). Therefore, a lower technology value refers to lower time delay value.
In the next section, the changes that happen to the power and time delay when the number of bits in the pipeline increases will be explained. Figures (11) and (12) show that the number of bits is increased to four, and a comparison is made using voltages with different values (0.9, 1.2, 1.5, 2.5, and 2.5). Several techniques have been selected (45, 22, and 16). It is found that the increase in the number of bits resulted in increasing the values of power and time delay, which means that there is a direct relationship between the number of bits and the power, and at the same time, the speed increased significantly.

**Figure 10.** Time Delay by Using the Power Model 1-Bit pipeline.

**Figure 11.** Power Dissipation Vs Frequency 4-Bit pipeline using the MATLAB.
Therefore, the changes of the time delay and power when the number of bits increases into 8 is observed. It is found that increasing the number of bits increases speed, as shown in Figures (13) (14).

The following results show the changes of the power when using fuzzy logic control with the pipeline circuit. Also, the results show how to detect and eliminate the error by choosing the appropriate voltage.
If the frequency increases, the power increases as well, as according to the Equation (2). The task of fuzzy logic is to detect this change in frequency and choose the appropriate voltage to accomplish power reduction.

Fuzzy logic reduces the voltage to its lowest value to ensure that power consumption is low as possible as. The simulation is performed using many techniques (45, 22, 16,180) nm, and many different frequencies have been utilized. The fuzzy logic control for the designed pipeline has been entered, and the following figures show how to control the voltage and choose the appropriate voltage, and how Razor detects errors and corrects them.

The first technique used in the simulation is technique 16, which is the smallest technique used in this design, and the effect that the choice of technique has on time delay and energy for one bit of the pipeline was noted. Figure (15) shows the average time delay of the pipeline circuit that has been used when inserting the controller.

Figure (16) shows each of the power values, as well as the voltage value chosen by the fuzzy logic. And from the Figure, it can be seen that there is no error in the 1-bit of the proposed design, and the power value has been shown; when increasing the frequency, power starts to increase as it is directly proportional to the frequency according to Equation (2).

![Figure 15. Time Delay of 16nm by using the fuzzy logic 1-Bit pipeline.](image1)

![Figure 16. Power Dissipation Vs Frequency of 16nm 1-Bit pipeline using the fuzzy logic.](image2)
In the next section, the changes to the power and time delay will be explained and the detection of errors when the number of bits in pipeline design increases from one bit to four for the same technology, which is 16nm.

It can be noticed that the time delay has been represented between $10^{-10}$ and $10^{-9}$ in the four bits pipeline, while in the one-bit pipeline, it has been between $10^{-11}$ and $10^{-10}$. With the increase in the number of the bits, the time delay values start to increase. It can be noted that the power has been between $10^{-8}$ and $10^{-7}$ in the four bits pipeline, while the one-bit pipeline has been represented between $10^{-9}$ and $10^{-8}$. That is, with the increase in the number of bits, the power values start to increase.

In this part, the technique that is used in the simulation is technique 22, and the effects of this technique on the time delay and energy for the one bit of pipeline were observed. Figure (19) shows the average time delay of the pipeline circuit that has been used when inserting the controller.

Figure (20) refers to each of the power values, as well as the voltage value chosen by the fuzzy logic. And Through the Figure, it is noticed that there isn’t any error in 1-bit of the proposed design. The value of the power was shown; when increasing the frequency, power starts to increase as it is directly proportional to the frequency according to the Equation (2).
The next section explains what happens to power and time delay when the number of bits in pipeline design increases to four bits for the same technology, 22nm. It can be noted that the increase in the number of bits results in increasing the time delay values. Therefore, with the increase in the number of bits, the power values increase.
The dynamic power consumption of the 45nm pipeline for one bit and eight-bit is shown in Figures (23) and (25). The time delay is shown in Figures (24) and (26), where the results of this test are similar to that of the 22nm and 16 nm technologies.

Figure 22. Power Dissipation Vs Frequency of 22nm 4-Bit pipeline using the fuzzy logic.

Figure 23. Time Delay of 45nm by using the fuzzy logic 1-Bit pipeline.

Figure 24. Power Dissipation Vs Frequency of 45nm 1-Bit pipeline using the fuzzy logic.
It can be noted how the Razor detects the errors and correcting them and how the fuzzy chooses the appropriate voltage to obtain the suitable value for the power in Figure (26).

For finding the fuzzy logic performance, the pipeline using the controller was compared with another pipeline that doesn’t contain a controller. V_DD has a constant 0.9 Volt, and the frequency is constant, 22 nm technology size is used in the simulation. The other techniques are neglected because the remaining values give the same results.

Figure 25. Time Delay of 45nm by using the fuzzy logic 8-Bit pipeline.

Figure 26. Power Dissipation Vs Frequency of 45nm 8-Bit pipeline using the fuzzy logic.

Figure 27. Power Dissipation Vs number of bit of 22nm.
It is clear that fuzzy can reduce the power of the pipeline circuit by reducing the value of $V_{DD}$. And when increasing the number of bits, power began to increase, meaning a direct relationship between the number of bits and the power.

Figure (28) shows the value of the power and the ability of the controller to reduce energy consumption when using a constant voltage 0.9V and constant technology 45nm of the pipeline circuit, and the comparison between the power values in case of (with) and (without) controller has been made. It can be noted effect of these frequencies on the power value.

![Figure 28. Power Dissipation Vs Frequency of 45nm.](image)

Figure (29) shows the obtained power calculations, compared with the power and without a controller. In case of without using many different technologies, as well as a constant value of voltage 0.9V and frequency 80MHz. It can be concluded that the smaller value of the technology is, the less energy consumption.

![Figure 29. Power Dissipation Vs Technology.](image)
7. Conclusion
In this paper we designed the pipeline as shown in the figure (2), we dealt with a complete set of N bits and chose the effect of increasing these bits on both the time delay and energy consumption of several pipeline gate technologies, and we explained the effect of these technologies on the pipeline where the smaller the size Technology the lower the energy consumption. We also introduced a fuzzy logic controller into the electronic circuit of the pipeline so that it can automatically control the power requirements of the pipeline and reduce the power consumption clearly, and we made a comparison when using the controller and when not using it and worked to reduce energy consumption.

8. Appendices
To control voltage, the fuzzy logic we used in our design are is constructed, consisted of two inputs, namely bit-error and power, and one output $V_{DD}$.
And the rules used in fuzzy logic are shown in Table (1) and can be read as follows: If the bit error is 0 and the power is Vsmall, then $V_{DD}$ is Z. Table (1) the rules used in fuzzy.

![Figure 30: fuzzy logic controller](image)

| Bit error | power | VDD |
|-----------|-------|-----|
| IF 0      | and Vsmall | then | Z   |
| IF 0      | and Small  | then | Z   |
| IF 0      | and Normal | then | NS  |
| IF 0      | and Big    | then | NB  |
| IF 0      | and Vbig   | then | NB  |
| IF 1      | and Vsmall | then | Z   |
| IF 1      | and Small  | then | PS  |
| IF 1      | and Normal | then | PS  |
| IF 1      | and Big    | then | PB  |
| IF 1      | and Vbig   | then | PB  |
| IF 2      | and Vsmall | then | PS  |
| IF 2      | and Small  | then | PS  |
| IF 2      | and Normal | then | PB  |
| IF 2      | and Big    | then | PB  |
| IF 2      | and Vbig   | then | PB  |
| IF 3      | and Vsmall | then | PS  |
| IF 3      | and Small  | then | PB  |
| IF 3      | and Normal | then | PB  |
| IF 3      | and Big    | then | PB  |
| IF 3      | and Vbig   | then | PB  |
| Condition  | THEN  | PB |
|------------|-------|----|
| 4 and Vsmall | then  | PB |
| 4 and Small  | then  | PB |
| 4 and Normal | then  | PB |
| 4 and Big    | then  | PB |
| 4 and Vbig   | then  | PB |
| 5 and Vsmall | then  | PB |
| 5 and Small  | then  | PB |
| 5 and Normal | then  | PB |
| 5 and Big    | then  | PB |
| 5 and Vbig   | then  | PB |
| 6 and Vsmall | then  | PB |
| 6 and Small  | then  | PB |
| 6 and Normal | then  | PB |
| 6 and Big    | then  | PB |
| 6 and Vbig   | then  | PB |
| 7 and Vsmall | then  | PB |
| 7 and Small  | then  | PB |
| 7 and Normal | then  | PB |
| 7 and Big    | then  | PB |
| 7 and Vbig   | then  | PB |
| 8 and Vsmall | then  | PB |
| 8 and Small  | then  | PB |
| 8 and Normal | then  | PB |
| 8 and Big    | then  | PB |
| 8 and Vbig   | then  | PB |

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