Elimination of strength degrading effects caused by surface microdefect: A prevention achieved by silicon nanotexturing to avoid catastrophic brittle fracture

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The unavoidable occurrence of microdefects in silicon wafers increase the probability of catastrophic fracture of silicon-based devices, thus highlighting the need for a strengthening mechanism to minimize fractures resulting from defects. In this study, a novel mechanism for manufacturing silicon wafers was engineered based on nanoscale reinforcement through surface nanotexturing. Because of nanotexturing, different defect depths synthetically emulated as V-notches, demonstrated a bending strength enhancement by factors of 2.5, 3.2, and 6 for 2-, 7-, and 14-μm-deep V-notches, respectively. A very large increase in the number of fragments observed during silicon fracturing was also indicative of the strengthening effect. Nanotextures surrounding the V-notch reduced the stress concentration factor at the notch tip and saturated as the nanotexture depth approached 1.5 times the V-notch depth. The stress reduction at the V-notch tip measured by micro-Raman spectroscopy revealed that nanotextures reduced the effective depth of the defect. Therefore, the nanotextured samples were able to sustain a larger fracture force. The enhancement in Weibull modulus, along with an increase in bending strength in the nanotextured samples compared to polished single-crystal silicon samples, demonstrated the reliability of the strengthening method. These results suggest that this method may be suitable for industrial implementation.

Defects inevitably exist in all materials regardless of how they are prepared. These defects significantly degrade material strength. From a practical standpoint, achieving the theoretical limit of material strength due to pre-existing, micro-sized manufacturing defects that cause ductile or brittle fracture under applied load is impossible¹⁻⁴. Over the past few decades, researchers have explicitly addressed the causes and remedies of fracture for various material types, either brittle or ductile, to achieve the
Silicon, which is extensively used in very large scale integrated (VLSI) circuits, nano/microelectromechanical systems (N/MEMS), and photovoltaic products, is quite brittle and suffers from catastrophic fracture due to concentrated stress at microdefects\(^{8-10}\) on its surface. These microdefects are generated because of external loading\(^8\), thermal processes\(^{10,11}\), or film growth\(^{12,13}\). Silicon wafer manufacturing includes several processing steps that are extensively used in industry, each of which multiplies the probability of surface defect formation. These steps include wafer handling\(^8\), back-side grinding\(^{14}\), chemical mechanical polishing (CMP)\(^{15,16}\), and dicing\(^{17}\). Each of these steps generates microdefects, such as scratches, dimples, mounds, and hazes. These undesirable features degrade wafer strength by localizing stress concentrations associated with crack initiation, which is responsible for wafer fracture.

Fulfilling the demands for silicon wafers to have an increased diameter and reduced thickness requires precise control of defects. This requirement has led numerous researchers to investigate various methodologies, such as crack deflection through implanting external elements into the bulk\(^8\) or reducing defect size\(^8\), for strengthening silicon wafers. Dopant diffusion by oxygen\(^{18}\), nitrogen\(^{19-21}\), and germanium\(^{22}\) has been shown to generate a greater pinning effect on dislocations, which delocalizes the stress concentration at defects and obstructs crack propagation. In a doped material, some of the original Si–Si bonds are replaced with higher-energy bonds that eventually strengthen the material\(^{23}\). However, the doping concentration changes the resistivity of the materials and influences the bulk properties of the silicon, which may be detrimental. Methods such as CMP\(^24\), and annealing the silicon wafer in oxygen\(^{25}\) reduce defect size while retaining bulk properties. Unavoidable large particles in the incoming slurry and agglomerated slurry on the polishing pad are the most likely causes of micro-scratches generated during the CMP process. This process can be controlled to an extent through process optimization, but optimization cannot effectively eliminate the presence of microdefects\(^{26}\).

Recently, nanoscale reinforcements for material strengthening have been developed for ceramics and glass. These methods have demonstrated a pronounced strengthening capability. Nanocoatings form brittle matrices and fibres to deflect the crack propagation pathways of ceramic materials\(^{27-29}\). Nanoparticles in the coating material on a glass tend to migrate into surface defects and reduce the stress concentration, thus improving the glass mechanical properties\(^{30,31}\). Most nanoscale reinforcement techniques fail to retain the bulk properties of the material. Approaches for improving the mechanical properties of silicon materials have not been sufficiently researched from the perspective of nanoscale reinforcement, and considerable material loss due to fracture still occurs in semiconductor processing. In our previous study, we demonstrated that nanotexturing on the surface of single-crystal silicon (sc-silicon) substrates could substantially enhance the strength of the material by a factor of six while maintaining its bulk properties\(^{32}\). The results of this previous study led us to conduct an in-depth macroscopic and microscopic exploration to elucidate the mechanism involved in the nanotexturing process.

### Results

Defects are randomly distributed on the surface of silicon, and predetermining which particular defect will result in fracture is difficult because of extremely fast crack initiation and propagation. In the present study, we evaluated the strengthening induced by surface nanotexturing through the introduction of a dominant V-notch defect in sc-silicon samples. The V-notch emulated a synthetic defect that functions as a single-stress concentrator that dominates all other defects and serves as a crack initiation point\(^{33-36}\) for strengthening silicon wafers. Dopant diffusion by oxygen\(^{37}\), nitrogen\(^{38-40}\), and germanium\(^{41}\) has been shown to generate a greater pinning effect on dislocations, which delocalizes the stress concentration at defects and obstructs crack propagation. In a doped material, some of the original Si–Si bonds are replaced with higher-energy bonds that eventually strengthen the material\(^{42}\). However, the doping concentration changes the resistivity of the materials and influences the bulk properties of the silicon, which may be detrimental. Methods such as CMP\(^43\), and annealing the silicon wafer in oxygen\(^{44}\) reduce defect size while retaining bulk properties. Unavoidable large particles in the incoming slurry and agglomerated slurry on the polishing pad are the most likely causes of micro-scratches generated during the CMP process. This process can be controlled to an extent through process optimization, but optimization cannot effectively eliminate the presence of microdefects\(^{45}\).

Two types of samples, including non-textured and nano-textured V-notch samples as shown in Figs. 2(a–c), were prepared to study the interaction between nanotextures and defects. The V-notch shown in Fig. 2(d) was fabricated through anisotropic tetramethylammonium hydroxide (TMAH) etching. As shown in Figs. 2(e,f), wet-chemically etched silicon nanotextures with a pitch (p) and a width (w) of 100±10 nm were fabricated over the entire surface of silicon surrounding the V-notch using electronless metal deposition with Ag\(^+\) ions in an etchant composed of 4.6 M hydrofluoric acid (HF) and 0.02 M silver nitrate (AgNO\(_3\)). The precipitated Ag dendrites formed as etching byproducts were removed with an aqueous solution of 70% concentrated nitric acid (HNO\(_3\)).
The morphology of the silicon nanotextures was controlled by fabricating a smooth nanotexture bottom, which may influence the strength and fracture of the samples (see Fig. S1 in supplementary material).

**Macroscopic analysis for strength enhancement.** Macroscopic measurements, including bending-strength analysis, were performed to evaluate the effects of increasing nanotexture depth \( (d_n) \) on a given notch depth \( (d_c) \). The samples were 60 mm in length, 20 mm in width, and 0.61 mm in thickness, satisfying the ASTM E 855-90 standard\(^{22} \) for the three-point bending (3PB) test (Fig. 3 (a)). The test was performed at a loading rate of 30 mm/min. The bending strength \( \sigma_{br} \) was determined by equation (1)\(^{22} \):

\[
\sigma_{br} = \frac{1.5F_L}{wt^2},
\]

Figure 1. Illustration of the systematic investigation performed to elucidate the mechanism involved in strengthening silicon through nanotexturing.

Figure 2. Structural description of samples. Schematic of (a) V-notch, (b) and (c) nanotextured V-notch. (d) and (e) SEM images of a non-textured V-notch and nanotextured V-notch sc-silicon sample, respectively. (f) SEM image of surface nanotexturing.
where $F_r$ is the load at rupture and $L$, $w$, and $t$ are span length, width, and thickness of the sample, respectively. A bending strength of 0.24 GPa for flat, polished sc-silicon samples was used as a reference and is shown by the black dotted line in Fig. 3(b). The microdefect depth of the silicon wafer was generally within the range of 1–8 μm.43–46 Three different controllable depths of synthetic defects were added to the midpoint of the samples. The V-notch depths of 2, 7, and 14 μm were designed to validate the possibility of nanotexture strengthening for the entire range of microdefect depths generated during the wafer-processing steps. Although the depths of microcracks on the surface of polished sc-silicon samples is on the order of several microns, different samples may contain microcracks of different depths at various locations. The V-notch represents a major crack of controllable depth at the midpoint, and this defect supersedes all other defects. The stress concentration increased as the defect depth increased47, resulting in degradation of bending strengths to 0.19 GPa, 0.13 GPa, and 0.06 GPa for the 2-, 7-, and 14-μm-deep V-notch samples, respectively. The depth of V-notch was increased to 7 μm and 14 μm for ensuring the dominance of V-notch on other pre-existing defects. Samples with different nanotexture depths for each V-notch depth were fabricated to evaluate the effect of nanotexturing depth on strengthening. The
bending strength of nanotextured V-notch samples was enhanced from 0.19 GPa to 0.48 GPa (2.5-fold) for 2-μm-deep V-notches, from 0.13 GPa to 0.41 GPa (3.2-fold) for 7-μm-deep V-notches, and from 0.06 GPa to 0.36 GPa (6-fold) for 14-μm-deep V-notches (Fig. 3(b)). For all V-notch depths, the bending strength increased with increasing nanotexture depth. The results indicate that nanotexturing ceases crack initiation from the notch tip and allows the silicon to sustain larger forces before fracture. The bending strength enhanced by nanotexturing of the V-notched samples was also insensitive to loading rate under quasistatic conditions (see supplementary Fig. S2).

The force displacement curves from the 3PB tests for the non-textured and nanotextured V-notch samples are shown in Fig. 3(c). All samples demonstrated very similar responses, which included nonlinear behaviour near the starting point, a linear region, and sudden fracture at the end. Insufficient friction between the fixture support and the sample resulted in the nonlinear behaviour due to slipping from the initial load. The stiffness (i.e., the slope of the force-displacement curves), given as 39.5 and 39 kN/m, was translated into Young’s modulus values of 169.8 GPa and 167.3 GPa for non-textured and nanotextured V-notch samples, respectively (see the Methods section for additional details). These values are similar to the reported value of 169 ± 7 GPa. The small changes in the Young’s modulus for nanotextured samples also signifies that the bulk properties of the silicon were preserved.

The dynamic response of the fracture in the 3PB test was also observed using a high-speed camera. Fragmentation analysis is another direct macroscopic method for examining the strengthening mechanism. For any type of brittle material, a greater number of fragments produced during fracture will result in a greater sample strength due to high absorption of strain energy. The non-textured V-notch samples broke neatly into two main pieces under an applied load, as shown in Figs. 4(a,c), because the V-notch suppressed the effects of all other pre-existing defects and functioned as a dominant crack initiation point. Fracture of the V-notch samples into only two fragments illustrates a reduction in material strength due to the V-notch. The nanotextured V-notch samples broke into several fragments during the fracture process, as shown in Figs. 4(b,d), which indicates the strength of the samples had been enhanced. The fragmentation of flat polished sc-silicon samples during fracture was also compared to that of the nanotextured V-notch samples (see Fig. S3 in supplementary material). The flat polished sc-silicon samples broke into a larger number of fragments compared to the non-textured V-notch samples and into
a smaller number of fragments compared to the nanotextured V-notch samples. This result suggests that the strength of the samples was degraded by the V-notch and that the nanotextured samples were stronger compared to the non-textured samples or the flat polished sc-silicon samples.

Macroscopic observations confirmed that tuning the depth of nanotexturing for a defect size can effectively increase the strength of a material above the non-defective baseline strength. The overall phenomenon indicates the existence of some mechanism connecting the nanotexture to defects. The fragmentation results indicated that the V-notch induced a large concentration of stress at the notch tip compared to other regions and functioned as the exclusive crack initiator. The multiple fragments after fracture from the nanotextured samples might have been generated by the elimination of concentrated stress at the notch tip, which would likely have reduced the effective depth of the V-notch. To validate this hypothesis and to elucidate the mechanism, we conducted an in-depth microscopic-level investigation to analyse the stress behaviour.

**Microscopic analysis of stress distribution.** The stress behaviour was studied by simulating non-textured and nanotextured V-notch samples in a 3PB model using the ANSYS 12.1 (finite element analysis) software. Structural discontinuities, such as defects, are considered to induce localized stress, resulting in a large increase in the stress above a nominal value derived from completely defect-free samples (which are practically unachievable) under an applied force. The effects of a stress inducer can be determined in terms of a stress concentration factor (SCF) by which the stress of the region local to the discontinuity is increased over the nominal stress. The V-notch on the surface concentrated the stress at the notch tip (Fig. 5(a)), representing a condition suitable for evaluating the SCF. The factor SCF was defined as the ratio of the maximum stress \(\sigma_{\text{max}}\) to the nominal stress \(\sigma_{\text{nom}}\), as expressed in equation (2):\(^{47}\)

\[
SCF = \frac{\sigma_{\text{max}}}{\sigma_{\text{nom}}}
\]

The nominal stress \(\sigma_{\text{nom}}\) refers to the maximum stress applied to a flat polished sc-silicon substrate. An average fracture force of 31 N was experimentally evaluated by the 3PB test for flat polished sc-silicon samples, and this value for \(\sigma_{\text{nom}}\) was applied to all the simulation scenarios. The nominal stress was uniformly distributed over the flat silicon sample (see Fig. S4 in supplementary material); however, the presence of the V-notch concentrated and increased the stress in a small region near the notch tip to a level above the nominal value of stress. Consequently, no stress appeared at the surface near the V-notch, as shown in Fig. 5(a). For a nanotexture depth of zero, simulated samples with V-notch depths of 2, 7, and 14 \(\mu\)m exhibited SCF values of 2.9, 4.4, and 5.6, respectively, as shown in Fig. 5(d). These findings agree with the observation that SCF increases along with increasing V-notch depth\(^{47}\) and is responsible for the observed reduction in bending strength. As shown in Fig. 5(b), nanotexturing at half the depth of the V-notch initiated a reduction in stress at the notch tip and enhanced stress distribution in the nanotexture region. The extent of stress reduction and distribution increased when the nanotexture depth approached the depth of the V-notch, as shown in Fig. 5(c). This result implies that the effective depth of the V-notch was reduced until the effect of the V-notch was completely eliminated. Figure 5(d) shows that the SCF decreased to approximately 1.8 and saturated as the nanotexture depth approached 1.5 times the V-notch depth. The stress decreased at the notch tip and simultaneously increased in the nanotextured region near the V-notch as the depth of nanotexturing increased, which implies a redistribution at the notch tip. Our finite element analysis results revealed two significant regions—the notch tip and the nanotextured region in the vicinity of the V-notch—worthy of further exploration through real-time stress measurements using micro-Raman spectroscopy.

The stress distribution is schematically shown in Fig. 6(a). Major stress appeared at the notch tip \(n_t\) and at the region nearby the V-notch \(n_n\). The stress was measured by micro-Raman spectroscopy under the 3PB condition to evaluate changes in stress distribution due to nanotexturing (refer to the supplementary material for the experimental setup, Fig. S5). Curve-fitting approximations using a Lorentzian function\(^{50}\) (refer to the methods section and supplementary Fig. S6) were generated to obtain the wavenumber shift \(\Delta \omega\), which can be converted into tensile stress \(\sigma\) for sc-silicon using equation (3):\(^{50}\)

\[
\sigma (\text{GPa}) = 0.47 \times \Delta \omega
\]

With no load applied, both non-textured and nanotextured V-notch samples measured at the notch tip retained the Raman peak at approximately 520.6 cm\(^{-1}\) (Figs. S6(a,c)), which is similar to the reported value for a non-stressed silicon peak\(^{51}\). The fracture force measured for a 7-\(\mu\)m-deep V-notch with and without nanotexturing was 34 N and 13.2 N, respectively. The Raman spectra were obtained just prior to fracture at 32.4 N and 12 N of force for the non-textured and nanotextured samples, respectively. These values were close to the fracture force. Under the 3PB condition, the peak shifted by 0.53 cm\(^{-1}\) to lower wavenumbers under the applied load of 12 N for the non-textured V-notch sample and by 0.55 cm\(^{-1}\) under 32.4 N for the nanotextured V-notch sample (Figs. S6(b,d)). The Raman spectrum was also captured for the nanotextured region near the V-notch \(n_n\), and the wavenumber shifted by 0.11 cm\(^{-1}\) under an applied load of 12 N for the non-textured V-notch sample and by 0.32 cm\(^{-1}\) under 32.4 N for the
nanotextured V-notch sample. The generated stress corresponding to wavenumber shift was determined by equation (3). Fig. 6(b) demonstrates that a larger fracture force was endured by the nanotextured V-notch samples. The mechanism can be explained by observing the behaviour of generated stress with increments in the force for both non-textured and nanotextured V-notch samples. The non-textured V-notch sample generated a maximum sustainable stress of 0.24 GPa (at notch tip) after a force of 12 N was applied; however, the nanotextured V-notch sample generated 0.1 GPa (at notch tip) after the same 12 N of force was applied. These results indicate that the larger fracture force of 34 N was accommodated while generating nearly the same maximum sustainable stress of 0.26 GPa. Simultaneously, the
nanotextured region began distributing stress from the notch tip as soon as the force was applied, which was evident from the observed increase in stress from 0.05 GPa (for non-textured V-notch samples) to 0.15 GPa (for nanotextured V-notch samples) in the region near the V-notch (n_s) just prior to fracture (Fig. S6(e)). This result implies that nanotexturing the V-notch samples reduced the effective defect depth, which enabled the samples to accommodate a larger force and led to the same amount of stress at the notch tip. These results agree with the fact that the mechanical strength of brittle materials can be improved by reducing defect depth through reduction in stress generated by an applied force47.

**Discussion**

The modest enhancement in strength achieved by nanoscale reinforcement is now possible for silicon. The macroscopic 3PB test was coupled with micro-Raman stress measurements to establish a correlation between macro and micro measurements for investigating the strengthening mechanism. The enhanced strength along variations in a series of measured bending strengths under identical testing conditions was also essential and was analysed through Weibull estimation. The presence of unpredictable, randomly distributed micro-defects in polished sc-silicon samples cause large variations in bending strength, which is undesirable. The Weibull modulus (m) is a parameter that defines statistical variations in measured bending strength of nominally identical brittle-material samples under the same testing conditions (larger
variations result in a lower value of $m$) based on the probability of failure ($P_f$)\(^{52,53}\) (see the Methods section for more details of Weibull estimation). A statistical analysis of bending strength measured by a 3PB test was performed. The Weibull modulus ($m$) estimated for polished sc-silicon samples was 10.5, which was comparatively lower than the non-textured V-notch samples measured as 22.2, 23.6, and 30.2 for 2-, 7-, and 14-μm depths of the V-notch, respectively (Fig. 7(a)). Predicting the dominant defect (responsible for fracture) among pre-existing defects is difficult and varies from sample to sample for polished sc-silicon, leading to a relatively low value of $m$. The large value of $m$ for non-textured V-notch samples ensured that the intentionally created V-notch defect was predominant over other pre-existing defects. The value of $m$ increased, but the bending strength decreased as the V-notch depth increased (Fig. 7(a)). This result demonstrated that the inevitability of the crack initiation from the notch tip increases with V-notch depth and further justifies that the non-textured V-notch samples fractured into two fragments because of the presence of large stress concentration under an applied load at the notch tip.

The bending strength of 2μm for non-textured V-notch samples was similar to that of the polished sc-silicon samples and was further analysed by Weibull estimation (refer to the supplementary material for the Weibull estimation of the 7- μm-depth samples, Fig. S7). Nanotexturing not only recovered and enhanced the bending strength but also increased the Weibull modulus ($m$) compared to that of polished sc-silicon samples. The Weibull modulus was improved because of nearly uniform nanotexturing over the surface, which
prevented any non-predictable pre-existing defects from becoming dominant (also demonstrated by the occurrence of multiple fragments during fracture) and demonstrated the reliability of the methodology. We conclude that silicon nanotextures with a pitch and a width of 100–150 nm and a depth greater than the pre-existing manufacturing defect depth can effectively enhance the strength of silicon wafers. A nanotexturing depth of 5–10 μm, depending on the wafer type, could eliminate the strength-degrading effect of defects. The 3PB tests revealed enhanced material strength, resulting in a larger displacement before fracture for nanotextured V-notch samples compared to non-textured samples (Fig. 3(c)). The results suggest that nanotexturing can enhance the strength of silicon materials such that less fragile silicon substrates with thicknesses below 100 μm are now possible. Silicon wafers with a 70 ± 5 μm thickness incorporating nanotextures at a 5 μm depth are feasible for mass production of rollable wafers, shown in Figs. 8(a,b). Generally, the backsides of silicon substrates used in semiconductor manufacturing industries do not contain electronic circuitry. Here, we also present a rollable silicon wafer in Fig. 8(c) with nanotexturing on the backside and a polished surface on the front side for semiconductor processing (see the supplementary video). These wafers would allow for manufacturing of flexible silicon solar cells.
with thicknesses less than 100 μm and of RF devices with thicknesses less than 50 μm. This technology
need not be limited solely to flexible and bendable electronics. In the future, we believe that the backside
of silicon substrates, which is generally not used for any purpose, could be nanotextured to enhance
strength and control for material loss due to fracture, thereby reducing manufacturing costs. The semi-
conductor, photovoltaic, and MEMS industries suffer from yield losses due to mechanical failure, and
these industries could all benefit from this technology.

Methods
Specimen preparation. A dry silicon oxide 250-nm-thick (hard mask for TMAH etching) was
formed on n-(100) sc-silicon wafers (1–10 Ω-cm resistivity). The wafers were diced along the Si (110)
direction with a sawing machine (Disco DAD 2H/6T) at a dicing rate of 5 mm/s, producing samples of
60 mm (length) × 20 mm (width) × 0.6 mm (thickness). The slow dicing rate was maintained to reduce
the damage layer produced at the edges and sidewalls of the diced samples. The produced damage layers
were etched by HNA composed of HF (49%), HNO3 (70%), and CH3COOH (99%) in a volume ratio of
2:7:1 24. The top and bottom surfaces of the samples were protected by anti-acid tape to avoid undesirable
acidic and alkali attack on the surfaces. The sidewall and edges (<1 mm) were exposed to the HNA etch-
ing to remove the damage layer of 50–80 μm produced by dicing. The samples with protective tape were
submerged in acetone solution and isopropyl alcohol to remove the protective tape and subsequently
 cleaned with DI water. The samples were photolithographically patterned and then chemically etched
with a 25% concentrated TMAH and IPA (isopropyl alcohol) solution at 85 °C to fabricate the V-notch.
The IPA was mixed with TMAH to reduce the surface roughness during the anisotropic etching of the
V-notch. The TMAH etching time depended upon the photolithographically obtained pattern width of 3,
10, and 20 μm specifically designed for 2-, 7-, and 14-μm-deep V-notches, respectively. The hard mask of
SiO2 was removed by buffer oxide etching (BOE), which also removed residues from the anti-acid pro-
tection tape, to obtain the most immaculate samples possible for the nanotexturing process. Electroless
metal deposition etching was performed using 4.6 M HF and 0.02 M AgNO3 that produced silicon nano-
textures26 on the samples, except for the V-notch, which was covered with polymer. The residual pattern
formed as Ag dendrites were removed with an aqueous solution of 70% concentrated nitric acid (HNO3)
(refer to the supplementary material for the complete process, Fig. S8).

Macroscopic analysis using the 3PB test. The sample was placed under the material testing
machine (Hung Ta 8336) at room temperature using a load cell that yields to rupture at a displacement
rate of 30 mm/min by the load applicator. The support span for testing was 40 mm
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Microscopic characterization by micro-Raman spectroscopy for stress analysis. A micro-Raman spectroscopy system (Jobin-Yvon T64000) was integrated with the 3PB testing machine and a thermoelectrically cooled charge-coupled device, as shown in the supplementary material (Fig. S5).
Line scanning was conducted at each applied force by moving the sample stage for focusing the laser
spot within the V-notch and in the nearby nanotextured region. The measurement technique employed a linearly polarized neodymium-doped yttrium aluminium garnet (Nd:YAG) 532-nm laser focused on a
spot size of approximately 1-μm-diameter via a microscope. The light source yielded a penetration depth
of approximately 0.1 to 0.7 μm in silicon55. An Olympus (100 × NA = 0.9) objective lens was used for
laser focusing and Raman signal collection. As shown in Fig. 6(a), the stress-free silicon surface and the
remainder of the stressed silicon region were organized into voxels. Large stress values were observed
only at the notch tip and nanotexture bottoms. The angled wall of the V-notch and nanotexture pillars
was nearly stress-free, and each of them was covered by a single voxel. The obtained Raman spectrum
consisted of a very large volume of information from the stress-free silicon surface; this information
was separated from the information derived from the stressed silicon regions. Two curve-fitting approxima-
tions using a Lorentzian function40 were applied to separate the non-stressed spectra from the stressed

Dynamic fracture behaviour observed by high-speed camera. The rupture photographs of
non-textured and nanotextured V-notch samples were captured using a high-speed camera (IDT Y-4)
recording at a frame rate of 2,000 frames/s under the illumination of a 500-W halogen lamp with a 950-μs
exposure time and 1,280 × 1,024 pixel resolution. The camera was equipped with a lens (TAMRON
A09N) with a focal length of 30 cm. To better illustrate the detailed fracture phenomena, the fracture of
the polished sc-silicon sample was also compared to that of the nanotextured sample (see supplementary
Fig. S3).
Raman spectra, as shown in supplementary Figs. S6(a–d). The curve fitting performed using the Lorentz function was determined using equation (5)26:

\[ y = y_0 + \frac{2A_1}{\pi} \frac{FWHM_1}{4(x-x_{c1})^2 + FWHM_1^2} + \frac{2A_2}{\pi} \frac{FWHM_2}{4(x-x_{c2})^2 + FWHM_2^2} \]

where \( y_0 \), \( A \), \( FWHM \), and \( x \) are the offset, area, full-width at half-maximum, and centre (x-coordinate of the peak), respectively, derived from the Raman spectrum; \( A_1 \), \( FWHM_1 \), and \( x_{c1} \) are the information related to the non-stressed silicon peak; and \( A_2 \), \( FWHM_2 \), and \( x_{c2} \) are the information related to the stressed silicon peak.

**Estimation of Weibull modulus (m).** The Weibull estimation is widely used in engineering to relate the scattering of measured bending strength to the probability of failure (\( P_f \)), where \( n \) is the rank (number of samples with strength \( \sigma \) or lower) and \( q \) is the total number of samples tested. The Weibull distribution was estimated by the function shown in equation (6)27:

\[ P_f(\sigma) = 1 - e^{-\left(\frac{\sigma}{\sigma_0}\right)^m} \]

The double logarithm of equation (6) was used for ease of accessing information for the bending-strength analysis. According to the linear regression, \( m \) is the slope of the graph plotted from equation (7). A large value for \( m \) is desirable because it represents less scattering in the measured bending-strength values and more predictable failure behavior.

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Author Contributions
J.A.Y. conceived the idea and supervised the project. K.K., A.K. and C.T.H. designed and conducted the experiments. K.K., Y.Y.L. and M.T.H. performed the data analysis. K.K., A.K. and C.T.H. wrote the manuscript. All authors discussed the manuscript.

Additional Information
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