Hybrid technology for the production of highly integrated multi-chip microcircuits: problems and solutions

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Abstract: Innovative technologies in the field of microelectronics provide technological transformation of the crystal and multichip microcircuit industry, combining various methods of crystal mounting and packaging processes. An increase in the integration of electronic circuits, an increase in the number of peripheral elements and, as a result, an increase in the energy consumption of the crystal, lead to a significant increase in the complexity of solving the problems of packaging when the case is converted into a complex electronic device.

Chip crystals, according to current technological standards, are produced by a small number of specialized companies owned by transnational corporations. At the same time, in a number of countries there are qualified personnel specializing in the design of integrated circuits. One of the trends in the Russian market of multifunctional miniature devices is import substitution. A patent information search was conducted to identify trends and directions in the development of technologies in the field of packaging integrated circuits. A detailed analysis of the problem of the production of multi-chip microcircuits, systems in a package combining various packaging processes is shown; ways to solve it are shown, including applied research aimed at creating a hybrid multi-chip packaging technology combining crystals installed in a single package and on a single substrate using various methods installation - Wire bond and Flip chip.

Keywords: hybrid packaging technology, innovative technologies, multi-chip microcircuits, microelectronic modules, system in the case, case on the case, microelectronic industry, microwelding, crystal mounting.

1. Introduction

Currently, there are tendencies in the transition to innovative technologies in the field of microelectronics, which ensure the technological transformation of the crystal manufacturing industry, innovative microcircuits, and systems in the housing, combining various packaging processes (Zhmurin, 2000).

One of the trends in the Russian market of multifunctional miniature devices is import substitution. In conditions when a small number of specialized companies belonging to transnational corporations produce chip crystals, and designing the topology of crystals and systems is carried out in several countries of the world, including Russia, the problem of producing multi-chip microcircuits with a high degree of integration arises in Russia. Since the system in the case may contain a processor chip, installation of which, as a rule, takes place using Flip Chip technology and memory crystals installed using Wire bond technology, it is necessary to consider the possibilities and prospects of packaging such microelectronic modules that combine different methods of mounting crystals. A patent information search was carried out with the identification of trends and directions of technology development in the studied area.

Microelectronics is dominated by two technologies for assembling crystals into cases or into multi-chip modules: Wire Bond and Flip Chip (Elenius & Levine, 2000). When choosing the type of packaging for a long time, Wire
Bond technology was preferred, based on the connection of the case leads with the contacts on the periphery of the crystal. This technology has been tested, has a developed infrastructure, a high level of quality and a percentage of yield of suitable crystals. However, this method of packaging has a number of disadvantages associated with the fact that the welding effect can lead to latent defects in complex and brittle crystals, and the welding operation is a sequential procedure, which reduces labor productivity; in addition, it is impossible to weld the contacts in the working region of the chip, which dramatically reduces the number of I/O pins on the chip. These shortcomings are leveled when using cases made on the basis of flip-chip technology. In this case, the housing allows contact with any point of the crystal and is able to minimize signal interference. One of the advantages of flip-chip technology is also the ability to mount crystals with a matrix arrangement of contacts. The problems of this technology include the complexity of the switching base (substrate) and low thermomechanical characteristics during thermal cycling.

Therefore, at present, developers use precisely these two packaging methods (Wire Bond and Flip Chip) for various single and multi-chip assemblies (Takahashi, 2017).

The analysis showed the promise of developing technological solutions for hybrid multi-chip packaging that combines the main methods of wire bond and flip chip mounting on a substrate in a single device. The hybrid technology for systems in the "SiP" case will allow the use of crystals prepared for different assembly methods by different suppliers in one product. The basic principle of the "PoP" technology ("Package on package") is the creation of a unified case, which has the ability to connect several cases in a stack through the classic surface mount process. In these cases, you can place any crystal: processor, memory, digital and analog crystals, including systems on a SoC chip. By combining crystals and using standard bus interconnects, you can get modules with different functionality. This technology is currently the main one for the production of highly integrated solutions for wearable electronics and is actively used by companies such as APPLE, SAMSUNG and QUALCOMM.

2. Literature Review

In works written by Belyakov S. (2014), Shadeyiko A. (2009), Yablochnikov E.I., Smirnov P.V. and Vorobev A.S. (2014), it was shown that the process of packaging integrated circuits is fairly well studied. It is promising to increase the degree of integration of microcircuits at the crystal level and at the housing level, when two or more crystals are connected in one housing connected to each other by System in Package (SiP), as well as at the packaging level: housing in the Package in housing Package (PiP) or the case on the case of" Package on Package (PoP). An increase in the degree of integration at the SiP level is ensured by three-dimensional integration, in which the crystals are mounted on top of each other, forming a multi-level wiring of electrical connections, including through a layer of silicon Through Silicon Via (TSV). In order to fit into the standards of the size of the crystal housing, the crystals and substrates on which they are mounted are becoming thinner. The substrate is a printed circuit board on which crystals are mounted, followed by filling the compound with a protective layer. In the classical case, the packaging technology consists of several processes - thinning and cutting silicon wafers into individual crystals, mounting crystals on a substrate, creating electrical connections, creating a compound layer for electrical and physical protection of sensitive elements of the crystal circuit, creating ball leads on the back for attaching to printed circuit board, separation of the substrate into separate modules, as well as their testing, labeling and packaging.

It has been established that 3D microcasing and microassemblies reduce the area, volume, and mass of the electronic unit (Harajidi et al., 2018). In Bychkov’s doctoral dissertation and his numerous works (2014, 2015, 2016), the methodology for designing processor microcircuit cases and the principles for designing the periphery of chip crystals are scientifically substantiated. The results of the analysis of the main approaches to the use of different interconnect technologies when creating semitransmitter microcircuits within the framework of the concept of spatial integration are shown in (Khmel’nytskiy, 2011; Daits, 2017). Thus, the problem under study is relevant and requires the development of new innovative solutions based on the study of a wide range of research objects, including hybrid packaging technology, various methods of crystal mounting.

The microcircuits made by proposed technology can be utilized in the future technologies including boards used in IoT discussed by Neeraj et al., 2018.
3. Materials and Methods

The aim of the study is to identify problems and solutions in the development of a hybrid technology for packaging multi-chip microcircuits that combines the basic technologies for mounting on a wire bond and a flip chip in a single device. The development should provide progressive shifts in the microelectronic industry and substitution of import of consumer microcircuits. At the same time, the tasks of developing technological operations of hybrid multi-chip packaging, combining the basic methods of mounting on a wire bond and flip chip substrate in a single device, using integration methods, should be solved using the following methods: a) a system in a SiP package; b) the case on the “PoP” case using the “TMV” method.

As the research materials, the results of an extended system patent information search based on the methodology considered in the work (Shegelman et al., 2019) were used, with the identification of trends and directions in the development of technologies in the studied field. The technologies developed as part of the research project will become the basis for the innovative development of the Russian market of microelectronics products, providing new methods for constructing multi-chip assemblies. The significance of the tasks to be solved during the implementation of the project from the point of view of overcoming technical and technological limitations in the relevant areas of the country's economic development is very high, since it allows solving the problems of import substitution, increasing the country's security in the field of microelectronics. Analyzing the current level of development of civil microelectronics in the Russian Federation, the relevance of the project is confirmed by the uniqueness of the hybridization of the packaging process and the creation of microelectronic modules (including three-dimensional) of a high degree of integration.

The technology of three-dimensional crystal assembly, or 3D-assembly, is the most promising, it allows reducing the size of microcircuits by increasing the packing density, increasing the throughput of the compounds inside the crystal and reducing its energy consumption. This technology makes it possible to combine digital and analog circuits, memory and microelectromechanical systems produced by various technologies in one housing (Bondar, 2011, Mukhina & Bashta, 2009, Stoyanov, 2017).

Research Institute of Electronic Technology offers its solution. The objectives of the proposed solutions are: reducing the cost of production; increased reliability. Technical results are achieved by the fact that in the method of assembling three-dimensional 3D IS LSIs, including the operation of mounting the crystals on each other with subsequent connection to the housing using the leads; the connection of the crystals with the housing is carried out using the leads mounted on a polyimide tape (Zenin et al., 20.05.2016).

The Scientific Research Institute of Molecular Electronics and Mikron Plant (Krasnikov, 10.06.2011) proposed a method for manufacturing multi-level VLSI copper multilayer metallization. The method includes deposition of metal and dielectric layers, photolithography and selective etching of these layers, chemical-mechanical polishing of dielectric layers. Novelty of the method consists of the following: A multilayer conductive film consisting of an adhesive-barrier, seed and auxiliary layers is deposited on a silicon plate coated with a dielectric. Grooves to the seed layer are formed by the electrochemical method. Inside the grooves in the open areas of the seed layer, horizontal transmitters are grown until the grooves are completely filled; a second auxiliary layer is deposited on the surface of the plate. Holes are formed to the surface of the horizontal copper transmitters. The electrochemical method in open areas horizontal transmitters grown vertical copper transmitters until the holes for vertical wires are completely filled the transmitter. Then the second and first auxiliary layers are removed, the conductive layers between the horizontal copper transmitters are removed. Dielectric layers are applied to the surface of the plate by smoothing and filling methods and then by the method of chemical-mechanical polishing, the dielectric layers above the vertical transmitters are removed.

The work (Zemlyansky et al., 2018) presents the results of studies of the processes of using copper metallization with a nickel connecting layer on the contact pads of crystals of silicon semitransmitter products. The technology of deposition of films of vanadium, copper and nickel in one technological cycle at a substrate temperature of 320 °C, excluding subsequent annealing, is considered. An analysis of the methods for forming gold wire joints with a
diameter of 30 μm to the contact pads of crystals with Cu-Ni metallization showed that welding with a “split” electrode is optimal for a high-quality connection.

The work (Zenin et al., 2008) considered the formation of columnar leads on the contact pads of crystals for assembly using the flip-chip method, and the work (Stoyanov et al., 2014) considered the results of studies of the assembly processes of microelectronic products using metallization and copper wire, in (Smolin, 2004) - the results of studies on the use of aluminum metallization in integrated circuits, in (Lanin et al., 2010) - substantiated ways to improve the quality of microwelded joints in integrated circuits using ultrasonic systems of higher frequency.

Chip packaging technologies are being transformed from developing technologies into a mechanism for implementing future applications and products based on microelectronics. Technologies for heterogeneous integration of multiple crystals, including mixing high-density compound technologies with low-cost traditional technologies, lead to a high level of customization in the development of packaging technologies. Improving the technology of packaging contributes to the development of the semitransmitter industry (Baranov, 2014; Getz & Rentuk, 2018, Gubarev, 2012; Nisan, 2011). In the works of Gubarev (2012), it was noted that the implementation of super-large integrated circuits of the class “System on a Chip” (Gubarev, 2012) is noted modern technologies of packaging.

Specialists of the Voronezh State Technical University conduct research to solve the problems of improving the quality of the connection of the crystal with the body; reduce the complexity of assembly operations; improving the quality of cleaning gold foil; improving the environmental situation. To this end, a method of attaching silicon crystals of discrete semitransmitter devices and integrated circuits to the housing with the formation of a silicon-gold eutectic, including the placement of gold foil between the crystal and the base of the housing and soldering them, has been patented. The novelty of the method lies in the fact that before the soldering, the foil is annealed in vacuum at a temperature of 160-250 °C or in hydrogen at a temperature of 25 °C and atmospheric pressure of 101 kPa (Zenin et al., 27.04.2007). In the Russian microelectronic industry, at the moment there are a number of problems and technological barriers to launching a fundamentally new innovative technology and products. The main problems and technological barriers can be identified: the lack of technological maps of the process of mounting crystals, using modern methods and materials, the absence of the described methods of process quality control; processing plates with a thickness of less than 80 microns and a diameter of 300 mm or more; creation of three-dimensional micrcircuit structures up to 8 crystals; the impossibility of mass acquisition of components in which 3D integration is carried out. The task is aimed at creating tangible, qualitatively new products in the form of microelectronic modules of a high degree of integration and methods for their production; new, because it does not have well-established technological solutions; risky, since its solution is not obvious and requires research and experimental development.

4. Results and Discussion

As part of the research, an extensive patent information search was performed, which showed a wide range of publications and developments (Volkova & Popkov, 2018; Kochegin et al., 2017; Sammins, 2010; Skupov, 2016), including patentable ones and which confirmed relevance of the studied topics. The role of packaging technology in improving the performance and functionality of microelectronic systems is shown in (Balan & Ivashov, 2014). It is known that packaging electronic devices (modules) is a time-consuming and costly operation (Vikulov, 2009). Technologies for packaging microelectronic systems directly on the Wafer-Level Packaging (WLP) plate are being developed. WLP technology allows three-dimensional integration of microwave microelectronic systems on different substrates. Experts note that the stability of power integrated circuits in metal- and metal-glass cases to thermocyclic loads is provided by seam-assisted roller welding (Turtsevich et al., 2015).

Currently, traditional packaging technologies, well-debugged and provided with equipment and materials, are actively used, and advanced packaging technologies are gradually being developed, which include technologies: “Fan-Out WLP” (“Fan-Out Wafer Level Packaging”, polymer packaging of crystals using polymer matrices), encasing crystals on a plate before cutting, embedding crystals in a printed circuit board. According to the well-known data of the analytical agency “Yole”, the production of advanced packaging technology in 2018-2022 will
have a combined average annual growth rate of total revenue of 7%. The fastest growing is Fan-Out WLP packaging technology. The Flip-Chip technology is the most demanded and constitutes the main market share of advanced packaging technologies. According to experts, the penetration of Fan-Out technology will reduce the Flip-Chip market share by 2022. According to experts, advanced packaging technologies will dominate the markets of high-performance computing and data storage, as well as in the telecommunications industry, with further penetration into the markets of analog and high-frequency devices and the mobile segment, while considering growth opportunities in the automotive and industrial segments.

JSC Vega Radio Engineering Concern patented an invention in the field of radio electronics for use in the manufacture of hybrid integrated circuits and packaging of multi-chip electronic components containing thinned semitransmitter crystals as part of a single electronic component or substrate (Verba et al., 13.03.2017). The technical result of the invention is the expansion of the arsenal of methods for temporarily fixing substrates on a technological basis. To achieve this technical result, the following is done: an adhesive material is applied to the technological base either by spraying a slip, by vacuum or gas-dynamic spraying, for example, of fusible mineral glass "SiO2," with a eutectoid additive, or by applying a thin sheet of this material. Carry out the installation of the workpiece on the adhesive surface of the technological media. The resulting package is subjected to the temperature necessary to attach the workpiece to the technological plate; if necessary, apply a pressing force in a vacuum or atmosphere. As a result, the workpiece and the technological base are a single system penetrated by channels along the connection plane. Above the workpiece-base system carries out the usual technological operations. After performing all technological operations, the workpiece is separated from the technological base. To do this, the channels of the workpiece-base system are connected to the nozzles through which pumping a liquid substance that quickly dissolves the adhesive material, for example, a solution of hydrofluoric acid salts. When the ligament material is dissolved, release from adhesive forces occurs. To restore the geometry and integrity of the workpiece after its separation from the base, adhesive residues are removed from it. To do this, for example, it is mounted on a vacuum table and the side with adhesive residues is ground.

Closed Joint-Stock Company Research Institute of Microdevices-Technology has solved the problem of increasing the reliability and expanding the functionality of a three-dimensional multi-chip module on a flexible board by increasing the packing density and assembly accuracy, protecting the flexible board from mechanical and climatic influences in the manufacture and operation of the module, and improving thermal conditions and scalability in the number and type of chips used. For the manufacturing method of the named module, which includes the formation of side protrusions on a flexible board with microcircuits mounted on them, two mounting protrusions with contact pads serving as the terminals of a multi-chip module located symmetrically from two opposite edges of the flexible board are formed. Side protrusions containing connecting and mounting sections located on one or both sides of the flexible board are placed perpendicular to the central part of the flexible board, pairwise and coaxially along the same edges of the flexible board, cover both sides of the flexible board, with the exception of the contact pads, with a continuous anticorrosive material. Three-dimensional assembly of the module is carried out sequentially; laying and gluing with the adhesive-sealant side protrusions with microcircuits placed on them on the central part of the flexible board coaxially one above the other. Then the central part of the flexible board is folded, the sides of the microcircuit are combined without distortions of the module parts relative to each other, and the mounting tabs of the flexible board are located at the base of the assembled three-dimensional multi-chip module from two opposite edges. To improve the thermal regime of the three-dimensional multi-chip module, through windows are formed on the flexible board on the side protrusions in the center of the mounting sections, on the central part of the flexible board at the points of attachment of the side protrusions and between the mounting protrusions of the flexible board, and in the case of three-dimensional assembly of the multi-chip module, the windows are arranged coaxially one above the other, and then fill them with glue-sealant, providing an effective heat sink (Blinov et al., 08.06.2018).

Petrozavodsk State University has patented a device for attaching crystals for thinning, consisting of a base with an adhesive layer on which the crystals are face down, characterized in that the base with an adhesive layer is made in the form of a flexible film fixed to a rigid frame with magnetic holders (Belyaev et al., 11.09.2018). The technical result of the proposed device is to simplify the design of the device and increase ease of use by reducing the number of operations for the preparation of both plates of non-standard shapes and sizes, and individual crystals for the
operation of thinning. A technical result is achieved due to the fact that the base with an adhesive layer is made in the form of a flexible film fixed to a rigid frame with magnetic holders. In this case, the mechanical rigidity of the structure is achieved by pressing the film to the vacuum table of the installation to thin and film tension on the mounting device due to magnetic holders.

Another development of Petrozavodsk University (Putrolaynen et al., 12.12.2018) relates to the field of packaging integrated circuits and is aimed at limiting the displacement of substrates in the horizontal plane, simplifying the design and reducing the size of the clamping device, and accordingly increasing the number of products placed in the furnace in one polymerization cycle. For this, the housing is made in the form of a magazine with dividing plates for placing substrates between them to form a stack of substrates, with side walls made with guide angles used as guides for pressure plates and limiters to limit the horizontal displacement of plates and substrates. In this case, the housing is made with a hinged lid with clamping screws for clamping the upper pressure plate, and the lower pressure plate is mounted on the springs.

Closed joint-stock company NPO NIITAL has patented an integrated circuit case containing a ceramic base with a multilayer conductive structure and a matrix of column posts with a step hole in the center to accommodate the integrated circuit. The stepped hole is made blind, and a rim is fixed on the upper step of the hole to which a metal cover with a total thickness of 0.25 mm is welded seam-roller by welding, thinned to 0.1 mm in the welding zone. At the same time, the location of the matrix of column posts is made on the back of the installation site, and each of the terminals is made in the form of a column of low-temperature solder, or a solder column reinforced with a copper spiral, or a micro-spring of a cylindrical shape made of beryllium copper (Pilovova et al., 28.09.2017). The Boeing Company (US) has patented an invention that relates to a packaging method, system and device options for packaging photonic crystal sensors for use under extreme conditions (Karralero et al., 16.10.2017).

The patent of IP Photonics Corporation (US) states that the rapid development of semitransmitter laser technology has contributed to the use of high power laser diodes. The constant race for high-power lasers inevitably entails the need to improve the possibilities of thermoregulation when creating buildings, which would facilitate the simplification of controlled operations. Laser diodes generate a significant amount of heat, which can adversely affect their performance and reliability; therefore, it is necessary to find a thermally efficient packaging solution that will quickly remove the excess heat studied by the laser diode into the surrounding space. (Komissarov et al., 11.05.2017). In this regard, the companies patented a multilayer laser diode housing, comprising: a substrate having one surface for mounting a laser diode; a heat sink located at a distance from the surface of the substrate opposite the specified surface and directed towards it, moreover, the substrate and heat sink are characterized by the corresponding coefficients of thermal expansion "KTR". In this case, a metal layer deposited on the opposite surface of the substrate and interacting with it. A soft solder layer bonded to the metal layer and coupled to the heat sink so that the temperature of the p-n-junction of the laser diode remains substantially constant even after a predetermined number of repetitions of thermal cycles, at least several hundred cycles, at a temperature difference within each cycle, exceeding one hundred °C. A separation layer made of a material whose “KTR” coincides with the “KTR” of the substrate, and which is connected to the soft solder layer, and a solid solder layer located between the separation layer and the heat sink and connected to them.

Koninklijke Philips N.V. has patented a method for mounting VCSEL crystals on a crystal holder. The method comprises the steps. The formation of p-type mesastructures by providing electrical p-contacts on the upper part of the mesastructures. Formation of an n-type mesastructure, its coating with an electrically insulating passivating layer that overlaps at least the pn junction of the mesastructure. The deposition of non-wettable layer on the side of the connection of the crystals. The deposition of an additional non-wettable layer on the connection side of the crystal holder (non-wettable layers are deposited with the calculated pattern or their patterns are formed after deposition to form the corresponding connection areas on the crystal holder and crystals, the connection areas of which provide a wettable surface for solder). Application of solder to the joint area of at least one of the two sides of the joint. Placement and soldering of crystals to the crystal holder without fixation to allow the movement of crystals on the crystal holder due to the surface tension forces of the molten solder. The VCSEL crystal contains a grating with radiation from the lower side, which is soldered by its mesastructure to the crystal holder. Prior to deposition of the
non-wettable layer, a first metal layer is deposited onto the crystal bonding side, which is electrically connected to the VCSEL n-contacts and overlaps the n-type mesastructure. The n-contacts mentioned form a conductive network between the p-type mesastructures “VCSEL” for the electrical connection “VCSEL” and the current distribution uniformly among the p-type mesastructures. In order to overlap the p-type mesastructures and the p-contacts, the second metal layer is deposited at the same time as the first metal layer. The first and second metal layers mechanically stabilize VCSEL crystals so that the electrical connection with the n-contact is at the same height as the p-contacts (Preybom et al., 09.02.2017).

As noted in the patent (Chea et al., 28.06.2017), semitransmitter and micromechanical crystals or microcircuits are often provided with a housing to protect them from environmental influences. The housing provides physical protection, strength, external connections, and, in some cases, cooling for the crystal inside the housing. Typically, a chip or crystal is attached to a substrate, and then a cap is placed over the crystal that attaches to the substrate. Alternatively, the crystal is attached to the substrate, and then a body substrate is formed on the crystal. There is a tendency to add more functions to each crystal and to place more than one crystal in one housing. This makes the enclosures larger and also increases the specialization of enclosures. While a product with a very large production volume, such as a cell phone, can benefit from components designed for a highly specialized purpose, a product with a low production volume does not benefit from this. For products with lower production volumes and more specialized ones, the choice of multiple existing smaller crystals may be less expensive. This makes it possible to have greater flexibility in the functions that the product is endowed with and allows the use of smaller crystals in the case in the product.

Intel Corporation (US) has patented a method that relates to the field of creating enclosures of semitransmitter microcircuits and, in particular, to the creation of their enclosures, which is flexible in relation to curved forms of the case. The method comprises the steps of: closing a plurality of silicon crystals into a flexible substrate; form a flexible cushioning layer on top of the embedded crystals; forming a thin film heat-distributing layer on top of the substrate, opposite the flexible cushioning layer; they shape the substrate with crystals and a gasket and cure the substrate having the attached shape (Chea et al., 28.06.2017).

Siemens Matsushita Components GmbH & Co. KG patented an invention that relates to a casing device for electronic structural elements, in particular for those working on surface acoustic waves. According to the patent, the casing device for structural elements operating on surface acoustic waves is made with a cap that covers the structures of the structural elements on the substrate. The cap is formed by a coating provided on the substrate, which has recesses receiving them in the structural regions of the structural elements. The coating is formed by a vertical holder surrounding the structures of the structural elements on the substrate and a coating layer applied to the holder. As the material for the coating, a material structured by phototechnics is used and the coating is structured by phototechnics. (Fürbacher, 07.20.2000).

The invention of Russian patent holders relates to the field of development and production of electronic components, in particular, delay lines operating on surface acoustic waves (Dorokhov et al., 05.10.2018). According to the invention, the method of encasing the reflective delay line is characterized in that the reflective delay line is placed on the housing base through a dielectric gasket with a low dielectric constant, on the surface of which metallization is made with a topological pattern repeating the topological pattern of the elements of the reflective delay line, on one side of the gasket and continuous metallization on the other side of the gasket.

Specialists of the Moscow Institute of Electronic Technology solved the problem of reducing overall dimensions, increasing the reliability and functionality of multi-chip modules, microassemblies and system components in a housing based on flexible printed circuit boards with integrated component mounting. The solution is considered in the patent (Kruchinin & Vetryanov, 21.06.2019), according to which a three-dimensional multi-chip memory module is executed on a flexible polymer carrier, the base of which is equipped with open-frame memory microcircuits using the technology of solderless and non-welded mounting. Inter-level switching is carried out by means of microbumps located on the edges of the module around the modules with open-circuit microcircuits. The modules are coated with an organosilicon compound to give greater resistance to strength and climatic influences.

This solution allows you to create multi-level multi-chip memory modules and 3D microassemblies, where the
parameters for reliability, functionality and overall dimensions exceed the capabilities of the prototype. Since the contact between the open-circuit microcircuit and the carrier board is formed by direct metallization to the opened contact pads of the open-circuit microcircuit, the signal speed increases due to shorter transmitter lengths. Spatial assembly is not limited to only four open-circuit memory chips, but has the ability to install many times more with smaller overall dimensions, which gives another advantage over the prototype.

Specialists of the Research Institute of Microdevices-technology solved the problem of increasing the reliability and expanding the functionality of a three-dimensional multi-chip module on a flexible board by increasing the packing density and assembly accuracy, protecting the flexible board from mechanical and climatic influences during the manufacture and operation of the module, improving the thermal regime and scalability by the number and type of chips used. A method of manufacturing a three-dimensional multi-chip module on a flexible board includes the formation of side protrusions on a flexible board with microcircuits mounted on them. In this case, two mounting protrusions are formed with contact pads serving as the terminals of the multi-chip module located symmetrically from two opposite edges of the flexible circuit board, and the side protrusions containing connecting and mounting sections located on one or both sides of the flexible circuit board are arranged perpendicular to the central part of the flexible circuit board, in pairs and coaxially along the same edges of the flexible board, cover both sides of the flexible board, with the exception of the contact pads, with a continuous anti-corrosion material. Three-dimensional assembly of the module is carried out by sequentially laying and gluing lateral protrusions with glue-sealant with microcircuits placed on them on the central part of the flexible board coaxially one above the other. Then the central part of the flexible board is folded, the sides of the microcircuit are combined without distortions of the module parts relative to each other, and the mounting tabs of the flexible board are located at the base of the assembled three-dimensional multi-chip module from two opposite edges. To improve the thermal regime on the flexible board, through windows are formed on the side protrusions in the center of the mounting sections, on the central part of the flexible board at the attachment points of the side protrusions and between the mounting protrusions of the flexible board. In a three-dimensional assembly, windows are coaxially placed one above the other, and then they are filled with adhesive-sealant, providing an effective heat sink. For application as part of a three-dimensional multi-chip module on a flexible microcircuit board with a large number of pins and providing minimum weight and size characteristics, the flexible circuit board of the module is equipped with a matrix of soldered volumetric terminals formed on the back side of the flexible circuit within the projection area of the assembled module (Blinov et al., 08.06.2018)

The patent of the Scientific Research Institute of Electronic Technology (Brazhnikova et al., 10.12.2015) is intended to attach a semitransmitter crystal to a gilded case by contact-reactive soldering to form an Au-Si eutectic alloy in the manufacture of transistors and integrated circuits. The invention provides uniform distribution of the thermal field of high-power microwave multi-chip transistors, reducing thermal and electrical resistance. The scope of the patent (Bruchno et al., 20.08.2015) of the Silicon EL Group Company is the assembly production of multifunctional multi-chip modules and extra-large integrated circuits (VLSI) based on them. According to the patent, a silicon patch board consisting of a silicon substrate, layers of dielectrics and layers of metal wiring with interconnects and contact pads for mounting microcircuits by the inverted crystal method. Contact pads are made in the depressions of a silicon patch board with a depth of 15-25 μm, and silicon nitride is used as the upper layer of the dielectric. An extensive patent information search has shown the promise of creating technology that can significantly reduce the time and money for creating integrated circuits for various applications. The technology being created will allow us to construct microassemblies of any complexity using standard crystals and will solve problems that have not been solved previously in other ways, namely, by hybridizing the packaging process and creating three-dimensional microelectronic modules with a high degree of integration.

The competitiveness of a product created using research results on the Russian market is estimated to be extremely high due to the significant savings in the money spent on its use. Since the Industrial partner - GS NANO TECH is the only company in Russia that provides design and assembly services for multi-chip modules on a contract basis, including SiP (System in Package) systems, the technology will be in demand and competitive due to the natural monopolization of the market.
Marketing analysis and prospects for the implementation of microelectronic modules with a high degree of integration determine that the global market has been growing steadily over the past ten years, growing by an average of 14-16% annually, while gradually displacing traditional solutions from the market. Market growth for the corporate sector is around 20% per year. The annual market capacity of the Russian Federation totals about 200 thousand devices, with almost 30% being corporate-class microassemblies.

Experts believe that there is currently an interest from Russian market players for the volume of 50,000 devices per year. One of the trends in the Russian market of multifunctional miniature devices is import substitution. The issue of creating these devices on the Russian element base also becomes relevant. At the same time, packaging and assembly of key components are becoming more popular in the Russian Federation, the demand for such services will only grow in the coming years. The created technology will provide at least 80% of the technological processes of product creation carried out in the territory of the Russian Federation.

As a result of the research, the objectives of the project and possible solutions are formulated:

1. Development of circuitry solutions, design and technological documentation for devices of hybrid microcircuits with direct and inverted arrangement of crystals in a single housing using the technology "crystal in the housing" SiP.

2. Development of circuitry solutions, design and technological documentation for integrated circuits with a direct and inverted arrangement of crystals in a single device, including mounting the housing on the PoP housing.

3. Development of circuitry solutions, design and technological documentation for integrated circuits with a direct and inverted arrangement of crystals in a single device, including mounting the housing on the TMV PoP housing with the creation of interconnects made through the compound layer.

At the present stage, in Russia there are no manufacturers of systems in the package that combine various packaging processes. The implementation of the research project may be one of the first domestic developments capable of creating hybrid multi-chip packaging technology according to the SiP package system method, combining crystals installed in a single package and on a single substrate using various mounting methods - Wire bond and Flip chip , and also become an integrator of the process of designing and manufacturing integrated software and hardware solutions. The undoubted advantages of the product will be Russian assembly and customization according to customer needs at the hardware and software level.

Over the past 25 years, Petrozavodsk State University (PetrSU) has been working on the creation of integrated microelectronic systems for inertial navigation, local positioning systems, and distributed online measurement systems. All implemented projects are commercialized and have a business history, which suggests that the tasks associated with the development of packaging technologies for integrated circuits have a significant backlog. PetrSU has experience in implementing projects from concept development to the implementation of end devices on the market in the field of local positioning. The implementation period for complex projects of this kind amounted to 8 years: 3 years - creating a solution, 2 years - marketing work and positioning a product on the market, creating business applications, 3 years - spin-off companies and working in an international market.

GS NANOTECH, an industrial partner of this research, has formed an R&D group that fully meets world-class design requirements. The company has all the technological equipment required for the implementation of this project. Technical specialists have experience in mass production (over 1 million units) of SiP multi-chip modules using 2D WB technology. Existing equipment allows you to pack crystals in standard enclosures for proven technological processes. The company has a wide fleet of production equipment, a professional team for the maintenance and preparation of technological processes. The company has a mature quality management system in accordance with the requirements of ISO 9001: 2015. Purchase and delivery of materials and equipment is carried out directly from leading manufacturers. Currently, design documentation has been developed for hybrid microcircuit devices with a direct and inverted arrangement of crystals in a single housing using the "crystal in the case" technology of SiP and the technology of the case on the case of PoP. All design work was carried out in a
computer-aided design system, Cadence, which allows for the unified design of systems with support for contact bonding technologies of both Wire bond and Flip chip package. Mock-ups were developed for testing the “crystal in the case” SiP technology. The layout, which includes the substrate, is an integrated circuit designed to develop technologies for mounting crystals, and allows you to combine crystals with different mounting technologies on one substrate to minimize the dimensions of the finished product. A substrate is a workpiece made of dielectric material, intended for applying to it elements of integrated circuits, inter-element and (or) inter-component compounds, as well as contact ones. The substrate is intended for installation on it of one microprocessor chip using Flip-Chip technology and two memory crystals using Wire Bond technology. Layouts were made at the GS Nanotech manufacturing facility. Flip-Chip crystals were installed on the Datacon 2200 EVO. A 0.4 mm thick flux layer was formed in a special substrate; a crystal was immersed in it and then mounted on the substrate. The verification of the correct placement of crystals on the substrate was carried out using an x-ray apparatus. The soldering was carried out in a reflow oven according to a given thermal profile. To assess the quality of the soldering, repeated x-ray control was carried out at the facility. As a result, defects were discovered in the form of fusion of the grooves of the groove. Correction of this defect is possible by adjusting the soldering thermal profile or by changing the amount of flux. After increasing the flux thickness to 0.5 mm, the soldering defect no longer manifested. This was followed by washing the flux and drying the models in an oven and filling the cavities under the crystal with a compound (underfill) to distribute the mechanical load and increase reliability. The applied adhesive filler was polymerized in an oven and the degree of filling was monitored using a digital scanning acoustic microscope. After that, two more crystals were mounted on the Datacon 2200 EVO installation (Fig. 1) and their connection with the substrate was made by welding with a 25-μm gold wire on a Shinkawa UTC-2000 apparatus (Fig. 2).

![Figure 1. Installed crystals.](image1)

![Figure 2. The result of welding.](image2)

Finished mock-ups (Fig. 3) were used for testing.

![Figure 3. Finished mock-ups.](image3)

Parameters of the made models: length - 31 mm; width - 31 mm; thickness - 2 mm; number of pins- 898 pcs.

The processor chip is mounted on the upper plane using Flip-Chip technology, the cavities under it are filled with a special compound. On the substrate, with the help of glue, two NAND crystals of memory of different manufacturers were installed, and the welding was performed using gold wire with a diameter of 25 microns. Technological documentation prepared. Experimental samples of multichip microcircuit using SiP technology were fabricated. The next step is the manufacture of models and samples of microelectronic modules using the PoP and PoP technologies using the TMV method. The practical implementation of the project results involves the production of the main current products of the Industrial partner based on the developed technologies, as well as the
reduction in the cost of developing new types of products and the flexibility of their customization due to the universality of the case-to-case technology.

5. Conclusion

As part of the research, a detailed patent information search was performed, which showed a wide range of developments, including patentable ones, and confirmed the relevance of the subject under study. A detailed analysis of the problem of production of multi-chip microcircuits in the Russian Federation showed ways to solve it, including conducting applied research aimed at creating a hybrid multi-chip packaging technology using the method of a system in a case that combines crystals in a single case and on a single substrate, installed using various mounting methods - Wire bond and Flip chip. The analysis showed that the problem under study requires the study of a wide range of research objects, including hybrid packaging technology, crystal mounting, and interconnections through the compound. Important ways to solve the problem are the integration of the design and production processes of integrated software and hardware solutions that provide progressive shifts in the microelectronic industry. The ways of solving the problems of developing innovative technological operations of hybrid multi-chip packaging using integration methods are shown: a) a system in the SiP package; b) the case on the PoP case; and c) the case on the PoP case using the TMV method.

Petrozavodsk State University and its industrial partner - GS NANOTECH companies have the necessary scientific and technical potential to conduct research with the subsequent commercialization of the developed technological and technical solutions. The integration of the scientific, innovative potential of the university and the industrial partner ensures that research is carried out at a high scientific and technical level. The technology being created solves problems that have not been previously solved by other methods, namely, by hybridizing the process of packaging and creating microelectronic modules (including three-dimensional ones) of a high degree of integration. To create this kind of microelectronic devices, research is being conducted in the field of advanced packaging technologies and their applicability to the solution of tasks. Necessary technological operations have been identified; experimental work is underway to develop a technology that makes maximum use of the technological capabilities and equipment of the enterprise.

In the course of the work, research is being carried out on different methods of mounting crystals, creating intercrystal compounds in various designs, and testing the use of materials with taking into account different temperature conditions, the need to combine different types of physical effects on the crystal (ultrasound frequency 60-120 kHz, temperature effects (up to 350 degrees Celsius), chemical effects (flux, adhesive), crystal preparation technologies: thinning, cutting, machining. This research may become one of the first Russian developments, capable of creating hybrid multi-chip packaging technology according to the method of a system in a SiP package, combining crystals installed in a single package and on a single substrate using a different mounting method - Wire bond and Flip chip, and also become an integrator of the design and production of integrated software and hardware solutions. Methods for solving the problem under study should be the development of hybrid multi-chip packaging technology according to the method:

- a system in a SiP case, combining crystals installed in a different installation method - Wire bond and Flip chip in a single case and on a single substrate;
- a case on a PoP case, combining various methods of mounting crystals made on various partially enclosed substrates connected to a single device using surface mounting one on top of the other with the creation of interconnects by soldering;
- a case on the TMV PoP case with the creation of interconnects made through the compound layer of the underlying microcircuit case.

An important way to solve the problem is the practical implementation of research results, which involves the manufacture of the main current products of the Industrial partner based on the developed technologies, as well as the reduction in the cost of developing new types of products and the flexibility of their customization due to the universality of the case-to-case technology. The performed work will become the basis for the development of specific solutions necessary for the implementation of the Intelligent Transport Systems program in the spirit of
creating an elemental base of intelligent digital devices. The proposed solutions will ensure the creation and application of technologies defined by matrices of technological needs and markets.

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