Investigation of electronic properties of graphene/Si field-effect transistor

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Abstract
We report a high-performance graphene/Si field-effect transistor fabricated via rapid chemical vapor deposition. Oligolayered graphene with a large uniform surface acts as the local gate of the graphene transistors. The scaled transconductance, $g_m$, of the graphene transistors exceeds 3 $mS/\mu m$, and the ratio of the current switch, $I_{on}/I_{off}$, is up to 100. Moreover, the output properties of the graphene transistor show significant current saturation, and the graphene transistor can be modulated using the local graphene gate. These results clearly show that the device is well suited for analog applications.

Keywords: Graphene/Si field-effect transistor, CVD, Current saturation, Local graphene gate

Background
Graphene is a single-atom-thick carbon film [1,2] that has a very high carrier mobility ($2 \times 10^5$ cm$^2$/V$^{-1}$s$^{-1}$), a high saturation velocity, large current density, and thermal conductivity; as a result, it has attracted significant attention for use in high-speed applications and flexible electronics and as a candidate for next-generation technologies that enhance transistor performance beyond dimensional scaling [3,4]. To date, graphene-based electronics, including graphene field-effect transistors (GFETs) [5,6], nanoelectromechanical systems [7], molecular sensors [8], graphene-based luminescent diodes [9], and solar cells [10,11], have been reported. The simplest and most common approach for the fabrication of GFETs is to borrow mature microelectronic technology. This technology requires the deposition of large and uniform graphene thin films on a Si substrate in order to form a back gate. However, it is a challenge to synthesize low-defect and structurally continuous graphene monolayers or oligolayers; this represents a major limitation for the rapid adoption of high-quality GFET applications. Graphene can be deposited on Si using the widely studied stripped method [12], cut-and-choose transfer printing [13], the epitaxial method [6,14], chemical vapor deposition (CVD) [15], and other methods [16,17]. The former two methods are very complex and increase the risk of impurities, which negatively affect transistor performance. Herein, for the rapid preparation of high-quality graphene films and GFETs, we adopt a low-pressure, rapid CVD technology. The surface morphology, structure, carrier concentration, and carrier mobility of the resultant graphene films are systemically studied. In addition, the transport properties of the GFET, such as transconductance, $g_m$, ratio of current switch, $I_{on}/I_{off}$, and current saturation characteristics, are analyzed. Finally, the carrier transport mechanism in the GFET is discussed.

Methods
Figure 1 illustrates the structure of the graphene/Si field-effect transistors. Graphene acts as a local gate positioned on a highly doped n-type Si substrate separated by a 300-nm-thick thermal layer of silicon oxide. The oligolayered graphene film was fabricated using a rapid chemical vapor deposition process. The growth system comprises a large horizontal quartz tube furnace, a vacuum system, a gas meter, and a temperature controller. The n-type Si(100) substrates were ultrasonically cleaned with a sequence of acetone, ethanol, and deionized water, then dried with flowing $N_2$, and placed at the center of the furnace. Prior to deposition, the furnace was evacuated to $10^{-2}$ Pa, heated to 300°C, and maintained at this temperature for 30 min to remove any moisture from the mixture. The furnace was then heated to 700°C for the deposition. A 300-$\mu m$ SiO$_2$ layer

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was thermally oxidized for 30 min using high-purity oxygen gas followed by annealing at 900°C for 40 min. The source and drain sections were formed by doping the Si with B atoms via exposure to an Ar gas flow carrying an analytically pure C₃H₉BO₃ doping agent into the reactive chamber at 900°C for 20 min, followed by annealing at 950°C for 30 min. After doping, a mixture of CH₄ gas (99.999%) and Ar gas at a volume ratio of 1:10 was introduced into the reaction chamber at the same temperature (950°C). CH₄ decomposed to give a mixture of C, H⁺, and H₂ when the vapor-phase CH₄ and Ar gases flowed through the furnace; the C atoms condensed on the Si substrates to form the graphene film under a working pressure of 50 Pa. The growth process was carried out for 2 min, and the samples were then annealed at 1,000°C for 30 min. To observe the surface morphology and structure of the graphene film, a few graphene reference samples were concurrently deposited. Subsequently, the graphene film was capped with a 300-μm SiO₂ layer, and the graphene and SiO₂ layers above the source and drain sections were removed. Finally, the GFET was completed by depositing Al electrodes on the gate, source, and drain sections via evaporation. The morphologies and structures of the samples were characterized using optical microscopy, atomic force microscopy (AFM), and Raman spectroscopy. The electronic properties were assessed via Hall effect measurement (HMS-3000) and micro-current (4200, Keithley, Cleveland, OH, USA) measurements.

Results and discussion

Figure 2a shows an optical microscopy image of the graphene deposited on the Si substrate. It is evident that many graphene slices or islands of about 10 μm in diameter are uniformly scattered on the substrate. Figure 2b is an enlarged picture of the graphene film obtained via AFM. The large-area graphene film has a smooth and uniform surface free of carbon clusters. The film is about 2-nm thick, which is equal to a few layers of graphene. From Figure 2, we can confirm that the growth of the graphene film is characteristic of the layer-island mode. C atoms from the decomposition of CH₄ at 950°C (the decomposition temperature of CH₄ is about 900°C) absorbed, condensed, and formed islands on the Si substrate. The graphene film was formed by the combination of many islands over time.

Figure 3a shows the Raman spectrum of the graphene film, which contains two major scattering peaks: a 2D-band peak at 2,690 cm⁻¹ and a G-band peak at 1,590 cm⁻¹. The intensity ratio of the peaks (I₂D/I_G) is 14, which confirms that the graphene film comprises a few layers and is of high quality. The surface carrier concentration, carrier mobility, and current–voltage (I-V) properties of the graphene film were determined via Hall effect measurements. The carrier concentration of the samples is about 10¹⁰ cm⁻², while the electron mobility is 5.1 × 10⁴ cm² V⁻¹ s⁻¹, which is very close to the known ideal value of 2 × 10⁵ cm² V⁻¹ s⁻¹ [3,4]. The surface I-V behavior of the graphene film is shown in Figure 3b. Clearly, the graphene surface shows a linear current–voltage relationship, which suggests good transport of electrons on the graphene film. For the Hall effect measurements, four measuring pole points are arranged in a square on the
graphene surface. The I-V behaviors presented in Figure 3b indicate the relationships between the measured points. Since graphene film is a highly conductive material [18], electrons in graphene have high mobility. The voltage between two points changes in a linear relationship with the applied current, which closely obeys Ohm’s law.

The gate current, \( I_g \), versus gate voltage, \( V_g \), behavior of the graphene/Si transistor is shown in Figure 4a. Remarkably, the device shows good rectification properties. The current increases exponentially with the applied positive voltage but is almost zero under the revised voltage. This shows that the GFET device does not have any significant gate leakage. Figure 4b shows the drain current, \( I_{ds} \), versus the source-drain voltage, \( V_{ds} \), under different gate voltages; the GFET exhibits a nearly linear plot when \( V_{ds} \) is less than 2.5 V for different gate voltages. As \( V_{ds} \) increases above 2.5 V, \( I_{ds} \) tends towards saturation. The results indicate that the I-V plot for a \( V_g \) of 4 V is optimal as a ratio of current switch, \( I_{ds}/I_{ds} \), of 100 is obtained. Moreover, the GFET has a smaller threshold voltage, and the \( I_{ds}-V_{ds} \) plots of the graphene transistor show significant current saturation characteristics, which is typical of Si FETs but rare for GFETs. It has been suggested that the velocity saturation of the carrier at higher biases may lead to the current saturation phenomenon in graphene transistors [19].

The saturation velocity depends on the charge carrier concentration and scattering by interfacial phonons in the SiO\(_2\) layer that supports the graphene channels [20,21]. The achieved current saturation of the GFET makes this device well suited for analog applications. These results demonstrate the feasibility of two-dimensional graphene devices for analog and radio-frequency circuit applications without the need for bandgap engineering.

Moreover, we determined the transfer characteristics of \( I_{ds} \) versus \( V_g \) at a \( V_{ds} \) value of 1 V (Figure 5a). The plot clearly shows that the graphene transistor can be modulated via the local graphene gate within the range of -2 to 3.5 V, which demonstrates that graphene can act as an effective gate for graphene transistors. Figure 5b shows the measured electron transconductance, \( g_m \) (where \( g_m = \partial I_{ds}/\partial V_{ds} \)), of the GFET as a function of the gate voltage. A peak transconductance of 3 mS/\( \mu m \) was obtained at a \( V_{ds} \) value of 1 V in this
The authors declare that they have no competing interests.

Conclusions

High-performance graphene/Si transistors were fabricated by rapid chemical vapor deposition. The electron mobility of the graphene film is $5.1 \times 10^4$ cm$^2$ V$^{-1}$ s$^{-1}$, the scaled transconductance of the graphene transistors exceeds 3 mS/um, and the ratio of the current switch, $I_{on}/I_{off}$, is as high as 100. The fabricated GFET shows current saturation characteristics which demonstrate that two-dimensional graphene devices can be used for analog and radio-frequency circuit applications without the need for bandgap engineering.

Competing interests

The authors declare that they have no competing interests.

Authors’ contributions

XM designed the structure of the graphene transistor, analyzed the results, and wrote the manuscript. WG participated in the fabrication of the graphene film on the substrate. JS fabricated the drain, source, and gate of the transistor and participated in the analysis of the results of the transistor. YT measured the electrical properties of the transistor. All authors read and approved the final manuscript.

Authors’ information

XM is a professor and PhD degree holder specializing in semiconductor materials and devices, specially expert in nano-scaled optical-electronic materials and optoelectronic devices. WG is a graduate student major in fabrication of new semiconductor nanometer materials. JS is a lecturer and PhD degree holder specializing in semiconductor devices. YT is an engineer specializing in optoelectronic measurements.

Acknowledgments

This work was supported in part by the National Natural Science Foundation of China (no. 60976071) and the Scientific Project Program of Suzhou City (no. SYG201121).

Received: 12 October 2012 Accepted: 1 December 2012 Published: 17 December 2012

References

1. Novoselov KS, Geim AK, Morozov SV, Jiang D, Zhang Y, Dubonos SV, Grigorieva IV, Firsov AA: Electric field effect in atomically thin carbon films. Science 2004, 306:666.
2. Geim AK, Novoselov KS: The rise of graphene. Nat Materials 2007, 6:183.
3. Williams JR, Carlo LD, Marcus CM: Quantum Hall effect in a gate-controlled p-n junction of graphene. Science 2007, 317:638.
4. Novoselov KS, Jiang Z, Morozov SV, Zhang Y, Morozov SV, Stormer HL, Geim AK: Room-temperature quantum Hall effect in graphene. Science 2007, 315:1379.
5. Lin YM, Jenkins KA, Vaides GA, Small JP, Farmer DB, Avouris P: Operation of graphene transistors at gigahertz frequencies. Nano Lett 2009, 9:426.
6. Lin YM, Dimitrakopoulos C, Jenkins KA, Farmer DB, Chiu HY, Grill A, Avouris P: 100 GHz transistors from wafer-scale epitaxial graphene. Science 2010, 327:662.
7. Lin YM, Vaides GA, Han SJ, Farmer DB, Melic I, Sun Y, Wu YQ, Dimitrakopoulos C, Grill A, Avouris P, Jenkins KA: Wafer-scale graphene integrated circuit. Science 2011, 332:1294.
8. Cohen KT, Qing Q, Li Q, Fang Y, Lieber CM: Graphene and nanowire transistors for cellular interfaces and electrical recording. Nano Lett 2010, 10:1098.
9. Chung K, Lee C, Yi GC: Transferable GaN layers grown on ZnO-coated graphene layers for optoelectronic devices. Science 2010, 330:560.
10. Li X, Zhu H, Wang K, Cao A, Wei J, Li C, Jia Y, Li X, Wu D: Graphene-on-silicon Schottky junction solar cells. Adv Mater 2010, 22:2743.
11. Jo G, Na S, Oh S, Lee S, Kim TS, Wang G, Choe M, Park W, Yoon J, Kim DY, Kohng YH, Lee T: Tung of a graphene-electrode work function to enhance the efficiency of organic bulk heterojunction photovoltaic cells with an inverted structure. Appl Phys Lett 2010, 97:213303.
12. Kim SK, Zhao Y, Jang H, Lee SY, Kim JM, Kim KS, Ahn JH, Kim P, Choi JY, Hong BH: Large-scale pattern growth of graphene films for stretchable transparent electrodes. Nature 2009, 457:766.
13. Liang XS, Fu ZL, Chou SY: Graphene transistors fabricated via transfer-printing in device active-areas on large wafer. Nano Lett 2007, 7(12):3840–3844.
14. Berger C, Song Z, Li X, Wu X, Brown N, Naud C, Mayou D, Li T, Hass J, Marchenkov AN, Conrad EH, First PN, de Heer WA: Electronic confinement and coherence in patterned epitaxial graphene. Science 2006, 312:1191.
15. Dreyer DR, Park S, Bielawski CW, Rudolf RS: The chemistry of graphene oxide. Chem Soc Rev 2010, 39:228.
16. Reina A, Jia XT, Ho J: Large area, few-layer graphene films on arbitrary substrates by chemical vapor deposition. Nano Lett 2009, 9:30.
17. Bae S, Kim H, Lee Y, Xu X, Park JS, Zheng Y, Balakrishnan J, Lei T, Kim HR, Song YI, Kim YJ, Kim KS, Ozyilmaz B, Ahn JH, Hong BH, Iijima S: Roll-to-roll production of 30-inch graphene films for transparent electrodes. Nat Nanotech 2010, 5:574.

Figure 5 The drain-source current, $I_{ds}$ versus top gate voltage ($V_g$), and the electron transconductance, $g_m$ (b).
18. Yang Z, Gao R, Hu N, Chai J, Cheng Y, Zhang L, Wei H, Kong ESW, Zhang Y: The prospective two-dimensional graphene nanosheets: preparation, functionalization, and applications. Nano-Micro Lett 2011, 4:1–9.

19. Meric I, Han MY, Young AF, Ozylmaz B, Kim P, Shepard KL: Current saturation in zero-bandgap, top-gated graphene field-effect transistors. Nat Nanotech 2008, 3:654.

20. Fratini S, Guinea F: Substrate-limited electron dynamics in graphene. Phys Rev B 2008, 77:195415.

21. Chen JH, Jang C, Xiao S, Ishigami M, Fuhrer MS: Intrinsic and extrinsic performance limits of graphene devices on SiO2. Nat Nanotech 2008, 3:206.

22. Lin YM, Chiu HY, Jenkins KA, Farmer DB, Avouris P, Valdes GA: Dual-gate graphene FETs with fT of 50 GHz. IEEE Electron Device Lett 2010, 31:68.

doi:10.1186/1556-276X-7-677

Cite this article as: Ma et al. Investigation of electronic properties of graphene/Si field-effect transistor. Nanoscale Research Letters 2012, 7:677.