Upset and damage mechanisms of the three-dimensional silicon device induced by high power microwave interference

Yang Li¹, Changchun Chai¹, Yuqian Liu¹, Yun Li¹, Han Wu¹, Wei Zhang¹, Fuxing Li¹, and Yintang Yang¹

Abstract The paper clearly reveals the mechanism of upset (bit error) and damage caused by high power microwave (HPM) interference for the three-dimensional silicon device. The 0.35μm process related three-dimensional model of two stages cascaded CMOS inverters is established for the first time utilizing semiconductor device simulator Sentaurus-TCAD to comprehensively study the HPM interference mechanism. Moreover, a detailed mechanism about the upset induced by HPM interference is performed. Furthermore, the process and mechanism of damage generated by HPM interference are explored by using this model. The dependences of the damage power threshold P and damage energy threshold E on the pulse-width τ are both in negative exponential relationship. The simulation results in this paper have a good coincidence with the experimental results.

Keywords: three-dimensional silicon cascaded CMOS inverters, HPM interference, bit error, damage effect, pulse-width effect

Classification: Electron devices, circuits and modules (Silicon)

1. Introduction

The integrated circuits (ICs), components and systems are increasingly susceptible to the HPM interference with the advancement of semiconductor process technology. The interference is easy to be coupled into IC systems through front-door (such as receiver antennas, etc.) and back-door (such as power wires, transmission cables, etc.), thereby affecting normal operation of the whole circuit system [1, 2, 3, 4, 5]. In recent years, several experimental and theoretical researches about HPM interference effect of ICs have been carried out [6, 7, 8, 9]. In terms of CMOS circuits and devices. The experiment indicates that HPM interference can cause upset for inverters, and the upset can propagate to subsequent stage inverters [10, 11]. Previous study reveals the physical mechanism of inverter’s latch-up effect induced by excessive carrier injection and the relationship between self-recovery process and HPM interference [12]. Yu et al. and Liu et al. reported the HPM damage mechanism for high electron mobility transistor [13, 14]. The CMOS inverter soft logic flip model is obtained in the Ref. [15]. Chen and Du theoretically revealed the influences of some HPM parameters on the performance of CMOS inverter [16, 17]. Yu et al. analytically discussed and deduced the effects of HPM frequency, HPM pulse-width and temperature on CMOS inverter by analyzing fundamental physical parameters [18, 19, 20]. For other types of circuits and devices, Ma et al. and Chai et al. explained the failure mechanism induced by HPM of bipolar transistor and proposed several protective measures [21, 22, 23, 24, 25]. However, some theoretical analysis of CMOS inverter and their associated circuits under the influence of HPM interference still need to be further solved, such as bit error and damage.

This paper reveals the mechanism of upset and damage of HPM interference for cascaded CMOS inverters. The remainder of this paper is organized as follows. In the section 2, a three-dimensional model of two stages cascaded CMOS inverters is established. Section 3 describes some numerical model applied to the simulation. In the section 4, the mechanism of bit error and damage are revealed. The pulse-width effect is obtained in the section 5. Section 6 provides the conclusion.

2. Structure model

The three-dimensional schematic diagram of two stages cascaded CMOS inverters is depicted in Fig. 1(a). The sectional views of PMOS region and NMOS region are shown in Fig. 1(b) and Fig. 1(c), respectively. P is the substrate region of the device where the doping method is uniform doping with doping concentration of 1×10¹⁷ cm⁻³. N well represents N-well region where the doping method is uniform doping with doping concentration of 1×10¹⁷ cm⁻³. N⁺ and N⁻ are the NMOS drain of the device where the doping method is Gauss doping with surface doping concentration of 1×10¹⁹ cm⁻³, respectively. N⁺ is a common source of NMOS where the doping method is Gauss doping with surface doping concentration of 1×10¹⁹ cm⁻³, P⁺ and P⁺ are PMOS drain of the device where the doping method is Gauss doping with surface doping concentration of 1×10¹⁹ cm⁻³, etc.
respectively. $P$ is a common source of PMOS where the doping method is Gauss doping with surface doping concentration of $1 \times 10^{19}$ cm$^{-3}$. The thermal electrode is specified at the bottom of the device, where the lattice temperature maintains at 300 K. In addition, several structural parameters including total lateral length, substrate thickness, lateral length and depth of N well are also illustrated in Fig. 1. the transient simulation result of two stages cascaded CMOS inverters operating at 5 V supply voltage is indicated in Fig. 2. Out1 is the output of first stage inverter, Out2 is the output of subsequent stage inverter. The $V_{OH}$ and $V_{OL}$ represents output high threshold voltage and output low threshold voltage, respectively. The $V_M$ represents switching threshold.

![Fig. 1. (a) The three dimensional view of two stages cascaded CMOS inverters. (b) Sectional view of PMOS region. (c) Sectional view of NMOS region.](image)

![Fig. 2. The transient simulation result of two stages cascaded CMOS inverters.](image)

### 3. Numerical model

To investigate the physical effect and mechanism of bit error and damage, it is necessary to use the semiconductor device simulator Sentaurus-TCAD to solve the Poisson equation and the carrier-continuity equation. Owing to the high bias voltage and current of the device during injecting the interference signal, the thermodynamic model is used to solve the physical quantity inside the device, the current density equations of electron $J_e$ and hole $J_h$ are modified to

$$ J_e = -nq\mu_e (\nabla \phi_e + P_e \nabla T) $$  \hspace{1cm} (1)

$$ J_h = -nq\mu_h (\nabla \phi_h + P_h \nabla T) $$  \hspace{1cm} (2)

Considering the self-heating effect inside the device, it is necessary to solve the following equation

$$ \frac{\partial T}{\partial t} - \nabla \cdot k \nabla T = -\nabla \cdot [(P_e + \phi_e) J_e + (P_h + \phi_h) J_h] - (E_c + \frac{3}{2} k_b T) \nabla \cdot J_e $$  \hspace{1cm} (3)

where $\mu_e (\mu_h)$ is the electron (hole) mobility, $\phi_e (\phi_h)$ is the electron (hole) quasi-Fermi potential, and $P_e (P_h)$ is the absolute thermoelastic power electron (hole), $c$ is lattice heat capacity, $k$ is thermal conductivity, $k_b$ is Boltzmann constant, $E_c$ and $E_F$ are top of conduction band and bottom of valence band, respectively.

Besides, the effect of the internal temperature of the three-dimensional device on carrier generation-recombination process needs to be taken into account. The carrier generation-recombination process considers carrier avalanche generation, SRH and Auger recombination on which it takes the effect of doping concentration and temperature. An avalanche model named van Overstraeten-de Man model [30] is used to describe the generation process of the electron-hole pair, and avalanche generation rate $G$ is

$$ G = \alpha_{nv} + \alpha_{nv} $$  \hspace{1cm} (4)

Where $v_e (v_p)$ is the electron (hole) drift velocity, $a_{nv}$ ($a_{np}$) is the electron (hole) ionization rate, $\alpha(E)$ and $\gamma$ are given by

$$ \alpha(E) = \frac{\exp(yb/|\nabla \phi|)}{y} $$  \hspace{1cm} (5)

$$ \gamma = \frac{h\omega}{2kT_a}/\frac{\tan(h\nu_0/2kT_a)}{\tan(h\nu_0/2kT_a)} $$  \hspace{1cm} (6)

Where $h\omega_{0p}$ is optical phonon energy, $\nabla \phi$ is the quasi-Fermi potential, the $a$ and $b$ are the default coefficients in the model.

In this study, the HPM interference signal model is equivalent to a sinusoidal signal, the mathematical expression is as follows:

$$ U = U_0 \sin(2\pi ft + \phi) $$  \hspace{1cm} (7)

where $U_0$ is the amplitude, $f$ is the frequency, and $\phi$ is the initial phase.

### 4. Results and discussion

#### 4.1 Mechanism of upset under the injection of input port

In the section, the mechanism of this upset called bit error is explored. Figure 3 shows that a schematic diagram of injecting HPM interference into the two stage cascaded CMOS inverters. According to the Ref. [26], the external pulsed interference that is assumed to be sinusoidal wave and has been proved to be reasonable in the experiment. The waveform injected into the input port is illustrated in Fig. 4. In the experiment, Kim et al. injected the HPM interference from high power microwave sources into the input port of the device [27]. The experimental result is as shown in Fig. 5. There are some spikes appear, and they occurring in one
The operational cycle of the inverters don’t change the logic state of inverters to produce logic errors. These spikes are divided into bit error, bit-flip error and noise, which peak value exceeds the switch threshold $V_m$ but does not reach $V_{OH}$ or $V_{OL}$ are called bit error, the peak value is flipped from $V_{OH}$ to $V_{OL}$ or vice versa is called bit-flip error, others are noise. The bit error and bit-flip error are more harmful to the digital circuits than noise among these spikes.

![Fig. 3. Schematic diagram of the circuit with the input injection.](image)

![Fig. 4. The waveform of injected HPM interference at the input port.](image)

![Fig. 5. The voltage transfer characteristic about cascaded CMOS inverters with 1 GHz HPM interference are reported in Ref. [27].](image)

The phenomenon of the upset (bit error, bit-flip error) is analyzed from the voltage transfer characteristic curve. The load curves of NMOS and PMOS in static CMOS inverter are plotted in Fig. 6(a), and according to the Fig. 6(a), the voltage transfer characteristic curve of CMOS inverter can be obtained as shown in Fig. 6(b). We take the first bit-flip error in Fig. 5 as an example to analysis. It is assumed that the NMOS and PMOS are both in the cut-off area at 0.5 V and 5 V, respectively. When HPM interference is on, it is assumed that $V_{in}$ (the gate of first stage inverter) will increase from 0.5 V to 5 V, as shown in Fig. 7(a), the NMOS load curve moves up from $V_{in} = 0.5$ V to $V_{in} = 5$ V and the PMOS load curve moves down from $V_{in} = 0.5$ V to $V_{in} = 5$ V. Therefore, DC operating point will move to left, the output voltage will drop, which result in bit-flip error in Figure 7(b). The mechanism explanation of bit error and noise is similar to bit-flip error, so the bit error, bit-flip error and noise in the CMOS inverters are caused by DC operating point drift under HPM interference.

![Fig. 6. (a) The load curves of NMOS and PMOS in static CMOS inverter ($V_{dd} = 5$ V). Dots represent DC operating points at various input voltages ($V_{in} = 0$ V, 1 V, 2 V, 3 V, 4 V, 5 V). (b) The voltage transfer characteristic curve of inverter is derived from Fig. 6(a).](image)

![Fig. 7. (a) Schematic diagram of the DC operating point drift. (b) The schematic diagram of bit-flip error.](image)

According to the previous analysis, in order to study the distribution of carriers inside the device when DC operating point drift occurs. In the simulation, the sinusoidal voltage signal with a frequency of 1 GHz and an amplitude of 5 V is injected directly into the input port of the three-dimensional device. The mechanism of upset (bit error, bit-flip error) produced by DC operating point drift can be clearly explained by comparing the variation on carrier density of the device with and without interference. In the transient simulation, when the input ($V_{in}$) is in low-level input voltage, and in the absence of HPM interference, as shown in Fig. 8(a) and Fig. 8(b). For the first stage inverter, the electron density of NMOS channel and the hole density of PMOS channel is relatively low and high, respectively. For the subsequent stage inverter, the electron density of NMOS channel is relatively high, the hole density of PMOS channel is relatively low. However, when HPM interference is on, as shown in Fig. 8(c) and Fig. 8(d), the carrier densities of NMOS channel and PMOS channel are opposite to the situation of no HPM interference, respectively. This indicates that interference can change electric field, which affects the carrier...
density of NMOS channel and PMOS channel, thereby resulting in the DC operating point drift and forming bit error and bit-flip error. Hence, whether it is bit error, bit-flip error or noise, such behavior is clearly related to carrier density variation in the channel.

The schematic of on-chip measurement set-up is shown in Fig. 9. The HPM interference signal is generated by the network analyzer (e.g. HP8753C). The normal DC input $V_{DC}$ and power supply $V_{dd}$ is produced by semiconductor parameter analyzer (e.g. HP4145B). And the test chip should be designed and fabricated specially: the input and output of the cascaded CMOS inverters should have coplanar waveguides in ground-signal-ground (GSG) configuration. The two kinds of signal (DC input and HPM interference) are coupled into test-chip through Bias-T, and the voltage transfer characteristic curves of the two stage cascaded CMOS inverters are measured by the monitor unit Out1 and Out2 in the semiconductor parameter analyzer.

**Fig. 8.** The distributions of carrier density about NMOS channel and PMOS channel. (a) Two NMOS channels without interference. (b) Two PMOS channels without interference. (c) Two NMOS channels with interference. (d) Two PMOS channels with interference.

**Fig. 9.** Schematic of on-chip measurement set-up.

### 4.2 Damage effect and mechanism under the injection of GND port

In the section, the damage process is explored when the HPM interference is injected directly into the GND port. A schematic representation of the two stages cascaded inverters with injection of HPM interference into the GND port is shown in Fig. 10. The interference waveform is continuous sinusoidal wave, and the sinusoidal voltage signal with a frequency of 1 GHz and an amplitude of 10 V is used to study the damage process by injecting directly into the GND port of the device. Figure 11 shows the variation of the peak temperature of the device with time from 0 ns to 6 ns. Obviously, the internal maximum temperature of the device exhibits a periodic variation of “rise-fall” with the time. The maximum temperature decreases in the positive half-period, while in the negative half-period, there is a trend of increasing. Over-all, the maximum temperature rises until it reaches the melting point of silicon at 1688 K.

**Fig. 10.** Schematic diagram of the circuit with the source injection.

**Fig. 11.** The variations of interference waveform and peak temperature with time.

The external NMOS part current density and temperature distribution of the device is shown in Fig. 12(a) when the excitation is positive half-period peak. In the positive half-period, the electric potential of source (GND) is higher than the electric potential of substrate, which causes PN junction is in a reverse bias state. Reverse bias current (10$^6$ A·cm$^{-2}$) is in low level extremely compared to forward current. In addition, due to the low doping concentration of the substrate, the PN junction formed by the source and the substrate is not sufficient to generate an avalanche effect, resulting in the current density is in low level. The power is determined by electric field and current, although there is a strong electric field exists, its power still remains at a low level, which causes heat generation less than heat dissipation. Therefore, the peak temperature decreases inside the device. The external NMOS part current density and temperature distribution of the device is shown in Fig. 12(b) when the excitation is negative half-period peak. In the negative half-period, the source and substrate is in forward-bias, which causes the large forward current (10$^7$ A·cm$^{-2}$) from source to substrate. Generating a large
amount of Joule heat, the heat generation is greater than heat dissipation. Therefore, the peak temperature increases inside the device. In addition, the radius of curvature at the space charge region formed by the source and the substrate near the gate is larger, so the current density near gate are higher. Therefore, the peak temperature (730K) of device is near the edge of GND port. If the power which is injected into the device is sufficiently large, the temperature inside the device can reach the melting point of silicon material (1688K) during the action of HPM interference, causing partial burnout of the device and resulting in irreversible physical damage to the device. Figure 13(a) shows the distribution of temperature inside the device at burning time. There is only one damage point which is in the source of NMOS near the gate of first stage inverter. Moreover, the experiment result also shows that the primary destruction about CMOS inverters is to inverter gate on the source (Vdd and GND) sides (see in Fig. 13(b)) [29]. Therefore, the simulation result in the section is in line with experiment result, and the model could be used to analyze the damage effect induced by the high power microwave interference well.

**Fig. 12.** The distribution of temperature and current density. (a) $t = 4.25$ ns, (b) $t = 4.75$ ns.

**Fig. 13.** (a) The distribution of temperature inside the device at burning time. (b) Reported surface microscopy of HC-CMOS inverter after injecting HPM interference from back-door in Ref. [29].

### 5. Pulse-width effect with the HPM injection

This section provides a good prediction of the CMOS device damage and a guiding significance for HPM destruction, the sinusoidal voltage signal with a frequency of 1 GHz and different amplitudes are used to study the pulse-width effect by injecting directly into the GND port. The dependences of the damage power threshold $P$ and the damage energy threshold $E$ on the pulse-width $\tau$ under the GND port are obtained. In this section, the pulse-width $\tau$ is defined as the duration of injected HPM interference signal before the device is burned down, the damage power threshold $P$ and the damage energy threshold $E$ are average power and total injection energy, respectively. The variation of damage power threshold $P$ and damage energy threshold $E$ under the injection of GND port are shown in Fig. 14. The pulse-width versus damage power threshold $P$ and damage energy threshold $E$ obey the following formulas:

$$P = 37.2e^{-0.107}$$  \hspace{1cm} (8)

$$E = 1.22e^{-0.47}$$  \hspace{1cm} (9)

The Eq. (8) and Eq. (9) are obtained by fitting, and the correlation coefficients of Eq. (8) and Eq. (9) are 0.95 and 0.99, respectively. Moreover, the damage thresholds ($P$ and $E$) are in line with the classic Wunsch-Bell relationship [28].

**Fig. 14.** The damage power threshold $P$ and damage energy threshold $E$ versus pulse-width with the GND port injection.

### 6. Conclusion

A three-dimensional model of two stages cascaded CMOS inverters is established to study the mechanism of upset and damage induced by HPM interference. The simulation and theoretical analysis concentrating on the HPM interference induced upset in this model are presented firstly. This kind of upset called bit error is directly caused by carrier density variation of the NMOS and PMOS in these inverters under the effect of the interference electric field, which result in DC operating point drift of these inverters, forming bit error. In addition, a detailed investigation of process and mechanism about damage caused by HPM interference is performed by analyzing the distribution of current density and temperature inside the device. The analysis reveals that temperature elevation process appears in the negative half of every interference period, the temperature decreases in the positive half-period. It is due to the difference in current density under strong...
electric field. There is only one hot point which locates near the edge of GND port and the gate of first stage inverter. Moreover, the dependences of damage power threshold $P$ and damage energy threshold $E$ on pulse-width $t$ are obtained, respectively. And the relationships of damage thresholds ($P$ and $E$) with pulse-width $t$ are in line with classic Wunsch-Bell relationship [28]. These simulation results are supported by the reported experimental results. These findings in this paper provide an in-depth understanding of the upset and damage induced by HPM interference in cascade CMOS inverters.

References

[1] Backstrom M G and Lovstrand K G: “Susceptibility of electronic systems to high-power microwaves: summary of test experience,” IEEE Transactions on Electromagnetic Compatibility, Vol. 46, No. 3, (2004) 396 (DOI: 10.1109/TEMC.2004.831814)

[2] G. V. Rao, et al.: “Electromagnetic interference by high power microwaves,” International Conference on Electromagnetic Interference and Compatibility. (2002) (DOI: 1.1109/ICEMIC.20
02.1006455)

[3] R. Przesmycki and M. Wnuk.: “Susceptibility of IT devices to HPM pulse,” Safety and Security Eng. Vol. 8, pp. 223-233, (2018) (DOI: 1.2495/SAFE-V8-N2-223-233)

[4] H. L. You, et al.: “Research on CMOS inverter latch-up triggered by nMOS channel capacitance under HPM interference,” IEEE 116. International Conference on Solid-State and Integrated Circuit Technology. (2012) (DOI: 10.1109/ICSCIT.2012.646773)

[5] Ira Kohlberg.: “A stochastic process and chaos interpretation of HPE and HPM effects on electronic systems,” Asia-Pacific International Symposium on Electromagnetic Compatibility. (2010) (DOI: 10.1109/APEMC.2010.5475483)

[6] G. Goransson: “HPM effects on electronic components and the importance of this knowledge in evaluation of system susceptibility,” IEEE International Symposium on Electromagnetic Compatibility. (1999) (DOI: 10.1109/ISEMC.1999.812964)

[7] L. Zhou, et al.: “Investigation on Failure Mechanisms of GaN HEMT Caused by High-Power Microwave (HPM) Pulses,” IEEE Transactions on Electromagnetic Compatibility, Vol. 59, No. 3, (2017) 902-909 (DOI: 10.1109/TEMC.2016.2628046)

[8] F. Brauer, et al.: “Susceptibility of IT network systems to interferences by HPEM,” IEEE Transactions on Electromagnetic Compatibility. (2009) (DOI: 10.1109/EMC.2009.5284569)

[9] Michael A. Holloway, et al.: “Study of basic effects of HPM pulses in digital CMOS integrated circuit inputs,” IEEE Transactions on Electromagnetic Compatibility, Vol. 54, No. 5, (2012) (DOI: 10.1109/TEMC.2012.2188720)

[10] Kim K and Iliadis A A: “Latch-up effects in CMOS inverters due to high power pulsed electromagnetic interference,” Solid-State Electronics. Vol. 52, pp. 1589-1593, (2008) (DOI: 10.1016/j.sse.2008.06.041)

[11] Kim K and Iliadis A A: “Operational upsets and critical new bit errors in CMOS digital inverters due to high power pulsed electromagnetic interference,” Solid-State Electronics. Vol. 54 pp. 18-21 (2010) (DOI: 10.1016/j.sse.2008.06.041)

[12] Y. H. Zhang, et al.: “Investigation on latch-up susceptibility induced by high-power microwave in complementary metal-oxide-semiconductor inverter,” Chinese physics B. Vol. 26, No. 2, (2017) 028501 (DOI: 10.1088/1674-1065/26/2/028501)

[13] X. H. Yu, et al.: “Simulation and experimental study of high power microwave damage effect on AlGaAs/InGaAs pseudomorphic high electron mobility transistor,” Chinese physics B. Vol. 24, No. 4, (2015) 048502 (DOI: 10.1088/1674-1065/24/4/048502).

[14] Y. Liu, et al.: “Damage effect and mechanism of the GaAs high electron mobility transistor induced by high power microwave,” Chinese physics B. Vol. 25, No. 4, (2016) 048501 (DOI: 10.1088/1674-1065/25/4/048504)

[15] Y. Q. Liu, et al.: “Physics-based analysis and simulation model of electromagnetic interference induced soft logic upset in CMOS inverter,” Chinese physics B. Vol. 27, No. 6, (2018) 068505 (DOI: 10.1088/1674-1065/27/6/068505).

[16] J. Chen, et al.: “Device simulation studies on latch-up effects in CMOS inverters induced by microwave pulse,” Microelectronics reliability. Vol. 53 (2013) (DOI:10.1016/j.microrel.2012.10.012).

[17] J. Chen, et al.: “Understanding and modeling of internal transient latch-up susceptibility in CMOS inverters due to microwave pulses,” Microelectronics reliability. Vol. 53, pp. 1891-1896, (2013) (DOI:10.1016/j.microrel.2013.07.004).

[18] X. H. Yu, et al.: “Modeling and understanding of the frequency dependent HPM upset susceptibility of the CMOS inverter,” Science China Information Sciences. Vol. 58, pp. 1-11, (2015) 082402 (DOI: 10.1007/s11432-015-5323-9).

[19] X. H. Yu, et al.: “Modeling and analysis of the HPM pulse-width upset effect on CMOS inverter,” Journal of Semiconductors. Vol. 36, No. 5, (2015) (DOI:10.1088/1674-4926/36/5/054011)

[20] X. H. Yu, et al.: “Temperature dependence of latch-up effects in CMOS inverter induced by high power microwave,” Journal of Semiconductors. Vol. 35, No. 8, (2014) 084011 (DOI: 10.1088/1674-4926/35/8/084011).

[21] Z. Y. Ma, et al.: “The damage effect and mechanism of the bipolar transistor caused by microwaves,” Acta Physica Sinica. Vol. 61, (2012) 078501 (DOI: Y2012/V61/17/078501)

[22] Z. Y. Ma, et al.: “Microwave damage susceptibility trend of a bipolar transistor as a function of frequency,” Chinese physics B. Vol. 21, (2012) 098502 (DOI: 10.1088/1674-1056/21/9/098502)

[23] Z. Y. Ma, et al.: “Effects of microwave pulse-width damage on a bipolar transistor,” Chinese physics B. Vol. 21, (2012) 058502 (DOI: 10.1088/1674-1056/21/5/058502)

[24] Z. Y. Ma, et al.: “The pulsed microwave damage trend of a bipolar transistor as a function of pulse parameters,” Chinese physics B. Vol. 22, No. 2, (2013) 028502 (DOI: 10.1088/1674-1056/22/2/028502)

[25] C. C. Chai, et al.: “Hardening measures for bipolar transistors against microwave-induced damage,” Chinese physics B. Vol. 22, No. 6, (2013) 068502 (DOI: 10.1088/1674-1056/22/6/068502)

[26] S. Korte, et al.: “Hardware and software simulation of transient pulse impact on integrated circuits,” IEEE International Symposium on Electromagnetic Compatibility. P. 489 (2005) (DOI: 10.1109/ISEMC.2005.1513564)

[27] K. Kim.: “High power microwave interference effects on analog and digital circuit in IC’s;,” (Ph.D. Dissertation). P. 117-130 (2007)

[28] D. C. Wunsch, et al.: “Determination of threshold failure levels of semiconductor diodes and transistors due to pulse voltage,” IEEE Transactions on Nuclear Science. Vol. 15(6), P. 244-259, (1968) (DOI: 10.1109/TNS.1968.4325054)

[29] S. M. Hwang, et al.: “characterization of the susceptibility of integrated circuits with induction caused by high power microwaves,” Process in Electromagnetics Research. PIER 81, pp. 61-72, (2008) (DOI: PIER/pier81/04.07121704)

[30] R. van Overstraeten and H. de Man: “Measurement of Ionization Rates in Diffused Silicon p-n Junctions,” Solid-State Electronics, Vol. 13, No. 1, pp. 583-608, (1970) (DOI: 10.1016/0038-1101(70)90139-5)