Effect of Polymer Liners in Different Via Shapes: Impact on Crosstalk Induced Delay

Maya Chandrakar  
Dr Shyama Prasad Mukherjee International Institute of Information Technology

Manoj Kumar Majumder (✉ manojbesu@gmail.com)  
Dr Shyama Prasad Mukherjee International Institute of Information Technology

Research Article

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Effect of Polymer Liners in Different Via Shapes: Impact on Crosstalk Induced Delay

Maya Chandrakar · Manoj Kumar Majumder

Abstract

The performance of a through silicon via (TSV) based 3D integrated circuit technology is primarily dependent on the choice of an appropriate liner material. The most commonly used liner material SiO$_2$ is undergoing considerable reliability challenges such as coefficient of thermal expansion (CTE) mismatch, scallop formation, and interfacial delamination related problems. Therefore, TSVs employed with a polymer liner have achieved significant attention in recent years due to their low dielectric constant and excellent step coverage along the via surface that can effectively reduce thermal stress and crosstalk induced delay. This paper presents a comprehensive and accurate $RLGC$ model for different via shapes considering the impact of various liner materials on the crosstalk induced delay. Considering an accurate via geometry and material properties at 32 nm and 45 nm technology, the proposed equivalent $RLGC$ parameters include the cumulative effects of TSV metal, liner, bump, and the silicon substrate. The aforementioned parameters are used to model a novel $T$-type equivalent electrical network of cylindrical, tapered, and coaxial TSVs considering a coupled driver-via-load (DVL) setup. The proposed equivalent models of different via shapes are used to demonstrate the worst-case crosstalk induced delay in TSVs under the influence of various liner materials. Considering a tapered TSV, a significant improvement in crosstalk induced delay at 32 nm w.r.t. 45 nm technology is observed as 53.5%, 33.76%, and 19.12% at aspect ratios of 2.4, 3, and 4, respectively for the BCB liner.

Keywords Through Silicon Via (TSV) · Resistance-Inductance-Conductance-Capacitance ($RLGC$) · Driver-Via-Load (DVL) · Crosstalk Induced Delay · Coefficient of Thermal Expansion (CTE) · Miller Coupling Factor (MCF)

1 Introduction

Three-dimensional integrated circuits (3D ICs) have been proposed as a prospect for developing more-than-Moore technology. A Through Silicon Via (TSV) based three-dimensional integration has the capability to provide the highest vertical interconnect density while providing a compact footprint, enhanced efficiency, and heterointegration capacity [1,2]. TSVs with shorter interconnect lengths, and higher density primarily provides smaller form factor, lower power consumption, and higher bandwidth than wire bonding and micro-bump chip stacking techniques [3,4]. A cylindrical TSV is advantageous over the square, coaxial, and tapered TSVs due to its uniform structure, high breakdown voltage, and simplicity of electrical modelling. At low frequencies, it also outperforms other TSV structures in terms of heat dissipation [5]. However, the cylindrical TSV demonstrates a significant worst-case crosstalk induced delay and less conductivity compared to the other shapes due to more footprint area [5]. In this regard, a coaxial shaped TSV can be considered in terms of less footprint area and improved noise performance. Additionally, a coaxial TSV provides a reduced coupling with its surroundings due to the insulator based guard ring structure. However, as per the fabrication house, the formation of this guard ring between the inner and outer conducting filler is still a challenging task. Therefore, a tapered TSV is preferred due
to its straightforward fabrication, less footprint area, balanced power and thermal distribution in 3D ICs [5]. Additionally, the tapered TSV has a reduced electrical resistance [6], less reflection noise, and power loss. Apart from the different via shapes, it is equally important to choose an appropriate filler material for TSV. In general, copper (Cu) is preferred as via filler material for its silicon compatibility, straightforward fabrication and testing process [7]. However, the coefficient of thermal expansion (CTE) of Cu (16.5ppm/K) is significantly higher than that of silicon (Si) substrate (2.6ppm/K), and hence a CTE mismatch can occur between the Cu and Si. It results in Cu pumping and interfacial delamination that affects the overall performance of a TSV [8]. In this regard, polymer liners with lower CTE values, elastic modulus, dielectric constants, and more uniform thicknesses can be adopted in TSVs to prevent the thermal stress problem commonly encountered in Cu filled TSVs. The capacitive coupling of TSVs can be reduced by substituting polymer liner instead of silicon dioxide (SiO₂) liner that results in superior performance. Therefore, a proper TSV shape with an appropriate liner material is important for the analysis of via performance.

Previously, Savidis and Friedman [9] demonstrated the electrical modelling of cylindrical shaped TSVs to obtain closed-form expressions of resistance, inductance, and capacitance. However, a maximum difference of 8% between the results obtained from the closed-form expressions and the simulations have been observed. Afterwards, Katti et al. [10] encountered the difference while demonstrating the validity of the proposed RLC model using numerical simulators and experimental measurements. However, the suggested approach was only appropriate for the modeling of TSVs with small-geometries. Later, Gerakis and Hatzopoulos [11] proposed an Improved Transmission Line Model (ITLM) to compute the resistance and inductance of the cylindrical TSVs operating at high frequencies. However, the authors limited their discussion only to the cylindrical shaped TSVs. In order to address the other different via shapes, Xu and Lu [12] investigated the electrical performance of a coaxial TSV in terms of latency, crosstalk and power by considering the processing materials and physical geometries of the TSV configuration. Although the researchers addressed the via performance using a coaxial TSV but neglected the impact of a cylindrical and tapered shape. Afterwards, Su et al. [13] developed closed-form expressions based on Maxwell’s equations to calculate the capacitances of the insulator and substrate for a tapered shaped TSV. The results indicated that the tapered TSVs had a longer delay and less crosstalk than cylindrical TSVs. Moreover, the expressions were considered suitable for TSVs with a high aspect ratio (AR), and a maximum of 4% errors between the calculated and simulated results was observed. Later, Nabil et al. [14] addressed the error by presenting electrical modelling of tapered TSVs at high frequency using the Transmission Line Method (TLM). In the proposed electrical model, the authors have considered substrate coupling and MOS effects. Although detailed analyses have been performed for modelling of TSVs with different shapes but the impact of the coupling capacitance is constrained only to the SiO₂ liner. In recent, Murugesan et al. [15] used a TSV structure wherein a Polyimide (PI) liner with a low modulus value was employed instead of SiO₂ to reduce Cu extrusion, interfacial delamination, thermal stress between the TSV metal and the Si substrate, and the keep-out zone. However, the charge-trap density in the PI layer is relatively high that resulting in modulation of the parasitic capacitance existing between TSV metal and the Si substrate. Apart from this, Kino et al. [16] used Polybenzoxazole (PBO) as the polymer liner material of TSV to reduce the capacitance modulation. Subsequently, a Polypropylene Copolymer (PPC) liner was also used to further reduce the insulating capacitance of the TSV, which resulted in a 25% [17] and 30% [18] reduction in crosstalk compared to the conventionally used TSV structures. Later, Su et al. [19] proposed the development of low capacitance TSVs by replacing the SiO₂ liner layer with a Benzocyclobutene (BCB) polymer liner, as well as the reduction of thermal expansion stress and leakage current. Based on the above state-of-the-art research [9-19], it can be inferred that a comprehensive analysis of modelling of various TSV shapes with the impact of different liner materials is required to address. Moreover, a detailed investigation is required to apostrophize the worst case crosstalk induced delay of TSVs by taking all physical geometries into consideration.

In order to address the above-mentioned research problems, the paper, for the first time, presents electrical modelling of different TSV shapes along with the impact of liner materials to address the crosstalk performance. A crosstalk induced delay and noise can be demonstrated by Miller’s effect, according to which a victim line experiences an increased coupling capacitance when opposite input signals are sent to the neighbouring TSVs. Due to this, a voltage spike (peak noise) can be observed on the victim line that affects the TSV performance. In order to observe this phenomenon in a crosstalk, a closed-form expression is obtained for modelling of cylindrical, tapered, and coaxial TSVs. During the RLG model of the TSV, the influence of Metal Oxide Semiconductor (MOS) is also taken into account. The liner and depletion layers are used to insulate the TSV from the Si substrate that helps to reduce the crosstalk effect between neighbouring TSVs. Similarly, the Inter Metal Dielectric (IMD) layer isolates the bumps from the Si substrate to minimize leakage. An underfill layer is provided to separate the bumps to avoid cross-coupling and inter-bump leakage. Considering all the aforementioned facts, the crosstalk induced delay performance of a TSV pair is investigated in detail using a driver-via-load (DVL) setup wherein the TSVs are modelled using Cu as a filler material with several liner materials such as SiO₂, PI, PPC, PBO, and BCB. The equivalent circuits are modelled at the 32 nm and 45 nm technology employing a coupled DVL with a CMOS driver. The fundamental reason behind choosing the aforementioned technology parameters is
that the use of a liner beyond 32 nm increases the leakage and is hence inappropriate for low-power and high-performance applications. Additionally, the electrical circuit models are implemented using a specific $T$-type network. Due to such modelling of the via line, the capacitive charging current flows through half of the via line, which results in reduced crosstalk interference between the coupled TSVs.

The following is the structure of this paper: Section I provides an insight into the current state-of-the-art research situation and describes the modelling of differently shaped TSVs while considering the effects of polymer liners. The physical configuration of various TSV structures, the critical design parameters and their equivalent electrical models are presented in Section II. The detailed analytical equations for modelling cylindrical, tapered, and coaxial TSVs employing various liner materials are also developed in this section. Section III examines the impact of various liner materials in TSV, examining the impact of liners for different aspect ratios of TSV and the impact of liners in various TSV shapes. Finally, this work is summarized in Section IV.

2 TSV Configuration and Equivalent Model

This section includes the modelling configurations of cylindrical, tapered, and coaxial TSVs at 32 nm and 45 nm technology. Furthermore, a high-frequency equivalent electrical model of a TSV pair is presented for a variety of via shapes that consist of the effect of the liner, underfill layer and the bump. The analytical $RLGC$ model expressions are used to develop these models based on the $T$-type network with 20 distributed sections. Accurate physical parameters and material properties are used as variables in the analytical $RLGC$ equations. Consequently, novel equivalent electrical models of cylindrical, tapered, and coaxial TSVs are presented, considering the impact of various liner materials in the following sub-sections.

2.1 TSV Structure and Physical Configuration

This sub-section presents a thorough understanding of the TSV structure and quantitative values of physical parameters and material properties that are employed in the modelling of equivalent $RLGC$ models. The physical configurations of cylindrical, tapered, and coaxial TSVs are shown in Figs. 1 (a), 1(b), and 1(c), respectively. The $t_{\text{liner}}$, $d_{\text{TSV}}$, $t_{\text{dep}}$, and $h_{\text{TSV}}$ represent the thickness of the liner layer, TSV diameter, depletion layer thickness, and via height, respectively for cylindrical, tapered and coaxial shapes. For a tapered shaped TSV (shown in Fig. 1(b)), $\theta$, $r_1$, and $t_{\text{liner,1}}$ represent the slope angle, bottom radii of the TSV and the liner, respectively, whereas $t_{\text{liner,inner}}$ represents the thickness of the inner insulating layer of a coaxial TSV (shown in Fig. 1(c)).

Considering the different TSV shapes, Tables 1, 2 and 3 summarize the via physical parameters, material properties of TSV, liner and filler, respectively. In order to consider the MOS effect (shown in Fig. 1(d)), it is required to surround the TSV metal with a dielectric, such as a liner layer, to isolate the via filler from the Si substrate. TSV liner can be composed of SiO$_2$ or a variety of polymers such as PBO, BCB, PI, PPC, etc. Apart from this, a depletion layer is used to enhance the isolation between the TSV metal and the Si substrate to prevent inter-metal leakage. Lossless silicon is primarily utilized as the depletion layer, wherein the losses are at their lowest levels. Additionally, an Inter Metal Dielectric (IMD) layer is employed to minimize the leakage between the bump and Si substrate. An underfill layer, composed of anhydride resin polymers, is used to physically isolate the bumps while reducing cross-coupling and leakage. The bump comprises Cu as filler, is used to connect the TSVs with the functional block of the dies. Lossy silicon material is used as a substrate in this application.

![Fig. 1 Physical configurations of: (a) cylindrical, (b) tapered, (c) coaxial TSVs, and (d) MOS effect.](image-url)
2.2 Equivalent Electrical Model of TSV

This sub-section demonstrates the modelling of Cu based TSV by considering the geometry of tapered, cylindrical, and coaxial shapes (as shown in Fig. 1) along with different liner materials. Figures 2(a), 2(b), and 2(c) depict the structures and parasitics of a TSV pair of different shapes with connected bumps. The physical dimensions of via (presented in Table 1) are used to develop closed-form equations of RLGC parasitics of TSVs, as demonstrated in the following sub-sections.

### Table 1 Physical parameters of TSV at 32 nm and 45 nm technology nodes

| TSV parameter symbol | Description                                      | At 32 nm technology node | At 45 nm technology node |
|----------------------|--------------------------------------------------|--------------------------|--------------------------|
| \(d_{\text{TSV}}\)  | TSV diameter                                      | 4\(\mu m\)               | 5\(\mu m\)               |
| \(h_{\text{TSV}}\)  | TSV height                                        | 9.6\(\mu m\)             | 12\(\mu m\)              |
| \(t_{\text{liner}}\) | Liner thickness                                    | 0.1\(\mu m\)             | 0.1\(\mu m\)             |
| \(t_{\text{liner,bot}}\) | Bottom liner thickness                          | 0.1\(\mu m\)             | 0.1\(\mu m\)             |
| \(t_{\text{dep}}\)  | Depletion layer thickness                         | 0.02\(\mu m\)            | 0.05\(\mu m\)            |
| \(h_{\text{Bump}}\) | Bump height                                       | 0.835\(\mu m\)           | 1.25\(\mu m\)            |
| \(d_{\text{Bump}}\) | Bump diameter                                     | 5\(\mu m\)               | 7.5\(\mu m\)             |
| \(h_{\text{IMD}}\) | IMD layer height                                   | 5\(\mu m\)               | 5\(\mu m\)               |
| \(p_{\text{TSV}}\) | TSV pitch                                         | 15\(\mu m\)              | 20\(\mu m\)              |
| \(r_{b}\)          | Bottom radius of tapered TSV                      | 1\(\mu m\)               | 1.25\(\mu m\)            |
| \(d_{\text{inner}}\) | Inner diameter of coaxial TSV                     | 2.5\(\mu m\)             | 3.125\(\mu m\)           |
| \(t_{\text{ins,liner}}\) | Thickness of insulating liner of coaxial TSV     | 0.25 \(\mu m\)           | 0.3125 \(\mu m\)         |
| \(d_{\text{Bump,inner}}\) | Diameter of bump covered by inner part of coaxial TSV | 3.75 \(\mu m\)           | 4.6875 \(\mu m\)         |

### Table 2 Material properties of TSV

| Symbol | Description                     | Value                  |
|--------|---------------------------------|------------------------|
| \(\sigma_{Si}\) | Conductivity of silicon substrate | 10 [S/m]               |
| \(\sigma_{TSV}\) | Conductivity of TSV               | 5.9524\times10^7 [S/m] |
| \(\sigma_{Bump}\) | Conductivity of bump              | 5.9524\times10^7 [S/m] |
| \(\rho_{TSV}\) | Resistivity of TSV                | 1.68\times10^{18}[\Omega-m] |
| \(\rho_{Bump}\) | Resistivity of bump               | 1.68\times10^{18}[\Omega-m] |
| \(\varepsilon_{r, Si}\) | Relative permittivity of silicon substrate | 11.9                   |
| \(\varepsilon_{r, SiO_2}\) | Relative permittivity of SiO_2    | 3.9                    |
| \(\varepsilon_{r, IMD}\) | Relative permittivity of IMD      | 4                      |
| \(\varepsilon_{r, Underfill}\) | Relative permittivity of underfill | 7                      |
| \(\mu_{r, TSV}\) | Relative permeability of TSV      | 1                      |
| \(\mu_{r, Bump}\) | Relative permeability of bump     | 1                      |
Fig. 2 The structures and parasitics of a TSV pair of (a) tapered, (b) cylindrical, and (c) coaxial TSVs with connected bumps.

### 2.2.1 Equivalent Resistance

Using the accurate physical configurations (Shown in Fig. 1) of different TSV shapes, this sub-section demonstrates the modelling of equivalent resistance considering the physical geometries of TSVs. As shown in Fig.2, the equivalent electrical models of tapered, cylindrical, and coaxial TSVs are presented by following a 20-distributed T-type network.

When an induced electromagnetic field propagates along TSV metal and bumps and penetrates through the material surfaces, it causes equivalent resistance that represents the heat dissipation in TSV metal and bumps. Thus, the equivalent resistance ($R_{equ}$) can be defined as

$$ R_{equ} = r'_{equ} \times h_{TSV} $$

where $r'_{equ}$ is the p.u.h. equivalent resistance as shown in Fig. 2.

Considering a tapered TSV, the equivalent resistance ($R_{equ(T)}$) of Fig. 2(a) can be expressed as

$$ R_{equ(T)} = R_{equ1(T)} = R_{equ2(T)} = R_{TSV(T)} + R_{Bump(T)} (1) $$

The "skin effect" refers to the phenomenon in which high-frequency current flows near to the surface of a conductor due to the development of eddy current. Skin depth is obtained to model the TSV and bump resistances ($R_{TSV(T)}$ and $R_{Bump(T)}$) with a non-uniform current distribution at high frequencies. Therefore, $R_{TSV(T)}$ and $R_{Bump(T)}$ (mentioned in Eqn. (1)) can be expressed as

$$ R_{TSV(T)} = \sqrt{(R_{dc, TSV(T)})^2 + (R_{ac, TSV(T)})^2} $$

$$ and $$

$$ R_{Bump(T)} = \sqrt{(R_{dc, Bump(T)})^2 + (R_{ac, Bump(T)})^2} $$

where $R_{dc, TSV(T)} = \frac{\rho_{TSV} h (1+0.5\beta^2)}{\pi r_1 (r_1 + h \beta)}$ and $h = h_{TSV} - h_{IMD}$

and $R_{ac, TSV(T)} = \frac{1}{4\pi \beta \delta_{skin depth, TSV}} \rho_{TSV} (2 + \beta^2) \ln \left[ 1 + \frac{2 \beta}{2r_1 - \delta_{skin depth, TSV}} \right]$ (2b)

where $\delta_{skin depth, TSV(T)} = \frac{1}{\sqrt{\pi J/\mu_{TSV}}} \rho_{TSV}$ is the skin depth of tapered via.

$$ R_{Bump(T)} = \sqrt{(R_{dc, Bump(T)})^2 + (R_{ac, Bump(T)})^2} $$

and $R_{ac, Bump(T)} = k_p \left( \rho_{Bump} \times \frac{h_{Bump}}{\pi \times \left( \frac{d_{Bump}}{2} \right)^2} \right)$

where, $\delta_{skin depth, Bump(T)} = \frac{1}{\sqrt{\pi J/\mu_{Bump}}} \rho_{Bump}$, $k_p = \frac{p_{TSV}}{d_{TSV}} = \frac{p_{Bump}}{d_{Bump}}$ represent the skin depth of the bump and the proximity factor, respectively, and $\beta = tan \theta$, $\theta$ is taken as $15^\circ$ [13].

Similarly, for a cylindrical TSV, the equivalent resistance ($R_{equ(cyl)} = R_{equ1(cyl)} = R_{equ2(cyl)}$) can be obtained from Eqn. (1) by considering $\beta = 0$ and $r_1 = d_{TSV}/2$. Apart from this, for a coaxial TSV, the expression of inner equivalent resistance ($R_{equ in(c)} = R_{equ1 in(c)} = R_{equ2 in(c)}$) can be obtained using Eqn. (1) by considering $\beta = 0$, $d_{TSV} = d_{inner}$, $d_{Bump} = d_{Bump,inner}$, and $r_1 = d_{inner}/2$. Consequently, the outer equivalent resistance ($R_{equ out(c)} = R_{equ1 out(c)} = R_{equ2 out(c)}$) can also be obtained from Eqn. (1) by putting $\beta = 0$, and $r_1 = d_{TSV}/2$.

### 2.2.2 Equivalent Inductance

Inductance is a property of a conductor that opposes the sudden change in amplitude and direction of current when the current flows through it. Equivalent via inductance plays a key role for an increasing operating frequency. As shown in Fig. 2, the equivalent inductance ($L_{equ}$) can be expressed as

$$ L_{equ} = l'_{equ} \times h_{TSV} $$

where $l'_{equ}$ is the p.u.h. equivalent inductance as shown in Fig. 2.

As the current-carrying conductor (ex. TSV and bump) generates a magnetic field which results in the development of emf that resists the change of current flowing through the conductor. Hence, the TSV and bump inductances ($L_{TSV(T)}$ and $L_{Bump(T)}$) come into existence in TSV and bump,
respectively. Considering a tapered TSV, the equivalent inductance \( L_{equ(T)} \) of Fig. 2(a) can be expressed as
\[
L_{equ(T)} = L_{equ1(T)} = L_{equ2(T)} = L_{TSV(T)} + L_{Bump(T)}
\]
where \( L_{TSV(T)} \) and \( L_{Bump(T)} \) represents the inductances of TSV and bump, respectively.

Therefore the \( L_{TSV(T)} \) and \( L_{Bump(T)} \) can be obtained as
\[
L_{TSV(T)} = \frac{\mu}{4\pi} \left[ \frac{h}{2} + 2h \ln \left( \frac{\sqrt{r_1^2 + h^2 + h}}{r_1} \right) + 2r_1 - 2\sqrt{r_1^2 + h^2} + \frac{4h \beta (h + r_1) (\sqrt{r_1^2 + h^2 - h} - (4r_1 + \beta h))}{(\sqrt{r_1^2 + h^2 - h}) (4r_1 + \beta h)} \right]
\]
(4a)

\[
L_{Bump(T)} = \frac{1}{2} \left[ \frac{\mu \rho \delta R_{Bump}}{2\pi} \times h_{Bump} \times \ln \left( \frac{d_{TSV}}{2} \right) \right]
\]
(4b)

Whereas, for a cylindrical TSV, the equivalent inductance \( L_{equ(cy)} = L_{equ1(cy)} = L_{equ2(cy)} \) can be calculated using Eqn. (4) wherein the \( L_{TSV(cy)} \) can be derived as
\[
L_{TSV(cy)} = L_{TSV1(cy)} = L_{TSV2(cy)} = \frac{1}{2} \left[ \frac{\mu \rho \delta R_{TSV}}{2\pi} \times h_{TSV} \times \ln \left( \frac{d_{TSV}}{2} \right) \right]
\]
(5)

Also, the bump inductance \( L_{Bump(cy)} = L_{Bump1(cy)} = L_{Bump2(cy)} \) of cylindrical TSV can be calculated from Eqn. (4b).

In addition, considering a coaxial TSV, the expressions of inner equivalent inductance \( L_{equ(in(co)} = L_{equ1(in(co)} = L_{equ2(in(co)} \) and outer equivalent inductance \( L_{equ(out(co)} = L_{equ1(out(co)} = L_{equ2(out(co)} \) can be obtained using Eqn. (4). The inner and outer TSV inductances \( L_{TSV,in(co)} = L_{TSV,in1(co)} = L_{TSV,in2(co)} \) and \( L_{TSV,out(co)} = L_{TSV,out1(co)} = L_{TSV,out2(co)} \) can be calculated using Eqn. (5) by representing \( d_{TSV} = d_{inner} \) and \( d_{TSV} = d_{outer} \) respectively, and inner and outer bump inductances \( L_{Bump,in(co)} = L_{Bump,in1(co)} = L_{Bump,in2(co)} \) and \( L_{Bump,out(co)} = L_{Bump,out1(co)} = L_{Bump,out2(co)} \) can be calculated using Eqn. (4b) considering \( d_{Bump} = d_{Bump,inner} \) and \( d_{Bump} = d_{Bump} \) respectively.

### 2.2.3 Conductance

Another critical design parameter is the Si substrate conductance \( G_{Si} \) that exists between TSV pairs due to the lossy nature of the Si substrate. It has a substantial impact on the insertion loss of a TSV as Si conductivity \( (\sigma_{Si}) \) is the primary cause of this conductance that is governed by major carrier concentration. Therefore, the \( G_{Si} \) can be expressed as
\[
G_{Si} = g_{Si}' \times h_{TSV} ; \text{ where } g_{Si}' \text{ is the p.u.h. Si substrate conductance as shown in Fig. 2.}
\]

For a cylindrical TSV, the expression of \( G_{Si(cy)} \) can be obtained as
\[
G_{Si(cy)} = \frac{\pi \times \sigma_{Si} \times h}{\cosh^{-1}(\frac{h_{TSV}}{d_{TSV}})}
\]
(6)

where \( h = h_{TSV} - h_{IMD} \)

Similarly, the expressions of Si substrate conductance of tapered TSV \( (G_{Si(T)}) \) and coaxial TSV \( (G_{Si(co)}) \) can be obtained from Eqn. (6).

### 2.2.4 Capacitance

The capacity to store electrical energy is referred to as capacitance. In TSV, the charge accumulation occurs because of the existence of dielectric material between the two conducting materials. Due to this, a potential difference across the conducting materials appears due to the accumulation of charge. Thus, the amount of charge accumulated is known as capacitance. There are different types of capacitive parasitics associated with TSVs that can be defined as

1. Substrate capacitance \( (C_{equ}) \)
2. Equivalent capacitance \( (C_{equ}) \)
   - where \( C_{equ} = C_{ins} + C_{Bump1} + C_{Bump2} \)
   - \( C_{ins} = \epsilon_{liner} \epsilon_{dep} \)
   - Other bump capacitance in coaxial TSV \( (C_{Bump(\delta tw)(co)}) \)
3. Underfill, IMD, and bottom capacitances \( (C_{Underfill}, C_{IMD}, \text{ and } C_{Bottom}) \)
   - where \( C_{ui} = c_{ui}' \times h_{TSV} = C_{Underfill} + C_{IMD} \)
   - \( C_{ub} = c_{ub}' \times h_{TSV} = C_{Underfill} + C_{Bottom} \)
   - Inner liner capacitance \( (C_{inner,liner(co)}) \) in a coaxial TSV.

The above-mentioned capacitances are described in brief in the following subsections.

### 2.2.4.1 Substrate Capacitance

A capacitive coupling exists between the TSVs since the Si substrate is a semiconducting material with a considerable relative permittivity value that functions as an insulator. Hence, the substrate capacitance \( (C_{Si}) \) between two parallel TSVs is an important parameter that needs to be considered. In general, \( C_{Si} \) can be expressed as
\( C_{Si} = c'_{Si} \times h_{TSV} \); where \( c'_{Si} \) is the p.u.h. Si substrate capacitance as shown in Fig. 2.

Considering a pair of tapered TSVs (shown in Fig. 2(a)), the TSVs are divided into an infinite number of small elements (as shown in Fig. 3(b)). The substrate capacitance of the element \( dC_{Si(T)} \) can be considered as the parallel-wire capacitance. Therefore, the total capacitance of the infinite differential capacitors in parallel is equal to the substrate capacitance \( C_{Si(T)} \), which can be obtained as

\[
C_{Si(T)} = \int_{0}^{h} dC_{Si(T)} dz = \int_{0}^{h} \frac{2\pi \varepsilon_{Si}}{\cosh^{-1}\left(\frac{PTSV}{2t_{liner,1}+\beta r^{2}}\right)} dz
\]

(7)

Eqn. (7) can be expanded in the Taylor series. After simplification, the expression of \( C_{Si(T)} \) can be expressed as

\[
C_{Si(T)} = 2\pi \varepsilon_{Si} \varepsilon_{r,Si} \left[ \frac{h}{\cosh^{-1}\left(\frac{PTSV}{2t_{liner,1}}\right)} - \frac{h^{2} \beta P_{TSV}}{2r_{liner,1}^{2}} \left( \frac{PTSV^{2} - P_{TSV}^{2}}{PTSV^{2} - 4r_{liner,1}^{2}} \right) \right] \frac{1}{4r_{1}} \left( \cosh^{-1}\left(\frac{PTSV}{2t_{liner,1}}\right) \right)^{2} \left( \cosh^{-1}\left(\frac{PTSV}{2t_{liner,1}}\right) ^2 - 1 \right)
\]

(8)

For a pair of cylindrical TSVs, the parallel-wire capacitance model can be used to describe the capacitance of the Si substrate (as shown in Fig. 3). The expression of \( C_{Si(cy)} \) can be obtained as

\[
C_{Si(cy)} = \frac{\pi \times \varepsilon_{Si} \times h}{\cosh^{-1}\left(\frac{PTSV}{2r_{TSV}}\right)}
\]

(9)

Similarly, the Si substrate capacitance of a pair of coaxial TSVs \( C_{Si(co)} \) can be obtained by using Eqn. (9).

### 2.2.4.2 Equivalent Capacitance

The equivalent capacitance \( C_{equi} \) is a parallel combination of insulating capacitance \( C_{ins} \), upper bump capacitance \( C_{Bump1} \) and lower bump capacitance \( C_{Bump2} \). In general, \( C_{equi} \) can be defined as

\[
C_{equi} = c'_{equi} \times h_{TSV} \; ; \; \text{where} \; c'_{equi} \; \text{is the p.u.h. equivalent capacitance as shown in Fig. 2.}
\]

Considering a pair of tapered TSVs, the expression of \( C_{equi(T)} \) can be obtained as

\[
C_{equi(T)} = C_{equi1(T)} = C_{equi2(T)}
\]

\[
= C_{ins1(T)} + C_{Bump11(T)} + C_{Bump21(T)}
\]

(10)

Where an insulating capacitance \( C_{ins(T)} \) is the series combination of liner and depletion capacitances \( C_{liner(T)} \) and \( C_{dep(T)} \) that can be obtained as

\[
C_{ins(T)} = C_{ins1(T)} = \frac{C_{liner(T)}C_{dep(T)}}{C_{liner(T)}+C_{dep(T)}}
\]

(11)

A liner capacitance \( C_{liner} \) is formed between the TSV metal and the Si substrate due to the presence of a liner layer. In order to obtain the expression of \( C_{liner(T)} \), a tapered TSV without a depletion layer is depicted in Fig. 3(a). Here, \( t_{liner} \), \( h \), \( r \), \( r_{1} \) and \( r_{2} \) represent the liner thickness, TSV height, slope angle, lower radius and upper radius of the tapered TSV, respectively.

![Fig 3](image-url)
As indicated in Fig. 3 (b), the tapered TSV can be subdivided into an infinite number of small cylindrical sections with a height of \(dz\). There is a \(de\) charge associated with each small cylindrical element and the potential difference between the TSV metal and the Si substrate can be defined according to the Gauss law [13]

\[
dv = \int_{r_1 + \beta z}^{r_1 + \beta z} E \cdot d\overrightarrow{r} = \frac{de}{2\pi\varepsilon_{\text{liner}} de} \ln \left( \frac{r_1 + \beta z}{r_1 + \beta z} \right)
\]

(11a)

where, \(E = \frac{de}{2\pi\varepsilon_{\text{liner}} de} \beta = \tan \theta\), \(r_{\text{liner},1} = r_{\text{liner}} + t_{\text{liner}}\), and \(\theta\) is taken as 15° [13].

Therefore, the equivalent liner capacitance is constituted of the capacitances of infinite differential capacitors connected in parallel. Hence, \(C_{\text{liner}(T)}\) can be obtained as

\[
C_{\text{liner}(T)} = \int_0^h dc_{\text{liner}(T)} dz = 2\pi\varepsilon_{\text{liner}} \int_0^h \frac{dz}{\ln \left( \frac{r_{\text{liner},1} + \beta z}{r_1 + \beta z} \right)}
\]

(11b)

where, \(h = h_{TSV} - h_{IMD}\)

After simplification, the first three terms of the Taylor series expansion of Eqn. (11b) can be given as

\[
C_{\text{liner}(T)} = 2\pi\varepsilon_{\text{liner}} \left[ \frac{h}{\ln \left( \frac{r_{\text{liner},1}}{r_1} \right)} + \frac{\beta t_{\text{liner}} h^2}{2r_1 r_{\text{liner},1} \ln \left( \frac{r_{\text{liner},1}}{r_1} \right)} \right] + \frac{2\beta^2 t_{\text{liner}}^2 h^3 \ln \left( \frac{r_{\text{liner},1}}{r_1} \right)}{12r_1 r_{\text{liner},1} \ln \left( \frac{r_{\text{liner},1}}{r_1} \right)}
\]

(11c)

Further simplification of the above equation provides the modified expression of the liner capacitance as,

\[
C_{\text{liner}(T)} = 2\pi\varepsilon_0 E_r \left( 1 + \frac{h}{\ln \left( \frac{r_{\text{liner},1}}{r_1} \right)} \right)
\]

\[
+ \frac{\beta t_{\text{liner}} h^2}{2r_1 r_{\text{liner},1} \ln \left( \frac{r_{\text{liner},1}}{r_1} \right)}
\]

(11d)

where, \(\zeta = \frac{0.075(5\beta)^3}{1 + (5\beta)^3}\) is defined as an error factor.

The lower cross-sectional view of a tapered TSV with a depletion layer is demonstrated in Fig. 3 (c). Since the depletion layer has a structure that is similar to that of the liner layer, the capacitance of the depletion layer \(C_{\text{dep}(T)}\) can be calculated from Eqn. (11d) considering \(r_1 = \eta_{\text{liner},1}, \eta_{\text{liner},1} = r_{\text{dep}},\) and \(t_{\text{liner}} = (r_{\text{dep}} - r_{\text{liner},1})\).

\(C_{\text{Bump1}(T)}\) and \(C_{\text{Bump2}(T)}\) exist between the upper bump and the Si substrate due to the IMD layer and between the lower bump and the Si substrate due to the bottom insulating layer, respectively. These capacitances can be represented mathematically as parallel-plate capacitors.

\[
C_{\text{Bump1}(T)} = C_{\text{Bump12}(T)} = \varepsilon_0 E_r \cdot \frac{\pi}{h_{\text{IMD}}} \left( \frac{(d_{\text{Bump}/2)}^2 - (d_{\text{TSV}/2} + t_{\text{liner, bot}})^2}{\beta_{\text{liner}}} \right)
\]

(12)

\[
C_{\text{Bump2}(T)} = C_{\text{Bump22}(T)} = \varepsilon_0 E_r \cdot \frac{\pi}{h_{\text{IMD}}} \left( \frac{(d_{\text{Bump}/2)}^2 - (r_1 + t_{\text{liner, bot}})^2}{t_{\text{liner, bot}}} \right)
\]

(13)

Similarly, considering a pair of cylindrical TSVs, the expression of equivalent capacitance \(C_{\text{equiv}(cy)}\) can be expressed using Eqn. (10) wherein the expression of insulating capacitance \(C_{\text{ins}(cy)} = C_{\text{inst}(cy)} = C_{\text{ins2}(cy)}\) can be obtained using Eqn. (11) by putting \(\beta = 0\), however, the expressions of upper bump capacitance \(C_{\text{Bump1}(cy)} = C_{\text{Bump11}(cy)} = C_{\text{Bump12}(cy)}\) and lower bump capacitance \(C_{\text{Bump2}(cy)} = C_{\text{Bump21}(cy)} = C_{\text{Bump22}(cy)}\) can be obtained using Eqns. (12) and (13) respectively, considering \(r_1 = d_{\text{TSV}}/2\).

In a similar manner, considering a pair of coaxial TSVs, the expression of equivalent capacitance expression \(C_{\text{equiv}(co)}\) can be expressed using Eqn. (10) wherein the expression of insulating capacitance \(C_{\text{ins}(co)} = C_{\text{inst}(co)} = C_{\text{ins2}(co)}\) can be obtained using Eqn. (11) by putting \(\beta = 0\), however, the expressions of upper bump capacitance \(C_{\text{Bump1}(co)} = C_{\text{Bump11}(co)} = C_{\text{Bump12}(co)}\) and lower bump capacitance \(C_{\text{Bump2}(co)} = C_{\text{Bump21}(co)} = C_{\text{Bump22}(co)}\) can be obtained using Eqns. (12) and (13) respectively, considering \(r_1 = d_{\text{TSV}}/2\).

However, in a coaxial TSV, another bump capacitance, denoted by the symbol \(C_{\text{Bump}(btw)(co)}\) exists within the bump due to the presence of an insulating layer between the inner and outer parts of the coaxial TSV, which divides the inner and outer surfaces of the bump. This bump capacitance \(C_{\text{Bump}(btw)(co)}\) can be represented by the coaxial-cable capacitance model that can be expressed as

\[
C_{\text{Bump}(btw)(co)} = 2\pi \times \varepsilon_0 E_r \times \frac{h}{\ln \left( \frac{d_{\text{Bump,inner}/2 + t_{\text{liner}}}}{d_{\text{Bump,inner}/2}} \right)}
\]

(14)

### 2.2.4.3 Underfill, IMD, and Bottom Capacitances

As shown in Fig. 2, the \(C_{\text{UI}}\) and \(C_{\text{UB}}\) are the parallel combinations of IMD \((C_{\text{IMD}})\) and bottom \((C_{\text{Bottom}})\) capacitances with an underfill capacitance \((C_{\text{Underfill}})\), respectively and can be defined as

\[
C_{\text{UI}} = c'_{\text{UI}} \times h_{\text{TSV}} = C_{\text{Underfill}} + C_{\text{IMD}}
\]

(15)

\[
C_{\text{UB}} = c'_{\text{UB}} \times h_{\text{TSV}} = C_{\text{Underfill}} + C_{\text{Bottom}}
\]

(16)

where \(c'_{\text{UI}}\) and \(c'_{\text{UB}}\) are the p.u.h. UI and UB capacitances as shown in Fig. 2.
Considering a pair of tapered TSV, an underfill capacitance \( C_{\text{underfill}} \) exists between the upper (or lower) bump of \( TSV_1 \) and the upper (or lower) bump of \( TSV_2 \) due to an underfill layer. Likewise, an IMD capacitance \( C_{\text{IMD}} \) occurs between \( TSV_1 \) and \( TSV_2 \) due to the presence of an IMD layer. Similarly, a bottom capacitance \( C_{\text{Bottom}} \) forms between \( TSV_1 \) and \( TSV_2 \) due to a bottom insulating layer. The TSV and bump have circular cross-sectional areas, so, \( C_{\text{underfill}} \), \( C_{\text{IMD}} \), and \( C_{\text{Bottom}} \) are derived from the parallel-wire capacitance model. These capacitances are expressed as

\[
C_{\text{underfill}} = \frac{\pi \times \varepsilon_0 \times d_{\text{bump}}}{\ln \left( \frac{d_{\text{inner}}}{d_{\text{outer}}} \right)} \times h_{\text{bump}}
\]  
(17)

\[
C_{\text{IMD}} = \frac{\pi \times \varepsilon_0 \times d_{\text{TSV}}}{\ln \left( \frac{d_{\text{outer}}}{d_{\text{inner}}} \right)} \times h_{\text{IMD}}
\]  
(18)

\[
C_{\text{Bottom}} = \frac{\pi \times \varepsilon_0 \times d_{\text{TSV}}}{\ln \left( \frac{d_{\text{inner}}}{d_{\text{outer}}} \right)} \times t_{\text{liner,bot}}
\]  
(19)

Considering a pair of cylindrical TSV, the expressions of \( C_{\text{underfill}} \), \( C_{\text{IMD}} \), and \( C_{\text{Bottom}} \) can be calculated using Eqn. (17), (18), and (19) respectively, considering \( 2r_1 = d_{\text{TSV}} \).

Similarly, for a pair of coaxial TSVs, the expressions of \( C_{\text{underfill}} \), \( C_{\text{IMD}} \), and \( C_{\text{Bottom}} \) can be calculated using Eqn. (17), (18), and (19) respectively representing \( 2r_1 = d_{\text{TSV}} \). Apart from these capacitances, a coaxial TSV, an inner-liner capacitance \( C_{\text{inner,liner}} \) exists between the inner and outer parts of a coaxial TSV due to the inner insulating layer. The \( C_{\text{inner,liner}} \) can be represented mathematically by the coaxial-cable capacitance model, and it can be obtained as

\[
C_{\text{inner,liner}} = 2\pi \times \varepsilon_0 \times \frac{h}{\ln \left( \frac{d_{\text{inner}}}{d_{\text{outer}}} \right)}
\]  
(20)

The via parasitics are obtained based on the technology-dependent physical parameters of the TSV. Table 4 presents a list of these parasitic values for different TSV shapes considering an AR of 2.4 at 32 nm and 45 nm technology.
3 Impact of Liner on TSV

This section examines the effects of various liner materials on the crosstalk induced delay performance of different TSV shapes at the 32 nm and 45 nm technology nodes using their presented *RLGC* models (as shown in Fig.2). Fig. 4 illustrates a 2-line DVL setup employed for electrical modelling of the TSV with 20 distributed *T*-network.

![Fig. 4 Schematic view of the DVL setup with capacitively coupled TSV lines.](image)

As shown in Fig. 4, each TSV line is represented by a set of *RLGC* parasitic elements, as depicted in Fig. 2. Each TSV line is driven by a CMOS driver with a supply voltage of 0.9V and 1V at 32 nm and 45 nm technology, respectively. As shown in Fig. 4, the capacitive loadings (*C*<sub>Load</sub>) of 0.1aF at the aggressor and victim lines are taken into consideration. Using the above mentioned DVL setup in Fig. 4, the subsequent sections have analyzed the impact of liner materials on the overall performance of TSVs in terms of crosstalk induced delay for different via shapes and aspect ratios.

3.1 Impact of Liners on Different Aspect Ratios of TSVs

This sub-section presents the crosstalk induced delay analysis of cylindrical, tapered, and coaxial TSVs for different aspect ratios of 2.4, 3.0 and 4.0 while considering via heights ranging from 9.6μm to 12.6μm and 12μm to 20μm at 32 nm and 45 nm technology, respectively. The out-phase dynamic crosstalk induced delay occurs for opposite switching phenomenon that causes worst-case crosstalk induced delay with a significant Miller Coupling Factor (MCF). Hence, in order to calculate the worst-case crosstalk induced delay, the out-of-phase switching transition state is considered in this work.

![Fig. 5 Crosstalk induced delay of (a) tapered, (b) cylindrical, and (c) coaxial TSVs, using SiO<sub>2</sub> and BCB liners at 32 nm and 45 nm technology nodes.](image)
By varying the aspect ratios of TSVs, Fig. 5 (a), (b), and (c) present the crosstalk induced delay of tapered, cylindrical, and coaxial TSVs, respectively with SiO$_2$ and BCB liners at 32 nm and 45 nm technology nodes. It is observed that the TSVs with BCB liners exhibit lesser crosstalk induced delay than the TSVs with SiO$_2$ liners, irrespective of the shape and AR of the TSVs under consideration. The reason behind this is that the BCB polymer dielectric has less ability to support electrostatic forces between TSV metal and Si substrate, and hence the $C_{\text{liner}}$ of TSV using BCB is lower than that of SiO$_2$. It is due to a substantially lower dielectric constant of BCB ($\varepsilon_r$=2.65) than that of the SiO$_2$ ($\varepsilon_r$=3.9). In addition, a more consistent thickness of BCB polymer liner (1-5 $\mu$m) compared to the SiO$_2$ liner (typically 0.1–1 $\mu$m) results in a reduced liner capacitance in TSVs. From Fig. 5, it is observed that the worst-case crosstalk induced delay at the 32 nm is lesser when compared to the 45 nm technology, regardless of the liner material used or the AR of the TSV. The improvement in crosstalk induced delay using a tapered TSV (as shown in Fig. 5 (a)) at 32 nm w.r.t. 45 nm technology can be observed as 53.5%, 33.76%, and 19.12% at aspect ratios of 2.4, 3, and 4, respectively for the BCB liner. The primary reason behind this is that the quantitative value of via resistance at a lower technology is smaller than that of higher technology, as presented in Table 4. This is owing to the fact that the reduced physical dimensions of TSVs (ex. height and diameter of TSV) at lower technology results in the lesser value of via resistance. Another important observation is that the crosstalk induced delay reduces for a lower via aspect ratio, as presented in Fig. 5. It can be perceived that for a tapered TSV with BCB liner, crosstalk induced delay at an AR = 2.4 is improved by 48.37% and 15.14% at 32 nm and 45 nm technology, respectively compared to the AR = 4. Therefore, it can be inferred that TSVs with a smaller aspect ratio exhibit a large reduction in crosstalk induced delay when compared with TSVs with a larger aspect ratio. This is due to the fact that the crosstalk induced delay of a coupled TSV with a smaller aspect ratio reduces because of its substantially lower value of via resistance and coupling capacitance. The resistance and capacitance primarily reduce for an overall reduction in footprint area at a smaller via aspect ratio.

Considering the crosstalk induced delay in different scenarios (shown in Fig. 5), Table 5 summarizes the percentage reduction in crosstalk induced delay of cylindrical TSV with aspect ratio=2.4 is 39.27%, 34.35%, 29.54%, and 29.38% using SiO$_2$, PI, PBO, and PPC liners respectively at 32 nm technology node; similarly, the overall % reduction in crosstalk induced delay with aspect ratio=4 is 9.36%, 8.54%, 6.04%, and 0.64%, respectively. It is noted that the primary cause for this reduction is the lower quantitative values of liner capacitances in TSV when polymer liners are employed. The reason for this is that the dielectric constants of polymer liners are significantly lower than that of SiO$_2$ liner. In comparison to SiO$_2$ and other polymer liners with relatively larger dielectric constants, the lower dielectric constant of BCB significantly reduces capacitance value that is resulting in reduced crosstalk induced delay. Another observation from Table 5 is that as the aspect ratio changes from a higher value to a lower value, there is a significant percentage reduction in crosstalk induced delay.

| Aspect Ratio | TSV Shape | SI02 | PI | PPC | PBO | PPC |
|--------------|-----------|------|----|-----|-----|-----|
| 2.4          | Cylindrical | 39.27 | 34.35 | 29.54 | 29.38 | 39.27 |
| 3             | Coaxial    | 25.00 | 19.73 | 15.30 | 15.30 | 25.00 |
| 4             | Tapered    | 24.33 | 19.73 | 15.30 | 15.30 | 24.33 |
This can be observed as the differences in % reduction in crosstalk induced delay of cylindrical, coaxial, and tapered TSVs using SiO\textsubscript{2} liner w.r.t. crosstalk induced delay of these TSVs using BCB liner are 29.91%, 16.64%, and 9.03% respectively at 32 nm technology node. Similarly, these differences at 45 nm technology node are 14.42%, 3.99%, and 3.64%. This is because TSVs with a smaller aspect ratio have smaller heights, so the overall areas of the TSVs are reduced, and as a result, the overall crosstalk induced delay is lowered by substantial percentage values.

### 3.2 Impact of Liners on Different TSV Shapes

This sub-section examines the impact of various liner materials on the via performance as defined by the crosstalk delay between the TSV lines. When the TSVs are exposed to high temperatures during the manufacturing process, the large mismatch in CTE values of Cu (16.5 ppm/K); the Si substrate (2.6 ppm/K) and SiO\textsubscript{2} (0.5ppm/K) causes considerable stress in the Cu, Si substrate, and SiO\textsubscript{2} liner. This phenomenon primarily results in severe physical reliability issues such as die cracking or breaking, copper pumping, and interfacial delamination. The Cu pumping and current leakage caused by the insulator/barrier failure can be prevented by an increasing thickness of the liner. Additionally, the low dielectric constants of polymers and their large thicknesses enable them to achieve low capacitance and improved electrical performance. Figures 6(a) and 6(b) demonstrate the crosstalk delays of cylindrical, coaxial, and tapered TSVs using SiO\textsubscript{2}, PI, and BCB liners at 32 nm and 45 nm technology, respectively. It is observed that the crosstalk delay of the cylindrical TSV is significantly higher compared to the other via shapes, whereas the least delay can be witnessed using the tapered shape. The cylindrical TSV has larger via resistance and coupling capacitance (as presented in Table 4) than other via shapes that causes a worst-case crosstalk delay. This is due to the lower conductivity of cylindrical shaped TSV owing to its large cross-sectional area and uniform surface. Consequently, the cylindrical TSV possesses a higher value of coupling capacitance that is a function of radius, length, via pitch, and dielectric thickness and increases monotonically for higher radius and reduced via pitch. However, the tapered TSV outperforms the other via shapes in terms of crosstalk delay since it has a lower via resistance and coupling capacitance due to its smaller cross-sectional area and radius, as evidenced from Table 4.

Apart from this, Fig. 6 also demonstrates that the SiO\textsubscript{2} liner introduces more worst-case crosstalk delay compared to the BCB irrespective of the via shapes. It is due to the lower dielectric constant of BCB with a thicker polymer liner than the SiO\textsubscript{2} that allows to obtain a reduced coupling capacitance. This fact can be demonstrated in terms of the MCF wherein it is stated that during opposite switching transitions of TSVs, the charge provided to the coupling capacitor becomes $Q=CEQU\Delta V$, where $\Delta V$ is the change in voltage between the TSVs. In this scenario, $\Delta V$ becomes $2V_{DD}$, where $V_{DD}$ is the supply voltage, and hence the equivalent coupling capacitor can be considered as being effectively twice as large as switching through $V_{DD}$. As a result, the total charge becomes twice as much required, and the MCF becomes 2 in case of worst-case crosstalk delay [20,21]. Thus, the cumulative effect of the $\Delta V$ and the dielectric constant possesses lower worst-case crosstalk delay in the case of BCB liner based TSV. Furthermore, it can be inferred that considering a tapered TSV, the worst-case crosstalk delays using a BCB liner are improved by 32.16% and 26.93% at 32 nm and 45 nm technology, respectively compared to a SiO\textsubscript{2}. Whereas the improvements using the BCB compared to the PI
liner are only 26.48% and 10.21% at 32 nm and 45 nm technology, respectively. Therefore, the BCB liner based tapered shaped TSV has the lower relative dielectric constant ($\varepsilon_r = 2.65$) that results in a significant reduction in liner capacitance and hence a reduced crosstalk induced delay.

4 Conclusion

The paper presented a novel 20 distributed $T$-type electrical model of cylindrical, tapered, and coaxial TSV configurations at 32 nm and 45 nm technology. The impact of different liner materials on the crosstalk delay of various TSV shapes at a frequency of 20 GHz is investigated. It has been observed that the crosstalk delay is significantly improved at an advanced technology due to its lower via resistance and coupling capacitance. This improvement using a tapered TSV at 32 nm w.r.t. 45 nm technology can be observed as 53.5%, 33.76%, and 19.12% at aspect ratios of 2.4, 3, and 4, respectively for the BCB liner. Moreover, considering a tapered TSV, the improvement in crosstalk delay using a BCB liner has been observed as 32.16% and 26.93% at 32 nm and 45 nm technology, respectively, compared to the SiO$_2$ liner. The above-mentioned results are obtained by considering the influence of the dielectric permittivity, which implies that BCB is the most appropriate liner material for crosstalk applications. Moreover, it is noticed that the tapered shaped TSV causes the least crosstalk delay as it offers a consistent insulating layer that minimizes the leakage from the TSV metal to the Si substrate. Also, its parasitic values are significantly lower due to the smaller surface area compared to the cylindrical and coaxial TSVs. Thus, it can be predicted that a tapered shaped TSV with BCB liner is an appropriate configuration for reduced crosstalk induced delay in 3D integrated circuits.

References

1. Fang, R., Sun, X., Miao, M., Jin, Y.: Characteristics of Coupling Capacitance Between Signal–Ground TSVs Considering MOS Effect in Silicon Interposers. IEEE Transactions on Electron Devices, 62(12), pp. 4161 – 4168 (2015).

2. Jawed, S.A., Afridi, S.S., Anjum, M.A., Khan, K.: IO circuit design for 2.5D through-silicon-interposer interconnects. International Journal Of Circuit Theory And Applications, 45(03), pp. 376-391 (2017).

3. Hwang, C., Achkir, B., Fan, J.: Capacitance-Enhanced Through-Silicon Via for Power Distribution Networks in 3D ICs. IEEE Electron Device Letters, 37(4), pp. 478 – 481 (2016).

4. Naga, T., Kolanti, J., Patel, V., Rao, K.S.: Crosstalk noise analysis in ternary logic multilayer graphene nanoribbon interconnects using shielding techniques. International Journal of Circuit Theory and Applications, 48(12), pp. 2041-2055 (2020).

5. Chandrakar, S., Gupta, D., Majumder, M.K.: Role of through silicon via in 3D Integration: Impact on delay and power. Journal of Circuits, Systems and Computers, 30(03), pp. 2150051 (2021).

6. Zhang, Z.M., Lin, S.C., Pan, C.L.: Electrical modelling of 3D stacked TSV. In Proceedings of the 12th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), pp. 254-257 (2017).

7. Badugu, D.M., Sunithamani, S.: Crosstalk reduction in copper on-chip interconnects with graphene barrier for ternary logic applications. International Journal of Circuit Theory And Applications, 48(12), pp. 2097-2110 (2020).

8. Xue, C., Cheng, Z., Chen, Z., Yan, Y., Cai, Z., Ding, Y.: Elimination of scallop-induced stress fluctuation on through-silicon-vias (TSVs) by employing polyimide liner. IEEE Transactions on Device And Materials Reliability. 18(02), pp. 266 – 272 (2018).

9. Savidis, I., Friedman, E.G.: Closed-form expressions of 3-D via resistance, inductance, and capacitance. IEEE Transactions on Electron Devices, 56(09), pp. 1873 – 1881 (2009).

10. Katti, G., Stucchi, M., Meyer, K.D., Dehaene, W.: Electrical modeling and characterization of through silicon via for three-dimensional ICs. IEEE Transactions on Electron Devices, 57(01), pp. 256-262 (2010).

11. Gerakis, V., Hatzopoulos, A.: Improved transmission line model for high-frequency modelling of through silicon vias. International Journal of Electronics, 106(05), pp. 785-798 (2019).

12. Xu, Z., Lu, J.Q.: Three-dimensional coaxial through-silicon-via (TSV) design. IEEE Electron Device Letters, 33(10), pp. 1441-1443 (2012).

13. Su, J., Wang, F., Zhang, W.: Capacitance expressions and electrical characterization of tapered through-silicon vias for 3-D ICs. IEEE Transactions on Components, Packaging and Manufacturing Technology, 5(10), pp. 1488 – 1496 (2015).

14. Nabil, A., Bernardo, J.A., Ma, Y., Abouelatta, M., Shaker, A., Bouchet, L.F., Ragai, H., Gontrand, C.: Electrical modelling of tapered TSV including MOS-Field effect and substrate parasitics: Analysis and application. Microelectronics Journal, 100, pp.104797 (2020).

15. Murugesan, M., Fukushima, T., Bea, J.C., Sato, Y., Hashimoto, H., Lee, K.W., Koyanagi, M.: Highly beneficial organic liner with extremely low thermal stress for fine Cu-TSV in 3D-integration. In Proceedings of the IEEE International Electron Devices Meeting, pp. 14.7.1-14.7.4 (2014).

16. Kino, H., Tashiro, M., Sugawara, Y., Tanikawa, S., Fukushima, T., Tanaka, T.: Minimized hysteresis and low parasitic capacitance TSV with PBO (Polybenzoxazole) liner to achieve ultra-high-speed data transmission. In Proceedings of the IEEE International Interconnect Technology Conference (IITC), pp. 1-3 (2017).

17. Ganimidi, M., Kumar, V.R.: Design of novel through silicon via structures for reduced crosstalk effects in 3D IC applications. In
Proceedings of the Intelligent Communication, Control and Devices conference, pp. 599-605 (2018).

18. Rao, K.N., Nath, G.V., Kishore, K.H.: Crosstalk noise minimization in novel through silicon via structures. International Journal of Engineering & Technology, 7(2.8), pp. 56-62 (2018).

19. Su, J., Zhang, W., Yao, C.: Partial coaxial through-silicon via for suppressing the substrate noise in 3-dimensional integrated circuit. IEEE Access, 7, pp. 98803 – 98810 (2019).

20. Reddy, K.N., Majumder, M.K., Kaushik, B.K.: Delay uncertainty in MLGNR interconnects under process induced variations of width, doping, dielectric thickness and mean free path. Journal of Computational Electronics, 13(03), pp. 639-646 (2014).

21. Kumar, V.R., Majumder, M.K., Alam, A., Kukkam, N.R., Kaushik B.K.: Stability and delay analysis of multi-layered GNR and multi-walled CNT interconnects. Journal of Computational Electronics, 14(02), pp. 611-618 (2015).

22. Sahu, C.C., Anand, S., Majumder, M.K.: Analysis of Eddy Effect for Cu and CNT Bundle Based Through-Silicon Vias: Impact on Crosstalk and Power. Journal of Computational Electronics, (2021).

23. Liu, B., Li, C., Li, C., Zhang, S.: Effect of temperature and single event transient on crosstalk in coupled single-walled carbon nanotube (SWCNT) bundle interconnects. International Journal of Circuit Theory and Applications, 49(10), pp. 3408-3420 (2021).

24. Kumbhare, V.R., Paltani, P.P., Majumder, M.K.: Analysis of top and side-contact MLGNR interconnects: impact on crosstalk, stability, and electromigration. Journal of Computational Electronics. 19(04), pp. 1588-1596 (2020).
