0.3–4.4 GHz wideband CMOS frequency divide-by-1.5 with optimized CML-XOR gate

Hua Chen¹,², Guiliang Guo¹(a), Qiangtao Lai¹, Yulin Zhang¹, Jingyu Han¹, and Yuepeng Yan¹

¹ Institute of Microelectronics, Chinese Academy of Sciences,
No. 3 Beitucheng West Rd., Chaoyang District, Beijing, China, 100029
² University of Chinese Academy of Sciences,
No. 19A Yuquan Rd., Shijingshan District, Beijing, China, 100049
a) guoguiliang@ime.ac.cn

Abstract: An ultra-wideband differential divide-by-1.5 divider based on current-mode logic (CML) is proposed. It consists of a divide-by-3 circuit and an optimized CML-XOR gate. Fully symmetric and differential structure is proposed to extend upper bound working frequency. In the CML-XOR gate, two identical Gilbert cells with optimized eight-input signals are developed to strengthen the pull-down force, which benefits the high-speed division. Fabricated in TSMC 180 nm CMOS process, this divider achieves an operating frequency of 0.3–4.4 GHz for 0 dBm input, and consumes 4.14 mW from 1.8 V supply. The chip size is 0.02 mm².

Keywords: frequency divider, divide-by-1.5, wideband, CML, CMOS

Classification: Integrated circuits

References

[1] J. Kim, et al.: “A CMOS direct conversion transmitter with integrated in-band harmonic suppression for IEEE 802.22 cognitive radio applications,” IEEE Custom Integr. Circuits Conf. (2008) 603 (DOI: 10.1109/CICC.2008.4672158).
[2] S. A. Osmany, et al.: “An integrated 0.6–4.6 GHz, 5–7 GHz, 10–14 GHz, and 20–28 GHz frequency synthesizer for software-defined radio applications,” IEEE J. Solid-State Circuits 45 (2010) 1657 (DOI: 10.1109/JSSC.2010.2051476).
[3] H. Shin, et al.: “A 4.5 to 9.2-GHz wideband semidynamic frequency divide-by-1.5 in GaInP/GaAs HBT,” IEEE Microw. Wireless Compon. Lett. 17 (2007) 73 (DOI: 10.1109/LMWC.2006.887280).
[4] Y. L. Yeh, et al.: “A W-band divide-by-1.5 injection-locked frequency divider in 90 nm CMOS process,” IEEE MTT-S Int. Microw. Symp. Dig. (2014) 1 (DOI: 10.1109/MWSYM.2014.6848332).
[5] V. B. Minuhin, et al.: US Patent. 4,866,741 (1989).
[6] B. Razavi: RF Microelectronics (Prentice Hall, New Jersey, 2011) 2nd ed. 677.
[7] R. Hulfachor, et al.: U.S. Patent 7,348,818 (2007).
[8] U. Singh and M. Green: “Dynamics of high-frequency CMOS dividers,” IEEE Int. Symp. Circuits Syst. 5 (2002) V-421 (DOI: 10.1109/ISCAS.2002.1010730).
1 Introduction

Multi-modulus local oscillator generation (LOGEN) plays an important role in wideband frequency synthesizers [1, 2]. In the LOGEN, wideband divide-by-1.5 is a challenging block to realize the quadrature-output divide-by-3 divider [1, 2]. Semi-dynamic structure is mostly used to realize the divide-by-1.5 [1, 3]. In [1], a divide-by-1.5 is implemented by semi-dynamic structure, and a three-stage RC poly-phase filter is used for the quadrature generation. However, the divider exhibits large silicon area due to the RC array. In [3], semi-dynamic style is also used and wide bandwidth is achieved by utilizing tunable technique. Unfortunately, the power of the whole divider is huge and the area is large. Moreover, it generates many unwanted spurs due to the inherent mixing mechanism. Injection-locked technique also can be utilized to realize divide-by-1.5, but it shows narrow working frequency range and large silicon area [4]. In [5], a divide-by-1.5 divider is realized by cascading a divide-by-3 with an AND gate, which is based on waveform transfer technique instead of mixing or injection-locking mechanism. Like [5], this letter proposed a similar architecture, but it is based on current-mode logic (CML) style to obtain wideband operation and robust division [6]. Instead of AND gate, XOR gate is utilized to achieve the multiply-by-2 function. Divide-by-3 and CML-XOR gate are both optimized to achieve a fully symmetric and differential style, which extend upper bound operation frequency.

2 Circuit design

Fig. 1(a) shows the circuit schematic of the divide-by-1.5 divider revealed in US patent 4,866,741. By cascading divide-by-3 with an AND gate, a divide-by-1.5 function is realized. Two D-type flip-flops (DFFs) are driven by complementary clocks “CK” and “CKN”, so the state machine responds to both edges of the input clock “CK”. By virtue of an OR gate, the state of “Q1\Q2” circles in the following order: “10”→“10”→“11”→“01”→“01”→“11” [5]. Hence a divide-by-3 divider is achieved [5]. On the other hand, the patent takes advantage of the particular waveforms of “Q1” and “Q2” to do AND operation, then a multiply-by-2 function is obtained [5]. Finally, the patent has successfully realized a divide-by-1.5 divider.

Based on the same methodology, this letter proposed a novel divide-by-1.5 divider used for wideband and high-speed applications, which is shown in Fig. 1(b). All modules of the divider are CML style. DFF is realized by two
CML latches, which operate in master-slave manner [7, 8]. “Master1” and “slave1” latches constitute the DFF1, with “master2” and “slave2” the DFF2. NOR gate is placed between the master latch and the slave latch to generate input data for the slave latch. As shown in Fig. 1(c), the state of \(Q1\) changes with both falling edge and rising edge of input “\(CK\)”. Starting at time \(t_0\), “\(Q1\)\(\backslash Q2\)” is “00”. At the subsequent edge times from \(t_1\) to \(t_6\), “\(Q1\)\(\backslash Q2\)” changes in the following manner: “10”→“10”→“00”→“01”→“01”→“00”, and then circles. Hence a divide-by-3
function is realized. Moreover, the topology of the divide-by-3 divider has a fully-symmetric structure, which reduces critical path time and extends working frequency.

CML-XOR gate is used to realize the multiply-by-2 function. To decrease the load capacitance of “slave1” and “slave2”, the outputs of “master1” and “master2” are sent to the CML-XOR gate. As shown in Fig. 1(c), a multiply-by-2 output can be obtained by doing OR or XOR operation on signals “A” and “B”. Compared with CML-OR gate, CML-XOR gate maintains a balanced structure, which helps high frequency operation. Considering the stack style of CML XOR gate, signal “B” passes through a level-shifter to lower its common-mode level, labeled by “BL”. As depicted in Fig. 1(c), the output of the XOR gate is about 66.7% duty cycle, which means the low level is half time of the high level.

To generate sufficient pull-down strength during the low level, this letter proposed an optimized CML-XOR gate, as shown in Fig. 2(b). Compared to the traditional structure, illustrated in Fig. 2(a), the proposed CML-XOR gate has two identical cells. Each cell dissipates a half current, and the dimensions of transistors and resistors have to adjust accordingly. The copied cell has complementary inputs, which calls for another level-shifter to adjust common level of signal “A”. As depicted in Fig. 1(b), the two level-shifters, together with the proposed eight-input CML-XOR gate, form a fully symmetric structure, which contributes to a high frequency operation.

To demonstrate this idea, the divide-by-1.5 divider with conventional and proposed CML-XOR gates are conducted pre-simulation, respectively, using spectreRF tool in Cadence, ignoring the layout parasitic. The simulated results are shown in Fig. 3 and Fig. 4. In Fig. 3(a), the deformity appears in the waveform of the output “VOP”, which is caused by the insufficient pull-down force during high-speed operation. And in Fig. 3(b), this problem is solved. Fig. 4 shows the improvement of input sensitivity of the divider-by-1.5 divider using the proposed eight-input CML-XOR gate. In Fig. 4, the red curve stops at 4.5 GHz because of the severe malformation of the output signal “VOP”. Therefore, for the traditional CML-XOR case, the input frequency range is limited.

---

Fig. 2. (a) Conventional CML-XOR circuit; (b) Proposed CML-XOR circuit.
3 Experimental results

The divide-by-1.5 circuit was fabricated in TSMC 180nm CMOS process. Fig. 5 shows the layout and die micrograph of the proposed divide-by-1.5 divider. The active area is \(160 \mu m \times 130 \mu m\). Prudent layout techniques are used to balance the parasitic capacitors between the differential signal paths [9]. The output of divider is buffered through using an inverter chain to drive external measurement instruments [9]. Chip was mounted on a printed circuit board by wire bonding. Considering the single-ended source signal provided by Agilent E8267D, balun devices of JA4220 and LDB183G7010C are paralleled to achieve a 0.1–4000 MHz single to differential conversion.

Fig. 3. Simulated results of divide-by-1.5 divider with (a) conventional (b) proposed CML-XOR circuit @ typical corner, 27°C, \(f_{in} = 4\) GHz, \(amp = 150\) mVpk.

Fig. 4. Simulated input sensitivity curve of divide-by-1.5 divider @ typical corner, 27°C.
Fig. 6 shows the input sensitivity curve of the divider measured at 1.8 V supply using a Rohde & Schwarz FSV signal analyzer. The divider has a 4.1 GHz operation frequency range for 0 dBm input power. At 3 GHz, there is a swell. This is mostly due to the frequency transition between the two parallel baluns.

Fig. 7 shows the measured output spectrum when the input frequency is 400 MHz and the output frequency is 266.67 MHz. The output power is $-2.72$ dBm, and the input power is $-3$ dBm. The measured phase noises are $-139.76$ dBc/Hz and $-141.91$ dBc/Hz at 10 kHz and 1 MHz offsets, respectively.

Table I compares the proposed divide-by-1.5 divider with previously published works in terms of input frequency range, divide-by-N, differential operation capability and other performances. This work demonstrates the widest input frequency range among the mentioned differential dividers in CMOS technology; besides, it has the lowest power and the smallest area.
4 Conclusion

An ultra-wideband CMOS CML-based divide-by-1.5 frequency divider is presented. By cascading divide-by-3 with multiply-by-2, divide-by-1.5 is realized. In the divide-by-3 circuit, fully differential and symmetric configuration benefits high-frequency division. In the multiply-by-2 block, two identical CML XOR cells with exchanged inputs are employed to strengthen the pull-down force, which guarantees fast-speed operation. Fabricated in TSMC 180 nm CMOS technology, the proposed wideband divide-by-1.5 has a measured operation frequency range of 0.3–4.4 GHz with a maximum power dissipation of 4.14 mW. The chip size is 0.02 mm².

Acknowledgments

This work was supported by the National Natural Science Foundation of China (grant: 61501453).