Nanowire Tunnel FET with simultaneously reduced Subthermionic Subthreshold Swing and Off-current due to Negative Capacitance and Voltage Pinning effects - Supporting Information

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Growth

Metal organic vapor phase epitaxy (MOVPE) growth was performed in an Aixtron CCS 18313 reactor with EPISON controllers to control the concentrations of the non-dopant metal-organic precursors used. The vapor-liquid-solid mechanism was utilized to grow nanowires from 44 nm diameter 15 nm thick Au seeds patterned by EBL on high resistivity Si(111) substrates with a 260 nm highly doped InAs layer on top. The total flow was 8000 sccm at a pressure of 100 mbar. The growth was initiated by 10 min annealing at 550° C in Arsine (AsH₃) followed by InAs growth at 460° C using Trimethylindium (TMIn) and Arsine (AsH₃) with a molar fraction of \( X_{TMIn} = 6.1 \times 10^{-6} \) and \( X_{AsH_3} = 1.3 \times 10^{-4} \), respectively. The bottom part of the InAs segment was n-doped by Tetraethyltin (TESn) (\( X_{TESn} = 6.1 \times 10^{-6} \)). The growth was then paused in an Arsine flow to reduce the amount of In dissolved in the Au seed particles. After this the InGaAsSb segment was grown using Trimethylgallium (TMGa) \( (X_{TMGa} = 4.9 \times 10^{-5}) \), Trimethylantimony (TMSb) \( (X_{TMSb} = 1.3 \times 10^{-4}) \), and AsH₃ \( (X_{AsH_3} = 5.1 \times 10^{-6}) \) corresponding to a gas phase composition of \( \text{AsH}_3/(\text{AsH}_3+\text{TMSb}) = 0.04 \). In remaining, the Au particle after the InAs growth is incorporated into the InGaAsSb segment. Finally, a GaSb segment was nucleated at 460° C with TMGa \( (X_{TMGa} = 4.9 \times 10^{-5}) \) and TMSb \( (X_{TMSb} = 1.3 \times 10^{-4}) \). The growth continued with reduced V/III \( (X_{TMSb} = 7.6 \times 10^{-5}) \) while heating to 515° C to avoid significant radial growth. Both the InGaAsSb and the GaSb segments were p-doped using Diethylzinc (DEZn) \( (X_{DEZn} = 1.9 \times 10^{-5}) \).

Fabrication

During the growth of GaSb segment, a shell was formed on the bottom segments, which was removed by subsequent digital etching steps. Ozone plasma was used to oxidize the surface followed by wet etching with citric acid to remove the oxide. This process also reduced the diameter of InAs and InGaAsSb segments down to 26 nm and 28 nm, respectively.
There was no observed etching of GaSb segment. Nanowires were covered with a high-K bilayer using atomic layer deposition. This layer was applied by using 5 cycles of Al₂O₃ and 36 cycles of HfO₂ at temperatures of 300° C and 120° C, respectively. A 30-nm-thick SiOₓ-bottom spacer layer, was deposited using thermal evaporation without tilt but with rotation. The thicker GaSb-segment helps to keep the channel region free of SiOₓ due to shadowing. However, sidewalls of the GaSb segment were covered with SiOₓ-flakes, which were removed in subsequent HF etching step. To compensate for the thinning of high-K, another 12 cycles of HfO₂ at 120° C were deposited. The gate was formed by first sputtering on a 30-nm-thick tungsten (W) layer, followed by spin-coating of the sample with S1800 resist. The physical gate-length was defined by the usage of an etch-back process, with O₂-plasma in a reactive ion etching reactor (RIE). Using RIE, the W was removed from exposed sections with SF₆/Ar. The gate-pad was defined utilizing photoresist and UV-lithography followed by etching of W in exposed regions. The top-spacer was formed by spin-coating the sample with S1800 photoresist followed by etching back of the resist to wanted thickness with RIE. UV-lithography and RIE were used to realize gate and drain vias. Formation of source and drain contacts began by removal of the high-K on top of the nanowires and in drain-via using HF, followed by sputtering of 10-nm-thick Ni and 150 nm-thick Au. The contact pads were patterned using UV-lithography and wet-etching.

**Characterization**

An SEM-image of a nanowire after the growth can be viewed in Figure 1a, and an illustration of the different segments and their doping in Figure 1b. Every device used in this paper has 184 nanowires divided into four parallel lines with nanowires into double rows as the SEM image in Figure 1c shows. The first step of the device fabrication was digital etching, to remove the GaSb-shell and reduce the diameter of the channel region down to 26 nm, thereby improving the electrostatics. Directly after the digital etching, a high-K bilayer (Al₂O₃/HfO₂) was deposited using atomic layer deposition. Estimated EOT of the high-K
layer was 1.4 nm. To separate the drain and gate regions, a 30 nm-thick SiO$_2$ spacer layer (Bottom-spacer), was deposited utilizing thermal evaporation. The gate layer was formed by sputtering a 30 nm-thick tungsten film, followed by definition of the physical length ($L_g = 240$ nm) using reactive ion etching and mask definition. A spacer to separate the source and gate metals (Top-spacer) was realized with S1800 photoresist. Top-contacts and pads were formed by sputtering on a Ni and an Au layer, followed by masking and UV-lithography. An illustration of a final device can be viewed in Figure 1d. Transfer data from one of the devices in Figure 1e, confirms that the devices exhibit good electrostatics with low drain induced barrier lowering (DIBL) and small hysteresis. However, there is some source depletion mainly observed at low drive voltage due to the gate overlap. The device exhibits a point subthreshold swing that is below 60 mV/decade, for both sweeps in forward and reverse direction, Figure 1f. Previously, devices with the same heterostructure but with fewer and thinner nanowires, have demonstrated an even lower subthreshold swing well below the thermal limit.$^{1,2}$ The output data shown in Figure 1g confirms that this device exhibits a negative resistance region (NDR). The highest peak-to-valley current ratio (PVCR) is 6.9 which is similar to values for devices with fewer nanowires obtained in.$^{2}$ This demonstrates a good uniformity between the nanowires in the array.

**Current Normalization**

All reported current values in the manuscript are normalized with respect to the channel width of baseline TFETs. The reference devices that have been employed for both PZT and Si:HfO$_2$-based NC-TFETs have the same physical dimensions, as it is schematically depicted in Figure 2a. Each transistor consists of 180 nanowires, having a pitch of 300 nm. The real measurement data and the normalized value of the gate and drain current, belongs to the reference device of the Si:HfO$_2$-based NC-TFET, are reported in Figures 2b and 2c.
Pb(Zr,Ti)O$_3$ (PZT)

Fabrication

For the first experiment, 46±3 nm of Pb(Zr$_{43}$,Ti$_{57}$)O$_3$ (PZT) ferroelectric film has been grown via the chemical solution deposition route (REF) on a Pt-coated silicon wafer. The stack of Pt(100 nm)/TiO$_2$(30 nm) has been sputtered on SiO$_2$(500 nm)/Si wafer at 300° C. The PZT film consisted of tetragonal ferroelectric phase with the predominant (100) orientation, with virtually no inclusion of any secondary non-ferroelectric phase like pyrochlore, as confirmed by XRD theta-2theta scans. The polycrystalline PZT film had a dense columnar grain structure with the grain size of 200±100 nm. Pt top electrodes were deposited on PZT film by sputtering and post-annealed at 550° C in an oxygen atmosphere in order to remove the sputtering damage at the Pt/PZT top interface.

Electrical Characterization

The ferroelectric capacitors exhibited the dielectric properties typical for high-quality ferroelectric PZT layers of this type as it is illustrated in Figures 3 and 4. Specifically, the polarization hysteresis loop measured at 1 kHz showed the remanent polarization of 25±3 \( \mu \)C/cm$^2$ and coercive fields of +80/-300 kV/cm, with the polarization imprint that favors the top-to-bottom polarization direction. Low-signal C-V measurements show the hysteretic behavior of the dielectric constant with the maximum values of 600-700 near the coercive voltage.

Training procedure

The negative capacitance (NC) effect has been reached using a chemical-solution-deposited polycrystalline PZT film. Generally, high-quality epitaxial ferroelectric layers are considered suitable for NC devices$^3$ as they are more likely to form a mono-domain state characterized by a single coercive field. This is in contrast to the typical behavior of the polycrystalline
films, which tend to form complicated poly-domain patterns with a broad distribution of nucleation energies and coercive fields (Figure 5a). We have shown that this behavior can be changed dramatically by applying a repetitive bipolar voltage stress known as the "training" procedure of ferroelectric. Piezoelectric loops measured through the top electrode of the PZT capacitor after 20 cycles at 7 V show sharp switching and nearly constant piezoelectric response amplitude (Figure 5b) within the voltage range from -2 V to 1 V (or from 2 V to -1 V). This behavior suggests that the poled ferroelectric layer approaches the mono-domain behavior and does not switch at least at low DC voltage up to 2 V. Note that the piezoelectric loops collected on the as-fabricated capacitor without any training reveal different behavior typical for region-by-region poly-domain switching expected from a polycrystalline film. The demonstration of NC effect using a polycrystalline ferroelectric layer constitutes a significant step towards the integration of NC gates in CMOS technology. In fact, fabrication of epitaxial perovskite layers on silicon is an extremely challenging task, whereas polycrystalline ferroelectrics like PZT can be integrated, as shown in previous reports.4,5

Silicon-doped HfO₂

Fabrication

Different thicknesses of silicon-doped HfO₂ films were deposited using atomic layer deposition (ALD) on silicon wafers covered by 10 nm of TiN as the bottom electrode of capacitors. The precursors were tetrakis(ethylmethylamino)hafnium (TEMAHf) for Hf and SiH₂(N(C₂H₅)₂)₂ (SAM24) for SiO₂. Ozone and water were used as the oxygen source. The deposition temperature was 300°C and the silicon concentration has been defined by the cycle ratio of SiO₂ and HfO₂. A 10 nm TiN capping layer was deposited by sputtering technique at room temperature on the oxide film prior to rapid thermal annealing (RTA) at 800°C for 20 s in a nitrogen ambient. The Metal-Insulator-Metal capacitor was completed by the deposition of 50 nm of Pt as the top electrode. The Pt layer was patterned using a lift-off process. Then
the top TiN was removed by a wet etching process, using RCA1 solution.

**Characterization**

Essential prerequisites for ferroelectric layers suitable for exploiting the NC effect include sharp and coherent switching and weak intrinsic leakage. In order to evaluate ferroelectricity in the Si:HfO$_2$ layer in the nanometer scale we measured local polarization switching and mapped the polarization domain structure using the off-resonance piezoelectric force microscopy (PFM). The technique has been enhanced for probing extremely weak electromechanical coupling typical for 10 nm HfO$_2$-based films with an outstanding sensitivity < 0.1 pm. For most device-relevant data the local piezoelectric response was detected through the top electrode, using a sub-coercive AC driving signal of 0.5 V/92 kHz. The resulting maps of amplitude and phase of the local piezoelectric response (Figure 6c) reveal a sharp polarization domain pattern expected for good quality polycrystalline ferroelectric layers. The loop of transverse piezoelectric coefficient $d_{33}$ measured through the top electrode shows that the polarization switches in a sharp, complete and saturating way, with a coercive voltage close to 1 V. An abrupt 180° flip of the phase of the local piezoelectric signal observed at the coercive voltage indicates that the leakage conduction is low and does not affect the measurements. The use of low leakage ferroelectrics is crucial for the NC effect because the leakage causes intrinsic polarization screening and therefore inhibits the conditions required for the NC regime.

For switching performance of polycrystalline ferroelectric films the grain boundaries often represent a critical issue. Charged defects accumulated at the grain boundaries can block propagation of polarization domains and/or pin the domain walls resulting in a domain pattern that closely follows the grain structure. The PFM data in Figure 6c suggests that the grain boundaries in the studied Si:HfO$_2$ layer do not obstruct the switching process. This is confirmed by the size of polarization domains of 50-300 nm, which incorporate many grains of Si:HfO$_2$ with an average size of about 25 nm. The sharp boundaries between
the polarization domains attest to the homogeneous ferroelectric phase, without any visible inclusions of secondary non-ferroelectric phase earlier reported in HfO$_2$-based ferroelectric films (REF). Thus the PFM analysis suggests that the structural features of the ferroelectric film do not significantly disturb the uniform polarization response required for the NC effect.

**Process Optimization**

The fabrication process of the silicon-doped HfO$_2$ is optimized by varying the silicon concentration, annealing temperature, and the film thickness to ensure a sufficient remanent polarization together with a relatively low leakage current (Figure 7). Figure 7a shows the impact of the silicon concentration on the polarization characteristic of the Si:HfO$_2$, having a thickness of 13.2 nm. The Si% has been defined by the cycle ratio of HfO$_2$ and SiO$_2$, i.e. HfO$_2$:SiO$_2$:HfO$_2$. The cycle ratio of 16:1:16, which leads to a silicon concentration of 3.4%, shows a higher remanent polarization and better ferroelectric response comparing other cycle ratios while the rest of the fabrication process was identical. Increasing or decreasing the Si% from the noted value degrades the polarization response of the Si:HfO$_2$ thin film. Figure 7b illustrates the effect of the annealing temperature on the ferroelectric behavior of silicon doped HfO$_2$. It is validated that a higher annealing temperature, 800$^\circ$ C comparing to 650$^\circ$ C, leads to a higher level of remanent polarization together with a higher leakage current. Any annealing temperature superior to 800$^\circ$ C causes a large amount of leakage current and hence, the P-V loop of the ferroelectric could not be measured. On the other hand, a Si:HfO$_2$ thin film annealed at a temperature lower than 600$^\circ$ C does not provide a sufficient level of remanent polarization. The impact of the layer thickness on the P-V curve of Si:HfO$_2$ is demonstrated in Figure 7c, degrading the ferroelectric properties by increasing the thickness. This is due to the fact that a lower portion of HfO$_2$ gets crystallized in a thicker film. Figure 7d compares the P-V curve of a Si:HfO$_2$ that is fabricated with the proposed optimized conditions of this work and previous reports.$^6$–$^8$
Experimental Configuration of NC-TFETs

As schematically shown in Figure 8, the experimental results are obtained by connecting an external PZT/Si:HfO$_2$ ferroelectric capacitor to the gate of a TFET. It should be noted that the baseline tunnel FET corresponds to InAs/InGaAsSb/GaSb nanowire TFETs. This external connection offers the flexibility of testing different series combinations and tuning the hysteresis behavior of NC-TFETs. The experimental setup used for the electrical characterization of NC-TFETs is presented in Figure 8 (left). The internal contact is probed while a voltage is applied to the top gate (a zero current is injected to the internal node). As reported before, this probing has a negligible impact on the reported subthreshold swing. An HP 4156A precision semiconductor parameter analyzer is employed for the electrical characterization of NC-TFETs in this study.

Impact of Temperature on TFETs Characteristic

As it is mentioned in the manuscript, regarding the high leakage of Si:HfO$_2$ ferroelectric capacitors that severely degrades the negative capacitance effect, the measurement of the Si:HfO$_2$-based NC-TFET have been performed at the low temperature of 80 K. This cancels out the trap-assisted tunneling (TAT) in the capacitor and reduces the leakage current by more than three orders of magnitude. In order to make sure that the low-temperature measurement does not severely affect the baseline TFET operation, the input transfer characteristic of the reference tunnel FET at room temperature and 80 K are compared. The main current mechanism in tunnel FETs is band-to-band tunneling of carriers from source to the channel, which is independent of the operating temperature. However, at high temperatures, trap-assisted tunneling also collaborates to the channel current. This impact is observable in Figure 9, where the $I_d$-$V_g$ curve of a TFET at 300 K and 80 K are compared. The input transfer characteristic of the TFET at 80 K is steeper and the $I_{off}$-current is lower comparing the room temperature measurement. This is due to the fact that the current
of the TFET at 80 K is purely a band-to-band tunneling current. It is worth noting that
the impact of the TAT in the employed TFETs of this work is weak as a result of the ex-
tremely low defect fabrication of the heterostructure which makes us eligible to demonstrate
a Si:HfO$_2$-based NC-TFET at low temperature of 80 K as a proof of concept.$^{1,2}$

**Output Transfer Characteristic of NC-TFETs**

In order to investigate the impact of negative capacitance effect on the output transfer
characteristic of NC-TFETs, I$_d$-V$_d$ curves of the reference TFET (corresponding to the case
of the PZT-based NC-TFET) and NC-TFET are plotted in Figure 10. Figure 10a shows
the output transfer characteristic of the baseline TFET while V$_{gs}$ was swept from -100 mV
to 200 mV with a 100 mV step. Figure 10b demonstrates the I$_d$-V$_d$ curve of the NC-TFET
for both forward and reverse sweeps of the drain voltage. The gate voltage was set in order
to provide internal voltages, V$_{int}$, corresponding to the V$_{gs}$ of the previous case. Figure
10c compares the I$_d$-V$_d$ curves of the baseline TFET with the one of NC-TFET (forward
sweep). It is evident that by sweeping the drain voltage, there is no considerable impact
due to the negative capacitance. This is due to the fact that sweeping of the drain voltage
does not provide any considerable change in the vertical electric field inside the ferroelectric.
Hence, ferroelectric dipoles do not change their stable state and the capacitor acts as a linear
dielectric. In this case, the structure works as a capacitive voltage divider between V$_{gs}$ and
V$_{int}$.

**Off-Current Reduction in NC-TFETs**

It is evident that the off-current of NC-TFETs is considerably lower than the one of the
reference device (Figure 11a). This can be explained by focusing on the internal voltage, the
actual gate voltage of the baseline TFET, and the related band diagram of the TFET. Here,
we explain the impact on the PZT-based NC-TFET and it would be similar for Si:HfO$_2$-
based NC-TFET. The measured internal voltage of the NC-TFET, $V_{\text{int}}$, demonstrates that the gate voltage of the baseline TFET is almost constant in the OFF state, having an average of -0.08 V. This happens as a result of the charge balance condition between the ferroelectric dipoles and electrical charges in the channel. Therefore, the PZT capacitor set the internal voltage at -0.08 V. The band diagram of the TFET in the OFF state is simulated and compared with various gate biases, using the Silvaco Atlas commercial TCAD tool. The physical parameters of the InAs/InGaAsSb/GaSb nanowire have been chosen in correspondence to the fabricated TFET. Figure 11c depicts the band diagram of the InAs(n++)/InAs(n−)/InGaAsSb(p++)/GaSb(p++) nanowire TFET while the gate bias of -0.08 V is applied. Figure 11c demonstrates the band diagram of the nanowire TFET, showing that there is no narrow tunneling path available in the source-channel or drain-channel junction. This is the main reason that the proposed NC-TFET provides a remarkably low off-current. A value of $V_{\text{int}}$ lower than -0.08 V, -0.5 V in case of Figure 11d, effectively reduces the tunneling barrier near the channel-drain junction and creates a leakage path which extends by using lower internal voltages. On the other hand, a high $V_{\text{int}}$, such as 0.0 V and 0.5 V that are presented in Figures 11e and 11f, provides a tunneling path in the source-channel junction and the TFET operates in the ON state. In short, the reduction of the off-current in the proposed NC-TFETs is due to the fact that the ferroelectric dipoles set the value of the internal node in a voltage that blocks the tunneling current in the OFF state.

**Gate Leakage Current**

The gate leakage current of the baseline TFET, PZT-based NC-TFET, and Si:HfO$_2$-based NC-TFET is depicted in Figure 12. The leakage current of all cases is relatively low and negligible compared to the drain current and therefore, it can be neglected in the reported effects. There is no clear correlation and impact of the leakage current on the transfer
characteristic of our devices which is mainly due to the following reasons: (i) Although the baseline transistor of all devices where fabricated in the same batch with the same physical dimensions, due to the process variation the transfer characteristic of the base device were different. (ii) The gate leakage current that we have reported here is the measured current of the gate terminal. This means that it does not only correspond the gate current of the reference TFET and also includes the dipole polarization switching current of the ferroelectric capacitor. (iii) The two ferroelectric capacitors that have been used in this work have totally different properties, PZT has a much lower leakage and higher polarization comparing to Si:HfO$_2$. As a result of the noted reasons, it is not possible to define any correlation between the measured gate leakage current and transfer characteristics of the reported devices of this work.

**Benchmarking**

Table 1: Performance of reported NC-FETs comparing the proposed Si:HfO$_2$-based NC-TFET of this work.

| Device type | Ferroelectric | $L_g$ | Hysteresis | $SS_{min}$ | $I_{ON}/I_{OFF}$ | Range |
|-------------|---------------|-------|------------|-----------|-----------------|-------|
| Si- nMOSFET$^1$ | PZT | 10 µm | 12 V | 13 mV/dec | $10^9$ | 1 |
| Si- FinFET$^{10}$ | BiFO$_3$ | 100 nm | 5 V | 15 mV/dec | $10^6$ | 7 |
| Si- nMOSFET$^{11}$ | PVDF | - | $\approx$ 0 V | 52 mV/dec | $10^7$ | 2-4 |
| Si- nMOSFET$^{12}$ | PZT | 70 nm | 1 V | 20 mV/dec | $10^5$ | 5 |
| Si- nMOSFET$^{13}$ | HZO | - | 100 mV | 52 mV/dec | $10^4$ | 1-2 |
| Ge- NW FET$^{14}$ | HZO | 80 nm | $\approx$ 0 V | 54 mV/dec | $5.3 \times 10^4$ | 1 |
| Ge- FinFET$^{15}$ | HZO | 60 nm | $\approx$ 0 V | 58 mV/dec | $3.8 \times 10^7$ | 1-2 |
| Si- nMOSFET$^{16}$ | Al: HfO$_2$ | 30 µm | $\approx$ 10 mV | 40 mV/dec | $10^6$ | 1-2 |
| TFET- This Work | Si: HfO$_2$ | 240 nm | $> 50$ mV | 15 mV/dec | $10^5$ | 5 |

The reported NC-TFETs in this manuscript is the first experimental demonstration of negative capacitance tunnel FETs with a sub-60 mV/decade swing. Therefore, we have benchmarked the proposed NC-TFET with the previously reported negative capacitance MOSFETs. Due to the high interest in the recently proposed CMOS compatible ferroelectric, doped HfO$_2$, the performance of the reported Si:HfO$_2$-based NC-TFET is compared with the
recently reported NC-FETs. Despite the fact that the Si:HfO$_2$-based NC-TFET of this work is measured at 80 K, it is possible to compare it with NC devices at room temperature as the performance of tunnel FETs is almost independent of the operating temperature. Hence, the DC electrical performance of the proposed Si:HfO$_2$-based NC-TFET is demonstrated and compared with reported NC-FETs in Table 1. The proposed NC-TFET with a minimum swing of 15 mV/decade, a sub-thermal swing over 5 decades of current, a relatively high $I_{ON}/I_{OFF}$ ratio of 5, and an extremely low off-current together with a negligible hysteresis below 50 mV, shows a significant performance boosting that is obtained using NC effect of Si:HfO$_2$.

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Figure 1: Baseline TFET structure and electrical characterization. (a) SEM image of an InAs/InGaAsSb/GaSb nanowire after growth. The nanowire has three segments, where the InAs/InGaAsSb heterojunction is marked with a dotted arrow. (b) Schematic illustration of the nanowire including the doping profile. The composition of segment 2 is x=0.29 and y=0.66. (c) SEM image of nanowires in an array with 46 nanowires. (d) Schematic diagram of all layers of the device (the thickness of some layers has been enlarged for clarity). (e) Transfer data for one of the devices with forward and reverse direction sweeps at drain voltages of 50 mV and 500 mV. At low drive voltage, there is an impact from source depletion due to the overlapping gate. (f) Subthreshold swing as a function of $I_d$. In spite of a large number of relatively thick nanowires, $SS_{min}$ is lower than 60 mV/decade. The sweep direction has only a minor impact on SS. (g) Output data from the same device, showing a superlinear behavior in the reverse direction and a negative differential resistance in the forward direction. The highest peak-to-valley current ratio (PVCR) is 6.9 (inset).
Figure 2: Current normalization. (a) shows the schematic diagram of the employed reference TFETs in the PZT and Si:HfO₂-based NC-TFETs. In both cases, the baseline device has 180 nanowires with the presented dimensions and a pitch of 300 nm. The measured and normalized values of the drain and gate currents are demonstrated in (b) and (c), respectively.
Figure 3: The electrical and physical characterization of PZT ferroelectric thin film. 46 nm of PZT with 43/57 (Zr/Ti) ratio is deposited on a TiO$_2$/(2 nm)/Pt(100 nm)/TiO$_2$/Ti/SiO$_2$/Si substrate by employing the sputtering technique. A Pt top electrode is deposited at room temperature and patterned by shadow masking. The film polarization, permittivity, and the phase angle of the capacitance measurement hysteresis loops regarding the applied voltage (electric field) on the ferroelectric layer are depicted in (a). The relative permittivity of the PZT thin film is 220 – 240. The SEM analysis (b) and XRD 2-theta profile (c) of the PZT thin film illustrate that the film is polycrystalline (see microstructures in SEM image) and textured 111-oriented, which is the most commonly used orientation.
Figure 4: The polarization (a) and current (b) hysteresis loops of the fabricated PZT capacitor. The extracted values of the coercive field and remanent polarization are around 260 KV/cm and 25 μC/cm² respectively.

Figure 5: Piezoelectric response of the PZT thin film. The results are measured before (a) and after (b) the training procedure. This behavior suggests that the poled ferroelectric layer approaches the mono-domain behavior and doesn’t switch at least at low DC voltages.
Figure 6: Ferroelectricity in CMOS compatible ferroelectric, Si:HfO₂. (a) P-V curve (left) that is measured through the top electrode of the Si:HfO₂ capacitor, having a thickness of 13.2 nm and a Si concentration of 3.4%. The right image shows the crystal structure of Si:HfO₂ in two stable polarization states. (b) AFM results on the surface of Si:HfO₂ confirms the conformality that was expected from atomic layer deposition technique. (c) The maps of amplitude and phase local piezoelectric response reveal a polarization domain pattern typical for good quality polycrystalline ferroelectrics (left). The loop of transverse piezoelectric coefficient d₃₃ through the top electrode shows that the polarization switches in a sharp, complete and saturated way.
Figure 7: Process optimization of Si:HfO₂. (a) Impact of Si% on the polarization characteristic of Si:HfO₂ thin film. The Si% is varied by the cycle ratio of HfO₂ and SiO₂. The legend is depicted in correspondence to the HfO₂:SiO₂:HfO₂ cycle ratio. The 16:1:16 condition provides the highest level of remanent polarization, corresponds to the silicon concentration of 3.4%. (b) Effect of the annealing temperature on polarization and leakage current of the Si:HfO₂ is investigated at 800°C and 650°C (20 s). (c) Increasing the thickness reduces the crystallized portion of Si:HfO₂ and hence, the remanent polarization. (d) The optimized conditions of Si:HfO₂ in this work is compared with the previously reported results, showing a similar remanent polarization and a relatively lower leakage.
Figure 8: Experimental configuration of the NC-TFET including the measurement setup utilized for probing the internal voltage (left) and the simple capacitance model of the structure (right).

Figure 9: Impact of the temperature on the operation on reference TFETs. $I_d$-$V_g$ curve of a TFET at room temperature is compared with the input transfer characteristic of the same device at 80 K.
Figure 10: Impact of NC on output transfer characteristic of NC-TFETs. (a) demonstrates the $I_d$-$V_d$ curve of the baseline TFET for gate voltages from -100 mV to 200 mV. (b) compares the output transfer characteristic of the NC-TFET for the forward and reverse sweeps of the drain voltage. The gate voltage has been tuned to provide an internal voltage corresponding to the previous case. (c) $I_d$-$V_d$ plot of the forward sweep of the NC-TFET shows similar results comparing to the baseline TFET. It should be noted that the $V_{gs}$ of the NC-TFET was tuned to provide an internal voltage ($V_{int}$) similar to the gate voltage of the reference TFET.
Figure 11: Impact of the ferroelectric capacitor on off-current of the NC-TFET. (a) $I_d-V_{gs}$ curve of the PZT-based NC-TFET comparing with the reference device, showing a considerable off-current reduction. The measured internal voltage (b) demonstrates a relatively constant voltage around -0.08 V on the gate of the baseline TFET during the OFF state. The simulated band diagram of the TFET depicts that with a gate voltage around -0.08 V (c), there is no tunneling path in the OFF state. On the other hand, any gate voltages lower (d) or higher than the mentioned value (e) and (f), provides a tunneling region that causes leakage current while the device operates in the OFF region.

Figure 12: Gate leakage current. The gate leakage current of the baseline TFET (a), PZT-based NC-TFET (b), and Si:HfO$_2$-based NC-TFET (c).