A 92 fs\textsubscript{rms} jitter frequency synthesizer based on a multicore class-C voltage-controlled oscillator with digital automatic amplitude control

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Abstract This letter presents a frequency synthesizer based on a multicore Class-C voltage-controlled oscillator (VCO) with a digital automatic amplitude control (AAC) loop. A novel digital tail current estimation is adopted to mitigate the risks of unexpected VCO oscillation failure, due to current shortage during frequency calibration. Meanwhile, a digital amplitude recalibration is proposed to provide continuous amplitude control, avoiding noise distortion resulted from amplitude drift after a conventional disposable amplitude calibration. The digital AAC loop achieves a specific VCO amplitude with good stability and introduces no extra noise. Fabricated in a 28 nm CMOS process, the presented frequency synthesizer occupies an active area of $1.43$ mm$^2$. By measuring a 3 GHz carrier, the open loop VCO phase noise is $-132$ dBc/Hz at 1 MHz offset and the close loop root mean square jitter is 81 fs.

Keywords: phase-locked loop (PLL), voltage-controlled oscillator (VCO), automatic amplitude control (AAC), phase noise, jitter

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Direct-RF sampling data converters [1, 2, 3, 4, 5] simplifies transceiver systems by eliminating frequency conversion stages. For multi-GHz signal sampling, phase noise (PN) of the clock signal generated from the frequency synthesizer has a significant effect on the noise performance of data converters [6, 7]. Frequency synthesizers based on charge pump phase-locked loops (CPPLL) with octave-range VCOs are widely adopted to satisfy the noise requirement and to cover various frequency bands [8, 9, 10, 11, 12].

Octave-range VCOs commonly suffer from a trade-off between tuning range and phase noise. The switched-capacitor banks (SCB) adopted for wider tuning range induce a variation in the amplitude of the VCO output signal, as a result, degrade the out-of-band noise performance of the CPPLL. Therefore, efforts have been made in automatic amplitude control (AAC) systems [13, 14, 15, 16]. However, analog AAC loops inject extra noise so that large current is required to reduce the injected noise [13]. Meanwhile, analog AAC loops suffer from stability problems especially when they are adopted in Class-C VCOs with start-up loops [17, 18, 19, 20, 21]. Therefore, digital AAC techniques have been proposed to eliminate the noise and stability problems [22, 23]. However, in most of the reported works, the trigger to start amplitude calibration were not specified, and these systems were vulnerable to applications where the temperature changes continuously. For example, if the VCO is adopted in a high speed data converter, the high power consumption will heat the chip gradually. Therefore, the continuous amplitude monitoring and recalibration are essential for such practical application.

This letter presents an Integer-N frequency synthesizer with an integrated octave-range Class-C VCO, which employs the proposed digital AAC loop. The digital AAC loop is optimized with a novel digital tail current estimation and an amplitude recalibration. The tail current estimation guarantees a definite and stable initial current needed in the automatic frequency calibration (AFC) process. The proposed amplitude recalibration detects the amplitude drift and operates recalibration to reduce noise distortion resulted from probable PVT variation after traditional single calibration.

2. Multicore class-C VCO

As shown in Fig. 1, the presented frequency synthesizer is architected in a type-II CPPLL structure. A phase and frequency detector (PFD), a feedback frequency divider chain (/N FB) and an output frequency divider (/N Output) are designed with CMOS logic circuits. The frequency division ratio of the frequency divider chain ranges from 1 to 120, therefore the synthesizer’s output signal frequency varies from 50 MHz to 12GHz. A charge pump (CP) with a common mode feedback is designed to reduce the reference spur. A bandwidth-programmable loop filter (LF) and an octave-range Class-C VCO are integrated on-chip. A digital finite state machine (FSM) is adopted to realize the AFC and the AAC. The FSM is clocked by a divided reference clock.

To generate low-phase-noise clock signals from 50 MHz to 12 GHz, the octave-range VCO is designed using four dynamic-biased Class-C VCO cores as shown in Fig. 2. Each core covers 20% frequency range by the combination of SCB...
and varactors. The SCB and varactors are designed to cover every frequency spot with at least two frequency bands to guarantee tuning continuity. The $K_{\text{VCO}}$ of each band is limited between 40 MHz/V and 80 MHz/V to reduce noise injected from the low-dropout regulator (LDO).

For further noise reduction, each core couples two VCO cells shown in Fig. 3 with ultra-thick metal lines. Due to low parasitic resistance of the metal lines, the 3 dB phase noise reduction is fully preserved [24, 25, 26]. Furthermore, in each VCO cell, a dynamic-biased Class-C loop is adopted to reduce the power consumption. The low gate bias voltage prevents the transistors from entering triode region, leading to high current efficiency and low phase noise [17, 27, 28]. The feedback loop also solves the inherent start-up problem under low gate bias voltage.

### 3. Digital automatic amplitude controlling

In this design, a modified digital AAC scheme with tail current estimation and amplitude recalibration is introduced.

The tail current estimation reduces the cycles needed for calibration and guarantees a robust start-up. The amplitude recalibration works when the chip temperature changes after a traditional single calibration to reduce phase noise distortion caused by new amplitude drift.

#### 3.1 Digital tail current estimation

In an AFC process, the initial current code for each frequency band should be large enough to guarantee a robust start up. Recent works solve this problem by starting from the largest current [29] or by saving the initial current code in a large amount of registers [30]. However, these methods cause reduction in the lifetime of transistors and also waste time for calibration and chip area. In this work, these problems are solved by the proposed digital tail current estimation.

In order to keep a constant VCO output amplitude, the tail current $I_{\text{tail}}$ should be adjusted accordingly with the equivalent parallel resistance $R_p$ across the resonator, which is mainly affected by the SCB. The structure of a SCB cell is shown in Fig. 4. The inverter sets the bias voltage of the switches $M_{1-3}$ through $R_{\text{bias}}$ to prevent the junctions of $M_{1-3}$ from breakdown in the presence of high voltage swings. $M_5$ and $M_3$ improve the Q-factor in on-state but increases the parasitic capacitance in off-state. According to [31], the Q-factor of the inductor is much lower than the rest parts. Therefore, the equivalent parallel resistance across the LC-tank can be derived as:

$$R_p = \frac{2\pi \cdot f_{\text{osc}}^2}{R_s} = \frac{L}{R_s C}$$  \hspace{1cm} (1)

where $f_{\text{osc}}$ is the oscillation frequency and $R_s$ is the series parasitic resistance of the inductor. For a properly biased Class-C VCO, to keep a constant amplitude, the required tail current $I_{\text{tail}}$ is derived as:

$$I_{\text{tail}} \propto \frac{\Delta A_{\text{tank}}}{R_p} = \frac{A_{\text{tank}} R_s (C_0 + \Delta C)}{L}$$  \hspace{1cm} (2)

where $A_{\text{tank}}$ is the single-ended peak-to-peak output swing of the VCO, $C_0$ is the total capacitance in the LC-tank at the highest frequency and $\Delta C$ is the capacitance change at $f_{\text{osc}}$ compared with $C_0$. Therefore, $I_{\text{tail}}$ is proportional to the capacitance controlled by $\text{band}_{\text{sel}}<6:0>$. When the AFC process selects a new frequency band, a new current code $\text{cur}_{\text{sel}<8:0>}$ can be calculated by the following equation:

$$\text{cur}_{\text{sel}<8:0>} = \text{current}_{0<8:0>} + \alpha \cdot \text{band}_{\text{sel}<6:0>}$$  \hspace{1cm} (3)

where $\text{current}_{0<8:0>}$ is the current code when the VCO oscillates at the highest frequency, at which the VCO consumes the least current, $\alpha$ equals to $(I_{\text{max}} - I_{\text{min}})/127$. $I_{\text{max}}$ and $I_{\text{min}}$
are the optimized tail currents for the lowest and the highest frequency, respectively. Fig. 5(a) shows the simulated relationship between \( R_p \) and \( I_{\text{tail}} \). With (3), the estimated \( I_{\text{tail}} \) guarantees a robust start-up and a stable amplitude. The VCO amplitude after digital automatic amplitude calibration at different frequency is shown in Fig. 5(b).

3.2 Amplitude recalibration

Most reported digital AAC loops will stop running after a single calibration. However, a high-speed data converter heats the chip significantly, the digital AAC loops are required to monitor the amplitude of VCO continuously and to adjust the amplitude when the chip temperature changes.

The proposed amplitude recalibration starts to monitor the amplitude after the PLL locks. The comparators provide a programmable amount of hysteresis that guarantees the stability of monitoring loop. When the amplitude drifts significantly, the comparators can detect the variation and change the output \( \text{amp}_\text{high} \) and \( \text{amp}_\text{low} \), which mean that the amplitude is too large or too small, respectively. Then the digital AAC loop will start amplitude recalibration to reduce the noise distortion caused by new amplitude drift.

3.3 Circuit implementation

As shown in Fig. 2, the proposed digital AAC loop consists of a peak detector, a source follower, two hysteresis voltage comparators and an FSM. The peak detector generates a signal that is proportional to the VCO amplitude [14] and compares it with referential voltages. It is worth noting that PVT change will result in a variation in the \( V_{th} \) of the peak detector’s input transistors, so we adopt a source follower to copy the \( V_{th} \) variation. The FSM adjusts \( \text{cur}_\text{sel}<8:0> \) according to the comparators’ outputs. Resulted from the precise comparator and fine current adjustment step, the digital AAC loop realizes an accurate and flexible amplitude control.

Fig. 6 shows the flow chart of the modified digital AAC process. An estimated current for the selected frequency band will be set in mode 1 when the AFC process selects a new frequency band. The second mode continuously monitors the amplitude and carries out recalibration whenever PVT change results in amplitude drift.

As the digital loop only controls the switching of the tail current, the digital AAC loop injects no extra noise from the tail current source to the LC-tank. Compared with conventional analog AAC loops, the size of filtering capacitor and current of the peak detector used to reduce noise from the peak detector are minimized. Therefore, there is no need to trade-off among the noise, area and power consumption of the peak detector. Fig. 5(b) compares the simulated VCO’s amplitude drift. The digital AAC can optimize the drift from 400mV to 15 mV.

4. Measured results

The frequency synthesizer is fabricated in a 28nm CMOS process and occupies a 1.43 mm\(^2\) chip area. Fig. 7 shows the micrograph of the frequency synthesizer. Measured from a digital-to-analog convertor (DAC), when the VCO oscillates at 12 GHz and output frequency dividing ratio is 2, the output

![Fig. 5](image-url)  
(a) Simulated \( R_p \) is inverse proportional to frequency band in core0 and the compensated current is proportional to the band. (b) Simulated VCO amplitude indicates that the DAAC limits the amplitude drift within 15 mV throughout the whole tuning range.

![Fig. 6](image-url)  
Fig. 6  Proposed digital AAC flow chart.

![Fig. 7](image-url)  
Fig. 7  Micrograph of the frequency synthesizer.
signal frequency with an external divide-by-two divider is 3 GHz and the open loop VCO PN reaches \(-132\) dBc/Hz at 1 MHz offset. The results of recalibration are shown in Fig. 8. The PN deterioration at 1 MHz offset is reduced by 1.6 dB at 125°C and 2.2 dB at \(-40°C\) respectively. Fig. 9 shows that with a 500 MHz reference clock, the frequency synthesizer achieves an 81 fs root mean square (RMS) jitter integrated from 10 kHz to 10 MHz. By changing the reference clock, the measured RMS jitter over the whole VCO frequency range is lower than 92 fs.

Table I [32, 33, 34, 35] compares the performance of the proposed frequency synthesizer with other reported works. This work achieves low phase noise and RMS jitter with the widest tuning range.

### 5. Conclusion

A frequency synthesizer based on a multicore Class-C VCO, and a modified digital AAC loop has been implemented. The multicore structure widens the frequency range with low deterioration in phase noise. The Class-C feedback loop guarantees a robust VCO start-up and realizes low phase noise and low power consumption. The digital AAC loop provides a constant VCO output amplitude at variant frequency bands and prevents amplitude drift resulted from temperature change with amplitude recalibration. The circuit shows superior noise performance and good stability against temperature variation. Measured from the output of the data converter, the RMS jitter is lower than 92 fs across the tuning range.

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