A graphical approach for controller design with desired stability margins for a DC–DC boost converter

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Abstract
A novel graphical tuning method of PID controller for output voltage regulation of a DC–DC boost converter is proposed. The advantage of the presented method is that the desired robustness level in terms of gain and phase margins can be pre-specified. A technique to limit the noise level in the control signal to a pre-specified value by selecting the derivative gain ($k_d$), is also discussed. Simplicity of the technique is an added advantage. Concept of root crossing boundaries along with the gain phase margin tester is applied to compute constant gain and phase margin boundaries in the controller parameters plane. The overlapping area of constant gain and phase margin boundaries within the all stability region is the desired gain and phase margin region (DGPMR). Controller parameters are obtained by computing the centroid of the triangular convex region of the DGPMR. Effectiveness of the proposed tuning strategy is illustrated by simulation and hardware experimental results. Furthermore, the proposed method yields improved closed-loop performance compared to a recently reported tuning strategy in nominal as well as perturbed scenarios.

1 | INTRODUCTION

DC–DC boost converters are used in applications that require output voltage higher than the input voltage. It finds wide application in renewable energy processing, electric vehicles, battery sources, fuel cells, DC motor drives, radar systems, personal computers, pulsed laser, street and industrial lighting, etc. [1, 2]. For the above-said applications, it is necessary to track and regulate the output capacitor voltage in the presence of significant input voltage fluctuation and load variation. Research on control of boost converter has drawn significant attention due to its implicit difficulties such as non-minimum phase (NMP) nature, non-linear characteristic and variation in system parameters (inductance and capacitance) [3]. Presence of RHP zero in boost converter increases the overall phase lag, causes inverse response phenomenon and tends to destabilize the system. Furthermore, the RHP zero imposes limitation on the achievable closed-loop bandwidth and thereby on the speed of the dynamic response [1]. Numerous control strategies have been reported in the literature for output voltage regulation of boost converter. $H^\infty$ control theory was used for output voltage control in [4]. A comprehensive review and some general design issues related to sliding mode controllers for boost converter were presented in [5]. However, sliding mode controllers have chattering problem and it enhances the ripple content in output voltage. In [6], an optimal linear quadratic regulator (LQR) using convex optimization method was proposed for the boost converter. A model predictive control (MPC) approach has been reported in [7]. A robust control scheme using the concept of time-delayed switching was designed in [8]. A two degree-of-freedom internal model controller for output voltage regulation of boost converter was experimentally evaluated in [9].

Despite many recent theoretical and practical developments in modern control theory, PID controllers are still most widely used in industries. This is because of its simplicity, robustness, acceptable control effort and an outstanding cost/benefit ratio with satisfactory performance for a large class of process models. Furthermore, PID controllers can be easily implemented on analogue as well as digital hardware. In [10], authors have designed a PID controller for boost converter using a novel optimization algorithm named as Bees GA, which combines the evolution of a queen bee in a hive with Genetic Algorithm (GA). Rise time, peak overshoot, settling time and
steady-state error of output voltage response of the boost converter were used to formulate the objective function for the optimization process. In [11], authors have used an optimization algorithm based on the foraging behaviour of a colony of honey bees to obtain the optimal values of PID controller for the boost converter. A modified form of particle swarm optimization (PSO), namely probabilistic PSO was applied to compute the PID controller parameters in [12]. Three different evolutionary algorithms, namely genetic algorithm (GA), differential evolution (DE) and artificial immune system (AIS) were used to design the PID controller in [13]. Objective function based on the error between the desired reference voltage and the actual output voltage was used in the optimization algorithms. However, the above-reported approaches do not guarantee robustness to system parameter variations. Tuning rules for a PI controller in terms of boost converter parameters to ensure stability were obtained in [14]. In [15], authors have tuned the PID controller by Ziegler–Nichols method, internal model control (IMC) method, synthesis method and equating coefficient method. It was observed from the results that the synthesis method yields the least ISE value. Complete root contour (CRC) method was used for controller design of boost converter in [16]. PID controller parameters for buck and boost converters were obtained from a switching surface based on a state trajectory in [17].

Since closed-loop stability is the primary requirement, it is desirable to obtain all stabilizing PID gains set before controller tuning. Various methods have been reported in the literature to compute the all stabilizing PI, PD and PID controllers such as Nyquist plot approach [18], D-decomposition method [19], stability boundary locus approach [20], singular frequency method [21], kronecker summation method [22], Hermite–Biehler theorem [23], signature method [24]. Gain and phase margins are the two commonly used relative stability measures. All stabilizing PI/PID controllers with user-defined gain and phase margins have been computed in [19, 23].

A robust and non-fragile PI controller was designed by calculating the centroid stable point of the all stability region in [25]. PI/PD controller parameters were obtained by computing weighted geometrical centre (WGC) from the all stability region in [26]. A method for obtaining the PI/PD controller parameters by calculating the centroid from the all stability region has been reported in [27]. However, the above three reported methods do not guarantee a desired degree of robustness. Moreover, procedure to tune the PID controller was not addressed.

A novel and simple graphical tuning method is presented in this paper which ensures desired stability margins and also limits the noise level in the control signal to a pre-specified value. All stability region is obtained by computing different root crossing boundaries in the controller parameters plane. Furthermore, the desired gain and phase margin boundaries are obtained using the gain phase margin tester (GPMT). Overlapping area of the above-said boundaries inside the all stability region is called the desired gain and phase margin region (DGPMR). Required controller parameters are obtained by computing the centroid of the triangular convex region of the DGPMR.

The paper is organized as follows: Mathematical model of the boost converter is derived in Section 2. Controller design is addressed in Section 3. Simulation, hardware experimental results and comparison are given in Section 4 whereas Section 5 provides the concluding remarks about the proposed work.

2 | MATHEMATICAL MODEL OF DC–DC BOOST CONVERTER

Figure 1 shows the equivalent circuit of a DC–DC boost converter, where \( v_{in}(t) \), \( i_{L}(t) \) and \( i_{D}(t) \) are the dc input voltage, output capacitor voltage and inductor current, respectively. \( R \), \( L \), \( r_{L} \) and \( C \) denote the load resistance, inductance, ESR of the inductor and output capacitance, respectively. Perturbation in load current is denoted by \( \dot{i}_{L}(t) \). The switch \( M \) and the diode \( D \) operate complementarily in continuous conduction mode (CCM). Dynamics of the boost converter operating in CCM can be expressed by following state-space equations,

\[
\begin{bmatrix}
\dot{i}_{L}(t) \\
\dot{v}_{0}(t)
\end{bmatrix} = \begin{bmatrix}
-\frac{r_{L}}{L} & -\frac{1}{L} \\
\frac{1}{C} & -\frac{1}{RC}
\end{bmatrix} \begin{bmatrix}
i_{L}(t) \\
v_{0}(t)
\end{bmatrix} + \begin{bmatrix}
1 \\
0
\end{bmatrix} v_{in}(t),
\]

where, the value of \( m(t) \) is ‘0/1’ when ‘M’ is ‘ON/OFF’. Presence of switch in the circuit makes the above state-space equation discontinuous with respect to time. Controller design generally requires averaged model of the switching power converters [1]. Control input (duty cycle), \( u(t) \) is the average value of \( m(t) \) over a complete switching cycle. Perturbation signals about the nominal steady-state values are introduced to obtain the small-signal model of the boost converter as follows:

\[
v_{in}(t) = V_{in} + \dot{v}_{in}(t),
\]

\[
i_{L}(t) = I_{L} + \dot{i}_{L}(t),
\]

\[
v_{0}(t) = V_{0} + \dot{v}_{0}(t),
\]

\[
u(t) = U + \dot{u}(t),
\]

where steady-state values are represented by upper case letters, while ‘ \( \dot{\cdot} \)’ denotes corresponding perturbed values. From the control point of view, \( \dot{v}_{in}(t) \) and \( \dot{i}_{L}(t) \) denote the disturbances in input voltage and load current, respectively. Steady-state values of inductor current and output voltage are obtained by equating the derivatives in (1) to zero and are obtained as follows:

\[
I_{L} = \frac{V_{in}}{r_{L} + R(1 - U)^2},
\]

\[
V_{0} = \frac{R(1 - U)V_{in}}{r_{L} + R(1 - U)^2}.
\]

The state trajectory is given in Section 2.
where $U$, $V_{in}$ and $R$ represent nominal values of duty ratio, input voltage and load resistance, respectively. Substituting (2) in (1), we get

$$
\begin{bmatrix}
i_L + \dot{i}_L(t) \\
V_0 + \dot{V}_0(t)
\end{bmatrix} = \begin{bmatrix}
\frac{-r_L}{L} & -\frac{(1 - U - \hat{u})}{L} \\
\frac{1}{C} & -\frac{1}{RC}
\end{bmatrix}
\begin{bmatrix}
i_L(t) \\
V_0(t)
\end{bmatrix}
+ \begin{bmatrix}
1 & 0 \\
0 & -\frac{1}{C}
\end{bmatrix}
\begin{bmatrix}
(V_{in} + \hat{v}_{in}(t)) \\
\dot{i}_d(t)
\end{bmatrix}.
\quad(4)
$$

Considering only the perturbed values and the first-order terms, the small-signal model of the system defined by (1) is obtained as

$$
\begin{bmatrix}
i_L(t) \\
\dot{V}_0(t)
\end{bmatrix} = \begin{bmatrix}
\frac{-r_L}{L} & -\frac{(1 - U)}{L} \\
\frac{1}{C} & -\frac{1}{RC}
\end{bmatrix}
\begin{bmatrix}
i_L(t) \\
\dot{V}_0(t)
\end{bmatrix}
+ \begin{bmatrix}
1 & 0 \\
0 & -\frac{1}{C}
\end{bmatrix}
\begin{bmatrix}
\dot{v}_{in}(t) \\
\dot{u}(t)
\end{bmatrix}.
\quad(5)
$$

Taking Laplace transform of (5), the small-signal transfer functions from control-to-output voltage, load-to-output voltage and load current-to-output voltage are obtained as follows:

**Control input to output voltage transfer function:**

$$
G_p(s) = \frac{\dot{v}_0(s)}{\dot{u}(s)} = \frac{(1 - U) V_0 - r_L I_L - L \dot{I}_L s}{LC^2 + (CR_l + L_0) s + \frac{r_L}{R} + (1 - U) s^2}.
\quad(6)
$$

**Input voltage to output voltage transfer function:**

$$
G_{d1}(s) = \frac{\dot{V}_0(s)}{\dot{v}_{in}(s)} = \frac{(1 - U)}{LC^2 + (CR_l + L_0) s + \frac{r_L}{R} + (1 - U) s^2}.
\quad(7)
$$

**Load current to output voltage transfer function:**

$$
G_{d2}(s) = \frac{\dot{I}_d(s)}{\dot{i}_d(t)} = \frac{-L \dot{I}_L - r_L I_L}{LC^2 + (CR_l + L_0) s + \frac{r_L}{R} + (1 - U) s^2}.
\quad(8)
$$

From (6), it is observed that control input to output voltage transfer function contains one RHP zero, whose location in s-plane is given by

$$
\omega_{RHPZ} = \frac{V_0 (1 - U)}{L I_L} - \frac{r_L}{L}.
\quad(9)
$$

Effect of the RHP zero becomes more pronounced when it moves towards the origin. As can be seen by (9), duty ratio, output voltage, inductor value and average value of the inductor current are some of the important parameters which determine the location of the RHP zero.

## 3 CONTROLLER DESIGN

Figure 2 shows a general 2-DOF feedback control structure. $G_c(s)$ denotes the transfer function of controller. Change in reference voltage is denoted by $\dot{v}_{in}(s)$ while $\dot{v}_0(s)$ represents the deviation in output voltage.

Let the transfer function of plant (i.e., boost converter) be

$$
G_p(s) = \frac{\dot{v}_0(s)}{\dot{u}(s)} = \frac{N_p(s)}{D_p(s)} = \frac{-a_1 s + a_0}{s^2 + b_1 s + b_0},
\quad(10)
$$

where,

$$
a_1 = \frac{I_L}{C}, a_0 = \frac{(1 - U) V_0 - r_L I_L}{L C} \quad b_1 = \frac{r_L}{L C}, b_0 = \frac{r_L}{R L C} + \frac{(1 - U)^2}{L C}.
$$

Parameters of the DC–DC boost converter considered in the present work are given in Table 1. Substituting these values in (6), (7) and (8), we get

$$
G_p(s) = \frac{-1670 s + 5.93 \times 10^7}{s^2 + 420 s + 7.28 \times 10^5},
\quad(11)
$$

$$
G_{d1}(s) = \frac{1.2 \times 10^6}{s^2 + 420 s + 7.28 \times 10^5},
\quad(12)
$$

$$
G_{d2}(s) = \frac{-1000 s - 4 \times 10^5}{s^2 + 420 s + 7.28 \times 10^5}.
\quad(13)
$$

Transfer function of the PID controller is assumed as follows:

$$
G_c(s) = \frac{N_c(s)}{D_c(s)} = k_p + \frac{k_i}{s} + k_d s,
\quad(14)
$$

where $k_p$, $k_i$ and $k_d$ are the proportional, integral and derivative gains, respectively.
From Figure 2, the closed-loop transfer function is obtained as

\[ T(s) = \frac{\tilde{y}_0(s)}{\tilde{p}_{1,ref}(s)} = \frac{G_p(s)G_c(s)}{1 + G_p(s)G_c(s)} = \frac{N_p(s)(k_d^2s^2 + k_p^2s + k_i)}{sD_p(s) + N_p(s)(k_d^2s^2 + k_p^2s + k_i)}. \tag{15} \]

From (15), it is observed that zeros of controller appear in the numerator of \( T(s) \). Presence of these zeros deteriorates the closed-loop performance. A pre-filter with the following transfer function from set-point to output is obtained as

\[ G_f(s) = \frac{N_f}{(k_d^2s^2 + k_p^2s + k_i)}. \tag{16} \]

Transfer function from set-point to output is obtained as

\[ T_c(s) = \frac{\tilde{y}_0(s)}{\tilde{p}_{1,ref}(s)} = \frac{N_fN_p(s)}{sD_p(s) + N_p(s)(k_d^2s^2 + k_p^2s + k_i)}. \tag{17} \]

\( N_f = k_c \) ensures zero steady-state error for a step change in reference voltage. The characteristic equation is given by

\[ \delta P(s) = 1 + G_p(s)G_c(s) = D_p(s)D_c(s) + N_p(s)N_c(s) = 0. \tag{18} \]

Substituting the values of \( N_p(s), D_p(s), N_c(s) \) and \( D_c(s) \) in (18), we get

\[ \delta P(s) = (1 - a_1 k_d)s^3 + (b_1 - a_1 k_p + a_0 k_d)s^2 + \ldots \]

\[ (b_0 - a_1 k_0 + a_0 k_p)s + a_0 k_i = 0. \tag{19} \]

Substituting \( s = j\omega \) in (19), we get

\[ \delta P(j\omega) = Re(\delta P) + jIm(\delta P) = 0. \tag{20} \]

Where \( Re(\delta P) \) and \( Im(\delta P) \) denote the real and imaginary parts of \( \delta P(j\omega) \) and are obtained as

\[ Re(\delta P) = U_1 k_p + V_1 k_i + W_1 k_d + X_1, \tag{21} \]

\[ Im(\delta P) = U_2 k_p + V_2 k_i + W_2 k_d + X_2, \tag{22} \]

where,

\[ U_1 = a_1 \omega^2; \quad V_1 = a_i; \quad W_1 = -a_i \omega^2; \quad X_1 = -b_1 \omega^2; \]

\[ U_2 = a_i; \quad V_2 = -a_i; \quad W_2 = a_1 \omega^2; \quad X_2 = b_0 - \omega^2. \tag{23} \]

Roots of any stable polynomial can become unstable by crossing the imaginary axis. So the imaginary axis is mapped on the controller parameters plane to obtain stable and unstable regions. Boundaries of the two regions (stable and unstable) are the root crossing boundaries, which can be finite (Real Root Boundary, Complex Root Boundary) and infinite (Infinite Root Boundary). All stability region in controller parameters plane is the area bounded by the above-said boundaries which contains all values of the controller parameters to ensure stability. Procedure to obtain the root crossing boundaries is as follows:

(i) Real Root Boundary (RRB): A real root can cross the imaginary axis at \( s = 0 \). RRB line is obtained as \( k_i = 0 \) by substituting \( s = 0 \) in (19).

(ii) Infinite Root Boundary (IRB): A real root can cross the imaginary axis at \( s = \infty \). IRB line is obtained as \( k_d = \frac{1}{a_1} \) by substituting \( s = \infty \) in (19). Substituting the value of \( a_1 \) gives \( k_d = 5.988 \times 10^{-4} \) as the IRB line.

(iii) Complex Root Boundary (CRB): Complex roots on the imaginary axis can become unstable which implies that both real and imaginary parts of \( \delta P(j\omega) \) will become zero simultaneously.

By equating \( Re(\delta P) \) and \( Im(\delta P) \) to zero, two equations with three unknowns are obtained. Assuming a suitable value of one of the controller parameter, the root crossing boundaries are drawn in the plane of other two parameters. Pre-specification of one of the controller parameters needs the stable range of the same. Intersection of RRB line, IRB line and CRB curve in the \( (k_p, k_i) \)-plane and \( (k_p, k_d) \)-plane provides the stable ranges of controller parameters [28]. Furthermore, the procedure to calculate the stable ranges of controller parameters is given in Sections 3.1 and 3.2.

### 3.1 All stability region in \( (k_p, k_i) \)-plane for a fixed value of \( k_d \)

By substituting \( s = 0 \) in (19), \( k_i = 0 \) is obtained as the RRB line. On the other hand, substituting \( s = \infty \) in (19) gives no solution for \( k_p \) and \( k_i \) for any value of \( k_d \) and therefore IRB line does not exist in \( (k_p, k_i) \)-plane. Expressions for CRB curve are obtained by equating (21) and (22) to zero and solving for \( k_p \) and \( k_i \) yields

\[ k_p = \frac{(a_0 + a_1 b_1)\omega^2 - a_1 b_0}{(a_0^2 + a_1^2 \omega^2)}, \tag{24} \]

\[ k_i = \frac{(a_0^2 \omega^2 + a_1^2) \omega^2 k_d + (a_1 \omega^2 - a_0 b_0 - a_1 b_1) \omega^2}{(a_0^2 + a_1^2 \omega^2)^2}. \tag{25} \]

(24) and (25) are plotted to obtain CRB curve by varying \( \omega \) from 0 to \( \omega_c \), where \( \omega_c \) is known as critical frequency. Furthermore, \( \omega_c \) is the lowest value of frequency other than \( \omega = 0 \) at which \( k_i = 0 \), the value of \( k_i \) on the RRB line. \( \omega_c \) is obtained by
equating (25) to zero and is given below.

\[
\omega_i = \sqrt{\frac{a_1 b_1 + a_0 b_1 + a_0^2 k_d}{a_1 - a_0^2 k_d}}. \tag{26}
\]

Using the above-discussed procedure, all stability region in \((k_p, k_i)\)-plane for \(k_d = 5.988 \times 10^{-4}\) is obtained as shown in Figure 3a.

### 3.2 All stability region in \((k_p, k_d)\)-plane for a fixed value of \(k_i\)

By substituting \(s = 0\) and \(k_i = 0\) in (19), \(k_p = \frac{b_0}{a_0}\) is obtained as the RRB line. \(k_d = \frac{1}{a_1}\) is obtained as the IRB line by substituting \(s = \infty\) in (19). Expressions for CRB curve are obtained as follows:

\[
k_p = \frac{(a_1 + a_0 b_1) \omega^2 - a_0 b_1}{(a_0^2 + a_0^2 \omega^2)}, \tag{27}
\]

\[
k_d = \frac{(a_0^2 \omega^2 + a_0^2) k_j - (a_1 b_1 + a_0 b_1) \omega^2 + a_1 \omega^4}{a_0^2 (a_0^2 + a_0^2 \omega^2)}, \tag{28}
\]

CRB curve in \((k_p, k_d)\)-plane is obtained by plotting (27) and (28) by varying \(\omega\) from 0 to \(\omega_i\). Where, \(\omega_i\) is the lowest value of frequency at which \(k_d = \frac{1}{a_1}\), the value of \(k_d\) on the IRB line. \(\omega_i\) is obtained by equating (28) to \(\frac{1}{a_1}\). On similar lines as discussed in the previous subsection, all stability region in \((k_p, k_d)\)-plane for \(k_i = 0\) is obtained as shown in Figure 3b.

From Figure 3a,b, stable ranges of controller parameters are obtained by intersection of RRB line, IRB line and CRB curve as \(-0.0123 \leq k_p \leq 21.514, 0 \leq k_i \leq 7.6135 \times 10^3\) and \(-7.428 \times 10^{-5} \leq k_d \leq 5.988 \times 10^{-4}\). In this paper, value of \(k_d\) is pre-specified and the root crossing boundaries are drawn in \((k_p, k_i)\)-plane. A suitable value of \(k_j\) is chosen from stable range to have a trade-off between transient performance and noise.

### 3.3 Desired gain and phase margin region

The DGPMP is obtained by placing a GPMT \((G_{pmp} = B e^{-\lambda t})\) in feed-forward path of the closed-loop shown in Figure 2. \(B\) and \(\lambda\) denote the values of gain and phase margins for constant GM and PM boundaries, respectively. Steps to compute different root crossing boundaries in Section 3.1 is repeated with GPMT in the loop. RRB line remains same, that is, \(k_i = 0\). There will not be any IRB line in the \((k_p, k_i)\)-plane for any value of \(k_d\). Corresponding \(k_j\) and \(k_i\) expressions for the CRB curve are given below:

\[
k_p = \left( (a_1 b_1 \omega^2 + a_0 b_1 \omega^2 - a_0 b_1) \cos \lambda + (a_1 b_1 - a_1 \omega^2 B + \cdots \right.
\]

\[
\left. \cdots + a_1 b_1 \omega \sin \lambda \right) / \left( B(a_0^2 + a_0^2 \omega^2) \right), \tag{29}
\]

\[
k_i = \left( (a_0^2 \omega^2 + a_0^2 \omega^2 \omega^2 B - (a_0 \omega^2 + a_1 b_1 \omega^2 - a_0 b_1) \omega \sin \lambda - \cdots \right.
\]

\[
\left. \cdots + a_1 \omega^2 - a_1 b_1 - a_1 b_1) \omega^2 \sin \lambda \right) / \left( B(a_0^2 + a_0^2 \omega^2) \right). \tag{30}
\]

CRB curve for Constant GM boundary is computed by substituting the desired value of GM and \(\lambda = 0\) in (29) and (30), whereas we put \(B = 1\) and the desired value of PM in (29) and (30) to obtain CRB curve for constant PM boundary. \(\omega_i\) is obtained by equating (30) to zero for desired GM and PM values. Common area of the above-said boundaries inside the all stability region is called the DGPMP. Controller parameters in the DGPMP yield stability margins greater than or equal to the pre-specified values.

A triangular convex region of the DGPMP is obtained by identifying peak point on the CRB curve and two corner points on the RRB line of DGPMP. Coordinates of the peak point is assumed as \((k_{pmp}, k_{j_{mp}})\) and that of corner points are \((k_{p1}, k_{j1})\) and \((k_{p2}, k_{j2})\). Values of \(k_p\) and \(k_i\) are obtained by finding the centroid of the triangular convex region of the DGPMP as follows:

\[
k_p = \frac{(k_{p1} + k_{p2} + k_{j2})}{3}, \tag{31}
\]

\[
k_i = \frac{(k_{p1} + k_{p2} + k_{j2})}{3}. \tag{32}
\]
3.4 | Selection of $k_d$ based on noise constraint

A new approach for selecting the value of $k_d$ to limit the noise level in the control signal to a pre-specified value is presented in this section. Noise in the control signal degrades the performance and shortens the actuator life of a closed-loop system [29]. Power converters are prone to noise due to the presence of multiple noise sources. Standard deviation, which is one of the most commonly used measures of noise level, is calculated as

$$\sigma_u = \sqrt{\frac{1}{k-1} \sum_{j=1}^{k} (u_j - u_{av})^2}, \quad (33)$$

where $k$ is the number of samples of the control signal in steady-state. $u_{av}$ is the average value of $k$ samples of the control signal. In the present work, 20,000 samples of the control signal in steady-state are considered to increase the accuracy level.

An arbitrary value of $k_d$ (say $1 \times 10^{-5}$) is chosen from the stable range. Figure 4a shows the all stability region in $(k_p, k_i)$-plane for $k_d = 1 \times 10^{-5}$, which is obtained using the procedure given in Section 3.1. It is mentioned in [30] that robust stability is ensured by simultaneous satisfaction of $GM > 6$ dB and $PM > 30$ deg. Constant $GM$ (9 dB) and $PM$ (60 deg) boundaries for $k_d = 1 \times 10^{-5}$ are obtained using the procedure given in Section 3.3 and shown in Figure 4b,c respectively. Figure 4d shows the all stability region, Constant $GM$ (9 dB) and $PM$ (60 deg) boundaries. The shaded region in Figure 4d is the DGPMR. Centroid of the triangular convex region of the DGPMR is obtained as $(0.0068, 3.254)$.

A band-limited white noise of standard deviation 0.1 with sampling period equal to $5 \times 10^{-7}$ is considered here. Closed-loop simulation for a unit step reference voltage change is performed by using the above controller parameters with and without considered white noise present in the loop to obtain $\sigma_u$ and integral of absolute error ($IAE = \int_0^\infty |e(t)| dt$), respectively. Instantaneous error, $e(t)$ is the difference between reference voltage change, $\tilde{v}_{ref}(t)$ and output voltage change, $\tilde{v}(t)$ at time $t'$. Values of $\sigma_u$ and $IAE$ are obtained as 0.0076 and $5.87 \times 10^{-3}$, respectively. Above-discussed procedure is repeated for several values of $k_d$ to obtain values of $\sigma_u$ and $IAE$. Curve fitting toolbox of MATLAB is then used to obtain a graphical relationship between $\sigma_u$ and $IAE$ as shown in Figure 5 and a mathematical relationship between $k_d$ and $\sigma_u$ as follows:

$$k_d = a \times (\sigma_u)^b + c, \quad (34)$$

where $a = 0.0005002$, $b = 0.8232$ and $c = 2.153e - 06$. It is observed from Figure 5 that improved transient response (i.e. lower $IAE$ value) is obtained at the cost of higher value of $\sigma_u$ (i.e. increased level of noise content in the control signal) and vice versa. Using (34), value of $k_d$ is selected for a specified $\sigma_u$. 

![Figure 4](https://example.com/figure4.png)
4 SIMULATION AND HARDWARE EXPERIMENTAL RESULTS

Following commonly used parallel form of PID controller is considered for simulations and hardware experiments.

\[ G_c(s) = k_p + \frac{k_i}{s} + \frac{k_d s}{0.1(k_d/k_p)^3 + 1}. \]  

(35)

In the present work, \( \sigma_u = 0.03 \) from Figure 5 is considered for controller design which yields \( IAE = 2.66 \times 10^{-3} \). Using (34), corresponding value of \( k_d \) is calculated as \( 3.005 \times 10^{-3} \). All stability region, constant GM (9 dB) and PM (60 deg) boundaries for \( k_d = 3.005 \times 10^{-3} \) in \( (k_p, k_i) \)-plane are obtained as shown in Figure 6. The DGPMR is shown by the shaded region. Centroid point is calculated as \( (k_p = 0.0256, k_i = 13.82) \), which is the required controller setting for \( k_d = 3.005 \times 10^{-3} \). Proposed method is compared with that of Kobaku et al. [9]. In [9], authors have proposed a two degree-of-freedom internal model controller for boost converter. Two filters namely set-point filter \( (F_r(s)) \) and disturbance filter \( (F_d(s)) \) were designed. Tuning parameter, \( \lambda_r \) for \( F_r(s) \) was calculated to have a desired set-point tracking performance, whereas \( \lambda_d \) for \( F_d(s) \) was computed to achieve a desired degree of robustness based on maximum value of sensitivity function \( (M_s) \). \( M_s \) is defined as inverse of the shortest distance from the Nyquist curve of open-loop transfer function to the critical point \((-1, j0)\) and is expressed as follows:

\[ M_s = \max_{\omega} \left| \frac{1}{1 + G_p(j\omega)G_c(j\omega)} \right|. \]  

(36)

Value of \( M_s \) less than 2 ensures robust stability [30]. The proposed method yields \( M_s = 1.246 \). For a fair comparison, the tuning parameters of the two filters in [9] are selected as \( \lambda_r = 1.14 \text{ms} \) and \( \lambda_d = 0.61 \text{ms} \) to achieve the same values of settling time in set-point tracking response and \( M_s \) as obtained by the proposed method.

Different performance measures like settling time \( (\tau_s) \), overshoot \( (O.S.) \) / undershoot \( (U.S.) \) and \( IAE \) are used for comparison. As reported in [9], \( \tau_s \) is considered as the time required to reach and stay within \( \pm 1\% \) band of the steady-state value. Matlab simulations are performed on the linear as well as non-linear model of the boost converter. The switching frequency is considered as 20 kHz.

Figure 7 shows the hardware set-up for experimental evaluation. Control schemes are implemented using a dSPACE 1104 microcontroller. Programmable DC power supply is used to provide variable input voltage to the boost converter, whereas DC programmable load is connected in parallel with the nominal load to provide a step change in connected load. Three different cases are considered to demonstrate the effectiveness of the proposed method.

4.1 Case 1: Servo performance

Servo performance is evaluated by applying step changes in reference voltage. First, a step-up change in reference voltage from 50 to 60V at \( t = 0.1 \text{s} \) is considered. Input voltage and load resistance are kept constant at their nominal values of 30V and 50Ω, respectively. Figure 8 shows the simulation results of output voltage, control effort (duty ratio) and inductor current. Values of performance measures are given in Table 2. It is observed from Figure 8 and Table 2 that the two methods yield same settling time \( (\tau_s) \) as considered in the design. Hardware experimental results are shown in Figure 14. Furthermore, the benefit of the proposed control scheme is illustrated by applying a step-down change in reference voltage from 60 to 50V at \( t = 0.15 \text{s} \). Corresponding simulation and hardware...
TABLE 2  Performance measures

|                  | Kobaku et al. [9] |                  | Proposed |
|------------------|-------------------|------------------|----------|
|                  | $T_c$ (ms) | O.S./U.S. (%) | $\text{IAE} \times 10^{-3}$ | $T_c$ (ms) | O.S./U.S. (%) | $\text{IAE} \times 10^{-3}$ |
| SIMULATION (LINEAR) |              |                 |                 |       |         |               |
| Case-1 ($v_{ref}(t)$: 50 V to 60 V) | 5.2 | 0 | 23.1 | 5.2 | 0 | 27.43 |
| Case-1 ($v_{ref}(t)$: 60 V to 50 V) | 6.98 | 1.56 | 21.87 | 4.45 | 0.55 | 26.04 |
| Case-2 ($v_{in}(t)$: 30 V to 45 V) | 19.8 | 5.57 | 41.79 | 18.1 | 2.93 | 21.97 |
| Case-2 ($v_{in}(t)$: 45 V to 30 V) | 21.4 | 5.47 | 41.52 | 18.4 | 2.91 | 21.82 |
| Case-3 ($R$: 50 W to 125 W) | 2 | 1.62 | 1.737 | 1.2 | 1.174 | 1.055 |
| Case-3 ($R$: 125 W to 50 W) | 2.03 | 1.72 | 1.84 | 1.244 | 1.27 | 1.12 |
| SIMULATION (NON-LINEAR) |              |                 |                 |       |         |               |
| Case-1 ($v_{ref}(t)$: 50 V to 60 V) | 4.6 | 0.6 | 22.78 | 4.6 | 0 | 26.07 |
| Case-1 ($v_{ref}(t)$: 60 V to 50 V) | 22.3 | 9.6 | 83.99 | 20.5 | 9.5 | 79.82 |
| Case-2 ($v_{in}(t)$: 30 V to 45 V) | 21 | 5.25 | 41.42 | 18.3 | 2.82 | 21.66 |
| Case-2 ($v_{in}(t)$: 45 V to 30 V) | 19.95 | 5.88 | 41.52 | 18.05 | 3.03 | 21.71 |
| Case-3 ($R$: 50 W to 125 W) | 2.1 | 1.8 | 2.76 | 1.2 | 1.35 | 1.83 |
| Case-3 ($R$: 125 W to 50 W) | 1.8 | 1.63 | 1.86 | 1 | 1.2 | 1.29 |
| HARDWARE EXPERIMENTS |              |                 |                 |       |         |               |
| Case-1 ($v_{ref}(t)$: 50 V to 60 V) | 9.2 | 2.22 | 27.7 | 7.4 | 1.56 | 24.4 |
| Case-1 ($v_{ref}(t)$: 60 V to 50 V) | 21.5 | 10.2 | 85.6 | 19.3 | 10.2 | 77.9 |
| Case-2 ($v_{in}(t)$: 30 V to 45 V) | 18.3 | 5.38 | 36.4 | 16.3 | 2.85 | 18.5 |
| Case-2 ($v_{in}(t)$: 45 V to 30 V) | 18.6 | 5.3 | 36.1 | 17.2 | 2.99 | 19.8 |
| Case-3 ($R$: 50 W to 125 W) | 3.3 | 2.74 | 4.2 | 2.2 | 2.1 | 2.5 |
| Case-3 ($R$: 125 W to 50 W) | 3.5 | 2.64 | 4.5 | 2.2 | 1.9 | 2.4 |

FIGURE 8  Simulation results for a step change in reference voltage from 50 to 60 V (Case 1: Tracking performance). (a) Output voltage. (b) Control effort. (c) Inductor current

FIGURE 9  Simulation results for a step change in reference voltage from 60 V to 50 V (Case 1: Tracking performance). (a) Output voltage. (b) Control effort. (c) Inductor current

Experimental results are given in Figures 9 and 15, respectively. Obtained values of performance measures are given in Table 2. For the step-up case, controllers of the two schemes first increase the inductor current to a high value (approximately 9 A) in transient phase to quickly ramp up the output voltage and then decrease until it achieves a level that corresponds to steady-state power balance when the converter attains the reference voltage. Moreover, for the step-down case, controllers try to decrease the inductor current in transient phase to a low value (in the negative direction), but inductor current cannot
**FIGURE 10** Simulation results for input voltage variation from 30 V to 45 V (Case 2: Regulatory response). (a) Input voltage. (b) Output voltage. (c) Control effort. (d) Inductor current.

**FIGURE 11** Simulation results for input voltage variation from 45 to 30 V (Case 2: Regulatory response). (a) Input voltage. (b) Output voltage. (c) Control effort. (d) Inductor current.

**FIGURE 12** Simulation results for a step change in connected load from 50 to 125 W (Case 3: Regulatory response). (a) Load current. (b) Output voltage. (c) Control effort. (d) Inductor current.

**FIGURE 13** Simulation results for a step change in connected load from 125 to 50 W (Case 3: Regulatory response). (a) Load current. (b) Output voltage. (c) Control effort. (d) Inductor current.
go below 0 A due to unidirectional capability of the boost converter. Consequently, the converter temporarily enters and stays in discontinuous conduction mode (DCM) until average value of inductor current is greater than half of the peak-to-peak ripple in inductor current. However, since the two control schemes are designed with sufficient robustness, they ensure closed-loop stability and output voltage regulation in non-linear simulation as well as hardware experiments. Furthermore, the proposed control scheme outperforms the method of Kobaku et.al. [9] in non-linear simulation and hardware experimental results for the step-down case as can be seen by Figures 9 and 15 and Table 2.

4.2 | Case 2: Regulatory performance for input voltage disturbance

Input voltage is changed from 30 to 45V at $t = 0.3s$ and 45 to 30V at $t = 0.35s$ while the load resistance is kept constant at 50Ω. Corresponding simulation results of input voltage, output voltage, control effort and inductor current are shown in Figures 10 and 11, respectively. Performance measures are given in Table 2. Figures 10 and 11 and Table 2 show that the proposed method yields improved regulatory performance for disturbance in input voltage with lower values of settling time, overshoot and IAE as compared to the method of Kobaku et al. [9]. Corresponding hardware experimental results in Figures 16 and 17 closely agree with the simulation results.

4.3 | Case 3: Regulatory performance for load current disturbance

Regulatory performance for disturbance in load current is considered for a step change in load from 50 to 125W (i.e. 50 to 20Ω) at $t = 0.5s$ and 125 to 50W (i.e. 20 to 50Ω) at $t = 0.55s$. 

FIGURE 14 Hardware experimental results for a step change in reference voltage from 50 to 60V (Case 1: Tracking performance). (a) Output voltage. (b) Control effort. (c) Inductor current

FIGURE 15 Hardware experimental results for a step change in reference voltage from 60V to 50V (Case 1: Tracking performance). (a) Output voltage. (b) Control effort. (c) Inductor current

FIGURE 16 Hardware experimental results for input voltage variation from 30 to 45V (Case 2: Regulatory response). (a) Input voltage. (b) Output voltage. (c) Control effort. (d) Inductor current
Input voltage is kept constant at 30 V. Corresponding simulation results of load current, output voltage, control effort and inductor current are shown in Figures 12 and 13, respectively. Proposed method yields improved regulatory performance than the method of Kobaku et al. [9] as evident from Figures 12 and 13 and Table 2. Figures 18 and 19 show the corresponding hardware experimental results.

From Figures 8 and 19 and Table 2, it is observed that hardware experimental results are qualitatively matching with corresponding simulation results in all the above three cases.

### 4.4 Simulation results for the perturbed model

To illustrate the robustness of the proposed controller against perturbation in plant parameters, values of $L$ and $C$ are increased by 20%. MATLAB simulations are performed on the linear and non-linear perturbed models. Corresponding results for the above-said three cases are shown in Figure 20. It is observed from the obtained results that the proposed controller is robust to the assumed perturbations in $L$ and $C$. Furthermore, the proposed method also outperforms the strategy reported in [9] in the perturbed scenario.

From the above simulation and hardware experimental results, it can be observed that the proposed method yields improved closed-loop performance compared to the strategy.
voltage control of a DC–DC boost converter is presented in this paper. A linearised model in the neighbourhood of the equilibrium point is used to design the controller. Frequency–domain performance measures such as gain and phase margins can be pre-specified to achieve a desired degree of robustness. Furthermore, $k_d$ is selected to have a trade-off between closed-loop transient performance and noise level in the control signal. Simplicity of the technique is an added advantage for the practising engineers in industries. The presented technique has an extra benefit over mathematical-based tuning methods as the controller parameters are obtained graphically whereas later needs tedious calculations. Simulation and hardware results show that the proposed method yields satisfactory closed-loop responses. Robustness of the proposed controller is illustrated by simulation and hardware results. Closed-loop responses of simulation as well as hardware experiments are found to be superior as compared to a recently reported tuning strategy for the boost converter in nominal as well as perturbed scenarios.

REFERENCES

1. Ahmad, S., Ali, A.: Active disturbance rejection control of DC–DC boost converter: A review with modifications for improved performance. IET Power Electron. 12(8), 2095–2107 (2019)
2. Forouzesh, M., et al.: Step-up DC–DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications. IEEE Trans. Power Electron. 32(12), 9143–9178 (2017)
3. Yazici, İ., Yaylaci, E.K.: Fast and robust voltage control of DC–DC boost converter by using fast terminal sliding mode controller. IET Power Electron. 9(1), 120–125 (2016)
4. Naim, R., Weiss, G., Ben-Yaakov, S.: $H_\infty$ control applied to boost power converters. IEEE Trans. Power Electron. 12(4), 677–683 (1997)
5. Tan, S.C., Lai, Y.M., Chi, K.T.: General design issues of sliding-mode controllers in DC–DC converters. IEEE Trans. Ind Electron. 55(3), 1160–1174 (2008)
6. Ollota, C., et al.: Robust LQR control for PWM converters: An LMI approach. IEEE Trans. Ind. Electron. 56(7), 2548–2558 (2009)
7. Karamanakos, P., Geyer, T., Manias, S.: Direct voltage control of DC–DC boost converters using enumeration-based model predictive control. IEEE Trans. Power Electron. 29(2), 968–978 (2014)
8. Wang, Y.X., Yu, D.H., Kim, Y.B.: Robust time-delay control for the DC–DC boost converter. IEEE Trans. Ind. Electron. 61(9), 4829–4837 (2014)
9. Kobaku, T., Patwardhan, S.C., Agarwal, V.: Experimental evaluation of internal model control scheme on a DC–DC boost converter exhibiting nonminimum phase behavior. IEEE Trans. Power Electron. 32(11), 8880–8891 (2017)
10. Sundareswaran, K., Sreedevi, V.: Boost converter controller design using queen-bee-assisted GA. IEEE Trans. Ind. Electron. 56(3), 778–783 (2009)
11. Sundareswaran, K., Sreedevi, V.: Design and development of feed-back controller for a boost converter using a colony of foraging bees. Electr. Pow. Compo. Syst. 37(5), 465–477 (2009b)
12. Sundareswaran, K., Devi, V.: Application of a modified particle swarm optimization technique for output voltage regulation of boost converter. Electr. Pow. Compo. Syst. 39(3), 288–300 (2011)
13. Sundareswaran, K., et al.: Feedback controller design for a boost converter through evolutionary algorithms. IET Power Electron. 7(4), 903–913 (2014)
14. Alvarez-Ramirez, J., et al.: A stable design of PI control for DC–DC converters with an RHS zero. IEEE Trans. Circuits Syst. I: Fundam. Theory. Appl. 48(1), 103–106 (2001)
15. Arulselvi, S., Uma, G., Chidambram, M.: Design of PID controller for boost converter with RHS zero. In: The 4th International Power Electronics and Motion Control Conference, vol. 2, IEEE, pp. 532–537 (2004),

5 Conclusion

A novel graphical-based controller design method for output voltage control of a DC–DC boost converter is presented in
16. Balestrino, A., et al.: Circle-based criteria for performance evaluation of controlled dc–dc switching converters. IEEE Trans. Ind. Electron. 53(6), 1862–1869 (2006)
17. Kapat, S., Krein, P.T.: Formulation of PID control for DC–DC converters based on capacitor current: A geometric context. IEEE Trans. Power Electron. 27(3), 1424–1432 (2012)
18. Almodaresi, E., Bozorg, M.: $kp$-stable regions in the space of PID controller coefficients. IET Control Theory Appl. 11(10), 1642–1647 (2017)
19. Srivastava, S., Pandit, V.: A PI/PID controller for time delay systems with desired closed loop time response and guaranteed gain and phase margins. J. Process Control 37, 70–77 (2016)
20. Saxena, S., Hote, Y.V.: Decentralized PID load frequency control for perturbed multi-area power systems. Int. J. Electrical Power Energy Syst. 81, 405–415 (2016)
21. Almodaresi, E., Bozorg, M., Taghirad, H.D.: Stability domains of the delay and PID coefficients for general time-delay systems. Int. J. Control 89(4), 783–792 (2016)
22. Ghooi, M., Jain, S., Hote, Y.V.: Proportional integral derivative controller tuning via Kronecker summation and modified particle swarm optimization with experimental validation. Eng. Optim. 53(2), Taylor & Francis, 237–257 (2021)
23. Jin, Q., Liu, Q., Huang, B.: New results on the robust stability of PID controllers with gain and phase margins for UFOPTD processes. ISA Trans. 61, 240–250 (2016)
24. Han, S., Bhattacharyya, S.P.: PID controller synthesis using a $\sigma$-Hurwitz stability criterion. IEEE Control Syst. Letters 2(3), 525–530 (2018)
25. Rahimian, M.A., Tarazoei, M.S.: Application of stability region centroids in robust PI stabilization of a class of second-order systems. Trans. Inst. Meas. Control 34(4), 487–498 (2012)
26. Ozyetkin, M.M., Onat, C., Tan, N.: PI-PD controller design for time delay systems via the weighted geometrical center method. Asian J. Control 22(5), 1811–1826 (2020)
27. Onat, C.: A new design method for PI-PD control of unstable processes with dead time. ISA Trans. 84, 69–81 (2019)
28. Luo, Y., Chen, Y.: Stabilizing and robust fractional order PI controller synthesis for first order plus time delay systems. Automatica 48(9), 2159–2167 (2012)
29. Sun, B., Gao, Z.: A DSP-based active disturbance rejection control design for a 1-kw h-bridge DC-DC power converter. IEEE Trans. Ind. Electron. 52(5), 1271–1277 (2005)
30. Dey, J., Mondal, R., Halder, S.: Generalized phase compensator of continuous time plants. ISA Trans. 81, 141–154 (2018)

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