Enabling Super-Fast Deep Learning on Tiny Energy-Harvesting IoT Devices

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Abstract—Energy harvesting (EH) IoT devices that operate intermittently without batteries, coupled with advances in deep neural networks (DNNs), have opened up new opportunities for enabling sustainable smart applications. Nevertheless, implementing those computation and memory-intensive intelligent algorithms on EH devices is extremely difficult due to the challenges of limited resources and intermittent power supply that causes frequent failures. To address those challenges, this paper proposes a methodology that enables super-fast deep learning with low-energy accelerators for tiny energy harvesting devices. We first propose RAD, a resource-aware structured DNN training framework, which employs block circulant matrix with ADMM to achieve high compression and model quantization for leveraging the advantage of various vector operation accelerators. A DNN implementation method, ACE, is then proposed that employs low-energy accelerators to profit maximum performance with minor energy consumption. Finally, we further design FLEX, the system support for intermittent computation in energy harvesting situations. Experimental results from three different DNN models demonstrate that RAD, ACE, and FLEX can enable super-fast and correct inference on energy harvesting devices with up to 4.26X runtime reduction, up to 7.7X energy reduction with higher accuracy over the state-of-the-art.

Index Terms—Deep Learning, Low-energy Accelerator, Energy Harvesting, IoT

I. INTRODUCTION

In this IoT era where all things trends towards to be embedded with electronics, DNN brings new opportunities for embedded IoT devices to be smarter, more versatile, and able to handle more complex jobs. Such exciting opportunities enable processing function to be placed on embedded IoT devices instead of solely depending on the cloud by uploading all collected data to the cloud server and waiting for results to be processed and downloaded. Such a procedure not only significantly reduces processing pressure on the cloud but also improves energy efficiency as well as IoT service response time.

Resource-constrained embedded IoT devices face three major challenges from computation, memory, and energy perspectives for implementing DNNs. First, embedded IoT devices have significantly less computational units and lower CPU frequency (1-16MHz). Since DNNs are computationally expensive, implementing DNNs on embedded IoT devices results in significantly longer execution time. Second, embedded IoT devices are equipped with much smaller (1-16Kb) memory due to the size constraint. Third, majority IoT devices are powered with batteries, which can be depleted in days or even hours, requiring high maintenance cost which is especially undesirable if devices are implanted or deployed in harsh environment.

Energy harvesting (EH), which can scavenge energy from ambient environment, has become a promising technology to provide energy supply for IoT devices. However, the power supply can be intermittent and low. Since DNN execution is time and energy consuming, the power outage is prone to happen frequently in the middle of the execution. As a result, implementing DNN in energy harvesting devices is a highly challenging job because the implementation requires consideration of both the resource constraints and the intermittent power supply which complicates the development of such systems. Recent work proposed software system SONIC and TAILS [6] to enable fast deep learning inference on battery-less systems. Those systems exploits the special structured and loop-heavy computations of DNN and enable their intermittent executions by continuously saving the loop control states to the non-volatile memory after each instruction. However, correctness of intermittent execution requires special mechanism to handle the inconsistency issues.

To our knowledge, none of existing work has considered the various vector operations supported by the low-energy accelerators in the training process and thus fail to efficiently leverage those accelerators in implementation and cause severe progress setback with existing software support for intermittent execution. To generate a best framework for the DNN implementation, we need to design the DNN model based on the resource constraints and employ the compression methods that can take advantage of those hardware accelerators while considering their limitations and the constraints of device. Besides, to avoid the progress setback while guaranteeing correctness, we need special support for those vector operations executed on accelerators. To this end, this paper proposes the first framework that enables super-fast deep learning leveraging low-energy accelerators on resource-constrained EH IoT devices as follows with three contributions as follows:

- A resource-aware structured DNN training framework, RAD, consisting four different components: architecture search, compression, normalization, and fixed point calculation by addmm quantization.
- A software system, ACE, that implements DNN algorithm, consisting four different components: acceleration-aware dataflow design, hardware acceleration, overflow-aware computation and circular buffer convolution.
- A novel on-demand robust checkpointing scheme, FLEX, is proposed which can minimize or completely avoid progress setback even if a power outage happens.

The remainder of this paper is organized as follows: Section II provides the background and motivation; Section III provides the framework overview and the three contributions; Section IV presents the experimental evaluation; Section V discusses related work and Section VI concludes this work.
II. BACKGROUND AND MOTIVATION

Energy Harvesting Resource-Constrained Devices: Typical microcontrollers of IoT edge devices have minimal memory size and compute resources. Even a small DNN model like LeNet that has millions of operations takes several minutes to execute [6]. As a result, implementing DNN algorithms is more challenging. DNN algorithms need to be redesigned and optimized to fit those small devices with good accuracy and run time. Besides, the energy needs to be harvested to a certain threshold to begin computation. However, the energy drained fast, resulting in frequent power failures, which incurs a problem with two dimensions. First, resuming the computation without wasted work. Second, checkpointing must not consume much energy and time. As a result, there are also opportunities to re-think the traditional checkpointing mechanism.

Low Energy Accelerators: To efficiently deploy DNN algorithms on energy harvesting devices, we should take advantage of the computation resources of vector operation accelerators like TI’s low-energy accelerator (LEA) [12], which can perform vector operations such as FFT/IFFT, MAC, ADD, etc. It’s a low-power coprocessor that performs vector operations without any CPU intervention.

DNN Pruning: Compared with other pruning solutions of DNN algorithms, block-circulant matrix (BCM) based DNNs [5] and structured pruning [15] turn to be the most promising solution for energy harvesting resource-constrained devices.

a) Structured Pruning: Structured pruning is proposed to structurally remove entire filters, channels, or filter shapes from the weight matrix. Structured pruning becomes more hardware-friendly by taking advantage of the pruned weight matrices with regular shapes, avoiding introducing extra indices that indicate the pruned locations.

b) Block-circulant matrix: Block-circulant matrix (BCM) based DNN algorithm can drastically reduce memory footprint and computation pressure, consequently achieving low energy consumption. Since its implementation requires Fourier and inverse Fourier transformation, we can employ the FFT/IFFT accelerators for implementation.

The key idea of block-circulant matrix (BCM) based fully connected (FC) layers is to partition the original weight matrix $W \in \mathbb{R}^{m \times n}$ into blocks of square sub-matrices, and each sub-matrix is a circulant matrix. Specifically, the matrix-vector multiplication can be implemented via “FFT→element-wise multiplication→IFFT”, i.e., $\text{IFFT}(\text{FFT}(p_{ij}) \circ \text{FFT}(x_j))$ using the BCM format. For the inference phase, the computational complexity of this FC layer is $O(pqk \log k)$. Similarly, the storage complexity is $O(pqk)$ because only $w_{ij}$ or $\text{FFT}(w_{ij})$ of each sub-matrix needs to be stored, which is equivalent to $O(n)$ for small $p$, $q$ values. Therefore, the simultaneous acceleration and model compression can be achieved.

III. SUPER-FAST DEEP LEARNING ON ENERGY HARVESTING DEVICE

System overview: We propose a resource-aware training, pruning, and implementation framework that takes various types of vector operations supported by low-energy accelerators into consideration. Figure 1 shows the system overview of the proposed framework which consists of three techniques named RAD, ACE, and FLEX, as well as the responsibility of each technique, and their correlation. Resource-aware structured DNN training and pruning method, RAD, provides the resource-aware model with architecture search, compression, normalization, and fixed point calculation methods by ADMM quantization. ACE then implements DNN algorithm on EH device with efficient data flow design, circular buffer convolution, and hardware accelerators. A novel on-demand hybrid checkpointing method, FLEX, that also takes advantages of the special structure of DNN helps deal with the frequent power failures while avoiding progress setback.

A. Resource-aware DNN modeling (RAD)

RAD aim to design and train a DNN model that is aware of the deployed device resources. After achieving a model by manual architecture search that fits into the available memory footprint with good accuracy, RAD performs further compression with small accuracy loss while achieving less memory footprint and latency. RAD trains the model offline and deploy the trained model for inference into the device. Figure 1 shows the typical computing and memory resources in the IoT device. Both CPU and LEA are responsible for completing DNN operations, while SRAM and FRAM are used as data storage. The SRAM is smaller with lower dynamic read-write energy compared with FRAM. SRAM is used as a buffer for intermediate data where FRAM is used for storing the DNN model, OS, and the control data for intermittent computation, which will be discussed in Section III.C.

Modeling challenges: There are several challenges during DNN modeling. 1) SRAM/FRAM size 2) CPU frequency and inference time 3) Overflow error 4) Model accuracy. Aware of the above challenges, RAD trained the DNN model offline. The model must fit into the FRAM with acceptable inference time and accuracy. RAD’s architecture search technology finds a suitable model and further compresses it. As we deal with fixed-point calculation in a resource constraint device, there is possible data overflow during vector operation like MAC and FFT. As a result, RAD performs several normalization so that data stays between ranges during calculation.

Fixed point calculation: Traditionally DNN models are trained using high precision, which is generally not required during inference. In this work, we use low-precision fixed-point representation to avoid the costly floating-point computation and
reducing the memory footprint. RAD employs ADMM based quantization method so that ACE can deploy the DNN model with fixed-point calculation.

**Normalization:** For normalization, RAD first sets the data range \( G_i \) with a minimum value, \( G_{\text{min}} \), as -1 and a maximum value, \( G_{\text{max}} \), as 1. RAD then normalizes the data within this range of \([-1, 1]\]. Finally, to avoid the value of the computed intermediates exceed this range during inference, RAD uses the cosine normalization \([10]\) to constrain the values of the computed intermediates into \([-1, 1]\).

**Compression:** For the model compression, RAD implements FFT-based block circulant matrix (BCM) \([3]\) computation for fully connected (FC) layers and structured pruning for convolutional (COV) layers, which can achieve drastically reduced memory footprint with a negligible accuracy drop \([3]\). Table I shows that BCM can reduce more than 99% memory footprint for any fully connected layer. For the structured pruning, RAD used filter pruning and channel pruning on convolutional layers.

**TABLE I:** BCM compression for 512*512 fully connected layer Table: 

| Kernel Size | Block size | Compressed kernel | Storage reduction |
|-------------|------------|-------------------|------------------|
| 1048576 Byte | 16         | 65536 Byte        | 93.75%           |
|             | 32         | 32768 Byte        | 96.87%           |
|             | 64         | 16384 Byte        | 98.33%           |
|             | 128        | 8192 Byte         | 99.21%           |
|             | 256        | 4096 Byte         | 99.50%           |

**ADMM-Regularized Quantization:** We combine BCM compression and customized quantization on accelerators into the ADMM-regularized training process \([3]\), as it will not only mitigate the accuracy degradation of DNN-activator mapping imperfection, but also helps reduce the design area and power consumption to improve system performance since fewer bits (state levels) are needed.

Consider an \( N \)-layer DNN, where the weight and biases matrices in the \( i \)-th layer are \( W_i \) and \( b_i \). BCM compression and customized quantization can be merged with the loss function as an joint optimization problem as shown below.

\[
\begin{align*}
\text{minimize} & \quad F(\{W_i\}_{i=1}^N, \{b_i\}_{i=1}^N), \\
\text{subject to} & \quad W_i \in S_i, \quad W_i \in Q_i, \quad W_i \in R_i, \quad i = 1, \ldots, N.
\end{align*}
\]

(1)

BCM compression has constraint set \( S_i = \{\text{block circulant matrix with block size } \alpha_i\} \). Quantization has constraint set \( Q_i = \{\text{the consecutive weights on the same kernel have different sign and the weights in layer } i \text{ are mapped to the quantization values}\} \), where \( M \) is the number of quantization levels. The filter pruning and channel pruning has constraint set \( R_i = \{\text{remaining non-zeros filters or channels in convolutional layer}\} \) satisfying the requirement of filter pruning and channel pruning. Assume set of \( \{Q_{i,1}, Q_{i,2}, \ldots, Q_{i,M}\} \) is the available accelerator state value which is the elements in \( W_i \). Suppose \( q_{i,j} \) indicates the \( j \)-th quantization level in layer \( i \), which gives \( q_{i,j} \in [G_{\text{min}}, G_{\text{max}}], \) where \( G_{\text{min}}, G_{\text{max}} \) are the minimum and maximum conductance value of the selected energy harvesting device. Given the value of \( l_i \) (number of non-zero filters or channels in the weights of the \( i \)-th convolutional layer), the constraint, \( R_i \), becomes \( W_i \in R_i := \{W_i \mid \forall W_i : \text{card}(W_i) \leq l_i\} \), where \( \text{card}(W_i) \) returns the number of non-zero filters or channels in \( W_{\text{conv}} \).

We use indicator functions to incorporate the BCM compression, customized quantization and structured pruning constraints into the objective function, which are

\[
g_i(W_i) = \{h_i(W_i) \text{ or } t_i(W_i)\} = \begin{cases} 0 & \text{if } W_i \in S_i \text{ or } Q_i \text{ or } R_i, \\ +\infty & \text{otherwise} \end{cases}
\]

Then the original problem (1) can be equivalently rewritten as

\[
\text{minimize} \quad \sum_{i=1}^N g_i(W_i) + \sum_{i=1}^N h_i(W_i) + \sum_{i=1}^N t_i(W_i)
\]

(2)

With formation of augmented Lagrangian \([6]\), the problem (2) can be decomposed into three subproblems. The first subproblem deals with loss function of DNN and can be solved using stochastic gradient descent because of the differentiability. The second and third subproblems can be solved using Euclidean Projections onto the discrete subspace thanks to the characteristics in combinatorial constraints. The projection process is: generate block circulant matrices with block size of \( \alpha_i \), keep the consecutive weights on the same kernel to have different sign, make the number of non-zero weights in the CONV layer smaller than \( l_i \) and be mapped to the quantization values. The three subproblems are solved iteratively according to ADMM rule \([3]\) until convergence.

**B. Accelerator Enabled Embedded Software (ACE)**

To implement on-device DNN, we propose vector accelerator-powered embedded software, ACE. ACE deploys DNN algorithms efficiently and ensures full utilization of the device accelerators for operations like FFT, IFFT, MAC, etc. It also enables efficient data flow during DNN computation. ACE utilizes DMA for data transfer and achieves significant performance improvement over CPU-based data transfer. ACE restructures the DNN computation to fit with the device accelerator and ensures full utilization of the accelerator, which had not been implemented before. Recent work \([6]\), TAILS utilizes the accelerators to some extent, but the performance is not adequate because TAILS cannot unleash the maximum benefits of the accelerators.

**Acceleration-aware dataflow:** Figure 3 demonstrates the vector based dataflow. Before executing each layer, the input window and kernel are buffered in the SRAM first for invoking the accelerator (MAC, ADD, FFT/IFFT). The buffered vectors are then sent to the accelerator for computation. Next, the outputs from the accelerators, buffered in SRAM, stored to the FRAM. The subsequent Maxpooling layer and activation function (ReLU) is loaded directly into the CPU without SRAM buffering. ACE achieves significantly faster data transfer rate.
by exploiting two methods. First, it used direct memory access (DMA). Second, the data transfer is designed focusing on maximum single unit transfer rather than splitting the transfer into several time frames. ACE is implemented with 16-bit fixed-point quantization to represent the floating-point data. $B = A + 2^{k-1}$ is the quantization rule where “A” is a floating-point number, “B” is quantized number and “b” represents quantization bit.

**Overflow-aware Computation:** Fixed point calculation in resource constraint device frequently suffers from data overflow error. During FFT computation, there is a possible data overflow if the totaling of the input array exceeds the capacity of the quantized bit. For example, in an 8-bit data quantization, the FFT will produce wrong results if the addition of the input array elements exceeds $2^3 = 256$. To address the challenge, ACE performs data scaling based on the array size in Algorithm 1. Besides, there are also possible overflow during accelerator operation (e.g., MAC, ADD, MPY). And the solution is provided using normalization as discussed in Section III-A.

**Circular Buffer Convolution:** ACE optimizes the memory usage by reusing the input/output buffer after a layer-level computation takes place. In the existing DNN implementation, an inference with N layers requires N buffers, as shown in figure 4. Instead of allocating memory for individual layers, ACE requires only two buffers (input and output) at most. ACE implemented circular buffer convolution, restructured the DNN inference, which reuses the buffer by interchangeing and overwriting the input and output pointer after finishing a layer-level computation. ACE can considerably reduce the memory footprint, irrespective of the layer size in a DNN inference. The size required for the buffer is $max(L_i), 1 \leq i \leq N$.

**Intermittent Inference with FLEX:**

This session presents FLEX, the software support for enabling intermittent inference when there are frequent power failures. Previous work can successfully checkpoint the system state, which however do not work efficiently due to the large amount of intermediate results and computation state that takes much time and energy. A recent work [6] proposes TAILS that exploits the special structured and loop-heavy computations of DNN and enables their intermittent executions by continuously saving the loop control states. This mechanism avoids the need to checkpoint large system states. However, it will cause severe progress setbacks when accelerators are utilized.

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**Algorithm 1 On-device BCM implementation**

1. **Input:** $W, I, cI, cW, cOut$
2. **Output:** $O$
3. $I \leftarrow SCALE-DOWN(I, \text{len}(I))$
4. $W \leftarrow SCALE-DOWN(W, \text{len}(W))$
5. $cI \leftarrow COMPLEX(I)$
6. $cW \leftarrow COMPLEX(W)$
7. $cOut \leftarrow IFFT(FFT(cI) \times FFT(cW))$
8. $O \leftarrow REAL(cOut)$
9. $O \leftarrow SCALE-UP(O, \text{len}(I), \text{len}(W))$
10. **return** $O$
11. **procedure** SCALE-DOWN($D, \text{length}$)
12. for each element in $D$
13. \hspace{1em} $element \leftarrow element/\text{length}$
14. end for
15. **return** $D$
16. **end procedure**
17. **procedure** SCALE-UP($D, H, I, W$)
18. for each element in $D$
19. \hspace{1em} $element \leftarrow element \times H \times I \times W$
20. end for
21. **return** $D$
22. **end procedure**

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**Hardware Acceleration of FL:** With the FFT/IFFT vector accelerators that run in extremely low power mode, the DNN inference time and energy can be significantly reduced for fully connected layers (FLs). We redesigned the computation of fully connected layer (CL) kernel at a time. For example, a typical convolution of a 3x3 kernel needs 18 operations (9 multiplication and 9 addition) with an input window. But accelerator can replace the whole with a single MAC operation, resulting in drastic improvement in overall convolution performance.

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**C. Intermittent Inference with FLEX:**

This session presents FLEX, the software support for enabling intermittent inference when there are frequent power failures. Previous work can successfully checkpoint the system state, which however do not work efficiently due to the large amount of intermediate results and computation state that takes much time and energy. A recent work [6] proposes TAILS that exploits the special structured and loop-heavy computations of DNN and enables their intermittent executions by continuously saving the loop control states. This mechanism avoids the need to checkpoint large system states. However, it will cause severe progress setbacks when accelerators are utilized.
ABC-based FC layer: The left part of Figure 5 demonstrates the drawback of TAILS when we try to employ FFT-based BCM computation under the intermittent power supply. An FFT-based BCM computation has to go through several steps including DMA, FFT/IFFT, and MPY as shown in algorithm 1. The arrays highlighted in red, x, w, y, y' are intermediate values. In loop-index based technique, these are very much susceptible to data loss whenever a power failure happens. On power restore, the program has to roll back to the initial DMA operation because only the loop index is insufficient to retrieve the current state of the Algorithm. It causes wasted work and hurts the progress. As a solution, FLEX stores block index, intermediate input data and state bit of the Algorithm. As shown in the right part of Figure 5, FLEX specifies the four additional bits b0-b2 to indicate the current state, resulting in a successful continuation from the interrupted operation on power failure. Adding these four flags will cost only four bits in a successful continuation from the interrupted operation on power restoration because only the loop index is insufficient because read/write only happens when the system is restored.

Other layer: Apart from the BCM-based FC layer, FLEX follows loop index-based checkpointing mechanism. With the help of a voltage monitor system, FLEX predicts a power failure if the voltage drops below a threshold. And finally, checkpoint and restore the system based on loop index.

IV. EXPERIMENTS

A. Experimental Setup

Hardware Setup: The proposed DNN implementation framework is evaluated with TI’s MSP430FR5994 ultra-low-power evaluation board, consisting of a 16 MHz MCU, a 8KB volatile RAM, a 256KB nonvolatile FRAM memory, and a low-energy Accelerator (LEA) that runs independently of CPU. The LEA accelerator supports FFT, IFFT, MAC, and MPY operation. The board is connected to the function generator SIGLENT SDG1032X to simulate the energy harvesting scenario. Energy is buffered with capacitor of 100μF. For the energy measurement we used CCS energy trace technology.

DNN Models: This paper considers three DNN models as shown in Table 1. They are Image Classification (MNIST) [8], Human Activity Recognition (HAR) [2], and Google Keyword Recognition (OKG) [15] to represent image-based applications, wearable applications, and audio applications respectively.

B. Experimental Results

We evaluated our framework by comparing with Base, a baseline implementation that does not tolerate intermittent operation, and SONIC and TAILS [9], the state-of-the-art solution.

1) CNN Model Training and Pruning: Table 1 shows the compression technique and ratio applied in each layer of the three DNN models. We applied filter pruning and BCM on the MNIST dataset, performing 1.6x and 128x compression. For the HAR dataset, channel pruning performed 2.3x, and BCM performed 128x, and 64x compression for the two fully connected layers. OKG is the largest, and each of its layer is compressed except the last FC layer. Here, channel prunning and filter prunning are performed for the first two layers with compression of 2x and 2.3x, respectively. The subsequent FC layers are compressed with 256x and 128x ratio. Our model obtained 0.30%, 2.16%, and 0.10% higher accuracy than SONIC & TAILS on the three datasets as shown in figure 6(a).

2) Inference Time under Continuous Power Supply: We can observe from the figure 6(a) that ACE and FLEX run 3x, 4x, 3.3x faster inference than the Base, SONIC, and TAILS, respectively, on MNIST dataset. For HAR dataset, it is 5.4x, 5.7x, 2.6x faster. And lastly, it performs 1.7x, 3.3x, 2.1x faster on OKG dataset. This significant performance improvement is achieved by allowing the on-board acceleration engine to perform at the full extent with DMA-based data transfer. During the inference, we can see that most of the computation time is spent on convolutional layer while FC layer runs extremely fast.

3) Inference Time under Intermittent Power Supply: Under intermittent power supply, as shown in figure 6(b) the Base model and ACE can never be completed because they do not tolerate intermittent power failure. However, ACE with FLEX can successfully complete the inference because FLEX is developed to provide intermittent support. Besides, FLEX also reduced the wasted work and checkpointing overhead. Due to power failure, there is a negligible increase in latency and energy consumption, achieving almost similar latency and energy as continuous power. Here, ACE + FLEX run 5.1x, 3.8x faster than the SONIC, and TAILS, respectively on MNIST dataset. For HAR dataset, it is 4.7x, 2.4x faster. And lastly, it performs 3.3x, 1.7x faster on OKG.

4) Energy Consumption and Performance: In terms of energy consumption, our techniques performed ever better. We can observe from figure 6(c) that ACE and FLEX outperform SONIC and TAILS by achieving 6.1x and 4.31x energy-saving on MNIST. 10.9x and 5.26x energy-saving on HAR. And finally, 6.25x and 3.05x energy is saved on OKG. LEA and DMA run in ultra-low power mode and resulting in a significant amount of energy saving.

Specifically, Figure 7 demonstrates how ACE is successful in improving the overall performance of an FC layer. ACE is performed both independently and with different BCM block size (32, 64, 128) on first FC layer of MNIST model. Employment of BCM proposed in this paper can significantly reduce the latency and energy needed. A larger block size of BCM reveals better performance and more compression. However, selecting a larger block size is limited by device...
Inference time on intermittent power (100µF)

Energy breakdown

Energy of our resource-constrained framework.

Support and accuracy degradation which proves the efficiency of our resource-constrained framework.

Evaluation of checkpointing overhead:

The proposed novel checkpointing mechanism considers special structure of DNN models and thus only saves a result, necessary loop indices, and several control bits as shown in Figure 5. Every checkpoint/restore cost is at most 0.033mj, which was reached if power failure happens when computing the FFT-ery checkpoint/restore cost is at most 0.033mj, which was reached if power failure happens when computing the FFT-

V. RELATED WORK

With the advancement of CNN and IoT, several works have been proposed to implement CNN on IoT devices. SONIC is an intermittence-aware software system with specialized support for DNN inference [8]. NeuroZERO introduces a co-processor architecture consisting of the main microcontroller that executes scaled-down versions of a (DNN) inference task [9]. A software/hardware co-design technique that builds an energy-efficient low bit trainable system is proposed in [4]. Efficient memory aware data flow technique is proposed to implement DNN on resource constraint devices [7]. TF-Net pipeline efficiently deploys sub-byte CNNs on microcontrollers [14]. Different from the above works, this is the first work that explores BCM-based DNN algorithms on resource-constrained energy harvesting IoT devices.

VI. CONCLUSION

An efficient framework for DNN implementation on energy harvesting devices is proposed which includes a resource-aware DNN training and pruning method, a DNN implementation method utilizing accelerators, and novel software support for intermittent computation that considers accelerators. The experimental results demonstrate significantly reduced DNN footprint and energy consumption, and improved performance.

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