Performance Analysis of Vertically Stacked Nanosheet Tunnel Field Effect Transistor with Ideal Subthreshold Swing

Garima Jain 1 · Ravinder Singh Sawhney 1 · Ravinder Kumar 1 · Amit Saini 2

Received: 18 April 2021 / Accepted: 29 July 2021 / Published online: 5 August 2021 © Springer Nature B.V. 2021

Abstract
In this paper, a novel vertically stacked silicon Nanosheet Tunnel Field Effect Transistor (NS-TFET) device scaled to a gate length of 12 nm with Contact poly pitch (CPP) of 48 nm is simulated. NS-TFET device is investigated for its electrostatics characteristics using technology computer-aided design (TCAD) simulator. The inter-band tunneling mechanism with a P-I-N layout has been incorporated in the stacked nanosheet devices. The asymmetric design technique for doping has been used for optimum results. NS-TFET provides a low leakage current of order $10^{-16}$ A, an excellent subthreshold swing (SW) of 23 mv/decade, and negligible drain induced barrier lowering (DIBL) having a value of 10.5 mv/V. The notable ON to OFF current ratio of the order of $10^{11}$ has been achieved. The device exhibits a high transconductance of $3.022 \times 10^{-5}$ S at the gate to source voltage of 1 V. The radiation effect of an alpha particle at different energies on NS-TFET is investigated. The injection causes drain current fluctuation for a short span and the result can serve as a guideline for designing of a robust circuit. NS-TFET shows tremendous improvement in short channel effects (SCE) and is a good option for advanced technologies.

Keywords Nanosheet-tunnel field effect transistors (NS-TFET) · Nanosheet-field effect transistors (NS-FET) · Short Channel effects (SCE) · Band to band tunneling (BTBT) · Subthreshold swing (SW)

1 Introduction
Nanosheets have emerged as a potential successor to conventional Finfets and stacked nanowires for 7 nm technology and beyond [1–3]. Finfets need tall and thin fins, which enhance the fabrication cost and complexity [4] while the surface roughness factor degrades the performance of stacked nanowires [5]. The Nanosheet Field Effect Transistor (NS-FET) exhibits enormous current density due to its increased effective width per footprint [6]. NS-FET has good electrostatics control and hence remains immune to short channel effects [7]. It has been reported that NS-FET shows superior electrostatic performance in comparison to stacked nanowires or Finfets [8]. Thus NS-FET with 3D vertically stacked channels is a promising candidate for future advanced technology applications [6].

At low voltages, the device miniaturization below 50 nm leads to immense OFF-state power consumption and elevated subthreshold swing (SW) [9, 10]. The SW at CPP of 48 nm has been reported as 83 mv/decade and 94 mv/decade for nfet and pfet respectively [11]. The thermionic conduction mechanism of NS-FET makes SW temperature-dependent and this temperature constraint makes SW worse.

Vertically stacked Junctionless nanosheets(JL-Ns) show highly improved performance in terms of leakage current and SW [12]. JL-Ns with a different number of channels exhibit high ON current. At channel/oxide interface, JL-Ns provide indemnity for mobility degradation due to scattering of carriers [13]. The major bottleneck associated with JL-Ns is the exhibition of high leakage current while SW becomes non-scalable below 60 mv/decade.

© Springer
Tunnel Field Effect Transistors (TFETS) provide a remedy for high OFF-state current and exhibit steep SW [14–16]. TFETS work on the principle of the BTBT mechanism. In NS-FETS, the BTBT mechanism can be incorporated; thus making it a novel device consisting of vertically stacked nano-sheet tunnel field effect transistor (NS-TFET). Inner spacers can be treated as an underlapped region for TFETS. It has been further reported that underlapped source and drain regions assist in reducing ambipolarity [17, 18]. The fabrication process of TFETS varies from that of Mosfets in terms of their source doping. Thus, the fabrication of NS-TFET is comparatively easier to implement with minimal deviation from the NS-FET fabrication process [19, 20].

In section 2, we have discussed the calibration characteristics of NS-FET. Section 3 describes the design of a vertically stacked NS-TFET device with three layers. In our proposed work, the design parameters of the NS-TFET device are optimized to achieve good electrostatics. To the best of our knowledge, no tunneling-based Silicon stacked nanosheets with P-I-N configuration have been reported in the literature. Section 4 highlights the performance metrics of NS-TFET. The ultimate aim of NS-TFET is to tune the tunneling barrier at the extended source-channel junction; thereby reducing short channel effects such as low leakage current, minimal DIBL, and superior Subthreshold swing. Section 5 explains the drawn conclusions.

I. Calibration Characteristics

Vertically stacked Nanosheet transistors exhibit excellent ON-current density due to their increased effective width. The reference model of NS-FET with three layers having CPP of 48 nm, the gate length of 12 nm, and a sheet thickness of 5 nm are simulated on a visual TCAD platform [21]. The inner spacer thickness and the width of NS-FET are kept at 5 nm and 50 nm respectively. The vertical sheet-to-sheet spacing is 10 nm. A combination of high-k dielectric material HFO₂ having thickness 1.28 nm and SiO₂ having thickness of 0.5 nm has been used for effective oxide thickness of 0.7 nm. The symmetrical source and drain doping have a value of $3 \times 10^{20}$ cm$^{-3}$ while the channel doping is $1 \times 10^{17}$ cm$^{-3}$. Titanium Nitride material has been selected for gate with gate metal work function of 4.7 eV. The calibration graph of the simulation result is benchmarked with the experimental data at a drain voltage of 0.65 V as shown in Fig. 1.

1.1 The Fabrication Process Flow of NS-TFET in Tcad

The process flow of NS-TFET starts with the formation of Silicon on insulator (SOI) substrate. Then nanosheet stack is epitaxially grown over the substrate. The nanosheet stack comprises of alternating series of Si/SiGe layers. After that, fin patterning is done by anisotropic etching of Si and SiGe layers. Shallow trench isolations are filled with oxide in low thermal budget conditions. In a selected region of nanosheet stack, patterning of dummy gate and spacers is done. After dummy gate patterning, source and drain regions are epitaxially grown. The doping of the p⁺ source region involves three steps i.e. lithography, implantation and removal of photo-resist. The same procedure is then followed for n⁺ drain doping. Then etching of the dummy gate stack is performed. Then the subsequent release of the Si channel is done with the etching of sacrificial SiGe layers. The gate stack is formed by depositing high-k oxide and gate metal. A similar fabrication process flow is reported in the literature [11,35].

1.2 Device Structure

The dimensions of NS-TFET are in accordance with the reference structure [21]. The proposed NS-TFET device differs from the NS-FET device in terms of the type of doping. The reference structure has n-type symmetrical doping in both source and drain [21] while in NS-TFET; asymmetrical P-I-N configuration has been employed. P-I-N design with BTBT mechanism shows tremendous improvement in short channel effects (SCE). In the BTBT mechanism, the width of the tunneling barrier is modulated on the variation of gate voltage at constant drain voltage. The asymmetric lower drain doping is used to curb ambipolar behavior [22, 23]. Work function engineering has been done to achieve desirable results. For simulation of NS-TFET, the work function is chosen to be 5.00 eV. Figure 2 represents the 3-D view of NS-TFET. Figure 2b depicts a cross-sectional view of NS-TFET with P-I-N configuration. The geometric parameters, doping concentrations of NS-TFET are listed in Table 1.

Fig. 1 Calibration graph of transfer characteristics of NS-FET [21]
Physical models used in Genius code define the behavior of semiconductor devices [22]. These models specify physical parameters like mobility, recombination rate, etc. Drift-Diffusion (DD) model is the fundamental solver for Poisson’s and continuity equations [23] and has been recommended to use for determining the transport of charge carriers and computation of the drain current. The Lombardi model is invoked for carrier mobility in the inversion layer of the NS-TFET device. This mobility model incorporates bulk mobility, mobility due to surface charge, and scattering [24]. Gate tunneling plays a pertinent role in NS-TFET devices. Kane’s Model invokes the BTBT mechanism for carrier generation. For 3D simulations; Kane’s model provides better convergence results [31]. Shockley-Read-Hall (SRH) model has been considered for carrier recombination mechanism and it stimulates the leakage current that determines Ioff in TFETs [32].

2 Results and Discussion

Three-dimensional simulations of NS-TFET are done using COGENDA-TCAD software [24]. The physical models such as the DD model, Lombardi mobility model, Kane’s BTBT model, and SRH model are evaluated at each mesh node using TCAD software. The performance metrics of vertically stacked NS-TFET device has been discussed in this section.

2.1 Triple Nanosheet

Gate all-around devices provide little room for carriers to drift when the transistor is in ON state [25]. The stacking of nanowires increases the effective width and allows the carriers to flow, but the increased device capacitance along with surface roughness decreases the speed of carriers [26]. Stacking thin nanosheets atop one another enhances the effective width and hence provides larger room for carriers to flow. This further enables the large drive current while maintaining constricted control of the leakage current [25, 26].

We have performed the simulations for vertically stacked single, double and triple NS-TFETs at the drain to source voltage (Vds) of 0.65 V. The plot of drain current of single nanosheet (Id_1ns), double nanosheet (Id_2ns), and triple nanosheet (Id_3ns) is depicted in Fig. 3. The results show that ON-current increases exponentially in the case of double and triple NS-TFETs as compared to single NS-TFET. The drain current of Id_3ns and Id_2ns is observed to be 2.0168 and 3.03 times higher than Id_1ns respectively. Ion/Ioff ratio in triple-stacked NS-TFET is 9.557 times that of single NS-TFET while with double-stacked NS-TFET, it is observed to be 4.73 times high. Hence, three-layered NS-TFET exhibits superior performance in terms of drive current.

| Table 1 | The design parameters of vertically stacked NS-TFET [21] |
|---------|----------------|
| Parameters | Dimension |
| Gate length (Lg) | 12 nm |
| Gate work function of n-NS-TFET | 5.0 eV |
| Gate work function of p-NS-TFET | 4.23 eV |
| Source Doping (Na) | $3 \times 10^{20} \text{ cm}^{-3}$ |
| Drain Doping, (Nd) | $1 \times 10^{17} \text{ cm}^{-3}$ |
| Channel Doping, (Nch) | $1 \times 10^{16} \text{ cm}^{-3}$ |
| Effective oxide thickness, (EOT) | 0.7 nm |
| Nanosheet width, (Ns_W) | 50 nm |
| Nanosheet Thickness, (Ns_Th) | 5 nm |
The NS-TFET exhibits similar behavior to that of n-TFET on the application of constant drain voltage. In NS-TFET, an interband tunneling conduction mechanism has been incorporated. In the OFF state of the p-type extended source of NS-TFET, very few electrons are available at the conduction band of the source for injection into the channel. This results in negligible movement of carriers and hence poor leakage current. With variation in the gate voltage, the energy band of the channel varies relative to the extended source. From Fig. 4, it is evident that at saturation voltage of $V_{ds} = 0.65$ V with positive gate to source voltage ($V_{gs} > 0$ V), the valence band of the extended source is aligned with the conduction band of the channel. The carriers tunnel through the potential barrier between the valence band of the extended source and the conduction band of the channel. These charge carriers present in channel drift towards the extended drain (ext_d) to produce drain current.

### 2.3 On Current and OFF Current

Figure 5 depicts the transfer characteristics of NS-TFET. In the off state of TFETs with zero gate to source voltage, the movement of charge carriers from the valence band of the extended source region into the channel region is hindered due to large tunneling barrier width. Hence, the leakage current is extremely low. In the off state, linear leakage current ($I_{Lin}$) is of the order $10^{-16}$ A at gate voltage $V_{gs} = 0$ V with drain voltage $V_{ds} = 0.10$ V. On application of positive gate voltage, bandgap modulation takes place as shown in Fig. 4. With the gradual increase in gate bias, the bands of the channel are lowered; thus enabling more electrons to tunnel from the valence band of the extended source into the conduction band of the channel. The tunneling barrier width is reduced near the extended-source channel region leading to a steep increase in the drain current. At saturation voltage of $V_{ds} = 0.65$ V, leakage current is of order $10^{-14}$ A. The saturation ON current ($I_{sat}$) reported is $1.26 \times 10^{-5}$ A at $V_{ds} = 0.65$ V with $V_{gs} = 1.2$ V. Thus, the Ion/Ioff ratio for three-layered NS-TFET is $1.101 \times 10^{11}$. This high Ion/Ioff ratio is desirable for high-performance nanoscale devices.
2.4 Sub-Threshold Swing and DIBL

The main premise of designing NS-TFET as an alternative to NS-FET is due to its refined subthreshold swing. NS-FETs operate on a thermionic injection mechanism and thus have a thermal limit of 60mV/decade [27]. In NS-TFETs, the BTBT conduction mechanism is utilized. NS-TFET offers desired steep SW of 23mV/decade at low Vds = 0.10 V with the desired ON-state performance. For this subthreshold regime, the threshold voltage is 0.402 V and negligible Drain induced barrier lowering (DIBL) of 10.5 is found. SW gives a higher Ion/Ioff ratio and thus makes itself apt for faster switching circuitry. Table 2 represents the performance metrics of NS-TFET in terms of threshold voltage, SW, DIBL, etc.

2.5 Ambipolarity

The transfer characteristics of three-layered NS-TFET under different doping concentrations have been represented in Fig. 6. It is evident from the figure that NS-TFET shows its ambipolar behavior when it is subjected to the negative gate to source voltage(Vgs < 0 V). The electrons tunnel from the channel to the conduction band of the extended drain and thus results in the current flow of the same polarity and hence behave as p-type. This behavior is not desirable in digital circuitry where tunneling between channel and drain is curbed [28–30]. The best results are observed for the doping concentration of 10^{17} cm^{-3}. It is evident that with the decrease in the doping concentration of drain, an ambipolar current is reduced up to a considerable amount. The depletion width of the drain side increases due to lower drain doping concentration. As a result, the ambipolar current reduces.

2.6 Transconductance (g_m)

Transconductance (g_m) is a performance metric, which reflects the device efficiency in terms of effective input voltage conversion into output current [31]. It is described by first-order differentiation of drain current with reference to the gate to source voltage [32].

$$g_m = \frac{\partial I_{dd}}{\partial V_{GS}}$$

where I_{dd} represents current tunneling from the source terminal to the drain end. V_{gs}, V_{ds} represents the gate to source voltage and constant drain voltage respectively.

The simulation of single, double and triple NS-TFETS is done at Vds = 0.65 V. The plot of the transconductance variation of single nanosheet (single_ns), double nanosheet (double_ns), and triple nanosheet (triple_ns) is depicted in Fig. 7. From the figure, it is evident that there is an

| Table 2 | Figures of merit of NS-TFET |
|----------------|----------------------------|
| Figures of Merit | Values of n-NS-TFET | Values of p-NS-TFET |
| Leakage current | 1.0144 x 10^{-16}A | 1.16147 x 10^{-16}A |
| Ion/Ioff ratio | 1.101 x 10^{11} | 9.378 x 10^{11} |
| Threshold Voltage | 0.402 V | 0.400680 V |
| DIBL | 10.5 | 11.4 |
| Subthreshold swing | 23mV/decade | 23.786mV/decade |
enhancement in transconductance with an increase in gate voltage. This is due to the hike in tunneling of carriers in the channel. It is unambiguously clear that triple NS-TFET exhibits comparatively higher transconductance of $3.022 \times 10^{-5}$ S at the gate to source voltage of 1 V. The transconductance of triple ns is 1.5 and 3 times higher than double ns and single ns respectively. Hence, three-layered NS-TFET exhibits enhanced transconductance due to the larger effective width.

2.7 Transconductance Generation Efficiency (TGF)

Transconductance generation efficiency (TGF) is another vital parameter that determines the efficiency of NS-TFET in terms of conversion of the current into transconductance ($g_{m}$) and is given by [33]. The value of TGF increases with an increase in transconductance. High TGF depicts good analogue performance.

$$TGF = \frac{g_{m}}{I_{dd}} V^{-1}$$

(B)

The TGF variation of single (TGF_1ns), double (TGF_2ns) and triple nanosheet (TGF_3ns) with respect to the gate to source voltage is depicted in Fig. 8. It is observed that the TGF of NS-TFET reduces with an increase in gate voltage. This is due to the saturation of the drain current to a specific value. As a result, TGF decreases with an increase in $V_{gs}$. At low voltages, three layered NS-TFET shows max TGF. For the selected value of $I_{dd} = 10^{-10}$ A, TGF_1ns, TGF_2ns, TGF_3ns is found to be 41 $V^{-1}$, 50 $V^{-1}$ and 54 $V^{-1}$ respectively.

2.8 Total Gate Capacitance ($C_{gg}$)

The total gate capacitance ($C_{gg}$) is the summation of intrinsic capacitances of the source and drain terminals. High transconductance and low gate capacitance are requisite for good analogue performance [32]. The plot of the total gate capacitance ($C_{gg}$) as a function of gate-source voltage ($V_{gs}$) at $V_{ds} = 0$ V and $V_{ds} > 0$ V is depicted in Fig. 9. For $V_{ds} = 0$ V, total gate capacitance ($C_{gg}$) shoots at a lower value of $V_{gs} = 0.8$ V while for $V_{ds} > 0$ V, a significant increase of ($C_{gg}$) is observed at higher $V_{gs}$. The value of ($C_{gg}$) at $V_{gs} = 1$ V and $V_{ds} = 0.65$ V $V_{gs} = 1$ V is found to be $1.662 \times 10^{-17}$ F.

2.9 P-ns-TFET Design

The vertically stacked NS-TFET with N-I-P configuration has been designed to demonstrate its p-type characteristics. The geometry parameters are kept the same as mentioned in Table 1. Work function engineering has been implemented to match ON and leakage currents. For p-SN-TFET, the work function is kept at 4.23 eV. The source has donor impurities with a concentration of $3 \times 10^{20}$ cm$^{-3}$ while the drain has
acceptor impurities having a concentration of $10^{17}$ cm$^{-3}$. The transfer characteristics of p-SN-TFET at linear voltage $V_{ds} = -0.10$ V and saturation voltage of $V_{ds} = -0.65$ V are simulated using TCAD. The simulation results of both p and n-type at linear and saturation voltage are displayed in Fig. 10. The performance metrics of p-NS-TFET are mentioned in Table 2.

2.10 Alpha Particle Effect on NS-TFET

The effect of alpha particle radiation on NS-TFET has been investigated in Fig. 11. The impact of alpha particle injection into the source region is greater than that into the drain region [34]. So in the proposed device, the particle is injected into the centre of the source region with an incident angle of 90°. On injection, drain current shoots due to the generation of electron-hole pairs and then restores to the steady-state due to recombination of electron-hole pairs. Figure 11 depicts the variation of drain current with time at three different alpha particle energy injections (3 MeV, 4 MeV and 5 MeV). The peak drain current is observed to be 24.9 μA, 23.3 μA and 21.83 μA for 3 MeV, 4 MeV and 5 MeV alpha particle energy injections respectively. The hike in the current is observed for a short duration of 13.80 ps, 13.70 ps, and 13.50 ps at incident energies of 3 MeV, 4 MeV and 5 MeV respectively.

3 Conclusion

In this paper, vertically stacked NS-TFET with three layers has been modeled and simulated. The short channel effects have reduced tremendously by using the BTBT mechanism with P-I-N configuration. A high Ion/Ioff ratio with a low leakage current has been achieved. NS-TFET renders 23mV/decade SW and 10.5 DIBL which is 70% and 65% lower than NS-FET respectively. High Transconductance, device efficiency, total capacitance parameters of NS-TFET have been extracted. The injection of an alpha particle on NS-TFET results in drain current fluctuation for a short span and recovers soon. p-TFET configuration for NS-TFET has also been proposed which makes it apt for faster switching applications. All these advantages make NS-TFET a viable option for next-generation applications and future advancements.

Acknowledgements We thank the Group, department of Electronics Technology, Guru Nanak Dev University, Amritsar for their interest in this work and useful comments to draft the final form of the paper. The support of CADRE Design Systems is gratefully acknowledged. We would like to thank Guru Nanak Dev University, Amritsar and Cadre Design Systems for lab facilities and research environment to carry out this work.

Authors’ Contributions All authors contributed to the design and simulation. Material preparation, data collection and analysis were performed by Garima Jain, Dr. Ravinder Singh Sawhney, Dr. Ravinder Kumar and Amit Saini. The first draft of the manuscript was written by Garima Jain and all authors commented on previous versions of the manuscript. All authors read and approved the final manuscript.

Declarations

Conflicts of Interest/Competing Interests the authors have declared that no competing interests exist.

Availability of Data and Material Not applicable.

Compliance with Ethical Standards This study was approved by the university research ethics committee. All procedures performed in this study follow the ethical standards of the institutional and research committee.

Consent to Participate Not applicable.

Consent for Publication Yes

References

1. Jang D, Yakimets D, Eneman G, Schuddinck P, Bardo MG (2017) Device Exploration of NanoSheet Transistors for Sub-7-nm Technology Node. IEEE Trans Electron Devices 64(6):2707–2713. https://doi.org/10.1109/TED.2017.2695455
2. Barraud S, Lapras V, Previtali B, Samson MP, Lacord J, Martinie S, Jaud MA, Athanasiou S, Triorzon F, Rozan O, Hartmann JM, Vizioz C, Combroure C, Andreiu F, Barbé JC, Vinet M, Ernst T (2017) Performance and design considerations for gate-all-around stacked-NanoWires FETs. IEEE International Electron Devices Meeting (IEDM). doi: https://doi.org/10.1109/IEDM.2017.8269473
3. Yakimets D, Bardon MG, Jang D, Schuddinck P, Sherazi Y, Weckx P, Miyaguchi K, Parvais B, Raghavan P, Spessot A, Verkest D, Mocuta A (2017) Power-aware FinFET and lateral nanosheet FET targeting for 3nm CMOS technology. IEEE international Electron devices meeting (IEDM), San Francisco. https://doi.org/10.1109/IEDM.2017.8268429
4. He X, Fronheiser J, Zhao P, Hu Z, Uppal S, Wu X, Hu Y, Sporer R, Qin L, Krishnan R, Bazizi EM, Carter R, Tabakman K, Jha AK, Yu...
H, Hu O, Choi D, Lee JG, Samavedam SB, Sohn DK (2017) Impact of aggressive fin width scaling on finFET device characteristics. IEEE international Electron devices meeting (IEDM), San Francisco. https://doi.org/10.1109/IEDM.2017.8268427

5. Bufler FM, Ritzenhaller R, Mertens H, Eneman G, Mocut A,柄higuchi N (2018) Performance Comparison of n-Type Si Nanosheets, and FinFETs by MC Device Simulation. IEEE Electron Device Lett 39(11):1628–1631. https://doi.org/10.1109/LED.2018.2868379

6. P. Feng, S. Song, G. Nallapani, J. Zhu, J. Bao, V. Moroz, M. Choi, X. Lin, Q. Lu, B. Colombue, N. Breil, M. Chudzick and C. Chadambaram, "Comparative Analysis of Semiconductor Device Architectures for 5-nm Node and Beyond pp.," IEEE Electron Device Lett, vol. 38, no. 12, p. 1657–1660, Dec 2017. doi: https://doi.org/10.1109/LED.2017.2769058

7. Kalna K, Nagy D, Garcia-Loureiro AJ, Seoane N (2019) 3D Schrödinger equation quantum corrected Monte Carlo and Drift diffusion simulations of stacked Nanosheet gate-all-around transistor, in IWCN. Institute for Microelectronics, TU Wien, Wien, pp 33–35

8. Kim SD, Guillom M, Lauer I, Oldiges P, Hook T, Na MH (2015) Performance Trade-offs in FinFET and Gate-All-Around Device Architectures for 7nm-node and Beyond. IEEE SOI-3D-subthreshold microelectronics technology unified conference (S3S), Rohnert Park. https://doi.org/10.1109/S3S.2015.7335251

9. Yakimets D, Bardon MG, Jang D, Schuddinck P, Sherazi Y, Weckx P, Miyauchi K, Parvais B, Raghavan P, Spessot A, Verkest D, Mocuta A (2017) Power aware FinFET and lateral nanosheet FET targeting for 3nm CMOS technology. IEEE International Electron Devices Meeting (IEDM), p. 501–504. doi: https://doi.org/10.1109/IEDM.2017.8268429

10. Cai L, Chen W, Du G, Zhang X, Liu X (2018) Layout design correlated with self-heating effect in stacked Nanosheet transistors. IEEE Trans Electron Devices 65(6):2647–2653. https://doi.org/10.1109/TED.2018.2825489

11. Loubet N, Hook T, Montanini P, Yeung CW, Kanakasab S Stacked nanosheet gateallaround transistor to enable scaling beyond FinFET. In Symposium on VLSI Technology, T230–T231, 2017. doi: https://doi.org/10.23919/VLSIT.2017.7998183

12. Moon D, Choi S, Duarte JP, Choi Y (2013) Investigation of silicon nanowire gate-all-around Junctionless transistors built on a bulk substrate. IEEE Trans Electron Devices 60:1355–1360. https://doi.org/10.1109/TED.2013.2247763

13. Chen H, Wu Y, Chang C, Han M, Lu N, Ch Y (2013) Performance of GAA poly-Si nanosheet (2nm) channel of junctionless transistors with ideal subthreshold slope. In Symposium on VLSI technology

14. Choi WY, Park B, Lee JD, Liu TK (2007) Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec. IEEE Electron Device Lett 28(8):743–745. https://doi.org/10.1109/LED.2007.901273

15. Colinge J (2008) FinFETs and other multi-gate transistors. Springer, New York. https://doi.org/10.1007/978-3-540-71752-4

16. Kumar S, Goel E, Singh K, Singh B, Singh PK, Baral K (2017) 2-D analytical modeling of the electrical characteristics of dual-material double-gate TFETs with a si02/hf02 stacked gate-oxide structure. IEEE Trans Electron Devices 64(3):960–968. https://doi.org/10.1109/TED.2017.2656630

17. Vaddi R, Agarwal RP, Dasgupta S (2011) Analytical modeling of subthreshold current and subthreshold swing of an underlap DGMOSET with tied–independent gate and symmetric-asymmetrical options. J Microelectron 42(5):798–807. https://doi.org/10.1016/j.mejo.2011.01.004

18. Wadhwa G, Raj B (2018) Label free detection of biomolecules using charge-plasma-based gate underlap dielectric modulated Junctionless TFET. J Electronics Material Springer 47(8):4883–4893. https://doi.org/10.1007/s11664-018-6343-1

19. Cao W, Sarkar D, Khatami Y (2014) Subthreshold-swing physics of tunnel field-effect transistors. AIP 4(6):067141–1–067141-9. https://doi.org/10.1063/1.4881979

20. Vijayvargiya V, Reniwal BS, Singh P, Vishvakarma SK (2016) Analogue/RF performance attributes of underlap tunnel field effect transistor for low power applications. Electron Letters 52(7):559–560. https://doi.org/10.1049/el.2015.3797

21. Jegadheesan V, Sivasankaran K, Konar A (2019) Impact of geometrical parameters and substrate on analog/RF performance of stacked nanosheet field effect transistor, Mater Sci Semicond Process 93:188–195. https://doi.org/10.1016/j.mssp.2019.01.003

22. Dutta U, Soni MK, Pattanaik M (2018) Design and Optimisation of GATE-All-Around Tunnel FET for Low Power Applications. Int J Eng Technol 7(4):2263–2270. https://doi.org/10.14419/ijet.v7.i4.12352

23. D. B. Abdi and M. J. Kumar, “Controlling Ambipolar Current in Tunneling FET’s using Overlapping Gate-on Drain,” J. Electron Devices Soc, vol. 2, no. 6, pp. 187–190, Nov. 2014. doi: https://doi.org/10.1109/JEDS.2014.2327626 Genius Semiconductor Device Simulator Reference Manual

24. Bardhan PH, Ganguly AS, Gangu U (2019) Threshold voltage variability in Nanosheet GAA transistors. IEEE Trans Electron Devices 66:4433–4438. https://doi.org/10.1109/TED.2019.2933061

25. Ye P, Ernst T, Khare MV (2019) The last silicon transistor: Nanosheet devices could be the final evolutionary step for Moore’s law. IEEE Spectr 56:30–35. https://doi.org/10.1109/MSPEC.2019.8784120

26. Dash TP, Dey S, Mohapatra E, Das S, Jena J (2019) Vertically-Stacked Silicon Nanosheet Field Effect Transistors at 3nm Technology Nodes. Devices for Integrated Circuit (DevIC), pp. 99–103. doi: https://doi.org/10.1109/DEVIC.2019.8783300

27. Lu H, Seabaugh A (2014) Tunnel FET transistors: state-of-the-art. IEEE J Electron Devices Soc 2(4):44–49. https://doi.org/10.1109/JEDS.2014.2326622

28. Ionescu AM, Riel H (2011) Tunneling field-effect transistors as energy-efficient electronic switches. Nature 479:329–337. https://doi.org/10.1038/nature09679

29. Kumar J, Vishnoi R, Pandey P (2017) Tunnel field-effect transistors (TFET): modelling and simulation, John Wiley & Sons, Ltd. doi: https://doi.org/10.1002/9781119246112

30. Dash S, Sahoo GS, Prasad G (2016) Improved cut-off frequency for cylindrical gate TFET using source delta doping. Procedia Technol 25:450–455. https://doi.org/10.1016/j.protcy.2016.08.131

31. Dutta U, Soni MK, Pattanaik M (2018) Simulation study of hetero dielectric tri material gate tunnel FET based common source amplifier circuit. Int J Electron Commun 9:2263–2270. https://doi.org/10.1016/j.aeue.2018.12.004

32. Vakkalakula BS, Vadthiya N (2021) Design and temperature assessment of junctionless nanosheet FET for nanoscale applications. Silicon 14:5067–5074

Publisher’s Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.