The Design of Virtual Low-Voltage Power Line Noise Generator

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Abstract. Proposed to apply the virtual instrument way to structure the noise generator, according to the complex features of the noises on the low-voltage power line. It talks about the design of the core circuit, used the CPLD-based DDS to stimulate the PLL frequency synthesiser to form the clock generator. Analyzed the method to suppress the phase-noise and the spurious signals of the frequency-synthesis system, proposed to use the balanced scrambling system to suppress the spurious noises from the phase truncation, solved the difficulties in the broad-band signal coupling.

1. Preface
There are many advantages like convenience, quickness, less labor when using low-voltage power line as the communication channel in controlling the applied electronics and multi-meter copying. For the communication channels, the characteristic of the noise is one of the major features. Because the low-voltage net faces directly to the customers, the load noise from all the customers under one distribution transformer will surely disturb the channels, as well as the original side noise from the transformer, so they bring a lot of difficulties to an reliable communication.

This article designed a USB-interfaced virtual noise generator based on the test and analysis of the noises ranged from 100K to 10MHz, the complicated data analyzing, processing and synthesizing are manipulated through a managing software on computer. To simulate the usual noises that affect the communication, and output through high-speed D/A and power amplifier. So it can offer a testing platform for the developers and testers of the carrier communication. The USB bus device is very convenient, flexible, low cost and universal to work as the interfaces on virtual instruments.

2. Classification and analysis of the noises on low-voltage power line
The noises on the low-voltage power line are mainly from the connected applied electronics, we classified and counted some typical electronic noises, there are mainly four forms of them:

(1) Random pulse noise
It is mainly occurred when the protection switch turning off or on. Each pulse noise will affect a very broad band. Its arrival time is random, and it can last from several μs to several ms. The pulse wave shape is like damping sine wave or serried damping sine wave.

(2) Continuous noise irrelevant to the power frequency.
It is mainly produced by the horizontal scanning signals of the TV set and monitors, the peak on the power spectrum graph appears at the horizontal scanning signal and its harmonic frequency points. The repeating frequency is usually 50 to 200Hz.

(3) Periodic noises synchronized to the power frequency.
It is mainly produced by the electronic devices, the repeating rate is 50Hz or 100Hz, it last only for a very short time, the power spectrum decreases when the frequency increases. These electronic devices are air conditioner, computer, etc. The disturbance sometimes can be very large, the peak-peak value can reach over 10V.

(4) Background noise

It is a compound interference produced by all the noises on the power line, is a random interference varied slowly with time, its power spectrum density decreases when frequency increases. The background noise basically keeps a level state in the 100kHz to 10MHz band. Its feature appears to be white noise.

The noises on the power line are very complicated, the amplitude damps with the growing frequency, the distribution of the noise changes when the time, address and load varies. We setup the noise generator in a virtual instrument way, the noise synthesis is done by software, the customer can expand the functions with programming to get the highest cost performance, without changing the original circuits.

3. The structure of the virtual low voltage power line noise generator

The basic principal structure of the virtual low-voltage power line noise generator is shown in Figure 1. because the output frequency of the noise signal can reach 10MHz, the microcontroller can not control it to make real-time output. In the design, a high-speed CPLD was used to produce the logics, and control the process of the output. The software of the computer then changes the data into the correspondent numbers, and transmit them to the microcontroller through the USB bus. When the microcontroller receives the updating command, it asks the CPLD for the SRAM bus control permission, and updates the waveform data in the SRAM, after that, it returns the SRAM control permission back to CPLD. CPLD then control the high-speed D/A converter to complete the waveform output. the amplitude, frequency and cycle time can be modified by the software. This design makes full use of the CPLD’s features like high-speed, high-integrity, and programmable, to complete the logic design, it can promote the system performance, and simplified the designing and testing job at the same time.

The virtual instrument software is designed using Visual Basic under WINDOWS operation system, including the waveform editing and choosing. The soft panel is shown in Figure 2. the amplitude, frequency, offset can be changed, to control the instrument to generate the needed waveforms. It receives different commands from the customer, and control the instrument.
4. The principles and design of the core circuits

The core of the noise generator is the microcontroller, it has the global control power. In one way, it deals with the computer through USB interface, let computer send the waveform data; in another way, the microcontroller controls the CPLD to manipulate the to-generate signals.

4.1. The USB interface and the microcontroller control.

The microcontroller module is composed of a USBN9604, and a low-power-cost microcontroller Cygnal8051-F231. The microprocessor communicates with the USBN9604 in the SPI mode [1]. Figure 3 shows the connection of the microprocessor and USBN9604.

4.2. The design of the high frequency clock generator circuit

According to the requirements of the design, the noise generator’s resolution should reach 10mHz, the maxim output frequency should reach 10MHz, we use a 40MHz system crystal, the phase adder is 32-bit. \( \Delta f = f_c / 2^N = 10 \text{mHz} \). We chose EMP7128S84 as our CPLD, when use the 32-bit adder, the clock could only reach 18.66MHz, it obviously fail to meet the requirements. So, to gain a high-resolution, fast transformation, broad bandwidth signal, the clock generator adopts using the low-frequency DDS to stimulate PLL, and synthesis the frequency [2]. We applied high phase-detection frequency to improve the PLL transforming speed, and we use the high resolution of the DDS to make the output highly resolved. Meanwhile, the band of bandwidth filter of the PLL loop can suppress the stray outside the DDS band. To keep the purity of the output spectrum, a bandwidth filter is connected to the output of the DDS, to suppress the broadband stray of the DDS referenced frequency\(^1\). The principal block diagram is shown in Figure 4.
To make sure the output signal has a wide editable range, we insert a M frequency divider between the DDS output frequency $f_1$ and the PLL phase comparator. And insert a M frequency divider between the VCO output frequency $f_0$ and the phase comparator, so here we got: $f_0=Nf_1/M$, we can get different frequency by editing the integer M,N. The phase adder and the frequency dividing and counting circuit are realized in the CPLD, This is shown in Figure 5. CPLD is the key to the whole system. We use EMP7123s84 chip of the ALTERA company. It has the technology of COMSEEPRM, the highest clock frequency can reach 100 MHz, and it has 5000 logic gates, 64 I/O ports, 192 registers. It receives the commands and waveform data from the computer, and produce the control and address signal for the chips and SRAM, and output the damping data to the damping net. A piece of NE564 was applied in the phase lock loop circuit, after a series test of simulation, the clock generator can work at about 45.78 MHz, it met our requirements.

4.3. The design of the waveform storage circuit.
Concerning the flexibility and speed, we use a SRAM to store the waveform in the design, the chosen device is 62C256, the total capacity is 32KB, the fastest writing and reading time is 12ns, there are 15 address ports, 8 data ports. Because the D/A converter we use (AD9762) has 12 bit data bus, so two SRAM chips are used. Considering of all the waveforms, the capacity and the resolution of the DA converter, we change every cycle of the waveform into 4096 numbers.

4.4. The design of the D/A converter
The data from the SRAM will come to the DA converter, and output the waveform. In this design, the DA converter AD9762 was applied. AD9762 applies a segmented current source architecture. There is a 1.2V internal reference voltage, if a stable full range output current is required, the internal reference source can be used directly. however, when a modifiable full range current output is needed(take amplitude for an instance)or the accuracy should be promoted and the drift feature should be contained, the exterior reference source is in need.

4.5. The design of the power line coupler
Because the structure and the load is changing all the times, the characteristic impedance and the load impedance of different frequency spots also changes, and it brings lots of difficulties to the design of the coupling device. In order to perfect the damping features of the coupling device, the high frequency impedance decoupling must be kept as low as possible, to satisfy the flat and low working damping in the broad bandwidth. Figure 6 is the principal circuit of the power line coupler.
5. The suppress of the phase truncation spurious signals

In the real DDS, there are many spurious signal in the spectrum of the output signal, including the phase truncation, storage of compressed data, data transforming, DAC’s non-ideal features, and the stray signal from the non-ideal features of the low-pass filter, among all of these, the stray signal from the phase cut-off is the major problem. The technology of balanced scrambling, the diagram is Figure 7. The results of the simulation proved that, balanced scrambling technique perfected the output signals better than traditional scrambling technology, the spectrum of the output can be 20 dB better.

6. Conclusion

The power line noise generator can produce modifiable noises. We could first store some real-time noises using a digital oscilloscope, then transmit to the computer, and to the circuit to stimulate. We considered EMC in the design, deeply analyze the choosing and aligning of the chips, and the routing, grounding and shielding, proposed our responding solutions.

References

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