Impact of PECVD µc-Si:H deposition on tunnel oxide for passivating contacts

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Abstract. Passivating contacts are becoming a mainstream option in current photovoltaic industry due to their ability to provide an outstanding surface passivation along with a good conductivity for carrier collection. However, their integration usually requires long annealing steps which are not desirable in industry. In this work we study PECVD as a way to carry out all deposition steps: silicon oxide (SiOx), doped polycrystalline silicon (poly-Si) and silicon nitride (SiNx:H), followed by a single firing step. Blistering of the poly-Si layer has been avoided by depositing (p+)-microcrystalline silicon (µc-Si:H). We report on the impact of this deposition step on the SiOx layer deposited by PECVD, and on the passivation properties by comparing PECVD and wet-chemical oxide in this hole-selective passivating contact stack. We have reached iVoc > 690 mV on p-type FZ wafers for wet-chemical SiOx(p+)-µc-Si:SiNx:H with no annealing step.

Keywords: Silicon solar cell / passivating contact / silicon oxide / µc-Si:H / PECVD / XPS / passivation / cast-mono

1 Introduction

Crystalline silicon solar cell is the dominant technology in today’s photovoltaic (PV) market. In order to foster PV development and make it economically more competitive, it is necessary to further reduce production costs as well as to increase cell efficiencies. In order to achieve the latter, reducing recombination losses at the metal/semiconductor interface is of paramount importance. To do so, the integration of so-called passivating contacts is a mainstream option [1–3]: they consist of a silicon oxide (SiOx) doped polycrystalline silicon (poly-Si) and silicon nitride (SiNx:H), followed by a single firing step. Blistering of the poly-Si layer has been avoided by depositing (p+)-microcrystalline silicon (µc-Si:H). We report on the impact of this deposition step on the SiOx layer deposited by PECVD, and on the passivation properties by comparing PECVD and wet-chemical oxide in this hole-selective passivating contact stack. We have reached iVoc > 690 mV on p-type FZ wafers for wet-chemical SiOx(p+)-µc-Si:SiNx:H with no annealing step.

2 Methods

2.1 Sample fabrication

2.1.1 Substrate

Firstly the SiOx and (p+)-poly-Si layers were developed on one side of double side polished (DSP) n-type Cz silicon wafers (280 µm thick, and wafer resistivity of 1–5 Ω·cm), that were cleaned with a HF dip (5% for 30 s). Secondly, the “lifetime samples” were symmetrical structures, deposited on three kinds of p-type silicon substrates described in Table 1.

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Table 1. Characteristics of p-type wafers used for lifetime samples. SDR stands for saw damage removal, and the texturation bath is composed of KOH and additives.

| Float-zone | Cz | Mono-cast |
|------------|----|-----------|
| DSP        | SDR + textured | SDR + textured |
| 280 μm     | 170 μm | 190 μm    |
| 3–5 Ω.cm   | 2–4 Ω.cm | 1–3 Ω.cm |

These wafers were RCA cleaned and the remaining oxide was removed by an HF dip (HF 5% diluted in deionized water DIW, for 20s).

2.1.2 Tools

The SiO$_2$ layer was either deposited in an RF-PECVD reactor Octopus II (INDEOtec) at 175°C with a gas mixture of SiH$_4$, H$_2$ and CO$_2$, or wet-chemically grown with the DeltaPsi2 Jobin Yvon Uvisel 2 ellipsometer. The data were processed using the Thermo Avantage® software.

The optical properties of the deposited layers were acquired using a WCT-120 (Sinton Instruments). Photoluminescence (PL) images calibrated in lifetime were acquired with an LIS-R2 (BT Imaging).

### 3 Results and discussion

#### 3.1 PECVD process

We developed a process for depositing SiO$_2$ by PECVD at 175°C (Batch 1). In order to supply the required oxygen amount, we increased the $r = CO_2/SiH_4$ gas flow rates ratio. The optical properties of these films were measured by SE, and fitted with Tauc-Lorentz model [7]. For $r = 10$ we got a material with $n(633 nm) = 1.6$ and $k(400 nm) = 0.007$.

In standard passivating contact fabrication, a hydrogenated amorphous silicon (a-Si:H) layer is deposited, and then annealed for a long time at high temperature (usually 850°C for 30 min or more [5,8–10]). This can lead to the formation of blisters. The aim of this work being to spend a low thermal budget, this annealing step was skipped. A single firing step, however, leads to even higher stress, resulting in an easier formation of blisters. One way to tackle this issue was to dilute SiH$_4$ into H$_2$ [10,11]. We deposited 1–2 μm of PECVD SiO$_2$ (30 s deposition), and subsequently deposited the boron doped silicon layer on top of it. Doing so, we varied the SiH$_4$ flow rate, and consequently its dilution into hydrogen. The samples were then subject to a firing step (850°C for a few seconds). The confocal images of the surface are shown in Figure 1. It can be seen that at lower R = H$_2$/SiH$_4$ flow rate ratio ($R = 50$), a lot of blisters form, whereas at $R = 125$, none can be seen. The thicknesses of the layers are respectively, for $R = 50$/63/83/125: 38/33/26/24 nm, measured by ellipsometry in the layers that are shown in Figure 1. Experiments were carried out with adapted layer thicknesses (35/37/35/37 nm) and the same trend is obtained, with blisters appearing for the first 3 samples, and no blister for $R = 125$.

The optical properties of these four samples were measured by SE before annealing, and models have been made in order to fit them as a stack of a-Si$_2$O$_2$ layer with fixed optical properties – known by SE measurements from the SiO$_2$ optimization step – and an effective medium layer composed of a mixture of a-Si:H, voids and μc-Si:H on top of it (Bruggeman model [12]). Figure 2 shows the crystalline fraction of the silicon layer (fraction of the material being fitted as small-grain c-Si material), and the fitted thickness of the underlying oxide layer. The crystalline fraction increased when decreasing the silane flow rate. Surprisingly, the thickness of the oxide layer also seemed to decrease. In order to investigate this phenomenon, an XPS analysis was carried out on the samples deposited with $R = 50$ and $R = 125$ flow rate ratios.
3.2 Morphology of PECVD SiO\textsubscript{x} layer

To get insight on the possible evolution of the buried SiO\textsubscript{x} layer thickness, XPS depth profile analyses were realized on Batch 2 samples with a 30 nm thick silicon layer deposited with $R = \text{SiH}_4/\text{H}_2 = 50$ or $R = 125$ on top of the same oxide. The XPS Si and O concentration profiles obtained on the $R = 125$ sample are presented in Figure 3. Despite the high surface sensitivity of XPS, the detection of this ultra-thin SiO\textsubscript{x} layer is challenging since its 1–2 nm thickness is inferior to the escape depth of the emitted photoelectrons, requiring the optimization of the abrasion sequence not to cross over the layer.

This profile evidences three regions in agreement with the corresponding mc-Si:H, SiO\textsubscript{x} and c-Si stack structure. Contrarily to what was estimated by SE, for sample with SiH\textsubscript{4}/H\textsubscript{2} = 125, this profile shows that the oxide layer is still present in-between the c-Si and the mc-Si:H layer. An oxygen concentration bump is clearly visible, with a maximum of the oxygen content corresponding to the moment when the surface of the silicon oxide layer is reached. Indeed, since depth resolution is limited by the approximate 10 nm escape depth of the photoelectrons, the oxygen starts being detected before the interface is physically reached by sputtering and then starts decreasing afterward, while the Si content conversely rises.

Figure 4a shows the Si\textsubscript{2p} core levels measured at the surface of the buried oxide layer samples with a-Si:H ($R = 50$) and mc-Si ($R = 125$) as silicon layer. The reference spectrum obtained on a 1–2 nm of SiO\textsubscript{x} deposited by PECVD on a silicon wafer previously cleaned by HF is presented as a comparison. The intensity of the peak situated at 98.8 eV corresponding to the Si–Si bonds is the same for all the spectra. Since it is related to the collection of the photoelectrons emitted by the c-Si wafer underneath the oxide, and that the intensity decreases with the thickness of oxide on top of it, we can assess that there is no apparent etching of the SiO\textsubscript{x} layers. However, it can be seen that the Si–O contributions at higher binding energy are notably modified. The well-defined and roughly symmetric characteristic feature around 103.0 eV obtained for the reference PECVD SiO\textsubscript{x}, is modified indicating changes in the oxide network and the presence of a set of suboxides in relation with the tail like shape of the left part of the Si\textsubscript{2p} peak. This is an important piece of information since it

Fig. 1. Confocal images of the surface of SiO\textsubscript{x}(p) mc-Si:H samples after firing step (Batch 1) for different $R = \text{H}_2/\text{SiH}_4$ ratios.

Fig. 2. Evolution of crystalline fraction in the PECVD silicon layer, and fitted silicon oxide thickness with the SiH\textsubscript{4}/H\textsubscript{2} flow rate ratio on Batch 1 samples before firing step. Nominal SiO\textsubscript{x} thickness is 2.2 nm.

Fig. 3. Concentration profile of an as-deposited stack of c-Si:PECVD SiO\textsubscript{x}:PECVD (p) mc-Si:H (deposited with $R = 125$) from Batch 1.
means that in both studied conditions the deposition of the silicon layer changes significantly the oxide layer chemistry. Figure 4b shows the corresponding O1s photopeaks. It can be seen that the overall oxygen content of the encapsulated layers has significantly decreased, in agreement with the presence of suboxides. A possible explanation for the oxygen loss after silicon deposition may be an etching phenomenon by the hydrogen plasma operated during the \( (p) \) mc-Si:H deposition step. To sum up, the deposition of the silicon layer on top of our SiO\(_x\) layer grown by PECVD does not remove it nor reduce its thickness, but it modifies its chemistry, leading to oxygen removal, and changes in the oxidation degree. However, no major difference could be observed between the two samples studied (\( a\)-Si:H with \( R = 50 \) and \( \mu\)-c-Si with \( R = 125 \)), thus questioning the accuracy of the SE model for such thin buried layers.

### 3.3 Passivation of FZ DSP wafers

In Tables 2 and 3, we compare the minority carrier lifetime and implied Voc of symmetric samples for RF-PECVD and standard wet-chemical oxides (RCA2) as deposition methods for the oxide in the stack SiO\(_x\)\( (p) \) \( \mu\)-c-Si:SiN\(_x\). The \( (p) \) \( \mu\)-c-Si:H layer is deposited with a \( H_2/\text{SiH}_4 \) gas ratio of 125. The samples are as-deposited (no annealing step). It can be noticed that the passivation provided by the stack with the PECVD oxide is very low, contrarily to the one with wet-chemical oxide. This means that the process conditions used are not yet suited for passivating contacts. Although the lifetime of this sample was limited to 6\( \mu \)s, the one with the wet oxide with SiN\(_x\)H capping reached 909\( \mu \)s and 693 mV of implied Voc. The very large increase of the passivation with SiN\(_x\)H may be explained by the hydrogen in-diffusion from the SiN\(_x\)H layer to the c-Si/SiO\(_x\) interface. A photoluminescence image calibrated in lifetime of this sample is shown in Figure 5. Locally, the passivation achieved is significantly higher than the average 909\( \mu \)s, reaching values up to 1.3\( \mu \)s.

### Table 2. Lifetime of symmetric samples from Batches 2 and 3 on FZ wafers with wet SiO\(_x\)\( (p) \) \( \mu\)-c-Si before and after deposition of SiN\(_x\)H (no annealing step).

| SiO\(_x\) layer | Before SiN | After SiN |
|-----------------|------------|-----------|
| RF-PECVD        | 5 \( \mu \)s | 6 \( \mu \)s |
| Wet-chemical    | 67 \( \mu \)s | 909 \( \mu \)s |

### Table 3. Implied Voc of symmetric samples from Batches 2 and 3 on FZ wafers with wet SiO\(_x\)\( (p) \) \( \mu\)-c-Si before and after deposition of SiN\(_x\)H (no annealing step).

| SiO\(_x\) layer | Before SiN | After SiN |
|-----------------|------------|-----------|
| RF-PECVD        | 549 mV     | 558 mV    |
| Wet-chemical    | 619 mV     | 693 mV    |

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**Fig. 4.** (a) Si2p and (b) O1s spectra at the surface of the oxide layer (Batch 1).

**Fig. 5.** Photoluminescence image calibrated in lifetime of a \( p \)-type FZ DSP 1/4 wafer passivated by a wet SiO\(_x\)\( (p) \) \( \mu\)-c-Si/\( \text{SiN}_x\)H stack (Batch 3) with no annealing step.
The samples have been submitted to a firing step. The passivation was severely damaged (5 μs, 570 mV). This was an expected behavior in the case of no further hydrogenation step. Indeed, Lehmann et al. have recently shown that in the case of fired passivated contacts, a subsequent hydrogenation step is necessary in order to achieve high passivation quality [13]. Further investigations need to be carried out on the capping layer in order to hinder the hydrogen effusion during this step.

### 3.4 Cz vs. mono-cast textured wafers

For industrial integration, it is of major importance to deposit the passivating contacts on industrially relevant substrates, such as textured Cz or mono-cast silicon wafers. The passivation provided by passivated contacts with wet SiO$_2$ is also compared with the one provided by amorphous silicon (i) a-Si:H (n) a-Si:H stack as reported in Table 4. No difference is observed between mono-cast and Cz wafers as far as iVoc is concerned, meaning that the integration of passivating contacts on mono-cast wafers is definitely worth being investigated. It is broadly known that textured wafers are harder to passivate than chemically polished wafers, mostly because of increased surface area and a greater number of crystallographic imperfections [14]. As a consequence, the process still needs to be optimized to reduce the difference between passivating contacts and a-Si:H passivation, and the firing step needs to be carried out in order to allow the hydrogen contained in the SiN$_2$H layer to diffuse and passivate the interface.

### 4 Conclusion

In this study we have shown that it is possible to achieve a blister-free passivating contact structure after a single firing step by depositing doped μc-Si:H by PECVD without annealing on top of the oxide layer. It has been demonstrated that this deposition step leads to changes in the buried oxide stoichiometry, with evident oxygen loss, causing conversion into suboxide phases and probable oxide network modification. 693 mV of iVoc and 930 μs of lifetime were reached on a p-type FZ wafer with a simple stack of wet-SiO$_2$(p) μc-Si:H/SiN$_2$H in the as-deposited state, with no annealing step. The comparable passivation between Cz and Monocast wafers showed that it is of interest to keep studying the integration of passivating contacts on this kind of wafers.

| Passivation stack | Cz  | Mono-cast |
|-------------------|-----|-----------|
| SiO$_2$(p) μc-Si:H | 647 mV | 648 mV |
| (i,n) a-Si:H      | 673 mV | 670 mV |

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### Author contribution statement

Anatole Desthieux: main author and contributor to this work. Made all the experiments apart from the XPS measurements. Wrote the article. Jorge Posada: made all the chemistry related to the cleaning of the samples, and chemical oxides. Davina Messou: XPS measurements and analyses. Barbara Bazer-Bachi, Cédric Broussillou and Gilles Goar: industrial expertise, scientific feedback on the impact of TOPCon integration in industry. Processing and preparation of Monocast substrates. Muriel Boutteny: XPS expertise for data analysis. Pierre-Philippe Grand: expertise on silicon solar cell processes. Etienne Drahi: expertise on silicon solar cell processes. Project leader and a lot of feedbacks on characterization techniques, and other investigations. Pere Roca i Cabarrocas: expertise on plasma and vacuum processes. Helped analyse all the data, and mostly the spectroscopic ellipsometry measurements which lead to the XPS investigation.

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