Toward Valley-Coupled Spin Qubits

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The bid for scalable physical qubits has attracted many possible candidate platforms. In particular, spin-based qubits in solid-state form factors are attractive as they could potentially benefit from processes similar to those used for conventional semiconductor processing. However, material control is a significant challenge for solid-state spin qubits as residual spins from substrate, dielectric, electrodes, or contaminants from processing contribute to spin decoherence. In the recent decade, valleytronics has seen a revival due to the discovery of valley-coupled spins in monolayer transition metal dichalcogenides. Such valley-coupled spins are protected by inversion asymmetry and time reversal symmetry and are promising candidates for robust qubits. In this report, the progress toward building such qubits is presented. Following an introduction to the key attractions in fabricating such qubits, an up-to-date brief is provided for the status of each key step, highlighting advancements made and/or outstanding work to be done. This report concludes with a perspective on future development highlighting major remaining milestones toward scalable spin-valley qubits.

1. Introduction

There is an intense race to scale up the number of qubits in the quantum computer for quantum advantage (or supremacy) ostensibly to demonstrate finally that the quantum computer is able to solve certain problems deemed infeasible for its classical counterpart.[1,2] While it is possible to expediently build the support stack for demonstrating one or two qubits using "off-the-shelf" components and standard measurement electronics, scaling up to a full-fledged universally programmable quantum computer would require the ability to not only scale the qubits, but also the concomitant scalable development of the peripheral components for quantum state readout, manipulation and transfer.[1-6] Increasing from a few tens of qubits to beyond thousands of qubits would require rather radical rethinking of the overall architecture, material and process compatibility, and operational strategy. The tour de force to build a quantum computer typically involve significant investments at the national level (e.g., Australia, Canada, US, EU, UK).[7-12] or by industry juggernauts,[13] since the entire technology stack needed to drive a quantum computer is quite specific to the particular type of qubit used. To this end, a solid-state qubit platform that could be compatible with the existing Si microelectronics is often seen as beneficial and economical since the classical electronics portion is already a well-established technology with ready foundries.

Silicon-based qubit technologies appear to be an obvious choice and various groups have pursued this option using the spin states associated with single dopant atoms[6,14-16] or electrostatically gated quantum dots[1,17,18] as qubits in Si. The key challenges in these strategies are the atomically precise dopant placement,[19] access and control of single dopant states,[20] and the negligible spin–orbit interaction in Si perhaps makes it less efficient for electrical access and control.[21]

More recently, 2D materials have emerged as an alternative class of materials which could be potential solid-state hosts for spin-based qubits.[22-25] In particular, single-layer transition metal dichalcogenides (TMDCs) are 2D semiconductors with an intrinsic bandgap and strong spin–orbit coupling which promises fast spin operation times.[22,23,26] Significantly, the inherent inversion asymmetry in such TMDCs results in a unique spin-valley coupling which is expected to enhance the coherence lifetime of spin-valley states thus making the TMDC platform advantageous for robust qubits.[22,23,27] The single-layer TMDCs are readily transferrable[28] to a Si wafer or may be grown[29] directly onto a Si wafer, and the majority of TMDC-based devices have been fabricated on the Si wafer.[30,31] Significant research efforts are also underway to develop strategies for compatibility with Si CMOS technologies.[32,33] Hence, the 2D TMDC family is a very compelling alternative for building solid-state qubits. Various groups[31,34-40] have therefore invested efforts (see for example the facilities highlighted in Figure 1) to build electrostatically gated quantum dots in 2D TMDCs which could potentially lead to the development of qubits on the same platform. This report provides an update of the progress in this field. The key challenges in materials development will be highlighted. Following a brief review of potential device architectures proposed in the literature, two quantum dot fabrication strategies are presented together...
with discussions on the respective experimental progress. This report concludes with a summary of the key achievements to date, the challenges ahead, and provides an outlook for the field.

2. Materials Development: Challenges and Progress

2.1. Growth of High Quality TMDCs

TMDCs tend to occur naturally or grow preferentially in the 2H phase which is semiconducting and non-centrosymmetric in monolayer form. The lack of an in-plane inversion center, implies that the single-layer TMDCs intrinsically host inequivalent valleys at the K and K’ points of their hexagonal Brillouin Zone. In addition, the large spin–orbit coupling carried by the transition atoms combined with the time reversal symmetry, introduces an energy splitting of opposite signs at the K and K’ valleys, leading to a coupling of opposite spins to the K and K’ valleys. This unique “spin-locking” mechanism makes the valleys addressable via their incumbent spins and primes the single-layer TMDCs for spintronic and valleytronic applications, where the spin and valley degrees of freedom are explored for accelerating electronic computing and information processing.

Various synthesis approaches and strategies were explored to obtain high quality large-scale single- and few-layer TMDCs so to fully exploit their promising properties in various applications. TMDC layers with lateral size of few micrometers were first obtained from bulk single crystals by mechanical exfoliation. Despite the possibility of isolating high structural and electronic quality of small exfoliated TMDCs flakes, this technique is unlikely to be scalable for industrial production. To meet the wafer-scale fabrication requirements for industry adoption, different TMDC preparation methods are required. Among them, chemical vapor deposition (CVD) is a promising option, presently allowing to synthesize TMDCs triangular domains (10–100 μm) over a large (~cm² size) substrate area. In its simplest form, the CVD growth process consists of the co-evaporation of metal oxides and chalcogen precursors that lead to vapor phase reaction followed by the formation of a stable TMDC layer over a suitable substrate. Despite the considerable experimental and theoretical research efforts, there remains major hurdles toward achieving high quality as grown TMDC layers. Chemical defects (i.e., vacancies) and grain boundaries introduced during the growth process, for example, can affect both the TMDC optical and electronic properties of the TMDC film. As the nucleation density is a determinant of the film quality, various growth parameters can be adjusted to reduce the number of nucleation points, so as to achieve a continuous film made of a few larger single-crystal domains. The atomic layer of TMDC materials is also influenced by the nanoscale surface morphology, terminating atomic planes of substrates, as well as by lattice mismatching between the layer and the substrate. Recently, Lim et al. succeeded in synthesizing highly oriented wafer-scale MoS₂ using a single crystal sapphire substrate. The synthesized MoS₂ showed a highly ordered in-plane distribution with two main orientation (30° differences). This highly oriented MoS₂ film could also be easily removed from the sapphire substrate by simply immersing the substrate into water. These results show that growth on a single crystal substrate could be another key factor toward the CVD growth of large-area, oriented high-quality TMDCs.

2.2. TMDCs Quality Assessment by Optical and Electronic Properties

In current state-of-the-art valley physics experiments, specific valleys can be commonly targeted and selectively populated by controlling the helicity of the incident radiation on the material. This possibility of selective valley population was first demonstrated in monolayer MoS₂ through optical pumping of circularly polarized light and then confirmed for a wider class of single-layer TMDCs. The opposite spin polarization at K and K’ also results in unlike spins moving in opposite directions, perpendicular to an in-plane electric field (valley Hall effect) which has been reported for single-layer bilayer MoS₂ based transistors.

Optical techniques such as microscopy and Raman mapping are frequently the first line of quality checks carried out for assessing TMDC flake size or growth coverage, and layer numbers. For checking the TMDC specific band structure fingerprints, photoluminescence (PL), with linearly- or circularly-polarized light, is a fast-turnaround and noninvasive tool. A major issue related to the determination of valley related lifetimes is the inconsistencies in material quality used in optical based experimental studies of TMDCs. In this context, a wide range of life-times (from picoseconds to nanoseconds) was reported depending on the excitation species (exciton, trions, etc.). Analogous to other 2D materials, single-layer TMDCs are in fact difficult to isolate from the environment, and thus determining their intrinsic properties can be quite challenging. The physical properties of 2D materials are often affected by unknown substrate interactions originating for example by the presence of interface defects. Free-standing layers may also alter electronic and optical properties as a result of intrinsic structural relaxation such
Figure 1. Snapshots of the key facilities available at A*STAR (Singapore) for the growth and characterization of transition metal dichalcogenides (TMDC) materials.[27,83] a) The system shown is a 3 zone furnace for growing high quality TMDC layer by chemical vapor deposition (CVD) technique. The quality of as-grown TMDC materials can be typically assessed by optical microscopy and Raman spectroscopy, but the b) circular dichroic photoluminescence (CDPL) setup allows a rapid, noninvasive screening of valley polarization in 2D materials. c) TMDC’s electronic band structure, which ultimately determines the electrical and optical response of the layers, as well as their valley and spin polarization can also be independently detected by spin and angular resolved photoelectron spectroscopy (SARPES). CDPL and SARPES represent critical experimental tools to quantitatively rationalize the impact of supporting substrate and/or structural and chemical defect introduced by the sample preparation process on the electronic and optical properties of the TMDC layers utilized in the fabricated quantum devices. d) These devices can be investigated in dilution refrigerators enabling electrical transport measurements at temperatures down to 10 mK.

Finally, the temperature of the system can also directly control the valley polarization/depolarization in single-layer TMDCs via phonon activated processes. This is well exemplified in the recent work reported by Chellappan et al. (reproduced in Figure 2) showing the circular dichroic PL response of a single-layer WSe$_2$, at 8 and 300 K. In particular, this study observed a dramatic reduction of the valley polarization from 45% to 5% with increasing temperature. Therein, a detailed analysis of the emission line-width suggests that this change is caused by the strong exciton–phonon interactions which efficiently scatter the excitons into different excitonic states that are easily accessible due to the supply of excess photoexcitation energy.

As the unique spin-valley coupling is deemed a key advantage of using the TMDC for valleytronics and qubits development, the determination of this property via circular dichroic PL measurements would be an important first step in screening the TMDC materials before extensive device fabrication is carried out. Here, a dedicated circular dichroic PL system is useful to enable high-throughput screening for valley polarization in TMDC materials.[58] Figure 3 demonstrates an example of such a screening done for a single-layer WS$_2$ grown using CVD on a sapphire single-crystal substrate. The sample was mounted in a cryostat with an optical window and cooled to a minimum of $\approx$4 K using a closed cycle helium circulation. Circularly polarized 594 nm laser light was focused onto the sample, and the resulting PL collected with the same microscope objective and split into two beams of orthogonal polarization states. The separated beams were then coupled into a spectrometer via a bifurcated optical fiber to obtain the circular-dichroic PL spectra. Furthermore, the cryostat is mounted on an automated translation stage, which enables circular-dichroic PL of large-area samples up to several hundred micrometers in size to be mapped efficiently. This technique allows nondestructive screening of CVD-grown WS$_2$ samples for homogeneity and batch-to-batch variations, for...
example by comparison of the linewidths and degrees of circular polarization.

“Environmental” and temperature-related effects can also impact the charge transport properties of TMDC materials as indicated by the large variability of hole/electron mobility obtained even for a specific materials under same nominal experimental condition. A detailed understanding on how defects, substrate, temperature, and any other related fabrication and operational conditions affect the single-layer optoelectronic properties is critical for controlling charge and spin transport in TMDC based device and therefore to encode any information in their valley states. Despite recent progress in the field, a full picture of the above processes and their consequent impact is yet to be provided. Useful information on the electronic properties near the valley regions of single-layer TMDCs can also be provided by angular resolved photoemission spectroscopy (ARPES),
where monochromatic radiation is incident on a sample and electrons are consequently emitted into the vacuum.\cite{54,64} By analyzing the electron kinetic energy and angular distribution, this technique allows a direct determination of the electronic band structure along high symmetry directions of the Brillouin zone.\cite{54}

ARPES studies on the electronic properties of TMD layered materials typically involved small size (~micrometer) TMDC flakes obtained by direct exfoliation from single bulk crystal and then transferred onto a conductive substrate.\cite{65–69} Band structure investigations were therefore mainly conducted by micro-ARPES techniques at synchrotron radiation facilities where the reduced photon beam size (~micrometer) combined with microscopy techniques can be achieved to allow an accurate selection of the probed micrometer-size flakes. This technique was successfully employed in mapping the electronic band dispersion of TMDCs exfoliated layer of various thicknesses revealing, for example, the change of the valence band maximum position in the reciprocal space from K to \( \Gamma \) point and the increase of band branches near \( \Gamma \) when the layer thickness increases from single-layer to multilayer (Figure 4a,b).\cite{65–69}

Large-scale single-layer TMDCs (of up to \( \approx 100 \) µm of domain lateral size) were also grown by physical\cite{70,71} and chemical deposition\cite{72–75} processes on single crystal metallic substrate, the electrical conductivity of the substrate being required to avoid charging effects during photoemission in ARPES measurements. Via epitaxy, high quality and large crystal domains (of up to \( \approx 100 \) µm) can be achieved, thus allowing a detailed characterization by more conventional ARPES systems, where higher energy/momentum resolution limit can be generally achieved (Figure 4c).

Even though ARPES studies can yield important information on the interface-related effects on single-layer TMDCs electronic properties, the critical parameters governing the interfacial potential (i.e., layer-substrate distance, defects, etc.) are normally difficult to control experimentally. Progress is made in a recent ARPES study on the MoS\(_2\) (single-layer)/HOPG interface,\cite{30,76} where the interfacial potential landscape was tuned by temperature-induced change in the layer-substrate separation. These changes are reflected in the slight distortion of the valence band dispersion, i.e., change in the energy difference \( \Delta E_{\text{CK}} \) of the extrema (\( \Gamma \) and \( K \)) of the Brillouin zone (Figure 5a,b) pointing to the increased proximity of the MoS\(_2\) layer to the HOPG substrate as temperature is decreased from 295 to 11 K, in accord with dedicated band structure calculations as shown in Figure 5d. Note that the calculated trend in Figure 5c rules out in-plane contraction as the cause of the change in \( \Delta E_{\text{CK}} \) since it has an opposite trend.

The impact of interface tuning was evidenced by significant changes observed in the line shape of energy distribution curves (EDCs) at \( \Gamma \) point with temperature (Figure 5e), where the out of plane localization of the electronic wave function makes the charge dynamics more sensitive to change in the interfacial potential landscape (Figure 5f). In contrast, the EDC line shape at the K point is basically unaffected by temperature change (Figure 5e), a result favored by the strong in-plane localization of electronic state near the valley point (Figure 5f). The above results suggest that the charge and locked spin dynamics at the K valley is essentially protected from the local change in the interfacial potential landscape originating from the increased proximity to the substrate at lower temperatures. Such potential variations could arise, for example, from structural inhomogeneity in the
Figure 5. Angular resolved photoemission spectroscopy (ARPES) study of the single-layer MoS₂ on HOPG substrate. a,b) ARPES intensity plot (normalized to maximum) showing the VB dispersion of single-layer MoS₂ along ΓK at a) 295 K and b) 11 K. Dashed black curves in panel (a) denotes the calculated band dispersion for free-standing single-layer MoS₂. The energy separation between the band extrema at Γ and K point (ΔEΓK) is also indicated at both temperatures. c,d) Calculated ΔEΓK with varying lattice constant a in a free-standing single-layer and distance d from supporting substrate (single-layer graphite used, for computational efficiency). e) Energy Distribution Curves (EDCs) at Γ for 295 and 11 K (left panels) and at K point for 295 and 11 K (right panels). EDCs near VB local maximum were fitted by Voigt functions, (dashed curve with green shading). The extracted Lorentzian (wL) and Gaussian (wG) are reported in panels each panel. f) Schematic impact of substrate interaction and impurities/defects Coulomb potential on the single-layer MoS₂ electronic states near the local VB maximum at Γ and K. Calculated charge density plot reflects the wavefunction symmetry at different points of the Brillouin zone. Reproduced with permission. [76] Copyright 2019, American Physical Society.

TMDC/substrate interface resulting from the change in the layer substrate separation and/or presence of impurities. This demonstration of the “immunity”, of the valley locked spins to interfacial landscape may have crucial implications for hole transport in single-layer devices seeking to exploit valley pseudospins and the control thereof in TMDC based heterointerfaces.

By proper modifications of the electron detection scheme,[54] the ARPES technique can also be utilized to directly address the spin polarization of valley states in TMDCs. With respect to the electronic band studies, such spin-resolved ARPES (SARPES) measurements of TMDC materials are comparatively less reported, mainly as a consequence of the limited energy resolution of spin detector and ii) overlap between the signals of twin domains (relative rotation of 60°) by epitaxy on graphene. In particular, the latter effect results in a superimposition of the spin signal from the K and K' valley points of different domains and thus reduce the measured spin polarization value. Interestingly, a recent theoretical study suggested that the spin texture of the TMDCs could be probed by SARPES even in the inversion symmetric bulk crystals (termed “hidden” spin-polarization), as a result of the localization of two spin-degenerated valence band maxima on different layers of the unit cell.[82] The existence of spin-polarized electronic states was demonstrated by synchrotron based SARPES investigation on high quality 2H-WSe₂[79] and 2H-MoS₂ single crystal.[80] With the availability of larger TMDC films grown by CVD or other techniques (e.g., physical vapor deposition), laboratory-based SARPES system[83] become viable options for local laboratories to provide rapid feedback to the TMDC grower for the purpose of material optimization, instead of large synchrotron facilities. Using such a laboratory-based SARPES system,[83] the local...
("hidden") spin polarizations in WS$_2$ bulk layers were detected for the first time in a local laboratory (Figure 6).[84]

With the availability of the above tools for assessing the spins localized in valleys, it becomes possible now to address important materials development questions such as whether substrate effect, dielectric capping, TMDC defects, and impurities could be detrimental to the preservation of spin-valley coupling in TMDCs. Bussolotti et al.[76] addressed the substrate impact and found the K-valley hole dynamics in TMDC monolayers to be well-protected, while Moody et al.[61] found that certain species of Se-vacancy defects induced in WSe$_2$ by electron irradiation actually formed defect-bound exciton states with longer lifetimes indicating enhanced spin-valley coupling. These studies point to the tolerance of TMDCs to likely substrate interactions and material defects which are unavoidable in practical fabrication scenarios.

3. TMDC-Based Qubits

3.1. Theoretically Proposed Architectures

In semiconductor systems, it is possible to spatially confine charge carriers down to the few-electron regime in potential wells using electrostatic gates. The resulting devices, also known as quantum dots or single electron transistors, allow for individual control of single charge or spin.[85] In such systems, the spin states can form a qubit basis for quantum computation, as described in the original proposal by Loss and DiVincenzo in 1998.[86] The five criteria necessary for universal quantum computation are i) a scalable physical system with well-characterized qubits, ii) qubit initialization, iii) long decoherence times longer than gate operation times, iv) two-qubit operation, and v) qubit readout. Many of these five criteria have been largely fulfilled in studies of solid state quantum dot systems such as GaAs, silicon, graphene, Si/SiGe, semiconductor nanowires and carbon nanotubes etc.[85]

Electrostatically defined quantum dots can also be created in 2D TMDCs. As a class of 2D semiconductors, single (or mono) and few layers of TMDCs offer several interesting properties advantageous for creating qubits. These atomically thin semiconductors offer natural carrier confinement in one spatial dimension. The monolayers possess a sizeable direct bandgap of ≈1.5–2 eV in the optical range allowing electrostatic confinement and optical manipulation of carriers.[87] TMDCs also exhibit several isotopes with zero nuclear spin which minimizes hyperfine interactions with the electron spin. Isotopic purification in other material systems have already been proven to boost decoherence times which is advantageous for criterion (iii).[88] Furthermore, TMDCs possess an additional valley pseudospin that can be flexibly utilized as a valley qubit or be combined with the electron spin to form a spin-valley qubit. TMDCs also exhibit
very strong spin–orbit coupling, in contrast to other spin-valley systems such as graphene and carbon nanotubes, and thus offer the potential for fast gate operations on TMDC qubits.[23,24]

Several theoretical studies have explored the viability of TMDC qubits, including valley qubits, spin qubits, spin-valley qubits, and even impurity based qubits.[23–25,87,89–91] Figure 7 shows the schematics of theoretical proposals for a TMDC based a) valley qubit,[90] b) spin-valley qubit,[23] and c) impurity-assisted qubit.[25] A key advantage that these schemes offer is the ability to manipulate the qubits by fully electrical means which could provide a potentially less complex route for scale-up.

For the valley qubit,[90] the design in Figure 7a uses gate electrodes G1–G4 to create an external electrostatic potential in order to confine a single electron. The application of oscillatory voltages to opposite gate electrodes can modulate the electron confinement potential and in turn the electron wave function. These induce transitions of the electron between the valley states.

To exploit the spin-valley coupling in TMDCs, Kormányos et al. proposed the spin-valley qubit architecture in Figure 7b, using DFT calculations to support their analyses for WS2, MoSe2, and WSe2.[23] Their results show that in order to implement the spin-valley qubit in quantum dots the level spacing in the quantum dot should be larger than thermal energy. The mean level spacing in a quantum dot is given by:

\[ \Delta E = \frac{\pi \hbar^2}{2 m_{\text{eff}} A}, \]

where \( A \) is the area of the dot and \( m_{\text{eff}} \) is the effective mass. Based on this analysis, one expects relatively small quantum dots are necessary to ensure that energy level spacing in the quantum dot is larger than the thermal energy. For instance, in MoS2 with an \( m_{\text{eff}} = 0.7 m_e \) and a quantum dot radius \( r = 40 \) nm, \( \Delta E \approx 150 \) µeV.[14] Similarly, for WS2: \( m_{\text{eff}} = 0.35 m_e, r = 40 \) nm, and \( \Delta E \approx 270 \) µeV. For WSe2, \( m_{\text{eff}} = 0.4 m_e, r = 40 \) nm, and \( \Delta E \approx 240 \) µeV. Such level spacings can be adequately resolved in transport spectroscopy performed in dilution refrigerator with a base temperature of 10 mK (typical electron temperature \( T_e = 100 \) mK corresponding to \( k_B T_e = 8.6 \) µeV, where \( T_e = \) electron temperature).

In this respect, TMDCs with smaller effective masses, such as WS2 and WSe2, might be more advantageous compared to MoS2 and MoSe2. However, for the same effective magnetic field, the splitting between different valley states is significant larger for MoS2 compared to WS2, suggesting that MoX2 compounds are more suitable for spin and valley filtering. The authors conclude that the most realistic approach in terms of the choices for qubit states is to use the lowest Kramers pairs at around zero magnetic field as a spin-valley qubit. An external magnetic field can then be used to tune the energy splitting between these two states. This also means that the relaxation time of such spin-valley qubits will only be limited by the longer spin or valley relaxation time while the pure dephasing time will be limited by the shorter of the two. The exchange interaction can then be utilized to couple adjacent spin-valley qubits for operating two-qubit gates.

For the impurity-assisted qubit,[25] Széchenyi et al. show that a short-range impurity such as a vacancy, substitutional atom or adatom in a monolayer TMDC qubit can couple the basis states of the spin-valley qubit. This allows for resonant qubit control via electrically driven spin resonance with the help of an in-plane magnetic field. In the case of MoS2, an S-type impurity, e.g. a sulfur vacancy, the qubit Rabi frequencies were estimated to be...
3.2. Experimental Demonstrations of Electrostatically Gated Quantum Dots

Despite the availability of several architectural proposals, experimental realization has proven challenging due to issues such as contacting and gating monolayer TMDCs. Low material and interface quality and the lack of a robust contact strategy remain key hindrances for progress. Yet, encouraging efforts in the last few years have reported the fabrication of electrostatically gated TMDC quantum dots with varying degrees of device quality and tunability.\textsuperscript{[34–38,40]} They include single quantum dots in monolayer MoS\textsubscript{2},\textsuperscript{[34]} trilayer MoS\textsubscript{2},\textsuperscript{[40]} quasi-2D (>7 layers) WSe\textsubscript{2}, WS\textsubscript{2}, and few-layer InSe\textsubscript{2},\textsuperscript{[35,36,38]} and double quantum dots in monolayer MoS\textsubscript{2} and quasi-2D MoS\textsubscript{2}.\textsuperscript{[34,37]}

3.2.1. Fully Electrostatically Gated Quantum Dots

Since 2015, there has been several report toward the development of valleytronic devices\textsuperscript{[92]} and spin-valley qubits based on TMDCs.\textsuperscript{[34–40,54,83]} The strategy is to employ electrostatic gating to form quantum dots and realize a scalable TMDC based qubit platform, relying on the concepts espoused in the theoretical proposals of Figure 7. These reports demonstrate the ability to electrostatically gate a range of 2D TMDC materials to achieve carrier confinement. Figure 8 shows the schematic architectures of several electrostatically gated 2D TMDC quantum dot devices reported in literature.

While these works demonstrate the viability to electrostatically confine carriers in 2D TMDCs given sufficiently high-quality materials and suitable contacts and dielectrics, there is still no consensus on the best device architecture and fabrication process. Even in the choice of contacts to TMDCs, there is as yet no established standards for ready implementation. For few-layer InSe quantum dot, gated graphene was the material of choice for contacts. For monolayer and trilayer MoS\textsubscript{2}, gated graphene and Ti were utilized. For quasi-2D WS\textsubscript{2} and WSe\textsubscript{2}, Pd contacts were employed. Proper ohmic contacts are key for studying quantum transport in these systems but are difficult to achieve due to the work function mismatch with most metals and Fermi level pinning effects. However, recent works are increasingly pointing to ultraclean interface between metallic contacts and TMDCs as the critical factor in obtaining high quality ohmic contacts at low temperatures.\textsuperscript{[93,94]} The presence of adsorbed contaminants on TMDC surfaces can result in the creation of interface states leading to Fermi level pinning and large contact resistance. Ultraclean metal-TMDC interfaces can be achieved through ultrahigh vacuum metal evaporation or using hBN as an etch mask.\textsuperscript{[94,95]} In the latter approach, the hBN sheets are typically mechanically exfoliated and stacked onto the TMDC material in an inert environment, before etch windows are opened for evaporation in the hBN through selective plasma etching. However, ultrahigh vacuum evaporators are not common laboratory equipment, and hBN etch masks requiring assembly of mechanically exfoliated heterostructures is labor intensive and can be limited in scalability. Another promising approach is the use of indium metal deposited at low evaporation rate.\textsuperscript{[93]} The low evaporation rate reduces damage to the TMDC film via kinetic energy...
transformation between the metal atoms and the 2D TMDC. Cross-sectional annular dark-field scanning transmission electron microscopy reveal ultraclean interfaces between the In and TMDC film, while electrical measurements reveal record low contact resistances across a variety of TMDC films such as MoS$_2$, WS$_2$, WSe$_2$, and NbS$_2$. Consequently, the high-quality contacts formed by these different techniques based on ultraclean TMDC-contact interfaces allow for high carrier mobilities up to $\approx 10^4$ cm$^2$ V$^{-1}$ s$^{-1}$ on exfoliated samples and $\approx 10^2$ on CVD samples.

Aside from contacts, suitable dielectrics for local confinement electrostatic gates are also important. In electrostatically gated quantum dots, disorder limits device mobility and homogeneity, which prevents precise control over the confinement potential shape and tunnel couplings. These problems were observed in the quasi-2D MoS$_2$, WSe$_2$, and WS$_2$ quantum dots devices demonstrated using SiO$_2$ substrate and Al$_2$O$_3$ high-k dielectrics.$^{34-38}$ In a typical low temperature stability measurements of quantum dot devices, diamond-shaped regions of suppressed conductance, also known as Coulomb diamonds, are signatures of single-electron transport through a quantum dot. Measurements of the quasi-2D MoS$_2$, WSe$_2$, and WS$_2$ devices reveal the existence of overlapping Coulomb diamonds, suggesting that more than a single quantum dot is formed. The tunnel couplings were also found to be dominated by impurity defined traps. As a result of the disordered potential, it was not possible to reach the few-electron regime. Such impurity dominated transport were also recently observed by Lau et al. in studies of dual-gated few-layer exfoliated MoS$_2$ and WSe$_2$ as shown in Figure 9.$^{39}$ While transport through the TMDC film could be independently pinched off by split top gates, the current shows only a single current step in contrast to the expected multiple regularly spaced steps seen in higher quality hBN encapsulated devices.$^{34,35}$ Our experiments on top-gated CVD monolayer MoS$_2$ films with HfO$_2$ dielectric likewise show strong disorder-defined tunnel couplings with Coulomb oscillations that are dominated by a single gate (Figure 9e,f), similar to observations by Wang et al.$^{40}$ In contrast, a quantum dot formed by the top gates over uniform 2DEG should display diagonal resonances in a $V_L$ versus $V_R$ plot, where $V_{UR}$ refers to the top gate voltage applied to the left/right confinement gates.

Figure 9. Electrical measurements of exfoliated few-layer WSe$_2$ and chemical vapor deposition (CVD) grown single-layer MoS$_2$ devices. a) Current through the WSe$_2$ device with split top gates on an Al$_2$O$_3$ dielectric, showing independent gate control over current pinch off. b) A horizontal cut of (a) taken at $V_{MG} = -8.5$ V showing a distinct current step that is increasingly smeared out at higher temperatures. c) Multiple 1D cuts of (a) at different $V_{MG}$. SEM images of the d) exfoliated few-layer WSe$_2$ device measured in (a–c) and the e) CVD single-layer MoS$_2$ device with top confinement gates patterned on a HfO$_2$ dielectric. Scale bars are 500 nm. f) Current through the device in (e) as a function of $V_R$ and $V_L$. $V_{MG}$ and $V_{P}$ were set to $-15$ V. Multiple horizontal and vertical resonances are observed, indicating a disordered 2DEG. Reproduced with permission.$^{[39]}$ Copyright 2019, Springer Nature.
Disorder was found to be greatly reduced in devices where the TMDC films were prepared in an inert environment and encapsulated with hBN to form hBN/TMDC/hBN van der Waals heterostructures. The devices made using such heterostructures include monolayer and trilayer MoS$_2$, few-layer InSe$_2$. In these devices, measurements reveal clear diagonal resonances in the $V_L$ versus $V_D$ plots, implying a well-defined quantum dot located at the center of the gate-defined confinement.

### 3.2.2. Electrostatic Confinement in Nanoribbons and Nanotubes

While full electrostatic gating could simplify process requirements, the total number of top-gates required to achieve effective confinement could potentially increase architectural complexity and limit scaling. In order to satisfy the condition on quantum dot size to resolve quantum dot level spacing, alternative ways of creating strong confinement with few top-gates may be pursued. One way to achieve this is by physically shrinking one dimension of the 2D host materials to form nanowires. This can be done in two ways. The first is a top-down approach where a large TMDC flake is etched into a 1D nanoribbon. The second approach relies on the bottom up growth of 1D TMDC nanotubes or nanoribbons by chemical vapor deposition or other synthesis methods. Thereafter, electrostatic gates across the wires are used to confine the quantum dots.

The top-down approach requires a fabrication process which minimizes any degradation in the performance of the nanoribbon based devices. Nanoribbons based devices have been extensively studied in graphene at room temperature\[96\] as well as at low temperature.\[97,98\] Graphene being a semimetal, has been shown to exhibit measurable currents down to few tens of nanometers even at cryogenic temperatures.\[96,99–101\] However, shrinking the dimensions while maintaining a measurable current is quite challenging in semiconducting TMDC. First, the large Schottky barrier between metal and semiconducting TMDC which significantly suppresses device current at low temperatures. Second, it is quite challenging to resolve the excitation spectrum in a quantum dot.

Fabrication of nanoribbon field effect transistors in single-layer MoS$_2$ is achieved with existing lithographic processes. However, the requirement of physically shrinking the dimension of the host material down to few tens of nanometres as required to resolve the excitation spectrum in a quantum dot can be achieved with existing lithographic processes. However, the evaluation of their electrical properties at low temperature is crucial for implementing spin based qubits in nanoribbon and nanotubes based devices. Figure 11, reproduced from a recent report\[108\], shows the device characteristics of such a nanoribbon when cooled down from room temperature to low temperature (77 K). The authors report a shift in the threshold voltage with decrease in temperature as well as oscillatory current behavior at sufficiently low temperature (e.g., <4 K).\[104,108\] The current mobility before etching the TMDC flakes (Figure 11a, red trace). Typical mobility measured in TMDCs field effect transistors are $<10$ cm$^2$ V$^{-1}$ s$^{-1}$. After etching the TMDC flake into a nanoribbon, the mobility increased up to 50 cm$^2$ V$^{-1}$ s$^{-1}$ in single-layer MoS$_2$.\[101\] The origin of enhanced mobility is not so well understood and remains the subject of further studies.

The bottom-up approach involves synthesis of 1D TMDC nanotubes and nanoribbons. Growing single-layer TMDC nanotube has been quite challenging however, and several experiments have shown synthesis of multiwall nanotubes with diameter ranging from 10 nm to several micrometers (Figure 10b).\[105,106\] With nanotubes grown vertically in well defined array, scaling of such devices might be possible as shown in other material systems.\[105\] Field effect transistor fabricated from multiwall MoS$_2$ nanotubes exhibit mobility of 43 cm$^2$ V$^{-1}$ s$^{-1}$, steep subthreshold slope of 200 mV dec$^{-1}$, a current ON/OFF ratio of 10$^5$ as well as current density 1 µA µm$^{-1}$ comparable to the etched nanoribbons.\[106\]

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oscillations observed are attributed to Coulomb blockade due to single electron tunneling through a quantum dot as shown in inset of Figure 11b. The authors rule out other phenomenon such as conductance quantization\(^{109,110}\) and Fabry Perot\(^{111,112}\) interference due to the very small mean free path (200 nm) reported for encapsulated MoS\(_2\).\(^{113}\) These conclusions were further supported by the observation of diamond shaped domains in the 2D conductance (\(dI/dV\)) map as a function of source-drain and backgate voltage which are typical characteristics associated with Coulomb blockade (Figure 11b).

Unlike in nanoribbon devices, nanotubes devices with a direct comparison between room temperature and low temperature transport measurements have yet to be reported. However, Coulomb blockade in a multilayer MoS\(_2\) nanotube has been demonstrated (Figure 11c).\(^{105}\) Observed Coulomb blockade in both nanoribbon and nanotube devices are thus far due to accidental formation of quantum dots typically attributed to either external environment factors, intrinsic material system nuances, or combination of both. External environmental sources resulting in quantum dot originate from outside the material system and may include trap states (defects) in the SiO\(_2\) substrate,\(^{114,115}\) residues from the fabrication process,\(^{116}\) and dirt on the TMDC material.\(^{117}\) These sources result in charge localization in material system creating a quantum dot (Figure 12a) evidenced by Coulomb blockade at low temperature. Intrinsic sources resulting in quantum dot in both types of device may arise from the edge effects which includes microscopic roughness along the etched edges,\(^{117}\) molecule bound to the edge,\(^{118}\) or edge reconfiguration\(^{119}\) (Figure 12b). In this regard, nanotube-based devices may offer advantage over nanoribbon-based devices since they do not suffer from the edge states allowing to eliminate accidentally formed quantum dot due to abrupt edges. However, one must take caution that while nanotubes may be scalable in synthesis, they may not easily be scalable for aligned incorporation onto a substance to enable large-scale device processing. Hence, the use of nanotubes remains a controversial option despite some advantages.

Measures may be taken to minimize or eliminate the source of defects in nanoribbon and nanotube-based devices. Environmental defects may be largely reduced or eliminated by encapsulating the nanoribbon or nanotube in hBN. This could minimize not only the influence of substrate but also exposure to chemicals and solvents during the fabrication process. Intrinsic sources of defects may be mitigated by chemically functionalizing the channel to generate smooth edges especially in nanoribbon devices.\(^{119}\) Alternatively, if ALD deposition of a suitable high-k dielectric can passivate the unwanted edges states, this would also facilitate using local gates to electrostatically define quantum dot as well as to tune out the unwanted states. An example of a proposed nanoribbon-based device combining the measures to minimize the environmental and intrinsic defects along with local gates is shown in Figure 12c. This approach may potentially lead to device with electrostatically controlled quantum dot in nanoribbon/nanotube based devices similar to other material platforms.\(^{120,121}\)

Although the developments above demonstrate concerted efforts toward the promise of TMDC based qubits, 2D materials is a relatively recent field and TMDC based qubit development lags behind those based on more mature technological materials like Si and GaAs. Significant efforts currently underway to demonstrate a tunable gate defined quantum dot are a key step toward fulfilling the criterion (i), i.e., a scalable physical system with well characterized qubits. To move beyond exfoliated TMDs and van der Waals heterostructures which are limited in terms of scalability, new advances in material processing and device fabrication will be required in order to realize high quality scalable TMDC based qubits.

4. Summary, Challenges, and Perspectives

The expectation of quantum computing is likely at an unprecedented high, but the hardware required to realize a universal programmable quantum computer has not yet arrived. Although quantum computers with few to tens of qubits are now commercially available on the cloud, the lagging hardware development
signals that incumbent qubit technologies may be suffering from the scale-up bottleneck. Electrically controlled solid-state qubits, though faced with an initial high barrier of stringent materials engineering, have begun to come of age with the recent demonstration of few-qubit gates.\cite{6,16,122} It is envisaged that such solid-state platforms have great scale-up potential and would be strong contenders for the universal quantum computer. In this progress report, the focus has been on a recent entrant into the solid-state qubit arena based on a relatively new class of 2D semiconductors known as transition metal dichalcogenides. The motivation of spin-valley coupling in 2D TMDCs for building robust qubits is explained, accompanied by brief descriptions of proposed architectures in the literature. The key purpose however is to update on the state-of-the-art in the development of such valley-based spin qubits and reveal remaining challenges associated with the essential research and engineering of the materials, interfaces, and device fabrication.

While qubit gates based on 2D TMDCs have not yet been demonstrated, significant progress and understanding have been achieved in building quantum dot devices in 2D TMDCs, and quantum confinement and Coulomb blockade manifestations have now been observed by a few groups including the authors herein. Such observations allude to single electron control and are important precursors toward optimized quantum dots which could serve as qubits. Challenges remain with regards to showing the full viability of such qubits and we provide a nonexhaustive mention of some of them. For materials engineering, there is an urgent need for reliable large-area and high-quality 2D TMDCs, a reproducible ohmic contact strategy, an effective encapsulation of the 2D TMDC without destroying the desirable spin-valley coupling. An effective doping strategy, although less known or reported, is also likely required. From the quantum dot fabrication perspective, current lithographic techniques appear not to hinder the gate patterning required for quantum dots of a few tens of nanometers. However, it remains to be seen if the gating architectures, dielectric performance and control of crosstalk would be able to cope with the requirements for scale-up. These near term challenges are currently being addressed. In parallel, it is expected that developments for measuring the related coherence lifetimes and for qubit readout will follow as those would be critical determinants prior to qubit gate demonstrations. Although a latecomer to the solid-state qubit scene, the recent progress toward valley-coupled spins over a relative short period of time has been significant and encouraging, and this augurs well for the prospect of a solid-state spin-valley quantum computer.

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**Conflict of Interest**

The authors declare no conflict of interest.

**Keywords**

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