Portability for GPU-accelerated molecular docking applications for cloud and HPC: can portable compiler directives provide performance across all platforms?

Mathialakan Thavappiragasam*, Wael Elwasif*, Ada Sedova*,
*Oak Ridge National Laboratory, Oak Ridge, TN
Corresponding email: [thavappiragm, elwasifwr, sedovaaa]@ornl.gov

Abstract—High-throughput structure-based screening of drug-like molecules has become a common tool in biomedical research. Recently, acceleration with graphics processing units (GPUs) has provided a large performance boost for molecular docking programs. Both cloud and high-performance computing (HPC) resources have been used for large screens with molecular docking programs; while NVIDIA GPUs have dominated cloud and HPC resources, new vendors such as AMD and Intel are now entering the field, creating the problem of software portability across different GPUs. Ideally, software productivity could be maximized with portable programming models that are able to maintain high performance across architectures. While in many cases compiler directives have been used as an easy way to offload parallel regions of a CPU-based program to a GPU accelerator, they may also be an attractive programming model for providing portability across different GPU vendors, in which case the porting process may proceed in the reverse direction: from low-level, architecture-specific code to higher-level directive-based abstractions. MiniMDock is a new mini-application (miniapp) designed to capture the essential computational kernels found in molecular docking calculations, such as are used in pharmaceutical drug discovery efforts, in order to test different solutions for porting across GPU architectures. Here we extend MiniMDock to GPU offloading with OpenMP directives, and compare to performance of kernels using CUDA, and HIP on both NVIDIA and AMD GPUs, as well as across different compilers, exploring performance bottlenecks. We document this reverse-porting process, from highly optimized device code to a higher-level version using directives, compare code structure, and describe barriers that were overcome in this effort.

Index Terms—high-performance computing, molecular docking, computational biology, performance portability, OpenMP, GPU acceleration

Drug discovery is a lengthy process; computational efforts aid bench-top scientists search for possible small molecule therapeutics to test experimentally [4], [16]. Computational approaches are much faster and cheaper than experimental methods for filtering combinations of compounds and proteins, and can help to decrease the size of the chemical space that must be searched for lead compounds. Chemical synthesis companies today promise the ability to synthesize over a billion different molecules that could serve as lead compounds for optimization as drugs. By acting as a screening tool, computational molecular docking, an approach that simulates the three dimensional interactions of small molecules with a target protein [11], [16], [26], can reduce this space to a reasonable subset for experimental testing. Recently, high-throughput molecular docking has made use of large, parallel computing resources to perform extremely large screens, from millions to billions of small molecular ligands against proteins [6], [7].

This manuscript has been authored by UT-Battelle, LLC under Contract No. DE-AC05-00OR22725 with the U.S. Department of Energy. The United States Government retains and the publisher, by accepting the article for publication, acknowledges that the United States Government retains a non-exclusive, paid-up, irrecoverable, world-wide license to publish or reproduce the published form of this manuscript, or allow others to do so, for United States Government purposes. The Department of Energy will provide public access to these results of federally sponsored research in accordance with the DOE Public Access Plan (http://energy.gov/downloads/doe-public-access-plan).

1 https://catalog.ngc.nvidia.com/orgs/hpc/containers/autodock

Fig. 1. Scheme of the high-throughput GPU-accelerated molecular docking workflow. A large set of small molecule drug-like ligands (tens of thousands to billions) is rapidly screened using all available GPUs on a cloud or cluster resource to find an optimal position within a target protein active site.

As part of this work, acceleration with graphics processing units (GPUs) has been recently shown to provide a dramatic speedup for molecular docking programs [6], [11], [19]. Figure 1 illustrates the workflow for high-throughput structure-based screens of small molecule ligand databases with distributed GPU-accelerated molecular docking; NVIDIA provides the AutoDock-GPU program in its NGC Catalog of containerized software for servers. The high-throughput par-
Parallel deployment of docking on large set of heterogeneously-sized input ligands also presents a load balancing and dataflow execution optimization problem [24].

Computer architectures are changing rapidly. High-performance computing (HPC) has increasingly made use of heterogeneous multi-node systems with accelerators such as GPUs, and parallelization over multicore central processing units (CPUs), to provide optimal performance for applications in both leadership computing facilities and on cloud and data-center resources. Likewise, distributed cloud resources have also made extensive use of GPUs, especially for deep learning applications. Over the past decade, much effort has gone into programming GPUs using device-specific APIs and optimizations to maximize performance. Recent emergence of several GPU vendors competing for cloud and HPC users has upended this programming paradigm: optimizing and maintaining multiple versions of a program for each GPU vendor quickly becomes intractable. Therefore, portable programming solutions that can provide performance as close to optimized architecture-specific versions as possible are becoming more urgent needs for maintaining productivity in HPC [8], [17], [20], [21], [25].

Mini-applications (miniapps) are an essential tool used by the HPC community to test and optimize both performance and portability of important HPC-based programs. Miniapps aim to capture the key kernels used in larger applications to test program performance and portability, and to aid with transitions to these new systems [14], [25]. We have developed a miniapp which focuses on the computational kernels used to test program performance and portability, and to aid with the original implementation on CPUs was developed over several decades.

Multiple strategies and solutions exist today aimed at achieving performance portability between varying GPU architectures and across a wider set of parallel programming targets such as CPU-based threading. OpenCL was designed to provide parallel programming solutions for both CPU threads (and SIMD) and GPU accelerators [23], and is supported on NVIDIA GPUs, AMD GPUs, and FPGAs. The Kokkos middleware API [4] is facilitated by C++ template libraries and has been focused on portability across many parallel architectures as well, including CPU threads and GPUs, with support for AMD GPUs currently being provided through an interface with the HIP API [5].

In the following subsections, we provide further details on the molecular docking algorithm used here, the structure of the miniapp, and the use of directives for GPU programming.

### A. Design and Structure of MiniMDock

MiniMDock provides a testing application with an algorithmic pattern different from many other HPC miniapps [14]. The calculation, which is ultimately an optimization over a potential-energy surface described by a particle-grid interaction, is based on a genetic algorithm. While MiniMDock’s kernels are adapted from our work [11] porting the relatively new, GPU-accelerated AutoDock-GPU program [18], [19] from OpenCL to CUDA and applying modifications for high-throughput use in screening large numbers of small-molecule compounds (ligands) against a protein receptor, the algorithm and the original implementation on CPUs was developed over several decades.

OpenMP is a portable directive-based parallel programming API used ubiquitously in computational applications to program CPUs. Recently, compiler-directive-based parallelization offloaded to GPU devices has become possible with OpenMP target offload [15] using OpenMP 4.5/5.1 compilers. These directives would, in principle, be completely portable to any GPU regardless of vendor as long as a compiler backend exists targeting that device. The main challenges are then 1) for compiler developers to provide high-performing implementations capable of optimizing many types of code patterns and 2) for application developers to develop an optimized code structure that maximizes performance over multiple GPU devices. Here, we explore both of these challenges as we extend the miniMDock miniapp to OpenMP target offload, testing performance using both NVIDIA and AMD GPUs with several compilers per architecture, and compare to the performance of device-specific code which for both types of devices, makes use of low-level optimizations.

Briefly, the program represents the protein-ligand interaction with a reaction field for the protein portion, and with an particle representation for the ligand. The reaction field is described by a three-dimensional grid. The ligand atoms are represented by points in space that, along with the effects of hydrogen bonding, van der Waals forces, and desolvation...
effects. The algorithm is an energy minimization problem designed to find the most energetically favorable pose for the ligand within the protein’s binding pocket. The genetic algorithm uses a set of “crossover” events where features of each solution are mixed and interchanged across a “population” of possibilities, and individuals in the population are selected for the next iteration based on a numerical fitness score. The algorithm also incorporates a memetic component, wherein a local optimization is performed on a random sample of individuals of each generation, with the possibility to pass on fitness benefits obtained during the local search to the offspring during the crossover. The local optimization method is based on a random optimizer called the Solis-Wets algorithm [22]. The docking algorithm parallelizes well on GPUs, as each local optimization occurs independently from other members of the population. As an additional level of parallelism, several full optimizations each with a starting population of 150 individuals are computed simultaneously. The final solution is the best scoring pose out of all final solutions over all runs.

For the miniapp, several file writing tasks were removed from the program, to focus on the time spent in compute kernels. Three different inputs are provided for testing: a small, medium, and large task. These differ by the number of atoms in the ligand, which are used in the calculation of the interaction energy, the number of rotatable bonds, which together with translations of the ligand are the degrees of freedom for the optimization [23]. The small, medium, and large inputs have 21, 43, and 108 atoms, and 2, 15, and 31 rotatable bonds, respectively, and are shown in Figure 2.

Fig. 3. Software stack of the miniapp MiniMDock.

Figure 3 shows the software-stack layers in the MiniMDock miniapp. Here we focus on comparing the new OpenMP target module to the two versions that use the device specific APIs: CUDA for NVIDIA GPUs, and HIP for AMD GPUs. While HIP is designed to be portable to CUDA devices, it has been developed by AMD to provide optimized performance on AMD GPUs, so here we treat it as the most hardware-specific programming model for AMD GPUs.

B. Directives for GPU Offloading

OpenMP began as a CPU-threading programming model and began offering offloading to GPUs in version 4.0; it has continued to develop support for new features to date [15]. OpenACC was originally supported only by the PGI compiler, which was recently acquired by NVIDIA and now is distributed as part of NVIDIA HPC SDK (NVHPC). OpenMP offloading for NVIDIA GPUs is currently supported by the IBM XL compiler, LLVM, and NVHPC, while support for AMD GPUs has recently been provided by HPE Cray’s Programming environment, specifically the Cray Compiling Environment (CCE), and by AMD’s ROCm environment, in preparation for the Frontier supercomputer soon to be deployed at the Oak Ridge Leadership Computing Facility (OLCF).

While OpenACC was created for a “descriptive” programming style, wherein the compiler is responsible for most decisions about the way a parallel region is offloaded and distributed across the GPU, OpenMP was traditionally designed for a “prescriptive” model, where the application developer provides specific instructions for mapping parallel regions to the architecture. The prescriptive model thus can create code that may not be as performance portable across architectures. However, research efforts have focused on understanding how OpenMP can be used in a less architecture specific manner to improve portability [10]. Performance gaps between optimized CUDA code and directive-based versions have been narrowing in recent years, for both OpenACC and OpenMP [2], [3], [20], paving the way for more large applications to invest time in supporting a directive-based version or to chose a directive-based offloading strategy as the primary programming model for GPU support, such as was recently done for the widely-used materials program VASP [7] and the polarizable molecular dynamics program Tinker-HP [1].

II. RELATED WORK

Numerous studies have focused on directive-based offloading as a solution for performance portability over the past decade [3], [5], [9], [10], [12], [13], [21]. Multiple reports compared the OpenACC and OpenMP approaches and explored difference in usage and performance on GPUs compared to CUDA, and for CPU-based threading and accelerators like the Xeon Phi [2], [5], [10], [12], using simplified kernels and miniapps. Our miniapp contains examples of compute patterns different from other commonly used miniapps for HPC. Here we present one of the first studies, to our knowledge, of performance portability for directives across NVIDIA and AMD GPUs, using several compilers, with a new module of this miniapp. We also describe the reverse-porting of a highly optimized architecture-specific code to a directive-based code, and explore how this endeavor affects the final program and the performance, while providing guidance based on our experiences.

III. PORTING FROM OPTIMIZED CUDA

The starting point for the port to OpenMP target offload is a derivative of a hand-optimized version resulting from a collaboration between NVIDIA, Scripps Research and the Oak Ridge National Lab. The final product included warp-level primitives and the ability to utilize different numbers of threads per block to tune performance [11], [25]. Code restructuring

https://www.vasp.at/wiki/index.php/OpenACC_GPU_port_of_VASP
was therefore required for the OpenMP target version. This resulted in what may be a different final product from what may have come from either a de novo programming effort or from applying OpenMP offloading to a serial CPU version or one with CPU threading. One of the main differences between programming using OpenMP directives versus using architecture-specific code is that directives provide a more high-level set of instructions to the compiler; the compiler and the runtime have more flexibility as to how to perform the actual operation. Directives such as OpenMP allow the developer to express code and the control flow in the problem domain, as opposed to the explicit mapping of operations to specific threads; the decisions about how to assign computations to the hardware are made by the compiler and runtime. Lower-level APIs such as CUDA and HIP require the developer to express the problem in terms of the hardware. One of the key challenges in porting from architecture-specific code is that it is typically not possible to understand the difference between the programming models, and what can be expected in both: where the compiler has flexibility, and how parallel constructs such as synchronization and barriers must be implemented. This understanding can be crucial for correct program behavior. The lower-level code already lays out the parallelism, and to reduce re-writing, some decisions regarding design of these regions may potentially produce sub-optimal performance for the directive-based version. Another key difference between low-level massively-parallel programming models such as CUDA and HIP and the OpenMP programming model is the availability of a hierarchy of parallel constructs in OpenMP that is not available natively in CUDA. In CUDA, a kernel is executed by a single thread, and higher level constructs (e.g. block-level operations) need to be implemented in the kernel code itself, with no support directly from the CUDA programming model. The OpenMP teams construct maps naturally to block-level operations (as parallelism is implemented using a single thread per CUDA block or HIP workgroup). This difference manifests itself in the need to restructure a complex kernel where certain code regions are done by a single thread. In OpenMP, a sequence of parallel regions where all threads in the team are participating in a (typically) worksharing construct, using threadIdx, interleaved with code regions where team-level parallelism is in effect (and a single thread in the team is active), can help to facilitate this translation. In this section we demonstrate how the architecture-specific CUDA/HIP code was restructured to address these differences.

A. Removing architecture-specific code

For OpenMP code to be highly portable, it needs to avoid the use of architecture-specific APIs and low-level primitives that are not universally available. In CUDA and HIP, low-level primitives are used to perform operations that typically involve participation by threads in an entire block (these are typically referred to as warp-level primitives). Listings 1 and 2 show an example of the restructuring of a parallel region going from a mapping in CUDA or HIP to threads and blocks, followed by a warp-level reduction, to the use of OpenMP teams within a target region, and an inner parallel for reduction. In both versions, the structure cData is accessed to obtain the required information for each member of a population in the genetic algorithm, across the nruns independent replicas. In both versions, a flattened array is also used, although this was done to reduce code restructuring (and thus increase productivity), and not because this is required by OpenMP.

Listing 1. The sum_evals kernel in CUDA; HIP version is very similar.

```c
void gpu_sum_evals(uint32_t nruns, uint32_t work_pteam, ...)
{
#pragma omp target teams distribute
  num_teams(nruns) thread_limit(work_pteam)
for (int idx = 0; idx < nruns; idx++)
  {
    int sum_evals = 0;
    int* pEvauls_of_new_entities = cData.pEval_mems_of_pops[idx];
    for (int entity_counter = threadIdx.x;
        entity_counter < cData.dockpars._pop_size;
        entity_counter += blockDim.x)
      pEvauls_of_new_entities[entity_counter] += work;
  }
}
```

Listing 2. The sum_evals kernel in OpenMP target offloading.

```c
__global__ void gpu_sum_evals_kernel(...) {
  __shared__ int sSum_evals;
  int partsum_evals = 0;
in_s* pEvauls_of_new_entities = cData.pMem_evals_of_pops + blockIdx.x * cData.dockpars.pop_size;
for (int entity_counter = threadIdx.x;
    entity_counter < cData.dockpars.pop_size;
    entity_counter += blockDim.x)
  partsum_evals += pEvauls_of_new_entities[entity_counter];
}
```
parallelism in OpenMP, it is an explicit construct provided by the programming model. OpenMP provides support for high-level operations that involve threads in a parallel region through the reduction construct with many pre-defined reduction operators that are part of the OpenMP standard. The combined use of OpenMP reduction and OpenMP team-level parallel regions allows the desired operation to be expressed at a higher level, while leaving it up to the OpenMP compiler implementation to generate the most efficient inter-thread code that may involve the use of low level primitives for the target platform.

We implemented two different programmatic approaches for the OpenMP target offload and evaluated their performance portability features; in general, a good compiler-directive implementation should be relatively insensitive to variations in program structure and control flow, but in practice, this may not be the case. Therefore, our tests for performance portability also include this aspect.

B. Approach 1: Using “teams distribute” construct

In this approach (which was introduced above), we use the higher-level OpenMP constructs distribute and parallel for to automatically distribute the work over threads, without directly specifying thread-level work assignments. The outer-loop is distributed over teams using distribute construct and the inner-loop is shared over the threads using parallel for construct. However, extra effort is required for dealing with thread synchronization in this approach.

Listing 3. Thread synchronization in CUDA.

```c
__global__ void gpuKernel(parameters ...){
  __shared__ float3 A[N];
  float x = device_function(A, ...);
  compute(...);
  if (threadIdx.x == 0) {
    // Work for the master thread
  }
}
void use_gpukernel(uint32_t nblocks, uint32_t threads_pblock, parameters ...){
  gpu_kernel<<<nblocks, threads_pblock>>>(parameters ...);
}
```

Listing 4. Thread synchronization in OpenMP target offloading using Approach 1.

```c
void gpukernel(uint32_t nteams, uint32_t threads_pteam, parameters ...){
  #pragma omp target teams distribute num_teams(nteams)
  // thread_limit(threads_pteam)
  for (int i = 0; i < nthreads_per_team; i++){
    float3 struct A[N];
    #pragma omp parallel for
    for (int j = 0; j < work_pteam; j++){
      float x = device_function(A, ...);
    }
    // end of a team -- implicit barrier
  }
  // end for rotations: a rotation cycle
  #pragma omp parallel for reduction(+:energy)
  for (int atom_id = 0; atom_id < natoms; atom_id++){
    energy += calc_energys(atom_id, ...);
  }
  // team-level reduction
  #pragma omp parallel for reduction(+:energy)
  for (int atom_id = 0; atom_id < natoms; atom_id++){
    energy += calc_energys(atom_id, ...);
  }
  // end for rotation cycles
}
```

Thread synchronization ensures that no race conditions occur during write/read accesses and make the current (correct) values visible for each thread over the period of execution. Different programming models use different synchronization functions to synchronize runtime activities based on the architecture. CUDA uses the function __syncthreads() to place thread-level barriers and coordinate communication among threads in the same block. Similarly, memory-fence functions enforce the ordering of memory accesses, depending on the scope in which the ordering is enforced. The CUDA memory-fence function __threadfence() works beyond the thread block and ensures that there are no race condition for any threads on the device. OpenMP provides an omp barrier directive for thread synchronization, but unfortunately this directive cannot be used to synchronize across teams. However, an implicit barrier exists for a team construct when a omp parallel for directive is nested within the omp target team distribute directive.

Listings 3 and 4 show the differences between CUDA and OpenMP code for a region that requires a barrier and thread synchronization (line 4 in Listing 3). In order to apply the same barriers in OpenMP code, we use omp parallel for by introducing a for loop code segment as shown between lines 5 and 8 in Listing 4.

To implement device-function-level synchronization in OpenMP, we decomposed target functions into sets of subroutines to enable thread synchronization, and call these subroutines in a global function.
C. Approach 2: Using “teams” construct

Another approach which is closer to a direct conversion from the CUDA version, is currently more portable over the different compilers because it uses only the older and more fundamental features within OpenMP, but is less desirable in that it does not make use of the more human-readable, closer-to-the-algorithm high-level style that compiler directives provide, but requires a more hardware-level programming style. We used the **omp parallel** construct to manually specify shared and distributed work over threads similar to the CUDA version.

Listing 6 shows the equivalent OpenMP code, written in this approach, for the CUDA kernel shown in Listing 5. One benefit of this method is direct-handling of thread synchronization; we can use **pragma omp barrier** for thread synchronization directly.

```c
void gpu_kernel( uint32_t nteams, uint32_t threads_per_team, parameters ... )
#pragma omp target teams num(nteams) thread_limit(threads_per_team)
{
    float3_struct A[N]; // shared data
#pragma omp parallel
    {
        const int threadIdx = omp_get_thread_num();
        const int blockDim = omp_get_num_threads();
        const int gridDim = omp_get_num_teams();
        for (uint32_t tidx = blockDim; tidx < nteams; tidx += gridDim) // for teams
        {
            #pragma omp barrier
            compute( ... );
            f( threadIdx, x == 0 ) { // Work for the master thread
                }
        }
    } // end of parallel region
} // end of teams region
```

Listing 6. Thread synchronization in OpenMP target offloading using Approach 2.

Even with the choice to maintain as much code structure as possible from the original low-level architecture-specific code such as CUDA (which may potentially not result in the most optimal performance), there is a significant amount of work required to rewrite the program into a higher-level version appropriate for OpenMP offloading, including the careful restructuring of thread barriers and synchronization, of device functions, and of the deep copies of complex structures onto the device. This effort may be greater than the effort required for adding directive-based offload to an existing program written for the CPU. However, with the hope that the resulting version will be portable to multiple architectures, this time investment may be worthwhile if the performance of the portable version is close to that of the architecture-specific version. In the next section, we present performance results across compilers and GPU devices, both AMD and NVIDIA GPUs.

A. Summary of compilers and systems tested

We ran tests over four compilers and two GPU architectures (AMD and NVIDIA), using NVHPC for CUDA on NVIDIA, ROCm for HIP on AMD, and for OpenMP target offload, two compilers for NVIDIA GPUs: LLVM and NVHPC and three compilers for AMD GPUs: ROCm, OpenMP focused LLVM-Clang based OOMP, and HPE-Cray’s Cray Compiling Environment (CCE). Values presented are means over 10 replica runs for each test. For NVIDIA testing, we used the Summit supercomputer, and for AMD testing, we used the Spock system. Both systems are housed at the Oak Ridge Leadership Computing Facility (OLCF). Summit is an IBM system containing approximately 4,600 IBM Power System AC922 compute nodes. Each node contains two IBM POWER9 processors and 6 NVIDIA Tesla V100 accelerators. Each processor is connected via dual NVLINK connections capable of a 25GB/s transfer rate in each direction. Spock is an early-access testbed for the upcoming OLCF Exascale supercomputer, which contains 36 compute nodes each with a 64-core AMD EPYC 7662 CPU and four AMD MI100 GPUs. The CPU is connected to all GPUs via PCIe Gen4, with 32 GB/s transfer rate in each direction. On Summit we used the NVHPC 21.11 compiler as well as the LLVM 14.0 and 15.0 main branch development snapshots. On Spock we used the rocvm 4.5, aomp/14.0.11 and the CCE/12.0.1 compiler suites.

B. Results

The two OpenMP programming approaches introduced above will be denoted as labeled **omp_dist** for approach 1 (distribute construct-based automatic work sharing) and **omp_par**, for approach 2, (parallel construct-based manually specified work sharing).

In order to establish the baseline with which to determine the performance portability of the target offload version, a best-performing value must be established for the non-portable code. There may be several parameters that can be tuned to optimize code performance. For both the CUDA and HIP versions using V100 and MI100 GPUs, respectively, we noted that tuning a variable within the code designating the number of threads-per-block (in CUDA) or threads-per-workgroup (in HIP) affected the performance of the program, with the most significant effects being on performance with the large input. Figure displays these variations for CUDA on the NVIDIA V100 GPU and for HIP on the AMD MI100. The CUDA version is less sensitive to this parameter, and while the optimal value of threads-per-block provides a non-trivial improvement (up to 1.3x speedup) for CUDA, for HIP, performance is much more sensitive to the analogous...
threads-per-workgroup value, with larger values providing 2-3x speedup. Also notable is that for HIP, larger speedups from increasing this value above 32 were obtained for smaller loads (close to 3x for \( n_{	ext{runs}} = 10 \) compared to less than 2x for \( n_{	ext{runs}} = 100 \)).

Compiler-level optimizations are also possible for OpenMP GPU offload, and should be considered while assessing performance portability of a directive-based solution. Figure 5 shows the effects of the tuning the \( \text{thread}_{-}\text{limit} \) and maximum register count per thread parameters on performance with OpenMP-NVHPC using the omp_par control flow. Tuning the maximum register count from the default value, 254, to 60 shows significant performance improvements for each thread_limit; the effect grows from smaller thread_limit 32 at 35.58%, to 61.23% relative speedup for 128. The thread_limit parameter has a similar effect as the threads-per-block/workgroup parameter in the CUDA/HIP versions. The increase of \( \text{thread}_{-}\text{limit} \) value to 128 results in a significant improvement in performance, about 91.29% relative speedup compared to using the original setting of 32 for the best choice of maximum register count 60. Tuning both of these parameters brings the comparative slowdown with respect to the CUDA version on the V100 GPU down to 1.52× from the almost 4.51× for the large input. LLVM-clang gives the best performance for maximum register count 60 and \( \text{thread}_{-}\text{limit} \) 64. Tuning both parameters bring the comparative slowdown with respect to the CUDA version down to 2.47× from the almost 4.16× for the large input.

An additional optimizations, recently added to LLVM, are the use of link-time optimization (LTO)\[^{12}\] and no thread state which was used with the latest LLVM version 15. Figure 6 shows the cumulative performance improvements for LLVM-Clang and NVHPC compilers for the various compiler optimizations, including the use of LTO for LLVM, with the omp_par control flow. The LTO optimization helps bring LLVM closer to the optimized performance that NVHPC achieves. Additional LLVM optimizations for OpenMP offload on NVIDIA GPUs are currently in development. The effects of this optimization on the V100 are also shown in Figure 5 showing significant performance increase for both strategies, around 43.26% for omp_dist and 27.18% for omp_par, using thread_limit 64. LTO reduces slowdown from 2.92× to 1.98× and 2.47× to 1.80× for the two versions, respectively, with respect to the CUDA version.

\[^{12}\]https://github.com/llvm/llvm-project/commit/2f9ace9e9a5816684b3c19528bd4a3908b2b8ac0

---

**Fig. 4.** Effect of tuning threads-per-block parameter in CUDA on the NVIDIA V100 GPU (top panel) and threads-per-workgroup parameter in HIP on the AMD MI100 (bottom panel) for the large input. Shown is runtime in seconds for variations of this parameter and \( n_{	ext{runs}} \), using values of the threads per block parameter of 32, 64, 128 and 256.

**Fig. 5.** Effects of tuning \( \text{thread}_{-}\text{limit} \) and maximum register count on run time for the large input for OpenMP using NVHPC and LLVM compilers on NVIDIA V100 GPUs.

**Fig. 8.** The performance of the two OpenMP programmatic approaches, omp_dist (approach 1), and omp_par (approach 2), using LLVM-clang OpenMP target offload and the NVIDIA HPC SDK NVHPC OpenMP target offload, compared with the CUDA version, for \( n_{	ext{runs}} = 10 \). Here we used the optimal combination of compiler tuning strategies described above, in all cases. The CUDA-style manually-
Fig. 6. Effects of the tuning parameters on the performance of the program for the large input for OpenMP on NVIDIA V100 GPUs using LLVM and NVHPC compiler. Shown is runtime in seconds for variations of thread_limit.

Fig. 7. Effects of LLVM’s link time optimization feature for the large input for OpenMP using LLVM compiler on NVIDIA V100 GPUs, for both program strategies. Shown is runtime in seconds for variations of thread_limit.

specified work sharing strategy (omp_par, approach 2) consumes less time than the automatic version (omp_dist, approach 1) for both LLVM-clang and NVHPC compilers, but with a much smaller gap for LLVM. As mentioned above, reducing compiler sensitivity to program control flow with respect to performance is a desired approach to enable high-level programming APIs to maximize productivity.

For the LLVM omp_dist version, the maximum slowdown compared to CUDA is for the small input, at $1.6 \times$ slower, while for the medium and large inputs this declines to $1.8 \times$ and $1.67 \times$. The NVHPC omp_dist version follows the same pattern: the slowdown gets progressively better as the input size increases, from $4.89 \times$ for the small input, to $2.58 \times$ for the large one. A similar pattern is found for NVHPC with omp_par for NVHPC, but not for LLVM: for the small input it is $1.44 \times$ slower, while for the medium and large inputs this grows to $2.05 \times$ and $1.58 \times$. These results indicate that both implementations are sensitive to the program control flow, but that LLVM is less so.

Fig. 8. Performance of OpenMP target offload on NVIDIA V100 GPUs using NVHPC and LLVM compilers for the two different programmatic strategies, teams distribute (dist, approach 1) and teams with parallel for (par, approach 2). Indicated are times in seconds, and slowdown ($\times$) compared to the CUDA version for each input (small, medium, and large ligand): $n_{\text{runs}}=10$.

In either case, the performance can be considered significantly less than the CUDA version, indicating that true performance portability has not yet been achieved for NVIDIA GPUs despite trying different code structuring and compiler-level optimizations. Our initial speculation was that due to the code structure being originally designed for CUDA, these codes patterns were sub-optimal for OpenMP offloading, and that loop structures and data patterns would have to be rearranged. However, results on AMD GPUs seemed to contradict this conclusion.

Fig. 9. Performance of OpenMP target offload on AMD MI100 GPUs for $n_{\text{runs}}$ set to 10. Indicated are the exact times in seconds, and the slowdown ($\times$) compared to the HIP version for each input (small, medium, and large ligand).

Figure 9 shows performance on AMD MI100 GPUs, using HIP and the OpenMP offload versions of the miniaapp with the HPE-Cray CCE compiler and with AMD’s ROCm and AOMP compilers. Notable is a narrower gap in performance between HIP and the OpenMP version with the CCE compiler.
for the medium and large inputs. For the medium input, performance is nearly identical, which is an outstanding result. For the small and large input, the gap increases, resulting in a 1.55× and 1.47× slowdown, respectively, for omp_dist using CCE and 1.87× and 1.29× slowdown, respectively, for omp_par using CCE. For the best version of the large and medium input, this is within an acceptable range for a portable solution, while performance with the small input could be improved. The tuning of threads-per-workgroup with the CCE compiler did not result in any improvements (in fact, performance was slightly decreased) and gives the best performance at the default threads-per-workgroup value of 64. The AOMP compiler for the OpenMP version shows slightly better performance than CCE for the large input, and gives the minimum slowdown for that input, 1.22×. Performance of the ROCm compiler for the OpenMP version was considerably worse, and in contrast to all other compilers it shows better performance for omp_dist strategy than omp_par strategy in some cases. However, the performance of the AOMP compiler shows advances that will soon be incorporated into the ROCm compiler, and thus provides a more favorable view of the future ROCm stack. Figure 10 shows a summary of the best performing versions across the two GPUs (NVIDIA and AMD), with the CUDA, HIP, and OpenMP target offloading results for nruns set to 10 across the input sizes. We see that for the small input size, the HIP version actually gets better performance than CUDA. In the other cases, CUDA is best. OpenMP-LLVM on the NVIDIA GPU and OpenMP-CCE on the AMD GPU provide identical performance for the small input, but for the medium input size, OpenMP-CCE provides better performance than OpenMP-LLVM, and shows a similar to HIP with respect to CUDA. For HIP, there is a similar relative slowdown for the medium and large inputs. OpenMP-NVHPC and OpenMP-AOMP give better performance among the OpenMP compilers for the large input, with OpenMP-NVHPC on NVIDIA GPU outperforming OpenMP-AOMP on AMD.

We therefore see that a compiler-directive-based solution for a performance portable molecular docking program is becoming more of a viable reality. This implies the possibility of maintaining a single version of a program that can run on multiple GPU architectures, in a rapidly changing landscape for cloud servers and HPC clusters where several new vendors are entering the GPU arena. Our results also indicate that in general, compiler-based GPU offloading solutions for other types of programs may prove to be practical. However, it is clear that careful tuning of available compiler optimization parameters, choice of compiler, and even rearrangements in programmatic control flow may be necessary to achieve optimal performance with the directive approach. In principle, such considerations detract from productivity, which is one aim of performance portability efforts. Luckily, tools for autotuning performance are a focus of HPC research, and may provide assistance in reducing time spent tuning for compiler-based solutions.

V. DISCUSSION AND CONCLUSION

Here we tested the miniMDock molecular docking miniapp on NVIDIA and AMD GPUs using both native APIs for each device and new compiler-directive strategies. As a baseline, performance of the HIP version on AMD GPUs was slightly faster than the CUDA version on NVIDIA GPUs for our small input, and under 1.4× slower for the other two inputs, after tuning of thread-grouping parameters. We found that for miniMDock, it is possible to port an architecture-specific GPU-accelerated program to a more portable OpenMP offload version that can run on two different GPU architectures while avoiding a complete re-writing of the program, and achieve comparable performance to the original version– depending on the underlying decisions made by the compiler. Care must be taken to correctly translate thread synchronization and the placement of implicit barriers. The resulting program more closely reflects the scientific problem and less the architecture of the device, and can make use of multiple levels of nested parallelism explicitly, via constructs provided by OpenMP. We found that for the available compilers that support GPU offloading using OpenMP, truly comparable performance is not yet achieved for NVIDIA GPUs, with slowdowns compared to the CUDA version exceeding 1.5× for all input sizes tested, and despite tuning of several compiler optimization parameters and testing two different programmatic patterns. Performance of OpenMP offloading using the HPE-Cray CCE compiler resulted in a slowdown of 1.3× for the large input compared to HIP, and almost identical performance for the medium input, compared to the HIP version. This indicates that true performance portability using directives is becoming increasingly more realizable. It should be noted, however, that controls such as the thread limit and maximum register...
count do have a major impact on performance of higher-level programming models, as does the choice of compiler. Our results thus demonstrate the importance of the compiler back-ends for enabling truly performance-portable programs with directive-based offloading across different GPU vendors, and provide an optimistic outlook for performance-portable solutions as new GPU architectures enter the HPC and cloud ecosystems.

VI. ACKNOWLEDGMENT

This research used resources of the Oak Ridge Leadership Computing Facility, which is a DOE Office of Science User Facility supported under Contract DE-AC05-00OR22725. We thank Oscar Hernandez for valuable discussions.

REFERENCES

[1] Olivier Adjoua, Louis Lagardère, Luc-Henri Jolly, Arnaud Durocher, Thibaut Very, Isabelle Dupays, Zhi Wang, Théo Jaffrelot Inizan, Frédéric Célere, Pengyu Ren, et al. Tinker-hp: Accelerating molecular dynamics simulations of large complex systems with advanced point dipole polarizable force fields using gpus and multi-gpu systems. Journal of chemical theory and computation, 17(4):2034–2053, 2021.

[2] Swen Boehm, Swaroop Pophale, Verónica G Vergara Larrea, and Oscar Hernandez. Evaluating performance portability of accelerator programming models using spec accel 1.2 benchmarks. In International Conference on High Performance Computing, pages 711–723. Springer, 2018.

[3] Christopher Daley, Hadia Ahmed, Samuel Williams, and Nicholas Wright. A case study of porting hpgmg from cuda to openmp target offload. In International Workshop on OpenMP, pages 37–51. Springer, 2020.

[4] Jürgen Drews. Drug discovery: A historical perspective. Science, 287(5460):1960–1964, 2000.

[5] Rahul Kumar Gayatri, Charlene Yang, Thorsten Kurth, and Jack Deslippe. A case study for performance portability using openmp 4.5. In International Workshop on Accelerator Programming Using Directives, pages 75–95. Springer, 2018.

[6] Jens Glaser, Josh V Vermaas, David M Rogers, Jeff Larkin, Scott LeGrand, Swen Boehm, Matthew B Baker, Aaron Scheinberg, Andreas F Tillack, Mathialakan Thavapriragasam, et al. High-throughput virtual laboratory for drug discovery using massive datasets. The International Journal of High Performance Computing Applications, page 10943420211001565, 2021.

[7] Christoph Gorgulla, Andras Boeszoermenyi, Zi-Fu Wang, Patrick D Fischer, Paul W Coote, Krishna M Padmanabha Das, Yehor S Malets, Dmytro S Radchenko, Yuriy S Moroz, David A Scott, et al. An open-source drug discovery platform enables ultra-large virtual screens. Nature, 580(7805):663–668, 2020.

[8] Stephen Lien Harrell, Joy Kitson, Robert Bird, Simon John Pennycook, Jason Sewall, Douglas Jacobsen, David Neill Asanza, Abigail Hsu, Hector Carrillo Carrillo, Hessam Kim, et al. Effective performance portability. In 2018 IEEE/ACM International Workshop on Performance, Portability and Productivity in HPC (P3HPC), pages 24–36. IEEE, 2018.

[9] Abigail Hsu, David Neill Asanza, Joseph A Schoonover, Zach Jibben, Neil N Carlson, and Robert Robey. Performance portability challenges for fortran applications. In 2018 IEEE/ACM International Workshop on Performance, Portability and Productivity in HPC (P3HPC), pages 47–58. IEEE, 2018.

[10] Guido Juckeland, Oscar Hernandez, Azpith C Jacob, Daniel Neilson, Verónica G Vergara Larrea, Sandra Wienke, Alexander Boby, William C Brantley, Sunita Chandrasekaran, Mathew Colgrove, et al. From describing to prescribing parallelism: Translating the spec accel openmp suite to openmp target directives. In International Conference on High Performance Computing, pages 470–488. Springer, 2016.

[11] Scott LeGrand, Aaron Scheinberg, Andreas F Tillack, Mathialakan Thavapriragasam, Josh V Vermaas, Rupesh Agarwal, Jeff Larkin, Duncan Poole. Diogo Santos-Martins, Leonardo Solis-Vasquez, Andreas Koch, Stefano Forli, Oscar Hernandez, Jeremy C Smith, and Ada Sedova. GPU-Accelerated Drug Discovery with Docking on the Summit Supercomputer: Porting, Optimization, and Application to COVID-19 Research. In Proc. 11th ACM Int. Conf. Bioinformatics, Comput. Biol. Heal. Informatics, 2020.

[12] M Graham Lopez, Verónica Vergara Larrea, Wayne Joubert, Oscar Hernandez, Azzam Haidar, Stanimire Tomov, and Jack Dongarra. Towards achieving performance portability using directives for accelerators. In 2016 Third Workshop on Accelerator Programming Using Directives (WACCPD), pages 13–24. IEEE, 2016.

[13] Matt Martineau, James Price, Simon McIntosh-Smith, and Wayne Gaudin. Pragmatic performance portability with openmp 4. x. In International Workshop on OpenMP, pages 253–267. Springer, 2016.

[14] OE Bronson Messer, Ed D’Azevedo, Judy Hill, Wayne Joubert, Mark Merrill, and Christopher Zimmer. MiniApps derived from production HPC applications using multiple programming models. The International Journal of High Performance Computing Applications, 32(4):582–593, 2018.

[15] OpenMP. OpenMP 5.0 Reference Guide. https://www.openmp.org/wp-content/uploads/OpenMPRef-5.0-1119-01-TSK-web.pdf

[16] Nataraj S Pagadala, Khajamohiddin Syed, and Jack Tuszyński. Software for molecular docking: a review. Biophysical reviews, 9(2):91–102, 2017.

[17] Simon J Pennycook, Jason D Sewall, and Victor W Lee. Implications of a metric for performance portability. Future Generation Computer Systems, 92:947–958, 2019.

[18] Diogo Santos-Martins, Jerome Eberhardt, Giulia Bianco, Leonardo Solis-Vasquez, Francesca Alessandra Ambrosio, Andreas Koch, and Stefano Forli. D3R grand challenge 4: prospective pose prediction of BACE1 ligands with AutoDock-GPU. Journal of Computer-Aided Molecular Design, 33(12):1071–1081, 2019.

[19] Diogo Santos-Martins, Leonardo Solis-Vasquez, Andreas Koch, and Stefano Forli. Accelerating AutoDock4 with GPUs and gradient-based local search. ChemRxiv, 2019.

[20] Ada Sedova, John D Ehlen, Reuben Budiardja, Arnold Thrallington, and Jeremy C Smith. High-performance molecular dynamics simulation for biological and materials sciences: challenges of performance portability. In 2018 IEEE/ACM International Workshop on Performance, Portability and Productivity in HPC (P3HPC), pages 1–13. IEEE, 2018.

[21] Ada Sedova, Andreas F Tillack, and Arnold Thrallington. Using compiler directives for performance portability in scientific computing: kernels from molecular simulation. In International Workshop on Accelerator Programming Using Directives, pages 22–47. Springer, 2018.

[22] Francisco J Solis and Roger J-B Wets. Minimization by random search techniques. Mathematics of operations research, 6(1):19–30, 1981.

[23] John E. Stone, David Gohara, and Guochun Shi. Opencl: A parallel programming standard for heterogeneous computing systems. Computing in Science Engineering, 12(3):66–73, 2010.

[24] Mathialakan Thavapriragasam, Vivek Kale, Oscar Hernandez, and Ada Sedova. Addressing load imbalance in bioinformatics and biomedical applications: Efficient scheduling across multiple gpus. In 2021 IEEE International Conference on Bioinformatics and Biomedicine (BIBM), pages 1992–1999, 2021.

[25] Mathialakan Thavapriragasam, Aaron Scheinberg, Wael Elwasi, Oscar Hernandez, and Ada Sedova. Performance portability of molecular docking miniapp on leadership computing platforms. In 2020 IEEE/ACM International Workshop on Performance, Portability and Productivity in HPC (P3HPC), pages 36–44. IEEE, 2020.

[26] Josh Vincent Vermaas, Ada Sedova, Mathew B Baker, Swen Boehm, David M Rogers, Jeff Larkin, Jens Glaser, Nicholas W Coote, Krishna M Padmanabha Das, Yehor S Malets, Oscar Hernandez, and Jeremy C Smith. Supercomputing pipelines search for therapeutics against covid-19. Computing in Science & Engineering, 23(1):7–16, 2020.