SEVENTH FRAMEWORK PROGRAMME
Call FP7-ICT-2009-4  Objective ICT-2009.8.1
[FET Proactive 1: Concurrent Tera-device Computing]

Project acronym: EURETILE
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WP9 – Training, Exploitation and Dissemination
D9.3 – Third Report on Training, Exploitation and Dissemination

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**Third Report on Training, Exploitation and Dissemination**

**Table of Contents**

1. **CASTNESS’12 WORKSHOP ON COMPUTING ARCHITECTURES SOFTWARE TOOLS AND NANO-TECHNOLOGIES FOR NUMERICAL EMBEDDED AND SCALABLE SYSTEMS** ............................................. 3
   1.1 CASTNESS 2013 AGENDA ........................................................................................................... 3

2. **PAPERS - POSTERS - TECHNICAL PRESS – NEWSLETTERS** ................................................. 4
   2.1 ETHZ .................................................................................................................................................. 4
   2.2 RWTH ............................................................................................................................................... 7
   2.3 TIMA ............................................................................................................................................... 8
   2.4 INFN ............................................................................................................................................... 9

3. **PRESENTATIONS** ..................................................................................................................... 13
   3.1 ETHZ ............................................................................................................................................. 13
   3.2 RWTH ........................................................................................................................................... 15
   3.3 INFN ............................................................................................................................................ 17
   3.4 TARGET ...................................................................................................................................... 19
   3.5 TIMA ........................................................................................................................................... 20

4. **BOOKS** .................................................................................................................................. 20
   4.1 ETHZ ............................................................................................................................................. 20
   4.2 RWTH ........................................................................................................................................... 21
   4.3 TIMA ............................................................................................................................................ 21
   4.4 JOINT REPORTS ....................................................................................................................... 21
1. CASTNESS’13 WORKSHOP on Computing Architectures
Software tools and nano-Technologies for Numerical
Embedded and Scalable Systems

During 2013, an important WP9 action has been the contribution to the organization of the
CASTNESS’13 Workshop (Computer Architectures, Software tools and nano-Technologies
for Numerical and Embedded Scalable Systems).

Twenty speakers, representing the four Teradevice Computing projects (EURETILE,
TERAFLUX, TRAMS and SooS) presented their activities.

The CASTNESS’13 workshop has been held in Barcellona (28th June 2013).

This year, according to the TERACOMP plan, the organizational leadership has been
assumed by the TRAMS project (coordinator Prof. Antonio Rubio, Universitat Politècnica
de Catalunya (UPC)) and the workshop has been chaired by Antonio Rubio and Lutz
Schubert (Universität Ulm).

1.1 CASTNESS 2013 Agenda

9.00 Welcome and introduction
9.10 90 MINUTES SLOT FOR TRAMS PROJECT

• “Overview of the TRAMS project”, Antonio Rubio
• “Controlled Degradation Stochastic Resonance in Future Nanoarchitectures”, Nivard
  Aymerich
• ”New cells and reliability mechanisms for next generation memories”, Ramon Canal
• “Performance, power and reliability aware designs for tera-scale processors”, Intel
• “Dynamically Capturing Vulnerability Variation for Caches”, Intel

10.40 Coffee break

11.20 90 MINUTES SLOT FOR S(o)Os PROJECT

12.50 Lunch time

14.30 90 MINUTES SLOT FOR EURETILE PROJECT

• “The EURETILE parallel simulation environment”, Jan H. Weinstock, RWTH Aachen
• ”Distributed application layer: mapping dynamic applications on many-core systems”,
  Iuliana Bacivarov, ETH Zurich
• “Full Methodology of a Lightweight Task Migration in Embedded Multi-Tiled
  Architecture Using Task Code Replication”, Ashraf ELANTABLY, TIMA
• ”The EURETILE hardware experimental platform” - Andrea Biagioni, INFN - TARGET
• ”Fault and critical event awareness: a no single point of failure approach for
  distributed systems” - Laura Tosoratto, INFN-TARGET

16.00 90 MINUTES SLOT FOR TERAFLUX
17.30 CONCLUSIONS; ROUND TABLE and CLOSING

2. Papers - Posters - Technical Press – Newsletters
Here after the list updated to the reporting date.

2.1 ETHZ

2013

• H. Yang, I. Bacivarov, D. Rai, J.-J. Chen, and L. Thiele: Real-Time Worst-Case Temperature Analysis with Temperature-Dependent Parameters. Real-Time Systems. Volume 49, Issue 6, p. 730-762, November 2013.
• L. Schor, A. Tretter, T. Scherer and L. Thiele. Exploiting the Parallelism of Heterogeneous Systems using Dataflow Graphs on Top of OpenCL. Proc. IEEE Symposium on Embedded Systems for Real-time Multimedia (ESTIMedia), Montreal, Canada, p. 41-50, October 2013.
• L. Schor, H. Yang, I. Bacivarov and L. Thiele. Expandable Process Networks to Efficiently Specify and Explore Task, Data, and Pipeline Parallelism. Proc. International Conference on Compilers Architecture and Synthesis for Embedded Systems (CASES), Montreal, Canada, Oct. 2013.
• L. Schor, I. Bacivarov, H. Yang and L. Thiele. Efficient Worst-Case Temperature Evaluation for Thermal-Aware Assignment of Real-Time Applications on MPSoCs. Journal of Electronic Testing: Theory and Applications. Volume 29, Issue 4, p. 521-535, August 2013.
• L. Schor, D. Rai, H. Yang, I. Bacivarov and L. Thiele. Reliable and Efficient Execution of Multiple Streaming Applications on Intel's SCC Processor. Proc. Workshop on Runtime and Operating Systems for the Many-core Era (ROME), Aachen, Germany, August 2013.
• D. Rai, L. Schor, N. Stoimenov, I. Bacivarov and L. Thiele. Designing Applications with Predictable Runtime Characteristics for the Baremetal Intel SCC. Proc. Workshop on Runtime and Operating Systems for the Many-core Era (ROME), Aachen, Germany, August 2013.
• D. Rai, L. Schor, N. Stoimenov and L. Thiele. Distributed Stable States for Process Networks - Algorithm, Analysis, and Experiments on the Intel SCC. Proceedings of the 50th Annual Design Automation Conference, Austin, TX, USA, p. 167:1--167:10, June 2013.
• L. Schor, H. Yang, I. Bacivarov, D. Rai and L. Thiele. Distributed Application Layer - Adaptive Mapping of Multiple Streaming Applications onto On-Chip Many-Core Systems (Poster). Joint Switzerland-Korea Symposium 2013, May 2013.
• L. Thiele, L. Schor, I. Bacivarov, and H. Yang. Predictability for Timing and Temperature in Multiprocessor System-on-Chip Platforms. ACM Transactions in Embedded Computing Systems (TECS), Volume 12, Mar. 2013.
• P. Kumar, D. Chokshi, and L. Thiele. A Satisfiability Approach to Speed Assignment for Distributed Real-Time Systems. Proc. Design, Automation & Test in Europe Conference (DATE), Grenoble, France, Mar. 2013.
P. Kumar, and L. Thiele. Behavioural Composition: Constructively Built Server Algorithms. Proc. 5th Workshop on Compositional Theory and Technology for Real-Time Embedded Systems, San Juan, Puerto Rico, p. 9-12, Dec. 2012.

P. Kumar and L. Thiele. Quantifying the Effect of Rare Timing Events with Settling-Time and Overshoot. Proc. IEEE Real-Time Systems Symposium (RTSS), San Juan, Puerto Rico, p. 149-160, Dec. 2012.

S.-H. Kang, H. Yang, L. Schor, I. Bacivarov, S. Ha, and L. Thiele. Multi-Objective Mapping Optimization via Problem Decomposition for Many-Core Systems. Proc. IEEE Symposium on Embedded Systems for Real-Time Multimedia (ESTIMedia), Tampere, Finland, p. 28-37, Oct. 2012.

L. Schor, I. Bacivarov, D. Rai, H. Yang, S.-H. Kang, and L. Thiele. Scenario-Based Design Flow for Mapping Streaming Applications onto On-Chip Many-Core Systems. Proc. Intl' Conf. on Compilers Architecture and Synthesis for Embedded Systems (CASES), Tampere, Finland, p. 71-80, Oct. 2012.

D. Rai, H. Yang, I. Bacivarov, and L. Thiele. Power Agnostic Technique for Efficient Temperature Estimation of Multicore Embedded Systems. Proc. Intl' Conf. on Compilers Architecture and Synthesis for Embedded Systems (CASES), Tampere, Finland, p. 61-70, Oct. 2012.

L. Schor, H. Yang, I. Bacivarov, and L. Thiele. Thermal-Aware Task Assignment for Real-Time Applications on Multi-Core Systems. Proc. Intl' Symposium on Formal Methods for Components and Objects (FMCO) 2011, Turin, Italy, Volume 7542 of LNCS, p. 294-313, Oct. 2012.

L. Schor, H. Yang, I. Bacivarov, and L. Thiele. Worst-Case Temperature Analysis for Different Resource Models. IET Circuits, Devices & Systems, Volume 6, Issue 5, p. 297-307, Sep. 2012.

K. Huang, W. Haid, I. Bacivarov, M. Keller, L. Thiele. Embedding Formal Performance Analysis into the Design Cycle of MPSoCs for Real-time Streaming Applications. ACM Transactions in Embedded Computing Systems (TECS Journal), ACM, Volume 11, Issue 1, p. 8:1-8:23, 2012.

L. Schor, I. Bacivarov, H. Yang, and L. Thiele. Fast Worst-Case Peak Temperature Evaluation for Real-Time Applications on Multi-Core Systems. Proc. IEEE Latin American Test Workshop (LATW), Quito, Ecuador, p. 1-6, Apr. 2012.

L. Schor, I. Bacivarov, H. Yang, and L. Thiele. Worst-Case Temperature Guarantees for Real-Time Applications on Multi-Core Systems. Proc. IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), Proc. IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), Beijing, China, p. 87-96, Apr. 2012.

P. Kumar and L. Thiele. Timing Analysis on a Processor with Temperature-Controlled Speed Scaling. Proc. IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), Beijing, China, p. 77-86, Apr. 2012.

I. Bacivarov, I. Belaid, A. Biagioni, A. El Antably, N. Fournel, O. Frezza, J. Jovic, R. Leupers, F. Lo Cicero, A. Lonardo, L. Murillo, P.S. Paolucci, D. Rai, D. Rossetti, F. Rousseau, L. Schor, C. Schumacher, F. Simula, L. Thiele, L. Tosoratto, P. Vicini, H. Yang – “DAL: Programming Efficient and Fault-Tolerant Applications for Many-Core Systems” - Poster at HIPEAC12 - Jan 23-25, 2012 Paris, France
2011

- P. Kumar, J.-J. Chen, and L. Thiele. Demand Bound Server: Generalized Resource Reservation for Hard Real-Time Systems. Proc. Int'l Conference on Embedded Software (EMSOFT), pages 233-242, Oct. 2011.
- L. Schor, H. Yang, I. Bacivarov, and L. Thiele. Worst-Case Temperature Analysis for Different Resource Availabilities: A Case Study. Proc. Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), Lecture Notes on Computer Science (LNCS), Springer, Vol. 6951, pages 288-297, Sep. 2011.
- P. Kumar, J.-J. Chen, L. Thiele, A. Schranzhofer, and G. C. Buttazzo. Real-Time Analysis of Servers for General Job Arrivals. Proc. Intl. Conf. on Embedded and Real-Time Computing Systems and Applications (RTCSA), pages 251-258, Aug. 2011.
- L. Thiele, L. Schor, H. Yang, and I. Bacivarov. Thermal-Aware System Analysis and Software Synthesis for Embedded Multi-Processors. Proc. Design Automation Conference (DAC), pages 268-273, Jun. 2011.
- D. Rai, H. Yang, I. Bacivarov, JJ. Chen, L. Thiele. Worst-Case Temperature Analysis for Real-Time Systems. In Proceedings of Design, Automation and Test in Europe (DATE), Grenoble, France, March 2011.
- S. Perathoner, K. Lampka, L. Thiele. Composing Heterogeneous Components for System-wide Performance Analysis. In Proceedings of Design, Automation and Test in Europe (DATE), Grenoble, France, March 2011 (invited paper).
- I. Bacivarov, H. Yang, L. Schor, D. Rai, S. Jha, L. Thiele, Poster: Distributed Application Layer - Towards Efficient and Reliable Programming of Many-Tile Architectures. Design, Automation and Test in Europe (DATE) Friday Workshop, Grenoble, France, March 2011.
- K. Huang, L. Santinelli, JJ. Chen, L. Thiele, and G. C. Buttazzo. Applying Real-Time Interface and Calculus for Dynamic Power Management in Hard Real-Time Systems. Real-Time Systems Journal, Springer Netherlands, Vol. 47, No. 2, pages 163-193, Mar. 2011.

2010

- A. Schranzhofer, JJ. Chen, L. Thiele. Dynamic Power-Aware Mapping of Applications onto Heterogeneous MPSoC Platforms. IEEE Transactions on Industrial Informatics, IEEE, Vol. 6, No. 4, pages 692 -707, November, 2010.
2.2 RWTH

2013

- L. G. Murillo, S. Wawroschek, J. Castrillon, R. Leupers and G. Ascheid: "Automatic Detection of Concurrency Bugs through Event Ordering Constraints", in Proceedings of the Conference on Design, Automation & Test in Europe (DATE), 2014, Dresden, Germany (accepted for publication).
- J. H. Weinstock, C. Schumacher, R. Leupers, G. Ascheid and L. Tosoratto: "Time-Decoupled Parallel SystemC Simulation", in Proceedings of the Conference on Design, Automation & Test in Europe (DATE), 2014, Dresden, Germany (accepted for publication).
- C. Schumacher, J. H. Weinstock, R. Leupers, G. Ascheid, L. Tosoratto, A. Lonardo, D. Petras, A. Hoffmann: "legaSCi: Legacy SystemC Model Integration into Parallel Simulators", ACM Transactions on Embedded Computing Systems, Special Issue on Virtual Prototyping of Parallel and Embedded Systems. (to appear)
- J. H. Weinstock, C. Schumacher, R. Leupers and G. Ascheid: "SCandal: SystemC Analysis for Nondeterminism Anomalies", in Models, Methods, and Tools for Complex Chip Design (Haase, J., ed.) vol. 265 of Lecture Notes in Electrical Engineering. Springer, 2013.
- C. Schumacher, J. H. Weinstock, R. Leupers, G. Ascheid, L. Tosoratto, A. Lonardo, D. Petras, A. Hoffmann. "legaSCi: Legacy SystemC Model Integration into Parallel SystemC Simulators". 1st Workshop on Virtual Prototyping of Parallel and Embedded Systems (ViPES), 2013, Boston, USA.

2012

- C. Schumacher, J. H. Weinstock, R. Leupers and G. Ascheid. Cause and effect of nondeterministic behavior in sequential and parallel SystemC simulators. IEEE International High Level Design Validation and Test Workshop (HLDVT'12). Nov 2012, Huntington Beach (California-USA).
- C. Schumacher, J. H. Weinstock, R. Leupers and G. Ascheid: Scandal: SystemC Analysis for NonDeterminism Anomalies. Forum on Specification and Design Languages (FDL '12), Sep 2012, Vienna (Austria)
- L. G. Murillo, J. Harnath, R. Leupers and G. Ascheid. Scalable and Retargetable Debugger Architecture for Heterogeneous MPSoCs. System, Software, SoC and Silicon Debug Conference (S4D '12), Sep 2012, Vienna (Austria)
- L. G. Murillo, J. Eusse, J. Jovic, S. Yakoushkin, R. Leupers and G. Ascheid: Synchronization for Hybrid MPSoC Full-System Simulation. Design Automation Conference (DAC ‘12), Jun 2012, San Francisco (USA)
- R. Leupers, F. Schirrmeister, G. Martin, T. Kogel, R. Plyaskin, A. Herkersdorf and M. Vaupel. Virtual platforms: Breaking new grounds (More Real Value for Virtual Platforms). Design, Automation and Test in Europe (DATE ‘12), Mar 2012, Dresden (Germany)
J. Jovic, S. Yakoushkin, L. G. Murillo, J. Eusse, R. Leupers and G. Ascheid: Hybrid Simulation for Extensible Processor Cores. Design, Automation and Test in Europe (DATE '12), Mar 2012, Dresden (Germany)

2011

• S. Kraemer, R. Leupers, D. Petras, T. Philipp, A. Hoffmann. Checkpointing SystemC-Based Virtual Platforms. International Journal of Embedded and Real-Time Communication Systems (IJERTCS), vol. 2, no. 4, 2011
• L. G. Murillo, W. Zhou, J. Eusse, R. Leupers, G. Ascheid. Debugging Concurrent MPSoC Software with Bug Pattern Descriptions. System, Software, SoC and Silicon Debug Conference (S4D '11), Oct 2011, Munich (Germany)
• R. Leupers, G. Martin, N. Topham, L. Eeckhout, F. Schirrmeister, X. Chen: Virtual Manycore Platforms: Moving Towards 100+ Processor Cores. Design Automation & Test in Europe (DATE), Mar 2011, Grenoble (France)
• J. Castrillon, A. Shah, L. G. Murillo, R. Leupers, G. Ascheid. Backend for Virtual Platforms with Hardware Scheduler in the MAPS Framework. 2nd IEEE Latin America Symp. on Circuits and Systems, Feb 2011, Bogota (Colombia)
• S. Kraemer, Design and analysis of efficient MPSoC simulation techniques, dissertation, 2011, Aachen, Germany.

2010

• C. Schumacher, R. Leupers, D. Petras and A. Hoffmann. parSC: Synchronous Parallel SystemC Simulation on Multi-Core Host Architectures. In Proceedings of CODES/ISSS '10, October, 2010, Scottsdale, Arizona, USA.

2.3 TIMA

2013

• M. Jaber, A. Chagoya-Garzon, F. Rousseau, From System Model Formalization Towards Correct and Efficient HW/SW Design, DTIS Conference , March 2013, pp. 88 – 94, Abu Dabi, UAE.

2012

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2011

- A. Chagoya-Garzon, N. Poste, F. Rousseau. Semi-Automation of Configuration Files Generation for Heterogeneous Multi-Tile Systems, Computer Software and Application Conference (COMPSAC 2011), Munich, Germany, 18-21 July 2011.
- H. Chen, G. Godet-Bar, F. Rousseau, F. Petrot. Me3D: A Model-driven Methodology expediting Embedded Device Driver Development, International Symposium on Rapid System Prototyping (IEEE RSP 2011), pp. 171-177, May 2011, Karlshruhe, Germany.

2.4 INFN

2013

- R. Ammendola, M. Bernaschi, A. Biagioni, M. Bisson, M. Fatica, O. Frezza, F. Lo Cicero, A. Lonardo, E. Mastrostefano, P. S. Paolucci, D. Rossetti, F. Simula, L. Tosoratto, and P. Vicini, “GPU Techniques Applied to a Cluster Interconnect,” in Parallel and Distributed Processing Symposium Workshops PhD Forum (IPDPSW), 2013 IEEE 27th International, pp. 806–815, 2013.
- R. Ammendola, A. Biagioni, O. Frezza, A. Lonardo, F. Lo Cicero, P.S. Paolucci, D. Rossetti, F. Simula, L. Tosoratto and P. Vicini, “APEnet+ 34 Gbps data transmission system and custom transmission logic,” in JINST, Journal of Instrumentation, Proceedings of Topical Workshop on Electronics for Particle Physics (TWEPP) 2013, IOP Publishing, 2013.
- Roberto Ammendola, Andrea Biagioni, Ottonino Frezza, Francesca Lo Cicero, Alessandro Lonardo, Pier Stanislao Paolucci, Davide Rossetti, Francesco Simula, Laura Tosoratto, Piero Vicini, “Virtual-to-Physical Address Translation for an FPGA-based Interconnect with Host and GPU Remote DMA Capabilities.,” in Field-Programmable Technology (FPT), 2013 International Conference on, 2013.
- R. Ammendola, A. Biagioni, O. Frezza, F. Lo Cicero, A. Lonardo, P. S. Paolucci, D. Rossetti, F. Simula, L. Tosoratto and P. Vicini, “Analysis of performance
improvements for host and GPU interface of the APENet+ 3D Torus network”, Journal of Physics: Conference Series, Workshop on Advanced Computing & Analysis Techniques in Physics Research (ACAT) 2013, to be published

- R. Ammendola, A. Biagioni, L. Deri, M. Fiorini, O. Frezza, G. Lamanna, F. Lo Cicero, A. Lonardo, A. Messina, M. Sozzi, F. Pantaleo, P.S. Paolucci, D. Rossetti, F. Simula, L. Tosoratto and P. Vicini, “GPU for Real Time processing in HEP trigger systems”, Journal of Physics, Conference Series, Workshop on Advanced Computing & Analysis Techniques in Physics Research (ACAT) 2013, to be published

- Roberto Ammendola, Andrea Biagioni, Ottorino Frezza, Francesca Lo Cicero, Pier Stanislao Paolucci, Alessandro Lonardo, Davide Rossetti, Francesco Simula, Laura Tosoratto, Piero Vicini, “Architectural improvements and 28 nm FPGA implementation of the APEnet+ 3D Torus network for hybrid HPC systems”, Journal of Physics: Conference Series, International Conference on Computing in High Energy and Nuclear Physics (CHEP) 2013, to be published

- M. Bauce, A. Biagioni, R. Fantechi, M. Fiorini, S. Giagu, E. Graverini, G. Lamanna, A. Lonardo, A. Messina, F. Pantaleo, R. Piandani, M. Rescigno, F. Simula, M. Sozzi and P. Vicini “GPUs for real-time processing in HEP trigger systems”, Journal of Physics: Conference Series, International Conference on Computing in High Energy and Nuclear Physics (CHEP) 2013, to be published

- Roberto Ammendola, Andrea Biagioni, Riccardo Fantechi, Ottorino Frezza, Gianluca Lamanna, Francesca Lo Cicero, Alessandro Lonardo, Pier Stanislao Paolucci, Felice Pantaleo, Roberto Piandani, Luca Pontisso, Davide Rossetti, Francesco Simula, Marco Sozzi, Laura Tosoratto, Piero Vicini “NaNet: a low-latency NIC enabling GPU-based, real-time low level trigger systems”, Journal of Physics: Conference Series, International Conference on Computing in High Energy and Nuclear Physics (CHEP) 2013, to be published

- M.Bauce, A.Biagioni, R.Fantechi, M.Fiorini, S.Giagu, E.Graverini, G.Lamanna , A.Lonardo, A. Messina, F.Pantaleo; f , R.Piandani , M.Rescigno, F.Simula, M.Sozzi and P.Vicini, “GPU for Real Time processing in HEP trigger systems”, Proceedings of Science, European Physical Society Conference on High Energy Physics (EPS-HEP) 2013, to be published

- R. Ammendola, M. Bauce, A. Biagioni, R. Fantechi, M. Fiorini, S. Giagu, E. Graverini, G. Lamanna, A. Lonardo, A. Messina, F. Pantaleo, R. Piandani, M. Rescigno, F. Simula, M. Sozzi, P. Vicini “The GAP Project - GPU for realtime Applications in High Energy Physics and Medical Imaging”, IEEE Xplore, Nuclear Science Symposium and Medical Imaging Conference workshop (NSS/MIC) 2013, to be published.
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- Roberto Ammendola, Andrea Biagioni, Ottorino Frezza, Francesca Lo Cicero, Alessandro Lonardo, Pier Stanislao Paolucci, Davide Rossetti, Francesco Simula, Laura Tosoratto and Piero Vicini, "Design and implementation of a modular, low latency, fault-aware, FPGA-based Network Interface" IEEE Xplore, track on International Conference on Reconfigurable Computing and FPGAs (ReConFig) 2013, to be published.

- R. Ammendola, A. Biagioni, O. Frezza, G. Lamanna, A. Lonardo, F. Lo Cicero, P. S. Paolucci, F. Pantaleo, D. Rossetti, F. Simula, M. Sozzi, L. Tosoratto, P. Vicini "NaNet: a flexible and configurable low-latency NIC for real-time trigger systems based on GPUs", in *JINST*, Journal of Instrumentation, Proceedings of Topical Workshop on Electronics for Particle Physics (TWEPP) 2013, IOP Publishing, 2013, to be published

- Roberto Ammendola, Andrea Biagioni, Ottorino Frezza, Francesca Lo Cicero, Alessandro Lonardo, Pier Stanislao Paolucci, Davide Rossetti, Francesco Simula, Laura Tosoratto and Piero Vicini, “‘Mutual Watch-dog Networking’: Distributed Awareness of Faults and Critical Events in Petascale/Exascale systems,” *arXiv:1307.0433*, July 2013.

- Pier Stanislao Paolucci, Roberto Ammendola, Andrea Biagioni, Ottorino Frezza, Francesca Lo Cicero, Alessandro Lonardo, Elena Pastorelli, Francesco Simula, Laura Tosoratto and Piero Vicini, “Distributed simulation of polychronous and plastic spiking neural networks: strong and weak scaling of a representative mini-application benchmark executed on a small-scale commodity cluster” *arXiv:1310.8478*

- Roberto Ammendola, Andrea Biagioni, Ottorino Frezza, Werner Geurts, Gert Goossens, Francesca Lo Cicero, Alessandro Lonardo, Pier Stanislao Paolucci, Davide Rossetti, Francesco Simula, Laura Tosoratto, Piero Vicini "A heterogeneous many-core platform for experiments on scalable custom interconnects and management of fault and critical events, applied to many-process applications: Vol. II", 2012 technical report - arXiv preprint arXiv:1307.1270

**2012**

- Roberto Ammendola, Andrea Biagioni, Ottorino Frezza, Francesca Lo Cicero, Alessandro Lonardo, Pier Stanislao Paolucci, Davide Rossetti, Francesco Simula, Laura Tosoratto, Piero Vicini. APEnet+: a 3-D Torus network optimized for GPU-
based HPC Systems. New York, NY. Proceedings on 2012 J. Phys.: Conf. Ser. 396 042059 doi:10.1088/1742-6596/396/4/042059. (CHEP 2012).

- R. Ammendola, A. Biagioni, O. Frezza, A. Lonardo, F. Lo Cicero, P. S. Paolucci, D. Rossetti, A. Salamon, F. Simula, L. Tosoratto, P. Vicini. APEnet+: a 12x34 Gbps data transmission system with FPGAs embedded transceivers and QSFP+ modules. Poster at NSS-12 Nuclear Science Symposium. Anaheim, California, October 29 – November 3, 2012 -

- R Ammendola, A Biagioni, O Frezza, F Lo Cicero, A Lonardo, PS Paolucci, D Rossetti, F Simula, L Tosoratto, P Vicini. APEnet+: a 3D Torus network optimized for GPU-based HPC Systems. Journal of Physics: Conference Series - 396 042059 doi:10.1088/1742-6596/396/4/042059

- S. Amerio, R. Ammendola, A. Biagioni, D. Bastieri, D. Benjamin, O. Frezza, S. Gelain, W. Ketchum, Y. K. Kim, F. Lo Cicero, A. Lonardo, T. Liu, D. Lucchesi, P. S. Paolucci, S. Poprocki, D. Rossetti, F. Simula, L. Tosoratto, G. Urso, P. Vicini, and P. Wittich. Applications of GPUs to online track reconstruction in HEP experiments. - NSS-MIC 2012 Proceedings

- I. Bacivarov, I. Belaid, A. Biagioni, A. El Antably, N. Fournel, O. Frezza, W. Geurts, G. Goossens, J. Jovic, R. Leupers, F. Lo Cicero, A. Lonardo, L. Murillo, P. S. Paolucci, D. Rai, D. Rossetti, F. Rousseau, L. Schor, C. Schumacher, F. Simula, L. Thiele, L. Tosoratto, P. Vicini and H. Yang. EURETILE: Unified Networking Infrastructure for Embedded and HPC many-tile platforms. Poster at HIPEAC12. Jan 2012 Paris, France

- P. S. Paolucci. Brain Simulation Benchmark: Inspiring and benchmarking the scalability and fault-tolerance of future many-tile systems. Poster at HIPEAC12. Jan 2012 Paris, France.

2011

- Roberto Ammendola, Andrea Biagioni, Ottorino Frezza, Francesca Lo Cicero, Alessandro Lonardo, Pier Stanislao Paolucci, Davide Rossetti, Francesco Simula, Laura Tosoratto, Piero Vicini. QUonG: A GPU-based HPC System Dedicated to LQCD Computing. Application Accelerators in High-Performance Computing, Symposium on, pp. 113-122, 2011 Symposium on Application Accelerators in High-Performance Computing, (SAAHPC 2011)

- Roberto Ammendola, Andrea Biagioni, Ottorino Frezza, Francesca Lo Cicero, Alessandro Lonardo, Pier Stanislao Paolucci, Davide Rossetti, Francesco Simula, Laura Tosoratto and Piero Vicini. APEnet+ project status. - Proceedings of XXIX International Symposium on Lattice Field Theory (Lattice 2011). July 10-16, 2011. Squaw Valley, Lake Tahoe, CA

2010
3. Presentations

3.1 ETHZ 2013

- Iuliana Bacivarov, How model-based design simplifies the debugging of many-core systems. 1st International Workshop on Multicore Application Debugging (MAD 2013). Nov. 2013, Munich, Germany.
- Iuliana Bacivarov, Distributed Application Layer: mapping dynamic applications on many-core systems. CASTNESS’13. June 28th, 2013, Barcelona, Spain.
- Iuliana Bacivarov, Distributed Application Layer - Run-time mapping of streaming applications on heterogeneous many-core systems. DAC CHANGE - Computing in

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**2012**

- Iuliana Bacivarov, System-Level Thermal Aware Design of Real-Time Embedded Systems, Lecture at Design and Test Summer School 2012, Oct. 2012, Puebla, Mexico.
- Iuliana Bacivarov, Distributed Application Layer: Scenario-Based Design Flow for Mapping Streaming Applications onto On-Chip Many-Core Systems, Invited talk at Thales Paris, Aug. 2012, Paris, France.
- Iuliana Bacivarov, EU FP7 project EURETILE - EUropean REference TILed architecture Experiment (2010-2013): Distributed Application Layer, in Special Session on Ongoing EU Projects at ASAP 2012, Jul. 2012, Delft, Netherlands.
- Iuliana Bacivarov, Distributed Application Layer: Efficient Programming of Reliable Many-Core Systems, Invited talk at TU Delft, Jun. 2012, Delft, Netherlands.
- Iuliana Bacivarov, Distributed Application Layer: Mapping Dynamic Streaming Applications onto Many-Core Systems, Invited talk at Map2MPSoC/SCOPES, May 2012, Schloss Rheinfels, St. Goar, Germany.
- Iuliana Bacivarov, Management of Process Network Dynamism in the Distributed Application Layer, CASTNESS 2012, Jan. 2012, Paris, France.

**2011**

- Iuliana Bacivarov, Thermal-Aware Design of Real-Time Multi-Core Embedded Systems, Invited talk at Mapping Applications to MPSoCs, Jun. 2011.
- Iuliana Bacivarov, Temperature Predictability in Multi-Core Real-Time Systems, Invited talk at DAC Workshop on Multiprocessor System-on-Chip for Cyber Physical Systems: Programmability, Run-Time Support, and Hardware Platforms for High Performance Embedded Applications, Jun. 2011.
- Iuliana Bacivarov, Distributed Application Layer – Towards Seamless Programming of Many-Tile Architectures, CASTNESS 2011, 17 and 18 January 2011, Rome, Italy

**2010**

- Iuliana Bacivarov, Distributed Operation Layer: An Efficient and Predictable KPN-Based Design Flow, invited talk at Workshop on Compiler-Assisted System-On-
Chip Assembly 2010, in conjunction with Embedded Systems Week, Scottsdale, AZ, US, October 2010

- Iuliana Bacivarov, Efficient Execution of Kahn Process Networks on CELL BE, invited talk at Summer School on Models for Embedded Signal Processing Systems at Lorentz Center, Leiden, Netherlands, 30 Aug - 3 Sep 2010
- Iuliana Bacivarov, Distributed Operation Layer: A Practical Perspective, tutorial at Summer School on Models for Embedded Signal Processing Systems at Lorentz Center, Leiden, Netherlands, 30 Aug - 3 Sep 2010
- Iuliana Bacivarov, Distributed Operation Layer: Efficient Design Space Exploration of Scalable MPSoC, invited talk at Combinatorial Optimization for Embedded System Design workshop 2010 in conjunction with CPAIOR2010, 7th International Conference on Integration of Artificial Intelligence and Operations Research techniques in Constraint Programming, Bologna, Italy, June 2010
- Iuliana Bacivarov, invited talk at Efficient Execution of Kahn Process Networks on MPSoC, Mapping Applications to MPSoCs 2010, June 29-30, 2010, St. Goar, Germany.

3.2 RWTH

2013

- J. H. Weinstock. Time-decoupled Parallel SystemC Simulation. Joint RWTH/Synopsys Seminar. Dec 2013, Aachen, Germany.
- L. G. Murillo. Simulation-based Concurrent Software Debugging. Joint RWTH/Synopsys Seminar. Dec 2013, Aachen, Germany.
- L. G. Murillo. Automatic Exploration of SW Concurrency Bugs through Deterministic Behavior Control. 1st International Workshop on Multi-core Applications Debugging. November 2013, Munich, Germany.
- R. Leupers, L. G. Murillo. 1st International Workshop on Multi-core Applications Debugging (co-organization with TU Munich). November 2013, Munich, Germany.
- R. Leupers. Keynote at Sabanci Univ, Oct 2013, Istanbul, Turkey
- R. Leupers. Two new Use Cases for Virtual Platforms. 13th International Forum on Embedded MPSoC and Multicore (MPSoC’13). July 2013, Otsu, Japan
- J. H. Weinstock. The EURETILE Parallel Simulation Environment. CASTNESS’13, June 2013, Barcelona, Spain.
- L. G. Murillo. Simulation-based MPSoC Software Debugging. Joint RWTH/TU Munich Research Seminar, May 2013, Munich, Germany.
- R. Leupers. System-Level Design Technologies for Embedded Multicore Devices. HiPEAC workshop, Apr 2013, Sibiu, Romania
- R. Leupers. HiPEAC boot at DATE’13, Mar 2013, Grenoble, France
- R. Leupers. System-Level Design Technologies. Joint RWTH/Intel Lab seminar, Mar 2013, Aachen, Germany
- R. Leupers. Embedded Processor Design, Block lecture ALaRI, Jan-Feb 2013, University of Lugano, Lugano, Switzerland.
- R. Leupers (organizer). Programming Embedded Multiprocessor Systems: Application Code Mapping and Performance Estimation Technologies. Tutorial. 8th
Asia and South Pacific Design Automation Conference (ASP-DAC), Jan 2013. Yokohama, Japan
- R. Leupers. Joint RWTH/U Ghent Seminar, Jan 2013, Aachen, Germany
- R. Leupers. Embedded Processor Design, course. Thai-German Graduate School (TGGS), Jan 2013, Bangkok, Thailand

2012
- R. Leupers. Multicore Platform Design: Tackling a Grand Challenge in Embedded Computing. Keynote at the 15th Euromicro Conference on Digital System Design (DSD ’12), Sep 2012, Izmir, Turkey
- R. Leupers. Embedded Multicore Design Technologies: The Next Generation. Keynote at the IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP ’12), Jul 2012, Delft, The Netherlands
- R. Leupers. Design Technologies for Wireless Multiprocessor Systems-on-Chip, PhD course, University of Pisa, Jul 2012, Pisa, Italy
- Christoph Schumacher. Virtual EURETILE Platform: a Platform for Many-tiled Systems Simulation. Joint RWTH/TU Poznan Seminar, May 2012, Poznan, Poland
- R. Leupers (session chair). Workshop at DATE 2012: "Quo Vadis, Virtual Platforms? Challenges and Solutions for Today and Tomorrow". Mar 2012, Dresden, Germany
- R. Leupers (organized by). Special session at DATE 2012: "Virtual Platforms: Breaking New Grounds". Mar 2012, Dresden, Germany
- R. Leupers, H. Meyr. Embedded Processor Design, Block lecture ALaRI, Feb 2012, University of Lugano, Lugano, Switzerland
- R. Leupers. What's hot on Embedded System Design. Keynote at the Embedded Technology Conference (ETC ‘12), Feb 2012, San Pedro, Costa Rica
- Luis Murillo. Simulation-based software debugging in many-tile systems. CASTNESS 2012, January 26, 2012, Paris, France

2011
- Juan Eusse. Hybrid Simulation Technology for Extensible Cores and Full System Simulation of Complex MPSoCs. Presentation at HiPEAC Computing Systems Week, Nov 2011, Barcelona, Spain
- R. Leupers. SoC Design Research in the UMIC Excellence Cluster, Seminar, TU Berlin, Sep 2011, Berlin, Germany
- S. Yakoushkin. Advanced Simulation Techniques, Joint RWTH/TU Tampere Seminar, June 2011, Tampere, Finland
- R. Leupers (organized by). ICT Technology Transfer Workshop targeting Horizon 2020, Apr 2011, Brussels, Belgium
Project: **EURETILE** – European Reference Tiled Architecture Experiment
Grant Agreement no.: **247846**
Call: FP7-ICT-2009-4 Objective: FET - ICT-2009.8.1 Concurrent Tera-device Computing

- R. Leupers and G. Martin (organized by). Special session at DATE 2011: Virtual Manycore Platforms: Moving Towards 100+ Processor Cores, March 2011, Grenoble, France
- R. Leupers, H. Meyr. Embedded Processor Design, Block lecture ALaRI, Feb 2011, University of Lugano, Lugano, Switzerland
- Jovana Jovic, Simulation Challenges in the EURETILE Project, CASTNESS 2011, January 17-18, 2011, Rome, Italy

**2010**

- Christoph Schumacher, Virtual Platform Technologies for Multi-core Platforms, UMIC Day, 19 October, 2010, RWTH Aachen, Germany
- Rainer Leupers, HiPEAC Cluster Meeting (Design and Simulation Cluster), October 2010, Barcelona, Spain
- Rainer Leupers, Design Technologies for Wireless Systems-On-Chip, Huawei ESL Symposium, September 2010, Shenzhen, People's Republic of China
- Christoph Schumacher, Stefan Kraemer and Rainer Leupers, demonstration at DAC 2010 exhibition: parSC: parallel SystemC simulation, deterministic, accurate, fast, June 14-16, 2010, Anaheim, USA
- Rainer Leupers, MPSoC Design for Wireless Multimedia, Tutorial, MIXDES, June 2010, Wroclaw, Poland
- Stefan Kraemer, Advanced Simulation Techniques for Virtual Platforms, May 26, 2010, Imperial College London, London, United Kingdom
- Rainer Leupers, Cool MPSoC Design, ASCI Winter School on Embedded Systems, March 2010, Soesterburg, Netherlands
- Rainer Leupers, Embedded Processor Design and Implementation, course in MSc in Embedded Systems track at ALaRI Institute, March 1-4, 2010, University of Lugano, Switzerland

**3.3 INFN**

**2013**

- Roberto Ammendola - Virtual-to-Physical address translation for an FPGA-based interconnect with host and GPU remote DMA capabilities - 2013 International Conference on Field-Programmable Technology (ICFPT) 2013 - 9-11 dec - Kyoto, Japan
- Alessandro Lonardo - Building a Low-latency, Real-time, GPU-based Stream Processing System - GTC 2013 - March 20, 2013 - San Jose (California)
- Andrea Biagioni - The EURETILE hardware experimental platform - CASTNESS 2013 - 28 June 2013 - Barcelona, Spain

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Grant Agreement no.: **247846**

Call: FP7-ICT-2009-4 Objective: FET - ICT-2009.8.1 Concurrent Tera-device Computing

- Laura Tosoratto - Fault and Critical Event Awareness: a no-single-point-of-failure approach for distributed systems - CASTNESS 2013 - 28 June 2013 - Barcelona, Spain
- Andrea Biagioni - APEnet+ 34 Gbps Data Transmission System and Custom Transmission Logic - TWEPP 2013 - Sept 23-27, Perugia, Italy 2013
- Francesco Simula - From GPU-accelerated computing to GPU-accelerated data acquisition for physics experiments; the QUonG cluster, the APEnet+ network card and the APE project evolution - X Seminar on Software for Nuclear, Subnuclear and Applied Physics 2013 - Alghero, Italy
- Piero Vicini - Analysis of performance improvements for host and gpu interface of the APEnet+ 3D Torus network - XV International Workshop on Advanced Computing and Analysis Techniques in Physics (ACAT)- Beijing, China - May 2013
- Piero Vicini - GPU for Real Time processing in HEP trigger systems - XV International Workshop on Advanced Computing and Analysis Techniques in Physics (ACAT)- Beijing, China - May 2013
- Davide Rossetti - GPU Techniques Applied to a Cluster Interconnect - Parallel and Distributed Processing Symposium Workshops PhD Forum (IPDPSW) 2013 - Boston, MA.
- Alessandro Lonardo - Architectural improvements and 28 nm FPGA implementation of the APEnet+ 3D Torus network for hybrid HPC systems - International Conference on Computing in High Energy and Nuclear Physics (CHEP) 2013, 14-18 Oct 2013, Amsterdam, Nederlands.
- Ottorino Frezza - Design and implementation of a modular, low latency, fault-aware, FPGA-based Network Interface - ReConFig 2013 - Dec 2013 - Cancun, MEX.

2012

- R. Ammendola, apeNET+: a 3D toroidal network enabling petaFLOPS scale Lattice QCD simulations on commodity clusters, Lattice 2010, THE XXVIII INTERNATIONAL SYMPOSIUM ON LATTICE FIELD THEORY, Villasimius, Italy, June 2010
- D. Rossetti, Leveraging NVIDIA GPUDirect on APEnet+ 3D Torus Cluster Interconnect - GTC 2012 - GPU Technology Conference - May 2012 - San Jose, CA
- R. Ammendola, Comunicazioni Peer to Peer tra GPU remote con APEnet+ - E4 Workshop 2012 - Sept 2012 - Bologna, Italy
- D. Rossetti, Multi GPU simulations: status and perspectives - New Frontiers in Lattice Gauge Theory, GGI Firenze, Italy
- Davide Rossetti, Breadth First Search on APEnet+ - talk at IA^3 Workshop on Irregular Applications at SC12 conference, 10 Nov 2012
- Pier Stanislao Paolucci, Brain Inspired Many-Tile Experiment: second year overview of EURETILE, CASTNESS’12, 26 January 2012, Paris, France
- P. Vicini, Peer-to-peer GPGPU-APEnet+connectivity on HPC EURETILE platform, CASTNESS’12, 26 January 2012, Paris, France

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2011

- D. Rossetti, apeNET+ Project Status, Lattice 2010, THE XXIX INTERNATIONAL SYMPOSIUM ON LATTICE FIELD THEORY, Squaw Village, Lake Tahoe, CA, USA, July 2011
- P. Vicini, QUonG: A GPU-based HPC System Dedicated to LQCD Computing - Symposium on Application Accelerators in High-Performance Computing, Knoxville, TN - USA, July 2011
- D. Rossetti, Remote Direct Memory Access between NVIDIA GPUs with the APEnet 3D Torus Interconnect - SC11 - International Conference for High Performance Computing, Networking, Storage and Analysis - Seattle, WA
- Pier Stanislao Paolucci, EURETILE: Brain-Inspired many-tile SW/HW Experiment, CASTNESS 2011, 17 and 18 January 2011, Rome, Italy,
- P. Vicini, EURETILE: The HPC and Embedded Experimental HW Platform, CASTNESS 2011, 17 and 18 January 2011, Rome, Italy,
- P.S. Paolucci, Future Emerging Technologies High Performance Computing Projects, 17 Jan 2011, Lab. Naz. Legnaro, Italy

3.4 Target

2011

- G. Goossens, “Why Compilation Tools are the Catalyst for Multicore SoC Design”, Electronic Design and Solutions Fair, Yokohama (Japan), January 27-28, 2011.
- G. Goossens, “Why Compilation Tools are a Catalyst for Multicore SoC Design”, Third Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Design Automation and Test in Europe (DATE-2011), Grenoble (France), March 18, 2011.
- G. Goossens, P. Verbist, “Enabling the Design and Programming of Application-Specific Processors”, Sophia-Antipolis Micro-Electronics Conference (SAME-2011), Sophia-Antipolis (France), October 12-13, 2011.
- G. Goossens, “Building Multicore SoCs with Application-Specific Processors”, Electronic Design and Solutions Fair, Yokohama (Japan), November 16-18, 2011.
- P. Verbist, “Building software-programmable accelerators for ARM-based subsystems”, ARM Technical Symposium, Taipei and Hsinchu (Taiwan), November 17-18, 2011.
- G. Goossens, “Building Multicore SoCs with Application-Specific Processors”, Intl. Conf. on IP-Based SoC Design (IP-SoC-2011), Grenoble (France), December 7-8, 2011.
- G. Goossens, “Design Tools for Building Software-Programmable Accelerators in Multicore SoCs”, Workshop on Tools for Embedded System Design, Sint-Michielsgestel (Netherlands), December 13, 2011.
2010

- G. Goossens, "How ASIP Technology can Make your RTL Blocks More Flexible", Electronic Design and Solutions Fair, Yokohama (Japan), January 28-29, 2010.
- S. Cox, G. Goossens, "Hardware Accelerator Performance in a Programmable Context: Methodology and Case Study", Embedded Systems Conference, San Jose (CA, USA), April 26-29, 2010.
- G. Goossens, "Design of Programmable Accelerators for Multicore SoCs", First Artemis Technology Conference, Budapest (Hungary), June 29-30, 2010.
- W. Geurts, G. Goossens, "Ideas for the Design of an ASIP for LQCD", CASTNESS 2011, Rome (Italy), January 17-18, 2011.
- G. Goossens, E. Brockmeyer, W. Geurts, “Application-Specific Instruction-set Processors (ASIPs) and related design tools for tiled systems”, CASTNESS 2012, Paris (France), January 26, 2012.

3.5 TIMA

2013

- Ashraf Elantably, Frédéric Rousseau. Lightweight task migration in embedded multi-tiled architectures using task code replication, CASTNESS 2013, Barcelona, Spain.

2012

- Frédéric Rousseau, Requirements in Communication Synthesis for EURETILE: The use of Communication Path Formalization, CASTNESS 2012, January 26th, 2012, Paris, France
- Frédéric Rousseau, presentation of the EURETILE project in front of the Board of directors of the University Joseph Fourier, March 2011, Grenoble, France (in French)
- Frédéric Rousseau, Communication Synthesis in Low Level Software for Hierarchical Heterogeneous Systems, CASTNESS 2011, January 17-18, 2011, Rome, Italy

4. Books

4.1 ETHZ

- Book chapter: I. Bacivarov, W. Haid, K. Huang, L. Thiele. Methods and Tools for Mapping Process Networks onto Multi-Processor Systems-On-Chip. Handbook of Signal Processing Systems, Springer, pages 1007-1040, October, 2010.
4.2 RWTH

- Book chapter: J. H. Weinstock, C. Schumacher, R. Leupers and G. Ascheid: "SCandal: SystemC Analysis for Nondeterminism Anomalies", in Models, Methods, and Tools for Complex Chip Design (Haase, J., ed.) vol. 265 of Lecture Notes in Electrical Engineering. Springer, 2013.
- Book: T. Kempf, G. Ascheid, R. Leupers: Multiprocessor Systems on Chip: Design Space Exploration, Springer, Feb 2011, ISBN 978-1441981523
- Book: R. Leupers and O. Temam (Eds.), Processor and System-On-Chip Simulation, Springer, September 2010, ISBN 978-1441961747

4.3 TIMA

- Katalin Popovici, Frederic Rousseau, Ahmed A. Jerraya, Marilyn Wolf: Embedded Software Design and Programming of Multiprocessor System-on-Chip, Simulink and SystemC Case Studies, Springer, April 2010, ISBN 978-1-4419-5566-1
- Book chapter: Xavier Guerin, Frederic Petrot, Operating System Support for Applications targeting Heterogeneous Multi-Core System-on-Chip in the book Multi-Core Embedded Systems, CRC Press, Chapter 9, 24 pages, April 2010.

4.4 Joint reports

2013

- Paolucci, P.S., Bacivarov, I., Goossens, G., Leupers, R., Rousseau, F., Schumacher, C., Thiele, L., Vicini, P., "EURETILE 2010-2012 summary: first three years of activity of the European Reference Tiled Experiment.", (2013), arXiv:1305.1459 [cs.DC] , http://arxiv.org/abs/1305.1459 - then published as ISBN: 978-88-908488-0-3 (2013), http://dx.doi.org/10.12837/2013T01