Deterministic vs. Non Deterministic Finite Automata in Automata Processing

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Abstract—Linear-time pattern matching engines have seen promising results using Finite Automata (FA) as their computation model. Among different FA variants, deterministic (DFA) and non-deterministic (NFA) are the most commonly used computation models for FA-based pattern matching engines. Moreover, NFA is the prevalent model in pattern matching engines on spatial architectures. The reasons are: i) DFA size, as in #states, can be exponential compared to equivalent NFA, ii) DFA cannot exploit the massive parallelism available on spatial architectures. This paper performs an empirical study on the #state of minimized DFA and optimized NFA across a diverse set of real-world benchmarks and shows that if distinct DFAs are generated for distinct patterns, #states of minimized DFA are typically equal to their equivalent optimized NFA. However, NFA is more robust in maintaining the low #states for some benchmarks. Thus, the choice of NFA vs. DFA for spatial architecture is less important than the need to generate distinct DFAs for each pattern and support these distinct DFAs’ parallel processing. Finally, this paper presents a throughput study for von Neumann’s architecture-based (CPU) vs. spatial architecture-based (FPGA) automata processing engines. The study shows that, based on the workload, neither CPU-based automata processing engine nor FPGA-based automata processing engine is the clear winner. If #patterns matched per workload increases, the CPU-based automata processing engine’s throughput decreases. On the other hand, the FPGA-based automata processing engine lacks the memory spilling option; hence, it fails to accommodate an entire automata if it does not fit into FPGA’s logic fabric. In the best-case scenario, the CPU has a 4.5x speedup over the FPGA, while for some benchmarks, the FPGA has a 32,530x speedup over the CPU.

I. INTRODUCTION

Pattern matching is essential in many applications, including genomics, virus detection, network intrusion detection, and machine learning techniques such as random forest. Most of these applications are latency-sensitive. If the pattern matching rate is not fast enough, it acts as a performance bottleneck for those applications. Finite Automata (FA) have proven to be a great computation model for linear time pattern matching \[1\]–\[5\]. For example, Schulz et al. used FA to accelerate the pattern matching for genomics applications \[6\]. On the other hand, network devices such as the Cisco family of security appliances and networking software such as Snort \[7\] use regular expressions to represent safe payload patterns; prior works have used FA to accelerate regexes \[1\]–\[2\].

FA has different variants. The most commonly used FA variants in pattern matching engines are 1. Deterministic Finite Automata (DFA) and 2. Non-deterministic Finite Automata (NFA). Even though both of the variants are functionally equivalent, their structure (state count & transition) differs \[8\]. As a result, while designing an FA-based pattern matching engine, the underlying hardware architecture influences the selection between NFA and DFA. NFA is less preferred for von Neumann architecture because the possibility of multiple active states leads to multiple random memory lookups, and high memory latency is a performance bottleneck in von Neumann’s architecture \[9\]. Micron’s Automata Processor \[10\] and spatial architectures, such as Field Programmable Gate Arrays (FPGA), offer workarounds to hide the high memory latency. For these architectures, NFA is a popular choice over DFA \[2\]–\[5\]–\[11\] for several reasons. The crucial one is if an NFA has \(n\) states, its equivalent DFA can have \(2^n\) states \[8\]–\[12\]. For instance, Yu et al. \[13\] stated that 20% of the Snort \[7\] DFAs suffer from exponential state growth relative to the corresponding NFAs. Moreover, prior works show that generating one DFA from a set of patterns could result in an enormous time and space overhead \[13\]–\[14\].

There are algorithms \[15\]–\[16\] to generate minimized DFAs for which state count is smaller than the expected exponential growth (although exponential growth remains a worst-case for arbitrary automata). Tabakov et al. \[17\] performed a study on synthetic automata and illustrated that based on the automata structure, DFA states exhibit a growth rate of the order polynomial to sub-exponential compared to the NFA, and in some cases, minimized DFAs have a smaller state count than the equivalent non-optimized NFA. Motivated by their study, this paper fills a very important gap in automata processing work. Our paper demonstrates the state count analysis of the minimized DFA and its equivalent optimized NFA using a broad set of real-world benchmarks. The analysis shows that for the real-world benchmarks, the DFA state count exhibits linear or polynomial growth. Therefore, DFAs can be considered a viable alternative to any FA-based pattern matching engine that uses NFA as the computation model. Please note that unlike prior work \[17\], NFAs used in this analysis are optimized using a heuristics-based approach.

Another reason for choosing NFA over DFA while designing FA-based pattern matching engines on FPGAs is that NFAs may activate multiple states per symbol cycle, which exploits FPGAs’ massive parallelism \[2\]–\[11\]–\[18\]–\[19\]. However, this paper shows that DFAs can also exploit the parallel architecture of the FPGAs if, instead of creating a single large DFA for all the patterns of an application, separate DFAs are generated for distinct patterns, and these DFAs are processed
in parallel (section IV).

Finally, this paper presents another interesting finding: the state-of-the-art CPU-based automata processing engine, Hyperscan [20] sometimes outperforms the state-of-the-art FPGA-based automata processing engine, Grapefruit, in terms of throughput (pattern matching rate). Even though FPGAs offer massive parallelism, FPGAs’ clock rate is considerably lower than CPUs. On top of that, applications face performance degradation if the computation model does not fit into the CPU cache. Prior works show that in the worst case, the FPGA-based pattern matching engine has equal throughput compared to the CPU-based pattern matching engine [2] [5]. Contrary to that, this paper shows that for some real-world benchmarks, the CPU gets 4.5x speedup over the FPGA (Section V). However, if a workload is such that it matches many distinct patterns, CPU throughput degrades. So, it can be affirmed that neither CPU nor FPGA is a clear winner for the FA-based pattern matching engine.

In summary, this paper makes the following contributions:

- It presents a detailed analysis of the state count of the optimized NFA vs. minimized DFA across various real-world automata benchmarks (section III).
- It shows that on FPGA, the choice of NFA over DFA is less important than the need to keep individual DFA separate and the ability to support parallel processing of a large number of DFAs (section IV).
- This paper presents an in-depth performance analysis of the state-of-the-art CPU-based automata processing engine vs. the state-of-the-art FPGA-based automata processing engine (section V).

II. RELATED WORK

The state count of the NFA and DFA has been studied previously from the perspective of network-intrusion detection, and synthetic benchmarks [13 21 22]. The studies on the network-intrusion detection benchmarks showed that generating a DFA for a specified pattern set can exponentially increase the DFA state count. They demonstrate that regular expressions containing constraints such as dot-star (pq.*rs) and repeated sub-patterns (xyz, {100}abc) induce exponential growth in DFA states. Contrary to the prior works, this paper performs state count analysis for a diverse state of real-world benchmarks and shows that if separate DFAs are generated for each pattern, the DFA state count is equal to the equivalent optimized NFA. However, in the worst-case DFA state count shows a polynomial growth rate.

Tabakov et al. [17] evaluated Hopcroft’s [15] and Brzozowski’s [16] DFA minimization algorithm using a synthetic automata type called random automata. Their analysis illustrates that the state count of a DFA depends on the automata graph’s transition density. For smaller transition densities, the DFA state grows super-polynomially but sub-exponentially. Additionally, their result shows that minimized DFA has a smaller state count than the equivalent NFAs with greater transition densities. One limitation of this analysis is that the NFAs used are not optimized. Even though NFA minimization is a PSPACE-complete problem [23], a heuristics-based approach can generate optimized NFA, as shown in this paper.

Since Floyd et al. [24] introduced hardware implementation of NFA, there has been a substantial amount of work on high-performance automata processors using either DFA [4 13 25] or NFA [1 6 26] as a computation model. The state-of-the-art CPU-based automata processing engine Hyperscan [20] uses regex decomposition to separate the pattern into disjoint strings and FA. Moreover, to process FA, Hyperscan exploits SIMD vector operation to perform the maximum possible state transition for each memory access. Hyperscan encounters throughput degradation due to the CPU’s high memory latency if the working set size does not fit into the CPU cache. Grapefruit [5], a state-of-the-art FPGA-based automata processing engine, maps a cluster of automata into the FPGA logic fabric. Even though this approach helps in accelerating Grapefruit’s throughput, if the automata graph does not fit into the FPGA logic fabric, Grapefruit fails to process it. This paper does not discuss GPU-based automata processing engine because prior works [27 28] have presented that GPU is not promising for processing FA.

Xie et al. [2] examined throughput comparison between the state-of-the-art CPU-based automata processing engine, Hyperscan [20] and an FPGA-based automata processing engine, REAPR. Their analysis shows that in the worst case, REAPR performs the same as Hyperscan, whereas, in the best case, REAPR has a 2,000x speedup over Hyperscan. However, this paper shows that, based on the workload and the benchmark, neither Hyperscan nor Grapefruit is a clear winner for the FA-based pattern matching engine.

Becchi et al. [14] presented a performance evaluation of a network processor and a general-purpose processor using NFA, DFA, and hybrid-FA. Hybrid-FA is a variant of automata formed by halting the NFA→DFA conversion in places where DFA blowup occurs. The evaluation at [14] shows that hybrid-FA has the overall best throughput across the network and general-purpose processors. The reason is that the DFA part of the hybrid-FA is less susceptible to high memory latency, and the NFA part of the hybrid-FA keeps a check on the state explosion issue of the DFA. This performance evaluation is limited to von Neumann architecture, whereas this paper does the performance evaluation for von Neumann vs. spatial architecture.

III. NFA VS. DFA STATE COUNT ANALYSIS

By definition, if an NFA requires $n$ states to express a regular language $L$ or pattern $P$, the equivalent DFA will require at most $2^n$ states [6]. As a result, DFAs are disregarded for designing FA-based pattern matching engines on FPGA [2 21]. The state count study of DFA vs. NFA across diverse real-world benchmarks is extremely important for automata processing research. Because it would resolve if, for real-world benchmarks, minimized DFAs’ state count exhibits an
Fig. 1: State count comparison between optimized NFA and minimized DFA by generating distinct DFA/NFA for each individual pattern (shown in log-log scale). For Snort, Brill, ClamAV, and DotStar a few of the DFA's states have polynomial growth rate compared to the NFA states. Hamming DFA state count is always equal to its equivalent NFA's state count. DFA shows polynomial growth in state count compared to it's equivalent NFA for Levenshtein.

Fig. 2: State count comparison between optimized NFA and minimized DFA by merging multiple patterns into a single automaton (shown in log-log scale). Regex-based benchmarks show linear growth-rate in state count for minimized DFA compared to its equivalent optimized NFA. Minimized DFAs for Mesh-Benchmarks exhibit exponential growth-rate while for synthetic benchmark, they have equal number of states as their equivalent NFA.

While a DFA representing multiple distinct patterns may be significantly larger [13], a simplified, single pattern DFA can be as small as its equivalent NFA [13]. Thus, this paper performs state count analysis from two different perspectives. First, the state count for minimized DFA and optimized NFA is analyzed by generating distinct NFAs and DFAs for each pattern (Fig 1). Second, the state count is compared by incrementally adding patterns to a single NFA or DFA (Fig 2). These two analyses show that while generating individual DFA for each pattern, DFA's state count is typically equal to the state count of the NFA. However, few DFAs exhibit exponential growth rate compared to its equivalent NFA. The scope of prior works that perform such study is limited to network intrusion detection and synthetic benchmarks [13, 17]. This section presents an empirical analysis of the state count of DFA vs. NFA using a diverse benchmark set taken from the real workload [29].

Experimental Setup: AutomataZoo [29] benchmark suite has been used for this experiment. Each benchmark of AutomataZoo comes with a single NFA, and that NFA contains all the patterns for that particular benchmark. However, the state count analysis needs distinct NFAs representing distinct patterns, so VASim’s [30] compute connected component option is used to divide individual patterns into separate NFA graphs. Then using Brzozowski’s DFA minimization algorithm, minimized DFA is generated for each NFA. NFA minimization is a PSPACE-complete problem [23]. So, a heuristic-based approach is used to generate optimized NFA: if multiple states have equivalent outgoing transitions (for all the symbols, they transition into the same states), merge those...
TABLE I: NFA vs. DFA Performance Analysis on FPGA.

| Benchmark          | #Patterns | FSA #States (k) | LUTs (k) | FFs (k) | Frequency (MHz) | Throughput (Gbps) |
|--------------------|-----------|-----------------|----------|---------|-----------------|-------------------|
| Brill              | 5,946     | NFA 116 116     | 115 115  | 345 345  | 2.1             | 1.1               |
|                    |           | mDFA 196 277 168 | 103 0.8  |         |                 |                   |
| Snort              | 2,348     | NFA 143 143     | 135 135  | 200 200  | 1.6             | 0.6               |
|                    |           | mDFA 196 277 168 | 103 0.8  |         |                 |                   |
| ClamAV             | 14,300    | NFA 848 1,047 848 | 172 1.4  |         |                 |                   |
|                    |           | mDFA 851 1,058 849 | 164 1.3  |         |                 |                   |
| YARA               | 2,620     | NFA 115 115     | 115 115  | 194 1.5  |                 |                   |
|                    |           | mDFA 120 150 118 | 333 2.7  |         |                 |                   |
| Hamming            | 1,000     | NFA 108 56      | 64 64    | 556 4.4  |                 |                   |
|                    |           | mDFA 108 67 63  | 556 4.4  |         |                 |                   |
| Levenshtein        | 1,900     | NFA 106 125 103 | 263 2.1  |         |                 |                   |
|                    |           | mDFA 735 783 528 | 222 1.8  |         |                 |                   |
| Random Forest      | 8,000     | NFA 248 407 240 | 303 2.4  |         |                 |                   |
|                    |           | mDFA 248 409 240 | 257 2.1  |         |                 |                   |
| Entity Resolution  | 10,000    | NFA 413 465 260 | 204 1.6  |         |                 |                   |
|                    |           | mDFA 422 541 275 | 250 2.0  |         |                 |                   |
| FileCarving        | 9         | NFA 0.179 0.187 0.122 | 666 6.7  |         |                 |                   |
|                    |           | mDFA 0.184 0.211 0.128 | 666 6.7  |         |                 |                   |

states into one state. All these steps compare the state count of NFA vs. DFA for distinct patterns. An extra step is needed for the comparison where multiple patterns are merged into a single NFA/DFA graph, incrementally add patterns into an NFA and create corresponding minimized DFA and optimized NFA using the above approach.

**Evaluation:** Figure 1 & 2 shows the summary of optimized NFA vs. minimized DFA state count analysis.

1) Among the three regex-based benchmarks, (Fig 1a [11]) most of the minimized DFAs have an equal number of states as their NFAs. However, a few minimized DFAs have a polynomial growth rate in state count compared to the equivalent NFA. When patterns are merged, these regex benchmarks exhibit linear growth rate in state count for minimized DFA (Fig 2a).

2) There are two mesh automata benchmarks in Automata-Zoo. Between them, Hamming benchmark’s minimized DFAs have an equal number of states as their equivalent optimized NFAs (Fig 1b). Whereas the Levenshtein benchmark’s minimized DFA state count has a polynomial growth compared to the equivalent optimized NFA (Fig 1c). On the other hand, if patterns are merged, the state count grows exponentially for minimized DFA compared to the equivalent NFA.

3) Synthetic benchmarks such as DotStar show a linear growth in minimized DFA state count except for some polynomial growth (Fig 1d). The DFA state count shows linear growth when patterns are merged for this benchmark.

4) All the patterns for the Random Forest [11] benchmark have an equal number of states for the NFAs. Moreover, the state count of DFA is the same as the NFA. As there is only one data point for this benchmark, it is not included in Fig 1.

IV. NFA vs. DFA PERFORMANCE ANALYSIS ON FPGA

Prior works on FPGA-based automata processing engine [2, 3, 5] selected NFA as their computation model because NFA enables processing multiple states simultaneously, which exploits FPGA’s parallel execution capability. Prior works also pointed out that DFA conversion and processing are expensive as DFA might suffer from exponential state growth [21]. In contrast, Section III of this paper shows that the DFA conversion will not be as expensive if distinct DFA is generated per individual pattern. This section shows that DFAs can also exploit parallelism offered by FPGA if distinct DFAs are processed in parallel (table I).

**Experimental Setup:** For this analysis, state-of-the-art FPGA-based automata processing engine, Grapefruit [5], is used to generate the Hardware Description Language (HDL) for the synthesis, and the FPGA throughput for NFA/DFA is calculated using the maximum frequency reported after finishing the synthesis. The DFAs and NFAs used in this experiment are all optimized.

**Evaluation:** Table I presents the detailed result of the experiment. On the FPGA, DFA has 1.8x and 1.3x speedup for YARA and Entity Resolution benchmarks, respectively. Further investigation shows that NFA graphs have a higher fan-out or node degree for these two benchmarks than the DFA. High fan-out or node degree works as a performance bottleneck for FPGA processing. FPGA has identical throughput for ClamAV, Hamming, and Random Forest benchmarks for both the NFA and DFA. For the rest of the benchmarks, FPGA has 2x-1.1x speedup while processing NFA instead of DFA.

V. CPU vs. FPGA PERFORMANCE ANALYSIS

Researchers designing high-performance FA-based pattern matching engines prefer FPGA over CPU because i) CPU has limited parallelism, while FPGA offers massive parallelism, ii) CPU faces high memory latency, but FPGA does not as automata states can be mapped into the logic fabric [2, 5]. This section shows that the choice of CPU vs. FPGA is not trivial.

High memory latency negatively affects the CPU’s throughput if the automata graph does not fit into the cache. On the other hand, FPGA has a significantly lower clock rate compared to the CPU. For example, in practice, FPGA’s achieve 200-500MHz, while high-end CPUs are 2-3 GHz or more. Besides, if the entire benchmark do not fit into the FPGA logic fabric, FPGA needs an optimal memory spilling technique to accommodate all the patterns of the benchmark. For example, even though Grapefruit [5] is the current state-of-the-art FPGA-based pattern matching engine, it fails to process the entire ClamAV benchmark (33k patterns) because it does not have a memory spilling option. Instead, it breaks the application into chunks and processes those in multiple passes over the input. On the other hand, the state-of-the-art CPU-based pattern matching engine, Hyperscan [20], can, in fact, process the entire ClamAV benchmark. Not only that, Hyperscan has 4.5x speedup over Grapefruit, even though Grapefruit was processing only 43.3% of the ClamAV benchmark. Having
TABLE II: Hyperscan vs. Grapefruit Throughput Comparison

| Benchmark     | Hyperscan Throughput (Gbps) | Grapefruit Throughput (Gbps) |
|---------------|-----------------------------|-----------------------------|
| Brill         | 0.007                       | 4                           |
| Snort         | 0.359                       | 1.6                         |
| SeqMatch      | 0.020                       | 2.3                         |
| Levenshtein   | 0.0002                      | 2.1                         |
| Hamming       | 0.0003                      | 4.4                         |
| Protomata     | 0.016                       | 2.9                         |
| Random Forest | 0.005                       | 2.4                         |
| Entity Resolution | 0.014                  | 1.6                         |
| APPRNG        | 0.000083                    | 2.7                         |
| ClamAV        | 6.245                       | 1.4                         |
| YARA          | 6.877                       | 1.5                         |
| FileCarve     | 22.475                      | 5.3                         |

said that, Grapefruit has 32,530x speedup over Hyperscan for the APPRNG benchmark. So, it can safely be asserted that neither Grapefruit nor Hyperscan is the clear winner here.

**Experimental Setup:** Hyperscan is used for the CPU-based pattern matching engine and Grapefruit as the FPGA-based pattern matching engine. Hyperscan is run on an Intel i7-6700K CPU running at 4 GHz with 32 GB memory. Intel Xeon E5-2686 v4 processor running at 2.3 GHz and 32 GB memory is used as FPGA host computer. Following approach explains the Hyperscan throughput calculation step for each benchmark of the AutomataZoo [29].

1) Compile: Hyperscan takes regular expression and compiles it into a pattern database [31]. However, all the benchmarks in AutomataZoo have their automata expressed either in ANML or MNRL format. As a result, to feed the automata to Hyperscan, I use hscompile’s [32] to compile the MNRL file to a pattern database.

2) Scan: I use hsrunt [33] executable of the hscompile tool to scan the input file of each benchmark, and log the scan time for this process. Then I calculate the throughput using equation 1.

\[ \text{throughput}_{\text{Hyperscan}}(\text{Gbps}) = \frac{\text{Input\_Size}(\text{Gb})}{\text{Scan\_Time}(\text{sec})} \]  

(1)

Hyperscan uses regex decomposition as one of its throughput optimization techniques. The throughput obtained here is cross-checked by running Hyperscan with the regex version of the benchmarks to confirm that the optimization technique does not fall short if NFAs are directly fed to Hyperscan.

Grapefruit throughput is calculated only for computation kernel, excluding I/O, based on the fact that the FPGA process one input symbol per clock.

**Evaluation:** Table II shows the throughput (Gbps) comparison between the Grapefruit and the Hyperscan. Except for ClamAV, YARA, and FileCarve, Grapefruit has significantly higher throughput (max speedup 32,530x) than Hyperscan. FileCarve is a special case as the benchmark size is very small (only nine patterns). However, further exploration into the characteristic (#patterns, #pattern matched per input) of ClamAV and YARA benchmarks show that the #pattern matched per input is significantly low for these benchmarks, which means only a small portion of the automata graphs are traversed.

This paper hypothesized that Hyperscan throughput is sensitive to #pattern matched per input. In support of this hypothesis, another empirical study is performed. First, a set of input is generated synthetically for the benchmarks. Next, Hyperscan’s throughput is calculated for those benchmarks using the synthetic inputs. Fig 3 shows the result for this analysis. It can be seen that, Hyperscan’s throughput decreases as the #pattern matched per input increases. The findings in this section shows that, the CPU might not offer high parallelism or suffer from high memory latency, but the CPU is better than the FPGA if the workload does not cause high memory access. Thus, a high-performance FA-based pattern matching engine may entail a heterogeneous system, where workloads are divided intelligently between the CPU and FPGA.

VI. CONCLUSION

Tabakov et al. [17] showed that sometimes DFAs can be more compact in state count than their equivalent NFAs. However, their work does not use optimized NFAs, while their DFAs are minimized. Motivated by their work, this paper performed a state count analysis for minimized DFA and heuristically-optimized NFA across a diverse set of real-world automata benchmarks. The analysis focuses on two perspectives: i) distinct DFA and NFA are generated for each pattern, and ii) multiple patterns are merged into a single DFA/NFA. This study shows that if distinct DFAs/NFAs are generated for each pattern, minimized DFAs’ state count growth rate is often similar to its equivalent optimized NFA for these benchmarks. However, some DFAs’ state counts show exponential growth rates if multiple patterns are merged into a single DFA. Based on this finding, we hypothesized that if individual distinct DFAs are generated for each distinct pattern and are processed in parallel, the FPGA throughput for processing DFA would be similar to the FPGA throughput for processing
NFA. Furthermore, an empirical analysis of the NFA vs. DFA throughput presented in this paper supports this hypothesis. Finally, unlike prior work \cite{2,5}, this paper shows that based on the workload and the benchmark, neither CPU nor FPGA is a clear winner for the FA-based pattern matching engine. Further optimization of our FPGA framework is ongoing.

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