UNBIAS PUF: A Physical Implementation Bias Agnostic Strong PUF

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Abstract—The Physical Unclonable Function (PUF) is a promising hardware security primitive because of its inherent uniqueness and low cost. To extract the device-specific variation from delay-based strong PUFs, complex routing constraints are imposed to achieve symmetric path delays; and systematic variations can severely compromise the uniqueness of the PUF. In addition, the metastability of the arbiter circuit of an Arbiter PUF can also degrade the quality of the PUF due to the induced instability. In this paper we propose a novel strong UNBIAS PUF that can be implemented purely by Register Transfer Language (RTL), such as verilog, without imposing any physical design constraints or delay characterization effort to solve the aforementioned issues. Efficient inspection bit prediction models for unbiased response extraction are proposed and validated. Our experimental results of the strong UNBIAS PUF show 5.9% intra-Fractional Hamming Distance (FHD) and 45.1% inter-FHD on 7 Field Programmable Gate Array (FPGA) boards without applying any physical layout constraints or additional XOR gates. The UNBIAS PUF is also scalable because no characterization cost is required for each challenge to compensate the implementation bias. The averaged intra-FHD measured at worst temperature and voltage variation conditions is 12%, which is still below the margin of practical Error Correction Code (ECC) with error reduction techniques for PUFs.

I. INTRODUCTION

Hardware security has become an important aspect in modern Integrated Circuit (IC) design industry because of the global supply chain business model. Identifying and authenticating each fabricated component of a chip is a challenging task [1]. A Physical Unclonable Function (PUF) has been a promising security primitive such that its behavior, or Challenge Response Pair (CRP) [2], is uniquely defined and is hard to predict or replicate. A PUF can enable low overhead hardware identification, tracing, and authentication during the global manufacturing chain.

Silicon delay based strong PUFs have been studied intensively since its first appearance in [3] because of its low implementation cost and large CRP space compared with a weak PUF [4]. However, there are still design challenges that restrain a strong PUF from being put in a widespread practical use. One of the major design challenges for a silicon delay based PUF is the strict symmetric delay path layout requirement. The wire delays of the competing paths must be applied to construct symmetric delay paths. The existence of systematic process variation can degrade the quality of silicon based PUFs because the local randomness should be the only desired entropy source of the delay based PUF [16]. The effect of systematic process variation is similar to having biased wire delay between two delay paths, which can also damage the uniqueness of the PUF. Another possible vulnerability caused by systematic variation is the induced process side channel attack as described in [17]. Due to intra-wafer systematic variation [18], PUFs fabricated at the same region on different wafers can have similar systematic behavior, which can be exploited as a process side channel attack.

To account for systematic variations, a compensation technique is proposed in [10], which requires careful design decisions to compare RO pairs that are physically placed close to each other. In [16], the systematic variation is modeled and subtracted from the PUF response to distill true randomness with the cost of model calculation. Similarly, in [19], the averaged RO frequency is subtracted from the original frequency, where the multiple measurements of each RO can lead to large latency overhead. In [20], a method is proposed to extract local random process variation from total variation, however, a second order difference calculation is needed, and hard-macro technique must be applied to construct symmetric delay paths.

C. Metastability of the Arbiter Circuit

The idea of an Arbiter PUF is to introduce a race condition on two paths and an arbiter circuit is used to decide which one of the two paths reached first. The arbiter circuit is usually a D flip-flop or a SR latch. If two signals arrive at an arbiter within a short time, the arbiter circuit may enter a metastable state due to setup time violation [21]. Once the arbiter circuit is in metastable state, the response becomes unstable. To eliminate the inconsistency caused by metastability of the arbiter circuit, existing approaches use the majority vote or to choose the paths that have a delay difference larger than the metastable window δ at the cost of CRP characterization and discarding the unstable CRPs [7].
D. Our Contributions

In this paper, we propose the physical implementation bias agnostic (UNBIAS) PUF that is immune to physical implementation bias. The contributions of this paper include:

- We proposed the first strong UNBIAS PUF that can be implemented purely by RTL without imposing any physical routing constraints.
- Efficient inspection bit selection strategy based on intra-/inter-FHD prediction models are proposed and verified on the strong UNBIAS PUF.

II. PROPOSED STRONG UNBIAS PUF

The proposed strong UNBIAS PUF compares two delay paths to generate PUF responses. Similar to Arbiter PUF, each bit of the challenge of the UNBIAS PUF specifies the path configuration of the delay path. As shown in Figure 1, the challenge c1 and c2 specify the path configurations, and an one-bit response is extracted from the difference register, which can be of several bits long. Once a challenge is given, a signal is applied at Trigger. Each of the Clock counter begins to count the number of clock cycles of the system clock (CLK) whenever the signal from Trigger is propagated to the START input of the counter, and stops counting whenever the signal from Trigger is propagated to the STOP input of the counter. For each challenge, the difference value of the two Clock counters is stored in the difference register for further response extraction, which is described in details in Section III.

The purpose of the ROs inserted between path configurations is to increase the path delay so that it will take multiple clock cycles for the signal to propagate to stop the clock counter. As shown in Figure 2, each RO is associated with a RO counter that counts the number of oscillations of the RO. The RO counter starts counting when the signal from its previous path configuration is arrived, and propagates the signal to the next path configuration only when the count reaches a certain threshold. All the ROs are composed of same number of inverters and neither configurations nor any layout constraints are needed.

Unlike the conventional Arbiter PUF, the strong UNBIAS PUF has no metastability issues caused by a D flip-flop or a latch. The delay difference of the two paths is transformed into counter values of the system clock. By judiciously extracting the response from the difference register, the physical implementation bias can be effectively mitigated, therefore the UNBIAS PUF can be implemented purely by RTL without any routing or layout constraints. Details of the response extraction are described in Section III.

III. BIAS-IMMUNE RESPONSE EXTRACTION

A. Inspection Bit on Unbiased/Biased Paths

In this section we describe how different selections of the inspection bit can change the intra- and inter-FHD. Figure 3 shows an example of a distribution of values from difference registers of symmetrically routed UNBIAS PUFs. The length of the difference register is 22-bit, so the range of the register value is between $-2^{21}$ and $2^{21} - 1$ as represented in 2’s-complement. The large inter-chip measurement curve gives the distribution of the values across all PUFs. Since the PUF is unbiased, roughly half of the difference values would be greater than zero due to random local process variation, therefore the inter-FHD of the UNBIAS PUFs would be close to 50%. In this case, the inspection bit is simply the MSB, which divides the range of 22-bit difference value into two groups $bin_{-1}$ and $bin_{0}$. All measurements fall into $bin_{-1}$ on the left output a 1; others output a 0. The small intra-chip measurement curve gives the distribution of multiple measurements of the PUF on a same chip. Due to noise, the difference values could be different, so the intra-FHD of the difference register may not be a perfect 0%.

Even though symmetric UNBIAS PUF layout is much preferred, it is difficult and takes much effort and overhead to achieve such requirement as described in Section I-A. In practice, if no layout constraints are imposed, the measurement distribution of the difference register can be as shown in Figure 3 where most of the difference values across chips are greater than zero. In this case, using the MSB as the inspection bit would cause low inter-FHD of the PUFs because most MSBs are 0’s.

Fig. 2. ROs are inserted between path configurations to increase the path delay for better stability. The signal from previous path configuration is propagated only when the count of the RO counter reaches a certain threshold.

Fig. 3. For a symmetrically routed PUF, the inter-FHD would be close to 50%. The intra-FHD may not be zero due to measurement noise.

Fig. 4. For a biased PUF, most of the difference values across all chips could be greater than zero, causing a low inter-FHD if the MSB is the inspection bit.
For the same biased distribution shown in Figure 4, if the $i^{th}$ bit is used as the inspection bit of the difference register as Figure 5 shows, the range of the 22-bit difference value is divided into multiple bins with width $2^t$, where the output of the measurement is decided by the bin in which it resides. Note that in this case the response is not an indicator of which delay is longer in the comparison. The smaller the width of the bin is, the closer the inter-FHD is to 50% because roughly half of the outputs would reside in bin $1$ even with biased delay. On the other hand, the width of the bin should be large enough so that multiple measurements of a same PUF should always fall into the same bin. In other words, the width of the bin should be larger than the variation of the intra-chip measurement distribution. Therefore, the choice of inspection bit is a tradeoff between inter-FHD and intra-FHD for a PUF with asymmetric routing.

![Figure 5](image5.png)

Fig. 5. For an asymmetrically routed PUF with proper inspection bit, roughly half of the difference values across all chips would fall in bin $1$, therefore the inter-FHD would be close to 50%.

### IV. Inspection Bit Identification

#### A. Intra-FHD Prediction Model

The intra-FHD depends on the width of the bins $w = 2^t$ when the inspection bit is $bit_i$. A straightforward way to determine the associated intra-FHD for each inspection location is to gather multiple measurements of the same challenge on a same PUF, and simply calculate the intra-FHD for each $bit_i$. A more efficient approach is to predict the intra-FHD without calculating it for each $bit_i$.

To predict intra-FHD of a challenge $C_k$ of an inspection bit, we first obtain $t$ measured difference registers of the challenge $C_k$ of a same PUF. Since the bin width and the range of the difference register is known, the $t$ difference values can be divided into two groups (responses) according to the bins they reside in. Let the number of difference values fall in bin $1$ be $n_{one}$, and number of difference values fall in bin $0$ be $n_{zero}$. $n_{one}$ and $n_{zero}$ represent the number of responses of the challenge $C_k$ to be one and zero during the $t$ measurements, respectively. Since the intra-FHD is essentially calculated from the response difference between any two measurements, the predicted intra-FHD is calculated as:

$$intra-FHD_{k} = \frac{n_{one} \times n_{zero}}{\binom{t}{2}} \times 100\%,$$  \hspace{1cm} (1)

where the final predicted intra-FHD would be the averaged intra-FHD of all challenges.

As shown in Figure 6, the expected intra-FHD is 0% because all measurements fall in the same bin and $n_{one} \times n_{zero} = 0$. The expected intra-FHD depends on the portion of measured values that fall in bin $1$. With larger bin width $w$, it is more likely that all responses would fall into the same bin.

#### B. Inter-FHD Lower Bound Prediction Model

The inter-FHD depends on the bin width $w$ with a given inspection bit $bit_i$. Assume the distribution of inter-chip difference value is a Normal distribution $N \sim (\mu, \sigma^2)$. Define $\epsilon$ to be the distance between the mean $\mu$ and the closest bin boundary on the left as Figure 7 shows. We first prove that the worst-case inter-FHD happens when $\epsilon = 0.5w$, followed by the prediction model of the inter-FHD for the worst-case scenario.

1) Worst-Case Inter-FHD Identification: Given a fixed $w$, define $A_1(\epsilon)$ and $A_0(\epsilon)$ to be the total underlying area in bin $1$ and bin $0$ as functions of $\epsilon$, respectively. For any Normal distribution, $A_1(\epsilon)$ and $A_0(\epsilon)$ are calculated as:

$$A_1(\epsilon) = \sum_{n = -\infty}^{\infty} F(-\epsilon + 2nw + w) - F(-\epsilon + 2nw)$$  \hspace{1cm} (2)

$$A_0(\epsilon) = 1 - A_1(\epsilon, w)$$  \hspace{1cm} (3)

where $F(\cdot)$ is the Cumulative Distribution Function (CDF) of the Normal distribution, and $n$ is the index for bin area summation.

The ratio $Ratio(\epsilon)$ is defined as:

$$Ratio(\epsilon) = \frac{A_1(\epsilon)}{A_0(\epsilon)}, \hspace{1cm} 0 < \epsilon < w$$  \hspace{1cm} (4)

where the range of $\epsilon$ is from $0$ to $w$ because of its periodic structure.

The closer the $Ratio(\epsilon)$ is to one, the closer the inter-FHD would be to 50% because the two areas are closer to each other. We want to show that the largest (most unbalanced) ratio happens at $\epsilon = 0.5w$ as Figure 7 shows.

To find the extreme value of $Ratio(\epsilon)$ given a fixed $w$, we take derivative with respect to $\epsilon$ of Equation 3 and replace $A_0(\epsilon)$ by $1 - A_1(\epsilon)$ from Equation 4.

$$\frac{d}{d\epsilon} Ratio(\epsilon) = \frac{A_1(\epsilon)}{(1 - A_1(\epsilon))^2}$$  \hspace{1cm} (5)

From Equation 4 we see that to find the extreme value of $Ratio(\epsilon)$, it is equivalent to find the solution of $A_1(\epsilon)$, which is given below:

$$\frac{d}{d\epsilon} A_1(\epsilon) = \sum_{n = -\infty}^{\infty} f(-\epsilon + 2nw + w) - f(-\epsilon + 2nw)$$  \hspace{1cm} (6)

where $f(\cdot)$ is the Probability Density Function (PDF) of the Normal distribution. Equation 4 shows that $A_1(\epsilon)$ is the summation of differences between two PDF terms where one is a shifted version by $w$ of another. Therefore, applying $\epsilon = 0.5w$ to Equation 4 we get a zero. Figure 6 shows that when $\epsilon = 0.5w$, each difference term in Equation 4 has its counter part at the mirrored location to the center, so that the summation becomes zero.

To conclude our derivation, given a $w$ of an inspection bit, the extreme value of $Ratio(\epsilon)$ happens when $\epsilon = 0.5w$, and the inter-chip stander deviation $\sigma$ is needed for the $Ratio(\epsilon)$ calculation.

2) Inter-FHD Lower Bound Prediction: To predict inter-FHD, we calculate the probability of which any pair of chips produce different responses. The inter-FHD prediction given the width $w$ of the inspection bit is:

$$inter-FHD = \frac{2Ratio(\epsilon)}{(1 + Ratio(\epsilon))^2}$$  \hspace{1cm} (7)
With $\text{Ratio}(\epsilon) = 1$, the two areas are the same, resulting in a predicted 50% inter-FHD. Given a selected bit$_i$, plugging in $\epsilon = 0.5w$ to Equation 7 would give the predicted inter-FHD lower bound.

Please note that to predict inter-FHD, the inter-chip standard deviation $\sigma$ is needed because the calculation involves the CDF. However, the mean $\mu$ does not affect the prediction because the extreme value is obtained by finding the worst-case $\epsilon$. Also, since changing the inspection bit results at least a 2x change of $w$, the inter-chip $\sigma$ does not have to be calculated with high accuracy. It can be obtained by pre-layout simulation or measuring a small number of chips.

C. Inspection Bit Selection

Given the Error Correction Code (ECC) specification corresponding to the PUF design, the intra-FHD threshold can be defined. From the intra-FHD prediction model, choose a set of candidate bits that would satisfy the intra-FHD threshold requirement. From the candidate bits, a best inspection bit can be determined by applying the intra-FHD prediction model given the standard deviation $\sigma$ of the inter-chip delay distribution.

Please note that only one chip is needed for the inspection bit selection since the measurement noise is similar for all chips from our experiment and the $\sigma$ is obtained from pre-layout simulation. The location of the final inspection bit, which is a public information, is passed to all PUFs for the secret response generation.

V. EXPERIMENTAL RESULTS

A. Strong UNBIAS PUF Implementation

The strong UNBIAS PUF structure is implemented on 7 Altera DE2-115 FPGA boards. In our implementation, no physical constraints, additional XORs, tunable delay units, or any systematic variation compensation techniques are used. The design is purely a RTL design.

The ROs inserted between path configurations are composed of 19 inverters, and the signal will be propagated to the next path configuration when the RO counter associated to the RO reaches a count of 50 thousand. The UNBIAS PUF has 10 path configurations, therefore the length of the challenge is 10-bit long. The length of the difference register is 19-bit, and the length of the final response for each challenge is one bit. For our experiment, 120 challenges are applied, and 120 bits of responses are obtained for each PUF within a second. Please note that the RO structure and the count of the RO counter are selected given the 50 MHz system clock of the FPGA.

The results are similar as long as no overflow occurs at the 19-bit difference register.

B. Prediction Model Validation

The inter-FHD is obtained from 7 FPGAs, and the intra-FHD is calculated by measuring each PUF 10 times. To show inter-chip variation and measurement noise of our experimental setup, we measure the frequency of a single RO across the chips 10 times, and the inter-chip variation is 6.1% with 0.2% measurement noise.

To validate the intra-FHD prediction model, we follow the procedure described in Section IV-A with $t = 10$ measurements. Figure 8 shows the results of the intra-FHD prediction of bit$_5$ and bit$_{10}$. The intra-FHD of bit$_5$ is much higher than bit$_{10}$ because its bin width is much smaller.

To validate the inter-FHD prediction model, for each challenge, we obtain an inter-chip standard deviation $\sigma$ from 7 FPGAs, and the final $\sigma$ used in the prediction model is the median of the $\sigma$ from 120 challenges, which gives $\sigma = 521$. The results shown in Figure 9 indicate that the inter-FHD lower bound prediction is well matched with the measured data. To demonstrate that the inter-FHD prediction model does not require an accurate inter-chip $\sigma$ estimation, Figure 9 also shows the prediction range with $\sigma \pm 15\%$ variation. We can see that the differences of the predictions are limited, which indicates that the $\sigma$ can either be obtained from pre-layout simulation or measurements of a small number of chips. The prediction gap is relatively large when $w$ is much larger than $\sigma$. However, as $w$ becomes comparable to $\sigma$, where potential inspection bits begin to occur, the prediction curve rises up quickly and matches the measured data well. Figure 9 also shows that bit$_{10}$ should be a proper inspection bit because the intra-FHD is low and the inter-FHD is close to 45%.

C. Uniqueness and Reliability Evaluation

The results of inter-FHD and intra-FHD with different inspection bit selections are shown in Figure 9. As we can see from the figure, using bits closer to the MSB gives low intra-FHD but also low inter-FHD. This verifies the fact that the delay paths are biased if no physical implementation constraints are imposed. On the other hand, using bits closer to the LSB gives 50% on both intra-FHD and inter-FHD because of the measurement noise. As predicted, the best inspection location appears at bit$_{10}$ with 45.1% inter-FHD and 5.9% intra-FHD. The results also indicate that the systematic variation is mitigated because no constraints are imposed at all.

Table 1 shows comparison results with previous work. With conventional Arbiter PUF (APUF) shown in the second column, the results from [9] show that the circuit is essentially a constant number generator with very little inter-FHD. The third column shows the 3-1 double Arbiter PUF with XORs [13], where symmetric layout is still required, and the hardware overhead is 2X or 3X from the duplicated circuits depending on the uniqueness requirement of the application. The inter-FHD is close to 50% but the intra-FHD is high due to the XORs. The fourth column shows the results from Path Delay Line (PDL) PUF [6]. Symmetric PDL and delay characterization for each CRP are required, which can cause scalability issues. Also the
ability of eliminating biased responses is limited because it depends on the number of tuning stages inserted. The last column shows the proposed strong UNBIAS PUF. Its behavior is unique and stable, and most importantly no symmetric layout at all.

D. Temperature and Voltage Variations

For temperature and voltage variations, the reference responses are measured at 20°C with standard voltage 12V. The reference responses are then compared with responses measured at 20°C and 75°C with 10% voltage variation. The results indicate the reliability of the PUF when it is enrolled at normal condition but verified at a high temperature environment with unstable voltage source.

Figure 10 shows the intra-FHD using bit$\_10$ as the inspection bit. All intra-FHD at 20°C with 10% voltage variation is below 8%, and all intra-FHD at 75°C with 10% voltage variation is below 14%, which is still within conventional ECC margin with error reduction techniques for PUFs [22, 23]. Compared with RO PUF presented in [13], one possible explanation of smaller intra-FHD for our strong UNBIAS PUF is that with multiple RO delay units, the overall delay variation is canceled out, where for the RO PUF, the variation of each RO is directly compared.

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**Fig. 9.** Inter-, intra-FHD, and inter-FHD prediction using $\sigma = 521$ with different inspection bit selections of the strong UNBIAS PUF.

**TABLE I**

|                  | APUF [9] | XOR [13] | PDL [6] | UNBIAS PUF |
|------------------|----------|----------|---------|------------|
| inter-FHD        | 7.2%     | 50.6%    | 45.25%  | 45.1%      |
| intra-FHD        | 0.24%    | 11.8%    | 4.1%    | 5.9%       |
| Symm. Layout     | No       | No       | Yes     | No         |
| Characterization | No       | No       | Yes     | No         |

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**Fig. 10.** Strong UNBIAS PUF intra-FHD under temperature and voltage variations.

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VI. CONCLUSIONS

We proposed the first strong UNBIAS PUF that can be implemented purely by RTL without complex post-layout analysis or hand-crafted physical design effort. The proposed measurement can effectively mitigate the impact of biased delay paths and metastability issues to extract local device randomness. The inspection bit can be determined efficiently from the intra-FHD and inter-FHD prediction models.

The strong UNBIAS PUF is implemented on 7 FPGAs without imposing any physical layout constraints. Experimental results show that the intra-FHD of the strong UNBIAS PUF is 5.9% and the inter-FHD is 45.1%, and the prediction models are closely fitted to the measured data. The averaged intra-FHD of the strong UNBIAS PUF at worst temperature and voltage variations is about 12%, which is still within the margin of conventional ECC techniques. The fact that the proposed scheme is immune to physical implementation bias would allow the strong UNBIAS PUF to be designed and integrated with minimum effort in a high-level description of the design, such as during RTL design.

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