An Open-source Library of Large Integer Polynomial Multipliers

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Abstract—Polynomial multiplication is a bottleneck in most of the public-key cryptography protocols, including Elliptic-curve cryptography and several of the post-quantum cryptography algorithms presently being studied. In this paper, we present a library of various large integer polynomial multipliers to be used in hardware cryptocores. Our library contains both digitized and non-digitized multiplier flavours for circuit designers to choose from. The library is supported by a C++ generator that automatically produces the multipliers’ logic in Verilog HDL that is amenable for FPGA and ASIC designs. Moreover, for ASICs, it also generates configurable and parameterizable synthesis scripts. The features of the generator allow for a quick generation and assessment of several architectures at the same time, thus allowing a designer to easily explore the (complex) optimization search space of polynomial multiplication.

Index Terms—schoolbook multiplier, karatsuba multiplier, toom cook multiplier, digitized polynomial multiplication, Large integer polynomial multipliers

I. INTRODUCTION

Polynomial multiplication (i.e., \(c(x) = a(x) \times b(x)\)) is a fundamental building block for cryptographic hardware and is often identified as the bottleneck in implementing efficient circuits. The most widely deployed public key crypto systems (e.g., RSA and ECC) need polynomial multiplications [1]. Many of the post-quantum cryptography (PQC) algorithms (e.g., NTRU-Prime, FrodoKEM, Saber, etc.) also require large integer multipliers for multiplying polynomial coefficients utilized to perform key-encapsulations and digital signatures [2]. Another application is in fully homomorphic encryption, a specific branch of cryptography that requires large integer multipliers to enable multi-party and secure-by-construction on the cloud computations [3]. There is a clear demand for large integer multipliers to perform multiplication over polynomial coefficients. To our knowledge, today, no widely available repository of open source multiplier architectures exists. This is the gap that our library addresses.

There are several multiplication methods employed to perform multiplication over polynomial coefficients, including the schoolbook method (SBM), Karatsuba, Toom-Cook, Montgomery, and number theoretic transformation (NTT). A quick scan of the PQC algorithms involved in the NIST standardization effort [4] reveals that many reference implementations suggest the use of these multipliers: SBM is suggested by the authors of NTRU-Prime and FrodoKEM, Karatsuba and Toom-Cook methods are used in Saber and NTRU, a combination of NTT and SBM is suggested for CRYSTALS-Kyber, SBM and Montgomery are considered in Falcon.

Examples of recent works employing non-digitized and digitized polynomial multiplication methods are given in [5]–[11] and [12]–[14], respectively. In [5], for different polynomial sizes, an architectural evaluation of different multiplication methods (SBM, comba, Karatsuba, Toom-Cook, Montgomery, and NTT) is performed over a Virtex-7 FPGA platform. An improved Montgomery polynomial multiplier is presented in [7] for a polynomial size of 1024 bits over a Virtex-6 FPGA. A run-time configurable and highly parallelized NTT-based polynomial multiplication architecture over Virtex-7 is discussed in [8]. A systolic based digit serial multiplier wrapper on an Intel Altera Stratix-V FPGA is described in [12], where digit sizes of 22 and 30 bits are considered for operand lengths 233 and 409 bits, respectively. A digit serial Montgomery based wrapper is provided in [13], where a digit size of 64 is selected for the operand length 571 bits, on a Virtex-6. Similarly, a digit serial modular multiplication based wrapper on Virtex-7 is shown in [14], where digit sizes of 2, 4 and 8 bits are preferred for an operand length of 2048 bits.

ASIC implementations, while less frequent, also explore the polynomial multiplication design space. In [6], different polynomial multipliers with different operand lengths are considered for area and power evaluations on a 65nm technology. On similar technology, a bit level parallel-in-parallel-out (BL-PIPO) multiplier architecture is proposed in [9]. Using a 65nm commercial node, a modified interleaved modular reduction multiplication algorithm and its bit-serial sequential architecture is proposed in [10] for an operand length of 409 bits. For fully homomorphic encryption schemes, an optimized multi-million bit multiplier based on the Schonhage Strassen multiplication algorithm is described in [11] where a 60nm technology is used for synthesis.

Although there are several reported implementations of different multiplication methods [5]–[14], these implementations tend to be specifically tailored for a given operand size and for a given target (e.g., high speed or low area). The matter
is that this trade-off space is rather complicated to navigate without automation. Consequently, a common approach to assess (several) multiplication methods is required.

In order to tackle the aforementioned limitations of the available literature and the need for automation, we develop an open-source library of multipliers which we name TTech-LIB. Our library is supported by a C++ generator utility that produces — following user specifications — a hardware description of four selected multiplication methods: (a) SBM, (b) 2-way Karatsuba, (c) 3-way Toom-Cook, and (d) 4-way Toom-Cook. For selected multiplication methods, our library also offers a digitized solution: a single parameterized digit-serial wrapper to multiply polynomial coefficients. By default, the wrapper instantiates a singular SBM multiplier, but it can be replaced by any other multiplier method since the interfaces are identical between all methods. Finally, FPGA and ASIC designers can select their own multiplication method, size of the input operands, and digit size (only for the digitized wrapper, naturally). Moreover, for ASIC designers, there is the possibility to generate synthesis scripts for one of two synthesis tools, either Cadence Genus or Synopsys Design Compiler (DC). The user is not restricted to generating a single architecture at a time, the generator will produce multiple solutions if asked to do so, which will appear as separate Verilog (.v) files.

The remainder of this work is structured as follows: The mathematical background for selected multiplication methods is described in Section II. The generator architecture and the structure of proposed TTech-LIB is provided in Section III. Section IV shows the experimental results and provide comparisons of non-digitized and digitized flavours of multiplication methods. Finally, Section V concludes the paper.

II. MATHEMATICAL BACKGROUND

In this section, we present the mathematical formulations behind polynomial multiplication. We assume the inputs are two \( m \)-bit polynomials and the output is a polynomial of size \( 2m - 1 \).

A. Non-digitized multiplication

The SBM is the traditional way to multiply two input polynomials \( a(x) \times b(x) \), as shown in Eq. 1. To produce resultant polynomial \( c(x) \) by performing bit by bit operations, it requires \( 2 \times m \) clock cycles, \( m^2 \) multiplications and \( (m-1)^2 \) additions.

\[
c(x) = \sum_{i=0}^{m-1} \sum_{j=0}^{m-1} a_i b_j x^{i+j} \tag{1}
\]

Other approaches such as the 2-way Karatsuba, 3-way Toom-Cook, and 4-way Toom-Cook are more time efficient since they split the polynomials into \( n \) equal parts, as shown in Eq. 2. The value of \( n \) for 2-way Karatsuba, 3-way Toom-Cook and 4-way Toom-Cook multipliers is 2, 3 and 4, respectively and as the name implies. In Eq. 2, the variable \( k \) determines the index of the split input polynomial. For example, for a 4-way Toom-Cook multiplier, the values of \( k \) are \( \{3, 2, 1, 0\} \), meaning the input polynomial \( a(x) \) becomes \( a_3(x), a_2(x), a_1(x), \) and \( a_0(x) \).

\[
c(x) = \left( \sum_{i=0}^{m-1} a_i x^i \right) \times \left( \sum_{i=0}^{m-1} b_i x^i \right) \tag{2}
\]

In Eq. 3, the expanded version of Eq. 2 is presented for the case of 2-way split of input polynomials. The straightforward computation would require four multiplications: (1) one for the computation of inner product resulting polynomial \( c_1(x) \), two multiplications for the computation of \( c_2(x) \), and finally one multiplication for the computation of \( c_0(x) \). However, \( c_2(x) \) could be alternatively calculated with only one multiplication, as shown in Eq. 4. This is the Karatsuba observation. To generate the final resultant polynomial \( c(x) \), addition of inner products is required, as presented in Eq. 5. Similarly, when considering the 3-way and 4-way Toom-Cook multipliers, the expanded versions of Eq. 2 produce nine and sixteen multiplications, respectively. These multiplications are then reduced to five and seven using a process similar to the 2-way Karatsuba, respectively. We omit the equations for Toom-Cook multipliers for the sake of brevity.

\[
c(x) = a_1(x)b_1(x) + a_2(x)b_0(x) + a_0(x)b_1(x) + c_0(x)b_0(x) \tag{3}
\]

\[
c_2(x) = (a_1(x) + a_0(x)) \times (b_1(x) + b_0(x)) - c_1(x) - c_0(x) \tag{4}
\]

\[
c(x) = c_0(x) + c_1(x) + c_2(x) \tag{5}
\]

Now, let us assume that the polynomials involved in the multiplications above remain relatively large in size even after split. Thus, SBM multipliers can be employed to resolve the partial products. For a 2-way Karatsuba multiplier of \( m \)-bit input polynomials, there will be 3 SBM multipliers and each will take two polynomials of size \( \frac{m}{2} \) as inputs. Each multiplier requires \( \frac{m}{2} \) clock cycles to be completed. If all multipliers operate in parallel, the overall computation also takes \( \frac{m^2}{4} \) cycles. For 3-way and 4-way splits, the number of clock cycles is \( \frac{m^2}{3} \) and \( \frac{m^2}{7} \), respectively. Since our library is aimed at large polynomials, the 2-way Karatsuba, 3-way Toom-Cook, and 4-way Toom-Cook codes available in it actually implement the parallel SBM strategy discussed above. In fact, our non-digitized multipliers are hybrid multipliers.

B. Digitized multiplication

The digit serial wrapper in TTech-LIB takes two \( m \)-bit polynomials \( a(x) \) and \( b(x) \) as an input and produces \( c(x) \) as an output. Digits are created for polynomial \( b(x) \) with different sizes which are user-defined as follows: \( d = \frac{m}{n} \).
In tables I–II, clock frequency (MHz), area (in $\mu m^2$), and power (mW) values are achieved after synthesis using Cadence Genus. Similarly, in Table III, clock frequency (MHz), look-up-tables (LUTs), utilized registers (Regs) and power (mW) values are achieved after synthesis using Vivado design tool.

Finally, latency for both digitized and non-digitized multipliers (in tables I–III) is calculated using Eq. 6:

$$\text{latency (\mu s)} = \frac{\text{clock cycles}}{\text{frequency (MHz)} \times \text{total digits}}$$

where $d$ determines the total number of digits, $m$ denotes the size of input polynomial $b(x)$, and $n$ is the size of each digit. Then, the multiplication of each created digit is performed serially with the input polynomial $a(x)$, while the final resultant polynomial $c(x)$ is produced using shift and add operations. The main difference here is that our digitized solution is serial, while the 2-, 3-, and 4-way multipliers are parallel. The required computational cost (in clock cycles) to perform one digit multiplication is $n$. Since there are $d$ digits, the overall computation takes $d \times n$ clock cycles. It is important to mention that users/designers can choose any multiplication method inside the described digit serial wrapper as per their application requirements. We have used an SBM multiplication method as default.

III. HOW TO ACCESS TTech-LIB

The complete project files (written in C++) are freely available to everyone on our GitHub repository [15]. A sample of pre-generated multipliers is also included in the repository. As shown in Fig. 1, the user settings can be customized by using a configuration file (config.xml). The structure of the library is rather simple and includes five directories: (1) bin, (2) run, (3) src, (4) synth, and (5) vlog. After running the generator binary, the produced synthesis scripts are put in the synth directory while the generated multipliers are put in the vlog folder. All generated multipliers have the same interface (i.e., inputs are $clk$, $rst$, $a$, and $b$; the output is $c$).

IV. EXPERIMENTAL RESULTS AND COMPARISONS

A. Implementation results and evaluations

The experimental results for non-digitized and digitized polynomial multiplication methods over NIST defined field lengths [16] on 65nm technology node is provided in Table I and Table II, respectively. Moreover, the implementation results for various digit sizes of digitized SBM multiplication method over an Artix-7 FPGA device is given in Table III.

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TABLE II
RESULTS OF NON-DIGITIZED MULTIPLIERS FOR NIST RECOMMENDED ELLIPTIC CURVES OVER PRIME AND BINARY FIELDS

| m            | digit size (n) | total digits (d) | Freq (MHz) | latency (µs) | Area (µm²) | Power (mW) |
|--------------|---------------|-----------------|------------|--------------|------------|------------|
| 32           | 17            | 505             | 1.07       | 106956.7     | 30.9       |
| 31           | 16            | 377             | 1.31       | 107378.7     | 26.1       |
| 30           | 15            | 340             | 1.55       | 94752.7      | 20.0       |
| 31           | 16            | 340             | 1.55       | 94752.7      | 20.0       |
| 32           | 17            | 487             | 1.18       | 114999.8     | 36.7       |
| 31           | 16            | 369             | 1.55       | 91393.9      | 18.1       |
| 30           | 15            | 312             | 1.86       | 76146.8      | 14.1       |
| 31           | 16            | 357             | 2.86       | 197611.2     | 38.0       |
| 32           | 17            | 357             | 2.86       | 178581.2     | 35.1       |
| 31           | 16            | 355             | 2.90       | 167536.4     | 31.5       |
| 30           | 15            | 343             | 2.98       | 166533.1     | 30.2       |
| 31           | 16            | 313             | 3.27       | 148489.5     | 23.0       |
| 30           | 15            | 285             | 3.59       | 122227.8     | 20.8       |
| 31           | 16            | 208             | 3.82       | 125104.6     | 19.9       |
| 30           | 15            | 265             | 3.89       | 117882.4     | 19.5       |
| 31           | 16            | 261             | 3.92       | 136292.4     | 23.1       |
| 30           | 15            | 259             | 3.95       | 177834.2     | 24.1       |

TABLE III
FPGA BASED RESULTS OF DIGITIZED 1024×1024 SBM MULTIPLIER FOR DIFFERENT DIGIT SIZES (ARTIX-7)

| m            | digit size (n) | total digits (d) | Freq (MHz) | latency (µs) | LUTs | Regs | Carry | Power (mW) |
|--------------|---------------|-----------------|------------|--------------|------|------|-------|------------|
| 32           | 17            | 33.11           | 16.43      | 6369         | 1692 | 408  | 184   |
| 31           | 16            | 29.15           | 18.26      | 7995         | 1681 | 416  | 192   |
| 30           | 15            | 28.32           | 22.72      | 8079         | 1732 | 417  | 191   |
| 31           | 16            | 34.84           | 14.95      | 5964         | 1881 | 424  | 220   |
| 30           | 15            | 30.12           | 18.06      | 6397         | 1847 | 447  | 194   |
| 31           | 16            | 27.17           | 19.62      | 8780         | 1834 | 455  | 192   |
| 30           | 15            | 26.04           | 20.35      | 9053         | 1880 | 449  | 187   |
| 31           | 16            | 28.01           | 23.13      | 8938         | 1951 | 452  | 226   |
| 30           | 15            | 14.22           | 72.11      | 10993        | 3634 | 1085 | 173   |
| 31           | 16            | 13.89           | 64.48      | 8024         | 3584 | 928  | 172   |
| 30           | 15            | 16.86           | 60.06      | 11074        | 3261 | 849  | 180   |
| 31           | 16            | 17.83           | 28.98      | 10683        | 3298 | 811  | 185   |
| 32           | 17            | 17.89           | 57.28      | 11371        | 3267 | 791  | 190   |
| 31           | 16            | 17.95           | 57.04      | 11947        | 3330 | 792  | 195   |
| 32           | 17            | 18.57           | 55.14      | 12037        | 3450 | 800  | 221   |
| 31           | 16            | 18.93           | 54.09      | 11367        | 3740 | 832  | 247   |
| 32           | 17            | 19.12           | 55.50      | 11462        | 5303 | 1024 | 235   |

 decreases, as shown in column three of Table I. The decrease in frequency leads to an increase in latency, as presented in column four of Table I. In addition to latency, the corresponding area and power values also increase with the increase in size of multiplier operands (see columns five and six of Table I). It is evident from these results that the SBM multiplier requires less hardware resources than 2-way Karatsuba, 3-way Toom-Cook, and 4-way Toom-Cook multipliers. Moreover, the 2-way Karatsuba achieves lower power values as compared to other selected multipliers. This is explained by the datapath and the composition of the different multipliers. SBM requires \(2m + 2m\) bit adder, 2-way Karatsuba requires \(m + m + m\) bit adder/subtractor for generating final polynomial, 3-way Toom-

Cook requires fifteen \(\frac{m^2}{2}\) bit incrementers, and 4-way Toom-Cook requires sixteen \(\frac{m^2}{3}\) bit incrementers. There is always a trade-off between various design parameters such as area, latency, power etc. Consequently, the SBM multiplier is more useful for area constrained applications. For better latency, other multipliers are more convenient.

2) ASIC digitized multipliers: For digitizing, we have selected 521, 571, and 1024 as the lengths of the input operands, as shown in column one of Table II. Moreover, for input lengths of 521 and 571, digit sizes of 32, 41, 53 and 81 have been adopted. For an input length of 1024 bits, digit sizes are given in powers of two, for \(n = 2, \ldots, 1024\). Digit size \(n\) and total digits \(d\) are listed in columns two and three of Table II, respectively. It is noteworthy that the increase in digit size results in a decrease in clock frequency, as presented in column four of Table II. Moreover, it also translates to an increase in latency, as shown in column five of Table II. For the \(1024 \times 1024\) multiplier, the obtained values for area and power show behavior similar to a parabolic curve with respect to digit size, as given in the last two columns of Table II. This is intuitive, as in the extreme cases of too small or too large digits, the wrapper logic becomes inefficient and may even become the bottleneck for timing. In summary, for an application that requires high clock frequency, shorter digits are preferred; however, this brings a significant cost in area and power.

3) FPGA digitized multipliers: Alike ASIC demonstrations (presented in Sec. IV-A2), we have chosen similar lengths of the input operands (521, 571, and 1024) for the evaluation on an Artix-7 FPGA platform, as shown in column one of Table III. Furthermore, for input lengths of 521 and 571, digit sizes of 32, 41, 53 and 81 have been considered. For an input length of 1024 bits, digit sizes are adopted in powers of two, for \(n = 2, \ldots, 1024\). Digit size \(n\) and total digits \(d\) are listed in columns two and three of Table III, respectively. The synthesis results (clock frequency, latency, area in terms of LUTs and Regs, and power) achieved for FPGA are totally distinct when compared to ASIC values as the implementation platforms are quite contrasting. It is important to note that the frequency of the multiplier architecture increases with the increase in digit size (shown in column four of Table III). This phenomenon keeps on-going until it reaches a saturation point (i.e., best possible performance in terms of clock frequency with respect to \(n\)). Once it reaches a saturation point, then there is a decrease in the clock frequency. Moreover, the saturation occurs at any digit size between 0 to \(n\) (in this work and for this experiment, the saturation occurs when the value for \(n = 512\)). The saturation point also varies with the change in operand size of the multiplier as given in Table III. For other reported parameters, i.e., latency, LUTs and power, the saturation point is not possible to show as there is a non-linear behavior (see columns five, six and nine of Table III).

4) Figure-of-Merit (FoM) for digitized SBM multiplier: A FoM is defined to perform a comparison while taking into account different design characteristics at the same time. A FoM to evaluate the latency and area parameters for both ASIC
and FPGA platforms is defined using Eq. 7. The higher the FoM values, the better. Similarly, a ratio for latency and power characteristics are calculated considering Eq. 8.

\[
FoM = \frac{1}{\text{latency (\mu s)} \times \text{area}} \tag{7}
\]

\[
FoM = \frac{1}{\text{latency (\mu s)} \times \text{power (mW)}} \tag{8}
\]

The calculated values of defined FoMs for ASIC are given in figures 2 and 3, where various digit sizes were considered for a 1024 × 1024 multiplier.

Fig. 2. Area and latency FoM for various digit sizes of a 1024 × 1024 multiplier

Fig. 3. Power and latency FoM for various digit sizes of a 1024 × 1024 multiplier

For both FoMs (shown in figures 2 and 3), it becomes clear that the extreme cases lead to suboptimal results. For the studied 1024 × 1024 multiplier, the variant with \( n = 64 \) and \( d = 16 \) presents an optimal solution. Other similar values, such as \( n = 32 \) and \( n = 128 \), also give very close to optimal solutions.

Likewise ASICs, the calculated values of defined FoM (from Eq. 7) for FPGA is given in Fig. 4, where various digit sizes were considered for a 1024×1024 multiplier. To calculate FPGA area utilizations, the slices flip-flops, LUTs and carry units are the basic building-blocks. Therefore, the FoM in Eq. 7 can be calculated by employing different metrics-of-interest (e.g., slices, LUTs, registers and carry blocks). Note that we have used an FPGA slices as area in Eq. 7. Fig. 4 reveals that the FoM value for \( n = 512 \) and \( d = 2 \) results an optimal solution.

Fig. 4. Slices and latency FoM for various digit sizes of a 1024 × 1024 multiplier

Fig. 5. Frequency, latency and power analysis for various digit sizes of a 1024 × 1024 multiplier

The combined relation between frequency, latency and power for different values of \( n \) is illustrated in Fig. 5. Therefore, it is noted from Fig. 5 that the value of latency decreases, frequency increases with the increase in \( n \). The increase in frequency and decrease in latency keeps on-going until saturation point occurs (when \( n = 512 \)).

B. Comparison to the state of the art

To perform a fair comparison with existing state-of-the-art modular multiplier architectures, we have used similar operand lengths, digit sizes and implementation technologies (for FPGA and ASIC) as used in the corresponding solutions, shown in Table IV. In state-of-the-art solutions, multiplication results are given for different operands length. However, we have provided comparison of our results with only the larger operands. Moreover, we have used symbol ‘N/A’ in Table IV where the values for design parameters (Freq, latency and area) are not given.

Concerning only the non-digitized multipliers for comparison, the 2-way Karatsuba multiplier of [5] over Virtex-7 FPGA for operand sizes of 128, 256 and 512 bits presents 38%, 39% and 20% higher latency when compared to 2-way Karatsuba multiplier generated by TTEch-LIB, as shown in Table IV. Moreover, the generated multiplier utilizes lower hardware resources in terms of LUTs (see column seven in Table IV) as compared to resources (LUTs) utilized in [5]. On 65nm node, the BL-PIPO multiplier of [9] utilizes 55% lower hardware resources in terms of gate counts as compared to our SBM multiplier generated by TTEch-LIB.
When digitized flavor of polynomials multiplication is considered for comparison over different digit sizes, the digital serial Montgomery multiplier based wrapper of [13] results 83% higher clock frequency and requires 58% less computational time as compared to our SBM based digital serial wrapper generated by TTech-LIB. On the other hand, the SBM based digital serial wrapper results 56% lower hardware resources over Virtex-6 FPGA. There is always a trade-off between performance and area parameters. Another digital serial modular multiplication based wrapper of [14] results 14% (for ds=2) lower FPGA LUTs while for remaining digit sizes of 4 and 8, it utilizes 35% and 63% higher FPGA LUTs as compared to SBM wrapper generated by TTech-LIB. The frequency and latency parameters cannot be compared as these are not given.

The comparisons and discussion above show that the multipliers generated by TTech-LIB provide a realistic and reasonable comparison to state-of-the-art multiplier solutions [5], [9], [13], [14]. Hence, not only can users explore various design parameters within our library, they can also benefit from implementations that are competitive with respect to the existing literature.

V. CONCLUSION

This work has presented an open-source library for large integer polynomial multipliers. The library contains digitized and non-digitized flavors of polynomial coefficient multipliers. For non-digitized multipliers, based on the values for various design parameters, users/designers can select amongst several studied multipliers according to needs of their targeted application. Furthermore, we have shown that for digitized multipliers, the evaluation of individual design parameters may not be comprehensive, and figures of merit are better suited to capture the characteristics of a circuit. Furthermore, we believe the results enabled by TTech-LIB will guide hardware designers to select an appropriate digit size that reaches an acceptable performance according to application requirements. This is achieved with the aid of TTech-LIB’s generator, which helps a designer to quickly explore the complex design space of polynomial multipliers.

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REFERENCES

[1] H. Eberle, N. Gura, S. Shantz, V. Gupta, L. Rarick, and S. Sundaram, “A public-key cryptographic processor for rsa and ecc.” IEEE, 2004, pp. 98–110.
[2] NIST, “Computer security resource centre: Pqc standardization process, third round candidate announcement.” 2020. [Online]. Available: https://csrc.nist.gov/news/2020/pqc-third-round-candidate-announcement
[3] A. López-Alt, A. T. E. Tromer, and V. Vaikuntanathan, “On-the-fly multiparty computation on the cloud via multkey fully homomorphic encryption,” in Proceedings of the Forty-Fourth Annual ACM Symposium on Theory of Computing, ser. STOC ’12. New York, NY, USA: Association for Computing Machinery, 2012, p. 1219–1234.
[4] NIST, “Computer security resource centre: Post-quantum cryptography, round 2 submissions.” 2020. [Online]. Available: https://csrc.nist.gov/projects/post-quantum-cryptography/round-2-submissions
[5] C. Rafferty, M. O’Neill, and N. Hanley, “Evaluation of large integer multiplication methods on hardware,” IEEE Transactions on Computers, vol. 66, no. 8, pp. 1369–1382, 2017.
[6] M. Imran, Z. U. Abideen, and S. Pagliarini, “TTech-LIB: Center for Hardware-Security/TTech-LIB,” IET Circuits, Devices Systems, vol. 12, no. 5, pp. 775–783, 2018.
[7] M. Morales-Sandoval, C. Feregrino-Uribre, P. Kitsos, and R. Cumplido, “Area/performance trade-off analysis of an fpga digit-serial gf(2m) montgomery multiplier based on lfsr,” Computers & Electrical Engineering, vol. 39, no. 2, pp. 542 – 549, 2013.
[8] J. Xie, P. K. Meher, X. Zhou, and C. Lee, “Low register-complexity systolic digit-serial multiplier over g f(2^m) based on trinomials,” IEEE Transactions on Multi- Scale Computing Systems, vol. 4, no. 4, pp. 773–783, 2018.
[9] R. Azarderakhsh, K. U. Jarvinen, and M. Mozaffari-Kermani, “Efficient algorithm and architecture for elliptic curve cryptography for extremely constrained secure applications,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 61, no. 4, pp. 1144–1155, 2014.
[10] S. R. Pillutla and L. Boppana, “An area-efficient bit-serial polynomial basis finite field gf(2m) multiplier,” AEU - International Journal of Electronics and Communications, vol. 114, p. 153017, 2020. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1434841119318485
[11] Y. Doröz, E. Öztürk, and B. Sunar, “Accelerating fully homomorphic encryption in hardware,” IEEE Transactions on Computers, vol. 64, no. 6, pp. 1509–1521, 2015.
[12] M. Imran, Z. U. Abideen, and S. Pagliarini, “TTech-LIB: Center for Hardware-Security/TTech-LIB,” IET Circuits, Devices Systems, vol. 12, no. 5, pp. 662–668, 2018.
[13] M. Imran, Z. U. Abideen, and S. Pagliarini, “TTech-LIB: Center for hardware security.” 2020. [Online]. Available: https://github.com/Centre-for-Hardware-Security/TTech-LIB
[14] C. Lily, M. Dustin, R. Andrew, and R. Karen, “Recommendations for discrete logarithm-based cryptography: Elliptic curve domain parameters.” 2020. [Online]. Available: https://nvlpubs.nist.gov/nistpubs/SpecialPublications/NIST.SP.800-186-draft.pdf

| Ref | Multiplier | Device | m | Freq (MHz) | Latency (µs) | Area (µm²)/LUTs |
|-----|------------|--------|---|------------|-------------|----------------|
| [5] | 2-way KM   | V7     | 128 | 104.5      | 0.61        | 3499           |
| [5] | 2-way KM   | V7     | 256 | 74.5       | 1.71        | 7282           |
| [5] | 2-way KM   | V7     | 512 | 51.6       | 4.96        | 20474          |
| [9] | BL-PIPO    | 65nm   | 163 | N/A        | N/A         | 5228 GE        |
| [13] | DSM (ds=64) | V6    | 571 | 258.5      | 0.03        | 10983          |
| [14] | DSM (ds=2) | V7    | 2048 | N/A        | N/A         | 18067          |
| [14] | DSM (ds=4) | V7    | 2048 | N/A        | N/A         | 33734          |
| [14] | DSM (ds=8) | V7    | 2048 | N/A        | N/A         | 62023          |
| [14] | DSM (ds=4) | V6    | 256  | 167.4      | 0.38        | 2110           |
| [14] | DSM (ds=2) | V7    | 256  | 119.9      | 1.06        | 4318           |
| [14] | DSM (ds=4) | V7    | 256  | 63.38      | 4.01        | 9582           |
| [14] | DSM (ds=8) | V7    | 256  | 17.4       | 3.07        | 25315          |
| [14] | DSM (ds=4) | V6    | 571  | 46.1       | 1.74        | 6181           |

V7: Xilinx Virtex-7, V6: Xilinx Virtex-6, ds: digit size, TW: this work, DSM: Digit Serial Montgomery multiplier based wrapper, BL-PIPO: Bit level parallel in parallel out multiplier using SBM multiplication method, GE: gate equivalents.