DATE: Defense Against TEMperature Side-Channel Attacks in DVFS Enabled MPSoCs

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Abstract—Given the constant rise in utilizing embedded devices in daily life, side channels remain a challenge to information flow control and security in such systems. One such important security flaw could be exploited through temperature side-channel attacks, where heat dissipation and propagation from the processing elements are observed over time in order to deduce security flaws. In our proposed methodology, DATE: Defense Against TEMperature side-channel attacks, we propose a novel approach of reducing spatial and temporal thermal gradient, which makes the system more secure against temperature side-channel attacks, and at the same time increases the reliability of the device in terms of lifespan. In this paper, we have also introduced a new metric, Thermal-Security-in-Multi-Proce-sors (TSMP), which is capable of quantifying the security against temperature side-channel attacks on computing systems, and DATE is evaluated to be 139.24% more secure at the most for certain applications than the state-of-the-art, while reducing thermal cycle by 67.42% at the most.

Index Terms—Lifetime reliability, multiprocessor systems-on-chip (MPSoCs), thermal management, side-channel attack, security, machine learning, DVFS.

1 INTRODUCTION AND MOTIVATION

As embedded computing systems become more and more ubiquitous, security issues in these and similar systems become more paramount. These embedded systems have to face hostile security threats [1]–[4] such as physical, logical/software-based and side-channel/lateral attacks. Amongst these, side-channel attack is a popular security threat due to ease of access to the physical hardware [1]–[3], where attacks are performed by observing the properties and behavior of the system such as power consumption, thermal dissipation, electromagnetic emission, etc.

Comparatively a lot less documented studies are performed in temperature based side channel attacks [1]–[3] in the embedded computing systems. Due to a rise in the use of heterogeneous multi-processors systems-on-chip (MPSoCs) [5], [6] in the embedded systems and a rise in studies on thermal side channel attacks [3], [7], [8], it is crucial that side channel attacks in such platform should be addressed with utmost importance [8]. Several studies [3], [7], [8] have pointed out processor’s core temperature could be used to carry out side channel attacks even when the system has strong spatial and temporal partitioning of resources such as separate partitioning of cache memory, bus bandwidth, etc. But all these studies are focused on general purpose processors (using Complex Instruction Set Computer (CISC) architecture) and not on embedded multi-processors (using Reduced Instruction Set Computer (RISC) architecture), which have different architecture and operating signature from the general purpose ones. On the other hand, we could also see several studies [9], [10] documenting power/energy consumption for different types of instructions. Since there is a direct correlation between power consumption and heat dissipation [11], [12], and armed with the knowledge of power consumption of each instruction executed on processors, it is even easier to launch a side channel attacks on these systems.

In the study [7] thermal covert channels on multi-processors were exploited by observing the exponential rise and fall of CPU temperature while executing a CPU intensive application. In order to verify this behavior on embedded multi-processors we observed the temperature readings on 4 ARM Cortex A-15 big CPU cores on the Exynos 5422 [13] system-on-chip (SoC) while almost idle (the system was only executing background OS processes and the Linux governor was running ondemand power scheme), which we denote as baseline temperature of the CPU cores. In Fig. 1 we could notice baseline temperature of ARM Cortex A-15 big CPUs1 in both 2D (Fig. 1.(a)) and 3D (Fig. 1.(b)) plots. The reason to provide a visual representation of both 2D and 3D plots is to highlight the spatial as well as temporal thermal gradient because the 2D representation might not be able to provide a microscopic view of spatial thermal gradient over time. The X-axis of the 3D graph represents the temperature, Y-axis of the graph represents time interval and the Z-axis represents the frequency of that particular temperature over time. Since the Odroid XU4 [6] platform, which implements the Exynos 5422 MPSoC, only have temperature sensors on 4 ARM Cortex-A15

1. The graph representing the baseline temperature readings for different ARM Cortex A-15 big CPUs closely mimicked the oscillatory pattern that of simple harmonic motion [14].
In temperature side-channel attacks focus on channels and hence leading to temperature side-channel attacks. Our earlier observation, it became evident that heat dissipation from multiple processors could in fact lead to thermal covert channels and hence leading to temperature side-channel attacks. In order to overcome the pressing issue of temperature side-channel attacks, we propose a novel thermal management methodology on Dynamic Voltage Frequency Scaling (DVFS) [5], [19]–[21] enabled MPSoCs in an embedded device, and to the best of our knowledge it is the first documented methodology on securing against thermal side-channel attacks on DVFS. DVFS helps to reduce the energy consumption by executing the workload over extra time at a lower voltage and frequency, which could be accounted for reduced power consumption. We have coined our proposed methodology as DATE, Defense Against TEmperature side-channel attacks. Another important advantage of our proposed methodology is that due to the overall reduction of operating temperature the reliability of the device in terms of lifespan also increases. We have also performed temperature based side-channel attack on the latest Samsung Galaxy Note9 [22] (utilizing Exynos 9810 MPSoC [23]) phablet to show the efficacy of DATE by using Covolutional Neural Network (CNN) [24]–[26] based Deep Learning [27] to analyze thermal behavior and predict which password is being used for cryptographic operations. In summary, this paper makes the following contributions.

1) A new metric to quantify the probability of the embedded device prone to temperature based side-channel attacks.
2) A novel thermal management scheme specific to executing application to secure against temperature side-channel attacks and improve reliability of the device in terms of lifespan.
3) Motivational case study with a real attack on real hardware platforms such as Galaxy Note9 [22] and Odroid-XU4 [6].
4) Implementation and validation of our proposed methodology on the real hardware platform (Odroid-XU4) using several benchmark applications.

The rest of the paper is organized as follows. Sec. 2 describes the problem definition and introduces some terms useful to understand the proposed methodology. In Sec. 3, we discuss the proposed methodology along with associated block diagram and algorithms. Sec. 5 explores the different experimentation and evaluation performed to prove the efficacy of our proposed methodology while discussing the future scope of this research. In Sec. 6, we explore the related works on this topic and finally, Sec. 7 concludes the paper.

2 Problem Formulation

If we assume that there are $n$ number of processing elements ($p$) in the MPSoC and $P$ represent the set of all the processing elements then we get Eq. 1
Now, if we consider \( b_i \) be the baseline temperature for a processing element \( p_i \), where baseline temperature is the temperature of the corresponding processing element \( i \) on the MPSoC while idle, and \( t_j \) be the maximum operating temperature of \( p_i \) while executing a task \( T \), then we get the formula for Baseline Temperature Difference (BTD) for \( p_i \) for task \( T \) as Eq. 2.

\[
BTD_{pi} = |t_j - b_i|
\]  

(2)

If \( S(BTD) \) be the set of all Baseline Temperature Difference for all processing elements for a particular task \( T \) in the system such that \( S(BTD) = \{ BTD_{p_1}, BTD_{p_2}, ..., BTD_{p_n} \} \), then from the Eq. 2 we can deduce the equation for Baseline Maximum Thermal Deviation (\( \tau \)) as follows:

\[
\forall p_i \in P: \quad \tau = \max(S(BTD))
\]  

(3)

Let’s assume that the temperature difference \( (d_i) \) between any two processing elements such as \( t_k \) and \( t_j \) be the average operating temperature of \( p_k \) and \( p_j \), respectively, while executing a task \( T \), then we get the following equation:

\[
d_i = |t_j - t_k|
\]  

(4)

Now, for all the processing elements \( P \) we will achieve \( n! \) combinations of temperature difference between any two processing elements in the system. If we consider Spatial Processing Temperature Differences (SPTD) be a set containing all the combinations \( \binom{n!}{2(n-2)!} \) of temperature differences between the processing elements while executing a task \( T \) then we could derive the formula for Spatial Maximum Thermal Deviation (\( \omega \)) as follows:

\[
\forall p_i \in P: \quad \omega = \max(SPTD)
\]  

(5)

For quantifying the security of a MPSoC against temperature side-channel attacks, we can derive an equation from the values of \( \tau \), \( \omega \) and the frequency of thermal cycle during execution of task \( T (\theta) \). The reason to choose these three variables (\( \tau \), \( \omega \) & \( \theta \)) is that from our experiments (described in Section 2.1) we observed that these three variables are directly correlated to thermal behavior of the processing elements. We define the security against temperature side-channel attacks as Thermal-Security-in-Multi-Processors (TSMP), shown in Eq. 6.

\[
TSMP = \frac{1}{\tau + \omega + \theta} \quad 0 < TSMP < 1
\]  

(6)

In Eq. 6 if the value is closer to 1 then it means that the device is more secure against temperature side-channel attacks, whereas, as value closer to 0 means that the device is more prone to security threats related to temperature side-channel. We also have to keep in mind that \( (\tau + \omega + \theta) \) can never be \( \infty \) or 0 in reality nor the value of \( \tau \), \( \omega \) and \( \theta \) could be decimal as per our platform. Now, from the Eq. 6 in order to improve the security of a device against temperature side-channel attacks our main objective is to keep the total value of \( (\tau + \omega + \theta) \) as low as possible such that the value of \( TSMP \) is as close to 1 as possible. Therefore, we could define our problem as follows.

**Given:** An application and a MPSoC platform with DVFS support.

**Find:** Maximum value of TSMP.

**Subject to:** Meeting performance requirement of each application within available MPSoC resources.

### 2.1 Importance of \( \tau \), \( \omega \) and \( \theta \) in TSMP metric

To understand the key factors that are related to establishing thermal side-channel attacks on a MPSoC such as Odroid XU4 [6], we performed RSA encryption and decryption several times on the platform and observed the thermal behavior of the four ARM A15 (big) CPU cores. On the Odroid XU4, the 8 CPU cores (big.LITTLE) are denoted as CPU 0, CPU 1 to CPU 7, where CPU 0 to CPU 3 are ARM A7 (LITTLE) cores and CPU 4 to CPU 7 are ARM A15 (big) cores. We are only performing the encryption and decryption on one of the big CPU cores (CPU 6) so that we could observe the thermal behavior on the other neighboring idle CPU cores (CPU 4, 5 and 7). Fig. 3
shows one such instance of the experiments performed where we are observing the thermal behavior 3 seconds before the RSA encryption and decryption is executed till 2 seconds after the execution completes. In Fig. 3 we have highlighted three important observations (see Observation 1, 2 and 3 in the figure), which were common in all the experiments performed. On the Y axis of Fig. 3 we could notice the temperature in degree centigrades of each of the A15 CPU cores, colour coded separately for individual CPU cores, and the X axis represents the time interval with 100 milliseconds gap between each interval. In Observation 1 we could notice that the temperature drastically increases on CPU 6 within 3 seconds and the most important thing to notice here is that only the temperature of CPU 6 increases but at the same time temperature of all neighboring A15 CPU cores (CPU 4, 5 and 7) also increase. The reason for this phenomenon is due to heat dissipation and propagation in the lateral direction. In Observation 2 we can notice that once the encryption and decryption complete on CPU 6 the temperature plummets not only on that core but also on the neighboring cores. Although in this observation it could be noticed that temperature plummets over 2 seconds and not instantaneously. As stated by Masti et al. [7], thermal covert channels can be exploited by observing the exponential rise and fall of CPU temperature. Therefore, Observation 1 and Observation 2 proves the theory proposed in the study [7]. More importantly, Baseline Maximum Thermal Deviation (\(\tau\)) and Spatial Maximum Thermal Deviation (\(\omega\)) directly reflect the issues mentioned in Observation 1 and 2 of Fig. 3.

More interestingly, if we notice Observation 3 (3.A and 3.B) we can find that whenever there is a spike in temperature on CPU 6 there is also a spike in temperature on the neighboring CPUs due to heat propagation. Thus proving that when the temperature of one CPU core increases, due to heat propagation from that CPU core to the nearby CPU cores the thermal behavior of these adjacent cores are also affected. Therefore, potentially opening up a vulnerability if one such adjacent CPU core could be used to establish a temperature side-channel attack.

Since, \(\tau\) and \(\omega\) reflect the temporal as well as spatial thermal gradient difference of the CPU cores while they are executing a task (or set of tasks) and being idle, the aforementioned variables are very important in understanding the vulnerability of MPSoCs against temperature side-channel attack. Whereas, the frequency of thermal cycle during execution of a task (or set of tasks) (\(\theta\)) directly reflects the phenomenon of Observation 3 (3.A and 3.B) and hence \(\theta\) also plays an important role in deducing vulnerability related to temperature side-channel attack. Therefore, it is crucial to define the Thermal-Security-in-Multi-Processors (TSMP) metric incorporating \(\tau\), \(\omega\) and \(\theta\).

### 3 Proposed Methodology: DATE

#### 3.1 Overview of DATE

An overview of the proposed DATE methodology is illustrated in Fig. 4. It has some offline and online steps. During offline profiling computed results for various applications are used to identify the appropriate temperature (\(T_{\text{App1}}\)) and frequency (\(f_{\text{App1}}\)) such that a cumulative least value for \((\tau + \omega + \theta)\) (see Eq. 6) is achieved. Since for each application we have to explore all the possible frequency values along with appropriate temperature and performance threshold such that TSMP is maximum for \(\text{App1}\), we do the profiling offline as part of the design space exploration. Once we have found out the best possible frequency and temperature which yields the least value for \((\tau + \omega + \theta)\), we save the frequency and temperature values along with some other parameters. These values are later used during the online step where we set the frequency and temperature threshold of the system to these saved values.

In DATE, we call the offline step as Learning Module whereas, the online step is called as Decision Module. Since, operating temperature of the device directly affects the reliability of such device in terms of lifespan, hence, DATE methodology affects the reliability of the device in a positive manner (more details in Sec. 5.3).

![Proposed Methodology: DATE](image)

#### 3.2 Learning Module

The complete algorithm explaining the working of Learning Module is provided in Algo. 1.

In the study [11] through experiments on real devices, it was noticed that on MPSoCs power and temperature follow a relationship of quadratic function. On the other hand, in DVFS enabled MPSoCs dynamic power and frequency follow a quadratic relationship due to the power consumption (\(P \propto V^2f\)) being directly affected by the operating frequency and voltage [28]–[30]. However, to make our approach fast during run time (Decision Module) we assume that frequency and temperature follows a linear relationship represented by Eq. 7.

\[
t_i = \alpha \times f_i + \beta
\]

In Eq. 7, \(f_i\) is the operating frequency at time instance \(i\), \(t_i\) is the operating temperature at the same time instance, \(\alpha\) is the relationship variable and \(\beta\) is the intercept variable.

Now, we first set a performance deadline (for our case we choose execution time deadline for each application) and then start executing \(\text{App}_i\) and vary the frequency as well as the temperature threshold of the system to observe the performance. Here, the temperature threshold is the operating thermal cap, which can not be surpassed by the system during the execution of the application. If we consider \(T_{\text{available}}\) is the set of all available operating temperature (\(T_{\text{available}} = \{t_1, t_2, ..., t_i\}\) of the
system, which will be used as the thermal cap during the profiling, then for each instance of operating temperature ($t_{available}$) from $t_{available}$, we monitor the performance while setting the temperature threshold to $t_{available}$. 

While monitoring performance the frequency of the PEs is reduced by one frequency scaling step (we start at the maximum frequency and this is denoted as ReduceFrequencyByOneStep() in Algo. 1) and returns the reduced frequency instance ($f_i$). We monitor the temperature of each PE (denoted as MeasureTemperatureValue() in Algo. 1) and returns the set of temperature values of all the PEs during the profiling. If the performance deadline for the application is met then the maximum value among the set of temperature is used as the temperature threshold. By this approach we leverage DVFS capability of the system and modify the frequency till the performance constraint is met and try to achieve least possible values for $\tau$, $\omega$ and $\theta$. After we have found the appropriate value of system's temperature threshold/cap ($t_{App}$) and frequency ($f_{App}$) we note the value of $\alpha$ and $\beta$ (from Eq. 7). For $App_i$, the relationship with pig and interval are denoted by $\alpha_i$ and $\beta_i$, respectively. For each profiled application we only save the values of maximum operating temperature threshold/cap ($t_{threshold_{App}}$) which should not be surpassed during the execution of $App_i$, operating frequency ($f_{App_i}$), $\alpha_i$, $\beta_i$, and baseline temperature ($b_{App_i}$) during the profiling period on the memory to be used in the Decision Module. Here, the baseline temperature ($b_{App_i}$) for the profiling application is the same baseline temperature, which is recorded before and after the application is executed such that $b_{App_i} = b_1$ in Eq. 2. In practice, we actually save the value of $b_{App_i}$ for each processing element in the system as a set of baseline temperatures ($B_{App_i}$).

Algorithm 1: Learning Module Execution

Input:
1. $Per f_{max}$: performance deadline for an application instance $App_i$
2. $B_i$: a set of baseline temperature ($b_i$) for each processing element (PE)
Output: $< t_{threshold_{App}}, f_{App_i}, \alpha_i, \beta_i, B_{App_i} >$
Initial: $\tau + \omega + \theta = \infty$

foreach $t_{available}$ in $t_{available}$ of the system do

\[ t_{threshold_{App}} = t_{available}; \] %\%Per $f_{App}$ is the current performance of the application%

while $Per f_{App} = Per f_{max}$ do

\[ f_i = \text{ReduceFrequencyByOneStep}($\omega$); \] (see Sec. 3.2)
\[ T_i = \text{MeasureTemperatureValue}($\omega$); \]
\[ \tau_i = \text{CalculateTau}($B_i$); \] %\%See Eq. 3\%
\[ \omega_i = \text{CalculateOmega}($B_i$); \] %\%See Eq. 5\%
\[ \theta_i = \text{CalculateTheta}($\omega$); \] %\%See Sec. 3.2\%

if ($\tau_i + \omega_i + \theta_i < (\tau + \omega + \theta)$) then

\[ \tau = \tau_i, \omega = \omega_i, \theta = \theta_i; \]
\[ t_{threshold_{App}} = \text{max}($T_i$), f_{App_i} = f_i; \]

return $< t_{threshold_{App}} , f_{App_i}, \alpha_i, \beta_i, B_{App_i} = B_i >$

3.3 Decision Module

The algorithm for Decision Module is provided in Algo. 2. In the Decision Module, a software agent, which we call as DATE as well, first loads the baseline temperature ($b_{App_i}$) for the profiled application and compares the current temperature with baseline temperature during this time instance ($b_{now}$. Since baseline temperature can vary depending on the surrounding and other unforeseen circumstances, it is important DATE is aware of the difference between the baseline temperature when the application was profiled and the baseline temperature for the time period when the Decision Module of DATE acts and could be represented as $b_{diff} = b_{App_i} - b_{now}$. For set of PEs it is $B_{diff}$.

Now, if we assume that the value of $\alpha$ and $\beta$ remains almost same (subject to some obvious deviation and we refer to it as error) then from Eq. 7 we can get the equation (see Eq. 8) that could define the relationship between two different operating temperature and their associated frequencies.

\[ f_2 = \frac{(t_2 - t_1)}{\alpha} + f_1 \]

(8)

We can modify the Eq. 8 to reflect the governing equation (see Eq. 9) to decide the operating temperature threshold and associated frequency by DATE.

\[ f_{desired} = \frac{(t_{desired} - t_{threshold_{App}})}{\alpha} + f_{App_i} \]

(9)

If the value of $b_{diff}$ is negative then DATE reduces the operating frequency by evaluating the new operating frequency value while comparing that $b_{diff} = (t_{desired} - t_{threshold_{App}})$ in Eq. 9. But if the value of $b_{diff}$ is positive then Eq. 9 could be modified as follows:

\[ f_{desired} = \frac{(t_{desired} + b_{diff})}{\alpha} + f_{App_i} \]

(10)

If the value of calculated $f_{desired}$ is more than the available frequency of the CPU cores then DATE do not modify the operating frequency, thus, $f_{desired} = f_{App_i}$ but modifies the operating temperature threshold as $f_{desired} = b_{diff} + t_{threshold_{App}}$. While executing the application, if the operating temperature of the CPU cores tries to go higher than the operating temperature threshold, DATE drops the frequency ($f_{desired}$) to next frequency scaling level, which is again evaluated from the Eq. 8 by assuming that the operating temperature of the system needs to be reduced by 1° Centigrade. The governing equation to achieve this is as follows:

\[ f_{desired} = f_{now} - \frac{1}{\alpha} \]

(11)

where, $f_{desired} - f_{now} = -1$

4 CASE STUDY: PERFORMING A REAL ATTACK ON GALAXY NOTE9 AND ODROID XU4

We performed a live attack on the Galaxy Note9 mobile device, which is one of the top rated smart phones of 2018 and 2019 [31], [32]. To prove the scalability and affect of the attack we also executed the same methodology on Odroid XU4. We executed a program sitting on one of the LITTLE cores on the device, while snooping the thermal behavior of the big core cluster during several encryption (AES-256 [33]) operations.
of a text file with 4 of the most common passwords used by the users. The main motive of this attack is to evaluate the vulnerability of the latest smart-phone against thermal side-channel attack. More details on the device, experimental setup and evaluation of the attack is provided in the following subsections.

4.1 Hardware & Software Infrastructure of Note9

Nowadays heterogeneous MPSoCs consist of different types of cores, either having the same or different instruction set architecture (ISA). Moreover, the number of cores of each type of ISA can vary based on MPSoCs and are usually clustered if the types of cores are similar. For this research, we have chosen an Asymmetric Multi-processors (AMPs) system-on-chip (AMPSoC), which has clustered cores on the system. We chose to execute a real attack on Galaxy Note9 [22], which is the latest mobile device from Samsung and utilizes the Exynos 9810 MPSoC [23]. The block diagram of Exynos 9810 is provided in Fig. 5. Exynos 9810 has two big clusters, one for big CPU cores consisting of 4 Mongoose 3 CPU cores, and the other cluster for LITTLE CPU cores consisting of 4 Cortex A-55 CPU cores. The Mongoose 3 CPU cores allow cluster wise DVFS and has 18 frequency scaling levels ranging from 650 MHz to 2704 MHz. Whereas, the LITTLE Cortex-A55 CPU cores has 10 frequency scaling levels ranging from 455 MHz to 1794 MHz. The Galaxy Note9 was running on Android 9 (Pie) [34] OS utilizing Linux kernel version 4.9.59, which has only one governor named schedutil based on Energy Aware Scheduling (EAS) [35]. The Galaxy Note9 is only utilized for this case study to prove the threat of thermal side channel attack in real popular commercial device.

4.2 Hardware & Software Infrastructure of Odroid XU4

We also chose Odroid XU4 board [6] (see Fig. 6) to execute the attack in order to verify the affect and scalability of thermal side-channel exploitation on a device other than Galaxy Note9. We also used Odroid XU4 for the rest of the experimentation and validation because of more availability of software execution support since Galaxy Note9 is vendor locked to only modify certain portions of the Android OS. Odroid XU4 employs the Samsung Exynos 5422 [13] MPSoC. As mentioned earlier Exynos 5422 MPSoC contains clusters of big and LITTLE cores. This MPSoC provides DVFS feature per cluster, where the big core cluster has 19 frequency scaling levels, ranging from 200 MHz to 2000 MHz with each step of 100 MHz and the LITTLE cluster has 13 frequency scaling levels, ranging from 200 MHz to 1400 MHz, with each step of 100 MHz.

The Odroid XU4 was running on UbuntuMate version 14.04 (Linux Odroid Kernel: 3.10.105), which was running on performance governor.

4.3 Dataset and CNN Model

To perform the attack we chose 4 of the 25 most common passwords of 2017 and 2018 [36], [37] as surveyed by the Internet security firm SplashData. The 4 common passwords used by the user, which are chosen for our attack, are 123456, password, 111111 and football. We executed AES-256 [33] encryption on a text file using the aforementioned passwords 500 times for each password. The reason to choose AES-256 is because of its

```plaintext
Algorithm 2: Decision Module Execution
Input:
< t_thresholdApp, f_App, α_App, β_Req, B_app > & B_now
B_diff = CalculateBaselineDiff(B_app, B_now); (Sec. 3.3)
for each PE in the set of PEs (P) on the system do
    bPE_diff = GetBaselineDiff(B PE, P); %Function to get the baseline difference (bPE_diff) for Pi
if bPE_diff > 0 then
    f_desired = CalculateDesiredFrequency(bPE_diff); (using Eq. 10)
    SetFrequencyOfPE(f_desired); %Function to set the frequency of the PE with the value of f_desired
    SetTempThres(t_thresholdApp); %Function to set the maximum thermal cap of the PE as t_thresholdApp
else
    f_desired = CalculateDesiredFrequency(bPE_diff); (using Eq. 11)
    % f.mx is the maximum frequency of the PE
    if f_desired > f_mx then
        f_desired = f_APP; SetFrequencyOfPE(f_desired); %Function to set the frequency of the PE
        SetFreqThres(t_thresholdApp); %Function to set the maximum frequency of the PE
    else
        SetFrequencyOfPE(f_desired); SetTempThres(t_thresholdApp);
```

Fig. 5: Exynos 9810 [23] MPSoC block diagram highlighting major components
Fig. 6: Odroid XU4 [6] MPSoC block diagram highlighting major components

popularity. The encryption operations were performed on the 4 Mongoose 3 big CPU cores (big CPU cluster) while one of the LITTLE cores snoop the operating temperature data of the big CPU cluster. This is due to the fact that only one thermal sensor is present on the big CPU cluster of Galaxy Note9 rather than individually placed on each big CPU core. After the temperature data for each password were collected, we transformed the data points into a graphical representation in order to be fed to a pre-trained CNN [38] for training and classification purposes. Since on the Odroid XU4 thermal sensors are individually placed on each big CPU cores, we chose to only record the thermal behavior of one of the big CPUs (CPU 7) for this experimental attack.

We chose ResNet50 CNN [26] as our network model, which could be used to train our graphical thermal data using Transfer Learning [38]. Since, CNN based Deep Learning usually requires a lot of training data in order to be used successfully for classification purposes, the network models are trained on large dataset such as ImageNet [39], consisting of millions of images, and then the weights and parameters of the model are saved and used later to train for a specific target application. This way of training is called transfer learning and we have used ResNet 50, which is pre-trained on ImageNet. Since, ResNet50 is pre-trained on ImageNet and has the last fully connected layer to classify 1000 different classes/labels from the ImageNet, we had to modify the last fully connected layer to suit our target application.

Since, we have 4 passwords as the classes/labels to classify, we removed the last fully connected layer, which was pre-trained on ImageNet, to cater for only 4 labels instead. We have also added a new fully connected layer (called Dense in Fig. 7), dropout regularization (called Dropout in Fig. 7) and a softmax function along with a classifier (called PREDICTIONS in Fig. 7) to only predict for 4 passwords (labels). In Fig. 7 we have shown the modified fully connected layer along with the custom classifier used in our ResNet50 CNN model. Here, the dropout regularization is used for better generalization and the softmax function is used for probability distribution for the 4 labels/classes. In Fig. 8, we show the graphical representation of the thermal behavior for each password label, which is fed

Fig. 7: Architecture of ResNet50 CNN model with modified last fully connected layer used in password classification
Fig. 8: Graphical representation of thermal behavior (time interval vs temperature in °C) of encryption operation using the following passwords: 111111, 123456, passw0rd & football

to the ResNet50 CNN model for training and classification purpose.

From the 500 graphical data for each password label, we separated 100 graphical data for cross-validation testing purpose. Whereas, 75% of the remaining 400 graphical data for each password label were used for training and rest of the 25% is used for validation during the training period. Validation data is used to provide an unbiased evaluation of a model fit on the training dataset while tuning hyperparameters of the model. Code availability: Program codes to implement the attack and generate the dataset could be accessed from ## Codewillbeprovideduponacceptance##.

4.4 Experimental Results

After training the ResNet50 model with the training and validation dataset from Note9, the total prediction accuracy achieved is 36.50%. When we used 400 graphical data (100 data from each password label) for cross-validation to evaluate the accuracy of the trained ResNet50 CNN in predicting the password being used for encryption operation, the CNN could predict 146 instances correctly and achieving a prediction accuracy of 36.50%. Whereas, when we implemented DATE on the system to improve the security against thermal side-channel on Note9 and performed the same training methodology with the CNN, the prediction accuracy achieved by the CNN model after the training is 26.75%. When we used the 400 graphical data for cross-validation the CNN was only able to successfully predict 25.25% (101 out of 400 data). Hence, using DATE to secure the system against thermal side-channel attack such as the one performed in this section, we are able to achieve 9.75% (for training process) and 11.25% (for cross-validation) increase in security.

When we performed the same training on the thermal data collected from Odroid XU4, the CNN achieved a training prediction accuracy of 56.75% when DATE was not implemented on the system. The CNN was also able to predict 52% of the 400 graphical data (208 out of 400) during the cross-validation. After we implemented DATE on the Odroid XU4 the training prediction accuracy achieved by the CNN is 26.75% and was able to predict 29.5% of the 400 data (118 out of 400) during cross-validation. Therefore, using DATE we are able to achieve an increase in security against thermal side-channel by 30% during training period and an increase in security by 22.5%
In order to determine whether our CNN is classifying the thermal data based on the features of the thermal peaks, we utilized Gradient-weighted Class Activation Mapping (Grad-CAM) [40] to visualize in which areas of the graphical data the CNN was focusing on to predict which password is being used for encryption process. Grad-CAM methodology uses the gradient of the target classes flowing into the last convolutional layer to produce a coarse localization map highlighting the important regions in the image (graphical data) for predicting the class label. Fig. 9 shows the thermal graphical data generated while encrypting the plain text using 111111 as password (Fig. 9.(a)) and the subsequent localization mapping created from the last convolutional layer (Fig. 9.(b)) and then portraying the region of interest as thermal map on the original image (Fig. 9.(c)).

5 EXPERIMENTAL AND EVALUATION RESULTS

5.1 Hardware & Software Setup for Experiments

Odroid XU4 could be utilized to run on both Android and Linux operating systems, and hence, we chose to perform most of our experiments on Odroid XU4 running on Linux OS. Further, since Linux is more versatile OS than Android and provides the ability to execute several established benchmark suits such as PARSEC [15] unlike Android, we chose to use Linux for the experimentations provided in this section to show the efficacy and scalability of DATE.

For multi-core systems, multi-threaded applications are heavily used in recent times to represent workloads as they could leverage concurrency and parallel processing. Examples of such applications are available in several benchmarks such as PARSEC [15]. For our experiments we have tried several applications from the PARSEC benchmark such as Streamcluster, Blackscholes, Facesim etc. but to evaluate the effectiveness of our DATE mechanism we chose Blackscholes and Streamcluster with native option because it closely represented a real-world mixed (compute and memory intensive) workload application and the execution period was long enough to observe the thermal behavior in the system. We also evaluated our approach for other real-world workload such as playing a Youtube video on the Chromium browser and RSA [41] encryption and decryption algorithm for 512, 1024, 2048 and 4096 bits. We have run all our experiments on UbuntuMate version 14.04 (Linux Odroid Kernel: 3.10.105).

5.2 Experimental Results

In Fig. 13, 14 and 15 we can see step by step evaluation of Baseline Maximum Thermal Deviation \( (r) \), Spatial Maximum Thermal Deviation \( (\omega) \) and frequency of thermal cycle \( (\theta) \) during execution of the application for different applications using DATE. In Fig. 13 Base T. represents the baseline temperature for different ARM Cortex A-15 CPUs.

Table 1 shows TSMP values for different applications when various resource management methodologies are employed. We evaluated DATE against ondemand and performance governor of Linux and the state-of-the-art methodology proposed by Basireddy et al. [5]. In [5], the researchers have proposed a workload management system, which classifies workloads of the executing applications based on Memory Reads Per Instruction (MRPI) metric and manages DVFS levels of cores based on it.

RSA encryption and decryption was performed for 512, 1024, 2048, 4096 bits for 10 secs for each types. Based on the TSMP values in Table 1 DATE is 4.30% more secure for RSA.
From Eq. 12, we can deduce the MTTF as the amplitude and/or frequency of the thermal cycle can be deduced from the modified Coffin-Manson equation (see Eq. 12) mentioned in [43].

\[ N_{TC}(i) = A_{TC}(\delta T_i - T_{th})^{-b} \exp\left(\frac{E_{a TC}}{T_{maxi}}\right) \]  

In Eq. 12, \( \delta T_i \) represents the maximum thermal amplitude change of the \( i^{th} \) thermal cycle, \( T_{th} \) is the threshold temperature of the component/device at which inelastic deformation begins, \( A_{TC} \) is an empirically determined constant [43], \( b \) is the Coffin-Manson exponent constant, \( E_{a TC} \) is the activation energy and \( T_{maxi} \) is the maximum temperature in the \( i^{th} \) thermal cycle. Therefore, from Eq. 12 we can deduce the MTTF \( (MTTF_{TC}) \) [44] related to thermal cycle \( (N_{TC}) \) as follows:

\[ MTTF = \frac{N_{TC} \sum_{i=0}^{n} t_i}{n} \]  

In Eq. 13, \( t_i \) is the temperature of the component/device at \( i^{th} \) thermal cycle, and \( n \) is the total number (frequency) of thermal cycle. Since, we focused most of the experiments on the Odroid XU4 MPSoC, and if we assume that the number of the thermal cycles \( (N_{TC}) \) that can result in the occurrence of failure due to the \( i^{th} \) thermal cycle is same for the same device platform, then we can easily evaluate the \( MTTF_{TC} \) for each executing application on individual thermal management methodologies. Now, if we take the example of Blackscholes application being executed on the MPSoC using Linux's ondemand governor and assume that \( t_i \) is the baseline maximum thermal deviation i.e. \( t_i = \tau \) since baseline temperature is the same during all the experiments performed during the time of experimentation, then from Fig. 13 and Fig. 15 we could notice that \( t_i (\tau) \) is 20 and \( n (frequency \ of \ thermal \ cycle) \) is 456. Hence, putting the value of \( t_i \) and \( n \) in Eq. 13, we get the value of \( MTTF_{TC} \) as \( \frac{N_{TC} \times 9140}{271} \). Now, if we consider the DATE methodology, where Blackscholes is executed on the Odroid XU4 using DATE, \( t_i \) is 7 (see Fig. 13) and \( n \) is 271 (see Fig. 15), then we get the value of \( MTTF_{TC} \) as \( \frac{N_{TC} \times 9140}{271} \). Therefore, comparing the \( MTTF_{TC} \) of executing Blackscholes using the Linux’s ondemand governor and the DATE, the DATE methodology is 2.85 (approx.) \( (\approx \frac{N_{TC} \times 9140}{271}) \) times more reliable and improve the lifespan of the device over time.

### 5.4 Discussion and Future Direction

For applications with data dependencies over the Internet such as Youtube or applications with workload imbalance between the CPU cores, a possible solution to reduce the Spatial Thermal Deviation is to add noise using software/algorithmic implementation to the temperature variance such that it becomes very difficult to understand the pattern of execution or data being processed on the CPU cores. Here, noise could be regarded as another random execution of secondary tasks in order to keep the CPU temperature high so that temperature dissipated due to execution of the current task could be masked. The main challenge in using such a solution is that to predict when to add the noise in order to mask thermal dissipation of the currently executing task properly.

### 6 Related Work

We have also chosen the state-of-the-art approaches [16–18], which is closely related to our study and address the temperature side-channel attacks on general purpose multi-processor/core devices but not on embedded platforms, and compared the methodologies with the DATE methodology. In the study by Gu et al. [16], (referred to as 3D-TASCS), the scholars have proposed a thermal-aware hardware functional unit that introduces noise to mask activity of encryption and decryption in order to secure against temperature based side-channel attack. Whereas, in the study by Long et al. [17], the researchers have proposed an approach to apply multiple transmitter to one receiver by generating noise to mask temperature behavior on the main transmitter and also establishing a new communication protocol between the transmitter and receiver. In [17], a transmitter is the CPU core, which is executing the main task or set of tasks such as encryption/decryption, encryption and decryption than the Linux Performance Governor. Whereas, DATE is 139.24% more secure for Streamcluster benchmark against temperature based side-channel attacks than the Linux Performance Governor. DATE is also 35.46% more secure than MRPI [5] for the Streamcluster benchmark.

Fig. 17 graphically shows the temperature peaks achieved for the Blackscholes application using DATE, which closely resonates with baseline temperature (see Fig. 1). In comparison, Fig. 16 highlights the temperature peaks achieved for the Blackscholes application while executing on ondemand and performance governors of Linux. From the figures (Fig. 16 and Fig. 17) it is also very evident that DATE is able to achieve the reduction in spatial thermal gradient as well as temporal thermal gradient while the overall operating temperature of the CPUs is also reduced at the same time (also see the histogram comparison in Fig. 18).

### 5.3 Effect on Device Reliability

Thermal gradient (spatial and temporal) and thermal cycling [42] play important role in the reliability of the system in terms of lifespan. The rate of temperature changes on the system affects the lifespan of the device over time due to degradation in the structural integrity and chemical property. More importantly, thermal cycle reduces the whole systems MTTF (Mean-time-to-failure) as the amplitude and/or frequency of thermal cycles increase. The number of the thermal cycles \( (N_{TC}(i)) \) that can result in the occurrence of failure due to the \( i^{th} \) thermal cycle can be deduced from the modified Coffin-Manson equation (see Eq. 12) mentioned in [43].

\[ N_{TC}(i) = A_{TC}(\delta T_i - T_{th})^{-b} \exp\left(\frac{E_{a TC}}{T_{maxi}}\right) \]  

In Eq. 12, \( \delta T_i \) is the maximum thermal amplitude change of the \( i^{th} \) thermal cycle, \( T_{th} \) is the threshold temperature of the component/device at which inelastic deformation begins, \( A_{TC} \) is an empirically determined constant [43], \( b \) is the Coffin-Manson exponent constant, \( E_{a TC} \) is the activation energy and \( T_{maxi} \) is the maximum temperature in the \( i^{th} \) thermal cycle. Therefore, from Eq. 12 we can deduce the MTTF \( (MTTF_{TC}) \) [44] related to thermal cycle \( (N_{TC}) \) as follows:

### Table 1: TSMP values for different methodologies

| App          | OnDemand | Performance | MRPI | DATE |
|--------------|----------|-------------|------|------|
| Blackscholes | 0.000798 | 0.001123    | 0.001792 | 0.003496 |
| Streamcluster| 0.000479 | 0.000450    | 0.000846 | 0.001116 |
| RSA          | 0.001811 | 0.002439    | 0.000912 | 0.002544 |
| Youtube      | 0.001661 | 0.002840    | 0.002906 | 0.003012 |

### Table 2: Thermal cycle reduction comparison with DATE

| App          | OnDemand | Performance | MRPI | DATE |
|--------------|----------|-------------|------|------|
| Blackscholes | 40.57%   | 67.42%      | 46.98% | |
| Streamcluster| 59.59%   | 62.21%      | 28.45% | |
| RSA          | 29.34%   | -2.91%      | 23.34% | |
| Youtube      | 48.15%   | 2.76%       | 1.06%  | |

Note: For data dependent applications over a network such as playing a video on Youtube in Chromium browser, it was still difficult to reduce the Spatial Thermal Deviation due to data dependencies over the Internet or due to workload imbalance between the CPU cores.

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whereas, a receiver is the CPU core, which is establishing the thermal side-channel attack. In the study by Knechtel et al. [18], referred to as thermal side-channel attack. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. where, whereas a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes. In the study by Knechtel et al. whereas, a receiver is the CPU core, which is establishing the applications on different power and mapping schemes.
side channel attack on Samsung Note 9 mobile device utilizing machine learning to release the feasibility of such an attack. Experimental studies evaluated on the Exynos 5422 MPSoC and comparative study with the state-of-the-art proves the efficacy of DATE in securing the device from thermal side-channel attack. Therefore, from experimental evaluation we also proved that DATE is not just effective against temperature side-channel attack but is also effective to enhance reliability in terms of the lifespan of the device.

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