SARVEY PAPER ON HIGH SPEED IIR FILTER USING PIPELINED

Sneha Bhujbal¹ and Suresh Gawande²

¹MTech VLSI Design, Dept. of ECE, Bhabha Engineering Research Institute, Bhopal, Madhya Pradesh, India
²Professor and Head, Dept. of ECE, Bhabha Engineering Research Institute, Bhopal, Madhya Pradesh, India

Abstract—Field-Programmable-Gate-Array (FPGA) based design and implementation of extremely high speed realization of Infinite Impulse Response (IIR) filter. The IIR Filters are being designed using HDL languages since speed is among the chief interest in this era; the main objective is to enhance the speed of the system. In the whole system if the speed of the individual block is enhanced the overall speed of the system is enhanced digital computer arithmetic is an aspect of logic design with the objective of developing appropriate algorithms in order to attain an effective utilization of the available hardware. To generalize its FPGA based design for specific speed up factor, a new efficient simpler approach utilizing Pascal’s Triangle is proposed to calculate the multiplier coefficients of feed-forward and feedback sections of extremely high speed IIR Filter. Since ultimately, speed, power and chip area are the most often used measures of the efficiency of an algorithm, there has a strong link between the algorithms and technology applied for its implementation. Here it is done by applying the technique pipelining. The comparative analysis of pipelined IIR filters is performed by using different FPGA’s. The results reveal that the implemented filters turn in a consistent quality of output.

Keywords- Infinite impulse response (IIR), Pipelining

I. INTRODUCTION

High-performance digital filters are all important to the execution of digital signal processing systems. The speed of a filter realization counts not alone on the potentialities of the hardware platform employed, but as well on the computational structure of the code. In pipeline processing, any operation on a long critical path is broken into levels of smaller, quicker operations, with registers between levels, so as to get a smaller critical path delay. The result is a higher operating frequency and a higher throughput. In a feedback system, viz an IIR filter, the requirement of digital filter to operate at extremely high clock frequency comes when military ESM receiver operating in wide-open configuration needs real-time processing of intercepted radar signal (especially V/UHF band) which is to be extracted by suppressing unwanted communication signals (e.g. FM, Spread Spectrum, Impulse Radar, Impulse Jammer, etc.) in the same band of interest. The filter is very essential to attenuate, if not outright suppress, the unwanted interfering signal in present day communication (GSM) as well as non-communication receivers (e.g. Radar, etc.). Various structures FPGA implementable high speed filters are discussed in literature. The An IIR filter is a recursive filter where the current output proposed design in this paper is an attempt to optimize the depends on previous outputs [5]. The condensed form of the system speed with minimal cost of hardware and software. This extremely high speed comes due to above-stated advanced signal processing techniques. Moreover, other credit goes to enhancement in sampling speed of Analog-to-Digital Converter (ADC). The cost paid for this extremely high speed is increase in latency, silicon area and power consumption in FPGA.

II. LITERATURE SURVEY

A. ADVANTAGES OF IIR OVER FIR FILTER

IIR filters have certain advantages over FIR filters. IIR filter involves feedback which helps to give accurate output. IIR filters make polyphase implementation possible whereas FIR filters cannot. IIR filters require less memory as compare to FIR filters. IIR filters are dependent on both
input and output and consists of both poles and zeros whereas FIR filters have only zeros. FIR filters can only use for the linear phase applications whereas IIR filters can use for non-linear phase applications.

B. INFINITE IMPULSE RESPONSE FILTER

Output from a digital filter is made up from previous stage inputs and previous stage outputs, which uses the operation of convolution. The difference equation for IIR filter which defines how the output signal is related to the input signal is given by

$$y[n] = \frac{1}{a_0} \left( b_0 x[n] + b_1 x[n - 1] + \cdots + b_p x[n - p] a_1 y[n - 1] - a_2 y[n - 2] - \cdots - a_Q y[n - Q] \right)$$

where P = feed forward filter order, bi = feed forward filter coefficients, Q = the feedback filter order, ai = feedback filter coefficients, x[n] = input signal, y[n] = output signal. An IIR filter is a recursive filter where the current output depends on previous outputs. The compressed form of the difference equation is

$$y(n) = \frac{1}{a_0} \left( \sum_{i=0}^{p} b_i x[n - i] - \sum_{j=1}^{Q} a_j y[n - j] \right)$$

III. DESIGN METHODOLOGY

Our proposed work is based on

- Optimizing the basic second order IIR notch filter using the SLA pipelining with power of decomposition-2 and parallel processing of multiplier and adder.
- Implementation on Virtex-5 FPGA for real-time clock signal.

IV. PROPOSED ARCHITECTURE

The basic IIR notch filter structure is as shown in fig 2. The proposed methodology will imply on this basic structure of the IIR notch filter.

Fig 1. Second order IIR notch filter

V. PROPOSED METHODOLOGY

A. PIPELINING

FPGAs offer Intellectual Property (IP) cores as specialized high-speed computational units (e.g., DSP48E in Virtex5 FPGA as multiplier) with a number of internal registers for enabling pipelining operation utilizing those, various possible pipelined structures for the feedback path of the IIR filter are considered and implemented in Virtex-5 FPGA XCV5SX240T-1. It is clear that
forward path pipelining can be performed easily in feed forward loop which is not so in case of feedback path. Hence, criticality of pipelining exists in feedback loop rather than in feed forward loop. The critical path as well as max clock frequency is calculated through Xilinx ISE software.

B. TECHNIQUES

For first order IIR filter Look ahead techniques are present which adds canceling poles and zeros with angular spacing at a distance from origin which is same as that of original pole.

C. LOOK AHEAD PIPELINING WITH OF DECOMPOSITION 2

Scattered look-ahead pipelining can be used to derive stable pipelined IIR filters. Decomposition technique along with scattered look ahead pipelining can also be used to obtain area-efficient implementation for higher-order IIR filters.

In scattered-look-ahead pipelining with power-of-2 decomposition if the transfer function of a recursive digital filter be described by

$$H(z) = \frac{N(z)}{D(z)} = \frac{\sum_{i=0}^{N} b_i z^{-1}}{1 - \sum_{i=1}^{N} a_i z^{-1}}$$

D. FAST ADDER

Adders form an almost obligatory component of every contemporary integrated circuit. The necessary condition of the adder is that it is primarily fast and secondarily efficient in terms of power consumption and chip area. There are various adder topologies present like ripple carry adder, carry look ahead adder, carry save adders, carry select adder etc. out of which we have selected a carry select adder for its low power consumption and lower delay. Fig illustrates the architecture of carry select adder. But carry select adder leads to increase of hardware.

VI. CONCLUSION

In this paper, FPGA based design and implementation methodology of extremely high speed tunable filter is presented. The concept of pipelining with FPGA interface makes the IIR filter to work with effective clock throughput as high . A new efficient and easy technique has been used to calculate the multiplier coefficients of extremely high speed IIR filter using PASCAL triangle. The extremely high speed comes at the cost of increase in latency, FPGA silicon area and power consumption.
REFERENCES

[1] Ravinder Kaur, Ashish Raman, Member, IACSIT, Hardev Singh and Jagjit Malhotra “Design and Implementation of High Speed IIRand FIR Filter using Pipelining” International Journal of Computer Theory and Engineering, Vol. 3, No. 2, April 2011

[2] K.K.Parhi and Messerschmitt, D.G. “Pipelined VLSI recursive filter architectures using scattered look-ahead and decomposition” IEEE Transaction, 11-14 Apr 1988

[3] K.K.Parhi and Messerschmitt, D.G. “Pipeline interleaving and parallelism in recursive digital filters- Part I : pipelining using scattered look ahead and decomposition” IEEE Transactions vol.37, Jul 1989

[4] K.K.Parhi and Messerschmitt, D.G. “Pipeline interleaving and parallelism in recursive digital filters- Part II : pipelined incremental block filtering” IEEE Transactions vol.37, Jul 1989

[5] Magnus Själander and Per Larsson-Edefors “High-Speed and Low-Power Multipliers Using the Baugh-Wooley Algorithm and HPM Reduction Tree”

[6] M. Hatamian, “A 70-MHz 8-bit x 8-bit Parallel Pipelined Multiplier in 2.5-ìm CMOS,” IEEE Journal on Solid-State Circuits, vol. 21, no. 4, pp. 505–513, August 1986.

[7] PramodiniMohanty “An Efficient Baugh-Wooley Architecture for BothSigned & Unsigned Multiplication” International Journal of Computer Science & Engineering Technology (IJCSET)

[8] Jin-HaoTu and Lan-Da Van, “Power-Efficient Pipelined Reconfigurable Fixed-Width Baugh-Wooley Multipliers” IEEE Transactions on computers, vol. 58, No. 10, October 2009.

[9] R.UMA, Vidy Vijayan, M. Mohanapriya, Sharon Paul “Area, Delay and Power Comparison of Adder Topologies” International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.1, February 2012

[10]Rick Decker, Stuart Hirshfield, Pascal’s Triangle: Reading, Writing and Reasoning about Programs, Belmont, California: Wadsworth Pub. Co., 1992.

[11] Kyung Hi Chang; Bliss, W.G.; , "Finite word-length effects of pipelined recursive digital filters," Signal Processing, IEEE Transactions on , vol.42, no.8, pp.1983-1995, Aug 1994.

[12] Xilinx Product Specification ”Virtex-4 Family Overview” (2007).

[13] Sounak Samanta and Mrityunjoy Chakraborty” FPGA Based Implementation of High Speed Tunable Notch Filter Using Pipelining and Unfolding”