Phase-orthogonal FIR filters: An efficient VLSI architecture for communication applications

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Abstract  
90° phase shifters are used in various communication applications such as analytic signal (I and Q) generation, image rejection and Single Side Band (SSB) modulation. In this article, we present an efficient VLSI architecture for the generation of IQ signal with reduced amplitude and phase mismatches using phase-orthogonal FIR phase shifter. The proposed design and implementation reduces the constant multipliers in FIR filter from 2N to N/2 in two steps. In the first step, the filter passband is centered around 0.25fs which makes the alternate filter coefficients zero, reducing the multiplier count to N. In the second step, the hardware architecture is designed in such a way that the time-reversal property of the two filters is exploited to further reduce the multiplier count to N/2. A transpose FIR filter structure with Canonic Signed Digit (CSD) coefficients is adopted for implementation on FPGA. The dual filter approach and the optimization technique has resulted in better filter performance compared to the conventional Hilbert filter approach. The FPGA implementation gives a phase and amplitude ratio error of −0.17° and 0.0002 dB for a filter order of 26 and −0.21° and 0.0053 dB for a filter order of 32 respectively. Despite having two filters, the area increase is only 50% of widely used Hilbert transformer method that uses a single FIR filter. The designed phase shifter is used to simulate an SSB modulator. A side band suppression of 18.9dB is achieved with the proposed phase-orthogonal phase shifter, which is +8 dB better than the Hilbert filter based SSB modulator.

Keywords: IQ signal, FIR filter, amplitude error, phase error, constant multiplier, phase shift, SSB modulator

Classification: Circuits and modules for electronic instrumentation

1. Introduction

Analytic signals I (in-phase) and Q (quadrature) are the signals with no negative frequency components and there are various methods of generating them [1, 2, 3, 4]. The phase and amplitude mismatches between I and Q signal affects the performance a communication system in applications such as single side band (SSB) modulator and image rejection [5, 6, 7, 8]. In time domain, Hilbert transformer is used to achieve 90° phase shift and generate the quadrature signal. Digital filters are designed to perform the transform. The Hilbert filtering approach of generating I and Q is shown in Fig. 1. Practical Hilbert filters does not have flat passband over the entire pass band [9, 10, 11, 12]. Also, delay compensations are required in the other signal path to align the phases of the two signals I(n) and Q(n) so that they are exactly 90° out of phase. In digital platform, FPGAs are used to implement signal processing algorithms for communication applications [13, 14, 15] and it is a prototyping option for ASIC developments [16, 17, 18, 19]. Hilbert FIR filter implementation on FPGA is presented in [9]. On the other hand, identical FIR filters which are matched in gain and having orthogonal phases are ideal for analytic signal generation as shown in Fig. 1b. The filters provide +45° and −45° phase shifts that are effectively 90°. Such FIR filter design algorithms have been proposed in [20, 21, 22]. Though, the dual filter approach is efficient in generating the analytic signals, the hardware cost of the two filters can be expensive as two filters are required.

Area efficient FIR filters using Canonic Signed Digit (CSD), Common Sub Expression (CSE) and Distributed Arithmetic (DA) [23, 24, 25, 26] offers a better filter design solution compared to multiply and accumulate-based approach [27, 28, 29, 30, 31].

In this paper, an efficient VLSI architecture is proposed for the IQ signal generation based on differential filtering. The area optimization is done in two-steps and is implemented both on FPGA and ASIC platform. The performance of the dual filter is compared with the Hilbert filter. Using the proposed phase shifter, a SSB modulator is simulated and the results are reported.

2. Phase-orthogonal FIR filter

Half band low pass FIR filter algorithm [20] with a cut off frequency fc=0.25fs provides 45° phase shift. However, the magnitude response is not flat which is essential for the generation of analytic signals. Moreover, the two filters are arbitrary in nature leading to increase in hardware cost. A phase-orthogonal or quadrature band-pass FIR filters proposed in [21] have identical magnitude responses. The two filters have time reversed coefficients i.e. $B(k)=A(-k)$ and there is no limitation on the order of the filter. The
time reversed characteristics can be exploited to reduce the hardware complexity. In this paper, the FIR filter algorithm proposed in [21] is used to design the 45° phase shifters.

2.1 Design of phase-orthogonal or quadrature FIR filters

Two filters $A(k)$ and $B(k)$ are designed that are identical in magnitude and whose phases are orthogonal. The in-phase filter $A(k)$ characteristics is shown in Eq.(1). $A(k)$ is found by sampling Eq.(1) at time intervals equal to $t = 2\pi (k - N - 1/2)$

$$A(t) = \begin{cases} \sqrt{2}(\omega_2 - \omega_1), t = 0 \\ a \sin \left( \frac{\pi}{4} \left( \frac{a + 2a}{a} \right) \right) - a \sin \left( \frac{\pi}{4} \left( \frac{a + 2a}{a} \right) \right), t = \pi \alpha \\ a \sin \left( \frac{\pi}{4} \left( \frac{a - 2a}{a} \right) \right) - a \sin \left( \frac{\pi}{4} \left( \frac{a - 2a}{a} \right) \right), t = -\pi \alpha \\ \frac{2a^2 \cos(\alpha \pi)}{t(4a^2 - \pi^2)} \left[ \sin(\omega_1 t + \pi/4) - \sin(\omega_2 t + \pi/4) \right], \text{ otherwise} \end{cases}$$

(1)

In the first step of optimization, $N$ is chosen to be even and the pass band is centered around 0.25fs to make the alternate coefficients of the filter zero. The total number of number of multiplications reduces from $2N$ to $N$. The following specifications are used to design the FIR filters.

1) Filter order: 26,32
2) Pass band (normalized): Centered around 0.25fs
3) Two half amplitude points $\omega_1 = 0.05$ and $\omega_2 = 0.452$
4) Filter type : Time reversed response

An Hilbert FIR filter is also designed to compare the magnitude responses and the specifications are adapted from [9]. The specifications of Hilbert FIR filter used for the design is as follows

1) Filter order: 27,33
2) Stop band attenuation :30 dB
3) Pass band (normalized): 0.1-0.9
4) Filter type : Negative symmetry

The Hilbert FIR filter coefficients are asymmetric and the magnitude response in Fig. 2 shows ripples of order 0.08dB. Fig. 3 shows the frequency response of phase-orthogonal FIR filter. It is seen that the filter has flat magnitude response without ripples. The phase error in the flatband region is ±0.3°. As the phase-orthogonal FIR coefficients are time reversed, $B(K)$ is found by reversing $A(k)$.

3. SSB modulation

The phase-orthogonal filter designed can be used for communication applications such as SSB, image rejection etc. Fig. 4 shows SSB modulation scheme using phase shift method. The Hilbert transformer generates a 90° phase shift of the message signal $m[n]$. Then, $m[n]$ and the phase shifted version $m'[n]$ are mixed with local oscillator signals. The mixer outputs are added or subtracted to cancel the one of the side bands. Before mixing, $m[n]$ is delayed by $(N - 1)/2$ to align the phases of the two signals so that the phase difference is 90°. Using Hilbert filter, the amplitudes of the two signals cannot be matched as there are ripples in the passband. Instead of using 90° phase shifter, differential phase

Fig. 2 Magnitude response of Hilbert FIR filter ($N=27$)

Fig. 3 Magnitude response and phase difference of phase-orthogonal FIR filters ($N=26$). Inset shows the flat magnitude and phase errors

(a) SSB modulation using Hilbert transformer ($N=27$)

(b) SSB modulation using differential filter ($N=26$)
shifters that shifts $45^\circ$ and $-45^\circ$ can be used, and because of the fact they are perfectly matched in magnitude and phase, the SSB modulator performance can be improved. Simulation of Fig. 1 gives 89.6° and 89.9° for Hilbert transformer and phase-orthogonal filters respectively. The SSB modulator is simulated with 1 KHz message signal and a local oscillator frequency of 5 KHz is used for mixing operation. The mixer outputs used are 4 KHz and 6 KHz. The spectrum of SSB for both the approaches are shown in Fig. 5. The phase-orthogonal filter approach gives a suppression of 18.9 dB and the Hilbert filter approach gives a suppression of 10.9 dB. An increase in 8 dB of suppression is obtained for the phase-orthogonal filter approach and is effective in cancelling one of the sideband. The magnitude of the phase orthogonal filter is less than the Hilbert filter. This is due to the choice of sampling frequency used to maximize the suppression of one of the sideband. For Hilbert filter, the message signal is well within the passband and for the FIR filter pair, it is at the edge of the passband. However, the use of two filters increases hardware cost. The following section gives the optimization of area for the phase-orthogonal filters.

4. FPGA architecture

The hardware architecture of the phase-orthogonal filters of order $N$ is shown in Fig. 6. The hardware complexity is reduced by eliminating the multipliers. The filter coefficients are converted to CSD codes [21]. While converting the filter coefficients to CSD codes, a precision of 12 bits is used. The asymmetrical property of the Hilbert transform and time-reversal property of the phase orthogonal filters are exploited to reduce the number of arithmetic operations.

In the second step of optimization, a transposed FIR filter structure (TDF) is adopted as it is efficient for FIR filters with CSD coefficients. In the TDF structure, the multipliers multiply the input and the filter coefficients after which the signal is delayed by a clock cycle and then added. As the coefficients of Filter $Q$ is the reverse order of the Filter $I$, dedicated multipliers are not required for each filter. The multipliers can be shared bringing the count to $N/2$. These $N/2$ multipliers are replaced by CSD multipliers. The CSD multiplier block has a set of shifters and coefficient adder/subtractor block. Filter $I$ and Filter $Q$ consists of tap adders and delays.

4.1 CSD multiplier

This block implements the CSD multiplication and is common for both the filters; Filter $I$ and Filter $Q$. As the CSD precision used is 12 bits, the shifter block contains 12 shifters that shifts from $2^{-1}$ to $2^{-12}$. The input data width used is 14 bits. The two extra bit precision is to avoid zero while performing the shift operation. The selected shifted outputs are added or subtracted according to the coefficient value to get the CSD multiplication result.

4.2 Filter $I$ and $Q$ block

Dedicated adders and delays are required in the filter $I$ and $Q$ blocks, the right outputs from the two CSD multipliers are added, delayed and passed to the next tap adder. The architecture of the phase-orthogonal FIR filters for $N=6$ is shown in Fig. 7. There are only three filter coefficients indicated as $h(n)$ as the alternate coefficient values are zero. As the filters are time reversed, $A(0)=B(5)=h(0)$, $A(2)=B(3)=h(2)$ and $A(4)=B(1)=h(4)$. The actual number of multipliers required is only 3 for both the filters. For order $N$, the number of multipliers reduces from $2N$ to $N/2$.

Virtex-4 FPGA device is used to implement the filters. A sinusoidal input signal of 10 MHz is used and the error per-
formance of the filters are calculated. The phase-orthogonal filters with multiplier is also implemented to validate the effectiveness of CSD multipliers. The architecture of Hilbert FIR filter (N=27) is shown in Fig. 8 is also implemented. The architectures are clocked at the rate of 100 MHz. Also, the filters are implemented in ASIC in 65 nm technology. The ASIC implementation of dual filter is shown in Fig. 9. The area required for the dual filter is 144\(\mu\)m \(\times\) 156\(\mu\)m.

5. Results and discussions

Two phase-orthogonal FIR filters with \((N=26\text{ and }N=36)\) are designed and implemented on Virtex-4 FPGA. Table I gives the performance comparison of three various architectures implemented on FPGA. The phase-orthogonal FIR filters implemented using multipliers has the lowest amplitude error. However, the presence of multipliers increases the hardware complexity. The CSD phase-orthogonal filters have a phase error of \(-0.17^\circ\) and \(-0.21^\circ\) and amplitude ratio error of 0.0002 dB and 0.0053 dB for 26 tap and 32 tap respectively. The IQ signals generated by the dual filter has very less mismatches compared to Hilbert transform method. Table II gives the area requirement of the two approaches on ASIC platform in 65 nm. The clocking frequency of CSD Hilbert transform is better than the phase-orthogonal filters. As filter order chosen is not same, for comparison area per tap is calculated. The CSD Hilbert filter requires 0.5426 \(\mu^2\)tap and 0.8726 \(\mu^2\)tap is needed for phase-orthogonal filters. The area required for the CSD phase-orthogonal filter is 144\(\mu\)m \(\times\) 156\(\mu\)m. Despite having two filters, the area increase is only 50% of widely used Hilbert transformer that uses a single FIR filter. Also, SSB modulator simulated using phase-orthogonal filters gives an increase in 8 dB of suppression for one of its side bands.

6. Conclusion

A dual filter method is proposed to generate IQ signals with very low amplitude and phase mismatches. Two FIR filters having identical magnitude response and orthogonal phases are used to obtain 45° and 45° phase shifts. The proposed phase shifter results in low IQ mismatches compared to Hilbert transform method. A two-step optimization technique is presented combining the advantages of time reversal property of the phase-orthogonal FIR filters, centering the pass-band at 0.25fs and eliminating the constant multipliers. For the dual filter architecture, the number of constant multipliers required reduced from \(2N\) to \(N/2\). The hardware implementations on FPGA shows better performance and the ASIC implementation shows that an additional 50% increase in area is required for the phase-orthogonal FIR filters. The SSB modulator simulated using the proposed deferential filtering gives an increase in 8 dB of suppression for one of its side bands.

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