Advances in La-Based High-k Dielectrics for MOS Applications

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Received: 3 March 2019; Accepted: 25 March 2019; Published: 27 March 2019

Abstract: This paper reviews the studies on La-based high-k dielectrics for metal-oxide-semiconductor (MOS) applications in recent years. According to the analyses of the physical and chemical characteristics of La2O3, its hygroscopicity and defects (oxygen vacancies, oxygen interstitials, interface states, and grain boundary states) are the main problems for high-performance devices. Reports show that post-deposition treatments (high temperature, laser), nitrogen incorporation and doping by other high-k material are capable of solving these problems. On the other hand, doping La into other high-k oxides can effectively passivate their oxygen vacancies and improve the threshold voltages of relevant MOS devices, thus improving the device performance. Investigations on MOS devices including non-volatile memory, MOS field-effect transistor, thin-film transistor, and novel devices (FinFET and nanowire-based transistor) suggest that La-based high-k dielectrics have high potential to fulfill the high-performance requirements in future MOS applications.

Keywords: lanthanum oxide; high-k dielectric; metal-oxide-semiconductor

1. Introduction

As the complementary metal-oxide-semiconductor (CMOS) technology is continually approaching the giga-scale in terms of integration level, the MOS devices have to be scaled to the nano-scale. According to the roadmap on the development of the semiconductor industry, the key geometric parameters for several technology nodes calculated by the technology rules are listed in Table 1 [1]. However, the minimum thickness of SiO2 as a gate dielectric is ~0.7 nm because at least two layers of neighboring oxygen atoms are needed to prevent the gate/SiO2 and SiO2/Si interfaces from overlapping with each other [2]. However, practically, for SiO2 dielectrics thinner than 3 nm, the gate leakage is too large for applications because direct tunneling of charge carriers occurs [3,4]. Figure 1a is an example of gate leakage increasing significantly with the decrease of dielectric thickness [5], where for a 1.5 nm oxide film, the unacceptable gate leakage exceeds 100 A/cm² at 2 V. Figure 1b shows the factors that contribute to the gate leakage current of MOS devices, including Fowler-Nordheim tunneling [6], Poole-Frenkel tunneling [7,8], trap-assisted tunneling [9,10], and direct tunneling [11]. Among them, direct tunneling has the closest relation with the thickness of the gate dielectric, and its current can be calculated as:

$$J_{DT} = J_0 \left(1 - \frac{V_{ox}}{\Phi_B}\right) \exp\left\{ -\frac{3 \sqrt{2m^* q T_{ox} \Phi_B}}{h} \frac{V_{ox}^{3/2}}{\Phi_B} \left[1 - \left(1 - \frac{V_{ox}}{\Phi_B}\right)^{3/2}\right]\right\}.$$
where \( J_0 \) is a constant, \( V_{ox} \) is the voltage drop of the dielectric, \( \Phi_B \) is the barrier height, \( m^* \) is the electron effective mass in the dielectric, \( h \) is the reduced Planck’s constant, and \( T_{ox} \) is the dielectric thickness. Obviously, the direct tunneling current increases exponentially with the decrease of \( T_{ox} \). Therefore, the replacement of \( \text{SiO}_2 \) by an alternative material with higher dielectric constant (k) allows the use of larger physical thickness for the same oxide capacitance, and so the tunneling current can be suppressed.

### Table 1. Key geometric parameters for several technology nodes [1].

| Gate Length (nm) | 22 | 16 | 11 | 8 |
|------------------|----|----|----|---|
| Dielectric thickness (nm) | 0.8 | 0.6 | 0.4 | 0.3 |
| Junction depth (nm) | 11.0 | 8.0 | 5.5 | 4.0 |
| Channel depletion thickness (nm) | 11.0 | 8.0 | 5.5 | 4.0 |

**Figure 1.** (a) Gate leakage current for nMOSFETs with different gate dielectric thicknesses [5], and (b) energy band diagram of an nMOS structure showing major tunneling mechanisms.

The first high-k material studied is silicon oxynitride (\( \text{SiO}_x\text{N}_y \)). By annealing in \( \text{NH}_3 \) or other gases containing nitrogen (N), effective N incorporation is achieved in \( \text{SiO}_2 \) to improve its thermal and high-field reliability [12]. Besides, reports show that N doping is capable of reducing oxide charges and border traps [13]. However, \( \text{SiO}_x\text{N}_y \) could no longer meet the requirement of gate leakage during scaling down in the ITRS report in 2007, and so novel high-k materials as gate dielectrics had to be explored. According to Figure 2, that demonstrates the dielectric constants of promising candidates for MOS devices together with their band gaps and conduction-band offsets (CBO) with Si and GaAs [14,15], inverse trends in the variations of \( E_g \) and CBO with the k value can be found. Therefore, in order to reach a balance in this trade-off, apart from possessing a high k value, sufficiently large \( E_g \) (usually > 5 eV) and CBO with the substrate (usually > 1 eV) to minimize carrier injection should also be required. Besides, thermal stability is an additional criterion for choosing proper high-k dielectrics: large Gibbs free energy to inhibit the reaction with the Si substrate and small oxygen diffusion coefficient to suppress the formation of low-k \( \text{SiO}_x \) interfacial layer during high-temperature processing steps are essential [16,17].
was proved to be an excellent gate dielectric for TFT [21]. However, its low k value limits its further use with Si than SiO₂, HfO₂ is still far from being ideal. Therefore, measures including post-deposition annealing (PDA) and nitrogen incorporating and doping of Si, Al, La, etc. to form ternary oxides have been tried with good results achieved [19]. In the past decade, much efforts have been made to study novel high-k dielectrics in a variety of semiconductor devices, and hundreds of reports have shown the high potential of high-k gate dielectrics for application in the CMOS and VLSI technologies. For example, Al₂O₃, ZrO₂, Ta₂O₅, and Al-doped TiO₂ have been proved to be promising candidates for DRAM. Hf- and Zr-based ternary oxides have been widely used in MOSFET, FinFET, etc. [20]. Recently, flexible and stretchable electronics has become a hotspot for applications such as flexible displays, wearable sensors and electronic skins. Therefore, massive studies have been made on thin-film transistors (TFTs) with flexible/stretchable substrates. At the beginning, Al₂O₃ was proved to be an excellent gate dielectric for TFT [21]. However, its low k value limits its further applications. So, research interests moved to composite/stack layers involving materials with higher k values such as Ga₂O₃, Hf-/Zr-based ternary oxides/oxynitrides, rare-earth oxides, and perovskites [22]. Speaking of perovskites, their super-high k value (300–6000) makes them stand out in high-k dielectrics, among which SrTiO₃ and BaTiO₃ are the most representative dielectric perovskite oxides. However, the phase of perovskite is critical because most perovskite oxides are insulators in the cubic phase while variation in crystallinity induces metallic, superconducting, ferroelectric, and ferromagnetic properties [23]. Therefore, the deposition of perovskite oxides as dielectrics in MOS applications is the main issue. Then, the idea of using perovskite nanocrystals or nanocomposites has been proposed. Firstly, self-assembled BaTiO₃ and (Ba, Sr)TiO₃ nanocrystals have been tried on pentacene TFT with a mobility of 0.35 cm²·V⁻¹·s⁻¹ [24]. Synthesized BaTiO₃ has also been studied with a k value of 4000 achieved [25]. Moreover, a study on BaTiO₃/polypropylene nanocomposites showed a rubber shell of nano-scaled BaTiO₃ could promote the compatibility and dispersion of nano-particles in polypropylene matrix and also improve the dielectric and tensile properties of nanocomposites [26]. However, the uncertainty in the phase of perovskite oxide is still limiting the performance of relevant MOS devices.

![Dielectric constant vs. (a) band gap and (b) conduction band offsets with Si and GaAs for promising materials as gate dielectrics [14,15].](image)

Through comprehensive consideration of the pertinent requirements for high-k gate dielectrics, following SiO₃N_y, hafnium (Hf)-based materials attracted much attention and were successfully introduced into production in 2007, with the TEM images of a PMOS transistor and its MOS gate stack shown in Figure 3 [18]. However, owing to lower thermal stability and lower interface quality with Si than SiO₂, HfO₂ is still far from being ideal. Therefore, measures including post-deposition annealing (PDA) and nitrogen incorporating and doping of Si, Al, La, etc. to form ternary oxides have been tried with good results achieved [19]. In the past decade, much efforts have been made to study novel high-k dielectrics in a variety of semiconductor devices, and hundreds of reports have shown the high potential of high-k gate dielectrics for application in the CMOS and VLSI technologies. For example, Al₂O₃, ZrO₂, Ta₂O₅, and Al-doped TiO₂ have been proved to be promising candidates for DRAM. Hf- and Zr-based ternary oxides have been widely used in MOSFET, FinFET, etc. [20]. Recently, flexible and stretchable electronics has become a hotspot for applications such as flexible displays, wearable sensors and electronic skins. Therefore, massive studies have been made on thin-film transistors (TFTs) with flexible/stretchable substrates. At the beginning, Al₂O₃ was proved to be an excellent gate dielectric for TFT [21]. However, its low k value limits its further applications. So, research interests moved to composite/stack layers involving materials with higher k values such as Ga₂O₃, Hf-/Zr-based ternary oxides/oxynitrides, rare-earth oxides, and perovskites [22]. Speaking of perovskites, their super-high k value (300–6000) makes them stand out in high-k dielectrics, among which SrTiO₃ and BaTiO₃ are the most representative dielectric perovskite oxides. However, the phase of perovskite is critical because most perovskite oxides are insulators in the cubic phase while variation in crystallinity induces metallic, superconducting, ferroelectric, and ferromagnetic properties [23]. Therefore, the deposition of perovskite oxides as dielectrics in MOS applications is the main issue. Then, the idea of using perovskite nanocrystals or nanocomposites has been proposed. Firstly, self-assembled BaTiO₃ and (Ba, Sr)TiO₃ nanocrystals have been tried on pentacene TFT with a mobility of 0.35 cm²·V⁻¹·s⁻¹ [24]. Synthesized BaTiO₃ has also been studied with a k value of 4000 achieved [25]. Moreover, a study on BaTiO₃/polypropylene nanocomposites showed a rubber shell of nano-scaled BaTiO₃ could promote the compatibility and dispersion of nano-particles in polypropylene matrix and also improve the dielectric and tensile properties of nanocomposites [26]. However, the uncertainty in the phase of perovskite oxide is still limiting the performance of relevant MOS devices.
Then, rare-earth oxide as a high-k dielectric has been studied, and La₂O₃ is a representative that has attracted much attention in recent years due to its high k value (~27) [27], large band gap (5.8–6.0 eV) [28], high breakdown field (> 13 MV/cm) [29], low leakage current for small effective oxide thickness (EOT) [30], good thermodynamic stability, and good high-field reliability on Si [30,31]. Based on the WKB approximation, the direct tunneling currents of ideal MOS structures with different dielectrics were modeled and simulated by H. Wu, et al., with results demonstrated in Figure 4 [32]. Significant gate leakage decrease is achieved by replacing SiO₂ with high-k materials, among which La₂O₃ has the lowest leakage current. Besides, unlike perovskites, high-quality La₂O₃ film can be easily deposited by sputtering, ALD, PVD, E-beam, etc. These make La-based high-k materials highly promising for MOS applications.

![Figure 3](image3.png)  
*Figure 3.* TEM images: (a) pMOS transistor and (b) MOS gate stack with Hf-based high-k gate dielectric [18].

![Figure 4](image4.png)  
*Figure 4.* Gate leakage vs. (a) gate voltage and (b) equivalent oxide thickness for ideal MOS devices with different gate dielectrics [32].

However, besides the crystallization temperature (~500 °C) of La₂O₃ [19] not being high enough for high-temperature processing during fabrication, its hygroscopicity and defects [31,33] are the main concerns for MOS applications. Therefore, similar to HfO₂, treatments including nitrogen incorporation and metal doping are necessary for La₂O₃ to improve its oxide quality. So, based on the advantages of La₂O₃ over other high-k materials and with the motivation of providing guidelines for making good use of La-based high-k materials to improve the performance of MOS devices for meeting the requirements of the technology nodes in the future, this review focuses on the advances of La-based high-k dielectrics in MOS applications. To have a better understanding of the characteristics...
of the La-based films; the basic theories for the main concerns of La$_2$O$_3$ as gate dielectric and the proposed solutions to these problems are discussed in Section 2, including the hygroscopicity of La$_2$O$_3$, the defects in La$_2$O$_3$, and the mechanisms for the effects of La in La-based ternary oxides. Then, the advances of the MOS applications with La-based high-k dielectrics are reviewed in Section 3 to provide a whole picture on the developments and advantages of La-based high-k dielectrics in MOS devices. The applications in Section 3 include non-volatile memory, MOSFET, TFT, Ge and III-V compound semiconductor devices, and novel MOS devices (e.g. FinFETs and nanowire FETs) because these are the main devices that need high-k dielectrics for high-performance MOS applications in the future. At last, a brief conclusion is made in Section 4 based on the discussions in Sections 2 and 3, and future studies are proposed to give directions to the developments of MOS devices with La-based high-k dielectrics.

2. Characteristics of La-Based High-k Dielectrics

2.1. Hygroscopicity of La$_2$O$_3$

As mentioned above, theoretically, the k value of La$_2$O$_3$ is ~27, but lower k values, even below 10, were found in early studies [34–36]. One important reason is the hygroscopic nature of La$_2$O$_3$, whose high ionicity leads to a direct reaction with H$_2$O:

$$\text{La}_2\text{O}_3 \rightarrow 2\text{La}^{3+} + 3\text{O}^{2-},$$
(2)

$$\text{H}_2\text{O} + \text{O}^{2-} \rightarrow 2\text{OH}^{-},$$
(3)

Experimental results [37] showed that after exposure to air for 12 h, the root-mean-squared (RMS) surface roughness of La$_2$O$_3$ increased from 0.5 to 2.4 nm (Figure 5a), which was probably caused by the non-uniform moisture absorption of the La$_2$O$_3$ film that led to a non-uniform volume expansion. Apart from the surface roughness, increases in physical thickness and thus capacitor equivalent thickness (CET) occurred as shown in Figure 5b which should be ascribed to the lower density of hexagonal La(OH)$_3$ (4.445 g/cm$^3$) than that of hexagonal La$_2$O$_3$ (6.565 g/cm$^3$). The obvious increase of CET resulted in a significant degradation in k value from 20 to 7 (Figure 5b). Besides, this moisture absorption further affected the electrical properties of MOS devices. Figure 5c demonstrates that the flat-band voltage ($V_{fb}$) shift and hysteresis of an MOS capacitor with La$_2$O$_3$ gate dielectric increase with exposure time, implying that negative charges and traps are induced near/at the La$_2$O$_3$/Si interface [38].

A lot of effort has been made to enhance the hygroscopic resistance of La$_2$O$_3$ so that its advantages as a gate dielectric can be made use of. The most widely used method is incorporating a second metal element to form a ternary oxide. The rate of the reaction between a metal oxide (M$_x$O$_y$) and moisture (H$_2$O) can be evaluated by the Gibbs free energy change ($\Delta G$) [39]. A negative $\Delta G$ means the system energy decreases after the reaction, implying that the reaction has a high possibility to occur, and so a more positive $\Delta G$ is more promising for the corresponding high-k material to suppress the hygroscopicity of La$_2$O$_3$ [37,40]. For example, in Ref. [37], Y incorporation exhibited obvious improvement in the moisture resistance of La$_2$O$_3$, as shown in the inset of Figure 6, where for Y concentration higher than 40%, the degradation in k value after exposure in air is negligible. Apart from the materials in Figure 6, Ta and Nb have also been proved to be promising dopants to improve the hygroscopic resistance of La$_2$O$_3$ by surface morphology and XPS analysis, which showed that the La–OH peak significantly decreased with increasing Ta and Nb contents in TaLaO [41] and NbLaO [42], respectively.
Another method is post-deposition ultraviolet (UV) ozone treatment using an Hg vapor UV lamp that primarily emits light with wavelengths of 185 and 254 nm [43]. The UV ozone treatment is compared with thermal N₂ and O₂ treatments in Figure 7. Obviously, the O₂ + N₂ annealing can inhibit the moisture absorption of La₂O₃ by a large extent, but the N₂ annealing together with the UV ozone treatment keeps the La₂O₃ surface roughness almost unchanged after exposing to air for 24 h.
Defects in La$_2$O$_3$

Although high-k dielectrics can keep the trend of device scaling, their higher density of bulk defects and poorer interface with Si than SiO$_2$ results in degradation in carrier mobility, thus making the device performance unsatisfactory [44–46]. As shown in Figure 8a, fixed charge, oxide trap, interface trap, interfacial dipole, and surface roughness are the factors that lead to Coulomb, phonon and surface-roughness scatterings (in Figure 8b), which govern the effective carrier mobility of MOS devices at low, moderate and high gate fields respectively. The origins of these scatterings are: Firstly, the defects in high-k oxide bulk cause charge trapping and lead to higher bias instability and unreliability [47]; secondly, optical phonons in high-k oxides have a low-lying soft polar mode which results in the remote scattering of channel carriers [48]. Besides, the larger surface roughnesses of high-k dielectrics with both the Si substrate and the gate than those of SiO$_2$ should be ascribed to the interaction between high-k elements with the Si substrate and the longer metal–O and metal-Si bonds than the Si–Si bond.

![Figure 7. Roughness of La$_2$O$_3$ with different post-deposition treatments vs. exposure time in air][43]

**Figure 5.** Impact of the hygroscopicity of La$_2$O$_3$ on (a) surface morphology, (b) the hygroscopic resistance of La$_2$O$_3$ by surface morphology and XPS analysis, which showed that the La–OH peak significantly decreased with increasing Ta and Nb contents in TaLaO$_3$ and NbLaO$_3$, respectively. [42].

**Figure 7. Roughness of La$_2$O$_3$ with different post-deposition treatments vs. exposure time in air [43].**

![Figure 8. (a) Schematic diagram demonstrating the origins of mobility degradation in MOSFET. (b) Factors that impact carrier mobility.][52]

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obtained by the first-principle calculations based on the total energy plane wave pseudopotential code CASTEP [50], with the band structure of La₂O₃ with neutral V̄O shown in Figure 9b as an example [51]. Four-fold V̄O has all five charged states including 2−, 1−, 0, 1+, and 2+. However, since high coordination prevents distortion from creating an extra gap state, the six-fold V̄O only consists of 0, 1+, and 2+ states. Obviously in Figure 9a, all the V̄O states in La₂O₃ are located above the band gap of Si, which differs from the case of HfO₂. The neutral V̄O state in HfO₂ is below the conduction band of Si [52], and so can be filled by the electrons injected from the silicon substrate, leading to a positive shift in the capacitance-voltage (C–V) curve [53]. J. X. Zheng, et al. calculated the concentrations of V̄O and oxygen interstitial (Ō) in La₂O₃ based on the density functional theory in the generalized gradient approximation using the projector augmented wave method, with results shown in Figure 9c [54].

For HfO₂, the concentrations of positively-charged oxygen vacancy and negatively-charged oxygen interstitial are too low (<10¹² cm⁻³) to significantly affect the device performance. However, for La₂O₃, the concentrations of V̄O²⁺ and Ō²⁻ are higher than 10¹⁶ cm⁻³, and so, apart from neutral V̄O, charged V̄O and Ō can also be the sources of charge trapping.

Figure 9. (a) Energy levels of four-fold and six-fold oxygen vacancies in La₂O₃ [49], (b) band structure of La₂O₃ with neutral oxygen vacancies [51], and (c) defect concentration in La₂O₃ at 1300 K [54].

Trap at the La₂O₃/semiconductor interface is another concern that impacts the device performance. La has been reported to easily react with semiconductor substrates such as Si and Ge to form a low-k interfacial layer (IL). As illustrated in Figure 10a, the thickness of the IL can be comparable to the thickness of the La₂O₃ bulk, which significantly decreases the effective k value of the dielectric and thus increases the EOT [55, 56]. As shown in Figure 10d, post-deposition annealing can enhance this reaction because an obvious increase in the La-silicate peak can be found for higher annealing temperature [57]. However, a tradeoff exists between the k value and the interface-trap density (Dit), according to
Ref. [56]. As the thickness of the IL (with a k value of 5.8) increases from 0.7 to 3.0 nm, $D_0$ decreases by almost two orders but the effective k value of the dielectric is reduced by ~70%. With a La-silicate IL, the interface states are depicted in Figure 10b [58]. It is known that La$_2$O$_3$ has an ionic bonding nature while the bond in the La-silicate layer is more covalent, thus creating a larger amount of oxygen vacancies at the La$_2$O$_3$/Si interface [59]. It has been reported that charge-pumping measurement can be used to detect the interface traps between ionic HfO$_2$ and covalent SiO$_2$, and so the traps located at the La$_2$O$_3$/La-silicate interface can be considered as slow states [60]. Figure 10c shows the density of this slow state ($D_{\text{slow}}$) together with $D_0$ calculated based on the measured conductance of the La$_2$O$_3$-gated MOS capacitor, with $D_{\text{slow}}$ much higher than $D_0$ and almost distributed uniformly in the Si band gap [58].

Besides, the grain-boundary state created by the crystallization of high-k material during high-temperature treatments is another kind of defect that induces shallow traps. Figure 10e shows the XRD patterns of La$_2$O$_3$ and LaON after annealing, and the weaker peak of LaON than that of La$_2$O$_3$ indicates that nitrogen incorporation can suppress the crystallization of La$_2$O$_3$ [61]. Apart from increasing the crystallization temperature, N incorporation is also capable of increasing the k value and reducing the border traps in the dielectric [62]. For many years, in order to decrease the defect density of the La$_2$O$_3$ gate dielectric, many efforts have been made, including high-temperature annealing, N incorporation, F or NH$_3$ treatment, doping other high-k metal elements to form complex oxides (e.g. LaYO [37], LaTaO [41]), and addition of an interfacial passivation layer (e.g., Al$_2$O$_3$ [27]). However, because of the trade-off between the k value and the dielectric/semiconductor interface quality, there is still ample room to improve the device performance

### 2.3. Effects of La on La-doped Ternary Oxides

As mentioned in the previous section, doping other high-k metal elements into La$_2$O$_3$ is capable of enhancing the device performance. It has been reported that doping La into other high-k materials
can also achieve improvements, and the most important effect of La doping is to passivate the oxygen vacancies in other high-k binary oxides. After several reports showing that La incorporated in HfO$_2$ could significantly improve the device performance [53–66], X. P. Wang et al. proposed that this improvement should be ascribed to the reduction of oxygen vacancies (V$_O$) in HfLaO [66]. Therefore, several studies on the physics of this phenomenon have been made and confirmed the V$_O$ passivation role of La as discussed below.

The relaxed structures of V$_O$ in HfO$_2$ and HfLaO were obtained by first-principle calculation based on the density-functional theory using a generalized gradient approximation (Figure 11a) [67], according to which the formation energies of V$_O$ near La and far from La were calculated to be 6.29 and 5.73 eV respectively, both larger than the V$_O$ formation energy of HfO$_2$ (5.58 eV), indicating that it is more difficult to form V$_O$’s after La incorporation. The reason for this increased V$_O$ formation energy by La incorporation can be explained by Figure 11b, with the contour plots for the wave functions corresponding to the V$_O$-related states. Although electrons are trapped in V$_O$ in both HfO$_2$ and HfLaO cases, the electron distribution around V$_O$ of HfO$_2$ differs from that of HfLaO. Since the La–O bond is 76% ionic and higher than Hf–O (70%) according to the Pauling’s electronegativity theory, electrons from the O2p states are localized at the O sites beside the La atoms, thus reducing the interaction between La5d and O2p when compared to that between Hf5d and O2p. Therefore, in Figure 11b, unlike in HfO$_2$, the oxygen atom nearest to La atoms does not contribute to the gap state at all [67]. Moreover, D. Liu et al. analyzed the band structures of HfO$_2$ and HfLaO with V$_O$’s and concluded that La was capable of passivating V$_O$’s in HfO$_2$ and ZrO$_2$ by shifting the vacancy gap into the conduction band, thus suppressing the Fermi-level pinning at the dielectric/Si interface as shown in Figure 11c [68].

In the case of pure HfO$_2$, oxygen tends to diffuse to the Si substrate and leaves a positive V$_O$ by releasing two electrons that fall down to the Fermi level of the metal gate. However, if a thin La$_2$O$_3$ layer lies on the HfO$_2$ dielectric, La can easily diffuse into HfO$_2$ under high-temperature annealing [69] and then the substitution of Hf by La creates holes in the valence band (VB). Therefore, in this case, the oxidation of Si drives this substitution without releasing electrons, and the VB holes are filled by the electrons in the conduction band to prevent the formation of V$_O$ states in the band gap.

![Figure 11](image_url)

Figure 11. For HfO$_2$ and HfLaO: (a) relaxed structure of oxygen vacancies V$_O$ [60], (b) contour plot of wave function corresponding to the V$_O$-related gap states [60], and (c) schematic band diagram showing oxygen vacancies [68].
Apart from oxygen-vacancy passivation, La incorporation has also been reported to be able to modify the flatband voltage (VFB) of the gate stack in nFETs [69,70] and so shift their threshold voltages (Vth). An obvious negative shift of VFB for HfLaO-gated MOS capacitor with increasing La concentration can be found in Figure 12a, and the effective work function (EWF) decreases by about 0.5 eV for the La content rising from 20% to 60% [71]. Recently, the EWF shift due to La incorporation into HfO2 has been found to be linearly dependent on the La concentration, with −53 meV per 1014 atoms/cm2 [72]. This should be ascribed to the formation of a dipole layer at the HfLaO/SiO2 interface as shown in the inset of Figure 12b and the VFB shift can be calculated by:

$$\Delta V_{FB} = -\left(\frac{Qd_1}{k_{SiO_2}} + \frac{Qx}{k_{HfLaO}}\right) + \frac{Q(x - d_2)}{k_{HfLaO}} = -Q\left(\frac{d_1}{k_{SiO_2}} + \frac{d_2}{k_{HfLaO}}\right)$$  \hspace{1cm} (4)

where Q is the areal charge density in the dipole layer, d1 and d2 are the widths of dipole layers on the SiO2 and HfLaO sides, kSiO2 and kHfLaO are the k values of SiO2 and HfLaO, and x is the thickness of the HfLaO layer. Since an offset can be caused by the dipole layer inside the dielectric film and is independent of the dipole position, the VFB shift almost remains constant as the CET varies (Figure 12a).

An interface dipole moment model has been proposed by P. D. Kirsch et al. through a study of Vth shift for nFETs with rare-earth element (La, Sc, Er, and Sc)-doped HfO2 [73]. Similarly, the dipole vector formed by incorporating rare-earth oxides could induce a shift in EWF, resulting in the Vth tuning of MOS devices. According to the experimental results, Vth approximately varied proportionally and inversely proportionally with the electronegativity and ionic radius of the dopant respectively. This is consistent with the conclusion drawn by L. Lin et al. that it is the dopant electronegativity that influenced the magnitude of the interfacial dipole moment and thus ΔVFB [74]. Moreover, the physical origin for the formation of the dipole layer has been ascribed to the difference in areal density of oxygen atoms (σ) between the oxides [75]. The formation process of the dipole layer is shown in Figure 12d, in which σHK and σSiO2 are the areal densities of oxygen atoms in high-k oxide and SiO2 respectively. For the case that σHK is smaller than σSiO2, in order to relax the structure, an oxygen atom tends to move towards the high-k side, thus resulting in the formation of a dipole consisting of a negatively-charged center in the high-k oxide and a positively-charged oxygen vacancy nearby.
3. Applications of La-based High-k Gate Dielectrics

3.1. Nonvolatile Memory

As the nonvolatile memory evolves from ROM (read-only memory) to flash memory, new materials and new structures and new operating principles have been continually explored in order to break the limitation that the electrons stored in the floating gate significantly decrease during the scaling down of floating-gate flash memory [76]. The new structures of flash memory include ferro-electric random-access memory (FeRAM), nano-electromechanical memory (NEMM), magneto-resistive random-access memory (MRAM), phase-change memory (PCM), and charge-trapping memory (CTM). Although CTM introduced in 1967 is the oldest, its high storage density, simple fabrication and compatibility with the CMOS technology make it a promising candidate for the next-generation flash memory technology [77]. Nowadays, the structure of CTM is based on a metal gate/oxide blocking layer (BL)/nitride charge trapping layer (CTL)/oxide tunneling layer (TL) gate stack on nm Si substrate as shown in Figure 13a. P-type Si is more often used than n-type Si because the electrons in the n-type channel formed at the surface of a p-type substrate have higher mobility than the holes in the p-type channel formed at the surface of an n-type substrate. Whether the CTL stores electrons or not is the way to define ‘1’ and ‘0’ respectively. The TL is formed by an insulating material, which allows electron tunneling from the substrate to the CTL under a positive gate bias and prevents electrons from escaping from the CTL to the substrate under no gate bias. The BL is also formed by an insulating material, which can prevent the electron transfer between the CTL and the gate electrode. Positive or negative voltage is applied to the gate electrode for programming or erasing operation, during which the electric field inside the gate stack enables electrons to flow into or out of the CTL via the TL. In order to further scale down the device, high-k materials such as the BL, CTL and TL have been widely studied, among which La-based high-k materials have been reported to achieve good results as discussed below.

**Figure 13.** (a) Cross-sectional schematic of a MONOS CTM transistor; (b) energy band diagrams of CTM in program, erase and retention states; and (c) energy band of CTM with SiO$_2$/LaAlO$_3$ double TL [78].

Firstly, when considering replacing SiO$_2$ by high-k material as the BL, apart from the k value, requirements including (i) large band gap and band offset with respect to the CTL, (ii) low density of traps at the interface or in the dielectric bulk, (iii) thermal and kinetic stability, and (iv) compatibility with the CMOS technology, should be fulfilled. According to Figure 13b, with an ideal high-k BL,
the electric field across the tunneling layer can be enhanced, thus improving the program/erase (P/E) speed [78]. Owing to a large band gap (8.8 eV) and good stability, Al₂O₃ has become the best choice for BL, but its low k value (~9) limits the device scaling. Therefore, La-doped Al₂O₃ (LaAlO₃) has been studied for higher k value, and results showed that not only the program speed and Vᵢₘ window increased, but the retention performance also improved [79]. The LaAlO₃ layer was deposited by ALD using La(ηPrCp)₃, Al(CH₃O)₃ and H₂O precursors and the atomic ratio of La/(La + Al) was 55%. Compared with Al₂O₃, LaAlO₃ as BL brought 40% and 32% improvements in program speed and Vᵢₘ saturation window, better robustness to voltage stress, and better retention performance below 120 °C. Besides, HfLaO has also been applied as BL and exhibited improvements in Vᵢₘ saturation window and robustness to voltage stress due to its higher k value (~22) compared to Al₂O₃. However, the retention performance degraded after La incorporation, probably due to decreased conduction-band offset [79,80].

Secondly, for the TL, a tradeoff exists between high P/E speed and good retention property, and so based on the investigation of the band-engineered barrier, the idea of multi-TL consisting of low-k and high-k dielectrics has been proposed. In Figure 13c, the LaAlO₃/SiO₂ double TL permits faster P/E because the AF and AE at the LaAlO₃/SiO₂ interface can give easier electron and hole tunnelings. Moreover, the added LaAlO₃ layer increases EOT, and so improves retention [81]. These were confirmed by experimental results: With the addition of the LaAlO₃ layer, the memory window measured at ±16 V for 100 µs increased from 3.3 to 5.6 V, and at 150 °C, an initial ∆Vᵢₘ of 5.6 V and a 10-year window of 3.8 V were achieved for the same P/E voltage and P/E time.

Moreover, La-based high-k materials have been widely investigated as the CTL due to the high k value and deep-level traps of La₂O₃ [53]. However, since the density of deep-level traps in La₂O₃ is not high enough, the memory window of the CTM with La₂O₃ as CTL was only 0.5 V at ±16 V for 1 s [82]. The main methods to solve this problem are: (i) nitrogen incorporation, which has been reported to induce traps in the bandgap and also remove shallow traps along the grain boundaries in CTLs [83]; (ii) doping other high-k material (e.g. Nb₂O₅, TiO₂), which is another way to increase the deep-level trap density in La₂O₃ and suppress its reaction with the SiO₂ TL as well [84]; (iii) multi-CTL for band engineering, which is capable of enhancing charge-trapping efficiency [85] and improving device reliability by suppressing the impact of TL degradation [86]. Experimentally, these methods have all been studied, and the results in Figure 14 [61,84,87–90] show obvious improvements in the performance of the memory device. HfLaO nanocrystal can provide the largest memory window, but the 50% degradation after 10 years in the retention property is not good for real applications. Comprehensively speaking, NbLaON is the most promising candidate so far due to its relatively large memory window, good P/E transient characteristics and negligible degradation after 10 years.

3.2. Metal-oxide-semiconductor Field-effect Transistors (MOSFETs)

Having been the basic device of ICs, MOSFET’s with high-k dielectrics have attracted a lot of efforts for more than 20 years. For the gate dielectric, the most important thing is to keep the carrier flow in the channel when biases are applied to the device. So, a sufficiently-large band gap and conduction-band (CB) offset with the channel material are necessary to prevent the current flow from the substrate to the gate. Moreover, the qualities of the dielectric film and the dielectric/substrate interface are also critical because as discussed in Section 2.2 (Figure 8), fixed charges, oxide traps, interface traps, interfacial dipoles, and surface roughness are the factors that lead to carrier scatterings and thus decreased carrier mobility. Therefore, it is important to explore different high-k materials and different post-deposition treatments in order to improve the device performance. Although HfO₂ has already been commercially dominant, La₂O₃ still holds its potential for future generations due to its larger CB offset with the Si substrate than its HfO₂ counterpart. As mentioned in Section 2.2, a La-silicate interfacial layer (IL) tends to be formed after high-temperature annealing, which is good for the interface quality but increases the EOT. K. Kakushima et al. have studied the properties of MOSFET with La₂O₃ as a gate dielectric, in which the La₂O₃ film was deposited by electron beam
Evaporation at 300 °C on a p-Si (100) wafer [91]. After a 500 °C rapid thermal annealing (RTA) in forming gas (N₂:H₂ = 97:3), a 1.57 nm silicate IL was formed in the 3-nm dielectric, leading to an EOT increase from 0.48 to 1.15 nm. However, the mobility peak increased from 60 to 300 cm²/Vs at room temperature and the subthreshold swing (SS) decreased from 120 to 66 mV/dec, which are impressive numbers for MOSFET.

Figure 13(c), the LaAlO₃/SiO₂ double TL permits faster P/E because the ΔEc and ΔEv at the LaAlO₃/SiO₂ interface can give easier electron and hole tunnelings. Moreover, La-based high-k materials have been widely investigated as the CTL due to the high mismatch to Si (1.3%), and small oxygen diffusion coefficient, which are all desirable for epitaxial gate dielectric on Si [93–95]. Si MOSFET with LaAlO₃ gate dielectric has been reported by I. Y. Chang, et al., where a 7.3-nm LaAlO₃ film was deposited on p-Si by RF sputtering and a post-deposition annealing was performed at 700 °C for 30 s in N₂ [96]. Results showed that the maximum effective mobility (μ_eff) at 300 K was 212.6 cm²/Vs; SS was 69.4 mV/dec; and hysteresis was 8.6 mV. According to the analysis on the mechanisms that caused mobility degradation, the Coulomb scattering was roughly the same for LaAlO₃ and SiO₂-gated MOSFETs, indicating that LaAlO₃ is indeed a promising candidate. N incorporation into LaAlO₃ has been proved to improve the device properties, including EOT, gate leakage, SS, and drive current [97]. Moreover, HfLaO, LaTiO, LaZrO, LaYO, etc. have all been tried as the gate dielectric for MOSFETs, and the device properties are listed in Table 2 [91,96,98–102]. The carrier mobility of the La₂O₃/LaSiO sample could reach 300 cm²/Vs, but its EOT was not small enough for further scaling down due to the low k value of SiO₂. The LaTiO sample was a good choice because of its high mobility (300 cm²/Vs), small EOT (0.63 nm) and low Vth (0.12 V). However, both the deposition method and post-deposition treatment are different for the dielectrics in Table 2, thus making a fair comparison among the samples difficult. However, all these results demonstrate the high potential of La-based high-k oxides as the gate dielectric of MOSFET.
LaLuO$_3$ with high k value (~30) and low leakage current has also attracted much attention and has been investigated in SOI-MOSFETs [103,104]. E. D. Ozhen, et al. first deposited it on an SOI (100) wafer by molecular beam deposition at 450 °C with a thickness of 6 nm, and a PDA was performed at 400 °C in oxygen and forming gas (H$_2$:N$_2$ = 1:9) sequentially for 10 min each [103]. According to the experimental results, the $V_{th}$ and SS of the SOI nFET and pFET were 0.22 V and −0.8 V, 72 mV/dec and 65 mV/dec, respectively. The LaLuO$_3$ film exhibited an EOT of 1.55 nm, low $D_{it}$ of 4.5 × 10$^{11}$ cm$^{-2}$·eV$^{-1}$, and the electron and hole mobilities on the SOI are similar to those of devices based on HfO$_2$ and HfSiON gate dielectrics with a similar EOT. However, the interface and bulk traps of the dielectric might cause a high level of 1/f noise, which could not meet the stricter requirements of the RF and analogue mixed-signal CMOS technologies. Therefore, M. Olyaei, et al. analyzed the low-frequency noise of the SOI-MOSFET with LaLuO$_3$ gate dielectric[98]. The normalized drain-current noise ($S_{ID}/I_D^2$) can be calculated by [105]:

$$\frac{S_{ID}}{I_D^2} = \frac{qkT N_i \gamma}{WLC_{ox}\mu_f C_{ox} I_D} \left(1 + \frac{\alpha \mu_{eff} C_{ox} I_D}{g_m} \right)^2,$$

where $W$ and $L$ are the width and length of the channel, $\lambda$ is the tunneling attenuation distance, $N_i$ is the volumetric oxide trap density, $C_{ox}$ is the gate-oxide capacitance, $\gamma$ is the transconductance, $\alpha$ is the scattering parameter, and $\gamma$ is the characteristic exponent. The calculation results showed that the LaLuO$_3$-gated device exhibited one to two orders of magnitude higher low-frequency noise than the standard MOSFETs, which is comparable to the devices with Hf-based dielectrics, implying that LaLuO$_3$ is a suitable candidate for balancing the tradeoff between device performance and device scaling.

### 3.3. Thin-film Transistors (TFTs)

TFT is a field-effect transistor operating as a voltage-controlled current source, and its conducting channel is formed in a thin film of semiconductor (<100 nm). When a bias is applied to the gate, carriers are accumulated at the interface between the gate dielectric and the thin-film semiconductor, thus forming a conducting layer as the channel. With an electric field along this channel generated by an applied drain-source bias, a drain current is created. Similar to the traditional MOSFET theory, the charges and traps in the gate dielectric and at the dielectric/semiconductor interface can influence the carrier mobility and threshold voltage, and so it is also important to improve the qualities of the high-k dielectric and the interface. For the development of TFT in a large-area flat-panel display with high resolution, the requirements cannot be satisfied by conventional Si as the channel material due to the low carrier mobility of amorphous Si and the non-uniform spatial distribution of grain structure in poly-Si. Oxide semiconductor as a channel material for TFT was proposed and studied at the beginning. ZnO TFTs were intensively studied from 2003 due to its high Hall mobility (~200 cm$^2$/Vs). Also, La-based high-k dielectrics were investigated, and especially a recent report proposed a solution-process method for LaAlO$_3$ deposition (spray pyrolysis) without the need for a vacuum environment to produce a TFT with $\mu_{eff}$ of 12 cm$^2$/Vs, $I_{on}/I_{off}$ ratio of 10$^6$ and SS of 650 mV/dec [106]. Unfortunately, the deposited ZnO film was polycrystalline and so suffered from grain-boundary
problems, leading to inadequate carrier mobility. After that, amorphous oxide semiconductor started to attract attention, and materials including ZnInSnO, ZnSnO, GaZnSnO, HfInZnO, and InZnO have all been investigated for TFT applications [107–111]. However, considering all the requirements of TFT (e.g. carrier mobility, thermal stability, controllability of carrier concentration, compatibility with current processing techniques), InGaZnO (IGZO) has become the most promising channel material.

First reported in late 2004 [112], IGZO TFT has been applied for mass production and sales since 2013, and adopted in high-end electronic products including iPad Pro and Surface Pro. Also, owing to the problems of scaling down, studies have been made on the use of high-k dielectric for IGZO TFT, especially focusing on La-based high-k materials in recent years. HfLaO was the first La-based high-k dielectric investigated for IGZO TFT in 2009 and achieved low V_{th} (0.22 V), small SS (76 mV/dec), high carrier mobility (25 cm²/Vs), and large I_{on}/I_{off} ratio (5 × 10⁷), which was the best performance among devices with other high-k gate dielectrics (e.g. Y₂O₃, Si₃N₄, AlTiO) [113]. However, there is still much room for improvement. Therefore, different annealing ambients for HfLaO film were then studied with results showing that N₂ was a better annealing ambient than O₂ and NH₃ and the carrier mobility could reach 35 cm²/Vs [114]. After that, more La-based ternary oxides have been studied with good results obtained. The characteristics of IGZO TFTs with promising La-based dielectrics are listed in Table 3 according to recent investigations [42,114–117], in which ZrLaO provided the highest carrier mobility (67.2 cm²/Vs) but lower high-field reliability, while LaAlO₃ was able to achieve low operating voltage (0.29 V) and small SS (98 mV/dec) but low mobility (5.4 cm²/Vs). Comprehensively speaking, NbLaO is the best candidate due to relatively high mobility (28.0 cm²/Vs), relatively low V_{th} (1.84 V), high on/off ratio (3.6 × 10⁷), and negligible hysteresis (0.07 V).

| Dielectrics | La₂O₃ [114] | HfLaO [114] | TaLaO [115] | NbLaO [42] | ZrLaO [116] | LaAlO₃ [117] |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| \(\mu_{ox}(\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1})\) | 16.6 | 35.1 | 23.4 | 28.0 | 67.2 | 5.4 |
| \(V_{th}(\text{V})\) | 2.14 | 3.3 | 2.4 | 1.84 | 2.59 | 0.29 |
| Hysteresis (V) | –0.61 | –0.03 | 0.1 | –0.07 | –0.56 | – |
| \(I_{on}/I_{off}(10^7)\) | 1.7 | 0.51 | 2.6 | 3.6 | 0.11 | 0.011 |
| SS (mV/dec) | 210 | 206 | 177 | 170 | 240 | 98 |
| \(C_m(\mu\text{F/cm}^2)\) | 0.21 | 0.24 | 0.262 | 0.26 | – | 0.23 |
| \(k\) | 8.5 | 10.9 | 11.8 | 10.1 | 8.9 | 10.4 |
| RMS (nm) | 0.96 | – | 0.51 | 0.24 | 0.82 | – |

As the large-area flat-panel display is developing for flexible applications nowadays, the idea of applying organic semiconductors as channel material has been proposed. Among the organic semiconductors, only a few have been reported to produce TFT’s with a carrier mobility higher than 1 cm²/Vs, namely 6T, dinaphtho [2, 3-b:29, 39-f] thieno [3, 2-b] thiophene (DNTT), and pentacene, with pentacene showing the greatest potential. Similarly, investigations of a pentacene-based organic thin-film transistor (OTFT) with La-based high-k dielectrics in recent years have achieved impressive device performances. C. Y. Han, et al. studied La incorporation into Y₂O₃, ZrO₂, and Nb₂O₅ for pentacene OTFT applications, and results showed that La incorporated in ZrO₂ and Nb₂O₅ significantly reduced their traps, thus increasing the carrier mobility [118]. The carrier mobilities of ZrLaO- and NbLaO-gated OTFTs were 70 times and 300 times those of their counterparts based on ZrO₂ and Nb₂O₅ respectively. However, the trap density in Y₂O₃ was increased by the La doping, leading to a degradation in carrier mobility. From another perspective, with Zr, Nb or Y added in La₂O₃, the moisture absorption of La₂O₃ could be suppressed, and so larger pentacene grains were grown on the smoother oxide surface (Figure 15a), thus resulting in higher carrier mobility. Table 4 lists the device properties of pentacene OTFT’s with La-based ternary oxides as gate dielectrics [41,118–122], with both NbLaO and TaLaO providing carrier mobility higher than 1 cm²/Vs. Similar to IGZO TFT, NbLaO can also achieve high performance for OTFT (high carrier mobility and high on/off ratio), which indicates its high potential in the applications of flexible electronics.
For flexible applications, pentacene OTFTs with La-based dielectrics have been tried on flexible substrates recently. M. F. Chang et al. reported pentacene OTFT on flexible polyimide (PI) (Kapton HPP-ST, Dupont) with HfLaO as a gate dielectric (Figure 15(b)) [123]. The device structure is depicted in the inset of Figure 15c: a 30 nm HfLaO dielectric was deposited on a TaN gate, followed by an O₂ treatment for 30 min at 200 °C, and Au was used as the source/drain electrodes. According to the transfer characteristics in Figure 15c, the carrier mobility, SS, V<sub>th</sub>, and I<sub>on</sub>/I<sub>off</sub> ratio were extracted to be 0.13 cm<sup>2</sup>/Vs, 130 mV/dec, −1.25 V, and 1.2 × 10<sup>4</sup> respectively, which can be useful for flexible electronics. Recently, vacuum tape has been reported to be the substrate of pentacene OTFT with NbLaO as a gate dielectric (Figure 15d) [124]. With the device structure shown in the inset of Figure 15e, Al electrode was first evaporated on vacuum tape as a gate electrode; then an 80 nm NbLaO film was deposited by RF sputtering; a PDA was performed in N₂ for 20 min at 200 °C; and Au was thermally evaporated as the source/drain electrodes. Similarly, the transfer characteristics in Figure 15e are used for parameter extraction, and the carrier mobility, SS, V<sub>th</sub>, and I<sub>on</sub>/I<sub>off</sub> ratio are 4.8 cm<sup>2</sup>/Vs, 174 mV/dec, −1.90 V, and 4.52 × 10<sup>4</sup> respectively, which are impressive. Especially, the carrier mobility in this work is higher than most previously reported on OTFT’s with flexible substrates, and is comparable to the highest (9.5 cm<sup>2</sup>/Vs) up till now [125].
3.4. Ge and III-V Metal-oxide-semiconductor (MOS) Devices

In order to further increase the drive current of transistors to meet the requirements in the future, semiconductors with higher carrier mobility have been investigated to replace Si for a few decades. The replacement began with strained Si and SiGe, but limitations were found in mobility degradation and $V_{th}$ shift. The next step was using Ge due to its superior intrinsic electron mobility (3900 cm$^2$/Vs) and hole mobility (1900 cm$^2$/Vs). Unfortunately, the insufficiently oxidized interfacial layer (GeO$_x$) with high $D_{it}$ could significantly deteriorate the performance of Ge MOS devices, and so the studies in recent years mainly focused on the passivation of the Ge surface for lower $D_{it}$.

Rare-earth oxides (e.g. CeO$_2$, Dy$_2$O$_3$, Gd$_2$O$_3$ and La$_2$O$_3$) have been suggested for passivating the oxide/Ge interface. Especially for La$_2$O$_3$, a stable La-germanate interlayer can be formed as mentioned in Section 2.2 (Figure 10a), and is capable of inhibiting the volatilization of the GeO sub-oxides at the Ge surface, thus suppressing the formation of interfacial defects [126]. O. Bethge et al. reported the characteristics of an Au-Ti alloy/ZrO$_2$/La$_2$O$_3$/Ge gate stack, in which La$_2$O$_3$ was the interfacial passivation layer (IPL) (1 nm) and ZrO$_2$ was the gate dielectric (6.5 nm), both deposited by ALD [127]. The PDA was in Ar for 5 min at 350 °C for covering purposes. Conditions for the PDA and PMA were 500 °C for 5 min and 300 °C in forming gas (H$_2$:N$_2$ = 1:9) for 30 min also at 350 °C. The extracted $k$ value of the dielectric stack was promising (14.7), but the $D_{it}$ at midgap of $1.2 \times 10^{12}$ cm$^{-2}$·ev$^{-1}$ was still not low enough. After that, nitrogen incorporation during the deposition of La$_2$O$_3$ by RF sputtering has been studied [128]. In order to suppress the moisture absorption of LaON, a 1-nm Al$_2$O$_3$ was deposited also by sputtering for covering purposes. Conditions for the PDA and PMA were 500 °C in N$_2$ for 5 min and 300 °C in forming gas (H$_2$:N$_2$ = 5:95) for 20 min respectively. Obvious improvements after nitrogen incorporation were obtained and LaON achieved a low $D_{it}$ with the Ge substrate ($4.96 \times 10^{11}$ cm$^{-2}$·ev$^{-1}$). Moreover, La-based ternary oxides and dual passivation layers have been investigated with good results available, and the characteristics of Ge MOS devices with La-based dielectrics and/or passivation layers reported recently are summarized in Table 5 [56,127–132].

| Dielectric | La$_2$O$_3$ [126] | ZrO$_2$ [127] | LaON [128] | HfO$_2$ [129] | LaTiON [130] | HfTiON [131] | HfO$_2$ [132] |
|------------|-----------------|---------------|-------------|----------------|----------------|----------------|----------------|
| Deposition | E-beam | ALD | Sputtering | LaON Sputtering | LaTiON Sputtering | LaTiON Sputtering | TaON/LaON Sputtering |
| $T_m$ (nm) | 5.5 | 7.5 | 8 | 10 | 8 | 7 | 8 |
| $k$ | 14.7 | 18.8 | 19.2 | 24.6 | 27.7 | 20.9 |
| $I_D$ (A/cm$^2$) at $V_{dd}$ = –1 V | $1 \times 10^{-4}$ | $2.89 \times 10^{-4}$ | $5.53 \times 10^{-4}$ | $2.2 \times 10^{-3}$ | $7.8 \times 10^{-4}$ | $1.77 \times 10^{-4}$ |
| CET (nm) | – | 1.92 | 2.0 | 1.2 | 1.1 | 1.49 |
| $D_h$ (cm$^2$·V$^{-1}$) | $8 \times 10^{11}$ | $1.2 \times 10^{12}$ | $4.96 \times 10^{11}$ | $4.2 \times 10^{11}$ | $3.1 \times 10^{11}$ | $7.8 \times 10^{11}$ | $5.32 \times 10^{11}$ |

The ZrO$_2$/La$_2$O$_3$ dielectric stack has been applied by W. B. Chen et al. in Ge n-MOSFET with a laser annealing (LA) treatment to increase its gate capacitance density [133]. The 5-nm high-$k$ IPL and dielectric stack were deposited by PVD, followed by a PDA in O$_2$. Then, the LA was performed in the air with laser spot sizes of 0.3 cm$^2$ (after focus) and 0.9 cm$^2$ (without focus) for $n^+$/p junction and high-$k$ dielectric respectively and was stepped continuously in the x and y directions until the whole sample was covered. Results showed that with the LA treatment, $C_{ox}$ rose from 1.8 $\mu$F/cm$^2$ to 2.7 $\mu$F/cm$^2$, thus decreasing the EOT from 1.6 to 0.95 nm. Besides, good transistor characteristics including high carrier mobility ($\mu_{eff, peak} \sim 600$ cm$^2$/Vs), small SS (106 mV/dec) and low $V_{th}$ (0.18 V) were obtained.

Compared with Ge, III–V compound semiconductors own even higher electron mobility and so have become promising candidates for Si replacement. Among all the III–V compounds, GaAs with five times higher electron mobility and larger band gap (1.42 eV) than Si has attracted the most attention in recent years, especially in MOS devices with high-$k$ gate dielectrics. However, like Ge, GaAs also suffers from high $D_{it}$ caused by its unstable and easily-formed native oxides [127], which lead to severe Fermi-level pinning. Therefore, similarly, the biggest challenge for GaAs-based MOS devices with high-$k$ dielectrics is the surface passivation of GaAs to improve the interface quality. Si and Ge were
first studied as IPL with $D_{th}$ reduction obtained [134,135]. However, since Si and Ge are amphoteric dopants for GaAs, the doping concentration in the channel might be influenced and so oxide IPLs are preferred. As mentioned in Section 2.2, the La-silicate interfacial layer is capable of improving the interface quality between Si and La₂O₃, and so the idea of applying an La₂O₃/Si stack has been proposed by T. Das et al. [136]. The Si and La₂O₃ layers were deposited on Zn-doped p-GaAs by RF sputtering, and a PDA at 500 °C in N₂ for 1 min was implemented. According to XPS analysis, La-O-Si bond was obviously detected, implying the formation of an LaSiO passivation layer. Like Ge, La-based complex oxides and dual IPL have been tried on GaAs recently with improvements achieved, and the characteristics are listed in Table 6 [136–142]. Compared with Ref. 129, improvements can be found in Refs. [137–142], indicating that as IPL, La-based oxides with nitrogen incorporation can provide higher interface quality with GaAs than with Si. In particular, for the case of LaAlO₃ deposited by molecular-beam deposition, $D_{th}$ reached the order of $10^{10} \text{ cm}^{-2} \cdot \text{ev}^{-1}$, which is comparable to those of Si-based MOS devices.

Another III–V compound, GaN, has recently drawn considerable attention in high-speed, high-temperature and high-power applications due to its wide bandgap (3.3 eV), high breakdown field ($\sim 5 \times 10^6 \text{ V/cm}$) and high electron saturation velocity. Much efforts have been made on GaN-based high-electron-mobility transistor (HEMT), especially with AlGaN/GaN substrate. Unfortunately, the trapping/detrapping of surface states and the high channel temperature under high drain voltage ($V_D$) are the main concerns that lead to output-power degradation and generation of undesirable harmonic signals at high input swing. Therefore, a high-k insulator is needed between the gate electrode and the AlGaN Schottky layer in order to solve these problems without sacrificing the gate-to-channel modulation ability [144]. H.C. Chiu et al. reported an AlGaN/GaN MOS HEMT with La₂O₃ as a gate dielectric, and the device structure and TEM image of the gate stack are illustrated in Figure 16a [145]. According to the comparison of transfer characteristics between the La₂O₃ MOS HEMT and conventional GaN HEMT, the gate-to-channel modulation ability was slightly suppressed by the existence of the dielectric, leading to a slight decrease of drain current. However, the La₂O₃ MOS HEMT exhibited a flatter transconductance ($g_{ms}$) vs. $V_{gs}$ curve than the standard HEMT (Figure 16b), indicating that the intermodulation of a high-frequency signal could be reduced by the La₂O₃ layer and the distortion problem under high-power operation could be suppressed. The lower 1/f noise of the La₂O₃ MOS HEMT than that of the conventional HEMT (Figure 16c) implies that plasma-induced surface states could be avoided by the La₂O₃ dielectric. Besides, the C-V curve of the MOS-ring capacitor (Figure 16d) shows a sharp transition from depletion to two-dimensional electron gas (2DEG) accumulation, demonstrating a high-quality interface. Later, LaAlO₃ has been applied as the dielectric layer in MOS HEMT by C.Y. Tsai, et al., and was deposited by e-beam evaporation with a 400 °C PDA in O₂ for 5 min [146]. The transfer and mobility characteristics are shown in Figure 16e, from which low $V_{th}$ (0.1 V), small on-resistance ($R_{on}$) (13.5 Ω-mm), high breakdown voltage (385 V), and relatively high peak mobility (201 cm²/Vs) are obtained. Therefore, the insertion of the La₂O₃ dielectric in GaN-based HEMT has high potential to improve the device performance for high-power and high-linearity amplifier applications.

| Table 6. Characteristics of GaAs MOS devices with La-based high-k oxides as IPL or gate dielectric. |
|----------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| Dielectric    | La₂O₃ [136]      | LaYO [137]       | LaAlO₃ [138]     | LaLuO₃ [139]     | TaYON [140]      | ZrON [141]       | LuTlON [142]     |
| Deposition    | Spattering       | Spattering       | ALD              | MBD              | ALD              | Spattering       | Spattering       |
| $T_{as}$ (nm) | k                |                   |                   |                   | k                |                   |                   |
| k             | 15               | 14               | 10               | 12               | 10               | 10               | 10               |
| $J_E$ (A/cm²) | $I_{V_{th}/-1V}$ |                   |                   |                   | $I_{V_{th}/-1V}$ |                   |                   |
| $I_{V_{th}/-1V}$ | 1.2 × 10⁻⁵       | 8 × 10⁻⁸         | 1.3 × 10⁻⁵       | 3.8 × 10⁻⁵       | 6.2 × 10⁻⁶       | 2.3 × 10⁻⁵       |
| CET (nm)      | 7.8              | 2.48             | 5.73             | 1.87             | 1.71             | 3.07             | 1.48             |
| Hysteresis (mV)| 260              | 30               | 35               | 30               | 45               |                   |                   |
| $D_{th}$ (cm²·ev⁻¹) | 1.2 × 10¹² | 5 × 10¹⁰ | 5 × 10¹⁰ | 7 × 10¹⁰ | 9 × 10¹¹ | 1.2 × 10¹¹ | 7 × 10¹¹ |

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Witters, et al. tried La$_2$O$_3$ as a thin capping layer for HfSiO gate dielectric in FinFET [147]. Results showed that the La$_2$O$_3$ capping layer was effective in fabricating nFinFETs with low V$_{th}$, which is consistent with the discussion in Section 2.3 that the V$_{th}$ of nFETs can be shifted in the negative direction by the insertion of La$_2$O$_3$. Recently, double-gate (DG) and tri-gate (TG) FinFETs with La$_2$O$_3$ as gate dielectric have been studied through device simulation. In Ref. [148], DG FinFETs with different gate dielectrics were simulated by the PADRE simulator from MuGFET. The device structure is shown in Figure 17a, where the gate length (L$_g$), EOT, fin width (W$_{ch}$), extension length to source/drain (L$_e$/L$_d$), channel and drain/source doping concentrations are set to be 12, 2, 10, 20 nm, 1 × 10$^{16}$ cm$^{-3}$ and 1 × 10$^{19}$ cm$^{-3}$, respectively. According to the simulation results in Figure 17b, La$_2$O$_3$ gate dielectric provided the smallest drain-induced barrier lowering (DIBL) (53 mV/V) and SS (85 mV/dec). Besides, when compared to SiO$_2$, La$_2$O$_3$ exhibited a 132% increase in g$_m$, indicating its better gate control on the drain current. The same simulation was also performed on GaAs FinFET, and similarly, La$_2$O$_3$ was capable of achieving the smallest DIBL (47 mV/V), lowest SS (76 mV/dec), and highest g$_m$ among all the gate dielectrics [149]. As for TG FinFET, simulation was carried out on SOI substrate by the SILVACO TCAD simulator with the device structure depicted in Figure 17d [150]. The L$_g$, EOT, fin width and height, buried-oxide thickness, body, and source/drain doping concentrations are set as 30, 1.2, 10, 20 nm, 5 × 10$^{17}$ cm$^{-3}$, and 5 × 10$^{20}$ cm$^{-3}$, respectively. Results showed that the V$_{th}$, SS and I$_{on}/I_{off}$ of La$_2$O$_3$-gated FinFET are 0.312 V, 63.7 mV/dec and 6.2 × 10$^6$ respectively, which are comparable to those of a device with an HfO$_2$ gate dielectric.

### 3.5. Other Novel Metal-oxide-semiconductor (MOS) Devices

For better supporting the roadmap of the semiconductor industry beyond the 14-nm technology node, fin field-effect transistor (FinFET) with multi-gate is considered to be the best candidate in order to avoid the adverse impact from the short-channel effects. Unlike MOSFET with one channel at the surface of the semiconductor substrate, FinFET has multiple channels which increase the equivalent channel width, but its working principle is same as that of the traditional MOSFET. Therefore, La-based high-k dielectrics are also promising in FinFET for the purpose of its down-scaling. Early in 2008, L. Witters, et al. tried La$_2$O$_3$ as a thin capping layer for HfSiO gate dielectric in FinFET [147]. Results showed that the La$_2$O$_3$ capping layer was effective in fabricating nFinFETs with low V$_{th}$, which is consistent with the discussion in Section 2.3 that the V$_{th}$ of nFETs can be shifted in the negative direction by the insertion of La$_2$O$_3$. Recently, double-gate (DG) and tri-gate (TG) FinFETs with La$_2$O$_3$ as gate dielectric have been studied through device simulation. In Ref. [148], DG FinFETs with different gate dielectrics were simulated by the PADRE simulator from MuGFET. The device structure is shown in Figure 17a, where the gate length (L$_g$), EOT, fin width (W$_{ch}$), extension length to source/drain (L$_e$/L$_d$), channel and drain/source doping concentrations are set to be 12, 2, 10, 20 nm, 1 × 10$^{16}$ cm$^{-3}$ and 1 × 10$^{19}$ cm$^{-3}$, respectively. According to the simulation results in Figure 17b, La$_2$O$_3$ gate dielectric provided the smallest drain-induced barrier lowering (DIBL) (53 mV/V) and SS (85 mV/dec). Besides, when compared to SiO$_2$, La$_2$O$_3$ exhibited a 132% increase in g$_m$, indicating its better gate control on the drain current. The same simulation was also performed on GaAs FinFET, and similarly, La$_2$O$_3$ was capable of achieving the smallest DIBL (47 mV/V), lowest SS (76 mV/dec), and highest g$_m$ among all the gate dielectrics [149]. As for TG FinFET, simulation was carried out on SOI substrate by the SILVACO TCAD simulator with the device structure depicted in Figure 17d [150]. The L$_g$, EOT, fin width and height, buried-oxide thickness, body, and source/drain doping concentrations are set as 30, 1.2, 10, 20 nm, 5 × 10$^{17}$ cm$^{-3}$, and 5 × 10$^{20}$ cm$^{-3}$, respectively. Results showed that the V$_{th}$, SS and I$_{on}/I_{off}$ of La$_2$O$_3$-gated FinFET are 0.312 V, 63.7 mV/dec and 6.2 × 10$^6$ respectively, which are comparable to those of a device with an HfO$_2$ gate dielectric.
without interface traps. Therefore, SL-FET with an La-based high-k dielectric should be a promising candidate for the future semiconductor industry.

Particularly, when comparing the HfO$_2$/La$_2$O$_3$ superlattice FET (SL-FET) with HfO$_2$/La$_2$O$_3$ could provide almost the same transfer behavior as Al$_2$O$_3$ without interface traps. Therefore, SL-FET with an La-based high-k dielectric should be a promising candidate for the future semiconductor industry.

Moreover, to achieve even higher drive current by devices with even smaller dimensions, the idea of nanowire-based transistors has been proposed and proved to be promising for future generations. However, the application of La-based high-k gate dielectric for nanowire transistors is still in the stage of simulation. Gate-all-around InAs transistors with different high-k gate dielectrics have been simulated based on the effective-mass theory using the Multigate Nanowire FET TCAD simulator by R. Gupta, et al [151]. The device structure is shown in the inset of Figure 18a, with a source/drain and gate length of 10 nm, oxide width (W$_{ox}$) of 1 nm, buried-oxide thickness (T$_{box}$) of 5 nm, substrate body width (W$_{InAs}$) of 5 nm, and substrate thickness of 25 nm. Similar to the results of FinFET with different high-k dielectrics, La$_2$O$_3$ outstood among the high-k materials, especially in transfer behavior and SS, as demonstrated in Figure 18a.b. Besides, an InGaAs/InAlAs nanowire superlattice FET (SL-FET) with HfO$_2$/La$_2$O$_3$ gate dielectric has been simulated by a full-band quantum simulator and its structure is shown in Figure 18c [152]. An optimal on-state current $I_{on}$ of 1 mA/μm has been achieved at a gate voltage of 0.4 V, and a small SS (27 mV/dec) could sustain for six decades of drain current. Particularly, when comparing the HfO$_2$/La$_2$O$_3$ and Al$_2$O$_3$ gate dielectrics, with an interface-trap density of $1.6 \times 10^{11}$ cm$^{-2}$, HfO$_2$/La$_2$O$_3$ could provide almost the same transfer behavior as Al$_2$O$_3$ without interface traps. Therefore, SL-FET with an La-based high-k dielectric should be a promising candidate for the future semiconductor industry.
Figure 18. (a) Transfer characteristics and (b) Ion, Ioff, gm and Ion/Ioff ratio of InAs nanowire gate-all-around transistors with different gate dielectrics [151]. (c) Device structure and (d) transfer characteristics of InGaAs/InAlAs nanowire superlattice-FET’s with Al2O3 and HfO2/La2O3 gate dielectrics [152].

4. Conclusions and Future Prospects

The progress of La-based high-k dielectrics in recent years has been reviewed, with an emphasis on MOS applications. Owing to its large band gap and high k value, La2O3 is considered as a promising gate dielectric for MOS devices. However, through the analyses on the physical and chemical characteristics of La2O3, its hygroscopicity and defects (including oxide traps, interface states and grain-boundary states) are the major concerns that lead to a degradation in device performance. The solutions to these problems can be summarized as: (i) high-temperature annealing in N2 or inert gas, (ii) nitrogen incorporation, (iii) laser treatment, and (iv) doping of other high-k metal element (M) to form complex high-k ternary oxide. From another perspective, incorporating La into other high-k binary oxides is capable of passivating oxygen vacancies and modifying the flatband voltage of the MOS system and so improves the qualities of the dielectric film and high-k/semiconductor interface and reduces the Vth of the nFETs respectively, thus contributing to higher drive current and lower power consumption for meeting the future requirements of the semiconductor industry. According to the review of La-based dielectrics in different MOS devices, including non-volatile memory, MOSFET, TFT, Ge device, III-V device, FinFET and nanowire-based transistor, LaMO (M = Al, Hf, Nb, Ti, Ta, Zr, Y, and Lu) with or without nitrogen incorporation as a gate dielectric or passivation layer could provide impressive performance for Ge and III-V devices, especially with the MBD-deposited LaAlO3 achieving a very low Dq in the order of 1010 cm−2·eV−1. Besides, based on simulation results, La2O3 showed high potential as the gate dielectric of FinFET and nanowire transistors. All these advantages of La-based high-k dielectrics can pave the way for the MOS research in the directions of higher speed, lower power consumption and smaller dimensions, based on transistors with novel structures (e.g., tunnel FET), 2D material (MoS2, graphene, etc.)-based transistors, and nanowire transistors with metal nano-structural plasmonics in MOS mode.

Author Contributions: Writing—original draft preparation, L.N.L.; revision, P.T.L. and W.M.T.; supervision, P.T.L.; project administration, P.T.L. and W.M.T.; funding acquisition, W.M.T.

Funding: This research was funded by University Development Fund (Nanotechnology Research Institute) grant number 00600009.

Conflicts of Interest: The authors declare no conflict of interest.

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