A multi-functional intelligent metasurface: Electromagnetic design accounting for fabrication aspects

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Abstract—In this paper we present the theoretical considerations and the design evolution of a proof-of-concept intelligent metasurface, which can be used as a tunable microwave absorber, as well as a wavefront manipulation and polarization conversion device in reflection. We outline the design evolution and all considerations taken into account, from the selection of patch shape, unit cell size, and substrate, to the topology of the structure that realizes the desired tunability. The presented design conforms to fabrication restrictions and is co-designed to work with an integrated circuit chip for providing tunable complex loads to the metasurface, using a commercially available semiconductor process. The proposed structure can perform multiple tunable functionalities by appropriately biasing the integrated circuit chip: Perfect absorption for a wide range of incidence angles of both linear polarization states, accommodating a spectral range in the vicinity of 5 GHz, as well as wavefront control demonstrated exemplified via anomalous reflection and polarization conversion. The end vision is for this unit-cell design to be scalable and deployable as a practical HyperSurface, i.e., an intelligent multi-functional metasurface capable of concurrent reconfigurable functionalities, such as absorption, beam steering, polarization conversion, wavefront shaping, holography, sensing etc.

Index Terms—Intelligent metasurface, microwaves, tunable absorption, wavefront manipulation.

I. INTRODUCTION

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Intelligent metasurfaces are electromagnetically ultra-thin sheets which are able to provide us with tunable electromagnetic functions on demand. They consist of sub-wavelength elementary units, the meta-atoms, which with proper engineering can enable particular interactions of the metasurface and the incoming wave [1]–[3]. This meta-atomic level manipulation has opened the path to the realization of a plethora of electromagnetic functions and applications involving wavefront shaping [4]–[9], polarization control [10]–[12], dispersion engineering [13], [14], perfect, broadband and asymmetric absorption [15]–[19], holography [20], non-reciprocity [21], extreme energy accumulation [22], wireless power transfer [23], harmonic generation [24] and many more. The key element in a tunable metasurface is to have an inclusion (material or component) whose electromagnetic properties can be modified by an external stimulus. Following this rationale, various tunable electromagnetic functions have been demonstrated in metasurfaces that comprise stimulus-sensitive materials such as graphene [25], [26] liquid crystals [27], photoconductive semiconductors [28] and so forth.

Most of the initial implementations referred to globally tunable metasurfaces, imposing limitations related to the lack of local control over the metasurface impedance. Clearly, for a multi-functional intelligent metasurface, an independently varying element is required in each unit cell to enable local control and reconfigurability. A practical solution to this problem, highly suited to microwave realizations, is given by incorporating lumped electronic elements in the meta-atoms. In this way, the local impedance of the metasurface can be modified by means of applying DC voltage signals (biasing) at the elements, commonly PIN switch diodes and P-N varactor diodes. Switch diodes have been widely used in global or local binary-state scenarios for functional metasurfaces [20], [29]–[35]. Binary-state control still restricts the realizable functions as the impedance configurations along the metasurface are limited. Varactor diodes, on the other hand, provide continuous but mainly reactive control and, thus, the ability to tune only the imaginary part of the surface impedance.

In Ref. [36], we presented a model metasurface with conceptual tunable integrated circuits (IC) incorporated in each unit cell to allow for full control over the complex surface impedance, i.e., independently and continuously variable re-
sistance and capacitance. This full impedance control enables to spatially shape both the phase and amplitude of the local reflection (or transmission) coefficient and allows maximum versatility in the realizable functionalities. More importantly, this concept infuses intelligence in the metasurface which can be programmatically controlled with a computer. In addition, by interconnecting the ICs with each other into forming a network, the vision of an intelligent metasurface fabric can be realized, where each unit can sense the ambient conditions, communicate information within the metasurface and with the main controller (computer), and perform its own programmable computing and actuation, with vast application within the emerging “Internet of Things” paradigm [37]–[43].

In this paper, we present the practical considerations and the design of a realistic multifunctional metasurface designed for operation at microwave frequencies (5 GHz). The metasurface consists of square patches placed on a metal-backed dielectric layer. It includes an envisaged custom IC (or “chip”), strategically placed behind the metal back plane. We thoroughly present the design process of the intelligent metasurface, from the perspective of the electromagnetic considerations and the implementation restrictions of the envisaged IC. We then evaluate the performance of the metasurface as a tunable perfect absorber, which is the primarily targeted functionality, and show successful operation at the design frequency for a range of incidence angles of both TE and TM polarization. In addition, we demonstrate wavefront manipulation functionality, exemplified through anomalous reflection, and polarization control capabilities, showcasing the multi-functional nature of the proposed system and its control over the amplitude, wavefront, and polarization properties of the output electromagnetic wave. Control over the frequency content of the impinging radiation could also be possible with the proposed linear metasurface, by using fast time modulations of the loads provided by the ICs. Additional steps towards the realization of this metasurface with a prime focus on the custom ICs (chips) implementation and practical aspects of the PCB design can be found in [44].

The paper is organized as follows: in Section II we present the evolution of the metasurface unit-cell design from the simple proof-of-concept version to a practically feasible prototype; dedicated subsections address different design aspects pertaining to metasurface topology and operation, basic structural decisions, available range from the IC chip, fabrication and practical restrictions, and, finally, the simulation design strategy we have followed, relying on S-parameters of both lumped and Floquet ports. In Section III we present the final design of the unit-cell of the tunable absorber metasurface, backed by full-wave simulation results for performance evaluation and parameter sensitivity. In addition, we assess the performance of indicative beam steering and polarization conversion functionalities. Finally, Section IV provides a summary and discusses future prospects and open challenges of such intelligent metasurface applications.

II. CONCEPTUAL DESIGN AND PRACTICAL CONSIDERATIONS

Electromagnetic design of a locally tunable multi-functional metasurface, that can be readily manufactured with existing fabrication processes and at a reasonable cost, poses practical challenges that can only be met with multi-facet considerations and performance compromises. This section addresses the design considerations needed to select and develop the most appropriate topology, allowing as general reconfigurability as possible and leading to a realistic metasurface design. We take into account both electromagnetic response and practical considerations, as well as simulated dynamic load tunability of the IC, while accommodating for the broadest possible functionality, quantified in terms of realizing the desired response for excitation by obliquely incident waves of different frequencies and polarizations.

A. Electromagnetic considerations for the design of versatile and fully reconfigurable metasurfaces

Probably the most natural choice for a topology of a tunable metasurface for applications in the microwave frequency range is the classical high-impedance surface formed by a sub-wavelength array of metal patches over a grounded dielectric layer, see pioneering papers [45], [46] and recent reviews [3], [47]. The patches can be either connected to the ground by metal vias (the so-called “mushroom” structure [48]) or left floating (e.g. [49], [50]). The presence of the vias pins affects the oblique-incidence performance for TM-polarized excitation (e.g. [51], [52]). This structure allows control over both amplitude and phase of the reflection coefficient by controlling the properties of the patch array only, it is very simple, compact, and can be manufactured using conventional printed circuit board (PCB) technology.

1) Uniform distribution of control elements versus clustering: The simplest way to tune the metasurface response is to modify the gap capacitance between the patches, this way tuning the effective sheet capacitance and resistance of the patch array. This approach has been used in earlier works, using both varactors (e.g. [45], [46], [29], [53], [31], [54] and MEMS capacitors (e.g. [55]). For plane-wave illumination, the response of the metasurface is determined by the parallel-type resonance of the distributed capacitance of the patch array and the inductance due to the magnetic flux between the ground plane and the patch array [49]. Thus, it appears reasonable to connect tuning elements (most commonly, varactors) into every gap between metal patches, and this topology was indeed used in [45], [46], [55], [29], [53], [31], and other works.

This approach works well for surface-uniform biasing (tuning the reflection coefficient for plane-wave illumination) or for slowly-varying biasing (realizing tunable phase-gradient metasurfaces). However, there are applications where fast (on the wavelength scale) tunable variations of the surface properties are needed. For example, to realize anomalous reflection from normal incidence to near-grazing direction, so called metagratings [56] offer arguably the most reasonable solution. To realize this regime, we need to configure the metasurface as a periodical array of electrically small elements.
with the period of the order of the wavelength. Moreover, to enable anomalous reflection into arbitrary directions, we need to have a possibility to configure the metasurface as a nonlocal, inhomogenizable periodical array (with the period from 1.5\(\lambda\) to 3\(\lambda\) where each super-cell contains several small elements, all of them being different [57]. The conventional topologies of tuning the surface-averaged sheet reactance of the patch array are not optimal for realization of these more demanding functionalities, because the change of each control element strongly affects the collective response of the whole array of patches [57].

For this reason, it appears preferable to form the metasurface as an array of patch clusters, each of which is separately controlled. The simplest topology is a cluster of four patches with control units between them, as illustrated in Fig. 1(a). In this topology, the patches of the two neighboring clusters are coupled only through the gap capacitance, while in the usual, uniform layout, there is also the admittance of the control unit, which in practice cannot be made negligibly small. A cluster of four patches with controllable loads between them can be viewed as one patch with tunable anisotropic sheet impedance. Thus, in contrast to the conventional approach of tuning capacitance of the array of slots, we tune each array element. Setting several clusters in the same or similar states, it is possible to tune the surface-averaged sheet impedance and realize phase-gradient metasurfaces or tunable absorbers. In the other extreme scenario, it is possible to connect four patches of one unit cell to the ground by different impedances, realizing one electrically small unit cell behaving as a tunable bianisotropic scatterer, while other clusters are tuned away from the resonance. This way it is possible to realize tunable diffraction gratings (metragratings [56]). Finally, we note that the control elements can be active or time-varying, opening possibilities to create amplifying, non-Foster, and nonreciprocal reconfigurable metasurfaces. In view of our goal to allow as general reconfigurability as possible, we prefer the clustering layout. Note that this patch layout is similar to that used in [54], although in that paper only uniform bias has been considered.

2) Optimal patch shape: Although the choice of the square shape of metal patches for realization of varactor-tunable metasurfaces appears to be well understood and well established, for completeness, we explain the reasons for this shape selection. In the literature on high-impedance surfaces and artificial magnetic conductors one can find suggestions of using patches of many different shapes, from simple Jerusalem crosses and various spiral shapes to space-filling curves, e.g. [58], [59], [60]. Shapes other than simple squares are used when there is a need to reduce the thickness of the structure and/or the size of the unit cell. In all these solutions, the equivalent circuit of the patch array contains an additional inductance in series with the effective capacitance of the patch array. This inductance increases the total inductance of the parallel resonant circuit (the main inductance is due to the magnetic flux between patch array and the ground plane), bringing the resonant frequency down and allowing reduction of the substrate thickness. However, this additional inductance reduces the bandwidth of the resonator, because it is in series with the capacitive branch, see detailed explanations and numerical examples in [46], [61]. Thus, if there is no need for reduction of the substrate thickness, the choice of square patches with small gaps between them is clearly preferable. If there is a need of miniaturization, it is preferable to increase the effective capacitance of the patch array by using double layers of patches instead of replacing wide patches by thinner strips of any shape.

Another issue related to the choice of the patch shape is the isotropy of the surface. For most applications, it is desirable that the properties of the metasurface are isotropic in the metasurface plane. Arrays of electrically small square patches are slightly anisotropic because waves propagating along the diagonal and along the patch edges see a different period of the array. In this respect, the use of hexagonal patches is preferable, since the anisotropy of such arrays (assuming the same patch area) is considerably weaker. However, this difference can be usually neglected for small arrays periods, and the square shape is still preferable due to a reduced number of control elements; in this work we adopt the square topology for the structure.

3) Optimal unit-cell size: From the practical point of view, it is desirable to use the smallest possible number of tunable unit cells, to minimize complexity and costs. This means that we should select the largest size of the unit cell, still allowing realizing full control of reflection. If the target functionality is to control the reflection coefficient for plane-wave illuminations (for example, realizing tunable absorbers for varying frequency, incidence angle, and polarization), there is no need for control of the surface properties at the subwavelength scale. A periodical array whose period is smaller or equal to \(\lambda/2\) will not create grating lobes, and for the plane-wave illumination we can configure all the unit cells identically, realizing an effectively uniform lossy boundary, matched to free space for the desired frequency, incidence angle, and polarization. Thus, for this application the optimal unit cell size equals \(\lambda/2\) at the highest operational frequency.

Another important functionality is anomalous reflection with moderate deflection angles. For instance, for realizing planar or conformal focusing mirror with the focal distance which is large compared with the array size. In this case, the array should be configured as a phase-gradient metasurface: the parameters of the unit cells slowly vary along the surface. This is actually the case of a conventional phased-array antenna (a reflectarray in this case) [62]. As is well-known, also in this case the use of \(\lambda/2\)-size array elements is appropriate. However, in this case the array is not uniform, and there is some scattering into parasitic propagating Floquet modes. Reducing the unit-cell size makes the effective (surface-averaged) response more uniform and reduces scattering and improves the bandwidth [63], [62]. However, improvements are not very dramatic, because for moderate deflection angles (for normal illumination, up to about 30° to 40°) the parasitic scattering is small [57], with only a few percent loss in power efficiency.

More severe limitations on the unit-cell size need to be taken into account, if the goal is to enable arbitrary shaping of reflected waves (in the far zone). As discussed above, in general, two different configurations are needed: diffraction
gating (metagrating) and nonlocal metasurfaces. In the first case, the period is of the order of the wavelength and we need to “activate” only one or two elements (the rest is to be set far from the resonance). In the second case, the period is larger than λ but still comparable to it. As demonstrated in [57], in this case we need about 8 to 10 unit cells per period, and all the cells are in general configured differently to enable efficient anomalous reflection to large angle. We see that to enable both these regimes it is appropriate to select the unit-cell size not larger than about λ/5. In view of the choice of the unit cell as a cluster of four patches with four tuning elements connected between the patches, selection of this size enables the most general reconfigurability of intelligent reflectors.

4) Choice of the substrate permittivity and thickness: As is well-known from the theory of high-impedance surfaces, the choice of higher permittivity values improves the stability of the resonant frequency with respect to the incidence angle and allows reduction of the substrate thickness, but decreases the bandwidth, e.g. [61]. For the applications in reconfigurable surfaces, the angular response can be adjusted by tuning the unit cells, while wider frequency bandwidth is desirable for robust operation. In addition, there is also the practical consideration of availability of cheap and fabrication-friendly low-loss substrates. In view of these considerations, we select moderate-permittivity low-loss dielectric substrates. The thickness of the substrate mainly determines the effective inductance of the equivalent parallel resonant circuit which models the high-impedance circuit [48], [49]. Higher inductance means higher frequency bandwidth, meaning that thicker substrates are preferable. Naturally, the thickness should be still considerably smaller than the wavelength.

5) Proof-of-concept study: These general design considerations have been recently validated for plane-wave illuminations in two orthogonal planes, parallel to the crystal axes of an array of square patches [36]. The unit cell of this metasurface is schematically shown in Fig. 1(a). In these illumination scenarios it is enough to consider only pairs of loaded square patches, because there is no current over the other two loads in each patch cluster. The load impedance was assumed to be complex, with variable capacitance and resistance. The studied range of capacitance variations was 1 pF to 5 pF, corresponding to the parameters of commercially available chip varactors for the target frequency range (about 5 GHz) and similar to the ranges of varactors used in recent experimental studies of tunable high-impedance surfaces [53], [54]. The tunable resistance was assumed to be varying from 0 to 5 Ohm, again in harmony with the parameters of commercial chip varistors, and allowing comparison with ideal, lossless structures.

The most critical issue was to validate the hypothesis that it is possible to realize near-perfect anomalous reflectors, not limited to any angular sectors, by tuning only load reactances of unit cells, while their sizes and shapes remain fixed and the same for all cells. The only known earlier realization of this functionality relied on careful optimization of sizes of subwavelength patches forming super-cells of a periodical lattice [57]. The results presented in [36] have shown that comparable performance can be achieved also using the proposed topology of fixed-size arrays of patch clusters with variable reactive loads, with practically realistic values of load capacitances. The study of tunable absorber configurations has shown that the same metasurface can be indeed configured to the regime of full absorption of incident plane waves of both TE and TM polarizations, as depicted in Fig. 1(a), in a wide range of incidence angles.

B. From the proof-of-concept unit cell to fully reconfigurable implementable unit cell design

Practical implementation of the unit cell design starts from the structure we studied in [36]. However, that is only a basic proof-of-concept design and there is still a long way toward industrial realization. For example, some open questions include: How should the chip be connected to the patches and how would the connectors affect the performance of the metasurface? Is the design compatible with fabrication technologies? How can the capacitive and resistive loads be optimally realized in practice? In this and the following subsections, we discuss all these practical issues and, based on these considerations, we propose a practically-realizable intelligent metasurface design.

1) One chip instead of four chips per cluster: The cluster topology shown in Fig. 1(a), with four chips connecting the patches, is not cost effective or practical to populate. In addition, more complex routing lines are required to control the chip when communications between the chips are demanded for programmability. Moreover, when the unit cell size is in the 10 mm order (λ/6 at 5 GHz), squeezing four chips inside such a small area demands advanced fabrication technologies, something which again raises the cost. A simple and effective way to reduce the complexity of the cluster design is to use just one chip inside each unit cell, as shown in Fig. 1(c). To enable the same functionalities, one chip is now essentially supporting at least four RC pairs, e.g., connecting the four neighbouring patch pairs. With this simplification and the change of the RC connection from the middle of the edge of the patches to the corner of the patches, the metasurface can still support the desired functionalities. In addition, we note that in this way we also select the best position for the load connection, i.e., the patch corner, because that is where the surface charge density maximum across the patch is located for illumination in both primary incidence planes of the structure shown in Fig. 1(a).

2) Load connection topology inside the chip: Another issue raised in the “one chip per cell” approach we adopt is the choice of the patch-load-patch connecting topology, as well as the number of loads the chip must internally implement. For practical reasons related to unavoidable parasitics inside the chip, as detailed in [44], an X-shaped connection was finally adopted with four independent loads connecting the corner of each patch to the common ground pin in the center of the chip. This load topology can implement the absorber functionality (four loads with identical RC values) by connecting pairs of patches, readily extending the proof-of-concept cell design, while also accommodating other functionalities, e.g., anomalous reflection and polarization conversion (two different RC values for each of the two diagonal connections). Finally, note that this topology still allows us to control the
spatial dispersion of the structure, which is important for TM-polarized incidence, by tuning the impedance of the ground connection.

3) Out of plane chip placement: While placing the chip in the center of the unit cell in the horizontal plane is intuitive for the sake of symmetry, a key decision that should be made is the placement of the chip in the vertical sense. Three options were examined: (a) on the top patch layer, (b) embedded inside the substrate, and (c) below the ground plane, as schematically shown in the respective panels of Fig. 2. Option (a) was abandoned because the chip would interfere with the incident radiation causing reflections and disrupting the absorber performance; additionally, a large number of through vias (TVs) would be required to pass communication power lines behind the backplane, and these vias would complicate the electromagnetic response especially for TM polarization where the electric field possesses a parallel component to them; finally, as TVs cannot be fabricated (drilled) directly below the chip, traces and landing pads would be required to displace them outside the chip footprint, which would also disrupt the metasurface topology. Option (b) was also abandoned because embedding the chip involves costly non-standard fabrication processes, it excludes probing and servicing malfunctioning chips post-fabrication, and also requires a large number of blind vias (which are thicker than TVs). The optimal option for chip placement is behind the backplane, with only four TVs penetrating it to connect to the back-side of each patch, as shown in Fig. 2c. From the point of view of electromagnetic design, the placement below the ground plane ensures that the electromagnetic environment ‘seen’ by the incident waves is controllable and isolated, because all the auxiliary chip wiring does not affect wave propagation being shielded behind the backplane.

Finally, a last issue related to the chip placement in the vertical sense is the positioning of the four TVs connecting the chip RF terminals to the patches. While in mushroom structures the vias connecting the patches to the ground plane are located at the center of the patches, here we stress that the optimal position for connecting the patches and the chip is at the patch corner which is the closest to the chip. The corner of the patch is where the surface current density is at its maximum for illumination in both primary incidence planes and therefore the impedance introduced by the chip can more widely control the metasurface response.

C. Integrated circuit design

In this section, the integrated circuit design of the metasurface loading elements is presented. More detailed information can be found in [44]. The integrated circuit aims to satisfy metasurface performance, cost and power constraints. The metasurface loading element simplified circuit is shown in Fig. 3a. It utilizes MOSFETs to implement both the variable capacitance (varactor) and variable resistance (varistor) elements. In the schematic, the varistor $M_2$ is adjusted through a gate voltage $V_R$, biasing voltage and the varactor $M_2$ is adjusted through $V_C$, biasing voltage. An RF choke inductor $L_1$ is used to block the RF signal to short on the low impedance node $V_C$. Similarly, a DC block capacitor $C_1$ is used to ensure the $V_C$ voltage shorting to ground through $M_1$. The circuit forms a parallel connection RC load which, at its steady-state, will draw negligible current due to gate leakage.

The simulated RC range shown in Fig. 4 was obtained by schematic simulations in Cadence Virtuoso. A 180 nm tech-
Having outlined the basic considerations that have led us to the approximate dimensioning of the metasurface unit cell in the lateral (cell and patch widths) and vertical (dielectric thickness) directions, and implementation rules for the custom IC, additional manufacturing limitations have been taken into account in the design.

An important design aspect is manufacturability of the through vias (TV) that will connect the IC RF terminals (on the back side of the metasurface) to the patches (on the front side of the metasurface). The available technology for TVS requires for a maximum 1:8 aspect ratio, i.e., the thickness of the material stack for the mechanical drilling of TVS must not exceed 8 times the diameter of the via, so as to achieve sufficient copper via electroplating. In contrast, blind vias (BV) require a 1:1 aspect ratio, leading to relatively thicker cylinders. Simulations and fabrication concepts have recommended an approximate thickness of the dielectric stack penetrated by the TVS to be 2.4 mm, and therefore a TV diameter of 0.3 mm was chosen. It is being numerically verified that increasing the diameter of the TVS leads to small increase in the resonance frequency, without degrading its quality factor (the amplitude of the reflection coefficient remains $-30$ dB or lower). For example, for TV diameter increase from 270 to 300 $\mu$m, the resonance frequency increases by roughly 70 MHz, which can be compensated by slightly increasing the capacitance introduced at the chip terminals, well within the tuning capabilities of the chip. Finally, it should be noted that all vias are copper electroplated so that they are essentially hollow metallic cylinders, inset of Fig. 5(a); although our EM simulations were conducted assuming solid-copper vias, for the sake of simplicity, additional numerical simulations have confirmed that the two models are equivalent owing to the small skin depth ($1 \mu$m at 5 GHz).

The next practical considerations concerned the dielectric material choices to be used above and below the metal backplane. Initial fabricated prototypes used high-frequency graded Rogers RT/duriod 5880 dielectric ($\varepsilon_r = 2.20, \tan \delta = 0.0009$) on the top side, and regular FR4 dielectric (Hitachi MCL-E-679FGB) on the back side, where low loss is not as important to minimize cost. Fabrication of the initial 3-layer substrates, e.g., as in Fig. 2(c), has resulted in significant warping (bending) of the printed circuit board after lamination of all build-up layers, even for small metasurface substrates, e.g., 10 cm by 10 cm, due to mismatch of the thermal-expansion coefficients of the two dissimilar dielectrics. For this reason, subsequent designs used the same dielectric substrate type, namely Panasonic Megtron7N dielectric ($\varepsilon_r = 3.35, \tan \delta = 0.0020$), with laminates and prepreg layers symmetrically positioned above and below the backplane, thus minimizing warping. Given the fixed dielectric thicknesses available, a stack of Megtron7N laminates and prepregs has been symmetrically laid up to achieve the total thickness required and ensure that warpage has been diminished; indeed, the homogeneous nature of prepregs and laminates used has yielded minimum warpage. Figure 5 provides a view of the
Ltr: The minimum values of these two offsets were chosen as δx = 0.4 mm and δy = 0.2 mm, respectively, and are depicted in Fig. 6. Please note that the resulting unit cell exhibits structural anisotropy, enforcing only mirror symmetry and not four-fold symmetry, meaning that the two normally impinging polarizations (x- and y-polarized) will behave differently. This compromise arose from limitations stemming from the RC values due to the physics of real chips and the size of the patches, and will be discussed in detail in Section III.

E. S-parameter modeling and simulation

In order to efficiently model and simulate this multi-parametric EM problem, we rely on S-parameters, enabled by the metallic backplane, which effectively decouples the metasurface- and the chip-side designs. Thus, using the backplane as a common reference ground, we can model the chip with four lumped ports, Fig. 7(a), and the incident and scattered plane waves with Floquet ports, Fig. 7(b). The lumped ports are 50 Ohm-referenced and fed by Touchstone data (complex spectra) depending on the IC architecture, i.e., ranging from a single generalized four-port network (most complicated case) to four identical decoupled RC loads (simplest case). The Floquet ports are defined for a given plane wave direction, i.e., a (θ, φ) pair, both polarizations (TE and TM), and are placed at the front and back side of the unit cell, at planes perpendicular to the z-axis; periodic Bloch-Floquet conditions are applied to the remaining four boundaries enclosing the unit cell, emulating infinite periodicity. Please note that in the case of uniformly configured chips we use a total of four Floquet ports: as the unit cell is subwavelength only the zero-order (specular) diffraction order is propagating and we in general need to consider both linear orthogonal polarizations. In the case of inhomogeneous unit cell setting where a supercell with periodicity exceeding the free-space wavelength is formed, such as the anomalous reflection scenario in Section III-B, the number of Floquet ports increases to accommodate the other propagating diffraction orders.

Concluding this part with restrictions related to the chip packaging and assembly, firstly, it was verified that laterally offsetting the BV connecting the ground pin of the chip (which is the one in its middle) to the metasurface ground plane has no effect on TE polarized absorber performance, our main target. Therefore, in the simulations performed in this work a single BV was placed in the center of the chip footprint. However, in the fabricated device [44], a copper trace brings this pin outside the chip footprint where the BV will short it to the metasurface ground plane, so that the chip terminals and the patches have a common reference ground. The length and path of this BV trace is expected to influence oblique TM performance due to mutual coupling with the RF terminal traces because of the current flowing through the BV (which is zero for TE polarization). Finally, and in order to model the device as thoroughly as possible, one would need to quantify the effect of the solder balls used to electrically connect the RF terminals of the chip to their respective pads on the metallization layer [44].
stated in Section II.D, we have intentionally designed the chip with its four RF ports decoupled, so that they can be directly replaced by lumped loads, with their RC values falling inside the prescribed IC map, Fig. 4. This allows us to rapidly find the chip configuration, in terms of RC pair, that leads to perfect absorption at a given frequency and polarization: For a given incident plane wave direction, we numerically evaluate the 8-port S-parameters of the unit cell with full-3D EM simulation; then, we attach a prescribed RC load to all four lumped ports (passed as 1-port Touchstone data) and, finally, we extract the scattered spectra at the remaining four Floquet ports, corresponding to the two polarizations (TE and TM) and to the two sides of the unit cell (top/back side, i.e., reflected/transmitted). Iterating over the RC loads using an optimizer, we can rapidly identify the optimal configuration for perfect absorption at a given frequency and polarization. However, note that changing a geometric/EM parameter of the structure and/or the incident plane wave direction, e.g., for oblique incidence absorption, requires for the numerical recalculation of the 8-port network S-parameters with a new full-3D EM simulation, which is computationally intensive (time consuming) due to the complex geometrical features. These simulations were conducted in CST Microwave Studio, using the 3D frequency domain solver with broadband sweep and the Design Studio environment for the 8-port S-parameter tasks.

III. ELECTROMAGNETIC DESIGN OF THE COMPLETE UNIT CELL AND THE MULTI-FUNCTION PERFORMANCE

In this Section we present the metasurface unit cell design, taking into account all the aspects and restrictions discussed in Section II. Prime focus is given on wide-angle tunable absorber functionality by thoroughly analyzing its performance; steering and polarization conversion functionalities are also assessed.

A. Perfect Absorption

The main functionality implemented by our metasurface device is tunable perfect absorption (PA) of plane waves, which can impinge from a large cone of incidence directions and both polarizations. As discussed, for the IC-loaded unit cell to achieve PA at a given frequency, polarization, and direction of incidence, we must properly tune both the resistive and reactive (capacitive) part of the equivalent lumped loads representing the IC. Given the tuning ranges of the varistor and varactors in the chip design, Section II.C, the optimization of the free structural parameters of the unit cell design is performed. The reference optimization case is PA at 5 GHz, normal \( y \)-polarized incidence, \( R_s = 2.1 \) \( \Omega \), and \( C_s = 3.2 \) pF; these RC values lie approximately in the middle of the chip range, thus allowing maximum tunability. The free structural parameters of the design are essentially the cell and patch width, \( w_c \) and \( w_p \), respectively, under the condition that the through vias are placed as close as possible to the inner patch corners, which is limited by the fabrication thresholds \( \delta x \) and \( \delta y \) discussed in Section II.D. In order to unveil the underlying design rules, one can parametrically calculate the reflection amplitude as a function of \( w_c \) and the newly defined filling ratio, \( \rho_f = 2w_p/w_c \), with the results presented in Fig. 8.

Full-wave EM simulations of the unit cell are employed, conducted in CST Microwave Studio, using the frequency-domain solver with tetrahedral mesh. An approximately linear trendline emerges, showing that smaller cells require for proportionally large patches to resonate for the same external load values. For our design, PA is achieved at the optimal values of \( w_c = 9 \) mm and \( \rho_f = 0.77 \), i.e., \( w_p = 3.465 \) mm. For these parameter values, the length and angle of the metal traces connecting the RF terminals of the chip to the landing pads of the through vias defined in Fig. 6 are \( L_{tr} = 0.41 \) mm and \( \theta_{tp} = -116.5^\circ \), respectively. The resulting unit cell and structural dimensions are summarized in Fig. 9 in millimeters.

Having completed the selection of all the structural dimensions, the performance for PA functionality is assessed. The amount of control imparted by resistance and capacitance tuning is depicted in Fig. 10, where \( C \) and \( R \) control the resonance...
frequency and quality factor (resonance “depth”), respectively; these spectra are for normal y-polarized incidence. The resonance bandwidth is over 100 MHz (or 400 MHz) measured at $-10$ dB (or $-3$ dB). The respective tolerance values of $C$ and $R$ for near-perfect absorption at 5 GHz are quantified in terms of the achieved reflection amplitude, $|r| < -10$ dB, Fig. 11. The attained range falls well within the varistor and varactor range of the chip thus allowing tuning and possible fabrication-deviation compensation.

The last step in validating the performance of the absorber is to quantify the coverage range, in terms of oblique incidence angle and/or frequency detuning, allowed by the available RC map of the IC. The S-parameter block modeling approach described in Section II.E is employed in order to efficiently calculate the optimal load impedance values for various combinations of incidence direction, polarization, and frequency. The results are presented in Fig. 12. Oblique incidence coverage is up to 60° for both TE and TM polarization planes as defined in Fig. 9(a), i.e., with the electric field always primarily polarized along the $y$-axis, where the lateral distance between the through vias is smallest. Frequency tuning is limited to ±50 MHz, owing to the sharp absorption resonance and the limited capacitance range.

1) Cross-polarized absorption performance: Since the targeted metasurface functionality was widely-tunable perfect absorption for at least one polarization, the unit cell design was allowed to be anisotropic, i.e., to exhibit mirror symmetry but not four-fold symmetry, as depicted in Fig. 9(a). In this regard, $y$-polarization (i.e., $E_y$ in TE and $E_{yz}$ in TM) will outperform $x$-polarization, for perfect absorption on the given RC range. We opted for this trade-off, in order to have at least one of the polarizations perfectly absorbed and with wide oblique incidence tunability; trying to accommodate both polarizations perfectly absorbed and with wide oblique incidence tunability while enforcing four-fold symmetry, as shown in Fig. 9(a). This led to meager simulated performance for both and/or very limited oblique incidence coverage. Nevertheless, we assessed the cross-polarized absorber performance, with the results summarized in Fig. 13. As expected, very limited coverage is offered, e.g., only highly-oblique $x$-polarized (TE) incidence can be perfectly absorbed for the given RC coverage, while suboptimal performance, e.g., reflection as high as $|r| \approx -10$ dB, can be attained for normal incidence.
Fig. 13. Cross-polarized tunable absorber performance at 5 GHz. The colormap corresponds to reflection amplitude of x-polarized normal incidence as series RC lumped loads are varied. Optimal RC values for oblique incidence (5° steps) in TE and TM planes are superimposed, with blue triangles and red squares, respectively. The inset depicts how TE and TM planes are defined in the anisotropic unit cell for the cross-polarized case.

Fig. 14. Double absorption resonance arising for very oblique TE incidence angles. (a) Reflection amplitude spectra for θ = 60°, y-polarized, Rs = 0.35 Ω, and two different values of series capacitance Cs. (b) Reflection amplitude at 5 GHz, depicting the two optimal series-RC configurations available.

2) Double resonance at highly oblique incidence: It must be noted that highly oblique incidence cases give rise to an interesting phenomenon of dual absorption resonance. For instance, in the θ = 60° TE y-polarized case, we can clearly see two minima of reflection spaced by approximately 100 MHz, Fig. 14(a). Naturally, the unit cell RC values can be tuned to optimize either of the two resonances for absorption at the desired frequency, as depicted in the tolerance map of Fig. 14(b). The series resistance is approximately the same, 0.35 Ohm in this case, while the series capacitance can vary up to 1 pF. This double resonance gradually emerges forθ > 45°, being more pronounced for y-polarized waves in the C-band (5 GHz) for our unit cell design.

B. Anomalous Reflection

The independent control over the RC values in each unit cell enables us to perform wavefront manipulation operations, such as anomalous reflection. Although the reflection amplitude is not particularly high within the realizable RC range by the chip, the coverage of the reflection phase is quite large, i.e., from -170 degrees to 170 degrees, as shown in Fig. 15(a). As a result, anomalous reflection can be achieved if we lower the requirement on the reflection amplitude. Anomalous reflection is obtained by grouping several unit cells into a supercell and allowing the reflection toward the desired direction while forbidding the scattering to other directions by selectively promoting a single propagating diffraction order over the others. Utilizing different supercell sizes and relying on different diffraction orders, the anomalous reflection direction can be tuned with a quasi-continuous angle coverage [36]. To demonstrate the anomalous reflection effect, we consider a supercell made of N = 8 unit cells, which will support anomalous reflection from normal incidence toward the 56.4 degrees, according to θ = arcsin(λ0/D) [8], [36], where D is the extent of the supercell and equals Nλ to steering inside the xz plane for example. In this supercell configuration, which is different from the one in Fig. 7 there are three ports, a, b, and c, corresponding to the three propagating diffraction orders m = 0, +1, −1 (since λ0 < D < 2λ0). Note that transmission and polarization conversion is negligible and, thus, power collected by the corresponding ports is negligible. Subsequently, we perform an optimization while constraining the RC values within the realizable range. Note that in order to speed up the optimization process one can use as an initial setting for the RC values those dictated by a linear phase profile along the supercell, i.e., φ(x) = φ0 − (2π/D)x [36].

The required RC values for the 8 unit cells after optimization are shown as white dots in Fig. 15(a). With this configuration, the normally incident wave with polarization E_y is reflected to 56.4 degrees without prominent scattering to the specular direction (port a) or the m = −1 diffraction channel (−56.4 degrees, port c), as the scattered E_y field pattern shows in Fig. 15(b). The amplitude of the reflection coefficient is |S_{aa}| = 0.38, which means that 14.4% of the power is reflected toward the desired direction. Meanwhile, the amplitudes of the reflection coefficients to the other two directions are |S_{0a}| = |S_{0c}| = 0.05. The absorbed power by the metasurface is given by Abs ≈ 1 − ∑_{n} |S_{na}|^2 = 85.1%, where n runs through the propagating reflection diffraction orders {a, b, c}; an anomalous reflection efficiency of Eff = |S_{aa}|^2 / ∑_{n} |S_{na}|^2 = 96.7% is calculated, meaning that...
96.7% of the scattered power goes to the desired direction. Finally, we emphasize that through the same principle of locally modifying the reflection phase, we can achieve more wavefront manipulation operations, such as retro-reflection and focusing [8], [66].

C. Polarization Conversion

Next, we exploit additional advantages of the proposed unit cell configuration. Organizing patches in groups of four and using a single chip to control them was judiciously chosen to save resources and additionally results in a geometrically isotropic unit cell design that can have polarization independent response. On the other hand, however, it offers the distinct capability of electrically breaking the four-fold symmetry rotational leading to polarization conversion.

Here, as a demonstration of the opportunities for polarization control we demonstrate linear polarization conversion to the orthogonal state. To this end, we appoint asymmetric load values to the four patches. More specifically, we use the complex loads \( R_1, C_1 = \{ R_3, C_3 \} \) and \( R_2, C_2 = \{ R_4, C_4 \} \) to electrically emulate the geometric structure of a 45-degree tilted cut wire, which has been shown in the literature to result in efficient linear polarization conversion [11]. We find that the optimal values are \( R_1, C_1 = \{ R_3, C_3 \} = \{ 0.35 \Omega, 2.6 \text{ pF} \} \) and \( R_2, C_2 = \{ R_4, C_4 \} = \{ 3.4 \Omega, 4.8 \text{ pF} \} \), since they allow for the maximum disparity regarding the capacitance values between on- and off-diagonal elements, while retaining the total resistance at the lowest possible levels. (Note that for the used values of \( R \) and \( C \) the reactances dominate over the resistances at the neighborhood of 5 GHz.) We succeed in getting perfect polarization conversion to the orthogonal state, i.e., \( R_{co} = 0 \) at 5.05 GHz, as depicted in Fig. 16. However, having used resistance values as high as 3.4 \( \Omega \) for the off-diagonal elements the absorption is high (\( A = 0.61 \) at 5.05 GHz), limiting the cross-polarized power transmission to 0.37 [Fig. 16]. The remaining power is found in transmission (not shown) which is in all cases small due to the presence of the (perforated) backplane.

Fig. 16. Linear polarization conversion by electrically breaking the four-fold symmetry using loads \( \{ R_1, C_1 \} = \{ R_3, C_3 \} = \{ 0.35 \Omega, 2.6 \text{ pF} \} \) and \( \{ R_2, C_2 \} = \{ R_4, C_4 \} = \{ 3.4 \Omega, 4.8 \text{ pF} \} \) to emulate a 45-degree tilted cut wire. Complete polarization conversion to the orthogonal state is observed. The cross-polarized power coefficient is 0.37 and absorption amounts to 0.61. The remaining power is found in transmission (not shown) which is in all cases small due to the presence of the (perforated) backplane.

the constraints on the IC range could be relaxed so as to be in line with the practical RC values available by affordable chip designs.

IV. CONCLUSIONS AND FUTURE PROSPECTS

Based on the introduced design procedure and the implementation constraints, we presented a fabrication-ready tunable microwave metasurface which offers continuous local control over the complex surface impedance and allows multiple reconfigurable functionalities. The dynamic control has been achieved by assembling a customized integrated-circuit chip in each unit cell and co-designing the electromagnetic and electronic components to fulfill the desired functionalities. The structure’s performance as a tunable perfect absorber, tunable anomalous reflector, and polarization convertor has been demonstrated, highlighting the multi-functional character of the proposed metasurface structure.

HyperSurfaces, combining the EM design aspect–detailed in the preceding Sections–with appropriate hardware and software, enables themselves to act as hypervisors for metasurface functionalities. In other words, using well-defined application programming interfaces and communication protocols [64], [65], a computer, a software service, or an individual can deploy and chain together multiple EM functionalities over the same HyperSurface. For instance, complex alterations over the phase, amplitude and polarization can be deployed over a HyperSurface at the same time. Recent studies have also modeled the wavefront detection as a software service, allowing a HyperSurface to concurrently sense and modify an impinging wave and enabling real-time adaptive operation [66], [67].

The inter-networked deployment of multiple HyperSurface units within a space yields a programmable wireless environment (PWE) as a whole, within which EM propagation becomes software-defined [68]. For instance, applying
HyPerSurface-coatings over walls, ceilings and other large surfaces in a floorplan, yields an indoors PWE. A central server can orchestrate the EM functionalities deployed to each HyPerSurface unit, matching it to the needs of mobile users present in the floorplan. In this manner, studies have showcased novel potential in PWE-assisted channel equalization, multipath fading, Doppler Effect mitigation, long-range wireless power transfer and physical-layer security [69]. These capabilities can enable novel, holistic data networking approaches, which will adaptively and jointly tune the data control logic and the physical propagation characteristics, to optimally serve the user needs.

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