Improvement of Power Converters Performance by an Efficient Use of Dead Time Compensation Technique

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Abstract: The advent of renewable energy resources and distributed energy systems herald a new set of challenges of power quality, efficient distribution, and stability in the power system. Furthermore, the power electronic converters integration has increased in interfacing alternate energy systems and industries with the transmission and distribution grids. Owing to the intermittency of renewable energy resources and the application of power electronic converters the power distribution faces peculiar challenges. The dead-time effects are among the main challenges, which leads to the distortion of third harmonics, phase angle, torque pulsation, and induction motor current, causing severe quality problems for power delivery. To tackle these problems, this paper proposes a novel dead time compensation technique for improving the power quality parameters and improving the efficiency of power converters. The proposed model is simulated in MATLAB and the parametric equations are plotted against the corresponding parametric values. Furthermore, by implementing the proposed strategy, significant improvements are attained in the torque pulsation, speed, and total harmonic distortion of the induction motor. The comparisons are drawn between with and without dead time compensation technique, the former shows significant improvements in all aspects of the power quality parameters and power converters efficiency.

Keywords: industrial microgrid; dead-time compensation; power quality; variable frequency drive; third harmonic distortion; induction motor

1. Introduction

The problems at the distribution side of electrical power systems are categorized under the umbrella of power quality problems consisting of distortion in phase angle, voltage waveforms, fundamental current, as well as frequency. The definition of power quality has been used to include several issues related to a power supply such as voltage and current quality, the stability of power supply, quality of the overall system, and efficiency of supply and consumption of power [1]. These problems primarily stem from the non-ideal characteristics of power electronic equipment. The power providers are warranted to ensure stable, smooth, and safe power supply conforming to a pure sinusoidal voltage signal to the end-user [2]. At present-day, with the worldwide energy
crisis becoming increasingly conspicuous and environmental pollution becoming increasingly serious, worldwide renewable generation technologies have been developed rapidly \cite{3-5}. However, the introduction of power electronics, necessitated by the presence of renewable energy sources (RES) at the distribution junction inflicts distortions in current and voltage causing difficulties in ensuring smooth electric supply \cite{6}. Contemporary research is focused on finding novel ways to achieve the standards of power quality and with the forecast of incessant RES growth will be a major challenge for years to come. The adverse impacts of less than ideal power quality are amply documented in \cite{7}. Almost all of these benchmarks are application-based, there have been almost tens of rules established by the Institute of European Commission (IEC) for the power quality. Although the most important power quality standard is IEC 61000-2-2, which ensures that the voltage harmonic levels in the power system do not surpass the compatibility levels \cite{8}.

Non-linear power electronic products have been finding a greater market in the residential and industrial sectors owing to their cost-effectiveness and high efficiency. Variable frequency drives (VFDs), power factor (PF) correction equipment, and switch-mode supplies (SMPSs) improve the overall system efficiency \cite{9}. Additionally, industrial application for power converters is also increasing. This has shifted the overall research focus on the development of state-of-the-art power converters \cite{10}. Pulse width modulation (PWM) and voltage source inverter (VSI) are generally installed for motor drives. Ideally, the turn-off-on of the two power devices at each leg of an inverter is complimentary. However, in the practical application, the time delay in the turn-off of one and turn-on of the other device may lead to short-circuiting of DC-link due to momentary simultaneous conduction \cite{11}. To address this problem a blank duration, called dead-time, is inserted between the switching on of the one device and off of the other ensuring safe operation \cite{12}. The effective voltage is affected by the dead time at lower frequencies, which further distorted the inverter output voltage and results in additional components of low-order harmonics. Moreover, this also causes distortion in the current waveforms \cite{13}. These effects necessitate devising novel dead-time compensation strategies detailed in \cite{14}. The strategies are categorized in two broad types: (1) feed-forward compensation entailing calculation of error stemming from the dead time and the concomitant forward voltage drop, and their subsequent compensation through control algorithms; and (2) stringent observation of disturbance magnitude and the subsequent proportionate compensation.

The first category of compensation strategies is contingent on the detection of current polarity-made difficult by high-frequency disturbances, and a phenomenon called “zero-current-clamp” \cite{15}. Current polarity detection circuits are undesirable due to complicated structures and extra cost \cite{16}. The low pass interference filtering strategy is rendered inefficient due to the phase lag they generate inducing new errors. Consequently, the current research is focused more on uncovering alternative means of current polarity detection, and interference filtering devoid of the phase lag problem. One such strategy involves the use of current reference value to offset the influence of clamp and avoid the repeated near-zero crossing of the actual sampled current \cite{17}. This strategy, however, suffers from the drawback of potential error between the actual and reference current as well as its suitability for only closed-loop control of current. Some have devised a strategy of calculating the current polarity angle and place a high significance on the angle between the current vector and rotor flux angle \cite{18}.

Similarly, some have employed the method of dead-time and forward voltage drop induced error calculation in off-line or on-line mode, followed by the addition of the error to power devices’ driving pulses \cite{19}. In \cite{20}, the dead-time effect is aptly compensated but at the expense of inducing forward voltage drop. Contrarily in \cite{21}, the forward voltage drop is addressed while ignoring the dead-time. There also exist some models which take both the dead-time and forward voltage drop into consideration and both the factors are separately analyzed suggesting the possibility of compensating both the effects and found them independent of each other \cite{22}. The error time and error voltage are mutually convertible as per the average value theory. Since inverter legs operate at disparate legs, the error of each can be independently measured to achieve more accurate compensation. This will involve constant estimation of error as the switching frequency changes \cite{23}. There is however the
danger of unexpected current clamp in this method when the compensation suddenly changes while current crosses zero.

In the second category of dead-time compensation techniques, the current direction is not necessary, and a complex model of the adaptive voltage compensation algorithm is implemented to suppress the dead-time effect [24]. A fast and a slow response disturbance observer are employed which makes a distinction between the back EMF and disturbance voltage, leading to voltage error correction [25]. However accurate motor parameters and complex calculations are major downsides to this approach. The effects of parasitic capacitances of power devices are also important in the context of the compensation method [26]. The dead-time causes an error in the modulation voltage. In [27], the dead-time compensation is utilized for the modulation error and the effects of the dead time have been analyzed on three-level inverters. However, the proposed technique on [27] isn’t used to eliminate the consequences of dead time effect on power quality.

In this paper, the five parameters of power quality have been improved by a novel DTC technique and the consequences of dead time effect on power quality have been eliminated. A schematic of an industrial microgrid with DTC is given in Figure 1. In this figure, industrial motors make up the majority of the industrial microgrid loads. Introducing DTC in power converters can help in curtailing the non-ideal nature of power electronics. The current research attempts to alleviate the effects of dead time on power converter parameters, for instance, curtailing fundamental voltage, distorting current waveforms, phase angle, and third harmonic as well as torque pulsation. The parametric equations for all the parameters are derived for normal scenarios and dead time compensation scenarios. The model is simulated in MATLAB with two different cases and the results, with and without the proposed model application, are drawn.

The article is organized as follows: Section 2 delineates the model structure for power quality enhancement with the DTC technique; Section 3 investigated the proposed DTC method along with the mathematical modeling of this method; Section 4 explains the outcomes of the research work with a discussion on the importance of the research to the field, and Section 5 lists the conclusions derived from the research endeavor.

Figure 1. Conceptual view of an Industrial Microgrid.
The article is organized as follows: Section 2 delineates the model structure for power quality enhancement with the DTC technique; Section 3 investigated the proposed DTC method along with the mathematical modeling of this method; Section 4 explains the outcomes of the research work with a discussion on the importance of the research to the field, and Section 5 lists the conclusions derived from the research endeavor.

2. System Modeling

The model of power quality improvement involves the incorporation of high-level pulse width modulation, in this case, IGBT, into the electrical switching system while retaining the switching frequency at 2–15 kHz levels [21]. To cope with the non-ideality in a small delay, called dead time, is inserted in the operation to avoid short circuits. Meanwhile, the dead time causes various parameters deterioration, therefore power quality analysis is carried out which mostly focused on the reduction of the negative consequences of dead time. The proposed method consists of dead time compensation (DTC) strategy for stabilization of 3 phase induction motors in the open-loop system using variable frequency drive (VFD) to govern the speed required for AC motors besides the offsetting of the adverse effects of DTC. A schematic of the proposed model is outlined in Figure 2. It consists of “volt-per-Hz” drive the design of which is delineated in the following. A specially minted control mechanism is applied for maintaining a fixed level of magnetizing current. Additionally, variable stator voltage support is also implemented.

Since dead time is directly proportional to PWM signal output; the increase or decrease of one directly decreases or decreases the other resulting in a closer-to-original voltage pulse. Accordingly, the current study employs two methods for correcting dead time induced distortion: full correction methodology which factors in the phase angle magnitude and initiates a novel s/w for enhanced output; and partial correction methodology which helps the PWM on-chip hardware. At least one of these correction methodologies is pertinent to improve the PWM inverter parameters. The increasing parameters of PWM inverter values used in pair register; need to be kept in check with the help of software. The value is dependent on the transistor and is important for the output voltage in DT. The
partial correction method essentially builds the basis for polarity detection, which is helpful in the improvement of load current waveform, the magnitude of fundamental voltage, phase angle, third harmonic distortion, and induction motor parameters such as current waveform, torque pulsation, and speed. Albeit many shortcomings are concomitant with this method; the current settles at zero at the point of disturbance.

3. Proposed Dead Time Compensation Technique

In this section, the proposed dead-time compensation (DTC) method is investigated. First, the DTC for the PWM inverter is performed. Then, the modeling of the proposed DTC technique is introduced.

3.1. Dead-Time Compensation for PWM Inverter

The design of a three-phase voltage-based inverter is given in Figure 3 where ‘n’ and ‘o’ indicate dc link and induction motor neutral points respectively and IGBTs paired with diodes work as switches. As an example, the effect of dead time and forward voltage drops have been examined in phase A leg. The phase A leg contains four different current paths as demonstrated in Figure 3. The forward voltage drop of IGBT is represented as ‘\(u_{ce}\)’ and that of the anti-diode as ‘\(u_d\)’. From Figure 4, phase A current \(i_a\) is represented by the dashed line in Figure 4. It is established from Figure 4a,b that when current flows from the inverter to load, \(i_a > 0\) and from Figure 4c,d it is evident that \(i_a < 0\) for opposite current direction reverses.

![Figure 3. Two-level inverter-motor system [21].](image)

![Figure 4. Analysis of different current flow paths of phase A. (a) When i_a>0 from D1 (b) When i_a>0 from D2 (c) When i_a<0 from D1 (d) When i_a<0 from D2 [21].](image)
Since the delay in the on-off of IGBTs for this study is extremely small in comparison to the dead time, it is considered negligible. In the beginning, the dead time setting is analyzed. The delays between turn on and off of power electronic devices (IGBTs) are considered negligible in this study as they are very small in comparison to the dead time. One switching cycle of sinusoidal pulse width modulation (SPWM) contains two stages of dead time in which power electronic devices remain in the OFF state. Hence, the load current is forced to pass through anti-parallel diodes D1 or D2 (depending on the direction). Current flows through D2 when \( i_a \) is positive during phase A and is interconnected to the negative terminal as evident from Figure 4b. If \( i_a \) is negative, current flows through D1 with phase A connection setting shown in Figure 4c.

Forward voltage drop occurs when the switching devices pass load current. When the current is positive, the voltage output at phase A is marginally less than the respective DC linkage voltage. In such instances, the IGBT S1 passes current from the positive linkage or D2 passes current from the negative linkage. Similarly, for negative \( i_a \), the voltage output at phase A is marginally greater in comparison to the DC linkage voltage. In this case, positive linkage gets current via D1, and negative linkage via S2. The various permutations of currents flow, and voltage waveforms at different instances are given in Table 1.

### Table 1. The error between the ideal voltage and the actual voltage.

| Time (T) | Ideal O/P Voltage/Actual Voltage | Ideal O/P Voltage | Actual O/P Voltage | Dead-Time Error |
|----------|---------------------------------|-------------------|--------------------|-----------------|
| \( t_0 - t_1 \) | \( D_2 / D_2 \) | \( -V_{dc} / 2 \) | \( -V_{dc} / 2 - u_d \) | \( u_d \) |
| \( t_1 - t_2 \) | \( S_1 / D_2 \) | \( V_{dc} / 2 \) | \( -V_{dc} / 2 - u_d \) | \( V_{dc} + u_d \) |
| \( t_2 - t_3 \) | \( S_1 / S_1 \) | \( V_{dc} / 2 \) | \( V_{dc} / 2 - u_{ce} \) | \( u_{ce} \) |
| \( t_3 - t_4 \) | \( D_2 / D_2 \) | \( -V_{dc} / 2 \) | \( -V_{dc} / 2 - u_d \) | \( u_d \) |
| \( t_4 - t_5 \) | \( D_2 / D_2 \) | \( -V_{dc} / 2 \) | \( -V_{dc} / 2 - u_d \) | \( u_d \) |
| \( t_5 - t_6 \) | \( S_2 / S_2 \) | \( -V_{dc} / 2 \) | \( -V_{dc} / 2 + u_{ce} \) | \( -u_{ce} \) |
| \( t_6 - t_7 \) | \( D_1 / D_1 \) | \( V_{dc} / 2 \) | \( V_{dc} / 2 + u_d \) | \( -u_d \) |
| \( t_7 - t_8 \) | \( D_1 / D_1 \) | \( V_{dc} / 2 \) | \( V_{dc} / 2 + u_d \) | \( -u_d \) |
| \( t_8 - t_9 \) | \( S_2 / D_1 \) | \( -V_{dc} / 2 \) | \( V_{dc} / 2 + u_d \) | \( -V_{dc} - u_d \) |
| \( t_9 - t_{10} \) | \( S_2 / S_2 \) | \( -V_{dc} / 2 \) | \( -V_{dc} / 2 + u_{ce} \) | \( -u_{ce} \) |

As seen from Table 1 the error voltage is the largest for the time range \( t_8 - t_8 \) where \( i_a \) is negative. These analyses for phase A leg can also be applied to three-phase legs. The gate signals and voltage waveforms of phase A as per the pulse generation rule of SPWM are given in Figure 5. It depicts the gate input and dead time incorporated gate input signals for top and bottom switching devices (\( u + g \), \( u - g \)), voltage output (\( u_{\text{ideal}} \)), real output voltage incorporating dead time (\( u_{\text{real}} \)), with both dead time and forward voltage drop (\( u_{\text{real2}} \)).

Accordingly, the corresponding dead time error is given as the difference between \( u_{\text{ideal}} \) and \( u_{\text{ideal2}} \). Similarly, \( V_{dc} \), \( T_s \), and \( T_d \) indicate the DC linkage voltage, switching period, and dead time respectively. It is evident from the left side of Figure 4 that for negative \( i_a \) ideal PWM voltage is greater than the actual PWM voltage. In other words, the ideal voltage output will exceed the actual voltage output. The actual o/p voltage will be slightly less when the forward voltage drop is applied. The voltage varies between \( V_{dc} - u_{ce} \) and \( -V_{dc} - u_d \) when the load current is applied to positive and negative terminal respectively. It is evident from Figure 5 that the deviation from ideal behavior is a function of dead time. Additionally, there is a dependence on the current direction; when altered from load to positive terminal, the output is \( V_{dc} / 2 + u_d \), while changes to \( -V_{dc} / 2 + u_{ce} \) for the opposite current direction.
Figure 4. Analysis of different current flow paths of phase A. (a) When $i_a > 0$ from D1 (b) When $i_a > 0$ from D2 (c) When $i_a < 0$ from D1 (d) When $i_a < 0$ from D2 [21].

Forward voltage drop occurs when the switching devices pass load current. When the current is positive, the voltage output at phase A is marginally less than the respective DC linkage voltage. In such instances, the IGBT $S_1$ passes current from the positive linkage or $D_2$ passes current from the negative linkage. Similarly, for negative $i_a$, the voltage output at phase A is marginally greater in comparison to the DC linkage voltage. In this case, positive linkage gets current via $D_1$, and negative linkage via $S_2$. The various permutations of currents flow, and voltage waveforms at different instances are given in Table 1.

As seen from Table 1 the error voltage is the largest for the time range $t_3 - t_4$ where $i_a$ is negative. These analyses for phase A leg can also be applied to three-phase legs. The gate signals and voltage waveforms of phase A as per the pulse generation rule of SPWM are given in Figure 5. It depicts the gate input and dead time incorporated gate input signals for top and bottom switching devices ($u_+g$, $u_-g$), voltage output ($u_{\text{ideal}}$), real output voltage incorporating dead time ($u_{\text{real}}$), with both dead time and forward voltage drop ($u_{\text{real}}^+$).

Figure 5. Illustration of voltage waveforms and gate signals [21].

3.2. Modeling of the Proposed Dead Time Compensation

The block diagram for 3-phase idealized PWM inverter is illustrated in Figure 6. The DTC model is schematically presented in Figure 7. The model employs an ideal relay possessing two specifications: memory-less, and nonlinearity. The voltage distortion $\epsilon$ depends on $T_d$ the delay time and carrier signal $V_c(t)$ the slope of the triangular waveform. Take the required signal $V_i(t)$ is gradually varying as compared to the high-frequency carrier signal $C$. The ratio $\epsilon/T_d$ is equal to $2V_c/(\frac{T_c}{2})$ the down-slope, the triangular carrier signal $V_c(t)$ and therefore we have $\epsilon = 2V_cT_d/(\frac{T_c}{2}) = 4f_cV_cT_d$. Where $\epsilon$ represents as voltage distortion, $T_d$ is a time delay and $f_c$ represents the frequency of the carrier signal.
\[ T_{\text{err}} = T_{\text{off}} - T_{\text{on}} - T_d + 2T_{\text{com}} \]  \hspace{1cm} (1)

where ‘\( T_{\text{com}} \)’ indicates the compensation time when \( i_a < 0 \).

For phase A:

\[ T_{\text{err},a} = \text{Sign}(i_a)T_{\text{ma}} \]  \hspace{1cm} (2)

where

\[ T_{\text{ma}} = T_{\text{off}} - T_{\text{on}} - T_d + 2T_{\text{com}} \]  \hspace{1cm} (3)

\[ \text{Sign}(i_a) = \begin{cases} 
1 & (i_a > 0) \\
1 & (i_a < 0) 
\end{cases} \]  \hspace{1cm} (4)

When voltage \( U_a \) is positive for phase A, the switching cycle time duration is \( T_a \), and for \( S_1 \), it is \( T_a \). For negative \( U_a \), the switching cycle time duration is \( T_a \) for phase A, and for \( S_4 \) it is \( T_a \).
Correspondingly the relation between effective time \(T_a\) and commanded time \(T^*_a\) comes out to be [21]:

\[
T_a = T^*_a + \text{Sign}(i_a)T_{ma}
\]  

(5)

Similarly, for Phase B and C the same quantities are given as:

\[
T_b = T^*_b + \text{Sign}(i_b)T_{mb}
\]  

(6)

\[
T_c = T^*_c + \text{Sign}(i_c)T_{mc}
\]  

(7)

where IGBTs \(S_3\) and \(S_1\) remain turned on and off respectively for (1) to (7). However, at the neutral point when fundamental voltage is balanced:

\[
V_{dc1} = V_{dc2} = \frac{V_{dc2}}{2}
\]

when \(i_a > 0\):

\[
V_{ao} = \frac{V_{dc}}{2} - 2V_{ce} \quad \text{(when } S_a = 1)  
\]  

(8)

\[
V_{ao} = -V_d - V_{ce} \quad \text{(when } S_a = 0)  
\]  

(9)

\[
V_{ao} = -\frac{V_{dc}}{2} + 2V_{ce} \quad \text{(when } S_a = -1)  
\]  

(10)

when \(i_a < 0\):

\[
V_{ao} = \frac{V_{dc}}{2} + 2V_d \quad \text{(when } S_a = 1)  
\]  

(11)

\[
V_{ao} = V_d + V_{ce} \quad \text{(when } S_a = 0)  
\]  

(12)

\[
V_{ao} = -\frac{V_{dc}}{2} + 2V_c \quad \text{(when } S_a = -1)  
\]  

(13)

Supposing no change in the direction of current, (8)–(13) gives:

\[
V_{ao} = S_a \left( \frac{1}{2}V_{dc} + V_d - V_{ce} \right) - \text{Sign}(i_a)(V_{ce} + V_d)  
\]  

(14)

When voltage drop increases with respect to current:

\[
V_{ce} = V_{ceo} + r_{ce}|i_a|  
\]  

(15)

\[
V_d = V_{do} + r_{rd}|i_a|  
\]  

(16)

Combining (15) and (16) with (14) gives:

\[
V_{ao} = S_a \left( \frac{1}{2}V_{dc} + V_d - V_{ce} \right) - \text{Sign}(i_a)(V_{ce} + V_d)  
\]  

(17)

As per volt-second balance theorem:

\[
S_a = \left[ \frac{T^*_a + T_{ma}\text{Sign}(i_a)}{T_s} \right] \text{Sign}(U_{a_{\text{ref}}})  
\]  

(18)

\[
V_a = \left[ \frac{T^*_a + T_{ma}\text{Sign}(i_a)}{T_s} \right] \left( \frac{1}{2}V_{dc} + V_d - V_{ce} \right) \text{Sign}(U_{a_{\text{ref}}}) - (V_{ceo} + V_{do})\text{Sign}(i_a) - (r_{ce} + r_d)i_a  
\]  

(19)

Now for phase \(b\) and \(c\):

\[
V_b = \left[ \frac{T^*_b + T_{mb}\text{Sign}(i_b)}{T_s} \right] \left( \frac{1}{2}V_{dc} + V_d - V_{ce} \right) \text{Sign}(U_{b_{\text{ref}}}) - (V_{ceo} + V_{do})\text{Sign}(i_b) - (r_{ce} + r_d)i_b  
\]  

(20)
\[ V_c = \left[ \frac{T_c + T_m \text{Sign}(i_a)}{T_s} \right] \left( \frac{1}{2} V_{dc} + V_d - V_{ce} \right) \text{Sign}(U_{c,ref}) - (V_{co} + V_{do}) \text{Sign}(i_c) - (r_{ce} + r_d)i_c \]  

Balanced load for three-phase loads is indicated as:

\[ V_a + V_b + V_c = 0 \]  

\[ i_a + i_b + i_c = 0 \]  

\[ \begin{cases} 
V_a = V_{ao} + V_o \\
V_b = V_{bo} + V_o \\
V_c = V_{co} + V_o 
\end{cases} \]  

Hence, the schematic illustration of the PWM inverter shown in Figure 3 is thus transformed into the final DTC model schematically represented in Figure 8.

**Figure 8.** Three-phase SPWM inverter with the proposed DTC method.

Subsequently, the control block of the upper section \((-\left(\frac{1}{2}\right)\text{sign}(i_a))\) is canceled out with a feedback block \((g(i_a) = \left(\frac{1}{2}\right)\text{sign}(i_a))a\). The Feed-forward \(f(\hat{e})\) method is employed for dealing with hysteresis. The hysteresis compensation block as given in Figure 7 is utilized. To achieve the characteristics of an ideal relay, transfer features such as \(m\), \(V_a\) are used. Figure 7 also gives a representation of the dead time feedback blocks \(g(i_a)\), and feed-forward block \(f(\hat{e})\) of the SPWM inverter model. Owing to the inherent phase lag the feed-forward compensation cannot be ignored. At this stage, the DTC technique can be applied to the 3-phase PWM inverter, an example of which has been demonstrated in Figure 3.

The compensation of dead time blocks \(g(i_a)\) (feedback) and \(f(e)\) (feedforward) of the 3 phase SPWM inverter model is presented in Figure 7 schematically. Due to an inherent phase lag, the \(f(\hat{e})\) (feed-forward compensation) cannot be ignored. Just now at this stage, the DTC technique is ready to be applied on 3-phase PWM inverter for practical implementation which is presented in Figure 3.

Furthermore, before the dead time compensation method the equation has the following shape:

\[ e = [V_i(t)] - V_c(t) \]  

After converting the deviation, \(e\), to phase voltage, \(V_a\); adjusting \(T_d\) and \(\epsilon\) equal to zero; eliminating the factor \(-\left(\frac{1}{2}\right)\text{sign}(i_a)\) through feedback factor \(g(i_a) = \left(\frac{1}{2}\right)\text{sign}(i_a)\) application; and applying for the compensation through feedforward for dealing with the inherent phase angle.

It is pertinent that the voltage control signal \(V_i(t)\) in (25) is equal to \([V_i(t) - f(\hat{e}) + g(i_a)]\) and Equation (25) becomes:

\[ e = [V_i(t) - f(\hat{e}) + g(i_a)] - V_c(t) \]  

where \(\hat{e} = V_i - V_c\) and \(f(e)\) and \(g(i_a)\) are nonlinear functions.
4. Results and Discussion

Following the mathematical modeling, the proposed dead-time compensation model was simulated using MATLAB/Simulink for validation of the method. The $V/f$ strategy was employed for system control. Since the compensation strategy only depends on the characteristics of the power devices, a three-phase Y-connected symmetrical RL load was deployed at the output terminal of the inverter. The key parameters used in the simulation are listed in Table 2 while the important characteristics of the industrial motor are given in Table 3. The simulation time is kept twice the fundamental period to avoid imprecise results and surplus data; otherwise, the simulation may stop due to computer memory exhaustion.

| No | Parameters                  | Input Values |
|----|----------------------------|--------------|
| 1  | Reference Signal $f_r$     | 50 Hz        |
| 2  | Carrier Signal $f_c$       | 5 kHz        |
| 3  | Amplitude modulation Index | 0.8          |
| 4  | DC Voltage                | 700 V        |
| 5  | Time Delay $T_d$           | 10 $\mu$s    |
| 6  | $V_c$                     | 1            |
| 7  | $V_r$                     | 0.8          |
| 8  | Load Resistance           | 12.6 $\Omega$|
| 9  | Load inductor             | 40 mH        |

| No | Parameters                  | Rating       |
|----|----------------------------|--------------|
| 1  | Nominal power of IM         | 5.4 HP       |
| 2  | The nominal voltage of induction motor | 400 V |
| 3  | Nominal frequency of induction motor | 50 Hz |
| 4  | Speed                      | 1430 rpm     |
| 5  | Power factor               | 0.8          |
| 6  | Rated torque               | 10 Nm        |

Dead-time distortion correction algorithms are a useful tool for adjusting PWM relevant to the actual polarity of phase current. The PWM control signal is extended by the addition of dead time, to match the actual pulse with the desired values, when the voltage pulse is shortened. Contrarily, for prolonged voltage pulse by dead time, the PWM signal is reduced by an equivalent time, leading to a match between the actual and desired voltage pulse. Resultantly an actual voltage signal equal to the desired signal is achieved, along with a sinusoidal phase current.

4.1. Impact of Dead Time on Load Current Waveform

Without the dead time compensation and the proposed dead time compensation method, when the fundamental frequency $f_1$ is 5 Hz, the load current waveform is substantially improved. The amplitude of the current waveform is increased and distortion is reduced significantly. The current waveform is almost the same as the ideal current waveform. The provision for the mandatory delay in switching signals in IGBTs to accommodate dead time can induce undesirable sub-harmonics, subsequently causing deviation in load current as illustrated in Figure 9. The proposed DTC compensates the distortions to make the signal more sinusoidal as shown in Figure 10.
Table 3. Characteristics of induction motor (industrial load).

| No. | Parameters                              | Value           |
|-----|-----------------------------------------|-----------------|
| 1   | Nominal power of IM                     | 5.4 HP          |
| 2   | The nominal voltage of induction motor  | 400 V           |
| 3   | Nominal frequency of induction motor    | 50 Hz           |
| 4   | Speed                                    | 1430 rpm        |
| 5   | Power factor                             | 0.8             |
| 6   | Rated torque                             | 10 Nm           |

4.1. Impact of Dead Time on Load Current Waveform

Without the dead time compensation and the proposed dead time compensation method, when the fundamental frequency $f_1$ is 5 Hz, the load current waveform is substantially improved. The amplitude of the current waveform is increased and distortion is reduced significantly. The current waveform is almost the same as the ideal current waveform. The provision for the mandatory delay in switching signals in IGBTs to accommodate dead time can induce undesirable sub-harmonics, subsequently causing deviation in load current as illustrated in Figure 9. The proposed DTC compensates the distortions to make the signal more sinusoidal as shown in Figure 10.

Figure 9. Load current with/without DTC (a) phase 1 (b) phase 2 (c) phase 3.

4.2. Total Harmonics and Individual Harmonics Distortions Calculation by FFT Analysis

The third harmonic distortion is the main problem due to the non-ideal characteristics of power converters. By nature, each regularly distorted waveform may be defined as a number of pure sine waves in which the frequency of each sinusoid is an integer multiple of the fundamental frequency of the distorted wave. The sum of the sinusoids is referred to as the "Fourier series." In recent years, they have also concentrated on the harmonic distortion of the power field.

Dead-time is unavoidable in inverter circuitry as it prevents short-circuiting. However, it comes with the side effect of total harmonic distortion, thus necessitating DTC. The proposed DTC can alleviate the side effects. As can be seen from Figure 10, the third harmonic distortion is 16.26% without DTC. However, after the application of the novel DTC, the distortion is mitigated by 3.77% to 12.49%, as presented in Table 4. This improvement of almost 4% will be instrumental for the health of the motors operating in industrial load.
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| Table 4. FFT analysis of the load current. |
|-----------------|-----------------|
|                 | Without DTC     | With DTC 10 µs |
| Fundamental Frequency (50 Hz) | 7.437           | 6.784         |
| Total harmonics distortion THD (%) | 16.26%        | 12.49%        |

Individual harmonic distortion (IHD) represents the relation between the root mean square (RMS) value of the fundamental (RMS) value of the individual harmonics in Equation (29) [28]:

\[ IHD_n = I_n / I_1 \] (29)

For third harmonic, \( n \) is represented by 3. From Figure 10, the RMS of the fundamental current is equal to 100. Also, the RMS of the third harmonic current without DTC is 11.615 A and with DTC is 7.475 A. Therefore, \( IHD_3 = 11.615 / 100 \times 100 = 11.615 \) without DTC and \( IHD_3 = 7.475 \) with DTC.

4.3. Improvement in Fundamental Voltage Magnitude and Phase Angle

Dead-time induces certain drawbacks in the power electronic circuitry such as a decrease in fundamental voltage and distortion of other parameters. These effects can be effectively coped with through the incorporation of the proposed DTC. The fundamental voltage magnitude can be restored, and the harmonics minimized. Figure 11a for dead time 10 µs presents the fundamental voltage
magnitude in the absence of DTC and presents the same parameter after DTC, respectively. It is evident that the fundamental voltage has significantly improved as a result of the application of the proposed DTC technique.

\[
\begin{align*}
\text{Without DTC} & \quad \text{With DTC 10\mu s} \\
\text{Fundamental Voltage Magnitude} & \\
\text{Phase Angle} & \\
\end{align*}
\]

Figure 11. Without/with 10 \mu s DTC (a) fundamental voltage \(V_a\) magnitude (b) fundamental voltage \(V_a\) phase angle.

Phase angle distortion is also a downside of dead time. However, an efficient DTC strategy can handle this drawback to a certain degree. The proposed DTC model can achieve significant improvements in this domain as well. Figure 11b for dead time 10 \mu s shows the phase angles distortion pre and posts using the DTC technique respectively. It is vividly evident from these figures that the phase angle distortion has been significantly reduced through the application of the proposed DTC technique.

4.4. Improvement in Power Quality Parameters of Induction Motor

The induction motors are major energy-using equipment, any issues with their smooth operation are extremely significant. The unavoidable delay in signal switching can cause sub-harmonics leading to waveform distortion in the current signal. Additionally, it can also lead to pulsation in torque, and reduction in the rotational speed of the motor, manifesting in heat dissipation from the motors. These distortions and the concomitant damages can be significantly reduced by employing an efficient DTC technique. The DTC technique can restore the current to one looking more like the sinusoidal curve which entails the remedy of the aforementioned drawbacks in motor performance. DTC insertion in the inverter circuitry has been shown to mitigate the harmonic distortion and load torque pulsation. Furthermore, DTC can lead to practical improvements in motor performance such as smooth operation, limited torque ripples, low noise, and enhance efficiency in operation due to lower harmonic losses.

The proposed DTC technique has been applied to the inverter circuit with the harmonic distortion mentioned above. Figure 12a–c show the improvement in the current waveform distortion, motor speed, and torque pulsation respectively. In Figure 12a–c, using DTC application shows better performance in comparison with using DTC application for the motor speed and the torque pulsation, respectively. The left side of these figures represents these parameters before the application of DTC, while the right sides represent the post DTC parameters’ behavior.
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Figure 12. Without/with 10 𝜇s DTC (a) induction motor current (b) speed of induction motor (c) Torque pulsation.

4.5. Case 2: Dead-Time 1 𝜇sec and Switching Frequency 1 kHz

In case 2, the studies show that the current magnitude of the harmonics is the same, while the distortion factors are different due to time increasing as shown in Figure 13. If we take 1 micro-second, as shown in Figure 13, the third harmonic distortion without DTC is 16.26 percent. Moreover, after the implementation of the proposed DTC, method the distortion is reduced from 18.36% to 10.20%, as seen in Table 5. For the quality of power in industrial loads, an average increase of almost 8% is important.
Def. 12. Calculation of total harmonic distortion (THD) without and with DTC. 

Table 5. FFT analysis of the load current.

|                           | Without DTC | With DTC 1 µs |
|---------------------------|-------------|---------------|
| Fundamental Frequency (50 Hz) | 8.227       | 6.714         |
| Total harmonics distortion THD (%) | 19.20%     | 16.16%        |

From Figure 13, the RMS of the fundamental current is equal to 100. Also, the RMS of the third harmonic current without DTC is 15.707 A and with DTC is 10.295 A. Therefore, $I_{HD3} = 29.2759/100 = 29.2759\%$ without DTC and $I_{HD3} = 14.645\%$ with DTC.

Similarly, the fundamental voltage magnitude may be recovered in case 2 and the harmonics reduced as shown in Figure 14a. Figure 14a explicitly indicates the voltage magnitude in the presence of the DTC and also displays the same parameter before the DTC when time is 1 microsecond. It is clear that the voltage magnitude has dramatically changed as a result of the implementation of the new DTC methodology.

In fact, the distortion of the phase angle in case 2 is also increased due to dead-time effects. However, if we take 1 micro-second, an effective DTC strategy will deal with this problem to some large extent. Figure 14b demonstrates the before and after the distorted phase angles of voltage magnitude.
by using the DTC methodology, respectively. It is clear from this figure that the distortion of the phase angle was greatly decreased by the implementation of the new DTC strategy.

In case 2 while the dead time is changed from 10 to 1 micro-seconds, the DTC incorporation in the inverter circuit is shown to reduce the total harmonic distortions and also torque pulsation as shown in Figure 15a. In addition, DTC will lead to realistic changes in an induction motor performance, along with the smooth operation, low noise, minimal torque ripples, and increased operating efficiency due to the lower harmonic losses. Figure 15a–c demonstrate the increase in current waveform quality, induction motor speed, and also torque pulsation, collectively.

**Figure 15.** Without/with 1 µs DTC (a) induction motor current (b) speed of induction motor (c) Torque pulsation.
5. Conclusions

The research endeavor successfully models and implements a novel dead time technique rooted in dead time compensation for enhancing the power quality parameters. The overall efficiency improvement of power converters has been achieved from cumulative improvements in several power quality parameters such as sinusoidal load current, phase angle, fundamental voltage magnitude, harmonic distortion. Further, the mitigation in a motor operation like torque pulsation smoothening, current waveform restoration, and speed enhancement are also enhanced. The parametric equations for all the parameters are derived for normal scenarios and dead time compensation scenarios. The model is simulated in MATLAB with two different cases and the results, with and without the proposed model application, are drawn. Finally, two separate case studies of the performance relative to the pre-model and major changes in all dimensions of the power quality parameters and the output of the power converters deficiency are found by the implementation of the dead time compensation technique. The proposed DTC results in significant improvement in the following parameters as exhibited in Figures 9–15:

(a) Sinusoidal load current waveform has been achieved by applying dead time compensation, leading to the removal of distortions accruing from harmonics
(b) Fundamental voltage magnitude has been significantly restored through the proposed DTC implementation.
(c) The phase angle has been improved through the proposed DTC strategy. Additionally, the third harmonic distortion has been significantly alleviated 3.77%, through the proposed DTC strategy in Case 1 and 3.04% in Case 2.
(d) Significant improvements have been achieved in the induction motor parameters post the DTC strategy application. Parameters like torque pulsation, speed, and THD which cause hindrance in smooth motor operation have been demonstrably improved through the novel technique.

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