Article

Reference-Free Dynamic Voltage Scaler Based on Swapping Switched-Capacitors

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Abstract: This paper introduces a reference-free, scalable, and energy-efficient dynamic voltage scaler (DVS) that can be reconfigured for multiple outputs. The proposed DVS employs a novel swapping switched-capacitor (SSC) technique, which can generate target output voltages with higher resolution and smaller ripple voltages than the conventional voltage scalers based on switched-capacitors. The proposed DVS consists of a cascaded 2:1 converter based on swapping capacitors, which is essential to achieve both very small voltage ripple and fine-grain conversion ratios. One of the serious drawbacks of the conventional voltage scalers is the need for external reference voltages to maintain the target output voltage. The proposed SSC, however, eliminates the needs for any reference voltages. This significant benefit is achieved by the self-charging ability of the SSC, which can recharge all its capacitors to the configured voltage by simply swapping the two capacitors in each stage. The proposed SSC-DVS was designed with a resolution of 16 output levels and implemented using a 130 nm CMOS (Complementary Metal Oxide semiconductor) process. We conducted measured results and post-layout simulations with an input voltage of 1.5 V to produce an output voltage range of 0.085–1.4 V, which demonstrated a power efficiency of 85% for a load current of 550 μA with a voltage ripple of as low as 2.656 mV for a 2 kΩ resistor load.

Keywords: switched-capacitor; voltage converter; dynamic voltage scaler; high energy efficiency; swapping capacitor

1. Introduction

Voltage converters are essential building blocks for many low power devices, such as biomedical devices, mobile phones, wireless sensor networks, energy harvesting devices, and internet-of-things (IoT) devices [1–6].

Nowadays, switched-capacitor voltage converters are the most popular architectures due to their process compatibility, high efficiency, and small area when integrated on-chip. Although inductor-based DC-DC converters have been commonly used in classical applications, they almost always require off-chip inductors, which makes them unsuitable for on-chip voltage scalers supplying multiple power domains. Implementing on-chip inductors incurs excessive chip areas for present process technologies. It also requires a special process to achieve an on-chip inductor with a high-quality factor, which increases both the complexity and the cost.

C. Huang et al. [7] demonstrated effective methods that can improve the quality factor of the inductor based on a packaged bond-wire-based inductive converter. This approach, however, requires special bonding wires that makes its fabrication impractical. On the other hand, conventional voltage converters based on switched-capacitors offer energy efficiency with only limited switching frequency and specific output voltages. Operating such voltage converters in non-optimal conditions often
result in significant degradation in their energy efficiency. Moreover, to add more conversion ratios to switched-capacitor (SC) voltage converters, like a series-parallel SC converter, often increases the design complexity and the area of capacitor array while degrading the efficiency [8–13].

Loai G. Salem et al. [14] presented a voltage converter based on recursive switched-capacitor topology. It achieves $2^n$ conversion ratios with a peak efficiency of 85.8%. This architecture; however, requires an excessive number of switches. In addition, the number of control signals increases, thus the complexity of the controller increases as well. Moreover, it needs extra bias voltage and a reference voltage, which requires additional circuits. Moreover, the reported architecture does not offer the scalability, which is important for DVS. In other words, if we need to change the target voltage or increase the number of voltage levels, we must redesign the whole circuit.

Switched-capacitor down-converters and up-converters based on the self-oscillation technique have been reported by [4,15,16]. To generate just one conversion ratio of 1:2 or 2:1, they implement an odd number of stages, usually more than three stages, with a delay circuit added between every two stages. Therefore, they require a large number of switches; in addition, they add two capacitors for each stage, leading to an area increment. They also do not offer the reconfigurability, which is required for DVS. Suyoung Bang et al. [9] reported a voltage converter based on the SAR (Successive Approximation Switched-capacitor) structure. It provides $2^n$ ratios with a peak efficiency of 72%. This architecture; however, suffers from the cascaded losses, in which some stages take the charges only from the previous stage, not from the supply voltage, so such losses are unavoidable in this architecture. It also requires a comparator and a reference voltage generator. To provide the reference voltage; thus, they implemented a voltage regulator based on $2^n$ diodes formed by connecting PFETs (P-channel Field Effect Transistors) in series. This makes the voltage regulator become excessively complex as N increases, in addition to the growing overhead of the configuration switches.

A soft-charging SC voltage converter is presented in [17]. It employs stage out-phasing and multi-phase soft-charging approaches. They can reduce the energy loss caused by charge-sharing, provide better capacitance utilization, and higher efficiency. It; however, divides each stage into m sub-stages with extra phase control signals. This leads to excessive design complexity and poor energy efficiency for a large number of sub-stages.

To resolve the problems of the previous converters discussed above, this paper presents a dynamic voltage scaler (DVS) based on cascaded, swapping switched-capacitors (SSCs). It provides high-resolution outputs, high power efficiency, and low voltage ripples. It also allows a wide-range input voltage, while concurrently producing multiple outputs with fine-grain steps. The proposed architecture provides a wide-range of conversion ratios (CRs). For an SSC with n stages, it produces $2^n$ steps with a voltage resolution of $V_{in}/2^n$. The essential component of the proposed DVS is the swapping capacitor stage with a 2:1 voltage ratio. It maintains the output voltage by periodically swapping the upper and bottom capacitors in each stage, which ensures that the bottom capacitor is always charged to the target voltage.

This paper is organized as follows: Section 2 presents the architecture of the proposed DVS based on cascaded SSCs. Section 3 provides analytic models of the output voltage, current flow, and steady-state energy efficiency of the proposed SSC-DVS. Section 4 demonstrates the simulation experiment results of the proposed circuit. Finally, Section 5 highlights the key contributions of this work.

### 2. The Architecture of the Swapping Switched-Capacitor-Based DVS

#### 2.1. Circuit Operation

Figure 1 shows the structure of each stage of the proposed SSC. It consists of two equal-sized capacitors and eight switches. The capacitors work as a voltage divider to generate the average of the two inputs, while the switches are used to swap the two capacitors’ positions. By swapping the
capacitors faster than the changes in their voltage, the capacitors can maintain the output voltage of each stage. The unit cell of Figure 1 operates as follows:

1. Two inputs $V_1$ and $V_2$ are applied to the SSC-DVS input ports to generate the average value $V_{\text{out}} = \frac{V_1 + V_2}{2}$.
2. In phase 1, the bottom capacitor, $C_B$, delivers the charges to the load circuit, and thus the amount of $C_B$’s charge decreases. Therefore, the voltage across $C_B$ decreases while the voltage across $C_T$ increases over time. When at the middle of switching time $\left( \frac{T_S}{2} \right)$, the controller switches to phase 2.
3. In phase 2, the controller reconfigures the cell by swapping $C_B$ and $C_T$. Then $C_B$’s positive terminal is connected to $V_1$, while its negative terminal is connected to $V_{\text{out}}$, as illustrated by Figure 1c. On the other hand, $C_T$’s positive terminal is connected to $V_{\text{out}}$ while its negative terminal is connected to $V_2$, as illustrated by Figure 1c.
4. In phase 2, $C_T$ supplies the load.
5. When $T_S$, the controller switches back to phase 1, and the above steps are repeated.

Figure 1. The basic unit cell of the proposed SSC (Swapping Switched-capacitor): (a) Schematic of the unit cell; (b) phase 1; and (c) phase 2.

2.2. SSC-DVS Architecture

Figure 2 shows the architecture of an n-bit SSC-DVS which generates $2^n$ levels of output voltages. Figure 3 illustrates the detailed circuit schematic of the n-bit SSC-DVS.

Figure 2. Block diagram of the proposed n-bit SSC-DVS (Dynamic Voltage Scaler) architecture.
poly–insulator–poly (PIP) or metal–oxide–metal (MOM) structures, in contrast, exhibit more parasitic energies, generating conversion ratios of $\frac{1}{12}$.

The aspect ratio of the body switch transistors was used to reduce leakage current using the body switching technique [20,21]. The aspect ratio of the body switches can be implemented using the transmission gate consisting of NMOS (N-type Metal Oxide Semiconductor) and PMOS (P-type Metal Oxide Semiconductor) devices, and their body switches. The body switches can generate the maximum target output current, while the aspect ratio of the body switch transistors were $\left(\frac{W}{L}\right)_{p1} = \left(\frac{W}{L}\right)_{p2} = \frac{0.15 \, \mu m}{0.13 \, \mu m}$.

To quantify the proposed SSC-DVS, we applied $D_1D_2 = (00)2$ to generate conversion ratios of $\frac{1}{2}$ and $\frac{1}{4}$. This was achieved by using the body switching technique [20,21]. The aspect ratio of the transmission-gate transistors were $\left(\frac{W}{L}\right)_n = \left(\frac{W}{L}\right)_p = \frac{20 \, \mu m}{0.13 \, \mu m}$, which were selected based on the maximum target output current, while the aspect ratio of the body switch transistors were $\left(\frac{W}{L}\right)_p = \left(\frac{W}{L}\right)_n = \frac{0.15 \, \mu m}{0.13 \, \mu m}$.

In the second configuration of Figure 7, we applied $D_1D_2 = (01)2$ to generate conversion ratios of $\frac{1}{2}$ and $\frac{3}{4}$. Figure 7 shows phases $\varphi_1$ and $\varphi_2$ to configure the switches of the swapping process to generate conversion ratios of $\frac{1}{2}$ and $\frac{3}{4}$. We connected inputs $V_1$ and $V_2$ of the first stage to $V_{in}$ and $GND$, respectively, leading to $V_{out1} = \frac{V_{in} + GND}{2} = \frac{1}{2} V_{in}$. Then, inputs $V_1$ and $V_2$ of the second stage were connect to $V_{out1}$ and $GND$, respectively, producing $V_{out2} = \frac{V_{out1} + GND}{2} = \frac{0.5V_{in} + GND}{2} = \frac{1}{4} V_{in}$. Figure 6a,b show $\varphi_1$ and $\varphi_2$ phases, used to configure the switches of the swapping process to generate conversion ratios of $\frac{1}{2}$ and $\frac{3}{4}$. We connected inputs $V_1$ and $V_2$ of the first stage to $V_{in}$ and $GND$, respectively, leading to $V_{out1} = \frac{V_{in} + GND}{2} = \frac{1}{2} V_{in}$. Then, inputs $V_1$ and $V_2$ of the second stage were connect to $V_{out1}$ and $GND$, respectively, producing $V_{out2} = \frac{V_{out1} + GND}{2} = \frac{0.5V_{in} + GND}{2} = \frac{1}{4} V_{in}$. Figure 6a,b show $\varphi_1$ and $\varphi_2$ phases, used to configure the switches of the swapping process to generate conversion ratios of $\frac{1}{2}$ and $\frac{3}{4}$.
GND, respectively, resulting in $V_{out1} = \frac{V_{in} + GND}{2} = \frac{1}{2}V_{in}$. Then inputs $V_1$ and $V_2$ of the second stage were connected to $V_{out1}$ and $V_{in}$, respectively, giving $V_{out2} = \frac{V_{out1} + GND}{2} = \frac{0.5V_{in} + V_{in}}{2} = \frac{3}{4}V_{in}$. With $V_{in}$ of 1.5 V, hence, the above SSC-DVS could generate 375 and 750 mV when $D_1D_2 = (010)_2$, while producing 750 and 1.125 mV when $D_1D_2 = (01)_2$.

![Figure 5](image)  
Figure 5. A 2-bit example of the proposed SSC-DVS architecture with two configurations of: (a) $D_1D_2 = (00)_2$; and (b) $D_1D_2 = (01)_2$.

![Figure 6](image)  
Figure 6. A small example of 2-bit SSC-DVS architecture with conversion ratios of $\frac{1}{2}$ and $\frac{1}{4}$: (a) Phase 1 ($\phi_1$); and (b) phase 2 ($\phi_2$).

![Figure 7](image)  
Figure 7. A small example of 2-bit SSC-DVS architecture with conversion ratios of $\frac{1}{2}$ and $\frac{1}{4}$: (a) Phase 1 ($\phi_1$); and (b) phase 2 ($\phi_2$).
3. Analytic Model

This section provides steady-state analysis for target output voltages of the proposed SSC-DVS. It also derives the current model of the proposed architecture while calculating its energy efficiency.

3.1. Steady-State Output Voltage

The output of the proposed SSC-DVS was connected in parallel with an output capacitor to reduce the voltage ripple. Table 1 shows the simulation results of the effect of the output capacitor size on the voltage ripple. Here, \( V_{\text{Ripple}} \) corresponded to \( V_{\text{outn}} \) where \( 1 < n < 4 \). The voltage ripple was measured for all the four outputs of 4-bit SSC-DVS. For example, Table 1 shows that the voltage ripple gave a maximum value of 2.16 mV for \( C_L \) of 500 pF, whereas it gave a minimum value of 0.199 mV for \( C_L \) of 4 nF.

| \( C_L \) (nF) | \( V_{\text{Ripple1}} \) (mV) | \( V_{\text{Ripple2}} \) (mV) | \( V_{\text{Ripple3}} \) (mV) | \( V_{\text{Ripple4}} \) (mV) |
|-------------|-------------|-------------|-------------|-------------|
| 0.5         | 2.16        | 1.72        | 1.67        | 1.72        |
| 1           | 1.1         | 0.854       | 0.849       | 0.955       |
| 1.5         | 0.74        | 0.568       | 0.567       | 0.575       |
| 2           | 0.556       | 0.424       | 0.425       | 0.43        |
| 2.5         | 0.44        | 0.335       | 0.338       | 0.337       |
| 3           | 0.363       | 0.28        | 0.283       | 0.288       |
| 3.5         | 0.317       | 0.237       | 0.242       | 0.245       |
| 4           | 0.275       | 0.21        | 0.199       | 0.212       |

In phase 1 (\( \varphi_1 \)), the bottom flying capacitor \( C_B \) delivered the charges to both the output capacitor and the load resistor. The \( n \)-bit SSC-DVS provided \( n \) output voltages. Each output voltage could be described by Equation (1). The conversion ratio (CR) of \( K \) output voltage could be expressed by Equation (4).

\[
\begin{bmatrix}
V_{\text{out1}} \\
V_{\text{out2}} \\
V_{\text{out3}} \\
\vdots \\
V_{\text{outn}}
\end{bmatrix} =
\begin{bmatrix}
0 & \cdots & 0 & 0 & (1 + D_1) \\
0 & \cdots & 0 & (1 + D_1) & D_2 \\
\vdots & \cdots & (1 + D_1) & D_2 & D_3 \\
\vdots & \vdots & \vdots & \vdots & \vdots \\
(1 + D_1) & \cdots & D_{n-2} & D_{n-1} & D_n
\end{bmatrix}
\times
\begin{bmatrix}
\frac{1}{2^4} V_{\text{in}} \\
\vdots \\
\frac{1}{2^{n-1}} V_{\text{in}} \\
\frac{1}{2^n} V_{\text{in}}
\end{bmatrix}
\]

(1)

\[V_{\text{out}} = CR \times V_{\text{in}}\]  

(2)

\[\text{Resolution} = V_{\text{in}} \frac{2^n}{2^k}\]  

(3)

\[CR = \text{Resolution} \times (1 + B_{\text{code}K})\]  

(4)

Here, \( V_{\text{outn}} \) is the output voltage of the \( n \) stage, \( D_n \) is the digital configuration bit of \( n \) stage to select the top voltage \( V_1 \) or bottom voltage \( V_2 \). \( B_{\text{code}K} \) is the binary code (decimal value) which consists of \( K \) digital bits \( D_1, D_2 \cdots D_K \) (\( D_1 \) is the MSB (Most Significant Bit)), and \( K \) is the number of stages in the range of \( 1 \leq K \leq n \). The following examples explain the voltage equations. A 6-bit SSC-DVS with 1.5 V input voltage generated \( 2^6 = 64 \) voltage levels with a voltage step of \( \frac{1.5}{2^6} \approx 23.44 \) mV, while it generated multiple outputs up to 6 outputs simultaneously. Figure 8 shows a 6-bit SSC-DVS example with two different configurations \( B_{\text{code}} = (010110)_2 \) and \( B_{\text{code}} = (001100)_2 \). Table 2 shows the conversion ratios for the generated output voltage levels. In Figure 8, the top port of the first stage was connected to the \( V_{\text{in}} \), while the bottom port was connected to GND with “0”. Hence, the \( V_{\text{out1}} \) equals the average of the two inputs of the first stage leading to \( V_{\text{out1}} = \frac{V_{\text{in}} + \text{GND}}{2} = \frac{1.5 + 0}{2} = 0.75 \) mV. Then, \( V_{\text{out1}} \) was supplied to the top port of the second stage, while the bottom port was connected to \( V_{\text{in}} \) due to the second bit “1”.

in $B_{\text{code}} = (010110)_2$. Hence, $V_{\text{out}2} = \frac{V_{\text{in}} + V_{\text{out}1}}{2} = \frac{1.5 + 0.75}{2} = 1.125$ V. In this way, the steady-state output voltage of each stage could be determined by selecting a configuration code.

**Table 2.** Two different configuration codes with conversion ratios and generated output voltages.

| $B_{\text{code}} = (010110)_2$ | $B_{\text{code}} = (001100)_2$ |
|---------------------------------|---------------------------------|
| $V_{\text{out}k}$ | $\text{CR}$ | Value (V) | $V_{\text{out}k}$ | $\text{CR}$ | Value (V) |
| $V_{\text{out}1}$ | $\frac{1}{2}$ | 0.75 | $V_{\text{out}1}$ | $\frac{1}{2}$ | 0.75 |
| $V_{\text{out}2}$ | $\frac{3}{4}$ | 1.125 | $V_{\text{out}2}$ | $\frac{3}{4}$ | 0.375 |
| $V_{\text{out}3}$ | $\frac{5}{8}$ | 0.5625 | $V_{\text{out}3}$ | $\frac{5}{8}$ | 0.9375 |
| $V_{\text{out}4}$ | $\frac{13}{16}$ | 1.03125 | $V_{\text{out}4}$ | $\frac{13}{16}$ | 1.2187 |
| $V_{\text{out}5}$ | $\frac{27}{32}$ | 1.26562 | $V_{\text{out}5}$ | $\frac{27}{32}$ | 0.609 |
| $V_{\text{out}6}$ | $\frac{63}{64}$ | 0.6328 | $V_{\text{out}6}$ | $\frac{63}{64}$ | 0.304 |

### 3.2. Analysis of Steady-State Current Flows in Each Stage

This subsection analyzes the current flow of SSC-DVS in two cases: A single-output case and a multi-output case.

#### 3.2.1. Single Output Case

Figure 9 shows two configuration examples of a 6-bit SSC-DVS with a single-output based on two different configurations. Figure 9a, b show current paths of the SSC-DVS with $B_{\text{code}} = (010110)_2$ and $B_{\text{code}} = (001100)_2$, respectively. The conversion ratios for the two examples were $CR = \frac{27}{32}$ and $CR = \frac{13}{16}$, respectively. Equation (5) describes a generalized equation of the output current at the $n$-th output $V_{\text{out}n}$ for the proposed SSC-DVS architecture, illustrated by Figure 3.
Equation (5) describes the current \( I_{\text{out}_n} \) drawn from the input \( I_{\text{in}} \) and \( I_{\text{out}_n} \) is the output current of the \( n \)-th stage. For the example of Figure 9a, which has \( B_{\text{code}} = (010110) \), each output from stage 1 to stage 6, respectively, provided \( \frac{1}{64} I_{\text{out}_6}, \frac{1}{32} I_{\text{out}_6}, \frac{1}{16} I_{\text{out}_6}, \frac{1}{8} I_{\text{out}_6}, \frac{1}{4} I_{\text{out}_6}, \frac{1}{2} I_{\text{out}_6} \) and \( I_{\text{out}_6} \). Based on Equation (5), the total input current at the input port \( V_{\text{in}} \) was \( I_{\text{in}} = \frac{27}{64} I_{\text{out}_6} \). Here \( I_{\text{out}_6} \) was the output current at the final output \( V_{\text{out6}} \), as illustrated in Figure 9a. The current \( I_{\text{in}} \) drawn from the \( V_{\text{in}} \) source could be calculated as \( I_{\text{in}} = \left( \frac{1}{64} + \frac{1}{32} + \frac{1}{16} + \frac{1}{8} + \frac{1}{4} \right) I_{\text{out}_6} \) by Equation (5).

In the second example given in Figure 9b, the current for each SSC stage could be calculated in the same way as the first example using Equation (5). The total current at the input port \( V_{\text{in}} \) was \( I_{\text{in}} = \frac{13}{64} I_{\text{out}_6} \), which was calculated by Equation (5) as \( I_{\text{in}} = \left( \frac{1}{64} + \frac{1}{32} + \frac{1}{16} + \frac{1}{8} \right) I_{\text{out}_6} \).

3.2.2. Multi-Output Case

Figure 8 shows the current flows of the same 6-bit SSC-DVS, as the single-output case, above using the same configuration codes. It was; however, configured to generate multi-outputs simultaneously. Figure 8a,b show the current flows in each stage for codes \( B_{\text{code}} = (010110) \) and \( B_{\text{code}} = (001100) \), respectively.

Equation (7) represents the current \( I_{\text{in}_n} \) of the \( n \)-th stage in terms of its load current and the input current taken by its next stage, which was the \((n+1)\)th stage. The current \( I_{\text{in}} \) drawn from the input voltage source \( V_{\text{in}} \) could be expressed by Equation (8). It was expressed by the half of the sum of the individual current for the stages that were supplied by \( V_{\text{in}} \). Equation (9) describes the current \( I_{\text{in}} \) as a
function of the output current and the conversion ratio of each stage where CRₙ is the conversion ratio of the n-th stage. By substituting Equation (10) in Equation (9), the Iᵢᵣ could be expressed by Equation (11).

\[ Iₛₙ = Iₒᵤₙ + \frac{1}{2ⁿ(𝑛+1)} \times Iₛ(𝑛+1) \]  \hspace{1cm} (7)

\[ Iᵢᵣ = \frac{1}{2} (Iₛ₁(𝐷₁ + 1) + Iₛ₂𝐷₂ + \cdots + Iₛₙ𝐷ₙ) \]  \hspace{1cm} (8)

\[ Iᵢᵣ = C R₁ Iₒᵤ₃ + C R₂ Iₒᵤ₄ + \cdots + C Rₙ Iₒᵤₙ \]  \hspace{1cm} (9)

\[ Iₒᵤₙ = \frac{Vₒᵤₙ}{Rₙₖ} = C Rₙ \times \frac{Vᵢᵣ}{Rₙₖ} \]  \hspace{1cm} (10)

\[ Iᵢᵣ = Vᵢᵣ \times \left( \frac{C R₁²}{Rₖ₁} + \frac{C R₂²}{Rₖ₂} + \cdots + \frac{C Rₙ²}{Rₙₖ} \right) \]  \hspace{1cm} (11)

Equation (12) to Equation (17) describe the current that was provided from each stage for the example of Figure 8.

\[ Iₛ₁ = Iₒᵤ₃ + \frac{1}{2} Iₒᵤ₄ + \frac{1}{4} Iₒᵤ₅ + \frac{1}{8} Iₒᵤ₆ + \frac{1}{16} Iₒᵤ₇ + \frac{1}{32} Iₒᵤ₈ \]  \hspace{1cm} (12)

\[ Iₛ₂ = Iₒᵤ₄ + \frac{1}{2} Iₒᵤ₅ + \frac{1}{4} Iₒᵤ₆ + \frac{1}{8} Iₒᵤ₇ + \frac{1}{16} Iₒᵤ₈ \]  \hspace{1cm} (13)

\[ Iₛ₃ = Iₒᵤ₅ + \frac{1}{2} Iₒᵤ₆ + \frac{1}{4} Iₒᵤ₇ + \frac{1}{8} Iₒᵤ₈ \]  \hspace{1cm} (14)

\[ Iₛ₄ = Iₒᵤ₆ + \frac{1}{2} Iₒᵤ₇ + \frac{1}{4} Iₒᵤ₈ \]  \hspace{1cm} (15)

\[ Iₛ₅ = Iₒᵤ₇ + \frac{1}{2} Iₒᵤ₈ \]  \hspace{1cm} (16)

\[ Iₛ₆ = Iₒᵤ₈ \]  \hspace{1cm} (17)

In the 6-bit SSC-DVS example of Figure 8a, configured by B_code = (010110)₂, six output voltages were achieved simultaneously with conversion ratios of \( \frac{1}{2}, \frac{3}{4}, \frac{3}{8}, \frac{11}{16}, \frac{7}{8}, \) and \( \frac{7}{16} \), respectively. Each SSC stage provided an output current for its own load and for the next stage as well. By substituting these conversion ratios in Equation (10) with \( Vᵢᵣ = 1.5 \text{ V} \) and all load resistances with \( Rₖ₁ = Rₖ₂ = \cdots = Rₖ₆ = 2 \text{ KΩ} \), the estimated total input current drawn from \( Vᵢᵣ \) source was \( Iᵢᵣ \approx 1.736 \text{ mA} \).

In the example of Figure 8b, a code B_code = (001100)₂ was applied to produce six outputs with conversion ratios of \( \frac{1}{2}, \frac{3}{4}, \frac{5}{8}, \frac{13}{16}, \frac{13}{32}, \) and \( \frac{13}{64} \), respectively. By substituting these conversion ratios in Equation (10) with the same conditions as in the previous example, the total input current drawn by the source was calculated as \( Iᵢᵣ \approx 1.177 \text{ mA} \).

Figure 10 shows a comparison between error currents that came from each stage based on the simulation and calculation in the example of Figure 8a. Both the ideal and calculated currents were estimated using Equations (12)–(17). The ideal current employed these equations with the assumption of ideal \( Vₒᵤₙ \) (no-load was connected), while the simulated current employed \( Vₒᵤₙ \) obtained from simulations with load resistances of \( Rₖ₁ = Rₖ₂ = \cdots = Rₖ₆ = 10 \text{ KΩ} \). It showed a maximum error of 2.6% between the simulated and ideal, while it showed a maximum error of 1.8% between the calculated and ideal. Figure 10 validates the correctness of the equations by proving that the equations well match the simulation results of the current per stages.
where $C_{eq}$ is the equivalent capacitance of the flying capacitance $C_T$ and $C_B$, where $C_{eq} = C_T + C_B$. $R_P$ is the parasitic resistance. For simplicity, we assume that $R_P$ is negligible in the remaining analysis.

Figure 10. Comparison between simulated and calculated input currents errors per stage.

Figure 11 shows the error current of calculated and simulated input currents, which were drawn from $V_{in}$ for the example of Figure 8a when the load resistance was varied from 1 to 60 KΩ. The error current curve shows that the simulated and calculated currents matched well in general, with the largest difference of less than only 7.5%, which occurred when a heavy load was connected. Figure 11 shows that Equation (11) perfectly matched the simulation results when a light load was connected.

Figure 11. Input current error drawn by the source $V_{in}$ with varying $R_L$ load.

3.3. Efficiency Analysis

This subsection analyzes the energy efficiency of the proposed SSC-DVS architecture. We used the example of 1-bit SSC-DVS in Figure 1 again for simplicity. Figure 12 represents the charge transfer model for 1-bit SSC-DVS. Here, $C_{eq}$ is the equivalent capacitance of the flying capacitance $C_T$ and $C_B$, where $C_{eq} = C_T + C_B$. $R_P$ is the parasitic resistance. For simplicity, we assume that $R_P$ is negligible in the remaining analysis.
If the maximum voltage $V_{C_{\text{max}}}$ across $C_{\text{eq}}$ is larger than the minimum output voltage $V_{\text{outmin}}$, the charges in $C_{\text{eq}}$ gets shared with $C_L$ and also gets dissipated by $R_L$ until $C_L$ is fully charged and $I_{CL}$ becomes 0 A, as shown in Figure 13. Right after this process, capacitors $C_{\text{eq}}$ and $C_L$ transfer part of their energy to the load resistor $R_L$. Depending on the status of $C_L$, we analyze the energy efficiency in two phases: (1) charge distribution phase, and (2) delivery phase.

3.3.1. Charge Distribution Phase

Due to unbalanced initial voltages on $C_{\text{eq}}$ and $C_L$, when $V_{C_{\text{max}}} \geq V_{\text{outmin}}$, $C_{\text{eq}}$ delivers charges to $C_L$ and $R_L$ until $C_L$ is fully charged. By using the charge conservation principle, we can model the amount of charge delivered from $C_{\text{eq}}$ to $C_L$ and $R_L$ by Equation (18). Let $I_{RL}$ represent the total load current drawn by the load circuit. For the sake of simplicity of proving the concept, we assume in this paper that the load current is constant regardless of the load’s supply voltage changes. Hence, we can model the load circuit by a resistor $R_L$.

$$C_{\text{eq}}(V_{C_{\text{max}}} - V_{C_{\text{min}}}) = C_L(V_{\text{outmax}} - V_{\text{outmin}}) + I_{RL}T_{\text{CD}}$$  \hspace{1cm} (18)

Here, $V_{C_{\text{min}}}$ is the voltage of $C_{\text{eq}}$ after the charge distribution process, while $V_{\text{outmax}}$ is the voltage of $C_L$ after the charge distribution process. In addition, $T_{\text{CD}}$ is the time duration for the charge distribution process to reach the condition $V_{C_{\text{min}}} = V_{\text{outmin}}$. The maximum output voltage can be expressed by Equation (19). The average output current $I_{RL}$ can be calculated by Equation (20) under the assumption that $T_{\text{CD}}$ is much smaller than the time constant of the circuit.

$$V_{\text{outmax}} = \frac{C_{\text{eq}}V_{C_{\text{max}}} + (C_L - \frac{T_{\text{CD}}}{2R_L})V_{\text{outmin}}}{C_{\text{eq}} + C_L + \frac{T_{\text{CD}}}{2R_L}}$$  \hspace{1cm} (19)
\[ I_{RL} = \frac{V_{outmax} + V_{outmin}}{2} \times \frac{1}{R_L} \quad (20) \]

### 3.3.2. Delivery Phase

In the delivery phase, capacitors \( C_{eq} \) and \( C_L \) transfer part of their charges to the load resistor \( R_L \) in the remaining time of \( \left( \frac{T}{2} - T_{CD} \right) \), where \( \frac{T}{2} \) is half of the switching period. By applying the charge conservation principle, we can model the amount of charge delivered from \( C_{eq} \) and \( C_L \) to \( R_L \) by Equation (21), while we can calculate the final voltage across the \( C_{eq} \) and \( C_L \) by Equation (22), assuming that \( R_P \) is negligible like in subsection C.

\[ C_{eq}(V_{outmax} - V_{Cmin}) + C_L(V_{outmax} - V_{outmin}) = I_{RL} \left( \frac{T}{2} - T_{CD} \right) \quad (21) \]

\[ V_{outmin} = V_{outmax} \times \left( \frac{(C_{eq} + C_L)R_L - \left( \frac{T}{2} - T_{CD} \right)}{(C_{eq} + C_L)R_L + \left( \frac{T}{2} - T_{CD} \right)} \right) \quad (22) \]

### 3.3.3. Losses Analysis

In SC voltage converters there are two kinds of losses that are dependent or independent of the load current \( I_{RL} \). The losses that are dependent on the output current include SC loss and switch conduction loss. While the losses that are independent (current loss, \( I_{loss} \)) of the output current include the gate and bottom plate capacitor switching losses [22,23].

Figure 14 presents a model to calculate the total power loss in the proposed circuit. In Figure 14, the independent losses were modeled by a series resistance \( R_S \), while the independent losses were modeled by a shunt resistance \( R_{Sh} \). The total power losses in the proposed circuit can be expressed by Equation (23)

\[ P_{Loss} = P_{RS} + P_{Rsh} \quad (23) \]

\[ P_{RS} = (I_{RL})^2 \times R_S \quad (24) \]

\[ P_{Rsh} = (I_{loss})^2 \times R_{Sh} = \left( \frac{V_{target}}{R_L} - I_{RL} \right)^2 \times R_{Sh} \quad (25) \]

Figure 14. Simplified model for power loss calculations.

The equivalent series resistance could be calculated by Equation (26), which was derived based on Equations (6) and (7) in reference [22]. While the equivalent shunt resistance could be calculated by Equation (27), which was derived based on Equations (10) and (11) in [22].

\[ R_S = \frac{1}{M_{Cap}C_{eq}F_{sw}} + \frac{R_{on}M_{Sw}}{W_{Sw}} \quad (26) \]

\[ R_S = \frac{1}{M_{bott}C_{bott}F_{sw}} + \frac{1}{W_{Sw}C_{gate}F_{sw}} \quad (27) \]
Here, $M_{\text{Cap}}$ is a constant related to the converter’s output resistance and it determined based on the converter topology (e.g., for the SSC $M_{\text{Cap}} = 4$). $F_{\text{sw}}$ is the switching frequency, $R_{\text{on}}$ is the switch resistance density, which is measured in $\Omega \cdot \text{m}$, $W_{\text{Sw}}$ is the total width of all transistors, and $M_{\text{Sw}}$ is a constant which is determined by the converter’s topology (e.g., for the SSC $M_{\text{Sw}} = 16$). $M_{\text{bott}}$ is a constant related to the converter’s topology (e.g., for the SSC $M_{\text{bott}} = 2$), $C_{\text{bott}}$ is the bottom plate capacitance, and $C_{\text{gate}}$ is the gate capacitance density in F/m of the switches.

Based on Equations (19) and (22) we could calculate the average output voltage; thus, we could estimate the power that delivered to the load $P_{\text{out}}$. We could, also, calculate the power loss by the proposed SSC by using Equation (20) and Equations (23)–(27). Thus, we could calculate the efficiency by Equation (28) as well.

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}}$$ (28)

Table 3 shows the simulation and calculation results of the power efficiency for the 1-bit SSC-DVS example shown in Figure 1. Schematic-level circuit simulations were conducted with two different loads, of 2 and 10 KΩ. We measured the maximum voltage across $C_{eq}$ for both stages from simulation, then we calculated the average output voltage using Equations (19) and (22). Table 3 validates the accuracy of Equations (19), (22), and (28) in estimating the output voltage and efficiency. Table 3 shows that the results calculated by our analytical model (Equations (19)–(28)) closely matched the simulation results. The difference in the output voltage and efficiency, respectively, was less than 1 mV and less than 0.05%.

| Parameter      | $R_L = 10$ KΩ, $CR = \frac{1}{2}$ | $R_L = 2$ KΩ, $CR = \frac{1}{2}$ |
|----------------|----------------------------------|----------------------------------|
| $V_{\text{out}}$ (mV) | 745.66 745.7 | 728.88 728.95 |
| $I_{\text{out}}$ (µA) | 74.566 74.57 | 364.405 364.475 |
| $I_{\text{loss}}$ (µA) | 0.434 0.43 | 10.595 10.525 |
| $P_{\text{out}}$ (µW) | 55.609 55.6068 | 265.6337 265.684 |
| $P_{\text{loss}}$ (µW) | 0.649 0.646 | 15.616 15.565 |
| $\eta$ (%) | 98.8 98.85 | 94.447 94.465 |

4. Experimental Results

4.1. Experimental Environment

We have implemented a test chip of the proposed dynamic voltage scaler using a 130 nm CMOS process. The design, simulation, and implementation were carried out using the Spectre simulator tool of the Cadence Design Suite. Figure 15 shows the circuit schematic of the implemented 4-bit SSC-DVS that provides 16 voltage levels. We supplied $V_{\text{in}}$ of the SSC-DVS with 1.5 V, while connecting the output to a simple load circuit. The load circuit was modeled by a resistor, $R_L$, of 2 KΩ in parallel with a load capacitor, $C_L$, of 1 nF (twice the flying capacitors) to demonstrate the performance of the proposed voltage scaler. Figure 16a shows the layout design of the test chip, while Figure 16b shows the micro-photo of its fabricated silicon. Due to area limitation in the silicon, we implemented a small 4-bit SSC-DVS architecture with on-chip capacitors of a small size of 0.4 nF, with RC load of 1 nF and 2 KΩ.
4.2. Performance of the Proposed Swapping DVS

4.2.1. Target Output Voltage

Figure 17 shows the simulation result of the output voltage of the implemented 4-bit SSC-DVS. It shows accurate 16 output voltage levels based on the configuration code D1D2D3D4. It also compares the circuit simulation results with the post-layout simulation results. Figure 17 shows the two simulation results that demonstrate 16 voltage levels. The circuit simulation, highlighted by black color, produced \( V_{\text{out}} \) from 82.3 mV to 1.42 V with a resolution of 85 mV. On the other hand, the post-layout simulation, indicated by red color, generated \( V_{\text{out}} \) of 16 output voltage levels from 80.76 mV to 1.35 V with 80 mV resolution. The voltage step of the output for this example circuit could be calculated by Equation (3) as 93.75 mV. The difference in \( V_{\text{out}} \)'s step-size between the analysis result and the circuit schematic simulation was 11.23 mV, while the difference in \( V_{\text{out}} \)'s step-size between the analysis result and the post-layout simulation was 13.75 mV. These differences were attributed to the voltage drop across the switches and parasitic components.

Figure 18 illustrates the measured results of the proposed SSC-DVS. It shows accurate 16 output voltage levels from 45 mV to 1.424 V for \( V_{\text{out}4} \), while it shows accurate eight output voltage levels from 117 mV to 1.242 V for \( V_{\text{out}3} \).

Figure 19 shows the measured settling time of the SSC-DVS. It shows 900 nS when the target output voltage was reconfigured from 465 to 550 mV, with an input supply of 1.5 V when the load current was 275 \( \mu \)A. It shows, also, a very small overshooting voltage of 5 mV.
calculated by Equation (3) as 93.75 mV. The difference in voltage levels from 45 mV to 1.424 V for decreased when the capacitor size increased. It also shows that the voltage ripple further ranged from 1.5 to 4.5 mV. This small ripple voltage was obtained thanks to the highly-efficient recharging operation of the swapping capacitors. It can be observed that the voltage ripple further decreased when the capacitor size increased.

### 4.2.2. Voltage Ripples

shows negative and positive transitions of the output voltage when the current changed from 50 to 275 µA. It shows, also, a very small overshooting voltage of 5 mV.

output voltage was reconfigured from 465 to 550 mV, with an input supply of 1.5 V when the load changes. When the target output voltage was set to 1.031 V and the load current received a perturbation by digital control signals, we observed fluctuation of the output voltage. Figure 20 shows the post-layout simulation results of the load regulation when the load current was 275 µA. It shows, also, a very small overshooting voltage of 5 mV.

Figure 18 illustrates the measured results of the proposed SSC-DVS. It shows accurate 16 output voltage levels from 117 mV to 1.242 V for the voltage drop across the switches and parasitic components. These differences were attributed to the analysis result and the post-layout simulation was 13.75 mV. These differences were attributed to the proposed SSC-DVS.

Figure 19 shows the measured settling time of the SSC-DVS. It shows 900 nS when the target output voltage was set to 1.031 V and the load current received a perturbation by digital control signals, we observed fluctuation of the output voltage. Figure 20 shows the post-layout simulation results of the load regulation when the load current was 275 µA. It shows, also, a very small overshooting voltage of 5 mV.

Figure 18. The measured results of the output voltage levels and the ripple voltage of the proposed SSC-DVS.

Figure 19. The measured results of settling time of the proposed SSC-DVS architecture.
Figure 20 shows the post-layout simulation results of the load regulation when the load current changes. When the target output voltage was set to 1.031 V and the load current received a perturbation by digital control signals, we observed fluctuation of the output voltage. Figure 20 shows negative and positive transitions of the output voltage when the current changed from 50 to 495 $\mu$A and from 495 to 50 $\mu$A. The settling time for load regulation was 300 ns for the negative transition, while the settling time was 360 ns for the positive transition.

Figure 20. The post-layout simulation results of the load transient performance of the proposed SSC-DVS architecture.

### 4.2.2. Voltage Ripples

Figure 21 shows the post-layout simulation result of the output voltage ripple for the above SSC-DVS test chip, which was obtained with a wide range of capacitor size. It can be observed that the voltage ripple ranged from 1.5 to 4.5 mV. This small ripple voltage was obtained thanks to the highly-efficient recharging operation of the swapping capacitors. It also shows that the voltage ripple further decreased when the capacitor size increased.

Figure 21. The post-layout simulation results of the output voltage ripple of the proposed SSC-DVS versus the flying capacitor C when $V_{in} = 1.5$ V, $R_L = 2$ K$\Omega$, and $F_{SW} = 50$ MHz.

Figure 22 shows the post-layout simulation result of the voltage ripple along with a wide range load resistance $R_L$. It changed exponentially from 90 $\mu$V to 8.43 mV, a significantly smaller ripple voltage than previous designs reported in [9,13,15].
This small ripple voltage demonstrated that the proposed SSC-DVS was highly efficient in minimizing voltage ripple. The voltage ripple changed almost linearly from 0.15 to 1.1 mV.

Figure 22. The post-layout simulation results of the output voltage ripple of the proposed SSC-DVS versus the load resistance $R_L$ when $V_{in} = 1.5$ V, $F_{SW} = 50$ MHz, and $C = 50$ pF.

Figure 23 shows the post-layout simulation result of the voltage ripple along with varying switching frequency $F_{SW}$. It varied exponentially from 78.3 to 0.166 mV along with a frequency range from 1 MHz to 1 GHz. The larger ripple voltage at low frequency was attributed to the fact that the difference ($\Delta V = V_{CB} - V_{out}$) between the voltage across the bottom capacitors $C_{Bi}$ and the voltage across the load resistor increased as the frequency decreased. This increased voltage ripple led to a slight loss in efficiency.

Figure 24. The post-layout simulation result of the voltage ripple along with varying target output voltage $V_{out}$. In this simulation, we applied $V_{in} = 1.5$ V, $F_{SW} = 50$ MHz, $C = 50$ pF, and $R_L = 2 \, \text{K}\Omega$. The voltage ripple changed almost linearly from 0.15 to 1.1 mV.

Figure 18 shows that the measured output voltage ripple for the SSC-DVS test chip was 2.656 mV. This small ripple voltage demonstrated that the proposed SSC-DVS was highly efficient in minimizing voltage ripple.
4.2.3. Efficiency

Figure 25 shows the efficiency of the proposed SSC-DVS obtained by post-layout simulations with varying capacitor size C. Figure 25a shows that it provided very high efficiency for most of the capacitor size, while it loss the efficiency down to 80% for the capacitor size below 1 pF. In order to maintain high efficiency in the case of small capacitors, we could use a higher switching frequency.

Figure 26 presents the simulation results of the efficiency for varying the load resistance $R_L$. In Figure 26, the schematic simulations showed high efficiency from 90% to 95% for heavy load cases, with $R_L < 25$ KΩ. This efficiency was measured as 85% to 92% when tested with post-layout simulations. This difference between the schematic simulation and post-layout simulation was due to the parasitic capacitance and resistance considered in the post-layout simulation.

Figure 27 illustrates the circuit simulation and the post-layout simulation of the efficiency for varying switching frequency, $F_{SW}$. The circuit simulation shows the efficiency increased exponentially from 30% at $F_{SW} = 1$ MHz to 99% at $F_{SW} = 1$ GHz. For higher $F_{SW}$ values, the efficiency saturated at 99%. In other words, the difference between the output voltage and the voltage across the bottom capacitor $C_B$ was very small. In contrast, at a very low switching frequency below 1 MHz, it exhibited a poor efficiency of 30%. This was due to slow charging and discharging operations for the bottom capacitor $C_B$. We could keep the efficiency high by increasing the capacitor size, as shown in Figure 25b. On the other hand, in Figure 27, the post-layout simulation exhibited efficiency 10%–20% lower than the circuit simulation result for the frequency higher than 200 MHz. The lower efficiency could be explained by the fact that we used regular transistors, not radio frequency (RF) transistors for the test chip design, thus the post-layout simulation experienced higher parasitic values at high frequency.
Figure 26. The post-layout simulation of the efficiency of the proposed SSC-DVS architecture versus the load resistor $R_L$ when $V_{in} = 1.5$ V, $F_{SW} = 50$ MHz, $C = 50$ pF.

Figure 27 illustrates the circuit simulation and the post-layout simulation of the efficiency for the switching Frequency $F_{SW}$ when $V_{in} = 1.5$ V, $C = 50$ pF, $R_L = 2$ KΩ.

The efficiency saturated at $C = 50$ pF. It showed almost constant efficiency of 94% for the schematic simulation, while it showed 91% efficiency for the post-layout simulation. Therefore, the proposed SSC-DVS was well suited for applications operating under large temperature changes.

Figure 28 presents the efficiency of the proposed architecture when the temperature varied from $-40$ to $120$ °C. It showed almost constant efficiency of 94% for the schematic simulation, while it showed 91% efficiency for the post-layout simulation. Therefore, the proposed SSC-DVS was well suited for applications operating under large temperature changes.
Figure 29 shows the measured efficiency of the proposed SSC-DVS versus the conversion ratio and output load current of the fourth stage (I_{out4}). The efficiency of more than 80% was obtained with an output load current of the fourth stage (I_{out4}) in the range of 50–550 µA. The efficiency values lower than the simulation results were primarily attributed to the slow transition of control signals as well as the parasitic circuit elements. We expect that the efficiency of the test chip could be improved to the level of post-layout simulations if we improved the control signals by adding buffer circuits.

![Figure 29](image-url)  
**Figure 29.** The measured results of the efficiency versus the conversion ratio and the output load current.

### 4.3. Comparison

Table 4 compares the key properties of the proposed SSC-DVS test chip with other switched-capacitor voltage converters recently published. The proposed 4-bit SSC-DVS showed $2^4 = 16$ conversion ratios. The 4-bit recursive voltage converter of [14] shows $2^4 - 1 = 15$ conversion ratios, while the 7-bit SAR of [9] can provide 117 conversion ratios. The designs reported in [15–17] show only one to three fixed conversion ratios.

|       | [9] | [14] | [15] | [16] | [17] | This Work |
|-------|-----|------|------|------|------|-----------|
| Year  | 2016| 2014 | 2016 | 2017 | 2017 | 2018      |
| Tech. (nm) | 180 | 250  | 28   | 180  | 28   | 130       |
| Topology | 7-bit SAR | 4-bit recursive | Self-oscillation | Multi-level self-oscillation | Soft-charging | 4-bit swapping |
| $V_{in}$ (V) | 3.4–4.3 | 2.5 | 1–1.2 | 0.7–20 | 3.2 | 1.5       |
| $F_{sw}$ (MHz) | 0.08–2.7 | 0.2–10 | - | - | 1600 | 50        |
| Conversion Ratio | 117 | 15  | 2.1 | $\frac{1}{2}, \frac{1}{3}, \frac{1}{4}$ | 3.1 | 16        |
| Step Size (mV) | 31.25 @ $V_{in}$ = 4V | 156 | - | - | - | 85        |
| $V_{out}$ (V) | >0.45 | 0.1–2.18 | 0.38–0.485 | 0.7–5.5 | 0.95 | 0.085–1.424 |
| $V_{ripple}$ (mV) | ≥17.15 | - | 48.5–75 | - | - | 2.656     |
| $I_{out}$ (µA) | 300 | 2000 | 0.172–435 | 10.7 | 2.722 | 1.5        |
| $C$ (nF) | 2.5 | 3  | 0.135 | 0.722 | 1.5 | 0.4        |
| Efficiency (%) | 72 | 85  | 87 @ $V_{out}$ = 0.46 | 68.7 @ $V_{in}$ = 7.5 | 82.6 | 85        |
| Area (mm²) | 1.69 | 4.645 | 0.104 | 0.55 | 0.117 | 0.334     |

The proposed SSC-DVS showed an almost rail-rail output voltage range, and thus, it could provide extremely low supply voltages to ultra-low power applications. The design of [9] provides a limited range of supply voltages that are larger than 0.45 V, while the designs reported in [15–17] provide an output voltage of only 0.5 $V_{in}$ or higher. Furthermore, the proposed SSC-DVS showed a smaller voltage ripple of 2.656 mV. For example, it showed around a 84% and 94% smaller voltage ripple than the recent voltage converters of [9,15], respectively. The measured results of the proposed
SSC-DVS showed a peak efficiency of 85%, which was higher than the previous circuits reported in [9,16,17].

The total size of its on-chip capacitors was 400 pF, while the total area of the SSC-DVS test chip was 0.334 mm$^2$, including the on-chip flying capacitors and output RC load.

5. Conclusions

In this paper, a reference-free, scalable, and high efficiency, multi-output DVS architecture based on $n$-bit swapping switched-capacitor topology is proposed. It employs $n$-cascaded 2:1 swapping capacitor stages to generate $2^n$ conversion ratios with a resolution of $\frac{V_{in}}{2^n}$. Its swapping switched-capacitor unit forms a structure of self-biasing, and, thus, ensures that the output voltage of each stage converges to the target voltage, which is determined by the digital code configuration. Thus, SSC-DVS does not require a power-hungry reference voltage generator and comparator feedback circuits, thus it can provide significantly higher energy efficiency than previous voltage converters. A 4-bit SSC-DVS was implemented into a test chip using a 130 nm MagnaChip CMOS process. Post-layout simulations were conducted with an input voltage of 1.5 V, switching frequency of 50 MHz, and a load circuit that modeled by a load resistor of 2 KΩ. The measurements and the realistic simulations, with all layout parasitic components, demonstrated that it achieved a stable 16 output voltage levels with a step size of 80 mV, and a ripple voltage as small as 2.656 mV. SSC-DVS exhibited a peak efficiency of 85% when it supplied a load current of 550 $\mu$A—a substantially higher energy efficiency compared with previous switch-capacitor converters.

Author Contributions: A.N.R. proposed, designed, and implemented the overall architecture of the proposed SSC-DVS. He, also, measured the performance of the proposed architecture to verify the test chip. H.W.K. guided and directed the first author for this work.

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