Research on Physical Layer Conformance Testing Technology of Ethernet Interface

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Abstract. The Ethernet physical layer is located at the bottom of the network structure and is responsible for the transmission and reception of electrical signals. The performance of the physical layer will directly affect the communication quality of network devices. According to the requirements of the IEEE 802.3-2000 and ANSI X3.263-1995 standards for the physical layer of the Ethernet, the physical layer conformance test standards and requirements of the 100Base-TX and 1000Base-T network interfaces are studied, and the physical layer is designed consistently. The test method shows that the test data is accurate and the test method can meet the requirements related to the physical layer conformance test.

1. Introduction
The Ethernet physical layer is at the bottom of the OSI reference model. It defines the electrical signals, optical signals, line status, clock reference, data coding and circuit characteristics required for data transmission and reception. It can be concluded in the industry that the impact of the physical characteristics of the Ethernet interface on the network performance plays an important role at a critical moment, which deserves extensive attention and attention.

2. Characteristic signal analysis of ethernet physical layer
In-depth study of the signal characteristics of the Ethernet physical layer is a prerequisite for the Ethernet physical layer conformance testing technology, and an important theoretical basis for testing technology research. According to the IEEE802.3 protocol specification, 100BASE-TX Ethernet in the forced 100M full-duplex communication mode, the output differential signal technical characteristics are as follows:
- Differential output voltage: 950mV ~ 1050mV;
- Overshoot: positive overshoot or negative overshoot <5% and decay to <1% within 8 ns;
- Signal symmetry test: 0.98 < positive overshoot / negative overshoot <1.02;
- Rise and fall time test: 3ns < rise, fall time < 5ns (10% ~ 90%);
- Rise and fall time symmetry test: the difference between the rising and falling times of the positive pulse is <0.5 ns, and the difference between the rising and falling time of the negative pulse is <0.5 ns.

The signal eye diagram template satisfies the requirements of the eye diagram model in the ANSI X3.263-1995 standard, as shown in Figure 1:
The consistency test of the 1000BASE-T Ethernet physical layer provides four modes. In each test mode, different characteristic signals need to be evaluated. The electrical signal and indicator evaluation requirements provided by test mode 1 are the most complicated and critical.

As shown in Figure 2, the signal template to be tested under test mode 1 conditions:

![Figure 2](image)

**Figure 1.** 100Base-TX eye diagram test template requirements

![Figure 2](image)

**Figure 2.** 1000Base-T network test mode 1 characteristic signal

The four transmitters of the PHY will continuously transmit the data sequence: +2,0 (127), -2,0(127), +1, 0(127), -1, 0(127), followed by +2 (128), –2(128), +2(128), –2(128), and finally 1024 zeros. When Mode 1 is enabled, the transmitter will transmit data at 125.00MHz ± 0.01% of the clock rate in the main clock mode. This sequence will be transmitted continuously without interruption. According to the test requirements, the 1000Base-T Ethernet card template 1 test needs to complete the peak voltage and symmetry and signal fading test of each of the 8 feature points of A, B, C, D, F, G, H, and J in Figure 1. The requirements for the peak voltage between point A and point B are: peak voltages of points A and B: 670 mV to 820 mV (150 mV tolerance range), and the difference between the peak voltages of points A and B cannot exceed 1%.

3. Research on Setting Method of Physical Layer Test Mode

To carry out the physical layer conformance test, the network interface to be tested needs to be set to a dedicated test mode, and the state of the interface physical layer indicator is determined by capturing a specific feature signal.

3.1. 100Base-TX network interface test mode setting

The 100Base-TX Ethernet physical layer conformance test is required to capture the 0x55 pattern signal for time domain testing and the 112 ns width pulse signal for amplitude domain testing.

For Ethernet cards that cannot be forced to set the communication rate, you can use the "taste" setting method to force the NIC communication rate to 100 Mbps full-duplex mode. The setting method is: using an Ethernet card capable of forcibly setting the communication rate, inputting an Idle signal forcing a 100M full-duplex rate to the RX end of the tested network card (DUT), and the
measured network card (DUT) according to the communication rate auto-negotiation mode and The rate parallel detection mechanism considers that the network is complete and synchronizes the 100M full-duplex rate. At this time, the TX end of the tested network card will issue a synchronous 100M full-duplex Idle code stream, which is convenient for capturing pulses of 96 ns width during the test. The circuit connection is shown in Figure 3:

![Figure 3. Schematic diagram of the "temptation" method](image)

3.2. 1000BASE-T network interface test mode setting
For the 1000BASE-T network interface, the test mode is set by enabling 9.13:15 bits of the GMII Management register, as shown in Table 1. The test mode only modifies the data sent by the transmitter circuit and does not modify the electrical and jitter settings of the transmitter and receiver in non-test mode.

| Bit1(9.15) | Bit2(9.14) | Bit3(9.13) | Mode                  |
|-----------|-----------|-----------|-----------------------|
| 0         | 0         | 0         | Normal mode           |
| 0         | 0         | 1         | Test Mode 1-Transmit Waveform Test Mode |

4. Research on Test Method of Physical Layer Consistency Characteristic Signal
Network interface physical layer characteristic signal test system, consisting of test instruments and test fixtures. The test instrument completes the capture analysis of the electrical parameters of the measured signal, the test fixture introduces the measured signal and complete input to the test instrument, triggers the design method to stably trigger the capture of the measured signal, and achieves accurate test technical indicators.

4.1. Test fixture selection
The IEEE Std 802.3-2000 standard requires test fixture load: $100\Omega \pm 0.2\%$ resistor and series inductance $\leq 20\text{nH}$ and parallel capacitance $\leq 2\text{pF}$ at frequency $\leq 100\text{MHz}$. In order to ensure that the test fixture meets the standard requirements, and the “impedance-frequency” characteristic curve of the fixture is flat, the standard recommends using the circuit structure shown below and the components used to meet the corresponding technical specifications.
4.2. Test instrument selection
In the IEEE Std 802.3-2000 standard, the minimum rise time of the output signal of the tested port is 3.0 ns. Therefore, the test instrument chosen must have sufficient bandwidth and sampling rate.

The design uses a 2.5GHz real-time oscilloscope and a 3.5GHz differential probe as a test instrument. The 2.5GHz real-time oscilloscope has a fast pulse edge setup time of 160ps, and the 3.5GHz differential probe has a fast edge setup time of 110ps. Test instrument + measured signal The pulse fast edge settling time is:

\[
T_{\text{r-total}} = \sqrt{\text{System rise time}^2 + \text{Signal rise time}^2} = \sqrt{160\,\text{ps}^2 + 110\,\text{ps}^2 + 3.0\,\text{ns}^2} = 3.01\,\text{ns}
\]

The test error of the rise/fall time is about 0.01 ns (about 0.3%), which fully meets the requirements of test accuracy. The test rate is 10 times the signal frequency, and the test error is about 0.5%. The test system sampling rate is consistent.

4.3. Oscilloscope trigger mode design
(a). 100Base-TX Ethernet physical layer parameter test
For the pulse width project test, the unique characteristic of the signal to be tested is 96 ns pulse width. The oscilloscope “pulse width” trigger mode is used to stably trigger the 96 ns pulse width signal, and the details of the parameter to be tested are observed by vertical offset and partial amplification to ensure test data. accurate. The trigger mode setting method is as follows:

Select the trigger mode as “pulse width trigger mode”, use the trigger mode within the specified time range, capture the positive voltage 96ns pulse width signal, set the trigger level to 500mV, select the pulse width range from 94.0ns to 98.0ns, and trigger the delay. 0ns, positive polarity voltage, trigger mode design interface shown in Figure 5:

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For the duty cycle distortion project test, the only characteristic of the signal to be tested is '01010101' for four consecutive MLT-3 hopping pulse waveforms. This paper uses the visual trigger design to complete the matching trigger capture for the specific waveform. The trigger mode design interface is shown in Figure 6. It is shown that a specific waveform is triggered by a matching window of six signal key feature points.

Figure 6. Visual triggering design diagram

(b). 1000BASE-T Ethernet physical layer parameter test

For the testing of the characteristic points of the test mode 1 template signal, it is necessary to use the "slow amplitude pulse" trigger mode and the "slow amplitude pulse + time base delay" trigger mode respectively.

"Slow amplitude pulse" trigger mode: Analyze the characteristic signal characteristics of test mode 1 and find that point A, point C and point H are positive voltage signals. According to the technical index point A, the voltage should be 0.67V~0.82V, and the voltage at point C should be A. 0.5 times the point voltage, ±2% error, H point voltage ≥ A point; B point, D point, F point is a negative voltage signal, according to the technical point B point voltage should be 0.67V~0.82V, D point voltage should be 0.5 times the voltage at point B, the error is ±2%, and the voltage at point F is ≥ point B. The characteristic signals A, C, H, B, D, and F are in accordance with the characteristics of the runt pulse. The voltage threshold design can be used to accurately capture the waveforms of the characteristic signals at the test point using the advanced trigger mode. Analyze signal parameters.

"Low pulse + time base delay" trigger mode: characteristic signal F point, G point, H point, J point are located at the top and bottom of two pulse wide-band, equal-amplitude pulse signals, which cannot be used because the measured signals are consistent in characteristics. A single trigger model accurately captures the signal, based on the use of the "slight pulse" trigger mode to accurately capture the results of the characteristic signal D point, the design uses the "slow amplitude + time base delay" trigger mode to signal F point, H point trigger design.

The wideband digital oscilloscope DPO7254C has a 5 ns to 250 s time base delay function with a delay accuracy of ±2.5×10⁻⁶. According to the definition of IEEE Std 802.3-2000 standard, the F point, the H point and the signal D point are separated by 2.0 μs and 3.0 respectively. Ss. Select the advanced trigger function of DPO7254C wideband oscilloscope, select the trigger mode as “trowth pulse trigger mode”, set the trigger high level to -400mV, low level to -200mV, as shown in Figure 7, the trigger
delay is 0ns, negative polarity Voltage, adjust the oscilloscope delay setting, the delay time is set to: "2.0µs", "3.0µs", respectively, used to capture the signal point F, H point.

![Figure 7. Schematic diagram of "attenuation pulse + time base delay" trigger design](image)

5. Test

Set up the test environment, set the oscilloscope trigger mode, and complete the test for each characteristic signal of the Ethernet interface.

5.1. 100Base-TX Ethernet physical layer characteristic signal test

(a). Signal amplitude and overshoot test

The “Differential Mode Output Voltage” and “Signal Amplitude Symmetry” items are tested using the oscilloscope's automatic measurement (Measure) function for peak voltage high/low measurement and calculated by |+Vout/-Vout| data. “Waveform overshoot Measure After the oscilloscope stably captures the 96ns pulse waveform, set the vertical offset to observe the waveform details of the top (bottom) part of the waveform (the positive voltage selects the 700mV~1050mV offset range, the negative voltage selects the -700mV~-1050mV offset range) The +Overshoot/-Overshoot parameter measurement is completed using the oscilloscope's automatic measurement (Measure) function.

(b). Signal fast edge test

Since the 100Base-TX interface is based on the 4B/5B signal encoding method, when the signal waveform shown in the figure below appears, the oscilloscope automatic measurement function will mistake the "101" pattern signal as a rising edge of the pulse waveform, and a test error will occur. In order to avoid the above errors and meet the horizontal resolution requirement of the rising edge of the pulse waveform test, after the oscilloscope stably captures the 96ns pulse width to be tested, the “vertical offset + partial amplification” method is needed to accurately test the rising and falling edge data of the waveform.

The signal rise time is from 0.01 ns to 5.0 ns. According to the test requirements, the oscilloscope horizontal time base resolution should reach 1 ns/div to 2 ns/div. After the oscilloscope stably captures the 96ns signal, the trigger point position is at the 96ns pulse width falling edge, which is limited by the oscilloscope's memory depth capability. Under the condition of the oscilloscope horizontal time base resolution of 1 ns/div to 2 ns/div, the delay cannot be directly observed by the delay function. Or lead the signal waveform at the 96ns position. Call the oscilloscope local amplification auxiliary function, select the local magnification according to the oscilloscope main time base parameter, and the amplified horizontal time base resolution should be controlled within the range of 1 ns/div to 2 ns/div, and adjust the partial amplification window to the pre-observed waveform detail. Implement an accurate test of this parameter.

(c). Duty cycle distortion test

The visual triggering method is used to stably capture the waveform to be tested. Since the duty cycle distortion refers to the change of the pulse width due to deformation, time delay, etc. during the transmission, the change changes the ratio of the pulsed and pulseless durations. The pulse width measurement position should be controlled during the test at Vout/2 of the pulse.

4.1. 1000BASE-T Ethernet physical layer characteristic signal test

(a). Peak voltage (signal amplitude symmetry test)
The “peak voltage” or “signal amplitude symmetry” item test uses the peak voltage high/low measurement function in the oscilloscope automatic measurement (Measure) function and is calculated by the |+Vout/-Vout| data.

(b). Signal fading test
Set the oscilloscope trigger mode, use the "Low pulse + time base delay" mode for stable capture, accurately distinguish the voltage amplitude waveform of each characteristic signal point, use the oscilloscope cursor measurement function, as shown in Figure 8: cursor 1 is placed in the characteristic signal F The maximum amplitude of the point is set. The cursor 2 is placed at the time base position of the characteristic signal F point 500.0 ns. The cursor 1 test value in the Measure parameter at the lower left of the recording screen is V1, the cursor 2 test value is V2, and V2/V1 is the signal fading value. The test result satisfies V2/V1 ≥ 73.1% and meets the technical requirements of the index.

![Figure 8. Signal fading test diagram](image)

6. Conclusion
The Ethernet physical layer is at the bottom of the OSI reference model and not only undertakes the physical media function of data transmission for the entire network but also provides the physical link function and standard interface for transmitting the original bit stream to the data link layer. The impact of the physical characteristics of the Ethernet interface on the network performance plays an important role at a critical moment, which deserves extensive attention and attention. Based on the analysis of the characteristics and generation methods of the physical layer characteristic signal parameters of the network equipment, based on the advanced trigger function of the digital oscilloscope, a test method capable of accurately capturing the specific characteristic signal is designed, which can meet the test and analysis requirements of the physical layer consistency characteristic signal and pass the test. Experiments show that the method is stable and reliable and can be used in engineering practice.

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