Pinch-Off Formation in Monolayer and Multilayers MoS$_2$ Field-Effect Transistors

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Abstract: The discovery of layered materials, including transition metal dichalcogenides (TMD), gives rise to a variety of novel nanoelectronic devices, including fast switching field-effect transistors (FET), assembled heterostructures, flexible electronics, etc. Molybdenum disulfide (MoS$_2$), a transition metal dichalcogenides semiconductor, is considered an auspicious candidate for the post-silicon era due to its outstanding chemical and thermal stability. We present a Kelvin probe force microscopy (KPFM) study of a MoS$_2$ FET device, showing direct evidence for pinch-off formation in the channel by in situ monitoring of the electrostatic potential distribution along the conducting channel of the transistor. In addition, we present a systematic comparison between a monolayer MoS$_2$ FET and a few-layer MoS$_2$ FET regarding gating effects, electric field distribution, depletion region, and pinch-off formation in such devices.

Keywords: 2D materials; KPFM; MoS$_2$; pinch-off

1. Introduction

Two-dimensional (2D) materials, such as graphene and transition metal dichalcogenides (TMDs), attract extensive interest from the research community as they are considered as possible candidates for post-silicon electronics [1]. Molybdenum disulfide (MoS$_2$), is considered a promising candidate for various applications in microelectronics [2–6], optoelectronics [7,8], sensing [9,10], spintronics [11,12], and many others [13,14] due to its unique electrical properties [15,16] and thermal stability. The performance of the applications listed above is entangled with specific electrostatic behavior at the interface between the MoS$_2$ and the other compounds within the device [17].

Depletion region formation at MoS$_2$ homojunctions, heterojunctions, and metal junctions has been modeled and investigated by many groups [17–20]. Nipane et al. [21] modeled the electrostatics of lateral junctions in atomically thin materials using line charges representation, Sohn et al. [22] investigated the electrostatic band alignment at Au/MoS$_2$ contacts as a function of the thickness of MoS$_2$ exfoliated flakes, and Chiu et al. [23] determined the band alignment in single-layer MoS$_2$/WSe$_2$ heterojunctions using micro X-ray photoelectron spectroscopy and scanning tunneling microscopy (STM).

Kelvin probe force microscopy (KPFM) is a powerful tool for the direct measurement of the surface potential of semiconductors [24]. Several groups have used this technique to monitor the work function difference between the different number of layers of MoS$_2$ samples [25], studying the effect of the substrate on the electrostatic properties of MoS$_2$ layers [26], and assessing the effect of gas and molecular adsorption on chemical vapor deposition (CVD)-grown MoS$_2$ flakes [27–29]. Other groups have measured the built-in potential of single-layer MoS$_2$ heterojunctions using KPFM [30] and demonstrated the electrical properties of the contact between MoS$_2$ and different metals [31]. These measurements resemble the use of KPFM for contact resistance evaluation [32] and contact-free mobility estimation [33] in thin-film organic transistors.
Current saturation in thin-film FET devices is attributed to both velocity saturation and pinch-off formation [6,34]—moreover, it is a major accelerator of the device’s performance, controlling the output conductance and on/off ratio of the transistor [3]. However, no experimental results on the pinch-off effect in ultrathin TMDs have been published. In this work we present a method for the direct observation and determination of the pinch-off voltage of a thin-layer TMD FET through the measurement of the electrostatic potential along the conducting channel of the transistor in operando. We observe, for the first time to our knowledge, pinch-off formation in such devices and discuss the differences between single- and few-layer MoS$_2$ FET devices.

2. Materials and Methods

Monolayer and few-layer MoS$_2$ samples were transferred on top of an 8 mm square dye made of a highly doped P-type silicon wafer covered by a 90 nm silicon oxide (SiO$_2$) layer via the mechanical exfoliation with scotch tape, initially developed for graphene [35], of MoS$_2$ crystals supplied by Structure Probe Inc. (SPI) Supplies (West Chester, PA, USA). The wafer was patterned with gold alignment marks prior to exfoliation using optical lithography, and monolayer and few-layer MoS$_2$ flakes were identified by their contrast using an optical microscope. Contacts made of 50 nm gold on top of a 3 nm titanium were designed by E-beam lithography and evaporated using an electron-beam evaporator (VST, Israel), and lift off was conducted using N-Methyl-2-pyrrolidone (NMP) at 80 $^\circ$C. The devices were then placed on a chip carrier, wire bonded, transferred into a N2 glove box and annealed at 95 $^\circ$C to reduce humidity.

The electrical measurements and device characteristics, performed inside a N2 glove box, were conducted using a semiconductor parameter analyzer (B1500A, Agilent Technologies, Santa Clara, CA, USA) and atomic force microscope (AFM)-based amplitude modulation-Kelvin probe force microscopy (AM-KPFM) (Bruker, MA, USA). The measuring step size was ~20 nm, enabling in situ measurements of the electrostatic potential with lateral resolution approaching the limit of the KPFM in nitrogen atmosphere [36].

3. Results and Discussion

An AFM image of a monolayer MoS$_2$ FET with a channel length (L) of 5.5 um and a width (W) of 0.75 um, in addition to a topography profile along the device, are shown in Figure 1a. Raman spectroscopy, presenting a separation of 18.06 cm$^{-1}$ between E$_{2g}^1$ and A$_{1g}$ corresponding to a single layer of MoS$_2$ [37], is presented in Figure 1b. Figure 1c shows the $I_d(V_g)$ characteristics of the device for several gate voltages ($V_g$), while Figure 1d depicts the $I_d(V_g)$ curves in linear scale for several drain voltages ($V_d$) showing n-type transistor behavior, as expected from unintentionally doped exfoliated MoS$_2$ flakes [38–40]. Logarithmic scale $I_d(V_g)$ curves, for a gate voltage range of 0.5 to 8 V in which the high drain voltage curves are united into a single curve and separated as the gate voltage increases, as expected in the presence of pinch-off, are presented in the inset. Standard metal–oxide–semiconductor field-effect transistor (MOSFET) theory [41] was used to extract the field-effect mobility from the $I_d(V_g)$ curves in the linear regime, and found to be 2.52 cm$^2$/V·s. Current saturation, as depicted in the inset of Figure 1c for gate voltages of 0 and 5 V, is likely to take place in FET devices, being more possible evidence of pinch-off formation near the drain electrode.
where the gate is grounded. It is observed that a depletion region, resulting in an increased electrostatic potential along the device with $V$ potential slope near the drain electrode, starts to form at a drain voltage of 3 V, while starting at the MoS$_2$ unintentionally n-type doping concentration of $1.4 \times 10^{12}$ cm$^{-2}$ [38] shifting the Fermi level position of the MoS$_2$ towards the conduction band, a Schottky barrier height of 1.4 eV will be formed and a built-in potential resulting in a depletion region will be created. Increasing the gate voltage will

$\psi_{bi} = \phi_{Au} - \chi_{MoS_2} + \frac{(E_c - E_f)}{q} + V$  \hspace{1cm} (1)

where $\phi_{Au}$ is the gold work function, $\chi_{MoS_2}$ is the MoS$_2$ affinity, $E_c - E_f$ is the energy difference between the conduction band and the Fermi level of the MoS$_2$, and $V$ is the potential induced by the gate electrode. Assuming a gold work function of 5.4 eV [44], a MoS$_2$ electron affinity of 4 eV [45], and an unintentionally n-type doping concentration of $1.4 \times 10^{12}$ cm$^{-2}$ [38] shifting the Fermi level position of the MoS$_2$ towards the conduction band, a Schottky barrier height of 1.4 eV will be formed and a built-in
potential resulting in a depletion region will be created. Increasing the gate voltage will increase the charge carrier concentration in the conducting channel, and the depletion region will become narrower.

The charge concentration induced by the gate is:

$$Q = C_{OX} \left( V_{gs} - V_t - V(x) \right)$$

(2)

where $C_{OX}$ is the structure capacitance per unit area, $V_t$ is the threshold voltage, and $V(x)$ is the measured electrostatic potential minus the electrostatic potential at $V_{gs} = 0 \ V$ [46]. Following this equation, a point with no charge will be created near the drain when $V(x) = V_{drain} = V_{gs} - V_t$; this is commonly defined as the pinch-off. Any additional increase in the drain voltage will increase the pinch-off region, inducing a larger electric field in this region, as depicted in Figure 2c above. By increasing the gate voltage, a large concentration of carriers is injected into the channel, and the pinch-off voltage is increased accordingly.

![Figure 2](image)

*Figure 2.* (a) Electrostatic potential measurements at varying drain voltages ($V_d = 1 \ V$ to $V_d = 12 \ V$ with 1 V steps), while gate and source electrodes are grounded. (b) Electrostatic potential measurements at varying drain voltages ($V_d = 1 \ V$ to $V_d = 7 \ V$ with 1 V steps), while $V_g = 5 \ V$ and the source electrode is grounded. (c) Electric field distribution along the transistor corresponding to the bias conditions in (a). The inset shows the electric field at the Au/MoS$_2$ interface near the source and drain electrodes as a function of the drain voltage at $V_g = 0 \ V$. (d) Pinch-off position extraction at $V_g = 0 \ V$ for representative drain voltages. In the caption, the pinch-off evaluation as a function of the drain voltage is given.

Figure 2c shows the electric field distribution across the single-layer MoS$_2$ FET device for drain voltages between 1 and 12 V, for $V_{gs} = 0 \ V$. The electric field is calculated as the first derivative of the electrostatic potential distribution, measured by the KPFM, as presented in Figure 2a. The inset of Figure 2c presents the electric field at the source–MoS$_2$ and MoS$_2$–drain interfaces as a function of increasing $V_{gs}$. At drain voltages lower than the pinch-off voltage, the electric field is accumulated at the source–MoS$_2$ interface, while at some other voltages, namely the pinch-off voltage, the electric
field at the source–MoS\textsubscript{2} interface remains constant and the electric field at the MoS\textsubscript{2}–drain interface increases. A vertical line marking the drain voltage at which the electric field becomes $1 \times 10^6 \, V/m$, representing the pinch-off voltage, is also shown in Figure 2c. Given a gate voltage of 0 \, V, the threshold voltage can be calculated using the following formulation: $V_t = -V_{\text{pinch-off}} \approx -5 \, V$.

As the electric field at the MoS\textsubscript{2}–drain interface increases, the portion of depleted channel required to screen this field increases. In order to establish a rigorous method for pinch-off positioning, we determined the pinch-off point in a manner similar to how the slope transition is extracted in logic device state determination. Following this method, the pinch-off position is defined as the intersection between the linear fit of the plateau region of the electrostatic potential along the conducting channel and the linear fit of the steepest electrostatic potential slope at the MoS\textsubscript{2}–drain interface. The results are presented in Figure 2d, while the inset of Figure 2d shows the pinch-off position as a function of the drain voltage. As expected, the pinch-off position remains constant for drain voltages lower than the pinch-off voltage and moves towards the source as the drain voltage increases beyond this voltage.

Figure 3 shows a detailed comparison between single-layer and multilayer (composed of 4–5 layers and exhibiting 20 \text{cm}^2/\text{V-s} field-effect mobility) MoS\textsubscript{2} FET devices. Figure 3a shows the accumulated electric field at the source–MoS\textsubscript{2} interface as a function of the drain voltage for several gate voltages for the monolayer MoS\textsubscript{2} FET device; the vertical lines represent the pinch-off voltage as described above. The threshold voltage, extracted using the above formula as a function of the gate voltage, is shown in the inset. Figure 3b demonstrates the pinch-off widening at the MoS\textsubscript{2}–drain interface as a function of the drain voltage for several gate voltages for the monolayer device, where the zero position is the pinch-off location for $V_d = 0 \, V$ and the negative values represent pinch-off widening into the conducting channel away from the drain. As expected, an increased gate voltage, resulting in enhanced conducting channel, requires a higher drain voltage to achieve pinch-off.

Figure 3c,d show the accumulated electric field at the source–MoS\textsubscript{2} interface, in addition to the corresponding threshold voltages, and demonstrate the pinch-off widening at the MoS\textsubscript{2}–drain interface for a multilayer MoS\textsubscript{2} FET device. As shown, the corresponding pinch-off voltages in the multilayer device are smaller relative to the monolayer device. This decrease in the pinch-off voltage with an increasing number of layers may arise from the unintentional doping in the exfoliated MoS\textsubscript{2} samples, which is known to be attributed to sulfur vacancies [39,40,47–49] formed mostly at interfaces, resulting in a higher carrier concentration in monolayer samples compared to multilayers [50]; this larger carrier concentration increases the threshold and pinch-off voltages.

Sulfur vacancies in addition to intentional doping of thin-film FETs will cause variations in device performance including on/off ratio, mobility, and current saturation. Observation of the pinch-off phenomenon, extraction of the pinch-off voltage, and calculation of the corresponding threshold voltage enables us to distinguish between the governing mechanisms in such devices. In addition, since the mobility in such devices is known to be field dependent [34] at drain voltages higher than the pinch-off voltage, the electric field along the device will remain constant, and hence the mobility will be independent of the drain bias. We have presented good agreement between the measured pinch-off voltage (Figure 3a) and the current saturation voltage presented in Figure 1c. Consequently, we deduce that the pinch-off phenomenon is the dominant mechanism of current saturation in the measured devices, and that the device performance is not limited by carrier velocity saturation.
代表电压下的电位差和电场强度的函数。在 caption 中，偏置电压条件下的 pinch-off 位置也给出。随着电场强度在 MoS_2– 源界面的增加，所需的去饱和通道部分增加以屏蔽该电场。为了建立一个严格的方法来确定 pinch-off 位置，我们以类似于逻辑器件状态确定中斜率转换的提取方式确定 pinch-off 点。根据这种方法，pinch-off 位置定义为电势分布沿导电通道的平坦区域的线性拟合与 MoS_2– 源界面的电势分布的最陡峭电势斜率的线性拟合的交点。结果如图 2d 所示，图 2d 的插图显示了 pinch-off 位置随偏置电压的变化。如预期， pinch-off 位置在偏置电压低于 pinch-off 电压时保持不变，并随着偏置电压超过此电压而向源端移动。

图 3 显示了单层和多层（由 4–5 层组成，具有 20 cm^2/V·s 电场效应迁移率）MoS_2 FET 器件的详细比较。图 3a 显示了源–MoS_2 接口附近 Au–MoS_2 接口的电场随偏置电压的分布；垂直线代表上述描述的 pinch-off 电压。用上述公式提取的阈值电压在不同 gate 电压下显示。图 3b 显示了 pinch-off 区域在 MoS_2– 源界面的宽度随偏置电压的分布；零位置为 pinch-off 位置，负值表示 pinch-off 区域向导电通道远离 drain 的延伸。如预期，增强的 gate 电压，导致增强的导电通道，需要更高的 drain 电压才能实现 pinch-off。

图 3. (a) 电场在 Au–MoS_2 接口的源电极附近随 drain 电压变化，不同偏置条件下的电场强度也列出。图 3a 的 inset 显示了单层 MoS_2 电晶体的阈值电压。 (b) pinch-off 位置随 drain 电压的变化，不同 gate 电压下，MoS_2 单层电晶体的 pinch-off 区域。 (c,d) 相当于 (a,b)，分别用于 few-layer MoS_2 FET。

4. 结论

总结，一个 KPFM 基于的分析研究被用于研究 thin-layer MoS_2 FET 器件中的 pinch-off 现象。我们通过详细分析电势分布沿器件来直接观察到单层和多层 MoS_2 FETs 中 pinch-off 区域的形成。我们展示了 pinch-off 区域宽度和 pinch-off 电压的依赖性，以及在不同偏置条件下应用的偏置。它被证明 pinching-off 电压随着 charge carrier 浓度的增加而降低，这与 MoS_2 表面的增加硫空位相对应。更好地理解 pinch-off 现象，以及它对 device 性能的关键影响，特别是在几层材料中，是设计下一代 TMD 基于器件的一个关键点。

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