Microprocessor Optimizations for the Internet of Things

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The Internet of Things (IoT) refers to a pervasive presence of interconnected and uniquely identifiable physical devices whose goal is to gather data and drive actions in order to improve productivity, and ultimately reduce or eliminate reliance on human intervention for data acquisition, interpretation and use. The proliferation of these connected low-power devices will result in a data explosion that will significantly increase data transmission costs with respect to energy consumption and latency. Edge computing reduces these costs by performing computations at the edge nodes prior to data transmission to interpret and/or utilize the data. While much research has focused on the IoT’s connected nature and communication challenges, the challenges of IoT embedded computing with respect to device microprocessors and optimizations has received much less attention. This article explores IoT applications’ execution characteristics from a microarchitectural perspective and the microarchitectural characteristics that will enable efficient and effective edge computing. To tractably represent a wide variety of next-generation IoT applications, we present a broad IoT application classification methodology based on application functions. Using this classification, we model and analyze the microarchitectural characteristics of a wide range of state-of-the-art embedded system microprocessors, and evaluate the microprocessors’ applicability to IoT edge computing. Using these analysis as foundation, we discuss the tradeoffs of potential microarchitectural optimizations that will enable the design of right-provisioned microprocessors that are efficient, configurable, extensible, and scalable for next-generation IoT devices. Our work provides insights into the impacts of microarchitectural characteristics on microprocessors’ energy consumption, performance, and efficiency for various IoT application execution requirements. Our work also provides a foundation for the analysis and design of a diverse set of microprocessor architectures for edge computing in next-generation IoT devices.

1. INTRODUCTION AND MOTIVATION

The Internet of Things (IoT) is an emerging technology that refers to a pervasive presence of interconnected and uniquely identifiable physical devices, comprising an expansive variety of devices, protocols, domains, and applications. The IoT’s goal is to gather data and drive actions in order to improve productivity, and ultimately reduce or eliminate reliance on human intervention for data acquisition, interpretation, and use [Ashton 2009]. The IoT has been described as one of the disruptive technologies that will transform life, business, and the global economy [McKinsey 2015]. Based on analysis of key potential IoT use-cases (e.g., healthcare, smart cities, smart home, transportation, manufacturing, etc.), it is estimated that by 2020, the IoT will constitute a trillion dollar economic impact and include more than 50 billion low-power devices that will generate petabytes of data [Gartner Newsroom 2015; Sundmaeker 2010; Zhou 2011].

Due to the IoT’s expected growth and potential impact, much research has focused on the IoT’s communication and software layer [Atzori 2010; Gubbi 2013; Li 2011; Miorandi 2012], however, the challenges of IoT computing, especially with respect to...
device microprocessors, has received much less attention. Computing on IoT devices introduces new substantial challenges, since IoT devices’ microprocessors must satisfy increasingly growing computational and memory demands, maintain connectivity, and adhere to stringent design and operational constraints, such as low cost, low energy budgets, and in some cases, real-time constraints. These challenges necessitate new research focus on microarchitectural optimizations that will enable designers to develop right-provisioned architectures that are efficient, configurable, extensible, and scalable for next-generation IoT devices.

Figure 1 depicts an IoT use-case that illustrates the high-level components of the traditional IoT model. The IoT typically comprises of several low-power/low-performance edge nodes, such as sensor nodes, that gather data and transmit the data to high-performance head nodes, such as servers, that perform computations for visualization and analytics. In a data center, for example, data aggregation from edge nodes facilitates power and cooling management [Bash 2006; Patel 2003].

However, the growth of the IoT and the resulting exponential increase in acquired/transmitted data poses significant bandwidth and latency challenges. These challenges are exacerbated by the intrinsic resource constraints of most embedded edge nodes (e.g., size, battery capacity, real-time deadlines, cost, etc.) that may conflict with design objectives (e.g., minimizing energy, size, etc.). Additionally, increasing consumer demands for high-performance IoT applications will necessitate acquisition and transmission of complex data. For example, another potential impactful IoT use-case is medical diagnostics [Medical Image Processing 2015]. With the advent of technological advances such as cheap portable magnetic resonance imaging (MRI) devices and portable ultra-sound machines, several gigabytes (GBs) of high resolution images will be transmitted to medical personnel for remote data processing and medical diagnosis. In some cases, this system must scale to a network of many portable medical devices that transfer data to medical personnel. Transmitting this data will result in bandwidth bottlenecks and pose additional challenges for real-time scenarios (e.g., medical emergencies) where the latency must adhere to stringent deadline constraints.

The IoT can also incur significant, and potentially unsustainable, energy overheads. Previous work [Kwok 2006] established that energy consumed while transmitting data is significantly more than the energy consumed while performing computations on the data. For example, the energy required by Rockwell Automation’s sensor nodes to transmit one bit of data is 1500-2000X more than the energy required to execute a single instruction (depending on the transmission range and specific computations) [Raghunathan 2004].

![Figure 1. High-level components of the Internet of Things (IoT)](image_url)
To address these challenges, edge computing performs computations that process, interpret, and use data at the edge nodes, in order to minimize the transmitted data, thereby improving latency, bandwidth, and energy consumption. For example, in the medical diagnostics use-case described above, rather than sending several GBs of MRI data to the medical personnel for diagnostics, the portable MRI machine (the edge node) is equipped with sufficient computational capabilities and algorithms to extract information and interpret the data. Only processed data (e.g., information about an anomaly in the patient) is transmitted to the medical personnel, thus speeding up the diagnosis process and reducing the MRI machine’s energy consumption. Alternatively, the data could be quantifiably reduced using intelligent algorithms and computations, such that only important information is transmitted to the medical personnel. However, the edge nodes’ computing capabilities must be sufficient/right-provisioned to perform and sustain the required computations, while adhering to the nodes’ design constraints (e.g., form factor, energy consumption, etc.).

To ensure that microprocessor architectures designed and/or selected for the IoT have sufficient computing capabilities, a holistic approach, involving both application and microarchitecture characteristics, must be taken to determine microarchitectural design tradeoffs. However, due to the wide variety of IoT applications and the diverse set of available architectures, determining the appropriate architectures is very challenging. This paper seeks to address these challenges and motivate future research in this direction.

In this paper, we perform an expansive study and characterization of the emerging IoT application space and propose an application classification methodology to broadly represent IoT applications. Based on this classification, we propose a benchmark suite that provides a tractable starting point for representing key computations that occur in the IoT application space. Our benchmark suite uses the computational dwarfs methodology [Asanovic 2006] and allows IoT computational patterns to be represented at a high level of abstraction. This method has also been used by other previous work in different computing domains (e.g., [Lovely 2014]). Furthermore, we propose a high-level design methodology for identifying right-provisioned architectures for edge computing use-cases, based on the executing applications and the applications’ execution characteristics (e.g., compute intensity, memory intensity, etc.). Using this methodology, we model and analyze several state-of-the-art low power processors’ microarchitectural characteristics using GEM5 [Binkert 2011] architectural simulations, and evaluate these processors’ applicability to IoT edge computing using various evaluation metrics. Finally, using these analysis, we discuss the tradeoffs of microarchitectural optimizations that will enable the design of right-provisioned IoT microprocessor architectures.

2. RELATED WORK

Due to the expected growth of the IoT, an increasing amount of research [Atzori 2010; Giusto 2010; Gubbi 2013] focuses on understanding and discovering insights into various aspects of the IoT. Much emphasis has been placed on the software layer of the IoT, however, the edge nodes’ hardware components and processing capabilities must also be considered [Sanchez-Sinencio 2014], especially in the context of edge computing.

Bonomi et al. [Bonomi 2012] proposed fog computing as a virtualized platform that provides compute, storage, and networking services between edge nodes and cloud computing data centers. Fog computing reduces the bandwidth bottleneck and latency by moving computation closer to the edge nodes. Our work explores further reduction in bandwidth, latency, and energy consumption by equipping the edge nodes with sufficient computation capacity in order to minimize data transmission. Gaura et al. [Gaura 2013] examined the benefits of edge mining, in which data mining takes place on the edge devices. The authors showed that edge mining has the potential to reduce
the amount of transmitted data, thus reducing energy consumption and storage requirements.

Previous works have proposed classifications for various IoT components. Gubbi et al. [Gubbi 2013] presented a taxonomy for a high level definition of IoT components with respect to hardware, middleware, and presentation/data visualization. Tilak et al. [Tilak 2002] presented a taxonomy to classify wireless sensor networks according to different communication functions, data delivery models, and network dynamics. Tory et al. [Tory 2004] presented a high level visualization taxonomy that classified algorithms based on the characteristics of the data models. However, to the best of our knowledge, our work presents the first classification of IoT applications based on the applications’ functions. Since the applications’ functions determine the execution characteristics, the functions have a more direct impact on the microprocessor execution requirements.

3. IoT APPLICATION CLASSIFICATION

The IoT offers computing potential for many application domains, including transportation and logistics, healthcare, smart environment, personal and social domains [Atzori 2010], etc. However, there is currently very little research that characterizes these applications with respect to their execution characteristics. One of the biggest challenges the IoT presents is the huge number and diversity of use-cases and potential applications that will be executed on IoT devices. This challenge is exacerbated by the fact that only a small fraction of these applications are currently available in society. Thus, a significant amount of foresight is required in designing microprocessor architectures to support the IoT’s emergence and growth.

As an initial step towards understanding IoT applications’ execution characteristics, we performed an expansive study of IoT use-cases and the application functions present in these use-cases. Since it is impractical to consider every IoT application within these use-cases/application domains, based on our study, we propose an application classification methodology that provides a high level, broad, and tractable representation of a variety of IoT applications using the applications’ functions. Our IoT application classification consists of five application functions: sensing, communications, image processing, compression (lossy/lossless), security, and fault tolerance. While this classification may not be exhaustive, it represents a wide variety of current and potential IoT applications and provides an extensible framework that allows emerging applications/application domains to be classified. In this section, we describe the application functions and motivate these functions using a medical diagnostics use-case, where applicable, or other specific examples of current and/or emerging IoT applications.

3.1 Sensing

Sensing involves data acquisition (e.g., temperature, pressure, motion, etc.) about objects or phenomena, and will remain one of the most common application functions in several application domains. In these applications, activities/information/data of interest are gathered for further processing and decision making. We use sensing in our IoT application classification to represent applications where data acquired using sensors must be converted to a more useable form. Our motivating example for sensing applications is sensor fusion [Nakamura 2007], where sensed data from multiple sensors are fused to create data that is considered qualitatively or quantitatively more accurate and robust than the original data.

Sensor fusion algorithms can involve various levels of complexity and compute/memory intensity. For example, sensor fusion could involve aggregating data from various sources using simple mathematical computations, such as addition, minimum, maximum, mean, etc. Alternatively, sensor fusion could involve more
computationally complex/expensive applications, such as fusing vector data (e.g., video streams from multiple sources), which requires a substantial increase in intermediate processing.

In a medical diagnostics use-case, for example, sensing is vital in a body area network [Chen 2011], where non-invasive sensors can be used to automatically monitor a patient’s physiological activities, including blood pressure, heart rate, motion, etc. Several sensing devices, such as portable electrocardiography (ECG), electroencephalography (EEG), and electromyography (EMG) machines, motion and blood pressure sensors could be equipped with additional computational resources that enable the devices to not only gather data, but also analyze the data in order to reduce the amount of transmitted data, with minimal energy or area overheads.

3.2 Communications

Communications is one of the most common IoT application functions due to the IoT’s intrinsic connected structure, where data transfers traverse several connected nodes. There are many communication technologies (e.g., Bluetooth, Wi-Fi, etc.), and communication protocols (e.g., transfer control protocol (TCP), the emerging 6lowpan (IPv6 over low power wireless personal area network), etc.). However, in this work, we highlight software defined radio (SDR) [Lee 2005], which is a communication system in which physical layer functions (e.g., filters, modems, etc.) that are typically implemented in hardware are implemented in software.

SDR is an emerging and rapidly developing communication system that is driving the innovation of communications technology, and promises to impact all areas of communication. SDR is growing in popularity because of its inherent flexibility, which allows for flexible incorporation and enhancements of multiple radio functions, bands, and modes, without requiring hardware updates. SDR typically involves an antenna, an analog-to-digital converter (ADC) connected to an antenna (for receiving) and a digital to analog converter (DAC) connected to the antenna (for transmitting). Digital signal processing (DSP) operations (e.g., Fast Fourier Transform (FFT)) are then used to convert the input signals to any form required by the application. SDR applications are typically compute intensive, with small data and instruction memory footprints. SDR algorithms can be efficiently executed using general purpose microprocessors or more specialized processors, such as digital signal processors (DSPs) or field-programmable gate arrays (FPGAs), or heterogeneous architectures combining different kinds of microprocessors. Other examples of communication applications include packet switching and TCP/IP.

3.3 Image processing

In the IoT context, image processing represents applications that involve any form of signal processing where the input is an image or video stream from which characteristics/parameters must be extracted/identified. Additionally, this classification also involves applications in which an image/video input must be converted to a more usable form. Several emerging IoT applications, such as automatic number license plate recognition, traffic sign recognition, face recognition, etc., involve various forms of image processing. For example, face recognition involves operations, such as face detection, landmark recognition, feature extraction, and feature classification, all of which involve image processing.

Image processing is important for several impactful IoT use-cases, which lends to the need for efficient microprocessor architectures for executing image processing applications. For example, in medical diagnostics, image processing can be used to increase the reliability and reproducibility of disease diagnostics. Image processing can provide medical personnel with quantitative data from historical images, which can be used to supplement qualitative data currently used by specialists. The National
Institute of Health (NIH) supports the Medical Image Processing, Analysis, and Visualization (MIPAV) application [Medical Image Processing 2015], which enables medical researchers to easily share research data and enhance their ability to diagnose, monitor, and treat medical disorders. However, since image processing applications are typically data-rich, and both memory and compute intensive, novel optimization techniques are required to enable the efficient execution of these applications in the context of IoT edge computing. Furthermore, some image processing applications require large input, intermediate, or output data to be stored (e.g., medical imaging), thus requiring a large amount of memory storage.

3.4 Compression

With the increase in data and bandwidth-limited systems, compression can reduce communication requirements to ensure that data is quickly retrieved, transmitted, and/or analyzed. Several emerging IoT use-cases will involve large volumes of data, which necessitates efficient compression techniques and processing to accommodate the rapid growth of the data and to reduce transmission latency and bandwidth costs [Xiong 2003]. Additionally, since most IoT devices are resource-constrained, compression also reduces storage requirements when storage on the edge node is required. For example, data gathered using sensors in a body area network can be quantifiably and intelligently reduced in order to minimize transmission and storage requirements for medical diagnosis devices.

Compression techniques can be broadly classified as lossy or lossless compression. Lossy compression (e.g., JPEG) typically exploits the perceptibility of the data in question, and removes unnecessary data, such that the lost data is imperceptible to the user. Alternatively, lossless compression removes statistically redundant data in order to concisely represent data. Lossless compression typically achieves a lower compression ratio and is usually more compute and memory intensive than lossy compression. However, lossy compression may be unsuitable in some scenarios where high data fidelity is required to maintain the quality of service (QoS) (e.g., in medical imaging).

3.5 Security

Since IoT devices are often deployed in open and/or potentially unsafe environments, where the devices are susceptible to malicious attacks, security applications are necessary to maintain the integrity of both the devices and the data. Furthermore, sensitive scenarios (e.g., medical diagnostics) may require security applications to prevent unauthorized access to sensitive data and functions. Implantable medical devices, such as pacemakers, implantable cardiac defibrillators, neurostimulators are especially susceptible to potentially fatal security and privacy issues (e.g., replay attacks) [Halperin 2008]. Since medical device security is still in its infancy, there still exists a wide knowledge gap with respect to the microprocessor characteristics that will support security algorithms’ execution requirements without sacrificing the devices’ functional requirements.

We highlight data encryption [Singh 2011], which is a common technique for ensuring data confidentiality, wherein an encryption algorithm is used to generate encrypted data that can only be read/used if decrypted. Data encryption applications (e.g., secure hash algorithm) are typically compute intensive and memory intensive, since encryption speed is also dependent on the memory access latency for data retrieval and storage.

3.6 Fault tolerance

Fault tolerance refers to a system’s ability to operate properly in the event of a failure of some of the system’s components. Fault tolerant applications are especially
vital since IoT devices may be deployed in harsh and unattended environments, where QoS must be maintained in potentially adverse conditions, such as cryogenic to extremely high temperatures, shock, vibration, etc. In some emerging IoT devices, such as implantable medical devices, fault tolerance could be the single most critical requirement, since faults can be potentially fatal. Thus, fault tolerance must be incorporated into such devices without accruing significant overheads.

Fault tolerance can be hardware-based, such as hardware-based RAID (redundant array of independent disks), which are storage devices that use redundancy to provide fault tolerance (we note that software-based methods do exist but typically suffer from reduced reliability). Alternatively, software-based fault tolerance involves applications and algorithms that perform operations, such as memory scrubbing, cyclic-redundancy checks, error detection and correction, etc.

4. IOT MICROARCHITECTURE DESIGN METHODOLOGY

Figure 2 illustrates our microarchitecture design methodology using a medical diagnostics use-case. The methodology comprises of three key design/analysis stages during which the applications, application functions, and execution characteristics are determined. In order to determine the right-provisioned microprocessors for the use-case, the designer must first determine the applications that will be executed on the IoT device. Determining the applications requires an analysis of the functional requirements of the IoT use-case/device. In Figure 2, for example, applications that execute on a portable ultrasound machine, in the context of edge computing, could include image capture, anomaly detection, data encryption, and data transmission.

The next step is to analyze each application to determine the application functions present in each application. Each application contains one or more functions that dictate the execution characteristics of those applications, based on the computational patterns present within each function. For example, anomaly detection involves image processing, which may be both memory and compute intensive. Data encryption

Figure 2. An illustration of our microarchitecture design methodology using a medical diagnostics use-case
Involves security algorithms, which are typically compute intensive, but have low memory intensity relative to other functions, such as image processing. Finally, based on the execution characteristics of the application functions, microprocessors and/or microprocessor configurations can be determined to satisfy the execution requirements.

### 5. IOT MICROARCHITECTURE CONFIGURATIONS

We performed an extensive survey and study of the state-of-the-art in commercial-off-the-shelf (COTS) embedded systems microprocessor architectures from several designers and manufacturers ranging from low-end microcontrollers to high-end/high-performance low-power embedded systems microprocessors. Our studies included publicly available information on these microprocessors’ configurations and conversations with researchers and engineers directly involved with microprocessor design and development in several manufacturing companies.

Based on our studies, we categorized the microprocessors in terms of several microprocessor characteristics, including number of cores, on-chip memory (e.g., cache), off-chip memory support, power consumption, number of pipeline stages, etc. Using this information, we developed a set of high-level microarchitecture configurations for IoT edge computing support. These configurations represent the range of available state-of-the-art COTS microprocessors, and provide a reference point from which future IoT microprocessors can be developed. These microprocessors reveal technology gaps that must be filled in order to design next-generation IoT microprocessors. We discuss some of these technology gaps in Section 8. While microprocessors could include central processing units (CPUs), graphics processing units (GPUs), DSPs, etc., in this study, we focus on CPUs and intend to evaluate other kinds of microprocessors for future studies.

Table 1 depicts the microarchitecture configurations, comprising of four configurations: conf1, conf2, conf3, and conf4, representing different kinds of microprocessors. We highlight specific state-of-the-art microcontroller/microprocessor examples to motivate the configurations, however, we note that these configurations are only representative and not necessarily descriptive.

| Sample CPU | Conf1 | Conf2 | Conf3 | Conf4 |
|------------|-------|-------|-------|-------|
| ARM Cortex-M4 | Intel Quark | ARM Cortex A7 | ARM Cortex A15 |
| Frequency | 48 MHz | 400 MHz | 1 GHz | 1.9 GHz |
| Number of cores | 1 | 1 | 4 | 4 |
| Pipeline stages | 3 | 5 | 8 | 15 |
| Cache | None | None | 32 KB I/D L1, 1MB L2 | 32 KB I/D L1, 2MB L2 |
| Memory | 512 KB flash | 2 GB RAM | 2 GB support | 1 TB RAM support |
| Execution | In-order | In-order | In-order | Out-of-order |

**Table 1. Microarchitecture Configurations (I=Instructions, D=Data, L1 = Level one, L2=Level two)**
8 pipeline stages, in-order execution, 32 KB L1 instruction and data caches, 1 MB level two (L2) cache, and support for 2 GB RAM.

Finally, conf4 represents high-end/high-performance embedded systems CPUs, such as the ARM Cortex-A15, and contains four cores with 1.9 GHz clock frequency, 8 pipeline stages, 32 KB L1 instruction and data caches, 2 MB L2 cache, support for 4 GB RAM, and out-of-order execution. Out-of-order execution allows instructions to execute as soon as the instruction becomes available, unlike in-order execution where instructions must execute in program order.

6. EXPERIMENTAL METHODOLOGY

This section describes our IoT benchmark suite, the performance metrics and simulators used in this study.

6.1 Benchmarks

To facilitate our studies, we created a benchmark suite based on our application classification methodology with seven kernels to represent emerging IoT edge computing applications. We used the kernels as computational basic blocks to represent the applications’ functions, which disconnects the executions from specific implementations, programming languages, and algorithms. This methodology is supported by the concept of computational dwarfs [Asanovic 2006]. Computational dwarfs represent patterns of computation at high levels of abstractions to encompass several computational methods in modern computing. Within these dwarfs, kernels are used to expose computational nuances that reveal characteristics that may not be visible at the level of the dwarfs.

Table 2 depicts our application functions, each application function’s representative benchmarks, and the benchmarks’ descriptions. For each benchmark, we used different input data sizes to model different real-world usage scenarios, and cross-compiled all benchmarks for the ARM instruction set architecture (ISA).

**matrixTrans**: Matrix transpose is a common memory-bound computation found in several applications, including sensing. The matrixTrans kernel is a naïve C-code implementation that performs a matrix transpose of a dense $n \times n$ matrix, where $n = \{128, 256, 512, 1024\}$.

**fft**: Fast Fourier Transform (FFT) is a common algorithm that rapidly computes the transmission of time or space to frequency. The fft kernel is an open source C-code implementation, available in the MiBench benchmark suite [Guthausch 2001]. To represent communication functions, fft_small and fft_large perform the FFT on polynomial functions with four pseudorandom sinusoids and 8192 samples, and eight pseudorandom sinusoids and 32768 samples, respectively.

**matrixMult**: We chose matrix multiplications to represent the complex and compute-intensive computational patterns that are common in image processing applications.

| Application function   | Benchmarks                        | Benchmark description                                      |
|------------------------|-----------------------------------|------------------------------------------------------------|
| Sensing                | matrixTrans (128, 256, 512, 1024) | Dense matrix transpose of $n \times n$ matrix              |
| Communications         | fft (small and large)             | Fast Fourier Transform (FFT)                               |
| Image processing       | matrixMult (128, 256, 512)        | Dense matrix multiplication of $n \times n$ matrix         |
| Lossy compression      | jpeg (small and large)            | Joint Photographic Experts Group (JPEG) compression        |
| Lossless compression   | lz4 (mr and xray)                 | Lossless data compression                                  |
| Security               | sha (small and large)             | Secure hash algorithm                                     |
| Fault tolerance        | crc (small and large)             | Cyclic redundancy check                                    |

Table 2. Application functions, representative benchmarks, and benchmark descriptions
The matrixMult kernel is a C-code implementation that performs matrix multiplication of two dense $n \times n$ matrices, where $n = \{128, 256, 512\}$.

jpeg: JPEG is a commonly used lossy compression method that typically achieves 10:1 compression with little perceptible loss in image quality. We used the small and large input data available in MiBench, where jpeg_small and jpeg_large perform JPEG compressions on images of a 7 KB image with $256 \times 256$ resolution and a 20 KB image with $512 \times 512$ resolution, respectively.

lz4: LZ4 is a relatively recent open source lossless data compression algorithm that focuses on compression speed, thus making the algorithm attractive for real-time applications on the IoT. We used an open source 10 MB medical magnetic resonance image (MRI) and 8 MB medical x-ray image [Silesa Corpus 2015] as input images for lz4_mr and lz4_xray, respectively.

sha: The Secure Hash Algorithm was designed by the United States National Security Agency, and is commonly used for generating digital signatures and securely exchanging cryptographic keys. The sha kernel is an open source C code implementation that produces a 160-bit message given an input data. We used the 300 KB and 3 MB input data from MiBench for sha_small and sha_large, respectively.

crc: Cyclic redundancy check is a commonly used error-detecting code for detecting errors in data transmission. The crc kernel is an open source C code implementation that performs a 32-bit CRC on a 1 MB and 25 MB input file for crc_small and crc_large respectively. We used the input files available in MiBench.

6.2 Performance Metrics

In this subsection, we define the performance metrics used to quantitatively compare the microarchitecture configurations.

Execution time: The execution time, $t$ is the time required to execute an application from start to finish, given as:

$$ t = \frac{1}{freq} \times cyc_{total} $$

where $freq$ is the processor’s clock frequency and $cyc_{total}$ is the total number of cycles required to execute the application.

Energy: The energy, $E$ is the product of the power consumed by the processor, $P_{total}$ and the application’s execution time, given as:

$$ E = P_{total} \times t $$

where $P_{total} = P_{leakage} + P_{runtime\_dynamic}$

Performance: We define the performance in terms of the number of giga (billion) operations per second (GOPS), calculated as:

$$ Performance\ (GOPS) = \left( freq \times \frac{1}{CPU} \right) / 1e9 $$

Efficiency: We define the efficiency in terms of the performance per watt (GOPS/W), i.e., the attainable performance while taking into account the power consumed.

$$ Efficiency\ (GOPS/W) = \frac{Performance}{P_{total}}. $$

6.3 Simulators

To evaluate the applicability of our microarchitecture configurations to the IoT, we modeled the different configurations using the GEM5 simulator [Binkert 2011], and generated execution statistics while running several benchmarks on the configurations as shown in Table 1. We used the McPAT simulator [Li 2009] to generate leakage,
dynamic power, and area values for the different configurations, and used Perl scripts to drive our simulations.

7. ANALYSIS OF MICROARCHITECTURE CONFIGURATIONS

In this section, we present simulation results for execution time, energy, performance, and performance per watt on the microarchitecture configurations listed in Table 1. We also perform sensitivity analysis with respect to varying application data sizes, various microarchitectural characteristics, and evaluate the impacts of idle energy and leakage power reduction.

7.1 Execution characteristics and sensitivity to data sizes

To evaluate the execution characteristics of the different benchmarks, we used the percentage of memory references per instruction (MPI) and the instructions per cycle (IPC) to provide insight into the benchmarks’ memory and compute intensities, respectively. Note that IPC can also provide an indication of a benchmark’s memory intensity (e.g., a low IPC could indicate long memory access times due to accesses to lower level memory, and hence, a memory intensive benchmark).

First, we evaluated the MPI and IPC on con4. While the MPI is microarchitecture-independent (i.e., the MPI remains the same across different microarchitectures), the IPC is microarchitecture-dependent. However, we observed that the IPC also remained relatively stable for different data sizes across all of the configurations. The execution characteristics (MPI and IPC) and sensitivity to different data sizes provides insights into the right provisioning of memory (cache) sizes and/or clock frequencies in order to satisfy the execution requirements.

![Figure 3. (a) Memory references per instruction (MPI) and (b) instructions per cycle (IPC) of the benchmarks with different data sizes](image-url)
Figure 3 (a) and (b) depict the MPI and IPC for all of the benchmarks for different input data sizes. Figure 3 (a) shows that the memory intensity for the different benchmarks remained stable regardless of the data size. *matrixTrans* was the most memory intensive benchmark with an MPI of 52%, since most of the computations were performed in memory. Similarly, *sha*, *cjpeg* and *lz4* were also memory intensive benchmarks with MPIs of up to 49%, while *fft* was the least memory intensive with an MPI of 21%.

Figure 3 (b) shows that the IPCs for different benchmarks were also relatively stable for different data sizes, since the working set sizes for these benchmarks remained stable, except for *matrixTrans* and *matrixMult*, which had variable working set sizes with different data sizes. For example, *matrixTrans*’ IPC reduced by 32% and 60% when the data size increased from *matrixTrans_128* to *matrixTrans_256* and from *matrixTrans_256* to *matrixTrans_512*, respectively. The IPC increased because the working set size increased as the data size increased. Thus, there were more processor stalls due to the increased memory activity. However, the working set size remained stable from *matrixTrans_512* to *matrixTrans_1024*, thus, the IPC also remained stable.

### 7.2 Execution time, energy, performance, and efficiency

Figure 4 (a) and (b) depict the execution time and energy of *conf1*, *conf2*, and *conf3* normalized to *conf4* for all of the benchmarks. We used *conf4* as the base configuration for comparison since this configuration was the biggest of our microarchitecture configurations. Figure 4 (a) shows that *conf1*, *conf2*, and *conf3* increased the average execution time by 202x, 23x, and 9x, respectively, for all of the benchmarks. These results show that *conf4* outperforms the other configurations when considering latency. Similarly, Figure 4 (b) shows that *conf1*, *conf2*, and *conf3* increased the energy consumption by 35x, 4.6x, and 4.7x. *Conf4’s* low energy consumption compared to the other configurations was due to the significant reduction in execution time, while the smaller configurations resulted in considerably longer execution times than *conf4*. The graphs do not show *conf1* results for some benchmarks because *conf1’s* memory was too small for the working set size of those benchmarks, and thus the those benchmarks
could not be executed on conf1. Since conf1 represents current MCUs that are used on the IoT, our results indicate that these current MCUs are not sufficiently equipped for all edge computing requirements.

Figure 5 (a) and (b) depict the performance and efficiency of conf1, conf2, and conf3 normalized to conf4 for all of the benchmarks. Results reveal that conf1, conf2, and conf3 degraded the performance by 171x, 17x, and 8x, respectively. Compared to conf4, conf1 degraded the efficiency by 33x, while conf2 and conf3 degraded the efficiency by 4x. These results reveal the significant improvements achieved by using the larger configurations. In a system that is not energy constrained (e.g., an IoT device that is consistently connected to a power source) or in real-time systems, where minimizing latency is the goal, conf4 provides the best performance for the system.

7.3 Sensitivity to various microarchitectural characteristics

To identify the most impactful microarchitectural characteristics on system execution time, energy, performance, and efficiency, we evaluated conf4 with a 1 GHz clock frequency, in-order execution, and a 16 KB cache size. For each of these evaluated configurations, all of the other configurations were held constant to isolate the impact of the evaluated configurations. For brevity, we only show results for a subset of the benchmarks’ input data sizes, however, all of the benchmarks are included in the averages.

Figure 6 (a) and (b) depict the execution time, energy, performance, and efficiency of conf4 with a 1 GHz clock frequency normalized to conf4 with a 1.9 GHz clock frequency. Figure 6 (a) illustrates the significant impact of the clock frequency on execution time and energy consumption. On average over all of the benchmarks, reducing the clock frequency to 1 GHz increased the execution time and energy by 75% and 41%, respectively. However, for matrixTrans, reducing the clock frequency to 1 GHz did not change the execution time and reduced the energy by 4%. Since matrixTrans was the most memory intensive benchmark and spent more execution time in memory activities, reducing the clock frequency had little impact on matrixTrans than on the
other benchmarks. Figure 6 (b) reveals that reducing the clock frequency reduced the average performance and efficiency by 40% and 27%, respectively. Similarly to the execution time and energy results, for matrixTrans, the performance did not change and the efficiency increased by 4% since matrixTrans's performance was more dependent on the memory than on the clock frequency. These results show the significant impact that the frequency has on edge computing for IoT applications.

Figure 7 (a) and (b) depict the execution time, energy, performance, and efficiency of in-order execution normalized to conf4 (out-of-order) execution. Figure 7 (a) shows that in-order execution increased the average execution time and energy by 4.8x and 2.9x, respectively, and by as high as 9x for sha_large, which is a highly compute intensive and memory intensive benchmark. The results reveal that out-of-order execution provides greater advantages over in-order execution for applications that are compute intensive, however, the impact is reduced for memory intensive applications. Figure 7 (b) shows that in-order execution reduced the average performance and efficiency by 75% and 63%, respectively. Similarly to the execution time and energy, the performance degradation was more significant for the more compute intensive benchmarks, such as sha_large.
Figure 8 (a) and (b) depict the execution time, energy, performance, and efficiency of conf4 when the cache size was reduced to 16 KB normalized to conf4 with the 32 KB cache. Unlike with the clock frequency and execution order, reducing the cache size did not significantly impact the overall results. Figure 8 (a) shows that the 16 KB cache only increased the average execution time by 4%, with increases as high as 18% for lz4_mr. The execution time increased for lz4_mr because the 16 KB cache was not large enough to hold lz4_mr’s working set size, thus incurring cache misses and requiring the data to be fetched from main memory. However, reducing the cache size did not negatively impact the execution time for most of the applications. The 16 KB cache reduced the average energy consumption by 4%, but increased lz4_mr’s energy consumption by 3% due to the additional cache misses incurred by the 16 KB cache. Similarly, Figure 8 (b) shows that the 16 KB cache degraded the average performance by 3% and improved the average efficiency by 5%. For applications with large working set sizes, such as lossless (lz4_mr) and lossy compression (cjpeg_large), the 32 KB cache was more appropriate. For all other applications, the 16 KB cache size was sufficient.

### 7.4 Impact of idle energy and power optimization

Since most IoT devices have a small form factor, their microprocessors will be more susceptible to leakage power. The CMOS device scaling trend allows for a reduction in supply voltage for small microprocessors. However, as the supply voltage is reduced, the threshold voltage must also be reduced to maintain the desired performance levels. This threshold voltage reduction results in an exponential increase in the subthreshold leakage current, thus leading to a significant increase in leakage power/idle energy. To design right-provisioned microprocessor architectures for the IoT, idle energy must also be carefully considered and minimized, in order to minimize overall energy consumption.

To illustrate the impact of the idle energy on overall energy consumption, we simulated various application execution scenarios for the shortest and longest running benchmarks (matrixTrans_128 and crc_large). We calculated the total energy consumed as the sum of the energy consumed during application execution and the idle energy, where the idle energy is the product of the leakage power and the idle time. We assumed power gating [Hu 2004] for power optimization in our evaluations, where the leakage power is reduced by 95%.

Power gating is a technique used to reduce a circuit’s leakage power consumption by shutting off blocks of the circuit that are not being used. To represent a real-world scenario, we experimented with periodic times and random application execution time intervals, and observed that the results were independent of the periodicity or

![Figure 8](image.png)

Figure 8. (a) Execution time and energy (b) performance and efficiency of 16 KB cache normalized to conf4 (32 KB cache)
randomness of the application executions. Thus, we present the results for both periodic and random execution time intervals together in this subsection.

Figure 9 (a) and (b) depict the total energy consumed by conf1, conf2, and conf3 normalized to conf4 for matrixTrans and crc_large, representing low and high duty cycle applications, respectively, without power gating and with power gating. Figure 9 (a) shows that without power gating, conf1 consumed the lowest amount of energy for both the low and high duty cycle benchmarks. Even though conf3 and conf4 executed the applications fastest and accounted for the least dynamic energy consumption, both configurations had high leakage power, thus negating the energy savings from the short execution times. Figure 9 (b) shows similar results for the matrixTrans with power gating. Since matrixTrans is a short benchmark that executed relatively fast on all of the configurations, there was not enough difference in the configurations’ idle times for power gating to provide any significant benefit. However, for crc_large, conf1 consumed the most overall energy with power gating, while conf2 consumed the least energy. Due to the length of the application, conf1 spent most of the time executing the application, while conf2, conf3, and conf4 were able to go into the idle mode much faster due to faster execution times. Conf2 provided the optimal balance, across all of the configurations, between the time spent executing the application and the time spent idling. Thus, these results reveal that the benefits of power gating are dependent on the application’s duty cycle. Applications executing on configurations that have low duty cycles have a higher potential of benefiting from power gating.

To further evaluate the impact of idle energy, we considered a scenario in which multiple applications were randomly executed periodically or at random time intervals. Figure 10 depicts the total energy consumed by conf2 and conf3 normalized to conf4 for a random selection of six benchmarks. The figure does not show results for conf1 because conf1 could not execute most of these benchmarks due to insufficient memory. Without power gating, conf2 consumed the lowest energy on average, showing that this configuration provided a good balance between idle time and leakage power. However,
with power gating, conf4 consumed the lowest energy on average, since this configuration provided much faster execution, enabling power gating to provide significant energy savings due to the leakage power reduction. Therefore, these results show that an application's duty cycle should be considered when selecting configurations for execution. Larger configurations (e.g., conf3 or conf4) that significantly reduce the duty cycle compared to smaller configurations provide greater power optimization benefits. However, when only short executions are required and an application's duty cycle is similar across the different configurations, and/or power optimization is not available (i.e., leakage power is high), the smaller configuration devices would consume less energy overall, since these configurations would typically have less leakage power than the larger configurations.

8. MICROPROCESSOR OPTIMIZATIONS AND KEY TECHNOLOGY GAPS

One of the major observations from our studies is that different IoT applications have different runtime resource requirements. With the growth of the IoT and the current trend of IoT applications, we envision that this variability in runtime resource requirements will increase even further with next-generation IoT applications. Therefore, these variable runtime resource requirements necessitate adaptable/configurable microprocessor architectures whose configurations can be autonomously specialized to different applications in order to achieve optimal execution, especially in terms of energy efficiency.

Based on the insights from our studies, we highlight a few potential optimization techniques for achieving adaptable IoT device microprocessors. The goal of these optimizations is to achieve an optimization goal (e.g., energy efficient execution) without significant degradation to other optimization goals (e.g., performance, area, deadlines, etc.). Thus, we discuss the tradeoffs of the different optimizations to provide designers with insights on the appropriate optimizations for their specific design needs.

8.1 Dynamic Voltage and Frequency Scaling (DVFS)

Dynamic voltage and frequency scaling (DVFS) [Firouzi 2010; Schmitz 2002; Shin 2000] is an optimization technique that allows for variable voltage and/or frequency levels during an application's execution. Since dynamic power is directly correlated with the voltage and frequency, reducing the frequency also reduces the required voltage for stable operation, thus reducing the power consumption. The major challenges of DVFS are the potential overheads from incorporating DVFS in a microprocessor and the performance degradation from reducing the operating frequency/voltage in order to save power/energy.
In order to address these challenges much work is still required, in addition to the already existent work (e.g., [Choi 2004; Hua 2003]), to develop techniques that will enable efficient DVFS implementation in IoT microprocessors. Different applications/application phases require different frequencies for optimal execution, which necessitates efficient algorithms and techniques to dynamically determine the best operating frequency for different applications/phases. These algorithms must be low-overhead, efficient, computationally simple, and achieve a good energy-performance tradeoff that satisfy the optimization goals of the specific use-case. For example, some applications may have stringent deadline constraints while other applications in the same system may have more relaxed deadlines. In addition, since incorporating DVFS introduces area and power overheads from the voltage regulators and transitions, the optimal number of supported frequency/voltage levels for IoT microprocessors must be determined in order to minimize these overheads.

8.2 Configurable/Adaptable Caches

Since emerging IoT applications will increase in memory and compute intensity, IoT microprocessors must be equipped with more advanced memory hierarchies to take advantage of the spatial and temporal locality of the IoT applications. Due to the memory hierarchy’s large impact on system performance and energy consumption, much emphasis must be placed on efficient caching techniques for IoT microprocessors.

Previous work has shown that specializing the cache configurations to different application or phase memory requirements can reduce the memory hierarchy’s energy consumption by up to 62% [Gordon-Ross 2005]. In addition, our studies revealed that the cache is one of the more easily over-provisioned resources in an IoT microprocessor, resulting in high energy consumption with no performance benefits. The energy consumption can be quantifiably reduced, without any performance degradation, by dynamically changing the cache configurations (e.g., reducing the cache size). Thus, a prominent optimization for IoT microprocessors is dynamically configurable cache architectures that allow the cache’s parameter values to be specified/changed during runtime.

Three major challenges must be addressed in order to enable dynamically configurable caches for IoT microprocessors: augmenting caches for configurability, cache tuning algorithms/heuristics, and cache tuners. In order to maximize the benefits of configurable caches, the required hardware optimizations to enable configurability must accrue minimal overhead. For example, a potential technique for enabling cache configurability uses bit-width configuration registers that allow a cache’s banks to be shutdown to configure the cache size, or concatenated to configure the cache associativity [Zhang 2003].

However, for optimal execution, the best configurations that achieve optimization goals and satisfy design constraints for different applications must be dynamically determined. Cache tuning determines the optimal cache configurations that matches an application’s runtime behavior. The cache tuning algorithm/heuristic can result in time and energy overheads, since the processor must stall during the tuning process. Thus, much previous work (e.g., [Adegbija 2014; Gordon-Ross 2005; Zhang 2003]) have proposed different algorithms/heuristics for cache tuning to minimize the potential of overhead and optimize the cache tuning benefits. These works offer a valuable foundation for IoT microprocessors. The intrinsic characteristics of the IoT necessitate further studies and development of innovative cache tuning techniques for IoT microprocessors that are low-overhead, robust, and versatile for the variety of applications that will execute on these microprocessors.

To orchestrate the cache tuning process, hardware and/or software cache tuners employ cache tuning algorithms/heuristics to determine the best cache configurations to meet design constraints. However, the tuner could impose significant power, area,
and/or performance overheads while exploring the configuration design space [Adegbija 2014]. Thus, to maximize the benefits of configurable caches in IoT microprocessors, novel cache tuners must be designed such that they constitute minimal overhead and effectively implement the cache tuning algorithms.

### 8.3 Heterogeneous Architectures

Heterogeneous architectures allow a coarse-grained specialization of system resources to the requirements of executing applications by equipping a microprocessor with different kinds of cores and/or different core configurations. The different cores execute the same instruction set, but have different capabilities and performance levels. Thus, at runtime, the system software evaluates the resource requirements of applications or application phases and determines the core that best satisfies the optimization goals for the executing applications. One of the major advantages of heterogeneous architectures for IoT microprocessors, from a design perspective, is that existing cores (e.g., CPUs, DSPs, GPUs, etc.) can be reused in the implementation of heterogeneous microprocessors, and this allows previous design and verification efforts to be amortized. However, unlike configurable architectures, heterogeneous architectures offer a much smaller design space, which necessitates greater design time effort in determining the best cores/core configurations that will satisfy the application requirements. In addition, in a system with a large number of applications, heterogeneous cores may have a lower optimization potential than configurable cores, since there are fewer configurations to choose from in heterogeneous cores.

Much previous research efforts have targeted heterogeneous cores in general purpose computers, embedded systems, etc., but their applicability to IoT microprocessors have yet to be explicitly determined. Two major challenges that must be addressed in designing heterogeneous microprocessors for the IoT are the number and choice of cores, and scheduling of applications to the appropriate cores. In order to maximize the optimization potential, designers must expend a considerable amount of effort to determine the best cores or configurations to incorporate into the microprocessor. To provide an effective platform that satisfies the execution requirements of a wide variety of application characteristics, the selected cores must cater to a wide range of computational complexities and performance requirements. This effort would require a priori knowledge and analysis of the applications/application domains that will execute on the microprocessor and extensive analysis of potential core configurations.

Given the application execution requirements, the appropriate core on which to execute/schedule the application must also be determined either statically or dynamically. Static scheduling suffices when the applications are known a priori. However, when the applications are unknown, dynamic scheduling evaluates application characteristics at runtime and schedules the applications to the appropriate cores. Much research is needed to develop low-overhead, computationally simple, and accurate scheduling techniques, for IoT microprocessors, that will achieve optimization goals and satisfy the microprocessors’ resource constraints.

### 9. CONCLUSIONS AND FUTURE RESEARCH

We provided a detailed study of microarchitectural characteristics that will enable and support the growth of the Internet of Things (IoT). The emergence and growth of the Internet of Things (IoT) is expected to transform life, business, and the global economy. The IoT’s scale and rapid proliferation will generate massive amounts of data that will result in communication bandwidth bottlenecks, and latency and energy overheads. Edge computing significantly reduces these overheads by equipping IoT devices with right-provisioned microprocessors and algorithms that can perform computations on the edge nodes to interpret, visualize, and use data.
As a foundation for designing IoT microprocessors to support emerging IoT applications, we presented a high-level holistic microprocessor design methodology that considers the applications' basic functions, and microarchitectures that support these functions' execution requirements. To tractably represent the vast IoT application space, we propose an application classification methodology consisting of a set of application functions and benchmarks that represent the basic computational patterns of current and emerging IoT applications. Using our microprocessor design methodology, we comprehensively studied state-of-the-art low-power microprocessors' microarchitectural characteristics and evaluated the microprocessors' applicability to IoT edge computing. We analyzed these microarchitectural characteristics with respect to various performance metrics and formulated insights that serve as a foundation for further analysis and design of IoT microprocessors. Since edge computing in the IoT is a burgeoning area of research, the goal of this work is to provide a foundation for further research into application requirements and microprocessor optimizations for next-generation IoT devices.

Our analysis showed that much foresight is required for designing future IoT microprocessors. We found that several current IoT-targeted microprocessors are not sufficient for edge computing, especially due to these devices' low memory capabilities (cache and main memory). In order to support edge computing, emerging IoT devices must be equipped with additional compute and memory capabilities. We also illustrated the need to design IoT microprocessors that prioritize optimization of the clock frequency and program execution order, due to these characteristics' large impacts on performance and energy consumption.

We also found that executing applications' duty cycles must be considered when developing optimizations for IoT microprocessors. In the presence of optimizations that reduce leakage power, such as power gating, large configurations that may increase the dynamic power but reduce the duty cycle are preferred. However, where leakage power is high (e.g., in a system without power gating), smaller configurations that reduce the dynamic power are preferred. Furthermore, our analysis revealed that optimizations that enable adaptability must be emphasized, due to the variable nature of emerging IoT applications' runtime execution characteristics.

Our future work includes validating the analysis presented in this work in actual real-world use-cases. We intend to prototype IoT edge computing in a medical diagnosis use-case, where real-time diagnosis must be made based on information gathered from connected medical devices. Medical diagnosis represents a data-rich use-case, involving several high-demand algorithms, and we intend to evaluate how these applications can be supported using the methodology presented in this paper. In addition, we plan to extend our studies and analysis to more complex microprocessors and systems including other IoT device components, such as input/output (I/O) bandwidth, secondary storage, etc., and evaluate how these components impact IoT edge computing. We also plan to study the impact of additional optimizations for low-power devices, and propose and prototype new architecture designs for IoT edge computing based on our analysis.

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