The NOνA Timing System: A system for synchronizing a long baseline neutrino experiment

A Norman, R Kwarciany, G Deuerling, N Wilcer
Fermi National Accelerator Laboratory, P.O. Box 500 Batavia IL 60510, USA
E-mail: anorman@fnal.gov

Abstract. The NOνA experiment is designed to measure key parameters in neutrino physics related to the neutrino mass hierarchy and the asymmetry between matter and anti-matter. To make these measurements the NOνA experiment must correlate the extraction of beam to the NuMI target with individual hits in both a near detector and a far detector located 810 km from Fermilab. Precisely correlating hits across these detectors and reconstructing particle trajectories require that all of the readout electronics be precisely synchronized to an absolute wall time with a channel to channel variation less than 15.6 ns. The NOνA Timing Distribution System accomplishes this through an integration of commercial GPS receiver technology and custom electronics. This paper describes the timing system, its component hardware and the synchronization method that is employed by it.

1. Introduction
The NOνA experiment is a new long baseline neutrino experiment designed to measure the oscillation probability for $\nu_\mu \rightarrow \nu_e$ and $\bar{\nu}_\mu \rightarrow \bar{\nu}_e$ transitions[1]. In order to perform these measurements the NOνA experiment will build a massive 15 kT far detector and a smaller 300 ton near detector. The two detectors have been specifically optimized to detect both $\nu_e$ interactions which are characterized by an electro-magnetic show, as well as $\nu_\mu$ interactions which are characterized by the vertex formed between a well defined muon track and a visible energy plume that is the signature of a nuclear recoil. The NOνA experiment will correlate these interactions with beam spill information from the Fermilab 120 GeV NuMI (Neutrinos at the Main Injector) beam. This correlation is made possible through the use of a sophisticated timing and synchronization system that is deployed to each of the detectors sites and to the accelerator complex at Fermilab. In this paper we discuss this system, its design, operational parameters and the real performance of the system that was demonstrated during it’s operation on the NOνA Integration Prototype Near Detector from December 2010 through May 2012.

2. NOνA Timing System
The NOνA timing system relies on a custom designed set of timing modules that provide the clock signals that are distributed to the front end readout electronics and also a set of associated timing and control signals lines that are used to perform synchronization of the electronics. The timing system establishes a master time specification based on a GPS satellite lock that is used to synchronized, sort and correlate hits within the NOνA detectors and then used to associate those hits with the beam spill events that occur at the Fermilab accelerator complex.
Figure 1. The NOνA far detector is a 15 kT calorimeter/range stack that uses an X/Y planar geometry to measure particle trajectories in two separate views. The detector is immense in size with a 15.6 m square cross section and a length of 67 m. The total detector volume is over 16000 m$^3$. The NOνA near detector has a 1/4 scale cross section and total detector mass of approximately 300 tons.

The timing system is required to ensure that the more than 368640 individual readout cells of the near and far detectors can be aligned in time to provide high resolution tracking for particles passing through the detector and also so that the exact times at which protons were extracted to the neutrino production targets can be projected to the far detector site 810 km away to predict the time window when the neutrino passed through the near and far detectors. Because the beam spill window is so narrow, even small errors in these timing correlations have the potential to misalign the neutrino beam so that their interactions in the detector are completely missed, or to incorrectly synchronize the readout within the detectors and cause events and tracks to be incorrectly reconstructed.

3. Timing Distribution and Topology
The NOνA detectors are instrumented with frontend boards attached to the top and side faces of the detector. These boards that are mated to avalanche photodiode detectors which readout groupings of 32 detector cells. The frontend boards are in turn connected to a “Data Concentrator Module” (DCM) which takes the data streams from 64 individual front end boards (2048 detector cells) and correlates and sorts the data into well defined time ordered data packets for transmission to a large farm of computers for further processing. This readout topology shown in Fig. 4, defines 180 independent geographically distinct readout regions along the top and side of the far detector which must be both internally synchronized (all frontend boards in a region) as well as globally synchronized with each other in order to obtain the proper event and track reconstruction.
In order to synchronized and drive the clocks for the 180 readout regions and more than 368000 detector cells, a hierarchical arrangement of custom timing hardware has been developed which is designed to create a tree topology that is capable of both generating and repeating commands and clock signals along each of its branches. The timing system topology used for the NOνA far detector is shown schematically in Fig. 5 which shows the arrangement of timing system masters, slaves, data concentrators (DCMs) and frontend boards (FEBs) that are used to establish the timing chains.

At the top of the tree topology of each timing chain, a single master timing distribution unit (MTDU) is connected to an external GPS antenna which is mounted on the roof of the detector building. The antenna is installed so that it has an unobstructed view of the sky and so that the GPS receiver mounted inside of the MTDU is capable of locking onto the signals from 12 satellites in the GPS constellation. In addition the MTDU is connected either to a set of accelerator input lines, if the unit is located at Fermilab, or a reference pulser system, if the system is located at a remote detector site. These inputs are used to timestamp the accelerator or reference pulse signals and provide beam spill and system diagnostics.

The MTDUs shown in Fig. 6 are installed at the far detector site in the NOνA computing center, which is adjacent to the detector hall. The distance between the computing center and the upstream most block of the detector is long enough that the copper timing lines used in the rest of the timing chain can not be used. Instead a single mode optical fiber link is used to connect the MTDU with the first slave TDU (STDU) in the detector hall.

A total of 15 STDUs form the “backbone” of the far detector and extend down the full length of the detector along the upper most catwalk in the detector hall. Each STDU is connected in a daisy-chain fashion to the adjacent TDUs by a copper timing cable that provide 4 LVDS lines that carry the master clock, command channel, SYNC and SYNC return signals. At the end of the slave TDU backbone a loopback connector is installed to permit delay calibrations in the
Figure 4. The NOνA detectors are instrumented through a series of independent readout regions, where a single Data Concentrator Module (DCM) aggregates data from a total of 2048 detector cells in a single X or Y-view. The photo shows the instrumentation of the NOνA prototype near detector with frontend boards in golden colored shielding boxes running down the length of the detector and data concentrator modules paired with low voltage power distribution fan-outs defining the readout regions along the surface of the detector.

A STDU is installed for each kiloton of detector mass and is designed to drive the timing for 12 DCM readout regions split into two separate branches of 6 DCMs each. The DCM branches that are driven by a given STDU are split so that one corresponds to the top (X-view) of the detector and one corresponds to the side (Y-view) of the detector. The DCMs are connected in the same daisy chain manner as the slave TDUs are, with the last DCM in each of these branches having a loopback connector installed in its timing output port.

The front end boards are connected to the DCMs by copper data links which carry the same master clock, control channel and SYNC lines, but replace the SYNC return echo line with the high speed serial data stream line that carries the hit data from the frontend boards to the DCMs. The lack of a SYNC return echo line prevents the time of flight along the DCM/FEB link from being calculated individually for each link and instead all DCM/FEB links are required to be the exact same length and are tested during the quality control and installation procedure to have the same propagation delay and signal characteristics. Links falling outside of this specification are rejected. This permits the synchronization procedure discussed in section 9 to operate correctly and induce minimal channel to channel variation in the timestamps of the data.
Figure 5. The timing system uses a master timing distribution unit connected to a backbone of 15 slave Timing Distribution Units (TDUs) to hierarchically fan out timing information to 180 data concentrator modules (DCMs) arranged in six unit chains across the far detector. Each DCMs then in turn fans out the timing information to a set of 64 front end boards which provide the readout and digitization of the detector cells. The system includes a loopback system for performing calibration along each leg of the timing chain and for determining device to device propagation delays.

Figure 6. The master TDUs provide front panel connections for time stamping signals from the Fermilab accelerator as well as additional inputs which support timing stamping of arbitrary 50Ω terminated TTL signals. The units provide small LCD displays which provide diagnostic information on the condition of the GPS receiver system, network and general timing information.

4. GPS Source
The heart of the NOνA timing system utilizes a high precision global positioning system (GPS) receiver which is used to establish a location and time fix lock with between 3 and 12 satellites. The receiver is a commercial unit and uses the standard GPS protocol and time specifications. When the receiver is correctly locked to the signals from a GPS constellation, it produces a stable 10 MHz reference clock and a 1 pps reference pulse on the LVDs output lines. The references pulse on the 1 pps line are aligned to the GPS time specification’s 1 second boundaries. The Conner-Winfield FTS-125-C00 also provides a National Marine Electronics Association (NMEA) standard data stream which includes additional diagnostic information regarding the number
of satellites being utilized by the receiver, their signal strengths and the type of lock that the receiver his able to establish and maintain and any error conditions the receiver has encountered.

The GPS receiver unit is mated, as shown in Fig 7, to a master timing distribution unit board which uses an ARM micro processor and a Altera FPGA to interface with the GPS receiver over the data link and reference clock lines, as well as provide limited control, configuration and reset of the receiver.

Figure 7. The master timing distribution units makes a Conner-Winfield high precision oven-controlled GPS receiver unit with an Altera FPGA running the NO\nuA timing/sync firmware. The master TDUs uses an ARM microprocessor for controlling the FPGA and GPS receiver. A PowerPC 8347 based single board computer is mounted as a daughter board on the main TDU board to provide a Linux platform on which to access the TDU FPGA and run data acquisition software.

The NMEA data stream is fully decoded by the ARM processor board and the information is made available to the end user via a small LCD display unit that is mounted on the front of the TDU, and also through a set of data registers which can be accessed through an ethernet interface.

5. NO\nuA Time Spec
The timing system uses the GPS receiver information to establish a custom time spec which is tailored to the needs of the detector readout system. The NO\nuA time specification defines a universal high resolution timestamp which counts the number of 64 MHz clock cycles that have occurred since the start of the “NO\nuA Epoch” defined as 00:00:00 January 1, 2010 GMT. The timestamp is limited to 56bits divided into a 32bit low word which records the full 64 MHz resolution timestamp of the last 67.1 s and a 24bit high word which records the lower resolution portion of the time stamp. The combined high/low timestamp has a 35.7 yr validity more than sufficient for covering the planned experimental runs of the NO\nuA experiment with a LSB of 15.6 ns.

In addition the NO\nuA timestamp has been design to be used under conditions where the base clock of the different detectors is variable based on the version of the front end hardware that
is being run. An example of this flexibility has been demonstrated by the front end electronics have been used on the integration prototype detector. These electronics were used at Fermilab starting in 2010 and will be used on the Ash River detector starting in 2012. They operate under a 16 MHz base digitization clock whose sampling cycles are aligned to the NO\(\nu\)A time specification and have an effective LSB of 62.5 ns (i.e. the time stamps of the digitizations are forced to fall on the 16MHz boundary such that the lowest two bits of the time stamp are always zero when time stamping a detector hit.) In contrast the NO\(\nu\)A near detector electronics that will go into service in 2013 will uses a different design capable of support a higher resolution 64MHz sampling clock to improve rejection of pileup in the detector. Detector hits that are time stamped with this board use the full resolution of the NO\(\nu\)A time specification and have a LSB of 15.6 ns.

The NO\(\nu\)A time specification has also been designed to be flexible with respect to future electronics and sampling frequencies. The 56bit base time stamp can be extended to support readout frequencies of 128MHz up to 1.024GHz through the use of an additional high word byte which serves as a base frequency tag indicator for the rest of time stamp. Standard frequencies of 128MHz, 256MHz, 512MHz, 1.024GHz retain the full time range of the normal NO\(\nu\)A clock and maintain both binary compatibility with the defined NO\(\nu\)A data formats and backwards compatibility with data taken at lower resolutions (i.e. data taken with a 128MHz base clock can be converted directly into either 64MHz or 16MHz time base for comparison with older readout data.) Non-standard time bases in the range of 1-255MHz, such as a proposed 20 and 24MHz readout modes, are supported and are binary compatible with the NO\(\nu\)A readout format, but require additional time base corrections to be directly compared with other data.

6. Accelerator Event Timestamps

The NO\(\nu\)A timing system is designed to accept inputs from the Fermilab accelerator complex which are decoded and time stamped. These time stamped accelerator signals are then used to provide the information that is used to form the NO\(\nu\)A beam spill triggers. The NO\(\nu\)A timing system is able to obtain higher timing resolution of these events than is otherwise available through the ACNET system that is used to publish and log data within the rest of the Accelerator system. This higher timing resolution is required to ensure accurate identification of the 10\(\mu\)s window associated with a NuMI beam spill, or the 1\(\mu\)s windows associated with extraction from the booster complex.

The timing system that was deployed for the integration prototype near detector featured full decoding and time stamping of the accelerator signals at a resolution of 16MHz. The system was designed to take inputs from the Fermilab beam-synchronous (BSYNC) clock system, as well as the lower precision Tevatron Clock (TCLK) [2] accelerator time line clocks. The timing system was capable of decoding both the BSYNC and TCLK lines simultaneously, giving additional information for accelerator events, like the NuMI extraction kicker signals, which are broadcast on both lines.

The timing system used logic in an Altera FPGA to deterministically decode and timestamp the accelerator clock lines, then filter the resulting data stream to publish the accelerator events of interest to a fixed length queue which could be read from either the ARM microprocessor board or from an attached powerpc single-board computer. The depth of the queue for the NO\(\nu\)A timing system was optimized to permit simultaneous acquisition of the NuMI accelerator signals (BSYNC signal MIB$74 and TCLK signal $A9) at 0.5-1.2 Hz, the booster permits and extraction signals (TCLK signals $1D and $1F) at 15Hz and reference and calibration signals published by the accelerator at 1Hz or slower. Under normal operation, if a new accelerator signal event is decoded while the queue is full the oldest event in the queue is dropped and the new event pushed onto the back of the queue. This operation prevents stale data from accumulating in the event queue during periods when no external process on the PowerPC is
actively draining the queue and broadcasting spill triggers to the DAQ system.

Tests of the timing system were performed to tune the queue depths to ensure that under standard operation of the NOνA beam spill server (the software that drains the queue and issues the beam spill triggers to the DAQ system) no decoded accelerator signals of interest would be dropped due to latencies in accessing the spill history or due to overlapping bursts of activity on the accelerator input lines. The queue depth was optimized to a depth of 256 entries to permit on average 16 s of accelerator data to be accumulated before the oldest data was expired and dropped.

The accelerator decoding functionality of the timing system tested over the 2011/2012 experimental run of the prototype detector by using a series of four separate timing system master units located in different locations at Fermilab. Two of the units were installed at the MINOS service building which is located next to the NOνA prototype detector hall. These units were connected to GPS antennas on the top of the MINOS building and to accelerator systems inside the building. A similar pair of timing units were installed at the Feynman computing center where an identical pair of antenna and a bank of accelerator clock lines were installed. The four systems were then independently initialized and configured to decode the NuMI, Booster and Calibration accelerator events. These events were logged by each system and the resulting event lists and times were compared across the ensemble of data sets to determine errors in decoding, time stamping, dropping of data due to overruns of the accelerator event queue, as well as other system instabilities such as drift of the system clocks due to GPS lock errors. The timing system ensemble was able to detect a systematic system-to-system variation in the time stamping of events of ±1 clock tick under normal operation and GPS lock of the system, and a much larger variation under initialization circumstances where the timing system initialized prior to the GPS receiver establishing a satellite lock. The small variation was attributed an ambiguity in the initial phase of oscillator that drives the timing system between any two independent units prior to the establishment of GPS lock. This can cause the system to lock onto the GPS reference pulses with up to a half clock cycle variation. This unit to unit variation across timing system resets resulted in an overall 15.6 ns uncertainty in the time stamps of the beam spills at the prototype detector.

The production timing systems that were deployed in March 2012, featured an updated accelerator time stamping system that improved upon the prototype design and removed the initialization uncertainties that lead to unit to unit variation. These new systems also added new functionality to allow for arbitrary 50 Ω terminated TTL signals to be treated as external trigger sources that would be time stamped and published to the event queue in the same manner as the accelerator events are. This permits the timing system to operate as a stand alone trigger system, capable of generating triggers based on auxiliary detectors or calibration sources and allows external trigger logic to be utilized to permit the otherwise free running/minimum bias NOνA detectors to be operated the fixed target and test beam facilities at FNAL.

7. Master Clock

The NOνA experiment needs to establish a universal clock system which can track the current time that is reported by every piece of readout electronics. To establish this universal clock each piece of electronics in the NOνA timing chain accepts as inputs a set of four LVDS timing lines whose signals are generated at the master timing system and each unit in the chain provides a counter that is intended to hold the value of the current time as represented in the NOνA time spec. The primary LVDS timing line that is fanned out to all readout hardware in the NOνA experiment, carries a stable clock signal that is derived via a PLL from the GPS 10 MHz clock output and can run at 16, 32, 64 or 128 MHz depending on the detector that the timing system is intended to drive. This clock line is denoted as the “Master Clock”, as it is derived by the master TDU for the timing chain and universally distributed across the detector systems. This
clock line is designed to drive the time stamp counter on each readout unit, incrementing them on each successive cycle. The result is a high resolution timer that is continuously counting in step with the master timebase regardless of the location of the physical location of the readout hardware along the timing chain.

The master clock is also used to drive the sampling components of the front end systems (ADCs and FPGAs) which permits the digitization and to be precisely synchronized to the NO\(\nu\)A time specification’s 16 MHz and 64 MHz boundaries. When the master clock line is not present, the timing distribution units and data concentrator modules have the ability to switch to an independent high precision oscillator which is not disciplined by the GPS lock system. This permits operation of the NO\(\nu\)A frontend electronics in a standalone mode for the purpose of diagnostics or testing.

During the actual operation of the system, the readout and digitization systems utilize only the value of the time stamp counter to affix timing information to the data packets. The system never is required to stop or start readout gates, nor perform clear operations in the way that a traditional TDC system would. This allows the value of the timestamp counter to be safely changed while the system is running without causing the readouts to fail or to suffer dead time. This feature is used by the NO\(\nu\)A system to allow for system wide synchronization and for periodic resynchronization to ensure that the full detector system remains synchronized to within 1 clock cycle at all times. This operation is described in detail in section 9.

8. Calibration
The delays between elements of the NO\(\nu\)A timing system are calibrated through a loopback time of flight procedure. The “SYNC echo return” LVDS timing line used in the time system is a unidirectional line that transmits a reflection of the SYNC pulse line in the direction opposite the three other timing lines (i.e. the SYNC return line runs upstream through the system, terminating at the Master TDU.) Calibration of the timing system is performed by placing the entire system into a diagnostic mode where a SYNC pulse is originated and each unit in the chain measures the time between when the pulse was received on the SYNC line and when the pulse was received back on the return/reflection line. Because the input and reflection circuits are symmetric with respect to cabling and internal propagation delays, this allows each unit to calculate the one way transmission time between that unit and the end of its timing chain.

The system can also be placed in a diagnostic mode where a SYNC pulse is originated and then reflected by a specific device instead of the end of the timing chain. This mode of calibration allows for the determination of the flight time between any two devices that are on the same branch of the timing system. This calibration technique is required to ensure that devices with multiple timing output branches, like the timing slaves, can be properly calibrated to with respect to each of their output branches.

9. System Synchronization
For the NO\(\nu\)A experiment to correctly reconstruct interactions in the detectors, each geographic region of the detector and each channel within those geographic regions must be absolutely synchronized to the universal NO\(\nu\)A time specification. The process by which the NO\(\nu\)A accomplishes this synchronization is centered around the use of the serial command channel and SYNC lines that interconnect all components of the NO\(\nu\)A timing chain.

The timing chain provides a unidirectional serial command channel which is capable of transmitting configuration and synchronization information to devices along the timing chain. The command format is a fully addressable scheme that allows for commands to be broadcast to the entire detector system or targeted to individual partitions or device groups within the detector. The commands consist of a register address and a data payload and upon reception
of a command the receiving device sets that value of the designated address to the given value or state.

While the command channel allows for efficient one way communication with the electronics, it does not provide a deterministic transmission or reception time. Commands are in fact repeated at each device interface in the chain and incur addition transmission delays at each step. The maximum number of stages that a single command needs to be transmitted across is 22 different boundaries, corresponding to the route from the master timing unit down to the last slave timing system in the chain (corresponding to the 15th kiloton of detector mass) and across to a frontend board on the outer most edge of the detector. This transmission can take upwards of 750µs with compound command sequences requiring 10’s of milliseconds to successfully complete.

Due to the non-deterministic nature of the serial command line, a separate line is used to provide deterministic signals to the electronics. This line is referred to as the SYNC line, although it is used more generally as a trigger line to initiate actions within the systems.

The NOνA system performs synchronization of the more than 357000 detector cell’s readout by combining the utility of these two lines along with always present master clock line to provide an elegant synchronization scheme. Simply described the synchronization follows the paradigm of “At the tone the time will be....” that was used extensively by commercial telephone time services. The NOνA system uses this paradigm but extends it to provide nanosecond level accuracy to the synchronization and to provide safe guards against line transmission errors and other signal transmission faults.

The synchronization procedure starts with a time circuit that is implemented in the firmware of each and every device in the NOνA timing/readout chain. The timing circuit is design to take as inputs the master clock, serial command channel and SYNC pulse lines. It provides a time stamp counter that can be enabled or disabled to increment against the master clock line and a set of 16 bit control registers that allow for data to be loaded into the circuit and for actions to be armed to be activated on reception of the next SYNC signal.

The synchronization process then is initiated from the master timing distribution unit, either as an automated process triggered by the NOνA DAQ system or as a request initiated by a user interfacing with the timing system. The master timing unit examines the current time (as derived from the GPS data stream) and determines how close it is to a 1 s boundary. The system then calculates a NOνA time sufficiently far in the future that lays on a 1 s GPS boundary and provides enough time to complete all of the data transmissions needed for the synchronization procedure. The value of this future time, converted into the NOνA time specification is then transmitted over the serial command channel into a set of four 16 bit registers that serve as “pre-load” values corresponding to high and low words the NOνA timestamp. Once all the values have been loaded into the registers, a “preset-enable-arm” command is sent over the command channel which toggles the time circuit to take an action, specifically a clock synchronization, on reception of the next SYNC signal. This process is shown in Fig. 8-11.

A SYNC pulse is then sent from the master timing unit at a calculated time prior to the upcoming 1 s boundary sufficient to allow for the SYNC to be received at all of the units in the timing chain prior to the designated time. Each timing circuit in the system receives the SYNC pulse and buffers it in a programmable delay. The delay is calibrated with the required offset of that specific device with respect to propagation delays of the rest of the timing chains. The timing circuit waits for the required delay as determined by the cycles of the master clock line, and then “delivers” the SYNC to the circuit.

Upon reception of the SYNC the timing circuit latches the values present in the preset registers into the master time stamp counter and then resumes incrementing the counter on the next master clock cycle. The finally “preset-enable-arm” register is cleared to prevent a subsequent SYNC from re-triggering the synchronization cycle.
Figure 8. Synchronization Step 1: Preload registers are populated with a predetermined time in the future.

Figure 9. Synchronization Step 2: The system is armed to react with a synchronization action upon reception of the next SYNC pulse.

Figure 10. Synchronization Step 3: The SYNC pulse is received and buffered in a calibrated delay loop.

Figure 11. Synchronization Step 4: The SYNC pulse is delivered to the timing circuit and the value of the preload registers is latched into the master timestamp counter.

Because each device has knowledge of the propagation delays required for each unit downstream of it, the delay buffer ensures that the SYNC signals are delivered system wide on the same master clock cycle, with the only potential for variation being slight phase differences in the master clock line at each device. To account for this the delay is actually programmable in quarter clock increments. For the 32 MHz base clock used on the NOνA integration prototype detector this permits system wide synchronization to within 7.8 ns across all detector elements. This level of synchronization is sufficient for the core measurements that the NOνA experiments is designed to make.

10. Site to Site Correlation
The NOνA data acquisition and triggering system is designed to receive information from the accelerator complex corresponding to the time at which an accelerator event occurred and the
duration of the event. In the case of NuMI or Booster beam spills the crucial information that is required by the trigger system is the time at which the beam spill started as denoted by the time at which the extraction signals were received at the NOνA timing systems installed in the MINOS service building. From these beam spill start times, the appropriate time of flight offsets can be calculated for each of the detector sites (near and far) and triggers issued.

What is unique about the NOνA experiment is that all of the data, every non-zero hit in the detector, has affixed to it a timestamp in the NOνA time specification. Because this time specification is a universal “wall” clock time, correlating the beam spill with the appropriate data in the detector is accomplished by simply searching the data stream for all hits with timestamps in the beam spill time window as propagated to the detector site.

The absolute “wall” clock time is established and linked at each site by the GPS receiver locks, but additionally cross checked by having redundant timing systems at each site utilizing independent receivers. The correct initialization and any subsequent drift in the systems at each site are checked through the use of a calibration system which generates and fans out a TTL signal which is then timestamped by all the timing units at the detector site. This permits detection of any anomalous offsets with respect to the GPS data streams and allows for addition calibration and pulser systems to be driven off of these signals to verify detector synchronization.

11. Conclusions

The NOνA timing system has demonstrated its capability to establish a stable clock system that can be distributed across the NOνA far detector, as well as synchronize the more than 357000 channels of detector readout with sub 10 ns accuracy. The timing system is additionally able to provide a method of time stamping beam spill information originating from the Fermilab accelerator complex and correlating that information through a GPS based timestamp specification to the data being produced by the NOνA detectors.

The first version of the NOνA timing system was deployed in 2010 for the integration prototype near detector and has been in constant operation since then. The system has proven that it is able to interface correctly with the Fermilab accelerator systems as well as synchronized the detector readout system to a precision meeting the experimental specifications.

The production version of the NOνA timing system, which include multiple upgrades to the prototype system originally installed in 2010, has been installed at the far detector sight in Ash River, MN and has been running in a diagnostic mode since March 2012. The system will be used to acquire the first detector data in the late summer and early fall of 2012.

References

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