Operation Merging for Hardware Implementations of Fast Polar Decoders

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Abstract—Polar codes are a class of linear block codes that provably achieves channel capacity. They have been selected as a coding scheme for the control channel of enhanced mobile broadband (eMBB) scenario for 5th generation wireless communication networks (5G) and are being considered for additional use scenarios. As a result, fast decoding techniques for polar codes are essential. Previous works targeting improved throughput for successive-cancellation (SC) decoding of polar codes are semi-parallel implementations that exploit special maximum-likelihood (ML) nodes. In this work, we present a new fast simplified SC (Fast-SSC) decoder architecture. Compared to a baseline Fast-SSC decoder, our solution is able to reduce the memory requirements. We achieve this through a more efficient memory utilization, which also enables to execute multiple operations in a single clock cycle. Finally, we propose new special node merging techniques that improve the throughput further, and detail a new Fast-SSC-based decoder architecture to support merged operations. The proposed decoder reduces the operation sequence requirement by up to 39%, which enables to reduce the number of time steps to decode a codeword by 35%. ASIC implementation results with 65 nm TSMC technology show that the proposed decoder has a throughput improvement of up to 31% compared to previous Fast-SSC decoder architectures.

Index Terms—Polar codes, wireless communications, successive cancellation decoding, throughput, 5G

I. INTRODUCTION

Polar codes, introduced by Arıkan [2], are a class of linear block codes that provably achieves channel capacity. They have been selected as a coding scheme for enhanced mobile broadband (eMBB) scenario under 5th generation wireless communication standards (5G) [18], [19], and are also being considered for ultra reliable low-latency communication (URLLC) and massive machine-type communication (mMTC) in 5G networks [20], [21].

Successive cancellation (SC) decoding of polar codes is the original decoding scheme proposed in [2], and can be represented as a binary tree search. However, this approach suffers from long decoding latency due to its sequential nature, and mediocre error-correction performance at moderate to short code lengths. In order to reduce the latency of SC decoding, SSC [3] and Fast-SSC [4] decoders proposed efficient decoding techniques for particular information and frozen bit patterns, called special nodes, without affecting the error-correction performance. Compared to conventional SC decoder implementations [5], Fast-SSC decoding is shown to improve the throughput by an order of magnitude. Further identification and use of special nodes were carried out in both SC-based [1], [6], [7] and SC-List based [9], [10] decoding techniques.

In [4], a number of parallel processing elements ($P_e$) allows to achieve high throughput. However, there are two problems regarding the use of parallel processing elements in Fast-SSC decoding. The first issue is that the memory utilization factor of the decoder decreases with increasing $P_e$. Secondly, for nodes with sizes smaller than $P_e$, a single operation is performed where the architecture is able to support multiple operations.

In this work, we present a new Fast-SSC decoder architecture that substantially increases the memory utilization. Unlike the previous Fast-SSC-based architectures, the new memory utilization is regardless of the parallelization factor. The new configuration allows an opportunity to perform multiple operations at a single step. By observing the distribution of frozen bits, we identify two categories of operation merging scenarios. The first category includes merging branch-type operations, where a leaf node estimation is not included. The second category includes merging of special nodes at the bottom of the SC tree. A subset of them is selected for a new SC-based decoder implementation to improve the decoder throughput. Results show that, our proposed decoder reduces the number of operations by up to 39%, which enables to reduce the number of time steps to decode a codeword by 35%. Results in 65 nm TSMC CMOS show that the proposed decoder has a throughput improvement of up to 31% compared to previous Fast-SSC decoder architectures, while increasing the memory utilization to 99.6%.

This paper is an extension of our previous works in [1], [8], where memory reduction and operation merging schemes were first introduced, followed by an FPGA implementation. In this paper, we generalize operation merging scenarios and implement a novel decoder architecture with significantly improved throughput.

The rest of this paper is organized as follows: In Section II preliminaries for polar code encoding and decoding are reviewed. A new memory design to improve utilization for Fast-SSC decoding is described in Section III. Section IV describes operation merging scenarios for Fast-SSC decoding. In Section V a new Fast-SSC decoder architecture is described. ASIC synthesis results for the new decoder are presented and compared against state-of-the-art decoder implementations in Section VI, and finally concluding remarks are addressed in Section VII.
Polar codes are able to achieve channel capacity through channel polarization, that splits $N$ channel utilizations into $K$ reliable ones, through which information bits are sent, and $N-K$ unreliable ones, used for frozen bits. A polar code, represented as $PC(N,K)$, is a linear block code of length $N = 2^n$ and rate $R = K/N$. Encoding of a polar code can be represented by a matrix multiplication:

$$x_0^{N-1} = u_0^{N-1}G^0,$$

where $u_0^{N-1} = \{u_0, u_1, \ldots, u_{N-1}\}$ is the input vector, $x_0^{N-1} = \{x_0, x_1, \ldots, x_{N-1}\}$ is the encoded vector, and the generator matrix $G^{\otimes n}$ is the $n$-th Kronecker product of the polar code matrix $G = [I \ 0]$. A polar code of length $N$ is composed of two concatenated polar codes of length $N/2$; Fig. 1 depicts the encoding process for $PC(8,5)$.

### B. Successive Cancellation Decoding

SC decoding [2] can be interpreted as a binary tree search and is explored depth-first, with priority to the left branch. An example to SC decoder tree for $PC(16,10)$ is shown in Fig. 2. The root of the tree consists of the information obtained by the channel, which is expressed in terms of log-likelihood ratio (LLR) for this work. At each stage of the tree, the LLR values $\alpha = \{\alpha_0, \alpha_1, \ldots, \alpha_{2^S-1}\}$ are passed from a parent node to its child nodes, and hard decision estimates $\beta = \{\beta_0, \beta_1, \ldots, \beta_{2^S-1}\}$ are passed from a child node to its parent node. The soft information passed to left child $\alpha^l$ and right child $\alpha^r$ are approximated as

$$\alpha^l_i = \text{sgn}(\alpha_i) \text{sgn}(\alpha_{i+2^S-1}) \min(|\alpha_i|, |\alpha_{i+2^S-1}|)$$

$$\alpha^r_i = \alpha_{i+2^S-1} + (1 - 2\beta^l_i)\alpha_i$$

where $0 \leq i < 2^S-1$ for stage $S$, and the root node is at stage $S = \log_2(N)$.

The hard decision estimates, $\beta$ for stage $S$, are calculated via the left and right messages from child nodes, $\beta^l$ and $\beta^r$, as

$$\beta_i = \begin{cases} \beta_i^l \oplus \beta_i^r, & \text{if } i \leq 2^{S-1} \\ \beta_i^{2^S-1}, & \text{otherwise.} \end{cases}$$

where $\oplus$ denotes bitwise XOR operation, and $0 \leq i < 2^S$. At the leaf nodes, $\beta$ values are hard decisions computed by observing the sign bit of their soft information, as

$$\beta_i^{\text{leaf}} = \begin{cases} 0, & \text{if } \alpha_i^{\text{leaf}} \geq 0 \text{ or } i \in \Phi \\ 1, & \text{otherwise.} \end{cases}$$

where $i$ represents the node index and $\Phi$ denotes the set of frozen indices.

### C. Fast-SSC Decoding

Simplified successive cancellation (SSC) decoding [3] showed that the SC tree can be pruned, avoiding the descent in case of nodes whose leaf nodes are either all information bits (Rate-1) or all frozen bits (Rate-0). The Fast-SSC decoding algorithm [4] evolves SSC by identifying special patterns and presenting efficient decoding techniques for such nodes.

1) Algorithm: If we denote an information bit with 1 and a frozen bit with 0, in addition to Rate-0 and Rate-1 nodes, special nodes can occur in three other different forms in a polar code: repetition (Rep) (FF···code: repetition (Rep) (FF···FI), single parity check (SPC) (FI···II) and a pattern (FFII) which is referred as ML node in [4]. In this work, we follow the same naming conventions for simplicity.

A repetition node contains a single information bit; all other nodes are frozen. An information node encoded with frozen bits contain the same information bit in all the nodes. The hard decision is made by adding the LLR values together and extracting the sign bit of the result:

$$\beta_i = \begin{cases} 0, & \text{if } \sum_{i=0}^{N_i-1} \alpha_i \geq 0 \\ 1, & \text{otherwise.} \end{cases}$$

In SPC nodes, due to the nature of the polar code construction, the frozen bit represents the parity of all the information bits of the node. Consequently, the parity check for all hard decisions (HDs) (Eq. 7) of an SPC node must be zero (Eq. 8).

$$\text{HD}_i = \begin{cases} 0, & \text{if } \alpha_i \geq 0 \\ 1, & \text{otherwise.} \end{cases}$$

$$\text{parity} = \bigoplus_{i=0}^{N_S-1} \text{HD}_i$$
If the parity constraint is satisfied, the decoding of the SPC node is assumed successful. If the parity is not satisfied, it means that there is at least one error. To satisfy the parity check constraint, the bit with the least reliable LLR is found (Eq. 9) and flipped (Eq. 10):

\[ j = \arg \min(|\alpha_i|); \ 0 \leq i < N_S, \]  

\[ \beta_i = \begin{cases} 
\text{HD}_i \oplus \text{parity}, & \text{when } i = j, \\
\text{HD}_i, & \text{otherwise.} 
\end{cases} \]  

Merging schemes for these special nodes were also proposed in the Fast-SSC decoder to improve the throughput further. A complete list of operations are detailed in Table I including their merged operations.

2) Decoder Architecture: The Fast-SSC architecture described in [4] contains separate memory units for channel LLR values, intrinsic LLR values \( \alpha \), partial sums \( \beta \), decoding instructions, and the final codeword. Words from channel, \( \alpha \) and \( \beta \) memory units are routed to an ALU unit, where the identified operations listed in Table I are performed. Left operation (F), right operation (G) and combine operation (C) are adopted from the SC decoding of [2]. The notations 0, 1 and R represent child nodes with Rate-0, Rate-1 and Rate-R \((0 < R < 1)\). The operations with P- notation represent the operations performed without explicitly visiting the right child node. Routing of the memory and configuration of the datapath are controlled based on the instruction list that is compiled offline. The datapath for the Fast-SSC decoder is depicted in Fig. 3.

Execution of a single operation is called a step, and each step may take one or more clock cycles, based on the tree stage and the number of physical processing units dedicated to perform the operation. If \( P_e \) is too small, operations to decode a codeword takes too many clock cycles which results in reduced throughput. The number of cycles to decode a single frame decreases with increasing \( P_e \), which helps increase the throughput. For example, for \( PC(1024, 512) \), number of clock cycles to decode a codeword is 571 when \( P_e = 16 \), and is 217 when \( P_e = 256 \). On the other hand, with increasing \( P_e \), the idle time of the computational resources increase, decreasing the resource utilization. Fast-SSC decoder is a special decoder that is based on semi-parallel SC decoder family [4]. According to [13], the utilization rate \( \theta_{SP} \) of a semi-parallel decoder is given by

\[ \theta_{SP} = \frac{\log_2 N}{4 \times P_e + \log_2 \frac{N}{P_e^2}}, \]

which leads to \( \theta_{SP} = 13.8 \) when \( P_e = 16 \) and to \( \theta_{SP} = 0.9 \) when \( P_e = 256 \), respectively. Fig. 5 plots the number of cycles to decode a codeword \( (T_{\text{latency}}) \) and resource utilization \( \theta_{SP} \) as a function of the number of processing elements. It can be seen that the utilization rate decreases significantly with increasing \( P_e \), whereas after \( P_e = 64 \), the latency improvement is marginal. Thus, while keeping a reasonable resource utilization and maintaining low decoding latency, \( P_e = 2^6 \) is a reasonable choice for \( N = 1024 \).

The SC tree for a \( PC(1024, 512) \) with nodes from Table I is presented in Fig. 4. The polar code construction is obtained from the 5G standard [18]. The Fast-SSC from [4] executes

![Fig. 4: PC(1024, 512) tree [18] with special nodes from Table I. Green circles are Rep nodes, yellow circles are SPCs, blue circles are ML nodes, white are Rate-0, black are Rate-1, gray are Rate-R. Dashed line represents the parallelization threshold when \( P_e = 2^6 \), under which the computational resources are under-utilized.](image-url)
a total number of 212 steps in 268 clock cycles to decode a single frame of Fig. 4 when \( P_e = 2^e \).

3) Memory: In the SC tree there are \( \log_2(N) + 1 \) stages, with the highest stage \( \log_2(N) \) corresponding to the root node, and the lowest stage \( \log_2(1) = 0 \) to the leaf nodes. For each stage of the SC tree, both \( \alpha \) and \( \beta \) are stored in designated memory modules. The \( \alpha \) memory is comprised of two banks, each of which is \( P_e \) LLRs wide. The partial sum \( \beta \) memory is composed of two memory units, each of which has two banks, and each bank is \( P_e \) bits wide. A full word is defined as the content from an index of a memory unit. At each clock cycle, a full word can be read from each memory. The F and G modules can process \( 2 \times P_e \) \( \alpha \) and \( P_e \beta \) values at once to generate \( P_e \) \( \alpha \) outputs, thus a half word can be written back to the \( \alpha \) memory. Combine (C) unit takes a half word from each \( \beta \) memory bank, to produce a full word that should be written to either of the banks. Consequently, a half word can be read from each \( \beta \) memories, and a full word can be written back to one \( \beta \) memory.

In terms of both \( \alpha \) and \( \beta \) memories, at least one word is reserved for each stage of the tree. Fig. 6 represents the memory architecture for both \( \alpha \) and \( \beta \) memories for \( PC(1024, K) \) code. The root node (S=10) is stored explicitly in the channel memory, because it has a different quantization scheme than the internal LLRs. Due to special node decoding techniques mentioned in Section II-C, the lower limit stage is S=2, thus no additional memory is required after stage S=2. In general, given that each word holds \( 2 \times P_e \) elements for \( \alpha \) and \( \beta \) memories, the number of words for each memory module is:

\[
\sum_{S=2}^{\log_2(N-1)} \left\lfloor \frac{2^S}{P_e} \right\rfloor .
\]  

III. IMPROVING MEMORY UTILIZATION

As it was previously mentioned in Section II-C, one or more words are reserved in both \( \alpha \) and \( \beta \) memories per decoding stage in the tree. The word size is decided by the number of processing elements \( P_e \), that acts as a parallelization factor. \( P_e \) can also be interpreted as a threshold on the SC tree (dashed line in Fig. 4), where the node size \( N_v = P_e \). The stages above this parallelization threshold are collectively called high-stage, and each stage in high-stage fully utilizes the dedicated memory words for that level; below the threshold (low-stage), only a portion of the memory is used. In fact, the total number of variables used at low-stage can be expressed as

\[
\sum_{S=2}^{\log_2(P_e)} 2^S < 2 \times P_e
\]

which can fit into a single memory word.

We improve the memory utilization by storing all the variables relative to the low-stage into a single memory word in both \( \alpha \) and \( \beta \) memory units. Fig. 7 describes the new memory configuration for the low-stage, using a polar code \( PC(1024, K) \) and \( P_e = 64 \) as an example. With the proposed solution, the number of \( 2 \times P_e \)-sized words for each memory becomes

\[
\sum_{S=\log_2(P_e)}^{\log_2(N-1)} \left\lfloor \frac{2^S}{P_e} \right\rfloor
\]

Considering a polar code \( PC(1024, K) \) and \( P_e = 64 \), the memory utilization increases from 66% to 99.6%.

With these modifications to the memory structure, when a node at the low-stage is to be processed, the entire last word is fetched from the memory. Since the content of the memory is relative to multiple stages, executing multiple operations per clock cycle becomes possible.

IV. OPERATION Merging

In this work, we define an operation as a leaf operation if it involves a leaf node estimation, and as a branch operation if it does not include any bit estimations. According to this
classification, hard decision [5], Rate-0, Rate-1, Rep [6] and SPC [8]–[10] calculations are leaf node operations, whereas F [2], G [3] and C [4] are branch operations for SC decoding. Note that proposed merged operations do not affect the error-correction performance.

A. Merging Branch Operations

If the memory configuration in Fig. 7 is used within the Fast-SSC decoder architecture, all α and β variables below the parallelization threshold become available for processing at the same time. This enables the Fast-SSC processor to perform multiple operations at a single cycle. In other words, operations below the parallelization threshold are available for merging. However, the impact of operation merging on system critical path should be minimized and thus the original critical path should be considered as an upper delay bound while performing multiple low-stage operations in a single cycle. It was observed that the critical path of the original Fast-SSC architecture is determined by the SPC node. Compared to SPC-related operations, branch operations introduce a significantly lower delay; this provides the opportunity to merge them without increasing the system critical path. Consequently, we exploit the branch operation merging opportunities at low-stage. Based on the data dependencies while decoding, the following merging scenarios are possible for operations of the same kind:

- Multiple F operations: The traversal of the SC tree has a left branch priority, which enables to perform multiple F operations consecutively.
- Multiple G0 operations: Tree traversal allows consecutive G operations only when the left node is a Rate-0 node and needs not to be traversed.
- Multiple C/C0 operations: A sequence of Combine operations is possible when the operation ascends from a right branch, i.e. β values of the left children are already available. This constraint does not apply to the last C operation in the sequence.

These four different merging branch operations of the same kind are visualized in Fig. 8.

The combination of different branch operations at low-stage is also feasible. It was observed that a G operation is often followed by an F operation, which can be merged together to form a new operation called G-F. Similar observations were made for F-G0, C-G and C0-G. A complete list of merged branch operations and their associated potential step reduction is presented in Table II for $PC(1024, K)$ [18]. According to Table II, the amount of time step reduction increases with $P_e$. It can also be observed that G-F merging scenario returns the most amount of reduction. Note that, the merging scenarios in Table III are computed independently, without considering any conflicts between the merging scenarios. A set of guidelines for how to merge operations are detailed in Section IV-C.

B. Merging Special Nodes

As mentioned in Section II-C, the Fast-SSC architecture from [4] uses merging of special nodes in order to improve the throughput. For example, the SPC and Sign operators in between G and C modules in Fig. 3 enable the datapath to execute P-RSPC, P-0SPC, P-R1, P-01, G0 and C0 operations from Table I. On the other hand, a separate module for RepSPC node is instantiated to avoid the critical path. In this Section, based on the observations made from the polar code tree in Fig. 2, we identify all possible special node merging scenarios. It should be noted that some of the special node merging scenarios in this Section fall within the generalized nodes from [11], where however no hardware implementation were proposed.

Table III describes a number of possible leaf node merging scenarios along with their node sizes, breakdown of operations (translations), and amount of time step reduction with respect to $P_e$. It is important that the $P_e$ threshold must be larger than 16 to support the new node sizes in Table III. If $P_e \leq 16$, described merging operations fall above the parallelization threshold in the polar code tree, and they...
cannot be merged. Rep-Rate1 and Rate0-RepSPC nodes were previously identified in \cite{7}; we include them in this work in order to compare them with newly identified nodes in terms of time step reduction. Similar to Table \ref{tab:potential_time_step_reduction}, the time step reduction calculations are done independently from each other. According to Table \ref{tab:potential_time_step_reduction}, merged special node operation Rep-RepSPC returns the most potential time step reduction, followed by F-Rep. Note that the instances of F-Rep operation occurs within Rep-RepSPC nodes, which can be observed in their translations. The selection of merging scenarios for special nodes should not only be performed with respect to their independent contribution on time step reduction, but also with respect to their impact on the maximum operating frequency. Merging a special node with a Rate-0 node is more favorable than merging with Rate-1 nodes since their calculation takes less time and area. The impact of merged operations on maximum operating frequency should be taken into account when compiling a new instruction set.

### C. Guidelines for Operation Merging

The time step reduction amounts in Table \ref{tab:potential_time_step_reduction} and in Table \ref{tab:potential_time_step_reduction} are observed independently: not all of the merging can be exploited at the same time. For example, if a series of operations such as (G-F-F) is present at low-stage, the potential time step reduction is a possible operation merging scenario, it is not used in our approach.

- **C-G vs. $C^x(2,3,4)$, (C0-G vs. $C0^x(2,3))$:** If C-G/C0-G operation will be used as a merging scenario, the merging of consecutive C (C0) operations is advised to begin from the head operation towards the tail operation, to maximize the chances of merging with a G operation that follows it, leading to a C-G (C0-G) operation.

- **F-G0 vs. $G0^x(2,3)$ and $F^x(2,3,4)$:** Merging of consecutive G0 operations starts from the tail G0 operation towards the head operation, to minimize the conflict with potential F-G0 operation. To further minimize conflicts, F operations should be merged starting from the head operation; however this decision would contradict the decision made for the sake of maximizing G-F operations. Based on observations, the number of occurrences of G-F is much higher than that of F-G0, thus F is decided to be merged starting from the tail F operation.

- **F-Rep vs. $F^x(2,3,4)$:** To minimize the conflict between F-Rep and consecutive F operations, merging F is advised to begin from the head operation. However, similar to the previous case, this conflicts with the G-F operation merging scenario. Although F-Rep is one of the leaf node operations that returns a favorable amount of time step reduction, if Rep-RepSPC node is used, most of F-Rep operations will be included within it. Because of this, F-Rep operation loses priority against G-F operation. Consequently, merging F operations begin from their tail operation, and F-Rep should be merged from the remaining ones.

- **Merged special nodes vs. F/G0/C/C0:** As described in Table \ref{tab:potential_time_step_reduction} merging special nodes include branch operations. Additionally, merging special nodes returns more time step reduction compared to branch operation merging. Thus, in order to minimize merging conflict and maximize savings, special nodes must be merged before merging branch operations.

| Merging Scenario | New Node Size | Translation | $P_e = 32$ | $P_e = 64$ | $P_e = 128$ |
|------------------|---------------|-------------|-------------|-------------|-------------|
| Rep-RepSPC       | $N_v = 16$    | F $\rightarrow$ Rep $\rightarrow$ G $\rightarrow$ RepSPC $\rightarrow$ C | 3.33% | 4.48% | 5.19% |
| Rate0-RepSPC     | $N_v = 16$    | G0 $\rightarrow$ RepSPC $\rightarrow$ C0 | 1.11% | 1.49% | 1.73% |
| RepSPC-Rate1     | $N_v = 16$    | F $\rightarrow$ RepSPC $\rightarrow$ P-R1 | 0.28% | 0.37% | 0.43% |
| Rep-Rate1        | $N_v = 8$     | F $\rightarrow$ Rep $\rightarrow$ P-R1 | 1.11% | 1.49% | 1.73% |
| Rate0-ML         | $N_v = 8$     | G0 $\rightarrow$ ML $\rightarrow$ C0 | 1.11% | 1.49% | 1.73% |
| ML-Rate1         | $N_v = 8$     | F $\rightarrow$ ML $\rightarrow$ P-R1 | 0.28% | 0.37% | 0.43% |
| F-Rep            | $N_v \in \{8, 16, 32\}$ | F $\rightarrow$ Rep | 2.78% | 3.73% | 4.33% |
TABLE IV: New instruction set for the proposed Fast-SSC decoder.

| Operation | Details |
|-----------|---------|
| F×2       | Two consecutive F operations. |
| G0×2      | Two consecutive G0 operations. |
| C×2, C×3  | Up to three consecutive C operations. |
| C0×2, C0×3| Up to three consecutive C0 operations. |
| G-F       | G operation followed by an F operation. |
| F-G0      | F operation followed by a G0 operation. |
| F-Rep     | F operation followed by a Rep node. |
| Rep-RepSPC| Node with Rep and RepSPC nodes as its children. |
| Rep-Rate1 | Node with Rep and Rate-1 nodes as its children. |
| Rate0-ML  | Node with Rate-0 and ML nodes as its children. |

TABLE V: Amount of savings in terms of number of operations and time steps, with operation set from Table IV for polar codes of various rates and $P_e$ compared to Fast-SSC decoder of [4].

| Polar Code | $R$ | $P_e$ | Oper. Savings | Time Step Savings |
|------------|-----|------|--------------|------------------|
| $PC(1024, 256)$ | $\frac{1}{4}$ | 32   | 27.43%       | 15.14%           |
|           |     | 64   | 34.86%       | 26.87%           |
|           |     | 128  | 38.86%       | 35.42%           |
| $PC(1024, 512)$ | $\frac{1}{2}$ | 32   | 26.54%       | 15.56%           |
|           |     | 64   | 32.70%       | 25.75%           |
|           |     | 128  | 35.55%       | 32.47%           |
| $PC(1024, 768)$ | $\frac{3}{4}$ | 32   | 22.54%       | 12.42%           |
|           |     | 64   | 26.01%       | 19.91%           |
|           |     | 128  | 30.06%       | 27.23%           |

The amount of savings in terms of the number of operations and the number of time steps with the new operation set listed in Table IV is detailed in Table V for polar codes of length $N = 1024$, $R \in \{\frac{1}{4}, \frac{1}{2}, \frac{3}{4}\}$ and $P_e \in \{32, 64, 128\}$. Note that the 5G standard allows a wide range of code rates with binary granularity. Thus, we limit our exploration within three selected rates. It can be seen that the amount of reduction in terms of both number of operations and number of time steps increases with $P_e$. It can also be observed that with increasing $P_e$, the amount of time step reduction increases at lower rate codes, since the new instruction list in Table V favors Rate-0/Rep nodes more than Rate-1/SPC nodes.

Fig. 9: High-level architecture of the proposed Fast-SSC decoder.

V. DECODER ARCHITECTURE

A. Architecture Overview

In order to evaluate the impact of merged operations on the throughput, a new Fast-SSC architecture has been implemented. The architecture supports the fast node decoding techniques from Table I as well as the new instruction set from Table IV. The high-level description of the architecture is depicted in Fig. 9. Decoding sequence begins after loading the instructions into the instruction RAM, and when Channel LLRs are present in the Channel RAM. Note that loading the instruction sequence has to be done only once. The LLR values obtained from the channel are stored in the channel memory, which has a different quantization scheme than the internal LLR $\alpha$ memory. The controller tracks the stage size for each instruction and routes the correct words to and from the $\alpha$ and $\beta$ memory units. A codeword RAM is separately instantiated from the $\beta$-RAM and stores the estimated codeword. From $\alpha$-RAM, $2 \times P_e$ LLR values are fetched and $P_e$ LLRs are stored at a time. In case of $\beta$-RAM, $2 \times P_e$ partial sum values can be read and stored in a single cycle. For high-stage LLR and partial sum computations, the information is processed $2 \times P_e$ elements at a time. Hence, for $S > \log_2 P_e$, $2^S/2 \times P_e$ time steps are required. For low-stage operations, a single time step is required.

In merged branch operations, the output of a prior sub-operation is immediately used by the operation that follows it, and storage can often be avoided. For example, the output of the first sub-operation of G0×2 is used only by its following G0 operation and is never used again. Consequently, only the output of last sub-operation is stored into memory. On the other hand, the output of each F sub-operation of F×2 will be used by another operation in the future, which makes it mandatory to store the output of the first F sub-operation. By avoiding the storage of intermediate values that will not be used in future instructions, it is possible to save memory bandwidth and increase the number of parallel operations that can be performed by merged operations. The complete list of the intermediate data storing choices, and maximum parallel operations for merged operations are listed in Table VI.
TABLE VI: Details of data storing requirements and maximum number of inputs for merged operations.

| Branch Operations | Storage of all data | Max. number of inputs |
|-------------------|---------------------|-----------------------|
| F×2               | Yes                 | $P_e$                 |
| G0×2              | No                  | $2 \times P_e$        |
| C/C0×{2,3}        | No                  | $P_e/2$               |
| G-F               | Yes                 | $P_e$                 |
| F-G0              | No                  | $2 \times P_e$        |
| C-G/C0-G          | Yes                 | $P_e/2$               |

Fig. 10: Proposed Fast-SSC datapath architecture to support operations from Table I and Table IV.

B. Datapath

Fig. 10 shows the datapath architecture for the proposed Fast-SSC decoder, based on the implementation in [4]. It supports all the operations listed in Table I and Table IV. The original critical path (in both Fig. 3 and Fig. 10) lies on the path G-SPC-C. To support multiple operations in a single cycle, the new G0 and C modules require more hardware complexity than the original G and C modules. Consequently, to avoid lengthening the critical path, modules including G and C operations are instantiated separately, and the old G and C modules are only used for P- prefixed operations from Table I. Modules F-G0 and G-F, and F-Rep are used only on the low-stage. Processing units for special nodes and their merged versions are clustered together in Fig. 10; they receive LLR values from the $\alpha$ memory and output their hard decision estimates to $\beta$ memory.

In order to support single operations of high-stage as well as single and multiple operations of low-stage, the F processing unit has been redesigned and is shown in Fig. 11. The new F processing unit is capable of performing high-stage operations in multiple clock cycles, as well as performing single and multiple operations at low-stage. The subscripts in Fig. 11 correspond to the number of parallel F processing elements, which is $P_e$ in total. At high-stage operations, the inputs of all F processing units in Fig. 11 are provided from the $\alpha$ memory. For multiple operations at low-stage, the multiplexers are configured by the controller to cascade the processing units. The configuration of multiple operations are established through the multiplexers in the design: if a merged F operation is performed, following operations within the merged F operation take their inputs from the output of a previous F module. Similar architectures have been implemented for G0 and C/C0 modules.

Fig. 12 presents the Rep-RepSPC processing unit from Table IV. The input and the output size of the Rep-RepSPC has a fixed length of 16. The units enclosed with dashed lines are instances of the RepSPC processing unit. The RepSPC modules assume the output of the Rep node as $0$ and $1$ and are processed in parallel with the Rep module. Modules G0 and G1 are G operations that assumes $\beta$ as $0$ and $1$, respectively. Based on the hard decision estimate of Rep node, the output of the RepSPC is selected from the final multiplexer and is stored in the $\beta$ memory.

VI. RESULTS

A. Error-Correction Performance

To validate the error-correction performance for the proposed decoder, a quantization scheme $Q(6, 5, 1)$ has been used, where $Q(Q_i, Q_c, Q_f)$ are quantization bit size for internal LLRs, channel LLRs, and fraction bit size for both internal and
TABLE VII: TSMC 65 nm CMOS implementation results for Fast-SSC based polar decoders, $N = 1024$, $R \in \{\frac{1}{4}, \frac{1}{2}, \frac{3}{4}\}$ and $P_e = 64$.

| Algorithm | [4] | [7] | [1] | This Work |
|-----------|-----|-----|-----|-----------|
| Rate      | 1/4 | 1/2 | 3/4 | 1/4 | 1/2 | 3/4 | 1/4 | 1/2 | 3/4 |
| Latency ($\mu$s) | 0.5 | 0.6 | 0.5 | 0.49 | 0.56 | 0.48 | 0.45 | 0.51 | 0.44 | 0.39 | 0.46 | 0.42 |
| Coded T/P (Mpbs) | 2030 | 1719 | 2039 | 2104 | 1829 | 2114 | 2288 | 2000 | 2337 | 2653 | 2213 | 2433 |
| Info. T/P (Mpbs) | 507 | 860 | 1529 | 526 | 914 | 1585 | 572 | 1000 | 1753 | 663 | 1106 | 1825 |
| Area (mm$^2$) | 3.38 | 2.87 | 3.4 | 4.78 | 4.16 | 4.8 | 4.01 | 3.51 | 4.10 | 4.14 | 3.46 | 3.80 |
| Energy (pJ/bit) | 316.81 | 187.02 | 105.14 | 216.72 | 124.69 | 71.91 | 303.80 | 173.72 | 99.11 | 285.15 | 170.92 | 103.64 |

Fig. 12: Architecture of Rep-RepSPC processor.

channel LLRs, respectively. Fig. 13 depicts the error correction performance of the proposed decoder in terms of bit error rate (BER) and frame error rate (FER). The polar code construction is obtained from [18] for $N = 1024$, and rates are selected as $R \in \{\frac{1}{4}, \frac{1}{2}, \frac{3}{4}\}$. The selected quantization values result in less than 0.03 dB loss at FER = $10^{-4}$ compared to floating-point precision. The introduced operation merging techniques do not change the error-correction performance of SC decoding, as they map thoroughly to SC decoding schedule.

B. ASIC Synthesis Results

The architecture for the proposed Fast-SSC decoder has been implemented in VHDL and synthesized in TSMC 65 nm CMOS technology using Cadence Genus RTL compiler. For a fair comparison scheme, three other Fast-SSC-based decoders from [1], [4], [7] have also been implemented using the same technology node, quantization, voltage supply and $P_e$. Table VII presents the ASIC implementation results for code rates $R \in \{\frac{1}{4}, \frac{1}{2}, \frac{3}{4}\}$.

According to Table VII, the proposed Fast-SSC decoder has a throughput improvement of up to 31% and 26% compared to the earlier implementations from [4] and [7], respectively. Compared to our previous work in [1], the throughput improvement is up to 16%. The power consumption of the proposed decoder has increased by 18% compared to the baseline Fast-SSC decoder from [4], which is due to the new decoding nodes introduced in Section V. On the other hand, due to increased throughput, energy consumption and area efficiency of the proposed decoder compared to [4] has been improved by up to 10% and 23% despite the increased power consumption. On the other hand, compared to [7], the proposed decoder implementation consumes 32% more energy per bit and has 13% less area efficiency.

It can be observed in Table VII that, for all Fast-SSC-based implementations, the latency and the coded throughput are the lowest when $R = 1/2$. This is due to the fact that the occurrence of Rate-0 nodes increase when rate becomes lower, and Rate-1 nodes increase when rate becomes higher. Around $R \approx 1/2$, Rep, SPC and ML nodes occur more frequently, which in general takes more time for decoding. As a result, the area efficiency has the same trend with latency and coded throughput with respect to code rate. On the other hand, the information throughput increases with the rate for all Fast-SSC-based implementations since the number of information bits in the codeword increases linearly with the rate. Finally, the energy dissipation per decoded bit is calculated using the number of information bits. As a result, energy per bit reduces with increasing rate for all Fast-SSC decoders in Table VII.

Table VIII presents a comparison scheme for the proposed Fast-SSC decoder against other SC-based architectures including tree, semi-parallel (SP) and combinational approaches. The throughput values for each implementation in Table VIII are scaled for 65 nm for a fair comparison. In [16], a combinational approach is used to decode the polar code, which results in low operating frequency, large throughput and increased area. Although the reported throughput is 2.2× higher than our decoder, the area is 2.62× larger, which results in 39% less area efficiency compared to the proposed architecture. In fact, compared with any Fast-SSC based architecture from Table VII, it can be observed that the area efficiency of the combinational decoder is very low due to its excessive area overhead. Compared to semi-parallel decoder implementations
with equal $P_e$, our work has up to $9 \times$ larger throughput and 8.8× better area efficiency. Finally, compared with tree-based decoder approaches, the proposed decoder has 3.18× larger throughput.

VII. CONCLUSION

In this work, we proposed a new Fast-SSC polar code decoder implementation. The proposed decoder increases the memory utilization by storing the variables relative to the stages below the parallelization threshold into a single memory word, which also enables the decoder to perform multiple operations within a single time step. A generalization of operation merging scenarios with their guidelines are presented for branch and special node operations, and a subset of the operation merging scenarios with their guidelines are presented.

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TABLE VIII: Comparison of state-of-the-art ASIC implementations decoding a PC(1024,512) polar code.

| Algorithm | This Work | [12] | [13] | [14] | [15] | [16] | [17] |
|-----------|-----------|------|------|------|------|------|------|
| $P_e$     | Fast-SSC  | Tree | Semi-Parallel | Tree | Semi-Parallel | Combinational | Semi-Parallel |
| Technology (nm) | 64  | 64  | 64  | 64  | 64  | 64  | 64  |
| Supply (V)  | -   | 1.0 | -   | 1.0 | -   | 1.3 | -   |
| Area (mm²)  | 0.64 | 0.31 | 1.71 | 3.21 | 0.68 |
| Area @ 65 nm (mm²) | 0.64 | 0.31 | 0.22 | 1.68 | 0.68 |
| Frequency (MHz) | 430 | 377 | 750 | 150 | 2.5 | 1010 |
| Throughput (Mb) | 1106 | 349 | 123 | 346 | 346 | 3544 | 497 |
| Area Efficiency (Gbps/mm²) | 3.46 | 0.39 | 0.62 | 2.11 | 0.73 |

†Scaled for 65 nm technology.
Fig. 13: Floating-point and quantized FER and BER performance for polar code with $N = 1024$ and $R \in \left\{ \frac{1}{3}, \frac{1}{2}, \frac{2}{3} \right\}$. Polar code construction is obtained from the 5G standard [18]. Solid and dashed lines represent FER and BER performances respectively.

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