Dielectric loss extraction for superconducting microwave resonators

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The investigation of two-level-state (TLS) loss in dielectric materials and interfaces remains at the forefront of materials research in superconducting quantum circuits. We demonstrate a method of TLS loss extraction of a thin film dielectric by measuring a lumped element resonator fabricated from a superconductor-dielectric-superconductor trilayer. We extract the dielectric loss by formulating a circuit model for a lumped element resonator with TLS loss and then fitting to this model using measurements from a set of three resonator designs: a coplanar waveguide resonator, a lumped element resonator with an interdigitated capacitor, and a lumped element resonator with a parallel plate capacitor that includes the dielectric thin film of interest. Unlike other methods, this allows accurate measurement of materials with TLS loss lower than $10^{-6}$. We demonstrate this method by extracting a TLS loss of $1.02 \times 10^{-3}$ for sputtered Al$_2$O$_3$ using a set of samples fabricated from an Al/Al$_2$O$_3$/Al trilayer. We observe a difference of 11% between extracted loss of the trilayer with and without the implementation of this method.

Keywords: superconducting quantum computing, TLS loss, resonator

I. INTRODUCTION

Two-level-state (TLS) loss is the dominant form of loss at millikelvin temperatures and single photon powers in superconducting quantum circuits. TLS loss is a type of dielectric loss that occurs due to an interaction with an electric field, and is generated in bulk dielectrics and interfaces between materials in superconducting quantum circuits. Materials improvements in superconducting quantum computing have largely focused on reducing the density and total loss of TLS by improving fabrication and modifying circuit design to reduce participation of lossy materials.

The total loss in a superconducting microwave resonator can be written as:

$$\tan \delta = \frac{1}{Q_t} = F \tan \delta_{TLS} + \frac{1}{Q_{HP}} \quad (1)$$

where $Q_t$ is the internal quality factor of the resonator and is equal to the inverse of the total loss in the resonator $\tan \delta$, $F \tan \delta_{TLS}$ is the TLS loss with $F$ denoting the filling factor of the TLS material, and $Q_{HP}$ is the high power loss. High power loss is generally small and power-independent in the operational regime of a superconducting quantum circuit, whereas TLS loss has a distinctive power dependence as well as a temperature dependence.

Much is still uncertain about the origins and behavior of TLS. The general model for weak-field TLS loss as a function of power and temperature is

$$F \tan \delta_{TLS} = F \tan \delta_{TLS}^0 \frac{\tanh \left( \frac{\hbar \omega_T}{2kT} \right)}{\left( 1 + \left( \frac{\nu_c}{\nu} \right)^2 \right)\beta} \quad (2)$$

where $F \tan \delta_{TLS}^0$ is the TLS loss of the system at zero power and temperature ($\langle n \rangle = 0$ and $T = 0$), $\omega_T$ is the angular resonance frequency, and $\beta$ is a variable determined by TLS population densities, but is usually close to 0.5. TLS become saturated at high powers, and therefore do not contribute to high power loss. As power decreases in the circuit, TLS loss participation increases until it flattens around single photon powers near the critical photon number $n_c$. $\tan \delta_{TLS}$ can be seen as an intrinsic value of the TLS material in question, and varies with properties of the material such as deposition parameters, surface treatments, and crystallinity.

Only capacitive components contribute to TLS loss. In the past, dielectric loss has been measured using coplanar waveguide (CPW) resonators. In a lumped element (LE) resonators with parallel plate capacitors (PPCs) and LE resonators with interdigitated capacitors (IDCs), in one strategy, the filling factor of the material is determined through simulation.

It has been previously assumed that, in a lumped element resonator with a PPC, a negligible amount of capacitance comes from the inductor so that the total TLS loss of the resonator is roughly equal to the TLS loss of the PPC. Using this assumption, a single resonator design can be measured to determine the TLS loss of a dielectric material in the PPC. This “single measurement technique” is valid when the participation and/or loss of the material in the capacitor dominates the loss of other components in the resonator.

The identification of low loss dielectrics (tan $\delta_{TLS}^0 \lesssim$ 10$^{-6}$) is in its infancy. Materials improvements in superconducting quantum circuits have largely focused on reducing the density and total loss of TLS by improving fabrication and modifying circuit design to reduce participation of lossy materials. Only capacitive components contribute to TLS loss, where $F \tan \delta_{TLS}^0$ is the TLS loss of the system at zero power and temperature ($\langle n \rangle = 0$ and $T = 0$), $\omega_T$ is the angular resonance frequency, and $\beta$ is a variable determined by TLS population densities, but is usually close to 0.5. TLS become saturated at high powers, and therefore do not contribute to high power loss. As power decreases in the circuit, TLS loss participation increases until it flattens around single photon powers near the critical photon number $n_c$. $\tan \delta_{TLS}$ can be seen as an intrinsic value of the TLS material in question, and varies with properties of the material such as deposition parameters, surface treatments, and crystallinity.

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10^{-6}) for use as substrates, junction insulators, and spacer materials for three-dimensional integration would allow for the expansion of possible circuit architectures. The implementation of a low loss dielectric could drastically decrease the qubit footprint from one millimeter to micrometers. In this work, we demonstrate that conventional methods such as the single measurement technique are not sensitive enough to determine the loss of low loss materials. A method to remove losses from other circuit components is necessary.

We present a technique to extract the TLS loss of a given material using measurements of three resonator designs: an LE resonator with a PPC, an LE resonator with an IDC, and a CPW resonator. We apply this technique to measure the TLS loss of sputtered Al/Al2O3/Al trilayers in order to report a TLS loss value of 1.02 x 10^{-3} with a difference of 11% from the single measurement technique. We also outline the design and materials regimes where the single measurement technique becomes invalid and the losses of other resonator components must be addressed.

II. DEVICE DESIGN AND FABRICATION

The material under test is a sputtered Al/Al2O3/Al trilayer deposited at the Naval Research Laboratory. 50 nm of Al, 50 nm of Al2O3, and 50 nm of Al were deposited consecutively at room temperature without breaking vacuum, with a base pressure of 6 x 10^{-6} Pa. The Al/Al2O3/Al trilayer is patterned into a PPC and incorporated into an LE resonator (Fig. 1 (a)) in order to perform TLS loss measurements. An LE IDC resonator (Fig. 2 (b) inset) and a CPW resonator (Fig. 2 (c) inset) are also measured in this work. These resonators are fabricated on the same wafer as the LE PPC resonators and are defined with liftoff in the same step as the inductors in the LE PPC resonators. More details on fabrication and geometry can be found in Table I and Appendix A.

III. TLS LOSS IN A SUPERCONDUCTING LUMPED ELEMENT RESONATOR

TLS loss in a superconducting lumped element resonator can be modeled by an RLC circuit. Under the assumption that TLS loss is the dominant form of loss, only the capacitive components have associated resistive components. Each lossy capacitor is modeled as a lossless ideal capacitor with equivalent series resistance (ESR) representing the TLS loss of that component. In this way, the lumped element capacitor is represented by an ideal capacitor of capacitance \( C_C \) with an associated ESR of resistance \( R_C \).

The inductor in a non-ideal resonator is not a purely inductive component. Some amount of stray capacitance will always be present within the inductor itself or to ground. Therefore, the inductor can be modeled as a pure lossless inductor \( L \) with a capacitor of capacitance \( C_L \) and ESR of resistance \( R_L \). A diagram of the full circuit is shown in Fig. 1 (b).

IV. LE PPC, LE IDC, AND CPW RESONATOR LOSS

The loss of the PPC can be determined from a set of three devices: an LE resonator with a PPC, an LE resonator with an IDC, and a CPW resonator. The PPC LE resonator loss is composed of inductor and PPC loss, as:

\[
F_A \tan \delta_A = \frac{C_{TLS}}{C_A} F_{PPC} \tan \delta_{PPC} + \frac{C_L}{C_A} F_L \tan \delta_L \tag{4}
\]

where the first term is PPC loss and the second term is inductor loss. We refer to the PPC LE resonator as device A.

We can measure a LE IDC resonator (device B) with the same inductor as above. Then we see:

\[
F_B \tan \delta_B = \frac{C_{IDC}}{C_B} F_{IDC} \tan \delta_{IDC} + \frac{C_L}{C_B} F_L \tan \delta_L \tag{5}
\]

We can use these measurements to solve for the PPC loss if we also know \( \frac{C_{IDC}}{C_B} \) and \( F_{IDC} \). An estimation of this term can be made by measuring a CPW resonator.
FIG. 2. Photon number sweeps for (a) an LE PPC resonator (device A), (b) an LE IDC (device B) and (c) a CPW (device C) resonator. Loss $\tan \delta$ as a function of mean photon number $\langle n \rangle$. For space reasons, optical micrographs of similar devices are shown as insets. Shown here: an LE PPC resonator of $N = 7$ (rather than $N = 17$), an LE IDC resonator of $N = 7$ (rather than $N = 13$), and a compressed CPW resonator, where $N$ is number of inductor arm pairs in design.

TABLE I. Parameters for three measured devices. $F \tan \delta_{\text{TLS}}$: measured TLS loss. $f_0$: measured resonance frequency. $N$: number of inductor arm pairs in design. $g_c$: designed coupling gap. $C_C$: capacitance of capacitor extracted from measurement, simulation, and analytical methods. $C_L$: capacitance of inductor extracted from a combination of measurement and simulation. $L$: inductance of inductor determined by simulation.

| Design  | Material            | Label | $F \tan \delta_{\text{TLS}} \times 10^{-6}$ | $f_0$ (GHz) | $N$ | $g_c$ (µm) | $C_C$ (fF) | $C_L$ (fF) | $L$ (nH) |
|---------|---------------------|-------|---------------------------------------------|-------------|-----|------------|------------|------------|----------|
| LE PPC  | Al/Al$_2$O$_3$/Al   | A     | 915 ± 6                                     | 3.7464      | 17  | 3          | 727.7      | 82.2       | 2.42     |
| LE IDC  | Planar Al           | B     | 8.91 ± 0.06                                 | 6.3798      | 13  | 30         | 34.7       | 64.4       | 1.87     |
| CPW     | Planar Al           | C     | 8.39 ± 0.08                                 | 4.5548      | -   | -          | -          | -          | -        |

that mimics the TLS loss environment of the IDC by having the same CPW gap and width as the fingers of the IDC. Then:

$$F_{\text{CPW}} \tan \delta_{\text{CPW}} \sim F_{\text{IDC}} \tan \delta_{\text{IDC}}. \quad (6)$$

If the capacitances of each element are known (see Sec. V), then from these three equations, and using the fact that $F_{\text{PPC}} = 1$, we can solve for $\tan \delta_{\text{TLS}}$. An application of this method is shown in the following two sections, where the loss of an Al$_2$O$_3$ PPC is extracted by measuring, simulating and modeling PPC, IDC, and CPW structures.

V. LOSS PARTICIPATION OF LUMPED ELEMENT INDUCTOR AND CAPACITOR

The inductor design is simulated in Sonnet (see Appendix B) with a varying LE capacitance $C_C$ in order to extract the resonance frequency $f_0$. The frequency response is given by:

$$f_0 = \frac{1}{2\pi \sqrt{L(C_C + C_L)}}. \quad (7)$$

This equation is used to extract the inductance $L$ and capacitance $C_L$ of the inductor. It is possible to engineer the inductor to minimize $C_L$ and maximize the participation of the capacitor, thus increasing the accuracy of the single measurement technique (see Appendix C for examples). Simulated values for measured resonators in this experiment are given in Table I.

The capacitances of the experimental Al$_2$O$_3$ PPC and planar IDC are determined by taking the measured resonance frequencies of a series of resonators of each type and solving for the capacitance of the capacitor, $C_C$ in the model above, where $L = L_{\text{offset}} + L_{\text{arm}}N$, and
\[ C_L = C_{L,\text{offset}} + C_{L,\text{arm}}N \]

\[ L \text{ and } C_L \text{ are determined by} \]

Sonnet simulations of an LE resonator with varying \( C_C \)

and number of inductor arm pairs \( N \). \( C_C \) is then
determined by comparing measured resonance frequencies to

Eqn. \[ \text{[7]} \]

Note that we find a residual \( N \)-dependent component

when performing this comparison, which acts as a
correction term within \( C_{L,\text{arm}} \). We attribute this to a

slight difference between the simulated and fabricated inductor

design; the simulated inductor arms have square corners in order to reduce simulation complexity, whereas

the fabricated inductor arms have rounded corners in order
to prevent current crowding.

Using this method with simulated values described in

Sec. \[ \text{V} \]

we obtain the \( C_C \) values shown in Table \[ \text{I} \]

for the PPC. We are able to perform the calculation above due
to the assumption that the PPC introduces negligible

ductance to the circuit. For the IDC, it is more accurate
calculate \( C_C \) analytically.\[ \text{[21]} \]

VI. TLS LOSS MEASUREMENTS

An LE PPC resonator, LE IDC resonator, and CPW

resonator are measured on three separate chips during

three separate cooldowns to 100 mK in an adiabatic de-

magnetization refrigerator. Device details are shown in

Table \[ \text{I} \]

Fig. \[ \text{2} \]

shows loss \( \tan \delta \) as a function of number of photons \( \langle n \rangle \)

for these measurements. Each data point is
determined by fitting an \( S_{21} \) frequency sweep to the

inverse \( S_{21} \) resonator model.\[ \text{[22]} \]

Fits to the TLS loss model in

Eqn. \[ \text{[2]} \]

are shown as solid lines.

From these measurements, we obtain the loss values in

Table \[ \text{I} \]

Using Eqns. \[ \text{[4]} \] \[ \text{[5]} \] \[ \text{[6]} \] and \[ \text{[7]} \]

we obtain an inductor loss of \( F_L \tan \delta_L = 9.19 \times 10^{-6} \)
as well as a loss for the

\( \text{Al}_2\text{O}_3 \) PPC of \( 1.02 \times 10^{-3} \).

This loss includes both the interface loss of the \( \text{Al}/\text{Al}_2\text{O}_3/\text{Al} \) interfaces as well as the

bulk sputtered \( \text{Al}_2\text{O}_3 \) loss. Due to the high vacuum in

situ growth of the trilayer, we assume that the interfaces

are much less lossy than the bulk, and thus the loss is

largely a representation of the sputtered \( \text{Al}_2\text{O}_3 \) loss.

We can compare the extracted PPC value above to the

value from measuring the PPC LE resonator and assuming

all loss is due to the PPC, \( F_A \tan \delta_A = 9.15 \times 10^{-4} \).

This application of the single measurement technique

gives an 11% difference in reported loss compared to di-

electric loss extraction.

VII. COMPARISON TO THE SINGLE MEASUREMENT

TECHNIQUE

A simpler and more commonly used method of deter-

mining TLS loss of a component of interest is to measure

a resonator with that component included in it, say, as

the capacitor, and then assigning all measured loss to

that component; i.e., the single measurement technique.

The fractional difference between the total loss of the res-

onator \( \tan \delta_{\text{tot}} \) and the loss of the component of interest

\( \tan \delta_C \) is the error in the single measurement technique:

\[ \sigma_{\text{err}} = (F_{\text{tot}} \tan \delta_{\text{tot}} - F_C \tan \delta_C)/F_{\text{tot}} \tan \delta_{\text{tot}}. \]  

The magnitude of \( \sigma_{\text{err}} \) depends on the participation ratio

of the component of interest, as well as the losses of the

component and the total resonator.

The dielectric loss extraction performed in this paper

uses losses in the mid- to high-range (\( 10^{-5} \) to \( 10^{-3} \)) and

an inductor with a participation ratio of 0.102 and two

orders of magnitude lower loss than the capacitor. In this

regime we can achieve an increase in accuracy of 0.11 by

implementing the dielectric loss extraction method over

the single measurement technique.

An outline of the various error regimes is shown in

Fig. \[ \text{3} \]

Fig. \[ \text{3} \] (a) shows the effect of mismatched losses

in the capacitor and inductor when \( C_L/C_{\text{tot}} = 0.102 \), as

in this paper. When the capacitor is much lossier than

the inductor, \( \sigma_{\text{err}} \) flattens out just above 0.11. In other

words, an inductor with loss \( F_L \tan \delta_L \sim 10^{-5} \) can mea-
sure capacitor loss \( F_C \tan \delta_C \gtrsim 10^{-5} \) with \( \sigma_{\text{err}} \lesssim 0.11 \).

However, when the inductor is lossier than the capaci-
tor, \( \sigma_{\text{err}} \gg 0.1 \) and the single measurement technique is

no longer valid. In this regime, dielectric loss extrac-
tion would need to be performed, or \( C_L/C_{\text{tot}} \) would need

to be decreased significantly by modifying the resonator

design. The effect of this design modification is shown in

Fig. \[ \text{3} \] (b). A decrease of the participation loss of the

inductor to below 0.01 would need to occur in order to

measure capacitor losses significantly lower than the in-
ductor loss with an error of 10% or lower using the single

measurement technique.

The grey boxes in Fig. \[ \text{3} \]

show the regime where we

are able to measure low loss materials accurately with-

out the use of the dielectric loss extraction method. A

low loss and/or low participation inductor design is re-

quired. Appendix \[ C \]

illustrates possible modifications to

the resonator design and their effects on participation ra-
tios, while reducing the inductor loss can be attempted

through nanofabrication techniques such as surface nitri-
dation or using higher quality liftoff films.

VIII. CONCLUSION AND NEXT STEPS

In conclusion, we demonstrate a method of TLS loss

extraction by measuring a lumped element resonator fab-

ricated from a superconductor-dielectric-superconductor

trilayer. We extract the dielectric loss by comparing to
coplanar waveguide resonators and lumped element res-
onators with interdigitated capacitors. When demonstrat-
ing this method using measurements of resonators on a

sputtered \( \text{Al}/\text{Al}_2\text{O}_3/\text{Al} \) trilayer, the TLS loss of

sputtered \( \text{Al}_2\text{O}_3 \) is shown to be \( 1.02 \times 10^{-3} \). We see a dif-
ference of 11% between estimated and extracted values. This

difference increases significantly with decreasing loss

in the material of interest, requiring the use of dielectric

loss extraction or specialized device design for materials

losses of \( 10^{-6} \) or lower.

Next steps include extracting interface loss and bulk di-

electric loss independently in a parallel plate capacitor by

measuring a series of parallel plate capacitor lumped el-

ement resonators with varying capacitor dielectric thick-
nesses, as well as performing design modifications to op-
timize the accuracy of the single measurement technique.
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SUPPLEMENTARY MATERIAL

Appendix A: Resonator Geometry and Fabrication

Three resonator types are measured in this work: floating LE resonators with PPCs, floating LE resonators with IDCs, and hanger-geometry λ/4 CPW resonators. All measured resonators are patterned on the same Si wafer. This wafer is initially sputtered with an Al/Al₂O₃/Al trilayer. Details can be found in the main text.

All patterning is performed with a Heidelberg MLA 150 maskless aligner. First, the top Al is wet etched with Transene Al Etchant Type A. Then Al₂O₃ is etched with phosphoric acid. The bottom Al is removed using Transene A. A wet-etched undercut is performed on the bottom Al layer with Transene A in order to prevent the top and bottom Al capacitor plates from shorting. Finally, a liftoff of 350 nm Al is used to connect to the top capacitor plate and define the inductor and feedline.

The PPC is designed to be 20 µm x 20 µm in size, with a capacitance of 727.7 fF determined by comparison between Sonnet simulation and measured resonance frequencies (see Sec. V in the main text for more details). The inductor is 15 µm in width with a gap between inductive arms of 30 µm and a ground gap of 5 µm. Each chip contains six multiplexed resonators and coupling gaps range from 3 to 30 µm for measured normalized coupling quality factors $Q_c$ from 50,000 to 2,000,000 in order to ensure critical coupling at several orders of magnitude of $Q_c$. Coupling is purely inductive due to the symmetric nature of the inductor design. Inductor lengths vary in order to vary resonator frequency for multiplexing purposes, with the lowest frequency resonator having an inductor with $N = 17$ arms on each side of length 147.5 µm, and the highest having an inductor with $N = 7$. Each inductive arm adds capacitance $C_{L,arm} = 2.614$ fF to the resonator, determined in Sec. V in the main text.

The IDC design has 20 fingers of width 5 µm and spacing 5 µm, with a measured capacitance of 316.5 fF (see Sec. V for more details). CPWs have conductor width 5 µm and gap 5 µm, with coupling arms of lengths 150 to 400 µm and a constant coupling gap of 25 µm.

Appendix B: Simulation and analysis of the inductor

Table S1 shows parameter values for inductors with number of arm pairs ranging from 7 to 17. The simulated resonators are composed of a lumped element inductor with the same geometry as in the design described in Appendix A, but with square corners rather than rounded in order to decrease simulation time. A lumped element capacitor of variable capacitance is connected to each end of the inductor, and the inductor is coupled to the feedline with a coupling gap $g_c = 3$ µm.

| $N$ | $L$ (nH) | $C_L$ (fF) |
|-----|----------|------------|
| 7   | 1.06     | 37.5       |
| 9   | 1.33     | 46.4       |
| 11  | 1.60     | 55.4       |
| 13  | 1.87     | 64.3       |
| 15  | 2.15     | 73.3       |
| 17  | 2.42     | 82.2       |

FIG. S1. Resonance frequency $f_0$ of simulated LE resonator as a function of lumped capacitance $C_L$ for a range of number of inductor arms $N$. Open circles represent simulation results, and solid lines represent the fit to Eqn. 7 in the main text.

Inductance $L$ and stray capacitance $C_L$ are first calculated by determining the simulated resonance frequency of the resonator design at a variety of values of lumped element capacitance, and then fitting to the model in Eqn. 7 in the main text (Fig. S1). Then, a corrective term is added to $C_L$ from comparison to measured frequencies of a six-resonator LE PPC chip with $g_c = 3$. These values are used in the main text to perform dielectric loss extraction.

Appendix C: Inductor Loss Parameter Space

If the stray capacitance in the inductor were reduced by more than an order of magnitude, a significant decrease would be seen in the estimation error of measuring a PPC LE resonator design only (Fig. B(a)). Geometric parameters can be modified within the inductor design in order to attempt to lower the capacitance of this element. The ground gap, coupling gap, and number of inductor arms were all studied using lumped element resonator simulations in Sonnet to determine their effect on the total capacitance of the lumped element inductor.

Simulations show that varying the gap between the inductor and ground planes between 2 and 10 µm has very little effect on total capacitance of the inductor (Table S2), as does varying the coupling gap from 3 to 30 µm (Table S3). However, the number of arms of the inductor could be decreased (and the size of the parallel plate
Appendix D: Variation of Resonator Performance

High power and low power loss measurements can vary significantly between resonators on a single die, as well as for a given resonator in subsequent cool-downs. In order to measure TLS loss with uncertainty less than this variation, a large set of resonators must be measured and their TLS loss averaged to determine each TLS loss value. Then these measurements can be used to perform dielectric loss extraction. Based on the work of Calusine et al., around 15 resonators should be measured, and the results averaged to determine the TLS loss value for a single resonator design.

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