Tolerance analysis of a GFET transistor for aerospace and aeronautical application

P Lamberti¹, M La Mura¹, F Pasadas², D Jiménez² and V Tucci¹

¹ Dept. of Information and Electrical Engineering and Applied Mathematics, University of Salerno, Via Giovanni Paolo II, 132, Fisciano (SA), Italy
² Departament d’Enginyeria Electrònica, Escola d’Enginyeria, Universitat Autònoma de Barcelona, Bellaterra 08193, Spain

mlamura@unisa.it

Abstract. Due to the high carrier mobility, graphene is considered a promising material for use in high-speed electronic devices in the post-silicon electronic era. Graphene high resistance to radiation and extreme temperatures makes the development of graphene-based electronics a key-enabling technology for aerospace, defence, and aeronautical applications. Nevertheless, achieving uniform device-to-device performance is still a challenge, and these fields require high reliability components. In particular, many critical issues remain to be solved, such as their reproducibility and guaranty of identical performances against possible variations of different manufacturing and environmental factors. In the present work, a model capable to take into account the physical characteristics linked to the production process of a Graphene Field-Effect Transistor (GFET) is exploited to carry out a tolerance analysis of process-related geometrical parameters on the device performance. The most influential parameters that affect the device behaviour are studied in order to enhance the fabrication yield.

1. Introduction

Graphene’s unique properties of high carrier mobility, thermal efficiency and atomic thickness make it, in theory, the perfect channel material for the Field-Effect Transistor (FET), capable of opening new frontiers in the improvement of FETs’ miniaturization, energetic efficiency, and performance upgrade [1,2]. In fact, graphene and graphene-related materials (GRM) were included in the International Technology Roadmap for Semiconductors first [3], and in the International Roadmap for Devices and Systems later [4].

The development of high-performing RF electronic devices [5] is a matter of great interest for aerospace and aeronautical applications, due to the appealing possibilities enabled by nanoelectronics. For what concerns the aerospace field, the recent 2020 NASA Technology Taxonomy [6] frequently refers to graphene, confirming the material is a main actor on the scene of avionics component technology research, especially due to the property of being highly radiation resistant/tolerant and temperature tolerant. Further, graphene is much likely to be involved in the development of nano-scale sensing devices for in-situ structural health monitoring systems, photon sources for miniature spectroscopy tools, tunable THz sources, nano-fluidics systems [7–9]. Finally, both the aerospace and
the aeronautical field would take great advantage of the mass saving enabled by nanodevices, which are characterized by very small features and light weight. Nevertheless, both fields require that devices have reliable performance standards and good robustness to failures. To meet these goals, the repeatability of the manufacturing is a key-aspect. Unexpected variations of process-related parameters can affect the evenness of the fabricated devices characteristics, leading to non-uniform performance [10]. For instance, tolerance on the layout geometry largely affects the device performance. Also, the carrier mobility in the graphene channel varies due to the unintentional doping caused by grain boundaries and surface contaminants in the deposition of large-scale graphene by CVD.

Performing a sensitivity analysis to investigate the relation between the variability of selected output performance indicators and the variability of process-related parameters allows both computing the performance unevenness we should expect from the fabricated devices and assessing which are the most influential parameters [11–13]. By knowing which of the process variables can have the most detrimental effects on the quality of the device behavior, process engineers can optimize the fabrication process by improving the accuracy of the most effective parameters.

For these reasons, in this work we propose the sensitivity analysis of some interesting figures of merit describing the GFET RF performance [14], namely the device differential output conductance $g_{ds}$ and the transconductance $g_{m}$. In this preliminary study, the process parameters considered are the lateral dimensions of the channel, $W$, $L$, and the top oxide thickness $t_{ox}$. The assessment of the impact of such process parameters tolerance on selected performance indicators was carried out by applying sensitivity analysis techniques to a GFET voltage amplifier in Common-Source configuration, simulated by using the transistor Verilog-A model described in [15] in order to provide a tool to support the optimization of graphene-based RF devices design and production.

2. Design of Experiments approach for the tolerance analysis of a GFET

Three geometrical parameters affected by uncertainty were considered as input factors of the tolerance analysis: the GFET channel length $L$, the channel width $W$ and the top oxide thickness $t_{ox}$. The selected output performance indicators were computed in correspondence of different combinations of the input parameters. Such combinations are selected according to a 3-factors 3-levels full factorial Design of Experiments (DoE) approach [16]. This approach allows assessing the variability of the output quantities while accounting for simultaneous variations of all the considered input parameters, which are instead neglected in the classical “one-factor-at-a-time” method to the sensitivity analysis. The factors were assumed affected by a 10% tolerance around their nominal value. The vertex analysis technique [17,18] was applied to define the input sets for the simulations: each factor was considered equal to its minimum and maximum value. Further, the center value (i.e. the nominal value) was also included to assess the linearity of the performance variation dependence upon the variation of factors within the considered range. The simulation outcome was analyzed by graphical investigation by means of the Dex Scatter Plot and the Main Effect Plot [19], and the first-order sensitivity coefficients were computed.

2.1. Input parameter space

As previously mentioned, the simulation settings were designed according to a 3-factors 3-levels full factorial DoE. The array of the input factors is therefore $x = [x_1, x_2, x_3] = \{x_i\}$. Each of these factors has a nominal value $x_{i,n}$ and is a stochastic variable uniformly distributed across an interval ranging from a minimum value, $x_{i,L}$, to a maximum value, $x_{i,U}$. The input parameter space with $m = 3$ factors is therefore defined by the compact $D = [x_{1,L}, x_{1,U}] \times [x_{2,L}, x_{2,U}] \times [x_{3,L}, x_{3,U}]$. By assuming that each process parameter $x_i$ can be realized with a tolerance $\Delta_i$ equal to the 10% of its nominal value $\Delta_i = 0.1x_{i,n}$, the minimum and maximum values of each factor are defined by $x_{i,L} = x_{i,n} - \Delta$ and $x_{i,U} = x_{i,n} + \Delta$.

According to the vertex analysis technique, if the variation of the observed performance is linear with the factors variation within the range $[x_{i,L}, x_{i,U}]$, computing the output in correspondence to the minimum and maximum values of each factor (i.e. the vertices of the hypercube $D$) returns the first-
order sensitivity coefficients $\beta_i$ and the interaction coefficients $\beta_{ij}$ that can be used to predict the performance according to the model

$$y = y_0 + \sum \beta_i x_i + \sum \beta_{ij} x_i x_j + \epsilon, \quad i \neq j$$

in which $y_0$ is the considered output performance parameter $y$ computed by considering the nominal set of input parameters, and $\epsilon$ is the error due to the non-linearity.

By assuming that the interactions between the factors and the error are negligible, and considering the case of $m = 3$, equation (1) becomes

$$y \approx y_0 + \beta_1 x_1 + \beta_2 x_2 + \beta_3 x_3$$

and the sensitivity coefficients $\beta_i$ can be computed from the simulation results by using

$$\beta_i = \frac{\partial y}{\partial x_i} \approx \frac{\Delta y}{\Delta x_i}$$

in which the performance variation is the difference $\Delta y = (y_{avg}^U - y_{avg}^L)$ and the input variation is $\Delta x_i = (x_{i,U} - x_{i,L})$, with $y_{avg}^U$ and $y_{avg}^L$ output mean value obtained in correspondence of the upper and lower value of the $i$-th input factor $x_{i,U}$ and $x_{i,L}$, respectively.

Nevertheless, the linearity of the performance dependence upon each factor needs to be assessed before the interaction effects and the error can be neglected. Therefore, it is useful to add the center point $x_{i,n}$ of the input variation interval to the vertex analysis.

For this reason, in the proposed analysis each of the $m = 3$ factors varies within the 10% tolerance range taking $l = 3$ values $x_i = [x_{i,L}, x_{i,n}, x_{i,U}]$, making for $n_c = l^m = 27$ parameters combinations provided to the simulator. Figure 1 shows the points representing the considered combinations of the factors spatially placed in the 3-factors parameter space.

![Figure 1](image.png)

Since the geometric tolerances are non-negligible in large-scale graphene deposition during the GFETs fabrication, the three factors considered are the GFET channel length $L$, the channel width $W$ and the top oxide thickness $t_{ox}$. The minimum, nominal and maximum values for $L$, $W$ and $t_{ox}$ are listed in Table 1. The nominal set of parameters refers to the design described in [20].

| Factor $x_i$ | Minimum value $x_{i,L}$ | Nominal value $x_{i,n}$ | Maximum value $x_{i,U}$ |
|--------------|-------------------------|-------------------------|-------------------------|
| $L$          | 450 nm                  | 500 nm                  | 550 nm                  |
| $W$          | 27 μm                   | 30 μm                   | 33 μm                   |
| $t_{ox}$     | 3.6 nm                  | 4 nm                    | 4.4 nm                  |
2.2. Performance indicators

The main figures of merit for analogic circuits in RF operation are the device differential output conductance $g_{ds}$, the transconductance $g_m$, the ac voltage gain $A_v$, the cut-off frequency $f_T$ (at which the current gain drops below unity), and the maximum oscillation frequency $f_{\text{MAX}}$ (at which the power gain drops below unity) [14].

In this work, we perform the sensitivity analysis of $g_{ds}$ and $g_m$ as defined by

\[
\begin{align*}
g_{ds} &= \frac{\partial I_{DS}}{\partial V_{DS}} \quad \text{(at constant $V_{GS}$)} \\
g_m &= \frac{\partial I_{DS}}{\partial V_{GS}} \quad \text{(at constant $V_{DS}$)}
\end{align*}
\]

(4) (5)

to the input factors variation within their tolerance range. The $g_{ds}$ is important because the smaller is the output conductance, the higher is the amplifier voltage gain. In order to increase the $g_{ds}$, the Drain current saturation must be improved. The $g_m$ also is of great importance, because the voltage gain is proportional to the transconductance, too. Moreover, the higher is $g_m$, the better is the Gate control over the Drain current. The criterion for the choice of the GFET bias point was to compute the small-signal parameters $g_{ds}$ and $g_m$ around the DC bias point that returned the maximum DC voltage gain.

2.3. Large-signal GFET model

The model used to perform the circuit simulations is the charge-based intrinsic capacitance model for large-signal operation of GFETs described in [15]. Contrary to common Meyer-like capacitance models, charge-based models ensure charge conservation. Further, featuring non-reciprocal capacitances enables a higher accuracy in the modelling of the high-frequency behavior of the device. The model describes the intrinsic GFET behavior by relying on the drift-diffusion theory for the electronic transport. Implemented in Verilog-A, this model is compatible with many of the most common circuit simulators.

2.4. The simulated GFET device

The simulated device was described in [20] as the first high-frequency voltage amplifier obtained by using large-area CVD-grown graphene. The transistor owes its ac voltage gain to the clear current saturation, achieved by means of an ultra-thin gate dielectric [21]. The GFET was simulated as a general purpose Common-Source amplifier, which is a main “building block” of all RF electronic circuits. The bias point is set by means of a bias-tee, and lumped resistors are connected to the terminals to account for the contact resistances, which, at this step of the work, are considered fixed. Figure 2 shows the schematic of the simulated circuit. The Drain and Source resistance is $R_D = R_S = 435 \, \Omega/\mu\text{m}$ and the Gate resistance is $R_G = 14 \, \Omega$, and the physical constants input to the Verilog-A model are set as in [22].

![Figure 2. The schematic of the GFET Common-Source amplifier adopted for circuitual simulation.](image-url)
3. Biasing of the GFET
The computation of the performance parameters $g_{ds}$ and $g_m$ is performed by assuming a linear variation of the input voltage around a fixed bias point, that must be chosen according to a given criterion. For example, we chose to compute the device $g_{ds}$ and $g_m$ by differentiating the drain current $I_{DS}$, and to find the couple $(V_{GS}, V_{DS})$ that gave the highest DC voltage gain, as defined by

$$A_{DC} = g_m g_{ds}^{-1}.$$  

(6)

The maximum voltage gain bias point is strongly dependent on the device geometry. For this reason, devices with structural dimensions slightly different from the nominal value (due to the process parameters tolerance) biased at the nominal optimum bias point will exhibit amplification properties worse than expected. By biasing the GFET at the point that is optimal for the voltage gain maximization as found for the geometrical parameters nominal set, the assessment of the amplification performance variation can quantify the impact of the process-related parameters tolerance.

3.1. DC output characteristic and transfer curve
The drain current was simulated by considering a Drain-Source voltage $V_{DS}$ sweep from $-1.5$ V to 0 V. This GFET exhibits clear current saturation in a small range of $V_{DS}$ values depending on the applied Gate-Source voltage $V_{GS}$. Saturation occurs in correspondence of negative $V_{GS}$ values higher than $-0.6$ V. The $I_{DS}-V_{DS}$ curves are shown in Figure 3.

The so-called “kink” in the I-V curves observed by increasing $V_{DS}$, where the current saturates before developing in a second linear phase, is frequently observed in graphene-based transistors and is due to the polarity shift of carriers. This behaviour is a consequence of the GFET ambipolar nature and can be clearly observed in Figure 3.

Figure 4 shows the transfer curves $I_{DS}-V_{GS}$, computed by varying $V_{GS}$ from $-0.6$ V to 0.6 V for different values of $V_{DS}$, ranging from $-1.4$ V to 0 V in steps of 0.2 V. The shift of the Dirac voltage ($V_{GS}$ at the minimum conductivity point) described in [20] can be clearly observed.

These plots validate the simulations, since the curves are in good agreement with the results described in [22] and with the experimental characterization in [20].

![Figure 3. The DC output characteristic $I_{DS}-V_{DS}$ for different $V_{GS}$ values. The output current $I_{DS}$ is normalized with respect to the channel width $W$.](image)

![Figure 4. The DC transfer curve $I_{DS}-V_{GS}$ for different $V_{DS}$ values. The output current $I_{DS}$ is normalized with respect to the channel width $W$.](image)

3.2. Output conductance and transconductance
The output conductance $g_{ds}$ and transconductance $g_m$ curves were obtained by computing the first derivative of the Drain current curves shown in figure 3 and 4, and according to equations (4) and (5), respectively. The results are reported in figure 5 and figure 6.

Figure 5 shows that, for certain bias voltage values, the $g_{ds}$ has a well-defined peak towards zero, reaching values as small as 0.03 mS. This confirms that the saturation of the drain current is particularly clear under certain conditions.
Figure 6 highlights that the $g_m$, that peaks when the variation of the output current is more consistent in response to the input voltage variation, increases by increasing the Drain voltage, thus improving the Gate control over the current. The highest $g_m$ obtained from the simulation is 36.8 mS.

Figure 5. The output conductance $g_{ds}$ computed by differentiating the $I_{DS}-V_{DS}$ curve of Figure 3.

By computing the DC voltage gain according to equation (6), the optimal bias point chosen as the bias leading to the highest voltage amplification in static condition was found at $V_{GS} = -0.2$ V and $V_{DS} = -1.2$ V.

4. Tolerance analysis of the GFET

The output conductance and the transconductance for the considered GFET device were computed by varying the factors $L$, $W$ and $t_{ox}$ according to the DoE proposed in section 2.1. The results were used to assess the impact on the Drain current saturation (described by the $g_{ds}$) and the Gate control capability (described by the $g_m$) of the input parameter variation within the assumed tolerance range. The effect of each factor was quantified by means of the first-order sensitivity coefficients computation, as described by equation (2). If the performance variation upon the three factors is linear, the expected output variability for input parameters variations smaller than 10% of their nominal value can be computed according to

$$\Delta y \approx \beta_1 \Delta x_1 + \beta_2 \Delta x_2 + \beta_3 \Delta x_3$$

4.1. Output conductance sensitivity

The value of output conductance obtained in correspondence of the nominal set of input parameters is $g_{ds,n} = 0.021$ mS/μm.

The Dex Scatter Plot (DSP) in Figure 7 shows the distribution of the $g_{ds}$ values obtained for the 27 input sets considered according to the DoE, with respect to each factor’s settings. By observing the minima and maxima trend, it can be noticed that the dependence of the $g_{ds}$ upon all three factors variation is non-linear in the investigated range. Hence, the computation of the expected variability of the performance by means of the first-order sensitivity coefficients, reported in red in Figure 8, cannot be done by equation (7) because the nonlinearity error is not negligible.

The Main Effect Plot (MEP) in Figure 8, traced by connecting the mean values of the performance as obtained in correspondence of the lowest and highest setting of each factor, assesses that the geometrical parameter most effective on the output conductance is the channel length $L$. Nevertheless, the dependence on $t_{ox}$ is also appreciable. The parameter $W$ is the least influential on the $g_{ds}$. Figure 8 also reports the percentage variation with respect to the nominal value $g_{ds,n}$ caused by each factor’s variation within the considered 10% tolerance range.
4.2. Transconductance sensitivity

The transconductance computed by using the nominal set of input parameters is \( g_{m,n} = 1.086 \) mS/\( \mu \)m.

By observing the DSP in figure 9, it can be seen that the \( g_m \) dependence upon all three factors is linear, and therefore the slopes of the lines connecting the performance mean values at the low and high setting of the factors, shown in figure 10, accurately represent the \( g_m \) sensitivity with respect to \( L \), \( W \) and \( t_{ox} \). The greater performance location shift is caused by the channel width \( W \), which generates a \( g_m \) variation of 12.1\% with respect to the \( g_{m,n} \), and is therefore the most influential parameter. Nevertheless, the variation induced by the other two factors is within the same order of magnitude. Thus, none of the three factors can be neglected in the optimization of the fabrication process.

5. Conclusions and future work

A tolerance analysis was performed by simulating a GFET voltage amplifier in Common-Source configuration, with the aim of assessing the impact of a 10\% tolerance of process-related geometrical parameters, i.e. the channel length \( L \), the channel width \( W \) and the top oxide thickness \( t_{ox} \), on the device performance. The simulations, run on a large signal GFET model, were performed by setting the input parameters combination according to a 3-factors 3-levels full factorial Design of Experiment approach. After choosing the optimal bias point for the considered device (\( V_{GS} = -0.2 \) V, \( V_{DS} = -1.2 \) V), the first-order sensitivity coefficients and the percentage variation with respect to the nominal \( g_{ds} \) and \( g_m \) were computed in response to the variation of each input factor. The most effective parameter on the \( g_{ds} \) at the considered bias point is the channel length \( L \). For what concerns the \( g_m \), it is mostly affected by the channel width \( W \), though \( L \) and \( t_{ox} \) also affect the transconductance in a non-negligible way.

The proposed method can be applied to find the most influential parameters that affect the device behaviour and the issues to address in the view of improving the fabrication yield. Finally, this analysis also returns a mathematical representation of the performance variability with respect to the factors’ variation. In the next future, the effect of the process parameters variation on other performance parameters useful for the assessment of the GFET RF performance, such as the low-frequency AC...
voltage gain, the cut off frequency and the maximum oscillation frequency, will be assessed. Furthermore, the impact of other process-related factors such as the contact resistance and the graphene mobility will be investigated.

Acknowledgments
This project has received funding from the European Union’s Horizon 2020 research and innovation programme Graphene Flagship under grant agreement No 881603.

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