A Novel Low Noise Instrumentation Amplifier for Bio-Medical applications

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Abstract: In this work we propose an efficient and a novel Instrumentation amplifier design fabricated using CMOS technology that can be used for the amplification of bio-medical signals. Instrumentation Biological amplifiers play a crucial role in biomedical devices like hearing aids, pacemaker etc. An instrumentation amplifier with current feedback and Current re-use topology along with the Chopper Offset-stabilization technique which was used in op-amps will also be extended to current-feedback instrumentation amplifiers, will help us to minimize and eliminate the flicker (1/f) noise and the offset voltages that will occur during the design of the feedback amplifiers. The gain mismatch problems that usually occurs due to the use of Current re-use topology was also minimized by the use of dynamic element matching technique that will be described in the paper. The design is simulated using Cadence Spectre tool. The Instrumentation amplifier final layout is designed in Cadence Layout editor with 0.18μm CMOS technology.

Keywords: CFIA, IA, Current Reuse, CMRR

1 Introduction

In Recent years MEMS sensors have gained huge popularity and used in various applications like compact anemometers, biological ventilators development, industrial process, and aerospace thrusters. Growth of Integrated circuits design with CMOS transistors and MEMS concepts helped us to design instrumentation amplifier [6] (IA) with high gain, CMRR and also with less noise and low power. The mandatory part involved in the instrumentation amplifier design is improving the gain to high scale and CMRR according to the size of transistors. We have selected an efficient and an appropriate operational amplifier circuit topology and an optimum CMOS transistor sizing for improving the gain margin to the desired level of applications mentioned above and common mode rejection ratio for using the instrumentation amplifier in EMG, ECG and EEG applications.

Figure 1: MEMS Flow sensor
There are different techniques like level shifting, cascading and multistage amplifiers are consider majorly to improve gain, CMRR with the reduction of power consumption. We have tabulated for existing amplifiers by using power, dc gain, noise, and bandwidth are carried out in this paper. This is followed by a single operational amplifier which is configured as a differential amplifier. Finally, the use of feedback instrumentation amplifiers with current-reuse technique have been excellent methodology in order to obtain a high CMRR. This paper describes area effective Chopper-Offset-Stabilization techniques which [9] was used in designing of op-amp also it will broadened towards current-feedback instrumentation amplifiers [CFIA].

2 Effective methods to reduce Common mode voltages and Offset in Instrumentational amplifier design

2.1 Using Folded Cascade Structure

Common mode voltages that occur in designing an instrumentation amplifier are of huge concern. The interferences which will be generated has to be thus reduced in order to improve the gain. In order to mitigate it, a conventional 3-stage instrumentation amplifier are now used in design configuration such that, input stage have two op-amps [10] and at output stage have cascaded operation amplifier design. Below Figure (2) represents the use of the Cascade structure in order to reduce the Common mode voltages and the offset that usually will arise during the design of amplifiers.

![Figure 2: Folded Cascode circuit](image)

The Main advantage you get with the effective usage of 3 stage amplifier methodology is considerably good gain and very high CMRRR and controlling of gain by altering the value of only one resistance. But disadvantage is that use of different resistances leads to increased chip die area of this type instrumentation amplifier, due to the.

2.1 Using Dynamic Offset Cancellation

When the CMOS based Op-amp amplifier are designed at very low frequencies the main sources of noises are offset noise, flicker, and drift noise. Few novel techniques are used to minimize the noise sources such as the offset topology and drift methodology using chopping technique, trimming and auto-zeroing (AZT) method. The process of trimming is usually done at the initial phases which helps to remove the offset voltage.

\[ V_{n}^{2} = \frac{k}{W L C_{aux}}(1) \]
Finally, in chopping Technique[3] chopper ripples are produced at the output of amplifier circuit, by modulation in CT domain, the input signal and the offset voltages are modulated to various other frequency levels.

When we use the different variations in offset cancellation topologies like stabilized chopper methodology and auto-zeroing technique, topologies mentioned in [4-5] we will achieve significantly very low input voltage noise, high CMRR and low input offset voltage as well. When these structures are implemented with exactly the same offset compensation techniques and with less variation in their topologies, we are able to high gain at the amplifier output stage.

3 Conventional CFIA [Current feedback Instrumentation amplifier]

CMOS Instrumentation Amplifier (IA) can be implemented using various topologies. Diagram shows a functional overview of CFIA. In the feedback amplifier design using the input trans-conductor (gm,in), the differential current [I-in] is found out by modifying the differential input signal (Vin). The feedback voltage(V-fb) is applied at end stage as a differential current (I-fb) is generated in the form of feedback trans conductance. The resulting voltage got from the output design is a attenuated form of final output signal (Vout). When we consider the case of the ideal Op-amp’s, where Vin+-Vin- = 0 and this actually means that the input differential signal at the circuit beginning section and the output differential signals at the end section are equal to null value.
4 Proposed Technique

A Fully-differential CR- CFIA has been used in Bio-medical applications [7]. The Transconductance \([Gm1-Gmfb\ stage]\) was cascaded, and thus its named CR topology. The Transconductance \(-Gm2\) stage is also connected to Current re-use topology. The feedback topology used here in Common Mode which is presented in the both circuits to make sure that output CM voltage (VCM) is also stable. Dynamic element Matching [DEM] technique was used in order to minimize the gain mismatch problem due to P-MOS and NMOS that will be cascaded in CR topology. The problem of modulation effects were minimized in Chopper stabilization technique to the required signal of considerably larger frequency where, there will be less 1/f noise. At the back end efficient demodulation technique are used to convert the desired noise affected signal back to base-band gain after amplification process. In this paper we have presented an efficient CMOS low noise amplifier (LNA) that can be used in low-power ultra-wideband wireless applications. In wearable biomedical usage for obtaining less power usage and considerable bandwidth , the design uses a CR methodology and a High Pass that will be used along with the circuit. The design was fabricated in CMOS technology 0.18-\(\mu\)m and it shows a [3.7–11.2 GHz] Bandwidths.

\[
Output\ Voltage\ V_o = \frac{g_{m,\text{in}}}{g_{m,\text{fb}}} \cdot \frac{R_1 + R_2}{R_2} \cdot V_{\text{in}} \quad (2)
\]

4.1 Current Re-use mechanism

We can Obtain a considerably lower input-referred voltage noise power density with an efficient design of Current reuse techniques. By the design of the Ultra-wide band Low Noise amplifiers, the current-reuse technique may be the efficient option for providing high gain, less noise figure and also very low power usage. In current-reuse technique the Radio Frequency input signal is amplified by two cascade CS amplifier stages to provide a very high gain , but its also helps to achieve considerably very low noise figures. A high-pass filter is used in the Cascaded input matching circuitry in order to reduce noise level. The transconductance of the input stage \(g_{m1} * g_{m2}\), helps to solve the issue of low transconductance and low gain in CMOS transistor amplifiers when used for LNA applications. But transconductance may be increased, when use same bias current when it used as single source and dissipates considerably more power.

![Current Re-use mechanism](image)

The CR is well known for its use in Low Noise amplifier applications, and its efficiency topology of getting very efficient performance with considerably less power usage that is very lower than regular 2-stage amplifiers with common -source stage that is used for Bio-medical applications.
4.2 Cascoded Gm1 Gmfb Stage

The Current topology with reuse technique will provides the perfect match of very less noise figure, comparatively very high power gain and consumes minimum power which will be ideal option for the usage in Ultra Wide Band Low Noise Amplifier designs and also in Bio-Medical ECG applications. A high gain is achieved in CR techniques with help of the aRadio Frequency signal which will be increased to higher gain stage by the use of two common-source amplifier stages which are cascaded in this architecture.

For using IA’s in Electro-cadiogram applications the frequencies of signals will be in the range of around 100’s of hertz, and minimum level amplitudes values near to millivolt-level [around 1.45 mV at 108 Hz]. The output Gain of Current Reuse -CFIA [7] was defined based on the parasitic component resistances, and was designed for amplification of thirteen times as the incoming signal following ADC input and this ADC is much better than mentioned in [16]. In the proposed block diagram of CR-CFIA topology the supply voltage is around 2.45 V, incoming inputs signal [Vin ±] and the feedback [fb] inputs are given as (Vfb ±) are interchanged by 17 kHz freq of Dynamic element Matching. The frequency of choppers was also set as 8 kHz because the 1/f noise, flicker noise of the Gm1-Gmfb stage of this amplifier was at 8 kHz. And finally the resistances of R1, R3 were 380kΩ, R2 was 40kΩ.

4.3 Chopper feedback stage

Conventional Current feedback Instrumentation amplifier is composed of actually 2 stages and they are affected by noise and offset. We will use the chopper stabilization technique architecture and the auto-zeroing techniques for mitigating these problems. Auto-zero technique has limitation that it causes a switching noise problem when the signal is sampled and it significantly increases the baseband noise due to noise folding.
The chopper stabilization however also has an disadvantage of having a low bandwidth. The chopper stabilization architecture is implemented in the low-frequency path of the operational amplifier. It is then again changed with help of demodulation technique to the odd harmonics of chopping frequency. Spikes of the chopper due to the presence of matching within chopper switches to the parasitic capacitance values and clock lines of the choppers at input and output section, leads to residue-offset voltage which will be around 11v. The chopper clock frequency is directly proportional to this offset voltage so it can be reduced [6,24], but it cannot be further minimized below the flicker-noise corner. Thus the noise can’t be eliminated if we reduced lower than the center frequency of flicker noise and can be fully resolved by eliminating the spikes only.

Thus we also presented completely different variant of chopper switching topology which will work in a lower carrier frequency circuit to reduce the offset range. Also the fast chopping action can also be used eliminate the flicker-noise and DC offset which will be arise in the Instrumentation amplifier design.
Table 1. Performance Analysis of CR-Chopper Offset-stabilization

| Parameters          | [2]     | [6]     | [8]     | This work |
|---------------------|---------|---------|---------|-----------|
| Process             | 180 nm  | 180 nm  | 65 nm   | 180 nm    |
| Power (μW)          | 864     | 920     | 652     | 634       |
| Input-referred Noise(μVrms) | 2.8   | 2.8     | 1.9     | 0.32      |
| Area (mm²)          | 0.28    | 0.34    | 0.65    | 0.15      |
| Gain (dB)           | 42-60   | 89      | 90-100  | 50        |
| Bandwidth           | 10k     | 11.8k   | 15.7k   | 14.2k     |
| NEF                 | 1.2     | 1.25    | 1.8     | 1.1       |
| CMRR (dB)           | 100     | 88      | 89      | 105       |
| PSRR (dB)           | 78      | 114     | 132     | 101       |

For the designed Current Feedback Instrumentation amplifier [CFIA] we compare the Gain (dB), Bandwidth, Noise efficient factors, CMEE, PSRR (dB) with already existing methodologies. We find that proposed technique using Current re-use technique had less power and CMRR compare to the existing topologies.

![Figure 10: Input Noise signal vs Frequency values](image)

Thus, the results are tabulated for the number of occurrences Vs Residue offset for the designed amplifier. Current feedback Instrumentation amplifier actually is chopped at the frequency range of 60 kHz to reduce the effect of errors that will be occurring in lower frequency ranges like offset noise and the flicker disturbances during the design of Instrumentation amplifier.

![Figure 11: Residue offset occurrences by using Montecarlo method](image)
5 Conclusion

Since CMOS Instrumentation amplifiers are basic building blocks for most of the electronic circuit applications since it requires very less chip area and comparatively and less power. Proposed Instrumentation amplifiers improves the CMRR and the DC gain, which amplifies the weak signal. The novel technique proposed will comparatively decrease the flicker disturbances, 1/f noise while designing the CMOS instrumentation amplifier that can be used in biomedical applications. We have also reduced the noise of the instrumentation amplifier by using dynamic offset cancellation techniques.

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