Implementation of a pulse generator and pulse width modulation to a three-level diode-clamp inverter as a case study

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Abstract

Three-level diode clamp inverters (DCI) are designed and implemented in this paper using two different switching scheme technologies namely (PG) pulse generator and (PWM) pulse width modulation using Matlab Simulink to make certain the efficiency of this logic control method. The PG is assumed to transmit a precise, stable and accurate square pulse signal. The current PG innovation is too big to be fully encapsulated. Comparative study between the most fitting domination and modification methods sophisticated for these converters PG and PWM are implemented to drive the MOSFET switching device, to make constant high voltage pulses which give a pulse electric range of up to high intensity.

1. Introduction

Many industrial appliances require variable power (medium or low) to operate, and some industries require high power. In recent years, 1975 multi-level inverter (MLI) was introduced as an alternative in high power and medium voltage situations [1]. It converts medium voltage sources (solar cells, batteries, mega capacitors) into high power output; these transformers consist of several switches, diodes, and capacitors [2]. MLI can generate output voltages with significantly low distortion; it can reduce dv/dt stresses and input current draw with low distortion; it can reduce stress in motor bearings because it produces a smaller voltage in Common Mode. It can also operate within the base and the high frequencies of PWM switching. (The lower conversion frequency results in less conversion loss in addition to higher efficiency) [3,4]. Here is a summary of some of the benefits of MLI; as for its drawbacks, the main one is its requirement for many semiconductor switches [5].

Figure 1: Types of MLI
Whereas each drive circuit switch requires a relevant gate which may cause the overall system overhead to increase. MLI is divided into three main types, and each type has some benefits and DE benefits, table 1 and fig. 1.

| Names                          | Advantages                                      | Disadvantages                                      | Applications                                      |
|--------------------------------|-------------------------------------------------|---------------------------------------------------|--------------------------------------------------|
| Diode Clamped Multilevel Inverter | • Capacitance is low  
• Back to back inverters can be used.  
• Capacitors are pre changed.  
• Efficiency is high at fundamental frequency | • Number of clamping diodes increases with the increase of each level.  
• DC level will be discharge when control and monitoring are not precise. | • Static var compensation  
• Variable speed motor drives.  
• High voltage system interconnections  
• High voltage DC and AC transmission lines |
| Flying Capacitors Multilevel Inverter | • Static var  
• For balancing capacitors’ voltage level, phase redundancies are available.  
• We can control reactive and real power flow. | • Voltage control is difficult for all the capacitors.  
• Complex startup  
• Poor Switching efficiency  
• Capacitors are expensive than diodes. | • Introduction motor control.  
• Static var generation.  
• Both AC-DC and DC-AC conversion applications.  
• Converters with harmonic distortion capability.  
• Sinusoidal current rectifiers. |
| Cascade H Bridge Multilevel Inverters | • Output voltage levels are doubled the number of sources.  
• Easy and quick manufacturing.  
• Packaging and layout is modularized.  
• We can control it easily with a transformer.  
• Inexpensive. | • Every H bridge need a separate DC source  
• Due to large number of DC source, applications are limited. | • Active Filters  
• Electric vehicle drives  
• DC power source utilization  
• Power factor frequency link system  
• Interfacing with renewable energy resources |

2. **Diode clamp (DCMLI)**

This inverter uses diodes and supplies multiplied voltage levels out of the various phases to the capacitor banks who are in chain [1,6]. A diode transmits a limited quantity of voltage, that way reducing the strain on other electrical equipment’s. The main drawback is the maximum output voltage is half of the input DC voltage, it can be solved by increasing the number of switches, diodes, capacitors. because of using fundamental frequency for all the switching devices this inverter provides high efficiency and it is a simple method of the back-to-back power transfer systems [7]. The voltage across each switch is \( V_{dc}/2 \) ((\( V_{dc} \)/2) is the voltage of each capacitor). Table 2 shows the switches modes against the magnitude of o/p voltage. Two switches are On for each mode and the other two switches are Off with different o/p. Dc bus voltage share into three levels by Two capacitors C1 and C2 which are connected in series [6,8].

![Figure 2: Sector Divisions of 3 Level DCI](image-url)
The switching modes is to guarantee that switches action in
tangent style. O/p voltage Van has three cases (Vdc/2), (Zero),
(-Vdc/2), Fig. 7. These three cases are achieved when depend-
ing on the newer logic states.

- Upper switches (Mosfet and Mosfet1) are ON and all
  lower switches (Mosfet2 and Mosfet3) be Off to get
  (Vdc/2).
- Switches (Mosfet1 and Mosfet2) be ON, Mosfet and
  Mosfet3 be Off to get Zero.
- Switches (Mosfet2 and Mosfet3) be ON, Mosfet and
  Mosfet1 be Off to get (-Vdc /2).

2.1 Pulse Generators PG

Control strategies in the Matlab program by using the para-
eters in the source block of each switch (amplitude, period,
pulse width, and phase delay) by issuing a square wave at fixed
intervals are called pulse generators [8].
Amplitudes are one for all switches with period 1/f, phase de-
lay and pulse width are changing depending on table 2. As an
example switch 1, is ON in one time Vdc/2 o/p, and at whole
else time is OFF, works of 10% from the life cycle.

Switch 1 works without delay, so phase delay is equal to zero,
and pulse width is equal to 12.5% of the period. Switch 2 works
without delay, so phase delay is equal to zero also. Switch 2 is
two times ON in Vdc/2 and Zero, off for all other times, so
pulse width is equal to 25% of the period and so on for other
switches, Fig. 5&6.

2.2 Pulse Width Modulation PWM

In a pulse generator, there is only one pulse per half-cycle, Fig.
7 (the converter output is controlled by changing the phase de-
lay, period, and pulse width, Fig. 4&6), then the minimal order
harmonic is the third (It's tricky to filter out) [9-11].
Figure 6: Switches Source Block Parameters
In each half cycle, Switches are transitioned On/Off much times, and the output voltage is controlled by changing width of the pulses, these are called a PWM control. Fig. 10. The gateway signals produced by matching a dc signal with a triangular wave [12], Fig. 8. The lower order harmonics can be eliminated by selecting the number of pulses. as a result, growing the number of pulses should also grow the amount of the higher-order harmonics, then it's easy to be filtered.

Inverters established with a PWM technology, are excellent in many factories in proportion to others established with other technologies. PWM is the modifying method to the pulses width in the pulse chain at a direct rate to a small control signal. PWM produces a path to lessening the load current total harmonic distortion [13,14].

A PWM inverter output mostly meets THD demand (together with several filtering which is more readily from the quadrate wave switching planner). The unfiltered PWM output has a comparatively high THD, fabricate filtering is easier (the harmonics so higher frequencies proportion to a square wave).

In PWM, the amplitude of the output voltage can be streaked together with the modifying waveforms. eliminated filter matters to harmonics reduction and the output voltage amplitude control are two distinguished benefits of PWM [10].

Switches circuits complicated control, and frequent switching losses are the disadvantages of PWM. a reference signal is needed to the switches control for the sinusoidal PWM output (a sinusoidal and a carrier signal in this case) that is a triangular wave who observations the switching frequency. These inverters are prepared as stated by:

- Input voltage Vdc = 440 volt
- Capacitors 100 µF
- Switching frequency fsw = 50 KHZ
- O/P voltage 440-volt peak-peak
- Vdc = Vc1 + Vc2
- Vc1 = Vc2 = Vdc/2
- Period time = 1/fsw

The PWM output voltage has a fundamental frequency in the Fourier series that is identical to the reference signal. Multiples of switching frequency have Harmonic frequencies at and concerning of it. The bulk of some harmonics are perfectly considerable, so because of these high frequencies harmonics, a
natural low-pass filter could be functional in ejecting them. The ratio of the carrier frequencies to reference signals is defined as the frequency modulation ratio \( mf \) [11].

\[
mf = \frac{F_{\text{carrier}}}{F_{\text{reference}}} = \frac{F_{\text{tri.}}}{F_{\text{sine}}}
\]

when the carrier frequency growing, (rising \( mf \)) growing the frequencies at whose the harmonics take place. High switching frequencies have a disadvantage of more losses at the switches utilized to perform the inverter.

The attribution of the amplitudes of the reference to carrier signals is defined as amplitude modulation ratio \( ma \):

\[
ma = \frac{V_{\text{m. reference}}}{V_{\text{m. sine}}} = \frac{V_{\text{m. sine}}}{V_{\text{m. Tri.}}}
\]

whether \( ma \) is \( \geq 1 \), then capacity of the output voltage essential frequency \( V1 \) is linearly proportionate to \( ma \). Then \( V1 = ma \cdot Vdc \)

The switches have to be eligible of carrying current in every direction (full-bridge circuit) for PWM same as they did before for the square-wave operation [18]. The real switches are not turned on/off right away. So, it’s requisite to allow for switching control times, same as for square wave inverter.

The sinusoidal reference voltage should be possessed from an outgoing reference or created with the inverter control circuit. a sinusoidal voltage should be existent prior to the bridge working to make a sinusoidal output (so it seems the function of the inverter bridge is needless). The intentional objective of the inverter is to providing the load power from the dc power source.

3. Conclusions

PG and PWM both are a switching scheme technique. In a PG, there is only one pulse per the half cycle, In PWM, the switches are turned On/Off many times through the same period. In a PG the converter output is controlled by changing the phase delay, period, and pulse width, In PWM, the output voltage is controlled by changing the width of pulses.

In PWM, the lower order harmonics could be reduced by selecting the number of pulses per the half cycle, as a result, growing the number of pulses should also grow the amount of the higher-order harmonics (mostly meets THD demand), then it’s easy to be filtered. In a PG, the minimal order harmonic is the third (It's tricky to filter out).

Switches circuits complicated control, and frequent switching losses are the disadvantages of PWM.

References

[1] Suresh, L. Padma. "A brief review on multi-level inverter topologies." 2016 international conference on circuit, power and computing technologies (ICCPCT). IEEE, 2016.

[2] Siddique, Marif Daula, et al. "A new multilevel inverter topology with reduce switch count." IEEE Access 7 (2019): 58584-58594.

[3] Shi, Shunji, et al. "A new diode-clamped multilevel inverter with balance voltages of DC capacitors." IEEE Transactions on Energy Conversion 33.4 (2018): 2220-2228.

[4] Prayag, Aparna, and Sanjay Bodkhe. "A comparative analysis of classical three phase multilevel (five level) inverter topologies." 2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES). IEEE, 2016.

[5] Jayabal, Maalmarugan, Baskaran Jeeravathinah, and Thamizharasan Sandirasegarane. "Reduced switch count pulse width modulated multilevel inverter." IET Power Electronics 10.1 (2017): 10-17.

[6] Venkatraman, Thiyagarajan, and Somasundaram Periasamy. "Multilevel inverter topology with modified pulse width modulation and reduced switch count." Acta Polytechnica Hungarica 15.2 (2018): 141-167.

[7] Meraj, Sheikh Tanim, Law Kab Haw, and Anmar Masaoud. "Simplified sinusoidal pulse width modulation of cross-switched multilevel inverter." 2019 IEEE 15th International Colloquium on Signal Processing & Its Applications (CSPA). IEEE, 2019.

[8] Sabarad, Jayaprakash, and G. H. Kulkarni. "Comparative analysis of SVPWM and SPWM techniques for multilevel inverter." 2015 International Conference on Power and Advanced Control Engineering (ICPACE). IEEE, 2015.

[9] Shrivastava, R. G., M. B. Daigavane, and P. M. Daigavane. "Simulation analysis of three level diode clamped multilevel inverter fed PMSM drive using carrier based space vector pulse width modulation (CB-SVPWM)." Procedia Computer Science 79 (2016): 616-623.

[10] Peddapalli, Satish Kumar. Pulse Width Modulation. De Gruyter Oldenbourg, 2016.

[11] Singh, Shubham, et al. "Matlab Simulation Study and Comparison of Different Multiple Carrier PWM Schemes for Multi-Level CHB Inverter." 2020 IEEE First International Conference on Smart Technologies for Power, Energy and Control (STPEC). IEEE, 2020.
[12] Kavali, Janardhan, and Arvind Mittal. "Analysis of various control schemes for minimal total harmonic distortion in cascaded H-bridge multilevel inverter." Journal of Electrical Systems and Information Technology 3.3 (2016): 428-441.

[13] Maheshwari, Ramkrishan, Sergio Busquets-Monge, and Joan Nicolas-Apruzzese. "A novel approach to generate effective carrier-based pulse-width modulation strategies for diode-clamped multilevel DC-AC converters." IEEE Transactions on Industrial Electronics 63.11 (2016): 7243-7252.

[14] Prabaharan, Natarajan, and Kaliannan Palanisamy. "Comparative analysis of symmetric and asymmetric reduced switch MLI topologies using unipolar pulse width modulation strategies." IET Power Electronics 9.15 (2016): 2808-2823.

Cite this article as: Othman M. Hussein Anssari, Adiy Aljaberi, Maghrib Abidalreda Maky Alrammahi, Zahraa Raheem Mahdi Alzuabidi, Implementation of a pulse generator and pulse width modulation to a three-level diode-clamp inverter as a case study, International journal of research in engineering and innovation (IJREI), vol 5, issue 6 (2021), 349-355.

https://doi.org/10.36037/IJREI.2021.5603.