TOWARDS LATENCY-AWARE DNN OPTIMIZATION WITH GPU RUNTIME ANALYSIS AND TAIL EFFECT ELIMINATION

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ABSTRACT
Despite superb performance of State-Of-The-Art (SOTA) DNNs, the increasing computational cost makes them very challenging to meet real-time latency and accuracy requirements. Although DNN runtime latency is dictated by model property (e.g., architecture, operations), hardware property (e.g., utilization, throughput), and more importantly, the effective mapping between these two, many existing approaches focus only on optimizing model property such as FLOPS reduction and overlook the mismatch between DNN model and hardware properties. In this work, we show that the mismatch between the varied DNN computation workloads and GPU capacity can cause the idle GPU tail effect, leading to GPU under-utilization and low throughput. As a result, the FLOPs reduction cannot bring effective latency reduction, which causes the sub-optimal accuracy versus latency trade-offs. Motivated by this, we propose a GPU runtime-aware DNN optimization methodology to eliminate such GPU tail effect adaptively on GPU platforms. Our methodology can be applied on top of existing SOTA DNN pruning and NAS methods to achieve better latency and accuracy trade-offs. Experiments show 11%-27% latency reduction and 2.5%-4.0% accuracy improvement over several SOTA DNN pruning and NAS methods, respectively.

1 INTRODUCTION
Deep Neural Networks (DNNs) have achieved great performance on various cognitive applications, such as image classification (Deng et al., 2009), object detection (Lin et al., 2014), speech recognition (Graves et al., 2013), etc. However, such a success is built on a considerable cost of computing resources with increasingly larger model parameter volume and structure complexity.

To relieve the computation cost and improve system performance, many DNN optimization techniques have been studied. Started with an algorithm perspective, deep model compression once became a mainstream approach, such as the weight sparsity (Han et al., 2015). Although theoretically outstanding, these methods’ effectiveness was latterly proved to be hardly translated into actual computation load reduction (Wang et al., 2019). Further works also demonstrated that practical optimization has to consider the hardware perspective, and match the model structure reconfiguration with the hardware mechanisms (e.g. structured pruning (Li et al., 2016; He et al., 2017)). Therefore, the design gap emerged between the theoretical algorithm design and hardware deployment, which considerably complicated the current DNN development.

To fill this gap, many hardware-aware DNN designs have been proposed recently (Yang et al., 2018; Cai et al., 2018). One of the current masters is network architecture search (NAS). Leveraging various DNN configuration perspectives and methods, NAS profiles different DNN structures’ performance on dedicated systems, in terms of floating point operations (FLOPs), overall latency, power consumption, etc. (Wu et al., 2019; Tan et al., 2019). Such profiling is further utilized to search and identify the optimal DNN structure to accommodate specific system expectations.

However, hardware-aware algorithm designs as comprehensive as NAS, also have certain underlying ineffective performance interpretations, just like non-structured weight sparsity back then. On one hand, the understanding of the DNN structure’s impact on the system performance is still based on “end-to-end” profiling, lacking the understanding of the intrinsic operations (Cai et al., 2018; Tan et al., 2019). In other words, the optimized DNN model configuration may not fully match the hardware mechanisms. On the other hand, FLOPs reduction is always utilized as a general performance indicator by previous optimization works (Lin et al., 2020; Tan & Le, 2019). However, the actual system gain translation between FLOPs and other performance perspectives is barely analyzed before, especially when applying...
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such a static indicator into dynamic operations in terms of runtime latency.

Our analysis verifies these issues from a runtime latency perspective, and shows that the FLOPs reduced by popular DNN optimization methods could not consistently translate to the runtime latency reduction in the practical system processing. Fig. 1 shows the optimization results of a DNN model – ResNet50 with a structural filter pruning method (Li et al., 2016). Specifically, one convolutional layer’s FLOPs and latency reduction are plotted in Fig. 1(a). It is obvious that, although the FLOPs perform a linear reducing trend with constantly pruned filters, the latency reduction demonstrates a non-linear “staircase” shape. Such a latency staircase indicates the inconsistency of the performance translation from FLOPs to latency reduction. Moreover, when we look into the GPU processors’ utilization rate and throughput, as shown in Fig. 1(b)(c), they demonstrate a fluctuated decreasing trend but with certain cyclical patterns, which implies the potential GPU operation characteristics the adopted optimization cannot reach.

Motivated by such an observation, in this work, we focus on the practical GPU latency optimization with DNN processing. Although GPU runtime optimization has been well studied in conventional tasks, the aforementioned DNN related issues are still highly overlooked. Therefore, we explore the practical GPU runtime mechanism behind DNN processing, and propose a set of practical latency optimization solutions. Specifically, we make the following contributions:

- We propose a set of GPU runtime-aware DNN model structure configuration methodology, which eliminates the GPU tail effect with thread-adaptive DNN deployment. The proposed methodology can also be utilized to enhance cutting-edge DNN optimization algorithms to escalate their system latency performance. (§4)
- Extensive experiments across common benchmarks are conducted. Specifically, the effectiveness of the proposed methodology is demonstrated with distinguishable system speed up and accuracy enhancement, e.g., 11%-27% latency and 2.5%-4.0% accuracy improvement over SOTA DNN pruning and NAS methods. Moreover, the feasibility and generalizability of the methodology are also well discussed with various algorithms and hardware configurations. (§5)

2 BACKGROUND AND RELATED WORK

2.1 GPU Architecture Overview

As our work mainly focuses on DNN optimization on GPUs, we first describe the GPU architecture from both hardware architecture and computation deployment perspectives.

GPU Architecture Hierarchy Without loss of generalizability, we take NVIDIA architecture (Wittenbrink et al., 2011) as an illustrative example. As shown in Fig. 2(a), the GPU is made up of an array of Streaming Multiprocessors (SMs), each of which is formed by multiple CUDA Cores. For example, NVIDIA Titan-V GPU (NVIDIA, 2020b) is made up of 5120 CUDA cores, which are grouped into 80 SMs. Similar mechanisms also apply to other GPU architectures like AMD Polaris (AMD, 2020).

Computation Deployment into Threads When deploying a multi-threaded program into a GPU, the program will be partitioned into Blocks of threads for processing. Each thread block contains certain groups of Warps, and each warp composes of 32 Threads, as shown in Fig. 2(b).

Therefore, thread blocks are the basic units deployed to SMs (one-to-one, or multi-to-one depending on the SM capacity). When the number of thread blocks exceeds the maximum GPU capacity, it would take multiple GPU processing cycles to complete the deployed workload. In such cases, multiple Waves of thread blocks will be processed sequentially until the workload is completed.

2.2 Runtime Latency on GPUs

Runtime latency reflects the GPU execution efficiency given particular workload and throughput (Sze et al., 2020):

\[
\text{Latency} = \frac{\text{Workload}}{\text{Throughput}}. \quad (1)
\]

When processing DNNs, the workload is quantified by the
number of floating point operations, i.e., FLOPs. \textit{Throughput} measures the number of floating point operations per second (FLOPs/s). Taking a step further, when loading a DNN model into multiple SMs, the GPU throughput will be affected by \textit{i}) peak throughput per SM, \textit{ii}) number of SMs, and \textit{iii}) the utilization of SMs:

\[
\text{GPU Throughput} = \text{Peak throughput per SM} \times \text{Number of SMs} \times \text{Utilization of SMs},
\]

(2)

The peak throughput and the number of SMs are determined by the GPU hardware and thus can be regarded as constant values. While the GPU utilization changes over time throughout the model execution (NVIDIA, 2020a).

In a nutshell, both model-level workload and hardware-level GPU throughput (also SM utilization) affect the runtime latency of DNN models. However, most of the existing works focus only on the model-level workload optimization and omit the hardware characteristics, as we will show next.

2.3 Reviewing Existing DNN Latency Optimizations

Before diving into the technical part, we discuss existing research efforts directly related to our work. Based on aforementioned analysis, we can divide the current DNN latency optimization works into two major types.

One type of works simplified their latency optimization objective as FLOPs reduction. For example, convolutional filter pruning first proposed to remove the non-significant filters to reduce the model parameter volume as well as FLOPs and therefore speed up the system (Li et al., 2016). Following that, many works designed different filter significance criteria, such as channel pruning (He et al., 2017), geometric mean pruning (He et al., 2019), and feature map rank based pruning (Lin et al., 2020). However, due to the lack of understanding of intrinsic hardware runtime mechanisms, such FLOPs reduction can only translate to sub-optimal latency mechanisms as mentioned in (Yang et al., 2018).

The other type of work aimed at the “end-to-end” hardware-aware optimization, which treated the DNN execution on GPUs as a black box and leveraged the overall system real-time performance to guide DNN architecture search. For example, NetAdapt (Yang et al., 2018) and Partial order pruning (Li et al., 2019) conducted latency measurement and built look-up tables to estimate the DNN model’s general execution latency, which was used to guide DNN optimization with the sampling-based configuration search process. To improve the search efficiency, some works like ProxylessNAS (Cai et al., 2018) and SinglePath (Stamoulis et al., 2019) designed differentiable latency modeling and integrate it into the optimization objectives. Despite different search policies, most methods utilized similar end-to-end profiling-oriented DNN structure configuration, but is limited to those methods’ lack of understanding of intrinsic hardware mechanisms, especially during runtime operation.

Beyond conducting end-to-end latency optimization, we dive into the GPU thread-level to analyze the DNN runtime performance and reveal one of the root causes for the sub-optimal latency reduction on existing works (Lin et al., 2020; Tan & Le, 2019). Based on the deep understanding of both algorithm deployment and hardware operation, we further propose a holistic optimization methodology that leads to practical latency reduction.

3 Latency Staircase: GPU Tail Effect on DNNs

In this section, we further examine the aforementioned latency staircase phenomena (§3.1), and reveal the critical DNN execution mechanism on GPUs, which causes the mismatch between FLOPs and latency reduction (§3.2). With complementary latency modeling and verification, we also shed light on potential optimization approaches (§3.3).
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3.1 A Glimpse of Latency Staircase Issue

In addition to the experiment results shown in Fig. 1, we profile the runtime latency of two representative DNN architectures on an NVIDIA Titan-V GPU: (1) VGG16 on CIFAR10 (32x32x3) and (2) ResNet50 on ImageNet (224x224x3). For each DNN architecture, we measure each convolutional layer’s runtime latency and repeat the measurement with different layer width settings (obtained by filter pruning). Both models are implemented using PyTorch-1.6 with CUDA-10.0 and CuDNN-7.6.5 backend.

The latency profiling results are shown in Fig. 3. We find that the latency curves differ from each other significantly w.r.t different convolutional layers. Nevertheless, all of them show a similar staircase-like growing trend as we gradually increase the layer width. Taking the latency curve of the layer of conv-4 on VGG16 as an example, we can see it grows rapidly as we increase the layer width from 10% to 20%. Through the latency staircase, we term this period as a growing interval. It then enters a steady interval, where the latency stays still when the layer width grows from 20% to 50%. The latency curve repeats this stair-case growing pattern as we further increase the layer width to 100%.

Through these experimental results, we have three major findings: i) The latency staircase phenomena widely exist in different DNN architectures’ realtime performance; ii) The latency performance is highly related to the DNN layer configurations; iii) Blindly DNN structure optimization (e.g., reducing layer width) may not always benefit the latency. Therefore, a thorough understanding of the practical DNN deployment on GPUs and the latency staircase phenomena’s root cause would effectively guide a comprehensive optimization for the system latency reduction.

3.2 Understanding DNN Execution on GPU Runtime

To understand the root cause of this latency staircase issue, we conduct a “full-stack” examination of DNN execution on GPUs. Specifically, the examination covers two major execution stages: i) DNN deployment to programming threads, and ii) programming threads to GPU mapping. As the latency bottleneck of a DNN lies in convolutional layers (Zhang et al., 2015), we mainly focus on the convolutional layer computation in this work.

DNN Deployment with Programming Thread Mapping.

As illustrated in Algorithm 1, the convolutional layer operation involves N filters convolving with the input feature map I, which can be implemented by a multi-level loop calculation. The computations shown in the three inner loops (line 8—11) are the atom unit running in the same cycle.

Algorithm 1 The Convolutional Layer Operation.

1: Input: Input $I[H, W, D]$, N Filters $F_i[h, w, D]$.
2: Output: Output $O[H, W, N]$.
3: for Filters $i = 1$ to $N$ ($←$ blocks) do
4:     for Input Height $j = 1$ to $H$ ($←$ thread.idx) do
5:         for Input Width $k = 1$ to $W$ ($←$ thread.idy) do
6:             $O[j, k, i] = 0$.
7:             for Kernel height $x = 1$ to $h$ do
8:                 for Kernel width $y = 1$ to $w$ do
9:                     $O[j, k, i] += I[x, y, z] \times F_i[x, y, z]$.
10:                    — Per Thread Kernel Func. Ends.—
11:                    — Per Thread Kernel Func. Starts.—
12:                    — Per Thread Kernel Func. Ends.—
thread. While the computation in the three outer loops (line 3—5) corresponds to different filters or pixels on the feature map. Hence they are parallelized using multiple threads. As a rule of thumb, the number of filters \( N \) usually determines the number of thread blocks in need, and the height \( H \) and width \( W \) of the input determine the number of threads in each thread block. Fig. 4(a) illustrates how the convolutional workload is divided and mapped to threads.

**Programing Thread to GPU Mapping.** Threads are then mapped to GPUs in the granularity of the thread block. As shown in Fig. 4(b), threads are first grouped into blocks, and then loaded to SMs on the GPU. The mapping can be “One-to-One” or “N-to-One.” The maximum number of blocks loaded on one SM is determined by its physical capacity (e.g., number of registers, size of share memory). The DNN model size grows rapidly, which renders the number of thread blocks in need exceed the GPU capacity. Therefore, the GPU will divide these thread blocks into multiple consecutive waves, and run these waves in sequence.

**GPU Tail Effect on DNN.** In general GPU computing scenarios, the “GPU tail effect” happens when the thread blocks on the last wave did not fully occupy all SMs on the GPU. However, the last wave’s processing-cycle still costs the same time with the full-wave ahead, as the processing cycle depends on the wave that takes the longest running time.

Through the “full-stack” DNN execution mechanism examination, we redefine the GPU tail effect with the DNN model structure configuration as the unstructured DNN execution deployment to GPU operation threads and processors. It is worthy to note that, the GPU tail effect with DNN is increasingly prominent with light-weight DNN design especially in the embedded domain, while embedded GPUs are becoming increasingly powerful with larger computing unit capacity. Therefore, without dedicated optimization, the mismatch between the algorithm deployment and hardware utilization can be increasingly severe.

### 3.3 Latency Staircase Modeling & Verification

By revealing the GPU tail effect with DNN, we can build up a dedicated DNN latency staircase model. With the verification of the effectiveness, such a model can effectively guide latency-aware DNN optimization.

**DNN Latency Staircase Modeling on GPUs** Based on the above analysis, the GPU runtime latency \( L \) of one convolutional layer could then be modeled as follows:

\[
L = \Delta L \times \lceil B \div S \rceil,
\]

where \( B = \frac{\text{Number of threads per filter} \times F}{\text{Number of threads per block}} \).

In Eq. 3, \( \Delta L \) is the duration of one processing cycle for each SM to finish one thread block, \( B \) is the number of thread blocks for this layer, and \( S \) is the number of SMs per GPU. The \( \lceil \cdot \rceil \) is the rounding-up function which returns the least integer greater than or equal to the input, e.g., \( \lceil 2.1 \rceil = 3 \), denoting the latency ceiling effect caused by the last GPU tail. For one convolution layer, the overall number of blocks \( B \) is determined by two factors: (i) the overall workload, which depends on the number of threads per filter \( \times \) the number of filters \( F \), and (ii) per block workload, i.e., number of threads per block. Therefore, both filter amount and input shape can influence the per-filter workload, translating to a different number of blocks for this layer during deployment.

**Effectiveness Verification** To verify the DNN execution latency model established above, we test the model with a set of convolutional layers with different filter numbers from 64 to 512. We keep the same kernel size \((3 \times 3)\) and the input feature map \((64 \times 64 \times 512)\). The batch size, by default, is set to 1. All benchmarks are conducted on a Titan-V GPU\(^2\). To better understand the results, we also show the number of blocks \( B \) and the number of waves \( W \) corresponding to each layer settings. The result is shown in Fig. 5. We have the following three key observations.

**Verification 1:** The number of blocks \( B \) grows with the number of filters \( F \). For example, \( \Delta F = 80 \) leads to \( \Delta B = 80 \). Therefore, the current layer deployment has mapped its convolution filters one-by-one to the thread blocks, which is similar to Fig. 4(a).

**Verification 2:** With the number of blocks \( B \) growing, the latency increases with a granularity of 80 blocks \( \Delta B = 80 \), which is the full GPU capacity (80 SMs). This verifies that the latency increases with the step size of \( S \) in Eq. 3.

**Verification 3:** For a wave in one flat interval, the latency remains the same regardless of how many blocks are in the wave or how many SMs are actually utilized. This verifies the latency ceiling effect, i.e., the GPU processing cycle per wave depends on the longest time that SM takes.

The above latency performance analysis, mechanism modeling, and effectiveness verification reveals the actual correlation between DNN model structure and GPU runtime operation. By filling the algorithm and hardware gap, in the next section, we propose a GPU-aware model optimization methodology to eliminate the GPU tail effect and achieve better latency optimization performance.

### 4 Eliminating the GPU Tail: Hardware-aware Optimization

In this section, the proposed methodology is firstly presented with the design challenges (§4.1), followed by the specific design rules (§4.2). Finally, the latency-aware DNN optimization methodology is presented (§4.3).

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\(^2\)We will show in later experiments that such phenomenon is general for both high-end and low-end GPUs like Jetson Nano.
4.1 Design Challenges

When designing the model optimization technique for runtime latency reduction, we should jointly address two critical challenges: (i) The design should address the GPU tail effect as it often leads to GPU under-utilization. A comprehensive FLOPs reduction method may not achieve lower runtime latency. For instance, FLOPs reduction effort applied on the steady interval will not improve the runtime latency (§3.1). (ii) The design should also consider the hardware diversity of GPU configurations. Different GPUs may differ drastically in their capacity (e.g., number of SMs). Hence no one-fit-all DNN model configuration exists even for the same model running on different GPU platforms.

4.2 Combining SM Utilization and GPU Throughput

Combined Design The GPU tail effect leads to an inefficient utilization of SMs on GPU. Hence an intuitive idea is to employ the SM utilization rate to guide the DNN model optimization, so that we can eliminate the tail effect and achieve the optimal latency reduction. In practice, however, the profilesd SM utilization can often be imprecise\(^3\), hence cannot serve as a reliable cue to guide the DNN model structure optimization.

Therefore, we leverage both SM utilization and GPU throughput to guide the model optimization. The effectiveness of using both SM utilization and GPU throughput can be better illustrated by Fig. 6: Taking the middle latency staircase as an example, the left and right edge points denote two layer configurations within the same wave, but with the most under-utilized GPU tail (left) and no GPU tail (right). As a result, the left point shows the lowest GPU utilization (73\%) and throughput (8.5 TFLOP/s). While the right point shows the highest SM utilization (93\%), and near upper-bound GPU throughput (11.8 TFLOP/s). Thus, by jointly considering the configurations with the maximum utilization and throughput, we can effectively identify the optimal layer configuration without any tail effect.

Design Formulation The optimal configuration for layer \(i\) can be obtained by maximizing the utilization \& throughput:

\[
C_i[m] = \arg \max_m(U_i \times T_i),
\]

where \(U_i\) and \(T_i\) denote the utilization and throughput information for this layer, and \(m\) is the number of optimal candidates. For example, in Fig. 6, by considering the maximum \(U\) and \(T\), we can identify five layers’ width configurations that yield the optimal GPU runtime efficiency.

Based on such GPU efficiency guidelines capable of identifying the optimal layer configuration candidates, we then propose our GPU-aware model optimization algorithm.

4.3 GPU-Aware Model Configuration Optimization

Accuracy-Latency Optimization Objectives We first define the model-level accuracy-latency trade-off objectives.

Naturally, the accuracy latency trade-off can be defined as trading off the latency gain (LG) and the accuracy loss. Also, we use the parameter gain (PG) to describe the model capacity expansion and therefore as an accuracy gain ap-
Algorithm 2 GPU-Aware Model Optimization Algorithm.
1: **Input:** Model’s initial layer width configs \( r[l] \), latency \( L[l][n] \), utilization \( U[l][n] \), and throughput \( T[l][n] \).
2: **Output:** Optimized model configs \( R_{\text{new}}[l] \).
3: Identify candidate \( C_i[m] \) for each layer \( l \) by Eq. 4.
4: Initialize latency & parameter gain list \( LG[l], PG[l] \).
5: for layers \( i = 1 \) to \( l \) do
   6: Get \( LG_i, PG_i \) estimation by Eq. 5a and 5b.
   7: Sort the layer index list by \( LG[l] \) or \( PG[l] \).
   8: while layer index list is not empty do
      9: Pop out layer \( j \) with Argmax \( LG[l] \).
   10: Scale down \( R_{j,\text{new}} \) by Eq. 8a for max latency gain.
   11: while \( \sum_i PG(R_{\text{new}}) \notin (-\tau, \tau) \) do
      12: Pop out layer \( k \) with Argmin \( LG[l] \).
      13: Scale up \( R_{k,\text{new}} \) by Eq. 8b to balance param gain.
14: Get runtime latency evaluation \( L_{\text{new}} \) of config \( R_{\text{new}} \).
15: if \( L_{\text{new}} \leq L_{\text{old}} \times \delta \) then
   16: Train and evaluate the model accuracy.
17: else
   18: Set \( \tau = 2 \) and repeat the algo. from line 9.
19: **Return** Optimized config \( R_{\text{new}} \).

proximation. The latency gain and parameter gain can be estimated based on latency profiling \( L_i \) and layer width \( R_i \):

\[
LG_i = L_i[R_{i,\text{old}}] - L_i[R_{i,\text{new}}], \quad (5a)
\]

\[
PG_i = R_{i,\text{old}} - R_{i,\text{new}}, \quad (5b)
\]

where \( R_{i,\text{new}} \) and \( R_{i,\text{new}} \) denote the optimized and the original layer configuration, \( LG_i \) indicates the latency gain, and \( PG_i \) indicates the parameter gain which can be negative if we scale down the layer width.

Accuracy-Oriented Optimization: The accuracy-oriented optimization aims to boost the accuracy without incurring any latency overhead. As a larger parameter gain demonstrates better accuracy, the goal can be represented by:

\[
\text{Maximize } \sum_i PG_i, \quad \text{s.t. } \sum_i LG_i \geq 0. \quad (6)
\]

Latency-Oriented Optimization: For latency-oriented optimization, we aim to reduce the latency while maintaining no or negligible accuracy drop. The objective can be formulated as maximizing the latency gain while maintaining parameter gain in a tolerable range \( (\tau) \):

\[
\text{Maximize } \sum_i LG_i, \quad \text{s.t. } \sum_i PG_i \in (-\tau, \tau). \quad (7)
\]

Latency-Aware DNN Model Optimization Based on the previous objective, we then propose our GPU-aware model optimization method. We take the latency optimization algorithm to illustrate as following. The overview is shown in Algorithm 2, which includes four major steps.

Step 1. DNN Structure Modification Pre-Analysis: Given the DNN model structure, we first profile the full-spectrum guideline metrics (i.e., latency, utilization) for each layer. The throughput information can then be derived by theoretical FLOPs and profiled latency. The optimal candidate configurations \( C_i[m] \) for layer \( i \) can be identified by Eq. 4. As we show before, the optimal configurations per layer usually consist of only several discrete settings. Thus, we can greatly reduce the search space.

Step 2. Layer-Level DNN Structure Adjustment: For each convolutional layer in the model, the layer width adjustment follows two ways, i.e., either scaling down for latency gain \( (LG) \) or scaling up for parameter gain \( (PG) \):

\[
R_{i,\text{new}} = \max(*C_i[m] < R_{i,\text{old}}), \quad (8a)
\]

\[
R_{i,\text{new}} = \min(*C_i[m] > R_{i,\text{old}}), \quad (8b)
\]

where \( R_{i,\text{new}} \) and \( R_{i,\text{old}} \) indicate adjusted and original layer width for layer \( i \), and \( C_i[m] \) is the optimal candidate list. The first strategy Eq. 8a denotes we scale down the layer width to the left optimal configuration candidates. By doing so, we can remove the last GPU tail, thus reducing the latency. By contrast, the second strategy Eq. 8b indicates that we can scale up the layer width to fully-occupy the last GPU tail, thus potentially enhancing the model accuracy without incurring any latency overhead.

Step 3. Model-Level DNN Structure Adjustment: One naive solution of maximizing the latency optimization is to scale down all layers according to Eq. 8a. However, this can incur larger negative parameter gain and thus hurt the model accuracy. To maintain the parameter gain in the small range \( (\tau, \tau) \), we propose a balanced model adjustment strategy by simultaneously scaling down and scaling up different layers in a balanced manner.

Specifically, we maintain two queues of layer indexes ranked by \( LG_i \) and \( PG_i \). To maximize \( LG \) while meeting the \( PG \) constraints, we greedily pop up layers with top \( LG_i \) to scale down by Eq. 8a, while simultaneously pop up layers with the least \( PG_i \) to scale up by Eq. 8b to balance the negative parameter gain. The model optimization will stop when all layers are popped out and adjusted accordingly.

Step 4. DNN Structure Determination: After generating the new model configuration, we first conduct a runtime latency check to filter out configurations that cannot meet the model latency reduction requirements \( L_{\text{new}} \leq L_{\text{old}} \times \delta \). The \( \delta \) here denotes the targeted latency reduction ratio. If the current model cannot meet the latency requirements, the algorithm can repeat by loosing the constraints, e.g., allowing larger parameter gain tolerance \( \tau \). It allows for more aggressive optimization to meet the latency reduction target.

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4The accuracy-oriented optimization follows the similar procedure, which could be found in supp. material.
Advancing NAS For NAS task, on one hand, our method can provide similar discrete search space for layer configurations, thus enhancing both the search efficiency and the final model’s GPU-utilization performance. On the other hand, we can also conduct post-optimization by further adjusting the existed NAS model architectures to achieve better latency-accuracy trade-off.

5 EXPERIMENTAL EVALUATION

5.1 Experimental Setup

We conduct experiments using the software stack including PyTorch-1.6, CUDA-10.1 and CuDNN-7.6.5. For GPU generality, we evaluate three GPUs from high-end (Titan-V, P6000) to embedded ones (Jetson Nano). The specification comparison of them is shown in Table 1.

We apply our method into two common model optimization methods: Filter pruning and NAS. For the pruning task, two state-of-the-art pruning methods are chosen as baselines, including HRank (Lin et al., 2020) and SoftPruning (He et al., 2018). For the NAS task, we mainly apply our model optimization method onto the EfficientNet series (Tan & Le, 2019), one of the SOTA efficient model architectures.

5.2 Evaluation in the Pruning Task

We compare our method on filter pruning tasks with HRank (Lin et al., 2020) and SOFT (He et al., 2018).

Latency Reduction: As Table 2 presents, by optimizing the pruning configurations, our method achieves consistently lower latency than baseline methods (11.3% to 17.7% latency reduction) with negligible accuracy influence. Our latency improvements can also be explained from the following two aspects.

Throughput Maximization: As Table 2 shows, our method shows consistently higher GPU throughput than the baselines (see (FLOPS) column). Take VGG16 architecture as an example, the optimized model using our method can achieve 3.90 TFLOPs on GPU, showing 1.6× throughput increase compared to the baseline method, 2.41 TFLOPs.

Balanced Parameter Gain (PG): In addition to lower latency, our method can even maintain more parameters and improve the baseline accuracy. As (Params) column shows, our optimized models have maintained the parameter gain either in positive range or small negative range, which ensures our models’ accuracy performance.

5.3 Evaluation in the NAS Task

In this part, we apply our optimization method to further optimize the NAS network’s performance on GPUs. Specifically, we optimize the EfficientNet series of model structures to achieve better accuracy latency trade-offs. The evalua-

Figure 7. VGG pruning configuration optimization on HRank. We slightly scale down Conv1-Conv4 using minimal accuracy drop to trade for major latency reduction, while scale up Conv5-Conv12 to compensate the accuracy drop without obvious latency increment.

Optimization Demonstration with A Case Study To illustrate the algorithm, we demonstrate one of the SOTA method’s (Lin et al., 2020) sub-optimal optimization results on GPUs and then show our optimization mechanisms.

Fig. 7 shows the per-layer configuration from (Lin et al., 2020) (red) and our optimized ones (green). As we can see, for CONV1, 3, 4, the original layer width is obviously non-optimal, which leads to the tail effect with low GPU throughput. To optimize that, we scale down the layer width slightly to meet the left optimal configuration and thus eliminate the GPU tail. By such adjustment, the latency of these layers shows a dramatic reduction. Then as the compensation, we scale up certain later layers, e.g., CONV5, 9, 11, to balance the negative parameter gain without incurring obvious latency overhead. As a result of such configuration optimization, we can reach the similar accuracy (92.9%) as the baseline (93.1%) but deliver 17.7% overall latency reduction, which demonstrates better accuracy-latency trade-offs than the baseline method.

4.4 Applicability in Different Optimization Methods

As an orthogonal hardware-oriented optimization dimension, our configuration optimization method can be applied to enhance existing model optimization methods:

Advancing Filter Pruning Filter pruning methods usually design the filter pruning criteria based on the accuracy influence, forming usually a continuous search space for each layer’s width (i.e., how many filters to prune). Our method can be integrated into such methods by providing per layer optimal candidates list, thus providing a discrete pruning space. The further training strategies can remain the same.
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Table 1. The Evaluated GPUs and Specifications.

| GPU Name   | Architecture | #SMs | #Cores | Peak FLOP/s |
|------------|--------------|------|--------|-------------|
| Titan-V    | Volta        | 80   | 5120   | 14.9T       |
| Quadro P6000 | Pascal       | 30   | 3840   | 12.0T       |
| Jetson Nano| Maxwell       | -    | 128    | 0.24T       |

Table 2. Latency Optimization on SOTA Pruning Works. HRank: High Rank Pruning [CVPR20], SOFT: Soft Pruning [IJCAI18].

| Model       | Method       | Params | #FLOPs | FLOP/s | Acc. % | Time (ms) |
|-------------|--------------|--------|--------|--------|--------|-----------|
| VGG16       | HRank        | 1.90M  | -      | -      | -      | -         |
| CIFAR10     | Ours         | 2.85M  | 104.1M | 3.90T  | 92.9   | 2.05E6    |
| ResNet56    | HRank        | 0.48M  | 65.9M  | 0.83T  | 93.6   | 4.20E6    |
| CIFAR10     | Ours-1       | 0.50M  | 79.1M  | 1.00T  | 93.8   | 3.72E6    |
|             | Ours-2       | 0.50M  | 75.1M  | 0.95T  | 93.5   | 3.51E6    |
| ResNet56    | SOFT-1       | 0.53M  | 68.5M  | 0.88T  | 93.1   | 4.05E5    |
| CIFAR10     | Ours         | 0.43M  | 71.4M  | 0.92T  | 93.2   | 3.52E6    |
|             | SOFT-2       | 0.45M  | 53.1M  | 0.68T  | 92.3   | 3.64E6    |
|              | SOFT-3       | 0.43M  | 66.0M  | 0.79T  | 92.3   | 3.01E6    |

*Note that, SOFT-1 and -2 denotes two configs with different pruning rates from the original paper. The latency is evaluated on Titan-V with batch size = 128.

Table 3. Accuracy Optimization on EfficientNets.

| Method       | Acc. % | GPU | Time (ms) | FLOP/s | Time (ms) | FLOP/s |
|---------------|--------|-----|-----------|--------|-----------|--------|
| EfficientNet  | B0     | 77.52 | 12.6 | 61.9G | 13.8 | 56.5G |
| (ImageNet)    |        |     |        |        |        |        |
| Ours          | +3.97% | 81.49 | 12.7 | 414.2G | 14.1 | 373.0G |
| EfficientNet  | B1     | 79.38 | 17.8 | 78.7G | 19.8 | 70.7G |
| (ImageNet)    |        |     |        |        |        |        |
| Ours          | +2.7%  | 82.08 | 18.0 | 442.7G | 19.9 | 396.0G |
| EfficientNet  | B2     | 80.18 | 18.2 | 109.9G | 19.9 | 100.5G |
| (ImageNet)    |        |     |        |        |        |        |
| Ours          | +2.14% | 82.32 | 18.4 | 547.3G | 20.4 | 488.2G |

5.4 Generalizability across DNN Architectures

In this part, we conduct generalizability evaluation of DNN latency staircase in terms of DNN hyper-parameters, including batch sizes, input resolutions and filter shapes.

Batch Size Variation Fig. 9 shows the latency w.r.t. varied batch size from 1 to 256 for two CONV layers of VGG16 on ImageNet resolution. The latency staircase consistently exists for all layers with different batch sizes. Specifically, layers with larger batch size incurs a longer processing cycle for a wave, leading to a higher latency staircase.

Number of Filters Variation Fig. 9 also shows that CONV-5 has more levels of staircase compared to CONV-3. The reason is that CONV-5 has more filters (128) than CONV (64). Since the number of filters determines the number of thread blocks, more sequential GPU waves are needed with a larger number of filters, leading to more levels of staircase.

Input Resolution Variation Similar latency evaluation is also conducted w.r.t. varied input resolution from 128 to 1024 for CONV-3 and CONV-5 in Fig. 10. The latency staircase...
5.5 Generalizability across GPU Platforms

We evaluate the generalizability of our methods on both high-end GPU, P6000 and Embedded GPU, Jetson Nano. Their specifications in Table 1. Although Jetson Nano has much less capacity with only one unified chip (similar to one SM), and much less CUDA cores (only 128 CUDA cores), our method can be generally applied and help achieve better accuracy-latency trade-offs on both platforms. The results are shown in Table 4 and Table 5.

As the results show, we could achieve 9.0% to 27.2% latency reduction than the baseline methods, while maintaining similar accuracy for VGG16 and ResNet56 on the P6000 GPU. Similar latency benefits (13.3% to 20.5%) could be achieved for the Jetson Nano GPU, demonstrating the generality of our method across different GPU platforms.

The above results demonstrate the effectiveness and generalizability of our GPU efficiency guideline and algorithm design. Without any GPU-specific assumptions, our methods could be applied to a spectrum of GPUs to enhance the current DNNs’ accuracy-latency trade-off.

6 Discussion and Conclusion

Here we discuss the uniqueness and significance of our work and then draw the conclusion.

This work extends the concept of structured DNN optimization and corresponding granularity. Rather than taking structured filter configuration as the optimization units, the basic GPU runtime granularity, e.g., waves, also needs to be considered. Although this work mainly focuses on GPUs, similar tailing effects also potentially exist in other platforms with massive parallelism. Therefore, the proposed optimization methodology in this work also has significant potential to be applied for more other computing platforms.

In summary, our current proposed DNN optimization framework can effectively eliminate the GPU tail effect for DNN execution. With effectiveness, feasibility, and generalizability well proved, our work shows outstanding DNN latency accuracy trade-offs within various computing scenarios.
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