Improved Electrical Characteristics of 1200V/20A 4H-SiC Diode by Substrate Thinning and Laser Annealing

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Abstract. In this paper, two kinds of silicon carbide (SiC) backside metallization processes were developed, which were backside thinning combined with laser annealing to form ohmic contact and direct rapid annealing (RTA) to form ohmic contact. The specific contact resistivity obtained by both annealing processes was 3.4E-5 Ω·cm² to 3.8E-5 Ω·cm². In order to obtain the effect of thinning combined with laser annealing process on forward conduction characteristics of medium voltage devices, 1200V/20A JBS diode was developed, and the backside contact adopted the above two annealing schemes, the thickness of 4H-SiC substrate is 200μm. According to the statistical results of hundreds of JBS diodes, the electrical characteristics of the two types JBS are basically the same. Compared with the JBS diode without substrate thinning, the forward conduction voltage (V_F) of the thinned JBS diode is decreased about 0.048V. When the substrate of 1200V SiC JBS diodes is reduced to 80μm, the value of V_F can only be reduced by about 0.0868V.

Keywords: 4H-SiC, laser annealing, RTA, thinning, diode, V_F.

1. Introduction

Due to the excellent physical, chemical and electrical properties, SiC has a good application prospect in the field of power semiconductors. It can be used to make high voltage, high frequency and high-power density integrated electronic devices. SiC power devices usually use vertical structure to achieve high current handling capacity, the substrate will introduce large on-state resistance to medium and low voltage devices, especially low voltage diodes, and on-state resistance is one of the most key performance parameters in practical applications. In order to further improve the on-state resistance, the substrate of SiC wafer needs to be thinned. Generally, Ni film annealed at 900-1000 °C of Rapid Thermal Annealing (RTA) will be used to form backside ohmic contact. However, RTA annealing will cause a thermal impact on the front side of wafer. The combination of thinning and laser annealing process replaces the traditional backside ohmic contact process, which further simplifies the process flow and improves the reliability of the process [1].

SiC junction barrier Schottky (JBS) diode has become the preferred power diodes because of its low switching loss, high recovery speed and high reverse breakdown voltage [2]. It has been found that the
substrate resistance of 600V-650V 4H-SiC devices accounts for about 60%-70% of the total forward on-state resistance of devices. The forward on-state current can be nearly doubled when the substrate of 600V JBS diode is thinned to 200nm. There are many reports on low voltage diodes performance improvement by thinning and laser annealing [3,4], the improvement of forward conduction characteristics of 1200V 4H-SiC diodes by substrate thinning process has not been reported, it needs to be evaluated.

In this paper, backside thinning combined with laser annealing to form ohmic contact processes were developed, the specific contact resistivity ($\rho_c$) should be lower than 1E-4Ω·cm², which is compared with direct RTA processes by CTLM (Circular transmission line model) method [5]. After that, those two types SiC backside metallization processes were used in 1200V/20A 4H-SiC JBS diode, named as JBS-A and JBS-B, respectively, the thickness of thinning substrate of JBS-A is 200μm. The electrical properties result of hundreds of JBS-A and JBS-B chips are counted, the enhancement effect of the backside thinning combined with laser annealing process on the forward characteristics of the diode is evaluated. Finally, the improvement effect of forward conduction characteristics of 1200V/20A 4H-SiC JBS diode after substrate thinning to 80μm is predicted.

2. Process Development

Two 6inch 4H-SiC substrates with similar doping concentration are selected, named Sub-A and Sub-b respectively, with an initial thickness about 360μm. Ohmic contacts are prepared on the C surface of Sub-A by mechanical thinning, sputtering Ni and laser annealing. After mechanical thinning, the thickness of Sub-A was 200μm, the thickness variation range≤4μm, and the roughness Ra is about 18.6nm. Before thinning, the Sub-A wrap≤40μm, and after thinning, the wrap had increased to about 120μm. The thickness of 200μm is the relative limit thickness to ensure process stability. After standard cleaning process, 120nm Ni is sputtered on sub-A and sub-b, and form CTLM test pattern by photolithography and wet etching process, the CTLM test pattern is shown in Figure 1, it is composed of several groups of concentric rings with gradual ring spacing. R0 to R6 are 200μm, 230μm, 225μm, 220μm, 215μm, 210μm, 205μm, respectively.

![Figure 1. CTLM test pattern, the blue area represents the metal Ni coverage area, the white area represents the silicon nitride exposure area.](image)

Then, laser annealing is applied to Sub-A, the wavelength is 355nm, the spot size is 100μm*100μm, the laser energy density is 2.8J/cm², and the overlay is 67/50%. It can be obtained by simulation calculation that the temperature of the annealed surface is up to 1400℃, and the temperature of Si surface is lower than 200℃. Sub-b is annealed at 1000℃ 180s using RTA. Finally, 4μm Al is evaporated on Sub-A and Sub-B, photolithography and wet etching are used to shape Al film to CTLM measurement pattern. Finally, an Agilent 1505a power device analyzer is used to test the I-V curves of sub-A and sub-b, the I-V curves of sub-A and sub-b are similar, which is shown in Figure 2, all I-V curves show ohmic contact characteristics. And calculate the specific contact resistance. The resistance fitted by the I-V curve is called $R_{\text{tot}}$, and linear fit the $R_{\text{tot}}$ of different concentric rings I-V curves to ln ($R_{\text{tot}}/R_0$) to get the slope and intercept, as in Figure 3. The square resistance ($R_s$) and transfer length ($L_T$)
can be calculated by slope and intercept, the specific contact resistivity ($\rho_c$) can be calculated by Equation (1)

$$\rho_s = R_s \times L_t^2$$  \hspace{1cm} (1)

$\rho_c$ of Sub-A was $3.4E-5 \Omega \cdot \text{cm}^2$, $\rho_c$ of Sub-A was $3.8E-5 \Omega \cdot \text{cm}^2$. Take 5 points to monitor the $\rho_c$ uniformity, the uniformity of Sub-A was 8.73%, and the uniformity of Sub-A was 11.25%, the uniformity might cause by contact instability during I-V test.

![Figure 2. The I-V curve of CTLM test structure.](image1.png)

![Figure 3. Linear fitting of contact resistance corresponding to different ring spacing.](image2.png)

### 3. Device Fabrication

Two commercial 6inch 4H-SiC epitaxial wafers are selected, the thickness of the epitaxial layer is about 12.5μm, which is N doped, the doping density range is within $8.50 \times 10^{15} \text{cm}^{-3}$-$9.30 \times 10^{15} \text{cm}^{-3}$. The substrate resistivity is 0.019 $\Omega \cdot \text{cm}$, and its thickness is about 360μm. Two type 1200V/20A JBS diodes with the same structure are manufactured, and we name them as JBS-A and JBS-B, respectively, the JBS-A uses the mechanical thinning and laser annealing process, and the JBS-B uses RTA process. A single diode
size is $3500\mu m \times 3500\mu m$, and the active region size is $3300\mu m \times 3300\mu m$, and the effective conduction area of a chip accounts for about 88.9%. The injection depth of the P+ region is about 0.5μm, and the width of the P+ region is about 1.58μm. The terminal adopts a field limiting ring structure with gradual ring spacing [6]. The detailed JBS diode structure is shown in Figure 4.

![Figure 4. 1200V/20A 4H-SiC JBS diode structural drawing.](image)

Then, JBS-A and JBS-B are fabricated, and an Agilent 1505a power device analyzer is used to test the forward and reverse characteristics, the pulse width of forward test is 1ms. The reverse voltage of devices is independent of the SiC substrate, and both JBS-A and JBS-B devices meet $V_R \geq 1400V@IR=10\mu A$. In order to obtain the effect of backside metallization process on the forward characteristics of those devices, $V_F@IF=20A$ and $T_j=25^\circ C$ of hundreds of JBS-A and JBS-B are statistically analyzed as shown in Figure 5 and Figure 6, respectively. The mean values of $V_F$ ($V_F$) are obtained by Gaussian function fitting. All of the results are shown in Table 1.

![Figure 5. The $V_F$ Statistical results of JBS-A devices.](image)
Figure 6. The $V_F$ Statistical results of JBS-B devices.

Table 1. Electrical characteristic table.

| Test Item | Description                  | Test Conditions | Value       |
|-----------|------------------------------|-----------------|-------------|
| $V_R$     | DC Peak Reverse Voltage      | $I_R=10\mu A$   | $\geq1400 V$|
| $V_F$     | Mean Value of Forward Voltage| $I_F=20 A$, $T_j=25^\circ C$ | $V_{F(JBS-A)}=1.318 V$ |
|           |                              |                 | $V_{F(JBS-A)}=1.366 V$ |

The improved forward electrical characteristics of 1200V/20A 4H-SiC JBS diode by substrate thinning and laser annealing can be seen from the difference between the statistical average value $V_{F(JBS-A)}$ and $V_{F(JBS-A)}$. $V_{F(JBS-A)}$ is decreased about 0.048V. Since the substrate thickness of SiC wafer used to prepare 1200V diode is much greater than the epitaxial thickness, it can be defaulted that the current direction in the substrate is perpendicular to the substrate. The resistivity of substrate is 0.019$\Omega \cdot \text{cm}$, and the reduced substrate thickness of JBS-A is 160$\mu m$. Given the single chip area, @$I_F=20 A$, it can be calculated that the value of $V_F$ drop caused by the thinned substrate is about 0.0496V, which is close to the change of $V_F$. Therefore, it can be believed that the improvement of forward electrical characteristics comes from the substrate thinning process. For 1200V SiC JBS diodes, even if it is reduced to 80$\mu m$, the value of $V_F$ can only be reduced by about 0.0868V. If we want to improve the forward conduction characteristics of 1200V SiC JBS diode, we still need to design the epitaxial layer and device structure.

4. Conclusions

Two kind of backside metallization processes about back thinning combined with laser annealing and direct RTA are developed, $\rho_c$ can be 3.4E-5$\Omega \cdot \text{cm}^2$ and 3.8E-5$\Omega \cdot \text{cm}^2$, respectively. After that, Both SiC backside metallization processes are used in 1200V/20A 4H-SiC JBS diode. After electrical characteristics test, we find that $V_R$ of JBS devices is independent of the backside metallization processes when $\rho_c$ is similar. By comparing statistical results and calculation results of $V_F$, we find that the improvement of forward electrical characteristics of 1200V SiC JBS diodes comes from the substrate thinning process. Through calculation, we find that the forward characteristic cannot be significantly improved by the thinning process for 1200V SiC JBS diodes, and more work should be down on the design of epitaxial layer and device structure.
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