A 14 \( \mu \)J/Decision Keyword-Spotting Accelerator With In-SRAM Computing and On-Chip Learning for Customization

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Abstract—Keyword spotting (KWS) has gained popularity as a natural way to interact with consumer devices in recent years. However, because of its always on nature and the variety of speech, it necessitates a low-power design as well as user customization. This article describes a low-power, energy-efficient KWS accelerator with static random access memory (SRAM)-based in-memory computing (IMC) and on-chip learning for user customization. However, IMC is constrained by macro size, limited precision, and nonideal effects. To address the issues mentioned above, this article proposes bias compensation and fine-tuning using an IMC-aware model design. Furthermore, because learning with low-precision edge devices results in zero error and gradient values due to quantization, this article proposes error scaling and small gradient accumulation to achieve the same accuracy as ideal model training. The simulation results show that with user customization, we can recover the accuracy loss from 51.08% to 89.76% with compensation and fine-tuning and further improve to 96.71% with customization. The chip implementation can successfully run the model with only 14 \( \mu \)J per decision. When compared to the state-of-the-art works, the presented design has higher energy efficiency with additional on-chip model customization capabilities for higher accuracy.

Index Terms—Model personalization, on-chip training, quantized training.

I. INTRODUCTION

MOTIVATED by the breakthrough of deep learning in speech recognition, voice recognition using keyword spotting (KWS) is a natural and increasingly popular way to interact with consumer devices. Since KWS is always on, it should have very low power for edge devices.

Various works have been proposed for low-power KWS. Zhang et al. [1] implements several KWS models on microcontrollers to compare their accuracy and memory/compute requirements. Zheng et al. [2] proposed a binary neural network-based design with on-chip self-learning to update the entire model. Dbouk et al. [3] uses recurrent attention network and hybrid digital and multibit in-memory computing (IMC) for ultralow power KWS. Guo et al. [4] proposes hybrid digital circuits and 16 \( 64 \times 64 \) static random access memory (SRAM)-based IMC macros with 3-bit analog-to-digital converter (ADC) for recurrent neural network-based KWS. Liu et al. [5] uses precision self-adaptive computing for a binary weight network to reduce power, and [6] uses mixed mode computing for low-power KWS. In summary, they reduce power consumption through recurrent models, quantized/binary neural network models, or voice activity detection (VAD). However, their model design did not consider the underlying hardware constraints or nonideal effects for IMC.

In addition to the low-power requirement, KWS models often face accuracy degradation due to the accent and pronunciation of different users in different regions. To recover accuracy, model personalization or customization is a popular technique for applications with data that vary significantly from person to person, such as KWS [7], human activity recognition [8], and handwriting recognition [9], which are demanded for edge AI devices. Model customization can be executed on either the chip or server side. For KWS, on-chip model customization is preferred over the server-side one due to the privacy concern to retrain the entire model or fine-tune a pre-trained model with a small amount of local data. However, edge devices usually use low-precision fixed-point hardware that poses a big problem for high-precision training. This situation is getting worse for fine-tuning a pre-trained model since the errors and gradients are quite small in such a case, and their quantization will lead to zero error and gradient. Thus, fine-tuning will lead to catastrophic failure.

To solve above issues, this article proposes a low-power KWS chip with SRAM-based IMC and on-chip learning for customization. The model customization issue on low-precision hardware is solved by the proposed error scaling, small gradient accumulation, and random gradients, which can restore the accuracy as the full precision fine-tuning. IMC is adopted for its highly parallel computation and ultralow power consumption. However, IMC also faces limited precision in the weight and activation and nonlinearity effects of analog circuits. Thus, this article proposes an IMC-aware model that uses a binary neural network with in-memory-batch normalization (BN) to minimize the conversion between digital and analog. Only the first and final layers use digital implementation due to its higher precision needs. The
nonideal effects are solved by bias compensation and fine-tuning. The chip implemented shows higher energy efficiency compared to other state-of-the-art works with customization capability.

The remainder of the article is organized as follows. Section II shows the baseline model for KWS. Section III presents the proposed on-chip training for model customization. Section IV shows the nonideal effects of the IMC macro and how to solve them. Section V presents the proposed KWS chip architecture. Section VI shows the experimental results and comparisons. Finally, this article is concluded in Section VII.

II. BASELINE MODEL FOR IMC AWARE KWS

Fig. 1 shows the overall IMC aware binary neural network model for KWS. The binary neural network is selected because the multibit ADC required for IMC could be simplified as a low area cost and low power sense amplifier (SA) when combined with in-memory BN [10]. The input is 8-bit raw audio data of nearly 1-s length. The model outputs the class of the input keyword. The model consists of one binarized sinc convolution layer [11], which is a learned filter bank to process raw audio. Compared to conventional Mel-Frequency Cepstral Coefficients (MFCC), the computational complexity will be smaller, and this also makes the model an end-to-end learning model. Following the filter banks, five binary convolution layers are adopted that use group convolution with group size set to 24 and in-memory BN as the basic block. With in-memory BN, convolution and BN can be executed together within the array, and the array output can be a binary activation output that can be implemented by SAs instead of multibit ADCs. The weights of the sinc convolution layers are also binary for hardware consideration. Thus, the model uses only binary computation in the convolution layer in inference, while the final classifier layer uses 8-bit fixed-point computation.

In addition to the above model, for better model training results, we adopt the trainable offset for binarized activation [12], as shown in Fig. 2. This offset value can be merged with BN in the inference phase, which will not incur additional overhead for hardware implementation. Fig. 3 shows the trained offset value for each layer. Initial values are set to 0 for all layers. The figure shows that the appropriate offset is not the same for each layer, and the trainable offset can effectively preserve the extracted features.

III. ON-CHIP TRAINING METHODS

A. Related Work

For on-chip training and inference, the most recent studies show that training needs at least 8 bits of precision to ensure accuracy [13]–[15] although precision can be extremely low at the inference phase. Most of the related work focuses on training models from scratch and building a software framework [16] for quantized training to reduce computational resources. Yang et al. [14] observed the requirement of a large
Fig. 4. Gradient distribution of our KWS model on the personal dataset before quantize (top) and after quantize (bottom).

bit width to realize model convergence, and thus introduce a layer-wise scaling factor and an extra flag bit to solve the problem. Instead, this article uses a more straightforward scaling method, as mentioned later. Zhu et al. [15] suggested clipping the gradient value for integer training, but the clipping value is based on the cosine distance between the floating point gradient and its quantize–dequantized counterpart, which is impractical in the edge device. Banner et al. [13] proposed the range BN for a higher tolerance to quantization noise, but collecting BN statistics has a high overhead on hardware. Furthermore, since a small training dataset has too much variation, changing the BN statistics may make training unstable. Therefore, this article decides to freeze the BN statistics during training.

B. Model Customization

For model customization, this article fine-tunes the last classification layer, which can avoid computational overhead and storage for backpropagation of the internal layers. Additionally, the required feature map will be used right after the error calculation without storing it in a buffer. This will also be hardware-friendly.

To implement this fine-tuning in hardware, we choose 8-bit fixed-point for the training part since fixed-point numbers are more hardware-friendly than floating-point numbers. However, when this on-chip fine-tuning is implemented with hardware-friendly quantized computation units, it is easy for the on-chip fine-tuning to fail because of the quantized value. In the following, we will propose hardware-oriented techniques to make on-chip fine-tuning more robust and hardware-friendly.

C. Error Scaling

Training from scratch in a low-precision format has been proven to work well. However, when fine-tuning a pre-trained model, most of the error values will be close to zero, as shown in Fig. 4, since the model has converged well. These small error values will be quantized to zero after quantization, causing the model not to learn any information from the personal data. Thus, we add a scaling factor before the error quantization. For a desired scale error ScaleError as shown in (1), its scaling factor can be derived as (2) to make training more general. This method does not need an extra flag bit, as in [14] to indicate whether the absolute value is smaller than the scaling factor.

![Algorithm 1 Small Gradient Accumulation (SGA)]

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\[
G : \text{The weights gradient value of this iteration} \\
G_{\text{accu}} : \text{The accumulated gradient value} \\
G_{\text{th}} : \text{The accumulation threshold} \\
G_{\text{update}} : \text{The gradient value used to update weights} \\
\text{if } G < G_{\text{th}} \text{ then} \\
\quad \text{if } G_{\text{accu}} < G_{\text{th}} \text{ then} \\
\quad \quad G_{\text{accu}} \leftarrow G_{\text{accu}} + G \\
\quad \text{else} \\
\quad \quad G_{\text{update}} \leftarrow G_{\text{accu}} + G \\
\quad \quad G_{\text{accu}} \leftarrow 0 \\
\quad \text{end if} \\
\text{else} \\
\quad G_{\text{update}} \leftarrow G \\
\text{end if}
\]

D. Small Gradient Accumulation

As mentioned above, most of the gradient values are close to zero after quantization, and therefore the gradient values will be too small to change the model weights. In addition, these gradient values will become smaller updated weight values since the learning rate (LR) during fine-tuning is also quite small, which will make the model easily stop learning at the early training stage.

To avoid this, we accumulate the gradient whose value is smaller than the threshold. Once the accumulated gradient is larger than a threshold, we use the accumulated gradient to update the weight and then reset the accumulated value to 0. These accumulated values are in 16-bit fixed-point format to ensure that the training will not use any full precision number. The pseudocode is shown in Algorithm 1. In which


### TABLE I

**Examples for Threshold Values With Min (Weight) = 1/128**

| LR=0.05 | LR=0.01 | LR=0.001 |
|---------|---------|----------|
| Threshold | 0.078  | 0.039  | 0.39     |

Fig. 5. (left) Weight update with random gradient prediction, where the yellow arrow means the random direction. (right) Weight update without random gradient prediction.

the quantization threshold $G_{th}$ depends on the LR. Equation (3) shows the relationship, where $\text{min}(\text{weight})$ means the minimum weight value that can be expressed. Table I shows some examples of the threshold value when the weight value is quantized to one sign bit and seven decimal bits, which means that $\text{min}(\text{weight})$ is $1/128$

$$G_{th} = \frac{\text{min}(\text{weight})}{2} \times LR.$$  (3)

### E. Random Gradient Prediction (RGP)

When the training dataset is small enough, we can read all data in a single batch, which means that the input data for the last layer will be very close in each epoch. Thus, we add Gaussian noise to predict the gradient of the next epoch as the following equation:

$$G' = G + \text{quantize} \left( \frac{\text{rand}}{\lambda} \right).$$  (4)

In (4), rand is a random sample of the Gaussian distribution, and the value of $\lambda$ is a hyperparameter. With a suitable value of $\lambda$, the noise value will not dominate the update direction and can avoid the model stuck at the local minimum. Another advantage is that we can ensure that the small truncated error caused by the hardware calculation will not affect the overall training of the model. Fig. 5 illustrates this weight update method.

### IV. DESIGN FOR NONIDEAL EFFECTS OF THE IMC MACRO

The IMC macro used in this article is based on the binary neural network macro from our previous work [17]. One IMC macro contains eight $64 \times 64$ banks as Fig. 6 to compute eight outputs, which is equivalent to the size of 4 KB. This macro uses 8T SRAM bit cells from the foundry to avoid a read disturb problem. For multiplication and accumulation in a convolution, weights are first written into the 8T SRAM array. The read bitlines (RBLs) are precharged according to the input data. Then a wordline of weights are read from the SRAM to decide whether to discharge or keep the RBL voltage according to the weight as the multiplication results. These results are accumulated and averaged by charge sharing on AVG lines ($AVG_P$ and $AVG_N$) based on their sign. Finally, the AVG lines will be sent to SAs to convert them into 1-bit output results. For more details, see [17]. Due to this analog computing for multiply and average (MAV), IMC has some model design limitations and nonideal effects as shown below.

#### A. Limited BN Range and Value

The in-memory BN mapping is the same as the weight mapping, which will map a bias value to a wordline of memory cells. For example, to map 32 to our $64 \times 64$ IMC array, half of a wordline of memory cells will store “1” as “+1,” and the other half will store “0” as “−1.” The input for the in-memory BN is set to 1. Thus, bias = $\sum_{i=0}^{63} W_i$. For example, assume that bias = $W_0 + W_1 + W_2 + W_3$. If all $W_i = 1$, bias = 4. If $W_0 = −1$ and other $W_i = 1$, bias = $−1 + 1 + 1 + 1 = 2$. Thus, the BN bias is even only if the width of the memory array is even (as in our case). Similarly, the BN bias will be odd only if the width of the memory array is odd. To fit such constraints for in-memory BN mapping, we tried four different mapping methods: add, absolute add, sub, and absolute sub, on the target model. The one with the lowest accuracy drop will be selected as the choice.

Furthermore, the BN bias value will be limited to $(-64, 64)$ due to the crossbar size of our IMC macro. To solve this problem, we first analyze the distribution of the BN bias, as shown in Fig. 7. In this case, most of the BN bias does not exceed the limitation of $(-64, 64)$, and thus the limited BN range has almost no impact on the accuracy of the model.

#### B. MAV Offset and SA Sensing Variation

The convolution result of the IMC macro is not as ideal as in the software case due to the MAV offset and SA sensing variations. This will lead to a catastrophic failure of the model if we do not take any compensation measures. For the MAV offset, the MAV result is decided by the voltage difference between $AVG_P$ and $AVG_N$. This voltage difference shall be zero if the numbers of positive and negative values are the same in the ideal case. However, this difference (denoted as
the MAV offset) is not zero due to the matching problem. For SA sensing variation, the requirement of SA circuit input resolution is very high. Therefore, when the difference of two inputs is small, the variation may lead to the wrong comparison result.

To solve the above issues, we treat the MAV offset and SA variations as a random offset noise for inference, which is based on the Monte-Carlo simulation results with PVT variations. We applied this random noise to the model inference and compared the convolution results with the original ones to collect the statistics of their difference. A bias is then determined based on the statistics to restore the results as the original ones. This extra bias can be combined with the in-memory BN bias, since most of the BN bias values are within the limitation. After the compensation, we fine-tune the model for a few epochs, which could almost recover the accuracy drop due to these nonideal effects.

V. PROPOSED ARCHITECTURE

A. Overall Architecture

Fig. 8 shows the overall architecture for our six layer KWS model. This design stores all weights in the IMC macros to avoid weight load/store overhead. For the model, we implement the first layer with digital circuits since the resolution of SA is too low to achieve the model requirement. Moreover, the final global average pooling (GAP) layer and fully connected layer are implemented by digital circuits as well for higher bit precision requirements. The other binarized group convolution layers are all implemented by the IMC macro as shown in Fig. 9, which consists of an IMC macro for convolution and in-memory BN computation and digital domain computations such as BN decoder for correct sign operation, channel shuffle, and pooling. The input data are from the previous layer or the buffer, and the output data is also output to the next layer or buffer. In addition, we have added a test mode to check the correctness and impact of nonideal effects of each IMC macro, which can monitor the circuit variation of MAV and SA based on the input pattern and the result of each IMC macro. For our KWS task, the hardware utilization of each layer is (L1: 100, L2: 100, L3: 50, L4: 25, L5: 25, L6: 12.5) due to the pooling layer.

B. Sinc Convolution Circuits

Fig. 10 shows the block diagram for the sinc convolution layer, which consists of eight PEs for eight channel results in a single cycle to meet throughput requirements. Each PE computes 15 (kernel size) \( \times \) 8 (input bitwidth) XNOR operations for binary multiplication and accumulates them along with the BN bias as the channel output. The BN computation in this layer is also simplified as a bias value as the in-memory BN due to the binary output, which can be implemented with an adder instead of complex circuits.

C. On-Chip Training Circuits

Fig. 11 shows the proposed on-chip training flow for model customization. Fig. 12 shows the hardware block diagram of the training circuits. First, the input feature for the last layer will be stored in an SRAM buffer for data reuse during the...
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**VI. EXPERIMENTS AND RESULTS**

**A. Results of Model Customization**

1) Original Dataset: In our experiment, we use ten keywords in the Google speech command dataset (GSCD). They are: yes, no, up, down, left, right, stop, go, ON, OFF. Each utterance is an audio file of nearly one second with a total of 18947 training utterance and 4735 test utterance.

2) Personal Dataset: The personal dataset is collected from three people with 607 utterance, where each utterance is also nearly one second. We use three utterance from each person as the training set for each keyword, which means that the customization training set will have three utterance \( \times 10 \) keywords \( \times 3 \) people \( = 90 \) training utterance. The rest are used as test. In our experiments, we only show customization for three people at the same time to mimic the real application scenario in a family.

3) Settings: For the original model, we randomly add Gaussian noise with values within 0.001 to 0.015 and randomly shift the audio by \(-0.5\) to 0.5 s for data augmentation, and train the model for 500 epochs with Adam optimizer. The initial LR is set to 0.01 and gradually decreased to the minimum value \( 1 \times 10^{-9} \) during training.

For model customization, we fine-tune the model using the SGD optimizer for 1000 epochs. The initial LR is set at 1/16, which is decreased every ten epochs by a factor of 0.5 to the minimum value of 1/128. It should be noted that the LR cannot be set too low. Otherwise, the gradient value will be too small to update the parameters after multiplied by the LR. The quantization format for fine-tuning the classifier layer is listed as follows.

1) **Weight:** One sign bit, seven decimal bits.
2) **Activation:** One sign bit, three integer bits, four decimal bits.
3) **Gradient:** One sign bit, seven decimal bits.
4) **Error:** One sign bit, seven decimal bits.

4) **Performance of the Original Model:** Table II shows the accuracy result of the original model on GSCD and related comparisons. Our compressed model uses a 7 \( \times \) smaller model size with more than 90% accuracy due to the binary neural network compared to other state-of-the-art work.

| Model                  | Accuracy | Parameters | Model Size (bits) |
|------------------------|----------|------------|-------------------|
| DS-CNN-S [1]           | 94.1%    | 39K        | 1.2M              |
| TC-ResNet8 [18]        | 96.1%    | 66K        | 2.1M              |
| SincConv+GDSConv [19]  | 96.4%    | 62K        | 2M                |
| **Ours**               | 90.83%   | 125K       | 171K              |

For the simulation with MAV offset and SA sensing variation, the results in the table are the averages of the five random seed simulations to cover the randomness. The result has shown that nonideal effects will cause the model failure. However, accuracy can be restored to 89.76% after the proposed bias compensation and fine-tuning.
When applied this model to the personal dataset, the accuracy will be dropped to 75.94%, which can be further recovered with our customization approach.

5) Customization: Table IV shows the customization result. In this case, the baseline (full-precision) is fine-tuned with full-precision on GPU as a reference. As shown in the table, naively fine-tuning on the quantized hardware will significantly degrade the performance. With the proposed method, we can achieve a much better performance close to the full precision one. In the case of training with RGP, the accuracy is higher than in the full precision baseline, which seems to be unreasonable. This could be the error caused by the insufficient amount of our test data, since the loss of the full precision baseline is still lower than the RGP one.

Among the methods for on-chip customization, error scaling brings the largest gain, since it avoids training being early stopped. The accumulation of small gradients also improves the accuracy, which means that small gradients in the training process are important to improve the convergence of the model. Furthermore, for $\lambda$ in the random gradient prediction, our experiment shows that the value within a reasonable range (larger than 4) will not affect the result. Our method can make training on the fixed point hardware to get results comparable to that of the ideal model fine-tuning on GPU.

### B. Hardware Implementation Results

1) Results and Comparison: We have synthesized this design with Synopsys Design Compiler and performed the placement and routing with cadence encounter. All are in TSMC 28-nm CMOS technology. Fig. 13 shows the layout and summary of this chip. This chip can work at different clock rates ranging from 1 to 100 MHz at 0.9 V. Timing and power consumption are evaluated at the TT corner. The power is analyzed by Synopsys PrimeTime PX based on the post-layout results and the gate-level simulation pattern of the KWS. This chip achieves 23.6–68 TOPS/W for the real model considering all on-chip power and real task inference time for 100- and 1-MHz operating frequencies, respectively. The lowest power consumption is 89 and 105 $\mu$W in the inference and training phase on the 1-MHz clock.

Table V compares this work with other state-of-the-art works. Due to the difference of model and technology, the comparison is only possible to a limited extent. Most of the other works used MFCC for feature extraction and VAD for voice activity detection [2]–[6]. Since the VAD is for power savings, this could be integrated into this work as well. In this comparison, this work consumes less power than other works with similar model architecture [2], [5], [6] even though we process the entire raw data for the predicted results. Dhouk et al. [3] and Guo et al. [4] used RNN as the model architecture, but [3] does not include feature extraction on the chip.

Another key point of this work is that we combine the IMC architecture for higher energy efficiency. Dhouk et al. [3] and Guo et al. [4] also used IMC and [5], [6] uses approximate computation that is also an analog domain computation for lower power consumption. Zheng et al. [2] is the full digital design counterpart for a similar application. Compared to these state-of-the-art works, this work has higher energy efficiency and on-chip training capability for customization.

2) Hardware Analysis: Fig. 14 shows the power breakdown for model inference on the 1-MHz clock. In this case, most of the power is consumed by the fully connected layer and the IMC controller, since the fully connected part includes a large SRAM buffer and high-precision computation, and the IMC controller is implemented by many Flip-Flops. Therefore, the relative power consumption is higher. Furthermore, for higher throughput, the first layer needs more hardware overhead for greater parallelism, which occupies 18% of the power. At the same time, the computation of the analog part consumes only 3% of the total power. The leakage power will dominate the power consumption when the clock rate is low, as shown in Fig. 15.
Table V

| Technology          | This work | TCAS2019 [2] | ISSCC2020 [3] | VLSI2019 [4] | IEEE2019 [5] | IEEE2019 [6] |
|---------------------|-----------|--------------|---------------|--------------|--------------|--------------|
| Algorithm           | Sinet + CNN | MFCC + CNN | MFCC + CNN | MFCC + CNN | MFCC + CNN | MFCC + CNN |
| Dataset(keyword number) | GSCD(10) | TIMIP/TIDIGITS/HOME(1) | GSCD(7) | GSCD(10)/Hey snips(1) | GSCD(10) | GSCD(10) |
| Accuracy(%)         | 89.76/96.52↑ | 93.3/98.6/96.0 | 90.38 | 90.5/91.9/98.0 | 89.7 | 90.51 |
| Architecture        | digital + IMC | digital | digital + IMC | digital + IMC | mixed mode | mixed mode |
| Weight/activation bits | 1/1       | 1/1 | mixed (4, 8) | 1/1 | 1/(4, 8, 16) | 7/8 |
| Core area(mm²)      | 1          | 1.29 | 4.13 | 6.2 | 0.94 | 0.75 |
| Normalized core area(mm²)¹ | 1          | 1.29 | 0.77 | 1.15 | 0.94 | 1.21 |
| SRAM buffer size (KB) | 24         | - | 36 | 10 | - | - |
| Frequency (MHz)      | 1/100      | 2.5-50 | 1000 | 5-75 | 2.6 | 0.25 |
| Latency (ns)         | 160-1.6   | 0.5-10 | 0.0399 | 0.137 | 20 | 20 |
| Power (mW)           | 89-2833    | 141 | 11000 | 26000 | 77.8 | 52 |
| Normalized power (mW)² | 89-2833    | 328 | 3838 | 9072 | 175 | 177 |
| Energy efficiency (TOPS/W)³ | 23.6-68    | 90 | 0.91 | 11.7 | 137 | 46.8 |
| Normalized energy efficiency (TOPS/W)³ | 23.6-68 | 38.7 | 2.6 | 33.5 | 60.9 | 13.7 |
| Remark               | Customization | - | No preprocessing | - | - | - |

¹ Normalized core area = Core area / 28² / tech²
² Normalized power = Power * (28 / tech) * (0.9² / voltage²)
³ Normalized energy efficiency = energy efficiency / ((28 / tech) * (0.9² / voltage²))

In our implementation, the circuit for the training part only adds 5% of the area in the overall design, around 9187 gate count, which means that our additional cost for the model customization function is relatively low. Within the training part circuits, the area is dominated by the large SRAM buffer for feature map storage.

VII. Conclusion

This article presents a low-power SRAM-based IMC design with model customization for KWS, which is optimized from algorithm to hardware. For the algorithm, we propose an IMC-aware model with fewer parameters to achieve over 90%
accuracy and solve the nonideal effects of IMC macro with bias compensation and fine-tuning. The model customization is designed to be executed on an 8-bit fixed-point quantitized hardware. The limitation of the quantized hardware training is solved by scaling error, accumulating small gradients, and adding random gradients. The results show that the proposed approach can successfully restore accuracy and achieve a similar performance compared to fine-tuning with full precision. The hardware implementation uses hybrid digital/IMC computing to get better energy efficiency and fit model precision requirements, which has higher energy efficiency and also delivers on-chip model customization capability when compared to the state-of-the-art works.

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