Design and Simulation of a Small Power Two-Bit MC Circuit via Full Adder Logic

Soumik Bhattacharjee, Aparna Vyakaranam, Satya Devu Svpk, SSS Shameem, Rafida Sulo, Ahmad Anwar Zainuddin*

Computer Science and Engineering, School of Engineering, Manipal International University, Negeri Sembilan, Malaysia.
*Corresponding Author: ahmad.anwar@miu.edu.my

Abstract. In Very Large-Scale Integration (VLSI) systems, a magnitude comparator (MC) is a component of Arithmetic Logic Unit (ALU) used to make binary decisions. Recent technologies demand the use of power-efficient methodologies as well as techniques that require a lesser number of transistors. In this paper, a magnitude comparator is developed using full adder design logic. Full adders are basic components of the ALU which is the logical and arithmetical unit of the microprocessors and Digital Signal Processing (DSP). This design consumes less power and area when compared to other logic styles in the literature. The proposed comparator has been designed using DSCH 3.5 and simulations are done on Microwind 3.5 via 0.12 μm technologies. This comparator shows a power consumption of 31.746 μW using 36 transistors. The proposed design exhibits a full adder logic-based comparator with less power consumption and transistor count as compared to those in recent literature.

1. Introduction

The rapid development and modification of modern sophisticated electronic circuits and equipment led to the creation of many intelligent systems for applications in different industries. VLSI circuits with high computation speed and low power loss are needed for these smart systems. Low-power, high-speed portable devices are needed by industries. These VLSI circuits provide sufficient performance to satisfy certain requirements. The new microprocessors need highly efficient circuits with limited area usage. Their advanced features and high integration density must be maintained. Build methodologies on VLSI circuits have thus gained enormous interest in the research community.

In VLSI circuits, the magnitude comparator (MC) is an essential component of the ALU that helps make decisions between two binary numbers, such as whether one is equal to, greater than, or less than another binary number. Binary number analogy is a concept that can be used to explain this phenomenon. [1]. A magnitude comparator, in general, takes two binary numbers as inputs and outputs the binary comparison results. The result of a 2-bit comparator is determined by three variables, each of which indicates A<B, A=B and A>B. While the XNOR gate functions as a simple 1-bit comparator, as the bit size expands, other components are required [2]. The block diagram of a 2-bit comparator is shown in Figure 1.
MC is applied in training sorting in microprocessors for multiprocessing and parallel processing [3]. To maintain high efficiency, digital signal and parallel processing operations necessitate efficient MC circuits. Furthermore, it is commonly used as an elementary component in Digital Signal Processing (DSP) circuits for data processing [4]. Additionally, comparators are used in modern microprocessors to perform the task of decoding binary commands. Hence, recent technologies demand comparators to operate with smaller number of transistors for miniaturizing capabilities and low power consumption. The aim of this project is to design and simulate a small power two-bit MC circuit based on full adder logic. The proposed schematic is to be designed on DSCH 3.5 and the layout will be simulated in Microwind EDA. Another objective of this study is to review recent works on 2-bit comparators and compare their performance with this proposed work.

The paper is arranged as follows: After this introduction, the architecture of full adder circuit is presented in Section II which focuses the truth table for full adder. Section III focuses on the study of previous works in research methodology. Section IV discusses the proposed work. Section V describes the results and findings on the circuit which is simulated using DSCH 3.5 and Microwind EDA. Finally, section VI summarizes and concludes this paper.

2. Related Research Works
There have been many designs of magnitude comparators based on different kinds of logic techniques each of which have different outputs of power consumption as well as area. Different technologies are employed to build faster and energy efficient logic circuits. Physical components of circuits, on the other hand, have limitations that limit the speed and energy efficiency that can be achieved [6]. As a result, binary comparator circuits have been designed to reduce circuit implementation area, delay, and power loss [3]. Table 1 summarizes the recent literature on the magnitude comparators using various design techniques along with their average power consumption.

Conventional CMOS logic requires 66 transistors to build a 2-bit comparator but [3] and [7] have used a hybrid logic along with C-CMOS thus using no more than 46 transistors. Both produce efficient comparators consuming 9.865μW and 7.642μW respectively when simulated at 90nm technology. These hybrid technologies reduce the area by using lesser transistors. However, pass transistor logic (PTL) provides good performance with even lesser number of transistors as seen in [8], [9] and [10]. This technique also obtains very low power dissipation of 1.394μW, 2.423μW, and 0.068μW, respectively. CMOS technique show ineffective results due to its high power consumption [2] and large circuitry area. In comparison, another popular technique called the GDI technique requires lesser number of transistors and consumes low power for the implementation of different logic styles. In this technique a simple cell consisting of only two transistors and three inputs are used to implement various complex functions. A 2-bit magnitude comparator developed by [11] shows 9.791μW of power dissipation with 30 transistors using the GDI technique. 2-bit comparators using Full adder logic as seen in [12] and [5] provide high performance in terms of power consumption of only 9.341μW and 0.818μW covering 326.2μm² and 290.8μm² area, respectively. These techniques include two complete adders, two inverters at one input, two AND gates at comparator output, and one XOR gate at output. This work proposes an efficient logic design of a 2-bit comparator using full adder logic.
Table 1. Recent Works on Two-bit MC using different design methods.

| References | Year | Technology | Comparator Type | Transistor Count | Power   | Area      |
|------------|------|------------|-----------------|------------------|---------|-----------|
| [2]        | 2015 | 45nm       | CMOS            | 174              | 0.311mW | 769μm²   |
| [2]        | 2015 | 45nm       | GDI             | 78               | 0.164mW | 187μm²   |
| [3]        | 2019 | 90nm       | C-CMOS hybrid logic | 46        | 9.865μW | Not specified |
| [5]        | 2014 | 90nm       | Full adder Logic | 24 routed wires | 0.818 mW | 290.8μm² |
| [7]        | 2020 | 90nm       | Hybrid CCMOS, PTL | 46        | 7.642 μW | Not specified |
| [8]        | 2017 | 180nm      | PTL             | 40               | 1.394μW | 44.657μm² |
| [9]        | 2015 | 45nm       | PTL             | 24               | 2.423 μW | 121.8μm² |
| [10]       | 2013 | 90nm       | PTL             | 40               | 6.836e-9 W | Not specified |
| [11]       | 2014 | 45nm       | GDI             | 30               | 9.791 μW | Not specified |
| [12]       | 2014 | 120nm      | Direct Full Adder logic | 30 routed wires | 9.341 μW | 326.2μm² |
| [13]       | 2015 | 45nm       | Full Adder      | 100              | 85.500 μW | Not specified |
| [13]       | 2015 | 45nm       | Hybrid PTL/CMOS | 56               | 4.430 μW | Not specified |
| [14]       | 2014 | 120nm      | GDI Full Adder  | 56               | 13.739 μW | 1320.3μm² |
| **This work** | 2021 | 120nm      | Full adder Logic | 36               | 31.746 μW | 437.84μm² |

3. Theoretical Framework
A fundamental complete addition consists of 3 inputs and 2 outputs that are sum and carry. The logic circuit of this complete adder can be implemented with the AND gate, XOR gate and OR gate support logic. Table 2 provides a true table for a classic complete adder logic. The sum logic includes XOR gates while the transport logic contains AND and OR gates. Complete adder is one of many digital VLSI circuit’s main building blocks. Since its invention, its structure has been changed many times. Moreover, Amendments are made to reduce the number of transistors, reduce power consumption, and ultimately improve operating speed [5]. A simple complete adder logic diagram is shown in Figure 2.

Table 2. Complete Adder Truth Table.

| A | B | C<sub>in</sub> | Sum | Carry (C<sub>out</sub>) |
|---|---|----------------|-----|------------------------|
| 0 | 0 | 0              | 0   | 0                      |
| 0 | 0 | 1              | 1   | 0                      |
| 0 | 1 | 0              | 1   | 0                      |
| 0 | 1 | 1              | 0   | 1                      |
| 1 | 0 | 0              | 1   | 0                      |
| 1 | 0 | 1              | 0   | 1                      |
| 1 | 1 | 0              | 0   | 1                      |
| 1 | 1 | 1              | 1   | 1                      |
Recent literature shows various techniques of designing a low power magnitude comparator [2], [5], [3], [7]–[14]. It is seen that Full Adder Logic style provides low power consumption with respect to their small area. This paper offers a two-bit comparator design using a logical style Full Adder. Figure 3 illustrates a (basic) Full adder based two-bit comparator. Table 3 displays the truth table of a complete adder-based comparator to consider the logic of a comparator.

![Figure 2. Full Adder Logic Diagram.](image)

**Table 3.** Two-bit Comparator table based on the simple Complete Adder Logic.

| A0 | A1 | B0 | B1 | A>B | A<B | A=B |
|----|----|----|----|-----|-----|-----|
| 0  | 0  | 0  | 0  | 0   | 0   | 1   |
| 0  | 0  | 0  | 1  | 0   | 1   | 0   |
| 0  | 0  | 1  | 0  | 1   | 0   | 0   |
| 0  | 0  | 1  | 1  | 0   | 1   | 0   |
| 0  | 1  | 0  | 0  | 1   | 0   | 0   |
| 0  | 1  | 0  | 1  | 0   | 0   | 1   |
| 0  | 1  | 1  | 0  | 0   | 1   | 0   |
| 0  | 1  | 1  | 1  | 0   | 1   | 0   |
| 1  | 0  | 0  | 0  | 1   | 0   | 0   |
| 1  | 0  | 0  | 1  | 1   | 0   | 0   |
| 1  | 0  | 1  | 0  | 0   | 0   | 1   |
| 1  | 0  | 1  | 1  | 0   | 1   | 0   |
| 1  | 1  | 0  | 0  | 1   | 0   | 0   |
| 1  | 1  | 0  | 1  | 1   | 0   | 0   |
| 1  | 1  | 1  | 0  | 1   | 0   | 0   |
| 1  | 1  | 1  | 1  | 0   | 1   | 0   |

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Figure 3. Two-bit Comparator based on basic Full Adder Logic.

4. Proposed Work

A classical full adder consists of 2 XOR gates, 2 AND gates and one OR gate using 18 transistors in total. A basic full adder-based comparator may consume up to $1\mu W$ power as seen in [5]. The following work explains a new design style based on full adder logic. This design is seen to consume less power with respect to the area covered. Moreover, the number of transistors is comparatively lesser here than in other logic styles. The schematic layout is designed on DSCH 3.5 the diagram of which is shown in Figure 4. While the layout conversion is carried out in Microwind 3.5. There are four inputs for the 2-bit comparator, namely A0, A1 and B0, B1. This new comparator design uses two 16 transistor full adders and additionally two AND gates which are of 2 transistors each.

Figure 4. Schematic logic design of proposed comparator on DSCH 3.5.
5. Results and Discussion
When simulated at 120nm technology on DSCH 3.5, a timing diagram shown in Figure 5 is obtained. A Verilog file is extracted from the schematic layout which is simulated in Microwind 3.5. Figure 6 shows the layout of the proposed 2-bit comparator. Figure 7 is the timing diagram obtained from the layout simulation. It obeys the truth table of a basic comparator shown in Table 3. Power dissipation of this circuit as shown is 31.746 μW when input voltage is set at 1.2V. The area covered by the layout design is found to be 437.84μm². From the results, it can be stated that the proposed design using 36 transistors consumes less power than references [2], [5] and [13]. It can also be noticed that this design consumes less area than [2] and [14].

![Figure 5. Timing diagram of proposed comparator on DSCH.](image)

![Figure 6. Layout design of proposed comparator on Microwind 3.5.](image)
6. Conclusion
This paper describes various logical styles for implementing a 2-bit magnitude comparator and proposes a low power and size efficient, complete adder style design. The proposed nature of the comparator requires less power than other logical types in literature. The proposed design provides greater performance than concepts based on Complete Adder and hybrid CMOS technology as seen in the literature with a power consumption of 31,746 $\mu$W and 36 transistors. The future scope of this paper is hybrid design to further reduce the area and transistor count with static CMOS design as demonstrated in [15].

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