Remapped Cache Layout: Thwarting Cache-Based Side-Channel Attacks with a Hardware Defense

We propose Remapped Cache Layout (RCL) — a pure hardware defense against a broad range of conflict-based side-channel attacks. RCL obfuscates the mapping from address to cache sets; therefore, an attacker cannot accurately infer the location of her data in caches or using a cache set to infer her victim’s data. To our best knowledge, it is the first defense to thwart the aforementioned largely undefended side-channel attacks. RCL has been implemented in a superscalar processor and detailed evaluation results show that RCL incurs only small costs in area, frequency and execution time.

1. INTRODUCTION

For decades computers have been designed to run applications fast and energy-efficiently. As one of the key enabling techniques, caches are utilized to bring recently and frequently used data close to cores. They are scarce microarchitectural resources which are dynamically shared between processes, cores and virtual machines (VMs). To exploit the full benefits of caches, they are mostly self-managed [1] in a way that address space isolation is relaxed and traded for cache efficiency. As a result, data from different processes, cores and VMs can reside in the same cache set and interfere with each other. This interference opens a gate for various types of cache-based side-channel attacks.

As cache-based side-channel attacks become serious security problems for current computers, various defenses have been proposed and deployed in both software and hardware. Consequently, cache-based side-channel attacks on processes co-residing on the same core are becoming extremely difficult. Most of recent attacks then shift their focus to the last-level cache (LLC). Although cache partitioning is currently the most promising defense against the attacks abusing LLC, it is ineffective in thwarting the side-channel attacks that automatically create eviction sets or bypass the user address space layout randomization. In fact, these attacks are largely undefended in current computer systems.

We propose Remapped Cache Layout (RCL) — a pure hardware defense against a broad range of conflict-based side-channel attacks. RCL obfuscates the mapping from address to cache sets; therefore, an attacker cannot accurately infer the location of her data in caches or using a cache set to infer her victim’s data. To our best knowledge, it is the first defense to thwart the aforementioned largely undefended side-channel attacks. RCL has been implemented in a superscalar processor and detailed evaluation results show that RCL incurs only small costs in area, frequency and execution time.

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their focus to the last-level cache (LLC) because it is shared by processes running on different cores. The cflush instruction of Intel x86-64 has been extensively exploited in flush-based cross-core attacks to manipulate the memory shared between processes [8,9]. In the case where memory sharing is impossible, attackers can launch conflict-based attacks by triggering accurate cache eviction inside LLC [10,11]. Furthermore, advanced attackers are capable of automatically creating eviction sets [12], locating the security-critical data [13], bypassing the address space layout randomization (ASLR) [14,15], and breaking the Intel SGX or ARM TrustZone isolation [16,17].

Cache partitioning [18] is currently the most promising defense against attacks abusing LLC. Cache partitioning separates security-critical data from normal data; therefore, attackers cannot flush security-critical data or evict them using normal data. However, cache partitioning is ineffective when security-critical data cannot be easily separated from normal data [17,19] or normal data become the attacking targets [14,15]. As a result, cache partitioning fails to thwart attacks that automatically create eviction sets [12] or bypass the user ASLR [15], leaving them largely undefended in current computer systems.

In this paper, we propose Remapped Cache Layout (RCL) – a pure hardware defense against a broad range of conflict-based side-channel attacks. Unlike cache partitioning which seeks to separate security-critical data from normal data, RCL obfuscates the mapping from address to cache sets; therefore, an attacker cannot accurately infer the location of her data in caches or using a cache set to infer her victim’s data. To our best knowledge, RCL is the first defense to thwart the aforementioned largely undefended attacks. RCL is also a pure hardware defense which requires no software involvement. In summary, the main contributions of this paper are as follows:

- A pure hardware defense against a wide range of conflict-based side-channel attacks, namely Remapped Cache Layout (RCL), is proposed.
- A systematic review of the common cache-based side-channel attacks and the existing defenses shows that three types of advanced attacks are largely undefended in current computer systems.
- A detailed analysis reveals how RCL thwarts these three types of attacks.
- RCL has been implemented in a superscalar processor and the evaluation results show that RCL incurs only small costs in area, frequency and execution time.

2. CACHES IN MODERN PROCESSORS

In modern processors, caches are utilized to store recently or frequently used data to reduce access time. Data are stored in units of fixed-sized cache lines. Caches are organized in a hierarchical structure. Each core contains a pair of small but fast private L1 caches for data (L1-D) and instruction (L1-I). The core may contain a medium-sized and unified level-two (L2) cache. All cores share a large but comparatively slow LLC cache. Commonly, caches are set-associative which allows a group of cache lines to reside in one of the many cache sets. Cache sets are addressed by an internal cache index, which is typically a subset of the address bits shared by all cache lines in the same set. When a new cache line is fetched but the corresponding cache set is full, a cache replacement policy chooses and evicts a cache line from this set.

A typical L1 cache is addressed by the virtual address (VA), while other levels of caches are addressed by the physical address (PA). The VA to PA translation in L1 caches proceeds in parallel with cache set accesses. A translation lookaside buffer (TLB) is used to reduce this translation latency. The mapping from VA to PA is managed by the OS kernel in units of pages. The whole mapping is recorded in a page table stored in memory. The aforementioned TLB caches the recently accessed mapping so that no actual access to the page table is needed for a recently accessed page.

An inclusive cache hierarchy is normally assumed, where a cache line evicted from LLC is also purged from all cache levels. A cache coherence protocol is utilized to ensure data are correctly updated in all levels of caches.

3. ATTACK CLASSIFICATION

Cache-based side-channel attacks involve an attacker and a victim sharing a cache. The attacker utilizes this cache to infer information belonging to the victim. Table 1 provides a summary of common cache-based side-channel attacks.

A: Conflict-based side-channel attacks

Conflict-based side-channel attacks [30] exploit the fact that caches indiscriminately store congruent cache lines (lines sharing the same subset of address bits) in the same cache set. This allows attackers to maliciously prime certain cache sets using her own data (such as Prime+Reload [2]) or evict the victim from certain cache sets (such as Evict+Time [3]). According to the level of caches being targeted, conflict-based side-channel attacks have two varieties:

A-1: Conflict-based attacks targeting the co-resident processes sharing the L1 cache. Since the L1 cache is small and fast, the attacker can extract detailed information with low noise and at high speed. To synchronize with her victim, the attacker can utilize SMT to run concurrently with the victim [23] or preempt her victim at short intervals [3,20]. However, running attacking process on the same core with the victim can be difficult in multicore processors. Most cloud service providers have disabled SMT and disallowed multiple VMs running on the same core.

A-2: Conflict-based cross-core attacks targeting LLC. To remove the co-residence requirement, a conflict-based attacks can be launched from a process running on another core or even another VM [10,12,21,22] through side-channels in LLC. What is worse, the advanced attacks can automatically create eviction sets [12,29] or
discover security-critical data [11]. This is the by far the most sophisticated type of cache-based side-channel attacks and is thus classified separately as type C.

**B: Flush-based side-channel attacks**

Although conflict-based side-channel attacks are powerful and extremely adaptive, when the target memory is shared between the attacker and her victim, with the permission of the OS, the attacker can easily launch side-channel attacks by flushing the cache lines of interest. Unfortunately, the cflush instruction of the Intel x86-64 ISA deliberately allows user applications to flush cache lines from LLC, which becomes a notorious vulnerability utilized by a family of attacks [12, 29, 31].

As a prerequisite, the target memory must be shared between the attacker and her victim. Shared libraries have been used to attack processes running in the same OS [22]. The physical page mapping exposed by some OSs (/proc/self/pagemap) and memory deduplication have been used to launch cross-VM attacks [8, 22, 29]. Although both vulnerabilities have been neutralized in latest OSs and VMs.

**C: Automatic side-channel attacks**

As mentioned in A-2, advanced conflict-based attacks become adaptive at run-time.

**C-1: Automatically creation for eviction sets.** When an attacker runs in non-pointer environment, she cannot even obtain the VAs of her own variables. To launch conflict-based attacks targeting LLC, attacker must create eviction sets to trigger accurate cache evictions. For this purpose, a large amount of memory is acquired using system APIs [14, 29] or larger pages [12]. A blinded but optimized search algorithm [12] is then used to create eviction sets at run-time.

**C-2: Reversing the VA to PA mapping.** Furthermore, attackers can mobilize the eviction sets created by C-1 to exploit other side-channels, such as the row buffer in current DRAM chips. By exploiting the PA invariance related to the row buffer, the attacker can infer a part of the PA of the created eviction set [14, 30, 31].

**D: Page table side-channel attacks**

Since modern processors cache the recently accessed page table entries (PTEs) in L1-D cache, caches are exploited to break the ASLR protection.

**D-1: Bypassing the user ASLR.** If running in a sandboxed environment, the virtual memory space is normally randomized by ASLR. As the first step to jailbreak the sandbox, an attacker can launch conflict-based attacks on the cached PTEs to bypass ASLR [15].

**D-2: Bypass the kernel ASLR.** ASLR has also been used to randomize the kernel memory space as a first defense against code-reuse attacks [15, 46]. To break the kernel ASLR, attackers can flush or prefetch the targeted PTE from the L1-D cache and then reload the target page. A timing difference could be detected if the page exists [19, 32].

**E: Privileged side-channel attacks**

If an OS kernel is malicious, the kernel can launch direct side-channel attacks on trusted execution environment (TEE) [43], such as the Intel SGX [16, 17, 33] and the ARM Trustzone [34, 35]. These attacks normally exploit the facts that TEEs still rely on the kernel to allocate memory and a malicious OS kernel can launch flush-based cache attacks using PAs rather than VAs, which significantly increases accuracy.

### 4. EXISTING DEFENSES

Various defenses have been proposed using software, hardware or together. For the various types of attacks, some types are better resolved in software but many are better handled by hardware to avoid software modification and severe performance loss.

On the software side, most cryptography standards are hardened with constant-time programming [47] utilizing the cryptographic instruction extensions supported by major processors [48, 49]. Furthermore, enforcing the flushing of local caches (including L1 caches) during process switching appear to be effective for all cross-process attacks targeting L1 caches. Deploying the Intel hardware transnational memory support to enforce the preloading of security-critical data upon context switch also shows strong defense against all cross-process attacks. Optimistically speaking, cache-based side-channel attacks targeting co-resident processes sharing the L1 cache (sub-type A-1) can be effectively handled by software defenses.

For conflict-based cross-core attacks targeting LLC
(sub-type A-2), using page color \[51\] or explicit management on LLC \[18,52\] to achieve cache partitioning has been proven effective. These defenses normally require changes in hypervisors. Explicit cache management also compromises the self-management of caches, which may lead to significant performance loss.

The flush-based cross-core attacks (type B) rely on the availability of flush and prefetch instructions, and the sharing of the target memory between the attacker and her victim. A majority of these attacks can be effectively resolved by constraining the flush and prefetch instructions \[39\], denying unprivileged accesses to page maps (/proc/self/pagemap) \[19\], and removing the memory deduplication in hypervisors \[9\].

The attacks trying to bypass the kernel ASLR (sub-type D-2) can be effectively resolved by separating the kernel virtual space from the user virtual space \[46\], namely the kernel page table isolation (KPTI).

On the hardware side, Table 2 summarizes the existing hardware defenses. Cache partitioning can be enforced in hardware as well. Both software and hardware cache partitioning can effectively thwart cross-process attacks. The hardware enforced partitioning reduces the burden of software \[6,18,29\] but may still require software to manage the cache set/way allocation \[18,37–39\].

| Defenses                     | Software modification       | A-1 | A-2 | B  | C-1 | C-2 | D-1 | D-2 | E  |
|-----------------------------|----------------------------|-----|-----|----|-----|-----|-----|-----|----|
| Cache partitioning          | Yes (set/way allocation)   | S   | S   | S  | W   | W   | W   | W   | M  |
| Random (pre-)fetch/decay    | Might (set fetch region)   | M   | M   | S  | W   | W   | M   | M   | M  |
| Random cache layout         | Might (set way priority)   | S   | W   | W  | M   | W   | M   | W   |
| Software isolation          | Yes (enclave management)   | S   | S   | S  | W   | W   | W   | W   | S  |

SW: software, S: strong, M: medium, W: weak.

In summary, software defenses can effectively thwart attacks of types A, B and D-2. Hardware defenses can effectively thwart attacks of types A, B and E. These leave the attacks of types C and D-1 largely undefended in current computer systems. To thwart these attacks, this paper proposes RCL, which also randomizes the cache layout but does not suffer from the limited randomization as the previous defenses do. A comparison will be provided in Section 9.

5. REMAPPED CACHE LAYOUT

As described in Section 3 A, conflict-based side-channel attacks exploit the fact that caches indiscriminately store congruent cache lines in the same cache set. To thwart conflict-based attacks, we propose Remapped Cache Layout (RCL), which deliberately randomizes the mapping from addresses to cache sets. In the view of attackers, irrelevant cache lines are stored in the same cache set; therefore, they cannot deterministically create eviction sets. Even if eviction sets are created using an automatic searching algorithm \[12\], it is extremely difficult to figure out which cache sets are evicted.

In a normal \(w\)-way 2\(s\)set L1-D cache, the cache index \(CI\) comes from the lower \(s\) bits of the VA\(^1\):

\[
CI = VA[s + 5 : 6] \quad (1)
\]

This direct mapping from VAs to cache sets (PA for other cache levels) is the fundamental microarchitectural vulnerability enabling all conflict-based attacks.

In a RCL enabled L1 cache, as depicted in Figure 1, the randomized cache index \(CI_R\) is calculated from both VA and PA:

\[
CI_R = RT(PA[k + s + 5 : s + 6]) \oplus VA[s + 5 : 6] \quad (2)
\]

Here \(k\) is a implementation defined parameter tuning the level of introduced randomness. RCL picks \(k\) bits from PA \((PA[k + s + 5 : s + 6])\) and uses it as an index to obtain an \(s\)-bit true random number from the random generator. The randomized cache index is:

\[
CI_R = RCI(RT(2^{k}VA[k + s + 5 : s + 6] \oplus 2^{k}RT(PA[k + s + 5 : s + 6]))) \quad (3)
\]

This mapping is effective only if both VA and PA provide enough randomness. The protection level against attack is given in Table 2. Here \(k\) is an implementation defined parameter tuning the level of introduced randomness.
6. SECURITY ANALYSIS OF RCL

Table 3 summarizes the effectiveness of RCL related to the common cache-based side-channel attacks listed in Table 1. RCL thwarts most attacks that need to evict cache sets. Most importantly, to our best knowledge, RCL is the first defense to thwart the automatic side-channel attacks (type C) and the attacks bypassing the user ALSR (sub-type D-1).

A: Conflict-based side-channel attacks

RCL is effective in thwarting all conflict-based side-channel attacks when the VA to PA translation is not exposed and the VAs of security-critical data are not leaked by other means. The strong protection of RCL comes from three reasons:

- **RCL significantly increases the difficulties in creating eviction sets.** In normal conflict-based attacks, attackers utilize the direct mapping revealed in Equation 1 to deterministically construct eviction sets containing congruent cache lines. Without knowing the PA of her own data and the content of the random table, attackers are incapable of constructing eviction sets in the usual way. The only available to create eviction sets is the automatic search algorithm [12] as described in Section 3.C.

- **RCL significantly reduces the amount of information leaked by cache eviction.** Even eviction sets are created using the automatic search algorithm, as it will be revealed in Section 6.C, RCL introduces significant amount of noises when they are applied to LLC.

- **Ultimately, RCL removes the spatial correlation between an attacker and her victim through a cache.** Even if eviction sets are created by a yet unknown means and there is a yet unknown way to reduce the noise introduced by RCL, an attacker still needs to infer useful information using a certain cache set as a medium. Since the cache layout is randomized, without disclosing the PA and deciphering the random table, there is no deterministic way to spatially correlate the data of any two pages.

For the conflict-based attacks targeting L1 caches (sub-type A-1), if an attacker can successfully acquire a physically and virtually consecutive memory space, such as a larger page, larger than \( w \cdot 2^{k+s+6} \) bytes, the attacker is able to deterministically create eviction sets as any
cache lines sharing the same PA\[k + s + 5 : 6\] are still mapped to the same cache set. Figure 2a shows a bitmap representing the cache lines inside a larger page (2 MiB) mapping to the same set in a RCL enabled cache \((s = 6, k = 6)\), where the x axis denotes pages and the y axis denotes the cache lines in each page. The distribution of cache lines is randomized only in the 64 pages space and then duplicated 8 times in the larger page, which is enough to form an eviction set for a 4-way cache. However, without knowing the exact PA and the content of the random table, the attacker cannot know which cache set is evicted. No existing attacks (targeting L1 caches) works in this way. Nevertheless, if we are determined to eliminate this threat, an implementation can increase \(k\) to make \(w \cdot 2^{k+s+6}\) bytes larger than a larger page (at the cost of a larger random table). As shown in Figure 2b, the distribution of cache lines is totally randomized when \(k\) is increased to 9. Alternatively, the system can disable the larger page support for user applications [21]. Flushing the L1 caches during process switching [6,7] is another way to effectively thwart any cache-base side-channel attacks targeting L1 caches.

For the conflict-based attack targeting LLC (sub-type C-1), since the number of cache sets are significantly larger than that in L1 caches and the cache is addressed by PAs rather than VAs, creating eviction sets becomes even more difficult than doing it in L1 caches. RCL breaks the direct mapping from addresses to cache sets. All existing means to deterministically create cache sets cease to work. For advanced attacks that create eviction sets using an automatic search algorithm (sub-type C-1), RCL also provides a strong protection. Detailed analysis will be provided later in Section 6.C related to sub-type C-1.

**B: Flush-based side-channel attacks**

The flush and prefetch operations explicitly evict or load a cache line in the cache system using VAs. These are legal cache management operations which will succeed no matter where the cache line is stored. As a result, randomizing the cache layout has no effect. RCL cannot stop flush-based side-channel attacks. Fortunately, flush-based attacks can be effectively resolved by constraining the flush and prefetch instructions and removed the potential vulnerable memory sharing mechanisms as described in Section 4.

**C: Automatic side-channel attacks**

For conflict-based attacks targeting LLC, especially those attacking the post Sandy Bridge Intel processors which have LLC sliced and addressed using the complex addressing scheme [30], attackers rely on a blind but optimized search algorithm to create eviction sets for LLC (sub-type C-1). Most automatic search algorithms are derived from Liu’s algorithm [12]. The input is a large set of cache lines containing enough lines to evict a cache set. By iteratively trimming irrelevant cache lines, the search algorithm produces a comparatively pure eviction set targeting LLC. This search algorithm is extremely robust. It is ignorant to the complex addressing scheme, appears to work in inclusive or non-inclusive cache hierarchies, and even shows resistance to RCL.

Figure 2b shows an eviction set created in a two-level inclusive cache hierarchy. Utilizing this eviction set, the attacker is able to prime a LLC cache set. Thanks to the direct mapping from addresses to cache sets and the inclusive cache hierarchy, evicting a set in LLC effectively evicts a large portion of a cache set inside the victim’s L1 cache.

Now let us apply RCL to LLC. RCL may fail to prevent Liu’s algorithm from producing an eviction set. Assuming this eviction set is pure, as shown in Figure 3a, loading lines in this eviction set does evict a cache set in LLC but they are distributed across arbitrary cache sets in the attacker’s L1 cache.

Although RCL cannot prevent the creation of eviction sets, it significantly reduces the usefulness of these eviction sets. This reduction comes from two reasons: ① The lines of a target cache set in the victim’s L1 cache are scattered across a large number of cache sets in LLC. Evicting a set in LLC most likely purges only one cache line from the target cache set in the victim’s L1 cache. ② It is likely that a set in LLC contains lines belonging to multiple cache sets in the victim’s L1 cache. Evicting the victim’s cache lines through priming LLC is significantly noisy. For these two reasons, most conflict-based side-channel attacks relying on the automatic creation of eviction sets stop to work.

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2In Figure 3a, the whole set in the victim’s L1 cache is evicted for simplicity.
Some advanced attacks might combine cache side-channels with other side-channels to reverse part of the PA (sub-type C-2). However, these attacks either still rely on the direct mapping from address to cache sets in LLC [14,30], or requiring precisely evict two cache lines from LLC [31]. The former no longer works if RCL is applied to LLC. For the latter, a randomized cache replacement policy would significantly reduce the required precision. Alternatively, oblivious RAM [44] would provide a strong protection against such attacks. Other sophisticated attacks might use cache set collision to locate the security-critical information stored in the victim’s L1 cache. However, the actual information leak relies on the correlation between cache indexes and page offset [13]. Such correlation is removed by RCL. In summary, RCL is effective in thwarting the automatic side-channel attacks, which is so far the most sophisticated cache-based side-channel attacks.

D: Page table side-channel attacks

RCL easily thwart any attacks trying to bypass the user ASLR protection (sub-type D-1). These attacks run in restricted environment (normally sandboxed) where an attacker cannot obtain the VA of her own variable [13]. The attacker launches accurate cache evictions to locate the cached PTEs related to a VA and then infer part of the VA using the cache indexes of these PTEs. When RCL is applied, the correlation between the cache indexes of PTEs and the VA is safely removed.

For attacks trying to bypass the kernel ASLR protection (sub-type D-2), RCL can thwart the attacks accurately evicting PTEs from the L1-D cache. However, RCL cannot stop the attacks that flush/prefetch the PTEs in the L1-D cache [19] or the attacks exploiting the caches inside the memory management unit (MMU) [32] (translation and page table caches [55]). Nevertheless, the thorough solution is adopt KPTI to separate the kernel page table from user’s [46].

E: Privileged side-channel attacks

For the attacks disguising themselves in OSs, the translation from VA to PA is already exposed and attackers may have explicit control over the cache content (flush or prefetch). Obscuring the cache layout, such as RCL, provides little protection. A TEE armed with strong resource isolation [44] provides better protection.

7. IMPLEMENTATION

This section demonstrates the implementations of RCL in the open-source BOOM system-on-chip (SoC) [56,57]. The BOOM processor is an open-source 6-stage out-of-order execution superscalar processor running the 64-bit RISC-V ISA [58]. Every BOOM processor has a pair of private L1-D and L1-I caches while all processors share a unified L2 cache (LLC) with coherence support. We choose this open-source BOOM SoC because it allows us to implement and evaluate RCL an actual and Linux-ready SoC.

7.1 RCL in L1 caches

Figure 4 depicts the implementation of a L1 cache in the BOOM processor. It is pipelined and serves a memory read in two cycles if the requested data (instruction) is cached. To reduce the cache access latency, inquiry to the TLB and accessing the cache array proceed in parallel within the same clock cycle.

To implement RCL in such a cache, the cache array is indexed by CI_R as described in Equation 2 which is the original s-bit CI XORed with an s-bit hash key (hkey) calculated from a part of the PA:

$$hkey = RT( PA[k+s+5:s+6])$$

This requires the PA to be translated before accessing the cache array. As shown in Figure 5, the TLB inquiry is thus made to operate one cycle before accessing the cache array. This serialization increases the cache access latency by one cycle. Section 8.2 will analyze this impact in details.

The random table contains $$2^k$$ true random numbers, each of which is s bits wide. The hkey is an entry read from the random table using a k-bit index extracted from the PA (PA[k+s+5:s+6]). The implementation of the random table is cache depended. In L1 caches, it is normally implemented in registers to reduce the table access latency. The size of the random table in a small L1 cache is limited; therefore, implementing the table using registers (which is more area demanding than SRAMs) does not incur significant area overhead. For other levels of caches, random tables are implemented in SRAMs for area efficiency.

7.2 A speculative L1-D cache

As mentioned in Section 7.1, the serialization of TLB and array access introduces an extra cycle for every cache access, which can incur a noticeable performance penalty. To avoid this extra cycle, a cache can speculate a hash key (hkey’) using VA, as depicted in Figure 6.

The key component is the prediction table. It is a small content addressable register file storing the hash keys of previously visited virtual pages. Assuming the data access pattern present strong spatial locality, most
cache access are within a small number of pages and would hit in the prediction table. Also since the table is small, it would not make the path critical in timing.

If a VA is missed in the prediction table, such as when a new page is visited or a new page table is used due to context switch, the speculated hash key would be wrong. To detect such misprediction, hkey’ is registered and compared with the correct hash key (hkey) in the next cycle. If hkey’ ≠ hkey, denoting the wrong cache set is accessed in the previous cycle, the produced cache data is discarded, the correct hash key is fed back to update in the prediction table (by setting the update flag), and the corresponding cache access is replayed (by setting the replay flag), which incurs a penalty of two cycles in minimum.

### 7.3 A speculative L1-I cache

In the L1-D cache, the target VA comes from a register inside the BOOM load store unit. Adding the prediction table does not make the path critical in timing. However, the target VA in the L1-I cache might come from the fully-associative branch target buffer (BTB). The path is already tight in timing. To avoid prolonging the clock period, the implementation of RCL in the L1-I cache can introduce further speculation.

Figure 7 reveals the internal structure of the speculative L1-I cache. Depending on the sources of requests, the target VA is separated into the predicted VA (\(VA_{prd}\), including the VA generated by the BTB) and the requested VA (\(VA_{req}\), when the predicted VA is wrong or the processor pipeline is redirected). The timing for the paths though \(VA_{prd}\) is much tighter than those through \(VA_{req}\). When \(VA_{req}\) is chosen as the target VA (denoted by the positive request flag), the prediction table is used to generate the speculated hash key (\(hkey_{RT}\)) in the same manner as in the speculative L1-D cache.

When the predicted VA (\(VA_{prd}\)) is chosen, the instruction cache always predicts that the current instruction comes from the same page with the previous instruction; therefore, the hash key of the previous cycle (\(hkey_{RT}\) generated from the random table by the next pipeline stage) is directly used as the speculated hash key (\(hkey’_{RT}\)). The latency incurred by the prediction table is thus avoided. If this simplified speculation is wrong and \(VA_{prd}\) indeed crosses the page boundary, the hash key check in the next cycle would fail as \(hkey’_{RT} ≠ hkey\). \(VA_{prd}\) is then thrown into the replay queue and the instruction fetch is replayed using the requested VA \(VA_{req}\). Since the failure of hash key check triggers the update in the prediction table, the replay is guaranteed with a correct speculation using \(hkey’_{RT}\).

We believe the simplified speculation on \(VA_{prd}\) is correct most of the time. The access pattern for instructions is mostly linear. The instruction flow thus crosses the page boundary for around a thousand instructions. For branches, BTB is usually accurate only for direct branches while performs poorly for indirect ones. Direct branches are normally used for control flows inside small code segments, such as functions. The probability of crossing the page boundary is also low.

### 7.4 RCL in LLC

The cache accesses to LLC are normally treated as simultaneous transactions and handled by multiple trackers in parallel. The internal architecture of the L2 (LLC) cache in the BOOM processor is depicted in Figure 8. According to Equation 3, a random table is added as a shared resource to all trackers and the writeback unit. Since LLC can tolerate longer access latency than L1 caches, the random table is implemented in SRAM rather than registers for area efficiency. The tag and data arrays are indexed by the randomized cache index \(CI_R\). The state machines inside all trackers and the writeback unit are therefore modified according to Equation 3. An arbiter is added to serialize simultaneous accesses to the SRAM-based random table.

### 7.5 Initialize random tables

Random tables are initialized during power-up process or by request. Individual caches need to guaran-
processors might choose to apply RCL against cross-process attacks targeting L1 caches, some conflict-based attacks. Considering flushing L1 caches RCL to LLC alone is effective to thwart most cross-core of eviction sets in Section 6.C (Figure 3b), applying Recalling the analysis related to the automatic creation of benchmark cases fail to compile or crash in execution. Linux support are in constant development, a number benchmark suite [63]. Since the RISC-V ISA and its implementation, simple pseudo-random number generators are used to initialize the randomization tables.

8. EVALUATION

8.1 Experiment Platforms

Four different designs of BOOM SoCs have been implemented and evaluated with various configurations:

- **Baseline**: The original BOOM SoC.
- **RCL-N**: All caches are implemented with the non-speculative version of RCL.
- **RCL-S**: All caches are enabled with RCL but the speculative RCL is implemented in L1 caches.
- **RCL-L2**: RCL is enabled only in L2 (LLC).

Recalling the analysis related to the automatic creation of eviction sets in Section 6.C (Figure 3b), applying RCL to LLC alone is effective to thwart most cross-core conflict-based attacks. Considering flushing L1 caches during process switching [67], is a strong protection against cross-process attacks targeting L1 caches, some processors might choose to apply RCL only to LLC as in RCL-L2. The default parameters shared by all BOOM SoCs are illustrated in Table 4.

All SoCs are tested on a Xilinx ZC706 FPGA [62]. We have managed to run a subset of the SPEC 2006 benchmark suite [63]. Since the RISC-V ISA and its Linux support are in constant development, a number of benchmark cases fail to compile or crash in execution.

These failed cases are not caused by RCL because all benchmark cases that successfully run on the original BOOM SoC also run on the ones supporting RCL.

To evaluate the area overhead of supporting RCL in ASICs, all processor designs has been implemented using a standard cell library and a memory compiler in a 40 nm technology. The Synopsys Design Compiler topological synthesis flow is used to provide accurate post-synthesis area and frequency figures. All processors are constrained at 750 MHz for area results while they are pushed to their limits for frequency results.

8.2 Running the BOOM SoCs on FPGAs

Figure 9a reveals the prolonged execution time in supporting RCL in BOOM SOCs. The average execution time increases by 4.4%, 2.3% and 2.0% for RCL-N, RCL-S and RCL-L2 respectively. The execution time increases for two reasons: The L1 cache access latency increases due to the extra cycle in RCL-N or misprediction in RCL-S. The L2 cache access latency increases because extra cycles are needed to access the randomization table. In all benchmark cases, RCL-N incurs the longest execution time as it suffers both latency overheads. Utilizing speculation significantly reduces the latency overhead in L1 caches. The speculative RCL-S present the similar execution time overhead with the L2 only implementation (RCL-L2). In all benchmark cases, the execution time is prolonged for less than 3.5% for both RCL-S and RCL-L2.

Note that not all cases suffer from prolonged execution time. For certain combinations, such as ‘456.hmmer’ (with RCL-N) and ‘473.astar’ (with RCL-S), the regular access pattern of an application might cause execution time increases because extra cycles are needed to access the randomization table. In all benchmark cases, RCL-N incurs the longest execution time as it suffers both latency overheads. Utilizing speculation significantly reduces the latency overhead in L1 caches. The speculative RCL-S present the similar execution time overhead with the L2 only implementation (RCL-L2). In all benchmark cases, the execution time is prolonged for less than 3.5% for both RCL-S and RCL-L2.

Table 4: Parameters of the BOOM SoC

| Description              | Default value |
|--------------------------|---------------|
| ISA                      | 64-bit RISC-V |
| Pipeline stages          | 6             |
| Issue width              | 4             |
| Commit width             | 2             |
| TLB entries              | 8             |
| Reorder buffer entries   | 48            |
| L1 cache (I & D)         | 32KB (8-way)  |
| L2 cache                 | 1MB (16-way)  |
| Clock frequency (FPGA)   | 50MHz         |
| Clock frequency (ASIC)   | 750MHz        |

Figure 9a reveals the miss per kilo instructions (MPKI) collected from all cache levels. According to the results, there is no significant change in the MPKI on both cache levels with or without RCL except for ‘473.astar’ where supporting RCL actually reduces the MPKI in L1-D.
by 16%. To be specific, the average MPKI in L1-I is increased by 1.6% for RCL-N and decreased by 1.7% for RCL-S. The average MPKI in L1-D is reduced by 4.9% and 4.3% for RCL-N and RCL-S respectively. The change of the average MPKI in all other combinations are less than 0.1%.

To analyze the efficiency of the speculation, Figure 10 reveals the impact of the number of entries inside the prediction table (PT) on the execution time and cache misses. The number of PT entries $e$ increases from 4 to 8, which is the maximum number of entries without affecting the frequency. As shown in Figure 10a, most benchmark cases are sensitive to the number of PT entries except for ‘462.libquantum’. ‘456.hmmer’ is the most sensitive case where reducing $e$ to 4 (RCL-S,e=4) leads to >20% execution time overhead compared with (RCL-S,e=8). Nevertheless, the execution time overhead for all benchmark cases is reduced to 4.2% if $e \geq 6$. On average, the execution time increases by 8.4%, 4.0% and 2.3% for 4, 6 and 8 PT entries respectively.

Figure 10b shows the MPKIs in PTs, TLBs and the L1 caches. It is obvious that the size of PT has no impact on the MPKIs of TLBs and caches. The extra execution overhead is caused by the misprediction inside PT. This effect becomes more evident when a benchmark case lacks for spatial locality in its data accesses, such as ‘403.gcc’, ‘456.hmmer’ and ‘473.aster’. In these cases, the data TLB has a higher MPKI than the data cache itself. For the case of ‘456.hmmer’, which shows the most sensitivity to speculation, although the instruction shows a strong spatial locality, the pattern of heavily code-reuse leads to frequency cross-page branches, which leads to significant amount of misprediction in the simplified speculation for the $VA_{prd}$ produced by BTB (as shown in Figure 7).

### 8.3 Hardware Overhead in ASICs

To provide a relatively accurate estimation on supporting RCL in ASIC implementations, all configurations of the BOOM SoCs have been synthesized using the SMIC 40 nm technology. The area results of all levels of caches with different cache configurations are listed in Table 5 where the area results of the caches supporting RCL are normalized. In all caches, the parameter $k$ is set to $s$ by default, leading to a random table of $2^s$ entries. As described in Section 6A, a cache can increase the random table $(w \cdot 2^{k+s+6} > 2^{21})$ to prevent an attacker from deterministically create eviction sets using a larger page. For each L1 configuration, the area overhead with an enlarged random table is also evaluated (with a larger $k$). The L2 cache is normally large enough to cover a larger page.
The register-implemented random table with the default \( k = 2 \cdot s \) incurs a marginal area overhead of around 0.2% for all caches. The smallest cache (4-way 64-set) suffers the largest area increase of only 2.0%. Even with an enlarged random table, the area overhead is less than 5% for all caches. The speculative circuit in RCL-S introduces a negligible area overhead of around 0.5% for all caches. In L2 caches, the SRAM-implemented random table shows a good scalability with the increasing number of sets. The smallest L2 cache (8-way 512-set) has the maximal area overhead of only 3.4%.

As for the impact on clock frequency, L1 caches runs at the same frequency with the processor core. L1-I has a tighter timing than L1-D. The baseline BOOM SoC can run at 843 MHz. RCL-N reduces the frequency to 756 MHz introducing a drop of 10.3%. To reduce this effect, the speculative RCL-S runs at 846 MHz, the same speed with the baseline. Figure 11a reveal the clock frequencies of L1 caches with different random tables in a RCL-S BOOM SoC. Thanks to the speculation circuit, the random table is moved of the critical path. The size of the random table has no significant impact on clock frequency. It is also clear that the L1-I has a much tighter timing compared with L1-D. For RCL-L2, which implements RCL only in the L2 cache, Figure 11b reveals the frequency drop with the enlarged cache and random table. Supporting RCL in L2 incur a negligible additional drop in frequency from 0.11% for the 512-set cache to 0.42% for the 4096-set cache.

### Table 5: Cache Area

| Size (KI B) | Config \((w, s, k)\) | Baseline | RCL-N | RCL-S |
|------------|-------------------|---------|-------|-------|
| L1-I       | (4, 6, 6)         | 0.260   | 1.7   | 2.0   |
|            | (4, 6, 8)         |         | 4.6   | 4.9   |
|            | (8, 5, 5)         | 0.377   | 0.7   | 0.9   |
|            | (8, 5, 9)         |         | 4.5   | 4.7   |
| L1-D       | (8, 6, 6)         | 0.458   | 0.9   | 1.1   |
|            | (8, 6, 8)         |         | 2.6   | 2.8   |
| L2         | (8, 9, 9)         | 0.948   | 3.4   |       |
|            | (16, 8, 8)        | 1.019   | 2.6   |       |
| L2         | (8, 10, 10)       | 1.801   | 2.2   |       |
|            | (16, 9, 9)        | 1.860   | 1.7   |       |
|            | (8, 11, 11)       | 3.550   | 1.3   |       |
|            | (16, 10, 10)      | 3.566   | 1.1   |       |
| L2         | (8, 12, 12)       | 7.032   | 1.0   |       |
|            | (16, 11, 12)      | 7.063   | 0.6   |       |

9. RELATED WORK

As described in Section 4, RCL is not the first defense trying to randomize the cache layout. RPcache [38] and the later NewCache [39] are the first to randomize the mapping from VAs to cache sets. The randomized cache index in the PRcache can be described as \( f(VA[s + 5 : 6]) \) where \( f() \) is a random function similar to the random table in RCL. This defense can effectively thwart conflict-based attacks infer information from the L1 cache indexes. However, it does not alter the fact that congruent cache lines (sharing \( VA[s + 5 : 6] \)) are still mapped to the same cache set. The cache layout in L2/LLC is not randomized. These two drawbacks make PRcache ineffective in front of the advanced side-channel attacks typed C and D. Although later the NewCache enhanced the randomization by a ReMapping table [39], the aforementioned issues remains. Both PRcache and NewCache require software to set security flags on cache lines, which unnecessarily introduces modifications in software. Introducing PA into the cache layout randomization, RCL is the first pure hardware defense that deliberately avoids storing congruent cache lines in the same cache set, applicable in all cache levels and require no software involvement.

Any cache related technologies that introduce randomness into the cache layout can potentially work with RCL and strengthen its defense. Introducing randomness into the hardware prefetcher [42] or allow cache lines to decay at random intervals [40] provide extra defense against the flush-based attacks. If the secrecy-critical data can be identified by software, such as the lookup tables normally used in cryptographic algorithms, randomizing the fetched cache line [41] or ask software to explicitly randomize the security-critical data before storing them to memory [53] are effective as well. The complex addressing scheme utilized in modern Intel processors [30] can be enhanced to provide run-time slice mapping. The skewed cache [64], which was proposed to improve cache associativity, and the compressed cache [65] can be applied along with RCL to introduce further randomness into the cache layout.

Combining RCL with other defenses provides further protection. All the defenses described in Table 3 naturally
rally work along with RCL, such as constant time programming [47, 97], flushing of local caches during process switching [40, 46] KPTI and TEE [43, 44]. For cache partitioning, RCL can work with all defenses using way partitions [6, 36]. However, cache partitioning based on page color [41] and explicit cache management [18, 52] may no longer work because RCL has randomized the cache layout and cache lines with different page colors can be stored in the same cache set.

10. CONCLUSION

Based on a systematic review of the common cache-based side-channel attacks and the existing defenses, automatic side-channel attacks and bypassing the user ASLR have been identified as largely undefended in current computer systems. A pure hardware defense against a wide range of conflict-based side-channel attacks, namely Remapped Cache Layout (RCL), is proposed. RCL deliberately randomizes the mapping from addresses to cache sets. It prevents attackers from accurately infer the location of her data in caches or using a cache set to infer her victim’s data. To our best knowledge, RCL is the first defense to thwart the automatic side-channel attacks and the attacks of bypassing the user ASLR. It is also a pure hardware defense which requires no software involvement. RCL has been implemented in all levels of caches into the BOOM SoC. A speculative cache structure is proposed to reduce the cache access latency in RCL enabled L1 caches. Collected from running the SPEC 2006 benchmark on the RCL enabled BOOM in an FPGA, the detailed evaluation results show that RCL incurs only small costs in area, frequency and execution time.

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