**Voltage Differencing Buffered Amplifier (VDBA) Based Grounded Meminductor Emulator**

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**ABSTRACT** - A new meminductor emulator using a capacitor, a memristor and a voltage differencing buffered amplifier (VDBA) is proposed in this paper. This reported realization of meminductor is very simple than proposed in literature as it needs only 1 active block. The proposed emulator has been found suitable for low frequency operations with electrical tunability, and multiplier free topology. The characteristics of the proposed emulator have been verified for a frequency range of 1.8Hz to 4.9Hz using the LTspice simulation tool with 180nm CMOS technology parameters. Pinched hysteresis loops observed in flux versus current plane verifies its meminductive behavior. Moreover, the non-volatility test of the proposed emulator proves its memory behavior. The pinched hysteresis loops obtained through simulations show that the lobe area reduces with increase in frequency.

**Keywords:** VDBA; meminductor; Pinched hysteresis loop; memristor.

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1. **INTRODUCTION**

Earlier there were only three known fundamental circuit elements: inductors, resistors, and capacitors. L. Chua [25] in 1971, proposed a fourth fundamental circuit element named memristor [25]. Its memristive concepts were studied in detail in 1976. However, this theory was not of much use until its first physical realization was done using TiO₂ in 2008 by HP labs [24]. After the realization, this idea of memristor has been extended to capacitors and inductors giving the concept of memcapacitor and meminductor [21]. All these elements: memcapacitor, meminductor, and memristor have memory retaining capabilities and hence their performances are affected by past values [1]. However, these devices’ elements are not available in commercial form, so researchers discovered their alternative in the form of emulators [20]. The memcapacitor and meminductor emulators were created with the help of resistors, capacitors, operational amplifiers (op-amps), operational transconductance amplifiers (OTAs), and memristors. Various meminductor emulator realizations have been proposed in the literature. In [22], a meminductor emulator realization using a second-generation current conveyor (CCII), op-amp, floating memristor emulator, multiplier, one capacitor, and three resistors has been proposed. In the emulator design proposed in [9], a generalized emulator has been designed using two AD844s, a memristor, a resistor, and a capacitor that can imitate the behavior of a meminductor and a memcapacitor. Three trans-impedance operational amplifiers, a floating memristor, buffers, resistors, and capacitors were used to create a universal mutator [10]. As evidenced from the literature review, the designing of meminductor emulators can be broadly categorized into two categories. The first approach mainly depends on creating meminductor emulators by transforming a memristor emulator using a mutator circuit. This is the primary strategy backed by the majority of meminductor emulator circuits published in the literature. The downside of this technique is that meminductor emulator characteristics are inextricably linked to memristor emulator features. The memristor-less architecture of the meminductor emulator is the second approach. The circuits of the meminductor emulators that are designed using the second method are complex because of an excessive number of active/passive components and analog multiplier. The objective of this work has been to design a meminductor emulator with a simple structure. The work in this paper has been carried out with the aim of designing a robust meminductor emulator circuit with fewer active and passive components which are free from the requirement of a multiplier. The proposed meminductor emulator has been designed using a VDBA, a memristor, and a capacitor. The paper is divided in 6 Sections including the introduction section. The properties of VDBA have been discussed in Section 2. The methodology of the proposed meminductor emulator along with its mathematical analysis is given in Section 3. LTspice simulation results of the proposed emulator are presented in Section 4. A comparison with state-of-the-art meminductor emulators has been given in Section 5. This paper’s conclusion is given in the Section 6.

2. **CHARACTERISTICS OF VDBA**

In Figure 2 of MOS-based VDBA, it’s a combination of voltage to current converter (or transconductance amplifier) and the voltage follower.
In Figure 1 VDBA block diagram depicting various terminals and the corresponding port currents is shown. It has a pair of high-impedance input voltage terminals (V_N and V_P), a low-impedance output voltage terminal (V_W), and a high-impedance output current terminal (I_Z). Matrix equation of VDBA, depicting its terminal properties is given as:

\[
\begin{bmatrix}
I_P \\
I_N \\
I_Z \\
I_{ZC} \\
V_W
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 \\
0 & 0 & 0 \\
g_m & -g_m & 0 \\
-g_m & g_m & 0 \\
0 & 0 & 1
\end{bmatrix}
\begin{bmatrix}
V_p \\
V_N \\
V_Z
\end{bmatrix}
\]  

where \( g_m \) denotes the transconductance gain of VDBA and is given as:

\[
g_m = \frac{b_1 b_9}{\sqrt{2}} (V_{B1} - V_{SS} - V_{th})
\]

here, \( b_1 \) and \( b_9 \) are transconductance parameters of MOSFET M1 and M9 respectively, \( V_{B1} \) is DC biasing voltage applied at the gate terminal of MOSFET M9 and \( V_{th} \) is the threshold voltage of NMOS. The MOS-based circuit of voltage differencing buffered amplifier (VDBA) in Figure 2 is an alternative active building block that is slew-free and handles voltage signals. The VDBA, as its name implies, employs a voltage differencing input stage and generates a current output that is equal to the multiplication of the transconductance gain and differential input voltage. The fact that the transconductance has a biased current dependent allows for electrical circuit parameter tweaking [9]. As a result, the circuit design is simpler, with fewer passive components. It also has a buffered voltage output, resulting in architectures that are easily cascadable [10]. Furthermore, the VDBA's ability to output both voltage and current adds to the design freedom [11]. As a result, for the analog application, VDBA has emerged as a viable option.

### 3. METHODOLOGY AND PROPOSED MEMINDUCTOR EMULATOR

The complete circuit of VDBA based proposed meminductor emulator is shown in Figure 3. It consists of a memristor \( M_R \) connected between nodes N and W of VDBA. A floating capacitor is connected between nodes Z and ZC. The input voltage is applied at node N. From Figure 3 it can be analyzed that the circuit needs only 1 active block (VDBA), 1 memristor, and 1 capacitor for its realization. In this circuit, none of the terminals of VDBA is left open, giving low noise architecture. Furthermore, one of the differential input terminals of VDBA (p-terminal) is grounded leading to the robust configuration preferred by circuit designers.

Meminductance \( (M_L) \) of a meminductor is characterized by the following relation [25]:

\[
\Phi(t) = M_L I(t)
\]

A meminductor is characterized by pinched hysteresis loop observed in \( \Phi(t) \) vs. \( I(t) \) plane. The flux \( \Phi(t) \) of the meminductor is mathematically defined as:

\[
p(t) = \int_{-\infty}^{t} \Phi(t) \, dt
\]

\[
q(t) = \int_{-\infty}^{t} I(t) \, dt
\]

For a meminductor understanding, variables \( p \) and \( q \) are used and \( q \) is the time integral of current \( (I(t)) \) and \( p \) is the time integral of flux \( \Phi(t) \).

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The proposed meminductor emulator circuit is designed using the LTspice tool. A supply voltage of ±1.5V is provided to the CMOS-based VDBA shown in Figure 2. For proper operation, a bias voltage of 100mV is connected to \( V_{B1} \) and \( V_{B2} \). The aspect ratios of MOSFETs used in the design of CMOS-based VDBA are summarized in Table 1.

Table 1: Aspect ratios of MOSFETs used in the design of CMOS based VDBA

| MOSFET | W (µm) / L (µm) |
|--------|-----------------|
| M1, M2, M3, M4, M9, M10, M11, M15, M16 | 7/0.35 |
| M5, M6, M17, M19 | 21/0.7 |
| M7, M8, M18, M20 | 7/0.7 |
| M12, M13, M14 | 14/0.35 |

The results of the suggested meminductor emulator’s transient analysis are shown in Figure 4. A signal of 200mV amplitude, capacitor \( C_1 \) in the proposed meminductor has shown a linear increase of meminductance (\( M_L \)) value till the particular value. In the non-volatility behavior shown in Figure 5 it can be observed that the meminductance retains its value when the input pulse goes off and with the next pulse get ON its value starts from the previously stored meminductance (\( M_L \)) value. This behavior proves the memory retention characteristic of the proposed emulator.

Figure 4: Transient response of meminductor emulator with a sinusoidal voltage signal of 200mV amplitude and 2Hz frequency

Figure 5: Non-volatility behavior observed with 20mV pulse signal of 5ms period having ON time of 1ms
The simulation result observed in $\Phi(t) \text{ vs. } I(t)$ plane is shown in Figure 6. Pinched hysteresis loop (PHL) with zero-crossing observed in the PHL curve between $\Phi(t) \text{ vs. } I(t)$ shown in Figure 6 confirms the meminductive behavior of the proposed circuit. Figure 6 has been plotted for a sinusoidal input signal of 4.7Hz frequency and 850mV amplitude.

PHL curves observed at different frequencies of 4.3Hz, 4.5Hz, 4.7Hz, and 4.9Hz are shown in PHL between $\Phi(t) \text{ vs. } I(t)$ plane at Figure 7. Similar curves for frequencies 1.8Hz, 2Hz, and 2.2Hz are plotted in Figure 8. All these curves confirm that the increase in frequency area inside the lobes reduces.

From comparison with various meminductors reported in literature Table 2, the following points can be inferred for the proposed meminductor emulator:
1. Meminductor emulators reported in [6, 15, 20, 21, 24] use multiple active components, while the proposed meminductor emulator is implemented using only one VDBA hence it reduces the complexity of the proposed circuit.
2. The proposed meminductor emulator has no resistance, but the meminductor emulator is described in [6, 7, 8, 12,
6. CONCLUSION

A voltage differencing buffered amplifier, a memristor, and a capacitor have been used to create the suggested meminductor emulator. The suggested meminductor emulator operates for a frequency range from 1.8Hz to 4.9Hz. The non-volatility test confirms its memory behavior, and the pinned hysteresis loop proves its meminductive nature. PHL curves are observed to have a smaller area with an increase in frequency. The suggested emulator offers the advantages of simple circuitry, low voltage operation electrical tunability, and multiplier-free topology. It possesses a robust and less-noise structure, as one of its differential input terminals is connected to the ground and none of the VDBA terminals is left open. It is a good choice for circuit designers working in low-frequency zone. The VDBA can be realized using commercially available IC OPA860 and make the suggested meminductor economically viable.

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