TRINITY: Coordinated Performance, Energy and Temperature Management in 3D Processor-Memory Stacks

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ABSTRACT

The consistent demand for better performance has lead to innovations at hardware and microarchitectural levels. 3D stacking of memory and logic dies delivers an order of magnitude improvement in available memory bandwidth. The price paid however is, tight thermal constraints.

In this paper, we study the complex multiphysics interactions between performance, energy and temperature. Using a cache coherent multicore processor cycle level simulator coupled with power and thermal estimation tools, we investigate the interactions between (a) thermal behaviors (b) compute and memory microarchitecture and (c) application workloads. The key insights from this exploration reveal the need to manage performance, energy and temperature in a coordinated fashion. Furthermore, we identify the concept of “effective heat capacity” i.e. the heat generated beyond which no further gains in performance is observed with increases in voltage-frequency of the compute logic. Subsequently, a real-time, numerical optimization based, application agnostic controller (TRINITY) is developed which intelligently manages the three parameters of interest. We observe up to 30% improvement in Energy Delay\textsuperscript{2} Product and up to 8 Kelvin lower core temperatures as compared to fixed frequencies. Compared to the ondemand Linux CPU DVFS governor, for similar energy efficiency, TRINITY keeps the cores cooler by 6 Kelvin which increases the lifetime reliability by up to 59%.

1. INTRODUCTION

The performance of data intensive computing systems that process terabytes of data is increasingly limited by data movement and corresponding energy overheads. 3D packaging technologies enabled by advances such as Through-Silicon-Via (TSV) technology\textsuperscript{1}, has led to stacking of silicon dies thereby enabling the integration of memory and logic in a small footprint with significant reductions in data movement latency and energy. Further, the package provides an order of magnitude increase in memory bandwidth. For example, commercial standards like DDR3-1333\textsuperscript{3}, DDR4-2667\textsuperscript{3}, HBM2\textsuperscript{4} and HMC2\textsuperscript{5} realize 10.66 GB/s, 21.34 GB/s, 256 GB/s and 320 GB/s, respectively. To effectively exploit the high bandwidth provided by 3D die stacked DRAM, multiple efforts have explored moving compute logic inside the package as part of the die stack revisiting the early efforts at architecting Processing-In-Memory (PIM) designs\textsuperscript{6,7,8,9,10,11,12}. The compute logic layer in the 3D stack can range from simple atomic operations to multiple Out-of-Order (OoO) cores to general purpose low power GPUs. However, stacking memory and logic dies in this manner exacerbates thermal effects which, if left unchecked will preclude any performance gains from co-locating compute and memory. In particular, the exponential relationship between temperature and leakage current diminishes the performance that can be achieved for the heat capacity of the package thereby limiting the ability to exploit the order of magnitude increase in available memory bandwidth\textsuperscript{13,14}.

There is a rich body of work on managing thermal effects in processors. Software-based efforts\textsuperscript{15,16,17,18,19} typically seek to redistribute heat to avoid peak temperature violations. Hardware based efforts employ dynamic voltage frequency scaling (DVFS) to manage the thermal fields\textsuperscript{20,21,22}. Detailed thermal modeling using software packages such as HotSpot\textsuperscript{23} and 3D-ICE\textsuperscript{24} enables the study of
microarchitectural effects on temperature. Although bulk of the work has been pursued for 2D packages, the understanding is still relevant to 3D packages. For example, researchers have explored the thermal coupling between cores on the same layer and between cores on different vertically stacked layers [25]. In general these approaches have dealt with temperature as a constraint. We argue that temperature is a resource that has to be managed, like memory or compute cycles. This approach is rooted in a different view of the relationship between performance and heat capacity.

The heat capacity of the package is established based on the thermal design power (TDP) which is set independent of the application characteristics. However, some applications such as sparse matrix computations have components that are memory bound rather than compute bound. Temperature-based approaches to improve the performance of such applications by boosting voltage-frequency in an attempt to utilize the thermal headroom [26], will simply waste power with little or no performance gain and significant reductions in energy efficiency. An example is shown in Figure 1 where energy efficiency (temperature) of a memory bound benchmark decreases (increases) with increasing clock frequency. On the other hand, compute intensive applications such as dense matrix algebra may extract performance benefits from DVFS schemes but can exceed the temperature bounds. Furthermore, thermal coupling between adjacent cores can increase leakage current (and therefore static power) and accelerate temperature rise leading to premature throttling [27] and therefore performance and energy efficiency loss.

Our goal is to ensure that for the amount of heat generated by the compute logic for an application, the maximum performance (throughput) is delivered. Doing so must implicitly improve energy efficiency. A key insight is that applications, and some application phases, simply cannot utilize the package thermal headroom even when operating at the highest voltage-frequency state. We attempt to capture this observation by noting that for a specific application or phase there is an effective heat capacity (EHC) - this is the heat generated beyond which further gains in performance are infeasible with further increases in voltage-frequency of the compute logic. For example, an application may be operating in a memory bound phase and increases in compute logic frequency has little effect on performance but may consume the thermal headroom. Accordingly, we note that the EHC is application-specific and time-varying. Consequently, our goal is to maximize the performance that can be extracted from the time-varying EHC. The solution must be online, adaptive, and robust to modeling errors. The EHC corresponds to a value of temperature which we will refer to as the effective maximum temperature (EMT). Practical implementations will seek to operate at the EMT and minimize thermal coupling induced leakage power.

Therefore, we propose TRINITY, a DVFS controller that implements an on-line optimization technique that continuously balances performance, energy efficiency and thermal behaviors to fully utilize the EHC (See Fig. 1). Each voltage island implements an independently operated TRINITY controller that is (i) based on numerical optimization, (ii) computationally inexpensive to implement, (iii) self-tuning, (iv) distributed (per-core), and (v) application agnostic. The behavior of spatially adjacent controllers is implicitly coupled via temperature. Thus a network of interacting controllers locally seeks to maximize throughput from the locally available EHC and their coordinated actions indirectly makes the most efficient use of the package heat capacity. Our vehicle for exploration and demonstration is a cache-coherent multicore processor integrated as the bottom die in a 3D DRAM stack as shown in the Figure 15. Cores operate on distinct voltage islands and are capable of operating in independent power states each with a TRINITY controller. The controller is designed considering practical implementation challenges such as (i) measurement and actuation delays (ii) computation delays and (iii) hardware limitations such as having a discrete set of voltage-frequency states. In cycle-level simulations of a 16 core architecture, for 10% increase in Energy Delay Product, TRINITY keeps the temperature lower by 6 Kelvin while achieving similar energy efficiency as compared to on-demand Linux CPU governor. An added benefit of the reduced temperature is the increase in lifetime reliability of the 3D stack by up to 59%.

This paper seeks to make the following contributions:

1. The introduction of the concept of effective heat capacity as a thermal resource to be managed. (Section 2)

2. Development of TRINITY, an on-line DVFS controller (i) based on numerical optimization, (ii) computationally inexpensive to implement, (iii) self-tuning, (iv) distributed (per-core), and (v) application agnostic for cooperatively balancing the performance, energy efficiency, and thermal behaviors of applications. (Section 4.2)

3. A comprehensive simulation-based characterization of intra- and inter-die thermal coupling effects demonstrating the need to maximally utilize the effective heat capacity. (Section 5)

2. MOTIVATION

Figure 2: Heat map of the core layer showing reduction in thermal headroom for neighboring cores.

Consider a 3D architecture as described Section 5.1 and illustrated in Figures 15 and 16, where 16 cores are integrated
at the bottom of a 3D DRAM stack. When only one of the cores is executing an application thread while the rest are idle, the resulting thermal gradient from the ‘hot’ core to the neighboring ‘cool’ cores is shown in Figure 2. We note that the program thread executing on a core can increase the temperature of neighboring cores by > 7 Kelvin. Not shown here, is another observation that on migrating this thread from a location next to the package boundary to a location in the center of the core die decreases the temperature by up to 10 Kelvin (these are computed as steady state temperatures). Ideally, we would like the thermal gradients to be zero, performance to be maximum, and the temperature to be the local EMT at every core.

Achieving this goal via temperature regulation techniques are of limited utility. For example, consider the use of a temperature regulator at each core. The objective of the regulator is to maintain a fixed temperature. We ran a graph benchmark and set the target temperature to 340 Kelvin for each core. In Figure 3 we observe that none of the cores can reach the target temperature. For cores which are idle i.e. threads are waiting to be woken up, the controller tries to raise the temperature of the core by increasing the corresponding voltage-frequency but ends up wasting energy through increases in leakage power due the rise in temperature and no improvement in performance of the core. Temperature regulation in this form is therefore inefficient in 3D stacks because, (1) target tracking temperature (which is the EMT) has to be known apriori, (2) target temperature will be different for different cores and will vary at run-time, and (3) temperature dynamics is a rather slow process (100s of milliseconds) in comparison to application characteristics that can vary rapidly (micro-seconds). Therefore control techniques must be on-line, adaptive, and application agnostic.

The preceding example with temperature regulation illustrates an important point - for certain applications and during certain application phases, package heat capacity cannot be utilized completely. This points to the existence of an effective heat capacity which roughly corresponds to the temperature of the cores beyond which there is little or no increase in performance. We refer to this temperature as the effective maximum temperature. It also represents an energy efficient (ops/joule) operating point. Note that the heat capacity of the entire package is established independent of the specific workload and that effective heat capacity of an application can be time varying. A thread currently in a memory intensive phase with EMT of X Kelvin, may transition into a compute intensive phase where its EMT is Y Kelvin (Y > X). Without profiling an application extensively, tracking the EMT is a challenge. To further emphasize the effect of EHC, we present data from two benchmark applications blackscholes (PARSEC [29]) and tc (GraphBig [30]) in Table 1. The average temperature of the cores in Kelvin and average performance (Million-Instructions-Per-Second (MIPS)) for the two benchmarks is listed for three different fixed frequencies.

Performance and temperature characteristics of both applications vary widely. In order to demonstrate that there is room to improve performance, energy and temperature in these systems, we also compute the Energy Delay Product (ED2P) at the three fixed frequencies. For compute intensive applications like blackscholes, best ED2P is achieved at the highest frequency. But, for memory intensive benchmarks like tc, there is no appreciable improvement in ED2P beyond 1.0GHz. The goal of TRINITY is to dynamically track these behaviors with distributed on-line control.

We observe that it is important to make a distinction between peak temperature and effective heat capacity. The former is a constraint that all thermal management schemes seek to observe. Heat capacity reflects the net amount of heat that can be generated. Observing only the former will not seek to observe. Heat capacity reflects the net amount of heat that can be generated. Observing only the former will not maximize performance for the corresponding amount of heat. Our goal is to extract as much performance as possible from the heat generated by the application. Thread scheduling techniques that seek to redistribute heat can be re-purposed towards this end. In this sense, effective heat capacity is a resource which the proposed on-line distributed controller network is designed to exploit efficiently.

In light of the observations made in the previous paragraphs, we first present a microbenchmark characterization of the 3D stacked architecture in Section 3. We list the key insights which lead us to development of the optimization problem and its solution is described in Section 4. We then proceed to evaluate the proposed controller over a set of benchmark applications in Section 5. Finally, we list relevant works in Section 6 and conclude the paper in Section 7.

3. CHARACTERIZATION

In this section we seek to find answers to the following

Table 1: Table demonstrating variable application heat capacities and room for improving balance between performance, temperature and energy.

| Temp. (K) | Bench. | 0.5GHz | 1.0GHz | 1.5GHz |
|----------|--------|--------|--------|--------|
| blacks.  | 318.18 | 329.68 | 340.93 |
| tc       | 313.91 | 318.93 | 323.85 |
| blacks.  | 12378.3| 23710.7| 33065.6|
| tc       | 2741.3 | 3633.9 | 4026.7 |
| blacks.  | 0.67   | 0.33   | 0.26   |
| tc       | 0.76   | 0.58   | 0.58   |

Figure 3: Temperature Regulation Inefficiency: Except for CORE5 and CORE11, rest of the cores are idle. At 400ms mark CORE11 becomes idle as well.
questions:
(1) What is the thermal impact of a hot core on neighboring cool cores? What are the performance implications for both the hot core and the cool cores?
(2) What is the thermal and performance behavior of a program thread executing at different physical locations on the core layer?
(3) How does memory addressing patterns in the L2 Cache layer affect the temperature of the core layer and vice versa?

We therefore proceed by characterizing temperature and performance of the 3D stack (See Section 5.1). Fig. 5 and 6 under a variety of microbenchmark workloads. Temperature is measured in Kelvin and performance in MIPS. The temperature numbers reported are steady state values. The microbenchmarks are designed such that they (i) exhibit variable ops/byte ratio, (ii) access specific memory locations, and (iii) execute on specific physical cores.

3.1 Nomenclature
To better represent the characterization results, we first describe a naming convention in Figure 4 which is used throughout the characterization section of this paper. All the microbenchmarks are single threaded programs. Most of the results that follow have a single thread running on a single fixed core (source core) accessing data from a single fixed L2 Cache bank (source/remote bank). We make a distinction when two cores are running independent microbenchmark applications as and when required. While a microbenchmark is running on a single core, the rest of the cores are powered up (V_{dd} and CLK are supplied) but idle. The 1-hop and 2-hop neighbors of the source core are termed SC+1 and SC+2, respectively. Similarly, for the L2 Cache banks we have SB+1 and SB+2. In what follows, a “compute intensive benchmark” continuously performs load operations on sequential memory locations whereas a “compute intensive benchmark” repeats the following two steps: (i) load a block of data from memory (ii) perform integer and floating point operations for a fixed number of iterations.

Among the many cases of thermal coupling, we discuss 5 types in detail as shown in Figure 4:

(a) Thermal coupling between adjacent cores.
(b) Thermal coupling between a core and an L2 Cache bank directly on top.
(c) Thermal coupling between an L2 Cache bank and an idle core below it.
(d) Same as (c) but with a non-idle core.
(e) Thermal coupling variation when the computation is moved from the package boundary to the center of the die.

3.2 Thermal Coupling Analysis
Case (a): In Figure 5(a), the temperature of the source core SC, average temperature of its 1-hop neighbors and 2-hop neighbors, SC+1 and SC+2, respectively is plotted for a memory bound microbenchmark at three different clock frequencies with the SC accessing data from SB and RB. Figure 5(c) is similar to Figure 5(b) except that the microbenchmark is compute bound. Out of the 16 possible locations for the SC, accounting for symmetry, three locations viz. Core0, Core2 and Core3 are chosen. The temperature and performance trends for Core0, Core2 and Core3 are plotted in Figures 5(c) and 7, respectively. We note that regardless of whether the benchmark running on SC is memory intensive or compute intensive, although SC+1 is idle, due to thermal coupling, steady state temperature of SC+1 can go as high as 325 Kelvin. Thermal coupling effects are negligible beyond a 2-hop neighborhood concurring with prior work [31] (albeit [31] is for a 2D architecture). The extent of thermal coupling in a 3D architecture however, is more pronounced within the 1-hop neighborhood due to heat shielding from upper layers. The key observation we make is:

Observation 1: A ‘hot’ core reduces the EHC of neighboring ‘cool’ cores by up to 7 Kelvin.

A second more subtle observation to obtained by analyzing the steady state temperature and performance of the SC when accessing SB and RB (See Fig. 5(a) and 5(b)). By addressing a RB, the SC temperature can be reduced by up to 8 Kelvin. This however, comes at the price of 30% reduction in performance. Therefore, Observation 2: Memory address re-mapping has the potential to trade-off performance for reduction in temperature.

Case (e): Carrying forward from Case (a), we repeat the same set of experiments but choose to run the microbenchmark on a SC that is physically located at three specific locations: (1) Corner (Core0) (2) Boundary (Core2) and (3) Center (Core3). Using ‘Corner’ as the reference, we compute the differences in temperature and performance for the other two locations. Specifically, we annotate the differences as follows: Corner - Boundary (C-B) and Corner - Center (C-C). The trend of the data obtained is plotted in Figure 8. The difference between figures 8a, 8b and 8c is only with the memory location addressed, SB, RB and SB+1, respectively.

Temperature difference in Kelvin and performance difference in MIPS are plotted on the y-axis. In general, moving the application thread from the corner to the boundary or center reduces the temperature of the SC between 1 – 10 Kelvin with negligible loss in performance. The greatest difference is seen for the C-C case. Not only does the SC experience reduction in temperature, its neighbors SC+1 too benefit by up to 4 Kelvin due to the relocation. Note however, that this phenomenon does not nullify Case (a). Only the magnitude of thermal coupling is mitigated to a small extent.

Observation 3: Package boundaries become increasingly important in 3D stacked environments. OS level thread scheduling in cooperation with DVFS schemes can lead to better utilization of the EHC.

To completely understand the thermal coupling between the compute and memory layers, we divide this inter-layer thermal coupling into Cases (b), (c) and (d). For Cases (b) and (c) we refer to Figure 9 and for Case (d) we refer to Figure 10. Before we present the analysis, it is essential to note that for the 3D architecture under consideration, in steady state, the core layer always has the highest temperature when compared to upper layers.

Case (b): The heat flow between the SC and the SB is influ-
parameters: performance, energy and temperature to
300
305
310
315
320
325
330
335
0.4
0.6
0.8
1.2
Case (a) Case (b) Case (c) Case (d) Case (e)
Source Core (SC)
Source L2$ Bank (SB)
Remote Core (RC)
Remote L2$ Bank (RB)
Data Access
Thermal Coupling
Idle core
Case (a)
Case (b)
Case (c)
Case (d)
Case (e)
Figure 4: Microbenchmark characterization nomenclature.

Figure 5: Performance and temperature variation when running mem bound and compute bound benchmarks on a source core accessing source and remote cache banks at different core frequencies. SC is Core0.

enced by whether the SB is 'active' or 'idle'. The temperature trends for the SC and SB are presented in Figure 9a. When the SB is idle, the average SC temperatures are 312.7, 319.3 and 327.1 Kelvin at 0.5, 1.0 and 1.5GHz, respectively. But when the SB is active, the same SC temperatures increase by about 1, 2 and 4 Kelvin for 0.5, 1.0 and 1.5GHz, respectively. This clearly demonstrates the influence of memory addressing on the core layer temperatures. Not only does the average temperature rise with increase in frequency, but also the variance. At higher clock frequencies, thermal ramifications due to memory addressing patterns are more pronounced. The performance trend as seen if Fig. 9b is in accordance with our expectation, in that, instruction throughput benefits directly due to clock frequency increase.

Case (c): Moving along the same analysis path as before, for this case of thermal coupling, we wish to understand the variations in temperature of an 'idle' core directly underneath an 'active' L2 Cache bank. The temperature plots of the remote core (RC) and remote cache bank (RB) in Figure 9a illustrate this situation. Analogous to the previous case, bulk of the power dissipated by the idle RC underneath the active RB is on account of static power. Furthermore, as clock frequency increases, idle RC temperature can increase up to 5 Kelvin higher than the lowest temperature on the core layer.

Case (d): This case is essentially a superposition of Cases (b) and (e). The experiments here attempt to replicate a scenario where multiple cores can access a single L2 Cache bank. As described in Fig. 4 both the SC and the RC access the RB. Since RC is not idle anymore, we observe an increasing trend in its temperature with clock frequency. The slope of this increase however, is slightly steeper when compared to SC temperature (SB active) in Figure 9a. Furthermore, the increase in the clock frequency of the RC - RB island causes the performance of RC and SC to improve (See Fig. 10b). Due to difference in network delays however, slope of the performance curve for the SC is much smaller than that for the RC.

In summary, microbenchmark characterization of the 3D stack sheds light on subtle yet key insights. The EHC of an application thread is affected not only by its own phases but also by memory addressing patterns of neighboring cores. A greedy approach to maximizing performance can indeed utilize the thermal headroom of the package but may not deliver the best energy efficiency (ops/Joule). Consequently, the higher temperatures especially in thermally constrained environments such as the one under consideration, can increase thermal stresses and localized hotspots in turn reducing lifetime reliability of the device. Nevertheless, maximizing performance in the face of unavoidable thermal coupling, necessitates a strategy that cooperatively balances performance, energy and temperature.

4. TRINITY

In this section, we present our proposed approach, TRINITY, an online DVFS controller that dynamically balances the three parameters: performance, energy and temperature to completely utilize the EHC in a 3D stack. TRINITY is, (i) application agnostic, (ii) self-tuning, (iii) distributed (per-core), (iv) based on numerical optimization, and (v) computationally inexpensive to implement. The TRINITY controllers on each core are implicitly coupled via temperature. Therefore, the individual actions taken by the network of controllers works towards making the best use of the EHC. We now present a detailed description of the system models, optimization
Figure 6: Performance and temperature variation when running mem bound and compute bound benchmarks on a source core accessing source and remote cache banks at different core frequencies. SC is Core2.

Figure 7: Performance and temperature variation when running mem bound and compute bound benchmarks on a source core accessing source and remote cache banks at different core frequencies. SC is Core3.

Figure 8: Influence of package boundaries on thermal coupling and performance.
Temperature variation of (i) source core and cache (ii) remote core and cache.

Performance variation of the source core when source bank is ‘idle’ and ‘active’.

Figure 9: Thermal coupling Cases (b) and (c). The error bars are variances in temperature due to different ops/byte and physical locations of the source core.

Temperature variation of source core and remote core.

Performance variation of source core and remote core.

Figure 10: Thermal coupling Case (d). The error bars are variances in temperature due to different ops/byte and physical locations of the source core.

4.1 System Models

Power Model: We linearize the power model in [28] and arrive at a third order polynomial which captures both leakage and dynamic power of the core. The equation is as follows:

\[ P_k = \alpha f_k^3 + \beta f_k + \gamma T_k + \delta f_k T_k + \epsilon \]  

where \( k \) represents the sample time instant, \( f_k \) and \( T_k \) are clock frequency and core temperature, respectively. The first term models the dynamic power and the last four terms of the equation represent leakage power. Since leakage power is strongly correlated with the technology node and packaging parameters, via non-linear regression, we calculate \( \beta, \gamma, \delta \) and \( \epsilon \) offline (See Table 2). To enable TRINITY to be application agnostic, the constant \( \alpha \), which represents the activity factor is therefore determined online. Figure 11a shows that our approximation for the leakage power is within \( \pm 5 \) mW of the value measured on the simulator.

Table 2: Parameters estimated offline.

| \( \beta \)   | \(-426.7 \times 10^{-3}\)  | \( a_1 \) | 0.9998 |
| \( \gamma \) | 0.674 \times 10^{-3}     | \( b_1 \) | 8.46   |
| \( \delta \) | 1.618 \times 10^{-3}     | \( c_1 \) | 37     |
| \( \epsilon \) | -90.38 \times 10^{-3}   | \( \Delta t \) | 1ms    |

Temperature Model: Temperature at any given point in the 3D stack at any given time \( t \) is given by the dynamical equation

\[ \dot{T}(t) = AT(t) + BP(t) \]  

where \( T(t), P(t) \in \mathbb{R}^M \) are the temperature and power vectors, respectively and the matrices \( A \) and \( B \) consist of the thermal resistance and capacitance of the 3D stack [32]. In each of the 6 layers in the 3D stack, broadly, we have 16 power dissipating elements, therefore, \( M = 16 \times 6 = 96 \). The large \( A \) and \( B \) matrices capture the inter-layer and intra-layer thermal coupling allowing for an accurate estimation of the temperature trajectory. At this juncture it is relevant to note that for the 3D stack under consideration, we observe a time constant for the rise in temperature of approximately 40ms and thus the settling time is around 200ms. These numbers are in agreement with practical observations [27]. Solving an optimization problem as described in the Introduction becomes increasingly computationally intensive as the dimensionality of the model increases (typically \( O(M^3) \)). Instead of using Eqn. 2 we make an observation that discretizing and linearizing Eqn. 2 for a short duration of time \( \Delta t \), reduces the model complexity significantly from \( O(96^3) \rightarrow O(1) \). The price paid for this reduction in complexity is in the ability to accurately predict future temperature. Nonetheless, the temperature of a core can now be estimated \( \Delta t \) seconds into the future using the following scalar equation:

\[ T_{k+1} = a_1 T_k + \Delta t (b_1 P_k + c_1) \]  

where we observe that up to \( \Delta t = 1ms \), the simplified temperature model is within 1 Kelvin as compared with values obtained from the simulator (See Fig. 11b). Analogous to the power model, the constants \( a_1, b_1 \) and \( c_1 \) are dependent on the technology node and packaging design choices. Therefore they are estimated offline via non-linear regression (See
The weights $Q$ and $R\ (Q,R>0 \text{ for problem feasibility})$ are tuning parameters that can be modified at run-time to give variable importance to performance and temperature. We set $Q = 1$ and allow $R$ to tune itself at run-time. Equations [5]-[7] are solved periodically after every $T$ seconds by each core independently to determine $f_{k+1}^*$, the clock frequency that maximizes the cost.

The intuition behind the problem definition is as follows: Consider an application whose performance saturates beyond a particular clock frequency and does not vary with time. The periodic calculation of $f_{k+1}^*$ drives the system eventually towards a point where the temperature of the core reaches steady state. This steady state temperature is nothing but the EMT and any further increase in the clock frequency will reduce the cost thereby satisfying our original goal of maximally utilizing the EHC. For a particular choice of $R$, the behavior of the objective function is illustrated in Figure [2]. The value $T$, referred to as the control cycle, is a design parameter which has to be at least greater than (i) measurement, (ii) actuation, and (iii) computation delays. On processors available in the market currently, measurement and actuation delays are approximately 10s of microseconds [3]. The control cycle also depends on the model accuracy since, as observed in the previous section, the simplified temperature model has sufficient accuracy up to a duration of 1ms. Therefore, we choose $T=1$ms in our experiments. We assign 21 clock frequencies between $0.5-1.5$GHz spaced 50MHz apart. To solve the problem described in Eqn. [5] the three steps of the algorithm are listed in Fig. [5]. Since each core solves the optimization problem independently, computing $f_{k+1}^*$ requires finding the maximum element in a 21 length array.

Figure 12: Behavior of the optimization cost.

The tuning parameter $R$ influences all three variables: temperature, performance and leakage energy. In fact, $R \in [R_{min}, R_{max}]$ such that for $R < R_{min}, f_{k+1}^* = f$ and for $R > R_{max}, f_{k+1}^* = \bar{f}$. Emphasizing temperature over performance leads to lower leakage energy whereas greater importance to performance could potentially lead to wasted leakage energy. Therefore it is essential to choose an appropriate value in order to exact the behavior desired. Fixing the value of $R$ is one approach. However, we observe that such a strategy, (i) makes the solution application specific (ii) requires extensive time consuming offline analysis, and (iii) could easily push the controller into saturation where $f_{k+1}^*$ will be remain at either $f$ or $\bar{f}$ for prolonged periods of time. In order to adapt to dynamically varying application phases, we allow $R$ to re-calibrate itself periodically. We call this period $T_R \geq T$. The pseudo code for the re-calibration is described in Figure [14]. The re-calibration step basically determines the bounds for $R$ i.e. $[R_{min}, R_{max}]$ and calculates the next value as $R = R_{min} + \eta (R_{max} - R_{min})$ where $\eta \in [0, 1]$. For the OoO core under consideration, we set $\eta = \sqrt{IPC_{min}/IPC_{max}}$ with $IPC_{max} = \text{Issue Width} = 4$. The IPC ratio heuristic is a means to obtain information about the compute or memory boundedness of the application. The square root of the ratio is chosen to push $R$ towards $R_{max}$ (and thus better performance).

5. RESULTS

In this section we evaluate TRINITY. We first describe the simulation environment and list the benchmark applications...
$$R_{#JK} = 1 \times 10^{-6}$$

$$f(i) = (\sum_{i=0}^{20} z_{012} i^3 + R_{#JK} \times \chi_{012}(i), \quad i = \{0,1,2,\ldots,20\}$$

$$\Delta J_i = J(1) - J(0), \quad \Delta J_{20} = J(20) - J(19)$$

$$R = R_{init}$$

\[ \text{if} (\Delta J_0 < 0, \Delta J_{20} < 0) \]

\[ \text{increase } R \text{ until } \Delta J_0 > 0 \quad \& \quad \Delta J_{20} < 0 \]

\[ R_{max} = R \]

\[ \text{foo1}(R_{\text{max}}, 1) \]

\[ \text{if} (\Delta J_0 > 0, \Delta J_{20} > 0) \]

\[ \text{decrease } R \text{ until } \Delta J_0 > 0 \quad \& \quad \Delta J_{20} < 0 \]

\[ R_{min} = R \]

\[ \text{foo1}(R_{\text{min}}, 0) \]

\[ \text{foo1}(R_{\text{now}}, \text{flag}) \{ \]

\[ \text{if} (\text{flag} == 1) \]

\[ \text{increase } R_{\text{now}} \text{ until } \Delta J_0 > 0 \quad \& \quad \Delta J_{20} > 0 \]

\[ R_{max} = R_{\text{now}} \]

\[ \text{if} (\text{flag} == 0) \]

\[ \text{decrease } R_{\text{now}} \text{ until } \Delta J_0 < 0 \quad \& \quad \Delta J_{20} < 0 \]

\[ R_{min} = R_{\text{now}} \]

\} 

Figure 13: **TRINITY Algorithm.**

$$R_{init} = 1 \times 10^{-6}$$

$$f(i) = (z_{k+1}(i)^2 + R_{init} \times \chi_{k+1}(i)), \quad i = \{0,1,2,\ldots,20\}$$

$$\Delta J_i = J(1) - J(0), \quad \Delta J_{20} = J(20) - J(19)$$

$$R = R_{init}$$

\[ \text{if} (\Delta J_0 < 0, \Delta J_{20} < 0) \]

\[ \text{increase } R \text{ until } \Delta J_0 > 0 \quad \& \quad \Delta J_{20} < 0 \]

\[ R_{max} = R \]

\[ \text{foo1}(R_{max}, 1) \]

\[ \text{if} (\Delta J_0 > 0, \Delta J_{20} > 0) \]

\[ \text{decrease } R \text{ until } \Delta J_0 > 0 \quad \& \quad \Delta J_{20} < 0 \]

\[ R_{min} = R \]

\[ \text{foo1}(R_{min}, 0) \]

\[ \text{foo1}(R_{\text{now}}, \text{flag}) \{ \]

\[ \text{if} (\text{flag} == 1) \]

\[ \text{increase } R_{\text{now}} \text{ until } \Delta J_0 > 0 \quad \& \quad \Delta J_{20} > 0 \]

\[ R_{max} = R_{\text{now}} \]

\[ \text{if} (\text{flag} == 0) \]

\[ \text{decrease } R_{\text{now}} \text{ until } \Delta J_0 < 0 \quad \& \quad \Delta J_{20} < 0 \]

\[ R_{min} = R_{\text{now}} \]

\} 

Figure 14: **Pseudo code for re-calibrating R.**

used. Next we present an evaluation of the proposed control scheme in detail. We implement a DVFS strategy similar to the on-demand Linux CPU governor on the simulator and compare it against TRINITY. We also present results by fixing the core frequencies to 0.5, 1.0 and 1.5GHz. Since TRINITY attempts to balance performance, energy and temperature, we use Energy Delay Product (EDP) along with temperature as the primary comparison metric. In what follows, we also use Energy Delay Product (EDP), Energy Efficiency (ops/Joule), performance (MIPS) and lifetime reliability measured as Mean Time To Failure (MTTF) to understand the implications of using TRINITY.

### 5.1 Experimental Framework

The physical layout is shown in Fig. [15] with the dimensions listed in Table 3 and Figure 16 represents the functional diagram of the 3D stacked architecture. The 3D stacked architecture consists of 16 Out-of-Order (OoO) cores with two levels of cache hierarchy [34], interfacing an HMC style [3] 4GB DRAM via an interconnection network. The simulator is also equipped with power and thermal estimation framework called Kitfox [3]. Kitfox internally models power consumption based on McPat [35] and the thermal calculations are done using 3D-ICE [22], both scaled to 16nm. The front-end for the cycle level simulator [2] is a multicore emulator called Qsim [36] that boots a Linux kernel and executes applications of interest. The x86 instruction streams thus generated are fed into the OoO core timing model. We use DRAMSim2 [37] as the DRAM timing simulator whose voltage and timing numbers are modified based on the work in [38].

**Table 3: Simulation framework parameters. Technology node is 16nm.**

| Component | Parameters and Values |
|-----------|----------------------|
| Processor | Out-of-Order, 6-stage pipeline, 4-wide issue/commit, 0.5 – 1.5GHz |
| L1 Cache per core (16KB) | Private, 8-way, LRU replacement, 32 MSHRs, 64B lines, 1-cyc hit & lookup time |
| L2 Cache per bank (2MB) | 16 banks in total, shared, 8-way, LRU replacement, 128 MSHRs, 64B lines, 24-cyc hit & lookup time |
| Network (1GHz) | 4 x 4 torus ring, 6 port router, baseline x-y routing |
| Memory Controller | 16 MCs in total, rank then bank round robin, close page, Addr-map-chan:row:bank:rank:col |
| DRAM config per vault | 256MB, 1-channel, 4 ranks, 2 banks per rank, 64 bit bus @ 1600MHz |
| Heat Sink | Conventional heat sink, Heat transfer co-eff = 2.8 × 10⁻⁸W/μm²K |
| Per-Layer | TOP LAYER = BEOL: 35μm, SOURC ELAYER = SILICON: 10μm, BOTTOM LAYER = SILICON: 25μm |

![Figure 15: Physical layout of the 3D stacked architecture.](image)

![Figure 16: Functional description of the 3D stack](image)
5.2 Benchmarks

We evaluate the optimization technique proposed over 6 benchmark applications from the PARSEC, SPLASH2x [29] and GraphBig [30] suite. Specifically, we choose blackscholes, streamcluster, barnes (PARSEC and SPLASH2x) and kcore, pagerank and tc (GraphBig). Each of the benchmark applications are executed with 16 threads. The GraphBig applications stress the memory whereas PARSEC and SPLASH2x stress the compute units thus giving a range of application behavior.

5.3 Analyzing TRINITY Performance

Energy efficiency and ED2P results are plotted in Figures [18] and [17] respectively, comparing TRINITY against the three fixed frequencies and ondemand. The right y-axis in both the figures represents the spatial average temperature of the core layer. The control cycle T is set to 1ms. Recalibrating R every control cycle increases the amount of computations performed by the controller and hence we set T_R = 5ms.

The trend of ED2P is not the same for every benchmark. Consequently, the strategy to balance performance, energy and temperature (PET) should be different. In general, for compute intensive benchmarks (blackscholes, barnes and streamcluster), the highest clock frequency delivers the best performance and also results in the highest temperature. TRINITY on the other hand, trades performance for benefits in temperature (lower by 8 Kelvin w.r.t 1.5GHz and 6 Kelvin w.r.t ondemand). In fact, the reduction in ED2P for the compute intensive benchmarks is due to the reduction in performance. Energy efficiency results however reveal that TRINITY and ondemand perform equivalently (< 5% difference). We can therefore conclude that in the process of balancing PET for compute intensive benchmarks, TRINITY achieves similar energy efficiency as ondemand but keeps the temperature 6 Kelvin lower.

Analyzing memory intensive benchmarks (kcore, pagerank and tc), there is no appreciable improvement in performance (MIPS). For example, average MIPS for kcore at 0.5, 1.0 and 1.5GHz is 4360.3, 5074.2 and 5265.2, respectively. Possessing apriori knowledge that the application to be executed is memory intensive, could lead to choosing the lowest clock frequency as a possible strategy. While it certainly keeps the entire 3D stack at a lower temperature, ED2P suffers significantly. In these situations, TRINITY tunes R in such a way that the lower half of the clock frequencies (0.5-1.0GHz) are chosen in the memory intensive phases. For all three benchmarks, temperature of the core layer is at most as high as 1.0GHz. Performance and ED2P, while certainly better than 0.5GHz, are 5% and 13% worse than 1.0GHz, respectively. On closer analysis of the controller data, we observe that predicting performance for the upcoming control cycle based on the previous control cycle, sometimes causes TRINITY to choose a clock frequency that does not maximize performance for the EHC. These mispredictions are mitigated to a certain extent by re-calibrating R every T_R seconds but it is one of the limitations of TRINITY.

Energy efficiency, similar to ED2P, has different trends for different benchmarks as shown in Figure [18]. While it increases for barnes as clock frequency is increased, it reduces for kcore. A detailed breakdown of different comparison metrics is shown in Figure [20]. Note that trading off performance (MIPS), affects ED2P and ED2P directly. Energy efficiency of TRINITY however, is very similar to ondemand (3% better). This is on account of reduced temperature.

To understand the source of temperature reduction, we plot the average power dissipated at individual layers in Figure [19]. The x-axis represents different DVFS options for each benchmark and the y-axis shows average power in Watts. Total power for each DVFS setting is broken down into dynamic and leakage power for the core, L2 Cache and DRAM layers. This distribution of power helps understand the primary source of power consumption for each benchmark application. blackscholes and barnes, both compute intensive, consume majority of the power in the core layer. kcore and pagerank being memory intensive consume greater power in the L2 Cache layer, specifically dynamic power in L2 Cache. Additionally, DRAM dynamic power is higher as well due to increased L2 Cache misses. streamcluster, unlike blackscholes and barnes shows increasing L2 Cache power for increasing frequencies. Finally, although tc consumes approximately same amount of power in both core and cache layers, analyzing average MIPS for the three fixed frequencies and reveals that tc is indeed memory intensive (2741.3, 3633.8 and 4026.7 MIPS at 0.5, 1.0 and 1.5GHz, respectively).

As seen in Fig. [19] the bulk of the power reduction (consequently temperature) comes from reducing dynamic power consumption of the core and cache layers. This is intuitive since DVFS implemented by TRINITY directly affects only the core and the corresponding L2 Cache bank. As compared to ondemand, dynamic power of the core and cache layers reduce by 38.5% and 28.2%, respectively. Furthermore, with respect to ondemand, TRINITY is also able to reduce leakage power of the core and cache layers by 18% each. We attribute the power reduction to the on-line adaptation of R. In memory intensive parts of the application, η is low (< 1) thus guiding the controller to choose the lower end of the clock frequencies. In compute intensive regions, η is high (> 2) allowing for higher clock frequencies to be chosen.

5.4 Impact on Lifetime Reliability

Changes in operating temperatures and voltages incur significant impacts on reliability. Two dominant reliability mechanisms, electromigration (EM) and time-dependent dielectric breakdown (TDDB), are used to evaluate the reliability implications of TRINITY, compared to that of other execution modes. We used the reliability models and parameters from the work in [41] and references therein. Equations [8] and [2] show the reliability models of EM and TDDB, expressed as mean-time-to-failure (MTTF).

\[
MTTF_{EM} = A_{EM} \times \frac{1}{t_{act}} \times V^{-n} \times e^{\frac{E_F}{n}}
\]

\[
MTTF_{TDDB} = A_{TDDB} \times \frac{1}{t_{act}} \times V^{-a+bT} \times e^{\frac{n}{n+1}(z+\alpha\beta V)}
\]

In the reliability equations, V and T are operating voltage and temperature. t_{act} (0 \leq t_{act} \leq 1) is active-state residency obtained from the execution time of each workload. For instance, t_{act} = 0.5 means that a workload utilizes the computing system for 50% of time. It is assumed that the system
can be ideally power-gated for the remaining period and thus has no reliability impact; the system may be used to process other workloads, but resulting reliability impacts contribute to those workloads. \( k \) is Boltzmann’s constant, and other parameters are model-dependent scaling parameters [41]. As shown in Eqn. 8, EM is primarily accelerated by temperature, and voltage has a secondary effect. In fact, a few degrees of average temperature change throughout the lifetime can easily produce several months to years of EM variations. On the other hand, TDDB is more sensitive to voltage changes, but temperature also has a non-negligible effect. The results show that TRINITY achieves 59%, 88%, and 6% better reliability than the ondemand and two fixed frequency executions at 1.5GHz and 1.0GHz, respectively. However, it trades performance improvement with 24% reduction in reliability when compared with the 0.5GHz fixed frequency execution.

### 5.5 Effect of TRINITY Parameter Variations

As mentioned in the previous sections, one of our goals with TRINITY is to design it with practical implementation in mind. Simplifying the model and reducing computational complexity reduces the number of parameters that can be

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**Figure 17:** Controller performance compared against fixed frequencies and ondemand. Controller Parameters: \( T = 1 \text{ms} \) and \( T_R = 5 \text{ms} \). Left y-axis and right y-axis units are ED2P and Kelvin, respectively.

**Figure 18:** Controller performance compared against fixed frequencies and ondemand. Controller Parameters: \( T = 1 \text{ms} \) and \( T_R = 5 \text{ms} \). Left y-axis and right y-axis units are ops/Joule and Kelvin, respectively.

**Figure 19:** Average power consumption by TRINITY compared against fixed frequencies and ondemand. Controller Parameters OPT1: \( T = 1 \text{ms} \) and \( T_R = 5 \text{ms} \).
manually tuned. We study the sensitivity of TRINITY to variations in $T$ and $T_R$, which are the only manually tuned parameters. Reducing the control cycle duration and $T_R$ has the benefit of capturing rapidly varying application phases. But it also increases the amount of controller computations per unit time. We compare three different cases: (1) OPT1 ($T = 1$ms, $T_R = 5$ms), (2) OPT2 ($T = 1$ms, $T_R = 10$ms), and (3) OPT3 ($T = 0.5$ms, $T_R = 5$ms).

On the y-axis in Figure 21 we plot the % difference between TRINITY, ondemand and the three fixed frequencies over all six benchmark applications tested. We also compare temperatures of the three controller variations in the same figure. A notable feature from Fig. 21 is that with respect to 1.0GHz, TRINITY achieves 30%, 5% and 17% better ED2P at approximately same temperature. A second feature is that as compared to 1.5GHz and ondemand, TRINITY trades temperature for performance; on an average TRINITY keeps the cores at least 6 Kelvin cooler. The large improvement in EDP and ED2P in comparison with 0.5GHz is due to the significant reduction in the total run-time of the application.

The third feature concurs with intuition: Increasing $T_R$ implies tuning $R$ less frequently thereby making the controller less responsive to changes in application phases. This increases the effect of performance mispredictions and thus reduces EDP, ED2P and ops/Joule. Consequently, the average temperature for OPT2 is higher than OPT1. Finally, decreasing $T$ (OPT3) does not show appreciable improvement in EDP or ED2P as compared to OPT1.

Akin to any practical thermal/power/energy management approach, TRINITY too faces the challenge of modeling precision vs. controller performance. Applications that would benefit from TRINITY are those that have a mixture of compute and memory bound phases because of the ability to adapt itself at run-time to maximally utilize the EHC. However, if those phases are shorter than the control interval $T$, they might end up being overlooked. TRINITY works particularly well for memory intensive applications like GraphBig because at the same EDP, the average temperature and voltage is lower than ondemand which improves MTTF by 68%. If the objective is to maximize performance alone, we get limited returns in EDP and ED2P from TRINITY. Figure 21 shows that as compared to 1.5GHz, EDP, ED2P and ops/Joule are the lowest for TRINITY.

5.6 Effect of Starting Temperature

The analysis presented in Section 5.3 considers a starting temperature of 300K for every experiment. This however does not expose the secondary effects due to thermal throttling. To simulate practical runtime conditions, in this section we initialize the starting temperature to 323K. The corresponding EDP results are plotted in Figure 22 comparing TRINITY against the ondemand heuristic.

The trend of EDP is not the same for every benchmark. Consequently, the strategy to balance performance, energy and temperature should be different. For compute intensive workloads like blackscholes and barnes, the highest clock frequency (1.5GHz) delivers the best performance but also results in the highest temperature. This causes thermal throttling which significantly reduces performance. TRINITY on the other hand, tries to trade performance for benefits in temperature, 4 K on average with respect to ondemand. Energy efficiency results however reveal that TRINITY and ondemand perform equally well; TRINITY is 6.4% better, arguably within simulation error bounds. The implication is indeed in line with the definition of EMT. TRINITY chooses the clock frequencies such that same or better performance can be achieved at a much lower temperature.

Analyzing memory intensive benchmarks (kcore, pagerank, connectedcomponent and etc), there is no appreciable improvement in performance (MIPS) as core frequencies are increased. For example, average MIPS for kcore at 0.5, 1.0 and 1.5GHz is 4360.3, 5074.2 and 5265.2, respectively. Possessing apriori knowledge that the application to be executed is memory intensive, could lead to choosing a lower clock frequency as a possible strategy. While it certainly keeps the entire 3D stack at a lower temperature, EDP can suffer considerably. Although the average power is small, the application takes much longer to complete. In these situations, TRINITY tunes $R$ in such a way that the lower half of the clock frequencies (0.5 - 1.0GHz) are chosen in the memory intensive phases. Except for connectedcomponent, temperature of the core layer for the remaining three workloads is lower by about 6 K. For connectedcomponent, both ondemand and TRINITY perform equally well and no appreciable
temperature or EDP difference is observed.

Again, to understand the source of temperature reduction, the average power dissipated at individual layers is plotted in Figure 25. The x-axis represents different DVFS options for each benchmark and the y-axis shows average power in Watts. Total power for each DVFS setting is broken down into dynamic and leakage power for the core, L2 Cache and DRAM layers. This distribution of power helps understand the primary source of power consumption for each benchmark application. *blackscholes* and *barnes*, both compute intensive, consume majority of the power in the core layer. *kcore*, *pagerank* and *tc* being memory intensive consume greater power in the L2 Cache layer, specifically dynamic power. Additionally, DRAM dynamic power is higher as well due to increased L2 Cache misses. *connectedcomponent*, unlike other memory bound workloads shows much higher power consumed in the core die. However, power consumed in the L2 Cache and DRAM is larger as compared to compute intensive benchmarks.

As seen in Fig. 23, the bulk of the power reduction (consequently reduction in temperature) comes from reducing dynamic power consumption of the core and cache layers. This is intuitive since DVFS implemented by TRINITY directly affects only the core and the corresponding L2 Cache bank. As compared to ondemand, dynamic power of the core and cache layers reduce by 11.7% and 18%, respectively. Furthermore, with respect to ondemand, TRINITY is also able to reduce leakage power of the core and cache layers by 15.5% and 16.5%, respectively. The power reduction can be attributed to the on-line adaptation of $R$. In memory intensive parts of the application, $\eta$ is low ($<1$) thus guiding the controller to choose the lower end of the clock frequencies. In compute intensive regions, $\eta$ is high ($>2$) allowing for higher clock frequencies to be chosen.

TRINITY is designed so that it can be implemented on a real physical system. Simplifying the model and reducing computational complexity reduces the number of parameters that can be manually tuned. In this section, the sensitivity of TRINITY to variations in $T$ and $T_R$, which are the only manually tuned parameters, is discussed. Reducing the control cycle duration and $T_R$ has the benefit of capturing rapidly varying application phases. But it could also increase the amount of controller computations per unit time. Two cases are compared here: (1) OPT1 ($T = 1$ms, $T_R = 1$ms) and (2) OPT2 ($T = 1$ms, $T_R = 5$ms).

The y-axis in Figure 24b represents the absolute difference between TRINITY and ondemand whereas the y-axis in Figures 24a, 24d and 24e represent % difference. Overall, OPT2 fares slightly worse than OPT1 when using the metrics EDP, ED2P and ops/Joule. OPT2 keeps the temperature of the cores about a degree cooler than OPT1 by trading off performance. This aspect is clearly observed in Figures 24a and 24b.

The notable feature concurs with intuition: Increasing $T_R$ implies tuning $R$ less frequently thereby making the controller less responsive to changes in application phases. This increases the effect of performance mispredictions and thus reduces EDP, ED2P and ops/Joule. Consequently, the average temperature for OPT2 is higher than OPT1.

Akin to any practical thermal/power/energy management approach, TRINITY too faces the challenge of modeling precision vs. controller performance. Applications that would benefit from TRINITY are those that have a mixture of compute and memory bound phases because of the ability to adapt itself at run-time to maximally utilize the EHC. However, if those phases are shorter than the control interval $T$, they might end up being overlooked. TRINITY works particularly well for memory intensive applications like GraphBig because at the same EDP, the average temperature and voltage is lower than ondemand which improves MTTF by 10%.

6. RELATED WORK

Dynamic Thermal Management (DTM) of multicore processors (2D and 3D) has evolved from heuristic based approaches to formal feedback control based techniques. They can be divided into the following categories: (i) Hardware level and (ii) Software level. At the hardware level, DVFS of independent voltage islands has been explored in great detail, for example [20, 25, 28, 31, 42, 43, 44, 45, 46, 47, 48]. Recently, [49] discussed use of thermal TSVs to extract heat from the different layers in an architecture similar to the one described in this work. They boost the performance of applications by exploiting the improved cooling efficiency. Some other approaches to mitigate thermal effects are instruction fetch throttling, clock gating [50, 51] and moving the hottest datapaths closer to the heat sink (thermal herding) [39]. Finally, at the software level we have migrating threads from hot core to cool cores [52, 53], data compression at the memory controller [16], two-level prefetching with throttling off-chip memory links [15], dynamic page allocation
All the works listed in the previous paragraph except [28] and [47] design their techniques wherein core or die temperature is an upper limit i.e. a constraint. Some policies are triggered only under emergencies [50, 51], while the rest optimize a cost while staying within the thermal threshold. TRINITY is not designed to wait till an emergency is triggered. On the contrary, it tries to avoid such scenarios by trading reduction in performance. References [31, 43, 45] develop an MPC based optimal control problem, while [46, 48] present a numerical optimization based approach. The objectives of the problems considered vary: minimizing power [43, 46], maximizing performance [25, 31, 45] and maximizing power efficiency [48]. In contrast to optimization, references [42] and [28] design closed loop feedback controllers to maintain a fixed temperature. TRINITY is similar to the optimization based DVFS approaches but it offers an alternative approach to handle temperature and is computationally cheap to implement. Instead of considering temperature as a constraint, optimizing a cost based on it enables TRINITY to balance parameters which were otherwise dealt with in isolation. MPC and optimization based approaches referenced here are computationally intensive due to the large model dimensions and do not consider the leakage power dependence on temperature. Although [31] proposes a distributed
we present an analysis on lifetime reliability and demonstrate (ii) do not explicitly model static power, (iii) are heuristic
constraint. ligently managing temperature as a resource and not just a
EDP, ED2P, energy efficiency, temperature and also lifetime
parameters and package physical constraints. An analysis of intra- and inter-die thermal coupling effects, the ability
to maximally utilize the effective heat capacity is illustrated.

7. CONCLUSIONS
This work presents an approach to the coordinated control
of performance, energy efficiency and temperature on 3D processor-memory stacks. It introduces the concept of
effective heat capacity as a thermal resource to be managed. Through a comprehensive simulation-based characterization
of intra- and inter-die thermal coupling effects, the ability to
maximally utilize the effective heat capacity is illustrated. An on-line DVFS controller called TRINITY is developed
for the same. Unlike prior research efforts which (i) consider power, performance and temperature in isolation or in pairs,
(ii) do not explicitly model static power, (iii) are heuristic
based, this work acknowledges the complex interplay between
performance, energy, temperature, microarchitectural parameters and package physical constraints. An analysis of EDP, ED2P, energy efficiency, temperature and also lifetime reliability is presented demonstrating the benefits of intelligently managing temperature as a resource and not just a
constraint.

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