Quantum computations are expressed in general as quantum circuits, which are specified by ordered lists of quantum gates. The resulting specifications are used during the optimisation and execution of the expressed computations. However, the specification format makes it difficult to verify that optimised or executed computations still conform to the initial gate list specifications: showing the computational equivalence between two quantum circuits expressed by different lists of quantum gates is exponentially complex in the worst case. In order to solve this issue, this work presents a derivation of the specification format tailored specifically for fault-tolerant quantum circuits. The circuits are considered a form consisting entirely of single qubit initialisations, CNOT gates and single qubit measurements (ICM form). This format allows, under certain assumptions, to efficiently verify optimised (or implemented) computations. Two verification methods based on checking stabiliser circuit structures are presented.

I. INTRODUCTION

The first generation of large scale quantum computers will have to execute fault-tolerant quantum circuits protected by quantum error correcting codes (QECC). Such circuits require large amounts of computational resources (physical qubits and execution time). The computers will be resource constrained, and the mismatch between available and required resources is one of the major hurdles that have to be overcome for quantum computations to be practical. Therefore, before being executed, fault-tolerant quantum circuits need to be optimised with regard to their computational resource overhead.

A circuit is optimised after synthesis, which means that a mathematically formulated quantum algorithm is decomposed into an equivalent quantum circuit formed of quantum gates chosen from a discrete set that can be implemented using the QECC of choice. Furthermore, synthesis refers also to the translation of non-fault-tolerant quantum (non-ft) circuits into ft-circuits. Arbitrary non-ft circuits can be transformed into fault-tolerant ones [22] of the following form: 1) single qubit initialisation; 2) CNOT gates; and 3) single qubit measurements. Such circuits are called ICM, and this work uses them as a starting point for the discussion. Without loss of generality, when referring in the following to ft-circuits their ICM form is considered.

The ICM form of the ft-circuit is an intrinsic property of the non-ft variant: arbitrary non-ft quantum gates can be decomposed into an ICM sub-circuit, and the ft-circuit is the result of ICM decomposing each non-ft circuit gate. The structure of the ft-circuit will resemble the non-ft circuit. However, in order to achieve fault-tolerance, ft-circuits have to be protected by QECCs. QECC choice is flexible, because the ft-circuit’s structure is independent of the chosen QECC. Each QECC has its particularities including the realisation of fault-tolerant quantum gates: some can be easily realised (transversal construction [19]), while others are more complicated (e.g. using state injection, distillation and teleportation [4, 19]).

A. Motivation

This work is motivated by a straightforward problem. Ftcircuits protected by the surface code have two forms: 1) a canonical one, which is the direct result of translating the ICM structure into surface code elements; 2) an optimised one, which is obtained by optimising the surface code protected circuit using topological compression rules [9, 24].

A canonical topological circuit is illustrated in Figure 1a) with the corresponding quantum circuit illustrated in Figure 1b). This topological description of the circuit details how defects in the surface code or Raussendorf code are manipulated to enact the logic operations. The underlying error correction processing is abstracted away in this description and is handled by separate classical components in the software stack of the quantum computer [7, 10]. It is assumed that the quantum circuit level description has already gone through a separate layer of verification procedures and is an accurate implementation of some higher level subroutine. The canonical form is easily verifiable against the quantum circuit itself. For the example in Figure 1a) each pair of white structures running left to right in the im-
age represents the eight qubits in the original circuit, each of the five gray structures represent the five CNOT gates in the original circuit (with topological braids occurring over the relevant subset of qubits involved in each CNOT) and the seven colored pyramids represent state injection and teleportation gates for the seven S gates in the original circuit.

Once this canonical form is constructed from an input quantum circuit (the specifics of this construction can be found in Ref. [22]) it is further optimised using a series of topological compression rules [9, 24]. These compression rules preserve the function of the circuit (how quantum information flows and changes through the circuit) but reduce its 3D geometric volume. The 3D volume of these structures ultimately dictate the physical resource costs (individual qubits and wall time of the quantum computer) involved in implementing them. Consequently, the role of any optimisation technique is to shrink the physical size of the canonical quantum circuit as much as possible.

An example of this topological compression for the circuit in Figure 2a is illustrated in Figure 2b. This compression was performed in Ref. [9] and consisted of nearly 100 individual “moves” (see supplementary material of Ref. [9]). The optimised structure of Figure 2b has a 3D geometric volume over an order of magnitude smaller than its canonical counterpart of Figure 2a while performing exactly the same computational function. However, while Figure 2b can be compared to the original circuit specification of Figure 1a, the compressed version of Figure 2b cannot in an obvious way. Given that for large quantum circuits, potentially millions of “moves” will be needed to transform a canonical circuit to an resource optimised form, we need to find a technique that allows us to verify the resulting topological structure against the original canonical form and hence original circuit level specification.

The naive approach to verifying a compressed topological structure is to simply keep track of every single “move” that is made during compression. After each individual “move”, the two circuits are compared and any differences redundantly checked to ensure they satisfy valid compression rules [9]. This would, computationally, be an extremely costly component of a topological quantum circuit optimizer that is already anticipated to be a complex process in the classical compilation stack for an error-corrected quantum algorithm [13]. Ideally we would want to take a geometric structure that is output from an automated topological circuit optimizer (which currently does not exist) and verify it without having to examine, step-by-step, the detailed record of how it was derived from the canonical structure itself.

Consequently, there are two identical problems: 1) verify that a compressed form is the implementation of a given quantum circuit; 2) develop a translation technique from the optimised form back to the original canonical structure. Given that option 2) is essentially the reverse of keeping a detailed record of how an optimised structure is derived, this work addresses the first problem. By deriving a technique that verifies the optimal topological structure against the original circuit specification, we can not only apply it to the specifics of the surface and Raussendorf code but we can also generalise it further (Section III B).

It should be noted that it is currently unknown if a compressed/optimized topological structure can be derived directly from the original circuit specification. Current techniques start with a verified quantum circuit that has been decomposed into the Clifford + T gate library which is then converted to a resource inefficient canonical form [22] before undergoing compression.

This paper therefore addresses the following problem:

**Problem Statement.** Given two ft-circuits, ft\(_1\) and ft\(_2\), where it is supposed that ft\(_2\) is an implementation of ft\(_1\), determine if ft\(_1\) and ft\(_2\) are functionally equivalent (is the supposition true?).

### B. Implementation and black box analogy

The term implementation from the problem statement will be explained in the following using a black box analogy. If ft\(_1\) and ft\(_2\) would be expressed in the quantum circuit formalism, ft\(_2\) is seen as a transformation of ft\(_1\) through gate identities (e.g. \(HXH = Z\)) which leave the number of qubits unchanged. The transformation is considered unknown, and it is not computationally feasible to backtrack all potential gate identity sequences to obtain ft\(_1\). This allows to consider that, on the one hand, ft\(_1\) is known (its wires and gates are visible and its functionality is captured by a functional specification) and, on the other hand, ft\(_2\) seems to be hidden in a black box (it is not known how it was obtained). Thus, implementation indicates a kind of structural relation between ft\(_1\) and ft\(_2\): the latter should be obtained from ft\(_1\) without changing the number of qubits.

The circuit’s structure is partially determined by the number of operated qubits. The black box model used in this work considers that qubit initialisations and measurements (including ancilla) are external to the box containing the circuit. The ft\(_2\) circuit is applied to a known number of qubits (ancilla or not), and this indicates a compatibility between the black box model and the initial problem of determining if a canonical form circuit (an illustration of ft\(_1\)) is equivalent to a compressed form (an illustration of ft\(_2\)). Compressed circuits act like black boxes, because no method seems to be currently known about how to read the computation from a compressed braided circuit, and only qubit initialisations and measurements are recognisable (accessible, external to the box).

Consequently, because the number of ft\(_2\) qubits can be determined, the herein presented verification assumes that ft\(_1\) and ft\(_2\) operate on the same number of qubits. Otherwise, although the circuits may be functionally equivalent (e.g. ft\(_1\) is the identity computation on a
FIG. 1: A canonical topological circuit is constructed directly from a circuit level specification that is, in general, given in terms of the Clifford + $T$ library [22]. Our process assumes that the circuit level description has already been optimised and verified against a higher level specification and is therefore correct. The canonical topological circuit can be verified by inspection against the circuit description but is not optimised with respect to physical qubit and time resources due to its large 3D volume. Figure a) represents a small state-distillation circuit containing eight qubits, five multi-target CNOT gates, seven single qubits $S$-gates and seven Clifford measurements. The output of the circuit is the single uppermost qubit. Figure b) is the canonical topological form. Each of the eight qubits are represented as pairs of white puzzle pieces or “defects” running left to right. Each CNOT is a gray loop that braids with the relevant qubits in the circuit involved in the CNOT and the $S$-gates are the respective coloured pyramid structures [?].

C. Related Work and Contributions

The problem of verification is analysed in at least two contexts. First, verification is performed in the context of quantum circuit design automation: given a circuit that is known to be correct, the task is to prove that a new circuit (e.g. optimised) is equivalent to the original circuit [27]. Multiple approaches were investigated including verification during synthesis (compilation) [2], SAT-based approaches [27] and QMDD-based approaches [26]. Second, verification is concerned with checking whether quantum computers are indeed producing correct results [19], where a verifier with (almost) classical computing capabilities tries to determine if a black boxed machine (a prover which is an untrusted entity [1]) is falsifying the results of a quantum computation. The methods devel-
FIG. 2: Representation of an ft-circuit protected by the surface code [9]: a) canonical; b) optimised. Both circuits are functionally equivalent, and produce the same output, but circuit b) requires far less physical resources (physical qubits, time) than circuit a). Circuit, a) is easily mapped to the original circuit specification, while b) is not.

This work is based on the design automation interpretation of the verification problem. However, the methodology presented in this work is somehow related to [11], because it uses stabilisers for verifying optimised ft-circuits.

Previous results regarding the problem stated in this work were presented in [20]. In that work ft-circuits are protected by topological QECCs (e.g. surface codes), and the validity of optimised (compressed) ft-circuits is based on mapping the circuits to an underlying lattice of physical qubits (necessary for the QECC) and simulating the resulting lattice circuit. The ft-circuit was considered high-level and the lattice low-level. It was recognised that checking the validity of the high-level optimised circuit can be performed efficiently by simulating only low-level stabiliser circuits.

This work advances the results from [20]. First, the specification format was not defined clearly, and this work will fill this gap. Second, the ft-circuits were not considered in their ICM form, and this affected the generality of the approach, because it did not take into consideration that some ft-circuit gates require probabilistic corrections which cannot be tracked in the Pauli frame [21] (e.g. see Section II C). Third, we extend the results from [22] and show that there are two distinct types of ICM forms (see Section II A 1). Fourth, the methods presented herein do not require any lower level circuit simulations. Finally, we argue that the specification format
and the verification method can be used to replace (to a certain degree) tomographic methods for testing quantum computations implemented in hardware.

II. METHODS

This work proposes a quantum circuit specification format which includes all necessary information to represent ft-circuits. This section presents a step-by-step derivation of the proposed specification format. The important characteristics of a specified ft-circuit are determined starting from a classification of ancilla qubit types. Afterwards, the concept of stabiliser truth table is introduced. Finally, in conjunction with the ICM form of ft-circuits, the effect of single qubit measurements is briefly analysed. This allows to clearly define the specification format, and to highlight one of its applications, which is verification.

A. Classification of Ancilla Qubit Types

Quantum information processing can be analysed using a black-box analogy of quantum circuits. A black-box circuit operates on IO-qubits and various ancillae types: IO-qubits are the interface to the box, and ancillae are internal to the box. The main difference between the IO- and the ancilla qubits is that, the initialisation and measurement of the first is flexible (multiple bases are allowed), whereas ancillae are initialised and measured into specific bases.

Both ft- and non-ft circuits employ ancillae. In a non-ft circuit, computational ancillae are temporary work-benches (e.g. in quantum arithmetic circuits). Such ancillae are, by definition, initialised in a determined state, used during the computation, their state is reversed to the initial one, and finally the qubits are implicitly measured.

In particular, ft-circuits are commonly analysed from the perspective of the Clifford + gate set. As a result, two additional ancillae types exist: teleportation and distillation. Quantum information teleportation is a computational primitive used in the non-transversal ft-gate constructions of the T, P and V rotation gates. Gate functionalities are implemented by entangling an initial qubit (IO-qubit or ancilla) with a teleportation ancilla. Distillation ancillae are used during the preparation of rotated basis initialisation or measurement.

1. Rotated Initialisation and Rotated Measurement

Due to the manner in which ft-gates are implemented through teleportation, there are two techniques for implementing them: 1) rotated-initialisation (Figure 3a), where the teleportation ancilla is initialised into a rotated basis (A or Y, Equations 1 and 2) and the initial qubit is measured in either the X or Z basis; or 2) rotated-measurement (Figure 3b), having the teleportation ancilla initialised into either X or Z and the initial qubit measured in A or Y.

\[
|A_0\rangle = \frac{1}{\sqrt{2}} (|0\rangle + e^{i\frac{\pi}{4}}|1\rangle); |A_1\rangle = \frac{1}{\sqrt{2}} (|0\rangle - e^{i\frac{\pi}{4}}|1\rangle)
\]

\[
A = |A_0\rangle \langle A_0| - |A_1\rangle \langle A_1|
\]

\[
|Y_0\rangle = \frac{1}{\sqrt{2}} (|0\rangle + i|1\rangle); |Y_1\rangle = \frac{1}{\sqrt{2}} (|0\rangle - i|1\rangle)
\]

\[
Y = |Y_0\rangle \langle Y_0| - |Y_1\rangle \langle Y_1|
\]

An ft-circuit can be transformed with constant overhead (a supplemental ancilla and a single CNOT) from one technique to the other (e.g. Figure 3b, where the P gate is replaced by the circuit from Figure 3c). The transformation is based on the observation that a rotated
basis measurement is equivalent to first applying rotation gates before measuring in the X or Z basis.

Consequently, ft-gate construction techniques are equivalent. It is possible to rewrite an entire rotated-initialisation circuit into a rotated-measurement one, or vice versa, by: 1) reversing CNOT directions, and 2) switching the interpretation of initialisation and measurement (see the differences between Figure 5(a) and 5(b)).

High fidelity measurements or initialisations, necessary for reaching the fault-tolerant threshold, are achieved through distillation procedures (applicable to both A and Y states). The procedures, magic state distillation protocols [5], are implemented as stabiliser sub-circuits using distillation ancillae. These ancillae are initialised into the X or Z basis, are interacted during the protocol, and measured in a rotated basis (e.g. Figure 3g). A distillation sub-circuit outputs (probabilistically) a higher fidelity rotated state required as input (teleportation ancilla) to a rotated-initialisation gate (e.g. a P-gate in Figure 5g).

2. Classification Summary

IO-qubit and ancillae properties can be summarised: IO-qubits are initialised into X or Z, and are measured into X or Z. Computational ancillae are implicitly measured in the initialisation basis (e.g. if initialised into |0⟩, the measurement is in the Z basis). Teleportation and distillation ancillae are measured in a basis different to initialisation: initialised into a rotated basis and measured in X or Z, or vice versa.

There is a similarity between all ancillae types: they are interacted entirely through CNOT gates. Additionally, on the one hand, the IO-qubits, the computational and the teleportation ancillae are a priori known elements of the ft-circuits. On the other hand, distillation ancillae are dynamically included into circuits whenever the initialisation/measurement fidelities are low. The existence of distillation ancillae is a posteriori established: these are not required if state fidelities are sufficiently high.

B. Stabiliser Truth Table

Ft-circuits consist of a stabiliser and a non-stabiliser partition. The contents of each each partition depends on the chosen ft-gate implementation:

- rot. - meas. - stabiliser: initialisations and CNOTs; non-stabiliser: measurements;
- rot. - init. - stabiliser: CNOTs and measurements; non-stabiliser: initialisations.

The behaviour of the stabiliser partition is captured by a so-called stabiliser truth table, which can be constructed by conjugating input stabilizers with the unitary representing an all Clifford circuit. The table’s structure is introduced by the example of the smallest possible ft-circuit: a CNOT gate. This circuit contains two IO-qubits and no ancillae. Its inputs are initialised in either the X or the Z basis, and its outputs are measured in the same two bases. Table I is the stabiliser truth table (c indicates the control and the t the target qubits) representing the following stabiliser transformations:

\[
X_c I_t \rightarrow X_c X_t; I_c X_t \rightarrow I_c X_t; \\
Z_c I_t \rightarrow Z_c Z_t; I_c Z_t \rightarrow Z_c Z_t.
\]

Definition 1. A stabiliser truth table is the description of the functionality implemented by an ft-circuit stabiliser partition. The table enumerates as rows each relevant circuit input and its corresponding output.

Stabiliser truth tables are obtained by conjugating the circuit IO-qubit stabilisers (X or Z) through the gates from the CNOT region. As a result, a truth table consists of two regions (input stabilisers and output stabilisers) corresponding to the CNOT region of the ft-circuit. Definition 1 shows the similarity between a stabiliser and a Boolean truth table, but in contrast to the latter, the stabiliser version has a major advantage: it has a linear length in the number of qubits considered (see discussion in the section detailing its construction). The stabiliser truth table includes all qubit types except the distillation ancillae, because: a) their existence is determined only during the computation; b) distillation sub-circuits do not influence the computation.

1. Stabiliser Truth Table Operations

The usual stabiliser notation can be forced and stabiliser truth table rows can be handled as usual stabilisers. All possible circuit states can be inferred/computed using stabiliser table row additions and multiplications.

| Nr. | i_c, i_t, o_c, o_t |
|-----|--------------------|
| 1   | X I X X            |
| 2   | I X I X            |
| 3   | Z I Z I            |
| 4   | I Z Z Z            |

TABLE I: The stabiliser truth table of a CNOT.
For example, the expected output after inputing $X_cX_t$ to a CNOT results by multiplying the corresponding rows from Table 1 (superscript $i$ and $o$ indicate inputs and outputs): 

$$S_1 = (X_c^i I_c^i X_t^o X_t^o)(I_c^o X_c^o I_t^o X_t^o) = X_c^i X_t^i X_c^o I_t^o$$

The following sections will show that, similar to measurement-based computing [23] where qubit initialisation basis and qubit measurement order determine the implemented computation, the output state of an ft-circuit is determined by the sequence of table rows operations. For the beginning, the T- ft-gate is a straightforward example. The non-ft T gate would transform $X \rightarrow (X+Y)/\sqrt{2}$ and $Z \rightarrow Z$, but the ft-gate implementation will be structurally equivalent to the circuit from Figure 3 (has the Y basis replaced by an A basis). Therefore, in this case, stabiliser transformations are partially determined by the CNOT region of the circuit.

The expression $S_1$ shows that it is possible to express the transformation of the IO-qubit input stabiliser $X$ (upper qubit, before the CNOT target) to an output stabiliser $X$ (bottom qubit, after the CNOT’s control). Simultaneously, the stabiliser superposition resulting after the ft-gate application is expressed by $S_2$ and $S_1$ (row addition shows that $X_t^i$ can result to $Y_c^o I_t^o$ and $X_c^o I_t^i$).

$$S_2 = (X_c^i I_c^i X_t^o X_t^o)(Z_c^i I_c^o Z_t^o I_t^o) = Y_c^i I_c^o X_t^o$$

$$S_3 = S_1(I_c^o X_c^o I_t^i) = Y_c^i X_t^i I_t^i$$

$$\frac{(S_3 + S_1)}{\sqrt{2}} = ((Y_c^i X_t^i Y_c^o I_t^i) + (X_c^i X_t^i X_c^o I_t^i))/\sqrt{2}$$

2. Efficient Construction

The stabiliser truth table can be efficiently determined. The table is the result of simulating the stabiliser partition using all the basis input states. The simulation is straightforward for the rotated measurement construction: the non-stabiliser bases are at the end of the circuit, so simulation will stop right before measurements.

For rotated initialisation the construction seems more difficult. Not all the inputs are stabiliser states. Although the $A$ and the $Y$ matrices are members of the Clifford group [5], the eigenvectors of $A$ represent non-stabiliser states. Therefore, in this ft-gate construction, teleportation ancillae will be stabilised by superpositions (e.g. $|A_0\rangle$ is stabilised by $(X + Y)/\sqrt{2}$). Computing the truth table, having non-stabiliser inputs, results in an exponential overhead which is difficult to mitigate [12].

However, it is possible to efficiently construct a stabiliser truth table by temporarily replacing the rotated teleportation ancillae initialisations with $X$ and $Z$ basis initialisations. We motivate this decision by two equivalent arguments based on the observation that the truth table expresses ft-circuit basis states.

The first argument: due to $(X + Y)/\sqrt{2} = (X + iXZ)/\sqrt{2}$, it is sufficient to compute the $X$ and $Z$ stabiliser transformations originating after a teleportation ancillae initialised into the $A$ basis: the stabiliser superposition can be computed from the two $X$ and $Z$ transformations (similarly to Equation 3). The computation would still introduce an exponential overhead, but the computation itself is not required, because it is a direct result of qubit initialisations and measurements (see the section detailing measurement rules and specification definition).

The second argument: the circuit in Figure 3 (analogous to the circuit in Figure 3) constructs a Bell state on the second and third qubits (stabilised by $XX$ and $ZZ$, see dotted box in the figure). If rotated-initialisation circuits would be rewritten as rotated-measurements, the two resulting teleportation ancilla introduce two rows into the truth table: an $X$ and a $Z$ stabiliser transformation.

Therefore, in a $q$-qubit ft-circuit, each IO-qubit is initialised in either $I$ (the identity matrix), $X$ or $Z$, such that there are $3^q - 1$ possible input states ($I_1 \ldots I_q$ needs not to be included). However, at most $2q$ basis states are relevant. Each IO-qubit needs to be sequentially initialised into $X$ and $Z$, while keeping the remaining IO-qubits initialised into $I$. This consideration introduces two rows into the table for each IO-qubit. Ancilla qubits have a predetermined initialisation basis: a) rotated initialisation ancillae are simulated like IO-qubits (sequential $X$ and $Z$ initialisation) and two table rows are introduced into the table; b) rotated measurement ancillae introduce a single table row, because they are initialised in either the $X$ or $Z$ basis.

C. Measurement Rules

Finally, the measurement of qubits in fault-tolerant quantum circuits is analysed before introducing the specific format.

Fault-tolerant rotation gate implementations are probabilistic because they use teleportation mechanisms. Thus, gate outputs require a correction indicated by the measurement result of the initial qubit. An incorrect application of $P$ or $V$ is corrected a posteriori by the application of Pauli gates [21], but this does not hold for incorrect T gate applications. Such gates need $P$ gate corrections [5] (Figure 4).

The measurement basis of teleportation ancillae is classically controlled through a function of the initial qubit measurement. In Figure 4, if the $A$ basis measurement results in eigenvalue -1 it is an indication that $T^\dagger$ was applied instead of $T$, and the second measurement will be performed in the $Y$ basis (a correctional $P$ gate is implemented). Otherwise, eigenvalue 1 indicates the correct application of $T$, the second measurement is in the $X$ basis, thus only teleporting the intermediary state from the middle ancilla to the circuit’s output.
III. RESULTS

The previous analysis offers the necessary elements for defining a specification format. Quantum circuits are generally specified as gate lists. In contrast, classical circuits are specified in various manners including Boolean truth tables and gate lists. Generating classical circuit truth tables is an exponentially complex task, which is even more complicated for quantum circuits due to the non-discrete nature of qubit states.

A. The Specification

In the following the stabiliser truth table is a central component of the specification.

Definition 2. A quantum circuit specification is the tuple \((ST, I, O)\), where \(ST\) is a stabiliser truth table, \(I\) is the set of qubit initialisation basis, and \(O\) is a list of qubit measurement basis rules.

Definition 2 illustrates the relation between teleportation-based, measurement-based and fault-tolerant quantum computing \([6]\). Both sets, \(I\) and \(O\) refer only to ancillae (computational or teleportation), because IO-qubit measurement is flexible. The rules defined in \(O\) express the dynamics introduced by the probabilistic nature of measurements: the measurement basis of a qubit depends on previous qubit measurement results.

Due to the structure of the tuples, \(O\) specifies a measurement order of tuples of the form \((q_1, B_1, q_2, B_2, B_3)\) interpreted as “if the result after measuring qubit \(q_1\) in basis \(B_1\) has eigenvalue 1, then qubit \(q_2\) is measured in basis \(B_2\), otherwise in basis \(B_3\)”. The tuple \((q_1, B_1, 0, 0, 0)\) represents measurements that do not generate classical control signals.

For example, the specification of an uncorrected T\(t\) gate contains the initialisation set \(I = \{(q_2, A)\}\) and the measurement set \(O = \{(q_1, Z, 0, 0, 0)\}\). The stabiliser truth table would be again Table 1.

The output state could be constructed in a systematic and determined way by using information about teleportation ancillae initialisation basis: for \(Y\), \(row multiplications\) are required, and for \(A\), \(row multiplications and additions\). However, the output state is not required. Skipping its computation avoids an exponential representation and computational overhead of the circuit quantum state space. The functionality of the circuit is determined in a computationally functional manner by the measurement order from \(O\). That set is an expression of the initial non-\(t\)-circuit gate list.

B. Verification

The specification format can be used to solve the problem stated in Section I A.

Theorem 1. An \(t\)-circuit implementation passes the verification against a specification \(Spec = (I, ST, O)\), if and only if: 1) all of its ancillae are initialised according to \(I\), 2) its stabiliser partition supports \(ST\), and 3) all its ancillae are measured according to \(O\).

A circuit which satisfies the three properties of \(Spec\) is an implementation of the specification. Furthermore, the verification, as mentioned in Section I A, assumes that the \(t\)-circuit and the specification \((Spec)\) refer to the same number of qubits. Under this assumption, the opposite direction of the theorem requires only the proof of the second criterion. This can be shown using a method similar to reversible circuit equivalence checking \([26, 27]\) (following section).

C. \(t\)-circuits verification: Equivalence Checking

Definition 2 was based on the observation that \(t\)-circuits consist entirely of CNOT gates and, as a result, the task of \(t\)-circuit optimisation is to minimise the number of such gates. Thus, as long as the circuits have the same number of qubits initialised/measured in the same basis, \(t\)-circuit equivalence verification is efficient, because the second criterion in Theorem 1 is shown through stabiliser circuit equivalence: checking the stabilisers from the truth table (as defined in Section III A).

The following two examples illustrate the equivalence checking technique: the first uses the quantum circuit formalism, and the second is an application on compacted braided structures.

1. Circuit level verification

The rotated basis measurement ICM form of the T gate (Figure 6a) can be rewritten by commuting the CNOT gates into the circuit from Figure 6(b). According to the problem statement, Figure 6a is a potential illustration of \(ft_1\) and Figure 6b of \(ft_2\) existing in a black box with visible inputs and outputs.
fication $Spec = (I, ST, O)$ will be derived from $ft_1$:

$I = \{(q_2, Z), (q_3, Z)\}$

$O = \{(q_2, A, q_3, X, Y)\}$

| Nr. | Inputs | Outputs |
|-----|--------|---------|
| 1   | X I I  | X X X   |
| 2   | Z I I  | Z I I   |
| 3   | I Z I  | Z Z I   |
| 4   | I I Z  | I Z Z   |

Although, for the purpose of this example, the gate sequence of $ft_2$ is known, it is assumed that only its inputs and outputs can be accessed. It is necessary to check (verify) that the stabiliser transformations from the $Spec$ are supported by $ft_2$.

2. Verification of compressed braided structure

Simultaneously, the verification is efficient also, because ft-circuit optimisation does not change the measurement sequence determined by $O$. Such a change is analogous to executing a different non-ft circuit gate list. Additionally, it would not be of benefit to modify the initialisation and measurement sets without reducing the number of circuit qubits. The number of io-qubits is fixed through the algorithm specification (e.g., a quantum adder on 4 qubits) and only the ancillae number could be optimised. This is a task of non-ft circuit optimisation and there are two possible strategies. Firstly, there are various investigations about the trade-off between a non-ft circuit’s number of gates and the number of computational ancillae [18]. Secondly, the number of teleportation ancillae is a function of the number of single qubit rotational gates. Minimising the number of such gates is performed through optimal Clifford + $T$ circuit synthesis or efficient arbitrary gate decompositions [17, 25]. Reducing the number of distillation ancillae would also be the entirely separate problem of optimal distillation circuits which is a subproblem of non-ft circuit optimisation.

D. Implementation Verification

A circuit designed and optimised for a specific quantum computing architecture will be implemented and executed in hardware.

The verification of an implemented quantum circuit is generally performed through tomographic methods which are computationally expensive and not scalable for large circuits. The practicality of a quantum circuit specification is directly related to the complexity of verifying if implemented circuits are conforming to their specification. We argue that implemented circuits could be efficiently verified in a setting where: 1) the quantum computer architecture allows flexible qubit initialisations or measurements, thus supporting also rotated basis such as $A$ or $Y$, and 2) the initialisations and the measurements are trusted.

Assuming that the inputs and the outputs of the implementation are configurable, it is possible to efficiently verify the stabiliser truth table of the implementation using the same arguments as in Section II B. Verification is probabilistic, as each truth table row needs to be verified multiple times, but there is a constant number of repetitions required to polynomially increase the overall verification probability. This happens because the main issue with implementation verification is related to initialisations and the measurements.

The difficulty of verification is transformed into the problem of trusting the inputs and outputs of the circuits. From an engineering point of view, the devices used to initialise or to measure qubits are identical components of the computer. Ensuring their correct functionality is a general, and not a circuit, implementation problem. Therefore, trusting quantum IO-devices is similar to how one trusts the current transistor technology: once the technology is mature, individual IO-device instance will need testing, but this is performed separately from the quantum computer. Furthermore, we did not assume that any component of the quantum computer will have a Byzantine behaviour. The proposed implementation verification method assumes that hardware can be trusted, which is entirely opposite to approaches like [19].

IV. CONCLUSION

Ft-circuits are necessary during the implementation of practical large-scale quantum computations. Their regular structure is the foundation of a specification format consisting of a stabiliser truth table and two sets regarding qubit initialisation and measurement. The major advantage of the specification is that it shows that ft-circuits can be efficiently verified using a conceptually simple method. Future work will result in the development of a scalable verification software for large scale ft-circuits.

ACKNOWLEDGMENTS

A.P. acknowledges support from the Linz Institute of Technology (Project CHARON).

[1] Dorit Aharonov and Umesh Vazirani. *Is quantum mechanics falsifiable? A computational perspective on the foundations of quantum mechanics*. Computability: Tur-
[2] Matthew Amy, Martin Roetteler, and Krysta M Svore. Verified compilation of space-efficient reversible circuits. In *International Conference on Computer Aided Verification*, pages 3–21. Springer, 2017.

[3] Stefanie Barz, Joseph F Fitzsimons, Elham Kashefi, and Philip Walther. Experimental verification of quantum computation. *Nature physics*, 9(11):727–731, 2013.

[4] S. Bravyi and A. Kitaev. Universal quantum computation with ideal Clifford gates and noisy ancillas. *Phys. Rev. A.*, 71:022316, 2005.

[5] Sergey Bravyi and Alexei Kitaev. Universal quantum computation with ideal clifford gates and noisy ancillas. *Physical Review A*, 71(2):022316, 2005.

[6] Andrew M Childs, Debbie W Leung, and Michael A Nielsen. Unified derivations of measurement-based schemes for quantum computation. *Physical Review A*, 71(3):032318, 2005.

[7] Simon J. Devitt, Austin G. Fowler, Todd Tilma, William J. Munro, and Kae Nemoto. Classical processing requirements for a topological quantum computing system. *International Journal of Quantum Information*, 8:121–147, 2010.

[8] Austin G Fowler. Time-optimal quantum computation. *arXiv preprint arXiv:1210.4626*, 2012.

[9] Austin G Fowler and Simon J Devitt. A bridge to lower overhead quantum computation. *arXiv*, 1209, 2012.

[10] Austin G Fowler, Matteo Mariantoni, John M Martinis, and Andrew N Cleland. Surface codes: Towards practical large-scale quantum computation. *Physical Review A*, 86(3):032324, 2012.

[11] Keisuke Fujii and Masahito Hayashi. Verifiable fault tolerance in measurement-based quantum computation. *Physical Review A*, 96(3):032301, 2017.

[12] Hector Garcia and Igor L Markov. Quipu: High-performance simulation of quantum circuits using stabilizer frames. In *Computer Design (ICCD), 2013 IEEE 31st International Conference on*, pages 404–410. IEEE, 2013.

[13] Alexandru Gheorghiu, Theodoros Kapurniotis, and Elham Kashefi. Verification of quantum computation: An overview of existing approaches. *arXiv preprint arXiv:1709.06984*, 2017.

[14] Masahito Hayashi and Tomoyuki Morimae. Verifiable measurement-only blind quantum computing with stabilizer testing. *Physical review letters*, 115(22):220502, 2015.

[15] D. Herr, F. Nori, and S.J. Devitt. Lattice Surgery Translation for Quantum Computation. *New. J. Phys.*, 19:013034, 2017.

[16] Stephen P Jordan. Strong equivalence of reversible circuits is conp-complete. *Quantum Information & Computation*, 14(15-16):1302–1307, 2014.

[17] Vadym Kliuchnikov, Dmitri Maslov, and Michele Mosca. Fast and efficient exact synthesis of single-qubit unitaries generated by clifford and t gates. *Quantum Information & Computation*, 13(7-8):607–630, 2013.

[18] D Michael Miller, Robert Wille, and Rolf Drechsler. Reducing reversible circuit cost by adding lines. In *Multiple-Valued Logic (ISMVL), 2010 40th IEEE International Symposium on*, pages 217–222. IEEE, 2010.

[19] Michael A Nielsen and Isaac L Chuang. *Quantum computation and quantum information*. Cambridge university press, 2010.

[20] Alexandru Paler, Simon Devitt, Kae Nemoto, and Ilia Polian. Cross-level validation of topological quantum circuits. In *International Conference on Reversible Computation*, pages 189–200. Springer, 2014.

[21] Alexandru Paler, Simon Devitt, Kae Nemoto, and Ilia Polian. Software-based pauli tracking in fault-tolerant quantum circuits. In *Design, Automation and Test in Europe Conference and Exhibition (DATE), 2014*, pages 1–4. IEEE, 2014.

[22] Alexandru Paler, Ilia Polian, Kae Nemoto, and Simon J Devitt. Fault-tolerant, high-level quantum circuits: form, compilation and description. *Quantum Science and Technology*, 2(2):025003, 2017.

[23] R. Raussendorf, D.E. Browne, and H.J. Briegel. Measurement-based quantum computation with cluster states. *Phys. Rev. A.*, 68:022312, 2003.

[24] Robert Raussendorf, Jim Harrington, and Kovid Goyal. Topological fault-tolerance in cluster state quantum computation. *New Journal of Physics*, 9(6):199, 2007.

[25] Neil J Ross and Peter Selinger. Optimal ancilla-free clifford+ t approximation of z-rotations. *arXiv preprint arXiv:1403.2975*, 2014.

[26] Robert Wille, Daniel Große, D Michael Miller, and Rolf Drechsler. Equivalence checking of reversible circuits. In *Multiple-Valued Logic, 2009. ISMVL’09. 39th International Symposium on*, pages 324–330. IEEE, 2009.

[27] Shigeru Yamashita and Igor L Markov. Fast equivalence-checking for quantum circuits. In *Proceedings of the 2010 IEEE/ACM International Symposium on Nanoscale Architectures*, pages 23–28. IEEE Press, 2010.