Surface Preconditioning and Postmetallization Anneal Improving Interface Properties and $V_{th}$ Stability under Positive Gate Bias Stress in AlGaN/GaN MIS-HEMTs

Anthony Calzolaro,* Nadine Szabó, Andreas Großer, Jan Gärtner, Thomas Mikolajick, and Andre Wachowiak

Trapped states at the dielectric/GaN interface of AlGaN/GaN-based metal–insulator–semiconductor high electron mobility transistors (MIS-HEMTs) can cause threshold voltage ($V_{th}$) instability especially under positive gate bias stress. Herein, the influence of O$_2$ plasma surface preconditioning (SPC) before the atomic layer deposition of the Al$_2$O$_3$ gate dielectric and of N$_2$ postmetallization anneal (PMA) after gate metallization on the Al$_2$O$_3$/GaN interface quality is investigated. The interface is characterized by multifrequency capacitance–voltage measurements which show a smaller frequency dispersion after the employment of SPC and PMA treatments with a reduction of the interface trap density $D_{it}$ to a value in the order of $2 \times 10^{12} \text{cm}^{-2} \text{eV}^{-1}$ near the conduction band edge. The effectiveness of SPC and PMA is demonstrated in Al$_2$O$_3$/AlGaN/GaN MIS-HEMTs by pulsed current–voltage measurements which reveal improved $V_{th}$ stability.

1. Introduction

AlGaN/GaN metal–insulator–semiconductor high electron mobility transistors (MIS-HEMTs) are promising candidates for next-generation high-efficiency and high-voltage power applications.[1] This is a result of the excellent physical properties of GaN-based materials in terms of critical electric field and carrier saturation velocity, combined with the high carrier density and large mobility of the two-dimensional electron gas (2DEG) confined at the AlGaN/GaN interface which enables a low on-state resistance.[2] Moreover, the employment of an insulator in MIS-HEMTS compared to Schottky-Gate HEMTs gives the additional advantage of significant gate leakage reduction, enabling larger gate bias swing and better immunity to gate breakdown.[3,4] However, the insertion of a gate dielectric can cause operational instability due to the presence of high-density trap states located at the dielectric/III-nitride interface or within the dielectric.[5–8] Interface trap states can lead to dynamic charge/discharge processes which are critical especially in the case of wide bandgap GaN-based materials where traps can be deeply located in the bandgap and can result in a significant threshold voltage ($V_{th}$) instability due to their extremely slow detrapping behavior. The $V_{th}$ instability under different bias conditions in AlGaN/GaN-based MIS-HEMTs has been often reported.[9–13] In particular, serious $V_{th}$ shift induced by forward gate bias stress due to electron trapping at the dielectric/III-N interface is one of the major concern in terms of device reliability.[14–17] Therefore, the minimization of trap states at the interface is a critical issue for GaN-based MIS-HEMTs. Although a reduction of the interface trap density ($D_{it}$) has been reported after various surface treatments and postdeposition annealing,[6,18–24] still few reports have dealt with the effects of surface and postdeposition treatments in terms of $D_{it}$ and their related implications on $V_{th}$ stability during forward gate bias stress conditions.

In this context, this work investigates the interface of Al$_2$O$_3$/III-nitrides structures where atomic layer deposited (ALD) Al$_2$O$_3$ is used because of its promising properties as gate dielectric in MIS-HEMTs in terms of large bandgap (7–9 eV), high dielectric constant (8–10), and large conduction-band offset to GaN ($\approx 2.1 \text{eV}$).[25,26] In particular, the effects on the Al$_2$O$_3$/III-nitrides interface of an O$_2$ plasma-based surface treatment applied before the Al$_2$O$_3$ deposition and of a N$_2$ annealing after gate metallization are investigated. The Al$_2$O$_3$/GaN-cap/AlGaN/GaN interface is characterized using multifrequency capacitance–voltage ($C$–$V$) measurements from which the $D_{it}$ is determined. The combination of the O$_2$ plasma-based surface treatment and N$_2$ annealing is shown to reduce the frequency-dispersion in the $C$–$V$ curves which indicates a better Al$_2$O$_3$/III-nitride interface quality with reduced $D_{it}$ in the range of...
2 × 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}. The effectiveness of the O_2 plasma-based surface treatment and N_2 annealing is then demonstrated and discussed in AlGaN/GaN MIS-HEMTs using ALD-Al_2O_3 as gate dielectric by positive gate stress pulsed measurements which show improved $V_{th}$ stability.

2. Experimental Section

Figure 1 schematically shows the fabrication scheme and reference structures used in this work. The microfabrication is performed by contact lithography on a GaN-capped Al_{0.25}Ga_{0.75}N/GaN-2DEG heterostructure grown by metal organic chemical vapor deposition (MOCVD) on a silicon (111) substrate. The Al_{0.25}Ga_{0.75}N barrier thickness is 22 nm. First, isolation of the structures is obtained by Cl_2-based dry etching process assisted by inductively coupled plasma (ICP). Afterward ohmic contacts are formed using an evaporated Ti/Al/Ni/Au metal stack by lift-off technology and subsequent rapid thermal annealing (RTA) in N_2 ambient at 850 °C for 30 s. The gate structuring is then carried out using a 16 nm-thick Al_2O_3 deposited by thermal ALD as gate dielectric, followed by evaporation and lift-off of a Ti/Au gate electrode. Details of the ALD process conditions are reported in a previous study.\[27\] For this study, a surface preconditioning (SPC) treatment is applied before the Al_2O_3 deposition to the GaN surface which consists of a sequence of low power (100 W) O_2 plasma treatment for 90 s at 100 °C followed by HCl wet treatment for 1 min. In addition, a postmetallization anneal (PMA) is carried out after gate electrode formation in N_2 ambient at 350 °C for 10 min. The influence of both SPC and PMA on the Al_2O_3/III-nitride interface quality in MIS diodes (Figure 1a) and on the threshold voltage stability in MIS-HEMTs (Figure 1b) is investigated by multifrequency capacitance–voltage measurements and positive gate-stress pulsed sweep measurements, respectively. Capacitance–voltage ($C$–$V$) and pulsed current–voltage ($I$–$V$) measurements are carried out using an Agilent B1505A Power Device Analyzer. The GaN surface morphology before and after SPC is investigated by atomic force microscopy (AFM).

3. Results and Discussion

3.1. Surface Preconditioning

Figure 2a shows the AFM image of the as-grown MOCVD GaN-capped AlGaN/GaN heterostructure surface which shows the typical smooth surface with terraces of mono- or bilayer high step edges.\[10\] Pits at the step edge terminations which are associated to dislocations are also visible. As comparison, the GaN surface of a sample after ohmic contacts patterning, organic wet cleaning and subsequent annealing is shown in Figure 2b. The surface morphology appears rough and covered by particles which is attributed to a partial surface contamination and decomposition after lift-off and to the high temperature annealing for the ohmic contact formation. As the optimization of the device performance depends on the surface condition especially before the ALD-Al_2O_3 dielectric deposition, it is very important to obtain a clean surface by removing contaminants without damaging the crystal order or introducing additional defect states. For this purpose, an SPC consisting of a partial surface oxidation by O_2 plasma and a subsequent wet cleaning by HCl is applied to the GaN surface after ohmic contact formation. Figure 2c shows that the SPC is effective in removing contaminants and restoring
the flat step-like terrace structure of the surface resulting in a template similar to the usual as-grown GaN surface (Figure 2a). In the next sections, the impact of the SPC on the electrical properties of the Al2O3/III-nitride interface in MIS diodes and MIS-HEMTs is investigated.

3.2. C–V Characteristics of ALD-Al2O3 MIS Structures

The ideal C–V characteristic of an Al2O3/GaN-cap/AlGaN/GaN diode consists of a double-step curve which is a typical feature of a metal–insulator–heterostructure with a double-interface structure (Al2O3/GaN and AlGaN/GaN), as shown in Figure 3.[6,7] In the subthreshold region (below Vth) the 2DEG is depopulated and the capacitance is very small. Near Vth a rapid change in the capacitance starts to occur due to the electron population of the 2DEG at the AlGaN/GaN interface. In this region, the capacitance is almost bias independent and is given by the series capacitance of the AlGaN, GaN-cap, and Al2O3 layers. By applying a positive bias, electrons start to overcome the AlGaN barrier layer and accumulate at the Al2O3/GaN interface resulting in a second step in the C–V characteristic. This region is referred to as spill-over regime and its onset voltage is here indicated as Vspill-over. The capacitance value of the flat part in the spill-over region is given by CAl2O3. The ideal C–V behavior is modified when interface trap states are present at the Al2O3/GaN interface.[6,7,28] In the spill-over region, once electrons are trapped at the interface the negatively charged states screen the gate electric field resulting in a shift of Vspill-over toward the positive bias direction. Second, they lead to a drastic decrease in the C–V slope of the second step due the dependence of the traps occupancy as a function of the gate voltage. A schematic illustration of the conduction band diagram of an Al2O3/GaN/AlGaN/GaN structure at zero bias applied compared with the spill-over case is shown in Figure 3. In case of very high interface state densities, the second step might not be visible even at very high positive bias voltages due to a large positive shift of Vspill-over which cannot be detected due to the increase in leakage currents. On the contrary, near threshold voltage the trap occupancy of Dth does not depend on the gate voltage and results in a parallel shift of the corresponding C–V step without any stretch out.[29]

The experimental C–V characteristics of Al2O3/GaN-cap/AlGaN/GaN diodes with 16 nm thick Al2O3 in the cases that no treatment is applied, with SPC and with the combination of both SPC and PMA are shown in Figure 4. The first flat part in the C–V curves is in accordance with the described capacitance model considering 22, 2, and 16 nm of AlGaN, GaN, and Al2O3, respectively. However, in the case no treatment is applied, the second step is instead not visible in the voltage range considered because the amount of interface traps is probably so large that the second step is shifted beyond 4 V, after which the leakage current becomes too large to perform accurate measurement. Conversely, the typical double-step C–V curves are observed in the case of samples treated by SPC and SPC combined with PMA. By applying only the SPC, even though the presence of the second step indicates a reduced amount of interface states compared with the untreated case, as shown in Figure 4, the ideal value of CAl2O3 is not reached because of a large amount of traps still present at the interface causing a stretch out of the C–V curve. When the PMA is applied in combination with the SPC, the change of the capacitance of the second step becomes

Figure 4. C–V characteristics of Al2O3/GaN/AlGaN/GaN diodes having 16 nm-thick Al2O3 without treatment applied (black rectangle), after SPC (blue circle) and SPC combined with PMA (green triangle). The DC voltage sweep starts at −10 V. The AC signal frequency is 1 kHz with 30 mV amplitude.

Figure 3. Schematic conduction band diagram (not to scale) of the GaN-capped AlGaN/GaN heterostructure with Al2O3 as gate dielectric at a) zero bias (Vc = 0 V) and b) under forward bias in the spill-over regime (Vc ≥ Vspill-over). Electrons can overcome the AlGaN barrier from the 2DEG channel and be trapped in the states located at the Al2O3/GaN interface. Ef denotes the Fermi energy at 0 V gate voltage.
very steep by reaching the ideal value \( C_{AlO_2} \) and a slight shift of \( V_{spill-over} \) toward 0 V is also visible. This is a qualitative indication of the effectiveness of SPC combined with PMA to improve the interface quality by reducing the amount of traps at the Al\(_2\)O\(_3\)/GaN interface.

### 3.3. \( D_n \) Extraction Using Frequency Dispersion in C–V Characteristics

The extraction of \( D_n \) in MIS-HEMT structures is challenging due to the presence of two interfaces which complicates the potential distribution over the structure and a low emission rate of electrons in the wide bandgap semiconductor.\(^{[31]}\)\(^{[39]}\) The conventional conductance method may lead to an underestimation of \( D_n \) due to the presence of the additional capacitance introduced by the AlGaN barrier.\(^{[31]}\) As Yang et al. reported,\(^{[31]}\) the frequency-dependent C–V method is a better technique to map the interface traps at the dielectric/III-nitride interface, and it is used in our study to determine the interface trap density \( D_n \).

In particular, the interface trap analysis is carried out using the frequency dispersion of the C–V characteristics in the spill-over region of the Al\(_2\)O\(_3\)/GaN/AlGaN/GaN diode structures. In forward bias region, \( E_F \) is moving upward toward the conduction band at the Al\(_2\)O\(_3\)/GaN interface and its energy position is defined by the voltage applied (Figure 3). Once \( E_F \) is located at a certain energy position, the only electrons which can respond to the alternate current (AC) signal and be detected are the ones which are trapped and re-emitted from trap states with an emission time \( \tau_e \) smaller compared with the period \( \tau \) related to the frequency of the AC signal (\( \tau_e < \tau \)). The emission time constant for a trap level using the Shockley–Read–Hall statistics is

\[
\tau_e = \frac{1}{N_{C} \sigma \exp \left( \frac{E_C - E_T}{k_B T} \right)} \tag{1}
\]

where \( N_{C} \), \( \sigma \), \( E_C \), \( E_T \), \( k_B \), and \( T \) are the effective density of states in the conduction band, the thermal velocity, the capture cross section of the trap, the conduction band minimum, the trap energy, the Boltzmann constant, and the temperature, respectively. The period of the AC signal is given by

\[
\tau = \frac{1}{2\pi f} \tag{2}
\]

where \( f \) is the frequency of the AC signal. Combining Equation (1) and (2), the maximum trap energy depth \( E_{TF} \) with respect to \( E_C \) which can be probed by a certain frequency \( f \) can be deduced as

\[
E_C - E_{TF} = k_B T \ln \left( \frac{N_{C} \sigma}{2\pi f} \right) \tag{3}
\]

At a certain frequency \( f \), only charged trap states (depending on the position of \( E_F \)) which are in the energy range between \( E_C \) and \( E_{TF} \) contribute to the capacitance and lead to the onset of spill-over at \( V_{spill-over} \) in the C–V characteristic. Higher frequencies can therefore only probe energetically shallow states and lead to a positive shift of \( V_{spill-over} \) because a higher voltage is required to raise \( E_F \) towards \( E_C \). As a consequence, a smaller-frequency dispersion indicates a reduction of the interface state density.\(^{[6,31]}\)

In addition, a \( D_n-E_F \) energy map can be obtained using the voltage shift of the second step in the C–V curves using the following equation\(^{[31]}\)

\[
D_n(E_C - E_T) = D_n \left( E_C - \frac{E_{TF1} + E_{TF2}}{2} \right) = \frac{C_{AlO_2}}{q \Delta V_{TF1,TF2}} \tag{4}
\]

with

\[
\Delta V_{TF1,TF2} = \frac{C_{AlGaN}}{C_{AlGaN} + C_{AlO_2}} \Delta V_{TF1,TF2} \tag{5}
\]

where \( C_{AlGaN} \) and \( C_{AlO_2} \) are the capacitance values of the AlGaN and Al\(_2\)O\(_3\) layers determined by their physical thicknesses, \( q \) is the elementary charge, and \( \Delta V_{TF1,TF2} \) is the voltage shift in the second step between C–V curves at frequencies \( f_1 \) and \( f_2 \). \( \Delta V_{TF1,TF2} \) is determined at the midpoint of the capacitance in the second step of the C–V characteristics. Using Equation (3), the difference between \( E_{TF1} \) and \( E_{TF2} \) is instead given by

\[
E_{TF1} - E_{TF2} = k_B T \ln \left( \frac{f_1}{f_2} \right) \tag{6}
\]

In Figure 5, C–V curves with frequencies ranging from 1 kHz to 1 MHz are shown in the cases of no treatment applied, with SPC and with the combination of both SPC and PMA. In this case the bias voltage is swept from positive to negative direction to initiate each measurement in a defined state of maximum electron trapping. Note here that as shown from the comparison of the C–V characteristics measured at 1 kHz of Figure 4 and 5, the latter condition leads to a rigid shift toward positive direction of the C–V curve due to electrons trapped in deep energy states which are not re-emitted during the measurement time.
Figure 5 shows that in the untreated case the second step is still not visible at all frequencies. Conversely, different frequency dispersions are obtained in the other two cases with a smaller frequency dispersion in the case of the combination of SPC and PMA. A smaller $V_{\text{spill-over}}$ and a steeper $C-V$ slope are also revealed which indicates a reduction of the trap states at the $\text{Al}_2\text{O}_3/\text{GaN}$ interface.

Figure 6 shows $D_{\alpha}$-$E_T$ mapping in the $\text{Al}_2\text{O}_3/\text{GaN}/\text{AlGaN}/\text{GaN}$ diodes after SPC (blue circles) and SPC combined with PMA (green triangles).

3.4. Pulsed $I_{\text{DS}}$-$V_{\text{GS}}$ Measurements

For a comprehensive study, pulsed $I_{\text{DS}}$-$V_{\text{GS}}$ sweep measurements of $\text{Al}_2\text{O}_3/\text{GaN}/\text{AlGaN}/\text{GaN}$ MIS-HEMTs fabricated on the same samples as the capacitive test structures are carried out to investigate $V_{\text{th}}$ instability and for trap state analysis under positive gate stress condition.\textsuperscript{[8,11,12]} The measurement consists of a stress phase during which a positive voltage ($V_{\text{GS, stress}}$) is applied to the gate, whereas source and drain are kept at $0$ V ($V_{\text{DS, stress}}$) to ensure that trapping mainly occurs at the $\text{Al}_2\text{O}_3/\text{GaN}$ interface.\textsuperscript{[9]} In between each stress phase, short measurement pulses are applied to minimize detrapping from interface states consisting of a gate pulse of increasing height $V_{\text{GS}}$ and a low drain-source pulse $V_{\text{DS}}$. A low $V_{\text{DS}}$ is used to reduce field-assisted detrapping of the interface states.

Figure 7 shows the pulsed transfer characteristics of the $\text{Al}_2\text{O}_3/\text{GaN}/\text{AlGaN}/\text{GaN}$ MIS-HEMTs fabricated without and with SPC and PMA. The measurements are obtained by sweeping $V_{\text{GS}}$ from $-10$ to $0$ V at $V_{\text{DS}} = 1$ V for gate stress voltages $V_{\text{GS, stress}}$ from $0$ to $4$ V and $V_{\text{DS, stress}} = 0$ V. The pulse period and pulse width are 50 and 1 ms, respectively, with 1 ms being the time limit of the measurement system. It is observed that the $V_{\text{th}}$ stability of the MIS-HEMTs improves for the devices fabricated by applying the SPC and PMA treatments. To better visualize the effectiveness of the treatments, Figure 8 shows the threshold voltage shift $\Delta V_{\text{th}}$ as a function of the gate bias stress applied. Although the $V_{\text{th}}$ drifts in the positive direction for larger positive gate bias stress in all samples, the amplitude of the $V_{\text{th}}$ shift is significantly reduced in case of the MIS-HEMT treated by SPC and PMA. It is important to note here that the contribution of the interface traps to the $V_{\text{th}}$ shift obtained using pulsed $I_{\text{DS}}$-$V_{\text{GS}}$ sweep measurements only reflects the occupancy of traps with an emission time $\tau_e$ longer than the measurement pulse width. In fact, interface traps with emission time constants shorter than the pulse width are able to emit electrons before the sampling and cannot be detected using this method. The upper energy range limit which is detectable can be deduced from Equation (1) by considering...
the measurement pulse width of 1 ms and it is calculated to be $E_C - E_F \geq 0.5 \text{ eV}$. Therefore, the obtained pulsed $I_{DS}-V_{GS}$ measurements are sensitive to deeper interface states in energy compared with the frequency-dependent $C-V$ method. In addition, the $V_{th}$ shift obtained after positive bias stress is not only correlated to interface traps but also to border traps as already reported.\cite{10} In fact, during the stress time both interface states and border traps can be filled and can contribute to the $V_{th}$ instability due to their longer emission time. Even though the separate contributions of border and interface traps cannot be disentangled, an effective interface charge density accounting for $D_n$ and border traps can be determined by

$$n_{th} = \frac{C_{Al,O}}{q} \Delta V_{th} \quad (7)$$

The $n_{th}$ as a function of the gate stress voltage is also shown in Figure 8 which portrays a reduction of border and interface states for samples fabricated by combining SPC and PMA treatments. The effectiveness of the SPC and PMA treatments to reduce interface states at the Al$_2$O$_3$/III-nitride interface revealed by the frequency-dependent $C-V$ method is also demonstrated by the smaller relative change with increasing gate bias stress in pulsed $I_{DS}-V_{GS}$ to contribute to the improvement of the electrical properties of the GaN-based MIS-HEMTs under forward gate bias stress.

4. Conclusion

In summary, high-quality interface in terms of interface trap states between ALD-Al$_2$O$_3$ and GaN-capped AlGaN/GaN heterostructures have been achieved by the combination of an O$_2$ plasma-based surface preconditioning and N$_2$ postmetallization anneal. The O$_2$ plasma-based treatment has been shown to effectively restore the morphology of the GaN surface which is affected by the fabrication processes before the ALD-Al$_2$O$_3$ deposition. Moreover, MIS diodes treated by SPC and PMA showed a smaller-frequency dispersion of the $C-V$ characteristics than the samples without treatment or only SPC applied which indicates a reduction of interface trap states. The $D_n$ was estimated to be reduced to a value in the order of $2 \times 10^{12}$ cm$^{-2}$ eV$^{-1}$ near the conduction band edge. The reduction of interface trap states was also shown to improve the electrical properties of MIS-HEMTs which showed a better $V_{th}$ stability in pulsed $I_{DS}-V_{GS}$ sweep measurements.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

AlGaN/GaN, dielectric/III-nitride interfaces, interface traps, metal-insulator–semiconductor high electron mobility transistors, $V_{th}$ instability

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