Proximity Effect Transfer from NbTi into a Semiconductor Heterostructure via Epitaxial Aluminum

A. C. C. Drachmann,1 H. J. Suominen,1 M. Kjaergaard,1 B. Shojaei,2 C. J. Palmstrøm,2,3 C. M. Marcus,1 and F. Nichele1

1 Center for Quantum Devices and Station Q Copenhagen, Niels Bohr Institute University of Copenhagen, Universitetsparken 5, 2100 Copenhagen, Denmark
2 Materials Department, University of California, Santa Barbara, CA 93106, USA
3 Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106, USA

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We demonstrate the transfer of the superconducting properties of NbTi—a large-gap high-critical-field superconductor—into an InAs heterostructure via a thin intermediate layer of epitaxial Al. Two device geometries, a Josephson junction and a gate-defined quantum point contact, are used to characterize interface transparency and the two-step proximity effect. In the Josephson junction, multiple Andreev reflection reveal near-unity transparency, with an induced gap \( \Delta^* = 0.50 \text{ meV} \) and a critical temperature of 7.8 K. Tunneling spectroscopy yields a hard induced gap in the InAs 2DEG adjacent to the superconductor of \( \Delta^* = 0.43 \text{ meV} \) with substructure characteristic of both Al and NbTi.

Intimate coupling between semiconductors (Sm) and superconductors (S) gives rise to novel applications of superconducting electronics [1], as well as superconducting qubits [2] and new topological states of matter [3]. A critical building block for S/Sm hybrids system is a transparent interface, ensuring high probability of Andreev reflection [4, 5]. However, obtaining a transparent S/Sm interface has been a technological challenge for decades [6–9]. Recent work has largely resolved the interface problem by realizing epitaxial growth of Al on InAs via molecular beam epitaxy (MBE), both for nanowires [10, 11] and, more recently, for two-dimensional electron gases (2DEGs) [12], which are better suited for realizing complex, branched devices [3]. Focusing on InAs 2DEGs with epitaxial Al, high interface transparency and a hard induced superconductive gap \( \Delta^* = 0.18 \text{ meV} \) have been measured both by tunneling spectroscopy via a S-quantum point contact (QPC)-Sm junction [13] and by analysis of multiple Andreev reflection (MAR) in a S-Sm-S junction [14].

Despite its modest superconducting gap, critical temperature and critical magnetic field, Al has been the material of choice for Sm-S epitaxy to date because it is present in conventional III-V MBE systems and is compatible with standard fabrication recipes. In situ deposition (without breaking vacuum) or direct epitaxial growth of larger gap superconductors has proven challenging and requires dedicated growth systems. As an alternative, we demonstrate in this work the transfer of large-gap properties of NbTi via the proximity effect through a thin epitaxial Al layer into an InAs 2DEG.

Starting from an InAs heterostructure with epitaxial Al, we pattern ex situ a NbTi-based superconductive layer using standard lithographic techniques. The NbTi layer enhances the Al gap by the proximity effect [15, 16], which in turn results in an enhanced induced gap in the InAs 2DEG. As the processing only involves the topmost Al surface, the high transparency of the epitaxial InAs/Al interface is not affected. As discussed below, the induced gap in the InAs 2DEG is found to be more than twice as large as both the induced gap using Al alone [13] and the gap of the Al itself. The method can be extended to other choices of top-layer superconductor [15].

We investigate two device geometries, an S-Sm-S Josephson junction and a S-QPC-Sm junction. The S-Sm-S device shows pronounced MAR features, indicating high transparency, and we extract an induced gap, \( \Delta^* = 0.50 \text{ meV} \) and a critical temperature, \( T_c = 7.7 \text{ K} \), with the zero resistance state across the junction persisting up to 3.7 K. Tunnel spectroscopy in the S-QPC-Sm device yields an induced gap of 0.43 meV and a hardness of the induced gap (measured by a sub-gap conductance suppression in the tunnel regime) comparable to the theoretical limit for S/Sm junctions [17]. Tunnel spectroscopy in a magnetic field reveals a gap closing at a critical in-plane field value of \( B_{\|,c} \sim 750 \text{ mT} \), a value 2.5 times larger than in similar systems without NbTi [18].

The InAs heterostructure, grown on an undoped GaSb wafer along the [001] crystallographic direction, is shown in Fig. [1a]. The active region is similar to previous studies [12], but with a nominal 25 nm epitaxial Al layer, instead of the 10 nm Al layer used previously. Thicker Al allowed this layer to be thinned during fabrication without risking etching down to the interface, as discussed below. Transport measurements in a Hall bar with the Al removed were used to extract a mobility of 10,000 cm²/Vs at a density of 1 × 10¹² cm⁻².

Critical fabrication steps are outlined in Fig. [1b], with full details given in the Supplemental Material [18]. First, areas for NbTi deposition are patterned using electron-beam lithography. Inside the deposition chamber, the
native oxide on Al is removed using Kaufman Ar milling, followed immediately by evaporating Ti and sputtering NbTi/NbTiN without breaking vacuum, as shown in Fig. 1(c). The Ti bottom layer promotes adhesion and the NbTiN top layer prevents subsequent oxidation. Following liftoff, the patterned NbTi forms a self-aligned mask for a selective Al etch. (c) The NbTi stack includes a Ti layer to promote adhesion and a NbTiN capping to prevent oxidation. (d) False-color electron micrograph of an S-Sm-S device after the Al etch similar to the sample measured. (e) False-color electron micrograph of the finished S-QPC-Sm device.

The induced gap under the superconducting leads and the interface transparency can be extracted from MAR measurements in the S-Sm-S junction. As discussed in Ref. 14, a characteristic feature of InAs/epitaxial Al Josephson junction is that sub-gap MAR features appear as peaks in resistance rather than in conductance, a consequence of the high S/Sm interface transparency. Differential resistance \( dV/dI \) as a function of DC bias \( I_{DC} \) at various temperatures is shown in Fig. 2(a). At base temperature, the critical current, \( I_C = 7.5 \mu A \), with normal-state resistance \( R_N = 53 \Omega \) reached at \( I_{DC} = 45 \mu A \). The \( I_C R_N \) product was 0.40 meV and critical current density was 1.74 \( \mu A/\mu m \), both considerably larger than that measured S-Sm-S junctions with epitaxial Al alone 14.

As seen in Fig. 2(b) the junction remains in the zero-resistance state up to 3.7 K, above which resistance increases up to a plateau at 53 \( \Omega \), which we interpret as the normal-state resistance of the junction. The sharp transition at 7.7 K is associated with the critical temperature of the NbTi contacts. The differential resistance displays pronounced MAR features, appearing as sharp peaks in resistance [or dips in conductance, see Fig. 2(c)].

From the MAR relation \( eV = 2\Delta^*/\Delta_{MAR} \), a linear fit of the inverse MAR index \( 1/\Delta_{MAR} \) as a function of the voltage bias \( V \), [Fig. 2(c) inset] yields a base temperature induced gap \( \Delta^* = 0.51 \) meV. Repeating the procedure over a range of temperatures yields \( \Delta^*(T) \), shown in Fig. 2(d) along with a fit to the BCS form 22.

\[
\Delta^*(T) = \Delta^*(0) \tanh \left( \frac{1}{2} \sqrt{\frac{T_c}{T} - 1} \right),
\]

giving \( \Delta^*(0) = 0.50 \) meV and \( T_c = 7.8 \) K as fit parameters. Experimental data and the BCS fit are in good agreement.

A requirement for the use of S/Sm devices for certain applications, including topological quantum computing, is the absence of sub-gap states, reflected in a small sub-gap conductance. Using the approach of Ref. 10, 13, 23, 24.
we measured electron tunneling near the S/Sm interface using a gate-defined QPC fabricated on top of an ALD oxide. A false colored SEM of the device is shown on Fig. 1(e).

Figure 2(a) shows the differential conductance $dI/dV$ as a function of source-drain bias $V_{SD}$ where the gates are energized to set the QPC in the tunneling regime. In this case, the differential conductance maps the local density of states, allowing the induced gap $\Delta^*$ at the position of the QPC to be directly measured. Defining $2\Delta^*$ as the peak to peak separation gives $\Delta^* = 0.43$ meV, as shown in Fig. 2(a), similar to the value measured via MAR. In addition to the large energy gap—a factor $\sim 2.3$ larger than the Al-only case [13]—the hardness of the gap at zero energy is not affected by the additional fabrication. To demonstrate this, we measure similar curves as Fig. 2(a) for different values of out-of-gap conductance, which result in varying in-gap conductance, and produce the parametric plot of Fig. 2(b) (markers). These data are compared to theory of a single mode S/Sm interface [17],

$$G_{ns} = 2G_0 - \frac{G_{nn}^2}{(2G_0 - G_{nn})^2},$$

with no fit parameters.

Here $G_{ns}$ is the conductance in the superconducting regime, $G_{nn}$ is the normal state conductance (measured at high source drain bias) and $G_0 = 2e^2/h$ is the conductance quantum. The agreement is remarkable up to four order of magnitude, demonstrating our devices operate in the theoretical limit of low in-gap conductance.

The complete data set is presented in the Supplemental Material [18].

In order to drive the system in the topological regime, a necessary condition is that the Zeeman splitting in InAs, $g_{\text{InAs}}\mu_B B$, exceeds $\Delta^*$ while the parent superconductor remains gapped. Previous measurements on InAs/Al heterostructures showed a gap closing at in-plane fields $B_{||} \sim 300$ mT, compatible with $g_{\text{InAs}} \sim 10$, a reasonable value for InAs [13]. Similar measurements presented in Fig. 4(a,b) indicate a gap closing for in-plane magnetic fields $B_{||,c} \sim 750$ mT, consistent with an induced gap 2.3 times larger than experiments with epitaxial Al. We note that gap closing is not linked to the quenching of superconductivity in the parent superconductor as NbTi can sustain much larger fields than those used here. A different situation is observed when the field is applied out-of-plane, as shown in Fig. 4(c,d). In this case the most prominent effect is not a gap closing (the $\pm \Delta^*$ peaks do not approach zero), but rather a gap softening above 100 mT that makes the gap indistinguishable.
from the background. We interpret the softening as due to dephasing of Andreev pairs in the presence of vortices penetrating the S/Sm stack in a large out-of-plane fields [22].

The possibility to locally control the induced gap (and critical field) in the Sm by combining regions with only epitaxial Al or with NbTi/Al stacks allows the realization of complex devices required for future studies of topological states of matter [23]. For example, NbTi could be used to realize superconductive leads that persist in the trivial regime while one dimensional devices, proximitized by epitaxial Al only, undergo the topological transition.

In summary, we have demonstrated a method for obtaining a S/Sm heterostructure with high interface transparency and a large, controllable induced gap. The processing is based on MBE grown InAs/Al heterostructures and ex-situ deposition of a large-gap superconductor. The technique does not compromise the epitaxial interface and so should be compatible with a variety of materials and processing technologies. Our results suggest a path toward semiconductor-superconductor electronics, both conventional and topological, operating in the temperature range of liquid helium or pulse tube coolers.

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[1] H. Weinstock and R. W. Ralston, *The New Superconducting Electronics* (Kluwer Academic Publishers, 1993) p. 457.
[2] J. Clarke and F. K. Wilhelm, *Phys. World* **17**, 29 (2004).
[3] J. Alicea, Y. Oreg, G. Refael, F. von Oppen, and M. P. a. Fisher, *Nat. Phys.* **7**, 412 (2011).
[4] M. Leijnse and K. Flensberg, *Phys. Rev. Lett.* **107**, 1 (2011).
[5] G. E. Blonder, M. Tinkham, and T. M. Klapwijk, *Phys. Rev. B* **25**, 4515 (1982).
[6] P. Octavio, M. Tinkham, G. E. Blonder, and T. M. Klapwijk, *Phys. Rev. B* **27**, 6739 (1983).
[7] M. Amado, A. Fornieri, F. Carillo, G. Biasiol, L. Sorba, V. Pellegrini, and F. Giazotto, *Phys. Rev. B* **87**, 1 (2013).
[8] Z. Wan, A. Kazakov, M. J. Manfra, L. N. Pfeiffer, K. W. West, and L. P. Rokhinson, *Nat. Commun.* **6**, 7426 (2015).
[9] H. Takayanagi and T. Akazaki, *Phys. Rev. B* **52**, 8633 (1995).
[10] W. Chang, S. M. Albrecht, T. S. Jespersen, F. Kuemmeth, P. Kroghstrup, J. Nygård, and C. M. Marcus, *Nat. Nanotechnol.* **10**, 232 (2015).
[11] P. Kroghstrup, N. L. B. Ziino, W. Chang, S. M. Albrecht, M. H. Madsen, E. Johnson, J. Nygård, C. M. Marcus, and T. S. Jespersen, *Nat. Mater.* **14**, 400 (2015).
[12] J. Shabani, M. Kjaergaard, H. J. Suominen, Y. Kim, F. Nichele, P. K. Pakrouski, T. Stankevic, R. M. Lutchyn, P. Kroghstrup, R. Feidenhans’l, S. Kraemmer, C. Nayak, M. Troyer, C. M. Marcus, and C. J. Palmström, *Phys. Rev. B* **93** (2016).
[13] M. Kjaergaard, F. Nichele, H. J. Suominen, M. P. Nowak, M. Wimmer, A. R. Akhmerov, J. A. Folk, K. Flensberg, J. Shabani, C. J. Palmström, and C. M. Marcus, *Nat. Commun.* **7**, 12841 (2016).
[14] M. Kjaergaard, H. J. Suominen, M. P. Nowak, A. R. Akhmerov, J. Shabani, C. J. Palmström, F. Nichele, and C. M. Marcus, *ArXiv e-prints* (2016), arXiv:1607.04164 [cond-mat.mes-hall].
[15] G. Brammertz, a. Golubov, a. Peacock, P. Verhoeve, D. Goldie, and R. Venn, *Physica C* **350**, 227 (2001).
[16] V. Cherkez, J. C. Cuevas, C. Brun, T. Cren, G. Ménard, F. Debontridder, V. S. Stolyarov, and D. Roditchev, *Phys. Rev. X* **4**, 1 (2014).
[17] C. W. J. Beenakker, *Phys. Rev. B* **46**, 841 (1992).
[18] See Supplemental Material at [URL] for material and methods and presentation of additional measurements.
[19] Image is taken before etching, ALD and gate deposition.
[20] K. Flensberg, J. B. Hansen, and M. Octavio, *Phys. Rev. B* **38**, 8707 (1988).
[21] A. Chrestin, T. Matsuyama, and U. Merkt, *Phys. Rev. B* **55**, 8457 (1997).
[22] M. Tinkham, *Introduction to Superconductivity*, 2nd ed. (McGraw-Hill Book Co., New York, 1996) p. 454.
[23] D. Aasen, M. Hell, R. V. Mishmash, A. Higginbotham, J. Danon, M. Leijnse, T. S. Jespersen, J. A. Folk, C. M. Marcus, K. Flensberg, and J. Alicea, *Phys. Rev. X* **6**, 031016 (2016).
SUPPLEMENTAL MATERIAL

This supplemental Material Section describes the experimental procedures used to fabricate the devices presented in the main text and presents additional electrical measurements.

FABRICATION TECHNIQUES

Here we present detailed information on the fabrication of the reported devices. All patterning was done by e-beam lithography and unless otherwise stated, standard PMMA resist was used. To reduce exposure time, all designs were divided into inner structures with small beam current and outer structures with larger beam current.

To enable alignment of consecutive exposures, alignment marks are made from a Ti/Au (5/100 nm) deposition. The marks are placed near the edge, all around the 2.5×5 mm² chip.

Argon Milling and NbTi deposition

Starting from the blank chip with alignment markers, we spin coat an MMA/CZAR resist bilayer. The choice of this resist stack is particularly important for a successful Ar etching and deposition step. In particular, the bottom MMA layer provides a sizable undercut to facilitate the lift-off of closely spaced contacts while the CZAR layer can sustain prolonged Ar milling times.

Argon Milling is used to remove the native oxide that forms on the epitaxial Al upon exposure to air, allowing the NbTi to directly contact the metallic Al. For this step we used a Kaufman ion source installed in the superconductor deposition chamber. The etching was performed with a beam voltage of 600 V, an acceleration voltage of 120 V, an Ar-flow of 30 sccm at 1 mTorr pressure and with a rotating sample plate. The desired etching depth in the epitaxial Al is between 10 and 20 nm.

The etching rate of Kaufman source can fluctuate over long periods of time, requiring a fine tuning of the etching time prior to each run. In order to reduce the consumption of epitaxial material, two distinct etching rate calibrations was performed on Si chips with thermally grown SiO₂ layer. We found that etching 24.5 nm of SiO₂ resulted in an optimal etch depth in the epitaxial Al layer. The etching depth was measured with an optical profilometer for epitaxial Al and a spectral reflectometer for SiO₂. For every etching session, the Kaufman filament was heated by a 10 minutes milling of an empty sample plate. The sample was subsequently loaded in the deposition chamber and two more minutes of milling were performed on a closed sample shutter before allowing the Ar ions to reach the sample. The samples presented in the Main Text were etched 3 min and 31 sec.

Immediately after Ar etching the superconductive Ti/NbTi/NbTiN stack is deposited in the same chamber. First 2 nm of Ti are e-beam evaporated to ensure good contact between NbTi and Al. Second, 60 nm of NbTi are deposited from a Nb2/3 Ti1/3 sputter target with a beam power of 200 W in a 4 mTorr pressure with an Ar gas flow rate of 50 sccm, resulting in a deposition rate of 10 nm min⁻¹. When the desired NbTi deposition is terminated, the sample shutter is closed. Third, a N₂ flow of 6 sccm is let into the chamber and the shutter is opened again after 30 sec to deposit 5 nm of NbTiN. The sample is kept rotating during the entire deposition to ensure uniformity.

After deposition, the resist bilayer is lifted-off by immersion of the sample in dioxolane. Sputtering deposition on a undercut resist results in prominent sidewalls, high and narrow structures that can cause several problems during the remaining fabrication steps. Most sidewalls were removed by sonication during liftoff of the sputtered material.

The epitaxial Al wafers do not require specifically designed bonding pads, as low resistance (< 500 Ω) contacts can generally be obtained by directly bonding on the epitaxial Al. In the present case, however, the epitaxial Al covering the surface (and not protected by NbTi) will be removed in a subsequent step. For this reason it is important to deposit NbTi also on the bonding pads of the mesa structure.

Mesa Etching and Al etching

A new resist-pattern is defined for mesa etching on standard PMMA. After chemical development with MIBK:IPA 1:3, the chip is plasma ashed for 60 sec to remove possible resist leftovers. The etching is performed in two steps. First the epitaxial Al, that covers the entire surface of the wafer, must be removed. Second, the III/V semiconductor is etched to isolate different devices on the same chip. The epitaxial Al is removed by a 12 sec etching in 50 °C Transene Aluminum Etchant type D. The process is terminated first with 30 s stirring in 50 °C DI water and then 30 s stirring in room temperature DI water.

After blow drying the chip with nitrogen, the III-V is immediately etched by a prepared room temperature H2O:CH3H2O:6H3PO4:H2O2 (220:55:3:3) solution for 330 s, resulting in an etching dept of about 600 nm. The etching is stopped with stirring in room temperature DI water. The resist is lifted off with dioxolane, followed by washes in acetone and isopropanol. At this point the NbTi forms a self aligned mask that can be used for etching the epitaxial Al covering the mesas, so no further electron beam lithography step is needed. The Al etching step previously described is then repeated, but with no resist mask.
FIG. S.1. In-plane field dependence of the S-Sm-S. (a) Differential resistance $dV/dI$ as a function of source-drain current $I_{sd}$ and in-plane field $B_{||}$, applied perpendicular to the current flow. Colored squares show $B_{||}$-values at which line cuts in (b) are taken. These line cuts are not offset.

Atomic Layer Deposition of HfO$_2$ and gate deposition

Immediately after removing the unwanted epitaxial Al, the chip is transferred in an atomic layer deposition chamber for the growth of 50 nm HfO$_2$ as a gate insulator. To minimize the exposure of the uncovered III-V material to oxygen, a constant flow of 20 sccm of N$_2$ is maintained in the chamber at any stage, also during pumping down. HfO$_2$ is deposited by 500 cycles of Tetrakis(dimethylamido)hafnium pulse and 60 sec waiting time and water pulse and 60 sec waiting time preheated at 90 °C.

Top gate deposition is done in two steps, one for the fine features and the other for larger elements such as bonding pads. In Fig. 1(e) of the Main Text it is possible to distinguish the two depositions from their different metal height and surface roughness. The fine features are defined in a single PMMA layer by evaporation of 5 nm Ti/30 nm Au and lift-off. The larger features are defined in a MMA/PMMA bilayer and require the evaporation of 50 nm Ti/700 nm Au. In both cases the chips are plasma ashed for 60 s after development to remove eventual resist leftovers.

S-SM-S IN-PLANE FIELD DEPENDENCE

An in-plane field, perpendicular to the current direction, is applied on the S-Sm-S junction while measuring critical current $I_{C}$, see Fig. S.1. The vector-magnet was aligned before the measurement. Still $I_{C}$ is fluctuating at low fields, indicating flux jumps. These stabilizes at higher fields until the super-current dies out at $\sim$500 mT. The sweeps are taken going from negative to positive, causing heating effects in the negative current region giving rise to the visible asymmetry of $I_{C}$.

QPC CONDUCTANCE

Beenakker predicted in 1992 [17] that an Andreev-enhanced QPC, like the one reported in this work, should have $4e^2/h$ steps in conductance after pinch-off. This was observed in an InAs 2DEG with epitaxial Aluminum S-QPC-Sm junction [13]. Despite the reported S-QPC-Sm does not show clear step features, presumably for the lower electron mobility of the wafer used in this work, the first plateau fluctuates around $4e^2/h$ rather than $2e^2/h$, see figure. S.2.

Conductance in the tunneling regime

The parametric plot presented in Fig. 3(b) of the Main Text shows the QPC zero bias conductance as a function of the QPC high-bias conductance (which coincides with the normal state conductance up to experimental errors). The parametric plot was obtained from the measurement presented in Fig. S.3, showing the QPC conductance as a function of bias $V_{sd}$ and gate voltage $V_G$ close to pinch-off.

To accurately measure the sample conductance in the very low transmission regime, we used DC techniques only in a two-terminal configuration. A line resistance $R_{line} = 11.8k\Omega$ was determined in a four-terminal measurement at $V_G = -4.85$ V. Figure Fig. S.3 is obtained by numerical differentiation of the measured DC current as a function of $V_{sd}$. The voltage dropping on the QPC was calculated as $V_{eff} = V_{sd} - I_{DC}R_{line}$. The noise visible in Fig. S.3 is presumably due to a combination of the
differentiation method and intrinsic noise of the device, also noticed in AC measurements.
FIG. S.3. Numerically differentiated current $dI/dV$ vs source-drain voltage $V_{sd}$ for gate voltages $V_G$ close to pinch-off with the QPC.