A 97 fJ/Conversion Neuron-ADC with Reconfigurable Sampling and Static Power Reduction

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Abstract—A bio-inspired Neuron-ADC with reconfigurable sampling and static power reduction for biomedical applications is proposed in this work. The Neuron-ADC leverages level-crossing sampling and a bio-inspired refractory circuit to compressively converts bio-signal to digital spikes and information-of-interest. The proposed design can not only avoid dissipating ADC energy on unnecessary data but also achieve reconfigurable sampling, making it appropriate for either low power operation or high accuracy conversion when dealing with various kinds of bio-signals. Moreover, the proposed dynamic comparator can reduce static power up to 41.1\% when tested with a 10 kHz sinusoidal input. Simulation results of 40 nm CMOS process show that the Neuron-ADC achieves a maximum ENOB of 6.9 bits with a corresponding FoM of 97 fJ/conversion under 0.6 V supply voltage.

Index Terms—Analog-to-digital converter, Neuron-ADC, reconfigurable sampling, static power reduction, bio-signal recording

I. INTRODUCTION

With the development of biomedical technology and aging society, recent years have witnessed the rapid advance of bio-signal recording systems for personal healthcare. The conventional architecture of bio-signal recording system includes a pre-amplification stage. Then, the input signal is filtered and digitalized by SAR ADC, and sent to a wireless transmission module or signal processing engine for disease detection \cite{1}. Limited by the power budget of batteries and wireless power transmission, energy efficiency is critical to such systems. However, conventional system architectures adopt SAR ADC and Nyquist sampling, suffering from critical energy consumption issues. The highest frequency band of bio-signals determines the sampling frequency, which does not leverage bio-signals features and sparsity. A sparse bio-signal is repetitively sampled even during the silent signal period, thus wasting ADC power on needless data.

Recently, level-crossing ADC (LC-ADC) has been developed as a promising candidate for biomedical applications \cite{2}. It leverages signal sparsity and achieves event-driven sampling with lower average sampling rate. As presented in Fig. 1, the input signal is only sampled when predefined levels are crossed, thus saving ADC energy during the silent signal period and realizing data compression compared with Nyquist sampling. Moreover, LC-ADC is based on non-uniform sampling and time quantization, so it produces no aliasing at the output spectrum and is more suitable for low operation voltage and advanced nodes. Additionally, outputs of level-crossing sampling are inherently compatible with neuromorphic spiking neural networks, paving the way to neuromorphic recording and processing systems \cite{3}.

Prior architectures of LC-ADC suffer from several design drawbacks and performance issues. As shown in Fig. 2(a), the floating-window LC-ADC proposed in \cite{4} \cite{5} is composed of an n-bit DAC, two comparators, and a control logic module. This type of architecture needs complex DAC design that consumes high power. Moreover, circuit parameters and output data rate of this architecture are not reconfigurable and cannot be adapted to various bio-signals. The fixed-window LC-ADC illustrated in Fig. 2(b) reduces the energy consumption by utilizing a simple 1-bit capacitive DAC that generates a fixed range input to comparators \cite{6} \cite{7}. However, the sampling scheme and output data rate are still not reconfigurable. What’s worse, high static power of comparators dominates the power budget and is independent of input signal activity, which
counters advantages of event-driven sampling.

To solve the aforementioned issues, this work proposes a Neuron-ADC with reconfigurable sampling and static power reduction for biomedical applications. The proposed Neuron-ADC receives inputs of various bio-signals, and produces digital spike outputs with refractory period similar to biological neurons. As shown in Fig. 3(a), it is based on the fixed-window LC-ADC architecture. The main contributions are listed as follows:

- Propose a bio-inspired refractory circuit to achieve reconfigurable sampling.
- A charge-injection-free signal folding circuit is designed to perform as a 1-bit DAC.
- Dynamic comparators are utilized to reduce static power consumption.
- Simulation results under 40 nm CMOS process show that the Neuron-ADC achieves the ENOB up to 6.9 bits with a corresponding FoM of 97 fJ/conversion under 0.6 V supply voltage.

The rest of this paper is organized as follows. Section II introduces the system architecture of the proposed Neuron-ADC, followed by the circuit implementation in Section III. Section IV presents the simulation results. Finally, Section V concludes the paper.

II. SYSTEM ARCHITECTURE

The system architecture of the proposed Neuron-ADC is shown in Fig. 3(a). It includes a signal folding circuit, two dynamic comparators, and a bio-inspired refractory circuit. As illustrated in Fig. 3(b), no output is generated when input signal is between two levels of the fixed window, \( V_H \) and \( V_L \). When signal crossing happens, the input signal will be converted to two types of digital spike outputs, UP and DN, to represent up crossing and down crossing, respectively. Specifically, when the input signal passes through the predefined

III. CIRCUIT IMPLEMENTATION

A. Charge-Injection-Free Signal Folding Circuit

The signal folding circuit receives input analog signal and asynchronous clock signal from the bio-inspired refractory circuit. It produces a fixed range of output analog signal to be compared with reference voltage levels by the comparator. As shown in Fig. 4(a), a 1-bit capacitive DAC is used to implement the signal folding circuit in this design. Fig. 4(b) presents the timing diagram of the circuit. When it receives a clock signal produced by the refractory circuit, it will switch on the connection with \( V_M \), and thus fold the input signal to the value of \( V_M \) by charge redistribution. Then, the switch turns off, and the signal folding circuit continues to track the input signal. Two switches are used to deal with the asynchronous clock signals from up-crossing and down-crossing. Due to the fixed \( V_M \) connected with switches, charge injection is independent of input signals and converted to offsets that could be eliminated by proper calibration.

B. Dynamic Comparator with Static Power Reduction

Comparators are designed for comparing input signal with reference voltage levels to get digital decision output. Two dynamic comparators are used in Neuron-ADC to compare input signal with a high reference voltage level and a low reference voltage level, respectively. A 3-stage dynamic comparator
is utilized and presented in Fig. 5. A differential amplifier with PMOS input is exploited as the first stage, followed by one common source stage to increase gain performance and reduce the kickback noise. To achieve a rail-to-rail swing digital output, one inverter stage is employed at the output. Additionally, two power-gating PMOS transistors are added and controlled by the refractory circuit to turn off comparators during the signal folding process, which helps to reduce static power consumption.

C. Bio-Inspired Refractory Circuit

The bio-inspired refractory circuit is proposed to achieve reconfigurable sampling of Neuron-ADC. The refractory circuit is inspired by biological neurons and prior circuit implementations [8]. This is the first time the refractory circuit and level-crossing sampling are combined to achieve reconfigurable and compressive sampling. Fig. 6 shows the schematic and timing diagram of the bio-inspired refractory circuit. It includes a PMOS common source stage with an adjustable NMOS load connected with inverter buffers. By changing the refractory voltage of the NMOS load, the refractory circuit generates asynchronous clock signals with variable refractory period shown as CLK_UP/CLK_DN in Fig. 6(b). Low refractory voltage produces a long refractory period for the signal folding circuit, leading to a long signal folding time and reduced number of sampled data points. High refractory voltage works vice versa. Reconfigurable sampling is thus realized by changing the refractory voltage.

IV. SIMULATION RESULTS

The proposed Neuron-ADC is simulated using TSMC 40 nm CMOS process to evaluate its performance. The supply voltage of all circuit blocks is set to 0.6 V to reduce power consumption. The value of LSB is closely related to the power and operation condition of Neuron-ADC. LSB is calculated by

\[
LSB = \frac{A_{FS}}{2^M}
\]

where \(A_{FS}\) is the full-scale voltage range of input signal. \(M\) is the resolution bit of Neuron-ADC, producing \(2^M\) quantization levels. To balance the trade-off between power consumption and signal conversion linearity, \(V_H, V_M\) and \(V_L\) are set to 95 mV, 75 mV, and 55 mV, respectively. Therefore, 1 LSB is 20 mV. A sinusoidal signal ranging from 10 Hz to 10 kHz with 640 mV amplitude is used as the input. Fifth-order polynomial interpolation is performed in MATLAB to calculate the FFT and signal-to-noise-and-distortion ratio (SNDR) of the simulation results.

Fig. 7 presents the SNDR and power consumption as a function of input frequency from 10 Hz to 10 kHz. To have a fair comparison, the refractory voltage is 200 mV for each frequency point. As shown in Fig. 7(a), a higher input frequency typically leads to more power consumption because of high dynamic power. From 10 Hz to 50 Hz, the SNDR increases and peaks at 50 Hz input frequency, after which it decreases. For low input frequency, the SNDR is affected by the operation accuracy of the signal folding circuit and comparators. While for high input frequency, the overall loop delay of the Neuron-ADC limits the SNDR. It is worth mentioning that different refractory voltage results in different power consumption and SNDR given the same input frequency.

To demonstrate the reconfigurable sampling function of the Neuron-ADC, Fig. 8 illustrates the power consumption and number of output spikes as a function of refractory voltage given 10 kHz sinusoidal input. As illustrated in Fig. 8, the power consumption and number of output spikes both increase with refractory voltage. Reconfigurable sampling can be achieved by adjusting the value of refractory voltage, which offers a flexible option for circuit designers. If the major design target is low power consumption, a low refractory voltage is
### Table I

| Static Power Reduction of Comparators | Input Frequency (Hz) | Static Power (nW) | Reduction Percent |
|--------------------------------------|----------------------|-------------------|-------------------|
| W/O Reduction                        | 500                  | 9.8               | 14.8%             |
| With Reduction                       | 1000                 | 24.2              | 21.1%             |
|                                      | 2000                 | 27.5              | 26.6%             |
|                                      | 4000                 | 42.6              | 39.0%             |
|                                      | 10000                | 67.1              | 41.1%             |

* Refractory voltage is 100 mV.

### Table II

| Parameter                      | [2] | [4] | [9] |
|-------------------------------|-----|-----|-----|
| Technology (nm)               | 180 | 80  | 64  |
| Supply (V)                    | 0.35 | 0.8 | 0.6 |
| Gain (V/lin)                  | 1   | 1   | 1.5 |
| SNDR (dB)                     | 39.49 | 38.5 | 38.4 |
| ENOB (bit)                    | 6.2-6.7 | 6.1-6.8 | 6.3-6.9 |
| Power (nW)                    | 4.2-186 | 90-180 | 60-220 |
| FoM (fJ/conv.)                | 1400 | 103-343 | 610-22 |
| recon. samplings              | No  | No  | Yes |
| Static Power Reduction        | No  | No  | Yes |

This work proposes a bio-inspired Neuron-ADC with reconfigurable sampling and static power reduction for biomedical applications. The Neuron-ADC utilizes level-crossing compressive sampling and converts bio-signal to digital spikes to prevent wasting ADC energy on unnecessary data. Three design challenges of Neuron-ADC have been addressed: charge-injection-free signal sensing circuit, dynamic comparator with static power reduction, and bio-inspired refractory circuit. The reconfigurable sampling function makes the Neuron-ADC suitable for various bio-signals with either low power operation or high conversion accuracy. Moreover, the dynamic comparator can reduce static power up to 41.1% with 10 kHz sinusoidal test input. Simulation results of 40 nm CMOS technology show that from 10 Hz to 10 kHz input bandwidth, the ENOB is up to 6.9 bits with a corresponding FoM of 97 fJ/conversion. To sum up, the proposed Neuron-ADC paves the way to low-power and reconfigurable multi-modal biomedical recording and neuromorphic processing systems.

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