Test strategies for industrial testers for converter controls equipment

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ABSTRACT: Power converters and their controls electronics are key elements for the operation of the CERN accelerator complex, having a direct impact on its availability. To prevent early-life failures and provide means to verify electronics, a set of industrial testers is used throughout the converters controls electronics’ life cycle. The roles of the testers are to validate mass production during the manufacturing phase and to provide means to diagnose and repair failed modules that are brought back from operation. In the converter controls electronics section of the power converters group in the technology department of CERN (TE/EPC/CCE), two main test platforms have been adopted: a PXI platform for mixed analogue-digital functional tests and a JTAG Boundary-Scan platform for digital interconnection and functional tests. Depending on the functionality of the device under test, the appropriate test platforms are chosen. This paper is a follow-up to results presented at the TWEPP 2015 conference, adding the boundary scan test platform and the first results from exploitation of the test system. This paper reports on the test software, hardware design and test strategy applied for a number of devices that has resulted in maximizing test coverage and minimizing test design effort.

KEYWORDS: Detection of defects; Manufacturing; Modular electronics; Software architectures (event data models, frameworks and databases)

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1 Introduction

The Electrical Power Converters (EPC) group at CERN is in charge of the design, operation and support of various types of converters deployed in the accelerator complex. The control of these converters is based on different in-house systems composed of electronic boards and modules. The converter controls operate in a very specific environment such as; ionizing radiation or areas with limited access. Each failure impacts directly the operation of CERN’s facility, impacting machines such as the Large Hadron Collider (LHC). There is an increasing demand for production of new electronics, to renovate existing legacy systems, and to provide controls platforms for new facilities. To ensure a satisfactory uptime, a Mean Time Between Failure (MTBF) more than 1Mh is required as well as having early-life failures minimised before equipment installation. Thus, the assessment of electronic board quality must be performed in a simple and reproducible manner. Each board recently designed by the section has a corresponding automated test system which have been designed to easily detect and diagnose potential electrical errors (e.g. dry joins, open pins).

A set of testers based on the National Instruments PCI eXtension for Instrumentation (PXI) [1] modular acquisition platform was chosen to test boards of FGClite project [2]. FGClite is a radiation-tolerant Function Generator Controller (FGC) that has a modular design, facilitating test possibilities. The test software for FGClite was generally written in LabWindows, a C based language using PXI acquisition and generation instrumentation. This PXI Tester platform was described at the TWEPP 2015 [3] and since than more than 720 FGClite boards were successfully tested.

After building FGClite PXI testers, options for other testers were further explored and built, such as third-generation Function Generator Controller (FGC3) testers. In comparison to FGClite,
FGC3 is more complex and was not designed to facilitate test. In order to provide automatic test features and to increase the possible test coverage, the Boundary Scan (JTAG B-S) was included in the test platform. This allowed to establish different test approaches for different types of Devices Under Test (DUTs) in order to decrease test development time and increase test coverage. The JTAG B-S and PXI test platforms have been chosen depending on DUTs specificity (Analogue, Digital, Mixed), testability and test requirements. The test development strategy and guideline have been established, e.g. repositories and code change tracking were added to the test code development and validation process. To maintain high reliability of connections between test points and a DUT during testers’ lifetime, a modular mechanical bed-of-nails system has been introduced. The JTAG approach and mechanical fixture as well as the strategy were crucial to efficiently design and develop test systems for complicated boards without a big manpower effort.

2 Test platform

Figure 1 shows a block diagram of a generic test setup. Test equipment consists of three main parts: PXI, JTAG B-S and a Mechanical Fixture. The PXI chassis consists of different boards for data acquisition and generation as well as a control computer. Boundary-Scan is a generic digital IO cell interface. The test interfaces of each of the platforms are connected to a mechanical fixture which is mechanically interfacing them to the corresponding test points on the DUT.

As a DUT-specific part of the fixture, a mechanical bed-of-nails cassette contains a Test Control Card (TCC). The TCC is used for signal translation to/from the specific DUT IOs.

2.1 PXI acquisition and generation platform

The PXI-1042Q Chassis can house up to 7 data acquisition and generation modules and a controller card. The controller runs Windows, using C-based LabWindows as the platform to execute programs accessing PXI cards. The PXI crate accepts different modules to customize the tester according to

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**Figure 1.** Explicitive schematic of the test platform.

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Table 1. Parts of the PXI test platform

| Module Name   | Description                                                      |
|---------------|------------------------------------------------------------------|
| NI PXI-1042Q  | 8-slot 3U PXI Chassis with Universal AC                           |
| NI PXI-8108   | 2.53 GHz Dual-Core Windows Embedded Controller                   |
| NI PXI-4110   | Triple-Output Programmable DC Power Supply                        |
| NI PXI-6221   | 16 Analog Inputs, 2 Analog Output, 24 Digital IO                  |
| INCAA DIO8    | Low-Cost, 96 Ch, 5V TTL/CMOS Digital IO                           |
| Exoligent WorldFIP | Field-Bus interface card                                       |
| NI PXI-2533   | 256-Crosspoint SSR Matrix                                        |

The test to perform. Modules of the PXI System used for testers in converter controls electronic are shown on the table 1.

The measurement and control functionalities of the PXI test platform can be summed up as follows:

- 3 channel programmable power supply 0–6 V @ 0–1 A, 0–20 V @ 0–0.5 A, −20–0 V @ 0–0.5 A,
- 32 analogue inputs,
- 4 analogue outputs,
- 236 digital IO,
- WorldFIP communication,
- 4 × 64 cross point SSR matrix.

In order to extend the test possibilities and flexibility of the platform a cross point Solid State Relay (SSR) matrix is included in the system. The matrix functions as a software-defined relay matrix and it is able to interconnect sets of points of its interface. With this solution, the tester resources (analogue and digital channels in particular) can be multiplexed during the test execution. It gives numerous possibilities to test cards that require testing large set of signals of the same genre which would not be possible with the regular test resources. An example use of the SSR Matrix is shown and noted with the * in figure 1.

2.2 Multi-purpose JTAG Test Rack

Many of the modern digital Integrated Circuits (IC), especially programmable digital logic, are compliant with the IEEE 1149.1 standard [4], which can be used for validation of interconnection between JTAG-compatible electronics as well as functional tests of peripherals. Using the standard, the Multi-purpose Generic JTAG cell rack has been designed to unify the test environment, it contains 1024 JTAG IO cells in one chain. The outputs drive 3.3 V logic, inputs are compatible with the logic levels up to 5 V, extending the application of the platform.
To be able to send and receive digital values to and from the pin of an IC using JTAG it needs to be connected to a JTAG chain. The chain is managed by a controller through a TAP (Test Access Port). The controller used in the system has 2 such ports, the first is used for the Multi-purpose JTAG Test Rack and the second is used for a JTAG chain of a DUT (if required). Both the test infrastructure and the potential JTAG chain of the DUT are controlled by a device compatible with JTAG test generation software (JTAG Provision [5]). The controller can drive or sense any IO cell chained into its TAP. Interfaces of the controller are shown in figure 4.

When two boundary-scan compatible cells are inter-connected, it is possible to validate their connection by sending test vectors to their IOs. The methodology of this process is shown in figure 3. Most of the test vectors are generated automatically based on their netlists and board-to-board interconnections. The information about the JTAG compatible IC is included in a *.bsdl file. This requires minimum effort from the design point of view since the netlists are generated automatically and the inter-connection definitions can be easily integrated into the program. The concept of the automatic test generation is shown in figure 4.
More complex digital logic interconnections, such as memories or interface devices, can also be tested by using model files which are usually provided by the manufacturer or generated in JTAG software. If all necessary IOs are connected to boundary-scan cells and the *.model file exists, test vectors can be generated automatically. The cell can be either included in the DUT (i.e. FPGA, microcontroller) or external, coming from the multi-purpose JTAG Test Rack. In that case, the test signal is going through a DUT connector and the mechanical fixture. The information about routing is coming from the netlist files of the boards included in the test system and DUT. That connection is foreseen by the test designer during the test design phase and then set up in the JTAG test software.

2.3 Mechanical hardware

A mechanical fixture with an exchangeable Bed-Of-Nails was installed in the test site. It solves mechanical inter-connection problems by using spring loaded pins accessing test points and connectors. Its modular construction allows easy adaptation to DUT while maintaining test infrastructure connections. The mechanical fixture with a cassette is shown in figure 5.

Figure 5. Mechanical Fixture.

2.4 Unified test software

The software used to test boards includes C, LabVIEW, and python. Automated JTAG B-S tests are generated and executed using ProVision. Every test function is required to follow a certain procedure, described for every board. For all DUTs there is a need to be able to execute all the tests at once, but also separately. There are several test states: PASS, FAIL, SKIPPED (not in the test list), PENDING (currently under test) and ERROR. The board test is complete only if none of the registered tests are skipped [3]. After each test procedure, an output log file within a unified text structure is generated. To prevent board and equipment failure in case of detected failure, for each DUT, parameters such as current consumption for each test phase must be specified. All the aforementioned information is standard but different for every DUT. That is why, a generic software template in C language for the test was created to decrease the amount of development needed to create software for a new DUT. The functions defined in the template can call modules in other languages such as LabVIEW or python as well as execute previously generated ProVision tests. The template and the methodology were successfully used to create all test software components for FGClite and therefore defined a unified test software suite for future DUTs.

This provides a good user experience, since the software user interface (UI) is also unified among different tester software. Since most of the code is standard and included in the template,
the amount of work needed to develop software for a new DUT is limited to writing DUT-specific test functions (if not generated by JTAG-BS). The code and JTAG B-S files of each test software are put into the dedicated repository (GitLab) to be able to track improvements and organize the code. Each improvement, e.g. improvements during the production phase, are tracked in the repository system and are connected to the task management platform (Agile Jira). Each issue is fixed and related with a GitLab commit.

3 Devices under test description

This section describes FGC3 and FGClite boards. Additionally, the complexity of each board is defined based on the number of components and pins showed on the table 2.

FGClite is a radiation-tolerant FGC connected to the back-end industrial computers using the real-time communication. Its design is based on seven electronic boards containing 5 FPGAs. The Analogue Board (AB) embeds three voltage acquisition channels using delta-sigma ADCs and one analogue voltage output channel suing the 16-bit DAC, together with signal conditioning and a temperature compensated high-accuracy voltage reference. The Radiation Diagnostic Interface Module (RadDIM) contains an FPGA for twenty-four digital and four analogue input diagnostic channels. The Auxiliary Board (XB) contains an FPGA for external bus communication, radiation monitor and it interfaces with the RadDIM. The Communication Board (CB) has two FPGAs: one for communication at 2.5 Mbps with the CERN Control Centre (CCC) and the second implementing most of the critical functions together including the user front panel. The Input-Output Board (IOB) drives the current loops for the controls interlocks. The Power Board (PB) uses uninterruptible input voltages and embeds an FPGA to digitally control power delivery to all other boards. The Mother Board (MB) is a passive board interconnecting boards. Thanks to the modular design for test (DFT), FGClite provides a good access to test most of its components.

FGC3 is an FGC intended to work in a non-radiation environment and like FGClite, it is connected to the back-end industrial computer using a real-time communication. It is composed of three electronics boards. The Network Board (NB) embeds a CPLD handling network communication and network clock synchronization. Similarly to the FGClite, the Analog Board (AB) handles four voltage input acquisition channels using ADCs and two voltage output channels using DACs, together with a signal conditioning and a temperature compensated high-accuracy voltage reference. As shown in table 2, the Main Board (MB) is the most complex board to test and contains a Microcontroller and a DSP handling control loops, and controlling both NB and AB. It hosts an FPGA for external bus communication, interlocks, and power control.

| # elements / DUT | FGClite | FGC3 |
|------------------|---------|------|
|                  | CB      | AB   | PB   | XB   | IOB  | MB   | AB   | MB   | NB   |
| # components     | 211     | 298  | 112  | 111  | 249  | 14   | 297  | 566  | 71   |
| # pins           | 1163    | 1042 | 693  | 782  | 974  | 997  | 1080 | 3672 | 549  |

The board complexity of the FGC3 is much higher than in the case of the FGClite a similar functionality is embedded on three boards instead of seven. Many components are not accessible
on connectors, test points, etc. and therefore the advantages of in-circuit JTAG B-S has been significantly exploited.

4 Test strategies for different boards

The test strategy is specific to every board and the requirements for the test depend on its functionality and importance in the system overview. The test requirement is usually to be able to detect failures of all the components and connections in the board, however the core elements to be tested are usually identified by the DUT designers. For each DUT the test requirements are collected and after a detailed analysis of the requirements in combination with tester platform abilities, the appropriate manner of testing is decided, meeting the requirements with the least possible development effort. Many digital electronic components can be tested with JTAG B-S with little development effort as the test vectors are generated and executed automatically. Therefore, this test approach is preferred. If a board (or its part) is not JTAG B-S compatible, the PXI tests are likely to be chosen. Sometimes requirements include very specific module test that cannot be implemented with any available platform. In that case, the test concept is discussed with the DUT designers. As an example, the network interface part of the FGC3 Network Board could not be tested by PXI and JTAG B-S without a huge overhead of firmware and hardware development specific to that DUT. Therefore, the part is tested with the extra test with the FGC3 final functional test and the rest of the tests were generated automatically with JTAG B-S. Taking test requirements decisions usually leads to a trade-off between test coverage and test development time. To maintain a clear and reproducible way of communication between the test and design team, a test specification document is prepared and approved by the design and the test team to understand problems and testability trade-offs.

Generally, for the same DUT both platforms can be used concurrently. In comparison to having a single-platform used before [3], the most fitting test solution can be selected from two, which implies fewer constraints during the test design. Since both PXI and JTAG B-S can be managed with the same software and are connected to the same connection interface, the potential amount of development needed to change a platform during the test execution is reduced as well. This leads to an increase in test coverage as well as a decrease in test development time. Table 3 shows FGC3 and FGClite boards and tests chosen for their tests.

| Test Platforms / DUT | FGClite | FGC3 |
|----------------------|---------|------|
|                      | CB      | AB   | PB | XB | IOB | MB | AB | MB | NB |
| PXI                  | ✓       | ✓    | ✓  | ✓  | ✓   | ✓  | ✓  | ✓  |    |
| JTAG                 |         | ✓    |    |    | ✓   | ✓  | ✓  |    |    |
| Other                | ✓       |      |    |    |     |    |    |    |    |
| Test Availability    | Only PXI| PXI, JTAG B-S |

In the case of the FGClite, the PXI-based platform was used to test all active electronics, while the JTAG B-S was introduced for the passive MB due to a high number of connections. In the case of the FGC3, the JTAG B-S is used to test both the MB and the NB increasing the test coverage.
The components connected to the internal JTAG chain include: CPLD on the NB, and FPGA/DSP on the MB. All components not connected to any JTAG chain are tested by the PXI.

After each test a report is automatically generated, and is stored in a database. If all tests are passed, the Identification Number (ID) and Barcode of the tested DUT are associated and added to the database of group equipment. Otherwise, if any test has failed, the boards are diagnosed failures are reported to the board manufacturer.

5 Outcome after production tests

After a DUT is designed and a prototype is functionally validated, the process of production of boards is usually carried out as follows: component purchase (subcontractor 1), PCB production (subcontractor 2), assembly of boards (subcontractor 3) and reception testing at CERN.

This section describes the statistics of failures at the reception of the FGClite and FGC3 boards. Each board was tested with its dedicated tester. The boards from the subcontractor 3 are delivered in batches and before each subsequent batch is being assembled, CERN feeds back the failure statistics to the subcontractor 3, giving permission to continue the assembly process or working with the subcontractor 3 to improve the assembly process to meet CERN’s yield requirements [2].

The failure data is divided into two main groups:

1. Tester equipment failures not impacting the production but requiring to improve the test design.

| DUT Platform | Board name | Test Time | # Tested Boards | # Fail. boards | # Fail Test. | Comments |
|--------------|------------|-----------|-----------------|----------------|-------------|----------|
| FGClite      | MB         | 30s       | 120             | 1              | 0           | 2a: Connector inverted |
|              | CB         | 10m       | 120             | 0              | 8           | 1: FPGA programming   |
|              | AB         | 4m        | 120             | 5              | 0           | 2a: Pin not soldered  |
|              |            |           |                 |                |             | 2b: Transistor absent |
|              |            |           |                 |                |             | 2a: Chip incorrectly soldered |
|              |            |           |                 |                |             | 2a: Resistor network — dry joint |
|              |            |           |                 |                |             | 2c: Resistor network — pin open |
|              | PB         | 5m        | 120             | 0              | 1           | 1: 3V3 test point out of margin |
|              | XB         | 6m        | 120             | 0              | 0           |                     |
|              | IOB        | 2m        | 120             | 3              | 0           | 2b: transistor absent |
|              |            |           |                 |                |             | 2a: relay — pin not soldered |
|              |            |           |                 |                |             | 2a: transistor — pin not soldered |
| FGC3         | MB         | 6m30s     | 25              | 2              | 0           | 2a: connector pin not soldered |
|              | NB         | 0m50s     | 25              | 0              | 0           |                     |
|              | AB         | 4m        | 25              | 1              | 0           | 2c: Resistor network — pin open |

Table 4. Test performance from production of FGClite boards.
2. Production failures that will be analysed on case-by-case basis and will be communicated to the subcontractor. This group contains three different classes of failures: 2a soldering failure, 2b component placement failure, 2c component failure. The failure types are assigned manually by the technician performing tests, based on the detected error.

Testers could detect all FGC3 and FGClite production failures. The only tester problems (noted with 1 in the comment section) were related to an inaccurately calculated margin value and automated programming of the 2 FPGAs present on the FGClite CB board. After the first phase of using the testers, the failures were gathered and test functions were adjusted. It was possible because both PXI-based and Boundary-Scan platforms are executed within the test software that is possible to easily change during the first test-phase.

The group requires PCB production and assembly yield better than 99%. The test platform can assess this yield in a simple manner. Results from tests are then used to identify manufacturing quality problems and are fed back to subcontractors and improve their yield.

6 Conclusions

By using multiple design platforms and fitting a test strategy accordingly, it is possible to test complicated boards with relatively small design effort and manpower. Thanks to the Boundary-Scan automated test generation used for most of the digital circuits, the amount of time needed to create a test has significantly decreased in the section. For these tests the only requirement is to provide connection from tested IO to any B-S cell, the test logic design itself is often almost removed from test design workflow. If the DUT is mostly analogue or non-BS-compatible, it is tested with the PXI. During unit test development and validation phase, GitLab allows to easily track changes, effort and organizes the development process. By using unified software approach, it is possible to adaptively select different pieces of test software (including C, LabVIEW, python and Provision) to select the most efficient way to develop a test solution, maintaining single test execution standard.

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