Cost-Aware Exploration for Chiplet-Based Architecture with Advanced Packaging Technologies
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Abstract—The chiplet-based System-in-Package (SiP) technology enables more design flexibility via various inter-chiplet connection and heterogeneous integration. However, it is not known how to convert such flexibility into cost efficiency, which is critical when making a design decision. In this paper, we develop an analytical cost model that can estimate the cost of the 2.5D chiplet-based SiP systems under various interconnection options and technology nodes. We conducted two case studies using our cost model to explore the cost characteristics of the 2.5D chiplet-based SiP system. Based on the case studies, we made several observations on the interposer selection, design partition granularity, and technology node adoption for cost-efficient chiplet-based SiP design.

Index Terms—chiplet, cost model, heterogeneous integration

I. INTRODUCTION
Recently, the “chiplet”-based System-in-Package (SiP) becomes the potential replacement of the conventional System-on-Chip (SoC) which suffers from the increasing complexity and cost of new technology nodes. The SiP breaks a monolithic die based 2D SoC into multiple smaller pieces and keep them in the same package. These dies can be of different functionalities, hybrid technology nodes, and/or from multiple IP designers. Such a heterogeneous integration greatly reduces the design complexity of each die due to IP reuse. So far, the majority of the chiplet system research focuses on either demonstrating the chiplet prototypes [1]–[4]; or studying the workload-aware dataflow [5], and the network-on-package [6]–[8] under the performance, energy, and thermal constraints. However, little attention has been given to the cost, which will become a critical factor whether to adopt the chiplet/SiP in the design. All the potential advantages of the chiplet related technologies ultimately have to be translated into cost savings when evaluating a design strategy.

The analytical cost model can be the solution to estimate the cost and guide the early-stage cost-aware design. Previously, the analytical cost model has been used in evaluating the TSV-based 3D architecture [9] or the silicon interposer based 2.5D integrated system [10], [11]. These works cannot be directly adopted because several new design choices emerge in the chiplet-based SiP design and are not yet well explored, including the inter-chiplet connection, the homogeneous/heterogeneous integration, make up a large and complex design space that is not yet well explored.

In this paper, we make, to our best, the first attempt to build a cost model for chiplet-based SiP design space exploration. With the input of the system scale (e.g., the transistor count of compute die, memory cell count, and other statistics), the partition granularity (e.g., the die count), and the technology node, our cost model will first translate the system scale into the area and the number of wiring layers. The cost breakdown of the die, the bonding, and the package is then calculated based on these data. With the collected data of transistor density as well as the wiring pitches, our cost model is able to support the 2.5D Silicon interposer, the 2.5D organic interposer, and MCM under the technology nodes ranging from 28nm to 5nm to support the heterogeneous integration. Using the proposed cost model, we perform two case studies to explore the cost characteristics of the 2.5D chiplet-based SiP system; and made several observations on the interposer selection, design partition granularity, and technology node adoption for cost-efficient chiplet-based SiP design.

II. ANALYTICAL COST MODEL FOR CHIPLET SYSTEM WITH INTERPOSER AND MCM-BASED INTEGRATION
Our analytical cost model is made up of the manufacture cost of each die/interposer, the bonding cost, and the package cost; it is able to model the chiplet system with the silicon interposer, organic interposer, and MCM-based integration. The manufacture cost of single die and silicon interposer has been well studied in previous work [11]. For space limitation, this section focuses on the manufacture cost of organic interposer, the bonding and package cost.

A. Manufacture Cost Model of An Individual Organic Interposer
The organic interposer is built in a panel form (i.e., a large square or rectangle), different from die and silicon interposer, which are built in the wafer form, rather than a wafer form (i.e., a round plate). Eq. [1] shows the cost ($C_{\text{org\_int}}$) and yield ($Y_{\text{org\_int}}$) of an organic interposer.

\[ C_{\text{org\_int}} = \frac{C_{\text{panel}}}{N_{\text{org\_int}}} = A_{\text{panel}} / A_{\text{org\_int}} \times Y_{\text{panel}} \times (1 + \frac{A_{\text{org\_int}} D_0}{\alpha})^{-\alpha} \]

\[ Y_{\text{org\_int}} = Y_{\text{panel}} \times (1 + \frac{A_{\text{org\_int}} D_0}{\alpha})^{-\alpha} \]

Here $C_{\text{panel}}$ and $N_{\text{org\_int}}$ are the panel cost and the number of organic interposers obtained from a panel. $A_{\text{panel}}$ and $A_{\text{org\_int}}$ are the area of the panel and the organic interposer, respectively. $Y_{\text{panel}}$, $D_0$, $\alpha$ are the yield, defect density, and defect clustering parameter of the interposer panel, respectively. They are collected from ICKnowledge [12] and are determined by the technology node.

B. Bonding Cost Model
The unpackaged interposer-based chiplet system is made up of $n$ functional dies on top and one interposer die at the bottom; while the MCM based chiplet system directly deploys $n$ functional dies onto the organic substrate. The bonding cost of the unpackaged chiplet system is calculated by Eq. [2] and Eq. [3] which represent the interposer-based chiplet system ($C_{\text{int\_2.5D}}$) and the MCM-based chiplet system ($C_{\text{MCM\_2.5D}}$), respectively.

\[ C_{\text{int\_2.5D}} = \sum_{i=1}^{n} C_{\text{die\_int}} + \frac{\sum_{i=1}^{n} (Y_{\text{die\_int}} + C_{\text{bond\_int}})}{Y_{\text{bond\_int}}} \]

\[ C_{\text{MCM\_2.5D}} = \sum_{i=1}^{n} C_{\text{die\_int}} + \frac{\sum_{i=1}^{n} (Y_{\text{die\_int}} + C_{\text{bond\_int}})}{Y_{\text{bond\_int}}} \]

Here $n$ is the number of function dies, $C_{\text{die\_int}}$, and $Y_{\text{die\_int}}$ (i.e., the manufacturing cost and yield for the $i^{th}$ functional die. $C_{\text{bond\_int}}$ and $Y_{\text{bond\_int}}$ are the bonding cost and yield for the $i^{th}$ die. In most cases each functional die is assumed to have the same bonding cost and yield. $C_{\text{int\_2.5D}}$ and $Y_{\text{int\_2.5D}}$ are the manufacturing cost and yield for the interposer. Comparing Eq. [2] and Eq. [3] the cost of the interposer based chiplet system has an extra term of $C_{\text{int\_2.5D}} - C_{\text{int\_2.5D}}$, which depends on the material of the interposer.
Table I: Switching points of organic interposer/MCM based chiplet systems under different technology nodes

| Tech Node | Chiplet Type | 7nm (µm²) | 10nm | 12nm | 16nm | 20nm | 28nm |
|-----------|--------------|----------|------|------|------|------|------|
| 2D Area   | Org 2.5D     | 178      | 191  | 264  | 279  | 313  | 479  |
|           | MCM          | 119      | 120  | 126  | 128  | 131  | 147  |
| Tx Count  | Org 2.5D     | 11.17    | 10.11| 11.22| 7.66 | 6.12 | 3.02 |
|           | MCM          | 11.84    | 6.72 | 5.96 | 5.14 | 5.20 | 1.75 |

C. Package Cost Model

The package cost depends on the type of package. Flip chip based organic substrate can be used in both interposer based and MCM based chiplet system. For simplification we use the flip chip based organic substrate to showcase the package cost model. Similar cost models can also be used in other package types. In addition to the package type, the package cost is also determined by three factors, i.e., the package area, the layer number of package (#core and #buildup), and the pin count.

Given the numbers of core layers and the build-up layers, we collect the package cost under different combinations of substrate area and pin count from ICKnowledge [12]. With the collected data, we derive an empirical function of the package cost ($C_{P}$) with respect to the combination of the substrate area ($A_{sub}$) and the number of pins ($N_{pin}$) in Eq. (4). $\mu_0$, $\mu_1$, $\mu_2$ are the regression parameters determined by the numbers of core layers and the build-up layers.

$$C_{P} = \mu_0 A_{sub} + \mu_1 N_{pin} + \mu_2$$

Fig. 1 shows the regressive package cost model of the organic substrates of two different configurations (a) 2 core layers and 5 build-up layers; and (b) 2 core layers and 9 build-up layers. The result shows a satisfying linearity of the developed regressive model. We will use this regressive package model in the follow-up case studies.

III. CASE STUDY

In this section, we leverage the developed cost model to conduct two case studies and showcase the cost characteristics of the chiplet based architecture, i.e. a heterogeneous multi-chiplet system with HBM stacks (Sec. III-A), and a heterogeneous multi-chiplet system which partitions the core components and IO components onto different chiplets under different processes (Sec. III-B).

A. Heterogeneous Chiplet System with HBM Stacks

The heterogeneous chiplet system with high bandwidth requirement integrates the core dies and the HBM stacks onto the silicon interposer or the organic interposer. Each HBM stack is made up of a base die at the bottom and several layers of memory dies atop [13]. For the base die, the area of a 1024-bit signal interface is mainly determined by the pitch width of the microbumps. We set the pitch width as 45µm for the silicon interposer and 110µm for the organic interposer. We exclude MCM in this case study because the C4 bump pitch is too large to place the whole signal and I/O interface under the area constraint of existing HBM.

This case study aims to study the extra cost introduced by HBM stacks. Fig. 2 visualizes the relative cost breakdown of interposer and bonding, where the manufacture cost of core dies as the 100% base unit. The three subfigures show the system scales of 200mm$^2$, 400mm$^2$, and 800mm$^2$ under 7nm process respectively. We observe that the organic interposer based chiplet system introduces less than 50% overhead for HBM stacks and the bonding yield takes the majority of the overhead. While for the silicon interposer based chiplet system, the relative cost overhead is much larger.

B. Heterogeneous Chiplet System with Hybrid Processes

Considering the technology scaling of I/O and other peripheral circuits are much slower than that of the compute logic and the on-chip memory [14], the cost efficiency may potentially increase if different components are assigned to different dies and are implemented in different technology nodes. Inspired by AMD’s EYPC2 CPU [2], [3], this case study explores the heterogeneous architecture where the cores and the IO peripheral circuits are split into different dies and implemented in different technology nodes. As shown in Fig. 3 we study the MCM based chiplet system under different system scales and different I/O proportion. To quantitatively explore the cost efficiency of the heterogeneous chiplet system, we compare the cost of a 7nm monolithic system, a 12nm monolithic system, and three hybrid systems with different numbers of core dies where the core dies and the I/O die are respectively assumed at 7nm and 12nm technology nodes. The three subfigures of Fig. 3 respectively show the circumstances when the numbers of transistors on the core die are 5 billion, 10 billion, and 50 billion. And each subfigure includes the proportions of I/O circuits in the range of {30%, 40%, 50%}.

We find that the hybrid system which partitions the core logics and the I/O circuits into different dies achieves salient benefits on cost efficiency compared with the monolithic systems under both the mature and advanced technology nodes. Moreover, as the scale of the chiplet system gets larger, both the cost efficiency of the hybrid system and the optimal number of core dies increase. For the three different system scales in Fig. 3 the optimal chiplet system respectively achieves 34%, 48%, and 77% cost efficiency improvement compared with the 7nm monolithic counterpart, and the optimal numbers of core dies are respectively 2, 4, and 8.

IV. CONCLUSION

In this paper, we build an analytical cost model for the 2.5D chiplet system under various interconnection options and technology nodes. We conduct a series of case studies to explore the cost characteristics under both homogeneous and heterogeneous scenarios. By analysing the case study results, we made several observations on the interposer selection, design partition granularity, and hybrid technology node adoption for the cost-efficient chiplet-based SiP design.

Besides the manufacture cost and the package cost discussed in this paper, the testing cost and the cooling cost also play an important role in the early-stage design decision. Meanwhile, the exploration would be more comprehensive when considering the performance, power, area, and cost simultaneously. All these will be explored in our future work.
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