Continuous-wave electrically pumped 1550 nm lasers epitaxially grown on on-axis (001) silicon

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Heteroepitaxy of III–V compound semiconductors on industry standard (001) silicon (Si) substrates is highly desirable for large-scale electronic and photonic integrated circuits. Challenges of this approach relate primarily to lattice, polarity, and coefficient of thermal expansion mismatch, which ultimately generate a high density of defects and limit the reliability of active devices. Ongoing efforts to monolithically integrate lasers in silicon photonics include leveraging quantum dots for reduced sensitivity to defects and the ability to enable 1310 nm lasers with gallium arsenide (GaAs) and related compounds. In this work, to extend the operation window to the widely used 1550 nm telecommunications region, we have demonstrated continuous-wave (CW) electrically pumped indium phosphide (InP)-based quantum well lasers on complementary metal-oxide-semiconductor (CMOS)-compatible (001) Si. Heteroepitaxy of InP and related compounds on Si poses additional challenges because the lattice mismatch is significantly larger compared to GaAs. Key to our approach is the development of a low dislocation density InP-on-Si template by metalorganic chemical vapor deposition (MOCVD). Following an InP buffer with a surface defect density of $1.15 \times 10^8$/cm$^2$, a seven-layer indium gallium arsenide phosphide (InGaAsP) multi-quantum well laser diode structure was grown. Fabry–Perot ridge waveguide lasers were then fabricated. A 20-µm wide and 1000-µm long laser demonstrates a room temperature continuous-wave (CW) lasing threshold current density of 2.05 kA/cm$^2$ and a maximum output power of 18 mW per facet without facet coating. CW lasing up to 65°C and pulsed lasing greater than 105°C were achieved. This MOCVD-based heteroepitaxy approach offers a practical path toward monolithic integration of InP lasers in silicon photonics. © 2019 Optical Society of America under the terms of the OSA Open Access Publishing Agreement

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1. INTRODUCTION

Driven by the significant growth in IP traffic and power consumption of worldwide networks and data centers, silicon photonics has received significant attention in recent years [1]. This technology platform realizes photonic integrated circuits (PICs) by leveraging established complementary metal-oxide-semiconductor (CMOS) processes. For laser integration, hybrid and heterogeneous techniques have been demonstrated [2–5]. However, for large-scale integration, monolithic techniques are preferred, and direct heteroepitaxy of III–V lasers on silicon (Si) is particularly promising [6]. Discrete indium arsenide (InAs)/gallium arsenide (GaAs) quantum dot (QD) lasers on Si have generated notable device characteristics including low threshold and high temperature operation [7,8]. In addition to providing reduced sensitivity to defects, QDs allow for 1310 nm emission with GaAs-based heteroepitaxy. These lasers are promising for short-reach optical interconnects for data centers and supercomputers [9]. It is, however, challenging to extend the wavelength of the QDs to the 1550 nm wavelength region. The mature indium phosphide (InP) material system therefore prevails for longer wavelength lasers [10]. Additionally, operation in this regime enables a diverse set of applications outside of telecommunications including LiDAR, sensing, free space optical communications, and microwave photonics [11–13]. This work focuses on the development of 1550 nm InP-based quantum well (QW) laser diodes (LDs) monolithically grown on CMOS-compatible (001) Si by metalorganic chemical vapor deposition (MOCVD).

The first InP on Si laser, emitting at 1540 nm, was demonstrated with a multi-QW (MQW) structure in 1991 [14]. Vapor mixing epitaxy (VME) was utilized to produce a 13-µm-thick InP layer on a 2 µm GaAs buffer on a 2° offcut Si (001) substrate. No device degradation was observed for over 7000 h of aging owing to the relatively low defect density achieved (less than $10^7$/cm$^2$) [15]. Such a thick template is a concern for cracking and for integration into the silicon photonics platform. In recent work, a much thinner InP template was developed (as thin as 1.5 µm) utilizing an InP-on-V-grooved (001) Si approach [16]. An indium gallium arsenide (InGaAs)/indium aluminum gallium arsenide...
(InAlGaAs) MQW laser was grown on this template, and room temperature (RT) lasing was demonstrated under pulsed current operation only. Further advancements were also made by replacing the QW active medium with InAs/InAlGaAs QDs emitting at telecom wavelengths, whereby both optically pumped microlasers and electrically pumped diode lasers were demonstrated [17–19]. However, there have been no demonstrations of RT continuous-wave (CW) lasers realized with a total III-V layer thickness less than 10 µm above the bottom Si substrate, including all the III-V buffer layers and the topmost laser structure. A thinner buffer could be considered more realistic for coupling of light from III-V active regions to the silicon waveguide on a silicon-on-insulator (SOI) platform [20–22]. Some other issues such as the growth rates and facet control of selective heteroepitaxy of III-V lasers on Si, as well as thermal budgets in a CMOS silicon photonics process need to be addressed in the future to facilitate the integration of III-V lasers with silicon photonics circuits.

Several efforts have been attempted to improve the crystalline quality of InP buffers on Si to minimize nonradiative recombination centers [23–25]. In this work, multiple In$_{0.71}$Ga$_{0.29}$As/InP strained layer superlattices (SLSs) were utilized to interact with and consequently filter the propagating threading dislocations (TDs) in the InP buffer. The resulting InP-on-Si template exhibits a low surface defect density of 1.15 × 10$^{10}$/cm$^2$. A seven-period InGaAsP/InGaAsP MQW structure was grown on this template. The active region is surrounded by identical InGaAsP separate confined heterostructure (SCH) layers. Fabry–Perot ridge waveguide lasers were then fabricated. A 3D schematic and cross-section scanning electron microscopy (SEM) image of the Si-based laser are shown in Fig. 1. The lasers operate in CW conditions up to a chip temperature of 65°C, and under pulsed conditions over 105°C. A CW lasing threshold current density of 2.05 kA/cm$^2$ and output power of 18 mW/facet were demonstrated at RT, without any facet coating. The combination of a reduced InP buffer thickness on a CMOS-compatible (001) silicon substrate and subsequent realization of high temperature continuous-wave operation, these results represent a major advance for 1550 nm lasers monolithically integrated on Si.

2. GROWTH AND FABRICATION

The InP-on-Si template was first grown using a horizontal-reactor low-pressure (LP) MOCVD system. A nano-patterned V-grooved (001) Si substrate was utilized to provide an aspect ratio trapping (ART) of dislocations as well as to avoid the generation of anti-phase boundaries (APBs) [26]. A 2-µm-thick GaAs layer was then grown as an intermediate buffer to alleviate the ~8% lattice mismatch between InP and Si. Details of the V-grooved Si and GaAs buffer growth are available in [27]. Subsequently, an InP buffer was grown in three primary steps. A 30 nm low temperature (LT) InP was grown at 435°C to form a nucleation layer and to accommodate the high density of generated misfit dislocations (on the order of 10$^{10}$/cm$^2$). A 45 nm middle temperature (MT) InP layer was then grown at 540°C for coalescence and to planarize the InP growth surface. Afterwards, a 1-µm-thick high temperature (HT) InP primary buffer layer was grown at 600°C–630°C to enhance TD self-annihilation and subsequently improve the buffer quality. However, the thermal budget issue arising from the high temperature growth may be a concern for the compatibility with silicon photonics processes. Next, as depicted in Fig. 2(a), four to five sets of ten-period InGaAs/InP SLSs separated by HT-InP spacers were grown. The total thickness of the InP buffer layer is less than 4 µm. The cross-section scanning transmission electron microscopy (STEM) image shown in Fig. 2(b) clearly illustrates the generation, propagation, and interaction of the defects. A significant number of TDs are either redirected or terminated at the heterointerfaces of each stack of SLSs. Some stacking faults (SFs) are observed to penetrate through the SLSs and reach the InP top surface. These SFs would likely adversely affect device performance by introducing leakage paths [28]. The density of SFs is fairly low, on the order of 10$^7$/cm$^2$. Further details on the InP buffer and SLS growth optimization will be reported elsewhere.

Following the InP buffer growth, the surface is mirror-like with minimal hillocks as observed in the optical microscope image of Fig. 2(c). As shown in the atomic force microscopy (AFM) image of Fig. 2(d), the surface morphology is smooth with only a few pinholes observed. The surface roughness (RMS value) is 3.79 nm for an area of 10 µm × 10 µm. To accurately quantify the surface defect density, a large-area (total observation area of ~ 681 µm$^2$) electron channel contrasting imaging (ECCI) scan was performed. The channeling condition consists of both (040) and (220) excitations to maximize the detection of 60° misfit dislocations threading onto the surface [27]. A representative ECCI image is shown in Fig. 2(e), illustrating the ability to count and distinguish TDs, SFs, and pinholes. To accurately evaluate the effect of the SLSs on dislocation reduction, RT photoluminescence (PL) measurements were carried out at a low excitation regime (8.3 W/cm$^2$) to assess the optical quality of two InP-on-Si templates equipped with the same thickness of InP buffer but one with SLSs and the other without SLSs. As shown in Fig. 2(f), a more than five-fold increase in the PL peak intensity when the surface defect density was reduced from 4.81 × 10$^8$/cm$^2$ to 1.15 × 10$^8$/cm$^2$. 

![Fig. 1.](image-url) (a) 3D schematic representation of InP LD on CMOS-compatible (001) Si and (b) tilted cross-section false color SEM image of an as-cleaved 20 µm × 1000 µm device.
Fig. 2. (a) Epitaxial structure and (b) cross-sectional STEM image of the 3.9 \( \mu \)m InP buffer grown on V-grooved (001) Si. (c) Optical microscope image of the InP surface after growth and (d) a \( 10 \times 10 \) \( \mu \)m\(^2\) AFM scan of the surface morphology demonstrating a roughness of 3.79 nm. (e) Representative ECCI image of the InP buffer revealing surface defects. Low power excitation RT-PL spectra of (f) the InP-on-Si with and without insertion of SLSs, and (g) seven-layer InGaAsP-based QW active structure grown on InP-on-Si template and InP native substrate, respectively.

by introducing the SLSs. A further comparison is presented in Fig. 2(g), where a seven-layer InGaAsP/InGaAsP MQW active region with emission near 1550 nm was grown on the InP-on-Si template with SLS insertion, as well as on a premium InP (001) native substrate. The low power (3.7 W/cm\(^2\)) PL measurement indicates a reasonable PL intensity and a comparable full-width at half-maximum (FWHM) value for the QWs grown on InP-on-Si. The peak intensity for the QWs on Si is approximately 3.6 times lower than that demonstrated for the native InP substrate. Worth noting, QWs are considered to be more sensitive to dislocations than QDs. A reported PL intensity discrepancy is greater than an order of magnitude for QWs grown on GaAs-on-Si compared to those grown on native GaAs substrates [29]. These results suggest the suitability of our advanced InP-on-Si template for realizing 1550 nm lasers.

To investigate further, an MQW laser structure was grown both on a high quality InP-on-Si template and on a n-type InP (001) substrate. Disilane (Si\(_2\)H\(_6\)) and diethylzinc (DEZn) were used for the n- and p-type dopants, respectively, for cladding and contact layers. The detailed layer structure is depicted in Fig. 3(a). Ridge lasers for electrical pumping were fabricated following the steps summarized schematically in Figs. 3(b)–3(f). A Ti/Pt/Au metal stack was first deposited for the p-contact and then covered with silicon dioxide (SiO\(_2\)), which was subsequently patterned to provide a hard mask for ridge etching. The ridge waveguides were formed using inductively-coupled plasma reactive ion etching (ICP-RIE). The etch terminated well above the active region to avoid damage to the QWs. A smooth sidewall was realized using chlorine/hydrogen/argon (Cl\(_2\)/H\(_2\)/Ar) and an etch temperature of 200°C. Following sidewall passivation, another etch was performed to expose the n-InP contact layer. After the deposition of Ni/AuGe/Ni/Au alloyed metal contacts, dielectric material was deposited for sidewall passivation. The metal contacts were exposed with a patterned dielectric etch, and then 2-\( \mu \)m-thick Au contact pads were formed with a lift-off process. The final device geometry is shown schematically in Fig. 1(a). After the frontend fabrication was completed, the samples were thinned, and laser bars were cleaved to form facets. Devices were then mounted onto ceramic carriers to facilitate characterization.

3. RESULTS AND DISCUSSION

Figures 3(g) and 3(h) show broad view optical microscope images of devices fabricated on InP and on Si prior to cleaving. Hillocks are observed for lasers on Si with an extremely low density of \( \sim 1,052/\)cm\(^2\), originating from the indium clustering occurring during the InP buffer and SLSs growth. Fortunately, most of the ridge waveguides have bypassed the sparse hillocks. A 70° tilted SEM image of an as-cleaved laser bar with a 20 \( \mu \)m ridge width was shown in Fig. 1(b). The Si V-grooves are aligned parallel to the laser stripes along the [110] direction. The cleaved facets are clean, mirror-like, and free of corrugations for this device. The III-V layers can be clearly distinguished in the false color SEM image. Five stacks of SLSs were utilized for the InP-on-Si template (total InP buffer thickness of 3.9 \( \mu \)m) used for the final laser structure, which yields a surface defect density of 1.15 \times 10^9/cm\(^2\). Compared to state-of-the-art GaAs-on-Si template technology that achieves a defect density on the order of 10^8/cm\(^2\), the InP surface defect
density is higher due to several factors. The larger lattice mismatch between InP and Si (8%) compared to GaAs and Si (4%) requires a thicker buffer to reduce the dislocation density. Therefore, the higher dislocation density for InP-on-Si prior to SLS insertion results in a lower dislocation filtering efficiency due to a reduction of strain inside the SLSs [30]. Meanwhile, the larger lattice mismatch also results in a rougher surface morphology, degrading the efficacy of the inserted SLSs by deteriorating SLS interfaces and varying SLS alloy compositions, thus hindering dislocation glide [31].

The smaller mismatch in the coefficient of thermal expansion between InP and Si weakens the effect of thermal cycle annealing that propels the dislocations. Also, the operation of the SLSs in the InP-on-Si template is less effective compared to InGaAs/GaAs SLSs in GaAs-on-Si with similar strain fields, thus limiting their dislocation filtering ability. More specifically, the high indium-containing In$_{0.71}$Ga$_{0.29}$As/InP SLSs adopted here could progressively decrease the dislocation glide velocity, limiting the lateral motion of the dislocations [32].

Last, another possible explanation for the less effective SLSs is attributed to the reduced elastic shear modulus of the high indium-containing In$_{0.71}$Ga$_{0.29}$As/InP SLSs to repulse dislocations because the shear modulus decreases monotonically with increasing lattice constant [30]. The In$_x$Ga$_{1-x}$As/InP SLSs can therefore be further improved by reducing the indium composition to less than 30% [33].

Representative current-voltage (IV) and light-current (LI) characteristics for a 20 µm × 1000 µm ridge laser on InP and Si are shown in Fig. 4. These measurements were performed at a temperature-controlled stage temperature of 15°C. Although the turn-on voltage of the LDs on both substrates are similar, the extracted series resistance on Si (1.7 Ω) is more than twice that for the laser on InP (0.8 Ω). This is primarily attributed to the significantly thin n-InP conductive layer for the laser on Si, which adds lateral n-resistance to the total series resistance, compared to the >150-µm thick n-type InP substrate of the laser on InP. More n-type doping in the InP buffer for the laser on Si in future implementations is expected to improve performance. Additionally, defects also serve as carrier scattering centers, resulting in higher leakage and higher resistance [34]. The threshold currents and total wall-plug efficiencies (WPEs) can be inferred from Fig. 4(b).
on Si (the LD on InP typically demonstrates a lasing threshold current density of 650 A/cm²), the slope efficiency on Si is also approximately two times lower (0.07 W/A) compared to the InP laser (0.13 W/A). These discrepancies correlate well with their respective QW PL intensities from Fig. 2(g). The total WPE for the laser on Si is approximately 2.7% at its peak, more than five times lower than that for the laser on InP. This difference is mainly attributed to the lower injection efficiency for the laser on Si, as well as the larger series resistance.

Figure 5 presents the RT lasing spectra of a 20 µm × 500 µm laser device on Si. The measurement temperature was fixed at 20°C. (b) Lasing spectra for the same device at various stage temperatures with an injection current of 400 mA.

The lasing characteristics for various cavity lengths are further presented in Fig. 6, measured under both CW and pulsed operating conditions (300 ns current pulses, 10% pulse duty cycle). As demonstrated in Figs. 6(d)–6(f), a significant reduction (2–3 times) in threshold densities was observed under pulsed pumping, compared to the CW operation, indicating that the lasers on Si are primarily limited by the device self-heating. This heat could originate from the larger series resistance, and lower injection efficiency that results from TDs present inside the active region, as well as the higher free carrier loss at higher injection current levels. The threshold current density, Jth, is generally lower for longer cavities. However, the considerably large Jth for the 375 and 1500 µm long devices may be due to imperfect facet cleaving.

A high reflectivity (HR) coating on the rear facet is expected to lower the threshold, increase the output power, and improve the temperature stability [35].

Temperature-dependent LI characteristics were also measured, and the results are shown in Fig. 7. A thermal-electric cooler (TEC) was used to control the stage temperature. As demonstrated in Fig. 7(a), the 20 µm × 1000 µm laser bar can sustain lasing up to 65°C under CW operation. The highest output power at a chip temperature of 60°C is 5 mW. Thermal roll-over is observed in the LI characteristics; this could be associated with the severe device self-heating as discussed earlier, as well as an inferior heat sink on Si due to the highly defective InP/GaAs interface [see Fig. 1(b)] and the residual thermal stress inside the InP-on-Si template [36]. It is worth noting that all of the approximately 20 devices measured, of various cavity lengths, operated stably during repeated room-temperature LIV and temperature-dependent LI measurements without suffering any rapid degradation or failure. This is speculated to be related to the suppressed development of dark spot defects (DSDs) into dark line defects (DLDs) in InP-based LDs, caused by dislocation climbing [37].

It is well known that the major cause of device aging in AlGaAs/GaAs-based lasers is recombination enhanced dislocation climb (REDC) [38], and the growth of (100) DLDs and DSDs, which significantly extend with increasing current injection and higher junction temperature [39]. Specifically, the evolution of DLDs is caused by the climbing motion of dislocations, resulting in rapid degradation. Recently, the extracted device lifetime of the InAs/GaAs QD lasers on Si is partially attributed to their greatly reduced threshold current densities, in addition to the apparent lower sensitivity of QDs to defects. Although the thresholds and the buffer quality of InP-based LDs on Si are inferior to GaAs-based QD lasers on Si, the reliability of C-band InP-based LDs on Si is promising due to various intrinsic properties. First, for C-band InP-based lasers, experiments have revealed a lower recombination energy due to the longer lasing wavelength (1550 nm) [40]. This feature allows for a significantly reduced REDC compared with some 1300 nm lasers on Si, thus extending device lifetime. Second, the development of DLDs strongly depends on the bandgap energy, as proven experimentally in [41]. In that experiment, under the same severe aging conditions (injection current density of 10 kA/cm² and high junction temperature of 250°C), DLDs were only observed in devices lasing at 1290 nm, while no DLD was formed for the device lasing at 1550 nm. Additionally, the development speed of (100) DLD was calculated to be approximately 0.3 µm/h, under the 10 kA/cm² injection level and junction temperature of 250°C, which is two orders of magnitude smaller than AlGaAs/GaAs operating under similar current density but at room...
Fig. 6. LI characteristics for lasers on InP for various cavity lengths under (a) CW and (b) pulsed current injection. The cavity width is 20 µm for all devices. (c) Dependence of threshold current density of InP laser on the cavity length under both operation modes. (d) LI plots for lasers on Si for different cavity lengths under (d) CW and (e) pulsed operation, along with (f) their extracted threshold current densities.

Fig. 7. Measured LI characteristics for the 20 µm × 1000 µm ridge laser on Si as a function of stage temperature under: (a) CW pumping and (b) pulsed operation, and (c) temperature dependence of threshold current. (d) LI curves from the same device size on InP at various stage temperatures under (d) CW and (e) pulsed operations, and (f) temperature dependence of the threshold current.
temperature [41]. Moreover, the InP-on-Si buffer is equipped with a lower residual thermal strain, on the order of $10^8$ dyn/cm$^2$, which is an order of magnitude lower than that for GaAs on Si [40]. The growth of dislocations is aided by the presence of a large tensile strain that results from the mismatch in the thermal expansion coefficients [42]. Last, during an auto-current-control (ACC) aging test of 1550 nm InP-based LDs on Si [37], it was revealed that although the emergence of DSD is responsible for gradual degradation, the density of DSDs becomes saturated after a certain number are generated (the DSD density is on the same order as the dislocation density inside the active region). Therefore, no further degradation will take place, and the existing DSDs would neither evolve into detrimental DLDs, nor grow larger in size [37]. All of these inherent advantages of InP-based LDs demonstrate that reliable operation of 1550 nm LDs on Si should be attainable. It is also pointed out that by replacing the QWs in this work with InP-based QDs, a longer device lifetime can be anticipated. Even though further improvements can be made, the InP-on-Si laser results presented here show great promise for realizing practical 1550 nm lasers monolithically integrated in silicon photonics.

The pulsed measurements reported in Fig. 7(b) demonstrate lasing to greater than 105°C, limited by the temperature range of the TEC used. The characteristic temperature $T_0$ was calculated from the data reported in Fig. 7(c) using the following expression [16]:

$$\frac{I_{th}(T_1)}{I_{th}(T_2)} = \exp \left( \frac{T_1 - T_2}{T_0} \right).$$

For the QW laser grown on Si under CW pumping conditions, the characteristic temperature was extracted to be 65.3 K between 15°C and 50°C, and 41 K between 50°C and 65°C. In contrast, the $T_0$ value is higher (55 K) between 55°C and 105°C under pulsed current injection with a duty cycle of 10%. The same temperature-dependent measurement was also performed for the lasers grown on native InP with an identical device geometry. In addition to a higher output power as well as an elevated operating temperature (95°C under CW injection and greater than 105°C under pulsed operation), the threshold temperature stability is also apparently improved, as shown in Fig. 7(f). The $T_0$ value on InP was 74 K between 15°C and 55°C, and 44.2 K between 55°C and 85°C. The severe Auger recombination and carrier escape at above 85°C accounts for the sharp decrease of $T_0$ (28 K). Under pulsed operation, the $T_0$ was extracted to be 111.5 K between 15°C and 55°C, and 51.2 K between 55°C and 105°C. Improved temperature characteristics for lasers on both substrates can be expected by replacing the InGaAsP-based active region with InAlGaAs alloys due to their larger conduction band offset [43], as well as by replacing the conventional QW active elements with the InAs/InAlGaAs quantum dot or quantum dash materials for their lower thresholds and more isolated energy states characteristics [44,45]. Also, introducing more n-type doping in the InP buffer layer for the laser on Si, as well as incorporating in situ thermal cycle annealing, are both expected to improve the device performance without increasing the total III-V buffer thickness. Nevertheless, the results reported here represent a significant advancement for the realization of 1550 nm lasers on CMOS-compatible (001) silicon substrates.

4. CONCLUSION

Using a relatively low dislocation density InP buffer on a V-grooved (001) Si substrate, implemented with a GaAs intermediate buffer and incorporation of InGaAs/InP SLSs, we realized a RT CW 1550 nm laser on Si. The InP buffer thickness is only 3.9 μm thick, which mitigates cracking and allows for practical solutions to incorporate lasers in the silicon photonics process that can couple efficiently to silicon waveguides. The fabricated ridge waveguide lasers yielded a reasonable RT CW lasing threshold (2.05 kA/cm$^2$) and a respectable output power of 18 mW/facet for devices without facet coating. The temperature-dependent measurements reported CW operation up to 65°C with reasonable characteristic temperature values. Pulsed measurements were carried out simultaneously to minimize the self-heating; these measurement results suggest that performance of the lasers on Si is limited by self-heating, which can be improved in future devices. The heat generation on Si is attributed to the larger series resistance and lower injection efficiency, compared to the laser on InP. The inferior heat dissipation on Si may also be due to the residual thermal stress of the InP-on-Si template, as well as the defective InP/GaAs interface. Future work will investigate these factors further. To improve performance, heavily doped n-type graded buffers could be utilized to further reduce the resistance and the impact of defects generated at the InP/GaAs interface. More systematic measurements and aging tests will also be conducted to evaluate the influence of an HR facet coating on device performance and lifetime.

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