Parallel Decoders of Polar Codes

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Abstract—In this letter, we propose parallel SC (Successive Cancellation) decoder and parallel SC-List decoder for polar codes. The parallel decoder is composed of $M = 2^m (m \geq 1)$ component decoders working in parallel and each component decoder decodes a Polar code of a block size of $1/M$ of the original Polar code. Therefore the parallel decoder has $M$ times faster decoding speed. Our simulation results show that the parallel decoder has almost the same error-rate performance as the conventional non-parallel decoder.

Index Terms—Polar codes, SC decoder, SC-LIST decoder

I. INTRODUCTION

Polar codes are a major breakthrough in coding theory [1]. They can achieve Shannon capacity with a simple encoder and a simple successive cancellation decoder, both with low complexity of the order of $O(N \log N)$, where $N$ is the code block size. When the code block size is long enough, the simple SC decoder can approaches Shannon capacity. But for short and moderate lengths, the error rate performance of polar codes with the SC decoding is not as good as LDPC or turbo codes. A new SC-List decoding algorithm was proposed for polar codes recently [2], which performs better than the simple SC decoder and performs almost the same as the optimal ML (maximum likelihood) decoding at high SNR. In order to improve the low minimum distance of polar codes, the concatenation of polar codes with simple CRC was proposed [2], and it was shown that a simple concatenation scheme of polar code (2048, 1024) with a 16-bit CRC using the SC-List decoding can outperform Turbo and LDPC codes [3][4].

Although Polar codes provide good error-rate performance, the SC and SC-List decoder work in a serial fashion. They decode information bits one-by-one. It is very hard to achieve a high decoding speed or low latency due to this serial decoding. Some work [5][6] has been on reducing the decoding latency of SC decoder of Polar codes by optimizing the hardware design of the SC decoder, and the improvement in the decoding speed is 2 times faster. In this letter, we propose both parallel SC and SC-List decoder to overcome this drawback. This parallel decoder consists of many component decoders which work in parallel, therefore we can achieve much higher decoding speed or much lower latency. Our improvement in the decoding speed is $M = 2^m (m \geq 1)$ times faster if $M$ component decoders are used. Simulations show that the parallel decoders provide the same error-rate performance as the conventional decoders.

In section II, we propose three parallel decoders with two component decoders, with four component decoders and with eight component decoders. We also provide simulation results. Finally we draw some conclusions in section III.

II. PARALLEL SC AND SC-LIST DECODERS

A. Polar Codes

Let $F = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}$, $F \otimes n$ is a $N \times N$ matrix, where $N = 2^n$, $\otimes n$ denotes $n$th Kronecker power, and $F \otimes n = F \otimes F^{(n-1)}$. Let the $n$-bit binary representation of integer $i$ be $b_{n-1}b_{n-2}...b_0$. The $n$-bit representation $b_{n-1}b_{n-2}...b_0$ is a bit-reversal order of $i$. The generator matrix of polar code is defined as $G_N = B_N F \otimes n$, where $B_N$ is a bit-reversal permutation matrix. The polar code is generated by

$$x_1^N = u_1^N G_N = u_1^N B_N F \otimes n$$

where $x_1^N = (x_1, x_2, ..., x_N)$ is the encoded bit sequence, and $u_1^N = (u_1, u_2, ..., u_N)$ is the encoding bit sequence. The bit indexes of $u_1^N$ are divided into two subsets: the one containing the information bits and the other containing the frozen bits. For simplicity, the frozen bits are set "0".

B. Parallel SC Decoder with Two Component Decoders

Due to the special structure of $F \otimes n$, Polar code can be expressed as

$$x_1^N = u_1^N B_N f = \begin{bmatrix} F_{00}(n-1) & 0 \\ F_{01}(n-1) & F_{10}(n-1) \end{bmatrix}$$

$$= \begin{bmatrix} v_{N/2}^N B_{N/2} & \cdots & v_{N/2}^N B_{N/2} \\ v_{N/2+1}^N B_{N/2+1} & \cdots & v_{N/2+1}^N B_{N/2+1} \end{bmatrix}$$

where $u_1^N B_N = \begin{bmatrix} v_{N/2}^N B_{N/2} & \cdots & v_{N/2}^N B_{N/2} \\ v_{N/2+1}^N B_{N/2+1} & \cdots & v_{N/2+1}^N B_{N/2+1} \end{bmatrix}$

Furthermore, we have

$$x_1^N = \begin{bmatrix} v_{N/2}^N B_{N/2} f & \cdots & v_{N/2}^N B_{N/2} f \\ v_{N/2+1}^N B_{N/2+1} f & \cdots & v_{N/2+1}^N B_{N/2+1} f \end{bmatrix}$$

where $v_{N/2}^N B_{N/2} = v_{N/2}^N B_{N/2}$ and $b_{N/2}^N = v_{N/2+1}^N B_{N/2+1}$.

From (3), we can see that one Polar code of block size $N$ can be decomposed into two sub Polar codes each with a block size of $N/2$, but the encoding bits $u_{N/2}^N$ and $b_{N/2}^N$ are correlated.
After passing \( x_i^N \) through a channel, we have the received signal \( y_i^N \). We propose a parallel SC decoder to decode the received signal as follows. The parallel SC decoder consists of two component SC decoders: one uses \( y_i^{N/2} \) as input to decode \( a_i^{N/2} \), and the other uses \( y_i^{N/2+1} \) as input to decode \( b_i^{N/2} \). Two SC decoders calculate log likelihood ratios: \( L_{N/2}^{(i)}(y_i^{N/2}, a_i^{N/2-1}) \) and \( L_{N/2}^{(i)}(y_i^{N/2+1}, b_i^{N/2-1}) \) independently as follows

\[
L_{N/2}^{(i)}(y_i^{N/2}, a_i^{N/2-1}) = \log \frac{W_i^{(0)}(y_i^{N/2}, a_i^{N/2-1}, |a_i = 0)}{W_i^{(1)}(y_i^{N/2}, a_i^{N/2-1}, |a_i = 1)}
\]

\[
L_{N/2}^{(i)}(y_i^{N/2+1}, b_i^{N/2-1}) = \log \frac{W_i^{(0)}(y_i^{N/2+1}, b_i^{N/2-1}, |b_i = 0)}{W_i^{(1)}(y_i^{N/2+1}, b_i^{N/2-1}, |b_i = 1)}
\]

The decision on \( a_i \) and \( b_i \) is made either independently or jointly. If both \( v_i \) and \( v_{N/2+i} \) are information bits, then \( a_i = v_i \oplus v_{N/2+i} \) and \( b_i = v_{N/2+i} \) are independent from each other and decisions are made independently as

\[
\hat{a}_i = \begin{cases} 0, & \text{if } L_{N/2}^{(i)}(y_i^{N/2}, a_i^{N/2-1}) \geq 0 \\ 1, & \text{otherwise} \end{cases}
\]

\[
\hat{b}_i = \begin{cases} 0, & \text{if } L_{N/2}^{(i)}(y_i^{N/2+1}, b_i^{N/2-1}) \geq 0 \\ 1, & \text{otherwise} \end{cases}
\]

If both \( v_i \) is a frozen bit and \( v_{N/2+i} \) is an information bit, then \( a_i = b_i = v_{N/2+i} \), an equal gain combing of the log likelihood ratios is used to decode:

\[
\hat{a}_i = \begin{cases} 0, & \text{if } L_{N/2}^{(i)}(y_i^{N/2}, a_i^{N/2-1}) + L_{N/2}^{(i)}(y_i^{N/2+1}, b_i^{N/2-1}) \geq 0 \\ 1, & \text{otherwise} \end{cases}
\]

Fig. 1 shows the parallel decoder structure. Since the two component SC decoders operate decoding in parallel, the decoding speed of this parallel decoder is two times faster than the conventional SC decoder.

![Fig. 1 The Proposed Parallel SC Decoder with Two Component Decoders](image)

\[ x_i^N = u_i^N B_N \times \begin{bmatrix} F_B^{(0)N-2} & 0 & 0 & 0 \\ 0 & F_B^{(0)N-2} & 0 & 0 \\ 0 & 0 & F_B^{(0)N-2} & 0 \\ 0 & 0 & 0 & F_B^{(0)N-2} \end{bmatrix} \]

where

\[
\begin{align*}
(a_i, b_i, c_i, d_i) &= \left\{ \begin{array}{ll}
1 & \text{if } L_i = L_i^{(i)}(y_i^{N/2}, a_i^{N/2-1}) + L_i^{(i)}(y_i^{N/2+1}, b_i^{N/2-1}) \geq 0 \\
0 & \text{otherwise}
\end{array} \right.
\end{align*}
\]

Fig. 2 The Proposed Parallel SC Decoder with Four Component Decoders.
D. Parallel SC Decoder with Eight Component Decoders

Straightforwardly, let
\[ u^n_B = [v^{N/8}_1 B_{N/8}, v^{2N/8}_1 B_{N/8} \cdots v^{N}_1 B_{N/8}] \]

We have
\[ x^{N/8}_i = d^{N/8}_i B_{N/8} F_{\theta (n-3)} \]
\[ x^{2N/8}_i = d^{2N/8}_i B_{N/8} F_{\theta (n-3)} \]
\[ \vdots \]
\[ x^{N}_i = d^{N}_i B_{N/8} F_{\theta (n-3)} \]

where
\[ d^{N/8}_i = v^{N/8}_i \oplus v^{2N/8}_i \oplus \cdots \oplus v^{N}_i \oplus v^{N/8}_i \]
\[ d^{2N/8}_i = v^{2N/8}_i \oplus v^{2N/8}_i \oplus \cdots \oplus v^{N}_i \oplus v^{N/8}_i \]
\[ \vdots \]
\[ d^{N}_i = v^{N}_i \oplus v^{N}_i \oplus \cdots \oplus v^{N}_i \oplus v^{N/8}_i \]

From (14), we can obtain a parallel SC decoder with eight component SC decoders as shown in Fig. 3.

From (15), we can obtain a parallel SC decoder with eight component SC decoders as shown in Fig. 3.

E. Parallel SC-List Decoder with Two Component Decoders

We propose a parallel SC-List decoder to decode the received signal as shown in Fig. 4. The parallel SC decoder consists of two component SC-List decoder: decoder A uses \( y^{N/4}_1 \) as input to decode \( a^{N/4}_i \), and decoder B uses \( y^{N/2}_i \) as input to decode \( b^{N/2}_i \). Each path \( P_m = [A_m, B_m] \) (1 \( \leq m \leq L \)) consists of two sub-paths: \( A_m = [\hat{a}_{m1}, \hat{a}_{m2}, \cdots, \hat{a}_{m,k-1}] \) for the decoder A and \( B_m = [\hat{b}_{m1}, \hat{b}_{m2}, \cdots, \hat{b}_{m,k-1}] \) for the decoder B. At decoding time \( k \), the decoder A generates 2\( L \) new paths: \( \{A_m, \hat{a}_{m,k} = 0\} \) and \( \{A_m, \hat{a}_{m,k} = 1\} \) (1 \( \leq m \leq L \)), and the decoder B generates 2\( L \) new paths: \( \{B_m, \hat{b}_{m,k} = 0\} \) and \( \{B_m, \hat{b}_{m,k} = 1\} \) (1 \( \leq m \leq L \)). We generate L/2L/4L combined paths according to \( (v_k, v_{k+N/2}) \) as follows: 1) If both \( v_k \) and \( v_{k+N/2} \) are frozen bits, then \( \hat{a}_k = \hat{b}_k = 0 \) and L combined paths are generated as \( \{A_m, B_m, \hat{a}_{m,k} = 0, \hat{b}_{m,k} = 0\} \) (1 \( \leq m \leq L \)); These L paths are split into two groups: \( \{A_m, \hat{a}_{m,k} = 0\} (1 \leq m \leq L) \) for the decoder A and \( \{B_m, \hat{b}_{m,k} = 0\} (1 \leq m \leq L) \) for the decoder B. 2) If \( v_k \) is a frozen bit and \( v_{k+N/2} \) is an information bit, then \( \hat{a}_k = \hat{b}_k = v_{k+N/2} \) and we generate 2L combined paths: \( \{A_m, B_m, \hat{a}_{m,k} = 0, \hat{b}_{m,k} = 0\} \) and \( \{A_m, B_m, \hat{a}_{m,k} = 1, \hat{b}_{m,k} = 1\} (1 \leq m \leq L) \); The path metrics of the combined path \( \{A_m, B_m, \hat{a}_{m,k}, \hat{b}_{m,k}\} \) is the sum of path metrics of path \( \{A_m, \hat{a}_{m,k}\} \) and path \( \{B_m, \hat{b}_{m,k}\} \). 3) If both \( v_k \) and \( v_{k+N/2} \) are information bits, 4L combined paths are generated as \( \{A_m, B_m, \hat{a}_{m,k}, \hat{b}_{m,k}\} = v_k \oplus v_{k+N/2}, \hat{b}_{m,k} = v_{k+N/2}\) , where \( v_k, v_{k+N/2} \in \{0,1\}\); If the number of combined paths is larger than a predefined threshold \( L_{max} \), \( L_{max} \) best combined paths are kept. We choose \( L_{max} = L \) in Fig. 4. Each combined path is split into two sub-paths with one for the decoder A and one for the decoder B.

\[ L \text{ survival paths:} \{\hat{a}_{m1}, \hat{a}_{m2}, \cdots, \hat{a}_{m,k}\}\text{ }\text{ }\text{1 \leq m \leq L}\]

\[ L \text{ survival paths:} \{\hat{b}_{m1}, \hat{b}_{m2}, \cdots, \hat{b}_{m,k}\}\text{ }\text{1 \leq m \leq L}\]

\[ L \text{ survival paths:} \{\hat{a}_{m1}, \hat{a}_{m2}, \cdots, \hat{a}_{m,k}\}\text{ }\text{1 \leq m \leq L}\]

\[ L \text{ survival paths:} \{\hat{b}_{m1}, \hat{b}_{m2}, \cdots, \hat{b}_{m,k}\}\text{ }\text{1 \leq m \leq L}\]

Fig. 4 The Proposed SC-List decoder with Two Component Decoders.

F. Parallel SC-List Decoder with Four Component Decoders

We propose a parallel SC-List decoder to decode the received signal as shown in Fig. 5. The parallel SC decoder consists of four component SC-List decoders A/B/C/D: They use \( y^{N/4}_1, y^{N/2}_1, y^{3N/4}_1 \) and \( y^{N/4}_1 \) as inputs to decode \( a^{N/4}_i, b^{N/4}_i, c^{N/4}_i \) and \( d^{N/4}_i \), respectively. Each path \( P_m = [A_m, B_m, C_m, D_m] (1 \leq m \leq L) \) consists of four sub-paths: \( A_m = [\hat{a}_{m1}, \hat{a}_{m2}, \cdots, \hat{a}_{m,k-1}] \) for the decoder A, \( B_m = [\hat{b}_{m1}, \hat{b}_{m2}, \cdots, \hat{b}_{m,k-1}] \) for the decoder B, \( C_m = [\hat{c}_{m1}, \hat{c}_{m2}, \cdots, \hat{c}_{m,k-1}] \) and \( D_m = [\hat{d}_{m1}, \hat{d}_{m2}, \cdots, \hat{d}_{m,k-1}] \) for the decoder A, B, C and D, respectively. At decoding time \( k \), each decoder produces 2L new paths. We generate L/2L/4L/8L/16L combined paths according to all combinations by taking different values of information bits in \( (v_k, v_{k+N/4}, v_{k+N/2}, v_{k+3N/4}) \), and for each combination, \( \{\hat{a}_{m,k}, \hat{b}_{m,k}, \hat{c}_{m,k}, \hat{d}_{m,k}\} \) is calculated as follows: \( \hat{a}_k = \hat{v}_k \oplus \hat{v}_{k+N/4} \oplus \hat{v}_{k+N/2} \oplus \hat{v}_{k+3N/4}\), \( \hat{b}_k = \hat{v}_{k+N/4} \oplus \hat{v}_{k+3N/4}\), \( \hat{c}_k = \hat{v}_{k+N/4} \oplus \hat{v}_{k+3N/4}\), \( \hat{d}_k = \hat{v}_{k+N/4} \oplus \hat{v}_{k+3N/4}\).
\[ \hat{c}_k = \hat{v}_{k+3N/4} \oplus \hat{v}_{k+3N/4} \text{ and } \hat{d}_k = \hat{v}_{k+3N/4} \cdot \]

Let \( w \) be the number of information bits in \((v_k, v_{k+N/4}, v_{k+2N/4}, v_{k+3N/4})\), the number of the generated combined paths is \( 2^w L \). Since \( w \in \{0,1,2,3,4\} \), \( 2^w \in \{1,2,4,8,16\} \). If \( 2^w L > L_{\text{max}} \), the \( L_{\text{max}} \) best paths are kept, and these \( L_{\text{max}} \) paths are split into \( 4L_{\text{max}} \) sub-paths for the decoder A, B, C and D. We choose \( L_{\text{max}} = L \) in Fig. 5.

![Fig. 5 The Proposed SC-LIST decoder with Four Component Decoders.](image)

**G. Performance Simulations**

Fig. 6 shows bit error rate (BER) and frame error rate (FER) of Polar code (2048,1024) with the conventional SC decoding and our proposed parallel SC decoding. Fig. 7 shows BER and FER of Polar code (2048,1008) with 16-bit CRC using the conventional SC-LIST and our proposed parallel SC-LIST decoding, where the list size is \( L_{\text{max}} = 32 \) and the adaptive list algorithm[4] is used. It is shown that the parallel decoders perform almost the same as the conventional non-parallel decoder for both the SC and the SC-LIST decoding.

![Fig. 6 The error-rate performance of polar code (2048, 1024) with the conventional SC and our proposed parallel SC decoding.](image)

![Fig. 7 The error rates of polar code (2048, 1008) with 16-bit CRC using the conventional SC-List and our proposed parallel SC-List decoding.](image)

**III. CONCLUSION**

In this letter, we propose parallel SC and SC-LIST decoder which are composed of \( M = 2^w (m \geq 1) \) component decoders working in parallel. The proposed parallel decoder can provide \( M \) times faster decoding speed than the conventional decoder. Since each component decoder decodes a Polar code with a block size \( N/M \), the decoding complexity of each component decoder is in order of \( O(N/M \log(N/M)) \) for the SC decoder and in order of \( O((LN/M) \log(N/M)) \) for the SC-LIST decoder. The overall complexity of the whole parallel decoder is in order of \( O(N \log(N/M)) \) for the SC decoder and in order of \( O(LN \log(N/M)) \) for the SC-LIST decoder, which is less than the conventional SC and the SC-LIST decoder, respectively. Our simulation results show that the parallel decoders perform almost the same as the conventional non-parallel decoders.

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