Systematic Unsupervised Recycled Field-Programmable Gate Array Detection

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Abstract—With the expansion of the semiconductor supply chain, the use of recycled field-programmable gate arrays (FPGAs) has become a serious concern. Several methods for detecting recycled FPGAs by analyzing the ring oscillator (RO) frequencies have been proposed; however, most assume the known fresh FPGAs (KFFs) as the training data in machine-learning-based classification. In this study, we propose a novel recycled FPGA detection method based on an unsupervised anomaly detection scheme when there are few or no KFFs available. As the RO frequencies in the neighboring logic blocks on an FPGA are similar because of systematic process variation, our method compares the RO frequencies and does not require KFFs. The proposed method efficiently identifies recycled FPGAs through outlier detection using direct density ratio estimation. Experiments using Xilinx Artix-7 FPGAs demonstrate that the proposed method successfully distinguishes recycled FPGAs from 35 fresh FPGAs. In contrast, a conventional recycled FPGA detection method results in certain misclassification.

Index Terms—Recycled FPGA detection, Ring oscillator, Process variation, Unsupervised outlier detection, Direct density ratio estimation

I. INTRODUCTION

W ith the rapid progress of integrated circuit (IC) supply chain globalization, the distribution of recycled ICs in the market as new products has become a serious concern [1], [2]. Among the various ICs, field-programmable gate array (FPGA) is of particular interest for recycling because of the increase in distribution owing to the growing demand for deep-learning applications [3]–[5]. Manufacturers cannot guarantee their reliability due to aging degradation induced by previous usage. Therefore, recycled FPGAs not only result in economic loss but also cause serious problems, particularly when used in mission-critical applications such as automobiles and medical equipment.

Various recycled FPGA detection methods have been proposed [6]–[10]. The general idea behind these methods involves the analysis of the aging-induced degradation of circuit characteristics using the ring oscillator (RO) frequency. The RO frequencies of fresh units are measured and used to train a machine learning model. As these frequencies degrade with usage, the trained model can classify the FPGA under test (FUT) as fresh or recycled. These methods [6]–[9] assume the presence of known fresh FPGAs (KFFs). For accurate classification through machine learning algorithms, FPGA manufacturers need to measure a large volume of KFFs. If there are less KFFs available, these methods may not work properly.

To meet this requirement, an unsupervised recycled FPGA detection method was proposed in [10]. However, because this method uses the measured frequencies as the input vector for the k-means++ clustering algorithm [11] as is, its classification accuracy remains limited because of process variation. Besides, the characterized logic blocks for RO measurement must be carefully selected because the classification accuracy is poor if they are inappropriate and/or insufficient for the measurement.

Herein, we propose a novel method for detecting recycled FPGAs independent of KFF by comparing the frequencies on neighboring logic blocks. The key concept of the proposed method is shown in Fig. 1. When designing ROs in each logic block and calculating the probability density functions (PDFs) of these frequencies in each column, the frequency distributions of neighboring columns ideally match because of the systematic component of the process variation [12], [13]. However, this assumption does not hold if there is degradation due to aging on one side. The proposed method removes the need for KFFs by exhaustively comparing all the neighboring ROs. Based on the similarity of the compared frequencies, recycled FPGAs are detected through direct density ratio estimation [14] formulated as unsupervised anomaly detection. We would like to note that the proposed method not only has the advantage of not requiring KFFs but also can complement the classification results of the conventional supervised methods when KFFs are available.

This manuscript is based on our previous work [15]. While our previous evaluation insufficiently uses 10 FPGAs with a small benchmark circuit under a single aging scenario, a more practical evaluation is provided to show the effectiveness of the proposed method by increasing the number of FPGAs to 35.
and using RISC-V [16] under various aging scenarios. The 35 FPGAs used in experiments were manufactured in different lots and the experiments using them show the applicability of the proposed method to FPGAs having various initial process variations. RISC-V has been very attracting attention in recent years, and many implementations on FPGA have been reported. By using the processor, we evaluate the proposed method under the more practical and possible scenario. The various aging scenarios contain a short aging time, and the experimental results clarify the performance limit of the proposed method experimentally, that is how long the recycled/aging time on FPGA can be detected by the proposed method.

The main contributions of this paper are summarized as:

- Taking advantage of the fact that ROs in adjacent blocks have similar frequencies, we formulate an efficient detection scheme using an unsupervised outlier detection method through self-referencing based on density ratio estimation.
- Silicon measurement results using 35 commercial FPGAs demonstrate the proposed method successfully detected the aged FPGAs, excluding FPGAs with very short aging time, and could successfully classify fresh FPGAs. In contrast, the conventional method [10] fails to detect the aged FPGAs.

The remainder of this paper is structured as follows. In Section II, we review an existing unsupervised recycled FPGA detection method. In addition, we explain the direct density ratio estimation, which is used as an unsupervised outlier detection algorithm in the proposed method. Section III describes the proposed recycled FPGA detection method. The experimental procedure and silicon measurement results using commercial FPGAs are discussed in Section IV. Finally, we conclude our paper in Section V.

II. PRELIMINARIES

A. Conventional method

In [10], an unsupervised FPGA detection method has been proposed, which we briefly review as the conventional method. This method involves two steps: RO frequency measurement and outlier detection based on an unsupervised machine learning algorithm using the measured frequencies. If the FPGA has been previously used, the RO frequencies will degrade because of aging mechanisms, such as bias temperature instability (BTI) [17], hot carrier injection (HCI) [18], and time-dependent dielectric breakdown (TDBB) [19]. Suspicious FPGAs thus can be detected through unsupervised outlier detection by capturing the aging effect.

The general structure of an FPGA is depicted in Fig. 2. It includes several lookup tables (LUTs) in one configurable logic block (CLB), which can be used to design a multistage RO within a single CLB. In the design, as one LUT corresponds to one stage, an odd-number-stage RO can be configured.

In [10], an exhaustive LUT path measurement (hereafter called XP) has been proposed, enabling the analysis of all the LUT paths by appropriately setting the LUT input value and using XOR and XNOR gates for the RO stage. For a z-input LUT, \(2^{z-1}\) paths can be configured. In Fig. 2 a three-input LUT \(I_0, I_1, I_2\) is used as an example, where four \(= 2^{3-1}\) paths can be analyzed. After the measurement, the FUTs are tested using an unsupervised outlier detection method based on the measured frequencies. In [10], k-means++ clustering is exploited to partition the measured frequencies. If the FUT has been recycled, the number of clusters is more than that of a fresh one with a distance. To quantitatively evaluate the distance, the silhouette value [20] is introduced in [10].

All the LUT paths in the CLBs are completely covered in XP measurement, whereas the tested CLBs are carefully selected for the successful application of k-means++ clustering. More importantly, because the raw values of the measured frequencies that will be affected by process variation are used as the input vector for k-means++ clustering, this method may fail to detect recycled FPGAs.

B. Anomaly detection via direct density ratio estimation

In this subsection, we explain the core idea of a direct density ratio estimation [21], as used in our proposed method. This process is a well-established algorithm for robust outlier detection, and it is performed based on the non-similarity of the two vectors with \(n\) elements, \(f = \{f_1, f_2, \cdots, f_n\}\) and \(f' = \{f'_1, f'_2, \cdots, f'_n\}\), which are the inlier data and tested data (i.e., suspicious data), respectively. Although direct density ratio estimation can work even when the numbers of elements in \(f\) and \(f'\) are unmatched, the number of elements in both vectors is set to \(n\) for the sake of simplicity in this paper. By evaluating the data as vector, the noise in each sample can be suppressed, and the systematic features in the vectors can be effectively clarified. Furthermore, the detection sensitivity is considerably higher than the comparison of each element (i.e., residual), even when the probability of outliers in \(f'\) is small.

In the direct density ratio estimation, the non-similarity is modeled as the anomaly score \(a(\cdot)\) which is represented as the log-arithmetic of the density ratio as follows:

\[
a(f) = -\log r(f),
\]

Fig. 2. Typical FPGA structure. A multistage RO can be designed in a single CLB using multiple LUTs. By setting \(I_1 = 1\) and \(I_2 = 0\), the SRAM values are propagated, and the highlighted LUT path oscillates. The XP measurement enables the characterization of all the LUT paths [10].
where $r(\cdot)$ is the density ratio function and is represented as:

$$r(f) = \frac{p'(f)}{p(f)}. \quad (2)$$

Here, $p(\cdot)$ and $p'(\cdot)$ are the probability density functions of $f$ and $f'$, respectively. When $f$ is an outlier, $a(f)$ goes higher.

It is necessary to obtain the density ratio function $r(f)$ based on the given vectors as shown in Eq. (2). Because the direct solution of $r(\cdot)$ involves a division operation, the error can be large. To address this issue, several methods have been proposed to estimate $r(\cdot)$ without obtaining the probability distribution of $p(\cdot)$ and $p'(\cdot)$, such as Kullback-Leibler importance estimation procedure (KLIEP) \cite{22} and the least-squares importance fitting (LSIF) \cite{23}. In our proposed detection method, $r(\cdot)$ is estimated using the unconstrained LSIF (uLSIF) \cite{21}, which achieves the best performance among the density ratio estimation methods.

In the uLSIF, the density ratio function is approximated as a linear importance model:

$$\hat{r}(f) = \sum_{l=1}^{n} \alpha_l \varphi_l(f), \quad (3)$$

where $\alpha_l$ and $\varphi_l(f)$ are the fitting parameter and non-negative basis function, respectively. Here, we consider the radial basis function (RBF) kernel as the basis function:

$$\varphi_l(f) = K(f, f_l') = \exp \left( -\frac{||f - f_l'||^2}{2w^2} \right), \quad (4)$$

where $w$ is the bandwidth. The fitting parameters, $\alpha (= \alpha_1, \alpha_2, \ldots, \alpha_n)$, are calculated so as to minimize the squared error of $r(f)$ and $\hat{r}(f)$, $J_0$, which is expressed as

$$J_0(\alpha) := \frac{1}{2} \int (\hat{r}(f) - r(f))^2 p(f) df$$

$$\begin{align*}
&= \frac{1}{2} \int \hat{r}(f)^2 p(f) df - \int \hat{r}(f) p'(f) df \\
&\quad + \frac{1}{2} \int r(f)^2 p(f) df.
\end{align*} \quad (5)$$

In Eq. (5), the third term can be ignored because it is constant. Through empirical optimization, an approximation problem can be formulated as follows:

$$\min_{\{a_l\}_{l=1}^{n}} \left[ \frac{1}{2} \sum_{l=1}^{n} a_l^2 \hat{H}_{l,l} - \sum_{l=1}^{n} a_l \hat{h}_l + \frac{1}{2} \sum_{i=1}^{n} a_i^2 \right], \quad (6)$$

where

$$\hat{H}_{l,l} := \frac{1}{n} \sum_{i=1}^{n} K(f_i, f_l') K(f_i, f_l') \quad \text{and} \quad (7)$$

$$\hat{h}_l := \frac{1}{n} \sum_{j=1}^{n} K(f_j, f_l'). \quad (8)$$

In Eq. (6), $\frac{1}{2} \sum_{i=1}^{n} a_i^2$ is a regularization term. The solution $\tilde{\alpha}$ is analytically given by

$$\tilde{\alpha} = (\tilde{a}_1, \tilde{a}_2, \ldots, \tilde{a}_n)^T = (\hat{H} + \lambda I)^{-1} \hat{h}, \quad (9)$$

where $I$ and $\hat{h}$ are an $n$-dimensional identity matrix and a vector of $\hat{h}_l$, respectively. Note that, since elements of $\tilde{\alpha}$ can take negative values, it must be modified as

$$\tilde{a}_l = \max(0, \tilde{a}_l) \text{ for } l = 1, 2, \ldots, n. \quad (10)$$

Thus, the probability density ratio $r(\cdot)$ can be directly estimated, and the anomaly score vector $a = (a(f_1), a(f_2), \ldots, a(f_n))$ for each element of $f$ and $f'$ can be calculated using Eq. (1). Further, binary classification is performed using the anomaly score.

The primary advantage of the uLSIF over the KLIEP and LSIF is that the fitting parameters $w$ and $\lambda$ can be analytically calculated through leave-one-out cross-validation (LOOCV) using Eq. (5).

### III. Proposed Method

We propose a novel unsupervised method for detecting recycled FPGAs to realize better detection accuracy. The proposed method also utilizes the measured RO frequencies and classifies FUTs as either recycled or fresh. The distinction from the conventional KFF-free method is that the necessity of the KFF set is removed by comparing neighboring frequencies to effectively classify the FUTs. In addition, the RO analysis is exhaustively carried out for all the LUT paths of all the CLBs to avoid omission using a technique, called called X-FP measurement and proposed in \cite{9}. For classification, self-referencing outlier detection is formulated based on the uLSIF algorithm.

The proposed method is based on an unsupervised anomaly detection framework utilizing the uLSIF introduced in Section II-B. In contrast to the supervised methods such as \cite{6, 9}, the proposed method requires no golden samples and works well when the amount of golden samples is either limited or nonexistent. In addition, we would like to note that the proposed method is applicable to various commercial FPGAs. The proposed method assumes that the target FPGAs have the typical structure shown in Fig. 2. Although the proposed method also requires a design environment in which ROs can be configured for each LUT in order to measure frequency fingerprint as in \cite{9}, it can be realized by using an open-source design environment described in \cite{24}.

#### A. Key idea

For manufactured ICs, the process variation can be decomposed into random and systematic components \cite{12, 13}. The former is caused by physical phenomena such as random dopant fluctuation and is often modeled as a normal distribution with zero mean. Meanwhile, the latter is a gradual spatial variation in the die and modeled as a polynomial of the die coordinates $(x, y)$, where $x$ and $y$ are the position coordinate on an FPGA. The systematic components of the neighboring locations are similar because the frequencies of the neighboring ROs are ideally matched, which suggests that comparing the frequencies of adjacent CLBs also helps in eliminating the need for KFFs.
the RO frequencies are compared with the adjacent column, as shown in Fig. 2. In this example, $f_1$ is compared with $f_2$, $f_3$ with $f_4$, and $f_5$ with $f_6$. However, modern FPGAs have several block RAMs (BRAMs) and multipliers between the logic block areas; hence, anomaly score calculation is not carried out across them (for example, $f_3$ with $f_5$) as no similarity is guaranteed because of the distance between the columns.

The two frequency vectors of neighboring columns are inputted to the uLSIF as $f$ and $f'$ for calculating the anomaly scores. Given all the comparison combinations, the uLSIF returns the anomaly scores for each calculation, for example, $M$ scores are obtained as $A = \{a_1, a_2, \ldots, a_M\}$, when $M$ comparisons are made. It should be noted that the comparisons perform in the same LUT paths configuration because each path may have a different frequency trend. Therefore, the uLSIF procedure is iterated for all the LUT paths, in this case, $2^{\text{width}}$ times per one FPGA.

3) Classification: Finally, the FUT is classified as fresh or recycled based on the anomaly scores. If the FUT was used previously, large scores should be observed. However, it might be difficult to separate the scores for short usage. In this case, a fresh/recycled threshold can be determined if the information of a KFF set is available, but note that the data volume is very little as with [10].

IV. EXPERIMENTAL

To demonstrate the effectiveness of the proposed method, we conducted experiments using the Xilinx Artix-7 FPGA (XC7A35T-ICPG236C) [25]. Based on the measurement results, the proposed recycled FPGA detection method was compared to the conventional method presented in [10]. We used 35 FPGAs (FPGA-01 to FPGA-35) for this experiment. We here note that the 35 FPGAs were manufactured in different production lots because bought from different distributors at different timings. Since the proposed method relies on the feature of the systematic component of the process variation, it is important to evaluate FPGAs with various process variations between lots.

A. Setup

In the floorplan of the Artix-7 depicted in Fig. 5, most of the area is occupied by CLBs, and there is some empty space area with no logic resource. In addition, columns of BRAMs can
be found. An on-chip measurement system with 15-stage of ROs (two CLBs) was implemented using eight LUTs on the Artix-7 CLB. The RO was designed using XNOR or XOR logic gates. An Artix-7 FPGA has 6-input LUTs, and in the configuration of RO using XNOR or XOR, which make a total of 32 (= 2⁶⁻¹) LUT paths (path-0 to path-31) can be measured for each CLB. A total of 42,112 ROs were placed on a geometric grid, and their frequencies were measured using a counter circuit. By retaining the same internal routing through the hardware macro modeling function of Vivado (Xilinx CAD tool) [26], the logic resources and structure for each RO were placed in two CLBs such that the frequency variation caused by the difference in internal routing can be minimized. In the layout, 10 comparisons were made (M = 10) because of a couple of BRAM columns. The heatmaps of the measured frequencies of path-2 and path-4 for the fresh FPGA-01 and FPGA-02 are shown in Figs. 6 and 7. It can be observed that the frequency distributions in the fresh and aged fingerprints have a smooth variation along with the coordinates and are differing frequencies.

In the experiments, nine FPGAs (FPGA-01 to FPGA-09) were aged and used as the recycled FPGAs among the 35 FPGAs employed for testing as listed in Table I. The s9234 benchmark circuit [27] and a RISC-V processor run as a user circuit on the nine FPGAs for FPGA-01 to FPGA-05 and FPGA-06 to FPGA-09, respectively. While running the circuits, the FPGAs were heated up to 135 °C using a Peltier module with a thermal controller, as shown in Fig. 8, to accelerate the aging process. In the measurement schedule, measurements were made after a five-day recovery phase. The actual FPGA running time relative to the degradation time due to thermal acceleration can be estimated from the usage conditions of the thermal device [29]. The thermal acceleration factor $F_T$ can be calculated as [30]:

$$F_T = e^{\frac{E_a}{k} \left( \frac{1}{T_{op}} - \frac{1}{T_{stress}} \right)},$$

1The verilog code for the X-FP measurement is available at https://github.com/yuya-isaka/X-FP.
2The RISC-V environment is available at https://github.com/yuya-isaka/RV32.
where, the activation energy $E_a = 0.5 \text{ eV}$, Boltzmann constant $k = 8.62 \times 10^{-5} \text{ eV/K}$, nominal operating temperature $T_{op} = 313 \text{ K (40°C)}$, and stress temperature $T_{stress} = 408 \text{ K (135°C)}$, respectively. Note that it is difficult to accurately estimate the actual operating time since our experiment’s degradation schedule includes a recovery phase. We can roughly estimate the accelerated aging of 6, 3, 2, and 1 h as the actual operating time of 18, 9, 6, and 3 d, respectively.

Note that a similar aging acceleration was conducted for 24 h in [9]. With their study, it is difficult to accurately detect the aged FPGAs, even by the previous method based on a set of KFFs. Although a similar aging acceleration method using a temperature controller was performed in [10], the degradation in their method was greater because they did not consider a recovery phase. In our experiment, a recovery phase of over four days was included to reflect a realistic scenario in the recycling of FPGAs. In addition, the aging time was longer than that of our method. Therefore, the recycled FPGA detection method undertaken in our study is a greater challenge than the other previous works [9], [10].

We implemented the uLSIF and $k$-means++ clustering in the Python language.

B. Results

1) Measurement results: First, we presented the anomaly scores obtained from our proposed method. Fig. 10 displays the results of the five aged FPGAs of s9234 (FPGA-01 to FPGA-05) and fresh FPGAs (FPGA-01 to FPGA-35). The horizontal axis represents path IDs; from path-0 to path-31. The maximum anomaly score of the 10 comparisons (that is, $\max_M(A)$ for each path) for the 32 LUT paths is also represented. For example, in Fig. 10(a) while the anomaly scores for the fresh FPGAs ranged from 1.0 to 10.0, several remarkably high anomaly scores (such as, above 20) were observed for the 6-h aged FPGAs. The increase from 1.0 to 10.0 comes from the random component in the process variation. Here, we noted that the shorter the aging time, the lower the anomaly scores. Since high anomaly scores are observed in Figs. 10(a), 10(b), and 10(c), it is expected that the aged FPGAs are accurately detected. However, it is not easy to detect the 1-h aged shown in Fig. 10(d) because the anomaly scores of recycled and fresh one are almost the same.

Similarly, Fig. 11 shows the results of the four aged FPGAs of the RISC-V processor (FPGA-06 to FPGA-09) and fresh FPGAs. Even with these results, the obvious abnormal scores were observed for the 6-h, 3-h, and 2-h aged FPGAs, the anomaly score of the 1-h aged FPGA was almost equal to the fresh ones and we found it difficult to identify the difference caused by the aging.

Fig. 12 depicts the frequency heatmaps of FPGA-01 and
Fig. 13. Frequency heatmaps of the residual frequencies of the column comparison for the aged FPGA-01 to FPGA-05.

FPGA-02 when fresh, respectively. In the heatmaps, the residuals of the two columns are shown using the coordinates of the RO on the left-hand side in the compared column. The paths with the highest scores in Fig. 10 are shown. As expected, because the frequencies in the neighboring columns are similar, those residuals are almost zero. Although some of the fresh FPGAs, such as FPGA-03 and FPGA-04, are not included, similar results can be obtained.

In Fig. 13 the residual heatmaps of the aged FPGA-01 to FPGA-05 are shown, where the paths with the highest anomaly scores in Fig. 11 are shown. From the figures, the aging effect is observed in the lower right area where the s9234 benchmark circuit is located, for example, a notable difference of 6 MHz can be observed in Fig. 13(a). However, in Fig. 13(e) there is no significant difference in the residuals between the fresh and the aged cases. Fig. 14 also shows the frequency heatmaps of the highest scores of the four aged FPGAs with the RISC-V processor (FPGA-06 to FPGA-09). From the figures, we can see a similar result with Fig. 13. Note that the aging effect in the wider area was confirmed because the RISC-V processor has a larger circuit area than the s9234 circuit as shown in Figs. 14(a) and 14(b). This suggests that our proposed method works effectively even in large-scale circuits that require the full use of FPGA resources.

2) Recycled FPGA detection: Finally, the accuracy of our proposed detection method was evaluated using the anomaly scores. The receiver operating characteristic (ROC) curve is represented by Fig. 15 and shows the classification result of the proposed method. In the ROC curves, the horizontal and vertical axes express the misclassification result for the 35 fresh FPGAs and correct classification result for the aged FPGAs, i.e., the upper left corner of the ROC curves corresponds to the best result as highlighted in Fig. 15.

As shown in Fig. 15(a) the proposed method can detect the aged FPGAs with s9234 while failing to detect one aged FPGA. The proposed method detected the aged FPGAs with the RISC-V processor without misclassification as shown in Fig. 15(b). In Fig. 15(a), the undetected FPGA is the 1-h aged FPGA (FPGA-05) as expected from the discussion of Fig. 10(d). Although it may be difficult to detect the 1-h aged FPGA-08 in practical use, the FPGA can be detected by setting a fresh/recycled threshold if the information on KFFs is available as with [10]. From these results, we conclude that the proposed method detected a recycled FPGA regardless of
the cluster number for the values in bold point to the optimal number. For the fresh FPGAs, the average of the silhouette values is represented. In our study, the optimal cluster number. For the fresh FPGAs, the average of the silhouette values is represented. In our study, the optimal cluster number.

| 2 cluster | 3 cluster | 4 cluster |
|-----------|-----------|-----------|
| 35 fresh FPGAs | 0.557 | 0.522 | 0.518 |
| 6-h aged FPGA-01 | 0.622 | 0.613 | 0.592 |
| 6-h aged FPGA-02 | 0.625 | 0.611 | 0.591 |
| 3-h aged FPGA-03 | 0.562 | 0.549 | 0.548 |
| 2-h aged FPGA-04 | 0.545 | 0.529 | 0.527 |
| 1-h aged FPGA-05 | 0.553 | 0.525 | 0.520 |
| 6-h aged FPGA-06 | 0.611 | 0.593 | 0.585 |
| 3-h aged FPGA-07 | 0.627 | 0.614 | 0.580 |
| 2-h aged FPGA-08 | 0.554 | 0.531 | 0.524 |
| 1-h aged FPGA-09 | 0.555 | 0.531 | 0.523 |

The detection performance of the conventional method depends on the CLB selection. To demonstrate the best performance by the conventional method, all the RO configurations were used for the recycled FPGA detection. Table II shows the silhouette values for each cluster as with Table I. As a result, the optimal number of the clusters remained 2 in all the cases. We found it difficult to distinguish between frequency fluctuations caused by the process variation and those by aging degradation, nor did the clustering algorithm work accurately.

In spite of demonstrating a good result in the paper of [10], the conventional method could not detect the recycled FPGAs in our experiment. We consider this comes from the difference in the experimental conditions. Although similar aging acceleration equipment was used in the experiments of [10], the aging schedule did not contain the recovery phase. Meanwhile, in our experiment, the recovery phase of more than 4 days was added considering a realistic scenario of recycled FPGAs in the market. Thus, it can be considered that the recycled FPGA detection by the conventional method was more difficult in our experiment.

As a summary of the comparison of the proposed method and conventional method, the detection accuracy of the recycled FPGA is shown in Table IV. In this table, the best performances highlighted in Fig. 15 are shown as the result of the proposed method. The proposed and conventional methods could identify all the 35 fresh FPGAs as fresh. The proposed method classified the eight aged FPGAs but missed the 1-hour aged FPGA (FPGA-05) as recycled. However, the conventional method failed to detect all the aged FPGAs even when all the ROs are used. From these results, we can conclude that the proposed method can classify the recycled FPGAs better than the conventional method in the experiment of degradation using the s9234 circuit and RISC-V processor.

### V. Conclusion

In this study, we proposed an accurate KFF-free recycled FPGA detection method in which we mitigated the process variation effect in the measured RO frequencies. We reduced the systematic component of the RO frequency by comparing the RO frequencies of neighboring CLBs, which also contribute to eliminating the need for a set of KFFs. In addition, the random component of the RO frequency was canceled out by increasing the number of RO stages to further improve the
detected accuracy. Recycled FPGAs were effectively detected using an unsupervised outlier detection method based on direct density ratio estimation. Experimental results using 35 commercially available FPGAs demonstrated that the proposed method successfully mitigates process variation effect and captures aging effect to detect recycled FPGAs. We further confirmed that the proposed method successfully detected all the recycled FPGAs except for that with a short aging time, while the conventional method failed to detect aged FPGAs.

As future work, we intend to further improve the detection performance of unsupervised recycled FPGA detection. As discussed in Section IV, the proposed method failed to detect FPGAs with a short aging time. It is expected that it could be improved by introducing the degradation analysis proposed in [31] into the unsupervised detection framework with density ratio estimation of the proposed method.

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