MCAD: Beyond Basic-Block Throughput Estimation through Differential, Instruction-Level Tracing

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### Abstract

Estimating instruction-level throughput is critical for many applications: multimedia, low-latency networking, medical, automotive, avionic, and industrial control systems all rely on tightly calculable and accurate timing bounds of their software. Unfortunately, how long a program may run - or if it may indeed stop at all - cannot be answered in the general case. This is why state-of-the-art throughput estimation tools usually focus on a subset of operations and make several simplifying assumptions. Correctly identifying these sets of constraints and regions of interest in the program typically requires source code, specialized tools, and dedicated expert knowledge. Whenever a single instruction is modified, this process must be repeated, incurring high costs when iteratively developing timing sensitive code in practice.

In this paper, we present MCAD, a novel and lightweight timing analysis framework that can identify the effects of code changes on the microarchitectural level for binary programs. MCAD provides accurate differential throughput estimates by emulating whole program execution using QEMU and forwarding traces to LLVM for instruction-level analysis. This allows developers to iterate quickly, with low overhead, using common tools: identifying execution paths that are less sensitive to changes over timing-critical paths only takes minutes within MCAD. To the best of our knowledge this represents an entirely new capability that reduces turnaround times for differential throughput estimation by several orders of magnitude compared to state-of-the-art tools. Our detailed evaluation shows that MCAD scales to real-world applications like FFmpeg and Clang with millions of instructions, achieving < 3% geo mean error compared to ground truth timings from hardware-performance counters on x86 and ARM machines.

### 1 Introduction

Studying timing aspects of computer programs before production use can be critical in many use cases. However, predicting the running time of a computer program reduces to the halting problem [24], which is famously undecidable in the general case. Due to this fundamental limitation, it is common practice to assume a finite upper bound on a program’s execution time and study its behavior conservatively within those confines. How long a program may run under real-world conditions is then usually captured by measures like Maximum Throughput Estimation, Average Case, and Worst-Case Execution Time and there exist a number of tools and techniques to systematically study such timing properties of computer programs.

Existing approaches can roughly be categorized as (i) studying the program without executing it (i.e., *static analyses*), (ii) studying specific runtime instances of the program (i.e., *dynamic analyses*), as well as (iii) hybrid approaches that utilize runtime data to calculate a static throughput estimate.

While in theory static approaches [13, 14, 17, 18, 22] reason about all possible executions of a program, they are fundamentally limited in practice with respect to essential program constructs such as loops, data-dependent control flows, and memory accesses [7, 21].

Dynamic approaches, on the other hand, trade generality for higher precision through measured bounds using architectural simulators [10, 12, 25] which faithfully model the runtime behavior or by using hardware-performance counters [3, 19] on the target device together with executions of the target program on a production system. They provide concrete and generally accurate estimates, however, they suffer from high architecture dependence and complicated setup. This is especially true when production systems are involved, often requiring dedicated expert knowledge and/or giving rise to compatibility issues with standard tools or default environments.

For this reason, more recent approaches [6, 16, 20] aim at combining the strengths of static throughput prediction with the expressiveness of dynamic approaches through parametric models that are either trained end-to-end using throughput data [20] or programmatically tuned for key parameters such as port utilization that are publicly available in the form of experimentally determined measurements [6, 16].
the scope of these recent approaches is limited to throughput predictions of individual basic blocks, i.e., only a handful of instructions, and they cannot handle real-world binary programs which may encompass millions of instructions, since predictions do not usually hold across control-flow transfers.

In this paper, we present MCAD, a lightweight and developer-centric alternative that provides whole-program throughput prediction of binary software. MCAD predicts cycle count execution time of binary programs by capturing emulated execution traces using the Quick EMUlator (QEMU) [9] and dynamically forwarding them to the LLVM Machine Code Analyzer (MCA) [2] for instruction-level analysis. The main purpose of MCAD is to provide fast, yet accurate differential timing analyses: cycle counts for whole program execution traces which typically contain hundreds of thousands to millions of instructions can usually be produced within the order of minutes or seconds.

MCAD enables the assessment of timing effects induced by binary patches as part of the development process by comparing the cycle counts before and after program patching and identifying the least intrusive change with respect to execution time. We extensively test and evaluate MCAD with respect to scalability and accuracy on a number of different real-world applications such as FFmpeg and Clang to demonstrate that MCAD can model micro-architectural behaviors, such as instruction latencies in superscalar processors, accurately and with low cost. The geo mean error in differential timing between MCAD and hardware performance counters in our experiments is smaller 3% across several different microarchitectures and application software.

To summarize our contributions are:

**Contributions**

- We present MCAD: a new open-source\(^1\) framework for throughput estimation yielding highly accurate differential timings, on par or better than the current state-of-the-art, while reducing turnaround time by several orders of magnitude.

- Our prototype implementation leverages QEMU as a fast instruction executor, utilizing LLVM MCA to model individual execution cycles per instruction, rather than simulation-based approaches that faithfully model complex processor front-ends.

- We provide a detailed evaluation of MCAD with respect to accuracy and scalability for the popular x86 and ARMv8 instruction-set architectures using several different devices and hardware-performance counters to collect timing measurements for real-world traces as ground truth.

\(^1\)http://github.com/securesystemslab/LLVM-MCA-Daemon

## 2 Background and Motivation

Analyzing timing behavior of computer programs is important for a diverse set of tasks that range from diagnosing performance problems to assuring fixed timing requirements in mission critical systems.

Throughput estimation is an active area of research that aims to predict the performance upper bound of a program, usually measured by cycle counts or Instruction Per Cycle (IPC), of a single basic block. Current tools model microarchitecture details like instruction latency and number of micro-ops of the target processor. One of the biggest problems with this approach is that it does not easily transfer across branch instructions or function call boundaries. For example, Listing 1 shows an x86_64 assembly code snippet consisting of three basic blocks, `loop`, `L0`, and `L1`. Block `loop` calculates a vector dot product followed by a conditional branch into either block `L0` or `L1` based on a data-dependent comparison, with both blocks jumping back to `loop` at the end.

```
1 loop:
2  vmulps %xmm0, %xmm1, %xmm2
3  vhaddps %xmm2, %xmm2, %xmm3
4  vhaddps %xmm3, %xmm3, %xmm4
5  cmp %r9d, %eax
6  jle L1
7
8 L0:
9  mulq %r8
10  jmp loop
11
12 L1:
13  movl 16(%ebp), %eax
14  addl 8, %ebp
15  jno loop
```

Listing 1: An x86_64 assembly code snippet.

Using Intel Coffee Lake as an example target architecture, throughput predictions of the individual basic blocks of this program will not generalize across executions. The reason is that instruction-level throughput for this program actually depends on the ordering of executed basic blocks on that architecture. In particular, executions where `L0` follows `loop` (Listing 2) are roughly 5~10 cycles slower, per iteration, than executions in which `L1` follows `loop` (Listing 3). This might seem counterintuitive as Listing 2 contains more instructions than Listing 3 and more importantly there is a memory read instruction (movl 16(%ebp), %eax) in the latter trace, which should be slower than scalar multiplication (mulq %r8). However, measurements on the target architecture reveal that there is a substantial slowdown in traces that follow the shorter Listing 2 due to resource contention between the two basic blocks.

```
1  vmulps %xmm0, %xmm1, %xmm2
```
3 Design

In this section we present our overall design of MCAD as depicted in Figure 1. As explained in the previous section, current throughput prediction approaches face severe challenges with respect to prediction across basic blocks, as well as scalability and turnaround times. The main goal of MCAD is to tackle all of these challenges to enable scalable and precise differential throughput analyses that can be used to actively drive development and steer engineers towards implementations with favorable runtime behavior.

3.1 Goals and Challenges

MCAD’s design should tackle three main goals:

First, we would like to provide whole-program throughput estimates across thousands of basic blocks and potentially millions of instructions. At a high level MCAD uses a broker component that provides execution traces in form of an instruction stream and a core component that analyzes instruction-level throughput of the respective trace on-the-fly. Results can then be processed by a viewer component for human-readable summarization and data reporting. In principle, the method by which execution traces are obtained and streamed to the core component is not tightly coupled to the method that is used to analyze the instruction stream. In early tests we compared several existing throughput analysis tools for use with our core component. However, we encountered several challenges with adopting any of them for our framework. As illustrated in the previous section, state of the art throughput prediction approaches do not generalize across control-flow transfers, and, within MCAD, streaming instructions that follow a control-flow transfer should seamlessly interface with the microarchitectural throughput prediction engine used for our analysis. As existing throughput prediction tools are designed for single basic block use, they also fail to scale up, in terms of both memory consumption and processing capabilities, when streaming input instructions on-the-fly from the broker component even for trivial programs. We also encountered numerous bugs when using the tools that seemed most fitting in this dynamic context, some of which we detail in Section 4.

Second, MCAD aims to support a development-driven workflow. This means, that developers are able to use MCAD to analyze the timing impact after modifying some part of the code, which might take the form of both a binary patch or a source-level change of the original program under our model. In addition to whole-program analyses, developers hence are able to choose to analyze only parts of the program. Selecting which parts of the program to analyze is done at varying levels of granularity to reduce noise in the resulting reports and speed up the analysis if so required.

Third, MCAD aims to provide timely feedback for the throughput estimates using an approach that ideally also generalizes across architectures. While purely dynamic approaches are already capable of producing whole-program
estimates today, the associated turnaround times and costs of setting up and running full-scale system simulation can be prohibitively expensive (i.e., on the order of hours or even days) [10, 12, 25]. Furthermore, existing dynamic throughput analysis tools are often tightly coupled to a specific architecture, which is why we opt for an emulation-based approach for producing execution traces inside our broker component using QEMU [9].

We will elaborate how MCAD tackles each of the respective challenges to achieve these goals throughout the rest of this section.

3.2 Scalable Throughput Prediction

As explained in Section 2 all existing throughput prediction engines are designed with single-basic-block use in mind. In our prototype we build on top of LLVM MCA [2], a performance analysis tool and library that was designed to estimate the basic block throughput in a static fashion. LLVM MCA employs a microarchitectural simulator to simulate individual instruction’s timeline inside an out-of-order processor. It taps into the LLVM compiler’s scheduling database, a mature and production-tested data source whose contents are curated by hardware vendors.

However, we found that LLVM MCA has difficulties to scale up in our dynamic scenario. Like other throughput prediction engines it does not support analyzing instructions beyond a branch point or a function call out of the box. On top of that, we found that some of the design trade-offs inside LLVM MCA make it prone to high memory pressure while processing large number of instructions. Enabling online analysis within MCAD required several changes to the underlying analysis infrastructure, such as MCA’s serialization, memory model, and instruction lifecycle. For example, different memory operations were assumed to never access aliasing addresses. After introducing our changes we found that dynamic memory traces can actually help the existing load-store unit inside MCA perform better.

In Section 4.2, we explain our modifications of LLVM MCA used in MCAD to tackle the aforementioned issues and make MCAD’s core component scale up to real-world applications.

3.3 Development-Driven Workflow

MCAD enables a development-driven workflow by providing fast whole-program throughput estimates that can easily be compared between two versions of a program. Furthermore, for cases that only patch a small portion of the original binary, MCAD also provides an option to analyze only part of the binary. In this mode, developers can designate the desired area by either specifying the symbol of a function or providing explicit address ranges in the program. If an address range is provided, MCAD essentially yields the original basic-block granularity of the underlying analysis engine, while providing the flexibility of comparing the execution of multiple basic blocks at the same time.

3.4 Analysis Performance and Generalization Across Architectures

The broker component is responsible for supplying execution traces to the core component. This includes interoperating with the origin of execution traces and converting them into a unified low-level representation. This also means that the broker and core components need to work together to enable a timely and architecture-independent operation of MCAD. By default execution traces are transmitted remotely from QEMU using a custom plugin. QEMU’s emulation-based approach incurs around 30% runtime overhead [15], effectively enabling near-native execution speeds when using hardware virtualization extensions. QEMU also has extensive support for many major architectures, meaning that MCAD’s broker component is able to fulfill both of these requirements. It is noteworthy to mention that MCAD also provides a facility for reading offline execution traces, which can be collected from executions on a physical device using any kind of tracing method available for that device. As mentioned earlier, MCAD’s core component uses the LLVM Machine Code Analyzer. Since MCA uses LLVM’s infrastructure targeting different hardware architectures and processor models in the analysis engine is trivial. As a result, both the broker and the core component of MCAD generalize well across several architectures and provide top-of-the-line performance. Moreover, with QEMU and LLVM MCAD uses tools that many software developers will already be deeply familiar with.

4 Implementation

In this section we describe the workflow and implementation of MCAD in detail. Figure 2 depicts the interaction between the different components: first, the target binary program is executed by QEMU, which collects execution traces and sends them to our analysis engine in real time. Inside our analysis engine the executed instructions are further processed by timing analyses built on top of LLVM MCA [2], which provides algorithms for microarchitectural simulation and instruction scheduling of modern processors. Finally, MCAD provides estimates for key timing and performance metrics like the prospective cycle counts, instruction-level throughput, and the ability to identify potential bottlenecks while running the target binary in the emulated environment.

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2 QEMU supports x86, MIPS, SPARC, ARM, PowerPC, RISC-V among many others, including individual processor models and specific microarchitectures.

3 LLVM supports x86, MIPS, SPARC, ARM, PowerPC, RISC-V among many others.
4.1 Instruction Broker

MCAD’s broker implementation is a standalone process that produces MCInst [4] objects, an internal representation for machine code instructions used within LLVM, in batches to the core component. However, the broker interface is designed to be extensible and allow integration of custom implementations and enable streaming of instruction sequences to the core component from a variety of different sources. So far we integrated and tested two broker implementations: an assembly file broker that takes its input from an assembly file on disk and a QEMU broker that uses a QEMU plugin to communicate with the qemu-broker process using TCP sockets to process the raw execution trace in real time before streaming them into the core component for analysis.

Broker implementations can choose to attach arbitrary metadata to the streamed instruction trace: for instance, by attaching load and store addresses and the size of memory operations we can enable more precise dependency detection between memory accesses in the analysis engine of the core component. In particular, MCAD’s QEMU plugin collects raw instructions as executed by the emulator alongside additional information regarding memory operations, which is then used to improve analysis results with respect to instruction reordering. In this mode of operation MCAD’s broker dynamically instruments memory read and write operations to gather target address and size of the data. The QEMU plugin will then send these data over a TCP socket to the receiving core component that runs in parallel in a separate process. Inside the core component this metadata that is attached to memory operations is then inserted into a registry that is used by the core component for joint analysis.

Developing custom brokers is straightforward and only requires implementing a few callback functions before loading them as shared libraries during runtime. This allows users to rapidly switch between different workloads and environments depending on their needs. It is important to note that we do not make any assumptions about a broker’s internal execution model – so long as the broker adheres to the streaming interface to supply the next batch of instructions.

4.2 Analysis Core

Our core component builds on top of state-of-the-art throughput prediction engines, which are designed as offline tools for static throughput estimation of small sequences of machine instructions (usually at the basic block granularity). Given a (short) sequence of assembly instructions, they provide throughput estimation results on the micro-architectural level either through end-to-end trained models for a given architecture or through simulation of the different stages inside a modern processor with varying levels of detail and manually tuned key parameters per architecture. Unfortunately, all existing throughput prediction tools failed to scale up with our dynamic model of execution: as an example, using the standard video and audio encoder FFmpeg [23] produces around 20 million instructions on a Linux x86_64 machine while decoding a short MPEG-4 video with duration of 2 seconds. Within MCAD, this type of application would be considered a lightweight real-world workload. We found that none of the existing approaches were able to process anywhere near this kind of workload.

However, since the LLVM Machine Code Analyzer (LLVM MCA) [2] already had support for slightly larger pieces of code compared to all other related approaches through their loop kernel analysis, we implemented MCAD’s default analysis engine on top of that. Our investigation into adopting MCA for our core component showed several failure cases while handling larger workloads. Internally, LLVM MCA models
four distinct execution stages *Entry*, *Dispatch*, *Execute*, and *Retire*. Under MCAD’s workflow the instruction stream provided by the broker enters the pipeline from the *Entry* stage and is processed by each subsequent stage sequentially. Originally, this pipeline requires all input instructions be available before the start of the analysis. This requirement is not suited for our use case. LLVM MCA internally then assigns an object to each instruction to keep track of its scheduling status within the simulation pipeline. In some of our tests, MCA consistently drained all available physical memory on the machine running the analysis due to the allocation of this internal instruction representation.

To address the first issue we created a new incremental mode for the LLVM MCA simulation pipeline. In this mode, the simulation pipeline fetches input instructions incrementally. If there is no instruction available from the input source, the pipeline will save its current state and exit. Upon the arrival of new input instructions, the simulation will be restored and proceed from its previous state. To solve the second issue of high memory consumption when handling large number of instructions, we implemented a new instruction recycling mechanism for the LLVM MCA simulation pipeline. This instruction recycler will reclaim and collect internal instruction objects from retired instructions, instead of releasing their memory. These recycled instruction objects will then be reused to model new incoming instructions. Our experiments showed that with this recycling mechanism, MCAD’s core analysis uses one third of memory on average than the unmodified MCA implementation.

LLVM MCA simulates different execution units which process individual instructions and determine results of the operation in question. These estimates include cycle counts, potential pipeline stalling, and predictions of possible instruction re-ordering. For instance, MCA’s Load-Store Unit tracks the availability of memory operations and their (data) dependencies. This is crucial for simulating out-of-order scheduling in modern processors, which frequently reorder memory operations based on their dependencies. We significantly extended these existing capabilities by providing an online analysis workflow: by sequentially parsing the incoming instruction stream and processing each instruction according to the simulated pipeline, MCAD is able to present an estimate of how arbitrarily long instruction sequences might be scheduled within the processor.

LLVM MCA contains a component called Load Store Unit (LSUnit in Figure 2) which simulates load and store reordering that could happen in the hardware scheduler of the simulated processor model. This type of hardware optimization re-orders memory instructions to break dependencies when possible, which is largely determined by their memory aliasing properties at runtime. However, without precise memory access information, LLVM MCA can only make coarse-grained assumptions, for instance, all memory instructions are aliasing with each other, which are controlled by a command line parameter. MCAD leverages the memory traces collected from QEMU to improve this situation. We modified the Load Store Unit such that aliasing properties are now dictated by fine-grained memory accessing traces as provided by our QEMU plugin. This enables our custom core component to simulate load and store reordering with higher accuracy by using dynamic information as it becomes available during execution.

### 4.3 Sub-Region Feature and Viewer Component

MCAD’s viewer component displays throughput estimations with information like total cycle counts or potential pipeline stalls. An example of this can be seen in Listing 4. We also prototyped a view of the timing itinerary of individual instruction in a timeline view. For instance, given the execution trace in Listing 2, Listing 5 shows the corresponding timeline. This particular view is a fork from the timeline view that exists in LLVM MCA. However, the timeline view in LLVM MCA cannot inspect the itinerary of a subset of analyzed execution trace that is implemented as part of MCAD’s subregion feature and it has limitations on the maximum number of displayed instructions. For this reason, third-party visualization tools are also supported in this component. For instance, we prototyped a new timeline view based on Chrome Developer Tools (DevTools) [1] and provide a screenshot in Figure 5 in the Appendix. Chrome DevTools is a GUI-based tool built into the Chromium and Google Chrome browser that supports a wide variety of utilities for web development. One of the features visualizes HTTP requests sent and received by the web page and we re-purposed this functionality to show the timing details of individual machine instructions instead. More specifically, this GUI view is divided into two parts: on the top, there is a timeline showing the itinerary of every instruction, similar to the timeline view provided by LLVM-MCA; on the bottom half of the tool, executed instructions are presented as a list, with details like number of execution or stalling cycles shown on the side. In our early test we already found this a lot easier to scroll and navigate through the thousands or even millions of instructions that are processed by MCAD, compared to the terminal-based LLVM-MCA timeline view. Since this view was designed to analyze large number of network requests it provides a solid basis to help our new timeline view scale up.

| Instructions | 350 |
|-------------|-----|
| Total Cycles | 262 |
| Total uOps  | 600 |
| Dispatch Width | 6 |
| uOps Per Cycle | 2.29 |
| IPC          | 1.34 |
5 Evaluation

Since MCAD’s main goal is to enable developers to quickly assess and iterate on the timing effects of small modifications, including patches, we use binary programs of different release versions to evaluate performance and cycle-count accuracy against physical hardware traces to quantify how MCAD fares in comparison. More formally, given two different versions $i$ and $j$ of a program $P$, denoted as $P_i$ and $P_j$, as well as a throughput predictor $H$ that provides the number of execution cycles under a specific input for the respective program, we define the differential throughput $\Delta_H(P_i, P_j)$ describing the change in cycle counts between version $i$ and version $j$ of program $P$ as predicted by $H$ as follows:

$$\Delta_H(P_i, P_j) = \left| \frac{H(P_j) - H(P_i)}{H(P_i)} \right|$$

Given two versions of a program $P_i$ and $P_j$, as well as their inputs, we first use MCAD to predict their differential throughput, resulting in $\Delta_{\text{MCAD}}(P_i, P_j)$. Second, we similarly measure their relative difference in cycle counts from version $i$ to version $j$ using hardware-performance counters on physical devices, resulting in groundtruth differential throughput $\Delta(P_i, P_j)$. Finally, we formally define the error percentage of MCAD’s prediction of differential throughput between version $i$ and version $j$ as:

$$E_{ij} = \left| \Delta(P_i, P_j) - \Delta_{\text{MCAD}}(P_i, P_j) \right|$$

5.1 Accurate Differential Throughput Prediction Across Control Transfers

To assess the overall accuracy and ability to generalize throughput predictions across control transfers we conduct experiments using two popular and widely used applications as target programs: the ffmpeg video encoder and the C/C++/Objective-C compiler frontend clang. The main reason for picking ffmpeg for our case study is that video encoding represents a complex and highly performance-intensive task with many applications in real-world use cases. For clang, it represents a large-scale software consisting of complex branching logic, which is well suited to test MCAD’s cross-branch prediction accuracy and also plays an important role in many real-world scenarios. We collect baseline cycle-count measurements on physical devices averaged over 10 repetitions using three machines with different processor and microarchitectures: a 6-core Intel i7 8700K x86_64 CPU,
We conduct our experiment for ffmpeg using subsequent version pairs using 10 different release versions in the following order: 2.0, 2.2, 2.4, 2.6, 2.8, 3.1, 3.3, 4.0, 4.2, and 4.4. We used the same 14KB MPEG-4 video file as reference input and executed the following command:

```
ffmpeg -i input.mp4 -f null -
```

We collect baseline measurements using Linux Perf, which leverages the Performance Monitor Unit (PMU) provided by the underlying hardware. Figure 3a, Figure 3b, and Figure 3c depict $\Delta_{MCAD}(\text{ffmpeg}_i, \text{ffmpeg}_j)$ and $\Delta_j$ results for version pairs $(i, j)$ as $(2.0, 2.2), (2.2, 2.4)$, and so forth. In addition, Figure 3d, Figure 3e, and Figure 3f presented the $E_j$ results for the corresponding version pairs between groundtruth measurements on physical devices and predictions by MCAD. Our results show that MCAD closely follows the hardware cycle count and never deviates from the changes in the baseline count by more than 15%. On average, the error is 2.6% on the measurements collected from the Intel machine, 2.9% on the measurements from the AMD machine, and 0.9% on the measurements from ARM Cortex-A57 with a standard deviation of less than 5% in all cases.

### 5.1.2 Clang

We conducted our experiments for clang using 8 different release versions as follows: 6.0, 7.0, 8.0, 9.0, 10.0, 11.0, 12.0, and 13.0. We used the following C program as the reference input:

```
int foo(int x, int y) {
    return x * 2 + y;
}
```

Before version 10.0, Clang runs the compiler driver and the rest of the compilation pipeline in separate processes. Thus, in this evaluation we invoke the clang frontend and backend directly. We obtain these commands that are usually issued by the compiler driver using the following options:

```
clang -### -O2 -c input.c -o /dev/null
```

Again, we collect baseline numbers using Linux Perf on the respective target machines. Figure 4a, Figure 4b, and Figure 4c depict $\Delta_{MCAD}(\text{clang}_i, \text{clang}_j)$ and $\Delta_j$ for version pairs $(i, j)$ as $(6.7), (7.8)$, and so forth. Similarly, Figure 4d, Figure 4e, and Figure 4f plot $E_j$ between predictions by MCAD and groundtruth for each version pair. Again, our results show that MCAD closely follows the hardware cycle count and never deviates from the changes in the baseline count by more than 10%. On average, the error is 2.1% on the measurements collected from the Intel machine, 2.5% on the measurements collected from the AMD machine, and 0.9% on the measurements from ARM Cortex-A57 with a standard deviation of less than 5% in all cases.
5.2 Scalability and Comparison

Besides accurate predictions that generalize across control-flow transfers, another major goal of MCAD is scalability. In particular, we aim for MCAD to scale up with the complexity of real-world target programs. In this section, we compare against four state-of-the-art throughput prediction and analysis approaches: OSACA [16], Ithemal [20], uiCA [6], and LLVM-MCA [2]. We present the results in Table 1.

First, we focus on the benchmarks these tools used in their repositories or publications. We compare the type and size of benchmark, as well as their supported target instruction sets. All prior art operates on the individual basic block level with the exception of LLVM MCA which also contains designated support for loop kernels. However, in both cases instruction sequences usually consist of only 10–20 instructions at most. On the other hand, MCAD was designed to work on real-world program traces scaling millions of instructions. MCAD also supports most of the hardware architectures that QEMU and LLVM support, which amounts to nearly 20 different Instruction-Set Architectures (ISAs). In contrast, most other tools are highly architecture specific and only support x86_64.

We further evaluate these tools using the same reference input and compare their performance with respect to execution time and memory consumption. For this purpose we collected the execution trace of a ffmpeg invocation using version 4.2 as described in Section 5.1.1 storing the results into a file. The resulting instruction stream consists of roughly 27 million x86_64 instructions. To give state-of-the-art approaches the benefit of the doubt we perform this experiment on an 80-core Intel Xeon E7-4870 machine, clocked at 2.4GHz, equipped with 198GB of RAM and the same amount of swap space, setting a 48-hour time limit on the execution.

As shown, OSACA and Ithemal did not finish this task: OSACA bailed out with failures related to loading hardware models after parsing the input file; Ithemal promoted an out-of-memory error from its DynamoRIO [11] runtime before bailing out. Similarly, uiCA could not finish within the time limit after consuming significant amounts of memory. Last but not the least, despite being able to finish, LLVM-MCA took much more time and memory footprints compared to MCAD, demonstrating the effectiveness of our changes over standard MCA in our implementation.

### Table 1: Comparison of different tools to predict cycle counts of software across various dimensions. While the error metrics differ, we present error numbers as reported by the most recent work [6] for completeness.  

| Benchmark Type | OSACA [16] | Ithemal [20] | LLVM MCA [2] | MCAD |
|----------------|------------|--------------|--------------|------|
| Supported ISAs  | x86_64 only|x86_64 only   | x86 & x86_64 | ~20 ISAs |
| Handles branches| ☑          | ☑            | ☑            | ☑    |
| Memory usage    | 113GB      | N/A          | 29.39GB      | 2.16GB |
| Execution time  | Timeout after 48h. | Exit w/error after 24h. | Exit w/error after 2m. | 219.98s | 52.69s |
| Mean error      | 3% [6]     | ~30% [6]     | ~5% [6]      | ~20% [6] | 3% |
| Scales to # of instrs. | 10~20 | ~40 | 10~20 | ~1000 | >1000000 |

MCAD builds on top of this prior work that provides insights into modern processor pipelines through detailed measurements and experiments. Since a lot of this research has been contributed in part by vendors directly and in other parts incorporated by the community into the LLVM compiler infrastructure, MCAD currently uses LLVM MCA as the core analysis engine. However, the core analysis component in our design can support other throughput analysis engines in principle, which would allow us to predict timing effects of a number of optimizations in modern processors that are not explicitly modeled or learned.

 uiCA uses the Mean Absolute Percentage Error (MAPE) to compare the error of a prediction against a single execution on a physical device, whereas we use the mean error of the predicted difference in cycles between two executions.  

4
currently modeled by LLVM MCA, such as including instruction prefetching and branch prediction which usually happen in the processor frontend. The main obstacle towards that as demonstrated by our experiments in Section 5.2, however, remains overcoming scalability issues of the related approaches.

Looking ahead to future work we anticipate that research into analysis of multi-process executions should be feasible within MCAD in principle. As introduced in Section 3 we collect execution traces using QEMU and a custom plugin and certain recently-added QEMU plugin interfaces would allow us to distinguish traces originating from different virtual CPUs at runtime. Nevertheless, how to incorporate modern processors’ concurrency models into current throughput prediction approaches remain an open research question. It would also be possible to switch out QEMU for other methods of execution trace collection entirely: for instance, leveraging binary rewriting tools would enable us to insert instrumentation approaches that report the executed instructions natively.

Last but not least, we believe a more scalable, intuitive, and interactive timeline or waterfall view could provide developers with more insights by visualizing resource dependencies among instructions, pointing towards potential avenues for improving patches to timing-sensitive code.

7 Related Work

In this section, we categorize the most relevant prior approaches and also compare them against MCAD. To the best of our knowledge, none of the existing systems supports analyzing timing effects of programs in a timely manner that supports a development-driven workflow behind that can guide implementation changes with respect to timing-sensitive system behavior.

A large body of prior research focused on static prediction of worst-case timing behavior [13, 14, 17, 18, 22]. However, as mentioned in the beginning of this paper, reasoning about timing properties of arbitrary programs reduces to the halting problem in the general case and as a result static approaches make strong assumptions such as an upper bound on the number of loop iterations, recursion depth, effects of memory accesses, and external I/O operations. In practice, this means that the user of traditional tools has to provide upper bound information for all loop constructs, recursion, avoid indirect memory accesses through pointers, and avoid the use of I/O operations in analyzed parts of the code. Ensuring proper and correct usage then typically requires dedicated build toolchains and environment setups, as well as expert knowledge about the analysis framework. Moreover, static tools typically over-approximate cycle counts up to several orders of magnitude over physical hardware execution in order to remain sound, with several tools providing timing estimates in units of wall-clock time rather than cycles [7, 21].

In contrast, dynamic approaches aim at providing detailed and concrete timing analyses of the running software using concrete inputs. There are two main flavors of dynamic timing analysis tools: either using physical hardware tracing or using architectural simulators. Approaches using physical tracing execute the program on the target architecture and measure cycle counts directly using the facilities provided by the device [3, 19]. While in theory this yields the most precise results and should also be reasonably fast, in practice this is often not the case: the target architecture might be a production system that is not readily available to the developer running the test and in a collaborative environment each team would require their own physical device to test their changes against.

Additionally, setting up and using facilities for accurate cycle-count measurements can be a time-intensive task in and of itself, requiring complicated setup, and potentially support by the target program’s build toolchain as well as the operating system of the production system. Worse yet, the target architecture might not actually provide any built-in facilities for accurate measurement of cycle counts, requiring developers to implement purpose-built, custom, and highly architecture-dependent in-house measurement frameworks, whose accuracy might actually be limited in the end. Cycle-accurate architectural simulators [10, 12, 25] on the other hand promise to provide a similar level of accuracy as physical tracing without requiring an actual physical device to capture program execution. Unfortunately, simulation-based approaches also come with major drawbacks: first, performance is typically at least three orders of magnitude slower than native execution (or even slower) as they faithfully simulate microarchitectural details of modern processor pipelines completely in software. Second, they are usually aimed towards explorative hardware design and implementation studies of novel architectures rather than simulating throughput of software for existing platforms. As a result, these frameworks are not easily accessible and can be difficult to integrate with existing software development tools and continuous integration workflows due to the high resource requirements and time-intensive nature of the simulation-based approach.

More recently, a number of approaches [2, 6, 16, 20] proposed throughput modeling of machine code using parametric models for accurate, yet fast throughput prediction. Hybrid approaches combine the premise of dynamic approaches to predict timing aspects of a particular execution of the target program rather than reasoning about the entire set of possible executions at once like prior static approaches do. While their underlying parametric models require prior knowledge of key microarchitectural aspects such as port usage, instruction latencies, and other internal details that may not be publicly available, recent advances in machine learning showed that architectural dependence can be tackled to some extent by learning model parameters from data [8, 20]. However, in our evaluation, we show that all existing hybrid approaches are severely

\footnote{For instance, because of requiring \textit{instrumentation} of the original binary where instrumentation overhead cannot easily be measured at runtime.}
limited with respect to scalability, providing throughput estimates only for a handful up to a few hundred instructions at most, also lacking support for prediction across control-flow transfers. In contrast, MCAD handles complex binary programs containing literally millions of individual instructions with near-native execution speeds.

8 Conclusion

To summarize, our results show that MCAD improves on state-of-art by scaling up with the complexity of real-world softwares. It is well suited for lightweight, developer-centric cycle count estimates targeting multiple different hardware architectures. It can drive (patch) development by quickly iterating on small changes and assessing their timing impact on real-world programs like ffmpeg and clang with a mean error in differential throughput estimates of <3% compared to hardware-based traces.

References

[1] Chrome devtools. https://developer.chrome.com/docs/devtools/. Accessed: 2021-12-13.
[2] LLVM mca. https://llvm.org/docs/CommandGuide/llvm-mca.html. Accessed: 2021-06-28.
[3] Perf: Linux profiling with performance counters. https://perf.wiki.kernel.org/index.php/Main_Page. Accessed: 2021-11-08.
[4] Intro to the LLVM mc project. https://blog.llvm.org/2010/04/intro-to-llvm-mc-project.html. 2010. Accessed: 2021-07-08.
[5] Andreas Abel and Jan Reineke. uops.info: Characterizing latency, throughput, and port usage of instructions on intel microarchitectures. In ASPLOS, ASPLOS ’19, pages 673–686, New York, NY, USA, 2019. ACM.
[6] Andreas Abel and Jan Reineke. Accurate throughput prediction of basic blocks on recent intel microarchitectures. arXiv preprint arXiv:2107.14210, 2021.
[7] Jaume Abella, Carles Hernández, Eduardo Quiñones, Francisco J Cazorla, Philippa Ryan Conny, Mikael Azkarate-Askasua, Jon Perez, Enrico Mezzetti, and Tulio Vardanega. Wcet analysis methods: Pitfalls and challenges on their trustworthiness. In 10th IEEE International Symposium on Industrial Embedded Systems (SIES), pages 1–10. IEEE, 2015.
[8] Riyadh Baghdadi, Massinissa Merouani, Mohamed-Hicham Legehettas, Kamel Abdous, Taha Arbaoui, Karima Benatchba, et al. A deep learning based cost model for automatic code optimization. In Proceedings of Machine Learning and Systems, volume 3, 2021.
[9] Fabrice Bellard. Qemu, a fast and portable dynamic translator. In USENIX annual technical conference, FREENIX Track, volume 41, page 46. California, USA, 2005.
[10] Nathan Binkert, Bradford Beckmann, Gabriel Black, Steven K Reinhart, Ali Saidi, Arka Prapa Basu, Joel Hestness, Derek R Hower, Tushar Krishna, Somayeh Sardashti, et al. The gem5 simulator. In ACM SIGARCH computer architecture news, volume 39, pages 1–7, 2011.
[11] Derek Brunning and Saman Amarasinghe. Efficient, transparent, and comprehensive runtime code manipulation. PhD thesis, Massachusetts Institute of Technology, Department of Electrical Engineering . . . , 2004.
[12] Doug Burger and Todd M Austin. The simplescalar tool set, version 2.0. In ACM SIGARCH computer architecture news, volume 25, pages 13–25, 1997.
[13] Heiko Falk and Jan C Kleinsorge. Optimal static wcet-aware scratchpad allocation of program code. In Proceedings of the 46th Annual Design Automation Conference, pages 732–737, 2009.
[14] Damien Hardy, Benjamin Rouxel, and Isabelle Puaut. The heptane static worst-case execution time estimation tool. In 17th International Workshop on Worst-Case Execution Time Analysis (WCET 2017). Schloss Dagstuhl-Leibniz-Zentrum fuer Informatik, 2017.
[15] Diarmuid Corcoran Lars Rasmusson. Performance overhead of kvm on linux 3.9 on arm cortex-a15. https://www.diva-portal.org/smash/get/diva2:1043325/FULLTEXT01.pdf, 2013.
[16] Jan Laukemann, Julian Hammer, Johannes Hofmann, Georg Hager, and Gerhard Wellein. Automated instruction stream throughput prediction for intel and amd microarchitectures. In 2018 IEEE/ACM performance modeling, benchmarking and simulation of high performance computer systems (PMBS), pages 121–131. IEEE, 2018.
[17] Xianfeng Li, Yun Liang, Tulika Mitra, and Abhik Roychoudhury. Chronos: A timing analyzer for embedded software. In Science of Computer Programming, volume 69, pages 56–67, 2007.
[18] Björn Lisper. Sweet--a tool for wcet flow analysis. In International Symposium On Leveraging Applications Of Formal Methods, Verification and Validation, pages 482–485. Springer, 2014.
[19] RapitaSystems LTD. Automating wcet analysis for do-178b/c. 2017.

[20] Charith Mendis, Alex Renda, Saman Amarasinghe, and Michael Carbin. Ithemal: Accurate, portable and fast basic block throughput estimation using deep neural networks. In International Conference on machine learning, pages 4505–4515. PMLR, 2019.

[21] Enrico Mezzetti and Tullio Vardanega. On the industrial fitness of wcet analysis. na, 2011.

[22] Daniel Sehlberg, Andreas Ermedahl, Jan Gustafsson, Björn Lisper, and Steffen Wiegratz. Static wcet analysis of real-time task-oriented code in vehicle control systems. In Second International Symposium on Leveraging Applications of Formal Methods, Verification and Validation (isola 2006), pages 212–219. IEEE, 2006.

[23] Suramya Tomar. Converting video formats with ffmpeg. Linux Journal, 2006(146):10, 2006.

[24] A. M. Turing. On computable numbers, with an application to the entscheidungsproblem. Proceedings of the London Mathematical Society, s2-42(1):230–265, 1937.

[25] Matt T Yourst. Ptlsim: A cycle accurate full system x86-64 microarchitectural simulator. In 2007 IEEE International Symposium on Performance Analysis of Systems & Software, pages 23–34. IEEE, 2007.

A Appendix

Figure 5: Prototypical viewer component (based on Chrome dev tool).