A High Frame Rate Analog Front-End IC With Piezoelectric Micromachined Ultrasound Transducers Using Analog Multi-Line Acquisition for Ultrasound Imaging Systems

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ABSTRACT This paper proposes a high frame rate analog front-end (AFE) IC combined with a piezoelectric micromachined ultrasonic transducer (PMUT) for ultrasound imaging systems (UISs). The proposed AFE IC, which consists of 8-channel transceivers and a peripheral circuit, employs analog multi-line acquisition (AMLA) based on sub-array beamforming. This AMLA generates multiple scanlines during a scan time by simultaneously and precisely controlling the delay of the AFE IC, thus achieving the high frame rate of the AFE IC. The sensitivities of the PMUT for transmitting and receiving ultrasound waves are simulated to be 67.5 kPa/V and 1.2 mV/kPa, respectively, which are high enough to mitigate the needs of the high-voltage electronics for UISs. The proposed AFE IC was fabricated using a 0.18-µm silicon-on-insulator process and occupies an active area of 2.56 mm × 1.68 mm. The measurement results using the simulated PMUT parameters show that the proposed AFE IC with the AMLA precisely controls its delay up to 1 µs at a clock frequency of 40 MHz. It also acquires more than 9,000 scan/s even at a focal depth of 150 mm, which is at least twice greater than those of prior works, achieving a high frame rate of 93 Hz when 100 scanlines are used for a frame. In addition, a figure-of-merit, which considers the energy consumption per channel/scan and the energy loss, is achieved to be 20 nJ/scan/dB at a focal depth of 150 mm and a center frequency of 3.6 MHz; this is the best result compared to previously reported works. Therefore, the proposed AFE IC is suitable for UISs requiring a high frame rate.

INDEX TERMS Ultrasound imaging system, piezoelectric micromachined ultrasonic transducer (PMUT), analog multi-line acquisition, high frame rate, analog front-end.

I. INTRODUCTION

Ultrasound imaging systems (UISs) have been widely researched for medical applications due to their advantages of non-invasiveness to the human body and real-time imaging capabilities. Especially, to realize high-quality, real-time imaging of heart motions and cardiac events in the UISs, it is necessary to increase the frame rate, which represents a measure of how fast motion can be captured as an image [1]. However, the frame rate of the UISs is physically limited to less than 50 fps at a large focal depth (>10 cm) due to the acoustic velocity and the distance over which the ultrasound wave travels.

Various studies [2]–[11] have been conducted to overcome the above physical limitation in the frame rate of the UISs. Multi-line acquisition (MLA) using a parallel processing technique based on plane wave imaging [2]–[6] was reported to increase the frame rate by producing multiple scanlines from transmitted unfocused ultrasound waves at a pulse repetition frequency (PRF). However, these unfocused ultrasound waves caused a poor signal-to-noise ratio (SNR), particularly at a great focal depth. In addition, multi-line
transmission (MLT) [7]–[10] was reported to simultaneously transmit multiple focused beams in different directions, while increasing the frame rate without sacrificing the maximum focal depth or the number of scanlines. However, this MLT caused a large dynamic power in the ultrasound probe during the multiple transmissions of the ultrasound waves and limited the SNR due to crossstalk between the simultaneously transmitted beams [10].

The previous MLAs and MLTs mentioned above have been realized in the digital domain (FPGA or main instrument unit) followed by the analog front-end (AFE) IC and the analog-to-digital converters (ADCs) in the ultrasound probe. Here, the AFE IC transmits high-voltage (HV) signals to the ultrasound transducers and receives echo from the human body. These multi-line implementations in the digital domain have the advantages of generating multiple scanlines and allowing for flexible control of the beam formation. However, this flexible control must constantly adjust the entire delay range for the multiple beam formation even at a fine delay of less than a few micro seconds between the adjacent scanlines, resulting in computational inefficiencies. In addition, as the number of transceiver channels of the AFE IC increases, so does the number of ADCs, which increases the device area and power consumption in implementing the compact ultrasound probe. As such, attempts to increase the frame rate only in the digital domain have led to the aforementioned drawbacks, resulting in incomplete real-time imaging of the UISS. Nevertheless, not much research has yet been dedicated to AFE ICs in the ultrasound probe [12]–[15] to address the physical limitations in the frame rate of the UISS. In [14], a column-row architecture was employed in the AFE IC to increase the frame rate based on parallel processing with the plane wave; however, this architecture was still limited in terms of increasing the frame rate at a shallow focal depth.

In this paper, an analog multi-line acquisition (AMLA) with a focused beam is proposed to increase the frame rate of the AFE IC based on sub-array beamforming for UISSs. The proposed AMLA enables the proposed AFE IC to not only increase the frame rate by controlling only the fine delay, not the full delay, but also mitigate the increase in the number of ADCs. In addition, piezoelectric micromachined ultrasound transducers (PMUTs) have been employed to alleviate the need to use HV electronics in the UISSs. As a result, using the HV DC bias is no longer necessary, which is generally tens of volts for capacitive micromachined ultrasonic transducers (CMUTs). Also, these PMUTs achieve better sensitivity due to their higher capacitance and lower electrical impedance than the CMUTs [16].

The remainder of this paper is organized as follows. Section II presents the architecture of the proposed AFE IC employing the AMLA and its operating principle. In Section III, the circuit implementation of the proposed AFE IC is described in detail. Then, the experimental results are analyzed and compared with previous works in Section IV. Finally, the conclusions are given in Section V.

II. SYSTEM ARCHITECTURE

A. ANALOG FRONT-END (AFE) IC

Fig. 1 shows the block diagram of the proposed AFE IC that not only transmits HV signals to the PMUT arrays to generate ultrasound waves, but also receives the electronic signals of echo from the human body and performs signal conditioning before the analog-to-digital conversion. The AFE IC consists of two sub-arrays, each of which has 4 transceivers, and a peripheral circuit that includes a control block, a low-voltage differential signaling (LVDS) RX, and differential-to-single-ended (D2S) buffers. Each transceiver performs the TX operation for ultrasound waves through the TX circuit including a TX controller and a biphasic HV pulser, and the RX operation through the RX circuit including a low-noise amplifier (LNA), a variable gain amplifier (VGA), and a multiple analog delay line (MADL). Here, the VGA is employed for time-gain compensation. A protection switch (SW) employing a floating-source structure configured with only three HV devices [17] is implemented to protect the low-voltage devices used in the RX circuit during the TX operation.

In the peripheral circuit implemented in the AFE IC, the LVDS RX receives an 80 MHz clock signal (CLK_{80M}) and serial data (D_{AFE IC}) from the FPGA, and then sends them to the control block. D_{AFE IC} includes the frequency data, TX fine delay data (D_{FD_TX}), number of pulses for TX operation, and gain control data and RX fine delay data (D_{FD_RX}) for RX operation. Here, each D_{FD_RX} is continuously calculated by the FPGA based on the corresponding fine delays. The D2S buffer receives the differential signals (V_{OUTP[3:0]} and V_{OUTN[3:0]}) from the MADLs in two sub-arrays and converts them to the single-ended signals (V_{OUT[3:0]}) followed by sending them to the ADCs. Here, the D2S buffer not only reduces the number of output signals, but also achieves a conversion gain of 6 dB.

For TX operation, the control block delivers D_{AFE IC} with the frequency data, D_{FD_TX}, and the number of pulses to the TX circuit that is fully configured with digital circuits. Then, an HV pulse (V_{HV_OUT}) is produced to generate the ultrasound waves in the PMUT. Here, a TX input signal (V_{IN_TX[1:0]}) with the coarse delay is provided from the
FIGURE 2. Configuration of the proposed analog MLA (AMLA): (a) operational block diagram of the AMLA, (b) geometric diagram of a one-dimensional UIS, and (c) examples of coarse and fine delay profiles.

For RX operation, the RX circuit receives an electrically converted signal \( V_{IN} \) from PMUTs and performs an amplification operation through the LNA and VGA, as well as the micro-beamforming operation with the AMLA through the MADL. Here, the control block provides the gain control signals to the VGA and controls fine delays of the MADL based on \( D_{FD\_RX} \). Then, \( V_{OUT}[3:0] \) from the D2S buffers are converted to digital signals by the ADCs, and then coarse delays are applied to these digital signals in the FPGA for the beamforming.

B. ANALOG MULTI-LINE ACQUISITION

The proposed AMLA employs sub-array beamforming and produces multiple adjacent scanlines based on echo from the human body as transmitting the single-focused ultrasound beam, thus increasing the frame rate of the UIS. Here, the frame rate can be expressed as

\[
\text{Frame rate} = \text{PRF} \times \frac{N_{MLA}}{M},
\]

where \( M \) is the number of scanlines used for a frame, and \( N_{MLA} \) is the number of scanlines produced by the AMLA at a PRF. The PRF can be calculated by

\[
\text{PRF} = \frac{V_{\text{tissue}}}{L \times 2} + \frac{1}{T_{TX}},
\]

where \( V_{\text{tissue}} \) is the acoustic velocity in soft tissue, which is typically 1540 m/s, \( L \) is the focal depth, and \( T_{TX} \) is the time interval for TX.

To properly realize the proposed AMLA, the delay-and-summation (DAS) needs to be applied to the corresponding beam during the beamforming operation of the UISs. Here, the DAS represents that the ultrasound waves generated from the transducer array are delayed based on the delay profile according to the focal points and then summed together to form the beam. It can be implemented with three components: memory for storing the incoming ultrasound waves, a delay controller for applying the delay profile to the ultrasound wave, and circuits for summing the ultrasound waves.

Fig. 2(a), (b), and (c) show the configuration of the proposed AMLA, including the operational block diagram, geometric diagram of the one-dimensional UIS, and delay profiles with the coarse delay (\( T_{CD} \)) and fine delay (\( T_{FD} \)) based on the focal point located at Fig. 2(b), respectively.

In Fig. 2(a), the proposed AMLA simultaneously generates multiple RX signals \( \{W_{1,0}, W_{1,1}, W_{2,0}, W_{2,1}, \ldots, W_{k-1,0}\} \) with different fine delays \( \{T_{FD1}(k, n) \text{ and } T_{FD2}(k, n)\} \) applied through the DAS operation during the scan time, where \( T_{FD1}(k, n) \) and \( T_{FD2}(k, n) \) represent the fine delays of the \( n \)th transceiver in the \( k \)th sub-array in the AFE IC for the 1st and 2nd beams, respectively. For example, the 1st
A sub-array of the AFE IC at the bottom of Fig. 2(a) stores the ultrasound waves received from the transducer array into the analog memory, combines the stored ultrasound waves with $T_{FD}(1, n)$ and $T_{FD2}(1, n)$, and generates $W_{1,0}$ and $W_{1,1}$. Here, $W_{1,0}$ and $W_{1,1}$ correspond to $V_{OUT}[0]$ and $V_{OUT}[1]$, as shown in Fig. 1, respectively. Fig. 2(b) shows the geometric diagram of a one-dimensional UIS. At the focal point in the $m^{th}$ scanline (FP[$m$]), the time-of-flight ($t_{delay}$) of the ultrasound wave can be expressed as

$$t_{delay} = \sqrt{(dx + R_0 \cos \theta)^2 + (R_0 \sin \theta)^2},$$  

where $R_0$ is the distance between FP[$m$] and the origin (O) that is the center of the transducer array, $\theta$ is the angle between $R_0$ and the probe face, $dx$ is the distance between each transducer and O, and $V_{tissue}$ is the acoustic velocity in soft tissue.

Fig. 2(c) shows the delay profiles of $T_{FD}$ and $T_{CD}$, which are separately applied in the AFE IC and the FPGA, respectively. The total delay ($T_{d,m}(k, n)$) of the $n^{th}$ transceiver in the $k^{th}$ sub-array with respect to FP[$m$] can be expressed with $T_{FD}$ and $T_{CD}$ as

$$T_{d,m}(k, n) = T_{CD,m}(k) + T_{FD,m}(k, n),$$

where $T_{CD,m}(k)$ is the coarse delay of the $k^{th}$ sub-array and $T_{FD,m}(k, n)$ is the fine delay of the $n^{th}$ transceiver in the $k^{th}$ sub-array for FP[$m$]. Also, $T_{CD,m}(k)$ is the minimum $T_{d,m}$ of the transceivers in the $k^{th}$ sub-array, which can be expressed as

$$T_{CD,m}(k) = \min_{n \in k} T_{d,m}(k, n).$$

In order to increase the frame rate through the proposed AMLA, the MADL in the AFE IC should cover the range of $T_{FD}$ with respect to FP[$m$] and its adjacent scanline with the corresponding focal point (FP[$m-1$]) without changing $T_{CD}$. Therefore, the range of $T_{FD}$ in the MADL should be

$$0 \leq T_{FD} \leq \max\{\text{diff}[T_{CD,m}(1)], \text{diff}[T_{CD,m}(k)]\} + T_{FD_{MAX}},$$

where $\text{diff}[T_{CD,m}(k)]$ and $T_{FD_{MAX}}$ are the difference in $T_{CD}$ in the $k^{th}$ sub-array between FP[$m$] and FP[$m-1$], and the maximum fine delay over all the delay profiles, respectively.

In this way, the AMLA in the proposed AFE IC generates multiple RX signals by controlling only $T_{FD}$ in Eq. (6), unlike the conventional DMLAs covering the entire delay range; this results in an improvement in the computational efficiency. Moreover, the number of outputs ($V_{OUT}$) in Fig. 1 does not increase by a factor of $N_{MLA}$, but rather decreases to 4.

**C. PIEZOELECTRIC MICROMACHINED ULTRASOUND TRANSDUCER**

In this work, the PMUT transducer is designed with a focus on optimizing the TX performance to mitigate the needs of the HV electronics. Fig. 3(a) and (b) show the configuration of a PMUT and cross-sectional view of its unit cell, respectively, where one sub-channel of the PMUT is configured with 4 unit cells. The membrane of the unit cell is made of $\text{SiO}_2$ and Si, and its diameter was set to 80 $\mu$m. In addition, the top electrode (Pt) diameter was determined to be 48 $\mu$m (60% coverage) considering a maximum TX pressure through the frequency sweeping analysis. Here, Au is used for the top electrode interconnection of the 4 unit cells to configure the PMUT sub-channel. The material of the PZT is PZT-5H, and its thickness is designed to be 1.0 $\mu$m in order to acquire sufficient acoustic pressure, even when a lower-voltage device is used for the TX circuit. Accordingly, the TX circuit should be carefully designed in consideration of the large capacitance of the PMUT channel of 6.7 nF, which is calculated to be a load capacitance of a unit cell of 34.7 pF × 4 unit cells × 48 sub-channels for each transceiver of the AFE IC. The sensitivities of the PMUT used in this work were simulated using COMSOL Multiphysics [18] under the water loading condition. For the TX sensitivity, a single sine wave with 40 VPP at a center frequency of 3.6 MHz is biased to the PMUT, resulting in a TX acoustic pressure of 2.7 MPa (corresponding to a TX sensitivity of 67.5 kPa/V) at the center surface of the membrane. For the RX sensitivity, it is assumed that a plane wave with an acoustic pressure of 1 kPa propagates 1 mm from human body to the surface of the membrane, resulting in a generation of an RX sensitivity of 1.2 mVPP. Although the RX sensitivity of this work is ten times less

![Diagram](image-url)
than that of [19] (13.4 mV/kPa), the TX sensitivity of this work, which is about fifteen times greater than that of [19] (3.9 kPa/V), enables 10 VPP implementation for the TX operation. In addition, the fractional bandwidth (f_{BW}) is simulated to be 80% at a center frequency of 3.6 MHz under the water loading condition, as shown in Fig. 4. Moreover, the pitch in the array is determined to be 214 μm, which is half the wavelength at a center frequency of 3.6 MHz, considering the minimization of the side lobe [20]. Based on the determined pitch, the 1-D linear array with 128 channels has a size of 2.7 cm (lateral) × 1.0 cm (elevational). Subsequently, the angular resolution and focused beamwidth are respectively calculated to be 1° and 1.6 mm at focal depth of 10 cm, according to [21].

III. CIRCUIT IMPLEMENTATION

A. TX CIRCUIT

The TX circuit in the transceiver shown in Fig. 1 is configured with only digital logics, making it simple and flexible. The TX controller applies D_{AFE, IC} to V_{IN, TX} so as to generate V_{LV, TXS} for the HV pulser. Here, the frequency, maximum TX fine delay, and number of pulses included in D_{AFE, IC} used in this work are 1.2 MHz to 6.67 MHz, 1.6 μs, and 0 to 31, respectively.

Fig. 4 shows the HV pulser, which uses two stages (stages 1 and 2) to produce a biphasic waveform. V_{LV, TXS}, including V_{PU}, V_{PD}, V_{RZU}, and V_{RZD}, are made of 5 V digital signals for pull-up, pull-down, return-to-zero-up, and return-to-zero-down, respectively. Stage 1 pulls the output of the HV pulser (V_{HV, OUT}) up to VDDM (5 V) using V_{PU} and down to VSSM (−5 V) using V_{PD}. Then, stage 2 returns V_{HV, OUT} to 0 V from 5 V or −5 V and generates biphasic waveforms with V_{RZU} and V_{RZD}. Buffers in each stage are implemented to sufficiently drive the load capacitances of laterally diffused MOS (LDMOS) transistors, M1 to M4. Accordingly, the rising and falling times of V_{HV, OUT} are determined to be 25 ns to properly generate ultrasound waves in the PMUT array. Level shifters (LSs) are implemented to provide signals with a voltage range of 0 V to −5 V to the buffers so as to drive the pull-down transistors, M2 and M4. The protection diodes, D1 and D2, are implemented only in stage 2 to protect transistors M3 and M4, while preventing V_{HV, OUT} from being clamped to 0 V.

FIGURE 4. Simulated frequency response of the PMUT.

B. LNA AND VGA IN THE RX CIRCUIT

Fig. 6 shows the schematics of the LNA and VGA in the RX circuit, which are implemented in each transceiver to amplify the ultrasound waves generated from the PMUT. The gain of the LNA is determined by the maximum amplitude of the ultrasound waves and the ratio of the ADC aperture [22]. Here, the maximum amplitude of the ultrasound waves is determined to be 0.3 VPP based on the simulated sensitivities of the PMUT, while the conversion range of the ADC is determined to be a supply voltage of 1.8 V. Consequently, the maximum gain of the LNA is determined to be 9.5 dB when considering a D2S buffer gain of 6 dB.

To reduce the power consumption, the LNA shown in Fig. 6(a) adopts an open-loop-based structure with wide bandwidth [23]. It controls its gain from 3 dB to 9.5 dB by trimming the resistance values in Kelvin switches using a 2-bit register (REG_LNA[1:0]) to avoid signal saturation. Its input (V_{IN}) is AC-coupled to reduce the noise component and block the DC signal passing through R1 and C1, which are designed to have a cut-off frequency of 0.3 MHz. Here, V_{IN} is converted into the differential signal (V_{OUTP, LNA} and V_{OUTN, LNA}) in order to achieve better noise immunity of the AFE IC.

As the ultrasound wave travels through the human body, its energy is exponentially lost. The VGA is employed to compensate for such energy loss of the ultrasound wave, of which the maximum value (A_{att, max}) can be expressed as

$$A_{att, max} = \alpha \times 2 \times d_{max} \times f_u,$$

where $\alpha$ is the attenuation coefficient of soft tissue (typically 0.5 dB/MHz/cm), $d_{max}$ is the maximum focal depth, and $f_u$ is the maximum frequency of the ultrasound wave. Here, $A_{att, max}$ is calculated to be 75 dB at a $d_{max}$ of 15 cm and an $f_u$ of 5 MHz, which is determined by considering an 80% fractional bandwidth at a center frequency of 3.6 MHz. Since
FIGURE 6. Schematics of (a) LNA and (b) VGA without the common mode feedback circuits.

the minimum dynamic range required for a display image is considered to be about 42 dB with a margin of 12 dB for image generation [22], the total dynamic range required for the UIS is determined to be 117 dB; this should be achieved through the LNA, VGA, and ADC. Thus, the VGA requires a gain of 29.5 dB when the resolution and SNR of the ADC are assumed to be 12-bit and about 72 dB, respectively. The continuous VGA shown in Fig. 6(b), which consists of an R-2R attenuator, Gaussian interpolator, $g_m$ stage, and main amplifier, is implemented to achieve dB-linear characteristics for exponential energy suppression in the human body. Since each tab in the R-2R attenuator has a gain attenuation of 6 dB, five tabs are selected to cover the gain of 29.5 dB required for the VGA. The $g_m$ stages have the same number of stages as the number of tabs in the R-2R attenuator, and the Gaussian interpolator adjusts the total transconductance value of the $g_m$ stage by using ramp signals, $V_{CONP}$ and $V_{CONN}$. The main amplifier with a fixed gain of 29.5 dB is designed with a current feedback topology to avoid the trade-off between gain and bandwidth.

C. MULTIPLE ANALOG DELAY LINE (MADL) IN THE RX CIRCUIT

Fig. 7(a) shows the block diagram of the MADL in a transceiver of the proposed AFE IC, which employs a pipelined sample-and-hold architecture with a current-splitting method [24] to decrease the power consumption and increase the area efficiency. The MADL is configured with 41 analog memory cells, 4 buffering current sources ($I_{BUF}$), and 4 flipped-voltage-followers (FVFs). The control block receives $CLK_{80M}$ and $DAFE_{IC}$ from the LVDS RX, and then converts three 6-bit $DFD_{RX}$ in $DAFE_{IC}$ to three 41-bit one-hot-encoded signals ($WRITE[40:0]$, $READ_1[40:0]$, and $READ_2[40:0]$) to control the analog memory cells of the MADL. An analog memory cell is a unit cell that samples $V_{INP}$ or $V_{INN}$, and applies $T_{FD}$ to the sampled signal. Considering an extension to 128 channels for the 1-D linear ultrasound probe, the range of $T_{FD}$ in the MADL is set to 1 $\mu$s at a sampling frequency of 40 MHz, according to Eq. (6). This results in the implementation of 41 analog memory cells. Fig. 7(b) shows the schematic of the analog memory cell that consists of a buffer; a sampling capacitor ($C_{MOS}$) used as an analog memory cell; and three switches, including a writing switch ($SW_{WRITE}$) and two reading switches ($SW_{READ1}$ and $SW_{READ2}$). Here, $WRITE[i]$, $WRITE_{b[i]}$, $READ[i]$, and $READ_{b[i]}$ are the write enable signal, write enable bar signal of $SW_{WRITE}$, read enable signal, and read enable bar signal of $SW_{READ}$, respectively, where bar signals are generated from each analog memory cell (inverters are not shown in Fig. 7(b)). Since the conventional charge-based operation [25] suffers from loss of the data sampled in the
sampling capacitor once one reading operation is finished, a voltage-based operation that uses an inserted buffer is employed for the MADL in this work. This makes the sampled data stay in the CMOS capacitor, thus enabling simultaneous fine-delay control for the proposed AMLA. The FVFs are implemented to shift the DC output voltage level to $\frac{1}{2}V_{DD}$, while driving the fine-delayed differential outputs ($V_{OUTP[0]}$, $V_{OUTN[0]}$, $V_{OUTP[1]}$, and $V_{OUTN[1]}$) into D2S buffers. The differential outputs are averaged with the 4-channel transceiver outputs in the sub-array, thus suppressing noise by a factor of two, which is the root of the number of transceivers in the sub-array.

For proper read operation, the MADL is implemented in a way to protect the sampled data in CMOS from distortion, which can be caused by the following factors. First, the clock feedthrough and charge injection of $SW_{WRITE}$ due to the parasitic capacitances are taken into account by designing both the NMOS and PMOS transistor sizes to be equal. Next, $WRITE[i]$ between the adjacent analog memory cells is designed to avoid overlapping so as to prevent sampled data loss caused by charge sharing. Moreover, the distortion of the sampled data during the transition of the buffer output and the kT/C noise are taken into account by using a large capacitance value of CMOS of 512 fF, which is 80 times greater than the parasitic capacitance value of M1, considering the 12-bit ADC resolution [24]. In addition, the off-state leakage current flowing through $SW_{WRITE}$, which dominantly affects the analog memory cell in the 0.18-µm process used in this work, is investigated through simulation. This shows a negligibly small value of only few pA, which corresponds to less than 1 LSB (0.4 mV) of the voltage variation in CMOS at a 12-bit ADC resolution during a maximum fine delay of 1 µs.

Fig. 8 shows the timing diagram of the MADL with a 4-channel transceiver. The control block generates two clock signals: $CLK_1$ with 40 MHz and $CLK_2$ with 1/4 phase-shifted 40 MHz from $CLK_{80M}$. This is followed by the production of $WRITE[N]$, which has a width of 18.75 ns ($t_{WR}$) that is sufficient for avoiding the distortion due to the charge sharing between the adjacent analog memory cells. When $WRITE[N]$ becomes high, $SW_{WRITE}$ are turned on, followed by sampling $V_{INP}$. After that, $SW_{READ1}$ and $SW_{READ2}$ are turned on when $READ_1[N]$ and $READ_2[N]$ become high, respectively. Then, the proposed AMLA simultaneously generates $V_{OUTP[0]}$ and $V_{OUTP[1]}$ according to the fine delay of the sampled data, which is determined by the difference in delays between $SW_{WRITE}[N]$ and both $SW_{READ1}[N]$ and $SW_{READ2}[N]$. The MADL has a minimum unit delay ($t_d$), which is determined by a sampling frequency of 40 MHz, and a maximum delay of $(N-1) \times t_d$, as depicted in Fig. 8.

**IV. EXPERIMENTAL RESULTS**

Fig. 9 shows a microphotograph of the proposed AFE IC, which was fabricated using a 0.18-µm HV SOI process with 1 poly and 6 metal layers, and occupied an active area of 2.56 mm × 1.68 mm. Pads for $V_{HV\_OUT}$ and $V_{OUT[3:0]}$ are located at the top and bottom sides, respectively, where $V_{HV\_OUT}$ for each channel is double-wire bonded to reduce the voltage drop caused by the resistance and inductance of the wire. In addition, test pads on the left and right sides were implemented to test circuits within the AFE IC.
In the measurement of the proposed AFE IC, the TX load of the PMUT was modeled with passive devices on the printed circuit board, and an arbitrary waveform generator was used to supply the RX input signal, where the range is determined based on the simulated sensitivities of the PMUT.

Fig. 10 shows the measurement results of $V_{HV\text{-OUT}}$ after the TX operation is completed. Here, the operating frequency is selected to be a main frequency of 3.6 MHz, and the number of occurring pulses is set to one. Different fine delays of 375 ns, 175 ns, 75 ns, 25 ns, and a maximum value of 1.6 $\mu$s are applied to the TX circuits. The measurement results show that each TX circuit produces a 10 V $V_{PP}$ $V_{HV\text{-OUT}}$ with its corresponding fine delay, indicating that the proposed TX circuit works properly.

Fig. 11(a) shows the measured transient waveform of the VGA output ($V_{OUT\_VGA}$) when a 3 mV $V_{PP}$ sine wave with an operating frequency of 3.6 MHz is applied to the input of the AFE IC, given a focal depth of 150 mm. The measurement results show that as $V_{CONP}$ linearly increases with time, $V_{OUT\_VGA}$ exponentially increases due to its dB-linear characteristics. This results in an amplification of up to 479 mV, which corresponds to 44.06 dB. In addition, Fig. 11(b) shows the measured transfer function of $V_{OUT\_VGA}$, excluding the 6 dB gain of the D2S buffer. This shows the dB-linear characteristics according to $V_{CONP}$, while having the gain range from 8.1 dB to 38.3 dB at a center frequency of 3.6 MHz. The measured maximum gain of 38.3 dB is slightly attenuated by 0.7 dB, as compared with a target gain of 39 dB, due to the R-2R attenuator in the VGA and the AC-coupling capacitors, which are used to isolate the DC voltage in the measurement setup. In addition, the cut-off frequency of the high-pass filter was measured to be 0.3 MHz, showing the proper waveform tendency of the band-pass filter. In addition, Fig. 11(c) shows the simulated and measured input referred noises of the LNA and VGA of 1.04 nV/ $\sqrt{Hz}$ and 1.55 nV/ $\sqrt{Hz}$, respectively. The difference between the above simulation and measurement results is the noise caused by the off-chip component on PCB for the PMUT, which is induced into the input of the LNA.

Next, $V_{OUT[1:0]}$, which are the outputs of the sub-array in the AFE IC, were measured to verify the amplification of the LNA, VGA, and D2S buffers, as well as the MLA operation of the MADL. Fig. 12(a) and (b) respectively show the measured
FIGURE 12. Measured outputs of a sub array in the AFE IC (V_{OUT}[1:0]) when the fine delay differences between V_{OUT}[0] and V_{OUT}[1] are (a) 25 ns and (b) 975 ns.

V_{OUT}[1:0] when different fine delay differences of 25 ns and 975 ns are applied to the V_{OUTP,VGA} and V_{OUTN,VGA} in the MADL followed by the D2S buffers, producing V_{OUT}[1:0]. Here, two 6-bit fine delay data, 6’b000001 (25 ns delay) and 6’b000010 (50 ns delay), are simultaneously applied for a 25 ns fine delay difference, whereas a minimum fine delay (25 ns delay, 6’b000001) and a maximum fine delay (1 \mu s delay, 6’b101000) are simultaneously applied for a 975 ns fine delay difference. In addition, both the measured V_{OUT}[1:0] were amplified to approximately 420 mV_{PP} corresponding to 42.9 dB, which is a little less than the target gain of 479 mV_{PP} corresponding to 44.06 dB. This slight attenuation is caused by the buffers and FVF s of the MADL, each of which has a gain less than unity (≈0.93). Therefore, these measurement results demonstrated that the proposed AFE IC worked properly for the AMLA operation of the MADL and amplification of the LNA, VGA, and D2S buffers.

Fig. 13 shows the measured FFT (fast Fourier transform) of V_{OUT}[0] and V_{OUT}[1] with different fine delays at a center frequency of 3.6 MHz. The amplitudes of the 2nd and 3rd harmonic distortions (HD2 and HD3) were measured to be 44.7 dB relative to the carrier (dBc) and 42.8 dBc, both of which are greater than 40 dBc. This shows that the outputs of the proposed AFE IC were little distorted during the amplification and MLA operation.

Consequently, the measurement results in Figs. 12 and 13 demonstrate that the proposed AMLA in the proposed AFE IC properly performs simultaneous delay operations, thereby increasing the number of scanlines per second, resulting in an increased frame rate.

Table 1 summarizes the performance comparison of the proposed AFE IC with previous works for UIS applications. The voltage level of the proposed TX circuit was much lower than those of [12], [14], and [15], indicating that the PMUT used in this work can be adequately employed for transducers in low-power UIS applications. The number of scanlines
TABLE 1. Performance summary and comparison.

| PERFORMANCE COMPARISON | TBCAS15 [12] | ASSCC16 [13] | TUFFC18 [14] | JSSC19 [15] | This work |
|------------------------|--------------|--------------|--------------|--------------|-----------|
| Transducer             | Bulk PZT     | PMUT         | CMUT         | Bulk PZT     | PMUT     |
| Dimension / # of channels | 1-D / 7-ch. | 1-D / 8-ch. | 2-D / 256-ch. | 2-D / 3072-ch. | 1-D / 8-ch. |
| Process                | 0.18-μm HV   | 65-nm CMOS   | 0.18-μm HV SOI | 0.18-μm HV SOI | 0.18-μm HV SOI |
| TX voltage             | 32 Vpp       | 6 Vpp        | 30 Vpp       | 138 Vpp      | 10 Vpp   |
| TX waveform            | Monophasic   | Monophasic   | Unipolar     | Biphasic     | Biphasic |
| Center frequency        | 3.2 MHz      | 250 kHz      | 4.2 MHz      | 1.6 MHz      | 3.6 MHz  |
| Target focal depth (d_{focal}) | 50 mm | 100 mm | 8.5 mm | - | 150 mm |
| Λ_{att,max}            | 16 dB        | 2.5 dB       | 3.6 dB       | -            | 54 dB    |
| Pulse repetition frequency | 14.9 kHz | 7.7 kHz | 10 kHz | 4.3 kHz | 4.6 kHz |
| MLA (N_{MLA})          | No (1)       | No (1)       | No (1)       | No (1)       | Yes (2) |
| # of scanlines per second | d_{focal} : 50 mm | 14,925 scan/s | - | - | 23,547 scan/s |
|                        | d_{focal} : 100 mm | - | 7,692 scan/s | - | - | 13,344 scan/s |
|                        | d_{focal} : 150 mm | - | - | 4,300 scan/s | 9,310 scan/s |
| Frame rate             | 2-D image\(^1\) | 149 fps @ 50 mm | 77 fps @ 100 mm | - | - | 235 fps @ 50 mm |
|                        |            | 3-D image\(^1\) | - | 62.5 fps | - | 124 fps\(^2\) |
|                        | RX Gain     | -            | -            | 116 dBΩ      | 6.2 dB | 42.9 dB |
|                        | RX HD2      | -            | -            | 46 dBc       | -      | 44.7 dBc |
| Chip area              | 2.0 mm × 1.0 mm | 0.7 mm × 1.5 mm | 6 mm × 5.5 mm | 22.4 mm × 18.6 mm | 2.6 mm × 1.7 mm |

\(^1\) 100 scanlines for a frame at each focal depth.
\(^2\) The calculated frame rate under the same conditions in [13] at viewing angles of 13.5° × 13.5° for both X and Y, and at a focal depth of 8.5 mm.
\(^3\) FoM = (energy consumption per channel/scan)/A_{att,max}, where A_{att} is the energy loss considering the focal depth and center frequency.
\(^4\) The energy consumption of ADCs is excluded.
\(^5\) Chip area including only the active area of the AFE IC.

per second (scan/s) can be obtained by a multiplication of the PRF and N_{MLA}, and the proposed AFE IC achieved the number of scanlines of 23,547 scan/s and 13,344 scan/s at focal depths of 50 mm and 100 mm, respectively, both of which are much greater than those of [12] and [13]. Even with a focal depth of 150 mm, the proposed AFE IC obtained 9,310 scan/s, achieving a frame rate of 93 fps based on Eq. (2) with 100 scanlines for a frame. This shows that the proposed AMLA can achieve a higher frame rate than previous works. Moreover, the proposed AMLA enables the proposed AFE IC to achieve a frame rate of 124 fps with a 3-D image, which is about twice greater than that of [14] with 3-D image, under the same focal depth and viewing angle conditions.

To properly verify the performance of the proposed AFE IC, a figure-of-merit (FoM) is employed using FoM = (energy consumption per channel/scan)/A_{att,max} at the given center frequency and focal depth. This FoM also considers an N_{MLA} of 2 for the proposed AMLA at a PRF, and the energy loss in dB (A_{att}). Here, A_{att} was included in the FoM to consider the energy loss that exponentially increases according to the frequency and focal depth, as expressed in Eq. (7). As a result, the proposed AFE IC achieved an FoM of 20.1 nJ/scan/db, which is the best value among the compared works, indicating that the proposed AFE IC is very energy efficient, while still achieving the highest frame rate according to the acquired scanlines. Therefore, the proposed AFE IC is suitable for UISs requiring a high frame rate. Moreover, since the proposed work had a much larger target focal depth (150 mm) than [12], [13], its active area of 2.6 mm × 1.7 mm became slightly larger; however, this is still a reasonable value for the TX circuit considering the given target focal depth.

Since the proposed AFE IC has a better FoM than previous works and the PMUT used in this work mitigates the need to use HV electronics, it can be easily extended to portable UIS applications requiring less circuit complexity and low energy consumption. Moreover, unlike conventional MLTs that cause large dynamic power consumption problems in portable UISs, the proposed AMLA is not constrained in terms of its power budget for high frame rate applications.

V. CONCLUSION

This paper proposes an AFE IC combined with a PMUT array using its simulated parameters to achieve the high frame rates needed for ultrasound imaging systems. The proposed AFE IC employs an AMLA based on a sub-array beamforming architecture to achieve a high frame rate. The MADL in the AFE IC, which operates in the voltage domain, controls different fine delays without losing the stored data during the scan time. In addition, the simulated PMUT used in...
this work allows for the use of a relatively low voltage at a 3.6 MHz center frequency. The measurement results of the AFE IC using the proposed AMLA demonstrated simultaneous control of fine delays up to 1 µs with 25 ns resolution, while also achieving more than 9,000 scan/s at a focal depth of 150 mm; this is at least twice greater than those achieved in prior works. Consequently, this large number of scanlines enabled the proposed AFE IC to achieve a high frame rate of 93 fps when 100 scanlines are used in a frame in medical UISs. In addition, the proposed AFE IC achieved the best FoM of 20 nJ/scan/dB at a focal depth of 150 mm. Moreover, the gain and HD2 of the proposed AFE IC were measured to be 42.9 dB and 44.7 dBc, respectively, showing proper RX fitness.

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