A Two-staged Adaptive Successive Cancellation List Decoding for Polar Codes

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Abstract—Polar codes achieve outstanding error correction performance when using successive cancellation list (SCL) decoding with cyclic redundancy check. A larger list size brings better decoding performance and is essential for practical applications such as 5G communication networks. However, the decoding speed of SCL decreases with increased list size. Adaptive SCL (A-SCL) decoding can greatly enhance the decoding speed, but the decoding latency for each codeword is different so A-SCL is not a good choice for hardware-based applications. In this paper, a hardware-friendly two-staged adaptive SCL (TA-SCL) decoding algorithm is proposed such that a constant input data rate is supported even if the list size for each codeword is different. A mathematical model based on Markov chain is derived to explore the bounds of its decoding performance. Simulation results show that the throughput of TA-SCL is tripled for good channel conditions with negligible performance degradation and hardware overhead.

Index Terms—Polar codes, Successive cancellation list decoding, Adaptive decoding, Markov chain, Hardware-friendly algorithm

I. INTRODUCTION

To improve error correction performance of polar codes [1], successive cancellation list (SCL) decoding [2],[3] is the most popular decoding choice. \( L \) (called the list size) successive cancellation (SC) decodings [4],[5] are executed concurrently to decode a polar codeword and \( L \) candidates of decoded vectors are kept during decoding [4],[3]. Compared with SC decoding, SCL decoding improves the error correction performance as the probability of one of the \( L \) candidates to be the correct decoded vector is higher, and a larger list size brings a better error correction performance. In [6], cyclic redundancy check (CRC) codes are concatenated as outer codes with polar codes, and CRC is applied to all the candidates to see whether any candidate is the valid decoding output. From the experimental results presented in [7],[8], the CRC-aided polar codes decoded by SCL with a sufficiently large list size (≥16) outperform LDPC codes and turbo codes.

Due to the extraordinary error correction performance of CRC-aided SCL decoding, its hardware implementation has attracted much research interest recently. Several different VLSI architectures [8]–[16] have been proposed for SCL. The decoding throughputs achieved by the state-of-the-art architectures are shown in Fig. 1. It can be observed that the decoding throughputs of all the architectures are degraded with the list size. This is mainly because the critical path delay of some of the critical functional modules [17]–[19] in these architectures increases rapidly when the list size is increased. Although efforts have been made to optimize these modules as well as the overall architecture, the throughput is still reduced due to the high decoding complexity.

To increase the decoding speed so that it can match with that of LDPC or turbo code architectures, adaptive SCL (A-SCL) decoding was proposed in [20] and a corresponding software decoder was implemented on CPU in [21]. This algorithm first uses a single SC to decode a codeword. If the decoded vector cannot pass CRC, the list size is doubled and the decoding repeats. This process is iterated until a valid vector is obtained or a pre-defined \( L_{\text{max}} \) is reached. Experimental results [20] show that A-SCL significantly reduce the average list size \( L \) required to achieve an equivalent error correction performance of SCL decoding with \( L = L_{\text{max}} \). The average throughput of executing A-SCL on hardware can benefit from the reduction on the \( L \). However, if the algorithm is directly mapped to hardware, the decoding latency of each codeword is different, which may not support applications that need a constant input transmission data rate. Also, the hardware complexity is high as multiple SCL modules are needed.

The main contributions of this work are outlined as follows:

1) We simplify the algorithm of A-SCL [20] and propose a two-staged adaptive SCL (TA-SCL) decoding. Different from [20],[21], TA-SCL is more hardware-friendly as it is able to achieve a high throughput for applications that require a fixed input transmission data rate.

2) An analytical model of TA-SCL is developed based on Markov chain to analyse its error correction performance. Its accuracy is verified by simulation, and it can be used for the optimization of the VLSI architecture for TA-SCL.

3) Simulation results show that the throughput of TA-SCL with \( L_{\text{max}} = 32 \) is two times higher than that of the SCL decoder with \( L = 32 \) [8] for good channel conditions with negligible performance degradation. The throughput is also higher than those of SCL decoders with smaller list sizes [12],[13].

II. MISCELLANEOUS

A. Introduction of Polar Codes and SCL

Polar codes are a family of block codes [1] characterised by an \( N \times N \) binary generator matrix \( F_N \), where \( N \) is the code length. The source word \( u_N \) and codeword \( x_N \) of an \( N \)-bit frame are both binary vectors, and the encoding can be expressed as \( x_N = u_N \cdot F_N \). Among all the \( N \) bits in a frame, only \( K \) bits are used to send information and the rest are frozen bits which are set to 0. The last \( r \) information bits are used to transmit the checksum of the CRC code. SCL decoding of polar codes decodes a codeword bit-by-bit in a serial order, and the decoding process is similar to a search problem on a binary decoding tree whose depth is \( N + 1 \). A
Overflow

B. Adaptive SCL with CRC

Adaptive SCL with CRC was proposed in [20] and its operation is summarised in Algorithm 1. Each time, a new codeword which contains $N$ log-likelihood ratios (LLRs) of the input values is sent for decoding. A-SCL starts from an SCL with $L = 1$, i.e. a single SC. If there is at least one decoded vectors that pass CRC at the end of decoding, the one with the highest reliability is chosen as output. Otherwise, the list size is doubled and the codeword is decoded again by an SCL with the new list size. Usually, a pre-defined $L_{\text{max}}$ is used to limit the computational complexity, that is, after the decoding using an SCL with $L_{\text{max}}$, the decoding terminates even when there is no valid candidate. According to [20], the error correction performance of A-SCL is the same as that of an SCL with $L_{\text{max}}$. At the same time, as most of the valid decoded vectors can be obtained using SCL with smaller list sizes, the average list size $L$ of A-SCL is much smaller than $L_{\text{max}}$ and its average decoding speed is much higher than that of SCL with $L_{\text{max}}$.

C. Problems of Implementing A-SCL on Hardware

If the A-SCL algorithm is implemented on hardware, the throughput will be much higher than that of a traditional SCL.

III. TWO-STAGED ADAPTIVE SCL

A. Algorithm of TA-SCL

As mentioned above, the average list size $L \ll L_{\text{max}}$ in A-SCL. Actually, $L \approx 1$ in a high signal-to-noise ratio (SNR) operation region [20], indicating that most codewords are decoded by the single SC correctly. At the same time, the error correction performance follows that of SCL with $L_{\text{max}}$. Based on these observations, we propose a hardware-friendly two-staged adaptive SCL. The block diagram of TA-SCL and its timing schedule are shown in Fig. 3 and Fig. 4, respectively. Basically, it includes two SCL decodings, which are an SCL decoding with small list size (not necessarily to be 1), denoted as $D_s$, and an SCL decoding with large list size, denoted as $D_l$. Each codeword from the channel is first decoded by $D_s$. Most of the time, the decoded vector can be decoded correctly. If none of the candidates in the list passes CRC after this decoding, e.g. fr.1 in Fig. 3, the current codeword will be decoded again by $D_l$. This decoding usually takes longer time than decoding using $D_s$. However, different from A-SCL, $D_s$ will bring in and decode the next codeword from the channel input immediately instead of waiting for $D_l$ to finish decoding the current codeword. The continuous running

![Fig. 2. The decoding tree of a polar code whose $N = 4$ and $L = 2$. The $i$th source bit $u_i$ is mapped to the nodes of the decoding tree at level $i + 1$. A path from the root node to a leaf node represents a candidate of decoded vector. For a parent at level $i$, its left and right children at level $i + 1$ correspond to the expansions of the decoding path with $u_i = 0$ and 1, respectively. In the example, the path marked with single crosslines represents a decoding vector 0010. If a bit, such as $u_0$ in Fig. 2 is a frozen bit, the sub-tree rooted at the right child does not contain any valid candidate and hence is pruned. Therefore, the total number of the possible candidates in a decoding tree is $2^K$, and it is too large to exhaustively search the decoding tree to obtain the correct decoded vector when a practical code length is used. To limit the computational complexity, each SCL decoding has a pre-defined list size $L$. If the number of paths at a certain level exceeds $L$, a list management operation is used to select and keep the best $L_s$ survival paths and discard the rest ones. The example in Fig. 2 maintains a list with $L = 2$, so another path marked by double crosslines representing the decoded vector 0100 is also kept in the list. At the end of the decoding, the path in the list that passes CRC is selected as the output vector.

Algorithm 1: Adaptive SCL with CRC

Input: $N$ channel LLRs; Initial: $L = 1$;
while $L \leq L_{\text{max}}$ do 
- SCL with $L$: codeword from channel;
  if $\geq 1$ paths pass CRC then
    Output the most reliable path; Break;
  else
    $L = 2 \cdot L$;
end

Fig. 3. Block diagram of TA-SCL.

Fig. 4. Timing schedule of TA-SCL. The codewords in gray cannot be decoded correctly by $D_s$. The circle shows a buffer overflow.

However, direct mapping of the A-SCL algorithm onto a VLSI architecture requires the architecture to support multiple SCL decodings with all $L \in \{1, 2, 4, ..., L_{\text{max}}, \max \}$. This increases the design effort and also the hardware complexity. Moreover, different codewords may need SCL with different list sizes and SCL with a larger list size has a much higher latency. When a codeword needs longer latency to decode, the input has to be interrupted until the decoding of the current frame is finished. Because of that, a directly-mapped architecture may not be able to support applications that need to have a constant input data rate, such as the channel coding blocks in communication networks.

To improve the decoding speed on hardware, a CPU-based software A-SCL decoder was proposed in [21] in which A-SCL was simplified by only using a single SC and an SCL with $L_{\text{max}}$. However, the variable decoding latency issue has not yet been addressed. Moreover, the overall latency is very large as the latency for the data movement between the memory and the computing resources is dominant. Hence, neither the original A-SCL nor the simplified A-SCL in [21] is a good choice for high-throughput VLSI implementations. To solve these issues and map A-SCL to a high-speed and efficient VLSI architecture, we propose a two-staged adaptive SCL which will be presented in the next section.
of $\mathbf{D}_s$ permits the data to be transmitted at a constant data rate which is equal to the decoding speed of $\mathbf{D}_s$, while the decoding performance is guaranteed by $\mathbf{D}_t$. Also, the hardware complexity of TA-SCL is effectively reduced as only two SCL decoders are needed.

If the channel is subject to burst errors, it is possible that a new codeword cannot be correctly decoded by $\mathbf{D}_s$ and the decoding in $\mathbf{D}_t$ has not finished yet. To deal with this, an LLR buffer is needed to store the LLRs of the codeword from $\mathbf{D}_s$ temporarily, such as fr.3 and fr.4 shown in Fig. 4. An output buffer is also needed to re-order the decoded vectors as the codeword may be decoded out of order. For example, fr.7–fr.9 are stored in the output buffer until the decoding of fr.6 finishes.

### B. Error Correction Performance of TA-SCL

To analyse the error correction performance of the TA-SCL decoding, we define its parameters as follows.

- $L_s/L_t$: list sizes of $\mathbf{D}_s/\mathbf{D}_t$.
- $\epsilon_s/\epsilon_t$: BLERs of $\mathbf{D}_s/\mathbf{D}_t$.
- $t_s/t_t$: decoding time of each codeword using $\mathbf{D}_s/\mathbf{D}_t$.
- $\beta$: speed gain, which is defined as $\frac{t_s}{t_t}$. With out loss of generality, we assume $\beta \in \mathbb{Z}^+$.
- $\zeta$: size of the LLR buffer, which equals to the number of codewords that can be stored in the buffer.

We also denote a TA-SCL decoding whose speed gain is $\beta$ and buffer size is $\zeta$ as $\mathbf{D}_{\text{TA}}(\beta, \zeta)$. The TA-SCL decoding in the example shown in Fig. 4a, hence can be described as $\mathbf{D}_{\text{TA}}(3, 1)$ and the corresponding $\mathbf{D}_t$ needs $3t_s$ to decode a codeword. When a new codeword needs to be stored in the LLR buffer but the buffer is full and decoding in $\mathbf{D}_t$ has not finished yet, buffer overflow happens, which will lead to performance degradation for $\mathbf{D}_{\text{TA}}$. An example of buffer overflow is marked in Fig. 4b. Therefore, we first introduce the list sizes of $\mathbf{D}_{\text{TA}}(\beta, \zeta)$ as

$$l_s(\beta, \zeta) = \sum_{i=0}^{\zeta} \binom{i}{\beta}.$$

Hence, decoding will be interrupted to derive the relationship between $\Pr(\text{Overflow})$ and the parameters of $\mathbf{D}_{\text{TA}}$ in the next sub-section.

### C. Analytical Model of TA-SCL based on Markov Chain

To model the behavior of $\mathbf{D}_{\text{TA}}(\beta, \zeta)$, we first introduce the states that the decoder can operate at. In particular, these states reflect whether buffer overflow will happen. We define the number of codewords stored in the LLR buffer as $i_\zeta$ and the remaining time required to finish the decoding of $\mathbf{D}_t$ (in term of $t_s$) as $i_\beta$. Each codeword in the LLR buffer needs $\beta t_s$ to decode. Then, the state of TA-SCL indicates the time to clear the buffer and is defined as

$$X_\tau = \beta \cdot i_\zeta + i_\beta, \quad i_\zeta \in [0, \zeta], \; i_\beta \in [0, \beta],$$

(2)

To deal with buffer overflow, either the codeword in $\mathbf{D}_t$ or the new one should be thrown away. In the following, we just analyse the former case and the latter case can be analysed in the same way.

We show an example for $\mathbf{D}_{\text{TA}}(3, 1)$ in Fig. 5a, where the black and white arrows represent the probabilities of $\epsilon_s$ and $\epsilon_t$, respectively. The first three columns show $i_\beta$, $i_\zeta$ and $X_\tau$, respectively. Typical transitions from hazard and safe states are marked with “H” and “S” in the figure, respectively. Note that the transition from state 0 is a little different as $\mathbf{D}_t$ is idle.

Suppose that $\epsilon_s$ (BLER of $\mathbf{D}_s$) follows an identical and independent distribution (IID). Then, the state transitions only depend on current state of $\mathbf{D}_{\text{TA}}(\beta, \zeta)$ and $\epsilon_s$. Hence, decoding with $\mathbf{D}_{\text{TA}}$ is a Markov process and can be modeled with a Markov chain. The state diagram of $\mathbf{D}_{\text{TA}}(\beta, \zeta)$ can be easily obtained by finding out all the possible state transitions in Fig. 5a. Fig. 5b shows the state diagram of $\mathbf{D}_{\text{TA}}(3, 1)$. For further mathematical analysis, we map the state diagram to a transition matrix $P$ whose size is $S \times S$. An element $P_{x,y} \in P$ ($x, y \in [0, S-1]$) corresponds to the transition probability from state $x$ to state $y$, i.e.,

$$P_{x,y} = \Pr(X_{\tau+1} = y|X_\tau = x),$$

(3)

where $X_\tau$ is the current state and $X_{\tau+1}$ is the next state. The transition matrix of $\mathbf{D}_{\text{TA}}(3, 1)$ mapped from the state diagram is

$$P_{\text{TA}} = \begin{bmatrix} \epsilon_s & 0 & 0 & 0 & 0 & 0 \\ 0 & \epsilon_s & 0 & 0 & 0 & 0 \\ 0 & 0 & \epsilon_s & 0 & 0 & 0 \\ 0 & 0 & 0 & \epsilon_s & 0 & 0 \\ 0 & 0 & 0 & 0 & \epsilon_s & 0 \\ 0 & 0 & 0 & 0 & 0 & \epsilon_s \end{bmatrix}.$$  

(4)

With the transition matrix $P$, we can do steady-state analysis for $\mathbf{D}_{\text{TA}}$. Suppose that the decoding begins with $\mathbf{D}_{\text{TA}}$ at state 0, i.e., the state probability $\lambda_0 = [1, 0, \ldots, 0]$. After $k \cdot t_s$ ($k \in \mathbb{Z}^+$), the state probability becomes $\lambda_k = \lambda_0 \cdot P(k)$. Define $P_\infty = \lim_{k \to \infty} P(k)$, then the steady-state distribution $\lambda_\infty$ of $\mathbf{D}_{\text{TA}}$ is

$$\lambda_\infty = \lambda \cdot P_\infty = \{(P_\infty)_{0,0}, \ldots, (P_\infty)_{0,\beta+\zeta}\}.$$  

(5)

Actually, all the lines of $P_\infty$ are the same, which means the
steady-state distribution is irrespective of the initial state \( \lambda_0 \) of \( D_{TA} \). Buffer overflow happens when \( D_{TA} \) is in any hazard state and \( D_s \) cannot decode the next codeword correctly, and the probability of buffer overflow is then expressed as

\[
\Pr(\text{Overflow}) = \epsilon_s \cdot \Pr(\zeta = \iota \text{ and } i_\beta > 1) \label{eq:overflow}
\]

\[
= \epsilon_s \cdot \Pr(X_\tau > \beta \zeta + 1),
\]

\[
= \epsilon_s \cdot \sum_{i=\beta \zeta+2}^{\beta \zeta+s} (\lambda_{\infty})_i.
\]

This probability of overflow bounds \( \epsilon_{D_{TA}} \) in (1). It is a function of error correction performance \( \epsilon_s \), speed gain \( \beta \) and buffer size \( \zeta \), i.e., \( \Pr(\text{Overflow})=f(\epsilon_s, \beta, \zeta) \). If \( \beta \) and \( \zeta \) are fixed, the \( \Sigma \) term and hence \( \Pr(\text{Overflow}) \) is monotonically increasing with respect to \( \epsilon_s \). The proof is omitted due to page limitation and will be given in our future work. The monotonicity indicates we can either increase \( L_s \) or the SNR to get a better error correction performance.

We will show the accuracy of the proposed model by simulation results in the next section. We will also show that TA-SCL can improve the decoding throughput with a small hardware overhead.

IV. EXPERIMENTAL RESULTS

A. Accuracy of the Proposed Model

To verify the accuracy of the proposed model, we run simulations for a polar code with \( \{N, K, r\} = \{1024, 512, 24\} \) under AWGN channel conditions. The list sizes of the two component SCL decoders are \( L_s = 1 \) and \( L_t = 32 \), respectively. The simulated BLER results of \( D_{TA} \) under different speed gain and buffer sizes are obtained at an SNR of 2dB and are compared with the upper bounds calculated using (1) and (8).

Fig. 6 summarizes the performance loss with respect to the speed gain \( \beta \) when different \( \zeta \) are used. Here, the performance loss is calculated by \( \frac{\epsilon_{D_{TA}} - \epsilon_s}{\epsilon_s} \cdot 100\% \). The solid lines and the dashed lines show the calculated and simulated results, respectively. It can be seen that these two lines are almost overlapped, indicating \( \epsilon_{D_{TA}} \) is approximately equal to its upper bound derived in (8). The proposed model can thus be used to estimate the error correction performance of an \( D_{TA} \) accurately. The results also show that a larger buffer size enables the decoding to run at a higher speed gain with the same constraint of performance loss.

B. Analysis of Hardware Gain

In this sub-section, we show the improvement of hardware performance achieved by the proposed TA-SCL decoder. We use a polar code with \( \{N, K, r\} = \{1024, 512, 24\} \) and \( L = 32 \) as an example. The hardware performance of some VLSI architectures of SCL decoder in the literature [8], [22] is shown in Table I. They are used as the component SCL decoders in the TA-SCL decoder. Fig. 7 shows the error correction performance of \( D_{TA} \) with buffer size \( \zeta = 6 \). When the target \( \beta \) is 3, there is almost no performance degradation at a high SNR range (\( \geq 1.6\text{dB} \)) comparing with the baseline of \( \zeta = 6 \). The degradation is obvious at a low SNR range. If the target \( \beta \) is reduced to 2, the decoder can work in a wider range of SNR down to 1.4dB. All these observations is consistent with the intuitions mentioned in Section IV. It is noted that the throughput of \( D_{TA} \) is lower than \( D_s \) in both cases, so the speed gain \( \beta \) of up to 3x is achievable. The overall throughput of TA-SCL is also higher than that of the SCL decoders with smaller list sizes as shown in Fig. 1 [12], [13].

The area of the proposed architecture is shown in Table I which is estimated based on the results reported in the literature [8], [22]. It equals to the sum of area of the two SCL modules, the LLR buffer and the output buffer. As the area of the \( D_t \) module is dominant, the proposed \( D_{TA} \) only has a 18% area overhead. Moreover, due to the throughput improvement, the area efficiency of \( D_{TA} \) is also much higher than that of \( D_t \).

V. CONCLUSION

In this work, a two-staged adaptive SCL is proposed. This algorithm can support data input at a fixed data rate and has a low hardware complexity. To analyse its error correction performance, an analytical model is also proposed and its accuracy is then verified by simulations. With a good selection of the parameters of TA-SCL using the proposed analytical model, an optimal tradeoff between speed gain, error correction performance loss and hardware overhead can be obtained for designing the VLSI architecture.
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