High resolution digitization system for the CROSS experiment

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Abstract The signal digitization for CROSS, a bolometric experiment for the search of neutrinoless double beta decay at LSC Canfranc Underground Laboratory, will be based on a custom solution comprised of an analog-to-digital board interfaced to an Altera Cyclone V FPGA module. Each analog-to-digital board hosts 12 channels that allow data digitization up to 25 ksps per channel and an effective resolution of 21 bits at the typical sample rate required by the experiment (5 ksps). The board also allows to digitally select the cut-off frequency of the anti-aliasing filter with 10 bit resolution from 24 Hz up to 2.5 kHz, as required by fast scintillating bolometers. The FPGA is responsible for the synchronization of the analog-to-digital boards and for the data transfer to the storage, using UDP protocol on a standard Ethernet interface. Each FPGA can manage the data coming from 8 boards (96 channels), allowing an excellent scalability. In this contribution we will present a complete overview of the system, and a detailed characterization of the system performance.

Keywords Data acquisition system · High resolution · Bolometric experiment · Neutrinoless double-beta decay

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1 Introduction

CROSS (Cryogenic Rare-event Observatory with Surface Sensitivity) is a bolometric experiment devoted to the search of neutrinoless double-$\beta$ decay that will be installed in Canfranc Underground Laboratory (LSC, Spain).

The main innovation of the CROSS experiment with respect to current generation of bolometric experiments, like CUORE, is the capability to discriminate bulk events from surface background events by using pulse-shape discrimination (PSD). $0\nu2\beta$ and $2\nu2\beta$ candidate events, in fact, are expected to release their energy in the whole bulk of the crystal, while the main sources of background come from surface contamination of the crystal or from the surrounding environment. The discrimination of surface events in CROSS is possible thanks to ultra-pure superconductive Aluminum thin foils, deposited on the surface of the crystals, which act as energy absorbers for $\alpha$ surface events, providing a different dynamic in the conversion and propagation of phonons, hence a different signal shape. This technique has been already demonstrated both with Tellurium dioxide (TeO$_2$) and Lithium molybdate (LiMoO$_4$) crystals. The final choice of the $0\nu2\beta$ candidate material is still under study.

For what concern the phonon sensors, two options are being considered: NTD Germanium thermistors (widely used in bolometric experiments) and NbSi thermistors (faster and more sensitive to athermal phonons).

The adoption of PSD techniques has important implications in the design of both the front-end and back-end electronics. For what concern the DAQ system, there are some different requirements with respect to present $0\nu2\beta$ bolometric experiments (CUORE, CUPID-0, etc.):

- **Faster signals** – phonon signals in CROSS have rise times in the order of 1 ms (up to 500 Hz bandwidth), so the DAQ system should allow signal digitization at 5 ksp or faster.
- **Higher pile-up** – Lithium molybdate exhibits higher pile-up due to the higher $2\nu2\beta$ background, and this also requires a fast sampling rate, in order to properly discriminate pile-up events.
- **Higher resolution** – detector noise will be reduced thanks to the adoption of a quieter cryostat setup, so ~20 bit resolution will allow to exploit the large signal dynamic and the lower noise of both detector and front-end electronics.
- **Continuous acquisition** – this is required in order to apply more complex offline triggers and optimum filtering techniques, as successfully done in CUORE.
- **Spread in detector characteristics** – cut-off frequency should be finely tuned in order to adapt to the characteristics of each detector.

2 DAQ board for CROSS experiment

The DAQ board that has been developed for the CROSS experiment is shown in Fig. 1 while Fig. 2 shows its block schematic. The top part of the schematic shows the signal block for one channel out of the 12 available on the board.
Each channel is equipped with a 6-pole Bessel-Thomson anti-aliasing filter with 10-bit digitally selectable cut-off frequency from 24 Hz up to 2.5 kHz using high precision digital trimmers (1% absolute accuracy, 35 ppm/°C drift). The trimmers have a resistance of 100 kΩ, which allows to use high quality C0G capacitors of few tens of nF. Fig. 3 shows in more detail the schematic of the analog block. Inputs are buffered and can be grounded to allow offset self-calibration. The anti-aliasing filter can be bypassed.

Each pair of analog channels is equipped with dual-channel 24-bit ΔΣ ADCs which are able to digitize the signals up to 25 kspsc/ch in 12-channel mode or 250 kspsc/ch in 6-channel mode.

The board has output switches that allow it to operate in fully analog mode, with filtered analog signals provided to the external connector, or in fully digital mode, with digital lines to the ADCs provided to the external connector. In the CROSS experiment, this latter configuration will be used. The bottom part of the block schematic (Fig. 2) shows the slow control circuitry, responsible
of the setting of all the onboard peripherals, as well as monitoring. The onboard slow control circuit is connected via CAN bus to the experiment slow control server.

When operating in digital mode, as in CROSS, the digitized signals from the on-board ADCs are extracted from the ADCs by a commercial FPGA module (Enclustra Mars MA3) installed on the backpanel that collects the data from 8 boards (96 channels). The data interface to the ADCs uses 6 high speed (20 MHz) SPI lines, while slow control of the board is mediated by an on-board ARM Cortex-M3 microcontroller interfaced to the FPGA with CAN bus. This data is then transferred to the storage system using an inexpensive 1 Gbps Ethernet interface (optically decoupled). The chosen data transfer protocol is UDP (hardware-synthesized in the FPGA), with a maximum data rate of 768 Mbps (6 channels per board at 250 ksps and 64 bit data length). An illustration of the back-end communication is shown in Fig 4.

### 3 Board performance

The first samples of the board have been fully characterized in order to evaluate their performance. A summary of the board specifications and test results are gathered in Table 1.

The plot in Fig 5 shows the adjustment of the cut-off frequency using the digital trimmer. Six settings between 25 Hz and 2.5 kHz are selected and the transfer function is measured using an Agilent 4395A spectrum analyzer.
Table 1 Summary of specifications and performance of the system.

| Specification                              | Value                                    |
|--------------------------------------------|------------------------------------------|
| Channels                                   | 12                                       |
| Power supply                               | ±12 V, ±5.5 V                            |
| Power consumption                          | 220 mW/channel (grounded)                |
| Filter                                     | 6-pole Bessel-Thomson                    |
| Cut-off frequency                          | 24 Hz - 2.5 kHz                          |
| Cut-off frequency resolution               | 10 bit                                   |
| Input differential signal                  | ±10 V                                    |
| Gain                                       | 3.5 V                                    |
| Noise (analog)                             | < 7 μV RMS                                |
| PSRR (DC to 10 kHz)                        | -70 dB                                   |
| CMRR (DC to 100 Hz)                        | -70 dB                                   |
| ADC resolution                             | 24 bit                                   |
| Maximum sampling frequency                 | 25 kHz                                   |
| Cumulative sampling frequency              | 5.5 MHz                                  |
| Measured effective resolution (1 kHz)      | 22 bits                                  |
| Measured effective resolution (5 kHz)      | 21.3 bits                                |
| Measured effective resolution (25 kHz)     | 19.7 bits                                |
| Offset drift                               | 10 μV/°C (1 ppm/°C)                      |
| Gain error (calibrated)                    | 20 ppm                                   |
| Gain drift                                 | 10 ppm/°C                                |
| Board dimensions                           | 6U-220 (233 mm x 220 mm)                 |

Fig. 5 Analog filter transfer function at different cut-off frequency settings.

Fig. 6 Common mode rejection ratio (CMRR) at different cut-off frequency settings.

The common mode rejection ratio (CMRR) is plotted in Fig. 6. In DC, the CMRR is about −70 dB, mainly dominated by the mismatch in the gain of the input buffers (i.e. resistor mismatches). This value is largely sufficient for this application where a front-end stage is present.
Fig. 7 shows the noise of the analog filter at the same cut-off frequency settings. At low filter bandwidth (< 100 Hz), noise is dominated by the series noise of the trimmers (100 kΩ at 24 Hz), while at higher filter bandwidth, series noise of operational amplifiers becomes predominant. The contribution of both parallel and 1/f noise of the opamps was made negligible with proper selection of the opamps themselves. The total analog RMS noise is indicated in the legend of Fig. 7 and ranges from 5.7 µV at 25 Hz up to 7.1 µV at 2.5 kHz (0.1 Hz – 100 kHz bandwidth).

When the signals are read-out using the internal ΔΣ ADCs, the effective resolution is dominated by the noise of the ADC and its buffer at sampling frequencies above 5 kcps. The effective resolution is 22.0 bits at 1 kcps, 21.1 bits at 5 kcps and 19.7 bits at 25 kcps, which correspond to 4.7 µV, 9.2 µV and 24 µV RMS respectively. A noise spectrum of digitized data at 5 kcps is shown in Fig. 7.

The board has also been qualified in a climatic chamber in order to measure its stability against temperature variations, which is very important in this kind of experiments that are expected to run for long times while monitoring detector baseline stability. Offset drift was measured to be 10 µV/°C (1 ppm/°C), while gain sensitivity was measured to be 10 ppm/°C.

4 Conclusions and future developments

The board is already fully operational and characterized. It offers many improvements over widely used commercial solutions, mainly for what concern noise, stability and power consumption. Data read-out from the FPGA module has been successfully demonstrated using a provisional backpanel. Using this setup, a test with prototype CROSS detectors is foreseen in the near future, in order to qualify the system with real data from the bolometers and to compare its performance with standard commercial solutions. Following this test, the full backpanel will be designed, which will allow to test the system at full output data rate with multiple DAQ boards and also implement the required synchronization between different FPGA modules.
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