Distributed On-Sensor Compute System for AR/VR Devices: A Semi-Analytical Simulation Framework for Power Estimation

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ABSTRACT

Augmented Reality/Virtual Reality (AR/VR) glasses are widely foreseen as the next generation computing platform. AR/VR glasses are a complex "system of systems" which must satisfy stringent form factor, computing-, power- and thermal-requirements. In this paper, we will show that a novel distributed on-sensor compute architecture, coupled with new semiconductor technologies (such as dense 3D-IC interconnects and Spin-Transfer Torque Magneto Random Access Memory, STT-MRAM) and, most importantly, a full hardware-software co-optimization are the solutions to achieve attractive and socially acceptable AR/VR glasses. To this end, we developed a semi-analytical simulation framework to estimate the power consumption of novel AR/VR distributed on-sensor computing architectures. The model allows the optimization of the main technological features of the system modules, as well as the computer-vision algorithm partition strategy across the distributed compute architecture. We show that, in the case of the compute-intensive machine learning based Hand Tracking algorithm, the distributed on-sensor compute architecture can reduce the system power consumption compared to a centralized system, with the additional benefits in terms of latency and privacy.

KEYWORDS

Augmented/Virtual Reality, Near Image Sensor Processing, Distributed Compute System

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1 INTRODUCTION

Mixed Reality, consisting of Virtual Reality (VR) and Augmented Reality (AR) together, will be the next generation computing platform, dominating our relationship with the digital world for the next fifty years, much as personal computing has dominated the last fifty [1]. AI (Artificial Intelligence) processing is critical for AR/VR glasses, both for input (e.g., camera images, audio) and output (e.g., graphics rendering) [9]. Moreover, the AR/VR glasses have to deliver a responsive, low latency experience while consuming very limited power, both for battery life and to limit temperature rise on the skin for user comfort. At the system level, a large quantity of data is generated and must be processed in real time to support precise and low latency interaction between the physical world and the virtual world. In traditional AR/VR systems, the processing of the raw input data captured by several image sensors is performed in a central off-sensor edge-processor (named aggregator in Fig. 1 (a)). The new distributed on-sensor compute architecture (shown in Fig. 1 (b)) [1, 10, 11] exploits multiple levels of computing, including on-sensor processors (for initial feature extraction and first level of processing) and a nearby aggregator for further processing and final analysis. The distributed compute system allows for minimum data movement with rapid and localized inference on the sensors, where a shallow portion of each Computer-Vision Neural Network (CV NN) model is implemented. This results in significant benefits in terms of communication costs, latency constraints and privacy concerns compared to centralized computing systems. On the other hand, several challenges need to be solved to implement an on-sensor processing units capable of tackling real-time compute/memory intensive workloads in the very small footprint and low power budget of AR/VR image sensors. As illustrated in Fig. 1 (b), innovative 3D CMOS Image Sensor (CIS) architectures will permit further shrinking of the sensor footprint and introduction of key on-sensor AI functionalities. Complex three-layer wafer stacking technologies are a promising solution for intelligent image sensor fabrication with AI capabilities. Dense and tight 3D-IC technologies, such as micro-Trough Silicon Vias (μTSV) and wafer-level hybrid bonding, will enable heterogeneous monolithic integration of camera and processor. There is a clear need for integrating advanced logic as close to the sensors as possible. Moreover, use of hybrid memory hierarchy (including both SRAM and STT-MRAM) in the on-sensor computing architecture will allow for higher density and lower power. To quantify the trade-offs of Distributed On-Sensor Compute (DOSC) architectures for AR/VR workloads, a system simulation framework is required. Several accelerator simulation frameworks have been developed in recent years [2, 12, 13], mostly focused on the compute modules of the system. In this work, we propose a new semi-analytical model that captures the key technological features of the whole system hardware resources, including cameras, communication links, processors, and memories. Technological parameters used in the simulations for all modules are silicon-based. The compute and memory parameters of the system have been calibrated by using an
Figure 1: Schematic of (a) Traditional centralized camera-sensor computing architecture, (b) Distributed on-sensor computing architecture [11], where each sensor has an integrated on-sensor processor (via \( \muTSV \) and a hybrid memory hierarchy (i.e. SRAM/STT-MRAM).

Figure 2: Example of the optimal repartition of the AR/VR Hand Tracking workload [8] on the distributed on-sensor computing architecture. The workload consists in two consecutive NNs (the first for detecting hands, DetNet, and the second to estimate hand keypoint locations, KeyNet). We foresee that the first ML model (DetNet) is deployed on-sensor, while the second model (KeyNet) runs on the aggregator. Only the region of interest (ROI), as extracted from the raw image by the on-sensor processor, is transmitted to the aggregator through the energy-hungry MIPI serial interface.

event-based silicon-calibrated simulator (GVSoC [3, 6]). Finally, for the system modeling demonstration, we focus on a common AR/VR workload: the Hand Tracking algorithm [8] (see Fig. 2). In the case of a centralized compute system the complete image captured by the cameras is transmitted from the sensors to the aggregator through the MIPI and the full Hand Tracking workload is deployed on the aggregator. On the other hand, on a hierarchical compute system, an optimal repartition of the workload between the on-sensor processor and the aggregator is possible. In the distributed on-sensor compute system, the complete raw image is transmitted from the cameras to the on-sensor processors through the low-energy and high bandwidth \( \muTSV \) interconnects. The region of interest (ROI) is thus computed on sensor, and only this data is transferred from the sensors to the aggregator through the energy-hungry MIPI interfaces. As detailed in [8], the system uses four monochrome cameras. By means of our semi-analytical modeling, we will show that this optimal algorithm repartition across the novel distributed on-sensor compute architecture, as well as the introduction of new emerging technologies, allow for a significant improvement of the overall system power consumption.

2 SEMI-ANALYTICAL SYSTEM MODELING

In order to evaluate the energy efficiency of the distributed on-sensor computing system (Fig 1.(b)), we consider separately the system key modules, such as: cameras, communication links, on sensor processor and the corresponding on-sensor memory hierarchy, as well as aggregator processor and its memory hierarchy. We assume that the total energy per frame of the compute system is simply the addition of the energies of each module, i.e.:

\[
E_{Total} = \sum_{h=0}^{\#(Cameras)} E_{Ca,h} + \sum_{i=0}^{\#(Comm)} E_{Comm,i} + \sum_{j=0}^{\#(Comp)} E_{Comp,j} + \sum_{k=0}^{\#(Mem)} (E_{Read/Write,k} + E_{Lk,k})
\]

(1)

where \( E_{Ca,h} \), \( E_{Comm,i} \), \( E_{Comp,j} \), \( E_{Read/Write,k} \), and \( E_{Lk,k} \) are the total camera, communication, compute, read, write, and leakage energy per frame (as calculated in eq.3, eq.5, eq.7, eq.8 and eq.11 respectively) for each camera (h), communication link (i), compute processor (j) and memory instance (k) present in the system.
Table 1: Values used in simulations for power of the camera in different operating states, based on a custom AR/VR digital-pixel-sensor [10]

| Camera | Operation State | Power (mW) |
|--------|-----------------|------------|
| DPS    | Sensing         | 15         |
|        | Read Out        | 36         |
|        | Idle            | 1.5        |

Table 2: Values used in simulations for the energy and bandwidth of the communication links, based on literature data.

| Communication Link | Energy per Byte (pJ/Byte) | Bandwidth (GB/s) | Ref. |
|--------------------|---------------------------|------------------|------|
| μTSV               | 5                         | 100              | [17] |
| MIPI               | 100                       | 0.5              | [4, 15] |

Figure 3: Memory hierarchy and DNN hardware accelerator used in our simulations. We consider two separate L2 memories, an activation memory (implemented in SRAM), and a read-dominated weight memory (implemented in SRAM or MRAM). We optimized the tiling strategy and dataflow among the different memory levels for our workloads using DORY tiling engine [3].

2.1 Digital Pixel Sensor

We consider the image sensors of the distributed on-sensor compute system being based on a AR/VR custom digital pixel sensor (DPS) technology (detailed elsewhere [10]). The camera analytical model assumes that the sensing and readout energy are proportional to the sensing time, $T_{Sense}$, and the readout time, $T_{Read}$, respectively. The sensing time includes the exposure and the analog to digital converter (ADC) times. We calculate the energy of the camera as follows:

$$ P_{Avg} = \frac{(Cameras)}{\sum_{k=0}^{\#(Cameras)}} E_{Ca,k} + f_{fps} + \frac{(Comm)}{\sum_{j=0}^{\#(Comm)}} E_{Comm,j} + f_{fps} + \frac{(Mem)}{\sum_{j=0}^{\#(Mem)}} (E_{Read/Write,k} + E_{Lk,k}) \times f_{fps} $$

(2)

For each module, we investigate the critical parameters that define its energetic behaviour and we derive simple analytical expressions to capture this behavior (as explained in the following subsections). Once we fix the AR/VR workload, the key parameters of the on-sensor and aggregator processor behavior and optimal dataflow across the multi-level memory hierarchy were extracted by means of the GVSoC tool (a light-weight, event-based instruction set simulator [6]) and DORY [3], respectively.

2.2 Communication Links

Different interfaces are used in the DOSC architecture, as shown in Fig. 1 (b), in particular: μTSV between the image sensor and the on-sensor compute layer, and MIPI between the on-sensor processor and the aggregator. Each interface is characterized by the energy it requires to transmit a Byte of information ($E_{Byte,Comm}$) and by its bandwidth ($BW_{Comm}$). The total energy of the communication link ($E_{Comm}$) is given by the following equation:

$$ E_{Comm} = A_{Size} \times E_{Byte,Comm} $$

(5)

where $A_{Size}$ is the size of the data (in Bytes) transmitted through the interface, which depends on the workload. As shown in Fig. 2, $A_{Size}$ can correspond to the RAW image (transferred from the camera to the on-sensor processing layer), the Region of Interest (ROI) from the input image, or it could be the Neural Network activation map output (transferred from the on-sensor processing unit to the aggregator). The communication time ($T_{Comm}$) is then equal to:

$$ T_{Comm} = \frac{A_{Size}}{BW_{Comm}} $$

(6)

The energy and bandwidth values corresponding to the two interfaces μTSV and MIPI used in our distributed system are given in Table 2 (based on literature data).
weight streaming in the accelerator. As shown in Fig. 3, the simulated memory hierarchy includes two.

The computing architecture used for the on-sensor processing and

133 MAC/Cycle, running on 8-bit precision weights and activations.

an specific memory level) and

\( E \) is the throughput that the system has at layer \( j \) and \( f_{clk} \) is the clock frequency. The processing time is the time that the memory will be in On-state. The rest of the time the memory can be in Retention- or Off-state, depending on the memory type. We can simply calculate the idle time by using the following equation:

\[ T_{idle} = \frac{1}{f_{ps}} - T_{Processing} \]  

Finally, the total memory leakage energy per frame for each memory level will be given by the following equation:

\[ E_{Lk} = T_{Processing} \times L_{kOn} + T_{idle} \times L_{kRet/Off} \]

where \( L_{kOn} \) and \( L_{kRet/Off} \) are the leakage power in On, Retention or Off state respectively, depending on the specific technology.

The energy and power values used in simulations for the elementary MAC operation and the memory read/write access or leakage (i.e. \( E_{MAC} \), \( E_{Byte,Read/Write} \), \( L_{kOn} \) and \( L_{kRet/Off} \)) are extracted from post-synthesis simulations and memory compilers, respectively. In this work, we used 7nm and 16nm logic process nodes and libraries from leading foundries. STT-MRAM values correspond to values from test-vehicles fabricated in 16nm logic technology [7].

On the other hand, the number of operations, the processing efficiency, the memory operations counts and accelerator performance (#MAC, #MAC\(_j\), (MAC/cycle)\(_j\), and #(Read/Write)) are obtained by using the GVSoC/Dory/Nemo toolchain [3, 6] to simulate the deployment of our AR/VR workload on the computing platforms. GVSoC allows us to capture the processing performance depending on the layer configuration and the arithmetic intensity of the NN layer (on each memory level). This is especially important when complex memory hierarchies are considered with different capacities, bandwidths and non-symmetric read-write performances. To deploy the workload across the different memory levels, we modified DORY tiling engine [3] to work with the RBE accelerator.

Using GVSoC we also characterized several representative layers of our workloads that include among others Regular, Depthwise separable, and Pointwise convolutions with varying channel dimension and spatial fields. Using these simulations we obtained the roofline plot for the RBE accelerator shown in Fig 4. The roofline plot allows us to understand the accelerator performance in relation to memory bandwidth constraints. From the plot, we can see that layer performance is almost completely bounded by the weight streaming in the accelerator. The RBE demonstrates close to peak performance on full convolutional benchmarks, with diminishing performance for pointwise kernels, and even further decrease when doing depthwise kernels. We note that the RBE has been designed and optimized for a particular architecture, memory bandwidth, and set of workloads. Because of this, the architecture is most efficient for certain network types as compared to others, as shown by the high throughput of convolution kernels compared to pointwise and depthwise kernels.
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Figure 5: (a) Overall power comparison of centralized and distributed camera compute systems, showing the portion of different components when the AR/VR hand-tracking workload is deployed on the system. The power values are normalized to the case of a centralized system with aggregator in 7nm. Simulations assuming different technology nodes for the aggregator (A) and the on-sensor processors (O) are shown. (b) Power consumption of the on-sensor processor and corresponding memory system, assuming a pure SRAM on-sensor memory hierarchy or a hybrid on-sensor memory hierarchy (SRAM as both L2 activation memory and L1 cache and STT-MRAM as L2 weight memory). Here, we assume that the on-sensor processor is run at 10fps. Power values are normalized to the case of a pure SRAM memory hierarchy. Simulations are based on 16nm technology values.

Now that we have all the blocks to calculate the system energy per frame and the average power, we will use our semi-analytical simulation model to explore the Hand Tracking workload.

3 DISTRIBUTED ON-SENSOR SYSTEM SIMULATIONS FOR HAND-TRACKING

The semi-analytical model was used to compare the energy efficiency of the DOSC system versus a traditional centralized compute system, while deploying a Hand-Tracking (HT) workload for AR/VR experience. As mentioned previously, the HT NN consists in two consecutive Machine Learning algorithms (Fig. 2). The first ML model (DetNet) is used to define the region of interest (ROI), while the second model (KeyNet) is used to detect the joint locations and hand pose. Note that the two ML models, on sensor and in the aggregator, can run at different frames-per-second giving us an additional knob for power optimization. As suggested to improve energy efficiency in [8], the DetNet model is not run at every frame as the same ROI can be used for multiple frames. In our simulations, we assume that the on-sensor compute capability and corresponding memory size to be one fourth of the aggregators. The L2 weight memories were sized to hold the full weights of the models. The weight memories’ operations are mainly read-dominated. On the contrary, the activation memories need to support both read and write operations during the inference. This network has many features which help demonstrate it as a representative workload for our applications. Namely, it is a common and necessary AR/VR application, it has a natural partition point to demonstrate how computation can be split between on-sensor and off-sensor, and it is sufficiently computationally intensive to strain many current systems.

As shown in Fig. 5, our simulation results demonstrate that the cameras and MIPIs dominate the power dissipation of the centralized compute system. On the other hand, when we migrate from a centralized to a distributed system, results show a significant system power reduction (24%, as shown in Fig. 5 (a)). Even when the on-sensor processor technology node is less advanced than the aggregator’s (16nm rather than 7nm), there is still a significant power reduction (16%). The power gain is mainly due to the decreased usage of the energy-hungry serial interface (MIPI) thanks to the on-sensor processing and subsequent feature compression. Additionally, the image sensor power is also reduced. This is because the wider data bandwidth of the μTSV interconnects (between the camera and the on-sensor processor) compared to MIPI allows us to reduce the sensor digital data read-out time and consequently to extend the sensor low-power standby mode. However, it also appears that the total memory energy consumption slightly increases in the distributed computing system due to the duplication of the weight storage memory in each sensor, increasing the total memory size of the system and thus the leakage energy contribution. Finally, Fig. 5 (b) shows that a hybrid on-sensor memory architecture...
(STT-MRAM for weight storage and SRAM for activation) could reduce the overall on-sensor power consumption by 39% thanks to STT-MRAM’s negligible leakage. Moreover, the use of STT-MRAM also allows us to improve the overall on-sensor memory’s form factor, as STT-MRAM features approximately 2x higher memory density than SRAM [7].

4 CONCLUSION

In this paper, we proposed a semi-analytical simulation framework suitable for optimization of AR/VR distributed on-sensor computing architectures. This model allowed us to study simultaneously the impact of the main technological features of the system modules (cameras, interfaces, accelerators, memories) on the overall system power consumption, as well as the impact of the partitioning of the deployed AR/VR CV NNs across the different resources. When an AR/VR Hand Tracking optimized workload is partitioned over the distributed system, the model predicts significant power savings compared to traditional centralized systems, thanks to:

- Improved communication power, as only high-level data representation is transferred from the sensors to the aggregator through the energy hungry MIPI interfaces, while the first level of processing is performed on sensor.
- Reduced camera read-out time (and consequently reduced camera power consumption), thanks to monolithic integration of camera and on-sensor processor through high bandwidth/low energy μTSV interconnects
- Use of STT-MRAM as L2 weight memory on sensor, allowing for 2x higher memory density (thus smaller area) and improved power consumption, thanks to the negligible leakage of STT-MRAM compared to SRAM.

Finally, a significant reduction in the system power remains when the on-sensor processor is implemented in an older technology node than the aggregator’s. However, the older technology node will penalize the on-sensor processor form factor.

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