1 Introduction

Owing to technological advances in high-power semiconductors, high-voltage direct current (HVDC) energy transmission has become an increasingly important part of today's power systems. Besides point-to-point links, several multiterminal DC (MTDC) grids have been built in recent years or are planned shortly [1–4].

Similar to high-voltage alternating current transmission, meshed grids are only feasible if circuit breakers for fault handling are available. In HVAC, this task can be solved by mechanical interrupters (Mls), due to the frequent zero crossings at which current flow can be interrupted. This is not possible in HVDC applications, due to a lack of natural current zero crossings. Additionally, MTDC grids employing modern voltage-sourced converters have much stricter time requirements for fault clearance. Consequently, new topologies have been used to stop current flow in load and fault situations.

A considerable number of different topologies have been proposed for HVDC applications [3–7]. Typically, the topologies consist of three functional paths, the nominal current path (NCP), the current commutation path (CCP) and the energy absorption path (EAP). Two different schemes for interruption have emerged, one utilising a voltage drop in the NCP to commutate the fault current into the CCP, the other by injecting a current from energy storage in the CCP current injection (CI). The most widespread implementation of the first class is the hybrid breaker, employing an ultra-fast disconnecter and a load commutation switch in the NCP. The CCP contains a stack of power semiconductors with turn-off capability, creating a counter voltage to commutate the current to the EAP. While offering low interruption times and low dependency on the interrupted current [8, 9], the costs for the semiconductor stack make this topology expensive.

A less complex, more economical option is current injection breakers. These topologies are typically based on an inductor–capacitor (LC) circuit with a charged capacitor in the CCP. The switch activating the current injection can be realised using an inexpensive triggered spark gap [10]. Current injection topologies have been under investigation from the early stages of HVDC circuit breaker research on [11–13]. Recent prototypes have successfully interrupted peak fault currents of 16 kA without specified voltage (charged capacitor [14]) and 9.2 kA at 160 kV (coupled inductor [15, 16]). The second topology has been installed in the Nan'iao grid in 2017 [17] and successfully tested with intentional faults [18]. The key component determining the performance of current injection topologies is the MI, more specifically, its opening time and interruption performance.

Two important aspects for the design of the injection circuit of a CI topology are the maximum fault current and the interruption capability of the MI. The latter depends on the current and voltage gradient shortly before and after zero crossings, respectively. High injection currents can be reached economically by using a high-frequency LC circuit with very low inductance. However, this results in a higher-current/voltage gradients at zero crossings. For a given injection circuit, the interruption stresses increase with decreasing current, as the injection capacitor remains almost fully charged, resulting in high-current and -voltage gradients. Consequently, inductance and capacitance of the injection circuit need to be large enough to enable the interruption of small (fault) currents.

Current interruption limits and voltage withstand capability are important selection criteria for the used MI. While vacuum interrupters offer higher-current interruption limits, they lack the voltage withstand capability of gas interrupters. Consequently, a series connection of individual units is required for voltages, where a single gas interrupter would suffice. For these reasons, gas [12, 19] and vacuum interrupters [20, 21], as well as series connections of both [13, 22], have been used. Currently, research seems to favour vacuum interrupters [14, 23].

Regarding current interruption, it has been shown that a temporary reduction of current and voltage gradients around the current zero crossing considerably reduces the stresses for the MI. This can enable the use of a scaled down, more economic injection circuit [24]. While this effect will benefit both vacuum and gas interrupters, it could reduce the gap between their current interruption limits. This would make gas interrupters with their higher-voltage withstand capability a promising choice for the MI in current injection topologies.

In this paper, the interruption performance of a model gas interrupter is experimentally investigated for DC-specific stresses typical to current injection topologies. On the basis of the identified limits, two upgrades for the injection circuit are proposed and designed to reduce inductance and capacitance of the injection
circuit without reducing the range of interruptible current. These are based on resistive damping (RD) and resonant polarity reversal (RPR). The effects of the upgrades are verified experimentally. The experimental data is used to verify a simulation model. This model is then used to investigate the feasibility of the proposed upgrades for HVDC systems. As up-to-date data for the interruption limits of vacuum interrupters in current injection topologies is available (in contrast to data for gas interrupters), this is used for the HVDC simulations. However, the results and trends are transferable. For both measurement and simulation, interruption at the first current zero crossing is intended. This leaves a second zero crossing after interruption failure as a backup and does not require dependence on further, optional zero crossings. Additionally, a high number of zero crossings (ten and more have been observed in [12, 25]) can lead to a relevant delay in the interruption process.

2 Experimental setup and its simulation

To investigate the interruption performance of mechanical gas circuit breakers, a scaled down test bench was implemented (compare Fig. 1). Synthetic fault currents were generated by using an LC circuit; the used components resulted in a resonance frequency of 68 Hz (labelled ‘FAU’). The current is interrupted during the first quarter of the oscillation, modelling a rising fault current in a DC system. This circuit is connected to a current injection DC circuit breaker. It consists of a nominal path with a model gas interrupter (S0) and a parallel snubber circuit as well as a current injection path. The model circuit breaker uses pressurised air as interruption medium and is described in more detail in [26].

The injection path features a pre-charged capacitor (CINJ) and an inductor (LINJ) as well as a thyristor switch (S0). Both inductance and capacitance can be adjusted. The EAP has been omitted, as it is not active during the critical phase of interruption in the MI. The charging voltages of the capacitors can be adjusted. Also, a resistor (RND) can be mounted in the injection circuit to influence the damping of the injected current.

The settings, used for the experiments conducted for this paper, are listed in Table 1.

To be able to extrapolate the obtained results, a simulation model has been implemented using PLECS®. This model can be adjusted to the scale of the conducted experiments as well as to conditions for faults in HVDC systems. The circuit breaker is modelled using a series connection of an ideal switch and a resistive element representing the measured static $U$-$I$ characteristic of the model interrupter. In contrast to the energy dissipation, the interruption limits are not included in this black-box model.

Fig. 2 illustrates a typical measurement. At $t = 0$, the current crosses zero and is successfully interrupted. Immediately after the interruption, the remaining charge in the injection capacitor leads to a fast voltage build-up across the MI’s parasitic capacitance. This (negative) voltage is referred to as initial transient interruption voltage (ITIV). After reaching the (negative) peak, the current fault charges the injection capacitor with opposite polarity. This phase between $t \approx 0$ and 2.6 ms corresponds to the ITIV build-up. Owing to the structure of the experimental setup, the voltage across the MI drops to a negative value after reaching peak ITIV ($t \approx 2.6$ ms). While this differs from stresses in an HVDC network, it does not influence the interruption process.

### 2.1 Validation of simulation model

In the first step, the simulation model is compared with the obtained measurement data to verify its accuracy. For this, a series of experiments with different fault current levels was conducted by adjusting the charging voltage of $C_{FAU}$. For each experiment, a corresponding simulation has been conducted.

The difference between simulation and measurement is illustrated in Figs. 3–5. Successful interruptions are marked with circles, while failures to interrupt are marked with crosses. In all plots, the measured values are illustrated on the abscissa and simulated on the ordinate. A dashed line indicates the optimum result, where measured and simulated values coincide. The difference of the simulated from the measured value can thus be read from the vertical distance of the data point to the dashed line.

Fig. 3 illustrates measured current gradients at zero crossing as a function of the simulated values. Both values show close agreement between measurement and simulation. The simulated gradient is consistently higher than the measured one (median: +13.5%). A possible reason for this behaviour is the arc model. It is based on the steady-state $U$-$I$ characteristic of the arc and is extrapolated for very low currents, where the arc becomes unstable. Also, the fluctuating behaviour of the arc leads to a scattering of the results. Concerning successful and non-successful interruption, no considerable difference can be observed.

### Table 1 Component values

| Component | Value     |
|-----------|-----------|
| $C_{FAU}$ | 751 μF    |
| $I_{FAU}$ | 7.3 mH    |
| $C_{INJ}$ | 182 μF    |
| $L_{INJ}$ | 0.8 mH    |
| $C_{MI}$  | 9 nF      |
| $R_{RD}$  | 1.7 Ω     |
| $R_{ND}$  | 300 Ω     |
| $L_{RD}$  | 5.7 Ω     |
Compared to the current gradient before zero crossing, the median: +21.5% for successful interruptions). This is expected, as the arc model does not include the complex physical effects at the changes in conductance during interruption as the MI approaches bypasses it through the residual conductance of the arc. This results in a lower ITIV peak, becoming more pronounced the closer the MI is to its interruption limit. The increasing deviation between measured and simulated for higher interruption stresses, i.e. higher \( U_{\text{ITIV}} \), can be seen in Fig. 4a.

Moreover, in the simulation, current is always interrupted at first zero crossing. In the measurement, it can be observed that the voltage peak is decreased, when the switching action is not successful. This is due to a reignition of the arc and the corresponding voltage drop. Consequently, the simulation can predict values for the ITIV that would have been observed at a successful switching operation (with an ideal switch-off behaviour). These values are referred to as prospective values.

For the RRITIV, simulation and measurement do not agree well. The voltage gradient depends on the injection LC circuit, the capacitance of the MI, as well as the arc resistance, after current zero. In an ideal case, where the arc becomes non-conductive immediately after current zero crossing in the MI, an accurate calculation of the RRITIV is possible when parasitic and stray elements are known. However, if during the interruption, the residual conductance of the arc changes. It is also subject to fluctuations and varies between different circuit breakers [27]. The prospective stresses for the switch are a function of the (constant) circuit elements as well as the ITIV peak. While this varies, depending on the switching case, it can be predicted with good accuracy by the simulation. Consequently, \( U_{\text{ITIV}} \) can be used as a parameter for interruption performance of a given setup with fixed circuit elements.

The RRITIV is illustrated in Fig. 5. This corresponds to the counter voltage build-up by the fault current charging the injection capacitor. As these figures illustrate, it can be simulated very accurately (median of deviation: +1.6% for \( U_{\text{ITIV}} \) and +1.6% for RRITIV). The TIV is mainly determined by fault current and size of injection capacitor and inductor, rather than the dynamic behaviour of the arc model. This explains the lower deviation between simulation and measurement compared with the current gradient and ITIV.

The conducted investigations show that the simulation model can calculate the occurring voltage and current traces, except the RRITIV, with good accuracy.

### 3 Interruption limits in current injection topologies

To determine the interruption limits of the MI, a series of measurements with different fault current levels have been conducted. In the following, the different current and voltage wave shape characteristics are used to investigate the interruption behaviour of the MI.

Fig. 6 illustrates the ITIV properties as a function of the current gradient at zero crossing. Depending on the magnitude of the interrupted current, the gradient at zero crossing varies. For lower currents, it becomes steeper, and a higher amount of charge remains in the injection capacitor. This relation can be seen in the linear correlation between the current gradient and \( U_{\text{ITIV}} \). If the MI fails to interrupt, the recorded voltage peak corresponds to the reignition voltage, which is lower than the expected, prospective TRV in case of a successful interruption.

A similar pattern can be observed in the RRITIV, which, however, is subject to much larger scatter. This is expected as the interruption process for low stresses is much closer to that of an ideal switch. For higher stresses, gradient and peak of ITIV are impacted, which is likely caused by increased charge transfer through the plasma after the current zero crossing. For the conducted measurements, a rather clear transition point between interruption and failure can be identified for both current and voltage gradient. This indicates that the ITIV phase is crucial for the current interruption in HVDC circuit breakers. To determine a relation between current and voltage gradients for critical conditions, further investigations with different LC circuits for injection would be required. However, this is outside the scope of the presented work.

The ITIV that follows the ITIV does not seem to influence the interruption behaviour much (compare Fig. 7). For the highest values of \( U_{\text{ITIV}} \) and rate of rise of TIV (RRITIV), currents were...
successfully interrupted, while for lower values, both interruptions and failures were recorded.

The TIV constitutes the build-up of the system voltage across the HVDC circuit breaker, and thus the MI similar to the TRV in AC systems. However, in contrast to AC systems, the injection capacitor acts as a snubber for the MI, considerably reducing the voltage gradient. Additionally, current injection and, thus, zero crossing in the MI is controlled to occur after the MI reaches a sufficient contact distance. Consequently, a restrike such as in AC systems is not expected.

The observed characteristics allude that current gradient before zero crossing and ITIV are the most important parameters for the interruption. Consequently, upgrades to CCP or NCP that reduce current gradient before and voltage gradient after zero crossing can be expected to improve the interruption behaviour of current injection topologies.

4 Upgraded injection circuits

On the basis of the results of the previous section, auxiliary circuits can be developed to shrink the required current injection circuit without reducing the range of interruptible currents. This could reduce the (financial) footprint of the injection circuits (lower capacitance and inductance) and improve the competitiveness of current injection topologies.

4.1 Resistive damping

To reduce stresses at the current zero crossing in the MI, switchable damping can be employed (compare Fig. 8). This can be either a resistor or a surge arrester (SA). In case of a high fault current, the damping element can be bypassed using a parallel switch. If the full injection current amplitude is not necessary to create a zero crossing, the switch can be left open and the injection is damped. As no turn-off capability is required, the switch can be realised by a triggered spark gap.

If required, the RD upgrade can be realised with multiple damping stages.

4.2 Resonant polarity reversal

In the RPR upgrade (compare Fig. 9), the injection capacitor is split into two (or more) units. The voltage is split accordingly; all capacitors are charged with the same polarity. All, but one of the injection capacitors, have a parallel circuit that can reverse the polarity of its pre-charge voltage. This reduces the total voltage drop across all series-connected injection capacitors by two times the individual capacitor’s pre-charging voltage. The current injection peak is reduced accordingly. The polarity reversal circuit consists of an inductor and a thyristor switch connected in parallel to the respective injection capacitor.

During normal operation, the capacitors are pre-charged. After detecting a fault and signalling the MI to open, a prediction of the current fault level at the moment of current injection has to be made. According to this, the optimum injection current is determined and the respective number of polarity reversal circuits is triggered. The adjusted current is injected after the charge reversal has taken place and the MI contacts have separated sufficiently.

The charging mechanism that is required in current injection topologies can thus be used for this upgrade by adding resistive grading to ensure the correct voltage distribution.

5 Experimental investigation of upgraded circuits

To evaluate the performance of the proposed upgrades, experimental investigations have been carried out. For the
modelling of the RD upgrade, two different resistor values have been used (compare Table 1).

For the RPR upgrade, tests corresponding to one resonant stage with a pre-charging voltage of 25% and one fixed capacitor with a pre-charging voltage of 75% were conducted. To simplify the experimental setup, experiments have been conducted with a regular LC circuit, where the injection capacitor is charged to two different levels (100 and 50% pre-charges).

In contrast to a real application, the fault current of each test is known a priori. This reduces the complexity of the circuit breaker control, as no-fault detection and decision-making algorithms are required. The improved circuits can be realised without switches if they are wired in the correct configuration for the respective interrupted currents, as the focus of this paper is on the improvement of interruption performance.

The results are illustrated as a function of the interrupted current in Figs. 10–14. The measured results (circles and crosses) are in line with the simulation (lines), as discussed in Section 2.1. As expected, the tested model interrupter successfully interrupts the current (with and without upgrade stages) up to ∼3 A μs⁻¹. For currents below 1 kA, the reference configuration without upgrades exceeds the interruption limit. At this point, both upgrade circuits can considerably reduce the current gradient for lower currents and successfully increase the range of interruptible currents.

Owing to the described influence of the dynamic and fluctuating behaviour of the arc shortly before the interruption, the measured RRITIV values also show a visible scattering. However, the expected reduction of voltage gradient can indirectly be seen in the reduction of $U_{ITIV}$.

The simulation shows similarly accurate values for both RD and RPR upgrades.

Rate of the rise and peak value for the TIV for simulation and successful current interruption of the experimental setup are illustrated in Figs. 13 and 14. It can be seen that the impact of the upgrade circuits is minor. While this is not expected to influence the interruption behaviour of the MI, it underlines the predictive quality of the simulation.

### 6 Scaling of improved circuits

On the basis of the previous results, simulations are conducted to evaluate the application potential of the presented upgrades for HVDC. For this, a synthetic reference fault case has been implemented (compare Fig. 15). This consists of an ideal voltage source, a system inductance and a load as well as a fault resistance, between which can be switched. The values for the individual components are summarised in Table 2.

For the MI, a stack of vacuum interrupters is considered. The maximum interruption performance is approximated by $e = \frac{d}{dt} i/d\cdot\frac{d}{dt}U$ [28, 29].

An unmodified current injection reference topology (REF) serves as a benchmark. A second injection circuit (reference topology with high frequency injection circuit: REFhf), using an injection circuit with a higher resonance frequency (i.e. smaller
6.1 Resistive damping

For this test circuit, an RD upgrade with two stages was simulated (compare Fig. 16). The resistances in both ($R_{RD1}$ and $R_{RD2}$) can be inserted or short circuited independently, allowing four configurations.

For low fault currents, the effect of damping with resistors becomes small, as considerably less energy is dissipated. This can be compensated if SAs are used instead of resistors. In this paper, a two-stage damping upgrade using SAs is simulated for comparison [SA damping (SAD)].

Fig. 17 illustrates the energy dissipation of the damping elements as a function of interrupting current. For the RD upgrade, the energy dissipation reduces considerably with the interrupted current. For currents between 11 and 8 kA, RD 1 is used. Between 8 and 5 kA, the larger resistor RD 2 is used. If the current drops below 5 kA, both RD 1 and RD 2 are activated. The worst case for each resistor is just below the threshold, where it is first used.

Owing to the selection of the resistance values, $R_{RD2}$ has a considerably higher maximum energy dissipation than its counterpart. For the SAD upgrade, the dissipated energy decreases considerably less with the interrupted current, which is expected due to the use of SAs. The load is more evenly distributed and the dissipation is in total lower than for the RD upgrade.

6.2 Resonant polarity reversal

The RPR upgrade is simulated with two stages, as illustrated in Fig. 18. Results can be seen in Fig. 19. The stages are split and precharged such that the voltage is distributed (0.81/0.095/0.095).

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6.2 Resonant polarity reversal

The RPR upgrade is simulated with two stages, as illustrated in Fig. 18. Results can be seen in Fig. 19. The stages are split and precharged such that the voltage is distributed (0.81/0.095/0.095). Similar to the REF topology, the maximum voltage across the capacitors occurs with the maximum fault current.
The overvoltage across the two RPR stages can be effectively limited by protective SAs. While these do not have to absorb large energies, they can reduce the voltage withstand requirements considerably.

6.3 Comparison

The interruption stresses for the MI as a key indicator for the successful operation of the circuit breaker have been investigated over a broad range of fault currents. The results are illustrated in Fig. 20.

The interruption requirements are met for REF over the complete range of simulated fault currents. However, this topology employs rather large components and has a comparably long current commutation time ($t_{cc}$) between trip order and peak TIV, especially for low fault currents.

REFhf uses a scaled down injection circuit. Interruption requirements for the MI are not met for currents below $\sim$11 kA. From this point on, the first stage of the respective upgrades is used. The boundary for the activation of the second stage is $\sim$9 kA for the RD upgrade and about 7.5 kA for the SAD and RPR upgrades. Concerning interruption stresses for the MI, all performances are similar, except for low currents (<5 kA). Here, the RD upgrade starts to be less efficient in reducing current and voltage gradients.

Regarding $t_{cc}$, all upgrades benefit from the reduced injection circuit. The voltage rise (TIV) increases, as the injection capacitance is considerably smaller than in REF.

Component values and peak stresses are summarised in Tables 3 and 4. An illustration of the cost contribution of the individual components as well as the current commutation time (for the smallest simulated fault current of 2.1 kA) can be found in Fig. 20.
Table 4 Maximum stresses for used components

| Topology | Component | Maximum value | Reference |
|----------|-----------|---------------|-----------|
| REFh     | $U_{CINJREFh}$ | 680 kV | 2.13 - $U_o$ |
| REF      | $U_{CINJREF}$  | 688 kV  | 2.15 - $U_o$ |
|          | $U_{LINREF}$   | 320 kV  | 1.0 - $U_o$ |
|          | $E_{APREFh}$   | —      | —         |
|          | $E_{APREF}$    | 39.3 MJ | —         |
| RD       | $E_{RD,1}$    | 127 kJ  | 3.2‰ $E_{APREF}$ |
|          | $E_{RD,2}$    | 80 kJ   | 2.0‰ $E_{APREF}$ |
| SAD      | $E_{SA,1}$    | 65 kJ   | 1.6‰ $E_{APREF}$ |
|          | $E_{SA,2}$    | 83 kJ   | 2.1‰ $E_{APREF}$ |
| RPR      | $U_{C, RPR}$  | 551 kV  | 80% $U_{CINJREF}$ |
|          | $U_{C, RPR}$  | 46 kV   | 7% $U_{CINJREF}$ |
|          | $E_{SA,1}$    | 45 kJ   | 1.1‰ $E_{APREF}$ |
|          | $U_{C, RPR}$  | 46 kV   | 7% $U_{CINJREF}$ |
|          | $E_{SA,2}$    | 39 kJ   | 1.0‰ $E_{APREF}$ |

However, after the current interruption, the capacitor stack is recharged by the fault current during the TIV build-up. This can lead to a considerable overvoltage across the RPR stages (capacitor and thyristor), due to their small capacitance. In the presented setup, this can be as high as four times the pre-charging voltage. To avoid such a drastic increase in voltage withstand requirements, the stages should be protected with SAs. In this configuration, the cost for the capacitors is only 5% of what is expected for the REFh configuration. Besides, two thyristor stacks each rated ~14% of the system voltage (with ideal clamping behaviour each 9%) are necessary. This will probably not exceed the savings due to the smaller injection inductor and capacitor, and thus lead to an overall economic advantage.

Summarising, the SAD upgrade appears to have the most favourable characteristics. It offers an economic advantage over the REF topology while offering similar interruption performance and reduced current commutation time.

7 Conclusion

Compared to HVAC, circuit breakers for multiterminal HVDC networks require significantly more complex structures and will contribute a considerably higher share of the overall system costs. Consequently, an optimisation to reduce component requirements and size is of great importance.

The key component of modern HVDC circuit breakers is the mechanical switch. For current injection topologies, its limitations in speed and interruption capability define the minimum required capacitance and inductance in the injection circuit.

For this contribution, experimental and simulation studies have been conducted to investigate the interruption behaviour of MIs and develop auxiliary circuitry to reduce stresses during switching.

The experimental results support the observation that the current gradient before and ITIV gradient after the current zero crossing are the main factors to determine the success of the interruption. In contrast to HVAC, the build-up of system voltage (TIV) in HVDC systems did not show an influence, but rather the current injection topology specific ITIV.

On the basis of these results, two upgrade circuits are proposed to improve current and voltage wave shapes around the current zero crossing in the MI. This is realised either by adjustable RD of the injection current (RD and SAD) or by adjusting the total injection voltage using RPR.

On the basis of an experimentally verified model, the feasibilities of these upgrades have been investigated using simulation. It is possible to reduce the injection LC circuit considerably without reducing the range of interruptible current with both upgrades. Also, due to the reduced total capacitance of the injection circuits, the upgrades lead to a reduction of the internal current commutation time. However, they differ considerably in the expected cost of additional components.

The SAD upgrade is expected to be almost as economical as the scaled down high-frequency injection circuit since the additional components are SAs with low-energy rating and triggered vacuum gaps. The RPR upgrade also requires considerably less capacitance than the reference injection circuit. However, it requires additional semiconductors making it more expensive than the SAD upgrade.

The levels at which different stages of the updates are activated depending on the peak fault current. Consequently, a detection system that predicts the peak fault current during the opening of the MI and sends the respective switching commands is required.

Concluding, the presented study shows that current injection topologies provide further optimisation potential. Upgrading injection circuits provides a measure to further improve their economic advantage over other HVDC circuit breaker topologies.

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