Using Graph Neural Networks to model the performance of Deep Neural Networks

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Abstract—The unprecedented proliferation of machine learning-based software brings an ever-increasing need to optimize the implementation of such applications. State-of-the-art compilers for neural networks, such as Halide or TVM, incorporate a machine learning-based performance model to search the space of valid implementations of a given deep learning algorithm. For a given application, the model predicts the value of performance metrics such as the run time without executing the application on hardware. Existing performance models employ feed-forward networks, recurrent networks, or decision tree ensembles to estimate the performance of different implementations of a neural network. Graphs present a natural and intuitive way to model deep-learning networks where each node represents a computational stage or operation. Incorporating the inherent graph structure of these workloads in the performance model can enable a better representation and learning of inter-stage interactions. The accuracy of the performance model has direct implications on the efficiency of the search strategy, making it a crucial component of this class of deep-learning compilers. In this work, we develop a novel performance model that adopts a graph representation. In our model, each stage of computation represents a node characterized by features that capture the operations performed by the stage. The interaction between nodes is achieved using graph convolutions. Experimental evaluation shows a 7.75x and 12x reduction in prediction error compared to the Halide and TVM models, respectively.

Index Terms—Deep Learning, Neural Networks, Code Optimization, Performance Modeling, Graph Neural Networks.

I. INTRODUCTION

Compilation frameworks like Halide [1] and TVM [2] use a high-level domain-specific language to express tensor computations. Deep learning programs are written in this high-level language, which gets translated into low-level optimized code for a particular hardware platform. This approach separates the algorithmic computation, also known as the pipeline, from the way it is performed, called the schedule - a technique first proposed in Halide. Users can specify the computations to realize their machine learning model, and the compiler generates an efficient low-level implementation for the model. Depending on the target hardware architecture, the compiler has to determine an appropriate set of optimizations for the efficient execution of the application. In contrast, frameworks like Tensorflow [3] and PyTorch [4] rely on a library of optimized low-level implementations of common tensor operations, such as matrix multiplication, pooling, etc. These implementations are hardware-specific and are expert-written. Neural networks are represented as a computational graph, and the compilation process translates each operation into its optimized low-level counterpart. This approach has two drawbacks. First, it requires a lot of human effort to create and maintain these libraries. The implementations have to be rewritten and revised for new hardware and iterations, respectively. Secondly, code optimization happens at the operator level-granularity and often overlooks critical graph-level optimizations.

For a given deep-learning computation (or any computation for that matter), the quality of a schedule (how the computation is performed) depends on how well it can utilize the available hardware resources. For example, a convolution operation on a CPU will be more efficient if it can exploit the underlying cache hierarchy and locality using tiling and reordering of loads/stores. The computation will also take less time if the schedule can take advantage of the data parallelism provided by the hardware via SIMD or vector instructions. While Halide and TVM, in principle, have the capability to explore such optimization avenues, they have their own set of challenges. For a given neural network computation, a compiler has to explore an enormous number of schedules in a space parameterized by per-stage choices like loop unrolling, vectorization, tiling, etc. Schedule search is a time consuming combinatorial problem since any practical neural network represents a vast schedule space. To make the search process more efficient, analytical models that guide the search towards efficient schedules have been proposed.

The main idea behind a model like the one we have developed is to estimate the performance of a given implementation without actually running it on hardware. Figure [1] shows the typical construction methodology and working of a deep learning-based performance model like ours. The model takes as input features extracted from a deep-learning program. These features are designed to convey information about the structure of the network and the computation being performed. How these features are encoded depends on the model itself. The performance model uses these features and generates a performance metric, the run time in our case. Models are trained/tuned using the actual performance metrics obtained by benchmarking the input programs on the target hardware. Performance models offer a faster alternative to auto-tuning approaches when exploring schedules. This paper is another step towards improving the accuracy of the statistical performance models by utilizing the inherent graph...
Fig. 1: Performance model construction: Features obtained from a deep learning program are provided as inputs to the model. The output is the estimated run time of the program. The actual run-time of the application is used to train and tune the model.

structure of deep-learning networks. Specifically, we employ graph neural networks to estimate the performance of deep-learning pipelines in the Halide framework.

Previous models developed for the Halide framework used feed-forward [5] and recurrent neural network [6] architectures. TVM [7] relies on a decision tree based model. In this work, we introduce a novel performance model capable of utilizing the graph structure of deep-learning networks to capture inter-stage relationships. Incorporating neighborhood interactions using graphs can improve the quality of the predictions. Our approach represents the pipeline as a directed acyclic graph (DAG) and aggregates information about the neighboring stages using graph convolutions [8]. Experimental evaluation of the proposed design demonstrates a 7.75x and 12x reduction in prediction error compared to the Halide and TVM models, respectively.

This paper makes the following contributions.

- **A novel Graph Convolutional Network-based performance model.** We propose a novel machine learning-based model to predict the execution time of deep learning pipelines. Our model can capture interactions between neighboring nodes to generate richer representations that improve the accuracy of the predictions.

- **Implementation and Halide Interface.** We implement the proposed model in PyTorch. The model takes as input features extracted from Halide pipelines and schedules and outputs the run time. To train the model, we generate a dataset comprising over 1.6 million schedules from 10,000 pipelines. We focus on CPU-based hardware platforms and benchmark the schedules on Intel Xeon CPUs to obtain the run times for training.

- **Improved Accuracy.** An experimental evaluation of our approach shows the benefits of performance modeling using Graph Convolutional Networks (GCNs). On a random sampling of schedules, our model reduces the prediction error by a significant margin compared to the current Halide (7.75x) and TVM (12x) models. Moreover, our model is around 75% accurate when performing a pairwise ranking of schedules derived from real-world deep neural networks.

The rest of the paper is organized as follows. Section II provides a background of the basic constructs of algorithm-schedule separation in Halide. We also provide a brief overview of the Halide [5] and TVM [2] performance models in this section. Section III describes the proposed model architecture in detail. Section IV presents the evaluation methodology and results. We discuss related work in Section V future work in Section VI and conclude in Section VII.

## II. Background

### A. Scheduling in Halide

Neural network computations are usually modeled in terms of operations involving tensors. This computational model gained popularity with the advent of deep learning libraries and engines like Tensorflow, PyTorch, etc. However, as discussed in the previous section, these frameworks rely on low-level optimized implementations of commonly used tensor operators when translating the computational graph of the network, and this may result in missed optimization opportunities across operators. The primary philosophy behind Halide is to separate the algorithm (computation) from the schedule (how to carry out the computation). For a deep-learning pipeline composed of one or more tensor operations, the Halide compiler can generate code for these operations such that it optimizes the overall throughput of the pipeline. Halide exposes programmers to a design space mostly hidden in traditional deep-learning frameworks.

In this section, we provide a brief overview of the Halide framework and its scheduling primitives. As an example, we use Halide to implement a linear layer. Linear layers are common in deep learning and represent a fully connected neuron layer. The inputs to the layer are multiplied by a weight matrix followed by the addition of bias terms. In batched computation, multiple input samples are processed concurrently. The following equation expresses the linear transformation of an input batch represented as a two dimensional matrix $X$, where each row represents an input. $W$ and $B$ are the weight and bias matrices, respectively.

$$ Y = XW + B $$

The following code snippet shows a Halide implementation of a linear layer. Please note that while this is not the best way to implement this operation, it is sufficient for our illustration. When doing batched computations, the input and output matrices have the dimensions (batch_size, input_size) and (batch_size, output_size), respectively. In this example, we use a batch of 64, an input size of 1,024, and an output comprising 16 floats. ImageParam is used to define a multidimensional input to the pipeline. The input, weight, and bias have two dimensions and store floating-point numbers. We split the computation across two functions or stages, matrix_mul carries out the multiplication of the input with the weights, and add_bias, as the name suggests, sums the product with the bias terms. The variables $x$ and $y$ are used as indices to specify the computation. The multiplication...
stage has two update definitions, the first one (line 15) zeros the buffer, and the second update (line 16) computes the product. The two matrices are multiplied using a reduction domain (RDom) which denotes an implicit loop. For this two-stage pipeline, the add_bias stage consumes the result of the matrix_mul stage. The compute_root forces the completion of the matrix_mul stage before proceeding to the add_bias stage. Calling the realize operation on the final stage compiles the entire pipeline.

```
const int batch = 64, input = 1024, output = 16;
ImageParam input(type_of<float>(), 2) / / batch * inputs
ImageParam wts(type_of<float>(), 2) / / input * output
ImageParam bias(type_of<float>(), 2) / / batch * output
Var x(“x”), y(“y”);
Func matrix_mul(“matrix_mul”);
Func add_bias(“add_bias”);
RDom r(0, input);
RVar k = r[0];
matrix_mul(x, y) = 0.0f;
matrix_mul(x, y) += input(x, k) * wts(k, y);
add_bias(x, y) = matrix_mul(x, y) + bias(x, y);
Buffer<float> output(output, batch);
matrix_mul.compute_root();
add_bias.realize(output);
```

The rest of the section describes some typical scheduling options available in Halide.

1) **Inline Evaluation:** This option, invoked using compute_at, inlines the computations performed in the producer into the loop-nest of the consumer. The producer function is computed as needed by the consumer function, which avoids the need for a temporary buffer to store the intermediate result. Inlining the evaluation also improves the locality of reference as generated values are immediately consumed. A potential downside of inlining is that it may lead to redundant computations as intermediate results are not stored in memory. The following code inlines the computations of the product stage into the inner loop of the bias stage.

```
matrix_mul.compute_at(add_bias, x);
```

2) **Reorder:** Loop reordering changes the hierarchy of the loop-nest. In certain situations, reordering can take advantage of data storage pattern to improve locality. The sequence in which the loop iteration variables provided to reorder establishes the ordering beginning with the inner-most loop and ending at the outer-most loop. For example, the following line reorders the loop-nest of the add_bias stage.

```
add_bias reorder(y, x);
```

3) **Split:** The split functionality breaks a loop into a pair of nested loops. The split factor is the trip count of the inner loop, and the outer loop extent is the original extent divided by the split factor. Using a combination of splitting and reordering can achieve tiled execution or blocking. The amount of cache memory is limited, and arrays seldom fit entirely in the cache. In such situations, tiling partitions the iteration space into small chunks (working set) such that they fit in the cache, thus improving locality. The following code splits the x and y

```
add_bias.split(x, x_outer, x_inner, 4);
add_bias.vectorize(x_outer).parallel(y);
```

4) **Vectorize and Parallel:** The vectorize option computes multiple iterations of a loop simultaneously by utilizing the available SIMD hardware. To parallelize a computation across CPU cores, we use the parallel directive. For example, one way to parallelize and vectorize the add_bias stage would be to split the inner loop by a factor of 4 and vectorize the x_inner loop and parallelize the y loop. The following code shows the relevant operations to implement this schedule.

```
Var x_outer, x_inner, y_outer, y_inner;
int split_factor = 8;
matrix_mul.update(0).split(x, x_outer, x_inner, split_factor);
matrix_mul.update(0).split(y, y_outer, y_inner, split_factor);
matrix_mul.update(0).reorder(x_inner, y_inner, x_outer, y_outer);
```

5) **Other options:** In addition to the options discussed in this section, Halide has several other scheduling knobs like loop-unrolling, loop fusions, storing intermediate results in a buffer, etc. We refer the reader to the Halide documentation for further details.

It should be evident from this discussion that Halide exposes the programmer to a rich and complex schedule space. For a single stage, the number of available scheduling options increases combinatorially with the number of tensor inputs, dimensions (rank), and size of each dimension. As a result of this large search space, auto-tuning approaches that depend on benchmarking on actual hardware for feedback are simply too slow to be practical. This led both Halide and TVM to leverage performance models to assess the fitness of candidate solutions.

**B. Existing Performance Models**

As already mentioned, the Halide and TVM compilers search the schedule space and find an efficient implementation of a given program. Figure 2 depicts a basic search framework. The search technique generates a pool of candidate schedules and uses the performance model to select the most promising candidates for further exploration. In Halide, a computation comprises multiple stages or functions, and the search has to make a scheduling decision for each stage. In the Halide autoscheduler, the stage-wise scheduling decisions are made.
Algorithm specific feat.  
Schedule dependent feat.  
Embedding  
Embedding  
Stacked Embedding  
Coefficients

Fig. 3: Halide auto-scheduler model: The algorithm and schedule features are passed through fully connected layers to generate embeddings which are then combined and passed through a fully connected layer to get the final coefficients. The dot product of these coefficients with the 27 hand-crafted terms is the final run time [5].

using beam search, which uses feedback from the performance model to maintain a pool of candidate schedules. To add an unscheduled stage, the search graph expands by enumerating all possible schedules for that stage. The model is then used to rank the resulting candidates and prune the graph preserving only the top-k candidates.

The model is constructed using fully connected layers and is trained to predict the run time conditioned on features extracted from the application. The featurization process results in two types of features. Algorithm-specific features are invariant to the schedule and comprise a histogram of operations performed. These features characterize the computation and not the implementation. Schedule-dependent features, on the other hand, capture the impact of the scheduling choices. These include metrics to capture the memory footprint, parallelization, vectorization, etc. The performance model computes low-dimensional embeddings of the algorithm-specific and schedule-dependent features and stacks them to generate the final output. Instead of directly predicting the run time, the output learns the coefficients of 27 hand-crafted terms. These terms are derived from schedule-specific features. The network output assigns appropriate weights to each of the terms, and the run time is the dot product of the terms and coefficients.

Figure 3 is a high-level representation of the network used to construct the model. The model estimates the run time of each stage, and the summation of the run times of all scheduled stages provides the total run time or the performance of the pipeline [5].

The TVM auto-scheduler employs a gradient boosted tree (GBT) model based on XGBoost [7]. The inputs to the model are features that encode information about the loop nest. These context features include information about the loop structure like the loop extents, memory footprint, and annotations for vectorization, unrolling, etc. To make the context features more generalizable, the authors build context relation features which model the relationship between different features in the loop nest that affect the performance. TVM also has a second model built using TreeGRUs. Instead of directly learning an embedding for each identifier in the loop nest AST, the model uses embeddings derived from the GBT context vectors. In practice, both models exhibit similar performance. However, the GBT model is faster than the TreeGRU model [2].

C. Feature Engineering

The proposed work follows a methodology similar to the previous deep-learning based Halide models and extracts two categories of features from Halide programs (see [5], [6]). The first category of features, called pipeline or schedule invariant features, intends to characterize the nature of the computation. The second category, called schedule dependent features, captures how the computations are performed.

1) Schedule-invariant Features: Schedule-invariant features describe the computations and are independent of how they are carried out. As the name suggests, these features remain consistent across different schedules of the same pipeline. We compute a histogram of different types of operations performed to produce the result. These include floating-point arithmetic operations on tensors as well as integer arithmetic used for tensor indexing. We also capture boolean/logical operations like and, or, xor, etc. Memory access latencies have a significant impact on execution times. We also record access patterns like striding behavior, transposed access, and broadcasts.

2) Schedule-dependent Features: This set of features capture the scheduling choices made to execute a pipeline. Modern CPUs exhibit considerable variation in resources like the number of ALU units, cache sizes and hierarchy, memory bandwidth, number of cores, etc. An optimal schedule organizes the computation such that all available resources are utilized to the maximum extent possible. The pipeline is scheduled stage-by-stage, beginning from the last/output stage and going up the DAG to the source/input stage(s). Information about scheduling decisions for every stage is encoded using the following data points. Loop-splitting transforms a loop into a nested configuration with one outer and one inner loop. This scheduling option has implications on the locality of reference and determines the efficiency of cache utilization. The impact of splitting a loop is captured by recording the new loop ranges/ extents. The memory footprint of each loop is quantified by counting the number of unique cache lines accessed, histogram of accessed bytes, and memory reuse distance. A lot of current CPUs exploit data-level parallelism via SIMD/vector instructions. We count the number of vectorized and scalar floating-point and integer arithmetic operations. The CPU core utilization is measured as a ratio of parallel tasks and the total cores. The impact of inlining a function call is measured in terms of the additional computation performed. Schedule-dependent features also incorporate an estimate of other overheads that impact performance. These include the amount of allocations and deallocations on the heap, context switches, and page faults.

Compound Features: The Halide-based model introduced in [6] used a subset of the schedule-dependent features to capture products and ratios, which are difficult for a network
to learn without significantly bloating network capacity. The authors augmented the schedule-dependent features with these compound features derived from two or more basic features via comprehensive evaluation. These include features that quantify the impact of memory allocations, page faults, arithmetic intensity, to name a few. We also incorporate these features in our model.

III. ARCHITECTURE

This section describes the design and implementation of our model. To develop our model, we follow the standard supervised learning approach and use a corpus of randomly generated Halide pipelines and schedules for training. We begin this section by detailing the dataset generation methodology. We then explain the construction of the performance model and its building blocks.

A. Dataset Generation

The data generation framework depicted in figure 4 has four components. First, we use a random model generator to build models conforming to the ONNX [10] standard. The ONNX models are then converted to Halide pipelines. Next, we obtain multiple schedules for each randomly generated model, and finally, we benchmark the schedules to get the run time. The rest of this section describes the components in detail.

Algorithm 1 shows the data generation process. The random model generator constructs models by using operators commonly found in deep learning. These include operations like Gemm, Conv, Maxpool, Average Pool, Relu, Sigmoid, Softmax, etc. We have identified about 50 such operators. We now describe the procedure to generate random ONNX models. ONNX, short for Open Neural Network Exchange, is an open standard to specify neural network models that can be exported across a wide variety of environments and platforms [10]. After choosing the number of inputs to the model (line 3), we generate the input tensors (line 4). The tensor ranks and dimensions are sampled from a specified range. The set of inputs comprise the input stage of the model. The next step is to determine the number of layers in the model (line 5). We build each network stage by stage, with the outputs of the previous stage acting as inputs to the current one. (lines 8-10). Each stage comprises several computational nodes, and their number is randomly sampled from a range (line 23). We support different kinds of nodes depending on the number of inputs (node.type) and type of operation (node.op). When building a random node, we sample from predefined distributions to determine the type and the operation (lines 31, 35, 38). After building all the nodes, we copy the unused tensors (tensors that weren’t compatible inputs to any node) from the input stage to the next stage (line 27). To ensure the collection of only realistic networks, we add two filters that discard most graphs with more than one output (output_thresh = 1) and graphs with a depth of less than 5 (depth_thresh = 5). A large number of well-known deep neural networks make use of operators like convolutions, Relu activations, etc. (favored_ops). To obtain a more representative distribution of models, we filter a large number of networks lacking such operators (lines 15-16). We return the model only if it passes all the filters (lines 17-20). The random ONNX pipelines are then translated into Halide pipelines. At this stage, we extract the schedule-invariant features.

The next step is to generate schedules for the pipelines for which we utilize the Halide auto-scheduler [5]. By injecting the performance model with random noise, we can derive multiple schedules for each pipeline. For every schedule, we record the schedule-dependent features. Finally, for benchmarking, each schedule is run 10 times on the target hardware to obtain the run time. Our dataset comprises over 1.6 million schedules from around 10,000 pipelines. We use 10% of the dataset for evaluation and the rest for training. The schedules were benchmarked on 18 core Intel Xeon CPUs (D-2191) running at 1.60 GHz and having a memory of 48GB.

B. Model

Graphs are an effective way to model a collection of objects and their relationships. Machine learning formulations for
ONNX Model Generator

```plaintext
function BUILD_RANDOM_ONNX_MODEL
    model ← initialize model
    num_inputs ← determine no. of inputs
    input_stage ← generate_inputs(num_inputs, ...)
    num_stages ← number of stages in the pipeline

    > Add stages one by one
    while not done generating num_stages do
        new_stage ← build_new_stage(input_stage, ...)
        add new_stage to model
        input_stage ← new_stage

        valid_outputs ← filter_outputs(model.outputs, output_thresh)
        valid_depth ← filter_depth(model, depth_thresh)

        favored_ops = {conv, relu, ...}
        model_OK ← filter_model(model, favored_ops)

        if valid_outputs and valid_depth and model_OK then
            return model
        else
            return invalid_model
    end

    function BUILD_NEW_STAGE(input_stage, ...)
        new_stage ← list containing nodes in this stage
        width ← number of nodes in this stage

        > Add nodes to the stage
        while not done generating width nodes do
            new_node ← build_random_node(input_stage, ...)
            add new_node to new_stage

        add unused tensors from input_stage to new_stage
        return new_stage

    function BUILD_RANDOM_NODE(input_stage, ...)
        node ← initialize node
        node.type ← sample_categorical(unary, binary, ...)

        if node.type is unary then
            node.op ← sample_categorical(pad, pool, softmax, ...)
        else if node.type is binary then
            node.op ← sample_categorical(conv, gemm, batch_norm, ...)
        end
        return node
```

Each vertex $i$ in $V$ is represented by a feature vector $e_i$. In our case, each node is a Halide stage, and the initial embeddings ($e_i^0$) are derived as shown in figure 5. To generate the initial embeddings, we normalize the schedule-invariant and dependent features over the entire training set and embed the features to a low dimensional space for more efficient training.

$$
e_i^0 = f_{init}(stage_{sched}^{inv}, stage_{sched}^{dep})$$

The graph connectivity and structure are encoded by the adjacency matrix $A$. We do not differentiate between edge types and do not have a feature vector for the edges. The network is built using two standard computational modules.

**Aggregation-Update:** This operation involves the nodes propagating their information to the neighboring nodes. Each node aggregates the information it receives from its neighborhood and uses it to update its embeddings. Graph networks typically have multiple aggregation-update steps. At the $k^{th}$ round of aggregation-update, to compute the next set of embeddings for some vertex $i$, the function $f_{aggregate}$ takes
as input the current embeddings of \(i\)'s neighbors \((N(i, k))\) and consolidates them to generate the aggregated result \(m_i^k\):

\[
m_i^k = f_{\text{aggregate}}(N(i, k))
\]

The function \(f_{\text{update}}\), using this result and current embeddings of node \(i\), generates the new embedding.

\[
e_i^{k+1} = f_{\text{update}}(e_i^k, m_i^k)
\]

The aggregate operation is implemented by summing the embeddings of the neighboring nodes and passing the sum through a learnable weight matrix. For the update, we multiply the current embeddings of the node with another learnable matrix and add it to the output from the aggregate operation. The final result is passed through an element-wise non-linearity. Along with the weight matrix, we also incorporate learnable biases but exclude them here for simplicity. The reasoning behind the update operation is that the new node representations will depend on the representations of the neighboring nodes as well as their own current states. The equation below shows the combined aggregate-update operation.

\[
e_i^{k+1} = \sigma(W_{\text{self}}^k e_i^k + W_{\text{agg}}^k \sum N(i, k))
\]

We can transform the above equation, which captures these operations for individual nodes, to one representing the same operations on the graph level. \(E\) denotes the embedding matrix of all nodes at step \(k\), with each row corresponding to a graph node. Multiplication of the adjacency matrix with \(E\) results in the summing of the neighbors for every node, and multiplying the result with the weight matrix achieves the aggregation operation. Similarly, we can multiply \(E\) with \(W_{\text{self}}^k\) to compute the updates for all nodes.

\[
E^{k+1} = \sigma(W_{\text{self}}^k E^k + A E^k W_{\text{agg}}^k)
\]

Finally, we simplify the above equation along the lines of the graph convolutions proposed by Kipf and Welling [8]. In their technique, the two different weight matrices are replaced by a single learnable matrix. The adjacency matrix is modified to incorporate self-loops by adding it to an identity matrix. The resulting matrix is then row-normalized (each row sums to 1), and multiplication with the transformed adjacency matrix \(A'\) results in averaging the representation of the neighborhood nodes. Each aggregation-update step is referred to as a convolution layer, similar in spirit to traditional convolutional networks, with all nodes sharing the same set of weights.

\[
E_i^{k+1} = \sigma(A' E_i^k W^k)
\]

**Pooling-Readout:** After passing the initial node representations through one or more convolutional layers, we use the initial, intermediate, and final embeddings to learn representations for the entire graph. The pooling operation involves summing the node representations. Following a technique similar to [12], we preserve the initial, intermediate node representations along with the final representations. The sum-pool operation involves summing the node representations at every convolution step, including the initial embeddings. In the following equation, \(F(k)\) is the sum of all node embeddings after the \(k\)th convolution.

\[
F(k) = \sum_{i \in V} e_i^k
\]

The pooling operation produces a consolidated feature vector \(F\) whose width is equal to the width of node embeddings multiplied by the number of convolutional layers. To generate the final readout or output \((\hat{y})\), the runtime in our case, we pass the feature vector through a learnable weight matrix \((W_{\text{out}})\).

\[
\hat{y} = W_{\text{out}} F
\]
C. Implementation

The initial node representations are generated by normalizing the schedule invariant and dependent features and embedding them to a lower-dimensional space (figure 5). Figure 6 shows a single convolution layer. The current embeddings of every node are passed through a linear layer, and multiplication of the output with a normalized adjacency matrix with self-loop achieves neighborhood aggregation and update. The addition of a batch-normalization layer followed by a ReLU activation to generate the new embeddings results in better performance in practice. Our performance model, as seen in figure 7, comprises two convolutional layers. We arrived at this configuration after a parametric sweep of convolutional layers ranging from 0 to 8. Using the technique proposed in [12], we preserve the initial and intermediate embeddings for graph-level readout. To generate a representation for the entire pipeline, we sum across stages after every convolution and use a graph-level readout. Using the technique proposed in this configuration after a parametric sweep of convolutional layers ranging from 0 to 8.

We combine the three terms to compute the final loss, as shown in the equation below.

\[ l_{ps} = \xi, \alpha, \beta \]

Loss Function: We made the following choices to design our loss function.

- **Property 1.** We base our loss on the absolute ratio of the predicted and the measured run times. To account for noise in the measurements, every schedule \( s \) of a pipeline \( p \) is benchmarked \( N \) times on the hardware, and the term \( y_{ps} \) represents the mean of the measurements. \( N \) is set to 10 for the experiments in this paper. The following equation then determines the absolute relative error, where \( \hat{y}_{ps} \) is the output of the model.

\[ \xi = \frac{N \cdot \hat{y}_{ps}}{\sum_{i=1}^{N} y_{ps,i}} \]

- **Property 2.** We also want the model to differentiate between good and bad schedules. Making an accurate prediction on an efficient schedule is more important than making an accurate prediction on an inefficient schedule. To capture this behavior, we introduce a term \( \alpha \) which, for a given pipeline \( p \) and schedule \( s \), is the ratio of the run time of the best schedule for \( p \) and the run time for the current schedule \( s \).

\[ \alpha = \frac{\min(\text{Schedules}(p))}{y_{ps}} \]

- **Property 3.** The loss function should give more importance to less noisy measurements compared to measurements that have more noise. To embody this property, we define \( \beta \) as the inverse of the standard deviation of measurements of a schedule \( s \) of a pipeline \( p \).

\[ \beta = \frac{1}{\text{std}\_dev(y_{p_1}, y_{p_2}, ..., y_{p_N})} \]

We combine the three terms to compute the final loss, as shown in the equation below.

\[ l_{ps} = \xi, \alpha, \beta \]

IV. Evaluation

This section explains the evaluation methodology and presents our findings and results. We assess the prediction accuracy of the proposed performance model on the test dataset and compare it with the Halide and TVM models. We also evaluate the model’s performance on ranking schedules derived from nine well-known deep-learning networks.

A. Prediction Accuracy

(a) Average Error(%) (lower is better) Percentage error between the measured (actual) and predicted run times computed for the test set.

(b) Maximum Error(%) (lower is better) The maximum percentage error recorded.

(c) \( R^2 \) (higher is better) \( R^2 \) score or the coefficient of determination quantifies how well the model fits the observational data. With values between 0 and 1, a higher \( R^2 \) score indicates a better fit.

Fig. 8: Quality of our performance model vs. Halide and TVM models

We train our model on a database of 1.6 million schedules, derived from 10000 randomly generated ONNX models, converted into Halide pipelines. We use two existing performance models for comparative evaluation. The Halide [5] model also uses a neural network, and we train and evaluate it on our train and test set. The TVM [7] model does not use a pre-trained model. Instead, it uses adaptive online learning via an exploration phase where different schedule configurations are benchmarked. Since it does not require any pre-training, we used the test split of our dataset on this XGBoost based model.

The plots in figure 8 compare the three performance models. In terms of mean percentage error computed for the test set, our model is 7.75x and 12x better than the Halide and TVM models, respectively. The graph-based model can learn and represent relationships between different stages, making it more accurate. We also record the maximum error in the test set, and on this metric, our model outperforms the other two by a significant margin. The \( R^2 \) score, also called coefficient of determination, is a statistical measure of how well a regression model fits the observations. The closer this value is to 1, the
better the fit. The graph-based model achieves a higher $R^2$ score of 0.92 compared to the Halide and TVM models, which have a score of 0.89 and 0.81, respectively.

B. Ranking Performance

A standard application scenario uses models like ours to rank schedules. A searcher utilizes the ranking information to select a subset of promising schedules and explore them further. In such settings, rather than directly using the actual raw predictions, we use the model to estimate the relative performance of multiple schedules. The more accurate the model, the better it will be at ranking schedules and enable the search to progress in the right direction.

Figure 9 displays the pair-wise ranking performance of the model on several hundred schedules for the nine neural networks shown along the x-axis. The schedules were generated using the Halide auto-scheduler. For all possible pair-wise combinations of schedules belonging to a network, we count the number of pairs in which the model assigned a lower run time to the faster schedule. The chart shows the percentage of pairs correctly ranked by the model. The ranking accuracy ranges from 65\% for shufflenet to as high as 90\% for wavenet, with an average accuracy of around 75\%.

V. RELATED WORK

Apart from the Halide \cite{halide} and TVM \cite{tvm} models, which we used as baselines for comparative evaluation, there have been several efforts to develop statistical models to predict the performance of deep learning programs. These efforts vary in terms of the core architecture, target environment, feature engineering, etc. As has already been discussed, TVM incorporates two performance models based on gradient boosted trees (GBT) and treeGRUs, which represent the loop-nest (low-level AST) as a vector embedding and maps the embedding to the cost using a linear layer. The Halide model \cite{halide} uses a feed-forward neural network. The network learns to predict the run time conditioned on handcrafted features extracted from the program. Recent work on Halide replaces the feed-forward network with a bi-directional LSTM model and demonstrates significant improvement in prediction accuracy \cite{halide}. The performance model proposed in this work also targets Halide and uses similar handcrafted features. However, our model exploits the inherent graph representation of programs using graph convolutional networks.

In \cite{halide}, the authors develop a model to predict the efficacy of code transformations in the Tiramisu compiler. Their composite model built using LSTM and feed-forward networks comprises three distinct modules to embed the computations within a loop, embed the nested loop structure, and a layer to predict the final speed-up. Recently, graph networks based performance models have been proposed for XLA programs on TPUs \cite{tvm}. In addition to using a different graph architecture, their work targets a different class of hardware in contrast to our work which focuses on CPUs. Their approach also decomposes the computational graph of the XLA program into smaller sub-graphs, whereas our model analyzes the entire graph of a Halide pipeline. Moreover, the authors train separate instances of the model for distinct optimization tasks like tile size selection and operator fusion. Our model, on the other hand, is generic and meant for combinatorial optimization search strategies.

The first Halide auto-scheduler \cite{halide} utilized a simple static analytical model to perform a greedy search in a templated schedule space. The simplicity of the model led to fast compilation times with no benchmarking or tuning. However, the compiler explored a limited subset of the schedule space and ignored potentially useful schedules comprising multi-level tilings and a wide range of choices for vectorization and parallelism. Subsequent work \cite{halide} proposed a richer, still manual, model that incorporated the memory access features of modern CPUs like caching and prefetching to optimize the implementation of a Halide operator. An extension to this work \cite{halide} used the model as a part of a back-tracking search capable of scheduling entire pipelines. In the more general context of applying machine learning to improve compilation frameworks, \cite{tvm} provides a comprehensive survey. Ithemal \cite{tvm} is a deep learning-based architecture to predict the throughput of straight-line x86-64 code.
VI. Future Work

This work presents preliminary evidence of the benefits of using Graph Networks to model the performance of deep-learning applications. In this section, we discuss several ways to foster better integration and improve the proposed design.

A. Feature Engineering

The current model relies upon a very complex feature engineering process. Reliance on manual hand-crafted features limits a model’s portability. For example, while the current set of features is applicable across CPU platforms, it would require significant work when porting to other hardware architectures like GPUs, custom ASICs, and FPGAs. We plan to explore alternative ways to represent deep-learning programs to reduce our reliance on handcrafted features and foster better compatibility across platforms. Such an automated feature engineering strategy would rely on learning representations of the program structure (abstract syntax tree, for example) and learning direct embeddings of tokens in the program. We also intend to study the trade-offs between the two design choices.

B. Model Improvements and Optimizations

We evaluated our model on a dataset of 1.6 million schedules derived from 10,000 pipelines. Generating this dataset took weeks and required an enormous amount of computing power and resources. We plan to examine the role active learning can play in our application scenario and help retain the same accuracy with a smaller training set.

As a follow-up to the current work, we are integrating the proposed performance model with the Halide auto-scheduler to gain a measure of scheduling/computation times and analyze bottlenecks. Using a model like ours for compilation is significantly faster than auto-tuning approaches. However, we plan to compare our model with existing Halide models in different pipelines, evaluate the performance of our model with different benchmarks, and benchmark them on Intel Xeon CPUs. Experimental analysis demonstrates that the proposed model outperforms state-of-art Halide and TVM models, with a 7.75x and 12x reduction in prediction error, respectively. Moreover, our model is approximately 75% accurate when performing a pair-wise ranking of hundreds of schedules derived from 9 real world pipelines.

VII. Conclusion

This paper presented a novel Graph Neural Network-based performance model to estimate the run times of deep learning pipelines implemented using the Halide framework. We proposed a network architecture based on Graph Convolutions capable of capturing interactions between neighboring nodes to generate richer representations that improve prediction performance. The model, implemented in PyTorch, takes features extracted from deep-learning programs implemented in Halide as input and outputs the run time. We generated a dataset of 1.6 million schedules from around 10,000 different pipelines and benchmarked them on Intel Xeon CPUs. Experimental evaluation demonstrates that the proposed model outperforms state-of-art Halide and TVM models, with a 7.75x and 12x reduction in prediction error, respectively. Moreover, our model is approximately 75% accurate when performing a pair-wise ranking of hundreds of schedules derived from 9 real world pipelines.

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