DESIGN OF LOW POWER DICKSON CHARGE PUMP USING THE ASSOCIATED CIRCUIT AT SYSTEM LEVEL

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Abstract

This paper proposes the design strategy of low power Dickson charge pump using associated block who is help in proper functionality at full chip level because of single charge circuit cannot be design for portable handheld based application. When a low power optimization based high speed charge pump circuit is designed at system level, then entire circuit block operates at different supply voltage so it requires. For this, the circuit designer needs a level shifter to manage the dual supply voltage and provide a non-overlapping ring oscillator to provide the clock to the circuit to operate at high speed. CMOS clocked circuit is required to work in sufficient voltage level pushup up to end level. Thus, In this paper, the actual simulation results using the CMOS 180nm technology along with each block are shown. Along with this, good brief discussion on each block has also been done.

Keywords: Charge Pump, Ring Oscillator, NOC clock generator, clocked D-FF and CMLS level shifter.

I. Introduction

Charge Pump (CP) Circuit is very widely used in integrated devices. When require DC voltage higher than input supply voltages for the used in CP [1]. The
Circuit is a family of switch capacitor circuits as shown in Fig 1. The word of Charge Pump is a combination of Charge+ Pump means that charging phenomenon by pumping capacitors is connected with every transistor, and taking up generated charge through pumping action by non-overlapping clock generator circuit [II,III,IV]. Most of charge pump used in small electronics based hand held low power devices. The trends of low power VLSI Design at the same time, increasing requirements on speed and throughput have resulted in the use of shorter channel lengths and lower threshold voltage in CMOS process [III,IV,V]. Except in parallel operation, higher throughput demands increase in clock rate and active current consumption [VI, VII]. Low threshold devices suffer from significant sub threshold leakage currents [VIII]. Hence, even though as low power consumption has become important, technology trends are pushing it upward. Therefore, many researchers are required to deliver smart policies for power management, while still providing appearance of high-speed function [III, VIII]. So, it very emerging research area for huge DC/DC converter application (low and high power) as shown in fig 2. In this article, describe about system block of charge pump as shown in fig 3, which good clock generation circuits works as an accelerator to increase speed-up and reduce the losses. Thus, required clock generation circuits is vital role play for all types switch capacitor circuits family.

![Fig 1 Classified family of switched capacitors](image)

This is found in the research study linked by the Dickson CP and their individual circuits for example C2CMOS based DFF, NOC clock circuit using oscillator, manage the dual supply voltage based CMLS shifter at system level as shown in Fig 3. one of the most likely architecture in Dickson CP due to small topology with desired voltage can obtain according to requirement by modifying the circuit. This work is carried out of my previously published paper, which used several associated techniques in the Dickson charge pump [VIII, XIV, XVI, XVII]. In this article, a short chronological review of Dickson charge pump and their modification with utilization, describe in step by step is, Introduction in section I, key parameter of designing in section II, Ring Oscillator and clock generation circuit with simulation result in

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Clocked CMOS DFF based Dynamic logic circuit in section IV, supply management unit level shifter with simulation analysis result in section V, Dickson charge pump circuit in section VI, completed system block with result and analysis in section VII, comparative simulation result using associated block and without associated block in section VIII and conclusion in section IX.

Area and Application of Charge Pump

**CHARGE PUMP DESIGN AREA**

- Two phase clock based CPs
- Four Phase based clock CPs
- Circuit design according to application as well as low and high power.

**Research Area**
- ✓ Efficiency
- ✓ Power dissipation
- ✓ Area issue
- ✓ Parasitic Resistance
- ✓ Parasitic capacitance
- ✓ Body effect and threshold voltage cancellation
- ✓ High speed clock
- ✓ No. of stages

**Application**
- ✓ Non-volatile memory
- ✓ White LED driver
- ✓ Solar cell
- ✓ Pacemaker
- ✓ Biomedical applications
- ✓ RF application
- ✓ Sensor network
- ✓ RFID application
- ✓ Thermoelectric Generator
- ✓ Processor

**Circuit design mechanism**
- ✓ Inductor less charge pump (only capacitive architecture)
- ✓ Inductor based High Power application
- ✓ Small integrated inductor using meta wire low power application
- ✓ Inductor less charge pump is less efficient than capacitive charge pump

Fig 2 Charge Pump application and research area

Fig 3 Proposed Block diagram
II. PARAMETERS FOR DESIGNING

Better output results can be obtained in Dickson charge pump using the system architecture. As per the design rules given below in order to extract the full potential, enable increased profitability of systems [9] the following major points are considered.

- To Efficiency Improvement, current should be delivered up to regulation in whole circuit.
- Vt drop problem through high amplitude clock
- Reduced ripple in output voltage using LC techniques
- Reduced RON resistance through W/L sizing ratio techniques
- Efficiency Comparison for Dickson Charge Pump DC/DC Converters
- To reduce power consumption, circuit complexity must be reduced.

| Simulation                  | Transient Analysis              |
|-----------------------------|---------------------------------|
| Oxide capacitance           | 8.46 fF/ (µm)²                  |
| Technology used             | 180 nm NMOS Level-49Technology (MOSIS) |
| Vt                          | High Vt 0.49                    |
| Length of channel           | 0.89 µm                        |
| Oxide Thickness             | 4.6 nm (NMOS) & (PMOS)          |
| K_nμ*Cox                    | 292 micro-ampere/votage²       |
| K_pμ*Cox                    | 1455 micro-ampere/votage²      |
| Supply voltage              | 1.8V                           |

III Circuit Diagram Of Ring Oscillator Using Non-Overlapping Clock Generator

The clock generator circuit is pumping key of switch capacitors who’s provide alternating clock signal to continue increasing pumping action which elevating the charge is step by step as shown in Fig 4. So, clock circuit is design done by ring oscillator (overlapping clock generation) circuit who's play vital role for high efficiency and charge transferring in every period higher voltage gain conversion.
Every CMOS delay element is generally made using an even number of inverters. The role of every buffer stage to provide balanced rise and fall time up to output level. NOC generator circuit will fluctuate with voltage and temperature process variation is also reducing dynamic power operation during circuit switching operation [IX, XI]. In order to design the charge pump, it has designed several collaborative circuits for which non-overlapping two phase circuits are constructed through NAND / NOR circuits along with re-shaping supporting blocks such as clocked D flip-flop block is described in next section. Non-overlapping circuit is reducing dynamic power operation during circuit switching operation.

Fig 5 Ring oscillator with non-overlapping clock

Overlapping clock without NOR circuit                Non-overlapping clock provide using NOR

Fig 6 Clock waveform for charge pump circuit

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Fig 7. Clock Output of CMOS Ring Oscillator with MOS Capacitor using non-over clock

Fig 8 Power result of Ring Oscillator

Fig 9 Current of Ring oscillator
TABLE-2 Result of Ring Oscillator using non-Overlapping Clock

| Rise Time | Fall Time | Propagation Delay | Power Consumption | Current   |
|-----------|-----------|-------------------|-------------------|-----------|
| 5.15 ns   | 5.21 ns   | 3.1 ns            | 38.6 μw (max)     | 100 μA (max) |
|           |           |                   | 19.8 μw (Avg)     | 50 μA (Avg)  |

IV. Clocked CMOS Master-Slave Based DFF

The positive edge triggered static DFF master-slave structure based dynamic logic clocked CMOS circuit is useful for pulse recycling that is construct to minimize the loss of power during low to high transition [XII]. The almost reduce static power...
dissipation to large extent during, high to low transition due to CMOS property based dynamic logic circuit already consume less power [XIII]. Then ring oscillator output feed to Clocked DFF. The DFF is used to reshape the ring oscillator frequency, which is not perfect rectangular shape and also for divide the frequency by two. It is low power C^2MOS D-FF during this signal frequency of each stage is half that of its preceding regulation block.

CN and C provide non-overlapping clock with small rise-fall time by clock generation. The output of C^2MOS DFF is available during the entire clock cycle, actively during only when the clock is high, pull-up transistor also improves the noise immunity and allow longer evaluation time [VII].

![Dynamic Logic based CMOS based Master-slave D-FF](image)

**Table-3 Simulation Result of DFF**

| Vdd = 1.8V Frequency = 3.3 MHz | Power | Current | Rise/Fall Time (output)_V(Q) | Rise/Fall Time (output)_V(QN) |
|-------------------------------|-------|---------|-------------------------------|-------------------------------|
| 64.85 µw (max)                | 64.85 µw (max) | 942.41 ps/1000 ps | 635.71 ps/609 ps |
| 12.86 µw (avg)                | 12.86 µw (avg) |                         |                              |
ASIC designing become complicated because of the scaling down technology in low power domain at full chip level [VI, XVI]. As we know, to construct a CP circuit, we have to attach multiple circuits to better results such as minimal power outages to minimize unwanted effects and for efficiency improvements [XIV]. Now some of these circuit blocks operate at lower voltage and some higher voltage, the designer needs a shifter circuit to manage these voltages, that circuit needs to be a shifter of a voltage level is called level shifter [XV].

Block of level shifter is used to one supply level to another voltage level in between I/O circuits and core circuitry for shifting the level and reduce the crowbar current (VDDH to VDDL), which due to increase the switching speed as well as energy per switching according to minimum operating voltage has been chosen [XV]. Level shifter control block control and minimize the power of Dickson charge pump circuit output voltage. The contention mitigated level shifter (CMLS) is better than conventional level shifter from power dissipation, preferable in high frequency and delay point of view, along with this, the crowbar current can also be reduced contention with the help of CMLS level shifter.

The conventional level shifter cannot be used in high frequency. The shifter is shifting the supply of CP circuits (VDDH to least VDDL) that is need for the control circuit to function correctly. The converting voltage phase low to high to provide minimum switch losses.

Fig. 14 Output of clock voltage, current- power by dynamic D-FF

V. Circuit of Contetion Level Shifter

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Fig. 14 Output of clock voltage, current- power by dynamic D-FF
The Key benefit of CMLS shifter is avoiding crowbar current lowering. MOS transistor Positioning of MN1-MP3 & MN2-MP4 is works as partially inverter. So, the working point of A and B are speedy than Conventional shifter. Hence, transition delay and switching power can be reduced to a large extent in contention level shifter due to contention also reduces the current tide. The use of shifter in charge pump circuit, change the position of dual supply voltage 1.8 to 0 V or 0 to 1.8 during the transition.

Table 4  Simulation Result of Level shifter (CMLS) at Vdd =1.8V

| Power            | Current         | Rise/Fall Time (output)_ V(Q) | Rise/Fall Time (output)_ V(QN) |
|------------------|-----------------|-------------------------------|--------------------------------|
| 325 μw (max)     | 180 μw (max)    | 2.60 ns/1.23 ns               | 1.36s/1.65 ns                  |
| 22 μw (avg)      | 12.2 μw (avg)   |                               |                                |

Fig 16 Level Shifter (CMLS) simulation Result
VI. Charge Pump Circuit

The DCP (Dickson Charge Pump) architecture based on gate and drain is tied together based on NMOS Pass architecture. It is very popular DC/DC boost converter, easy to modified and changes in architecture [XVII]. It can be designed for low and high voltage applications. The problem of DCP is loss of voltage equal to $V_{TH}$ (threshold voltage) drop in preceding number of stages [XVIII]. The effect of threshold voltage can be reduced by increasing the voltage of the pump by a clock circuit design. Along with this, to remove the problem of body effect in its device $V_{sb1}=0, V_{sb2}=2=0$.

Fig 17 NMOS using charge pump

The voltage gain equation of Dickson charge pump on every stage is

$$V_{OUT} = V_{DD} + N \times (V_{DD} - V_{TH})$$  \hspace{1cm} (1)

Where is $V_{dd}$-$V_{th}$ is voltage gain of each subsequent stages, $N$ represented the cascaded stages $V_{CLK}$ is peak clock voltage of signal, $C_{pump}$ is the boosting capacitor, $C_{par}$ is the parasitic capacitance, $I_{out}$ is the pumping current. Increasing size of transistor, the total parasitic capacitance and overall silicon area, which reduces the total power efficiency, can be written as below [IV]

$$V_{OUT} = V_{IN} + N \times \left( \frac{C_{pump}}{C_{pump} + C_{par}} \right) \times V_{CLK} - \frac{N \times I_{out}}{(C_{pump} + C_{par}) \times t} - R_{ON} \times R_{OUT}$$ \hspace{1cm} (2)

$I_{power}$ is the average current consumed from power supply voltage; $\frac{V_{out}}{V_{dd}}$ is the voltage gain (Pumping gain), $\alpha$ is the ratio of the parasitic capacitance to pumping capacitor value [II, XVII].

$$\eta = \frac{I_{Lead} \times V_{out}}{I_{power} \times V_{dd}} \times 100 = \frac{V_{out}}{V_{dd}} \times \left( \frac{\sqrt{N+1} \times V_{out}}{(N+1) \alpha \times V_{dd}} \right) \times 100$$  \hspace{1cm} (3)
The α is a technology-dependent parameter and ranges from 0.1 (for poly-poly capacitors) up to 0.3 like metal-metal capacitors. The efficiency parameter is main design consideration in charge pump circuit design, it is depends on maximum power delivered from input to output with minimum loss.

VII. Complete System Design Block

This system block of Dickson charge pump as shown in figure help for designing in system level chip because it is crucial task power management at system level. Single block of charge pump circuit is never can work without clock generation circuit, therefore to make the better clock generation and reduce dynamic switching power at clock level through clocked CMOS based DFF. Some block operates below the supply voltage for which is managing the dual supply through Level shifter. Thus, all circuit block in system level designing is play major role.

![Fig 18 Proposed Design techniques of Dickson charge Pump](image1)

![Fig 19 output result of charge pump](image2)
This article presents the simulated results that characterize the Low Power Charge pump with Ring oscillator Using 180nm CMOS Technology. The specification of the Charge pump is given in the table.

**Table 5 Design Specifications:**

| Specification                        | Name            | Value           |
|--------------------------------------|-----------------|-----------------|
| Steady output Voltage                | V_{OUT}         | 10 V            |
| Pumping Cap (C₁ to C₅)               | C₅              | 4 pico farad    |
| Output Load capacitance              | C_L             | 1 pico farad    |
| Output voltage ramp time             | T_{RAMP}        | 5 micro second  |
| V_{DD}                               | V_{DD}          | 1.8V            |
| Average pump current consumption     | I_{PUMP}        | 6 μA            |
| Rise/fall time                       |                 | 2.60ns / 1.23ns |
| Ramp-up time (simulation time)       |                 | 10 μs           |
| Propagation Delay \( \tau \)         |                 | 245.38 ps       |
| Average Current                      |                 | 8.44 μA         |
| Average power                        |                 | 270 μW          |
| Mos Capacitance Value by using \( C_{ox} = \frac{C}{\alpha x * w * L} \) | W=L=22       | 2 Pico farad    |

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VIII. Simulation Result

From Fig 22 this is shown output voltage is directly proportional to numbers of pump stage, The comparative analysis between without associated pump block of charge pump and using system block, which directly impact on output voltage, actually output voltage is degraded due to Vt drop-loss problem in every stage means that also effect on pump current, pump power and efficiency.

Because of system block is provide better clock circuit which prevent the dynamic power switching loss and output voltage degradation.

![Fig 22 Relation between output voltage and No. of stage](image)

As from fig 23, relation between power efficiency and output current using associated block. The efficiency will be increasing then power conversion efficiency also increases with better improvement in efficiency in Dickson charge pump. it is big challenges because of Dickson charge pump efficiency cannot rise above 48% without design system block, while efficiency can achieve up to 80% using with system block architecture.

![Fig 23 Relation Between output current and Power Efficiency](image)
IX Conclusion

The final conclusion of this paper is when design a charge pump circuit small power and voltage for portable application then it is very difficult to design as per portable application requirement then that it is big challenge to design charge pump circuit in low power with minimal current operation for extended battery life time, so it cannot be possible without follow proper designing steps. In this article tries to explain which steps needed for a better charge pump such as better pump clock generation by Ring oscillator and Clocked CMOS D-FF to provide proper pumping action. This is very key block of charge pump circuit, another block is Level shifter when, at a system-level, two voltage levels are supplied, then Level-shifter voltage acts the level shifting of high to low and low to high voltage is vice versa during the manage dual supply (1.8 V & 1.0 V) system level, there is no need to provide a separate power supply to the circuit. is done with the help of level-shifter. Thus, the importance of article main system block is explained and the actual simulation result of individual block is presented.

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