EUV Lithography Technology for High-volume Production of Semiconductor Devices

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After years of efforts, extreme-ultraviolet (EUV) lithography reached a significant milestone in 2018: readiness for high-volume production of advanced semiconductor devices. A EUV source power of 250 W has been realized, providing a tool throughput capability exceeding 140 wafers per hour at a dose of 20 mJ/cm². The full-wafer critical dimension (CD) uniformity is now less than 0.5 nm for multiple systems and matched-machine overlay is at 1.1 nm. These imaging and overlay performances meet the production requirements for the 5-nm node logic and 16-nm dynamic random access memory (DRAM) devices. Meanwhile, ASML continues to improve the performance of EUV exposure tools to obtain higher throughput, better image quality, and tighter overlay specifications, thereby further enhancing productivity and capability. Further improvements in resist and mask materials are required to extend EUV single-patterning to the low-k1 regime. Finally, ASML has begun to develop an EUV exposure system with a numerical aperture (NA) of 0.55 to enable continued scaling in semiconductor manufacturing beyond the next decade.

Keywords: Extreme ultra violet, EUV lithography, Scanner, Reticle, Pellicle

1. Introduction

EUV lithography was first demonstrated by Prof. Hiroo Kinoshita in 1986 [1]. The first two full-field (26 mm × 33 mm) research systems were delivered by ASML to research and development organizations in 2006 [2]. Since then, the development of EUV lithography has accelerated, and a test device structure based on EUV was demonstrated [3,4]. In 2011, R&D exposure systems, the NXE:3100, containing newly developed optics with a NA of 0.25 were developed and delivered to semiconductor companies [5]. The NXE:3300 system, which has a higher NA of 0.33, was delivered in 2013 [6]. The development of these scanner systems prompted significant progress in the development of mask and resist materials. The latest system (NXE:3400) was developed in 2017 [7], and a total of forty 0.33NA EUV systems were delivered to our customers by the end of 2018. A brief history of EUV exposure systems is shown in Fig. 1 [8].

The minimum resolution of optical lithography continued to shrink over the decades as a result of wavelength (λ) reduction, better optics with higher NAs, and k1 (a process factor) reduction, since, in terms of the minimum half-pitch (HPmin), the resolution is given by

\[ HP_{\text{min}} = k_1 \frac{\lambda}{NA}. \]  

Fig. 1. A brief history of EUV exposure systems.

193 nm is the shortest available exposure wavelength that can work in conjunction with the maximum NA = 1.35 using water immersion. However, minimum feature sizes of semiconductor
devices continued to scale, and the theoretical limit of $k_1 = 0.25$ was reached and surpassed by adopting multiple patterning techniques. However, to continue scaling semiconductor devices, three to four exposures are required e.g. to form one metal layer in a 10-nm-generation logic device. As shown in Fig. 2 [9], fidelity of the device pattern resulting from three immersion exposures is degraded compared to that from a single EUV exposure. Moreover, the pattern suffers from degraded CD uniformity, overlay error between exposures, and poor defectivity. Besides, the EUV single-exposure process is much simpler than the multi-patterning processes and results in shorter processing time and a lower tool footprint in the fab. EUV lithography is finally entering the stage of volume production. Two semiconductor companies have announced that they would begin high-volume production using EUV lithography in 2019 [10,11].

Fig. 2. SEM image of 48nm pitch 2D pattern using ArF immersion triple patterning and EUV single exposure.

2. Outline of the EUV exposure system

EUV light with the wavelength of 13.5 nm is absorbed by all substances. Therefore, refractive optics cannot be; all reflective optics, including the mask, have Mo/Si multilayer reflective coatings based on Bragg’s law. Since air also absorbs EUV light, the system must be a vacuum system. Since mirror surface contamination affects EUV reflectivity, a clean vacuum chamber is critical. In particular, hydrocarbon and hydrogen oxide contamination must be kept to very low [12].

A high-power light source is critical for the EUV exposure system. Laser-produced plasma (LPP) sources with tin (Sn) droplets are commonly used [13]. The principle of LPP sources is shown in Fig. 3 [14]. A high-power and high-frequency (50–100 kHz) CO$_2$ laser zaps the Sn droplets to produce a plasma that emits EUV light. The EUV light is then reflected by an ellipsoidal mirror, the “collector”, and is re-focused onto the other focal point of the mirror, the “intermediate focus”, that leads to the inside of the EUV system. The shape of the droplet is optimized to achieve a high conversion efficiency of 6%.

Fig. 3. EUV light generation using laser-produced plasma.

An example layout of EUV optics with a six mirror projection optics design is shown in Fig. 4 [15]. All illumination and projection optics, including the mask, are mirrors. Since the wavelength of EUV light is 1/14th that of 193-nm deep-ultraviolet (DUV) light, the surface profile and roughness of the mirror require much higher accuracy to maintain sufficiently low aberration and flare [16]. As shown in Fig. 4, the chief ray angle is tilted away from the normal to avoid interference between the incident and reflected light.

Fig. 4. Example EUV optics design. 6 mirror projection optics are shown.

Fig. 5. Illumination optics supporting flexible source configurations.
Similar to DUV systems, the EUV system contains a flexible illumination system (Fig. 5). The illumination system combines a field facet mirror, which creates an exposure slit shape, and a pupil face mirror, which creates a pupil shape. A pupil fill ratio of 20% is supported in the NXE:3400 system without energy loss [17].

Some EUV-specific imaging issues should be considered, including shadowing [18] and mask three-dimensional (3D) effect [19]. Since the chief ray angle is at six degrees from the normal, the resulting shadowing effect of the absorber causes a difference in CD between features oriented in the vertical and horizontal axes. This difference must be pre-corrected in the mask patterns. Furthermore, the thickness of the absorber is much greater than the EUV wavelength; thus, the mask 3D effect is not negligible. Therefore, the optical constants n and k along with the absorber thickness must be optimized to extend the imaging performance into the low-k1 regime.

Another issue concerns the line edge roughness (LER) or local CD uniformity (LCDU). EUV light has a much higher photon energy than 193-nm DUV light. It has thus a larger stochastic noise than DUV light at the same dose. LCDU is expressed as [20].

\[
\text{LCDU(nm)} \approx \sqrt{\frac{h \nu}{\alpha}} \left(1 + \frac{1}{QE}\right) \frac{1}{E_{size} \text{NILS}}
\]

Where QE is the quantum efficiency, E_{size} is the dose to size, and NILS is the Normalized Image Log Slope. It is therefore important to reduce the resist contribution, improve the image quality, and optimize the mask bias to reduce LCDU under realistic dose conditions. All these factors have a large effect on total CD uniformity.

3. **System performance of NXE:3400B**

3.1. Imaging and overlay

Figure 6 shows aberration and distortion data for the NXE:3300, 3350, and 3400 systems. The aberration wavefront and lens distortion were clearly greatly improved as the system models advanced [7]. Figure 7 shows the CDU and overlay data for the NXE:3400B system [21]. The full-wafer CDU is less than 0.5 nm. The overlay, particularly the matched-machine overlay, is improved in the NXE:3400 system compared to the NXE:3350 system. The specification of 2 nm is consistently met, with some systems achieving values below 1.1 nm. These improvements are attributed to improvements in flatness in the reticle stage and wafer stage clamps along with improved calibrations.

![Fig. 6. Distortion (non-correctable error; NCE) and aberration has been improved from NXE:3300, 3350 to 3400 projection optics.](image)

![Fig. 7. CD uniformity and overlay performance of NXE:3400B.](image)

The performance meets the requirements for 5-nm-generation of logic and 16-nm-generation of DRAM devices.
3.2. Defectivity

The challenge of defectivity is addressed in parallel: reducing the scanner contribution and developing an EUV-compatible pellicle that can withstand the required high source power and throughput. Figure 8 shows the improvement of reticle front-side defectivity achieved over the past five years [8]. Coming from a situation of ~100 particles added to the reticle front side per 10,000 exposed wafers, the performances of the latest configuration systems are now well below 10 adders per 10,000 wafers, with multiple data points even showing no adders at all. We have developed a roadmap to allow us to consistently meeting the high-volume manufacturing target of fewer than 1 adder per 10,000 wafers. This roadmap addresses the mechanisms for particle generation, particle release, and particle transport to the reticle [22].

A detachable pellicle frame is shown in Fig. 9 [25]. As no material with high transmittance is available for the current photon- or electron-beams-based inspection tools, the pellicle must be removed during mask inspection. This frame enables mask pattern inspection using DUV light or an electron beam.

3.3. Productivity

Productivity has continuously improved through various source and scanner developments. A source power exceeding 200 W is required to support a productivity of 125 wafers per hour (wph). The latest source system is shown in Fig. 10. Enhancing Sn target formation through improved conversion efficiency and increased CO2 laser output power has enabled us to achieve a pulse energy of 5 mJ, corresponding to source power greater than 250 W [26,27]. A new high-power seed module that includes improved optical isolation is a key technology in delivering the required CO2 laser power. Figure 11 shows the operational power performance. As shown in the figure, stable operation at >250 W is achieved for over a period of one month in multiple systems.

Using the latest NXE:3400B system with improved throughput supported by the 250-W source power.

EUV-compatible pellicles are also being developed in parallel [23,24]. EUV pellicles must achieve high and uniform transmittance while meeting the requirements for heat resistance, mechanical strength, and durability against EUV light. We are developing pellicles based on polycrystalline silicon-based membranes, and we are currently focused on improving film cleanliness (defectivity), increasing EUV transmittance, and lowering its non-uniformity. The power levels of EUV sources are rapidly increasing; thus, there is strong demand for pellicle films with improved power capability.

Fig. 8. Defectivity trend of the reticle front side. The number has been reduced to under 10 per 10,000 wafer exposures.

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Fig. 9. EUV pellicle frame concept and demonstration model.
power along with improved transmission and reduced overhead, a productivity of 140 wph has been demonstrated at a dose of 20 mJ/cm². Excess power can be used to extend the collector lifetime and increase the throughput beyond 150 wph. We expect that 125 wph with the pellicle can be achieved using this configuration, based on the transmittance roadmap of the pellicle film. The rate of source power degradation has been reduced, allowing high system throughput to be maintained.

4. Future EUV lithography systems

ASML and our partner Carl Zeiss are developing a high-NA EUV exposure system with NA = 0.55 along with tightened specifications that allow continued scaling in semiconductor manufacturing beyond the next decade [28-30]. The goal of this effort is to enable EUV single-patterning at a minimum pitch less than 20 nm. Figure 11 shows that an effective throughput of contact hole formation with NA=0.55 versus NA=0.33 case [31]. 0.55 NA system enables much higher effective throughput thanks to a single exposure in a half pitch region which 0.33 NA need multiple exposures.

Fig. 12. Advantage of contact hole imaging using 0.55 NA compared with 0.33 NA. The clear advantage in the effective tool throughput for the high-NA case.

EUV lithography has advanced to the point where advanced semiconductor devices can be produced in high volume. Multiple patterning techniques involving ArF immersion have reached their scaling limit because of high process complexity along with difficulties related to CD and overlay control. EUV lithography enables continued scaling of semiconductor devices using a single-exposure process made possible by remarkable progress in industrialization techniques. A source power of 250 W has been realized, providing a tool throughput capability exceeding 140 wph at a dose of 20 mJ/cm². The latest system demonstrated a full-wafer CD uniformity of less than 0.5 nm and an overlay of 1.1 nm. These imaging and overlay performances meet the requirements for 5-nm-generation of logic devices. ASML continues to improve the performances of EUV scanners to obtain higher throughput and tighter overlay specifications, further enhancing productivity and capability. Additional improvements in resist and mask materials are required to extend EUV single-patterning to the low-\(k_1\) regime. Finally, ASML has begun to develop an EUV exposure system with NA = 0.55 to enable continued scaling in semiconductor manufacturing beyond the next decade.

5. Summary

EUV lithography has advanced to the point where advanced semiconductor devices can be produced in high volume. Multiple patterning techniques involving ArF immersion have reached their scaling limit because of high process complexity along with difficulties related to CD and overlay control. EUV lithography enables continued scaling of semiconductor devices using a single-exposure process made possible by remarkable progress in industrialization techniques. A source power of 250 W has been realized, providing a tool throughput capability exceeding 140 wph at a dose of 20 mJ/cm². The latest system demonstrated a full-wafer CD uniformity of less than 0.5 nm and an overlay of 1.1 nm. These imaging and overlay performances meet the requirements for 5-nm-generation of logic devices. ASML continues to improve the performances of EUV scanners to obtain higher throughput and tighter overlay specifications, further enhancing productivity and capability. Additional improvements in resist and mask materials are required to extend EUV single-patterning to the low-\(k_1\) regime. Finally, ASML has begun to develop an EUV exposure system with NA = 0.55 to enable continued scaling in semiconductor manufacturing beyond the next decade.

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