SeaPlace: Process Variation Aware Placement for Reliable Combinational Circuits against SETs and METs
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Abstract—Nowadays nanoscale combinational circuits are facing significant reliability challenges including soft errors and process variations. This paper presents novel process variation-aware placement strategies that include two algorithms to increase the reliability of combinational circuits against both Single Event Transients (SETs) and Multiple Event Transients (METs). The first proposed algorithm is a global placement method (called SeaPlace-D) that places the cells for hardening the circuit against SETs by solving a quadratic formulation. Afterwards, a detailed placement algorithm (named SeaPlace-G) is proposed to increase the circuit reliability against METs by solving a linear programming optimization problem. Experimental results show that SeaPlace-G and SeaPlace-D achieve 41.78% and 32.04% soft error reliability improvement against SET and MET, respectively. Moreover, when SeaPlace-D is followed by SeaPlace-G, MET reduction can be improved by up to 53.3%.

Index Terms—Circuit Reliability, Placement Algorithm, Single Event Transient, Multiple Event Transient, Process Variation.

I. INTRODUCTION

The reliability of nanoscale digital circuits is becoming increasingly important in recent years [1]. Due to aggressive technology scaling, the vulnerability of digital circuits to single-event transients (SETs) and single-event upsets (SEUs) caused by radiation induced transient faults is increasing [1]-[3]. On the other hand, process variations caused by technology scaling has introduced new challenges in the circuit reliability [4]. As shown in [5], process variations can impose 10%-50% variations to the soft error rate (SER) of circuits, leading to significant unreliable fabricated circuits. Hence, it is critical to address these issues to improve reliability of digital circuit designs.

SETs and SEUs are transient faults threatening the soft error reliability of circuits and are generated when a high energy particle strikes in combinational logics and sequential elements of circuits, respectively [6]. Due to technology scaling, the critical charge has reduced and a high-energy particle can affect several adjacent cells in a circuit causing Multiple Bit Upset (MBUs) and Multiple Event Transients (METs) in memory elements and combinational circuits, respectively [7]. When a transient fault is propagated through the combinational component and latched into a sequential element, a soft error is happened. Its occurrence rate is evaluated by Soft Error Rate (SER) metric [8]. The recent studies indicate that SER of the combinational component of a circuit comprises a remarkable portion of the SER of the entire circuit [9], [10]. Moreover, recent studies have shown that a notable fraction of particle strikes results in METs [11] and for technologies below 50 nm, the probability of MET occurrence is equal to that of SETs [12]. Therefore, in order to increase the circuit reliability effectively, both SETs and METs need to be considered in hardening techniques.

Over the past decade, various design techniques have been proposed to increase the soft error reliability of digital circuits. One promising approach is to use an SER-aware placement algorithm instead of a traditional placement algorithm in the physical design process. On the other hand, the process variations have a remarkable impact on SER [13] because of exponential dependence of SER on process parameters [14]. Process variations can be decomposed into two categories [14]: within-die (WID) and die-to-die (D2D) variations. WID variations model the variations within a die and D2D variations model the variations on identical cells of a circuit on various dies. The WID variations greatly affect the vulnerability of a cell against soft errors [15], and thus SER of the circuit. And the effects of WID variations on process parameters of a cell is identified after performing the placement process (note that D2D variations affect all cells of a circuit in the same manner and hence, it does not change the vulnerable cells). Therefore, an important question naturally arises: how important is it to consider the effects of WID variations while trying to find a SER-aware placement for a circuit?

In this paper, we propose SeaPlace, a WID process variation-aware and soft error aware placement methodology. The goal of SeaPlace is to use WID variation information in placement algorithms to improve the soft error reliability of combinational circuits against both SETs and METs. To the best of our knowledge, this is the first work that models and exploits WID variation information in SER-aware placement algorithms.

We first show that the effect of WID process variations on the circuit SER is significantly affected by the placement of circuit cells. Our experiments on some random placement algorithms reveal that neglecting WID variations in placement algorithms can easily miss the
The main contributions of this paper are as follows:

1) A novel WID variation-aware placement methodology called SeaPlace to improve soft error reliability against both SETs and METs including two consistent algorithms for global and detailed placement.

2) A fast SER-aware global placement algorithm based on quadratic programming for improving soft error reliability against SETs in the presence of WID variations.

3) A novel SER-aware detailed placement algorithm considering WID variations for hardening against METs.

The remainder of the paper is organized as follows: Section II provides an overview of the related work. Section III motivates the consideration of WID variations in placements aimed for soft error reliability improvement. Sections IV, V and VI explain placement methodology and the proposed algorithms SeaPlace-G and SeaPlace-D, respectively. Experimental results are presented in Section VII. Finally, the conclusion is given in Section VIII.

II. RELATED WORK

Various types of design techniques, with the aim of reducing the circuit SER, have been proposed during the recent decades. Adding hardware redundancy, gate sizing, increasing load capacitance and using error correcting codes are some of these conventional techniques [16]–[22]. In recent years, soft error-aware placement process is introduced as a promising technique to decrease the circuit SER [13], [23]–[32].

For SETs (or SEUs), in [30], a soft error reliability aware placement algorithm is presented to increase the reliability of designs to be mapped into SRAM-based FPGAs against SEUs. It modifies the placement algorithm in the VPR tool-set [31], [32] by adding reliability constraints to the cost function of simulated annealing-based placement algorithm of the tool. In [23], it is stated that the masking probability of SETs generated between nearby cells with high sensitivity is high. As a result, after computing cells sensitivity information, some placement constraints are produced as bounding commands of placement design tools to place highly sensitive cells in a close proximity. Although this method takes advantage of design automation tools, it is not performed automatically and it does not have enough flexibility.

For METs (or MUBs), in [24], via calculation of pass/fail value for all possible pairs of the circuit, all pairs are decomposed into two sets: good pairs and bad pairs. A simulated annealing-based optimization is then accomplished for maximizing the elements of good pairs set. As shown by the result, the runtime is increased greatly with the increase in circuit size. The method is not scalable and cannot be applied to large circuits. In methods presented in [25] and [26], the low-pass filtering behavior of long nets is focused and it is shown that enlarging the interconnections can result in SER reduction in combinational circuit. However, these approaches negatively affect the total wirelength and the circuit delay. In [27], a post-placement approach is used to redistribute white spaces for increasing the distance between most vulnerable adjacent cells and subsequently reducing the circuit SER. There are some works that take advantage of pulse quenching effect in which simultaneous charge collection on nearby nodes of a circuit can cause to shorten or quench a radiation induced transient pulse [28]. In [13], the introduced placement approach tries to increase the number of quenching units and also make them physically closer to decrease the soft error susceptibility. In [29], the authors proposed a detailed placement in which the distance between quenching units is reduced to increase the pulse quenching effect and decrease the circuit SER.

Although these prior studies have achieved considerable soft error reliability improvement for the circuits, they have overlooked one or two major issues:

1) Most of them only consider SETs ([23], [25], [26]) or METs ([24], [27]) and do not cover all transient faults originated by both SETs and METs. It should be noted that most of the methods proposed for hardening against METs cannot be simplified to handle SETs because having multiple error sites and using their interactions is their main assumption. As the occurrence probability of METs and SETs for technologies below 50 nm is equal [12], neglecting one of them will result in ineffective soft error reliability improvement.

2) None of the previous studies addressed the effect of process variations. Cell locations due to WID variations quietly affect the circuit SER [14]. Therefore, considering the effects of WID variations during an SER-aware placement is of great importance. Based on our characterization results which will be presented in Section III, omitting WID variations in SER-aware placements can easily lead to inefficient SER reduction by more than 30%.

III. MOTIVATION: IMPACT OF WID PROCESS VARIATIONS ON SER

WID variations impose a spatial correlation and also a random behavior to gates on different locations across
the die [14], which affects gates vulnerability against generation and propagation of transient pulses generated by particle strikes [15]. WID process variations can affect SER significantly: as it is shown in [15], it can result in \(-33.5\%\) to \(81.7\%\) variations for transistor critical charge (\(Q_{\text{critical}}\)).

In this section, we characterize the effects of WID process variations during an SER-aware placement. For illustration purpose, we estimate the SER of a few random placements for representative combinational circuits from the ISCAS’85 benchmark suite. The technology cells are 45nm Nangate [33] and the WID variations are imposed to \(V_{\text{th}}\) parameter (WID variation model will be described in Section VII).

The effects of WID variations on SER reduction is depicted in Figure 1. In this figure, for each combinational circuit of the ISCAS’85 benchmark suite, seven random placements are performed and a placement with minimum SER is considered as the base SER. Then, the SER values of the remaining placements are normalized with respect to the base SER. As shown in Figure 1, WID process variations have a great impact on SER values of different placements of a circuit, which can result in up to 36% variations in the estimation of circuit SER. Therefore, ignoring WID process variations in SER-aware placements may lead to inaccuracy in SER reduction of combinational circuits.

IV. SeaPlace: WID Variation-Aware and Soft Error-Aware Placement

Placement is an important step during the chip physical design in which the exact geometrical location of the logic cells are determined with the aim of minimizing an objective function, usually the total wirelength. Reducing the wirelength generally increases the routability and performance of the circuit [34]. In order to increase the circuit reliability, SER metrics can also be considered in the cost function of the placement.

Placement procedure typically includes two stages, i.e., global and detailed placements. Global placement distributes the cells over the placement region to optimize some objectives. The aim of global placement is to maintain a global view of placement and it focuses its attention on the cell positions globally. Because of this, global placement makes some geometrical approximations in order to simplify the placement problem and neglects some local concerns. Detailed placement takes a placement as its input and tries to improve the solution quality. Detailed placement is more bounded than global placement, because it transforms one legal placement solution into another while optimizing the objectives [35]. Detailed placement usually is performed for improving wirelength, timing and density of the layout.

In order to introduce a process variation-aware and soft error reliability-aware placement method that hardens the circuit against both SETs and METs, some considerations and limitations should be taken in advance:

- First, in order to perform hardening against METs, information of neighbor cells should be taken into account. Adding this information to the global placement step increases its complexity and runtime, as the global placement inherently does not focus on the locality and the neighbors of each cell.
- Second, it is not efficient to consider both SETs and METs in the detailed placement. The reason is that, the detailed placement has not enough degree of freedom to improve vulnerability against both SETs and METs efficiently, due to the constraints applied to the detail placement.

Therefore, in this work, we consider SETs in the global placement and METs in the detail placement step. Although SETs and METs are considered in separate placement phases, mechanisms are provided such that the two phases do not negatively affect each other. The flow of our proposed SeaPlace framework is presented in Figure 2. This framework receives a synthesized netlist as an input and generates a soft error-aware placement. In the first phase of the framework, region classification and cell classification are performed. Then, our proposed SET-aware global placement, SeaPlace-G, is accomplished using the input netlist and the prepared information, including variation map and R-map, in the first phase. Afterwards, our MET-aware detailed placement, SeaPlace-D, is performed receiving SeaPlace-G output and some of first phase outputs (such as SER estimation results). In the following sections, we will explain our introduced flow in detail.
V. SeaPlace-G: A Variation-Aware and SET-Aware Global Placement Algorithm

The placement is an NP-complete problem and should be solved heuristically [34]. Analytical algorithms based on Quadratic Programming (QP) optimization (also called quadratic placements) are very popular because they are quite efficient while presenting good quality of results [34]. In this section, we present SeaPlace-G, a WID variation-aware and SET-aware quadratic global placement algorithm to increase soft error reliability. The overall flow of SeaPlace-G is shown in Figure 3. The algorithm receives an R-map extracted from variation map, a synthesized netlist and a set of sensitive cells as inputs. Constraints and objectives of the optimization are formulated in the next phase. Then, a QP optimization approach is performed to achieve the final placement.

A. Quadratic Placement Formulation

A Quadratic placement solves a minimization problem where its objective function is the sum of weighted squared distance of connected cells, i.e.,
\[
\phi = \frac{1}{2} \sum_{(a,b) \in C} w_{ab} \left[ (a_x - b_x)^2 + (a_y - b_y)^2 \right]
\]
(1)

where C is the set of all connected cells, a and b are two connected cells, \(a_x\) and \(a_y\) are coordinates of cell a and \(w_{ab}\) is the weight of the connection between a and b. In Traditional area-driven and time-driven placements, \(w_{ab}\) is defined as the wirelength and a function of timing criticality of the net connecting cell a and b, respectively.

To have a variation-aware quadratic placement to reduce SER, defining \(w_{ab}\) as a function of an SER metric. This metric should be able to estimate the contribution of each cell to the total SER of the circuit. There are some SER metrics in the literature, but we choose PVW [4] [36], as its results are quite close to Monte Carlo results and its computation time is very low.

Eq. 1 can be decomposed into \(\phi = \phi_x + \phi_y\). So we narrow our analysis to the part that belongs to x coordinates. \(\phi_x\) can be written in the following form:

\[
\phi(x) = \frac{1}{2} x^T Q_x x + C_x x + \text{constant}
\]
(2)

where \(x\) is the vector of x-coordinates of all cells, and \(Q_x\) and \(C_x\) are weighted connectivity matrix denoting connections between movable cells, and connection between movable cells and fixed cells, respectively. Constant value in Eq. 2 is due to the presence of fixed cells such as I/O pins.

Using the approach of GORDIAN algorithm [37], our algorithm includes successive phases of optimization and bipartitioning. After the lth phase of bipartitioning, center of gravity constraints of each sub-region is generated as:

\[
A^{(l)} x = u^{(l)}
\]
(3)

where \(u^{(l)}\) is a vector containing center of gravity coordinates of sub-regions and \(A^{(l)}\) is a matrix constructed as:

\[
\begin{cases}
\sum_{a \in M_p} area_a & \text{if } u \in M_p \\
0 & \text{Otherwise}
\end{cases}
\]
(4)

where \(area_u\) is the area of cell u and \(M_p\) is a set of cells belong to the region p.

After construction of the constraints, the following quadratic optimization is formed. It is proved that this optimization is convex and has a global minimum [37].

\[
\min \left\{ \phi(x) = \frac{1}{2} x^T Q_x x + C_x x \mid A^{(l)} x = u^{(l)} \right\}
\]
(5)

After solving the optimization and sorting the cells based on x-coordinates, bipartitioning is carried out and then new constraints are generated. In the next phases, the bipartitioning process is repeated by alternating between sorting in horizontal (x-coordinates) and vertical (y-coordinates) directions. This consecutive QP optimization and bipartitioning is performed until each region contains an individual cell.

B. Adding the Effects of WID Variations

As mentioned earlier, WID variation information is not considered directly in the objective function of our QP placement. Rather, we present a sensitivity-based technique for efficient use of WID variations information which tries to avoid placing sensitive cells to soft errors, at some regions of the die, using WID variation map.

In this work, we use the VARIUS framework [38] to apply WID variations to process parameters of circuits. In this framework it is supposed that the chip is partitioned into N×N rectangular segments with the same dimensions. In each segment, the process parameter is modeled as...
a random variable with normal distribution having zero mean and a standard deviation of \( \sigma_{sys} \). VARIUS models the systematic variations with a multivariate normal distribution and uses a spherical structure for modeling the spatial correlation. Its function of correlation is dependent on Euclidean distance between segments.

Channel length (\( L_{eff} \)) and threshold voltage (\( V_{th} \)) are two process parameters that are typically considered to be affected by WID variations. In the model of VARIUS [38], the relation between these two parameters is modelled as:

\[
L_{eff} = L_{eff}^0 \left(1 + \frac{V_{th} - V_{th}^n}{2V_{th}^n}\right)
\] (6)

where \( L_{eff}^0 \) and \( V_{th}^n \) are nominal values of \( L_{eff} \) and \( V_{th} \), respectively. As a result, we only consider the variations in \( V_{th} \) in our work, as \( L_{eff} \) can be calculated using Eq. 6.

The extracted variation map of \( V_{th} \) has \( N \times N \) fragments where each fragment has a value of \( V_{th} \) and \( V_{th} \) values of cells placed at a fragment are equal to that of the fragment. Variations in \( V_{th} \) values of cells lead to changes in their delays which can greatly affect the amount of electrical masking and subsequently the circuit SER.

As values of \( V_{th} \) and \( L_{eff} \) of gates are dependent on their locations due to the WID variations, calculating the gate propagation delay is not straightforward. We all know that the delay of a gate can be calculated as follows:

\[
Delay_g = T_{INV} (LE_g + FO_g + P_g)
\] (7)

where \( T_{INV} \) is the intrinsic delay of an inverter, \( LE_g \), \( FO_g \) and \( P_g \) are logical effort, electrical effort and parasitic delay of a gate \( g \), respectively. The high dependency of \( T_{INV} \) on \( V_{th} \) can be explained by the well-known alpha-power law [39]:

\[
T_{INV} \propto \frac{L_{eff} V_{DD}}{(V_{DD} - V_{th})^\alpha}
\] (8)

where \( \alpha \) is a constant which is dependent on process technology. Substituting Eq. 6 and Eq. 8 into Eq. 10, following equations can be derived:

\[
T_{INV} \propto \frac{V_{DD} (1 + \frac{V_{th}}{V_{th}^n})}{(V_{DD} - V_{th})^\alpha}
\] (9)

\[
Delay_g \propto \frac{V_{DD} (1 + \frac{V_{th}}{V_{th}^n})}{(V_{DD} - V_{th})^\alpha} (LE_g + FO_g + P_g)
\] (10)

The increase in delay of a gate leads to the increase of electrical masking of the gate, based on the electrical masking modeling of PVW [4] [36]. So, in order to decrease the circuit SER, cells should be placed with an approach that results in increase of circuit electrical masking. It can be empirically observed that Eq. 9 has a quite linear behavior with respect to \( V_{th} \) in the parameter range of interest. Therefore, placing cells in regions with high \( V_{th} \) (HVT regions) reduce the circuit SER. To put it differently, for the sake of circuit SER reduction, placing cells in low \( V_{th} \) regions (LVT regions) should be preferably avoided.

However, this is not a feasible strategy for all cells because the die area is bounded and not all cells can be placed in HVT regions. Moreover, placing some cells in HVT regions should be carried out carefully, as it may negatively affect the critical path and the circuit delay. Therefore, we restrict this approach to sensitive cells to transient pulses.

Our aforementioned strategy includes three steps. First, sensitive cells to SER are identified. Second, chip fragments are classified with respect to the value of \( V_{th} \). Finally, the QP equations applying the placement strategy are generated.

1) Sensitive Cell Classification: Identifying sensitive cells to transient pulses needs an SER metric which has the ability to estimate the relative SER contribution of each individual cell to the circuit SER. In this regard, we choose the PVW model [4] [36] as an SER metric and use Eq. 11 for finding sensitive cells to soft errors.

\[
SER_A \leq \frac{SER_{ckt}}{number\ of\ cells} \rightarrow A \text{ is sensitive. (11)}
\]

where \( SER_{ckt} \) is the total circuit SER and \( SER_A \) is the individual SER of cell A.

2) Region Classification: Performing our placement strategy needs two sets of chip fragments classified with respect to the \( V_{th} \) value extracted from the variation map. Table I presents the empirically obtained criteria of chip regions classification in which \( \mu_{V_{th}} \) and \( \sigma_{V_{th}} \) are the mean and the standard deviation of \( V_{th} \) used for constructing variation map, respectively.

| Nominal Value | HVT region | LVT region |
|---------------|------------|------------|
| \( V_{th} \)  | 220 mv     | \( \mu_{V_{th}} + 1.3\sigma_{V_{th}} < V_{th} \) | \( \mu_{V_{th}} + 1.3\sigma_{V_{th}} \geq V_{th} \) |

By applying the definition presented in Table I to the variation map of the chip, we can generate a map named as LH-map. Due to the spatial correlation, there are many regions in the map in which adjacent fragments are in the same class. To simplify the formulating of our placement strategy used for considering WID variations, adjacent fragments belonging to the same class are merged leading to creation of some LVT and HVT blocks. We deploy rectangular map (R-map) [40] to address this issue. We consider LH-map as a binary matrix in which LVT and HVT fragments are denoted by 0 and 1, respectively, to obtain R-map representations. Giving this binary matrix as an input to R-map, it traverses the matrix and merges adjacent 0 and 1 to create maximal blocks of 0 and 1 [40]. The constructed variation map and its equivalent R-map is shown in Figure 4.

3) Optimization Formulation: Forming the optimization can be performed after classifying regions and cells. As mentioned previously, the algorithm should apply the placement strategy in which placing sensitive cells in LVT regions is preferably avoided. To this end, a penalty-based approach is used in which placing sensitive cells in LVT regions results in adding penalties to the objective function. Actually, using this approach the algorithm tries...
to make trade-off between decreasing the circuit SER by not placing sensitive cells in LVT regions and reducing the total wirelength by placing sensitive cells in nearby LVT regions.

To formulate the proposed placement strategy, let \( V \) and \( B \) be the sets of all cells and all LVT blocks, respectively. We assume that the set \( V \) is partitioned into two subsets \( V_S \) and \( V_{NS} \), respectively including sensitive cells and other cells. Eq. 12 presents the proposed objective function in which the second sigma sign is for calculation of imposed penalties caused by placing sensitive cells in LVT blocks.

\[
\phi = \frac{1}{2} \sum_{(m,n) \in V} (1 - \text{SER}_m')( (x_m - x_n)^2 + (y_m - y_n)^2 ) + \sum_{i \in V_S \text{ and } j \in B} \delta_{ij} \times e^{(\text{SER}_i' + 1)^K} \tag{12}
\]

where \( \text{SER}_m' \) is the normalized SER of cell \( m \) (SER of all circuit cells are normalized between 0 to 1), \( \delta_{ij} \) parameter is for identifying whether cell \( v_i \) is placed at LVT block \( b_j \) or not, and \( K \) is a constant parameter used for controlling the amount of penalties which is obtained after extensive experiments.

\[
\delta_{ij} = \begin{cases} 
1 & \text{if } v_i \text{ is placed in } b_j \\
0 & \text{if } v_i \text{ is not placed in } b_j 
\end{cases} \tag{13}
\]

Eq. 14 defines an LVT block \( b_j \) in which \( l_{x_j} \) and \( u_{x_j} \) are its lower and upper bounds in x-axis and \( l_{y_j} \) and \( u_{y_j} \) are the same for y-axis.

\[
b_j = \{(x,y) \mid l_{x_j} \leq x \leq u_{x_j} \text{ and } l_{y_j} \leq y \leq u_{y_j}\} \tag{14}
\]

Supposing \( v_i \) as a cell with \((x_i, y_i)\) coordinates, for modeling the proposed placement strategy the following condition should be satisfied: \( \delta_{ij} = 1 \), if and only if the cell \( v_i \) is placed at block \( b_j \); otherwise, \( \delta_{ij} = 0 \).

We introduce Eq. 15 in order to present constraints for modeling the aforementioned condition for \( x_i \) in which \( \delta_{ij}^1, \delta_{ij}^2 \) and \( \delta_{ij}^3 \) are temporary binary variables and \( M \) has a value greater than the maximum value of \( x \) and \( y \) coordinates of the chip. Generated constraints of \( y_i \) are the same.

\[
\begin{align*}
-M(1 - \delta_{ij}^1) + l_{x_j} & \leq x_i < l_{x_j} + M\delta_{ij}^1 \\
-M\delta_{ij}^2 + u_{x_j} & < x_i \leq u_{x_j} + M(1 - \delta_{ij}^2) \\
0 & \leq \delta_{ij}^1 + \delta_{ij}^2 - 2\delta_{ij}^3 \leq 1 \\
1 & - M(1 - \delta_{ij}^3) \leq \delta_{ij} \leq 1 + M(1 - \delta_{ij}^3) \\
-M\delta_{ij}^3 & \leq \delta_{ij} \leq M\delta_{ij}^3 \\
\forall i \in V_S, \forall j \in B
\end{align*} \tag{15}
\]

These constraints are generated for all LVT blocks, however some of these LVT blocks may be single and scattered as shown in Figure 4. It was observed that generating aforementioned constraints for these scattered blocks increases the algorithm complexity and the total wirelength overhead of the placement in most cases. Therefore, prior to generating constraints, some single and scattered LVT blocks are omitted and a few of HVT blocks, which partitioned big LVT blocks into small blocks, are counted as LVT blocks. Putting all these together, the pseudo code of our SeaPlace-G algorithm is shown in Algorithm 1.

VI. SeaPlace-D: A Variation-Aware and MET-Aware Detailed Placement Algorithm

In this section we introduce a detailed placement that is hardened against METs and shown in Figure 5. This algorithm receives sensitive cells and placed netlist generated by SeaPlace-G placement. In the first phase of the algorithm, a set of pair candidates for moving are constructed. This set is named as Candidate Move SET
As was shown in [27], if a particle strike affects two adjacent cells, their propagated errors may mask each other. The reason is that transient pulses generated by the strike may reach to a gate and cancel out each other. As a result, if a particle strike affects these two cells, their errors can propagate independently. So the total failure probability that a strike affects A and B is:

\[ FP_{A,B}^{\text{ind}} = FP_A + FP_B - FP_{A,B} = FP_A + FP_B - FP_{A}FP_{B} \]  

(16)

where \( FP_A \) and \( FP_B \) are the failure probabilities caused by affecting A and B. As \( FP_A \) and \( FP_B \) are independent, their intersection is equal to their product. We denote this probability with \( FP_{A,B}^{\text{ind}} \) in the rest of this paper and refer to it as the joint independent failure probability.

As shown in Figure 6, cells A and C are not independent, as they share some gates in their forward cones. We denote the failure probability of two dependent cells like A and C with \( FP_{A,C} \) and name it as the joint failure probability (JFP) which is calculated using the method in [41]. As the propagated errors from two affected cells may meet each other, their JFP may be changed. If two transient pulses, originated from two error sites, reach to a gate, their interaction can result in weaker or stronger pulses. So, depending on the circuit structure, having intersection between forward cones of error sites may or may not cause lower JFP. It is shown that the occurrence of this pulse shrinking, known as pulse quenching effect, is closely relevant to electrical relationship between physically adjacent cells and their distances [28]. Hence, identifying electrically related cells that can have such error propagation behaviors and making them physically closer, can be advantageous to mitigate MET SER. We call these cells as candidate pairs (CAP) and a set of all CAPs as CMS.

Reducing the distance between cells of each CAP to use their possible quenching effects should be done with respect to the patterns of MET occurrence. In this regard, the cells should be located in a distance in which hitting a particle to one of them can affect the other one. Similar to [27], we use an oval shape as the shape of the affected area for MET occurrence. Hence, to have a CAP, the two cells should be at a distance where cells can be fitted in the oval. The maximum amount of this distance is called as masking distance. In this paper, we only consider the horizontal distance as a masking distance, as the existence of VDD or GND trail between two consecutive rows leads to vertical distances bigger than the masking distance according to our experiments. In the following we explain our placement strategy.

A. Multiple Event Transient Model

Generally, our placement identifies some specific pairs of cells and tries to decrease the distance between cells of each pair. In this work, we only consider double event transients (DETs) because the probability of occurring more than two transient faults in the target technology of this work (45 nm) is about five percent [27].

As it was shown in [27], if a particle strike affects two adjacent cells, their propagated errors may mask each other. The reason is that transient pulses generated by the strike may reach to a gate and cancel out each other. Figure 6 shows an example. In this figure cells A and B are independent, i.e., they share no gates in their forward cones. As a result, if a particle strike affects these two cells, their errors can propagate independently. So the total failure probability of all possible pairs should be calculated in the first step. Calculation of JFP for all possible pairs of a circuit has a time complexity of order \( O(n^2) \) that is very time consuming for large circuits. In order to facilitate this calculation, we narrowed the search for CAPs to sensitive cells to transient pulses. More precisely, each sensitive cell \( c \) and the cells connected to its input and output pins are used to build our new search space. The reason of considering cells connected to each sensitive cell is that the expected pulse quenching
Before action | Move 1 | Move 2
---|---|---
(a) Before action | Before action | Move 1 | Move 2

![Diagram](image)

**Fig. 7. Examples of transfer (a-c) and swap (d-f) actions. Note that move 1 and 2 in this figure (and all following figures) are two different move options applied to the original cells; they are not applied on top of each other.**

is more probable especially for cells that have fan-in and fan-out relationships [28], [42]. After calculating JFP for each connected pair (A-B) of our search space, we compare \( FP_{(A-B)} \) and \( FP_{ind}^{(A-B)} \). If the former is less than the latter, A and B form a CAP, i.e.:

\[
FP_{(A-B)} < FP_{ind}^{(A-B)} \iff (A - B) \in CPS \tag{17}
\]

**C. Sensitive Cell Identification**

To identify sensitive cells to transient pulses, we apply the Eq. 11, which is the same process as discussed in Section V-B1.

**D. Sensitive Cell Transfer and Swap**

After identifying CAPs, we intend to make them physically closer in the layout to use their masking effects. Our algorithm uses two types of actions to reduce the distance between cells of each CAP that named as transfer and swap. Before going into the details, we propose a \( \Omega \) notation for denoting different types of actions. The superscript of \( \Omega \) operator is used to write cells of a pair with their final coordinates after doing the action and the subscript is for mentioning the cells supposed to move with their coordinates before doing the action.

The transfer and swap actions place the cells of each CAP at a distance less than the masking distance. Figure 7a shows two cells of a CAP placed at separate rows. Reducing the distance between these two cells can be done in two different moves as shown in the Figure 7b and Figure 7c. Moves 1 and 2 (called transfers in this case) are formulated by Eq. 18 and Eq. 19, respectively:

\[
\Omega_{c_x^i,c_y^j \rightarrow c_x^{i+1},c_y^{j+1}}^{m,n} \left( c_{x}^{m,n},c_{y}^{m,n+1},c_{x}^{m,n+1},c_{y}^{m,n+1} \right) = \left( c_{x}^{m,n},c_{y}^{m,n+1},c_{x}^{m,n},c_{y}^{m,n+1} \right) \tag{18}
\]

\[
\Omega_{c_x^{i-1},c_y^{j-1}}^{m,n} \left( c_{x}^{m,n-1},c_{y}^{m,n-1},c_{x}^{m,n-1},c_{y}^{m,n-1} \right) = \left( c_{x}^{m,n-1},c_{y}^{m,n-1},c_{x}^{m,n-1},c_{y}^{m,n-1} \right) \tag{19}
\]

where \( c_x^i \) and \( c_y^j \) denotes cell \( x \) that is placed at \( (i,j) \) coordinates of the layout grid. As only one cell is moved in a transfer action, the vacant position in \( (i,j+1) \) coordinates in Figure 7a, which is supposed to be filled by cell \( c_x^{m,n+1,j} \), is denoted by \( c_x^{m,n+1,j} \) in Eq. 18.

Swap action is performed in circumstances that it is not possible to place the cells close to each other by using a transfer action. An example is shown in Figure 7d. In this example, placing cells \( x \) and \( y \) at a very close distance is not possible due to the lack of sufficient space around both cells. In this situation, \( x \) and \( y \) swaps their location with that of the neighbor of \( \frac{x}{y} \). These two different moves (called swaps in this case) are shown in Figure 7e and Figure 7f and are described by Eq. 20 and Eq. 21 respectively:

\[
\Omega_{c_x^{i-1},c_y^{j-1}}^{m,n-1} \left( c_{x}^{m,n-1},c_{y}^{m,n-1},c_{x}^{m,n-1},c_{y}^{m,n-1} \right) = \left( c_{x}^{m,n-1},c_{y}^{m,n-1},c_{x}^{m,n-1},c_{y}^{m,n-1} \right) \tag{20}
\]

\[
\Omega_{c_x^{i-1},c_y^{j-1}}^{m,n-1} \left( c_{x}^{m,n-1},c_{y}^{m,n-1},c_{x}^{m,n-1},c_{y}^{m,n-1} \right) = \left( c_{x}^{m,n-1},c_{y}^{m,n-1},c_{x}^{m,n-1},c_{y}^{m,n-1} \right) \tag{21}
\]

As shown in Figure 7, making the cells of a pair closer can be done in different ways. There can be more ways if CAPs share some cells. In Figure 8, cell \( x \) is common between \( (x,y) \) and \( (x,w) \) pairs. In this example, there are four moves that can make cells of a CAP closer. Thus, each transfer or swap action can be performed through different moves and it is up to the algorithm to select one of these moves. A set that contains all possible moves for making cells of each CAP closer is named as Candidate Move Set (CMS).

After forming CMS, we calculate the delta failure probability (\( \Delta FP \)) for all of CMS members. Delta failure probability is a parameter that approximates the amount of changes in the failure probability of a circuit after performing a transfer or a swap action. In order to calculate delta failure probability, we first define Affected Sets (AS). When a change is made to a point of the layout by an action, a pair of cells where their JFP has changed after the action, form a pair that belongs to AS. After performing a transfer or a swap action, two ASes are formed. The ASes of a swap action are depicted in Figure 9. For calculating the delta failure probability, the changes made to the JFP of all members of each AS is calculated. Delta failure probability of Figure 9 is calculated as

\[
\Delta F PA_{c_i - c_j} = \sum_{(r,s) \in (AS_1 \cup \cup AS_2)} FP_{(r-s)}^2 - FP_{(r-s)}^1
\]

\[
= \sum_{(r,s) \in AS_1} FP_{(r-s)}^2 - FP_{(r-s)}^1 + \sum_{(r,s) \in AS_2} FP_{(r-s)}^2 - FP_{(r-s)}^1
\]

\[
= \sum_{r=(c_i, or c_j)} \sum_{s \in AS_1} FP_{(r-s)}^2 - \sum_{t \in AS_2} FP_{(c_j - t)}^2
\]

\[
\sum_{r=(c_i, or c_j)} \sum_{s \in AS_1} \sum_{u \in AS_2} FP_{(c_j - u)}^1
\]

where \( (r,s) \) is a pair, \( A_{c_i - c_j} \) is the \( i \)th move of an action related to cells \( c_i \) and \( c_j \) shown in Figure 9, and \( FP_{(r,s)}^1 \).
Before action

\[ \Delta \text{SER} \left( A_i^{c_1, c_2} \right) = \Delta \text{SER}(c_j) + \Delta \text{SER}(c_q) \]  

(23)

where \( \Delta \text{SER}(c_j) \) is the change made to SER of \( c_j \) due to the change of its location. Wirelength is another constraint that we consider in our algorithm aiming to control the imposed overhead by actions.

\[ \Delta \text{WL} \left( A_i^{c_1, c_2} \right) = \Delta \text{WL}(c_j) + \Delta \text{WL}(c_q) \]  

(24)

where \( \Delta \text{WL}(c_j) \) is the change made to wirelength of \( c_j \) due to the change of its location. Algorithm 2 shows the pseudo-code description of our algorithm for construction of CAPS and CMS. The algorithm has a linear time complexity of \( O(n) \).

Algorithm 2. The algorithm for construction of CMS

1. \( n \): Number of layout rows
2. \( G \): The grid of layout
3. SCS: Set of sensitive cells to transient pulses
4. CAPS : Set of CAPs
5. CMS: Set of all possible moves for all CAPS members
6. CS(i): Set of cells connected to cell \( i \)
7. Outputs: CAPS, CMS
8. \( \text{for each cell } c_j \text{ in } \text{SCS do} \)
9. \( \text{for each cell } c_j \text{ in } \text{CS} \) (\( c_i, c_2 \)) \( \text{do} \)
10. \( \text{if } FP_{c_1, c_2} < FP_{c_1, c_2}^{\text{ind}} \text{ then} \)
11. \( \text{CAPS.add } ( (c_1, c_2) ) \)
12. \( \text{end if} \)
13. \( \text{save } FP_{c_1, c_2} \)
14. \( \text{end for} \)
15. \( \text{end for} \)
16. \( \text{for each pair } (c_1, c_2) \text{ in } \text{CAPS do} \)
17. \( \text{ActionSet = findActions } (c_1, c_2) \)
18. \( \text{for each action } A_i \text{ in } \text{ActionSet} \text{ then} \)
19. \( \text{fp = calculate } \Delta FP(A_i^{c_1, c_2}) \)
20. \( \text{ser = calculate } \Delta \text{SER}(A_i^{c_1, c_2}) \)
21. \( \text{wl = calculate } \Delta \text{WL}(A_i^{c_1, c_2}) \)
22. \( \text{end for} \)
23. \( \text{CMS.add } ( (c_1, c_2, \text{fp, ser, wl}) ) \)
24. \( \text{end for} \)

E. Placement Algorithm

After calculating overhead and reliability related parameters for each move, we can apply an algorithm for performing the moves. During our experiments, we observed that performing the moves with negative and high delta failure probability increases the chance of pulse quenching effect and results in a considerable total failure probability reduction for the circuit. To this end, we perform an optimization over CMS. We propose an LP optimization that maximize the sum of delta failure probability of moves for the solution, while imposing some constraints to the delta SER and delta wirelength of the circuit. \( \text{SER}_{\text{total}} \) and \( \text{WL}_{\text{total}} \) are the total amounts of SER and wirelength of the circuit obtained before performing the optimization and \( \Delta \text{SER} \) and \( \Delta \text{WL} \) are the maximum allowed percentage of change in SER and wirelength respectively. To formulate the optimization, we suppose that CAPS has \( n \) elements and each element (each CAP) can be performed by at most \( m \) moves. In the following equations, \( \delta_{ij} \) is a temporary binary parameter used to specify actions which
can be done by checking the triple condition for each move.

There should be satisfied in consistency condition, called as Triple Condition. This the solution set, the consistency between the move and
d) physically closer. As a result, before doing a move of
pair (pair (b-d)) has been moved to another location by
because in both examples the fix cell (cell b) of A2 related
perform the action A2. But performing A2 is not effective,
and 10b. Both examples (Case 1 and Case 2) include two
between the solution moves are depicted in Figures 10a
it depends on previously performed moves of the solution
interested to perform all moves of the solution set. This
lution set of moves is obtained. However, we may not be
with previously performed moves.
condition starting from the move with maximum amount
optimization solution based on the delta failure probabil-
For example, the consistency verifying of Figure 10a is as
Because none of the cells in superscript of \( \Omega \) exist in
the operand set of \( \Omega \). After checking triple condition for
all moves of the solution set, some moves may not be
consistent with performed moves. So, a part of the solution
set is not usable and it will be worse when a considerable
part of the solution set is inconsistent with performed
moves. To resolve this challenge, we sort the moves of
optimization solution based on the delta failure probability.
We then perform the moves that satisfied the triple
condition starting from the move with maximum amount
of delta failure probability. Cells that are not consistent
with already performed actions are saved and are treated
as a new CAPS in the next iteration of algorithm.

The pseudo-code of our proposed detail placement al-
gorithm is presented in Algorithm 3. The notMoved set
is initialized by CAPS in the beginning of the algorithm
and then inconsistent cells are added to it during the main
loop of algorithm. As mentioned earlier, the optimization
algorithm may be executed in several iterations, because of
inconsistent moves. At the end of each iteration, the max
allowed overheads are updated for the next iteration. The
refine method in line 20 is responsible for terminating the
algorithm execution by modifying notMovedSet in cases
such as reaching the max allowed overhead and avoiding
non-convergence.

**Algorithm 3. SeaPlace-D, A Detail Placement Algorithm**

1. CAPS : Set of CAPs
2. CMS: Set of all possible moves for all CAPS members
3. toMoveSet : Set of all possible moves for all CAPS members
4. movedSet : Set of actions that are already performed
5. notMovedSet : Set of actions that are not performed
6. notMovedSet = construct_CMS()
7. while (notMovedSet is not empty) do
8. toMoveSet = optimize (notMovedSet )
9. sort toMoveSet based on \( \Delta FP \)
10. for each move M in toMoveSet do
11. if M is consistent with movedSet then
12. Perform move M
13. add A to movedSet
14. remove M from toMovedSet
15. remove M from notMovedSet
16. else
17. remove A from toMovedSet
18. end
19. end for
20. refine (notMovedSet)
21. end while

By solving the optimization problem in Eq. 25, a solu-
tion set of moves is obtained. However, we may not be
interested to perform all moves of the solution set. This
is because of an inconsistency between elements of the
solution set. Indeed, doing a move is not independent and
it depends on previously performed moves of the solution
set. So, performing a move is beneficial, if suitable cir-

Fig. 10. Examples of inconsistency between moves

are present in the solution set.

\[
min \left\{ \sum_{i=1}^{n} \sum_{j=1}^{m} \delta_{ij} \times \Delta FP \left( A_{j}^{Pair(c_{p},c_{q})} \right) \right\}
\]

Subject to:

\[
\forall i, 1 \leq i \leq n, \sum_{j=1}^{m} \delta_{ij} = 1
\]

\[
\forall j, 1 \leq j \leq n, \sum_{i=1}^{m} \delta_{ij} = 1
\]

\[
\delta_{ij} \times \Delta SER \left( A_{j}^{Pair(c_{p},c_{q})} \right) \leq \left( 1 + \Delta SER \right) \times SER_{total}
\]

\[
\delta_{ij} \times \Delta WL \left( A_{j}^{Pair(c_{p},c_{q})} \right) \leq \left( 1 + \Delta WL \right) \times WL_{total}
\]

\[
(25)
\]

\[
(26)
\]

**Triple Condition:** If two cells of subscripts and one of
cells in superscripts of an \( \Omega \) operator exist in its operand
set, the triple condition is met and this move is consistent
with previously performed moves.

\[
(c \in M \land d \in M) \land (a \in M \lor b \in M)
\]

\[
\rightarrow \Omega_{c-a}^{d-b}(M)_{\text{inconsistent}} \tag{27}
\]

Therefore, consistency checking of moves of solution set
can be done by checking the triple condition for each move.

\[
A_{1} = \Omega_{c_{a}^{m,n}-c_{b}^{m,n+1}}^{c_{a}^{m,n}-c_{b}^{m,n+1}} \left( c_{a}^{m,n}, c_{b}^{m,n+1}, c_{a}^{c_{a}^{m,n}}, c_{b}^{c_{b}^{m,n+1}} \right) = \phi
\]

\[
A_{2} = \Omega_{c_{d}^{p,q}-c_{b}^{m,n+1}}^{c_{d}^{p,q}, c_{b}^{m,n+1}} \left( c_{d}^{p,q}, c_{b}^{m,n+1}, c_{d}^{c_{d}^{p,q}}, c_{b}^{c_{b}^{m,n+1}} \right) = \phi
\]

As shown in Eq. 28, action \( A_{2} \) cannot be performed,
because none of the cells in superscript of \( \Omega \) exist in
the operand set of \( \Omega \). After checking triple condition for
all moves of the solution set, some moves may not be
consistent with performed moves. So, a part of the solution
set is not usable and it will be worse when a considerable
part of the solution set is inconsistent with performed
moves. To resolve this challenge, we sort the moves of
optimization solution based on the delta failure probability.
We then perform the moves that satisfied the triple
condition starting from the move with maximum amount
of delta failure probability. Cells that are not consistent
with already performed actions are saved and are treated
as a new CAPS in the next iteration of algorithm.

\[
(28)
\]
VII. EXPERIMENTAL RESULTS

A. Setup

The proposed algorithms are implemented in Java and applied to EPFL [43] benchmark circuits for 45-nm Nanogate technology. All simulations have been run on a Microsoft Windows machine with a Pentium Core i7 (2.1-GHz) processor and a 8-GB RAM.

For constructing a variation map of $V_{th}$, we assume that the chip is partitioned into a $N \times N$ grid and run VARIUS with $\mu = 0.22$ [44], $3\sigma = 55\%$ [44], $N = 300$ and correlation distance $\phi = 0.5$. The result is a variation map of systematic component of $V_{th}$. In this work, it is supposed that systematic and random components of $\sigma(V_{th})$ are equal; that is $\sigma_{sys} = \sigma_{rand} = \frac{\sigma}{\sqrt{2}}$ [45]. We then generate a $N \times N$ matrix of samples from a zero-mean normal distribution with $\sigma_{rand}(V_{th})$. The final $V_{th}$ map is constructed by superposing systematic and random maps segment by segment.

The controlling parameters of Plcae-G and SeaPlace-D (Eq. 26 and Eq. 12) were set as: $K = 2.5$, $\Delta SER= 0.1$ and $\Delta WL= 0.1$. To estimate SET-originated SER the method presented in [36] is used as its accuracy is close to the Monte Carlo results and has a low runtime. We use the method introduced in [27] for evaluating the achieved hardening against METs.

B. SER Reduction and Failure Probability Mitigation

In this section, we evaluate the amount of failure probability mitigation achieved by our algorithms. Figure 11 shows the failure probability reduction for two cases. In the case denoted by SeaPlace-G→SeaPlace-D, SeaPlace-G and subsequently SeaPlace-D are applied to circuits while the other case reports the results of applying only SeaPlace-D. The results show that applying SeaPlace-D after an SeaPlace-G averagely results in about 53% reduction in the failure probability while using only SeaPlace-D achieves about 32% failure probability reduction, on average. This experiment indicates the efficiency of applying SeaPlace-G prior to SeaPlace-D on hardening against METs. Actually, performing SeaPlace-G not only reduces the amount of SET-originated SER, but also results in more significant failure probability reduction achieved by subsequent SeaPlace-D because of increasing the masking effects.

C. Comparison to the State-of-the-art Studies

To assess the efficiency of SeaPlace-G algorithm, its results is compared with an SET-aware quadratic placement referred as QSP [26], which, as the best we know, is the sole SET-aware global placement in the literature considered three factors of transient fault masking (logical, electrical and timing masking).

Figure 12 presents the results of SeaPlace-G and QSP in terms of SET-originated SER reduction, delay and wirelength overheads. In this experiment, both aforementioned algorithms are compared with the wirelength optimized placement which is obtained using SOC Encounter [46]. As show in Figure 12, the average percentage of SER reduction achieved by SeaPlace-G (41.78%) is greater than that of QSP (30.74%) and this observation holds for all studied circuits. This is because, SeaPlace-G uses WID variation map information resulting in finding placements with lower SER. Moreover, delay and wirelength overheads of using SeaPlace-G is less than that of QSP for all circuits.
This is due to the fact that QSP algorithm increases the length of nets for the sake of using low-pass filtering nature of long nets. Although this approach may lead to SER reduction, it but imposes high delay and wirelength overheads.

To investigate the efficiency of our SeaPlace-D algorithm, we compare its results with [27] which presents an SER aware detail placement referred as MTAP. In MTAP, the location of cells within each row is adjusted by redistribution the existing whitespaces without changing the order of cells in each row.

Figure 13 illustrates the failure probability reduction for different placement combinations. The first two bars are dedicated to the MTAP and SeaPlace-D. The next two bars are hybrid methods in which MTAP and SeaPlace-D are performed after applying SeaPlace-G; i.e., the output placement of SeaPlace-G is used as an initial placement of MTAP and SeaPlace-D. All these four placement combinations use a random initial placement accomplished by SOC Encounter. In each combination, the reported failure probability reduction of each circuit is calculated with respect to the failure probability of initial placement of the combination.

As shown in Figure 13, the SeaPlace-D algorithm averagedly achieves 32.04% failure probability reduction in comparison to the MTAP with a failure probability reduction of 16.42%. The reason of this improvement is that, the proposed SeaPlace-D algorithm considers WID process variation information and also uses more different mechanisms to move the cells across multiple rows.

In Figure 13, it is observed that, the values of failure probability reduction for most of the circuits in SeaPlace-G→MTAP row are lower than their corresponding values in MTAP row. Since the MTAP algorithm redistributes white spaces in each row, it needs lots of whitespaces in each row to be able to adjust the cells’ locations. We observed that, the number of whitespaces in each row is usually reduced after applying SeaPlace-G to the initial placement. As a result, the amount of failure probability reduction for the average and the most of the circuits in SeaPlace-G→MTAP case is fewer than their values in MTAP case. Nevertheless, there are some circuits that, their failure probability reduction values in SeaPlace-G→MTAP row are greater than those of MTAP row. This can be explained by differences in pulse masking ability between these two placement combinations. In other words, SeaPlace-G achieves high amounts of pulse masking and subsequently SET-originated SER reduction for these circuits, as previously presented in Figure 13. So, these circuits have considerable potential to mask MET-based transient pulses, provided their masking characteristics are not negatively affected by MTAP.

Another observation is that, SeaPlace-G→SeaPlace-D combination has the most average failure probability reduction (53.3%) among all combinations. In this combination, SeaPlace-G hardens the circuits against SETs by enhancing three masking effects in them. Also, SeaPlace-D not only focuses on hardening against SETs by increasing the chance of pulse quenching effects, but also puts a constraint on maximum allowed changes in SET-originated SER of the circuits, i.e., ∆SER. Hence, the mechanisms of hardening against SETs positively affect the MET-aware failure probability reduction of circuits.

In order to investigate the effect of ∆SER on failure probability reduction of SeaPlace-D algorithm, an experiment is conducted to compare the achieved failure probability reduction of some circuits while applying different values of ∆SER to each circuit. Figure 14 shows the percent of MET-originated failure probability reduction for some large circuits of EPFL benchmark circuits in which different values of failure probability reduction for each circuit are obtained under multiple values of ∆SER.

As shown in Figure 14, for the cases with a ∆SER
lower than 15%, the average percent of MET failure probability reduction is increased by increase in $\Delta SER$ since further moves are performed, resulting in more pulse quenching effects. Performing even more moves result in more pulse quenching effects, but it may negatively affect the SET-originated SER as the location and subsequently electrical and timing masking factors of moved cells are changed. These changes in pulse masking factors not only change the SET-originated SER but also affect the MET-originated failure probability for the circuits. In Figure 14, MET failure probability reduction for $\Delta SER = 20\%$ is decreased in comparison to $\Delta SER = 15\%$ for all circuits, which is due to a compromise between increasing pulse quenching effects and decreasing masking factors for some cells. Also, the decrease of MET failure probability reduction for Mult and Hyp benchmarks for some amounts of $\Delta SER$ can be explained by this compromise.

D. Runtime Overhead

Figure 15 presents the runtime overheads for SeaPlace-G vs. QSP and SeaPlace-D vs. MTAP. The results show that, the runtime of SeaPlace-G for studied circuits is 26.72% more than the runtime of QSP, averagely; because SeaPlace-G has more complex objective function and additional constraints to consider WID variation information. Also, the execution of SeaPlace-D placement has 28.41% runtime overhead in comparison with MTAP method, that is because of solving some consecutive LP optimizations. It should be mentioned that SeaPlace-G and SeaPlace-D incur acceptable runtime overhead in all circuits, and the maximum amount of runtime overhead for SeaPlace-G and SeaPlace-D is about 47 and 13 minutes, respectively.

VIII. CONCLUSION

In this paper, novel WID process variation-aware placement algorithms for improving soft error reliability of combinational circuit against both SETs and METs are presented. Unlike previous placement-based SER reduction methods, in which the effect of WID process variations on their method is neglected, we modeled and utilized WID variation information in our placement algorithms aimed for increasing soft error reliability. Our algorithms included a global placement called as SeaPlace-G and a detailed placement named as SeaPlace-D. SeaPlace-G was proposed for increasing circuit reliability against SETs and SeaPlace-D was presented for hardening against METs. Experimental results showed that on average, SeaPlace-G achieved 41.78% SER reduction against SETs, SeaPlace-D and SeaPlace-G → SeaPlace-D (SeaPlace-G followed by the SeaPlace-D) reduced the failure probability against METs by 32.04% and 53.3%, respectively.

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