Towards Homomorphic Inference Beyond the Edge

Salonik Resch
resc0059@umn.edu

Zamshed I. Chowdhury
chowh005@umn.edu

Husrev Cilasun
cilas001@umn.edu

Masoud Zabihi
zabih003@umn.edu

Zhengyang Zhao
zhaox526@umn.edu

Jian-Ping Wang
jpwang@umn.edu

Sachin Sapatnekar
sachin@umn.edu

Ulya R. Karpuzcu
ukarpuzc@umn.edu

Abstract—Beyond edge devices can function off the power grid and without batteries, enabling them to operate in difficult to access regions. However, energy costly long-distance communication required for reporting results or offloading computation becomes a limitation. Here, we reduce this overhead by developing a beyond edge device which can effectively act as a nearby server to offload computation. For security reasons, this device must operate on encrypted data, which incurs a high overhead. We use energy-efficient and intermittent-safe in-memory computation to enable this encrypted computation, allowing it to provide a speedup for beyond edge applications within a power budget of a few milliWatts.

I. INTRODUCTION

Devices are now being built which can operate without batteries or other constant power sources [28]. This allows these devices to be deployed in a wide variety of environments, where traditional power sources are typically unavailable. Such environments are referred to as beyond the edge, and can reside inside the structures of buildings [61], in the remote wilderness [28], in outer space [54], inside the human body [32], or simply scattered throughout a city. The extreme deployment capability opens up many new applications.

A significant limitation of these devices, however, is the very strict power budget. Available power sources range from less than 1 µW from RF energy [45], [70], [71], to 60 µW from thermal energy harvesters [43], [60], up to 100 mW per square centimeter from solar panels [19], [21], [31], [37], [43]. Depending on the specific deployment location, devices could be limited to only the weakest power sources. For example, if embedded within the walls of a building, a device will have no access to sunlight and will have to rely on either RF or thermal energy. Hence, beyond edge devices have to operate effectively while consuming minimal power. Energy efficiency determines the performance [28], as typically most time is spent waiting for sufficient energy.

A potential solution to this power limitation is to perform the computation in a remote server, rather than on the device itself. Beyond edge devices can collect sensor data and then send it to a server to be processed, rather than performing computation locally. This can provide a benefit if intense processing is required. Homomorphic encryption can enable the use of untrusted servers, where the device can encrypt data and the server can process the data without decrypting it [21]. However, this data transmission itself can be costly. If the server is a few km away, the cost can be as much as 400 µJ per bit [11]. To send unencrypted data, for example a single sample of the MNIST data set [45] would consume 2.5 J. For encrypted data, for most practical purposes, the smallest homomorphic encryption configuration will consume approximately 400,000 bits [52]. In this case, transmission would cost 160 J, well beyond what is practically obtainable by beyond edge devices.

However, the transmission cost can be significantly reduced if it only needs to travel a short distance. For example, within tens of meters, Bluetooth Low Energy (BLE) can consume as little as 158 pJ per bit [73]. Hence, if the server is extremely close by, offloading computation is still tractable. Still, it is clearly impossible to deploy a typical server within tens of meters of all beyond edge devices. Hence, in this work, we propose a beyond edge accelerator which can serve as a local “mini-server”. If this accelerator can be deployed in a location which has relatively more power available, such as on a rooftop where sunlight can be collected, it can provide an effective means for computational offload.

While this beyond edge accelerator is a trusted device, it introduces new security concerns. As it is deployed beyond edge, in potentially insecure environments, the device itself may be compromised or stolen. In order to maintain security, the accelerator must store and operate on only encrypted data. Otherwise, sensitive information (such as machine learning models), could be compromised. Hence, the accelerator must perform homomorphic computation, which allows data to remain encrypted for the entire process. Unfortunately, this introduces a significant challenge, as homomorphic computation is orders of magnitude slower and more energy costly than standard computation. In this paper we investigate how to avoid much of this overhead with two approaches.

First, we perform only linear operations on the accelerator, such as multiplication and addition, which have a much lower homomorphic overhead (leaving the remaining non-linear operations to be performed on the original device). If most required operations are linear, such as in support vector machine (SVM) inference used in this work, this process remains efficient. Second, we are able to keep the computational depth low, which minimizes the amount of noise. This allows us to avoid the process of bootstrapping, which is the most costly component of homomorphic computation. Despite these advantages, homomorphic computation remains highly energy costly. Consequently, the accelerator must be extremely energy efficient in order to compensate.

An additional challenge of beyond edge deployment is that the accelerator must also be able to tolerate power outages. Checkpointing and guaranteeing correctness has significant overhead for energy efficiency and complexity [53]. We design the accelerator to make use of non-volatile processing-in-memory (PIM), which not only provides high energy efficiency, but inherent resilience to interruptions and low-cost
checkpointing mechanisms [77].

The remainder of the paper is structured as followed. In Section II we define the specific problem this paper addresses and discuss the requirements for a satisfactory solution. We briefly describe homomorphic computation in Section III-A and SVMs in Section III-B. We introduce the memory devices used in the accelerator and describe how we can perform logic with them in Section III-C. The architecture of the accelerator and its operating semantics are covered in Section IV. The evaluation is contained in Section V and a discussion of the limitations of our work is in Section VI. Related work is covered in Section VII and finally we conclude in Section VIII.

II. PROBLEM STATEMENT AND DEFINITIONS

In this section we cover the basic scenario covered and the assumptions made about the problem. We assume that there are three types of devices in play. The FLY (in the wall), the RODENT (on the roof), and the remote TURTLE.

The TURTLE is a distant and secure server in a secure environment with no power restrictions. It is the intended destination for all final results of interest. The FLY is a beyond edge device running on harvested energy. It acquires data with sensors, with the intention of reporting interesting results back to the TURTLE. The FLY also operates beyond the edge and relies on harvested energy. It acquires data with sensors, with the intention of reporting interesting results back to the TURTLE. The FLY is in an concealed environment, where the device itself is secure. Hence, it can operate on secure (un-encrypted) data and has access to a private key. Additionally, due to being in a highly concealed environment (eg. inside a wall), it is limited to RF or thermal energy, which is in the microwatt range [43]. Hence, it must operate under a very low power budget.

The RODENT also operates beyond the edge and relies on harvested energy. However, it is in a less concealed environment and is insecure, the device itself may be taken by an not trusted entity. An advantage of being in a less concealed environment (e.g., on a rooftop), is that it has a higher power budget. For example, it may be able to harvest sunlight, which can provide a power budget of tens of milliwatts [45]. Despite being insecure, RODENT can make use of sensitive information (such as proprietary machine learning models) to process information without introducing security leaks by using encryption. All sensitive data remains encrypted on RODENT at all times. Homomorphic computing [12], [26], covered in Section III-A, enables computation on this encrypted data.

The relative placements of the devices are shown in Figure 1. TURTLE is \(d_{FT}\) meters from FLY, and it takes \(E_{FT}\) \(\mu J\) per bit to transmit from FLY to TURTLE. RODENT is \(d_{FR}\) meters away from FLY and it takes \(E_{FR}\) \(\mu J\) per bit to transmit from FLY to RODENT. In this scenario, \(d_{FT} \gg d_{FR}\) because RODENT can be deployed into similar environments as FLY. Hence, FLY can much more easily communicate with RODENT than with TURTLE.

If the FLY wishes to report back to the TURTLE, it has 3 options.

1. Send all sensor readings to the distant TURTLE. TURTLE will be in charge of all computation.
2. Perform processing (inference) locally and only send TURTLE the meaningful results.
3. Offload processing (inference) to the nearby RODENT and then only send the meaningful results to TURTLE.

This equation almost always holds as long distance communication (beyond 3km) with low-power long-range (LoRa) hardware is relatively energy costly, consuming up to 400 \(\mu J\) per bit [11]. For example, sending data samples (such as an MNIST image sample [45]) would consume \(E_{FT} = 2.5 J\) per sample. Alternatively, the energy required for local inference (with standard beyond edge hardware) is in the range of \(E_F = 27 mJ\) [28]. In this case, local inference will be more efficient if \(\alpha < 98.9\%\). Given results of interest are relatively rare, this is likely to be the case.

Option 3 replaces local inference (consuming \(E_F\) \(\mu J\)) on FLY with

1. (Optional) Encoding and encrypting sensor data (consuming \(E_{encrypt}\))
2. Transmitting data to RODENT
3. Homomorphic inference on RODENT (consuming \(E_R\))
4. Transmission of results back to FLY (consuming \(E_{RF}\))
5. Decrypting results on FLY (consuming \(E_{decrypt}\))

For option 3 to be superior to option 2, the following equation must hold:

\[E_{encrypt} + E_{FR} + E_{RF} + E_{decrypt} < E_F\]  

(2)

In words, it must be more efficient for FLY to transmit to RODENT and receive the results than it is to process the data itself. If the input data collected by FLY is considered sensitive, FLY must encrypt the data before transmission, in order to maintain security in un-trusted environments. \(E_{encrypt}\) and \(E_{decrypt}\) can be done with 0.06 \(mJ\) (using the same parameters as this paper) with specialized hardware for homomorphic encryption on edge devices [91]. If the inputs are not sensitive, then they can be sent as raw data and \(E_{encrypt}\) can be dropped from Equation 2. However,
RODENT will still return encrypted data in order to protect its ML model, hence $E_{\text{decr}}$ is still required. Due to the close proximity of FLY and RODENT (in the order of meters), communication cost is significantly reduced. Technologies such as Bluetooth Low Energy (BLE) can be used, with some configurations offering as little as 158 pJ per bit [78]. At such efficiency, (un)encrypted data can be sent to RODENT ($E_{RF}$) and encrypted results can be transmitted from RODENT to FLY ($E_{RF}$) with less than (1 μJ) 80 μJ. Hence, BLE can provide communication which will cost FLY less energy than local processing. FLY will require both BLE (for communication with RODENT) and LoRa (for communication with the distant TURTLE).

The other condition required for option 3 to be viable is that the homomorphic computation energy on RODENT ($E_{R}$) must be reasonable. While operating beyond edge, RODENT has a higher energy budget than FLY. However, homomorphic computing has a very large overhead that can easily become excessive. RODENT must be sufficiently efficient in order to return results to FLY promptly. For RODENT to provide any benefit, the following equation must hold:

$$\frac{E_{FR}}{P_F} + \frac{E_{R}}{P_R} + \frac{E_{RF}}{P_R} < \frac{E_F}{P_F} \quad (3)$$

where $P_F$ is the power available to FLY and $P_R$ is the power available to RODENT. In words, RODENT must have sufficient efficiency to homomorphically compute and return data within its power budget faster than FLY can non-homomorphically compute within its power budget. In this paper, we design RODENT to perform such computations within a reasonable energy budget.

III. BACKGROUND

A. Homomorphic Computing

Homomorphic encryption allows computation to occur on encrypted data, typically with a significant time and energy overhead [12], [26]. However, some operations are more efficient than others. For example, linear operations tend to have the least overhead. The vast majority of the operations performed in SVMs are linear multiplications and additions, explained in Section III-B. We choose to perform only these linear operations on RODENT, leaving the final, non-linear operations to be performed after decryption on FLY.

We use the BFV scheme [12], [26], which provides integer arithmetic and is available on both Microsoft SEAL [82] and PALISADE [71]. First, a vector of data is encoded into a plaintext, which is a set of coefficients for a polynomial. Then, the plaintext is encrypted into a ciphertext. The length of the input vector is equal to the number of coefficients in both the plaintext and ciphertext (also called the degree of polynomial modulus). The length of the vector sets a noise budget, where larger vectors have larger noise budgets. All homomorphic computations consume some of the noise budget, and if the budget is exceeded, the data can no longer be successfully decrypted. Testing with Microsoft SEAL [82], we found 4,096 was the minimum vector size that could successfully complete the SVM computations. The coefficient modulus is the maximum value of the ciphertext coefficients, which is represented in a residue number system consisting of three 36-bit prime numbers. A ciphertext consists of two such polynomials. Hence, the total memory required by our ciphertexts is

$$2 \times 3 \times 36 \times 4096 = 110 \text{KB} \quad (4)$$

Homomorphic addition is relatively straightforward, consisting of element-wise additions of the vectors involved. Modulus operations must be performed routinely to prevent the coefficients from growing excessively large. Given that the coefficient modulus is known ahead of time, modulus can be implemented with efficient (virtual) shift, add, and subtract operations in the memory [61].

Homomorphic multiplication is significantly more complicated and consists of multiple steps. The primary components are the number theoretic transform (NTT), which is an integer variant of the FFT, and scales and base conversions [88]. We follow the computation steps laid out by Özerek et. al. [68] for NTT and by Al Badawi et. al. [5] for all other steps.

B. Support Vector Machines

Support vector machines (SVM) are popular machine learning (ML) algorithms which perform well on small problems. The advantages of SVMs are a strong theoretical foundation and proven performance on a wide variety of problems [60]. SVMs are trained by inspecting input samples to a problem, where samples which are indicative of each classification are identified. After training is complete, these samples are referred to as support vectors, and are used to compare to new inputs. The new inputs are classified based on how similar they are to support vectors from each class. By construction, a standard SVM model produces a binary classification, producing a classification of ±1. We use a simple extension to enable multi-class classification, where a separate SVM is trained to identify each class (the one-versus-all method [25]). For example, to classify MNIST, 10 SVMs are used where each identifies one digit 0-9.

A specific advantage for SVMs is that they consist mostly of linear operations, which can be implemented relatively efficiently in homomorphic computing. This provides an advantage over neural networks, for which sophisticated strategies must be invoked to reduce the overhead of frequent non-linear operations [14], [76]. SVM inference involves finding the dot product of the input sample with each of the support vectors. This involves purely multiplications and additions. At the very end, the dot products are squared (multiplication by self), summed, and finally compared, which represents a non-linear operation. While complete SVM training and inference has been successfully demonstrated using homomorphic operations [69], we opt to perform only the initial multiplication and summations on RODENT. We leave the final squaring and sum to be performed on FLY. This prevents us from exceeding the computational depth allowed by our homomorphic encryption (without performing bootstrapping) and avoids the high overhead incurred by the final sum (which requires highly expensive rotation operations to sum elements in the same ciphertext [76]).
output MTJ, as shown in Figure 2. For example, a NAND can be performed by presetting the output MTJ to logic 0 ($R_0$) from the inputs to the output. If both input MTJs are logic 1 ($R_1$) and only one of the MTJs is logic 0 ($R_0$), the current through the output will be less than $I_{\text{switch}}$, and it will remain 0. However, if either input MTJ is logic 0 ($R_0$) and the current will be greater than $I_{\text{switch}}$ and the output will switch to 1. In a nutshell, under the fixed gate-specific voltage the current through the output changes as a function of the input states, and only incurs switching (a change in the output state from the preset) according to the truth table of the corresponding gate. Different logic operations, including NOT, AND, and (N)OR can be performed in identical fashion, with different output preset values and gate-specific voltages, respectively.

C. (Digital) Computing with Magnetic Tunnel Junctions

Magnetic Tunnel Junctions (MTJ) are resistive memory devices consisting of two magnetic layers, a free layer and a fixed layer. The polarity of the free layer can change but the fixed cannot. When the magnetic layers are (not) aligned, the MTJ is in the parallel $R_P$ (anti-parallel $R_{\text{AP}}$) state and has a low (high) resistance. Passing a sufficient amount of current ($I_{\text{switch}}$) through the MTJ from the free (fixed) layer to the fixed (free) layer will set the MTJ into the $R_{\text{AP}}$ ($R_P$) state.

Logic can be performed with MTJs via thresholding \cite{15, 52}, where input MTJs (in parallel) are in series with an output MTJ, as shown in Figure 2. For example, a NAND can be performed by presetting the output MTJ to logic 0 ($R_0$). A (gate-specific) voltage is applied such that electrons flow from the inputs to the output. If both MTJs are logic 1 ($R_1$, high resistance) the current through the output will be less than $I_{\text{switch}}$, and it will remain 0. However, if either input MTJ is logic 0 ($R_0$, low resistance) the current will be greater than $I_{\text{switch}}$ and the output will switch to 1. In a nutshell, under the fixed gate-specific voltage the current through the output changes as a function of the input states, and only incurs switching (a change in the output state from the preset) according to the truth table of the corresponding gate. Different logic operations, including NOT, AND, and (N)OR can be performed in identical fashion, with different output preset values and gate-specific voltages, respectively.

IV. Architecture Design

RODENT must perform homomorphic computation while both remaining within a low power budget and being resilient to intermittent operation. We design an accelerator using a non-volatile processing-in-memory (PIM) substrate which is shown to be both highly energy efficient and inherently intermittent resistant \cite{63}. We augment the PIM capability with simple, intermittent safe protocols and hardware for reception, transmission, and encoding. The architecture is shown in Figure 3. First, in Section IV-A we describe the hardware contained within RODENT, then in Section IV-B we cover how different system components interact with each other, and tolerate intermittent operation.

A. Hardware

1) Computation Arrays: The primary component of RODENT are arrays of MTJ devices used for computation. We call these computation arrays. These arrays both hold data and perform all homomorphic computation on it. The array architecture and cell design is shown in Figure 4, which uses two transistors. This architecture allows for the logic operations discussed in Section III-C to occur in either the rows or columns of the memory array by applying voltages along the bitlines (BL) or the wordlines (WL). The access transistors, controlled by row activate (RA) and column activate (CA), remove potential sneak paths from the array. An example of row-logic is shown in Figure 6, where voltages $V_{\text{in}}$ and $V_{\text{out}}$ are applied to the bitlines, implementing the logic circuit shown in Figure 2. Many logic operations can be performed in parallel in each row (column) simultaneously, as long as the inputs and output reside in the same columns (rows) as shown in Figure 5. Having both row- and column-wise logic allows data to be moved efficiently within each array, removing the need for energy costly read and write operations. This computational capability is equivalent to digital cross-bar arrays \cite{10, 87}, but without the sneak paths which waste energy and introduce correctness concerns \cite{46}. In row-(column-) logic, for each operation the column (row) addresses of the input(s) and output must be specified, along with which rows (columns) are participating in the operation. When rows or columns are performing computation we refer to them as active.

Using two transistors per cell significantly increases the area per cell from 0.0012 $\mu\text{m}^2$ \cite{63} to 0.038 $\mu\text{m}^2$ \cite{96}. However, two transistors are essential for removing cross-bar sneak paths \cite{47}, which would significantly increase energy consumption. As energy efficiency is paramount for beyond edge devices \cite{29}, this cost in area is necessary. Due to the very large
amount of data required by homomorphic computing, the area overhead for computation arrays can become substantial. For the smallest benchmark, ADULT, the computation arrays consume $6.72\, \text{mm}^2$. For the largest benchmark, MNIST, the area is $377\, \text{mm}^2$. For reference, the TI-MSP430FR5994, commonly used as a sub-component of beyond edge systems [28], consumes roughly $100\, \text{mm}^2$.

As described in Section III-A, we use ciphertexts with 4,096 elements. Hence, it is ideal to have 4,096 rows in order to store all elements and enable parallel element-wise homomorphic multiplications and additions. However, due to parasitic bitline/rowline resistance and capacitance, arrays are limited to 1024x1024 [96]. Hence, we use 16 rows of computation arrays, where each array is 512x512. Similar to Gupta et. al. [33], a row of transistors are used to conditionally connect to the bitlines of neighboring computation arrays. This allows logic operations to transfer bits between the neighboring arrays.

Each row of the computation arrays must store all required data for its given computation. The most space intensive subroutine of the homomorphic SVM is the initial multiplication, which can be between two ciphertexts or between a ciphertext and a plaintext. A single element of each polynomial is assigned to each row. Hence, each row requires $2 \times 2 \times 3 \times 36 = 432$ bits for the ciphertexts, 36 bits for twiddle factors for NTT operations [68], plus additional bits for temporary workspace. This easily fits within two columns of computation arrays (1024 bits). However, a third column of computation arrays is required to store additional twiddle factors required for different stages of the NTT algorithm. In total, $\log_2(4096) = 12$ twiddle factors are required in each row.

Since logic operations can be used to transfer data within and between computation arrays, only the cells which store the final results (which are sent to the Bluetooth transmitter) need to be read. Hence, the vast majority of the computation arrays do not require sense amplifiers. As shown in Figure 3 only the first column of computation arrays contain sense amplifiers, which allows them to be used as a non-volatile buffer for the BLE transmitter/receiver and the encoder. Hence, input and output is passed through the first column on computation arrays.

In addition to the memory data, computation arrays must also maintain which rows or columns are currently active. For this purpose, we could use two dedicated non-volatile registers in each computation array - with as many bits in the registers as there are rows and columns in the computation array. Such registers can act as a bitmask for logic operations. However, rather than creating an additional hardware register, we can embed the registers into the memory itself, by dedicating a single row and column for each register. This allows registers to be written with standard logic and write operations. Dedicated instructions use the registers to activate the peripheral circuitry. For correctness guarantees which will be discussed in Section IV-B3 two copies of the registers are required for both rows and columns, as shown in Figure 7.

2) Drivers and Instruction Memory: Signals must be sent into the computation arrays to perform logic gates. For every operation in each array, we need to specify which logic gate...
is being performed (what voltage to apply) and the addresses of the input(s) and the output. Just as in prior work [77], the input and output addresses are specified with each instruction. Additionally, as noted in the previous paragraph, we must know which rows (or columns) are currently active. The currently active rows (or columns) are specified by the bitmask column and row within each computation array.

As each array could perform computation independently, many different gates, inputs, and outputs may need to be specified simultaneously. To efficiently distribute these signals, computation arrays are grouped into columns. Computation arrays in the same column act as a single unit and are driven by the same control signals. For each column of computation arrays, there is an associated driver and non-volatile instruction memory buffer.

The instruction memory arrays store the operations that each column of computation arrays is to perform (NOT, (N)AND, (N)OR) along with the row/column indices of the input(s) and the output of every operation. Each instruction requires the following information.

i. Opcode specifying the logic operation (3 bits)
ii. Up to three addresses for input(s) and output (12 bits each)
iii. Whether it is a row or column operation (1 bit)

To be specific, a driver is a CMOS circuitry that initiates the logic within the computation arrays. On command from the controller, each driver reads an instruction from the specified address and decodes it. Then it sends the input and output addresses to the row/column decoders and drives the appropriate voltage along the bit/row lines of the computation arrays. All drivers operate simultaneously, executing the instructions at the same address (specified by the controller) in their corresponding instruction memories.

3) Encoder: RODENT operates on encrypted data in order to keep the ML model secure (encrypted at all times). If the input is also considered sensitive, it should be encrypted on FLY (into a ciphertext) prior to transmission to RODENT, in which case RODENT can immediately begin processing and does not require an encoder. However, if the inputs are not considered sensitive, it will be more efficient to transmit the raw data. In which case the input, once transmitted to RODENT, must be encoded (into a plaintext) in order to properly interact with the encrypted ML model. Homomorphic encoders for edge devices have previously been developed [91]. We assume RODENT contains such a hardware chip for this purpose.

4) Receiver and Transmitter: RODENT uses Bluetooth Low Power (BLE) to communicate with the nearby FLY. BLE devices can offer extremely energy efficient communication at short distances [30], [42], [48], [84], [85]. We assume a configuration that enables particularly low power, down to 158 pJ per bit [78]. BLE will allow communication within a few tens of meters.

5) Controller: The controller comprises CMOS circuitry which orchestrates the operation of RODENT. It does not directly orchestrate the operation of the other components, rather it simply turns them off or on, and triggers their operation. It maintains a status register (SR), program counter (PC), activates the BLE transmitter/receiver and encoder, and sends trigger signals to the drivers to perform logic in the computation arrays.

B. Operating Semantics

Now that we have described the hardware components of RODENT, we describe how they work together and how they tolerate intermittency. The state transition diagram is shown in Figure 3. RODENT has efficient and fine-grain checkpointing mechanisms in the computation phase, due to the inherent resilience of non-volatile MTJ based memory to power interruptions. RODENT has less efficient checkpointing mechanism in the other phases, where more progress will be lost in the event of a restart.

1) Data Reception and Transmission (I/O): Due to intermittent power, RODENT cannot rely on continuous communication. To avoid complexity, we chose for RODENT to operate under a simple protocol. When RODENT is not busy (there is no input being processed), it is open to new input. RODENT will wait for new input from FLY. After fully receiving input data, RODENT enters the encoding phase and will no longer check for or acknowledge new inputs. Only once computation is complete will RODENT re-activate BLE in order to transmit outputs.

When receiving inputs, the data is stored into a dedicated non-volatile buffer, as shown in Figure 5. The size of the input data is set, so RODENT will know the number of packets it needs to receive. There is a dedicated region of memory for each packet, and there is a valid bit for each packet. RODENT will set all valid bits to 0 prior to reception. The valid bit for each packet is set strictly after the packet has been written into memory. If RODENT loses power after the packet is written but prior to setting of the valid bit, the packet is considered invalid and will need to be re-transmitted. Once all valid bits are set (all packets have been received), RODENT will set a completed bit, which acts as a signal to RODENT’s controller to move to the next stage.
During reception and transmission, no other components of RODENT are in use. The controller will stall all operation until data transfer is complete.

2) Encoding: RODENT uses specialized hardware accelerators for encoding [91]. To make the encoding process intermittent safe, we require it to be atomic. It reads input from the dedicated non-volatile buffer, performs encoding in full, and then writes output into the first column of computation arrays, shown in Figure 3. Due to being atomic, if it is interrupted at any stage it restarts from the beginning. This guarantees correctness on restart, as none of the inputs have been overwritten, however it can waste energy. There is significant room for optimization (i.e., adding efficient checkpointing mechanisms for the encoder), however, we do not focus on the encoder in this work. The vast majority of time and energy is spent on homomorphic computation, where it spends the vast majority of the time, due to ideal properties of MTJ devices.

Since the data is written directly into the computation arrays, it will be ready immediately for processing once encoding has completed. Computation arrays can transfer the data where it is required via logic operations during the computation stage.

3) Computation: Computation takes the most time and energy, therefore it is critical to make it resilient to intermittent operation and energy efficient. Prior work has demonstrated that in-memory logic performed with MTJs is inherently intermittent safe [77]. We exploit this same property to enable high frequency and light-weight checkpointing during computation. However, unlike prior work, we do not need to maintain standard memory functionality. This enables us to remove much energy-inefficient hardware, including most of the sense amplifiers.

During computation, the controller will broadcast the PC value to all drivers. Each driver reads the corresponding instruction in its instruction memory, decodes it, then drives the appropriate signals to the computation arrays in the same column. A sufficient amount of time is allotted between broadcasts of the PC value such that every instruction is guaranteed to have completed. This process repeats until the program has finished or RODENT runs out of power.

Write and logic operations with MTJs [15], [52], [95] remain correct when interrupted or performed multiple times [77]. This means that if the driver triggers a logic operation in the computation arrays, it can be interrupted

i. Before the operation begins
ii. In the middle of the operation
iii. After the operation has finished

and correctness will be maintained. The same logic operation (instruction) can be triggered again, and the output will be as if no interruption had occurred [77]. Hence, a single instruction represents an idempotent operation. This means that, after RODENT has restarted, the controller can safely send the same PC value to the drivers and the instruction will be performed (or re-performed) and produce the correct output.

Due to this inherent resilience, correctness of data in the memory is easy to guarantee as long as we progress in program order by only a single instruction at a time. This means we need to checkpoint after every instruction, and not start the next instruction until the previous has been completed. Such frequent checkpointing may be inefficient for more traditional architectures [43], [51], however RODENT can do this with ease. As the computation is occurring in (non-volatile) memory, all data backup happens automatically. All results are permanently stored after every instruction, regardless of the checkpointing strategy. Hence, RODENT can perform frequent checkpointing with low overhead by simply tracking architectural state variables in the controller. For computation, the controller only needs to keep track of the valid PC value.

As noted in Section IV-A1 which rows or columns are active is part of the architectural state. A single row and column from each computation array is dedicated to hold the bitmask for active columns and rows. Hence, the active rows and columns are protected by the same mechanism as all other data in memory. Being non-volatile, the bitmasks persist through power interruptions. However, the peripheral circuitry will need to be re-activated on restart. Dedicated instructions, activate rows and activate columns, restore the peripheral circuitry based on the bitmask values. These instructions are issued whenever the bitmask changes, the instructions switch between row-wise or column-wise, and on re-start.

An advantage of storing the active row/column bitmasks in the computation arrays themselves is that they can be set with standard write and logic operations. A disadvantage is that it introduces potential incorrectness. If a row- (column-) parallel instruction modifies the row (column) bitmask, the instruction relies on the current value of the bitmask. If this operation gets interrupted prior to completion of the instruction, some of the values in the bitmask may have changed. When the instruction is re-performed on startup, the modified value of the bitmask will be used instead. Our solution is to duplicate...
the bitmasks and maintain parity bits, row parity (RP) and column parity (CP), which indicate which bitmask is valid. Hence, two columns and two rows are dedicated for bitmasks. Instructions are only allowed to modify the currently invalid bitmask, leaving the currently valid bitmask unperturbed. After the invalid bitmask has been successfully modified, the corresponding parity bit can be flipped and the rows or columns re-activated.

4) Controller: RAT’s controller is responsible for maintaining the state transitions depicted in Figure 8 and it holds the architectural state variables required for driving computation. It maintains a status register (SR), which indicates whether RODENT is in the reception, encoding, computing, or transmission state. Additionally, it maintains the program counter (PC) which is sent to the drivers to initiate instructions during the computation state.

Given the relatively little information the controller must maintain, simple checkpointing strategies are sufficient. Both the SR and the PC are duplicated and have an ancillary non-volatile parity bit. The parity bit indicates which copy is valid, and it is flipped strictly after each variable is updated. Hence, a currently valid copy of either the SR and PC is never written to, which prevents potential corruption due to an interrupted write operation. Setting the parity bit is an atomic operation, the non-volatile MTJ holding the bit will either be successfully flipped or will remain in its old value (if interrupted during the write operation). If RODENT restarts without flipping the parity bit, the old value of the SR and PC will be used. As explained below, this will waste energy but not introduce incorrectness. If RODENT restarts after flipping the parity bit, effectively all progress has been saved and RODENT will start where it left off. To ensure correctness of these mechanisms, RODENT performs the states and instructions sequentially and strictly in order. There is no overlap of instructions, states of the controller, or updates of the architectural state variables.

During the transmission and reception phases, the controller hands control over to the BLE transmitter/receiver. An efficient protocol for intermittent safe transmission/reception is beyond the scope of this work – see Section VII for a discussion. However, we note that strategies for noisy transmission with large amounts of packet loss [6] could likely be adapted for handling intermittency. RODENT’s controller will hand over control and the simply wait for the completed signal, in which case it will transition to the next phase. If interrupted prior to the arrival of the complete signal, RODENT will again hand control over to the transmitter/receiver on restart. In the worst case, an entire data packet will need to be re-transmitted or received. Additionally, if transmission/reception have completed, but the completion signal was not sent prior to shut down, the controller will have to re-check the signal before progressing to the next stage.

The encoding process follows a similar strategy. During the encoding processes there are no checkpoints. Introducing checkpoints can guard against progress loss on restart, however, for this work we assume the encoding process must not be interrupted. Hence, if there is a restart in the encoding state, the controller will instruct the encoder to start from the beginning.

RODENT has efficient and finely-grained checkpointing mechanisms in the compute phase. Due to the ideal properties of MTJ based memory arrays discussed in Section V-A1, RODENT can easily checkpoint after every instruction [77]. The controller sends the instruction address to the drivers, which load the instruction and trigger it in the computation arrays. The controller waits a sufficiently long time to guarantee the completion of the instruction, after which it updates the PC and commits the instruction by flipping the non-volatile parity bit. As this checkpoint occurs after each instruction, at most one instruction needs to be re-performed in the case of a power outage. The logic operations performed in the memory are inherently idempotent [77], (meaning that they can be performed multiple times) and will produce the same result. Hence, the instruction can be interrupted at any stage in its progressing and we can safely restart it when the power is restored.

V. Evaluation

We evaluate RODENT performing one homomorphic SVM inference to assess the feasibility. We can then compare the net impact on FLY, to see if the presence of RODENT provides an improvement in performance. We analyze the scenario where inputs are not sensitive, however, the machine learning models that process them are proprietary, and are therefore sensitive. This means that FLY can transmit non-encrypted sensor data to RODENT, however RODENT must perform homomorphic inference and return encrypted results to keep the model secure.

For benchmarks, we use MNIST [45], Human Activity Recognition [4], [89], and ADULT [44]. These datasets are representative of the input sizes that will be expected for beyond edge devices. When performing homomorphic inference, the data size is determined by $D$, the dimension of the input sample sizes, and $N$, the length of our homomorphic ciphertexts. The $D$ individual elements from each sample must be in separate ciphertexts, as each element must be summed together (elements within the same ciphertext cannot be added without expensive rotation operations [76]). As described in Section III-A, our ciphertexts are fixed at $N = 4096$. The number of support vectors required for each benchmark fill the 4096 element ciphertexts, with the remaining elements padded with dummy data. Hence, regardless of the number of support vectors, each benchmark uses 4096 element ciphertexts. MNIST contains 784 elements (representing a $28 \times 28$ image), HAR contains 561 elements, and ADULT contains 14 elements. For all benchmarks, we normalized the input to fit within 3-bit integers (values 0-7). This lowers transmission cost and prevents arithmetic overflow during computation. We use customized SVM models which use only integer arithmetic and limited the number of support vectors to 4096. Despite these limitations, we were still able to achieve reasonable accuracy relative to full-precision SVMs provided by libSVM [13], which we accessed through R [73] with the ‘e1071’ package [62]. The SVM parameters and accuracies are listed in Table I. Using integers allows us to use the BFV homomorphic scheme for integer arithmetic [12], [26], which has a lower overhead. We validated that homomorphic operation produces identical output by using Microsoft SEAL [82] to perform the multiplications and additions within the SVM.
TABLE I: SVM benchmarks used in this work and parameters used in RODENT. The number of support vectors does not impact latency and energy as they are padded to 4096. For comparison, the accuracy of full-precision SVMs from libSVM [13] with unlimited support vectors is reported.

| Benchmark | Input Bits | Precision | Dimension (D) | # Support Vectors | RODENT Accuracy | SVM Accuracy
|-----------|------------|-----------|---------------|-------------------|----------------|----------------|
| MNIST     | 2          | 32-bit    | 784           | 1822              | 38.1%          | 92.6%         |
| HAR       | 7          | 64-bit    | 256           | 2064              | 93.6%          | 94.1%         |
| ADULT     | 3          | 32-bit    | 14            | 596               | 94.64%         | 93.05%        |

TABLE II: Parameters for MTJ devices.

| Parameter                  | Modern       | Projected    |
|----------------------------|--------------|--------------|
| $R_P$                      | 3.15 kΩ      | 7.34 kΩ      |
| $R_{AP}$                   | 7.34 kΩ      | 76.39 kΩ     |
| Switching Time             | 3 ns [67], [80] | 1 ns [81]    |
| Switching Current          | 10 μA [67], [80] | 15 μA [81]  |

MTJ based memory technology is already commercially available [1], [2], however, the devices are expected to significantly improve over the next few years. Hence, we evaluate RODENT with two different MTJs models. A modern model, which uses parameters of MTJs which have already been demonstrated, and a projected model, which estimates MTJ performance within 3-5 years. These parameters are listed in Table II.

We model the energy harvester as a constant power source, which fills a 1 mF capacitor (energy buffer) on the chip. In practice, tunable energy buffering systems such as Capybara [13] can be used. The power source increases the voltage on the capacitor up to a specified value, at which point RODENT turns on and consumes energy until the minimum voltage on the capacitor is reached. RODENT then shuts down and waits for the capacitor to recharge. We assume that RODENT has access to sunlight, which can provide a relatively large amount of power for beyond edge devices. We test from 2 mW (0.02 cm$^2$ solar panel [43]) up to 100 mW (1 cm$^2$ solar panel [43]). It is desirable to match the voltage level on the capacitor to the MTJ technology used. Projected MTJs have a lower operating voltage and power draw than modern MTJs. For modern MTJs, the voltage fluctuates between 400 mV and 700 mV and for projected MTJs the voltage fluctuates between 100 mV and 575 mV. As noted in Section II-C different logic operations require different voltages. We use switched-capacitor converters for upconversion and downconversion to provide all required voltages [34], [41], [74].

We generate latency and energy estimates of RODENT with an in house simulator which accounts for the overhead due to MTJs (as listed in Table II) and peripheral circuitry, which we extrapolate from NVSIM [24]. NVSIM gives us the relative share of latency and energy that peripheral circuitry will consume for non-volatile memories with the same size as our computation arrays. We clock RODENT at 30.3 MHz with modern MTJs and at 90.9 MHz with projected MTJs. This gives more than sufficient time for the controller to broadcast the PC and for the drivers to finish logic operations in the memory. This clock rate is conservative, which leaves potential performance improvements on the table. However, since the performance of beyond edge devices will be limited by energy efficiency rather than performance [28], [29] ensuring completion of all instructions far outweighs any potential performance gains.

As discussed in Section IV-B3 the logic operations in the memory are inherently resilient to interruption and we can checkpoint after every instruction with low overhead [77]. However, the reception, transmission, and encoding process do not have this benefit. For transmission and reception, we assume that a power interruption results in the re-transmission or reception of a single element of data. Elements transmitted prior would have been saved in non-volatile memory. For encoding, we assume that the entire encoding process must be restarted if interrupted. If interrupted once, RODENT will re-attempt on restart. At this point, the capacitor will be fully charged and RODENT will have sufficient energy to complete the process. For transmission cost, we assume 158 pJ/bit [78] and for encoding we take latency and energy directly from Van der Hagen et. al. [91] who developed an encoder/encryptor which operates on ciphertexts of the same size as in this work – 0.3 ns and 60 μJ, respectively.

The latency of one inference (including transmission and encoding) is shown in Figure 9 for modern MTJs and in Figure 10 for projected MTJs. Due to high energy cost of homomorphic computation, the latency is quite high and increases dramatically as the power source reduces. For RODENT to still demonstrate improvement, the latency on RODENT must be less than the latency of local processing on FLY and transmitting to a high-power distance server. For local processing, FLY can perform non-homomorphic inference, since FLY is in a secure location and can use non-encrypted ML models. SONIC [28], a beyond edge ML accelerator, requires 27 mJ to perform MNIST and 12.5 mJ to perform HAR. If FLY is operating on thermal energy (due to its deployment within the walls of a building, e.g.), we can assume that its power budget is roughly 60 μW [43]. If FLY is as efficient as SONIC, it will take 450 s to complete MNIST, 208 s to complete HAR, and 8.03 s to complete ADULT. Hence, we can see that RODENT can provide a faster solution than local processing on MNIST/HAR/ADULT if its power budget is 3.36 mW/4.28 mW/11.29 mW, even with modern MTJs. For sending data to a distant server, the cost of transmission is approximately 400 μJ per bit. To acquire enough energy to transmit inputs to the server, FLY will take 15,680 seconds for MNIST, 11,220 seconds for HAR, and 280 seconds for ADULT – much higher than the alternatives. These results are summarized in Table III.

Consistent with prior work [28], [77], latency is mostly determined by energy efficiency as the device is energy constrained. Consequently, projected MTJs, which are much more energy efficient, enable a significantly reduced latency. Due to the significant overhead of homomorphic computation, despite our lack of bootstrapping, RODENT requires a substantial power budget to remain within reasonable latency constraints. Due to the efficiency of our checkpointing mechanisms, energy consumption is determined mostly by the length of the program, rather than the number of interruptions. The absolute energy consumption of SVM inference on RODENT (evaluated at 2 mW) is listed in Table IV. To evaluate the efficiency of RODENT relative to prior work, we compare polynomial multiplication (the core of homomorphic multiplication and the most energy intensive component of our benchmarks) with
TABLE III: As described in Section II, a beyond edge device can (1) Report all results to a remote server, (2) Perform processing locally, or (3) Offload computation to the nearby RODENT. If FLY has the energy efficiency of the beyond-edge device SONIC [28] and is operating on a reasonable 60 µW (which can be harvested with thermal energy [43], [60]), options (1) and (2) result in the reported latencies. The energy per bit for transmission to the distant server is assumed to be 400 µJ [11]. Also shown is the power required by RODENT to achieve the fastest solution with option (3). Due to being more exposed, RODENT should have access to tens of milliWatts of power [43]. *Results extrapolated.

| Benchmark | Option 1: Remote Server | Option 2: Local Processing | Option 3: RODENT | Minimum power for RODENT to provide fastest solution (mW) |
|-----------|--------------------------|----------------------------|-----------------|----------------------------------------------------------|
| MNIST     | 15,680                   | 450                        | E_FT / P_FT     | 3.36                                                     |
| HAR       | 11,220                   | 208                        | E_FT / P_FT     | 4.28                                                     |
| ADULT     | 280                      | 8.03*                      |                 | 11.29                                                    |

![Latency of homomorphic SVM inference with modern MTJs using different power sources.](image1)

Fig. 9: Latency of homomorphic SVM inference with modern MTJs using different power sources.

![Latency of homomorphic SVM inference with projected MTJs using different power sources.](image2)

Fig. 10: Latency of homomorphic SVM inference with projected MTJs using different power sources.

![Energy consumption of homomorphic SVM inference on RODENT for different benchmarks.](image3)

TABLE IV: Energy consumption of homomorphic SVM inference on RODENT for different benchmarks.

| Benchmark | Energy (µJ) |
|-----------|-------------|
| MNIST     | 1,188,716   |
| HAR       | 831,282     |
| ADULT     | 317,736     |

![Energy consumption of polynomial multiplication (developed by Nejatollahi et. al [65]) on RODENT and related work. N is the polynomial size and b is the bitwidth.](image4)

TABLE V: Energy consumption of polynomial multiplication (developed by Nejatollahi et. al [65]) on RODENT and related work. N is the polynomial size and b is the bitwidth.

| Architecture (N,b) | Energy (µJ) |
|--------------------|-------------|
| X86 (1K,16) [64] | 2483.77     |
| X86 (4K,32) [64] | 10864.64    |
| FPGA (1K,16) [65] | 12.52       |
| CryptoPIM (1K,16) [64] | 11.04 |
| CryptoPIM (4K,32) [64] | 178.62 |
| RODENT (1K,16) | 9.68        |
| RODENT (4K,32) | 54.65       |

![Dead, restore, and backup overheads for both latency and energy [31]. Dead refers to latency and energy dedicated to re-performing operations after restart which were already performed before shutdown. This accounts for wasted operations – which completed but the results of which cannot be used. For RODENT, this comes from re-performing that last in-memory instruction, re-transmitting or receiving a packet of data, and re-encoding input. Restore refers to overhead associated with restarting the device, getting it back into working order after a power outage. For RODENT, this is the re-activation of rows and columns of the memory arrays. Backup is any operation performed in order to save state prior to shutdown. This typically involves saving the architectural state and storing volatile data to non-volatile memory. As RODENT performs all computation in the memory, data backup occurs automatically. Hence, the only backup cost for RODENT is saving the architectural state, setting the SR, PC, and parity bit. The latency overhead for each of these is shown in Figure 11 and the energy overhead is shown in Figure 12. The shown overheads are evaluated at 20 mW, the lowest power considered, which results in the maximum number of restarts, and therefore, the maximum overhead.

Overheads for projected MTJs are less because RODENT will have to restart less often due to their greater energy efficiency. Dead energy involves re-performing instructions (which typically involve performing many parallel logic operations). Overall, projected MTJs are much more efficient than modern MTJs. Dead energy is 0.2889% of the total for modern MTJs and 0.0040% for projected MTJs. The restore energy is also much lower for projected MTJs, as it is also incurred...
by only restarts where the peripheral circuitry needs to be reset. Restore energy is 0.0185% of the total for modern MTJs and 0.0002% of the total for projected MTJs. As it involves only updates to architectural state variables, the backup energy tends to be much lower. The backup energy is 0.0187% of the total for modern MTJs and 0.0147% of the total for projected MTJs. Backup energy is incurred on every instruction, so it is not largely impacted by the number of restarts.

Backup has no associated additional latency as it occurs during the execution of each instruction. The dead and restore latency are functions of the number of restarts. Dead (restore) latency is 0.0006716% (0.0001209%) of the total compute latency for modern MTJs. For projected MTJs the dead (restore) latency is a negligible 0.0000028% (0.0000006%).

VI. LIMITATIONS AND POTENTIAL IMPROVEMENTS

In this section we discuss the limitations of RODENT and potential improvements. While relevant, these extensions are beyond the scope of this paper or are left for future work.

A. Communication Protocol

In this work we use a simplified communication scheme, where FLY and RODENT transfer data back and forth. There are a number of complicating factors which can disrupt proper operation. FLY may begin transmission but then lose power for an extended period of time. In this case, RODENT would remain in reception mode, spending its entire time waiting for input that does not come. RODENT should contain some method of cancelling a reception and revert to an idle and available mode. While a variant of watchdog timer can be deployed to this end, data transfers during intermittent operation pose a considerable challenge. Additionally, if RODENT goes without power for an extended period of time, it may work on input which is old and no longer relevant. Keeping beyond edge devices working on relevant tasks across time is an important problem [86].

B. Communication Energy and Deployment

Communication between FLY and RODENT will only be efficient if they can be deployed in close proximity. Bluetooth Low Energy (BLE) only allows for communication within tens of meters. At further distances, they must resort to long-range (LoRa) technology [11], which can undo the benefit RODENT provides.

C. Power Limitations

Homomorphic computation, even without bootstrapping, remains an energy costly process. Even with the efficient computation enabled by RODENT, collecting enough energy beyond edge remains a challenge. Even simple computations will take a long time, which may be insufficient for a number of applications. Further methods to increase energy efficiency may be necessary for practical implementation. A possible solution is implementing fleets of beyond edge devices [22], [23]. As such, each individual device could compute slowly, but a high throughput could be achieved with their combined effort.

VII. RELATED WORK

Power delivery is particularly challenging for beyond edge devices. Tunable systems like Capybara [18] have been designed to optimally store and deliver energy. We assume RODENT relies on such a system.

Many low power processors and ML accelerators exist [20], [40], [49], [83], [90], [93], [97], however, these architectures do not guarantee correctness during intermittent operation. Adding such guarantees adds a large performance and efficiency overhead. Numerous beyond edge devices have been designed to function correctly in intermittent contexts [51], [57], including ML accelerators [28]. These devices have more traditional architectures, which have been augmented with nearby non-volatile memory for fast backup operations. Much research has been dedicated to tolerating intermittency for more general purpose architectures, including lowering checkpointing overheads and clever methods of detecting power outages [5], [7], [9], [16], [17], [27], [35], [36], [39], [50], [56], [58], [75], [79], [92] along with modifications of software [55], [59]. RODENT's advantage over these designs is significantly more energy efficient in-memory logic and simplified checkpointing mechanisms.

Resch et. al. [77] have proposed an in-memory intermittent safe accelerator. However, the architecture maintains standard memory format, which adds unnecessary space and energy overhead, and is capable only of 1D computations (only along rows or only along columns). In contrast, RODENT's architecture is capable of 2D computations (similar to a crossbar, along rows and columns, but digital) and is tightly tailored to homomorphic SVM inference. Mapping homomorphic inference onto [77] would incur a large communication (read/write) overhead due to the required intra-array data movement. ResiRCA [72] uses in-memory computation to accelerate parts of ML inference and adapts the amount of parallelism to match the amount of harvested energy. However, they rely on a battery to maintain a controlling CPU.

Significantly, none of the prior work mentioned thus far has accelerated homomorphic inference, which is necessary to maintain security in un-trusted environments. To the best of the author's knowledge, no beyond edge homomorphic accelerator exists. However, much prior work has been done on accelerating homomorphic computation with continuous power. This includes software optimization [76], FPGA implementations [65], [88] and processing-in-memory implementations like CryptoPim [64]. CryptoPim developed strategies to minimize latency and energy overhead for NTT operations, the core of
homomorphic multiplication. While CryptoPim is not designed to handle intermittent operation, we do use strategies they developed, such as efficient modulus operations, in our work. Efficient encoding and encryption is required to make homomorphic computation feasible in edge or beyond edge domains. Van Der Hagen et al. [91] developed energy efficient accelerators to this end.

VIII. CONCLUSION

Beyond edge devices operate on harvested energy, significantly increasing deployment capabilities and widening the potential applications. However, these devices are by construction extremely limited by the power available. In this paper we propose a beyond edge, intermittent safe accelerator which can compute homomorphically, and which can be used as a local server to offload computation. The deployment capability of this accelerator can significantly reduce the communication cost for other beyond edge devices to offload computation. The accelerator is capable of maintaining security by performing homomorphic computation and its unique architecture enables this to be done within a reasonable power budget.

REFERENCES

[1] https://www.everspin.com/supportdocs/EMD3D256M08G1-150CB51
2019, accessed: 2021-11-17.
[2] https://www.everspin.com/family/edm4e001g?path=3557
2019, accessed: 2021-11-17.
[3] A. Q. A. Al Badawi, Y. Polyakov, K. M. M. Aung, B. Veeravalli, and K. Rohloff, “Implementation and performance evaluation of rns variants of the bfv homomorphic encryption scheme,” IEEE Transactions on Emerging Topics in Computing, 2019.
[4] D. Anguita, A. Ghio, L. Oneto, X. Parra, and J. L. Reyes-Ortiz, “A public domain dataset for human activity recognition using smartphones,” in Esann, 2013.
[5] F. A. Aouda, K. Marquet, and G. Salagnac, “Incremental checkpointing of program state to nvram for transiently-powered systems,” in 2014 9th International Symposium on Reconfigurable and Communication-Centric Systems-on-Chip (ReCoSoC). IEEE, 2014, pp. 1–4.
[6] S. Arabi, E. Sabir, and H. Elbiaze, “Information-centric networking meets delay tolerant networking: Beyond edge caching,” in 2018 IEEE Wireless Communications and Networking Conference (WCNC). IEEE, 2018, pp. 1–6.
[7] D. Balsamo, A. Das, A. S. Weddell, D. Brunelli, B. M. Al-Hashimi, G. V. Merrett, and L. Benini, “Graceful performance modulation for power-neutral transient computing systems,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 35, no. 5, pp. 738–749, 2016.
[8] D. Balsamo, A. S. Weddell, A. Das, A. R. Arreola, D. Brunelli, B. M. Al-Hashimi, G. V. Merrett, and L. Benini, “Hibernate++: a self-calibrating and adaptive system for transiently-powered embedded devices,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 35, no. 12, pp. 1968–1980, 2016.
[9] G. Berthou, T. Delizy, K. Marquet, T. Risset, and G. Salagnac, “Periphal state persistence for transiently-powered systems,” in 2017 Global Event of Things Summit (GloTS). IEEE, 2017, pp. 1–6.
[10] D. Bhattacharjee et al., “Contra: area-constrained technology mapping framework for memristive memory processing unit,” in ICCAD, 2020.
[11] T. Bouguera, J.-F. Diouris, J.-J. Chaillout, R. Jaouadi, and G. Andrieux, “Energy consumption model for sensor nodes based on lora and lorawan,” Sensors, vol. 18, no. 7, p. 2104, 2018.
[12] Z. Brakerski, “Fully homomorphic encryption without modulus switching from classical gaps,” in Annual Cryptology Conference. Springer, 2012, pp. 868–886.
[13] C.-C. Chang and C.-J. Lin, “Libsvm: A library for support vector machines,” ACM transactions on intelligent systems and technology (TIST), vol. 2, no. 3, p. 27, 2011.
[14] J. Chao, A. A. Badawi, B. Unnikrishnan, J. Lin, C. F. Mun, J. M. Brown, J. P. Campbell, M. Chiang, J. Kalpathy-Cramer, V. R. Chandrasekhar et al., “Carenets: compact and resource-efficient cnn for homomorphic inference on encrypted medical images,” arXiv preprint arXiv:1901.10074, 2019.
[15] Z. Chowdhury et al., “Efficient in-memory processing using spintronics,” IEEE CAL, vol. 17, no. 1, 2017.
[16] A. Colín and B. Lucia, “Chain: tasks and channels for reliable intermittent programs,” in ACM SIGPLAN Notices, vol. 51, no. 10. ACM, 2016, pp. 514–530.
[17] A. Colín and B. Lucia, “Termination checking and task decomposition for task-based intermittent programs,” in Proceedings of the 27th International Conference on Compiler Construction. ACM, 2018, pp. 116–127.
[18] A. Colín, E. Ruppel, and B. Lucia, “A reconfigurable energy storage architecture for energy-harvesting devices,” in Proceedings of the Twenty-Third International Conference on Architectural Support for Programming Languages and Operating Systems, 2018, pp. 767–781.
[19] A. Collado and A. Georgiadis, “Conformal hybrid solar and electromagnetic (em) energy harvesting rectenna,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 60, no. 8, pp. 2225–2234, 2013.
[20] F. Conti, P. D. Schiavone, and L. Benini, “Xnor neural engine: A hardware accelerator ip for 21.6-fj/op binary neural network inference,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 37, no. 11, pp. 2940–2951, 2018.
[21] M. Danesh and J. R. Long, “Photovoltaic antennas for autonomous wireless systems,” IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 58, no. 12, pp. 807–811, 2011.
[22] B. Denby and B. Lucia, “Orbital edge computing: Machine inference in space,” IEEE Computer Architecture Letters, vol. 18, no. 1, pp. 59–62, 2019.
[23] B. Denby and B. Lucia, “Orbital edge computing: Nanosatellite constellations as a new class of computer system,” in Proceedings of the Twenty-Fifth International Conference on Architectural Support for Programming Languages and Operating Systems, 2020, pp. 939–954.
[24] X. Dong, C. Xu, X. Xie, and N. P. Jouppi, “Nsvim: A circuit-level performance, energy, and area model for emerging nonvolatile memory,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 31, no. 7, pp. 994–1007, 2012.
[25] K.-B. Duan and S. S. Keerthi, “Which is the best multiclass svm method? an empirical study,” in International workshop on multiple classifier systems. Springer, 2005, pp. 278–285.
[26] J. Fan and F. Vercauteren, “Somehow practical fully homomorphic encryption,” IACR Cryptol. ePrint Arch., vol. 2012, p. 144, 2012.
[27] K. Ganesan, J. San Miguel, and N. E. Jerger, “The what’s next intermittent computing architecture,” in 2019 IEEE International Symposium on High Performance Computer Architecture (HPCA). IEEE, 2019, pp. 211–223.
[28] G. Gobieski, B. Lucia, and N. Beckmann, “Intelligence beyond the edge: Inference on intermittent embedded systems,” in Proceedings of the Twenty-Fourth International Conference on Architectural Support for Programming Languages and Operating Systems, 2019, pp. 199–213.
[29] G. Gobieski, A. N. R. Serafin, M. M. Isgenc, N. Beckmann, and B. Lucia, “Manic: A vector-dataflow architecture for ultra-low-power embedded systems,” in Proceedings of the 52nd Annual IEEE/ACM International Symposium on Microarchitecture, 2019, pp. 670–684.
[30] C. Gomez, J. Oller, and J. Paradells, “Overview and evaluation of bluetooth low energy: An emerging low-power wireless technology,” Sensors, vol. 12, no. 9, pp. 11 734–11 753, 2012.
[31] A. Green, Y. Hishikawa, B. M. Al-Hashimi, D. H. Levi, J. Holub-Ebinger, and A. W. Ho-Baillie, “Solar cell efficiency tables (version 52),” Progress in Photovoltaics: Research and Applications, vol. 26, no. 7, pp. 427–436, 2018.
[32] H. Greenspan, B. Van Ginneken, and R. M. Summers, “Guest editorial: deep learning in medical imaging: Overview and future promise of an exciting new technique,” IEEE transactions on medical imaging, vol. 35, no. 5, pp. 1153–1159, 2016.
[33] S. Gupta, M. Imani, and T. Rosing, “Felix: Fast and energy-efficient logic in memory,” in 2018 IEEE/ACM International Conference on Computer-Aided Design (ICCAD). IEEE, 2018, pp. 1–7.
[34] R. Harjani and S. Chaubey, “A unified framework for capacitive series-parallel dc-dc converter design,” in Proceedings of the 2014 IEEE Custom Integrated Circuits Conference. IEEE, 2014, pp. 1–8.
[35] J. Hester, K. Storer, and J. Sorber, “Timely execution on intermittently powered batteryless sensors,” in Proceedings of the 53rd ACM Conference on Embedded Network Sensor Systems. ACM, 2017, p. 17.
[36] M. Hicks, “Clank: Architectural support for intermittent computation,” in 2017 ACM/IEEE 44th Annual International Symposium on Computer Architecture (ISCA). IEEE, 2017, pp. 228–240.
[37] P. Jaffe and J. McSpann, “Energy conversion and transmission modules for space solar power,” Proceedings of the IEEE, vol. 101, no. 6, pp. 1424–1437, 2013.
[87] N. Talati et al., “Logic design within memristive memories using memristor-aided logic (magic),” IEEE Transactions on Nanotechnology, vol. 15, no. 4, 2016.

[88] F. Turan, S. S. Roy, and I. Verbauwhede, “Heaws: An accelerator for homomorphic encryption on the amazon aws fpga,” IEEE Transactions on Computers, vol. 69, no. 8, pp. 1185–1196, 2020.

[89] https://archive.ics.uci.edu/ml/datasets/human+activity+recognition+using+smartphones, 2019, accessed: 2019-06-02.

[90] H. Valavi, P. J. Ramadge, E. Nestler, and N. Verma, “A 64-tile 2.4-mb in-memory-computing cnn accelerator employing charge-domain compute,” IEEE Journal of Solid-State Circuits, vol. 54, no. 6, pp. 1789–1799, 2019.

[91] M. van der Hagen and B. Lucia, “Practical encrypted computing for iot clients,” arXiv preprint arXiv:2103.06743, 2021.

[92] J. Van Der Woude and M. Hicks, “Intermittent computation without hardware support or programmer intervention,” in 12th {USENIX} Symposium on Operating Systems Design and Implementation ({OSDI} 16), 2016, pp. 17–32.

[93] J. Wang, X. Wang, C. Eckert, A. Subramaniyan, R. Das, D. Blaauw, and D. Sylvester, “A 28-nm compute sram with bit-serial logic/arithmetic operations for programmable in-memory vector computing,” IEEE Journal of Solid-State Circuits, vol. 55, no. 1, pp. 76–86, 2019.

[94] F. Yildiz, “Potential ambient energy-harvesting sources and techniques.” Journal of technology Studies, vol. 35, no. 1, pp. 40–48, 2009.

[95] M. Zabihi, Z. I. Chowdhury, Z. Zhao, U. R. Karpuzcu, J.-P. Wang, and S. Sapatnekar, “In-memory processing on the spintronic cram: From hardware design to application mapping,” IEEE Transactions on Computers, vol. 68, no. 8, pp. 1159–1173, 2018.

[96] M. Zabihi, A. K. Sharma, M. G. Mankalale, Z. I. Chowdhury, Z. Zhao, S. Resch, U. R. Karpuzcu, J.-P. Wang, and S. S. Sapatnekar, “Analyzing the effects of interconnect parasitics in the stt cram in-memory computational platform,” IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, vol. 6, no. 1, pp. 71–79, 2020.

[97] J. Zhang and N. Verma, “An in-memory-computing dnn achieving 700 tops/w and 6 tops/mm 2 in 130-nm cmos,” IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 9, no. 2, pp. 358–366, 2019.