Design of 1Gsps high-speed data acquisition card

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Abstract. In order to digitize the High-Frequency signal, a 12-bit 1Gsps RF Sampling data acquisition system is designed. The digital acquisition system includes an Analog-to-Digital Converter (ADC) daughter card and a data processing mother card equipped with Field Programmable Gate Arrays (FPGA) for communication, which has an external DDR3 memory module and a Gigabit Ethernet Interface. It focuses on the hardware system implementation of the daughter card and the realization of data receiving, transferring, and sending based on the FPGA. The test results show that the Effective Number of Bit (ENOB) of the acquisition card is above 9.1 Bits. Both Integral Non-Linear (INL) and Differential Non-Linearity (DNL) are anticipated. It accomplishes the requirements for engineering applications in many fields excellently.

1. Introduction
Data acquisition system is the core hardware of electronic engineering for scientific testing of High Energy Physics, Geospatial Physics, Cyberscience and other disciplines. This system can collect analogy signals, which include but are not limited to Photoelectric Pulses, Broadband Communication Signals and Radar Intermediate Frequency Signals required nanosecond-level accuracy [1].

In the past, the frequency and effective bits of acquisition card were not high enough to meet the requirements for digital analysis of these signals in electronics. To this end, 1Gsps high-speed data acquisition card is designed. The FPGA Mezzanine Card (FMC) connection is used to design as Daughter-Mother card structure [2]. Daughter card is designed to achieve the acquisition of analogy signal. Mother card is responsible for high-speed signal processing based on Virtex-6 FPGA. With a highly expandable FMC connector, mother card can be reused. It is convenient to upgrade or replace the daughter card in future.

2. Acquisition card system structure
The overall structure of the system is that the daughter card communicates with the mother card through the FMC. The daughter card is responsible for data acquisition, which is composed of signal conditioning circuit, frequency synthesizer, clock fan-out, power module and ADC circuit. The analogy signal usually passes through the conditioning circuit to adapt to the dynamic input range of the ADC. One channel of 500MHz clock produced by the frequency synthesizer passes through the clock fan-out chip to the ADC as the sampling clock and the other channel is given to the FPGA as the backup reference clock through the FMC clock pin. The mother card equipped with FPGA uses hardware description language to design the digital logic of ADC data receiving, transferring to DDR3.
and transmitting to PC via Gigabit Ethernet port. As a complete analogy-digital hybrid electronic system [3], its structure diagram is shown in Figure 1.

![Figure 1. Acquisition system structure diagram.](image)

The core of the frequency synthesizer is the ultra-low-noise frequency synthesizer LMX2541 with integrated VCO. The 3.3V voltage required by the chip and the 1.8V voltage required by the ADC are directly provided by the FMC pin. Its working mode is realized by the FPGA controlling its internal registers through the SPI bus linked by the FMC. A good phase detection frequency can support an output frequency of 500MHz to meet the ADC clock frequency requirements. Very low noise and jitter can meet the requirements of ADC input clock [4].

3. Analog signal conditioning

Signal conditioning includes amplitude attenuation resistor network, filter and single-ended to differential circuit. It is a key front-end part of an analogy signal acquisition card. Its structure is shown in Figure 2.

![Figure 2. Signal conditioning structure diagram.](image)

The amplitude attenuation circuit is an adjustable resistance attenuation network that attenuates the amplitude of analogy signals of different amplitude values and can meet the voltage range of the ADC sampling signal. The analogy signals all pass through a band-pass filter, which can filter out the extremely high and low frequency noise signals. It can effectively increase the effective bit of the acquisition card. The high-speed RF transformer converts the single-ended signal into differential signal that can meet the requirements of the ADC for ac-coupling analogy input.

4. High-speed ADC sampling

The ADC has two internal channels that can multiplex one analogy input and output 48-bit four-channel differential parallel data. The sampling clock frequency only needs 500MHz and the output channel clock frequency is 250MHz, which reduces the difficulty of the hardware system design to maintain signal integrity requirements for placement and routing delays and meets the FMC data transfer rate. Although FMC interface equal-length wiring poses great challenges, its flexibility cannot be replaced.

The ADC has two analogy input channels including I channel and Q channel, which can work in dual-channel 500Msps sampling mode or single-channel 1Gsps sampling mode. At this time, I channel is selected as the AC-coupled analogy input and the internal multiplexing module. It is transmitted to two ADC cores and sampled at the rising and falling edges of the 500MHz clock. Each ADC core
outputs two 24-bit parallel data after the DEMUX module and transmits 48-bit data at the rising edge of the clock DCO at 250MHz [5]. Its internal structure diagram is as follows:

![ADC internal structure diagram](image)

Figure 3. ADC internal structure diagram.

There are two ADC configuration modes include pin configuration and register configuration. The signal-to-noise ratio achieved by the pin mode in the system is not ideal and the effective bit is more than 8.2 in this mode. The pin configuration can reduce the design difficulty and adapt to the situation where the signal-to-noise ratio is not high. Finally, the register configuration that can adjust the phase error between channels is selected.

5. FPGA digital logic design in mother card

FPGA digital logic includes clock chip and ADC SPI control module, ADC pin configuration module, data receiving module, DDR3 and MAC transmission control module. The differential data signal is converted into a single-ended signal. After zero filling in FIFO48_256, it becomes 256-bit data that can be received by DDR3. FIFO256_256 synchronizes the data to the DDR3 clock domain. DDR3 reads out 256-bit data [6]. After FIFO256_32, the MAC reads out 32-bit transmission data driven by the clock generated by the PLL. Logical structure diagram is shown in Figure 4.

![Logical structure diagram](image)

Figure 4. Logical structure diagram.

ISERDES is the IP core of FPGA. Its maximum bit width allowed is 16 bits, which is increased to 48 bits by modifying its primitives. Asynchronous FIFO solves the issues of data transmission across the clock domain. DDR3 and MAC logic call the IP core, adding the control module. Its reading and writing transmission speed meets the design requirements [7].
6. Test result

The sine wave signal generated by Tektronix AFG3252C passes through narrow-band filters with central frequencies of 150Mhz and 200Mhz respectively and is connected to the input SMA interface of the acquisition card. The test physical map is as follows:

![Physical Prototype](image)

Figure 5. The physical prototype.

Differential nonlinearity (DNL) and integral nonlinearity (INL) are two ADC performance important parameters. DNL and INL of the ADC measured in the experiment are shown in the figure 6. The DNL is roughly between (-0.55, 0.55) and the INL is between (-4,4), which is in line with expectations. This test result is measured just above full scale of the ADC output.

![DNL and INL](image)

Figure 6. Test result of INL and DNL.

After FFT transformation, the time and frequency domain diagram waveform of the 152MHz sine wave sampled by the acquisition card is shown in Figure 7.

![Time and FFT](image)

Figure 7. TIME and FFT test result of 152Mhz signal.
Signal-to-Noise Ratio (SNR) of the signal can be calculated as 57.74dB and the ENOB is calculated by the formula (1) as 9.30bits.

$$SNR = (6.02 \times N + 1.76)dB$$

(1)

After FFT transformation, the time and frequency domain diagram waveform of the 200MHz sine wave sampled by the acquisition card is shown in Figure 8. In this frequency, the ENOB is 9.27bits.

Figure 8. TIME and FFT test result of 200Mhz signal.

The values of ENOB at different frequencies are shown in Figure 9. The results are in line with expectations, which indicates the performance of the acquisition card is stable.

Figure 9. ENOB changes as Fin.

7. Conclusion
The digital acquisition card realizes 1Gsps Analog-to-Digital conversion and controls the receiving, transferring and uploading of data through FPGA. With good static performance, ENOB are all above 9.1bits. The experimental test shows that the acquisition card has engineering application value of high-speed and high-precision sampling. This card completes a set of overall solutions for high-frequency analogy signal acquisition and explains that the FMC interface is feasible in engineering applications. A new solution based on the FMC interface for data acquisition is proposed. The advantage is that the daughter card can update flexibility. Multiple daughter cards can share one mother card to shorten the acquisition card design cycle and reduce costs.

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