ABSTRACT

This paper describes how we successfully used the HPX programming model to port the DCA++ application on multiple architectures that include POWER9, x86, ARM v8, and NVIDIA GPUs. We describe the lessons we can learn from this experience as well as the benefits of enabling the HPX in the application to improve the CPU threading part of the code, which led to an overall 21% improvement across architectures. We also describe how we used HPX-APEX to raise the level of abstraction to understand performance issues and to identify tasking optimization opportunities in the code, and how these relate to CPU/GPU utilization counters, device memory allocation over time, and CPU kernel level context switches on a given architecture.

Keywords Quantum Monte Carlo (QMC) · Dynamical Cluster Approximation (DCA) · Autonomic Performance Environment for eXascale (APEX) · HPX runtime system

1 Introduction

As users move their applications toward accelerated node architectures of different accelerator types and next-generation multi-core systems, they encounter significant challenges in their codes as there are few programming models available on all of these new architectures that can interoperate well with C++ and vendor specific APIs and libraries. Our goal is to examine how successfully we can use the HPX programming model to port codes between architectures, and what lessons we can learn from this experience. HPX also helps raise the level of abstraction in the application’s programming model in order to understand common performance problems across architectures. This helps to identify common optimization opportunities to hide latency, overheads, serializations and wait times while bringing performance improvements “off-the-shelf” to the application originally written using parallelism in C++. In this paper, we explain which performance issues HPX can address and describe how we use it in the DCA++ application, its evaluation on different platforms, and how we can tune it to target multiple platforms. With rapidly changing configurations of highly heterogeneous HPC systems, portability of code and performance of scientific applications is paramount for their software design and development efforts and long sustainability of applications.

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DCA++ (Dynamical Cluster Approximation) is a high-performance research software framework, providing a modern C++ implementation to solve quantum many-body problems [1][2][3]. The DCA++ code currently uses three different programming models (MPI, CUDA, and C++ Standard threads), together with numerical libraries (BLAS, LAPACK and MAGMA), to expose the parallelization in computations.

HPX is a C++ Standard Library for Concurrency and Parallelism [4][5][6][7]. It implements all of the corresponding facilities as defined by the C++ Standard. Additionally, in HPX we implement functionalities proposed as part of the ongoing C++ standardization process.

In this paper, we outline HPX as a potential solution to efficiently porting DCA++ across different architectures.

1.1 Contribution

The primary contributions of this work are outlined below:

(a) Ported DCA++ to various HPC architectures (POWER9, x86_64, ARM64) (see 4.2)
(b) Implemented the HPX threading model for on-node parallelization in DCA++
(c) Profiled DCA++ using performance measurement library APEX, integrated with HPX
(d) Collaborated with APEX performance observation tool team members, providing feedback and driving research
(e) Worked with DCA++ domain science application developers driving their new complex science problems with enhanced optimizations.

2 Background

Quantum Monte Carlo (QMC) solver applications are common tools and mission critical across the US Department of Energy’s (DOE) application landscape. For the purpose of this manuscript the authors choose to use one of the leading QMC applications, developed primarily at Oak Ridge National Laboratory in collaboration with ETH Zürich, the Dynamical Cluster Approximation (DCA++) algorithm. In recent years DCA++ has been ported and successfully optimized across various platforms (on both host side and accelerator based devices). A production scale scientific problem runs on the DOE’s fastest supercomputer, Summit, at Oak Ridge Leadership Facility (OLCF) on all 4600 nodes equipped with ∼28000 NVIDIA Volta V100 GPUs attaining a peak performance of 73.5 PFLOPS with a mixed precision implementation [8].

Although DCA++ has been highly optimized on existing hardware, this is the first effort to focus on the runtime execution level of the application and observe how it performs on each of the already supported systems and newer DOE supported architectures. In this work, the authors enable HPX runtime support to further optimize thread context switching and lower synchronization cost over the usage of C++ standard threads. We further verify such claims using the APEX performance measurement tool.

2.1 DCA++

Dynamical Cluster Approximation (DCA++) is a numerical simulation tool that is used to predict behaviors of quantum materials, such as superconductivity, magnetism, etc. It is an iterative convergence algorithm with two primary kernels: (a) Coarse-graining of the single-particle Green’s function to reduce the complexity of the infinite size lattice problem to that of an effective finite size cluster problem, and, (b) Quantum Monte Carlo (QMC) based solver for the cluster problem.

Most of the application’s performance, workload (computation), memory usage and bottlenecks come from the QMC solver kernel [8]. Fig. 1 shows the on-node (per MPI process) computation structure of a threaded QMC simulation using the custom-made thread pool in DCA++. We initialize several instances of independent Markov chains and distribute across nodes (MPI ranks), each node is responsible for that Markov chain assigned[1] computed by a walker object (producer) and an accumulator object (accumulator) that measures single- and two-particle Green’s functions.

Each object runs on an independent thread and no communication happens between these threads. We run multiple walker threads concurrently, and after each walker finishes a Monte Carlo (MC) update (sampling from the Markov chain), the accumulator is pulled from the head of accumulator waiting queue to compute MC measurement from the

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[1] On systems with the ability to run multiple MPI ranks per node with one or more GPUs per rank, each process is then only responsible for a portion of the chain assigned to that node.
Figure 1: Shows the computation structure of a threaded QMC kernel using the custom-made thread pool in DCA++ running on a single MPI process (rank). We run multiple walker threads concurrently, and after each walker finishes an MC update, an idle accumulator thread is pulled from the head of accumulator waiting queue to compute MC measurement from the walker. After the accumulator finishes its measurement, it’s pushed to the back of the queue.

walker. When each accumulator finishes its measurement, it’s pushed into the back of the queue. The queries to the queue are managed by the synchronization primitives (mutex and conditional_variable).

In this paper the analysis, optimization, and further performance gains will be discussed in reference only to the QMC solver portion of the DCA++ application.

2.2 HPX

HPX is a C++ standard library for distributed and parallel programming built on top of an asynchronous many-task runtime system (AMT). It has been described in detail in other publications [9, 10, 11, 12, 13]. Such AMT runtimes provide a means for helping programming models to fully exploit available parallelism on complex emerging HPC architectures. The HPX runtime includes the following essential components:

- An ISO C++ standard conforming API that enables wait-free asynchronous parallel programming, including Futures, Channels, and other primitives for asynchronous execution. The exposed API ensures syntactic and semantic equivalence of local and remote operations, which greatly simplifies writing complex applications [14, 15].
- A work-stealing lightweight task scheduler [5, 16] that enables finer-grained parallelization and synchronization, exposes greatly reduced overheads related to threading, and ensures automatic load balancing across all local compute resources (see 3).
- APEX [17], an in-situ profiling and adaptive tuning framework (see 2.3).
- In its distributed version (not utilized in the presented work), HPX also features an Active Global Address Space (AGAS) [11, 18] that supports load balancing via object migration and enables runtime-adaptive data placement and distributed garbage collection and an active-message networking layer that enables running functions close to the objects they operate on [5, 19].

In the context of the presented work we use HPX because of its full conformance to the recent C++ standards [20, 21], its reduced thread and synchronization overhead properties, and its sophisticated performance measurement and in-situ profiling capabilities provided by APEX.

2.3 HPX-APEX Integration

APEX [17] (Autonomic Performance Environment for eXascale) is a performance measurement library for distributed, asynchronous multitasking runtime systems such as HPX. It provides support for both lightweight measurement and high concurrency. To support performance measurement in systems that employ user-level threading, APEX uses a dependency chain in addition to the call stack to produce traces and task dependency graphs. APEX supports both
synchronous (so-called \textit{first person}) and asynchronous (\textit{third person}) measurements. The synchronous module of APEX uses an event API and event listeners. Whenever an HPX task is created, started, yielded or stopped, APEX will respectively create, start/resume, yield, or stop timers for measurements. Dependencies between tasks are also tracked.

The asynchronous measurement involves periodic or on-demand interrogation of operating system, hardware or runtime states (e.g. CPU utilization, resident set size, memory “high water mark”). HPX counters (e.g. idle rate, queue lengths) are also captured on-demand on a periodic basis.

APEX has native support for performance profiling, in which all tasks scheduled by the runtime are measured and a report is output to disk and/or the screen at the end of execution. The profile data contains the number of times each task was executed and the total time spent executing that type of task. In order to perform detailed performance analysis involving synchronization and/or task dependency analysis, full event traces including event identification and start/stop times have to be captured. To that end, APEX is integrated with the Open Trace Format 2 [22] (OTF2) library – an open, robust format for large scale parallel application event trace data. OTF2 is a robust reader/writer library and binary format specification that is typically used for high-performance computing (HPC) trace data. In order to capture full task dependency chains in HPX applications, all tasks are uniquely identified by their GUID (globally unique identifier) and the GUID of their parent task. These GUIDs are captured as part of the OTF2 trace output. OTF2 data can be visualized by the Vampir [23] trace analysis tool.

Before the DCA+HPX integration, the \textit{first person} measurement in APEX was only integrated with a handful of technologies, including the HPX runtime and OpenMP 5.0 runtimes that support the OMPT performance tools interface [24]. The \textit{third person} measurement in APEX was mostly limited to extracting data from HPX and the Linux /proc virtual filesystem. Because most of the DCA++ computation is offloaded to GPUs using the CUDA library, APEX was integrated with the CUDA Profiling Tools Interface (CUPTI) [25] and the NVIDIA Management Library (NVML) [26]. Synchronous CUDA API callback timers and some counters (e.g. Bytes transferred, bandwidth, vector lanes) from the CUDA runtime and/or device API are captured synchronously, whereas the NVML counters (e.g. utilization, bandwidth, power) are periodically captured asynchronously. Using APEX GUIDs mapped from CUDA Correlation IDs, the GPU activity such as memory transfers and kernel executions are captured and linked to the host-side tasks that launched them. To provide concurrent use of the GPU hardware, memory transfers between the host and GPU and kernels are executed within logical subdivisions of the device, identified by the device, context, and stream IDs. These IDs are associated with the OTF2 virtual “threads” of execution within the trace data, as shown in Fig. 7.

3 Implementation

In this section, we outline our implementation of the high-level threading abstraction layer in DCA++, which supports standard C++ threading and HPX threading implementations.\footnote{https://github.com/STEllAR-GROUP/DCA/releases/tag/hpx_thread} The design of HPX integration in DCA++ is presented in Fig. 2. Our implementation is non-intrusive to DCA++ code as it does not break the API of the custom-made thread pool and we have not modified original DCA++ workflow. It also allows the application developer to switch between hpx::thread and std::thread via compilation configuration. If user prefers HPX threading option, one needs to turn on DCA_WITH_HPX flag and provide the path of HPX library to the application’s CMake configuration.

![Figure 2: Custom-made thread pool in DCA++ now supports both std::thread (default) and hpx::thread (new feature). Threading options can be toggled at compilation.](https://github.com/STEllAR-GROUP/DCA/releases/tag/hpx_thread)
To parallelize computation tasks, DCA version 1.1.0 implemented a multi-threading strategy using POSIX threads which could cause large overheads when thousands of threads continuously spawned and joined. DCA version 2.0 lowered the overhead with the custom-made thread pool strategy [3] by maintaining constant number of C++ std:: thread objects during the execution. However, the implementation of the custom-made thread pool strategy was designed to spread worker threads to simultaneous multithreading (SMT) or virtual cores. Depending on the architecture of the processor, SMT might be a bottleneck if any of the SMT threads are competing for the shared physical core [27].

We manage to preserve the same API of the ThreadPool implementation in both versions primarily due to the fact that HPX is fully C++ standard conforming. All synchronization primitives of the standard C++ library are still valid in the context of HPX. For the C++ std:: thread version of the thread pool shown in Listing 1, we wrapped all C++ standard synchronization primitives (i.e. condition_variable, lock_guard, future) into a thread_traits class. For the HPX-enabled DCA++ shown in Listing 2 we construct a similar thread_traits class in a separate header file and replace all the C++ standard synchronization primitives with equivalent HPX synchronization primitives.

Listing 1: std:: thread version of the thread pool.

```cpp
namespace dca {
    namespace parallel {

        struct thread_traits {
            template <typename T>
            using future_type = std::future<T>;
            using mutex_type = std::mutex;
            using condition_variable_type = std::condition_variable;
            using scoped_lock = std::lock_guard<mutex_type>;
            using unique_lock = std::unique_lock<mutex_type>;
        };

        class ThreadPool {...};
    }
}
```

Listing 2: hpx:: thread version of the thread pool. Note that for the synchronization primitives implemented in class thread_traits, this version differs from the std:: thread version only by the used C++ namespace hpx.

```cpp
namespace dca {
    namespace parallel {

        struct thread_traits {
            template <typename T>
            using future_type = hpx::future<T>;
            using mutex_type = hpx::mutex;
            using condition_variable_type = hpx::condition_variable;
            using scoped_lock = std::lock_guard<mutex_type>;
            using unique_lock = std::unique_lock<mutex_type>;
        };

        class ThreadPool {...};
    }
}
```

For task-scheduling in the custom-made thread pool implemented in class ThreadPool, the C++ std:: thread version of the thread pool [3] maintains an array of std:: thread objects and array of queues of work items represented by std::packaged_task objects in a simple round-robin fashion; HPX threading version dispatches tasks asynchronously through hpx::async and manages tasks with its runtime scheduler that has various robust task scheduling methods [28].

For thread affinity, the C++ std:: thread version of the thread pool manually sets thread affinity and uses the (SMT) feature to achieve speedup [8]; the hpx:: thread version on the other hand handles these scheduling efforts automatically through its runtime system. HPX by default recognizes existing SMT and sets only one hyper-thread per physical processing unit. The runtime schedules user-level lightweight threads on top of operating system threads, which avoids expensive context switches at kernel-level [16].

HPX-threads are implemented as user-level threads. These are cooperatively (non-preemptively) scheduled in user mode by the HPX-thread manager on top of one OS thread per hardware thread (processing unit). By default, the OS threads have their affinities defined such that they run on one processing unit only. The HPX-threads can be scheduled

[3] https://github.com/CompFUSE/DCA/releases/tag/paper.2019.old_code
[4] https://github.com/CompFUSE/DCA/releases/tag/paper.2019.new_code
without a kernel transition, which provides a performance boost. Additionally, the full use of the OS’s time quantum per OS-thread is achieved even if an HPX-thread blocks for any reason. In that case, other HPX-threads are scheduled to run immediately. The scheduler is cooperative in the sense that it will not preempt a running HPX-thread until it finishes execution or cooperatively yields its execution. This is particularly important, since it avoids context switches and cache thrashing due to randomization introduced by preemption. The default thread scheduler is implemented as a ‘First Come First Served’ scheduler, where each OS-thread works from its own queue of HPX-threads. Other scheduling policies, e.g. supporting thread priorities, are available as well. If one of the cores runs out of work, it starts ‘stealing’ queued tasks from neighboring cores, thus enabling load-balancing across all cores 

4 Results

4.1 Systems overview

For our evaluation, we have used Oak Ridge Leadership Computing Facility’s (OLCF) Summit supercomputer and the Wombat system; and, National Energy Research Scientific Computing Center’s (NERSC) Cori Supercomputer (for this work we used the new CoriGPU partition). Each system was selected due to its host architecture diversity (shown in Table. 1) for comparing the performance of DCA++ using the HPX runtime and visualizing the results collected using APEX and visualized by Vampir.

Summit. [29] is a 4600 node, 200 PFLOPS IBM AC922 system. Each node consists of 2 IBM POWER9 CPUs with 512 GB DDR4 RAM and 6 NVIDIA V100 GPUs with total of 96 GB high bandwidth memory (divided into 2 sockets), all connected together with NVIDIA’s high-speed NVLink.

Table 1: Systems Comparison

| Configuration | Summit | Wombat | CoriGPU |
|---------------|--------|--------|---------|
| GPU           | NVIDIA Volta (6 per node) | NVIDIA Volta (2 per node) | NVIDIA Volta (8 per node) |
| CPU           | IBM POWER9™ (2 Sockets / 21 Cores per socket) | Cavium ThunderX2 (2 Sockets / 28 Cores per socket) | Intel Xeon Gold 6148 (2 sockets / 20 cores per socket) |
| CPU-GPU inter- | NVIDIA NVLINK2 (50 GB/s) | PCIe Gen3 (16 GB/s) | PCIe Gen3 (16 GB/s) |

Wombat. [31] is a 64-bit ARM cluster with 16 compute nodes, four of which have two NVIDIA V100 GPUs attached. Each compute node has two 28-core Cavium ThunderX2 processors (Cavium is now Marvell), 256 GB RAM (16 DDR4 DIMM’s) and a 480 GB SSD for node-local storage. Nodes are connected with EDR InfiniBand (∼100 Gbit/s).

CoriGPU. [32] is a development rack of 18 nodes recently added to the Cori system at NERSC. Each node contains two 20-core Intel Xeon Gold 6148 CPUs with 384GB DDR4 memory and 8 NVIDIA V100 GPUs with 128 GB HBM2 memory (divided into 2 sockets). All GPUs are connected to the CPUs and Infiniband network interface cards via PCIe 3.0.

4.2 Correctness verification across systems

To verify the correctness of our work across various HPC architectures, we follow the standard DCA++ protocol to study superconductivity in the 2D single-band Hubbard model in DCA++. The focus value is the superconducting transition temperature $T_c$, a property of the materials. We choose 100k Monte Carlo measurements as it is representative case to our science problems. The goal is to obtain the same $T_c$ with acceptable statistical noise across all HPC architectures for a specific scientific case as defined under the protocol.

Fig. 3a shows DCA++ with C++ std::thread threading generates consistent results across various platforms. It shows the temperature dependence of the leading eigenvalue $\lambda_\alpha$ of the Bether-Salpeter equation. $T_c$ is the temperature where $\lambda_\alpha(T=T_c)=1$. All $T_c$ are about 0.076 within acceptable statistical range. Similarly, Fig. 3b shows DCA++ with hpx::thread also generates accurate results across multiple HPC architectures. We use the DCA++ application with C++ std::thread threading results obtained from runs on Summit as a referencing result, and compare with all other runs of DCA++ using hpx::thread on various platforms. As one might note that we have obtained the same $T_c$ within an acceptable statistical deviation.

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5 Summit ranked the second place in the TOP500 list in June 2020 [30]

6 https://github.com/CompFUSE/DCA/wiki/Tutorial:-$\Delta T_c$
Figure 3: DCA++ correctness verification across multiple architectures as outlined in Table 1. For our scientific problem we obtain same superconducting transition temperature $T_c$ results (where leading eigenvalue $\lambda_d(T=T_c) = 1$) within acceptable statistical range. For each platform, we compute DCA++ with 100k Monte Carlo measurements (representative case to our science problems) for 5 independent calculations. The random number generator used in all experiments is std::mt19937_64 from C++ library.

4.3 Compare runtime: std::thread vs. hpx::thread

For this comparison analysis we compared a version of DCA++ with C++ std::thread and one with a hpx::thread implementation on a single Summit node with 6 MPI ranks, each rank mapped to 7 physical cores and 1 Volta V100 GPU. More performance analysis (i.e. performance analysis on other machines) will be uploaded to the public repository once available.

https://github.com/STEllAR-GROUP/dca
Fig. 4 shows DCA++ with hpx:: thread achieves 21% speedup over the one with C++ std :: thread version. The same improvement is also observed in the distributed runs as well. The speedup is mainly due to faster thread context switching and reduced scheduler and synchronization overheads in the HPX runtime system (see Section [3]). Fig. 5 verifies the speedup and shows by the end of the execution, hpx:: thread version has much less (∼ 2 × lower) voluntary context switches (639 times) relative to std :: thread version (1454 times) and ∼ 4 × lower non-voluntary context switches (18 times) relative to std :: thread version (70 times). For the non-voluntary context switches observed in hpx:: thread version, we consider these are most likely caused by the synchronization introduced by CUDA itself as CUDA synchronization is still happening on pthread level.

Figure 4: Time-to-solution for 100k Monte Carlo measurements with error bars obtained from 5 independent executions on Summit. Using the hpx:: thread implementation we observe up to 21% speedup over the C++ std :: thread version. Observed performance gain is due to faster context switch and scheduler and less synchronization overhead in HPX runtime system. Lower is better.

Figure 5: Comparison of non-voluntary and voluntary context switches using the APEX performance measurement counters when executing DCA++ with C++ std :: thread and hpx:: thread versions on Summit. We observe that the hpx:: thread implementation has much less context switches than std :: thread in DCA++ and aides to the performance gains in using HPX over std :: thread. Lower is better.

Fig. 6 was generated using the NVIDIA Nsight Systems on Summit. The figure shows two different threading affinity strategies adapted in C++ std :: thread (left) and hpx:: thread version (right) in DCA++. Each row in the figure represents average hardware thread utilization. The height of the hardware thread utilization is represented by the height of the black histogram.

For our test case we set the SMT to 4 for both executions. The C++ std :: thread version uses 4 hardware threads per physical core; while, HPX-enabled DCA++ by default utilizes only one hardware thread per physical core. Also, if we combine the adjacent 4 hyper-threads (SMT) for each physical core in C++ std :: thread version, the overall utilization is not as high as in the hpx:: thread version. Moreover, even if the DCA++ is modified to use the same affinity settings (which requires explicit changes in the code base) as HPX, the performance is not improved (i.e. the affinity settings do not cause the speedup of HPX). The reason of the speedup is due to the fact that HPX thread management (and context switching in particular) exposes less overheads and lower synchronization overheads. With faster context switch from HPX threads, DCA++ is able to feeds more computing workload into GPU faster. This directly increases the GPU utilization resulting in the observed performance improvement.
We further verified that thread caching malloc (i.e. tcmalloc) is not the cause of the speedup with hpx:: thread version which uses tcmalloc. TCMalloc assigns each thread a thread-local cache and reduces lock contention for multi-threaded programs[33]. We performed LD_PRELOAD tcmalloc for DCA++ std :: thread version, and the execution time remains the same as the one without tcmalloc. This finding strengthens our conclusion that the 21% speedup seen for the hpx:: thread version is due to the fact that user-level context switching is more efficient and synchronization with HPX threads imposes less overhead (see Fig. 4).

4.4 HPX-APEX Profiling Analysis

APEX was originally designed to be integrated with the HPX runtime, and enabling APEX support is straightforward. When configuring HPX, flags are passed to CMake in order to enable APEX support and provide the path to library dependencies such as OTF2, CUPTI and NVML. After configuration, build and installation the HPX runtime will have APEX performance measurement enabled. As mentioned in Section 2, all HPX tasks are timed by APEX. In addition, tasks defined in the application can be annotated to provide unique labels using the hpx:: annotated_function facility in HPX. At runtime, different APEX features (e.g. tracing, output summary format, different counter sets) are enabled/disabled through the use of environment variables, a configuration file, or the APEX programming interface.

For the experiments described below, APEX collected a full event trace to OTF2 and monitored several HPX, operating system, CPU and GPU utilization counters. Counters that were particularly useful for these experiments include kernel-level context switches (both voluntary and not), user and system level CPU utilization, GPU utilization and memory consumption, HPX idle rates and queue lengths.

We traced DCA++ with APEX on Summit as shown in Fig. 7. We are able to annotate any functions with hpx:: annotated_function function wrapper in the code to distinguish their execution time in final profiling data. Here we annotate walker and accumulator functions, as they are the most computation-intensive parts in DCA++ code. From Fig. 7b one can clearly observe that the walker function takes majority of the time in a single DCA++ run. The profiling measurement library can also gather HPX thread idle rate (as seen in Fig. 8a) and queue length (as seen in Fig. 8b). The idle rate counter indicates how utilized each of the HPX worker threads are during each sampled time period (lower is better). In the context of HPX, it is not a problem having the shown queue lengths as creating and managing HPX threads (tasks) is generally very cheap (less than 1 \(\mu s\) per thread). The queue depth indicates how much work, in the form of queued tasks, is available for each of the worker threads. The counters are collected on a per-worker basis, and the values shown here represent averages across all worker threads.
In [8] authors reported that while storing two-particle green function $G_{tp}$ on the device allows condensed matter physicists to explore larger and more complex (higher fidelity) science problems, but we are limited to the device memory size. The data of device memory usage from HPX-APEX shown in Fig. 9 can help us track memory usage and provide computational scientists guidance on how to address memory-bound challenge as defined in [8]. We are planning to distribute $G_{tp}$ across nodes and implement a token ring algorithm to transfer single-particle Green’s function $G$ between nodes. The implementation will take advantage of high-speed network between devices available on the machine (i.e. NVIDIA NVLink on Summit) in order to transfer device data efficiently.
5 Conclusion

In this paper we used the Dynamical Cluster Approximation (DCA++) one of the leading Quantum Monte Carlo solvers as a research vehicle to test the feasibility of the HPX runtime system and use the abstraction layer in the programming model to understand the performance bottlenecks across multiple architectures (both host side and accelerator based devices).

We observed significant performance benefit (~21% speedup over standard threads) by just using the HPX threading model due to the faster context switches and lower synchronization overheads guaranteed by the HPX runtime. In this work we also validated our claims using the APEX performance measurement library and with the HPX-APEX integration one can observe in-depth analysis of the threading behavior (e.g., CPU / GPU utilization counters, device memory allocation over time, kernel level context switches and more).

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