Resistive switching behavior of SiO$_x$ layers with Si nanoparticles

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Abstract: First results on resistive switching in SiO$_x$ film containing crystalline silicon nanoparticles are reported. SiO$_x$ layers ($x = 1.15$) with thickness of 50 nm were deposited on n-Si crystalline substrates and annealed for 60 min at 1000°C to grow crystalline nanoparticles. Part of the samples were annealed in an inert atmosphere, while the rest were subjected to a two-step (O$_2$+N$_2$/N$_2$) annealing process. Current-voltage (I-V) characteristics were by applying positive or negative voltage to the top contact. For both types of samples the I-V characteristics were asymmetric with lower currents measured at negative voltage, especially in the case of two-step annealed samples. In most of the N$_2$ annealed structures switching behavior high-low/low-high resistance state was observed in both polarities at voltages with amplitudes in the range (2 - 4) V. Uncontrolled switching low/high resistance was also seen, more frequently at positive voltages. In contrast, the two-step annealed samples showed stable behavior. The transition high-low resistance state was achieved by negative voltages in the (-2, -5) V range leading to an increase of the current by more than three orders of magnitude. The structures were reset to the high resistive state, by positive voltage in the range (3 - 4) V. Uncontrolled switching was not observed in the two-step annealed samples for both polarities and they showed higher reliability regarding the number of switching cycles.

1. Introduction

Resistive random access memory (RRAM) has drawn significant interest as a promising candidate for next generation nonvolatile memory due to its potential scalability beyond 10 nm feature size, fast switching speed, low operating power, and good reliability as compared with flash memory [1,2]. Large number of metal-oxide-metal (MIM) structures with CMOS (complementary metal-oxide-semiconductor) compatible metal oxides have been studied for memory switching properties (Al$_2$O$_3$, MoO$_3$, Ta$_2$O$_5$, NiO, TiO$_2$, WO$_3$, HfO$_2$, ZrO$_2$ etc.). Most of these MIM structures show bipolar switching and their behavior depends on both the metal oxide composition and the metal contacts used.

Resistive switching and related nonlinear conduction have also been observed in SiO$_x$, $x \approx 2.0$ layers sandwiched between two poly-Si layers [3]. SiO$_x$ resistive switching memory is attractive for its fully CMOS compatible material composition and processing [4]. Moreover SiO$_2$ is a conventional material with high availability and ease of integration with current and future technology platforms. Most
RRAM devices using SiO$_x$ as the active switching medium have unusual electrical characteristics where resistive switching only occurs in non-oxidizing ambient and a unique unipolar operation. Two types of resistive switching memory have been demonstrated based on SiO$_x$ (x $\approx$ 2.0). The first type relies on the formation and rupture of metal filament injected from the electrode and it features bipolar switching behavior. The second type normally shows unipolar current-voltage (I-V) characteristics with the reset voltage larger than the set value. This type of resistive switching is an intrinsic property of SiO$_x$ (x $\approx$ 2.0) and it is electrode-independent [5]. The intrinsic resistive switching in metal-free silicon oxide offers a simpler route to integration with CMOS technology.

The mechanism of the intrinsic resistive switching in SiO$_x$ is characterized as filament conducting. In electroforming stage, voltage bias application causes formation of conductive filament(s). The real-time formation and evolution of filament in a silicon oxide resistive switch has been imaged through in situ transmission electron microscopy [6]. It has been revealed that the electroforming process involves the local enrichment of silicon from the silicon oxide matrix. Semi-metallic silicon nanocrystals have been observed, which can account for the conduction in the filament. Joule heating at higher currents disrupts the filaments, returning the system to the high resistance state. The switching between high resistance state (HRS) and low resistance state (LRS) occurs at an electroforming voltage ($V_{ef}$) which is an important parameter for SiO$_x$ RRAM application. Lower $V_{ef}$ is demanded since a large electroforming voltage will increase the consumed power and will decrease the overall memory density. The underlying cause for the resistive switching in the SiO$_x$ (x $\approx$ 2) layer can be induced by unintended factors, such as defects in SiO$_x$ surface, pores, material-assisted local electric-field enhancement, current local heating, etc. [3,7].

In the RRAM devices using SiO$_x$ (x $\approx$ 2) as the active switching medium the resistive switching only occurs in non-oxidizing ambient [3,4,8-10]. The operation of such a device is possible only under vacuum due to oxidation of silicon conductive pathways on the device surface under ambient conditions. A study of resistive unipolar switching in a silicon-based ITO/n-poly-Si/SiO$_x$/p-Si device in which the active layer is silicon-rich silica (SiO$_x$, x < 2.0) has demonstrated that in contrast to other work in the literature, switching in that device occurred in ambient conditions, and was not limited to the surface of the active material [11]. A switching mechanism driven by competing field-driven formation and current-driven destruction of filamentary conductive pathways has been proposed. It has been assumed that conduction is dominated by trap assisted tunneling through noncontinuous conduction paths consisting of silicon nano-inclusions in a highly nonstoichiometric suboxide phase. It has been found that the reset currents were higher in devices annealed at 950°C. In those samples a high density of silicon nano-inclusions can exist within the SiO$_x$ film as a result of phase separation allowing highly conductive pathways to occur.

In this paper initial results on resistive switching in SiO$_x$ film containing crystalline silicon nanoparticles are reported. SiO$_x$ layers (x = 1.15) with thickness of 50 nm were deposited on n-Si crystalline substrates by thermal evaporation of SiO in vacuum and then annealed in an inert atmosphere for 60 min at 1000°C in order to grow Si nanocrystals. The switching behavior has been studied by measuring DC current-voltage (I-V) characteristics metal/oxide (SiNCs-SiO$_x$)/n-Si (MOS) structures. In contrast to [11], bipolar switching behavior has been observed.

2. Experimental details

Silicon-rich SiO$_x$ layers with initial composition x = 1.15 and thickness of 50 nm were deposited on n-type (100) crystalline silicon (c-Si) substrates ((4-6) $\Omega$·cm) maintained at room temperature. Thermal evaporation of SiO at a vacuum of $1 \times 10^{-3}$ Pa was used for the film preparation [12]. The deposition rate and film thickness were monitored by a calibrated quartz microbalance system. The silicon wafers were cleaned chemically prior to film deposition by applying a standard procedure for the microelectronics industry. All as-prepared layers were annealed at 250°C for 30 min in an Ar atmosphere to ensure good film stability at ambient conditions. This annealing does not lead to phase separation and Si nanoparticle formation [12]. Silicon nanocrystals (NCs) were grown in a SiO$_x$ matrix by furnace annealing at 1000°C in a nitrogen or nitrogen + oxygen/nitrogen atmosphere for 60 min.
Our previous results have shown that annealing of SiO$_{1.1}$ under these conditions leads to phase separation and formation of silicon nanocrystals with diameter of $\sim$ 5-6 nm [13,14] in a SiO$_2$ matrix [15,16]. The thickness of the oxide formed between the nanocrystals and the adjacent films is $\geq$ 3 nm. It has also been observed that the N$_2$ annealed samples the Si nanocrystals grown in the region close to the top surface ($\sim$ 5-6 nm) get transformed into SiO$_2$ due to native oxide formation after exposure to air [16]. The two-step thermal treatment, first in an O$_2$+N$_2$ (10 min), followed by N$_2$ annealing leads to formation of $\sim$ 15 nm SiO$_2$ region close to the top surface [17].

After the furnace annealing metallization was carried out through a mask and top electrodes (referred from now on as gates) of the MOS capacitors were formed with area of $\sim$ 2 $\times$ 10$^{-3}$ cm$^2$. Aluminum and gold were used as top-contact metals for the N$_2$ and O$_2$+N$_2$/N$_2$ annealed samples, respectively. Aluminum electrode was also prepared on the bottom side of the silicon substrate. DC current-voltage characteristics were measured by using Semiconductor Characterization System Keithley 4200-SCS with preamplifiers. The hold and delay times of all measurements were 5 and 1 s, respectively. The polarity of the applied voltage given below refers to the top electrode.

3. Results and Discussion

Typical current-voltage (I-V) characteristics of a N$_2$ annealed Al/c-Si/SiO$_2$-Si/Al structures are shown in figure 1. The numbers in the figure denote the sequence of the measurements. There were no longtime pauses between the measurements of the consecutive curves. As seen from the figure switching from low conductive to high conductive state is observed both on applying positive and negative voltage on the top electrode. A large number (more than 15) of samples were studied and it has been found that the voltage at which the switching takes place is not constant; it varies in the range (2 - 5) V. The current increase is normally about 3 orders of magnitude. It has to be noticed that the switching process is better controlled on applying negative voltage. The number of the observed switching cycles from HRS to LRS and back is small (less than 10) and finally the structures remain in the LRS.

![Figure 1. Current-voltage characteristics of an Al/c-Si/SiO$_2$-Si/Al structure prepared by annealing in nitrogen at 1000°C for 60 min. The numbers in the figure denote the sequence of the measurements.](image)

Figure 2 shows three curves measured first on increasing the applied negative voltage from 0 V to (-6) V (curve 1) and then going back from (-6) V to 0 V (curves 2, 3). It illustrates that uncontrolled switching from LRS to HRS may take place when a negative voltage is applied. During the voltage scan corresponding to curve 2 the MOS structures remains at LRS, while at one of the next scans it spontaneously switches from LRS to HRS (curve 3). No such spontaneous switching has been found on applying positive voltage but again uncontrolled transfer from LRS to HRS was observed in many
samples; for example curves 2, 3 and 4, 5 in figure 1. Hence, the experiments on this group of samples have shown two drawbacks, which make these structures not prospective for memory applications: (i) small number of switching cycles and (ii) uncontrolled return to the low conductive state.

Figure 2. Current-voltage characteristics measured on an Al/c-Si/SiO2-Si/Al structure showing a controlled switching from high resistive to low resistive state (curve 1) and uncontrolled switching from low resistive to high resistive state (curve 3).

It is seen from figure 1 that the I-V characteristics in the high resistive state are nearly symmetric while in the low resistive state they are asymmetric - on applying the same voltage the current is significantly higher when the gate voltage is positive. Assuming that the current through the oxide layer is due to electrons injected from the c-Si substrate at positive voltage and from the top Al contact at negative voltage, the observed symmetry for the low conductive state can be understood keeping in mind that the energy barriers at both interfaces are nearly equal in the case of stoichiometric SiO2 (~3.1 eV for the Si/SiO2 interface and ~3.2 eV for the Al/SiO2 one) and supposing that they remain close to each other for SiO2-Si NCs composite layers. As a possible explanation of the I-V characteristics asymmetry in the high conductive state one can consider the following idea, though other reasons cannot be excluded. According to the accepted mechanism of the intrinsic resistive switching in SiOx, in electroforming stage voltage bias application causes formation of filament (or filaments) which include highly conductive silicon nanocrystals. The band gap of silicon nanocrystals, due to the quantum size effect, is larger than that of bulk crystalline silicon but much smaller than the band gap of SiO2. Hence, the barrier height at both interface c-Si/SiNCs and Al/SiNCs may be quite different (this point will be explored in a further work).

Based on the accepted switching mechanism in SiOx and keeping in mind the experimental results in figure 1, one can assume that the Al/c-Si/SiO2-Si NCs/Al structures, if further optimized by varying the size and density of Si NCs and/or the contact type to avoid the uncontrolled return to the HRS, could be used as memory elements by applying an appropriate negative voltage on the gate electrode to switch from HRS to LRS and a positive voltage for the LRS to HRS switching.

In order to reduce to some extent the current at negative applied voltages and thus to avoid the uncontrolled filament “burning”, a SiO2 layer was formed by the two-step annealing process described in the Experimental details section. This layer can limit the electron injection from the top electrode and one can expect elimination of the spontaneous return to the HRS. Also the Al top contact was replaced by Au ones. These changes lead to another type of metal/insulator interface compared to the Al/SiO2-Si NCs one. Figure 3 shows current-voltage characteristics of an Al/c-Si/SiO2/SiO2-Si/SiO2/Au structure prepared by a two-step annealing at 1000°C. As seen from the figure the first switching at negative voltages (forming process) occurred at (-5) V. The following switching processes, as can be expected, take place at lower voltage, though some variations in the switching voltage still exist. They could be related to charge trapping in the top SiO2 layer produced by 10 min annealing of SiO1.15 at 1000°C in an O2+N2 atmosphere. For producing of top dioxide layer with a
higher quality, optimization of the annealing procedure should be carried out or separate SiO₂ deposition on top of the SiO₂-Si NCs layer may be applied (for example by chemical vapor deposition or sputtering).

It is important that the current increase with the voltage is significantly slower than that in figure 1 and no uncontrolled switching was observed at negative applied voltages in all samples studied. Based on the results obtained on a large number of samples one can conclude that a voltage of (-5) V can ensure a controllable switching between HRS and LRS. It is demonstrated in figure 3 that the structures can be reset to the initial HRS in a controllable way by applying positive voltages higher than 3 V. The currents measured in the HRS were in the range (10⁻¹² – 10⁻¹⁷) A, while the current measured in the LRS was above 10⁻⁸ A at all switching cycles. No uncontrolled switching was observed for the positive polarities, as well, and the samples showed higher reliability regarding the number of switching cycles. These results indicate that the O₂+N₂/N₂ structures with a gold top contact are promising for resistive memory applications.

Figure 3. Typical current-voltage characteristics of an Al/c-Si/SiO₂/SiO₂-Si/SiO₂/Au structure prepared by a two-step annealing at 1000°C. The numbers in the figure denote the consequence of curve measurement. For curves with the same numbers first a scan at negative voltages was applied and then at positive ones.

Figure 4 shows a comparison between two HRS/LRS transitions performed with scans from 0 to (-3) and (-4) V, curves 1 and 5, respectively. The LRS curve measured after the (-4) V voltage scan (curve 6) has the typical shape of a low resistance characteristic with currents between (10⁻⁹ – 10⁻⁸) A at voltages in the (-0.5) – (-2) V range. In contrast, the (-3) V scan leads to smaller currents in the 0 - (-1.5) V range (curve 2) resulting in a not well defined ‘current window’ (the currents measured in the 0 - (-2) V range). The next scan (curve 3), performed in the low resistive state, up to (-4) V stabilizes the LRS and the next curve 4 coincides with curve 6. These results demonstrate that voltages higher than (-4) V are required in order to realize reliable switching and high quality information storage.

4. Conclusions

Initial results have been reported on resistive switching in Al/c-Si/SiO₂-Si/Al and Al/c-Si/SiO₂/SiO₂-Si/SiO₂/Au structures containing crystalline silicon nanoparticles. Current-voltage characteristics taken at room temperature in air were asymmetric with lower currents measured at negative voltage, especially in the case of the samples from the second group (two-step annealed). Switching from high resistive state to low resistive state was observed in both groups of structures when applying both positive and negative voltage with amplitudes in the range (2 - 5) V to the top contact. In structures from the first group, annealed in N₂, uncontrolled switching from LRS to HRS was seen, more frequently at positive voltages indicating that this type of structures have to be further optimized to be suitable for resistive memory applications.
In the two-step annealed samples the transition from high to low resistance state was achieved by applying negative voltages and a current increase of more than three orders of magnitude was observed. The structures were repeatedly reset to the initial, highly resistive state, by applying positive voltage in the range (3 – 4) V. Uncontrolled switching was not observed for both polarities. The stable behavior of the ‘O2+N2/N2’ samples i.e. the higher reliability regarding the number of switching cycles and the absence of uncontrolled switching makes these structures promising for memory applications.

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