High-Density Qubit Wiring: Pin-Chip Bonding for Fully Vertical Interconnects

M. Mariantoni\textsuperscript{1,2} and A.V. Bardysheva

\textsuperscript{1}Institute for Quantum Computing, University of Waterloo, 200 University Avenue West, Waterloo, Ontario N2L 3G1, Canada
\textsuperscript{2}Department of Physics and Astronomy, University of Waterloo, 200 University Avenue West, Waterloo, Ontario N2L 3G1, Canada

(Dated: October 22, 2018)

Large-scale quantum computers with more than $10^5$ qubits will likely be built within the next decade. Trapped ions, semiconductor devices, and superconducting qubits among other physical implementations are still confined in the realm of medium-scale quantum integration ($\sim 100$ qubits); however, they show promise toward large-scale quantum integration. Building large-scale quantum processing units will require truly scalable control and measurement classical coprocessors as well as suitable wiring methods. In this blue paper, we introduce a fully vertical interconnect that will make it possible to address $\sim 10^5$ superconducting qubits fabricated on a single silicon or sapphire chip: Pin-chip bonding. This method permits signal transmission from DC to $\sim 10$ GHz, both at room temperature and at cryogenic temperatures down to $\sim 10$ mK. At temperatures below $\sim 1$ K, the on-chip wiring contact resistance is close to zero and all signal lines are in the superconducting state. High-density wiring is achieved by means of a fully vertical interconnect that interfaces the qubit array with a network of rectangular coaxial ribbon cables. Pin-chip bonding is fully compatible with classical high-density test board applications as well as with other qubit implementations.

Keywords: Quantum Computing; Scalable Qubit Architectures; High-Density Wiring; Pin-Chip Bonding; Fully Vertical Interconnects; Rectangular Coax Ribbon Cables; Superconducting Qubits; Large-Scale Quantum Computers

I. INTRODUCTION

Practical quantum computers are closer to reality than ever before \cite{1}. Among a variety of physical implementations \cite{2}, those based on superconducting quantum circuits \cite{3, 4} show promise for the realization of medium-scale quantum computers comprising on the order of 100 qubits \cite{5, 6}. It is expected that these computers will allow us to tackle problems with real-world applications, such as the quantum simulation of chemical reactions, quantum-assisted optimization, and quantum sampling \cite{7}. Most importantly, medium-scale quantum computers will serve as a test bed for quantum error correction (QEC) algorithms \cite{8}. These algorithms will make it possible to build a fault-tolerant digital quantum computer and, thus, to harness the full power of quantum algorithms \cite{9}. Building a useful, QEC-based quantum computer will require large-scale quantum integration (LSQI), where quantum processing units (QPUs) are comprised of two-dimensional qubit arrays with $\sim 10^5$ qubits.

Superconducting quantum circuits are planar devices fabricated from aluminum (Al) thin films deposited on silicon (Si) substrates and patterned by means of photolithography techniques similar to those used in classical integrated-circuit technology. The Al films are patterned to realize capacitive and inductive elements, $C$ and $L$, respectively. These elements can be used to implement harmonic oscillators, i.e., linear resonators. A nonlinear inductor can be realized by means of a Josephson tunnel junction, which comprises a pair of Al islands separated by an ultra-thin insulating layer of Al oxide. A suitable combination of linear and nonlinear circuit elements allows us to implement anharmonic oscillators, i.e., nonlinear resonators. Linear and nonlinear superconducting resonators are designed to have a resonance frequency $f_0$ in the microwave range, typically $f_0 \in [5, 10]$ GHz. Thus, they can be controlled with signals similar to those used in mobile telephones. Circuit operation at DC is also required in certain designs.

Microwave resonators can be prepared in the quantum regime by cooling them to a temperature $T \sim 10$ mK in a dilution refrigerator (DR) and limiting their population to the lowest quantum-mechanical states $\{|0\rangle, |1\rangle, |2\rangle, \ldots \}$. Low temperatures are required to reduce superconductor excitations (quasiparticles) and thermal noise. In the case of nonlinear resonators, it is possible to isolate states $|0\rangle$ and $|1\rangle$ from all higher states, thus forming a qubit. One of the most widely used superconducting qubits is the transmon qubit \cite{10}, where an $\sim 100$ nm$^2$ Al island is connected to a pair of $\sim 100$ nm$^2$ Josephson tunnel junctions. To date, “Xmon-type” transmon qubits \cite{11} have been used to realize a QPU comprising a one-dimensional array of nine qubits integrated on a single chip \cite{12}. Moreover, transmon qubits are at the core of the medium-scale quantum computers that are being developed by IBM Q, Google Santa Barbara, Intel-Delft, and Rigetti \cite{5, 6, 13, 14}.

The two main challenges to move from medium- to large-scale quantum computers are low error rates and true scalability \cite{15}. These two objectives must be developed simultaneously, as progressively scalable control
and measurement classical coprocessors and qubit wiring methods have to be compatible with high-fidelity qubit operations (e.g., one- and two-qubit gates and qubit measurement). In this blue paper, we introduce a fully vertical interconnect that will make it possible to address $10^6$ superconducting qubits fabricated on a single Si or sapphire chip: Pin-chip bonding. This method permits signal transmission from DC to $\sim 10$ GHz, both at room temperature and at cryogenic temperatures down to $\sim 10$ mK. At temperatures below $\sim 1$ K, the on-chip wiring contact resistance is close to zero and all signal lines are in the superconducting state. High-density wiring is achieved by means of a fully vertical interconnect that interfaces the qubit array with a network of rectangular coaxial ribbon cables. Pin-chip bonding is fully compatible with classical high-density test board applications as well as with other qubit implementations. Here, we focus on superconducting qubit applications as they set very stringent specifications, therefore representing an excellent benchmarking platform.

II. QUBIT WIRING: STATE OF THE ART AND CHALLENGES AHEAD

Arguably, the first method that made it possible to wire up superconducting QPUs with $\sim 100$ qubits has been the quantum socket [17]. Traditional wiring methods based on wire bonds [18] allow accessing the QPU only laterally, through the four edges of the QPU chip. The quantum socket is based on a vertical wiring approach and, thus, permits us to reach any area on the chip surface. The vertical wires are realized as spring-loaded micro coaxes, i.e., custom-made Pogo pins, which can carry signals in the microwave range as well as DC with low loss. The quantum socket has been used routinely to measure high-quality planar superconducting resonators [19] as well as qubits [20].

Vertical connectivity is one of the main innovations introduced by the quantum socket. However, the dimensions of the Pogo pins are too large to extend the socket to large-scale quantum computers. In fact, fabricating even smaller Pogo pins that those used in the works of Refs. [17][20] is challenging. The presence of the springs in the Pogo pins, in particular, makes further miniaturization exceedingly hard. Due to this limitation, the footprint of one fully coaxial Pogo pin assembly with characteristic impedance $Z_c \approx 50 \Omega$ is $\approx 1$ mm. This dimension can be reduced to $\approx 0.5$ mm by making an assembly with $Z_c \approx 25 \Omega$. Considering the largest Xmon transmon qubit is $\sim 500 \mu m \times 500 \mu m$ [12], the Pogo pin approach will not allow for high-density wiring as the smallest fully coaxial Pogo pin assembly is larger than the footprint of one (large) qubit. Additionally, the Pogo pin approach in the work of Ref. [20] interfaces a Pogo-pin array and the qubit control and measurement network by means of a printed circuit board connected to a high-throughput commercial connector. The work in Ref. [17], instead, interfaces the Pogo pins with EZ 47 coaxial cables. Both approaches effectively increase significantly the wiring footprint when interfacing the QPU with the qubit control and measurement network and, thus, are not suitable for a large-scale quantum computer.

In an effort to develop more scalable qubit wiring methods, MIT Lincoln Laboratory and Google Santa Barbara have built multi-chip QPUs where flip-chip technology is used to bond a chip with qubits (quantum chip) to a chip with control and measurement circuitry (classical chip) [21][22]. A typical bonding procedure consists of:

1. Patterning a two-dimensional array of indium (In) bumps on the top surface of the classical chip, with mating In pads on the bottom surface of the quantum chip;
2. flipping the quantum chip over the classical chip and aligning the two chips;
3. compressing the two chips with a pressure $p \in (10, 20) N \text{mm}^{-2}$.

Indium bumps are pillars up to $30 \mu m$ tall with pre- and post-compression diameters $d = 15 \mu m$ and $d = 30 \mu m$, respectively. Flip-technology makes it possible to access qubits in two-dimensional arrays, an otherwise impossible task using only wire bonds. However, it still relies on wire bonds that are ultimately used to interface the four edges of the classical chip with the control network. Wire bonds are used even in the most recent proposal on qubit wiring and integration by MIT Lincoln Laboratory [23].

Given $n_w$ wire bonds per chip edge, the total number of wires available with flip chip is $N_w = 4n_w$. On the other hand, the total number of qubits in a two-dimensional array is $N_q = n_q^2$, where $n_q$ is the number of qubits per chip edge. The linear scaling of the wires fails to match the quadratic scaling of the qubits, therefore limiting flip chip to medium-scale QPUs.

Present implementations of flip chip can potentially be extended to large-scale QPUs with $\sim 10^5$ qubits if it were possible to include one controller per qubit on the classical chip (similar arguments would apply to a qubit measurer), fulfilling three conditions [24]:

1. Qubit and controller have similar physical footprints;
2. each controller dissipates a power $P_c \sim 1$ nW;
3. controllers are heavily demultiplexed (DEMUXed).

Two types of cryogenic controllers have been proposed, single flux quantum (SFQ) [24] and cryo-CMOS [25]. McDermott et al. have shown that for the former $P_c \sim 100$ nW and for the latter $P_c \sim 10$ pW. Hence, both proposals suggest to operate the controller system at the 3 K stage of a pulse tube cooler, which has a cooling power of $\sim 1$ W but is $\sim 1$ m away from the quantum chip.

This approach thus hinders the use of flip chip, unless it were possible to devise a multi-chip QPU where the quantum chip is operated at $\sim 10$ mK, the classical
chip (with controllers) at 3 K, and the two chips are separated by an interposer chip for heat shielding. Assuming 100% heat shielding from the interposer substrate, metalized through-silicon vias (TSVs) will be needed to connect the classical and quantum chip vertically. Using niobium-titanium (Nb-Ti) for the vias, the heat load on the quantum chip would be $\sim 20 \text{ mW}$ [24], which is likely too high even for a specially designed DR.

Lastly, we could elect to operate the entire QPU at 3 K and refrigerate the quantum chip to $\sim 10 \text{ mK}$ by means of some sort of resolved-sideband cooling (microwave-induced cooling) [29], possibly followed by algorithmic cooling [27]. However, this approach will result in a significant runtime overhead in the quantum computation as well as, likely, one- and two-qubit gates with higher error rates. Therefore, a fully vertical wiring method with footprint smaller than the qubit footprint and uniform throughout the entire control and measurement network is highly appealing.

In this work, we show that it is possible to fabricate a fully coaxial pin-chip assembly with a footprint of 0.4 mm and $Z_c \approx 50 \Omega$ or 0.2 mm and $Z_c \approx 25 \Omega$. Additionally, we show that such a footprint can be maintained throughout the entire control and measurement network, if pin-chip is suitably interfaced with a network of rectangular coaxial ribbon cables.

### III. PIN-CHIP BONDING FOR FULLY VERTICAL INTERCONNECTS

In order to better understand the limitations of flip chip and the advantages of pin-chip bonding, we need to first outline the fundamental conditions for dense qubit wiring. As an example, consider a square qubit array, where each qubit has a footprint $\ell^2 = 500 \mu \text{m} \times 500 \mu \text{m}$, as in the work of Ref. [12] [28], with a qubit pitch $p_q$ equal to the qubit lateral dimension $\ell_q$, $p_q = \ell_q$. Further consider a square wire array with wire pitch $p_w$. In the case of flip chip, the minimum $p_w$ is set by the smallest available Al or gold (Au) bonding wire with diameter $d = 18 \mu \text{m}$ [29]. Since the qubit control signals are in the microwave regime, they must be carried by suitable transmission lines. Thus, it is necessary to use at least three bonding wires (two grounds and one signal) next to each other to realize such a line. Assuming an optimistic spacing of 10 $\mu \text{m}$ between adjacent wires and sharing grounds between two adjacent transmission lines, we obtain $p_w = 56 \mu \text{m}$.

The **first condition** for dense qubit wiring is

$$\frac{p_w}{p_q} \leq 1,$$

i.e., the overall wire lateral dimension cannot be larger than the qubit dimension. This condition can easily be fulfilled in the case of flip chip. The **second condition** applies to square wire arrays with lateral access, as flip chip, imposing a constraint on the lateral dimension of the quantum chip, $\ell$,

$$N_q \equiv \left( \frac{\ell}{p_q} \right)^2 \equiv 4 \frac{\ell}{p_w} \equiv N_w. \quad (2)$$

In Eq. (2) we assume only one wire per qubit (i.e., a significant DEMUX). The nontrivial solution to Eq. (2),

$$\ell = \frac{4}{p_w} p_q \quad (3)$$

is the intercept between the linear scaling curve of the wires and the quadratic scaling curve of the qubits. Notably, this condition does not prescribe a practical method to reach any qubit in the array, providing instead an upper bound for $N_q$. For an optimistic implementation of flip chip with $p_q = 500 \mu \text{m}$ and $p_w = 56 \mu \text{m}$, we obtain $\ell \approx 18 \text{ mm}$ that corresponds to $N_q = 1296$. This is the maximum number of qubits that makes sense to address using flip chip. For any given larger chip there would not be sufficient wires on the chip edges to address all qubits on a two-dimensional array. Flip chip is thus confined to the realm of medium-scale QPUs.

Figure 1 shows a schematic representation of the qubit wiring method proposed here, pin-chip bonding for fully vertical interconnects, which will make it possible to implement large-scale QPUs. This method is based on rectangular coaxial ribbon cables attached to micro-sized pins, forming coaxial transmission lines by means of an interposer block; the tip of each pin is bonded vertically to mating pads on the quantum chip using In. The quantum chip is patterned with a square array of $[5, 30] \mu \text{m}$ thick circular pads made from In with $d_{pad} \in [100, 200] \mu \text{m}$; the In pads can be fabricated above an underlying Al thin film, or other films. Each pad is electrically connected to an on-chip Al (or Nb) trace used to reach a qubit. The pad array is in a one-to-one correspondence with a mating pin array. Each pin is $\sim [15, 25] \text{ mm}$ long and has a core made from SUS 304 Austenite stainless steel (or similar) with $d \in [8, 178] \mu \text{m}$, coated first with a $\sim 1 \mu \text{m}$ thick titanium nitride (TiN) film and then with a $10 \mu \text{m}$ thick (or possibly thicker) In film resulting in $d_{pad} = d_{pin}$. The TiN coating, which can be applied using physical vapor deposition, guarantees that microwave signals are carried within a superconducting region at $T \sim 10 \text{ mK}$ and acts as an interdiffusion barrier [22], if necessary. The In film can be applied by means of thermal evaporation [other materials such as tin-lead (Sn-Pb) eutectic alloys may be used] and serves as the bonding agent between pin and pad.

We fabricate rectangular coaxial ribbon cables, each consisting of a $20 \mu \text{m}$ thick flexible polyimide tape coated with a $250 \text{ nm}$ thick Nb film (similar to the work in Ref. [16]). This film is patterned to form a set of parallel transmission lines in a coplanar waveguide (CPW) design, which are then coated with a $10 \mu \text{m}$ thick (or possibly thicker) Sn-Pb film. The pins are attached to the cables following this procedure:
FIG. 1. Overall view of pin-chip bonding for fully vertical interconnects, with cross-section of the interposer block showing the channels and through holes where the ribbon cables are inserted. Salmon: Polyimide tape. Dark gray: Nb films. The PTFE spacers (dark gray) sandwich a STYCAST block (yellow). Pins are white. On the quantum chip: Violet is Si; middle-metallic gray is Al; white is In (curbs).

1. The ∼10 mm tail of each pin is placed on one signal trace of a ribbon cable.

2. Another ribbon cable is flipped over and aligned with the underlying cable with a vertical offset of ∼1 mm, exposing part of its bottom;

3. The cable-pin-cable assembly is compressed and soldered in a reflow oven at $T \gtrsim 183^\circ C$, with the front segment of each pin free hanging at the bottom of the assembly [see Fig. 2(a) and (b)].

After the reflow step, In solder balls with $d \lesssim 50 \mu m$ are pressed on the exposed conductor of the ground traces, each of width $G = 50 \mu m$. The In balls are placed on the ground traces by means of an XY stage equipped with micro tweezers.

Note that a slight tapering of the transmission line on the ribbon cables must be engineered in order to transition smoothly from the cable region overlapping with the circular pin to the flat cable region. This taring allows us not to increase the wiring footprint [see Fig. 2(b)].

To form a coaxial transmission line and perform pin-pad alignment we fabricate an interposer block made of, e.g., oxygen-free high thermal conductivity (OFHC) copper (Cu), where a square array of through holes
FIG. 2. The three main elements of pin-chip bonding. (a) One ribbon cable forming a cable-pin-cable assembly. A row of In solder balls is shown. (b) Same as (a), but without the front cable, exposing pins, polyimide tape, and metallic film; only the first pin is shown. The CPW tapering at the top of each pin is visible. (c) Cross-section of the interposer block: Top view. (d) Cross-section of the interposer block: Bottom view. (e) Pin-chip bonding on the quantum chip. The color coding is as in Fig. 1.
each with \(d_{\text{hole}} \in [200, 300] \mu m\) is made by way of fast hole drilling electrical discharge machining. Each row of holes resides at the bottom of a channel of width \(\gtrsim [140, 240] \mu m\) and depth \(\sim 1 \text{ mm}\) [see Fig. 1 and Fig. 2 (c)]. The channel (groove) is fabricated by means of single-point diamond turning (SPDT) [30], which provides extremely high nanometric accuracy and precision and allows to trench narrow channels in Cu and possibly other materials. The aspect ratio of our channels is at a minimum \(\sim 140 \mu m/1 \text{ mm} = 0.14\), which is not terribly hard to achieve with SPDT. Boss extruders or dowels are used to align the interposer to a sample holder housing the quantum chip.

The exposed part of a cable-pin-cable assembly is inserted in one of the channels, with the front segment of each pin threaded through a matching hole in the interposer. Prior to pin insertion, the holes are filled with, e.g., STYCAST 1266 A/B [31], which has a relative electric permittivity \(\varepsilon_r \approx 3\). Two polytetrafluoroethylene (PTFE) spacers [see Fig. 2 (c) and (d)] are used to separate the pin from the hole’s wall, realizing a coaxial transmission line. During insertion the pins are protected by means of a \(\sim 250 \mu m\) thick photoresist film; the photoresist on the pin’s tip is stripped prior to bonding (the resist on the exposed part of the pin simply adds to the coaxial transmission line dielectric). After a curing step at \(T \approx 60 ^\circ C\), the entire assembly is heated in a vacuum oven at \(T \gtrsim 157 ^\circ C\), soldering the In balls to one wall of the channel. A dielectric spray or filling (grease) is used to isolate the exposed part of the transmission lines from the interposer block. The tip of each pin is adjusted to be flush with the interposer bottom surface [see Fig. 2 (d)]. All tips must be aligned vertically with a tolerance of at least \(\pm 2.5 \mu m\) pushing the pin array onto mesa stops patterned on an auxiliary Si chip. This chip is eventually substituted with the quantum chip when performing the actual pin-chip bonding step.

Note that many rows of rectangular coaxial ribbon cables will be in close proximity when wiring a large two-dimensional array of qubits. In order to shield adjacent cable rows and avoid large inter-cable crosstalk, the two outer surfaces of each polyimide tape must be coated with a \(250 \mu m\) thick Nb film. This conductive (superconducting below \(T \approx 9.2 K\)) film not only acts as an electromagnetic shield between adjacent cable rows, but also effectively results in a stripline transmission line [32]. This helps mitigate significantly the intra-cable crosstalk between adjacent transmission lines on the same tape due to a field confinement between the signal trace and outer ground larger than between the signal trace and lateral CPW grounds.

Depending on the chosen pin diameter, the characteristic impedance of the coaxial transmission line in the interposer is \(Z_c \approx [24, 14] \Omega\). We propose to depart from \(Z_c = 50 \Omega\) currently used for qubit control lines and resort to smaller impedances, where the inner conductor diameter is maximized for mechanical robustness and the outer conductor diameter is reduced to obtain smaller lines. We note that the vast majority of the control electronics used for medium-scale quantum computers is already fully custom made and, thus, can be designed with practically arbitrary values of \(Z_c\).

The bonding procedure is realized as follows:

1. The thin In oxide layer on the pin’s outer surface is etched with hydrochloric acid [33] and the In oxide film on the pad with a plasma etch [22];

   (a) *Conical bonding* (see Fig. 3 left) is realized with a sharp conical pin tip that penetrates into the In layer of the pad. In this case, the pin outer surface should not be coated with In and pre-bonding oxide cleaning may be unnecessary. Using a similar pressure per pin as for flip chip, our experience with Pogo pins [17] indicates that the pin will puncture only the first \(\lesssim 1 \mu m\) of a 10 \(\mu m\) thick In pad;

   (b) Alternatively, *Spherical bonding* (see Fig. 3 right) is realized using a rounded spherical pin tip that is compressed onto the underlying pad with a similar pressure as for flip chip, corresponding to \(\approx 280 \text{ to } 560 \text{ g per pin/pad. This pressure, which is comparable to that used in our previous work on Pogo pins [17], will not damage the pins;}

2. In both bonding procedures, a 20 kHz ultrasonic signal can be applied to ease pin-pad connection;

3. Standard In bump bonding as in flip chip is used for the ground connections at the quantum chip level. The bottom surface of the interposer block is coated with a \(\sim 10 \mu m\) thick In film that is bonded to an In curb on the ground planes of the quantum chip [see Fig. 2 (d) and (e)]. The PTFE spacers are flush with the uncoated Cu surface of the interposer block.

We note that, in the case of conical bonding, the pin may be coated with In or Al, the latter being stronger and more resilient during piercing. It is well known that Al
diffuses very rapidly into In [34], thus permitting an excellent electrical connection. Both Al and In films must be cleaned from their native oxide layers prior to piercing.

IV. CONCLUSION

In the case of an interconnect with full vertical access, as for pin-chip bonding, when \( \frac{p_w}{p_q} \leq 1 \) the second condition on dense wiring reduces to

\[
N_q = \left( \frac{\ell}{p_q} \right)^2 \leq N_w = \left( \frac{\ell}{p_w} \right)^2.
\]

without any constraint on \( \ell \). Considering the dimensions provided above, we find that the maximum number of qubits is limited by the qubit size: for a square chip out of a 12 in wafer, \( \ell = 200 \text{ mm} \) and, thus, \( N_q = 160000 \). This is a factor of more than 100 larger than for flip chip and, e.g., it will make it possible to implement \( \sim 80 \) quantum error corrected qubits [35], a remarkable number to start realize useful quantum algorithms.

Note that, in the case of flip chip, it is impractical to adopt a very large chip. A 200 mm\(^2\) chip, for example, would correspond to \( N_w = 4 \times 200 \text{ mm}/56 \text{ pm} = 14286 \) using optimal flip chip dimensions. In this case, the qubit pitch should be \( p_q \approx 1.7 \text{ mm} \) to fully take advantage of the chip size. Such a qubit spacing could be realized by means of qubit-resonator-qubit cells, where the resonator acts as a coherent qubit spacer. However, microwave planar resonators are bound to lengths in the few millimeter range due to their wavelength, typically larger than 1.7 mm. For instance, in the IBM Q quantum chip [20], the qubits are spaced by \( \approx 3.5 \text{ mm} \); in this case, we find \( N_q = (200 \text{ mm})^2/(3.5 \text{ mm})^2 = 3270 \). More compact coherent spacers may be realized using lumped element LC resonators or planar resonators with much higher resonance frequency. In all these cases, however, the spacer impact on qubit gate fidelities may be important.

Lastly, it is worth mentioning that rectangular coaxial ribbon cables can easily be engineered to embed attenuators and filters along the transmission lines, without impacting the wiring footprint. For example, Au or palladium traces can be added where required to form the large resistors used in attenuators. Infrared filters can be realized by altering the polyimide tape with a magnetically loaded black dye or a thin paint (or spray). Bundles of ribbon cables can be then pressed laterally in correspondence with attenuators or filters and heat sunk to the various stages of the DR.

ACKNOWLEDGMENTS

We thank our fruitful discussions with David P. DiVincenzo about qubit operation at 3 K as well as Bluhm’s group for discussions about heat shielding interposer chips.
John M. Martinis, “Qubit metrology for building a fault-tolerant quantum computer,” Quantum Science and Technology 3, 014005 (2018).

R. Das, J. Yoder, D. Rosenberg, D. Kim, D. Yost, J. Mallek, D. Hover, V. Bolkhovsky, A. Kerman, and W. Oliver, “Cryogenic qubit integration for quantum computing,” in 2018 IEEE 68th Electronic Components and Technology Conference (ECTC) (2018) pp. 504–514.

R McDermott, M G Vavilov, B L T Plourde, F K Wilhelm, P J Liebermann, O A Mukhanov, and T A Ohki, “Quantum-classical interface based on single flux quantum digital logic,” Quantum Science and Technology 3, 024004 (2018).

B. Pátra, R. M. Incandela, J. P. G. van Dijk, H. A. R. Hoomul, L. Song, M. Shahmohammadi, R. B. Staszewski, A. Vladimirescu, M. Babaie, F. Sebastian, and E. Charbon, “Cryo-cmos circuits and systems for quantum computing applications,” IEEE Journal of Solid-State Circuits 53, 309–321 (2018).

Sergio O. Valenzuela, William D. Oliver, David M. Berns, Karl K. Berggren, Leonid S. Levitov, and Terry P. Orlando, “Microwave-induced cooling of a superconducting qubit,” Science 314, 1589–1592 (2006).

http://science.sciencemag.org/content/314/5805/1589.full.pdf

Daniel K. Park, Nayeli A. Rodriguez-Briones, Gunaru Feng, Robabeh Rahimi, Jonathan Baugh, and Raymond Laflamme, “Heat bath algorithmic cooling with spins: Review and prospects,” in Electron Spin Resonance (ESR) Based Quantum Computing edited by Takeji Takui, Lawrence Berliner, and Graeme Hanson (Springer New York, New York, NY, 2016) pp. 227–255.

Note that, pin-chip bonding is not limited to this specific qubit footprint. Smaller qubit footprints and different qubit designs can be considered as well.

See, e.g., http://www.scanditron.com/sites/default/files/material/heraeus_bondingwire_brochure.pdf or https://www.cirex.com/wire-bonding/

See, e.g., http://research.physics.illinois.edu/berzyadin/labprotocol/stycast1266.pdf

Robert E. Collin, Foundations for Microwave Engineering - 2nd Edition (Institute of Electrical & Electronics Engineers (IEEE), Inc., and John Wiley & Sons, Inc., New York, NY, and Hoboken, NJ, USA, 2001).

IEEE, Inc., and John Wiley & Sons, Inc., New York, NY, and Hoboken, NJ, USA, 2001).

Teresa Brecht, Yiwen Chu, Christopher Axline, Wolfgang Pfaff, Jacob Z. Blumoff, Kevin Chou, Lev Krayzman, Luigi Frunzio, and Robert J. Schoelkopf, “Micromachined integrated quantum circuit containing a superconducting qubit,” Phys. Rev. Applied 7, 044018 (2017).

C. R. H. McRae, J. H. Béjanin, C. T. Earnest, T. G. McConkey, J. R. Rinehart, C. Deimert, J. P. Thomas, Z. R. Wasilewski, and M. Marianioni, “Thin film metrology and microwave loss characterization of indium and aluminum/indium superconducting planar resonators,” Journal of Applied Physics 123, 205304 (2018).

Austin G. Fowler, Matteo Marianioni, John M. Martinis, and Andrew N. Cleland, “Surface codes: Towards practical large-scale quantum computation,” Phys. Rev. A 86, 032324 (2012).