Synthesis and Optimization of Multi-Objective Multi-Output QCA Circuit using Genetic Algorithm

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Abstract—The physical limitations of CMOS technology triggered several research for finding an alternative technology. QCA is one of the emerging nanotechnologies which is gaining attention as a substitute of CMOS. The main potential of QCA is its ultra low power consumption, less area overhead, and high speed. Majority and inverter gates are the basic gates in QCA, which together work as a universal logic gate to implement any QCA circuit. This paper proposes an efficient methodology for optimal QCA circuit synthesis of arbitrary multi-output boolean functions. A multi-objective genetic algorithm based approach is used to reduce worst case delay and gate count of a QCA circuit. Different importance is given to worst case delay, no. of majority functions. A multi-objective genetic algorithm based approach is used to reduce worst case delay and gate count of a QCA circuit. The obtained results with the existing best techniques indicates, the proposed technique outperforms in terms of worst case delay and gate count.

Index Terms—Quantum-Dot Cellular Automata (QCA), Genetic Algorithm (GA), Optimization, Multi-output, Multi-objective, QCA-circuit

I. INTRODUCTION

THE traditional Complementary Metal Oxide Semiconductor (CMOS) technology is approaching towards the edge of its saturation level in terms of feature size and power efficiency, further improvement may not be possible due to physical limitations [1]. Finding an alternative technology is a prime concern of current research. For the past few years, Quantum-Dot Cellular Automata (QCA) technology has been gaining attention as an alternative to CMOS technology due to its low power overhead and area efficiency [2]. QCA cells are the basis of any QCA device. Information transfers from cell to cell through coulombic repulsion, no current flow occurs during information passing. So QCA circuits require very less power to operate. The fundamental elements in QCA technology are majority voter (MV) gate, inverter (INV) gate, and QCA wire. The set of majority and inverter gate works as a universal logic gate to design any QCA circuit.

Automatic design synthesis and optimization of the layout is a well-studied topic on general AND/OR gate based logic circuits [3], [4]. The minimal Sum of Product (SOP) or Product of Sum (POS) expressions is generally applied to implement the optimal layout of the logic circuits. But the QCA majority logic is different than AND/OR logic, so it is difficult to apply the minimal SOP or POS expression for implementation of the optimal QCA circuit. Previously, some research work has been carried out towards the automatic generation of optimal layout of a QCA circuit. But most of them has various limitations in different measures, like no. of input variables, no. of outputs and optimization criterion. Only a few attempts have been made which try to consider all these issues. The attempts are good in their own perspective, but still they are lacking at some points especially in optimization criterion. So, it is worth to present a technique considering all these aspects for optimal synthesis of QCA circuit. Heuristic based approach seems to be a good choice in the context of the current problem.

Genetic Algorithm (GA) which is based on the theory of natural evolution is well known for finding the optimal solution of NP problems. GA for its ability to find a globally optimal solution and less implementation overhead is a good candidate for heuristic search [5].

This paper propose a technique for the optimal synthesis of QCA circuit, especially multi-output QCA circuit based on GA. All the major optimization parameters like gate count, maximum clock delay are taken into consideration during the synthesis process. The proposed technique is applicable to single as well multi-output functions with arbitrary no. of input variables. The major contributions of this paper are summarized below

• An efficient fitness calculation approach is adopted for measuring the effectiveness of the candidate solutions. Importance is assigned to the different optimization criteria (gate and level) according to their cost in the QCA circuit. A relative fitness function is used to obtain a globally optimal solution for multi-output functions.

• An elitism based multi-objective GA is used to find the globally optimal solution in terms of gate count and maximum clock delay. Some improved techniques are used in different steps (i.e. Creation of the initial population, crossover, mutation) of GA for better performance. Additional methodologies are applied to reduce any redundancy in the obtained solution.

• Finally, simulation is performed on some standard functions. Comparison of the results with the available existing techniques indicates a significant improvement in terms of gate count and maximum clock delay.

The leftover paper is structured as follows. Section II describes the related background materials. Section III presents a brief literature review. In section IV the proposed technique is described. Section V contains the simulation results and comparisons. Section VI concludes the paper.

II. BACKGROUND MATERIALS

A. Quantum Dot Cellular Automata

1) QCA Basics: QCA is one of the emerging nanoelectronic technologies, which works based on the coulombic
Electron Quantum Dot

(a) QCA Cell

(b) QCA Logic Values

Fig. 1: QCA Basics

repulsion between electrons [6]. Each QCA cell contains four quantum dots and two free electrons trapped inside it. The four dots are positioned in four corners of a cell. In the most stable state due to coulombic repulsion the free electrons may move into two corner quantum dots along either of the two diagonals. In this way, in stable condition, a QCA cell may stay as either one of the two possible states. The two states are represented by $P = +1$ and $P = −1$ respectively, and considered as logic 1 and logic 0 respectively [7].

A QCA cell and its states are shown in Fig. 1a and Fig. 1b respectively.

The state of a QCA cell can be changed by simply applying negative or positive voltage on the cell. The signal propagates into the neighboring cells by reordering electron’s position due to coulombic repulsion.

2) QCA Fundamental Devices: Basic QCA gates are majority voter and inverter gate. Equation of a 3 input majority gate is

$$F = PQ + QR + RP$$  \hspace{1cm} (1)

Assuming $P$, $Q$, $R$ as inputs and $F$ as output. A majority voter gate is shown in Fig. 2a. The output of the majority gate depends upon the majority of the inputs, it yields logic 1 as output if at least 2 of the inputs are 1 and yields logic 0 if at least two of the inputs are 0 [8]. OR gate and AND gate can be implemented using majority voter simply by fixing one of the inputs to logic 1 and logic 0 respectively. Inverter gate takes only one input and produce its complement as output. Different variants of the QCA inverter gate are shown in Fig. 2b ((i)-(iii)).

QCA wire is used to propagate a signal from one point of the circuit to another point. QCA wire is formed by cascading QCA cells. A QCA wire is shown in Fig. 2c. The signal applied to one end of a QCA wires propagates to another end through re-positioning the electrons inside the QCA cells. Any complex QCA circuit can be formed by using majority and inverter gates connecting with QCA wires.

3) QCA Clocking: Clocking is used to synchronize and control the signal flow in different parts of a QCA circuit. To get the intended result, direction and timing of signal can be controlled through clocking. A QCA clock has 4 phase switch, hold, release and relax. In switch phase, the inter-dot barrier gradually starts increasing. In hold phase QCA cell holds the same state as the applying signal. In release phase, the inter-dot barrier starts decreasing and in relax phase the cell remains in the unpolarized state. A QCA circuit is divided into several clock zones as required. Cells in the same clock zone are driven by the same clock. Increasing the number of clocks increases the worst case delay of the circuit. Phases of a QCA clock are shown in Fig. 3.

B. Genetic Algorithm

GA is based on Darwin’s theory of natural evolution [9]. This algorithm proved to be very useful for finding a feasible solution of NP problems within a limited number of computations. At first, a set of random individual solutions (chromosomes) is created, called initial population. For measuring the feasibility of each individual a fitness is assigned to each individual. Next generation population is created through selection, crossover, and mutation. The selection function selects some parent chromosomes for crossover based on a selection criterion. Crossover function is used to generate new offspring chromosomes from parent chromosomes. Mutation is introduced to maintain variations in the population pool. Mutation is performed to a chromosome by a specified probability to introduce new characteristics. The algorithm iterates
several times until the goal achieved or the maximum number of iterations reached.

III. PREVIOUS WORKS

Several research papers have been proposed to synthesis and optimize conventional AND/OR-based logic circuits [10–12] but comparatively less number of works done to optimize QCA circuits. Zhang et al. [13] was the first to propose a method for automatic synthesis of optimal QCA circuit. The proposed method was based on Boolean Algebra and applied to generate optimal QCA circuit of 3 variable boolean functions by reducing no. of majority gates. The authors introduced 13 standard 3 variable functions, which were capable of synthesis all the 3 variable functions. Walus et al. [14] improved the technique of [13]. Implementation of the 13 standard functions using the improved method resulted QCA circuit with comparatively less number of majority gates. Kong et al. [15] deployed an algebraic method to systematically synthesis optimal QCA circuit for any 3 variable functions. They performed a cost analysis of a majority circuit and set priority to majority, inverter and level corresponding to their cost factor.

Optimization of QCA circuit using GA was first proposed by Bonyadi et al [16]. A chromosome was represented using a tree structure, where internal nodes represent majority or inverter gates and leaf nodes represent constant or variable. Node count was used as a measure to reduce no. of gates in a chromosome. This method can be used for a function with an arbitrary number of inputs. Implementation of some standard functions using this technique resulted major improvements in terms of gate count. Houshmand et al. [17] extended the work of [16] and proposed a method to reduce gate count in multi-output functions. They showed that for multi-output functions considering individual output may not lead to an optimal result, so in their technique, the circuit for n-th output function is optimized considering the previous n-1 outputs.

Rezaee et al. [18] extended the method proposed in [17] to reduce both gate counts and worst case delay of multi-output functions. Optimization of worst case delay was performed by optimizing the height of the chromosome tree. To calculate the fitness value the no. of gates and the height of the chromosome tree were treated with equal importance. They did not consider any methodology to eliminate redundancies present in a chromosome. Another major attempt to optimize multi-output QCA circuit was made by Tehrani et al [19]. They considered reducing gate count and worst case delay together as their objective. Their main focus was to reduce the no. of levels in the chromosome tree and totally ignored the no. of inverter gates, providing the reason that some of the implementations of inverter gate contain very few cells and it is not required to change the clock phase for an inverter (i.e inverter does not affect the speed). But the most stable representation of inverter gate (shown in Fig. 2.b.(ii)) contains a considerable amount of cells, so though it does not affect the speed of a circuit it affects the area. However, for multi-output functions they did not synthesis the n-th output function considering previous n-1 outputs, they stored the best chromosomes for each output and the set with the highest number of common gates selected as the best global solution.

IV. PROPOSED METHOD

It is clear from the previous works discussed in earlier section that still there are some important issues that need to be explored to synthesis the optimal solution. In the proposed work an improved technique is presented to automatically synthesis the optimal QCA circuit. The final solution is presented as a combination of majority and inverter blocks.

The overview of the proposed technique is presented as a flow diagram in Fig. 4.

Each output of a multi-output function is considered as an individual function, for example for a full adder two functions are required one for sum and another for carry. To apply the process first the output functions are ranked randomly as 1,2,3...N. The process begins with generating some random individual solutions each representing a valid QCA circuit. A fitness value is assigned to each individual for measuring the optimality of the solution. Some individual solutions with best fitness are selected as elite chromosomes to pass into the next generation without any alteration. Using tournament selection some parents are selected for crossover. A variant of uniform crossover is used to a pair of parents for generating child chromosome. Finally the leftover chromosomes are generated through mutation to keep the population size constant. Combination of elite chromosomes, crossover children and mutation children form the next generation population pool. This process repeats several times until the termination condition is reached. For multi output circuit the whole process is repeated for each output, distinct set of rules is used for fitness calculation of first output function and for the functions other than first output. The process returns the best combined solution satisfying all the outputs. Details of each step of the proposed approach are discussed below

A. Creation of Initial Population

An individual chromosome (solution) is represented using the conventional tree structure [16]. Internal nodes of the tree represent the majority or inverter gate and leaf nodes represent constant or variable. An individual chromosome (solution) is represented using a tree structure, where internal nodes represent majority or inverter gates and leaf nodes represent constant or variable. Node count was used as a measure to reduce no. of gates in a chromosome. This method can be used for a function with an arbitrary number of inputs. Implementation of some standard functions using this technique resulted major improvements in terms of gate count. Houshmand et al. [17] extended the work of [16] and proposed a method to reduce gate count in multi-output functions. They showed that for multi-output functions considering individual output may not lead to an optimal result, so in their technique, the circuit for n-th output function is optimized considering the previous n-1 outputs.

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To generate an individual chromosome first the majority, inverter and input variables are mapped into distinct integers (i.e. $MV \rightarrow 7$, $Inv \rightarrow 6$, $A \rightarrow 5$ etc.). A random string using the set of mapped integers is generated through following the rules

1) To start the process an integer from the set of mapped integers is chosen at random.

2) If the current number denotes a majority gate then 3 additional numbers are added following the current number in the sequence, if it denotes an inverter gate then one additional number is added following the current number. This rule is recursively applied to each number generated in the string. If the current number denotes an input variable or constant, then no more additional number is required.
Boolean functions representing the outputs

Run GA for 1st output using fitness1

Select output \((i) = 2\)

\(i \leq \text{no. of outputs (n)}?\)

update output \(i = i + 1\)

Satisfies one of the termination conditions?

Best fitness value < 1?

Store the combined chromosome set with best fitness value

Select best ‘e’ chromosomes as elite chromosomes

Create random initial population

Calculate fitness value using fitness2

Perform tournament selection for crossover

Perform random crossover on the selected parents

Remove redundancy from crossover children

Generate random chromosomes for mutation children

Create next generation population combining elite chromosomes, crossover and mutation children

update generation \(g = g + 1\)

Return the best chromosome set

Terminate the process

Fig. 4: Major steps of the proposed technique

Fig. 5: Tree Representing Chromosome \(M(M(B', C, O)A, 1)\)

3) If the string length is greater than a specified length then it is discarded and a new one is generated.

Validating the above rules bound the generated string to represent a valid QCA circuit. The string of integer is mapped into the corresponding QCA circuit.

For creating the set of initial population a set of chromosomes sized 10 times of the population size is generated first. Structurally Similar chromosomes are removed from the set to maintain variations. From the chromosome set, number of chromosomes same as the population size is randomly selected to fill the set of initial population.

B. Fitness Calculation

To calculate the fitness value the target function is represented by its canonical form. For example the 3 variable SOP expression \(AB + B'C\) is represented in its canonical form as \(ABC + ABC' + AB'C + A'B'C\). As mentioned earlier, two
distinct approaches are used to calculate fitness value, one for the first output function and another for the output functions other than first output.

Fitness value calculation for first output (fitness1) is represented in Fig. 6 same algorithm can be used for single output functions. The fitness function has two goals, the first goal is to synthesize a QCA logic circuit corresponding to the output function. To achieve this goal, the fitness function assigns better fitness value to a chromosome, which is closer to the valid solution. In our convention lower fitness value implies better solution. Fitness value is calculated as the ratio of no. of possible inputs using the input variables (i.e for n variable function no. of possible inputs = 2^n) and the no. of outputs similar to the target output function. A fitness value of 1 (i.e. 'temp_fit' = 1) indicates the chromosome represents a valid solution.

The second goal of the fitness function is to synthesize the optimal circuit. Once the valid solution is generated, the fitness function tries to minimize the no. of the gates and worst case delay of the circuit. Minimization of worst case delay is realized by reducing no. of levels in the circuit. No. of level is measured in terms of the no. of majority along the longest path from root to leaf node of the chromosome tree. Majority gate has 3 inputs, one output, so, synchronization is required for proper functioning of the gate, whereas inverter gate, having only one input and one output is not required to synchronize. Thus the inverter gate does not have much impact on delay. So inverter gates are not considered for counting the level. Increasing the level indicates increase in delay as well as area, [i.e. It increases no. of majority] which implies no. of levels is the most important factor to minimize. It was shown in [15], for optimization of QCA circuit, level is the most important factor followed by no. of majority. No. of inverter has lowest importance. The same is followed in the proposed technique. The fitness function implicitly assigns more importance to level than no. of gates. As level is calculated in terms of no. of the majority along the longest path of a QCA circuit, so no. of level cannot be more than the no. majority in a chromosome and in most of the practical circuit no. of level is less than no. of gates in a chromosome. So the value of the 'fitness' (Fig. 6) is more sensitive to the no of level than no. of gates.

For the output functions other than the first output a slightly modified version of the fitness function is used. The algorithm is named as fitness2 and represented in Fig7. To synthesis a valid chromosome corresponding to the output function, same steps as fitness1 is followed. The algorithm differs from fitness1 in next steps. A variable 'stored_fitness' is maintained throughout the process to store fitness of chromosomes with fitness value less than 1. In future, if the same chromosome is used again, its fitness value is just returned from 'stored_fitness'. This strategy reduces the computation overhead. If the current chromosome represents a valid circuit ('temp_fit = 1') and it's fitness value is not present in the 'stored_fitness' then the for loop is executed to calculate the fitness value. A matrix variable 'stored_chromosomes' stores chromosome from previous outputs. Suppose the rank of current output function is i, then each row entry of the 'stored_chromosomes' stores a chromosome set from 1 to i-1 th output, information about the no. of unique majority and inverter gates and maximum level of the chromosome set. The i th output function is optimized considering the previous i-1 outputs. For common gates between the output functions instead of repeating the common parts, both the functions can use the common parts. The common parts are checked in terms

1: Input: Chromosome
2: Return: Fitness Value
3: temp_fit ← No. of possible input
4: if temp_fit == 1 then
5: fitness ← 1 - \( \frac{1}{\text{No. of gates} + \text{No. of levels}} \)
6: else
7: fitness ← temp_fit
8: end if
9: return fitness

Fig. 6: Pseudo code for fitness1

Fig. 7: Pseudo code for fitness2
of their K-map value. To select a chromosome set of previous outputs for combining with the current chromosome, the no. of majority and inverter gets along the common parts of the previous chromosome set is subtracted from no. of majority (i.e. total_majority) and inverter (i.e. total_inverter) respectively. As circuit of an individual output function is considered as a part of the single combined circuit, so all the circuits have to operate under the same clocking scheme. Thus the worst case delay of the combined circuit depends upon the maximum worst case delay among all individual circuits. So maximum level among all the output functions is considered to measure worst case delay.

For choosing the chromosome set of previous outputs to combine with current chromosome maximum pressure is given to level. The set that minimizes the maximum level is chosen first. No. of majority and inverter is used to break a tie among the chromosome sets having a similar maximum level. No. of the inverter is given as one-third of the priority of no. of the majority as the majority has three inputs and one output and it requires to synchronize [15]. The no. of 'total_gates' is counted as the summation of no. of the majority with the one-third of the no. of the inverter. The combined chromosome set providing a minimum value of 'total_gates' is selected among the chromosome set having a similar maximum level. Once a previous chromosome set is finally selected, the common parts between the current chromosome and the previous chromosome set are replaced with the common part having minimum no. of gates. Then the no. of total gates and maximum level are calculated to determine the fitness value. The combination process for a two output function is shown in Fig. 8. As \( M(M(B, C, 0), A, A') \) and \( M(B, C, 0) \) has same K-map value but the 2nd one having less number of gates is selected to form the combined chromosome set.

### C. Selection of chromosomes

An elitism based approach is used to preserve the chromosomes with the best fitness. The chromosomes are sorted according to their fitness value and from the sorted list a small number of chromosomes (i.e. the number is predetermined) with better fitness value are forwarded into the next generation without any alteration. The tournament selection method is used for selecting parent chromosomes for crossover. No. of chromosomes similar to tournament size is selected at random. From the selected chromosomes the chromosome with best fitness value is finally picked. The tournament selection method is performed several times until the parent chromosome list for crossover is filled.

### D. Crossover

No. of Parent chromosomes twice of the size of crossover children is selected through selection method. From the parent chromosome list, two parents are selected at random to generate a single child chromosome. To perform crossover a node from parent1 and another node from parent2 are selected randomly. The selected nodes are exchanged along with their subtree to generate two offspring. Finally, the offspring with best fitness value is taken as child chromosome. n offspring chromosomes are generated from 2n parent chromosomes. Crossover operation between two parents is shown in Fig. 9 (a-b).

### E. Mutation

As the number of inputs in majority gate and inverter gate are different, so it is very difficult to use conventional mutation functions, because replacing an inverter gate with majority or reverse may lead to an invalid QCA circuit. So a different approach is used for mutation. The mutation children are not generated from the current population, they are generated externally and added to the next generation population set. At first a large set of chromosomes is generated randomly using the same procedure used for initial population. From the generated chromosome set, number of chromosomes equal to the no. of mutation children are selected at random and forwarded to the next generation population pool as mutation children.

The complete algorithm is shown in Fig. 10. After Crossover another step is added called 'local_improvement' to remove any redundancy from the generated offspring. This step tries to remove redundant inverter gates and try to replace majority gate with variable or constant having similar functionality. For example, replace \( M(A, B, 1') \) by \( M(A, B, 0) \), replace \( M(A, A, 1) \) by \( A \).

![Fig. 8: Combination process of a two output function](attachment:image.png)
than a dynamic approach is used to terminate the process. Generated early before approaching the maximum generation loop iterates for the 2nd to last output. The inner for loop i-1 outputs are stored in puts. The combined best chromosomes of ith output with best chromosome satisfying all the outputs. Output, the outer for loop breaks and returns the combined the ‘thresh_gen’ no. of consecutive generations. After the last no improvement in terms of best fitness is found throughout generations reached or after generating a correct chromosome output. The inner for loop iterates till the maximum no of current population pool with better fitness are selected as parents. After generation of new offspring. Tournament selection method with size crossover and leftover chromosomes are generated using mutation. Tournament selection method with size 3 is used to select parent chromosomes for creating new offspring. After generating the first valid chromosome corresponding to the SOP expression, the mutation rate is reduced through adopting a higher crossover rate of 80%. In case the valid solution is generated early before approaching the maximum generation then a dynamic approach is used to terminate the process.

Once a valid chromosome is generated a periodic checking is performed, if no improvement in terms of best fitness is gained throughout 300 consecutive generations then it stops execution.

Simulation has been performed with some standard functions. The simulation results and comparison using best available techniques are presented in Table [I-V]. Presented results demonstrate that most of the time the proposed method outperforms the existing best techniques. The important parameters used for comparison are the total majority (TMV), total inverter (TINV), total gates (TG) and maximum level.

V. SIMULATION RESULTS AND ANALYSIS

The proposed algorithm is implemented using Matlab. Simulation has been performed with a population size of 200 chromosomes. 10% of the total chromosomes in the current population pool with better fitness are selected as elite chromosomes. The process iterates till a maximum of 5000 generations. Initially, 70% of the next generation chromosomes excluding elite chromosomes are generated through crossover and leftover chromosomes are generated using mutation. Tournament selection method with size 3 is used to select parent chromosomes for creating new offspring. After generating the first valid chromosome corresponding to the SOP expression, the mutation rate is reduced through adopting a higher crossover rate of 80%. In case the valid solution is generated early before approaching the maximum generation than a dynamic approach is used to terminate the process.

In Table [I] the combined output result using the proposed method is same as [19] but improvement is achieved in terms of no. of the inverter for output function F1. In Table [II] the proposed technique provides a much better result for the combined output as well as for the individual output functions. Our technique yields superior results for the functions presented in [III] and [V] as well. For the function presented in [IV] the proposed method produces similar results for the combined output as in [18] and considering the individual output function it is difficult to decide which one is better.
TABLE I: Simulation result and comparison of a 3 input/2 output function

| Approach       | Minterms                          | Circuit                                                                 | NMV | NINV | Levels | CMV | CINV | TMV | TINV | TG | Max level |
|----------------|-----------------------------------|-------------------------------------------------------------------------|-----|------|--------|-----|------|-----|------|----|-----------|
| [19]           | $F_1 = \sum m_1, m_2, m_4, m_5, m_1_3$ | $F_1 = \{M(1',A',C), M(D',M(A,B,1'),M(A',B,A))$ | 4   | 3    | 2      | 1   | 4    | 2   | 16   | 10 | 2         |
|                | $F_2 = \sum m_3, m_4, m_5, m_1_3$   | $F_2 = \{M(0,M(0,A,B'),M(1,B,C'))$ | 3   | 2    | 2      |     |      |     |      |    |           |
| Proposed       | $F_1 = \sum m_1, m_2, m_4, m_5$    | $F_1 = \{M(A,C,B'),M(A,C',1),M(B,0,C))$ | 4   | 2    | 2      | 1   | 0    | 6   | 4    | 10 | 2         |
| Approach        | $F_2 = \sum m_3, m_4, m_5, m_1_3$   | $F_2 = \{M(O,B,C'),M(B,O,A),C'$ | 3   | 2    | 2      |     |      |     |      |    |           |

TABLE II: Simulation result and comparison of a 4 input/2 output function

| Approach       | Minterms                          | Circuit                                                                 | NMV | NINV | Levels | CMV | CINV | TMV | TINV | TG | Max level |
|----------------|-----------------------------------|-------------------------------------------------------------------------|-----|------|--------|-----|------|-----|------|----|-----------|
| [15]           | $F_1 = \sum m_0, m_2, m_4, m_1_2$ | $F_1 = \{M(A,B',1'),(M(D',M(B,A,1'),M(A',B,A))$ | 6   | 5    | 3      | 3   | 8    | 5   | 13   | 3  |           |
|                | $m_1_3, m_1_4$                    | $F_1 = \{M(B,M(A,C',1'),(M(A',B,A),D,M(B,A,C'))$ | 5   | 3    | 3      |     |      |     |      |    |           |
| Proposed       | $F_1 = \sum m_0, m_2, m_4, m_1_2$ | $F_1 = \{M(B,1',A'),M(B,C,1'),M(D')$ | 6   | 4    | 3      | 2   | 2    | 7   | 4    | 11 | 3         |
| Approach        | $m_1_3, m_1_4$                    | $F_1 = \{M(A,0,M(0,B,C')$ | 3   | 2    | 2      |     |      |     |      |    |           |

TABLE III: Simulation result and comparison of a 3 input/3 output function

| Approach       | Minterms                          | Circuit                                                                 | NMV | NINV | Levels | CMV | CINV | TMV | TINV | TG | Max level |
|----------------|-----------------------------------|-------------------------------------------------------------------------|-----|------|--------|-----|------|-----|------|----|-----------|
| [15]           | $F_1 = \sum m_2, m_4, m_6, m_7$   | $F_1 = \{M(1,C',B'),1,A),M(A,B,1'),B'$ | 4   | 3    | 3      | 4   | 4    | 8   | 6    | 14 | 3         |
|                | $m_1_3, m_1_4$                    | $F_1 = \{M(0,C,M(1,B,A))$, $F_2 = \{M(C,B,A),M(1',B,A)\),M(C,0,A')$ | 4   | 3    | 2      | 4   | 4    | 3   | 3    | 2  |           |
| Proposed       | $F_1 = \sum m_2, m_4, m_6, m_7$   | $F_1 = \{M(0,0,C',M(1,B,C'))$ | 2   | 1    | 2      | 3   | 1    | 7   | 6    | 13 | 2         |
| approach       | $F_2 = \sum m_0, m_1, m_3, m_6$   | $F_2 = \{M(C,B,A),M(1',B,A)\),M(C,0,A')$ | 3   | 2    | 2      |     |      |     |      |    |           |
|                | $m_7, m_1_2, m_1_3, m_1_5$        | $F_3 = \{M(C,B,A),M(1',B,A)\),M(C,0,A')$ | 4   | 3    | 2      |     |      |     |      |    |           |

TABLE IV: Simulation result and comparison of a 3 input/4 output function

| Approach       | Minterms                          | Circuit                                                                 | NMV | NINV | Levels | CMV | CINV | TMV | TINV | TG | Max level |
|----------------|-----------------------------------|-------------------------------------------------------------------------|-----|------|--------|-----|------|-----|------|----|-----------|
| [15]           | $F_1 = \sum m_1, m_4, m_5, m_7$   | $F_1 = \{M(A,B',C)$ | 1   | 1    | 1      | 3   | 4    | 9   | 6    | 15 | 3         |
|                | $m_1_3, m_1_4$                    | $F_2 = \{M(M(C,B,A),1,A),M(A',1',C)$ | 4   | 3    | 3      |     |      |     |      |    |           |
|                | $m_3, m_4, m_6, m_7$              | $F_3 = \{M(M(1,C,B'),1,A),M(A',1',C)$ | 4   | 3    | 2      |     |      |     |      |    |           |
|                | $m_0, m_2, m_5, m_6$              | $F_4 = \{M(A,B',C'),B,M(1',A',C)$ | 3   | 3    | 2      |     |      |     |      |    |           |
| Proposed       | $F_1 = \sum m_1, m_4, m_5, m_7$   | $F_1 = \{M(C,B',A)$ | 1   | 1    | 1      | 4   | 2    | 9   | 6    | 15 | 3         |
| approach       | $F_2 = \sum m_3, m_4, m_6, m_7$   | $F_2 = \{M(0,0,C',A),M(A,C,0'),M(B,C,0)$ | 4   | 2    | 2      |     |      |     |      |    |           |
|                | $m_0, m_2, m_5, m_6$              | $F_3 = \{M(M(C,0,A'),A,B)$ | 5   | 4    | 3      |     |      |     |      |    |           |
|                | $m_4, m_6, m_7$                   | $F_4 = \{M(A,M(0,C',A),M(B,C,0)$ | 3   | 1    | 2      |     |      |     |      |    |           |

However, on average the proposed technique exhibits better results than the best available techniques, which is satisfactory. Simulation is performed up to 4 outputs 4 variable functions, without loss of generality the technique is applicable to any multi-output functions with arbitrary no. of input variables.

VI. CONCLUSION

In this paper, an improved technique is proposed for the automatic synthesis of optimal QCA circuits. Genetic algorithm is utilized for achieving the goal. As multi-output circuits are more common in practice, so the main focus is given to optimizing multi-output QCA circuit in particular. Optimization is performed in terms of area consumption as well as the worst-case delay of a QCA circuit. Area consumption is
TABLE V: Simulation result and comparison of a 4 input/4 output function

| Approach       | Minterms                                      | Circuit                                                                 | NMV | NINV | Levels | CMV | CINV | TMV | TINV | TG | Max level |
|----------------|-----------------------------------------------|--------------------------------------------------------------------------|-----|------|--------|-----|------|-----|------|----|-----------|
| [18]           | $F_1 = \sum m_3, m_4, m_7, m_{15}$,          | $F_1 = M(M(C,1^*,D),M(D, M(C,B,A)',B,D))$                               | 4   | 3    | 3      | 8   | 6    | 9   | 8    | 17 | 4         |
| $F_2 = \sum m_1, m_3, m_4, m_{9}$, $m_{13}, m_{15}$ | $F_2 = M(M(1^*,M(D',A,1),B),M(D, M(C,B,A)',B))$                         | 5   | 4    | 3      |     |      |     |      |    |           |
| $F_3 = \sum m_3, m_6, m_{7,11}$, $m_{13}, m_{14,15}$ | $F_3 = M(C,D,M(1^*,M(D',A,1),B))$                                       | 3   | 2    | 3      |     |      |     |      |    |           |
| $F_4 = \sum m_2, m_6, m_{10}, m_{11,14}$           | $F_4 = M(M(C,1^*,D),M(D, M(C,B,A)',B,D))$                               | 5   | 5    | 4      |     |      |     |      |    |           |
| [19]           | $F_1 = \sum m_3, m_4, m_7, m_{15}$,          | $F_1 = M(M(A'B,D),M(1,C,D'),M(0,C,D))$                                  | 4   | 2    | 2      | 3   | 2    | 12  | 5    | 17 | 3         |
| $F_2 = \sum m_1, m_3, m_4, m_{9}$, $m_{13}, m_{15}$ | $F_2 = M(M(A'B,D),M(B,C,D'),M(0,D, M(A,B',D)))$                         | 5   | 3    | 3      |     |      |     |      |    |           |
| $F_3 = \sum m_3, m_6, m_{7,11}$, $m_{13}, m_{14,15}$ | $F_3 = M(0,M(1,A,C),M(B,C,D))$                                         | 3   | 0    | 2      |     |      |     |      |    |           |
| $F_4 = \sum m_2, m_6, m_{10}, m_{11,14}$           | $F_4 = M(0,M(1,A,C),M(B,C,D))$                                         | 3   | 2    | 2      |     |      |     |      |    |           |

Proposed approach $F_1 = \sum m_3, m_4, m_7, m_{15}$, $F_2 = \sum m_1, m_3, m_4, m_{9}$, $m_{13}, m_{15}$, $F_3 = \sum m_3, m_6, m_{7,11}$, $m_{13}, m_{14,15}$, $F_4 = \sum m_2, m_6, m_{10}, m_{11,14}$ $F_1 = M(M(B,A,M(B,D,C),M(0,D,C)),B)$ $F_2 = M(M(D,B,C),B,A)',B,M(M(D,0,A),B',D'))$ $F_3 = M(M(B,C,D),M(D,A,0),C)$ $F_4 = M(D',M(M(D,A,0),B',0),C)$ $4$ $1$ $3$ $5$ $1$ $10$ $4$ $14$ $3$ $1$

- Optimized by minimizing no. of gates and worst case delay is optimized by minimizing the maximum level in the circuit. Importance is assigned to level and gates according to their cost in the circuit. As optimizing individual circuit may not lead to the globally optimal solution, so fitness is calculated in such way that benefitted the local as well as the global optimal solution. Elitism is adopted in GA for preserving the best solutions. Improved techniques are applied in different steps of GA to get the best result. Redundancy elimination is performed for avoiding the chance of any redundancy in the final solution. Some useful strategies are introduced to reduce no. of computations. The experiment is performed using some standard functions. Simulation results signify, the proposed technique achieved better performance in terms of optimization in comparison to present best techniques. It is worth to say that the proposed technique can provide a good optimal result for any multi-output function with arbitrary no. of inputs.

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