Performance optimization and analysis of the unstructured discontinuous Galerkin solver on multi-core and many-core architectures

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Abstract—The discontinuous Galerkin (DG) algorithm is a representative high order method in Computational Fluid Dynamics (CFD) area which possesses considerable mathematical advantages such as high resolution, low dissipation, and dispersion. However, DG is rather computationally intensive to demonstrate practical engineering problems. This paper discusses the implementation of our in-house practical DG application in three different programming models, as well as some optimization techniques, including grid renumbering and mixed precision to maximize the performance improvements in a single node system. The experiment on CPU and GPU shows that our CUDA, OpenACC, and OpenMP-based code obtains a maximum speedup of 42.9x, 35.3x, and 8.1x compared with serial execution by the original application, respectively. Besides, we systematically compare the programming models in two aspects: performance and productivity. Our empirical conclusions facilitate the programmers to select the right platform with a suitable programming model according to their target applications.

Index Terms—Unstructured grid, DG, GPU, performance, productivity

I. Introduction

The high-order scheme receives considerable attention in Computational Fluid Dynamics (CFD) due to its low numerical dissipation for Large-Eddy Simulation (LES) [1] and the capability to capture the fine-grained structure in complicated flows. Discontinuous Galerkin (DG) [2] is a popular algorithm that possesses good mathematical properties in conservation, stability, and convergence in complex flow problems. However, DG suffers from severe computing overhead comparing with the low-order scheme. For example, solving the Euler equation with three-dimensional fourth-order DG method needs one hundred variables per grid element [3], [4], while the only single-digit variable is required in low-order methods, not to mention the additional volume and area integral computations in every grid element, which is not needed at all in low-order method.

To make computationally expensive DG algorithm available in practical engineering, many researchers have made considerable achievements on both GPU and CPU hardwares. Xia accomplishes the unstructured grid DG algorithm based on OpenACC Programming model [5]. Pazner employed a parallel-in-time strategy to compute the Runge-Kutta stages simultaneously under DG discretizations [6]. Duan applied total variation diminishing Runge-Kutta scheme coupled with the multigrid strategy to improve the parallel efficiency of DG method on CPUs [7]. Maurice presented a parallel computing strategy for a hybridizable discontinuous Galerkin nested geometric multigrid solver on many-core hardware, attaining 80% of peak performance for higher order polynomials [8]. Kronbichler integrated optimized DG code into a scalable framework of five supercomputers using both CPU and GPU hardwares [9].

The former studies usually focus on the algorithm
optimization and performance achievement with either CPU or GPU. However, few articles consider the performance portability across multi-core CPU and many-core accelerators, as they are generally used in high-performance computing (HPC) system. The latest TOP500 list shows that six out of the top ten supercomputers utilize many-core accelerators, this trend brings not only a good opportunity to accelerate DG algorithm on GPU, but also barriers in programming to migrate code on diverse computing architectures.

Therefore, this work aims to assess three programming models, namely OpenMP, OpenACC, and CUDA on both multi-core CPU and many-core accelerator, in the context of an unstructured grid high-order DG application called HOUR2D. The aspects to be compared are the implementational effort and performance evaluation, as well as the optimizations during code migration. Finally, we evaluate the performance and portability to give insights on appropriate language selection for different purposes. The work provides novelty from several perspectives:

- We give a high-performance migration of HOUR2D application in OpenMP, OpenACC, and CUDA, respectively, the parallelization in different programming models is elaborately chosen to adapt unique data structures and computing formats.
- We perform the grid renumbering method to optimize irregular memory access issue caused by the unstructured grid, then carry out the mixed floating-point method to improve computational performance, at last, the Unified Memory (UM) method are tested in OpenACC for workload reduction.
- We evaluate the performance and productivity, firstly the speedup of three programming models is listed using six different grid meshes, then some insights are indicated by using the roofline model, at last, a comprehensive assessment is displayed together with productivity metric.

This work is organized as follows: Section 2 gives a brief review of the mathematical method and typical data pattern used in HOUR2D. Section 3 displays the implementation to achieve high performance for three programming languages and the evaluation approaches. Section 4 presents the experiment of performance and productivity in HOUR2D code. Section 5 summarizes our whole research and gives insights.

II. Performance Implementation

HOUR2D can solve steady or unsteady field Navier-Stoke and Euler problems by using the explicit Runge-Kutta high-order DG algorithm, and it’s mainly composed of three parts: preprocessing, flow field calculation, and output postprocessing.

Time iterations is the hotspot which occupies more than 95% of total running time, including time step, right-hand-side (RHS), and file output, the RHS procedure involves inviscid flux, gradient, viscous flux, and residual calculation. The RHS step is counted twice in every time step because of the two-order explicit Runge-Kutta method, and it consumes approximately 90% of total running time, so it is the computationally intensive part of the whole application indeed, therefore the primary concern for performance optimization is RHS.

A. Data Structure and Computing Formats

The geometric topology of HOUR2D’s unstructured mesh consists of vertices, elements, and cells as shown in fig. 1, $E_i$ is the face unit in which stores the flux variable, $C_i$ is the cell unit in which stores the intermediate variables that include density, velocity, and pressure, besides the above data is organized as the array of structure(AOS) format.

![Fig. 1. Data structure and major computational modes. $C$ is the body center of the cell, and $E$ is the face unit where the data is stored in AOS format. The dotted box shows two major modes in our computations, the red dotted arrow means the data access flows in memory.](image)

We display two major computational modes that affect memory access pattern and parallelization format as the dotted box shows. The first one indicates the flux computation which is parallelized through elements, for every time step, the program reads the intermediate variables from neighbor cell units, then writes back to the current element unit after calculations. The other one is the physical quantity calculations that are stored in cells, which requires flux variable around adjacent cells at the present step, data race occurs if the element parallelization model is still utilized.

B. Grid Renumbering

The second computing formats mentioned in the former subsection involves the data access around the neighbor cells in every central cell. However, the number of these adjacent cells are not naturally continuous as the topology of unstructured grid is irregular. Hence, resulting in indirect memory access patterns when iterating over the cells of the unstructured grid for the flux, gradient, and residual computations.

To relieve the irregular memory access issue, we reorder the grid to reduce the cache miss and improve the data locality with Reverse Cuthill Meeke (RCMK) algorithm [10]. The RCMK is developed to minimize the bandwidth
in the adjacent graph by assembling the non-zero values as close as possible to the main diagonal [11]. So we reorder the topological adjacency derived from the computational grid to align the cell numbers. The optimization result is shown in Table I, it displays the bandwidth of four unstructured grids with different number of cells. The last two columns are the bandwidth of cell-based adjacency matrix which shows the degree of aggregation around the diagonal, the bandwidth is greatly reduced according to the results of all four grids, it can be inferred that bandwidth reduction attains 2-3 orders of magnitude. A more detailed plot about the cell aggregation in shown in fig. 2, it exhibits the fairly good result by comparing the adjacency before and after applying RCMK.

**TABLE I**
The bandwidth of different computational grids when using RCMK algorithm. The element is the number of grid cells, bandwidth shows the max aggregation of adjacent elements. The bandwidth is greatly reduced after applying RCMK.

| Grids | Number of cell | Original bandwidth | RCMK bandwidth |
|-------|----------------|-------------------|----------------|
| Grid1 | 2688           | 1427              | 69             |
| Grid2 | 4032           | 3992              | 35             |
| Grid3 | 16128          | 12410             | 67             |
| Grid4 | 64512          | 49016             | 131            |

Fig. 2. The intuitive illustration for bandwidth reductions of four computational grids. The upper figures show the original adjacency, while the lower figures are adjacency after applying RCMK.

Following the renumbering, the cell is arranged in the order of monotonical index, and a consecutive rank is performed on the element index according to the first constant cell index, so the second index reference will be visited in ascending order. The staple benefits of the optimizations above can be summarized as enhancing both spatial and temporal locality particularly when cells are referenced contiguously in memory and exploiting the available memory bandwidth. What’s more, the renumbering technique is executed only once before the time iteration starts for every process, hence it has a negligible effect on the whole application execution not to mention the time iteration is usually a fairly big number. The overall performance improvement by using the grid renumbering method is about 20%-30%.

C. Mixed Precision

The physical variables use the double-precision (DP) format to maintain good convergence and computational precision through CFD simulations compared with single-precision (SP), however, it increases the amount of memory data required for every floating-point operation, and the memory wall issue is further aggravated and restricts the CFD performance efficiency, under the conditions that off-chip memory bandwidth is considered to be the constraining resource in system performance for the foreseeable future [12]. The mathematical evidence proves that there’s no need to use DP format in all the physical parameters or the whole calculation procedures, even if taking into account the constraint of given computational precision [13], [14], so CFD application turn to use lower floating-point precision variables to achieve higher performance, naturally some mixed-precision (MP) strategies emerged [15], [16].

One of the methods is called the iterative refinement approach, at first, it employs SP parameters in previous iterations to improve the computational performance, then uses DP format immediately when the convergence rebound occurs, so convergence, precision, and high performance are guaranteed at the same time. We verify this approach in HOUR2D by using a NACA airfoil mesh grid as the fig. 3 shows, fig. 3 illustrates the $L_2$ residual convergence, in which MP-30k stands for the initial 30 thousand steps are computed in SP format, while the rest of the steps are computed in DP, it’s obvious that the precision of the output result decline as the SP step increases.

Fig. 3. Mixed precision approach verification using NACA grid. The comparison of the residual convergence in MP methodology with different time steps allocated in SP and DP, for example, MP-30k means the initial 30000 iterations are executed in SP format, the rest of the iterations are computed in DP.

We assess the performance improvement of our MP method after the correctness verification with two grid examples as table I shows. The experiment result is shown in table II, in which the total time steps are 100 thousand, too. DP shows the benchmark of our test, the run time decreases as the SP step increases. The last row SP indicates the most optimal improvement with no DP format variables are used at all, we can conclude from the table that the MP method achieves 15% per-
formance improvement at most compared with the DP format. However, the SP format is only comparable in performance, as the computational precision is not strictly guaranteed to meet the constraint in diverse grids from mathematical point of view, the SP format are usually not used in engineering computations, so the most optimal speedup is usually only a theoretical conclusion.

**TABLE II**
Clock time of our mixed precision approach running on two grids. The DP means the double precision calculation, and SP is single precision format. the MP-20k means the starting 20000 iterations are executed in SP format, followed by the rest of the iterations computed in DP.

|       | Grid1 | Grid2 |
|-------|-------|-------|
| DP    | 51.87 | 151.91|
| MP-20k| 49.68 | 145.83|
| MP-50k| 48.30 | 140.90|
| MP-80k| 46.68 | 135.95|
| SP    | 43.87 | 131.40|

D. Heterogeneous Implementations

We port HOUR2D code using both Compute Unified Device Architecture (CUDA) and OpenACC on Nvidia GPU to get an apparent comparison in performance and productivity. CUDA usually gains a better performance than OpenACC due to the fine-grained manipulation of hardware resources within kernels, however, this generally requires the time-consuming task of code revising to make use of the resources for developers. On the contrary, OpenACC is a declarative model using compiler pragmas which is not as effective as CUDA in computing performance.

The minimization of data transmission between CPU and GPU hardware is at prior consideration in HOUR2D as it’s an expensive operation over the time iterations, so the covered data is transported to GPU memory in the grid initialization stage to avoid the potential bottleneck caused by the frequent data transfer. We accommodate the grid data with the appropriate component from the GPU memory hierarchy like shared memory, constant memory, and global memory to achieve better memory access performance. For example, HOUR2D high-order algorithm needs 393 geometrical constants to accomplish element-integral and cell-integral in each time iteration step, so we place it in the constant memory to reduce memory transactions launched by thread warp.

As for the code migration, we port the whole iteration code into GPU as the blue dotted box shows in ??, on the one hand, the parallelization in RHS step can be implemented naturally in the way of fig. 1 shows without any data racing, the element-based or cell-based loop can be mapped to the one-dimensional thread in GPU directly.

On the other hand, the time step computation involves the minimal value of all local time steps in cell data, making data racing if it’s executed in direct parallelization. To achieve effective performance in entire computing procedures, we use GPU reduction to get minimal value by taking advantage of shared memory which enables synchronization within thread blocks. Furthermore, we design the consecutive reduction method to realize robust reduction under the restriction of max thread number in GPU block.

Porting the code by using OpenACC is much more convenient than CUDA by using compiler pragmas to parallelize compute-intensive code, for example, the time step reduction mentioned above only needs to use `#pragma acc parallel reduction` instead, and the specified process will be done by PGI compiler, but the performance also highly depends on the data layout in PGI compiler and the effectiveness of code generation.

UM is a pragmatic technology that can be used by CUDA 6.X or higher version, it manages the data between CPU and GPU independently which was relied on programmers, hence explicit function calls and data migration can be decreased evidently. We adopt the UM method during heterogeneous code migration by simply adding the `managed` compilation option so that memory space between host and device is established.

UM leads to possible performance loss due to the additional memory transmission and memory page fault [17], which is also observed in our OpenACC code, generally, the performance loss decreases as the grid size increases, eventually stabilizing below 3% especially when the grid’s element exceeds sixteen thousand, this may be caused the intensification of discontinuous memory access as grid size increases.

III. Experiments and Analysis

The HOUR2D code is fulfilled at the same level of optimization in three different programming models: OpenMP, OpenACC, and CUDA, while the computing hardware includes a computing node consisting of an Intel Xeon E5-2698 @2.20GHz CPU and an Nvidia A100 GPU, as for compiler toolchain, we use GCC – 5.4.0 for CPU code with optimization flag -O3, and the GPU compiler NVCC – 10.2.89 for CUDA and OpenACC. The computational grid is illustrated in table III which includes two steady NACA airfoil grids(grid1 and grid2), four unsteady front step grids (grid3-grid6), and an unsteady flow around double cylindrical(grid7). The latter grid is four times larger than the former one for those possess same aerodynamic shape, the last column is the grid type of every element.

A. Evaluation Approach

As the main hotspot of HOUR2D is time iteration that performs almost the same operation, and tens of thousands of time steps are usually required to reach a convergent result in practical CFD simulation, the pre-processing and postprocessing parts should be removed
for the seek precise evaluation. We apply Dual-phase measurement [18] method to exclude the non-primary impacts during the performance experiments. Specifically, the application is tested twice with different iterations, the subtraction data between two iterations shows the difference of exact iteration computations. Hence, the performance metric like Flops, DRAM bytes and run time of the can be computed precisely in this way.

We implement the roofline model to give some performance insights into memory bandwidth and floating-point operations. Roofline [19], [20] is a bound and bottleneck analysis function, it chooses the minimum value of either current peak machine performance, or peak DRAM bandwidth multiply arithmetic intensity, so that it provides insights into the primary factors affecting the performance of computer systems [21].

To measure the workload during the porting process, we apply productivity metric to quantify how efficiently HOUR2D code is developed with different programming models [22], specifically the “code divergence” is the average of the pairwise distances between the applications in different code versions A,

$$D(A) = \left( \frac{|A|}{2} \right)^{-1} \sum_{a_i, a_j \in A} d(a_i, a_j), \{a_i, a_j \} \subset A$$  \hspace{1cm} (1)$$

in which $d_{a,b}$ originates from the same code in the number of Source Line Of Code(SLOC) [23] normalized to the smaller application, the detailed equation is shown in eq. (2).

$$d(a, b) = \frac{|SLOC(a) - SLOC(b)|}{\min(SLOC(a), SLOC(b))}$$  \hspace{1cm} (2)$$

B. Performance Results

We use the complete grids to verify the correctness of output flow field, two intuitive shapes are selected to display the stable flow field as fig. 4 shows. The subfigure fig. 4a displays the final density of NACA airfoil illustration, the various color refers to differentiated values. While fig. 4b is the pressure of flow around double cylindrical, the flow clusters clusters in front of the first circular and forms relatively high pressure, the reversed side of the circular forms low pressure.

We choose OpenMP-based code as a benchmark to assess the performance of other two languages. Thread scalability is first evaluated with first six computational grids for the convenience of comparison, the run time is displayed in fig. 5a, and the number of thread varies from one to twenty. It can be inferred from the figure that the code obtains considerable scalability as the growth rate of the running time is roughly the same as that of the grid size. Besides, twenty-thread parallelization achieves a speedup of 6.0x - 8.1x comparing with serial execution according to different grids, the different speedup of grid may be affected by several reasons like insufficient parallelism for small-scale grid, memroy access exacerbation as grid size increases and so on.

The comparisons for three languages is applied after evaluating OpenMP code base, we analyze the speedup based on the serial execution for first six grids as fig. 5b shows. The colored columnurs are presented under the same optimization conditions, grid renumbering and mixed precision strategy are not included. The GPU-based code shows relatively lower speedup than OpenMP in small-scale grids, it’s due to the fact that the grid data is insufficient in parallelism gain to cover the data movement
cost. As the grid size increases, GPU-based code shows priority to OpenMP’s, particularly, CUDA is much better than OpenACC owe to the fine-tuning of thread scheduling, better memory hierarchy control, and some memory access optimizations. Generally, OpenACC’s speedup reaches 75% to 90% of CUDA’s, besides, UM approach is enabled in OpenACC-based code. The CUDA, OpenMP, OpenACC based code obtains a maximal speedup of 42.9x, 35.3x, and 8.1x among six grids comparing with serial execution, respectively.

To further explore the computing performance, we build the roofline model of all three programming models to find the possible bottleneck with floating-point operations and memory access, the execution details in the CPU are collected by Intel Vtune Profiler, while the Nvidia Nsight Profiler is utilized in GPU. The final chart is shown in fig. 6, the abscissa is the arithmetic intensity which represents the amount of data required (transported from DRAM to cache) for each floating-point operation, and the ordinate is the double-precision floating-point operations achieved per second, besides, the red and blue attributes belong to V100 GPU and Intel Xeon E5 CPU respectively, the solid line is the theoretical limit of the hardware unit, and the scatter points are the measured values through our experiments, moreover, the red dot shows the execution of CUDA-based code while the red star belongs to OpenACC, the different scatter points of the same color display the analysis of different grids.

We can infer from fig. 6 that the HOUR2D executions of all three models are faced with memory access bottleneck even if some memory optimization methods are applied, especially for CUDA-based code when grid size extends, this may be the increasing deterioration of frequent access to multi-dimensional array for element and cell integral, and the most important, non-consecutive memory access caused by the unstructured grid which is generally acknowledged as a tough issue for HPC researchers in CFD field. What’s more, the achieved Flops can be ranked as CUDA > OpenACC > OpenMP due to the abundant thread concurrency in GPU, particularly for the larger grids.

C. Productivity Evaluation

Although the CUDA-based code shows the absolute performance advantage over OpenMP and OpenACC, meanwhile CUDA certainly consumes the most effort on code tuning. So we use quantitative metric detailed in eq. (2) to further evaluate our workload as table IV shows, in which the second column is the porting workload from desktop version to current code, and the desktop is taken as the benchmark version with 2900 total source lines. The metric $d_{(current, desktop)}$ displays the relative workload porting from the desktop version to the current version as the eq. (2) shows, the fourth and fifth row stands for the situation of whether to use UM method or not, the bigger metric $d$ represents more porting workload and lower productivity. So under the basis of OpenMP-based code, the workload of the CUDA is 8.2 times larger and the OpenACC using UM is 2.7 times larger, however, this quantified number has an underlying assumption that the development difficulty of different programming models keeps consistent.

The relative effort time productivity (RDTTP) concept connects the performance and productivity which is $\Psi_{relative}$=speedup/relative effort, it’s useful under the condition of the same optimization level for three programming models, so the sort through $\Psi$ according to the metric above is: $\Psi_{OpenMP} > \Psi_{CUDA} > \Psi_{OpenACC}$. The OpenMP performs best because of the fairly high productivity, and CUDA is better than OpenACC. It’s
worth noting that RDTDP takes performance and productivity equally important which is not always true in reality, striking the appropriate balance between the performance and productivity relies on the ultimate use of the code [24].

IV. Conclusions and Future Work

We have presented the migration of a practical high-order DG application named HOUR2D into three programming models running on two architectures, performance analysis, and portability are further evaluated.

We first discuss some optimization methods in the light of data structure and computing format, the grid renumbering approach is used to relieve the discontinuous memory access, then the mixed-precision method to maximize the floating-point operations. We also capture the performance on CPU and GPU platforms with seven grids, concretely the CUDA, OpenMP, and OpenACC based code achieves roughly a speedup of 42.9x, 8.1x, and 35.3x based on the serial execution, then we find the memory access issue by using the roofline model which needs further research, the productivity of different programming models are measured with quantified metric.

We plan to carry out our future work in two aspects. On the one hand, we improve the memory bandwidth and the floating-point efficiency of the high-order algorithm. On the other hand, we evaluate the performance portability of our algorithm in more programming models to offer a practical assessment to the CFD developers.

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