Design and operation of distributed double-SQUID amplifier for RSFQ circuits

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Abstract. Recently, many groups have been developing on-chip Rapid Single-Flux-Quantum (RSFQ) output amplifiers which are designed to connect RSFQ circuitry to room temperature electronics. One of such amplifiers is a distributed SQUID amplifier comprising SQUIDs embedded in cascaded RSFQ RS flip-flops. In this paper, we propose a distributed double-SQUID amplifier, where a SQUID is replaced with a double-SQUID. Test circuit was fabricated using a niobium integration technology. Measurements were performed in a liquid helium bath. We confirmed that the maximum output voltage swing of a 4-stage distributed double-SQUID amplifier was 2.93 mV, which was comparable with the corresponding numerical value of 3.54 mV.

1. Introduction
Rapid Single-Flux-Quantum (RSFQ) circuitry [1] is an attractive digital technology and expected to bear the next-generation high-speed digital systems. This is because it has great advantage to low power consumption and high-speed operation. However, we have to implement superconductor–semiconductor interfaces between RSFQ circuitry and room temperature electronics, because the energy of a single flux quantum (SFQ) is relatively small. For the above reason, many groups have been developing on-chip RSFQ amplifiers which are designed to connect RSFQ circuitry to room temperature electronics.

RSFQ amplifiers can be classified according to their bias types, AC bias and DC bias. Table 1 is a list of RSFQ output amplifiers such as a Suzuki stack [2], a 4JL gate [3], a HUFFLE driver [4], a SQUID array [5] and a distributed single-SQUID amplifier (DSSA) with their bias types. Demonstrated performances reported in literature such as the maximum voltages swing \(V_{\text{max}}\) and maximum operation frequencies \(f_{\text{max}}\) are also listed with their Nb technologies.

In general, a distributed amplifier is a cascaded amplifiers coupled with signal transmission lines to obtain both wide bandwidths and high gains. For superconducting RSFQ circuitry, a 12-stage distributed amplifier was demonstrated, of which the output voltage swing was 1.75 mV for 10 Gbps data link [6]. In this paper, we refer to this distributed amplifier as a distributed single-SQUID amplifier (DSSA) for the comparison with our amplifier described below.

To improve the output voltage swing of distributed amplifiers, there are two choices available. One choice is to increase the number of stages, because the output voltage swing is expected to be proportional to the number of stages. This choice, however, requires more area occupancies and power consumption. The other choice is to increase the output voltage swing per stage if possible.
Table 1. Comparison of RSFQ output amplifiers.

| Bias type   | Suzuki Stack [2] | 4JL [3] | HUFFLE [4] | SQUID Array [5] | DSSA [6] |
|-------------|------------------|---------|------------|-----------------|---------|
| $V_{max}$ [mV] | AC               | AC      | DC         | DC              | DC      |
| $f_{max}$ [GHz] | 60               | 2.3     | 1.5        | 3.0             | 1.75    |
| Nb tech. [kA/cm$^2$] | 4.5             | 2.5     | 1.0        | 1.5             | 4.5     |

In this paper, for the latter method, we propose a distributed double-SQUID amplifier (DDSA), where a SQUID in a DSSA is replaced with a double-SQUID. A double-SQUID is expected to generate output voltage swings twice as large as those of a single SQUID. Below, we present our circuit design, numerical results, and experimental results.

2. Development of a fundamental circuit stage in a distributed amplifier

Figure 1(a) shows the equivalent circuit of a fundamental circuit stage in a DSSA.

![Figure 1](image_url)

**Figure 1.** Equivalent circuit of a single stage in a distributed single-SQUID amplifier (DSSA) (a) and a distributed double-SQUID amplifier (DDSA) (b). “X” and hourglass symbols represent a unshunted (under-damped) junction and a critically-damped junction, respectively.

One single stage consists of two parts. One part is an SFQ storage loop with two (SET and RESET) terminals, and the other part is a SQUID coupled to the storage loop. Input SFQ pulses are transferred alternatively to either SET or RESET terminal. Alternative transmission is realized through a TFF that is presented later. When an SFQ comes from the SET terminal, it is stored in the storage loop. Then, the critical current of the SQUID is reduced and its output voltage increases. We call this state the SET state and it is a finite voltage state. Next, when an SFQ comes from the RESET terminal, it annihilates the stored SFQ. The critical current of the SQUID then returns to the original value and the output voltage decreases. We call this state the RESET state and it is the zero-voltage state. The output signal is a voltage swing between the SET and RESET state and these operations realize non-return-to-zero (NRZ) signals. In the first DSSA paper [6], the circuit layouts were designed to realize the characteristic impedance of 50 Ω, whereas termination resistors of 50 Ω was also integrated on-chip.

We propose a DDSA where SQUIDs in a DSSA are replaced with double-SQUIDs as shown in Fig. 1(b), where two stacked SQUIDs sharing one sensing inductor are magnetically coupled to
the storage loop. That is, two-fold output voltage is expected by introducing the double-SQUID structure [11].

3. Numerical comparison between DSSA and DDSSA

3.1. Device parameters of a single stage in a DSSA and a DDSA

Figures 2 and 3 show the device parameters of a single stage in a DSSA and a DDSA.

**Figure 2.** Equivalent circuit and parameters of a stage in a DSSA. Parameters are determined as follows using an optimization tool. The values of external shunt resistors are presented next to the critical currents of Josephson junctions. \( L_1 = L_4 = L_5 = L_17 = L_20 = 0.50 \text{ pH}, L_2 = L_19 = 3.50 \text{ pH}, L_3 = 2.00 \text{ pH}, L_5 = 2.58 \text{ pH}, L_6 = 0.46 \text{ pH}, L_7 = L_8 = 5.70 \text{ pH}, L_9 = L_{10} = 4.70 \text{ pH}, L_{11} = L_{12} = 0.32 \text{ pH}, L_{13} = 2.40 \text{ pH}, L_{14} = 1.60 \text{ pH}, L_{16} = 4.00 \text{ pH}, L_{18} = 3.00 \text{ pH}, J_1 = J_8 = 0.22 \text{ mA (1.71 } \Omega), J_2 = J_6 = 0.13 \text{ mA (2.83 } \Omega), J_3 = J_7 = 0.20 \text{ mA (1.84 } \Omega), J_4 = 0.14 \text{ mA, J_5 = 0.14 mA (2.66 } \Omega), R_1 = 12.92 \text{ } \Omega, R_2 = 15.66 \text{ } \Omega, M_1 = M_2 = 3.62 \text{pH (k = 0.70).}

**Figure 3.** Equivalent circuit and parameters of a stage in a DDSA. Parameters are determined as follows using an optimization tool. The values of external shunt resistors are presented next to the critical currents of Josephson junctions. \( L_1 = L_4 = L_5 = L_17 = L_19 = L_{22} = 0.50 \text{ pH}, L_2 = L_{21} = 3.50 \text{ pH}, L_3 = L_{18} = L_{20} = 2.00 \text{ pH}, L_5 = 2.38 \text{ pH}, L_6 = 0.46 \text{ pH}, L_7 = L_8 = 4.09 \text{ pH}, L_9 = L_{10} = 4.12 \text{ pH}, L_{11} = L_{12} = 1.80 \text{ pH}, L_{13} = L_{14} = 1.20 \text{ pH}, L_{15} = 1.60 \text{ pH}, L_{16} = 2.40 \text{ pH}, J_1 = J_{10} = 0.22 \text{ mA (1.71 } \Omega), J_2 = J_9 = 0.20 \text{ mA (1.84 } \Omega), J_3 = J_8 = 0.13 \text{ mA (2.83 } \Omega), J_4 = J_7 = 0.10 \text{ mA, J_5 = J_6 = 0.10 mA (3.73 } \Omega), R_1 = 17.27 \text{ } \Omega, R_2 = 20.37 \text{ } \Omega, M_1 = M_2 = 3.20 \text{ pH (k = 0.73).}
We determined the parameters that realized the correct DSSA and DDSA operation by using a Josephson simulator (JSIM) [12] and an optimization tool SCOPE2 [13]. $J_3$ and $J_7$ in Fig. 3 as well as $J_2$ and $J_9$ in Fig. 3 play a role of escape junctions, which were not implemented in the original work of a DSSA [6]. Larger mutual coupling between the storage loop and SQUID was desirable. At the same time, it was important to make the $L_{LC}$ products of the SQUID as small as possible for wider operating margins. Therefore, during the optimization, we kept the critical current of the SQUIDs to 0.10mA (the minimum value allowed in the fabrication process described below) and changed inductances.

3.2. Numerical results of a 4-stage DSSA and a 4-stage DDSA

Figure 4 shows numerical results of the bias current ($I_{bias}$) versus output voltage of a 4-stage DSSA and a 4-stage DDSA. Results for the SET state ($V_{OUT,SET}$) and RESET state ($V_{OUT,RESET}$) are plotted. The voltage of the DDSA is roughly twice of that of the DSSA. Figure 5 presents the bias current versus output voltage swing, the voltage difference calculated by subtracting $V_{OUT,RESET}$ from $V_{OUT,SET}$. (That is, $V_{swing} = V_{OUT,SET} - V_{OUT,RESET}$.)

**Figure 4.** Numerical results of $I_{bias}$ vs. $V_{OUT,SET}$ and $V_{OUT,RESET}$ characteristics of a 4-stage DSSA and a 4-stage DDSA.

**Figure 5.** Numerical results of $I_{bias}$ vs. $V_{swing}$ characteristics of a 4-stage DSSA and a 4-stage DDSA.
The maximum output voltage swing of the 4-stage DSSA and the 4-stage DDSA are 1.71 and 3.54 mV, respectively. The $V_{\text{swing}}$ ratio of the DDSA and DSSA is 2.07, as same as expected from the double-SQUID configuration. It is found in figure 5 that $V_{\text{swing}}$ becomes negative for $I_{\text{bias}}$ from 0.19 to 0.24 mA, which is because $V_{\text{OUT,RESET}}$ is greater than $V_{\text{OUT,SET}}$. (We did not pay any attention to such reversed magnitude relation during the parameter optimization.) When we assumed that the 4-stage DDSA worked correctly until voltage swing decreased 3 dB from those of maximum value, numerical simulation indicates that the 4-stage DDSA would work for the input signal up to 9.5 Gbps. This value is 95% of that of the previous work [6] listed in Table 1. Because we focused on the voltage swing of the 4-stage DDSA, high-speed performance was put aside during the parameter optimization. Competing goals for the large voltage swing and high-speed operation will be balanced in the future.

4. Experimental characteristics of a 4-stage DDSA

4.1. Layout design and chip fabrication

We designed a single DDSA stage in an 80 $\times$ 80 $\mu$m$^2$ area connectable to cells in the CONNECT cell library [14]. InductEX [15] was used for extracting inductances of superconducting lines and coupling coefficients. To increase the coupling coefficient between the storage loop and double-SQUIDs, a hole in the ground plane layer was introduced, resulting in the coupling coefficient $k$ of 0.73 in calculation.

For a test circuit, we designed a 4-stage DDSA, of which the configuration is shown in Fig. 6. The entire size of a 4-stage DDSA was approximately 680 $\times$ 1300 $\mu$m$^2$ including a dc/SFQ terminal.

![Figure 6. Configuration of the designed 4-stage DDSA with the measurement setup. The input SFQ frequency was set at 1 kHz.](image)

Test chips were fabricated by using the 2.5 kA/cm$^2$ Nb/AlO$_x$/Nb integration process (the STP2 process of National Institute of Advanced Industrial Science and Technology, Japan). Figure 7 shows a micrograph of one stage in a 4-stage DDSA.

4.2. Bias current–output voltage swing characteristics

In measurements, a test chip was cooled down in a liquid helium bath. Measurement setup is illustrated in Fig. 6. The output voltage swing was acquired with an oscilloscope via a 100-fold low-noise preamplifier.

Figure 8 shows the bias current versus the output voltage swing between the SET and RESET states ($I_{\text{bias}}$ vs. $V_{\text{swing}}$ characteristics). The circles and triangles in Fig. 8 represent
Figure 7. Photomicrograph of one stage in a 4-stage DDSA.

Figure 8. Experimental and numerical results of $I_{\text{bias}}$ vs. $V_{\text{swing}}$ characteristics of a 4-stage DDSA.

the experimental and numerical results, respectively. The maximum $V_{\text{swing}}$ was 2.93 mV in experiments, which was comparable with the corresponding numerical value of 3.54 mV. In addition, the experimental $I_{\text{bias}}$–$V_{\text{swing}}$ characteristics agreed well with numerical results, which indicated that the 4-stage DDSA worked as expected.

5. Conclusion
We designed and operated a 4-stage DDSA. A SQUID in the original DSSA was replaced with double-SQUIDs, by which two-fold output voltage was realized. One DDSA stage was designed to be $80 \times 80 \, \mu m^2$ and compatible with the CONNECT cell library. In experiments, the maximum output voltage swing was 2.93 mV, which was comparable with the corresponding numerical value of 3.54 mV.

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