ARGG-HDL: A High Level Python Based Object-Oriented HDL Framework  
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Abstract—We present a High-Level Python-based Hardware Description Language (ARGG-HDL), It uses Python as its source language and converts it to standard VHDL. Compared to other approaches of building converters from a high-level programming language into a hardware description language, this new approach aims to maintain an object-oriented paradigm throughout the entire process. Instead of removing all the high-level features from Python to make it into an HDL, this approach goes the opposite way. It tries to show how certain features from a high-level language can be implemented in an HDL, providing the corresponding benefits of high-level programming for the user.

Index Terms—Computer languages, Object oriented programming, Open source software, Runtime library

I. INTRODUCTION

ARGG-HDL is a library that allows the user to write Python code and convert it to VHDL (VHSIC-HDL, Very High Speed Integrated Circuit Hardware Description Language). This document shows three of its defining features. Firstly ARGG-HDL is fully object oriented, which allows the user to create high-level objects. This Object Oriented approach allows the users of the library to express their intentions in a cleaner manner, which can result in much cleaner code. Secondly, it allows the user to write very generic code. This reduces the amount of code duplication. Due to its high-level templating mechanism, it can be used to write highly generic code. Thirdly, it uses a preexisting language, which allows the user to use the already well known and very powerful tools, which are provided in the Python language. Instead of having to learn both digital logic design practices AND a completely new language, the user only has to learn a few extensions provided by this library.

A. Competing Approaches

The idea of generating firmware from a high-level programming language is certainly not new; in fact some of these approaches have been around for decades. So far there exist at least 30+ approaches for High level Synthesis (HLS) and firmware generation, but what sets ARGG-HDL apart from the others is its high level approach to writing low level firmware. If compared to, for example, "VivadoHLS," it is clear that "VivadoHLS" provides very strong support for generating algorithms out of existing c/c++ code and porting them over to firmware, but the code written in c/c++ has very little resemblance to the firmware generated. In fact most of the time the generated code will only be used as a black box IP core. For many applications this is a solid approach but in cases where one still wants to have the low level control over the actual implementation it is difficult to achieve that. Here ARGG-HDL can really shine because it allows the user on one hand to write the firmware as low-level as is necessary to fulfill the task, and on the other hand gives a clear path of integrating high level features into the design. Another popular code generation tool is "MyHDL." It allows the user to write firmware in Python. This is a task it does very well but in doing so it loses many of the features that make Python a high-level programming language. Most noticeable here is classes. It provides rudimentary support for grouping signals together in containers but this is the highest level of abstraction that one can achieve. With ARGG-HDL classes are a core part of its design, furthermore ARGG-HDL sees itself as a platform for the user to create their own abstractions on-top of the existing ones. As shown later in this document virtually every behavior of the library can be customised for individual classes.

II. OBJECT-ORIENTED DESIGN

Object-oriented Design has been the foundation of virtually all modern programming languages. Object-Oriented design has been proven excellent at hiding complexity. Humans are able to use extremely complicated technology, such as computer chips, since its complexity is hidden inside powerful abstractions, which reduce its complexity to just pushing buttons.

A. Programming in VHDL without objects

Listing 1 shows a typical example of an entity declaration in VHDL. The entity declared on 1 is a queue or "First in First out" (FIFO) module (see figure 1). A FIFO consists of two sides. The data input side and the data output side. In order to stay synchronized each side provides three signals. For the Data Input side these signals are: write data, write enable, and full. For the correct use of this FIFO, it is crucial to handle these signals precisely according to specification. Yet when we look at the entity declaration the only thing that reveals which signals belong to which side of the FIFO is a vague naming convention. VHDL has no concept to describe these three signals belonging to one interface. A main reason for this is that each port has to be defined as an input or an output. Therefore it is not possible to make a record with these three signals. In this case the entire record and all its signals, would either be an input port or an output port.

Figure 2 shows, how two entities communicate with each other using three signals. As can be seen, it is not obvious that these three signals actually define one interface. The only thing that reveals this information is a naming convention. Inside each entity, the signals are also handled loosely. Their
**entity** FIFO_cc **is**

```vhd```
  generic(
    DATA_WIDTH : natural := 16;
    DEPTH : natural := 5
  );

  port(
    clk : in std_logic;
    rst : in std_logic;
    din : in std_logic_vector(
      DATA_WIDTH-1 downto 0);
    wen : in std_logic;
    ren : in std_logic;
    dout : out std_logic_vector(
      DATA_WIDTH-1 downto 0);
    full : out std_logic;
    empty : out std_logic
  );
end FIFO_cc;
```

Listing 1. Typical declaration of a FIFO with a native interface [5]. As shown in Figure 1, the FIFO consists of three signals handling the writing of Data to the FIFO (din, wen, full) and three output signals (dout, ren, empty). The only hint that the user has on how to use this FIFO is a naming convention. But of course a naming convention does not communicate the timing behavior of the interface. Compared to the more modern AXI4-Stream the native FIFO interface has the additional disadvantage of having two different interfaces for the data input side and the data output side.

Properties are usually checked/set at very different stages of the program. Therefore, the user code and the interface code are completely intermingled. This can get unmanageable quickly and leads to the typical "write only code", that is seen so often in VHDL.

**C. The Basics**

To start with ARGG-HDL a prior knowledge of any hardware design language is not required but, if possible, the names used to describe certain constructs are chosen to be similar to VHDL, therefore user with a VHDL background will find the overall structure familiar. Listing 2 shows a simple example of a counter. The Example starts by creating a class which inherits from "v_entity" this marks the object as an entity object. V_entities work very similar to to entities in VHDL. In our example the entity has no ports and defines only one function, the "architecture" function. Similarly to the architecture body of an entity in VHDL this contains the internal structure of the entity. Inside the architecture function the first thing that we create is a clock generator. The clock generator is derived from v_entity object itself. It has one (public) member which is the clock. Since it is a normal Python object the clock generated by the entity clock generator can be accessed like any other member of a Python class with "clkgen.clk". After this two signals are being created. One is the counter, the other one is the maximum value to which the counter should count. Both of these signals are of the type "v_slv(32)" which translates to a 32 bit standard logic vector. The second argument in "max_ent = v_slv(32,300)" is the default value. Since this is ordinary Python code the initial value could have been given in hexadecimal as well. The default initial value is zero. The next construct is a function definition "def proc():" which is modified by a decorator "@rising_edge(clkgen.clk)". This special decorated function that is generated here and appends it to the "on_change" list of the signal it received as an argument "clkgen.clk". But instead of executing on ever signal changed this decorator makes sure that it is only executed on a rising edge. Once the simulation has started the function "proc" gets executed on every rising edge of the signal "clkgen.clk". The
function proc does three things. First it increments the counter signal by one. For this it uses the stream (bit-shift) operator. The idea is that the new value gets stream into the existing and persistent object. Since the object might be connected to other object it is important that there is no new object generated but the existing object is modified. Similar to C++, ARGG-HDL uses the stream operator to stream data into objects (signals). In addition to the left shift operator (stream in operator) there is a right shift operator (stream out operator). Future examples will show them in action. Next, the counter is compared to max_cnt and if it is bigger or equal it is then set to zero again. The last statement is "end_architecture()" which handles some book keeping such as giving all the signals the correct name etc. It needs to be executed at the end of the "architecture" block.

On the use of streamer (bit shift) operators: In other programming languages, such as C++ overloading the streamer (bit-shift) operator to send data into an object (or read from it) has been part of the language for decades. It is a clear way of communicating to the user that this object is not replaced with a new object but its content is modified. Of course it would be possible to use a "next" function (or property) to achieve the same behavior. In the end it is a matter of taste which style one prefers but overall using the streamer (bit-shift) operator gives a very natural indication of data flow.

On variables and signals: ARGG-HDL allows you to define signals as either variable or signal. However since this "variableness" and "signalness" is part of the object definition there is no need for two separate assignment operators. The streamer (bit-shift) operator will work on both types.

1) Communication between Entities with Classes and Application Programming Interfaces (API): In ARGG-HDL the interface is defined as an object (see figure 3). The interface object contains all three signals as well as their directionality. Each entity has one port for the entire interface. This way it is clear that, these signals belong to one interface. Instead of defining a port as either input or output, the port are defined as either primary or secondary. In a primary port, the signals have the directionality defined in the interface class. In a secondary port, the directionality is flipped.

Inside the entity the interface is handle by a handler class. This class contains the API for interacting with the interface. Thereby, the user code and the interface code is separated. This makes it easier to write clean code that is easily understood. In addition, since the user never directly interacts with the interface signals, the interface author can ensure that the interface is used correctly.

2) Example: Clocked Entity sending data via AXI4-Stream

A clocked entity sends data via AXI4-Stream using the stream interface. Since it is a data source, it uses the "port primary" version of the interface. On the architecture level it first defines a handler object called "data out", which handles the interaction with the interface. The handler is used inside the process block. The process block is executed on every rising edge of the clock. Inside the process block the handler is first checked with the "if statement". Since the handler class is a high level object the author has the possibility to overload the "bool" function, which is called inside the test block of the "if" statement.

This allows for expressive code. If the bool function of the interface handler returns true, the interface is ready to use. Since the interface class has only one purpose, it is immediately clear what this statement means. It means that the interface is ready to send data. On the next line, the data can be assigned to the handler object, which is equivalent to calling the send data function. The user of the library never needs to know the internal structure of this interface nor does the user need to know the protocol for sending data. The users can always be sure that, as long as they are only using the functions provided by the API, the interface will always work correctly.

3) Example: Interface Class: How the interface class works is now described. Shown in Listing 5 is the interface class for an AXI4-Stream interface with a data width of 32 bits. It defines all signals it needs to operate. It sends from primary to secondary the following signals: valid, last and data. From secondary to primary it sends the ready signal. Primary and secondary are defined relative to the data flow. The data flows from primary to secondary.

4) Example: Interface Handler Class: Listing 6 describes how the interface handler class works, the interface class has to inherit from an ARGG-HDL base class called "v_class_primary". The constructor takes one argument, which
from arghhdl import *
from arghhdl.examples import *
class Counter(v_clk_entity):
    def __init__(self, clk):
        super().__init__(clk)
        self.Dout = port_out(axiStream_32())
        self.architecture()

@architecture
def architecture(self):
    data = v_slv(32)
data_out = get_handle(self.Dout)

@rising_edge(self.clk)
def proc():
    if data_out:
        data_out << data
        data << data + 1

Listing 4. Instead of defining individual inputs and outputs, an interface object is defined. The object “axiStream_32” contains all information about input and output signals. The object brings a handler with it. The handler is used for communication with the interface. The handler provides the API for the interface. The user never directly interacts with the data members.

is the interface class. Then defines a variable port of that type and connects the two objects together. Note that since these two object, “axi_out” and “TX”, are objects they know exactly which signal has to go in which direction in order to make the interface work. The handler class defines three additional functions. First is the send data function. It takes any data it receives and sends it out through the interface class. In addition, it also sets the steering signal “valid” to high. The second function is the “ready_to_send” function. It is used to check if the interface is ready to send new data. The interface is only ready to send data if it is not already sending data. Therefore, the “valid” signal needs to be low in order to send more data. The third function is the “on Pull” function. This function is called on every clock cycle at the beginning of the process block. In this case, it checks if the “ready” signal send from the secondary is high. If yes, it means that the secondary has read the current data and is ready to receive new data. If the ready signal is high, the steering signals can be reset and new data can be sent.

5) Example: Entities are Objects: Entities are themselves objects, therefore each port of an entity can be accessed as a member variable of this object. The example in Listing [7] shows how different entities can be connected together. Inside the architecture block of the entity, we first create a clock generator entity. The instance is called “clkgen”. The instance has an output port “clk”, which can be accessed like any other member variable in Python. We use the clock provided by “clkgen” in the constructor for the other entities. Now that we have created the entity “cnt” (short for counter) and “axiPrint” we can connect its signals together. We do this by simply assigning the output of the counter to the input of the “axi print” object. Since the interface is an object itself, it knows exactly which signals have to go in which direction. The signals do not need to be repeated on the test bench entity. Everything is contained inside the entities themselves.

class axiStream_32(v_class_trans):
    def __init__(self):
        super().__init__()
        self.valid = port_out(v_slv(32))
        self.data = port_out(v_slv(32))
        self.ready = port_in(v_slv(32))

Listing 5. This class describes the signals required for the interface. In addition to just storing the type of the data, it also stores the direction of the data. By definition, data flows from primary to secondary. port_out defines a signal that goes from primary to secondary. port_in defines a signal that goes from secondary to primary.

class axiStream_primary(v_class_primary):
    def __init__(self, Axi_Out):
        super().__init__()
        self.tx = variable_port_out(Axi_Out)
Axi_Out << self.tx

def send_data(self, dain):
    self.tx.valid << 1
    self.tx.data << dain

def ready_to_send(self):
    return not self.tx.valid

def onPull(self):
    if self.tx.ready:
        self.tx.valid << 0
        self.tx.last << 0

Listing 6. This class handles the primary(source) side of the interface. The constructor takes the Interface class as argument. It makes a local copy in a variable. It connects the local copy to the Input argument. The object knows exactly which signals have to go in which direction. The onPull functions allows the creator of the interface class to inject functionality on every clock cycle (before the user’s code).

class tb(v_entity):
    def __init__(self):
        super().__init__()

@architecture
def architecture(self):
    clkgen = clk_generator()
cnt = Counter(clkgen.clk)
axPrint = Axiprint(clkgen.clk)
axPrint.D_in << cnt.Dout
end_architecture()

class Axiprint(v_clk_entity):
    def __init__(self, clk):
        super().__init__(clk)
        self.D_in = port_in(axiStream_32())

Listing 7. Axiprint is an entity that prints out the values of the stream. It uses the same interface class as “Counter” but since it wants to consume the data it is a secondary port. In order to connect “Counter” with “Axiprint” the Data_in / Data_out Member needs to be connected. Since the interface class knows which signal goes in which direction the signals can just assigned to each other.
D. Example: Pipe Lines

A common approach to data processing is to subdivide the task into different stages. For example we start with a data source, which first needs to get stored in a FIFO, then filtered, then modified, and lastly sent to another module somewhere else. Many programming languages have for these kind of tasks a special operation: the so-called pipe line operator. Most languages use the bitwise "or" operator as the pipe operator. ARGG-HDL also uses the bitwise "or" operator "—".

1) Example: stream_delay_one Pipe Line: The example in Listing 8 shows how one can use this pipeline operator.

Creation of a new entity, one has simply to replace the "port_primary" keyword with the "port_stream_primary" keyword. This creates a new primary port, which will be used for the pipeline operator. In the same way does the "port_stream_secondary" port defines a secondary port, which is used for the pipeline operator. There can only be one of each type. The purpose of the entity shown in this listing is to delay the data from an AXI4-Stream by one clock cycle.

E. Classes: Combination of Data and Functions

Let us have a deeper look into classes. Classes are usually thought of as the combination of data and functions. That means they can contain both member data and member functions. Hardware Description Languages (HDL), usually to deal with many different types of data, and functions. For example, there are variables, signals and ports. In addition to normal functions, HDLs have to deal with functions, procedures, processes, and entities. In order for an object to be a fully high-level object, it is mandatory that classes in ARGG-HDL are able to contain all these different parts of the language.

1) Example: Class with Variables and Signals: Classes that contain variables, signals, and combinatorial logic (asynchronous push/pull functions) are useful for defining interfaces to other entities. In the example, shown in figure 5 we want to access a FIFO with a native interface. This specific FIFO requires the enable signal to be always zero if the empty signal is high. It needs to be done immediately and cannot wait for the next clock cycle; therefore, it needs to be done asynchronously. In ARGG-HDL it is possible to encapsulate all this complexity inside the interface handler class. The user of the class does not need to know that there is any additional logic. In fact, if the author of the classes uses the same public API, the user can switch back and forth between both types of interfaces without having to change the code.
A simplified version of this handler class is shown in Listing 10. As shown, it defines three sets of interface object: "rx", "rx1" and rx2. The interface object "Data_In" is connected to the signal "rx2". The qualifier "free_type" prevents this object from becoming part of the "NativeFIFO_in" signal record. This is necessary since a signal needs to have only one driver and the driver for (parts) of these objects is going to be in combinational block. The Signal "rx1" is connected to the variable port "rx". The connection between "rx1" and "rx2" is done in the combinational block inside the architecture function of the "NativeFIFO_in". Functions marked with combinational are executed as soon as one of their captured objects changes. The first statement of the combinational block is the conditional assignment of "rx2.enable". The first argument to the switch statement is the default value which is used when non of the cases match. There always needs to be an default statement. The second argument is a list cases. The first argument to the combination block the variables and signal records are given to the procedure with read and write access (inout).

**III. GENERIC PROGRAMMING**

The next feature any language needs in order to be considered a high-level language is generic programming. Even though VHDL provides a limited amount of generic programming it falls short when compared to a high-level language. Given the dynamic nature of Python it naturally provides possibilities for very generic programming. ARGG-HDL tries to preserve the generic programming model from Python as much as possible.

**A. Example**

1) Example: Interface Classes: Using templates in ARGG-HDL works very similar to Python. Listing 11 shows the actual implementation of the interface class for an AXI4-Stream interface. The data type is an argument to the constructor of the class. The data type can be every plain type, that includes standard logic vectors of different sizes, integers etc. In addition, it can also be records and arrays. For every new data type, the templating mechanism will create a new class.
### Example: Interface Handler Classes

In addition to the class itself being a template, all its member functions are templates too. This means that as long there is a valid assignment from "dataIn" type to "self.tx.data" in Listing 12 this code will compile and it will work.

Listing 11 shows a practical example of a member function template. We see the secondary handler class of an AXI4-Stream. Its purpose is to readout the data received. The data are first stored in an internal buffer. The readout can be done with the right shift/stream out operator. The first thing the function does is it resets the output object. Then it checks if the internal buffer has data. If the internal buffer has data, the data is then written to the output object. This function is clearly written for the case when the data output type is of the exact same type as the internal data type. But since it is a template it accepts any type that has a valid assignment operator for this data type.

A practical use case is shown in Listing 13. It shows a test bench with a counter as a data source and one process block, using the data. As described before the stream out operator is a template, which means, it accepts every type that has the following two features. Firstly, it needs to have a reset function and secondly it needs have an assignment operator that accepts this data type.

### Class Definitions

```python
class axisStream(v_class_trans):
    def __init__ (self, Axitype):
        super().__init__ ()
        self.valid = port_out (v_sl ())
        self.last = port_out (v_sl ())
        self.data = port_out (Axitype)
        self.ready = port_in (v_sl ())

Listing 11. For the actual implementation of the AXI4-Stream interface class the data object is a template variable. For each new data type the templating machine will create a new class. Data type can also be records and arrays.
```

```python
class axisStream_sender(v_class_primary):
    def __init__ (self, AxOut):
        self.tx = variable_port_out (A xiOut)
        A xiOut << self.tx

    def send_data(self, dataIn):
        self.tx.valid << 1
        self.tx.data << dataIn

Listing 12. Also the handler classes are templates. In addition to the class being a template so are the member functions. That means as long as the assignment operator is defined for the types: of "self.tx.data" and "dataIn" it will work.
```

```python
class axisStream_receiver(v_class_secondary):
    def rshift (self, rhs):
        rhs.reset ()
        if self.data_internal_isvalid2:
            rhs << self.data_internal2
            self.data_internal_was_read2 << 1

Listing 13. AXI4-Stream receiver handler stores the data received by the AXI4-Stream first internal before the user can extract it. If the handler does not have any data it will just reset the output object and nothing else. The output object must either be of the same time as the stream data Or must be of a type that accepts the data type as input.
```

```python

class tb(v_entity):
    def __init__(self):
        super().__init__ ()
        self, architecture ()

@architecture
    def architecture (self):
        clkgen = v_create (clk_generator ())
        cnt = v_create (Counter (clkgen.clk))
        cnt.out = get_handle (cnt.Data_out)
        data = v_slv (32)
        opt_data = optional_t (v_slv (32))
        @rising_edge (clkgen.clk)
        def proc ():
            cnt.out >> data
            cnt.out >> opt_data

end architecture

Listing 14. Optional_t is a generic container that stores data of a certain type, as well as a bit that indicates if the data is valid or not. cnt_out is an instance of a counter entity which uses the AXI4-Stream interface. It is written long before optional_t. Since optional_t has a reset function and an assignment operator that accepts this data type it will work.
```

![Fig. 7](image-url) This picture shows the result of the simulation of Listing 14. It shows how the AXI4-Stream handler class interacts with the two different objects (data and opt_data). The "data" object is a standard logic vector. The "opt_data" object is and optional data object. This means it has an extra bit which indicates if the data is valid or not. When reading out data from an AXI4-Stream interface using the right shift (stream out) operator the target is first reset, then the handler checks if it received data and only if it has received data it will write the data to the target. In red the raw AXI4-Stream input is shown. One can see that every N clock cycle a new value is sent. On reset the standard logic vector sets all bits to zero. If no new value was received the "data" object will remain zero. The "opt_data" object sets on reset only the valid bit to zero. As one can see from the picture both "data" and "opt_data" get set correctly to the new value as soon as it is received. This shows that even different data types can be set correctly by the AXI4-Stream interface handler as long as they provide a compatible set of public interface functions.
IV. ARGG-HDL IS NOT A LANGUAGE, IT IS A LIBRARY

A. Seamless integration with other Python libraries

When designing ARGG-HDL the question came up to either make it a completely new language, make it a precompiler for VHDL or use a preexisting high-level programming language. By considering the unfeasible amount of work that would be required to build just the precompiler, it became clear that the only reasonable solution was to use a preexisting language. Therefore ARGG-HDL is not a language it is a library. This gives it instantly access to all the high quality tools that are available for Python. Since Python is cross platform, simulations in ARGG-HDL run on any platform that supports Python. For the simulation, all libraries that are available for Python can immediately be used with ARGG-HDL. This includes all the powerful data visualization libraries such as ”Matplotlib”, ”Plotly” etc. The same is true for file access. Python has very powerful libraries when it comes to file IO. For example, currently it uses the library PY VCD for writing “variable change dump” files. However, it could easily make use of the ”Pandas” library. Alternatively, if necessary the data could be stored in a ”TTree” from the CERN ROOT library. All these powerful libraries are just one pip install away.

In addition, Python has a rich ecosystem of editors and tool chains. Virtually all editors support features such as auto completion, step debugging, data visualization etc. Furthermore, Python already has a packaging system in place. That means, if one wants to share code with the world it can be uploaded to PyPi. This will not only take care of the distribution of the library itself but will also take care of the dependencies.

One of the many features that are instantly available for ARGG-HDL is, for example, plotting the connection diagram in real-time while running the program (see figure 8).

B. Co-Simulation

Python is known for its outstanding integration to other languages. Virtually all modern programming languages have the possibility to interact with Python. The official Python website has examples on how to connect Python to other languages for 15 different languages, such as C/C++, Java, .Net, and Haskell. Further more Python provides support for inter-process communication such as network sockets. Especially the support for network sockets and TCP/UDP communication allows the user a straight forward integration of the co-simulation. A common mode of communication between PC and FPGA is the TCP or the UDP protocol. In this scenario the FPGA can be mimicked by a Python simulation of the firmware which listens on the address/port instead of the FPGA.

V. CONVERSION TO VHDL

The conversion from Python to VHDL is separated into different steps. In the first step the entity that should be converted needs to be instantiated. During the instantiating process all the connections between the individual signals entities and classes are created. At this point the entity would be able to run as a simulation in Python. The entities and all sub-entities have been instantiated at least once. Only objects that are currently instantiated get translated to VHDL. The library has a shadow register which contains all ARGG-HDL objects that are created during one session. In the next step it starts looping over all objects that have been created.

In order to allow the user of the library a more granular control over the conversion to VHDL every part of the conversion can be modified. In the end, the Python code and the VHDL code can be made completely independent of each other. For this, every VHDL file is subdivided into the blocks shown in figure 9. Every object in ARGG-HDL has the option to modify any of these blocks.

A. The different stages of the conversion

The Conversion is subdivided into three stages (see figure 9). Firstly parsing of the Python source files. This is done with a standard Python library called AST. It is part of the reference implementation of CPython. Second, the ARGG-HDL visitor, in order to traverse the AST, ARGG-HDL has its own visitor class. This class does not only traverse through the syntax tree but also carries all the context information. For example, it contains a list of all the functions and variables that are defined in this context. In addition, it stores information about the environment, for example if the code that is currently looked at is a process, function, procedure, etc. It then make the decision which function to call from the ARGG-HDL object converter. It is important to note that the visitor itself does not make any conversion it just calls the function from the ARGG-HDL converters. Last is the ARGG-HDL object converters.
Fig. 10. Every object in ARGG-HDL has a meta object which handles the conversion to VHDL. For consistency the object and the meta object has the same inheritance hierarchy.

Fig. 11. Any VHDL file consists of the blocks shown above. Each ARGG-HDL object has a function overload that can inject code at any of these location. The Python code and VHDL code can be made completely independent of each other (if necessary). Each Object can overload this function. Each function has a default but can be freely modified.

Each object possesses its own converter, which defines how it is supposed to be converted to VHDL. This converter also defines how each interaction with the object is converted. This gives the user a very granular way of defining how the object will converted to VHDL. In addition, its modular design makes it very easy to replace one set of object converters for another set, which would allow a conversion to, for example, Verilog or even C++.

**B. The ARGG-HDL object Converter**

In ARGG-HDL each object has a member called hdl_converter. This object contains all the code for the conversion to VHDL. As shown in figure 10 the hdl_converter objects follow the same inheritance hierarchy as the the objects themselves. This gives a consistent behavior. The actual working of the converter is understood with a practical example. The code in Listing 15 shows the visitor for the assignment operator. The first thing it does is it unfolds the arguments. Where "rhs" stands for right hand side and is the source of the assignment and "lhs" stands for left hand side, and is the target of the assignment. Once this is done the visitor asks the target what type it expect. Next it calls the "getValue" function of the hdl_converter. This function will return the "value object" of the target object. In the last step it calls the "reassign" function of the target. This is the generic part, it will be called for any assignment operation that is found in the conversion. In the next example we see a practical implementation of this.

Example: Assigning AXI4-Stream secondary handler to AXI4-Stream primary handler. In this example, the "getValue" function of the hdl_converter of the secondary handler is worth a deeper look. It is clear that the user of the class wants to assign the data value to the target. In order to extract the data from the AXI4-Stream secondary handler one has to call "read_data" function and assign the value to a variable. Since this function needs to modify the handler object and the function cannot modify the input, this function needs to be implemented as a procedure. Procedures can modify the input but cannot have a return value. This unnecessary limitation of VHDL can be overcome by creating a custom "getValue" function for the hdl_converter

Listing 15. ARGG-HDL AST visitor for value assignment (simplified).

```python
def body_LShift(self, Node):
    rhs = astParser.Unfold_body(Node.right)
    lhs = astParser.Unfold_body(Node.left)
    rhs = rhs.__hdl_converter__.reassign_type(lhs)
    return lhs.__hdl_converter__.getValue(rhs, lhs, astParser)
```

Listing 16. ARGG-HDL object hdl_converter for assigning a new value to an object (simplified).

```python
def reassign(self, obj, rhs, astParser=None):
    asOp = obj.__hdl_converter__.get_assignment_op(obj)
    return target + asOp + str(rhs)
```

Example: std_logic_vector (SLV) assigned to SLV. Since it is already a primitive type "reassign_type" will just return the object itself with no changes done. The same is true for "getValue". It will just return the object itself with no changes. Lastly the "reassign" function connects these two objects together. A simplified version of the "reassign" function is shown in Listing 16. It shows that in this case it converts the assignment from Python into VHDL. The only thing it needs to do is to extract the correct assignment operator. Depending on the target being either a variable or a signal, the operator has to be either ":=" or "::=".

Listing 17 shows a simplified version of the "getValue" function from the hdl_converter of the AXI4-Stream secondary handler. First it creates a name for a variable that will be used to buffer the data. On the next line it tries to get the variable from the list of defined variables. This is done to not create more than one of these buffer variables. If no variable with that name could be found the function returns "None". In this
def getValue(self, obj, ReturnToObj, astParser):

    vhdl_name = str(obj) + "_buff"
    buff = astParser.try_get_variable(vhdl_name)

    if buff is None:
        buff = v_variable(obj.rx.data)
        buff.__hdl_name__ = vhdl_name
        astParser.LocalVar.append(buff)

    hdl = obj.__hdl_converter__.call_member_func(
        obj, "read_data", [obj, buff], astParser)

    if hdl is None:
        astParser.Missing_template=True
        return "$missing_template$"

    astParser.AddStatementBefore(hdl)
    return buff

Listing 17. Shown is the getValue function of the AXI4-Stream secondary handler.

case we enter the "if" statement. In this we create a variable of the same type as the data. The new variable does not have an name yet. It receives it name on the next line. On the last line of the "if" statement we append this variable to the local variable list (process/function scope).

After the variable is successfully created we can use it to readout the AXI4-Stream secondary handler. This object is readout with the "read_data" function. This function takes two arguments. The handler object itself and the output buffer variable. The function "call_member_func" implements a member function call with the given parameters. Since functions are usually templates in ARGG-HDL, it is possible, that on the first call of the function the required function has not yet been created from the template. In this case the function return "None". In this case the conversion was not successful therefore this function has to inform the "astParser" that there is a template missing. This means that this object will be added to the conversion queue again and will be reprocessed once all the other objects have been processed. By then the necessary function will be created and it can be used. In this case the function that was just generated will be added as a statement before the current statement. The return of this getValue function is the buffer variable. With this trick it is possible to create functions in ARGG-HDL that modify the input as well as having a return type.

For completeness Listing 18 shows the implementation of the "reassign" function of the AXI4-Stream primary handler.

def reassign(self, obj, rhs, astParser):
    ret = obj.__hdl_converter__.vhdl__call_member_func(
        obj, "send_data", [obj, rhs], astParser)

    if ret is None:
        astParser.Missing_template=True
        return "$missing_template$"

    return ret

Listing 18. Shown is the reassign function of the AXI4-Stream primary handler.

VI. CONCLUSIONS

This document has shown that features from high-level programming languages can be ported to firmware development.

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